Test and characterization of 3D high-density interconnects

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Test et caractérisation des interconnexions 3D haute densité

Test and characterization of high-density 3D interconnects

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Acronyms

3D-IC: Three-Dimensional Integrated Circuit
ATPG: Automatic Test Pattern Generation
Ball Grid Array (BGA)
BEOL: Back End Of the Line
BIST: Built In Self Test
BSC: Boundary Scan Cell
BSR: Boundary-scan Register
CIS: CMOS Image Sensors
CMOS: Complementary Metal Oxide Semiconductors
D2W: Die to Wafer
DFT: Design for Test
DWR: Die Wrapper Register
F2B: Face to back
F2F: Face to face
FDSOI: Fully Depleted Silicon On Insulator
FEOL: Front End Of the Line
FPGA: Field Programmable Gate Array
HB: Hybrid Bonding
ICL: Instrument Connection Language
IJTAG: Internal Joint Test Action Group
JTAG: Joint Test Action Group
KGD: Known Good Die
KGS: Known Good Stack
PDL: Procedural Description Language
RF: Radio Frequency
SI: Scan Input
SIC: Stacked Integrated Circuit
SIP: System In Package
SO: Scan Output
SOC: System On Chip
SVF: Serial Vector Format
TAM: Test Access Mechanism
TAP: Test Access Port
TCK: Test Clock
TDI: Test Data Input
TDO: Test Data Output
TMS: Test Mode Select
TRST: Test Reset
TSV: Through Silicon Via
W2W: Wafer to Wafer
WBR: Wrapper Boundary Register
WIR: Wrapper Instruction Register
WPI: Wrapper Parallel Input
WPO: Wrapper Parallel Output
WSC: Wrapper Serial Control
WSI: Wrapper Serial Input
WSO: Wrapper Serial Output

Chapter I. Introduction

I. General context

Moore's law is the observation that the number of transistors per unit area doubling about every two years. The rate now is at the limits of physics, TSMC (Taiwan Semiconductor Manufacturing Company) can already scale its process to 5nm Fin Field-Effect Transistor (FinFET) [1]. Beyond that, miniaturization is very difficult and faces a lot of technological and physical issues. So, a new concepts are needed to overcome the technology limitations for CMOS scaling.

In 2000s, a new concept named "More than Moore" has thus appeared in order to extend Moore's Law and to enhance the overall chip performances. Figure 1 shows the different scaling directions to enhance system performances. This new "More than Moore" concept consists on vertical stacking; associate in single chip diversified integrated circuits such as analog/RF, passive, sensors, digital, biochips… This kind of integration is called Three-Dimensional (3D) integration which consists on the fact of stacking various functional blocks in a vertical way in order to form a single chip with high performances.

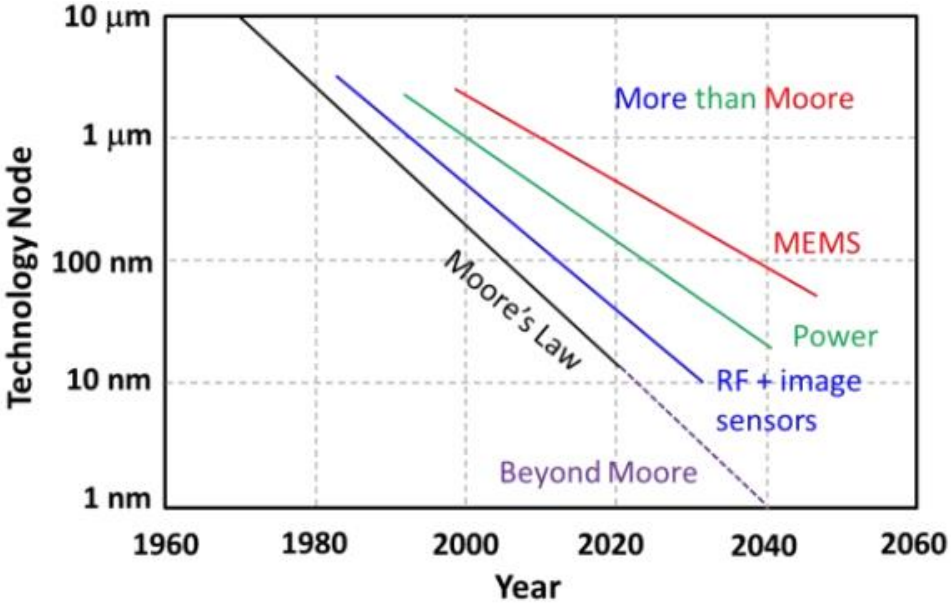


Figure 1: Evolution of More-Moore and More-than-Moore (source [2])

The 3D interconnect technology landscape was illustrated in figure 2 .The graph represents the various 3D integration approaches with respect to the achievable 3D interconnect density and pitch [3]. The first vertically stacked circuit was the system in package (SIP) using wire bonding technology or Ball Grid Array (BGA) technique (Package-On-Package (POP) stacking) with a contact pitches in the order of 400µm [4].

Afterwards, the 3D Stacked Integrated Circuit (SIC) appeared thank to a new bonding technique that is based on TSVs (Through Silicon Vias) and µ-bumps interconnects, Coarse contact pitches in the order of 20µm can be achieved [5]. Copper-to-copper (Cu-Cu) Hybrid Bonding (HB) technology is another alternative for System-On-Chip (SoC) implementation to scale the contact pitch down to 2µm [6].

The 3D connections are achieved by direct bonding of top and bottom dies/wafers using copper contacts on top of each metal layer stack and TSVs connect the lowest metal layer to backside solder bumps. Next come 3D sequential integration, also named 3D monolithic integration, consists in stacking active device layers on top of each other in a sequential manner to achieve a contact pitch below 100nm [7].

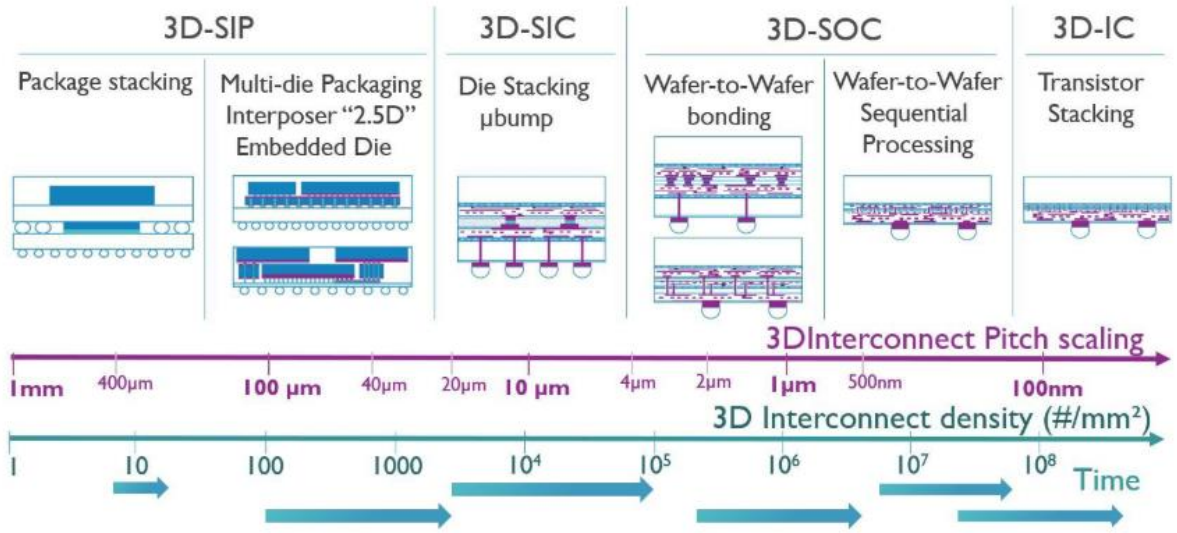


Figure 2: Evolution of 3D integration (source [8])

3D-ICs can be stacked in two major options: wafer-to-wafer (W2W), die-to-wafer (D2W) (Figure 3).

- W2W stacking consists on bonding a wafer on the top of another wafer and requires having the same size of dies. W2W stacking offers high throughput to address the needs of several applications such as smart imagers [9]. However W2W stacking is limited when talking about exploiting Known-Good Die (KGD) test results.
- Die-to-wafer (D2W) stacking consists on bonding a die on the top of a wafer. This assembly approach address the needs of several applications such as High

Performance Computing (HPC) [10] and it is advantageous for yield reasons (Known-Good-Die) and to integrate different sizes dies from different manufacturing lines.

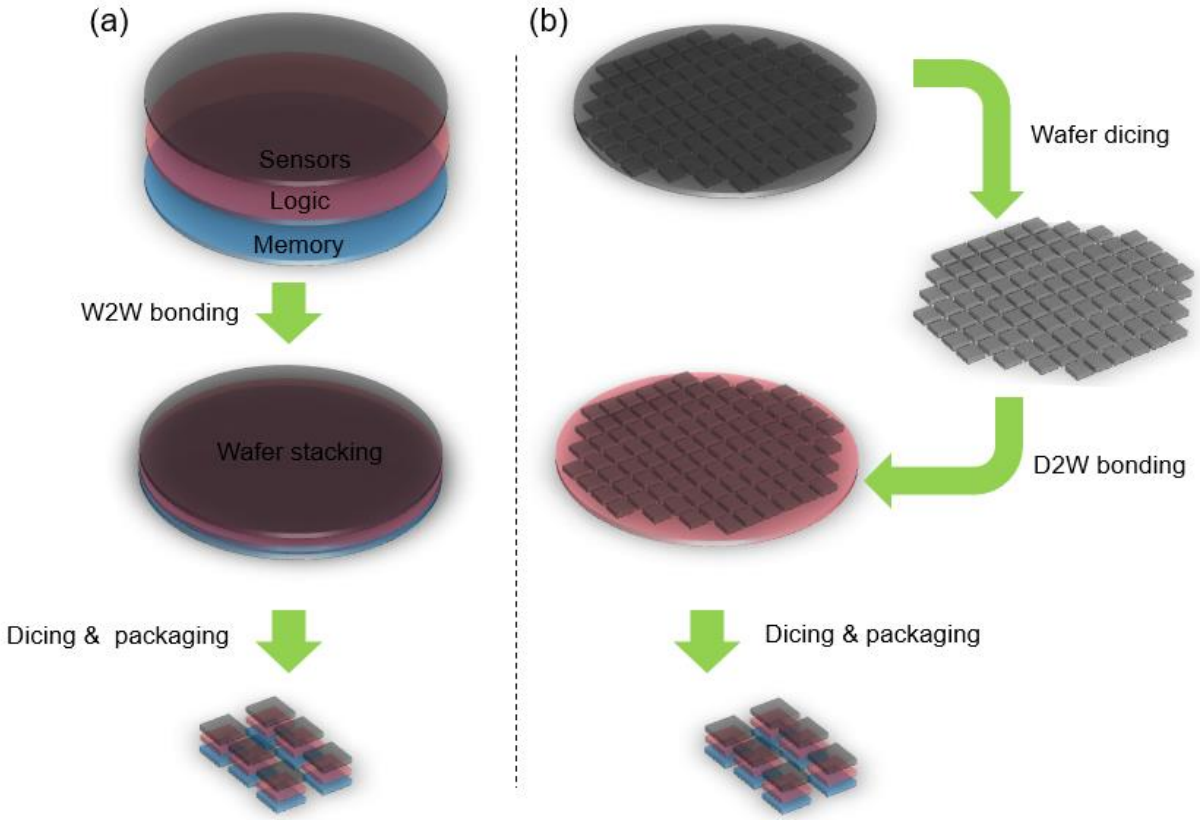


Figure 3: 3D stacking options: (a) W2W, (b) D2W

In this thesis work, we focuses on fine pitch interconnects, that optimize performance of 3D-IC by integration of fine grained architectures. The functional units are vertically stacked using inter-die interconnects like µ-bumps or Cu-Cu interconnects and intra-die interconnects Through Silicon Vias (TSV). 3D stacking integration has been providing an alternative to:

- Reduce the interconnections length and associated RC delay
- Integrate heterogeneous and homogeneous integrations
- Offer a small form factor
- Integrate different technology nodes
- Reduce power consumption

II. High-Density 3D-IC interconnects

1. Overview

Current high-end electronics consist of advanced 2D system-on-chips (SoC) stacking onto each other – usually named by 3D stacked ICs. This 3D integration has been driven by economically and technically attractive viewpoints for further developing high performance systems. However, the semiconductor industry is continuously demanding products with higher integration density, higher performance, lower power consumption and reduced cost.

Compared to µ-bumps integration, that face major challenges to go beyond 10µm pitch due to pattern processing complexity, stacking alignment accuracy and stable solder material, Cu-Cu direct bonding technique is more promising for fine pitch and high density interconnects [11] (Figure 4).

Cu-Cu hybrid bonding is a direct bonding technology which obtains metal-metal bonding and dielectric-dielectric bonding simultaneously and provides a solution for scaling below 10µm pitch with improved physical as well as an efficient 3D connection between processors and memories, digital and analogue circuits and MEMS co-integration [12].

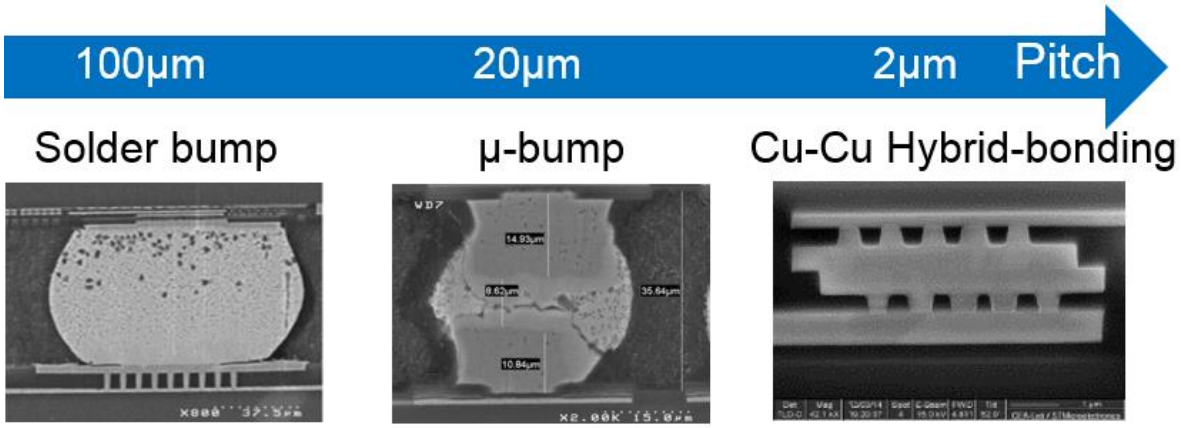


Figure 4: Evolution of inter-dies interconnects

2. Cu-Cu hybrid bonding interconnects

Figure 5 presents an example of high density 3D-IC using F2F bonding technology (Figure 5.a); the wafers/dies are connected thanks to Hybrid Bonding Metal pads (HBM) and Hybrid Bonding Vias (HBV): for both dice, HBV connect the top metal layer to the Cu-pads. The lowest metal layer of bottom die is connected to backside bumps using larger TSVs. Compared to conventional wire-bond chip interconnections, TSVs offer a number of key advantages: high density, low latency, and low power dissipation [13].

For F2B stacking orientation (Figure 5.b); silicon substrate side of a first die is bonded with metal layer of the second die using high density TSVs. The stacking process depends on many parameters such as the specifications of the application and the cost, and has an impact on the test of the 3D stack.

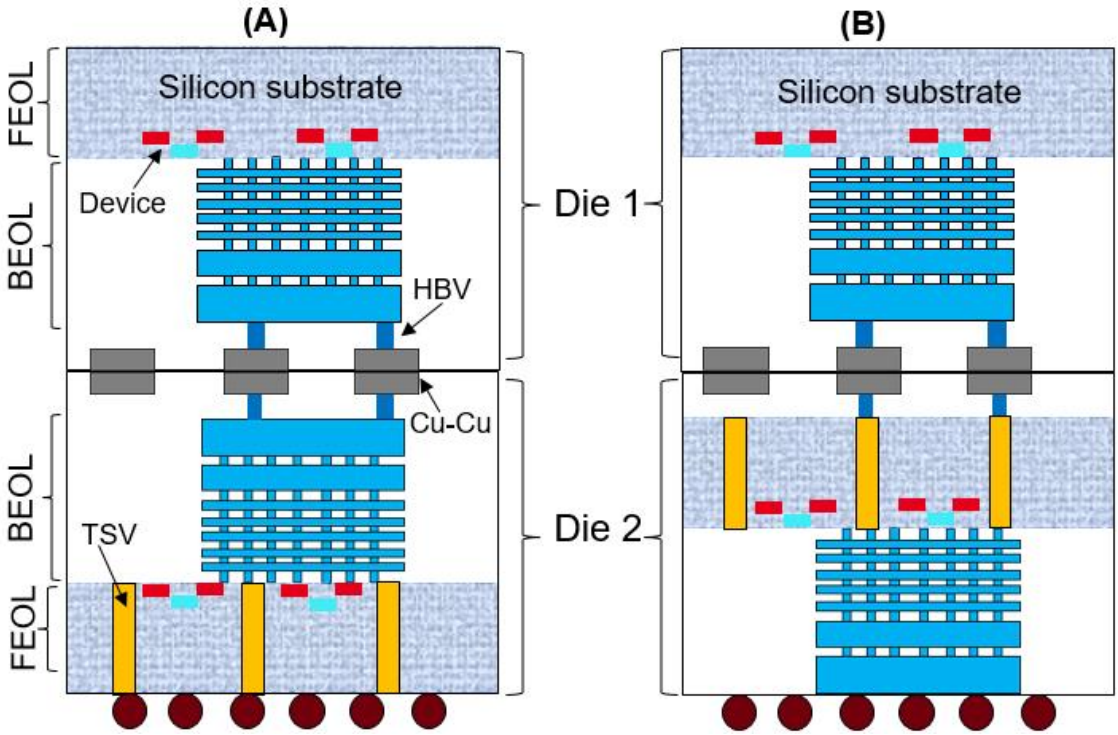


Figure 5: Cross-sectional view of high density 3D-IC structures: (a) F2F, (b) F2B

An example of process flow described in [14], [15] is shown in figure 6. Firstly, the metal lines are processed by single damascene step. Thereafter, the hybrid bonding level is deposited using a double damascene process; in this approach, two wafers/ dies modified to ensure very low final surface roughness and minimal Cu recess at the surface. After Chemical Mechanical Polishing (CMP) process for surface planarization and copper dishing minimization, the top and bottom wafer/die level are bonded. Finally, the wafer is thinned and the backside is opened to metal lines.

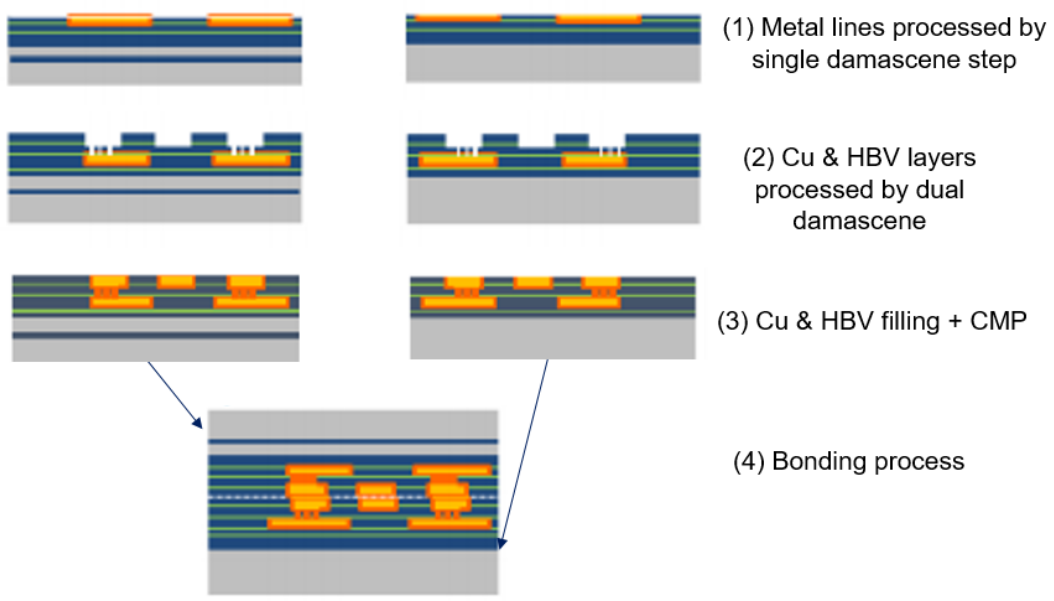


Figure 6: Example of hybrid bonding process flow (source [15])

3. High density TSVs

The idea of using through-silicon-via (TSV) technology has been around for many years. A through-silicon via (TSV) cross vertically the silicon layers in order to establish electrical links between the different stacked dies in the 3D-IC system. TSVs are often use as an alternative to wire-bond and flip chips. Many 2.5D and 3D packages are using the TSV technology compared Package-on-Package (PoP) technology. This is because the small pitch between TSVs that allows a high density of interconnections.

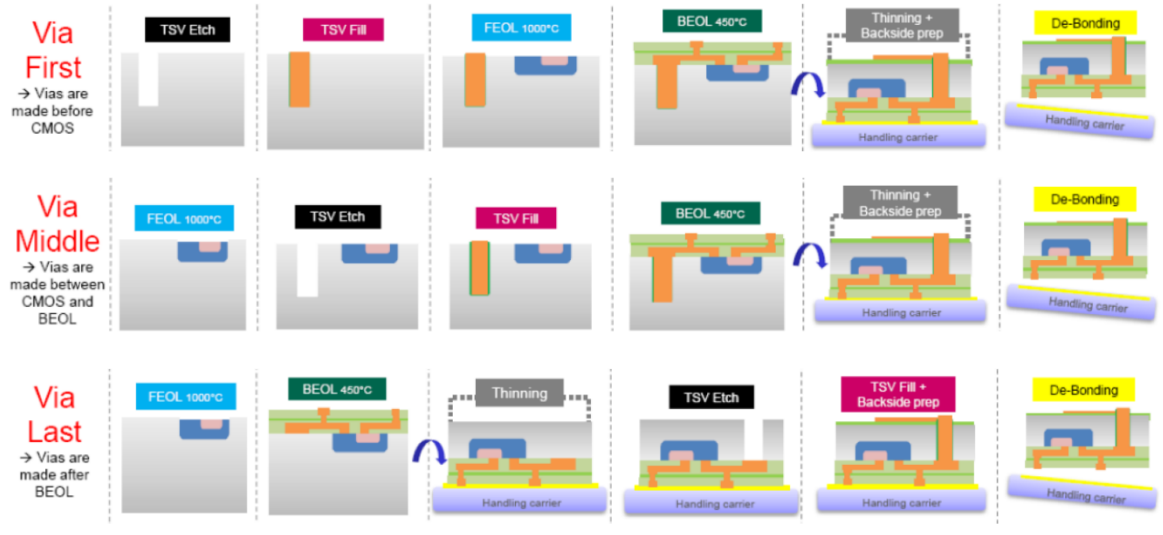


Figure 7: Via-first, via-middle and via-last illustration (source [16])

There are three main types of TSV approaches: TSV-first, TSV-middle, and TSV-last that correspond to three fabrication ways (Figure 7). The via-first TSV is fabricated directly on the silicon before any step of integration of active components, which means before the Front End of the Line (FEOL). The Via-middle TSV is fabricated after the

active components, which means after the FEOL process but before the Back End of the Line (BEOL) process. The via-last TSV is made after the FEOL and BEOL processes.

The semiconductor industry is actively pursuing 3D Integrated Circuits (3D-ICs) with TSV technology. The semiconductor industries already succeeded to reduce the pitch of hybrid bonding interconnects below 2µm. On the other hand, many methodology demonstrate the fabrication of reliable high-density TSVs that can be fabricated on the same Cu-Cu interconnects pitch [17], [18].

III. Applications

1. CMOS image sensor

CMOS image sensors (CISs) are widely used widely used in products such as digital still cameras or digital video [19]. Conventional CMOS image sensors contain the pixel section and the analog logic circuit on the same chip, which imposes many constraints due to large footprint. High density 3D integrations has many advantages for this kind of application; it helps maintain high performance and offers advanced functionality in a compact chip size. The principle of 3D CISs is to dedicate the top layer to pixels and bottom layer for logic processing (two layers image sensor) [20], [21] (see Figure 8.a). There are another implementation using three layers [22]; a memory layer is used to achieve high-speed readout (Figure 8.b).

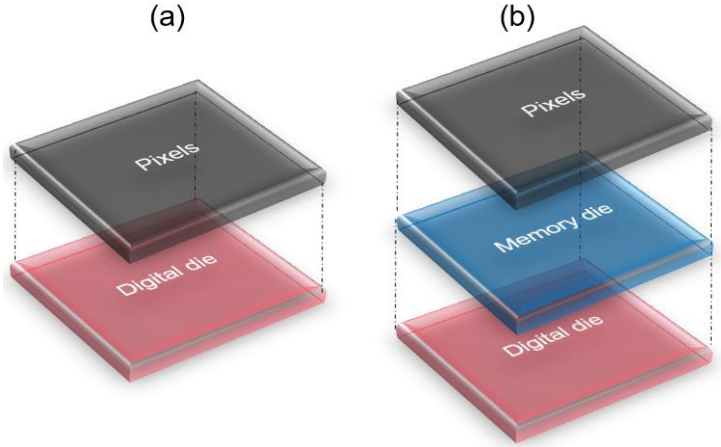


Figure 8: Structure of stacked CMOS image sensor: (a) two layers, (b) three layers

Sony was first to bring stacked image sensor chips to market; “Exmor RS” is the first stacked CMOS image sensor announced by Sony on 20 August 2012, widely used for phone cameras, which combine superior image quality and advanced functionality with a compact size with a pixel size of 1.12µm [23] (Figure 9). The via-last TSVs are used to connect top and bottom [24]. However, imperfect parallel processing limits the performance in such sensors because the TSV/micro-bump is larger than the pixel size (less than 10µm). High-density 3D-IC integration allows pixel-parallel signal processing

and provides excellent electrical connectivity and reliability with a higher 3D interconnect density (more than $10^6/cm^2$).

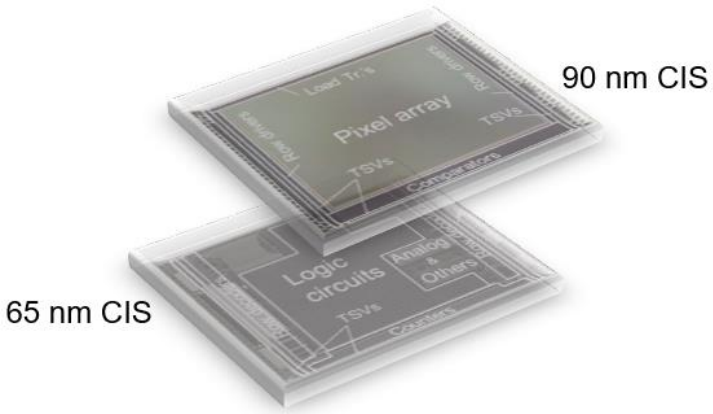


Figure 9: Micrograph of "Exmor RS" CMOS image sensor (source [23])

In 2016, Sony shifted its interconnect strategy for image sensors using Cu-Cu hybrid bonding with a pitch of 6.3 µm with dummies Cu-Cu pads covering most of the active pixel array and peripheral regions [25], [26]. In 2019, Sony was successfully developed a fine pitch 3 µm pitch Cu-Cu hybrid bonding process [27].

Among the producers of 3D image sensors there are also OmniVision with a first stacked chips, fabricated on the PureCel-S platform using TSV technology and a 1.12 µm pixel size. Later, OmniVision released 1.1 µm pixel generation PureCelPlus-S chips, fabricated by foundry partner TSMC [28], [29]. In 2018, Samsung Electronics introduced also the three-layer ISOCELL Fast 2L3 image sensor with a pixel size of 1.4µm.

In 2018, CEA-Leti and STMicroelectronics developed the hybrid bonding technology for image sensors with a pitch of 1.44µm [6]. It is expected that the future generations of 3D image sensors will allow pixel-parallel signal processing. So, the pitch of 3D interconnects must be equivalent to pixel size.

2. High performance computing

3D stacking integration allows integrating heterogeneous components such as Processor, FPGA, GPU, Memory, etc. and offers excellent platform to achieve superior bandwidth, low power consumption. It's the main driver of the high end computing applications such as data centers [30] .

3D integration offers a possibility to integrate multiple technologies (logic, memory, RF, sensors …) stacked together in a single package. Xilinx has developed Virtex-7 HT FPGA the world's first heterogeneous architecture for high-bandwidth and high-performance FPGAs (Figure 10). The architecture includes four separate 28nm FPGA dies were connected to each other through a 65nm passive silicon interposer using thousands of µ-bumps with a pitch of 45µm [31].

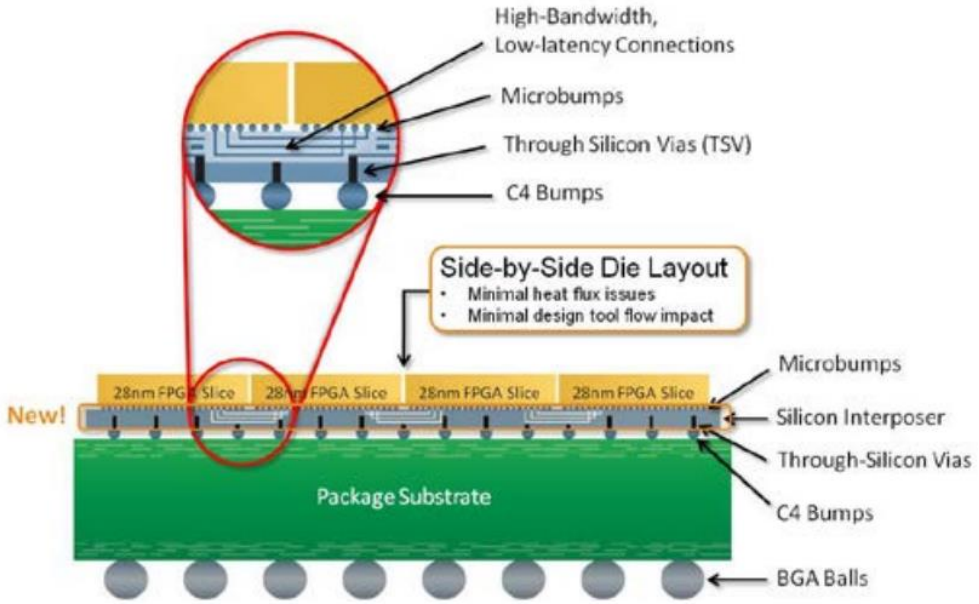


Figure 10: architecture of Virtex-7 HT (source [31])

The ability to stack high density DRAM, such as High Bandwidth Memory (HBM) and Hybrid Memory Cube (HMC), on top of the logic die is extremely precious for several applications because of the reduction of the interconnect length witch increases the performance in terms of RC delay, power consumption and form factor. A stacking example of high-density DRAM dies on the top of each other, with one logic die at the bottom for control have been introduced in [32], [33]. Another example of high-density DRAM towers connected to the CPU or GPU through an interposer using TSVs and µ-bumps is shown in [34] (see Figure 11).

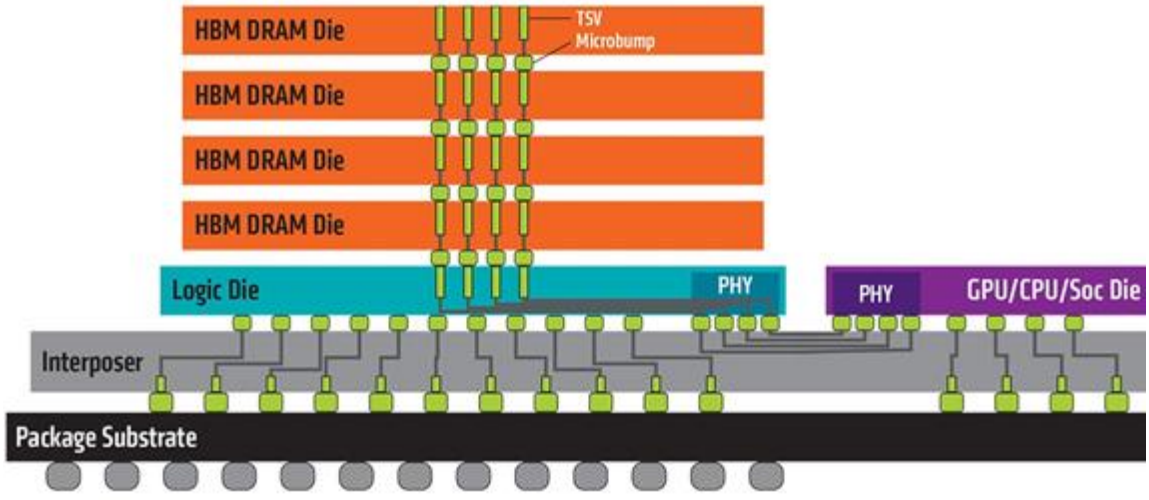


Figure 11: AMD Fury: HBM and CPU/GPU implementation using a passive interposer (source [34])

The main objective and challenge, in High Performance Computing (HPC) context, is to define modular and scalable computing with relatively low cost. Chiplet partitioning allows to reduce the overall system cost by designing smaller chips in an advanced

technology (FinFET 14nm or 10nm), which will be sorted using Know-Good-Die (KGD) method and finally assembled onto a large scale interposer structure. As recent examples, [35] is a chiplet based architecture, from AMD, with chiplet stacking onto large scale organic substrate with up to 4 chiplets, while [36] is a chiplet based approach from TSMC using Chip-on-Wafer-on-Substrate (CoWos) 2.5D passive interposer technology, and finally [37] is chiplet based approach from INTEL using Embedded Interconnect Bridges (EMIB) technology. All these technologies are using µ-bumps with different pitches, ranging from 40µm to 100µm pitches. HPC is not yet using hybrid-bonding technology, and for such application, the requirements are aggressive interconnect pitch and Die-to-Wafer (D2W) assembly scheme.

Another example of chiplet partitioning of a multi-core system was proposed by CEA-Leti and called Intact [38], [39] and [40]. Figure 12 shows the system architecture based on six identical 22mm² 28nm FD-SOI chiplets 3D-stacked onto 200 mm2 65 nm CMOS active interposer. The overall architecture integrates 96 cores with an innovative L1/L2/L3 coherent cache; 16 cores per chiplet (32-bit Microprocessor without Interlocked Pipelined Stage (MIPS) cores). The interposer integrates chip-to-chip communications using a robust asynchronous 3D Network-On-Chip (NoC), design-for-test, clocking and power management.

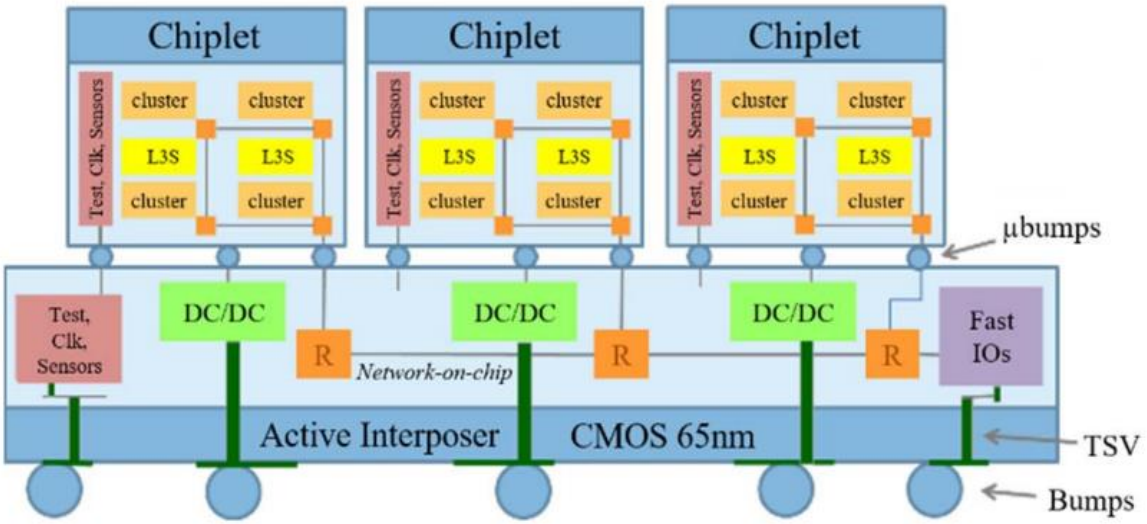


Figure 12: Intact system architecture overview (source [38])

IV. Test and characterization challenges of HD 3D-ICs

1. High-density 3D-IC interconnect defect

Cu-Cu hybrid bonding interconnects are prone to many structural defects due to fabrication process. Figure 13 shows misalignment and micro-voids defects in a Cu-Cu 3D-IC. A high precision wafer bonding tool it is important for 3D-IC fabrication, because it is necessary to have an important factor of accuracy to have a functional and performant

circuit. However, despite the rapid development of these new stacking technologies providing more and more interconnection density and even if stacking tools accuracy has been improved, providing accuracy down to ~200nm for Wafer-to-Wafer bonding and down to ~1µm for Die to-Wafer bonding [41].

Translation, rotation and the magnification effect (run-out) are the causes of local misalignment; the global translation and rotation value depend on bonding equipment accuracy and are steadily minimized by continued developments of commercial bond alignment tools. But the run-out effect, which is related to the wafer expansion due to the thermal stress, is still one of the most challenging issues in 3D-IC bonding process [42]. µ-voids defects are in the form of cavity caused by practices at the contact surface level due to insufficient cleaning before bonding, they depend on particle size. A non-optimized CMP process may generate also µ-void defects in the range of few nanometers due to copper dishing.

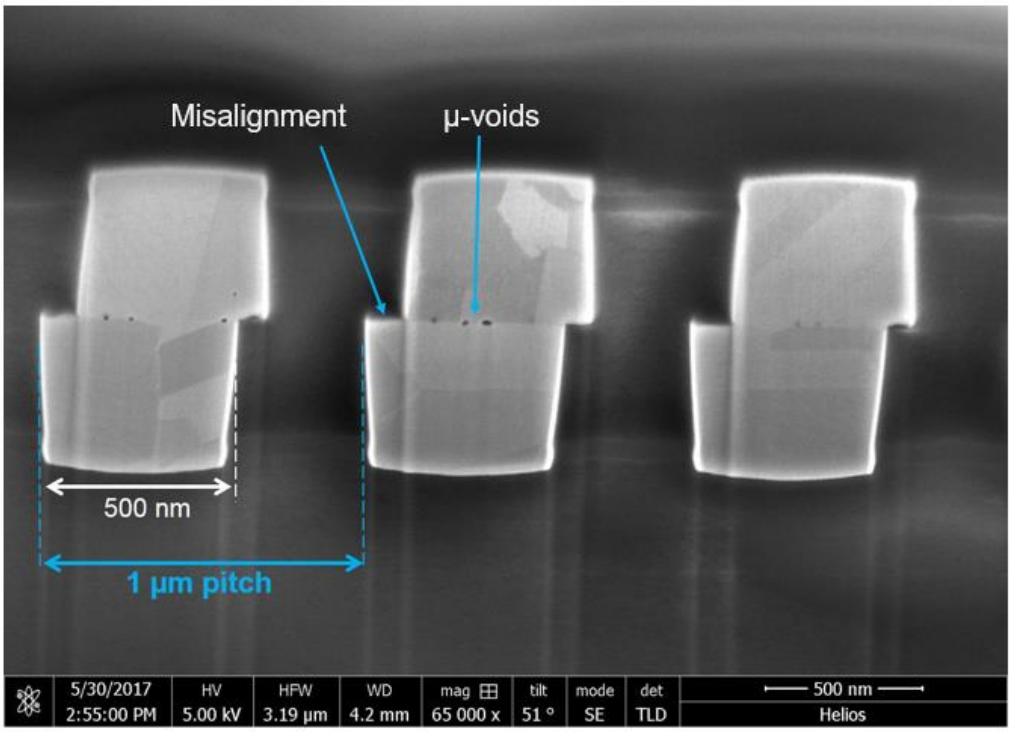


Figure 13: µ-voids and misalignment defect in Cu-Cu interconnects

The presence of this defects increases the interconnect resistance/ capacitance which will impact the performance and reduce the life time of 3D-ICs. Misalignment defect affects electrical characteristics (reduce the effective contact surface) and can cause leakage current overheads, resulting in an undesirable conductive path between two adjacent Cu-Cu interconnects which decrease the life time of the 3D-IC [43]. Therefore it is necessary to detect µ-void defects, measure the alignment after bonding and electrically characterize the vertical interconnections in order to estimate the potential impact on the global performances.

2. Test challenges at system level

The test in system level is based on Design for Testing or design for testability (DFT), which consists adding testability features to a hardware product design. The added features make it easier to develop and apply manufacturing tests to the designed hardware. The purpose of manufacturing tests is to validate that the product hardware contains no manufacturing defects that could adversely affect the product's correct functioning. Tests are applied at several steps in the hardware manufacturing flow and, for certain products, may also be used for hardware maintenance in the customer's environment.

The tests are generally driven by test programs using Automatic Test Equipment (ATE), the response of vectors (patterns) from a good circuit is compared with the response of vectors (using the same patterns) from a DUT (device under test). If the response is the same, the circuit is good. Otherwise, the circuit is not used.

Traditionally, in 2D context, there are two moments of test of the individual dies: the first one is the test at wafer level that is performed after wafer fabrication and before assembly and packaging. The second test is the final test which is done after assembly and packaging. In 3D context, the test may have to be performed at pre-bond phase in order to provide Known Good Die (KGD) before stacking, mid-bond phase to test a partially assembled 3D stacks to Known Good Stack (KGS), post-bond phase to tests the complete 3D stacks yet still not packaged and finally test the packaged product [44].

a) Challenges of pre-bond test

The pre-bond test is done using Electrical Wafer Sort (EWS), also known as probing, is used to check the electrical functionality of the die at the wafer level. As mentioned previously, this test is performed at the end of the front-end part of the process, before assembly. The Probe Card [45], [46] and [47] holds the contact elements that establish the connection with pads and perform the electrical measurements. There are two major challenges in pre-bond test of high-density 3D-ICs:

- Despite the development of probe cards, the probing pitch is much higher than the pitch of Cu-Cu interconnects. So it’s necessary to include non-contact testing methods such as Built-In-Self-Test (BIST) or adding oversized probe pads for probe needle touchdown.
- The probing process can damage the probing pads, causes particles at surface level and impact the bonding process (Figure 14); the damage in the bonding surface is equal to a thousand times that of the particle size. For this reason, the pre-bond test in D2W stacking option is unachievable.

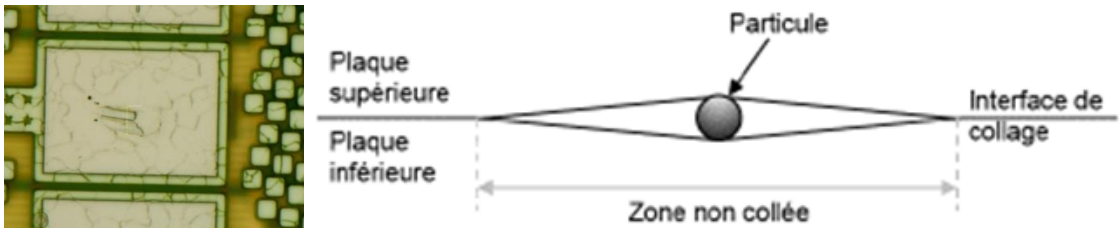


Figure 14: Impact of probing process

b) Challenge to test high-density 3D-IC interconnects

A DFT test access infrastructure is indispensable to achieve a high-quality test; some DFT structures are used such as internal scan chains, built-in self-test (BIST, Memory BIST) and Boundary Scan Cells (BSCs) around the embedded cores to provide isolation for internal testing (INTEST) and also external testing (EXTEST) of the 3D-IC interconnects between dies without requiring access to the entire die [48].

The BSCs on the first die provide observability, and the BSCs on the second die provide controllability (Figure 15). For timing reasons, the BSC cell must be close to the 3D interconnect to reduce the functional path length and the test time. For a high-density 3D circuit, the limited space for BSCs must be taken into account (the available surface per interconnect =Pitch²). Moreover, in F2B stacking orientation, the TSV and the keep-out-zone (KOZ) reduces the available surface.

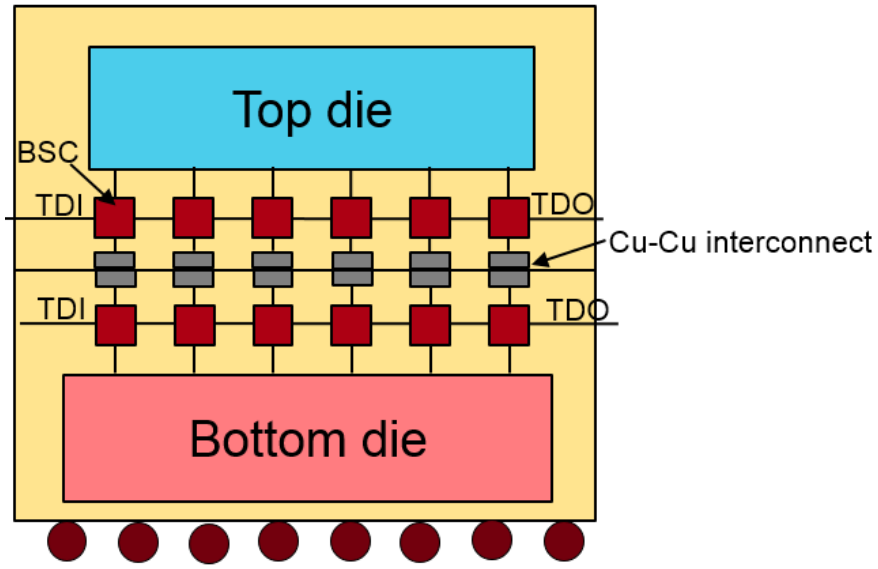


Figure 15: Test of 3D-IC interconnects at system level

V. PhD objectives and contributions

In this PhD thesis, we distinguish three main research axes:

- After studying the impact of Cu-Cu interconnect defect on electrical parameters, we need detect the presence of misalignment defect: our aims is to implement innovative and low cost test structures into the bonding interface

using Cu-Cu interconnects, used either in a passive way for technological process validation and characterization and obtain an additional information in case of misalignment such as direction, accurate value and obtain an additional information in case of misalignment such as direction and an accurate value. The proposed test structure will be explained, implemented for high-density 3D-IC interconnects in process development context and validated using overlay measurements obtained using IR metrology. Moreover, we need characterize Cu-Cu interconnects and estimate indirectly the contact resistance values.

- In the application circuit context, 3D DFT architecture ensures the test of all the components of the 3D system including the different stacked dies and the 3D interconnections at all the 3D bonding levels: pre, mid and post-bond levels. Test infrastructure of high-density 3D-ICs presents new test challenges because of the high interconnects density and the area cost for test features. Our objective is to analyze the testability of HD 3D-IC; we define the most optimized Design-For-Test infrastructure depending on used standard and the minimum acceptable pitch value for a given technology node to ensure the testability of circuits. Afterwards, we need propose an optimized DFT architecture allowing pre-bond and post-bond for high-bandwidth and high-density 3D-IC application (SRAM-on-Logic) in line with the ongoing IEEE P1838 standard.

- Finally, we try to implement the proposed misalignment test structure used either in a passive way for technological process validation and characterization in the 3D DFT architecture to detect misalignment and µ-void defects and assess performance of high-density 3D-ICs using BISTs. If the functional interconnection test is impossible because of the aggressive pitch of 3D interconnects, the proposal must be used to perform functional and structural test of high-density 3D functional interfaces

This thesis is organized as follows:

Chapter 2 focuses mainly on the measurement of misalignment defect. Initially, we present the proposed solution to measure bonding misalignments. Afterwards, test results are detailed to validate the proposed test structure. Finally, we present the impact of misalignment defect on R & C parameters.

Chapter 3 focuses on the test of high-density 3D-IC interconnects at system level. Firstly, we analyses the testability of HD 3D-IC interconnect. Then, we present the

optimized DFT architecture for high density SRAM/Logic 3D-IC. Finally, simulation results are detailed.

Chapter 4 explains in details the need to add the proposed test structure, discussed in chapter 2, to the application circuit. Initially, the test flow is explained in details, followed by the description of the proposed BISTs to test misalignment and µ-void defects. Finally, the validation of the model is explained by supporting simulation results.

Chapter 5 concludes the thesis with final outcome and future perspectives.

Chapter II. Characterization of high-density 3D-IC interconnects

Cu-Cu hybrid bonding is currently the ultimate fine pitch 3D interconnect solution with target pitch of 1µm, but that generates new challenges for characterization; Cu-Cu interconnects are prone to many structural defects due to fabrication process such as misalignment and µ-voids that affect the electrical characteristics. For technology development, before the production of the wafers with all FEOL and BEOL layers, several short loops, with only the top metal layer, must be carried out to enable incremental test and characterization. Several test vehicles are necessary to validate the technological process and perform electrical characterization of Cu-Cu interconnects: electrical characteristics, yield, reliability and electro-migration. In this chapter, we focus on characterization of Cu-Cu interconnects and we propose an innovative test vehicle to measure several information after bonding: perfect alignment, misalignment (direction, value) and contact resistance.

I. Impact of defects on electrical characteristics

1. Overview

Misalignment and µ-void defect affects electrical characteristics and can cause leakage current between Cu-Cu pads. Figure 16 illustrates the equivalent electrical model of Cu-Cu interconnect [49] to be used in simulation. The pad resistance (R_pad) depends on the effective contact surface and the resistance of Hybrid Bonding Vias (R_HBV) depends on the number of vias connecting the top metal layer to the Cu-pads, the gap between top and bottom Cu pad forms a coupling capacitance Cc and Cp is the parasitic capacitance due to the proximity between two adjacent Cu pads.

Figure 17 shows the impact of physical defects on our electrical model; in the defect-free case (Figure 17.a) the resistance of the Cu-Cu pad (R_pad) is typically quite small and equal to the theoretical resistance with 100% of contact surface. µ-voids at the bonding interface increase the resistance (Figure 17.b). Also, depending on the void area and the height (h), there may be a significant coupling capacitance (Cc).). In the case of a misalignment defect (Figure 17.c), a parasitic capacitance (Cp) is inserted depending

on the distance between two adjacent Cu-pads and the resistivity effect due to the contact area decrease. Figure 17.d illustrates the overlay of misalignment and µ-voids defects. Based on the proposed electrical model of Cu-Cu interconnects, we studied the impact of misalignment defect and µ-voids on the capacitance and resistance values.

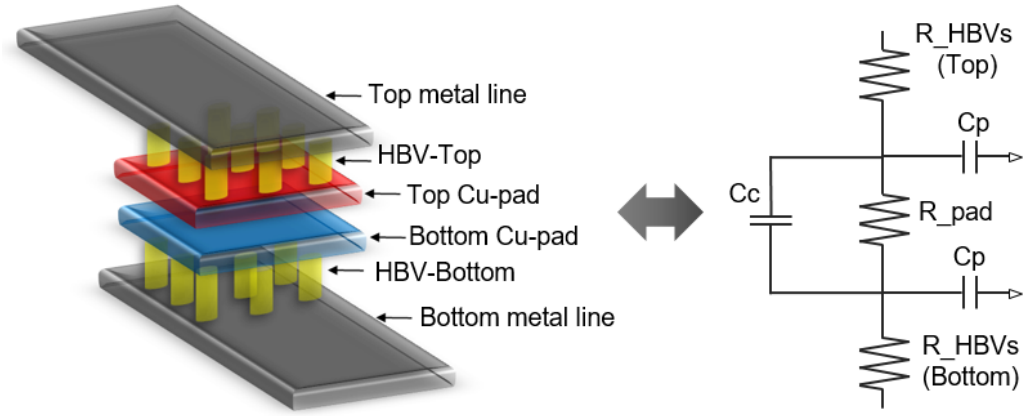


Figure 16: Equivalent electrical model of Cu-Cu interconnects

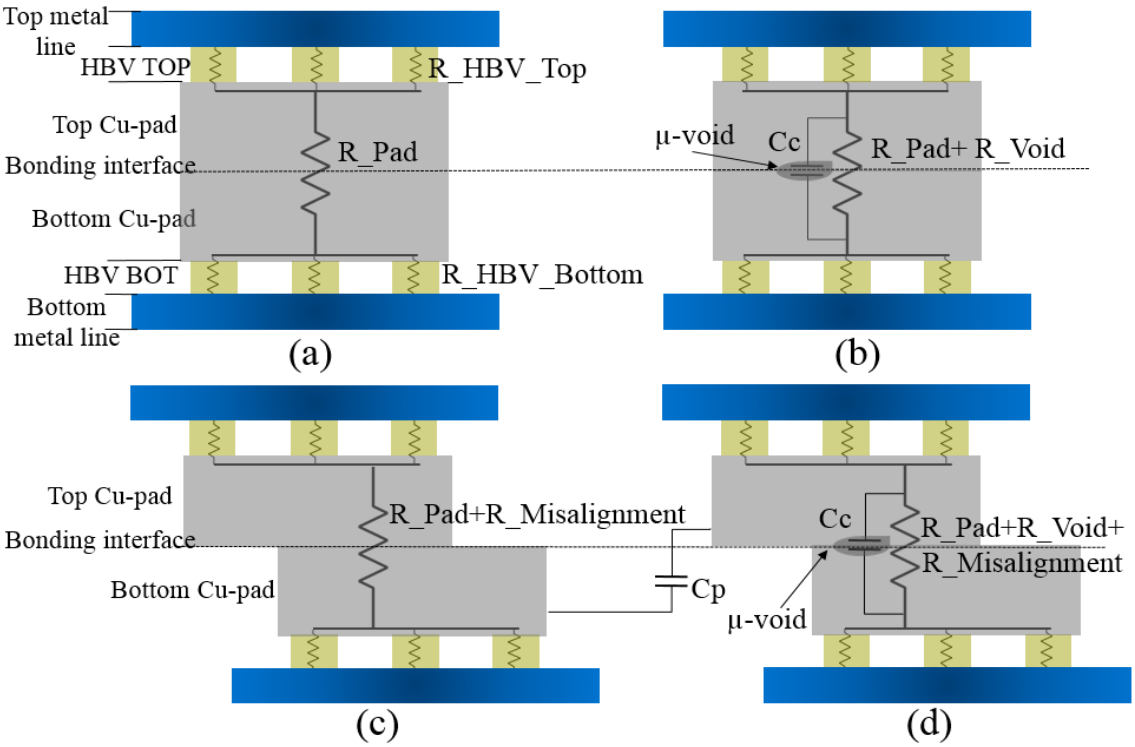


Figure 17: Impact of Cu-Cu interconnect defect on electrical characteristics

The first part of my work has been to study the impact of misalignment defect and µ-voids on the capacitance and resistance values using the proposed electrical model of Cu-Cu interconnects. The theoretical resistance and capacitance values are obtained using respectively equation 1 and 2; the Cu-Cu interconnect resistance is the sum of the resistance of HBVs top and bottom, that depend on HBV length "l", HBV diameter "D" and the copper resistivity "ρ Cu", and the resistance of Cu pads, that depend on the

copper resistivity, the effective contact surface between top and bottom pad and the pad thickness "h".

For capacitance calculation, the parallel-plate capacitor principle is used (Figure 18). The simplest model capacitor consists of two thin parallel conductive plates each with an area of "A" separated by a uniform gap of thickness "d" filled with a dielectric with permittivity Ɛ. It is assumed the gap d is much smaller than the dimensions of the plates. For the calculation of coupling capacitance "Cc", the area "A" and the gap thickness "d" are equal respectively to the µ-void-surface and µ-void-height. But, for parasitic capacitance calculation, the area "A" and the gap thickness "d" are equal respectively to Pad Size "PS" * pad thickness "h" and the distance between two adjacent pads.

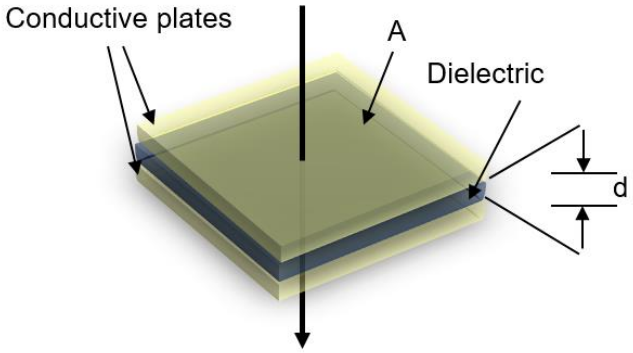


Figure 18: Parallel-plate capacitor model

$$Misalignment\ (M) = \sqrt{X^2 + Y^2} \qquad (1)$$

$$R = \frac{2\times\rho cu\times h}{contact\ surface} + R(HBV's_{Top}; HBV's_{Bottom}) \qquad (2)$$

With: - "ρcu" is the copper resistivity = 1.69×10^{-8} Ω.m.
- R (HBV's Top/Bottom) is the Hybrid Bonding via resistance.
- "h" is the pad thickness.

$$C = Ɛ * \frac{A}{d} \qquad (3)$$

With: - "Ɛ" is the permittivity = Ɛ0 Ɛr= 3.45×10^{-11} F.m^{-1}.*
- "A" is the area and "d" is the gap thickness

Using the equations shown previously, we performed simulations to quantify the electrical impact of misalignment and µ-void defects.

2. Impact of misalignment defect on electrical characteristics

Figure 19 shows the variation of pad resistance (R_pad) and parasitic capacitance (Cp) as a function of the misalignment value obtained using (1) (X=Y). The highest values of R_pad and Cp are obtained at the limit of misalignment for a given pitch; i.e. for a pitch of 1.4 µm (Pad-size=Pitch/2), the limit of misalignment ≈ $(0.7^2 + 0.7^2)1/2 \approx 0.99$ µm. The optimal pad resistance values (corresponding to the perfect alignment M ≈ 0) vary from one pitch to another: they depend on the pad size and the number of HBVs (equal respectively to 25, 9 and 1 for pitch of 7.6, 3.45 and 1.4 µm).

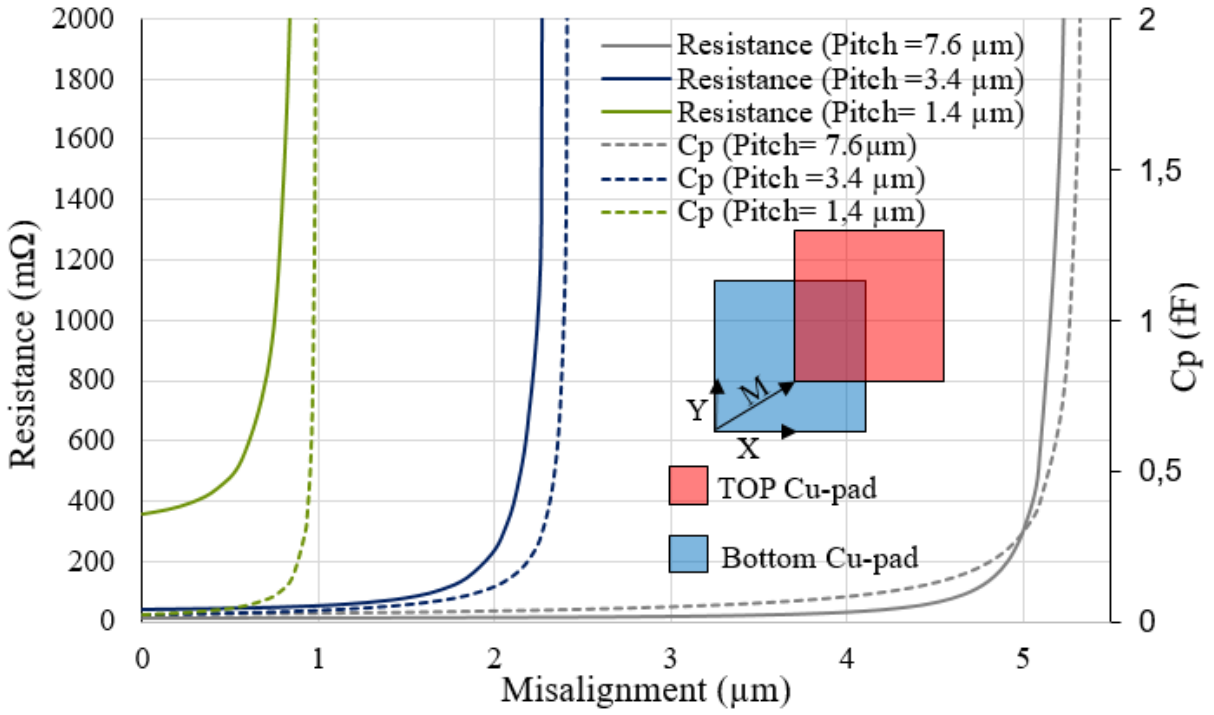


Figure 19: Variation of the resistance and parasitic capacitance of a Cu-Cu pad (pitch: 7.6, 3.45 and 1.4µm) as a function of misalignment.

3. Impact of µ-void defects on electrical characteristics

Figure 20 shows the impact of µ-void on R and C parameters; the resistance depends only on the µ-void surface but the coupling capacitance Cc depends on µ-void surface and the height h, for these reason the impact of the surface and the height on Cc are studied separately (Pink and black dashed lines). When the µ-void surface becomes comparable to the pad surface, the resistance and coupling capacitance reaches the maximum. In the other side, we observe that the increasing in Cc values becomes more important with a lower "h" values.

According to the study of high-density 3D-IC interconnects defects impact on electrical characteristics, we can affirm that misalignment and µ-void impact becomes more important with a lower pitch (1.4µm). We show also that electrical impact is mostly

resistive and it's similar for misalignment and µ-void defects since it depends on the effective contact surface, which makes it difficult to separate defects.

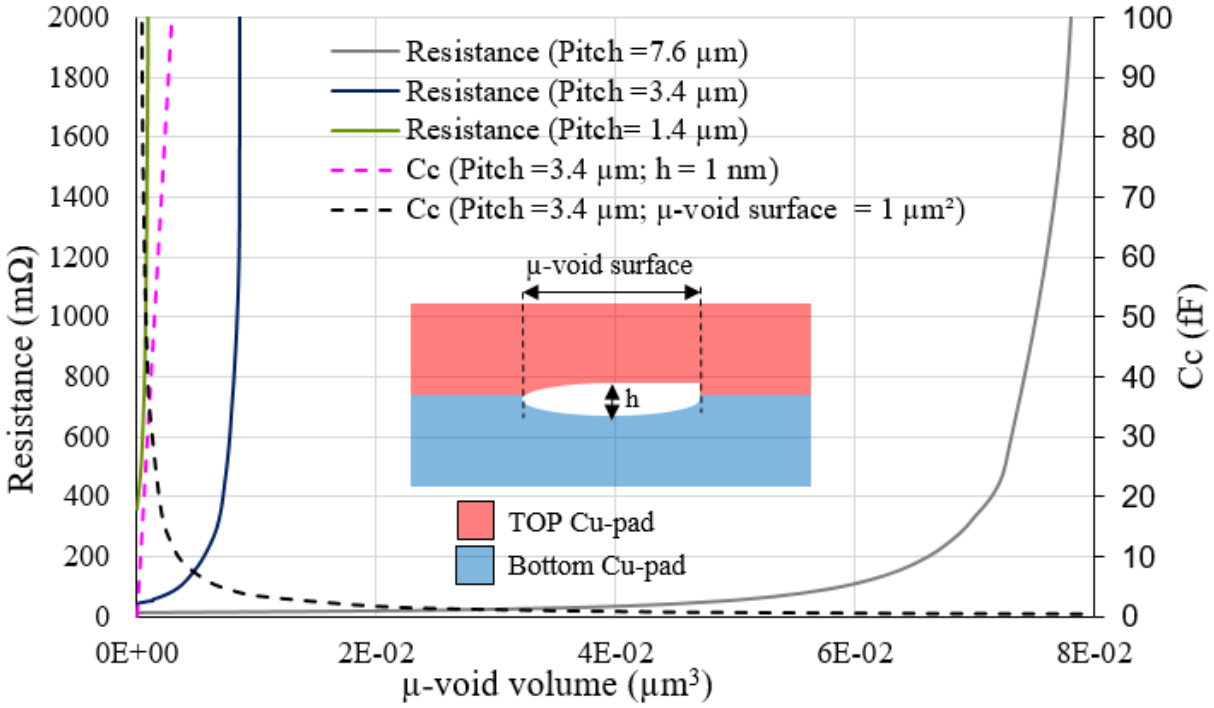


Figure 20: Variation of the resistance and coupling capacitance of a Cu-Cu pad (pitch: 7.6, 3.4 and 1.4µm) as a function of µ-void volume.

In the other hand, actually the parasitic capacitance "Cp" has a small value except in the case of high misalignment values (i.e. Misalignment in X or Y direction ≈ pad size). But the coupling capacitance "Cc" can have great values mostly when one or more µ-voids appears in the contact surface interface.

II. Characterization methods: state of the art

1. Morphological methods

There are lots of methods for failure analysis of damages on wafer, including but not limited to: optical microscopy, Scanning Electron Microscope (SEM), Transmission Electron Microscopy (TEM), X-ray and Scanning Acoustic Microscopy (SAM).

The Infra-Red (IR) metrology tool (IR light system and alignment marks) [50] controls and evaluate bonding quality before and after bonding process (Figure 21). This module allows to control the fine movement of the wafers before bonding process [51]. Although both translational and rotational errors could be controlled and minimized during the alignment step, the run-out error remains a key contributor to the entire overlay error. Therefore, to handle a wafer without damaging it and to achieve higher alignment accuracy, the wafer should be affixed to flat using an electrostatic chuck [52]. After

bonding process, the misalignment measurements for all wafer reticles, using IR metrology tool, require a long testing time. Moreover, the measurements must be disturbed because of the absorption of the IR ray by all the dielectric layers.

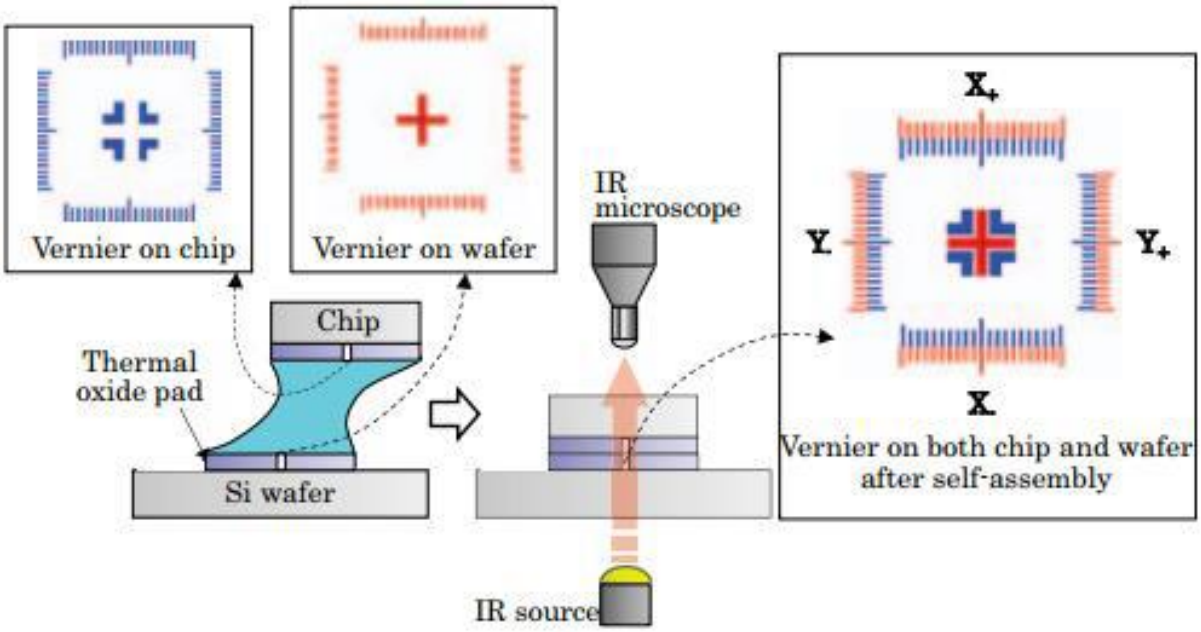


Figure 21: IR metrology tool principle (source [50])

In 3D-IC context, Scanning Electron Microscopy (SEM) and transmission electron microscopy (TEM) are the most used techniques, allows to visualize defects at the bonding interface [53]. The method used in SEM is based on scattered electrons while TEM is based on transmitted electrons. The scattered electrons in SEM produced the image of the 3D interconnects after the microscope collects and counts the scattered electrons. In TEM electrons are directly pointed toward the 3D interconnects. SEM provides a three-dimensional image but TEM delivers a two-dimensional picture. In terms of resolution, TEM has an advantage compared to SEM. The resolution of TEM is less than 0.2 angstroms while SEM has a few of nanometers. Contrariwise this techniques need a very expensive equipment's and must be housed in an area free of any possible electric, magnetic or vibration interference [54]. Moreover, this techniques are destructive, figure 22 shows an example of SEM image of Cu-Cu interconnect.

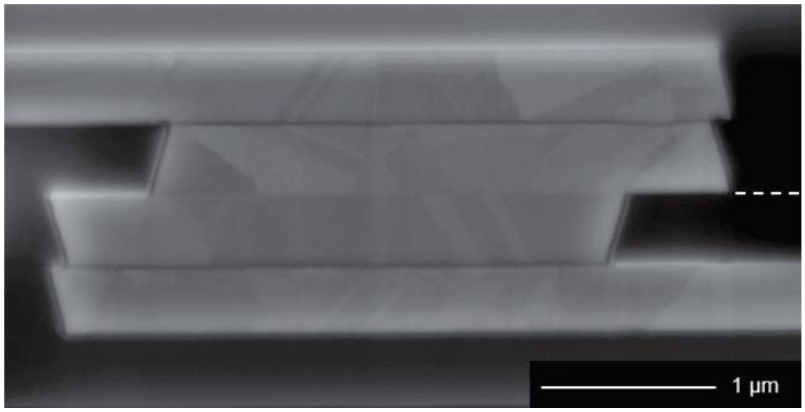


Figure 22: Example of SEM image of Cu-Cu interconnect (source [55])

2. Electrical measurements

Another alternative to detect misalignment is based on electrical measurements (resistance and capacitance) with two classical test structures (Kelvin and Daisy chain) [56]. In these works, Rth is obtained using equation (2) with contact surface equal to the pad area (PS^2). The principle of the Kelvin measurement method is shown in figure 23.a. Four-point V+, V-, I+, I- method is used for an accurate measurement of a single interconnect in regard to a typical 2- point resistance measurement. If we have a perfect alignment then R=Rth. And if we have a misalignment defect, the resistance value increases when top-bottom contact surface decreases. The same principle is used for daisy chains (Figure 23.b), but in this case the measured resistance value also includes horizontal interconnects resistance through the daisy chain. Electrical measurements allow to characterize high-density 3D-IC but do not allow to obtain an accurate information about defects characteristics (direction, contact surface …) because of the similar effect of the misalignment and µ-void defects on the electrical characteristics.

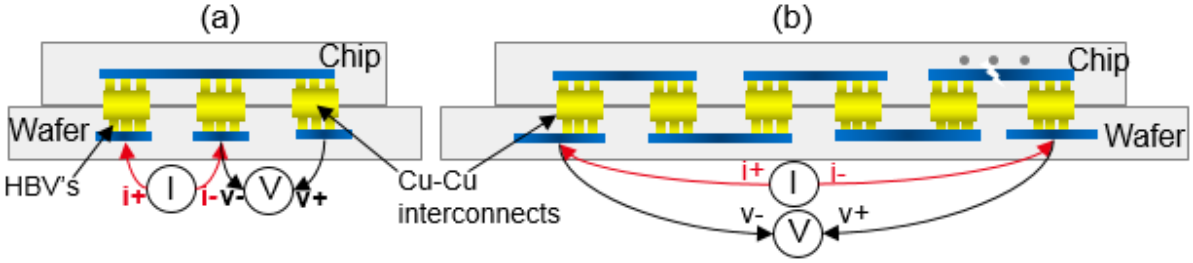


Figure 23: Electrical measurement test vehicle:
(a) Kelvin, (b) Daisy chain

Cu-Cu hybrid bonding offers very high-density interconnects (pitch around 2µm or less) in 3D stacking integrated circuits, but the smaller the Cu pad size, the more the bonding defects, such as misalignment and µ-voids, have an important impact on resistance and capacitance parameters. The currently used methods are all focusing on

process characterization and are not able to provide active performance characteristics of a real 3D Integrated Circuit because of the test time and cost.

Our aims is to implement innovative and low cost test structures into the bonding interface using Cu-Cu interconnects, used either in a passive way for technological process validation and characterization and implemented in high-density 3D-ICs to assess performance; we need distinguish defects (misalignment and/or µ-voids); obtain an additional information in case of misalignment such as direction, accurate value and detect also µ-void defect. In a second time, we try to characterize Cu-Cu interconnects and estimate indirectly the contact resistance values.

In the next part, a new methodology to determine both misalignment characteristics and performances as described thereafter. Firstly, the proposed test structure will be explained, implemented for high-density 3D-IC interconnects in process development context and validated using overlay measurements obtained using IR metrology. Subsequently, the proposed test structure will be implemented in an application circuit for a structural test of the 3D functional interfaces and will be used in conjunction with other test structure to detect µ-void defects.

III. Proposed structure to test bonding alignment and characterize HD 3D-IC interconnects

1. Overview

The vector formula of translation, rotation and run-out, that are the causes of local misalignment, are explained respectively in (4), (5) and (6). Translation (T_x and (T_y) and rotation (θ) relate to the misalignment of the wafer. The run-out effect (ρ) relates to the wafer size change or wafer expansion due to processing. Wafer processing will include a variety of stressed thin film depositions, hot anneals, and other processes which can change the wafer size. The run-out effect is expressed in ppm (parts per million, i.e., 10−6) range. So, to exhibit misalignment defect on a wafer map, we developed a specific tool using MATLAB in W2W context “virtual wafer vector map tool” to enable us to easily visualize the superposition of translation, rotation and end-of-course effects as a wafer map vectors.

$$\begin{pmatrix} x' \\ y' \end{pmatrix} = \begin{pmatrix} x \\ y \end{pmatrix} + \begin{pmatrix} T\_x \\ T\_y \end{pmatrix} \qquad (4)$$

$$\begin{pmatrix} x' \\ y' \end{pmatrix} = \begin{pmatrix} cos\,(\theta) & -sin\,(\theta) \\ sin\,(\theta) & cos\,(\theta) \end{pmatrix} * \begin{pmatrix} x \\ y \end{pmatrix} \quad (5)$$

$$\begin{pmatrix} x' \\ y' \end{pmatrix} = \begin{pmatrix} 1+\rho & 0 \\ 0 & 1+\rho \end{pmatrix} * \begin{pmatrix} x \\ y \end{pmatrix} \quad (6)$$

$$\begin{pmatrix} x' \\ y' \end{pmatrix} = \left[\begin{pmatrix} cos\,(\theta) & -sin\,(\theta) \\ sin\,(\theta) & cos\,(\theta) \end{pmatrix} * \begin{pmatrix} 1+\rho & 0 \\ 0 & 1+\rho \end{pmatrix} * \begin{pmatrix} x \\ y \end{pmatrix} \right] + \begin{pmatrix} T\_x \\ T\_y \end{pmatrix} \quad (7)$$

$$\Downarrow$$

$$x' = [x * \cos\,(\theta) * (1+\rho)] - [y * \sin\,(\theta) * (1+\rho)] + T\_x$$

$$y' = [x * \sin\,(\theta) * (1+\rho)] + [y * \cos\,(\theta) * (1+\rho)] + T\_x$$

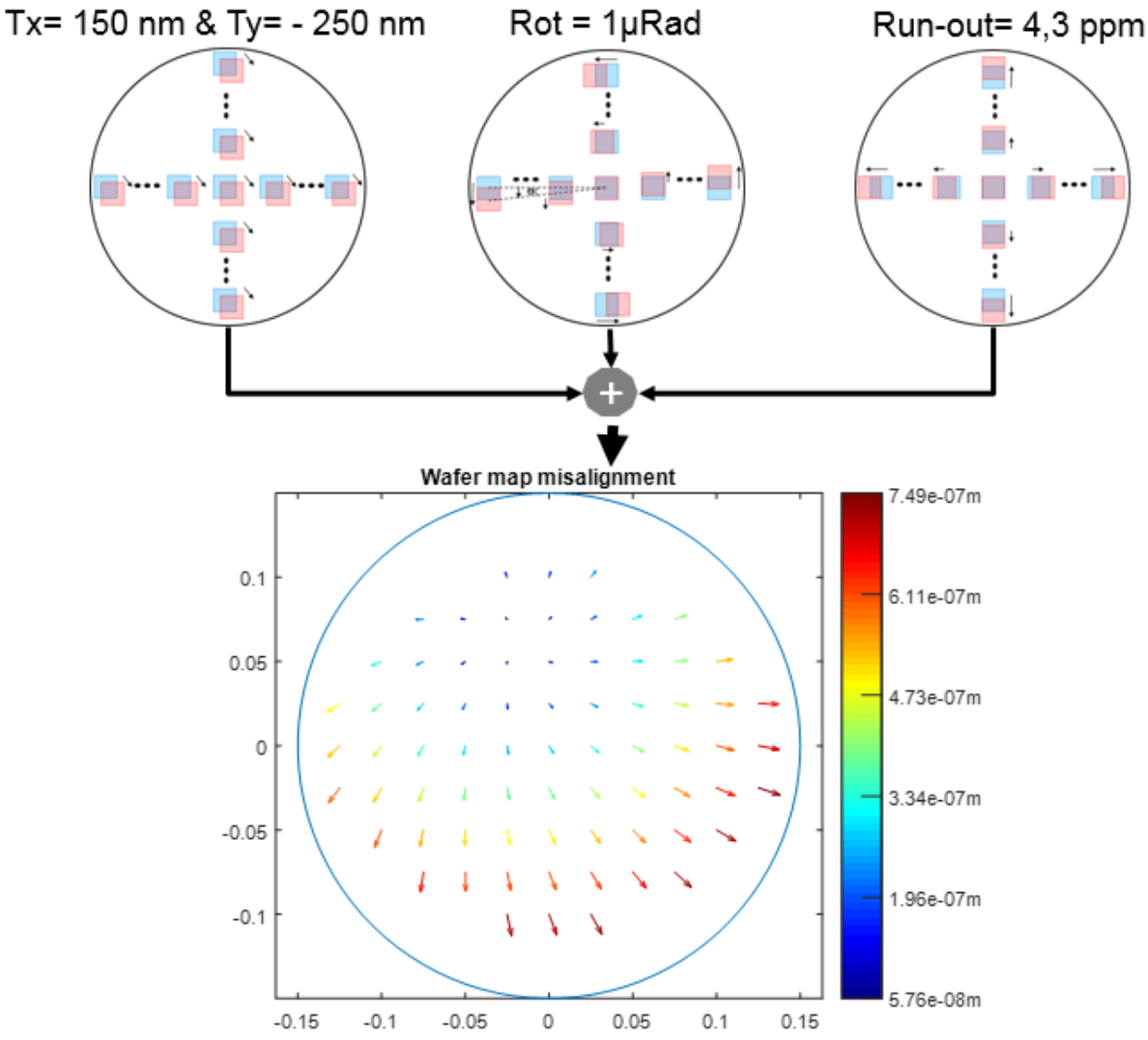


Figure 24: Wafer map: example of misalignment simulation

Figure 24 shows an example of simulation, the misalignment vectors shown in the wafer map are the results of the superposition of translation effect (T_X=150nm and

T_Y=-250nm), rotation of 1µRad and a run-out of 4.3ppm (part per million). For each vector, (x, y) are the origin coordinates of the vector (position in wafer) and (x', y') are the head coordinates of the vector calculated using (7). The color bar present misalignment value calculated using (1). We show that the maximum local misalignment value is equal to 750nm. In complement of misalignment prediction, the developed tool will also be used later to analyze the fabricated wafers.

In the other hand, we can affirm that the misalignment is not uniform at wafer level. So, a misalignment measurement module is needed in each reticle of the wafer to quantify misalignment defect, characterize high-density interconnects in the process development phase and classify the application circuits in order of performance in production phase.

2. Principle of the proposed test structure

According to the misalignment analysis shown previously, a low cost test structure is needed to measure accurately the misalignment defect and determine the misalignment direction in W2W and D2W stacking options. On the other side, as long as the structure will be implemented using Cu-Cu interconnects, there are many constraints that we can face: the respect of the bonding-interface planarity and the number of needed metal levels. Moreover, the test structure must be implemented for process development (using only metal layers) and for application circuit (using digital circuit), therefore for stimulus, the same signal must be used but it will be translated as analog signal (voltage) in the case of characterization (process development) and as a digital signal ('0', '1') in the application circuit.

In order to measure the misalignment, we describe a specific structure based on alignment reference patterns composed by a top Cu-pad (Red) and four Bottom Cu-pads (blue) (Figure 25). To test the bonding misalignment and its direction, we inject a signal at the input (in_TOP) and we observe the binary digital outputs: X+, Y+, X-, and Y-. In case of misalignment, the top Cu-pad is in contact with one or more bottom Cu-pads. On the other hand if there is no contact between top and bottoms pads, we can conclude that the alignment is perfect.

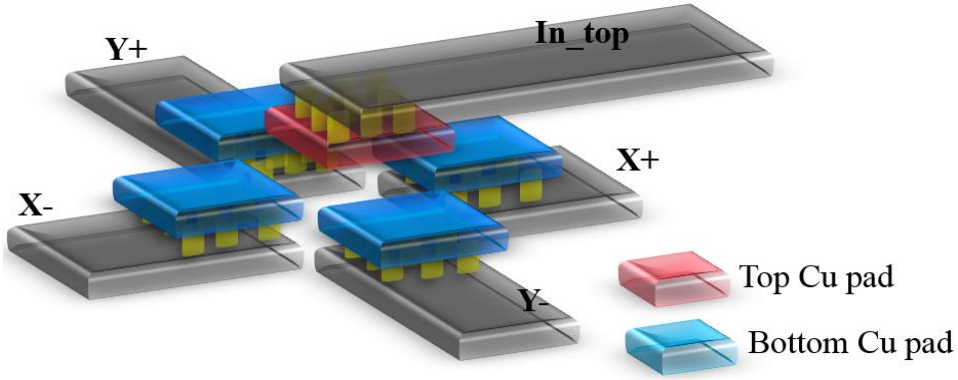


Figure 25: The reference pattern of misalignment test structure

The duplication of the reference pattern, using different spacing values (Offset_N) between bottom Cu-pads, offers the possibility to estimate the misalignment value (Figure 26). The misalignment value in X+, X-, Y+ or Y- direction is equal to the offset value of the last pattern which has top/bottom connections (contact between top pad and the tested direction bottom pad). So, the accuracy of the proposed test structure depend on the offset values as well as the number of the used patterns.

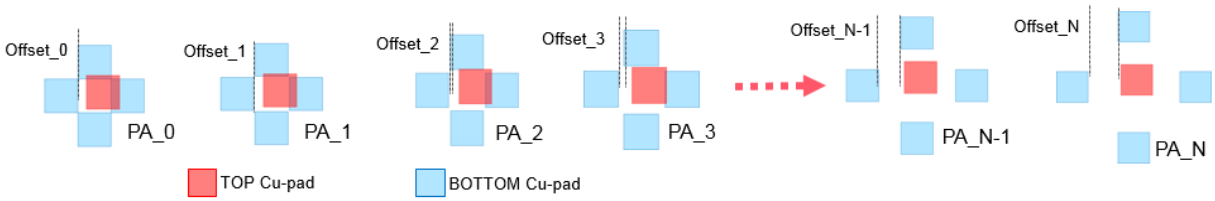


Figure 26: N patterns using different "offset" values

3. Misalignment test structure architecture

The implementation of the proposal for process development requires a probing test row to stimulus patterns. To reduce the number of test pads, the outputs are grouped to have common signals (X+, X-, Y+ and Y-) for all patterns. So, the number of patterns depends on probing test row pads. In this implementation a probing test row with 22 test pads is used: 4 test pads for the common signals (X+, X-, Y+ and Y-) and 18 for inputs patterns. The offset values will be set according to the used pitch as well as the accuracy of bonding equipment.

Figure 27 shows the architecture of the misalignment test structure. It contains 18 patterns (PA_0…PA_17) and a probing test row (22 test pads). To measure misalignment values, electrical test consists in current injection through pattern inputs and sensing outputs X+, X-, Y+ and Y- or vice versa. The layout of the proposed test structure is shown in figure 28; the area of the test structure is around 0.2 mm² and we show that the area of test pads is very large compared to that of the patterns.

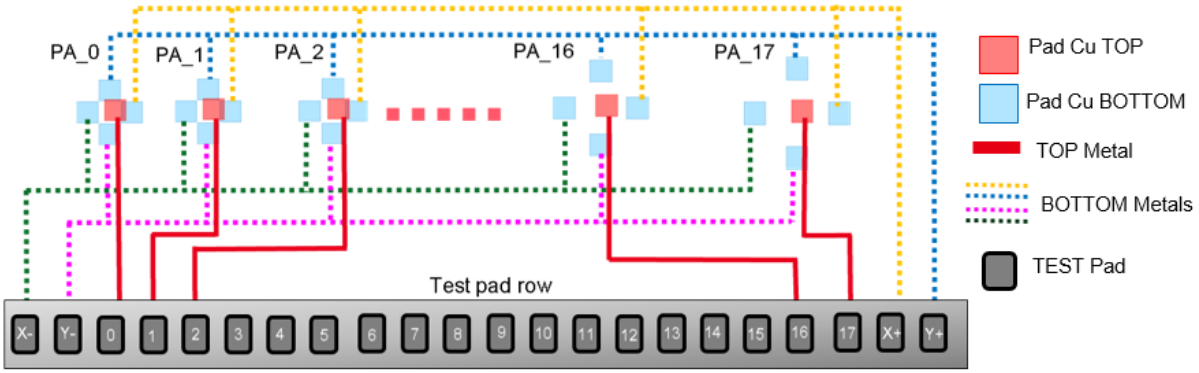


Figure 27: Misalignment test structure architecture

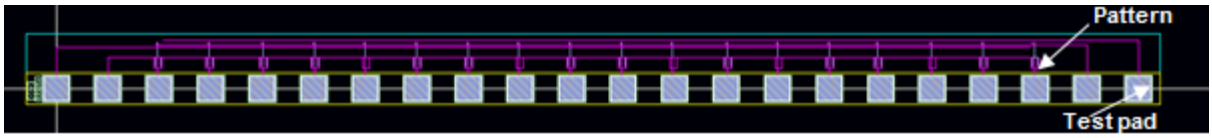


Figure 28: Layout of the proposed test structure

The test vehicle was fabricated in a Wafer-to-Wafer (W2W) assembly configuration with either a pitch of 3.42µm and 1.44µm using a very small measurement step for an accurate misalignment test structure. Table 1 shows the accuracy (step) and the offset values of the proposed misalignment test structure. We distinguish four zones; Z1, Z2 and Z3 corresponding to the coverage of the test structure while Z4 is out of the structure coverage. Due to test chip constraints, for the pitch of 3.42µm we have implemented X direction only and Y direction only with a double step of 45nm in Z1. While for the finest pitch (1.44µm), we have implemented X and Y with a step of 22.5nm to provide the best accuracy measurement.

	Bloc X only 3.4 µm Offset (nm)	**Bloc Y only 3.4 µm Offset (nm)**	**Step 3.4 (nm)**	**Bloc 1.4 µm Offset (nm)**	**Step 1.4 (nm)**	**Z**
PA_0	22.5		45	22.5	22.5	Z1
PA_1		45		45		
PA_2	67.5			67.5		
PA_3		90		90		
PA_4	112.5			112.5		
PA_5		135		135		
PA_6	157.5			157.5		
PA_7		180		180		
PA_8	202.5			202.5		
PA_9		225		225		
PA_10	247.5			247.5		
PA_11		270		270		
PA_12	292.5			292.5		
PA_13		315		315		
PA_14	360		X:67 Y:225	360	45	Z2
PA_15		540		405		
PA_16	810		X:450 Y:720	495	90	Z3
PA_17		1260		585		

Table 1: Offset values

4. Test structure validation

a) Test results: pitch 3.42µm and 1.44µm

➢ Pitch 3.42µm

After the bonding process using W2W assembly, an electrical test was performed for five multi-pitch wafers. Figure 29 shows the misalignment distributions of the five wafers using misalignment test structure (pitch =3.42µm) with 71 measurement points for each wafer (superposition for some measurements).

We distinguish four zones; Z1, Z2 and Z3 corresponding to the coverage of the test structure (see Table 1) while Z4 is out of the structure coverage. The misalignment values of W2 and W14 are located in Z1 and those of W3, W4 and W13 are in Z2 and Z3 area. For instance, in real wafers misalignment values are all included in the capability of our test structure. In addition, our design provides high resolution (45nm) for a misalignment values between 0 and 300nm (Zone 1) but this resolution decreases for higher misalignment values.

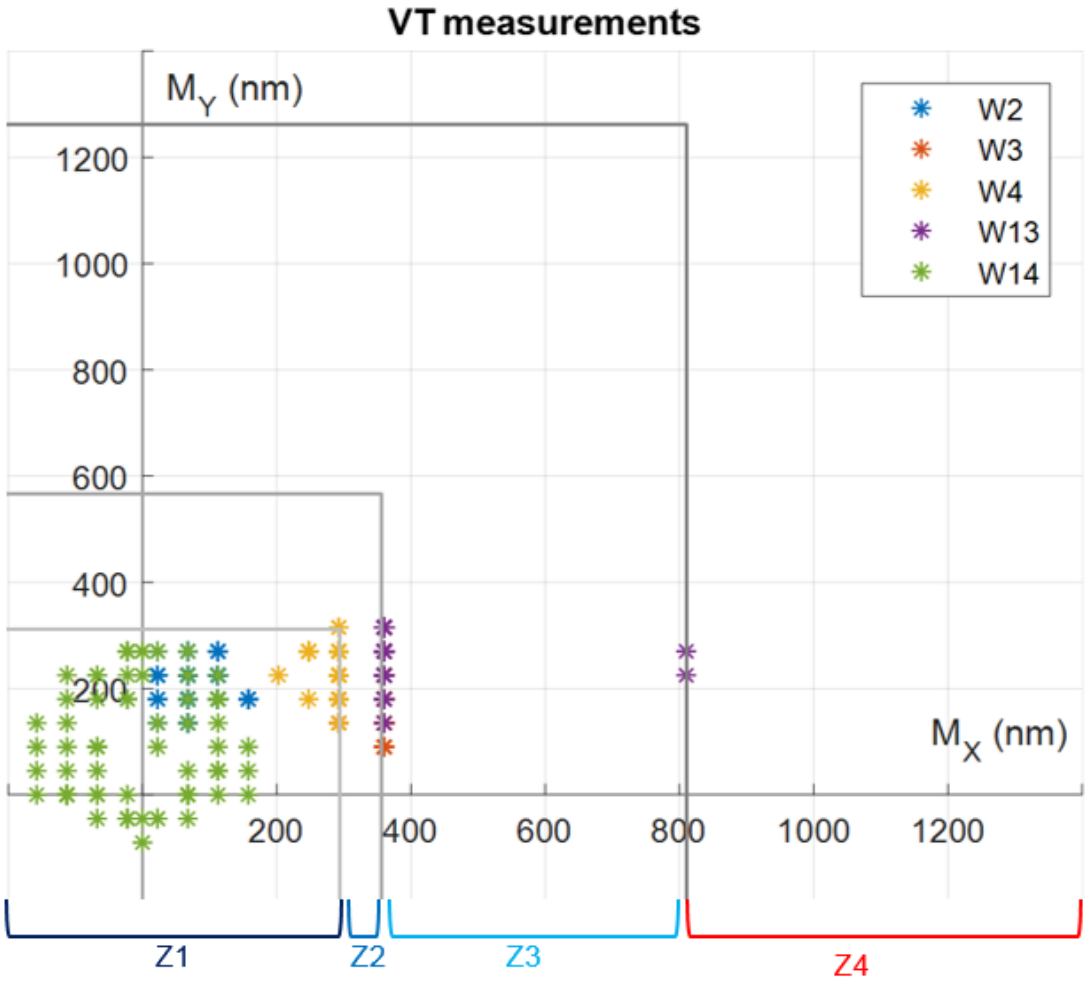


Figure 29: Misalignment test structure results (Pitch= 3.42µm)

The test coverage of the misalignment test structure is equal to 0.8µm for X direction and 1.2µm for Y direction. Using the virtual wafer vector map tool developed previously, we visualize the misalignment wafer map of the five tested wafer (see Figure 30). For W2, W3, W4 and W13 it happens that translation is the predominant effect whereas run-out is predominant for W14. Table 2 shows minimum, maximum, mean and 3sigma values for wafers.

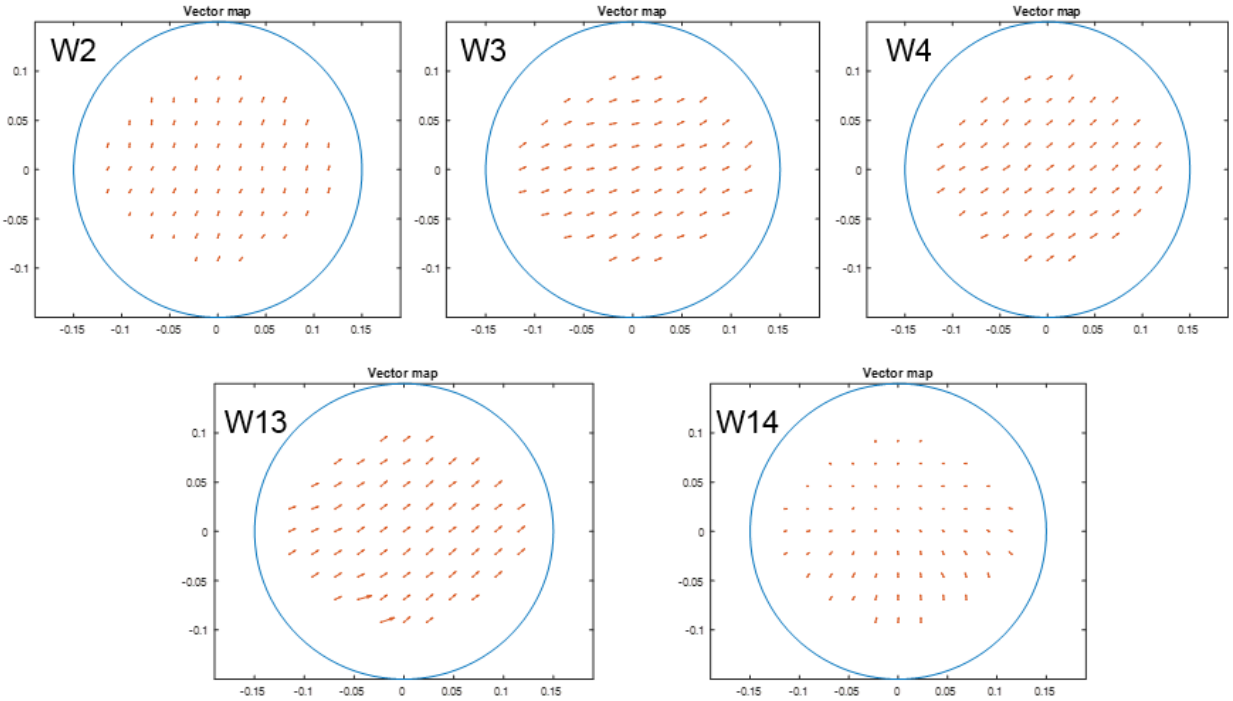


Figure 30: Misalignment wafer map for five wafers (Pitch= 3.42µm)

	W2		**W3**		**W4**		**W13**		**W14**	
Axis	X	Y	X	Y	X	Y	X	Y	X	Y
Max	158	270	360	315	360	320	810	320	158	270
Min	23	140	293	90	203	140	360	140	-160	-90
Mean	81	200	350	161	309	240	370	270	0	90
3 σ	102	90	72	147	117	120	210	150	267	330
Effect	Translation		Translation		Translation		Translation		Run-out	

Table 2: Statistical data of misalignment test results (Pitch=3.42µm)

We observe that the five wafers exhibit a different range of misalignment values; the minimum misalignment values are observed for W2 and W14 and the maximum

misalignment values are observed for W13. The 3-sigma value represents the dispersion of misalignment values and explain the distorted wafers (run-out effects).

- Pitch 1.44µm

Figure 31 and figure 32 show respectively the misalignment distribution and the wafer map of the five wafers using the test structure (pitch=1.44µm) with 71 measurement points for each wafer (superposition for some measurements). We show that the misalignment values of W2 and W14 are in Z1 area, those of W3 are in Z2 and Z3 and that and those of W4 are in Z2 (including some results in Z1). For W13 the misalignments values are in Z4 (off cover zone). Moreover, for W13 (in X direction), there are some misalignment measurements that exceed the pad size (PS) and induce an artifact on the results of Y direction.

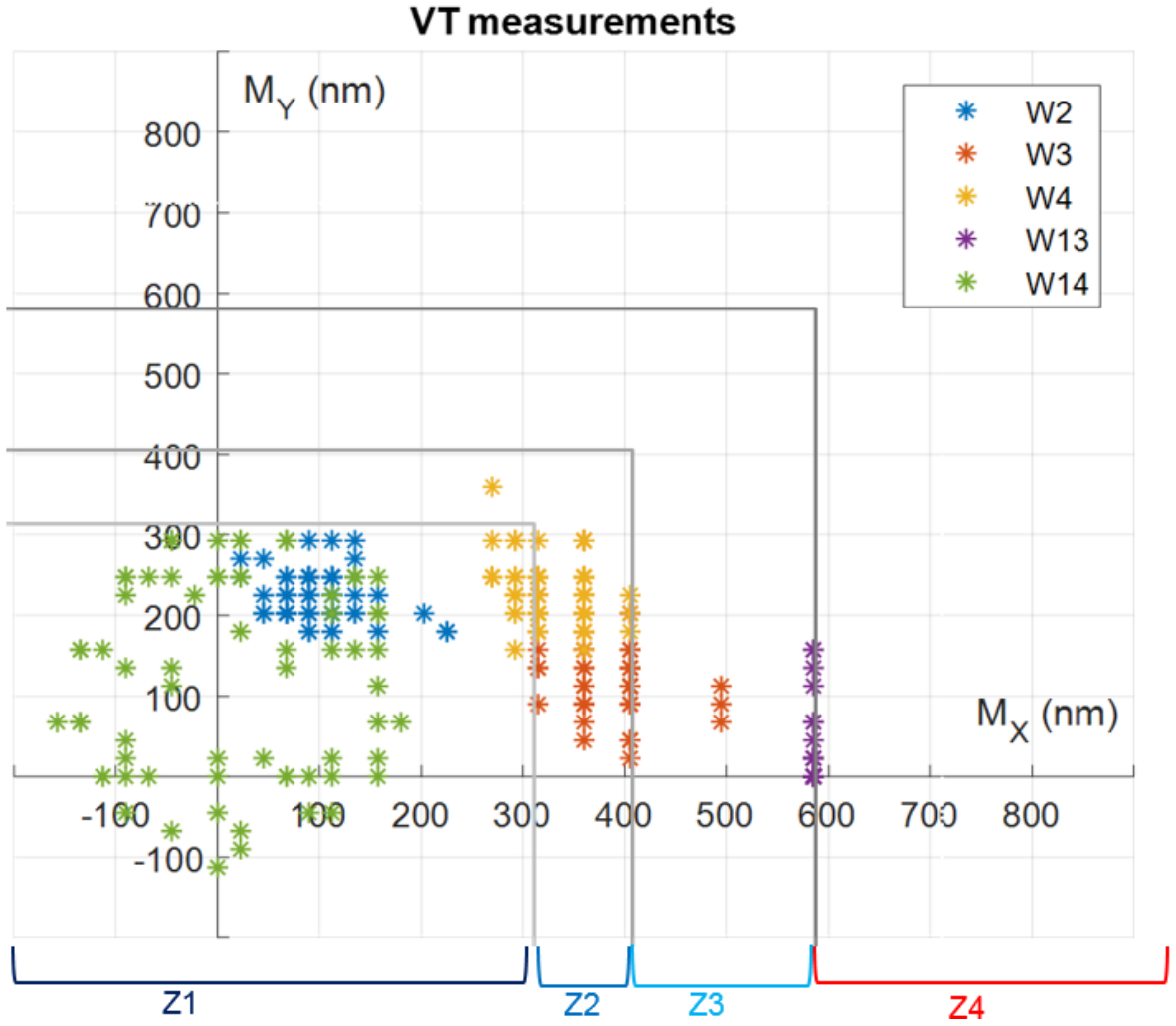


Figure 31: Misalignment test structure results (Pitch= 1.44µm)

Table 3 shows the minimum, maximum, mean and 3sigma values for each wafer. W2, W3, W4 and W14 the measurements are very close to the 3.42µm pitch results, due to the small distance between the test structures as well as the offset values. W13

misalignment values (in X direction) are greater than our actual structure's coverage. For the rest, we will not take the W13 measurements into consideration.

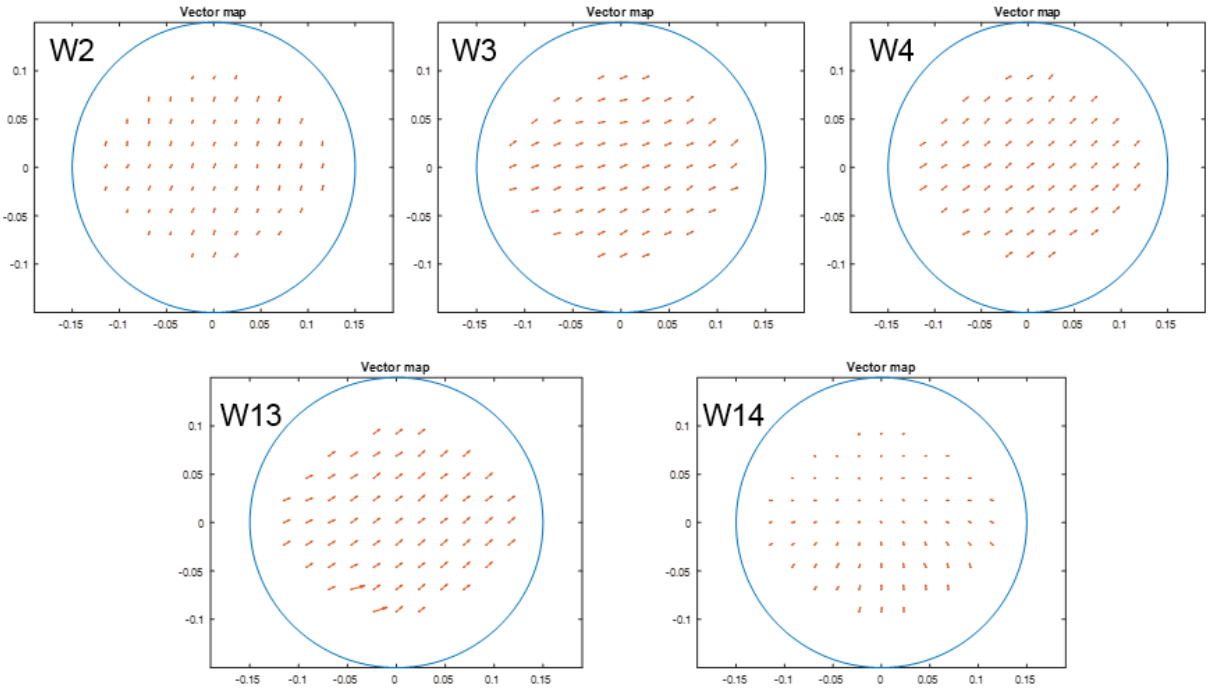


Figure 32: Misalignment wafer map for five wafers (Pitch= 1.44µm)

	W2		**W3**		**W4**		**W13**		**W14**	
Axis	X	Y	X	Y	X	Y	X	Y	X	Y
Max	225	293	495	292	405	360	585	157	180	293
Min	22	180	315	22	270	158	585	0	-158	-113
Mean	98	227	377	139	325	232	585	14	16	123
3 σ	118	91	122	176	103	113	0	117	292	364
Effect	Translation		Translation		Translation		Translation		Run-out	

Table 3: Statistical data of misalignment test results (Pitch=1.44µm)

b) Comparison of misalignment test structure results with overlay measurements

The test results of the five wafers for the pitches of 3.42 and 1.44 are similar and offer a different range of misalignment values. To validate the proposed test structure, we compare the test results with the overlay measurements obtained using IR imaging tool. Figure 33 and figure 34 show respectively the overlay measurements distribution and the wafer map of the five wafers with 71 measurement points for each wafer.

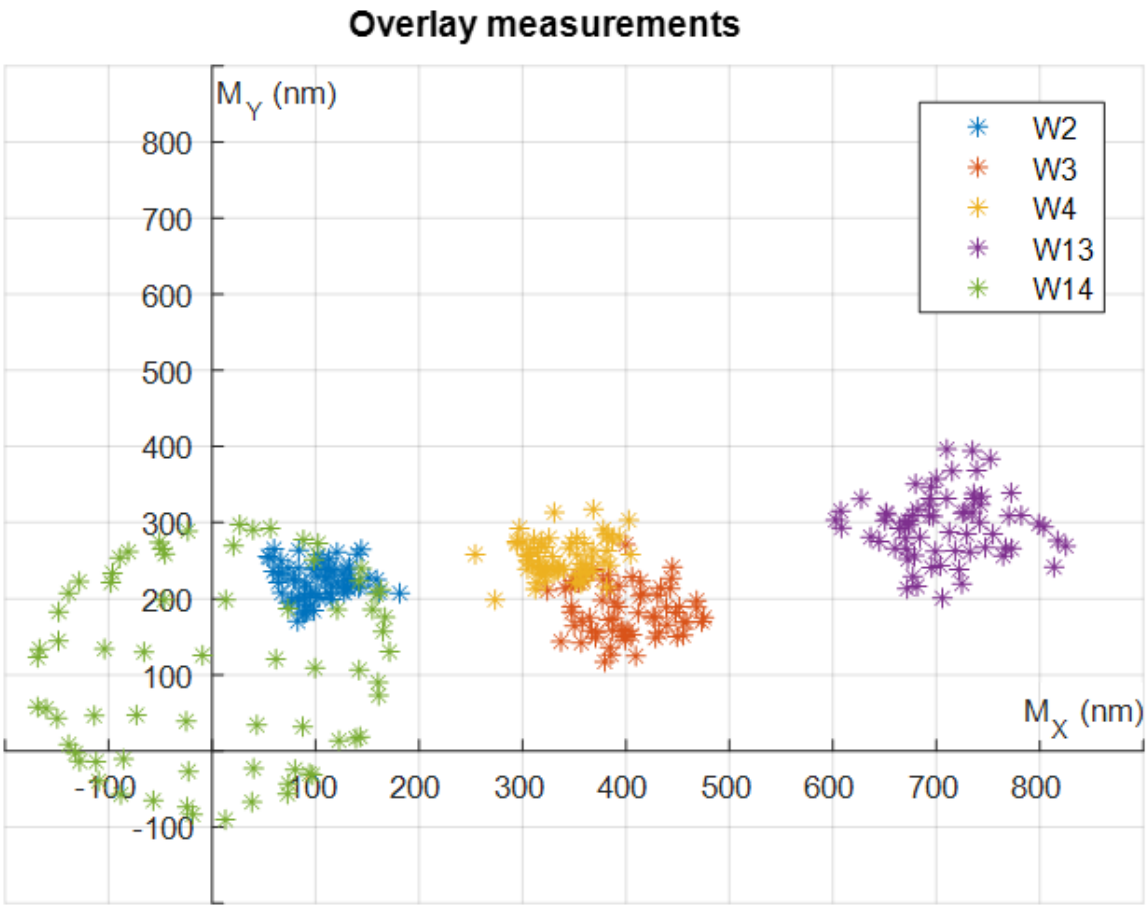


Figure 33: Overlay measurements distribution

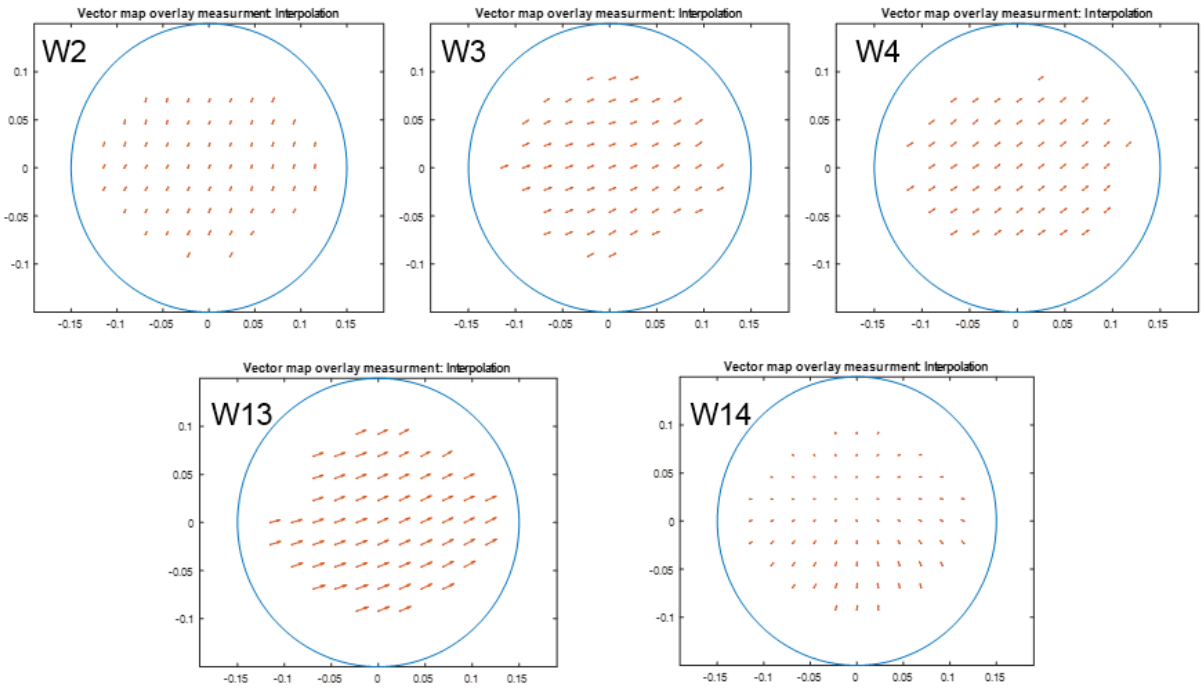


Figure 34: Wafer map results using overlay measurements

- Comparison of misalignment test structure results (pitch 3.42µm) with overlay measurement

The comparison between overlay measurements and test structures results is done using "boxplot" plots. On each box, the central mark indicates the median, and the bottom and top edges of the box indicate the 25th and 75th percentiles, respectively. The whiskers extend to the most extreme data points not considered outliers, and the outliers are plotted individually using the '+' symbol. We differentiate between overlay measurements and misalignment test vehicle results for each wafer and for 71 measurement points.

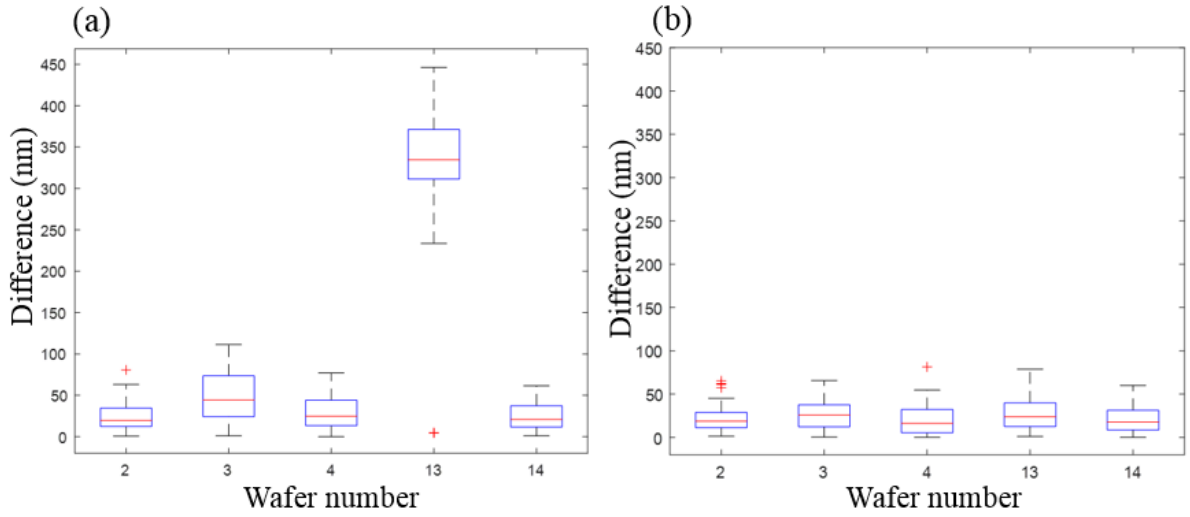


Figure 35: Comparison of test structure results (3.42µm pitch) and overlay measurements in X and Y direction

Figure 35 shows the comparison results for the five wafers in X and Y direction. For W2 and W14, we show that the most of difference values are smaller than the resolution in Z1 (45 nm), for W3 and W4 the difference is smaller than the resolution of Z2 (90nm) and Z3 (X/Y: 450/720nm) and for W13 the difference values are very high since the measurements are in Z3.

- Comparison of misalignment test structure results (pitch 1.44µm) with overlay measurement

Figure 36 shows the comparison for the five wafers in X and Y direction; concerning W2 and W14 we show that the majority of difference values are less than the resolution in Z1 (22.5 nm), for W4 and W3 the differences is respectively less than the resolution of Z2 (45nm) and Z3 (90nm). Then for W13 the differences values are very high. Because for X direction the misalignment values are in Z4 (off cover zone) and some misalignment values exceeds the pad size, it is not possible to measure misalignment in Y direction using this test structure. Therefore, we do not include the results of W13 in

the comparison. In conclusion for the wafers W2, W3, W4 and W14, we can affirm that the test structure results are aligned with conventional overlay measurements.

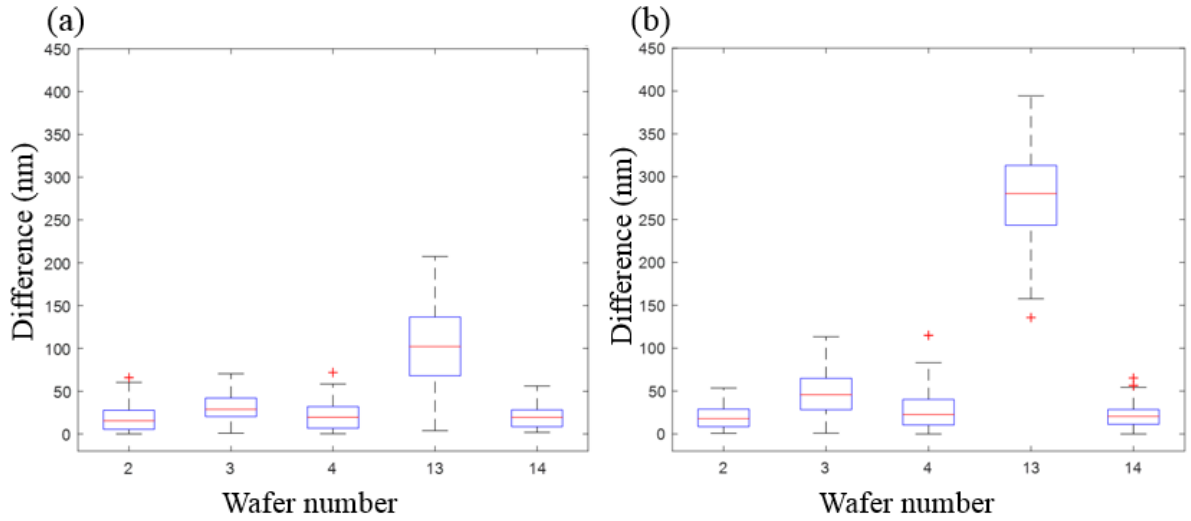


Figure 36: Comparison of test structure results (1.44µm pitch) and overlay measurements in X and Y direction

After comparison, we can claim that the test results of misalignment test structure with 3.42µm and 1.44µm pitch are aligned with conventional overlay measurements. The proposed test structure must replace the actual destructive methods to measure misalignment defect in process development phase. The accuracy of misalignment measurements, using the proposed test structure, depends on offset values. So, more patterns are needed for an accurate misalignment measurement but this increase the area of test pads. Therefore another alternative for test access is needed. In the next part, we need study the impact of this misalignment defect on resistance and capacitance parameters.

IV. Characterization of HD 3D-IC interconnect using the proposed test structure

The proposed method allows to measure misalignment values, the accuracy depends on offset values. Using the measurement values, we can estimate the contact surface and finally calculate the resistance using equation (2). The test flow is shown in figure 37.

We study the impact of misalignment defect on R and C parameters for the wafers used in III example W14 with a pitch of 1.44µm (because of the variation of misalignment values in the case of the run-out effect) using MATLAB tool. Figure 38.a and figure 38.b show respectively the resistance (of Cu-Cu pads and HBVs) and capacitance wafer map distribution (the run-out is the predominant effect).

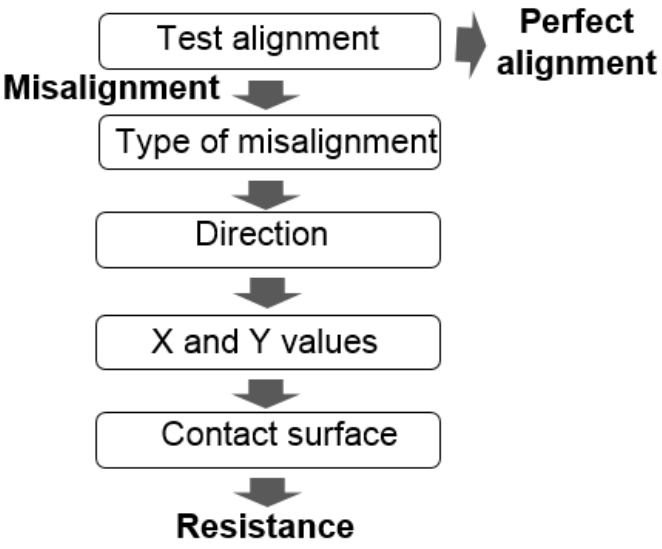


Figure 37: Overall test misalignment flow

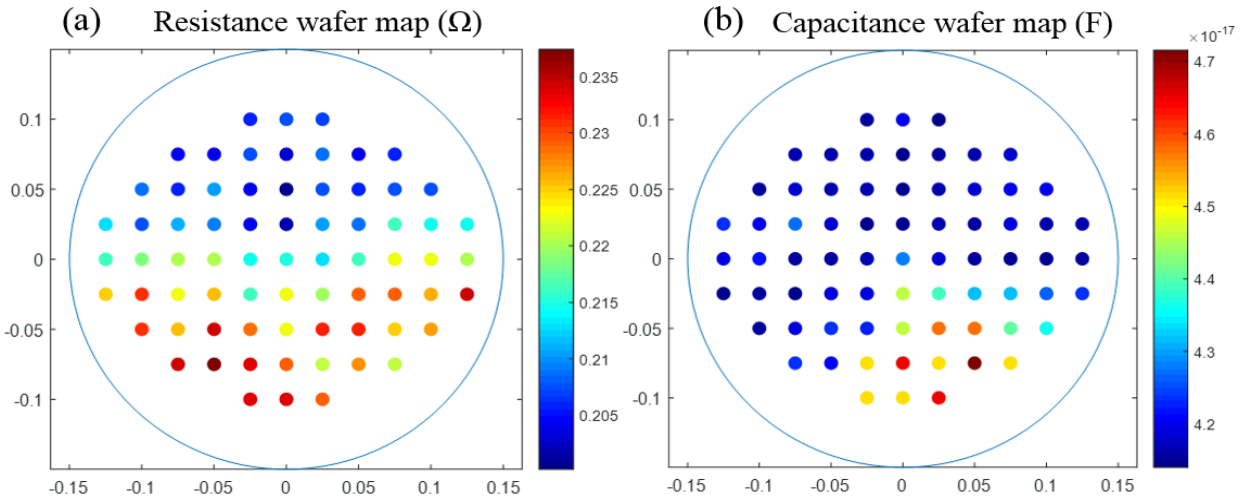


Figure 38: Resistance and capacitance values distribution (W14 with a pitch=1.44µm)

The maximum misalignment values in X and Y direction are equal to 180nm and 293nm respectively and the pad size (PS) is equal to 720nm. While the effective contact surface remains large, there is not a great variation in the resistance values; the minimum value is equal to 202mΩ and the maximum is equal to 237mΩ.

Concerning capacitance values, the distance between two adjacent Cu pads is large, so we do not have a big variation (min=0.042fF, max=0.047fF). On the contrary, the simulation of the electrical model of Cu-Cu pad (with a pitch of 1.44µm) shows that a 700nm misalignment value in X and Y direction increases significantly the resistance from 197 mΩ to 50Ω and the capacitance from 0.02fF to 0.74fF.

V. Conclusion

Our proposed misalignment test structure is based on basic reference pattern composed by a top Cu-pad and four Bottom Cu-pads. The proposed approach allows to measure accurately bonding misalignment and know the direction. The accuracy depends on offset values. The misalignment test structure was fabricated in a Wafer-to-Wafer (W2W) assembly configuration with a pitch of 3.42µm and 1.44µm using a very small measurement step for an accurate misalignment measurement (respectively 45nm and 22nm). Afterwards, the proposed was validated after the comparison of test results with overlay measurements. Finally, the impact of misalignment on R & C parameters was studied.

Benefits and drawbacks of our proposed test structure are summarized here:

- Benefits:
  - Measure accurately misalignment values
  - Know the direction of misalignment
  - Low cost
  - Reduce test time compared to overlay measurement
- Limitations:
  - Large area of test pad row compared to test patterns
  - To have more accuracy, many test patterns are needed and this increase the number of test pad rows.
  - The proposed structure does not allow to control misalignment during bonding process

The next chapters focus on the test of high-density 3D-IC interconnects at system level as well as the implementation of the proposed test structure in application circuit to assess performance of 3D-ICs.

Chapter III. Test of high density 3D-IC interconnect at system level

A 3D DFT architecture ensures the test of all the components of the 3D system including the different stacked dies and the 3D interconnections. The 3D DFT architecture must also allow the test of those components at all the 3D bonding levels: pre, mid and post-bond levels. Test infrastructure insertion for HD 3D-ICs presents new challenges because of the high interconnects density and the area cost for test features. In this chapter, we start with a state of the art of DFT architecture and a pre-analysis of the testability of HD 3D-IC; we define the most optimized Design-For-Test infrastructure depending on used standard and the minimum acceptable pitch value for a given technology node to ensure the testability of circuits. Afterwards, we propose an optimized DFT architecture allowing pre-bond and post-bond for high-bandwidth and high-density 3D-IC application (SRAM-on-Logic) in line with the ongoing IEEE P1838 standard.

I. State of the art

There exists the widespread use of embedded instruments (i.e. BISTs) each of which is accessed and managed by a variety of external controllers using a variety of mechanisms and protocols. Therefore, a need exists for standardization of these methods in order to unify and facilitate test access and control. Figure 39 shows the history of test standards. In the 90‟s, The Joint Test Action Group (JTAG) developed the initial approval boundary-scan standard that was standardized in 1990 as the IEEE Std. 1149.1-1990 [57] that allows the test of integrated circuit as well as interconnections between circuits on a printed circuit board (PCB). The JTAG standard allows the test circuits without using test needles. In 1994, a supplement that contains a description of the Boundary Scan Description Language (BSDL) was added which describes the boundary-scan logic content of IEEE Std 1149.1 compliant devices. Since then, this standard has been adopted by electronic device companies all over the world.

In 2005, the IEEE 1500 standard is approved [58]. It addresses the test of individual cores in complex integrated systems. The same principle is implemented as before on boards where individual circuits are independently tested thanks to the boundary scan strategy. The IEEE 1500 is inspired from JTAG with some modifications and adaptations

for core based circuits testing, especially by removing the JTAG finite state machine and replacing it by direct access controlling pins for parallel test. Nine year later, the IEEE P1687, also known as Internal Joint test Action Group (IJTAG), is approved [59] to facilitate the use and reuse of internal instrumentation by providing a standard yet flexible network architecture for accessing the instruments and standard descriptions of both the network and the operation of the instruments.

In January 2010, the IEEE 3D-Test Study Group was tasked to investigate whether or not there was a need and industrial support for one (or more) test and/or design-for-test standards in the domain of 3D integration, and whether the timing was right to start developing these standards. This led to the formulation of a Project Authorization Request (PAR) in November 2010, entitled "Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits". The PAR was approved by IEEE-SA's New Standards Committee (NesCom) on February 2, 2011, after which the Study Group transitioned in a Working Group, and the development on Project P1838 was started [60].

Actually, the P1838 standard is in evolution process [61]. The proposal facilitates data transport and test signal routing, addresses the test signal routing problem and creates die-level wrappers to partition on-die logic and to parallel test of 3D interfaces. It also aims to optimize the protocol and description language for test logic insertion, test patterns generation and to differentiate pre-, mid- and post-bond test.

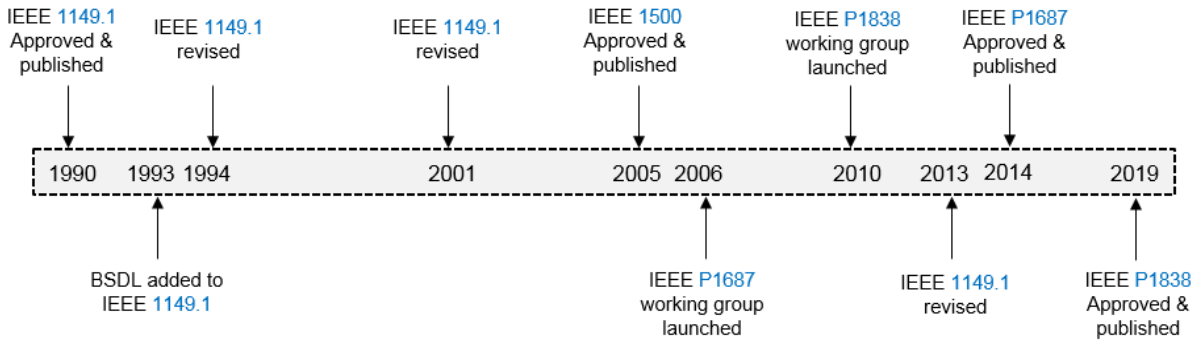


Figure 39: History of DFT test standards

The definition of test infrastructure and related test flow is thus more complex in 3D than for 2D equivalent systems and require appropriate solutions. Moreover, in high-density 3D context, it's necessary to detail all test standards and evaluate the area overhead of the test infrastructure. Our aims is to determine the most adapted test standard to high-density 3D-ICs.

1. IEEE 1149.1 (JTAG)

The IEEE 1149.1 test architecture offers the capability to test efficiently components on PCBs. The JTAG architecture tests pin connections without using physical test probes and captures functional data while a device is operating normally. The boundary scan

test standard uses four required pins Test Data Input (TDI), Test Data Output (TDO), Test Mode Select (TMS), and Test Clock Input (TCK), and one optional pin, Test Reset input (TRST). Figure 40 shows the principle of 1149.1 boundary scan test. In the "functional" mode, Boundary-Scan-Registers (BSRs) have no effect on the operation of the component. But in "test" mode, the cells isolate the functional core of the external pin component. BSRs force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results.

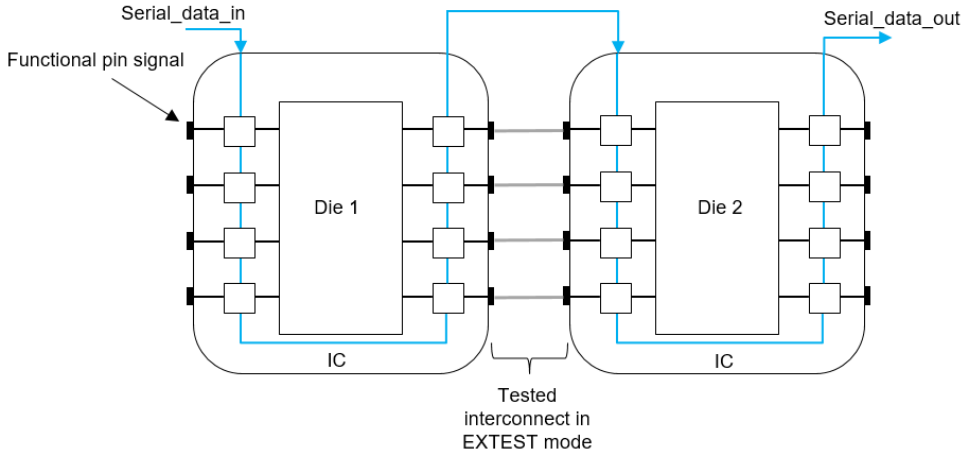


Figure 40: IEEE 1149.1 boundary scan test

The structure of BSR contains an input and output MUXs and two storage elements connected between the Cell Functional Input (CFI) and Cell Functional Output (CFO) (Figure 41). The first one is a shift register, moves the value from CFI or Cell Test Input (CTI) to Cell Test Output (CTO) and the second one is an output register moves the value from CTI or CFI to CFO. The boundary scan logic was described using BSDL language.

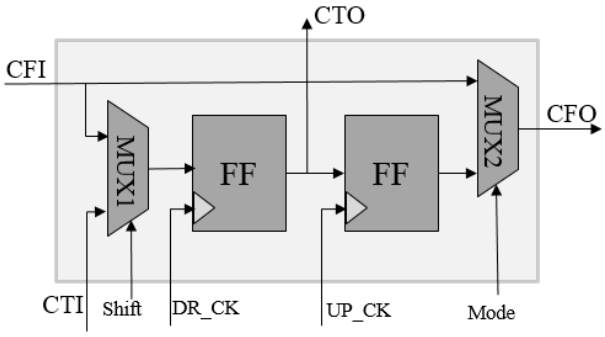


Figure 41: Boundary-Scan-Register (BSR) architecture

The JTAG standard was widely used for 2D circuits and it's supported by many test equipment's and industrial tester. Similarly in 3D context BSRs provide isolation for internal testing (INTEST); this mode is used when input vectors need to be applied to the core and the core response needs to be observed at the output. The BSRs on the core inputs provide controllability, and the BSRs on the core outputs provide observability.

Moreover, the BSRs placed between the I/O ports and the die allows also to test 3D-IC interconnects using external test instruction (EXTEST).

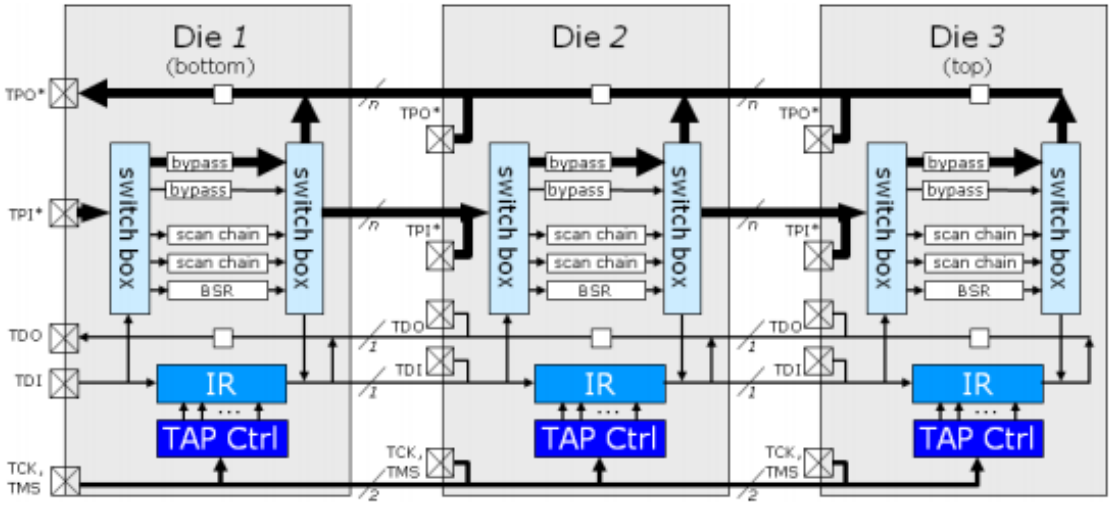


Figure 42: 3D DFT architecture based on IEEE 1149.1 (source [62])

In contrast with 2D circuits, 3D-ICs need to be tested during different stages of their fabrication process: pre, mid, and post-bond, which requires specific DFT architecture to enable the test during all these levels. An example for using IEEE 1149.1 standard in 3D-IC [62] is shown in figure 42, where JTAG I/Os are embedded in the bottom die (Die 1), and TSVs are added to transfer test data up and down in the 3D stack. The 3D stack becomes similar to a PCB, with a serial chain of JTAG TAP controllers from bottom to top, where only the bottom die can be accessed using tester. The pre-bond test access is done through the die TAP controller, as the usually with 2D circuits. The post-bond test access is done through the bottom die TAP controller, test sequence and instructions are shifted in serial to each die from the bottom die to the middle die to the top die using TSVs. As a conclusion, the JTAG interface, uses only 4 I/Os and 1 optional, which can be considered as an important advantage for test access but serial test data insertion requires a long test time, moreover the cost of BSR structure is still major issue.

2. IEEE Std 1500

The IEEE Std 1500 standard was originally created to solve testability issues of complex 2D System-On-Chips (SoCs) containing many cores with high interconnection rate to reduce the test time using serial and parallel Test Access Mechanisms (TAMs) and a rich set of instructions.

Figure 43 shows the principle of IEEE Std 1500, a serial port WSI-WSO is mandatory and used for both loading wrapper instructions as well as for low-bandwidth test data. An optional parallel port WPI-WPO can carry higher-bandwidth test data. In addition, IEEE Std 1500 defines features that enable core isolation and protection.

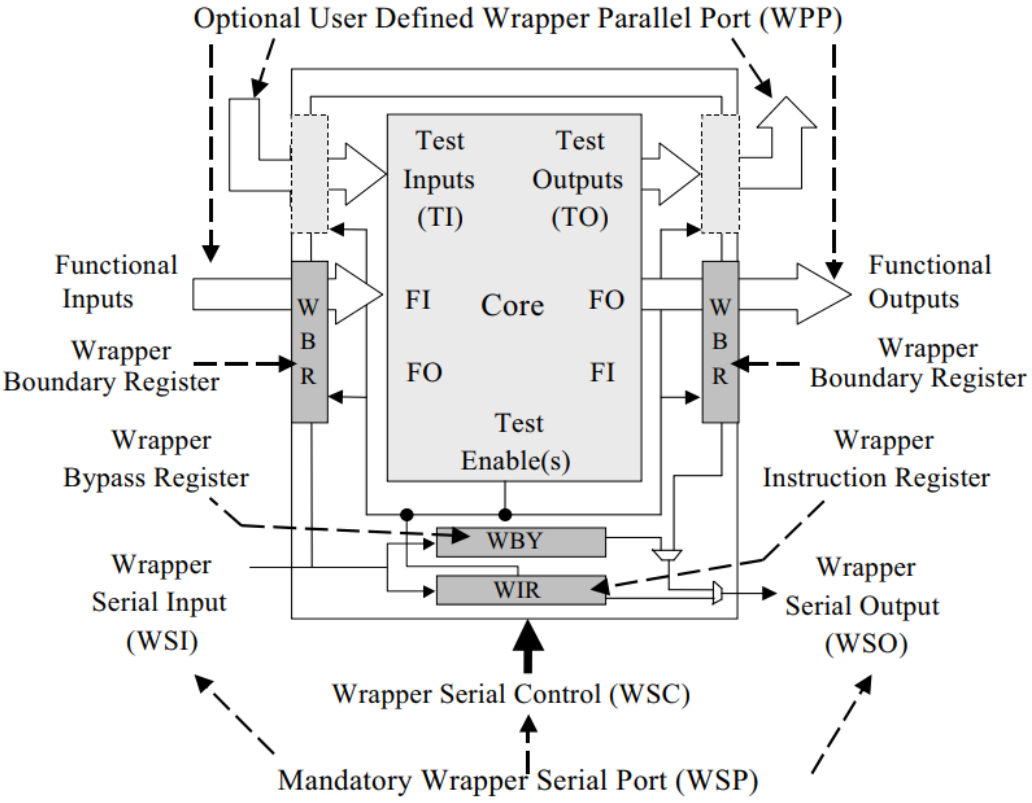


Figure 43: IEEE Std 1500 wrapper components (source [58])

The Wrapper Boundary Register (WBR) (Figure 44) contains only one storage element between CFI/CFO and CTI/CTO used to provide controllability, observability and shift capabilities. The combination of a pseudo-static wrapper instruction, shifted into the Wrapper Instruction Register (WIR), and the values on the Wrapper Serial Control (WSC) signals determines the operation of the wrapper.

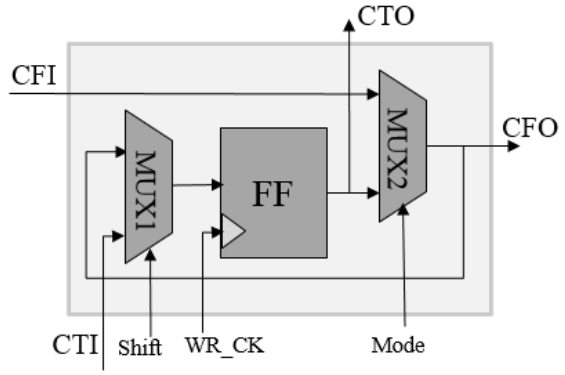


Figure 44: Wrapper-Boundary-Register (WBR) architecture

Stacked dies in a 3D-SIC can be considered similar to embedded cores in a System-on-Chip (SOC). Figure 45 shows the 3D DFT architecture based on IEEE Std 1500. The main features of this architecture are the good support of parallel testing using the WPI and WPO signals which are distributed using 3D-IC interconnects (TSVs and µ-bumps/ Cu-Cu) [62], [63]. We show also that the IEEE 1149.1 (JTAG) interface is used in the

bottom as a TAM. The JTAG TAP controller uses only the three JTAG inputs TRST, TCK and TMS to generate the six IEEE 1500 control signals Wrapper Serial Control (WSC) to all the IEEE 1500 wrappers in the different dies of the stack. This is done in order to limit the added I/Os of the 3D-IC [58].

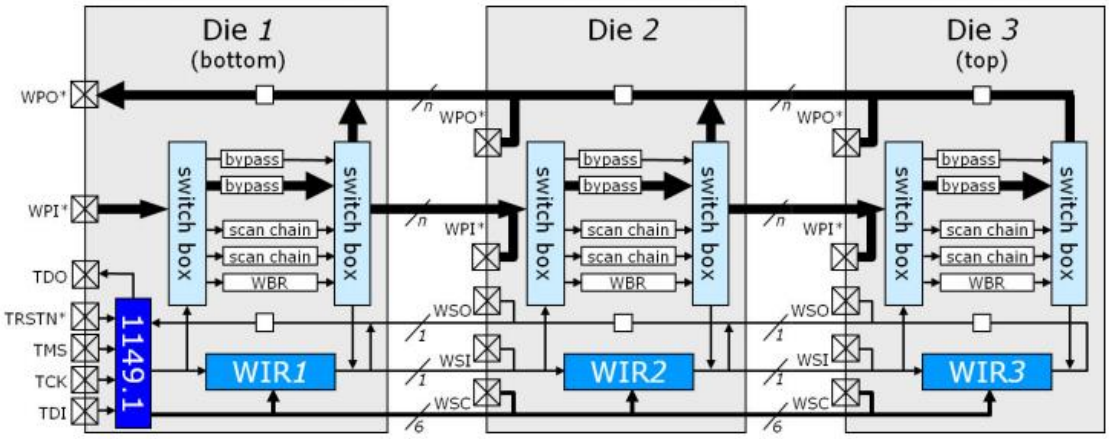


Figure 45: 3D DFT architecture based on IEEE 1500 (source [62])

The shown architecture allow 3D test at all bonding levels including pre, mid, and post bond levels. The 3D-DFT architecture contains a dedicated probe pads for pre-bond testing of non-bottom dies (Die 2 and Die 3), and "Test Elevators" to drive test signals up and down during mid-bond and post-bond test. The WBRs allows wrapper cells with an update register such as in the IEEE Std 1149.1 wrapper cell shown. Moreover, WBRs offer an optimized structure allows to captures from the net after the multiplexer to test the functional path through that multiplexer, unlike the 1149.1 cell.

3. IEEE P1687 (IJTAG)

The IEEE P1687 (IJTAG) seeks to optimize the access methods to embedded test and debug features via the IEEE 1149.1 TAP and additional signals that may be required. Figure 46 shows a conceptual IEEE P1687 network configuration that supports multiple instruments (i.e. BIST, LBIST, and MBIST …) and includes an element known as a Segment-Insertion-Bit (SIB) to allow the overall scan chain to be of variable length. The instruments are interfaced with the scan path via Test Data Registers (TDRs) with parallel I/O which corresponds to the BSR structure (Figure 41). The IEEE P1687 standard introduces two high level languages: Instrument Connectivity Language (ICL) which describes the instruments port functions and logical connection to other instruments and to the IJTAG TAP and Procedural Description Language (PDL) which describes how an instrument should be operated.

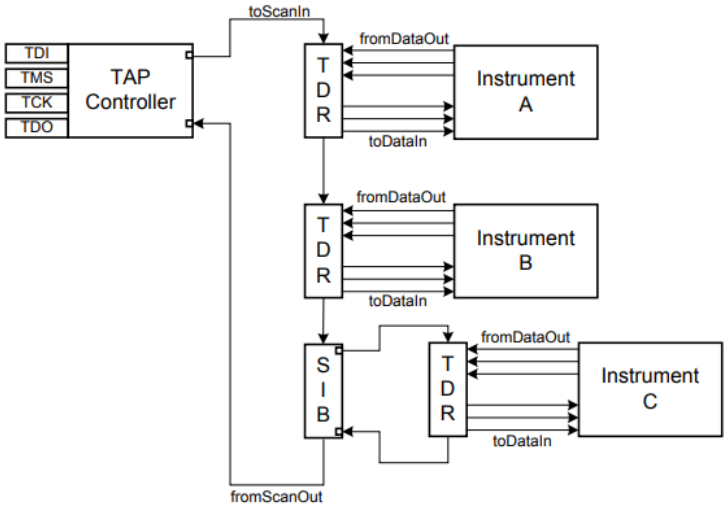


Figure 46: Conceptual IEEE 1687 network

Figure 47 shows a complete 3D DFT architecture, based on IEEE P1687, to test the "multi-chiplet" active interposer 3D system shown in chapter 1. The "chiplet footprint" offering a modular and configurable TAP chain, to test 3D active and passive interconnects [64].

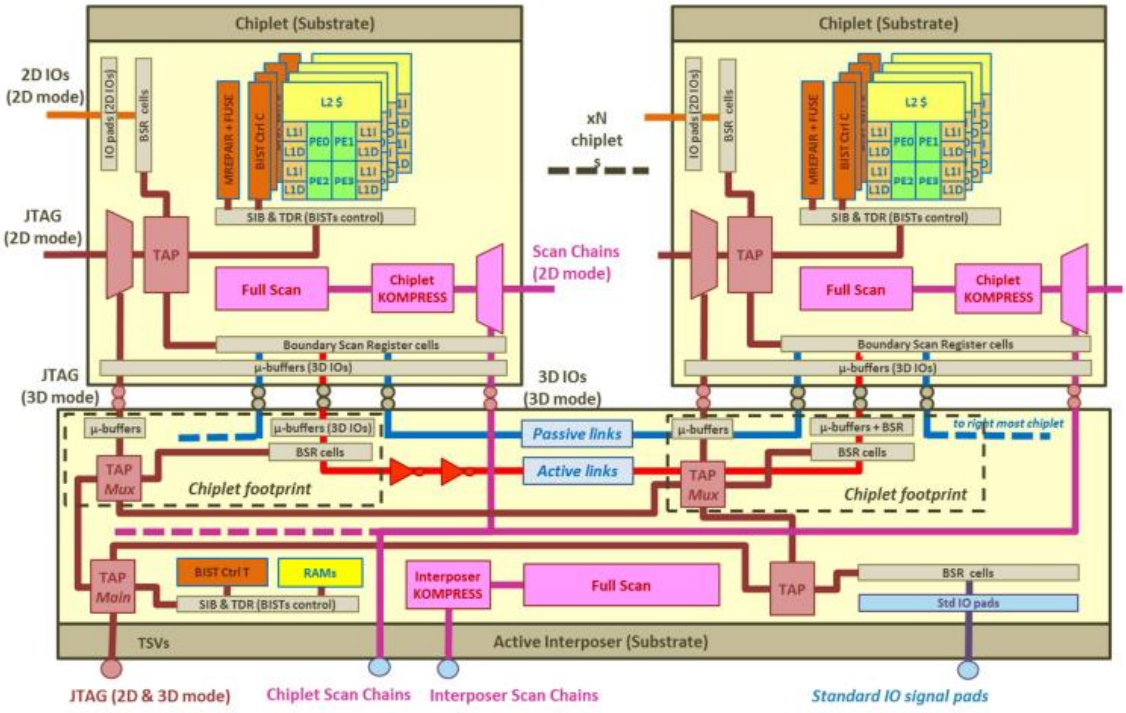


Figure 47: 3D DFT architecture based on IEEE P1687 (source [64])

In 3D context, the IJTAG offers the possibility of 3D test pattern retargeting by easily generate test patterns to support of pre-bond, post-bond and 3D interfaces test as well as reduces test time using different test parallelism options [64], [65], [66] . But, the structure of the TDR is similar to that of BSR (IEEE 1149.1) that it imposes an incremental cost compared to IEEE 1500 WBR.

4. IEEE Std P1838: 3D Test standard

The aim of IEEE Std P1838 is to define a standardized and scalable generic test access architecture between dies in 3D-ICs. The focus of the standard is on testing the intra-die circuitry as well as the inter-die interconnects in pre-bond, mid-bond, and post-bond cases in pre-packaging, post-packaging, and board-level situations. The IEEE Std P1838 standard consists of three main components: Serial Control Mechanism (SCM), Die Wrapper Register (DWR), and Flexible Parallel Port (FPP). SCM and DWR are 3D extensions of existing standards, respectively IEEE Std 1149.1 and IEEE Std 1500.

The IEEE Std P1838 uses the same structure of boundary scan cell as IEEE Std 1500 with two MUX and one storage element (Figure 44) that offer an optimized structure of wrapper boundary cell compared to IEEE 1149.1 standard that provide test controllability and observability and hence enable a modular test approach by supporting the internal test of dies (INTEST test mode) and the test of the 3D interface (EXTEST test mode).

P1838's FPP is an optional, scalable multi-bit test access mechanism that offers higher bandwidth compared to the one-bit ('serial') mandatory part of P1838 [67], [68]; using only a serial port would require millions of clock cycles only to shift in one test pattern, leading to significantly longer test times. Therefore, using FPPs that can transport multiple stimulus and response bits simultaneously becomes highly preferable to reduce the test time.

Relative to the die, the adjacent die connected in the direction of the external I/Os is referred to as the previous die; the collection of signals going to the previous die is referred to as the primary interface of this die. IEEE Std 1838 assumes that every die has a single primary interface, which connects to its unique previous die; an exception is the first die, for which its primary interface connects to the external system. Relative to the external stack I/Os, an adjacent die connected to this die in the opposite direction, (i.e, away from the external I/Os), is referred to as a next die; the collection of signals going to a next die is referred to as a secondary interface of this die.

Figure 48 shows the serial control mechanism for a middle die with two secondary interfaces. The primary interfaces are implemented at the bottom-side of each die and the secondary interfaces are implemented at the top-side of each die, the logic die contains all external I/Os as its primary interface and the secondary interface of the logic die is connected to the primary interface of the memory die. The serial control mechanism, equipped with an IEEE 1149.1 TAP, this interface allow to transports instructions, configuration data, test stimuli and test responses. The main originality of IEEE 1838 standard is the development and the standardization of a flexible parallel port (FPP) to provide more test bandwidth than the one-bit test access and an additional flexibility and configurability compared to the conventional parallel port.

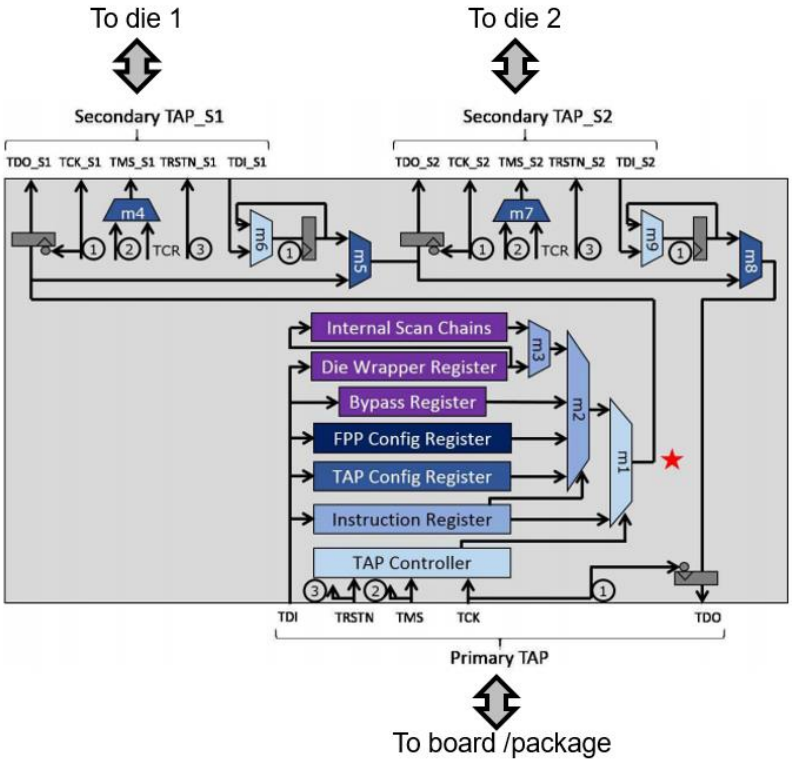


Figure 48: Serial control mechanism (SCM) (source: [68])

5. Conclusion

A Design-For-Test (DFT) test access infrastructure is indispensable to achieve a high-quality test; some DFT structures are used such as internal scan chains, built-in self-test (BIST, Memory BIST) and BSCs around the embedded cores to provide isolation for internal testing (INTEST) and also external testing (EXTEST) of the 3D-IC interconnects between dies without requiring access to the entire die. According to the test standards detailed previously, we can affirm that WBR (IEEE 1500) and the DWR (IEEE 1838) offer a reduced structures (see Table 4). For timing reasons, the WBR/DWR must be close to the 3D interconnect to reduce the functional path length and the test time. For HD 3D circuit, the limited space for WBR/DWR cells must be taken into account (the available area per interconnect =3D-Pitch^2). So, a comprehensive study of the testability of high density 3D-IC on different stacking modes (F2F and F2B) need to be provided.

Test standard	Boundary scan name	Components
IEEE 1149.1	BSR	Scan flip-flop+ Mux+ flip-flop
IEEE 1500	WBR	Scan flip-flop+ Mux
IEEE 1687 (IJTAG)	TDR	Scan flip-flop+ Mux+ flip-flop
IEEE P1838	DWR	Scan flip-flop+ Mux

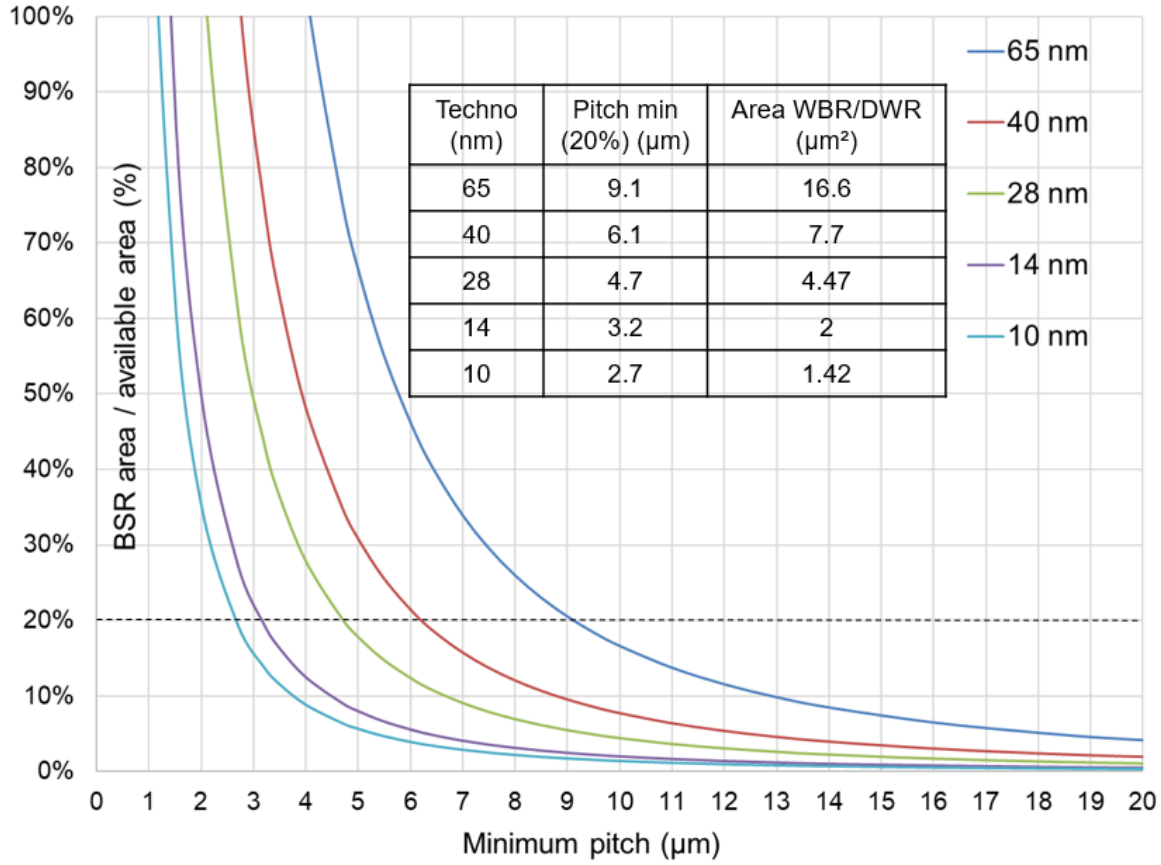
Table 4: Test standards comparison

II. Testability of high-density 3D-IC interconnects

Based on the WBR/DWR cells shown previously, we analyze the testability of 3D-IC interconnects using different technologies (65nm, 40nm, 28nm, 14nm and 10nm) in F2F and F2B stacking modes. Unlike coarse-grained 3D-IC where WBR/DWR with large pitches could be put either put apart or outside the matrix of TSV/bumps, in HD 3D-IC we aim at testing large side number of interconnects and we cannot enforce to have the DFT logic apart the HD-3D connection. This gives us the constraint to have the DFT logic within the pitch, while leaving enough place for the connection and some logic. It appears that a percentage of test infrastructure equal to 20% of the total available area seems a reasonable target value. For simulation we suppose that all 3D interconnects are tested but in reality a test is required only for functional inputs and outputs.

1. Face-to-Face (F2F)

Taking into account the previous hypothesis, we analyze the testability of 3D-IC interconnects using different technologies (65nm, 40nm, 28nm, 14nm and 10nm) in face to face stacking mode, in this case the total available surface for logic per interconnect is equal to Pitch². The area of WBR/DWR is the sum of the area of scan flip-flop and a multiplexer 2 to 1.



Techno (nm)	Pitch min (20%) (µm)	Area WBR/DWR (µm²)
65	9.1	16.6
40	6.1	7.7
28	4.7	4.47
14	3.2	2
10	2.7	1.42

Figure 49: Variation of the ratio between the area of WBR/DWR and the available area as a function of the minimum pitch (Face-to-Face)

Figure 49 shows the variation of the ratio between the area of the WBR/DWR cell and the available area as a function of the minimum pitch in F2F staking mode and the associated table shows the minimum pitch values at 20%. For example, we show that the minimum pitch using WBR/DWR, techno 28 nm and a percentage of test infrastructure of 20 % is equal to 4.7µm. If the used pitch is larger than the minimum pitch value, then the WBR/DWR cell must be integrated within the pitch. On the contrary, if the used pitch is smaller than the minimum pitch, the insertion of wrapper register cells becomes impossible.

2. Face-to-Back (F2B)

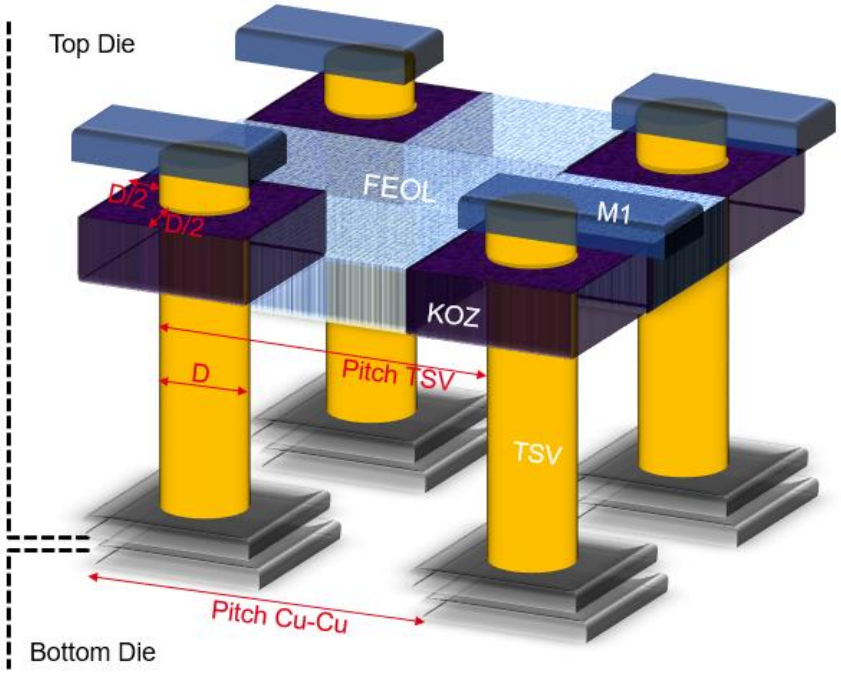
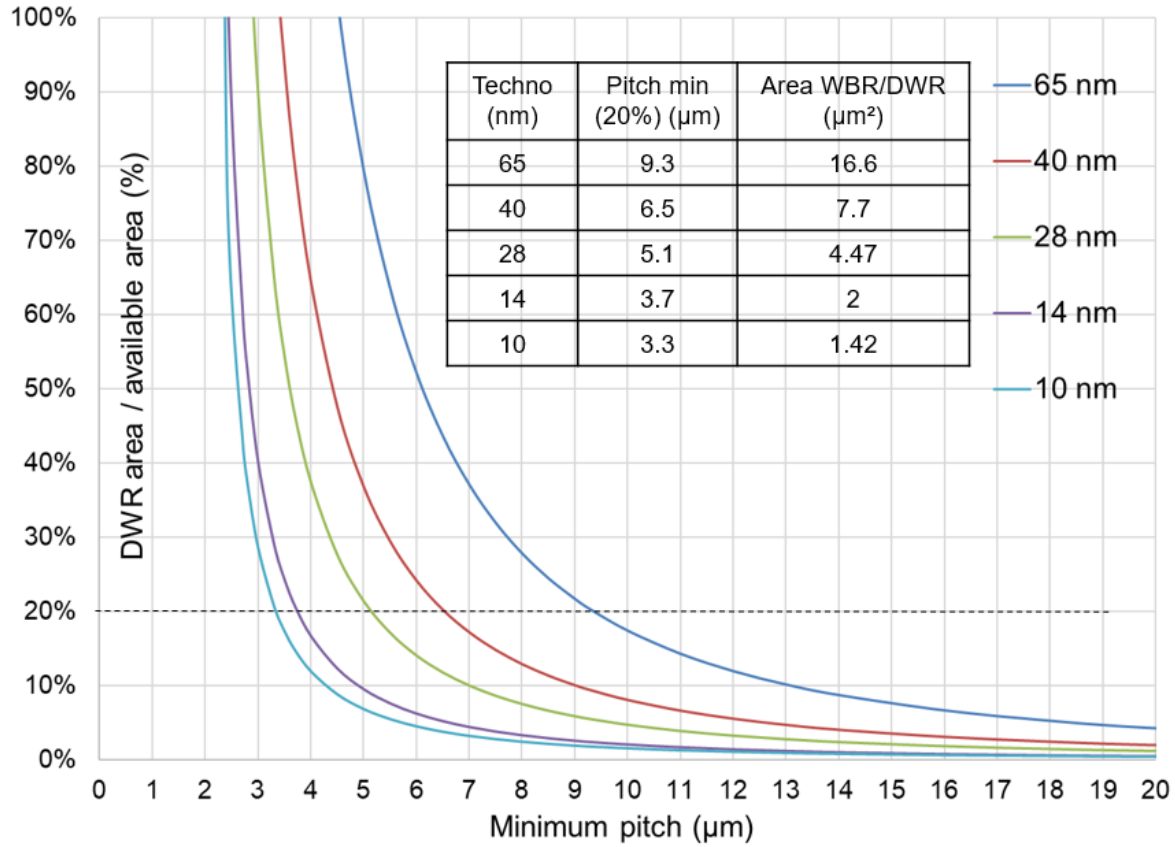


Figure 50: 3D view of 3D-IC interconnects (Face-to-Back stacking mode)

In the case of the Face-to-back (F2B) stacking mode, the FEOL (Front-End-Of-Line) of a first die is bonded with metal interconnect side of the second die using TSVs. The size of TSV's and Keep-Out-Zone (KOZ) surrounding TSVs reduce significantly the available for cells placement area. Figure 50 shows the 3D view of 3D-IC interconnects, we consider that the size of the KOZ is twice of the TSV diameter (D) and the pitch TSV is equal to the pitch of Cu-Cu interconnects.

Figure 51 shows the variation of the ratio between the area of the WBR/ DWR cell and the available area as a function of the minimum pitch in the F2B stacking mode using different technologies and a TSV diameter of 1µm. We show that TSV and KOZ sizes have a significant impact on the minimum pitch value. For example, we show that the minimum pitch using DWR/WBR, techno 28 nm and a percentage of test infrastructure of 20 % is equal to 5.1µm.



Techno (nm)	Pitch min (20%) (µm)	Area WBR/DWR (µm²)
65	9.3	16.6
40	6.5	7.7
28	5.1	4.47
14	3.7	2
10	3.3	1.42

Figure 51: Variation of the ratio between the area of WBR/DWR and the available area as a function of pitch (Face-to-Back)

3. Interpretation

The performed pre-analysis allows to evaluate the testability of high density 3D-IC interconnects in F2F and F2B stacking style. We show that the area of WBR/DWR is very large and increase the authorized minimum pitch value. Moreover, only the gross area of the WBR/DWR was taken into account and not the scan flip-flop and multiplexer standard cell size (Length, Width), which complicates the insertion of wrapper cells for high-density 3D-IC interconnects. In the other hand, in F2B stacking mode, the TSV and KOZ reduce greatly the available area.

According to the obtained results we can distinguish two cases:

- The first case when the used pitch is above the minimum pitch, here we use the classical test infrastructure to test all 3D-IC interconnects.
- The second case when the used pitch is below the minimum pitch, in this case we cannot insert wrapper cells within the pitch unless a more aggressive CMOS technology node is used. Otherwise, only a few number of 3D interconnects can be tested or a low cost test structures must be used to detect structural defects interconnects (misalignment, µ-voids at bonding interface, open defects) on HD 3D-IC. Alternatively an innovative test strategy, based on

optimization of the test infrastructure must be developed for high-bandwidth and high-density 3D-IC application.

III. Proposed DFT architecture for 3D SRAM-on-Logic partitioning

1. Overview

High-density 3D integration meets the need for some applications (i.e. smart imagers, high performance computing ...); the use of a fine pitch 3D-IC interconnects reduce the wiring distance between dies and increase the interconnection density which provides a higher bandwidth, lower power consumption and a reduced latency. In addition to a logic units and processing elements, the applications mentioned before contain also a large local memories (DRAM, SRAM …). These advanced nanoscale pitch 3D technologies nevertheless present some rather similar design challenges in terms of design partitioning, physical implementation and thermal dissipation. In the other hand, test access infrastructure is indispensable to achieve a high-quality test of 3D-ICs.

In this part, we will explore different ways of testing interconnects of high density stacked Memory/Logic 3D-IC both in the presence and in the absence of a boundary scan interface. Memory dies are typically tested using MBIST, which perform high quality at-speed tests. One or several of MBISTs might exist in the stack simultaneously and their number is a trade-off between area, test time, etc. The same engines must be used in pre-bond and post-bond-test of memories. A Built-in-Self-Repair (BISR) can be associated with the MBIST to repair memories; the MBIST generates test patterns (algorithms) and detect fault in SRAM which is under test and then the faulty information is given to the BISR, if the faulty memory is repairable, repair solutions are used to replace faulty lines by a spare lines. The logic dies are tested using WBR/DWR cells in all digital I/Os. Another part that requires testing in 3D-ICs are the vertical interconnects.

The state-of-the art in testing of 3D-ICs assumes mainly the presence of scan chains and DWR cells on each die for pre-bond testing, which are also used to perform post-bond test (functional interconnects test). According to pre-analyses carried out previously and because of the aggressive interconnect density, we distinguish two cases: (1) if the used pitch is above the minimum pitch, MBIST is used for pre-bond and post-bond test of the memory die, DWR cells are used for pre-bond and post-bond test of logic die and also used to test 3D-IC interconnects. (2) On the contrary, if the used pitch is below the minimum pitch, we can test memory die (using MBIST) but the insertion of wrapper cells within the pitch, to test logic die and 3D interconnects, becomes impossible. In this case, depending on the used pitch, a few number of WBR/DWR cells must be inserted to test some 3D interconnects but using this alternative we cannot achieve sufficient test coverage. Another method must be used consists on the optimization of the WBR/DWR:

except not registered I/O (i.e. Clock, voltage) that need a dedicated WBR/DWR, most die I/Os are equipped with a functional register which can be reused and turned into a shared wrapper cell [69]. Figure 52 shows the dedicated and the shared wrapper cell. For shared wrapper cells, there is zero area and performance impact. But we see that the test and functional outputs are common which will limit the insulation of dies in pre-bond test phase.

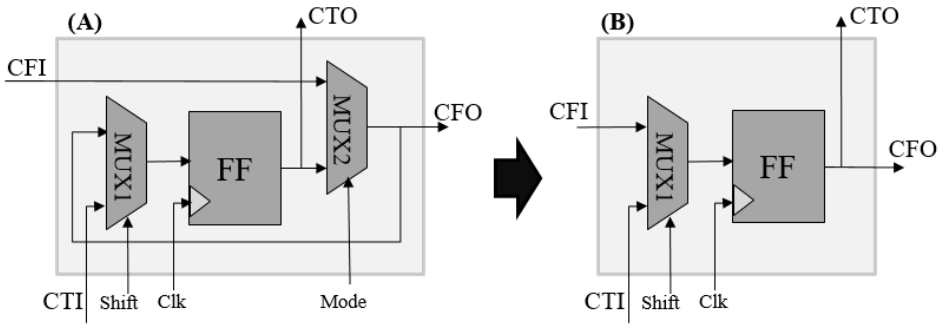


Figure 52: Dedicated (a) and (b) shared wrapper cell

The shared wrapper cells prevents simultaneous functional and test operation uses of the shared register. In the next part, an optimized DFT architecture based on shared wrapper cells was proposed to make pre-bond and post-bond test for high-density SRAM-on-Logic 3D-IC. The proposal is in line with the ongoing IEEE P1838 standard while keeping an optimal test coverage.

2. Optimized DFT architecture for SRAM/Logic 3D-IC

In this section, we propose within the framework of smart imager, an optimized 3D-DFT architecture for SRAM/Logic 3D-IC using F2B stacking mode and W2W stacking orientation, 28 nm FDSOI technology, a pitch of 4µm and a TSV diameter of 1µm. The main idea of the proposed test method is using an optimized test infrastructure of pre-bond testing to simultaneously test dies and high-density 3D-IC interconnects in post-bond test, the test methodology being able to test interconnects between memory and logic dies by performing write and read operations from the logic die to the memory die.

The proposed architecture is based on IEEE 1838 test standard; the primary interfaces are implemented at the bottom-side of each die and the secondary interfaces are implemented at the top-side of each die, the logic die contains all external I/Os as its primary interface and the secondary interface of the logic die is connected to the primary interface of the memory die. The serial control mechanism, equipped with an IEEE 1149.1 Test Access Port (TAP), including four input terminals TDI (Test Data Input), TCK (Test Clock), TMS (Test Mode Select), and TRSTN (Test Reset), and the output terminal TDO (Test Data Output). This interface allows to transport instructions, configuration data and test stimuli as well as test responses.

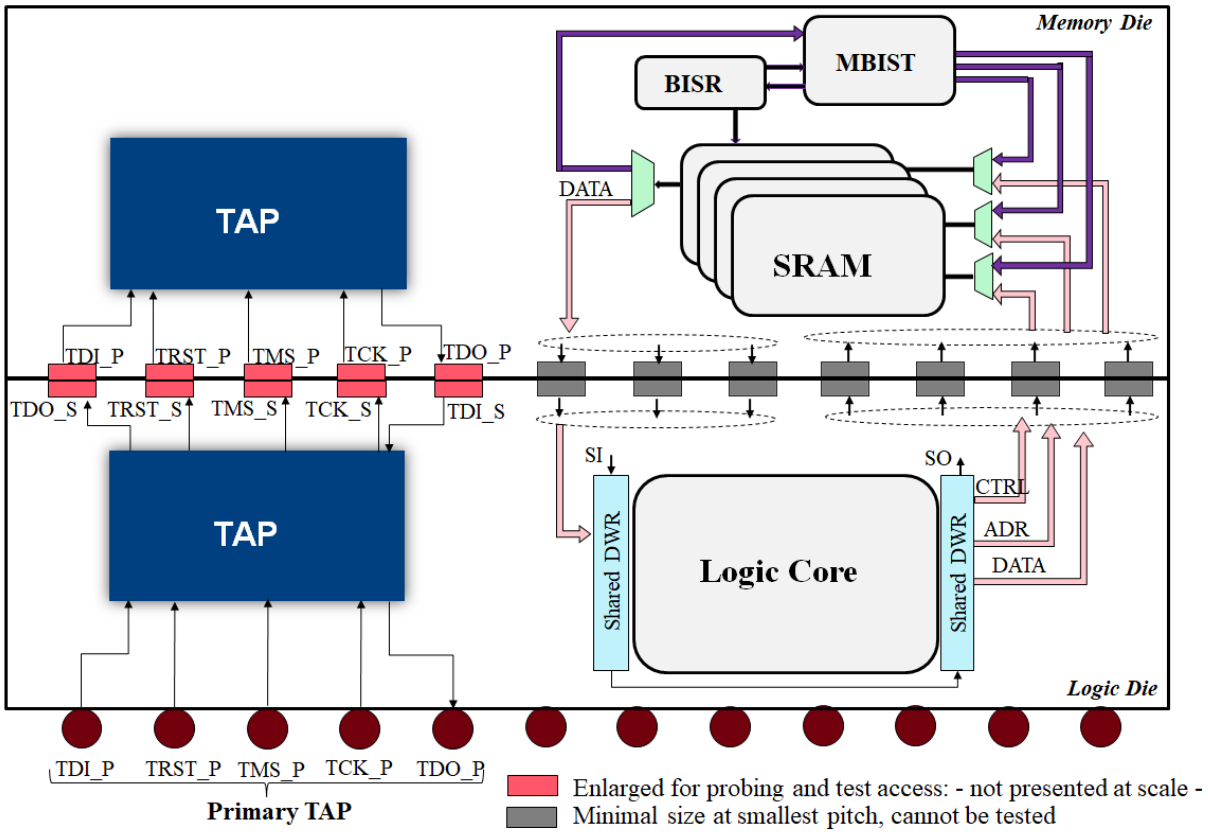


Figure 53: Optimized DFT architecture for SRAM/Logic 3D-IC

Figure 53 shows the architecture of the optimized 3D-DFT architecture. The MBIST/BISR and shared DWR, accessible via the TAP I/O (Cu-Cu pads with a red outline), are essential for a complete pre-bond test of the memory and logic dies. For area constraints, we suppose that SRAMs are without scan chains. The test of functional 3D interconnects (I/O between logic and memory dies: control, address and data signals), in post-bond test, is done using write and read operations; the first step is to write in the memory, the test sequence (Control signals, address and data input) is shifted through the shared DWR cells, then applied to the memory across the 3D-IC interconnects using the green multiplexer in memory die that must be in functional mode. The second step consist to read the previously written sequence, therefore in the same way (using shared DWR cells) the control and address signals are applied and the output data is shifted out. The last step is to compare the output data to the input data. Data signals can be controlled and observed directly through writing and reading operations. However, address lines are unidirectional and fault detection must be performed indirectly using data signals (e.g., by writing and reading to different addresses). Control signals, such as write or read command, are tested implicitly.

Table 5 shows the test infrastructures as well as the test access ports used in pre-bond and post-bond; in pre-bond test, the secondary TAP interface of the Logic die, and the primary interface of the Memory die are used. But after bonding, only the primary TAP

interface of the Logic die is used to test Logic die, Memory die and 3D interconnects.

	Pre-bond test		**Post-bond test**	
	Test access	**Test Features**	**Test access**	**Test Features**
Logic Die	Primary TAP	Shared DWR cells	Primary TAP	Shared DWR cells to re-test logic core
Memory Die	Secondary TAP	MBIST & BISR	Primary TAP	MBIST & BISR to re-test SRAMs
3D Interconnects	No test	No test	Primary TAP	Shared DWR cells

Table 5: Test methodologies

IV. Discussion

The test time in such 3D-IC architecture is a real issue, using only a serial port would require millions of clock cycles only to shift in one test pattern, leading to significantly longer test times. Therefore, using a FPP that can transport multiple stimulus and response bits simultaneously must be used to reduce the test time. Furthermore, as it's mentioned in chapter 1, the probing process in pre-bond test can damage the specific probing TAP pads, causes particles at surface level and impact the bonding process. So, a dedicated damage-less probing card is needed.

Concerning DFT insertion, the IEEE P1838 not yet approved and supported by test tools. In the other hand, the test pattern generation become harder using the proposed architecture because of passing from test to functional and conversely running the test. So, a conventional test pattern generation for such circuit must be integrated to the test tools. To sum up, the proposed DFT architecture is a future perception for high-bandwidth and high-density Memory-on-Logic 3D-IC, requires development of the IEEE P1838 test standard, probing and test tools.

We verified our optimized 3D DFT architecture, destined for high density 3D-IC applications, on a processor sub-system design in FDSOI 28nm technology, F2B stacking mode using 3D-High Density interconnects (pitch of Cu-Cu interconnects and TSVs=4µm) and a TSV diameter of 1µm. The design contains a RISC-V core with 4 memory instances (SRAMs 8K), which are respectively placed on the bottom and top layers of the 3D circuit. Figure 54 shows the floorplan of the SRAM-on-Logic physical design that is performed as proposed in [70]. The proposed 3D-DFT architecture has been partly implemented, including the TAP controller in each die, a shared core wrapper around the CPU core logic on bottom layer and an MBIST/BISR on top layer. The shared wrapper cells has been inserted using Synopsys® tools, while the MBIST and the BISR have been inserted using the commercial Mentor Tessent® tools for

Design-for-Test, logic insertion and test pattern generation. The proof of concept of the optimized test architecture were successfully verified thanks to gate-level simulation.

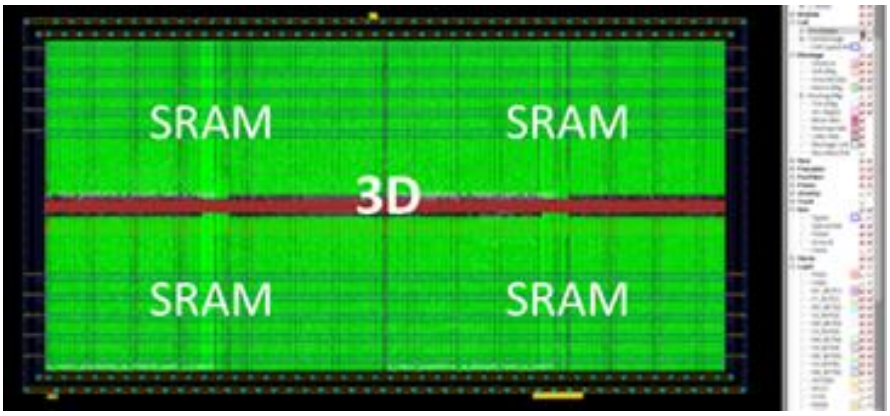


Figure 54: 3D SRAM-on-Logic RISC-V floorplan

V. Conclusion

High-density 3D-IC pose new challenges in terms of inter-die interconnect test. At first, we have shown the test concepts as well as the most optimized BSC depending on used DFT standard (IEEE 1149.1, IEEE 1500 or the ongoing 3D test standard IEEE P1838). Then we have studied the testability of high density 3D-IC interconnects on different stacking modes (F2F and F2B); we have shown that the size of TSV's and the KOZ can significantly reduce the area available for functional and test cells. Afterwards, an optimized 3D-DFT architecture based on shared DWR and IEEE P1838, for high-density SRAM/Logic 3D-IC, has been developed; the high-density interconnects are tested through memory read and write operations. The strengths and weaknesses of the proposed method have been discussed, this test approach reduces the area overhead as well as the propagation delay of the critical timing path. The proposed 3D-DFT architecture will be implemented in a future 3D imager.

For such DFT architecture, only function test is employed to detect static defects (i.e. short and open defects). However, 3D-IC interconnects might also be affected by misalignment and µ-void defect that manifest themselves as delay faults and impact performance of 3D-ICs. In the other hand, when we cannot insert wrapper cells within the aggressive pitch, the test of 3D-IC interconnects become unachievable. Hence the extension of the 3D-DfT architecture and the association of test structures to detect 3D-IC defect is necessary. The next chapters will be focusing on the implementation of the test structures in the 3D-DFT architecture for structural test of 3D-IC interconnects; detect misalignment and µ-void defect and assess performance of high-density 3D-ICs.

Chapter IV. Structural test of high density 3D-IC interconnects

We have seen previously that the separation between misalignment and µ-void defects presents a real challenge because of its similar effect on electrical characteristics. Moreover, concerning the misalignment test structure (proposed in Chapter 3), we show that the area of test pads is very large compared to that of the patterns. We show also in chapter 4 that if the used pitch is below the minimum pitch we cannot use BSC to test 3D-IC interconnect. Taking into account all this constraints, we can say that the same test structures used for characterization must be used in conjunction with more usual 3D DFT architecture for performance analysis of 3D-ICs and to perform functional and structural test of high-density 3D functional interfaces.

In this chapter, we propose two complementary BISTs to test and characterize high density 3D-IC interconnects. The first BIST allows to measure the misalignment defect with a great accuracy and the second measure the RC delay of a periodic signal applied to a daisy chain composed of Cu-Cu interconnects. The measured misalignment values and propagation delays allows to detect Cu-Cu full open, misalignment, and micro-voids, in order to assess performance of high density 3D Integrated Circuit. The two proposed BISTs are integrated and controlled with IEEE 1687, for an overall negligible area cost.

I. Related works

The structural test of Cu-Cu interconnect was not discussed in the state of the art, but many test solutions have been proposed in the literature for structural test of 3D-IC interconnects to detect small delay faults; resistive open/bridging faults, leakage faults, etc. The majority of these solutions are focused on TSVs test to reduce the overall test time and cost and to replace direct TSV probing such as MEMS probe and contactless probes because TSVs are fragile and any physical contact for the purpose of testing can affect their physical integrity.

Among the structural test solutions to cover TSV parametric faults reported in the literature we find a delay measurement method (Figure 55), is proposed in [71], [72] and [73] to determine the delay variations caused by TSV open resistive defects. In this

method a reference voltage is applied to the TSV under test and the output is compared with a reference response to determine pass/fail results.

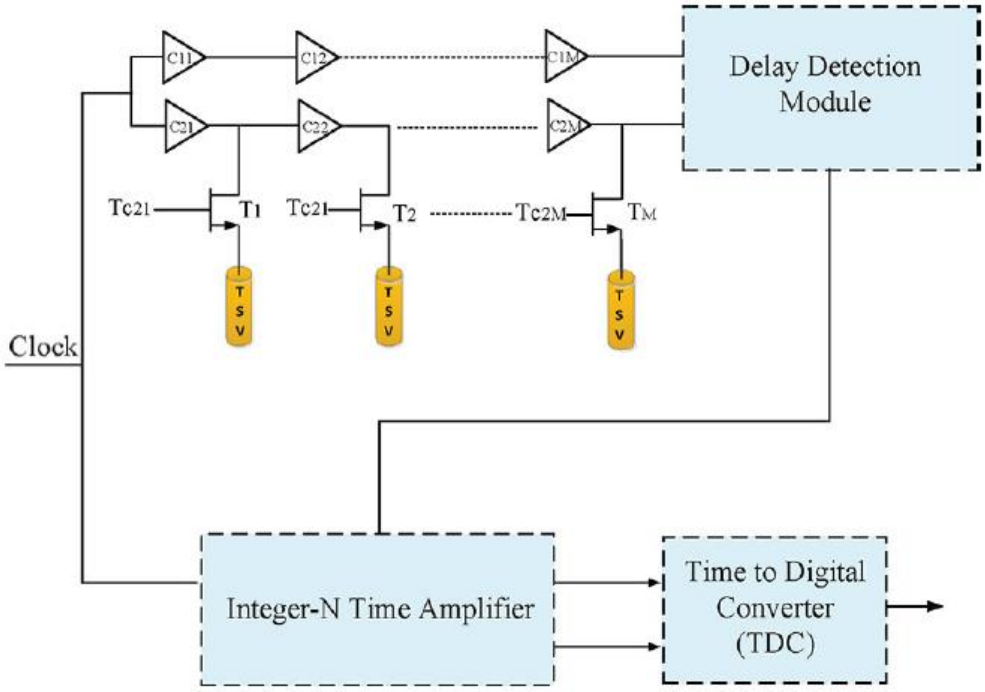


Figure 55: Example of delay measurement method (source [71])

Another alternative using ring oscillators (Figure 56) is also proposed to detect TSV defects [74], [75] ; the frequencies of the ring oscillator depend on the delay time of the closed inverter loop and the capacitances of series connected TSVs in the loop. The TSV defects are detected from the difference between frequencies of two ring oscillators which is the image of the capacitance effect.

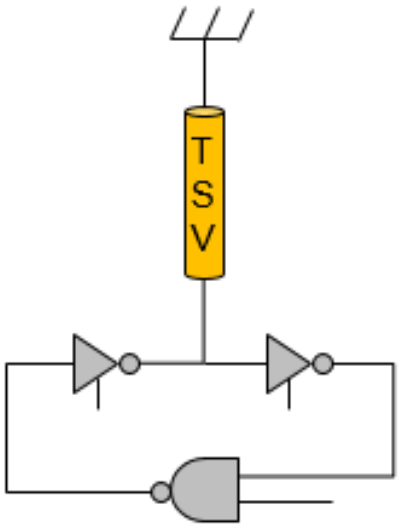


Figure 56: Test TSV using ring oscillator example

Ring oscillators are widely used on semiconductor production to monitor the gate delay and speed-power of products. In 3D context, many Built-In-Self-Test (BIST) architecture based on 3D ring oscillator for pre-bond testing multi-layer 3-D stacked integrated circuits with TSV are proposed in [76] and [77]. The impact of defects on TSV and Cu-Cu interconnect parameters has been shown previously; we observe that, for TSVs, the impact of defects on electrical parameters is mostly capacitive. Contrariwise, for Cu-Cu interconnects the electrical impact is mostly resistive and it's difficult to separate defects. For this reason, the ring-oscillator test method is not effective for structural test of Cu-Cu interconnects. In the next part, we show a structural test strategy for Cu-Cu hybrid-bonding interconnects. The proposed method is based on the use of the same test structure used in process development and implement them in an application circuit to measure misalignment defects and detect µ-void defects.

II. Proposed BIST's to test and characterize high-density 3D-IC interconnects

1. Overview

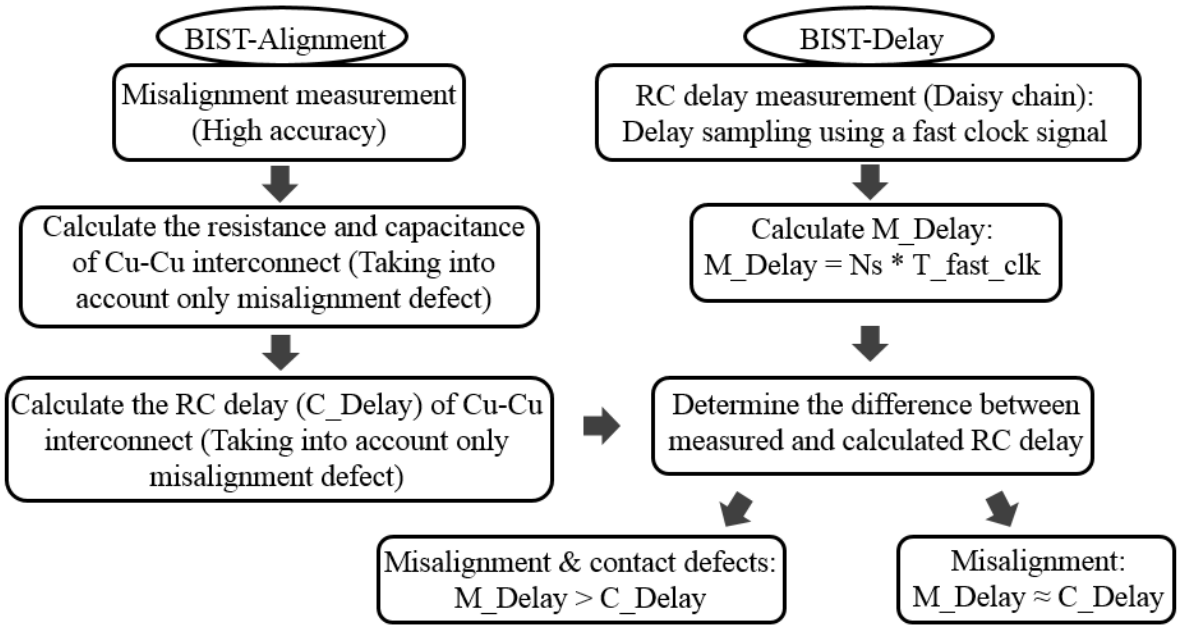


Figure 57: Proposed structural test flow for Cu-Cu interconnects

Figure 57 shows the suggested test flow; the proposal is to test misalignment defect (BIST-Alignment) before RC delay measurement in the daisy chain (BIST-Delay) so that we can conclude on the impact of misalignment on delay. BIST-Alignment measures the misalignment with high accuracy using the proposed misalignment test structure (proposed in chapter 2). Resistance and parasitic capacity are calculated before computing the obtained RC delay. For the BIST-Delay, a periodic signal is applied to the daisy chain of Cu-Cu interconnects under test and the propagation delay is measured.

The comparison between calculated (C_delay) and measured (M_delay) delay makes it possible to have two cases; the first is when C_delay ≈ M_delay, in this case we can study the impact of misalignment on propagation delay and characterize Cu-Cu interconnects. But if M_delay > C_delay, then we can validate the presence of contact defects.

2. BIST alignment

The idea behind the BIST is to facilitate, in one hand, the insertion of the misalignment test structure into the application and in the other hand to minimize the cost by elimination of test pads because it occupies a very large area compared to that of the patterns. Using a BIST to manage the test offers a possibility to use many test patterns for high accuracy misalignment measurements. The choice of test patterns number as well as offset values will be based on stacking options (W2W, D2W), the level of required precision, and the precision of bonding equipment's.

Figure 58 shows the BIST-Alignment architecture. It is composed of a passive part (N patterns) and the BIST to control the test. To reduce pin counts, all patterns share a single "In" signal, and exhibit N parallel X+, X-, Y+, Y- signals, that can be additionally forced by extra input signals for verification purpose. The BIST is composed of a Finite State Machine (FSM) to order the test using different state (start_test, Load_reg, shift_reg and end_test). The test runs if start_test = '1'; the input signal of test patterns "In" is forced to '1', then the register loads the selected input (X+, X-, Y+ and Y-) and shifts it in order to count the number of '1' and to detect a possible discontinuity of the data sequence (i.e. "111010…"), the number of counter and register stage is equal to test pattern number. Finally, the "result generator" provides test results and detects bonding error (i.e. if "X+(0) X-(0) Y+(0) Y-(0)" = "1110" since we have more than two contacts for a given pattern (P(0)). The End_test signal indicates the end of the test. In order to test the BIST itself, a multiplexer has been added to separate between functional mode (using X+, X-, Y+ and Y- of misalignment test structure) and external test inputs.

Contact_NB	Misalignment direction
000	X+
001	X-
010	Y+
011	Y-
100	X+Y+
101	X-Y+
110	X-Y-
111	X+Y-

Table 6: Contact_NB output interpretation

The output signals are interpreted with this order of priority: if Err_Discontinuity ='1' and/or Err_Contact ='1' so we do not consider the other output values because we detect a discontinuity and/or contact error in misalignment test structure results. Else, if the alignment is perfect Test_align ='0' in contrary, Test_align='1', in this case we focus on contact_NB that is the BIST output to encode misalignment direction (see Table 6) and X Y values that present misalignment values.

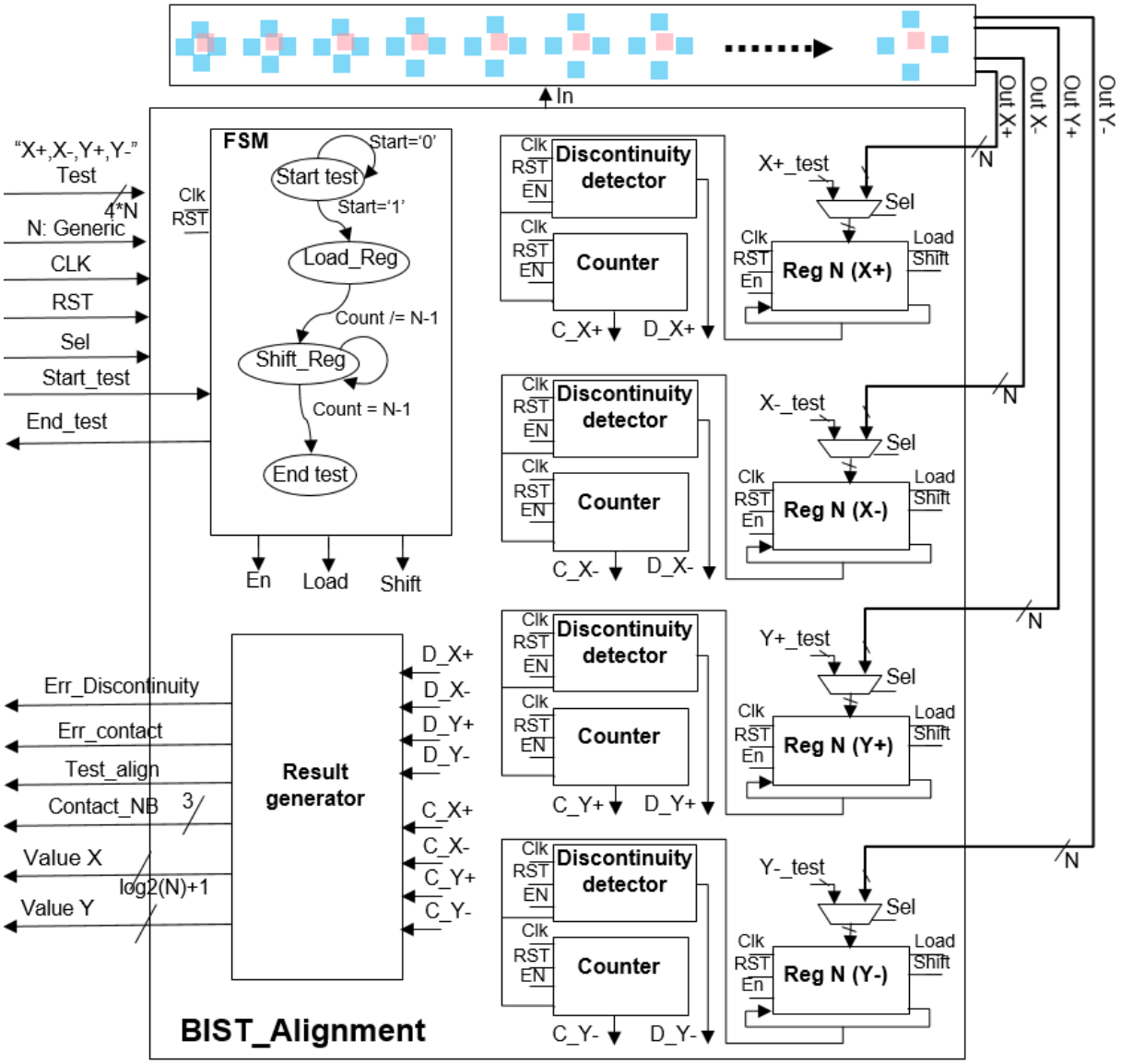


Figure 58: Proposed structural test flow for Cu-Cu interconnects

Taking into account a possible discontinuity and bonding errors due to a manufacturing defects in the structure itself, this architecture allows to test misalignment defect and measures accurately the values of misalignment in X and Y direction. To complete the flow proposed at the beginning of this section, we detail below the BIST-Delay architecture to characterize high-density 3D-IC interconnects, quantify the impact of misalignment defect and detect µ-void defects.

3. BIST delay

The daisy chain test structure (Figure 59) is widely used to solve process issues linked to the fabrication flow and for characterization. The electrical tests are carried out using four wires to measure the contribution of the resistance of the daisy chain, the value of the measured resistance includes not only the resistance of the Cu-Cu vertical contact, but also the resistance of the horizontal metal lines. In our work, a daisy chain is used, in a different way: a periodic signal is applied to the daisy chain under test to estimate the propagation delay. To achieve high resolution, the daisy chain should have large number of interconnects (in order of 10,000 interconnects) because the RC parameters of a single Cu-Cu interconnects are very small.

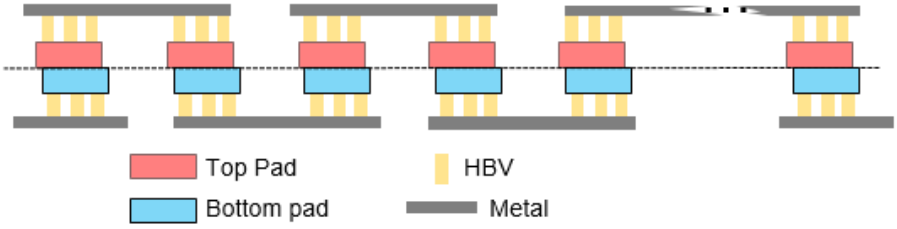


Figure 59: Daisy chain

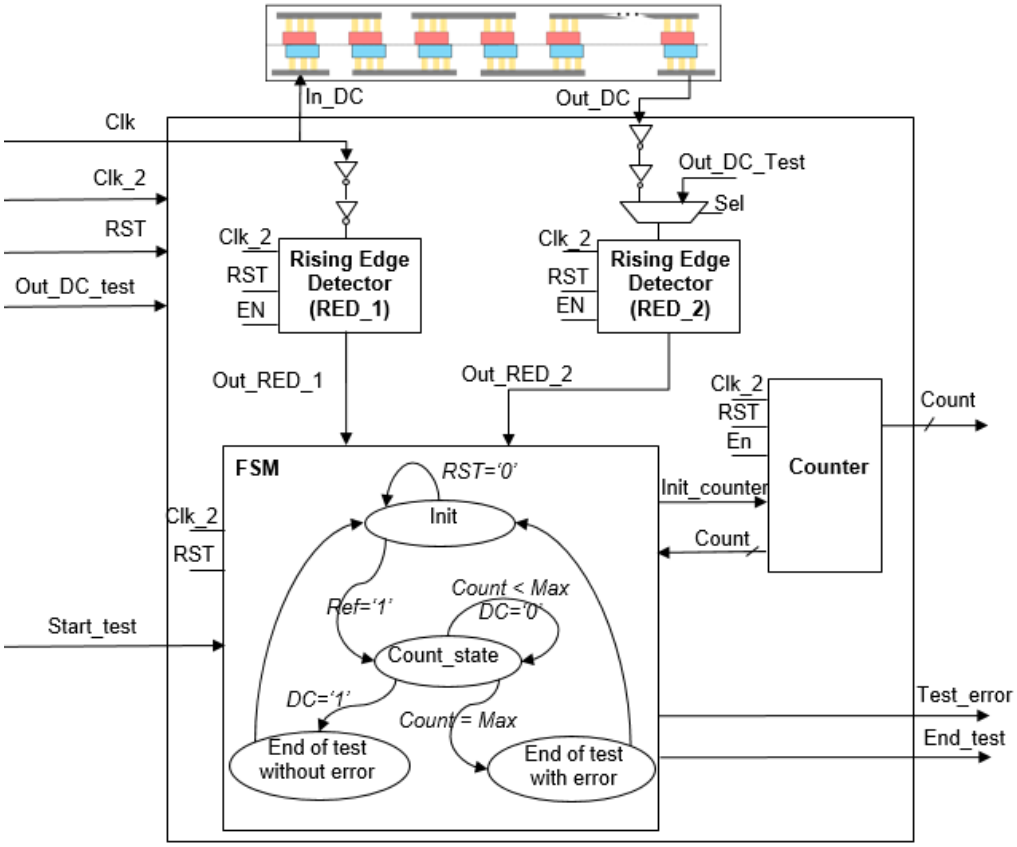


Figure 60: BIST delay architecture

Figure 60 shows the architecture of BIST-Delay, a periodic signal (Clk) is injected through the daisy chain, the propagation delay between the reference signal (In_DC) and the daisy chain output (DC_out) is sampled using a very fast clock (Clk_2). Then, from the signature "Count", we can determine the RC delay of the daisy chain.

The BIST-Delay is also able to detect a full open defect (discontinuity of the daisy chain); Test_error =1. The Finite State Machine (FSM) controls the counter. If "start_test ='1', the multiplexer chooses between the daisy chain output and user-defined input set from outside. The rising edge of the reference signal and the output signal of daisy chain are detected using respectively "RED 1" and "RED 2". If "out_RED_1"= '1', the counting starts until the detection of a rising edge of "Out_DC" (out_RED_2 ='1') or the counter reaches its maximum (Count =Max).

The two BISTs proposed previously allow to test and characterize Cu-Cu interconnects, the first one (BIST-Alignment) measures misalignment defects with a great accuracy and the second one (BIST-Delay) calculates the RC delay in a daisy chain composed of Cu-Cu interconnects. The two proposed BISTs will be implemented in INTACT demonstrator (see Chapter 1). In the next part, the integration in the design-for-test architecture is explained. Moreover the test results of the two BISTs will be correlated to detect µ-void defects.

III. IJTAG architecture

For Design-For-Test system level integration, the two proposed BIST engines: BIST-Alignment and BIST-Delay, are integrated and controlled with a JTAG interface (Figure 61). The standard interface specified by IEEE 1149.1 is applied, using the standard Test Access Port (TAP), and associated TDI, TDO, TMS, TCK, TRST signals.

Moreover, in order to provide easy DFT system level integration, the BIST engines are integrated using the IEEE 1687 Internal Joint test Action Group (IJTAG) standard. This offers the possibility of 3D test pattern retargeting, by easily generate test patterns from pre-bond test to post-bond test.

Essentially, the design for test infrastructure allows to connect the instruments to the boundary scan TAP controller. The example network consists in two instruments (BIST alignment and BIST delay) and in two Segment Insertion Bits (SIB) used to dynamically configure an on-chip IEEE 1687 IJTAG scan path. The instruments are interfaced with the scan path via Test Data Registers (TDRs) with parallel I/O. The IEEE 1687 standard introduces two high level languages: Instrument Connectivity Language (ICL) which describes the instruments port functions and logical connection to other instruments and to the IJTAG TAP and Procedural Description Language (PDL) which describes how an instrument should be operated.

Using an IJTAG specification, we create the IJTAG network (connect existing instruments and insert SIBs, TDRs, TAP controller) and extract the ICL description of the IJTAG network. The required test patterns are generated using PDL; the BISTs are stimulated with the command "iWrite". Then, using the "iApply" command, these stimulations are applied to the primary inputs and finally the "iRead" command allow to specify expected response and retrieve the test results of BISTs that are defined in the ICL description and compare them. The chip-level PDL commands can be translated to ATE (Automatic Test Equipment) pattern formats (STIL, WGL ...) useful as test vectors to be applied to the top level TAP or for simulation test benches that verify the ICL of the BISTs descriptions.

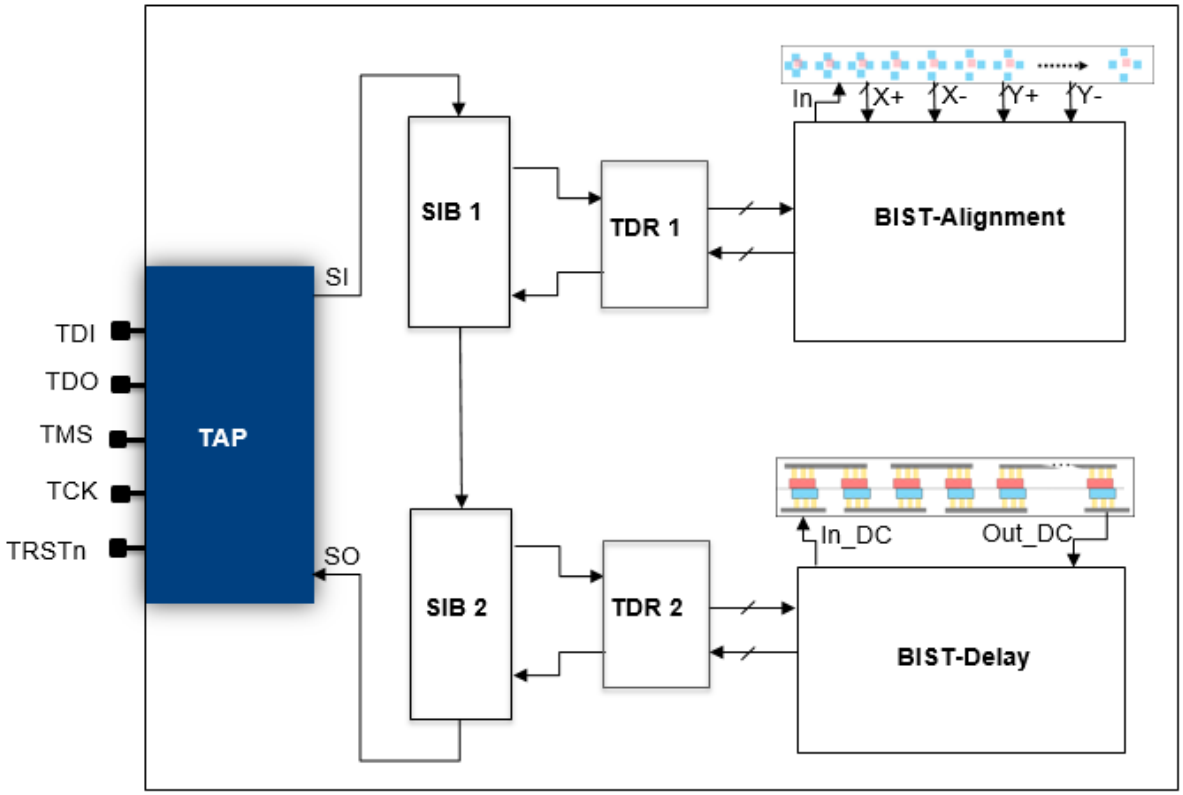


Figure 61: BIST's architecture integration within IJTAG infrastructure

The two BISTs, integrated within the IJTAG IEEE 1687 standard, allow to test and measure misalignment defect with a high accuracy (BIST-Alignment) and measure the propagation delay of a periodic signal in a daisy chain of Cu-Cu interconnects (BIST-delay). In the next part, the test results are explained to study in one hand the impact of misalignment defect on the propagation delay and on the other hand to detect full open and µ-voids defects.

IV. Simulation results

1. Electrical results

To verify the proposed test methods, the equivalent electrical model of Cu-Cu interconnect (introduced in chapter 2) is described using spice level simulations with three pitches (7.6, 3.45 and 1.4 µm). For this simulation, we take into account the HBVs' RC parameters and the metal lines. We assume that defects are uniform within a given daisy chain (10,000 vertical interconnects). The effect of temperature variation on the simulation results is negligible; i.e. for a pitch of 3.45 µm (fault free) the propagation delay = 0.349 ns and changes by 3 ps when the temperature changes from -50° to +50°.

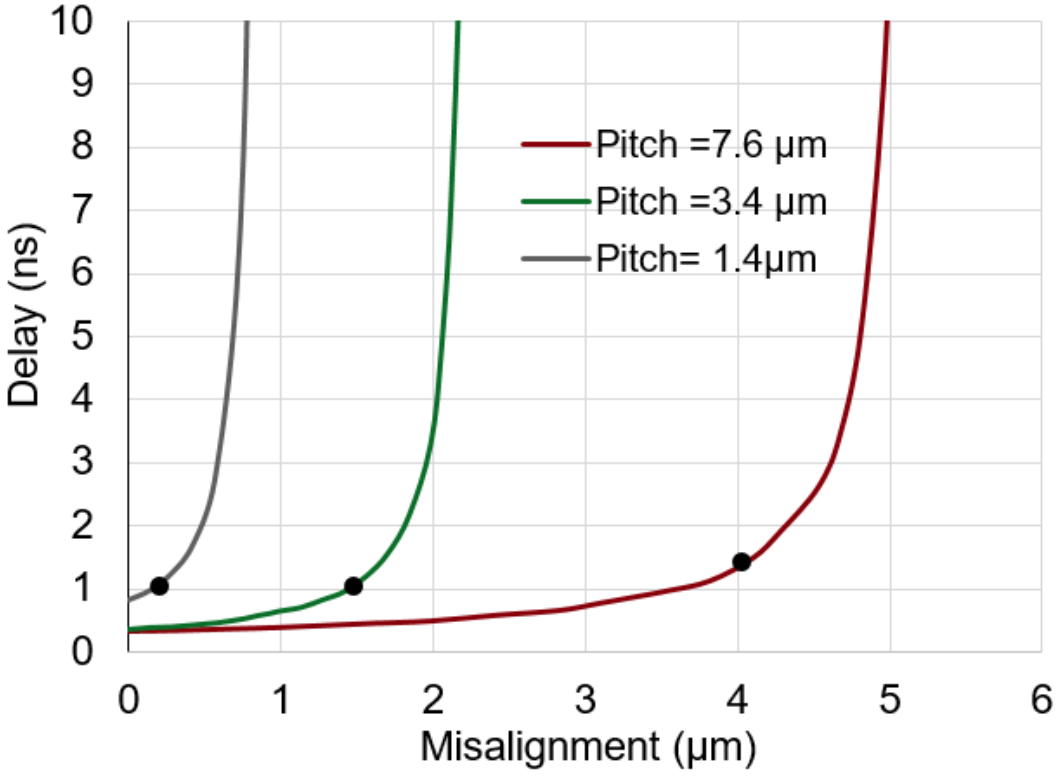


Figure 62: Delay variation of a daisy chain (10,000 Cu-Cu pads) (pitch: 7.6, 3.45 and 1.4 µm) as a function of the misalignment

Figure 62 shows the misalignment effect on the delay value, the misalignment is diagonal (X=Y). The delay depends essentially on the effective contact surface between top and bottom Cu-pads and the distance between two adjacent pads. In addition, we observe that the delay becomes very important when the slope of the tangent is less to 1 (µm/ns) (black dots); that corresponds to a misalignment equal to 76% for the pitch of 7.6 µm, 58% for the pitch of 3.45 µm and 15 % for the pitch of 1.4 µm. So, small pitch pads are clearly more sensitive to misalignment defects.

The effect of µ-void volume on daisy chain delay variation has also been investigated (Figure 63). For this simulations, we considered that $h \approx L/1000$. The highest values of

delay are obtained when the surface of a µ-void becomes comparable to the size of Cu-Cu pad under test; the delay of the daisy chain increases because of the reduction in the contact surface area between top and bottom pad. On the other side, the impact of coupling capacitance Cc on daisy chain propagation delay is negligible. Therefore, we cannot detect the small µ-void defects.

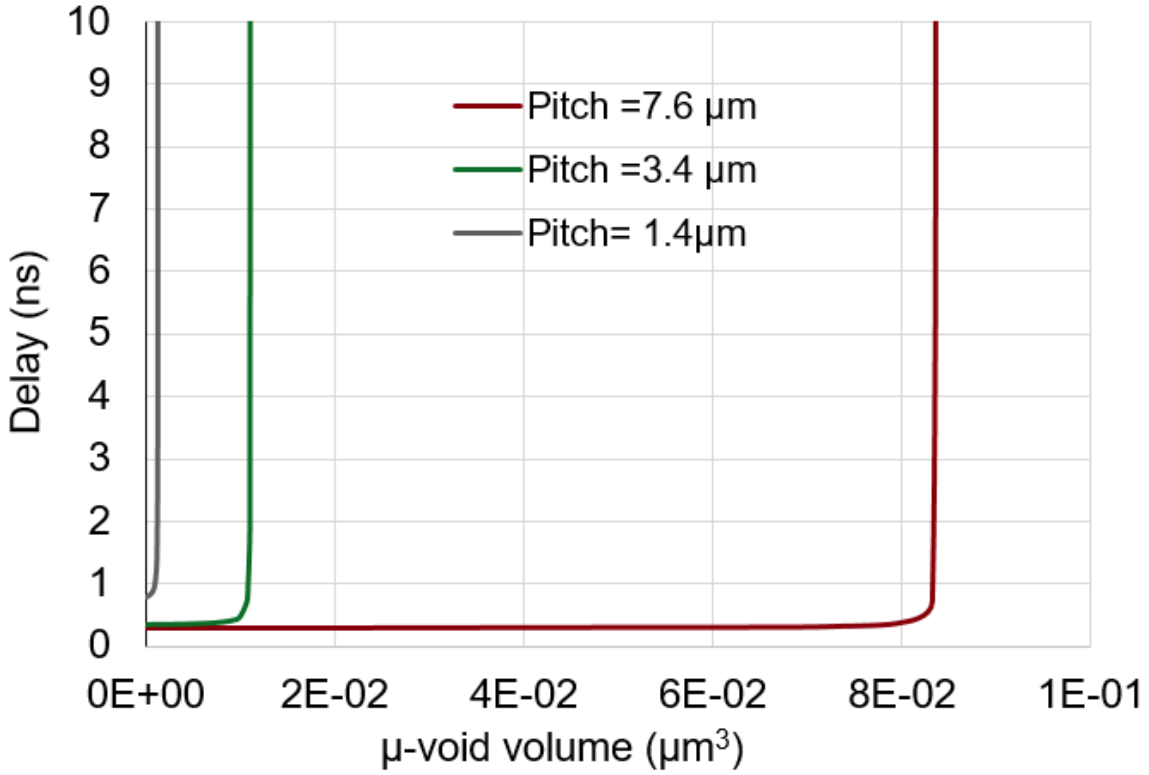


Figure 63: Delay variation of a daisy chain (10,000 Cu-Cu pads) (pitch: 7.6, 3.45 and 1.4 µm) as a function of µ-void volume

Figure 64 shows the simulation results; the input signal applied to the equivalent model of 10,000 interconnects daisy chain and the outputs signals in the case of fault free, misalignment, µ-voids defect and overlay of both defects. In this simulation, a pitch of 3.45 µm (pad size= 1.725 µm) is used with a misalignment of 1.84 (X = Y ≈ 1.3 µm) and a µ-void volume equal to 3.84e-4 µm3 (surface =0.16 µm²; h= 2.4 nm).The propagation delay (ΔT), measured at 0.6V, of the daisy chain (fault free) is around 0.349 ns. In the case of µ-void or misalignment defects, the delay is respectively equal to 0.350 ns and 2.182 ns, and in the case of defects overlay, the delay is ≈ 7.582 ns.

According to the simulations results, we observe that despite the large number of interconnects in the daisy chain, µ-voids are exceptionally difficult to cover. This is due to the fact that small voids do not affect the electrical performance of Cu-Cu interconnect considerably. But in the case of combination of µ-void (volume= 3.84e-4 µm3) and misalignment defect (1.84 µm), we can easily extract the propagation delay (ΔT). We observe that the propagation delay resulting from the overlay of the two defects (ΔT "µ-

void & misalignment") is higher than the sum of the delay of each defect separately (ΔT "µ-void" + ΔT "Misalignment") and that's due to the Effective Contact Surface (ECS); i.e. for the pitch of 3.45 the ECS (fault free) = 1.725^2= 2.89 µm², if we have a misalignment defect of 1.84µm the ECS becomes equal to 0.18µm² but in the case of combination of misalignment and µ-void defect (surface µ-void = 0.16µm²) the ECS ≈0.02 µm². The implementation we made contains a BIST-Alignment module including 18 patterns to measure misalignment in the range from 0 to 1.7 µm with a step of 0.1 µm.

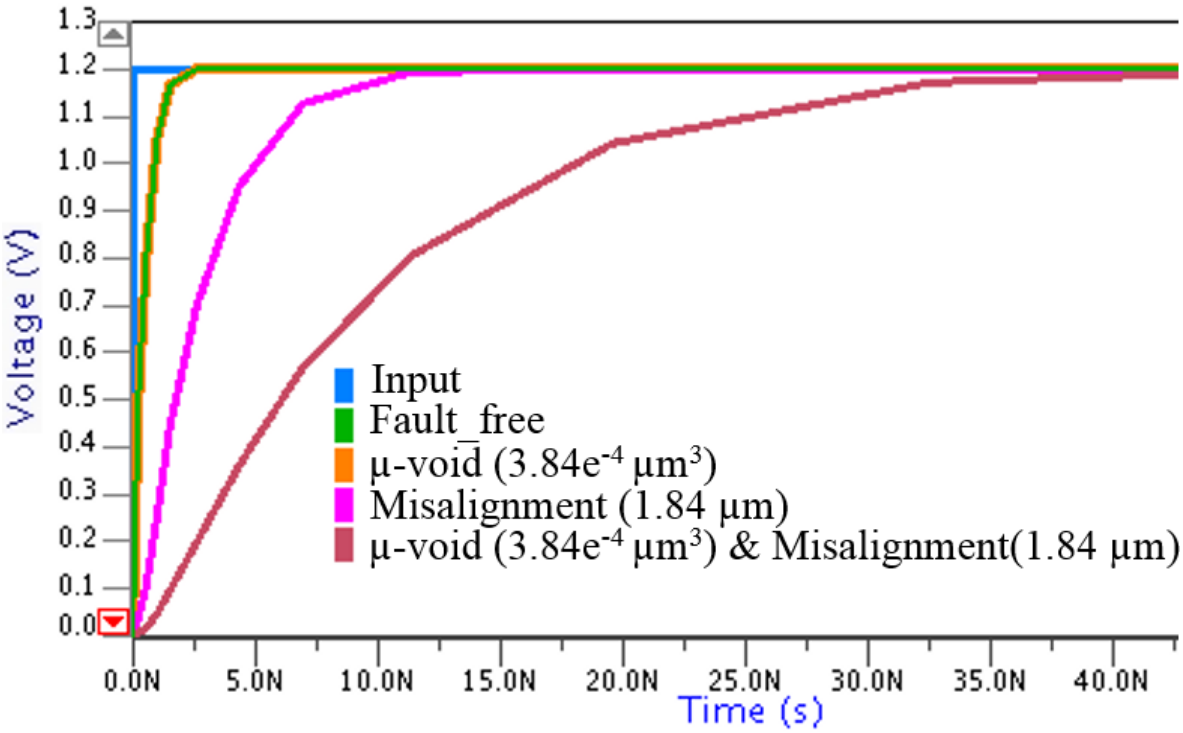


Figure 64: Simulation of the electrical equivalent model of daisy chain (10,000 Cu-Cu pads; pitch=3.45 µm)

Concerning the BIST-delay module, we measure the propagation delay (ΔT) in a 10,000 interconnects daisy chain using a very fast clock (Clk_2= 1 GHz) to achieve a resolution of 1 ns. Finally, comparing the estimated delay and the measured delay (ΔT), the µ-void defect can be detected. The BIST-delay allows also to detect full open defects caused by surface problems. BISTs can be integrated in bottom or top die depending on DFT system integration constraints.

2. System integration

A proof of concept of the test architecture was first completed thanks to VHDL simulation using a test signals: "X+X-Y+Y- test" (BIST alignment) and "Out_DC_test" (BIST delay) and mixed simulation using the equivalent electrical model of Cu-Cu interconnects.

Test structures	Area (µm²)	Area (%)
Passive part:	61,370	100%
Alignment patterns	1,870	3%
Daisy chain	59,500	97%
Active logic part:	28,600	100%
BIST alignment	12,880	45%
BIST delay	9,020	32%
IJTAG infrastructure	6,700	23%

Table 7: Area of the proposed test architecture (pitch= 3.4µm)

The design of BISTs was conducted according to the design flow shown in Figure 65. The proposed IJTAG architecture has been fully inserted using the commercial Mentor Graphics Tessent® product suite for Design-for-Test, logic insertion and test pattern generation. The proposed architecture was implemented using a FDSOI 28 nm standard cell libraries for Wafer-to-Wafer stacking with a pitch of 3.45 µm. The area of the passive and active parts are presented in Table 7. The dummies, added to guarantee an overall uniformity at wafer level and make easier planarization before bonding, are used to implement the passive part. The passive part overlaps the active logic part, the global area overhead is therefore negligible (≈ 0.3% for a 10 mm² circuit).

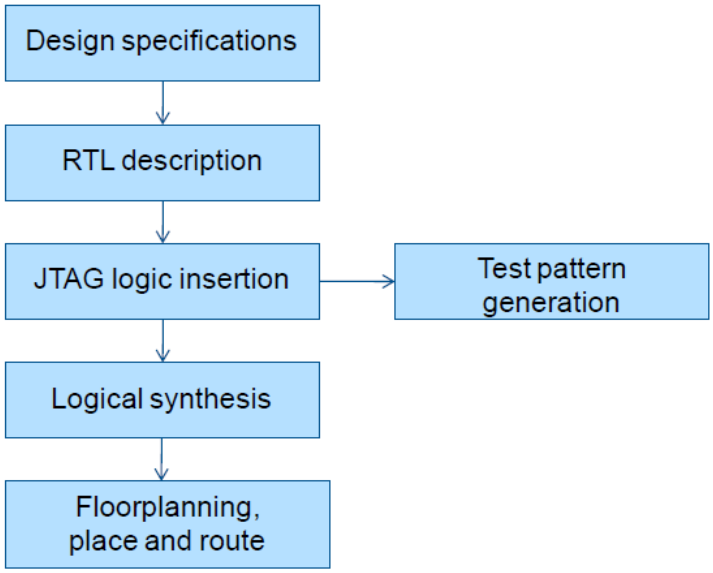


Figure 65: Design flow of the test chip circuit

V. Conclusion

In this chapter, a new approach to test high density Cu-Cu interconnects has been developed to perform functional and structural test of 3D functional interfaces. The two complementary BISTs integrated within the IJTAG IEEE 1687 standard allow to test and

measure misalignment defect with a high accuracy (BIST-Alignment) and measure the propagation delay of a periodic signal in a daisy chain of Cu-Cu interconnects (BIST-delay). Using test results, we can determine, on one hand, the impact of misalignment defect on the propagation delay and on the other hand we can detect full open and µ-voids defects at the contact surface level. Experiment results and analysis have been presented to validate the proposed test methodology, architecture, and structure circuits.

Chapter V.Conclusion and perspectives

High density 3D-IC poses new challenges in terms of test and characterization. In this thesis we presented 3 contributions for the definition of test strategies dedicated to high-density 3D-ICs.

The first contribution concerns the test of misalignment defect after bonding. Based on basic reference pattern composed by a top Cu-pad and four Bottom Cu-pads, the proposed misalignment test structure allows to measure accurately bonding misalignment (the accuracy depends on offset values "the spacing between bottom pads"). The proposed approach allows also to have additional information such as direction of misalignment and estimate the contact resistance of Cu-Cu interconnects. The technological test vehicle (passive version) was designed in short loop circuit for process development and implemented for W2W stacking with a pitch of 3.42µm and 1.44µm using a very small measurement step for an accurate misalignment measurement (respectively 45nm and 22nm). The area of this test vehicle is around 236,380 µm² (patterns + test pads). Electrical tests have been performed using five multi-pitch wafers with 71 measurements points per wafer. The experimental results show that the results of the proposed test structure are aligned with conventional overlay measurements. The impact of misalignment defect on electrical parameters of Cu-Cu interconnects has been also studied, the simulations show that high density 3D-IC interconnects are very sensitive to misalignment defect. So it is very interesting to use the same low cost test structure, with several test patterns to increase the accuracy of misalignment measurements, in conjunction with more usual 3D Design-For-Test (3D-DFT) architecture to perform functional and structural test of 3D interfaces in 3D-IC.

The second contribution concerns the testability of high-density 3D-ICs at system level. The 3D DFT architecture is essential to ensure the test of all the components of the 3D system including the different stacked dies and the 3D interconnects at all the 3D bonding levels: pre, mid and post-bond levels. Test infrastructure of HD 3D-IC presents new test challenges because of the high interconnects density and the area cost for test features. A pre-analysis of the testability of HD 3D-IC has been done to define the most optimized Design-For-Test infrastructure depending on used standard and the minimum acceptable pitch value for a given technology node to ensure the testability of high-density 3D-ICs. Afterwards, an optimized DFT architecture allowing pre-bond and post-bond for high-bandwidth and high-density 3D-IC application (SRAM-on-Logic) has been proposed. The proposed approach was partially implemented using the ongoing IEEE P1838 standard.

Finally, a new method to test high density Cu-Cu interconnects has been developed to perform functional and structural test of 3D functional interfaces. The two complementary Built-In Self-Test (BISTs) integrated within the IJTAG IEEE 1687 standard allow to test and measure misalignment defect with a high accuracy (BIST-Alignment) and measure the propagation delay of a periodic signal in a daisy chain of Cu-Cu interconnects (BIST-delay). Using test results, we can determine, on the one hand, the impact of misalignment defect on the propagation delay and on the other hand we can detect full open and μ-voids defects at the contact surface level. Experiment results and analysis have been presented to validate the proposed test methodology, architecture, and structure circuits. The perspective to this work is to propose reconfiguration and fault tolerance capabilities for high-density 3D-ICs to achieve the optimal test coverage rate.

Résumé en français

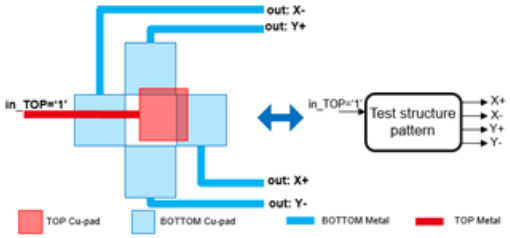
L'intégration de plusieurs puces dans un empilement 3D constitue un autre moyen d'avancer dans le domaine « More-than-Moore ». L'intégration 3D consiste à interconnecter les circuits intégrés en trois dimensions à l'aide des interconnexions inter-puces (µ-bumps ou Cu-Cu interconnexions) et les TSVs (Through Silicon Vias).

Ce passage d'une interconnexion horizontale à une interconnexion verticale est très prometteur en termes de rapidité et de performances globales (délai RC, consommation et facteur de forme). D'autre part, pour le développement technologique de l'intégration 3D avant la production des plaques (wafers) de 300 mm avec toutes les couches FEOL et BEOL, plusieurs plaques (short-loop) doivent être réalisées pour permettre la caractérisation incrémentale et le test structurel des interconnexions 3D afin d'évaluer la performances électriques (R, L, C…). D'autre part, le test des circuits d'application consiste à ajouter des fonctionnalités de testabilité (Boundary-Scan-Cells (BSC), Built-In-Self-Test (BIST) et des chaînes de scan …) pour le test fonctionnel du circuit 3D (y compris les puces empilées et les interconnexions 3D). L'architecture DFT (Design-For-Test) ajoutée facilite le développement et l'application des tests de fabrication au circuit conçu.

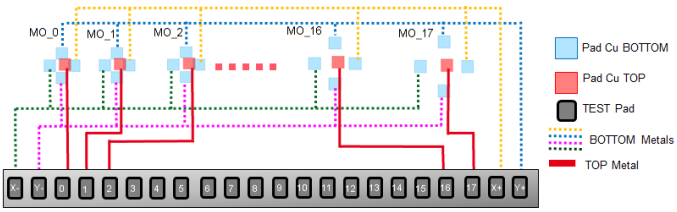
Les interconnexions 3D étant de plus en plus petites et denses, notamment en technologie collage hybride plaque à plaque, il est indispensable de les caractériser en termes de performances électriques lors du développement de la technologie, mais il est également crucial de pouvoir les tester et caractériser dans le circuit applicatif final, ceci afin de connaitre la dispersion et potentiellement tenir compte de leurs performances réelles pour les utiliser au mieux dans les communications inter circuits. Pour ce faire, le développement de véhicules de test spécifiques a été réalisé ainsi que leur intégration dans une architecture de test du type DFT (Design-For-Test) afin de permettre aux concepteurs de les intégrer facilement lors de la conception. Cette année, d'une part nous avons testé et validé le véhicule de test et d'autre part nous avons étudié la testabilité des interconnections 3D haute densité dans un circuit applicatif (test fonctionnel).

Dans un premier temps, un véhicule de mesure de désalignement a été dessiné et intégré pour qualifier la précision de collage au niveau de la plaque. La figure de gauche ci –dessous illustre le motif de base pour la mesure de désalignement : les 4 plots de cuivre sont dessinés en bleu pour la plaque « au-dessous » et le plot de la plaque « au-dessus » est en rouge ; celui-ci est parfaitement centré lorsque l'alignement est parfait, et dans ce cas il n'y a aucun contact avec les plots en rouge. Ce motif est répété N fois, et pour chacun d'eux on espace de plus en plus les 4 plots au-dessous de la position parfaite du plot au-dessus (figure de droite ci –dessous), le décalage entre 2 motifs correspond à

la précision de l'alignement que l'on va être capable de mesurer. La structure de test a été fabriquée avec un assemblage de Wafer-to-Wafer (W2W), des pas de 3,44µm et 1,44µm et une précision de mesure importante (respectivement 45 nm et 22.5 nm). Des tests électriques ont été effectués avec cinq plaques (71 mesures par plaque).

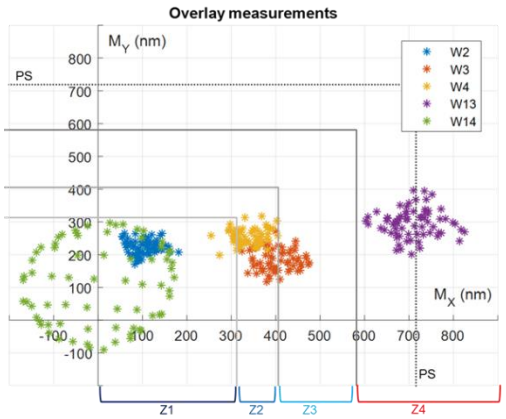


Motif pour la mesure de désalignement

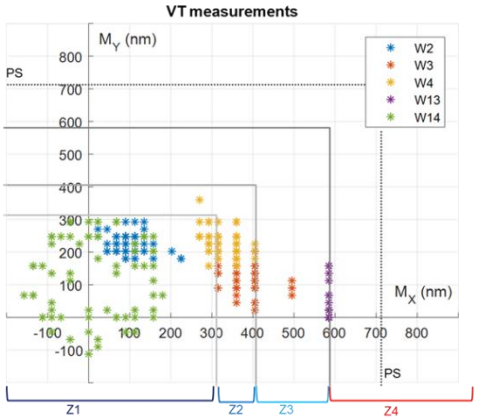


Véhicule de test du désalignement

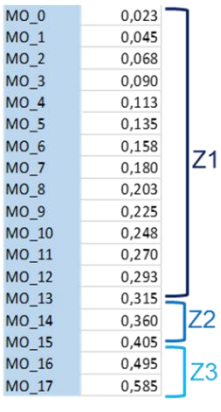
Pour valider la structure du test proposée, on va comparer les résultats du test aux mesures « d'overlay » géré par l'imagerie infrarouge (IR) à l'aide des marques d'alignement spécifiques. La valeur du décalage entre deux motifs n'est pas régulière (Voir tableau au-dessous), on peut donc distinguer quatre zones ; Z1, Z2 et Z3 correspondent à une résolution de mesure égale respectivement à 22,5 nm, 45 nm et 90 nm et pour la Z4 ou la valeur du désalignement est supérieur à la zone de couverture de la structure. Les figures ci –dessous montrent la distribution des mesures du désalignement pour les 5 wafers (W2, W3, W4, W13 et W14) à l'aide des mesures d'overlay (figure à gauche) et le véhicule de test du désalignement (figure à droite).



Distribution des mesures du désalignement (Overlay)



Distribution des mesures du désalignement (Véhicule de test)

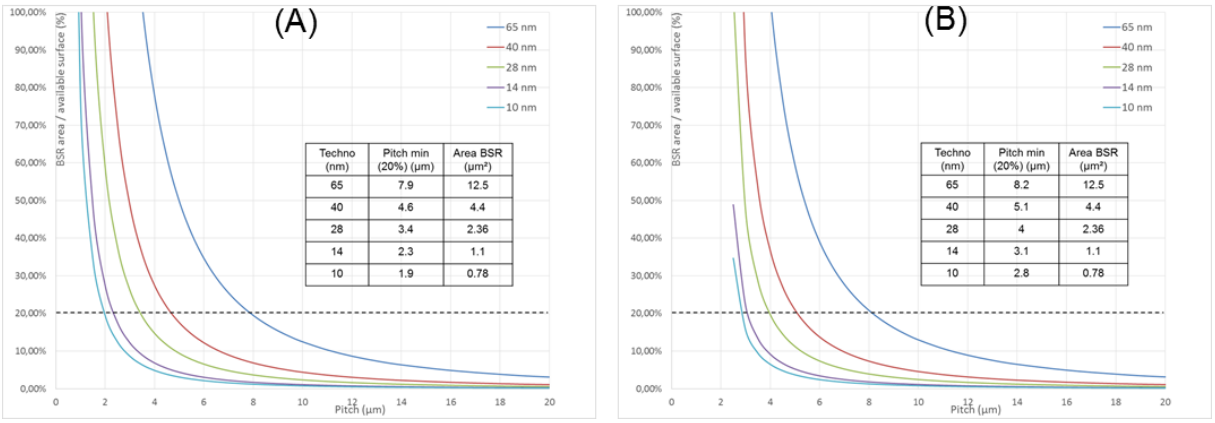


Précision du véhicule du test

Après la comparaison avec les mesures « d'overlay », nous validons la structure de test de désalignement. La précision de la mesure dépend des valeurs de décalage entre les motifs (résolution). La surface de la barrette de test est très grande par-apport à celle des motifs. Cette structure peut donc être associée à un «Built-In-Self-Test» BIST pour gérer le test. Une version active peut être utilisée dans un circuit applicatif pour tester et évaluer les performances des 3D-ICs.

Les circuits 3D doivent être testés pour garantir la fonctionnalité et la qualité des circuits. L'insertion d'une infrastructure de test dans le circuit applicatif est nécessaire pour réaliser un test de qualité. Mais ce surcoût présente toutefois des nouveaux défis en matière de test en raison de la densité d'interconnexion élevée et de la zone limitée consacré à cette infrastructure de test. Les Boundary-Scan-Regiser (BSR) placés au long des entrées/sorties permettent de tester les interconnexions 3D et d'assurer la contrôlabilité et l'observabilité du test à l'aide d'instructions de test externes (EXTEST). Pour un circuit 3D haute densité, il faut tenir compte de l'espace limité des cellules d'E/S (BSRs). Nous essayons donc, d'une part, de minimiser la surface d'un BSR et d'autre part, de proposer des solutions pour optimiser l'architecture de test. L'architecture DFT peut être basée sur les normes existantes : IEEE 1149.1, IEEE 1500 ou la norme de test des circuits 3D en cours de développement IEEE P1838. Selon la norme utilisée, il existe deux types d'architecture BSR. Les normes de test IEEE 1500 et IEEE 1838 offrent une architecture optimisée de cellules BSR (avec 2 Mux et une bascule). De plus, les registres d'entrées/sorties des blocs logiques peuvent êtres partager avec la cellule du BSR, dans ce cas nous pouvons optimiser l'infrastructure du test tout en gardant une fonctionnalité équivalente en mode fonctionnel.

Nous analysons la testabilité d'interconnexions 3D haute densité en modes d'empilement Face-to-Face (F2F) et Face-to-Back (F2B) à l'aide des cellules BSR IEEE 1500/1838 après optimisation. Pour la simulation, nous supposons que toutes les interconnexions 3D sont testées (E/S fonctionnelles, les « dummies » qu'ils permettent de garantir une uniformité globale, etc.), mais en réalité les cellules BSR sont nécessaires uniquement pour les entrées et sorties numériques. La figure ci-dessous montre la variation du rapport entre les surfaces de la cellule BSR et la surface disponible en fonction du pas en mode de collage F2F et F2B.

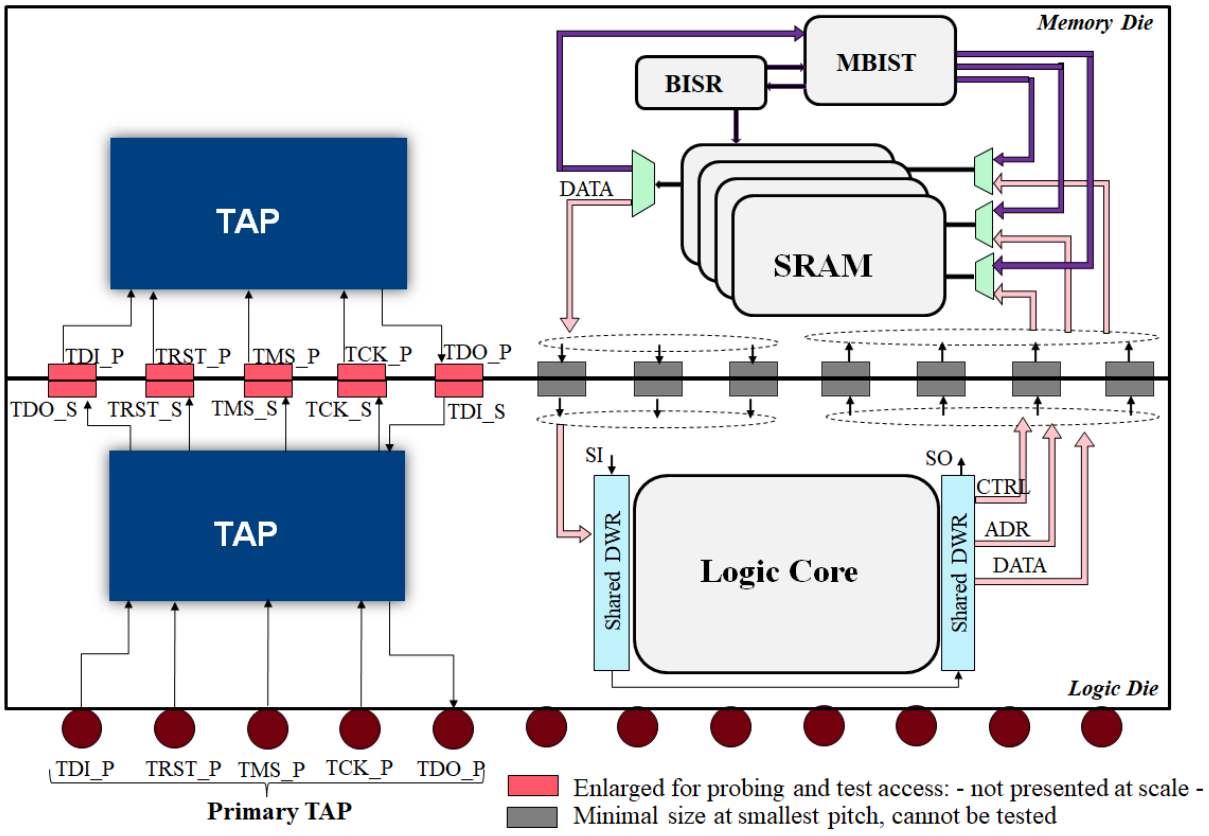


Le rapport entre la surface d'un BSR et la surface disponible en fonction du pas : (a) F2F, (b) F2B

Le pas minimal utilisant des cellules BSR optimales, techno 28 nm et un pourcentage d'infrastructure de test de 20% est égal à 3,4 µm pour le F2F et 6,5 pour le F2B. Cette

différence est due à la taille des Throught-Silicon-Via (TSV) et des Keep-Out-Zone (KOZ) autour des TSV qu'ils réduisent considérablement la zone de placement disponible pour les cellules BSR dans le mode d'empilement F2B.

Dans cette section, nous proposons dans le cadre de l'imageur intelligent, une architecture 3D-DFT optimisée pour SRAM / Logic 3D-IC utilisant le mode d'empilement F2B et l'orientation d'empilement W2W, la technologie FDSOI 28 nm, un pas de 4 µm et un diamètre TSV de 1 µm. L'idée principale de la méthode de test proposée est d'utiliser une infrastructure de test optimisée de tests de pré-liaison pour tester simultanément les matrices et les interconnexions 3D-IC à haute densité dans le test de post-liaison, la méthodologie de test pouvant tester les interconnexions entre la mémoire et la partie logiques en effectuant des opérations d'écriture et de lecture de la puce logique vers la puce mémoire.



L'architecture DFT-3D proposé

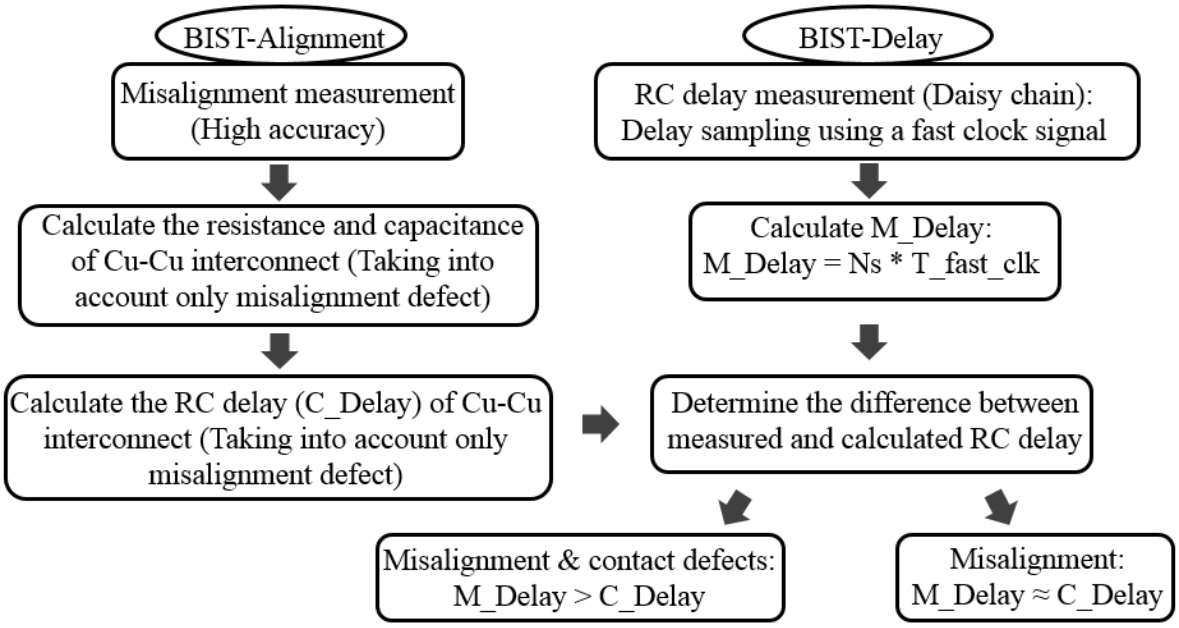
L'architecture proposée est basée sur la norme de test IEEE 1838; les interfaces primaires sont implémentées en bas de chaque puce et les interfaces secondaires sont implémentées en haut de chaque puce, la puce logique contient toutes les E / S externes comme interface principale et l'interface secondaire de la puce logique est connecté à l'interface principale de la puce de mémoire. Le mécanisme de contrôle série, équipé d'un port d'accès de test (TAP) IEEE 1149.1, comprenant quatre bornes d'entrée TDI (Test Data Input), TCK (Test Clock), TMS (Test Mode Select) et TRSTN (Test Reset), et le

borne de sortie TDO (Test Data Output). Cette interface permet de transporter des instructions, des données de configuration et des stimuli de test ainsi que des réponses de test. La figure ci-dessus montre l'architecture de l'architecture 3D-DFT optimisée. Le MBIST / BISR et le DWR partagé, accessibles via les E / S TAP (pads Cu-Cu avec un contour rouge), sont essentiels pour un test complet de pré-liaison de la mémoire et des matrices logiques.. Le test des interconnexions 3D fonctionnelles (E / S entre logique et mémoire : contrôle, adresse et signaux de données), dans le test post-liaison, se fait à l'aide d'opérations d'écriture et de lecture; la première étape consiste à écrire dans la mémoire, la séquence de test (signaux de contrôle, adresse et entrée de données) est décalée à travers les cellules DWR partagées, puis appliquée à la mémoire à travers les interconnexions 3D-IC en utilisant le multiplexeur vert dans la puce de mémoire qui doit être en mode fonctionnel. La deuxième étape consiste à lire la séquence précédemment écrite, donc de la même manière (en utilisant des cellules DWR partagées) les signaux de commande et d'adresse sont appliqués et les données de sortie sont décalées. La dernière étape consiste à comparer les données de sortie aux données d'entrée. Les signaux de données peuvent être contrôlés et observés directement par des opérations d'écriture et de lecture. Cependant, les lignes d'adresse sont unidirectionnelles et la détection des défauts doit être effectuée indirectement à l'aide de signaux de données (par exemple, en écrivant et en lisant à différentes adresses). Les signaux de contrôle, tels que la commande d'écriture ou de lecture, sont testés implicitement.

D’un autre point de vu, nous avons constaté précédemment que la séparation entre défauts d'alignement et µ-vides présente un réel défi du fait de son effet similaire sur les caractéristiques électriques. De plus, concernant la structure de test de désalignement, nous montrons que la surface des plots de test est très grande par rapport à celle des motifs. Nous montrons également que si la hauteur utilisée est inférieure à la hauteur minimale, nous ne pouvons pas utiliser BSC pour tester l'interconnexion 3D-IC. Compte tenu de toutes ces contraintes, nous pouvons dire que les mêmes structures de test utilisées pour la caractérisation doivent être utilisées en conjonction avec une architecture DFT 3D plus habituelle pour l'analyse des performances des circuits intégrés 3D et pour effectuer des tests fonctionnels et structurels d'interfaces fonctionnelles 3D haute densité.

La figure ci-dessous montre le flux de test suggéré ; le principe est de tester le défaut de désalignement (BIST-Alignment) avant la mesure du retard RC dans la marguerite (BIST-Delay) afin que nous puissions conclure sur l'impact du désalignement sur le retard. BIST-Alignment mesure le désalignement avec une grande précision en utilisant la structure d'essai de désalignement proposée (proposée au chapitre 2). La résistance et la capacité parasite sont calculées avant de calculer le retard RC obtenu. Pour le retard BIST, un signal périodique est appliqué à la connexion en série des interconnexions Cu-Cu testées et le retard de propagation est mesuré. La comparaison entre retard calculé (C_delay) et mesuré (M_delay) permet d'avoir deux cas ; le premier est lorsque C_delay

≈ M_delay, dans ce cas, nous pouvons étudier l'impact du désalignement sur le temps de propagation et caractériser les interconnexions Cu-Cu. Mais si M_delay> C_delay, alors nous pouvons valider la présence de défauts de contact.



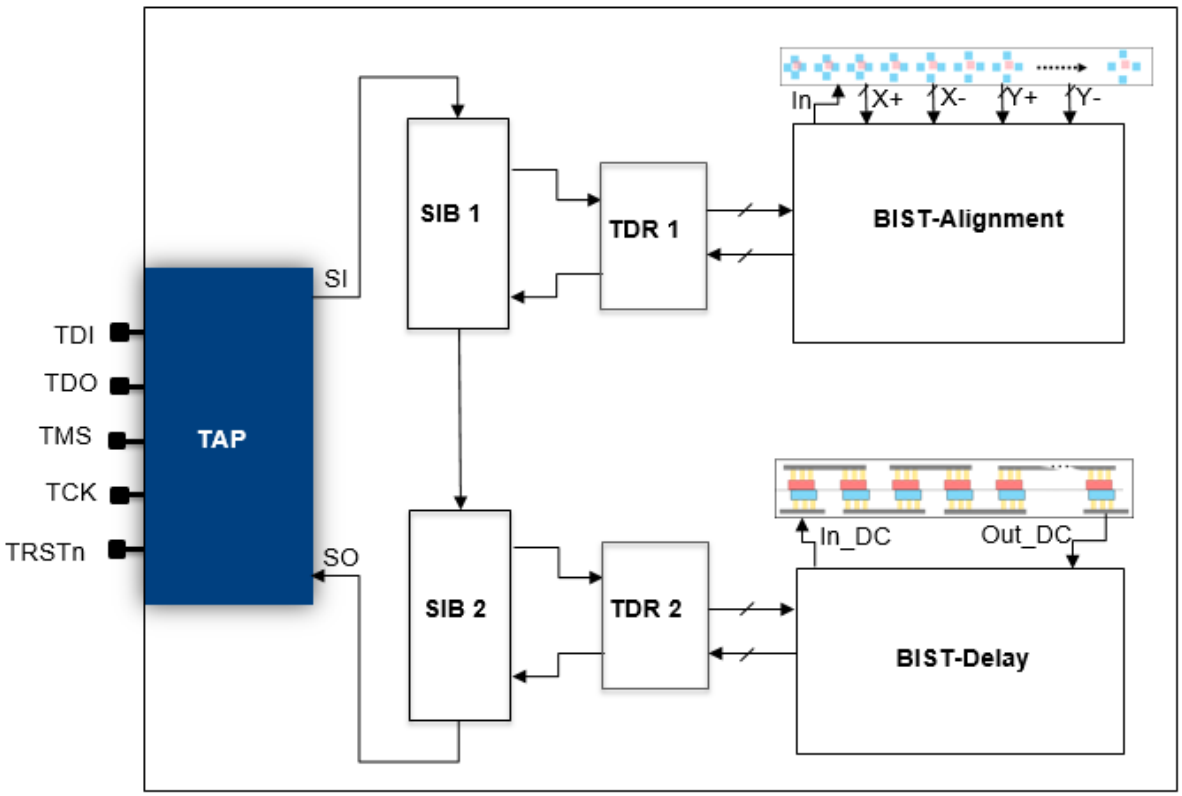
Flow de test proposé

Pour l'intégration au niveau du système Design-For-Test, les deux BIST proposés: BIST-Alignment et BIST-Delay, sont intégrés et contrôlés avec une interface JTAG (Figure ci-dessous). L'interface standard spécifiée par IEEE 1149.1 est appliquée, en utilisant le port d'accès de test standard (TAP) et les signaux TDI, TDO, TMS, TCK, TRST associés. De plus, afin de faciliter l'intégration au niveau du système DFT, les moteurs BIST sont intégrés à l'aide de la norme IEEE 1687 Internal Joint Test Action Group (IJTAG). Cela offre la possibilité de recibler le modèle de test 3D, en générant facilement des modèles de test du test pré-liaison au test post-liaison.

Essentiellement, la conception de l'infrastructure de test permet de connecter les instruments au contrôleur TAP. L'architecture consiste en deux instruments (alignement-BIST et delay-BIST) et en deux bits d'insertion de segment (SIB). Les instruments sont interfacés avec le chemin de balayage via des registres de données de test (TDR) avec des E / S parallèles. La norme IEEE 1687 introduit deux langages de haut niveau : le langage de connectivité des instruments (ICL) qui décrit les fonctions du port des instruments et la connexion logique aux autres instruments et le TAP IJTAG et le langage de description procédurale (PDL) qui décrit comment un instrument doit être utilisé.

En utilisant une spécification IJTAG, nous créons le réseau IJTAG (connectons les instruments existants et insérons des modules SIB, TDR, TAP) et extrayons la description ICL du réseau IJTAG. Les modèles de test requis sont générés à l'aide de PDL; les BIST sont stimulés avec la commande «iWrite». Ensuite, à l'aide de la commande «iApply», ces stimulations sont appliquées aux entrées primaires et enfin la

commande «iRead» permet de spécifier la réponse attendue et de récupérer les résultats des tests des BIST définis dans la description ICL et de les comparer.



Les deux BIST, intégrés dans la norme IJTAG IEEE 1687, permettent de tester et de mesurer les défauts de désalignement avec une grande précision (BIST-Alignment) et de mesurer le retard de propagation d'un signal périodique dans une chaine d'interconnexions Cu-Cu (BIST-delay).

En utilisant les résultats des tests, d'une part, l'impact du défaut de désalignement sur le temps de propagation a été étudié et, d'autre part, les défauts de contact et les « µ-voids » au niveau de la surface de contact ont été détectés.

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Appendix A: Misalignment Matlab simulator

To exhibit misalignment defect on a wafer map, we developed a specific tool using MATLAB in W2W context "virtual wafer vector map tool" to enable us to easily visualize the superposition of translation, rotation and end-of-course effects as a wafer map vectors (Figure A.1). Firstly, the results text file which contains the misalignment data of the different tested wafers has been exploited to detect discontinuity and contact defects and to determine the misalignment value for five wafers with 71 measurement points for each wafer. Therefore, the data obtained were processed using statistic function like histogram, boxplot … then displayed in wafer map form. Moreover, the obtained results has been compared with overlay measurements.

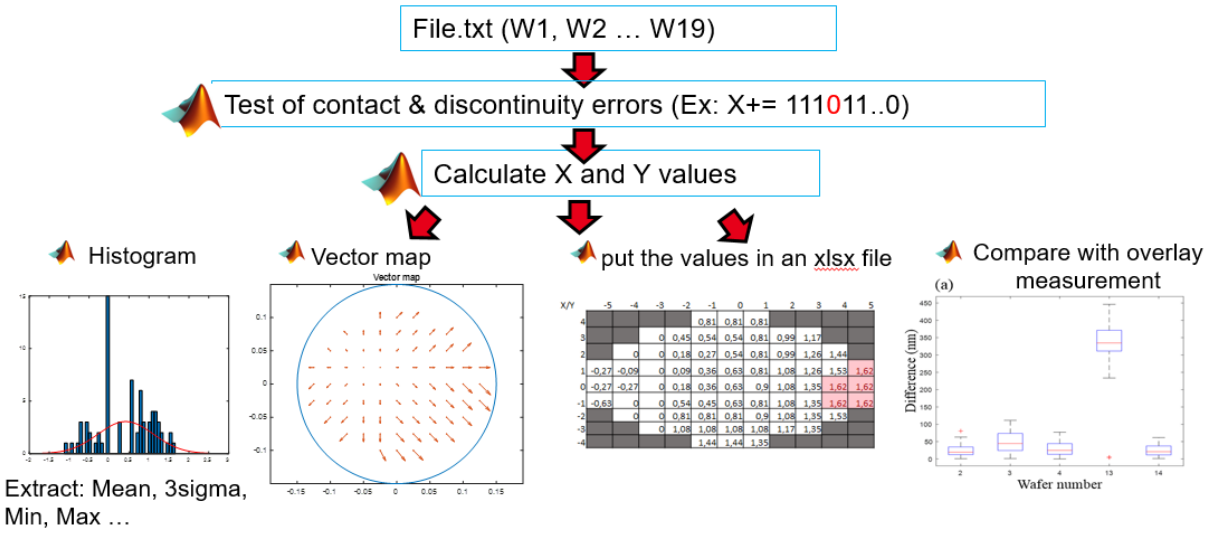

Figure A.1: principle of the developed virtual wafer vector map tool

- Used commands for statistic study:

```
% max, min, 3sigma
mean_x= mean(X);
mean_y= mean(Y);
sigma_x= (var(X))^(0.5);
sigma_y= (var(Y))^(0.5);
M_p_3sigma_x = mean_x +(3* sigma_x);
M_p_3sigma_y = mean_y +(3* sigma_y);
min_x = min (X);
min_y= min (Y);
max_x = max (X);
max_y= max (Y);
median_x=median(X);
median_y=median(Y);
```

- Xlsx write:

```
%% Mean, Min, Max, 3sigma (VT) ...
xlswrite(filename_2,mean_x,Wafer_n,'AH7');
xlswrite(filename_2,mean_y,Wafer_n,'AI7');
xlswrite(filename_2,sigma_x,Wafer_n,'AH8');
xlswrite(filename_2,sigma_y,Wafer_n,'AI8');
xlswrite(filename_2,M_p_3sigma_x,Wafer_n,'AH9');
xlswrite(filename_2,M_p_3sigma_y,Wafer_n,'AI9');
xlswrite(filename_2,min_x,Wafer_n,'AH10');
xlswrite(filename_2,min_y,Wafer_n,'AI10');
xlswrite(filename_2,max_x,Wafer_n,'AH11');
xlswrite(filename_2,max_y,Wafer_n,'AI11');
xlswrite(filename_2,median_x,Wafer_n,'AH12');
xlswrite(filename_2,median_y,Wafer_n,'AI12');
```

- Wafer map:

```
% results W2
fl=figure;
plot(X,Y);
hold on ;
q=quiver(Posx,Posy,X,Y,0);
set(q,'Marker','.')
title('Wafer map (W2)');
axis equal
```

- Box plot:

```
figure;
Err_X = [Err_X_W2; Err_X_W3; Err_X_W4;Err_X_W13; Err_X_W14]; % difference between VT results and overlay measurements
    g = [2*ones(length(Err_X_W2),1); 3*ones(length(Err_X_W3),1); 4*ones(length(Err_X_W4),1);13*ones(length(Err_X_W13),1);
        14*ones(length(Err_X_W14),1)];
    % boxplot for (W2, W3, W4, W13 and W14
    boxplot(Err_X,g);
xlabel('Wafer number')
ylabel('Difference (nm)')
title('Pitch 3.44: Difference between test vehicle measurement & overlay (X)')
figure;
 Err_Y = [Err_Y_W2; Err_Y_W3;Err_Y_W4;Err_Y_W13;  Err_Y_W14];
    g = [2*ones(length(Err_Y_W2),1); 3*ones(length(Err_Y_W3),1); 4*ones(length(Err_Y_W4),1);13*ones(length(Err_Y_W14),1);
        14*ones(length(Err_Y_W14),1)];   % boxplot for (W2, W3, W4, W13 and W14
    boxplot(Err_Y,g);
xlabel('Wafer number')
ylabel('Difference (nm)')
title('Pitch 3.44:Difference between test vehicle measurement & overlay (Y)')
```

Appendix B: BISTs misalignment & µ-void, specifications, DFT insertion flow and implementation

For Design-For-Test system level integration, the two proposed BIST engines: BIST-Alignment and BIST-Delay, are integrated and controlled with a JTAG interface. The standard interface specified by IEEE 1149.1 is applied, using the standard Test Access Port (TAP), and associated TDI, TDO, TMS, TCK, TRST signals. Moreover, in order to provide easy DFT system level integration, the two BISTs have been integrated using the IEEE 1687 Internal Joint test Action Group (IJTAG) standard. This offers the possibility of 3D test pattern retargeting, by easily generate test patterns from pre-bond test to post-bond test.

B.1) BISTs description:

B.1.a- BIST Alignment:

The BIST alignment is composed of two parts (Figure B.1): a passive part (18 patterns: similar to passive version patterns) and the BIST that allows to control the test and the generation of results. The BIST architecture should ensure: the launch of the BIST, detection of contact (We have more than two contact between top and bottom Cu-pads) and discontinuities faults (The pattern outputs are not consistent: e.g. 110110...00), counting the misalignment values (X and Y) during a given time and generation of a final result signals (Test alignment, Contact number, value X/Y). All input and output signals are presented in the Table B.1.

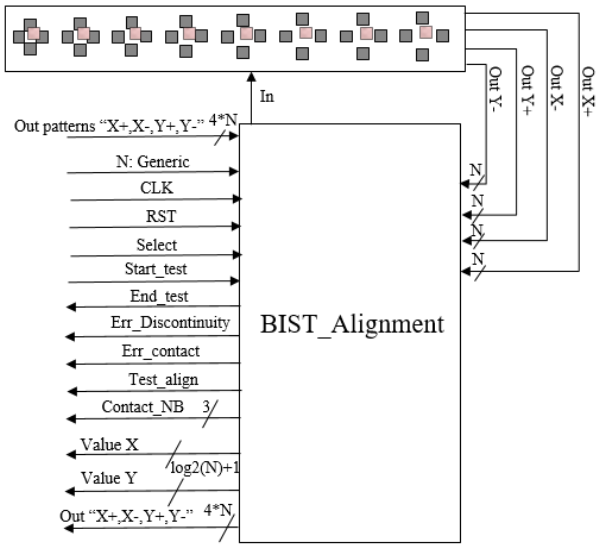

Figure B.1: BIST Alignment architecture

I/O's	Direction	Description
CLK	Input	External clock
RST	Input	Asynchronous reset (negative edge)
Select	Input	Allows to choose between the outputs of the patterns or inputs impose from outside to test BIST
N	Generic	Number of patterns
Start_test	Input	Start the test
In	Input	Input of patterns ='1'
End_test	Output	The output it indicates the end of test
Err_discontinuity	Output	Presence of discontinuity fault
Err_contact	Output	Presence of contact fault
Test_align	Output	Test alignment: '0' (Perfect alignment); '1' (Misalignment)
Contact_NB <2:0>	Output	Contact number between top and bottom Cu-pads (0 to 4)
Value_X <M:0>	Output	The X misalignment value : M=(log2(N))+1 (1: bit of sign)
Value_Y <M:0>	Output	The Y misalignment value : M=(log2(N))+1 (1: bit of sign)
Out_patterns (X+, X-, Y+ and Y-) <N:0>	Output	Patterns outputs (see them in case of default of contact or discontinuity)

Table B.1: BIST Alignment Input/ Output description

B.1.b- BIST Delay:

Figure B.2 shows the architecture of BIST-Delay, a periodic signal (Clk) is injected through the daisy chain, the propagation delay between the reference signal (In_DC) and the daisy chain output (DC_out) is sampled using a very fast clock (Clk_2). Then, from the signature "Count", we can determine the RC delay of the daisy chain. The BIST-Delay is also able to detect a full open defect (discontinuity of the daisy chain); Test_error =1.

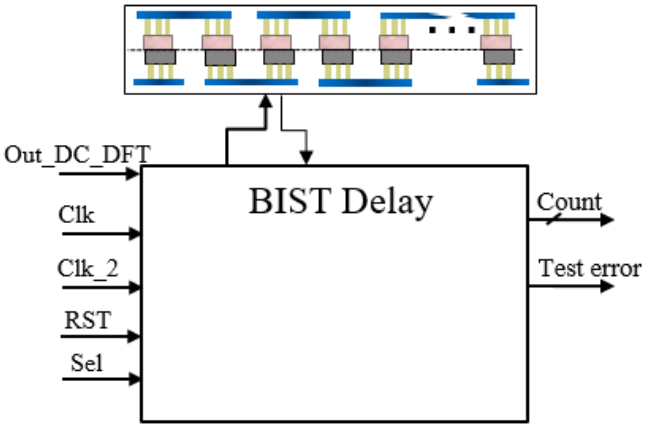

Figure B.2: BIST Delay architecture

B.2) DFT insertion:

The BISTs design was done in a digital design flow: RTL description, logic synthesis, simulation … The IJTAG logic insertion was done using Tessent Boundary-scan tool; using an IJTAG specification, we create the IJTAG network (connect existing instruments and insert SIBs, TDRs, TAP controller) and extract the ICL description of the IJTAG network. The required test patterns are generated using PDL. The chip-level PDL commands can be translated to ATE (Automatic Test Equipment) pattern formats (STIL, WGL ...) useful as test vectors to be applied to the top level TAP or for simulation test benches that verify the ICL of the BISTs descriptions. The pattern generation flow is shown in figure B.3.

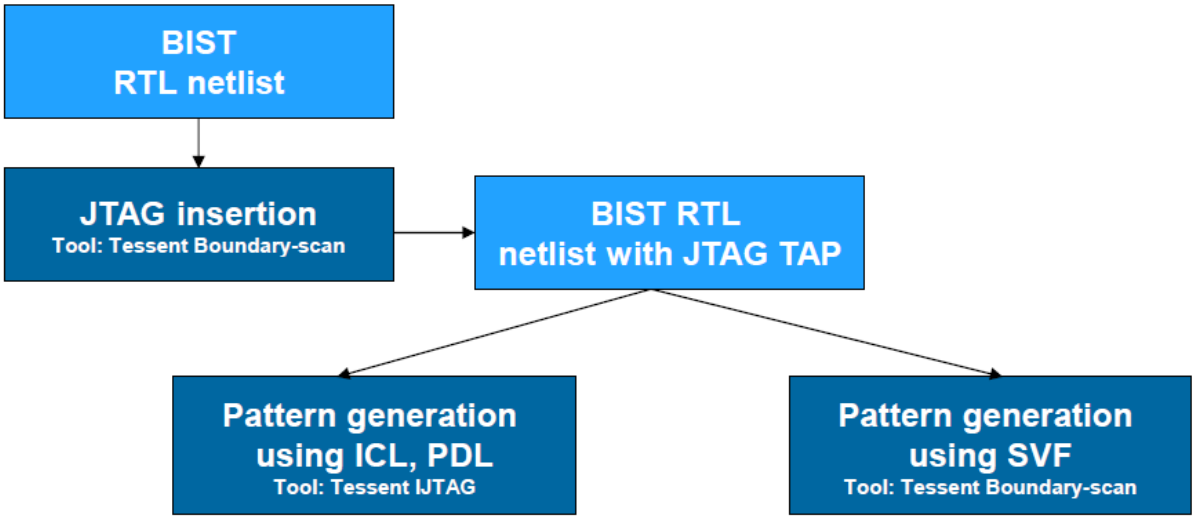

Figure B.3: DFT insertion step

The IJTAG insertion flow is done on four steps (Figure B.4):

- Checking (DFT rules, libraries ...): We use ETChecker tool to check the environment including all necessary files: netlists, libraries, check clock information and design rules of the design.
- Generation of the test plan environment: define output directories
- Insertion and Verification of embedded test: generate RTL netlist with embedded IJTAG logic coded in Verilog RTL. Additional verification steps are required to verify correct DFT insertion, create test benches and run RTL simulations.
- Extract ICL files and test pattern generation

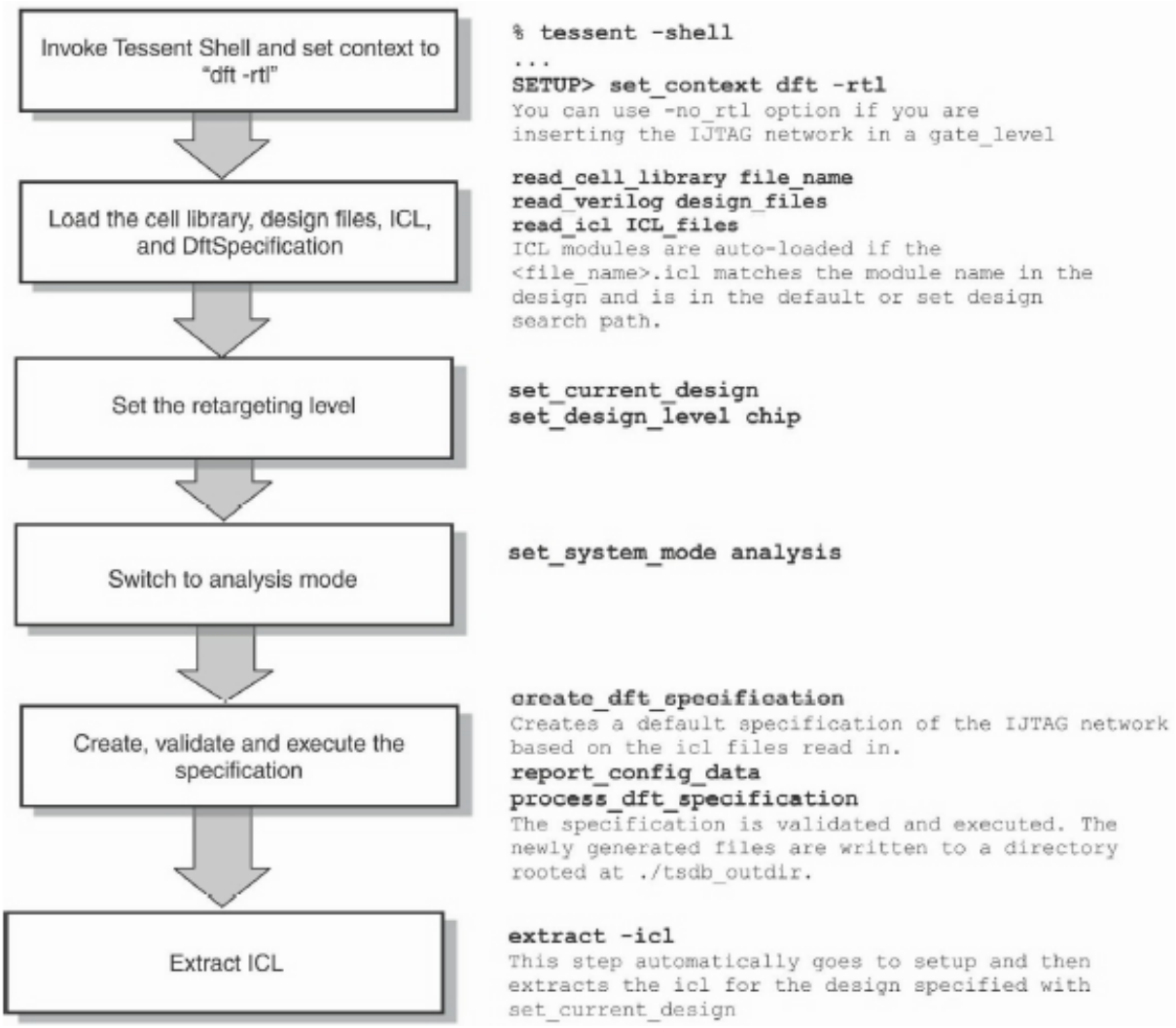

Figure B.4 DFT insertion flow

The used file for DFT specification is illustrated in figure B.5, this code allows to define the JTAG interfaces: TAP control, TDRs, SIB … and the ICL files extraction.

In addition to the ICL description, a PDL procedure is required to perform test pattern generation according to a retargeting level. The BISTs are stimulated with the command “iWrite”. Then, using the “iApply” command, these stimulations are applied to the primary inputs and finally the “iRead” command allow to specify expected response and retrieve the test results of BISTs that are defined in the ICL description and compare them. Figure B.6 shows the used PDL file.

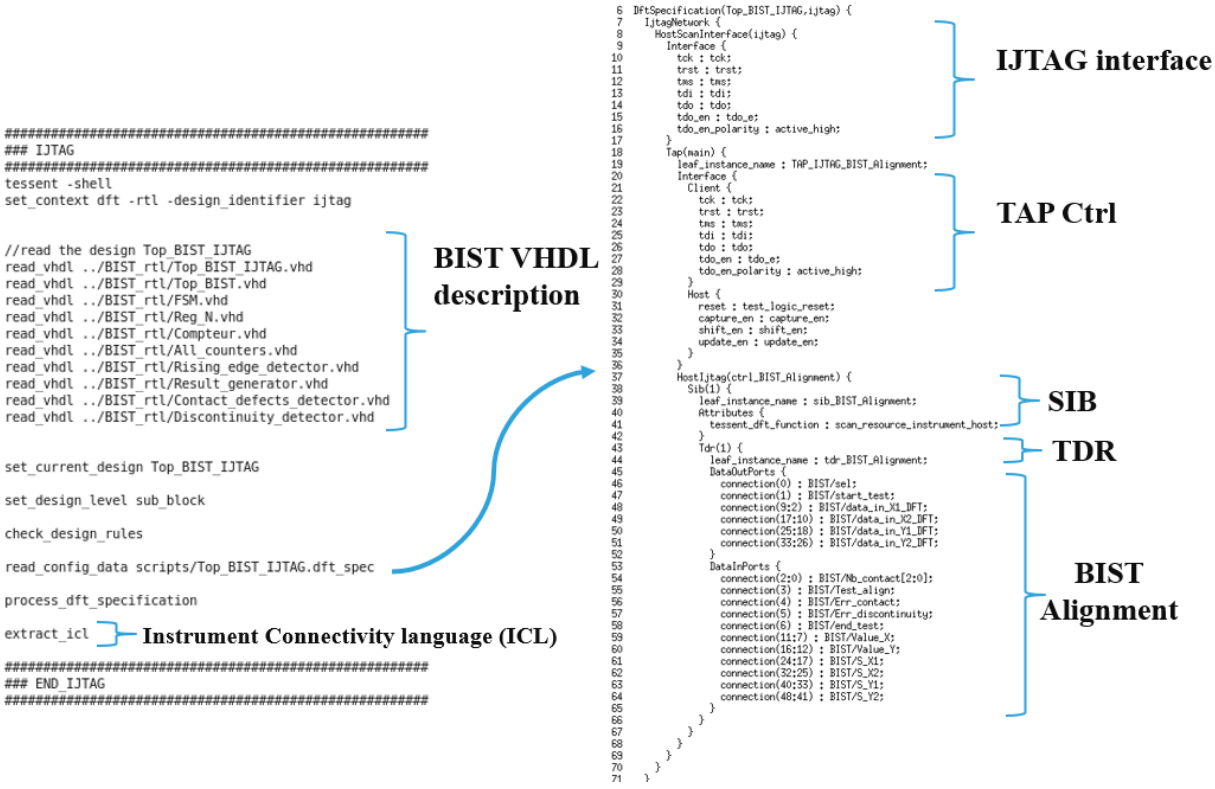

Figure B.5: DFT specification and ICL extraction

```
iProcsForModule Top_BIST_IJTAG
iProc X1_Y1 {  }  {
iWrite tdr_BIST_Alignment.ijtag_data_out[0] 0b0 \\ RST ='0'
iApply
iWrite tdr_BIST_Alignment.ijtag_data_out[0] 0b1 \\ RST ='1'
iWrite tdr_BIST_Alignment.ijtag_data_out[1] 0b1  \\ Sel ='1': Select input
iWrite tdr_BIST_Alignment.ijtag_data_out[2] 0b1  \\ start_test ='1'
iWrite tdr_BIST_Alignment.ijtag_data_out[10:3]  0b11110000 \\ X1
iWrite tdr_BIST_Alignment.ijtag_data_out[18:11] 0b00000000  \\ X2
iWrite tdr_BIST_Alignment.ijtag_data_out[26:19] 0b11000000   \\ Y1
iWrite tdr_BIST_Alignment.ijtag_data_out[34:27] 0b00000000    \\ Y2
iApply
iRunLoop 7-tck
iRead tdr_BIST_Alignment.ijtag_data_in[2:0] 0b010  \\ Nb_contact
iRead tdr_BIST_Alignment.ijtag_data_in[3] 0b0      \\ Test_align
iRead tdr_BIST_Alignment.ijtag_data_in[4] 0b0      \\ Err_contact
iRead tdr_BIST_Alignment.ijtag_data_in[5] 0b0      \\ Err_discontinuity
iRead tdr_BIST_Alignment.ijtag_data_in[6] 0b1      \\ End_test
iRead tdr_BIST_Alignment.ijtag_data_in[11:7] 0b00100   \\ Value_X
iRead tdr_BIST_Alignment.ijtag_data_in[16:12] 0b00010  \\ Value_Y
iRead tdr_BIST_Alignment.ijtag_data_in[24:17] 0b11110000 \\ S_X1
iRead tdr_BIST_Alignment.ijtag_data_in[32:25] 0b00000000 \\ S_X2
iRead tdr_BIST_Alignment.ijtag_data_in[40:33] 0b11000000 \\ S_Y1
iRead tdr_BIST_Alignment.ijtag_data_in[48:41] 0b00000000 \\ S_Y2
iApply
}
```

Figure B.6: PDL file for BIST Alignment

B.3) Simulation:

An example of pattern simulation for BIST Alignment is shown in figure B.7; to validate the alignment BIST, <e provoke a contact and discontinuity defects (data_in_y1= “11101000”) and contact defect (contact in Y1 “Y+” and Y2 “Y-“). The test results show that we have contact and discontinuity defects. We show also that simulated and expected patterns are identical.

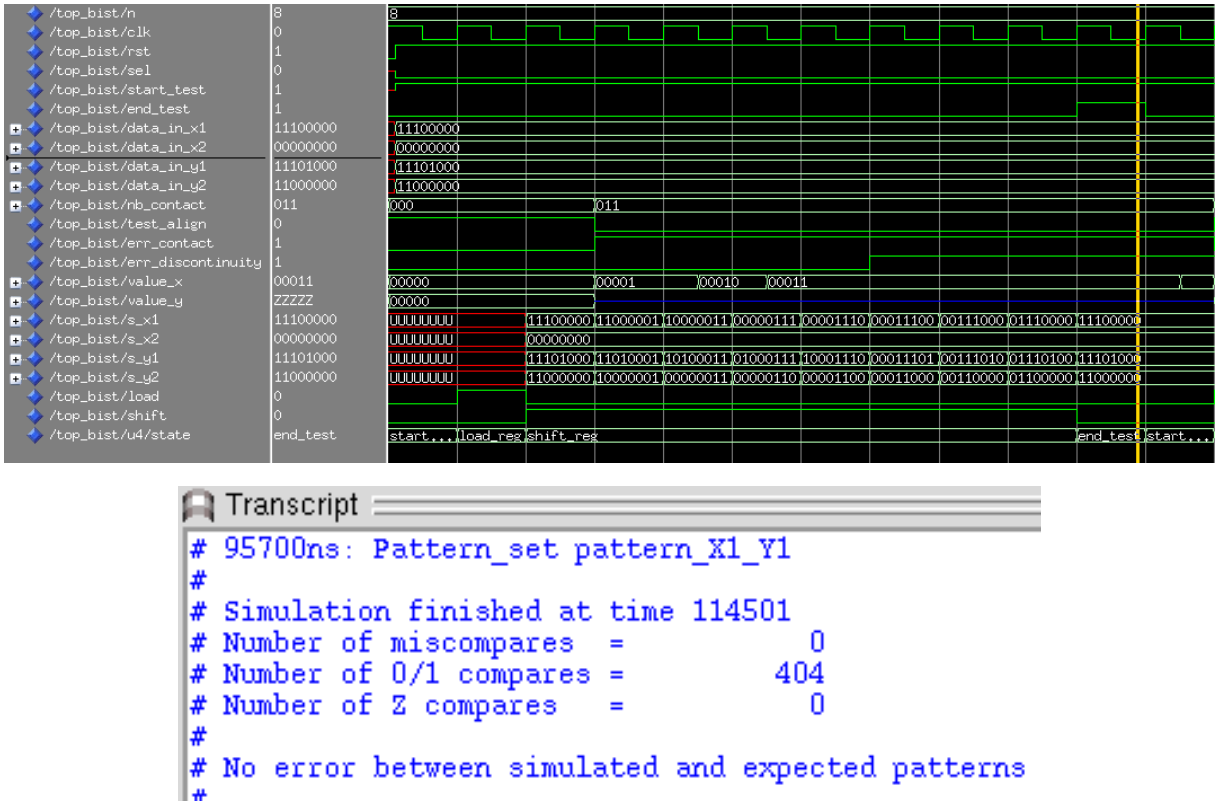

Figure B.7: pattern simulation for BIST Alignment

The proof of concept of the test architecture was first completed thanks to VHDL simulation using a test signals: “X+X-Y+Y- test” (BIST alignment) and “Out_DC_test” (BIST delay) and mixed simulation using the equivalent electrical model of Cu-Cu interconnects. The proposed IJTAG architecture has been fully implemented using the commercial Mentor Graphics Tessent® product suite for Design-for-Test, logic insertion and test pattern generation. The proposed architecture was implemented using a FDSOI 28 nm standard cell libraries for Wafer-to-Wafer stacking with a pitch of 3.45 µm.

Abstract

The integration of multiple chips in a 3D stack serves as another path to move forward in the more-than-Moore domain. 3D integration technology consists in interconnecting the integrated circuits in three dimensions using inter-die interconnects (µ-bumps or Cu-Cu interconnects) and Through Silicon Vias (TSV). This changeover from horizontal to vertical interconnection is very promising in terms of speed and overall performances (RC delay, power consumption and form factor). On the other side, for technology development of 3D integration before the production of the 300 mm wafers with all FEOL and BEOL layers, several short-loops must been carried out to enable incremental characterization and structural test of 3D interconnects in order to evaluate the electrical performances (R, L, C …). In the other hand, the test of application circuits consists in adding testability features (Boundary-Scan-Cells (BSCs), Built-In-Self-Test (BIST) and scan chains …) for functional test of the hardware product design (including the different stacked dies and the 3D interconnections) . The added Design-For-Test (DFT) architecture make it easier to develop and apply manufacturing tests to the designed hardware. Compared to µ-bumps, Cu-Cu hybrid bonding provides an alternative for future scaling below 10µm pitch with improved physical properties but that generates new challenges for test and characterization; the smaller the Cu pad size, the more the fabrication and bonding defects have an important impact on yield and performance. Defects such as bonding misalignment, micro-voids and contact defects at the copper surface, can affect the electrical characteristics and the life time of 3D-IC considerably. Moreover, test infrastructure insertion for HD 3D-ICs presents new challenges because of the high interconnects density and the area cost for test features. Hence, in this thesis work, an innovative misalignment test structure has been developed and implemented in short-loop way. The proposed approach allows to measure accurately bonding misalignment, know the misalignment direction and estimate the contact resistance. Afterwards, a theoretical study has been performed to define the most optimized DFT infrastructure depending on the minimum acceptable pitch value for a given technology node to ensure the testability of high-density 3D-ICs. Furthermore, an optimized DFT architecture allowing pre-bond and post-bond for high-bandwidth and high-density 3D-IC application (SRAM-on-Logic) has been proposed. Finally, to assess performance of HD 3D-ICs, two complementary BISTs has been implemented in an application circuit using the same misalignment test structure developed above and a daisy chain of Cu-Cu interconnects. Using test results, on the one hand, the impact of misalignment defect on the propagation delay has been studied and on the other hand full open and µ-voids defects at the contact surface level has been detected.

Key words: 3D-IC, high density interconnects, Cu-Cu hybrid bonding, misalignment, µ-void, test vehicles, DFT.

Résumé

L'intégration de plusieurs puces dans un empilement 3D constitue un autre moyen d'avancer dans le domaine « More-than-Moore ». L'intégration 3D consiste à interconnecter les circuits intégrés en trois dimensions à l'aide des interconnexions inter-puces (µ-bumps ou Cu-Cu interconnexions) et les TSVs (Through Silicon Vias). Ce passage d'une interconnexion horizontale à une interconnexion verticale est très prometteur en termes de rapidité et de performances globales (délai RC, consommation et facteur de forme). D'autre part, pour le développement technologique de l'intégration 3D avant la production des plaques (wafers) de 300 mm avec toutes les couches FEOL et BEOL, plusieurs plaques (short-loop) doivent être réalisées pour permettre la caractérisation incrémentale et le test structurel des interconnexions 3D afin d'évaluer la performances électriques (R, L, C…). D'autre part, le test des circuits d'application consiste à ajouter des fonctionnalités de testabilité (Boundary-Scan-Cells (BSC), Built-In-Self-Test (BIST) et des chaînes de scan …) pour le test fonctionnel du circuit 3D (y compris les puces empilées et les interconnexions 3D). L'architecture DFT (Design-For-Test) ajoutée facilite le développement et l'application des tests de fabrication au circuit conçu. Par rapport aux interconnexions µ-bumps, la liaison hybride Cu-Cu offre une alternative pour descendre au-dessous de 10µm de pas entre les interconnexions (pitch) avec des propriétés physiques améliorées, mais cela génère de nouveaux défis pour les tests et la caractérisation; plus la taille de la plaque de cuivre est petite, plus les défauts de fabrication et de liaison ont un impact important sur le rendement et les performances. Des défauts tels que le désalignement, des « µ-voids » et des défauts de contact à la surface du cuivre peuvent affecter considérablement les caractéristiques électriques et la durée de vie du circuit 3D. De plus, l'insertion d'une infrastructure de test pour les circuits intégrés 3D HD présente de nouveaux défis en raison de la densité d'interconnexions élevée et du coût de l'insertion de l'infrastructure du test. C'est dans ce contexte que s'inscrit cette thèse de doctorat dans laquelle une structure de test innovante de désalignement a été développée. L'approche proposée permet de mesurer avec précision le désalignement des interconnexions, de connaître la direction du désalignement et d'estimer la résistance de contact. Une étude théorique a ensuite été réalisée pour définir l'infrastructure DFT la plus optimisée en fonction de la valeur du pas minimal acceptable pour un nœud technologique donné, afin de garantir la testabilité des circuits 3D haute densité. De plus, une architecture DFT optimisée permettant un test avant et après assemblage des circuits 3D haute densité (Mémoire-sur-Logique) a été proposée. Enfin, pour évaluer les performances des circuits 3D haute densité, deux BISTs complémentaires ont été mis en œuvre dans un circuit d'application utilisant la même structure de test de désalignement développée ci-dessus et une chaîne d'interconnexions Cu-Cu. En utilisant les résultats des tests, d'une part, l'impact du défaut de désalignement sur le temps de propagation a été étudié et, d'autre part, les défauts de contact et les « µ-voids » au niveau de la surface de contact ont été détectés.

Mots clés: 3D-IC, interconnexions haute densité, collage hybride Cu-Cu, désalignement, « µ-void », véhicules de test, DFT.