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THÈSE

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Electromagnétisme et Photonique - Laboratoire
d'hyperfréquences et de caractérisation**
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Automatique, Traitement du Signal (EEATS)**

Echantillonneur opto-electronique femto seconde

Femto second sampler

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Declaration of Authorship

I, Hanae ZEGMOUT, declare that this thesis titled, "Femto-second sampler" and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
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- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

Signed: _____ Hanae ZEGMOUT

Date: _____ 10/10/2019

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*To my parents and my sisters Hind & Laila and to all
my friends and coworkers ...*

Résumé de thèse : Echantillonneur femto-seconde

Dans un monde de plus en plus connecté, il devient indispensable de trouver des moyens d'augmenter le débit d'informations qu'il est possible de véhiculer et de traiter. Ce besoin impose aux ingénieurs des contraintes plus serrées en termes de bande passante et de fréquence d'horloge des circuits qu'ils conçoivent.

En microélectroniques, cela constitue un réel obstacle pour la conception de circuits plus avancés. En effet, les horloges électroniques sont limitées par leur performance en termes de stabilité de la période d'horloge (cf fig1). Cela provient du bruit qui est inhérent à la structure du circuit de l'horloge.

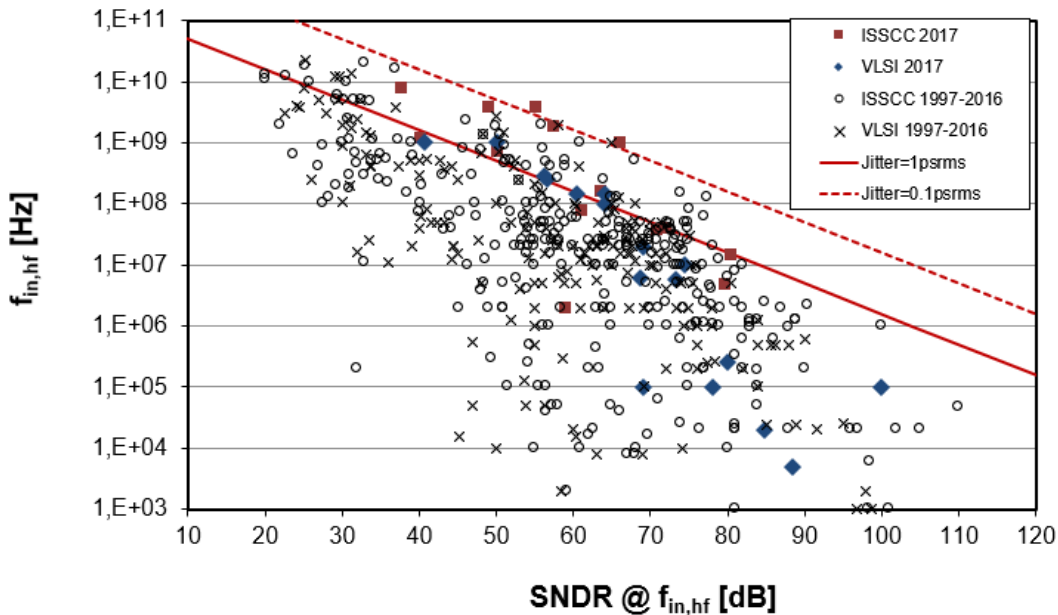


Figure 1: Limitation de la fréquence d'échantillonnage en fonction de la gigue d'horloge

En effet, une période d'horloge instable implique que le signal à traiter n'est pas échantillonné au bon moment. L'erreur alors commise au niveau

du signal échantillonné est d'autant plus grande que la fréquence du signal échantillonné est haute.

La photonique intégrée sur Silicium constitue une solution potentielle à ce problème. En effet, les horloges optiques, i.e les lasers pulsés, présentent des performances très intéressantes en termes de stabilité ou de gigue en comparaison avec les horloges en microélectroniques. Les lasers pulsés en photoniques présentent, même en version industrielle, des giges de l'ordre de 10fs alors que les horloges microélectroniques atteignent à peine les 50fs de gigue, et seulement dans la littérature.

L'idée principale de cette thèse est de tirer profit de la performance des lasers pulsés en gigue en concevant un circuit optoélectronique piloté par le laser et permettant d'échantillonner un signal électrique RF (cf figure 2).

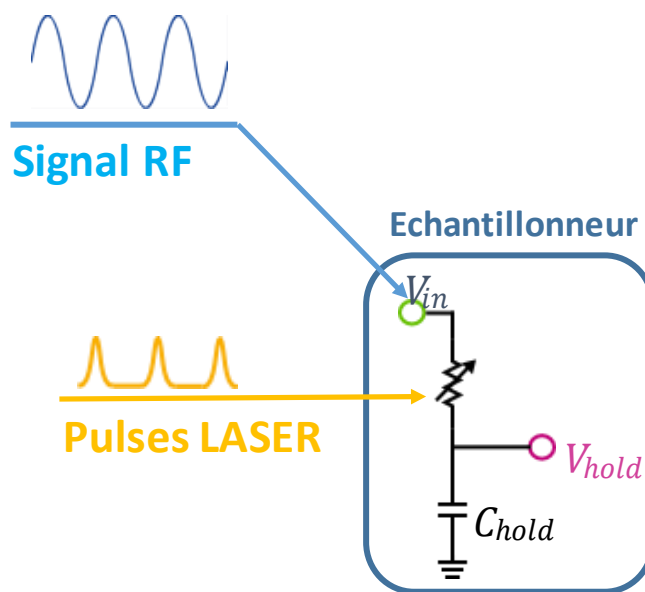


Figure 2: Circuit de base de l'échantillonneur optoélectronique

On utilise dans cette thèse un laser de longueur d'onde : 1550nm présentant une gigue de 11fs avec des pulses de 100fs toutes les 10ns. Les pulses du laser sont couplés dans une fibre et sont ainsi élargis de façon à ce que le circuit d'échantillonnage perçoive des pulses de 3,4ps au lieu de 100fs. Cette étape est nécessaire au fonctionnement du circuit parce que

100fs est une valeur très faible comparée aux constantes de temps de la partie électrique du circuit.

La brique de base du circuit en question est un photoconducteur en Germanium : une résistance en Germanium dont la résistivité varie selon la puissance du signal optique qu'elle reçoit du laser pulsé. Le photoconducteur dans ce cas précis joue le rôle d'un interrupteur piloté par le laser, et connecte l'entrée RF à la capacité d'échantillonnage (cf fig2). Quand l'interrupteur reçoit un pulse de lumière sa résistance chute et le signal RF peut être copié vers la capacité. Dès que le pulse de lumière s'arrête, le photoconducteur en Germanium retrouve sa résistance initiale et déconnecte ainsi l'entrée RF de la capacité qui contient le signal échantillonné.

Cette thèse se propose d'étudier la faisabilité d'un tel circuit et la possibilité d'exploiter la performance des lasers en termes de stabilité de l'horloge dans l'échantillonnage d'un signal électrique.

Dans un premier temps, nous avons essayé d'implémenter le circuit de base présenté auparavant. Nous avons constaté plusieurs problèmes :

- **Effet 1** : Les valeurs des résistances Off du photoconducteur utilisées n'étaient pas assez élevées pour permettre de déconnecter entièrement le signal RF de la capacité d'échantillonnage. Cette
- **Effet 2** : Le passage de la valeur Off à la valeur On du photoconducteur en Germanium ne se fait pas de manière instantanée ce qui complique d'autant plus le travail de l'échantillonneur.

Le premier effet provient de la présence d'un dopage résiduel de type P (Bore) au niveau du Germanium que nous avons utilisé. Ce dopage est relatif au procédé de fabrication à STMicroelectronics et ne peut pas être évité en amont (au moins pas à notre niveau). Cet effet est très gênant au niveau de la fonctionnalité du circuit d'échantillonnage parce qu'une faible résistance Off implique que le signal échantillonné n'est pas stocké longtemps au niveau de la capacité d'échantillonnage.

Le simple fait d'utiliser une géométrie plus conséquente pour le photoconducteur afin d'obtenir une grande valeur de R_{off} n'est pas une bonne option car cela entraînerait une augmentation de la valeur de R_{on} , ce

qui impliquerait que le signal ne serait même pas copié proprement vers la capacité d'échantillonnage.

Le deuxième effet est également important parce que ses conséquences sur le signal échantillonné sont du même ordre que celles du premier effet.

Nous avons donc essayé de contourner ces problèmes en utilisant trois méthodes :

- **Méthode 1** : une nouvelle géométrie des photoconducteurs en Germanium qui permettrait de maximiser les rapport Roff/Ron (géométrie brevetée).
- **Méthode 2** : Un contre dopage de type N (Phosphore) afin de contourner le dopage résiduel du Germanium.
- **Méthode 3** : L'utilisation d'un circuit électronique qui permet de re-échantillonner le signal en sortie du circuit de base avant qu'il soit perdu à cause des deux effets précédemment expliqués.

La première méthode repose sur le constat que la lumière est absorbée au niveau du Germanium de manière exponentiellement décroissante. Aussi, la géométrie utilisée épouse la décroissance de la lumière et permet ainsi d'avoir une densité de porteurs de charge photo-générés qui est homogène tout au long du photoconducteur.

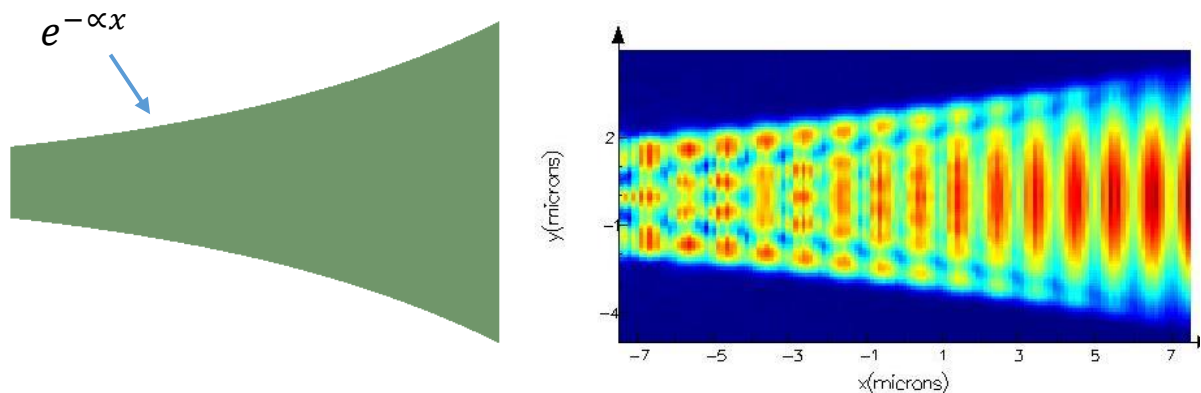


Figure 3: Propagation de la lumière dans une géométrie exponentielle

L'utilisation de cette géométrie permet d'avoir un rapport Roff/Ron deux fois plus grand que le rapport Roff/Ron d'une structure rectangulaire traditionnelle avec la même résistance Roff.

La deuxième méthode a également permis d'optimiser le rapport R_{off}/R_{on} : on a obtenu un rapport six fois plus grand que le rapport R_{off}/R_{on} initial tout en conservant la même valeur de R_{on} . Cela veut dire que la structure cristalline du Germanium n'a pas été altérée par l'application du contre-dopage.

La troisième méthode est plus élaborée, elle consiste à échantillonner le signal stocké au niveau de la capacité d'échantillonnage dès que le pulse de lumière est terminé. Afin de conserver la performance en gigue, on a utilisé pour cela un CAN (convertisseur analogique numérique) piloté par une horloge photonique créée à partir des mêmes pulses de lumière du laser.

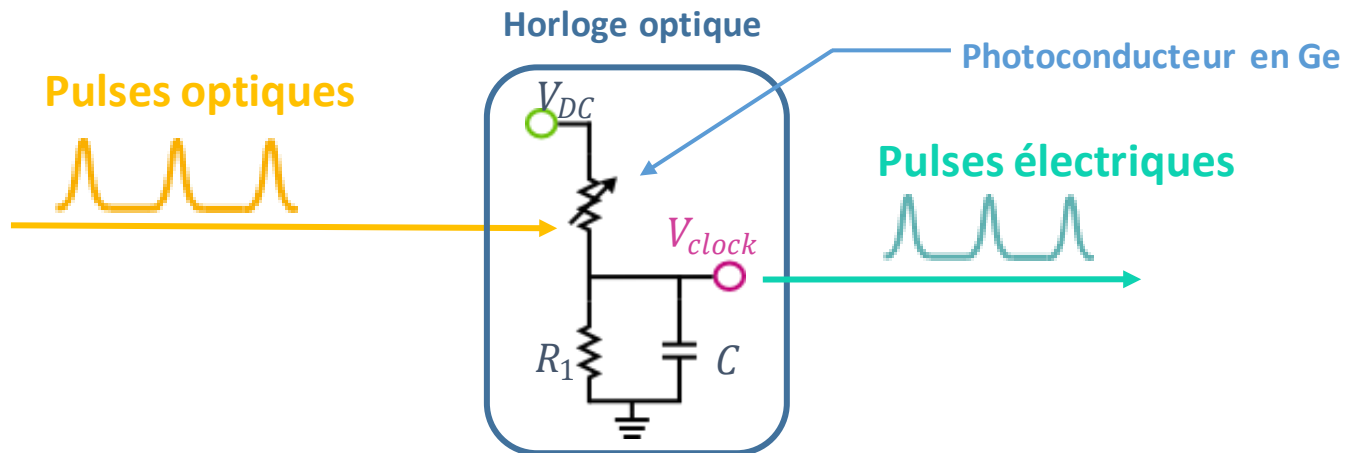


Figure 4: Schéma du circuit de l' horloge optique

Le schéma des horloges optiques ainsi créés est présenté sur la figure 4. Le seul inconvénient de ces structures est qu'elles présentent un temps de descente du signal électrique qui est très long (ce qui est dû à la valeur de R_{off} et le temps de passage de R_{on} à R_{off}).

La durée des pulses générés par ce circuit est également limitée à des dizaines de picosecondes. En effet, la génération du pulse de l'horloge est possible du moment que le signal de l'horloge reste relativement dans l'état haut.

Dans un premier temps, nous avons conçu une structure d'horloge optique qui permet d'avoir des fronts montant et descendant assez droits, ce

qui permet de maximiser la stabilité du signal d'horloge quand il se propage dans les circuits en aval (cf fig.5).

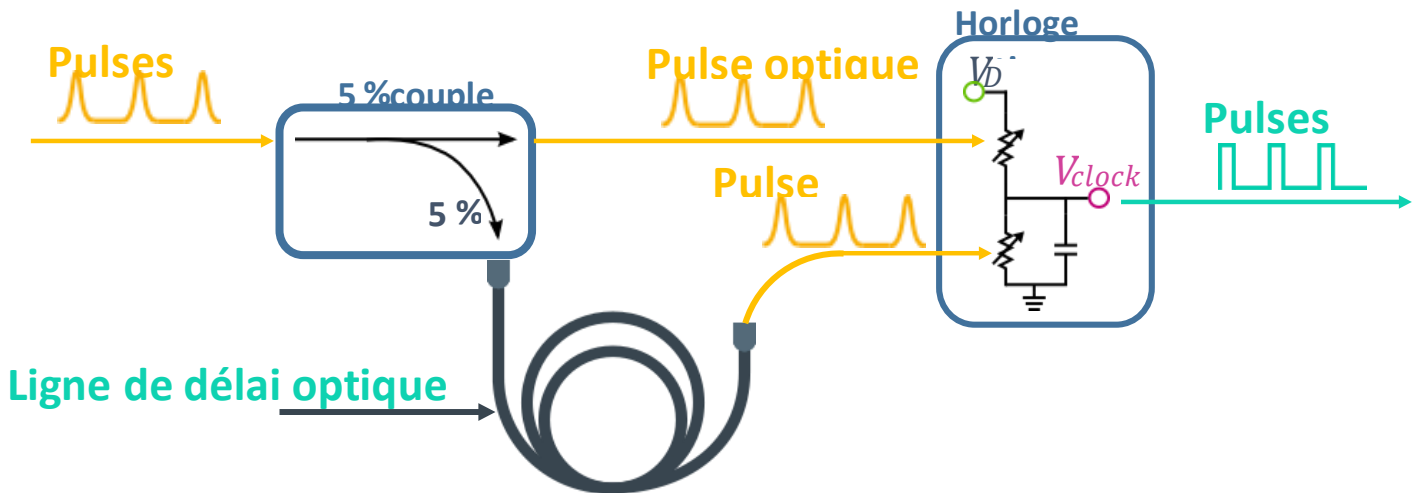


Figure 5: Schéma du circuit de la deuxième horloge optique

La durée de ces pulses est également limitée de la même manière que la structure d'horloge d'origine, dans ce cas précis, la ligne de délai optique génère un retard de 100ps.

Nous avons conçu également une dernière structure d'horloge qui utilise deux briques semblables à celles présentées dans la figure 5 et qui les combine pour créer un signal d'horloge à durée variable (cf figure 6).

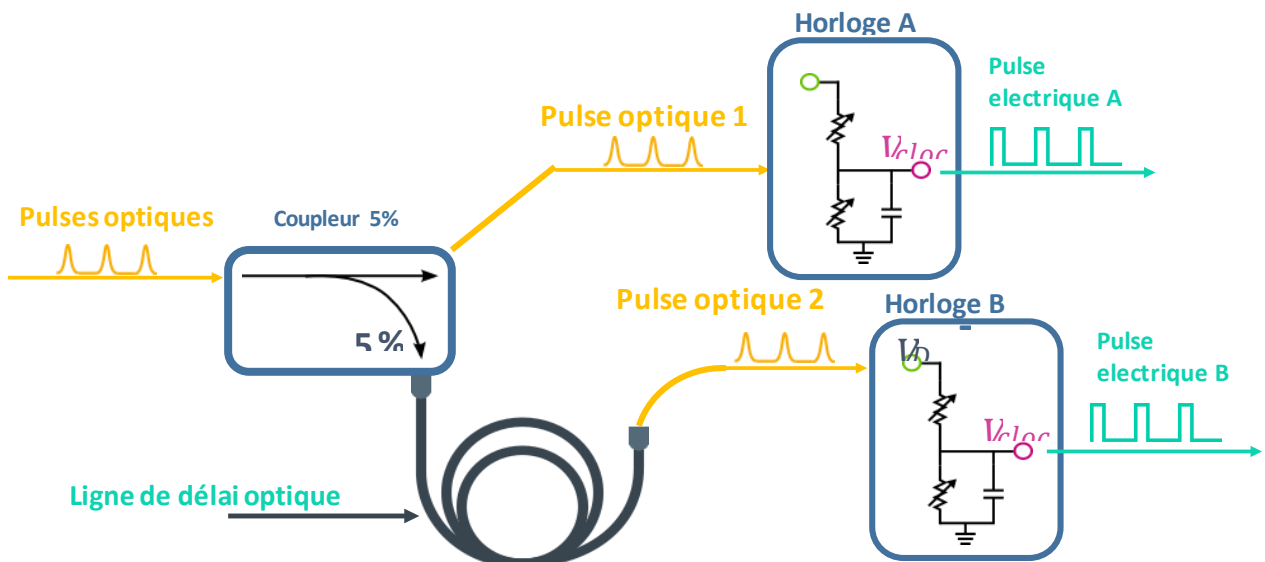


Figure 6: Schéma fonctionnel de la troisième horloge optique

Afin d'implémenter le premier circuit (échantillonneur + horloge optique simple), nous avons conçu un circuit électronique qui permet de coupler le signal électrique dans le circuit d'échantillonnage après le passage dans un câble coaxial (signal RF d'une source extérieur). Nous avons également implémenté un circuit de mise en forme du signal de l'horloge optique qui permet d'obtenir des signaux rectangulaires de durée adéquate à l'ADC en aval (approximativement 600ps).

Le dernier circuit d'horloge a également nécessité la conception d'un circuit de bascule avec les signaux Set et reset générés par les signaux en sortie des deux horloges optiques de base.

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Chapter 1

General introduction

As the world becomes more and more connected, the need for higher data throughput becomes increasingly urgent. This implies more creativity from designers to come up with higher bandwidth circuits and faster pace clocks to drive them.

However, the traditional microelectronics clock circuits fail short to fulfill the ever increasing need for higher sampling frequencies because of their inherent noise. The latter renders the sampled data altogether unusable and therefore hinders the efforts towards higher streams of data.

A fairly promising new technology field, integrated photonics, may bring an end to this problem. Indeed, when it comes to pulsed lasers, a "not that new" technology, the optical pulses clocking features a very low noise compared to its microelectronics counterpart. Indeed, even for the industrialized pulsed lasers, the clock noise, namely the jitter, is 5 times lower than the best microelectronics clock, yet the latter is only cited in literature and no industrial clock circuit was ever able to exhibit its performance.

With this idea in head, we try in this thesis to demonstrate the feasibility of a sampler with ultra low jitter using an external pulsed laser with ultra-low jitter (11fs).

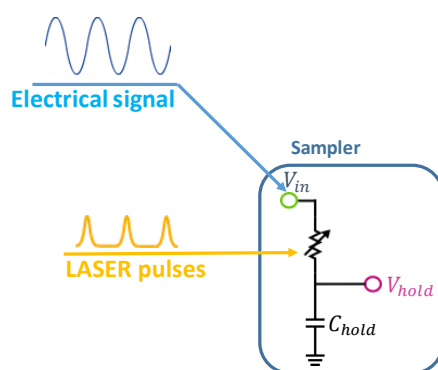


FIGURE 1.1: Electrical circuit of a basic sampler

The basic idea we start with is that of a classical microelectronics sampler, where the switch is replaced by a photo conducting material driven by the pulsed laser as depicted in fig.1.1.

As illustrated in the scheme, the switch plays the role of a variable resistance that is driven by the pulsed laser. This component counterpart in integrated photonics is a photo-conductor and is rarely used in nowadays photonics circuit.

Indeed, most of the optical interconnects are built with photo-diodes as light receivers. This choice is mainly due to the fact that the response of a photo-diode is directly proportional to the light intensity it receives while a photo-conductor current depends both on the light intensity and the electrical field that is applied on it. Therefore, photo-diodes fit more on interconnect circuits where the data is mainly coded by light, which is not what we are heading for in this application. This also explains why the literature is very poor when it comes to photo-conductors while it is very impressive for photo-diodes.

The photo-conducting material that we use is germanium. This is mainly due to the ease of integrating germanium in silicon-based technologies. Germanium absorption spectrum also fits perfectly with the laser wavelength (1550nm).

This thesis outline is the following:

In chapter 3, we will explain in details the photo-conductivity phenomenon. We will also discuss Germanium as our photo-conducting material and describe its properties. Finally we will present the photo-conducting circuits that we have designed, discuss their results and try to explain the behaviors they exhibit.

In chapter 4, we will present the different solutions that we intend to design. The circuits will be featured in this chapter only with their system view and generic design. We will explain each solution and present its optical and electrical components.

In chapter 5, the circuits will be presented in great details. We will explain the design choices that we made and illustrate the results of the simulations and of the final circuits, when available.

Chapter 2

Introduction:

2.1 Jitter in communications

In a reception chain, the analog-to-digital conversion (ADC) block role is highly sensitive. Errors during the conversion phase carry over the total receiver block chain performance and are hardly recovered afterwards. These errors originate possibly from the quality of the comparators, the accuracy of the comparison references, the linearity of the track and hold block but also from the accuracy of the sampling timing.

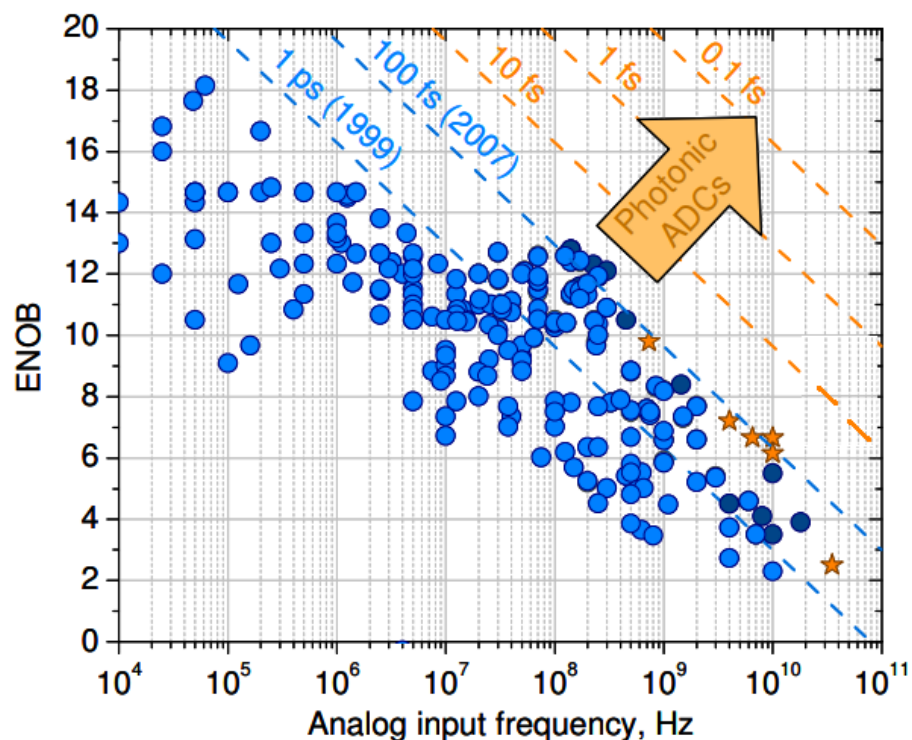


FIGURE 2.1: Plot representing the jitter impact on ENOB (Effective Number Of Bits) as a function of input frequency for ADCs (extracted from [1])

Jitter is a deviation of a given clock signal from the ideal equivalent clock output. This implies, in the case of an ADC, that the signal is sampled at the wrong time, which amounts to having an error at the sampled signal. When the frequency of the signal is high, the signal changes very rapidly, which means that a small timing error yields a consequent error at the sampled signal. This is why jitter affects and limits ADCs performance significantly at higher frequencies, see Fig.2.1.

2.1.1 Jitter in electronic clocks

The electronics-based clocks have inherent sources of noise, mainly thermal noise, that make it hard to go under a certain limit of jitter in room temperature operation. Indeed, the best electronic ADCs, to our knowledge, deliver jitter levels of 60 to 80 fs in the 100-400MHz frequency range [6].

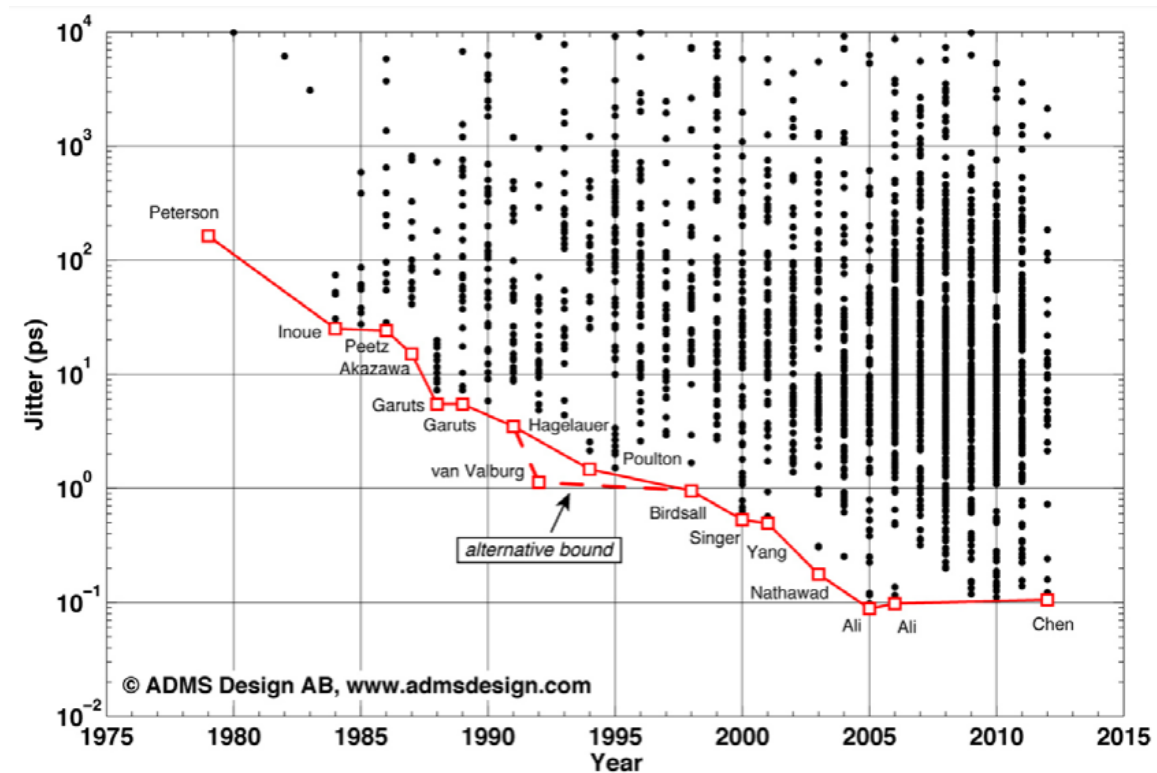


FIGURE 2.2: Plot representing jitter evolution over the years

The plot in Fig.2.2 shows the jitter evolution at any frequency taken from literature as it was described in Walden's report ¹.

¹Source:<https://converterpassion.wordpress.com/2012/07/30/adc-performance-evolution-jitter>

2.1.2 Jitter in photonics

Photonics offers an alternative solution to the jitter bottleneck problem thanks to mode-locked pulsed lasers.

These lasers exhibit nowadays, even in their commercial form, very low values of jitter (15fs).

The physical phenomena that lay behind lasers noise depends on their structure and operation process. However, in most cases, timing jitter in lasers is limited by quantum noise but is mainly dominated by the laser resonator vibrations and drift [7] [8].

The advantage that mode-locked lasers offer compared to electronic clocks has been rapidly spotted in the 70's and used in sampling and quantizing electrical signals with different methods as explained in the hereafter section.

2.1.3 Photonic ADCs

In his review [9], Valley defines a photonic ADC as a device with an *analog RF electronic input and a digital electronic output that uses photonics in the digitization process*. This is the definition that we will use in this section as well.

Although the first paper relating an RF signal sampling by optical sampling dates back to 1970 [10], the purpose of the paper was just to measure the duration of the optical pulses. The idea of effectively using the optical signal as a clock on an electrical circuit was first introduced by Auston with his paper on electro-optical switching in 1975 [11]. Wright et al designed, around the same period (1974), an optical quantization scheme [12].

Later on, Taylor would combine the idea of Wright and Kuizenga to design the first all photonic ADC see fig.2.3 (optical sampling and quantification) [2], [13]. From that moment on, the research focused on improving Taylor's scheme [14–23].

There are generally four classes of photonic ADCs [9]:

- **Class 1:**

Photonic assisted ADC: this first category includes circuits in which a photonic device is added to an electronic ADC to improve its performance.

The overall trend is to use optical switches made of photo-diodes to drive track and hold circuits [24], [25].

- **Class 2:**

ADCs in which sampling is achieved optically but quantification is done electrically .

The basic device for this class of ADCs is a mode-locked laser that feeds an

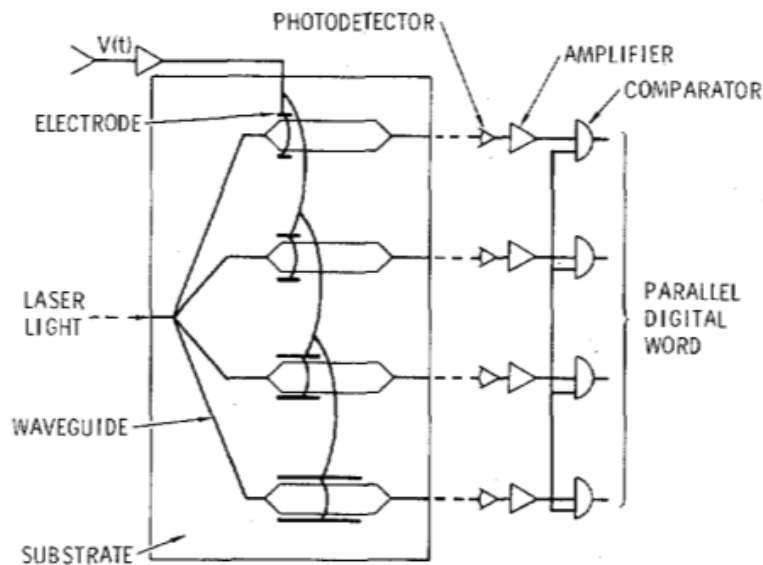


FIGURE 2.3: Schematic diagram of Taylor's optical A/D converter (taken from [2])

electro-optic modulator. The latter is driven by the input RF signal. The output of the modulator, i.e. the modulated optical pulses are then detected by a photodiode. The electrical signal at the output of the photodiode is eventually quantized through an ADC. Many researches were driven around this class of photonic ADCs since the 90's [26–34].

- **Class 3:**

ADCs in which sampling is achieved electrically but quantification is done optically.

The RF input signal is in this case sampled through a track and hold electrical circuit. The output code is then used to vary the wavelength of a semiconductor laser.

Many research works have been conducted around this theme [35–40].

- **Class 4:**

All-optical ADCs for electrical input signals: the signal is sampled and quantized optically.

The basic scheme for this class is the Taylor's one[13]. The works that have been conducted later on are just improvements of it [16],[17],[18],[19]. The system operates as follows: the RF signal drives 4 modulators that receive pulses from a laser. The modulators are of different lengths, with ratios of 2, as they represent the bits. The output of each modulator is injected into a photodetector (a high speed photodiode) then the obtained electrical signal goes through comparators to conclude on the final code.

We will now describe the technology of such photonic ADCs.

2.2 Silicon Photonics

In the social network era we are living, the internet traffic is increasing with an unprecedented pace: Cisco forecasts the global IP traffic to triple from 2016 to 2021 with an increase from 96 EB² per month to 278 EB per month, see Fig.2.4.

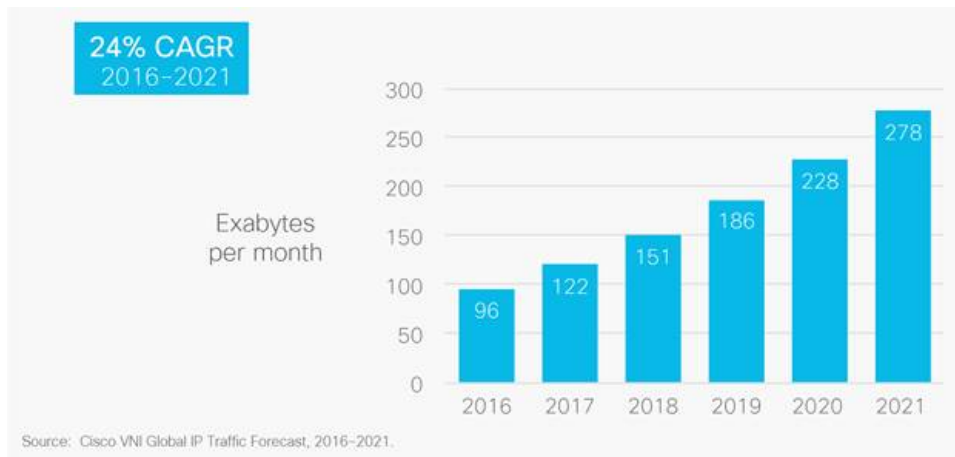


FIGURE 2.4: Cisco forecasts for global IP traffic growth

This tendency means that the bandwidth necessary to process and vehicle this data must follow the same pace. Optical technology is then proposed as a solution to counter the problem of bandwidth congestion in inter-data centers communications and again as a solution to drive the bandwidth inside the data centers.

As a matter of fact, the web giants (Google, Apple, Facebook, Amazon and Microsoft) are pushing the market towards new transceivers photonic technology to cover up their needs for data management. Some of them are already developing their own optical data centers technology in partnership with semiconductor manufacturers: Facebook and Microsoft have indeed started to work on theirs with Intel.

However, as the communications become faster and denser, the interconnect problem let alone the heat dissipation issue and the high cost of denser circuits, becomes a real bottleneck to achieve further bandwidth gains. Silicon Photonics, as a silicon-based optical technology, comes out as a new approach to the problem, offering both the cost-friendly silicon integration advantage as well as the possibility of overcoming the interconnect problem.

This tendency is even clearer when we see the forecasts for silicon photonics market that are expected to grow exponentially in the forthcoming decade, see Fig2.5.

²EB stands for ExaByte and is equal to 10^{18} Bytes

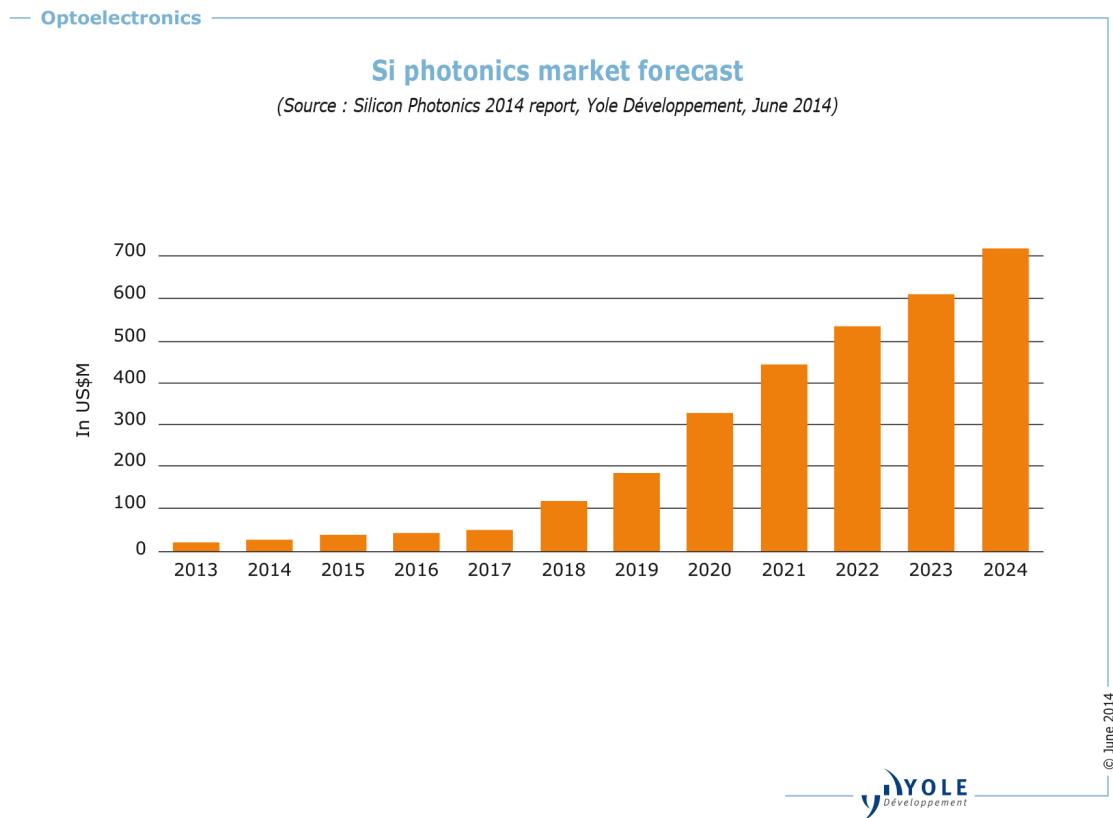


FIGURE 2.5: Silicon Photonics market for the 2013-2023 period forecast according to Yole Développement.

2.2.1 A brief history of Silicon Photonics

In the mid-eighties, many research centers launched projects around using light as a means of communication in an integrated circuit rather than electrical charge. Therefore, the choice of silicon as the main material for an optical integrated technology was obvious: not only is it inexpensive and very well studied and understood, it also provides a very easily native oxide, perfect electrical and thermal properties and a strong optical confinement on the optical wavelengths [41].

However, the silicon photonics research did not kick start right away as it was held back by two main problems [42]:

- Silicon has an indirect gap [43]. At that time, it was claimed that laser operation (negative absorption) in indirect bandgap semiconductors is nearly impossible [44]. This was backed by the belief that the small optical gain that could be achieved through phonon-aided band-to-band transitions will be largely counterpoised by free carrier absorption.

The up said means that designing light sources in a silicon based technology would be very challenging and call for nontraditional methods, unlike other

semi-conducting materials, see Fig.2.6. This is mainly why the III-V semiconductors were of choice to make lasers in the early years of silicon photonics.

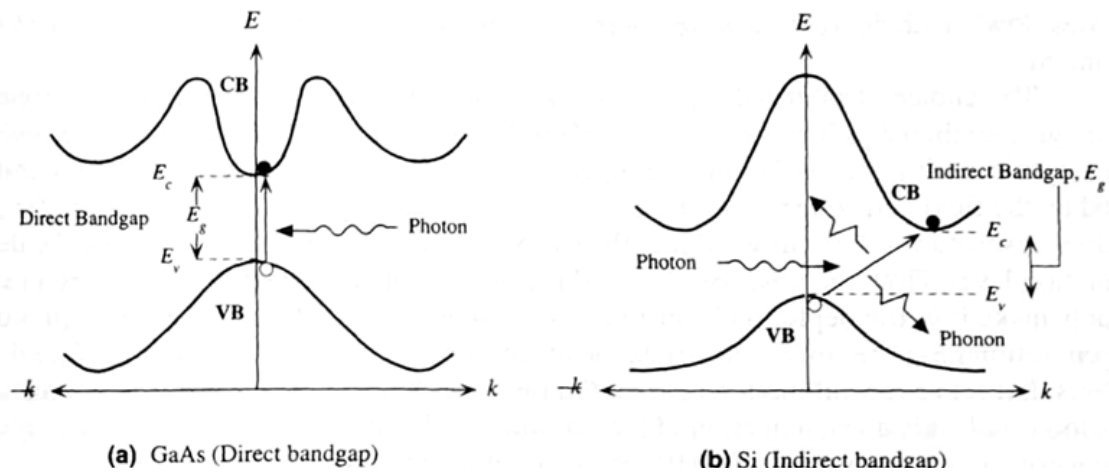


FIGURE 2.6: Silicon indirect gap versus GaAs direct gap (from [3])

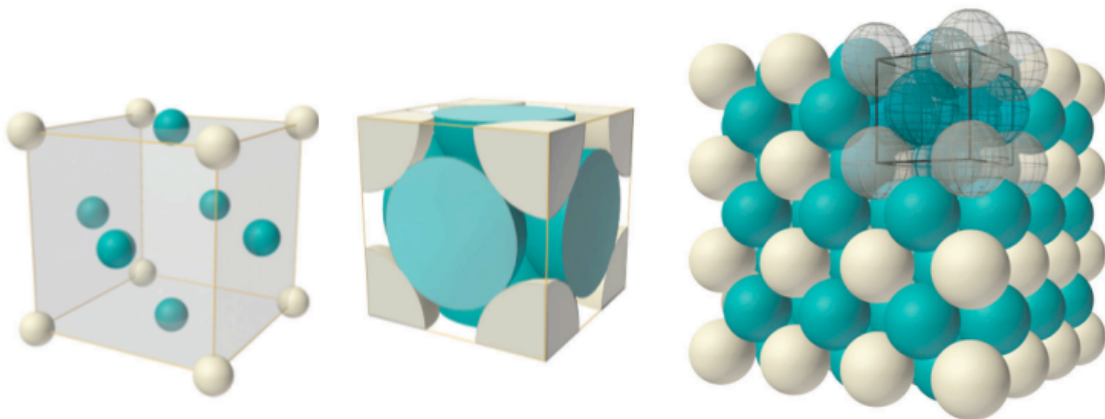


FIGURE 2.7: Silicon crystal structure: face-centered cubic

- The crystal structure of silicon being a face-centered diamond cubic, or a "two interpenetrating face-centered cubic" [45] which can be seen in Fig.2.7,³ there is no Pockels effect in silicon. This amounts to say that there is no linear electro-optical effect in silicon and thus no traditional way to design modulators such as the ones manufactured at that time in III-V materials.

Silicon emission remained for a long time the Holy Grail of Silicon Photonics, [46] [47], [48]. The interest given to this problem is not overrated, indeed resolving it would make it possible to bypass the heat dissipation problem and the limitations due to interconnect between Silicon Photonics circuits and ICs [49].

³The drawings are from: http://perso.neel.cnrs.fr/xavier.blase/OLDER/ssp_Blase.pdf

The fundamental claim that the indirect bandgap of Silicon was enough to make the laser operation impossible was quickly evicted by researches [50] [51] [52], showing that the optical gain in Silicon can overcome the recombination rate and therefore a laser operation is possible.

Research on other semi-conducting materials, namely on InGaAsP/InP, had just proven that the refractive index of a semiconductor waveguide is impacted significantly by injection of carriers (about 10^{18} per cm^3) from a forward-biased p-n junction [53]. Soref and Lorenzo used the same principle later on to prove the possibility of making a silicon-based modulator [54].

Starting from the latter publication, Silicon Photonics took off and became an independent research field in itself. The heavy investments that were drawn to Silicon Photonics contributed largely to its spawning in the nineties.

2.3 State of the art: photodetectors

The first germanium on silicon photodetector was published in 1984 by Luryi et al.[55]. But, just like photonics, the research around these photodetectors became very intensive in the late 1990's. This is mostly due to the spawn of germanium on silicon epitaxy [56], [57],[58] [59] with CVD⁴ technique that replaced the MBE⁵ that was used before.

Early germanium photodetectors were mostly vertical PN or PIN photodiodes (see 2.3.1.3) as they were designed for a surface illumination [60]. Later on, lateral PIN junction designs became the preference for designers for high speed applications especially for 1550nm devices since they require longer absorption lengths [61].

In this section, we will mainly focus on high speed germanium photodetectors as they are the ones we will use in our circuit.

2.3.1 Photodiodes

Photodiodes can be in general described as photosensitive components that exhibit an intrinsic potential barrier or a space-charge region. In order to understand the space-charge concept, we may first introduce Fermi levels in semiconductors.

⁴CVD stands for Chemical Vapor Deposition

⁵MBE stands for Molecular Beam Epitaxy

2.3.1.1 Fermi level

Consider a semiconductor material: electrons are distributed between conduction band and valence band. Fermi energy is a hypothetical energy level that stands for the maximum energy an electron has in a given material at zero Kelvin. It can also be defined as an energy level that is 50 % likely to be filled with electrons at a given temperature [62][63].

In less savvy terms, the Fermi level qualifies the electrons distribution in a semiconductor: for example the closer it is to the conduction band, the more electrons are in the conduction band compared to valence band and vice-versa. It is worth noting that the Fermi level of an intrinsic semiconductor changes with doping: it increases towards conduction band in the case of an N-doping (which increases the electrons density in the conduction band) and decreases towards valence band with a P-type doping.

2.3.1.2 Space-charge region

Now given the upsaid, say we bring together two portions of a semiconductor with opposite doping types. From the previous discussion, we know that the Fermi levels of these portions are not the same. This amounts to say that the density of electrons in the conduction band at one side (N-doping side) is higher than in the other side. The electrons then move from one side to another in order to even out their distribution, because the Fermi level of the whole device must be constant whatever the location in the device. The holes do the same, but in the opposite direction.

The movement of these electrons and holes, which is a diffusion current, is as said triggered by the difference in their density along the semiconductor.

While the electrons and holes move from one side to another, they create two adjacent opposite sign regions. This means that they create a voltage across the device, which is called the built-in voltage, see fig2.8, the electrical field that is relative to this voltage is called the intrinsic field.

The electrons and holes continue to move from one side to another until the density difference attractive force is counterpoised by the built-in voltage. The space-charge region that is then governed by the intrinsic field is a depletion region, i.e a semiconductor region that is depleted of free charge carriers [64].

2.3.1.3 Photodiode types

Photodiodes, as said earlier, are based on the space-charge region. The latter can be engineered in two different ways:

- Different dopings in the same semiconductor: this is the case that was discussed early on.

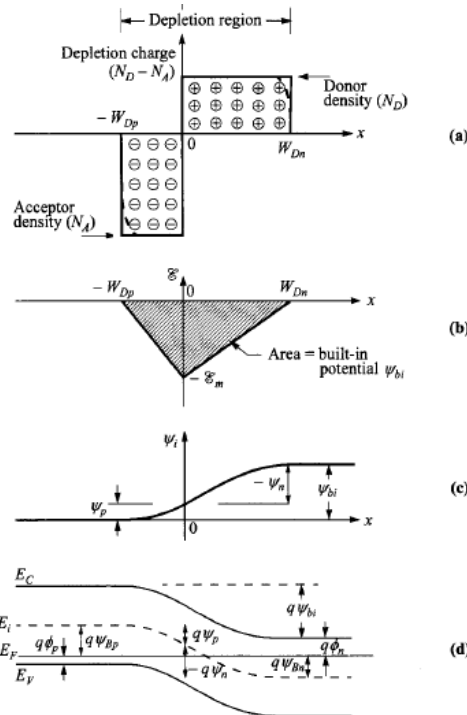


Fig. 1 Abrupt p - n junction in thermal equilibrium. (a) Space-charge distribution. Dashed lines indicate corrections to depletion approximation. (b) Electric-field distribution. (c) Potential distribution where ψ_{bi} is the built-in potential. (d) Energy-band diagram.

FIGURE 2.8: Band theory, adapted from [4]

- Different materials: by using two different materials, we have the same outcome of two different doping types since the Fermi level is generally not the same.

The second category of photodiodes, namely heterojunction photodiodes, can be engineered in two different ways that lead to two different uses of photodiodes:

- Semiconductor heterojunction photodiodes: these are made of two different semi-conducting materials.
- Metal-Semiconductor heterojunction photodiodes: in this case, the energy gap is between the semiconductor Fermi level and the metal Fermi level.

Semiconductor heterojunction photodiodes :

Semiconductor hetero-junctions have one constraint: the two semiconductors must have small lattice mismatch (see Fig.2.9), otherwise the hetero junction operation would be hampered by the dislocations due to the lattice mismatch [65].

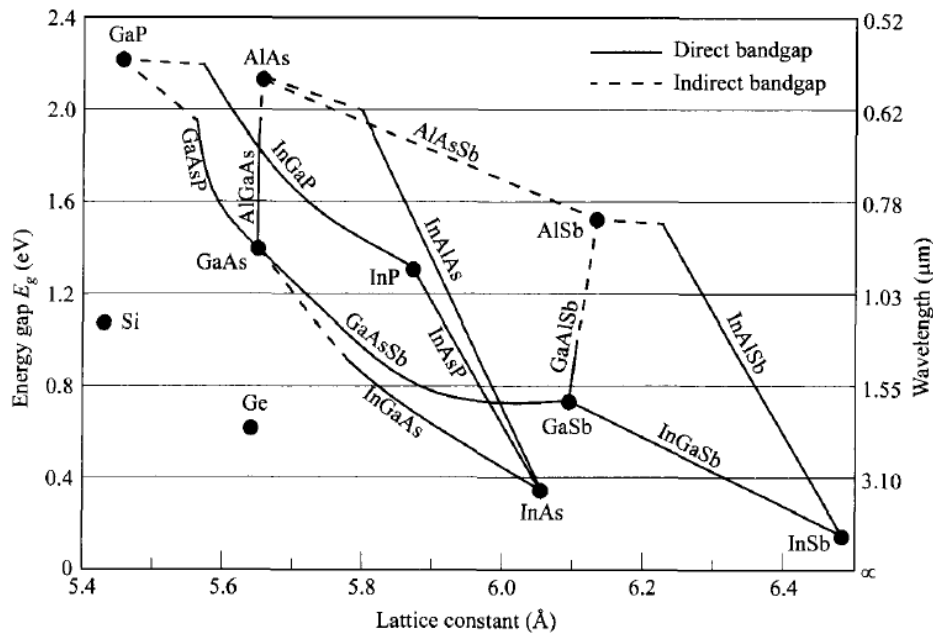


FIGURE 2.9: Lattice constant of the main semiconductor materials used in photo-detection [4]

The hetero-junction energy offset is generally emphasized through doping the two semiconducting materials. In photonics, there are many well known and studied elemental and compound heterojunction sets [66] such as : n-Si/p-SiGe, n-ZnSe/p-GaAs, p-AlGaAs/n-GaAs, p-Ge/n-GaAs, n-InGaAs/n-InP, p-InAlAs/n-InGaAs, p-GaN/n-InGaN, and p-AlGaN/n-InGaN.

Semiconductor-metal heterojunction photodiodes :

In the case of metal-semiconductor heterojunctions, the set of used materials is chosen according to the work function of the metal compared to the Fermi level of the semiconductor [67] [68]. Here again the energy gap is emphasized through doping and the most used pairs are as depicted in Fig.2.10.

Overall, in the up-said discussion, we considered the case of a PN photodiode type for the semiconductor hetero and homo-junctions cases and an MS photodiode for the metal-semiconductor case. However, this kind of photodiodes is in reality very little used in the industry of photo-detection. Indeed, since the detection area in a photodiode is the space-charge region, then, PN photodiodes offer very small responsivity (photogenerated current per injected optical power) notwithstanding the high parasitic junction capacitance that goes to decrease the bandwidth of the photodetector. One may argue that using smaller doping values would yield a wider space-charge region, but this has another side effect which is increasing the photodiode contact resistance.

The alternative photodiode structure is a PIN photodiode and an MSM photodiode:

	Ag	Al	Au	Cr	Ni	Pt	W
Φ_M (in vacuum)	4.3	4.25	4.8	4.5	4.5	5.3	4.6
n-Ge	0.54	0.48	0.59		0.49		0.48
p-Ge	0.5		0.3				
n-Si	0.78	0.72	0.8	0.61	0.61	0.9	0.67
p-Si	0.54	0.58	0.34	0.5	0.51		0.45
n-GaAs	0.88	0.8	0.9			0.84	0.8
p-GaAs	0.63		0.42				

FIGURE 2.10: Barrier heights in eV for metal-semiconductor barriers

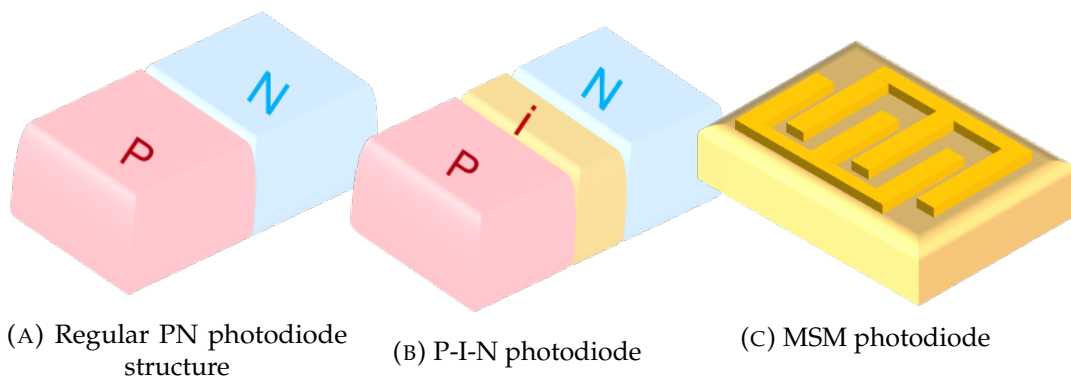


FIGURE 2.11: Plots of different photodiode structures

- P-I-N photodiode: is simply regular PN junction but with an intrinsic region in the middle, see Fig.2.11b. This addition makes the detection area bigger and acts as an extension to the space-charge region.
- MSM photodiode: is a photodiode made out of two metal-semiconductor junctions (two Schottky junctions). It has generally very high responsivity and bandwidth but features high dark currents as the metal-semiconductor barrier is generally not very high.

There is another class of photodiodes that is pretty close to PINs but serves another purpose: the avalanche photodiode. The latter is constructed exactly as a PIN but with an extra layer: a multiplication layer. The concept of an APD photodiode is to increase the velocity of photo-generated charge carriers to the point where they generate a new electron-hole pair through impact ionization [69],[70]. The newly created ones go through the same process again, so that the originally photo-generated pair creates multiple others.

This structure is widely used for sensitive detection applications [71] and exhibits great results compared to the other germanium-based silicon photonics

active component. The latter is mainly due to the fact that germanium APD structures rely mainly on their multiplication region performances, but since it is grown over silicon [72], the outcome is not hampered by lattice mismatch of excess noise in germanium as in other devices.

We will only discuss in the forthcoming state-of-the-art section the advances in high speed germanium photo-diodes because they are the closest to our application case.

2.3.1.4 State of the art

Before we dive in the state-of-the-art of the high speed germanium photo-diodes, we will first explain the measured metrics related to a photo diode performance, i.e.. dark current, responsivity and bandwidth. State-of-the-art optimization of each one of these metrics will be described and a final state-of-the-art summary will be given where performance records are detailed.

Dark current:

Dark current is the current of the photodiode in the absence of light. In a photodiode design, the aim is to reduce the dark current because having a high value of dark current implies:

- Reduced threshold of minimum detectable power for very sensitive detectors.
- More noise.
- It will be interpreted, in an eye diagram, exactly like a decrease in responsivity (less open eye diagram).

In Germanium photodiodes, the total dark current is the combination of bulk dark current and surface dark current contributions [73][74] where:

$$I_{dark} = I_{bulk} + I_{surface} = S * J_{bulk} + P * J_{surface} \quad (2.1)$$

- J_{bulk} : the bulk dark current density in A/m^2
 $J_{surface}$: the surface dark current density in A/m^2
 S : the photodiode surface
 P : the photodiode perimeter

Generally, in germanium photodetectors, the contribution of surface dark current is non negligible as it stems from the presence of dangling bonds [75], see Fig.2.12. These bonds include the ones in the edge of the germanium structure and at the interface with silicon dioxide. Indeed, unlike silicon, germanium annealing proves inefficient and several techniques are till now studied to improve its outcome [76].

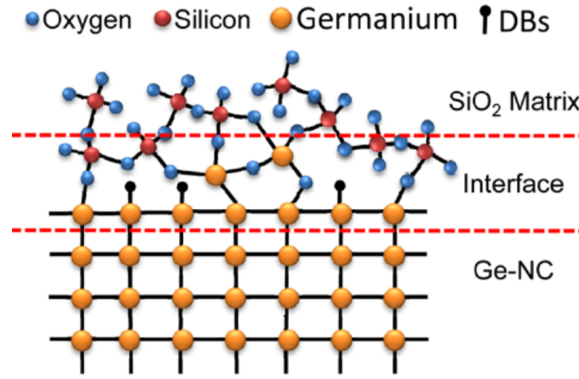


FIGURE 2.12: Germanium dangling bonds.

Bandwidth:

The bandwidth of a photodiode is determined by two factors:

- Transit time: the time that it takes the photo-generated charge carriers to cross from an electrode to another.
- RC constant: the low-pass RC filter made out of the junction capacitance C_j and the series resistance made out of the contact resistance and the bulk resistance.

The final bandwidth is given by the following equation:

$$f_{3dB} = \frac{1}{\sqrt{\frac{1}{f_{RC}^2} + \frac{1}{f_{transit}^2}}} \quad (2.2)$$

Where:

$$f_{RC} = \frac{1}{2\pi RC} \quad (2.3)$$

And

$$f_{transit} = 0,44 * \frac{v_d}{d} \quad (2.4)$$

v_d is the average drift velocity of the carriers and can be approximated by the saturation velocity v_{sat} . d is the junction depletion width.

Based on the above, there are two straightforward ways of increasing bandwidth: reducing the transit time or reducing the RC constant.

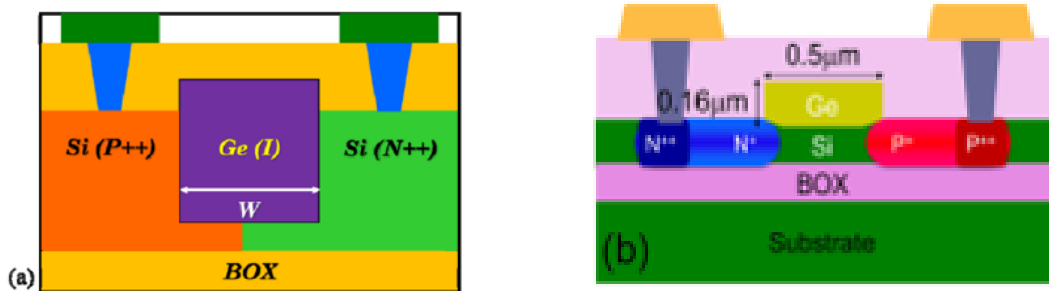
The first method, i.e. reducing transit time amounts to bringing the pGe and nGe closer to each other for full Ge photodiodes, which yields a smaller intrinsic region (less responsivity) and absorption within the doped regions (see Responsivity optimization).

For SiGeSi photodiodes [77], this reduction is limited because of:

- Optical power confinement in germanium: indeed if the germanium width becomes very small, the optical mode will expand out of germanium and this would cause a decrease in responsivity.
- Process limits: to have a proper Germanium epitaxy, the Germanium cavity should be around 300nm large for most manufacturing processes.

An alternative way to decrease transit time without impacting very much the width of the germanium cavity is to use a parallel plate junction as described in fig.2.13

By using parallel plate junctions, the transit time is reduced by strategically modifying the electrical field profile while keeping the Ge cross section relatively wide.



(A) Parallel plate Ge junction with Silicon PN (B) Parallel plate Ge junction with Silicon PIN from [77] from [74]

FIGURE 2.13: Parallel plate Ge junction photodiodes with different silicon doping configurations

This solution requires a thin Ge layer so that the electrical field is high enough over the Ge section. It also comes with a big parallel junction capacitance (the Si junction). It may also feature a « tail » response in the Eye diagram (similar to a jitter effect) since for the upper part of Ge, electrons and holes take a longer time to transit.

There are, up till now, two ways to implement this solution: either use a silicon P-I-N junction underneath the Germanium photodiode as in [78], see Fig.2.13a or use a silicon PN junction instead as in [77], see Fig.2.13a.

In the literature, there is a third method to increase bandwidth without changing the geometry of the photo-diode: inductive-gain peaking [79]. This technique was already in use in microelectronics for amplifier design [80] [81], and photo-receiver amplification [82] [83] [84].

The main idea here is to consider the RC equivalent circuit of the photo-diode and add an inductance in series with it so that the bandwidth can be improved. Design of high Q inductors in silicon photonics circuits became possible since the processing became mature and increasingly approaching the complexity of microelectronics designs. Indeed, nowadays several layers of metal are used to cover the needs of silicon photonics complex designs [85] and the use of high resistivity handle wafers for silicon on insulator is not uncommon anymore [86].

There are several ways of implementing this technique that yield improvements ranging from 40% up to many folds the original bandwidth [87].

We have summarized the different optimization techniques and their yield in the following table, see Fig.2.14.

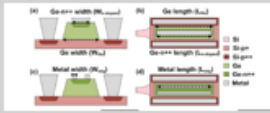
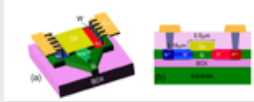
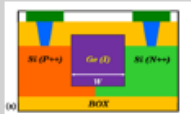
Bandwidth	Main Optimization	Design	Reference
42,5GHz(@-2V) L=20um W=8um H=380nm	Inductive Peaking.		M. M. P. Fard, G. Cowan, and O. Liboiron-Ladouceur, "Responsivity optimization of a high-speed germanium-on-silicon photodetector," Opt. Express, vol. 24, no. 24, p. 27738, Nov. 2016.
67GHz(@-2V) H=160nm Rs= 91 Ohm (-2V) Cj=6,2 Ff (-2V) 67GHz for an avg transit distance of 340nm.	Small width (0.5um Ge) + the electric field profile ==> curved The transit freq is= 45GHz. (for W=0,5um large) But: the doped regions are closer than that ==> Simulate E. (simulate the average Transit time). RsCj freq is= 282GHz ==> Not really why it is limited.		H. Chen et al., "-1 V bias 67 GHz bandwidth Si-contacted germanium waveguide p-i-n photodetector for optical links at 56 Gbps and beyond," Opt. Express, vol. 24, no. 5, p. 4622, 2016.
>50GHz(@-2V) L= 5,10,20um W= 0,3um H=260nm Rs(<<100 Ohm) Cj=0.613fF (5um long)	Small Ge (smallest so far) Small Rs (p++ and n++ dopings) Small transit time due to the fact that SiP++ and SiN++ meet under the Germanium.		[1] L. Virot et al., "Integrated waveguide PIN photodiodes exploiting lateral Si/Ge/Si heterojunction," Opt. Express, vol. 25, no. 16, pp. 19487–19496, 2017.

FIGURE 2.14: Bandwidth optimization techniques summary

Responsivity:

Responsivity is a measure of the photo-generated current versus the injected power. It does depend on many factors among which the coupling type and the length of the photo-detector.

As said earlier, the big tendency of normal light injection was used in the early years of germanium-on-silicon photodetectors out of ease and then lateral P-I-Ns took over. Here again, there are two main tendencies of light coupling: [88]

- Vertical coupling (Fig.2.15a), also called evanescent coupling [89] [90] [91]: incident light reaches out the germanium through the silicon waveguide underneath it. Basically, the germanium photodetector is just epitaxied on top of the silicon waveguide.

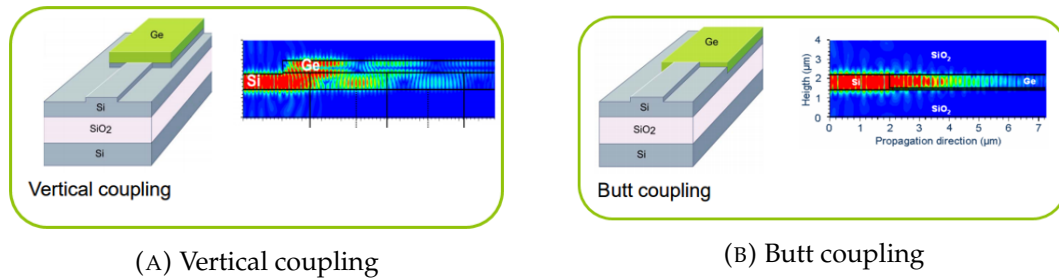


FIGURE 2.15: Ways of coupling light into a lateral germanium-on-silicon photodetector

- Butt coupling (Fig.2.15b) is basically injecting the light directly through germanium out of the waveguide [92] [93]. To achieve it, the silicon waveguide is first partially etched and a small silicon stem is left to build the germanium on top on it.

Butt coupling is more effective than vertical coupling when it comes to absorption length, i.e. the photo-detector length that is required so that 63% of the input light is absorbed. However, as said earlier, butt coupling calls for an additional manufacturing step (even more because the silicon stem must be flattened properly to build good quality germanium on it).

There are several design optimization techniques that allow for a better responsivity. The first and obvious one being using longer photodetectors (in the direction of light propagation). This rather simple optimization allows also for smaller contact resistances and, as intended, a higher responsivity. However, it comes with a bigger junction capacitance and a higher dark current.

Other techniques have been used to increase responsivity, among which using a DBR ⁶ at the end of the absorption length [94] [95]. The idea is that light crosses the photodetector twice which allows for a higher absorption without altering the electrical properties of the device. It is worth noting that this technique is very effective regardless of the delay due to propagation since it is generally very small compared to the circuit time constants.

There is also a final lever on which some publications worked to increase responsivity: reducing metal contact loss. Indeed, metal contacts, when placed above Ge directly, cause a big optical loss. There are three ways to reduce it:

- Using lateral P-I-N photodetectors rather than vertical ones [96], see Fig.2.16a.
- Using a small size off center contact above germanium [97], see Fig.2.16b.
- Using multi-finger contacts rather than large ones [95], see Fig.2.16c.

⁶DBR stands for distributed Bragg Reflector

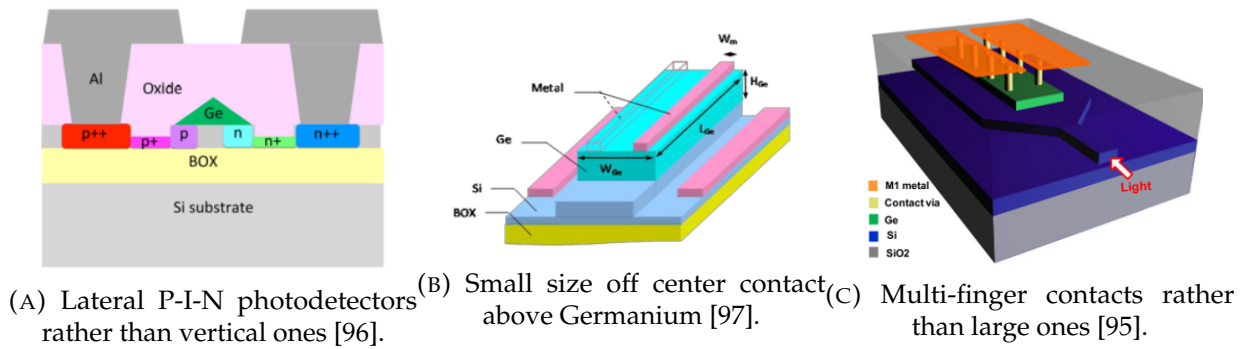


FIGURE 2.16: Plot of the different techniques used to reduce metal contact loss

Responsivity can also be optimized by reducing absorption in the doping regions. Indeed, when light hits the p-doped Ge (Boron doped Ge) and n-doped Ge (Phosphorous-doped Ge) regions, it is absorbed and generates electron-hole pairs. The latter wander randomly until they recombine: either they do outside the depletion region, in which case they do not contribute to the photocurrent, or they reach the depletion region and get swept by the electric field, which leads to an additional photocurrent, that is very random and slow (loss of responsivity).

There are two ways of reducing this loss:

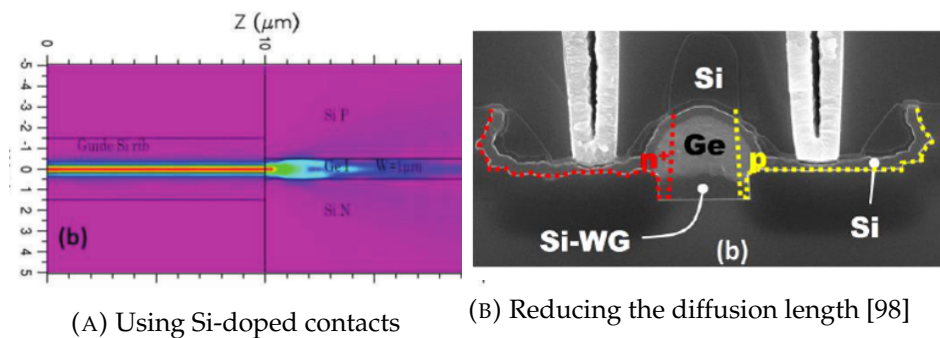


FIGURE 2.17: Plot of the different techniques used to reduce loss in the contact doping regions

- Using Si-doped contacts rather than Ge ones[99], see Fig.2.17a.
- Reducing the diffusion length (more defects or smaller GeP an GeN regions) [98], see Fig.2.17b.

The following table, see Fig.2.18, sums up the optimization techniques that it is possible to use to increase responsivity:

Responsivity	Main Optimization	Design	Reference
1,09A/W(@-2V) L=20um W=8um H=380nm	Off centered top contacts.		M. M. P. Fard, G. Cowan, and O. Liboiron-Ladouceur, "Responsivity optimization of a high-speed germanium-on-silicon photodetector," <i>Opt. Express</i> , vol. 24, no. 24, p. 27738, Nov. 2016.
0.72A/W(@-1V) L=14.2um W=0.5um H=400nm	No diffusion current (Silicon doping contacts) Contacts (lateral, no absorption).		[1] L. Virot et al., "Integrated waveguide PIN photodiodes exploiting lateral Si/Ge/Si heterojunction," <i>Opt. Express</i> , vol. 25, no. 16, pp. 19487–19496, 2017.
1,16A/W(@-1V) L= 40um W= 1um H=260nm	Silicon doping contacts (No diffusion currents + No absorption in the contacts) Long and large device.		[1] H.-J. Zang, G.-S. Kim, G.-J. Park, Y.-S. Choi, and H.-Y. Yu, "Asymmetrically contacted germanium photodiode using a metal-interlayer-semiconductor-metal structure for extremely large dark current suppression," <i>Opt. Lett.</i> , vol. 41, no. 16, pp. 3686–3689, 2016.
0,72A/W(@-1V) W=5um L=5um H=0,5um	DBR with adequate distance from the PD		Z. H. Z. Hou, "High-performance Ge-on-Si photodetector with optimized DBR location," vol. 42, no. 24, pp. 1–4, 2017.
1A/W(@-1V)	Small diffusion area		S. Lischke et al., "High bandwidth, high responsivity waveguide-coupled germanium p-i-n photodiode," <i>Opt. Express</i> , vol. 23, no. 21, p. 27213, 2015.

FIGURE 2.18: Responsivity state-of-the-art table

2.3.2 Photo-conductors

Photo-conductors have not drawn as much attention as photo-diodes. The main reason being that photo-diodes response, i.e. output current, is proportional to the optical power it receives, while this is not the case for photo-conductors.

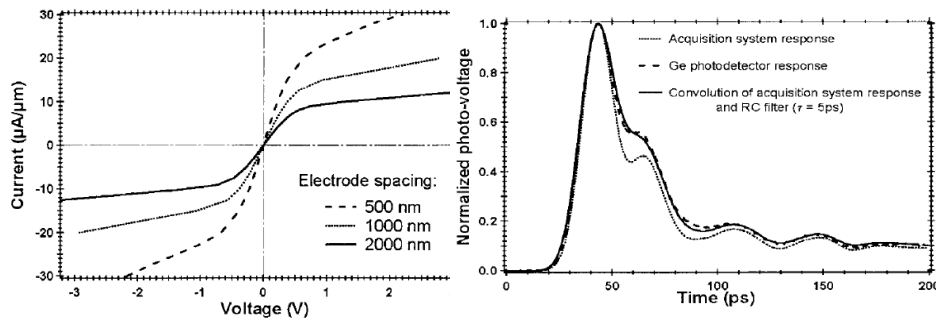
Another reason why the photo-conductors were generally discarded from research is the fact that the latter are believed to be slower than the photo-diodes, which was documented in many research works [100] [101]. Indeed, the latter claim that when a charge carrier is generated in a photo-diode, its contribution to the photo-diode ends when it reaches one of the contacts, while this is not the case for photo-conductors.

For the latter, a carrier that reaches the contact creates generally an imbalance in the overall electrical neutrality, which is right away recovered by the injection of a new carrier. This process keeps going on until the carrier recombines.

Based on the up said, photo-conductors response to pulsed light must then depend heavily on the carrier lifetimes, which in turn depends on the crystal quality.

Indeed, carrier lifetimes in germanium depend on a plethora of other parameters that make up for the crystal quality: metallic impurities, temperature and material resistivity for example [102]. For this sake, many research papers have focused on studying the way these imperfections affected the carrier lifetime, mainly in the 50's-60's, [103].

The work that has been done around photo-conductors was mainly intended to reduce the carriers lifetime by damaging or altering the crystal structure [104]. However, with the latter, came a decrease in the carriers mobility which is not very positive to the photo-conductors performance.



(A) Ohmic behavior of the MSM Ge photoconductor. (B) Pulse response of the Ge photoconductor.

FIGURE 2.19: Dark current and pulsed light response of Ge MSM photoconductor in [5].

On the other hand, there are many research works on photo-conductors that have reported no dependency of the pulsed response on the carriers' lifetime but rather on the transit time and the RC constant, just like a photodiode [5] [105] [106] [107].

Most of these research works, however, were based on a metal-semiconductor-metal structure. Therefore, although the I-V characteristic of the device shows an ohmic behavior for a range of voltages around 0V, see fig.2.19a, but the Schottky nature of metal-semiconductor contacts [5] still affects the overall response of the device and may explain, with the same logic given above, the reason why carriers lifetime does not affect the pulsed response as in fig.2.19b.

2.3.3 Conclusion

We have presented a very brief state-of-the-art of germanium photo-detectors. We have seen that a lot of work has been done around photo-diodes, mainly because they have a response that is directly proportional to the optical power that they receive and because their fall time is short compared to photo-conductors. However, photo-diodes applications are limited to telecommunication reception. Indeed, they cannot produce an electrical response that is linearly proportional to the electrical signal that is applied to them. Therefore, photo-diodes cannot be used for example in a sampling circuit, which is the reason why we have opted for photo-conductors for the achievement of this thesis purpose: the design of a sampler based on a pulsed laser.

Chapter 3

Germanium in silicon photonics

3.1 Germanium photo-conductors: presentation

Within this first section, we will present the mechanisms that rule the behavior of a germanium photo-conductor. We will also explain the design scheme of the devices that we will use along this thesis as well as the different sizing parameters that we have considered.

The main aim of this first part is to come up with a model that predicts the photo-conductors behavior under continuous wave light and under a pulsed light. We will then start with a general theoretical explanation of photo-detection and photo-conduction in germanium, then we will present the design scheme of the photo-conductors. We will eventually present the measurements that we have accomplished under continuous light and under pulsed light and an analysis of these measurements.

3.1.1 Photo-detection in germanium

In this first section, we will explain the mechanisms of photo-detection in germanium. Photo-detectors are devices that exhibit an increase in their conductivity upon exposure to a given range of wavelengths. Photo-detection in germanium happens when a photon is absorbed within a germanium atom, resulting in the release of an electron-hole pair. The photo-generated pair can then engage in the conduction process and therefore increase the overall conductivity of the germanium photo-detector.

For a photon to be absorbed by a germanium atom, its energy E_{photon} must be higher than the germanium gap, the gap being the separation between the highest energy level in the valence band and the lowest energy level in the conduction band :

$$E_{photon} = h\nu \geq E_g \quad (3.1)$$

where:

E_g : germanium energy gap
 h : Planck's constant
 ν : photon's frequency

The excess energy $E_{excess} = E - E_g$ transforms into kinetic energy.

Germanium has an indirect gap of 0.664eV (at $T = 300K$) at the L valley (in $\langle 111 \rangle$ directions), and a direct gap of 0.800eV at the Γ valley Fig.3.1.

The indirect gap of germanium matches the energy of a photon with a wavelength of [4]:

$$\lambda_{gap} = \frac{hc}{E_g} = 1872nm \quad (3.2)$$

where c is the speed of light in vacuum.

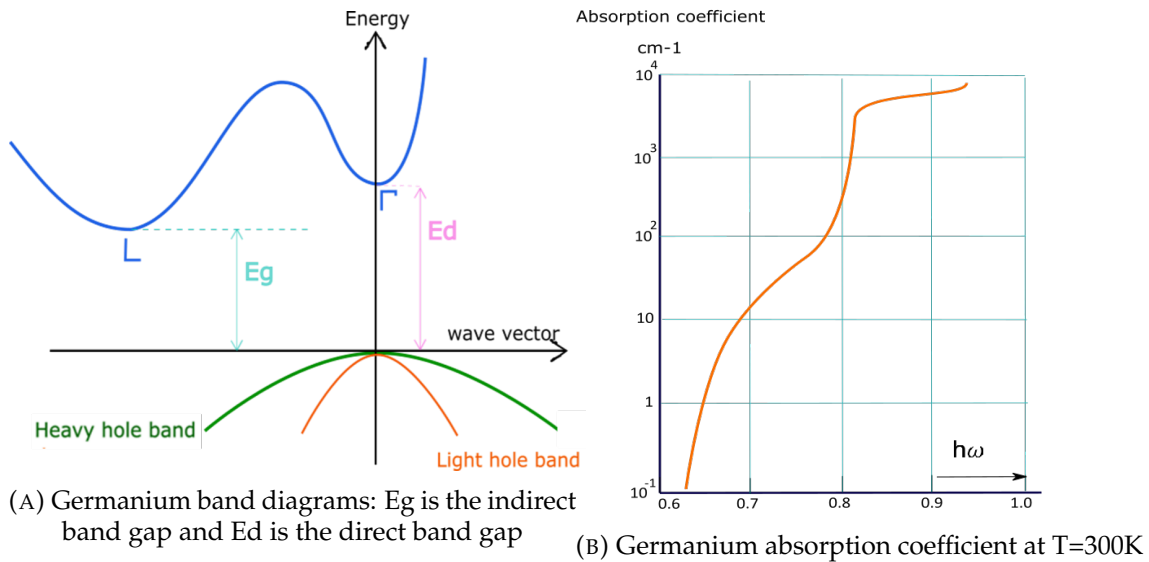


FIGURE 3.1: Plots of germanium band diagram and absorption coefficient

The direct transition matches a wavelength of $\lambda = 1554nm$.

Practically, if we consider an incident flux of photons propagating along the x direction over a germanium photo-conductor, with energies higher than the bandgap, the flux of photons in the absorbing media varies along propagation direction as follows:

$$\phi(x) = \phi_0 e^{-\alpha x} \quad (3.3)$$

where:

ϕ : the flux of photons in $m^{-2}.s^{-1}$
 ϕ_0 : the flux of photons at $x=0$ in $m^{-2}.s^{-1}$
 α : germanium absorption coefficient in m^{-1}

The up said absorption coefficient varies as a function of the light wavelength as shown in fig.3.1b.

The inverse of the absorption coefficient is the penetration depth: it stands for the distance a given photon flux has to cross inside a semiconductor before 60% of the flux is absorbed by the semiconductor. For germanium, this penetration depth is about $10\mu m$ at $\lambda = 1550nm$ [108] for direct coupling, this is why most of the subdies that we have designed have lengths around this range.

That said, the effective absorption coefficient of a given device depends heavily on the device integration scheme. Indeed, the absorption is affected by the coupling pattern as well as the device dimensions, which will be explained within the next section.

3.1.2 Technology impact on absorption in germanium

As said above, light absorption in a germanium device depends not only on the wavelength but also on two main factors:

- The Coupling type.
- The strain on germanium lattice.

These two parameters and their impact on the effective absorption length will be explained here after.

3.1.2.1 Absorption versus coupling type

There are two general ways to integrate Ge-photo-detectors into a silicon photonics circuit:

- Using a directly-coupled Ge-photo-detectors as depicted in fig.3.2a.
- Using an evanescent light coupling as in fig.3.2b.

As said above, the type of coupling has a big impact on the absorption length. For example, in [109], the direct coupling yields an absorption of light up to 95% within the first $4\mu m$, while the evanescent coupling/ direct coupling takes up to $20\mu m$ to achieve the same performance.

This is obviously due to the way light propagates across the device in both cases: in the direct coupling scenario, the germanium is hit by light in a frontal way which helps light to be absorbed within a shorter distance compared to the evanescent coupling in which light ripples between the germanium photo-detector and the silicon wave-guide underneath.

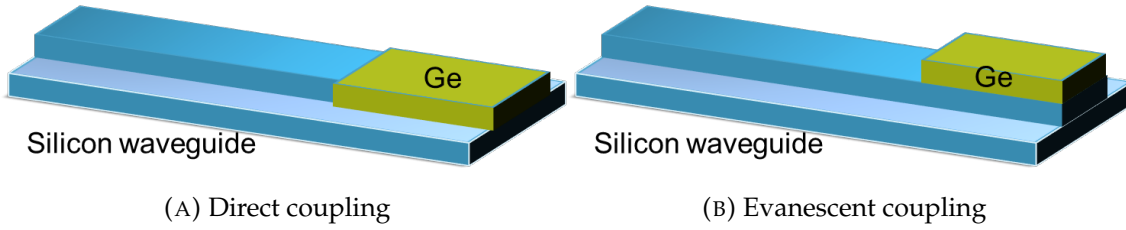


FIGURE 3.2: Plots of different coupling techniques for integrated Ge photo-detectors

Given the above, the germanium photo-detectors that we will use are all injected with light according to a direct coupling scheme in order to reduce the device length for reasons that will be explained later on.

3.1.2.2 Absorption versus lattice strain

Given the high lattice mismatch between germanium and silicon (4.2%), the epitaxy of very thin layers of Ge on Si, in the order of tens of nanometers, leads inevitably to a compressive strain in the germanium layer. This kind of strain is very detrimental to the germanium opto-electronic properties as it increases the difference between the direct and indirect gaps of germanium [110].

Practically, this strain is totally relaxed for a thickness above 200nm. However, because of the bigger thermal expansion coefficient of germanium as compared to silicon, the Ge layer develops a tensile strain when it cools down after its epitaxy on silicon. The latter strain is beneficial to germanium optoelectronic performance as it makes the direct and indirect gaps shrink, which implies a detection at longer wavelengths compared to bulk germanium. It does also imply a higher absorption coefficient at 1550nm: about $3 \times 10^3 \text{cm}^{-1}$ for bulk germanium versus approximately $4 \times 10^3 \text{cm}^{-1}$ for strained germanium. [108].

Given the up said, we can see that the absorption coefficient depends on the germanium layer height. In our case, the used technology involves a germanium height of approximately 250nm with a range of 10nm [111]. For heights of this range, the germanium layer is expected to have relaxed enough into a tensile-strained Ge on Si rather than a compressive strained Ge-on-Si, which is, as said above, beneficial to the absorption coefficient of the Ge photo-detector.

3.1.3 Photo-conductors design scheme

The photo-conductors scheme that we have used was inspired by the already existing schemes of germanium photo-diodes in STMicroelectronics PIC25G technology. The integration scheme is depicted in fig.3.3:

the germanium photo-conductor is basically made of an intrinsic germanium layer with p-type (Boron) dopings at each side. The doping regions are then connected electrically to the outside electrical pads through electrical vias.

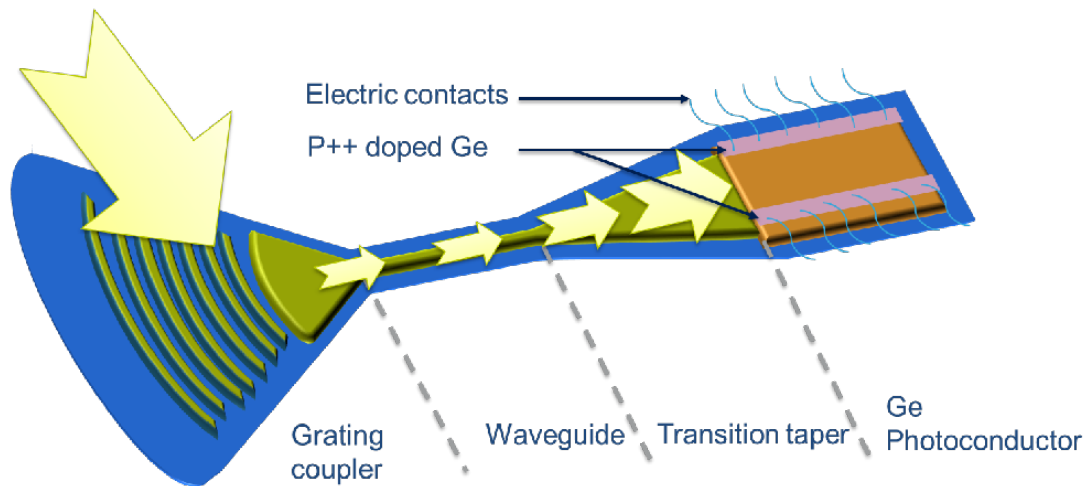


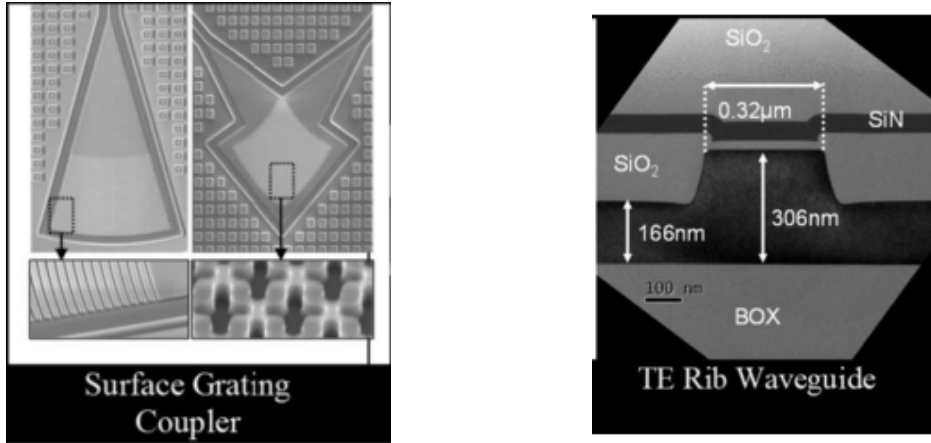
FIGURE 3.3: Photo-conductors integration scheme

The photo-conductor is injected with light through a grating coupler then through waveguides and finally tapers. The latter, also called spot-size converters, ensure the optical power that is coupled to the photo-conductor is evenly spread upon the photo-conductor section, especially when the said section is much different from the waveguide section.

In our case, we use STMicroelectronics PIC25G 1550 nm grating couplers, depicted in fig 3.4a, which exhibit an insertion loss of approximately 2.5dB. It is then injected into a 1550nm monomode waveguide (fig 3.4b).

NB: Throughout this thesis, we have designed three generations of germanium photo-conductors: generationA, generationB and generationC. GenerationA, designed in early 2014, was mainly intended to check the basic operation of the photo-conductors, therefore the subdies dimensions were chosen based on the already existing photodiodes dimensions and the number of then designed subdies was very small: four in total. It is also different than the others by the fact that it was supposed to function at 1310nm and not 1510nm.

Based on generationA measurement results, we have designed a new set of photo-conductors, this time with a bigger sweep over the dimensions and different light injection patterns in generationB. The main objective of this new set of designs was to help build a model of the photo-conductor behavior with and without light. The final set of designs, generationC, featured two types of devices: simple photo-conductors with sweeps over length and width, in order to validate the photo-conductor behavior model and photo-conductors used in photonic circuits, mainly sampling circuits.



(A) SEM of STMICROELECTRONICS PIC25G surface grating coupler (B) TEM of 1330nm STMICROELECTRONICS PIC25G monomode waveguide

FIGURE 3.4: Plots of SGC and 1330nm single mode waveguide of STMICROELECTRONICS PIC25G technology

All the generations underwent the same process flow, which means that the height of the germanium cavity, for example, is the same for all.

The detailed presentation of the dimensions of the devices in these generations is given in appendix.A.

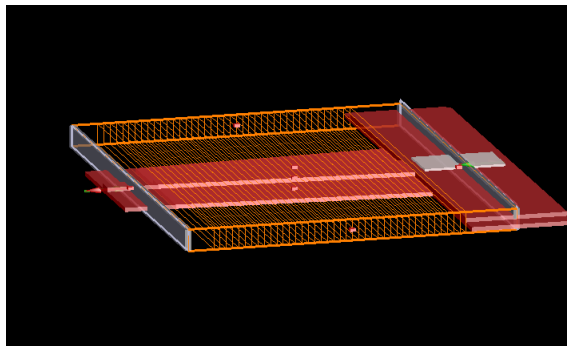
So, in the forthcoming sections, since we will mainly present the photoconductors model, designs from generationB will be the ones that we will discuss most of the time.

To choose the tapers lengths, we simulated the transmission of the TE mode versus the length of the taper for each photoconductor width as depicted in fig 3.5c. These simulations were carried on through LUMERICAL Eigenmode solver in mode-solutions simulator. In fig.3.5, plots of Lumerical Eigenmode solver views for subdie3 and subdie5 of generationB designs (see §.Appendix A). The dimensions of these subdies are the following:

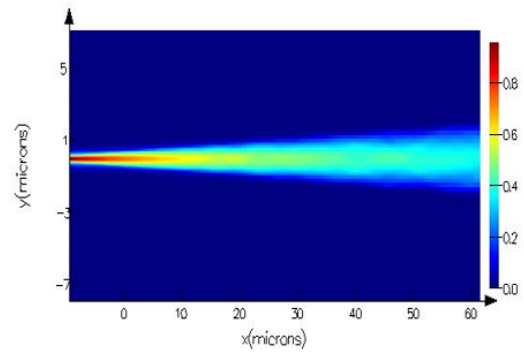
Subdie	Width(μm)	Length(μm)
Subdie3	3.3	13.07
Subdie5	5.4	13.07

To simulate the tapers, Lumerical EME solver uses a "Continuously Varying Cross-sectional Subcell" method (CVCS). This amounts to using a staircase approximation to resolve geometrical or material variations along the direction of propagation.

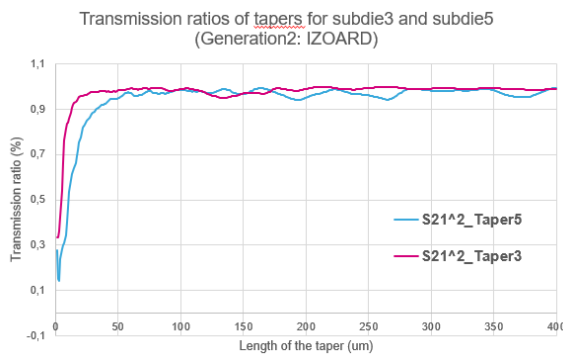
In general, the staircase approximation method is not very accurate since it involves non physical reflections. However, in the case of Lumerical, this is avoided through extensive benchmarking versus 3D finite-difference time-domain (FDTD) simulations for a wide variety of waveguide structures.



(A) Perspective view of the transmission simulation in mode-solutions(Lumerical)



(B) Cross section of light propagation through taper (Subdie 3)



(C) Transmission ratio of TE mode versus taper lengths for Subdie3 and Subdie5 (generationB)

FIGURE 3.5: Eigenmode solver simulation to optimize taper's length for Subdie3 and Subdie5

In using this method, we chose the number of cells after sweeping this number and comparing the results in order to have a good accuracy within an acceptable processing time. In Fig3.6, these simulations results are plotted and we can see that 100 cells is a good approximation, actually we can even go slightly lower.

NB: We could have used the symmetry with respect to the propagating mode in order to further reduce the simulation time.

3.1.4 Photo-conductors fabrication process

In order to fabricate Ge photo-detectors, the process flow (3.7) starts by etching partially the silicon rib waveguide. The partial etch leaves a silicon seed of approximately $90nm$. The germanium selective epitaxy into the newly formed cavity is then performed through two steps; the resulting germanium layer is approximately $250nm \pm 10nm$ high.

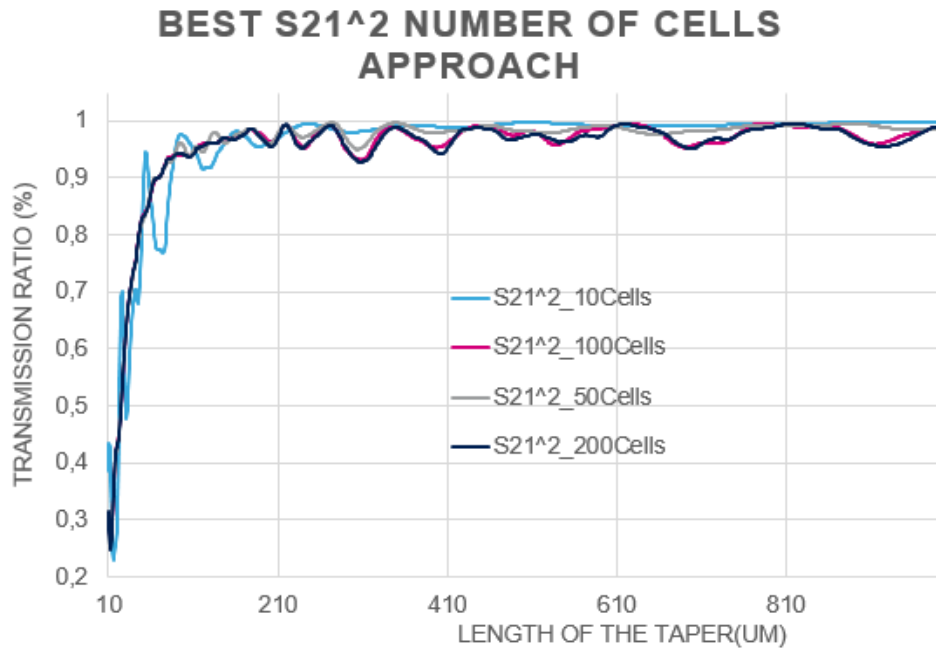


FIGURE 3.6: Effect of taper length on the transmission ratio calculations

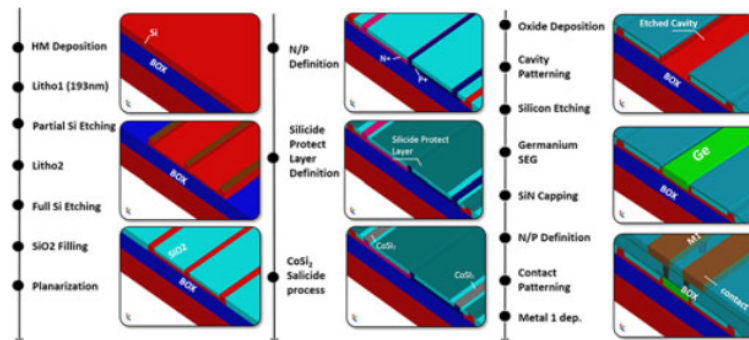


FIGURE 3.7: PIC25G photoconductors/photodiodes fabrication process flow

The germanium is finally encapsulated by a layer of SiN (etch stop layer), then the p and n dopings are performed.

3.1.5 Photo-conductors operation

Within this section, we will explain why we expect the germanium devices to have an ohmic behavior given the process and design scheme that we have presented above.

Indeed, the doping profile of the devices is that of $p - \pi - p$ diodes, i.e. $p++$ type contacts with a slight p background doping along the device. In fig.3.8, the

conduction band of $p - \pi - p$ diodes is depicted both at equilibrium and with an applied voltage .

The current equation in this case is:

$$J_p(x) = e\mu_p p(x)E(x) - eD_p dp/dx \tag{3.4}$$

Where

J_p : holes current density

D_p : holes diffusion coefficient

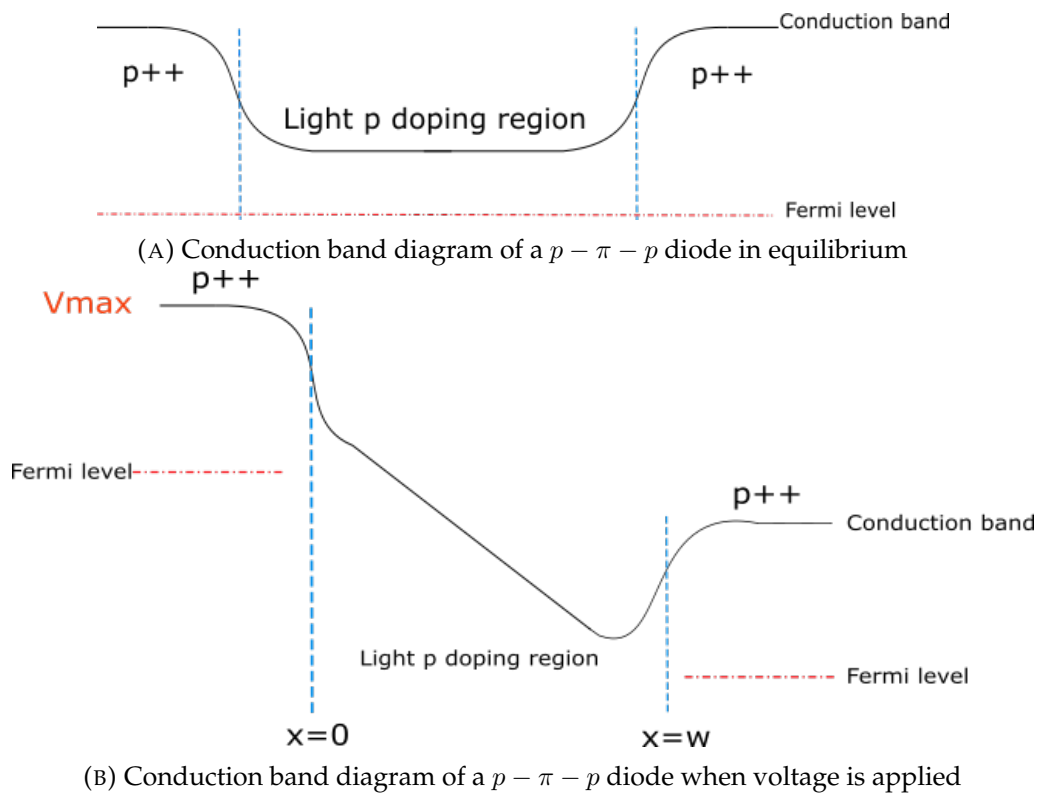


FIGURE 3.8: Plots of $p - \pi - p$ diode conduction band diagrams in equilibrium and when voltage is applied

We neglect the diffusion current contribution as the device is evenly doped but at the contacts. Poisson's equation gives:

$$dE/dx = e(p(x) - N_a)/\epsilon\epsilon_0 \tag{3.5}$$

Where: N_a is the density of the acceptor atoms in germanium. So, by combining equation 3.5 and 3.4, we obtain:

$$J_p(x) = \mu_p \epsilon \epsilon_0 E(x) dE/dx + e\mu_p N_a E(x) \tag{3.6}$$

We integrate equation 3.6:

$$xJ_p(x) = 1/2\varepsilon\varepsilon_0\mu_p(dV/dx)^2 + e\mu_pN_a(V - V_{max}) \quad (3.7)$$

At low voltages, the term $(dV/dx)^2$ is negligible. The current at the contact ($x = w$ and $V = V_a$) becomes:

$$J_p(x) = e\mu_pN_a(V - V_{max})/w \quad (3.8)$$

We can see that at these voltages, the $p - \pi - p$ diode acts as a resistor. At higher voltages, the term $(dV/dx)^2$ predominates, the current response is therefore:

$$J_p(x) = 1/2\varepsilon\varepsilon_0\mu_p(dV/dx)^2/w \quad (3.9)$$

We can here again, make the approximation that:

$$dV/dx = V/w \quad (3.10)$$

The response in this case is quadratic and we are no more in the Ohmic behavior region. The law that applies in this case is space-charge-limited-current

The threshold voltage above which the current response switches from one behavior to another is:

$$V_{tr} = 8epw^2/(9\varepsilon\varepsilon_0) \quad (3.11)$$

In our case, this threshold is about thousands of voltages (11.218×10^3 V) due to the high background doping (2.5×10^{-19} at/cm³) and the large widths of the devices (above $3.3 \mu m$). Therefore, the study that we made (ohmic behavior) is well justified.

3.2 Continuous wave measurements and model

3.2.1 I-V characterization of the photo-conductors in the dark state

For each subdie, dark current versus applied voltage was measured over a statistical sample (over 60 dies). These measurements are direct on-wafer and were carried on at CEA-Leti to take advantage of their automated measurements capabilities.

The measurement setup is presented in Fig.3.9

The Keithley sourceMeter is used to inject biasing voltage on the subdie under test with values ranging from -4V to 4V, while measuring the resulting current.

These measurements were conducted over GenerationB subdies as it features sweeps over the width and length of the subdies. The dimensions of the different subdies that will be discussed within this section are the following:

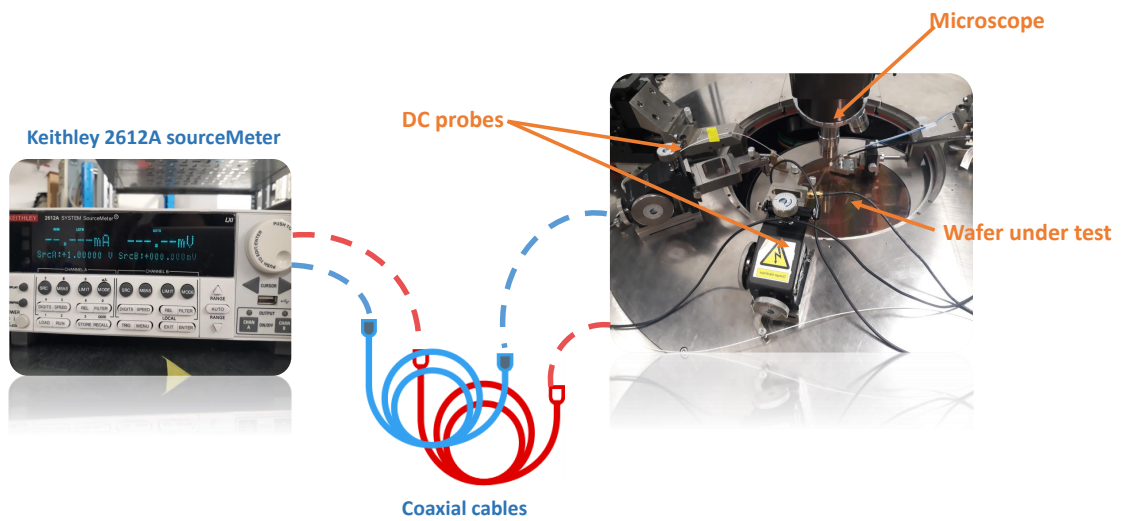


FIGURE 3.9: Dark current measurement setup at CEA-Leti

Subdie number	2	3	5	6	7	9	11	13
Width(μm)	4.68	3.3	5.4	42.68	90.68	8.36	8.36	14.36
Length(μm)	13.07	13.07	13.07	15.2	15.2	30	15	30.015

3.2.1.1 Versus voltage

In order to model the photo-conductors dark current response, two series of voltage values were applied: a first one from -4V to 4V with a 0.1V step and a second one from -100mV to 100mV with a step of 10mV.

In Fig.3.10, an example of dark current variations over voltage is presented. The subdie for which these measures were obtained is of dimensions: $w=17.36\mu\text{m}$ and $L=7\mu\text{m}$. For each voltage value, a span over the 60 samples was done and the max and min values were retained. This is how the I_{offmax} and I_{offmin} curves were plotted. The average curve was implemented by estimating the average current value at each applied voltage.

First, we observe that the good homogeneity of the results as the dispersion featured is less than 2.5% over the set of devices.

We can also see that the current curve is slightly asymmetrical between positive voltages and negative ones. This asymmetry can be explained by the probable mismatch between the contacts on both side of the photo-conductor. It could also be the result of the measurements process, i.e. fast automated measurements, and the parasitic capacitors of the device since, for every series of measurements, the side in which the current is larger is always the same for all tested subdies.

For simplicity sake, in the forthcoming analysis, we will only study the average current response for positive voltages and try to accurately model it.

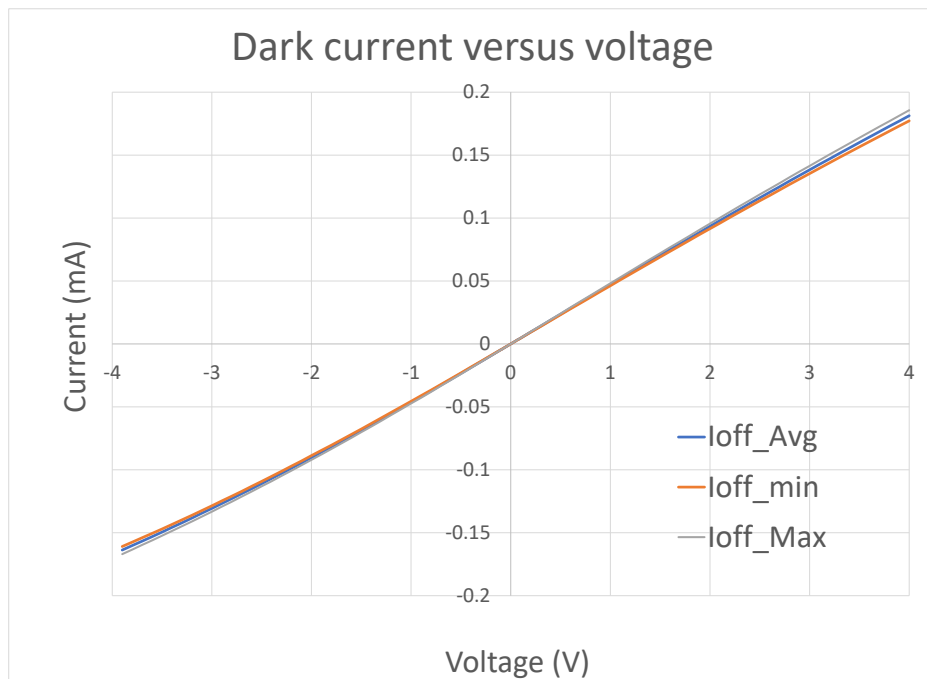
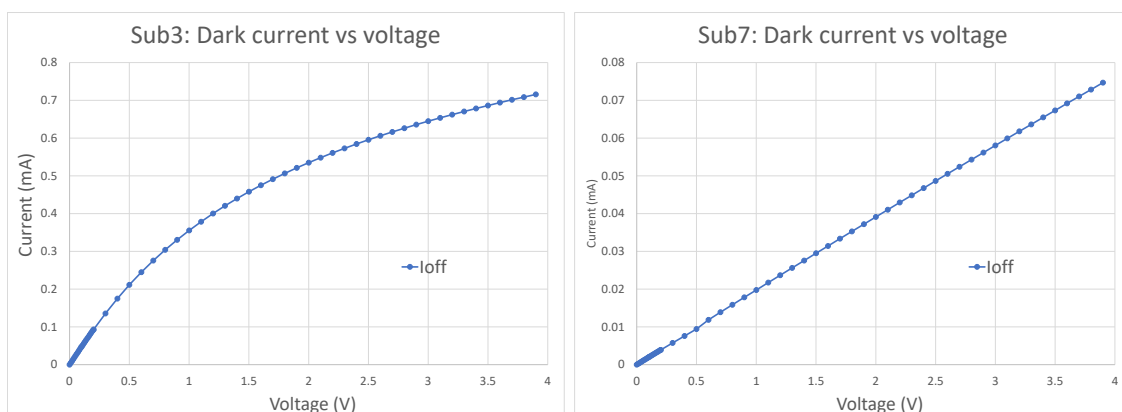


FIGURE 3.10: Dark current versus voltage for a $W=17.36\mu m \times L=7\mu m$

Now we will investigate the impact of the geometry of the structure on its current response. In fig.3.11, the dark current responses of two subdies are plotted. The first subdie dimensions are $W=3.3\mu m$ and $L=13\mu m$, and the second subdie's dimensions: $W=91\mu m$ and $L=15\mu m$. By comparing the plots, we can see that for the larger subdie, the current response is almost linear while for the other subdie, the current response saturates with increasing voltage. This effect is due to electrons and holes velocity saturation at high electrical field levels [4].



(A) Dark current versus voltage for a $3.3\mu m \times 13\mu m$ subdie (B) Dark current versus voltage for a $91\mu m \times 15\mu m$ subdie

FIGURE 3.11: Plots of dark current versus velocity saturation model for two subdies with different geometries

Indeed, if we consider a germanium photo-conductor with ohmic contacts, as presented in fig.3.11, then the current response I over voltage V can be expressed as:

$$I = eLH(nv_n + pv_p) \quad (3.12)$$

Where:

e : elementary charge

L : Length of device

H : The height of the device (germanium height)

n : The electrons density

p : The holes density

v_n : The electrons drift velocity in germanium

v_p : The holes drift velocity in germanium

In this study, for simplification purposes, we consider that the electric field is orthogonal to the contacts along the device. This approximation is a good one as the heights of the devices are very small compared to their widths, i.e. an average height of 300nm versus a minimum width of 3.3 μ m. This yields very big bending radii for the electric field lines, which is in line with an orthogonal field approximation.

We note that the very small height of the devices means also that the p++ doping is distributed evenly along the contact height, which is also in compliance with the orthogonal field approximation.

So, we can consider that:

$$E = V/w \quad (3.13)$$

where w is the width of the device. And

$$v_x = \mu_x E \quad (3.14)$$

Therefore:

$$I = eLH(n\mu_n + p\mu_p)V/w \quad (3.15)$$

Where:

μ_n : electrons mobility

μ_p : holes mobility

The electrical neutrality translates into: $n=p$, therefore:

$$I = eLnH(\mu_n + \mu_p)V/w \quad (3.16)$$

In germanium, the mobility changes with the electrical field according to the following model [112]:

$$\mu(E) = \frac{\mu_0}{(1 + (\frac{\mu_0 \cdot E}{v_{sat}})^\beta)^{1/\beta}} \quad (3.17)$$

Where:

- μ_0 : mobility at very low electric field values
- v_{sat} : saturation velocity
- β : fitting parameter

This model was applied to the measured I-V characteristic as follows:

- First we start by the current response at low voltage: we determine the coefficient:

$$A = \frac{eLnH}{w} \quad (3.18)$$

For that, considering the measured quantities I and V, we have:

$$A = \frac{I}{V}(\mu_n + \mu_p) \quad (3.19)$$

- We then calculate the velocity saturation current model at higher voltages: -

$$I = A(\mu_n + \mu_p)V \quad (3.20)$$

Where:

$$\mu_x = \frac{\mu_{x0}}{(1 + (\frac{\mu_{x0} \cdot V}{v_{sat}})^\beta)^{1/\beta}} \quad (3.21)$$

The fitting parameters that were used for the model are [112]:

β_n	β_p
2.4	1.1

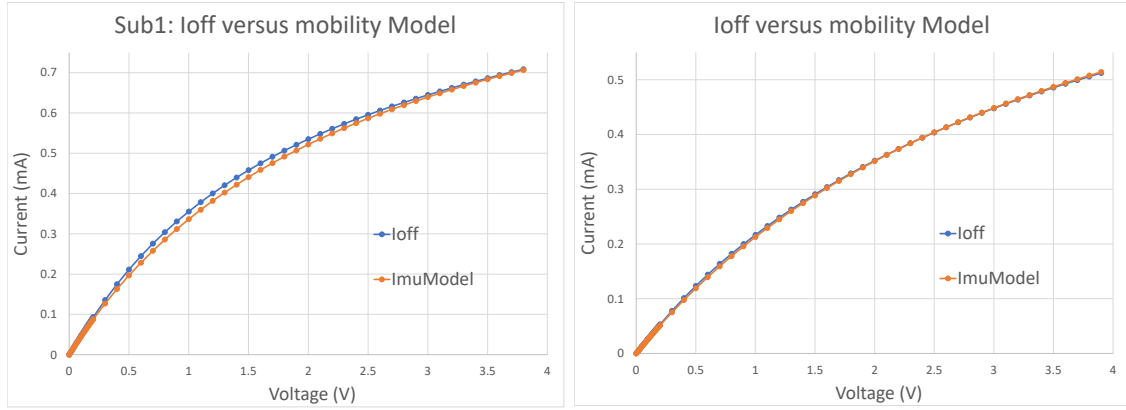
We considered the following values:

$\mu_n(cm^2/V/s)$	$\mu_p(cm^2/V/s)$
3900	1900

The fitting parameters values are close to the ones cited in [113].

Note that the experiments of Sabnis and Clemens [114] have clearly demonstrated that the saturation velocity is almost independent of the doping concentration. We base our model on this assumption.

This model was applied to the I-V response of the devices. In Fig.3.12, the photo-currents of two devices with different geometries are plotted versus the velocity saturation model.



(A) Measured dark current versus velocity saturation model for a $3.3\mu m \times 13\mu m$ subdie (B) Measured dark current versus velocity saturation model for a $5.4\mu m \times 13\mu m$ subdie

FIGURE 3.12: Plots of measured dark current versus velocity saturation model for two subdies with different geometries

3.2.1.2 Versus geometry

We ran another statistical test in order to see if there is any correlation between the subdies dimensions and their dark square resistance.

In principle, the square dark resistance should not depend in theory on the aspect ratio of the device. Indeed, starting from Eq.3.16, we can conclude that the square dark resistance is:

$$R_{square} = \frac{1}{eH(p * \mu_p + n * \mu_n)} \quad (3.22)$$

Here, we consider this ratio through the proportion in between the largest and the smallest lateral dimensions i.e. maxdimension/minidimension. In most cases, the length of the device (ranging from 13 to 30 μm) represents the largest dimension while the width (ranging from 3.3 to 90 μm) is the smallest. These values give dimension ratios ranging from 1.5 up to 5.5.

In Fig.3.13, we plot the average square dark resistance versus this aspect ratio. The resistance was evaluated first for the same voltage value, then for the same average electrical field (i.e. for a constant “bias voltage” / “width” ratio). The test was conducted for voltage and electrical field values that fall within the ohmic behavior region for all the subdies, i.e. before the velocity saturation occurs.

Our best guess is that it is related to the dislocations [115]. Indeed, because of the mismatch lattice between germanium and silicon, silicon having the smallest lattice, germanium relaxes its strain after epitaxy through dislocations, mainly threading dislocations.

The latter increase dark current in photo-detectors because they introduce new

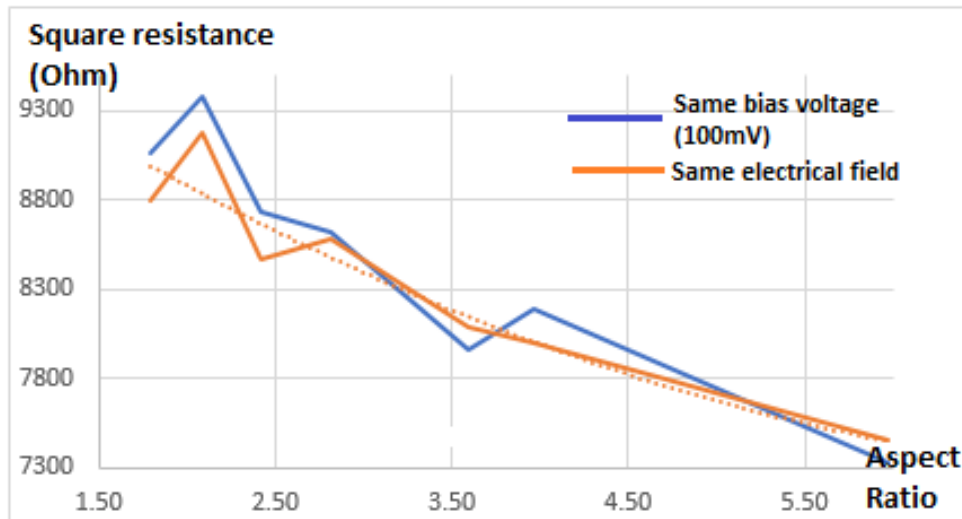


FIGURE 3.13: Square resistance dependency on aspect ratio.

energy levels.

For the low aspect ratio devices, the strain is big on both dimensions w and L since they are not very different. Therefore, no dimension is more likely to give rise to threading dislocations than the other. However, in the case of high aspect ratio devices, the big dimension features a bigger strain than the small dimension, this difference leads to more threading dislocations over the smaller dimension. Finally, the more dislocations, the higher the dark current, and therefore the lower the square resistance.

3.2.2 I-V characterization of the photoconductors under continuous illumination

The aim of the "ON measurements" is to quantify and model the current response of the devices when a continuous wave light at 1550nm and a DC voltage are applied to them.

The ON measurements were conducted in an on-wafer automated fashion. The coupling of the light is checked each time through a first measurement ON current over a span of x and y adjustments.

We were able to perform measurements at 1310nm and 1550nm. The light is guided up to the grating coupler using a standard SMF28 single mode fiber with polarization maintenance.

These measurements were also carried on at CEA-Leti.

The subdies that will be measured have different light injection patterns. Indeed, some of the subdies feature a double injection of light, i.e. light is coupled to the chip through a Polarization Splitting Grating Coupler (PSGC) as in fig.3.15b,

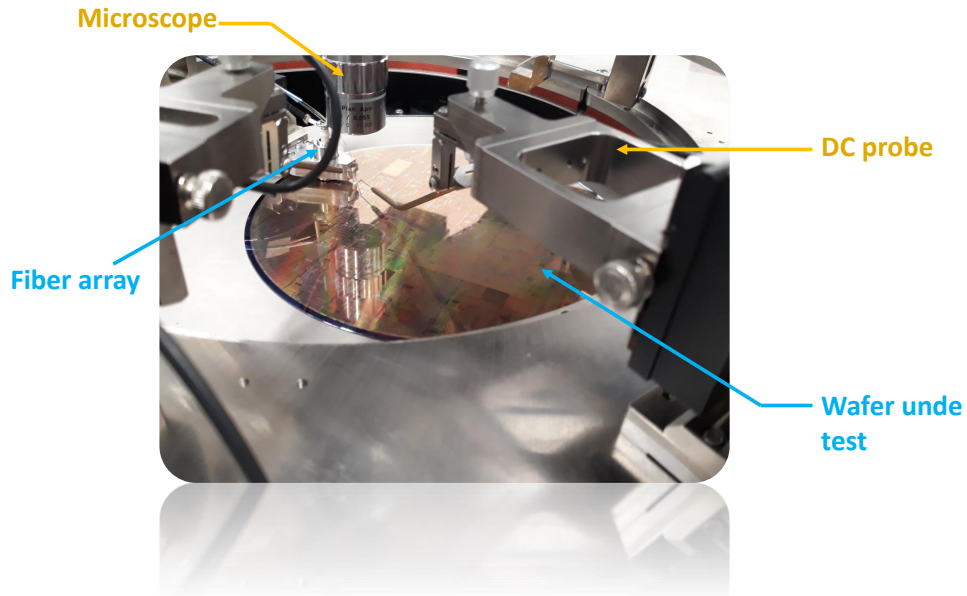


FIGURE 3.14: ON measurements test bench

each one of the resulting light beams is then coupled to a waveguide then a taper and finally injected into the Germanium cavity. The two light injection modes are presented in fig.3.15.

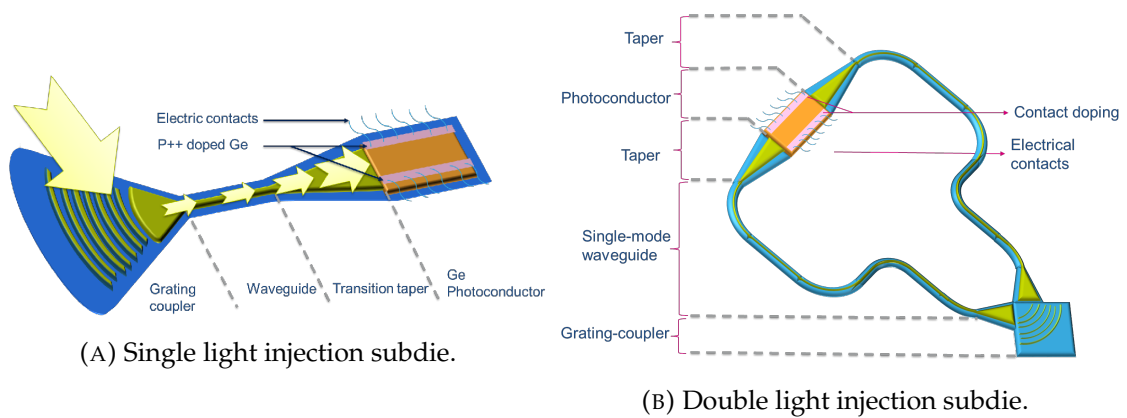


FIGURE 3.15: Plots of the different light injection patterns.

Within the following subsection, the subdies that will be measured are again generationB subdies and have the following dimensions and light injection mode.

Subdie Number	3	5	6	7	9	11	13
Width(μm)	3.3	5.4	42.68	90.68	8.36	8.36	14.36
Length(μm)	13.07	13.07	15.2	15.2	30	15	30.015
Light injection	Double	Double	Single	Single	Single	Single	Single

3.2.2.1 Versus voltage

We first ran a continuous wave test at $1550nm$ with a $13dBm$ light power and with a varying voltage. Since these measurements are mainly used to model the photo-conductor behavior and try to extrapolate on its behavior with pulsed light, we chose to run these tests at the maximal power the bench machine could deliver, i.e. $13dBm$. We can then estimate that $10dBm$ was reaching the Ge photodetector (3dB loss mainly due to the grating coupler).

As can be seen in fig.3.16, the current response is linear at low voltages and "saturates" over a given voltage. In order to better determine whether the saturation effect is due to the velocity saturation or not, we apply the model defined previously in Eq.3.17.

Here again, as in section § 3.2.1.1, we apply the following steps to model velocity saturation:

- As previously explained in the dark current measurements, we determine the coefficient:

$$A = \frac{eLnH}{w} \quad (3.23)$$

Where:

$$A = \frac{I}{V}(\mu_n + \mu_p) \quad (3.24)$$

-

The fitting parameters that were used for the model are the same than those used for the OFF current model in section 3.2.1.1:

$$\beta_n = 2.4 \quad (3.25)$$

And:

$$\beta_p = 1.1 \quad (3.26)$$

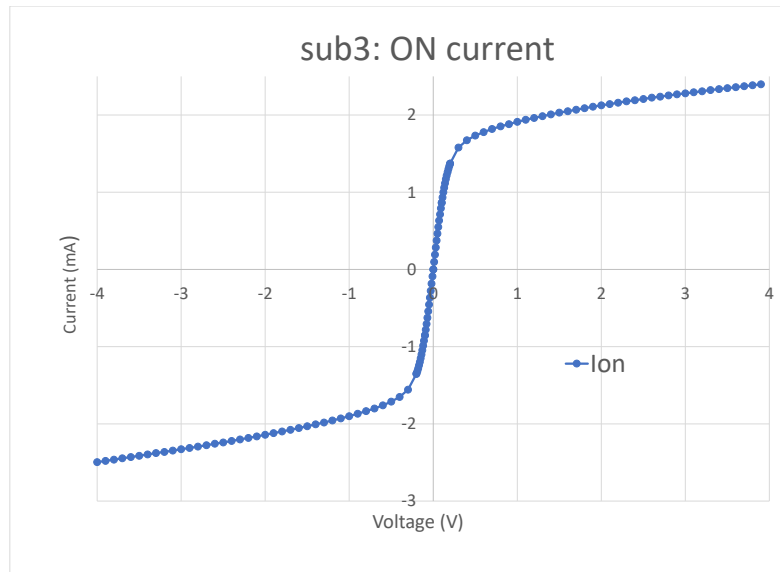
In fig. 3.17, the ON current versus the velocity saturation model is plotted.

We can clearly see that the velocity saturation model does not fit the ON current, which means that there is another limiting factor.

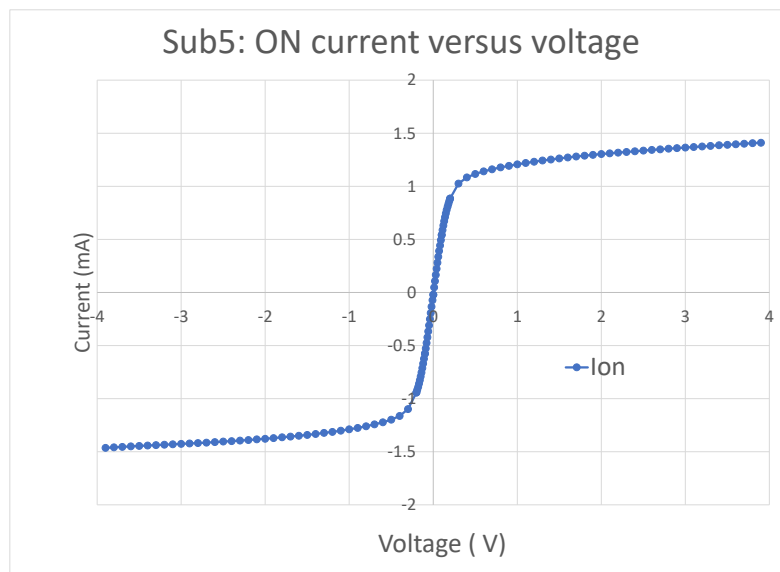
One possible scenario would be that, beyond a given voltage, the number of photo-generated electrons and holes per second is exactly equal to the number of electrons and holes swept through drift current per second, which would explain the fact that the current kind of saturates at higher voltages.

In order to validate this scenario, we implement a new phenomenological model, similar to the velocity saturation one, but this time based on conductance saturation.

$$I = \left(\frac{G_{0n}}{\left(1 + \left(\frac{G_{0n}V}{I_{max}}\right)^{\gamma_n}\right)^{1/\gamma_n}} + \frac{G_{0p}}{\left(1 + \left(\frac{G_{0p}V}{I_{max}}\right)^{\gamma_p}\right)^{1/\gamma_p}} \right) V \quad (3.27)$$



(A) Sub3: ON current versus applied voltage ($w = 3.3\mu\text{m}$ and $L = 13.07\mu\text{m}$)



(B) Sub5: ON current versus applied voltage ($w = 5.4\mu\text{m}$ and $L = 13.07\mu\text{m}$)

FIGURE 3.16: Plots of ON current versus voltage for two subdies with different geometries

Where:

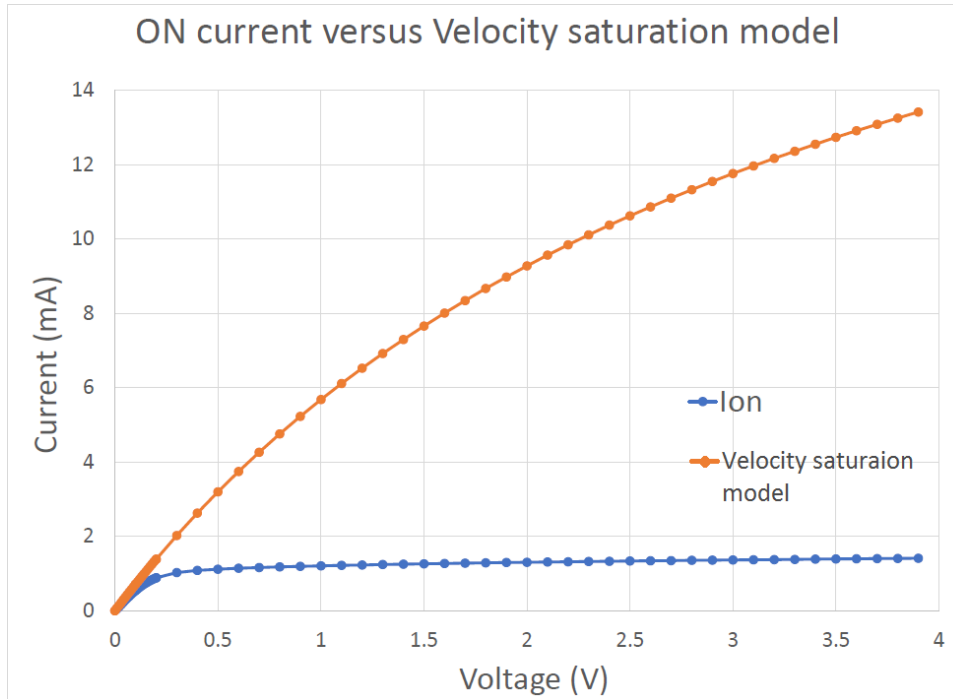


FIGURE 3.17: Measured ON current versus velocity saturation model for a $5.4\mu\text{m} \times 13\mu\text{m}$ subdie

G_{0n} : the low voltage electrons conductance

G_{0p} : the low voltage holes conductance

I_{max} : the saturation current

γ_n : the electrons current fitting parameter

γ_p : the holes current fitting parameter

Note that in the up said model, we considered the electrons and holes conductance separately because they have different values of mobility, which implies that their contributions to the current may saturate at different paces.

The term of conductance G_{0n} must also take into consideration the velocity saturation as in equation 3.17.

Therefore:

$$G_{0x} = \frac{en\mu_x}{w} = A_x\mu_x \quad (3.28)$$

Where: μ_x is the velocity saturation model mobility.

So that:

$$I = \left(\frac{A_n\mu_n}{\left(1 + \left(\frac{A_n\mu_n V}{I_{max}}\right)^{\gamma_n}\right)^{1/\gamma_n}} + \frac{A_p\mu_p}{\left(1 + \left(\frac{A_p\mu_p V}{I_{max}}\right)^{\gamma_p}\right)^{1/\gamma_p}} \right) V \quad (3.29)$$

This model versus the ON current were plotted in fig. 3.18 The fitting parameters that were used in this case are:

- $\gamma_n = 0.9$

- $\gamma_p = 3$
- $I_{max} = 1.7mA$

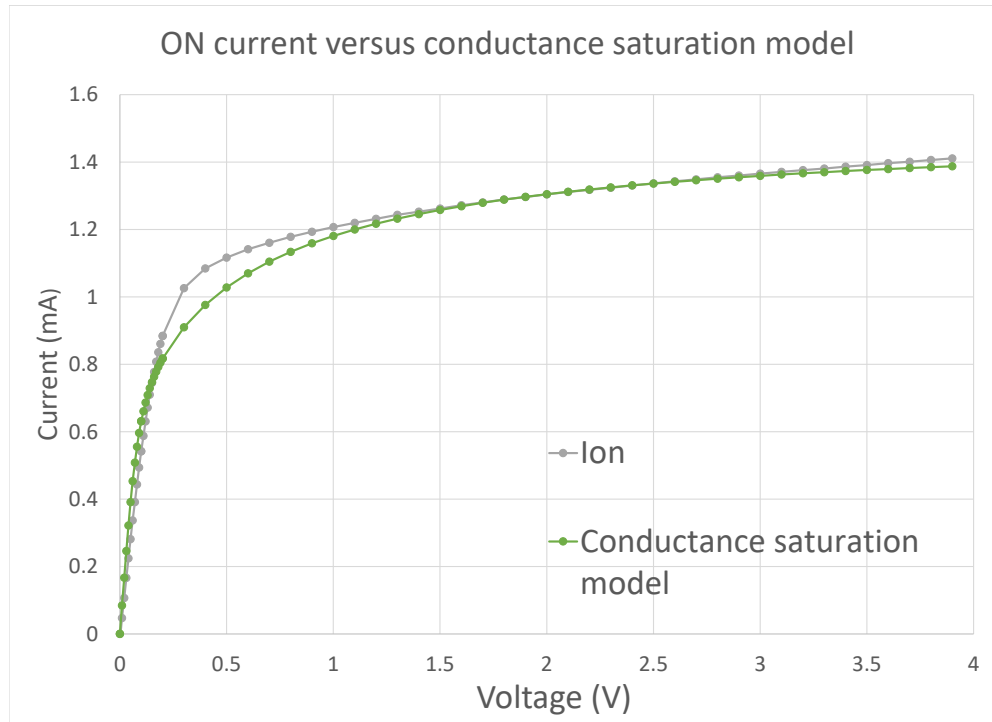


FIGURE 3.18: ON current versus conductance saturation model for a $5.4\mu m \times 13\mu m$ subdie

The phenomenological conductance saturation model fits to a good extent the ON current, so we can consider it for the total photo-conductor behavior model.

3.2.2.2 Electrical equivalent model of the photo-detector

Based on the analysis that we have conducted so far on the photo-conductors behavior with and without light, we can now build a model to be used later on to approach the photo-conductor behavior when lit with a pulsed laser. The previous analysis suggests a model made of two conductors in series, or two resistors in parallel, one being the OFF equivalent resistor and the second one being a power variable resistor that conveys the loss of resistance in presence of light. The approximation we made with resistors is fully justified for voltages below the mobility saturation voltage and for current values that are below the saturation current.

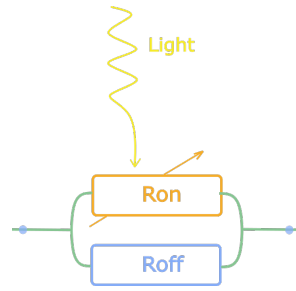


FIGURE 3.19: Electrical model of the photo-conductor

In this new model, and along the forthcoming sections, we will consider the following annotations:

I_{OFF} : the current when no light is applied.

I_{ON} : the current when light is applied.

I_{photo} : the photo-generated current, i.e. the ON current minus the OFF current.

3.2.2.3 Versus optical power

The aim of this section is to analyze the photo-generated current dependency upon the injected power at $\lambda = 1550nm$. The test bench is the same as in the previous section, the current is probed at a voltage of 50mV: low enough so that the velocity saturation effect does not occur yet.

In fig. 3.20, the photo-generated current is plotted versus the power that is really injected into the subdie, i.e. the power injected into the chip minus grating couplers loss.

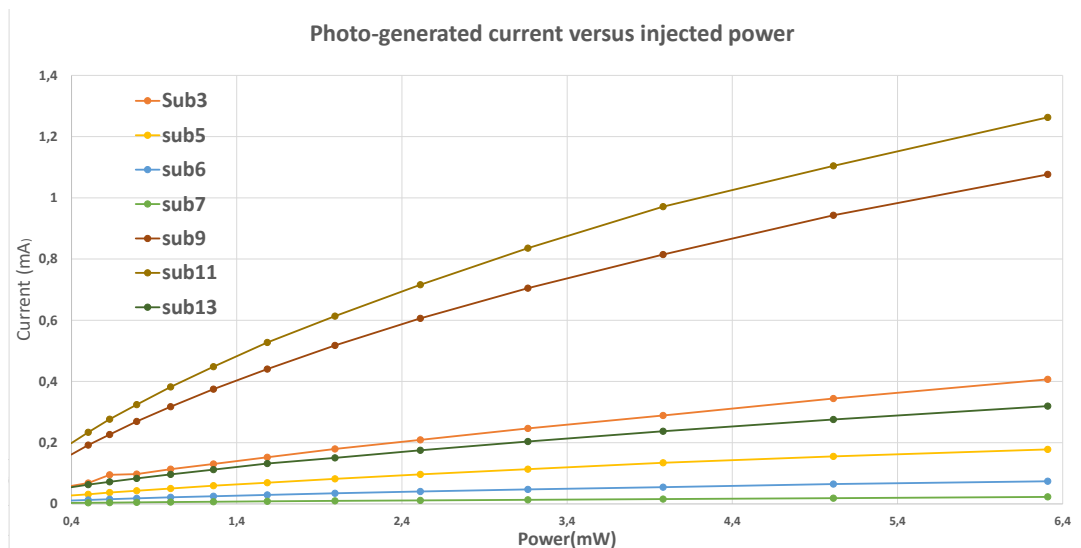


FIGURE 3.20: Photo-generated current versus the injected power for different subdie geometries

Here is a reminder of the dimensions of the subdies measured in fig. 3.20:

Subdie number	3	5	6	7	9	11	13
Width(μm)	3.3	5.4	42.68	90.68	8.36	8.36	14.36
Length(μm)	13.07	13.07	15.2	15.2	30	15	30.015
Power injection	Double	Double	Single	Single	Single	Single	Single

We can see that the current dependency upon power is not linear, i.e. the number of electron-hole pairs that engage in conduction is not proportional to the number of injected photons. This can be explained through photo-conductors continuity equations; indeed, say Δn is the photo-generated electrons density, if diffusion processes were neglected, Δn changes over time as follows:

$$\frac{d\Delta n}{dt} = G - \frac{\Delta n}{\tau_n} \quad (3.30)$$

where:

- n : electrons density
- Δn : photo-generated electrons density
- G : electrons generation rate
- τ_n : electron's time constant

τ_n stands for the average time the electron spends before it recombines with a hole. The latter depends mainly on the density of holes and electrons that are available for recombination, hence:

$$\frac{\Delta n}{\tau_n} = C(np - n_0p_0) \quad (3.31)$$

where:

- C : the recombination rate
- n_0 : electrons density before exposure to light
- p_0 : holes density before exposure to light
- n : electrons density after exposure to light
- p : holes density after exposure to light

Therefore:

$$\frac{d\Delta n}{dt} = G - C((n_0 + \Delta n)(p_0 + \Delta p) - n_0p_0) \quad (3.32)$$

Since the number of photo-generated electrons is equal to the number of photo-generated holes as they are created in pairs:

$$\frac{d\Delta n}{dt} = G - C((n_0 + p_0)\Delta n + \Delta n^2) \quad (3.33)$$

So, at equilibrium, we have:

$$G = C((n_0 + p_0)\Delta n + \Delta n^2) \quad (3.34)$$

Now there are two cases with reference to the injected power level:

- Case 1: low optical power injected (low current density): $\Delta n \ll n_0$ and $\Delta p \ll p_0$.

In this case, the density of photo-generated carriers is negligible compared to the density of carriers before exposure to light, hence we can consider that:

$$G = C((n_0 + p_0)\Delta n) \quad (3.35)$$

- Case 2: high optical power injected (high current density): $\Delta n \gg n_0$ and $\Delta p \gg p_0$.

In this case, we consider that n_0 is negligible compared to Δn , hence:

$$G = C\Delta n^2 \quad (3.36)$$

The generation rate G being directly proportional to the injected power P (in all cases):

$$G = KP \quad (3.37)$$

Where: K is a proportionality coefficient.

- Case 1: low power injected:

$$\Delta n = \frac{KP}{C(n_0 + p_0)} \quad (3.38)$$

In this case, the number of photo-generated carriers, and therefore the photo-generated current, is directly proportional to the injected power.

- Case 2: high power injected:

$$\Delta n = \sqrt{\frac{KP}{C}} \quad (3.39)$$

In this case, the photo-generated current dependency on the power is sub-linear and follows a square root function.

In fig. 3.21, the photo-generated current of two subdies is plotted versus injected power. We used a logarithmic scale both in the x and y axes in order to better highlight the linear and sub-linear modes and we virtually added a point at 0.0001V which represents the current at approximately 0V. We can see that the dependency is only sub-linear for all the plotted points (the first one is not taken into consideration) which may be due to the fact that the linear mode is achieved at very low values of injected power.

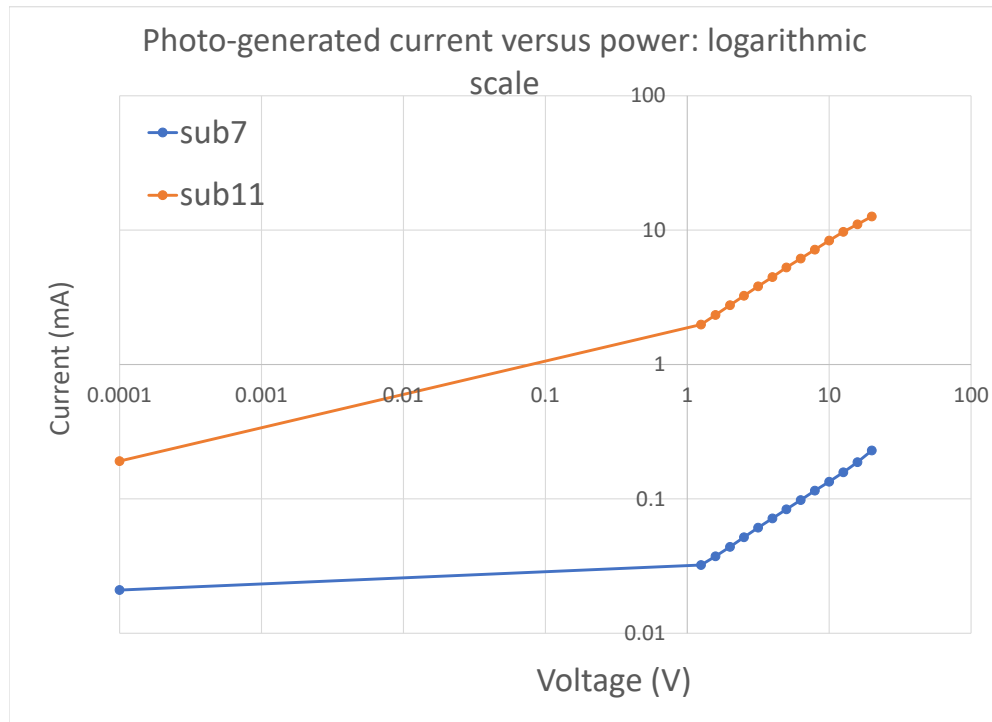


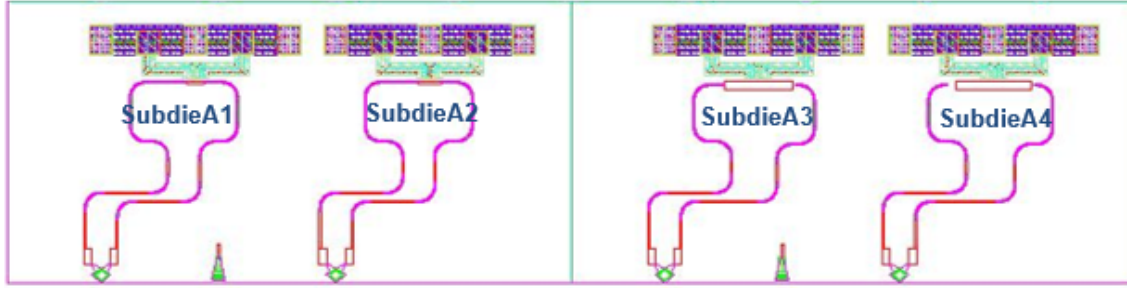
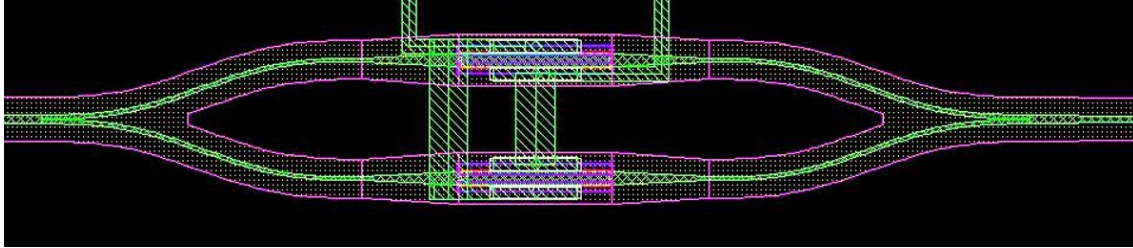
FIGURE 3.21: Photo-generated current versus the injected optical power with logarithmic scale for Subdie7 and Subdie11 at 50mV DC bias

The sub-linear mode in this case is not perfectly a square root mode: we have rather a power of 0.6 to 0.7 instead of 0.5. Indeed, this can be explained by the fact that the measurements match the transition mode between the linear and sub-linear model.

To better understand and illustrate this effect, we must run tests at higher power values or at higher absorption coefficients. Since the test bench that we use can only deliver a maximal power of 13dBm, we choose to run tests at $\lambda = 1310nm$, where the absorption coefficient of germanium is higher than at $\lambda = 1550nm$. We designed a set of 4 subdies, connected optically through 1310nm grating couplers and single mode wave-guides.

The subdies in this figure have the following dimensions:

- Switch1: $L=15.2\mu m$, $w=0.7\mu m$
- Switch2: two switches 1 connected electrically in parallel.
- Switch3: $L=30.4\mu m$, $w=0.7\mu m$

(A) Scheme of the $\lambda = 1310nm$ subdies

(B) Scheme of switch2 and switch4

- Switch4: two switches 3 connected electrically in parallel.

For these subdies, we can see that the photo-generated current dependency on power is a square root one, which means that for these devices, the photo-generated pairs are very important compared to the originally existing ones before light exposure, which is in adequacy with the analysis that we have conducted above.

The power dependency measurements will be harvested later on to better fit the photo-conductor model parameters with LUMERICAL. We can now make use of these measurements to have a first insight on the lifetime τ_n of electrons and holes in the photo-conductor.

To do so, we capitalize on the following equilibrium equation:

$$\frac{\Delta n}{\tau_n} = G \quad (3.40)$$

And

$$G = \alpha \eta \frac{P}{h\nu} \quad (3.41)$$

Where:

- α : the absorption coefficient
- η : the dimensionless quantum yield
- ν : the photon frequency

So:

$$\frac{\Delta n h \nu}{\alpha P} = \eta \tau_n \quad (3.42)$$

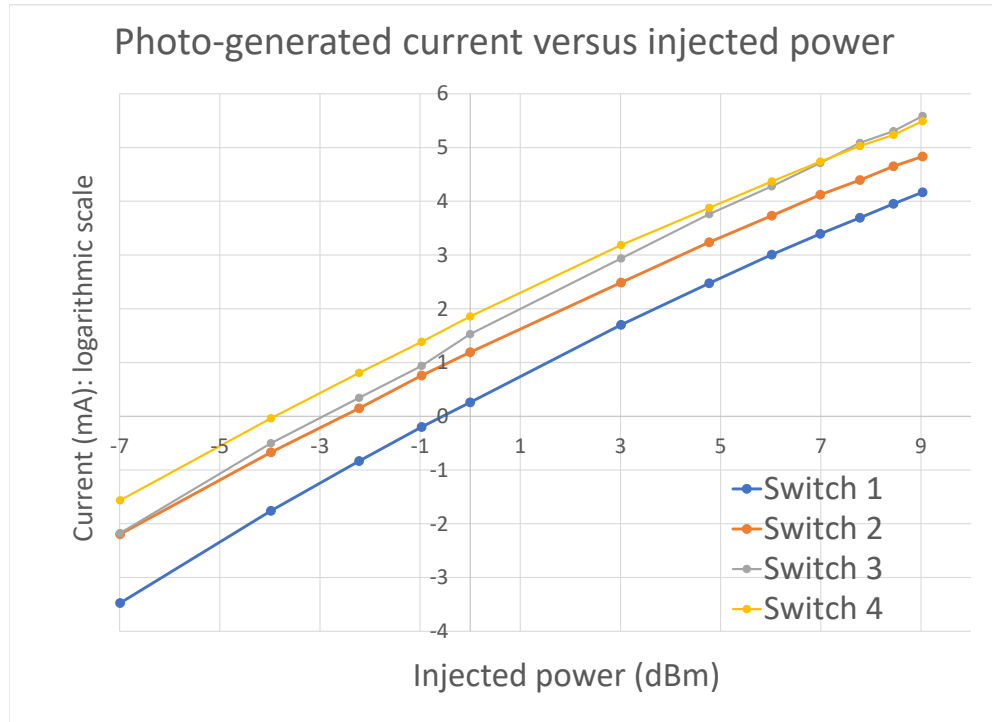


FIGURE 3.23: Photo-generated current versus the injected power at $\lambda = 1330nm$

Since Δn can be calculated from the photo-generated current values:

$$I_{Photogen} = \frac{\Delta n L H e \mu_n V}{w} \quad (3.43)$$

Where:

L : length of the photo-conductor

H : height of the photo-conductor

w : width of the photo-conductor

We can estimate the product $\eta\tau_n$ from the measurements as follows:

$$\eta\tau_n = \frac{I_{Photogen} h\nu}{\alpha P q V \mu_n} \frac{w}{HL} \quad (3.44)$$

In fig. 3.24, the product $\eta\tau_n$ was estimated for three subdie with the following dimensions:

- Subdie3: $L=13.07\mu m$; $w=3.3\mu m$
- Subdie5: $L=13.07\mu m$; $w=5.4\mu m$

- Subdie7: $L=15.2\mu m$; $w=90.68\mu m$

In the plot, η was considered equal to 1 for the three subdies.

The lifetime tendency is almost the same between the three subdies. However, one would expect the lifetime at subdie7 to be the highest since it is the largest subdie, then subdie5 and finally subdie3. The latter may be due to the difference in η between the three subdies, or it could be due to a bad coupling in subdie3 since these measurements are not average ones over a big number of subdies but rather one shot measurements.

We can all the same conclude that the electrons lifetime in the photo-conductor would be about tens of pico-seconds.

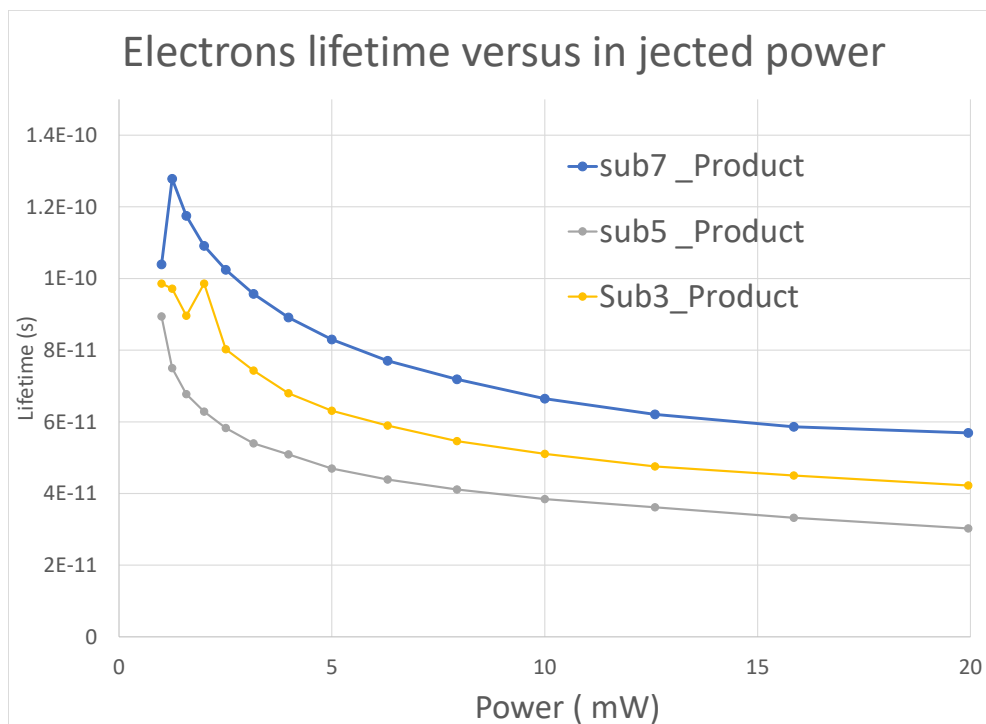


FIGURE 3.24: Lifetime versus power for three subdies with different geometries

3.3 Pulsed measurements

3.3.1 Test bench

Along this section, we will study the behavior of the photo-conductors under pulsed light. We used for this a mode-locked pulsed laser around 1560nm with a pulsing frequency of 100MHz. The optical pulses width is around 100fs at the output of the laser, however since we use a fiber to couple the laser output to the photo-conductor circuit, the pulses stretch and become 3.4ps long at the grating coupler. The optical power at the grating coupler is about 5mW, which amounts to approximately 3mW at the photo-conductor input.

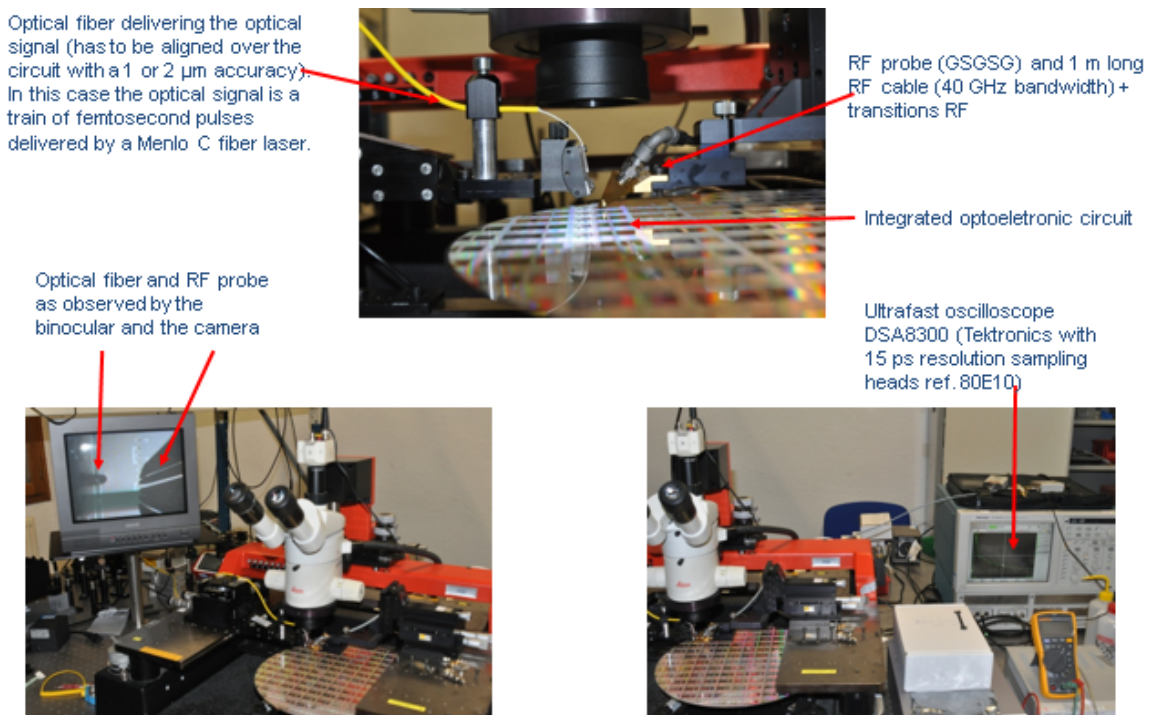


FIGURE 3.25: Pictures of the test bench used to simulate the pulsed response of the photoconductors.

The test bench used to measure the photoconductors pulsed response is presented in fig.3.25. We use Tektronics' ultrafast oscilloscope DSA8300 with the sampling head 80E10 (15ps resolution).

These measurements were conducted at IMEP-LAHC Bourget-du-Lac.

In Fig. 3.26, the electrical scheme of the test bench is presented.

For each photo-conductor circuit, we applied a span of voltages : from 200mV up to 3V.

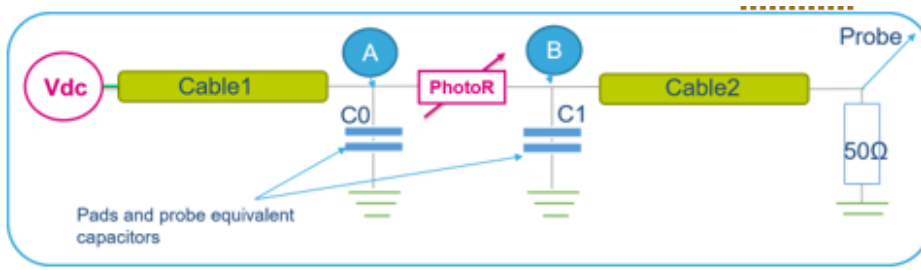


FIGURE 3.26: Electrical scheme of the pulsed measurements test bench

3.3.2 Measurements results

In fig. 3.28, the signal at the oscilloscope is depicted for subdie2 of generationB.

Subdie2 is made of three identical photo-conductors connected in series (electrically) as depicted in Fig.3.27.

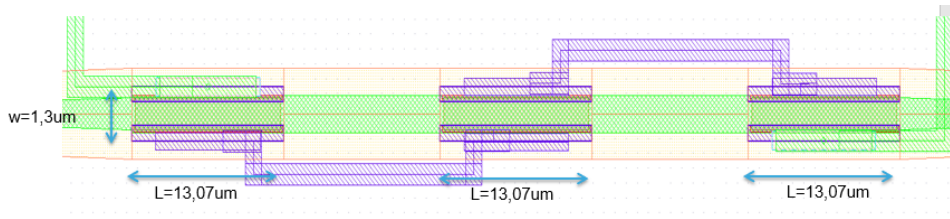


FIGURE 3.27: subdie2 (generationB) layout scheme

The dimensions of each photo-conductor are: $w = 1.3\mu m$ and $L = 13.07\mu m$. The final width on which the biasing voltage is applied is $3 * w = 3.9\mu m$

Note that this width includes also the p-doped regions, so that the real intrinsic germanium equivalent width would be: $w_{Gein} = 1.98\mu m$. This value supposes that boron did not diffuse through germanium, which is a good approximation.

The signals plotted in this figure were harvested separately then put together in a single diagram.

We can clearly see that the response depends heavily on the biasing voltage. This is even clearer on Fig.3.29, where the peak response for each biasing voltage was depicted along with the offset voltage.

Note that the max voltage in this figure is equal to the peak voltage minus the offset voltage.

The dependency of the max voltage on the biasing voltage is not linear as one would expect. This effect will be explained in details within the next section. We can also note that the values of the max voltages are very low compared to the biasing applied voltages; for example: for $V_{bias} = 3V$ the max voltage is only

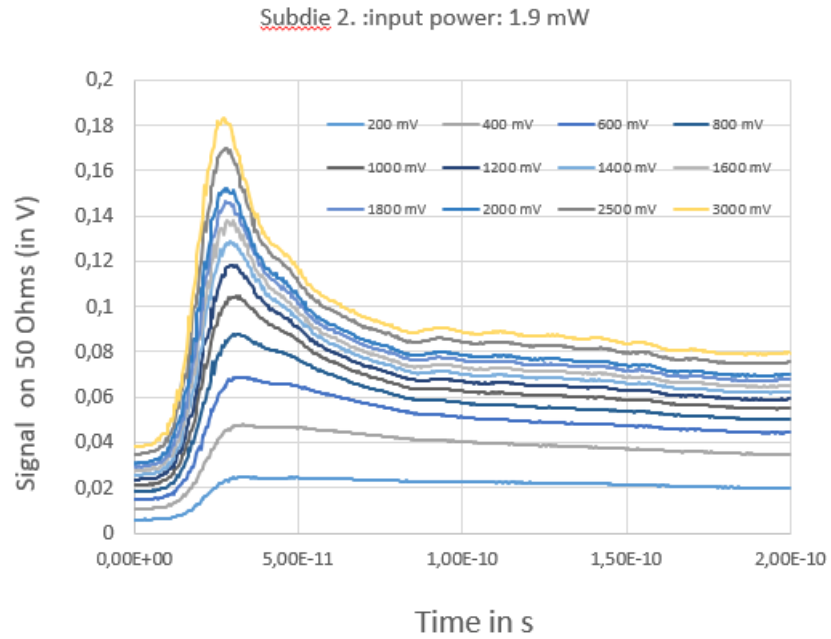


FIGURE 3.28: Pulsed response of subdie2(generationB) for different biasing voltages

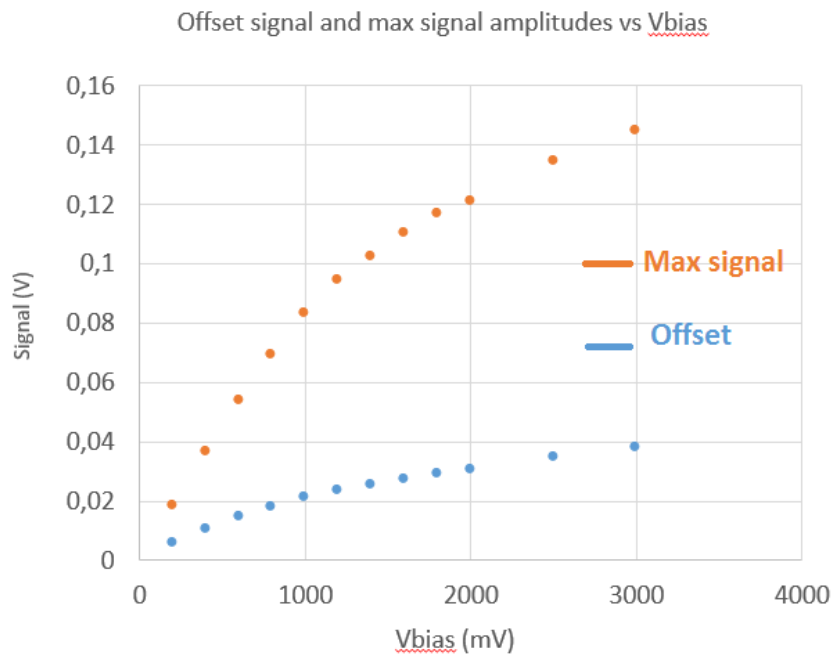


FIGURE 3.29: Offset signal and max signal vs Vbias for subdie2 (generationB)

140mV.

This could result from two different reasons: either the large time resolution of the oscilloscope (15ps) is not enough so that it can spot the peak when it happens or there is another circuit related reason.

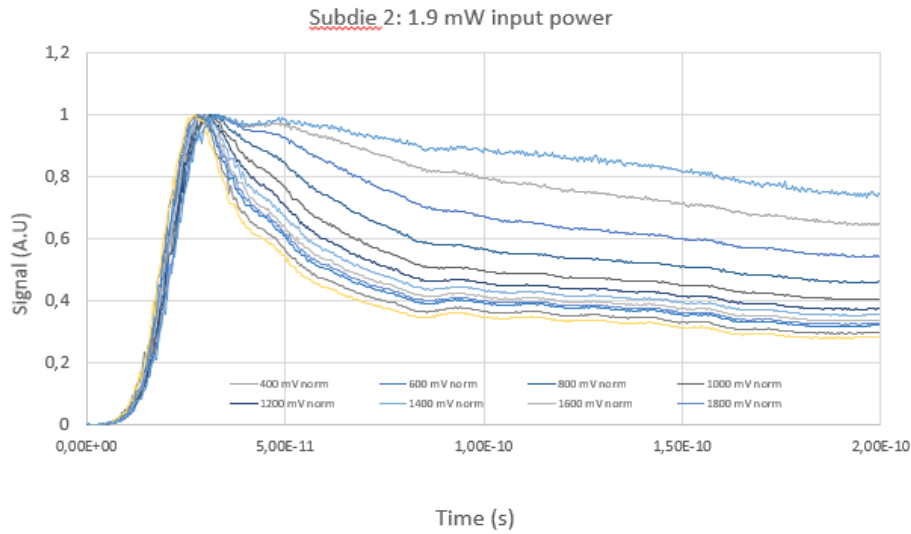


FIGURE 3.30: Normalized pulsed response of subdie2 for different biasing voltages

This second explanation will be given in details within the next section.

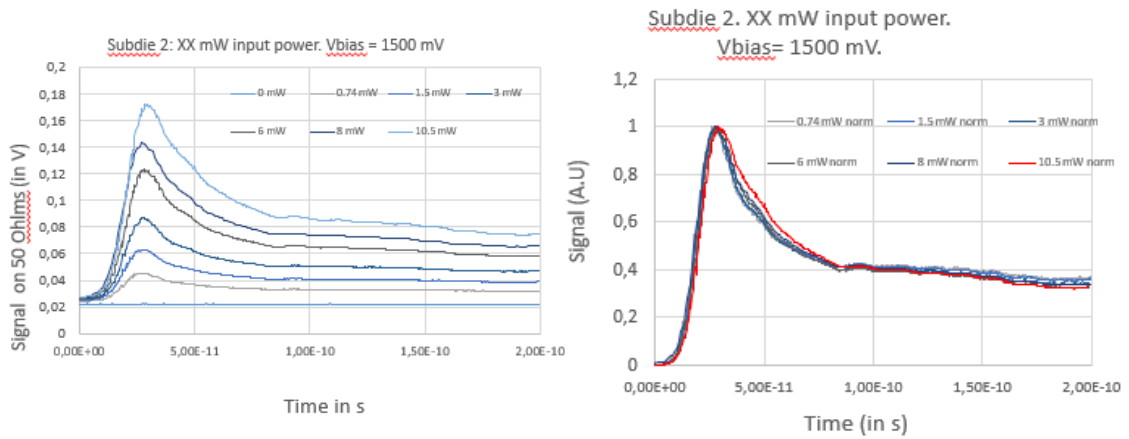
In fig.3.30, we plotted the normalized response of subdie2 (generationB) for different biasing voltages. The curves are normalized with respect to their own peak value so that the final curves have a maximum of 1. This would allow us to better compare the fall lines of the response curves. We can see that the decay time for high voltages is lower than for small biasing voltages. This effect is expected since, for high voltages, charge carriers are sped up much more than for small voltages and have therefore higher chances to recombine faster.

The effect of R_{on} value on decay time is minimal compared to the effect of biasing voltage. Indeed, we have simulated the effect of different R_{on} values, achieved through different optical energy levels, on the decay time as can be seen on fig.3.31.

We have also measured the power response of subdie11 of generationB, which is a basic rectangular photo-conductor with the following dimensions: $w = 7.66\mu m$ and $L = 15\mu m$ see § Appendix.A. The intrinsic germanium width would be in this case: $w = 7.02\mu m$.

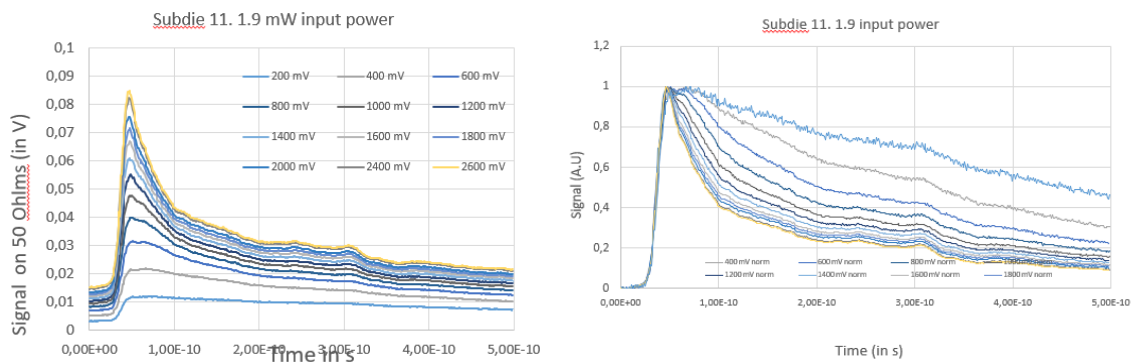
We expect the decay in this case to be even slower than subdie2 since the width of the structure is higher, which means that the electrical field across subdie11 is smaller than subdie2 for the same applied biasing voltage.

The pulsed response of subdie11 is depicted in Fig.3.32a. We can see that the decay times are not very different than subdie2 decay times. For instance, under 200mV, subdie2 reaches 80% of the peak voltage within 130ps approximately. Subdie11 reaches 80% within the same frame of time.



(A) Pulsed response of subdie2 under different optical power levels (B) Normalised pulsed response of subdie2 under different optical power levels

FIGURE 3.31: Pulsed response and normalized pulsed response of subdie2 under different optical power levels



(A) Pulsed response of subdie11 for different biasing voltages (B) Normalized pulsed response of subdie11 for different biasing voltages

FIGURE 3.32: Pulsed response and normalized pulsed response of subdie11 under different optical power levels

This effect can be explained in two different ways:

- The light does not reach the middle photo-conductor in subdie2. Therefore, since subdie2 is made of three photo-conductors in series electrically, the biasing voltage applied to subdie2 is mainly applied to the middle photo-conductor since its resistance is R_{off} while the others exhibit a resistance of R_{on} .
- The second way of explaining this effect would be the presence of doping regions in subdie2 more than in subdieB11 (6 doping regions in subdie2 and only 2 in subdieB11). Indeed, when light is injected into the photo-conductors, a part of it reaches the doping regions. The light is in this case absorbed and produces electron-hole pairs. However, since the electrical

field in these regions is very weak and there is no carriers density gradient, these photo-generated carriers may recombine within the doping region in which case they do not contribute to the total photo-current, or they diffuse and may reach the intrinsic region where they are swept by the electrical field and then contribute to the total photo-current.

However, the current produced by these pairs is a very slow one, since the diffusion is very slow [116].

We believe that the first effect is rather prominent since the doping regions widths are not very big ($0.32\mu\text{m}$ per doping region), the pairs have a limited diffusion length within these regions.

3.3.3 Analysis and model

3.3.3.1 First approach

In order to conclude on the photo-conductor parameters, the most intuitive approach would be to consider the signal at the oscilloscope as the outcome of a simple voltage divider made out of the photo-conductor and the 50Ω impedance of the oscilloscope. This would have been a valid approach in the case of a continuous wave optical signal or if the DC source was directly connected to the photo-conductor.

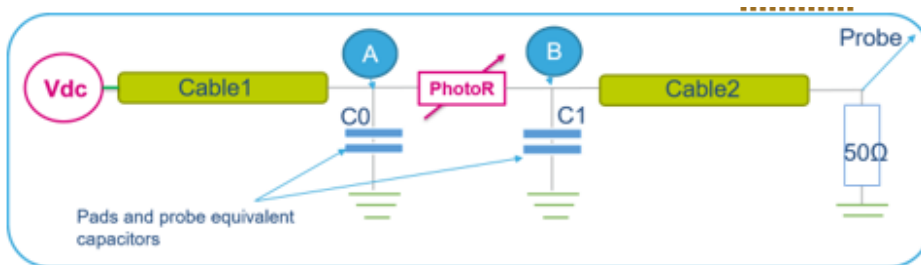
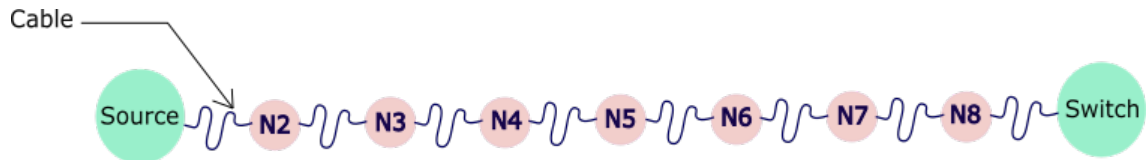


FIGURE 3.33: Electrical scheme of the pulsed measurements test bench

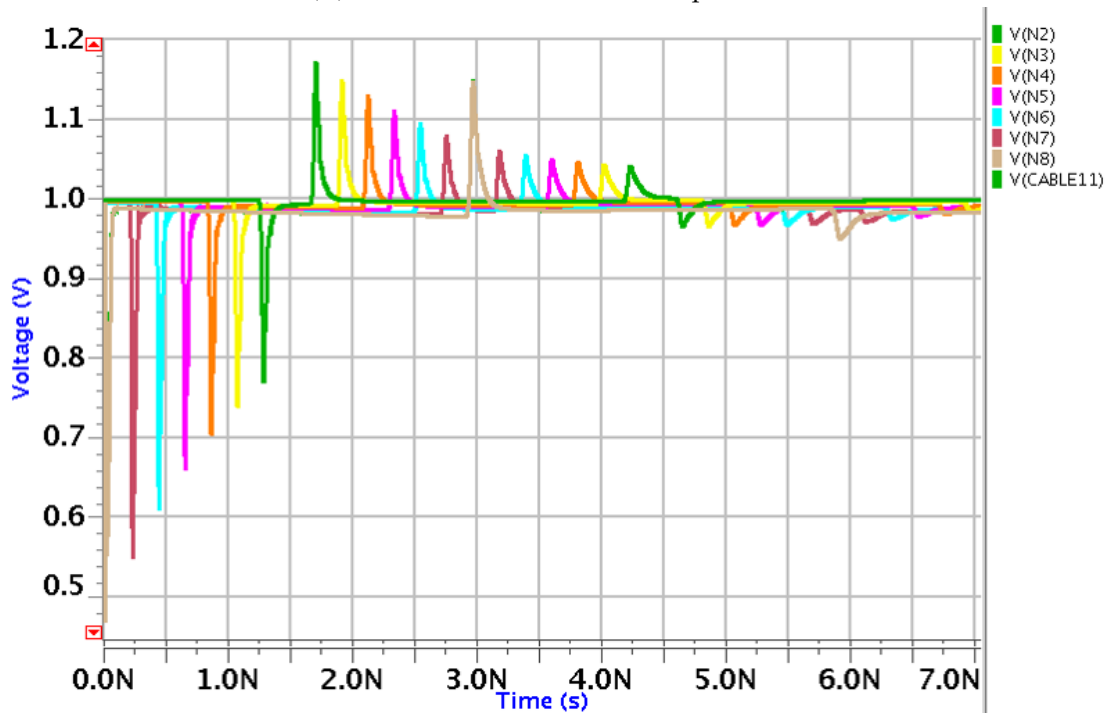
However, in our case, the presence of a cable between the source and the photo-conductor totally alters the final response of the system.

Indeed, when the photo-conductor receives the optical signal, it switches its value from a high resistance R_{off} into a lower one R_{on} . The total resistance seen by *nodeA* (fig 3.33) drops then, which creates a current call at *nodeA*. This current call is provided by the total capacitance at *nodeA* which loses therefore its charge and creates a new current call to the cable.

In order to illustrate the cable response to this current call, we simulated the circuit depicted in fig 3.34a. The circuit used to model the cable is explained in details in appendix.B.



(A) Scheme of a cable with multiple nodes



(B) Time voltage responses at the nodes

FIGURE 3.34: Time response of a cable, at different nodes, to a current call at the switch

The simulated circuit is a DC source that feeds a photo-conductor model (switch) through a coaxial cable, see fig.3.34a. We have divided the cable into eight segments in order to set nodes in between where the signal evolution can be traced. The segments model is similar to the cable model explained in appendix.B but with fewer unit cells.

At $t = 0$, the switch changes its resistance value which creates a current call at node8 which experiences then a voltage drop (see fig.3.34b). The current call is resolved by a charge transfer from the capacitance at node7 into the capacitance at node8, which automatically results in a voltage drop at node7 as depicted in fig. 3.34b. In reality, when node8 voltage drops, the capacitance at this node is charged by the cable unit cell at the node8 side of the cable segment between node7 and node8. The latter then creates a current call and gets charged through the capacitance of the next unit cell and so on until the current call reaches node7.

The voltage drop at node7 is smaller than at node8 because it is attenuated by the cable.

The same phenomenon happens again at the next nodes up till the current call reaches the source. The latter delivers back a current that is equal to the last

current call, which propagates back through the nodes. This can be seen through the positive voltage peaks at the nodes.

We must note that the current calls at this stage are much attenuated compared to the original current call.

When the current response finally reaches the switch node, the resistance of the switch has already come back to its initial value R_{off} : the system has already changed. This last remark is the reason why we cannot predict the system response to the switch current call based on the frequency diagram of the cable. Indeed, since the system changes its initial conditions, the frequency-time convolution becomes inaccurate.

Moreover, if we choose to use an S-parameter cable model, we must establish the cables S-parameter diagram up to $1/(\text{minimal time resolution})$, i.e. more than 10 GHz which requires more resources than just considering the time evolution of the system as we have done so far.

3.3.3.2 Model simulation

We consider again the electrical scheme of the test bench.

- NodeA is the node at which the DC supply voltage is applied to the photo-conductor.
- NodeB is the node after the photo-conductor.
- NodeC is the node after the second cable and is connected to the oscilloscope, namely the 50 Ohm impedance at which the results curves are harvested.

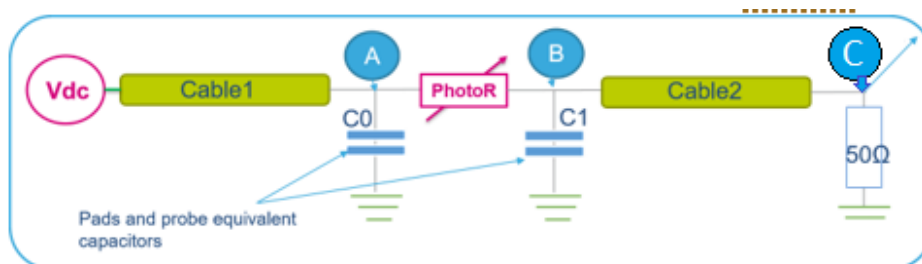


FIGURE 3.35: Electrical scheme of the test bench

With the cable model given in AppendixB, we simulate the voltage response at the probe node for a photo-conductor that goes from a 5 kOhm R_{off} to 10 Ohm R_{on} within a fall time of 10ps . The objective of this simulation is to understand how we can harvest the measurements to track back the photo-conductor parameters.

The signals evolution is depicted in Fig. 3.36.

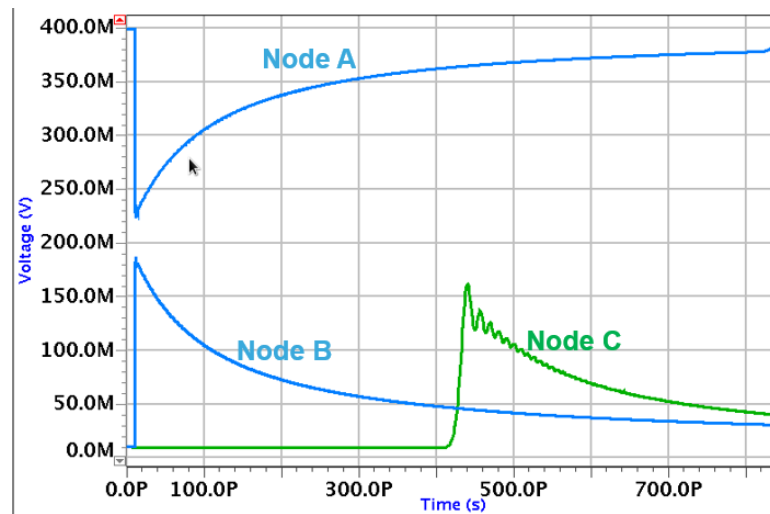


FIGURE 3.36: Signals evolution in nodeA, nodeB and nodeC

We can see that there are two phases:

- Phase 1:
When the photo-conductor is lit up, node A experiences a steep pulse of current call to which only the in-connected capacitors answer. The current provided from node A discharges the capacitors C0 and charges C1. Along this process, the cable at node B is seen as a 50Ω resistor which is the cable surge impedance. The voltage divider equation between node A and node B is preserved; however, the value of node A drops because C0 discharges to provide the current.
- Phase 2:
When the photo-conductor is no more lit up, node B voltage must drop to satisfy the voltage divider equation with node A. This is done by discharging C1 back into C0. We can see in Fig.3.36 how node A goes back to its initial value while node B drops back.

With this understanding, we can already see why this analysis is very important to harvest the measurement results. Indeed, we can already see that, even for extremely small values of R_{on} , the voltage at the oscilloscope will never reach the V_{source} value.

Moreover, the decay of the curve at the oscilloscope node does not give a very accurate idea about the decay at nodeB. For nodeC, many factors have to be taken into consideration:

- The bandwidth of the oscilloscope.
- The attenuation from nodeB to nodeC.
- The signal ripples due to impedance mismatch.

The last consideration becomes very important if the signal ripple reaches the switch node before the signal decay is achieved. In this case, the decay curve would not convey the real resistance decay of the sampler.

Therefore, the intuitive approach of just fitting the curve at the oscilloscope in order to trace back the value of R_{on} and the decay constant is completely false.

3.3.3.3 Conclusions

So, with the up said in mind, we can trace back to the photo-conductor resistance changes over time.

In order to achieve this, we have reversed the phases explained above for pulse measurements of subdie11 of GenerationB.

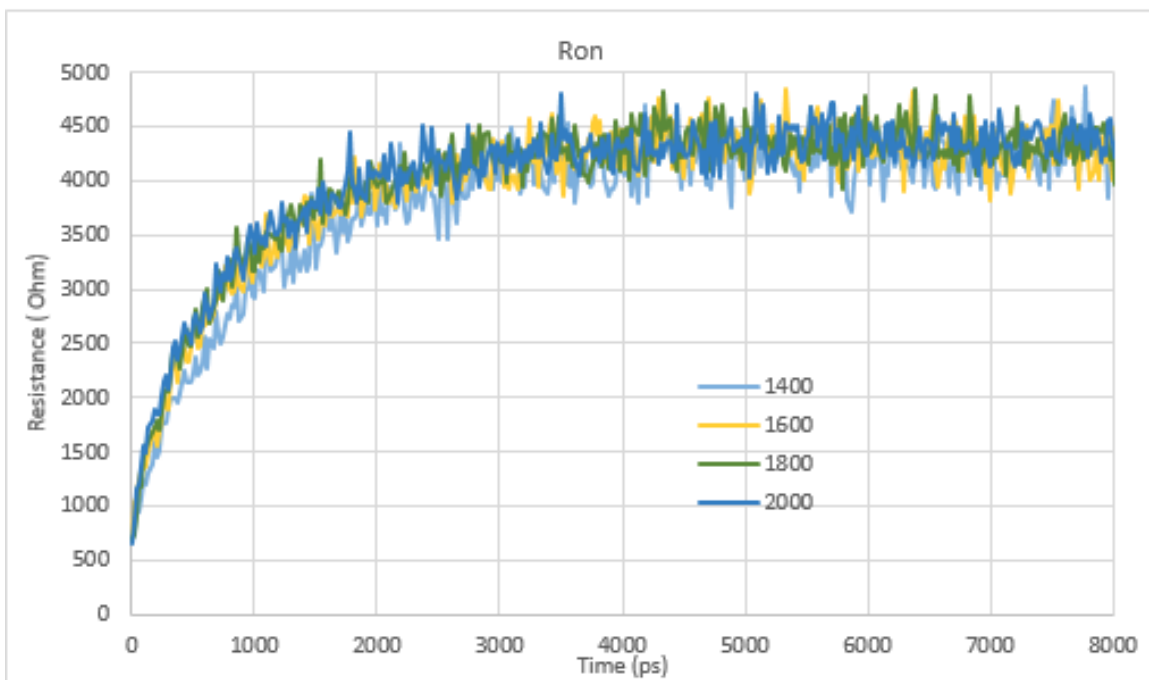


FIGURE 3.37: R_{on} evolution in time for different biasing voltages

In Fig.3.37, we presented the photo-conductor R_{on} changes versus time.

Based on this curve, we have concluded R_{gen} evolution over time in fig.3.38, where:

$$\frac{1}{R_{gen}} = \frac{1}{R_{on}} - \frac{1}{R_{off}} \quad (3.45)$$

3.39.

The biasing voltages in legend in both curves are given in mV.

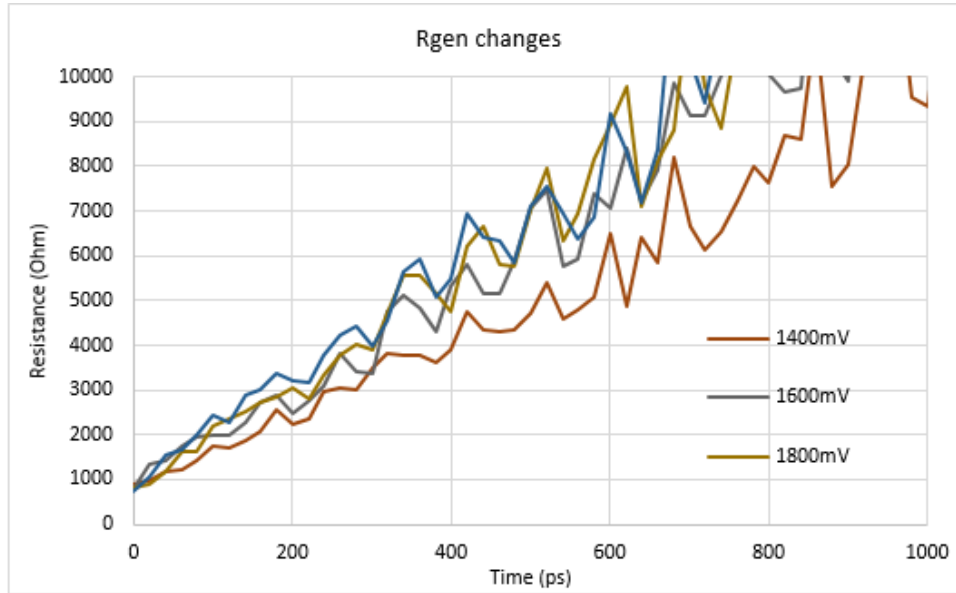


FIGURE 3.38: Photo-generated resistance curve in time

We just presented the results of R_{gen} over a restricted time period compared to R_{on} because above this time laps, evaluating R_{gen} becomes very difficult as we use the equation:

The voltage divider model based on which these results were investigated becomes inaccurate as R_{on} increases; the response of the system becomes delayed by the $R_{on}C_1$ time constant which increases at the same pace as R_{on} . Therefore, the R_{on} and R_{gen} changes curves do not give an accurate value of the photo-conductor fall time.

The 15 ps time resolution along with the short pulse width (3.4ps) makes it difficult to determine the R_{on} peak value. The attenuation along the second cable is not taken into consideration as well, which means that the peak R_{on} value may be even lower than what we suppose.

Now we can trace back to the time constant according to which the resistance changes. For this purpose, we investigate an exponential approximation that we try to fit on the normalized resistance curve, fig. 3.39.

The exponential approximation equation is: $f(t) = 1 - e^{-t/\tau}$, where τ is a time constant and is equal, for this example to 740ps.

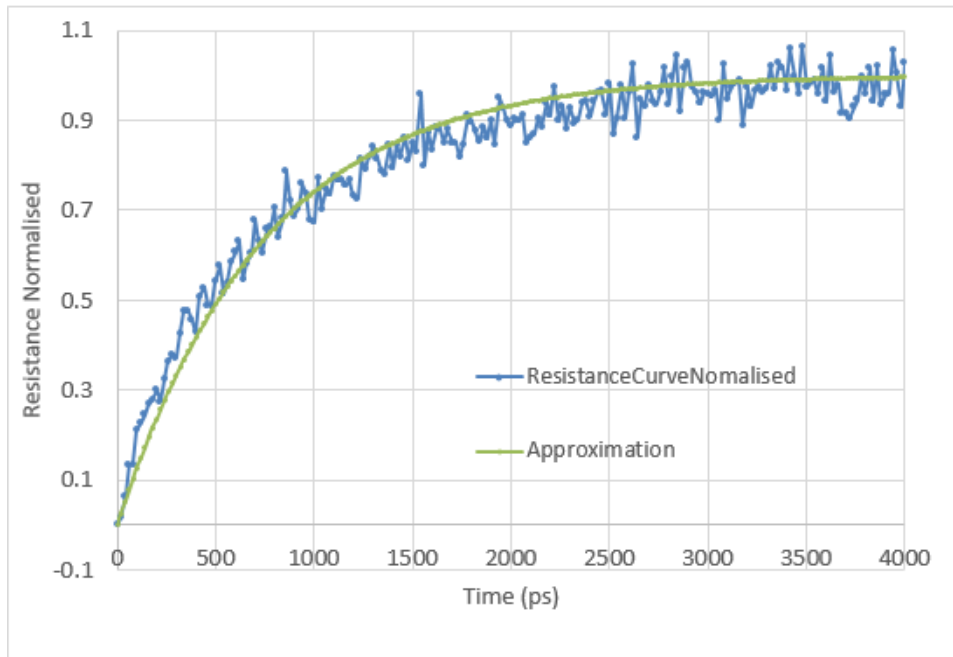


FIGURE 3.39: Exponential approximation of the Ron curve

Even if this approximation is based on a good understanding of the system dynamic over time (cables model above), we cannot conclude yet that this time constant value is the real resistance decay that we have, but we can all the same state that the decay time constant in our case is shorter than 740ps. Indeed, as explained above, many phenomena impede the harvesting of the decay constant, one of which being the signal ripple due to impedance mismatch along with the oscilloscope bandwidth and the cables time response.

For all these considerations, we have chosen to work around the decay time problem in the sampling circuits that we designed as will be explained in the forthcoming chapters.

3.3.4 Conclusion

In this chapter, the aim was to find a model to describe the behavior of the photo-conductors with and without light in order to better fit them to the constraints of the sampling circuit.

To do so, we have first harvested DC measurements of the photo-conductors response with and without light. These measurements were done on germanium photo-conductors with sweeps on length and width (generationB devices mainly) in order to conclude on a general behavior of the said devices.

This first analysis allowed us to see that the off resistance of the devices changes both according to their geometry and the voltage applied. The origins of the geometry dependency of the off resistance are mainly related to the germanium growth process. We have all the same established a tendency line between geometry, most precisely dimensions ratio, and the R_{off} value.

The R_{off} dependency on voltage was predictable and can be traced back to the carriers velocity saturation in germanium.

With this first understanding, we have harvested DC measurements of the photo-conductors with continuous wave light and tried to establish a model for the R_{on} variations with voltage, input power and geometry.

We have established then a phenomenological model that fits to a good extent the measurement results. The latter was inspired from the velocity saturation model and models the conduction saturation that occurs when the voltage applied is high enough to sweep the photo-generated pairs as soon as they are generated.

We have then harvested measurements of the photo-conductors with a DC source and pulsed light. To do so, we presented a model of the coaxial cables that explains the system time dynamic. Indeed, since the system is inherently not impedance-matched, i.e. the sampler impedance goes from R_{off} to R_{on} , we could not just rely on the frequency diagram of the cables to explain the total behavior of the system.

Even though the analysis did not allow us to come to a decision regarding the decay time constant or the value of the R_{on} peak resistance, but it was necessary to do. Indeed, in case we did not conduct this analysis, it would have been easy to jump to false conclusions about the decay time and the peak R_{on} value. The analysis makes it clear to see the complexity of the phenomena that interfere with the system time response.

Chapter 4

Germanium photo-sampler:

Within the previous chapter, we have measured the resistivity of the germanium photo-conductors both in off and on state. The steady state measurements (continuous wave and DC voltage), show low values of the R_{off} on R_{on} ratio (an average value of 27 can be retained). Moreover, we have simulated the photo-conductors response to pulsed light, and we have seen that the electrical response exhibits fall times of hundreds of pico-seconds.

In the first section of this chapter, we will explain the impact of these two effects on the operation of the basic optical sampler circuit. The alternative solutions that we have developed to overcome the latter problem will be exposed in details through the second section.

4.1 Basic sampler circuit: operation and problems

The purpose of this section is, as said before, to provide a deeper understanding of the impact of the photo-conductors characteristics on the sampler operation.

Therefore, the first subsection explains the basic operation of an optically-driven sampler. The second subsection presents the test bench that could be used to validate the jitter performance of the sampler circuit. The last subsection gives an elaborate illustration of the way the photo-conductors performance affects the operation of the sampler and alters the validation test bench results.

4.1.1 Sampler circuit

The basic sampler circuit, depicted in fig .4.1, consists of a switch that is optically controlled, in series with a hold capacitor.

The switch has two resistance values: R_{on} and R_{off} , where $R_{on} < R_{off}$. When an optical pulse hits the switch, its resistance drops from R_{off} to R_{on} . The low pass filter made of the switch and the capacitor, sees its cutoff frequency

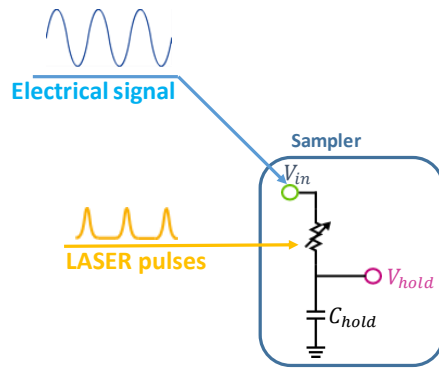


FIGURE 4.1: Electrical circuit of a basic sampler

increase and go from f_1 to f_2 ; where $f_1 = \frac{1}{R_{off}C}$ and $f_2 = \frac{1}{R_{on}C}$.

Therefore, the input signal V_{in} , assuming that its frequency f_{in} is lower than f_2 , is copied at node V_{hold} .

When the optical signal goes off, the cutoff frequency goes back to f_1 as R_{off} is supposed to be high.

The signal can no longer be copied to node V_{hold} and the latter node is disconnected from the rest of the circuit. The capacitor C_{hold} holds therefore the last tracked value of the signal V_{hold} .

Before presenting the jitter test bench circuit, we will first explain how the jitter affects the performance of a standard ADC and the way it is generally measured.

4.1.2 Jitter in ADC

The sampling circuit that we depicted in fig .4.1 is generally used at the front of an ADC stage. The held signal goes through a quantization block whose output is the digital code.

The presence of a jitter at the sampling block alters the held signal and can be deduced later on in the digital code, provided the input signal frequency is high enough.

We harvest this property to validate the optical clock jitter value and the good functioning of this sampler circuit.

In order to better understand the effect of jitter on the final quantized signal, we consider a sampling circuit with jitter at the sampler clock, see fig.4.2.

A jittery clock is a clock that experiences random period deviations from a perfect clock with the same frequency. Such a deviation, say Δt , causes the sampler to sample the wrong value of the input signal, see fig. 4.2.

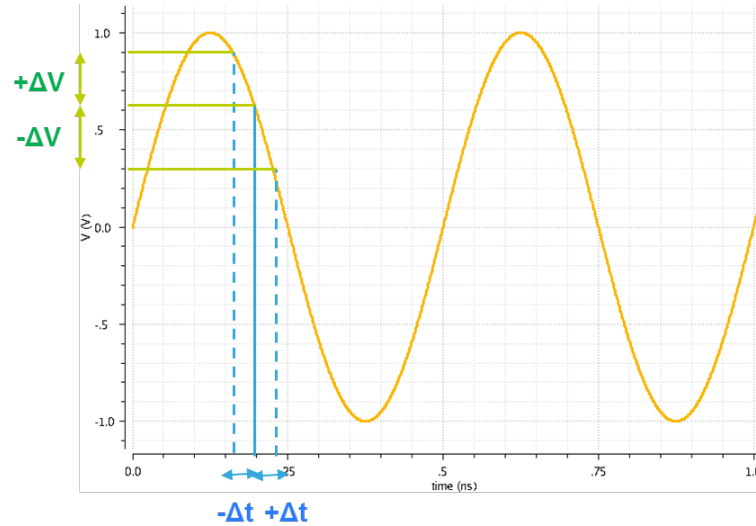


FIGURE 4.2: Effect of jitter at the sampler output

We can intuitively see, from fig.4.2, that the higher the frequency of the signal, the higher the error ΔV .

In a more practical level:

$$\Delta V = \Delta t \frac{dV}{dt} \quad (4.1)$$

Now since:

$$V = A \sin(2\pi f_{in} t) \quad (4.2)$$

Where A is the input signal amplitude and f_{in} its frequency.

$$\Delta V = A \sin(2\pi f_{in}(\Delta t + t)) - A \sin(2\pi f_{in} t) \quad (4.3)$$

Given that Δt is small enough, we can consider that:

$$\Delta V = A 2\pi f_{in} \Delta t \quad (4.4)$$

So, if we consider that the jitter root square mean is j_{rms} , then such a jitter causes a voltage error of:

$$\Delta V = A 2\pi f_{in} j_{rms} \quad (4.5)$$

We can see that the error is directly related to the jitter and to the signal frequency.

If we report this error to the input signal, we get an SNR of:

$$SNR = 20 \log\left(\frac{A}{A 2\pi f_{in} j_{rms}}\right) \quad (4.6)$$

So that:

$$SNR = -20 \log(2\pi f_{in} j_{rms})$$

The jitter is a noise contribution that adds up to the other ADC noise contributions. Therefore, if we want to detect the jitter effect on the SNR, its contribution must be at least 3dB above the noise level at the ADC output.

Based on the latter equation, from a given value of j_{rms} the jitter effect on SNR becomes more important as the frequency of the signal increases, see fig.4.3.

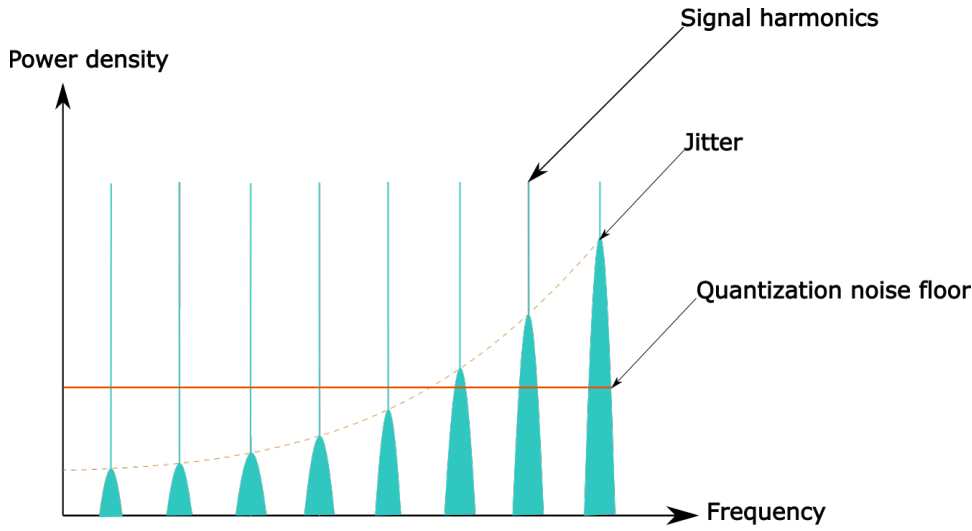


FIGURE 4.3: Jitter power density distribution over frequency

We can estimate the signal frequency at which the jitter contribution is 3dB higher than the quantization noise floor as follows.

$$SNR_{jitter} < SNR_q - 3 \quad (4.7)$$

Where: SNR_q is the output SNR of an ADC, i.e. quantization noise effect on the ADC output signal SNR, and [117]:

$$SNR_q = 6.02ENOB + 1.72 \quad (4.8)$$

Where: ENOB is the effective number of bits of the ADC, i.e. the number of bits that a perfect ADC, with only the effect of the quantization noise, would have for the same output SNR.

Therefore, in order to detect jitter, we need the input signal frequency to be at least equal to:

$$f_{in} \geq \frac{1}{2\pi j_{rms}} 10^{\frac{-6.02ENOB + 1.28}{20}} \quad (4.9)$$

So, say we need to detect a jitter of $j_{rms} = 0, 1ps$.

- With an ADC of ENOB=10 bits, we must have an input frequency of at least $f_{in} > 1,8GHz$
- with an ADC of ENOB=5 bits, we must have an input frequency of at least $f_{in} > 57GHz$

4.1.3 Test circuit limitations

The previous discussion gives us a method to validate the sampler jitter value. The test scheme is presented in fig .4.4.

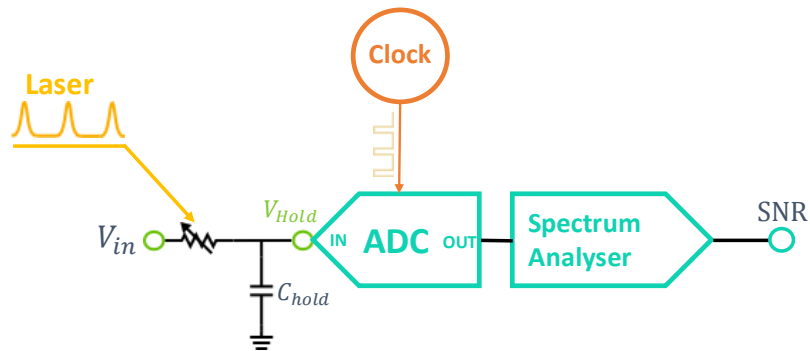


FIGURE 4.4: Jitter measurement circuit scheme

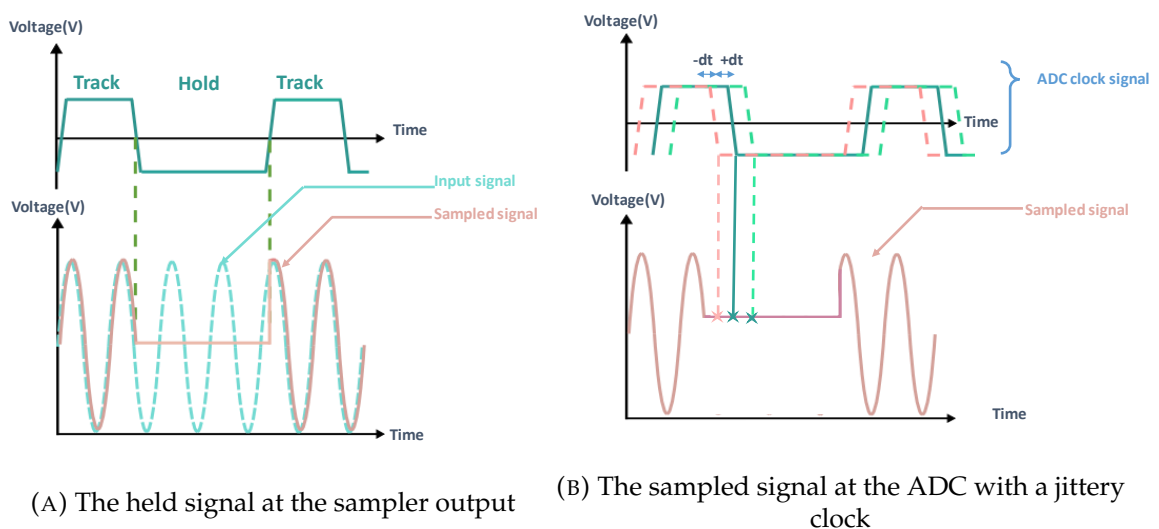


FIGURE 4.5: Plots of the test bench operation

The idea of this circuit is to re-sample the signal at the output of the sampler and quantize it through the ADC and then measure its SNR.

The test bench concept is that the signal is first sampled by our optoelectronic sampling circuit, see fig.4.5. At this point, the sampled signal is steady in time (within the hold time period), so that if we re-sample it again with an ADC, see fig.4.5, the ADC clock jitter causes no additional noise to the signal.

In fig.4.5, we considered a jittery ADC clock, with a period variation of ΔT . We can see that, since the held signal is steady, the re-sampled signal at the ADC in all the cases is the same so that the ADC clock jitter goes unnoticed.

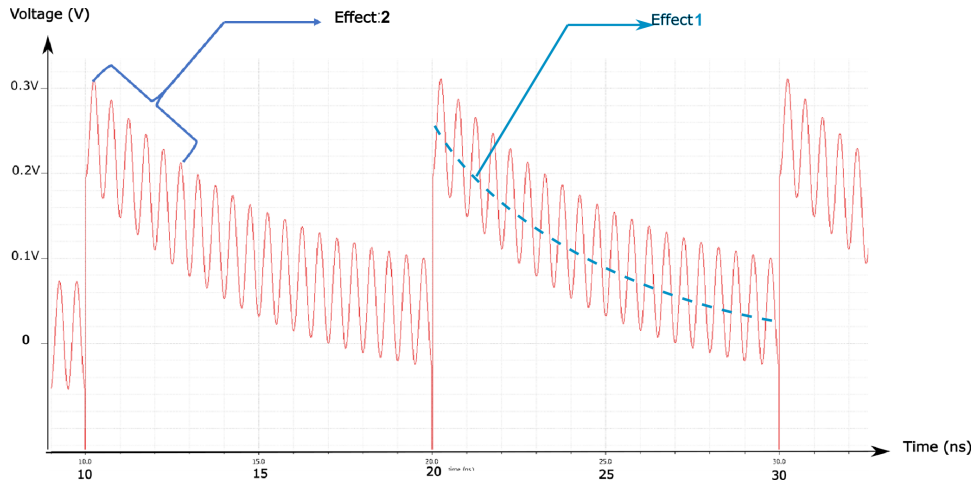


FIGURE 4.6: Sampler output signal in the case of low R_{off}

However, given that the sampler R_{off} values are not very high, the hold signal (at the sampler's output) is not properly held through the clock period, see fig. 4.6.

In fig.4.6, we simulated the time response of the a sampler model with a real R_{off} and R_{on} values. Here: $R_{off} = 5400\Omega$, $R_{on} = 10\Omega$ and $C_{hold} = 1pF$. The sampled signal is at 2GHz.

We can see two effects due to the limited value of R_{off} .

- **Effect1:**

The first effect is the fact that the signal tends to drop from the held value to a lower one along the hold phase. This first effect is a pretty predictable one. Indeed, if we consider the low-pass RC filter, made out of R_{off} and C_{hold} , then the input signal is attenuated at the hold node, provided its frequency is beyond the filter cutoff frequency.

This attenuation is given by the following formula:

$$G = \frac{1}{\sqrt{1 + (2\pi f_{in} R_{off} C_{hold})^2}} \quad (4.10)$$

However, this filter response, i.e. the input signal with an attenuated amplitude, is not obtained instantly. It is rather a permanent state response that

is reached through a transition state. The output signal starts at the held signal value and evolves slowly towards the attenuated sine wave signal. This transition phase is characterized by a time constant equal to:

$$\tau = R_{off}C_{hold} \quad (4.11)$$

This time constant, being directly proportional to R_{off} , explains why in our case where R_{off} is smaller than usual, this first effect is very noticeable.

- **Effect2:**

The second effect can now be very easily explained as it is adjacent to effect1. The oscillations that we see stand for the attenuated input signal and is commonly known as input signal leakage. Here again, if we go back to the signal attenuation amplitude given by equation. 4.10, we will see that the bigger R_{off} , the smaller the leakage amplitude.

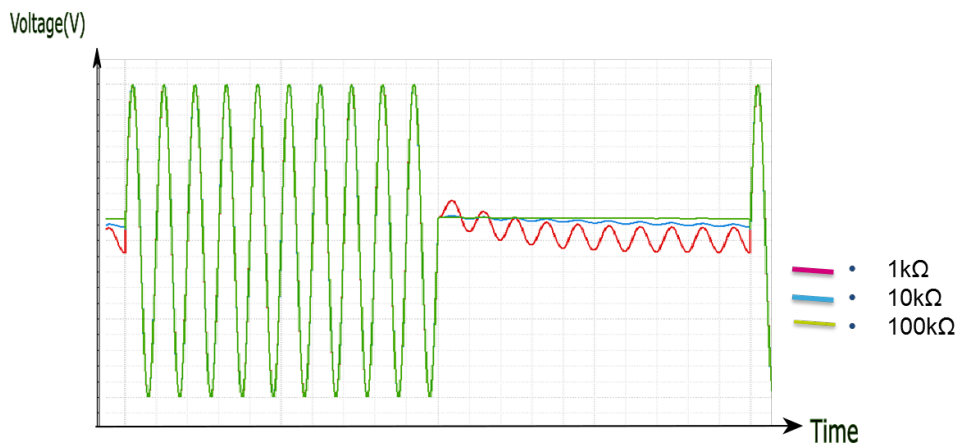


FIGURE 4.7: Sampler output signal in the case of different R_{off} values

In order to better visualize the effect of the value of R_{off} on the sampled signal, we ran a test with the sampler model, where R_{on} is the same (10Ω), and R_{off} changes, see fig. 4.7. We considered three different values of R_{off} : $1k\Omega$, $10k\Omega$ and $100k\Omega$.

Given these two effects, and especially the first one, the jitter test bench presented at fig.4.4 does not meet the requirements to achieve its task.

Indeed, the signal being not held throughout the hold phase means that the ADC, when it samples the held signal, makes an error that is relative to its own clock jitter.

In order to have more insight on the impact of a low R_{off} value,

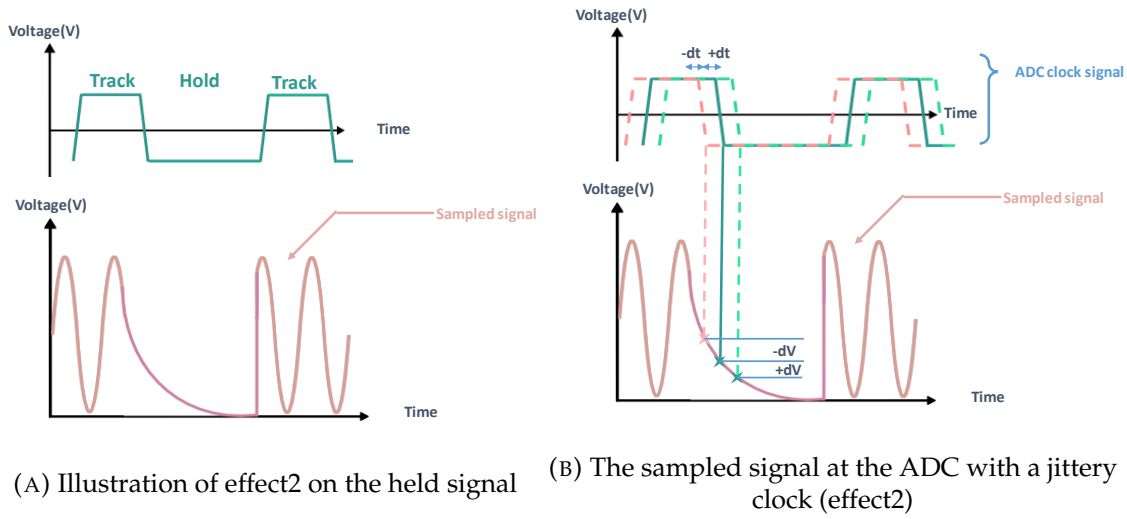


FIGURE 4.8: Illustration of the impact of effect1 on the sampled signal

We first consider the impact of effect1 on the final SNR. Say S is the value of the sampled signal at $t = T_{hold}$, see Fig.4.8.

The held signal evolves as follows:

$$S(t) = S * (1 - e^{-\frac{t}{\tau}}) \quad (4.12)$$

Therefore the error made due to effect1 is equal to:

$$\Delta V_{effect1} = S(1 - e^{-\frac{t + \Delta t}{\tau}}) - S(1 - e^{-\frac{t}{\tau}}) \quad (4.13)$$

So that:

$$\Delta V_{effect1} = S * \frac{\Delta t}{\tau} * e^{-\frac{t}{\tau}} \quad (4.14)$$

There are therefore two sources of error due to this effect:

- Signal loss: the actual decreasing exponential slope that is determined by the $R_{off}C_{hold}$ time constant
- Jitter of the ADC: represented by the $\Delta V_{effect1}$

Now we will investigate the impact of effect2 on the SNR.

Say the ADC's clock jitter mean square root jitter is $j_{ADC_{rms}} = \Delta t$. If we consider only the effect2, then, using Eq.4.4, this jitter causes an error on the sampled

signal equal to:

$$\Delta V = A * G * 2\pi f_{in} \Delta t \quad (4.15)$$

Where:

A : the input signal amplitude

G : the attenuation of the signal due to effect1, see eq.4.10

Therefore:

$$\Delta V = \frac{2 * A * \pi f_{in} j_{ADCrms}}{\sqrt{1 + (2\pi f_{in} R_{off} C_{hold})^2}} \quad (4.16)$$

The SNR degradation is therefore equal to:

$$SNR_{jitterADC} = 20 \text{Log} \left(\frac{A}{\frac{2 * A * \pi f_{in} j_{ADCrms}}{\sqrt{1 + (2\pi f_{in} R_{off} C_{hold})^2}}} \right) \quad (4.17)$$

So:

$$SNR_{jitterADC} = 20 \text{Log} \left(\frac{\sqrt{1 + (2\pi f_{in} R_{off} C_{hold})^2}}{2 * \pi f_{in} j_{ADCrms}} \right)$$

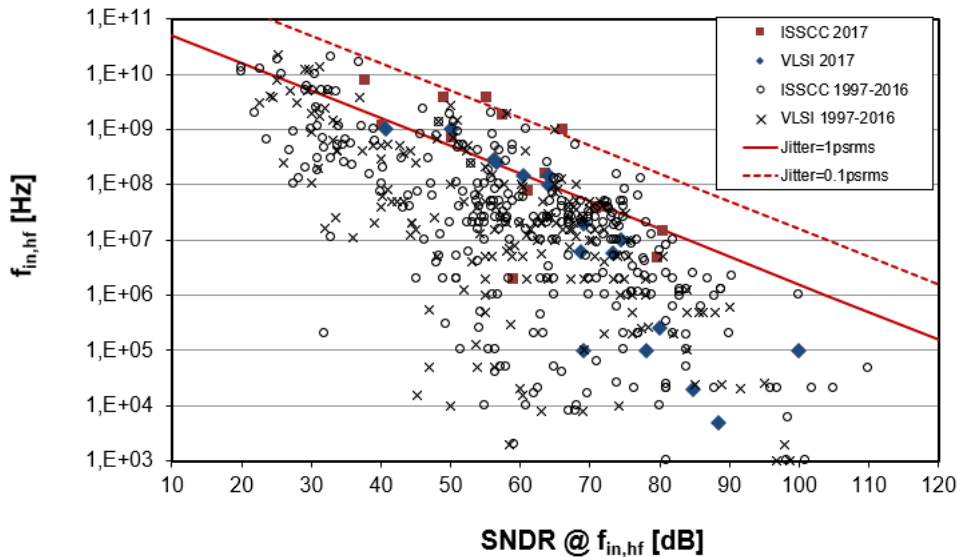


FIGURE 4.9: ADC jitter FOM survey by Boris Murmann

The output SNR in this case is then the result of two consecutive jitter contributions. Moreover, each contribution is relative to a different frequency which makes the task of recovering the original signal jitter even more complicated.

NB: For simplification purposes, we have not illustrated the real sampled signal. Effect2 was indeed omitted because the main problems we face at the ADC sampling occur because of effect1.

In fig.4.8b, we depicted the real sampler response to an input signal.

4.1.4 Conclusion

We can see that the low values of R_{off} impede very much the operation of the sampler as well as the jitter validation through the test bench. It is worth mentioning that in the previous section, only the effect of R_{off} value was considered, but there is another effect that affects as much, if not more the operation of the test bench, which is the slow fall time of the photo-conductors.

Therefore, we must come up with solutions that circumvent the R_{off} and fall time problems while maintaining a small value of R_{on} .

4.2 Basic sampler circuit: alternative solutions

Given what has been said before, we used two different approaches:

- Increase the R_{off} on R_{on} ratio.
- Work around the problem by using suitable electronic drivers.

The first approach is, as stated, to increase the R_{off} on R_{on} ratio, either by increasing R_{off} or by decreasing R_{on} . We can do so by optimizing the geometry of the photo-conductor in a way that favors the photo-generation efficient segments, mainly the first ones along the propagation direction, over the least efficient segments, i.e. the last ones. This possibility has been explored and will be explained in the first two subsections hereafter.

Now we know that the small values of R_{off} are also due to the residual p-doping in the germanium "intrinsic" region. So, an intuitive approach would be to try to cancel this doping. However, since it is an unwanted result of the ST process and can hardly be modified beforehand through design (we did not have the permission to alter STMicroelectronics process), we can only try to undo its damage afterwards. An N-type counter-doping solution was used and will be explained in the third subsection of this part.

The last approach is to use the opto-electronic sampler as is and try to work around its difficulties by using appropriate electronic circuits. This approach is provided with great details in the last subsection under "Workaround circuit".

4.2.1 Novel geometry

4.2.1.1 Basic concept

The first approach to increasing the R_{off} on R_{on} ratio is to use an optimized geometry that does so.

We need first to understand what limits the R_{off} on R_{on} ratio in a standard photo-conductor. So, let us consider a basic rectangular photo-conductor, with a lateral light injection.



FIGURE 4.10: Exponential photo-conductor view

When the light is injected into this photo-conductor, a part of it is absorbed into the material and gives rise to electron-hole pairs. The density of the photo-generated pairs decreases exponentially along the photo-conductor which is in agreement with the absorbed power evolution.

This is to say that the first micrometers of the photo-conductor generate way more pairs than the last micrometers, while both exhibit the same value of resistivity in off state.

The idea behind the novel geometry that we used (the exponential photo-conductor geometry), is to maintain a high and constant photo-generated pairs density along the photo-conductor, which yield a very optimized R_{off} on R_{on} ratio. It does so by maintaining a fix energy flux throughout the photo-conductor, i.e. while the number of photo-generated pairs decreases exponentially, the width of the structure decreases in the same exponential fashion, which leads to a constant pairs density along the photo-conductor.

4.2.1.2 Theoretical explanation

Say that we consider that, for an incident optical energy of E , N electron-hole pairs are generated where:

$$N = k * E \quad (4.18)$$

k is a coefficient that includes the mobility of electrons and holes and their lifetime as well as the inverse of the energy of a single photon. The exact expression of k is not relevant to this demonstration, so we will not give it now.

Then, let us consider a segment of the photo-conductor, taken vertically to the propagation direction, as depicted in fig.4.11.

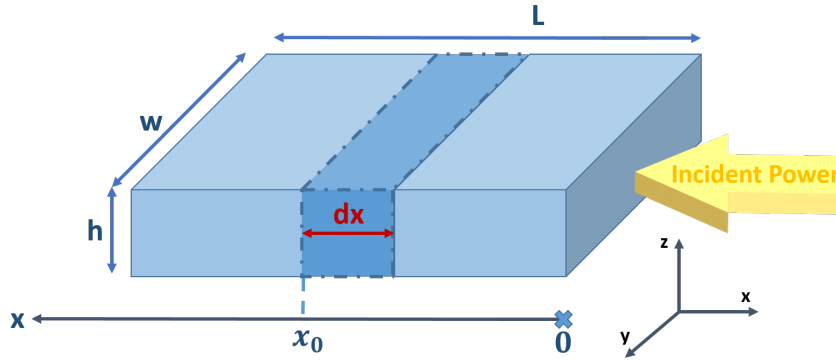


FIGURE 4.11: Overview of the photo-conductor

The current produced by this segment, for an applied voltage of V , is equal to:

$$dI = \frac{N}{W} * e * (\mu_n + \mu_p) * \frac{V}{W} \quad (4.19)$$

Where:

μ_n : the electron mobility

μ_p : the holes mobility

e : the electron charge

So that:

$$dI(x) = \frac{k * E_0 * e^{-\alpha * x} * \alpha * dx}{W} * e * (\mu_n + \mu_p) * \frac{V}{W} \quad (4.20)$$

Where E_0 is the incident energy at $x=0$.

In the case of a rectangular photo-conductor, the total photo-generated current is given by the integral of the latter current over x for $x=0$ to $x=L$:

$$I = \int_0^L \frac{k * E_0 * e^{-\alpha * x} * \alpha * dx}{W} * e * (\mu_n + \mu_p) * \frac{V}{W} \quad (4.21)$$

So that:

$$I_{recton} = \frac{k * E_0 * (\mu_n + \mu_p) * V}{W^2} * (1 - e^{-\alpha L})$$

The off current being equal to:

$$I_{rect_off} = \rho * \frac{L * h}{W} * V \quad (4.22)$$

Where: ρ is the conductivity of the material (germanium in our case).

So that:

$$\left(\frac{R_{off}}{R_{on}}\right)_{rect} = \left(\frac{I_{off} + I_{on}}{I_{off}}\right)_{rect} = \frac{\rho * \frac{L * h}{W} * V + \frac{k * e * E_0 * (\mu_n + \mu_p) * V}{W^2} * (1 - e^{-\alpha L})}{\rho * \frac{L * h}{W} * V} \quad (4.23)$$

$$\eta_{rect} = \left(\frac{R_{off}}{R_{on}}\right)_{rect} = 1 + \frac{k * e * E_0 * (\mu_n + \mu_p) * (1 - e^{-\alpha L})}{W * \rho * L * h}$$

Now, if we consider an exponentially decreasing photo-conductor as depicted in fig.4.10, then the contribution of a dx segment at x expressed in eq.4.21 must be changed by replacing w by $W_0 * e^{-\alpha * x}$

$$dI(x) = \frac{k * e * E_0 * e^{-\alpha * x} * \alpha * dx}{w_0 * e^{-\alpha * x}} * e * (\mu_n + \mu_p) * \frac{V}{W_0 * e^{-\alpha * x}} \quad (4.24)$$

Therefore, the total current becomes:

$$I_{exp_on} = \frac{k * e * E_0 * (\mu_n + \mu_p) * V}{w_0^2} * (e^{\alpha L} - 1)$$

The off current can be estimated following the same logic, and is equal to:

$$I_{exp_off} = \frac{\rho * h * (e^{\alpha L} - 1)}{\alpha * W_0} * V \quad (4.25)$$

Therefore, the exponential ratio is:

$$\eta_{exp} = \left(\frac{R_{off}}{R_{on}}\right)_{exp} = 1 + \frac{k * \alpha * e * E_0 * (\mu_n + \mu_p)}{W_0 * \rho * h}$$

We can see that the exponential photo-conductor ratio has no dependency on L , where the rectangular ratio decreases with L . In order to better illustrate this effect, we have plotted the ratio of $ratio_{exp}$ on $ratio_{rect}$ in fig.4.12. For this figure, we made the approximation that the ratios are greater than 1.

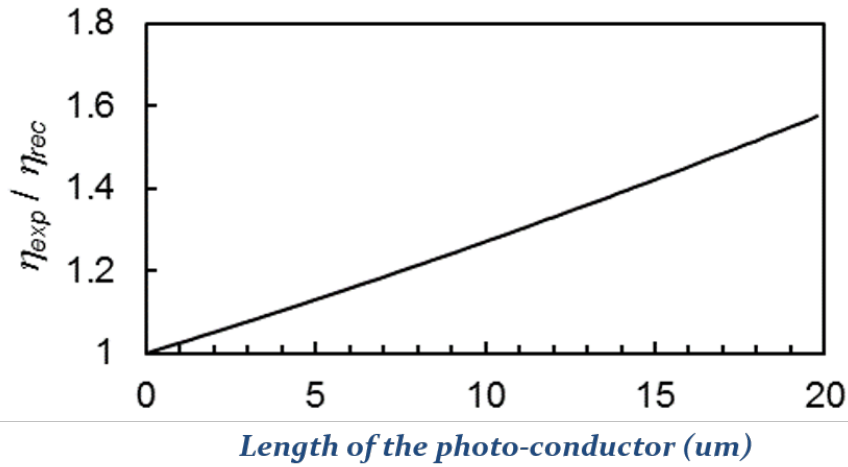


FIGURE 4.12: Evolution of η_{exp} on η_{rect} over the photo-conductor length

We can see that for lengths of the order of $20\mu m$, the ratio is approximately 1.6, which means that the R_{off} on R_{on} ratio is optimized using the exponential shape.

In order to have a more accurate comparison, we may consider comparing a rectangular photo-conductor with an exponential photo-conductor, where: $w_{rect} = |W_{exp}|$ with $|W_{exp}|$ being the width average over the length of the exponential photo-conductor, i.e.:

$$|w_{exp}| = 1/L * \int_0^L W_0 * e^{-\alpha x} dx = \frac{W_0}{\alpha L} * (1 - e^{-\alpha L}) \quad (4.26)$$

We use this value in the previous η_{exp} equation:

$$\eta_{exp} = \left(\frac{R_{off}}{R_{on}}\right)_{exp} = 1 + \frac{k * E_0 * (\mu_n + \mu_p)}{w_0 * \rho * h} \quad (4.27)$$

NB :

- For the same initial width, the exponential shape has a bigger capacitance value than the rectangular shape. However, since for these photo-conductors,

the capacitors are not very important (of the order of a few fF), we did not include the comparison here.

- For this demonstration, we considered that the electron-hole pairs are created within a very small lapse of time compared to their collection time. This approximation is valid in our case, since the optical beam we consider is about 3.4ps long, where transit time is about 167ps for a $1\mu m$ wide photo-conductor under a 1V bias.

4.2.1.3 Simulations and measurements

A. Simulations :

In order to validate this concept, we have first run measurements on Lumerical FDTD simulations.

The first simulation was run to validate the value of the absorption coefficient in germanium that we have used in our theoretical study for the given photo-conductor geometry. Indeed, as has been reported by [118], the absorption length can vary according to the photo-conductor power injection scheme.

a. Absorption coefficient

We used two different approaches:

- The first approach is to run a sweep over the length of the germanium and calculate the absorbed power through the Optical power analysis group, which returns directly the percentage of absorbed power versus injected power.
- The second approach is to use multiple 2D power monitors at different positions along the propagation direction for a long enough germanium photo-conductor. In this simulation, each power monitor measures the amount of power flowing across it.

We applied the two approaches to have a more accurate estimation of the absorbed power since the two have some degree of inaccuracy. Indeed, for the first case, the absorbed power takes into consideration the power that reflects back to the photo-conductor at the germanium-Silicon final interface. Although this setting is more similar to our real-life case, but it does not represent accurately the absorption coefficient.

The second method is built on the assumption that the power is perfectly confined within the germanium photo-conductor so that the difference in power between two successive monitors is entirely due to absorption. Although this approximation is acceptable in our case, the results of the two approaches put together give a more accurate idea of the absorption coefficient.

Within the next subsection, we will go through the two approaches simulation settings and results. The aim of this part is to explain the two methods and in the same time give the reader an idea about the Lumerical simulations settings that were used along this thesis.

Method 1:

We used for this simulation a mode source with a center frequency around $1.55\mu m$. The pulses length is approximately 40fs in order to reduce the simulation length. We do not use the option "optimize for short pulses" to avoid having a very rich spectrum because it is not necessary in our case.

The absorption analysis, i.e. "Power absorbed" analysis box, is set over the length of the germanium and a sweep is performed over this length.

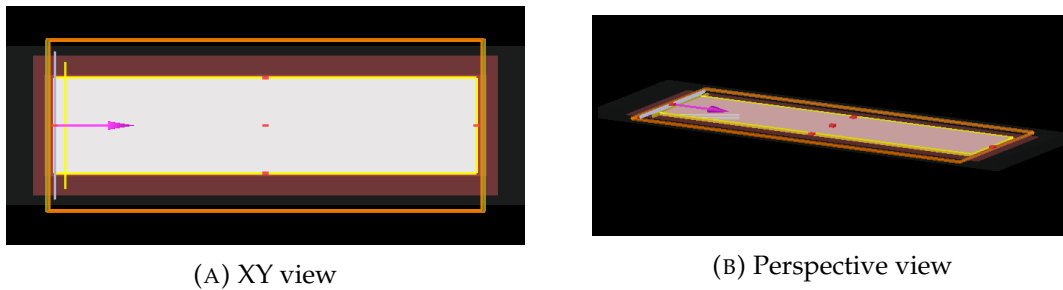


FIGURE 4.13: Views of method1 simulations on Lumerical FDTD solver

The simulation duration is chosen to be 600fs. This value is an approximation of the time it will take the energy pulse to cross the germanium photo-conductor based on its effective index.

For the input source we chose a mode source with the fundamental TE mode and an amplitude of 3.67×10^7 . Indeed, in Lumerical, only the value of the electrical field is specified in the source tab, and the real injected power can be estimated as follows:

$$P = 0.5 * \sqrt{\frac{\epsilon_0}{\mu_0}} * S * A \quad (4.28)$$

Where:

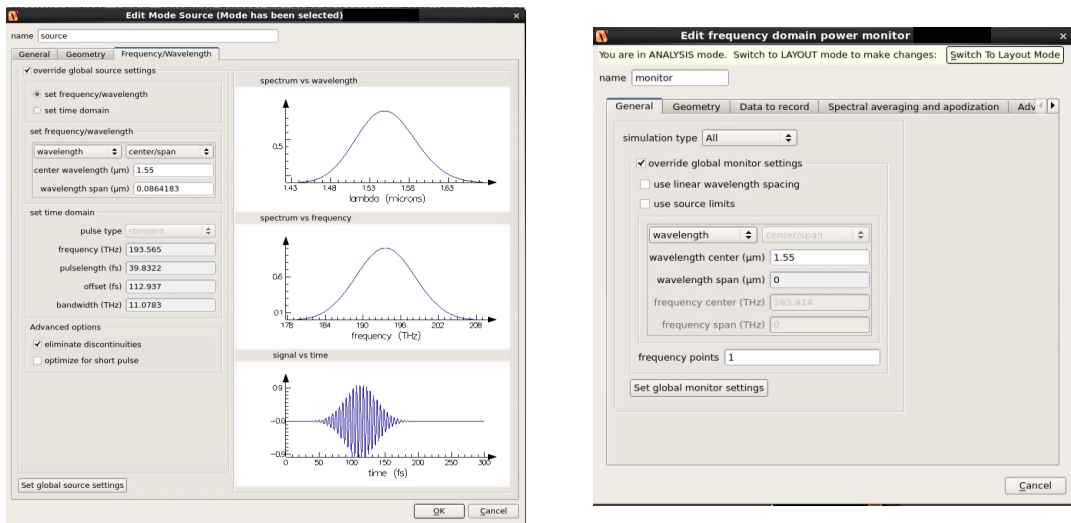
- ϵ_0 : vacuum permittivity
- μ_0 : vacuum permeability
- S : the source cross section in m^2
- A : the source amplitude value

In our case, we use a 1mW entry source, so that the amplitude is about: $3,67 \times 10^7 V/m$.

We set the value of the incident power to a known value even if the results are ratios rather than real values (the total absorbed power is reported to the incident power). This is important just to be sure that the power value is not big enough to generate nonlinear effects or to bleach the germanium.

Method 2:

We use the same settings than for the first approach simulation and we set the 2D power monitors as depicted in fig.4.14b.



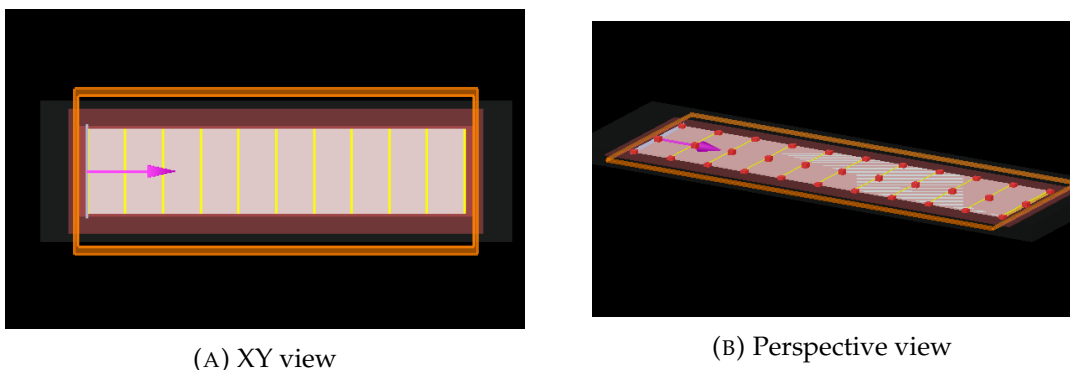
(A) Source settings for method1 and method2

(B) 2D power monitor settings for method2

FIGURE 4.14: Method2 simulation settings

We apply this approach to a $40\mu\text{m}$ long photo-conductor, with 2D power monitors positioned every $4\mu\text{m}$.

The results of this simulation and of the first method are depicted in fig.4.16.



(A) XY view

(B) Perspective view

FIGURE 4.15: Views of method2 simulations on Lumerical FDTD solver

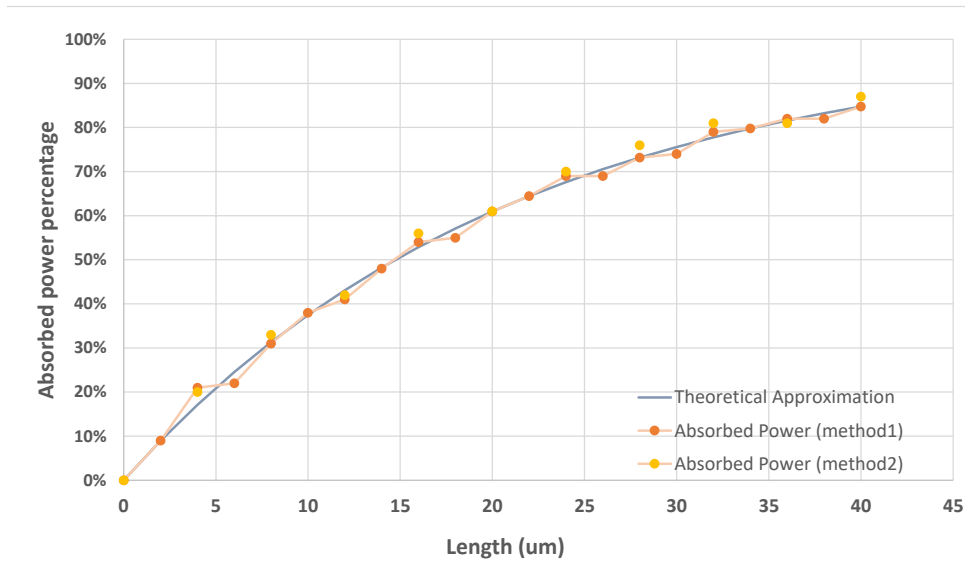


FIGURE 4.16: Absorbed power percentage over propagation length

The obtained absorption coefficient is therefore approximately equal to $0,05\mu m^{-1}$, as we could fit the latter curve with the following equation:

$$f(x) = 1 - e^{-0,05x} \quad (4.29)$$

Where x is the propagation length in μm .

b. Structure simulations

Based on the latter value of absorption coefficient, we have simulated an exponentially shaped photo-conductor with the following dimensions: $W = 9\mu m$ and $L = 10\mu m$ as a proof of concept. We compare the results of this photo-conductor to the results achieved with a rectangular photo-conductor of the same dimensions.

We have simulated the optical electrical field distribution in both photo-conductors in fig.4.17. We can already see that by the end of the rectangular photo-conductor, the intensity of the field is getting weaker compared to its exponential counterpart. The field distribution in the exponential photo-conductor is nonetheless not perfectly homogeneous, this is due to the fact that light is coupled into other modes of propagation. We can presume that, with appropriate sizing, the field distribution would remain more homogeneous by trying to size the exponential width above the fundamental mode coupling threshold (adiabatic transition).

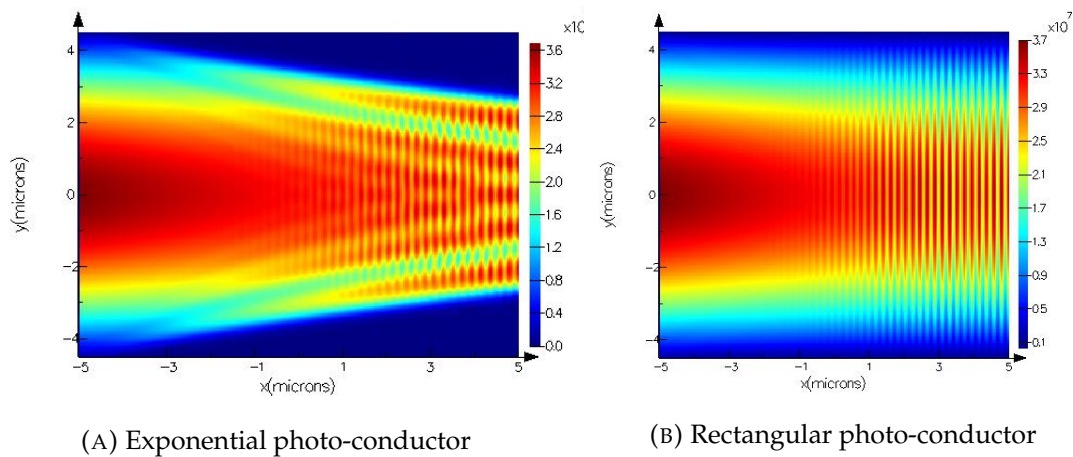


FIGURE 4.17: Optical electrical field distribution for the exponential and rectangular photo-conductors

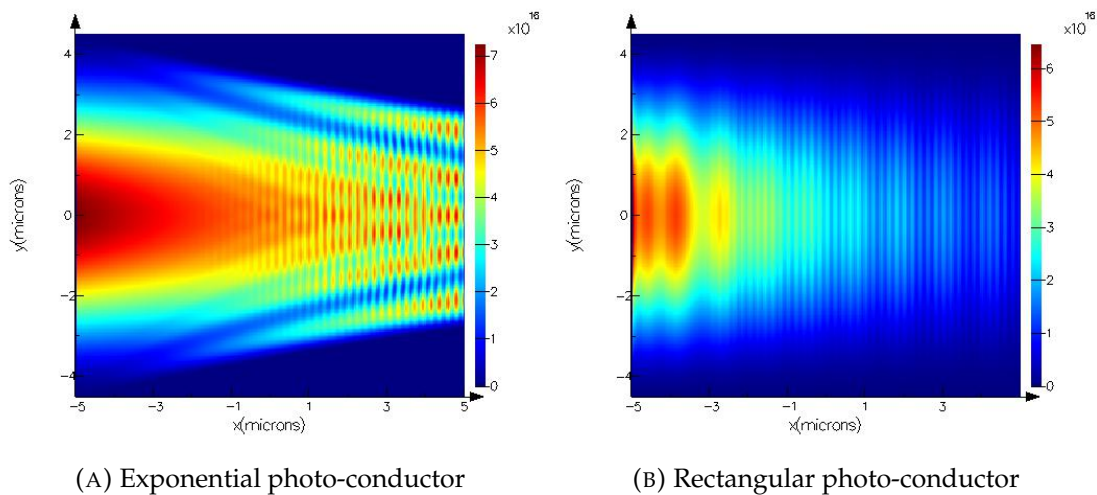


FIGURE 4.18: Absorbed power density for the exponential and rectangular photo-conductors

The effect of the exponential shape on the final performance of the photo-conductor is even more obvious in fig.4.18 where we have plotted the absorbed power density distribution. We can see that the exponential power make it possible to keep high absorbed power density values at the end of the photo-conductor.

The final short circuit current, i.e. the current that we would get assuming that all absorbed photons generate electron-hole pairs and that all of the pairs get collected (before combining and with no additional gain) is the same for both structures: $13,09mA/m^2$.

Note here that the value of the short circuit current, calculated through the "Generation rate" analysis box, is estimated by considering the z direction as the electrical field application direction i.e. by considering a vertical photo-conductor scheme, which is not our case. The current is therefore reported to the x and y

dimensions of the photo-detector, which are the same for the two structures (we use rectangular "Generation rate" analysis box for the exponential shape as well), but must be reported, for sake of accuracy to the z and x dimensions. We will not bother doing this estimation since the short circuit current has no physical meaning anyway and that it only helps give an idea about the total number of photo-generated pairs in both structures.

The latter means that the total generated pairs number is the same between the two structures. Knowing that the average width of the exponential shape is smaller than the rectangular one, then the total on current in the exponential shape is higher than the rectangular ones (Ron is smaller for the exponential shape than for the rectangular shape).

We have performed a sweep over different widths and lengths of the photo-conductor and the results are approximately always the same: the photo-generated number of pairs is the same between the two structures.

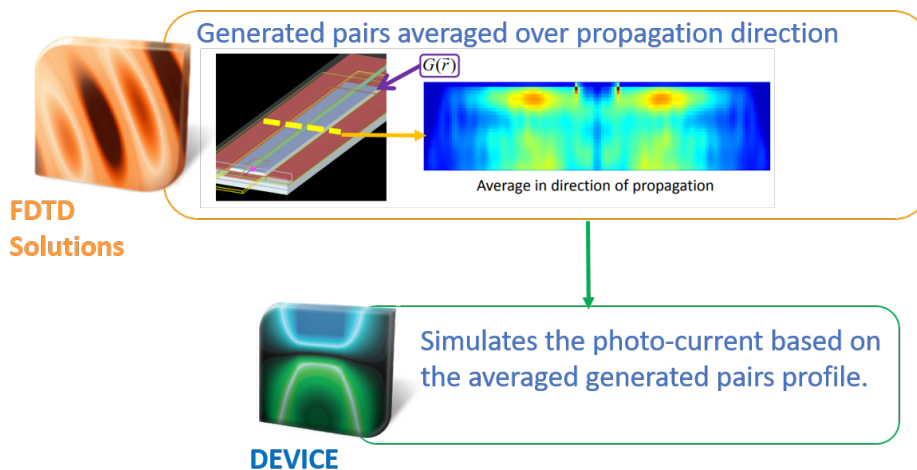


FIGURE 4.19: Lumerical optoelectronic simulation protocole

The final validation step was to inject the results of the photo-generation into DEVICE: Lumerical opto-electronic simulation software. The aim of this last step is to compare the photo-generated currents in the two structures.

However, two points should be taken into consideration:

- Only 2D simulations are possible with Lumerical DEVICE. Indeed, the generation rate GDS (Graphic Data System) that is generated by FDTD is averaged over a given dimension of the photo-conductor when it is imported into DEVICE, usually over the propagation direction, see fig.4.19. This solution is generally a good approximation for the photo-detectors that keep the same profile along the propagation direction. However, this does not work for the exponential case.

- An accurate photo-current simulation must be based on a first fit of the device's dark current response. However, for photo-conductors, the dark current depends very much on the carrier's lifetime, which, as we saw, is hard to determine in our case. Therefore, we will use germanium model values that are accepted in literature and will only take into consideration the final ratio of the two devices' photo-currents.

In order to overcome the first limitation, we have chosen to make multiple divisions along the exponential photo-conductor device and simulate the photo-generation rate of each of them in FDTD as in fig.4.20.

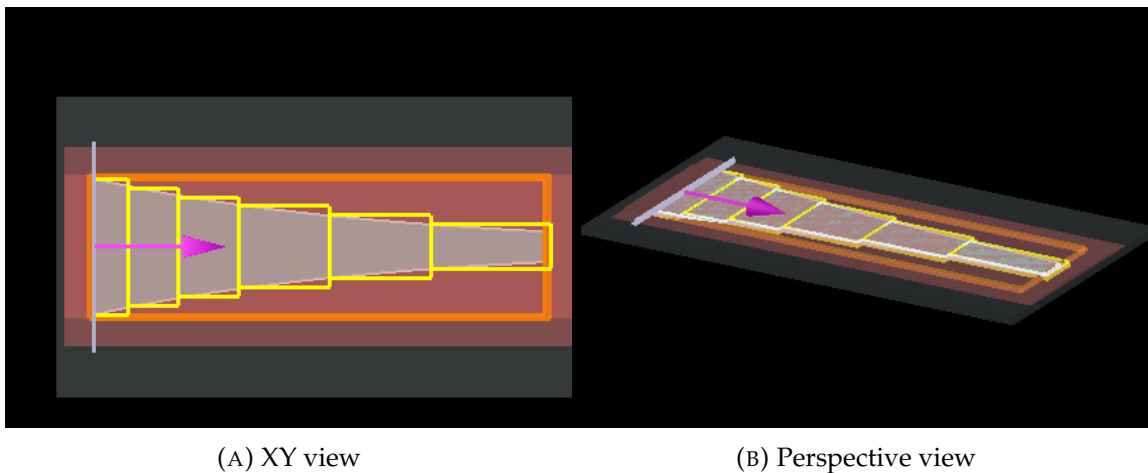


FIGURE 4.20: plots of the new work flow applied to an exponential device

The GDSs will be then imported into DEVICE, but this time, we will have a more accurate photo-generated current value since the averaging will not be done over the whole propagation dimension but rather on small sections along it.

As we said, we inject the results into DEVICE as in fig.4.21.

As we can see, in DEVICE's simulation the plugs were only put in the middle of each section because the electrical simulation will be a 2D simulation anyway. It is worth noting that we added two longitudinal metal contacts in the edges of the device to stand for the ground contact.

The germanium electrical model parameters are depicted in fig.4.22:

B. Measurements :

We tried to implement the exponential shape on silicon in order to validate the concept with measurements. However, applying the exponential shape was not possible because of process limitations. Indeed, only steps of more than $0,6\mu m$ are achievable with germanium epitaxy on silicon, which means that the exponential shapes could only be approximated with staircase-effect structures, see fig.4.25.

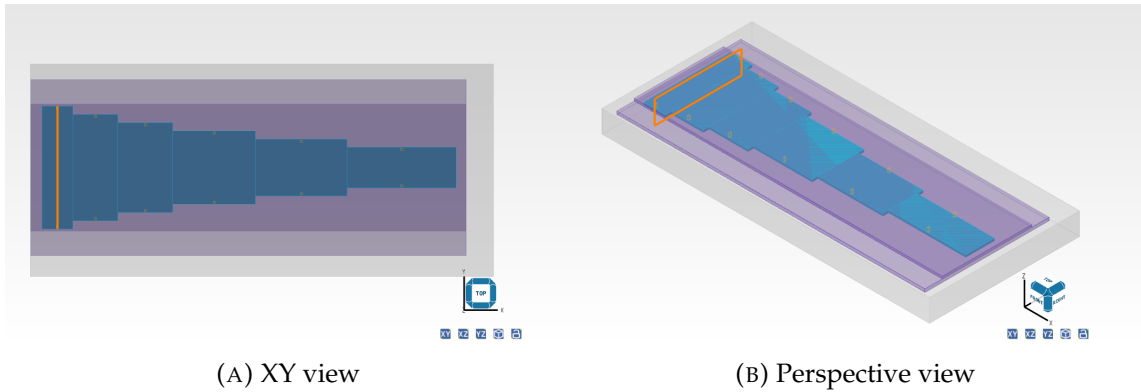


FIGURE 4.21: Plots of the exponential photo-conductor in for DE-VICE simulations

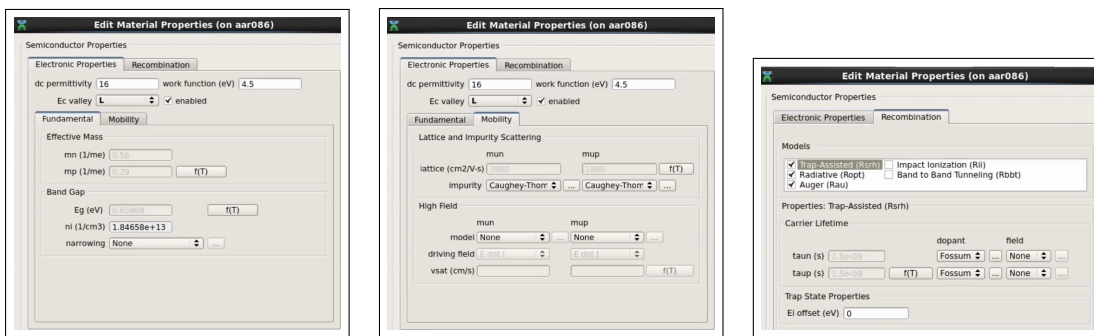


FIGURE 4.22: Germanium DEVICE model

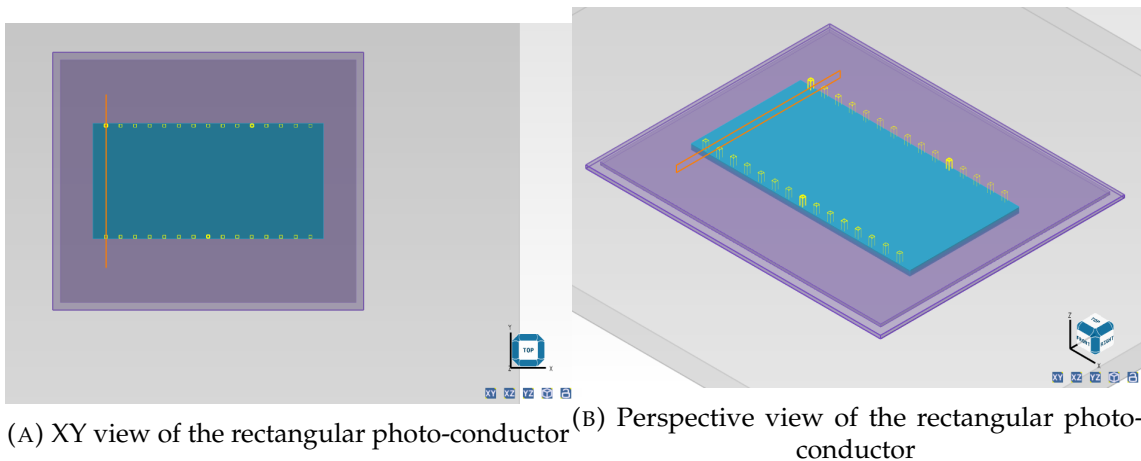


FIGURE 4.23: Plots of the rectangular photo-conductor in for DEVICE simulations

We have implemented three different structures in GenerationB mask. The detailed dimensions of the three structures are given in appendixA. Then we have characterized these devices under pulsed light and for different DC biasing values. The experimental set-up is similar to the one presented in the previous chapter. The results are compared with those of subdie11 which dimensions are: $w = 7.66\mu m$ and $L = 15\mu m$.

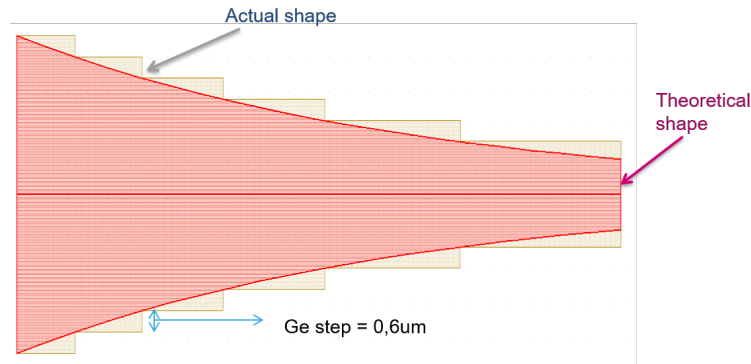


FIGURE 4.24: Exponential photo-conductor: implemented versus theoretical shape

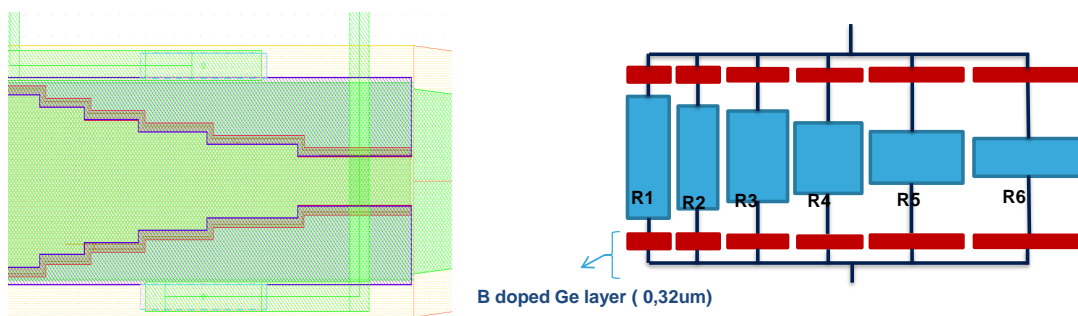
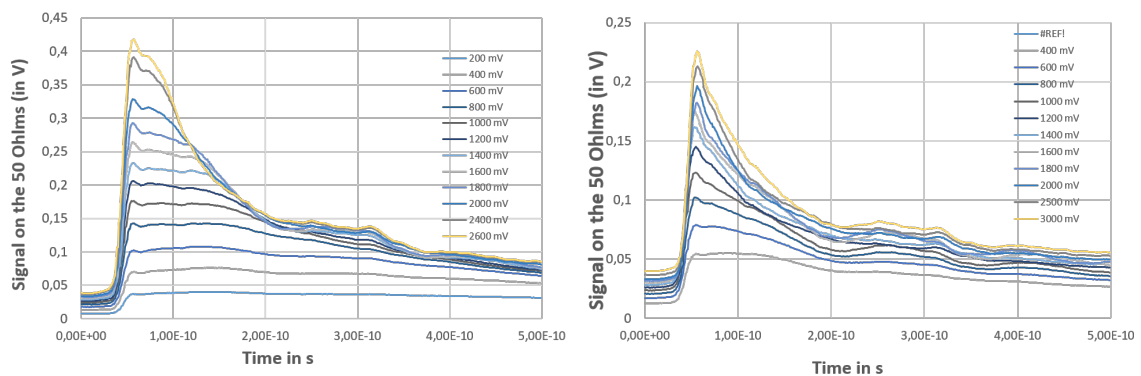


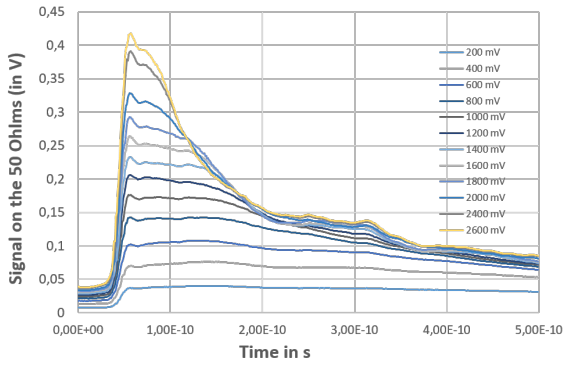
FIGURE 4.25: GenerationB subdie8 break down



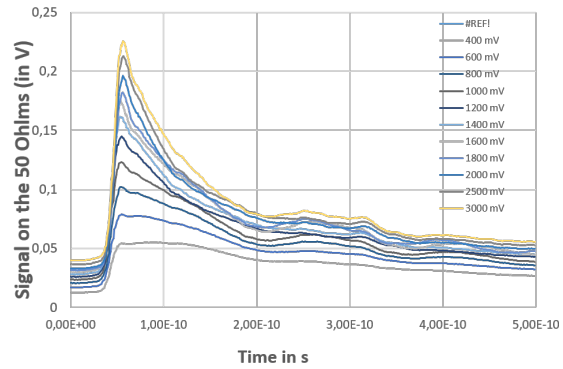
(A) Pulsed laser response of the exponential subdie (subdie10, generation2) for different biasing voltages
 (B) Pulsed laser response of a rectangular subdie (subdie11, generation2) for different biasing voltages

We can see that the exponential subdie has a lower value of R_{on} since the peak voltages it reaches are way higher than subdie11.

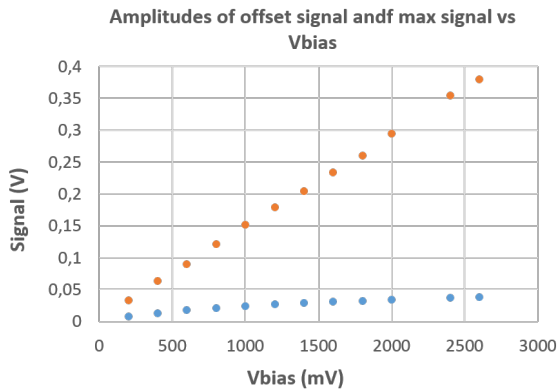
We can also see that the peak voltage and offset voltages are more linear with the biasing voltage than in the case of subdie11. This can be explained by the fact that in subdie10, velocity saturation is reached for lower values of biasing voltage. While in the case of subdie11, velocity saturation is reached for some segments of the photo-conductor while the others are still linear.



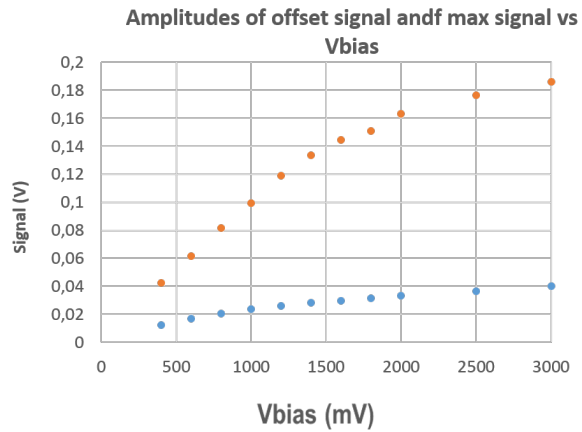
(A) Pulsed laser response of the exponential sub-die (subdie10, generation2) for different biasing voltages



(B) Pulsed laser response of a rectangular sub-die (subdie11, generation2) for different biasing voltages



(A) Peak voltage and offset voltage variation with biasing voltage for subdie10



(B) Peak voltage and offset voltage variation with biasing voltage for subdie11

4.2.2 Other geometries

We have also thought of other geometries to resolve the R_{off} on R_{on} ratio problem. Indeed, as we saw before, the length of the photo-conductors along the propagation axis is necessary for the optical power to be fully absorbed. However, this same length makes the off resistance smaller. The latter trade-off has a big impact on the R_{off} on R_{on} ratio.

We can work around the latter trade-off in many ways:

- **Method 1:** Separate the propagation direction from the electrical contact application direction: this amounts to say that the light must propagate along a direction that does not decrease the total resistance of the photo-detector, in other terms: light must propagate along the electrical field lines.

In fig.4.29, light is coupled into the germanium photo-conductor through its electrical contact side. The length of absorption in this case is exactly equal

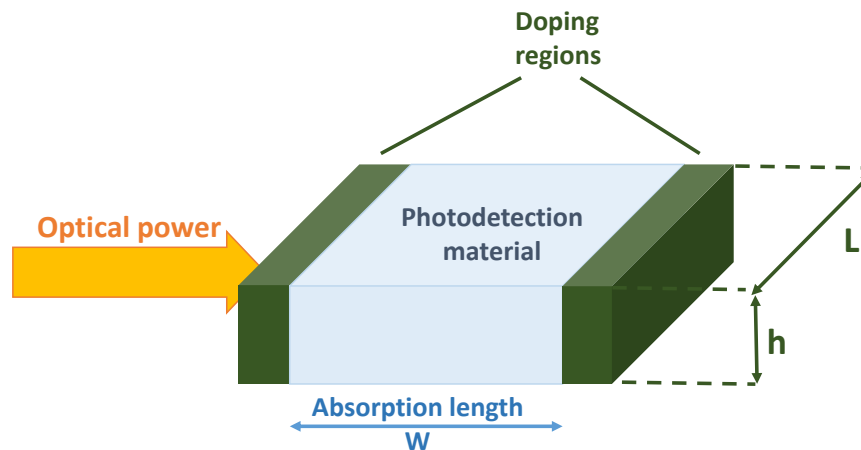


FIGURE 4.29: Upper injection photo-conductor scheme

to the width of the photo-conductor, which makes it possible to increase the width (the resistance) and the absorption length with no trade-offs.

The main drawback of this structure is the fact that light crosses first the germanium doping regions, that are connected to the metal vias, which do cause important losses.

- **Method 2:** Use Distributed Bragg reflectors to shorten the propagation length:

The idea behind this method is simply to make light propagate along the photo-conductor and to reflect the leftover energy back into the photo-conductor using a distributed Bragg mirror as depicted in fig.4.30.

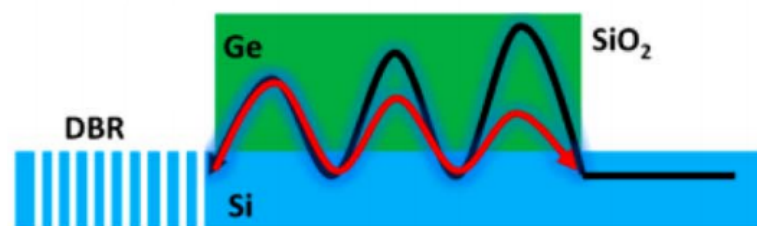


FIGURE 4.30: Optimized germanium photodiode using a DBR, courtesy image from [120]

The advantage of this method is obviously to use shorter photo-conductors for the same photo-generated current. Indeed, we can reduce the length of the propagation down to half the absorption length while having the same current outcome in ON state.

This method has been already used for the case of photodiodes .[119,120] and results in a 25% increase in the responsivity in the case of a $5\mu\text{m}$ long photo-detector, .[120].

- **Method 3:**

Using multiple photo-conductors in series:

The idea of this new structure is to use multiple photo-conductors, connected electrically and optically in series as depicted in fig.4.31.

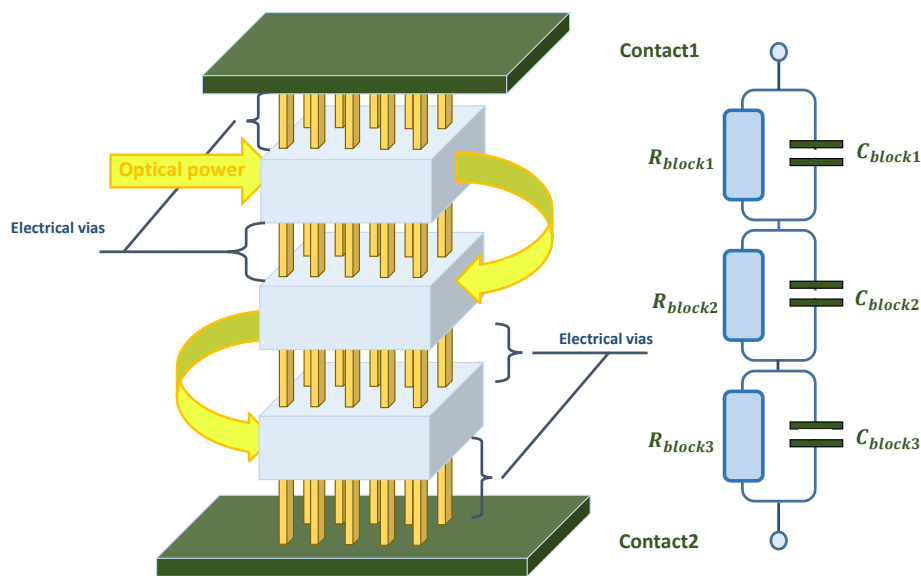


FIGURE 4.31: Upper injection photo-conductor scheme

Indeed, the absorption length in this case is the sum of the blocks lengths, mainly $3*L$. However, the equivalent resistance is only L long, because the three blocks are connected in series electrically, so that the resistances add up.

We expect this circuit to be also efficient when it comes to transit time. Indeed, if we suppose that the three photo-conductors generate the same density of electron-hole pairs in On state, i.e. they have the same R_{on} value, then for an applied voltage V , each photo-conductor is submitted to an electrical field: $E = \frac{V}{3W}$ where W is the width of each of the three photo-conductors in series.

Therefore, the transit time will be: $t_{transit} = \frac{W}{\mu_0 * \frac{3W}{V}} = \frac{3W}{\mu_0 V}$. This is three times less than the transit time of the equivalent photo-conductor (photo-conductor of width=3W).

For sake of accuracy, the transit time is not exactly equal to the given value because:

- Some voltage is lost on the electrical connections between the different photo-conductors.
- We should account for the time light takes to cross the waveguides. In the case of $10\mu m$ long waveguides, it takes light: 116 fs to reach the middle photo-conductor. This value remains negligible compared to the total transit time anyway.

a.Simulations

A first simulation in Lumerical FDTD was performed in order to validate the operation of this circuit. The main purpose of these simulations being to have an estimation of the decrease of resistivity of the middle photo-conductor compared to the side ones.

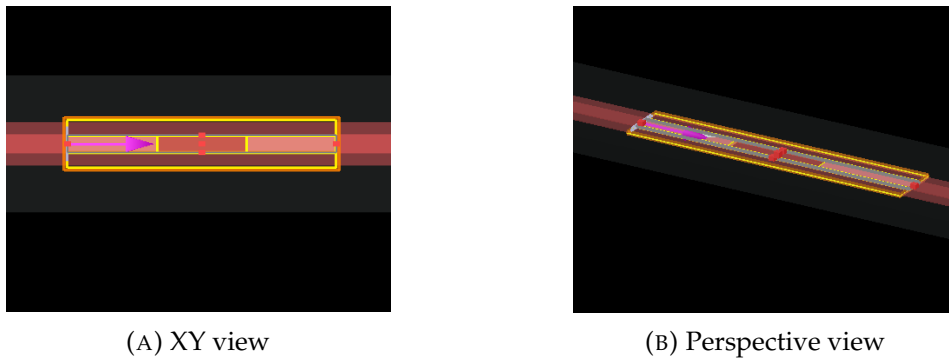


FIGURE 4.32: Views of the FDTD simulation of the series geometry

As depicted in fig.4.32, only two photo-conductors are simulated. Indeed, the series circuit is made of three photo-conductors in series with double injection of light, i.e. light is first split through a 3dB coupler and injected into the side photo-conductors.

We then only need to simulate one side photo-conductor and the middle one in order to have an estimation of the decrease of resistivity.

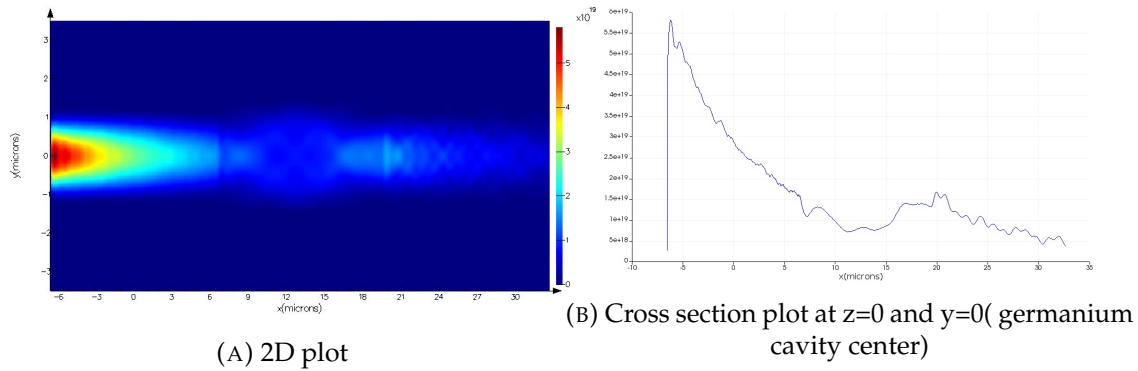


FIGURE 4.33: Power density plot in the series photo-conductors geometry

The settings of the FDTD simulation are the same than the ones used for the exponential photo-conductor. In the FDTD simulation, we first used a "frequency-domain field and power monitor" to visualize the propagation of power across the structure. The 2D plot of power propagation is depicted in fig.4.33a.

To have a clearer idea about the way power propagates across the structure, we plotted in fig.4.33b the power density on a section along the propagation axis, mainly at $y=0$ and $z=0$, which matches the middle of the germanium cavity.

We can see that by the end of the first photo-conductor, i.e. at $x = 6.5\mu m$, the power density remaining is less than half the one we started with: 5.6×10^{18} versus 1.6×10^{19} . This does not match exactly the theoretical expectations based on the absorption coefficient (we expect the remaining power to be half the initial one).

However, these values may be deceiving because they only give an idea about the power density value at a certain point and do not reflect the value of the total power that is injected into the photo-conductors. Indeed, light may have been coupled into different modes of propagation in the middle photo-conductor, in which case the latter values would not be representative of the ratios between the total absorbed power in the two photo-conductors.

We have therefore used two "absorption per unit volume" boxes, one for each photo-conductor. These are analysis groups that measure the spatial absorption profile. The total absorbed power in the first photo-conductor is 70% and only 10% in the second photo-conductor.

The latter values do not obviously match the theoretical expectations: 52% of power absorbed in the first photo-conductor and 25% in the second photo-conductor.

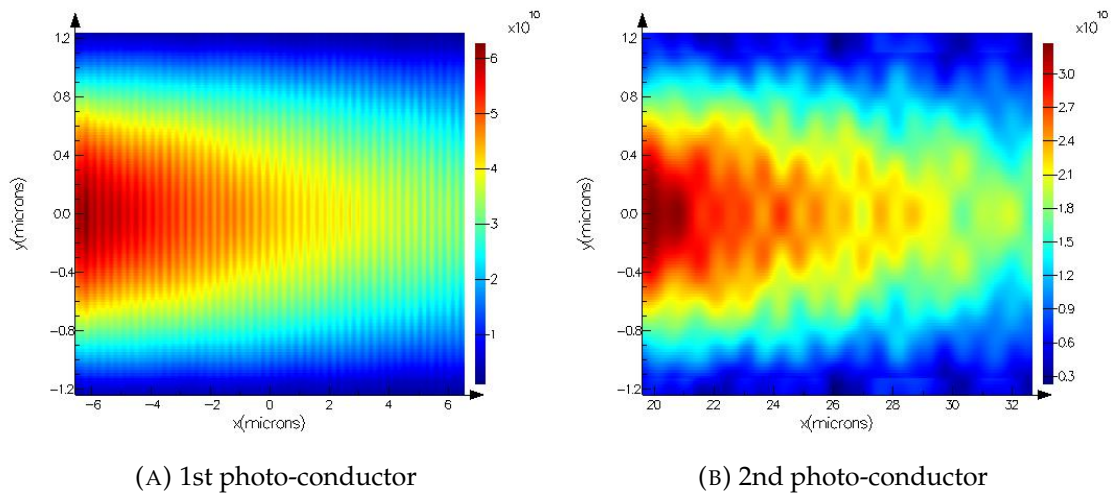


FIGURE 4.34: Optical electrical field distribution in the two photo-conductors in series

In order to better understand this discrepancy, we have plotted the optical electrical field of both photo-conductors in fig.4.34. We can see in fig.4.34a, that there are ripples of the electrical field.

This is due to light reflection at the silicon-Germanium interface. One can argue that these reflections were taken into consideration in the absorption coefficient calculation that we made earlier, however, in this case light is reflected not only at the first interface but also at the input of the second photo-conductor and again at its second edge.

It is worth mentioning that the reflections are attenuated by the angle due to the cavity etching. In fig.4.35, we can see the etching angle in the germanium-Silicon interface.

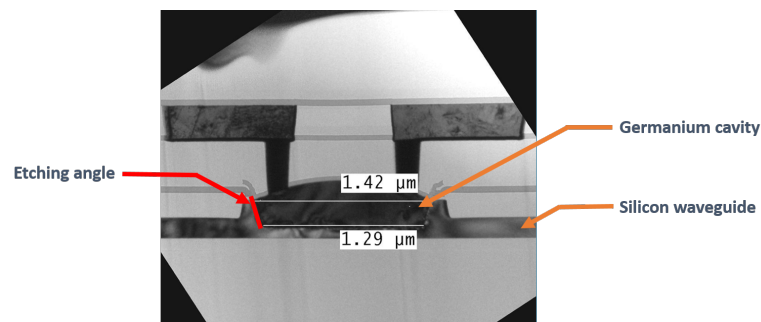


FIGURE 4.35: Cross section of a germanium photo-conductor

This can also be seen on the absorbed power plot in fig.4.36. Here again, we can see the ripples and they are even clearer in the cross section plot in fig.4.36b. The generation rate profiles show the same ripples (see fig.4.37).

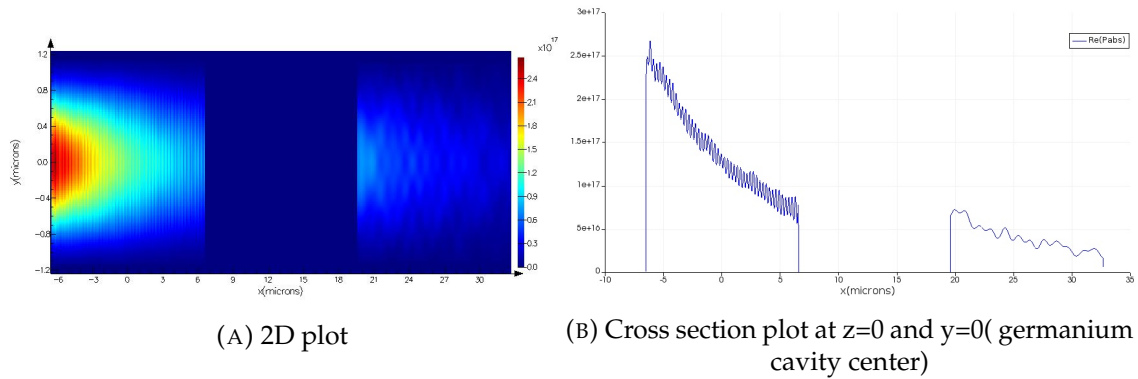


FIGURE 4.36: Absorbed power density across the series photo-conductors

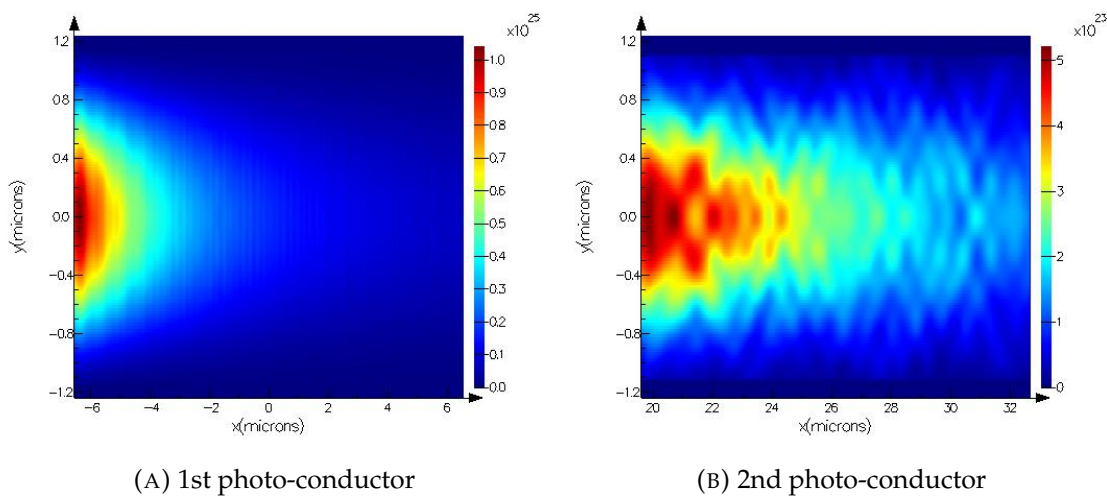


FIGURE 4.37: Generation rate in the two photo-conductors in series

The final short circuit current does also reflect the same ratio between the two photo-conductors. We have a short current circuit of for the first $50, 5\mu A/m^2$ photo-conductor and $7.2\mu A/m^2$, which matches the power absorbed ratios.

The simulations show that the resistivity decrease of the middle photo-conductor is $2/7$ of the side photo-conductors (photo-generated currents ratios). This is to say that if we were to inject an amount of power x in the total structure (x is first split then $0.5x$ is injected at each side), then 35% of x is absorbed in each side photo-conductor and only 14.3% x is injected into the middle photo-conductor. We will check these values with the measurements in the next section.

b. Measurements

We have designed two circuits with this structure as depicted in fig.4.38. The different blocks are connected together with a layer of metal which implies the use of vias. This may not be the most optimized electrical connection,

but we chose it because the other alternatives, mainly the one presented in fig.4.31, would have induced more technology-related drawbacks.

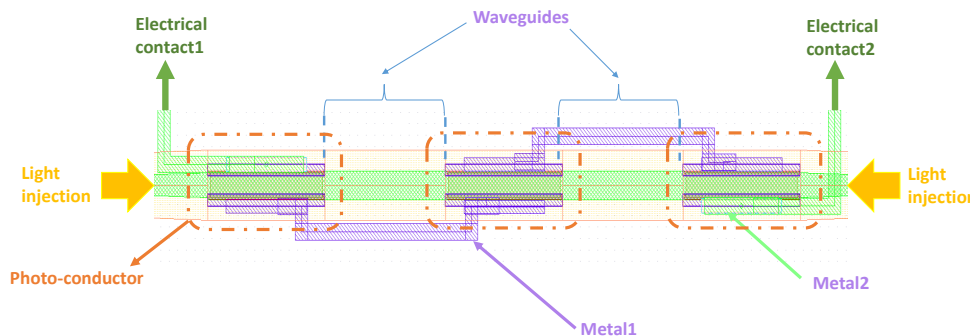


FIGURE 4.38: Scheme of subdie2 from Generation2 circuits

The dimensions of the photo-conductors are as follows:

Subdie	Width(μm)	Length(μm)
2	1.3	13.07
4	2.2	13.07

We have first run OFF measurements of the two subdies along with continuous wave ON measurements at $P=13dBm$ at $1550nm$. We depicted the results of subdie4 in fig.4.39. Subdie2's results follow the same tendency with the following average measurements: $R_{off} = 2330\Omega$ and $R_{on} = 489\Omega$.

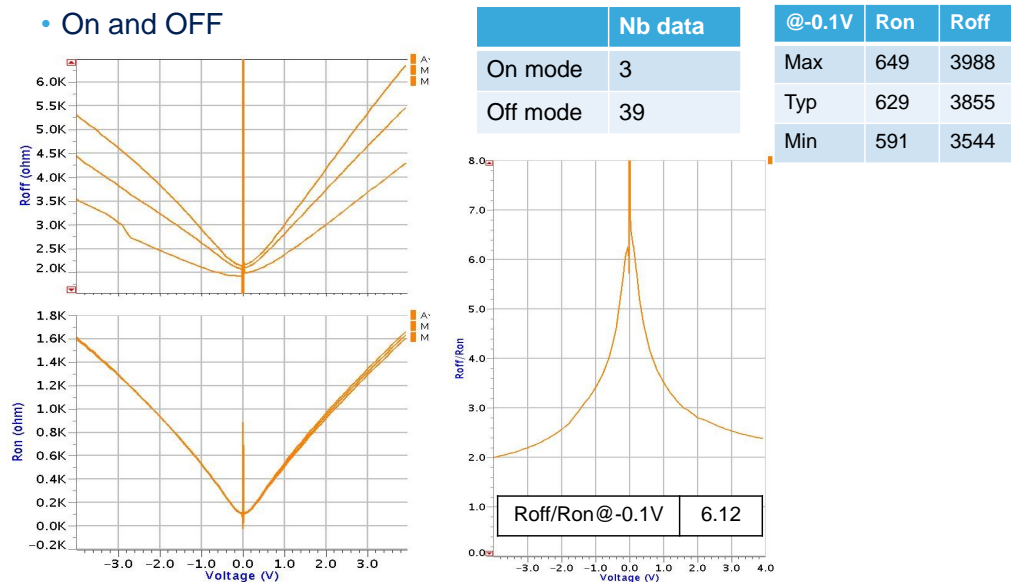


FIGURE 4.39: Generation2's subdie4 off measurements and CW on measurements

If we consider the simulations that we have performed in Lumerical beforehand, then we can already make conclusions about the R_{on} values of the

photo-conductors. Indeed, we saw that the photo-conductors resistances have the following ratios: $R_{middle} = \frac{7}{2} * R_{side}$.

We have the following R_{on} values (taken at 0.1V and at P=13dBm):

Subdie	$R_{middle}(\Omega)$	$R_{side}(\Omega)$
2	88.9	311
4	114	400

As we can see, up till now, the efficiency of these structures in optimizing the R_{off} on R_{on} ratio has not been demonstrated.

The ratio R_{off} on R_{on} of subdie2 (subdie4) structure for example is only 4.7 (6), while it is for example 17 for a regular subdie of dimension: $w = 3.3\mu m$ and $L = 13.07\mu m$ (subdie3 of generation2).

In order to validate this circuit's operation, we have run pulsed laser measurements. For sake of comparison, we considered a regular subdie with the following dimensions $W = 8.36$ and $L = 15\mu m$ (subdie11). The R_{off} and R_{on} measurements under continuous light for the said subdie are given in fig.4.40.

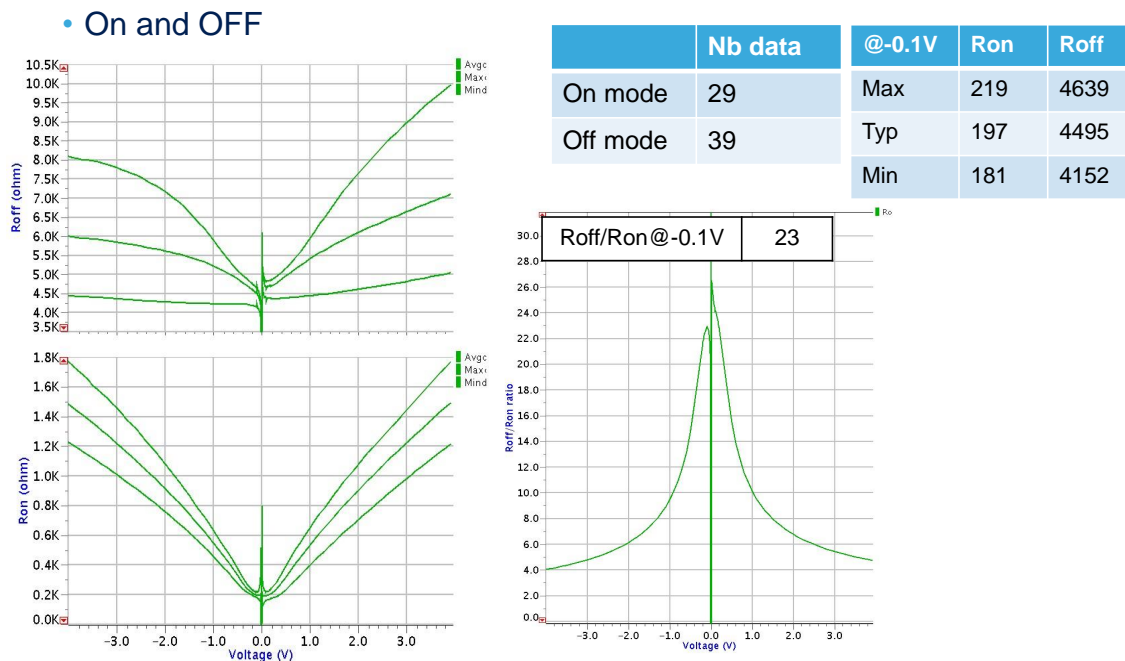
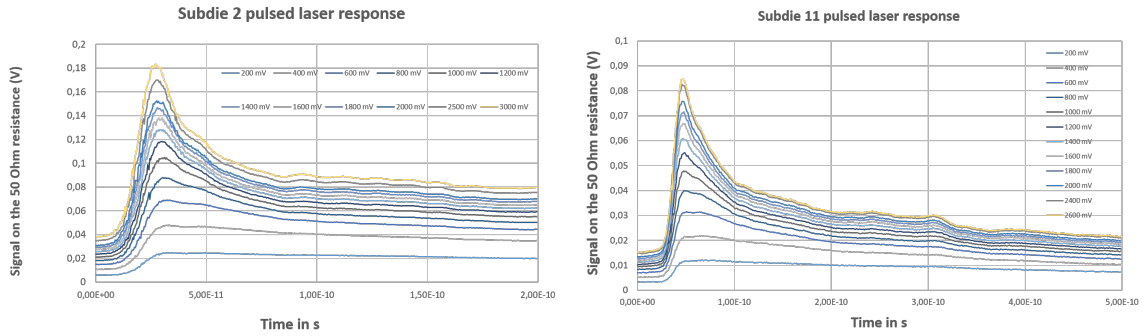


FIGURE 4.40: Measurement results of subdie11 under continuous light

The pulsed laser measurements of subdie2 and subdie11 have been performed and the results are plotted in fig.4.41.



(A) Subdie 2 pulsed laser measurements

(B) Subdie11 pulsed laser measurements

FIGURE 4.41: Plots of subdie2 and subdie11 pulsed laser measurements

We can first see that the peak voltages of subdie2, for different bias voltage values, are always higher than peak voltages of subdie11, which goes to say that R_{on} values of subdie2 are smaller than those of subdie11. Note that under continuous light the R_{on} value of subdie11 is much lower than subdie2: 197Ω for subdie11 versus 489Ω for subdie2.

The only plausible explanation is that under pulsed light, the energy is not totally absorbed within the side photo-conductors, i.e. the energy level is higher than the germanium bleaching threshold. Therefore, the leftover energy that is injected into the middle photo-conductor is high enough to lower its resistance to way less than the theoretical 0.35 of the side photo-conductor resistance.

c. Conclusion

The series photo-conductors structure may be a good candidate based on the pulsed light measurements, mainly the peak voltage values. However, we should have optimized the length of the photo-conductors more so that the resistance of the middle photo-conductor is exactly the same as the side ones. No clear conclusions can be drawn when it comes to the fall times as it seems that multiple processes are involved in the decaying response of the device. However, as can be seen in fig.4.41, the smaller width of the series photo-conductor does shorten the very beginning of the decaying time of the pulsed response.

4.2.2.1 Conclusion

We have investigated a panel of different techniques to increase the R_{off} on R_{on} ratio. We can see that the last technique, mainly the series photo-conductors

technique is quite promising. However, more work has to be done in order to fully characterize the efficiency of this technique since it is only relevant under pulsed illumination.

4.2.3 Counter-doping

The second approach that we have used to increase the R_{off} on R_{on} ratio is to use an N-type counter-doping to circumvent the p-type residual doping. For this technique, we have used several combinations of injection energies and doping doses.

The used counter-doping parameters are as follows:

In fig.4.42, we have plotted the measurements of the dark resistance of subdie3, for which the dimensions are the following: $W = 3.3$ and $L = 13.07\mu m$. In the said figure, Subdie3 curve stands for the average resistance variation over voltage for the subdie before counter-doping.

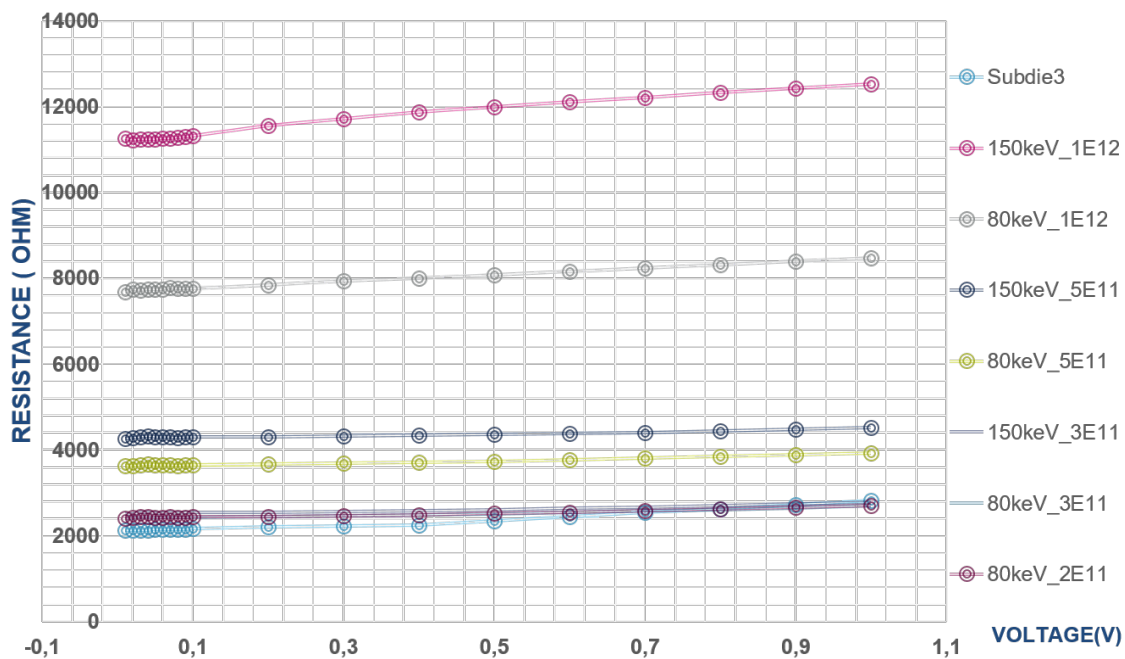


FIGURE 4.42: Subdie3 R_{off} for different voltages and different counter-dopings

We can see that the higher the counter-doping dose, the bigger the resistance. The latter seems also to increase with the injection energy.

The increase in the resistivity of the subdies with the counter-doping may be explained through two different hypotheses:

- **Hypothesis 1:**

One may argue that adding N-type doping should allow for a decrease in the resistance value since more charge carriers are available for conduction. However, these new charge carriers, electrons in this case, recombine with the already existing holes in the material and therefore reduce the total conductivity of the material.

Higher injection energies allow for a better activation of the doping material which may also explain the resistance increase with the injection energies.

- **Hypothesis 2:** The counter-doping may introduce damages on the crystal structure which could explain a decrease in the total conductivity. The higher the doping dose/ injection energy, the more damaged the crystal is, which fits perfectly with the obtained results.

One way to know which one of the two hypotheses holds true is to perform on measurements. Indeed, in case the crystal is damaged by counter-doping, we may expect a decrease in the on current as well.

On measurements were indeed performed and we have obtained the same values of on resistances than the no-counter-doping ones. This means that counter-doping is an efficient solution to circumvent the residual p-doping and artificially increase the R_{off} on R_{on} ratio.

The dependency on voltage and the R_{off} curve tendency seems to be the same though for all the counter-doping combinations.

In fig.4.43, we have plotted The measurements were performed at STMicroelectronics labs (see fig.4.44) under a top hat in order to protect the subdies from the wide spectrum lamps light. We used a Keithley 2700 Multimeter/Data acquisition system.

The final summary given in fig.4.45 is based on the average resistance values of all the subdies. In this table, we have reported, for each counterdoping setup CD the following ratio: $\frac{R_{offCD}}{R_{off_0}}$, where R_{offCD} is the off resistance with the counter-doping setting CD and R_{off_0} is the initial off resistance.

Since we have reported that the R_{on} values do not change with the counter-doping, then we can consider that the ratios in the summary table describe optimization of the R_{off} on R_{on} ratio that the counter-doping achieves.

We can see that a ratio of 6 is achievable by using a counter-doping of 10^{12} and an injection energy of 150keV. It is important to note that the values of the counter-doping were chosen by STMicroelectronics and are not essentially the optimal choice in our case.

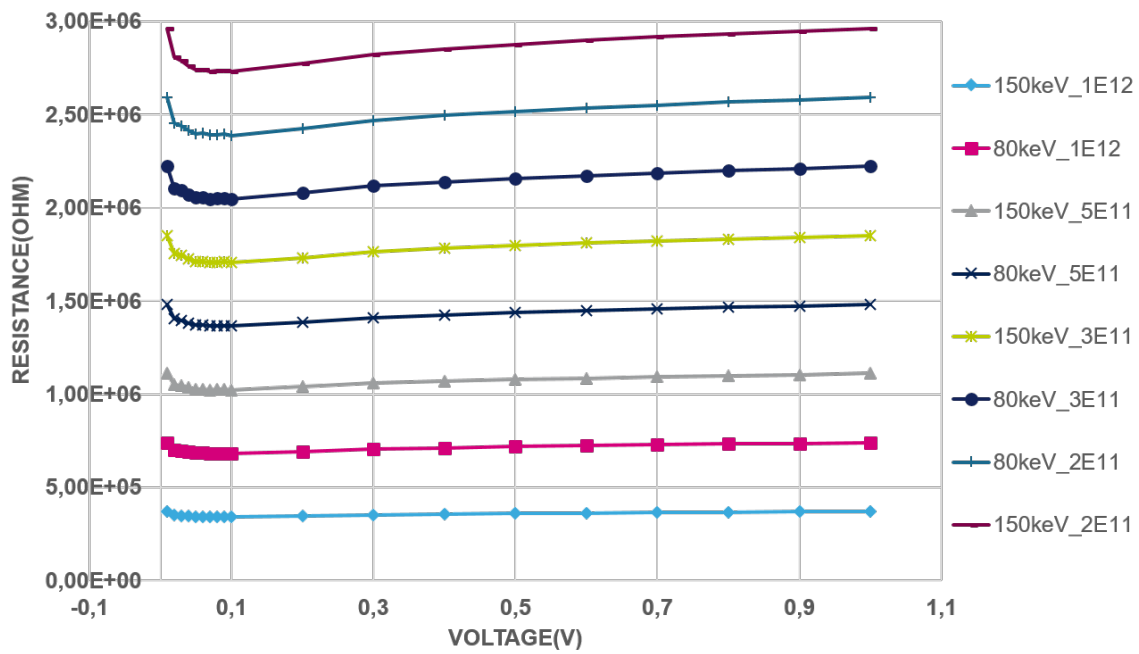


FIGURE 4.43: Subdie7 R_{off} for different voltages and different counter-dopings



FIGURE 4.44: Subdie3 R_{off} for different voltages and different counter-dopings

Doping/Energy	1,00E+12	5,00E+11	2,00E+11	3,00E+11
150keV	6,15	2,23	1,51	1,29
80keV	4,73	1,9	1,04	1,05

FIGURE 4.45: Summary of the R_{off} on R_{on} ratios obtained with different counter-doping combinations

4.2.4 Workaround circuit

In order to resolve the problem of the low R_{off} to R_{on} ratio, we can also use an electrical workaround circuit rather than try to change the optical performance of the photo-conductors as was done throughout the previous solutions. As was highlighted in section 1, this low ratio impacts the jitter validation and therefore an alternative solution to overcome this problem would be to have an ADC clock that has exactly the same period error than the sampler clock at every new clock rising edge, this way there is always the same time interval between the moment when the signal is held in the hold capacitor and the moment it is re-sampled by the ADC. This would allow us to trace back only the sampler jitter rather than measuring the sampler and the ADC clock jitter.

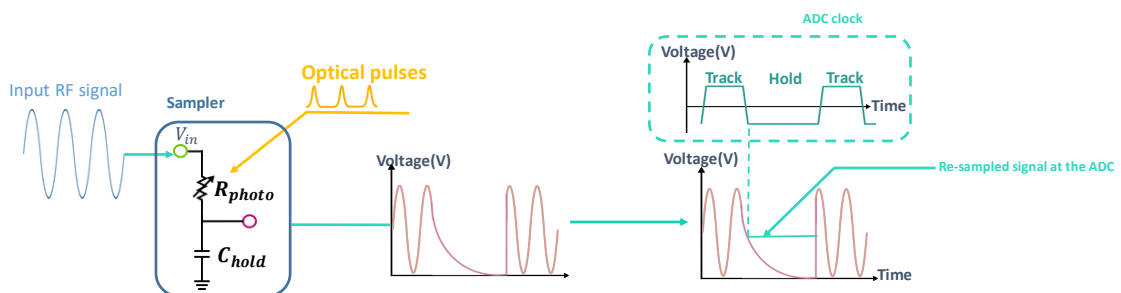


FIGURE 4.46: Workaround circuit concept illustrated

Now practically, the up said circuit would be possible if we could split the optical pulses in two pulses A and B so that pulse A feeds the sampler circuit and pulse B feeds the ADC clock. The latter would be then made through a new circuit that would transform the optical pulses into electrical ones that are suitable for the ADC operation.

Within the forthcoming sections, we will first start by exhibiting the layout of the clock generation circuit and explaining its operation. We will eventually explain the whole sampler + ADC clock integration scheme.

4.2.4.1 Clock generation: circuit operation

The clock generation circuit main purpose is, as said, to create an electrical clock out of the laser pulses.

The circuit basic scheme is the one depicted in fig .4.47.

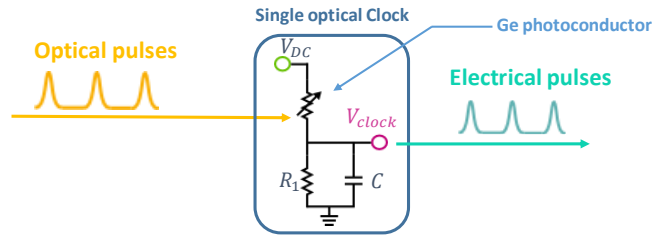


FIGURE 4.47: Clock generation circuit scheme

The circuit works as follows:

- At $t=0$, the photo-conductor resistance is equal to R_{off} . The output node voltage is equal to: $V_{clock} = \frac{R_1}{R_1 + R_{off}} V_{DC}$.
- At $t = T_1$, an optical pulse hits the photo-conductor and makes its resistance drop to: R_{on} . The output node voltage then becomes: $V_{clock} = \frac{R_1}{R_1 + R_{on}} V_{DC}$.

This new voltage is higher than the initial one, which creates a first rising edge. The time constant that rules this transition is:

$$\tau_{on} = R_{on}C \quad (4.30)$$

This is to say, the rising edge time equation is:

$$V_{clock}(t) = V_{on} - (V_{on} - V_{off})e^{-t/\tau_{on}} \quad (4.31)$$

Where:

V_{off} : is the value of V_{clock} when there is no light on the photo-conductor.

V_{on} : is the value of V_{clock} when photo-conductor is lit up.

And we have:

$$V_{off} = \frac{R_1}{R_1 + R_{off}} * V_{DC} \quad (4.32)$$

And:

$$V_{on} = \frac{R_1}{R_1 + R_{on}} * V_{DC} \quad (4.33)$$

- After $t = T_1 + T_{pulse}$, the photo-conductor resistance goes back to its original value: R_{off} . The output node voltage drops then back to V_{off} . Here again, the transition is achieved with a time constant τ_{off} where:

$$\tau_{off} = R_{off}C \quad (4.34)$$

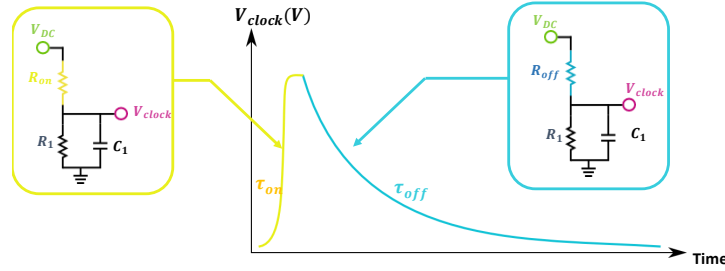


FIGURE 4.48: Clock generation operation process

$$V_{clock}(t) = V_{off} + (V_{on} - V_{off})e^{-t/\tau_{off}} \quad (4.35)$$

NB The choice of the resistor R_1 value is made as to maximize the gap between V_{on} and V_{off} . This is to have the highest possible pulses.

Say:

$$V_{gap} = V_{on} - V_{off} \quad (4.36)$$

Then:

$$V_{gap} = \frac{R_1}{R_1 + R_{on}} * V_{DC} - \frac{R_1}{R_1 + R_{off}} * V_{DC} \quad (4.37)$$

And:

$$\frac{dV_{gap}}{dR_1} = \frac{(R_{on} - R_{off})(R_1^2 - R_{on}R_{off})}{(R_{on} + R_1)^2(R_{off} + R_1)^2}$$

Therefore, in order to maximize V_{gap} , we need R_1 to be equal to:

$$R_1 = \sqrt{R_{off}R_{on}}$$

This clock circuit as easy as it may seem, demonstrates the benefits of using a photo-conductor rather than photo-diodes in our case. Indeed, in order to harvest the low jitter performance of the laser, this circuit is well suited compared to a photo-diodes made circuit in which the photo-generated current must be converted to a voltage through the use of a resistor which comes inevitably with a big noise contribution. This clock circuit was patented in [121].

4.2.4.2 Clock generation: circuit limitations

The clock generation circuit, is as said, aimed at generating a clock signal out of the optical pulses to feed the ADC circuit. The ADC that we use is a 12 bits ADC with the following clock constraints:

- Differential signal at the input.
- 600ps long pulses.
- 1V peak-to-peak signal.

Given these constraints, the clock circuit, presented above cannot feed the ADC directly. This circuit must be coupled to other ones in order to make the output signal suitable to the ADC operation. We must therefore add the following stages:

- Single to differential stage.
- 1V stage.

The full clock circuit would basically be the following, see fig.4.49:

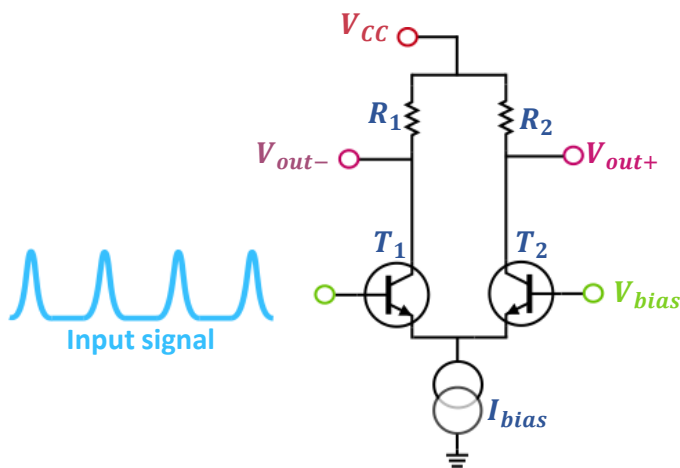


FIGURE 4.49: Clock circuit scheme

The clock signal is first injected into the base of transistor T_1 , it is then compared to the DC signal V_{bias} at the base of transistor T_2 . The differential pair steers current from I_{bias} according to the two signals comparison, which creates a differential current signal between the two output branches. The latter translates into a differential voltage signal via the output resistors: R_1 and R_2 .

The output resistors and the biasing current I_{bias} must be chosen so that the output signal's amplitude is a 1V peak-to-peak.

There are however two main problems that would hinder this circuit operation:

- The input signal is asymmetrical.
- The limited gain of this circuit.

We will explain here after the two problems and how they affect the circuit operation.

a. The input signal is asymmetrical

Let us consider, here again the following values of the optical clock signal:

R_{off}	R_{on}	C_{hold}	V_{CC}
5000 Ω	10 Ω	1pF	2V

Using these values, the output signal will rise up to $V_{ON} = 1,92V$ and will decay with a time constant of 5000ps, which means that after 600ps, the clock signal falls down from $V_{ON} = 1,92V$ down to $V_{DM} = 1,7V$, where V_{DM} stands for voltage of Decision Making as depicted in fig.4.50.

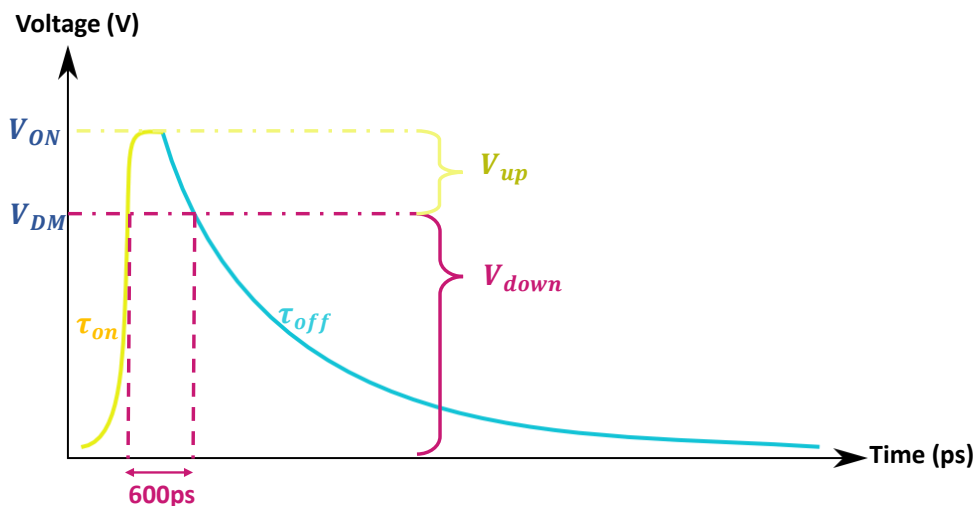


FIGURE 4.50: Clock signal versus time

As we can see, the clock signal features two parts with respect to the decision making voltage: an upper voltage V_{up} that is approximately equal to 200mV and a bottom voltage V_{down} of about 1.72V.

With these values in mind, we can see that injecting this signal into the circuit in fig.4.49 would imply first that the input signal should be DC biased again so that the input transistor T_1 does not crush when the clock signal goes to 0V at the end of its exponential decay. Say that the biasing is effectively achieved, and that the signal had been DC lifted to a biasing voltage of $V_{down} + 0.7V + 0.3V$, where the 0.7V is the operation voltage of T_1 's V_{BC} , and 0,3V is the minimum operation voltage for the current source transistor below (the transistor that would provide I_{bias}).

In this case, with our current values, the signal must be biased at 2.7V, which leaves very small room to the output voltage (for a V_{CC} of 3.3V we have only 500mV, and a maximum of 900mV at the operation limit of T_1).

One may argue that 500mV per branch is exactly the voltage room we need for an output 1V peak to peak signal. However, this is without taking into consideration the fact that we need a big gain in order to preserve the jitter performance, which will be better explained in the forthcoming paragraph.

We may be also tempted to reduce V_{down} by reducing the voltage of the clock supply: V_{CC} in order to circumvent the voltage headroom problem. However, this would reduce the V_{gap} , namely the difference between the high voltage of the clock pulse and its bottom value. This is not going to impact the gain specifications directly, but will inevitably reduce the slope of the falling edge as it is directly related to V_{gap} , which will in return make it harder to keep the jitter performance at its lowest; this final effect is the key topic of the next paragraph.

b. The limited gain of this circuit

As said before, the asymmetrical nature of the input signal leaves a 500mV to 900mV room maximum for the output signal. Now keep in mind that this circuit gain is given by $Gain = \frac{I_C R_L}{V_T}$, where $V_T = 26mV$ at $T=27^\circ C$, see [122].

The gain therefore depends directly on the product $I_C R_L$, which depends on the output voltage room.

In our case, the gain constraints are the following:

- 1V peak to peak output signal.
- a 30ps falling edge clock.

The second constraint is based on the fact that we need the clock falling edge to be as steep as possible, which will be explained below, but that we know that edges steeper than 1V/30ps cannot be properly conveyed through the output pads and the wire bonding into the ADC chips, which will be explained in a more detailed way in the next chapter, so there is no need to go higher than this value.

In order to better understand the importance of the falling edge slope on the jitter performance of the clock circuit, let's consider two clock signals with different falling edge slopes, see fig. 4.51. Let's consider a voltage noise at the power supply, and let's assume that the noise root mean square is the same for both clock circuits. The supply noise builds up on the falling edges as we can see in fig. 4.51. However, its impact is far from being the same.

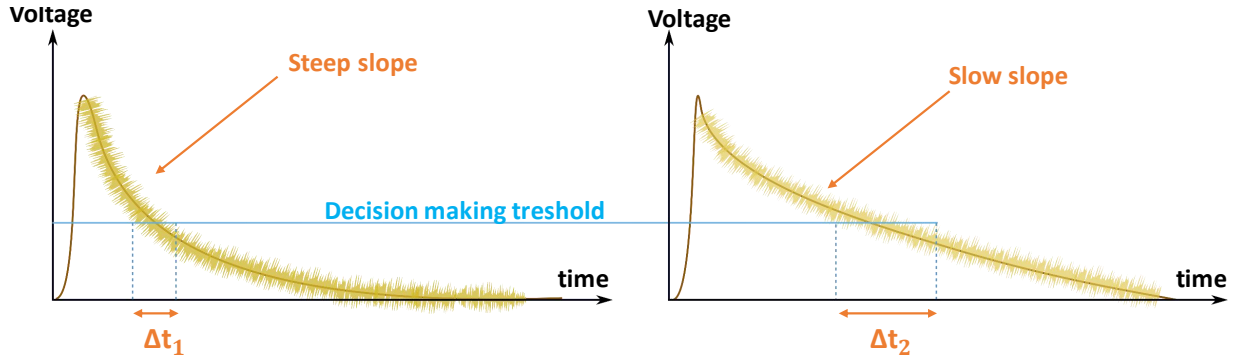


FIGURE 4.51: Effect of a steep and a slow slope on jitter

Let's consider A as the decision making voltage level, i.e. the ADC samples the signal when the clock signal crosses A .

We can see that the slow slope in fig.4.51 right causes an uncertainty at the decision taking moment that is much bigger than the one in fig.4.51 left where the slope is steeper.

In order to have an idea about the impact of the slope on the decision taking moment, we will consider two falling edges with exponential fashion with the following time constants:

- First case: $\tau_1 = 5ns$
- Second case: $\tau_2 = 20ns$

For both cases, we will consider a supply noise of $N_{rms} = 100\mu V$. The decision taking uncertainty is:

$$dT = \frac{N_{rms} * \tau_{off}}{A - V_{off}} \quad (4.38)$$

Where A is the decision taking voltage.

Say we consider: $V_{off} = 0.5V$, $V_{on} = 1V$ and $A = 0.75V$. Therefore, we have the following time errors:

- First case: $dT = 20fs$
- Second case: $dT = 800fs$

Therefore, we can see that the time errors are very affected by the clock edge slope: the slower the slope the bigger the time error.

Now that the importance of the steep falling edge has been explained, we can better see why the basic circuit scheme in fig.4.49 cannot be used. Indeed, for a falling edge of 1V/30ps, and knowing that we start with a falling edge of: $\frac{(V_{on} - V_{off})}{\tau_{off}} * e^{-600ps/\tau_{off}} = 3.58 * 10^8 V/s$, we need a gain of at least 60dB.

This means that we need to have $Gain = \frac{I_C R_1}{V_T} = 60dB$, which amounts to having: $I_C R_1$ equal to 26V, which is impossible.

One may argue here that it would be easier to increase the value of V_{CC} in order to increase the V_{gap} and therefore the slope of the falling edge, which would reduce the gain constraints on the circuit.

However, there are two limitations to this solution:

- The voltage headroom: by increasing V_{gap} , we mainly increase V_{down} as it represents 88% of V_{gap} . This will result in a smaller headroom for the output voltage as has been explained above.
- R_{on} is not constant: as explained in the first chapter of this manuscript, the value of R_{on} is not constant over voltage: the more we exceed the saturation voltage the higher R_{on} gets. This is to say that we cannot increase the supply voltage indefinitely, which puts a limitation to this solution.

Given what has been said, the clock generation circuit final scheme is updated and the new scheme will be detailed within the next section.

4.2.4.3 Clock generation: final circuit scheme

The new clock generation circuit is now made of a whole pulse shaping stage, which is in turn made of three different blocks:

- Single to differential + biasing stage.
- Amplification stage
- 1V stage

The operation of these three blocks is depicted in fig.4.52. Within the forthcoming sections, we will explain in details the operation and design constraints of each one of these blocks, the final designs will be disclosed in the next chapter.

Single to differential + biasing stage:

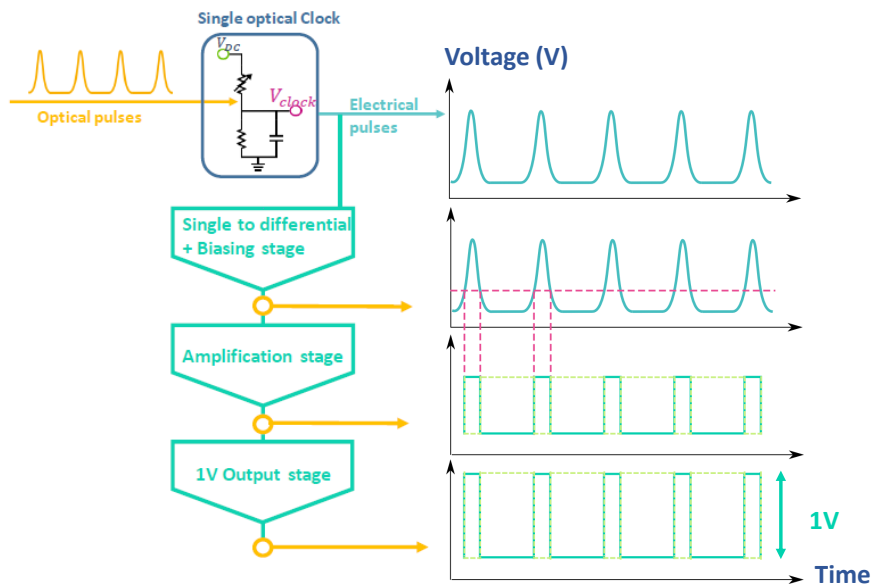


FIGURE 4.52: Pulse shaping circuit diagram

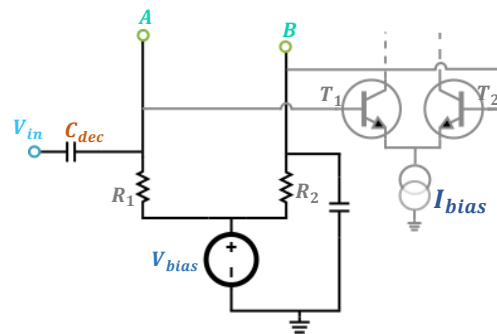


FIGURE 4.53: Basic biasing circuit

The basic design we will be using is depicted in fig.4.53

Where:

- C_{dec} : a decoupling capacitor
- R_1 and R_2 : Biasing resistors
- A and B : The input nodes of the amplification stage
- V_{bias} : The voltage biasing source
- C_{bias} : a decoupling capacitor at node B
- T_1 and T_2 : stand for the next amplification stage entry transistors

The gray stage stands for the amplification stage that comes right after this biasing stage.

The signal at node A is the AC signal coming from the optical clock circuit which adds up to the DC voltage provided by V_{bias} . The biasing resistor R_1 is

necessary here because it allows node A to oscillate with the AC signal while having a DC component through V_{bias} . Node A voltage is equal to:

$$A = V_{bias} - I_b R_1 \quad (4.39)$$

Where I_b is the base current of the input transistor of the amplification stage at node A.

The second biasing resistor R_2 is also necessary, because if else, the voltage at node B will be different from voltage at node A.

The capacitor C_{bias} is implemented at node B to prevent the AC signal, coming from A through the transistors path (T_1 and T_2), from affecting the biasing voltage.

The V_{bias} component will be an external source, this way we can adapt the final pulse width according to the different falling times that we obtain with the different optical clocks.

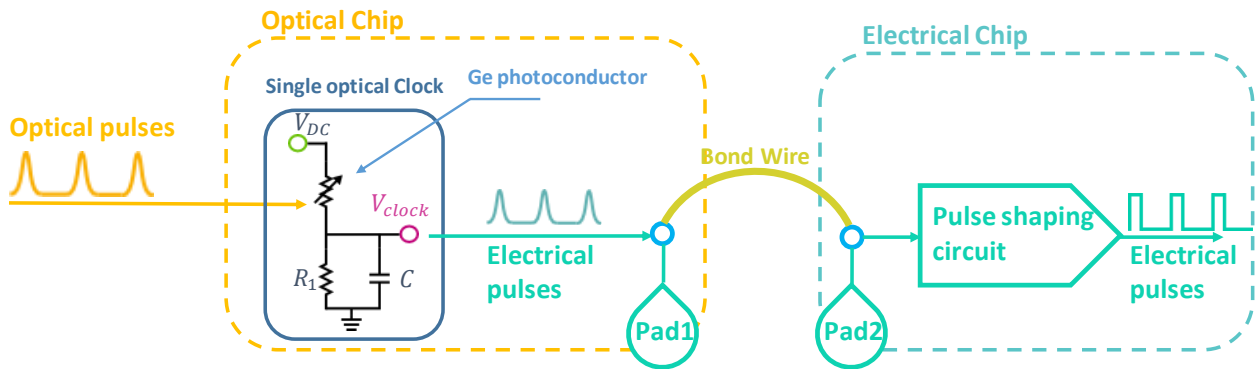


FIGURE 4.54: Clock circuit with connections explicated

As said earlier, this stage is intended to allow for a single to differential transformation of the clock signal. However, it is also the first block of the electrical chip, which means that the design must take into consideration the eventual parasitics coming from the pads and the wirebondings, see fig.5.20.

Indeed, the inductance of the wirebonding coupled to the different capacitances of this stage will eventually give rise to a ringing frequency which we will have to take into consideration in the bandwidth calculations. For now, we will give general specifications for this stage, but the operation and sizing will be discussed in full detail within the next chapter.

The single to differential stage must allow for the full spectrum of the optical signal to be coupled to the amplification stage. This means that the bandwidth must start from the signal repetition frequency: f_{dn} , and cover up to the frequency of the steep rising edge: f_{up} , where: $f_{dn} = 100MHz$ and $f_{up} = 16GHz$.

f_{up} is estimated as follows:

$$f_{up} = \frac{V_{pk}/T_{rise}}{2 * \pi * V_{pk}} = \frac{1}{2 * \pi * T_{rise}} \quad (4.40)$$

We set for now the minimum achievable T_{rise} at 10ps, because, as said in the earlier chapter, we consider R_{on} 's smallest value to be 10Ω so that the on time constant is 10ps.

To sum up, the specifications of this stage are the following:

- Single to differential operation.
- Bandwidth of 100MHz up to 16GHz.

Amplification stage:

The amplification stage is at the heart of the pulse-shaping circuit, its main purpose is obviously to amplify the now differential signal and transform it into a rectangular pulse signal.

Ideally, we would like the final falling edge to be 1V/30ps.

The signal we start with, namely the falling edge of the optical clock (OFF slope), can be approximated by a decaying exponential slope:

$$V_{in}(t) = (V_{on} - V_{off})e^{\frac{-t}{\tau_{off}}} \quad (4.41)$$

Where:

τ_{off} is the falling edge constant, namely $R_{off}C$.

So, at $t = t_0$, the slope of the input signal is equal to:

$$\frac{dV_{in}}{dt}(t_0) = -\frac{(V_{on} - V_{off})}{\tau_{off}}e^{\frac{-t_0}{\tau_{off}}} \quad (4.42)$$

Since we need the output pulses to be 600ps long, then we consider:

•

$$t_0 = 600ps \quad (4.43)$$

•

$$V_{on} - V_{off} \approx 2V \quad (4.44)$$

•

$$\tau_{off} = 5000ps \quad (4.45)$$

For the falling edge time constant τ_{off} , we actually considered a R_{off} of $5k\Omega$ and a capacitor of $1pF$.

The amplification that we are heading for is therefore approximately equal to $60dB$.

The constraints of the amplification stage are:

- Bandwidth of $100MHz$ up to $16GHz$
- Gain of approximately $60dB$.

1V stage:

Technically, the 1V stage is part of the amplification stage. However, it has special constraints that are relative to the fact that it is also the last stage of the pulse shaping electronic chip.

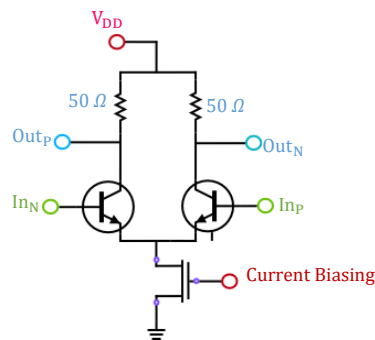


FIGURE 4.55: Scheme of the 1V stage design

Indeed, this stage being at the output, it will be directly connected to a coaxial cable when the circuit will be characterized, or to a 50Ω transmission line in the pcb (Printed Circuit Board) when mounted. Therefore, the circuit must exhibit a 50Ω resistance at the output.

We chose the basic common emitter structure (see fig.4.55) for this circuit with a 50Ω output resistors and an adequate biasing current.

Given the current circuit structure, we will need an additional stage that has not been discussed above in order for the sampling+clock circuit to properly function. This additional stage is an input buffer stage that would buffer the RF input signal to the sampling signal and will be presented within the following section along with the reasons that made us add it to the final circuit.

4.2.4.4 Input Buffer circuit:

As explained in section §.4.1.2, in order to test the jitter in our circuit, we need an input signal of frequency at least equal to:

$$f_{in} \geq \frac{1}{2\pi j_{rms}} 10^{\frac{-6.02ENOB + 1.28}{20}} \quad (4.46)$$

In our case, we use a 12 bits ADC with an ENOB of 10.5 and we are trying to measure a jitter of approximately 11fs. Therefore, the jitter is noticeable at:

$$f_{in} = 11.6GHz$$

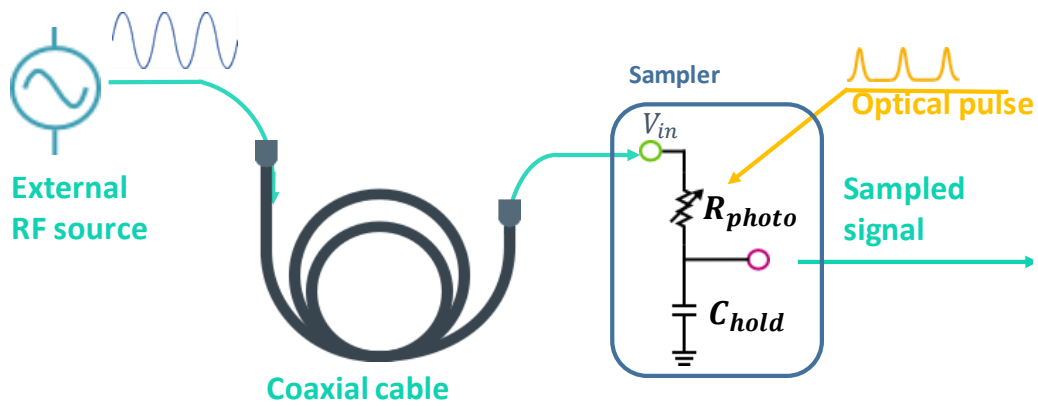


FIGURE 4.56: Photo-conductors integration scheme

The RF input signal with $f_{in} = 11.6GHz$ is injected into the chip from an external source through a coaxial cable; the bandwidth of the used cable must be higher than f_{in} .

If we were to use the test scheme exactly as depicted in fig.4.56, then the 50Ω cable would be connected to the sampler input impedance. The impedance of the sampler is equal to:

$$Z_{in} = R_{photo} + \frac{1}{j\omega C_{hold}} \quad (4.47)$$

R_{photo} is the resistance of the photo-conductor and is equal to:

R_{on} : when the photo-conductor is lit by the laser

R_{off} : in the absence of light

Two problems stem from this configuration:

- Impedance matching: R_{on} and R_{off} are not necessarily equal to 50Ω . Therefore, the signal that finally reaches the sampler experiences a reflection because of the impedance mismatch (lookup §appendix.B). This causes the final SNR measurements to be altered.

- The impedance changes between the off and on states, this means that the signal at node V_{in} does not remain the same between the track and hold phases. The signal at node V_{in} will therefore experience another reflection because the sudden current call due to the impedance variation, kicks the system out of its steady state. The source has to answer the current call, which will happen after the cable propagation time. Contrarily to the case explained in chapter1, this time, the reflection wave will last even longer because the input signal is a sine-wave and not a DC signal. This means that measuring the SNR after the sampler and concluding on the jitter will be very challenging.

Furthermore, in both phases on and off, the input impedance of the sampler, see eq.4.47, depends on the signal frequency. This effect is especially noticeable within the on phase, since in the off phase the input impedance is approximately equal to R_{off} (R_{off} is way bigger than the Hold capacitor impedance around the used frequency).

Indeed, if we consider the following orders of magnitude of the sampler components: $C_{hold} = 1ps$ and $R_{on} = 10\Omega$, then at: $f_{in} = 10GHz$ the input impedance is equal to 18Ω . While at: $f_{in} = 1GHz$, the input impedance is equal to: 160Ω .

This amounts to say that, provided the steady state is established within the ON phase, the amplitude of the signal that reaches V_{in} node is not the same for all the input frequency values.

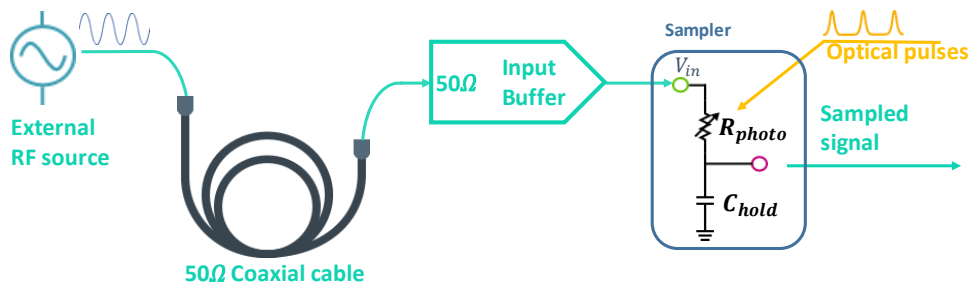


FIGURE 4.57: New sampler circuit scheme with input Buffer included

Therefore, in order to avoid these problems, we must implement an input buffer between the coaxial cable output and the chip, see fig.4.57. The latter should provide a constant 50Ω input impedance to the cable connected circuit side, while also copying the input signal to the sampler input as correctly as possible.

The input buffer circuit scheme is the one depicted in fig. 4.58.

Where:

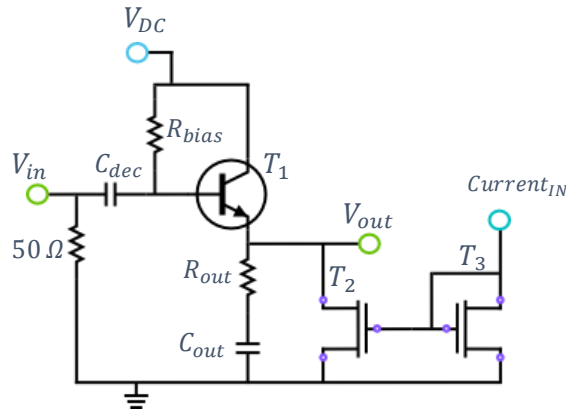


FIGURE 4.58: Input buffer electrical scheme

Node V_{in} is the node connected to the coaxial cable. The RF signal is injected into the circuit at the latter node and sees a 50Ω resistor for impedance matching as explained above.

The capacitor C_{dec} is a decoupling capacitor, i.e. a capacitor that eliminates the DC signal so the biasing is achieved through the circuit and not imposed by the input signal DC level.

R_{bias} is the biasing resistor for the transistor T_1 , it fixes the transistor base voltage using its base current.

R_{out} is the circuit output resistance and C_{out} is another decoupling capacitor. Both are connected in series to the V_{out} node which is the output node of the circuit.

T_2 and T_3 pair are a basic current mirror, where the reference current is injected externally at node $Current_{IN}$, then copied into T_2 through T_3 and injected into the emitter of transistor T_1 to bias it.

4.2.4.5 Final sampler circuit scheme:

To sum up, the final updated sampler scheme is given in fig.4.59.

In this scheme, we can see the different electrical circuits to design that we have presented early on, but also the optical parts. Indeed, as we saw, the clock generation circuit relies on optical pulses as much as the sampler circuit does. Therefore, we need to split the power between the two. In the scheme above, we have used a 10% coupler to split the light but this could be done in other ways that will be explained under the Divider block within the next paragraph.

The optical signal that feeds the clock must also be delayed, hence the use of a delay line (delay block below). These components, along with the optical chip of the clock generation circuit, will be presented within the next paragraph.

a: Divider block:

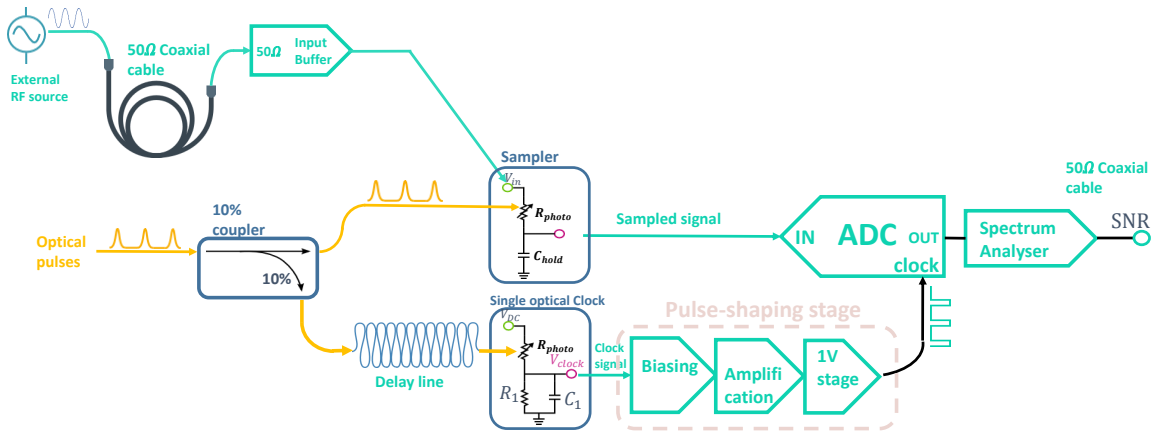


FIGURE 4.59: Final sampler scheme

The aim of this block is to split the laser output beam into two signals: one designed to feed the sampler circuit and another one to help generate an optical clock.

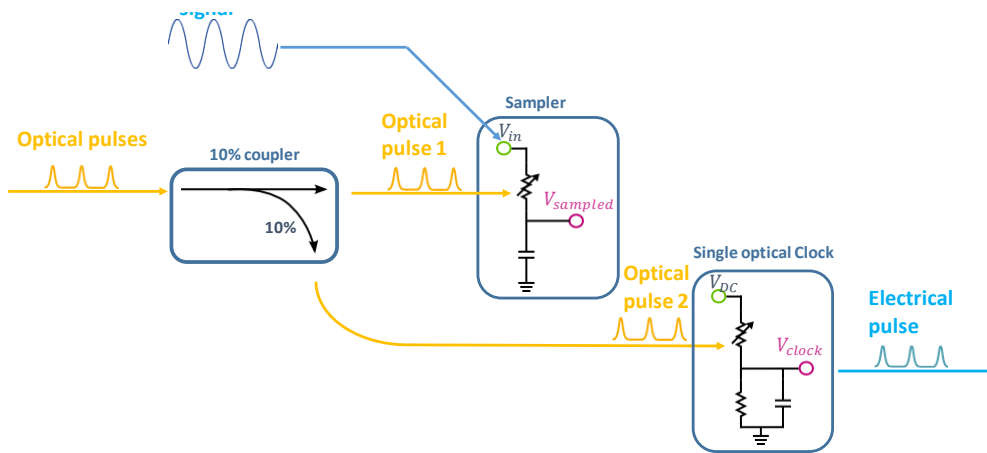


FIGURE 4.60: Optical scheme implemented to feed the clock generation circuit with 10% of the laser pulse energy

The straightforward way to make this block is just to use an optical decoupler, or a Y branch waveguide.

We effectively implemented this solution using a 10% optical decoupler where 10% of the laser signal is used to feed the clock circuit and the rest is used in the sampler circuit as depicted in fig.4.60.

There is another way to make the divider block. This time, we use the sampler optical energy leftovers. Indeed, as seen in the previous chapter, if we use photo-conductors that are shorter than the germanium absorption lengths, the incident energy is not totally absorbed. Therefore, we can harvest the leftover energy to feed the clock generation circuit

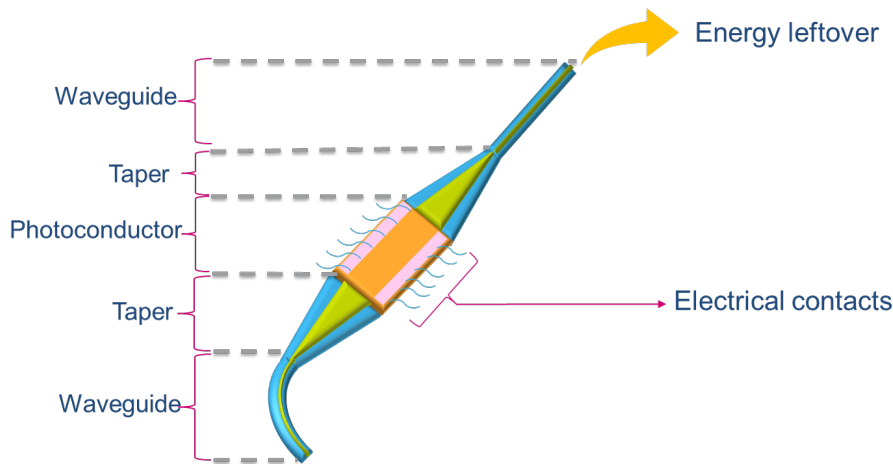


FIGURE 4.61: Optical scheme implemented to feed the clock generation circuit with the non-absorbed leftover energy

as depicted in fig .4.61.

In our case, we used $7\mu m$ long photo-conductors, which allows for enough energy to feed the clock generation circuit.

b: Delay block:

The delay block is made out of different lengths of simple wave-guides depending on the optical delay that we want to implement. These delay lines exhibit better reliability and better noise immunity performance than the electrical delay lines. The wave-guides lengths are estimated as follows:

- For straight waveguides, a $100\mu m$ long waveguide yields $1.3ps$ delay and very low loss (propagation loss of about $2.4dB/cm$).
- Bends introduce $819fs$ each and 0.34% loss of energy.

The delay time values were estimated first by a mathematical estimation based on the effective index of the waveguides and the length of the bends. We also simulated the response of the delay lines on Cadence based on STMicroelectronics Pic25G photonics design kit.

NB :

The optical signal at the output of the delay lines is slightly widened and attenuated in amplitude. This is not a problem because we can adjust the next stages to make up for these defaults.

4.2.4.6 Conclusion and perspectives

In the previous section, we have demonstrated a theoretical circuit that would make it possible to use the germanium photo-conductor basic sampling scheme while dealing with the problems that it has raised in the first section of this chapter. The final upgraded circuit is made of the sampling block, along with a first input buffer that allows the signal to sample to reach the sampler through the coaxial cables without ripples or impedance matching problems.

The new upgraded scheme includes, most importantly, a clock generation circuit that makes it possible to create an electrical clock signal from the laser pulses and with approximately the same jitter performance. The then new generated clock drives the ADC that re-samples the signal, which make it possible to overcome the low R_{off} value problem.

This first clock circuit made us think about the perspectives of using photo-conductors in order to generate clock signals with low jitter values. Indeed, compared to a classical photo-diode based clock circuit, we do not need to add a big resistor/Trans-impedance Amplifier (TIA) in order to get a neat clock signal which means that the noise performance is better controlled with photo-conductors than with photo-diodes.

Indeed, for a long time, the silicon photonics industry and research has overseen the photo-conductors use and preferred rather the photo-diodes solely because of the slow decay response of the photo-conductors. Yet, the latter present valuable advantages compared to the photo-diodes:

- A simpler design: in our case we need only one type of doping rather than two in the case of photo-diodes, and this comes with shorter post-treatments (activation process for example). One can also argue that with the use of Boron for the P doping, we have smaller diffusion length which simplifies the design and allows for a better control of the detection area compared to a Phosphorous doped device (in the case of photo-diodes for example).
- Smaller parasitic capacitance: in the case of photo-diodes, the junction capacitance is one of the main problems that hinder the photo-diodes frequency response. In the case of photo-conductors, we do not have the same problem, the capacitance is very small by construction and does not impede much the frequency response of the device.
- The need for TIAs for photo-diodes while it is not the case for photo-conductors, which affect the noise performance as said earlier.

For all these reasons, we decided to dig deeper the possibilities of clock generation based on photo-conductors and tried to overcome the limitations of the first circuit. The solutions that we have found are explained within the next section.

4.3 Photonic clock circuit

In order to upgrade the idea of the single clock that we have used in the previous section, we designed another circuit: the single photonic clock. This new circuit does not feature the problems of the previous circuit, i.e. the need for an amplification stage and the constraint of not perfectly controlling the pulse width as we do not know the falling edge length.

4.3.1 Single photonic clock circuit

The idea behind the single photonic clock is to use the steep rising edges to define both the rising and falling edges of the new clock.

Indeed, with the first clock circuit, the slow falling edge slope is the reason why we had to add the pulse shaping stage (other than the pulse duration). The falling edge is very important in the first circuit configuration because the holding decision is taken on that edge and not on the rising edge. With this new circuit, we try to make both edges as steep as possible.

The single photonic clock is presented in fig.4.62.

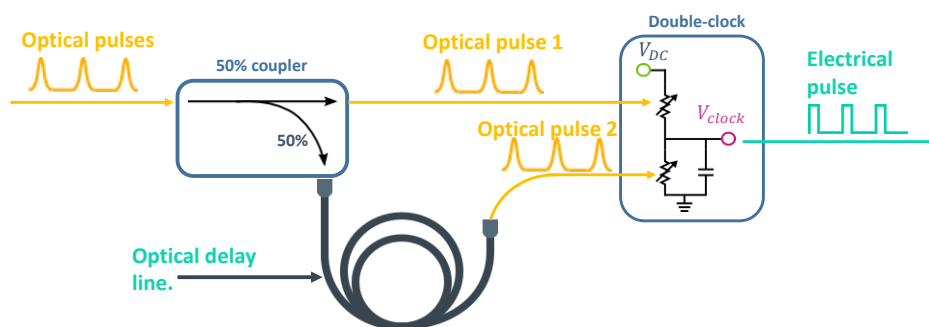


FIGURE 4.62: Single photonic clock circuit

The main idea of this new clock circuit is to harvest the rising edges of two photo-conductors in series.

The modus operandi of the single photonic clock is illustrated in fig.4.63. At first, the upper photo conductor is hit by the laser pulse, its resistance decreases and the inner node voltage increases till it reaches its final value. Then, after the second laser pulse hits the bottom photo conductor, (fig.5.27b), the output node voltage goes back to its initial value.

The laser pulses required for this block are generated through a 3dB coupler at the output of the grating coupler and an optical delay line. The latter ensures less pulse width variations than a regular electrical delay line.

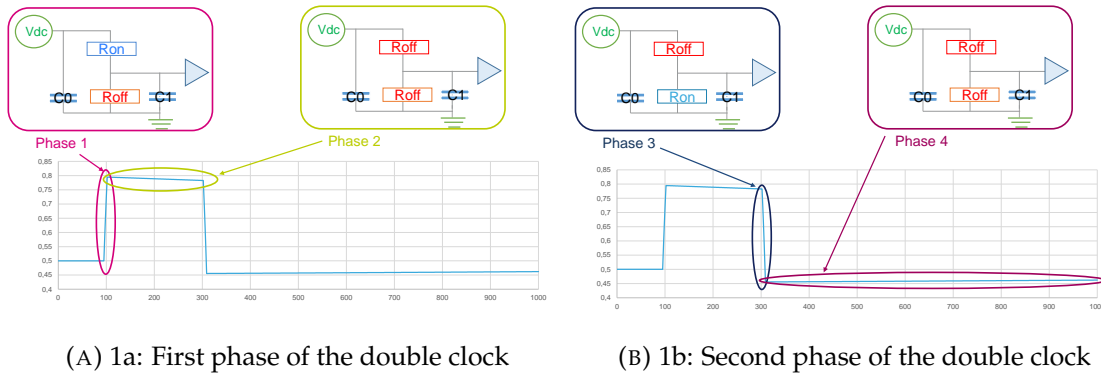


FIGURE 4.63: Plots of double clock operation process

With this new configuration, the slow decay of the photo-conductors is taken advantage of and is no longer a problem. Indeed, the longer the decay time constant, the longer we can make the pulse last since the upper voltage lasts longer. This is why this circuit was patented under [123].

This means that the importance of the high R_{off} value becomes priority over the low R_{on} value if we want long pulses.

The main problem of this circuit is that the output electrical pulse width cannot exceed the falling edge duration of the optical pulse. This binds us to optical pulses of at most 100ps lengths, which implies ADCs of 5 GHz sampling frequencies and more.

In order to overcome this problem, we have thought about a new structure based on the single photonic clock circuit but without the pulse width problem, this circuit is presented in the next paragraph.

It is worth noting here that the photonic clock circuits that we are developing in this chapter will not be used within the final sampler circuit. Therefore, the previous constraints of the photonic clock, namely the pulse width that should be >600ps, do not apply in this case.

4.3.2 Double photonic clock circuit

As said earlier, the single photonic clock is bound in pulse width by the fall time of the photo conductor. The double photonic clock is an alternative to this problem: it relies on two separate single photonic clocks, delayed by an optical delay line of known length and used later on to generate a final pulse through a logical combination of the two pulses via an electronic logical circuit.

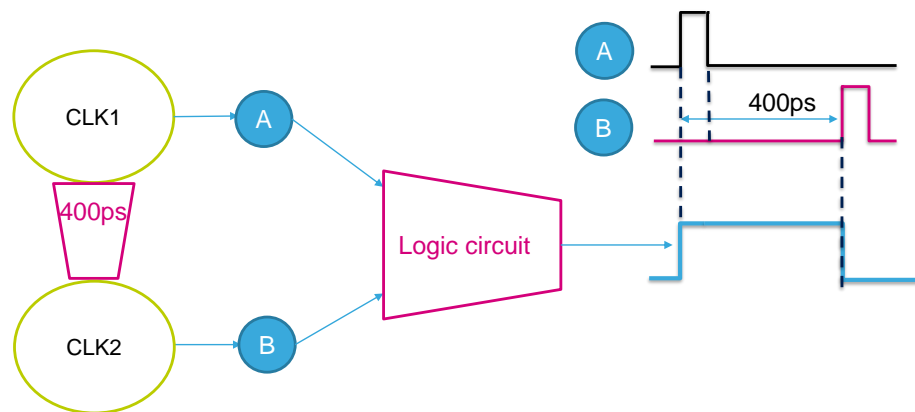


FIGURE 4.64: Double photonic clock circuit operation

To better illustrate the operation of the double photonic clock, we depicted its scheme in fig.4.64.

As depicted, the rise and fall edges are made out of the two rising edges of the single photonic clocks, which in turn are the rising edges of the photo conductors.

The circuit's operation is basically the following, see fig.4.65:

The optical pulse is first split between two single clock circuits: say pulse A and pulse B.

Pulse A feeds the first single photonic clock, say $clock_A$. This means that pulse A is split between two pulses: pulse A1 and pulse A2, where pulse A2 is delayed by an optical delay line. As explained earlier, pulse A1 hits the upper photo-conductor of $clock_A$ and pulse A2 hits the bottom photo-conductor after the delay (that we will call Δt_1).

Pulse B feeds a second single clock, that we will call $clock_B$, after going through an optical delay line with total time delay: Δt_2 . The pulse is therefore split again and we have the same operation than explained early on for pulse A.

This yields two electrical signals: the first signal of $clock_A$ and the second signal of $clock_B$ that we will call respectively V_A and V_B , where V_B is a replicate of V_A with a delay of Δt_2 .

These two signals are then processed through a logical circuit: a flip flop. The latter's operation is the following:

The circuit first receives a rising edge from V_A which yields a rising edge at the output of the circuit: V_A is actually considered as the set signal. The output is then an upper state (a 1), up till V_B exhibits a rising edge (V_B acts then as a reset signal). The output then goes back to 0. This way, the flip flop circuit returns a Δt_2 wide pulse signal with steep rising and falling edges. This last statement is based obviously on the hypothesis that the flip flop circuit is fast enough to conserve the clock's steep edges, this is why we have chosen to design the clock circuit using ECL logic.

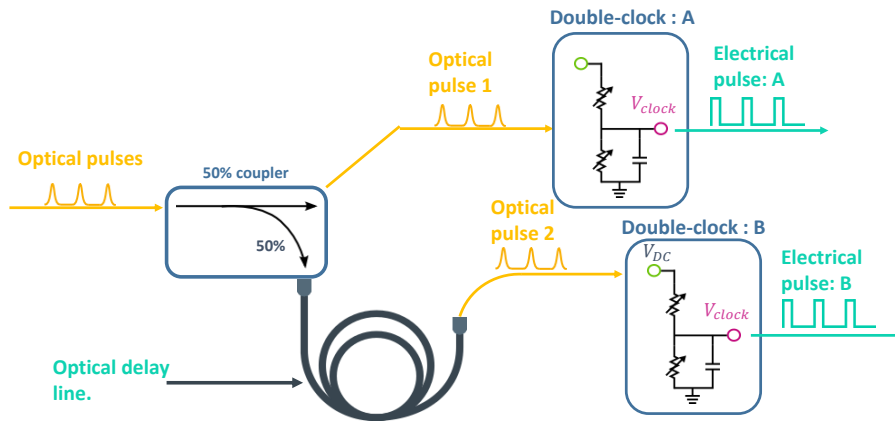


FIGURE 4.65: Double photonic clock circuit layout

ECL logic, i.e. Emitter-Coupled-Logic, also called CSL logic which stands for Current-Steering-Logic is a logical circuit design approach based on the use of differential pairs of bipolar transistors with passive loads. The logical operations are achieved by steering the current from one branch to another, which translates into a differential voltage through the resistive load.

We have chosen to use a bipolar technology to design the logical circuit rather than a CMOS technology based on two main reasons:

- The low voltage swing: indeed, rail-to-rail CMOS logic is capable of achieving high switching speeds, however, it calls for high voltage swings in order for the circuits to switch. This translates generally into adding amplifying stages, which is not the case for the bipolar logic.
- The switching noise: CMOS switches generate a big noise contribution on the substrate and the supplies, which in turn would disturb the jitter performance of the clock.

The choice of ECL over other bipolar logic circuit design techniques, such as TTL (transistor-transistor logic) , RTL (Resistor-transistor logic) or DTL (diode-transistor Logic) is mainly due to the high speeds achievable through the use of this technology.

Indeed, nowadays most of the optical communication circuits are based on ECL because the latter allows for a reduced voltage swing, which translates into higher operation speeds [124]. ECL does not involve putting transistors in saturation mode which also reduces the switching time because the saturated transistors in other logic circuit technologies are slow to get out of saturation mode because of the diffusion time constant [125].

In our case, as will be explained in the next chapter, the whole design was made in BiCMOS55 technology from STMicroelectronics.

In the operation scheme that was presented in fig.4.65, we have chosen the following delay values:

- First delay time, $\Delta t_1 = 100ps$, this is the single clocks' pulse duration.
- Second time delay: $\Delta t_2 = 400ps$, this is the double clock's pulse duration in total.

The first delay value is motivated by the fact that we needed a pulse duration that is long enough to be processed by the logical circuit. Yet, it has to be short enough so that the single clock signal is clear enough. Indeed, as we saw early on, the single clock signal duration is limited by the τ_{off} time constant value.

For the second value, the objective was to go for a value that is high enough to prove the concept of the double clock. However, as we will see, we were limited by the wafer surface that we were assigned as the delay lines take a lot of surface (see next chapter).

4.4 Conclusion

In this chapter, we have first discussed the operation of the basic sampler circuit and demonstrated all the problems that it raises given the photo-conductors characterization work that has been presented in the first chapter. Therefore, we have proposed different solutions to overcome these limitations, namely a novel photo-conductor geometry and counter-doping, both of which were aimed at increasing the R_{off} on R_{on} ratio of our devices. These two techniques exhibited optimized results but their impact was not big enough to fully overcome the low ratio limitation.

We have therefore presented an electrical circuit that would allow to work around the low ratio problem by re-sampling the signal with a clock with the same jitter performance. The latter called for a new clock generation circuit, which was presented and patented. Other variations of this clock generation circuits were later on exposed with better performance and less electrical drivers needed.

In the forthcoming chapter, we will present the design details of these different circuits and the final layout along with the simulation results.

Chapter 5

Design and layout

In this chapter, we will explain in details the design and layout of each of the blocks that we have talked about in the previous chapter. We will first give a short glimpse about the technologies we use then we will dive into the design details.

5.1 Technology

For the design of the electronic chips, we use the SiGe BiCMOS 55nm technology of STMicroelectronics. This technology was developed to address applications such as radar designs operating at 77GHz and very high throughput optical communications (100 Gbits/s). It comes after a long series of improvements on STMicroelectronics BiCMOS technologies as presented by STMicroelectronics in fig.5.1.

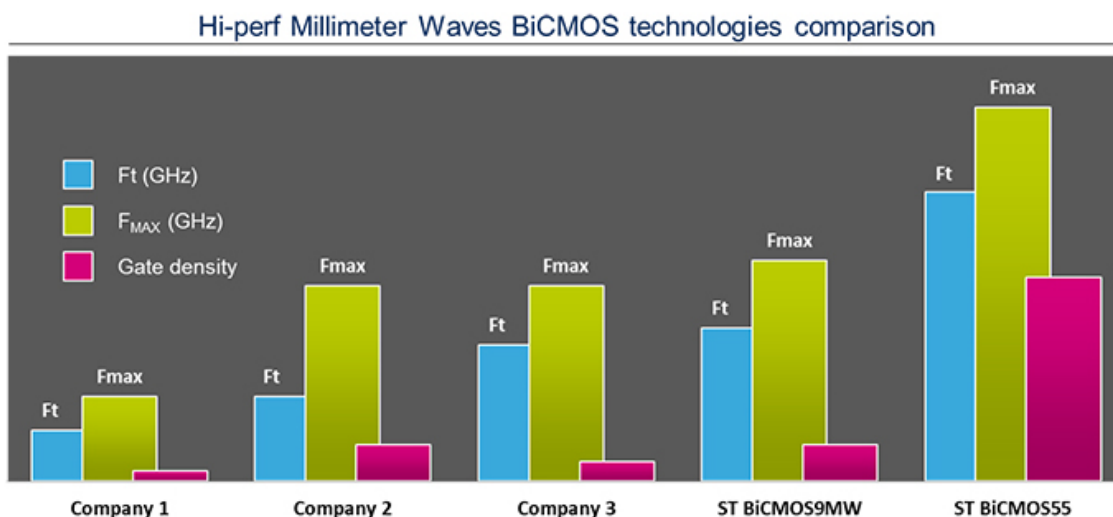


FIGURE 5.1: STMicroelectronics BiCMOS technologies performance evolution.

BiCMOS55 technology is derived from a 65nm low power/ general purpose mix (LP/GP) CMOS platform called C065 fully presented in.[126]. It provides different flavors of NMOS and PMOS transistors: High- V_T (HVT), standard- V_T (SVT) and a low- V_T (LVT) option. A minimum gate length of 45nm is achieved for GP NMOS transistors.

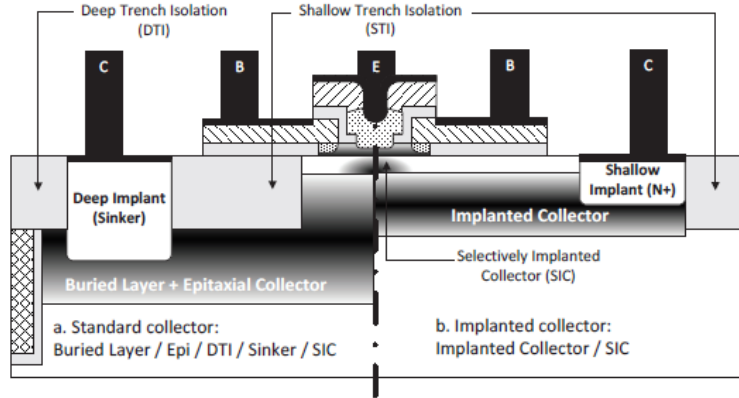
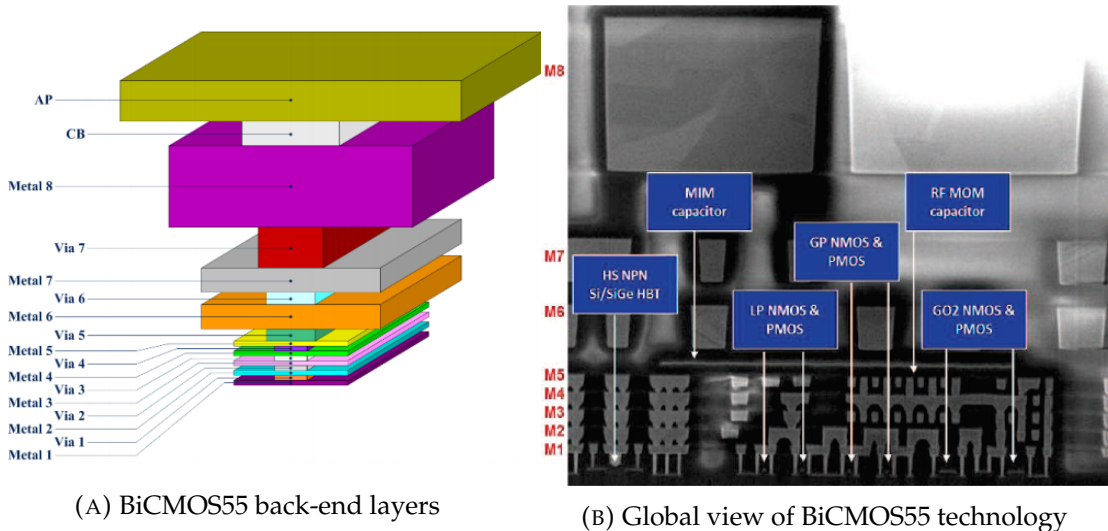


FIGURE 5.2: Illustration of SiGe HBT different collector variations.

High speed silicon germanium transistors, SiGe HBTs, feature a double-polysilicon self-aligned architecture where emitter-base self alignment is provided by Selective Epitaxial Growth of the SiGe:C base [127]. Here again, different flavors are available : High Speed (HS), Medium Voltage (MV) and High Voltage (HV). These three flavors are made by using different techniques for the collector, see fig.5.2.



(A) BiCMOS55 back-end layers

(B) Global view of BiCMOS55 technology

FIGURE 5.3: Sketches of STMicroelectronics BiCMOS55 technology features

Emitters are scalable in width and length with a minimum area of $0.10 \times 0.30 \mu\text{m}^2$.

BiCMOS55 technology is suitable for high speed low noise applications because the SiGe-C HBTs offer the best speed-to-noise ratio. Indeed, with this technology, transit frequencies f_T of more than 300GHz and maximum oscillation frequencies of 400GHz have been measured [128].

The back-end of line (BEOL) of this technology is based on the BEOL of the 55nm CMOS technology. A $3\mu m$ thick copper layer and a $1.5\mu m$ thick via layer have been added so that the total copper metal layers are now 8 (plus the Aluminium layer (AP)). The stacking of the different back-end layers is depicted in fig.5.3a.

Now that we have presented the technologies we will be using, we will explain the design logic that we have followed for each electrical circuit and illustrate the simulations that we have performed. The circuits will be presented under two sections:

- Section 1: Sampler circuit: this section will cover the circuits designed to be used with a basic sampler +ADC.
- Section2: Double clock generation circuit: this section covers the flip-flop design that is relative to the double clock circuit.

5.2 Sampler circuit design

The sampler circuit electrical drivers are basically: the input buffer and the pulse shaping circuit for the single optical clock that would drive the ADC.

5.2.0.1 Input Buffer

As explained in §.4.2.4.4, the main purpose of the input buffer is to copy the input signal, at $f_{in} = 11.6GHz$, (which is the frequency value at which the 11fs jitter becomes measurable) with our ADC to the photo-conductor circuit, while providing a 50Ω input impedance at the coaxial cable output node as depicted in fig.5.4.

A. Circuit specifications:

The input buffer circuit is expected to meet the following constraints:

- **Bandwidth:**

The upper bandwidth limit depends obviously on the input signal frequency, i.e. $f_{in} = 11.6GHz$. Therefore, in order to have a proper gain at the target frequency, the input buffer cutoff frequency must be at least 10 folds the target frequency, i.e. $f_{up} = 116GHz$.

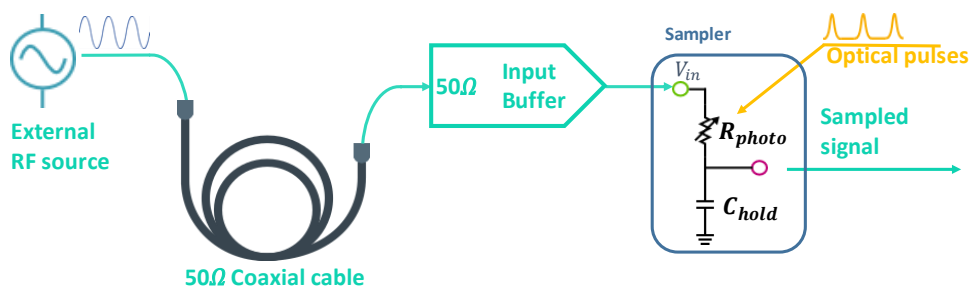


FIGURE 5.4: Input buffer integration scheme

This constraint is built on the approximation that the input buffer has a first order low pass filter behavior.

We plan to test the circuit at a lower frequency in order to check the accuracy of the test bench. Indeed, at lower frequencies, the effect of the jitter is not measurable so that we only have the impact of the other noise sources on the input signal. We can therefore compare the output SNRs at low and high frequencies to conclude on the jitter performance.

We set the lower frequency value at $f_{low} = 200MHz$. This value's choice is actually random since we can choose any frequency value that is less than the $f_{in} = 11.6GHz$.

Here again, we make the approximation of a first order high pass filter, and we set the lower edge of the bandwidth to be equal to $f_{up} = 20MHz$.

In conclusion, we need the bandwidth of the input buffer to be larger than: $BW = [20MHz; 11.6GHz]$, but should keep in mind the approximations made to choose this bandwidth value.

Gain:

The first function of the input buffer is to copy the signal from the coaxial cable output to the input of the photo-conductor circuit. Therefore, the gain is expected to be unity, i.e. $G = 0dB$ over the upsaid bandwidth.

Input impedance:

The input buffer input impedance is supposed to be equal to 50Ω in order to achieve the impedance matching.

Output impedance:

The input buffer is connected at its output to the photo-conductor circuit, the latter input impedance changes with light as was explained in §.4.2.4.4.

In order for the input buffer to operate correctly, it should have a constant impedance at its output. The only way to achieve this constraint with the photo-conductor varying impedance is to choose an output impedance that is smaller than the photo-conductor input impedance in all cases, so that once put in parallel, the input buffer only sees its inherent small output impedance.

Since in our approximations so far the R_{on} value is always higher than 10Ω , then, we set the output impedance to 10Ω .

Noise performance:

The input buffer will certainly add its own noise contribution to the input signal. However, we need this noise contribution to not false the final jitter measurements. A way to ensure this will not happen is to make sure the noise induced voltage error stays below the threshold of the ADC.

This is to say the following:

Say V_{rms} is the root mean square of the voltage error due to the input buffer noise: we need:

$$V_{rms} < \frac{V_{pk-pk}}{2^{ENOB+1} - 1} \quad (5.1)$$

We consider here the ENOB value rather than the real number of bits because it accounts for the quantization noise of the ADC.

If we consider an input RF signal with $V_{pk-pk} = 1V$, then the input buffer added noise voltage must be smaller than: $691\mu V$ (rms value integrated over the signal bandwidth).

To sum up, the constraints of the input buffer circuit are as follows:

- Bandwidth: $BW = [20MHz; 116GHz]$.
- Gain: $G = 0dB$.
- Input impedance: $Z_{in} = 50\Omega$.
- Output impedance: $Z_{out} = 10\Omega$.
- Noise performance: $V_{noise_{rms}} < 691\mu V$ (for $V_{pk-pk} = 1V$).

B. Design and simulations

In the following section, we will explain in details the design of the input buffer stage. We will walk the reader through the design method that we have used in order to choose the circuit architecture and the components sizing. The same method was applied for all the other circuits, however we will not explain all of them the same way to keep this manuscript as concise as possible.

B.1. Design considerations

The first function of the input buffer is to copy the input RF signal from the coaxial cable output to the photo-conductor circuit input. Therefore, the most intuitive approach is to use an emitter follower scheme (also called common collector amplifier), see fig.5.5:

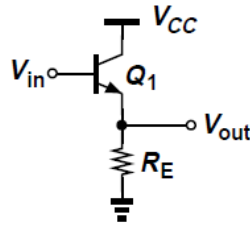


FIGURE 5.5: Emitter follower basic scheme

The emitter follower operates as a voltage buffer because its voltage gain is approximately equal to [122]:

$$G_{CC} = \frac{g_m R_E}{g_m R_E + 1} \quad (5.2)$$

Where $g_m = \frac{I_c}{V_T}$ is the trans-conductance of the transistor Q_1 and $g_m R_E \gg 1$. (I_c is the transistor's collector current).

i. Circuit upgraded

We start with this basic scheme and add the following components:

- **Decoupling capacitors:**

We add two decoupling capacitors, one at the input node: C_1 and one at the output node, in series with the output resistor: .

C_1 role is to eliminate C_2 the DC component out of the received signal at the coaxial cables' output. This would make it possible to bias the signal afterwards in order for the input buffer to process it properly.

We added C_2 so that the photo-conductor circuit receives only the RF signal.

- **Biasing resistor and current source:**

In order to bias the transistor Q_1 , we have added first a biasing resistor, R_{bias} between the base node and the supply, which fixes the base voltage at $V_{cc} - I_b R_{bias}$, I_b being the base current.

We have also added a current source at the emitter node to fix the current that crosses the transistor. This is done through the use of a basic current mirror made of two CMOS transistors: T_1 and T_2 , and fed by an external current source.

- **Biasing resistor and current source:**

In order to bias the transistor Q_1 , we have added first a biasing resistor, R_{bias} between the base node and the supply, which fixes the base voltage at $V_{cc} - I_b * R_{bias}$, I_b being the base current.

We have also added a current source at the emitter node to fix the current that crosses the transistor Q_1 . This is done through the use of a basic current mirror made of two CMOS transistors: T_1 and T_2 , and fed by an external current source.

- **Matching impedance**

We have added a 50Ω resistor at the input of the circuit in order to achieve the input impedance constraint.

The final circuit is presented in fig.5.13.

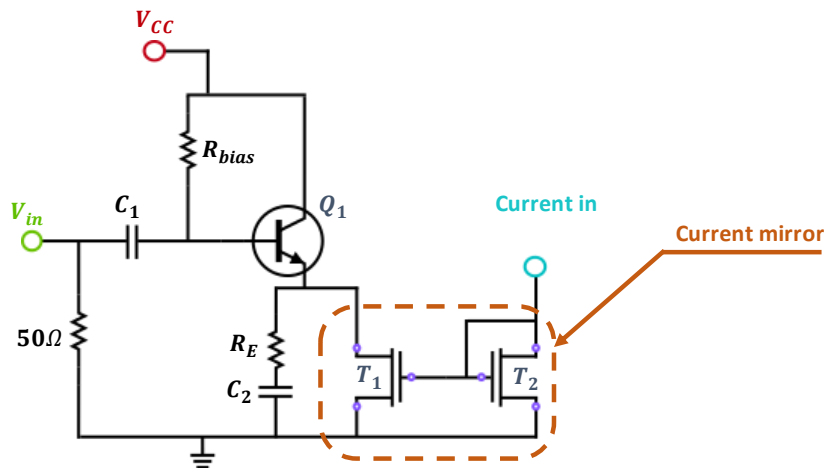


FIGURE 5.6: Input buffer updated circuit scheme

As we saw before, the constraints of the input buffer are very challenging, therefore, we will explain in details the sizing logic that we have followed. Actually, if the components sizing is not carefully optimized, such circuit might fall short to achieve the full list of specifications that we have mentioned above (low bandwidth, high noise contribution...).

ii. Circuit operation:

Before we present the sizing approach, we will walk the reader through a detailed theoretical study of the circuit operation that shows how each component value influences the circuit operation.

To do so, we may go back to the small signal model of the emitter follower, which is depicted in fig.5.7.

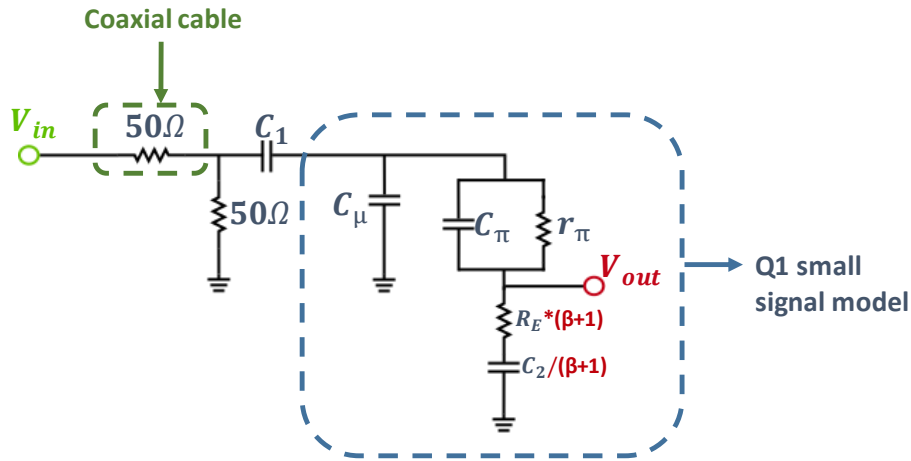


FIGURE 5.7: Input buffer small signal model

In this model, the coaxial cables were approximated with a 50Ω resistor. This approach is accurate in this case because we are studying the steady state response of the system, so no sudden current calls to handle as in the previous chapter study, and also because the RF input signal frequency is within the bandwidth of the used coaxial cables.

At the output node, V_{out} , we have not modeled the current source transistor T_1 because it represents a high impedance in parallel with smaller impedance (R_E in series with C_2), so it would have been neglected anyway.

At the input node, the current is i_B , the base current of the transistor Q_1 . However, R_E and C_2 are crossed by i_E which is the emitter current of Q_1 where $i_E = i_B * (\beta + 1)$. We can either, represent this by adding a current source at the output node: $i_c = \beta * i_B = g_m * V_\pi$, where V_π is the voltage on r_π and C_π , or the way we did, by multiplying the impedance by the current gain.

We have not modeled R_{bias} because it is a big resistance in parallel with smaller ones, so there is no need to take it into consideration.

In order to simplify the impedance calculus, we will rather make approximations based on the real values of the different components rather than just write the transfer function equation.

So we consider the following approximation:

Component	C_1	C_2	C_μ	C_π	r_π	β
Approximation	2pF	2pF	30fF	0.4fF	1k Ω	100

The values of C_π and C_μ that were considered are of a very small transistor. We chose these values this small just to clearly separate the different cut-off frequencies so that it becomes easier to understand the different regimes of operation of the input buffer.

The new circuit is depicted in fig.5.8

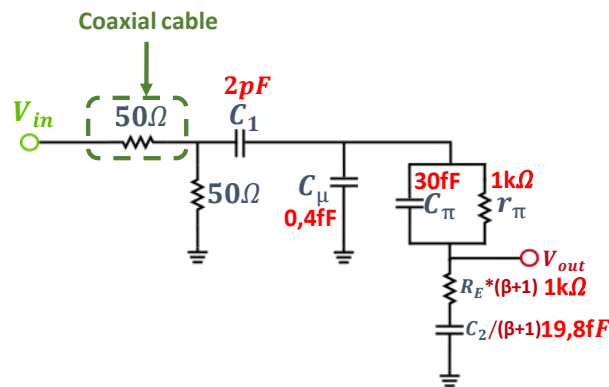


FIGURE 5.8: Input buffer small signal model with approximated component values

The value of r_π was estimated based on $r_\pi = \beta * \frac{V_T}{I_c}$ where β is considered equal to 100 and an I_c is set at 2.6mA, which is the minimal value of this current based on the emitter follower gain equation ($g_m R_E \gg 1$).

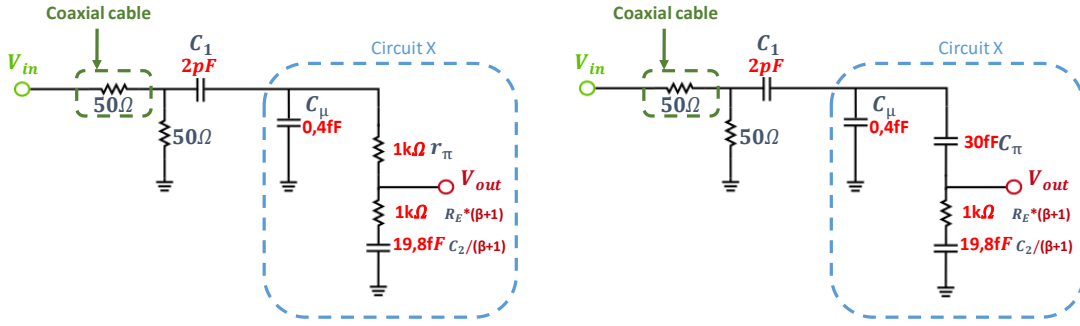
So, first we start with the r_π series C_π circuit: below the cut-off frequency :

$$f_\pi = \frac{1}{2\pi r_\pi C_\pi}$$

this circuit can be modeled only by the resistor r_π , but above it, the capacitor's impedance becomes smaller than the resistance, and the circuit's total impedance becomes mainly equal to the capacitor's impedance (because the capacitor and the resistor are in parallel).

With the approximate values, this cut-off frequency is about: $f_\pi = 5.3GHz$.

Now if we consider circuit X (which is highlighted in blue in fig.5.9):



(A) Input Buffer small signal model below f_π (B) Input Buffer small signal model above f_π

FIGURE 5.9: Emitter follower small signal circuit below and above f_π

If we consider the first circuit (fig.5.9a), the impedance of C_μ becomes equal to the impedance of the other branch at a cut-of frequency f_{x1} , where:

$$\sqrt{(r_\pi + R_E * (\beta + 1))^2 + \frac{\beta + 1}{2\pi f_{x1} C_2}} = \sqrt{\frac{1}{2\pi f_{x1} C_\mu}} \tag{5.3}$$

So that:

$$f_{x1} = \sqrt{\frac{1}{(2\pi * (r_\pi + R_E * (\beta + 1)))^2 * \left(\frac{1}{C_\mu^2} - \left(\frac{\beta + 1}{C_2}\right)^2\right)}}$$

With the up said values, we get a cut-off frequency of: $f_{x1} = 198GHz$, however, this value is beyond f_π , which means that below f_π , we can ignore the capacitor C_μ since its impedance is way higher than the other branch.

We apply the same logic to the second case, and we get the following cutoff frequency:

$$f_{x2} = \sqrt{\frac{1}{(2\pi R_E (\beta + 1))^2 * \left(\frac{1}{C_\mu^2} - \frac{1}{C_\pi^2} - \left(\frac{\beta + 1}{C_2}\right)^2\right)}}$$

In this case, the cut-off frequency is: $f_{x2} = 397GHz$.

Now we get the following configurations:

The objective now is to know when does circuit Y impedance become smaller than the parallel 50Ω . In the first case (see fig.5.10a), circuit Y is $R_E * (\beta + 1)$ in

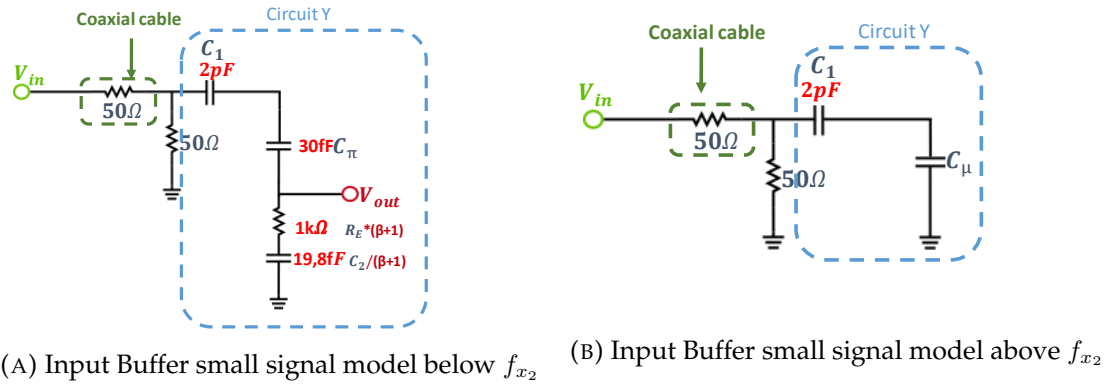


FIGURE 5.10: Emitter follower small signal circuit below and above f_{x2}

series with the capacitors, so that the minimum impedance vs frequency of this circuit is $R_E * (\beta + 1)$.

Now since $R_E * (\beta + 1)$ is approximately equal to $1k\Omega$ (the approximative value of β is very realistic), then circuit Y impedance is always bigger than the 50Ω . In this case, the impedance matching circuit operates as expected, meaning that the voltage at node Y is set only by the impedance matching circuit and is equal to $V_{in}/2$.

In the second case, the cut-off frequency is:

$$f_{y1} = \frac{1}{2\pi * 50\Omega * \frac{1}{(1/C_1) + (1/C_\mu)}}$$

With the approximate values, we have $f_{y1} = 7.96THz$.

So we can basically consider that the impedance matching circuit sets the Y node value up to $f_{y1} = 7.96THz$, starting from the said frequency, node Y experiences a roll off.

So to sum up so far, we have the following configurations:

In fig.5.11, the impedance of node X is fixed by the part of the circuit that is highlighted in red, and likewise, the impedance of node Y is fixed by the blue highlighted part of the circuit.

We will now study the transfer functions of these different regimes:

- So, for the first regime, the transfer function is the following:

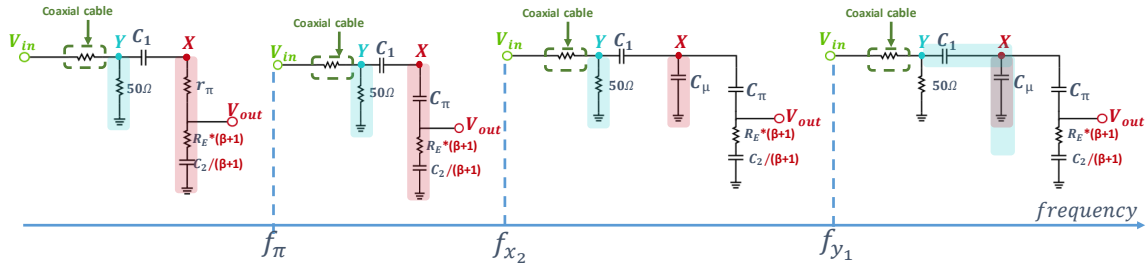


FIGURE 5.11: Input Buffer small signal model evolution with frequency

$$\frac{V_{out}}{V_{in}} = 1/2 * \frac{(R_E * (\beta + 1) + \frac{(\beta + 1)}{sC_2})}{R_E * (\beta + 1) + r_{\pi} + \frac{(\beta + 1)}{sC_2} + \frac{1}{sC_1}}$$

We have a pole and a zero:

$$- f_{p1} = \frac{1}{2\pi * \frac{1}{(\frac{\beta + 1}{C_2} + \frac{1}{C_1})} * (r_{\pi} + (\beta + 1)R_E)}$$

$$- f_{z1} = \frac{1}{2\pi R_E C_2}$$

We can already see that in order to have a gain of 1/2, we need r_{π} to be as small as possible. Now since: $r_{\pi} = \frac{\beta * V_t}{I_c}$, then we need a big collector current.

- For the second scenario, the transfer function is equal to:

$$\frac{V_{out}}{V_{in}} = 1/2 * \frac{(R_E * (\beta + 1) + \frac{(\beta + 1)}{sC_2})}{(R_E * (\beta + 1) + \frac{\beta + 1}{sC_2} + \frac{1}{sC_1} + \frac{1}{sC_{\pi}})}$$

We have, here again, a pole and a zero:

$$- f_{p2} = \frac{1}{2\pi * (R_E * (\beta + 1)) * \frac{1}{\left(\frac{\beta + 1}{C_2} + \frac{1}{C_1} + \frac{1}{C_\pi}\right)}}$$

$$- f_{z2} = \frac{1}{2\pi R_E C_2}$$

- For the third scenario, the transfer function is the following:

$$\frac{V_{out}}{V_{in}} = 1/2 * \frac{(R_E * (\beta + 1) + \frac{(\beta + 1)}{sC_2})}{R_E * (\beta + 1) + \frac{(\beta + 1)}{sC_2} + \frac{1}{sC_\pi} + \frac{1}{sC_1}} * \frac{C_1}{C_1 + C_\mu}$$

So that we have again a zero and a pole:

$$- f_{p3} = \frac{1}{2\pi * \frac{1}{\left(\frac{\beta + 1}{C_2} + \frac{1}{C_\pi} + \frac{1}{C_1}\right)} * (\beta + 1)R_E}$$

$$- f_{z3} = \frac{1}{2\pi R_E C_2}$$

- For the fourth regime, the transfer function is the following:

$$\frac{V_{out}}{V_{in}} = 1/2 * \frac{(R_E * (\beta + 1) + \frac{(\beta + 1)}{sC_2})}{R_E * (\beta + 1) + \frac{(\beta + 1)}{sC_2} + \frac{1}{sC_\pi} + \frac{1}{sC_1}} * \frac{1}{1 + \frac{C_\mu}{C_1} + s50\Omega C_\mu}$$

So that we have again a zero and a pole:

$$- f_{p4a} = \frac{1}{2\pi * \frac{1}{\left(\frac{\beta + 1}{C_2} + \frac{1}{C_\pi} + \frac{1}{C_1}\right)} * (\beta + 1)R_E}$$

$$- f_{p4b} = \frac{1}{2\pi 50 * \frac{C_\mu}{1 + \frac{C_\mu}{C_1}}}$$

$$- f_{z4} = \frac{1}{2\pi R_E C_2}$$

The three last regimes exhibit poles at the same frequency.

NB :

The three last regimes exhibit poles at the same frequency, so we will note the said frequency f_{p2} for the three of them .

The given cut-off frequency values are based on the approximations , but give a good idea about the circuit operation. These values will be checked later on to ensure they are not far from the final ones and that the approximations that we have considered fit.

Based on the up said, we expect the final transfer function of the circuit to be as follows:

The high-pass filter is made by capacitor C_1 and the biasing resistor R_{bias} that we have rightfully neglected in the equations above. The cut-off frequency of the said filter is: $f_{HPF} = \frac{1}{2\pi * R_{bias} * C_1}$, (HPF stands for High-Pass-Filter).

B.2. Sizing:

Based on the explanation above, we will explain below the component sizing logic, but first, we will put a reminder of the constraints that the input buffer is supposed to meet:

- Bandwidth: $BW = [20MHz; 116GHz]$.
- Gain: $G = 0dB$.
- Input impedance: $Z_{in} = 50\Omega$.
- Output impedance: $Z_{out} = 10\Omega$.
- Noise performance: $V_{noise_{rms}} < 691\mu V$ (for $V_{pk-pk} = 1V$).

We size the components according to the following logic:

- **Output resistor:** We need an output impedance of 10Ω to match the circuit constraints, therefore $R_E = 10\Omega$.
- **Biasing resistor:** The biasing resistor R_{bias} must above all be big compared to 50Ω so that it does not affect the impedance matching scheme. We choose $R_{bias} = 20k\Omega$.
- **Decoupling capacitors:**

For capacitor C_1 , we have three main constraints:

- Bandwidth low cut-off frequency:

Indeed, the low cut-off frequency of the input buffer bandwidth is set at:

$$f_{HPF} = \frac{1}{2\pi * R_{bias} * C_1}, \text{ therefore we should have: } C_1 > \frac{1}{2\pi * 20MHz * R_{bias}},$$

i.e. $C_1 > 390fF$.

- The gain constraint:

We saw that in the third regime, the voltage gain is multiplied by $\frac{C_1}{C_1 + C_\mu}$, so in order to maximize the gain, we must have: $C_1 \gg C_\mu$.

Now we know that C_μ depends on the transistor sizing, and is mainly of the order of femtoFarads for the most high-speed transistors.

- Bandwidth high cut-off frequency :

$$\text{The high cut-off frequency is equal to: } f_{p_{4b}} = \frac{1}{2\pi 50 * \frac{C_\mu}{1 + \frac{C_\mu}{C_1}}}$$

. Therefore, we need to have: $C_1 \gg C_\mu$, which is the same constraint than before.

Based on the above considerations, we chose a C_1 value of 2pF. This value is also chosen to fit the limited layout area that we had to work with.

For capacitor C_2 , we have three constraints:

- f_{p_2} frequency :

We need the pole frequency to be as high as possible as the voltage drops afterwards. Therefore, we need to have:

$$f_{p2} = \frac{1}{2\pi * (R_E * (\beta + 1) * \frac{1}{(\frac{\beta + 1}{C_2} + \frac{1}{C_1} + \frac{1}{C_\pi})})} \quad (5.4)$$

as big as possible. We cannot for now give an exact estimation of the maximum allowed value of C_2 because the transistor values are not given yet, but we will check this constraint with simulation.

– f_{z2} frequency:

We need the zero frequency to be as close to the pole frequency so that the drop in voltage does not last long. So we need to have:

$$\frac{\beta + 1}{C_2} + \frac{1}{C_1} + \frac{1}{C_\pi} \approx \frac{\beta + 1}{C_2} \quad (5.5)$$

. This means: $C_2 < \beta * C_\pi$

– Output impedance constraint:

The output resistance of the input buffer must stay smaller than the input impedance of the sampler block so that the input buffer achieves its objective: buffering the signal. The input buffer impedance is at its lowest equal to $R_{on} + \frac{1}{sC_{hold}}$, where $C_{hold} = 1pF$. The output impedance of the input buffer is $R_E + \frac{1}{sC_2}$. We have supposed that the lowest value of R_{on} is $10\Omega = R_E$, therefore we need to have: $C_2 > C_{hold}$, i.e. $C_2 > 1pF$.

We chose $C_2 = 2pF$.

– **Transistor current**

The value of the transistor's current impacts the operation of the circuit in multiple ways, the main ones are:

* Gain value:

In the first regime, the voltage gain is the following:

$$\frac{V_{out}}{V_{in}} = 1/2 * \frac{(R_E * (\beta + 1) + \frac{(\beta + 1)}{sC_2})}{R_E * (\beta + 1) + r_\pi + \frac{(\beta + 1)}{sC_2} + \frac{1}{sC_1}} \quad (5.6)$$

Since C_1 and C_2 are equal to each other, then the gain is approximately:

$$\frac{V_{out}}{V_{in}} = 1/2 * \frac{1}{1 + \frac{r_{\pi}}{R_E * (\beta + 1) + \frac{(\beta + 1)}{sC_2}}} \quad (5.7)$$

So the smaller r_{π} compared to $R_E * (\beta + 1)$, the bigger the gain.

Now we know that: $r_{\pi} = \beta * \frac{V_t}{I_c}$, therefore, the higher the current, the lower r_{π} .

We can see that, the smaller r_{π} , the closer the gain is to 1/2.

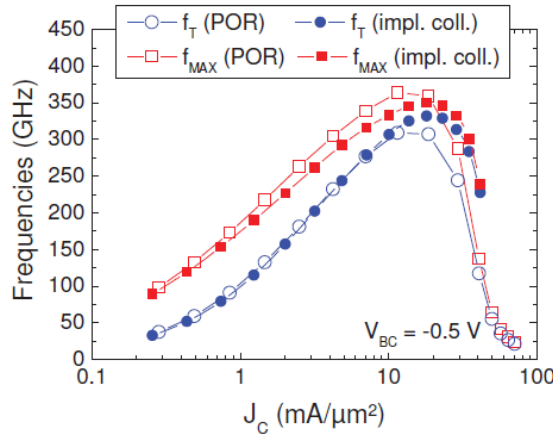


FIGURE 5.12: Transit and maximum oscillation frequency variation with the current density in BiCMOS55 HS-HBT

- * The current value impacts the frequency behavior of the transistor Q_1 : the higher the current, the higher the transit frequency as we have: $f_t = \frac{I_c}{V_t C_{\pi}}$ [122]. Indeed, to size the transistor, we use transit frequency versus current density curves (STMicroelectronics PDK) like the ones presented in fig.5.12.
In our case, we chose $I_C = 70mA$ (which matches a high transit frequency), this choice was mainly made through simulations as we only had a minimal value of 2.6mA (see previous section).

To sum up, here are the final components values:

Component	C_1	C_2	R_E	R_{bias}	I_C
Approximation	2pF	2pF	10Ω	20kΩ	70mA

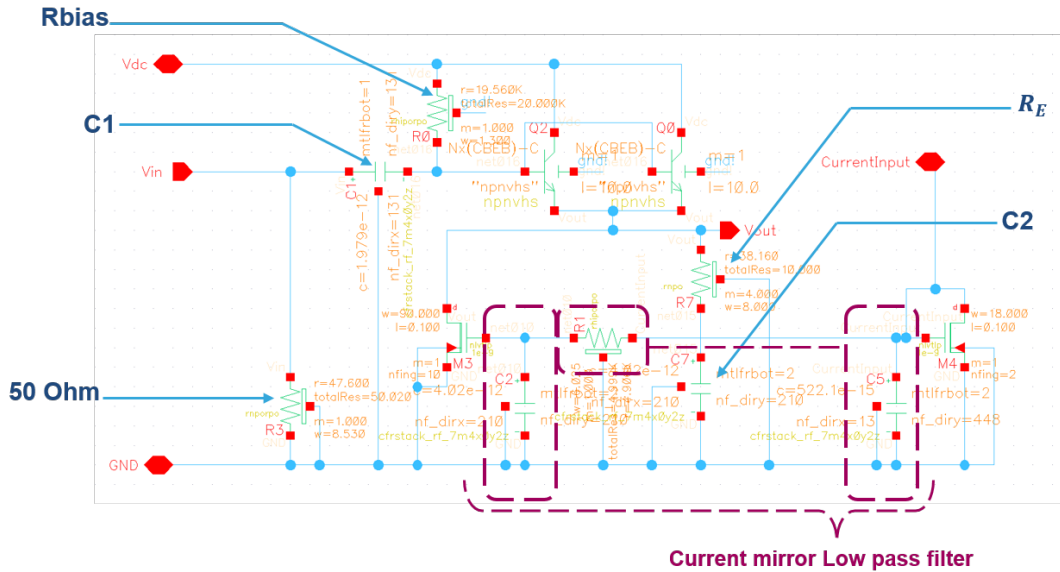


FIGURE 5.13: Input buffer final circuit scheme

B.3. Simulation

The final circuit that we have designed is the one depicted in fig.5.13.

The circuit is the same as before, but we added a low pass filter at the gates of the current mirror transistors. This would prevent signal leakage to the current mirror.

The possibility of adding a low pass filter is a main reason behind the choice of MOS transistors for the current mirror rather than bipolars.

The current injected into the circuit is 14mA, the current source multiplies the current by 5: this is done by making the second transistor of the current mirror T_2 equal to 5 transistors like T_1 in parallel.

The transistor Q_1 was sized in order to have the highest f_t as explained above.

We first started with simulating the frequency response of the circuit, the test scheme is depicted in fig.5.14.

The test scheme includes, other than the circuit, the coaxial cable 50Ω and the additional decoupling capacitors that we added in the layout at the supply and ground nodes.

The input source is set at 2V so that we get a 0dB (or approximately) curve in case the input buffer operates as expected.

We can see in fig.5.17, as expected, the different regimes at different frequencies. The ranges of the latter are very close to the approximate values that we have calculated before.

We can first see that the lower edge of the bandwidth is at 8MHz, which fits the constraints that we have set in the beginning. The upper edge is, as we can see

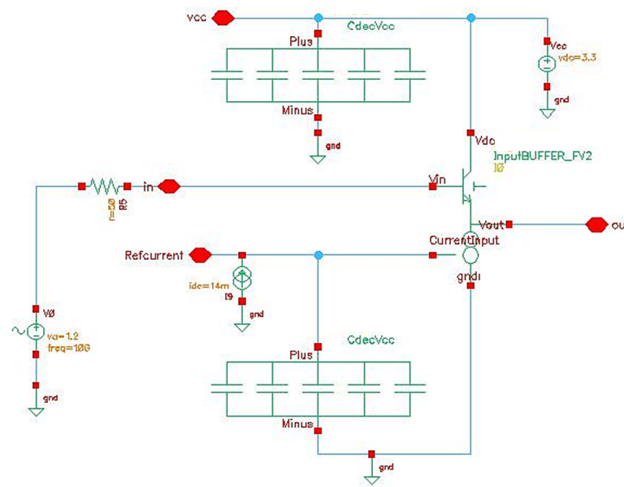


FIGURE 5.14: Input buffer test circuit scheme

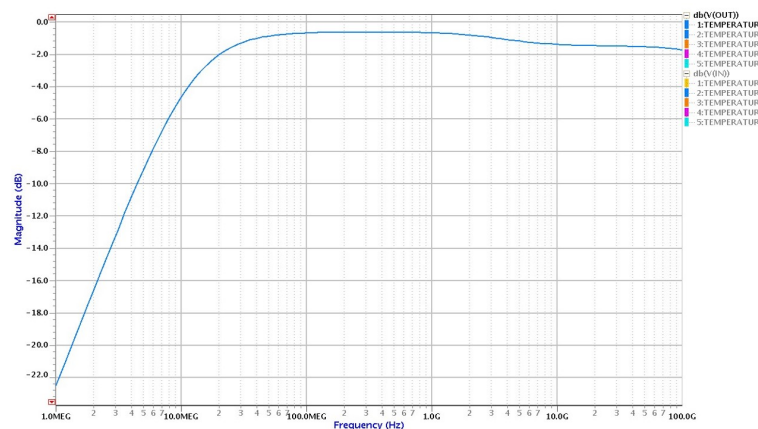


FIGURE 5.15: Input buffer AC response

higher than 100GHz. Therefore the bandwidth constraint is validated.

The gain is approximately -1.4dB around 10GHz, which does not fit perfectly the constraints but is close enough. This is not very problematic as we can adjust the input signal level in order to fit a 1V peak-to-peak signal at the output of the input buffer. This circuit is simulated at 27°C.

We have also simulated the circuit performance dependency on temperature, and the results are plotted in fig.5.16.

We can see that the gain does not change very much with temperature, indeed it exhibits only a variation of 0.01dB centered around 75°C.

Finally, we have simulated the noise performance of the input buffer. In fig.5.17, we have simulated a 1.2V input voltage source and the root mean square noise

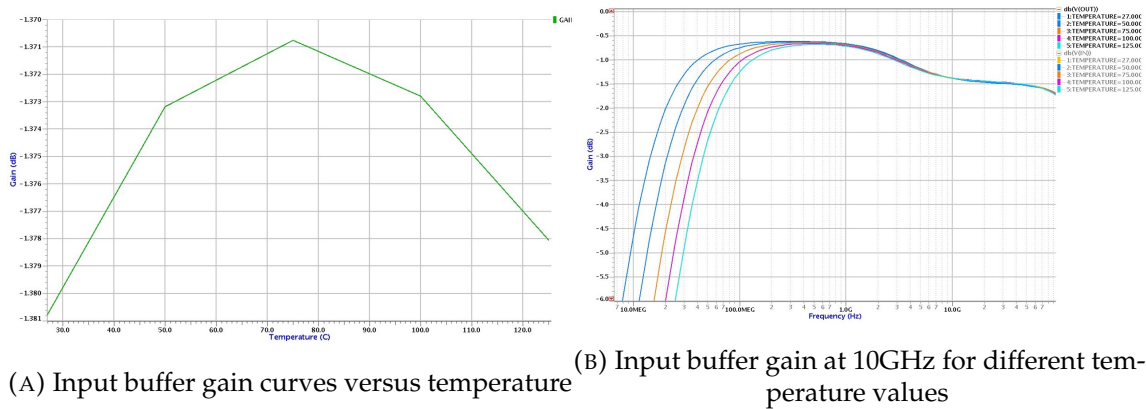


FIGURE 5.16: Input buffer gain versus temperature

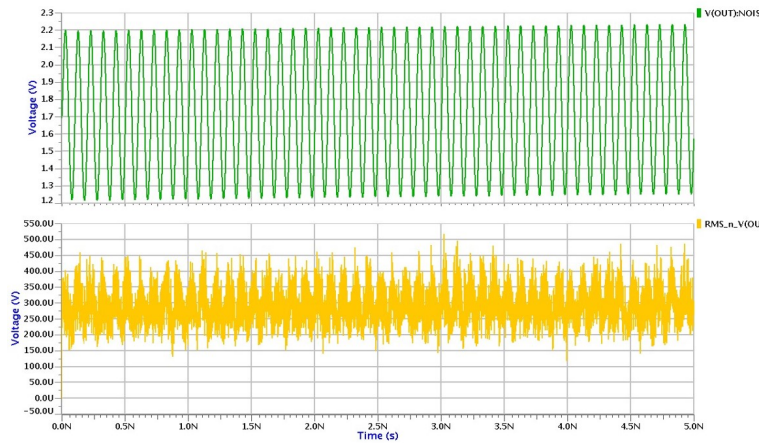


FIGURE 5.17: Input buffer AC response

voltage at the output of the input buffer.

We can see that the root mean square noise voltage is approximately $400\mu V$. If we report this value to the 1V pk-pk signal that we have in the circuit constraints, we get an average noise of about $333\mu V$, which is smaller than the constraint value ($691\mu V$).

Therefore, up till now, the simulation results confirm that the constraints of the input buffer circuit are met.

C. Layout

The input buffer final layout is plotted in fig.5.18.

The yellow rectangles are the decoupling capacitors, and we can see how they take a lot of space compared to the other components.

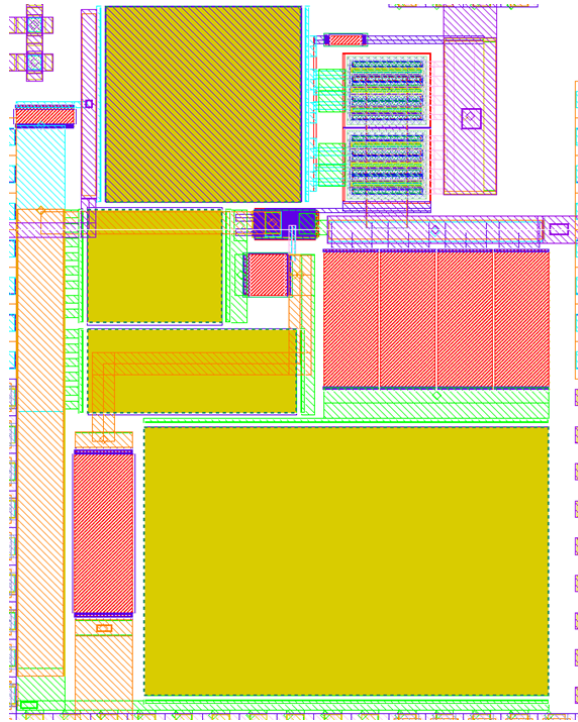


FIGURE 5.18: Input buffer layout

5.2.1 Clock generation circuit:

As explained in the previous chapter, the clock generation circuit is made of several blocks:

- The single-to-differential + biasing stage
- The amplification stage
- The 1V output stage

5.2.1.1 The single-to-differential + biasing stage

The aim of this circuit is to cover two distinct functions:

- Add a DC biasing to the single clock signal coming from the optical chip.
- Transform the single signal of the optical clock into a differential signal so that it can be properly processed by the amplification stage that comes right after.

While designing this circuit, many precautions should be taken into consideration, mainly with regards to the wire bonding and the electrical pads that the signal has to cross before reaching this circuit. That is why we have gone through many circuit designs before settling for the final circuit that will eventually be presented.

Within the forthcoming sections, we will go through the different designs that we have considered, exhibit their features and the limitations that made us discard them. These designs will be listed as numbered versions in the following sections.

A. Version 1:

The basic structure that we use for this first stage is the following:

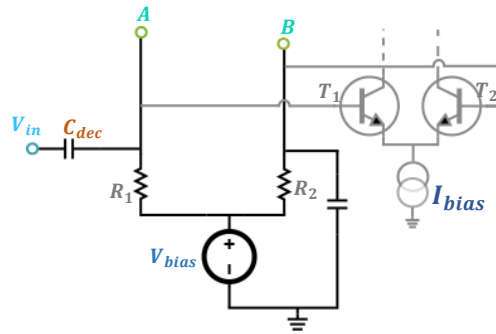


FIGURE 5.19: Basic biasing circuit

Where:

C_{dec} : a decoupling capacitor

R_1 and R_2 : biasing resistors

A and B : the input nodes of the amplification stage

V_{bias} : the voltage biasing source

C_{bias} : a decoupling capacitor at node B

T_1 and T_2 : stand for the next amplification stage entry transistors

The gray stage stands for the amplification stage that comes right after this biasing stage.

In order to fix the values of R_1 , R_2 and C_{dec} , we consider the biasing block along with the optical clock circuit and the connections in between as in fig. 5.20.

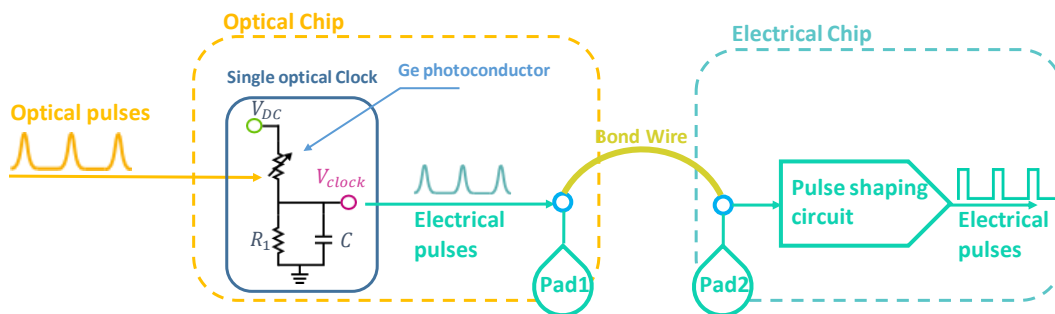


FIGURE 5.20: Clock circuit with connections explicated

In order to properly design this circuit, we first need to set models for the electrical pads and for the wire bonding that we use. This is the object of the next section.

Now we consider the small signal model of the biasing circuit in order to fix the values of its components. We actually need to consider the small signal model of the circuit including the pads in the optical and electrical chip, the wire bonding and the transistors at the input of the amplification stage.

a. Simulation models

Pads :

In order to model the electrical pads of both the electrical and the optical chip, we use STMicroelectronics' pad model given in fig.5.21.

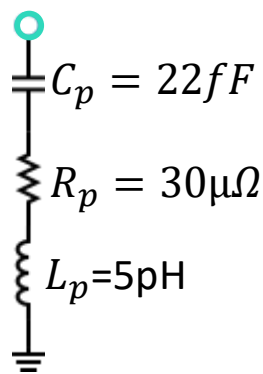


FIGURE 5.21: Pad model

Given the components' values given in this model, we will consider only the capacitor when we will model the pads in the next circuits. Indeed, the impedance of the capacitor is always higher than the other components over frequency up till : $f_{pad} = \frac{1}{2\pi\sqrt{LC}}$, where $f_{pad} \simeq 480GHz$; we have only considered the impedance of the inductance compared to the capacitor because the resistor value is far smaller than the first two, as a matter of fact, the capacitor impedance becomes comparable to the resistor's at a frequency of about: $241PHz$ ($241 \times 10^{15}Hz$).

a.2 Wire bonding :

In order to model the wire bonding, we only consider their inductance component because it is the one that affects the most the performance of the circuits. This section is aimed at explaining the logic that we have used in order to set this inductance value.

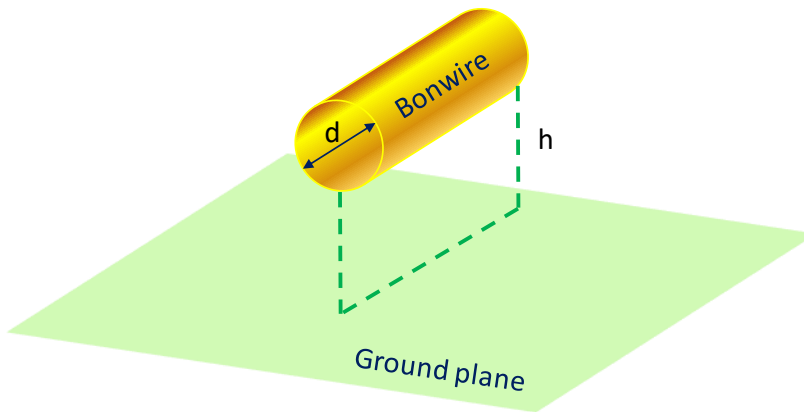


FIGURE 5.22: Wire bond inductance estimation scheme

As will be explained later, we use wire bonding to connect the supply, the ground and the signal of the optical clock.

The wires used in our case are golden wires of diameter: $d = 34\mu m$.¹

The self-inductance of each bondwire is given by [129], see fig.5.22:

$$L = 0,2 * \ln\left(\frac{2h}{r}\right)nH/mm \quad (5.8)$$

Where:

h : is the distance from the wire bond to a ground plane, in our case h is about $675\mu m$.

r : is the wire bond radius.

In the up-said approximation, we took the basic case of a flat wire bonding over a ground plane. In reality, the wire bonding that we use is a curved one, which makes the self-inductance calculus slightly more complicated. We will all the same keep this equation as it is still a good approximation to the final inductance value.

Therefore, the self inductance of the used wire bonds is approximately: $0,875nH/mm$. In the forthcoming equations, we will round this value and consider the wire bonds to have a self-inductance of $1nH$ each.

There is also another factor to take in consideration for the inductance estimation: the mutual inductance between the wires. Indeed, as depicted in fig.5.23, the signal wire bonding is surrounded by the supply and ground wire bonds.

The mutual inductance in our case, considering the upsaid height of the wires, and a distance of $100\mu m$ between each two (distance between pads) is given by:[130]

¹These values are given by Gamberini company where the chips assembly was expected to be achieved, see: <http://www.microelectronics-sc.com>

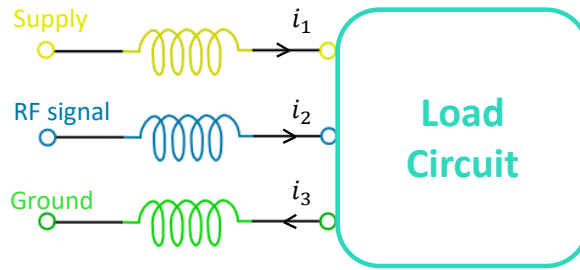


FIGURE 5.23: Wire bonding connections and mutual inductance illustrated

$$M = 0.1 \times \ln\left(1 + \left(\frac{2h}{d}\right)^2\right) nH/mm \quad (5.9)$$

Which amounts to a mutual inductance of roughly $50nH/mm$.

We must point out that this is an overestimation of the mutual inductance since the distance between the two wires is at its minimal value equal to the spacing of the pads, namely $100\mu m$. We have also made the approximation that the wire bonds are flat where they are in reality curved, which reduced noticeably the mutual inductance.

In reality, based on STMicronics models, the mutual coupling coefficient is about: $k = 0.4$, where:

$$k = \frac{M * 1mm}{\sqrt{L_1 * L_2}} \quad (5.10)$$

In fig.5.23, each one of the supply and ground coils currents, i_1 and i_3 , yields a magnetic field, respectively: B_1 and B_3 . Part of these magnetic fields is coupled into the signal coil: L_2 , with a coupling coefficient of $k = 0.4$.

That means that the total field that is coupled into L_2 is equal to:

$$B_{tot} = B_2 + k * (B_1 - B_3) \quad (5.11)$$

The magnetic fields are proportional to the current that induced them:

$$B_j = \frac{\mu_0 * \mu_r * i_j}{D} \quad (5.12)$$

Where:

μ_0 : the permeability of free space.

μ_r : the relative permeability of air (approximately 1).

D : the distance at which the magnetic field is measured.

We suppose that the wire bonds that we use are identical and that the distance supply-to-signal wire bond and ground-to-signal wire bonds are the same, which is a good approximation.

The electrical neutrality of the circuit implies that:

$$i_1 + i_2 = i_3 \quad (5.13)$$

Therefore, we can assume that:

$$B_1 + B_2 = B_3 \quad (5.14)$$

So that:

$$B_{tot} = B_2 + k * (B_1 - B_3) = (1 - k) * B_2 \quad (5.15)$$

This amounts to say that, for a given value of current across the signal coil, the induced magnetic field is $(1 - k)$ times smaller than the magnetic field induced by this coil in the absence of the other coils. This means that the wire bond exhibits a total inductance of smaller value than its internal inductance, that we estimated earlier to be equal to 1nH per wire bond; we rather have: $L_2 = (1 - k) * 1nH = 0.6nH$

The previous discussion was meant to show that, when we will take the approximation of a 1 nH inductance for the signal wire bond, this will be rather a consideration for the worst case and not the other way around. It is though important to say that we made a lot of assumptions before we reached the 0,6nH value, which are mainly: the flat wire bond approximation and the perfectly identical and equally spaced wire bonds. Therefore, it is safe now to go with the 1nH approximation.

b. Sizing study

Now that we have set the models we will be working with, we will attempt at listing the circuit components' constraints that the sizing must take into consideration. To do so, we will study the circuit's transfer function.

b.1 Transfer function :

The small signal model of the total biasing circuit is given in fig.5.24, where C_{trans} is the input equivalent capacitor of the transistors of the amplification stage, and we have:

$$C_{trans} = C_{\pi} + (1 + G) * C_{\mu} \quad (5.16)$$

G being the gain of the first transistor stage.

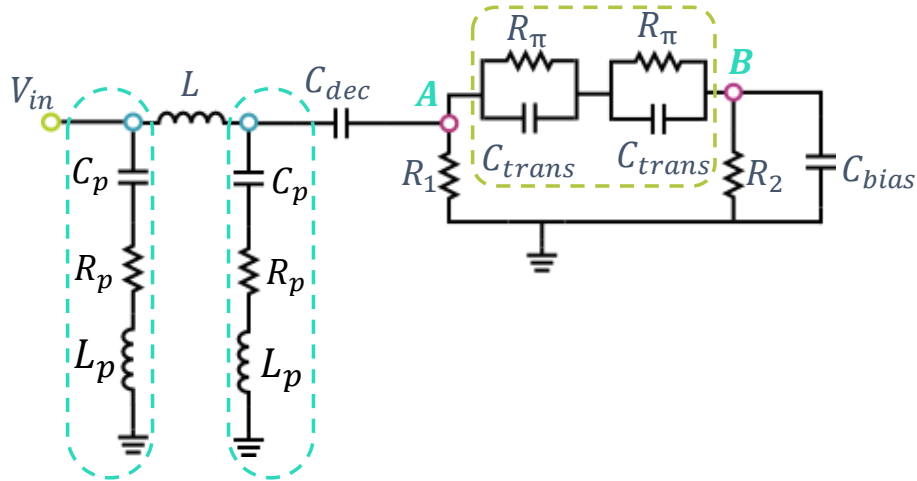


FIGURE 5.24: Small signal model of the complete circuit of biasing

We have:

$$\frac{V_{AB}}{V_A} = \frac{\frac{2R_\pi}{1 + jR_\pi\omega C_{trans}}}{\frac{2R_\pi}{1 + jR_\pi\omega C_{trans}} + \frac{R_2}{1 + jR_2\omega C_{bias}}} \quad (5.17)$$

Then:

$$\frac{V_{AB}}{V_A} = \frac{2R_\pi * (1 + j\omega R_2 C_{bias})}{2R_\pi * (1 + j\omega R_2 C_{bias}) + R_2 * (1 + j\omega R_\pi C_{trans})} \quad (5.18)$$

$$\frac{V_{AB}}{V_A} = \frac{2R_\pi * (1 + j\omega R_2 C_{bias})}{(2R_\pi + R_2) + j\omega(R_2 C_{bias} + R_\pi C_{trans})} \quad (5.19)$$

At this point, we can see that the transfer function between V_{AB} and V_A ($\frac{V_{AB}}{V_A}$) exhibits a pole and a zero as follows:

- Pole at frequency:

$$f_{p1} = \frac{1}{2\pi * (2R_\pi \parallel R_2)(C_{bias} + C_{trans}/2)} \quad (5.20)$$

- Zero at frequency:

$$f_{z1} = \frac{1}{2 * \pi * R_2 C_{bias}} \quad (5.21)$$

We can now express this first transfer function as follows:

$$\frac{V_{AB}}{V_A} = \frac{2R_\pi}{2R_\pi + R_2} * \frac{(1 + j\omega/2\pi f_z)}{(1 + j\omega/2\pi f_p)} \quad (5.22)$$

NB : As explained early on, the biasing resistors R_1 and R_2 need to be identical. Therefore, within the forthcoming sections, we will consider just R_1 in the calculations.

In fig.5.25, we have plotted the transfer function of $\frac{V_{AB}}{V_A}$.

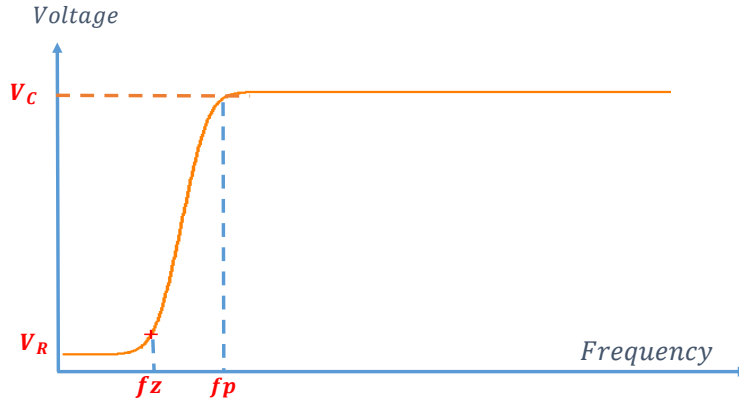


FIGURE 5.25: Transfer function of $\frac{V_{AB}}{V_A}$

We have:

$$V_R = \frac{2 * R_\pi}{2 * R_\pi + R_1} \quad (5.23)$$

And:

$$V_C = \frac{1}{1 + \frac{C_{trans}/2}{C_{bias}}} \quad (5.24)$$

We can already state that, in order to have an acceptable biasing performance, we need V_C to be equal to 1. This amounts to having:

$$C_{trans}/2 \lll C_{bias} \quad (5.25)$$

Now back to the final transfer function. Within the forthcoming equations, we will not consider the pads. Indeed, given the value of their impedance, they will not impact much the calculations.

We have:

$$\frac{V_A}{V_{in}} = \frac{Z}{Z + j\omega L + \frac{1}{j\omega C_{dec}}} \quad (5.26)$$

With:

$$Z = \frac{R_Z}{1 + j\omega R_Z C_Z} \quad (5.27)$$

Where:

$$R_Z = (R_2 + 2R_\pi) // R_1 \quad (5.28)$$

And:

$$C_Z = \frac{C_{trans}}{2} \text{series} C_{bias} \quad (5.29)$$

So that:

$$\frac{V_A}{V_{in}} = \frac{\frac{R_Z}{1 + j\omega R_Z C_Z}}{\frac{R_Z}{1 + j\omega R_Z C_Z} + j\omega L + \frac{1}{j\omega C_Z}} \quad (5.30)$$

$$\frac{V_A}{V_{in}} = \frac{R_Z}{R_Z + (1 + j\omega R_Z C_Z)(j\omega L + \frac{1}{j\omega C_{dec}})} \quad (5.31)$$

We have therefore a pole at:

$$f_{p2} = \frac{1}{2\pi\sqrt{LC_{dec}}} \quad (5.32)$$

The final transfer function is, by combining equations eq.5.22 and eq.5.31:

$$\frac{V_{AB}}{V_{in}} = \frac{R_Z}{R_Z + (1 + j\omega R_Z C_Z)(j\omega L + \frac{1}{j\omega C_{dec}})} * \frac{1}{1 + \frac{R_1}{2 * R_\pi}} * \frac{(1 + j\omega/2\pi f_z)}{(1 + j\omega/2\pi f_p)}$$

To sum up, the transfer function is as depicted in fig.5.26.

It exhibits the following features:

- A pole at:

$$f_{p1} = \frac{1}{2\pi * (2R_\pi || R_2)(C_{bias} + C_{trans}/2)} \quad (5.33)$$

- A second pole at:

$$f_{p2} = \frac{1}{2\pi\sqrt{LC_{dec}}} \quad (5.34)$$

- A zero at frequency:

$$f_{z1} = \frac{1}{2 * \pi * R_2 C_{bias}} \quad (5.35)$$

As we can see in fig.5.26, the circuit experiences a ringing at frequency:

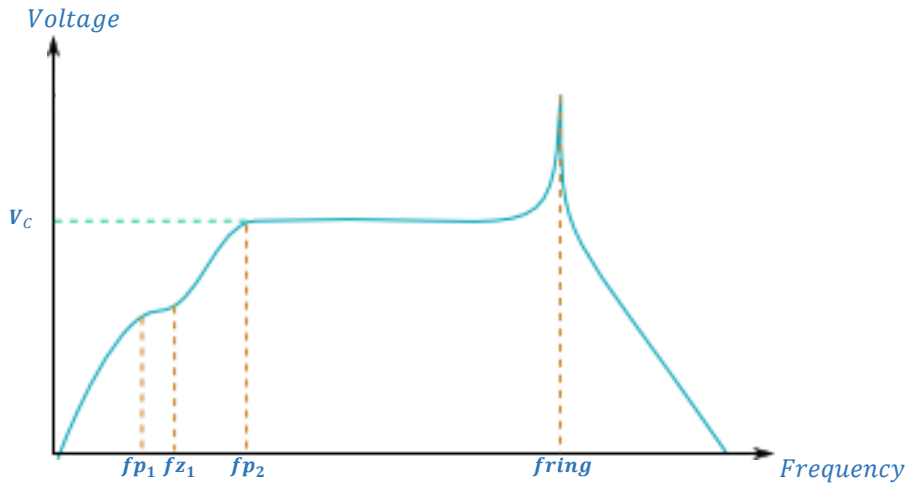


FIGURE 5.26: Transfer function of the biasing stage.

$$f_{ring} = \frac{1}{\sqrt{L(C_{dec}seriesC_{trans}/2seriesC_{bias})}} \quad (5.36)$$

In the following section we will explain the effect of each of these frequencies on the final response, and how we must accommodate the design components based on these effects.

b.2 Poles and zero frequencies effect :

The main constraint when it comes to the poles and zero frequencies is for them to be inferior to 100MHz. Indeed, the lower edge of the biasing stage bandwidth is set by these frequencies, and especially by the second pole frequency.

This amounts to the following specifications:

$$\frac{1}{2 * \pi * R_1 C_{bias}} < 100MHz \quad (5.37)$$

And:

$$\frac{1}{2\pi\sqrt{LC_{dec}}} < 100MHz \quad (5.38)$$

And

$$\frac{1}{2\pi * (2R_{\pi} \parallel R_1)(C_{bias} + C_{trans}/2)} < 100MHz \quad (5.39)$$

We should also consider the constraint related to the gain within the biasing circuit bandwidth:

$$V_C = \frac{1}{1 + \frac{C_{trans}/2}{C_{bias}}} \cong 1 \quad (5.40)$$

The up-said constraints translate into the following specifications:

We start first with the gain constraint (see eq.5.40), which translates into:

$$C_{bias} \gg \gg C_{trans}/2 \quad (5.41)$$

Now since:

$$C_{trans}/2 = (C_{\pi} + (1 + G) * C_{\mu})/2 \quad (5.42)$$

Where G is the gain of the amplification stage input differential pair.

For C_{π} and C_{μ} , we consider here the values of the smallest transistor in the technology to set a minimal value of C_{bias} . We also consider a ratio of 100 as enough to consider that:

$$C_{bias} \gg \gg C_{trans}/2 \quad (5.43)$$

We must then have:

$$C_{bias} > 2pF \quad (5.44)$$

We have not discussed the value of the gain (G) that we considered because the capacitor C_{π} is way higher than C_{μ} in a way that makes the gain value obsolete.

Now if we take the first constraint:(eq.5.37), and couple it to the last specification on C_{bias} , we get:

$$R_1 > 769\Omega \quad (5.45)$$

This same specification goes for the resistance $2R_{\pi} \parallel R_1$ (see eq.5.39).

The last constraint that we consider is the one stated in eq.5.38, which amounts to say:

$$C_{dec} > 2.5nF \quad (5.46)$$

To sum up, the poles and zero frequencies have the following constraints:

-

$$C_{bias} > 2pF \quad (5.47)$$

-

$$R_1 > 769\Omega \quad (5.48)$$

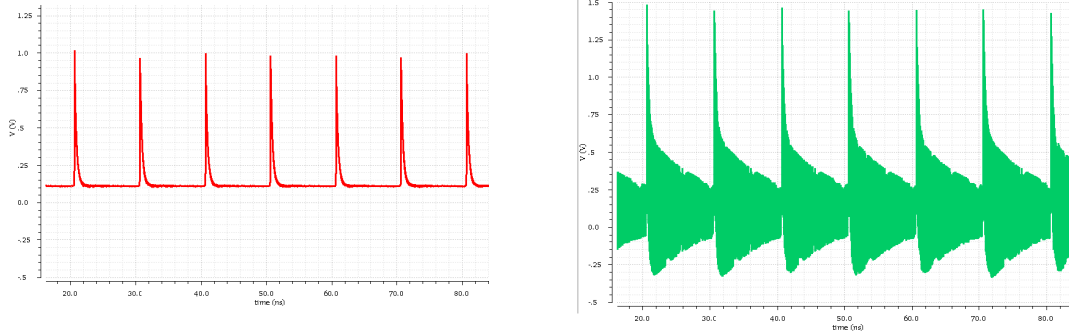
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$$C_{dec} > 2.5nF \quad (5.49)$$

b.3 Ringing frequency effect :

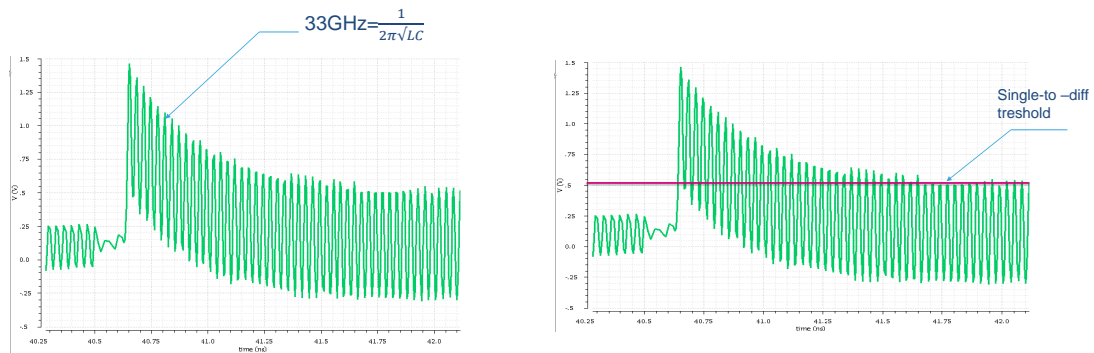
Before we dive into the specifications related to the ringing frequency, we will first illustrate the effect that it has on the circuit response and in which it affects the total biasing circuit performance.

For this sake, we simulated the biasing circuit response with R_1 being $200k\Omega$. The electrical signal at the biasing stage input was plotted in fig5.27a(right before the wire bonding). We plotted the electrical signal at node A of the biasing circuit in fig.5.27b.



(A) Signal at the output of the optical clock circuit(B) Signal at the input of the pulse shaping circuit

The signal becomes more "jittery" after the wire bond which is due to the ringing frequency that we have calculated before.



(A) Ringing effect on the input signal (B) Effect of the ringing frequency on the decision taking

FIGURE 5.28: Zoom in the effect of ringing frequency on biasing stage

If we take a closer look at the signal at node A, as depicted in fig.5.28a, we can clearly see the presence of the ringing frequency. The latter is annoying in the sense that it prevents the next stage, the amplification stage, from operating accurately. Indeed, if we consider a decision taking voltage, as depicted in fig.5.28b, we can see that this threshold is reached multiple times within a pulse width, which makes this stage obsolete.

Therefore, the ringing must be eliminated (out of the used bandwidth) or attenuated beyond what the decision making stage can detect, i.e. 26mV.

As said earlier, the ringing occurs at frequency:

$$f_{ring} = \frac{1}{2\pi \sqrt{L(C_{dec}seriesC_{trans}/2seriesC_{bias})}} \quad (5.50)$$

Since the two biasing capacitors will be necessarily way bigger than the capacitor $C_{trans}/2$, then:

$$f_{ring} = \frac{1}{2\pi \sqrt{LC_{trans}/2}}$$

At this frequency, the amplitude of the signal is equal to:

$$V(f_{rin}) = 2\pi * C_Z * R_Z \quad (5.51)$$

Namely:

$$V(f_{rin}) = 2\pi * (C_{trans}/2seriesC_{bias}) * ((R_1 + 2 * R_\pi) \parallel R_1) \quad (5.52)$$

The amplitude of the ringing signal needs to be smaller than the threshold of what the amplification stage can detect, namely $V_t = KT/e$. This translates into having:

$$R_1 < 3.5\Omega \quad (5.53)$$

With the same considerations taken in the previous subsection, we estimate the ringing frequency to be at least equal to: 35 GHz (smallest input transistors that the technology allows).

c. Conclusion

So far, we have the following constraints for this first version of the biasing circuit:

- $C_{bias} > 2pF$ (5.54)
- $R_1 > 769\Omega$ (5.55)
- $R_1 < 3.5\Omega$ (5.56)
- $C_{dec} > 2.5nF$ (5.57)
- $\frac{1}{2\pi\sqrt{LC_{trans}/2}} \gg 16GHz$ (5.58)

This biasing structure features many problems, the main one being: the contradicting value of R_1 that both gives a small ringing amplitude and a wide bandwidth. There is also the low ringing frequency and the high constraint on the C_{dec} . Indeed, since the L pole is at the upper edge of the bandwidth, its low value causes the loss of the steep rising edge of the optical pulse, b.

B. Version 2:

Given the up-said biasing circuit constraints, we tried to implement another biasing circuit, the one depicted in fig.5.29.

Biasing circuit 1 The first biasing circuit we tried to implement is the following: (see fig.5.29)

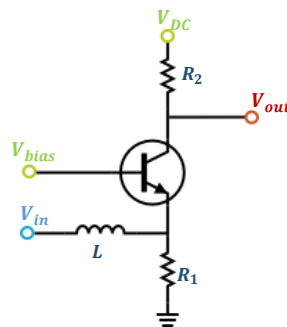


FIGURE 5.29: Biasing circuit: version 2

The aim of this circuit is to couple the signal without adding a decoupling capacitor, and therefore without having the low LC_{dec} pole problem.(see eq.5.38).

For this circuit, we have the following input impedance:

$$R_{in} = j\omega L + R_1 \parallel \frac{1}{g_m} \parallel C_\pi \quad (5.59)$$

And the circuit features the following poles and zeroes:

- A pole at:

$$f_{p1} = \frac{g_m}{2\pi C_\pi} \quad (5.60)$$

- A second pole at:

$$f_{p2} = \frac{R_1 \parallel 1/g_m}{2\pi L} \quad (5.61)$$

- A ringing frequency at:

$$f_{ring} = \frac{1}{2\pi\sqrt{LC_\pi}} \quad (5.62)$$

This circuit, even though it allows us to get around the decoupling capacitor problem, features other problems:

- Very low input impedance:
At lower frequencies, the input impedance is effectively equal to $1/g_m$ which may alter the operation of the optical pulse circuit.
- Low L pole: The L pole in this case is also the upper bandwidth limit. However, as we can see in eq.5.61 this pole is very low, namely: 4GHz if we consider that the current crossing the transistor is of 1mA.

If we want to push this pole on the upper edge, we would have to use very small values of biasing current and therefore, very high values of R_2 , which is detrimental both to the noise and the frequency performance of the circuit.

Another way to push this pole is to use a resistance between the emitter of the transistor and the input node of the circuit. This resistance would add to the $1/g_m$ resistance and increase the cutoff frequency. However, most of the voltage would be applied to this resistance and not to the transistor, and therefore we would have to make an extra effort to amplify the signal. More precisely we would have to use again a bigger resistance R_2 .

Given all that has been said earlier, we discarded this structure.

One may think that using a basic common emitter structure would be a good biasing circuit. However, this structure would imply to degenerate the emitter with a resistance and falling again in the problem of using a bigger resistance at the collector node, plus the fact that there is not enough voltage headroom for this degeneration.

C. Version 3:

Given all that has been said before, we implemented the following solution (see fig.5.30):

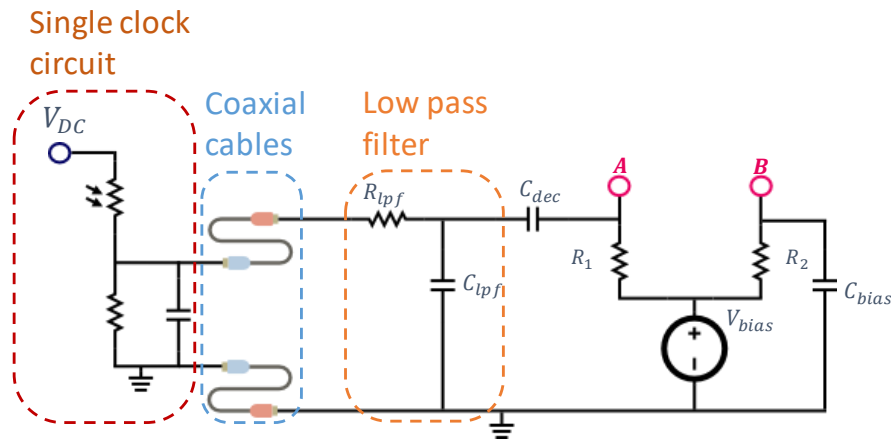


FIGURE 5.30: New biasing stage circuit scheme

This new circuit is based on the addition of a low pass filter right before the biasing stage. The aim of this being to attenuate the ringing frequency while preserving the signal bandwidth.

This new circuit has advantages and drawbacks: Indeed, this circuit brings an attenuation of about 20dB to the ringing since we chose the cutoff frequency to be: $f_{LPF} = 3.4GHz$. However, in the other side, it also attenuate part of the signal bandwidth (up to 16GHz). The direct consequence of this attenuation would be an increase in the total width of the pulse, but we can get around this problem by choosing a voltage threshold for the amplification stage that is higher than before.

The final circuit scheme implemented is depicted in fig.5.31, the layout of the up-said circuit will be given later on along with the total clock generation circuit.

5.2.1.2 The amplification stage

For the amplification stage, we chose to use a double Cherry-Hooper amplifier stage. This circuit is widely used for broadband amplifier design in biCMOS technologies, mainly because its gain and bandwidth can be set and adjusted independently [131] [132], which offers a big flexibility to designers.

The Cherry-Hooper amplifier basic circuit is depicted in fig.5.32.

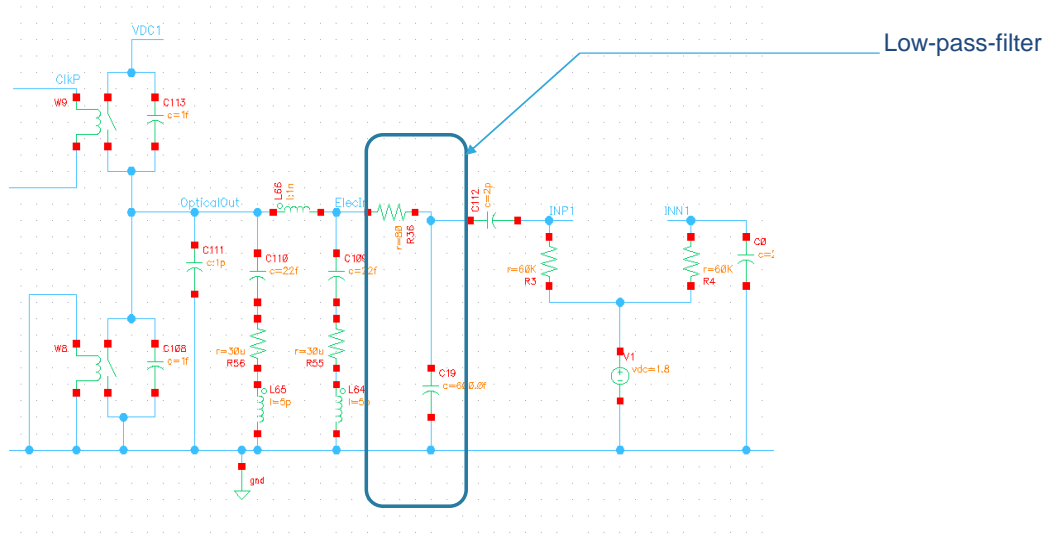


FIGURE 5.31: New single to differential stage

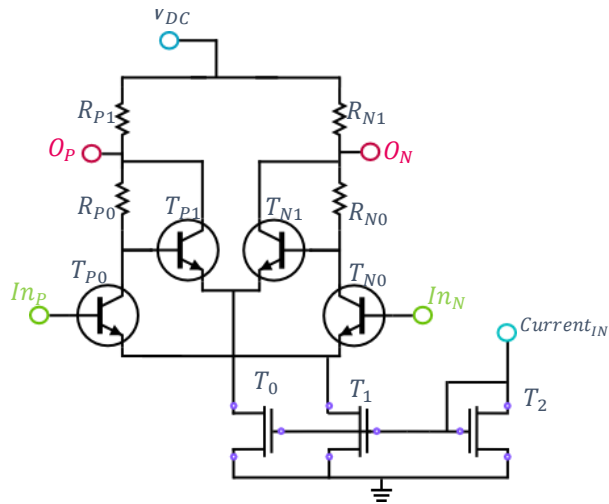


FIGURE 5.32: Cherry Hooper basic circuit

If we consider that the first set of transistors, T_{P0} and T_{N0} , have a trans-impedance of g_{m0} and, likewise, if we consider the trans-impedance of the second set of transistors: T_{P1} and T_{N1} as g_{m1} , then: the gain of the Cherry-Hooper stage can be approximated by:

$$A \approx \frac{g_{m0}R_0}{1 + j\omega C_l/g_{m1}} \quad (5.63)$$

Where C_l is the equivalent capacitance at the output node.

This formula brings more to perspective the main advantage of Cherry-Hooper design, which is the possibility of tuning gain and bandwidth independently.

We only have to take into consideration the voltage drop through R_{P1} and R_{P2} as it experiences both I_1 and I_2 at DC. This limitation is the main one we should

take into account while setting the values of the Cherry-Hopper components.

We have chosen to use two successive Cherry-Hooper stages rather than just one in order to cover the amplification constraint along with the high bandwidth constraint.

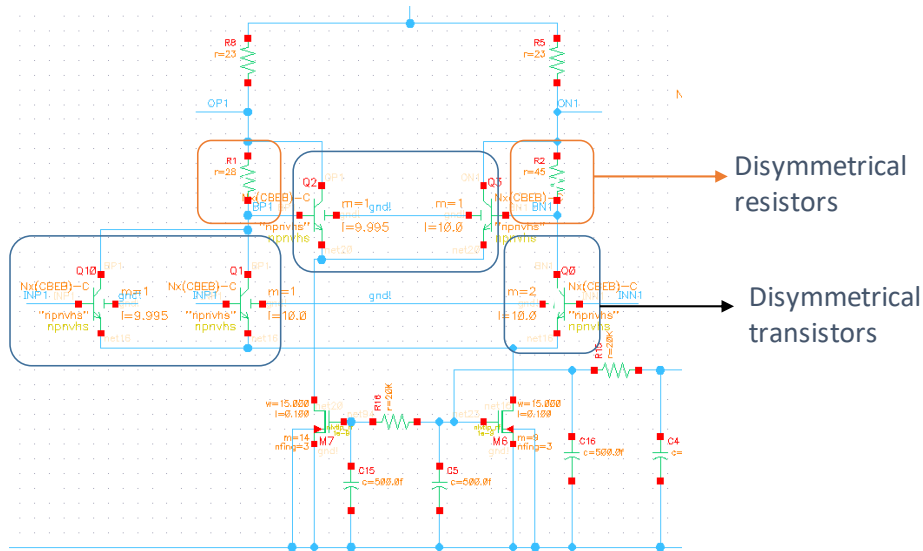


FIGURE 5.33: First Cherry Hooper stage

Given the particular features of the input signal, i.e. the asymmetrical signal at the input of the amplification stage, we chose to use an asymmetrical first Cherry-Hooper stage. This will emphasize the amplification of the signal that enters at node P and make it easier to obtain a symmetrical signal at the end without using a big amplification gain.

For this sake, we used a slightly smaller resistance value at R_{P0} value compared to R_{N0} and a slightly smaller transistor T_{P0} compared to T_{N0} as can be seen on fig.5.33. The second set of transistors and resistors need not be changed since only the first ones impact the gain as explained above. Indeed, it would even be a bad idea to touch on the second set of components since that would create two output nodes with different bandwidths.

We tried to keep the resistors as small as possible and rather play on the trans impedance values for two different considerations:

- Noise considerations: we try to keep the noise contribution of the amplification circuit as small as possible since it is the key performance of this whole design.

This is why we kept the values of R_{P1} and R_{N1} as small as possible as they are the main contributors at the output of this stage (provided R_{P0} and R_{N0} are bigger, which is most probably the case since they are used for gain).

- As said earlier, the second set of resistors, namely R_{P1} and R_{N1} receives the sum of the two currents I_0 and I_1 . Therefore, we need the latter set of resistors to be small enough so that the voltage drop across it does not make the second set of transistors saturate.

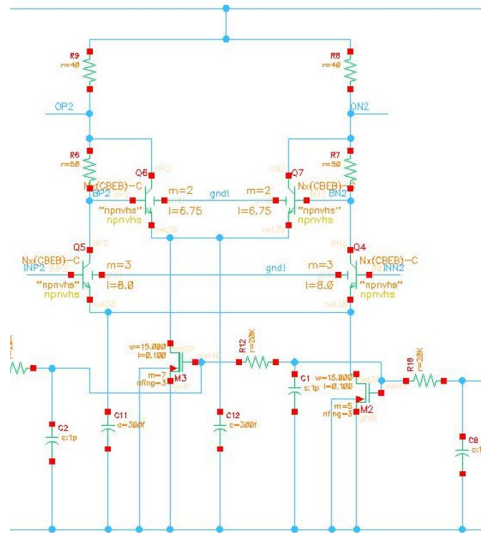


FIGURE 5.34: The second Cherry-Hooper stage

The second Cherry Hooper stage is a regular one (symmetrical branches) with a smaller gain value compared to the first one (first stage 27dB and second stage 18dB).

5.2.1.3 The 1V output stage

The 1V stage specifications and design have been already explained in the previous chapter.

To sum up, we use a basic common emitter structure with 50Ω resistors at the output, and a biasing current of 40mA.

5.2.1.4 Final circuit

The final pulse-shaping stage circuit is depicted in fig.5.35.

Given all that has been said, we simulated the total circuit with the following stimuli:

- The on resistance is 10Ω in the on state and 5000Ω in the off state.
- The biasing voltage of the circuit is about 2V.

We have first run a transient simulation in order to see if the circuit achieves the target operation. To do so, we use the circuit in fig.5.36 in order to model the behavior of the optical clock.

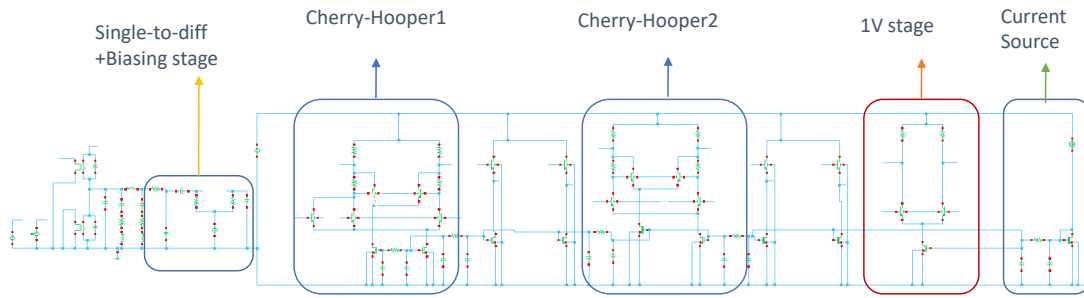


FIGURE 5.35: Final design of the pulse-shaping circuit

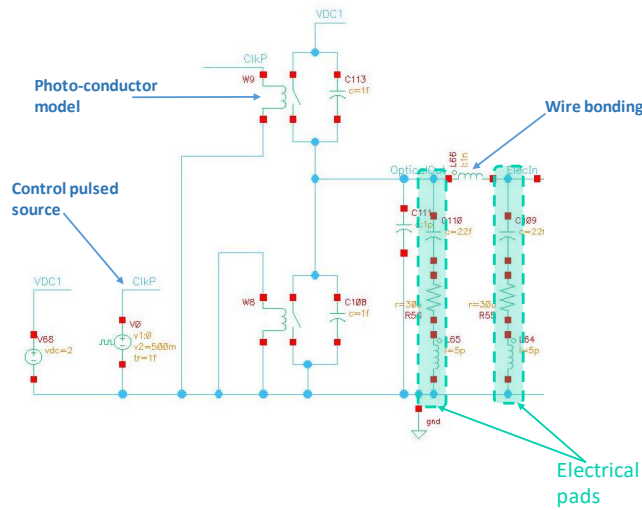


FIGURE 5.36: Optical clock electrical model

As we can see, the photo-conductors are modeled by switches with different resistance values that change according to the control voltage. The latter is modeled by the control pulsed source. We have also depicted the pads and the wire bonding model.

In fig.5.37, the signal evolution through the circuit has been depicted.

For this simulation, we have considered the following settings:

V_{supply}	V_{clock}	V_{bias}
3.3V	2V	1.8V

Where: V_{supply} is the supply voltage value for the electrical pulse shaping circuit, V_{clock} the DC voltage applied to the optical clock circuit and V_{bias} the voltage applied to to bias the single optical clock signal.

The first signal on fig.5.37 stands for the laser pulses. In order to model the latter, we used a voltage pulse source that delivers 3.4ps long pulses every 10ns and drives the photo-conductors. With Cadence Virtuoso + Eldo, we can use a pulsed source with a given jitter value, in our case we set the jitter at 11fs.

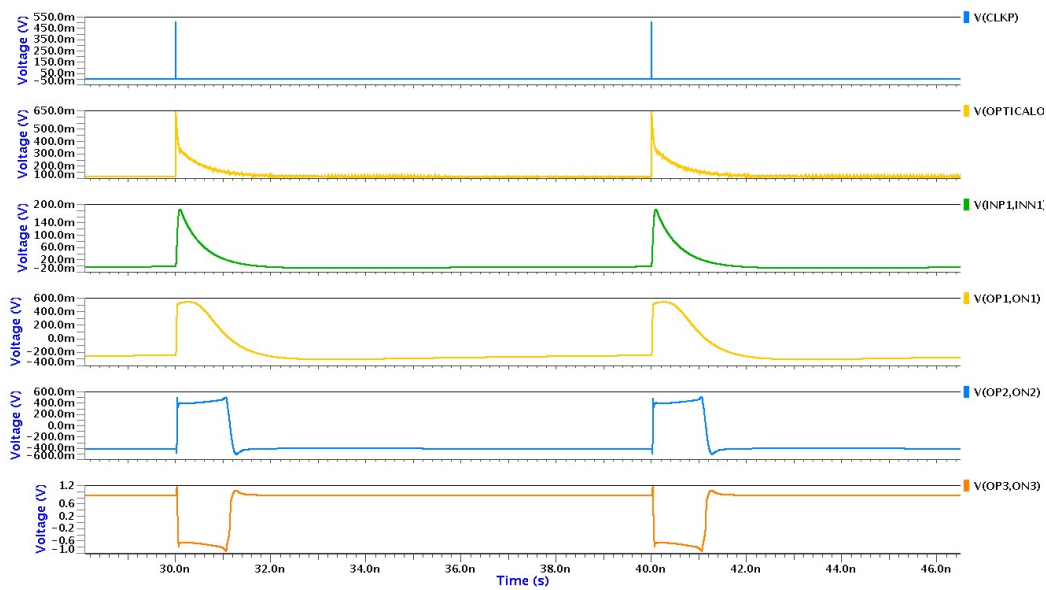


FIGURE 5.37: Signal evolution through the pulse-shaping stage

The second signal is the signal at the output of the optical clock, and its fall time here only takes into account the electrical fall time due to the R_{off} and C_{hold} . The third signal is the signal that is injected into the first Cherry-Hooper stage, at this point the signal has been transformed into a differential signal and the DC biasing has been added.

The three last signals refer to the evolution through the two Cherry-Hooper stages and the 1V stage at the end. With the up said values, the current consumption of the block is 227mA.

NB : The pulse duration in this case is $1.07ns$ which fits the specifications (pulse longer than $600ps$). However, this value can be modified as to fit exactly the $600ps$ long pulse specification by changing the biasing voltage of the single-to-differential stage.

Indeed, as explained before, we kept this biasing voltage unset so that we can use the same pulse shaping circuit for different optical clock circuits.

In this simulation, we presumed that the photo-conductor resistance goes from one value to another within 3ps. This approximation is not very accurate but is adequate to evaluate the jitter added solely by the pulse-shaping circuit.

We ran a noise tran simulation with the following parameters:

f_{min}	f_{max}	Number of runs	V_{supply}	V_{clock}	V_{bias}
0	$10^{12}Hz$	40	3.3V	2V	1.8V

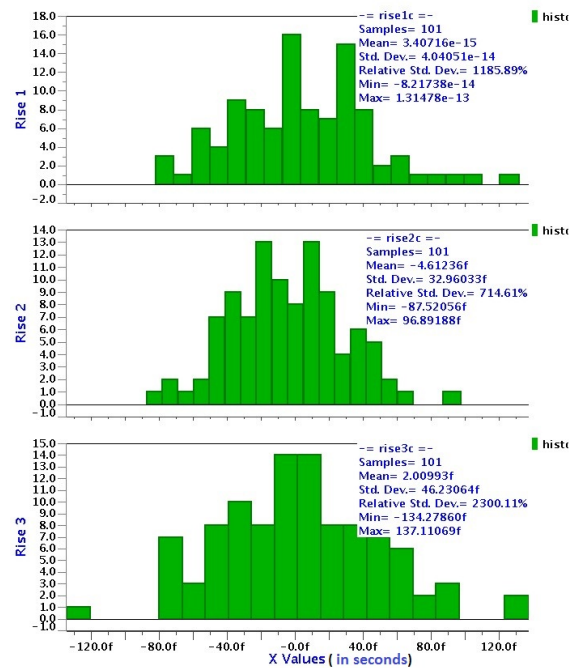


FIGURE 5.38: Jitter performance across the pulse shaping stage

We have plotted a histogram for the different runs that sums up the jitter evolution through the different blocks of the circuit as depicted in fig.5.38.

We can see that the final jitter value is approximately equal to 46fs which is still below the electronic clocks literature values.

NB :

Given the value of f_{min} , we could have relied on one run in order to estimate the jitter contribution of the stage. Indeed, when f_{min} is set at 0, the noise sources are modeled through the addition of multiple square sources with different amplitudes and pulse widths at the nodes of the circuit. This is not the case when f_{min} is not equal to 0: the noise is then modeled through sine wave sources' addition. Now we know that a square source has a much wider spectrum than a sine wave source, which makes our simulation much more accurate. The need for multiple runs does not stand anymore, but we chose to go for multiple runs anyway for double accuracy.

The final layout of the pulse shaping circuit is presented in fig.5.39. This layout is a quite accurate reproduction of the simulation circuit, only decoupling capacitors have been added on the supply and ground nodes whenever it was possible.

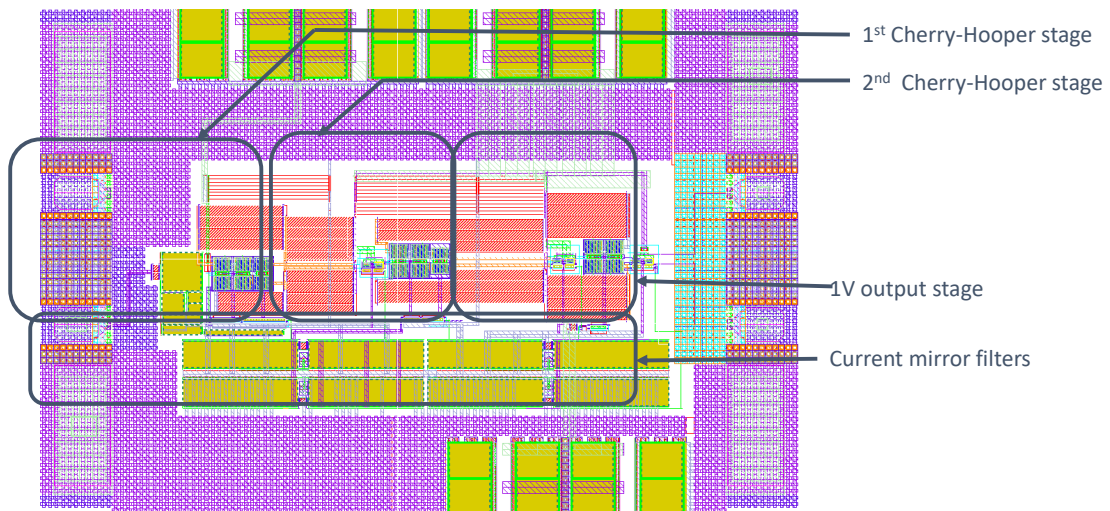


FIGURE 5.39: Final layout of the pulse-shaping circuit

5.2.1.5 Conclusion

The design of the single clock generation circuit shows good simulation results. Indeed the circuit covers the following constraints:

- Bandwidth of $100MHz$ up to $16GHz$
- Gain of approximately $60dB$.
- $1V$ output signal.
- Final jitter of less than $50fs$.

We have used two Cherry-Hooper stages in order to achieve the final gain along with the bandwidth. The $1V$ stage does also contribute to the final gain.

In designing the first Cherry-Hooper stage, we have chosen asymmetrical components in order to create a symmetrical output signal out of the asymmetrical input signal. We could have achieved the same with a regular symmetrical Cherry-Hooper stage, however, this would mean to aim for a higher gain.

This circuit can be optimized furthermore in order to decrease the noise contribution to the total jitter value.

5.3 Double clock generation circuit

As said in the previous chapter, the double clock circuits are made by using logical latches. The latter receives the two electrical pulses the clock creates and turns them into a big pulse whose duration is equal to:

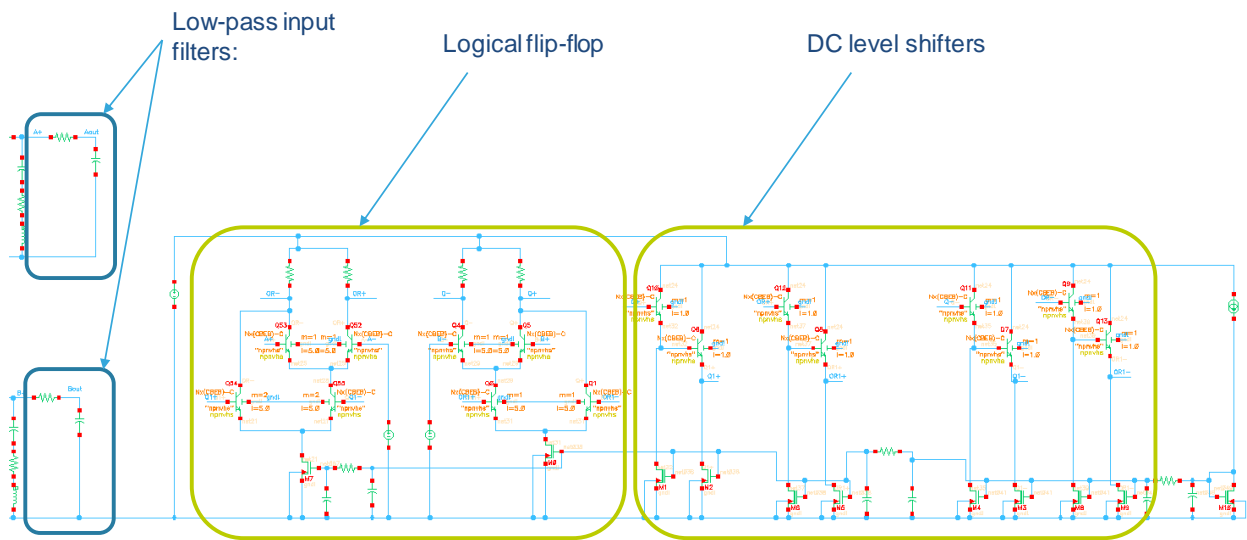


FIGURE 5.40: Design of the latch circuit

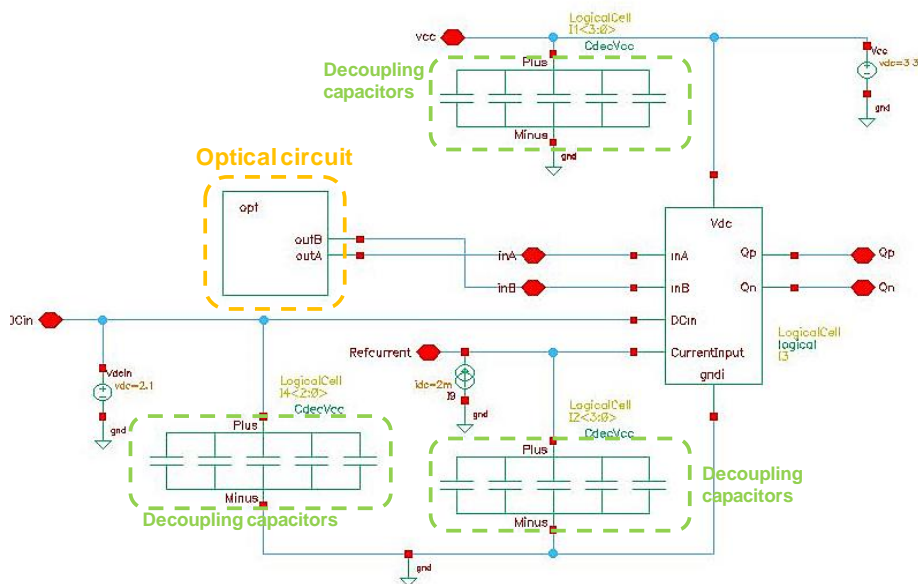
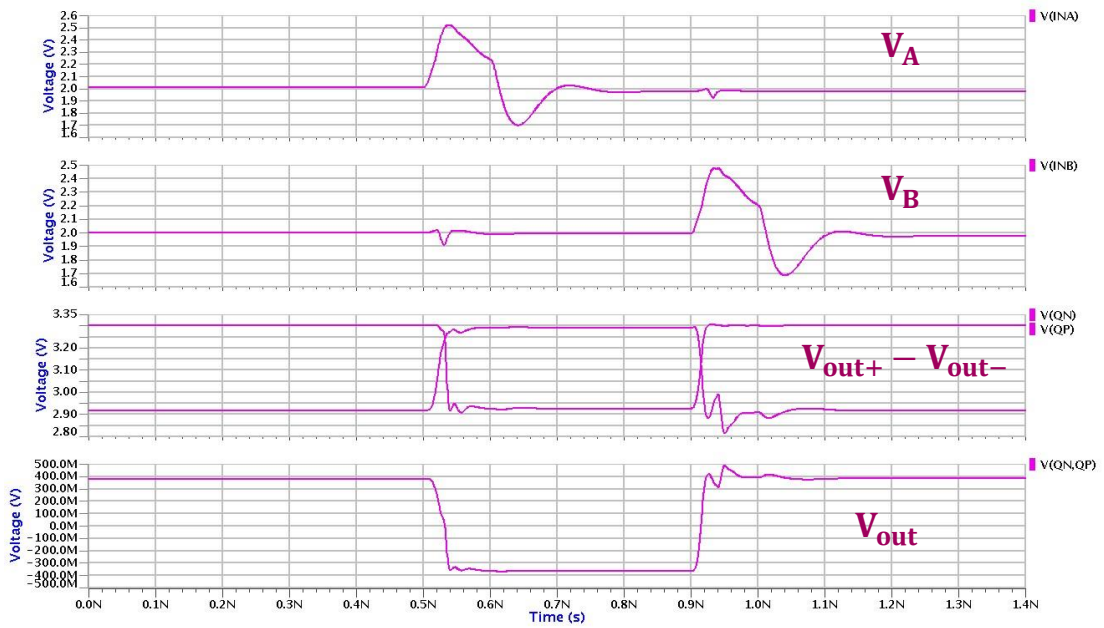
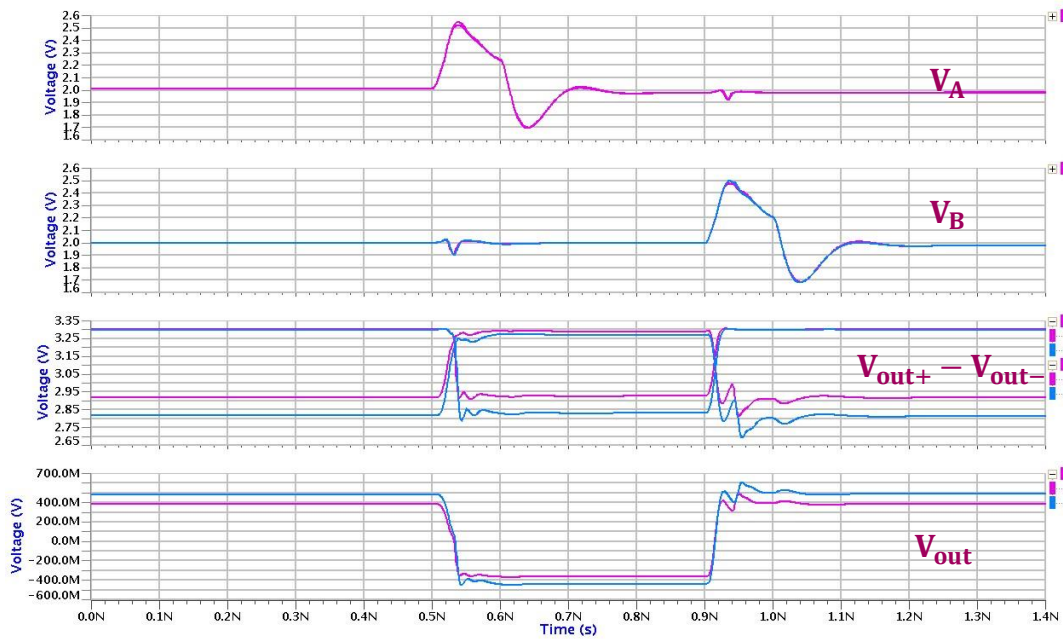


FIGURE 5.41: Logical circuit test bench

$$T_{out} = T_{pulse} + T_{delay} \tag{5.64}$$



(A) Logical circuit output signals at T=27°C



(B) Logical circuit output signals versus different operation temperature values

FIGURE 5.42: Plots of the logical circuit output signals versus temperature

The latch operation is based on the following equation:

$$Q_{n+1} = A + \bar{B}.Q_n \tag{5.65}$$

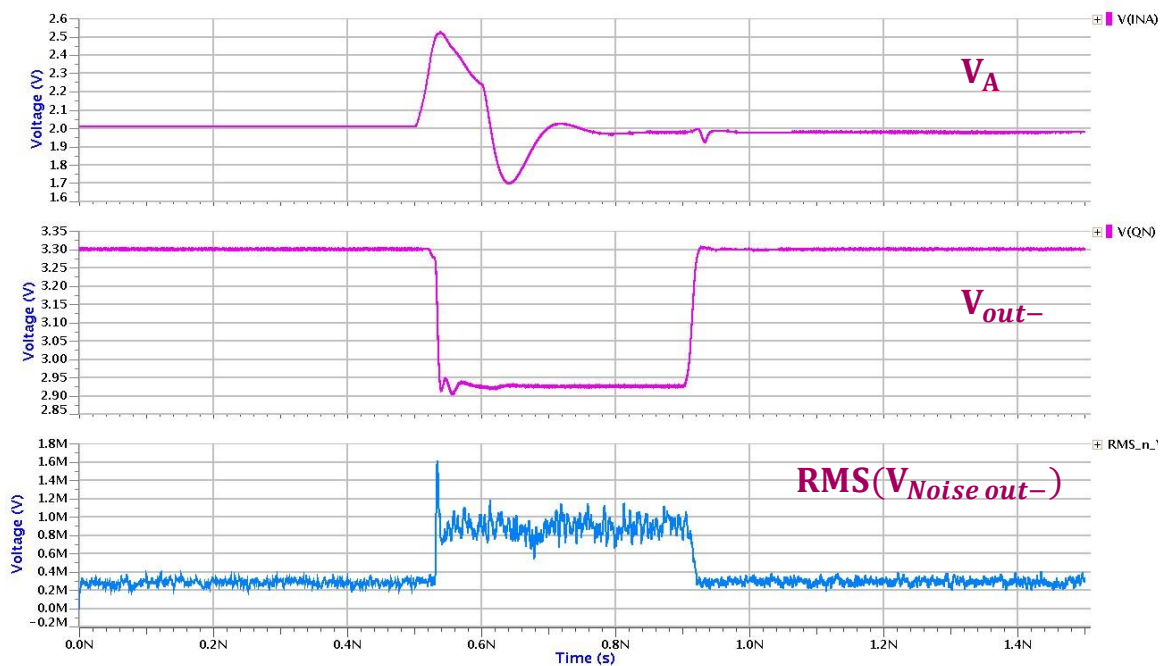
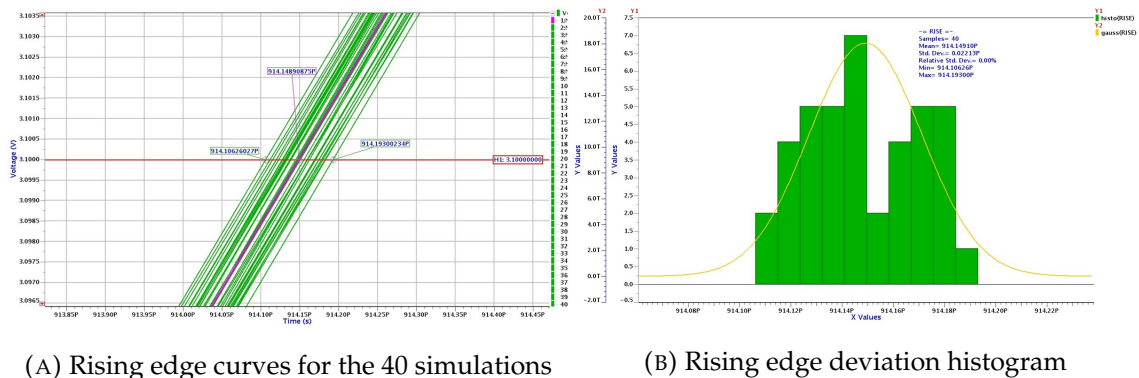


FIGURE 5.43: Noise simulation on double clock output signal over 40 simulations



(A) Rising edge curves for the 40 simulations

(B) Rising edge deviation histogram

FIGURE 5.44: Plots of double clock rising edge curves for the 40 simulations

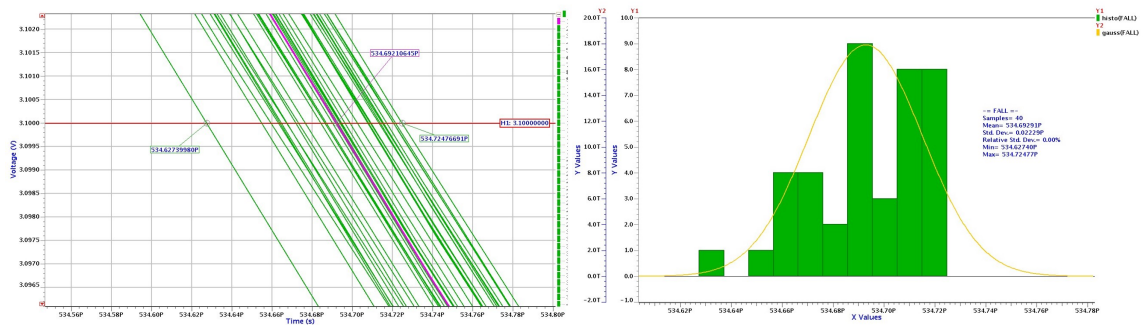
Where Q_i is the logical state at the output of the latch and A the first electrical pulse and B the second one.

The circuit that we use is depicted in fig.5.40.

As we can see on the design, we used here again the low pass filters because we have the same wire bonding problem.

The circuit simulation test bench is presented in fig.5.41.

In this simulation bench, we have represented all the decoupling capacitors that we added to the circuit after it was layouted.



(A) Falling edge curves for the 40 simulations (B) Falling edge time deviation histogram

FIGURE 5.45: Plots of double clock falling edge curves for the 40 simulations

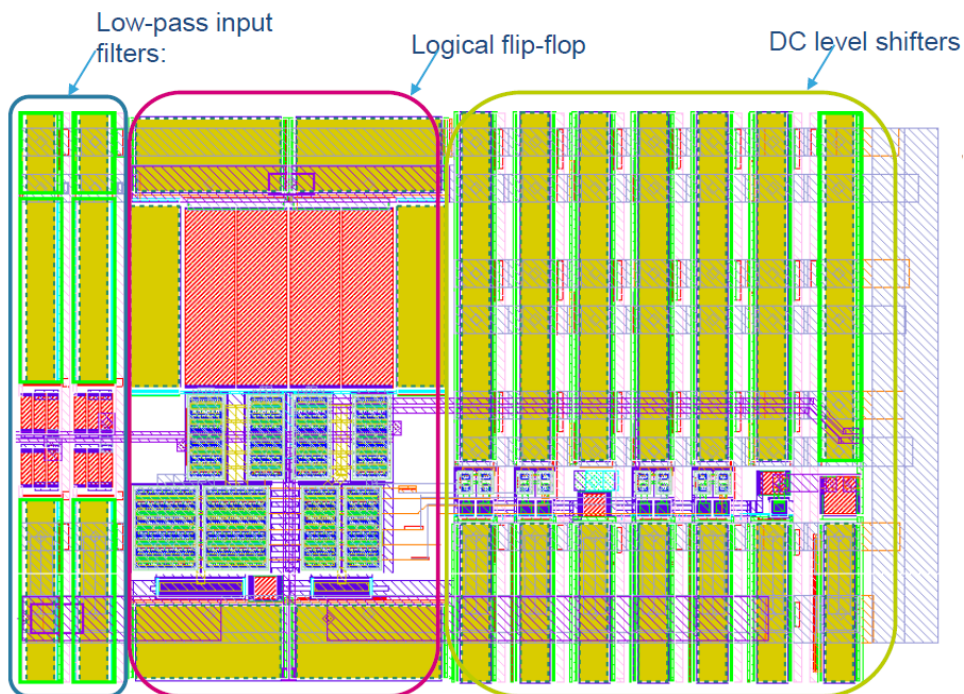


FIGURE 5.46: Layout of the logical circuit of the double photonic clock

The final clock signal is a 800mV peak to peak signal, which is in agreement with the ECL logic voltage levels (mainly 300mV). In fig.5.42a, we have presented the different signals of the clock, namely the two single clocks signals: V_A and V_B , and the output signal of the logical cell: V_{out} .

The rising and falling edges here are about 10ps long.

We have also run simulations with two different temperature values: 27°C and 125°C.

We can see that the output curves change with the temperature variations: the pulse height is slightly smaller. However, the rise and fall edges do not seem to be very impacted by the temperature changes which is beneficial to our case study.

In order to have a jitter equivalent value, we have plotted the 40 simulations resulting output signals and superposed them in order to evaluate the rising and falling edges deviation in time (fig.5.44).

The rising and falling edges jitter is determined by measuring the discrepancy of the time at which each one of the simulation curves crosses the decision taking voltage. These values are then analysed through the histogram and the average value is representative of the jitter induced.

As we can see in fig.5.44b, the average value of the rising edge jitter is approximately 22fs. It is worth saying that this value takes into consideration the initial jitter of the optical clock because we have used a jittery pulses source in order to model the optical pulses.

We have also represented the falling edge curves and histogram in fig.5.45. We can see that the falling edge jitter is 22fs as well.

The final layout of the circuit is depicted in fig.5.46. We simulated the full circuit using transient noise simulation in Cadence and optimized the logical circuit up to the point where the output total jitter (including the 11fs rms jitter of the optical signal) is equal to 22fs rms, which is still lower than the best low jitter of fully electrical clocks.

5.4 Conclusion

In this chapter, we have explained the design of the electrical circuits presented in the previous chapter. We started with the basic sampler circuit. For the latter, we have explained in details the method that we have used in order to design the input buffer circuit. This was meant to walk the reader through the design approach that we have used throughout the thesis.

The obtained design was simulated and we could see that it matched the constraints. Then, we presented briefly the design of the single clock generation block.

As explained before, the basic sampler circuit, in our case, can work with the use of the input buffer and the single clock circuit combined.

This setting is the closest to the first aim of the thesis since it allows to directly sample the signal using the germanium photo-conductor.

However, we saw that this configuration exhibits a total jitter of less than 50fs for an initial 11fs jitter at the laser. Although this remains smaller than the best literature electrical clocks, it is not very optimized in our case.

We could aim for better performance if the clock generation circuit was more optimized though.

We then presented the design details of the double clock circuit which exhibits a total jitter of 22fs on rise and fall edges. This circuit is then very promising for our case study and can be used in conjunction with a basic sampler circuit since the high light power that is injected during a laser pulse is high enough to feed the clock and the sampling circuit.

The only problem with the double clock is the area that it needs which is mainly due to the optical delay lines.

In conclusion, we can see that, according to simulation, the designed circuits cover the initial aim of the thesis which is to perform an opto-electrical sampling with very low jitter performance (less than 50fs).

Chapter 6

Conclusion and perspectives

The aim of this thesis was to study the feasibility of a an ultra-low jitter sampler clocked by a pulsed laser and based on a integrated germanium photo-conductor.

The first step that we have taken was to properly characterize the germanium photo-detectors that we were going to use. In order to do so, we have designed a first set of basic germanium photo-conductor schemes that were mainly inspired from the already existing germanium photo-diodes in STMicroelectronics PIC25G technology.

This first set of devices, namely generationA, was then tested under a DC bias and continuous wave light. The measurement results showed an ohmic behavior of the photo-conductors and very low R_{off} on R_{on} ratios, along with a dependency of the resistance on voltage above the carriers velocity saturation field.

We have then designed a second set of devices that was aimed at properly characterizing the R_{off} of the photo-conductors and optimizing the R_{off} on R_{on} ratio. Therefore, generationB included sweeps over length and width of the regular rectangular devices with different light injection patterns(single light injection and double light injection and a study of the tapers). This second generation also included devices with a novel geometry, an exponentially decaying width, that is believed to optimize the R_{off} on R_{on} ratio. This novel geometry was patented.

We conducted the following measurements on generationB devices:

- DC source with no light measurements:the aim of these measurements is as said to conclude on the R_{off} dependency on the devices dimensions.
- DC source with continuous wave light measurements: the aim of these measurements is to measure the R_{on} values and to quantify the R_{off} on R_{on} ratio for different geometries and for different light injection patterns. These measurements would also validate the exponential photo-conductors operation.
- DC source with pulsed light: these measurements would give us an idea about the photo-conductor behavior as a sampler. The main pieces of information to collect being the peak R_{on} value and the decay time.

The first set of measurements that we have conducted showed that the value of R_{off} for the different devices, and in their ohmic behavior voltage range, does not scale linearly with the dimensions. We have then found a tendency that would predict the way $R_{off, square}$ changes with the dimensions of the device. The model that we found is a phenomenological one and was not obtained through physical equations although it may have a physical interpretation.

In all the cases, we believe that the variations of $R_{off, square}$ can be explained and probably better modeled if the whole fabrication process was taken into consideration.

The second set of measurements confirmed the theoretical study on the exponential shapes with optimized R_{off} on R_{on} ratios for equivalent starting R_{off} . These measurements helped us find a model to characterize the R_{on} dependency on power, voltage and device dimension. It also showed that R_{off} on R_{on} ratios of all the devices are not high enough to fulfill the constraints of a sampler.

The third set of measurements was harvested through a study of the cables response in order to understand the time dynamic of the system. This analysis, even if it did not provide exact values of the decay time and peak R_{on} value, but it helped us understand how the system time response is affected by all its components and prevented us from jumping to quick conclusions regarding the fall time of the output signal.

With these measurements in hand and the limitations they shed light on, namely long decay times and low R_{off} on R_{on} ratios, we have decided to try an alternative solution in order to increase the R_{off} on R_{on} ratio: try counter-doping the germanium. Indeed, the low values of R_{off} that we have are mainly due to the presence of a residual p-type doping that results from the process flow. Therefore, we used an n-type counter-doping and obtained an increase on the R_{off} values of 6 compared to the original ones. Moreover, the R_{on} values stayed the same which means that the crystal quality was not damaged by the counter-doping. This also means that we have optimized the R_{off} on R_{on} ratio by a factor of 6 (for the best counter-doping formula), which still is not good enough for the targeted application.

One must note that the counter-doping formulas that we used were set by STMicroelectronics based on existing formulas, therefore a more thorough study on the formula to use could yield better results.

Given what was said, we decided to use a workaround solution in order to circumvent the problems that we have. Indeed, we decided to re-sample the signal, that is first sampled by a basic photo-conductor based sampler, through a regular ADC. This will allow to work around the low R_{off} value constraint. Moreover, the ADC circuit will be driven by an optical clock, i.e. a circuit made of germanium photo-conductors and electrical drivers that transforms the optical pulses of the laser into electrical pulses with low jitter values.

This circuit was implemented in generationC mask. The electrical circuits were designed as to provide the lowest possible contribution in jitter, in our case, according to noise simulations, we would have a total jitter performance of 46fs which is better than literature electrical clocks. Optimizing furthermore the electrical drivers design would certainly allow a better performance.

This new electrical clock structure was also patented.

Based on the latter idea, we have designed other variations of the photonic clocks with different features. Indeed, the original single photonic clock signal needed to be handled afterwards by a pulse-shaping stage in order to properly fit the forthcoming ADC specifications. The addition of the pulse-shaping stage adds inevitably noise to the clock signal which increases the total jitter of the clock signal.

The new photonic clock circuit is based on two single photonic clocks, and uses optical delay lines to set the pulse width. This design allows us to have clock signal right at the output of the optical chip which means that the jitter performance is better than the first circuit. The second variation of the photonic clock circuit involves two double photonic clocks and a latch circuit. This last variation is very versatile since it makes it possible to create pulses with very long widths which is not possible with the first double clock. These last two circuits were also patented.

We have implemented all the upsaid photonic circuits in generationC mask and the compatible electrical drivers in a BiCMOS mask. The circuits were fabricated and cut for pcb assembly. The pcb board was also designed and manufactured by STMicroelectronics. However, the assembly was not done yet. This is why we could not provide the final measurements of the full sampling system.

The simulations and theoretical work that has been conducted in this thesis proves the feasibility of an ultra-low jitter sampler clocked by a pulsed laser and based on a integrated germanium photo-conductor (all the circuits show a jitter of less than 50fs). However, as was explained above, the basic sampler circuit is not the way to go in this case since it does not fulfill the sampler requirements. Therefore, the following should be harvested furthermore:

- Counter-doping study in order to find the best formula to increase R_{off} on R_{on} ratio.
- A more thorough study of the exponential shape designs: more precisely a study on a way to circumvent the design rules that led to the staircase geometries.
- An optimization of the electrical drivers in order to further reduce their noise contribution.

Appendix A

Photodetectors description

In this appendix, we will give a thorough description of the different photodetector devices that were realized throughout this thesis.

There are three generations of devices: GenerationA, GenerationB and GenerationC.

A.1 GenerationA

In this first generation, the photodetectors were designed to receive a $1310nm$ illumination.

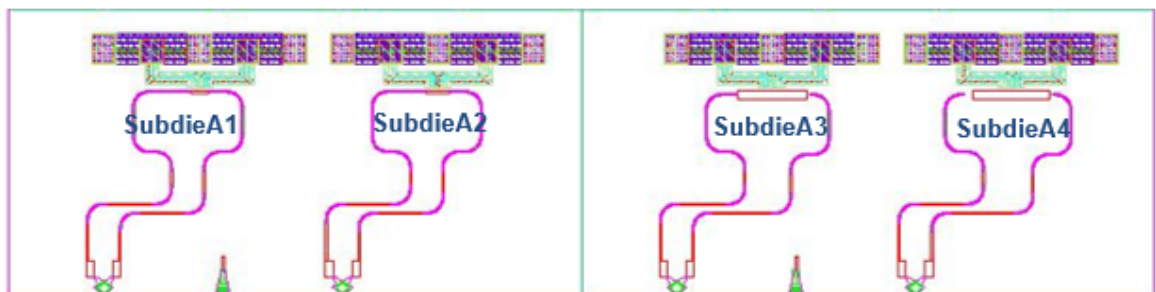


FIGURE A.1: Overview of the first generation subdies

This first generation is made up of four structures: two basic structures (subdieA1 and subdieA3) and two slightly elaborate ones (subdieA2 and subdieA4).

The basic structures, i.e subdieA1 and subdieA3, are $p - \pi - p$ Germanium waveguide integrated photoconductors.

We use a double optical power injection pattern in order to homogenize the photogeneration of charge carriers throughout the devices. The light is actually injected through the chip by a 2D grating coupler then it is injected by the two sides of the photoconductor through waveguides and tapers.

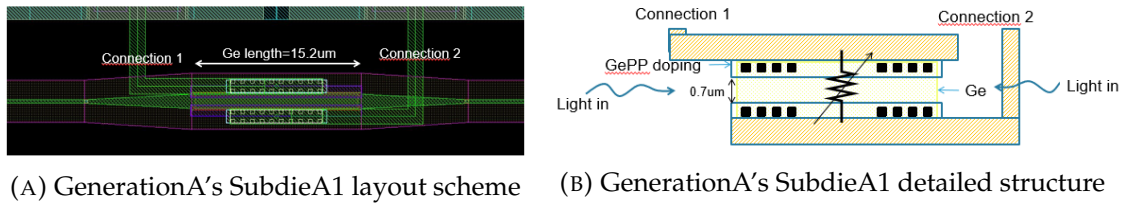


FIGURE A.2: Plots of Germanium band diagram and absorption coefficient

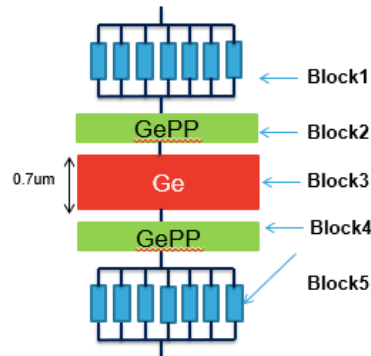


FIGURE A.3: Build-up of subdie A1 and subdie A3

Each one of these two structures is basically built as follows (see Fig.A.3) :

- **Block1 & Block5** : the contact between the metal layer and the P doped Germanium is made up through 8 vias (16 for subdie A2 and subdie A4). Each via is a 50 Ohm resistance.
- **Block2 & Block4** P-doped Germanium layer; this layer prevents from having a Schottky contact between Germanium and the metal layer, the drawn width being 360nm. The diffusion length is unknown, it is nonetheless supposed to be neglectable since Boron does not diffuse much. The square resistance of this layer is 47 Ohm / square.
- **Block3** Intrinsic Germanium with an average square resistance of : 60 kOhm/square (between 50kOhm and 70kOhm)

The structures' dimensions are:

- Subdie A1: $w = 0.7\mu m$ and $L = 15.2\mu m$
- Subdie A3: $w = 0.7\mu m$ and $L = 30.4\mu m$

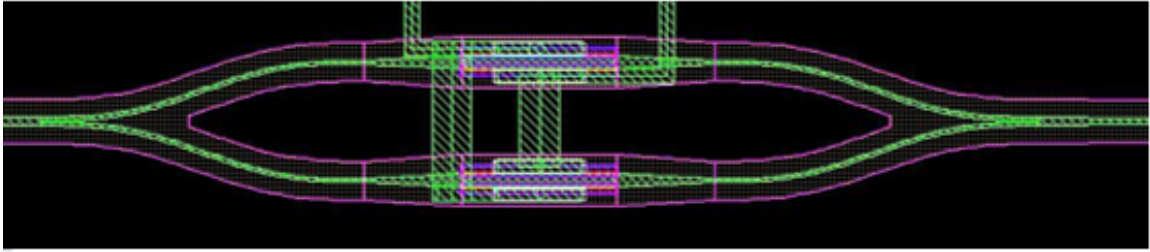


FIGURE A.4: SubdieA2 and SubdieA4 layout scheme

The second set of structures (see Fig.A.4)are made of two basic structures connected in parallel (electrically). SubdieA2 is made up of two SubdieA1 in parallel and SubdieA4 is made up of two SubdieA3;

Light is injected into these structures through a 2D grating coupler, single mode $1310nm$ waveguides then through a Y branch and finally through tapers.

A.2 GenerationB

In this second generation, the photodetectors were designed to receive a $1550nm$ illumination.

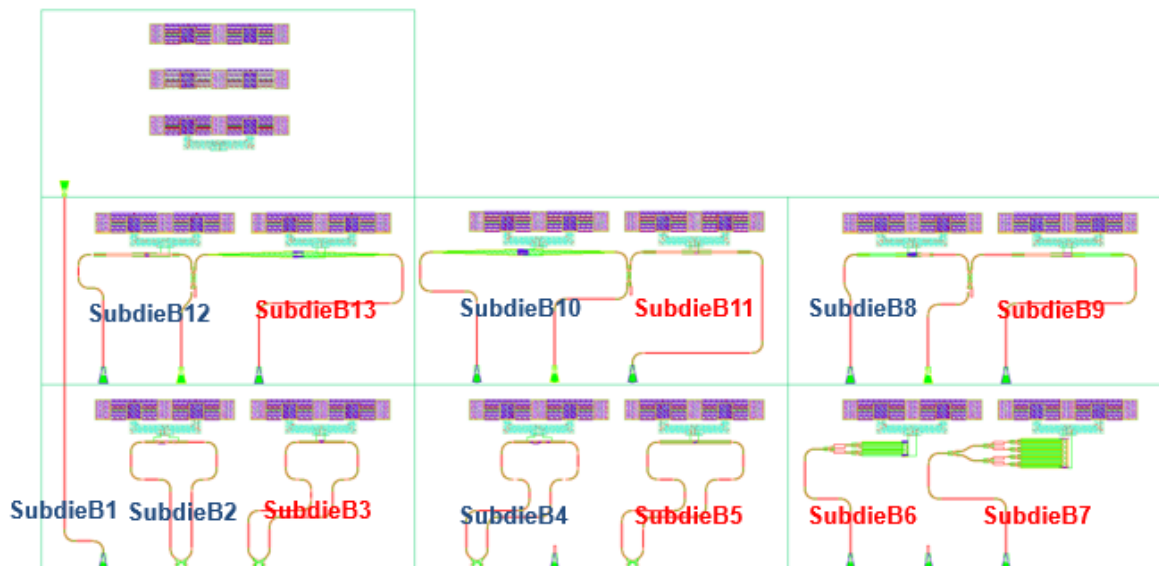


FIGURE A.5: Overview of the second generation subdies

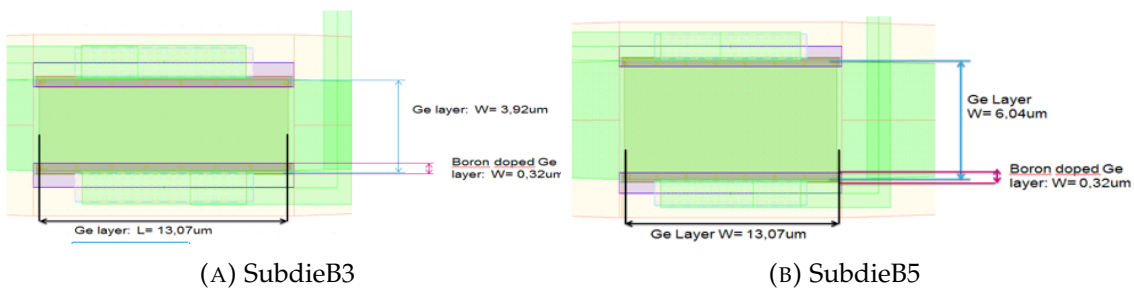
This second generation is made up of eleven photoconducting structures:

- The red structures are basic rectangular photoconducting devices like SubdieA1 and SubdieA3.

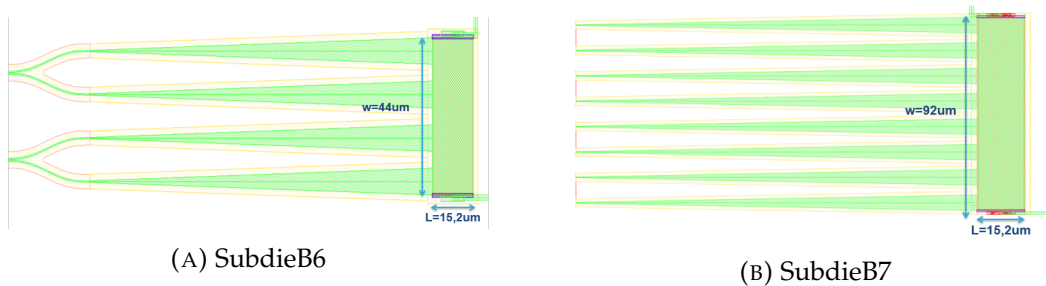
- The blue structures are more elaborate structures and will be described in details below.

Note that the first structure, SubdieB1 is a coupling test structure.

- SubdieB3: $w = 3.92\mu m$ and $L = 13.07\mu m$ and double injection
- SubdieB5: $w = 6.4\mu m$ and $L = 13.07\mu m$ and double injection



- SubdieB6: $w = 44\mu m$ and $L = 15.2\mu m$ and single injection
- SubdieB7: $w = 92\mu m$ and $L = 15.2\mu m$ and single injection



- SubdieB9: $w = 8.3\mu m$ and $L = 13.07\mu m$ and single injection
- SubdieB11: $w = 8.3\mu m$ and $L = 15\mu m$ and single injection
- SubdieB13: $w = 14.3\mu m$ and $L = 30.015\mu m$ and single injection

Note that the widths given here are the widths of Germanium, which include the doped regions. However, in the resistance estimations for example, only the intrinsic Germanium widths are taken into consideration.

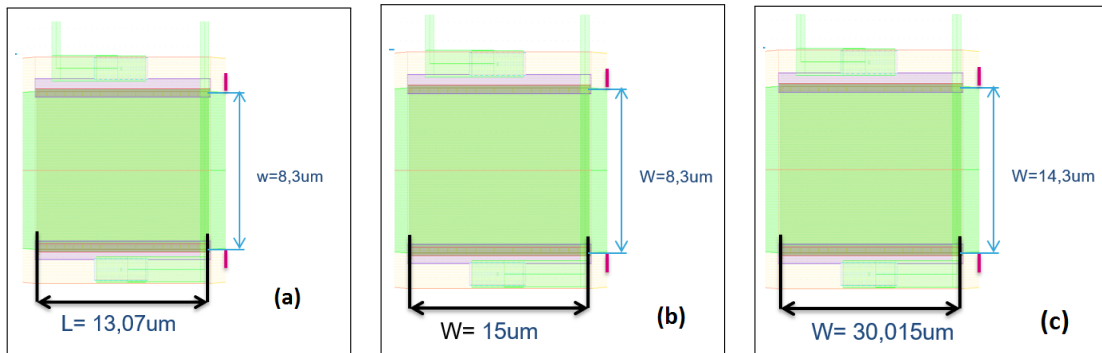
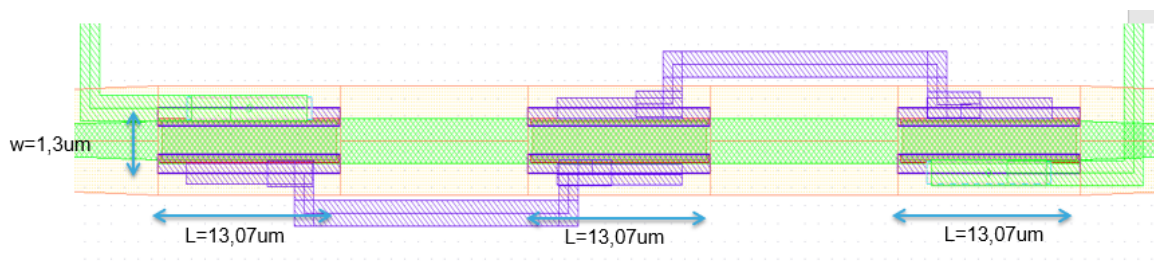


FIGURE A.8: Layout scheme of respectively: subdieB9, subdieB11 and subdieB13

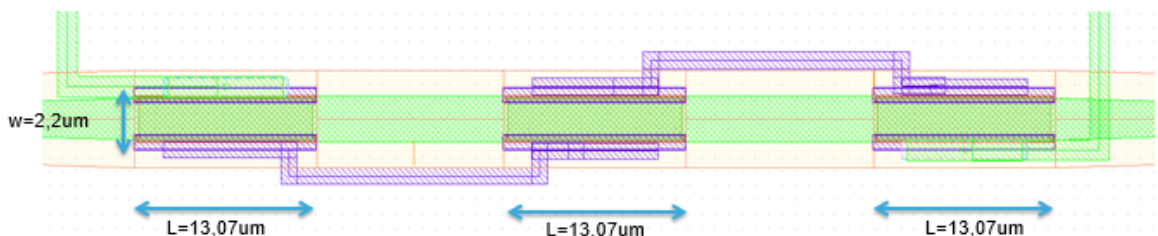
The second batch of structures are as follows:

SubdieB2 and subdieB4 are made of three photoconductors connected in series electrically and in parallel optically, i.e the light is injected in a double injection fashion from both sides and the leftover energy from the two lateral photoconductors is injected into the middle photoconductor.

- SubdieB2: $w = 1.3\mu m$ and $L = 13.07\mu m$
- SubdieB4: $w = 2.2\mu m$ and $L = 15\mu m$



(A) SubdieB2



(B) SubdieB4

SubdieB8, subdieB10 and subdieB12 are exponentially shaped.

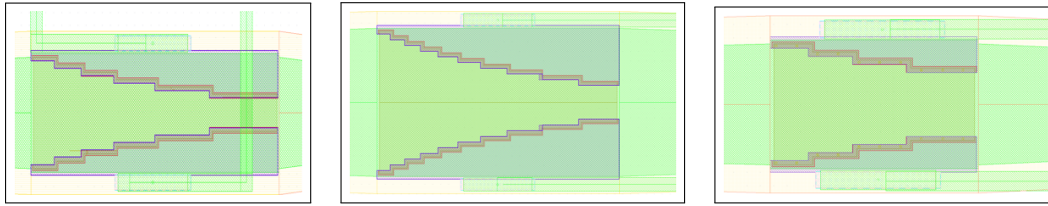


FIGURE A.10: Layout scheme of respectively: subdieB8, subdieB10 and subdieB12

In order to give the dimensions of the exponential subdies, we deconstruct the latter into many rectangular sub-blocks as depicted for subdieB8 in Fig.A.11.

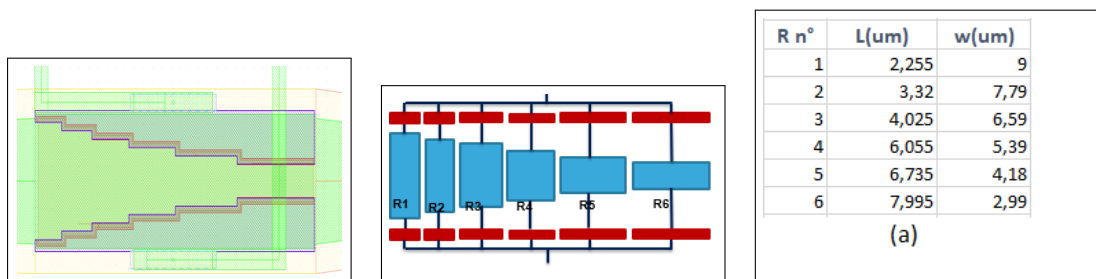


FIGURE A.11: (a): SubdieB8, (b): deconstruction of subdieB8 (c): subdieB8 dimensions

R n°	L(um)	w(um)
1	1,675	15
2	18,9	13,8
3	2,005	12,28
4	2,21	11,4
5	2,505	10,2
6	2,87	9
7	3,34	7,8
8	4,03	6,6
9	5,015	5,4
10	4,53	4,2

(A) SubdieB10 dimensions

R n°	L(um)	w(um)
1	2,859	9
2	3,325	7,73
3	4,025	6,59
4	4,785	5,39

(B) SubdieB12 dimensions

FIGURE A.12: SubdieB10 and SubdieB12 dimensions

The dimensions of the deconstructed exponential photoconductors are given in Fig.A.12.

A.3 GenerationC

In this third generation, the photodetectors were designed to receive a $1550nm$ illumination.

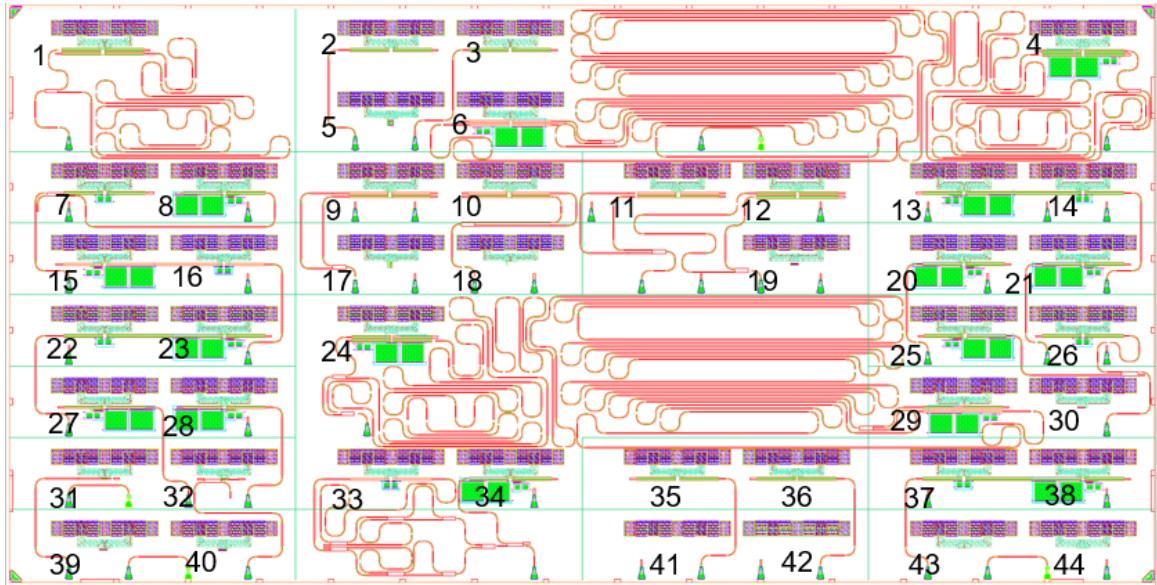


FIGURE A.13: GenerationC overview

In this appendix, only a small portion of the devices of GenerationC will be presented, the other ones will be presented along the concerned chapters (chapter3).

The first set of photoconducting structures are basic rectangular photoconductors with a single side injection (see Fig.A.14) of light or no injection of light at all for some(see Fig.A.15). The latter were designed mainly to characterize the dark current response of the devices.

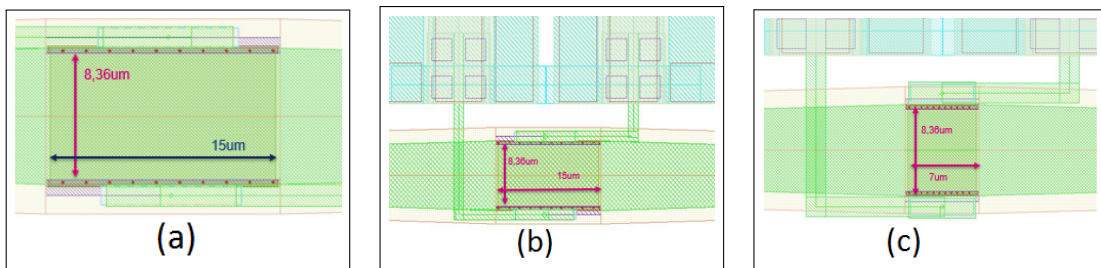


FIGURE A.14: Single injection subdiodes: (a): SubdieC2, (b): SubdieC35
(c): SubdieC36

The dimensions of these subdiodes are as follows:

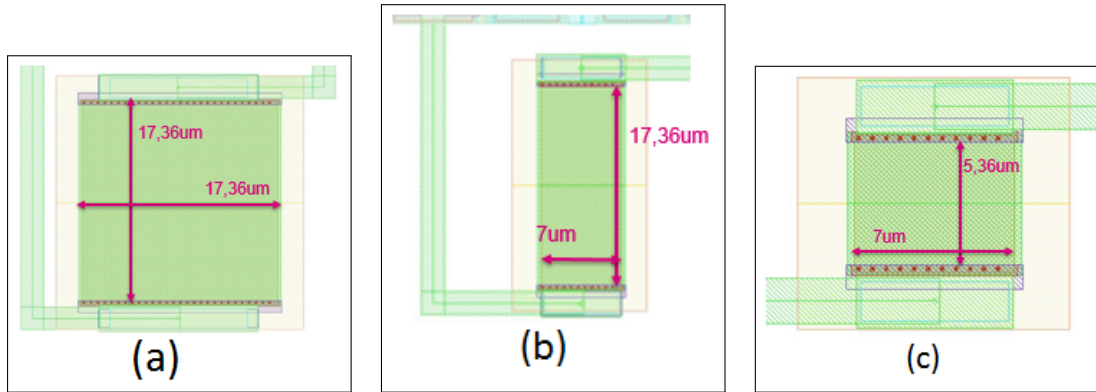


FIGURE A.15: No light injection subdies:(a): SubdieC5, (b): SubdieC17 (c): SubdieC18

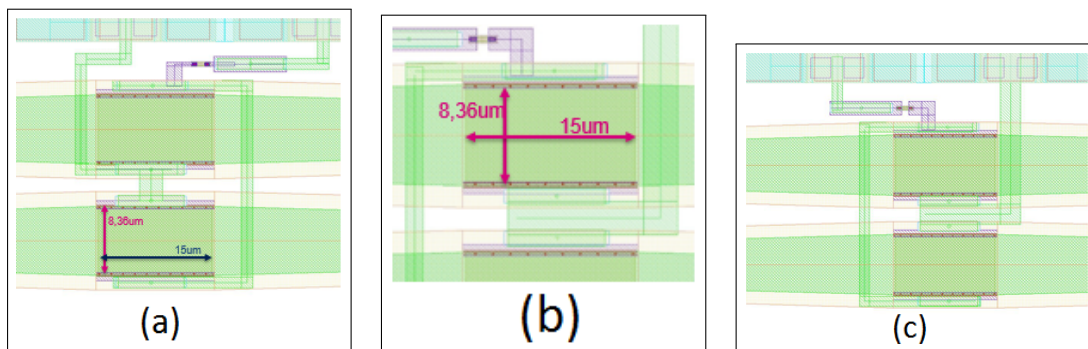


FIGURE A.16: Double injection subdies:(a): SubdieC1, (b): SubdieC12 (c): SubdieC19

- SubdieC1: two photoconductors in parallel (electrically) $w = 8,36\mu m$ and $L = 15\mu m$.
- SubdieC2: single injection of light $w = 8,36\mu m$ and $L = 15\mu m$.
- SubdieC5: no injection of light (electrically) $w = 17,36\mu m$ and $L = 17,36\mu m$.
- SubdieC12: two photoconductors in parallel (electrically) $w = 8,36\mu m$ and $L = 15\mu m$.
- SubdieC17: no injection of light $w = 17,36\mu m$ and $L = 7\mu m$.
- SubdieC18: no injection of light $w = 5,36\mu m$ and $L = 7\mu m$.
- SubdieC19: two photoconductors in parallel (electrically) $w = 8,36\mu m$ and $L = 15\mu m$.

- SubdieC35: single injection of light $w = 8,36\mu m$ and $L = 15\mu m$.
- SubdieC36: single injection of light $w = 8,36\mu m$ and $L = 7\mu m$.

Appendix B

Cables model

B.1 Cables model

In order to model the cables, we used a transmission line classic model, since the cable is one. The model is made up of several identical unit cells as the one depicted in fig. B.1. We set the number of cells to 1300; this number is chosen

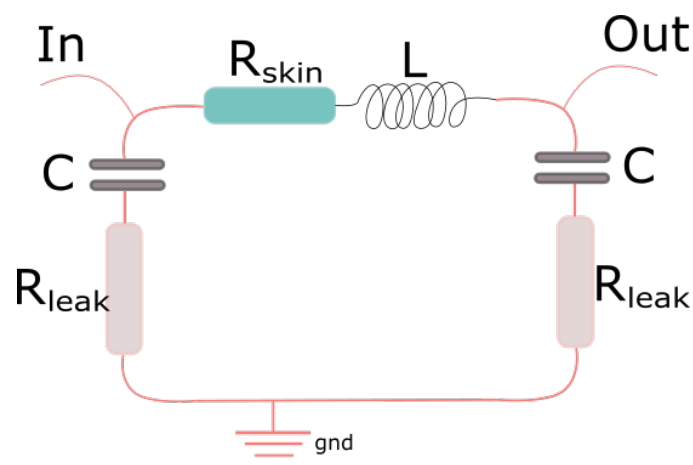


FIGURE B.1

so to keep the cell length very small compared to the ongoing phenomena and in the same time to keep the processing as time efficient as possible.

In order to understand what each parameter in the unit cell model stands for and how it is set, we may first start by presenting a regular cable composition. In fig. B.2, we can see that the cable is made out of an inner conductor surrounded by a dielectric layer. The latter is covered by a screen made of silver plated copper then covered by an outer sheath.

The unit cell that we consider, fig. 3.34, includes:

- **Two capacitors:**

They stand for the capacitance made out of the conductor, the dielectric

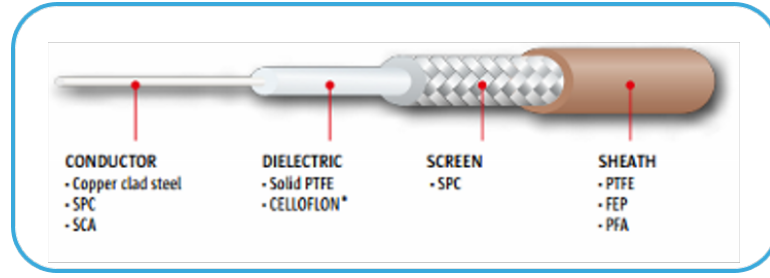


FIGURE B.2: Cable layers composition

and the screen.

The value of these capacitors in the model is set as follows:

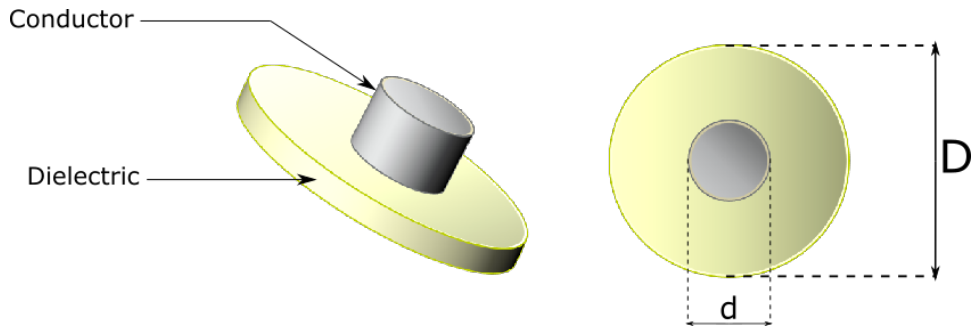


FIGURE B.3: Cable layers composition

If we consider a 1mm long cable segment as in fig.B.3, and we apply Gauss theorem to this segment, we find:

$$\frac{Q_{in}}{\varepsilon} = \oint E \cdot dS = E \cdot \pi D \quad (B.1)$$

Where D is the diameter of the dielectric.

And since the voltage V applied on this cable piece can be expressed as:

$$V = \int_d^D E \cdot dx \quad (B.2)$$

We have:

$$V = \int_d^D \frac{Q_{in}}{\varepsilon \pi D} \cdot dx \quad (B.3)$$

Where: ε is the dielectric constant of the dielectric of the cable. Therefore:

$$V = \frac{Q_{in}}{\varepsilon \pi D} \ln \frac{D}{d} \quad (B.4)$$

Now since:

$$V = \frac{Q_{in}}{\varepsilon\pi D} \ln \frac{D}{d} \quad (\text{B.5})$$

Since:

$$CV = Q_{in} \quad (\text{B.6})$$

$$C = \frac{\pi\varepsilon}{\ln \frac{D}{d}} \quad (\text{B.7})$$

This is how we evaluated the capacitance of a 1mm segment of the cable at:

$$C = 95 \text{ fF/mm}$$

Therefore, each capacitor in the unit cell circuit has a capacitance of: 47.5 fF.

- **Skin resistor:**

This resistor models the skin effect in the conductor and in the screen. Indeed, at high frequencies, the current tends to flow mainly close to the surface, which means that the section through which the current flows decreases with frequency [133]. This effect is quantified by a parameter: skin depth δ , where:

$$J(x) = J(0) \exp -x\delta \quad (\text{B.8})$$

$J(x)$ being the current density at a distance x from the surface.

Therefore, the value of the resistor that models this effect is:

$$R(f) = R(0) \times \sqrt{1 + \frac{f}{f_c}} \quad (\text{B.9})$$

Where: f_c is the frequency at which the skin depth is equal to:

$$\delta(f_c) = \frac{S}{P} \quad (\text{B.10})$$

S being the section of the conductor and P its perimeter.

And we have:

$$f_c = \frac{4}{\pi\mu\gamma r_0^2} \quad (\text{B.11})$$

Where:

μ : the permeability of the conductor
 γ : the conductivity of the conductor
 r_0 : the radius of the conductor

And:

$$R_0 = \frac{l}{\pi\gamma r_0^2} \quad (\text{B.12})$$

Where l is the length of the cable segment.

Since the skin effect occurs for the conductor and the screen, we sum um their skin resistance contributions as follows:

$$R_{skin}(f) = \frac{4l}{\pi\gamma d^2} \sqrt{1 + \frac{f\pi\mu\gamma d^2}{16}} + \frac{4l}{\pi\gamma(D-d)^2} \sqrt{1 + \frac{f\pi\mu\gamma(D-d)^2}{16}} \quad (\text{B.13})$$

With the used cabel parameters, we have:

$$R_{skin}(f) = 6.044 \times 10^{-3} \sqrt{1 + \frac{f}{76.9 \times 10^3}} + 6.6135 \times 10^{-3} \sqrt{1 + \frac{f}{83.53 \times 10^3}} \quad (\text{B.14})$$

- **An inductor:**

In the unit cell model the inductance stands for the tendency of both the conductor and the screen to oppose sudden changes in current. And we have:

$$Z = \sqrt{\frac{L}{C}} \quad (\text{B.15})$$

Where:

Z : the characteristic impedance of the cable
 L : the inductance of a 1mm segment of the cable
 C : the capacitance of a 1mm segment of the cable

Since the cables that we use are 50Ω cables: $L = 247.5pH/mm$.

- **Leakage resistors:**

These resistors model the leakage current through the dielectric and are calculated as regular resistors. In our case, they are about 200Ω each.

Appendix C

PCB making

The PCB board stackup is made of three copper layers, separated by two substrates. The upper copper layer is used to make the RF connections, the intermediate layer is for ground and the third layer (bottom) is for DC connections.

This distribution of layers is made so that RF signals do not interfere with DC paths.

We chose an "RO4350" 0.254mm^1 as a substrate to the RF layer (top layer), and a Nelco 4000-13 SI 0.508mm^2 as a substrate to the DC layer.

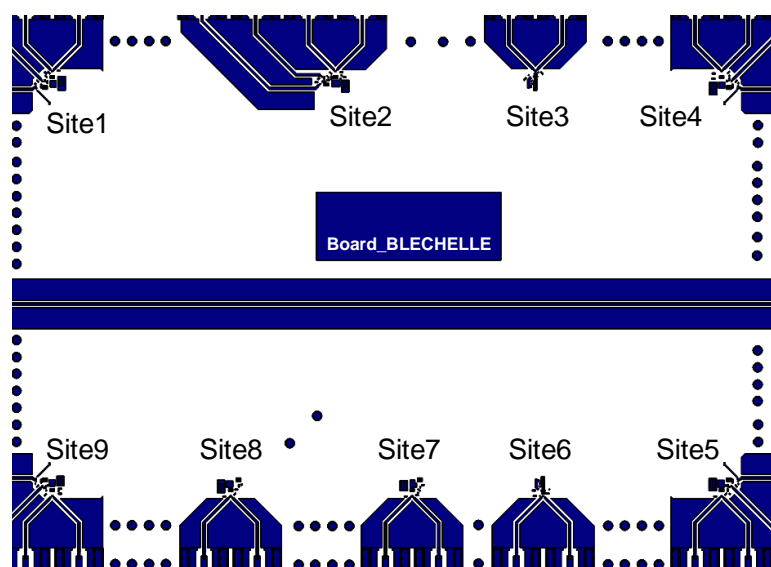


FIGURE C.1: PCB top layer with the nine sites depicted

The final assembly is composed of nine sites in total, each of which is an assembly, via wire bonding, of an electrical chip and a photonic one. The nine sites are depicted in fig.C.1 where the top layer (RF connections) is illustrated

¹See: <http://www.rogerscorp.com/acs/products/55/RO4350B-Laminates.aspx>

²See: <https://parkelectro.com/products/n4000-13-13-si/>

NB : The writings in fig.C.1 are not part of the top layer, they were just added to showcase the sites positions on the PCB board.

The PCB design was made with ADS. As said earlier, the board is made of three copper layers (see fig.C.2):

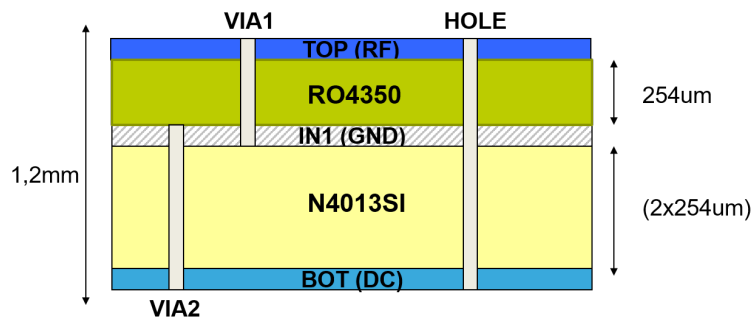


FIGURE C.2: PCB layers stack-up detailed

- Top layer: $35\mu m$ high.
- Intermediate layer, called IN1: $18\mu m$ high copper.
- Bottom layer: $35\mu m$ high.

and here are the different layers used:

The three copper layers are illustrated below:

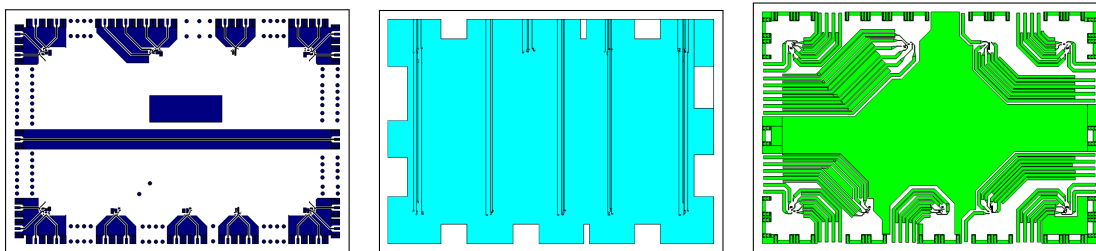


FIGURE C.3: Plots of the three copper layers in the PCB stack-up respectively: top layer, intermediate layer and bottom layer

As can be seen in fig.C.2, the connections between the different metal layers are made through vias. Via1 layer is the via layer between the top layer and the intermediate layer, Via2 connects the intermediate layer to the bottom layer and finally, Hole is the via layer that connects the top and bottom layers. These different layers layout is depicted in fig.C.4

We used two insulating solder resist masks and two silkscreen layers, a top and a bottom one. The latter are used to print text or shapes on the top and bottom layers and are depicted in fig.C.10.

The final board is $1,2\mu m$ high with the following dimensions: $216,8 * 150,5\text{mm}$.

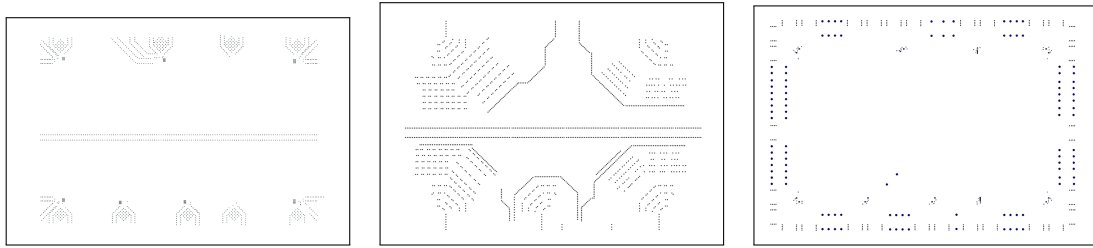


FIGURE C.4: Plots of the three metal interconnection layers in the PCB stack-up respectively: Via1 layer, Via2 layer and Hole layer

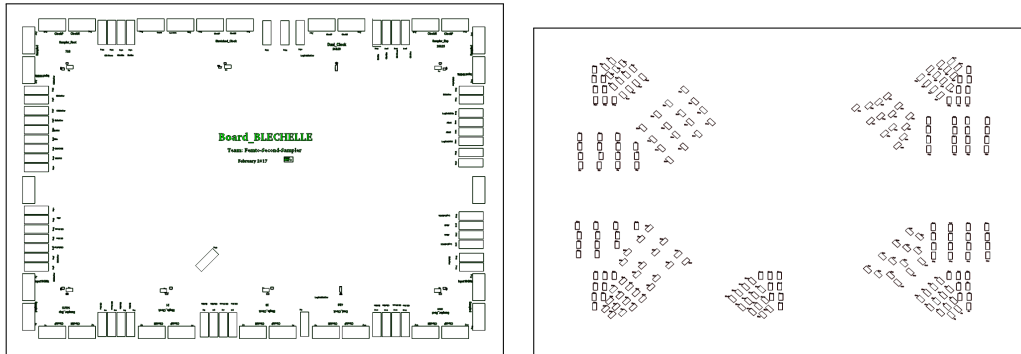
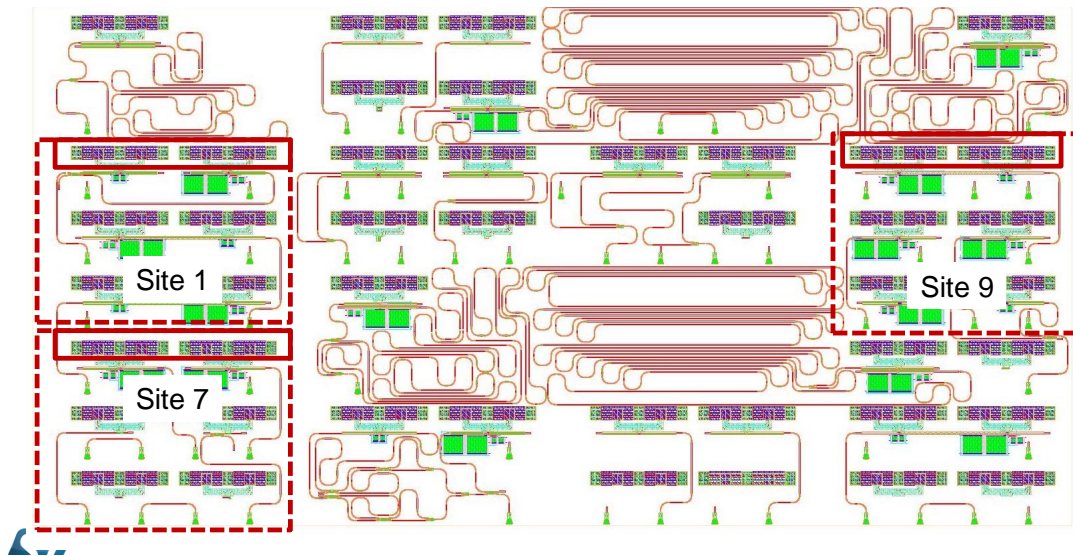
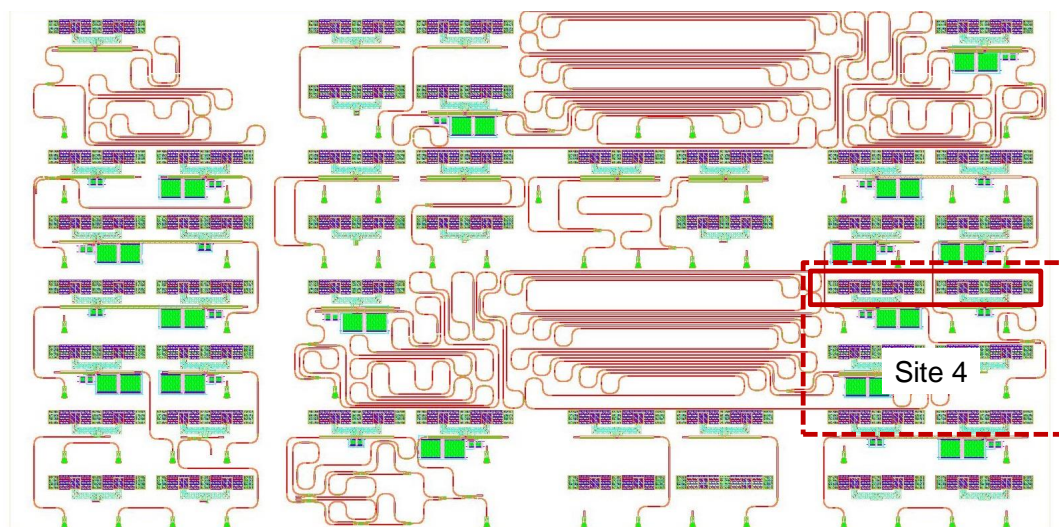
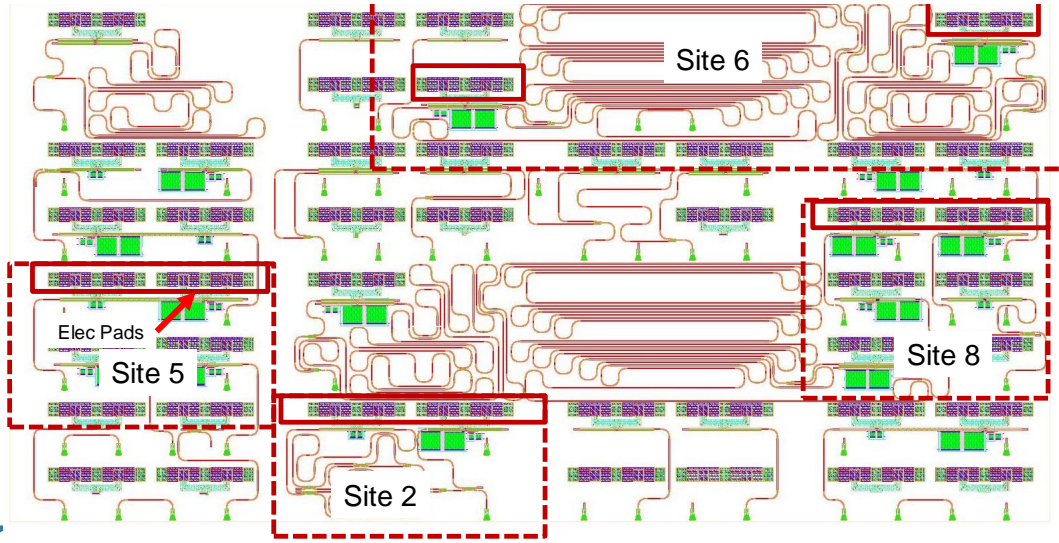


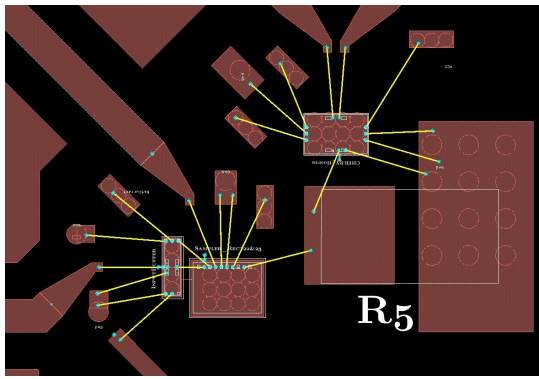
FIGURE C.5: Plots of the two silkscreen layers in the PCB stack-up respectively: silkscreen1 layer (Top layer print), silkscreen2 layer (Bottom layer print)



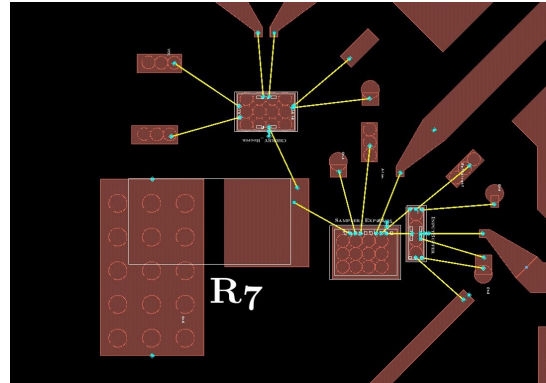
The nine sites, as explained above, are combinations of electrical and photonic ones, they are arranged as follows:

The design of these sites and their position were optimized so that the RF lines are as short as possible. A special attention was drawn to the transmission lines and the wire bonds of the differential signals to make them as symmetrical as possible.

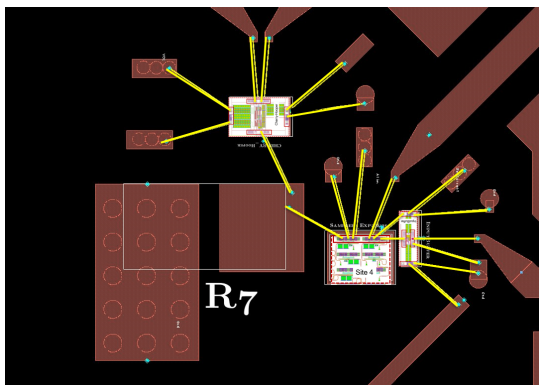




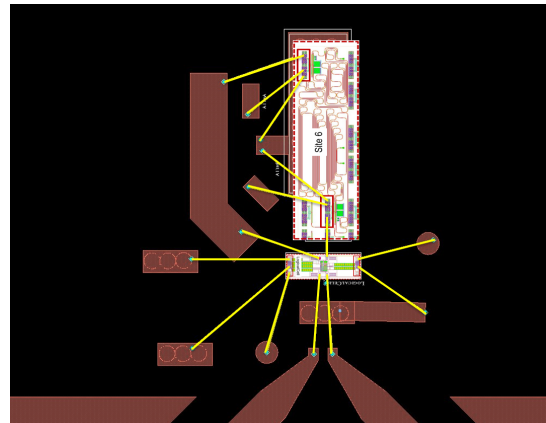
(A) Site 1



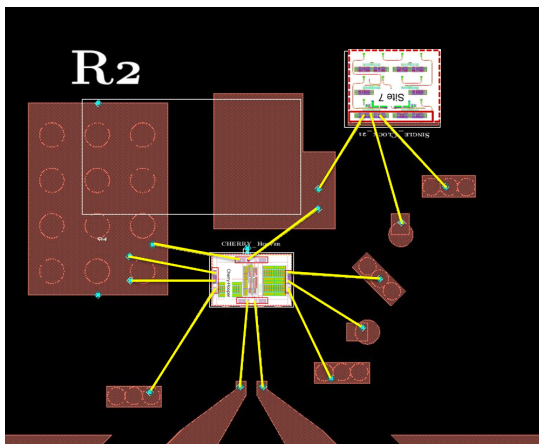
(B) Site 3



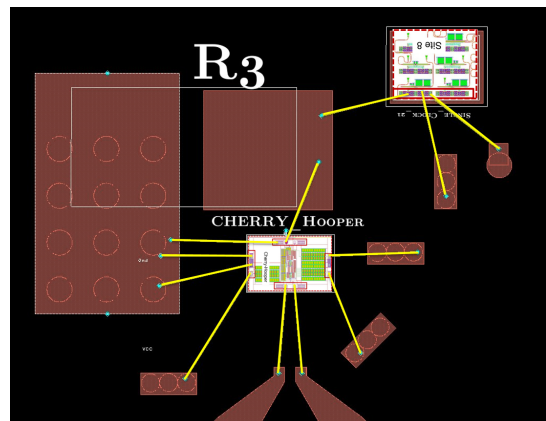
(A) Site 4



(B) Site 6



(A) Site 7



(B) Site 8

NB : We discarded site2 because of an error on the layout (wrong chip orientation) that we discovered after filing the pcb layout to fabrication.

The different sites are depicted below:

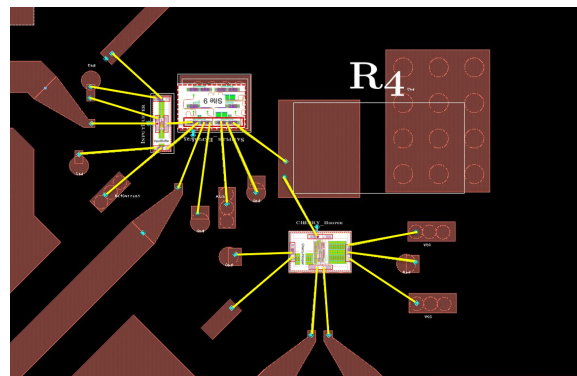


FIGURE C.9: Site 9

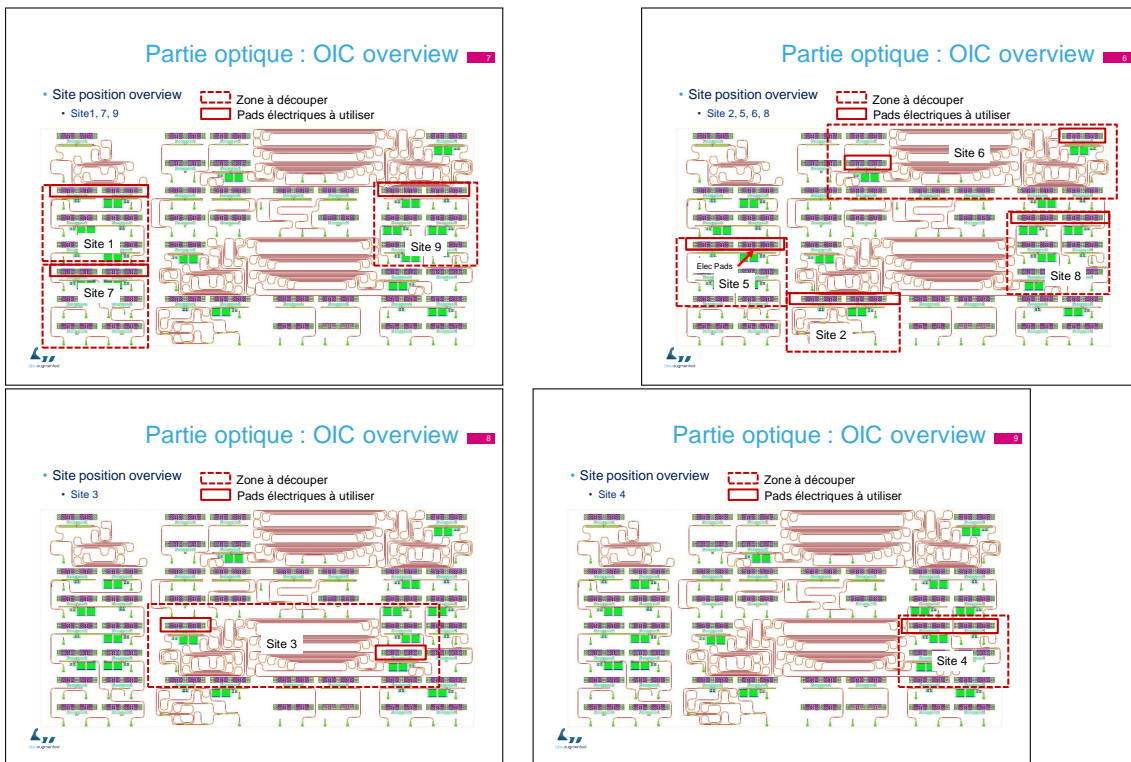


FIGURE C.10: Plots of the three metal interconnection layers in the PCB stack-up respectively: Via1 layer, Via2 layer and Hole layer

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