Integration of Single Photon Avalanche Diodes in Fully Depleted Silicon-on-Insulator Technology

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Contents

List of Acronyms

ABA	Approximate Breakdown Analysis
AQC	Active Quenching Circuit
AQRC	Active Quenching and Recharge Circuit
ATP	Avalanche Triggering Probability
BOX	Buried Oxide
BSI	Back Side Illumination
B2B	Band To Band Tunneling
C28FDSOI	CMOS 28 nm FDSOI technology platform from STMicroelectronics
CIS	CMOS Image Sensor
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
DCR	Dark Count Rate
DIBL	Drain-Induced Barrier Lowering
DNW	Deep N-well
DRC	Design Rule Checking
EG	Extended Gate
EHP	Electron Hole Pair
FBB	Forward Body Biasing
FDSOI	Fully Depleted Silicon On Insulator
FF	Fill Factor
FLIM	Fluorescence Lifetime Imaging Microscopy
FOM	Figure Of Merit
FSI	Front Side Illumination
FWHM	Full-Width at Half Maximum
LIDAR	Light Imaging Detection and Ranging
LVT	Low V_{th}
MOSFET	Metal Oxide Semiconductor Field Effect Transistor

NIR Near Infra Red
NOSO No SOI
NW N-Well
NUV Near Ultra Violet
PCB Printed Circuit Board
PDE Photon Detection Efficiency
PDK Physical Design Kit
PDP Photon Detection Probability
PEB Premature Edge Breakdown
PID Plasma Induced Damage
PQAR Passive Quench Active Recharge
PQC Passive Quenching Circuit
PQRC Passive Quenching and Recharge Circuit
PW P-well
RBB Reverse Body Biasing
RVT Regular V_{th}
SACM Separate Absorption Charge and Multiplication
SCR Space Charge Region
SDE Synopsys Sentaurus™ Structure Editor
SOI Silicon On Insulator
SOTA State of the Art
SPAD Single Photon Avalanche Diode
SRH Shockley-Read-Hall Generation-Recombination
STI Shallow Trench Isolation
TAT Trap Assisted Tunneling
TCAD Technology Computer-Aided design
TCSPC Time Correlated Single Photon Counting
TOF Time-Of-Flight
TSV Through-Silicon Vias
UTBB Ultra Thin BOX and Body

Introduction

With the advances of technologies, many new applications and markets were developed. Smartphones are omnipresent in today's life. Cameras' resolution and functionalities are improved every day. One of the promising features is 3D imaging and ranging. Those implementations could enable big advances such as autonomous cars, thanks to smart driving.

For 3D imaging applications, not only regular imagers are needed, but also detectors that are able to measure the distance of the surrounding objects. Those systems can employ Time-Of-Flight (TOF) measurements, which is an advanced technique where a luminous source emits a signal, that is then reflected by a target. For a direct TOF approach, the reflected beam impinges then the sensor and the time elapsed between those two events is measured so the distance can be inferred from half the measured time (by considering the round trip of photons).

Single Photon Avalanche Diodes (SPAD) have shown to be great devices for implementing this receiver. Those devices are PN junctions operating at high reverse voltage bias, and have the great advantage of presenting very high sensitivity and response time, which are mandatory for this kind of application, where diffused reflected beams are common and not so certain of reaching the sensor in real situations. Another benefit of using SPAD is the fact that simple associated electronics easily provide a digital signal at its output, without the need of integrating fast and complex Analog to Digital Converters.

The objective of this PhD thesis is to study the implementation of SPAD devices in an advanced CMOS FDSOI technology. This work was conducted as a part of the ARC6 research program 2016 (no 16 - 005689 - 01), funded by the Auvergne Rhone Alpes region, France, in a partnership between two French laboratories: Institut des Nanotechnologies de Lyon (INL) and Laboratoire Hubert Curien (LHC), under the supervision of Prof. Francis Calmon and Prof. Raphaël Clerc. We also had the technical support of both CEA-LETI and STMicroelectronics. The manuscript is organized as follows:

In Chapter 1 the physics of SPAD devices is reviewed, along with its main Figures of Merit (FOM), i.e., Dark Count Rate (DCR), Afterpulsing, Photon Detection Probability (PDP), Time Jitter, Fill Factor and Crosstalk. The current State of the Art of those devices is also presented, along with the main implementations of SPAD in SOI technologies and some of the main applications.

In Chapter 2, a quick review of CMOS SOI technologies is done, focusing on the advanced 28 nm FDSOI technology and its great advantages for low-power applications. Then, the design of different variants of Single Photon Avalanche Diode (SPAD) cells in such a technology is presented, along with its main constraints and the proposed

solutions for such a challenging implementation. An innovative indirect avalanche sensing cell is also proposed in FDSOI.

In Chapter 3, the proposed SPAD is simulated by means of TCAD tools, by analyzing the main models available to describe the physical phenomena involved in the correct operation of Geiger mode avalanche diodes. Also, post-processing is implemented for estimating SPAD parameters, such as Dark Count Rate (DCR) and Photon Detection Probability (PDP). An analytical simplification for calculating Avalanche Triggering Probability (ATP) is proposed too.

In Chapter 4, the electric characterization of the fabricated devices is presented. Results such as the I-V curves, Dark Count Rate and Electroluminescense response for the different designed cells are discussed. Also, the proposed indirect avalanche sensing circuit is validated experimentally.

Finally, some general conclusions are made about design, simulation, modeling and electrical characterization of the proposed SPAD architecture. A comparison with the already existing SPAD devices is made, with the perspectives for future work.

Chapter 1

SPAD and Applications

In this chapter, the working principle of Single Photon Avalanche Diode (SPAD) is presented, along with its main Figure Of Merit (FOM), such as Dark Count Rate, Photon Detection Probability, Time Jitter and Fill Factor. Some discussions about SPAD applications for future technologies are also outlined. At the end of the chapter, the State of the Art for SPAD implemented in CMOS is presented, with a special focus on Silicon On Insulator (SOI) technologies. Finally, the thesis objectives and the content of the following chapters are detailed.

1.1 Geiger Mode Operation of Silicon Photodetectors

Single Photon Avalanche Diode (SPAD) are PN junctions working in reverse bias, above breakdown voltage, in the so-called Geiger mode region. Due to the high voltage bias, the electric field in Space Charge Region (SCR) is also high, which configures a very unstable state of the junction, because a single free carrier present in SCR (or multiplication region) would be quickly accelerated by the electric field and could easily cause a series of impact ionization processes, resulting in a self-sustained avalanche, and a consequent electric current.

This free carrier can be the result of a photogeneration process directly in SCR once a photon is absorbed in that zone, or even a diffusion process from near layers, when the carrier is generated there. In this case, the device is said to be a Single Photon Avalanche Diode (SPAD), because a single impinging photon is able to generate a macroscopic current signal, easily detectable [1].

SPAD devices can be used for detecting not only photons but also charged particles, because energy is released in their trajectory, possibly causing a succession of Electron Hole Pair (EHP) generation [2]–[5]. SPAD avalanches can also be observed in dark condition, due to undesired carriers in SCR. Those are quantified by the so-called Dark Count Rate (DCR) parameter (as explained in Section 1.2.1)

The basic operating mode of SPAD is illustrated in Fig. 1.1. The device is initially biased above breakdown voltage (point 1). Once the avalanche event is triggered (point 2), a high current circulates through the device and may damage it, if not properly extinguished (quenched) [1], [6], [7]. For avoiding that, quenching circuits (such as a simple series resistor) are used to reduce the reverse voltage across the diode and, consequently, the avalanche current (point 3). Once it happens, the voltage across the

diode is increased back to its initial value (point 1), and the SPAD is ready for another detection.

In order for an avalanche to occur, two conditions are necessary: 1) The electric field must be high enough to provide a non-null avalanche triggering probability; 2) at least one free carrier must exist in SCR. When the junction is biased above breakdown voltage, but no free carrier is available, the SPAD is ready for a detection (Fig. 1.1 (point 1)). When a photon is absorbed in SCR, an electron-hole pair is generated and the carriers are accelerated, starting an impact ionization process: avalanche is triggered and the current rapidly increases. The associated quenching circuit then reacts and starts decreasing the bias voltage across the diode in (point 2). Once the avalanche current is extinguished (point 3), the voltage is increased again through recharge circuit, making the SPAD ready for another detection.

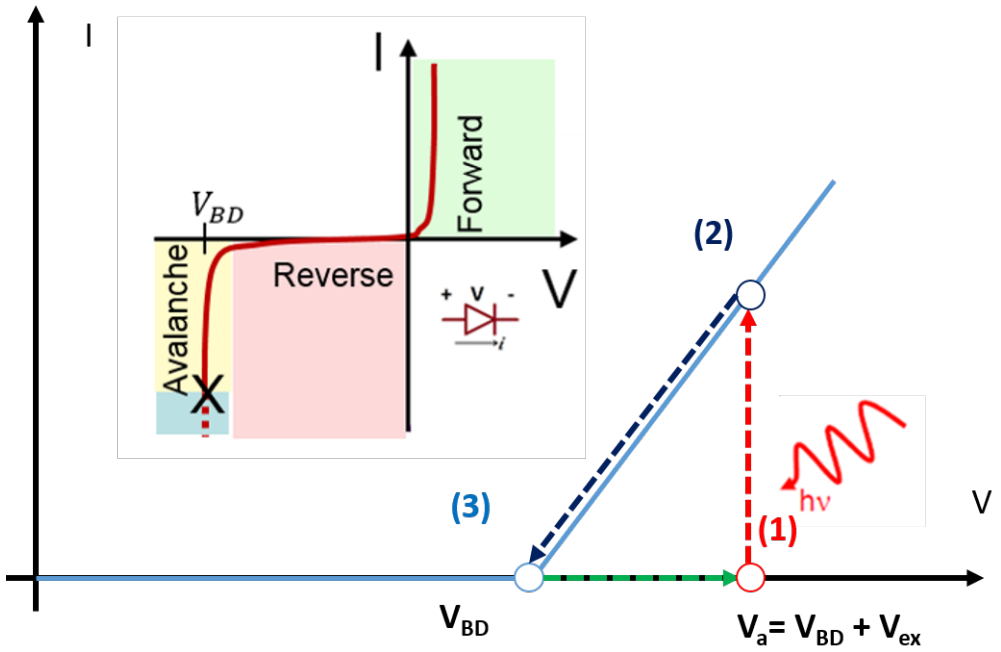

Figure 1.1: *Working principle of Geiger mode operating photodiodes (Adapted from: [7]).*

It should be noted that, unlike regular silicon photodetectors working at lower reverse bias, the SPAD detector by itself can only detect the occurrence of a physical event, not being able to quantify the amount of photons that actually impinged the SCR, since the amplitude in output signal does not depend on the amount of photogenerated carriers.

Unlike in linear mode operation, where the magnitude of the electric field is only enough to provide ionization caused by electrons, the photodiode operating in Geiger mode has an electric field high enough for both carriers to provoke such a phenomenon, and can be described as in Eq. 1.1, known as ionization integral [6].

$$1 \leq \int_0^W \alpha_e \exp\left(\int_x^W (\alpha_h - \alpha_e)\, dx'\right) dx \tag{1.1}$$

In Eq. 1.1, W is the width of the SCR, α_e and α_h are respectively the ionization coefficients for electrons and holes.

1.2 Figures of Merit

In this section, the main Figures of Merit for SPAD are presented, as they serve as the parameters that characterize the performance of the devices and are later used for comparisons between SPAD implemented in different technologies.

1.2.1 Dark Count Rate

The Dark Count Rate (DCR) is the intrinsic noise of the device, and can be defined as the rate of spurious pulses, caused by events other than optical. In other words, the rate, in Hz or Hz/μm^2, that avalanches created by thermal generation, Band To Band Tunneling (B2B), or even from the release of trapped charges contribute to the DCR [1], [6].

This parameter is of high importance in SPAD performance, because the time interval between two consecutive dark events should be long enough to provide an efficient photodetection [8].

Several aspects can influence dark counting. The choice of the technology, for instance, has a tremendous impact in DCR, as doping levels and density of defects (in silicon, but also in silicon-oxide interface close to the SCR) have a direct influence in counting.

External operating conditions, such as temperature and excess voltage, can also modify values of DCR considerably. Basically, as the temperature increases, the Shockley-Read-Hall Generation-Recombination (SRH) generation-recombination rate and the DCR increase too. In addition, if the excess voltage is enhanced, the triggering probability increases and consequently, so does the DCR. The delay time between avalanche detection, quenching and recharge also affects the total DCR, through the afterpulsing phenomena (described in Section 1.2.2). Lastly, the dimensions and geometry of SPAD cells should also be taken into account in design phase, in order to reduce DCR, as will be explained in Chapter 2.

The physical generation process of EHP is the same for the reverse current in PN junctions [8] and their corresponding avalanche pulses are randomly distributed in time, being described by a Poisson process [9]. An example of measured DCR is presented in Fig. 1.2

1.2.2 Afterpulsing

Total DCR includes primary and secondary output pulses. Those latter are also known as afterpulsing and have their origin from the release of charges trapped in the deep levels of the junction. Those generation-recombination centers are localized energy states in the forbidden energy gap and exist due to the defects and impurities in the semiconductor, facilitating the transitions between valence and conduction bands, as shown in Fig. 1.3 [7], [9].

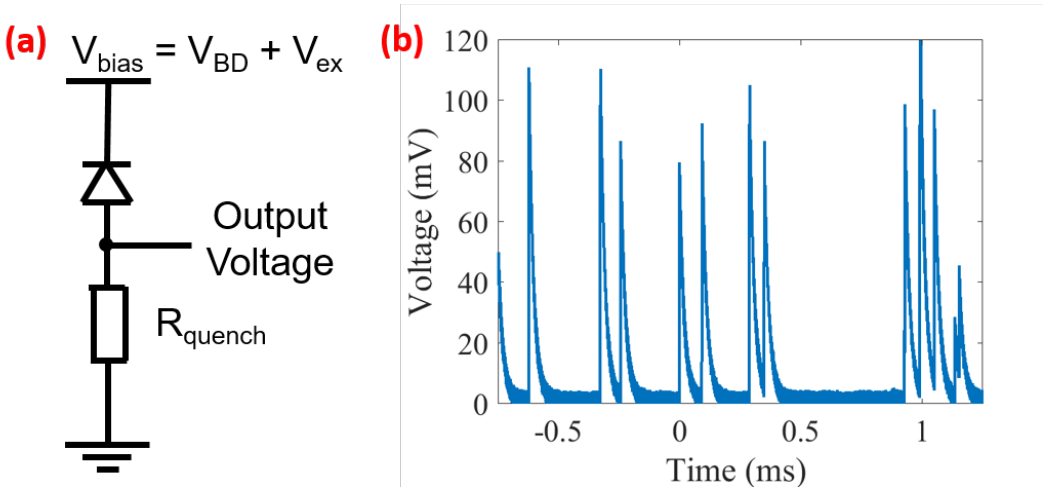

Figure 1.2: *(a) Schematic representation of the SPAD with its quenching resistor. (b) Measured output pulses for SPAD operated in dark conditions from [10]. The average of counts for a fixed time window corresponds to DCR.*

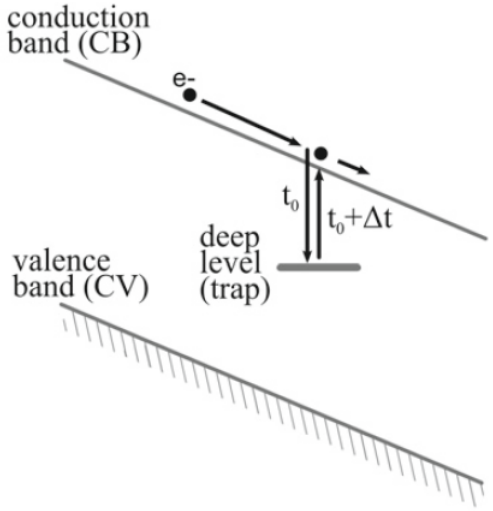

Figure 1.3: *Trapping and releasing mechanisms of charges in the deep levels, responsible for afterpulsing events. Adapted from [7].*

During avalanche events, carriers can be trapped in those deep levels, being subsequently released, generating another avalanche, correlated with the previous one. The shorter the SPAD recharge time, the more likely is the releasing that implies in afterpulsing. Current intensity, proportional to excess voltage, also increases afterpulsing probability [11]–[13].

1.2.3 Photon Detection Probability and Efficiency

Photon Detection Probability (PDP) can be defined as the probability of an absorbed photon to generate an output current pulse, due to a self-sustained avalanche. PDP

represents the sensitivity of the SPAD and is directly affected by electric field magnitude and distribution along the junction, depending, then, on the doping levels of the structure and on the applied voltage at the diode's terminals [6]. Physically, PDP is directly related to the photogeneration rate (quantum efficiency) and the avalanche triggering probability.

PDP is also a function of the impinging photon's wavelength, through the photon absorption coefficient of the material. There are SPAD implementations in different semiconductor materials for the near ultraviolet spectrum (300 - 400 nm) [14]–[17], the visible spectrum (400 - 800 nm) [18]–[30] and the Near Infra Red (NIR) (800 - 1550 nm) [14], [30]–[54].

In silicon technologies (our study), because of its bandgap, photodetection is limited to wavelengths below 1125 nm. Due to the shallow SCR in common Complementary Metal Oxide Semiconductor (CMOS) SPAD, they present poor PDP in Front Side Illumination (FSI) (below 5%) at suitable NIR wavelengths (840 or 930 nm) [6]. For applications in such range, Back Side Illumination (BSI) might be preferred [14], [49]–[54], often combining with 3D assembling at wafer level (see Section 1.4).

PDP can be adversely affected by three main factors [1]. The first one is reflectance of the layers that compose the stack of materials of the technology (often metals), or even the interface between two layers. This first factor can be attenuated by using antireflection top coating. The second factor that decreases PDP is the absorption of the photons at a depth other than the one of the junction's SCR (shallower or deeper), or at a position from which the photogenerated carriers cannot reach the multiplication region. The third reason is self-quenching, when avalanche is initiated, but is interrupted before causing a potential difference that could be detected. This effect can be minimized by guaranteeing that the electric field reaches a high enough value, which is why it is important to apply considerably high excess voltages to the SPAD detector.

Since the Avalanche Triggering Probability (ATP) increases with electric field, PDP also depends on that factor. The excess voltage V_{ex} is the main parameter that influence electric field magnitude and ATP is expected to initially increase linearly with V_{ex}, and then to saturate at high V_{ex}. PDP follow, then, the same tendency [7], [55], [56].

For measuring PDP, a common procedure is to illuminate the SPAD device with a monochromatic light source in an integration sphere coupled with a reference diode. By varying the wavelength of the incident beam, curves such as the one presented in Fig. 1.4 can be obtained [14].

In order to improve PDP at NIR wavelengths, some research papers employ the so-called Separate Absorption Charge and Multiplication (SACM) structures [59], [60]. As shown in Fig. 1.5, those devices make use of absorption layers made of materials other than silicon, such as InGaAs or Ge, better adapted for NIR detection. Once the photon is absorbed, the resultant photogenerated carriers, due to electric field, are accelerated through the charge layer into the multiplication layer, made of silicon. In that region, ATP values are better for detection.

For characterizing the effective sensitivity of SPADs, the Photon Detection Efficiency (PDE) is often used, being defined as the product of the PDP by the Fill Factor (FF) [6].

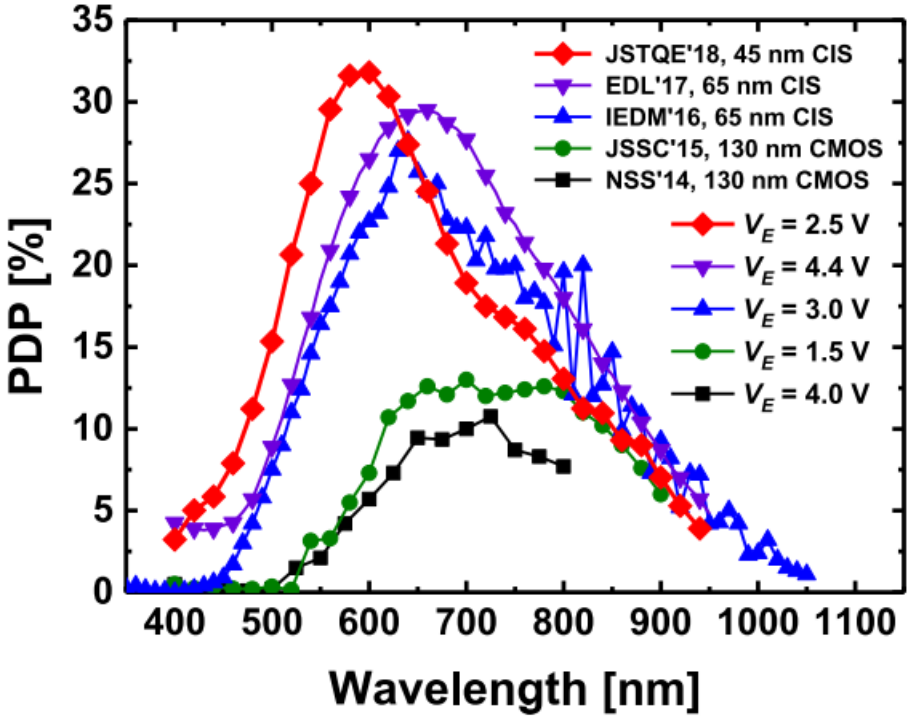

Figure 1.4: *Measured PDP as a function of wavelength for several SPADs. (Original figure from [14]). References in the figure: JSTQE'18 ([52]), EDL'17 ([57]), IEDM'16 ([51]), JSSC'15 ([35]), NSS'14 ([58])*

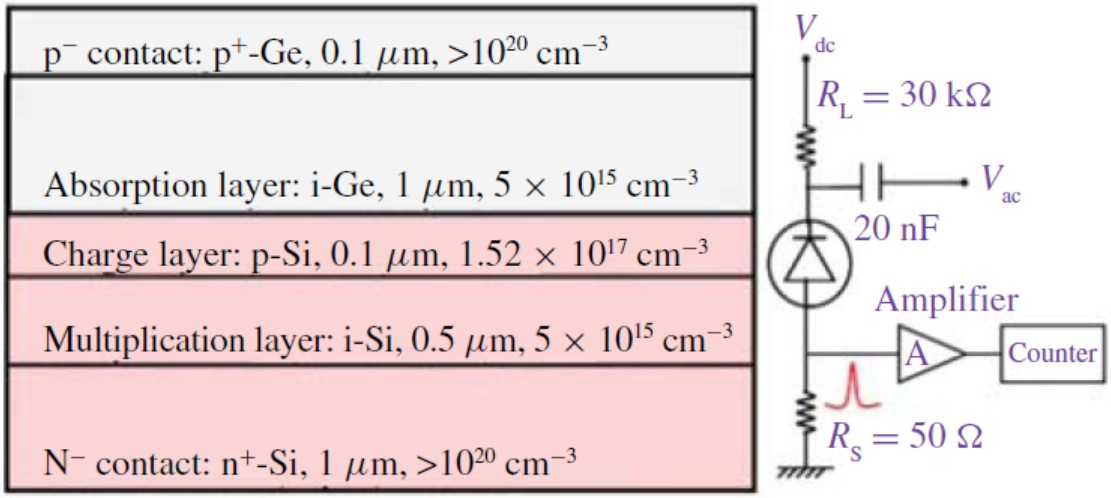

Figure 1.5: *Separate Absorption Charge and Multiplication (SACM) structure, from [59]).*

1.2.4 Time Jitter

In SPAD, the time interval between the arrival of the photon and the beginning of the avalanche effect is not constant, presenting statistical fluctuations. When analyzing

photon arrival time distribution, one can define time jitter (or timing resolution) as its Full-Width at Half Maximum (FWHM) [7], [61], [62]. In the ideal case where jitter is zero, every pulse in the output signal starts after the same time delay from the photon absorption. The variations that occur in real devices are due mainly to discrepancies in avalanche process and associated electronics. This FOM is also a function of impinging wavelength and the specific place where avalanche is initiated. [63]

In order to measure time jitter, one common procedure is to bias the SPAD at its operation voltage above breakdown, and then to illuminate it by using a picosecond laser diode source with known pulse width, repetition rate and emitted wavelength. Then, the time interval between the source trigger signal and the corresponding leading edge of the SPAD output signal is measured several times. By making a histogram of this data, it is possible to estimate the time jitter, taken as the FWHM [64]. One example of such type of histogram can be seen in Fig. 1.6, from [14].

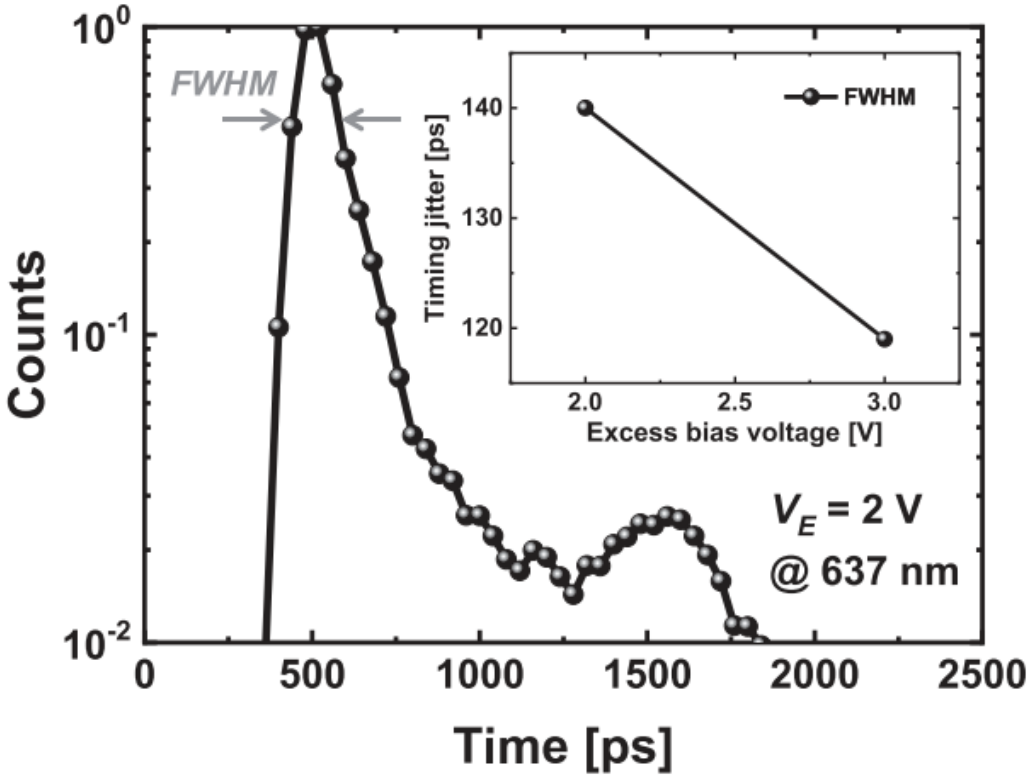

Figure 1.6: *Time jitter example from [14]*

The so-called "tail" present in the time response curves for values of time bigger than the one where maximum counts occur is due to the diffusion of carriers generated in the neutral regions, when they diffuse into the SCR (multiplication region) [62], [64]–[66].

1.2.5 Fill Factor

Another decisive FOM for SPAD detector is the Fill Factor (FF), defined as the ratio between the photosensitive and total areas of the pixel, including quench and recharge circuits. The size of both associated electronics and guard rings (low doped zones used to reduce electric field at edges) represents the main causes for the unwanted reduced FF to the order of a few percent [7].

When estimating Photon Detection Efficiency (PDE), a high FF is desirable, since the total device efficiency is expressed as the product of PDP by FF [6]. Thus, many recent research papers have focused on improving integration techniques of SPAD devices for increasing FF, such as the use of microlenses [31], [67], [68] and 3D stacking [53], [57], [69].

Microlens arrays can be used to highly improve FF [18], [31], [37], [67], [70]–[72], as illustrated in Fig. 1.7. They also improve PDP characteristics, by focusing the optical beam into the center of the diode, raising the collection of the optical signal in the device. Also, the use of metal layers is not compromised with the introduction of such apparatus, guaranteeing high digital gate density [31]. Nevertheless, their integration often require several technological constraints and is not always possible in available commercial technologies [1].

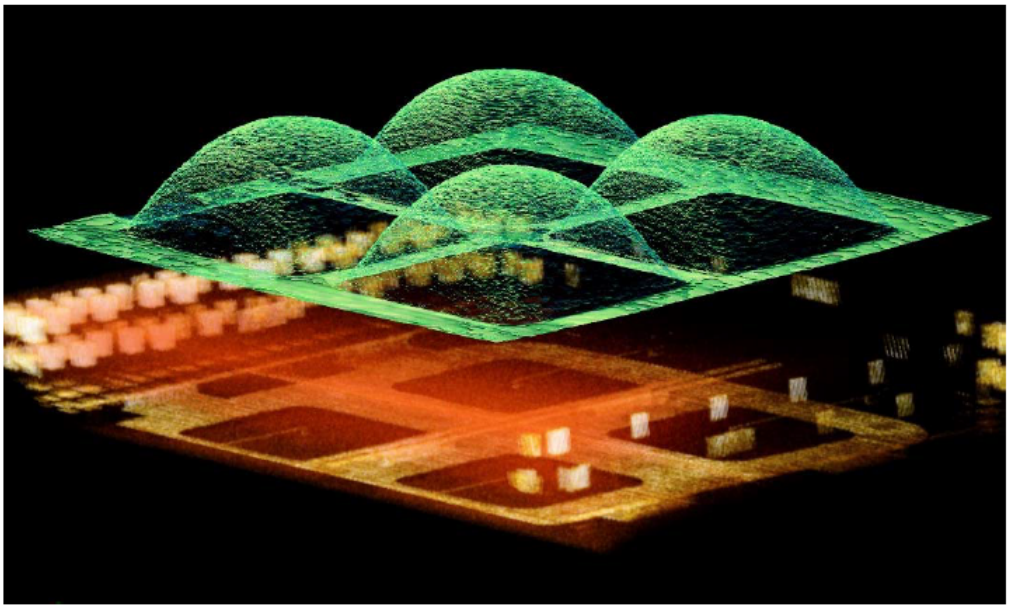

Figure 1.7: *3D FIB-SEM characterization of the microlenses from [31]*

In 3D stacking, two dies are superposed and interconnected, one hosting the SPAD devices and another one for integrating associated electronics. In this approach, two different dedicated technologies can be used for the optimization of the chips' individual performances. Since SPAD and its electronics are vertically assembled, instead of being placed side-by-side, a better FF is obtained, but at a cost of an expensive and very complex technological procedure [53], [57], [69].

1.2.6 Crosstalk

When implementing SPAD matrices, optical and electrical crosstalks are two factors that may adversely affect the correct functioning of the system. When a photon is absorbed in one pixel of the matrix, a lateral diffusion of carriers can be triggered, reaching perhaps an adjacent SPAD (electrical nature). In the case of optical crosstalk, when an avalanche is generated, it often produces an electroluminescence effect, emitting photons that can possibly be absorbed in a neighbor cell's SCR, as illustrated in Fig. 1.8. For both cases, the result is a false detection, which needs to be avoided. During design phase, crosstalk effects have to be taken into account when estimating spacing between neighbor SPAD cells. The final result is generally a reduction of FF [1], [73].

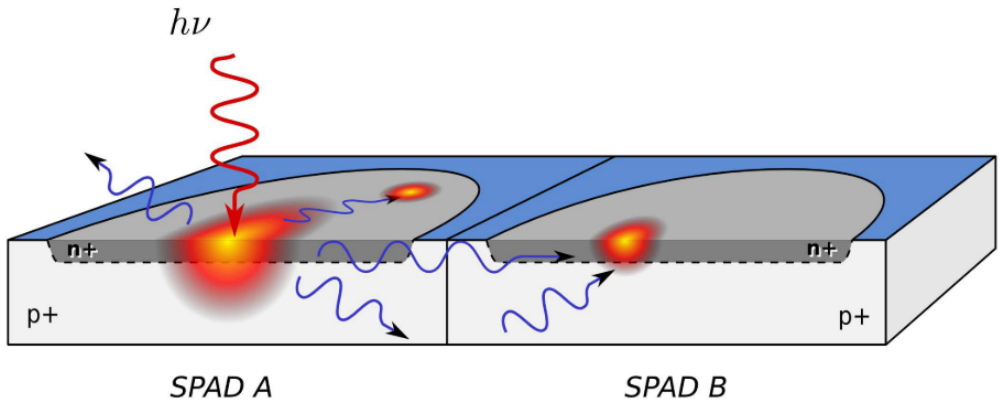

Figure 1.8: *Illustration of optical crosstalk effect for two adjacent SPAD. [73]*

1.3 Applications

Thanks to the high sensitivity and picosecond timing resolution of SPAD devices, they can be used for several different purposes, such as Time Correlated Single Photon Counting (TCSPC) measurements, Fluorescence Lifetime Imaging Microscopy (FLIM) [74]–[80], Time-Of-Flight (TOF) [36], [81]–[88], detection of charged particles [2]–[5], [69], [89], [90].

In Time-Of-Flight (TOF) (Fig. 1.9), a luminous source emits a monochromatic or wide-spectral signal, that is then reflected by a target object and impinges the detector. In direct time-of-flight, the time elapsed between the start signal (connected to the light source) and the stop signal, produced by the sensor, is measured. SPAD detectors are remarkably good candidates for this type of measurement, thanks to their timing resolution of the order of tens of picoseconds [6]. Time-Of-Flight (TOF) is a great option for applications such as 3D imaging [36], [82], [83], [86], [87], Light Imaging Detection and Ranging (LIDAR) and smart driving [81], [83], [85]. The use of such approach has the big advantage of easy integration in CMOS technology.

Nevertheless, for short distances, a resolution of a few picoseconds is required, which is not possible to obtain with SPADs operating at room temperature. In order

to overcome this limitation, electronic instrumentation techniques are needed, such as performing several measurements and averaging the results. A typical procedure is to employ Time Correlated Single Photon Counting (TCSPC) [6].

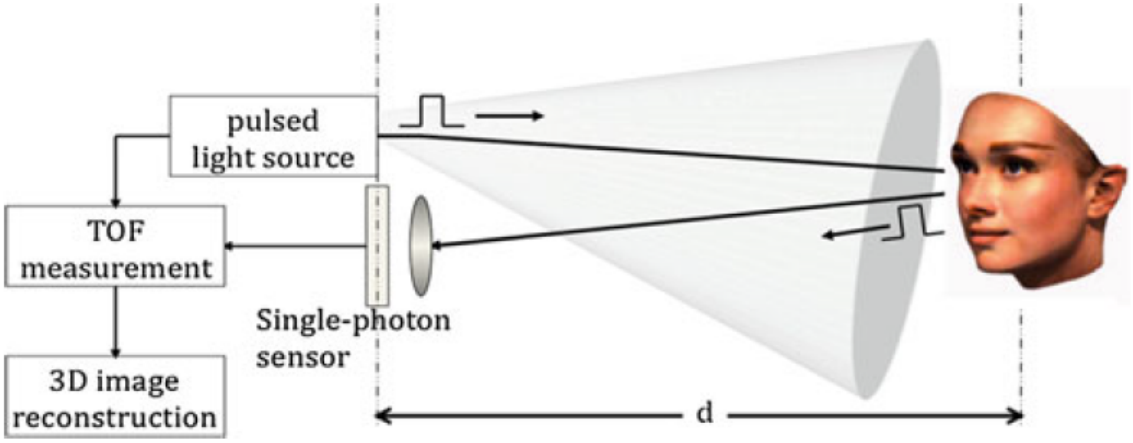

Figure 1.9: *Schematic of a Time-Of-Flight (TOF) measurement for 3D imaging applications, from [6].*

Fluorescence Lifetime Imaging Microscopy (FLIM) is an imaging method very used in biological sciences for identifying dyed components in samples. The different dyes have specific spectral signatures. For this purpose, it is possible to use fluorophores: fluorescent chemical compounds that can re-emit light after an initial light excitation. They have an associated lifetime (often in the order of nanoseconds), which represents the exponential fluorescent decay time after the removal of the excitation source and depends on the environment conditions [77], [91].

One of the standard techniques used for measuring this fluorescence lifetime is TCSPC, mainly because of its high accuracy. The approach here is to excite several points of the sample with a laser source operating with pulsated signal. Then, one can measure the arrival time of the corresponding photon from the fluorescent response of the sample. The process is then repeated several times and a histogram of those arrival times is built. The lifetime is therefore extracted from the exponential fit of the distribution, as shown in Fig. 1.10 [77], [79].

Another application of SPAD is the direct detection of charged particles. In this context, since an intrinsic DCR is always present in SPAD and sometimes at a rate much higher than the signal, one convenient approach is the use of coincidence signals, when a particle impinges two superposed detectors, as shown in Fig. 1.11 [2]–[5]. In this figure, the continuous waveforms represent the SPAD output signals, while the dashed lines symbolize the ultra-short pulses (whose width represents the coincidence time-window) that are synchronous to the leading edge of an avalanche event. This concept allows the efficient detection of charged particles at rates that are much lower than the SPAD DCR, which is often the case of medical and high energy physics applications [3].

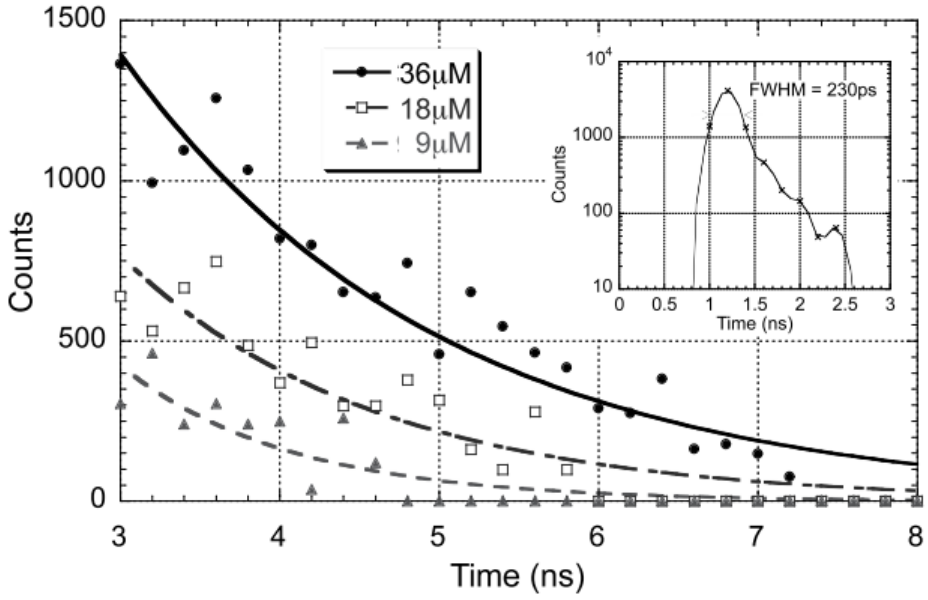

Figure 1.10: *Histogram of photon counts resulting from FLIM measurements for different spots of a DNA sample. The inset shows a median FWHM jitter of* 230 ps *for the detector. The excitation source is based on a pulsed laser diode (Advanced Laser Diode System, GmbH, Germany) with a wavelength of* 637 nm *and a pulse width of* 40 ps *(FWHM). From: [79].*

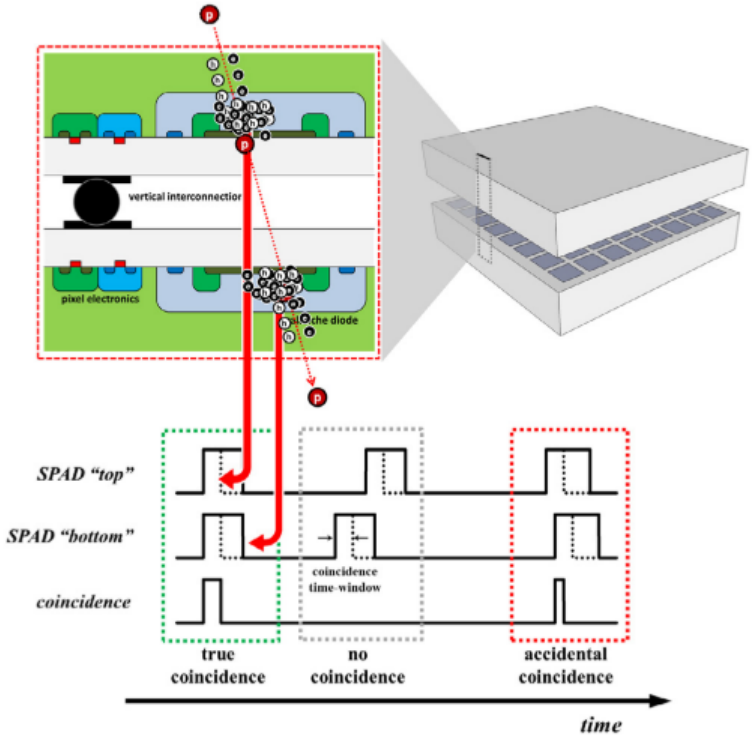

Figure 1.11: *A 3D-SiCAD (Silicon Coincidence Avalanche Detector) pixel: schematic representation of the detection concept considering a possible implementation in a CMOS process, from: [3].*

1.4 State of the Art of SPAD in CMOS technologies

1.4.1 SPAD in CMOS Bulk Technologies

Even if different materials can be used for Geiger-mode diodes implementation (such as Ge-on-Si [60], [92], [93] and InP/InGaAs [39], [70], [94], [95]), their integration with mass production CMOS electronics is not always simple. Hence, since the first SPAD implemented in CMOS [21], [30], that provided monolithic integration with reliable and reproducible readout electronics, those devices received much more attention in the market, due to their low cost and high-performance fully integrated imaging systems.

The main difficulty when integrating imagers in advanced CMOS is that these technologies are normally not conceived for this purpose. Instead, their main objective is reducing transistor size, while improving circuit efficiency. This often imposes restraining design rules that adversely affect conceiving SPAD devices, such as the requirement of orthogonal shapes, generally problematic when a uniform electric field is desired, which is the case for SPAD. For reducing the edge effects caused, lower doped regions (known as guard-rings) are placed at the lateral borders of the junction. Besides, the wells in commercial advanced CMOS technologies generally present very high doping levels, which translates in high DCR and low PDP. Thus, the use of dedicated CMOS Image Sensor (CIS) technologies is preferable from the point of view of optimized SPAD performance [54], [96].

By considering the aforementioned FOMs, some recent SPAD implemented in CMOS present the current State of the Art (SOTA). The best results up to this date are obtained by using 3D stacking techniques at wafer level, because they provide the combination of the best dedicated technologies (for SPAD, but also for data processing), resulting in optimized developments, according to application.

When it comes to 3D stacking, its main advantages are the higher fill factor and the better NIR response for BSI, which is suitable for LIDAR applications. For this approach, the SPAD is implemented in the top-tier chip (normally conceived in a dedicated CIS), while the associated electronics for data processing are integrated in the bottom-tier chip (conventionally realized in advanced CMOS), providing better energy efficiency solutions, with reduced consumption [35], [51]–[54], [57], [58], [96], [97].

There are two possible ways of assembling the independent tiers, according to the kind of illumination desired, as shown in Fig. 1.12. The top-tier is always the one that contain the SPAD, but in FSI, the bottom of this die is connected to the top of the one containing the electronics. In this case, additional Through-Silicon Vias (TSV) are required for the necessary interconnections, since the junction is shallower. For the same reason, this method is more adapted for detection of Near Ultra Violet (NUV) radiation or visible light. On the other hand, for BSI, face-to-face stacking is implemented and the junction is naturally much deeper. Backside thinning becomes often necessary for enhancing PDP, and this approach is, then, more adapted for red and NIR sensing [98].

For the 3D stacking with face-to-face interconnection, the top-tier can benefit from a die thinning process of few micrometers, improving PDP at a chosen range of wavelengths [54]. The main drawback when using 3D stacking lies in the limit of transistors' operating voltage and consequently, in the limitation of excess bias, when

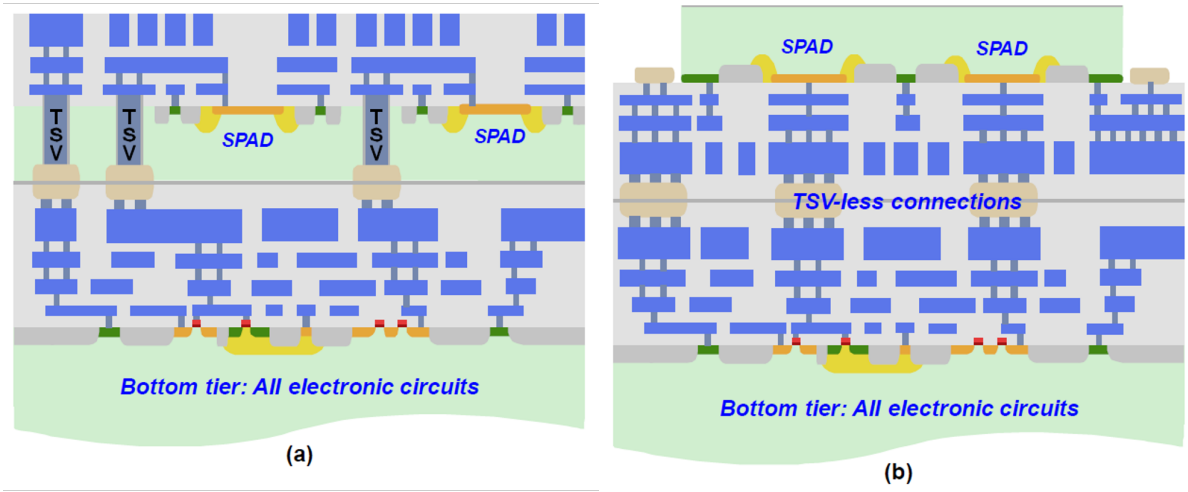

Figure 1.12: *Types of 3D assembling, according to the desired approach of illumination: (a) Front Side Illumination (FSI); (b)Back Side Illumination (BSI). Adapted from [98]*

using a single transistor as quenching circuit. This inconvenience might be a non-negligible disadvantage, because increasing excess voltage often produces better time jitter and PDP [57].

Over time, both tiers experienced better performance with the evolution of their respective dedicated technologies. Concerning the die hosting the diode, in [57], implemented with 65/40 nm technologies (respectively for top and bottom dies), an afterpulsing probability of 0.08% was achieved, thanks to a combination of passive quenching and active recharging, with a recharge time of 8 ns, at excess bias voltage of 4.4 V, representing a suitable device for photon counting rates as high as 125 Mcps.

In [52]–[54], using 45/65 nm technologies, it was possible to obtain the best DCR, PDP, jitter and FF for 3D-stacking CMOS SPAD so far. A comparison between those results and the previous SOTA is presented in Fig. 1.13, for DCR and in Fig. 1.14, for PDP.

Comparing these different technologies at different operating conditions can be not so evident. A good way to compare and interpret those results is by plotting PDP as a function of DCR, as shown in Fig. 1.15 (a). The highest PDP obtained at lowest DCR is then the most efficient device for the given operating conditions.

Finally, time jitter analysis is of high importance when comparing SPADs. The SOTA results for this parameter is presented in Fig. 1.15 (b). Even if those results represent very low values of jitter in CMOS devices, it should be noted that they were not obtained for the exact same operating conditions (particularly, wavelength). Thus, they are not necessarily suitable for the same applications.

Another very interesting work was published in [31], where a CIS 40 nm technology was used. The SPAD junction being composed of a P-well (PW) and a Deep N-well (DNW), as illustrated in Fig. 1.16. Their implants were especially calibrated for optimization of SPAD characteristics. A dedicated microlens process was also developed, for lowering attenuation effect in the several layers placed over the device.

This SPAD presents excellent results at room temperature at 1 V excess voltage,

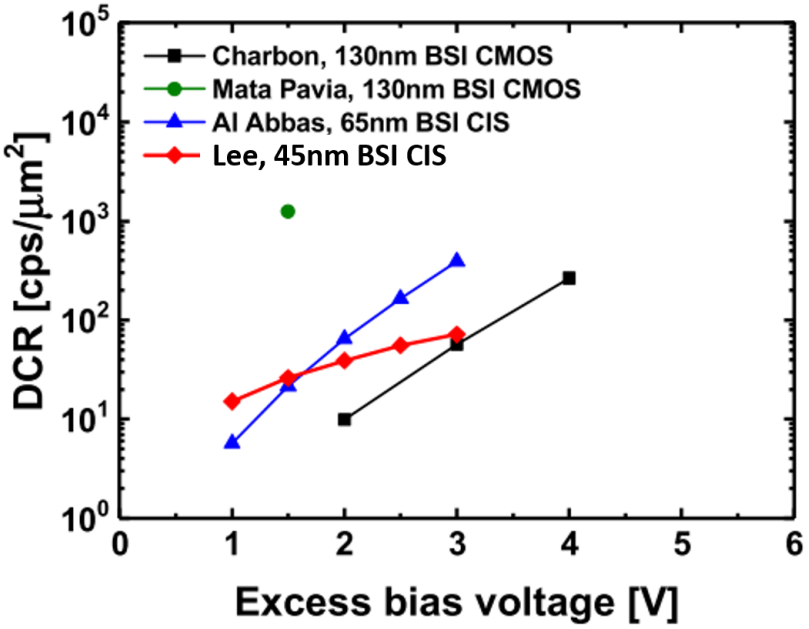

Figure 1.13: *Comparison between SOTA DCR values according to excess voltage. (Adapted from: [54]). References in the figure: Charbon ([58]), Mata Pavia ([35]), Abbas ([51])*

such as: DCR around 50 counts per second (cps), afterpulsing probability at 0.1%, PDP around 5% and time jitter equals 140 ps, at 840 nm. Optical crosstalk was also estimated to be lower than 2%. Besides those prodigious results, this integration can be directly used for 3D stacking processes [31].

As seen previously, SPAD characteristics depend on several conditions: internal (such as doping levels of the wells composing the junction, the density of defects in silicon and silicon-oxide interface in contact with SCR) and external (as the applied voltage, temperature, and impinging wavelength). Those conditions need to be carefully taken into account when using SPAD for a given application.

1.4.2 SPAD Associated Electronics for Quenching and Recharge

As previously mentioned, in order to avoid damaging the SPAD device, due to high current values present in its operation, quench and recharge circuits are needed. Since the objective of this PhD Thesis is not the development of high performance quench and recharge circuits, the review here presented is not exhaustive [7].

The simplest circuit for achieving this purpose is the ballast resistor (possibly being implemented by means of a MOS transistor), as presented in Fig. 1.17. When avalanche current flows, the voltage across the resistor is enhanced, thus automatically reducing the voltage across the diode, and eventually its current. Through this same ballast resistive device, the diode's voltage is increased back to its original value [7]. Passive circuits are largely used when it comes to selection of devices among different variants during the first characterizations, because they are compact and have reduced power consumption [11], [99]–[101].

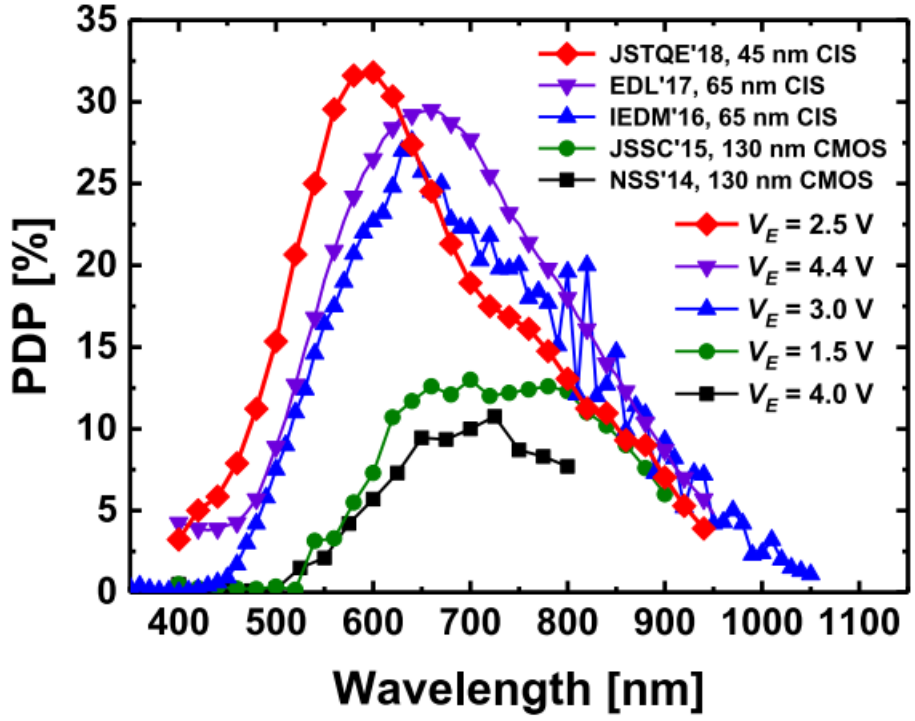

Figure 1.14: *Comparison between SOTA PDP values according to wavelength. (Original figure from [14]). References in the figure: JSTQE'18 ([52]), EDL'17 ([57]), IEDM'16 ([51]), JSSC'15 ([35]), NSS'14 ([58])*

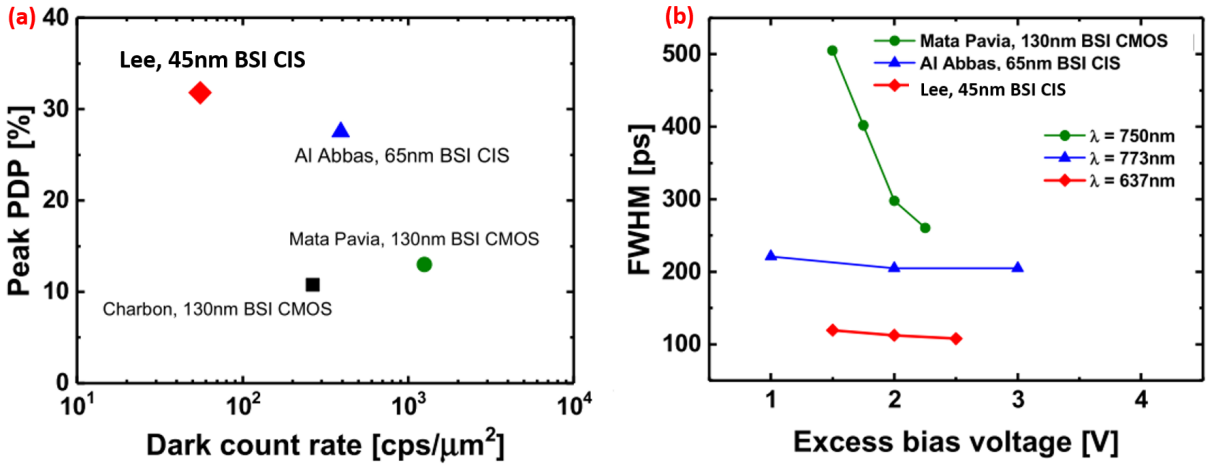

Figure 1.15: *Comparison between SOTA: (a) PDP values according to their corresponding DCR values. (b) Time jitter according to V_{ex} (Adapted from: [54]). References in the figure: Lee ([54]), Charbon ([58]), Mata Pavia ([35]), Abbas ([51])*

However, in order to obtain the best characterization of devices in optimal conditions, active circuits are needed. Several architectures have been proposed [23], [94], [102], [103]. In every case (see Fig. 1.18), the active circuit first needs to detect the

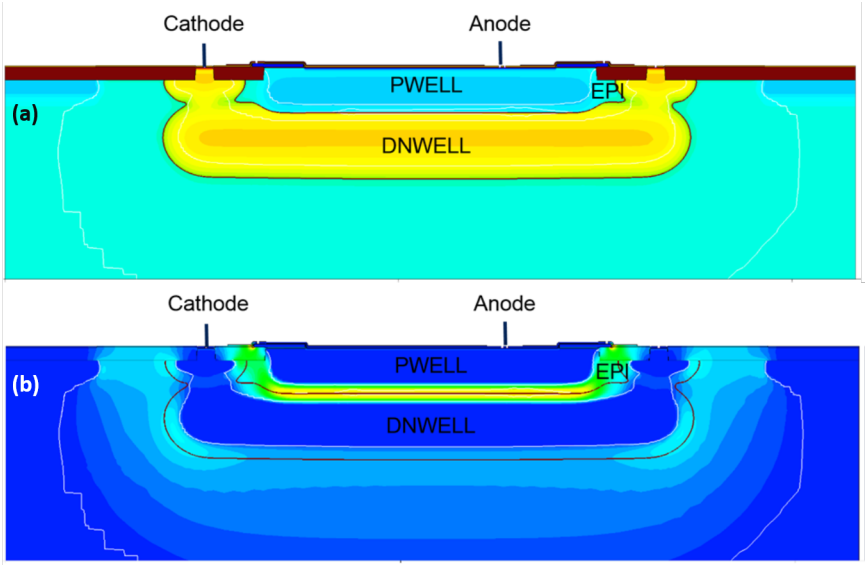

Figure 1.16: *SPAD implemented in CMOS* 40 nm *technology: (a) Doping; (b) Electric field. Adapted from [31].*

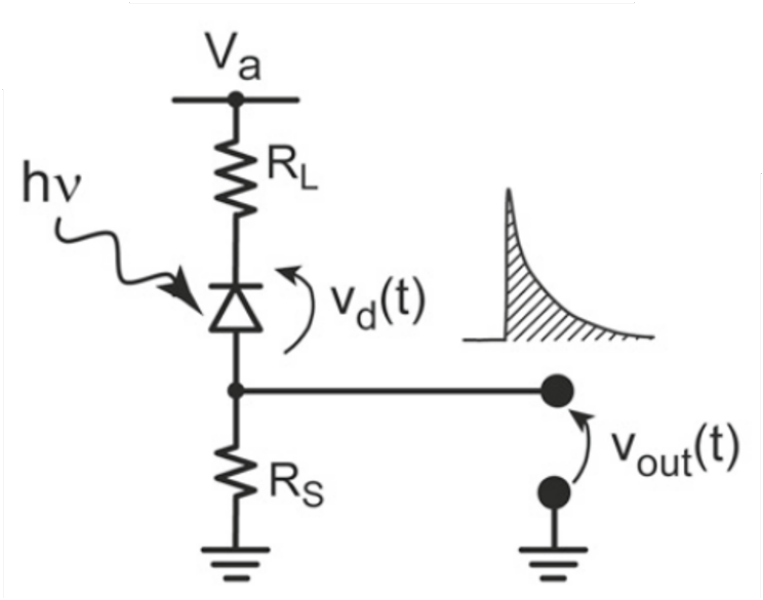

Figure 1.17: *Ballast resistor used as Passive Quenching Circuit (PQC). Adapted from [7].*

avalanche pulse generated by the SPAD (by using a fast comparator, for example). Once this task is accomplished, it should quickly reduce the reverse bias voltage to a value below breakdown, keeping this value during the so-called hold-off time (often defined by the user). Then, the device voltage is increased back to its original value for a new detection. This approach have the great advantage of being fast, which implies that the number of charges that go through the junction is decreased and thus afterpulsing probability is reduced. Also, a quick recharge makes the device ready for a new detection faster, which increases the chance of correctly sensing a new incoming photon.

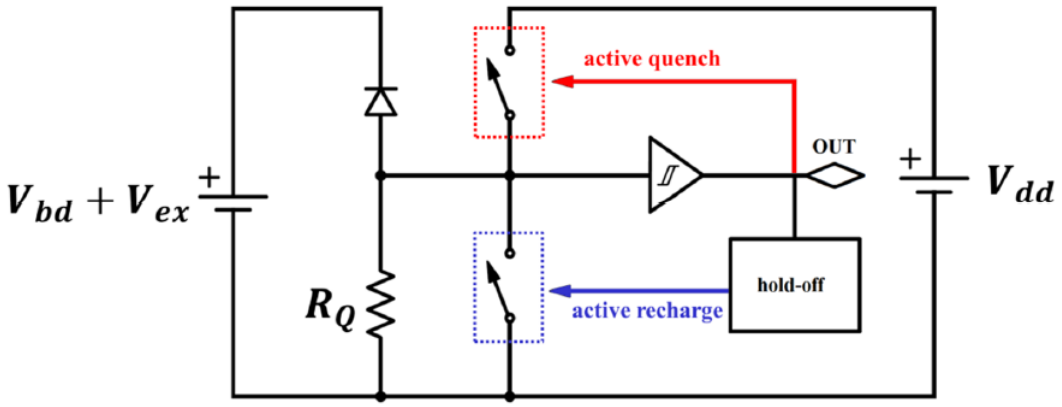

Figure 1.18: *Operating principle of active quench and recharge circuits.*

Nevertheless, often passive quench is largely sufficient for the application, recharge time being the main constraint. For this reason, but also due to simplicity and for reducing power consumption, a Passive Quench Active Recharge (PQAR) circuit is sometimes preferred [29], [36], [57], [104].

1.4.3 SPAD Implemented in Silicon On Insulator Technologies

With the evolution of transistors, attempting to pursue Moore's law, new technologies have been developed. In particular, Silicon On Insulator (SOI) has shown to be one of the most promising approaches for highly innovative and energy efficient circuits, keeping transistors isolated from substrate in a silicon film placed over a Buried Oxide (BOX) (more details in Section 2.1). The integration of SPAD in CMOS also follow those advances and researchers are often enthusiastic for developing new SPAD architectures in those modern technologies.

The first implementation of SPAD in CMOS SOI was done in 2013 [105] (and further developed and characterized in [49], [50], [99], [100], [106]) to be operational for both FSI and BSI. For those references, the pn junction is integrated in the 1.5 µm doped silicon film placed over BOX, as shown in Fig. 1.19. The original substrate is then etched until reaching the buried oxide. Breakdown voltage was measured to be around 12 V, and DCR was measured for different temperatures (Fig. 1.20 (a)), having its main cause due to Band To Band Tunneling (B2B). PDP (Fig. 1.20 (b)) has its peak at 460 nm (11% in FSI, 6% in BSI) and jitter is approximately 500 ps at 1.2 V excess bias, being improved (65 ps (FWHM) at room temperature, 3 V excess bias, and 405 nm wavelength in BSI) in [49]. Afterpulsing is negligible at a dead time longer than 1 µs. Also, in [100], [105], since the desired applications were flexible electronics for bio-compatible imaging systems, a 10 µm-thick flexible polyimide was formed under BOX.

An updated version of this work, in which microlenses are also included, is presented in [72], [107]. An array of 1024 quenched pixels with CMOS readout and addressing circuitry were implemented. An epitaxy step is performed over the silicon film. Then, doping and diffusion steps occur. The process is made in a way that the

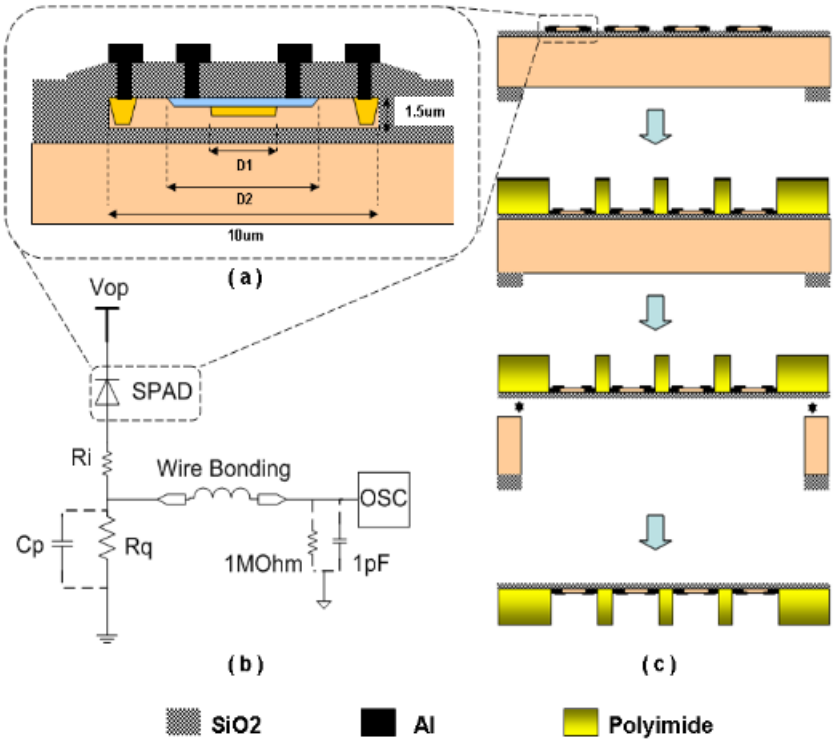

Figure 1.19: *First SPAD implemented in CMOS SOI. From [105].*

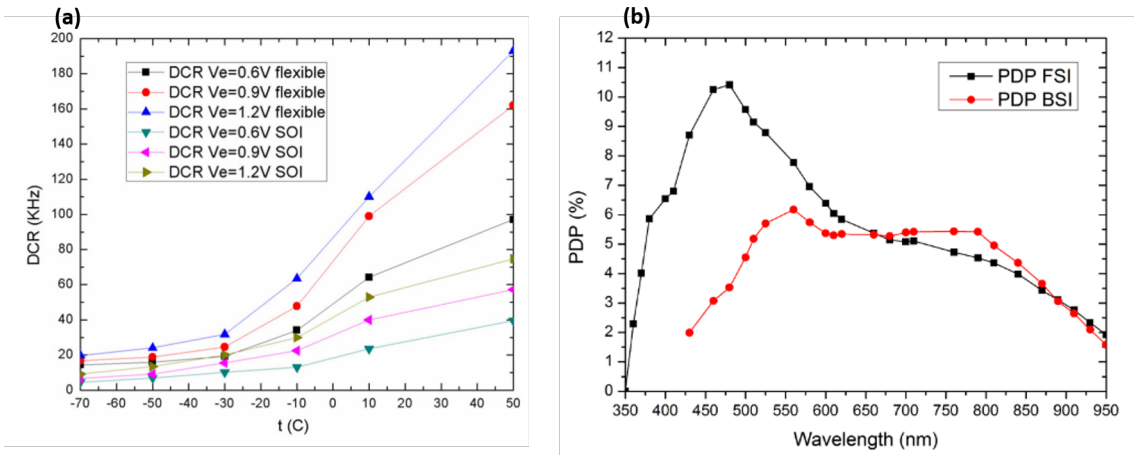

Figure 1.20: *Characteristics of the first SPAD implemented in CMOS SOI: (a) DCR, (b)PDP. Adapted from [100].*

electric field in the neutral region is enhanced, facilitating the drift into SCR, increasing PDP (e.g. 13% for both FSI and BSI, at 490 nm), as shown in Fig. 1.21. Thanks to the integrated CMOS buffer circuits at pixel-level, higher values of excess voltage could be applied (e.g. 4 V) and, due to microlenses, FF could reach values up to 10%.

The same research group pursued the study of this innovative device in [108], by analyzing the effect of different silicon on insulator thicknesses and their corresponding

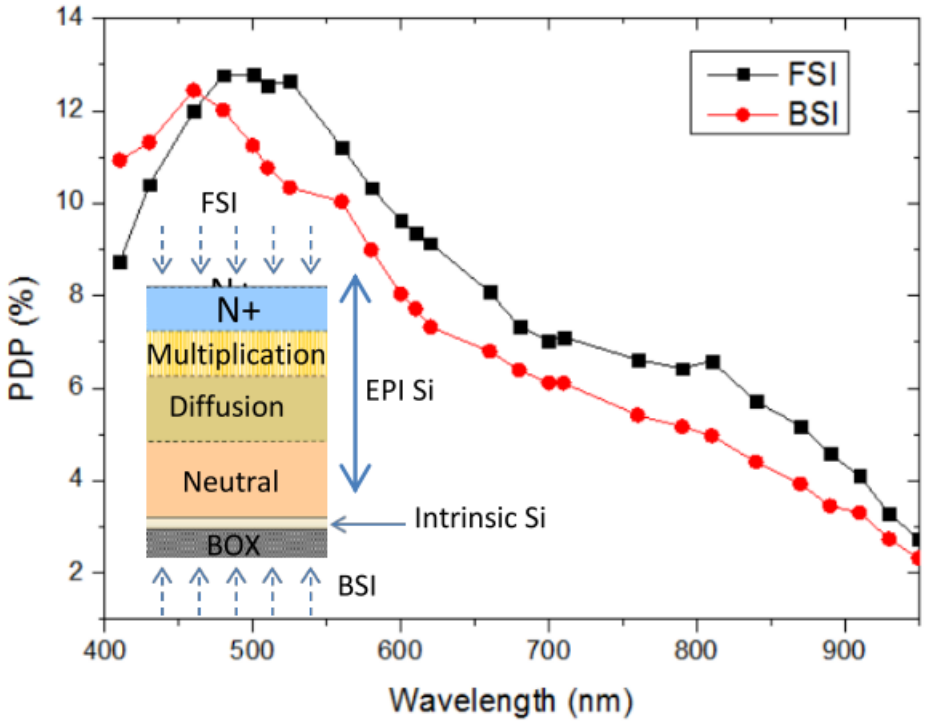

Figure 1.21: *SPAD implemented in CMOS SOI: PDP from [72].*

implanted doses. DCR (here, mainly due to B2B) could be reduced by optimizing doping in multiplication region. At cryogenic temperatures (80 K), a DCR value of 0.15 kHz/μm^2 could be obtained. FWHM jitter for this proposed device was evaluated to be 450 ps in FSI and 480 ps in BSI for 637 nm, which is consistent with the PDP symmetric performance for the two illumination approaches (13% in FSI and 12.5% in BSI).

Very recently [14], standard 140 nm SOI CMOS technology was used for developing BSI SPAD. The junction is formed from P+/N-well layers, while keeping the interfaces silicon/silicon oxide (BOX and Shallow Trench Isolation (STI) layers) far from the multiplication region of the device. Indeed, due to etching-induced crystal lattice defects and charge trapping associated with STI, DCR may be adversely raised [14]. A circular geometry was chosen for implementing the SPAD, reducing geometric Premature Edge Breakdown (PEB).

Due to relative high doping concentration of the N-well, breakdown voltage is quite low (11.25 V). Nevertheless, the fabricated devices present remarkable results, such as a DCR varying from 1.2 Hz/μm^2 to 396.1 Hz/μm^2 at room temperature, according to excess voltage. In terms of PDP, a significant sensitivity in blue, NUV and violet, as well as good values for red and NIR were obtained (Fig. 1.22). Like in most of BSI operating devices, due to the absence of metal layers, FF is enhanced. A time jitter of 119 ps was also obtained for 637 nm.

A similar process was also implemented in [32], where SPAD devices were integrated in 0.35 µm SOI technology (1 µm buried oxide and 3 µm silicon film) and were only partially characterized. The junction is composed by a p+/deep n-well in the silicon

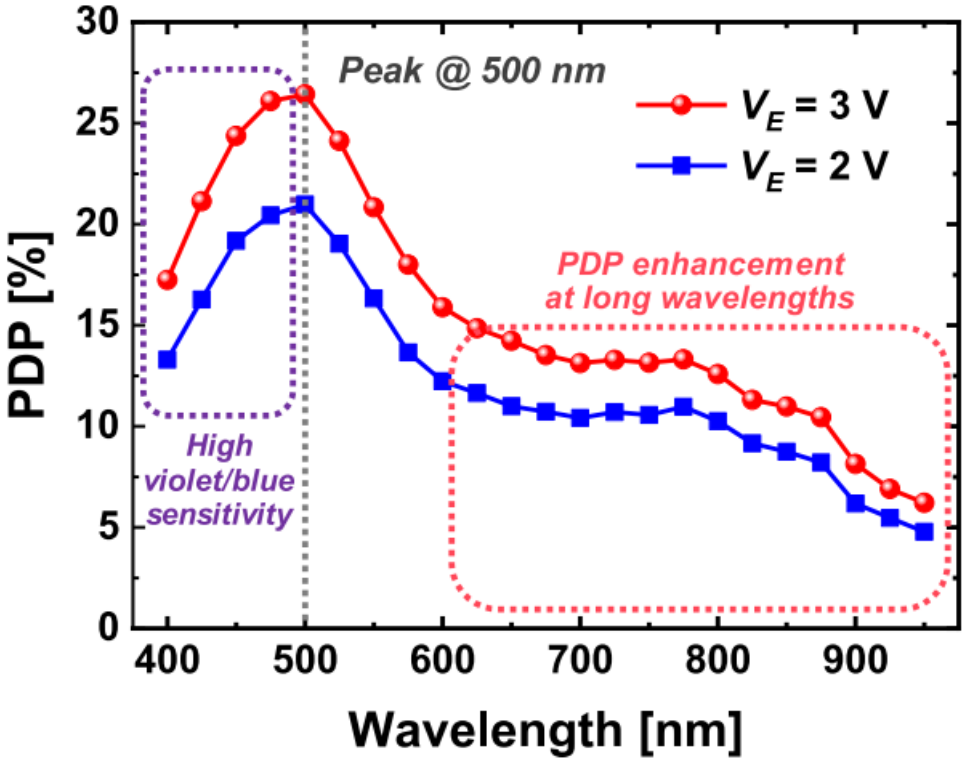

Figure 1.22: *PDP for SPAD implemented in* 140 nm *SOI CMOS technology [14].*

film, with a p guard-ring. The substrate is etched until reaching the BOX, the die is then flipped for 3D stacking with a second one with associated electronics fabricated in bulk 0.35 µm technology. With breakdown voltage around 30 V, a FF of 75% could be reached without using microlenses.

1.5 Thesis Objectives

It is important to notice that so far, in all of the reviewed papers concerning integration of SPAD in SOI technologies, the junction is placed over the BOX, used as stopping layer during etching process, mainly to improve PDP in BSI and FF.

It was only in [109], [110] that the integration of SPADs were proposed in advanced Fully Depleted Silicon On Insulator (FDSOI) technology (28 nm), by means of Technology Computer-Aided design (TCAD) simulations. Since a very thin silicon film (7 nm) is placed over an ultra thin buried oxide (25 nm), the junction stays underneath this insulation layer, while transistors are implemented in the thin silicon film, being electrically isolated from SPAD, as shown in Fig. 1.23. Those transistors could, then, be placed over the SPAD device, instead of staying side-by-side. This configuration would allow increasing FF in BSI, in an monolithic and intrinsic 3D integration of the pixels and their associated electronics, without the need of complex and expensive 3D stacking processes.

The main objective of this PhD thesis is to prove the feasibility of this challenging

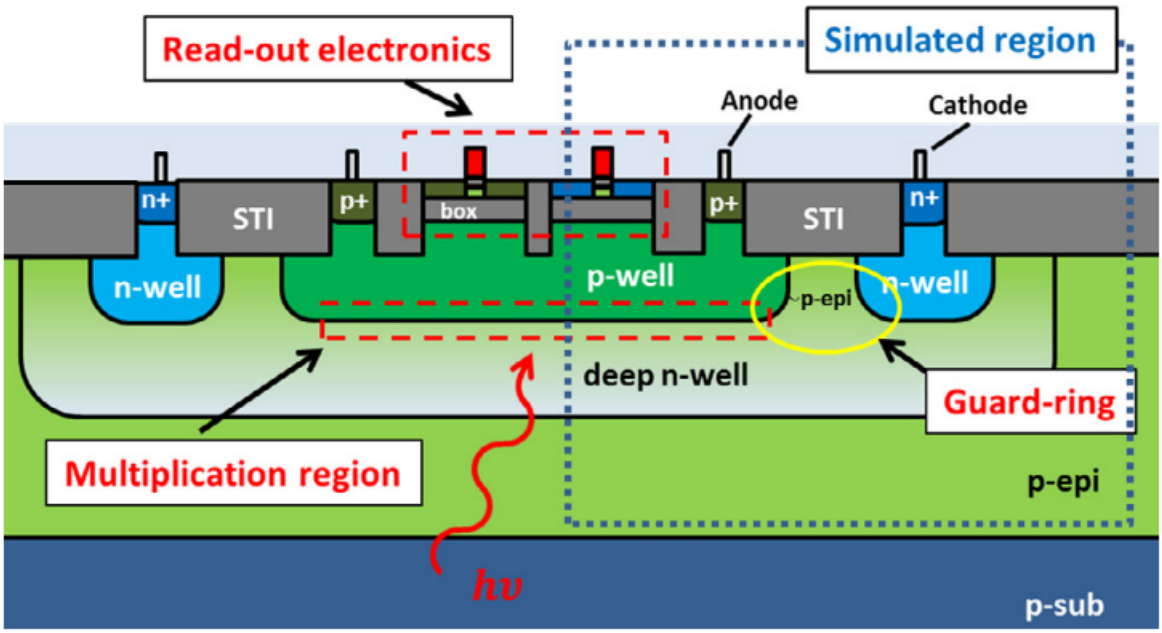

Figure 1.23: *Proposed implementation of SPAD in FDSOI CMOS technology in [110].*

and certainly interesting approach by means of SPAD design, TCAD simulation and electrical characterization. For this purpose, the advanced CMOS 28 nm FDSOI from STMicroelectronics was addressed. At first, all the design rules were respected without any process modification or customization.

We aim at the experimental demonstration of SPAD FDSOI architecture, at its electrical characterization and modeling. With those results, it was possible to propose process modifications for improving performances so the technology can be used for hosting those devices.

Conclusions

In this chapter, the operation of Geiger-mode silicon photodetectors was presented. Such devices are pn junctions biased above breakdown voltage in a quite unstable state. When a single photon is absorbed, creating a photogenerated Electron Hole Pair (EHP) inside the Space Charge Region (SCR), or inside a neutral region, but reaches the multiplication region, it is enough to produce a self-sustained avalanche very easily detectable, due to the resulting high current. The Single Photon Avalanche Diode (SPAD) device needs then to be protected from the possible damaging effects induced by this current, so quenching circuits are added to the structure. Finally, a recharge circuit brings the junction to its original state, so it can be ready for another detection.

The main Figures of Merit (FOM) of such devices are also presented: Dark Count Rate (DCR), afterpulsing, Photon Detection Probability and Efficiency (PDP, PDE), time jitter, Fill Factor (FF) and crosstalk. DCR representing the intrinsic noise, it is a key parameter for providing efficient photon detection, which highly depends on the electric field at the multiplication region and, as a consequence, on the applied voltage bias.

Afterpulsing characterizes the probability to observe "echo" events, due to carriers' trapping and releasing processes after primary avalanches. Time jitter refers the statistic deviation between the moment at which the photon is absorbed and the actual detection of the avalanche, being an extremely important FOM to some applications such as Time-Of-Flight (TOF). The fill factor being the ratio between the active area and the total pixel's surface, its estimation is needed for device photon detection efficiency calculation. Crosstalk quantifies the coupling (electrical and optical) between SPAD pixels in matrix configuration.

Then, the State of the Art (SOTA) for SPAD is briefly reviewed, focusing on the CMOS implementations, since these technologies provide the most reliable and reproducible electronic circuits. In this context, the most advanced devices are compared by means of the aforementioned FOM and their corresponding operation conditions, such as voltage bias, temperature and mode of illumination (Front Side Illumination (FSI) or Back Side Illumination (BSI)). Up to this date, the most efficient technique employed is 3D stacking, when two dies are assembled, the first one hosting the SPAD devices, while the second one accommodates the associated pixel electronics. In this case, the different tiers are individually optimized for their purpose: CMOS Image Sensor (CIS) technologies being used for the SPAD integration, while transistors are implemented in advanced CMOS. 3D SPAD offers the best trade-off between photodetection efficiency and fill factor, but requires complex and expensive technological processes.

One of the CMOS most outstanding technologies nowadays uses Silicon On Insulator (SOI). Some SPADs have recently being integrated in such a technology, using the silicon film placed over the Buried Oxide (BOX) to implement the pn junction. As SOI evolved, the silicon film became thinner and, in 2016, the first SPAD integrated in FDSOI (under the BOX layer) was proposed by means of TCAD simulation. Its main advantage being the monolithic 3D integration of SPAD and its associated electronics, which is the object of study of the next chapters of this PhD dissertation.

In Chapter 2, the design of SPAD cells in CMOS 28 nm FDSOI is addressed, along with the main technological constraints, due to design rules.

In Chapter 3, the simulation and modeling of the designed cells is presented. Discussions are made about doping profiles, carrier generation and avalanche processes, with some proposed improvements.

In Chapter 4, the electrical characterization of the fabricated devices is discussed. Comparisons are made between the different variants of SPAD cells, while conclusions about their performances are presented.

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Chapter 2

SPAD Cells Design in CMOS FDSOI 28 nm Technology

In this chapter, the CMOS Fully Depleted Silicon On Insulator (FDSOI) technology is presented, along with its main advantages, that make it very worthwhile for future applications, where energy efficiency is priority. The integration of SPAD in such an advanced technology was then addressed in section 2.2. For this purpose, the native commercial CMOS 28 nm FDSOI technology from STMicroelectronics was used. At a first step, no design customization was done, i.e., all design rules were respected. The methodology for developing such cells is reported, design rules constraints are also presented, forcing adaptations of SPAD cells. The designed cells are then described, with their respective fundamental elements (e.g. photosensitive areas, contacts), necessary for the correct functioning of the cells. Then, Section 2.4.2 is dedicated to present an indirect avalanche sensing circuit, possible to implement thanks to the body biasing effect in FDSOI. The antenna effect in FDSOI is briefly discussed, since it was a source of problems for some of the implemented devices. Finally, the top layout of the fabricated circuits is presented, along with a dedicated Printed Circuit Board (PCB), used for electric characterization.

2.1 CMOS 28 nm FDSOI Technology

Although bulk CMOS has been widely used in electronics for decades, due mainly to the good-quality oxide in silicon, it still presents limitations below 40 nm node. Metal Oxide Semiconductor Field Effect Transistor (MOSFET) integrated in bulk technologies often only occupy the very top region of their silicon wafer, leaving more than 99% of total volume to be the base substrate, serving almost exclusively as a simple mechanical support for most applications. This bulk integration is also responsible for inducing several parasitic effects that can deteriorate transistors' performance, such as non-negligible drain/source to substrate capacitance, latch-up (i.e., unintentional activation of parasitic devices, such as inherent PNPN thyristor) and leakage current. These undesired effects become even more critical as devices are scaled-down below 40 nm, when the channel electrostatic control requires new architectures (FinFET, Gate-All-Around FET, and FDSOI) [1]–[4].

A very clever solution to overcome these limitations was the use of SOI structures.

In such devices, transistors are dielectrically isolated from the substrate, thanks to a BOX layer, as can be seen in Fig. 2.1. Thanks to the SiO_2 BOX, the maximum capacitance between junctions is reduced to the buried oxide's, making this approach suitable for high-speed operation at the same time that allows low voltage supply and low leakage current, reducing thus power consumption as well. Since there is no electrical contact between transistors and substrate, the PNPN junctions no longer exist and latch-up problems are also solved [1], [3].

As the CMOS SOI technologies evolved, the thickness of both the silicon film and the buried oxide were reduced, becoming today as narrow as 7 nm for the former and 25 nm for the latter (see Fig. 2.2) in commercial Ultra Thin BOX and Body (UTBB) CMOS28FDSOI technology from STMicroelectronics (hereby named C28FDSOI) [5]–[7]. FD stands for Fully-Depleted, which means the whole silicon film is depleted, presenting no neutral zone. This feature provides several advantages, such as a low threshold voltage, small leakage current and smaller floating-body effects. Also, improvements are observed in the slope in sub-threshold region, as well as in Drain-Induced Barrier Lowering (DIBL). These characteristics make FDSOI most suitable for low-voltage operation, and thus for low power consumption market [3], [7], [8].

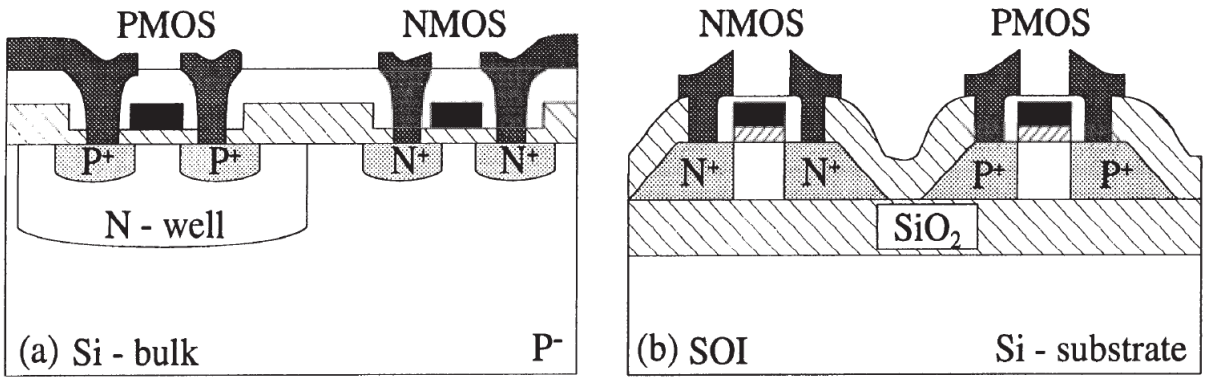

Figure 2.1: *Comparison between bulk (a) and SOI (b) structures. (Adapted from [1])*

In C28FDSOI, two distinct families of transistors exist, according to the body doping type underneath the BOX (PW or N-Well (NW)): Regular V_{th} (RVT) and Low V_{th} (LVT), as can be seen in Fig. 2.3 (a) and (b). The former keeps the original bulk configuration, i.e., the bodies have the source-drain opposite doping type. LVT devices, also called "flipped-well", have the same well type [7], [8].

C28FDSOI has another intrinsic and ingenious trait, which is the possibility to use dynamic body-biasing techniques, consisting essentially of applying a voltage bias to the well underneath transistors, as illustrated in Fig. 2.2 (b). Even if this technique is well known for bulk technologies, it has very limited range of voltage bias (see Fig. 2.4) and also becomes less efficient for advanced bulk technologies [9], [10]. Nevertheless, it does not degrade in FDSOI, where it is the key aspect that grants great versatility to this technology, since it will adjust threshold voltage (V_{th}) according to body voltage (V_{bb}), either for increasing speed and performance, in case of Forward Body Biasing (FBB), or for reducing leakage power consumption, in case of Reverse Body Biasing (RBB).

When performing RBB, the absolute value of the threshold voltage of transistors is

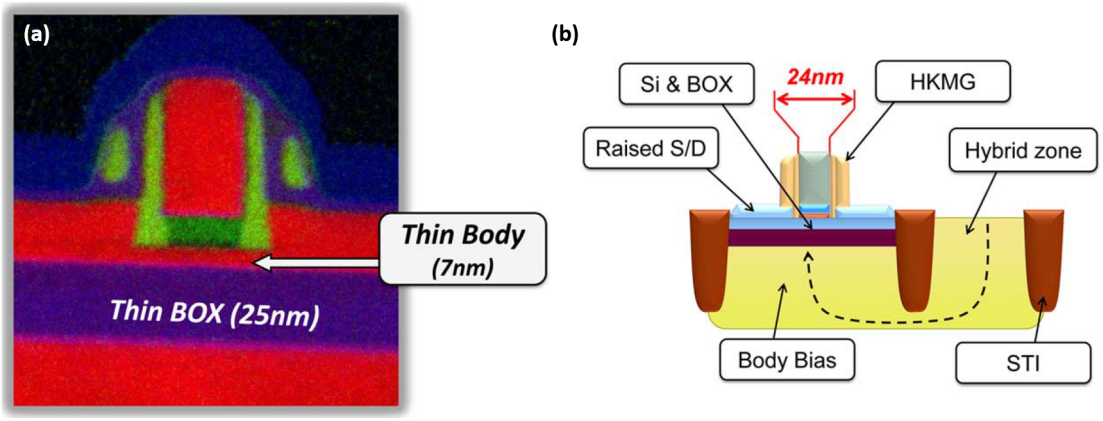

Figure 2.2: *Planar transistor integrated in CMOS 28nm FDSOI (a) TEM cross section (b) Generic cross section. (Adapted from [8])*

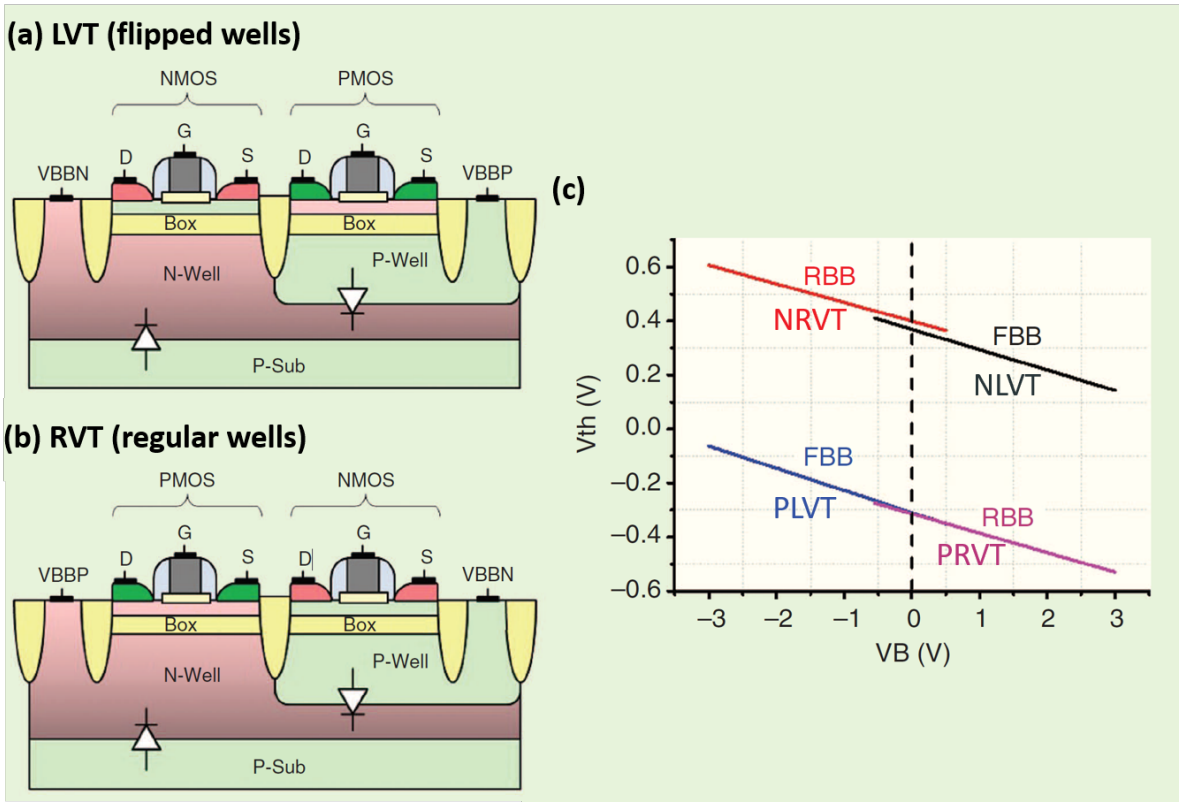

Figure 2.3: *Cross section of C28FDSOI transistor families : (a) LVT, Low threshold voltage; (b) RVT, Regular threshold voltage; (c) Threshold voltage variation according to Body Voltage for NMOS and PMOS transistors of both families (Adapted from [7]).*

increased, which can in turn produce a significant reduction of leakage current. It can be achieved by decreasing the body bias voltage in NMOS and by enhancing it for PMOS. Similarly, FBB implies in a reduction of $|V_{th}|$, which can be conveniently exploited for boosting performance. In order to produce this type of body biasing, one can reduce the

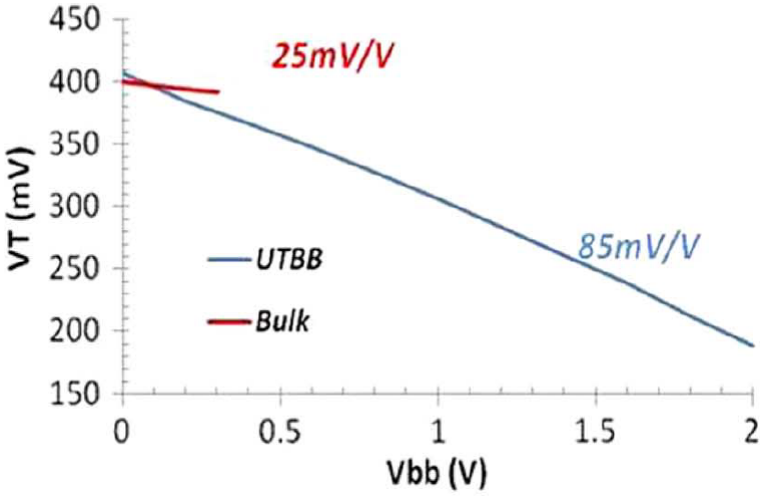

Figure 2.4: *Variation of threshold voltage according to body biasing voltage for C28FDSOI and Bulk (From [8])*

body bias voltage in PMOS and also increase it for NMOS. RVT transistors are the most suited for RBB, while the fast but leaky LVT transistors can be best employed when using FBB, as can observed in Fig. 2.3 (c) [7], [11].

It should be noted that at least two thicknesses for the front gate oxide are available in C28FDSOI, the default value being 18 Å. Thicker gate oxide transistors are also available (28 Å). The transistors featuring this larger value of thickness can be biased up to V_{DS} = 1.8 V and are referred to as EG transistors, for extended gate. Another attractive feature of these transistors is their larger body-bias factor ($\Delta V_{th}/\Delta V_{bb}$ = 140 mV/V), while normal gate thickness transistors provide 85 mV/V and can only be biased up to V_{DS} = 1 V.

After these considerations, it is clear that bulk technologies won't fulfill the requirements of future circuits in both performance or energy efficiency, C28FDSOI being one of the most suited alternatives for the aforementioned demands. The choice of such a technology for integrating SPAD devices is certainly appropriate for upcoming applications, such as Internet of Things, 3D cameras and smart driving.

In addition to the remarkable advantages presented previously, the fact that the SPAD junctions can be intrinsically integrated in a 3D structure along with associated electronics (i.e., quench and recharge circuits), while being electrically insulated from each other, thanks to the BOX layer, illustrates the many advantages of this combination, especially an optimization of the FF.

2.2 SPAD implemented in CMOS FDSOI technology below the BOX

In order to design a SPAD in native FDSOI technology, two main layers were addressed to be used as the PN junction: P-well (PW) and DNW, as illustrated in

Fig. 2.5. The former is conventionally used for body-biasing effects, and the latter (also known as triple well, layer T3 in Physical Design Kit (PDK)), being biased through N-Well (NW), is normally employed for isolating two different PW [8]. As can be seen in Fig. 2.6 (a), the junction is vertically integrated under the BOX layer and is thus electrically isolated from transistors - implemented in the thin silicon film.

Since PW exists by default, and NW is more doped than DNW, PEB can occur between PW and NW. For avoiding this problem, BFMOAT PDK layer is introduced between them, preventing P or N implants in this area, as can be observed in the corresponding doping profiles shown in Fig. 2.6 (b) and (c) [12].

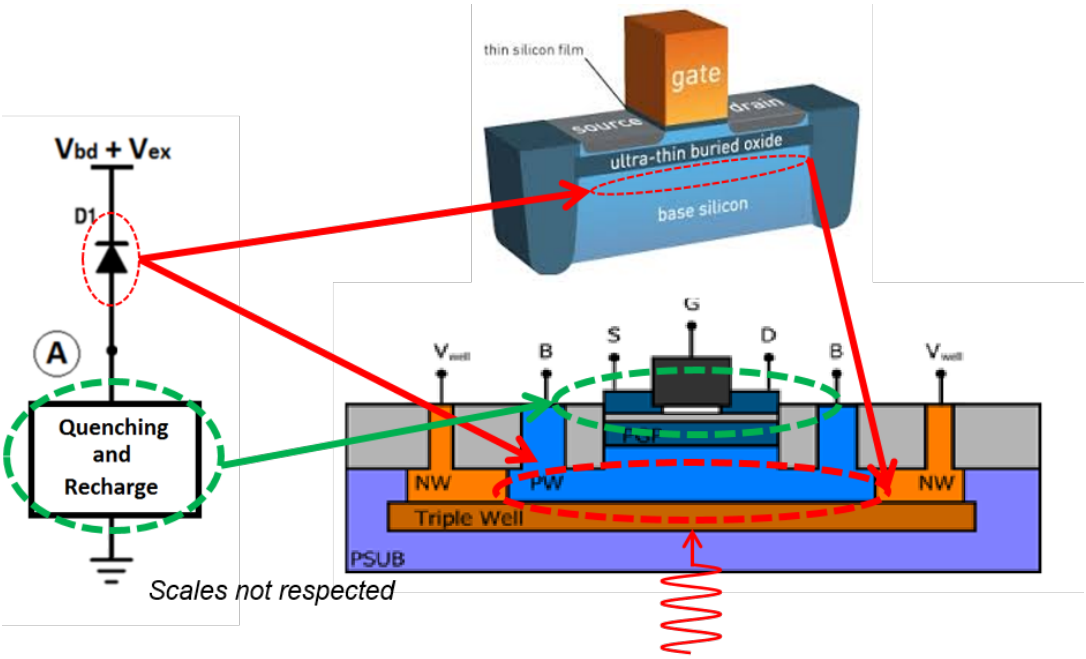

Figure 2.5: *Proposed implementation of SPAD in commercial C28FDSOI technology. The junction is realized under the BOX layer.*

Once the PN junction is formed, it is necessary to provide contacts for biasing cathode and anode. They can be done with BP and NW PDK layers, as illustrated in Fig. 2.6 and 2.7. The anode is then connected to a quenching circuit (either internal or external), which is, in turn, also connected to the ground potential. Cathode is biased at high voltage (V_{BD} + V_{ex}). The substrate contact can be connected to the ground potential too, as the DNW-SUB junction presents a much higher Breakdown voltage V_{BD} than PW-DNW, as measured in Chapter 4, section 4.1. This option of bias configuration was chosen considering the future implementation of a SPAD matrix, where a common DNW can be implemented for BSI, but also taking into account the body-biasing effect, expected to affect transistors placed over the PW, due to the variations in their voltage when avalanche occurs, as explained in Section 2.4.2.

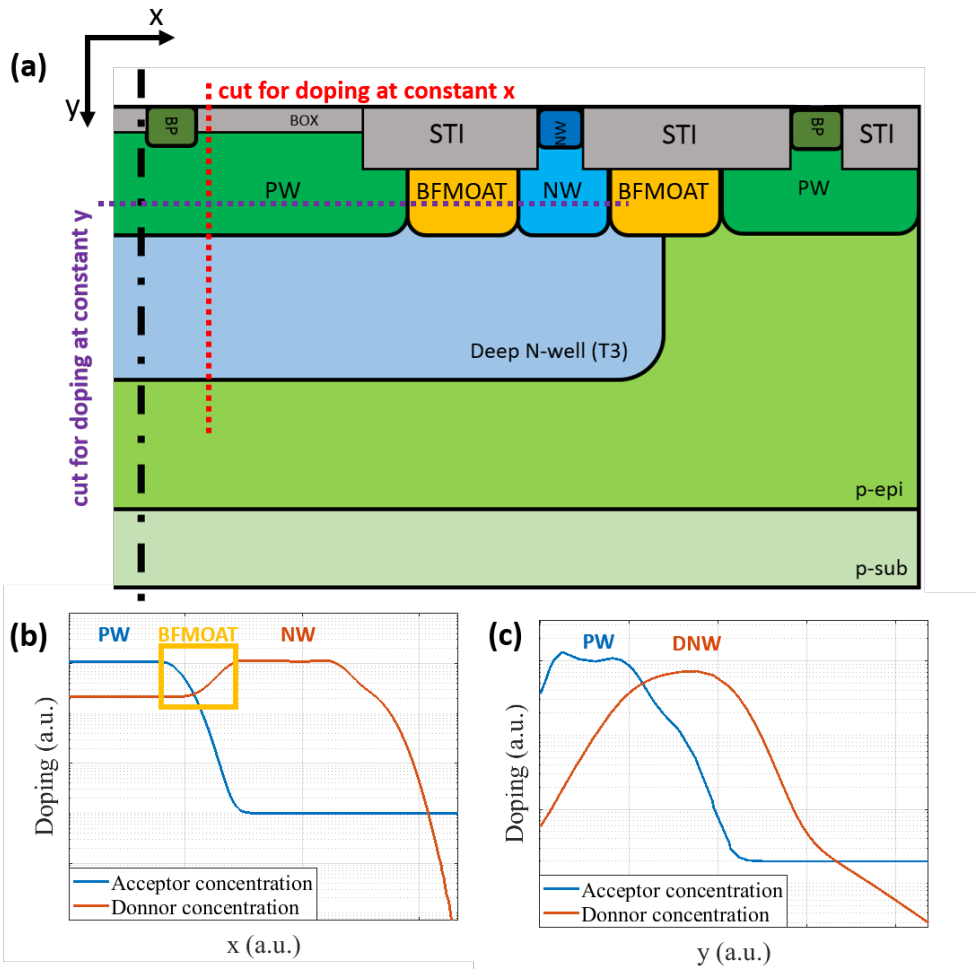

Figure 2.6: *(a) Cross section of SPAD vertically integrated in C28FDSOI (PW-DNW junction). Here, only half of the cell is represented, as it has cylindrical symmetry (scales not respected); (b) Doping profile at constant y, where BFMOAT layer plays the role of guard-ring; (c) Doping profile at constant x, where the SPAD junction is shown. Arbitrary units were used here for confidentiality reasons.*

2.3 Design Rules Constraints

For every IC design, minimum widths, areas and distances between layers are imposed by the technology rules, to make sure the proposed design is physically feasible. One of the major challenges in designing SPAD cells in commercial technologies is the respect of all design rules, sometimes very constraining.

First, a geometry needs to be chosen, which is particularly difficult in C28FDSOI technology, since only orthogonal shapes are allowed for almost all of the PDK layers (including T3 and BFMOAT). This feature makes it difficult to avoid PEB, since edges normally produce localized high electric field, which in turn produce a higher ATP on edges, not being an optimized feature for SPAD, where a uniform electric field is required for maximizing the Photon Detection Probability (PDP).

In order to overcome PEB, a BFMOAT PDK layer was introduced to the design

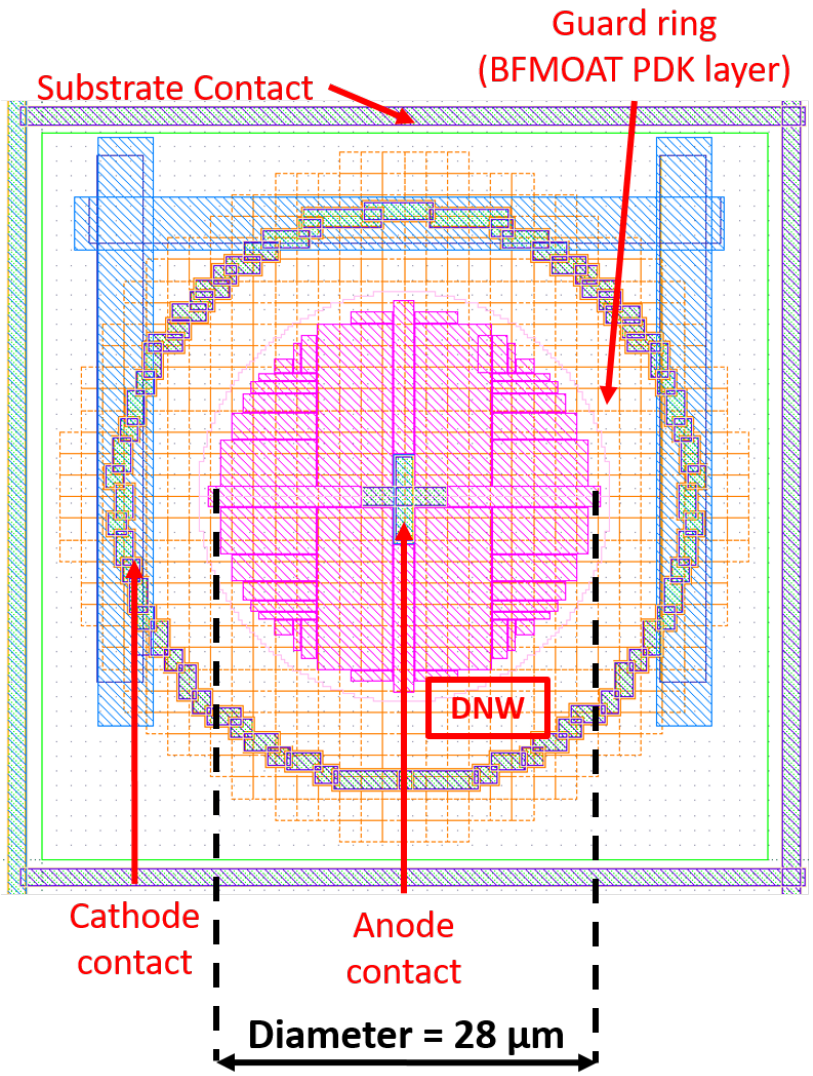

Figure 2.7: *Layout of a circular SPAD cell in C28FDSOI region with its main components. The purple rectangles correspond to the areas where BOX and thin silicon film are present (RX PDK layer), as STI is present by default. Since RX can only have rectangular shapes, due to design rules, the staircase approximation needed to be used here as well.*

between PW and DNW, playing the role of guard-ring, since it prevents P or N implants and creates a low doped region around PW (in this case, a N-type, retrograde from DNW implant), automatically reducing local electric field, as can be seen in Fig. 2.6 [12]. TCAD simulations including the electric field were performed and are presented in Chapter 3 to confirm the proper functioning of this guard ring in the structure.

In case of FSI, the photosensitive area needs special attention. In fact, several layers can attenuate or even block the incident luminous beam, such as metals used for contacts, dummies and also the passivation layer. In order to address these issues, contacts' sizes and shapes must be studied, to provide a uniform anode biasing without shadowing the photosensitive area, while still respecting design rules.

In C28FDSOI (version DP 1.0a, used here), eight different metal layers exist (two

of which are thick). For minimizing the light attenuation in FSI, a limited amount of metal was used, keeping the minimal widths and surfaces for all eight levels in the photosensitive area. The first level of metal (M1) was used for biasing the cathode at high voltage, and for decreasing the chance of breaking the dielectric between two consecutive metals, the last level (IB) was used to reach the anode contact.

Furthermore, according to PDK design rules, the NW contacts can have any shape, as long as they only have orthogonal angles. This feature ensures a very uniform biasing of the cathode. The PW contacts, on the other hand, can only have either a cross or a straight line shape, which limits the options of geometry for anode contact.

Advanced technologies such as C28FDSOI also require a flat wafer surface between each metal layer, normally done with Chemical Mechanical Polishing (CMP). In order to fulfill this specification, the so called "dummy tiles" are inserted during design phase to homogenize the density of each metal layer. They can, however, have a negative impact on photon detection if they cover the photosensitive surface. A tiling-exclusion layer must be used to avoid this problem, while respecting minimal and maximum density values for each PDK layer.

Passivation layer can also have an impact on photo-detection. Nevertheless, due to fabrication process issues, it may not be possible to exclude this layer, which was the case for C28FDSOI. The imposed attenuation must then be taken into account while analyzing PDP.

One last aspect that needs close attention in the case of C28FDSOI is the STI that is by default everywhere in the circuit. In order to produce the true SPAD FDSOI, RX PDK layer must be used. It replaces STI by the BOX physical layer (25 nm), right below the thin silicon film (7 nm).

2.4 Description of Cells

2.4.1 SPAD Cells

In order to provide an optimized SPAD in FDSOI, during the device conceiving phase, several design parameters were varied and their influence in SPAD performance were analyzed. In particular: geometry, guard distance, cell size and associated quenching circuit, as well as the implementation in different zones (under BOX, under STI or even in a No SOI (NOSO) area - see Fig. 2.8 and 2.9).

The NOSO region, also known as the HYBRID zone, is obtained by etching the silicon film and BOX from FDSOI zones (right after well doping) and was introduced in order to allow the co-integration of bulk and SOI devices on the same die, since the equivalent 28 nm bulk technology already existed [8]. In order to obtain such a region, a combination of RX and HYBRID PDK layers must be provided.

The integration in different zones is essential for understanding the influence of each layer in SPAD performances. For instance, due to design rules constraints, STI is kept at the edges of the photosensitive surface in SPAD integrated under BOX. Since there is a significant difference in their oxide thickness (see Fig. 2.10), for a fixed depth, the implants go through a thicker layer of silicon oxide in STI region before reaching the silicon itself. These processes result in different doping profiles, which in turn imply in distinct SPAD performances, as will be explained in Sections 3.1.2 and 4.5.

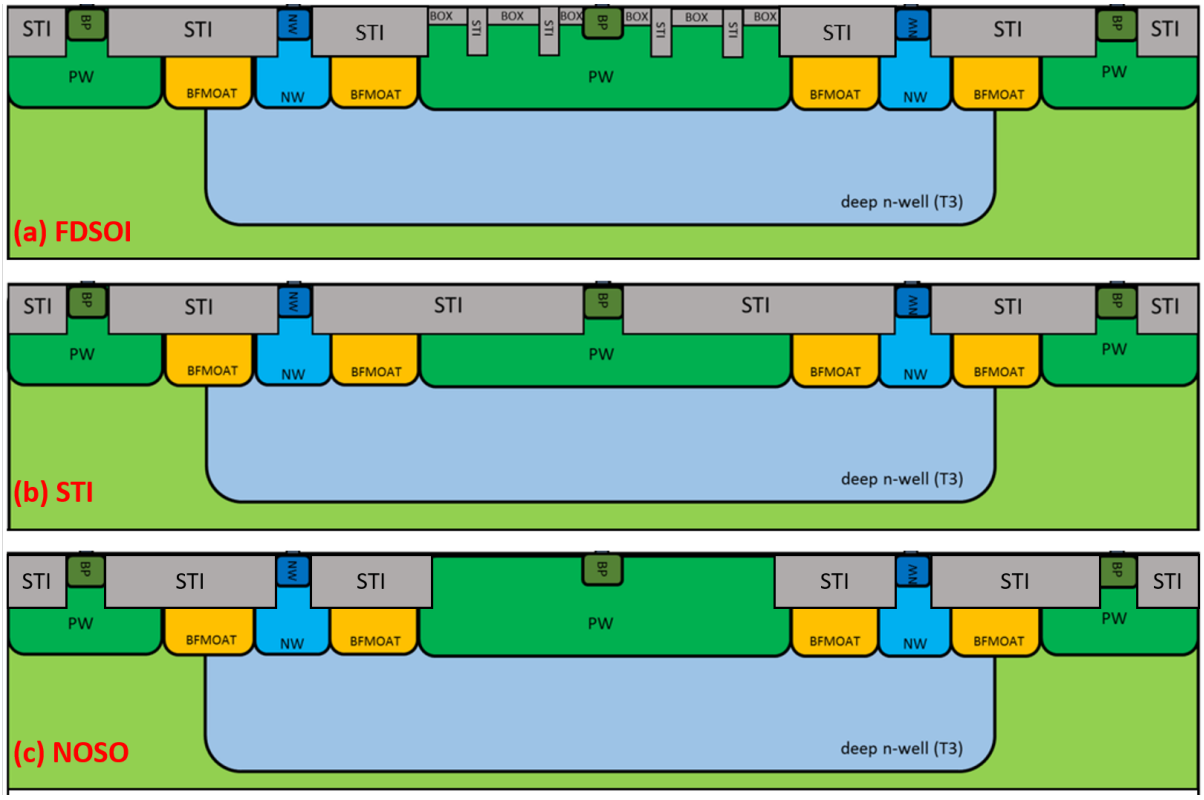

Figure 2.8: *Cross section of the three different regions available in C28FDSOI in which the SPAD can be implemented: (a) FDSOI; (b) STI; (c) NOSO*

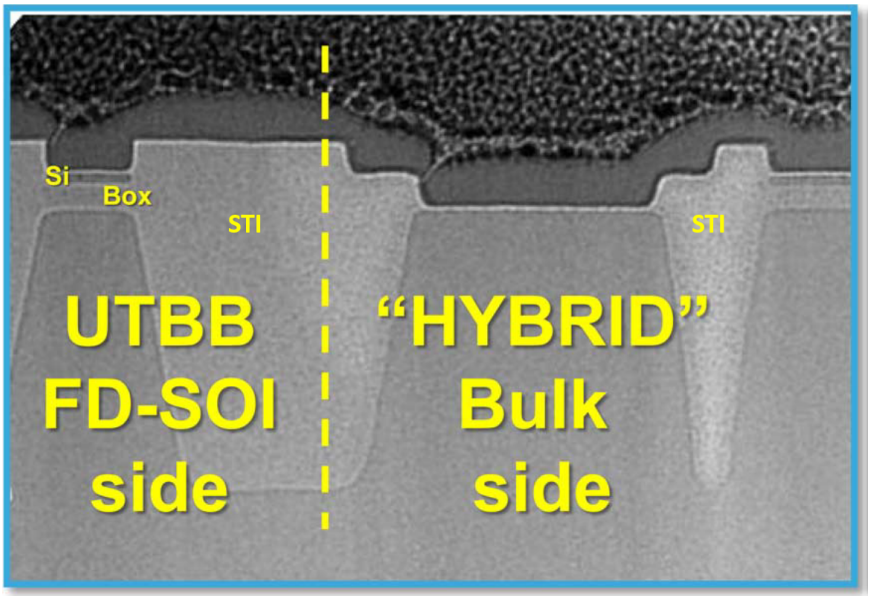

Figure 2.9: *Microscopic picture of the three different zones available in C28FDSOI: FDSOI, STI and NOSO (adapted from [8]).*

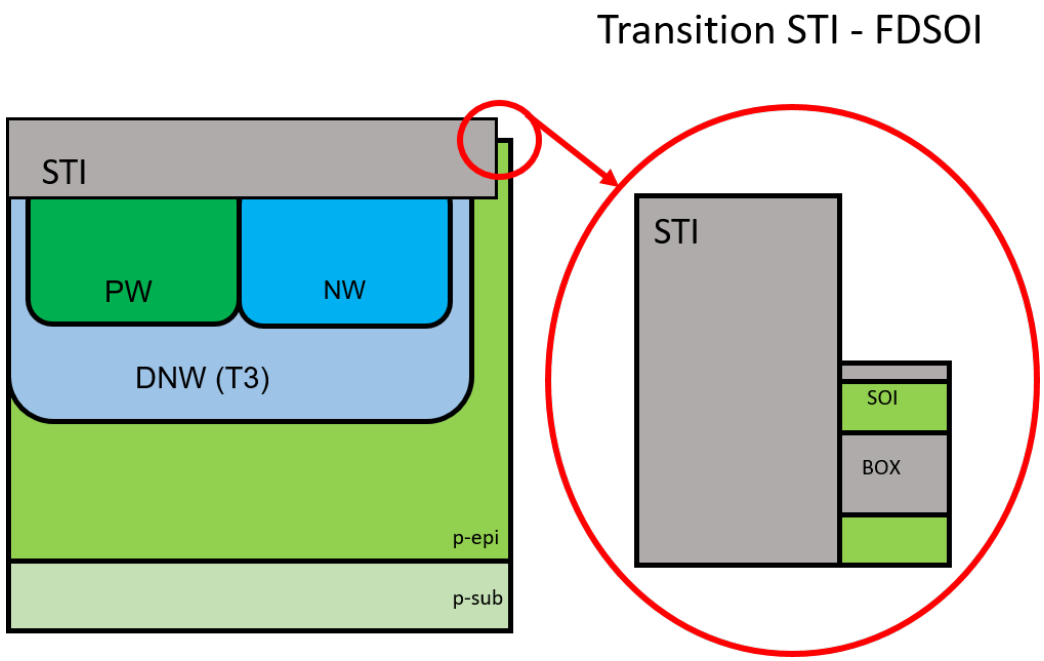

Figure 2.10: *Transition of a STI zone into a FDSOI. The difference in the material through which the doping processes are done influence SPAD performance.*

Concerning geometry, three main shapes were conceived: squared, octagonal-like and staircase-approximation circular cell, as can be seen in Fig. 2.11. Due to design rules constraints, all cells had staircase approximation geometries, since only orthogonal shapes are allowed in the commercial technology. The main objective here is to verify the influence of the geometry in breakdown process, including edge effects.

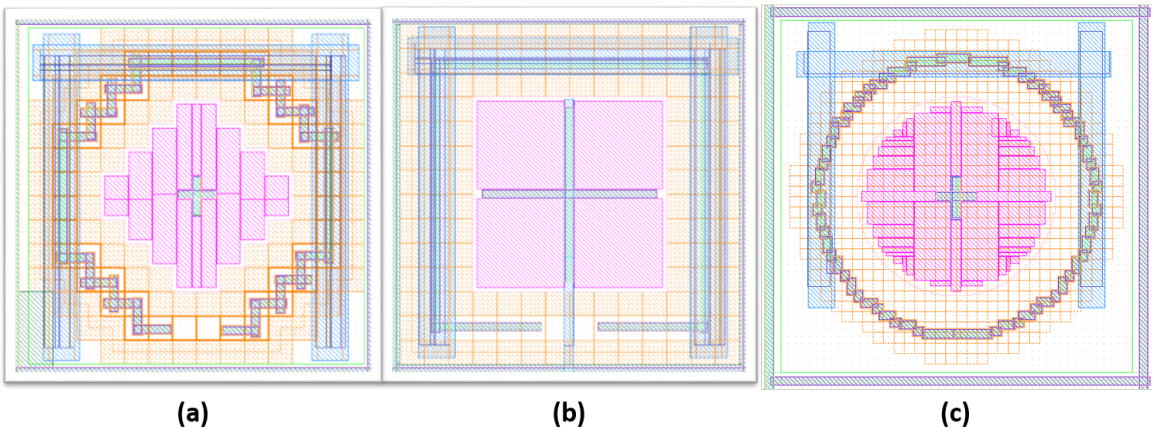

Figure 2.11: *Three different SPAD geometries were implemented: (a) octagonal; (b) squared; (c) circular. All cells were designed with staircase approximation, due to design rules requirements.*

Guard distance is defined here as the width of the BFMOAT PDK layer, used to isolate PW from NW, avoiding PEB. Two values were used: 3.5 µm or 5.0 µm. By varying

this distance, one can expect to find the optimized guard distance. TCAD simulation is often not enough to accurately determine this value, due to high incertitude while simulating doping profiles.

Cell size was another parameter taken into account. Five different dimensions were used for the photosensitive area: for octagonal cells, 500 μm^2 and 1000 μm^2. For squared cells, 785 μm^2. For circular cells, 615 μm^2 and 2460 μm^2. This parameter is quite important when measuring dark current in such devices, since it is quite difficult to measure currents smaller than 100 fA, which is often the case for smaller cells. For comparison reasons, some cells were developed under STI and also in NOSO areas (out of FDSOI zone), while keeping constant the other parameters.

PQC were also implemented: either a high precision p+ polysilicon resistor (200 kΩ) or a single transistor, placed next to the diode. Passive circuits have the advantages of not taking much place in the circuit, have reduced power consumption and no need for much interconnection, being suited for initial characterization and selection of devices [13]. For both passive components, the adopted configuration was the diode on top, i.e. the PQC is connected to the anode of the SPAD, while the cathode is biased at high voltage, as shown in Fig. 2.12. This choice is particularly interesting for FDSOI, because the anode voltage is by default at ground potential, varying only during avalanche events, which can be properly exploited in sensing circuits placed over BOX layer, due to body-biasing effects.

2.4.2 Indirect Avalanche Sensing Cells

One of the main features in C28FDSOI is the body-biasing effect in transistors. This intrinsic characteristic can be conveniently explored for SPAD cells, i.e., during avalanche events, transistors placed over SPAD cells may have their threshold voltage varied, allowing to indirectly detect avalanche events. This possibility has been previously proposed in [14] and was implemented here, with a simple voltage divider circuit, as shown in Fig. 2.13 and Fig. 2.14.

Since both transistors are placed over the same P-well (i.e., the SPAD anode), a RVT NMOS and a LVT PMOS were used. Two types of transistors were employed (for two independent sensing cells): regular gate oxide (referred as GO1, 18 Å) and thick front gate oxide (GO2, 28 Å, also called Extended Gate (EG) transistors), featuring a larger body-bias factor ($\Delta V_{th}/\Delta V_{bb}$).

The output node of the voltage divider V_{out} varies dynamically with the SPAD state. Each avalanche event gives a positive transient voltage pulse on the anode, i.e., a PW voltage increase. Then, $V_{th,n}$ of NMOS will decrease (forward body-biasing) while the absolute value $|V_{th,p}|$ of PMOS will increase (reverse body-biasing). A transient negative voltage spike is then expected at the output node (V_{out}) of the voltage divider.

Both PMOS and NMOS have W = 10 μm and L = 150 nm as size parameters, for both EG and thin gate oxide families. This very simple sensing circuit for direct measure with oscilloscope is certainly not optimized, as it presents a high power consumption (hundreds of μW), but surely can be used as a proof of concept, as shown in Chapter 4, Section 4.8.

Another very simple and yet effective circuit for indirect sensing of avalanche is presented in Fig. 2.15, where a single transistor is placed over the SPAD and has its source

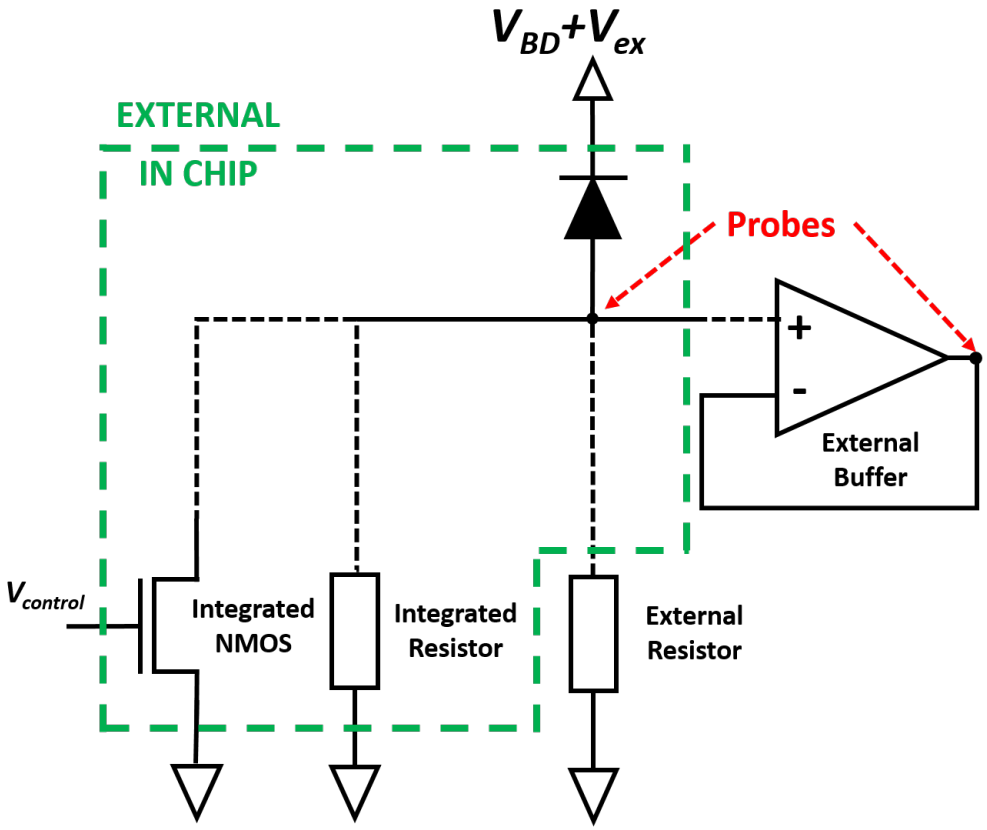

Figure 2.12: *Schematics of SPAD and its quenching circuits, connected through anode. Cathode is biased at breakdown + excess voltage. Black dotted lines represent the possible connections with three distinct and independent quenching circuits. Red dotted lines represent the two possible nodes to which the oscilloscope probes can be connected. The green dotted line symbolizes the interface between internal and external circuitry*

and drain connected to each other, as an output node. Its working principle is based on the two intrinsic capacitances presented in the structure (gate - gate oxide - channel and channel - BOX - PW). This architecture can be translated into an equivalent capacitor-based voltage divider, where a variation in anode voltage, during avalanche, is enough to change the voltage at the channel, producing an output voltage pic, synchronized with avalanche events. The consumption for this configuration is negligible, but in order to verify this effect, a larger transistor is needed (almost 3 times bigger than the ones required for the first proposed sensing circuit). Also, since the capacitive divider cannot drive a load, a buffer circuit is needed, and its power consumption should also be taken into account. This cell was only tested by means of SPECTRE simulation, in Cadence Virtuoso software [15].

2.4.3 Antenna Diodes

During IC fabrication for regular bulk CMOS devices, the gate oxide in transistors connected to a large path of metal layer can be damaged, due to the so-called Antenna

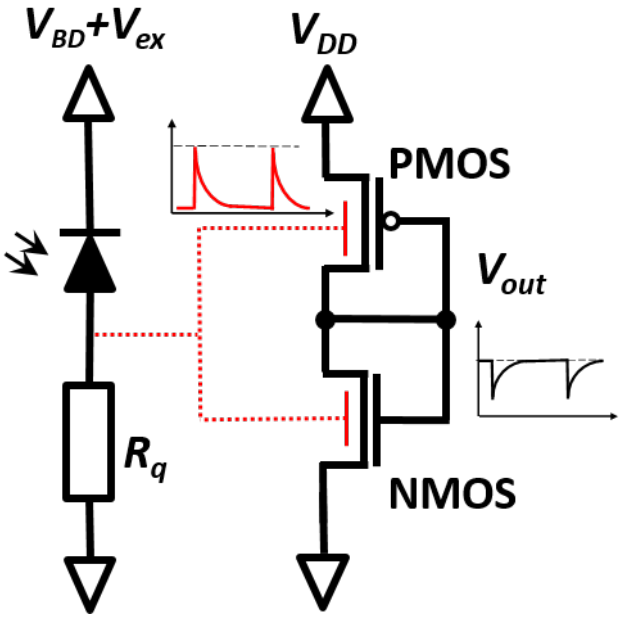

Figure 2.13: *Schematics of sensing circuit, composed by a RVT NMOS and a LVT PMOS, in a voltage divider configuration, where the output voltage varies with avalanche events, thanks to body biasing effect.*

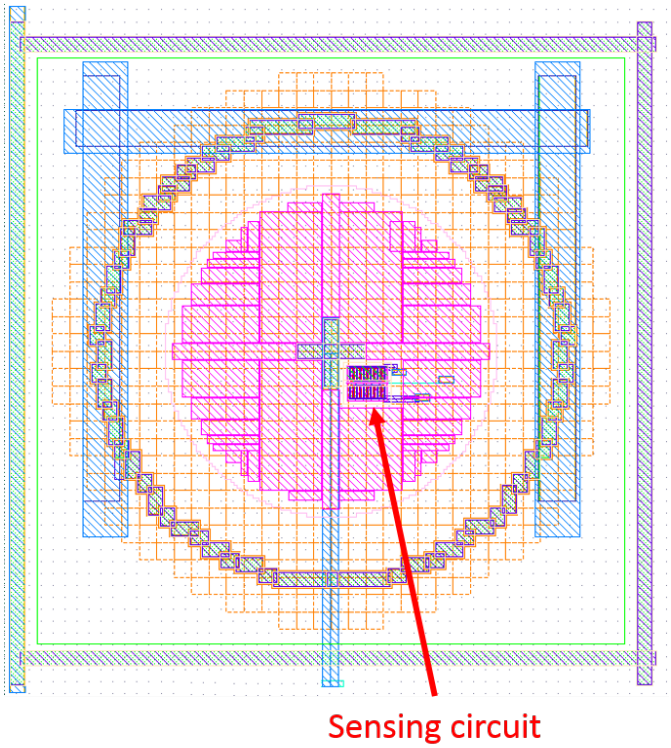

Figure 2.14: *Layout of SPAD circular cell with sensing circuit over PW, in the middle.*

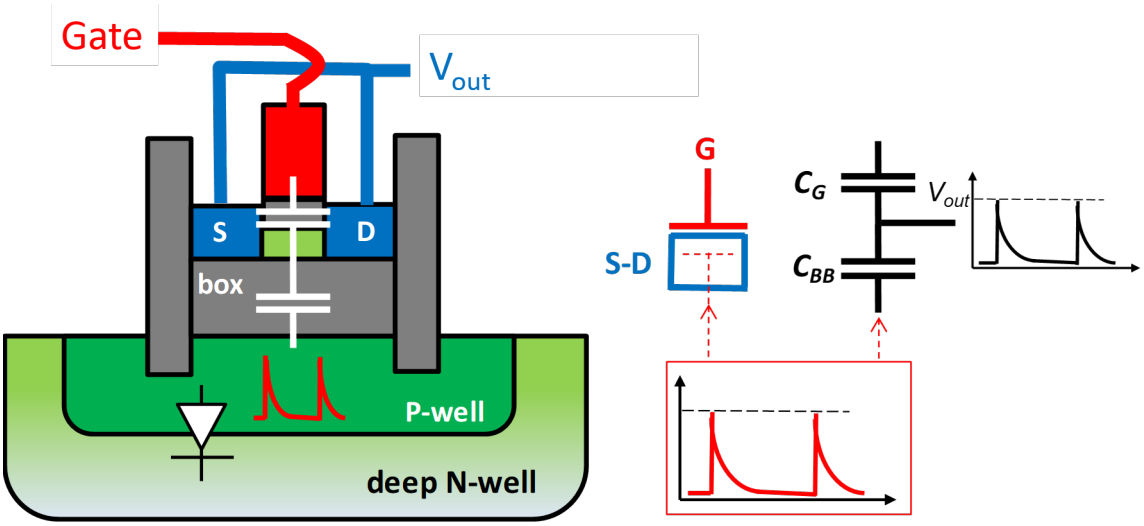

Figure 2.15: *Another proposed architecture of sensing circuit in FDSOI, thanks to body biasing, based on a capacitive divider (Scales not respected) [15].*

Effect or Plasma Induced Damage (PID). This phenomenon consists of collecting charges in gate layer during plasma etching, for instance. These charges can produce an unwanted DC current flow through thin gate oxides, making the affected transistors useless [16]–[18].

In C28FDSOI, this problem is even more disturbing, because source and drain are also isolated from substrate by BOX layer, and thus exposed to plasma damage. For this reason, additional antenna design rules are added to FDSOI process, to avoid this problem [19], [20].

The simplest solution for both bulk and C28FDSOI, is to place an "antenna diode" between the first metal layer (M1) and the substrate. Once the charges are collected in the transistors' terminals, they are sufficient to break these antenna diodes, evacuating the charges into substrate and thus avoiding damaging both BOX and gate oxide, preserving then the device for its correct utilization. It should be noted that Design Rule Checking (DRC) predict the correct diode surface, according to metal path surface, for evading this problem.

In the specific case of SPAD integrated in C28FDSOI, the correct placement of these protective diodes is crucial, since they may damage SPAD device, as illustrated in Fig. 2.16. Most of the time, such antenna diodes are placed close to the connected transistor, and this does not constitute a problem when DNW is used for the only purpose of isolating different PW, which is not at all the case for SPAD, where they compose the PN junction biased above breakdown. An easy but effective solution is to move them to another PW that is not used for SPAD purposes, as can be seen in Fig. 2.17. In the implemented test chips, the misplacement of such antenna diodes was the reason for the malfunctioning of some SPAD cells. These errors were corrected in an updated version of the test chip, currently under fabrication.

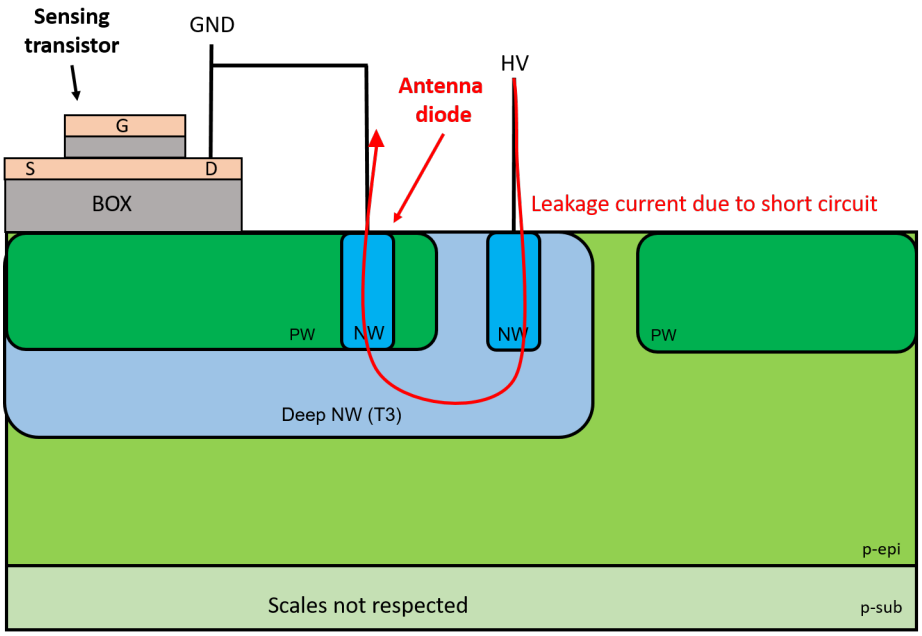

Figure 2.16: *Leakage current due to misplacement of protective antenna diode, in the surroundings of SPAD integrated in C28FDSOI.*

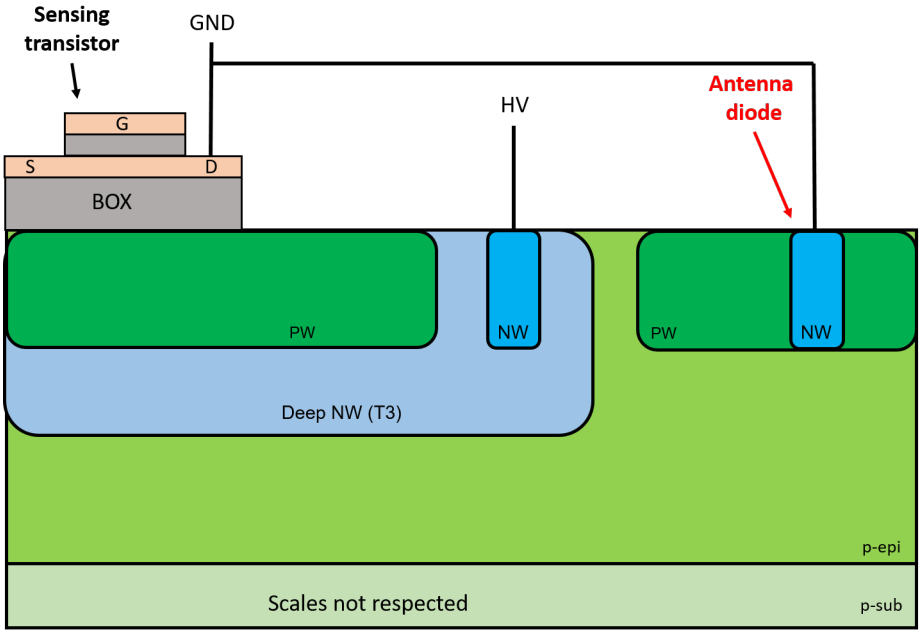

Figure 2.17: *By placing the protective antenna diode in an isolated PW, no leakage current is produced in SPAD.*

2.5 Circuit Top Layout

The final layout, sent to fabrication by means of Multi-Project Circuit (CMP), is presented in Fig. 2.18. It is composed of 8 SPAD cells designed for probe station tests (in

red squares) and 12 other for PCB tests (in purple squares). Those last are connected to a custom padring composed of cells from C28SOI_IO_EXT_ANAF_EG library provided in the PDK. Adaptations were needed especially in the superior pads, used for high voltage biasing, where the native overvoltage protection needed to be suppressed. Since thick oxide transistors were used for some of the sensing cells, the so-called EG pads were needed, allowing biasing voltages up to 1.8 V, contrary to the thin gate oxide, where maximum voltage is limited to 1.0 V. One pad with this last configuration was needed for biasing an integrated buffer in the circuit. A photo of the received fabricated circuit is shown in Fig. 2.19.

A dedicated PCB was also implemented for testing the dynamic behavior of the SPAD cells. It is illustrated in Fig. 2.20. A mechanical switch was placed in order to select which SPAD cell is connected to the high voltage. Several SMB connectors (with their respective decoupling capacitors) allow to bias the padring, the sensing cells and also to provide the input signal to transistor-based quenching circuit. Finally, some pins allow the signals to be read by an oscilloscope, for a direct waveform analysis.

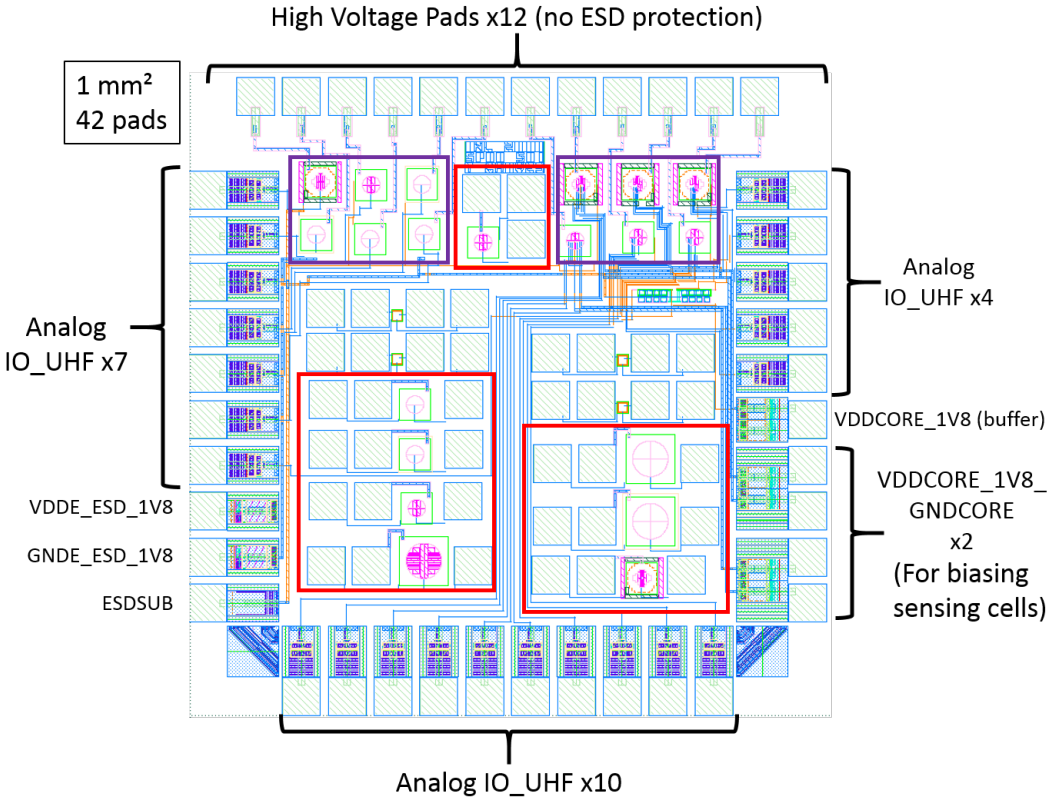

Figure 2.18: *Final layout.*

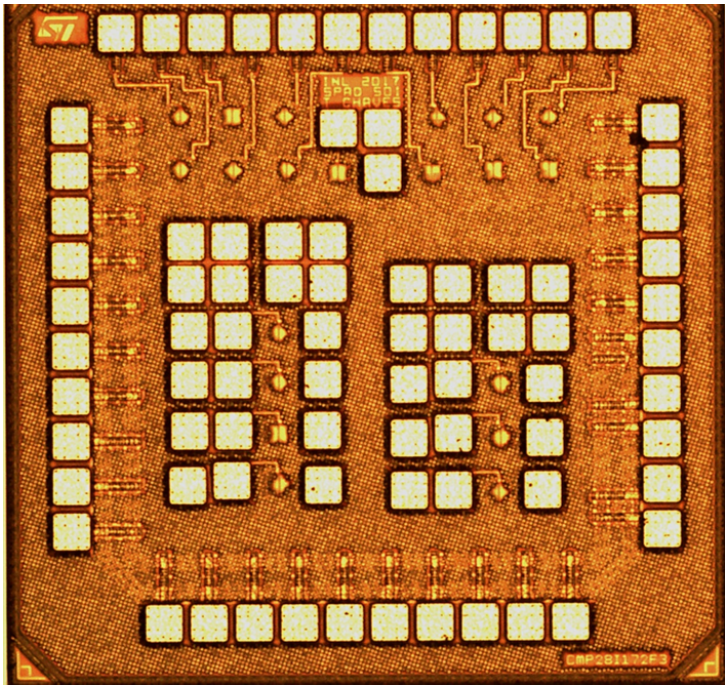

Figure 2.19: *Microscopic photograph of fabricated circuit.*

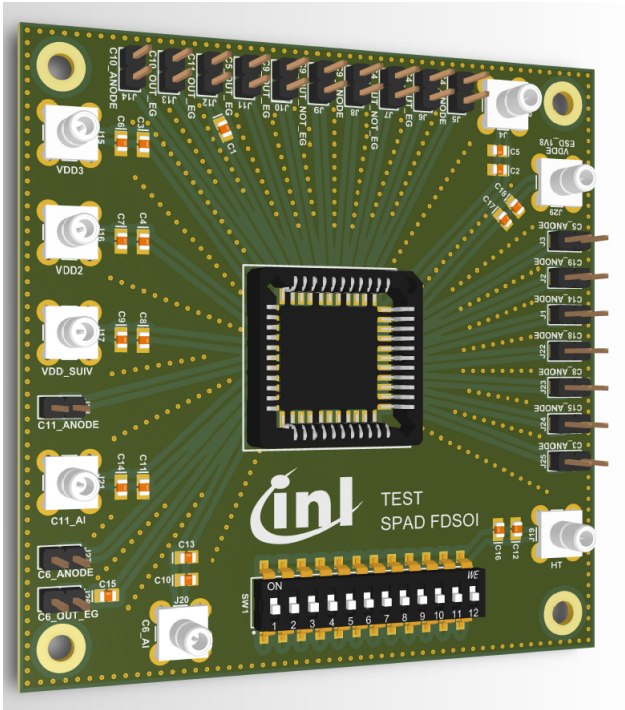

Figure 2.20: *Printed Circuit Board used for testing SPAD cells.*

Conclusions

In this chapter, the proposed implementation of SPAD cells in C28FDSOI was presented. Firstly, the technology was discussed with its main advantages, such as great suitability for low voltage operation, proving to be one of the most well adapted technologies for future applications, where circuit performance and energy efficiency are the top priority.

To the best of our knowledge, this is the very first time SPAD devices are integrated in advanced C28FDSOI, the main advantage of such an achievement being the possibility of obtaining an intrinsic 3D structure with Fill Factor (FF) optimization, without the need of expensive and complicated 3D assembly techniques currently used in State of the Art, where two dies are connected together: one with the sensor and the other one with the associated electronics.

In the case of the proposed integration, the PN junction operating in Geiger mode is located under the Buried Oxide (BOX) layer and is thus electrically isolated from the transistors, that stay on top. Then, they can be used for composing the associated circuits for the correct operation of the SPAD, such as quenching, recharging and addressing, in the case of a matrix implementation.

Concerning the design of the SPAD cells, several parameters were varied in order to verify the influence of each one in their performance. Many problems were faced due to design rules constraints, such as mandatory orthogonal shapes, antenna diodes design and adaptation of padrings. Nevertheless, even if limited circuit surface was available (1 mm^2) for each test chip, a quite fair amount of variants could be implemented (and most of them could also be tested), as a proof of concept of SPAD in C28FDSOI: two guard distances, three geometries, three possible quenching circuits, five different values of photosensitive areas and three different integration zones: FDSOI, STI and NOSO.

Two indirect avalanche sensing cells were also proposed, based on the capacitive coupling provided by body-biasing effect feature in C28FDSOI. In the first one, a transistor-based voltage divider has its output voltage varying when avalanche events occur. Such indirect sensing supports the use of larger excess voltage, as compared to direct approaches and paves the way for simpler and innovative SPAD processing electronics.

The characteristic of the proposed cells are verified by means of TCAD simulation in Chapter 3, such as electric field distribution and by means of electrical characterization in Chapter 4.

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Chapter 3

TCAD Simulation and Modeling

In this chapter, the work of simulation, post-processing and modeling performed during this PhD, in order to investigate the expected performances of FDSOI SPAD devices, is presented. This chapter is organized as follows: first, the simulation software, its approximations and the used procedures are presented and discussed. Then, the ionization coefficients models, used for avalanche triggering probability calculation, are reviewed. Later, the main mechanisms of carrier generation that can effectively start off avalanche process are discussed. Post-processing analysis is also introduced, allowing to estimate DCR and PDP. At last, an approximated analytical version of McIntyre's calculation of Avalanche Triggering Probability is proposed, which can be used in compact modeling.

3.1 Structure Definition for Electrical Simulation

In this section, the procedure used to represent by simulation the SPAD implemented in FDSOI is presented. This procedure includes two steps: geometry definition and doping determination.

3.1.1 Geometry

In order to create a simulation structure that fulfills all design rules requirements, imposed by the technology, Synopsys Sentaurus™ Structure Editor (SDE) tool was used. It is essentially a two-dimensional (2D) and three-dimensional (3D) device structure editor, and a 2D/3D process simulator [1]. The device structure created in SDE is presented in Fig. 3.1. It represents half of cross-section of the designed SPAD sent to fabrication. A cylindrical symmetry is then considered, having the position $x = 0$ as the symmetry axis. It means that a 3D device is specified by a 2D mesh and the axis around which the device is rotated [2]. This feature allows a much faster simulation and a quite fair approximation of the real designed SPAD.

3.1.2 Doping

l In order to have more accuracy when simulating doping profiles, an implantation process was simulated in 1D, using energy and dose data provided by foundry. Those

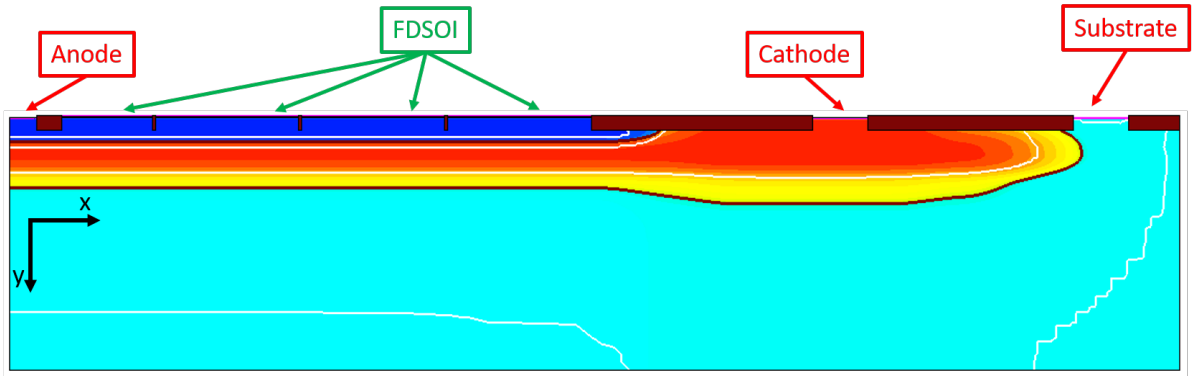

Figure 3.1: *Half cross section of designed SPAD, simulated in TCAD.*

doping profiles were then imported into the SDE structure. Since SPAD intrinsic characteristics are highly dependent on the doping of the junction, they need to be precisely simulated in order to have a reliable model.

In Fig. 3.1, the dark blue area corresponds to the P-well (PW), while red areas represent Deep N-well (DNW) and N-Well (NW). Shallow Trench Isolation (STI) is present between FDSOI areas, on top of PW, due to the previously discussed design constraints (cf. Section 2.4). Due to confidentiality reasons, doping and depth are indicated only in arbitrary units. In dark red, SiO_2 areas are represented, for both BOX and STI physical layers.

TCAD Application: Impact of the Deep N-well Implants

When characterizing the fabricated devices, some differences between structures implemented under BOX and STI layers have been noticed, especially in breakdown voltage and electroluminescence tests, where STI cells have a slightly lower V_{BD} and a much more homogeneous electric field distribution (Sections 4.1 and 4.5). By observing this behavior, some extra TCAD simulations were conducted in order to investigate the influence of the aforementioned layers in the structure.

In fact, all the implants for PW, NW and DNW are done through either BOX + Silicon film or STI layers. Since the thickness of each is very different (STI layer is more than ten times thicker than BOX), the layer through which the implants have been done can significantly change the resulting doping of the junction.

Process simulation was performed in 1D, with the default implantation analytical model (simple Gaussian function) and default annealing model (constant diffusion model). No model customization was used. The results of these simulations can be observed in Fig. 3.2.

These simulation results explain the difference between the two regions, the one implemented under STI been slightly more abrupt. Although the doping difference seems small, it is large enough to provide a lower breakdown voltage and a higher B2B generation rate, as explained later in Chapter 4.

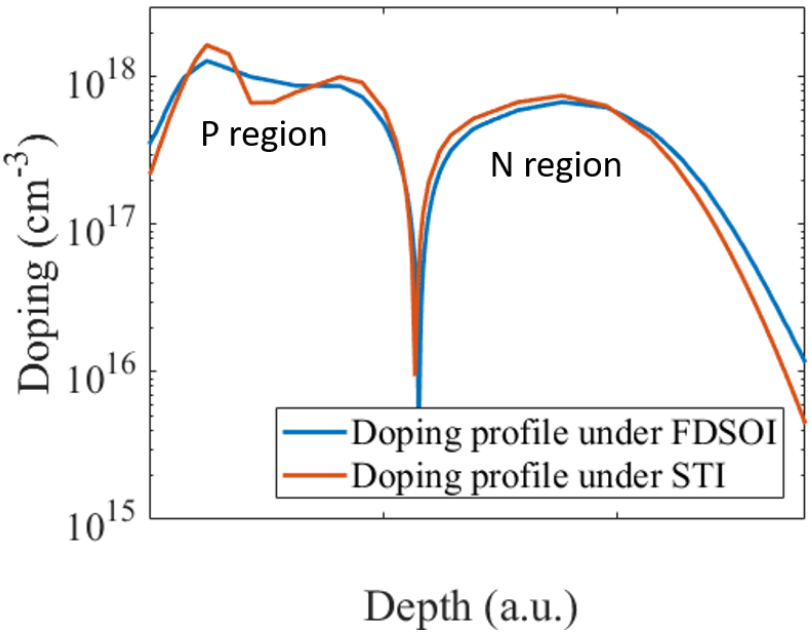

Figure 3.2: *Net doping profiles provided by 1D SPROCESS Simulation, for two different regions: under FDSOI and under STI.*

Proposition of a Modified Deep N-well

First, the chips were fabricated with the native commercial technology, where, for DNW, two implants are made. The electrical characterization of these devices is presented in Chapter 4, where it is possible to verify that the doping levels are too high and that the native junction is too abrupt ($V_{BD} \approx 10\,V$). The fabricated device is then not optimized to be used in Geiger mode, since breakdown voltage is low and B2B and Trap Assisted Tunneling (TAT) are not negligible. In agreement with the foundry, a TCAD study was conducted in order to verify the possibility of improving the junction (without affecting its original role of isolating different PW), by changing its implants for a special dedicated wafer.

For confidentiality reasons, the data about the implants, as energy and dose, as well as junction depth cannot be disclosed. In order to obtain the original DNW, two implants are normally performed. For obtaining a smoother PN junction and thus a higher breakdown voltage, a parametric optimization was carried out based on a single implantation step for the DNW, without changing the native implants for PW and NW. This single proposed implantation should be done at 25% higher energy and 30% lower dose, as compared to the value at second implant used in original process.

Original and optimized net-doping profiles are shown in Fig. 3.3. For the modified version, the metallurgical junction is shifted at greater depth, and the optimized deep N-well is about three times less doped than the original one. It results in a smoother junction, with a breakdown voltage increase of about 65%, as experimentally verified in Chapter 4. For the following sections of this chapter, the simulation results will be presented for both original and modified DNW versions of the simulated SPAD.

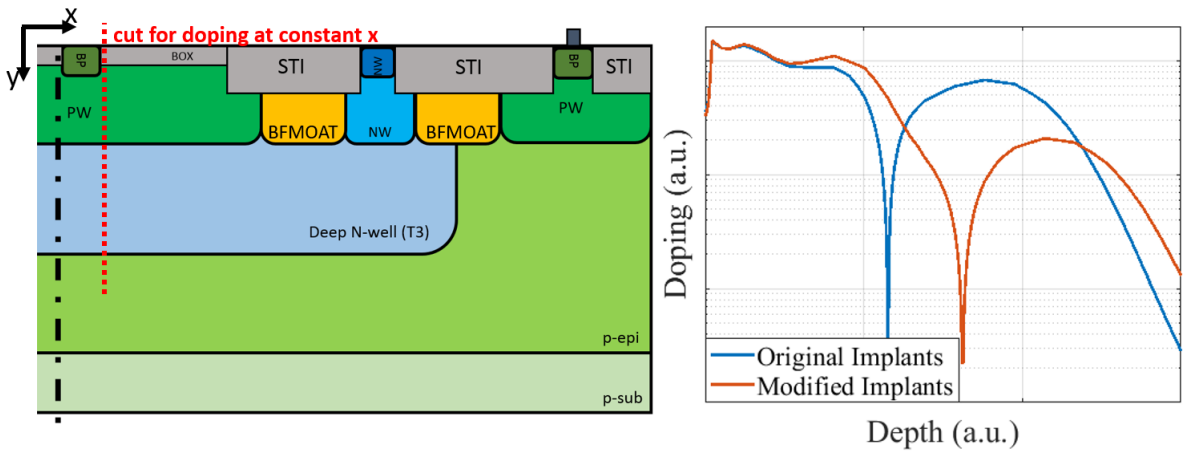

Figure 3.3: *Net doping concentration according to depth for both versions of DNW*

3.2 Electrical Simulations: Physics and Models

In order to model the SPAD device, several physical effects need to be properly accounted, and in particular: carrier transport, carrier generation by light, impact ionization, traps and band to band tunneling. Several models are available in SDEVICE TCAD tool from Synopsys Sentaurus [1] and needed to be carefully selected for a correct description of the actual fabricated device.

3.2.1 Carrier Transport

The classical drift-diffusion model was used for estimating carrier transport in all simulated devices. The drift component is created by the electric field, and the diffusion component is caused by the carrier-concentration gradient. The current density for electrons and holes are described by Equations 3.1 and 3.2, respectively [3], [4].

$$\vec{J_n} = e\mu_n n\vec{E} + eD_n\vec{\nabla}n \tag{3.1}$$

$$\vec{J_p} = e\mu_p p\vec{E} - eD_p\vec{\nabla}p \tag{3.2}$$

where:
$e = 1.6 \times 10^{-19}$ C is the elementary charge
$\vec{E}$ is the electric field

Also, respectively for electron and holes:

$\vec{J_n}$ and $\vec{J_p}$ are their current densities
μ_n and μ_p are their mobilities
n and p are their densities
D_n and D_p are their diffusion constants
$\vec{\nabla}n$ and $\vec{\nabla}p$ are their concentration gradient

Considering that the semiconductor used here are moderately doped and thus non-degenerate, diffusion constants can be expressed by the Einstein relation (Eq. 3.3), the current densities can be re-written as in Eq. 3.4 and 3.5.

$$D = \frac{kT}{e}\mu \tag{3.3}$$

$$\vec{J_n} = -ne\mu_n\vec{\nabla}\Phi n \tag{3.4}$$

$$\vec{J_p} = -pe\mu_p\vec{\nabla}\Phi p \tag{3.5}$$

where :
Φ_n and Φ_p are the electron and hole quasi-Fermi potentials, respectively.

Also, the electrostatic potential in the structure is calculated from Poisson's equation (3.6). The electric field is related to the electric potential by a gradient relationship (3.7).

$$\text{div}\,\vec{E} = \frac{\rho}{\varepsilon} \tag{3.6}$$

$$\vec{E} = -\nabla\vec{V} \tag{3.7}$$

where:
ρ is the charge density, including ionized dopants and free carriers (electrons and holes), and
ε is the material permittivity.

Drift Diffusion simulations (a low field approximation of the more exact Boltzmann Transport Equation) is known to suffer from several limitations. Indeed, it does not properly describe the transport of hot electrons and holes. Secondly, it is a local approximation: for instance, impact ionization coefficients only depend of the local field, and not of the carrier trajectory history in a not constant field profile. Thirdly, the description of trap and band to band tunneling is not only local, but also simplified, using empirical models. A more accurate physical description of electrons and holes transport in SPAD device would require the solution of the Boltzmann Transport Equation for both carriers, including full band description, scattering with phonons, impact ionization mechanism, etc. (See [5] for details). If this physics has been extensively investigated in the field of MOS transistors and NOR nonvolatile memory recently, little has been done in SPAD device so far. Moreover, these models are not completely available in commercial TCAD tools, and are consequently out of the scope of this thesis.

3.2.2 Ionization Coefficients and Avalanche Generation

The avalanche process is caused by the ionization impact phenomenon, in which, from a certain threshold value of electric field (and, thus, carrier kinetic energy), one free carrier can generate several others, as shown in Fig. 3.4. In (1), a free electron-hole pair is created (here, due to thermal generation).The electron is then accelerated in (2) due

to the high electric field to finally have, in (3), enough kinetic energy to create another electron-hole pair, due to impact. Since the original electron loses some energy due to this impact, it is found at a lower level of the conduction band [4]. If the multiplication region is longer enough, this process can go on, in a self-sustained avalanche mechanism. The electron-hole pair generation rate G_{II} from impact ionization is given by Eq. 3.8 [3].

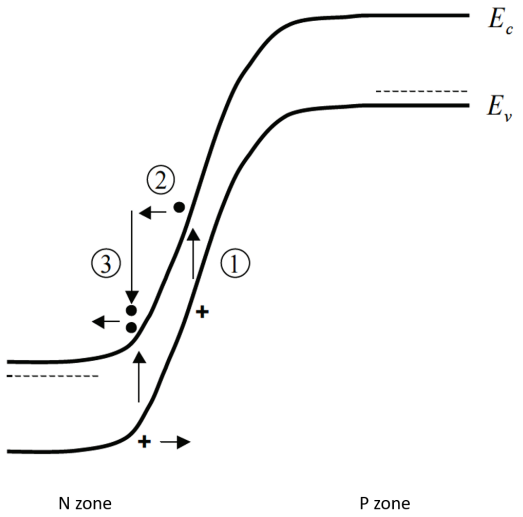

Figure 3.4: *Impact Ionization process, caused by electron. In (1), an Electron Hole Pair (EHP) is generated. The electron is accelerated in (2) and creates another EHP in (3), due to impact ionization. Adapted from [4]*

$$G_{II} = \alpha_n n v_n + \alpha_p p v_p \tag{3.8}$$

where, respectively for electrons and holes:
α_n and α_p are the ionization coefficients.
v_n and v_p are the velocities.

Physically, the ionization coefficients α_e and α_h represent the number of electron-hole pairs per unit distance traveled generated by electrons and holes, respectively, and are usually expressed in cm^{-1}. These coefficients are critical parameters for the correct simulation of avalanche process. For SPAD, they have a direct influence on reverse I-V curve characteristics, breakdown voltage and avalanche triggering probability.

Several models exist in TCAD simulation softwares. Each can be more or less adapted to the considered simulated structure, according to material, temperature, and electric field magnitude. Most of them are based on Chynoweth's model (Eq. 3.9) [6]. For all of the models, the coefficients presented in the equations (a and b for Chynoweth's) were calibrated empirically in order to fit experimental data, obtained with different devices. The main models studied here are: van Overstraeten-de Man, Okuto-Crowell and two versions of the University of Bologna model.

$$\alpha(E) = a \exp\left(-\frac{b}{E}\right) \tag{3.9}$$

van Overstraeten - de Man Model

The van Overstraeten model, expressed by Eq. 3.10, is similar to Chynoweth's, but introduce the factor γ, which takes into account the optical phonon energy, responsible for representing temperature dependency of the ionization coefficients. The value of the parameters used in this model make it valid over a range of fields from 1.75×10^5 V/cm to 6×10^5 V/cm [7].

$$\alpha(E) = \gamma a \exp\left(-\frac{\gamma b}{E}\right) \tag{3.10}$$

Okuto-Crowell Model

The empirical model developed by Okuto and Crowell [8] follows the dependency described in Eq. 3.11, where $T_0 = 300\ K$. The values by default for this model's coefficients are fixed for silicon. They are tuned for large electric fields varying from 1×10^5 to 1×10^6 V/cm.

$$\alpha(E) = a\left(1 + c(T - T_0)\right) E^{\gamma} \exp\left[-\left(\frac{b\left[1 + d(T - T_0)\right]}{E}\right)^{\delta}\right] \tag{3.11}$$

University of Bologna Models

The model developed more recently by researchers in University of Bologna [9], [10] relies on numerical solutions of the Boltzmann Transport Equation and experiments. It includes a more accurate description of impact ionization at low electric field as well as temperature variation of the model parameters. The model is calibrated for a large range of electric fields: from 5×10^4 to 6×10^5 V/cm. Also, the model was tested at different temperatures (from 300 K to 700 K).

$$\alpha(E) = \frac{E}{a(T) + b(T) \exp\left[\frac{d(T)}{E + c(T)}\right]} \tag{3.12}$$

Later, the same research group re-calibrated the model's empirical parameters to better fit the ionization coefficients at higher temperature (up to 773 K) [11]–[13]. Both versions are available in Synopsys Sentaurus.

3.2.3 Carrier Generation in Space Charge Region

Several other phenomena can cause an electron-hole pair generation (or recombination), especially in SCR. This processes represent the exchange of carriers between conduction and valence bands. When working with SPAD, at high electric field, these generated pairs are very likely to trigger avalanche process, stressing the importance of modeling accurately each generation mechanism. In this subsection, the main generation/recombination phenomena used in TCAD simulation are presented.

Shockley-Read-Hall

Carriers can also be generated through the deep defect levels in the gap, and this process is described by Shockley-Read-Hall (SRH) statistics [14]–[16]. In Sentaurus Device, this phenomena is defined by the net value R_{net}^{SRH}, which represents the total SRH recombination minus the total SRH generation, as shown in Eq. 3.13.

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{3.13}$$

with:

$$n_1 = n_{i,eff} \exp\left(\frac{E_{trap}}{kT}\right) \tag{3.14}$$

and

$$p_1 = n_{i,eff} \exp\left(\frac{-E_{trap}}{kT}\right) \tag{3.15}$$

where

E_{trap} is the difference between the defect level and the intrinsic (midgap) level, having null value by default (traps in midgap).

$n_{i,eff}$ is the effective intrinsic density, which takes bandgap narrowing into account.

τ_n and τ_p are the lifetimes for electrons and holes, respectively.

Note that the SRH is a recombination mechanism when $np > n_i^2$ ($R_{net}^{SRH} > 0$) and a generation mechanism when $np < n_i^2$ (in dark regime).

The lifetimes were modeled here by considering their dependency on temperature, electric field, and also on doping (which depends on trap concentration, addressed here with default value), as shown in Eq. 3.16. It is important to notice that potential trap excess due to fabrication process (e.g. implantation, interfaces) are not taken into account here.

$$\tau = \tau_{dop} \frac{f(T)}{1 + g(E)} \tag{3.16}$$

The doping dependency is here expressed by the Scharfetter relation (Eq. 3.17) [17], [18]. For the following simulations, the minimum and maximum values of lifetimes were taken as ten times the default values provided by Synopsys Sentaurus, in order to better fit experimental data.

$$\tau_{dop} = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \left(\frac{N_A + N_D}{N_{ref}}\right)^{\gamma}} \tag{3.17}$$

The temperature dependency is modelled here with a power law (Eq. 3.18) [19].

$$f(T) = \left(\frac{T}{300K}\right)^{\alpha} \tag{3.18}$$

As for the last dependency, on the electric field, the Hurkx model [20] was used.

It predicts a combination between Band To Band Tunneling (B2B) and SRH, which is called Trap Assisted Tunneling (TAT). When exceeding electric fields of 3×10^5 V/cm, TAT generation is non-negligible. Eq.3.19 describes the model.

$$g(E) = \int_0^{\tilde{E}_n} \exp\left[u - \frac{2}{3}\frac{\sqrt{u^3}}{\tilde{E}}\right] du \tag{3.19}$$

with

$$\tilde{E} = \frac{q\hbar}{\sqrt{8 m_0 m_t k^3 T^3}} E \tag{3.20}$$

where:
$\tilde{E}_n$ is a fixed value of the electric field, calculated according to E_{trap} and E_g.
$\hbar$ is the reduced Planck's constant.
m_0 is the free electron mass.
m_t is the carrier tunneling mass.
k is the Boltzmann's constant.

If the Hurkx model is not activated, $g(E) = 0$ and R_{net}^{SRH} does not depend on the applied bias.

Band To Band Tunneling

One of the main generation phenomena, especially in heavily doped PN junctions, is the Band To Band Tunneling effect (B2B). It can happen when the junction is submitted to a certain threshold value of electric field and an electron in the P-region valence band directly migrates to the conduction band of the N-region, as illustrated in Fig. 3.5 [3], [4].

Some empirical models were developed for describing this phenomenon, such as the Hurkx [20], [21], Schenk [22] and Liou [23]. In our structures, all models were tested using the default parameters. Not many differences were observed between the results, so the simplest model (Liou) was kept. It is described by Eq. 3.21. It should be noted that this model is only suitable for high field regime (which was always the case in the simulations here presented), but provides a poor approximation for structures operating with low electric field.

$$G^{B2B} = AE^P \exp\left(-\frac{B}{E}\right) \tag{3.21}$$

3.3 TCAD Simulations: Methodology and Results

In order to correctly represent the SPAD behavior, several steps were adopted, as shown in Fig. 3.6. First, 1D SPROCESS simulation was used for estimating the doping profiles in the wells. Those profiles are then exported to a SDE environment, that sets parameters such as geometry, material and regions to be doped, but also places contacts for biasing the device. The built structure is, then, electrically simulated in SDEVICE, providing results that, in post-processing, can be used for estimating some of the SPAD

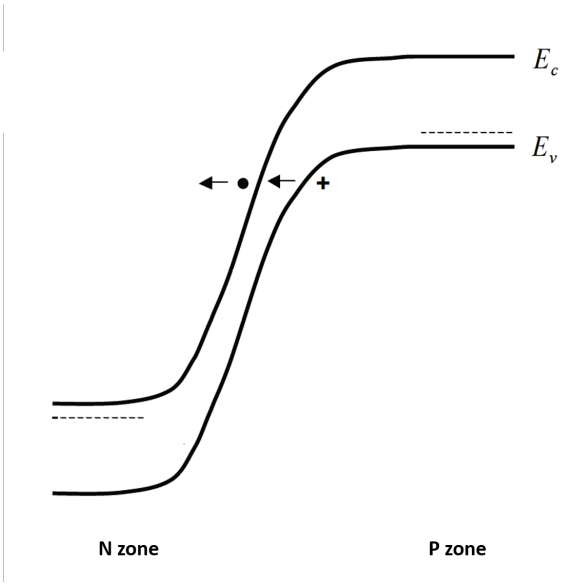

Figure 3.5: *Band To Band Tunneling effect. Adapted from [4]. An electron moves from the P-side valence band into the N-side conduction band.*

Figure Of Merit (FOM), such as DCR and PDP. Two types of TCAD electrical simulation were performed: Approximate Breakdown Analysis (ABA), and two variants of Resistor simulation (with and without avalanche). Their results are complementary and together help in the construction of a SPAD model.

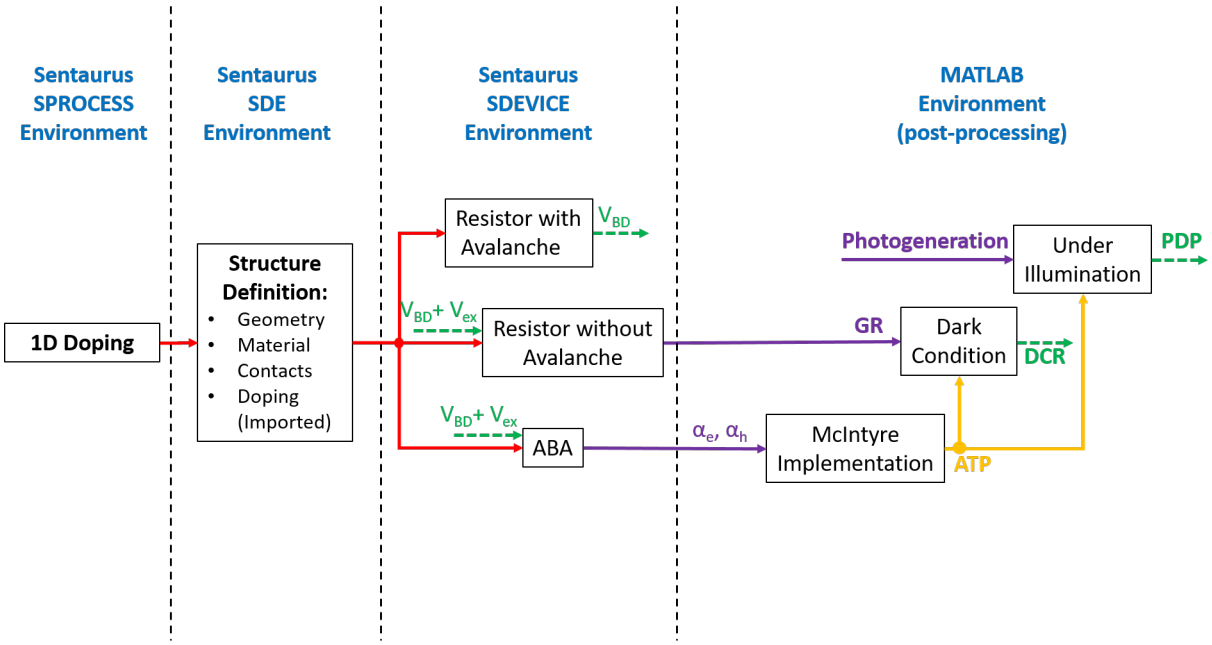

Figure 3.6: *Methodology for using TCAD tools and post-processing routines.*

3.3.1 Resistor Simulations with Avalanche

Since SPADs operate above breakdown voltage, the first step is to determine the breakdown voltage. There are two methods to calculate it. The first one, more accurate, consists in simulating the full avalanche diode and quenching resistance in a mixed mode approach. This approach is more computationally expensive. However, the results obtained have been found in better agreement with experiments [24]. The second approach is based on a model, named ABA model. This model calculates an expression of the multiplication factor M_P . The breakdown voltage is defined as the voltage for which M tends to the infinite. This second approach is more numerically efficient, but also less accurate (see section 3.3.3).

For both resistor-type simulations, Sentaurus Device takes into account an external load resistor and connects it to one of the device's terminals (here, the anode). The other terminal of the resistor is connected to the ground, while the cathode is biased at the high voltage. Once the circuit is properly biased, the I-V curve can be plotted and Sentaurus DEVICE can check its slope. By automatically adjusting the value of the load resistance, an optimal boundary condition (external voltage) is reached. In this case, the local tangent of the curve is orthogonal to the load line [2]. This tools facilitates convergence, and the breakdown voltage can be extracted from its steep slope, as shown in Fig. 3.7, for both original and modified versions of the junction, in the same way that it is done with measurement results.

At room temperature, the original diode presents $V_{BD} = 9.6\,\mathrm{V}$, while the structure with the new version of the DNW has its breakdown voltage increased in about 6 V, confirming the positive impact of the reduction of doping that makes the junction less abrupt.

The evolution of the breakdown voltage with temperature is shown in Fig. 3.8, for several ionization coefficients models (Section 3.2.2). It is easy to notice the influence of the models and their ionization coefficients in this characteristics, since, for the same simulated device, the values of the breakdown voltage, as well as their evolution (slope dV_{BD}/dT) vary according to the chosen model. This fact can be advantageously exploited when trying to better adapt the simulation to the real experimental data. All the models predict an increase in the breakdown voltage when the temperature rises, which makes sense, since the ionization coefficients tend to decrease when increasing temperature. When doping is reduced (modified DNW), V_{BD} increases, which is normal for less abrupt junctions. For both doping configurations, the highest slope and values are obtained for vanOverstraeten model, while Okuto-Crowell predicts a smoother growth. The Okuto-Crowell model was kept for the rest of the simulations, because it has been found in better agreement with experiments (Section 4.4).

According to [25], for avalanche process, with increasing temperature, the energy E_R that a carrier loses to the lattice during its travel through the space charge region (scattering with phonons) also increases, reducing in turn the ionization rate. To compensate this loss, the field strengths and that means the applied voltage must be increased to get that specific value and thus generate a self-sustained avalanche process.

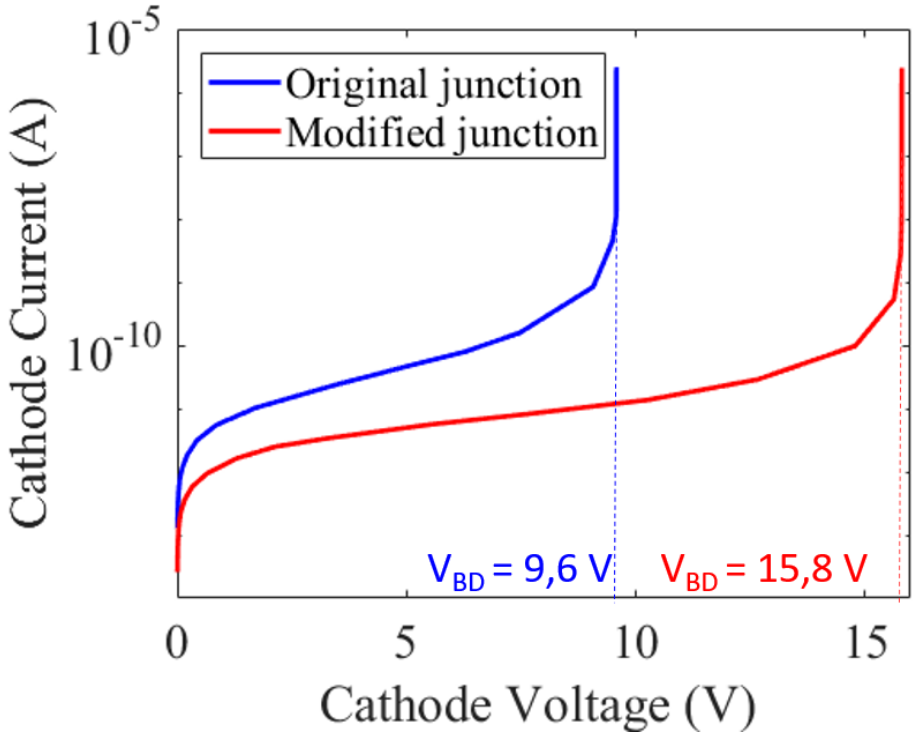

Figure 3.7: *I-V characteristics from TCAD resistor simulation, avalanche ON. At room temperature, Breakdown voltage is about* 9.6 V *for the original doping profile, while for modified DNW,* V_{BD} = 15.8 V

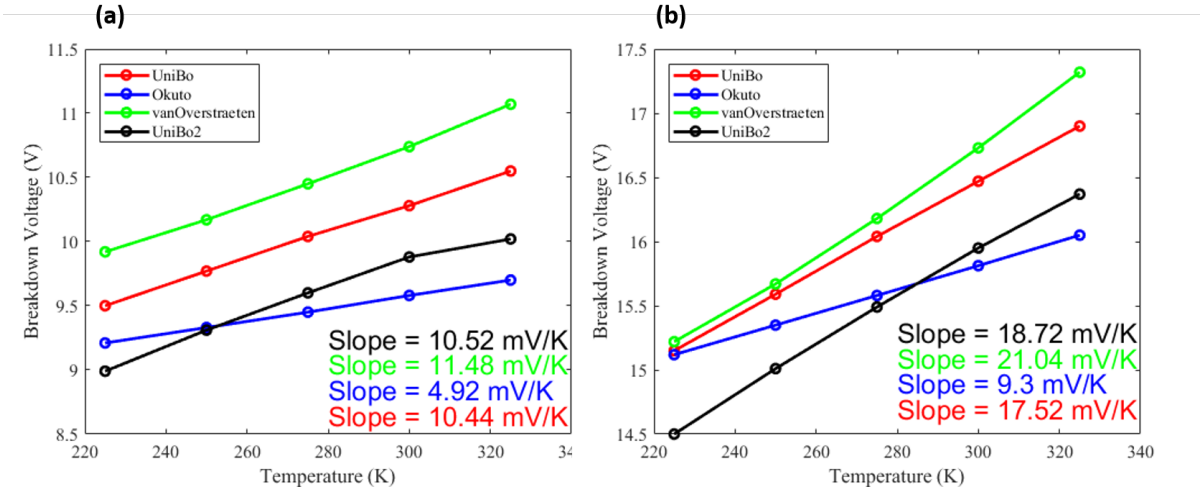

Figure 3.8: *Simulated breakdown voltage according to temperature for (a) original doping profile and (b) modified DNW. The influence of the models used for ionization coefficients can be easily verified.*

3.3.2 Resistor Simulations without Avalanche

So far, only steady state simulations have been presented. When the applied voltage exceeds the breakdown voltage in the steady state regime, the avalanche has, by definition, already started. However, Dark Count Rate (DCR) and Photon Detection Probability (PDP) are calculated in a non-equilibrium situation, where the avalanche has not started yet, but is likely to occur. In order to calculate DCR and PDP in a post processing approach using data (such as electric field profile), simulations where the impact ionization coefficients have been artificially switched off need to be performed.

The device simulation without avalanche represents the moment that immediately precedes the avalanche generation, i.e., when a carrier is generated (due to B2B, for example) and is then accelerated through SCR, starting impact ionization. This kind of simulation is quite useful for understanding the structure state (e.g. electric field) just before the avalanche event is triggered and the consequent current increases. From this simulation, carriers' generation rates are extracted at a certain V_{ex} value, as shown in Fig. 3.9.

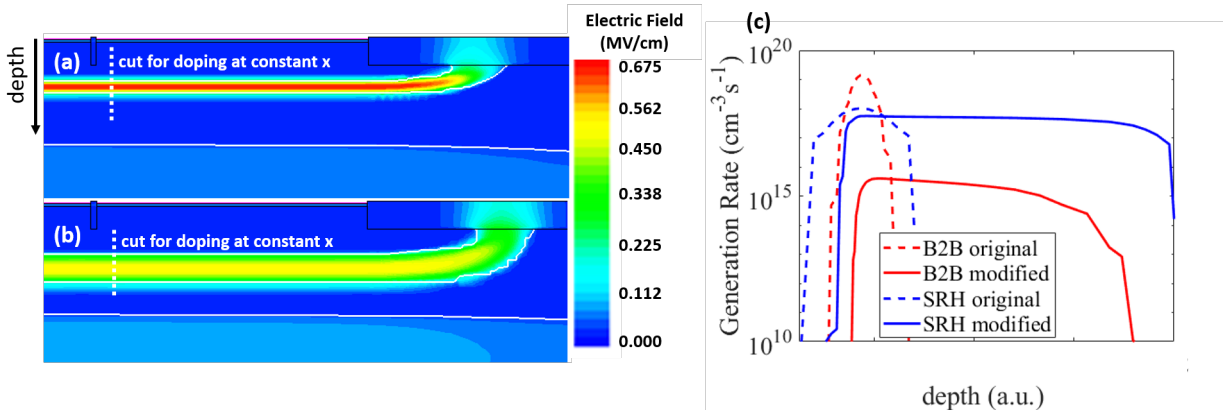

Figure 3.9: *Electric field cartography of the simulated structure with original (a) and modified (b) doping profiles for $V_{ex} = 1$ V). (c) Generation rate (SRH and B2B) at constant x, obtained from Resistor-OFF simulation, only at SCR for the both structures. The modification of the doping for the second structure implies in a drastic reduction of dark generation rate [26].*

As can be observed, in Fig. 3.9 (a) and (b), respectively for original and modified doping profiles, the electric field (here, for $V_{ex} = 1$ V) is uniform along the depletion region. For that reason, a cut at constant x can be done at nearly every position at SCR (except at borders, where the simulated field is decreased, thanks to guard ring). The generation rates (SRH and B2B) for this cut are represented in 3.9 (c). The use of this 1D approach is quite convenient for post-processing analysis, and its results can be interpreted as the standard behavior of the structure along the photosensitive area, since the parameters involved depend mostly on the electric field, which is quite uniform, according to this simulation.

It is easy to notice that the proposed modification of the DNW doping provides a drastic reduction in the generation rate caused by B2B effect: in the proposed modified DNW doping, B2B is decreased by a factor 1×10^4. This effect being one of the major phenomena responsible for the high dark count rate measured in Section 4.6, the new

doping configuration was proposed for reducing their influence in device performance. This modification seems to improve the intrinsic characteristics of the device in terms of noise, while keeping the original function of DNW, which is to isolate different PW.

3.3.3 Approximate Breakdown Analysis (ABA) Simulations

The ABA simulation takes into account the so-called ionization integrals ϕ_e and ϕ_h, two parameters dependent on both ionization coefficients, respectively for electrons and holes. They are useful for calculating the multiplication factor M_P, that should be infinite when avalanche occurs, since a single carrier generates a macroscopic current, through impact ionization.

In order to analyse these parameters, let us consider the impact ionization's generation rate (G^{II}) for both carriers in the structure [3]:

$$G^{II} = \alpha_n n v_n + \alpha_p p v_p \tag{3.22}$$

By neglecting diffusion, Eq. 3.22 can re-written:

$$G^{II} = \alpha_n \frac{J_n}{q} + \alpha_p \frac{J_p}{q} \tag{3.23}$$

Considering a 1D case, along the SCR, the current density is kept constant and can be expressed as the sum of the electrons' and holes' current densities:

$$J = J_n(x) + J_p(x) \tag{3.24}$$

For a PN junction, at the position $x = W$ (at the limit of SCR from N-side), the hole's current density reaches its maximum value $J_p(W) = J$. When comparing with its initial value $J_p(0)$, one can express:

$$J_p(x) = M_P J_p(0) = J \tag{3.25}$$

where M_P is the Multiplication Factor.
Also, the variation of J_p through SCR is given by the conservation equation:

$$\frac{dJ}{dx} = G \tag{3.26}$$

$$dJ_p = J_p \alpha_p dx + J_n \alpha_n dx \tag{3.27}$$

By considering Eq. 3.24 and rearranging:

$$\frac{dJ_p}{dx} - J_p(\alpha_p - \alpha_n) = J\alpha_n \tag{3.28}$$

The solution for the differential equation 3.28, by taking into into account the initial condition from 3.25 is

$$1 - \frac{1}{M_P} = \int_0^W \alpha_p \exp\left(-\int_0^x (\alpha_p - \alpha_n)dx\right)dx = \phi_p \tag{3.29}$$

When avalanche occurs, the gain (M_P) tends to the infinite (a single carrier generates a macroscopic current), which means the ionization integral equals 1:

$$1 = \int_0^W \alpha_p \exp\left(-\int_0^x (\alpha_p - \alpha_n)dx\right)dx = \phi_p \tag{3.30}$$

In the case of an electron is responsible for triggering the avalanche, the analysis is similar:

$$1 = \int_0^W \alpha_n \exp\left(-\int_0^x (\alpha_n - \alpha_p)dx\right)dx = \phi_n \tag{3.31}$$

The ABA simulation basically calculates these ionization integrals. The ionization coefficients cannot be extracted from resistor simulation when avalanche is activated, because, due to the current flow through the device, the voltage across the junction will not go any higher than V_{BD}, as previously shown in Fig 3.7. The ionization coefficients in this case are calculated at V_{BD}, which do not represent the much higher values expected when avalanche has not yet been triggered (situation when the junction is biased at $V_{BD} + V_{ex}$). On the other hand, in ABA simulation, no current flows through the device, allowing the coefficients to be calculated at the proper biasing condition.

In Fig. 3.10 (a), the ionization coefficients at room temperature are plotted, according to depth, for an excess voltage 1 V. Again, arbitrary units were used to preserve the confidential data. In (b), it is possible to observe the ionization integrals ϕ_e and ϕ_h. When avalanche occurs, the integrals equal one. This method gives a quick approximation of the value of breakdown voltage, but is less accurate, when compared with resistor simulation, as shown in Fig. 3.11.

3.4 Post-Processing Calculations for SPAD Performance Estimation

Once the three simulations were performed and their respective data were extracted from TCAD simulations (Fig. 3.6), post-processing is often needed in order to estimate some of SPAD's Figure Of Merit (FOM), such as Avalanche Triggering Probability (ATP), Dark Count Rate (DCR) and Photon Detection Probability (PDP). Here, MATLAB codes were used to calculate these characteristics, as shown in Fig. 3.6.

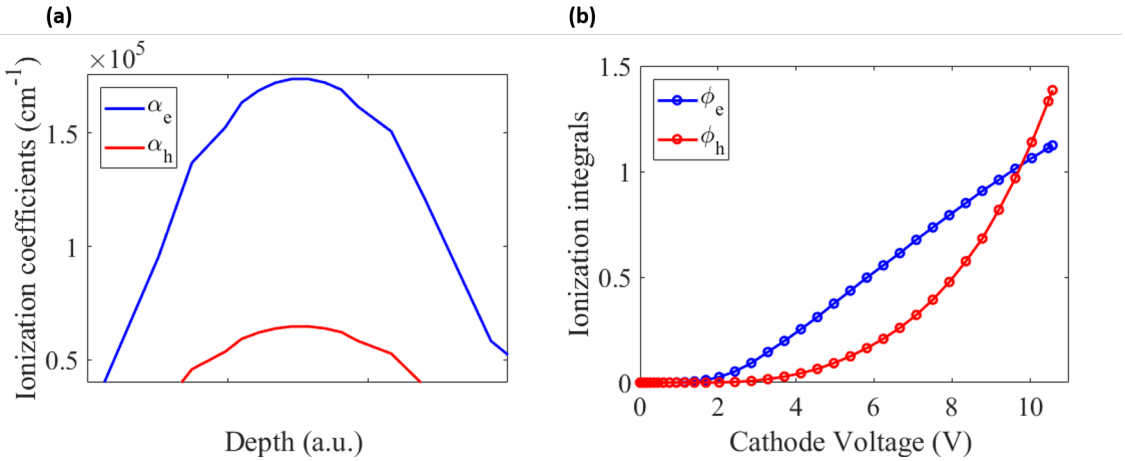

Figure 3.10: *(a) Extraction of ionization coefficients, for the same structure as Fig. 3.9, at the same position (b)Demonstration of the ionization integrals, calculated in ABA method, providing a quick first estimation of breakdown voltage, when the integrals equal one.*

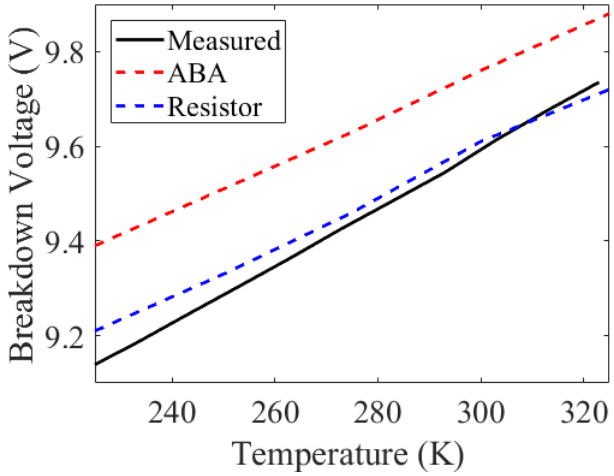

Figure 3.11: *Comparison between experimental and simulated V_{BD} according to the temperature, for both ABA and resistor simulations. Okuto-Crowell model was kept here, because it provides the best approximations.*

3.4.1 Avalanche Triggering Probability Calculation

Avalanche Triggering Probability (ATP) is one of the main parameters needed for estimating important factors of merit in SPAD, such as DCR and PDP. A well-known theory was built in order to calculate this probability: the McIntyre model [27]. Let us review the main features of this model, creating from a simple NP junction, as shown in Fig. 3.12.

Once a carrier is generated (or transported) into SCR, it needs to be accelerated through the SCR in order to cause impact ionization. It actually does not matter which carrier triggered the avalanche process, since the gain tends to infinite. Thus, the joint

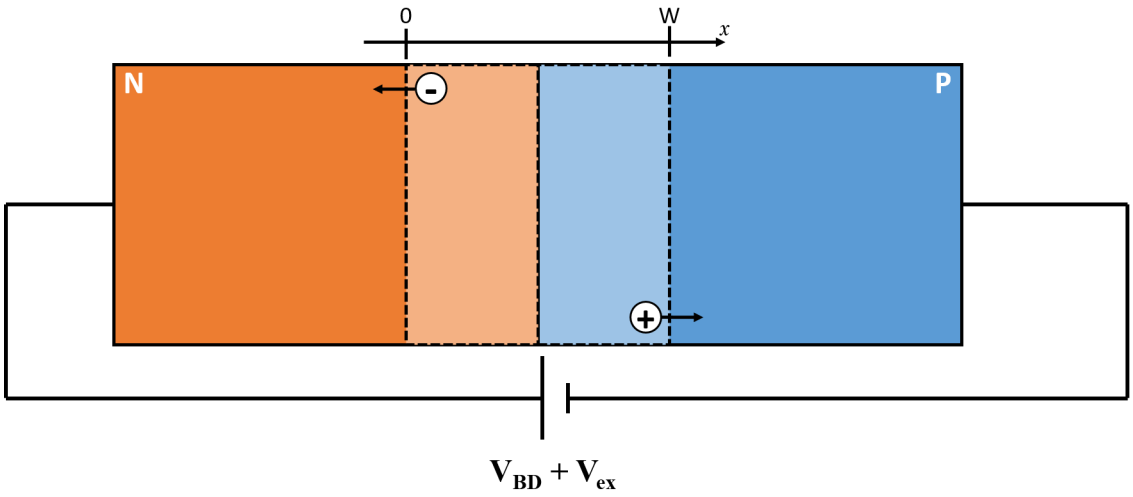

Figure 3.12: *NP junction reversed biased above breakdown voltage.*

avalanche triggering probability $P_P(x)$ (or ATP), according to the position x in SCR can be expressed as in Eq. 3.32.

$$P_P(x) = P_e(x) + P_h(x) - P_e(x)P_h(x) \tag{3.32}$$

Where

$P_e(x)$ and $P_h(x)$ are respectively the probabilities of an electron or a hole to trigger an avalanche.

Rearranging Eq. 3.32 and then deriving, one gets:

$$P_P(x) = 1 - (1 - P_h(x))(1 - P_e(x)) \tag{3.33}$$

$$\frac{dP_P}{dx} = (1 - P_e)\frac{dP_h}{dx} + (1 - P_h)\frac{dP_e}{dx} \tag{3.34}$$

From [28]:

$$\frac{dP_e}{dx} = (1 - P_e)\alpha_e P_P \tag{3.35}$$

$$\frac{dP_h}{dx} = (1 - P_h)\alpha_h P_P \tag{3.36}$$

By replacing Eq. 3.35 and 3.36 in Eq. 3.34, one gets:

$$\frac{dP_P}{dx} = (\alpha_e - \alpha_h)P_P(1 - P_P) \tag{3.37}$$

Since, due to reverse bias, the electrons are accelerated to the N region and holes

to P region, in Fig. 3.12:

$$P_e(0) = 0 \tag{3.38}$$
$$P_h(W) = 0 \tag{3.39}$$

and thus:

$$P_P(0) = P_h(0) \tag{3.40}$$
$$P_P(W) = P_e(W) \tag{3.41}$$

With these limit conditions, McIntyre was able to propose a solution for Eq. 3.37 [27]:

$$P_P(x) = \frac{P_h(0)f(x)}{P_h(0)f(x) + 1 - P_h(0)} = ATP(x) \tag{3.42}$$

with

$$f(x) = \exp\left(\int_0^x (\alpha_e - \alpha_h)dx\right) \tag{3.43}$$

By replacing Eq. 3.42 into Eq. 3.36, $P_h(x)$ can be expressed as:

$$P_h(x) = 1 - (1 - P_h(0)) \exp\left(\int_0^x \alpha_h(x)P_P(x)dx\right) \tag{3.44}$$

In order to calculate the solution for Eq. 3.42, $P_h(0)$ needs to be known. This can be easily achieved by solving the transcendental Eq. 3.44, which comes to numerically solve Eq. 3.45

$$-\ln\left[1 - P_h(0)\right] = \int_0^W \frac{P_h(0)\alpha_h(x)f(x)}{P_h(0)f(x) + 1 - P_h(0)}dx \tag{3.45}$$

This method was only very recently implemented in Sentaurus SDEVICE (version 2018, [2]) and that is the reason why Post-processing tools needed to be used here in order to estimate ATP, for most of the cases. In this case, only a 1D analysis was provided, but since the electric field is uniform for the simulated structure, the analysis can be extended for most of the SCR.

It should be noted that since none of the models for ionization coefficients can be analytically integrated, all of the previously presented equations can only be numerically solved. Firstly, $f(x)$, then the solution for $P_h(0)$. If one is also interested in the probabilities for each carrier, along SCR, at least Eq. 3.35 or Eq. 3.36 needs to be numerically solved. In summary, in order to estimate ATP, at least two numerical solutions need to be provided (typically 3 or 4, if $P_e(x)$ and $P_h(x)$ need to be estimated), which can be time

consuming, especially when analyzing the case of 2D or 3D structures, or even in a matrix implementation.

Proposed Method for Simplifying McIntyre Calculations

In order to simplify and accelerate post processing calculation, we propose an analytical solution, based on a high electric field approximation for the ionization coefficients. Indeed, all the models for ionization coefficients predict a linear dependency on the electric field, for high values of this parameter, as can be seen in Fig. 3.13 and in Eq. 3.46 for Okuto-Crowell (derived from Eq. 3.11) and 3.47 for University of Bologna models (derived from Eq. 3.12).

$$\lim_{E\to\infty} \alpha_{OC}(E) = aE \tag{3.46}$$

$$\lim_{E\to\infty} \alpha_{UB}(E) = \frac{E}{a+b} \tag{3.47}$$

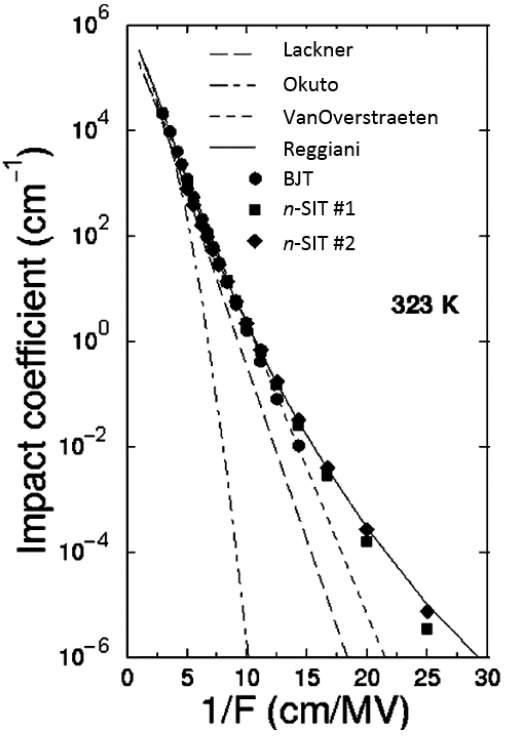

Figure 3.13: *(Adapted from [29]) Electron impact-ionization coefficient according to the inverse of electric field at T = 323 K, for several models. Symbols represent measured data for different devices, presented in [29]. A linear dependency can be observed for high electric field in all models here represented.*

This approximation can be very conveniently explored when integrating the electric field:

$$\int_0^x E(x)dx = \int_{V(0)}^{V(x)} -dV = V(0) - V(x) \tag{3.48}$$

However, the high field (HF) approximation of the ionization coefficient is typically valid in a limited extent, close to the maximum of the electric field profile, and not in the full space charge layer, where, on the contrary, the ionization coefficient become rapidly negligible at its edges. By taking into account these observations, the following linear approximation for the ionization coefficient is used for $x_a < x < x_b$:

$$\alpha(E) = \beta E \tag{3.49}$$

where x_a and x_b are the abscissas for which the electric field has a fixed minimum value E_{min}:

$$E(x_a) = E(x_b) = E_{min} \tag{3.50}$$

The value of β_e and β_h can be taken from their maximum values in high field (HF) condition. Since the Okuto-Crowell model provided the best fit for our experimental $V_{BD} = f(T)$ curves (as presented in Section 4.4), it was used here to illustrate the concept of the approach:

$$\beta_{HF} = a \tag{3.51}$$

In order to account for eventual deviation to the high field approximation (real SPADs typically operate in moderate electric fields for avoiding excessive DCR), the following fitting parameter γ has been introduced for electrons and holes. Their values depend on the maximum electric field in the structure, which is directly related to the applied voltage across the junction. A discussion on how to properly choose the fitting parameters is presented at the end of this section.

$$\beta = \frac{\beta_{HF}}{\gamma} \tag{3.52}$$

Thus, according to the proposed approximation:

$$\alpha = \begin{cases} \beta E(x), & \text{if } x_a < x < x_b \\ 0, & \text{otherwise} \end{cases} \tag{3.53}$$

This consideration can be applied to the calculation of the $f(x)$ function (Eq. 3.43):

$$f(x) = \exp\left(\int_0^x (\alpha_e - \alpha_h)dx\right) \tag{3.54}$$

$$f(x) = \exp\left(\int_{V(x_a)}^{V(x)} -(\beta_e - \beta_h)dV\right) \tag{3.55}$$

$$f(x) = \begin{cases} \exp\left((\beta_e - \beta_h)(V(x_a) - V(x))\right), & \text{for } x_a < x < x_b \\ \exp\left((\beta_e - \beta_h)(V(x_a) - V(x_b))\right), & \text{for } x > x_b \end{cases} \tag{3.56}$$

The probability $P_h(x)$ can be calculated according to Eq. 3.44 [27]. Let us introduce the quantity $I(x)$ as:

$$I(x) = \int_0^x \alpha_h(u) P_P(u) du \tag{3.57}$$

$$I(x) = \int_0^x \frac{\alpha_h(u) P_h(0) f(u)}{1 - P_h(0) + P_h(0) f(u)} du \tag{3.58}$$

By using the results of the proposed approximation, $I(x)$ can be integrated, leading to:

$$I(x) = \int_{x_a}^x \frac{\beta_h E(u) P_h(0) \exp\left((\beta_e - \beta_h)(V(x_a) - V(u))\right)}{1 - P_h(0) + P_h(0) \exp\left((\beta_e - \beta_h)(V(x_a) - V(u))\right)} du \tag{3.59}$$

$$I(x) = \int_{V(x_a)}^{V(x)} \frac{-\beta_h P_h(0) \exp\left((\beta_e - \beta_h)(V(x_a) - V)\right)}{1 - P_h(0) + P_h(0) \exp\left((\beta_e - \beta_h)(V(x_a) - V)\right)} dV \tag{3.60}$$

$$I(x) = \frac{\beta_h}{\beta_e - \beta_h} \left[\ln\left(1 - P_h(0) + P_h(0) \exp\left((\beta_e - \beta_h)(V(x_a) - V)\right)\right)\right]_{V(x_a)}^{V(x)} \tag{3.61}$$

$$I(x) = \frac{\beta_h}{\beta_e - \beta_h} \ln\left[1 - P_h(0) + P_h(0) \exp\left((\beta_e - \beta_h)(V(x_a) - V(x))\right)\right] \tag{3.62}$$

$$P_h(x) = 1 - (1 - P_h(0)) \left[1 - P_h(0) + P_h(0) \exp\left((\beta_e - \beta_h)(V(x_a) - V(x))\right)\right]^{\frac{\beta_h}{\beta_e - \beta_h}} \tag{3.63}$$

As previously seen, the holes are accelerated towards the neutral P region. Thus, the holes generated in at $x = x_b$ will not travel through SCR, having zero avalanche triggering probability at this position, as shown in Eq. 3.64. Its solution can only be obtained numerically, but in the case of this high electric field approximation, this is the only solution that cannot be achieved analytically, which can be time saving, especially complex simulated structures.

$$0 = 1 - (1 - P_h(0)) \left[1 - P_h(0) + P_h(0) \exp\left((\beta_e - \beta_h)(V(x_a) - V(x_b))\right)\right]^{\frac{\beta_h}{\beta_e - \beta_h}} \tag{3.64}$$

Similarly, for electrons:

$$P_e(x) = 1 - \left[1 - P_h(0) + P_h(0) \exp\left((\beta_e - \beta_h)(V(x_a) - V(x))\right)\right]^{\frac{\beta_e}{\beta_e - \beta_h}} \tag{3.65}$$

Equations 3.63 and 3.65 are analytical expressions for $P_h(x)$ and $P_e(x)$, respectively, provided that $P_h(0)$ is extracted from a numerical solution of Eq. 3.64, and that the fitting parameters γ_e and γ_h have been found.

In order to validate the model and its assumptions, a comparison have been performed with TCAD simulations (Synopsys) (Fig. 3.14) for an arbitrary junction with Gaussian doping profile, bias at $V_{ex} = 2\,\mathrm{V}$. The popular Okuto-Crowell impact

ionization model has been used. In the model, the threshold for ionization has been set to $E_{min} = 0.1$ MV/cm for both electrons and holes, and the fitting parameters γ have been set by adjusting the values of the analytical calculation of the function $f(x)$ (Eq. 3.56) to the original numerically calculated values (Eq. 3.43), obtained directly from Synopsys Sentaurus, in the most recent version of the software.

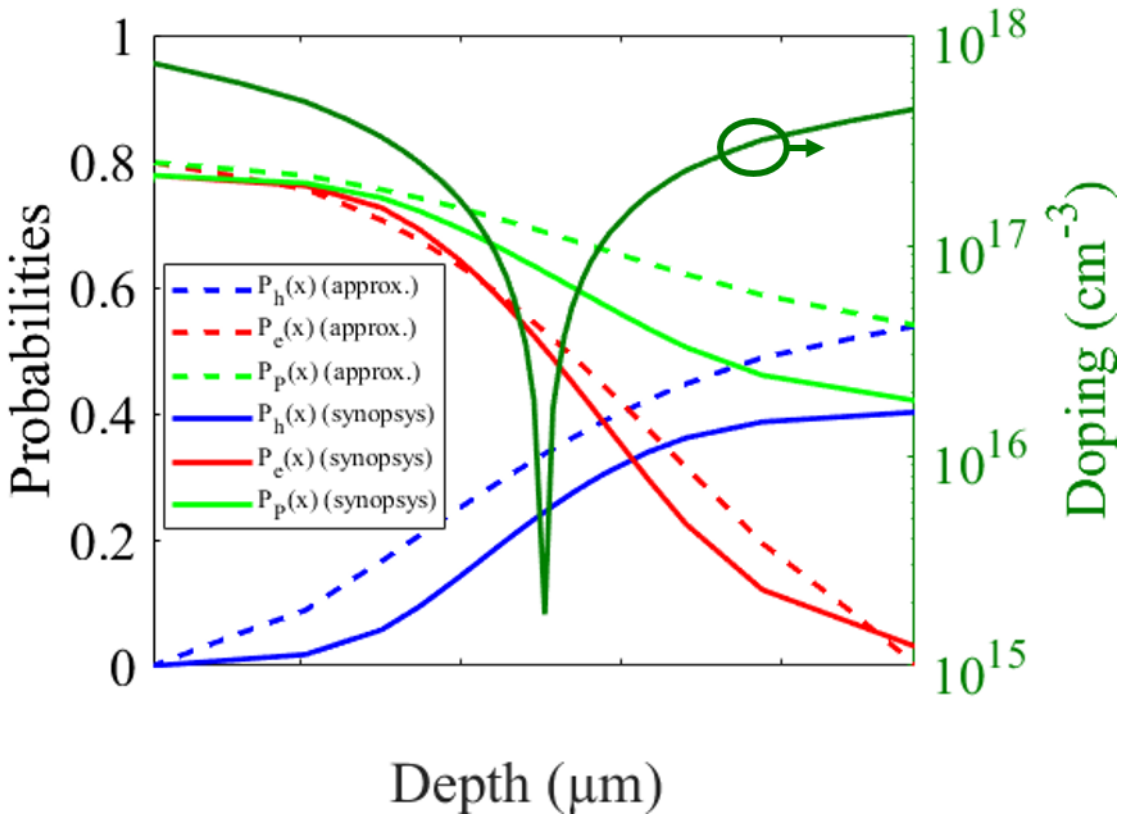

Figure 3.14: *Avalanche Triggering Probabilities for electrons, holes and pair for a NP junction simulated in TCAD.*

In order to obtain a good agreement between both approaches, the classical McIntyre model and the high field approximation, the fitting parameters γ_e and γ_h need to be correctly chosen. As previously explained, these fitting parameters are used to validate, in not so high electric field regions, the approximation for high field regions, in a way that a single linear dependency of the ionization coefficients on the electric field can be used along all SCR.

So far, these parameters have been extracted specifically for each voltage and each doping profile. In the following, an empirical procedure is proposed to determine a reasonable value of γ without calibration.

For better understanding the behavior of these fitting parameters, two different junctions were simulated in TCAD. The first one is a symmetrical abrupt junction, while the second one is asymmetrical. Their doping concentration can be seen in Table 3.1. For both junctions, the applied reverse voltage was varied, aiming at changing the value of the Electric Field. Then, the fitting parameters were manually adjusted to provide a

good approximation of the probabilities (maximum error = 10 %, when compared to TCAD results).

Junction	N_D (cm^{-3})	N_A (cm^{-3})
Asymmetrical	2×10^{18}	3×10^{18}
Symmetrical	3×10^{18}	3×10^{18}

Table 3.1: *Doping parameters for simulated symmetrical and asymmetrical junctions.*

It is possible to observe in Fig. 3.15 that the fitting parameters highly depend on the maximum value of electric field in the junction, which is basically a function of applied voltage and doping parameters, the latter often not precisely known for commercial technologies, due to confidentiality issues.

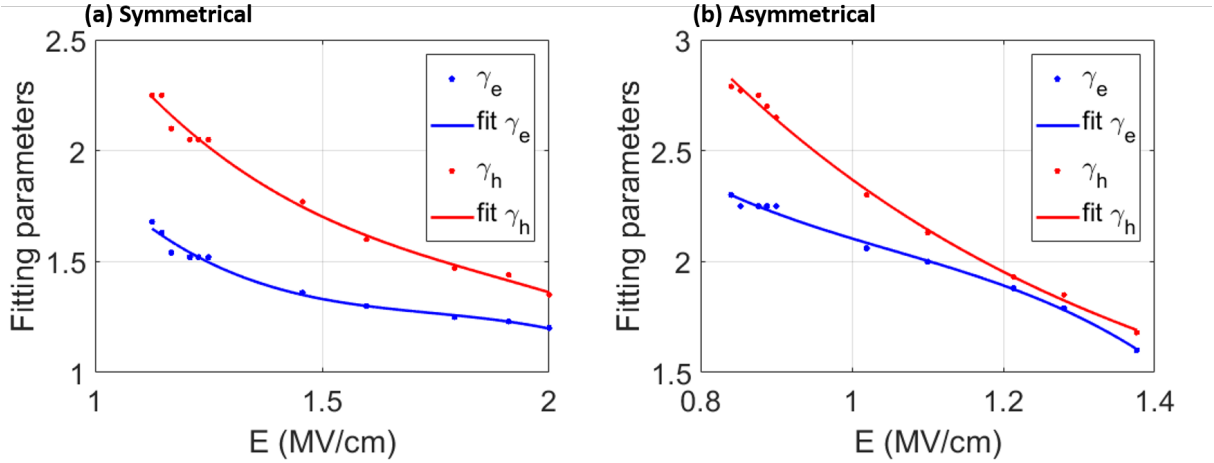

Figure 3.15: *Fitting parameters as a function of maximum electric field for symmetrical (a) and asymmetrical (b) NP junctions simulated in TCAD.*

The dependency of such fitting parameters, according to the maximum electric field, for all cases, follow a third-order polynomial evolution, according to excess bias voltage:

$$\gamma(E) = aE^3 + bE^2 + cE + d \tag{3.66}$$

The coefficients that describe curves in Fig. 3.15 can be seen in Table 3.2. By taking into account the nature of the junction's doping (symmetrical or asymmetrical), one can determine the fitting parameters for the model, by using the aforementioned curves.

Coefficients	Symmetrical		Asymmetrical	
	γ_e	γ_h	γ_e	γ_h
a	-1.106	-0.822	-3.7	-1.028
b	5.777	4.664	11.72	5.243
c	-10.26	-9.406	-13.37	-9.874
d	7.453	8.092	7.454	8.03

Table 3.2: *Coefficients used in Eq. 3.66 to describe fitting parameters' evolution according to maximum electric field at the junction.*

3.4.2 Dark Count Rate

The Dark Count Rate (DCR) is one of the main FOM for SPAD, since it represents how noisy the device is. From the data provided by TCAD simulation, it is possible to roughly estimate DCR in post-processing, by taking into account the generated carriers in the SCR and using Eq. 3.67.

$$DCR = \int_{x_a}^{x_b} ATP(x)GR(x)dx \tag{3.67}$$

where:
x_a and x_b are the limits of the SCR
$ATP(x)$ is the joint avalanche triggering probability
$GR(x)$ is the carrier generation rate in dark condition (e.g. SRH, B2B)

This 1D analysis was implemented in MATLAB and can be expanded to the areas in SCR that share the same values of electric field, since it is the main parameter that determines the values of $ATP(x)$ and $GR(x)$. This analytical calculation is not able to give the absolute value of DCR, because it depends on many parameters (e.g. electric field, ionization coefficients, generation rate models), but it allows parametric analysis or relative comparison between structures. The results of this integration, done for a FDSOI SPAD, for several values of excess voltage and temperature can be seen in Fig. 3.16 and 3.17, respectively for the native and modified DNW. For those simulations, both B2B and SRH dark generation rates are considered.

As can be observed, the calculated DCR increases both with excess voltage and temperature, being a reduced by a decade, when DNW is less doped. Some values of simulated excess voltage were kept low because measured DCR could only be obtained at most 0.3 V, as explained in Chapter 4. The activation energy determined by TCAD simulation is around 0.11 eV and 0.52 eV, respectively for the original and modified versions of DNW. This difference can be explained by the fact that the B2B contribution is drastically reduced, when simulating the new doping configuration, as previously shown in Fig. 3.9. The new value is close to the mid-gap of silicon, which is mainly related to SRH effect [30]–[32].

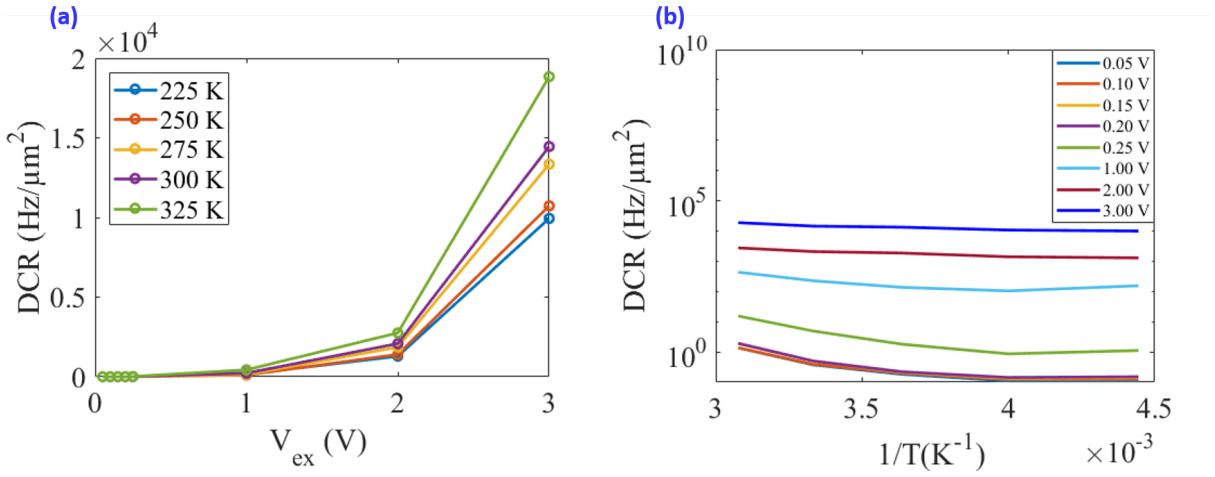

Figure 3.16: *For the original DNW: (a) DCR according to excess voltages for several values of temperature; (b) Arrhenius plot for DCR.*

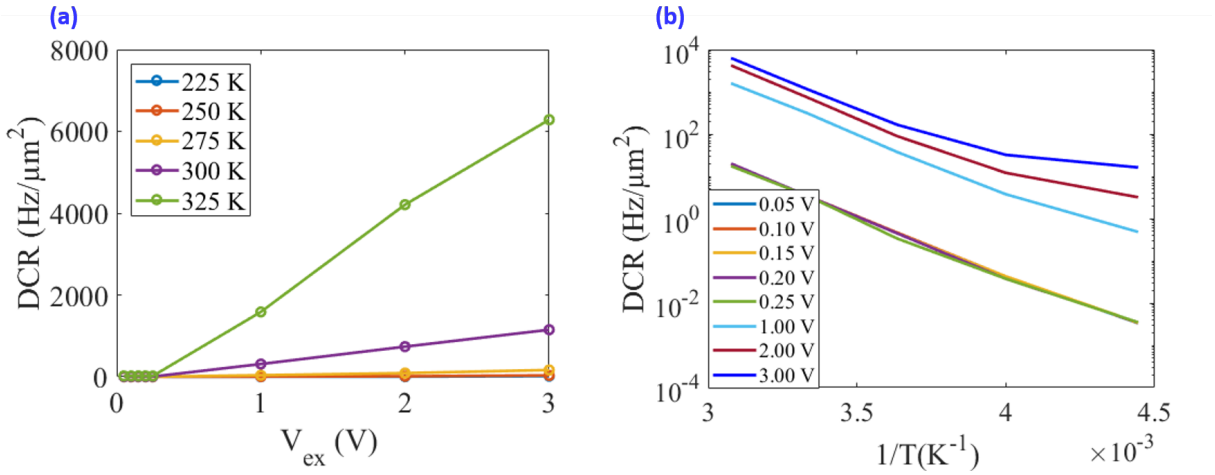

Figure 3.17: *For the proposed modification of DNW: (a) DCR according to excess voltages for several values of temperature; (b) Arrhenius plot for DCR.*

3.4.3 Photon Detection Probability

When a photon impinges silicon, it can be absorbed and generate an electron hole pair. If this absorption happens in SCR, the electric field accelerates those carriers and can start an self-sustained avalanche, according to the aforementioned probabilities at the position where the pair is generated.

In a simplistic approach, the photon absorption density in the SCR can be modelled by the Beer-Lambert law (Eq. 3.68) [33], [34]:

$$P_{abs}(z) = \alpha_{Si} \exp\left(-\alpha_{Si} z\right) \tag{3.68}$$

where

α_{Si} is the absorption coefficient for silicon, dependent on the wavelength.

Thus, in a similar way that is calculated the DCR, the PDP can be expressed as in Eq. 3.69, by only taking into account the photogenerated carriers in the SCR.

$$PDP = \int_{x_a}^{x_b} ATP(x) P_{abs}(x) dx \tag{3.69}$$

Since in practice the experimental excess voltage could not be highly increased for the first fabricated devices, as explained in Chapter 4, the ATP and thus the PDP were very low for such values of V_{ex}.

By optimizing the structure and reducing its intrinsic noise, it should be possible to reach higher values of excess voltage. For such optimized conditions, an initial estimation of PDP was addressed in this section, for $V_{ex} = 2\,\text{V}$. The results of this first approach are shown in Fig. 3.18

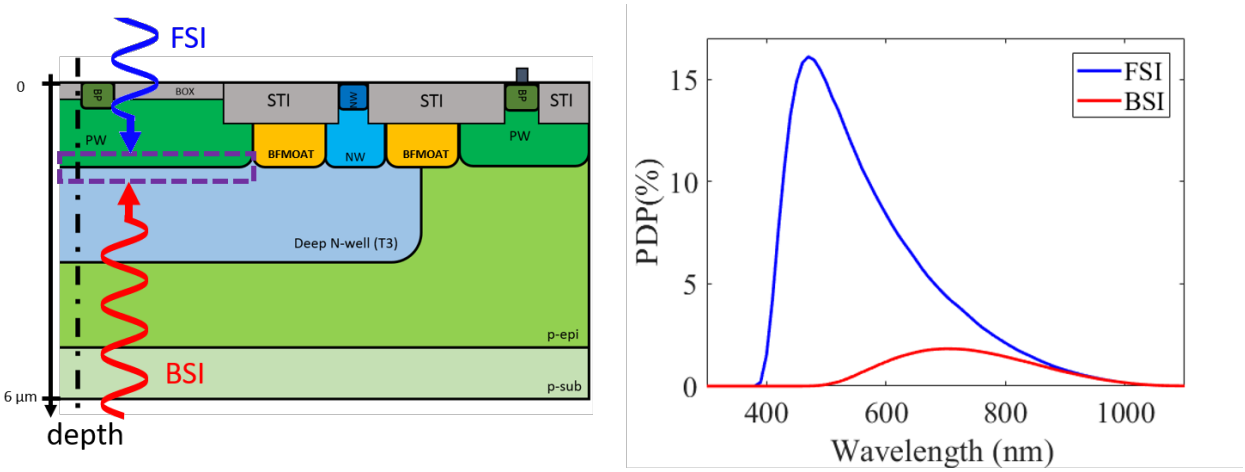

Figure 3.18: *Estimation of PDP at $V_{ex} = 2\,\text{V}$ for (a) Front Side Illumination; (b) Back Side Illumination. Silicon thickness:* 6 µm

Since the junction is located at a fair enough shallow depth of the silicon structure, it is normal to have a higher PDP for Front Side Illumination (FSI) approach, with visible light. The analysis here presented do not consider any reflection that can happen with photon travelling through the structure, before impinging SCR. This can be quite likely to happen, because of the several metal layers present for circuitry connection. Back Side Illumination (BSI) should then provide better results in practice, after die thinning.

Carriers can also be generated at the top and bottom neutral regions, outside SCR. They could be then transported into the depletion region, by drift or diffusion processes, and then trigger an avalanche event, achieving then the photon detection. Such approach needs to take into account the carriers' diffusion length and also the electrical field, in order to have a fair estimation. Also, reflection effect in the layers' interfaces should be considered. Such path should be addressed in future, once the PDP can be properly measured, the main objective of our approach being achieving in BSI the same efficiencies obtained in FSI, while increasing FF thanks to the intrinsic 3D integration provided by the technology.

Conclusions

In this chapter, the main methods of simulation for SPAD implemented in FDSOI were presented. In order to better understand the behavior of these structures, several types of TCAD simulations were performed and discussed.

First, the device was defined using geometric parameters from the designed structure presented in the previous chapter, along with some data provided by the foundry, such as thickness of some layers.

In order to perform an accurate simulation, the doping profiles of the structure need to be precisely known. The best way to implement these data correctly in the structure is by means of process simulation, where the implants information can be accurately taken into account. By performing this kind of simulation for different structures, it was possible to explain some of the measured characteristics obtained, especially between STI and FDSOI regions.

Once the device structure is correctly constructed in TCAD, electron and hole transport can be simulated, by reversely biasing the diode and observing important parameters such as breakdown voltage, electric field magnitude and its spatial distribution, SCR limits, ionization coefficients and carrier generation rates. In order to obtain these data, three different types of simulation were performed, to correctly represent the physics right before triggering avalanche and also during such events. Different models were also studied for some physical phenomena, the ones the most adapted to the experimental data being kept for comparisons with measurements.

Once the ionization coefficients and generation rates are obtained for a given excess voltage, they could be used in post processing for estimating Avalanche Triggering Probability (ATP), Dark Count Rate (DCR) and Photon Detection Probability (PDP).

For ATP, McIntyre model was initially used. An approximated analytical solution for this model was also proposed, based on a high electrical field approximation for the ionization coefficients. This approximation was extended to the whole SCR, thanks to the fitting parameters introduced for regions with moderate values of electric field. The model was validated by means of comparison with the original McIntyre solution, the main advantage of this new approach being the reduction of the numeric solutions for the concerned original equations, that were excessively time consuming. This approach can also be used for compact modeling of DCR and PDP.

Dark Count Rate was also estimated by means of post-processing, where ATP and dark carrier generation rate were taken into account. The evolution according to temperature of this important figure of merit was also analyzed, thanks to Arrhenius plot. The extraction of activation energy from its slopes proved the high influence of B2B and TAT phenomena in dark events, being intrinsic to structure.

Moreover, a rough estimation of Photon Detection Probability was made, by taking into account the Beer-Lambert law, describing the photon absorption in the material. Unfortunately, the detection efficiency for the simulated device proved to be negligible for the low excess voltages that could be used in practice for the first prototypes. Nevertheless, for higher values of excess voltages, the results seemed promising.

In order to optimize the structure, and also in agreement with the foundry, a modification in the DNW implants was addressed for increasing breakdown voltage.

By means of TCAD simulation, it was possible to prove that making the junction less abrupt, dark generation rates induced by B2B can be drastically reduced, which should provide less noise, in theory.

Since the C28FDSOI technology was not initially designed specifically for SPAD implementation, it makes sense that even in simulation FDSOI SPAD appears less efficient than state of the art bulk SPAD. Nevertheless, it is expected, as shown for instance by changing the doping profile, that there is still room for improvements using minor technological modifications.

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Chapter 4

Characterization of SPAD Cells

In this chapter, different SPAD cells developed in FDSOI technology were characterized. The tests here covered are: I-V and C-V curves, Breakdown Voltage as a function of temperature, electroluminescence response and dark count rate. The sensing cells for indirect avalanche detection were also electrically characterized in static and dynamics. The results are then discussed, and improvements are proposed. A wafer with deep N-well dedicated implant was characterized as well, their results being presented at the end of the chapter.

4.1 I-V Curves

Even if SPAD diodes are only used in reverse bias, direct characteristics are useful to determine the ideality factor of the diode, which in turn informs about the internal conduction mechanisms in the PN junction [1]. The forward-biased diode characteristics for a diode integrated under the BOX layer (hereby named FDSOI zone), is shown in Fig. 4.1. The measure was obtained by probe station test, using semiconductor analyzer Keithley 4200. According to Sze [1], the direct current I through a PN junction can be expressed as a function of the applied voltage V as expressed in equation 4.1.

$$I \approx I_S \exp\left(\frac{qV}{\eta kT}\right), \tag{4.1}$$

where:

I_S is the saturation current,
q is the elementary charge,
k is the Boltzmann's constant,
η is the ideality factor of the diode.

Thus:

$$\ln(I) \approx \ln(I_S) + \left(\frac{q}{\eta kT}\right) V \tag{4.2}$$

The ideality factor η varies between 1 and 2, according to the main conduction phenomenon in the diode. When recombination current dominates, η equals 2, while η equals 1 represents a domination of diffusion current [1]. The slope of the curve

presented in Fig. 4.1 is obtained from the linear fit of the anode current $ln(I_a)$ according to the applied voltage V and equals 38.4 V^{-1}, which means $\eta \approx 1$, making the diode nearly ideal, which represents a domination of diffusion mechanisms.

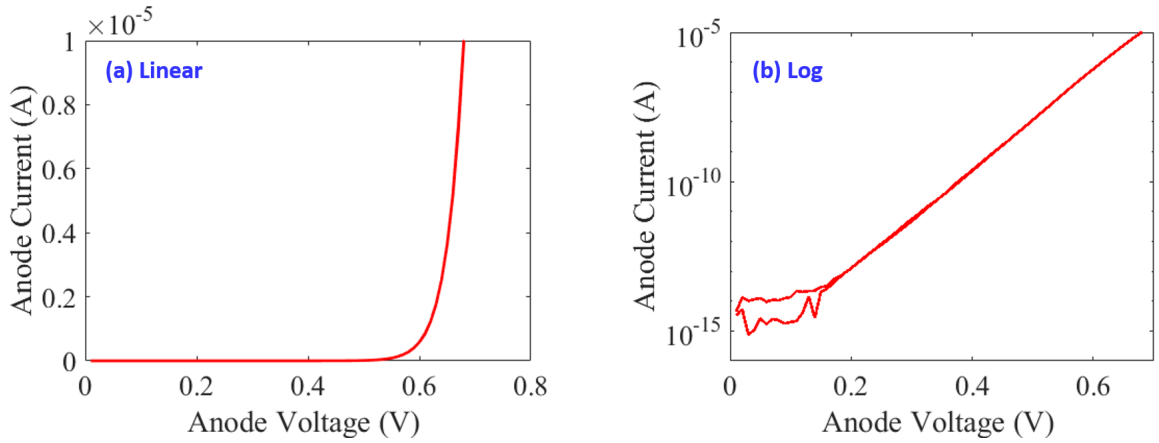

Figure 4.1: *Measured forward characteristics for a SPAD diode integrated in a FDSOI zone: (a) linear scale; (b) log scale.*

The reverse I-V curves for both FDSOI and STI zones (PN junction under STI layer: no BOX, no thin silicon film, as previously shown in Fig. 2.9) is presented in Fig. 4.2, for illuminated cells. Breakdown voltage at room temperature was taken at a current value of 10 µA and is respectively 9.50 V and 9.35 V for FDSOI and STI. This slight difference between these values is probably due to the implants, done through different layers for each zone, as explained in section 3.1.2.

As previously discussed in Chapter 2, several parameters were varied during SPAD cells design: geometry, zone in which the cell is integrated, guard distance and cell size. By analyzing their corresponding I-V curves, the only parameter that appears to have an influence in those curves is the integration zone: STI cells have a smaller breakdown voltage than FDSOI, the other aforementioned parameters not having any interference in results.

4.2 C-V Curves

It is well known that reversed bias pn junctions can behave as a dynamic capacitances, whose value is expressed by Eq. 4.3 [2], for an ideal plate capacitor.

$$C = \frac{\varepsilon S}{W} \tag{4.3}$$

where:

ε is the electric permittivity of the material
S is the junction's surface
W is the width of the space charge region.

The capacitances of the fabricated SPAD cells were measured with Agilent 4284 LCR meter in probe station. The results for both FDSOI and STI cells are presented

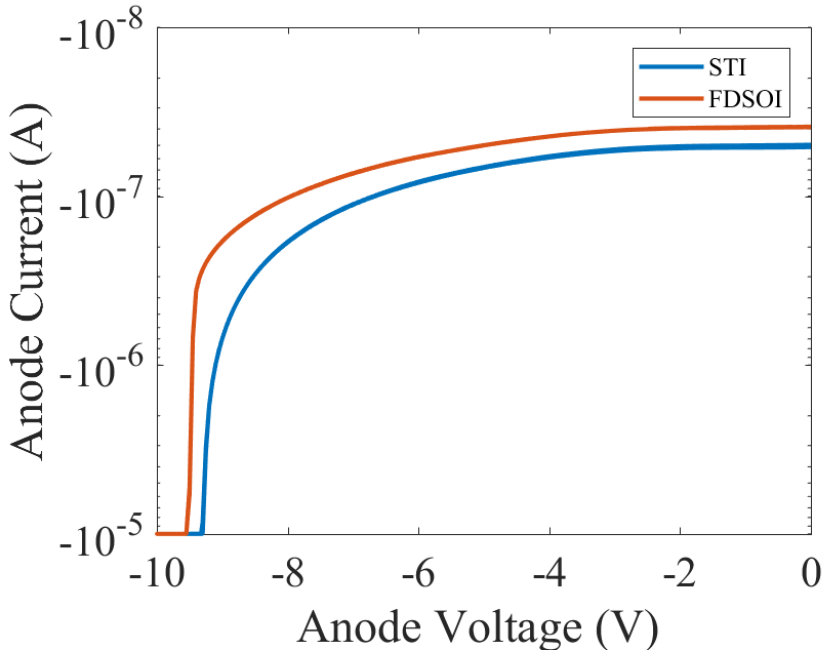

Figure 4.2: *Measured reverse characteristics for octagonal SPAD diodes integrated in FDSOI and STI zone (under illumination).*

in Fig. 4.3. As can be observed, the values increase with the size of the cell for all cases. Another interesting fact checked is that STI cells present slightly more elevated capacitance values, which can be easily explained by the fact that those junctions are more abrupt (cf. Section 3.1.2), which makes the value of W_n lower for such cells and implies then a higher capacitance.

It should be noted that, for circular cells, the values of the capacitances do not increase proportionally to the diodes' surfaces, because the contribution of parasitic capacitances is not negligible for those measurements.

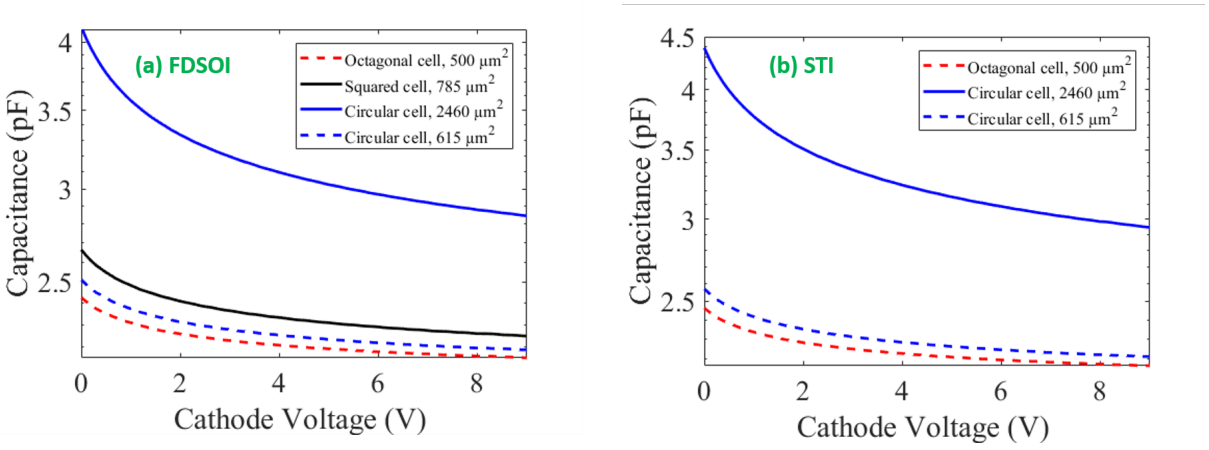

Figure 4.3: *Measured Capacitance for a SPAD diodes integrated in: (a) FDSOI; (b) STI.*

4.3 Dark Current

In order to better understand the physical phenomena involved in the proposed SPAD cells, the variation of dark current according to temperature can be evaluated [3], [4].

In Fig. 4.4, it is possible to observe the Arrhenius plot for Dark Current for FDSOI and STI cells. Due to the small junction area in most of our SPAD, Dark Current could only be measured in circular cells with 2460 μm^2 surface. For the other cells, the measured values are in the same order of magnitude of the sensitivity of the measurement equipment, which cannot be taken into account. The values of dark current were taken at a voltage corresponding to 80% of the value of breakdown voltage for each temperature.

In order to calculate the activation energy (extracted from the slope of the curves), only the measured values bigger than 100 fA (minimum value possible to measure with accuracy) were considered. The activation energies are around 0.33 and 0.20 eV (for FDSOI and STI, respectively). Such values indicate that the dark current does not vary much in temperature. Indeed, this value is placed between the midgap and zero, which in turn indicates a strong presence of B2B and/or TAT effects [4]–[6], which is not satisfactory for an optimized SPAD operating condition.

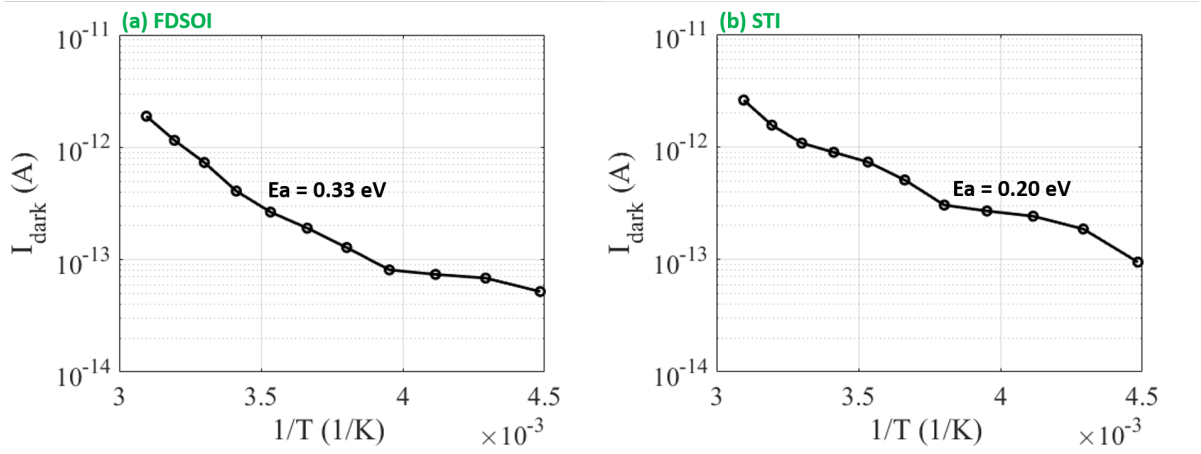

Figure 4.4: *Arrhenius plot for dark current in (a) FDSOI and (b) STI cells. The small slope indicates a predominance of Band To Band and Trap Assisted Tunneling effects. The current values were extracted at 80% of the breakdown voltage.*

4.4 Breakdown Voltage According to Temperature

Temperature tests are usually employed to distinguish between zener and avalanche breakdown, because Zener mechanism (based on band-to-band tunneling) has negative temperature coefficient, while avalanche breakdown voltage increases with temperature [1], [2], [7]. In order to perform such tests, the Keithley 4200 Semiconductor Analyzer was coupled with a cryogenic probe station, where the chips

have been placed, allowing the accurate control of temperature (in this case, from −50 °C up to 50 °C, with a 10 °C step).

For the octagonal FDSOI and STI cells, these curves are presented in Fig. 4.5. Avalanche signature is verified for both, with positive slopes dV_{BD}/dT equals 6.10 and 5.93 mV K^{-1}, respectively. Similar results were obtained for SPADs implemented in technologies with abrupt junctions, such as 65 nm [8], where a slope of 5.25 mV K^{-1} was measured. As discussed in the previous section, the integration zone is the only design parameter influencing I-V curves (including breakdown voltage values). Moreover, the results obtained in TCAD simulation with Okuto-Crowell model represent a good fit of this characteristics, as presented in Section 3.3.1.

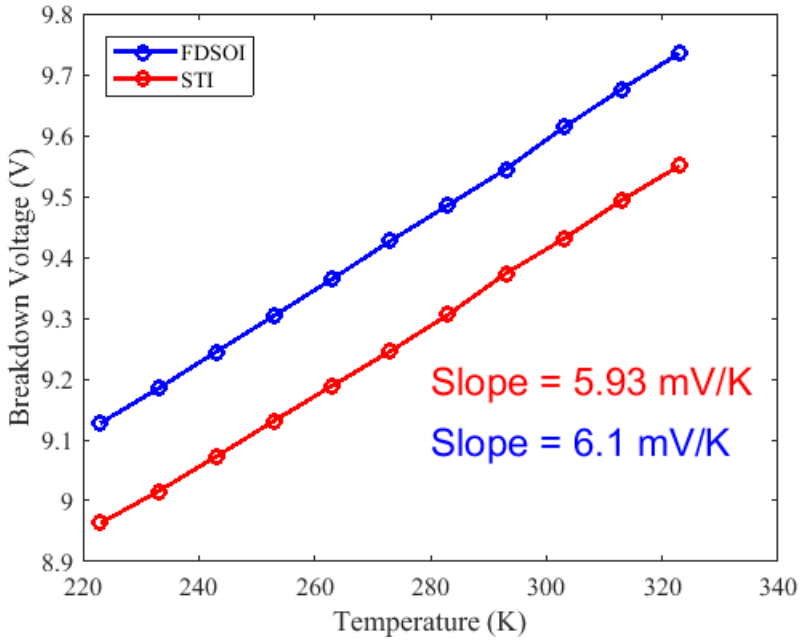

Figure 4.5: *Measured breakdown voltage evolution according to temperature, for octagonal SPAD diodes integrated in FDSOI and STI zone.*

4.5 Electroluminescence Response

Visible light emission from reversed-bias PN junctions in silicon was first observed by Newman [9]. Since then, it is well known that when biasing a diode at breakdown voltage (or over this value), a large spectrum (from 350 nm to 1.7 µm) is radiated, due to the presence of hot carriers (electrons and holes with high kinetic energy, due to high electric field) [10]–[12]. The luminous spots observed in these situations occur where avalanche is triggered. They are directly related to the electrical field magnitude, providing a microcartography of the electrical field, and thus being very useful for detection of Premature Edge Breakdown (PEB) [13], [14].

The experimental setup used for electroluminescence tests is presented in Fig. 4.6. It consists of a voltage source, able to limit current values (avoiding then damaging the

diode, when biasing above breakdown), connected to the PCB that contains the chip under test, and also a high sensitivity camera (Andor Zyla 5.5 sCMOS) [15] coupled with a microscope with magnifying objectives of x50 and x100. All the tests presented here were performed at room temperature. First of all, a reference image is captured with ambient light, when the SPAD had not been biased yet. After that, dark condition is imposed, and the camera is set for an integration time of 5 s (successive frames are integrated for providing a better signal to noise ratio in the image). The diode is then reversed biased at its operating voltage and it emits light. The resulting image is then acquired by the camera.

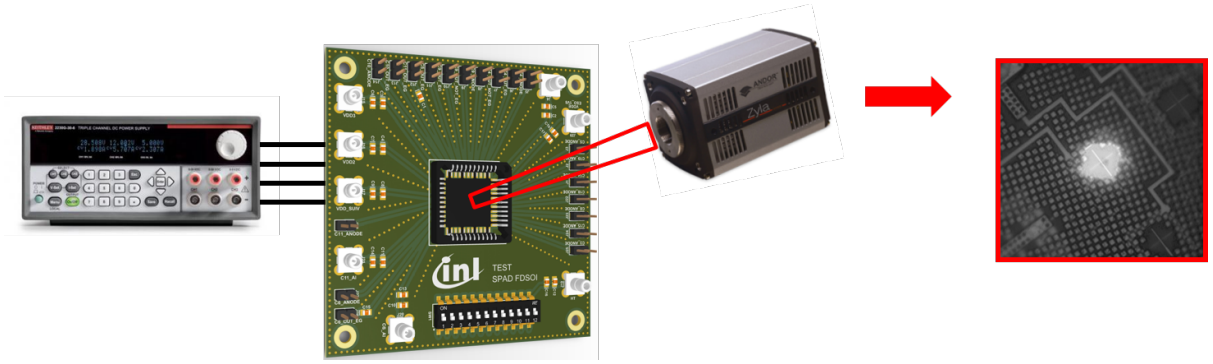

Figure 4.6: *Experimental setup used for electroluminescence tests.*

By varying the reverse bias across the SPAD, the evolution of the electroluminescence response presented by the cell can be evaluated. For an easier analysis, the reference picture (with ambient light and without biasing voltage) is superposed with the dark ones, in post-processing. The resulting image clearly shows the exact areas where avalanche occurs, indicating if the electric field is well distributed or not.

Let us recall the cross section of the actual fabricated devices, according to the integration zone, in Fig. 4.7.

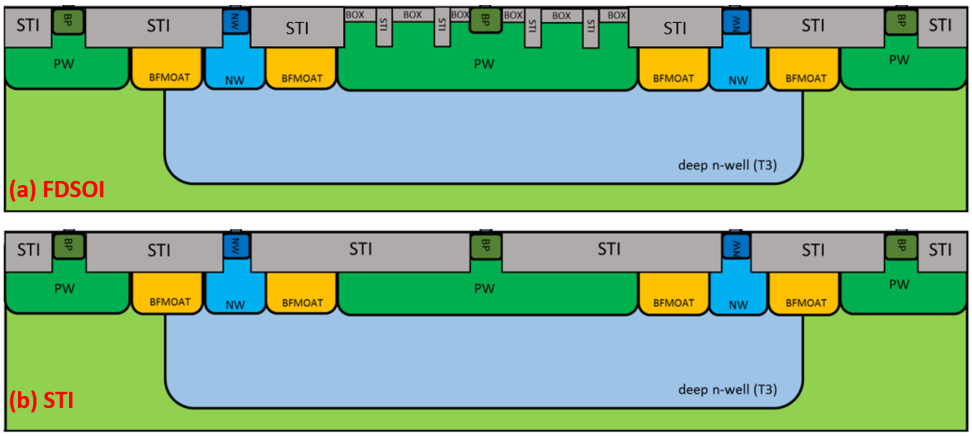

Figure 4.7: *Cross section of the SPADs integrated in (a) FDSOI; (b) STI zones.*

The results of electroluminescence tests for FDSOI cells are shown in Fig. 4.8, 4.9 and 4.10. Current limit was kept constant at 2.5 mA, while applied voltage was increased

up to the voltage value for which the cell is completely lit, situation at which the electric field is spread everywhere in the active region. For all FDSOI cells, Premature Edge Breakdown could be observed, despite the use of a BFMOAT guard ring. This can be explained by the STI layer that exists at borders, due to design rules constraints, through which the implants are done. Indeed, as presented in Section 3.1.2, the PW-DNW junction is more abrupt under STI, which means that their breakdown voltage is lower. Hence, the avalanche process naturally starts at borders for SPAD implemented in FDSOI zone.

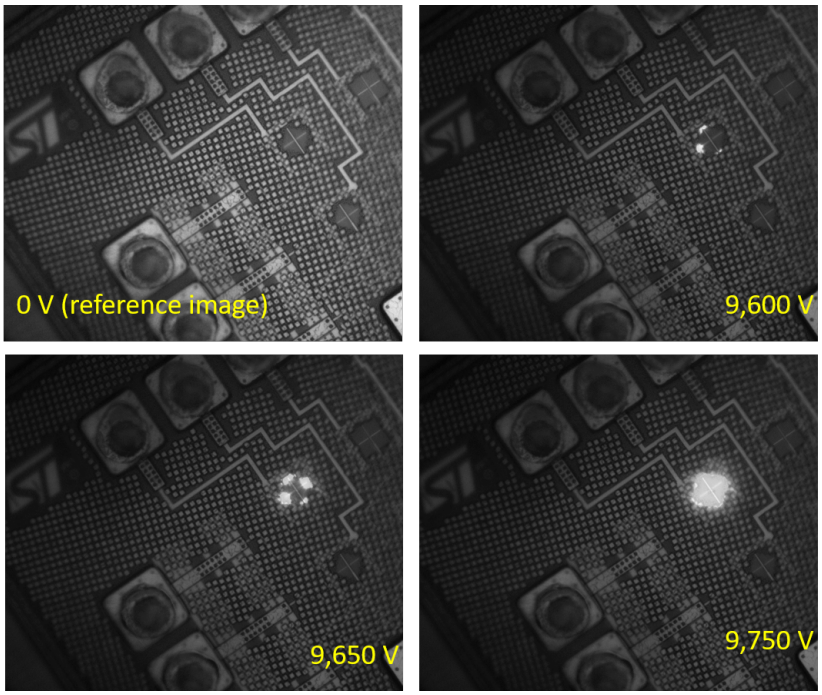

Figure 4.8: *Electroluminescence response for octagonal FDSOI cell.*

The confirmation of such phenomenon can be deducted from Fig. 4.11 and 4.12, where the octagonal and circular STI cells, being completely integrated under a uniform layer of STI, were submitted to the same electroluminescence test protocol. No PEB effect was observed, and the junction breaks at a lower applied voltage, not needing much excess bias for a complete illumination of the cell.

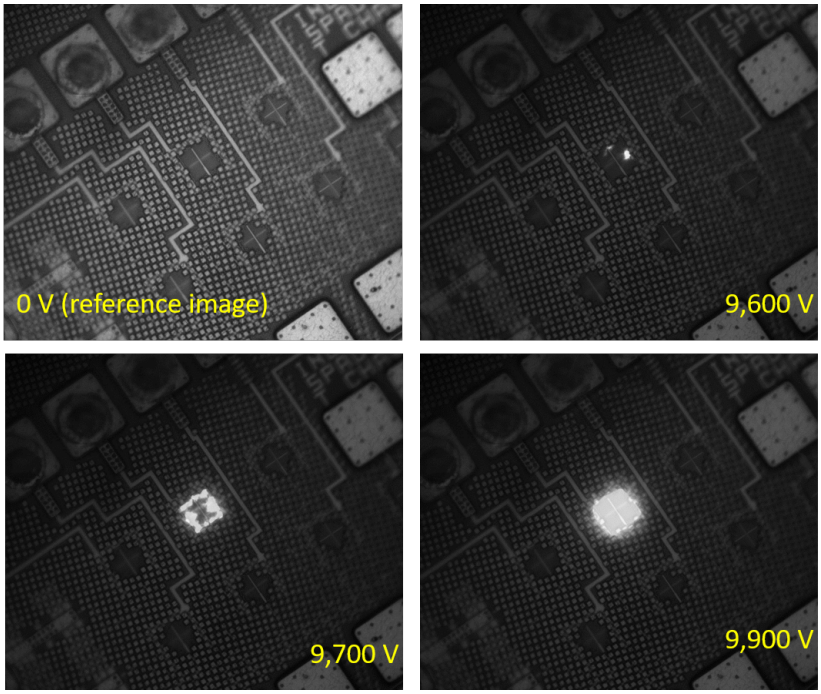

Figure 4.9: *Electroluminescence response for squared FDSOI cell.*

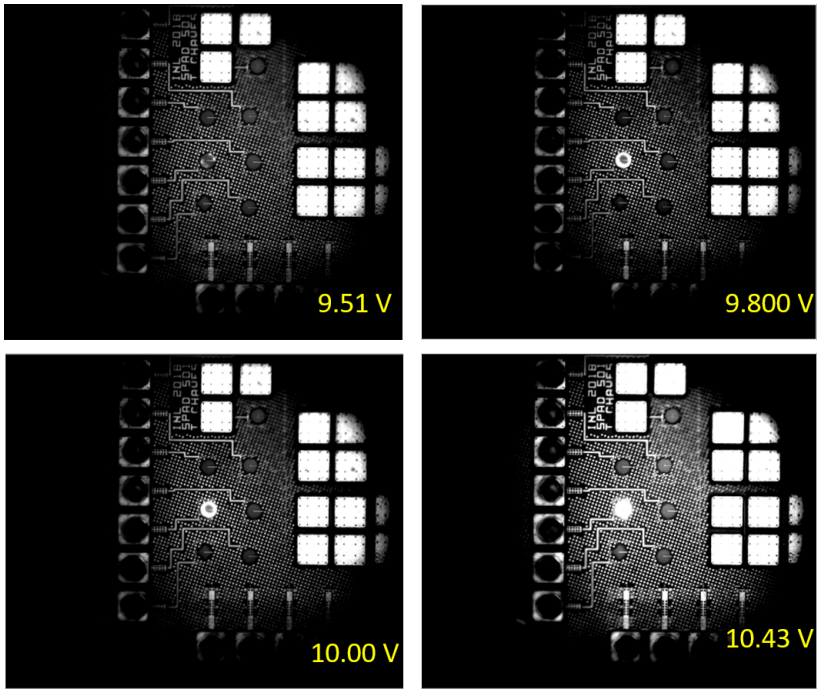

Figure 4.10: *Electroluminescence response for circular FDSOI cell.*

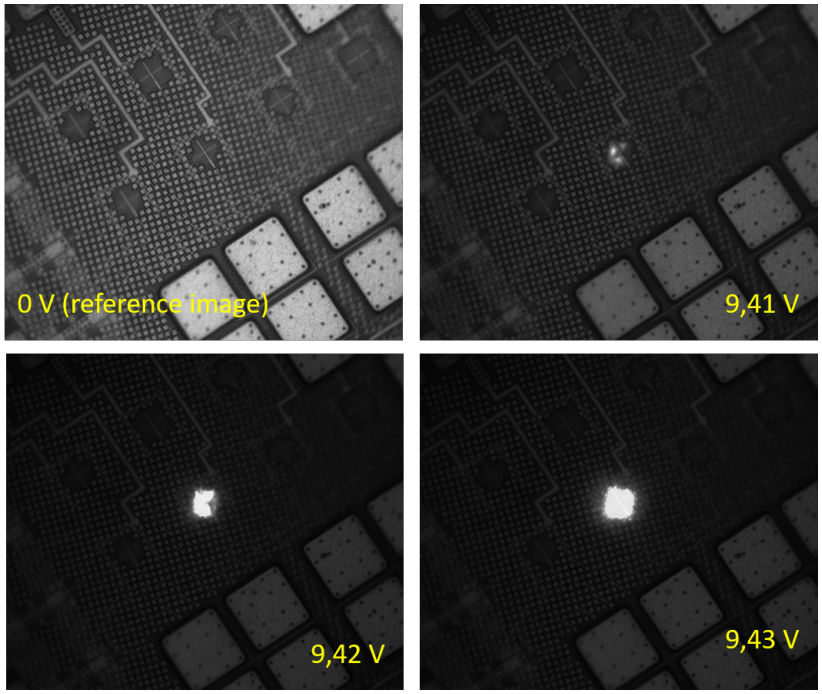

Figure 4.11: *Electroluminescence response for squared STI cell.*

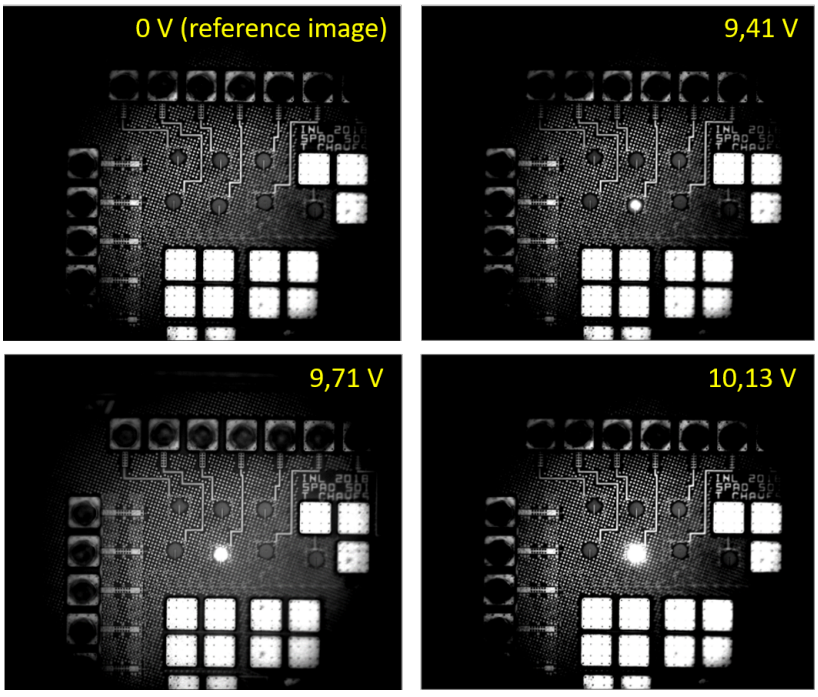

Figure 4.12: *Electroluminescence response for circular STI cell.*

4.6 Dark Count Rate

One of the most important Figure Of Merit (FOM) for SPAD is Dark Count Rate (DCR). It represents essentially the noise presented by the device in dark condition,

i.e., the number of avalanches triggered without an impinging photon. This noise can be produced by several physical phenomena that generate a free carrier in SCR (multiplication region) and start off the avalanche process, such as Band To Band Tunneling (B2B), Shockley-Read-Hall Generation-Recombination (SRH), diffusion current from neutral regions or even charge release from defects between interfaces Si/SiO_2. It is normally expressed in Hz/μm^2, since it also depends on the diode's photo-sensitive area [16].

In order to perform DCR measurements, it is necessary to associate a quench and recharge circuit to the SPAD, so the device won't be damaged and a new detection can be done once the avalanche is extinguished. Unfortunately, in our final layout, the internal quenching circuits were connected to SPAD cells with a sensing circuit in which misplaced antenna diodes were present, as explained in Section 2.4.3, making these cells dysfunctional. Therefore, for DCR measurements, an external PQC (resistor) was connected to the anode, thanks to a dedicated PCB. Cathode was biased at a constant $V_{BD} + V_{ex}$ voltage. The experimental setup is shown in Fig. 4.13.

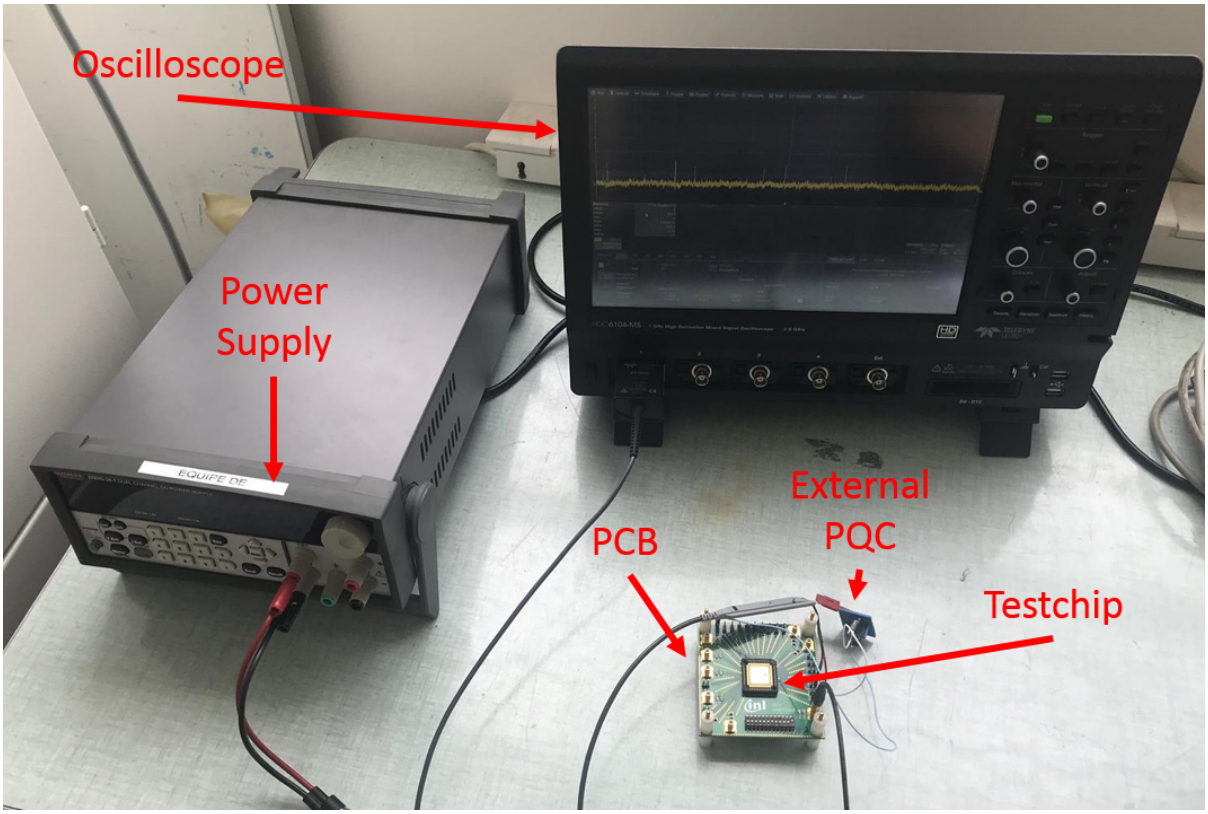

Figure 4.13: *Setup for DCR measurements. During the measurements, evidently, the PCB was covered, so the dark condition could be reached: a top cover from original packaging was kept closed, under a dark foam sheet. The PCB was then placed in the thermal cage, whose glass window was also covered by black curtains, guaranteeing dark conditions for measurements.*

It was possible to directly measure, with a wide-band oscilloscope [17], the transient voltage rise across the quenching resistor with spike-like signal corresponding to the avalanche events, as shown in Fig. 4.14. Statistical extraction of the DCR was carried out by counting the number of events for a fixed time window in which the voltage

spikes exceeded a fixed threshold voltage.

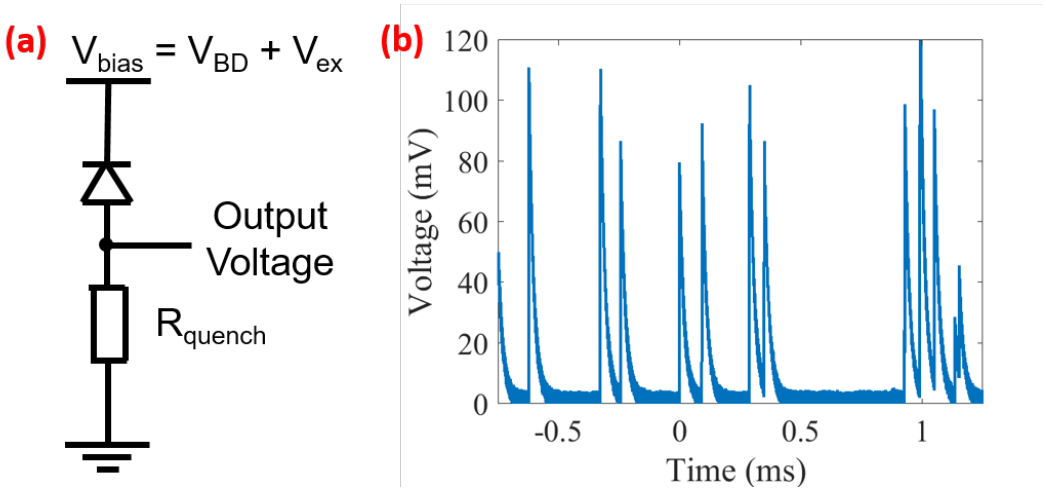

Figure 4.14: *(a) Schematic of circuit used for DCR measurements; (b) Output voltage at anode, with the image of the current through SPAD. Each spike corresponds to an avalanche event [18].*

By varying the excess voltage V_{ex} and also temperature (from −40 °C up to 50 °C, with a 10 °C step), thanks to a thermal cage in which the PCB was inserted, average measured DCR for cells with standard doping (no DNW modification) was plotted in curves presented in Fig. 4.15, for octagonal FDSOI and STI cells. An external quench resistor of 200 kΩ was used for both. For each average DCR value, around 3000 acquisitions were done for a fixed 2 ms time window.

The evolution of DCR when V_{ex} is increased, for a fixed temperature, is presented in Fig.4.15 (a) and (c), respectively for FDSOI and STI. It is possible to notice a linear evolution initially, but around $V_{ex} = 0.25\ V$, saturation occurs, due to pile-up. This effect is due to the external quenching with large parasitic capacitances values, which produce a long recharge time constant (around 20 µs) that does not allow increasing the excess bias above 0.3 V [18]. Indeed, pile-up effect can happen when carriers are generated in dark condition during reset time. The device not being biased at the proper excess voltage, avalanches are not triggered and some events are not detected, resulting in the saturation phenomena observed.

The Arrhenius plot at fixed excess voltages, for both cells, can be observed in 4.15(b) and (d), respectively. The activation energies E_a extracted from the slopes of such curves are an indication of the main phenomena involved in the SPAD structure that generates avalanche [4]–[6], in a similar way of the evaluation of dark current. The very low activation energy values obtained (around 0.1 eV in the presented curves) indicate the predominance of B2B and field-enhanced TAT, confirming the hypothesis elaborated from the low values of breakdown voltage, naturally present for an abrupt junction.

In general, STI cell is noisier, because, as discussed in Section 3.1.2, implants are done through STI physical layer, which makes the junction more abrupt. Naturally, the higher the doping, the higher the B2B generation rate. In terms of DCR values, this difference could be clearly observed in the measurements, confirming the results obtained in TCAD study.

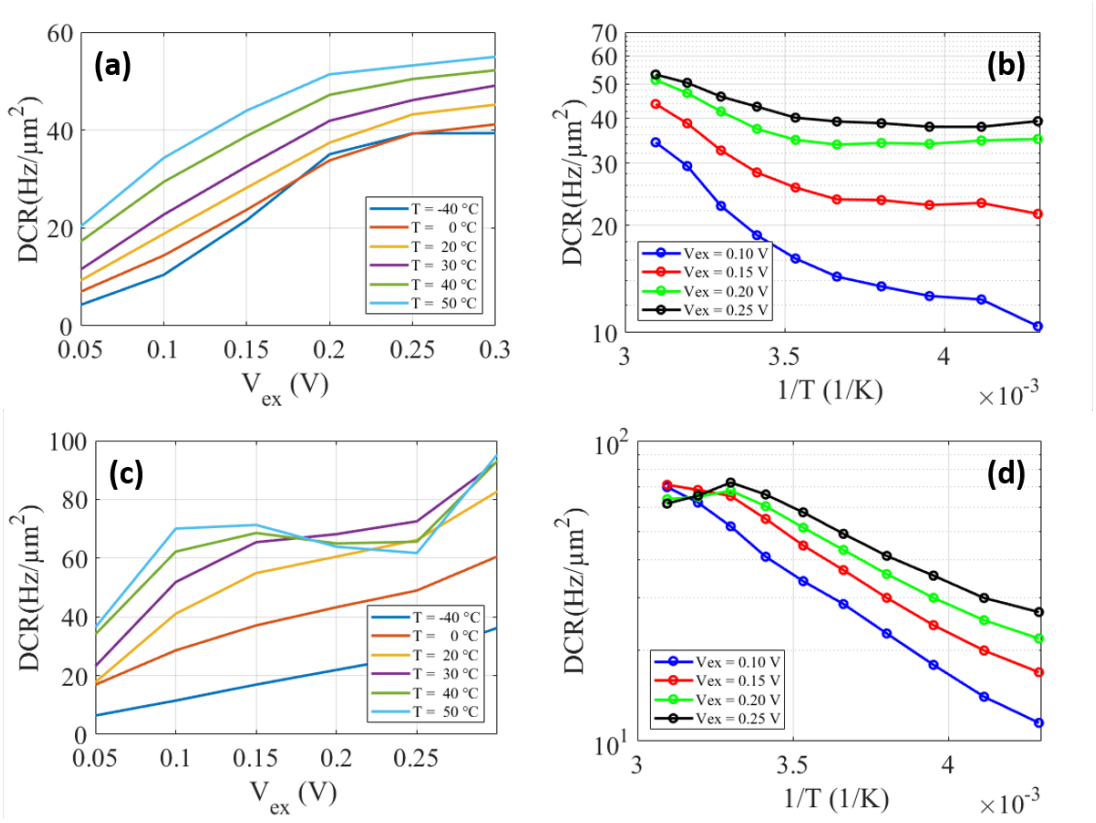

Figure 4.15: *DCR measurements for octagonal cells: (a) and (b) FDSOI; (c) and (d) STI cells.*

An active probe (with lower input capacitance of a few pF) was also used for new DCR measurements. A comparison between the results obtained with two different probes is presented in Fig. 4.16 (a). Since it presents a much smaller capacitance value, it naturally reduces recharge time τ, so it takes less time for the SPAD to recharge to its total applied voltage $V_a = V_{BD} + V_{ex}$ value. Considering that Avalanche Triggering Probability (ATP) highly increases with voltage, it is normal to have more DCR, including also a higher afterpulsing contribution, increased due to the shorter recharge time τ (Fig. 4.16) (around 800 ns, as shown in Fig. 4.17). Similar results can be obtained with smaller values of resistance, as shown in Fig. 4.16 (b). An external buffer cell was also implemented, but without any successful improvement. Despite the huge efforts employed to reduce afterpulsing, the external setup with Passive Quenching Circuit (PQC) still limits V_{ex} to 0.3 V. Even if the values of average DCR are much higher with this new active probe, temperature tests confirmed that B2B associated with field-enhanced TAT are indeed the dominant phenomena for this SPAD, due to same magnitude range of activation energy, extracted from Arrhenius plot.

The values of measured average DCR are quite elevated for such small excess voltage, when compared to State of the Art SPAD. Nevertheless, since this was a very first integration of SPAD in FDSOI, and the original technology was not at all conceived for such devices, these are promising first results. Similar limitations were obtained in 65 nm bulk technology [8], [19].

It should also be noted that, due to imposed design rules for the C28FDSOI

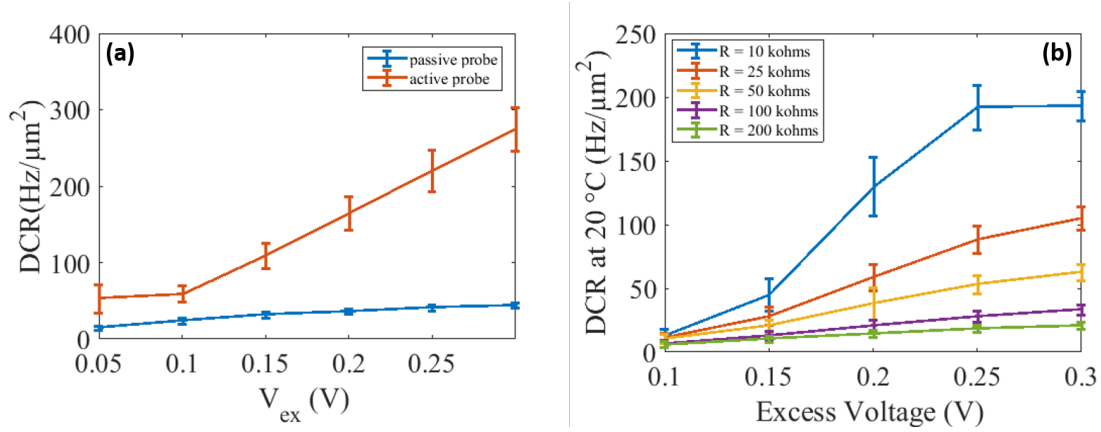

Figure 4.16: *DCR measurements for octagonal FDSOI cell, with: (a) two different probes, same* 270 kΩ *resistance. (b) Different values of ballast resistor, same passive probe. For both, error bars represent the standard deviation for each measured DCR value.*

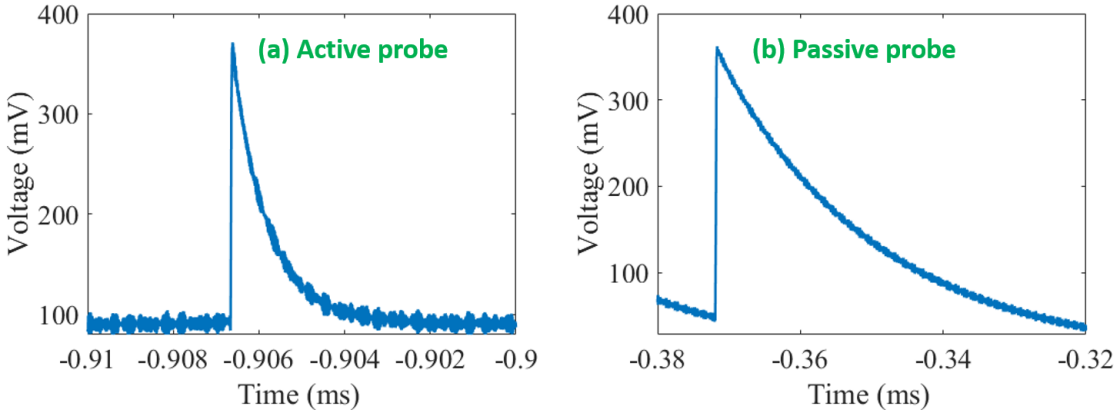

Figure 4.17: *SPAD recharge time (obtained from anode voltage) for (a) active and (b) passive probes, with the same quenching resistor (*270 kΩ*).*

technology, STI is kept at the borders of the active region (see Section 2.4). The interfaces between silicon and silicon-oxide layer are well known for presenting many deep-level defects in their structures [20], [21]. In our case, the SCR is directly in contact with STI, which implies many free carriers injected in the multiplication region, resulting in a very high DCR [22]. A possible solution for this problem would be the the increase of the distance between the STI layer and the SPAD junction, but this would require violating design rules. Another possible solution adopted in [20] is to add several passivation implants around STI (as shown in Fig. 4.18), creating regions considerably more doped around STI. This approach would drastically decrease the chance of free carriers in those regions being dragged into SCR. This solution obviously require major technological modifications and seems more complicated than the previous one.

As presented in Section 1.4.2, PQC are very useful when it comes to initial characterization and selection of SPAD, because of its simple implementation, effectively enough for low or moderate counting. However, in order to fully test SPAD up to its

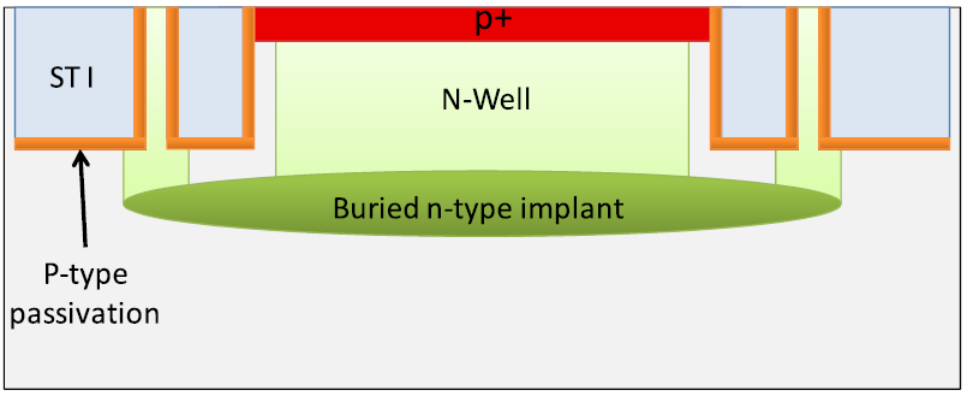

Figure 4.18: *SPAD proposed in [20], with STI guard ring surrounded by multiple p-type implants, for reducing the probability of free carriers from the interface infiltrating SCR and then triggering dark counts.*

intrinsic physical limits, Active Quenching Circuit (AQC) are needed, because they allow a reduction of the amount of charges through the diode. Also, an active recharge allows controlling the dead time and, thus, quantifying afterpulsing [23].

Furthermore, a reduction of B2B and TAT generation can reduce DCR. For C28FDSOI SPAD, these parameters are quite important, since it has been demonstrated that they are the most important generating processes for the fabricated structure. In order to reduce the influence of this mechanism, one of the possible approaches is to smooth the doping profile of the junction and, thus, increase breakdown voltage, as proposed in Section 3.1.2 and studied in the following section.

4.7 Modified Deep N-well

As precised at section 3.1.2, by means of TCAD simulation, a modified version of the Deep N-well (DNW) with reduced doping levels, can improve SPAD performances by providing a smoother junction, and, as a consequence, a higher breakdown voltage, lower B2B and TAT generation rates and expected lower DCR. With the agreement of STMicroelectronics, a dedicated wafer was submitted to the modified DNW implant proposed in the aforementioned section. The same measurements were performed for this updated version of the cells and the results are presented in the following sub-sections.

4.7.1 I-V Curves

In Fig. 4.19, the direct characteristics for the new SPAD are presented. As in the precedent version, the surface of the junction is the only parameter having an impact on the direct curve. The ideality factors here are 1.19 and 1.11, respectively for the circular FDSOI cells with 2460 and 615 μm^2 areas.

Concerning reverse I-V curves, they are presented in Fig. 4.20. It was possible to notice an increase in breakdown voltage for all temperatures, indicating that the new

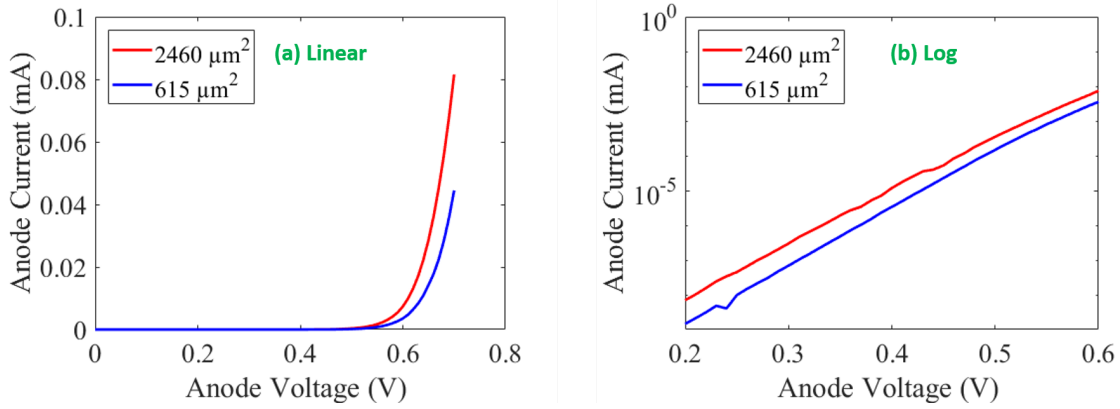

Figure 4.19: *I-V direct curves for SPAD cells implemented in FDSOI zone (a) linear scale; (b) Log scale.*

junction is less abrupt, as predicted in TCAD simulations (Section 3.3.1).

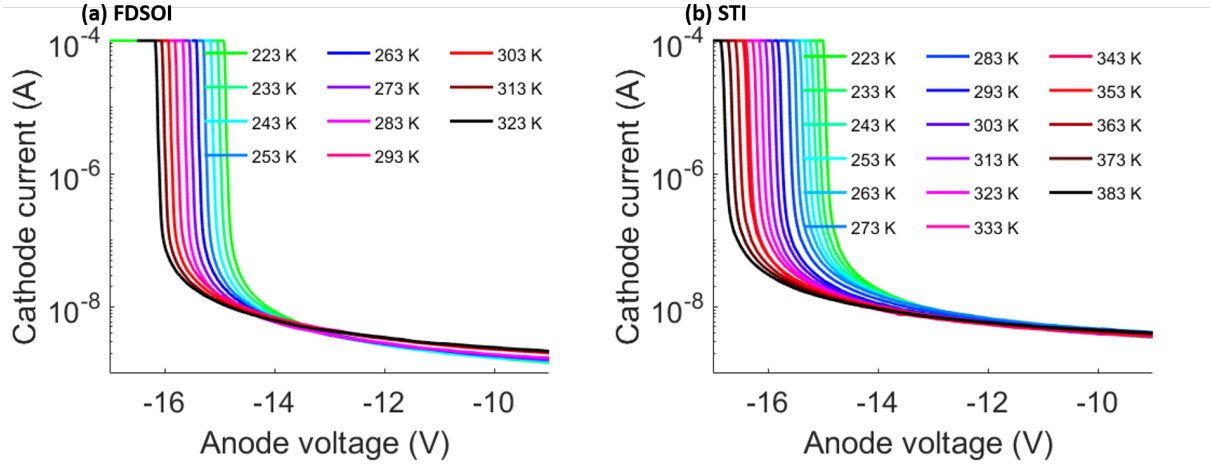

Figure 4.20: *Reverse I-V curves (under illumination) for SPAD cells in a customized deep N-well implant configuration: (a) FDSOI; (b) STI.*

Some other promising results could be measured, such as the dark current, presented in Fig. 4.21. From the curves, it is possible to notice a general reduction of the current values, when compared to the original structure. Again, the values below 100 fA should not be taken into account, because they are at the same order of magnitude of the minimum value possible to measure with the available equipment. For the values bigger than this threshold, the activation energy was extracted: E_a = 0.52 and 0.59 eV (for FDSOI and STI, respectively), representing a dominance of SRH mechanism. All values for dark current were extracted at a 80% of their corresponding breakdown voltage.

For both cells, these results represent a big difference with respect to the original SPAD, in which only a combination of B2B and TAT could be observed. The experimental results confirm then the TCAD simulation prediction for these analysis.

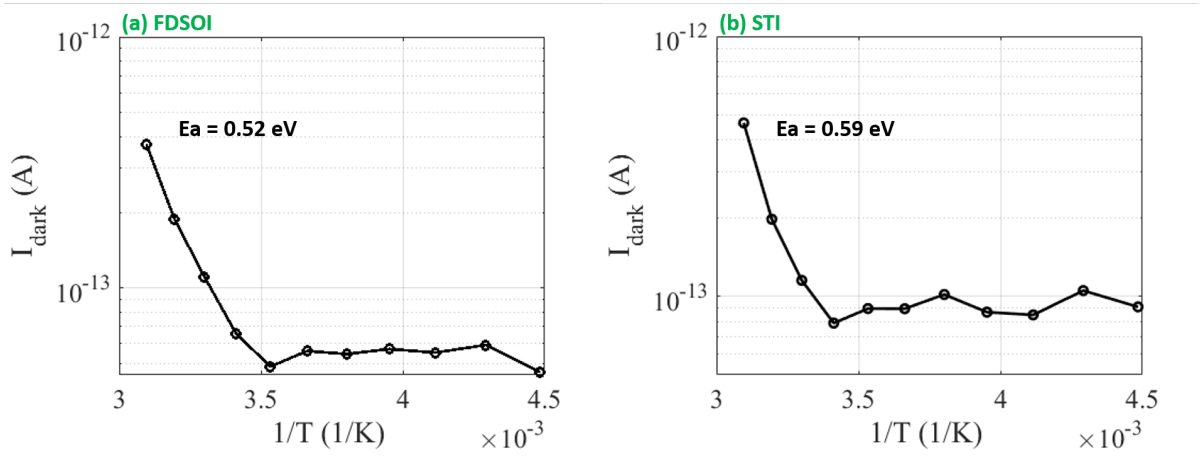

Figure 4.21: *Arrhenius plot for dark current for (a) FDSOI and (b) STI cells with modified DNW. The current values were extracted at 80% of the breakdown voltage.*

4.7.2 C-V Curves

For this new version of Deep N-well (DNW), with customized implant, the C-V curves were also measured (Fig. 4.22). A decrease in the values of capacitance is observed (Fig. 4.23), which is normal for a less doped junction. Indeed, when decreasing doping, the width of SCR is increased, and the capacitance is then reduced. The difference between the capacitance of cells integrated in STI and FDSOI for this new version is almost negligible, being mostly due to the parasitic capacitances.

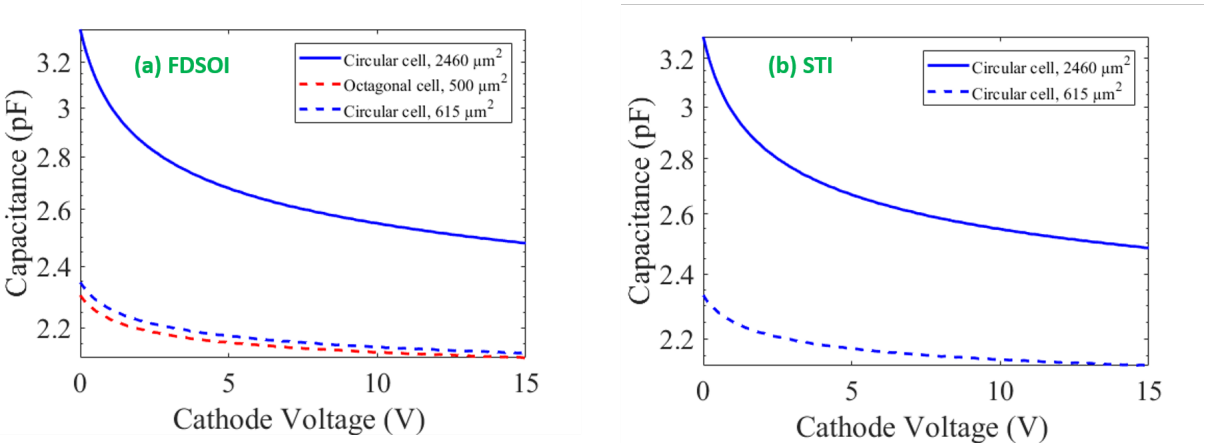

Figure 4.22: *Measured Capacitance for SPAD diodes integrated in a customized DNW implant in: (a) FDSOI; (b) STI.*

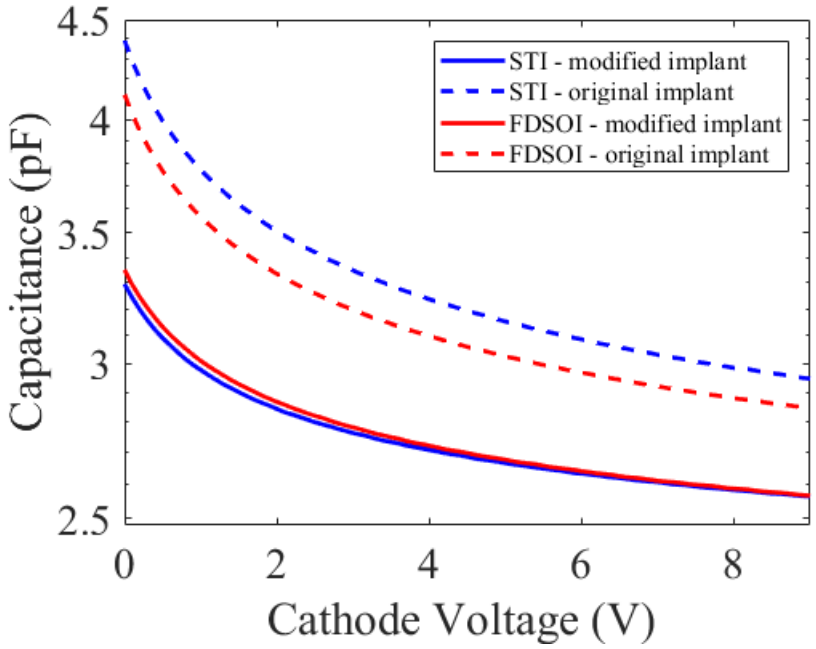

Figure 4.23: *Comparison between capacitance values for the circular cells with* 2460 μm^2 *integrated in FDSOI and STI for the original and proposed deep N-well doping profiles.*

4.7.3 Breakdown Voltage According to Temperature

The breakdown voltage according to temperature for these new devices is presented in Fig. 4.24. As can be observed, the breakdown voltage has increased in about 6.5 V, when compared to original technology, as predicted in TCAD simulations. At room temperature, V_{BD} = 15.92 V. Here, the slope of the curve is 11.6 mV/K, which is in agreement with TCAD results (9.16 mV/K) obtained with Okuto-Crowell model [24]. Due to timing constraints, the results, even representing a fair enough approximation, were not optimized, so other models should be tested, and simulation parameters should be studied.

4.7.4 Electroluminescence Response

The same electroluminescence tests were performed for this new version of the circuit. The results are shown in Fig. 4.25 and 4.26. Apart from the new values of breakdown voltage, not much difference could be observed, which means that the new doping profile does not have much impact in electric field distribution. Premature Edge Breakdown (PEB) was still detected for FDSOI cells, since STI is still present at the borders of the junction, as discussed previously (Section 3.1.2).

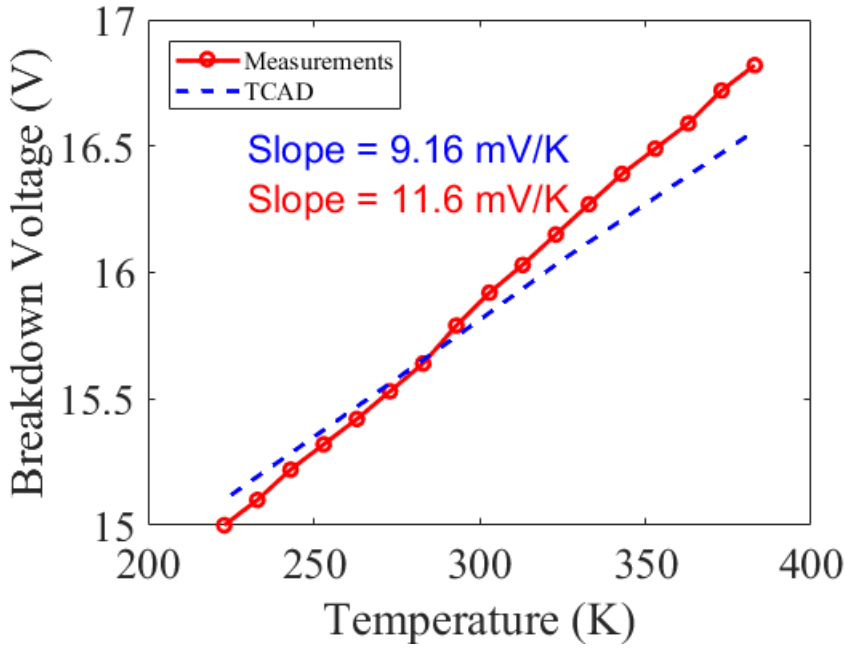

Figure 4.24: *Breakdown Voltage according to temperature for SPAD with modified implants. The increase predicted in TCAD simulation was confirmed by the measured results.*

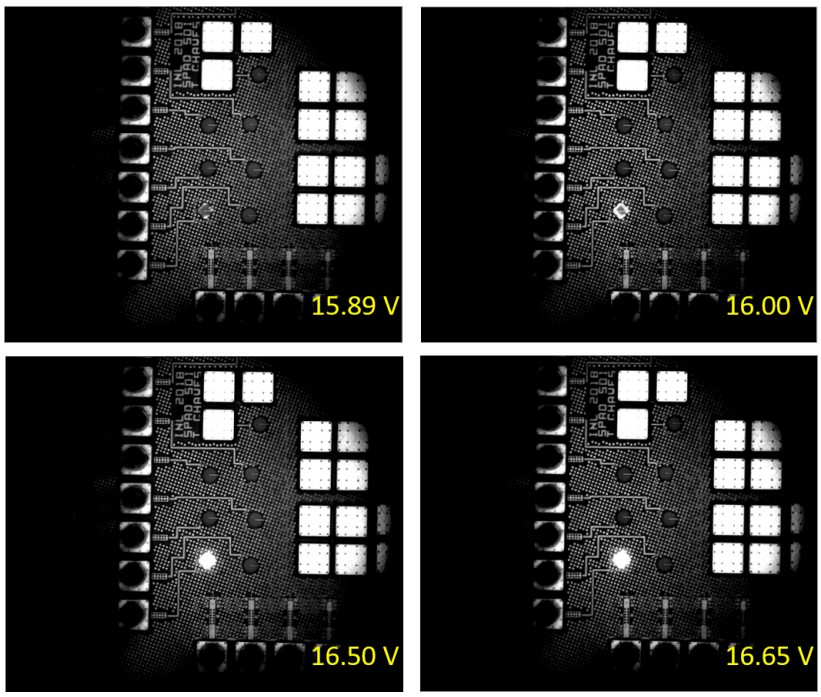

Figure 4.25: *Electroluminescence response for octagonal FDSOI cell, with dedicated implant.*

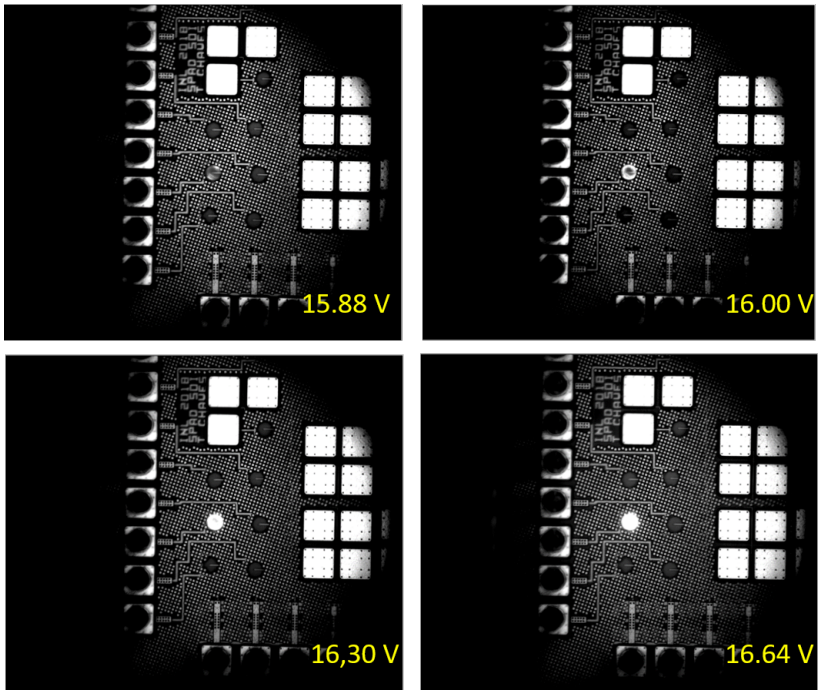

Figure 4.26: *Electroluminescence response for circular FDSOI cell, with dedicated implant.*

4.7.5 Dark Count Rate

As observed in the precedent sections, the new junction is indeed less abrupt, since breakdown voltage was increased and capacitance was reduced. Nevertheless, when measuring DCR for the new devices, not much difference was observed when applying reverse bias above breakdown: the high levels of DCR for low excess voltage did not seem to change (Fig. 4.27). Pile-up effect can also be seen for these new measurements, which could be improved by using active recharge.

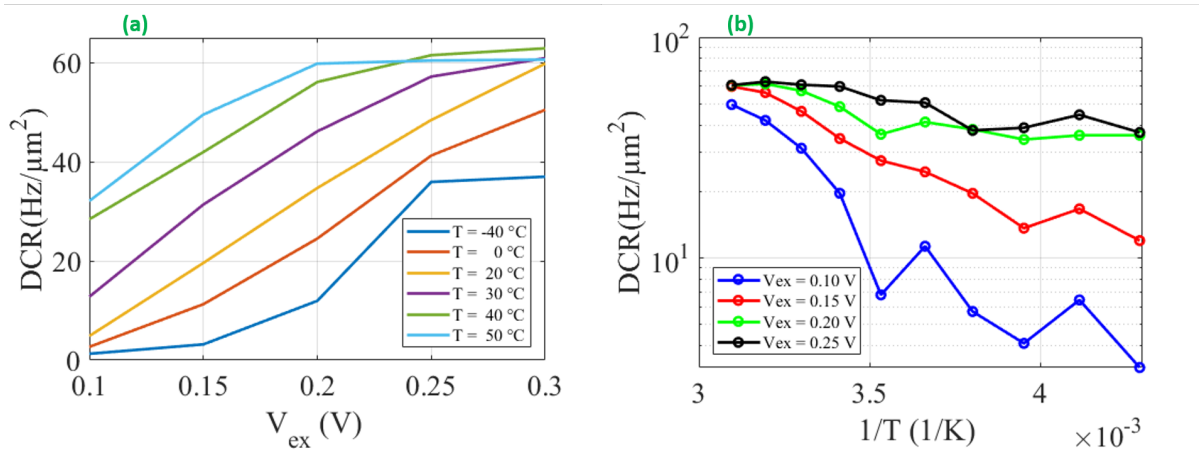

Figure 4.27: *DCR measurements for octagonal FDSOI SPAD.*

Actually, the initial idea of modifying the implants to make a smoother junction

came from the attribution of Band To Band Tunneling (B2B) generation rate to the high measured DCR. However, the new junction did not seem to provide better DCR. Another hypothesis was then formulated, by associating the high levels of DCR to the traps presented in the interface between silicon and silicon-oxide (STI in our case), that actually are directly in contact with the SCR, due to imposed design rules. In agreement with STMicroelectronics, another version of the circuit (to be characterized) has less contact between the STI layer and the SPAD junction. A better DCR is then expected, which would enable measuring Photon Detection Probability (PDP), so far impossible due to the huge pile-up effect even for small excess voltages.

4.7.6 Afterpulsing Probability

In order to estimate afterpulsing probability in SPAD, the so-called histogram method can be used [25]–[27]. It consists in observing the output signal of the SPAD with an oscilloscope and measuring the time interval elapsed between two pulses, as shown in Fig. 4.28.

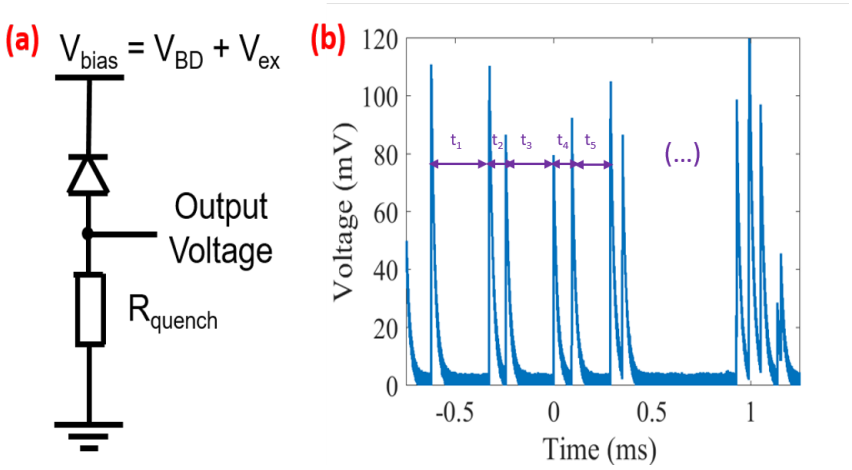

Figure 4.28: *Afterpulsing probability measurement: (a) Schematic of experimental setup. (b) Time delay measurement between spikes.*

A histogram is then made with these data. When only primary DCR is present, the delays are generally bigger than 1 µs at room temperature and the histogram follows an exponential distribution. When afterpulsing is present, i.e., region in the histogram corresponding to short time delays, there are more counts than the predicted values in the exponential distribution, as shown in Fig. 4.29. One can extrapolate the exponential distribution curve for shorter delays and identify the extra counts generated by afterpulsing events. The afterpulsing probability is then calculated as the ratio of the area between the two curves to the surface under the experimental one [27].

The test chip with dedicated implants was then used for measuring this characteristic. The histogram of measured time delays was plotted and then an exponential fit was done for values bigger than 1 µs, as shown in Fig. 4.30. As can be observed, the number of measured counts below threshold value of time was lower than the estimation provided by the fit. This can be explained by the long recharge time, due to

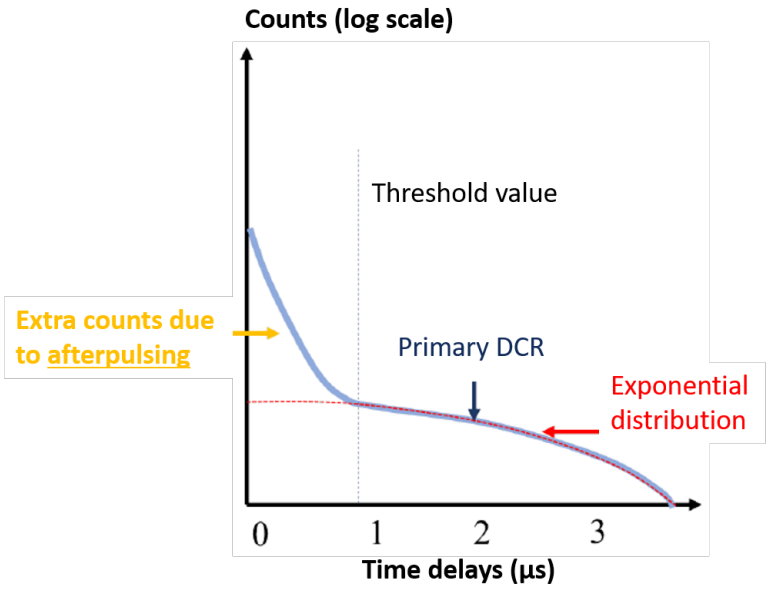

Figure 4.29: *Histogram method for estimating afterpulsing. Adapted from: [27]*

the use of passive external circuitry. A proper active circuit should make afterpulsing probability measurable.

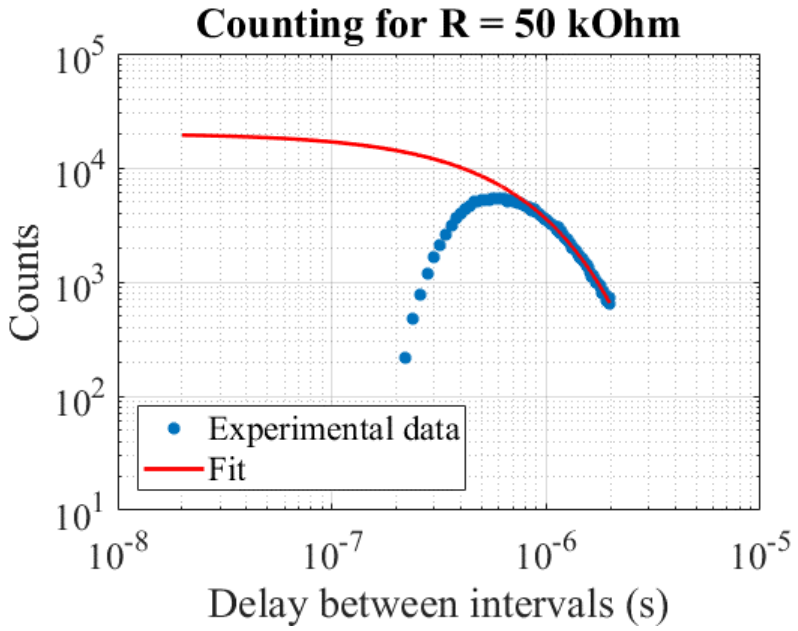

Figure 4.30: *Histogram for measured time delays between output pulses. A* 50 kΩ *ballast resistor was used as quenching circuit.*

4.8 Indirect Avalanche Sensing in FDSOI

One of the most impressive features of C28FDSOI is the back biasing effect. Indeed, this trait can be conveniently explored in SPAD implemented in C28FDSOI, since avalanche could be easily detectable without any need of electric contact, as explained in Section 2.4.2. A resistive divider was implemented both for probe station characterization (for static tests) and over the SPAD in a FDSOI zone (over BOX), for dynamic analysis, as shown in Fig. 4.31.

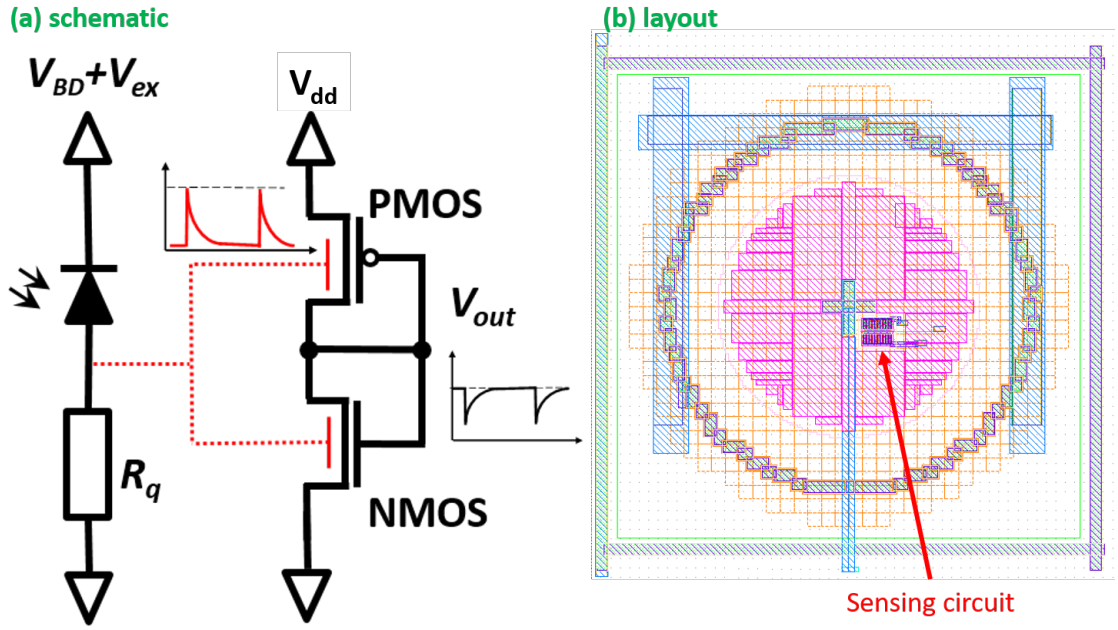

Figure 4.31: *Sensing circuit, composed by a RVT NMOS and a LVT PMOS, in a voltage divider configuration, where the output voltage varies with avalanche events, thanks to body biasing effect: (a) Schematics; (b) Layout [28].*

As previously stated, with C28FDSOI technology, the concept of body-biasing allows to modulate the transistor properties, changing its threshold voltage V_{th} to obtain high performance or low leakage devices. Thanks to this capacitive coupling between the P-well (i.e., SPAD anode) and the transistor channel separated by the ultra-thin BOX, an indirect detection or sensing of the SPAD-FDSOI avalanche events is possible. The transistor threshold voltage V_{th} will change according to the SPAD anode voltage fluctuations (P-well layer) [28].

The anode voltage varies from 0 (standby state) to a maximum value of around V_{ex} (when an avalanche occurs). As the CMOS buffer cannot tolerate an input voltage larger than V_{dd} (e.g. 1.8 V), the excess voltage V_{ex} range is also limited to V_{dd} (limiting thus PDE), except if cascode transistors are used. With this indirect sensing feature, it is no longer necessary to physically connect the avalanche detection circuitry to the SPAD anode. Furthermore, the excess voltage range is no more limited to V_{dd}.

For static characteristics, the variation of the drain current, as well as the output voltage, was plotted according to V_{dd} for the circuit implemented with thick gate oxide

(called "eg transistors"), as shown in Fig. 4.32. The simulation results are obtained with SPECTRE simulator and the calibrated models available in the PDK. The difference between simulation and measurements results, especially for V_{dd} lower than 0.5 V, can be easily explained by the low current flow, that does not allow the divider to work properly for such values of applied voltage. The back biasing voltage was kept at zero for this initial characterization.

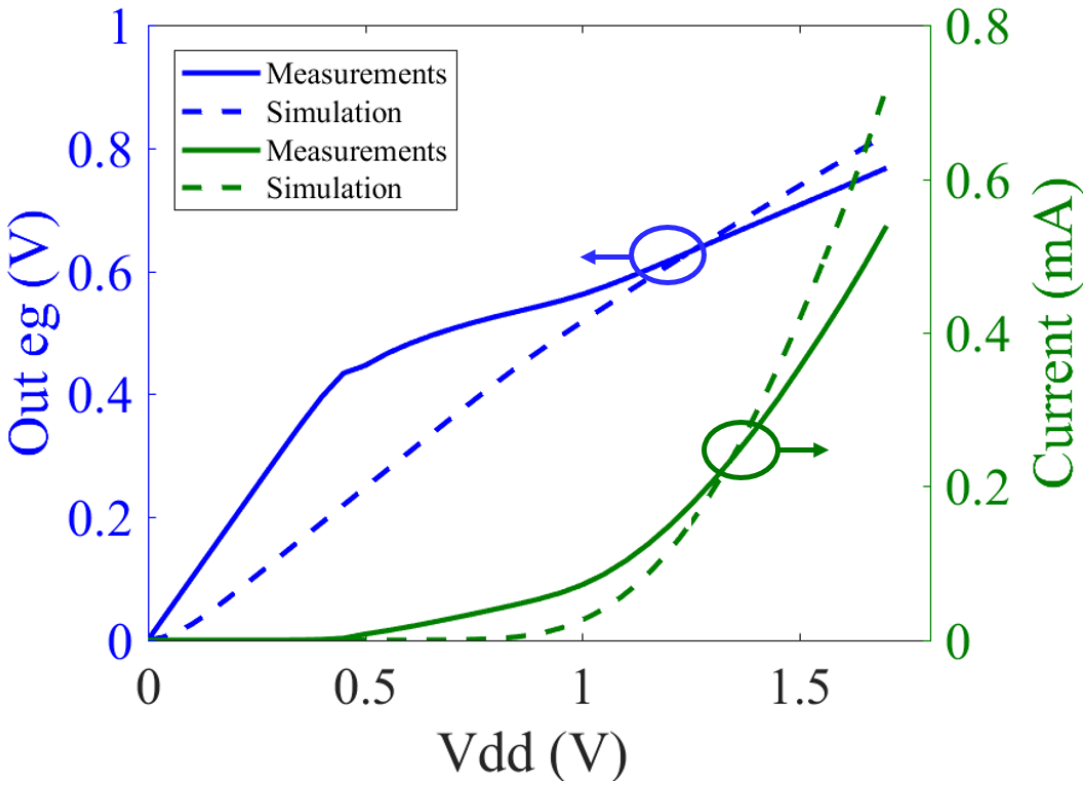

Figure 4.32: *Static characterization of sensing cell with eg-type transistors, at* $V_{bb} = 0$ V.

In Fig. 4.33, V_{dd} is kept constant at 1.7 V, while V_{bb} is varied. The Back-biasing effect can be easily observed with the slopes V_{out}/V_{bb} that present a value of around −140 mV/V, for both simulation and measurements. The vertical shift observed between the experimental and simulated curves can be justified by a slight difference in V_{dd} voltage biasing during measurements, as well as transistor variability (here large transistors ($W = 10\,\mu$m and $L = 150$ nm for both PMOS and NMOS) are used for a direct acquisition of the output with an oscilloscope).

The use of the voltage divider for demonstration of the indirect detection concept, although effective, presents a natural (direct) sensitivity to the variation of the supply voltage. With respect to process variations (SS FF SF FS) and temperature (−40 °C to 120 °C), the simulations give a relatively constant sensitivity factor of (142 ± 8) mV/V and an output voltage of (790 ± 65) mV at zero back-biasing voltage. Under these conditions, the voltage divider circuit will be robust only for high excess voltage, to compensate for the offset of the operating point. It may be noted that a more complex detection circuit will make possible to obtain better robustness to PVT variations (for

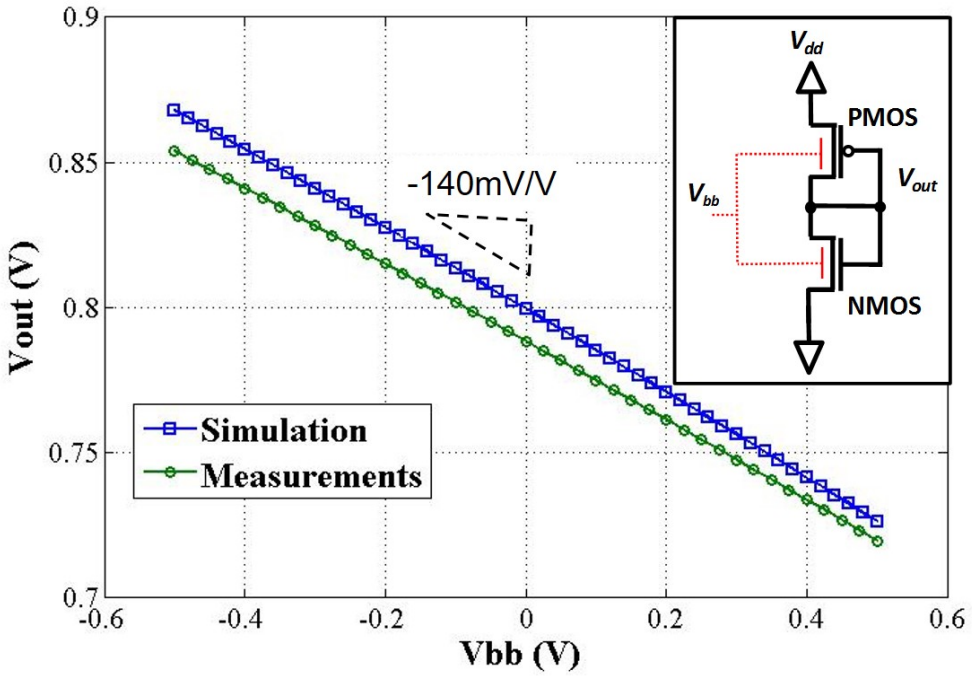

Figure 4.33: *Static characterization of sensing cell with eg-type transistors. The back-biasing voltage is varied here, while V_{dd} is kept constant at* 1.7 V *[28].*

example differential circuitry) [28].

The sensing circuit was also characterized during SPAD operation, as shown in Fig. 4.34, by measuring simultaneously the anode voltage and the output of the indirect sensing circuit for several avalanches (here the avalanches correspond to dark events). The proposed indirect sensing allows avalanche event detection at excess bias voltages as low as V_{ex} around 0.2 V.

The average relative magnitude of the spikes V_{out}/V_{anode} is around 140 mV/V, which is consistent with the static characteristic. The long *RC* time constant of the event is due to the passive quenching with a 200 kΩ ballast resistor associated to the total capacitance of at least 3 pF (SPAD, load, pad, printed circuit board, oscilloscope active probe). It should be noted that the path through the deep N-well may also contribute to the total quenching resistance and therefore leads to an increase of the effective quenching resistance (and thus the *RC* time constant).

The measurement of the time jitter between the two output pulses provided by anode and sensing circuit was also addressed. The results were compiled in the histogram presented in Fig. 4.35. Nevertheless, the measured values (in the order of ns are mainly associated with the external circuitry used, not actually representing the jitter of sensing circuit when compared with anode, that should be smaller.

Another sensing circuit, based on the equivalent capacitor divider, presented in Section 2.4.2 (Fig. 4.36), was tested by means of SPECTRE simulation, although it was not physically implemented. Simulation results are presented in Fig. 4.37. Impinging photons are simulated and the output voltage V_{S-D} varies accordingly. Both circuits are interesting and innovative, the capacitive divider presenting a quite large area

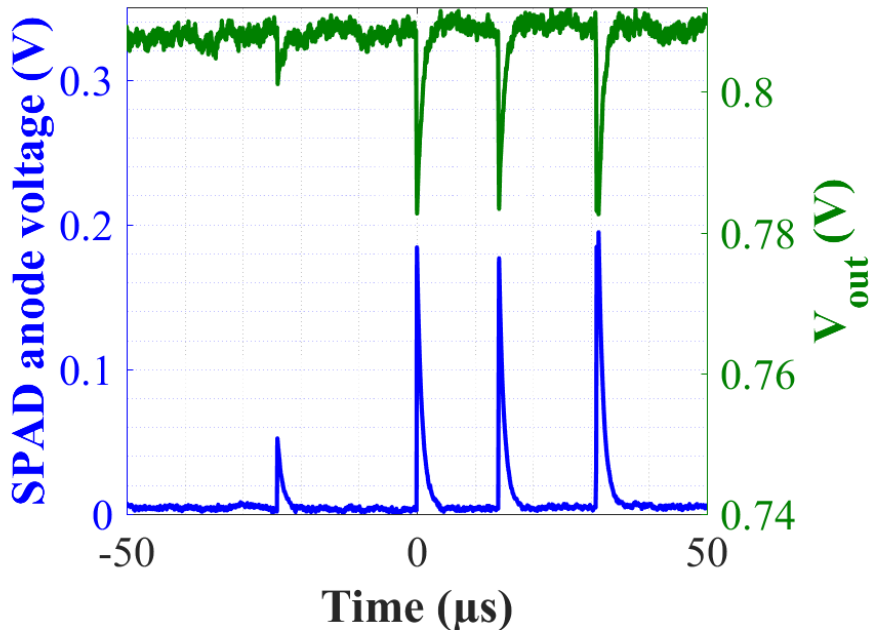

Figure 4.34: *Dynamic characterization of sensing cell with eg-type transistors. Each spike corresponds to an avalanche event. The indirect avalanche detection thanks to body-biasing effect is here validated [28].*

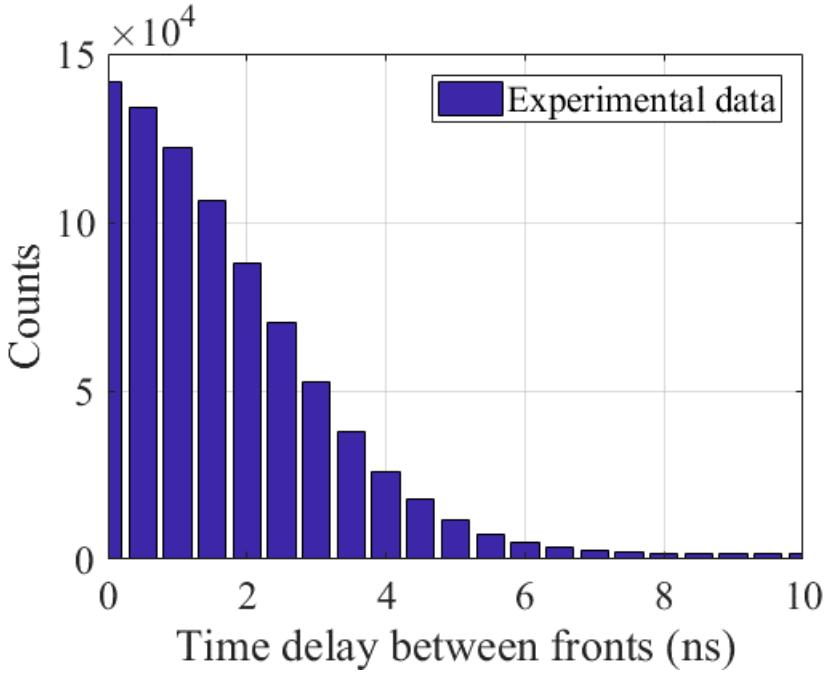

Figure 4.35: *Histogram of time delays between the fronts: anode and sensing output voltages.*

(minimum NMOS size: L×W 4 µm^2) and a negligible static power consumption, while the resistive divider (experimentally validated) occupies less area but presents a static

consumption around 100 µW.

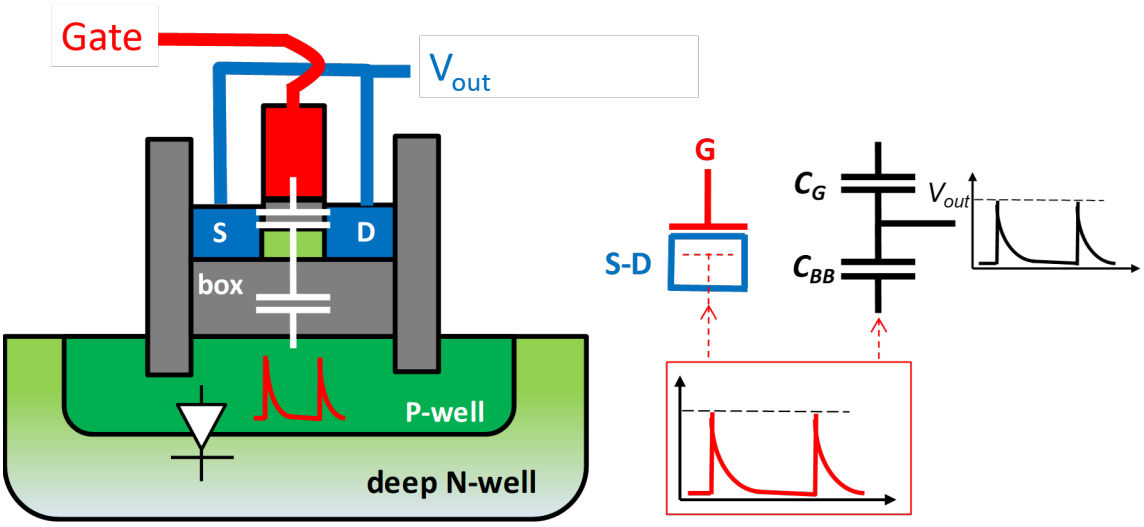

Figure 4.36: *Another proposed avalanche indirect sensing circuit, based on the equivalent capacitance divider.*

Such indirect sensing feature supports the use of larger excess voltage, as compared to direct approaches and paves the way for simpler and innovative SPAD processing electronics, while providing the SPAD integration in an intrinsically 3D technology in order to optimize FF and to avoid expensive and complex 3D assembly techniques.

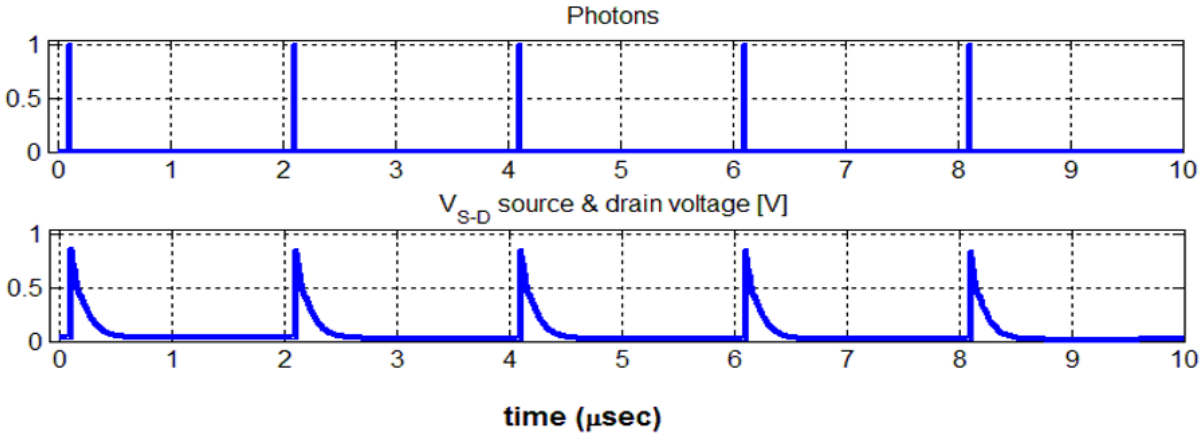

Figure 4.37: *Dynamic simulation of capacitor divider-based sensing circuit. The output voltage (V_{S-D}) varies synchronously with impinging photons, thanks to body-biasing effect, demonstrating indirect avalanche detection for this very simple circuit.*

Conclusions

The SPAD cells designed in C28FDSOI technology were characterized and the corresponding results are shown and discussed in this chapter. The I-V curves showed that the native PN junction composed of PW and DNW present very low breakdown voltage, when compared with State-of-the-Art components. This is an indication of the high doping levels of wells, which is translated into a very abrupt junction.

By means of temperature tests, it was possible to analyse the evolution of Dark Current and also Dark Count Rate (DCR). From their corresponding Arrhenius plot, due to low activation energy, it was evident that most of the generated carriers are produced by Band To Band Tunneling (B2B) and Field Enhanced Trap Assisted Tunneling (TAT) Effects, which is common for abrupt junctions. Nevertheless, as shown in the evolution of breakdown voltage according to temperature, these carriers are indeed accelerated by the strong electric field, and then generate other carriers by impact ionization effect, due to its positive dV_{BD}/dT slope.

Electroluminescence tests showed the difference between implants for FDSOI and STI regions, the latter being more doped. Due to design rules constraints, at borders of FDSOI structure, STI was present, implying in Premature Edge Breakdown. As the foundry later make an exception for this specific design rule, a third test chip was sent to fabrication during this PhD work, in order to correct this PEB problem, but has not yet been characterized.

The characterization of DCR proved to be rather difficult, due to three main reasons: 1) the high Band To Band Tunneling (B2B) and Trap Assisted Tunneling (TAT) generation rates, that adversely impacts its performance (producing a rather noisy device); 2) the use of passive quenching circuits, which is not optimal for SPAD performance analysis; and 3) the STI layer present at the borders of the SPAD junction

In order to address the first issue, the foundry has accepted to make an exception and perform the dedicated implant proposed in Section 3.1.2, for a specific wafer, that were received in April 2019. These devices were also characterized and showed great improvement in terms of breakdown voltage (significantly increased), and also in dark current evolution according to temperature (presenting higher variation). These recent results can be interpreted as a reduction of B2B and TAT effects. Nevertheless, this improvement did not have a considerable impact while measuring DCR.

The Passive Quenching and Recharge Circuit (PQRC) was used here due to the short deadlines imposed by the foundry and its long fabrication time delay, sometimes undergoing through manufacturing time extensions. The use of Active Quenching and Recharge Circuit (AQRC) should not only reduce pile-up effect, but also allow measuring other important SPAD parameters, such as Photon Detection Efficiency (PDE) and time jitter, that could not be evaluated during this work.

Lastly, the presence of silicon/silicon-oxide interfaces directly in contact with the SPAD's Space Charge Region (SCR) (represented here by the STI layer at the borders of the SPAD) adversely affect DCR. Indeed, those interfaces are well known for presenting a large concentration of defects associated with charge trapping, that are liberated during recharge time, increasing total DCR. For addressing this issue, the foundry has accepted the violation of the concerned design rule, increasing the distance between the junction and the STI layer. The concerned device has not been characterized yet, since

it was only very recently received (September 2019).

Even with all of those issues, it was still possible to perform DCR measurements for low excess voltages up to 0.3 V.The devices proved to be very noisy, when compared to the State of the Art (SOTA) implementations, which is normal for a technology that was not conceived for the purpose of SPAD implementation.

Despite the main constraints faced during characterization, the implemented device proved to be able to operate in Geiger-mode, even in native technology. Although current results are not really comparable to SOTA SPAD, they constitute a proof-of-concept of the use of C28FDSOI technology for implementing SPAD devices, which is of great interest as an alternative for the certainly complicated and expensive 3D integration, which is nowadays employed for optimization of Fill Factor.

Another great advantage of the implementation of SPAD in C28FDSOI is the possibility of integrating indirect avalanche sensing circuits, as demonstrated in this chapter, thanks to body-biasing feature in C28FDSOI. The proposed voltage divider proved to be a simple and yet effective validation circuit, as it could detect avalanche events simultaneously with Passive Quenching Circuit (PQC), even for very low excess voltages, as demonstrated in experimental results. An equivalent capacitor divider was also proposed as indirect sensing circuit and was validated by means of simulation. The aforementioned devices are certainly not optimized, but they pave the way for innovative circuitry for SPAD processing electronics in FDSOI technology.

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Conclusions and Perspectives

In this work, an implementation of Single Photon Avalanche Diode (SPAD) in native CMOS 28 nm Fully Depleted Silicon On Insulator (FDSOI) (C28FDSOI) is proposed. The main objective here being the verification of the feasibility of such a concept, SPAD cells were designed, simulated, modelled, and characterized.

In chapter 1, the physics of SPAD, also known as Geiger-mode silicon photodetectors, is briefly reviewed. Those detectors are basically pn junctions biased above breakdown voltage until a photon is absorbed in the device's multiplication region, generating an avalanche event and a consequent high current, easily detectable. Quench and recharge circuits are, then, needed for avoid damaging the diode and for resetting it to its original state, respectively.

The main Figures of Merit (FOM) are then explained: Dark Count Rate (DCR), afterpulsing, Photon Detection Probability and Efficiency (PDP, PDE), time jitter, Fill Factor (FF) and crosstalk. Those parameters highly depend on the SPAD architecture (e.g. doping levels at layers, interfaces) and on the operating conditions (e.g. biasing, temperature).

In the same chapter, the current State of the Art (SOTA) for SPAD implemented in CMOS is discussed. Those technologies are preferred thanks to their reliable and reproducible integrated electronics. The most advanced implementations are compared by means of several SPAD FOM, even if the operating conditions are quite different between the presented implementations. Indeed, several parameters, such as voltage bias, temperature, incident wavelength and mode of illumination (Front Side Illumination (FSI) or Back Side Illumination (BSI)) have a direct impact in SPAD performance, making the suitability for a certain application determined by their performance at the required operating conditions. The most efficient devices so far make use of complex and expensive 3D stacking techniques, where two dies are assembled at wafer level. This approach allows the optimization of a first die for hosting the SPAD (normally in CMOS Image Sensor (CIS) technologies) and the second one for associated electronics (commonly in advanced CMOS). Up to this date, 3D SPAD is the best compromise between Photon Detection Efficiency (PDE) and FF.

Some SPAD have been recently implemented in Silicon On Insulator (SOI) technologies, having the concerned pn junction integrated over the Buried Oxide (BOX) layer, used to stop substrate etching process. The first SPAD implemented in Fully Depleted Silicon On Insulator (FDSOI) was proposed by means of TCAD simulation, with the promise of an intrinsic monolithic integration of both SPAD device and associated electronics. The physical implementation of this device and the analyzis of its characteristics are the main objectives of this PhD thesis.

In chapter 2, the design of the SPAD cells in CMOS 28 nm FDSOI (C28FDSOI) is

addressed. First, a review of the technology, with its main features is addressed, with a special focus on the body biasing effect, key feature for high performance and energy efficient electronics, mandatory parameters for future technologies.

C28FDSOI was mainly chosen for providing the possibility of an intrinsic and monolithic 3D integration of both SPAD devices (under the Buried Oxide (BOX) layer) and associated electronics (on top of it), both being electrically isolated from one another. To the best of our knowledge, this is the very first implementation of the aforementioned approach. This could allow an optimization of the Fill Factor (FF), like in the current State of the Art (SOTA) 3D stacking approach, but without the need for expensive and complex technological processes.

In order to investigate the feasibility of the proposed implementation, several variants of SPAD cells were designed. Parameters such as zone of integration (FDSOI, STI, NOSO), geometry, guard distance, photosensitive surface and quenching circuit. Due to mandatory design rules (orthogonal shapes, antenna diodes design and adaptation of padring), the optimization of geometry was limited. Nevertheless, a fair amount of variants were successfully implemented.

Thanks to body biasing feature in C28FDSOI, two indirect avalanche sensing circuits were proposed: a transistor-based voltage divider and an equivalent capacitance divider. Both have their output voltage varying during avalanche events. Such innovative approaches support the use of larger excess voltage and pave the way for simpler and innovative SPAD processing electronics.

Then, in chapter 3, the proposed devices are investigated by means of Technology Computer-Aided design (TCAD) simulation. Starting from the definition of the simulated structure and the corresponding doping profiles, some differences between the resulting doping for distinct zones of integration (FDSOI, STI) were identified. For such an estimation, Sentaurus SPROCESS was used, applying the implants' data provided by the foundry.

The simulation structure being correctly constructed, the carriers' transport mechanisms could be simulated. For this purpose, the junction was reversely biased. It was possible to estimate electric field magnitude and spatial distribution, breakdown voltage, Space Charge Region (SCR) characteristics, the ionization coefficients and integrals, as well as carrier generation rates, according to Shockley-Read-Hall Generation-Recombination (SRH) and Band To Band Tunneling (B2B) phenomena.

Different types of TCAD simulation were performed (steady-state and dynamic behavior just before avalanche is triggered), in order to correctly estimate those characteristics. For each of the carrier generation phenomena, different models were studied. Those providing the best fit of experimental data were kept.

With the extracted ionization coefficients and generation rates, a rough estimation of DCR and PDP could be obtained by means of post-processing routine. Even if those results do not represent the actual measured values (as they actually depend on many parameters), they are quite useful for comparison between different structures and operating conditions.

In order to calculate Avalanche Triggering Probability (ATP) (useful for DCR and PDP estimation), McIntyre model was initially used. Also, an approximated analytical solution for this model was proposed and validated for high electric field condition. Thanks to fitting parameters, this model was extended to the whole Space Charge

Region (SCR). The advantage of this new approach is the reduction of numerical solutions, implying optimization of calculation time and consequently, allowing compact modeling.

DCR evolution with increasing temperature was then analyzed and, thanks to Arrhenius plot, an estimation of the main contribution effects in carrier generation (Band To Band Tunneling (B2B) and TAT) was proved, in agreement with measurements.

For evaluating PDP, the Beer-Lambert law was used, describing the photon absorption in the SCR. The model used is simplistic, because it does not take into account the diffusion from the neutral regions. The small excess voltages that could be applied in practice did not provide considerable values of PDP. Nevertheless, better results are obtained at higher excess voltages.

In agreement with the foundry, a special wafer could benefit from customized implants. For this purpose, a TCAD study was conducted for determining the implants parameters needed for improving SPAD performance (increasing breakdown voltage). By making the P-well/Deep N-well less abrupt, lower B2B contribution is obtained in simulation, resulting in a fair reduction of DCR.

In chapter 4, the electrical characterization of the fabricated SPAD in C28FDSOI technology is addressed. Measurements such as I-V and C-V curves, dark current, breakdown voltage according to temperature, electroluminescence response were provided.

Low breakdown voltage was measured for devices implemented in the native technology, without any modification or process customization. It indicates high doping of the wells used for the junction that is quite abrupt.

When performing temperature tests, thanks to the low activation energy extracted from Arrhenius plot, both dark current and DCR measurements proved the device to present a main contribution of Band To Band Tunneling (B2B) and field-enhanced Trap Assisted Tunneling (TAT) effects in carrier generation. Even if those phenomena are common for abrupt junctions, the positive dV_{BD}/dT slope clearly states the avalanche event that takes place for the concerned device.

The electroluminescence response proved that, despite the use of BFMOAT layer as guard ring, FDSOI junction breaks first at borders, characterizing Premature Edge Breakdown (PEB). Nevertheless, STI cells have shown uniform electric field distribution. This difference can be explained by the STI layer at the borders of FDSOI cell. Indeed, by means of TCAD simulation presented in chapter 3, the two zones present a non negligible difference in their doping profiles, the former being even more abrupt. A new version of the circuit, in which a design rule is violated (with agreement of the foundry), is expected to present a better field distribution.

Dark Count Rate (DCR) characterization proved to be rather difficult due to the high device noise associated not only to the elevated Band To Band Tunneling (B2B) and Trap Assisted Tunneling (TAT) contributions, but probably also due to the interface silicon/silicon-oxide, well known in the literature to be a zone with a high concentration of deep levels. Due to this interface in direct contact with the SPAD's Space Charge Region (SCR), a high DCR was measured at low excess voltage. This problem is expected to be reduced for the new version of the test chip, where STI does not cover the edges of the photosensitive area.

Moreover, the use of a simple passive quenching circuit, although useful for initial

tests and selection of architectures, does not provide an optimal measure of DCR, due to the nonexistence of a proper controlled dead time. Pile-up effect was then observed. However, it was still possible to measure DCR to excess voltages up to 0.3 V. The experimental estimation of PDP was unfortunately not possible, due to the small excess voltage and the large amount of dark counts, adversely impacting the detection.

When the special wafer with customized implants were characterized, the increase in breakdown voltage values was observed, as predicted in TCAD simulations. These results prove that the junction is less abrupt, and should have less B2B generation rate. Nevertheless, DCR was still high, probably influenced by the defects in the STI interface, responsible for injecting carriers in SCR. The combination of active quench and recharge circuits with the suppression of STI layer in contact with the SCR should provide not only a better DCR characterization, but also enable the correct estimation of other important FOM, such as PDP and time jitter.

The fabricated indirect avalanche sensing circuit proposed (i.e. transistor-based voltage divider) was also validated by means of electrical characterization. Its principle is based on the outstanding body-biasing feature of FDSOI. Although simple, this circuit proved to be effective when it comes to the detection of avalanche events. An equivalent capacitor divider was also proposed as indirect sensing circuit and was validated by means of simulation. The aforementioned devices are certainly not optimized, but they pave the way for innovative circuitry for SPAD processing electronics in FDSOI technology.

Despite the main constraints faced during characterization, the implemented device proved to be able to operate in Geiger-mode, even in native technology. Although current results are not really comparable to State-of-the Art SPAD, they constitute a proof-of-concept of the use of FDSOI technology for implementing SPAD devices, which is of great interest as an alternative for the certainly complicated and expensive 3D integration, which is nowadays employed for optimization of Fill Factor.

List of Publications

Journal articles as first author

T. Chaves de Albuquerque et al. “Indirect Avalanche Event Detection of Single Photon Avalanche Diode Implemented in CMOS FDSOI Technology,” Solid-State Electronics , no. 33, p. 107 636, Sep. 2019, i s s n : 00381101. d o i : 10.1016/j.sse. 2019.107636 . [Online]. Available: https://linkinghub.elsevier.com/ retrieve/pii/S0038110119303648

Conference contributions as first author

T. Chaves de Albuquerque et al. “Integration of SPAD in 28nm FDSOI CMOS technology,” in 2018 48th European Solid-State Device Research Conference (ESSDERC), vol. 2018-Sep, IEEE, Sep. 2018, pp. 82–85, i s b n : 978-1-5386-5401-9. doi: 10.1109/ESSDERC.2018.8486852. [Online]. Available: https://ieeexplore.ieee.org/document/8486852/

T. Chaves de Albuquerque et al. “Lowering the Dark Count Rate of SPAD Implemented in CMOS FDSOI Technology,” in 2019 5th EUROSOI – ULIS 2019 Conference vol. 2019-Apr, IEEE, Sep. 2019;

T. Chaves de Albuquerque et al. “Body-biasing considerations with SPAD FDSOI: advantages and drawbacks,” in 2019 49th European Solid-State Device Research Conference (ESSDERC), vol. 2019-Sep, IEEE, Apr. 2019;

Other contributions

Vignetti, M. M., et al. "3D Silicon Coincidence Avalanche Detector (3D-SiCAD) for charged particle detection." in Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 881 (2018): 53-59. Available: https://doi.org/10.1016/j.nima.2017.10.089

Résumé long en français

Introduction générale

Avec les progrès des technologies microélectroniques, de nombreuses nouvelles applications et marchés ont été développés. Les smartphones sont omniprésents dans la vie d'aujourd'hui. La résolution et les fonctionnalités des caméras s'améliorent chaque jour. Une des fonctionnalités les plus prometteuses est l'imagerie 3D et la télémétrie. Ces implémentations pourraient permettre de grandes avancées telles que les voitures autonomes, grâce à la conduite intelligente.

Pour les applications d'imagerie 3D, non seulement des imageurs normaux sont nécessaires, mais également des détecteurs capables de mesurer la distance des objets environnants. Ces systèmes peuvent utiliser des mesures de temps de vol (TOF), technique avancée dans laquelle une source lumineuse émet un signal, qui est ensuite réfléchi par une cible. Pour une approche TOF directe, le faisceau réfléchi frappe ensuite le capteur et le temps écoulé entre ces deux événements est mesuré afin que la distance puisse être déduite de la moitié du temps mesuré (en considérant le va-et-vient des photons).

Les diodes à avalanche à photon unique (SPAD) se sont révélées être d'excellents dispositifs pour la mise en oeuvre de ce récepteur. Ces dispositifs sont des jonctions PN fonctionnant avec une polarisation en tension inverse élevée et présentent le grand avantage d'avoir une sensibilité très élevée, indispensable pour ce type d'application où les faisceaux réfléchis diffus sont courants et peu sûrs d'atteindre le capteur dans des situations réelles. L'utilisation de SPAD présente un autre avantage: elle fournit directement un signal numérique à sa sortie avec une électronique simple, sans qu'il soit nécessaire d'intégrer des convertisseurs analogiques-numériques rapides et complexes.

L'objectif de cette thèse est d'étudier la mise en œuvre de dispositifs SPAD dans une technologie CMOS FDSOI avancée. Ces travaux ont été réalisés dans le cadre du programme de recherche ARC6 2016 (n ° 16 - 005689 - 01), financé par la Région Auvergne Rhône Alpes, en France, dans le cadre d'un partenariat entre deux laboratoires français: l'Institut des Nanotechnologies de Lyon (INL) et le Laboratoire. Hubert Curien (LHC), sous la supervision du Prof. Francis Calmon et du Prof. Raphaël Clerc. Nous avons également bénéficié du support technique du CEA-LETI et de STMicroelectronics.

Après cette section d'introduction générale, ce long résumé en français présente les différentes étapes de conception, simulation, modélisation et caractérisation du prototype en quatre sections, suivis d'une conclusion générale et de perspectives.

1 SPAD et applications

Dans cette section, le principe de fonctionnement de la diode à avalanche à photon unique (SPAD) est présenté, ainsi que ses principaux facteurs de mérite, tels que le taux de comptage dans l'obscurité, la probabilité de détection de photons, la gigue temporelle et le facteur de remplissage. Quelques discussions sur les applications SPAD pour les technologies futures sont également décrites. À la fin du chapitre, l'état de l'art des SPAD mis en œuvre dans la technologie CMOS est présenté, avec un accent particulier sur les technologies SOI (Silicon On Insulator).

1.1 Fonctionnement en mode Geiger des photodétecteurs en silicium

Les diodes à avalanche à photon unique (SPAD) sont des jonctions PN fonctionnant en polarisation inverse, au-delà de la tension de claquage, dans la zone dite de mode Geiger. En raison de la polarisation haute tension, le champ électrique dans la région de charge d'espace (ZCE) est également élevé, ce qui configure un état très instable de la jonction, car un seul porteur libre présent dans la ZCE serait rapidement accéléré par le champ électrique et pourrait facilement provoquer une série de processus d'ionisation par impact, entraînant une avalanche auto-entretenue et un courant électrique conséquent.

Ce porteur libre peut être le résultat d'un processus de photogénération. Dans ce cas, le dispositif est dit diode à photon unique (SPAD), car un photon incident unique est capable de générer un signal de courant macroscopique, facilement détectable.

Le mode de fonctionnement de base des SPAD est illustré à la Fig. 1.1. Le dispositif est initialement polarisé au-dessus de la tension de claquage (point 1). Une fois que l'avalanche est déclenchée (point 2), un courant élevé circule dans le dispositif et peut l'endommager s'il n'est pas correctement éteint (étouffé). Pour éviter cela, des circuits d'extinction (comme une simple résistance en série) sont utilisés pour réduire la tension inverse à travers la diode et, par conséquent, le courant d'avalanche (point 3). Une fois que cela se produit, la tension aux bornes de la diode est ramenée à sa valeur initiale (point 1) et la SPAD est prêt pour une autre détection.

1.2 Figures de mérite

Bruit dans l'obscurité ou dark count noise (DCR)

Le taux de comptage dans l'obscurité (Dark Count Rate - DCR) est le bruit intrinsèque du dispositif et peut être défini comme le taux d'impulsions parasites, provoqué par des événements autres qu'optiques. En d'autres termes, le taux, en Hz or Hz/μm^2, d'avalanches créées par la génération thermique, l'effet tunnel bande à bande (B2B), voire la libération de charges piégées, contribuent au DCR.

Plusieurs aspects peuvent influencer le comptage dans l'obscurité. Le choix de la technologie, par exemple, a un impact considérable sur le DCR, dans la mesure où les niveaux de dopage et la densité de défauts (du silicium, mais également des interfaces silicium-oxyde proche de la SCR) ont une influence directe sur le comptage.

Les conditions de fonctionnement externes, telles que la température et la tension d'excès, peuvent également modifier considérablement les valeurs de DCR. Fondamen-

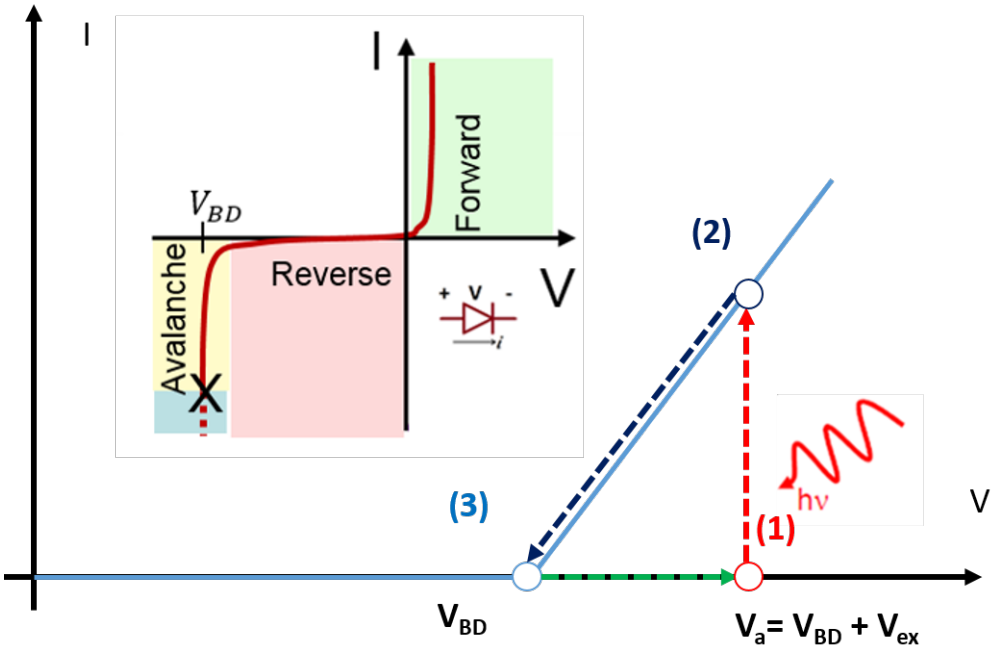

Figure 1.1: *Principe de fonctionnement des photodiodes en mode Geiger.*

talement, à mesure que la température augmente, le taux de recombinaison et génération Shockley-Read-Hall (SRH) et le DCR augmentent également. De plus, si la tension d'excès est augmentée, la probabilité de déclenchement augmente et, par conséquent, le DCR augmente également. Le délai entre la détection, l'étouffement et la recharge des avalanches influe également sur le DCR total, par le phénomène d'afterpulsing. Enfin, les dimensions et la géométrie des cellules SPAD doivent également être prises en compte en phase de conception, afin de réduire le DCR.

Déclenchements secondaires ou afterpulsing

Le DCR total inclut les impulsions primaires et secondaires en sortie. Ces dernières sont également connues sous le nom de afterpulsing et proviennent de la libération de charges piégées dans les centres de génération-recombinaison localisés dans la bande interdite et existent en raison des défauts et des impuretés du semiconducteur, facilitant ainsi les transitions entre les bandes de valence et de conduction. Ces évènements générèrent une autre avalanche, corrélée avec la précédente. Plus le temps de recharge est court, plus le relâchement de ces charges piégées est probable. L'intensité du courant, proportionnelle à la tension d'excès, augmente également la probabilité d'afterpulsing.

Efficacité de détection

La probabilité de détection de photons (PDP) peut être définie comme la probabilité qu'un photon absorbé génère une impulsion de courant de sortie, en raison d'une avalanche auto-entretenue. Le PDP représente la sensibilité de la SPAD et est directement influencé par l'amplitude du champ électrique et sa distribution le long

de la jonction. Physiquement, le PDP est directement lié au taux de photogénération (efficacité quantique) et à la probabilité de déclenchement d'une avalanche. Le PDP est également fonction de la longueur d'onde du photon incident, par le biais du coefficient d'absorption des photons dans le matériau. Il existe des implémentations SPAD dans différents matériaux semiconducteurs pour le spectre proche ultraviolet (300 - 400 nm), le spectre visible (400 - 800 nm) et le proche infrarouge (NIR) (800 - 1550 nm).

Gigue temporelle ou jitter

En travaillant avec des SPAD, l'intervalle de temps entre l'arrivée du photon et le début de l'avalanche n'est pas constant, ce qui présente des fluctuations statistiques. Lors de l'analyse de la distribution temporelle de l'arrivée des photons, il est possible de définir la gigue temporelle (ou résolution) en tant que largeur maximale à mi-hauteur (FWHM). Ce facteur de merite est fonction de la longueur d'onde incidente et de l'endroit précis où l'avalanche est déclenchée.

Facteur de remplissage ou Fill Factor

Le facteur de remplissage (Fill Factor - FF) est un autre facteur déterminant pour le détecteur SPAD. Il est défini comme le rapport entre les surfaces des zones photosensible et totale du pixel, y compris l'aire des circuits d'étouffement et de recharge. La taille à la fois des composants électroniques et des anneaux de garde associés (zones faiblement dopées utilisées pour réduire le champ électrique aux bords) représente la principale cause de la réduction non désirée de FF (de l'ordre de quelques pour cent).

Couplage ou cross-talk

Lors de la mise en œuvre des matrices SPAD, le couplage optique et électrique est un facteur qui peut nuire au bon fonctionnement du système. Lorsqu'un photon est absorbé dans un pixel de la matrice, une diffusion latérale de porteurs peut être déclenchée, atteignant peut-être une SPAD (nature électrique) adjacente. Dans le cas d'un couplage optique, lorsqu'une avalanche est générée, elle produit souvent un effet d'électroluminescence, émettant des photons qui peuvent éventuellement être absorbées dans le ZCE d'une cellule voisine. Dans les deux cas, le résultat est une fausse détection, qui doit être évitée. Lors de la phase de conception, les effets de couplage doivent être pris en compte lors de l'estimation de l'espacement entre les cellules SPAD voisines. Le résultat final est généralement une réduction du FF.

1.3 Applications

Grâce à la sensibilité élevée et à la résolution temporelle de l'ordre de quelques dizaines de picoseconde des dispositifs SPAD, ils peuvent être utilisés à différentes fins, telles que le comptage de photons uniques corrélés dans le temps (Time Correlated Single Photon Counting - TCSPC), la microscopie par imagerie de fluorescence résolue dans le temps (Fluorescence Lifetime Imaging Microscopy - FLIM), le temps de vol (Time Of Flight - TOF)) et la détection de particules chargées.

Dans le Time-of-Flight (TOF), une source lumineuse émet un signal monochromatique ou à spectre large, qui est ensuite réfléchi par un objet cible et heurte le détecteur. En temps de vol direct, le temps écoulé entre le signal de démarrage (connecté à la source de lumière) et le signal d'arrêt, produit par le capteur, est mesuré. Les détecteurs SPAD sont remarquablement bons candidats pour ce type de mesure, grâce à leur résolution temporelle de l'ordre de la dizaine de picosecondes. Le temps de vol (TOF) est une excellente option pour des applications telles que l'imagerie 3D, la détection et la télémétrie par imagerie lumineuse (LIDAR) et la conduite intelligente. L'utilisation d'une telle approche présente le gros avantage d'une intégration facile dans la technologie CMOS.

1.4 Etat de l'art des SPAD dans les technologies CMOS

SPAD dans les technologies CMOS bulk

Même si différents matériaux peuvent être utilisés pour la mise en œuvre de diodes en mode Geiger (tels que Ge-on-Si InP / InGaAs), leur intégration à la production en masse de composants électroniques CMOS n'est pas toujours simple. Ainsi, depuis le premier SPAD implémenté en CMOS, qui offrait une intégration monolithique avec une électronique de lecture fiable et reproductible, ces dispositifs ont fait l'objet d'une attention accrue sur le marché, en raison de leur système totalement intégré, économique et performant.

En prenant en compte les FOM susmentionnés, certaines SPAD récemment mis en œuvre en CMOS présentent l'état de l'art actuel. Les meilleurs résultats à ce jour sont obtenus en utilisant des techniques d'empilement 3D au niveau des puces, car elles combinent les meilleures technologies dédiées (pour la SPAD, mais aussi pour le traitement de données), ce qui permet d'optimiser les développements, en fonction de l'application.

En ce qui concerne l'empilement 3D (Fig. 1.2), ses principaux avantages sont le facteur de remplissage plus élevé et la meilleure réponse proche infra rouge (Near Infra Red - NIR) pour l'éclairement en face arrière (Back Side Illumination - BSI), qui convient aux technologies futures. Pour cette approche, la SPAD est implémentée dans la puce du premier niveau (normalement conçue dans une technologie CIS (CMOS Image Sensor) dédiée, tandis que l'électronique associée pour le traitement des données est intégrée dans la puce de dernier niveau (généralement réalisée dans la technologie CMOS avancée), ce qui permet des solutions avec efficacité énergétique, et consommation réduite.

Dans la littérature, en utilisant les technologies 45/65 nm, il était possible d'obtenir jusqu'à présent les meilleurs DCR, PDP, jitter et FF pour l'empilement 3D CMOS SPAD. Une comparaison entre ces résultats et le précédent état de l'art est présentée à la Fig. 1.3 pour le DCR et à la Fig. 1.4 pour le PDP.

SPAD implémenté dans les technologies Silicon On Insulator

Avec l'évolution des transistors, dans le but de poursuivre la loi de Moore, de nouvelles technologies ont été développées. Silicon On Insulator (SOI) s'est révélé être l'une des approches les plus prometteuses pour les circuits très innovants et faible consommation, en maintenant les transistors isolés du substrat dans un film de silicium

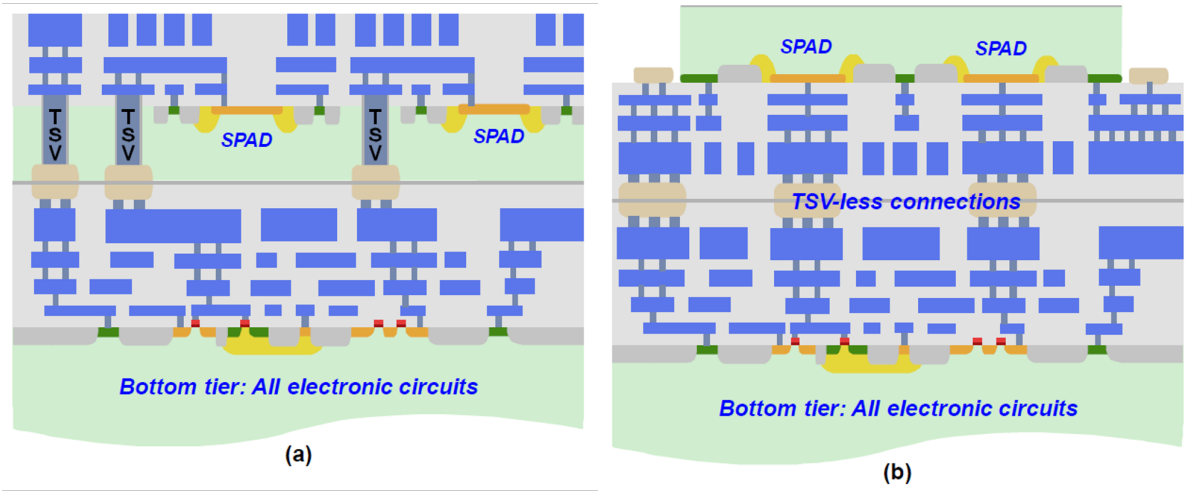

Figure 1.2: *Types d'assemblage 3D, selon l'approche d'illumination souhaitée: (a) face avant (FSI); (b) face arrière (BSI). (Adapté de [1])*

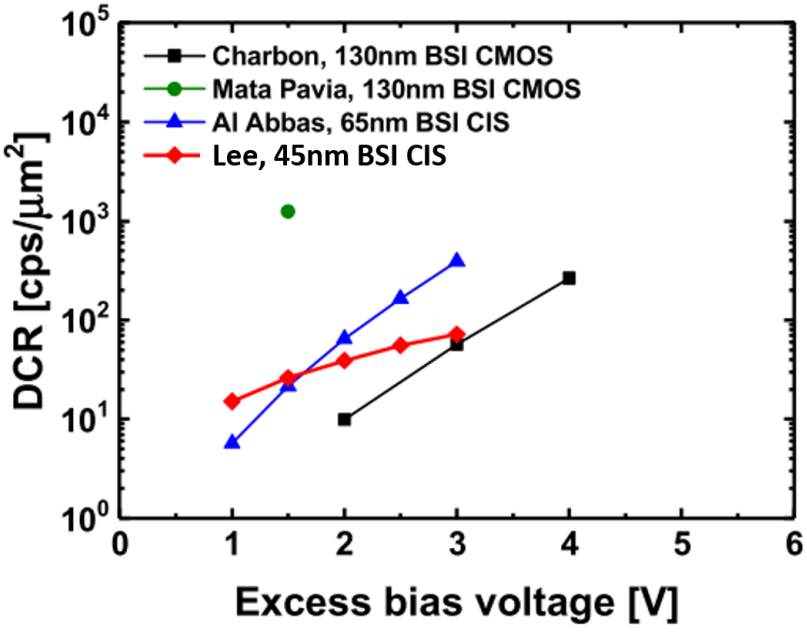

Figure 1.3: *Comparaison entre l'état de l'art actuel pour les valeurs de DCR en fonction de la tension d'excès. (Adapté de: [2]). Références dans la figure: Charbon ([3]), Mata Pavia ([4]), Abbas ([5]).*

placé sur une couche isolante enterré (Buried Oxide (BOX)). L'intégration de SPAD en CMOS suit également ces avancées et les chercheurs sont souvent enthousiastes à l'idée de développer de nouvelles architectures SPAD dans ces technologies modernes.

La première mise en œuvre de SPAD dans la SOI CMOS a été réalisée en 2013, puis développée et caractérisée pour être opérationnelle à la fois pour FSI et BSI. La jonction

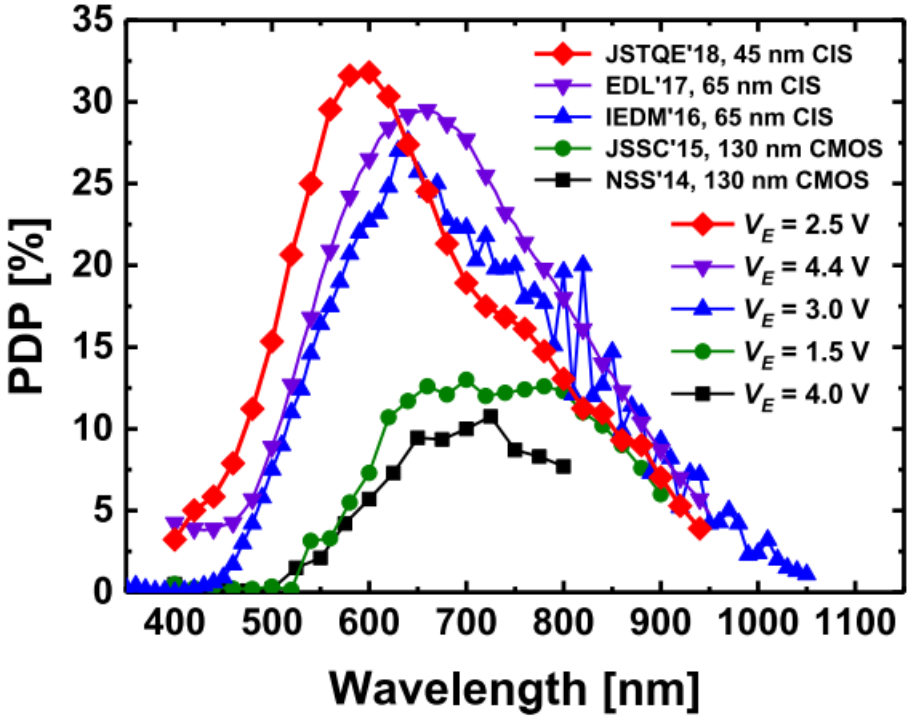

Figure 1.4: *Comparaison entre l'état de l'art actuel pour les valeurs de PDP en fonction de la longueur d'onde. (Adapté de [6]). Références dans la figure: JSTQE'18 ([7]), EDL'17 ([8]), IEDM'16 ([5]), JSSC'15 ([4]), NSS'14 ([3]).*

pn est intégrée dans le film de silicium dopé (épaisseur de 1.5 µm) placé sur le BOX, comme illustré à la Fig. 1.5. Le substrat d'origine est ensuite gravé jusqu'à atteindre l'oxyde enterré. La tension de claquage était d'environ 12 V. Le PDP a son maximum à 460 nm (11% en FSI, 6% en BSI) et la gigue est d'environ 500 ps à une polarisation excédentaire de 1.2 V, étant améliorée récemment (65 ps). L'afterpulsing est négligeable avec un temps mort supérieur à 1 µs.

Très récemment, la technologie standard 140 nm CMOS SOI a été utilisée pour développer des BSI SPAD. La jonction est formée de couches P + / N, tout en maintenant les interfaces silicium / oxyde de silicium (couches BOX et Shallow Trench Isolation (STI)) éloignées de la région de multiplication du dispositif. En effet, en raison des défauts du réseau cristallin induits par la gravure et du piégeage de charges associé à la STI, le DCR peut être augmenté de manière défavorable. Une géométrie circulaire a été choisie pour la mise en œuvre du SPAD, réduisant ainsi le claquage prématuré aux bords (PEB).

Néanmoins, les dispositifs fabriqués présentent des résultats remarquables, tels qu'un DCR variant de 1.2 Hz/µm^2 à 396.1 Hz/µm^2 à la température ambiante, en fonction de la tension d'excès. En termes de PDP, une sensibilité significative en bleu, proche ultra violet et violet, ainsi que de bonnes valeurs pour le rouge et le NIR ont été obtenues (Fig. 1.6). Comme dans la plupart des dispositifs conçus pour le BSI, en raison de l'absence de couches métalliques, le FF est amélioré. Une gigue temporelle de 119 ps a également été obtenue pour 637 nm.

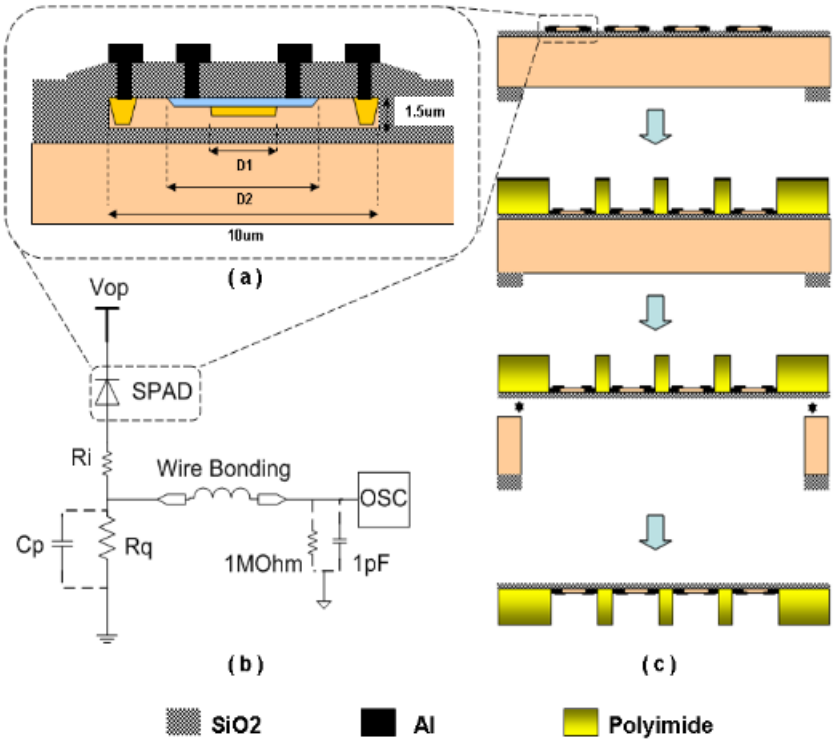

Figure 1.5: *Premier SPAD fabriqué en CMOS SOI. Adapté de [9].*

1.5 Objectifs de la thèse

Il est important de noter que jusqu'à présent, concernant l'intégration de SPAD dans les technologies SOI, la diode est placée sur le BOX, utilisée comme couche d'arrêt pendant le processus de gravure, principalement pour améliorer le PDP dans le BSI et aussi le FF.

L'intégration de SPAD dans une technologie FDSOI (Fully Depleted Silicon on Insulator) (28 nm) a été proposée en 2016, en simulations (TCAD). Comme un film de silicium très mince (7 nm) est placé sur un oxyde ultra mince (25 nm), la diode reste sous cette couche isolante, tandis que des transistors sont mis en œuvre dans le film de silicium mince, isolé électriquement de la SPAD, comme illustré à la Fig. 1.7. Ces transistors pourraient alors être placés sur le dispositif SPAD, au lieu de rester côte à côte. Cette configuration permettrait d'augmenter le FF en BSI, dans une intégration 3D monolithique et intrinsèque des pixels et de leurs composants électroniques associés, sans la nécessité de processus d'empilement 3D complexes et coûteux.

L'objectif principal de cette thèse est de prouver la faisabilité de cette approche difficile et certainement intéressante par la conception, la simulation TCAD et la caractérisation électrique. À cette fin, la technologie avancé CMOS 28 nm FDSOI de STMicroelectronics a été utilisée. Au début, toutes les règles de conception ont été respectées sans aucune modification ni personnalisation du processus. Nous visons la démonstration expérimentale de l'architecture SPAD FDSOI, sa caractérisation électrique et de sa modélisation. Avec ces résultats, il a été possible de proposer des modifications de processus pour améliorer les performances afin que la technologie

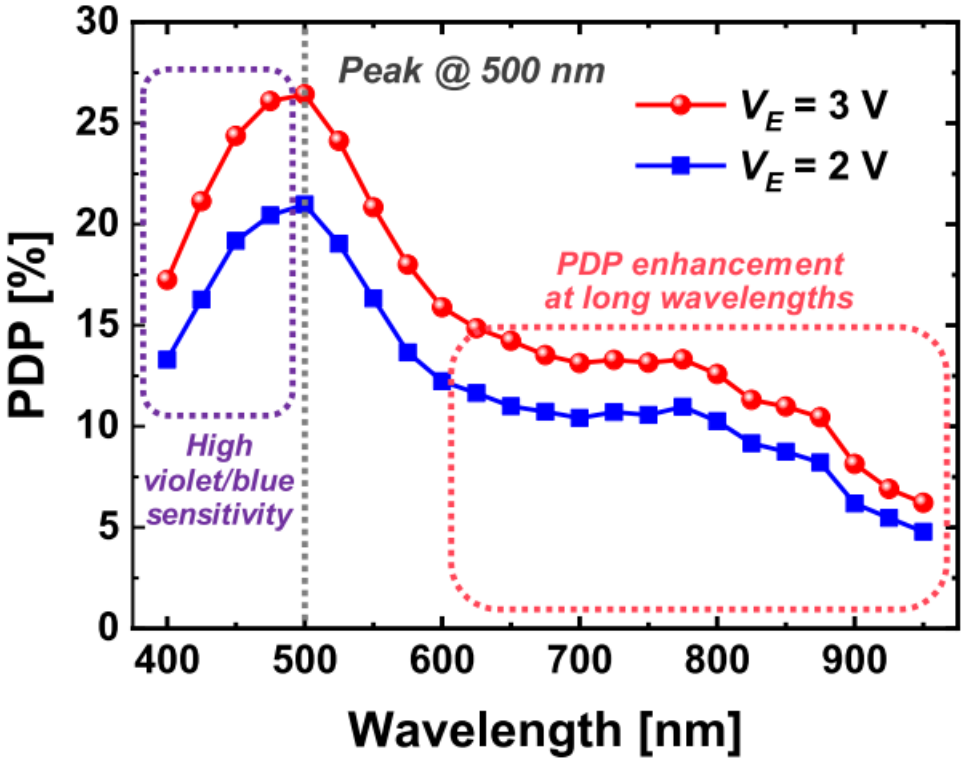

Figure 1.6: *PDP pour SPAD fabriqué dans une technologie* 140 nm *SOI CMOS [6].*

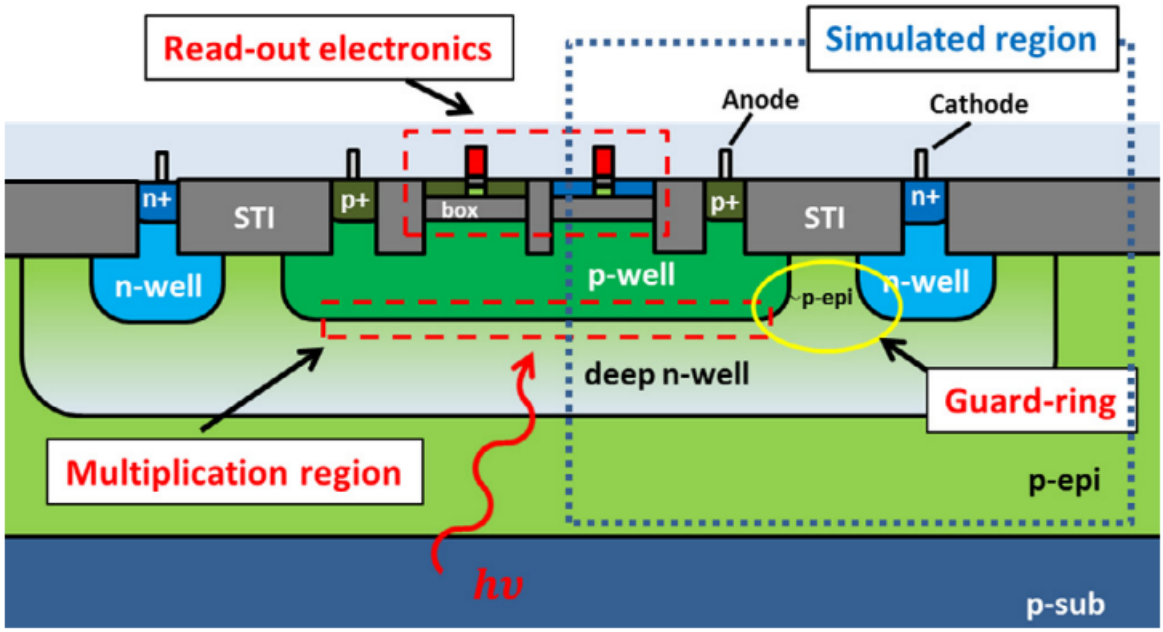

Figure 1.7: *Proposition de SPAD intégré dans une technologie CMOS FDSOI. Adapté de [10].*

puisse être utilisée pour intégrer ces dispositifs.

1.6 Conclusion partielle

Cette section a permis de rappeler les éléments essentiels du fonctionnent des diodes SPADs et de leurs caractéristiques. Ensuite, nous avons présenté l'actuel état de l'art et le concept d'une nouvelle architecture de SPAD en FDSOI, où la jonction reste sous le BOX, pendant que l'électronique associée est intégrée sur cette couche isolante, résultant une structure monolithique et intrinsèquement 3D, optimisant ainsi le FF.

2 Conception de cellules SPAD en technologie CMOS FDSOI 28 nm

Dans cette section, la technologie CMOS 28 nm Fully Depleted Silicon On Insulator (FDSOI) de STMicroelectronics (dorénavant C28FDSOI) est présentée, ainsi que ses principaux avantages, qui la rendent très utile pour les applications embarquées, où l'efficacité énergétique est une priorité. L'intégration de SPAD dans une technologie aussi avancée a ensuite été abordée. Dans un premier temps, aucune personnalisation de la conception n'a été réalisée, c'est-à-dire que toutes les règles de dessin ont été respectées. Des contraintes de règles de conception sont présentées. Les cellules conçues sont ensuite décrites, avec leurs éléments fondamentaux respectifs. Ensuite, un circuit de détection d'avalanche indirect est présenté. Enfin, la présentation du layout final fabriqué est présentée.

2.1 La technologie CMOS 28 nm Fully Depleted Silicon On Insulator

Bien que la technologie CMOS bulk soit largement utilisée dans l'électronique depuis des décennies, en raison principalement de la qualité de son oxyde dans le silicium, elle présente toujours des limites pour les nœud inférieures à 40 nm. Les MOSFETs intégrés dans les technologies bulk occupent souvent seulement la région la plus haute de leur plaquette de silicium, laissant plus de 99% du volume total constituant le substrat de base, servant presque exclusivement de simple support mécanique pour la plupart des applications. Cette intégration en masse est également responsable de l'apparition de plusieurs effets parasites susceptibles de nuire aux performances des transistors, tels que la capacité non négligeable de drain/source au substrat, le verrouillage et le courant de fuite. Ces effets indésirables deviennent encore plus critiques lorsque les dimensions des dispositifs sont réduites en dessous de 40 nm.

L'utilisation de structures SOI était une solution très intelligente pour surmonter ces limitations. Dans de tels dispositifs, les transistors sont isolés diélectriquement du substrat, grâce à une couche Buried Oxide (BOX) (Fig. 2.1). Grâce à elle, la capacité maximale entre les jonctions est réduite à celle des oxydes enterrés, ce qui en fait une solution idéale pour un fonctionnement à grande vitesse tout en permettant une alimentation à basse tension et un courant de fuite réduit, réduisant ainsi la consommation énergétique. En l'absence de contact électrique entre les transistors et le substrat, les problèmes de verrouillage sont également résolus.

En C28FDSOI, deux familles distinctes de transistors existent, en fonction du type de dopage du caisson sous le BOX (P-well (PW) ou N-Well (NW)): V_{th} régulier ou standard (Regular V_{th} (RVT)) et V_{th} bas (Low V_{th} (LVT)), comme on peut le voir à la Fig. 2.2. Le premier conserve la configuration globale des structures bulk, c'est-à-dire que les caissons ont le type de dopage source-drain opposé. Les dispositifs LVT, également appelés "caissons inversés", ont le même type de caisson.

Le FDSOI présente un autre trait intrinsèque et ingénieux, à savoir la possibilité d'utiliser des techniques dynamiques de polarisation du substrat, consistant essentiellement à appliquer une polarisation de tension au caisson situé sous les transistors, comme illustré à la Fig. 2.1(b). En FDSOI, cet attribut est l'aspect essentiel qui confère une grande polyvalence à la technologie, car il ajustera la tension de seuil (V_{th})

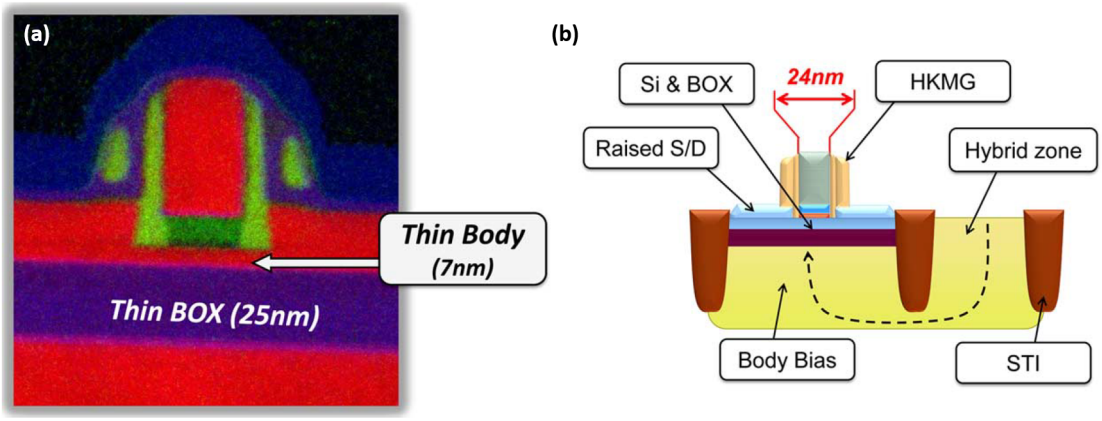

Figure 2.1: *Transistor planar intégré dans CMOS 28nm FDSOI (a) coupe transversale TEM (b) coupe transversale générique.*

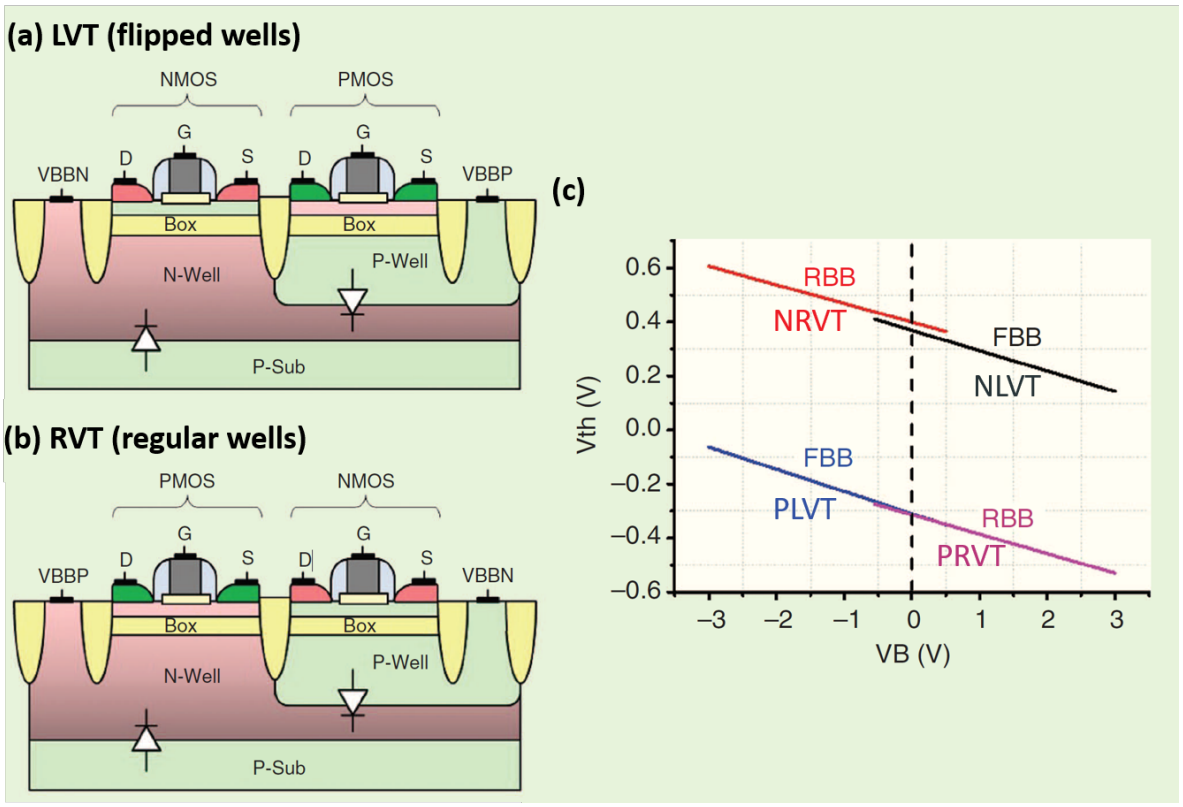

Figure 2.2: *Coupe transversale des transistors C28FDSOI pour les familles : (a) LVT, Low threshold voltage; (b) RVT, Regular threshold voltage; (c) Variation des tensions de seuil selon la tension V_{bb} pour les transistors NMOS et PMOS des deux familles.*

en fonction de la tension du substrat (V_{bb}), que ce soit pour augmenter la vitesse et les performances, FBB (Forward Body Biasing), ou pour réduire la consommation de puissance des courants de fuite, en cas de Reverse Body Biasing (RBB).

Il convient de noter qu'au moins deux épaisseurs pour l'oxyde de grille sont

disponibles dans C28FDSOI, la valeur par défaut étant 18 Å. Des transistors à oxyde de grille plus épais sont également disponibles (28 Å). Les transistors présentant cette plus grande valeur d'épaisseur peuvent être polarisés jusqu'à $V_{DS} = 1.8V$ et sont appelés transistors EG, pour extended gate. Une autre caractéristique intéressante de ces transistors est leur facteur de polarisation plus grand ($\Delta V_{th}/\Delta V_{bb} = 140\,\mathrm{mV/V}$), alors que les transistors à épaisseur de grille normale ont 85 mV/V et ne peuvent être polarisés que jusqu'à $V_{DS} = 1V$.

2.2 Implémentation de SPAD en CMOS FDSOI sous le BOX

Afin de concevoir une SPAD en technologie FDSOI native, deux couches principales ont été adressées pour réaliser la jonction PN: P-well (PW) et Deep N-well (DNW), comme illustré sur la Fig. 2.3. Le premier est classiquement utilisé pour les effets de polarisation de substrat (*body biasing*), et le second (également appelé triple well), étant polarisé via N-Well (NW), est normalement utilisé pour isoler deux différents PW.

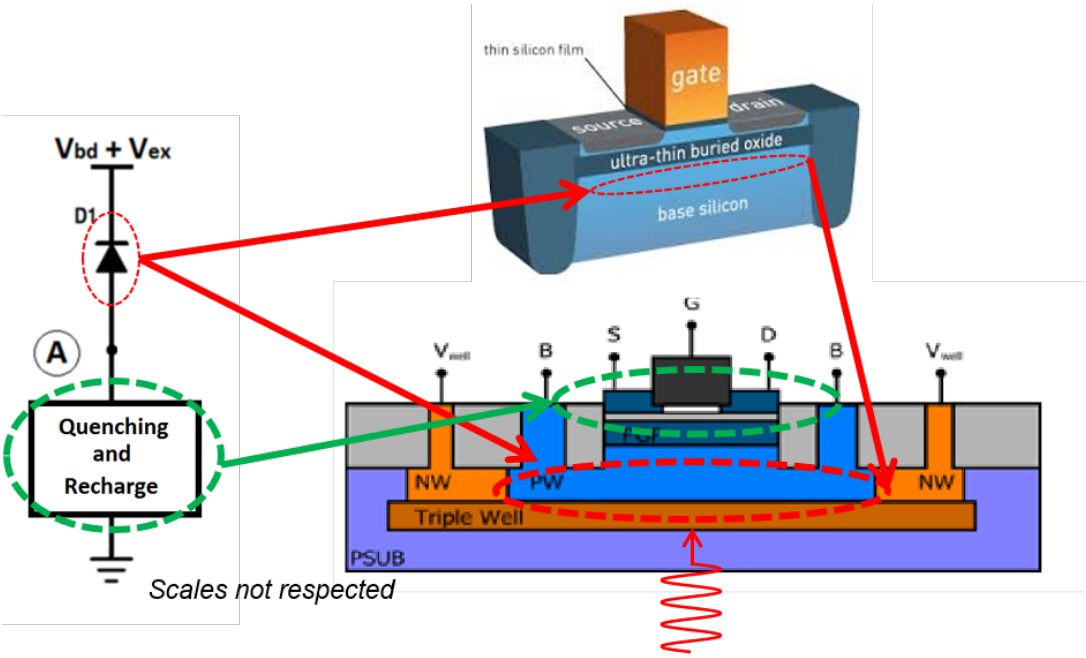

Figure 2.3: *Proposition d'intégration de SPAD dans une technologie CMOS FDSOI sous BOX.*

Puisque PW existe par défaut et que NW est plus dopé que DNW, un claquage prématuré aux bords (Premature Edge Breakdown (PEB)) peut se produire entre PW et NW. Pour éviter ce problème, une couche de BFMOAT du Physical Design Kit (PDK) est introduite entre eux, empêchant les implants P ou N dans cette zone, comme on peut le constater dans les profils de dopage correspondants représentés sur la Fig. 2.4.

2.3 Contraintes de règles de dessin

Pour chaque conception de circuit intégré, les règles technologiques imposent des largeurs, des surfaces et des distances minimales entre les couches afin de garantir la

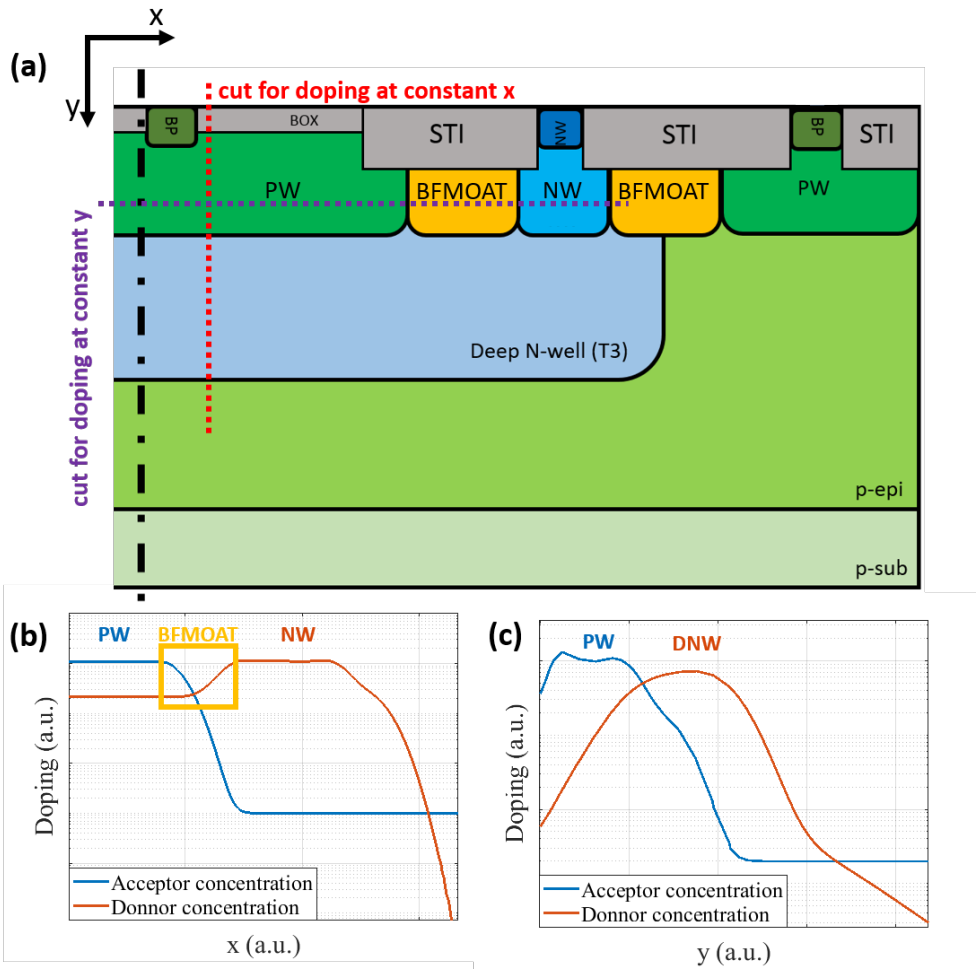

Figure 2.4: *(a) Coupe transversale de SPAD intégrée verticalement dans FDSOI (jonction PW-DNW). Ici, seule la moitié de la cellule est représentée, car elle présente une symétrie cylindrique (échelles non respectées); (b) Profil de dopage à y constant, où la couche de BFMOAT joue le rôle d'anneau de garde; (c) Profil de dopage à x constant, où la jonction SPAD est montrée. Des unités arbitraires ont été utilisées ici pour des raisons de confidentialité.*

faisabilité physique du dessin proposée. Le respect de toutes les règles de conception, parfois très contraignantes, est l'un des défis majeurs de la conception de cellules SPAD dans des technologies commerciales.

Tout d'abord, il faut choisir une géométrie, ce qui est particulièrement difficile en technologie C28FDSOI, car seules les formes orthogonales sont autorisées pour la quasi-totalité des couches du PDK (y compris DNW (T3) et BFMOAT). Cette caractéristique rend difficile l'évitement du PEB, car les arêtes produisent normalement un champ électrique élevé, ce qui produit une probabilité de déclenchement plus élevé sur les arêtes, ce qui n'est pas une fonctionnalité optimisée pour SPAD, dans laquelle un champ électrique uniforme est requis pour maximiser la probabilité de détection de photons (PDP).

De plus, selon les règles de conception de PDK, les contacts de type NW peuvent avoir n'importe quelle forme, à condition qu'ils n'aient que des angles orthogonaux.

Cette caractéristique assure une polarisation très uniforme de la cathode. En revanche, les contacts PW ne peuvent avoir qu'une forme en croix ou en ligne droite, ce qui limite les options de géométrie pour le contact anodique.

Les technologies avancées telles que C28FDSOI nécessitent également une surface plate entre chaque couche de métal, généralement réalisée avec un polissage chimico-mécanique (CMP). Afin de satisfaire à cette spécification, les "fausses tuiles" sont insérées pendant la phase de conception afin d'homogénéiser la densité de chaque couche métallique. Cependant, ils peuvent avoir un impact négatif sur la photodétection s'ils recouvrent la surface photosensible. Une couche d'exclusion doit être utilisée pour éviter ce problème, tout en respectant les valeurs de densité minimale et maximale pour chaque couche du PDK.

Un dernier aspect qui mérite une attention particulière dans le cas de C28FDSOI est la STI qui est par défaut partout dans le circuit. Afin de produire le véritable SPAD FDSOI, la couche RX du PDK doit être utilisée. Elle remplace le STI par la couche physique BOX (25 nm), juste en dessous du film mince de silicium (7 nm).

2.4 Description des cellules

Cellules SPAD

Afin de fournir une SPAD optimisée en C28FDSOI, au cours de la phase de conception du dispositif, plusieurs paramètres de conception ont été modifiés et leur influence sur les performances du système SPAD a été analysée. En particulier: la géométrie, la distance de garde, la taille de la cellule et le circuit d'étouffement associé, ainsi que l'implémentation dans différentes zones (sous BOX, sous STI ou même dans une zone sans SOI (NOSO) - voir Fig. 2.5).

L'intégration dans différentes zones est essentielle pour comprendre l'influence de chaque couche sur les performances des SPAD. Par exemple, en raison de contraintes de règles de dessin, le STI est maintenu sur les bords de la surface photosensible dans les SPAD intégré sous le BOX. Comme il existe une différence significative d'épaisseur d'oxyde (voir Fig. 2.6), les implants traversent une couche plus épaisse d'oxyde de silicium dans la région STI avant d'atteindre le silicium lui-même. Ces processus conduisent à des profils de dopage différents, ce qui implique des performances de SPAD distinctes.

En ce qui concerne la géométrie, trois formes principales ont été conçues: carrée, octogonale et circulaire, comme illustré sur la Fig. 2.7. En raison de contraintes de règles de dessin, toutes les cellules avaient une géométrie d'approximation en marches d'escalier, étant donné que seules les formes orthogonales sont autorisées dans la technologie commerciale. L'objectif principal ici est de vérifier l'influence de la géométrie dans le processus de claquage, y compris les effets de bord.

La distance de garde est définie ici comme la largeur de la couche BFMOAT du PDK, utilisée pour isoler le PW du NW, en évitant le PEB. Deux valeurs ont été utilisées: 3.5 ou 5.0 μm. La taille des cellules était un autre paramètre pris en compte. Cinq dimensions différentes ont été utilisées pour la zone photosensible : pour les cellules octogonales, 500 μm^2 et 1000 μm^2. 785 μm^2 pour les cellules carrées. Pour les cellules circulaires, 615 μm^2 et 2460 μm^2. Ce paramètre est assez important pour mesurer le

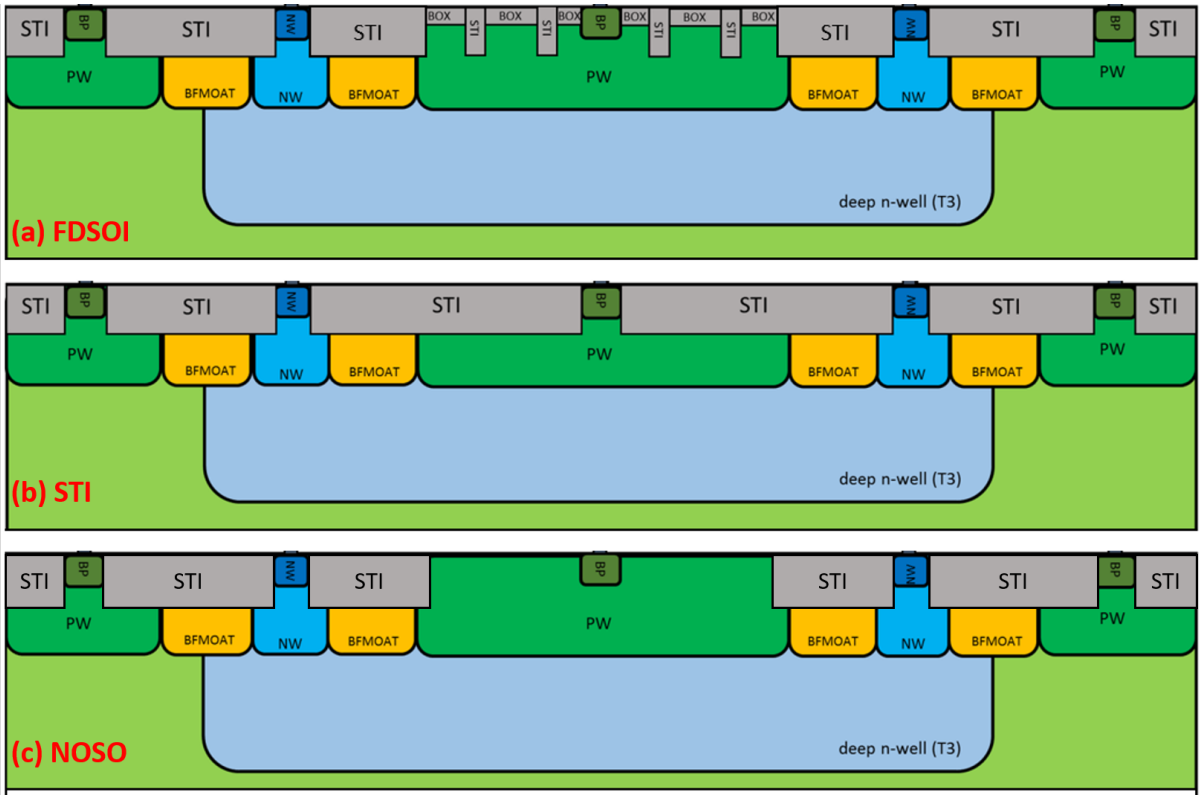

Figure 2.5: *Coupe transversale des trois régions différentes disponibles dans C28FDSOI dans lesquelles la SPAD peut être implémentée: (a) FDSOI; (b) STI; (c) NOSO*

courant d'obscurité dans de tels dispositifs, car il est assez difficile de mesurer des courants inférieurs à 100 fA, ce qui est souvent le cas pour les cellules plus petites.

Cellules de détection indirecte d'avalanche

L'une des principales caractéristiques du C28FDSOI est l'effet de polarisation du substrat sous les transistors. Cette caractéristique intrinsèque peut être facilement explorée pour les cellules SPAD, c'est-à-dire que, lors d'éventuelles avalanches, la tension de seuil des transistors placés sur des cellules SPAD peut être modifiée, ce qui permet de détecter indirectement des événements d'avalanche (voir Fig. 2.8).

Puisque les deux transistors sont placés sur le même caisson P (c'est-à-dire l'anode de la SPAD), un NMOS RVT et un PMOS LVT ont été utilisés. Deux types de transistors ont été utilisés (pour deux cellules de détection indépendantes): un à épaisseur d'oxyde de grille normal et un à oxyde de grille épais.

Le nœud de sortie du pont diviseur V_{out} varie dynamiquement avec l'état de la SPAD. Chaque événement d'avalanche donne une impulsion de tension transitoire positive sur l'anode, c'est-à-dire une augmentation de la tension du PW. Ensuite, $V_{th,n}$ du NMOS diminuera, tandis que la valeur absolue $|V_{th,p}|$ du PMOS augmentera. Une impulsion de tension négative transitoire est alors attendue au noeud de sortie du pont diviseur. Tous les transistors ont comme taille $W = 10\,\mu m$ et $L = 150\,nm$.

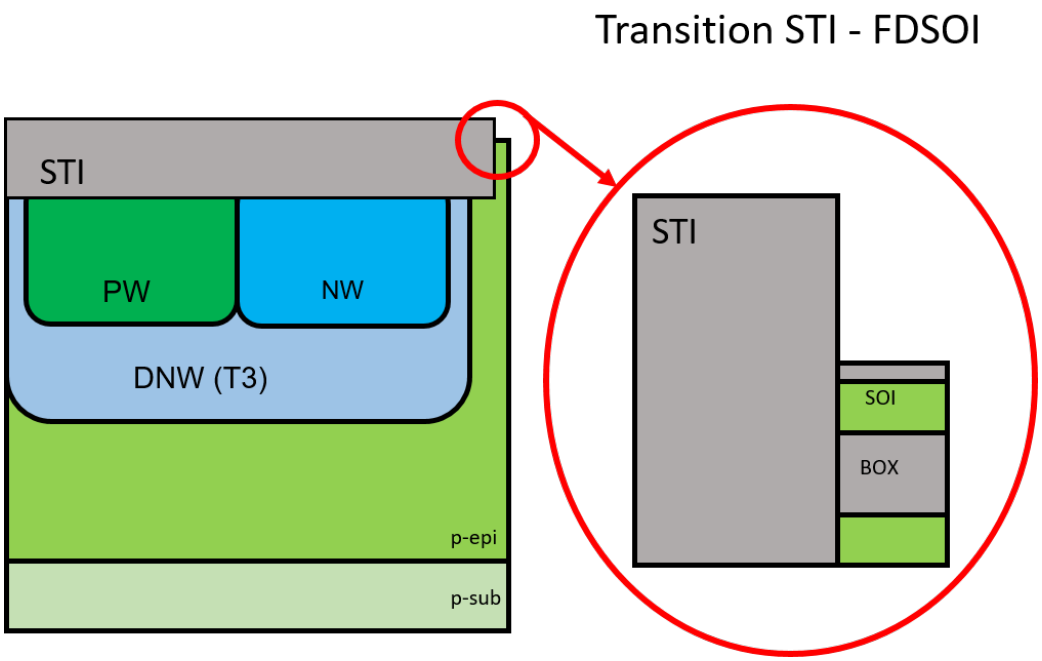

Figure 2.6: *Transition d'une zone STI en FDSOI. La différence de matériau à travers lequel les processus de dopage sont effectués influence les performances de la SPAD.*

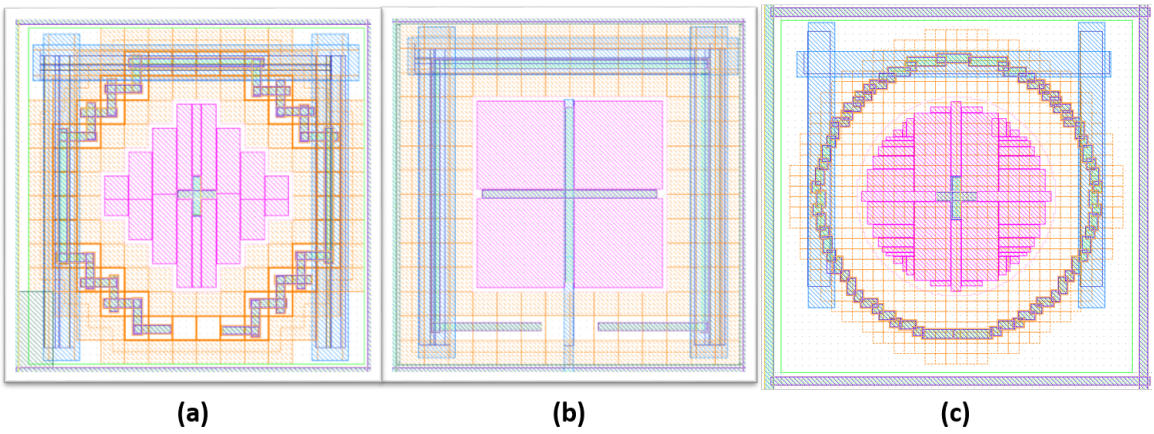

Figure 2.7: *Trois géométries SPAD différentes ont été implémentées: (a) octogonale; (b) carrée; (c) circulaire. Toutes les cellules ont été conçues avec une approximation en marches d'escalier, en raison des exigences des règles de dessin.*

2.5 Diodes Antennes

Lors de la fabrication de circuits intégrés pour des dispositifs CMOS bulk, l'oxyde de grille dans les transistors connectés à un grand chemin de couche métallique peut être endommagé, en raison de ce que l'on appelle l'effet antenne ou dégâts causés par le plasma (Plasma Induced Damage (PID)). Ce phénomène consiste par exemple à collecter des charges dans la couche de grille lors de la gravure plasma. Ces charges

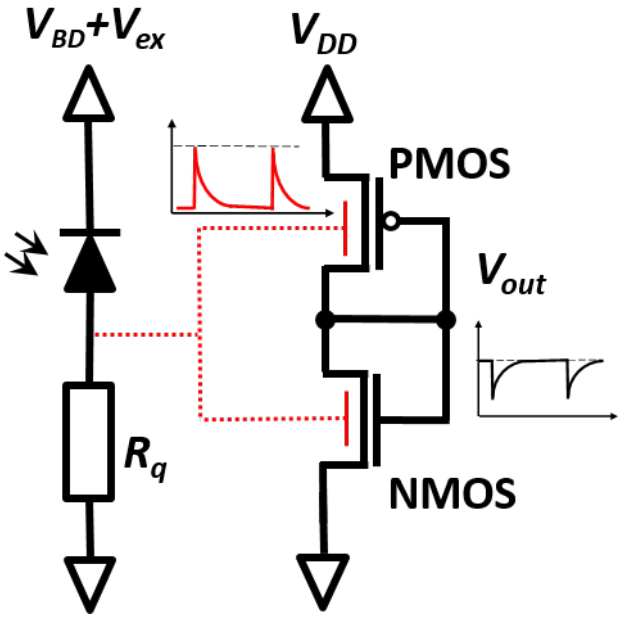

Figure 2.8: *Schéma du circuit de détection indirecte, composé d'un RVT NMOS et d'un LVT PMOS, dans une configuration de pont diviseur, où la tension de sortie varie en fonction des avalanches, grâce à l'effet de polarisation du substrat.*

peuvent produire un courant continu indésirable à travers des oxydes à grille mince, rendant les transistors concernés inutiles. En C28FDSOI, ce problème est encore plus préoccupant, car la source et le drain sont également isolés du substrat par la couche BOX et sont donc exposés aux dégâts causés par le plasma. Pour cette raison, des règles de conception d'antenne supplémentaires sont ajoutées dans le processus C28FDSOI afin d'éviter ce problème.

La solution la plus simple consiste à placer une "diode d'antenne" entre la première couche métallique (M1) et le substrat. Une fois que les charges sont collectées dans les bornes des transistors, elles sont suffisantes pour rompre ces diodes d'antenne, en évacuant les charges dans le substrat et en évitant ainsi d'endommager BOX et l'oxyde de grille.

Dans le cas spécifique de SPAD intégré en C28FDSOI, l'emplacement correct de ces diodes de protection est crucial, car elles peuvent endommager le dispositif SPAD. La plupart du temps, de telles diodes d'antenne sont placées à proximité du transistor connecté, ce qui ne pose pas de problème lorsque le DNW est utilisé dans le seul but d'isoler les différents PW, ce qui n'est pas du tout le cas pour notre SPAD, où ils composent la jonction PN polarisée au-delà de la tension de claquage. Une solution simple mais efficace consiste à les déplacer vers un autre PW qui n'est pas utilisé à des fins SPAD. Dans les puces de test implémentées, le mauvais placement de telles diodes d'antenne était à l'origine du mauvais fonctionnement de certaines cellules SPAD.

2.6 Layout final

Le schéma final, envoyé à la fabrication en passant par circuit multi-projets (CMP), est présenté sur Fig. 2.9. Il est composé de 8 cellules SPAD conçues pour les tests de stations sous pointes (carrés rouges) et de 12 autres cellules pour les tests de PCB (carrés violets). Ces derniers sont connectés à un padring personnalisé composé de cellules de la bibliothèque C28SOI_IO_EXT_ANAF_EG fournie dans le PDK. Des adaptations étaient nécessaires en particulier dans les plots supérieures, utilisées pour la haute tension, où la protection native contre les surtensions devait être supprimée.

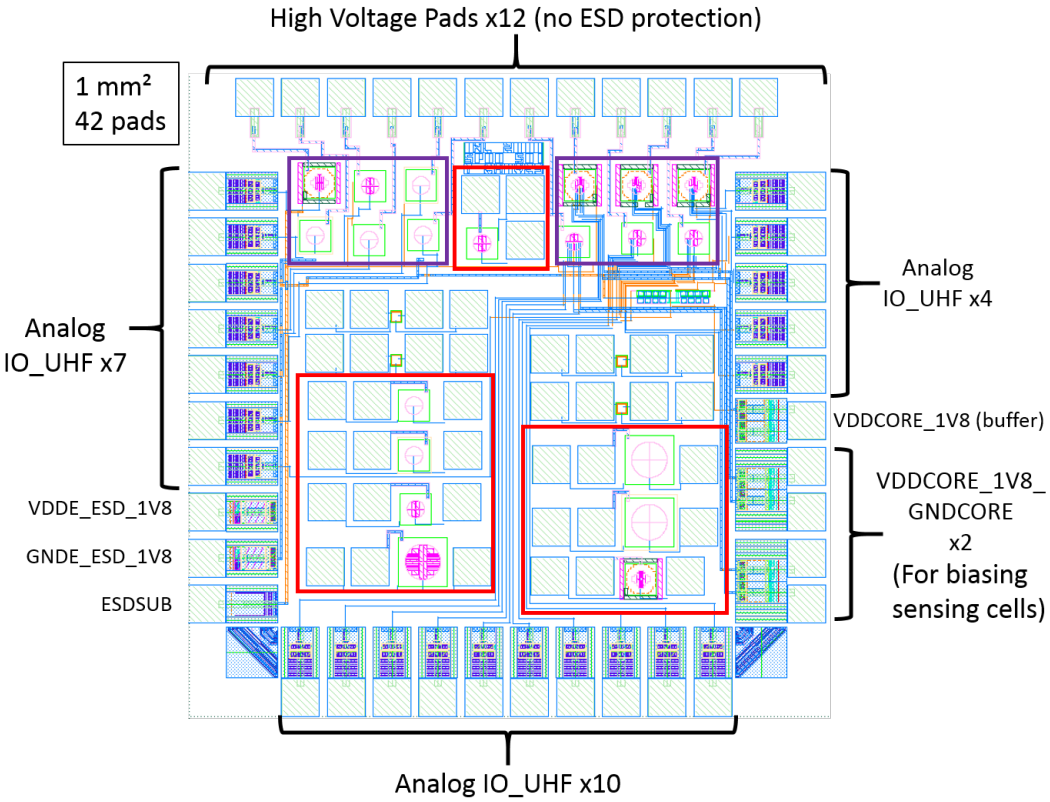

Figure 2.9: *Layout final.*

2.7 Conclusion partielle

Dans cette section, l'implémentation proposée des cellules SPAD en C28FDSOI a été présentée. La technologie a été exposée avec ses principaux avantages, certains d'entre eux étant très intéressants pour l'intégration proposée de SPADs. Au meilleur de notre connaissance, c'est la toute première fois que les SPAD sont intégrés en C28FDSOI, le principal avantage d'une telle réalisation étant la possibilité d'obtenir une structure intrinsèque 3D avec l'optimisation du facteur de remplissage (FF), sans besoin de techniques d'assemblage 3D complexes et chères actuellement utilisées dans l'état de l'art. Notre SPAD est constituée des couches PW et DNW, sous le BOX. Concernant la conception des cellules SPAD, plusieurs paramètres ont été modifiés afin

de vérifier l'influence de chacun sur leurs performances. De nombreux problèmes ont été rencontrés en raison de contraintes de règles de conception, telles que les formes orthogonales obligatoires, la conception des diodes d'antenne. Des cellules de détection indirecte des avalanches ont également été proposées, sur la base du couplage capacitif fourni par la fonction de polarisation du substrat en C28FDSOI. Une telle détection indirecte permet l'utilisation d'un excès de tension plus important, par rapport aux approches directes, et ouvre la voie à une électronique de traitement SPAD plus simple et innovante.

3 Simulation TCAD et modélisation

Dans cette section, nous présentons les travaux de simulation et modélisation qui ont permis de proposer, d'optimiser l'architecture SPAD FDSOI et d'estimer ses performances. Cette section présente tout d'abord la définition de la structure pour la simulation électrique TCAD (logiciel de simulation : Synopsys Sentaurus), puis les équations de base et les principaux modèles utilisés. Ensuite, quelques résultats importants sont donnés en présentant la méthodologie de simulation à suivre en fonction du type d'information à extraire. Finalement, une approche analytique complémentaire est présentée pour obtenir la probabilité de déclenchement avec un calcul original, puis l'estimation du bruit dans l'obscurité et de l'efficacité de détection des photons.

3.1 Définition de la structure pour la simulation électrique

Géométrie

La géométrie a été créée avec le module Structure Editor (SDE) de Synopsys Sentaurus (Fig. 3.1) La structure est 2D avec un axe de symétrie en X=0, ce qui correspond à une pseudo-simulation 3D avec une symétrie cylindrique. L'avantage de cette approche est de définir seulement la demie-structure avec un gain en temps de simulation.

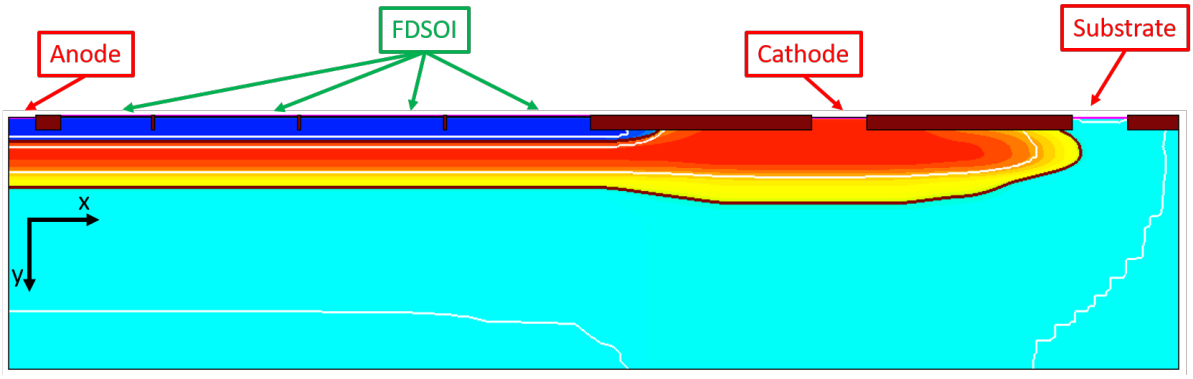

Figure 3.1: *Structure décrite pour la simulation TCAD: géométrie 2D avec symétrie cylindrique*

Dopages

La description des dopages des différentes zones est un prérequis à toute simulation électrique. Les profils de dopage ont été simulés à 1D (module SPROCESS) puis importés dans le module Structure Editor (SDE) pour reconstituer la structure 2D à symétrie cylindrique. Dans la Fig. 3.1, la zone bleue correspond au caisson P ou « P-well » PW, la zone rouge-orange au caisson N « N-well - NW et au caisson N profond « deep N-well » DNW. Les zones en brun – rouge foncé correspondent aux tranchées d'isolation (« Shallow Trench Isolation » - STI). La zone d'oxyde enterrée (« Burried oxide » - BOX 25 nm) ainsi que la fine couche de silicium (7 nm) ne sont discernables sans un zoom à la surface. Les échelles ne sont pas données pour raison de confidentialité.

Simulation TCAD de l'implantation du caisson N profond (DNW)

Lors de la phase de caractérisation, des différences ont été observées entre les diodes SPAD implantées dans une zone FDSOI (présence du BOX et du film silicium) et dans une zone 100% STI (sans film silicium). Nous avons ainsi relevé une tension de claquage légèrement plus faible ainsi qu'une image d'électroluminescence plus homogène (et du champ électrique associé) pour la SPAD dans la zone STI. Dans le procédé de fabrication, toutes les implantations sont réalisées au travers des couches BOX, STI, film silicium (lorsque celles-ci existent). Pour mieux reproduire le profil de dopage, la simulation SPROCESS 1D a été réalisée dans les deux cas : zone FDSOI et zone STI. La Fig. 3.2 illustre les profils obtenus. Nous notons ainsi un profil légèrement plus abrupt du profil dans la zone STI qui explique une tension de claquage plus faible pouvant entraîner une courant tunnel (« band-to-band tunneling ») plus élevé.

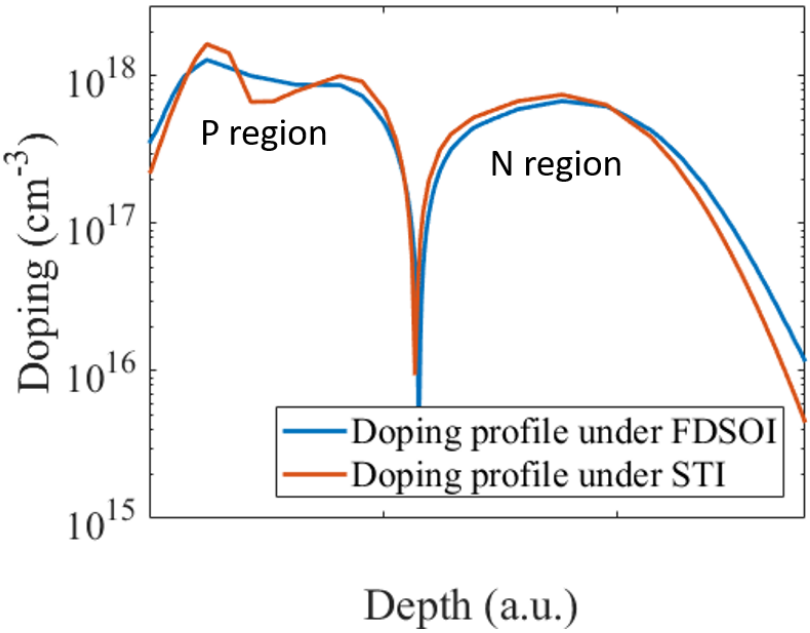

Figure 3.2: *Dopage net simulé en 1D sous les zones FDSOI et STI.*

Proposition de modification du caisson N profond (DNW)

La caractérisation électrique du premier lot de SPAD fabriqué avec la technologie native C28FDSOI a montré que la tension de claquage semblait un peu faible (inférieure à 10 V, voir section 4) pouvant expliquer un courant d'obscurité élevé lié à la présence d'un courant tunnel assisté par pièges. En accord avec le fondeur, il a été possible de proposer une modification du process (la plus simple possible) visant à monter la tension de claquage. Notre choix s'est porté sur une modification des conditions d'implantation du caisson N profond (DNW). Des simulations process associées aux simulations électriques ont été lancées pour dégager le nouveau jeu de paramètres d'implantation (énergie, dose etc.). La Fig. 3.3 illustre la coupe schématique de la

structure simulée à gauche ainsi que le profil de dopage net obtenu avec le process original-natif et le process modifié.

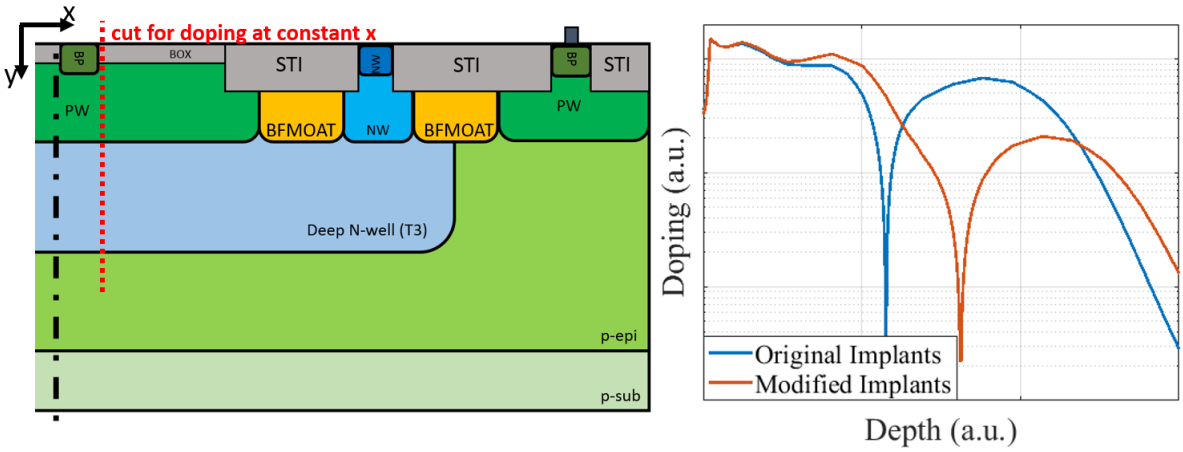

Figure 3.3: *Structure schématique simulée et dopage net simulé en 1D avec les process original et modifié (implantation du caisson N profond)*

3.2 Simulations électriques: Physique and Modèles

Les simulations électriques TCAD ont été obtenues avec le module SDEVICE de Synopsys - Sentaurus. Dans ce paragraphe, nous décrivons les équations physiques utilisés pour le calcul du transport des charges ainsi que les principaux modèles (génération-recombinaison, avalanche, courant tunnel « band-to-band tunneling »).

Transport des charges

L'approche classique appelée dérive-diffusion a été choisie, donnée par les équations 4.4 et 4.5, respectivement pour les électrons et les trous.

$$\vec{J_n} = e\mu_n n\vec{E} + eD_n\vec{\nabla}n \tag{4.4}$$

$$\vec{J_p} = e\mu_p p\vec{E} - eD_p\vec{\nabla}p \tag{4.5}$$

avec:
$e = 1.6 \times 10^{-19}$ C la charge élémentaire
$\vec{E}$ le champ électrique

Et, respectivement pour les électrons et les trous: :

$\vec{J_n}$ et $\vec{J_p}$ les densités de courant
μ_n et μ_p les mobilités
n et p les densités de concentration
D_n et D_p les constantes de diffusion
$\vec{\nabla}n$ et $\vec{\nabla}p$ les gradients de concentration

Coefficients d'ionisation et génération par avalanche

Le processus d'avalanche lié à l'ionisation par impact est à l'origine du déclenchement des SPADS lors de l'absorption d'un photon (génération d'une paire électron-trou). Le taux de génération de paires électron-trou lié à l'ionisation par impact est donné par l'Eq. 4.6.

$$G_{II} = \alpha_n n v_n + \alpha_p p v_p \tag{4.6}$$

avec, respectivement pour les électrons et les trous :
α_n et α_p les coefficients d'ionisation.
v_n et v_p les vitesses des porteurs.

Physiquement, les coefficients d'ionisation représentent le nombre de paires électron-trou générés par unité de longueur traversée par l'électron ou le trou accéléré par le champ électrique (unité cm^{-1}). Ces coefficients sont très importants pour une bonne description du processus d'avalanche et vont directement influencer : les probabilités d'avalanche, la tension de claquage, la caractéristique I-V inverse etc. Plusieurs modèles sont disponibles (dépendant du champ électrique, température etc.). Tous les modèles contiennent des paramètres à calibrer avec des données expérimentales. Parmi les différents modèles étudiés et utilisés dans notre travail, nous avons gardé Okuto-Crowell (équation 4.7) [11], qui donne les meilleurs approximations des caractéristiques obtenues expérimentalement.

$$\alpha(E) = a\,(1 + c(T - T_0))\,E^{\gamma} \exp\left[-\left(\frac{b\,[1 + d(T - T_0)]}{E}\right)^{\delta}\right] \tag{4.7}$$

Génération de porteurs dans la zone de charge d'espace

Mise à part la photogénération de porteurs (mécanisme privilégié dans la SPAD), d'autres phénomènes peuvent générer des paires électron-trou dans ou à proximité de la zone de charge d'espace (zone de multiplication) susceptibles de déclencher une avalanche indésirable et contribuant au bruit dans l'obscurité. Différents processus de génération-recombinaison de porteurs sont décrits dans cette section et permettront de mieux comprendre les performances et limitations de notre SPAD FDSOI dans le chapitre 4.

Shockley-Read-Hall Le mécanisme principal de génération-recombinaison associé à la présence de défauts profonds dans le gap et activé thermiquement est décrit par le formalisme de Shockley-Read-Hall (SRH). Ce processus SRH est décrit dans Sentaurus SDevice par le terme R_{net}^{SRH}, qui représente le taux de recombinaison SRH moins le taux de génération SRH, comme donné dans l'équation 4.8.

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p(n + n_1) + \tau_n(p + p_1)} \tag{4.8}$$

avec:

$$n_1 = n_{i,eff} \exp\left(\frac{E_{trap}}{kT}\right) \tag{4.9}$$

et

$$p_1 = n_{i,eff} \exp\left(\frac{-E_{trap}}{kT}\right) \tag{4.10}$$

Dans laquelle

E_{trap} est la position énergétique du défaut par rapport au milieu du gap (zéro par défaut).

$n_{i,eff}$ est la densité intrinsèque effective (prenant en compte la réduction du gap avec le dopage « bandgap narrowing »).

τ_n and τ_p sont les durées de vie des électrons et des trous, respectivement.

La durée de vie des porteurs dépend à la fois du dopage, de la température et du champs électrique (modèle de Hurkx) qui représente l'effet des pièges « Trap Assisted Tunneling (TAT) » c'est-à-dire une combinaison du courant tunnel (« Band To Band Tunneling » -B2B) avec le processus de génération-recombinaison Shockley-Read-Hall (SRH).

Courant tunnel bande à bande (« Band To Band Tunneling ») Le courant tunnel bande à bande se produit dans les jonctions abruptes fortement dopées et polarisées pour courber les bandes de conduction et de valence, il est dénommé « Band To Band Tunneling - B2B ». De nombreux modèles empiriques existent: Hurkx, Schenk et Liou. Dans notre structure, tous les modèles ont été testés sans trop de différence observée. Ainsi nous avons sélectionné le modèle le plus simple ; celui de Liou, Eq. 4.11 [12] (valide pour les forts champs, ce qui est notre cas).

$$G^{B2B} = AE^P \exp\left(-\frac{B}{E}\right) \tag{4.11}$$

3.3 Simulations TCAD : méthodologie et résultats

La Fig. 3.4 donne une vue d'ensemble sur la méthodologie mise en place pour utiliser efficacement les outils TCAD et ensuite reprendre certaines données dans des routines analytiques en post-processing afin d'extraire certaines figures de mérite. En partant de la gauche de la Fig. 3.4, la simulation process 1D (SPROCESS) donne les profils de dopage permettant de créer la structure complète 2D (SDE) pour ensuite adresser la simulation électrique (SDEVICE) avec plusieurs options décrites dans les sections suivantes (méthode dite « Resistor » avec ou sans avalanche, méthode appelée « Approximate Breakdown Analysis » - ABA) et finalement certaines données issues des simulations TCAD permettent de calculer analytiquement la probabilité d'avalanche (avalanche triggering probability - ATP), le bruit dans l'obscurité (Dark Count Rate - DCR) et la probabilité de détection des photons (Photon Detection Probability - PDP).

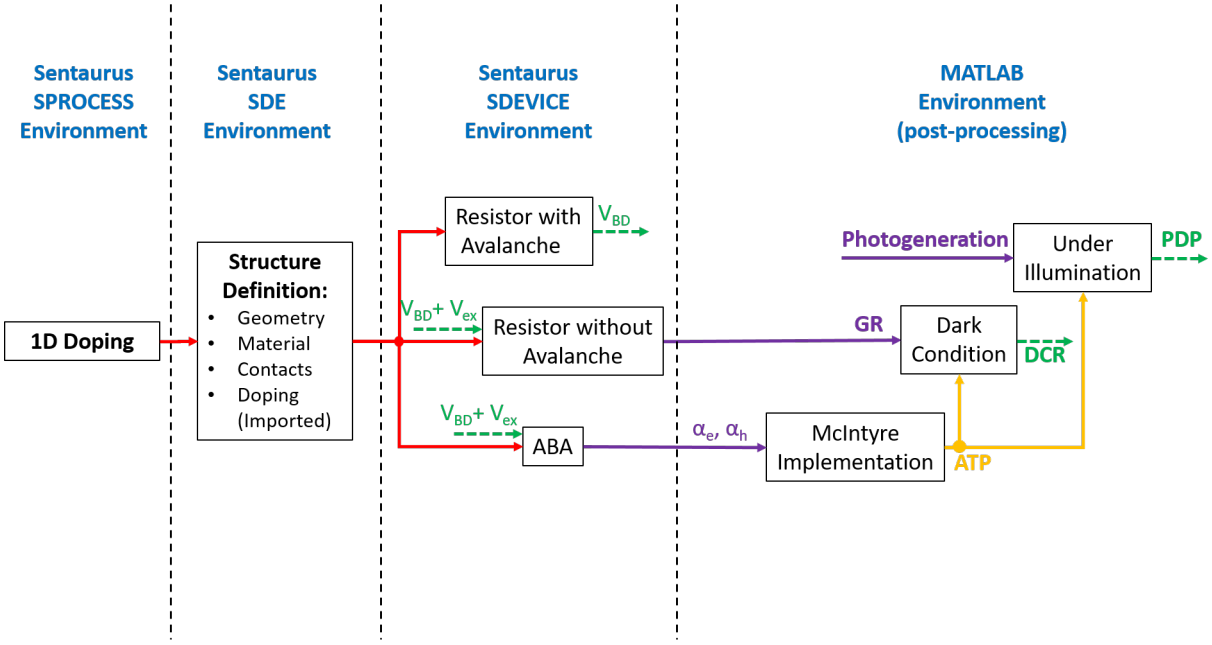

Figure 3.4: *Méthodologie pour l'utilisation des outils TCAD et des routines en post-processing.*

Simulation Resistor avec avalanche

La détermination de la tension de claquage de la SPAD est la première information à obtenir en simulation. Elle peut être extraite d'une simulation dite « resistor avec avalanche » ou alors avec la méthode appelée « Approximate Breakdown Analysis » - ABA (décrite plus loin). La simulation dite « resistor avec avalanche » est la plus précise (mais la plus longue en temps de calcul) pour extraire la tension de claquage. Cette méthode est en réalité une simulation associant la diode SPAD (en 2D avec symétrie cylindrique dans notre cas) avec une résistance en série pour permettre d'obtenir la caractéristique I-V complète sans problème de convergence lors de l'avalanche (simulation en régime permanant). La Fig. 3.5 donne la caractéristique inverse I-V simulée de notre structure SPAD FDSOI avec le process original (tension de claquage de 9.6 V à température ambiante) et le process modifié (implantation du caisson N profond ajusté pour augmenter la tension de claquage à 15.8 V en raison d'une jonction moins abrupte).

Cette méthode permet aussi d'obtenir l'évolution de la tension de claquage en fonction de la température dont la pente lorsqu'elle positive est bien la signature d'une avalanche liée au processus d'ionisation par impact (Fig. 3.6).

Simulation Resistor sans avalanche

Ce type de simulation sans le mécanisme d'avalanche activé permet d'obtenir l'état de la structure juste avant que l'avalanche se déclenche en raison de la présence d'une paire électron-trou dans la zone de multiplication. Ainsi, il est possible d'avoir la cartographie du champ électrique, les taux de génération par différents processus (SRH, B2B etc.) pour une tension de polarisation au-delà de la tension de laquage ($V_{BD} + V_{ex}$).

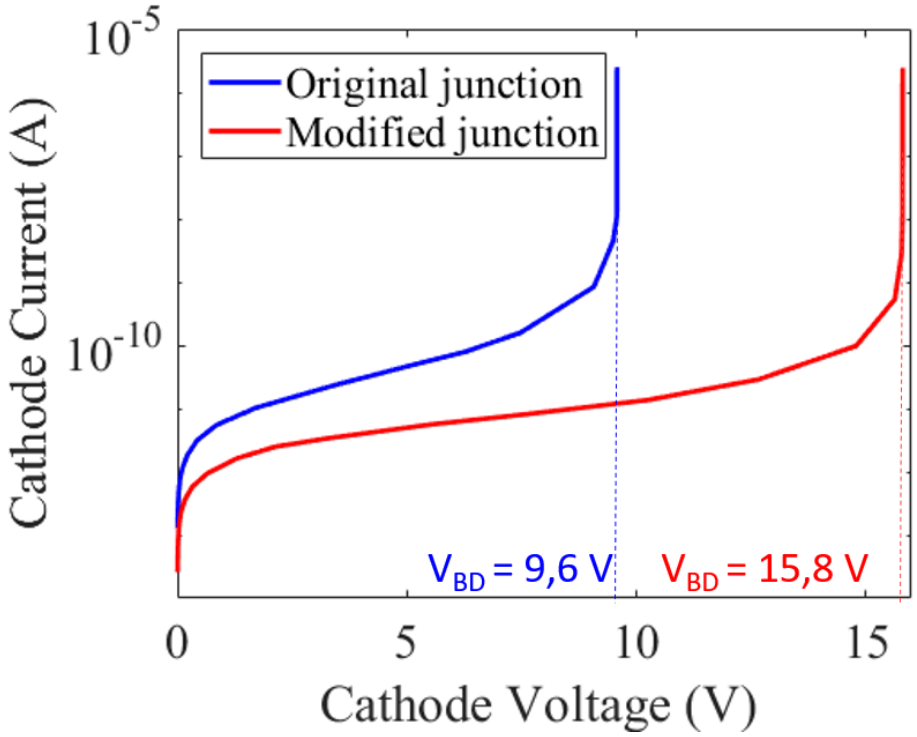

Figure 3.5: *Caractéristique I-V obtenue par la simulation TCAD avec la méthode dite "resistor, avalanche ON », à température ambiante. La tension de claquage V_{BD} extraite est de 9.6 V avec le profil de dopage original et de 15.8 V avec le profil modifié du caisson N profond.*

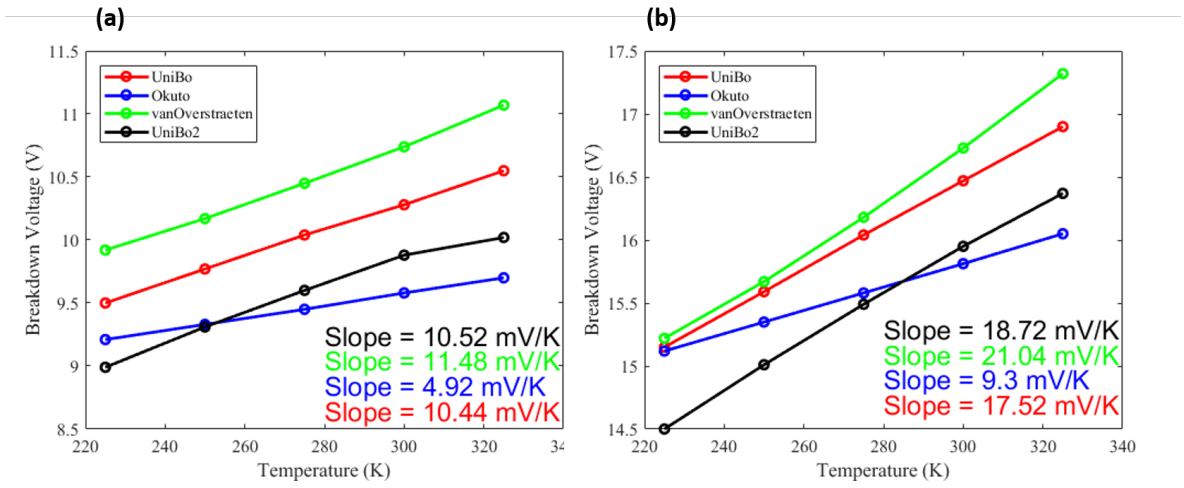

Figure 3.6: *Simulation de la tension de claquage en fonction de la température pour le dopage initial (a) et le dopage modifié du caisson N profond (b) avec différents modèles d'ionisation par impact.*

La Fig. 3.7 donne un exemple de résultats avec la carte 2D de champ électrique et le tracé en fonction de la profondeur des taux de génération-recombinaison des porteurs

par les processus SRH et B2B pour le dopage initial et le dopage modifié du caisson N profond. Sur cette figure, on note que le champ est homogènement réparti le long de la jonction. Une analyse plus fine laisserait apparaître une zone où le champ électrique est légèrement plus fort sous le STI dans le bord du caisson P. L'adoucissement du profil de dopage avec la modification de l'implantation du caisson N profond baisse le niveau du champ électrique de façon générale, augmente la tension de claquage et surtout permet d'abaisser les taux de génération notamment B2B (Fig. 3.7 (c)) avec, en conséquence, une diminution attendue du taux de comptage dans l'obscurité (DCR - Dark Count Rate).

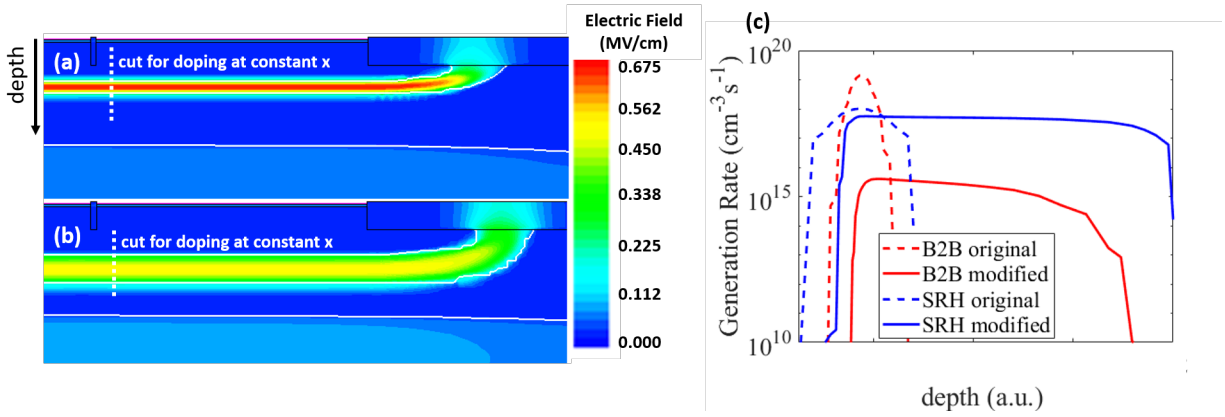

Figure 3.7: *Carte du champ électrique pour le dopage initial (a) et le dopage modifié du caisson N profond (b) pour $V_{ex} = 1V$). (c) Taux de génération-recombinaison (SRH and B2B) en fonction de la profondeur à une position x donnée. Ces résultats sont obtenus en simulations sans activer l'avalanche.*

Méthode Approximate Breakdown Analysis (ABA)

La méthode dite ABA pour « Approximate Breakdown Analysis » utilise les intégrales d'ionisation ϕ_e et ϕ_h (qui dépendent des coefficients d'ionisation) sans calcul de courant, pour extraire la tension de claquage. Elle est beaucoup plus rapide, moins précise mais elle permet d'atteindre des points de fonctionnement bien au-delà de la tension de claquage (à une tension d'excès au-delà de la tension de claquage) afin d'extraire les données internes juste avant le déclenchement ; notamment pour extraire les coefficients d'ionisation (et ensuite calculer analytiquement l'ATP, le DCR le PDP).

Le formalisme de la détermination de l'avalanche avec les intégrales d'ionisation (méthode ABA) est donné par les équations ci-après, Eq. 4.12 à Eq 4.21.

$$G^{II} = \alpha_n n v_n + \alpha_p p v_p \tag{4.12}$$

qui peut se réécrire :

$$G^{II} = \alpha_n \frac{J_n}{q} + \alpha_p \frac{J_p}{q} \tag{4.13}$$

La densité de courant étant constante :

$$J = J_n(x) + J_p(x) \tag{4.14}$$

Pour une jonction PN, avec position $x = W$ (à la limite de la ZCE du côté N), la densité de courant de trous atteint son maximum en W et $J_p(W) = J$. On peut déduire la valeur $J_p(0)$:

$$J_p(x) = M_P J_p(0) = J \tag{4.15}$$

avec M_P le facteur multiplicatif lors de l'avalanche
La variation de J_p à travers la ZCE est donnée par l'équation:

$$\frac{dJ}{dx} = G \tag{4.16}$$

$$dJ_p = J_p \alpha_p dx + J_n \alpha_n dx \tag{4.17}$$

soit:

$$\frac{dJ_p}{dx} - J_p(\alpha_p - \alpha_n) = J\alpha_n \tag{4.18}$$

La solution en prenant en compte la condition au limite permet d'obtenir :

$$1 - \frac{1}{M_P} = \int_0^W \alpha_p \exp\left(-\int_0^x (\alpha_p - \alpha_n)dx\right)dx = \phi_p \tag{4.19}$$

Lorsque l'avalanche apparaît, le gain (M_P) tend vers l'infini, c'est à dire que l'intégrale d'ionisation tend vers 1:

$$1 = \int_0^W \alpha_p \exp\left(-\int_0^x (\alpha_p - \alpha_n)dx\right)dx = \phi_p \tag{4.20}$$

Une étude similaire peut être menée si c'est l'électron qui est responsable du déclenchement de l'avalanche pour obtenir l' Eq. 4.21. La figure 3.8 représente les valeurs des coefficients d'ionisation en fonction de la profondeur pour un point de polarisation donnée ainsi que le tracé des intégrales d'ionisation en fonction de la polarisation pour extraire la tension de claquage lorsque celles-ci se croisent à la valeur 1.

$$1 = \int_0^W \alpha_n \exp\left(-\int_0^x (\alpha_n - \alpha_p)dx\right)dx = \phi_n \tag{4.21}$$

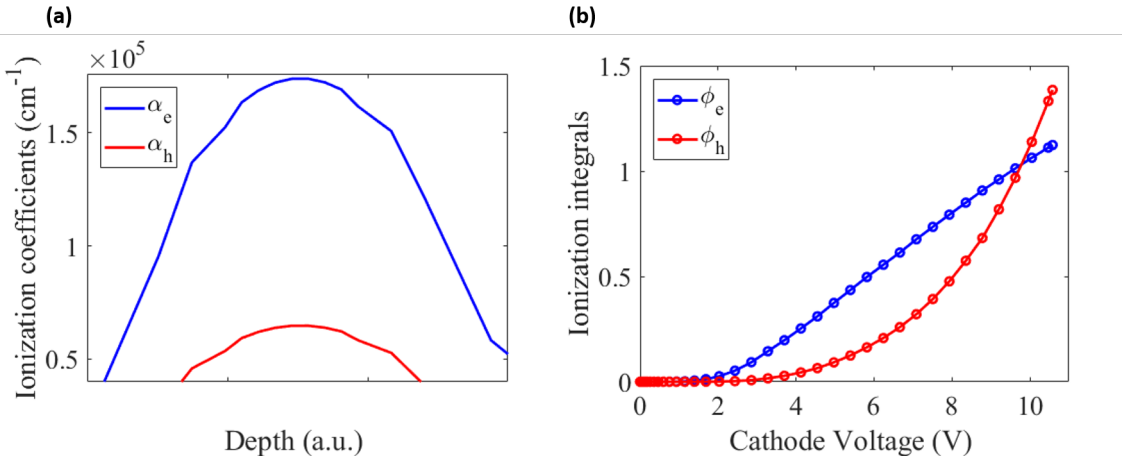

Figure 3.8: *(a) Extraction des coefficients d'ionisation pour la structure présentée sur la Fig. 3.7, à la même position (b) Tracé des intégrales d'ionisation pour les électrons et les trous (méthode ABA) permettant d'extraire rapidement la tension de claquage lorsque celles-ci se croisent à la valeur 1.*

3.4 Calculs analytiques en Post-Processing pour estimer les performances de notre SPAD

En se référant à la Fig. 3.6, les données issues de la simulation TCAD nous permettent d'estimer grâce à des routines analytiques (implémentées sous Matlab) les principales figures de mérite de notre SPAD telles que la probabilité de déclenchement d'une avalanche (Avalanche Triggering Probability - ATP), le taux de comptage dans l'obscurité (Dark Count Rate - DCR) et l'efficacité de détection des photons (Photon Detection Probability - PDP).

Calcul de la probabilité d'avalanche

La probabilité de déclenchement d'une avalanche (Avalanche Triggering Probability - ATP) est la première information à obtenir car elle est nécessaire pour estimer le taux de comptage dans l'obscurité (Dark Count Rate - DCR) et l'efficacité de détection des photons (Photon Detection Probability - PDP). Dans une approche 1D, le modèle de McIntyre est largement utilisé pour calculer l'ATP que l'on note $P_P(x)$, qui s'écrit sur l'Eq. 4.22 [13] :

$$P_P(x) = P_e(x) + P_h(x) - P_e(x)P_h(x) \tag{4.22}$$

avec
$P_e(x)$ et $P_h(x)$ les probabilités qu'un électron ou un trou déclenche une avalanche. L'Eq. 4.22 peut se réécrire:

$$P_P(x) = 1 - (1 - P_h(x))(1 - P_e(x)) \tag{4.23}$$

$$\frac{dP_P}{dx} = (1 - P_e)\frac{dP_h}{dx} + (1 - P_h)\frac{dP_e}{dx} \tag{4.24}$$

A partir du travail de Oldham, en 1972 [14]:

$$\frac{dP_e}{dx} = (1 - P_e)\alpha_e P_P \tag{4.25}$$

$$\frac{dP_h}{dx} = (1 - P_h)\alpha_h P_P \tag{4.26}$$

En remplaçant Eq. 4.25 et 4.26 dans Eq. 4.24, nous obtenons :

$$\frac{dP_P}{dx} = (\alpha_e - \alpha_h)P_P(1 - P_P) \tag{4.27}$$

Les conditions aux limites imposent :

$$P_e(0) = 0 \tag{4.28}$$

$$P_h(W) = 0 \tag{4.29}$$

et :

$$P_P(0) = P_h(0) \tag{4.30}$$

$$P_P(W) = P_e(W) \tag{4.31}$$

Avec les conditions aux limites, McIntyre propose une solution de l'Eq. 4.27 [13]:

$$P_P(x) = \frac{P_h(0)f(x)}{P_h(0)f(x) + 1 - P_h(0)} = ATP(x) \tag{4.32}$$

avec

$$f(x) = \exp\left(\int_0^x (\alpha_e - \alpha_h)dx\right) \tag{4.33}$$

En remplaçant Eq. 4.32 dans l'Eq. 4.26, nous obtenons :

$$P_h(x) = 1 - (1 - P_h(0)) \exp\left(\int_0^x \alpha_h(x) P_P(x) dx\right) \tag{4.34}$$

Pour obtenir une solution de l'Eq. 4.32, $P_h(0)$ doit être déterminée en résolvant l'Eq. 4.34, qui peut se réécrire:

$$-\ln\left[1 - P_h(0)\right] = \int_0^W \frac{P_h(0)\alpha_h(x)f(x)}{P_h(0)f(x) + 1 - P_h(0)} dx \tag{4.35}$$

Deux intégrations numériques sont nécessaires pour obtenir $P_P(x)$ ce qui peut être très long dans une simulation 2D ou 3D et incompatible avec une approche analytique compacte. Nous avons ainsi proposé dans la section suivante une nouvelle approche, plus compacte et moins lourde en calculs avec quelques hypothèses amenant des simplifications.

Proposition d'une méthode pour simplifier les calculs de McIntyre Partant du constat que dans notre zone d'intérêt (à fort champ), les coefficients d'ionisation varient linéairement avec le champ électrique, le modèle Okuto-Crowell peut se réécrire à fort champ :

$$\lim_{E\to\infty} \alpha_{OC}(E) = aE \tag{4.36}$$

Avec

$$\int_0^x E(x)dx = \int_{V(0)}^{V(x)} -dV = V(0) - V(x) \tag{4.37}$$

Pour un point x de la zone à fort champ ($x_a < x < x_b$), l'approximation linéaire permet d'écrire l'Eq. 4.38

$$\alpha(E) = \beta E \tag{4.38}$$

β_e and β_h peuvent être déterminés avec la valeur prise au champ max (high field - HF) du modèle Okuto-Crowell:

$$\beta_{HF} = a \tag{4.39}$$

On introduit un facteur d'ajustement noté γ tel que :

$$\beta = \frac{\beta_{HF}}{\gamma} \tag{4.40}$$

Ainsi :

$$\alpha = \begin{cases} \beta E(x), & \text{si } x_a < x < x_b \\ 0, & \text{sinon} \end{cases} \tag{4.41}$$

La fonction f(x) (Eq. 4.33) s'écrit alors:

$$f(x) = \exp\left(\int_0^x (\alpha_e - \alpha_h)dx\right) \tag{4.42}$$

$$f(x) = \exp\left(\int_{V(x_a)}^{V(x)} -(\beta_e - \beta_h)dV\right) \tag{4.43}$$

$$f(x) = \begin{cases} \exp\left((\beta_e - \beta_h)(V(x_a) - V(x))\right), & \text{pour } x_a < x < x_b \\ \exp\left((\beta_e - \beta_h)(V(x_a) - V(x_b))\right), & \text{pour } x > x_b \end{cases} \tag{4.44}$$

La probabilité $P_h(x)$ peut se réécrire en introduisant le terme $I(x)$ as:

$$I(x) = \int_0^x \alpha_h(u)P_P(u)du \tag{4.45}$$

$$I(x) = \int_0^x \frac{\alpha_h(u)P_h(0)f(u)}{1 - P_h(0) + P_h(0)f(u)}du \tag{4.46}$$

En déroulant le calcul (non détaillé ici), nous obtenons :

$$P_h(x) = 1 - (1 - P_h(0))\left[1 - P_h(0) + P_h(0)\exp\left((\beta_e - \beta_h)(V(x_a) - V(x))\right)\right]^{\frac{\beta_h}{\beta_e - \beta_h}} \tag{4.47}$$

$$0 = 1 - (1 - P_h(0))\left[1 - P_h(0) + P_h(0)\exp\left((\beta_e - \beta_h)(V(x_a) - V(x_b))\right)\right]^{\frac{\beta_h}{\beta_e - \beta_h}} \tag{4.48}$$

Et pour les électrons:

$$P_e(x) = 1 - \left[1 - P_h(0) + P_h(0)\exp\left((\beta_e - \beta_h)(V(x_a) - V(x))\right)\right]^{\frac{\beta_e}{\beta_e - \beta_h}} \tag{4.49}$$

Les équations 4.47 and 4.49 donnent les expressions analytiques de $P_h(x)$ et $P_e(x)$, et $P_h(0)$ doit être extrait de la résolution numérique de 4.48. Cette approche a été validée tel que montré sur la Fig. 3.9. Une étude complémentaire (non présentée ici) sur la calibration du l'approche simplifiée a été menée (ajustement du facteur noté γ).

Taux de comptage dans l'obscurité (Dark Count Rate – DCR)

Le calcul du taux de comptage dans l'obscurité (Dark Count Rate – DCR) est donné par l'Eq. 4.50, en se limitant aux termes de génération-recombinaison dans la ZCE :

$$DCR = \int_{x_a}^{x_b} ATP(x)GR(x)dx \tag{4.50}$$

avec:

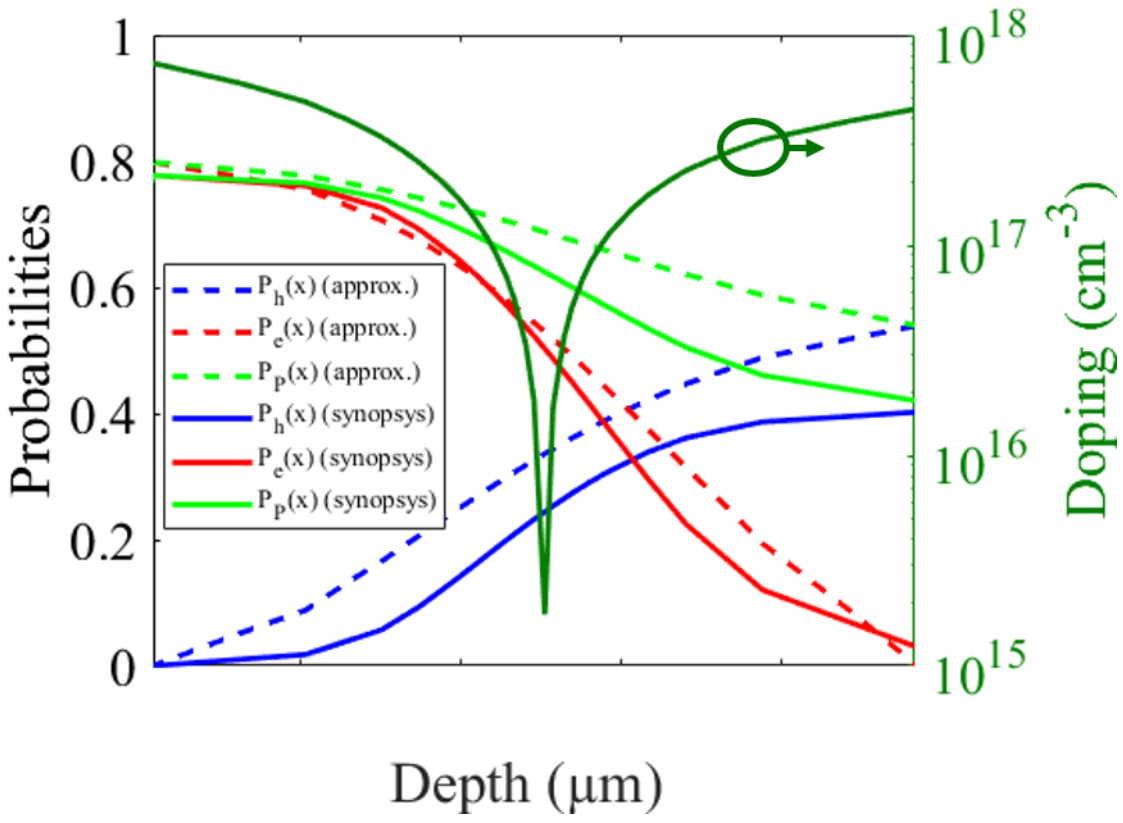

Figure 3.9: *Calculs de la probabilité de déclencher une avalanche : approche rigoureuse de McIntyre et approche simplifiée (notre proposition).*

x_a et x_b les positions limites de la ZCE
$ATP(x)$ la probabilité d'avalanche en fonction de la position
$GR(x)$ taux de génération-recombinaison (exemple SRH, B2B)

Cette approche analytique a été implémentée dans Matlab et donne les résultats $DCR = f(Vex)$ pour différentes températures et $DCT = f(1/T)$ pour différentes tensions d'excès V_{ex} dans les figures Fig. 3.10 pour le process original et Fig. 3.11 pour le process modifié (dopage modifié du caisson N profond). Nous vérifions que le process modifié donne des niveaux de DCR plus bas (moins de génération-recombinaison de type B2B, cf. Fig. 3.7).

Probabilité de Détection des Photons

Dans une approche simplifiée ne prenant en compte que l'absorption des photons dans la ZCE avec une probabilité d'absorption donnée par la loi de Beer-Lambert (Eq. 4.51), la probabilité de détection des photons (« Photon Detection Probability » – PDP) se calcule avec l'Eq. 4.52

$$P_{abs} = \alpha_{Si} \exp(-\alpha_{Si} z) \tag{4.51}$$

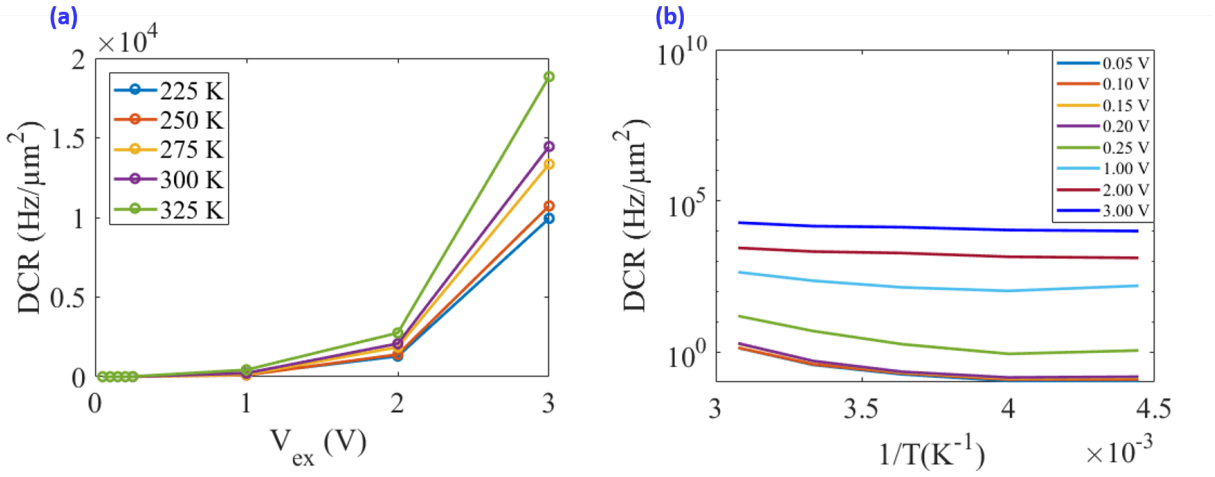

Figure 3.10: *Process original (a) DCR en fonction de la tension d'excès pour différentes températures (b) Plot d'Arrhenius DCR en fonction de l'inverse de la température pour plusieurs tensions d'excès (génération-recombinaison SRH et B2B).*

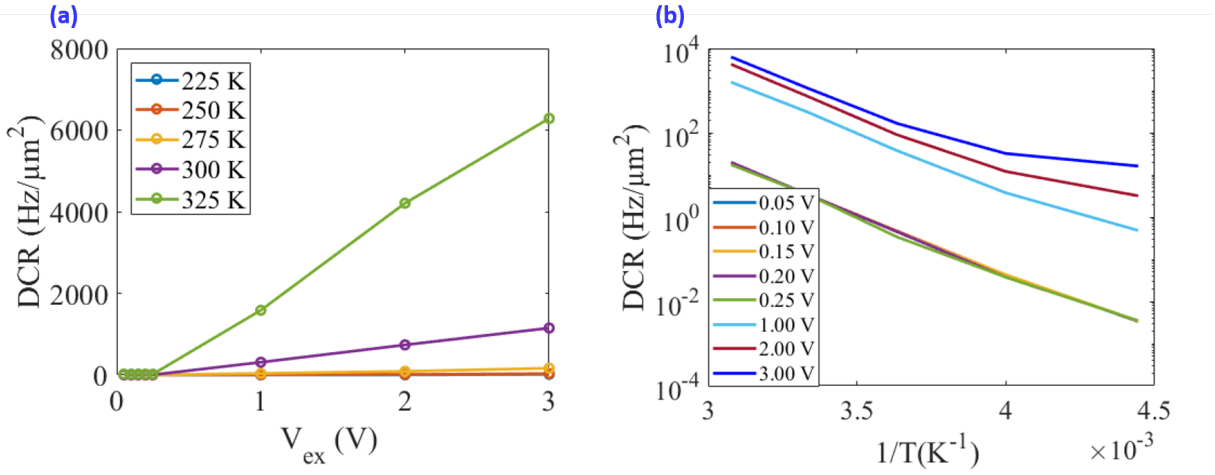

Figure 3.11: *Process modifié - dopage modifié du caisson N profond (a) DCR en fonction de la tension d'excès pour différentes températures (b) Plot d'Arrhenius DCR en fonction de l'inverse de la température pour plusieurs tensions d'excès (génération-recombinaison SRH et B2B).*

avec α_{Si} le coefficient d'absorption fonction de la longueur d'onde.

$$PDP = \int_{x_a}^{x_b} ATP(x) P_{abs}(x) dx \tag{4.52}$$

La Fig. 3.12 représente le PDP estimé en éclairage face avant (FSI- Front Side Illumination) et face arrière (BSI - Back Side Illumination) après amincissement. Cette estimation ne prend pas en compte d'éventuelles réflexions, ni la contribution des porteurs photogénérés dans les zones neutres pouvant atteindre la zone de multiplication

par dérive et/ou diffusion. Néanmoins, nous observons que la SPAD FDSOI, en illumination face arrière, permet d'atteindre le même PDP dans le proche infrarouge qu'avec un éclairage face avant en offrant l'avantage d'un meilleur facteur de remplissage grâce à la structure intrinsèquement 3D.

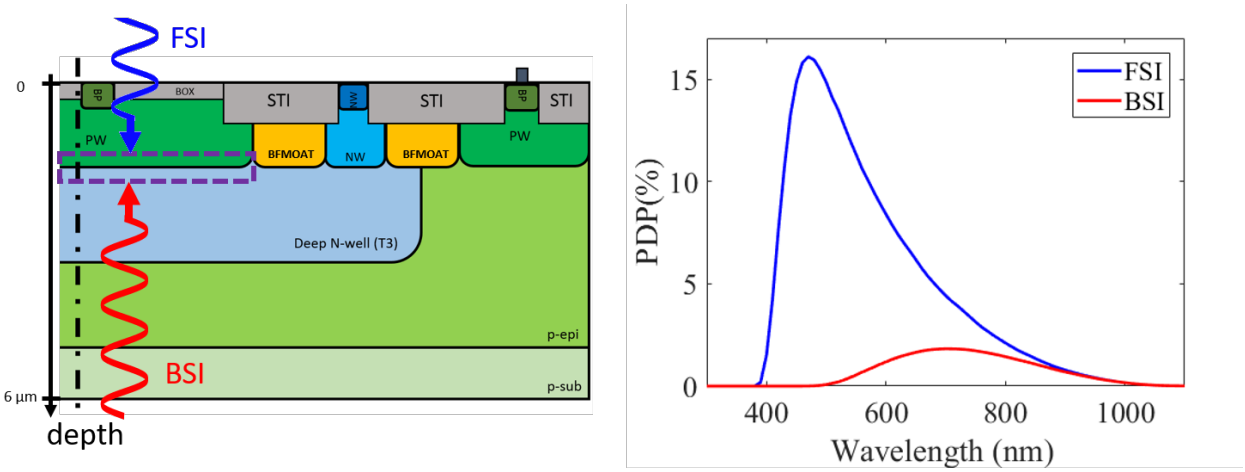

Figure 3.12: *Estimation du PDP pour Vex = 2 V (a) Front Side Illumination; (b) Back Side Illumination. (Épaisseur:* 6 µm*)*

3.5 Conclusion partielle

Nous avons présenté dans cette section la méthodologie de simulation TCAD ainsi que les routines analytiques permettant d'estimer les principales figures de mérite telles que la probabilité d'avalanche (Avalanche Triggering Probability - ATP), le bruit dans l'obscurité (Dark Count Rate - DCR) et la probabilité de détection des photons (Photon Detection Probability - PDP). Les simulations TCAD ont permis d'optimiser la structure SPAD FDSOI, notamment le dopage du caisson N profond pour augmenter la tension de claquage et réduire le courant tunnel et le bruit. Une approche originale est proposée pour simplifier le calcul de la probabilité d'avalanche et elle a été validée par rapport à des simulations rigoureuses. Finalement, le bruit dans l'obscurité (Dark Count Rate - DCR) et la probabilité de détection des photons (Photon Detection Probability - PDP) ont été estimés pour notre structure SPAD FDSOI. Ces estimations sont satisfaisantes avec notre approche simplifiée et idéalisée mais demanderont à être confrontées aux mesures dans la section suivante.

4 Caractérisation des cellules SPAD

Dans cette section, différentes cellules SPAD développées dans la technologie C28FDSOI ont été caractérisées. Les tests décrits ici sont les suivants: courbes I-V, tension de claquage en fonction de la température, réponse électroluminescente et taux de comptage dans l'obscurité. Les cellules pour la détection indirecte des avalanches ont également été caractérisées électriquement en statique et en dynamique. Les résultats sont ensuite discutés et des améliorations sont proposées. Une plaque avec implantation dédiée du caisson N profond a également été partiellement caractérisée.

4.1 Courbes I-V

La courbe I-V en inverse pour les cellules implémentées dans les zones FDSOI et STI est présentée à la Fig. 4.1. La tension de claquage à la température ambiante a été prise à une valeur de courant de 10 µA et est respectivement de 9.50V et 9.35V pour FDSOI et STI. Cette légère différence entre ces valeurs est probablement due aux implants, réalisés à travers différentes couches pour chaque zone, comme expliqué dans la section précédente. Le seul paramètre de dessin qui semble avoir une influence sur ces courbes est la zone d'intégration: les cellules STI ont une tension de claquage inférieure à celle du FDSOI, les autres paramètres susmentionnés ne perturbant pas les résultats.

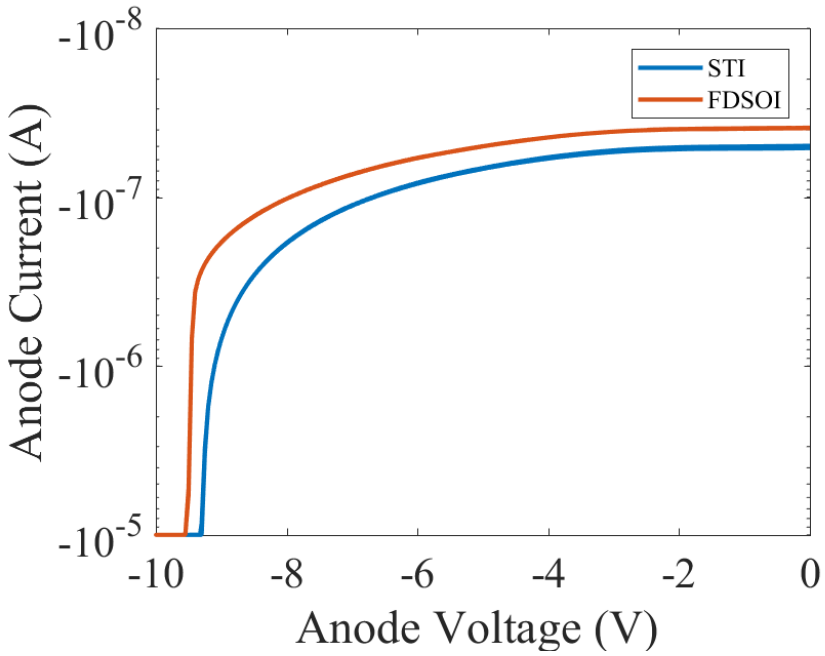

Figure 4.1: *Caractéristique inverse mesurée pour les diodes SPAD octogonales intégrées dans les zones FDSOI et STI (sous éclairage).*

4.2 Courant d'obscurité

Afin de mieux comprendre les phénomènes physiques impliqués dans les SPAD FDSOI, il est possible d'évaluer la variation du courant d'obscurité en fonction de la température. Dans la Fig. 4.2, il est possible d'observer le tracé d'Arrhenius pour le courant d'obscurité. En raison de la petite surface de jonction dans la plupart de nos SPAD, le courant d'obscurité ne peut être mesuré que dans des cellules circulaires de 2460 μm^2. L'énergie d'activation extraite de la pente de la courbe est de 0.21 eV, ce qui signifie qu'elle ne varie pas beaucoup en température. En effet, cette valeur se situe entre le midgap et le zéro, ce qui indique une forte présence d'effets B2B et TAT.

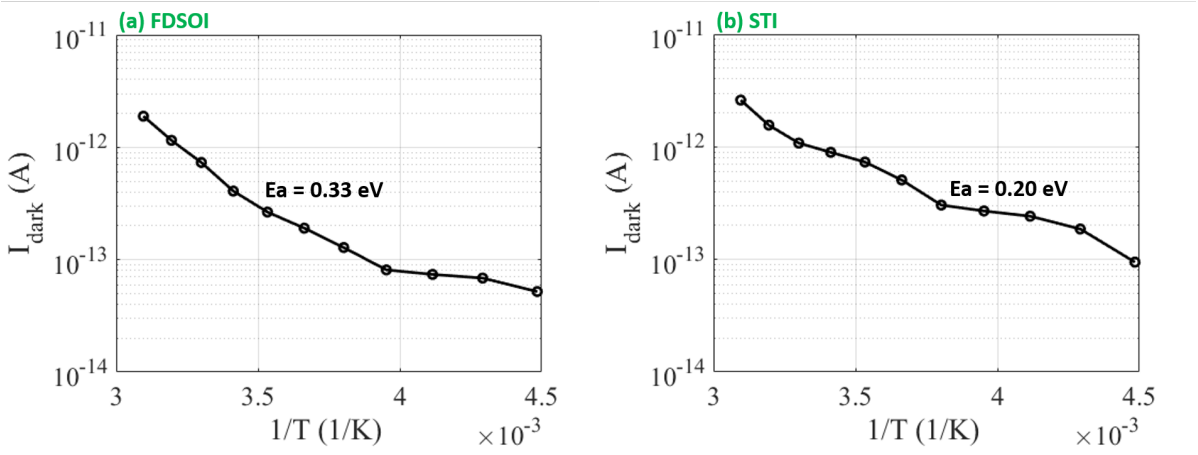

Figure 4.2: *Tracé d'Arrhenius pour le courant d'obscurité pour la cellule STI. La faible pente indique une prédominance des effets de courant tunnel (pur et assisté par pièges).*

4.3 Tension de claquage en fonction de la température

Les tests en température sont généralement utilisés pour distinguer entre la rupture par Zener et les avalanches, car le mécanisme de Zener (basé sur le courant de tunnel bande à bande) a un coefficient de température négatif, alors que la tension de rupture en avalanche augmente avec la température. Afin de réaliser de tels tests, le Keithley 4200 Semiconductor Analyzer a été couplé à une station sous pointes cryogénique où les puces ont été placées, permettant le contrôle précis de la température (dans ce cas, de -50 °C à 50 °C, avec un pas de 10 °C).

Pour les cellules FDSOI et STI octogonales, ces courbes sont présentées à la Fig. 4.3. La signature d'avalanche est vérifiée pour les deux, avec des pentes positives dV_{BD}/dT égales à 6.10 et 5.93 mV K^{-1}, respectivement.

4.4 Réponse électroluminescente

Il est bien connu qu'en polarisant une diode à la tension de claquage (ou à une valeur supérieure), un large spectre (de 350 nm à 1.7 µm) est émis, du fait de la présence de porteurs chauds (électrons et trous à forte énergie cinétique, due à un champ

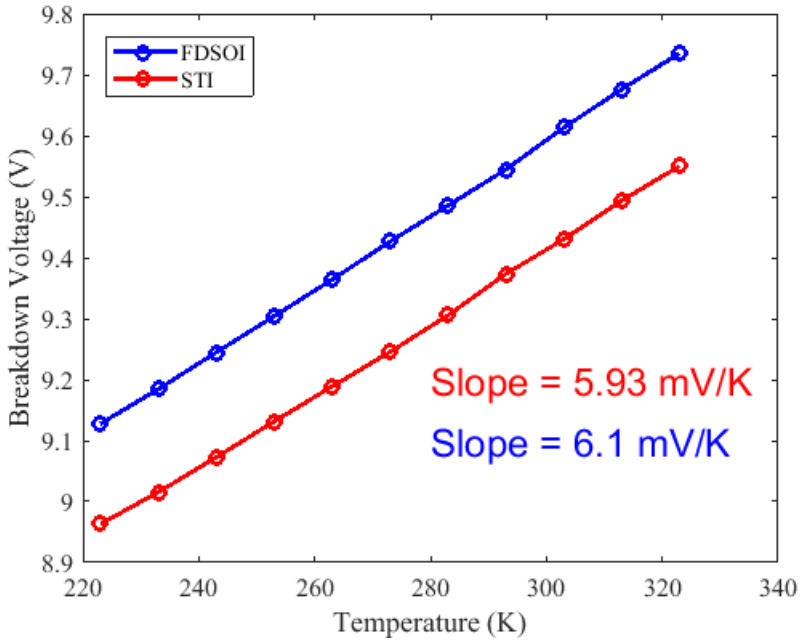

Figure 4.3: *Évolution de la tension de claquage mesurée en fonction de la température, pour les diodes SPAD octogonales intégrées dans les zones FDSOI et STI.*

électrique élevé). Les taches lumineuses observées dans ces situations se produisent lorsque l'avalanche est déclenchée et sont directement liées à l'amplitude du champ électrique, fournissant une microcartographie du champ, et sont donc très utiles pour la détection du claquage prématurée du bord (PEB).

La mesure d'électroluminescence présentée ici consiste à utiliser une source de tension, capable de limiter les valeurs de courant, connectée au circuit imprimé contenant la puce avec des SPADs en cours de test, ainsi qu'une caméra haute sensibilité (Andor Zyla 5.5 sCMOS) couplé à un microscope avec des lentilles grossissantes de x50 et x100. Tous les tests présentés ici ont été réalisés à température ambiante. Tout d'abord, une image de référence est capturée avec la lumière ambiante, alors que la SPAD n'avait pas encore été polarisée. Après cela, l'obscurité est imposée et la caméra est réglée sur un temps d'intégration de 5 s. La diode est alors polarisée en inverse à sa tension de fonctionnement et émet de la lumière. L'image résultante est ensuite acquise par la caméra.

Les résultats des tests d'électroluminescence pour la cellule FDSOI octogonale sont présentés à la Fig. 4.4. La limite de courant a été maintenue constante à 2.5 mA, tandis que la tension appliquée a été augmentée jusqu'à la valeur de tension pour laquelle la cellule est complètement allumée, situation dans laquelle le champ électrique est réparti partout dans la région active. Un claquage prématuré aux bords a pu être observé, malgré l'utilisation d'un anneau de garde BFMOAT. Cela peut s'expliquer par la couche STI qui existe aux frontières, en raison de contraintes de règles de dessin, à travers laquelle les implants sont réalisés. En effet, la jonction PW-DNW est plus abrupte sous STI, ce qui signifie que leur tension de claquage est plus basse. Par conséquent, le processus d'avalanche commence naturellement aux frontières.

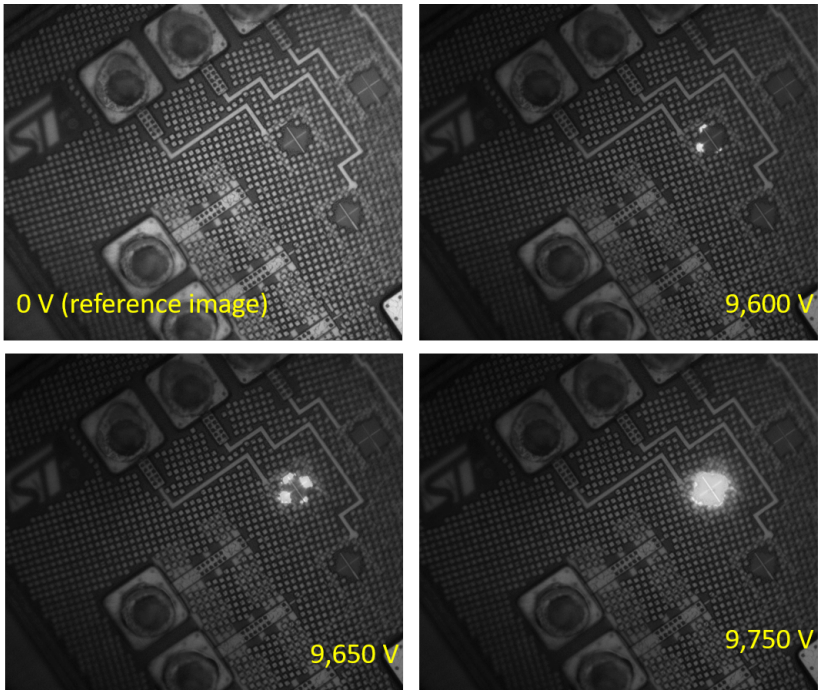

Figure 4.4: *Réponse électroluminescente pour cellule octogonale FDSOI.*

La confirmation de ce phénomène peut être déduite de la Fig. 4.5, où la cellule STI octogonale, complètement intégrée sous une couche uniforme de STI, a été soumise au même protocole de test d'électroluminescence. Aucun effet PEB n'est observé et la jonction se claque à une tension appliquée inférieure, ne nécessitant pas beaucoup de surtension pour un éclairage complet de la cellule.

4.5 Taux de comptage dans l'obscurité - DCR

Le DCR est l'un des FOM les plus importants pour les SPADs. Il représente essentiellement le bruit présenté par le dispositif dans l'obscurité, c'est-à-dire le nombre d'avalanches déclenchées sans photon incident. Ce bruit peut être produit par plusieurs phénomènes physiques qui génèrent des porteurs libres dans la ZCE et qui déclenchent le processus d'avalanche, tels que le B2B, la SRH.

Pour effectuer des mesures DCR, il est nécessaire d'associer un circuit d'étouffement et de recharge à la SPAD afin que le dispositif ne soit pas endommagé et qu'une nouvelle détection puisse être effectuée une fois l'avalanche éteinte. Pour les mesures DCR, un circuit passif (résistance) externe était connecté à l'anode, grâce à une carte électronique dédiée. La cathode était polarisée à une tension constante $V_{BD} + V_{ex}$.

Il était possible de mesurer directement, avec un oscilloscope à large bande, l'augmentation de tension transitoire à travers la résistance, avec un signal en forme de pic correspondant aux événements d'avalanche, comme illustré à la Fig. 4.6. L'extraction statistique du DCR a été réalisée en comptant le nombre d'événements pour une fenêtre temporelle fixe dans laquelle les pics de tension dépassaient un seuil de tension fixe.

En faisant varier la tension d'excès V_{ex} ainsi que la température (de -40 °C à 50

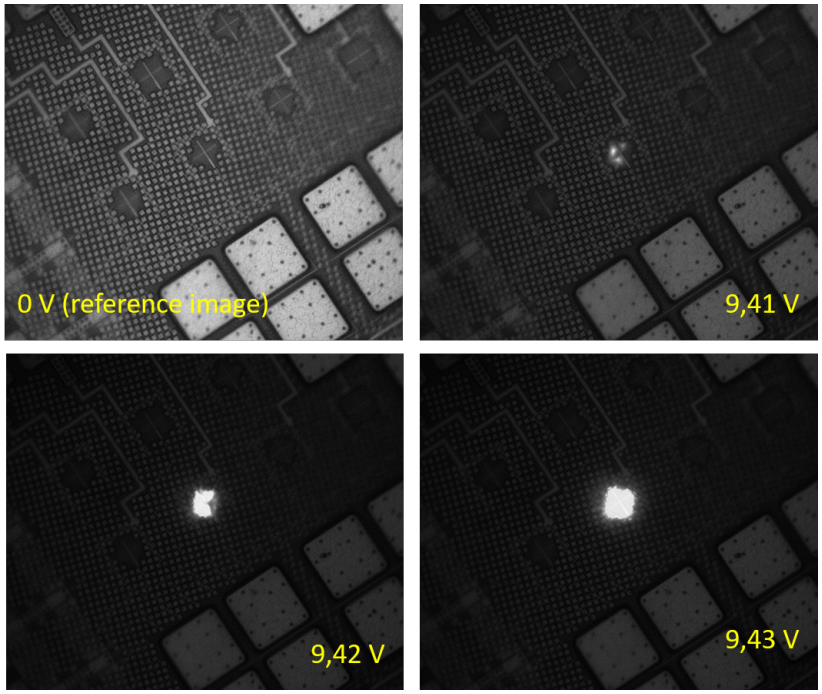

Figure 4.5: *Réponse électroluminescente pour cellule carrée STI.*

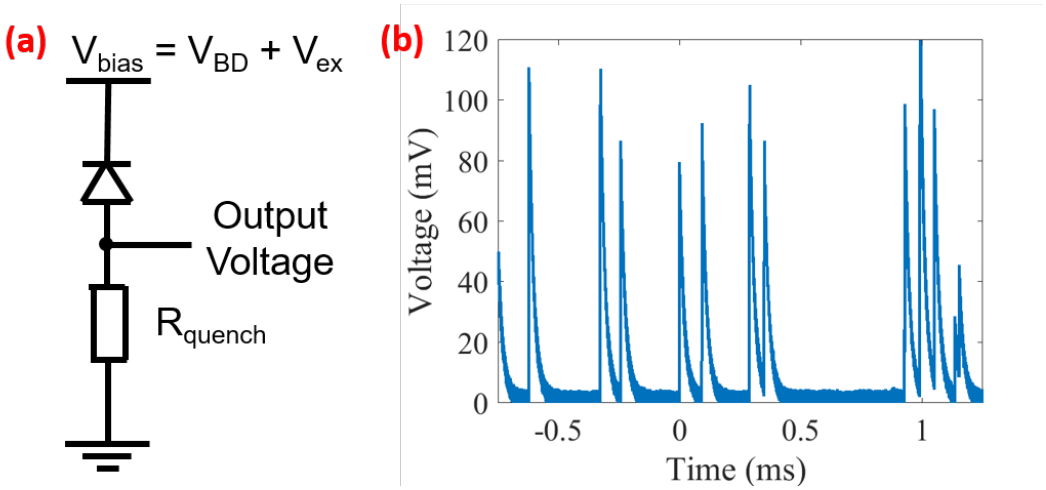

Figure 4.6: *(a) Schéma du circuit utilisé pour les mesures de DCR; (b) Tension de sortie à l'anode, avec l'image du courant qui traverse SPAD. Chaque pointe correspond à un événement d'avalanche.*

°C, avec un pas de 10 °C), grâce à une cage thermique dans laquelle la carte de circuit imprimé a été insérée, le DCR mesuré moyen a été tracé dans les courbes présentées dans la Fig. 4.7, pour les cellules FDSOI et STI octogonales. Une résistance d'étouffement externe de 200 kΩ a été utilisée pour les deux. Pour chaque valeur DCR moyenne, environ 3 000 acquisitions ont été effectuées pour une fenêtre temporelle fixe de 2 ms.

L'évolution du DCR lorsque V_{ex} est augmenté, pour une température fixe, est

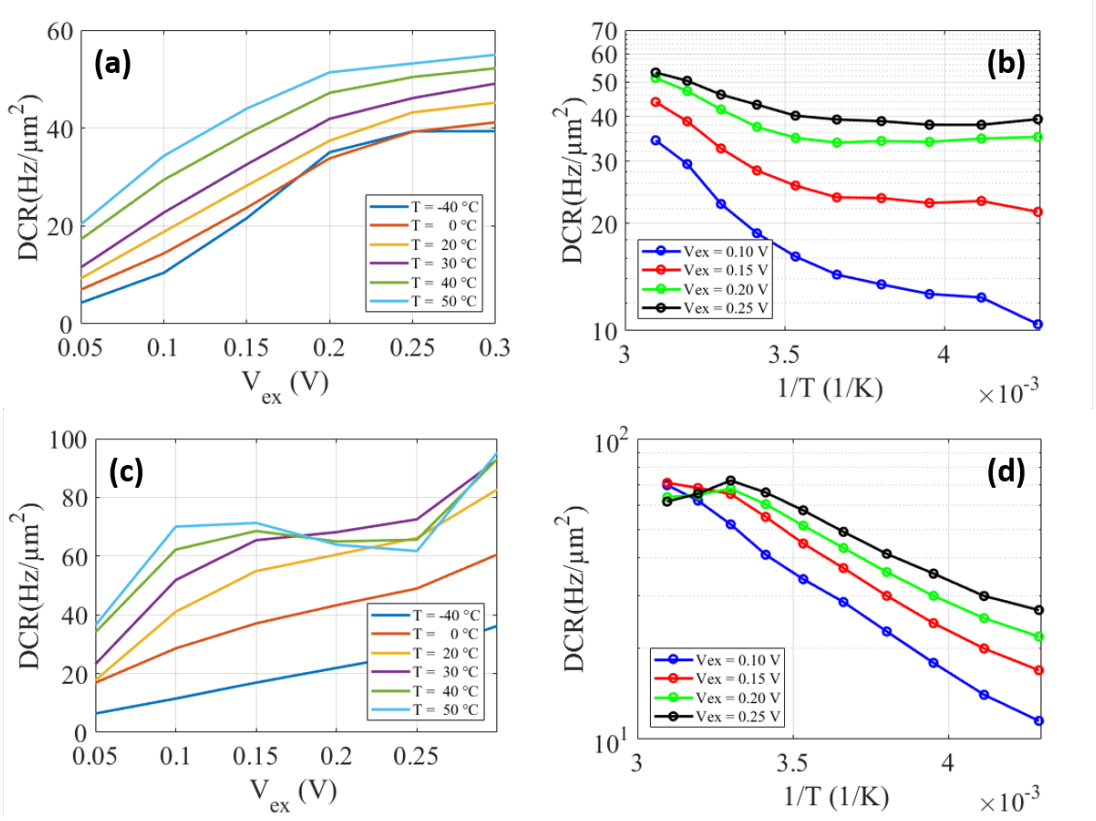

Figure 4.7: *Mesures DCR pour les cellules octogonales: (a) et (b) FDSOI; (c) et (d) cellules STI.*

présentée dans les Fig. 4.7 (a) et (c), respectivement pour FDSOI et STI. Il est possible de noter une évolution linéaire au départ, mais autour de $V_{ex} = 0.25V$, une saturation se produit. Cet effet est dû au circuit d'étouffement externe avec des valeurs de capacité parasite élevées, qui produisent une constante de temps de recharge longue (environ 20 µs) qui ne permet pas d'augmenter l'excès de polarisation au-dessus de 0.3 V, car les événements afterpulsing ne sont plus négligeables.

Le graphique d'Arrhenius à des tension d'excès fixes, pour les deux cellules, peut être observé dans la Fig. 4.7 (b) et (d), respectivement. Les énergies d'activation E_a extraites des pentes de telles courbes sont une indication des principaux phénomènes impliqués dans la structure du SPAD générant une avalanche. Les très faibles valeurs d'énergie d'activation obtenues (environ 0.1 eV dans les courbes présentées) indiquent la prédominance du B2B et TAT, confirmant l'hypothèse élaborée à partir des faibles valeurs de tension de claquage, naturellement présentes pour une jonction abrupte.

Les valeurs du DCR moyen mesuré sont assez élevées pour un excès de tension aussi faible, par rapport aux SPADs de l'état de l'art. Néanmoins, puisqu'il s'agissait d'une toute première intégration de SPAD dans FDSOI et que la technologie d'origine n'était pas du tout conçue pour de tels dispositifs, ces premiers résultats sont prometteurs. Des limitations similaires ont été obtenues dans la technologie bulk CMOS 65 nm.

Il convient également de noter que, en raison des règles de dessin imposées pour la technologie C28DFSOI, la couche de STI est conservée aux frontières de la région active. Les interfaces entre le silicium et la couche d'oxyde de silicium sont bien connues

pour présenter de nombreux défauts profonds dans leurs structures. Dans notre cas, la ZCE est directement en contact avec une STI, ce qui implique de nombreux porteurs libres injectés dans la région de multiplication, ce qui entraîne un très haut DCR. Une solution possible à ce problème serait l'augmentation de la distance entre la couche STI et la ZCE, mais cela nécessiterait de violer les règles de dessin.

Afin de caractériser complètement les SPAD jusqu'à ses limites physiques intrinsèques, un circuit d'étouffement et recharge actif (AQC) est nécessaire car il permet de réduire le nombre de charges passant par la diode. De plus, une recharge active permet de contrôler le temps mort et ainsi de quantifier l'afterpulsing.

4.6 Caisson N profond modifié

A partir des simulations TCAD, nous avons constaté qu'une version modifiée du caisson N profond (DNW), en changeant ses niveaux de dopage natif, peut améliorer les performances du système SPAD, notamment en fournissant une tension de claquage plus élevée, une jonction plus lisse, et, par conséquent, des taux de génération B2B et TAT plus faibles et un DCR plus faible. Avec l'accord de STMicroelectronics, une plaquette dédiée a été soumise à l'implant DNW modifié proposé dans la section précédente. Certains résultats prometteurs pourraient être mesurés, comme indiqué dans les sous-sections suivantes.

Courbes I-V

Certains résultats prometteurs ont été mesurés, tels que le courant d'obscurité, présenté à la Fig. 4.8. À partir des courbes, deux régions différentes peuvent être identifiées pour la cellule FDSOI: basse température, où E_a est presque nulle ; et haute, avec $E_a = 0.52eV$, représentant le mécanisme SRH.

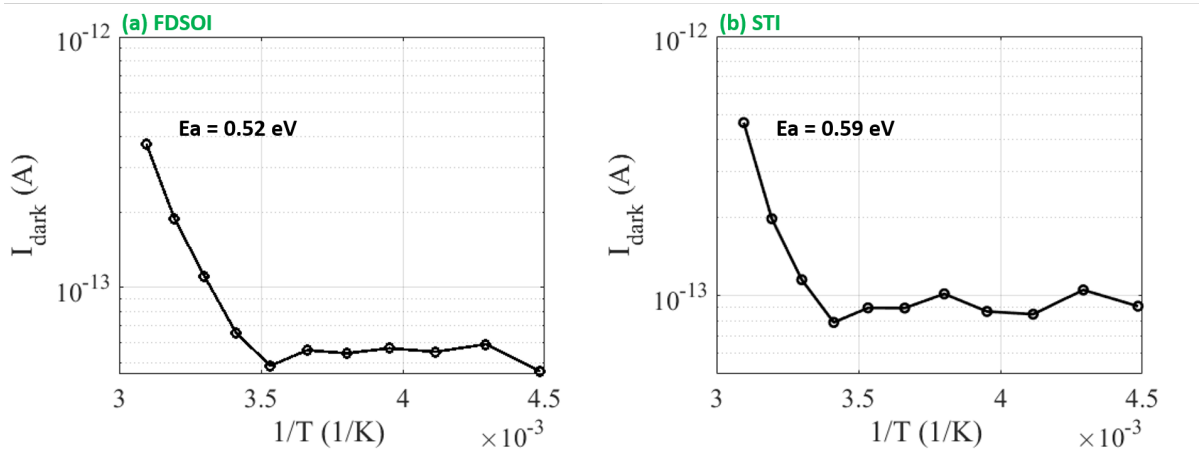

Figure 4.8: *Tracé de Arrhenius pour le courant d'obscurité pour (a) des cellules FDSOI et (b) des cellules STI (les deux avec DNW modifié).*

Pour les cellules STI, les régions sont légèrement différentes: basse température, présentant une énergie d'activation E_a presque nulle; une température moyenne, où

E_a vaut 0.76 eV; et une température élevée, où E_a est égal à 1.1 eV. Les régions STI étant légèrement plus dopées que le FDSOI, il est normal que les premières soient plus sensibles aux effets de la température que les dernières.

Pour les deux cellules, ces résultats représentent une grande différence par rapport au SPAD d'origine, dans lequel seule une combinaison de B2B et de TAT pouvait être observée. Les résultats expérimentaux confirment ensuite le modèle de simulation TCAD pour ces mesures.

Tension de claquage en fonction de la température

La tension de claquage en fonction de la température de ces nouveaux dispositifs est présentée à la figure 4.9. Comme on peut le constater, la tension de claquage a augmenté d'environ 6.5 V par rapport à la technologie originale, comme nous avons prédit avec les simulations TCAD. À la température ambiante, VBD = 15.92 V.

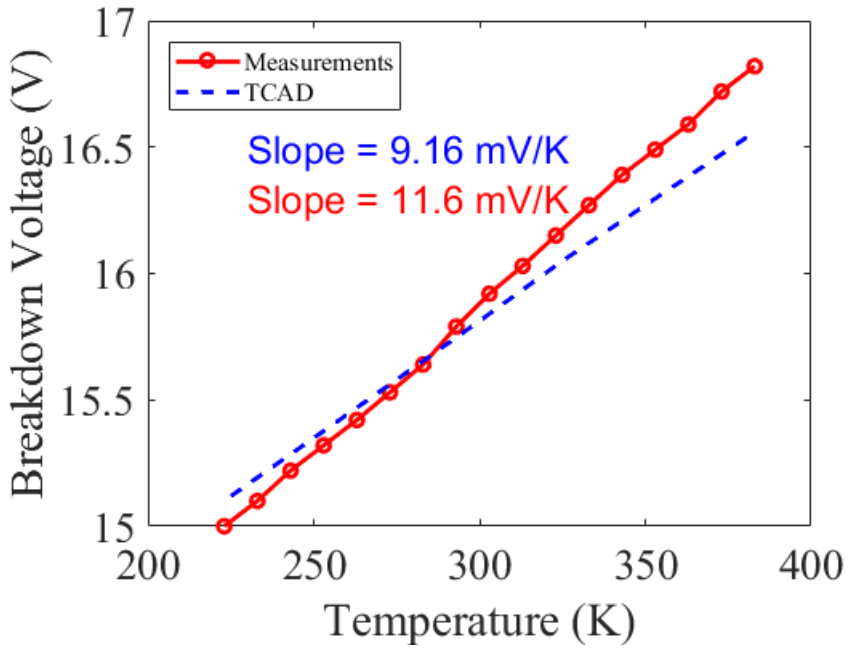

Figure 4.9: *Tension de claquage en fonction de la température pour SPAD avec implants modifiés. L'augmentation prévue dans la simulation TCAD a été confirmée par les résultats des mesures.*

4.7 Circuit de détection indirecte d'avalanche en FDSOI

Un diviseur résistif a été implémenté (Fig. 4.10 et 4.11) sur la SPAD dans une zone FDSOI (sur BOX) à la fois pour la caractérisation en statique avec station sous pointes et pour l'analyse dynamique.

La tension d'anode varie de 0 (état de veille) à une valeur maximale d'environ V_{ex} (en cas d'avalanche). Comme le suiveur CMOS ne peut tolérer une tension d'entrée supérieure à V_{dd} (par exemple 1.8V), la plage de tension en excès Vex est également

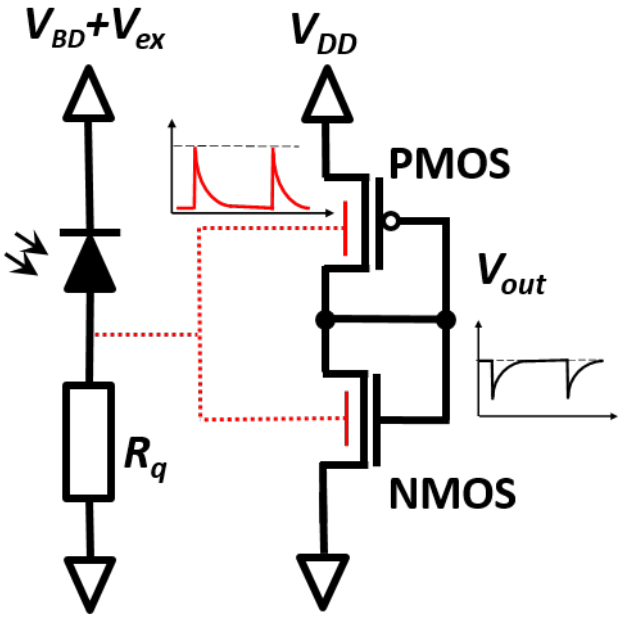

Figure 4.10: *Schéma du circuit de détection, composé d'un RVT NMOS et d'un LVT PMOS, dans une configuration de division de tension, où la tension de sortie varie en fonction des avalanches, grâce à l'effet de polarisation du substrat (body biasing).*

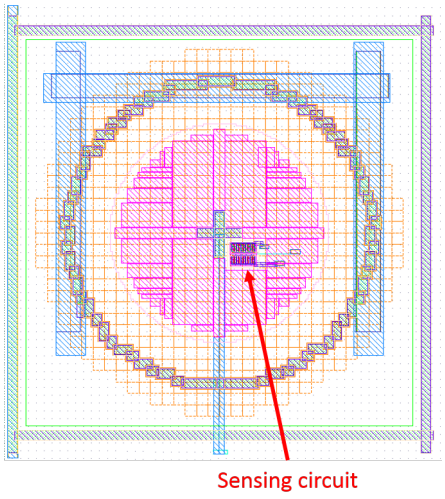

Figure 4.11: *Layout de la SPAD circulaire avec le circuit de détection indirecte de l'avalanche sur la couche PW, au milieu.*

limitée à V_{dd} (limitant ainsi le PDE), sauf si des transistors cascode sont utilisés. Avec cette fonction de détection indirecte, il n'est plus nécessaire de connecter physiquement le circuit de détection d'avalanche à l'anode SPAD. De plus, la plage de surtension n'est plus limitée à V_{dd}.

Pour les caractéristiques statiques, la variation du courant de drain ainsi que la tension de sortie ont été tracées selon V_{dd} pour le circuit mis en oeuvre avec un oxyde

de grille épais, comme indiqué sur la figure 4.12. Les résultats de la simulation sont obtenus avec le simulateur SPECTRE. La différence entre les résultats de la simulation et ceux des mesures, en particulier pour les V_{dd} inférieurs à 0.5V, s'explique facilement par le très faible flux de courant, qui ne permet pas au diviseur de fonctionner correctement pour de telles valeurs de tension appliquée. La tension de polarisation de la grille arrière a été maintenue à zéro pour cette caractérisation initiale.

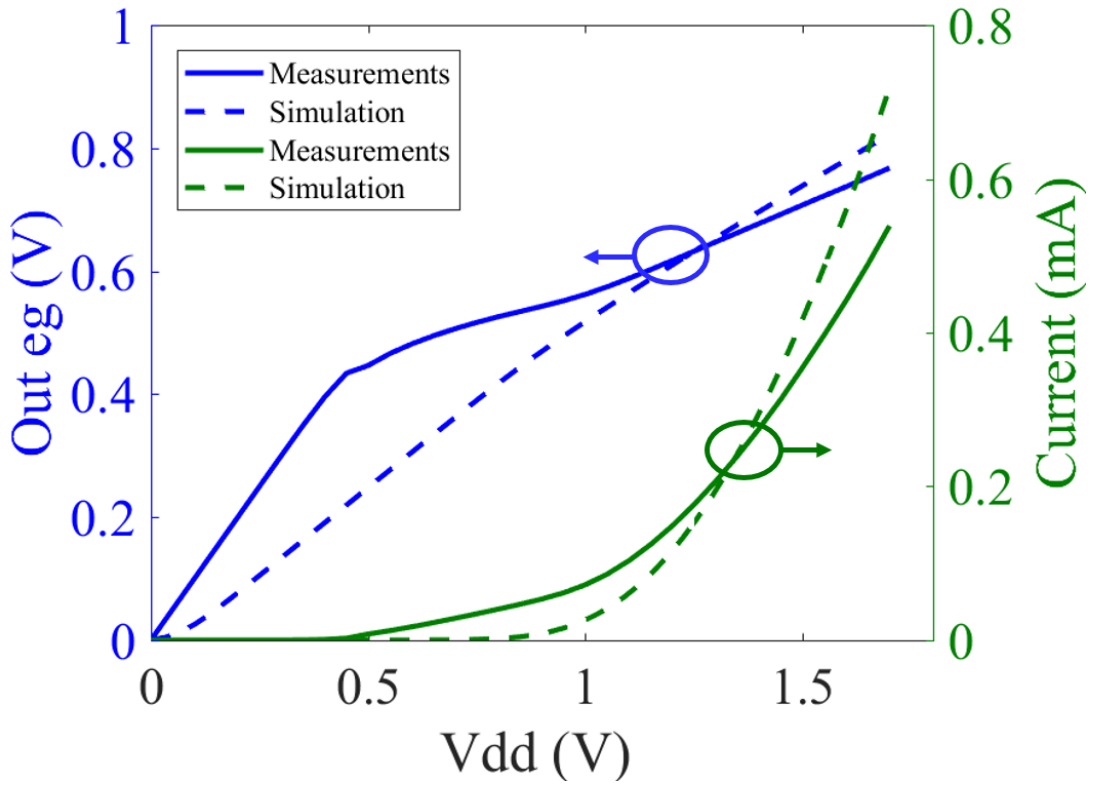

Figure 4.12: *Caractérisation statique d'une cellule de détection insirecte avec des transistors du type EG, à* $V_{bb} = 0$ V.

Le circuit de détection a également été caractérisé pendant le fonctionnement de la SPAD, comme indiqué à la Fig. 4.13, en mesurant simultanément la tension de l'anode et la sortie du circuit de détection indirecte pour plusieurs avalanches (ici, les avalanches correspondent à des événements dans l'obscurité). La détection indirecte proposée permet d'identifier les avalanches à des tensions de polarisation excessives aussi basses que V_{ex} autour de 0.2 V.

4.8 Conclusions partielles

Les SPAD conçues dans la technologie C28FDSOI ont été caractérisés et les résultats correspondants sont montrés et discutés dans cette section. Les courbes I-V ont montré que la jonction PN native composée de PW et de DNW présente une très faible tension de claquage par rapport aux composants de l'état de l'art. Ceci est une indication des niveaux de dopage élevés des caissons, ce qui se traduit par une jonction très abrupte,

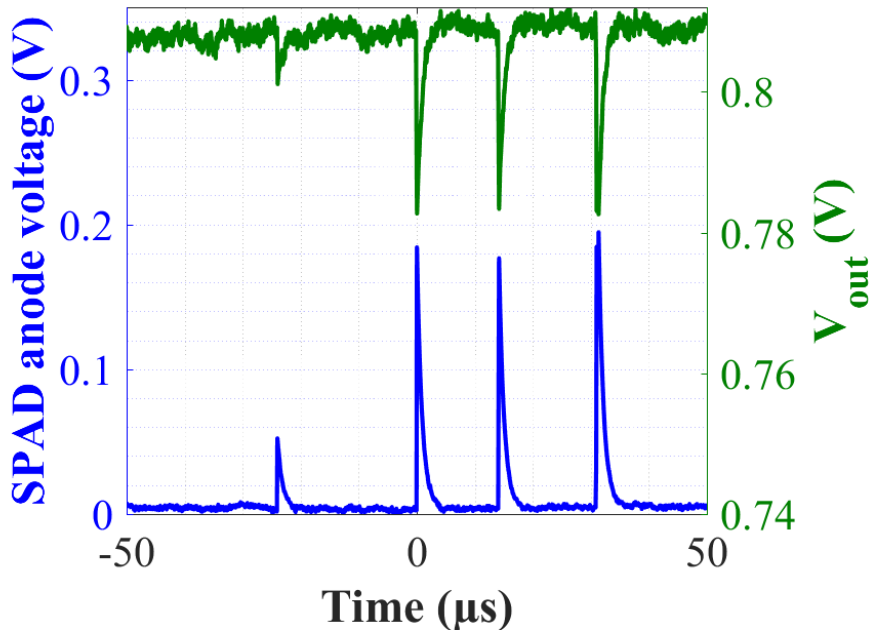

Figure 4.13: *Caractérisation dynamique de la cellule de détection indirecte avec des transistors type EG. Chaque pic correspond à un événement d'avalanche. La détection indirecte d'avalanche grâce à l'effet body biasing est ici validée.*

avec de grands taux de génération B2B et TAT. Les tests d'électroluminescence ont montré la différence entre les implants pour les régions FDSOI et STI, ces derniers étant plus dopés. En raison de contraintes liées aux règles de conception, STI était présent aux limites de la structure FDSOI, ce qui impliquait un claquage prématuré sur le bord. La caractérisation du DCR s'est avérée plutôt difficile car le taux de génération bande à bande élevé, qui affecte ses performances (produisant un dispositif plutôt bruyant) et aussi à cause de la grande quantité de charges injectées dans la ZCE par l'interface avec l'oxyde du STI. Cependant, il était encore possible d'effectuer des mesures DCR pour de faibles tensions d'excès jusqu'à 0.3 V. Une plaque avec implantation N profond dédiée a été réalisée, avec une tension de claquage plus élevée, mais toujours trop bruyante à cause du STI. Les circuits de détection indirecte d'avalanche ont été validés expérimentalement.

Conclusions générales

Ce travail de recherche s'est focalisé sur la conception, la simulation, la modélisation et la caractérisation des diodes à avalanche à photon unique (Single Photon Avalanche Diode (SPAD)) dans une technologie CMOS Fully Depleted Silicon On Insulator (FDSOI) avancée (28 nm).

Nous avons présenté dans un premier temps le mode de fonctionnement de ce type de dispositif, ainsi que l'état de l'art actuel, où les meilleurs compromis entre la photodétection et le facteur de remplissage sont obtenus avec des techniques d'intégration 3D assez compliquées et chères, avec l'assemblage de deux plaquettes de silicium. Nous proposons ensuite une nouvelle approche, avec l'intégration de SPAD dans une technologie CMOS Fully Depleted Silicon On Insulator (FDSOI) avancée (28 nm). Dans ce cas, grâce à la couche d'oxyde enterrée (Buried Oxide (BOX)), la jonction PN est isolée des transistors, augmentant le facteur de remplissage du circuit total dans une approche monolithique et intrinsèquement 3D.

Ensuite, la conception de telles cellules SPAD est proposée. Notre SPAD est constitué des couches PW et DNW, sous le BOX. Plusieurs variantes ont été fabriquées, afin de vérifier l'influence de chaque paramètre de dessin (géométrie, distance de garde, zone d'intégration) sur les performances du dispositif. Dans un premier temps, aucune règle de dessin n'a été modifiée, ce qui imposait des contraintes telles que les formes orthogonales obligatoires, non adaptées pour éviter le claquage prématuré sur le bord (Premature Edge Breakdown (PEB)). Des cellules de détection indirecte des avalanches ont également été proposées, sur la base du couplage capacitif par la polarisation du substrat en C28FDSOI. Cette implémentation ouvre la voie à une électronique de traitement SPAD plus simple et innovante.

La simulation TCAD des structures proposées a été également adressée, permettant d'estimer les principales figures de mérite telles que la probabilité d'avalanche (Avalanche Triggering Probability - ATP), le bruit dans l'obscurité (Dark Count Rate - DCR) et la probabilité de détection des photons (Photon Detection Probability - PDP). Une optimisation des profils de dopage a été présentée, ce qui entraîne une réduction de taux de génération de porteurs dûs au courant tunnel (Band To Band Tunneling (B2B)), et une augmentation de la tension de claquage. Une approche originale est proposée pour simplifier le calcul de la probabilité d'avalanche et elle a été validée par rapport à des simulations rigoureuses.

Nous avons caractérisé les composants fabriqués avec plusieurs tests. Les courbes I-V ont montré que la jonction PN native composée de PW et de DNW présente une très faible tension de claquage par rapport aux composants à l'état de l'art, car notre jonction a des niveaux de dopage élevés. Les tests d'électroluminescence ont montré la différence entre les implants pour les régions FDSOI et STI, ces derniers étant plus dopés. Les mesures du taux de comptage dans l'obscurité n'a été possible que pour de faibles valeurs de tension d'excès (jusqu'à 0.3 V), à cause de la grande quantité de charges injectées dans la ZCE par l'interface avec l'oxyde du STI. Les circuits de détection indirecte d'avalanche ont été validés expérimentalement.

Malgré les principales contraintes rencontrées lors de la caractérisation, les dispositifs implémentés se sont révélés capables de fonctionner en mode Geiger, même en technologie native. Bien que les résultats actuels ne soient pas vraiment comparables

aux SPADs de l'état de l'art, ils constituent une preuve de concept de l'utilisation de la technologie FDSOI pour la mise en œuvre de dispositifs SPAD, ce qui présente un grand intérêt en tant que solution de remplacement pour les techniques 3D compliquées et coûteuses.

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FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : **CHAVES DE ALBUQUERQUE** DATE de SOUTENANCE : **12/11/2019**

Prénoms : Tulio

TITRE : **Integration of Single Photon Avalanche Diodes in Fully Depleted Silicon-on-Insulator Technology**

NATURE : Doctorat Numéro d'ordre : **2019LYSEI091**

Ecole doctorale : EEA (Électronique, Électrotechnique et Automatique)

Spécialité : Electronique, micro et nanoélectronique, optique et laser

RESUME :
Ce travail a pour objectif la conception, la simulation, la modélisation et la caractérisation électrique de diodes à avalanche à photon unique (Single Photon Avalanche Diodes - SPAD) dans une technologie CMOS Fully Depleted Silicon on Insulator - FDSOI. Les SPAD sont des jonctions PN polarisées en inverse au-delà de la tension de claquage, fonctionnant dans le mode Geiger. Une telle implémentation devrait fournir une intégration monolithique intrinsèque de ces dispositifs, ainsi que de leurs composants électroniques associés obligatoires, grâce à la couche d'oxyde enterrée présente dans cette technologie, optimisant ainsi le facteur de remplissage. Grace à sa haute sensibilité, les SPAD sont utiles pour plusieurs applications, telles que les mesures de temps de vol (Time of Flight - ToF) et de (Fluorescence Lifetime Imaging Microscopy - FLIM), ainsi que la détection de particules chargées, dans le domaine de la physique de haute énergie. Les cellules conçues respectent les principales règles de dessin imposées par la fonderie et présentent des variations d'aspect telles que zone d'intégration, géométrie, distance de garde et circuit d'étouffement. Des simulations TCAD ont été effectuées afin d'estimer certaines des principales figures du mérite de SPAD. Plusieurs modèles de génération d'avalanche et de porteurs ont été étudiés pour une meilleure adaptation du modèle simulé aux dispositifs fabriqués. Des caractérisations électriques ont été réalisées pour estimer des paramètres importants tels que la tension de claquage, le taux de comptage dans l'obscurité (DCR) et la réponse à l'électroluminescence. Bien que les résultats obtenus restent inférieurs par rapport à l'état de l'art, leur faisabilité a été démontrée et peut être utilisée comme preuve de concept, en même temps que des améliorations sont proposées.

MOTS-CLÉS : single photon avalanche diode (SPAD), CMOS, UTBB FDSOI, body-biasing.

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