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Diamond Schottky diodes improvement to pave the way to high power electronic application

Juliette Letellier

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Communauté UNIVERSITÉ Grenoble Alpes

THÈSE

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Spécialité : **NANO ELECTRONIQUE ET NANO TECHNOLOGIES**

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Co-encadrée par **David EON, Université Grenoble Alpes**,

préparée au sein du **Laboratoire Institut Néel**
dans **l'École Doctorale Electronique, Electrotechnique, Automatique, Traitement du Signal (EEATS)**

Diodes Schottky en diamant un nouveau pas vers les applications pour l'électronique de puissance

Diamond Schottky diodes improvement to pave the way to high power electronic applications

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Doctoral Thesis

Diamond Schottky diodes improvement to pave the way to high power electronic applications

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Physical Constants

All relatives values are given for diamond

Light velocity	$c = 2.99 * 10^8 m.s^{-1}$
Vacuum permittivity	$\epsilon_0 = 8.85 * 10^{-12}\ F.m^{-1}$
Elementary charge	$\mathrm{q} = 1.6 * 10^{-19} C$
Boltzmann constant	$k_B = 1.38 * 10^{-23}\ m^2.kg.s^{-2}.K^{-1}$
Planck constant	$\mathrm{h} = 6.62 * 10^{-34}\ m^2.kg.s$
Free electron effective mass	$m_0 = \mathrm{kg}$
Band gap	$E_g = 5.45$ eV
Relative permittivity	$\epsilon_r = 5.5$
Saturation drift velocity	$v_s = 1.1 * 10^7 cm.s^{-1}$ (holes)
Thermal conductivity	$\lambda = 22\ W.cm^{-1}.K^{-1}$
Effective Richardson constant	$A^* = 92\ A.cm^{-2}.K^{-2}$
Breakdown field	$E_B = V.cm^{-1}$
Hole mobility	$\mu_p = cm^2.V^{-1}.s^{-1}$
Schottky barrier height	$\phi_b = \mathrm{eV}$

Introduction

Nowadays, one of the biggest problematic the world has to face on is the global warming. Since the 2015 United Nations Climate Change Conference (COP21) Paris' agreement, it has been stated that the global temperature increase should be limited at less than 2 °C and even 1.5°C with 0 emission between 2030 and 2050[1]. At the same time the European Union (EU) promises to reduce the greenhouse gases from at least 40%. The problem is that the energy world demand is still increasing with the increasing population and the new ways of life leading to a raise of greenhouse emission going against these recommendations. One of the first source of greenhouse emission comes from the fossil fuel.

For both initiatives to occur the use of alternative energies has to be increased and energies have to be saved. To do so, the electric grid has to evolve to let current coming from renewable energy sources (solar panels, wind turbines,...) to reach the consumer. It is called a *Smartgrid* (fig. 1). New ways of transportation such as electrical car need to be reload, this new way of living has to be integrated directly on the new electrical grid.

FIGURE 1: *Schematic of the future electrical grid, the Smartgrid (source: http://solutions.3m.com)*

For this new electrical grid power devices components are needed. Those components have to be more efficient, i.e power losses have to be reduced. The current components are mostly silicon based but some limitations are reached due to its own intrinsic properties such as it low breakdown voltage and its need to low temperature working conditions. To overpass those limitations new materials are under investigation: wide band gap semiconductors with Silicon carbide (SiC), Gallium Nitride (GaN), Gallium Oxide (Ga_2O_3) and Diamond. Those materials present some interesting electronic properties (breakdown voltage, electron or hole mobility, ...) to overcome silicon limitation. From this list some materials are more advanced than others, SiC and GaN are already commercialized and start to be

[1] https://www.ipcc.ch/sr15/

implemented into electronic circuits even if still under investigation. Ga_2O_3 and Diamond are still under laboratory investigation all over the world (USA, Japan, China, France, etc..).

Today, the most advanced component in the diamond community is the Schottky diode but several drawbacks are still existing and need to be solved, to reach diamond full potential.

France with the CNRS and the National Research Agency (ANR) is one of the world leader in diamond power electronic devices with different founded projects . This thesis addresses two of this projects.

The first one, the Diamond-HVDC project. Its goal is to provide diamond Schottky diodes with an high breakdown voltage and the highest ON state current as possible. At the end of the project the idea is to integrate those diodes inside a commutation cell and test its reliability. In collaboration with Laplace laboratory in Toulouse, SATIE in Versailles and the Grenoble Electrical Engineering Laboratory (G2Elab) I have been working on the diamond Schottky diodes fabrication in order to improve the electrical characteristics and finally do the preliminary characterizations.

The second one is the Diamwafel project which is founded to provide heteroepitaxialy grown diamond suitable for electronic power device. This project is a collaboration between CEA List, Institut des nanosciences from Lyon, Groupement de la matière condensée (GEMAC) in Versailles, the Laboratoire des sciences des procédés et des materiaux (LSPM) and Institut Néel. My role in this project was to fabricate and characterize diodes made with this new materials.

The goal for both projects is to create the diamond power electronics of tomorrow with two different approaches. The first one by improving what already exists by working on the architecture for example. And the second one by working on a new type of diamond substrate that can help to solve one of the biggest issue of the diamond community: the substrate size by providing big size wafer. But this new material has to be investigated and tested with component already known on the usual diamond material. Working on both project is a good opportunity to combine knowledges coming from electrical engineering perspective with Diamond-HVDC and from material science perspective with Diamwafel and to see the full picture with all problems related.

This manuscript is composed of 6 chapters going from fabrication to electrical characterization of diamond Schottky diodes. At the beginning, in chapter 1 a simplest comparison between diamond and some of this competitors will be done. After a quick review on what have been already developed in the diamond power device community and finally theoretical keys about Schottky diode will be given.

In chapter 2, diamond Schottky diodes fabrication process will be shown. This fabrication process has some keys steps (growth, clean room fabrication) in order to obtain efficient diodes. Each step need to be improved in order to have better diode. In a first part diamond growth will be explained with an highlight on the improvements made to increase

the layer quality and thickness. At the same time new growth techniques will be presented. In this chapter the second part will be focused on the clean room fabrication steps to obtain proper Schottky diode and some difficulties linked to it will be presented and solutions will be given.

Chapter 3, will mainly focus on on finding a technique to increase the ON-state current by designing a new component taking into account previous work revelling some common anode problem by using parallelization process. At the end of the chapter a simple full diamond power rectifier will be presented.

Chapter 4, will focus on Schottky diode OFF-state. Diode OFF-state with its breakdown voltage is one of the key parameter and currently the diamond full potential is not reach. In this chapter it will be presented the characterization of the three different solutions proposed in chapter 2 in order to increase the breakdown voltage of diamond components. For each solution samples will be presented with its characteristics and see if it is a good solution or not.

In chapter 5, a diamond Schottky diode transverse study will be presented. With this, the electric field will be under investigation into the depth of the material thank to electron beam induced current technique. The influence of an electron beam on the Schottky diode reverse characteristics. At the same time cathodoluminescence will be performed to do material characterization. At the end both techniques will be combine in order to have a global view.

Finally in the last chapter I will present the first diode fabricated on an heteroepitaxial substrate fully fabricated in France. As say above this material have to be tested with simple component like lateral Schottky diode. Those diodes will also be electrically characterized and electron beam induced current measurement will also be performed. All of this measurement will give us information on the suitability of this materials to be a real alternative for future diamond power electronics device.

Chapter 1

State of the art & theoretical background

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In this first chapter, wide band gap power device will be introduced. For that some concepts about semiconductor physics will be presented. A comparison between each material available will be done to see which is the best candidate to create new kind of power devices. At the end the focus will be put on Schottky diode which is the heart of this thesis.

1.1 Introduction

Electronic power devices are present all around us. They are used to convert high power energy from the energy sources to a lower power energy. On figure 1.1 from Kimoto *et al.* [1] are summarized all power devices different categories. Each of them will have different characteristics. In this first section different materials used for power device will be compared. During all this thesis the focus will be mostly done on the high voltage group and on the best material for such kind of component.

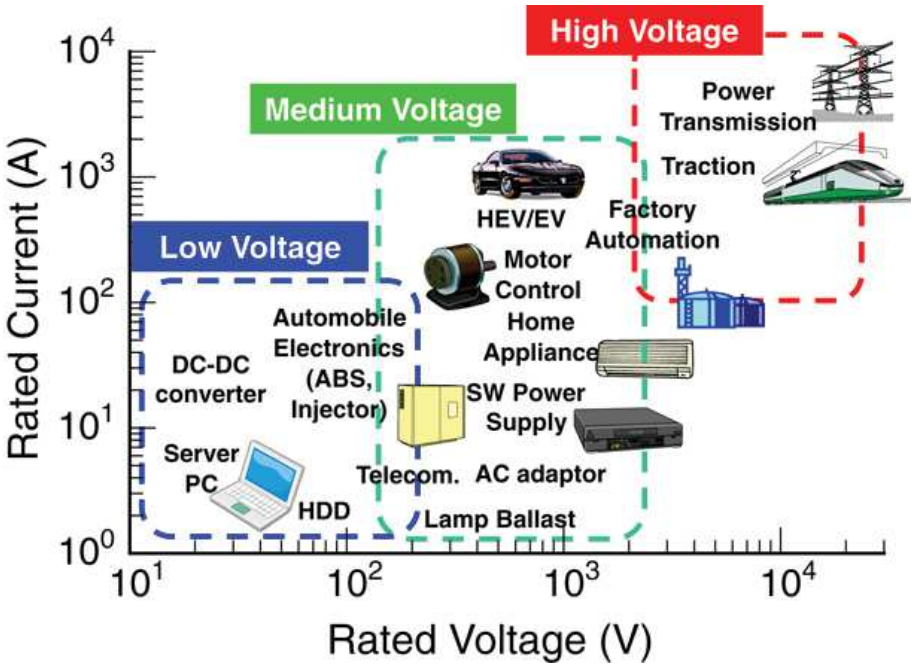

FIGURE 1.1: *Different applications for electronics power device [1]*

1.1.1 Wide band gap semiconductor materials

1.1.1.1 General comparison

Nowadays, silicon (Si) is still the most used material in the power devices community, this is due to its low production cost of big size wafer (300 mm of diameter at 150$/per wafer) as well as the fabrication process maturation to obtain reproducible working devices. But some physical limitations appear over time and new candidates have to be proposed. To compare them with each other material, some figure of merits (FOM) have been developed over the years. Three of them are commonly used and listed below.

- **Baliga's figure of merit** (BFOM): which define the material efficiency to decrease the conduction losses. [2]

$$BFOM = \epsilon_0.\epsilon_r.E_B^3 \tag{1.1}$$

- **Johnson's figure of merit** (JFOM): which define the material ability to be used for high frequency and high power application. [3]

$$JFOM = \left(\frac{E_B.v_s}{2\pi}\right)^2 \tag{1.2}$$

- **Keys' figure of merit** (KFOM): which displays the material thermal limitation to the switching behavior at high frequency the device. [4]

$$KFOM = \lambda.\left(\frac{c.v_s}{2\pi.\epsilon_0.\epsilon_r}\right)^{1/2} \tag{1.3}$$

In those equations c, ϵ_0, ϵ_r, E_B, v_s and λ are respectively the light velocity, the vacuum permittivity, the relative permittivity, the the material critical electric field, the majority carriers saturation velocity and finally the thermal velocity.

From table 1.1, are presented the physical properties of Silicon (Si), Silicon carbide (4H-SiC), Gallium nitride (GaN), Gallium oxide (Ga_2O_3) and Diamond (C). Out of the list of candidates diamond shows the best features: it has the largest: band gap (5.45eV), carrier mobility, breakdown field (more than 10 times than Si). Concerning FOM diamond has the highest value for BFOM and KFOM. Focusing on Baliga's FOM diamond is the best to be used for high power application.

TABLE 1.1: *Summary of different physical properties and FOM at Room Temperature for Si, 4H-SiC, GaN, Ga_2O_3 and diamond.*

Physical properties	**Si**	**4H-SiC**	**GaN**	**Ga_2O_3**	**Diamond**
Band gap (E_g eV)	1.1	3.23	3.45	4.85	5.45
Dielectric constant (ϵ)	11.8	9.8	9	10	5.5
Breakdown field (E_B MV/cm)	0.3	2	3	8	10
Thermal conductivity (λ $(W/cm.K)$)	1.5	5	1.5	0.1	22
Sat. velocity e^- (v_s $(10^7 cm/s)$)	1	2	2.2	1.8	2.7
Sat. velocity h^+ (v_s $(10^7 cm/s)$)	1	-	-	-	1.1
Electron mobility ($\mu_n(cm^2/V.s)$)	1500	1000	1250	300	1000
Holes mobility ($\mu_p(cm^2/V.s)$)	480	100	200	-	2000
Baliga's FOM	1	165	635	3214	23017
Johnson's FOM (10^{23} $\Omega W.s^{-2}$)	2	405	1103	5252	3064
Keyes' FOM ($10^7 W/K.s$)	9	49	16	0.0092	215

1.1.1.2 Different materials diodes comparison

An other way to compare each material is to look at an ideal unipolar device such as 1kV diode on a 1cm^2 substrate. A p-type unipolar device under different conditions is shown on figure 1.2. When a positive bias is applied on the ohmic contact which acts as the cathode the holes can flow from one side to the other, this is called the ON state. On the contrary when a reverse bias is applied the device is on the OFF state. No current is flowing and the depletion region, which is present at 0V just below the Schottky contact (anode) to obtain the device thermal equilibrium. Depletion region will increase with the reverse bias and will go up until reaching the p++ layer. At that point the punch through condition is reached.

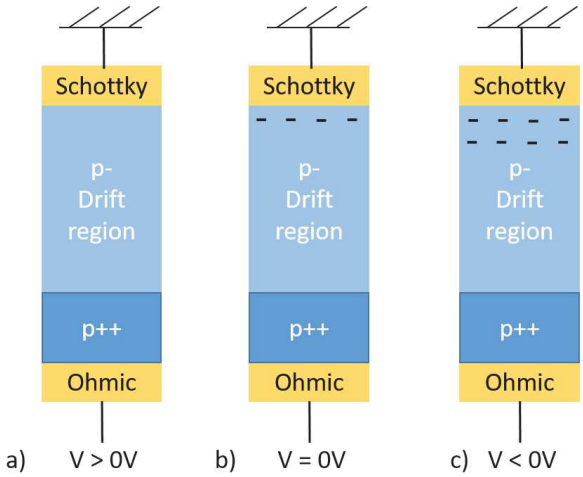

FIGURE 1.2: *p-type unipolar device (Schottky diode) diagram under different bias configuration "-" represents the depletion width, a) a positive bias is applied, the device is ON, b) at 0V the device is at equilibrium a small depletion layer is created underneath Schottky contact, c) a reverse bias is applied the depletion width is increasing*

To compare each diode some important concepts have to be introduce. The first one, is the specific ON-resistance $R_{on}S$ which will give information about the ON state of the diode and can be defined as:

$$R_{on}S = \frac{W_D}{q\mu_p(N_a - N_d)} \tag{1.4}$$

With q the elementary charge, W_D the drift region width, μ_p the holes mobility and $N_a - N_d$ the effective acceptor concentration. The second one is the breakdown voltage (V_B) where the electric field reaches the material breakdown field. This can be defined as the area under the drift width vs. electric field plot as shown in figure 1.3. And V_B can be express as:

$$V_B = \frac{W_D E_B}{2} \tag{1.5}$$

Two situations can occur depending on the drift layer thickness (e_D) and the depletion width (W_D):

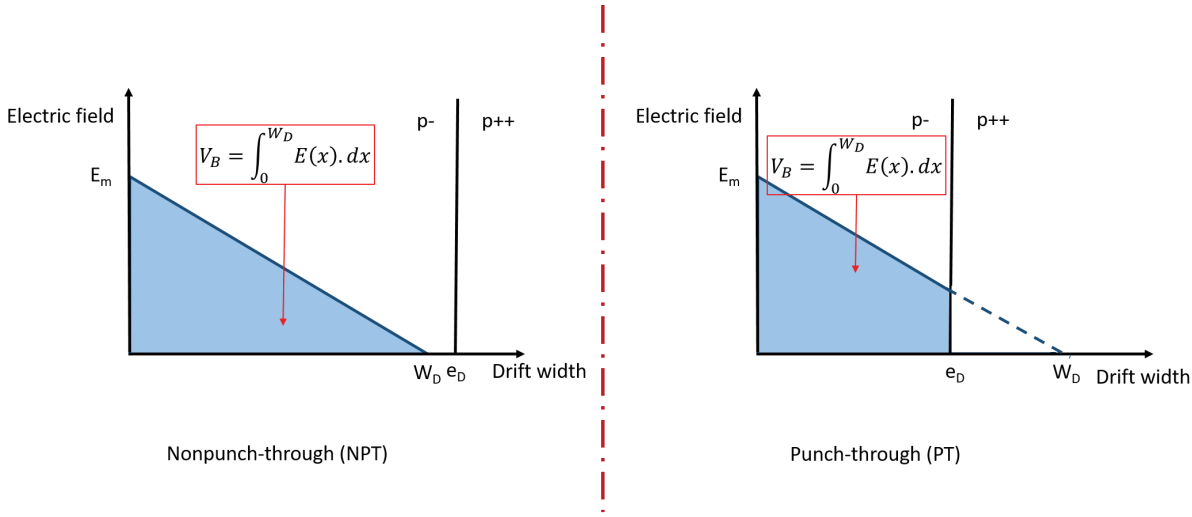

FIGURE 1.3: *Electric field profile in nonpunch-through ($e_D > W_D$) and punch-through ($e_D < W_D$) condition, with e_D the active layer thickness and W_D the depletion width*

- if $e_D > W_D$: the device is in nonpunch-through (NPT) condition, the electric field can extend completely into the active layer. (fig. 1.3 left part)
- if $e_D < W_D$: the device is in punch-through (PT) condition, the electric field will be stopped by the heavily doped layer and will not completely extend. (fig. 1.3 right part)

A trade-off between active layer thickness and the depletion width has to be found in order to obtain the best component as possible. [5]

The acceptor concentration (N_a) in the the drift region thanks to equations 1.4 and 1.5 can be written as follow:

$$N_a = \frac{\epsilon_0 \epsilon_r E_B^2}{2qV_B} \tag{1.6}$$

By combining all these equations it is possible to compare $R_{on}S$ with V_B, that give us the Baliga's figure of merit.

$$\frac{V_B^2}{R_{on}S} = \frac{\epsilon_0 \epsilon_r \mu_p E_B^3}{4} = \frac{BFOM}{4} \tag{1.7}$$

Now using formula presented above as well as the theoretical values for each material from table 1.1 each diode characteristics can be calculated. Those results are presented in table 1.2.

From this comparison diamond shows its full potential, in fact for the same V_B the drift layer needed is more than 30 times thinner than silicon. Diamond has a 4 decades difference $R_{on}S$ with Si while other material have only 2 decades difference with p-type diode. If n-type diodes are taken into account this difference can be reduced at less than 1 decade with Ga_2O_3. The advantage of Ga_2O_3 is the big size wafer availability but other physical parameters are problematic for the power device community for example its low thermal conductivity which does not allow to work at high temperature (i.e silicon device).

TABLE 1.2: *1kV on 1cm² substrate from different materials ideal diode*

Parameters	Si	4H-SiC	GaN	Ga_2O_3	Diamond
W_D (μm)	66	10	6.6	2.5	2
$R_{on}S$ ($\Omega.cm$) p-type	2.95E-5	5.76E-8	9.29E-8	-	4E-10
$R_{on}S$ ($\Omega.cm$) n-type	9.45E-6	5.76E-7	1.48E-8	2.94E-9	8.21E-10
Baliga's FOM	1	165	635	3214	23017

Comparison can also be made thanks to the graph presented in figure 1.4. This plot the specific on-resistance as function of the breakdown voltage. It presents one dimensional simulations made by Umezawa *et al.* [6] at room temperature for Si, SiC and diamond and at high temperature (523K) for the last two. On this graph are also placed some experimental data for each material.

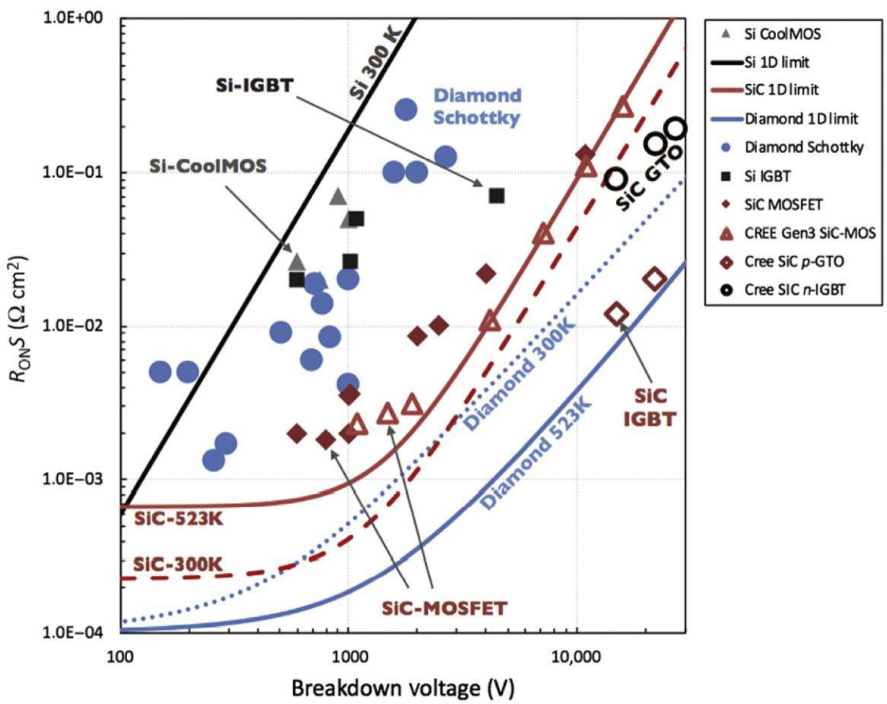

FIGURE 1.4: *Specific on-resistance as function of the breakdown voltage for different materials Si, SiC and Diamond. On this graph the theoretical 1D simulations are presented at room temperature and at high temperature [6]. Dots are experimental data. [7]*

It appears that diamond Schottky diode experimental data are far from the theoretical curve with an higher specific On-resistance and a lower breakdown voltage. As say before the model used for the theoretical curve is 1D but the measured device are 3D which can differ from 1D theoretical device. Also it appears than other technologies manage to get

to close to their theoretical value but lots of effort have been done by many groups and industries for Si and SiC and in comparison diamond is still "young" only lab are working to improve the component characteristics and lot of technological locks need to be solved.

1.1.2 Current power device market

The power device market is still under Silicon device domination. This power device market can be separated into different sector high frequency device with new component such as HEMT GaN and high voltage our target. The best Si Schottky diode on the market sustained 1000V in blocking mode and can work under 175°C. From 2001 SiC Schottky diode started to be commercialized. And Wollfspeed proposed a device that can sustained 1700V in reverse mode [1] with a 50A DC current available and working at a maximum temperature of 325°C.

1.2 State of the art

During the last decade several diamond components were proposed. In this section a quick summary of existing devices will be made with a special attention on diamond Schottky diode devices.

1.2.1 Diamond power devices

In the power device community there is two kind of devices, unipolar devices and bipolar devices. For diamond bipolar devices are more difficult to achieve due the difficulty to obtain n-type diamond. In figure 1.5, diamond band diagram is presented with the three available main dopants ionization energy. For p-type diamond, boron is used with a 380 meV ionization energy. For n-type, there are two possible dopants both with an higher ionization energy, phosphorus at 570 meV and nitrogen at 1.7 eV. So even when the doping of the material is achieved, it is more complicated to obtained activated dopants with electrical properties. For n-type with phosphorus dopant several group have been working on its incorporation firstly Koizumi *et al.* [8] and after other group on different crystallographic orientation [9, 10, 11]. For p-type doped diamond, which is easier to obtain, several group are working on it [12, 13, 14, 15] and is started to be available commercially. [2]

Different components can be find in the literature from the easiest one which are Schottky diode (developed in the next section) to more complicated ones such as field effect transistor (FET) bipolar junction. In the FET familly several devices have to be mentioned. A FET can be realized with metal-oxide-semiconductor stack (MOSFET) or directly with a metal-semiconductor interface (MESFET). Junction FET can also be created but required to have both p and n type diamond layers. Different examples are presented in figure 1.6

All of this FET can have two different terminations hydrogen or oxygen ones which will bring different properties.

[1] https://www.wolfspeed.com/power/products/sic-schottky-diodes/cpw5-1700-z050b
[2] http://diamfab.eu/

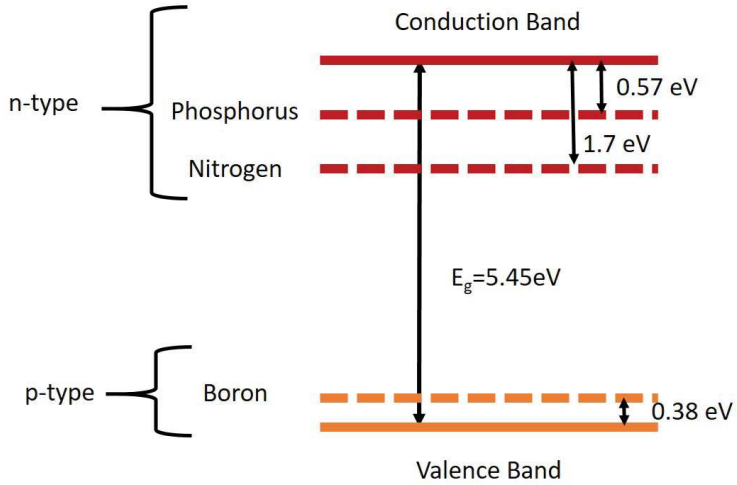

FIGURE 1.5: *Diamond band diagram with the different dopants ionization energy (eV)*

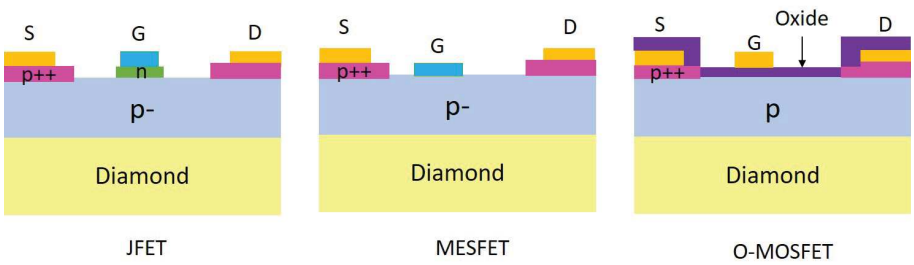

FIGURE 1.6: *Schematic side view of JFET, MESFET and MOSFET architecture, here G, D and S stand for gate, drain and source contacts*

- **H-terminated FET (H-FET)**

In that case the channel conduction will occur at the diamond surface thank to two dimensional holes gas (2DHG) creation. Those devices have been investigated by several groups [16, 17, 18] and the latest reported [19]. This last device is showing the lower ON-state resistance and the higher current densities (212 mA.mm^{-1} at RT and 200°C; BV around 350V) but those characteristics are temperature dependant and decrease with the temperature increasing. Currently some passivations are under study to have a better stability at high temperature [20]. With this technique breakdown capabilities of HFET have been improve up to 1700V [21]. All of this devices are mainly fabricated for high frequency (>1GHz) work such as micro-wave and radio frequency applications and not related to this work.

- **O-terminated FET (O-FET)**

In this other case, the conduction mechanism will be different and occur directly inside the bulk material due to an higher doping level. For oxygen terminated device JFET, MESFET and MOSFET have been reported. Several JFET have been reported by Isawaki *et al*. [22, 23, 24] with some promising results (BV > 600V, I_{max}=2μA). In the MESFET case, it have recently been reported a new reverse blocking MESFET with a blocking capability around 3kV [25] following the work initiated by Umezawa *et al.* [6]. Both JFET and MESFET show promising blocking capability but the ON-state current density is still a limiting factor for power electronic used. An other device, called D3MOSFET for Diamond Deep Depletion MOSFET is now showing very interesting results and have been first demonstrated by T.T Pham *et al*. [26]. This first device was showing a blocking capability about 200V but a poor ON state current density. An improved version with a better ON state have been published since with the add on of a p++ layer underneath source and drain [27].

1.2.2 Diamond Schottky diodes

Diamond Schottky diode is the most advance component first results appeared in the 90's [28, 29, 30] and a lot of work have been published after that by different groups around the world: Japan, US, China and France with some good results for the ON state and the OFF state. Different types of devices are coexisting: vertical, pseudo-vertical, PN and P-i-N Schottky diodes (fig. 1.7).

Vertical Schottky diodes have shown good results with the highest breakdown voltage reached for a Schottky diode (>7.5kV) by Volpe *et al*. [31] but a poor the ON-state. Other work have been done later in order to reduce the serial resistance and to improve the device ON-state [32, 33, 34]. One of the issue with this kind of device is the heavily doped substrate used, due to the high number of defects present in the substrate and later in the grown layer. This will by the way increasing the risk of premature breakdown or leakage current of the vertical device. Another approach was to create PN-Schottky diodes as done by [35, 36, 37, 38], those devices show the best ON-state for a Schottky diode with a current density of 60 000 $A.cm^{-2}$ at a forward bias of 6V [36]. The last device proposed is a bipolar device called

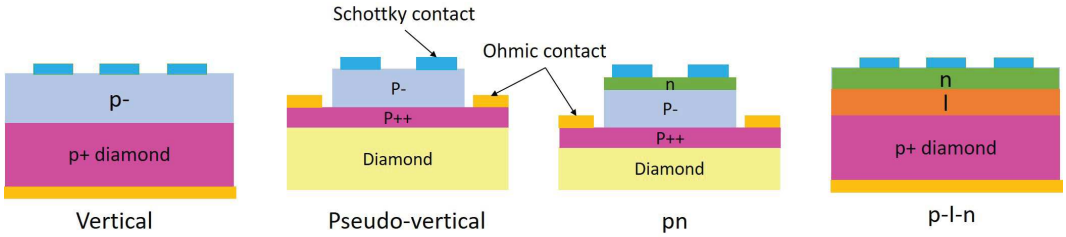

FIGURE 1.7: *Schematic side view of vertical, pseudo-vertical, pn and p-I-n Schottky diode*

a p-I-n diode, a diamond intrinsic layer is introduce between the p and the n type layer [39, 40, 41]. The best p-I-n diode reports a breakdown voltage about 1.1kV but with a current density inferior to 10 A.cm−2 at 10V and room temperature [39]. But with a temperature increase current density becomes higher than 100 A.cm−2 also at 10V and published by Dutta *et al.* [40].

Edge terminated devices are also under investigation to improve the device OFF-state. The edge termination will allow a better distribution of the electric field at the Schottky contact edge. Therefore the breakdown voltage should increase and the leakage current decrease. Different edges terminations are competing and presenting in figure 1.8.

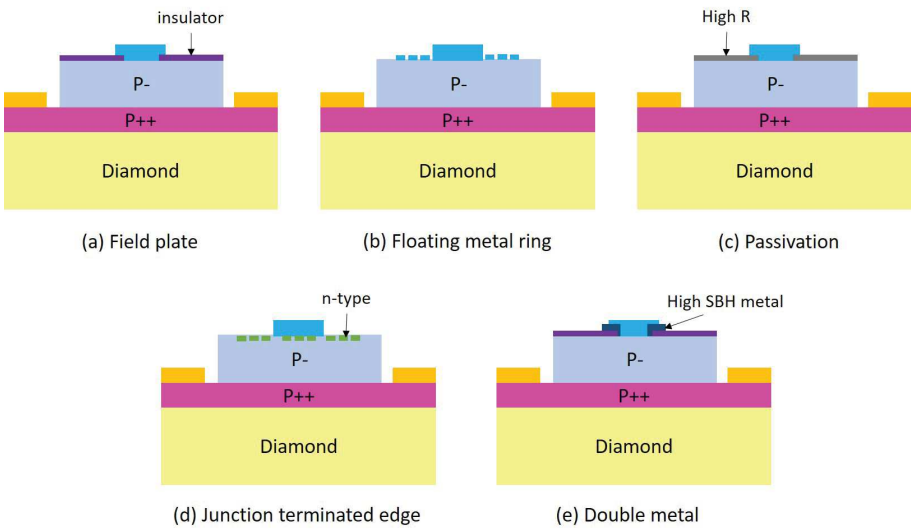

FIGURE 1.8: *Schematic side view of different edges terminations possible for diamond Schottky diode*

On this figure the first edge termination (a) is the field plate technique, an insulating layer (most of the time Al_2O_3 or SiO_2) is deposited on top of the active layer. [42, 32, 43, 44]. The second technique presented is to deposit floating metal ring (FMR), the FMR can be from the same metal that the Schottky diode (b) [45], or can it can be with a different metal with an higher Schottky barrier height (c) [46]. Another solution is to use surface termination like fluorination as presented by Zhao *et al.* [47].

Recently new applications have been under investigation with diamond Schottky diode. Thanks to the diamond high resistance to high temperature and radiations (α particules, X-ray,...) some groups are looking at it to work in harsh environment such nuclear facilities and even for space. [48, 49] Lot of possibilities are open and the interest for diamond Schottky diode is still increasing.

1.3 Theoretical background

In this section the theoretical background about unipolar device and especially Schottky diode will be explained in order to promote a better understanding of the following chapters.

1.3.1 General concepts

A Schottky diode is composed with two different metal-semiconductor (MS) contacts: the ohmic contact and the Schottky contact. The difference between each contact will depend of the metal work function (Φ_m). If it is higher or lower of than the one of the semiconductor (Φ_s) depending of the type of device (p or n). In both cases the work function can be defined as the energy needed to promote one electron from the Fermi level of semiconductor or metal (E_F) to the vacuum level. In this section the focus will be made on p-type Schottky diode.

1.3.1.1 Ohmic contact

In the case of the ohmic contact Φ_m has to be higher than Φ_s. The band diagram for the ohmic contact is shown in figure 1.9. When the junction is made between the metal and the semiconductor both Fermi level $E_{f,m}$ and $E_{f,s}$ are aligned and an upperward band banding occurs. In that case the holes accumulation will flow directly from the semiconductor to the metal with an applied bias. The semiconductor resistance is then determined by the Ohm law: $R = \frac{V}{I}$ with V the bias and I the current intensity.

1.3.1.2 Schottky contact

For the Schottky contact Φ_m is higher than Φ_s leading to a downward band banding at the thermal equilibrium (right part of figure 1.10). In that situation the creation of a built-in potential appears Φ_b and can be defined as the difference between the semiconductor valence band (VB) minimum and the metal Fermi level at the interface. This is called the Schottky barrier.

The ideal Schottky barrier can be written thanks to the Mott equation as:

$$\Phi_b = \frac{E_g}{q} - (\Phi_m - \chi_s) \text{ with } \chi_s = \Phi_s - (E_c - E_{f,s}) \tag{1.8}$$

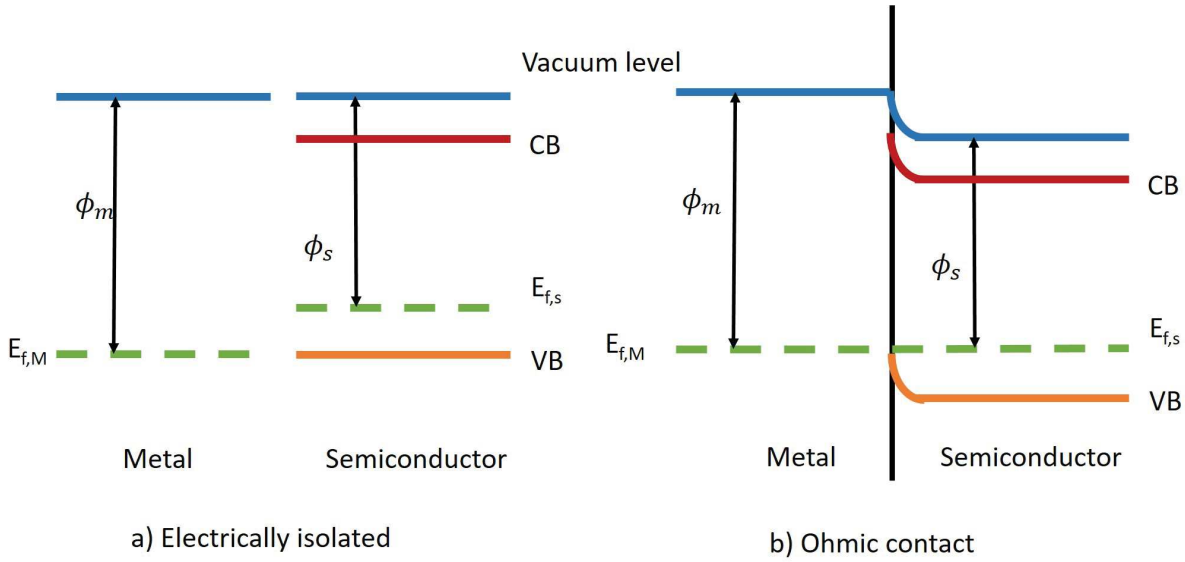

FIGURE 1.9: *Band diagram between a metal and a p-type semiconductor forming an ohmic contact with upward band bending to the metal, electrically isolated in a) and at equilibrium in b) with Φ_m the metal work function and Φ_s the semiconductor work function*

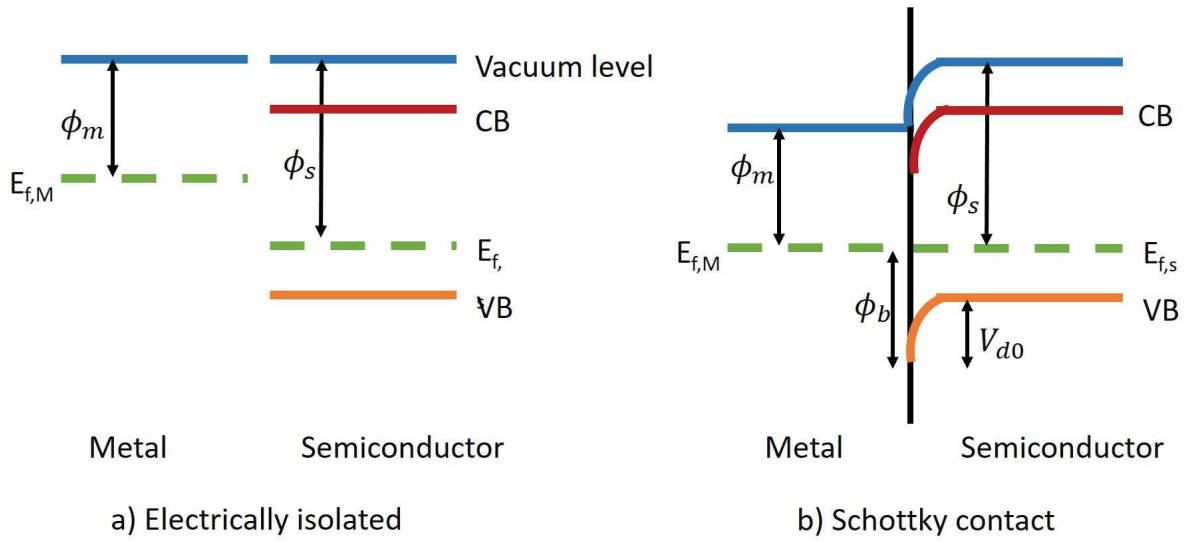

FIGURE 1.10: *Band diagram between a metal and a p-type semiconductor forming a Schottky contact with downward band bending to the metal, electrically isolated in a) and at equilibrium in b) with Φ_m the metal work function, Φ_s the semiconductor work function, Φ_b the Schottky barrier height and V_{d0}*

where χ_s and E_c stand for the semiconductor electronic affinity and its conduction band energy. Another important parameter for the Schottky contact is the V_{d0} which represents the potential barrier encounter by the free carrier diffusing toward the metal. In the case of lightly doped semiconductor it can be approximated like $qV_{d0} \approx q\Phi_b - E_a$ with E_a the acceptor activation energy. When a bias (V) is applied to the junction the V_{d0} will change and it will change the current depending of the sign. The new potential barrier can be written as follow:

$$qV_d = qV_{d0} + qV \tag{1.9}$$

- If V > 0, the barrier will lowering and will facilitated the carrier passage from the semiconductor to the metal.
- If V = 0, it is the thermal equilibrium the current coming from one side to the other are equals.
- If V < 0, the barrier will increase and will facilitated the carrier passage from the metal to the semiconductor.

In reality an intermediate layer is created at the interface between the metal and the semiconductor which will take into account all the imperfections of the junction. This model was proposed by Bardeen in 1947 [50] and it introduced the idea of interface states which will modify the value of the Schottky barrier and the depletion region.

1.3.2 I-V characteristics

For a Schottky diode two states can be defined, as presented before, the forward ON state where current is flowing and the OFF state in reverse where there is supposedly no current, the red curve on figure 1.11. This graph represents the ideal case (red) and the real case (the blue curve) where some leakage currents are visible on reverse. In this section the forward and the reverse currents will be explained with more details, all mechanisms needed to be taken into account will be presented.

1.3.2.1 Forward current

Thermionic and diffusion current

In the forward region two main mechanisms are in action and will be explained in this section. The thermionic emission current refereed as J_{TE} which corresponds to holes from the semiconductor going to the metal passing toward the Schottky barrier and the diffusion current (J_D). These mechanisms can be combined in one equation thank to the thermionic-emission-diffusion model (J_{TED}) proposed by Crowell and Sze in 1966 [51] and based on the thermionic recombination velocity v_R the derivative of the boundary conditions:

$$J_{TED} = \frac{qN_v v_R}{1 + \frac{v_R}{v_D}}.exp\left(-\frac{q\Phi_b}{k_B T}\right)\left[exp\left(\frac{qV_j}{k_B T}\right) - 1\right] \tag{1.10}$$

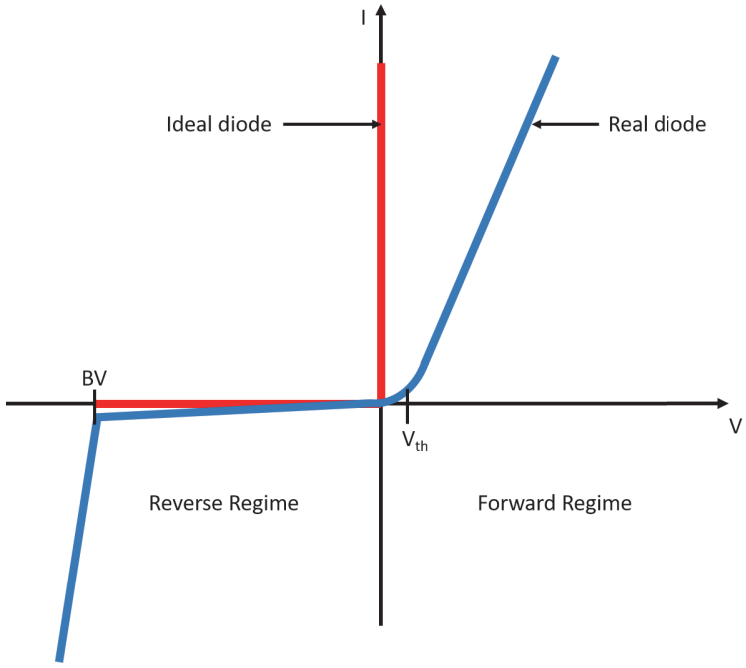

FIGURE 1.11: *Intensity-current diagram of a Schottky diode, in red the ideal diode and blue a real diode*

with N_v the state valance band effective density, v_D the effective carrier diffusion velocity and V_j the forward bias. Both v_R and v_D have been expressed by Mönch [52]. The maximum recombination velocity is related to the thermal velocity v_{th}.

$$v_R^{max} = \frac{< v_{th} >}{4} = \frac{1}{4}\left(\frac{8k_BT}{\pi m^*}\right)^{(1/2)} \tag{1.11}$$

v_D can be approximated by taking into account the holes diffusion constant D_p and the holes mobility μ_p.

$$v_D \approx \frac{qD_p}{k_BT}E_i = \mu_p E_i \text{ with } E_i = \sqrt{\frac{2q(V_{d0} - V_j)N_a}{\epsilon_0\epsilon_s}} \tag{1.12}$$

So depending of the ratio between v_D and v_R the limiting mechanism will change. In the case of p-type diamond Schottky diodes $v_D >> v_R$ and regarding Bethe's criterion as done by Traore [53] this is leading to thermionic emission (TE) current only. This current can be express as follow:

$$J_{TE} = J_0^{thermo}\left[exp\left(\frac{qV_j}{k_BT} - 1\right)\right] \tag{1.13}$$

J_0^{thermo} is defined thanks to the saturation current model for thermionic emission:

$$J_0^{thermo} = qN_v v_{coll} exp\left(\frac{-q\Phi_b}{k_BT}\right) \tag{1.14}$$

an other way to write it is:

$$J_0^{thermo} = A^* T^2 exp\left(\frac{-q\Phi_b}{k_B T}\right) \tag{1.15}$$

Where A^* stands for the effective Richardon's constant and is defined for p-type doped diamond with respect to the effective mass of light and heavy holes i.e m^*_{lh}=0.366m_0 and m^*_{hh}=0.427m_0 ([54]) and the effective mass of free electron m_0.

$$A^* = \frac{(m^*_{lh} + m^*_{hh})A}{m_0} \text{ with } A = \frac{q\pi m_0 k_B^2}{h^3} = 120\ A.cm^{-2}.K^{-2} \tag{1.16}$$

In that case A^* is usually taken equal to 92 $A.cm^{-2}.K^{-2}$. [55].

Schottky Barrier lowering

Another parameter has to be taken into account when looking at the forward current: the Schottky barrier lowering phenomena. It is also called the image force lowering. This principle is shown is figure 1.12. In the case of p-type diamond when a hole is at an x distance from the junction at is equal distance to metal an image charge will be created to allow the electric field to be perpendicular at the interface.

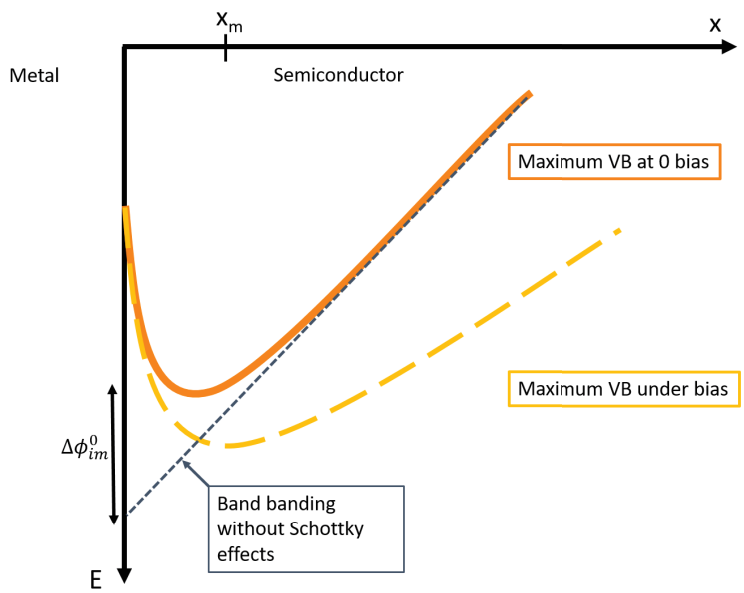

FIGURE 1.12: *Diagram of the Schottky effect in the case of p-type doped diamond with the valance band (VB) under different bias*

The lowering of the barrier can be expressed as:

$$\Delta\Phi_{im} = \sqrt{\frac{qE_m}{4\pi\epsilon_0\epsilon_r}} \tag{1.17}$$

with the maximum electric field at the surface calculated using the depletion approximation:

$$E_m = \sqrt{\frac{2qN_a(V_{d0} + V_j)}{\epsilon_0 \epsilon_r}} \tag{1.18}$$

where N_a is the acceptor doping level.

The actual Schottky barrier taking into account the barrier lowering is written as follow:

$$\Phi_b = \Phi_{b0} - \Delta\Phi_{im} \tag{1.19}$$

this new value is dependant of the applied bias. When a positive bias will be applied, the barrier will have the tendency to increase and can be express as:

$$\Phi_b(V) = \Phi_b^0 + (1 - \frac{1}{n_{ij}})V \tag{1.20}$$

with n_{ij} which is the ideality factor defined as:

$$n_{ij} = \left(1 - \frac{\Delta\Phi_{im}^0}{4qV_{d0}}\right)^{-1} \approx \left[1 - \frac{1}{4q}\left(\frac{2q^3N_a}{(4\pi^2(\epsilon_0\epsilon_r)^3}\right)^{1/4}(V_{d0})^{-3/4}\right]^{-1} \tag{1.21}$$

At the contrary when a reverse bias is applied, the Schottky barrier height is decreasing. So finally the Schottky barrier can be express like this [56, 57]:

$$\Phi_b(V_r) = \Phi_b^0 - \Delta\Phi_{im} - \alpha E_m \tag{1.22}$$

This equation is taking into account the dipole creation at the interface between the metal and the semiconductor [58]. By replacing into the last equation Φ_b^0, $\Delta\Phi_{im}$ and E_m by their expressions define above Φ_b is becoming:

$$\Phi_b(V_r) = \Phi_b^0 - \left(\frac{2q^3N_a}{(4\pi)^2(\epsilon_0\epsilon_r)^3}[V_{d0} + V_r]\right)^{1/4} - \alpha\left(\frac{2qN_a}{\epsilon_0\epsilon_r}[V_{d0} + V_r]\right)^{1/2} \tag{1.23}$$

on both cases α is a constant linked to the interface state present in the device.

Final forward current

So finally taking into account all phenomena presented above with the barrier lowering and the thermionic emission, the total forward current can be expressed like this:

$$I = I_s exp\left(\frac{q(V - RI)}{nk_BT}\right)\left[1 - exp\left(-\frac{q(V - RI)}{k_BT}\right)\right] \tag{1.24}$$

with I_s is the saturation current which can be written as follow:

$$I_s = A^*ST^2exp\left(-\frac{q\phi_b^0}{k_bT}\right) \tag{1.25}$$

with S the surface of the diode. The ideality factor, n, which can be calculated thanks to the next formula (1.26) and determine the quality of the interface between the Schottky

contact and the diamond. If n is equal to 1 the interface is considered as perfect, it will be shown in the following chapter that it is not the case for working devices.

$$n = 1 - \beta = 1 - \left(\frac{\partial \Phi_b}{\partial V_j}\right) \tag{1.26}$$

1.3.2.2 Reverse current

The reverse current as well as the forward is dependant of the Schottky effect presented in the previous section. This current was express by Padovani and Stratton [59] using the thermionic emission for reverse current theory as follow:

$$J = \frac{2A^*(q\pi TV)^{1/2} qE_{00}}{k_B^{3/2}} exp\left(-\frac{q(\Phi_b(V_r)}{k_B T} + \frac{q^3 V E_{00}^2}{3(k_B T)^3}\right) \tag{1.27}$$

In this equation $\Phi_b(V_r)$ can be replaced by the equation in formula 1.22 and 1.23. Also E_{00} is defined as [59]:

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N}{m^* \epsilon_0 \epsilon_r}} \tag{1.28}$$

It has also been express by Umezawa [55]:

$$E_{00} = 18.5 * 10^{-15} * \frac{N_a}{(5.7m^*)^{0.5}} \tag{1.29}$$

This can only be used for the non punch-through deign device.

1.3.3 C-V characteristics

From the reverse side of a diode other parameters can be measured allowing to have information about the active diamond layer. The measure of the capacity is one them [60]. To do so, a small AC voltage is superimposed on the DC bias used to measure. The frequency of the AC voltage can be determined by performing capacitance-frequency measurement. The choice of the working frequency is very important, the chosen frequency has to be in the device bandwidth if not the obtained measure will be false.

$$C = \frac{-dQ_s}{dV} = qA\frac{d}{dV}\int_0^w N_a \mathrm{d}x = qN_a(w)\frac{dw}{dV} \tag{1.30}$$

with Q_s standing for the charges inside the semiconductor and w the space charge region width.

$$w = \sqrt{\frac{2\epsilon_0 \epsilon_r V}{q(N_a - N_d)}} \tag{1.31}$$

The capacitance can also be express as:

$$C = \frac{\epsilon_0 \epsilon_r S}{w} \tag{1.32}$$

In this last formula the capacity is related to S which is the surface of the diode. From both previous equations it is possible to determine the effective doping level $N_a - N_d$ by plotting the $1/C^2$ in function of the bias as shown on figure 1.13 and by fitting the linear part (red dash line). With the same plot it is possible to extract the build in potential V_{bi}.

$$N_a - N_d = \frac{-2}{q\epsilon_s\epsilon_0 S^2 \frac{d(1/C^2)}{dV}} \tag{1.33}$$

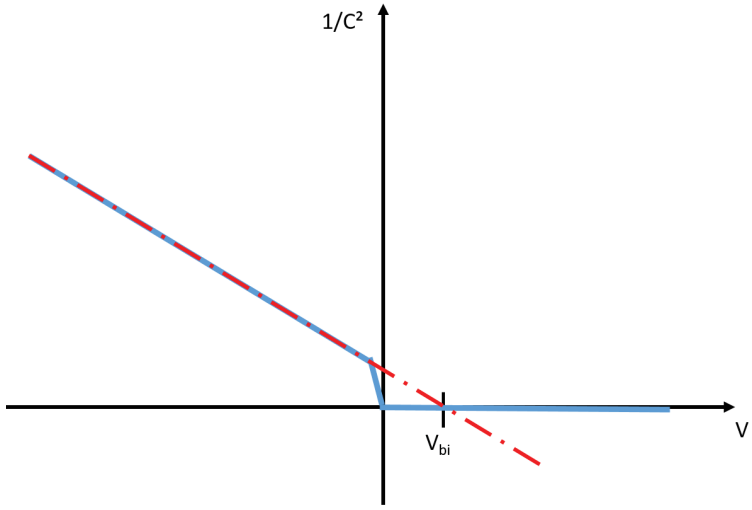

FIGURE 1.13: $1/C^2$ *in function of bias diagram for a p-type Schottky diode in blue and in red dash line the fitting used for doping extraction*

On some cases the linear part does not exist and that means that the doping level of the probe layer is not homogeneous. In that case it is possible to plot the doping depth profile using equation 1.32 and 1.33.

1.4 Summary

To sum up, lot of parameters have to be taken into account when fabricating diamond Schottky diodes. The doping level as well as the layer thickness have a big impact on the diode electric field (i.e punch through or non-punch through design) and so on the diode figure of merit especially the Baliga's one. Also it appears by looking at the equations that the interface between the diamond active layer and the Schottky metal play a very important role on the diode electrical characteristics (i.e leakage and premature breakdown). Equations presented in this chapter will be used in the following chapters to extract diodes parameters and to compare them for example with the Schottky barrier height, the serial resistance and the effective doping level of the active layer.

Chapter 2

Diamond Schottky diodes fabrication

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Fabrication process to obtain diamond Schottky diodes is composed with several steps which can become a limitation for the component improvement. In this chapter, all steps will be presented with an highlight on the techniques developed during this thesis in order to overcome those limitations. The accent will put on diamond growth new techniques and clean room fabrication.

2.1 Diode Structure and problematic

As shown in the previous chapter, one of the best candidates for diamond power device is the vertical Schottky diode. But this architecture requires a good quality and an heavily doped layer which is currently not available (number of dislocations to high). To bypass this issue the pseudo-vertical architecture has been proposed (figure 2.1 right part). In that case the heavily doped layer is grown on top of good quality substrate allowing to increase the p++ layer quality and then after the p- one's. To compare them, both architectures are presented in figure 2.1. In each case Schottky contacts are on the p- layer (in dark blue on the figure) and the ohmic ones (in orange on the figure) on the p++.

For the vertical structure the heavily doped substrate is about 300 μm thick which is 600 times higher than the heavily doped layer included in the pseudo-vertical architecture. It is known that heavily doped diamond have more chance to introduce dislocations and defects that lightly doped one and that unfortunately increases with the thickness [6, 61]. One important step in the diamond Schottky diode fabrication is the interface between the p++ and the p- layer. This interface is crucial because it will have an impact on the quality on p- grown layer. More dislocations at the interface will lead to more chances to have a bad quality grown layer at the end. Finally, this could impact the electrical characteristics of the diode. Pseudo-vertical architecture have a thinner p++ layer grew on a good quality substrate (HPHT substrate) so number of defect will be lower in the p- layer. On figure 2.1 also appears the two conduction paths for both devices. In the vertical one it have to go through the entire p++ layer increasing the risk to meet with a defect. On the other hand, the conduction path in the pseudo vertical architecture is going through the p- and along the p++/p- interface inside the p++ layer. For the conduction an other important parameter is the doping level of the layer. Higher the p++ doping level is, lower will be the resistance, for the grown p++ layer by CVD it is "easy" to reach more than 10^{20} atom.cm^{-3} unlike p++ substrate which can be doped only up to 10^{19} atom.cm^{-3}. Pseudo-vertical architecture shows also some limitations with the presence of mesa etched structures for example (etching, thickness,..).

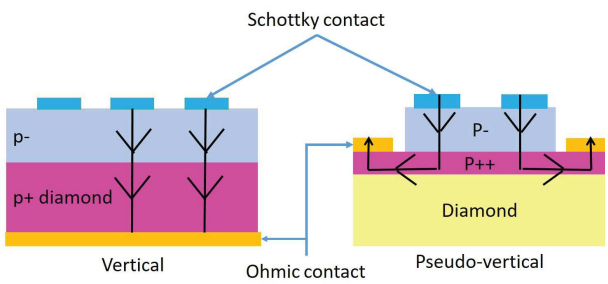

FIGURE 2.1: *Sketch of both architectures: vertical on the left, pseudo vertical on the right*

In order to improve the performance of the diode for reverse blocking capabilities an increase of the p- thickness is needed. This will generate an additional difficulty to reach

the p++ and realize the ohmic contact in the pseudo-vertical case. Currently this layer is reached by performing deep reactive ion etching (DRIE). This technique allows us, at the present time, to etch about $4\mu m$ which will not be sufficient to improve our components. In this chapter all the step needed to obtain diamond Schottky diode shall be presented and various solutions shall be suggested to remove the deep etching issue.

2.2 Diamond growth

Diamond (CFC structure) is one of the carbon alloptrope as shown on carbon phase diagram presented in figure 2.2. On this graph the different ways of obtaining synthetic diamond are presented. There are two main ways to do so. The first one is close to the natural one: applying high temperature and high pressure (HPHT), the second one which requires less pressure and less temperature is the chemical vapor deposition (CVD) technique. To compare, HPHT growth occurs around $1500°C$ and 7GPa either 7.10^7 mBar, for CVD it is around $900°C$ and 150 mBar.

CVD growth is used because it allows good control of the physical and electrical properties of the diamond such as impurities incorporation which can creates issues for doing power devices as well as the thickness of the grown layer. Also CVD growth cost is lower than the one for HPHT which requires bigger equipment.

By CVD the two types of doping can be achieved p-type doping with incorporation of boron atoms and n-type with incorporation of phosphorus atoms.

There are two different CVD methods. The hot filament (HFCVD) method and the microwaves plasma enhanced one (MPCVD). This last will be more detailed in the next section. The choice of MPCVD over HFCVD had been chosen because of the absence of contamination risk by the tungsten wire [62]. Anyway the HFCVD methode is still under investigation in other laboratories [63, 64]. Lately combination of both methods shows promising results in order to decrease the dislocations numbers.

2.2.1 MPCVD

CVD growth consists of depositing the wanted material on top of a substrate thanks to gaseous precursors. Substrates used for those growths can be from the same materials, in that case it is called homoepitaxy, or from a different material and that is called heteroepitaxy, both are presented in figure 2.3. In this thesis only homoepitaxy growth was realized. Heteroepitaxy will be presented in chapter 6 as a solution to increase substrate size. For the diamond growth the gaseous precursors are dihydrogen (H_2), methane (CH_4) for the non intentionally doped layer. For the p-type layer other gazes are added as oxygen and diborane (B_2H_6) (in our case).

The first mechanism had been proposed by Harris and Goodwin in 1993 [65] following the equations presented below and it is summarized on schematics 2.4 and 2.5. The direct transformation from gaseous carbon (C(g)) to diamond (C(d)) is thermodynamically not possible at low pressure. The Gibb's free energy is equal to: $\Delta G = 2.9kJ/mole$. So an

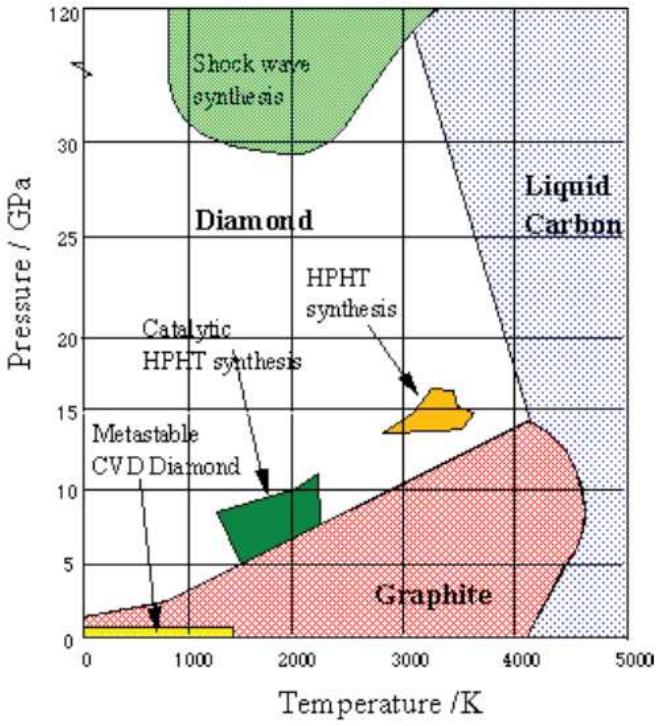

FIGURE 2.2: *Carbon phase diagram*

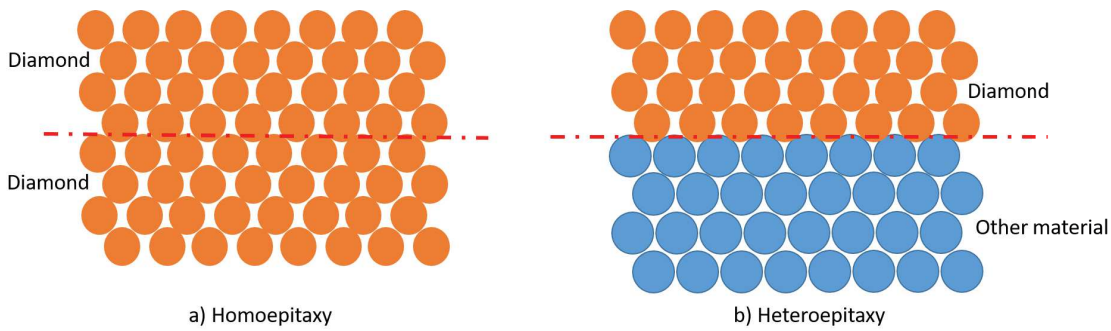

FIGURE 2.3: *comparison between homoepitaxy a) and heteroepitaxy b)*

indirect process is used to pass from C(g) to C(d). This transformation occurs in fact with five steps.

1. Hydrogen dissociation: $H_2 = 2H$ ($\Delta G \gg 0$)
2. Radical formation in the gaseous mixture: $CH_4 + H = CH_3 + H_2$ ($\Delta G \ll 0$)
3. Surface hydrogenation: $C(d) + H = C(d)H$ ($\Delta G \ll 0$)
4. Hydrogen removal: $C(d)H + H = C(d) + H_2$ ($\Delta G \ll 0$)
5. Methyl absorption: $C(d) + CH_3 = c(d)CH_3$ ($\Delta G \ll 0$)
6. **Finally:** $H + CH_4 + C(d) = C(d)CH_3 + H_2$ ($\Delta G \ll 0$)

Finally at the end, the transformation from C(g) to C(d) can occur thanks to all this reactions with a favorable energy balance.

All reactions presented above will help the diamond growth. Inside the plasma ball hydrogen dissociation will first appear. Dissociated hydrogen will have two different reactions with the diamond substrate as shown in figure 2.4. The first one will be the active site creation by taking an hydrogen atom from the diamond surface. The second one will hydrogenate open active site. Both reactions happened at the same time and the available active site number, named f^*, is only temperature dependant. It can be express by:

$$f^* = \frac{k_1}{k_1 + k_2} \tag{2.1}$$

with k_1 and k_2 respectively the probability to create and to hydrogenate an active site.

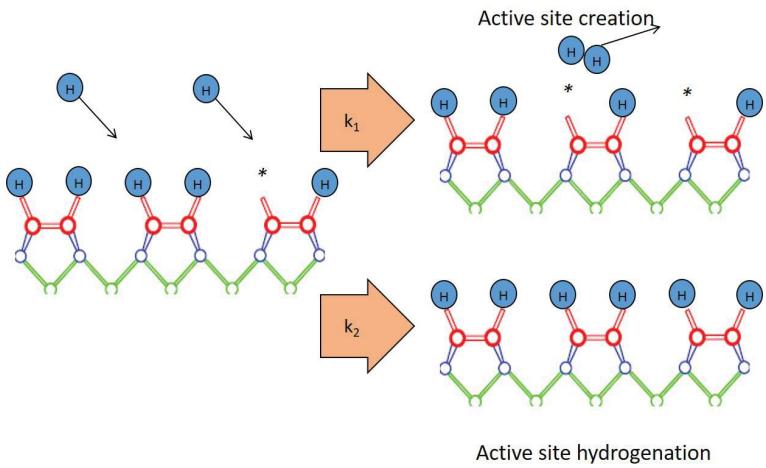

FIGURE 2.4: *Chemical reaction for active site creation and hydrogenation, with k_1 and K_2 the probability for each reaction*

On an active site a CH_3 group provided from equation 2 can be fixed on the diamond substrate. Once the group is fixed an hydrogen atom will come and combine with an hydrogen atom from CH_3 and leave a CH_2 link to the diamond. Finally another hydrogen will

come to pick the last hydrogen available and the remaining carbon atom will be integrated inside a new diamond layer. New dangling bounds will be created allowing the process to continue as long as wanted. All of these reactions are summarized in the figure 2.5.

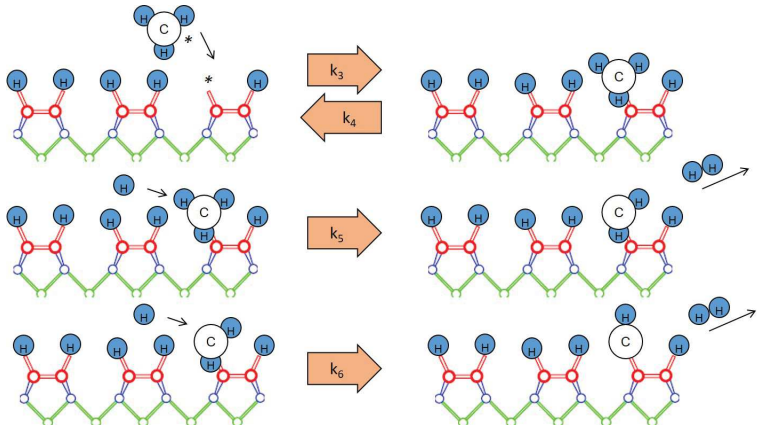

FIGURE 2.5: *Chemical reaction for the incorporation of carbon atom during diamond growth, k_3, k_4, k_5 and K_6 the probability for each*

Sample preparation and growth characterization

In the next section diamond growth by MPCVD will be presented. But to perform homoepitaxy, substrates are needed and some treatments have to be performed previous to the growth.

During this work all substrates used were (100) monocrystalline HPHT substrates supplied by New Diamond Technology (NDT) and re-polished after by Syntek company in Japan. This choice is motivated by the better results obtained with Syntek polishing than other polishing experts available. In general the surface roughness after polishing and before growth was below 0.3nm as shown on the optical profilometer view of the polished substrate in figure 2.6.

Once received samples were cleaned into an hot acid mixture and rinsed into acetone followed by isopropanol bath and, at the end, dried with argon or nitrogen. This treatment was also applied after each growth.

Growth quality and layer thickness were characterized by two methods at each steps.

Optical profilometry: This technique based on the Michelson's interferometer principle is used to check the roughness of the surface and the presence of surface defects. The one used is a Veeco 3D Contour GT, with two available modes the vertical scanning interferometry (VSI) mode for rough surfaces and the phase shifted interferometry (PSI) one for smooth surfaces. The resolution of this technique is 0.5 μm in lateral and 0.1 nm in vertical. This technique will be also used to check etching depth.

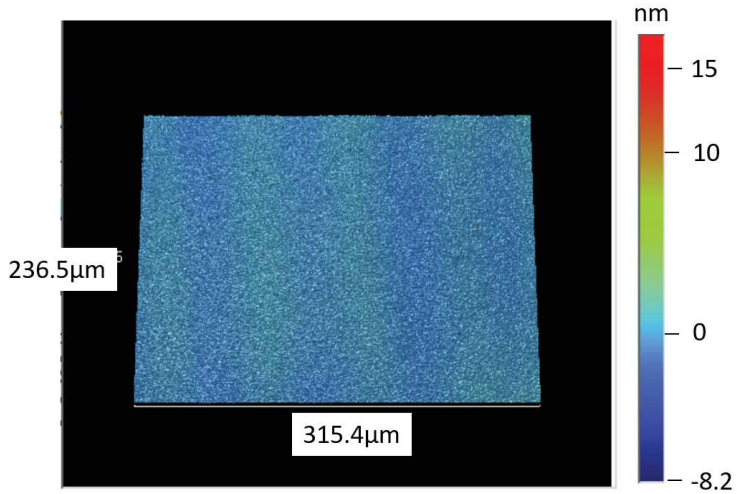

FIGURE 2.6: *Optical prolfilometer image of the surface after polishing by Syntek*

Ellipsometry: This technique is used to measure the thickness of the grown layer. It is based on the difference of polarization between the incident beam which has a linear polarization and the reflective beam from the sample which has an ellipsoid polarization. This difference is measured thank to two ellipsometric angles Φ and Δ. After those measurements were fitted as demonstrated by Bousquet *et al*. [66] to extract the thickness value. The resolution of this measure is about 5nm. The apparatus used is a Woollam M2000 ellipsometer running with the Complete Ease software.

In this thesis the CVD was enhanced using micro-wave plasma that is called micro-wave plasma enhanced chemical vapour deposition (MPCVD).This technique allows to grow diamond with a wide range of doping level from highly doped diamond i.e $[B] > 10^{21}\ atom.cm^{-3}$ which will be called p++ on the rest of this work to non intentionally doped i.e $[B] < 5 * 10^{15}\ atom.cm^{-3}$ (p- layer).

2.2.2 From heavily doped layer to slightly doped one

At Institut Néel one reactor is dedicated to grow from heavily doped to slightly doped boron layer.

First the sample is introduced into the growth chamber and placed at the intersection with the microwave generator wave guide. A 2.45GHz microwaves generator is used to enhanced and stabilized the plasma by providing an electromagnetic wave with a 12cm free space wave length. This electromagnetic wave will provide kinetic energy to the gaseous precursors electrons that will be able to ionize other molecules from the gaseous mixture and ignite the plasma. The plasma will take place at the intersection between the wave guide and a dielectric tube within the gaseous mixture is injected. The wave guide is sizable thank to a piston at the end, this allows to work on the reflective wave and the plasma position. Once the plasma started the microwave has to be adjusted to have the less reflected power

as possible by playing with impedance tips. If the reflective power is to high the plasma can stop. It is preferable to start the plasma at low power and low pressure. When the plasma is on and stable, the microwave power and the pressure inside the growth chamber can be modified to change plasma size and density. For example by increasing the pressure inside the chamber the plasma will be smaller and denser. During this step the impedance have to be adjusted in real time to avoid a plasma switching off by a reflective power increase. This reactor allows us to work in different conditions, for example the working pressure can be chosen between 5 and 133 mBar. Also the microwave generator working at 2.45GHz produces a power range from 0 to 2000 W. Another important parameter is the sample positioning inside the chamber. The entire sample has to be centered inside the plasma ball. The plasma ball typical size during growth is about 2cm diameter. This positioning has also some consequences on the substrate temperature. The temperature has to be well controlled during the growth and measure during all the time.

Before performing any type of growth in this reactor a pre-treatment was applied at each sample to ensure that there were no contamination from other carbon phases (i.e graphitic layer). This pre-treteament is a two hours 33 Torr, 200 sccm H_2 plasma pre-treatment. This step is also necessary to get the sample at growth temperature.

For the Schottky barrier diode the first grown layer is an heavily doped one with a very high boron concentration to reach the metallic transition which is above $[B] > 5 * 10^{20}$atom.cm^{-3} [67]. In figure 2.7 is plotted the boron concentration as function of the boron over carbon (B/C) ratio for different carbon over hydrogen (C/H) ratios. First, on this graph the boron concentration evolves in the same direction than the B/C ratio and C/H. From this work, it was chosen to work at 4% ratio between methane and hydrogen as well as a B/C ratio higher than 10^3 to ensure reaching the metallic transition. All samples presented in this thesis with a pseudo-vertical architecture were grown with the same recipe for the p++ layer which is a 15 minutes, 44 mBar and around 880°C growth. Taking into account all these parameters the average thickness of the p++ layer is about 600 nm. Profilomertry was performed and the average result is presented in figure 2.8, the roughness is about 0.35nm in PSI mode.

In the next section will be presented a new type of growth with different parameters allowing to remove the etching step.

2.2.2.1 Encapsulated growth

One solution to remove the etching problem of the pseudo vertical diode and to continue to use good quality HPHT substrate is to find a way to grow on both sides of the substrate. To do so a new kind of architecture was developed during this thesis. This new structure is presented in figure 2.9 and called the encapsulated diode.

To obtain the p++ growth on both side of the substrate the usual growth process was modified. Normally the diamond substrate is put onto a silicon sample holder in the growth chamber. In that configuration the plasma ball is only wrapping the top surface and the growth occurs only on the top (left part of figure 2.10). To obtain the encapsulated growth a

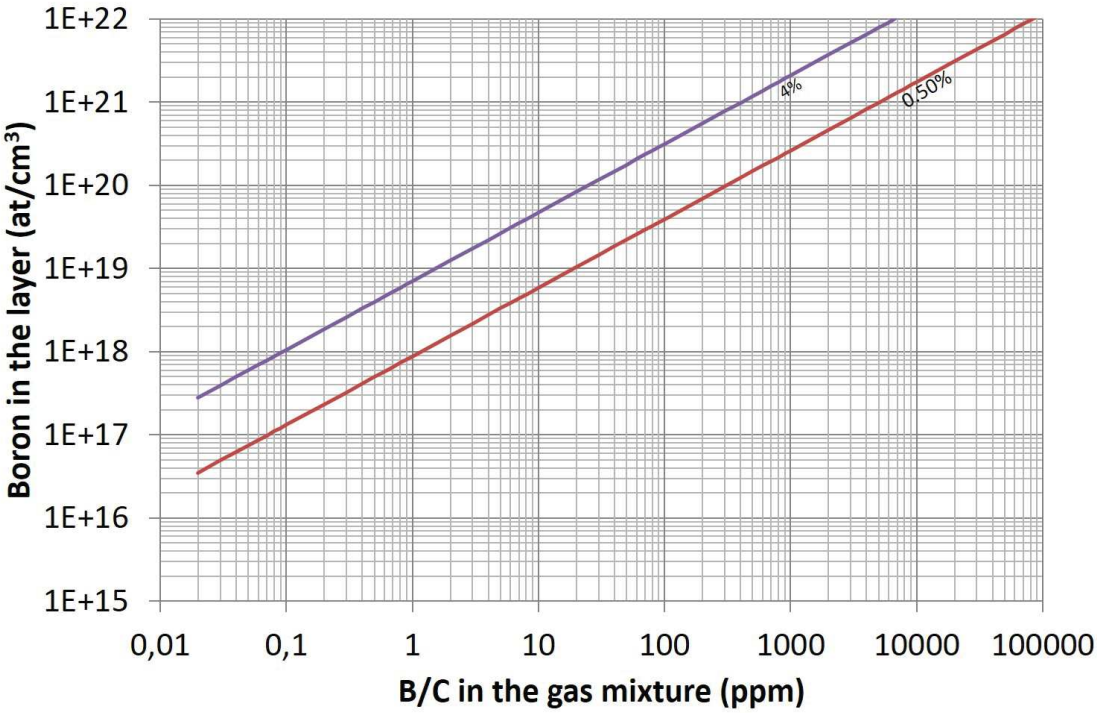

FIGURE 2.7: *Boron incorporation vs. B/C ratio into the gas mixture for different CH_4/H_2 ratio [68]*

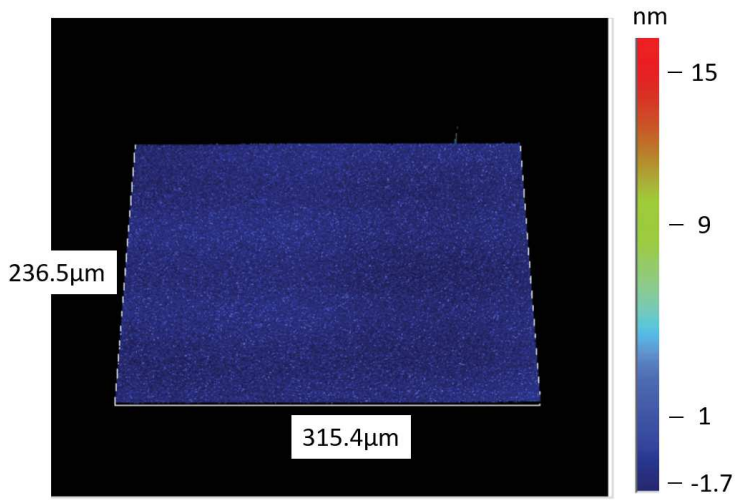

FIGURE 2.8: *p++ surface studying by optical profilometry in PSI mode*

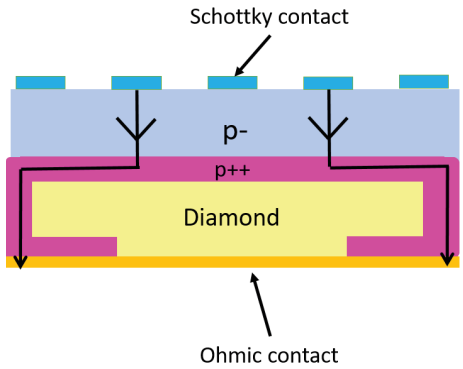

FIGURE 2.9: *The encapsulated architecture*

diamond pillar is added. The diamond substrate is put on the top of it with a rotated angle of 45° with respect to the surface of the diamond pillar that will allow the plasma ball which has a diameter of 2cm to embrace the entire sample. The four corners are free (not protected by the sample holder or the diamond pillar) and can go inside the plasma ball so the growth can occur on all available surface like shown in figure 2.10.

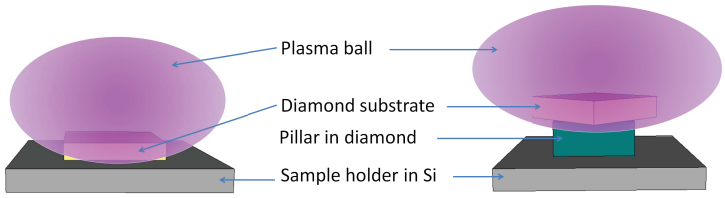

FIGURE 2.10: *On the left side the old sample positioning on the right the new one allowing growth on both side*

To perform such a growing the previous recipe was adapted by playing on different parameters. Ellipsometry was performed and a thickness of 1.9μm was measured.

Optical micrographs of the back side corners are presented in figure 2.11. On each corner it is possible to see some irisations which indicates the presence of diamond growth. To confirm it, electrical measurements were performed to see if there was some conduction continuity between the top surface and the back of the substrate. This sample was glued with silver paste on a alumina plate with metallic contact on it. One probe was put on the alumina metallic pad and the second one a rectangular metallic pad (400x100 μm^2) deposited in Ti/Pt/Au. The results is shown in the I-V curve in figure 2.12.

2.2.3 Non intentionally doped layer

The non intentionally doped layer (NID/p-) are grown in a dedicated reactor. This reactor, a BJ 150, is a bell jar reactor designed by the Laboratoire des Sciences des procédés et des matériaux (LSPM) in collaboration with Plassys. This reactor is presented in figure 2.13. It is composed as well with 2.45 GHz microwave generator which can work from 0 to 6000W. It

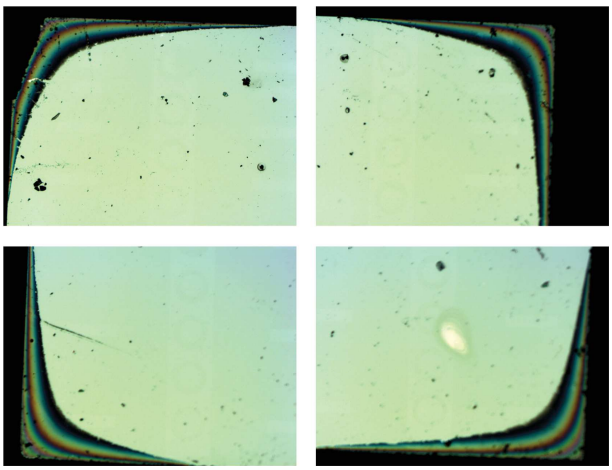

FIGURE 2.11: *4 corners 4*4 sample back optical micrographs, on each corner the presence of irisations indicates p++ growth*

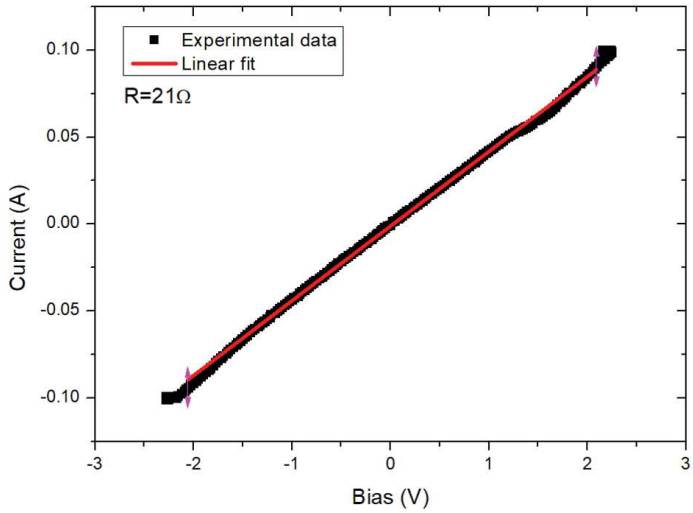

FIGURE 2.12: *p++ I-V measured between a rectangular metallic pad on the top and the back glued with silver paste to see the electrical conductivity*

is also composed with a resonant cavity excited by an antenna allowing the plasma ignition. The working pressure inside the chamber can vary from 0 to 300 mbar. The plasma ball takes place inside the silica bell jar chamber. On this reactor the sample holder is made of molybdenum and can support 2 inches sized wafer. This sample holder is cooled down thank to industrial water flowing.

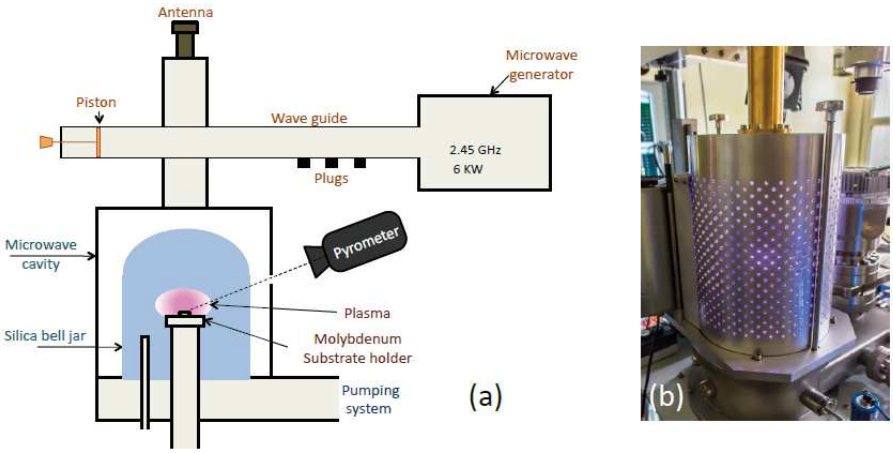

FIGURE 2.13: *Diagram of the Plassys reactor (a) and its picture (b)*

In the case of NID layer grown in this reactor the hydrogen pre-treatment was reduced to 5 min at 150 mbar and 200 sccm to lower the risk of etching the entire p++ underneath due to the high power needed to start the plasma. Growth conditions will depend on the wanted thickness of the layer. In this work, new way of growing NID layer has been developed in order to obtain better quality and thicker film. This method is summarized in figure 2.14. This process is composed of two different phases. Phase 1 where the carbon over hydrogen ratio is stable during t1 and a phase 2 where this ratio is decreasing at a constant rate until reaching 0 and stopped the growth. The idea behind the ratio decrease comes from the fact that at low methane concentration the defects number was smaller as shown by Lloret *et al.* [69]. So reducing the C/H ratio should decrease the defect number on the top of the grown layer. On the other side starting at constant methane concentration allows to grow faster and to obtain a thicker layer. For all samples presented here the decay time was equal to the constant time i.e t1=t2. Further experiments are still needed to be performed in order to find the best ratio between t1 and t2. But the crystalline quality of such grown layer has been checked and will be presented in the next paragraph.

Summary of all growth conditions for each sample used during this thesis will be presented at the end of this chapter 2.1.

2.2.3.1 Transmission Electron Microscopy: crystal quality verification

To check the new growth conditions and see if the crystalline quality was improved, one sample using the same stack that the one for the Schottky diode was grown. In the summary table is refereed as $4\mu m$TEM. In collaboration with the University of Cadiz in Spain, it was

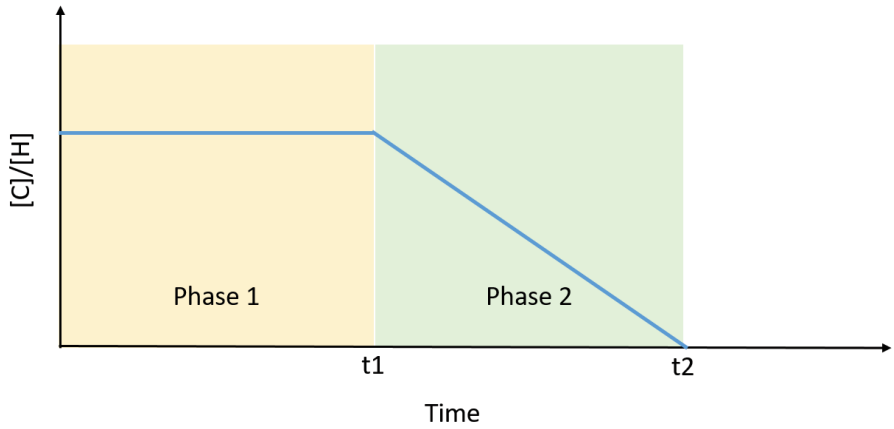

FIGURE 2.14: *[C]/[H] ratio versus time for NID layer growth*

studied by Transmission Electron Microscopy (TEM). To performed TEM some constraints have to be taken into account. The layer thickness is one of them in order to see the full stack (i.e: substrate, p++, p-, metallic contact). In fact for the TEM observation the fabrication of a lamella is needed and it cannot be thicker than 6 μm. So the full thickness of the grown layer should be around 5μm. This sample have p- layer with a thickness of 4.4μm which allows to make a lamella from the entire stack.

The lamella preparation was performed using the focused ion beam (FIB) technique. In that case a gallium FIB was used. The fabricated lamella is shown in figure 2.15, the size is 6 by 12 μm^2 with a thickness of 5nm. On top of the lamella platinum was deposited to protect the lamella process during the FIB etching. It is also possible to see a different contrast between the left and the right part in a), this is due to the lamella different thicknesses. The left part is thinner than the right one, and the two white zones from the left side are even thinner. Thinner is the lamella better resolution will be obtained in TEM. The b) SEM image shows a lateral view of the lamella and picture c) the lamella before being removed from the substrate. At this point of the process the lamella is extracted thank to an omniprobe glued on it with platinum.

After, this lamella was studied by TEM. First scanning TEM (STEM) was done onto the entire stack, the obtained micrograph is shown in the left part of figure 2.16. From this image a lot of information can be extracted. First, on the thicker part of the lamella which is in light grey, the entire stack can be decomposed and all interfaces are visible. From the left to the right: first the substrate with its interface with the p++ layer. After, between the two arrows, the p++ layer, which is delimited by 2 lines. Those two lines are due to the differences of constraints between an heavily doped layer and a lightly doped one. From both side of the p++ layer interfaces are clear, nothing is propagating from one side to other. Inside the p- , grown with the new process explained above, nothing appears meaning that there is no defect. Also the interface with the zirconium is continuous.

High resolution TEM (HRTEM) was also performed to see at the atomic scale the crystalline quality of the layer. One typical result obtained on this sample is shown in figure 2.16

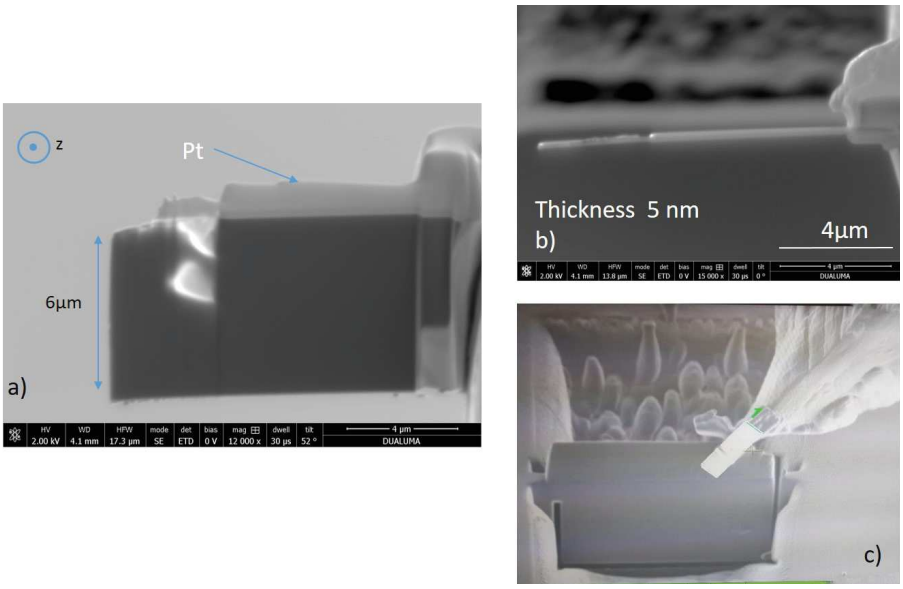

FIGURE 2.15: *SEM images of the lamella preparation for TEM, a) the all lamella, b) the sideview to see the thickness and c) the extraction of the lamella from the sample*

right part. On this image the white line is the interface between the p- and the metal. Below this line is the p- layer with an atomic resolution, each dot is corresponding to a carbon atom in a hexagonal array. To confirm it, a fast Fourier transform (FFT) was done and included in the figure. On this FFT the obtained diffraction pattern is the one expected for crystalline diamond. Above the white line is the metallic layer and it is amorphous.

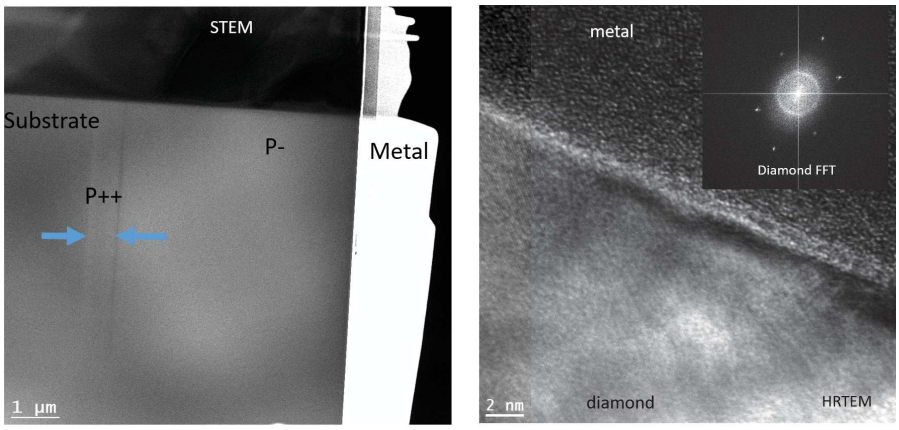

FIGURE 2.16: *on the left STEM image to see interfaces and on the right HRTEM image to check the layer crystalline quality with in inclusion the diamond FFT*

From all this results, the new growing approach is conclusive and seems to go in the good direction in order to obtain thick good quality layer.

2.2.3.2 Selective growth

An other way to removed the etching step is to do selective growth but, up to now, only thin ones have been performed using lithography and lift-off process with Titanium and gold mask [70] or Silicon oxide [71]. To grow thick NID layer, this technique is not doable because the metal mask thickness should be at least three time bigger than the wanted one (i.e 30μm thick Ni mask for 10 μm thick diamond) and could contaminate the growth chamber.

To avoid this issue it has been decided to create an hard mask that can resist to high temperature. So it was decided to use molybdenum which can sustain temperature more than 2000°C. The picture of the designed mask is presented in figure 2.17 and a 3D representation in figure 2.18.

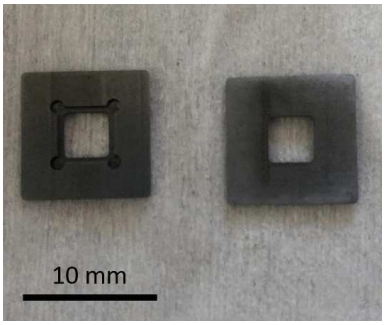

FIGURE 2.17: *Picture of the designed molybdenum mask for selective growth, on the left part the back side and on the right the front side of the mask*

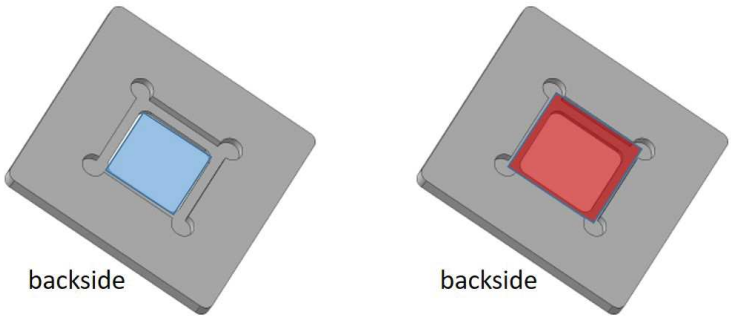

FIGURE 2.18: *Backside 3D representation of the mask used for doing selective growth, in blue the first imprint and in red the second imprint*

To designed the mask a lot of parameters were needed to be taken into account, sample size, available technique and tool to do it... First it was decided to create it for 4 by 4 mm^2 substrate with 400 μm thickness. This mask has a square open window of 35 mm in the middle to allow the growth and to protect 5mm of the diamond substrate on each sides (bleu imprint in figure 2.18). To ensure the good positioning of the mask, on the backside a second print was made (red imprint in figure 2.18). This print is 4 by 4 mm^2 square with Mickey Mouse ears type corner, due to technical fabrication issue with no possibility to do sharp corner. This second print has to be as deep as the sample thickness because if it is too thin the mask will be only on the substrate and not on the sample holder allowing to cool down

the temperature of the mask. In the contrary, if the mask is too thick it will be in contact with the sample holder and no more with the substrate allowing growth everywhere. So at the end, the mask is 600 μm thick with a 400 μm second print.

On a first try the mask was placed directly on the sample and the sample holder. In that situation the mask was not well placed on sample and the mask was too much heated due to bad thermal conduction, temperature was over 2000° C (pyrometer limitation). The result of this first attempt was a growth below the mask and lot of defects on the grown surface.

A second try was done with the mask in a better position to reduce the growth underneath it. This growth followed the same protocol than presented before, for 24 hours. The results is shown in figure 2.19, on the right part picture of the growth of a clear mesa structure in the sample middle. To check the height of the mesa structure optical profilometry was performed (left part of the figure), this allows to measure the step's height about 12μm. Ellipsometry revealed a 10.7μm thickness on the middle of the sample.

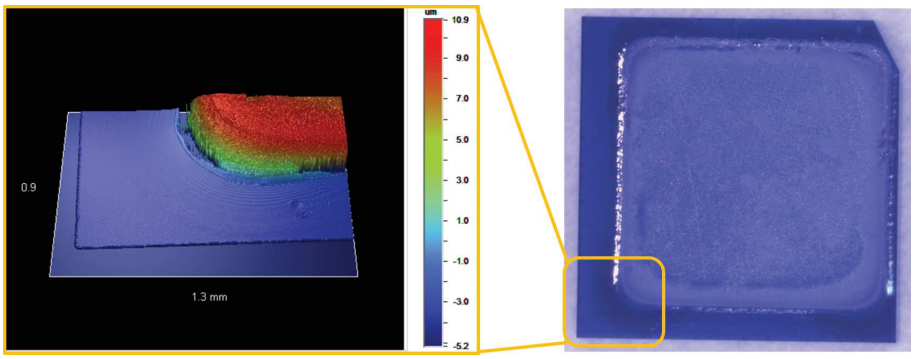

FIGURE 2.19: *On the right the picture of the selectively grown sample and on the left part an optical profilometry image of the delimited orange area on the picture.*

On both picture and profilometry it is possible to see the bad quality of the grown mesa upper surface. This is probably induced by the utilization of the hard mask.

New sample holder

Even before trying selective growth the sample positioning was not reproducible from one growth to the other and some temperature variations between two growths were noticed. Those problems were even bigger with the use of the hard mask. So a new sample holder was needed to continue to improve the growth condition and to win in reproducibility. This new sample holder has to answer some criteria, allowing to have the same positioning of the sample for every growth in the reaction chamber, permitting to deposit the hard mask without risking to misplaced it on the sample and to have a better temperature control of the sample. On figure 2.20 on the left the old sample holder picture and on the right the new one.

This new sample holder is based on the old one but three imprints with different thickness and different positions have been made. Like for the mask presented above, one of the

key parameter to define the imprint thickness is the substrate thickness to allow the sample positioning into the imprint and putting the mask in top of it. For those reasons it was decided to use two different thicknesses with 100μm depth in the middle and on the side and one on the side with 50μm depth for the imprint. The space between each imprint is 8 mm, allowing to grow two samples with the hard mask at the same time. And free space can be used for bigger size substrate. In most cases no over-mask was used during growth and the 100μm imprint is used.

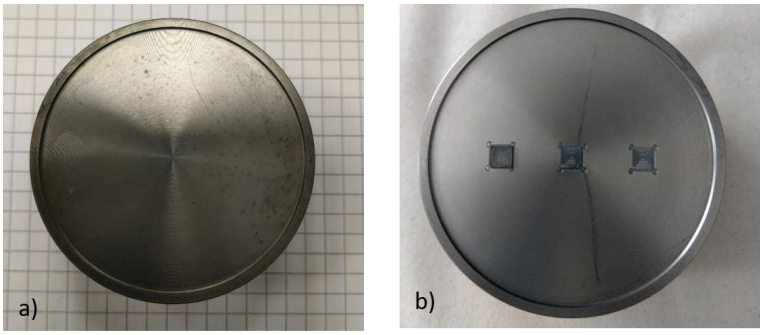

FIGURE 2.20: *a) photo of the previous sample holder and b) photo of the new sample holder*

2.3 Devices fabrication

After the growth of the two layers by the usual way or by new ones samples were processed in order to obtain functional diamond Schottky diodes. In this section the general process will be presented and some particularities would be treated in the needed section depending of the sample specificities. The main process can be separated within 3 main steps which correspond to a total of 27 steps:

1. Etching of the p- layer
2. Ohmic contact realization
3. Schottky contact realization

All these steps have been realized into two facilities which are Institut Néel clean room NANOFAB for the main part and the clean room of the Plateforme Technology Amount (PTA) for the etching part.

2.3.1 Problematic and solution for diamond device fabrication

As a difference with other materials where the equipment is adapted to the sample size for diamond device fabrication everything has to be adapted and solution have to be found in order to use available equipment in the laboratory.

One of the biggest issue is due to the sample small size coupled with the envy to put as many devices as possible on the sample like for silicon. This conduct us to use the sample's

edges. Nevertheless one of the recurrent steps in microelectronics is lithography and in the same time resist coating. In silicon industry mask design takes into account the edge effect on the resist spin-coating (i.e resist thicker at the edge) and one doesn't put devices there or put them on knowing that will not go out of fabrication process but the of number devices available elsewhere on the substrate is enough. For diamond with the current 4 by 4 mm^2 size the resist spin coating is challenging due to this edge effect (i.e all the sample is an edge effect). To reduce this phenomena different ways are possible, increasing the spin-coater speed rotation and the acceleration from the traditional one and/or switch the sample holder. During this thesis lot of samples were fabricated and the best way to decrease as much as possible the edge effect was to switch from the regular sample holder to an home made sample holder from NANOFAB (fig. 2.21). In this sample holder the resist excess can be evacuated from the diamond more easily thank to the holder shape, the sample is at the same height than the holder. Most of all this work was done using a UV sensitive resist Shipley S1805 with a 500 nm thickness expected and annealed for 1 minute at 115°C.

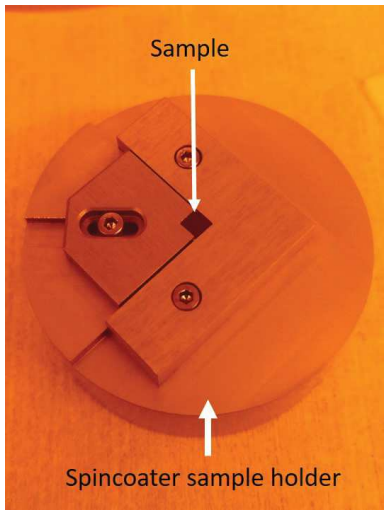

FIGURE 2.21: *Home made Nanofab sample holder for small sample spin-coating picture*

Laser lithography DWL66FS from Heidelberg was used in this thesis. With this technique the edge effect is decreased enough for regular lithography in the middle of the sample with the standard dose which will not deform the wanted design. If edge lithography is required for Ohmic contact definition the solution found was to launch the lithography four times in a raw without removing the sample the ensure the good alignment and increase the insulation dose. If the design is big enough the over-exposition of the resist will not impact the contact shape.

After, the development a smooth O_2 plasma etching was performed by reactive ion etching (RIE) at 20W to ensure the removing of all the resist inside the lithography spot.

Before all of this, the mask for the different steps has to be designed thanks to Klayout software providing a ".gds" file directly compatible with the laser lithography. To do a

proper mask design some parameters have to be taken into account. First the problem mentioned above, the edge effect if the structure is closed to the edge: can I increase the dose and over-expose without risking to damage it? Also the laser lithography resolution to ensure to have a good and clean lift-off after deposition. The possibility to align easily each layer from the entire design one with the other (i.e alignment cross well designed, well placed). One mask design example developed during this thesis is presented in figure 2.22. On this mask the crosses are for the ohmic contact and the round one are for Schottky contacts.

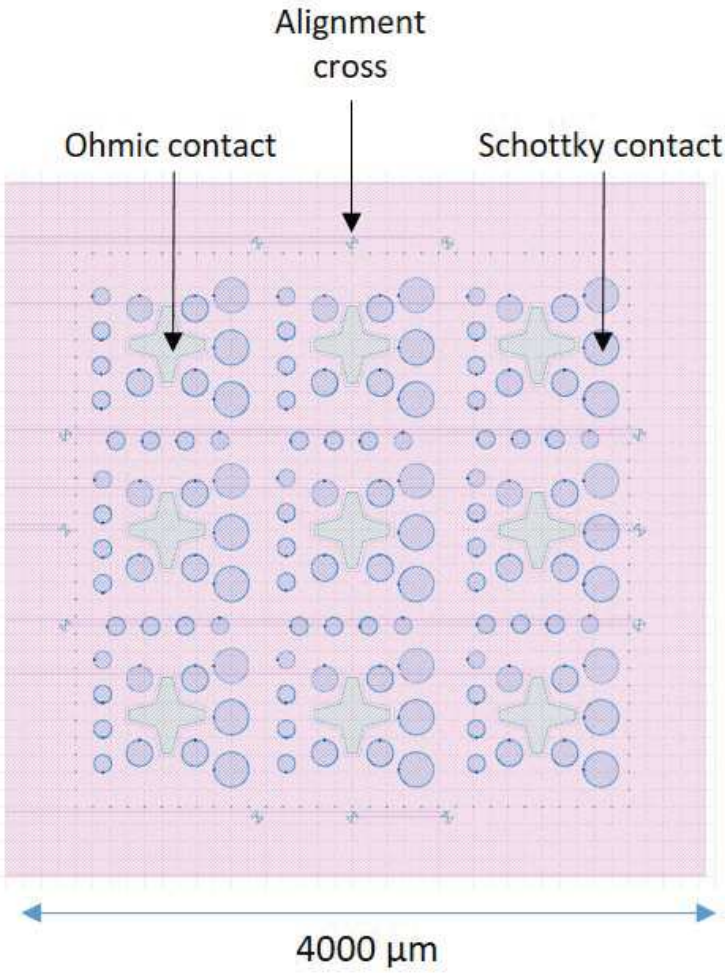

FIGURE 2.22: *Mask design example realized during this work, crosses are Ohmic contact and round contacts are Schottky contacts*

2.3.2 Etching of the p- layer

The purpose of this step is to etch the entire p- layer in some part of the sample to be able after all to deposit the ohmic contact on top of the p++ layer.

The etching process is summarized in figure 2.23. It starts with the deposition of the hard mask. The mask was done by laser lithography and a titanium/aluminum mask with a 5 and 200 nm thickness respectively deposited by electron beam evaporation and lift-off.

In that case Ti is used as a sticking layer for Al deposition, Al has been chosen because its etching rate under this plasma condition are way much lower and will protect the diamond enough time to do the etching.

Etching was performed by inductively coupled plasma etching (ICP), in a DEEP RIE SPTS (SPX HRM 180) equipment. This technique allows to have an independent control of the plasma density and reactive ion energy onto the etched surface. Two radio frequencies (RF) are involved, the first one by inductive coupling through the dielectric wall of the chamber allows plasma ignition and control of its density. The second one which will define the etching rate and its anisotropy because it is sourcing the sample holder by capacitive coupling and that will attract the positive ions toward the etched surface and defines their kinetics energy. There are two keys parameters: the substrate holder power and the coil power. Depending of the first one if the power is low the etching will be smooth by chemical reaction and if it is high the etching rate will be quicker but anisotropic due to sputtering mechanism. The second is here to promote the high densities of reactive species.

The recipe uses a pure oxygen plasma with 1000W coil power and a 40W holder power. The gas flow was settled at 100 sccm and the pressure at 10 mTorr. The etching rate is about 51 nm per minute.

When etching was performed the hard mask was removed by using hot Aqua Regia mixture ($3HNO_3 : 1HCl$ ratio).

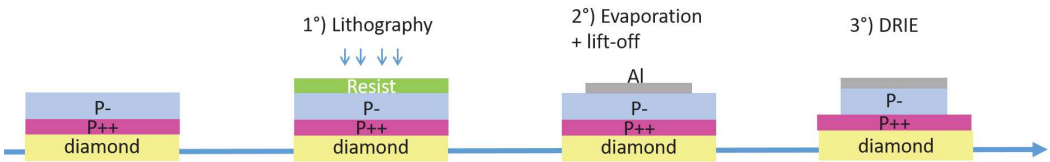

FIGURE 2.23: *Recap of the etching step process*

2.3.3 Ohmic contact realization

Ohmic contacts are also defined by laser lithography, using the same resist than before. The deposited metal in that case is a stack of titanium (30 nm), platinum (50 nm) and gold (40 nm). Each metal of this stacks has an interest, titanium is here to form a titanium carbide at the interface with the diamond, platinum is here to avoid the gold diffusion, an gold is chosen for its good conductivity ($45.2 * 10^6\ S.m^{-1}$), stainless and stable characteristics. This step is summarized in figure 2.24.

2.3.4 Schottky contact realization

Before defining the Schottky contact an ozone treatment was performed, in order to obtain oxygen terminated diamond. To do so, it was demonstrated by Teraji *et al.* [72] than performing a deep UV ozone treatment gives a better result than the use of chemical oxidation due to an easier control, a better reproducibility and a better homogeneity. The treatment

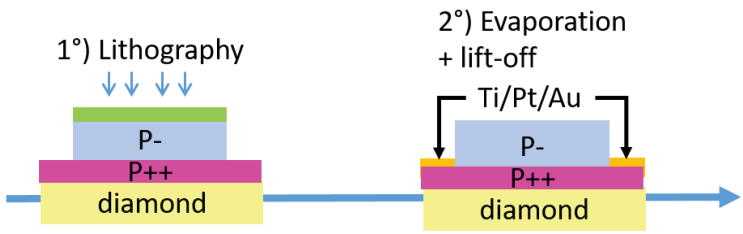

FIGURE 2.24: *Recap of the ohmic step process*

was performed during 2 hours under a pressure of 500 mBar. The ozone plasma ignition was done thanks to a Xenon EXCIMER lamp centered at 172 nm.

Same lithography process than before was performed and a second ozone treatment was done to ensure the good oxygenation of the surface after the smooth RIE etching described before.

For the Schottky contact as demonstrated by Aboulaye TRAORE during his thesis [53] Zirconium (20nm) , platinum (30 nm) and gold (10nm) were deposited by e-gun evaporation under high vacuum.

After all of these steps sample was annealed at 450°C for one hour under vacuum (around 10^{-7} mbar). The introduction in the oven occur only after thermalization at the wanted temperature.

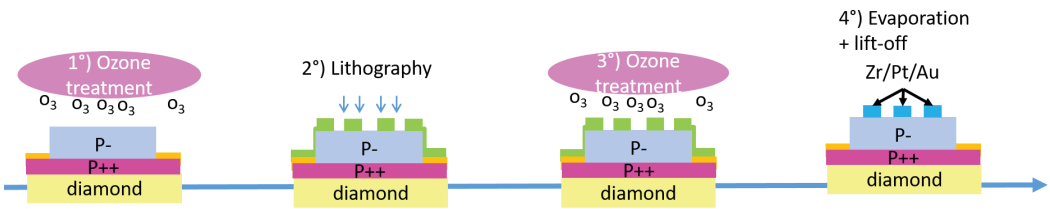

FIGURE 2.25: *Recap of the Schottky step process*

Electron beam lithography

By looking closer at the mask presented in figure 2.22, it possible to see around Schottky contact a ring. This ring was designed to create floating metal ring in order to decrease the electric field. Nevertheless, for working the ring has to be very close to the Schottky contact (less than 1μm) and quite thin. Inner contacts were 100, 150 and 200 μm diameter. The spacing between the ring and the contact were 150, 300 and 500nm for 2 μm ring width. (fig.2.26)

As said previously the laser lithography resolution is not good enough so a new lithography process have to be developed. This technique is called electron beam lithography where electrons are used instead of photon for the resist insulation. The resolution is now around 10nm. Numerous number of attempt have been tried in order to find the good process (i.e dose, resist,..). At the end, it was chosen to use a PMMA 4% resit deposited with the same sample holder and baked during 5 minutes at 180°C. Several doses test have been run

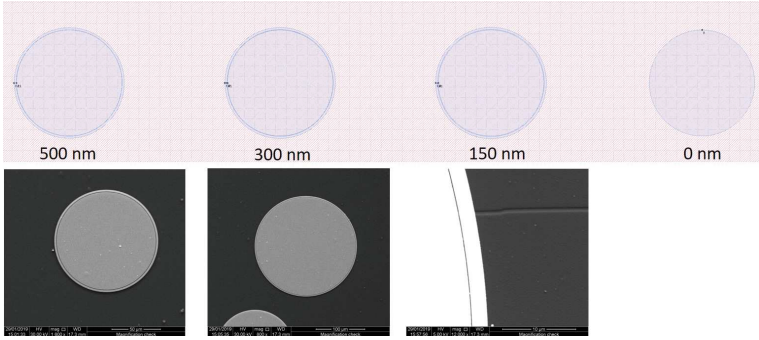

FIGURE 2.26: *Zoom on some Schottky contact from the mask design and SEM picture after lift-off process*

in order to find the good one, which vary from one sample to the other due to the insulating substrate creating charging effect. Unfortunately this sample was not electrically measure due to restriction time.

2.4 Summary of grown and fabricated samples

During this thesis more than hundred of growth have been performed in order to test different parameters. Only some of them will be presented in this thesis. In this section a summary will be done, to clarify the growth condition, the goal of each sample that will be explained into the next chapters.

Nine samples have an interest for this thesis which represent 15 growths, all of the growth key parameters are summarized in table 2.1.

TABLE 2.1: *Summary of grown samples with their growth conditions, thickness measured by ellipsometry and doping level. In yellow the p- and p grown on the home made reactor and in orange p- grown on the Plassys BJ 150*

Sample name	Substrate	Growth condition											Objectives
		layer	Power (W)	Temp (°C)	Pressure (mBar)	CH4/H2	02/H2	B/C (ppm)	Total flow (sccm)	Time (min)	Thickness (nm)	Doping level (atom.cm^{-3})	
20µm	NDT (100)	p++	260	880	43.89	4%	-	1200	113	15	612	$> 10^{20}$	Thick NID layer and elctric field study
		p-	2500		150	4.20%	-	-	198	1440	19900	$4x10^{14}$	
10µm_selective	NDT (100)	p++	260	840	43.89	4%	-	1200	113	15	≈ 600	$> 10^{20}$	thick selective growth
		p-	2500		150	4.20%	-	-	198	1440	10760	$<10^{15}$	
5µm_encap	NDT (100)	p++	240	860	33.25	4%	-	1200	113	30	1616	$> 10^{20}$	Encapsulated growth
		p-	2500		150	4.20%	-	-	198	240	5190	$4x10^{14}$	
2µm_encap	NDT (100)	p++	240	860	33.25	4%	-	1200	113	30	1947	$> 10^{20}$	Encapsulated growth
		p-	2500		150	4.20%	-	-	198	480	2000	$4x10^{14}$	
10µm_etched	NDT (100)	p++	260	880	43.89	4%	-	1200	113	15	≈ 600	$> 10^{20}$	deep etching by UCL
		p-	2500		150	4.20%		-	198	720	10400	$<10^{15}$	
4µm_TEM	NDT (100)	p++	260	880	43.89	4%	-	1200	113	15	≈ 600	$> 10^{20}$	TEM Cadiz
		p-	2500		150	4.20%	-	-	198	240	4480	$<10^{15}$	
HVDC1	NDT (100)	p++	260	870	43.89	4%	-	1200	113	15	598	$> 10^{20}$	increase of current
		p-	260	880	150	0.75%	0.25%	-	202	150	1614	$5.28x10^{14}$	
HVDC2	NDT (100)	p++	260	880	43.89	4%	-	1200	113	15	535	$> 10^{20}$	isolated cell
		p-	260	880	43.89	0.75%	0.25%	-	202	150	1880	$5x10^{15}$	
hetéro1	Diamwafel consortium	p	270	910	43.89	1%	0.25%	60	104.25	120	1600	$1x10^{16}$	heteroepitaxial diodes fabrication

Chapter 3

Current increase and diode integration

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Once a sample is fabricated, it needs to be characterized. This chapter will propose to look at diodes parallelization in order to work on increasing the ON state current and planning the future with the diamond component integration. We will go from the component design to the characterization of the final device taking into account what was already reported in the literature. We will finish with a diamond Schottky integration inside a simple power rectifier: a diode bridge.

3.1 How to increase the current?

In order to be efficient and useful to the power device community the device ON state is important, it must express the smallest $R_{on}S$ with the lowest threshold voltage in order to flow the maximum current at the lowest voltage as possible. With the current diamond Schottky diode the available current is around 0.1A at 10V. Working on the improvement of the ON state could be obtained by the different options proposed below. The first one will be to work directly on the properties of the diamond layer by increasing the active layer doping level but this will act on the reverse characteristic by increasing reverse leakage current. An other solution will be to increase the p++ thickness which will increase the risk to have defects coming from the p++ growth and after spreading into the p- active layer. The second way, is to play on the component design itself. Different parameters can be modified, the easiest one is to increase the Schottky contact size but that will extend the chance to have killer defects underneath it and decrease the blocking capabilities of the device.

As said before one way to raise current flowing into the device is to increase the contact area. In the industry one important parameter is the number of working devices per entire sample. This Yield number is dependant of defects density as well as the contact area. It can be calculated using the Poisson's equation [73]:

$$Y = e^{-NDA} \tag{3.1}$$

In this formula, D is the defect density (defect/cm^2), A the contact area (cm^2) and N the number of masks used to obtain contact, in the case of Schottky contact N=1.

In figure 3.1 are plotted different working device yields in function of the Schottky contact area for different defects density. On this graph the yield of working device is decreasing with the the increase of the defects density. To ensure a good yield number when the defect density is increasing the contact area should decrease. For diamond device considering that defect density is more than 1000 defects per cm^2 meaning that for having half of device working contact area should be less than 7.10^{-4} cm^2 which correspond to round contact with a 300 μm diameter or a square contact with a 264 μm side size.

The other parameter that can be changed in order to raise the current flowing is to decrease the distance between the ohmic and the Schottky contact.

The last way to increase the current is to put several diodes in parallel. This can happen by using diodes from the same die or from different dies. In this chapter both proposal will be studied: an architecture change with a new design drawing and diodes parallelization.

3.2 Common anode problematic

The current architecture used in the lab is a pseudo-vertical one presented in figure 3.2. This architecture is composed with only one ohmic contact acting like a common anode to all diodes.

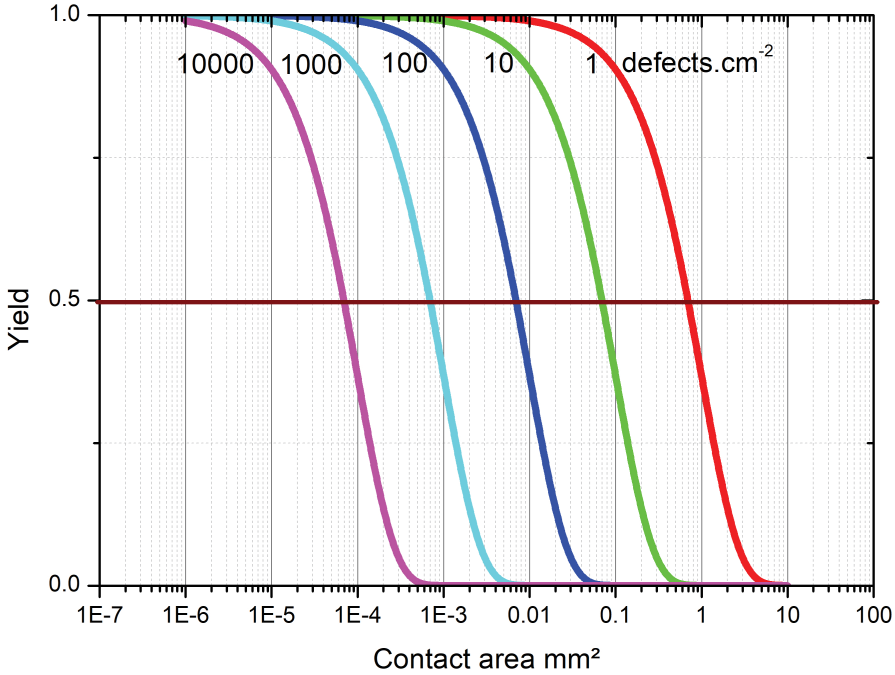


FIGURE 3.1: *Working device yield in function of the contact surface area for different defects density*

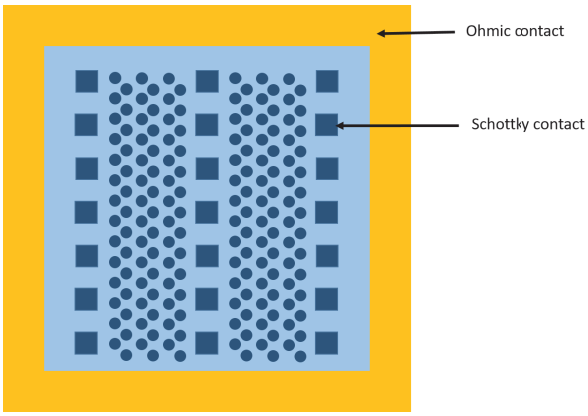
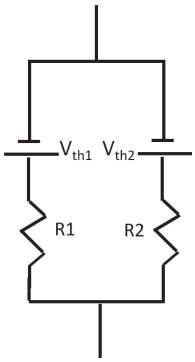


FIGURE 3.2: *Previous architecture schematic top view with only one ohmic contact for all diodes*

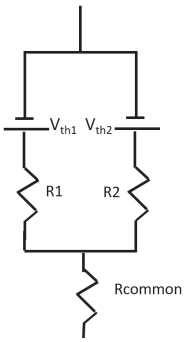
From the work done by Gaetan PEREZ during this thesis [74, 75] he showed that if two diodes were put in parallel the obtain results was not the one expected from the theory. Normally by looking at the equivalent circuit presented in figure 3.4 which is composed with a resistance representing the ohmic part of the diode (R_1 and R_2) before each resistance voltage source is added in order to represent the diode threshold voltage they are named V_{th1} and V_{th2}. The sum of two diodes is given by equation 3.2. In that case if both diodes exhibit the same current behavior limited by the same resistance (i.e $R_1 = R_2$) and with the same barrier height the resulting resistance should be divided by 2 allowing to have a diode with a higher current.



$$\frac{1}{R_1//R_2} = \frac{1}{R_1} + \frac{1}{R_2} \quad (3.2)$$

FIGURE 3.3: *Equivalent circuit for two diodes in parallel with two different V_{th1} and V_{th2} and its equivalent formula*

Results of this study shows that the resulting resistance was lower than the one obtain theoretically by parallelization and highlighted the presence of a common resistance. A new equivalent circuit have been presented with its equivalent equation in figure 3.3.



$$R_{total} = \frac{R_1 * R_2}{R_1 + R_2} + R_{common} \quad (3.3)$$

FIGURE 3.4: *Equivalent circuit for two diodes in parallel with two different V_{th1} and V_{th2} and its equivalent formula including the common resistance*

Some simulations have been run by Aurélien Maréchal to have a better understanding of the phenomena. Simulations were based on the model developed previously [76, 77] for TCAD simulation. Those simulations have been run for a device having the same thickness than the real one but the total surface was reduced to $50 * 50\mu m^2$ to allow the simulation to converge. Some results are presented in figure 3.5. On the right part of the figure electrical

measurements show that when two diodes K1 and K2 are put in parallel (K1//K2) the obtained current is lower than the one calculated with formula 3.2 (K1+K2). On the left side, the device simulation highlighted the common path issue. The distribution current path is identical for both diodes inside the p++ layer laterally and are independent one from the other inside the p-. To avoid this, some solutions have been proposed thanks to simulation. The first one is to increase the p++ thickness from 500nm to several micron but with this option there is an higher risk of growing a bad quality layer. The second one will be presented in the next section.

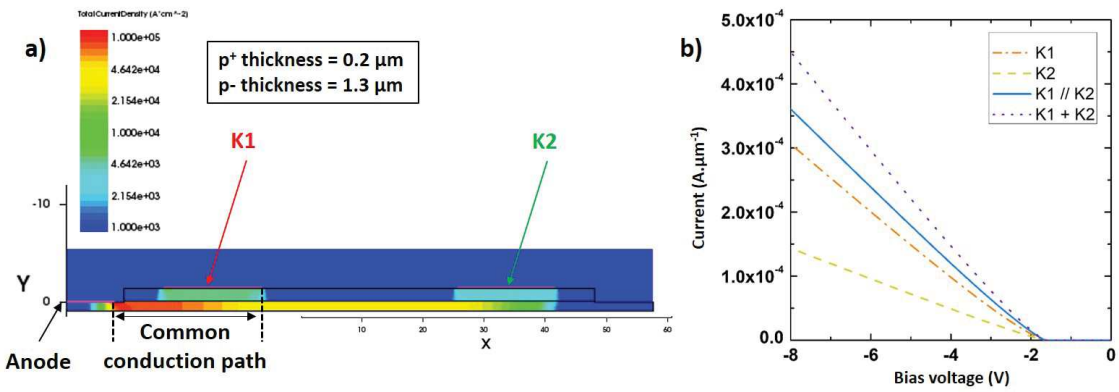


FIGURE 3.5: *Previous results obtain by G. Perez et al. [75], in a) the simulation highlighting the common path and b) the experimental results (courtesy of G2Elab, Grenoble)*

3.3 Diamond isolated island diode

3.3.1 Component design

In order to remove the common anode issue another design for pseudo-vertical Schottky diode must be proposed. For this new design this work offered to used the diamond insulating property and to create separated anodes by etching trenches. Trenches roles will be to electrically isolate one island from the other thanks to the insulating substrate and by cutting the common current path by etching all epilayers from the top to the substrate. Moreover diamond has a very good thermal conductivity so by introducing trenches the thermal conductivity between cells is not damaged. This property can be used after all to have a thermal control of the device. Using a Schottky diodes as a thermosensitive parameter. It is possible due to the hole mobility temperature dependence ([78]).

Also another condition which must be respected is to have all Schottky contacts at the same distance from the ohmic one. To do so, the mask presented in figure 3.7 was designed. It is composed of 16 islands separated with 100μm large trenches. Each island has an ohmic contact in the middle, four 200μm large square Schottky contacts and 8 round ones with a 100 μm diameter. With this design every Schottky contact is separated of its ohmic contact

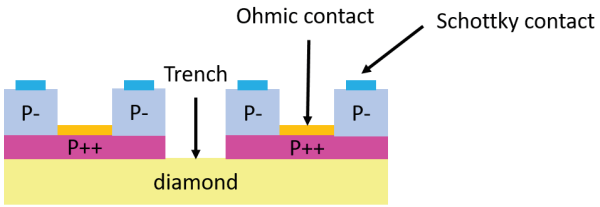


FIGURE 3.6: *New architecture schematic side view*

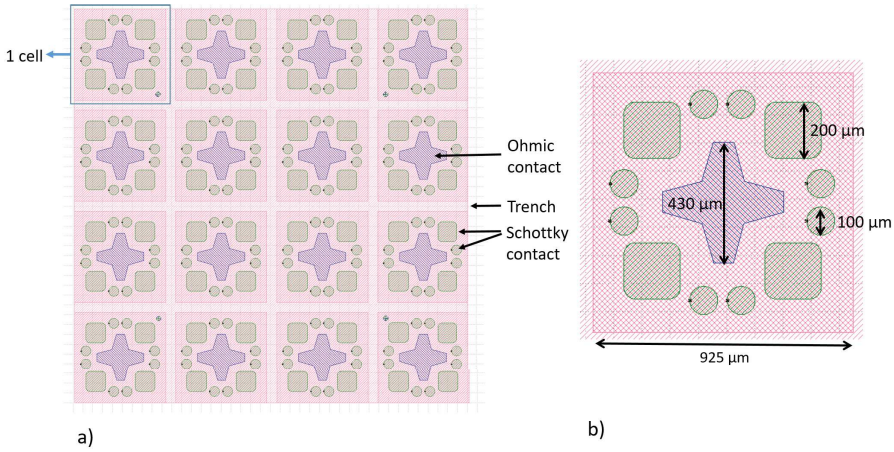


FIGURE 3.7: *New design mask with insulating cells one with the other, in blue ohmic contacts and green Schottky contacts the process used for fabrication is adapted from chapter 2, a) the full design and b) zoom on one cell*

from less than 100 μm. This architecture will allows us to measure Schottky diode with the ohmic contact closest to the Schottky ones.

From the original process used and presented in section 2.3 of chapter 2 an etching step is added just after the p- layer growth. The etching process is the same that the p- one (section 2.23) but deeper. Adding an etching step also brings some new challenges. One of them is the etching depth. To avoid this it was decided to grow about 2 μm thick very slightly doped layer. Two samples have been fabricated with this design. Growth conditions, doping and thickness for both samples are reported in the summary table 2.1 and refereed as HVDC1 and HVDC2. Each of them has been annealed at 450°C for 1 hour under vacuum. In figure 3.8 HVDC1 fabricated device picture is presented. It shows that the four cells located at the corners are not well defined. Also it seems that all trenches do not have the same depth and can create some trouble for the island insulation. That can be explained due to the difficulty to have a resist deposition thin and homogeneous on the edge of the substrate.

Electrical insulation between each cell has to be tested for HVDC1. In this order I-V measurements were performed between two different ohmic contacts. Results are presented in figure 3.9. On this graph it is clear that each cell is not insulated one from the other. This can be explained thanks to profilometry. In fact the trenches etching is not deep enough at certain points and p++ layer is still in place allowing conduction between the cell.

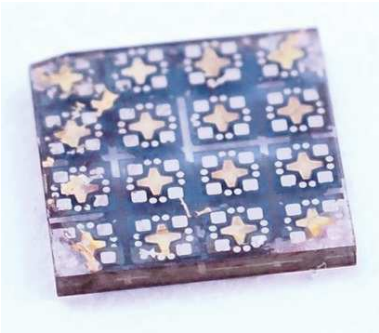


FIGURE 3.8: *HVDC1 device picture after full processing.*

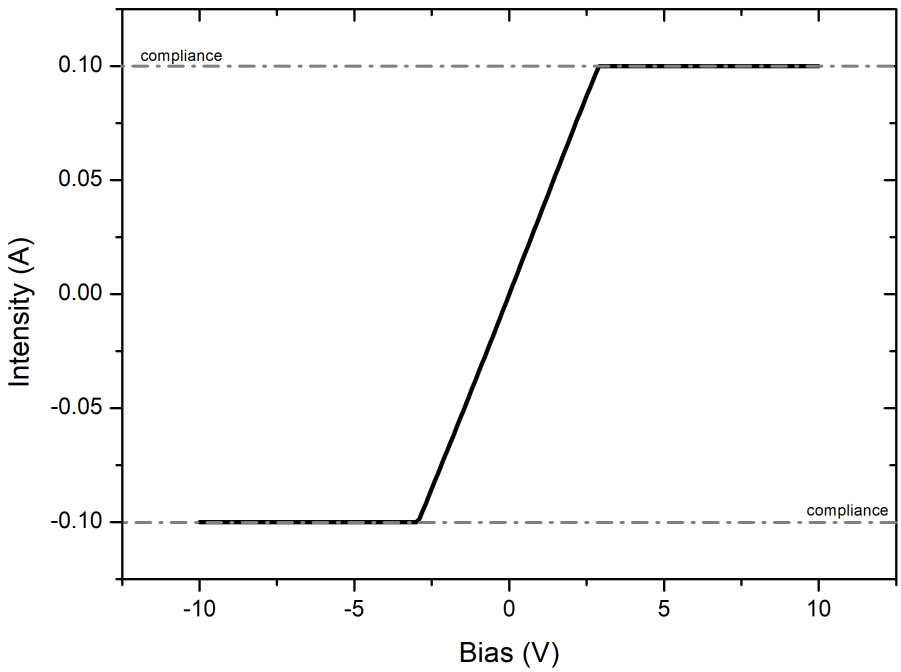


FIGURE 3.9: *I-V between the two ohmic contacts from the two different cells in HVDC1 sample*

3.3.2 Characterization

After devices fabrication, they have to be characterized. In this order, intensity-voltage measurements (I-V) have been performed as well as capacitance-voltage (C-V) ones. Those measurements have been performed inside the Institut Néel home made probe station presented in figure 3.10. On the top there is a glass window in order to visualize the sample thanks to a Leica M205C binocular. The binocular is linked to computer allowing to take device pictures and have a good look of the contact for probes deposition. Four tungsten probes are available inside and piloted thanks to piezoelectric manipulators. Piezoelectric manipulator authorized to work under vacuum and to make some nanometric displacements in the three directions (x, y and z). With this, the contact between the tip and the contact is very soft and permits to preserve the contact integrity. Inside the box a 2 cm diameter sample holder is placed. This sample holder is connected to a Linkam LNP 95 allowing to have a temperature control thanks to PT100 resistance inside the sample holder. This versatile equipment allows to work at different conditions, from 77K to 900K and under vacuum at less than 10^{-3} mbar. Moreover a several number of source measure unit (SMU) can be added in order to perform different electrical measurements like high resolution in current or high voltage measurements. It is also possible to performed capacitance - voltage measurement with a Modulab MTS working in different configurations.

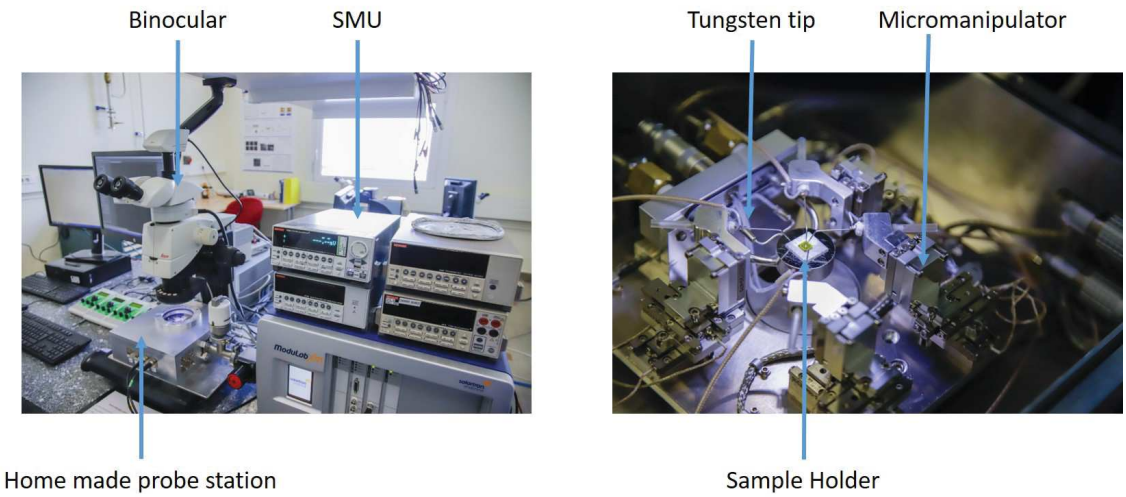


FIGURE 3.10: *Home made Institut Néel probe station picture (copyright Institut Néel)*

3.3.2.1 I-V

I-V have been performed under vacuum at room temperature with a Keithley 2612. For each samples HVDC1 and HVDC2 all diodes presented on figure 3.7 and which came out well defined from fabrication process have been measured between -10 and 10V. Some of those results are presented in figure 3.11. From this graph the serial resistance as well as the Schottky barrier height is not equal from one diode to the other. The serial resistance

is included between 105 and 30000 Ω. For the Schottky barrier the value is between 1.05 and 1.51 eV with an ideality factor superior at 2. All of these data are extracted using the formulas 1.24 and 1.25.

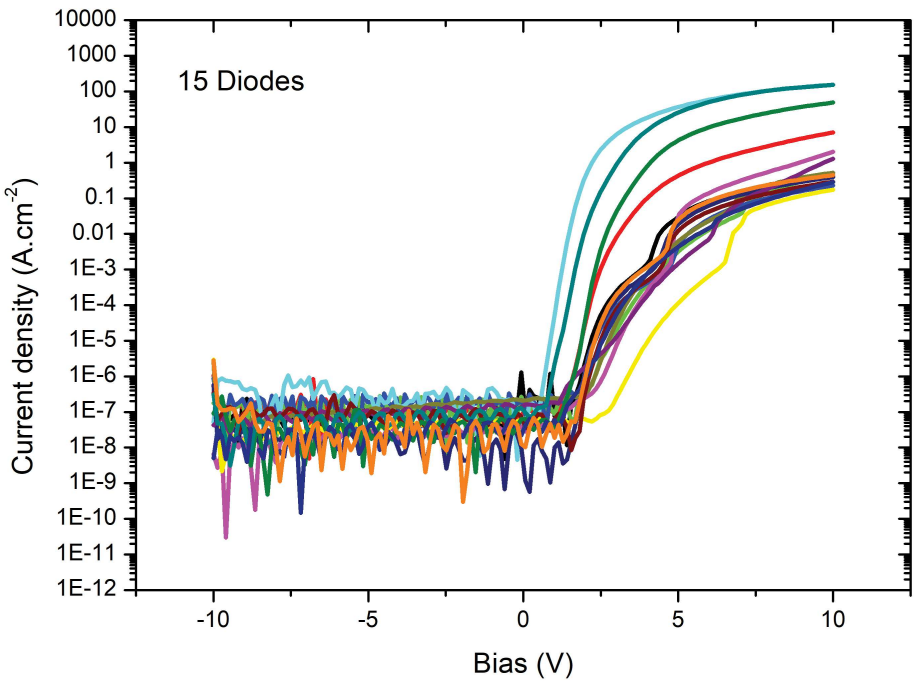


FIGURE 3.11: *HVDC1 sample J-V characteristic for 15 diodes*

Some reverse measurements have also been performed at low temperature at G2ELab on HVDC1, like the forward current the devices blocking capabilities are inhomogenous and can vary from less than 50V to more than 250V as shown on figure 3.12. From this measurement it seems that breakdown is due to avalanche.

3.3.2.2 C-V

On HVDC1, capacitance measurement was also performed to determine the p- layer effective doping level. This measurement was performed and the obtained results are presented in figure 3.13. This graph does not look like the usual $1/C^2$ curve as presented in chapter 1 which is the case in non punch through condition. In the HVDC1 graph, it appears that the diode is in punch through condition because the layer is directly fully depleted. From this measurement, the $1/C^2$ curve in function of the bias (fig. 3.13) the extracted doping level was $5.28 * 10^{14} atom.cm^{-3}$ thanks to the linear fit. The depletion width can be calculated with the formula:

$$w = \sqrt{\frac{2\epsilon_0 \epsilon_r V}{q(N_a - N_d)}} \tag{3.4}$$

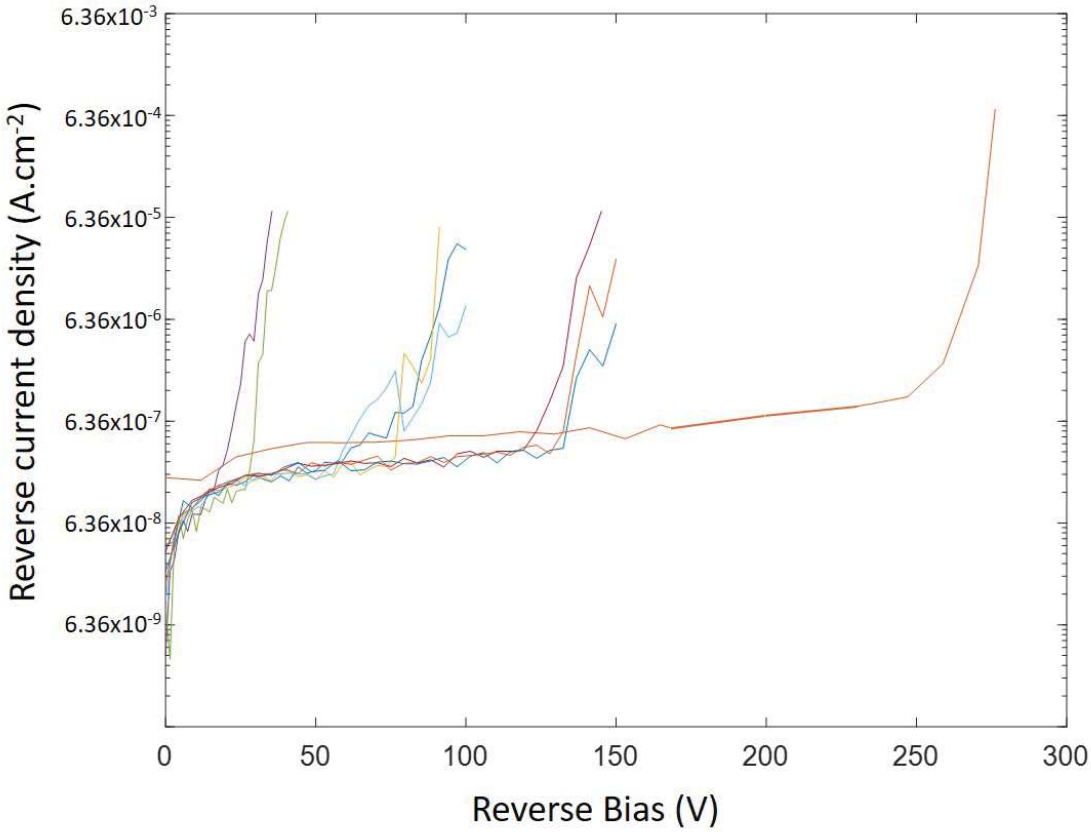


FIGURE 3.12: *HVDC1 sample J-V reverse characteristic for 9 diodes (courtesy of G2Elab, Grenoble)*

where q is elementary charge (C), ϵ_0 and ϵ_r are respectively the vacuum permittivity and the diamond one. V the bias and $N_a - N_d$. In HVDC1 case the p- layer thickness is 1.6 μm measured by ellipsometry and the extracted doping level $5.28 * 10^{14} atom.cm^{-3}$, by applying the formula above (eq. 3.4) at 2V already 1.5 μm are depleted. This explain the punch-through condition of this device, the electric field propagation is directly stopped on the p++ layer as presented in chapter 1. The extremely low doping level can be explained by the growth condition. This low doping level is part of the explanation about the sample high resistance behavior observed before.

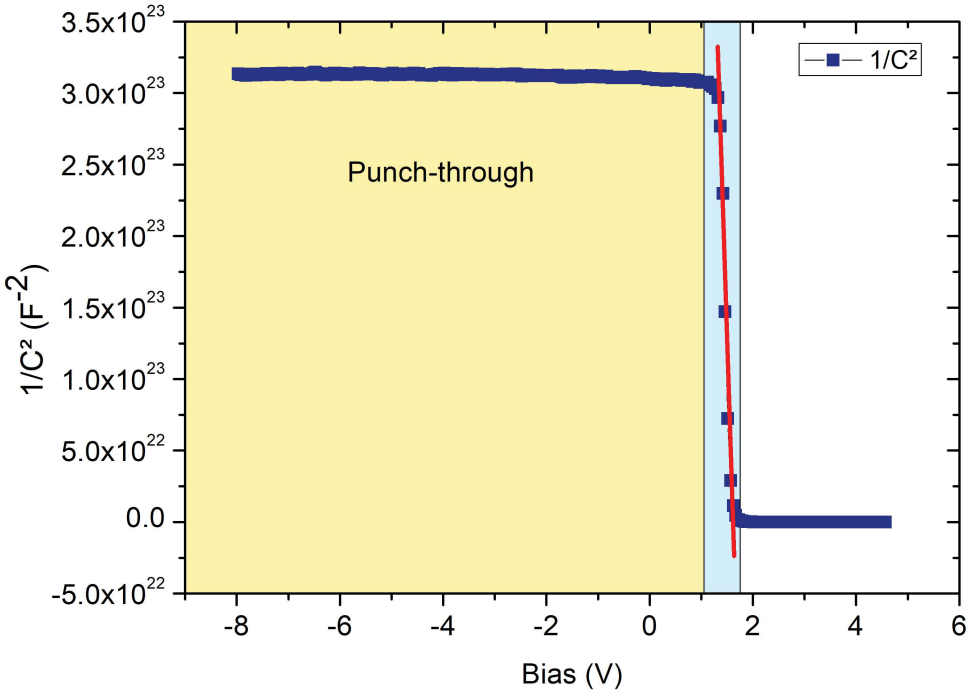


FIGURE 3.13: *HVDC1 $1/C^2$ vs. bias, the diode is in punch-through condition and extracted doping level* $5.28 * 10^{14} atom.cm^{-3}$

Now, that diodes on HVDC1 have been characterized individually. Let's have a look about diodes parallelization in the next section.

3.4 Diodes parallelization

In order to increase the current, two types of parallelization have been tested. The first one with two diodes from different cells and the second one with two diodes from the same cell. Both will be explained with more details in the next sections.

3.4.1 Diodes parallelization from two different cells

The parallelization has been performed with the following process. Firstly both diodes used have been characterized independently one from the other and will be refereed as Schottky 3 and Schottky 4. In that case as shown on figure 3.14 each diode has its own ohmic contact, for this type of setup four probes are needed. In this configuration, the two diodes are refereed as Schottky 3 and Schottky 4. Both diodes characteristics are presented in figure 3.15 Schottky 3 with the black curve and Schottky 4 in red. For the parallelization the resulting current is presented in blue on the same graph. It can be noticed a current increase in the forward regime for the parallelization.

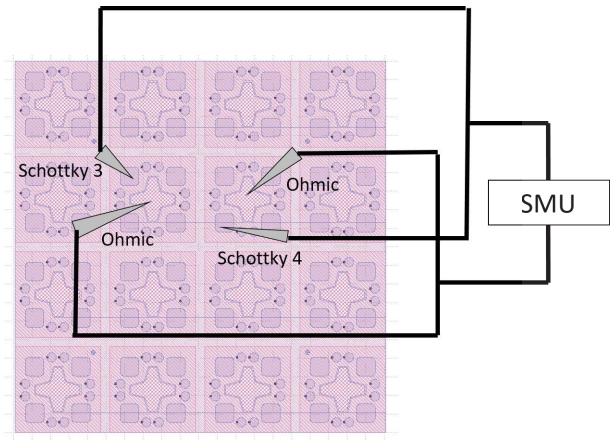


FIGURE 3.14: *Parallelization schematic from two diodes from the same cell*

The 3 serial resistances have been extracted and summarized in table 3.1.

TABLE 3.1: *Extracted serial resistance summary for Schottky 3 and 4 and for parallelization of both*

Cases	Serial resistance (Ω)
Schottky 3	24509 ± 122
Schottky 4	31948 ± 408
Parallelization	13736 ± 208

3.4.2 Diodes parallelization from the same cell

After, the same process has been performed to measure parallelization between two Schottky diodes from the same cell. Those first characteristics are presented with the red and black curves on figure 3.17. After, the parallelization was done using a third probe, as shown on the schematic below. (fig.3.16) In this situation, both Schottky are sharing the same ohmic contact they are named Schottky 1 and Schottky 2. The parallelization result is shown in

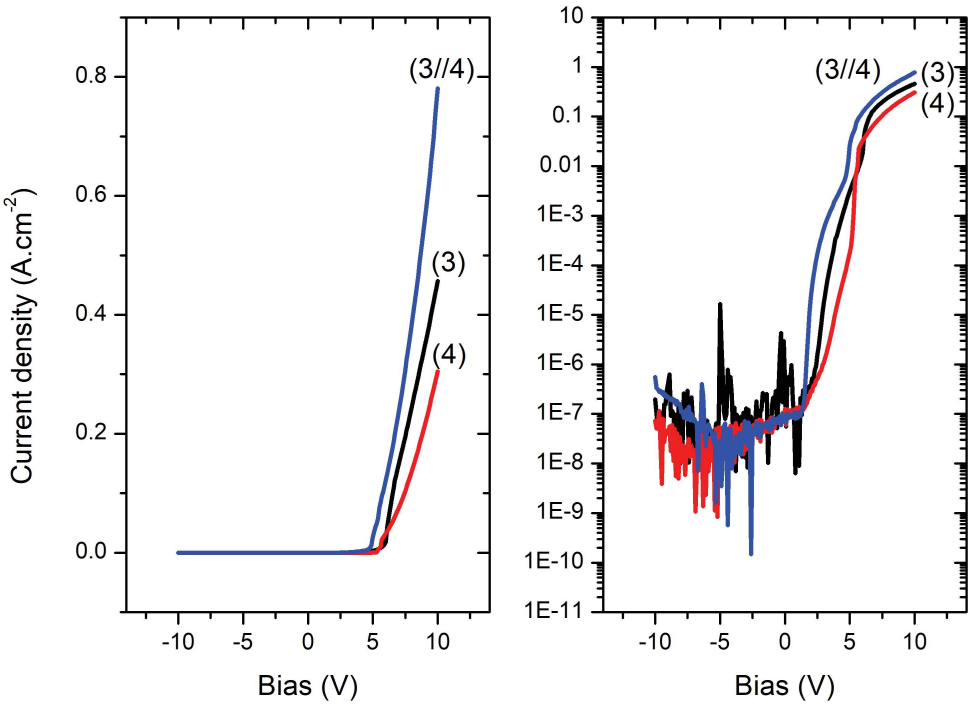


FIGURE 3.15: *I-V characteristics from two independent diodes: Schottky 3 and Schottky 4 and from their parallelization*

green in figure 3.17. The first thing to be noticed is the forward current increase when both diodes are put in parallel.

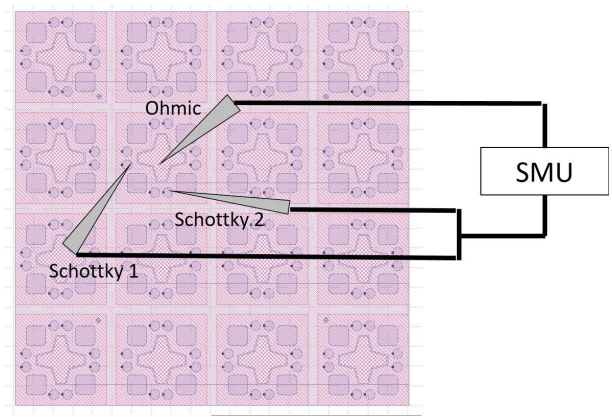


FIGURE 3.16: *Parallelization schematic from two diodes from the same cell*

All serial resistances extracted for those measurements are reported into table 3.2.

In this configuration even if both Schottky diodes are sharing the same ohmic contact, current paths are different for both diodes (i.e fig.3.18) allowing to put them in parallel without having the p++ common resistance problem.

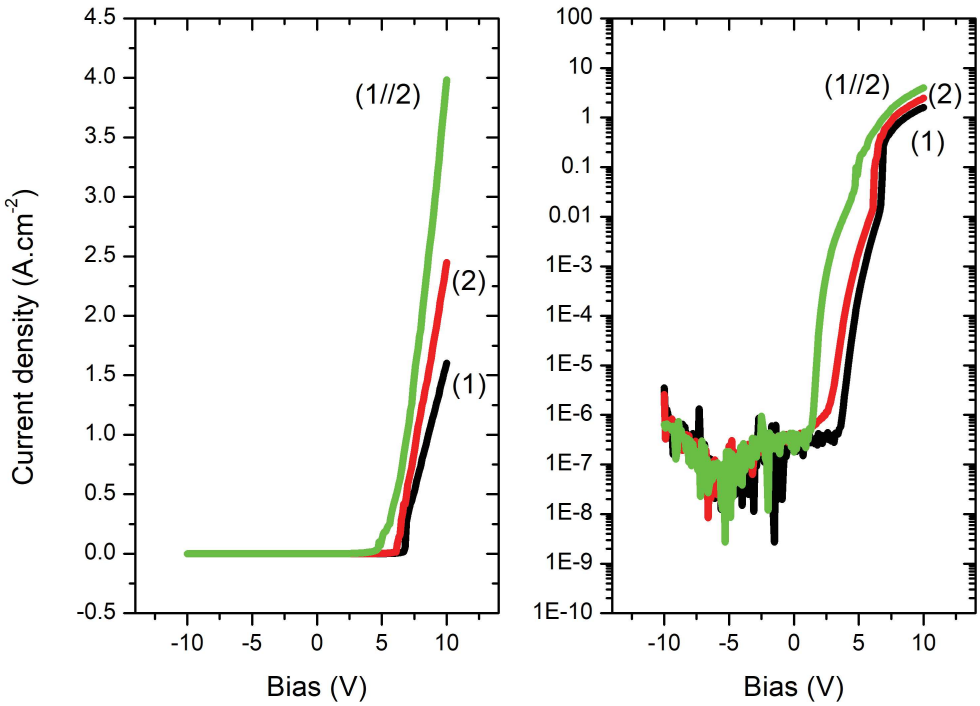


FIGURE 3.17: *I-V characteristics from two independent diodes: Schottky 1 and Schottky 2 and from their parallelization*

TABLE 3.2: *Serial resistance for each measured diodes and parallelization presented before*

Cases	Serial resistance (Ω)
Schottky 1	29673 ± 71
Schottky 2	20661 ± 111
Parallelization	13280 ± 129

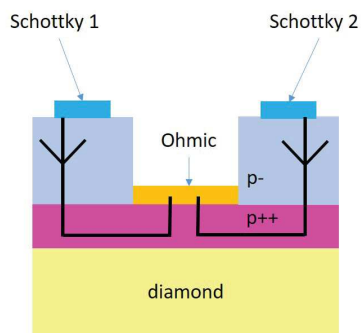


FIGURE 3.18: *Current path schematic for 1 cell with 2 diodes put in parallel with the new architecture*

3.4.3 Comparison between parallelization from same cell or from different cell

In this section the comparison between both parallelizations will be done and an attempt of explanation will be given.

Now to understand what is happening let's look at the formula 3.2 which can be rewriten in terms of current (formula 3.5).

$$I_{eq} = I_1 + I_2 \tag{3.5}$$

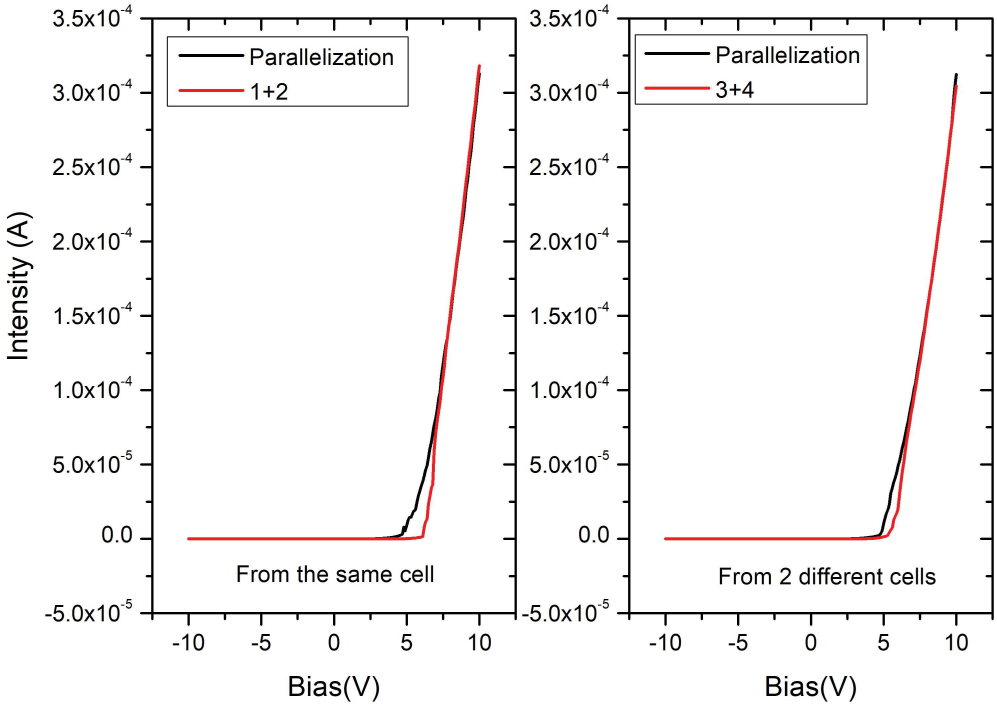


FIGURE 3.19: *I-V comparison between the two previous cases and between the parallelization (black) and the current sum (red)*

Looking at figure 3.19, presenting both case studied before. On the left, the parallelization from two diodes of the same cell (black curve) and the Schottky 1 and Schottky 2 sum in red. On the right side the same plot but this time with the two diodes from different cells and the Schottky 3 and Schottky 4 sum. In both cases, it seems that in the ohmic part of the I-V characteristic both black and red curves are superimposed, and the thermionic ones is not. The thermionic current is not taken into account in the model presented before. This is not an issue because in order to increase the current in the ON state the limiting factor will be the ohmic region which does not seem to be impacted. But by zooming closely to the ohmic part (fig. 3.20) it appears that the parallelization curve is slightly below the intensity sum for the case where Schottky diodes are sharing the same ohmic contact which is the case for the same cell measurement. This is not the case when each Schottky has its own ohmic contact. In the first case the common resistance is still present but minimized. On the other

hand, when there is two diodes with two different ohmic contacts the common impedance disappear.

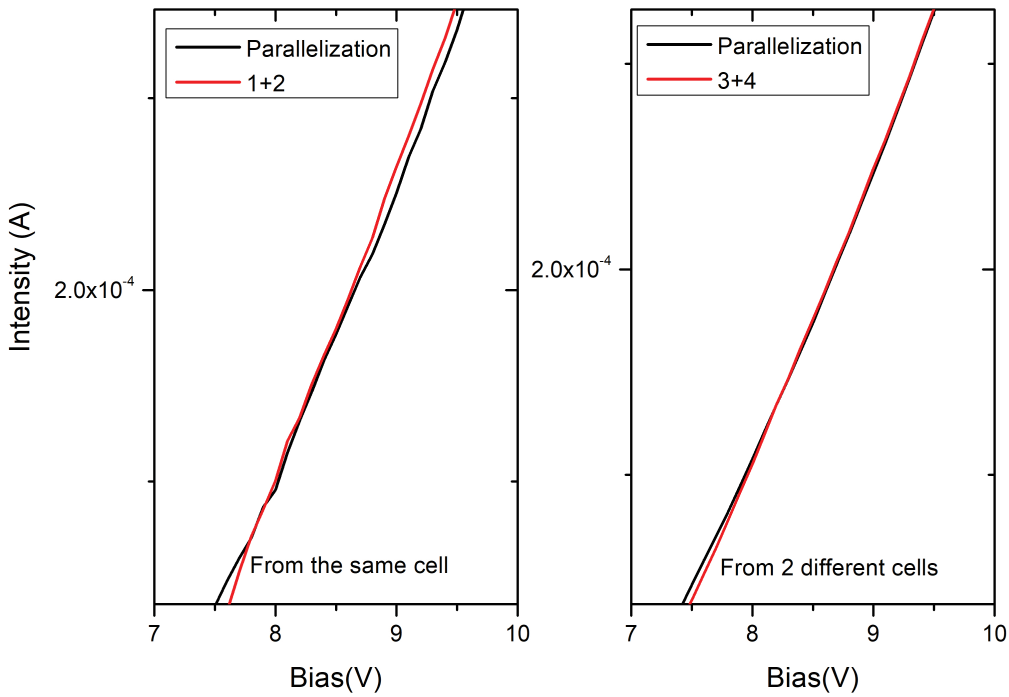


FIGURE 3.20: *Zoom of the ohmic part from the 2 previous graph*

3.4.4 Conclusion

The same type of measurements has been performed on sample HVDC2 and the same behavior has been observed. From all of this, it is possible to say that the new mask design allows to reduce and even to make the common impedance problem to disappear. It appears that an electrical insulation of the cell is not compulsory to remove the common impedance. Ohmic contacts multiplications over the entire sample closer to Schottky contact seem to be the key to remove this issue. But it seems that having more fabrication step which are required to have the electrical insulation impacts the diodes characteristics when taken one by one. Also the use of NDT substrate which have been demonstrated as conductive is not a good option for having insulating cell one from the other.

3.5 What's next: integration

In collaboration with G2Elab in the framework of the french ANR project Diamond HVDC, integration of diamond component was targeted, for example into a commutation cell. Like that diamond device can be implemented more and more for power devices purposes. With this new design, it is also possible to think about what is next for the diamond power device

community. The easier integration to do is to create a diode bridge. This bridge permits to transform any AC current entering the bridge in to DC at the output. The bridge's electrical diagram is presented in figure 3.21.

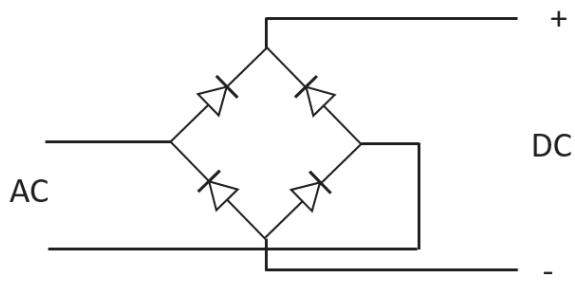


FIGURE 3.21: *Diodes bridge diagram*

To create such a bridge 4 diodes are needed with at least 3 different ohmic contacts. In this configuration , isolated cell on the same substrate can be a solution to ensure to have same epilayer characteristics and by the same time diodes with the same characteristics and temperature. Unfortunately, isolated cell didn't work as wanted, so the bridge will be fabricated with diodes coming from different substrates. In that case, bridge's temperature will not be uniform. The bridge was realized by G2Elab with 3 different samples grown and fabricated previously to the work presented here. A picture of the bridge is shown in figure 3.22 with some preliminary results 3.23 obtained at room temperature with a 1kΩ resistance to close the DC circuit. On the preliminary results the AC bias is represented with the blue curve and the DC bias leaving the bridge (orange curve). It appears a bias dropped inside the bridge which is due to the voltage dropped inside the four diodes.

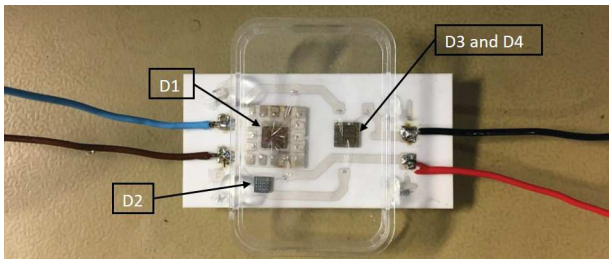


FIGURE 3.22: *Diamond diode bridge's picture*

More measurements have to be run and another bridge has to be fabricated with more efficient diodes. To continue with diamond power device integration Schottky diode need to be associated with MOSFET or MESFET in order to create commutation cells or even converters. But this is requiring to all components working with the same caliber(same current range).

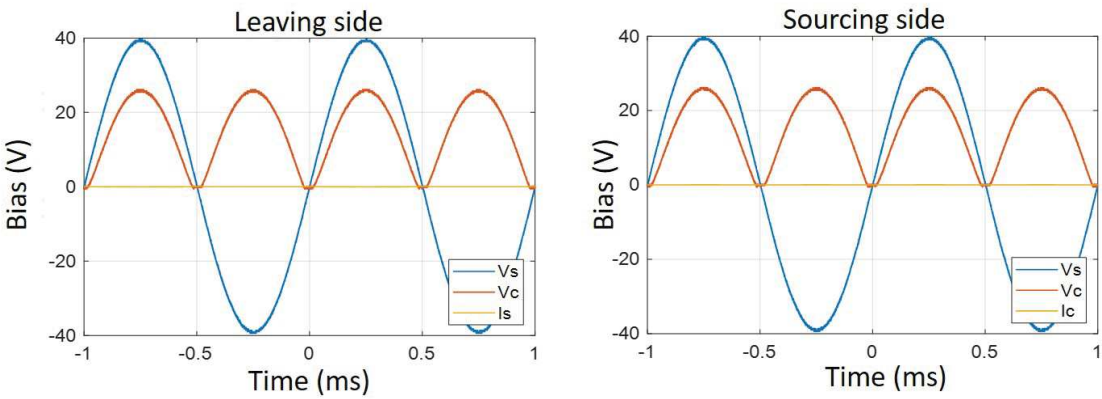


FIGURE 3.23: *Diodes bridge's preliminary results with the the bias at the bridge entrance (blue curve) and at the leaving (orange curve) in function of the time*

Chapter 4

Diodes for high voltage breakdown

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After working on current increase and the integration of diamond Schottky diodes, other issues have been studied: the diamond component premature breakdown voltage and leakage current. Here, the main focus will be the device characterization of the new Schottky diodes developed in chapter 2 to see if these new approaches are suitable for sustaining higher breakdown voltage.

4.1 How and why should the breakdown voltage be increase?

Currently the highest breakdown field for a diamond Schottky has been reported by A. Traore [79] with a diode sustaining more 7.7MV/cm where the p- layer was about 1.3 μm thick and with Zirconium Schottky contact. But the highest breakdown voltage for a pseudo-vertical architecture reported came from Kumaresan *et al.* [80], with a 1.6kV breakdown voltage for a 14 μm p- layer but in that case the electric field is 1.1MV/cm. Also in that case the Schottky metal used is Molybdenum. On the other hand, for vertical architecture the highest breakdown voltage is 1.8kV by Umezawa *et al.* [6] which corresponds to 1.8MV/cm for the electrical field. In that case field plates were also used in order to increase the breakdown voltage value. In each diode presented above the breakdown field obtained is still far from the theoretical value calculated for diamond 10MV/cm. In order to improve the diamond Schottky diode breakdown voltage, some parameters can be tuned. One of them was to work on the active layer by increasing the thickness and keeping a low doping value (i.e $[B] < 5.10^{15}$). This tuning comes with some challenges and some barriers have to be unlocked. This is why this work proposes 3 different solutions following this direction. During chapter 2 three new type of growth have been developed: encapsulated, selective and thick growth in order to improve the diamond Schottky diode breakdown voltage.

Once each device has been grown and fabricated, this chapter will focus on the characterization of this new type of device. The electrical measurement setup presented in section 3.3.2 in chapter 3 have been used to do so as well as SMU allowing to go to a higher voltage like the Keithley 2410 (V $\leqslant$1.1kV).

4.2 Solution 1: Encapsulated diodes

4.2.1 Samples' presentation

The first solution proposed in order to increase the active layer thickness was to developed the encapsulated architecture. The growth process is presented in section 2.2.2.1. Using this new technique two samples have been grown and refereed as 5$\mu m_encapsulated$ (fig. 4.1) and 2$\mu m_encapsulated$ into the summary table (table 2.1). This architecture's advantage is that etching is no longer required to deposit the ohmic contact. In that case the ohmic contact is deposited using the same process and the same thickness than the one presented in chapter 2 but on the entire substrate backside to ensure a good conduction between the four corners. After, it is glued with silver paste on a metallic pad printed on top of an alumina plate to allow the tip deposition for the Ohmic contact. The Schottky contacts fabrication does not change from chapter 2. Each device is composed with square diodes: 9 of 600 μm, 9 of 300 μm, 36 of 200 μm and circular ones with a 100μm diameter.

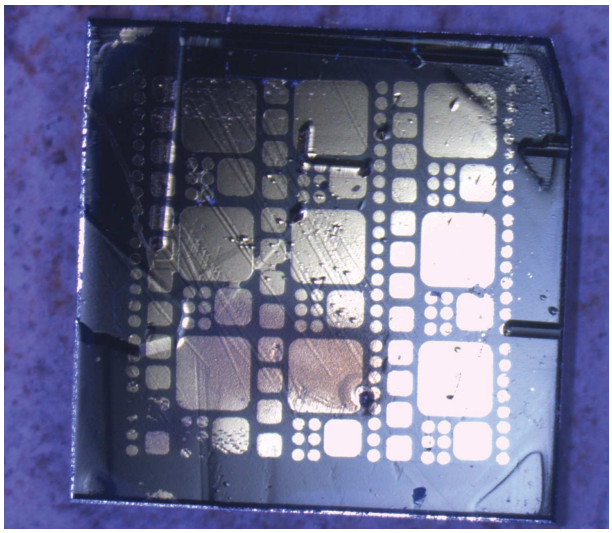


FIGURE 4.1: $5\mu m_encapsulated$ *device picture after full processing.*

4.2.2 Electrical characterizations

4.2.2.1 I-V

On both samples the same protocol was applied, first a voltage ramp between -10 and 10 V was applied in order to see diodes general behavior and after some reverse bias measurements have been performed to check the reverse capability of the device.

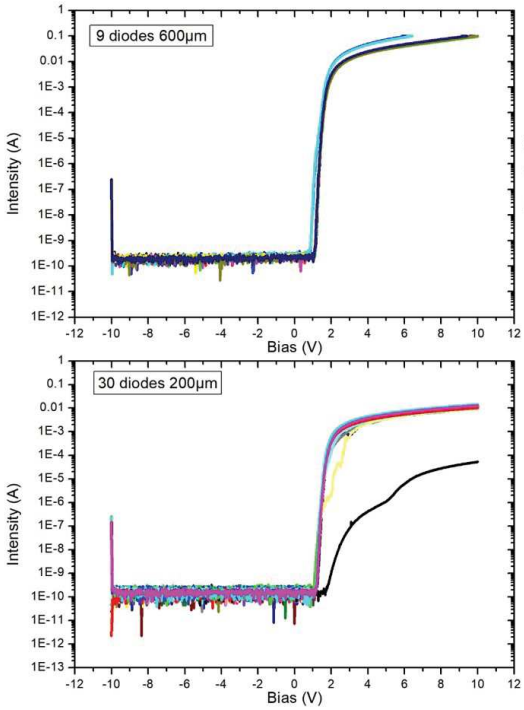
From -10 to 10V

Figure 4.2 presents the different results obtained at room temperature and under vacuum for $5\mu m_encapsulated$. Those results represent the I-V curves plotted with the current in semi-logarithmic scale. For each diode size the Schottky barrier is the same excepted for one in the 200 μm plot. It is also possible to see a slight variation of the serial resistance in each case. The extracted parameters such as the Schottky barrier height, the ideality factor and the serial resistance are obtained by fitting the different curves using formula from chapter 1 (1.24). Results have been summarized in figure 4.2 table. From this table it appears that the ϕ_b has a 1.25eV mean value, an ideality factor close to 1 indicating a good Schottky interface between diamond and zirconium. The serial resistance varies from one to the other diodes maybe due to the different distances between the ohmic contact and the Schottky one. The specific resistance is also calculated, it appears that the serial resistance is decreasing with the contact size.

Same results have been observed for the other sample $2\mu m_encapsulated$, with a reproducible Schottky barrier height and a serial resistance varying slightly from one to the other.

Reverse measurements

In order to check the blocking capability of this new architecture reverse bias measurements were performed. To do so, a Keithley with a better detection limit (10^{-12} A) has been used



5µm_encapsulated sample

Diodes	600 µm	300µm	200µm
ϕ_b (eV)	1.20	1.29	1.25
n	1.05	1.01	1.13
R_s (Ω)	[84;108]	[305;367]	[602;813]
$R_{on}S$ (Ω.cm²)	[0.30;0.38]	[0.27.033]	[0.24;0.32]

FIGURE 4.2: *5µm_encapsulated I-V characteristics for different contacts size*

in order to measure the leakage current from the beginning. For that, measurements have been taken by increasing the reverse bias by 10V step until reaching an hard breakdown or until the leakage current is one order of magnitude below the forward current. For *5µm_encapsulated* breakdown capability of this device is not quite reproducible some diodes are sustaining more than 300V and for the same size only 200V as shown in figure 4.3. For this sample avalanche is not reached yet, only the set up was the limitation for this sample.

For the other sample which is thinner the reverse blocking capability, is lower around 200V. The best feature for this sample is presented in figure 4.4. For this diode, the maximum electric field calculated is 1.5MV/cm.

4.2.2.2 C-V

For each sample the effective doping levels have been measured thanks to C-V measurements. For *5µm_encapsulated*, the $1/C^2$ plot is presented in figure 4.5. From the linear fit, the extracted slope is $-1.07 * 10^{21}$ and the diode is a $600\mu m$ square. In that case the effective doping level using formula 1.33 is equal to: $1.8 * 10^{15} atom.cm^{-3}$.

For the second sample *2µm_encapsulated* same measurements have been performed and the resulting curve is given in figure 4.6. In that case the measurement was taken with a lower frequency, explaining why the curve is more noisy than the previous one. However, it is still possible to performed the linear fit, the slope coefficient is $-5.76 * 10^{20}$ also for a 600 μm square diode an effective doping level of $3.44 * 10^{15} atom.cm^{-3}$.

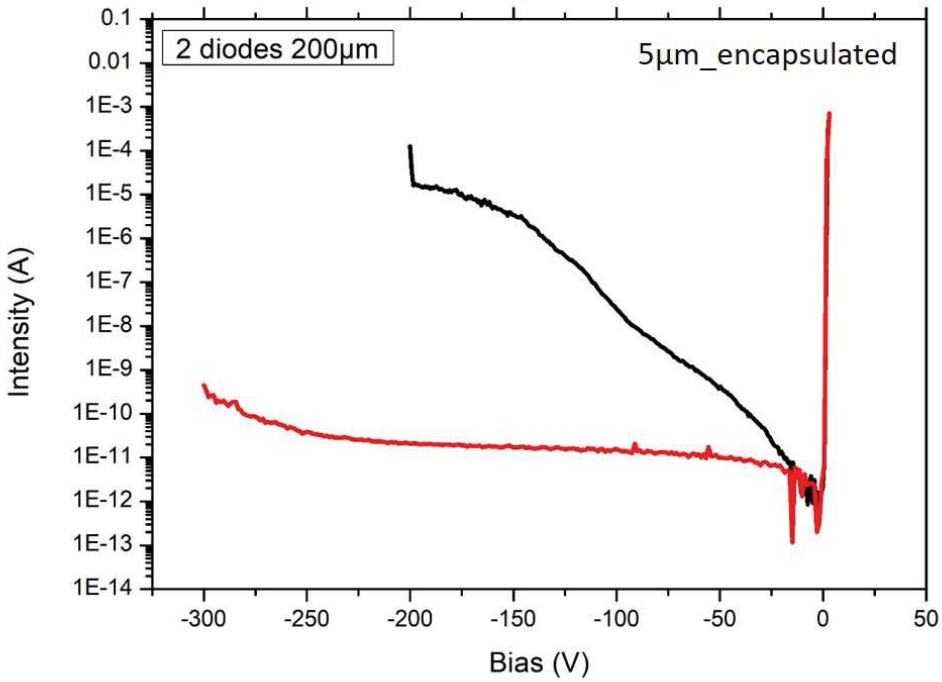


FIGURE 4.3: *5µm_encapsulated I-V reverse characteristic for 2 different diodes with the same size (200µm)*

Both extracted doping levels are in good agreement with what was expected due to growth condition. The thinner sample (2*µm_encapsulated*) with an higher doping level can be explained due to growth process, boron concentration inside the plasma ball is higher at the beginning and its concentration is decreasing inside the plasma with the growth time increasing. So the concentration is lower for thicker sample with a longer growth time .

4.2.2.3 Conclusion

From this two samples it seems that the encapsulated growth is a good option in order to remove the etching step. The device ON state is reproducible at the die scale for the off state work still need to be done. Other samples have to be grown with this technique with a thicker active layer to see if this device is able to sustain more in reverse with more reproductibility. Nevertheless the lateral growth wrapping the substrate should be more studied to understand if this is a limitation parameter as suggested by an extra experiment run on the 2*µm_encapsulated* with diodes bonding and current which is not increasing with the number of bounded diodes. This limitation is also a possible explanation for the specific on resistance evolution.

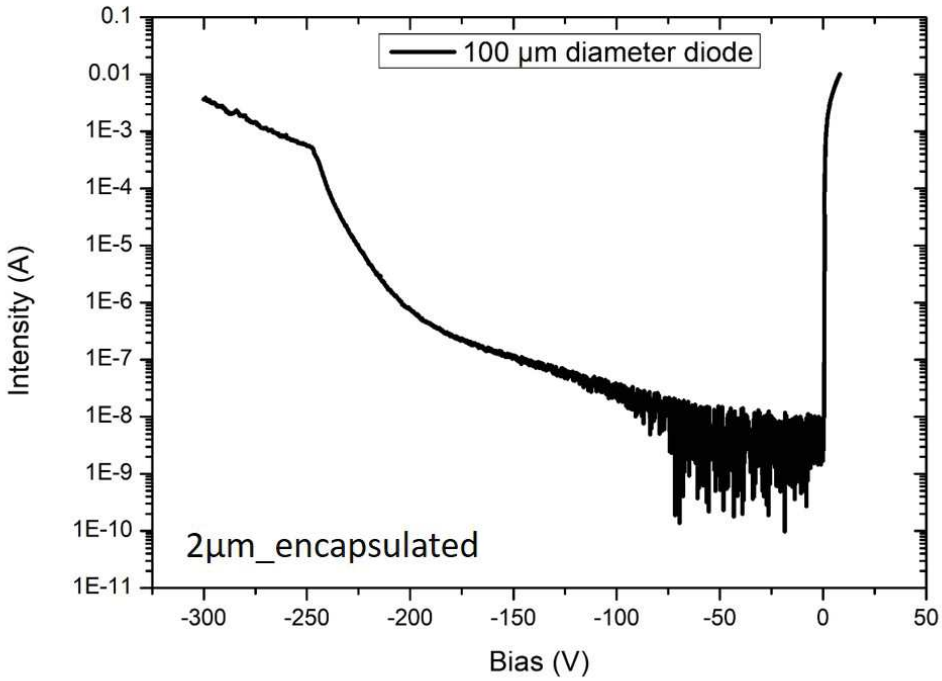


FIGURE 4.4: *2µm_encapsulated I-V reverse characteristics showing the best reverse capability*

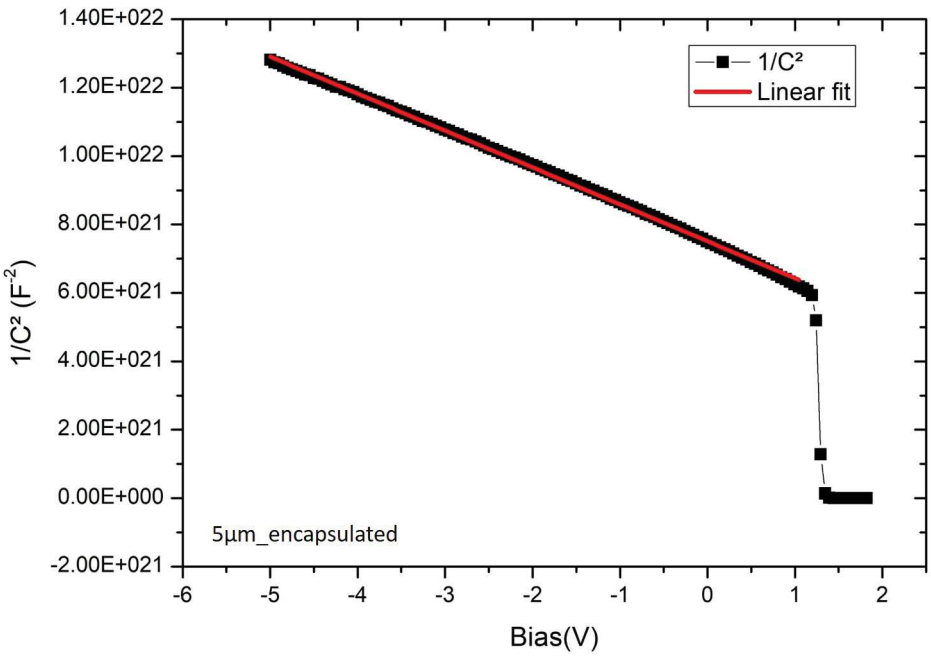


FIGURE 4.5: *5µm_encapsulated* $1/C^2$ *plot in function of the bias with its linear fit*

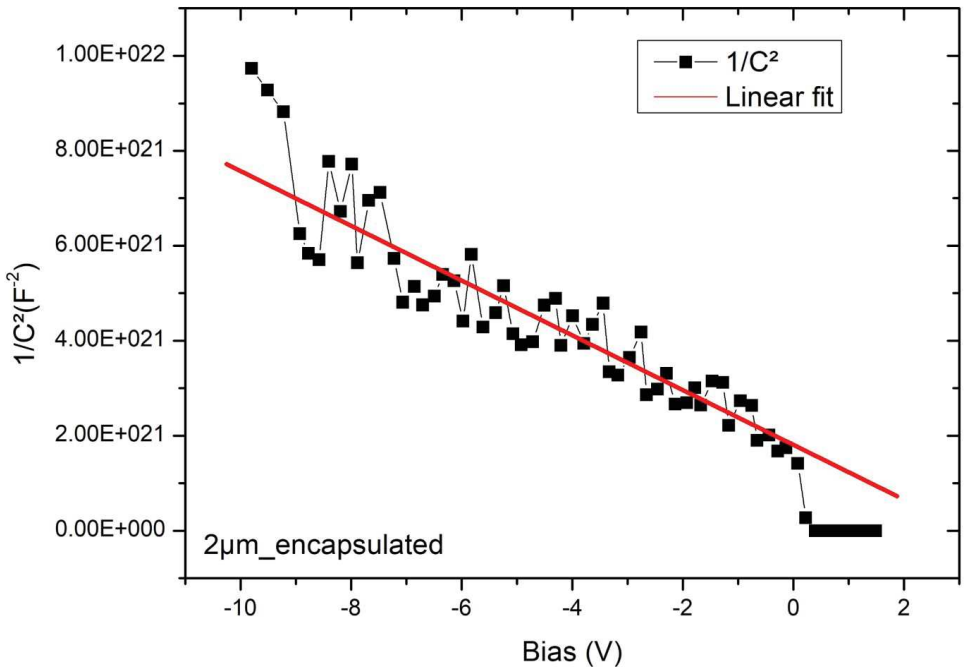


FIGURE 4.6: *2µm_encapsulated* $1/C^2$ *plot in function of the bias with its linear fit*

4.3 Solution 2: Selectively grown diode

4.3.1 Sample's presentation

The second solution this thesis have been looking on was the thick selective growth. To obtain a working device the process presented previously is used (chap. 2, section 2.3) from the beginning without the etching step. For that sample the used design is presented in figure 4.7, it is composed with one Ohmic contact and several Schottky contacts with different sizes 600, 300, 200 μm square ones and round ones with two diameters 150 and 100 μm.

4.3.2 Electrical Characterization

4.3.2.1 I-V characterization

The first measurements were performed on the 200 μm size diodes between -40 and 40V and results are shown in figure 4.8. On this graph 16 diodes are presented. The I-V characteristics are showing in the forward regime an high threshold voltage around 10V as well as a low current with 40mA at 40V. On the reverse regime the diode characteristics show high leakage current especially by looking at the logarithmic scale graph. For those diodes the rectification ratio ($I_{forward}/I_{reverse}$) at 40V is less than 500.

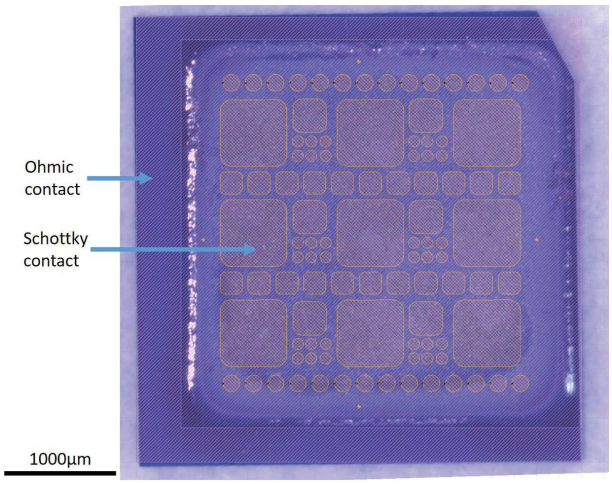


FIGURE 4.7: *Sample optical view with the mask design on top it*

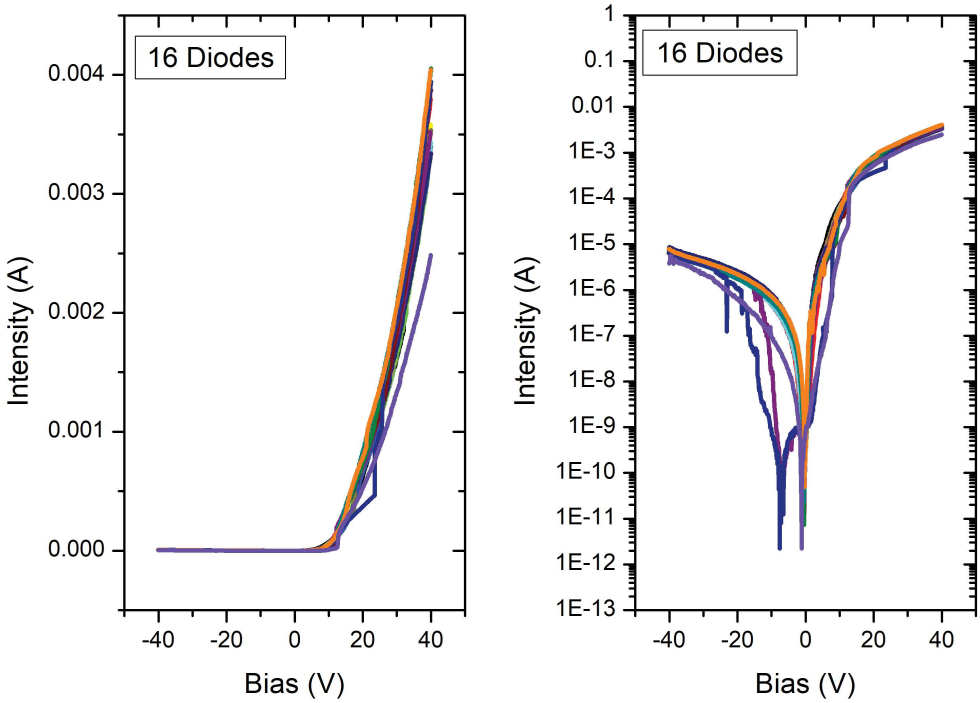


FIGURE 4.8: *I-V characteristics in linear (left) and logarithmic (right) scale obtain on the selectively grown sample in a first attempt*

To have a better understanding the diode physical parameters are extracted, the Schottky barrier height $\phi_b = 0.52eV$ and the ideality factor n=7. This high value is probably due to the bad interface between the diamond and the Schottky contact and the presence of interface states [81]. This bad interface comes from the roughness of the grown layer as presented in chapter 2. The low ϕ_b value explains why the measured diodes have a leakage current so high. The mean diodes serial resistance equals to 4784 Ω. This high serial resistance can be explained by the low active layer doping level targeted.

C-V measurement was performed but due to the low doping level targeted (non intentionally doped layer), nothing came out from those measurements.

4.3.2.2 Conclusion

Electrical characteristics obtained with this sample confirm that it is possible to obtain Schottky diode by a thick selective growth of the active layer and removing the etching step. Nevertheless, the obtained characteristics are on the reverse regime very leaky and with some dispersion in the forward regime. One option to improve the diode characteristics will be to perform a slight etching to remove the p-overgrowth below the hard mask to improve the Ohmic contact. Leakage current is also coming from the the p- layer poor crystalline quality and gives some perspective to find better conditions to obtain thick selective grown layer.

4.4 Solution 3: 20 μm thick diode

The last option was to grow even thicker active layer. As presented in chapter 2, one focus of this thesis was to improve the growth of thicker non intentionally doped layer. Thanks to this, a 20μm thick p- was grown (referred as 20μm in table 2.1) and Schottky diodes were fabricated.

4.4.1 Sample's presentation

Once this sample was grown, one issue was to reach the p++ layer below the p- and covered by lateral overgrowth. Etching was not a option, the latest report [82] to have good surface after a deep etching is for 8 μm layer which is much thinner than this sample. The choice was made to send the sample back to Syntek for side polishing as shown in figure 4.9. The polishing process removed about 200 μm of the diamond plate total size.

After polishing SEM image (figure 4.10) have been taken to ensure the the polished side good quality. On this image the three layers are visible with the proper thickness i.e p-, p++ and substrate. It also appears some cavities inside the p++ layer, one explanation is that it could come from the polishing done by Syntek which has a preferential etching orientation.

After, an adapted process (2.3) have been performed to do the diode fabrication but ozone treatment and annealing are staying the same. First the ohmic contact have been deposited on the polished side (a) fig. 4.11) and followed by the Schottky ones on the top (b) fig. 4.11). The final device is presented with SEM view (c) fig.4.11). There is 2 Ohmic contact

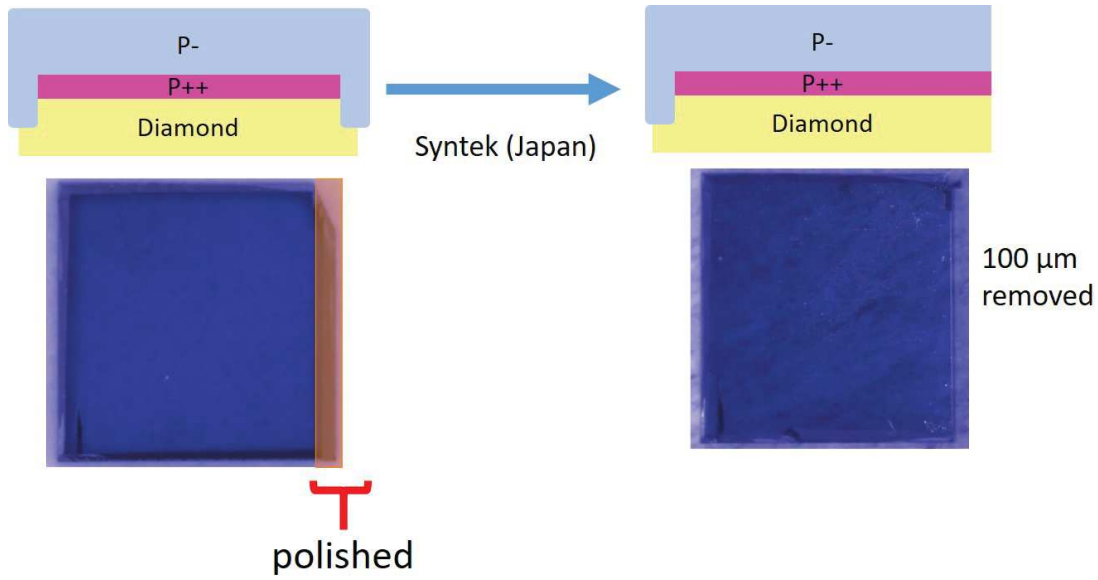


FIGURE 4.9: *Side etching process schematic with optical micrograph sample's top view before and after polishing*

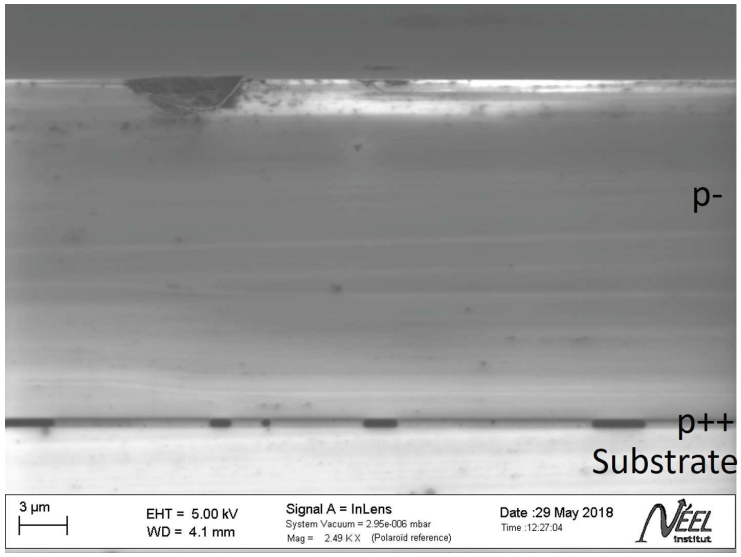


FIGURE 4.10: *Polished side SEM picture, some cavities appear inside the p++ layer*

not well defined due to the deposition process and 19 Schottky contacts (70x70 μm^2) placed at the edge. This choice of "limited" design was made due to the constraint imposed by the experiments ran in the next chapter (chap. 5). Other Schottky contacts have been deposited after on the sample entire surface with bigger sizes.

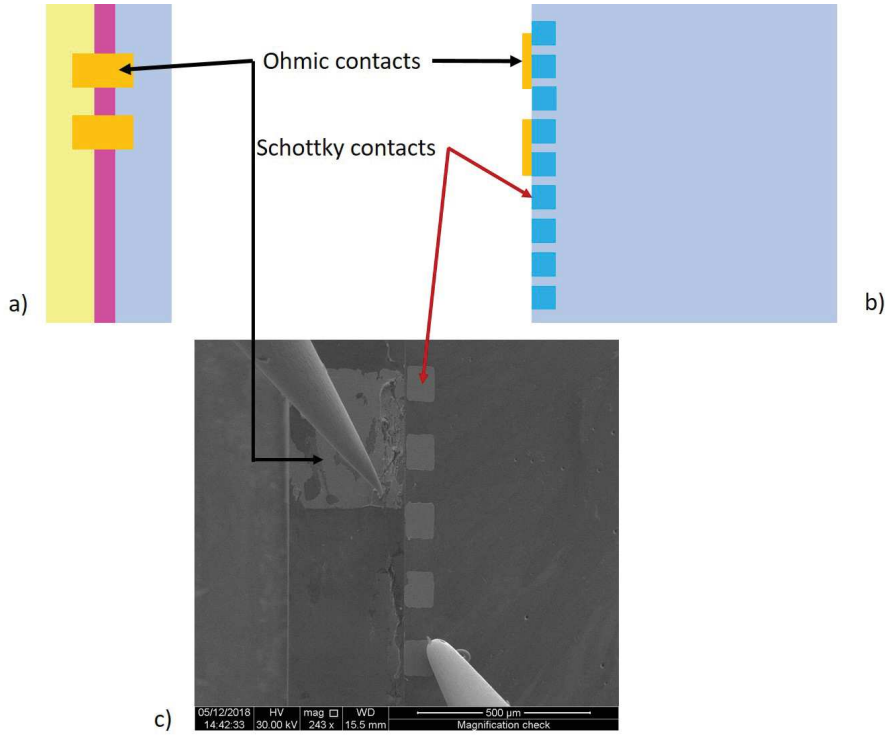


FIGURE 4.11: *a) Schematic 20µm sample side view before Schottky contact deposition, b) Top view after Schottky contact deposition and c) SEM view with both contact with a 45° angle*

4.4.2 I-V Electrical characterizations

Due to the contacts size and positioning on the substrate, the first measurement have been done inside the SEM equipped with the same probes technology than the characterization box presented in the previous chapter (fig. 3.10) and the same source measurement units (SMU) are used. Inside the SEM measurements are done under high vacuum (10^{-6} mbar) with the electron beam off, in order to be close to the condition used for the other samples.

Typical I-V characteristics obtained in the case of this sample are presented in figure 4.12. First, the rectifying behavior of the diode can be noticed meaning that our ohmic contact is well positioned on the p++ layer which was not verified yet. From the logarithmic curve it is possible to extract the Schottky barrier height and the ideality factor which are respectively 1.02eV and 5.7. This indicates that the interface between the diamond and the Schottky contact is not perfect. This bad interface can be linked to the difficulty to realize such contact at the substrate edge. On the other side from the linear curve it is possible to extract the serial resistance of the diode. The serial resistance is equal to 1.65MΩ. This big

value can be explained by the Schottky contact small size the active layer thickness (20 μm) and the low doping level of the layer due to growth condition. The doping level is expected to be around 1.10^{15}atom.cm^{-3} and will be determined later by cathodoluminescence (c.f chapter 5 section 5.4).

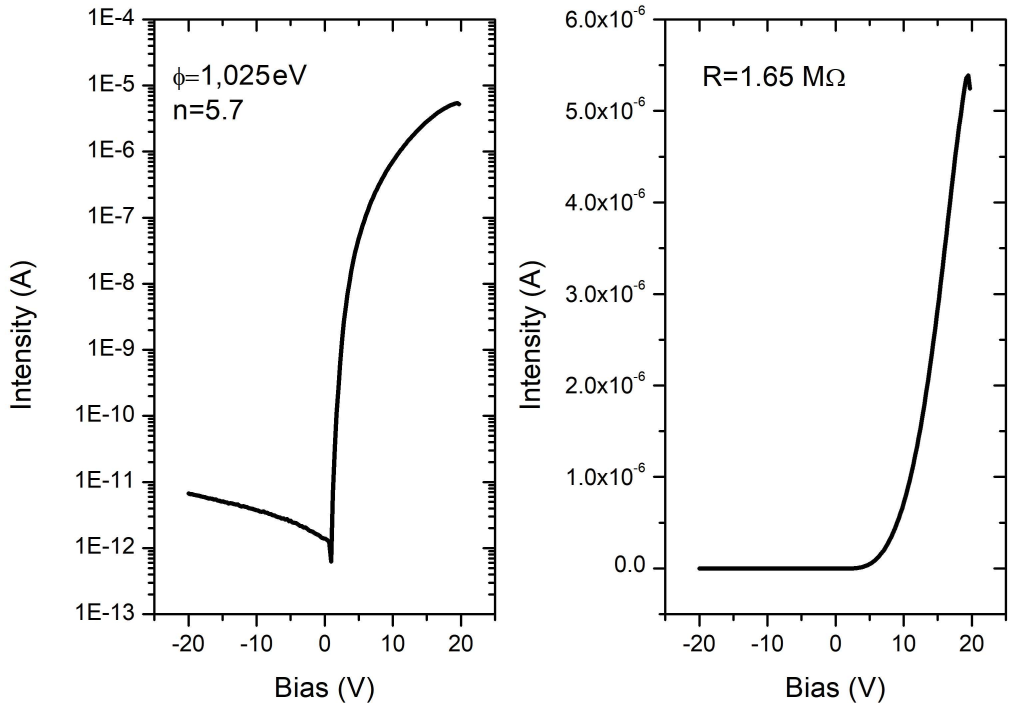


FIGURE 4.12: *Typical I-V characteristics obtained in logarithmic scale on the left and linear scale on the right for a Schottky contact for the 20 µm thick sample*

Moreover, reverse bias measurements have been done to check the breakdown voltage. First measurements were also performed inside the SEM by increasing the bias little by little in order to see if the breakdown occurs. Those measurements are presented in figure 4.13. In that case the Keithley has a 10^{-9} A detection limit, also measure is stopped at 600V because the SEM sealed passage does not allow to go further. Anyway, some information are given by this graph all the measured contact sustain at least 600V without hard breakdown. Also the leakage current which is below the detection limit at the beginning is increasing faster for some contacts.

To reach a higher voltage, the use of the probe station is required as well as the Keithley 2410 allowing to go up to 1.1kV and with a 10^{-12} A detection limit. In this experiment only one contact has been measured and the obtained result is given is figure 4.14. On this graph I-V is plotted, the maximum bias applied is 1.1kV which is the SMU limit, at that point the intensity reached is still below the forward bias and no hard breakdown occured. A maximum 0.5 MV/cm electric field is obtained. In order to go at higher voltage an other experiment has to be used as well as bigger size contact.

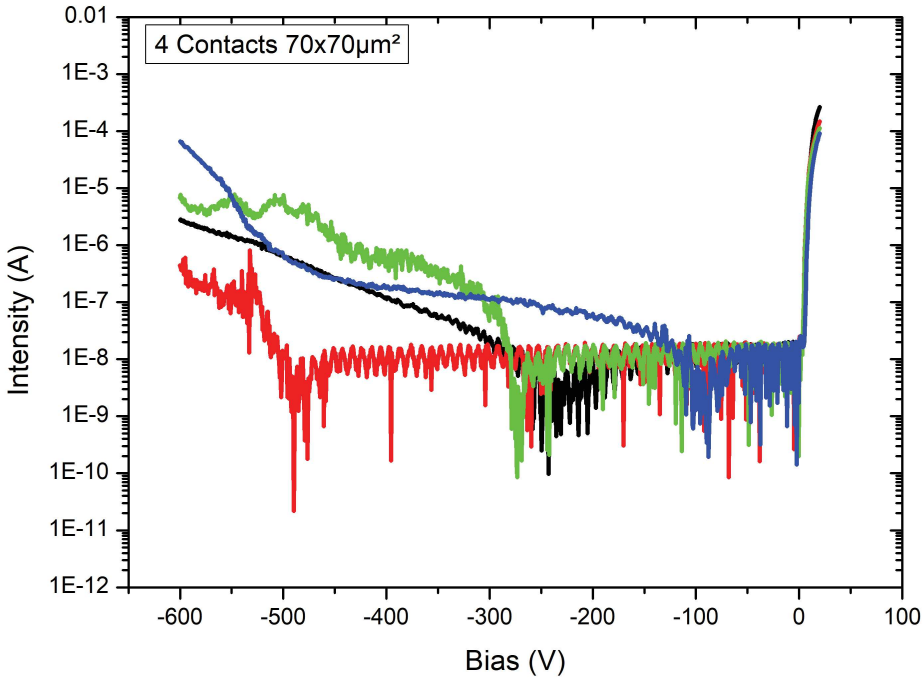


FIGURE 4.13: *I-V reverse measurements done inside the SEM for 4 (70x70μm²) different contacts*

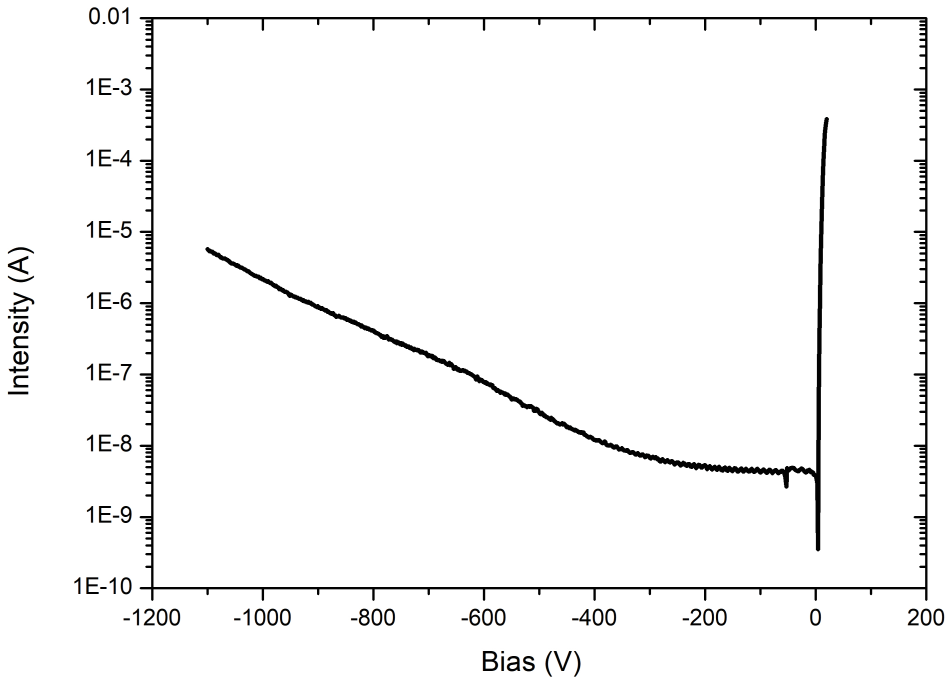


FIGURE 4.14: *I-V reverse characteristic, maximum bias reached 1.1kV*

In this option bigger sized contacts (square 500 and 200 μm and 100 μm diameter rounds one) have been deposited and annealed in the same condition. After the sample was reported on an alumina plate with metallic pad and glued with silver paste for the ohmic contact electrical conduction.

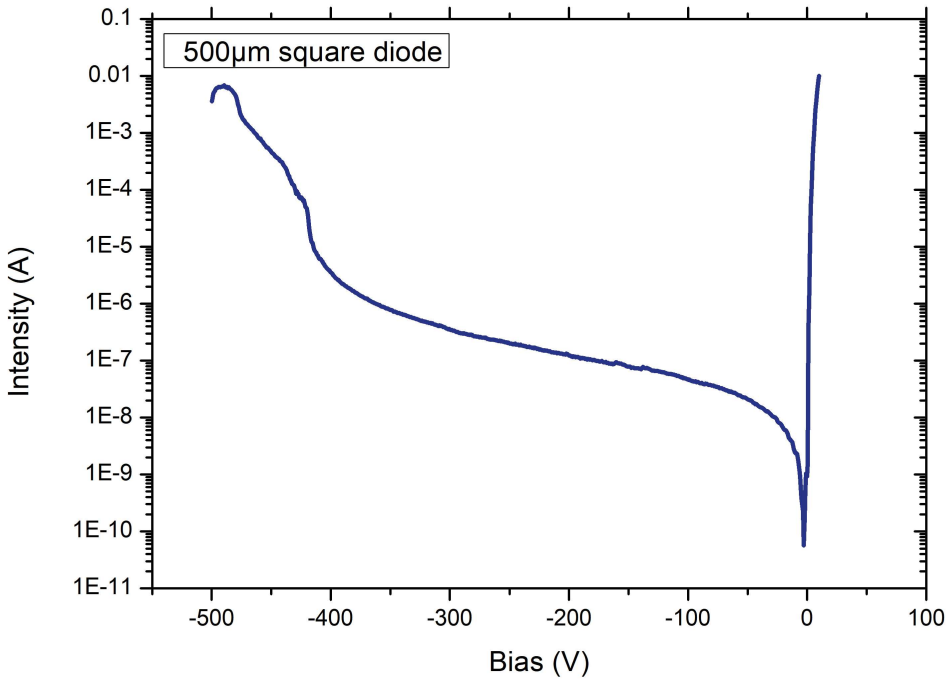


FIGURE 4.15: *I-V reverse characteristic, for a 500 µm square Schottky diode*

Unfortunately those new contacts do not sustain the same voltage as shown in figure 4.15. This graph represents the I-V characteristic obtained for a 500 μm square contact, it is visible that the reverse current is increasing and the rules about a decade of difference between $I_{forward}$ and $I_{reverse}$ is reached around -460V. For a smaller contact same experiment was done and results are in the same order reverse bias before reaching the limit is higher but still lower that the first contact deposited. Those results can be due to the contact's size which are bigger and potentially have more defects underneath which link to more leakage current. This leakage can also come from the bad contacts deposition due to the configuration.

4.4.2.1 Conclusion

From the I-V measurements ran on this sample, it has been shown that increasing the the thickness of the active layer is increasing the sustainable reverse bias. But this kind of architecture is requiring a polishing step and the deposition of the ohmic contact on the side of

the sample. Small contacts show better characteristic in reverse and can be used to be compared with the state of the art devices. While there is no easy possibilities to go at higher reverse bias. This sample will be more investigated in the next chapter 5.

4.5 Conclusion

To conclude, it appears that the different new techniques set up during this thesis shows promising results and new perspectives for diamond Schottky diodes. Encapsulated diodes show, up to now, the best feature with good ON state reproducibility and blocking capabilities up to 200V. Even so, new sample would have to be grown and fabricated to see the full potential of this architecture with thicker p-layer (i.e 10 μm). More work have still need to be done on thick selective growth because as it was shown previously lot of defects are present at the surface and the I-V characteristics presented show very poor blocking capabilities which is the one interest of using diamond component. To finish growing 20μm thick p- layer on the entire sample was a step forward but the fabrication process is more complicated for the ohmic contact deposition. Nevertheless this sample shows the best feature in reverse bias and the breakdown voltage was not reached meaning that this device can go at higher voltage with small contact. The bigger contact tried did not show the expected results (premature leakage) probably because the number of defects underneath the contact is higher increasing the leakage current.

Chapter 5

Diamond Schottky diode transverse study

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On the previous chapter a 20 µm thick sample was presented. This chapter will be devoted to the in depth characterization of a diamond Schottky diode. To do so, several techniques will be used such as cathodoluminescence and electron beam induced current in order to have an experimental view of what is really happening inside the material and not only simulation method.

As presented in previous chapter 2 and chapter 4 a thick layer was grown and Schottky diodes were fabricated and measured. This sample also gave an unique opportunity because of its architecture to have a better understanding of what is happening into the depth of a Schottky diode.

5.1 Introduction

Up to now, in order to answer some critical questions about the power electronic devices properties such as: "how is the electric field distribution inside the material" one solution was to run some finite element modeling. Several studies have been reported in the literature [76, 44, 83, 84, 85] for diamond Schottky diode. In all of those studies the electric field underneath the Schottky contact is well defined but does not take into account the material reality like defects, interface states and so on. This study is the starting point to have a better understanding but does it fit the reality?

One experimental technique used in other materials to investigate the electric field distribution is to use Electron Beam Induced Current (EBIC) [86, 24, 87, 88], this technique can also be used in order to electrically characterized defects [89]. Some experiments have already been done on diamond components by Umezawa *et al.* [49, 90]. In this study the sample is studied from the top and only the lateral electric field from a Schottky contact is under investigation. Following the same technique edge termination was also studied [25].

In this chapter we proposed to investigate the electric field distribution into the diamond depth thanks to the EBIC technique. At the same time this sample will be used to perform cathodoluminescence (CL) in order to check defects and doping level always into the material depth.

5.2 Sample

The sample used to performed this study is the 20 μm thick sample presented in chapter 4 section 4.4. This sample advantage is its polished edge allowing to see the entire stack. The contact positioning at the substrate edge it is because if those contacts were placed some few microns nearer the center the EBIC signal would not be measurable.

5.3 Setup presentation

Institut Néel has a unique equipment allowing us to perform at the same time EBIC measurement and cathodoluminescence one. This facility in presented in figure 5.1. This setup is composed with a FEI Quanta 200 Scanning Electron Microscope (SEM) with an acceleration voltage from 0.2 up to 30kV. Inside the SEM chamber a GATAN sample holder can work at room temperature or cool down at 4k with liquid helium. On this stage four probes can be added and controlled at a nanometric scale by piezoelectric motors in x, y and z direction (same than the one used in the probe station).

In CL mode a parabolic mirror is placed to collect and reflect the beam toward a lens and the monochromator entrance slit. This monochromator (HR460 Jobin Yvon) allows to obtain spectra from 200 to 900 nm. The signal is recorded through a CCD camera.

In EBIC mode, two solutions are available to do electrical measurement. The first one is to do only measurement without image in that case usual SMU presented in previous chapter are used. The second solution is to use a preamplifier Standford Research System model SR570 and graphic card that will transform the electrical signal into an EBIC image in a grey scale.

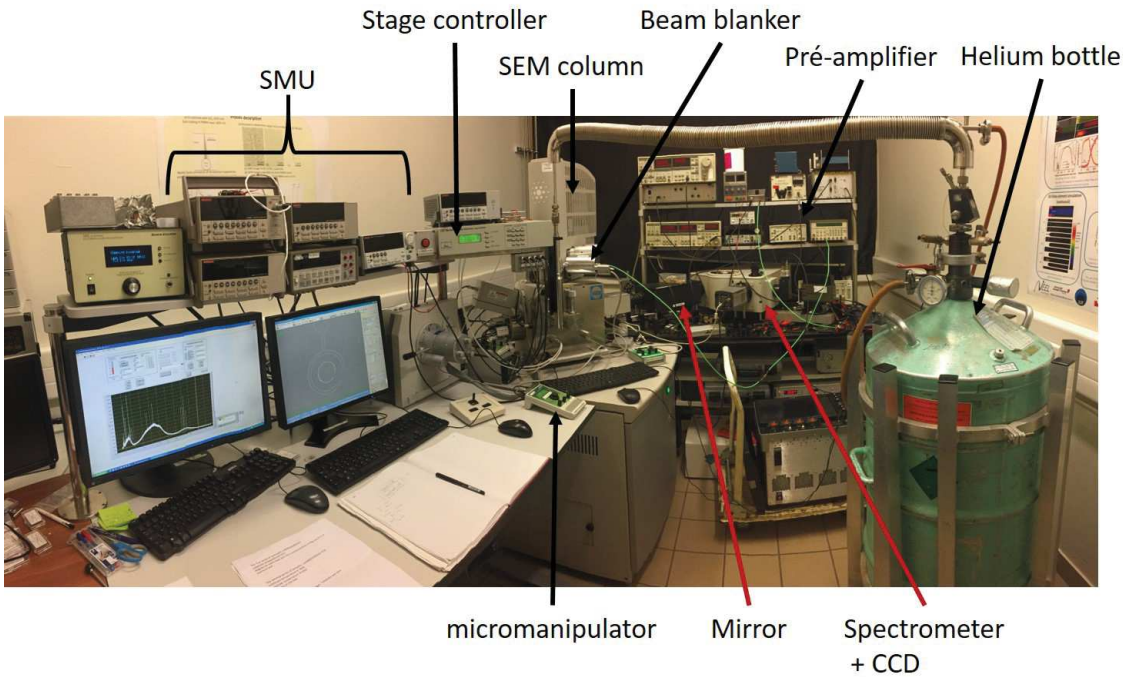

FIGURE 5.1: *Institut Néel's EBIC and cathodoluminescence setup picture*

The sample is glued with silver paint on an alumina plate with an angle of 90° to perform CL and a 45° for EBIC with an example in figure 5.2. The alumina plate addition is here to insulate the sample from the stage and to decrease the risk of ground leakage through the sample holder. In both positions the electron beam is going to probe the sample's polished side.

5.4 Cathodoluminescence study

5.4.1 Principle

Cathodoluminescence is an optical method used in material science to identify defect and the doping level of the material. This technique is based on the light emission of the material under electron beam excitation. This light emission is due to radiative electron-hole pair or exciton recombinations. There are two kinds of excitons, the free exciton (FE) and the bound exciton (BE). A BE is a FE linked to neutral impurities (i.e dopant) with Van der Walls forces.

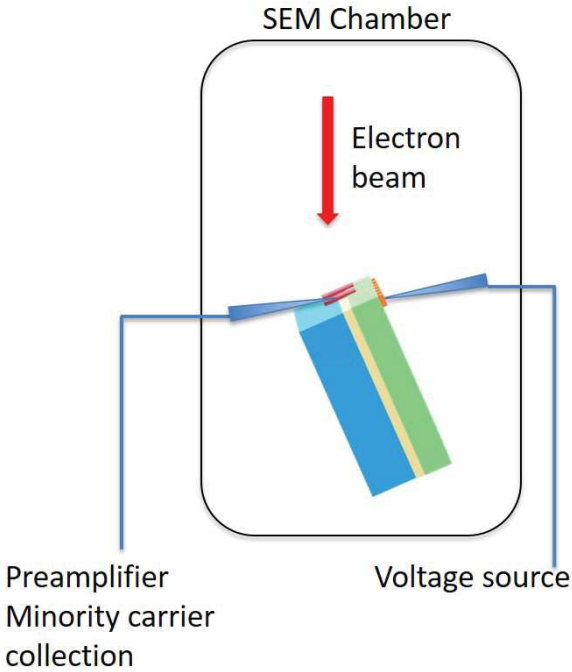

FIGURE 5.2: *Schematic EBIC setup inside the SEM*

For diamond which has an indirect band gap the radiative recombination is helped with phonon. Each transition can be related to defect type or a well known transition, most of those transitions are listed in *Optical Properties of Diamond, A Data Handbook* by A. Zaitsev. [91].

For boron doped diamond it was shown by Omnes *et al*. [92] that cathodoluminescence is a good technique to verify the layer's doping level. To do so, two transitions are observed: the FE assisted with Transverse Optic phonon (FE_{TO}) and the BE assisted with Transverse Optic phonon (BE_{TO}). Both with a precise energy which are respectively 5.268eV (λ =235.35 nm) and 5.215eV (λ =237.74 nm). This technique uses a linear relationship [92] between the boron concentration and the intensity of those 2 peaks in the diamond cathodoluminescence spectrum.

$$[B] = 3.5 * 10^{16} * \frac{I_{BE_{TO}}}{I_{FE_{TO}}} \tag{5.1}$$

Here [B] correspond to the neutral boron concentration in atom.cm^{-3}, $I_{BE_{TO}}$ and $I_{FE_{TO}}$ correspond to the maximum intensity of BE_{TO}O and FE_{TO} peak. This equation is only working for spectrum obtained at 4K, if the spectrum has been obtained at 100K the relationship proposed by Barjon *et al*. has to be used [93].

One important parameter doing cathodoluminescence as well as EBIC measurement is the electron beam acceleration energy which is linked to the probing depth. In order to have a good idea some Monte-Carlo simulations can be run thanks to the Casino software [94]. Those simulations will give the shape and the size of the interaction peer. Nevertheless, it

also gives the deposited energy inside the material as function of the depth for monocrystaline diamond (fig. 5.3). On this graph it appears that by increasing the acceleration voltage the probing depth will be higher. In that case the probing depth will be taken as the CL intensity maximum. That indicates that a measurement taken at an higher acceleration voltage will be less sensitive to the surface.

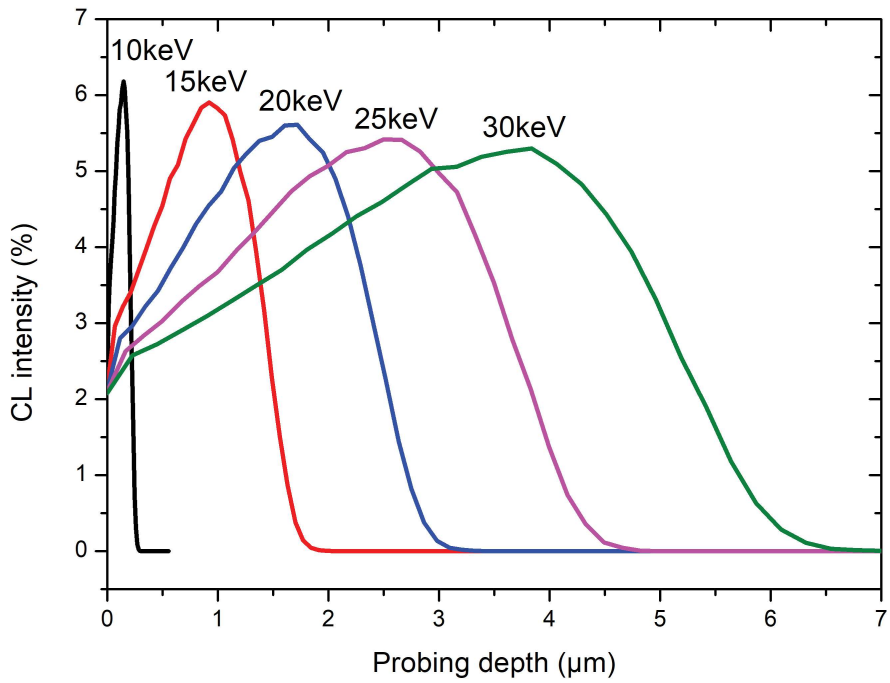

FIGURE 5.3: *Monte Carlo simulation obtained with CASINO software of the CL intensity as function of the probing depth for different e-beam acceleration voltages*

5.4.2 Results

With this information cathodoluminescence was performed at 10keV at the beginning and after at 30keV. Two kinds of measurements have been taken, first a full spectrum from 1.5 to 5.5 eV which will give information about defects and allowing to extract the doping level. The second one will be a cartography in order to see how some defects spread over the layer. Each of them are made at 4K permitting us to use formula 5.1 to extract the boron doping concentration. All presented spectra in this section are normalized with the FE_{TO} maximum intensity peak.

5.4.2.1 Full Spectra measurement from 1.5 to 5.5 eV

10 keV measurement

First spectra have been taken on the sample side with one measurement every 2 μm from the edge of the sample as shown on figure 5.4. Two of the obtained spectrum are presented in figure 5.5. The first one which has a big peak at 3.56 eV has been taken inside the substrate and the other one taken inside the p- layer. By comparing both of them, a large number of peaks is present inside the grown layer and missing from the substrate but the 3.56 eV band has a bigger intensity inside the substrate. A noticeable band is present at 4.64eV on both spectra. This was reported in 1995 by Lawson *et al*. [95] and is related to boron incorporation inside HPHT and CVD diamond. First the wide band at 2.4eV was affected to the band A defects but by running another round of measurement using a different filter it appears that this band comes from the second harmonic of the 4.64 eV band. The excitonic region from 5 to 5.5eV is also present in this graph.

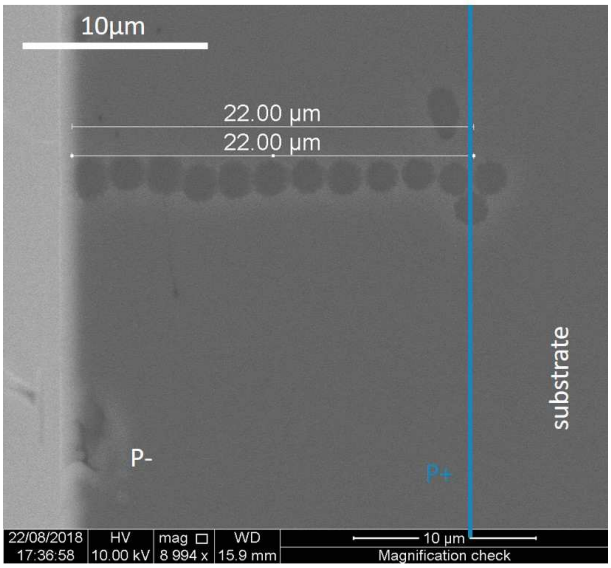

FIGURE 5.4: *Sample side SEM image with one dot for each CL measurement performed.*

A zoom is them realized on the excitonic region in order to see BE_{TO} and FE_{TO} peaks for the determination of the doping level inside the layer (figure 5.6). At every position the ratio between BE_{TO} and FE_{TO} has been measured formula 5.1 has been applied. The obtained results are presented in graph 5.7 where the obtained boron concentration is plotted as a function of the position. The boron concentration inside the layer is non-homogeneous and is value is varying from $1.5 * 10^{15}$ to $4.5 * 10^{15}$ atom.cm^{-3}. Boron concentration is higher at the interface between the p- layer and the p++ layer. This can be explained thanks to the growth process because this is a non intentionally doped layer (from chapter 2) meaning that there is no boron inside the gaseous mixture added from an external source. The boron comes directly from the p++ layer underneath and the boron concentration inside the plasma ball will be higher at the growth beginning. The second boron incorporation increase

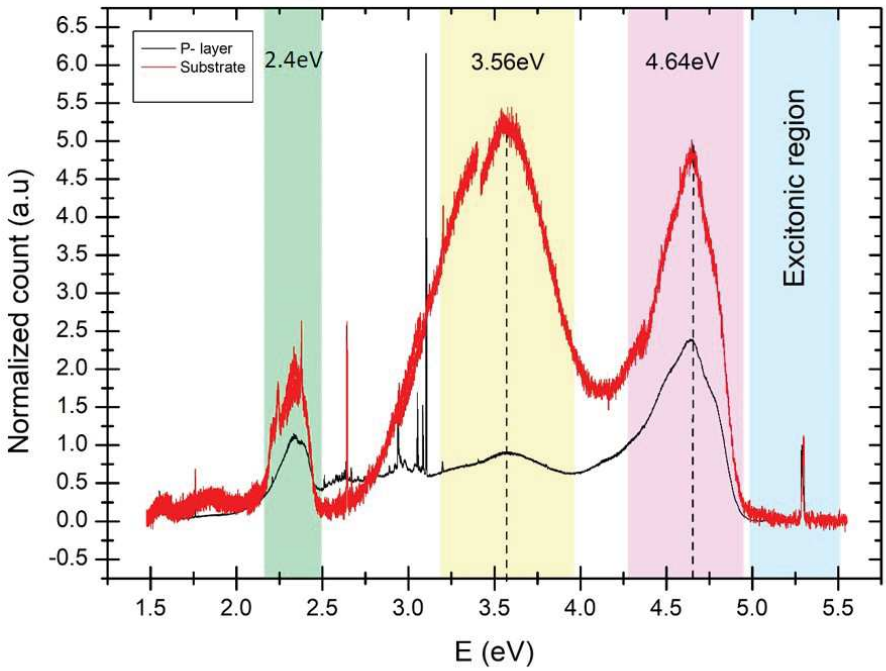

FIGURE 5.5: *Cathodoluminescence signal at 10 keV for two positions the black one inside the p- layer and the red one inside the substrate.*

can also be explained with the growth process, the decrease of the methane concentration will help the boron incorporation at the growth end.

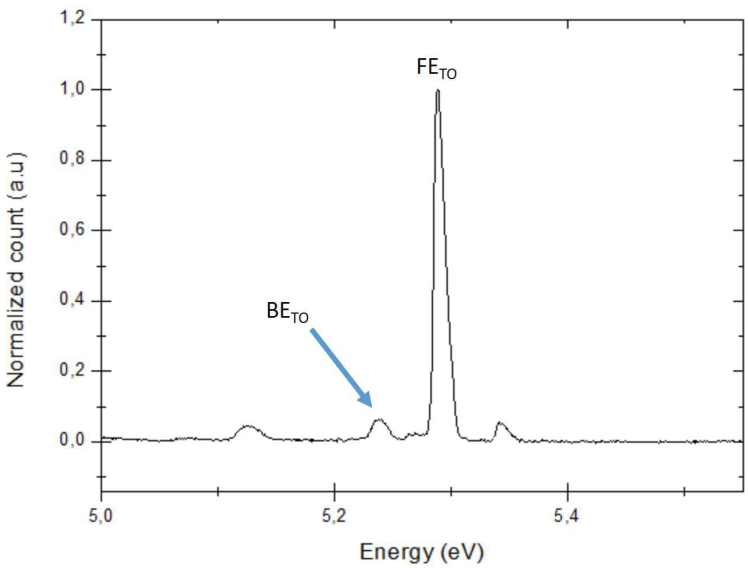

FIGURE 5.6: *Zoom on the excitonic region of the cathodoluminescence spectra obtained inside the p- layer*

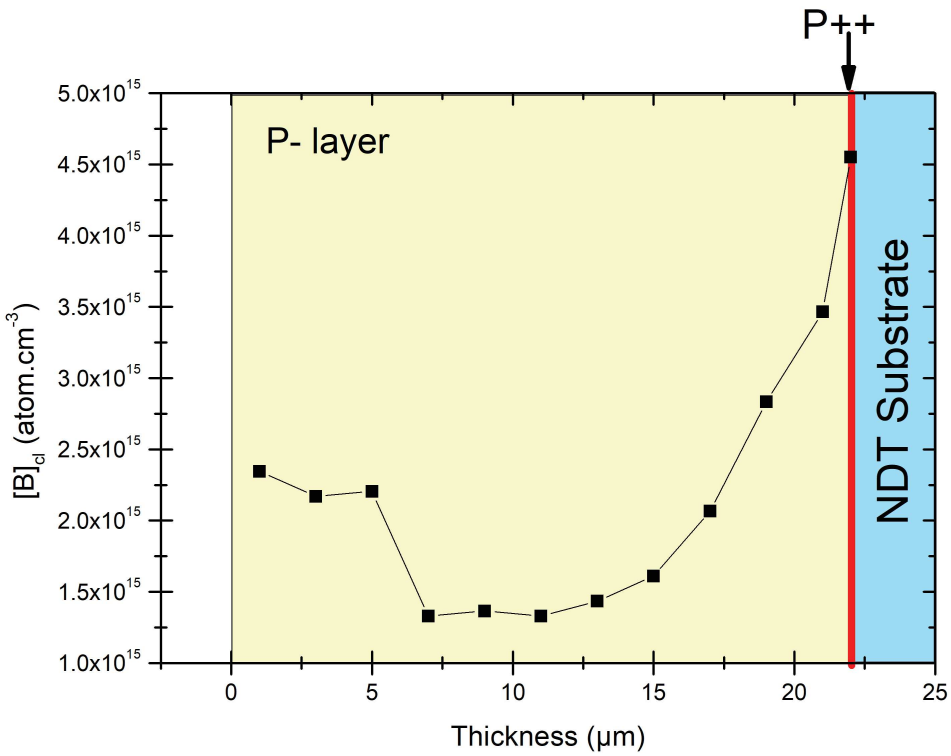

FIGURE 5.7: *Boron concentration extracted from cathodoluminescence as function of the position*

30keV measurement

As said before, the acceleration voltage has a big impact on the probing depth, as a lot of peaks where present at 10 keV which is a measurement very sensitive to the surface like surface recombination. Also some of the peaks might be related to the side polishing process. In order to discriminate those peaks the same experiment was run at 30 keV. This time the step between two measurements was 5 μm. In figure 5.8, two spectra are presented taken at the same distance from the edge than before.

Comparison between 30 keV and 10 keV measurements

Plotting on same plot both spectra obtained at the same position for two different e-beam voltage accelerations 10 and 30 keV will allow to compare them. This is done in figure 5.9. On this graph it can be noticed that the 4.64eV band is still present on both curves but the 3.58eV is missing from the 30 keV spectrum meaning that this band is related to the surface. Nevertheless, a number of narrow peaks present with a 10 keV acceleration voltage also disappears at higher beam energy. In remaining side the 2.64eV peak is present in both spectrum and it is a known peak for CVD grown diamond [91].

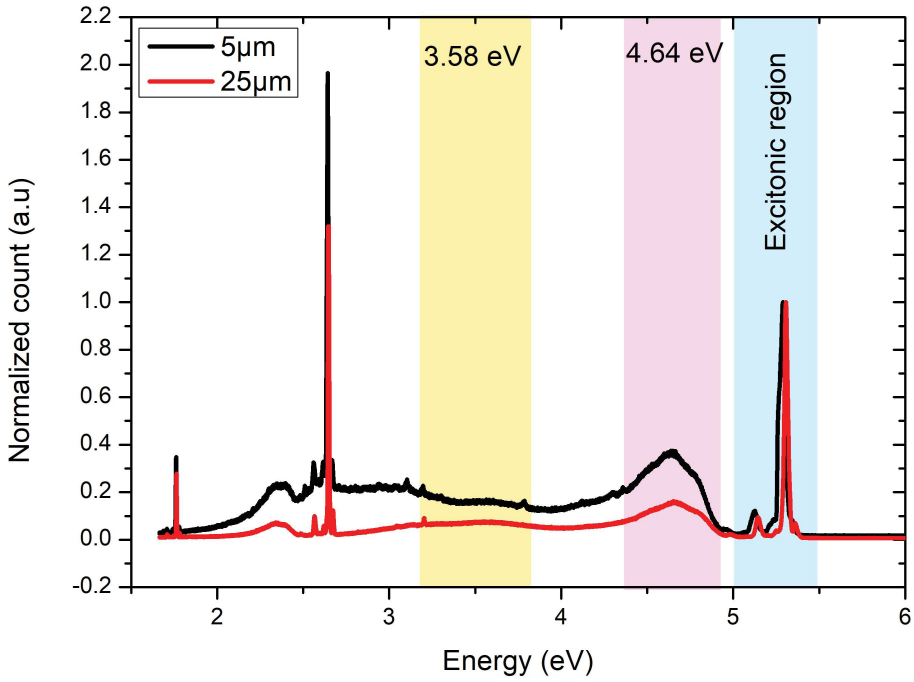

FIGURE 5.8: *Cathodoluminescence signal at 30 keV for two position the black one inside the p- layer and the red one inside the substrate.*

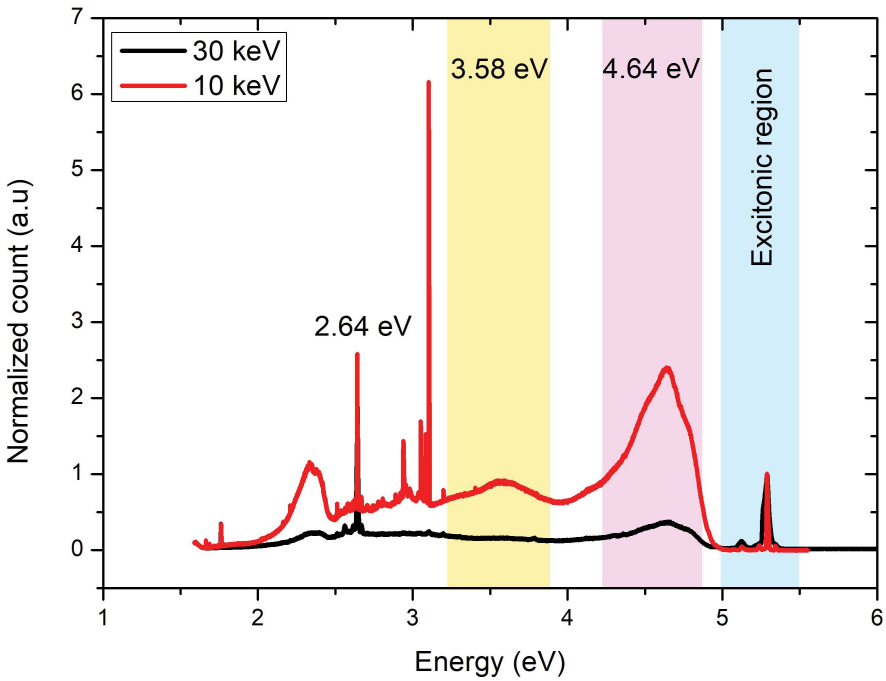

FIGURE 5.9: *Cathodoluminescence signal at 30 keV (black) and 10 keV (red) for inside p- layer.*

5.4.2.2 Cathodoluminescence mapping

With this setup cathodoluminescence mapping can also be performed in order to follow the defect distribution inside the material. Several mappings have been done for different energy range, here all of them have been done at 5keV acceleration beam and 4K. The first one presented (fig. 5.10) was performed to see the 4.64eV band. It appears that this defect is present in both substrate and the epitaxial layer, the signal is constant inside the substrate and stronger inside the p- layer. Also the peak width is visible. On the contrary in figure 5.11, we can see the two peaks, one weak at 2.9eV and a second one stronger at 3.1eV . Both of them are only present inside the p- grown layer.

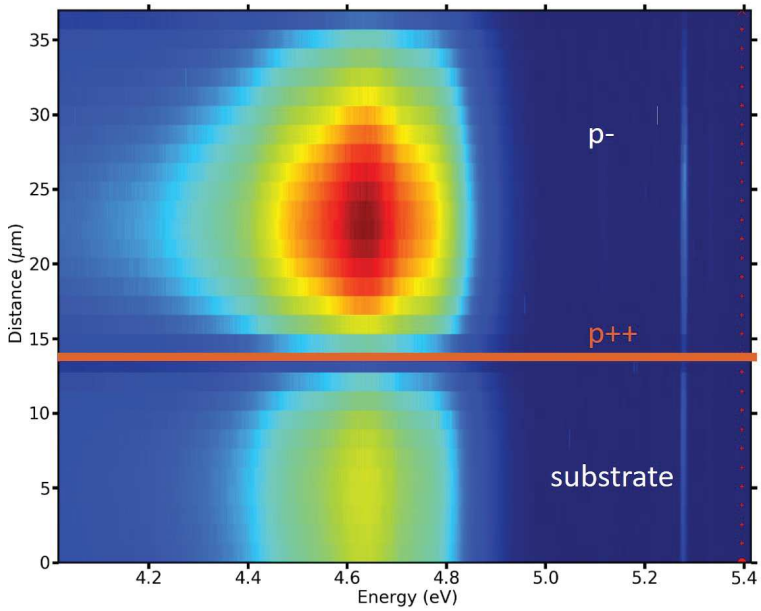

FIGURE 5.10: *CL mapping around the 4.64 eV peak, this defect is present inside substrate and the grown layer*

This technique is very useful to see the defect origin.

5.5 Electron beam induced current

In order to see the electric field inside the material, EBIC measurements were performed.

5.5.1 Principle

EBIC is a powerful tool in order to see the electrical field. It was firstly used in Silicon based integrated circuit in 1982 by Leamy [96]. As for CL this technique is based on the excitation created by an electron beam. The electron beam will bring some energy in order to create some electron-hole (e-h) pairs inside the material. The number of e-h pairs created per second can be estimated thanks to formulas [7]:

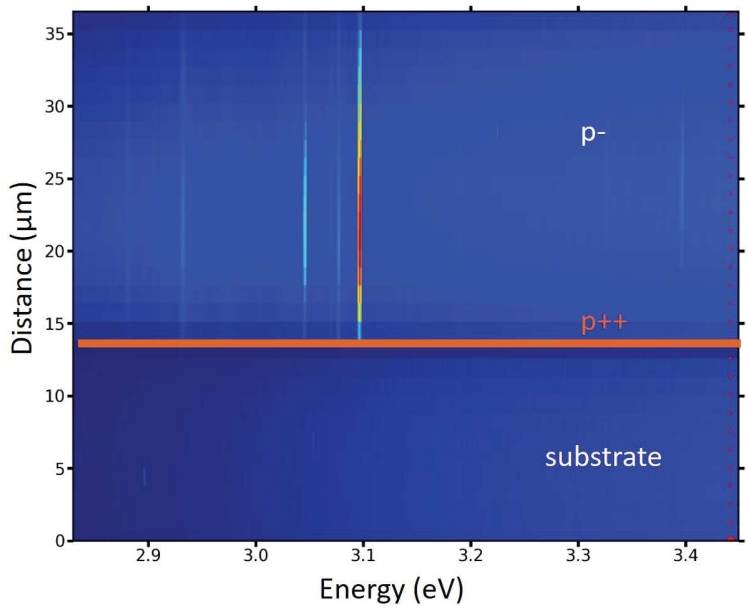

FIGURE 5.11: *3eV CL mapping, this defect is present inside substrate and the grown layer*

$$\Delta N = \frac{I_{beam}}{q} G \tag{5.2}$$

$$\text{with } G = \frac{V_{acc}}{\epsilon_{e-h}}(1-\beta) \tag{5.3}$$

with β,V_{acc}, ϵ_{e-h} and q are respectively: the energy average fraction from the incident electron beam lost by back scattering, the acceleration voltage, the average energy needed for e-h pair creation equal to 13.1 eV [97] and the electrical charge value. Following the minority carrier concentration (n) can be approximated by considering that the carrier distribution is sphere-shaped and by applying next formulas:

$$n = \Delta n.\tau_e \text{ with } \Delta n = \frac{\Delta N}{(4/3)\pi(R_e/2)^3} \tag{5.4}$$

with R_e and τ_e respectively the electron beam depth penetration and minority carrier lifetime excess. If there is no electric field inside the material these carriers will have two options to recombine or to drift to a recombination site. In that last situation no current will be created. In the case of Schottky diode an electric field is present even at 0 bias called the internal electric field. Inside this electric field those charge carriers will be separated, electrons will go in one direction and holes will go in the opposite direction. In that case an electrical current will be created and called the EBIC current. This current can be measure thanks to the minority carrier collection, for p-type diamond it will be electrons. They will drift and diffuse. All mechanism used in EBIC are summarized in figure 5.12. On this schematic the e-h pair are created under the electron beam influence. After the separation due to the electric field the electrons will be drifting and diffusing.

The minority carrier collection is possible thank to an high resolution ammeter.

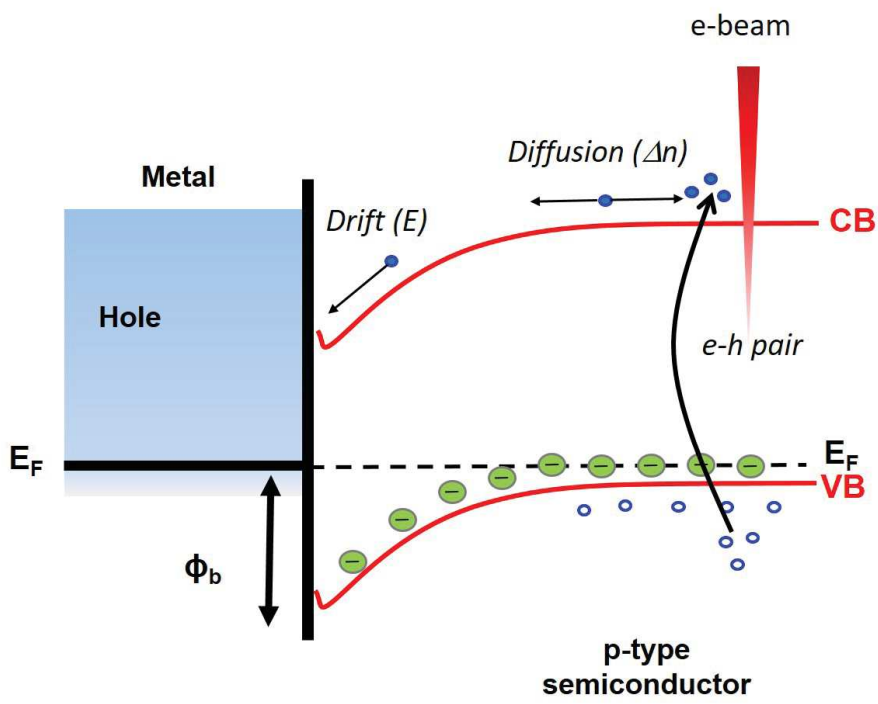

FIGURE 5.12: *EBIC schematic principle in the case of p-type semiconductor, here electrons are considered as minority carriers*

In this work the electric field was investigated in the depth of diamond Schottky diode. To ensure that the sample was properly insulated from the SEM stage in order to avoid leakage path sample was glued on an alumina plate. Then different measurements were performed. First of all, in order to see the electric field expansion some EBIC images have been taken. After EBIC current measurement was done to extract some properties such as the depletion width (w) which is related to the layer doping level. Also some experiments have been run in order to see the electron beam impact on the Schottky diode I-V characteristic. And at the end, the minority carrier life time was investigated.

5.5.2 Diamond Schottky diode electric field distribution

During this first section the focus will be put on the visualization and the characterization of the electric field underneath a Schottky contact. First of all EBIC images have been realized and after extraction of the depletion width was done.

5.5.2.1 EBIC image

In order to obtain EBIC image of the electric field, a non leaky Schottky diode was chosen. On this diode a reverse bias was applied between 15 and 600V (setup limitation). For each applied bias an image was taken. For low reverse bias measurement between 15 and 175V, the electron beam characteristics was 30keV acceleration voltage and a spot size 1.

Obtained images are presented in figure 5.13 and acquisition parameters in table 5.1. On the first picture (15V) a thin light grey area is visible this area will increase when the reverse bias is increasing. This area corresponds to the electric field extension. The electric field extension is not the same at every point along the Schottky contact i.e the electric field is not homogeneous. This can be an indication for a local variation of the doping level or a non homogeneous interface between Schottky metal and diamond. Some hot spots are also appearing along the contact indicating the presence of defects. [49].

TABLE 5.1: *Parameters used to performed EBIC from -15 to -175V*

Parameters	-15V	-25V	-50V	-75V	-100V	-175V
Offset	+100nA	+100nA	+100nA	+100nA	+200nA	+200nA
Sensitivity	100nA/V	100nA/V	100nA/V	100nA/V	100nA/V	100nA/V
Acquisition time	100μs	100μs	100μs	100μs	100μs	100μs

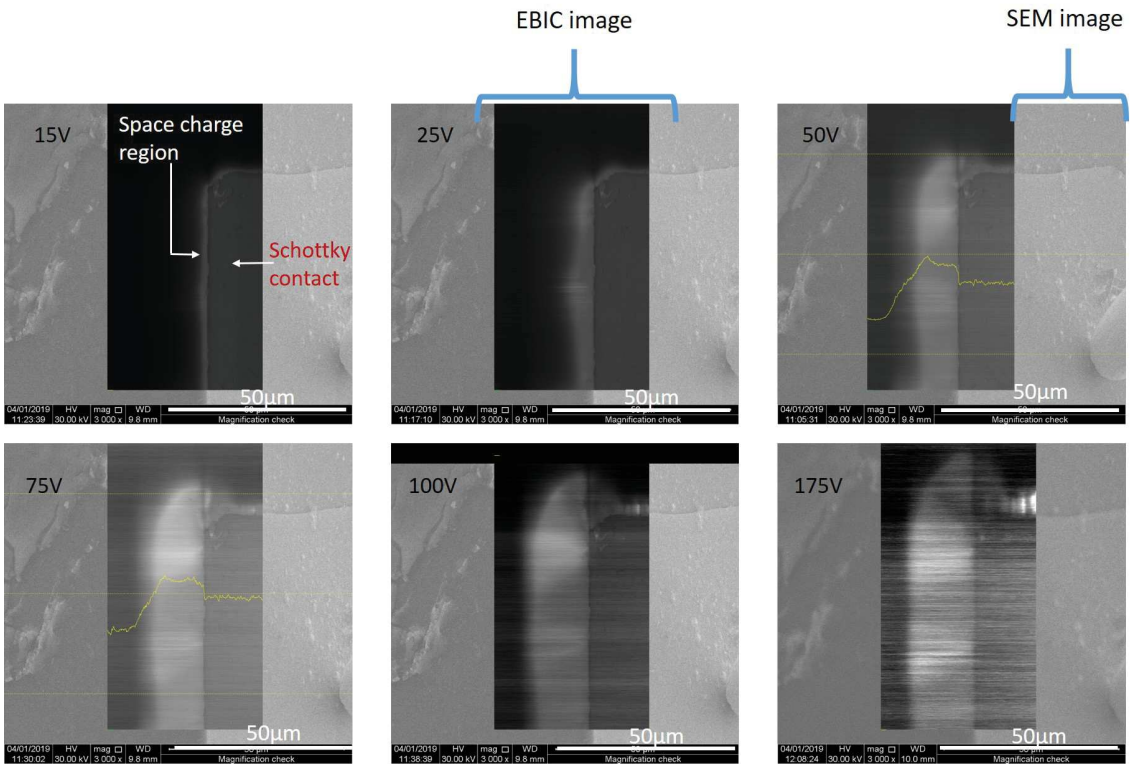

FIGURE 5.13: *Space charge region EBIC image obtain at different bias from 15 to 175V under a 30keV e-beam and a spot size 1*

More measurements have been done after by increasing the reverse bias from 200 to 600V. For those measurements the electron-beam was at 30keV and with a spot size 5 and other acquisition parameters are summarized in table 5.2. EBIC images for this reverse bias are presented in figure 5.14. Here the electric field seems not to extend anymore. In order to confirm that EBIC measurement will be presented in the next section which allows to have

the precise extension width. A hot spot also appears on top of the Schottky contact and one in the middle. One explanation is that the ohmic contact is placed on top of this Schottky contact creating a preferential path and increasing the electric field at this point.

TABLE 5.2: *Parameters used to performed EBIC from -200 to -600V*

Parameters	-200V	-250V	-300V	-400V	-500V	-600V
Offset	+10μA	+5μA	+20μA	+10μA	+10μA	+20μA
Sensitivity	10μA/V	5μAA/V	20μA/V	10μAA/V	10μAA/V	20μA/V
Acquisition time	100μs	100μs	100μs	100μs	100μs	100μs

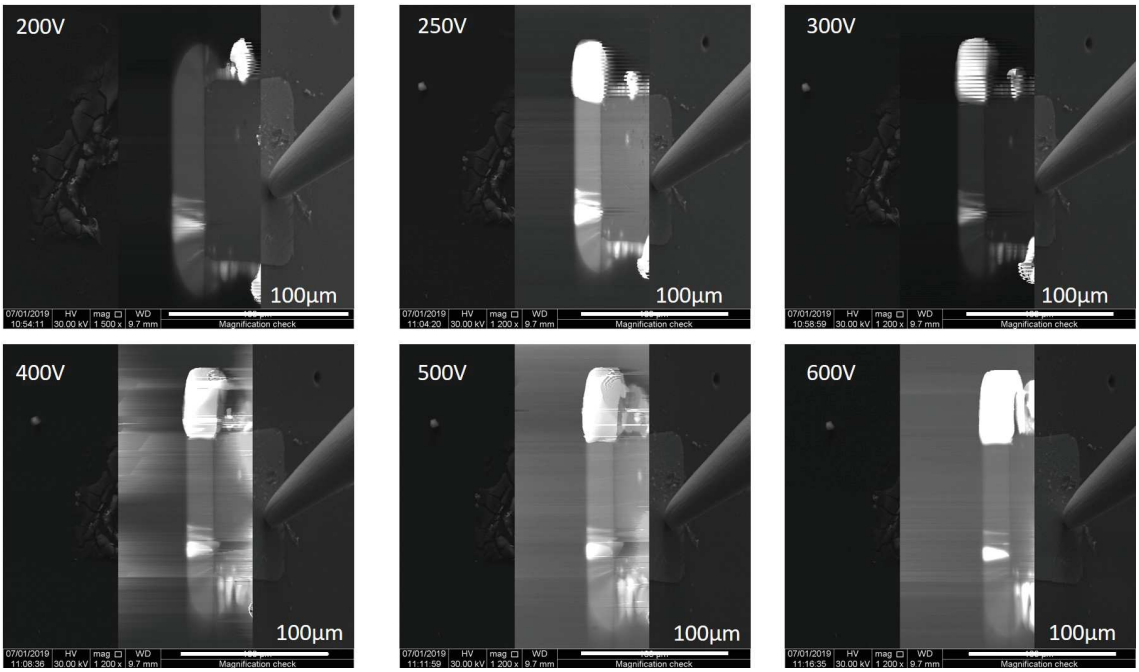

FIGURE 5.14: *SCR EBIC image obtain at different bias from 200 to 600V under a 30keV e-beam and a spot size 5*

5.5.2.2 Depletion width and doping level determination

As shown on the different EBIC images presented above, two different space charge regions (SCR) can be studied, the transverse and the lateral one as shown on figure 5.15.

Each SCR has been measured for each reverse bias, some of them are presented in figure 5.16. On this graph the space charge region starts at 0 which is defined as the Schottky contact edge and expanse is negative distance, the used distance takes into account the angle of measure presented in the setup presentation section. Like on the EBIC images showed previously, the SCR width is increasing with the reverse bias.

After the SCR width is plotted as function of the reverse bias to see its evolution. The obtained graph is presented in figure 5.17. On this graph the transverse SCR is plotted with

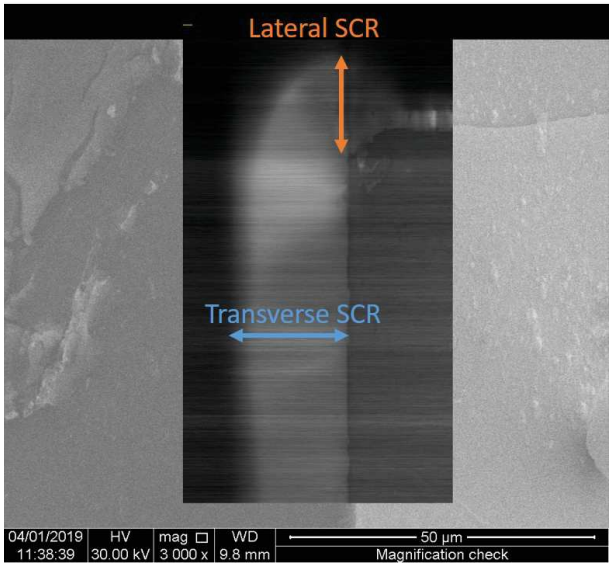

FIGURE 5.15: *EBIC image with two arrows representing the transverse and the lateral SCR*

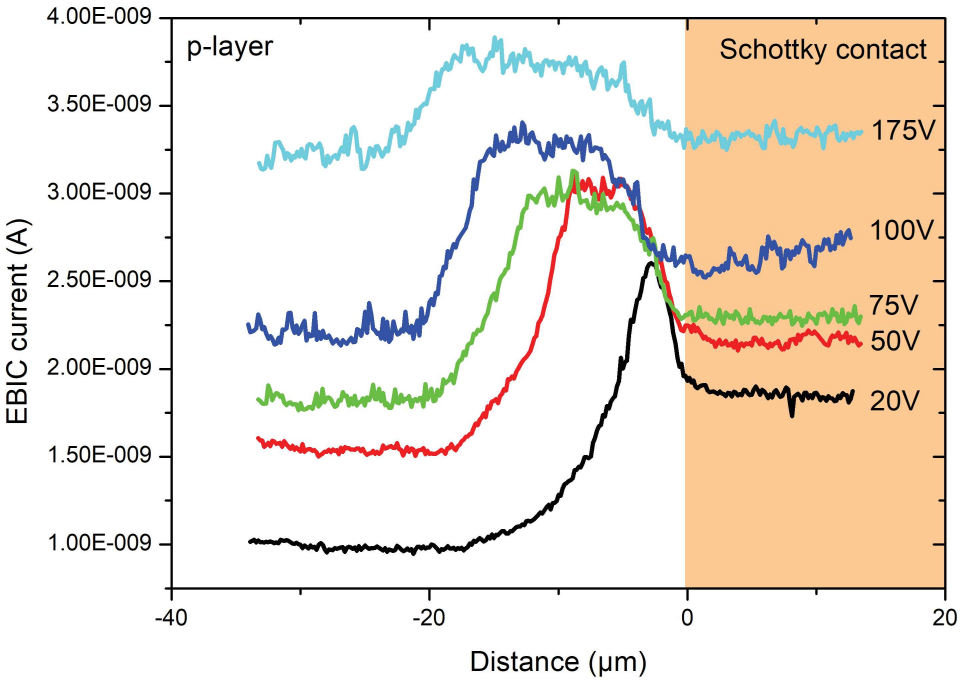

FIGURE 5.16: *EBIC current measurement obtained at different reverse bias as function of the corrected position (i.e taking into account the angle of measure)*

blue square and the lateral one is plotted with orange triangle. A difference between both SCR is highlighted in this graph, the transverse one is reaching a limitation at 200V while the lateral one is still increasing. This can be explained with the diode architecture. The p- layer thickness is about 20μm, with a low doping level, in that situation the diode is in the punch through situation as presented in chapter 1, the electric field is getting to the p++ layer and can not expand anymore. On the contrary the lateral SCR does not meet any barrier and can continue to expand.

The space charge region width can express as follow:

$$w = \sqrt{\frac{\epsilon_0 \epsilon_r V}{q(N_a - N_d)}} \tag{5.5}$$

with w the SCR width in meter, $(N_a - N_d)$ the effective doping level in atom.cm^{-3}.

On this graph some simulated SCR widths are also plotted for 3 different effective doping levels $2 * 10^{14}$, $3 * 10^{14}$ and $4 * 10^{14}$ atom.cm^{-3}.

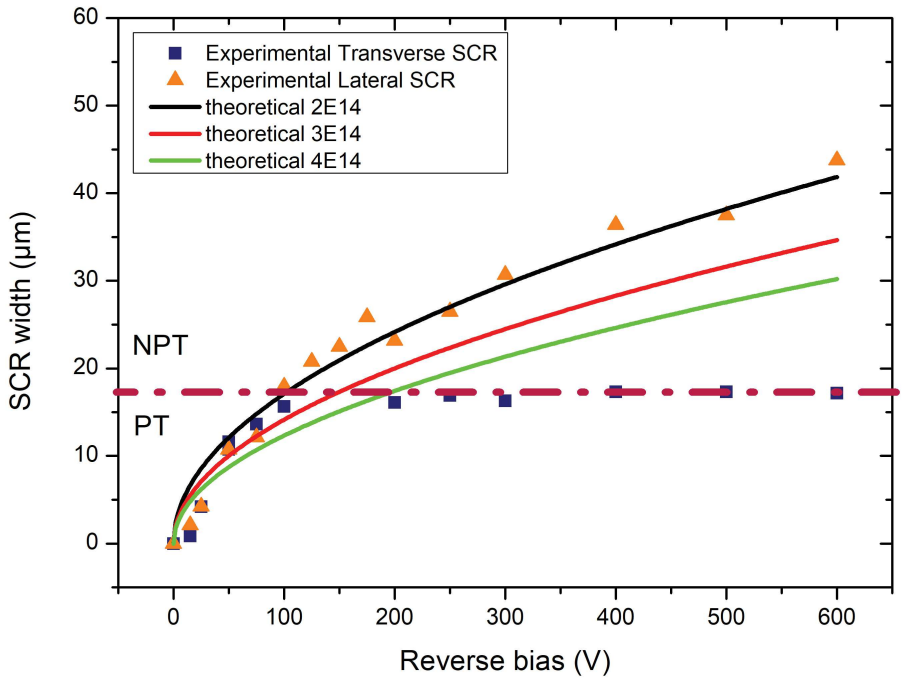

FIGURE 5.17: *Transverse (blue square) and lateral (orange triangle) space charge region (SCR) extracted from experimental data for different reverse bias and plotted as function of the latest. Also simulated curves as function of 3 different doping level*

Finally by comparing the experimental data obtained for the lateral SCR and the simulated curve, the layer effective doping levels can be extracted. In the present case the effective doping level can be estimated at 2.10^{14} atom.cm^{-3}.

5.5.2.3 Vertical EBIC scanline

After performing some horizontal scanlines to see the SCR, vertical scan line have been performed to verify the electric field homogeneity underneath the Schottky contact. For a fixed reverse bias several scan have been taken at 5, 10, 25, 20 μm.

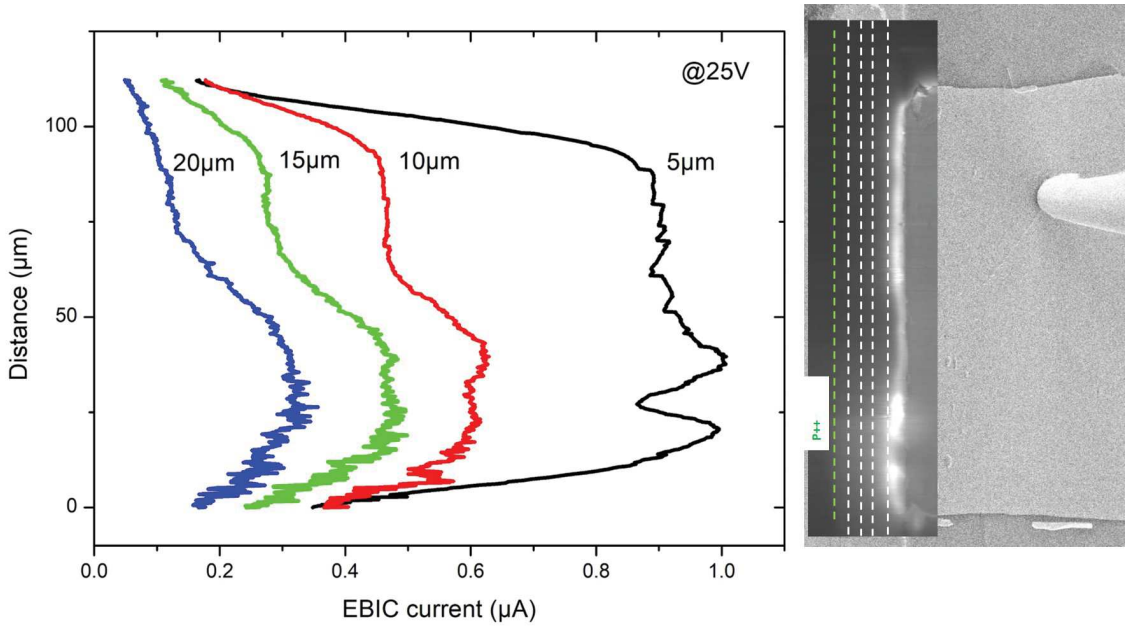

FIGURE 5.18: *EBIC Scanline obtained for different distances from the Schottky diode and the EBIC image associated for 25V reverse bias*

As it clearly appears on the EBIC image that the electric field is not homogeneous. On the graph presented in figure 5.18, on the 5μm curve 2 peaks are present instead of a plateau indicating a homogeneous EBIC current bellow the contact.

5.5.3 I-V characteristics under different conditions

Once the electrical field has been studied and characterized. This work will now focus on the impact of electron beam on the electrical characteristics of a diamond Schottky diode. In order to achieve this goal different parameters will be tuned: the electron beam energy, the beam spot size and finally the beam position on the substrate. SEM image in figure 5.19 listed the different positions used in this study from 1 to 4, here each point is separated with 5μm (i.e 5, 10, 15 and 20 μm), this will be used in section 5.5.4.

5.5.3.1 Electron beam energy influence

Firstly, the electron beam energy was investigated, for that I-V characteristics were performed at the same position, in that case the position 2, with the same beam spot size and only the electron beam energy changing from 5keV to 30keV. Obtained results are presented in the next graph (fig. 5.20). On this graph it appears that leakage current is increasing

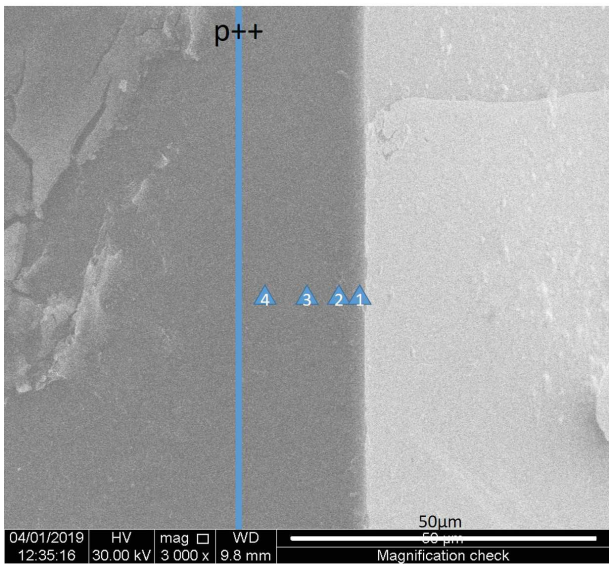

FIGURE 5.19: *Device SEM image indicating the four position taken numbered 1 to 4 in order to realized the electrical measurement*

with the electron beam energy. A plateau appears around -50V indicating that the full EBIC current is collected.

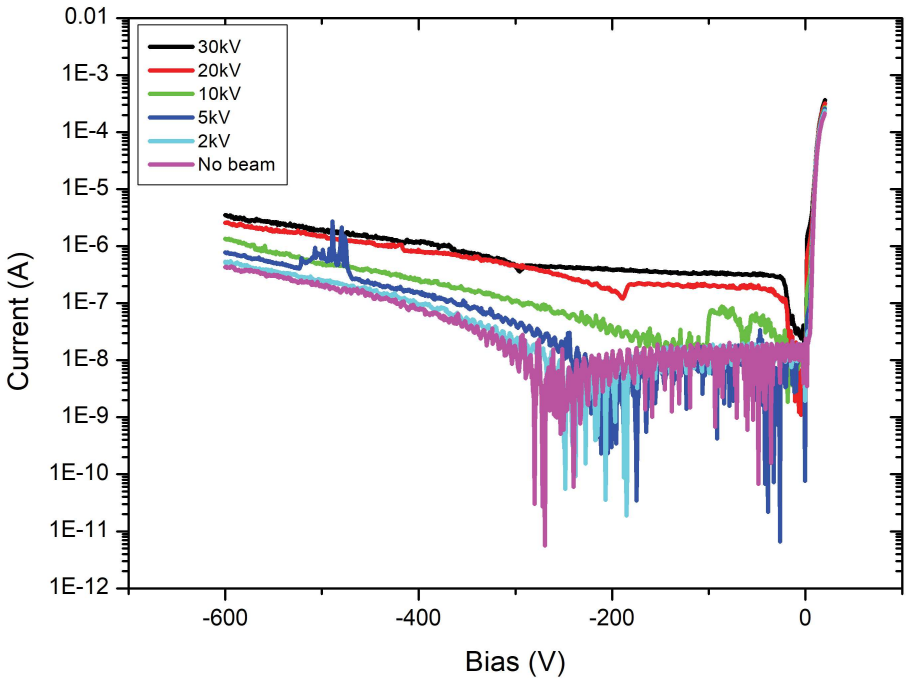

FIGURE 5.20: *I-V characteristics obtained under different conditions, here changing the electron beam energy from no beam to 30keV at the same position and with the same beam size*

5.5.3.2 Spot size influence

Another set of measurements was performed but this time keeping the same beam energy, in that precise case 30keV, the same position and changing the beam spot. Those I-V characteristics are shown in figure 5.21. It appears that the reverse current is increasing with the spot size. For a given beam energy the spot size is related to the electron beam current, when the spot size increase the beam current is also increasing.

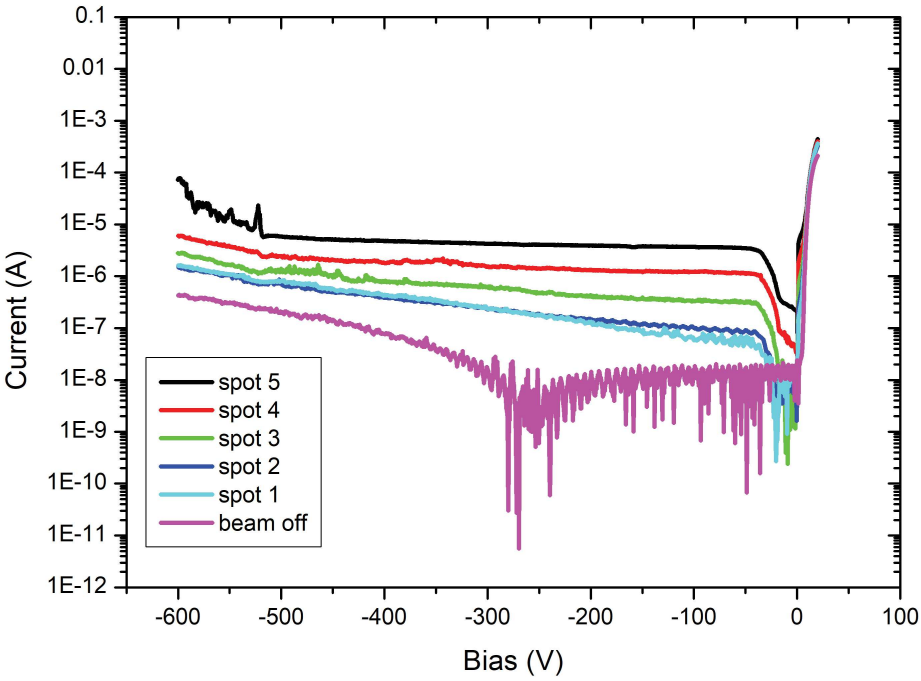

FIGURE 5.21: *I-V characteristics obtained under different conditions, here changing the spot size from 0 to 5 at the same position and with an 30kV energy beam*

From the previous graph, the diode current can be extracted for a specific bias and for the different spot size. That have been done and presented in graph 5.22. In our situation the extracted currents have been taken at -100V before reaching the punch through condition. A linear relationship appears between the diode current and the beam current.

For a diode under an electron beam the obtained current can be expressed as follow:

$$I_{diode} \approx \frac{E_{beam}}{E_{e\text{-}h}} * I_{beam} \tag{5.6}$$

with in this equation I_{diode}, I_{beam}, E_{beam} and $E_{e\text{-}h}$ standing respectively for the diode current, electron beam current, the beam energy (eV) and finally the energy needed to create an electron-hole pair inside the diamond (eV).

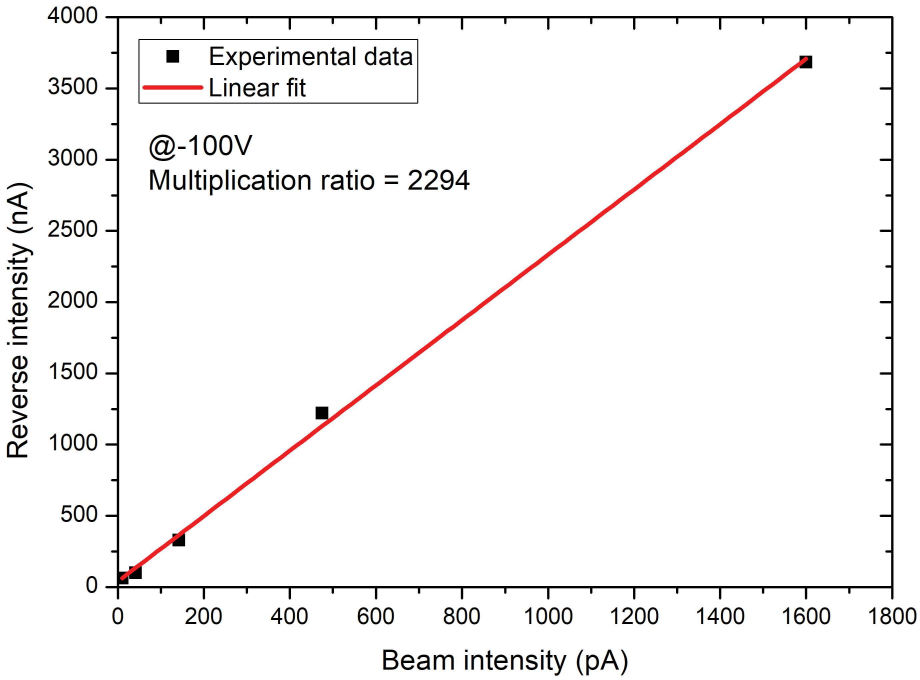

FIGURE 5.22: *Reverse diode current obtained at -100V plotted as function of the electron beam current*

So by applying a linear fit on the experimental data it is possible to find the electron hole pair creation energy. A 2294 multiplication ratio is extracted and with the formula mentioned above (5.6), taking the 30kV energy beam into account, we find an electron-hole pair creation energy of 13.08eV. This results is in good agreement with the expected value of 13.1eV [97]. This obtained value also indicates that we have a minority carrier full collection.

5.5.4 Beam blanker measurement: A way to determine carrier lifetime inside a p- layer

Another experiment has been run on this sample with a beam blanker. The beam blanker will permit to deflect the electron beam with a defined periodicity with this technique the sample is not always under the electron beam influence, allowing to see the effects as function of the time. Here the EBIC current is measured as function of time and for the different electron beam positions presented below (5, 10, 15 and 20 μm from the Schottky contact) . In this setup the injection time is defined by the beam blanker setup parameters. In our case the injection time is defined at 2.1 ms and the we are measuring during 3.5 ms. During this time the diode is bias at -10V. In this conditions we assumed that only diffusion occurs. The current is measured with a Tektronix DPO 2014B Oscilloscope with a 1MΩ resistance at the entrance and a 200 MHz bandwidth.

Those results are presented in figure 5.23. During the injection time, the current is increasing until reaching the maximum. After when the beam is deflected the EBIC current is decreasing until reaching 0. From the different positions it appears that the equilibrium state on the first phase is not achieved at the same speed and the EBIC current is higher when the beam is closer to the Schottky contact (5μm curve).

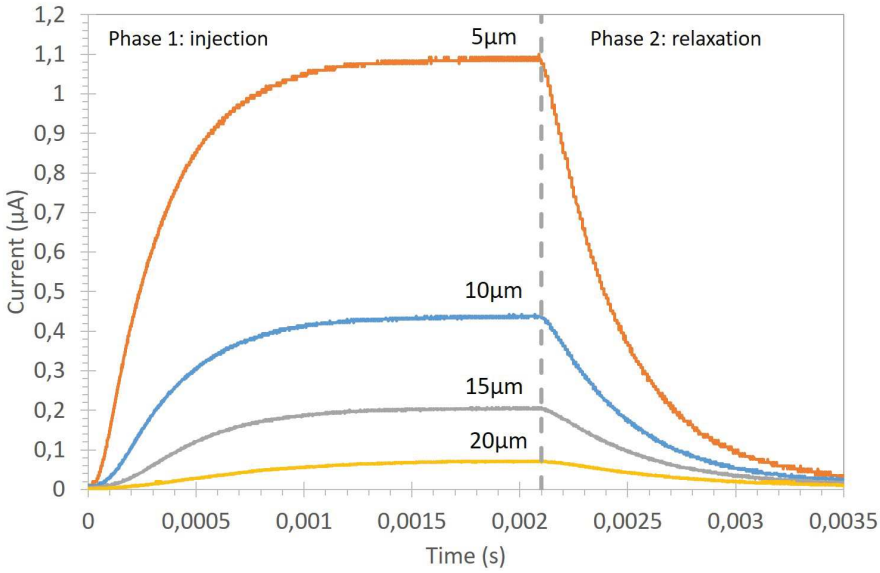

FIGURE 5.23: *EBIC current as function of time and for different positions. The injection time is 2.1 ms and the diode is biased at -10V*

After the maximum current reached at each positions is plotted as function of the distance from the ohmic contact as shown in figure 5.24.

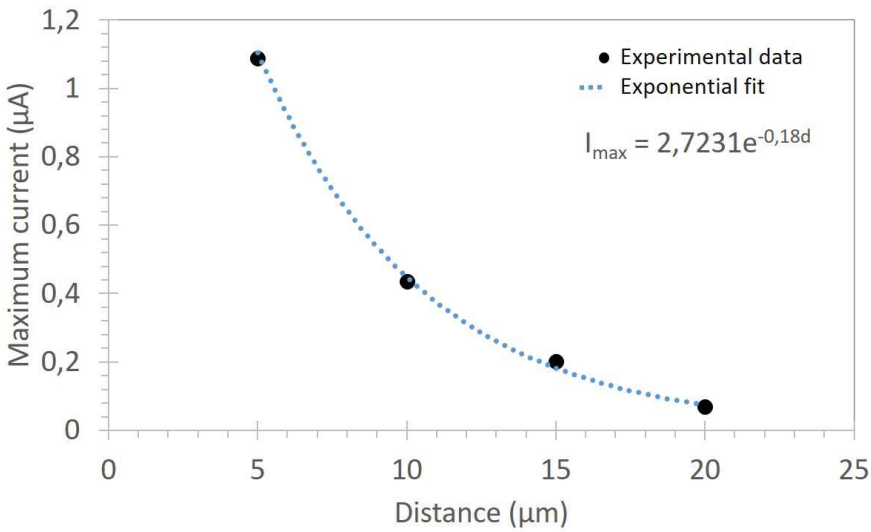

FIGURE 5.24: *Maximum currents extracted from the previous measurements as function of the Schottky contact distance*

With this graph the minority carrier diffusion length can be extracted. Normally the minority carrier diffusion length can be express as follow:

$$L_D = \sqrt{D_n \tau} \text{ and } D_n = \frac{kT}{q}\mu_n \tag{5.7}$$

with L_D the diffusion length, D_n the minority carrier diffusion coefficient, μ_n the minority carrier mobility and τ the lifetime.

But an other way is to fit the previous graph with an exponential decay:

$$I_{max} = A.exp\left(\frac{-x}{L_D}\right) + cte \tag{5.8}$$

By applying this method a 5.6 μm diffusion distance is found. This value is in good agreement with the expected one for this doping level.

5.6 Conclusion

From this sample lots of experiments has been run with different techniques which are cathodoluminescence and electron beam induced current measurements. CL measurement give us information about the layer doping level and defects present inside it. EBIC measurements performed on the sample which have never been done in the diamond community give us access to a lot of new information. For example we have been able to visualize a Schottky diode space charge region into its depth and see how it was evolving with the increase of the reverse bias. It appears that under the Schottky contact the electric field is not homogeneous. I try to combine CL with EBIC to see if this non-homogenous field can be linked with a defect from the CL spectrum but no difference appears as shown in figure 5.25

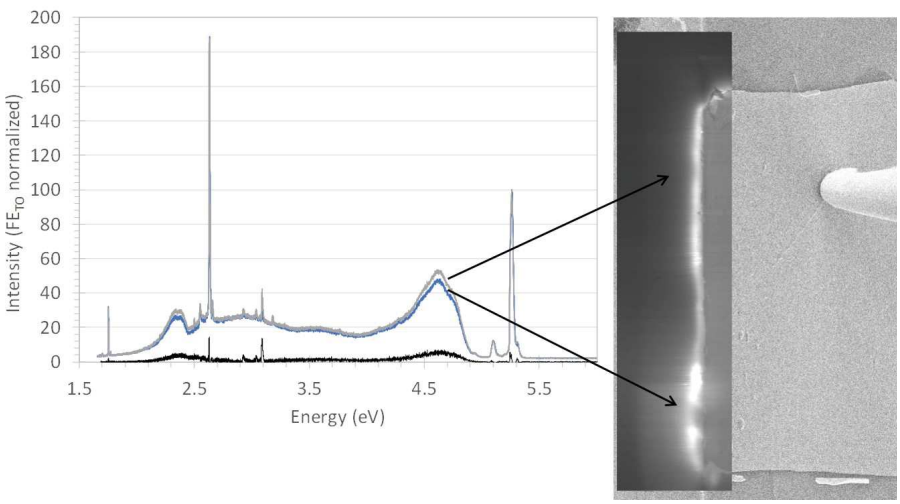

FIGURE 5.25: *Combination of CL (left) and EBIC (right) measurement to try to understand the non homogeneity of the electric field underneath the Schottky contact, EBIC black curve correspond to the substrate EBIC measurement*

Following experiments should be done to try to have a better understanding of this phenomena. From the EBIC measurements the doping level has been extracted from the space charge region profile as well as the minority carrier diffusion length. More analysis should be performed on those time resolve measurement to have a better understanding.

Chapter 6

Heteroepitaxial diodes

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One recurrent criticism for diamond as a replacement of silicon devices is the small size of available substrate. On this last chapter, a new type of diamond substrate obtained by heteroepitaxial growth will be investigated in order to see if they are suitable for diamond power devices because heteroepitaxial growth can be a good approach for increasing the substrate size.

6.1 Introduction about hetereoepitaxy

In big size diamond wafer quests to compete with the silicon wafer, one way is to use heteroepitaxy. Heteroepitaxy consists to grow diamond on top of an other material as presented in the previous chapter (chap.2, figure 2.3). At the beginning silicon substrate was used and followed by β silicon carbide, boron nitride and finally iridium which showed the best feature thanks to its 7.1% lattice mismatch with diamond and its high epitaxial rate over 90%. Iridium has to be deposited on a substrate and several candidates are available. To see which is the best, some key parameters have to be taken into account such as the crystalline structure, the lattice mismatch and the thermal dilatation coefficient between these different substrates and Iridium. All of them are summarized in table 6.1 for different substrates like magnesium oxyde (MgO) [98], Strontium titanate ($SrTiO_3$) [99], Aluminum oxyde (Al_2O_3) [100], Yttria-stabilized zirconia on silicon (YSZ/Si) [101] and Strontium titanate on Silicium ($SrTiO_3$/Si) [102] used by different research group.

TABLE 6.1: *Summary of key parameters for different substrates with Iridium, when there is a * it is between the 1st material and Ir*

Substrate	MgO	$SrTiO_3$	Al_2O_3	YSZ/Si	$SrTiO_3$/Si
Crystalline structure	cubic	cubic	hexagonal	cubic	cubic
Lattice mismatch in %	9.6	1.7	23.9	25.4*	1.7*
Thermal dilatation coefficient ($10^{-6}.K^{-1}$)	12.4	7.4	3.7	2.6	2.6

Looking at this table 6.1, the best candidate seems to be $SrTiO_3$/Si by having the same crystalline structure as well as the lowest lattice mismatch and lowest thermal dilatation coefficient. However for heteroepitaxial diamond the dislocation density is about $10^8 - 10^9\ cm^{-2}$ [103] which is far bigger than the one obtained by homoepitaxial growth which is $10^3 - 10^4\ cm^{-2}$.

Heteroepitaxy grown diamond is already available commercially by different companies *Adamant Namiki precision Jewel co. Ltd* in Japan and *AUDIATEC (Augsbourg diamond technologies GMBH)* in Germany. The last one reported a single 92 mm diameter free standing crystal grown by heteroepitaxy [104].

Some working devices made from heteroepitaxial diamond have been reported in the literature. The first MESFET was done in 2003 by Mathias SCHRECK group [99] on bulk $SrTiO_3$. After MISFET was produced on Ir/$SrTiO_3$ (bulk) and reported by YOKOTA *et al.* in 2007 [105] and the National Institute of Advanced Industrial Science and Technology (AIST) in Japan worked on P-i-n and Schottky diodes [106, 107].

DIAMWAFEL's aim project founded by the french research agency, is to propose a suitable diamond heteroepitaxial layer for industrial diamond power devices. For all the reasons explained above the stack proposed for the project is Diamond/Ir/$SrTiO_3$/Si which seems to be the best candidate. In order to check the material suitability and to compare it with what already existed for homoepitaxially grown diamond device, this work proposes

to translate what is working from homoepitaxial diode to heteroepitaxial ones and by taking into account all the difficulties working with such material and other unknown parameters.

In this chapter the stack realization (section 6.2) with all the partners involved and the first device fabricated with the adapted method from chapter 2 and its characterization will be presented to see if this material is suitable or not for power devices applications.

6.2 Sample structure

The stack used during the DIAMWAFEL project is presented in the figure 6.1.Each layer is grown by one of the project partners.

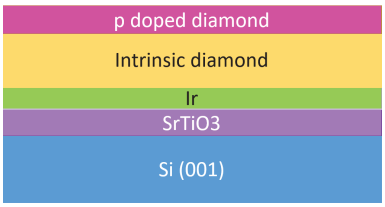

FIGURE 6.1: *presentation of the stack used for the DIAWAFEL framework*

6.2.1 $SrTiO_3$ layer

The starting point is a (001) oriented 500 μm thick silicon wafer. On top of this wafer is deposited a $SrTiO_3$ layer, that was made by the *Institut of nanotechnologies of Lyon (INL)*. $SrTiO_3$ was deposited by molecular beam epitaxy (MBE) using Knudsen effusion cells for co-deposition of strontium and titanium, the main parameters are a 400 °C temperature, a $6.65 * 10^{-8}$ mBar pressure and a 1.5 monolayer/min speed ; more details about this can be found in the previous work published by Saint-Girons *et al*. [108]. The deposited layer thickness was 38.6 nm and with a 1.5° mosaicity all this measurement have been obtain by X-ray diffraction.

6.2.2 Iridium deposition

On top of $SrTiO_3$ a thin Iridium film was grown, by the CEA Saclay, by e-beam evaporation on a 5 by 5 mm^2 piece of the wafer. The method used is explained in details by Lee *et al*. [109]. In the same time, work is done to deposit iridium on bigger size wafer, at the moment 10 by 10 mm^2 are under consideration. For this particular deposition condition were 1nm/min deposition rate, a 660°C temperature and a pressure lower than 10^{-6} mBar. The epitaxy was confirmed by SEM and the crystalline orientation by X-ray diffraction (XRD), in that case the orientation is mostly (001) as shown in figure 6.2.

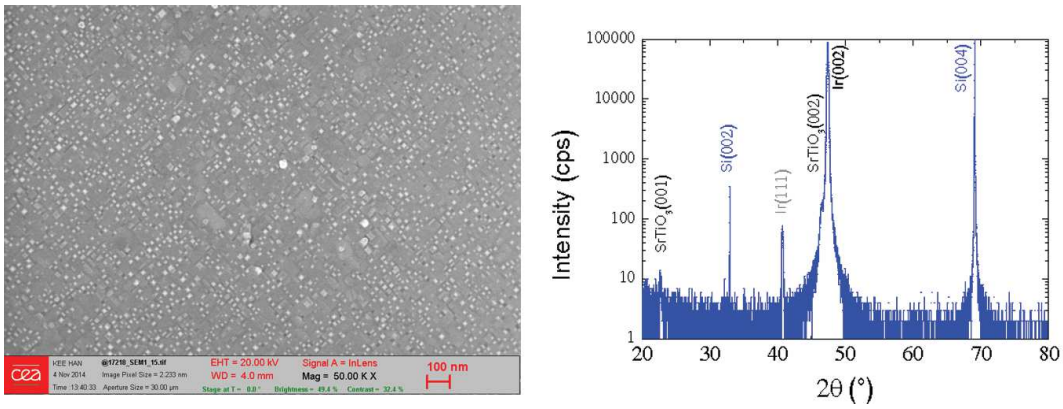

FIGURE 6.2: *Left SEM of the Ir Layer, on the right the XRD characterization with $\theta/2\theta$ scan courtesy of CEA list and INL*

6.2.3 Intrinsic diamond

Bias enhanced nucleation (BEN) is performed to start the diamond growth in MPCVD reactor. BEN principle consists to apply a negative bias on the sample holder to create a potential difference between the chamber and the sample inside the plasma ball. The positive species (i.e $C_xH_y^+$) will be accelerated through the surface of the sample. Under certain conditions nuclei will be created at the surface, the goal is to have a lot of nuclei close to each other and homogeneously spread on the substrate to ensure a good epitaxial growth .

The BEN conditions for this sample were: 45 minutes growth with a 607V bias voltage on the sample, microwave power of 400W, with a 4% CH_4 into the volume of H_2, the total pressure inside the growth chamber was 20mBar. Following the BEN process MPCVD as explained in the previous chapter was performed in two different laboratories. The first one, done by CEA and the second one by the Laboratoire des Sciences des Procédés et des Matériaux (LSPM). The first layer grown is called the template layer and was grown in the same reactor than the BEN process for 2 hours at a 200mbar pressure with a 0.6% CH_4 content of the volume in H_2 and a 400W microwaves power. The expected thickness is about 200 nm. The second layer was grown by the LSPM following the process developed by Achard *et al*. [110] The goal of this overlayer is to obtain a thicker diamond layer. The growth condition were at 4% methane concentration in hydrogen, the overall pressure was 200mbar and a 3000W microwave power. After these two growths an estimated 240 μm thick layer is obtained.

6.2.4 p-doped layer and diodes

To finish the stack a boron doped layer was grown. Growth conditions are given in the summary table in chapter 2 (table 2.1). The targeted thickness was about 1.6 μm and the doping level about $1.10^{16} atom.cm^{-3}$. Surface characterization had been performed and an average roughness of 30.40 nm was measured. Defects are present on the entire surface especially at the edge of the sample as visible on the micrograph in figure 6.3 left part and with the profilometry image on the right side it is possible to determine defect kind. In this

case with this particular shape of square base pyramid defects can be identify as pyramidal hillocks [111]. The average defects height is about 500 nm and the highest ones around $1\mu m$.

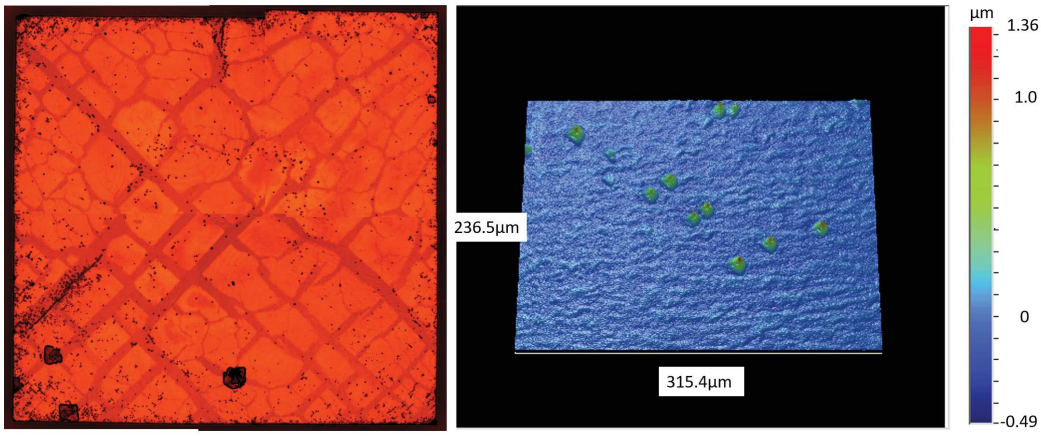

FIGURE 6.3: *On the left sample's optical micrograph obtain with orange filter (UV), dark spots are defects and after investigation cracks are below diamond layers and on the right profilometry image obtain in VSI mode*

Only one doped layer was grown in order to create lateral Schottky diodes. The purpose was to check if this stack could be suitable for doing power electronics devices.

To realize lateral Schottky diodes the same process is used than the one presented in chapter 2 without the etching step. The chosen design is presented on the figure 6.4 with the mask and the device final picture. This design has been chosen to increase the chance to have a working device and to reduce the distance between a Schottky and an Ohmic contact. Also in the case of lateral device the ratio between the ohmic contact surface and the Schottky one has to be the biggest as possible to ensure the rectification behavior of the diode. It is composed of two different zones strictly identical with one big ohmic contact with a 1.9mm^2 surface (top arrows on the figure) encircling Schottky contacts (bottom arrows on the figure). Those last ones are round contacts with different diameters, $200\mu m$ (11 contacts), $100\mu m$ (12 contacts), $40\mu m$ (66 contacts) and $20\mu m$ (66 contacts).

6.3 Diode Characterizations

Once the sample was finished it was first electrically characterized and then some electron beam induced current measurements were performed to check if the device was working properly and to see its homogeneity below the Schottky contact. Electrical measurement consist to intensity-voltage (I-V) characterization at room temperature and temperature variations. Also capacitance measurements have been performed according to frequency (C-f) and voltage (C-V).

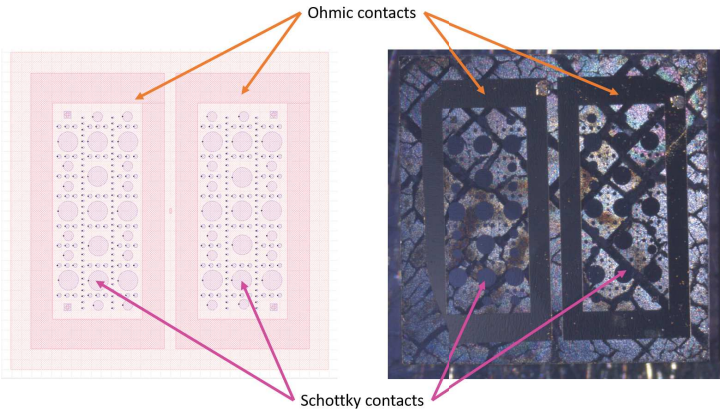

FIGURE 6.4: *On the left the design mask of the sample and on the right terminated device's picture. Orange arrows indicate both ohmic contacts and pink arrow some Schottky contacts*

6.3.1 I-V

All the measurements have been performed under vacuum (i.e $< 10^{-3}$ mbar), with a SMU Keithley 6517B allowing to work up to 1100V with a detection limit of $10^{-15} A$.

6.3.1.1 Room temperature

First room temperature measurements have been performed, on the 100 and 200 μm diodes. A -5 to 5V ramp was applied and currents have been measured. I-V curves in linear and semi-logarithmic scale are shown in figure 6.5 for the 200μm diodes. On those graphs the ON and the OFF state are well defined. On the logarithmic scale the thermionic current starts to rise at 1V. The thermionic current is the same for all the diodes. On the linear scale a slight variation appears for the serial resistance between each diode. From this characterization it is possible to see that serial resistance vary from 9.78 MΩ to 12.2 MΩ. This high serial resistance could be the result of the low doping level and a high contact resistance due to the absence of heavily doped layer under the ohmic contact. Also, Schottky barrier height was extracted by fitting the thermionic part of the forward current and equal to 1.45eV. The ideality factor is also extracted and is closed to 2. It means that the interface between diamond and metallic contacts isn't as good as expected. By compiling all these measurements and putting as a definition that a working device, is when the rectification ratio defined like: $\frac{I_{forward}}{I_{reverse}}$ is higher than 150. With this criteria, the yield number of working devices is up to 92%.

Following these promising results some devices have been pushed to see their blocking voltage capabilities. To do so, this time a Keithley 2612A was used, each device have been tested by increasing the reverse voltage by 10V steps. Only the last curve obtained for the highest reverse bias reached is presented in figure 6.6. In this part, it is considered that a the blocking capability is reached when $I_{forward}$ is at least 10 times higher than $I_{reverse}$. Because no sharp breakdown have been seen, $I_{reverse}$ is only increasing due to leakage current. The

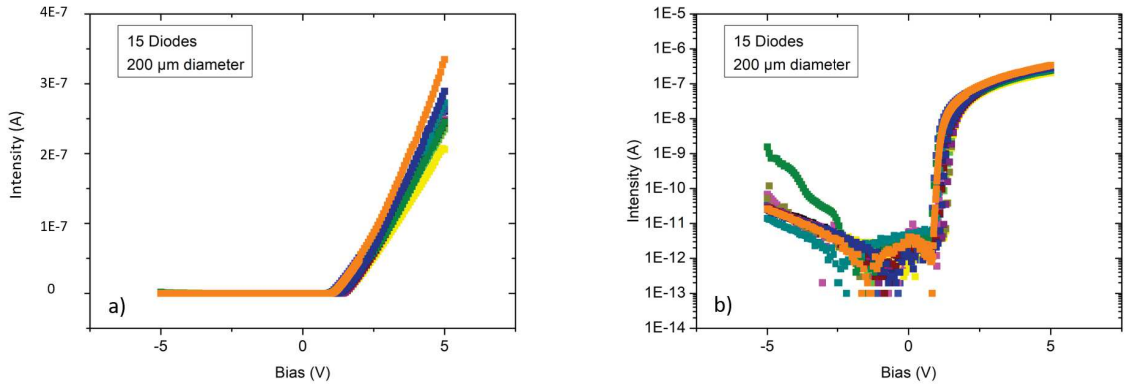

FIGURE 6.5: *I-V characterization at room temperature in a) linear scale and b) log scale*

blocking voltage obtained for each device varies from one to the other. The best measured component has a blocking capability about 70V and bad one of 20V. Two of this contacts which are presented on figure 6.6. On this graph contact A (black curve) with a blocking capability of 60V and contact B (red curve) of 30V. To have a better understanding of this difference this two contacts will be studied by EBIC in the next section.

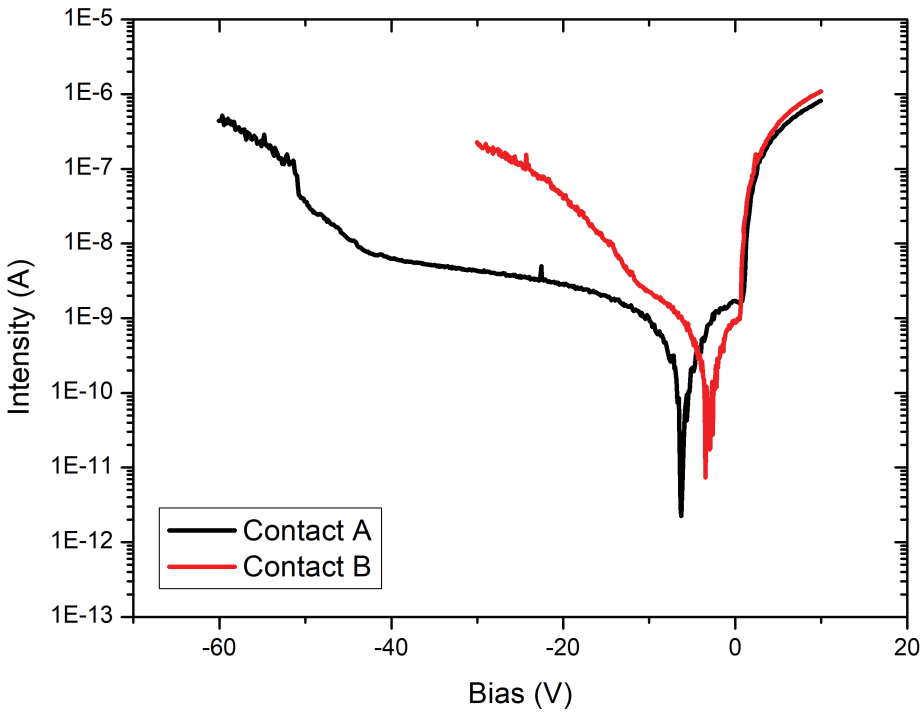

FIGURE 6.6: *I-V characterization at room temperature of 2 different contacts to see their blocking capabilities in logarithmic scale*

6.3.1.2 I-V characterization under different temperature

Characterizations were also performed by increasing the temperature from room temperature (323K) up to 573K. Those results are presented for one diode in figure 6.7 which represents the general behavior of the device.

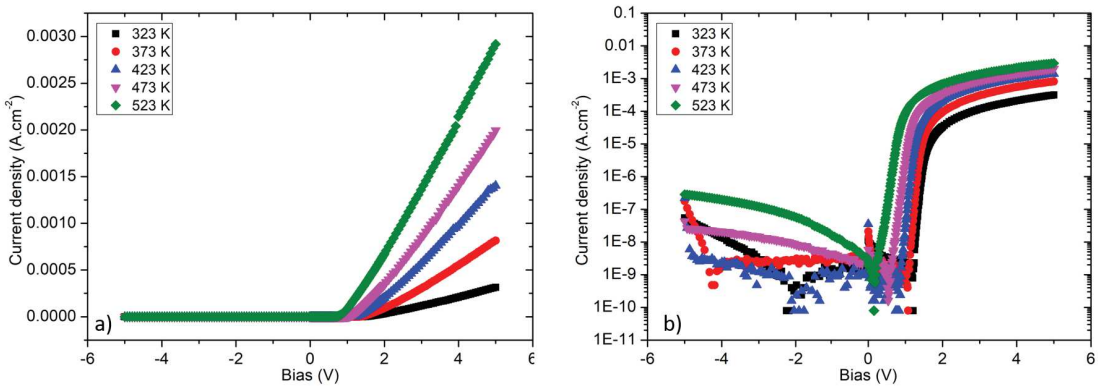

FIGURE 6.7: *I-V characterization as function of the temperature a) linear scale and b) log scale*

The first thing visible on the graph in linear scale is that the serial resistance is decreasing when the temperature is increasing. From the logarithmic plot an other phenomena is highlighted with the decrease of the Schottky barrier height also with temperature increase. The serial resistance decrease can be explained with resistivity decreasing in the 300 to 600K as show by Pernot *et al*. [78] With this graph it is possible to extract both ideality and Schottky barrier height and plot them according to the temperature, all of these parameters are summarized in table 6.2. Those results are plot in function of the temperature in figure 6.8. On this graph two things are highlighted. First one, the ideality factor (round black dots) is increasing with the increase of the temperature meaning that the interface between contacts and diamond surface is deteriorating. As the temperature decreases the ideality factor goes back to its original value. On the contrary the Schottky barrier height is decreasing with the temperature square blue dots during the increase and star yellow dots during the temperature decrease. If it is compared with some studies that have been performed on homoepitaxial lateral Schottky diodes [112, 113] the behavior of the heteroepitaxial one goes strictly into the opposite direction.

6.3.2 C-f and C-V

Capacitance-voltage (C-V) measurements have also been performed to evaluate the effective doping level of the grown layer. Before performing the C-V measurements a capacitance-frequency (C-f) have been performed. Measures were performed at room temperature and under vacuum with a ModulabXM MTS from Solartron analytical. C-V measurements have

TABLE 6.2: *Summary of serial resistance, Schottky barrier height, ideality factor in function of the temperature*

Temperature (K)	R_s (MΩ)	ϕ_b (eV)	n
323	8.06	1.57	1.15
373	3.05	1.47	1.19
423	1.96	1.31	1.32
473	1.31	1.18	1.41
523	1.02	1.01	1.5

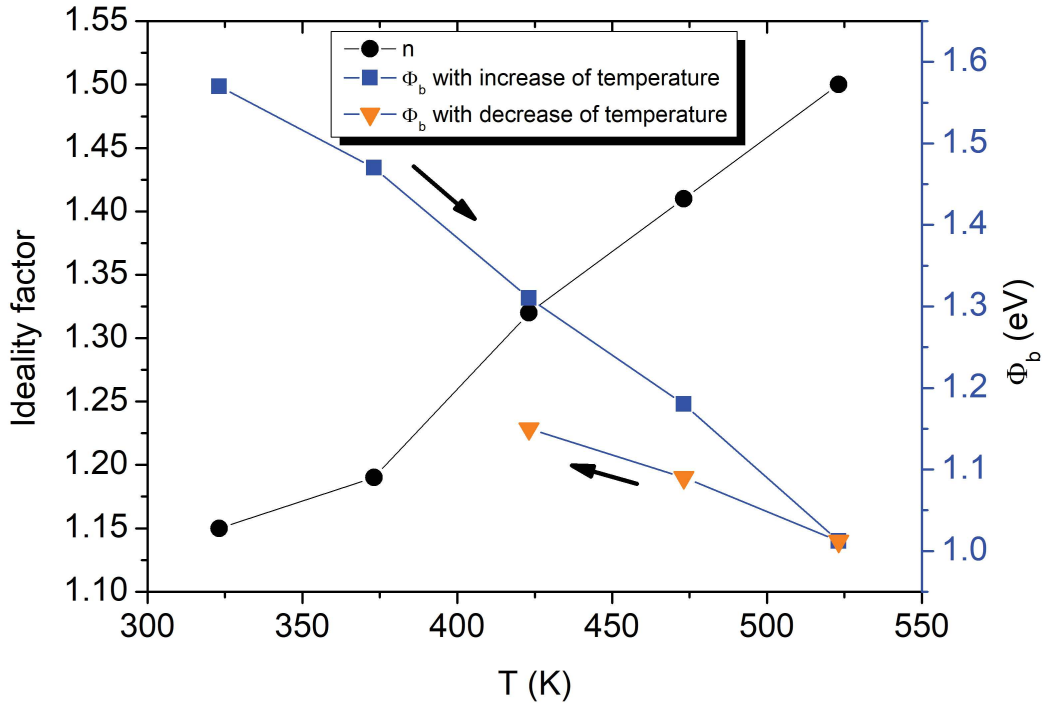

FIGURE 6.8: *Ideality factor and Schottky barrier height in function of the temperature. n with round black dot, ϕ_B with square blue dot during decrease and with star yellow dot during increase of the temperature*

been performed at 100Hz in agreement with the C-f measurement. Measurements are presented in figure 6.9 with the $1/C^2$ in function of the bias, the seven diodes measured are spread all over the sample to check the effective doping level homogeneity . From this graph the layer homogeneity is demonstrated thanks to the fitting of the linear part of the $1/C^2$ curve which gives the same slope. After, by using the formula 1.33, the effective doping level is determined and equals to $1.34 * 10^{16}$ $atom.cm^{-3}$. With this method the built in potential can be extracted, Vbi=3.4 V.

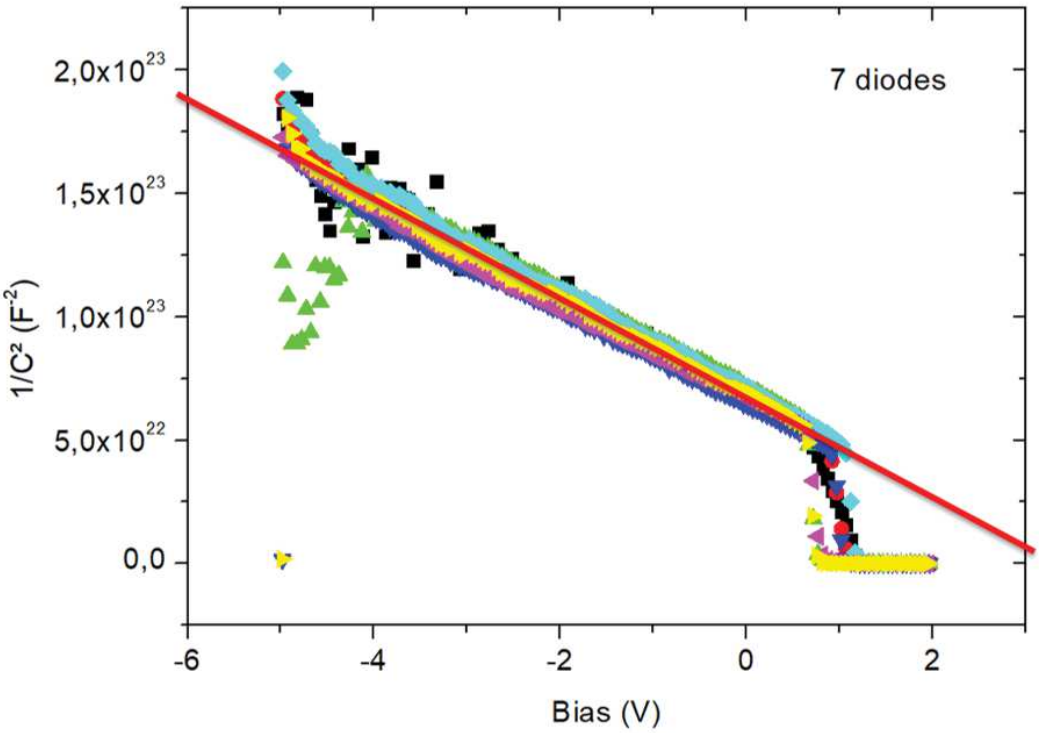

FIGURE 6.9: $1/C^2$ *in function of the bias for 7 diodes from all the sample, in red the fitting of the linear part*

6.3.3 EBIC

A qualitative study have been done to visualize the electric field homogeneity and the presence of defects underneath Schottky contact some EBIC measurements have been performed.The EBIC setup is the same than presented before. Full sized contact EBIC images have been taken as well as zoom ones on the Schottky contact edge. Full sized ones are used to highlight presence of defects and hot spots. And zoom ones, to see the field homogeneity and to extract the diffusion length. Parameters used in both cases are summarized in table 6.3.

Some full sized EBIC images from different contacts spread all over the sample have been done with a -10V polarization. Two of them, which are characteristics are presented in figure 6.10 with their SEM images associated. On contact A it is possible to see on the SEM image a crack underneath the contact but in EBIC this crack does not seem to have an impact on

TABLE 6.3: *Parameters used to performed EBIC*

Parameters	Full size picture	Zoom picture
Acceleration voltage	5kV	5kV
Spot size	4	2
Polarization	-10V	-5V and -10V
Offset	+50nA	+5nA
Sensitivity	50nA/V	5nA/V
Acquisition time	30μs	300μs

the electric field distribution. This confirms what was already explained previously. That cracks visible on the micrograph in figure 6.3 are not inside the diamond. It can also be noticed the arrival of a hot spot at the border between the contact and the diamond (circling in green on the figure). On Contact B, under the metallic part of the contact a brighter zone appears. This zone was not visible on the SEM image and it is electrically active. Those two things can be related to the presence of defects inside the grown layer as well as defects from the fabrication process. One explanation can be the resist remaining from the lift-off process. All of these features can increase the component premature breakdown risk and increase the leakage current. This EBIC measurement confirms the result obtain in the previous section with the breakdown voltage measurement (figure 6.6), with contact B showing a lower blocking capabilities than contact A.

To have a better idea of the electric field, zoom picture has been done to see how the electric field evolves with the polarization and to check its homogeneity. On figure 6.11, on the left side the zoom EBIC image of contact A. First thing, along the contact, the electric field non homogeneity is visible, the bright zone visualizing the electric field does not extend in the same way at every position. To quantify this, on the right side of the figure are extracted two profiles at two different positions represented by the dash blue and the straight red line on the image. On the extracted profile curve that represent the EBIC intensity in function of the distance, the non homogeneity of the electric field is clear, the dash blue profile is more extended than the other one. Also by fitting the exponential decay with an equation of form:

$$y = A.exp\left(\frac{-x}{L_{diff}}\right) + cts \tag{6.1}$$

with A the amplitude, the L_{diff} the exponential decay, in that case is equal to the diffusion length of the carrier. With this formula it is simple to extract the diffusion length by fitting the obtained profile and give the following results 191 nm for the dash blue profile and 138 nm for the straight red one. From the previous measurements on the entire contact the inhomogeneity between contacts appears. As well as with this one the inhomogeneity under one contact appears.

Also measurements have been performed with two different polarizations -5 and -10 V

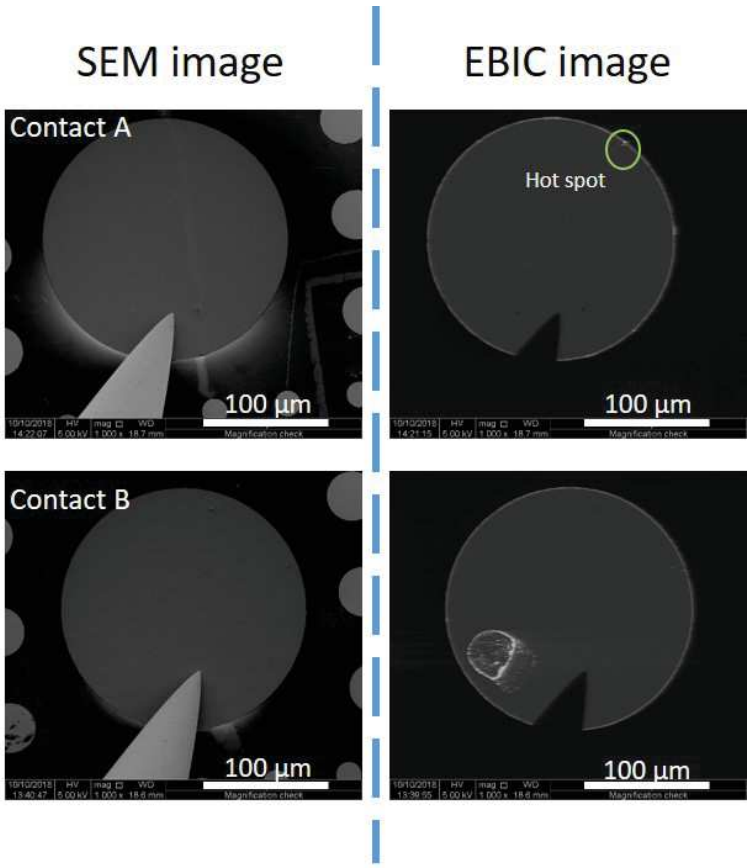

FIGURE 6.10: *Full size SEM and EBIC images of 2 different contacts*

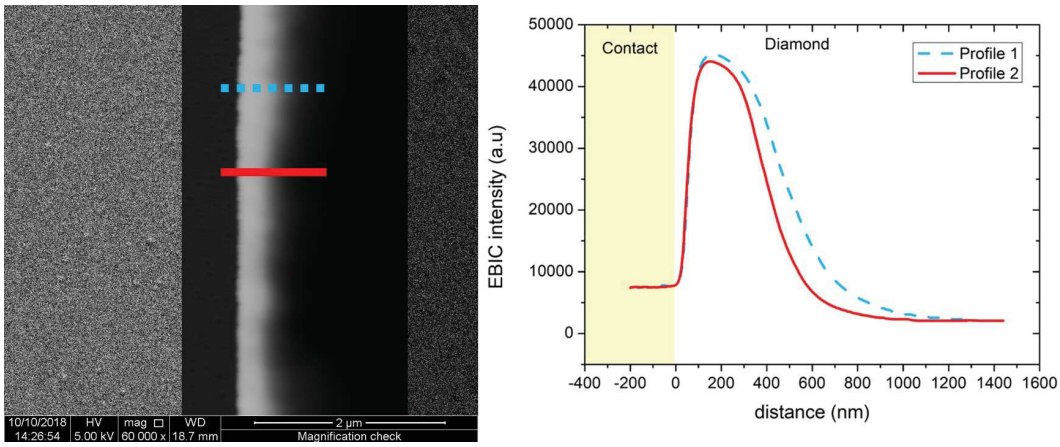

FIGURE 6.11: *Contact A zoomed EBIC image with two extracted profiles (dash blue and straight red lines). Profiles are representing the EBIC intensity in u.a in function of the distance*

in reverse to check the evolution of the electric field. Those are presented in figure 6.12 each profiles are taken at the same position but with 2 different bias the straight orange one at -5V and the dash green one at -10V. As expected the electric field extends as the bias increasing. The diffusion length is extracted by the same method than before using equation 6.1 and give 120 nm for -5 and 140 nm for -10.

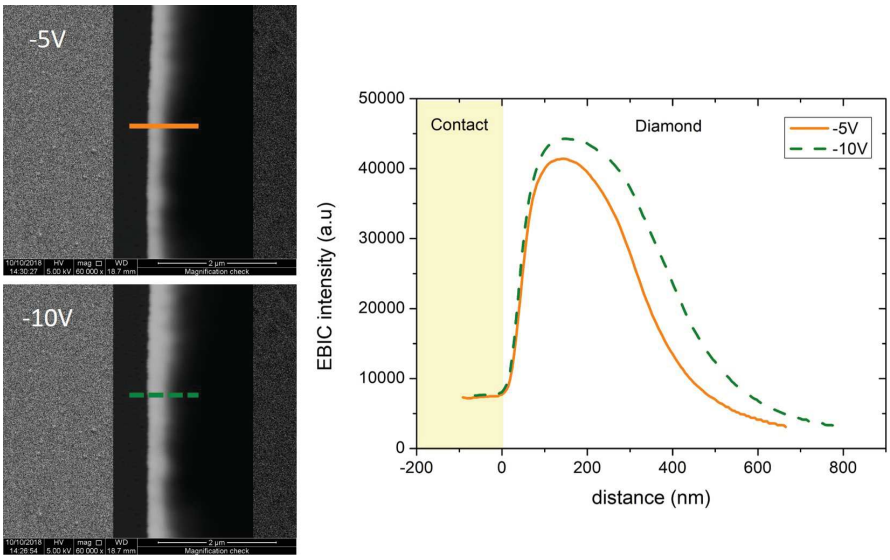

FIGURE 6.12: *Contact A zoomed EBIC image with two extracted profiles (straight orange and dash green line). Profiles are representing the EBIC intensity in u.a in function of the distance*

To sum up this part, EBIC measurements performed on this sample confirm the potential of heteroepitaxially grown diamond for power electronics but also highlight some issues. The electric field non homogeneity can come from the fabrication process with resist left underneath the contact and creates some leakage as shown before. It is also possible that it is coming from defects but in order to know which one cathodoluminescences measurements could be performed and be a good complementary characterization.

6.4 Conclusion

In this chapter was fabricated and characterized lateral diamond Schottky diodes on heteroepitaxially grown diamond. The purpose was to check if the stack used in the framework DIAMWAFEL was suitable for diamond power devices electronic. At the current point, this stack shows the possibility to grow boron doped layer with an average roughness of 30nm which is comparable with what is expected for the same doping level and thickness in homoepitaxial growth but number of dislocation has not been determined, it is expected to be higher than homoepitaxial diamond. Those Schottky diodes show a good rectification behavior and the current device blocking capabilities correspond to what was already obtained for silicon based diamond Schottky diode [107]. The characteristics of the diode could be improved by changing the architecture from lateral one to vertical one. To do so, the diamond

should be self standing without buffer layer and the last epilayer should be an heavily boron doped layer for example if the first layer is slightly doped. With this type of architecture the full potential of the diamond will be use but in that case the dislocation number due to heteroepitaxy can be a drawback and the use of the pseudo vertical or even the encapsulated one could be a good compromise.

Conclusions and Perspectives

During these three years, I have been working on improving diamond Schottky diode characteristics by different methods from the diamond growth to the component architecture and by using new kind of diamond substrate.

At the beginning one of the main issue was coming from the pseudo-vertical architecture used. In this architecture a lot of technical steps have to be performed and especially an etching step. This step is a limiting factor for the active layer thickness to few micrometers. Also each step can introduce some defect (i.e resist remain) and ultimately have an impact on the diode characteristics. In chapter 2 some growth solutions are presented in order to overcome those issues by removing the etching step and at the same time the ohmic contact fabrication steps (i.e: exposure, development and lift-off). The first solution developed is related to the highly doped layer and it is called the encapsulated growth. This allows to take a p++ contact on both side of the diamond substrate and also to create a new kind of architecture, the encapsulated diode. This new device has been tested in chapter 4. Both devices presented with this architecture are showing promising results with a good ON state characteristics (for the $5\mu m_encapsulated$ $\phi_b = 1.25$eV and n close to 1) reproducibility and the reverse characteristic are quite good for this new architecture (the 5μm thick encapsulated diode sustained at least 300V) in reverse bias, but improvement are still needed for the future. Lateral growth could probably be improved by performing polishing on the sample side also the crystallographic orientation of the side will have an impact. Both of this will help to obtained better reverse characteristics.

Another option has been tried, which is the thick selective growth. In that case it appears that the quality of the grown layer is not as good as full sample growing due to the hard mask used. Diodes have still been fabricated on this layer and showing diode I-V characteristics but not as good as the one obtained without the selective growth. Some adjustments on the growth parameter can be performed to optimize it (decreasing the mask temperature) and obtain better feature.

To be closer to the ideal diode the active layer thickness should also be increase. During this thesis new growth conditions have been developed to get thick non intentionally doped layer. I managed to grow a 20μm NID layer and fabricated diode on it side to reach the heavily doped layer. This technique allows me to obtain a diode sustaining at least 1.1kV and further measurements have to be performed in an other laboratory to see how much can be

really sustained. This thicker layer with this tricky architecture also brings interesting information about the electric field distribution inside a Schottky diode, and about the minority carrier (5.6 μm, diffusion length) thanks to EBIC and CL. The electric field non homogeneity has been investigated by combining EBIC and CL measurements but no conclusive results can be made with no obvious difference between spectra from two different areas.

From all the solutions presented in this thesis, it will be interesting for the future in order to get the ultimate diamond Schottky diode to combine the heavily doped encapsulated growth and the thick non intentionally doped recipe developed in this work. This future diode is presented in figure 6.13.

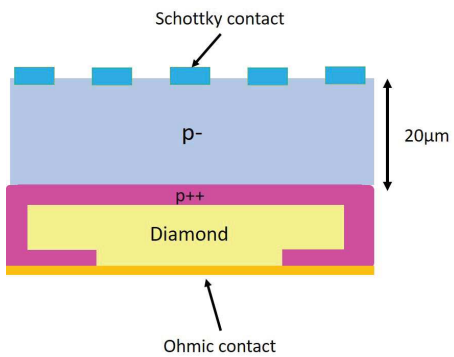

FIGURE 6.13: *Future diamond Schottky diode*

Also some leakage current issue are still present, it can be induced by the low zirconium Schottky barrier height used during this work. For the future it will be interesting to try new Schottky metal with an higher barrier. This will reduce the leakage current coming through the barrier. For example Molybdenum, Tungsten can be used instead of zirconium or an other more exotic idea is to play on the interface by adding a thin Boron nitrite (h-BN) flake between diamond and the metallic contact.

During this time, the common resistance issue highlighted before this work by Perez *et al*. [74] have been resolved by proposing a new design and keeping the pseudo architecture by putting the ohmic contact closer to the Schottky one and by creating some "island". Even if the insulation between island was a failure because of the substrate used. I was still able to perform diodes parallelization and still have convincing results. Diodes parallelization is an interesting solution to increase the ON state current density available on a chip when diodes by themselves have low ON state current density. This new architecture performed on insulating diamond substrate can provide interesting component chip with possibility to have an internal knowledge of the chip temperature using one of the diamond properties which is the temperature dependence of the mobility. The first full diamond diode bridge have been created with some diodes fabricated during this thesis and shows with the preliminary measure performed by G2Elab in Grenoble some promising results.

Another issue which is often coming back for diamond power electronics is the small

size of available substrate in comparison with other candidates. In this thesis a new type of material have been tested for power electronics it is an heteroepitaxial stack composed with Diamond/Ir/$SrTiO_3$/Si. Use of silicon wafer will allow at the end to have bigger diamond substrate than the one produced by HPHT. On the first 3 by 3 mm^2 available substrate of this material lateral Schottky diode have been fabricated. This requires a lot of caution to process because of the stack fragility. Those diodes show nice results with 92 % of them showing a rectification behavior but the reverse characteristics are far from the optimal probably due to the presence of interface state at the junction between diamond and zirconium and also the device chosen geometry. Next step for this material is to fabricate Schottky diode with a pseudo-vertical architecture like state of the art obtained on homoepitaxialy grown diamond. Another solution will be to go directly to vertical diode by removing the Ir/$SrTiO_3$/Si stack and by working directly on the doping level of the first diamond layer. At the end for this material to have a real interests for the industry the available sample size have still to be increase to be bigger than the HPHT substrate commercially available and easier to manipulate.

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Appendix A

Abstracts

Diamond Schottky diodes improvement to pave the way to high power electronic applications

Diamond is known as the best candidate for power electronics application. Currently the most advance component is the Schottky diode. This device is already showing promising results but some improvements are still needed, such as the increase in the forward currents combined with an increase in the breakdown voltage of the component. These electrical constraints are still closely related to the properties of the material and the quality of diamond CVD growth. In this thesis, some solutions will be proposed and presented from the diamond growth and fabrication steps and after characterized to see if they are suitable. I will first discuss about diamond growth and present new improvements about it, that concern the heavily doped layer as well as the non-intentionally doped one in order to simplify fabrication processes and reduce the influence of the serial resistance of the deposited layers. Concerning, the ON-state, an important work about diode parallelization has been conducted. In this topics, the first heterohepitaxial substrate allowing potentially component with larger surface grown diodes have been tested. Lateral Schottky fabricated on diamond/Ir/SrTiO3/Si will be described and characterized. The OFF-state and the breakdown voltage control has been also investigated by increasing the thickness of the diamond layer by maintaining a good growth quality and avoiding the etching step which is still a problem for diamond. At the same time a transversal (i.e in the diamond depth) study will be presented to understand how is the electric field underneath the diode by electron beam induced current and cathodoluminescence technics. This thesis made it possible to develop a process for thick film growth by potentially simplifying the diodes fabrication; to demonstrate the feasibility of diodes parallelization with their integration into a diode bridge; It also showed that beyond the breakdown voltage the reverse leakage still remains a blocking point for the development of diamond components.

Diodes Schottky en diamant un nouveau pas vers les applications de l'électronique de puissance

Le diamant est reconnu comme étant le meilleur candidat pour l'électronique de puissance. Actuellement, le composant le plus avancé est la diode Schottky. Ce composant présente déjà des résultats prometteurs, mais certaines améliorations restent nécessaires, telles que l'augmentation des courants à l'état passant combinée à une augmentation de la tension de claquage. Ces contraintes électriques sont toujours étroitement liées aux propriétés du matériau et à la qualité de la croissance du diamant par CVD. Dans cette thèse, des solutions seront proposées et présentées à partir des étapes de croissance du diamant et de la fabrication des diodes et ensuite caractérisées pour voir si elles conviennent. Je vais d'abord aborder la croissance du diamant et présenter de nouvelles méthodes, concernant la couche fortement dopée ainsi que la couche non intentionnellement dopée, afin de simplifier les processus de fabrication et de réduire l'influence de la résistance en série des couches déposées. En ce qui concerne l'état passant, un travail important sur la parallélisation des diodes a été effectué. Mais aussi, le premier substrat hétérohépitaxié permettant la création de composants ayant une plus grande surface a été testé. Des diodes Schottky laterales ont été fabriqués sur diamant / Ir / SrTiO3 / Si, elles seront décrites et caractérisées. L'état bloquant et le contrôle de la tension de claquage ont également été étudiés en augmentant l'épaisseur de la couche de diamant tout en maintenant une bonne qualité de croissance et en évitant l'étape de gravure qui reste problématique pour le diamant. Dans le même temps, une étude transversale d'une diode (i.e dans la profondeur du matériau) sera présentée pour comprendre comment est le champ électrique sous la diode grâce aux techniques de courant induit par faisceau d'électrons et de cathodoluminescence. Cette thèse a permis de développer un procédé de croissance de film épais en simplifiant potentiellement la fabrication des diodes; démontrer la faisabilité de la parallélisation des diodes avec leur intégration dans un pont de diodes; il a également été montré qu'au-delà de la tension de claquage, la fuite inverse reste un point de blocage pour le développement des composants en diamant.

Appendix B

Résumé de la thèse en français

Aujourd'hui, un des plus grands enjeux écologiques que le monde doit résoudre est la limitation du réchauffement climatique. Depuis l'organisation de la conférence sur le changement climatique à Paris en 2015 (COP 21), il a été décidé de limiter l'augmentation du réchauffement climatique à 2,5° C entre 2030 et 2050. L'Union européenne s'est engagé dans le même temps à réduire les émissions de gaz à effet de serre de l'ordre de 40 %. Cependant, avec une population grandissante et des besoins en énergie de plus en plus présent nos modes de vie doivent évoluer. Pour ce faire, l'utilisation des énergies fossiles doit diminuer et celle des énergies propres telles que l'énergie solaire et éolienne doit augmenter. Pour ce faire, notre réseau électrique doit évoluer pour devenir un réseau intelligent qui intègre ces nouveaux besoins et ces nouvelles sources d'énergie propre. Dans cette optique, l'utilisation de composant d'électronique de puissance est nécessaire. Actuellement, ce secteur est dominé par les composants en silicium, or les limites de ces derniers sont atteintes. Cela peut être des limites liées à leurs propriétés intrinsèques telles que leur tension de claquage, leur incapacité à travailler à haute température mais aussi leur grand taux de perte en énergie. De nombreux matériaux sont donc étudiés pour les remplacer. Ces nouveaux matériaux font partie de la famille des semi-conducteurs à large bande interdite. Les principaux sont le carbure de silicium (SiC), le nitrure de gallium (GaN), l'oxyde de gallium (Ga_20_3) et le diamant (C). En comparant les propriétés physiques de ces divers matériaux leur champ de claquage, leur mobilité, et les figures de mérite comme par exemple celle de Baliga qui décrit l'efficacité du matériau à diminuer ses pertes de conduction. En prenant tous ses paramètres en considération on se rend compte que le diamant est le meilleur candidat pour créer les composants d'électronique de puissance de demain.

L'électronique de puissance en diamant connaît depuis quelques années de nombreuse avancées. De tout les composants possibles le plus avancé est la diode Schottky. Cependant, cette dernière n'est pas encore arrivée à son plein potentiel. Et des améliorations doivent être apportées au niveau de l'état passant en augmentant les densités de courant et au niveau de l'état bloqué en augmentant les capacités de blocages de la diode.

Cette thèse avance dans cette direction. Une diode est basée sur un empilement de deux couches de diamant la première fortement dopée sur laquelle sera prise le contact ohmique est une faiblement dopée où seront déposé les contacts Schottky. Il existe plusieurs types d'architecture, la verticale et la pseudo-verticale qui est à l'état de l'art. (fig. B.1)

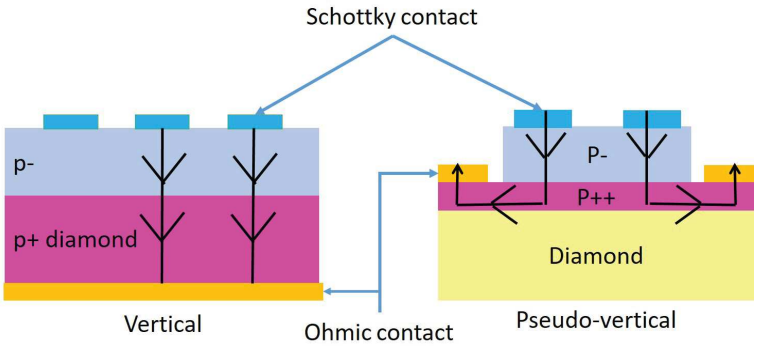

FIGURE B.1: *Les deux principales architectures disponible pour fabriquer des diodes Schottky en diamant, à gauche une architecture verticale et à droite l'architecture pseudo-verticale à l'état de l'art*

La première partie de cette thèse (chapitre 2) a été de travailler sur l'amélioration des croissances diamant obtenues par dépôt chimique en phase vapeur assisté par plasma micro-onde (MPCVD). Pour les couches fortement dopées une nouvelle technique a été mise au point, la croissance encapsulée. Cette technique permet d'avoir de la croissance de chaque côté du substrat permettant d'éliminer l'étape de gravure necessaire dans l'architecture pseudo-vertical. Cette nouvelle architecture est présenté en figure B.2 avec le contact ohmique pris directement en face arrière.

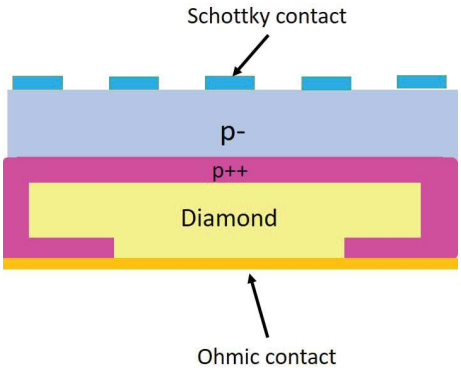

FIGURE B.2: *Schéma de diodes Schottky avec une architecture encapsulée*

Ensuite des efforts on était porté sur l'augmentation de l'épaisseur de la couche faiblement dopée en passant de quelques micromètres à une vingtaine tout en gardant une bonne qualité cristalline. Pour ce faire une recette en deux phases a été développée comprenant une phase à taux de méthane constant et la deuxième ou ce taux va progressivement décroître jusqu'à atteindre 0. Cette nouvelle façon de croître a été par la suite caractérisé par microscopie électronique à transmission en collaboration avec l'Université de Cadix en Espagne. Avec cette méthode une couche de plus de 20 μm a été obtenue. De plus, la croissance sélective épaisse a été initiée en proposant d'utiliser un nouveau type de masque solide fabriqué en molybdène. Ce chapitre 2 met également en avant les différentes étapes technologiques nécessaires à la réalisation de diode Schottky.

Dans un deuxième temps, un travail important a été réalisé sur l'augmentation du courant à l'état passant en develloppant la mise en parallèle de plusieurs diodes avec la création d'un nouveau design (chapitre 3). En effet dans une précédente étude effectué par Perez *et al.* [74] il a été montré qu'une résistance commune ne permettait pas de faire de la parallélisation efficacement. Il est montré ici que le fait de rapprocher le contact Schottky du contact ohmique et de découpler les chemins de conduction permet d'éliminer le problème de résistance commune et ainsi obtenir une parallélisation efficace et équivalente à ce qui est attendue. (fig. B.3)

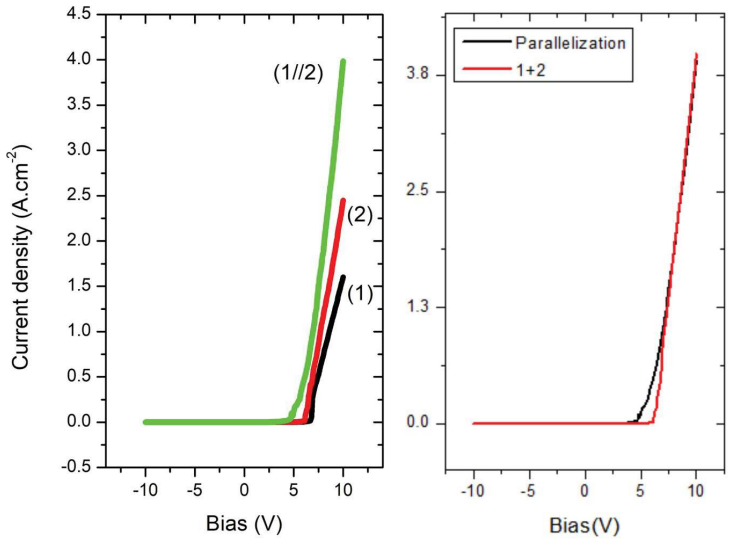

FIGURE B.3: *Caractérisation I-V de deux diodes indépandantes et de leur parallélisation à gauche et à droite comparaison entre la parallélisation et la somme mathématique des 2 diodes*

Ensuite l'accent a été mis sur la caractérisation des nouvelles diodes développées à partir des nouvelles techniques de croissance (chapitres 4 et 5). En premier, les diodes obtenues avec la croissance encapsulée ont été mesurées avec des résultats prometteurs. En effet, ces diodes montrent des caractéristiques reproductibles à l'état passant et des tenues en tension supérieur à 200V pour les différents échantillons (fig. B.4). En ce qui concerne la croissance sélective épaisse, les composants fabriqués montrent une caractéristique de diode cependant ces dernières ne sont pas idéales, avec une très grande résistivité et un fort courant de fuite observé lors de l'application de tension négative.

Pour la dernière méthode de croissance développée, une diode avec une couche active de 20 μm faiblement dopée a été fabriqué par polissage d'une des face latérale de l'échantillon avec le dépôt des 2 contacts ohmique sur la face latérale et des contacts ohmiques sur la face avant. (figure B.5 a) et b)) Cette diode ainsi obtenue montre une tenue en tension de plus de 1.1kV pour les plus petits contacts (70x70 μm^2) (figure B.5 c)). Avec cette architecture originale, une étude plus poussée sur l'évolution de la zone de charge d'espace à

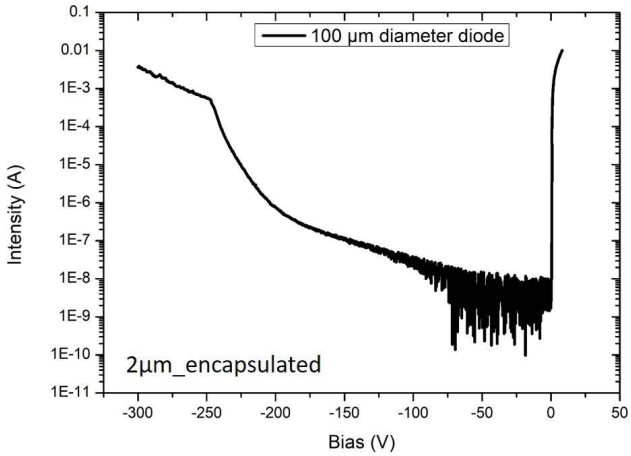

FIGURE B.4: *Caractérisation I-V typique d'une diode Schottky encapsulée*

l'intérieur des différentes couche de diamant. Grâce à la méthode de courant induit par faisceau d'électrons (EBIC), il est possible de suivre l'évolution de l'extension en fonction de la tension appliquée. Des mesures de cathodoluminescences ont également été effectués pour obtenir le dopage de la couche et identifier des défauts présents dans la couche. Par la suite, les deux méthodes ont été combinées pour essayer d'avoir un point de vue global de la situation.

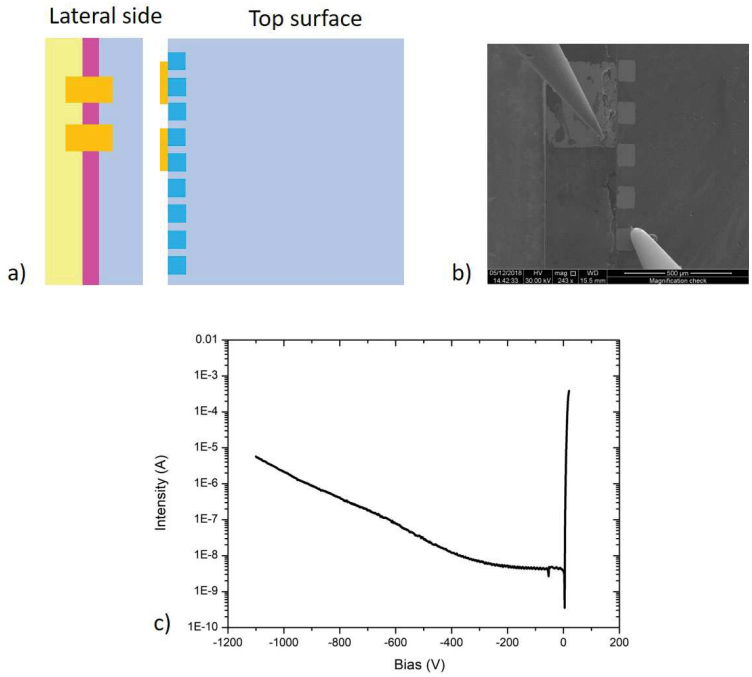

FIGURE B.5: *a) Schéma de la diode en orange les contacts ohmiques et en bleu les contacts Schottky, b) image MEB du composant et c) caractéristique I-V d'une diode de 70x70µm^2*

Pour finir, durant cette thèse en collaboration avec le consortium de l'ANR Diamwafel, les premières diodes sur substrat hétéroépitaxié entièrement fabriqué en France a été réalisé. Ce nouveau substrat est composé d'un empilement Diamant/Ir/$SrTiO_3$/Si qui doit permettre d'obtenir des substrats diamant de grande taille et ainsi lever un des verrous technologiques des composants électroniques en diamant. Mais ce nouveau matériaux doit être testé, dans cette optique le plus simple des composants a été réalisé. Des diodes avec une architecture latérale ont été réalisées privilégiées car nécessitant moins d'étapes de fabrication. Les diodes fabriquées ont une bonne reproductivité à l'état passant cependant l'état bloqué reste limité (moins de 100V de tenue en tension). Pour mieux comprendre pourquoi des mesures EBIC ont également été effectuées sur cet échantillon, les résultats donnent quelques pistes de travail pour améliorer leurs caractéristiques.

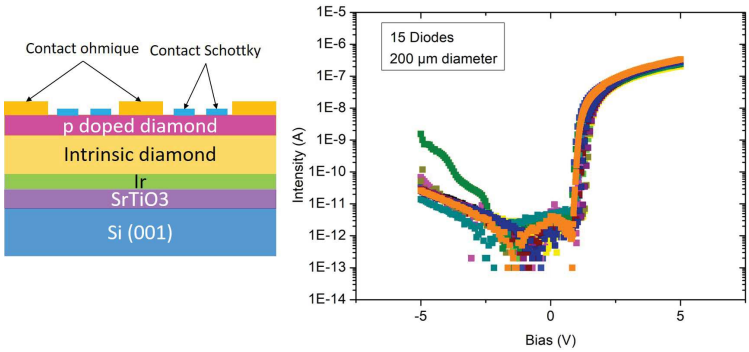

FIGURE B.6: *A gauche le schéma de la structure réalisée et des diodes Schottky latérales, à droite les caractéristiques I-V en échelle logarithmique des diodes fabriquées.*

Appendix C

Publications and Conferences

C.1 Publications

- G. Perez, **J. Letellier**, A. Maréchal, D. Eon, G. Chicot, P-O. Jeannin, N. Rouger: Diodes Schottky en Diamant : augmentation du calibre en courant et parallélisation", Symposium de genie électrique
- G. Perez, **J. Letellier**, A. Maréchal, D. Eon, G. Chicot, P. Jeannin, N. Rouger and J. Schanen: "Diamond Schottky barrier diodes for power electronics applications,"2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 1956-1963.
- C. Masante, J. Pernot, **J. Letellier**, D. Eon and N. Rouger, "175V, > 5.4 MV/cm, 50mΩ.cm^2 at 250 °C Diamond MOSFET and its reverse conduction,"2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD), Shanghai, China, 2019, pp. 151-154.
- J-C. Arnault, K. Lee, J. Delchevalrie, J. Penuelas, L. Mehmel, O. Brinza, S. Temgoua, I. Stenger, **J. Letellier**, G. Saint-Girons, R. Bachelet, R. Issaoui, A. Tallaire, J. Achard, J. Barjon, D. Eon, C. Ricolleau, S. Saada: "Diamond on Ir / SrTiO3 / Si (001): from sequential material characterizations to fabrication of lateral Schottky diodes", accepted to Diamond and Related Materials
- G. Alba, D. Eon, M. P. Villar, R. Alcantara, G. Chicot, J. Canas, **J. Letellier**, D. Araujo: "H-terminated diamond surface band bending characterization by angle-resolved XPS", Surfaces 2020, 3(1), 61-71; https://doi.org/10.3390/surfaces3010007 (registering DOI)

C.2 Conferences

C.2.1 Oral presentations

- J. Letellier, E.Gheeraert, G. Perez, P. Lefranc, P-O. Jeannin, N. Rouger and D. Eon: In situ temperature measurement of high power diamond Schottky diodes - OIST Diamond Workshop 2017 (5th French – Japonese symposium), Okinawa, Japan

- J. Letellier, G. Alba, F. Lloret, D. Araujo, M. P. Villar, F. Donatini, E. Gheeraert and D. Eon: TEM and electrical study of a vertical diamond Schottky diode – ICDCM 2018, Dubrovnik, Croatia
- J. Letellier, F. Donatini, E. Gheeraert , J. Pernot and D. Eon: Electrical field study of a diamond Schottky diode by electron beam induced current - Aussois Diamond Workshop 2019 (6th French – Japonese symposium), France
- J. Letellier, G. Jacopin, F. Donatini, J. Pernot, and D. Eon: In depth study of Schottky diode by electron beam induced current and cathodoluminescence - ICDCM 2019, Sevilla, Spain

C.2.2 Poster presentations

- J. Letellier, E.Gheeraert, G. Perez, P. Lefranc, P-O. Jeannin, N. Rouger and D. Eon: high power diamond Schottky diodes including a temperature sensor - Best student award for poster presentation EMRS Fall meeting 2017 – Warsaw, Poland
- J. Letellier, F. Donatini, E. Gheeraert, J. Pernot, D. Eon: Electrical field study into the depth of a diamond Schottky diode by EBIC - SBDD XXIII 2018 Hasselt, Belgium
- J. Letellier, F. Lloret, M.P Villar, D. Araujo, F. Donatini, E. Gheeraert, D. Eon: Transversal diamond Schottky lamella to study material and electrical properties, EMRS spring meeting 2018, Strasbourg, France
- J. Letellier, F. Donatini, E. Gheeraert , J. Pernot and D. Eon : Electrical field study into the depth of a diamond Schottky diode by Electron Beam Induced Current – SBDD XXIV 2019 Hasselt, Belgium

Diamond Schottky diodes improvement to pave the way to high power electronic applications

Diamond is known as the best candidate for power electronics application. Currently the most advance component is the Schottky diode. This device is already showing promising results but some improvements are still needed, such as the increase in the forward currents combined with an increase in the breakdown voltage of the component. These electrical constraints are still closely related to the properties of the material and the quality of diamond CVD growth. In this thesis, some solutions will be proposed and presented from the diamond growth and fabrication steps and after characterized to see if they are suitable. I will first discuss about diamond growth and present new improvements about it, that concern the heavily doped layer as well as the non-intentionally doped one in order to simplify fabrication processes and reduce the influence of the serial resistance of the deposited layers. Concerning, the ON-state, an important work about diode parallelization has been conducted. In this topics, the first heterohepitaxial substrate allowing potentially component with larger surface grown diodes have been tested. Lateral Schottky fabricated on diamond/Ir/SrTiO3/Si will be described and characterized. The OFF-state and the breakdown voltage control has been also investigated by increasing the thickness of the diamond layer by maintaining a good growth quality and avoiding the etching step which is still a problem for diamond. At the same time a transversal (i.e in the diamond depth) study will be presented to understand how is the electric field underneath the diode by electron beam induced current and cathodoluminescence technics. This thesis made it possible to develop a process for thick film growth by potentially simplifying the diodes fabrication; to demonstrate the feasibility of diodes parallelization with their integration into a diode bridge; It also showed that beyond the breakdown voltage the reverse leakage still remains a blocking point for the development of diamond components.

Diodes Schottky en diamant un nouveau pas vers les applications de l'électronique de puissance

Le diamant est reconnu comme étant le meilleur candidat pour l'électronique de puissance. Actuellement, le composant le plus avancé est la diode Schottky. Ce composant présente déjà des résultats prometteurs, mais certaines améliorations restent nécessaires, telles que l'augmentation des courants à l'état passant combinée à une augmentation de la tension de claquage. Ces contraintes électriques sont toujours étroitement liées aux propriétés du matériau et à la qualité de la croissance du diamant par CVD. Dans cette thèse, des solutions seront proposées et présentées à partir des étapes de croissance du diamant et de la fabrication des diodes et ensuite caractérisées pour voir si elles conviennent. Je vais d'abord aborder la croissance du diamant et présenter de nouvelles méthodes, concernant la couche fortement dopée ainsi que la couche non intentionnellement dopée, afin de simplifier les processus de fabrication et de réduire l'influence de la résistance en série des couches déposées. En ce qui concerne l'état passant, un travail important sur la parallélisation des diodes a été effectué. Mais aussi, le premier substrat hétérohépitaxié permettant la création de composants ayant une plus grande surface a été testé. Des diodes Schottky laterales ont été fabriqués sur diamant / Ir / SrTiO3 / Si, elles seront décrites et caractérisées. L'état bloquant et le contrôle de la tension de claquage ont également été étudiés en augmentant l'épaisseur de la couche de diamant tout en maintenant une bonne qualité de croissance et en évitant l'étape de gravure qui reste problématique pour le diamant. Dans le même temps, une étude transversale d'une diode (i.e dans la profondeur du matériau) sera présentée pour comprendre comment est le champ électrique sous la diode grâce aux techniques de courant induit par faisceau d'électrons et de cathodoluminescence. Cette thèse a permis de développer un procédé de croissance de film épais en simplifiant potentiellement la fabrication des diodes; démontrer la faisabilité de la parallélisation des diodes avec leur intégration dans un pont de diodes; il a également été montré qu'au-delà de la tension de claquage, la fuite inverse reste un point de blocage pour le développement des composants en diamant.