Growth and characterization of SiGe alloys on nanometer-size structures for microelectronics applications

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Growth and characterization of SiGe alloys on nanometer-size structures for microelectronics applications

Croissance et caractérisation d'alliages SiGe sur des structures de tailles nanométriques pour des applications en micro-électronique

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General introduction

The world is living a connected era driven by data analysis and exchange through a large network of communicating devices. Laptops, smartphones, tablets, connected watches and virtual assistants are the result from technological breakthroughs that started in the mid-20th century in the fields of semiconductor physics, electronics and materials. The journey from the discovery of transistor action by Bardeen and Brattain in 1947 to the latest "5 nm node technology" announcements by TSMC has been long. The best example of such a technological trajectory is the trend line associated with Moore's Law, where device density has doubled every 12 to 18 months for several decades. Silicon (Si) has been a key material in this technological journey. Thanks to the stability of its oxide, its fabrication ease and abundance, it is now an established and extremely mature technology.

The continuous scaling law initially observed by Moore has come a long way using the Si based technology. However, as transistors become smaller and smaller, previously insignificant issues become incredibly important. Some of the biggest issues are leakage current and short channel effects. Several methods considered as performance boosters have been introduced in order to stave off these effects. These include the straining of silicon (the context of this PhD), the use of silicon on insulator (SOI) substrates, high-k metal gates (HKMG), and Fin-type Field Effect Transistors. As we approach the end of the scaling era (3 nm node ~2021), state of the art developments will no longer rely on Si-based technology scaling but on alternative research axes such as new computing paradigms, emergent device architectures and alternative materials.

The latest developments in computing include fashionable computing paradigms such as neuromorphic and quantum computing. However, for device improvements, there are innovative architectures such as gate all-around transistors (GAA), tunnel field effect transistors (TFET), single electron transistors (SET), negative capacitance field effect transistors (NCFET), nano-electro-mechanical-switches (NEMS), oxide electronics using metal-oxide transitions (Vanadium oxide for instance) and emerging memories such as phase change memories (PCM), resistive (RRAM), magnetic (Spin Transfer Torque RAM) and ferroelectric (FRAM). There are also innovative global integration schemes like the CoolCube™ approach from CEA-LETI which consists of stacking transistors on top of each other sequentially.

Si is hardly the ideal semiconductor from a device or circuit designer's perspective. The carrier mobility for electrons and holes in Si is comparatively low compared to materials such as III-V and Ge. Much effort has been expended to integrate such alternative materials on Si, with III-V alloys such as GaAs or InGaAs being considered as channel materials for n-type Metal Oxide Semiconductor Field Effect Transistors (nMOSFETs). Meanwhile, pure Ge provides the highest hole mobility of all cubic semiconductors (1900 $cm^2.V^{-1}.s^{-1}$ instead of for instance 450 $cm^2.V^{-1}.s^{-1}$ for Si) and so it interesting for high performance p-type MOSFETs. However, the

use of high mobility materials instead of silicon involves complex technological breakthroughs, and so this has not been integrated into production devices.

An alternative way to boost mobility in Si is with the introduction of a tensile strain. The mainstream method for straining silicon is to grow a Si layer on a top of a SiGe virtual substrate (VS) (which has on top a fully relaxed layer of SiGe obtained by epitaxy on a silicon substrate). It is obvious that the quality of the SiGe virtual substrate will have a critical impact on the strained Si layer. However, SiGe heteroepitaxial growth on Si is lattice mismatched, thus mastering strain relaxation is very important in thick layers. Several schemes have been explored to obtain fully strain relaxed SiGe layers with reduced densities of defects. For instance, linearly graded buffer layers yield high quality fully relaxed SiGe layers on top. However, this technique results in SiGe layers several microns thick which can be detrimental in terms of cost (growth time, gas consumption, etc.) and wafer bowing issues (especially on 300 mm wafers).

In this thesis, we explored a new paradigm for growing mismatched SiGe epitaxial layers on silicon. Called nano-heteroepitaxy, this method was first proposed in 1986 by Luryi and Suhir from Bell Laboratories. The idea is to provide additional degrees of strain relaxation by starting the growth from nanometer sized seeds and so generate fast relaxation of the layers. The thesis manuscript will consist of six chapters:

The **first chapter** introduces the material of interest, i.e. SiGe alloys. Properties such as crystal structure and phase diagram are first presented. The growth of SiGe on Si is then discussed. Epitaxy and surface energy related growth modes are described and the concept of plastic strain relaxation is explained followed by a description of the most common crystal defects found in SiGe when grown on Si. The second part of this chapter gives an overview about the context of this PhD which is strained silicon-on-insulator (sSOI) technology. The most common defect engineering strategies used for SiGe virtual substrates fabrication are explained, and finally, a special focus is made on nano-heteroepitaxy, with the presentation of the concept and theory as well as a brief state of the art.

A nano-template integration scheme specifically designed for the investigation of SiGe nano-heteroepitaxy is described in the **second chapter**. Detailed technological steps include diblock copolymer patterning, surface preparation before epitaxy and SiGe growth by chemical vapor deposition. Several characterization techniques used for morphological and structural analysis of the samples are subsequently introduced.

In the **third chapter**, two SiGe nano-heteroepitaxy integration schemes are studied. The first consists in selectively growing Si nano-pillars followed by thick SiGe layers, and the second in selectively growing SiGe nano-pillars with on top thick SiGe layers with the same Ge content. For each scheme, the nano-pillars growth is investigated before the growth of the coalesced layers.

The **fourth chapter** deals with SiGe nano-pillars coalescence. The idea is to study the coalescence phenomena at the early growth stages. SiGe nano-pillars of different thicknesses are selectively grown and characterized by Atomic Force Microscopy, X-ray Diffraction, Scanning Spreading Resistance Microscopy and Transmission Electron Microscopy.

An investigation of the nano-template is performed in the **fifth chapter**. The impact of several parameters on the SiGe layer quality is studied. The size of the openings (and their pitch), the presence (or not) of the mask and the masking material (SiO_2 or SiN) are changed.

The nano-heteroepitaxy method is extended to pure Ge in the **sixth chapter**. Ge nano-pillars are first studied followed by thick coalesced Ge layers. A comparison is made between Ge thick layers grown using a best known method, on bulk and nano-patterned Si substrates.

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CHAPTER I:
From epitaxy to nano-heteroepitaxy

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I.1. Introduction

SiGe alloys have been a major add-on since their introduction in the Si-based semiconductor technology. With the miniaturization era coming to an end, alternative materials such as SiGe have been used as performance boosters in complementary metal oxide semiconductor transistors (in high mobility channels, as stressors in short gate length devices, in raised sources and drains and so on illustrated in **Figure I.1**). SiGe co-integration with Si yielded significant performance enhancements in SiGe heterojunction bipolar transistors. SiGe alloys are finding numerous other applications in fields such as optoelectronics (near infra-red detectors or mid infra-red waveguides). This paved the way for the use of Si/SiGe heterostructures in novel devices such as stacked nanowires or neuromorphic memories.

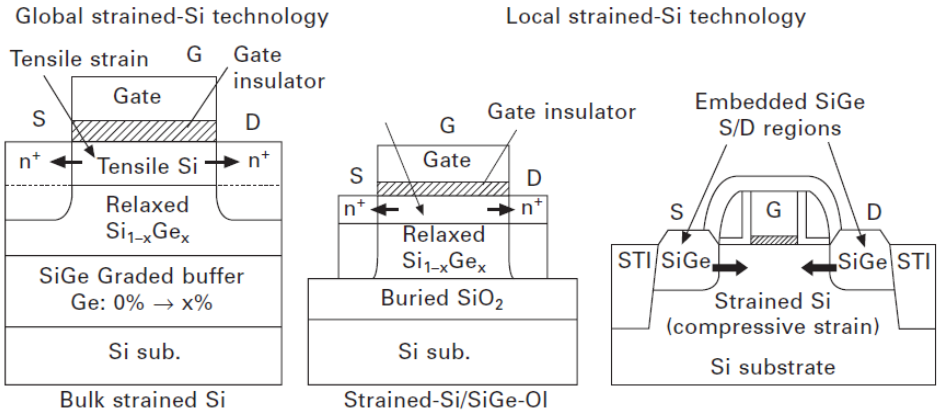

Figure I.1 Schematic cross-sections of typical bulk strained-Si MOSFETs, strained-Si/SiGe-on-insulator MOSFETs and strained-Si MOSFETs with SiGe embedded source/drain (Shiraki and Usami 2011)

SiGe based devices performances are mainly coming from the structural and electronic properties of the alloy. Epitaxial growth of SiGe layers on a Si substrate was early one identified as the method of choice to have a superior crystalline quality. However, SiGe hetero-epitaxial growth on Si is not lattice matched (4.18% difference between Si and Ge). Controlling strain relaxation in thick SiGe layers is therefore important to avoid highly bowed wafers and defective layers.

Our aim being, in the end, the fabrication of tensile-strained Silicon-On-Insulator substrates (with an electron mobility twice that in bulk, unstrained Si), we were interested in achieving a high quality fully strain relaxed SiGe layer a hundreds of nanometers thick, to be used later on as a template for the deposition of a strained Si layer. Several schemes can be explored to obtain fully strain relaxed SiGe layers. For instance, linearly graded buffer layers yield high quality fully relaxed SiGe layers. However, this technique results in SiGe layers several microns thick which can be detrimental in terms of cost (growth time, gas consumption, etc) and wafer

bowing issues (especially on 300 mm wafers). Therefore, we decided to explore a new growth approach called “Nano-heteroepitaxy” which is based on the pioneering theoretical work of Luryi and Suhir. This work suggests that if SiGe can be grown in sufficiently small nano-pillars, it can relax elastically then coalesce without generating additional defects. This is therefore a potential technique for the fabrication of high quality fully relaxed SiGe layers.

In this first chapter, we will summarize some of the SiGe properties and present some basic concepts about SiGe heteroepitaxy on Si. The context of this study will be then presented and some defect engineering techniques used to fabricate high quality SiGe layers discussed.

I.2. SiGe alloys properties

I.2.a. Crystal structure

Si, Ge and SiGe alloys have the same diamond crystallographic structure. This structure consists of two face-centered-cubic lattices displaced by one quarter of the unit cell’s diagonal. This structure is shown in **Figure I.2**, with the lattice constant a being the side length of the cubic unit cell. Each atom in the structure is covalently bonded to its four nearest neighbors with a distance of $\frac{\sqrt{3}a}{4}$.

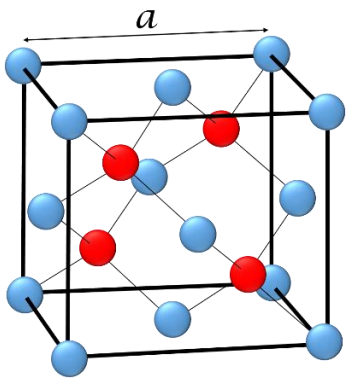

Figure I.2 Diamond crystal structure. Blue atoms are located in the center of the faces as well as the apexes of the cubic cell while red atoms are located inside the cubic cell in the tetrahedral sites

I.2.b. Phase diagram

The binary phase diagram of the Si-Ge system from Stöhr (Stöhr and Klemm 1939) is shown in **Figure I.3**. Si and Ge are completely miscible in all proportions and both materials can be alloyed as $Si_{1-x}Ge_x$ with any value of $0 \leq x \leq 1$. There is only one solid or one liquid phase irrespective of the Ge ratio and temperature considered. We can also note that the melting

point of SiGe alloys decreases continuously with the Ge concentration, i.e. from 1414°C for silicon down 938 °C for germanium.

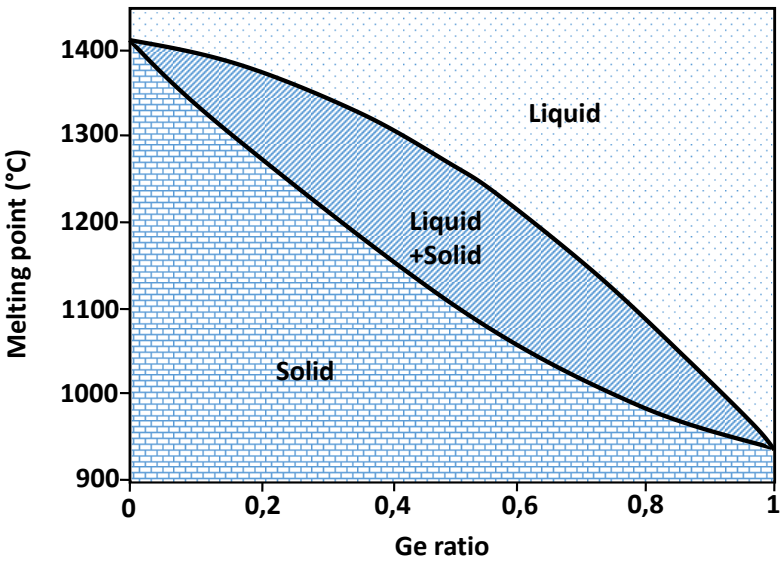

Figure I.3 Binary phase diagram of the Si-Ge system. After (Stöhr and Klemm 1939)

I.3. SiGe heteroepitaxy on Si

I.3.a. Epitaxy concept and growth modes

Epitaxy consists in the growth of a single-crystalline layer on a single-crystalline substrate. The layer grown will most of the time adopt the same crystalline structure as the substrate underneath. The term “Homo-epitaxy” will be used when the substrate and the layer are of the same material (for example: Si on Si) and the term “Hetero-epitaxy” used when the two materials are different e.g. SiGe on Si.

Crystal growth consists in transferring species (atoms or molecules) from a “reservoir” (a gas, a liquid or a solid) into the layer being deposited. When an atom or molecule arrives at a crystal surface, it can be trapped by a periodic potential imposed by the crystal. The minima of that potential form a regular network of adsorption sites (terraces, step edges, kinks and so on) on the surface. The growth mode and the morphology of an epitaxial layer are determined by (i) the surface free energy of the substrate γ_s , the surface free energy of the film γ_l and the interfacial free energy γ_i; as well as (ii) the strain inside the layer. Three major growth modes are generally distinguished (illustrated in **Figure I.4**):

- When $\gamma_s > \gamma_l + \gamma_i$, the growing layer tends to cover the substrate completely to eliminate the contribution of the high substrate surface energy γ_s. Adatoms diffuse on the surface and incorporate at step edges. This leads to the layer-by-layer growth

mode, also known as the Frank–van-der-Merwe (FM) growth mode (**Figure I.4(a)**). FM growth results in smooth 2D layers and is typical of homo-epitaxy.

- When $\gamma_s \leq \gamma_l + \gamma_i$, it is energetically favorable to keep the uncovered substrate area as high as possible. This is achieved by the formation of three-dimensional (3D) islands directly on the surface of the substrate. This growth mode is known as the Volmer–Weber (VW) mode (**Figure I.4(b)**). This 3D growth mode is typically observed when the layer material is too different from the substrate.
- When a crystalline layer is grown on a substrate made of a different material, there might be a non-negligible lattice mismatch between the two crystalline structures. In this case, the film surface might become three-dimensional after an initial layer-by-layer growth for a few atomic monolayers (**Figure I.4(c)**). This scenario, known as the Stranski–Krastanov (SK) growth mode, is typical of the growth of Ge films on Si surfaces. In the SK growth mode, the system starts with layer-by-layer growth. As the film gets thicker, the chemical influence of the substrate diminishes, and the surface energies of the substrate and the layer become essentially the same. At the same time, elastic strain accumulates in the growing film. Above a given thickness (4 atomic monolayers or ~ 6 Å for pure Ge on Si), 3D islands start to form on the surface.

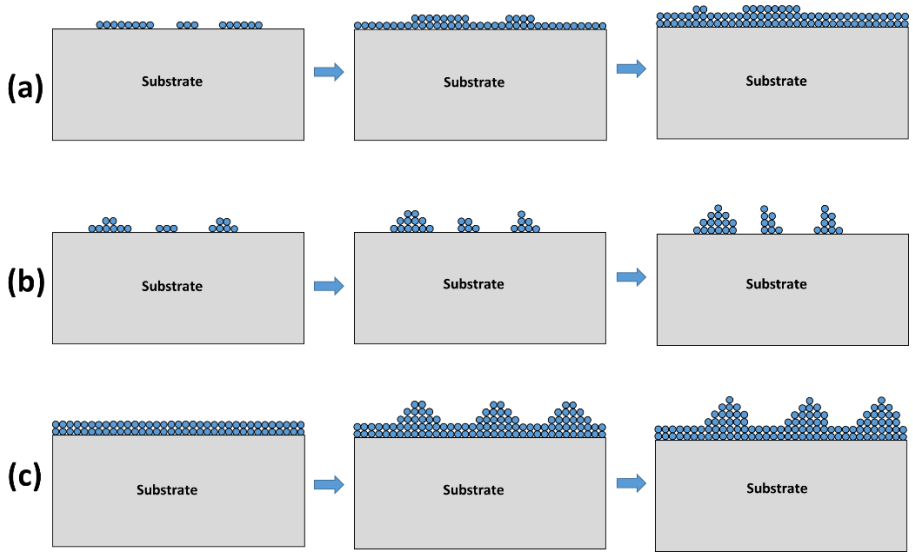

Figure I.4 Schematic diagram showing the major modes of epitaxial growth: a) Frank–van-der-Merwe; (b) Volmer–Weber; (c) Stranski–Krastanov

I.3.b Strain relaxation

In the case of SiGe heteroepitaxy on Si, the lattice constant of Ge (a_{Ge}=5.65785 Å) is 4.18% larger than that of Si (a_{Si}=5.43105 Å). The lattice parameter of $Si_{1-x}Ge_x$ alloys is given to a first approximation by a linear interpolation between the Si and Ge lattice parameters. This interpolation is known as Vegard's law:

$$a_{SiGe}(x) = a_{Si} + (a_{Ge} - a_{Si})x \qquad \textbf{E.q. I.1}$$

A more precise determination of the $Si_{1-x}Ge_x$ lattice parameter based on experimental measurements has been proposed by Dismukes et al (Dismukes et al. 1964). This deviation from the Vegard's law is parabolic:

$$a_{SiGe}(x) = 0.0263x^2 + 0.205x + 5.43105\ (\text{Å}) \qquad \textbf{E.q. I.2}$$

This relationship will be used for composition calculations in the chapters to come.

As illustrated in **Figure I.5**, a $Si_{1-x}Ge_x$ layer with x > 0 epitaxially grown on a Si substrate will be under compressive stress.

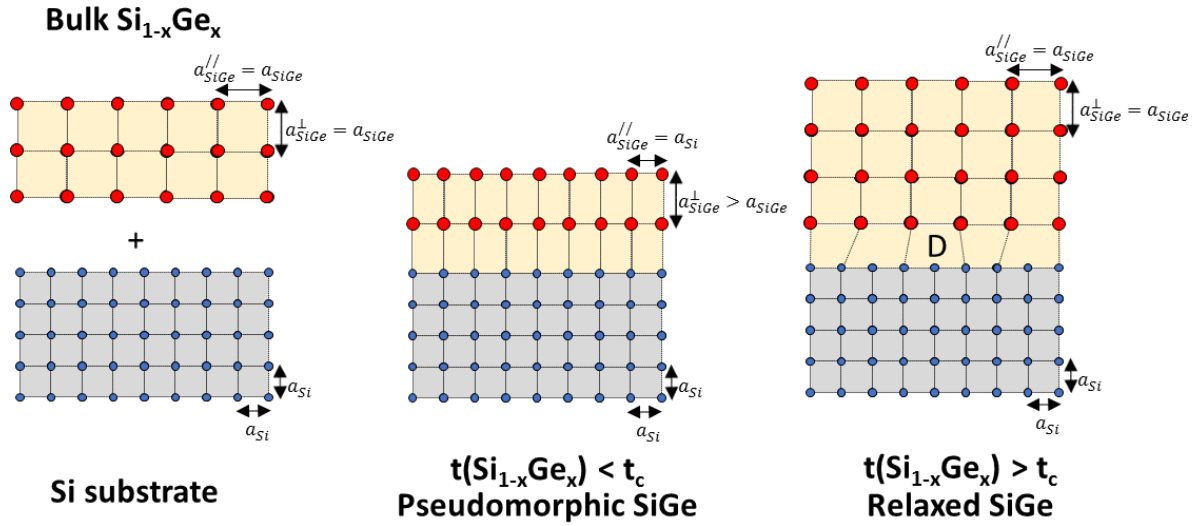

Figure I.5 Schematic diagrams of the atomic arrangement when growing a SiGe layer epitaxially on a Si(001) substrate.

Perfect epitaxial growth (i.e. pseudomorphic growth) of such a strained heteroepitaxial layer is only possible as long as its thickness does not exceed a critical thickness t_c (Van Der Merwe 1963)(Matthews et al. 1970). Above the critical thickness t_c, the strain is relaxed progressively through the formation of misfit dislocations (D).

The critical thickness for plastic relaxation can be calculated using the model of Matthews and Blakeslee (Matthews and Blakeslee 1974). In this model, the strain energy relaxed by the introduction of misfit dislocations is counter balanced by the energy needed to generate the dislocation. t_c is given by:

$$t_c = \frac{b(1-\upsilon cos^2\theta)}{8\pi(1+\nu)\varepsilon cos\lambda}\ln(\frac{\alpha t_c}{b}) \qquad \textbf{E.q. I.3}$$

Where t_c is the critical thickness for plastic relaxation, b is the magnitude of the misfit dislocation's Burgers vector, υ is the epitaxial layer's Poission ratio and ε is the lattice mismatch strain between the epitaxial layer and the substrate. θ is the angle between the misfit dislocation line and the Burgers' vector, while λ is the angle between the Burgers vector and a line in the interface perpendicular to the dislocation line. Finally, α is a factor related to the energy of the dislocation core.

Other models have been proposed in the literature for t_c. The People and Bean model (People and Bean 1985) is based on a localization of the dislocation self-energy in a finite space region:

$$t_c = \frac{1.9.10^{-2}\text{Å}}{f^2}\ln\left(\frac{t_c}{4\text{Å}}\right) \qquad \textbf{E.q. I.4}$$

Where f is the lattice mismatch between the epitaxial layer and the substrate, i.e. $f = \left(\frac{a_{SiGe}-a_{Si}}{a_{Si}}\right) \approx 0.042x$ where x is the Ge content.

The critical thickness for plastic relaxation was recently revisited by Hartmann et al. (Hartmann et al. 2011). They showed that plastic strain relaxation was postponed and more gradual in rather high Ge content layers grown at low temperatures. For instance, the critical thickness for plastic relaxation inferred from X-ray Diffraction (XRD) was, for Ge content 22% and above, approximately two times higher than predicted by the People and Bean's theory. Those results are summarized in **Figure I.6**.

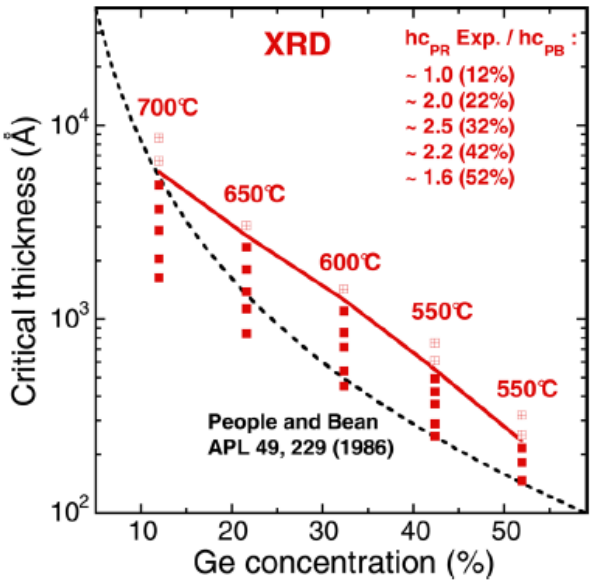

Figure I.6 People and Bean (dotted line) and experimental critical thickness for plastic relaxation (solid line) inferred from the various thickness and Ge content SiGe layers grown at different temperatures (see the insets). The solid squares correspond to layers seen as fully strained in X-Ray Diffraction, while the open, crossed squares correspond to layers seen as plastically relaxed in XRD (Hartmann et al. 2011)

A pseudomorphic SiGe layer on a (001) Si substrate surface has a tetragonally distorted unit cell with in plane $a_{SiGe}^{//}$ and perpendicular $a_{SiGe}^{\perp}$ lattice constants given by :

$$a_{SiGe}^{//} = a_{Si} \text{ and } a_{SiGe}^{\perp} = a_{SiGe} + \frac{2C_{12}}{C_{11}}(a_{SiGe} - a_{Si}) \qquad \textbf{E.q. I.5}$$

Where C_{ii} are the cubic elastic coefficients in the contracted index notation for the $Si_{1-x}Ge_x$ layer.

Above the critical thickness t_c, the strain is relaxed progressively through the formation of misfit dislocations (D). In order to quantify the residual stress in the SiGe layer, we use the macroscopic degree of stain relaxation R which is given by :

$$R = \frac{a_{SiGe}^{//} - a_{Si}}{a_{SiGe} - a_{Si}} \qquad \textbf{E.q. I.6}$$

Below the critical thickness, the layer is pseudomorphic and $a_{SiGe}^{//} = a_{Si}$ In this case R=0 which means that the layer is still fully strained.

Above the critical thickness, the layer starts relaxing, with an in-plane lattice constant $a_{SiGe}^{//}$ which increases until it reaches the bulk SiGe lattice parameter, i.e. $a_{SiGe}^{//} = a_{SiGe}$. In this case, R=1 and the layer is fully relaxed.

As described above, plastic strain relaxation takes place through the nucleation and propagation of dislocations which degrades the SiGe layer's quality. In addition to dislocations, several crystal defects can occur in the layer during crystal growth. The most common defects are described in the next section.

I.3.c. Defects

I.3.c.i. Point defects

All real crystals contain imperfections which locally disturb the regular arrangement of atoms. There are two categories of point defects: Native (or intrinsic) defects and impurity-related (or extrinsic) defects. Native point defects pre-exist in the crystal lattice (for instance in the pure silicon lattice), while impurity-related defects are due to the voluntary (or un-voluntary) introduction of foreign impurities (dopants for example).

The four types of point defects are illustrated for a simple cubic structure in **Figure I.7**:

- A vacancy is formed by the removal of an atom from an atomic site (**Figure I.7(a)**)
- A self-interstitial atom is the introduction of an atom (of the same type) into a non-lattice site (**Figure I.7(b)**)
- A substitutional atom is an impurity atom replacing an atom of the host lattice (**Figure I.7(c)**)
- A foreign interstitial is the introduction of an impurity atom into a non-lattice site (**Figure I.7(d)**)

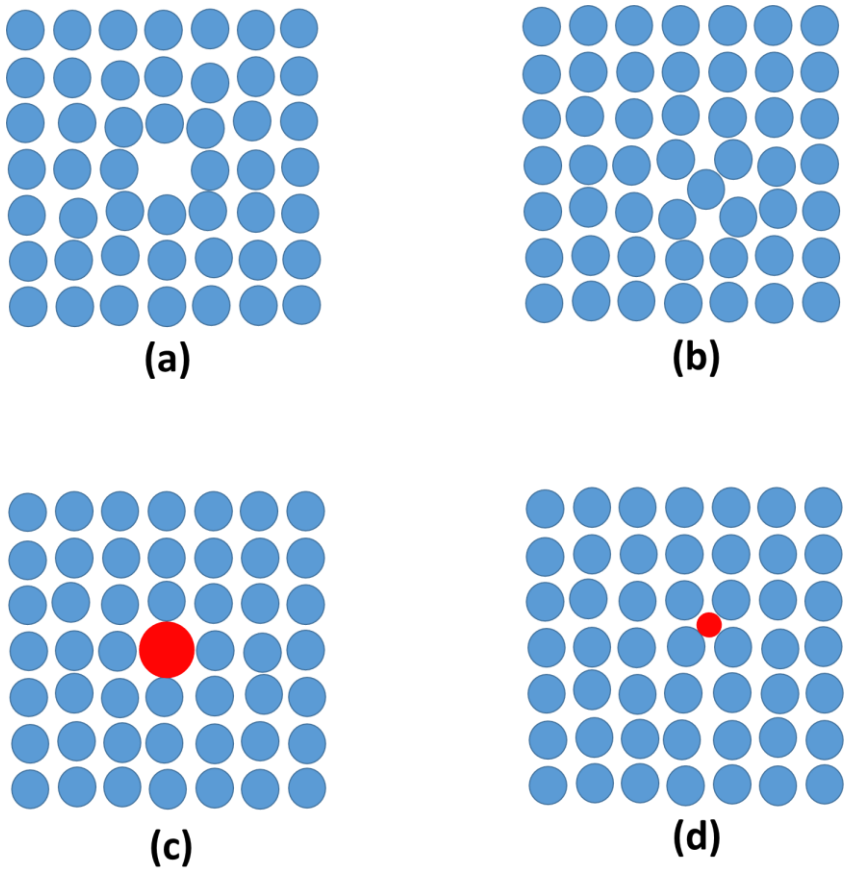

Figure I.7 Schematic diagram of (a) a vacancy, (b) a self-interstitial atom, (c) a substitutional impurity atom and (d) an interstitial impurity atom in a (001) plane of a simple cubic crystal

A stress field will be applied on the neighboring atoms of the lattice with the introduction of such defects. The stress can be tensile (vacancies or substitutional impurities smaller than the host atoms) or compressive (bigger substitutional or interstitial atoms). This stress field will locally modify the lattice and therefore change the electrical and physical properties of the materials. Finally, those defects can move inside the lattice and propagate the deformations.

The unintentional introduction of such defects during SiGe heteroepitaxy on Si is quite rare if the growth conditions are well controlled.

I.3.c.ii. Dislocations

Dislocations are linear defects, along which the interatomic bonding is disturbed compared to a perfect crystal. In the core of the dislocation, along its line, there are dangling bonds and local strains exceeding the limits of the continuum elasticity theory. There is around the core a strained region, in which the interatomic bonds are distorted by small amounts (Ayers 2007).

A dislocation is characterized by its line vector **l** and it Burgers' vector **b**. The line vector **l** is the vector along the dislocation line. The Burgers' vector **b** is the dislocation displacement vector. It is given by a closed path around the dislocation core, the so-called Burgers' circuit. The Burgers' vector completes the path around the dislocation line with respect to a similar path within a perfect reference crystal.

There are two basic types of dislocations, edge dislocations and screw dislocations. In an edge dislocation, **b** is perpendicular to **l**. Therefore, edge dislocations are sometimes referred to as 90° dislocations. Such dislocations may be formed by the insertion of an extra half-plane spanned by **l** and **b×l** (see **Figure I.8(a)**). In a screw dislocation, **b** is parallel to **l**, resulting in the terminology 0° dislocation. This kind of dislocation is built by a shift of one part of the solid by an amount **b** as shown in **Figure I.8(b)**. Dislocations may also have a mixed character with an edge and a screw component, and these are generally denoted by specifying the angle between **b** and **l.**

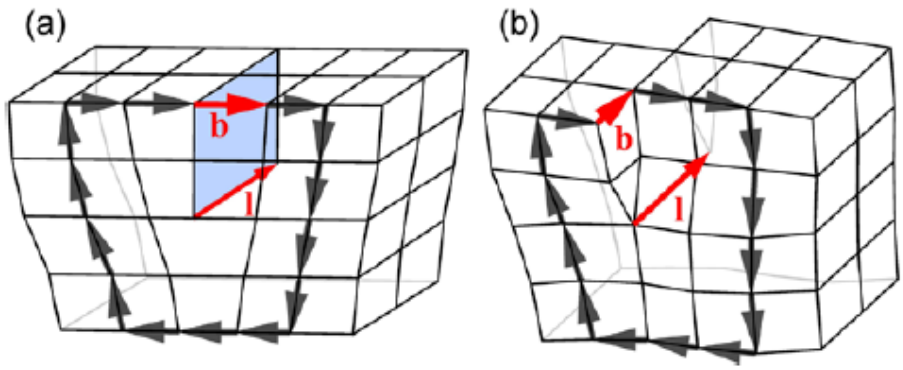

Figure I.8 (a) Edge dislocation and (b) screw dislocation. b and l denote the Burgers vector and the dislocation-line vector, respectively (Pohl 2013)

Geometrical considerations show that a dislocation line can neither begin nor end within the crystalline solid (Nabarro 1952)(Hirth and Lothe 1982). A dislocation line therefore either forms a closed loop within the crystal, or it begins and ends at an interface of the crystal. If a force acts on the crystal, the dislocation line can move along specific planes through the crystal. During gliding, the dislocation moves on crystal planes, as shown in **Figure I.9.** Such displacement is termed glide when it is produced by a single dislocation, and slip when it is produced by a number of dislocations. The total number of atoms and lattice sites is conserved in such motions. For pure edge dislocations the process can only occur along slip planes which contain both the Burgers' vector and the dislocation line. Pure screw dislocations can glide along any plane, since **l** and **b** are parallel.

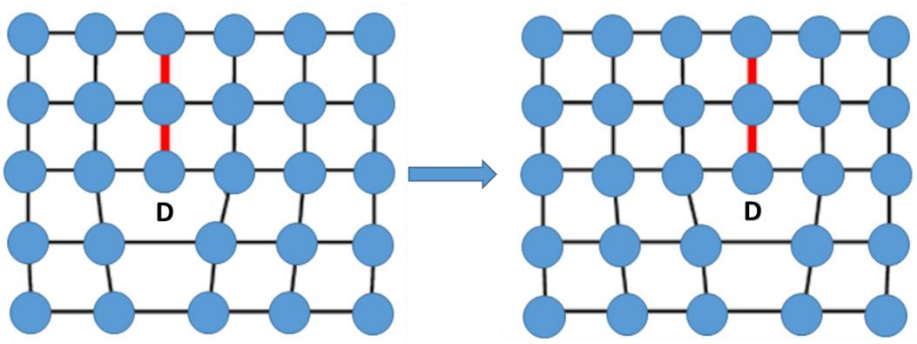

Figure I.9 An edge dislocation gliding

We previously outlined how an originally strained epitaxial layer in a pseudomorphic heterostructure may relax some strain thanks to misfit dislocations. Let us now discuss plastic strain relaxation in more details. To reduce strain in an epilayer with a thickness $t > t_c$, the introduction or omission of a lattice plane is favorable, creating a dislocation line at the layer/substrate interface. Since the dislocation line can neither begin nor end within a crystal, its ends must lie at the surface. There are two configurations fulfilling this condition (Matthews and Blakeslee 1974). One is based upon a dislocation line with a suitable Burgers' vector already existing in the substrate and terminating at its surface. As illustrated in **Figure I.10(a)**, the dislocation is replicated in the layer and forms a threading dislocation, i.e. a dislocation penetrating the layer. Under the action of strain, the dislocation line bends and glides along the interface (from position 1 to 2). A strain-relaxing misfit segment of the dislocation line is then created at the interface. Another mechanism is the nucleation of a dislocation half loop at the layer surface, illustrated in **Figure I.10(b)**. The half loop expands and glides towards the interface over slip planes, creating two threading segments crossing the layer and a misfit segment at the interface. Both mechanisms lead to the formation of a misfit dislocation network at the interface (**Figure I.10(c)**).

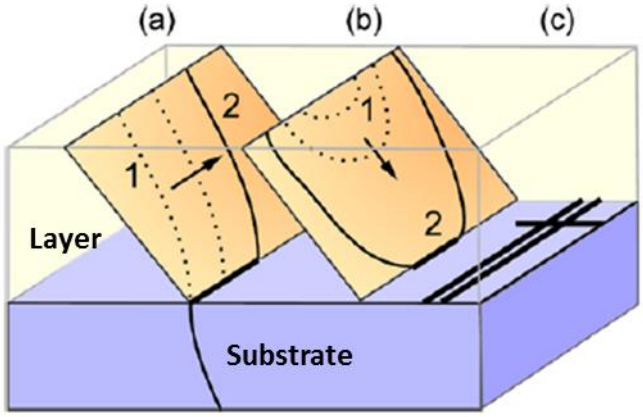

Figure I.10 Generation of a misfit dislocation network (c) at the interface between layer and substrate from (a) a preexisting threading dislocation in the substrate and (b) from the nucleation of a dislocation half loop on the surface (Pohl 2013)

The crystal structure determines in which plane dislocations have the lowest formation energy. SiGe has a diamond structure made of two FCC lattices shifted by a quarter of the diagonal of the cubic cell. All atoms have four nearest neighbors, which are positioned at the vertices of a tetrahedron and connected to the center atom by four bonds. Nearest atoms are along <111> directions, while atoms on the vertices are along <110> directions. By plotting the atom positions in the diamond structure along the <111> directions, one can see that atoms in (111) planes are close packed in bilayers which are connected to other bilayers by one bond per atom (see **Figure I.11**).

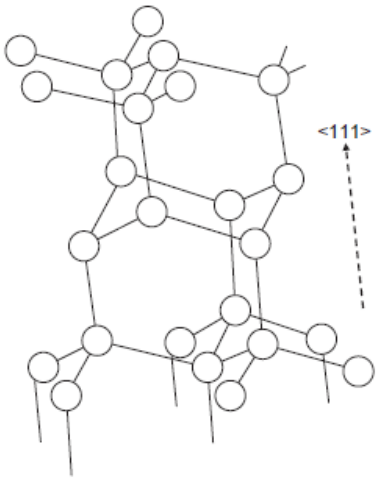

Figure I.11 Atom positions in the diamond structure along the <111> directions (Fleetwood et al. 2009)

Interactions within bilayers are strong and hard to break, while interactions between bilayers are relatively weak. Thus, the lowest energy glide for diamond structures is in the (111) plane. Therefore, dislocation lines in SiGe are generally in (111) planes. To determine the direction of the dislocation line, we need to inspect the directions formed by connecting atoms in the (111) plane. In any (111) plane, there are three <110> directions. These are the connecting lines between the three atoms at the vertices of a tetrahedron in one (111) plane. Due to the two planes fitting with each other after the glide, dislocation lines are usually along the <110> directions, which form a 60° angle with the Burgers' vector (Fleetwood et al. 2009). Hence, this type of dislocation is also called the 60° dislocation. The majority of dislocations in compressively strained SiGe layers are of the 60° type. The formation of a 60° dislocation is illustrated in **Figure I.12**.

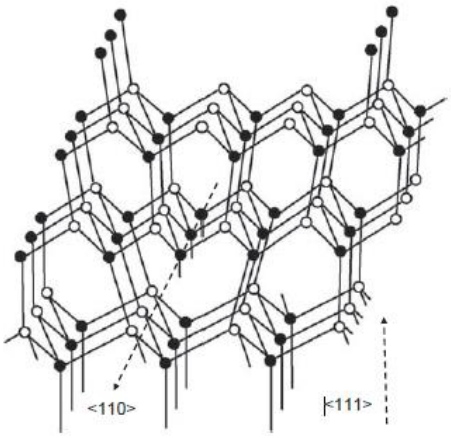

Figure I.12 Formation of 60° dislocation. The dislocation is created along the line with the extra half plane (Fleetwood et al. 2009)

I.3.c.iii. Stacking faults

The diamond structure contains {111} planes in the sequence AaBbCcAaBbCc, as shown in **Figure I.13**. Stacking faults involve the insertion or removal of pairs of the same index (Aa for example). Because layers must be added or removed in pairs, one can drop the double-index notation and describe the packing by the ABCABC sequence where each letter refers to a pair of atomic layers. A stacking fault can occur with an extra pair inserted into the stacking sequence, as in ABCBABC. This is called an extrinsic stacking fault. Another possible type of stacking fault involves the removal of one pair, as in ABCBC. It is called an intrinsic stacking fault. Faults formed between adjacent layers of the same letter do not restore tetrahedral bonding and have high energy.

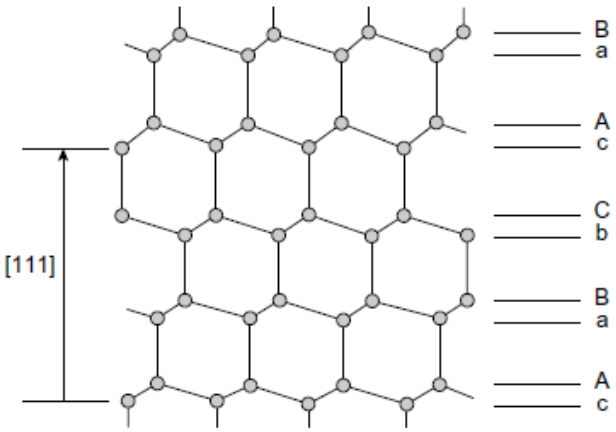

Figure I.13 (10-1) projection of the diamond-cubic lattice showing the stacking sequence of {111} planes (Hull and Bacon 2011)

Stacking faults are planar defects bounded on each side by partial dislocations. These are called partial dislocations because the Burgers' vector is not a lattice translation vector. In other words, the Burgers' vector does not start and end on normal lattice sites of the perfect crystal lattice.

Stacking faults are created by the dissociation of perfect dislocations into partial dislocations. This occurs naturally during the glide of dislocations, as shown in **Figure I.14**. This figure shows the lattice positions on a (111) plane of a diamond crystal, labeled A, along with the lattice sites of the underlying and overlying planes, labeled B and C, respectively. The unit of slip (Burgers' vector) for a perfect dislocation in the overlying layer is the vector $\mathbf{b_1}$. Using the hard sphere model for atoms, this translation takes a sphere in one B position directly to the next B position. However, such a hard sphere will more easily slide first to a C position and then to a B position, along the valleys between the A spheres. These translations are represented by vectors $\mathbf{b_2}$ and $\mathbf{b_3}$, respectively. Thus, the perfect lattice translation $\mathbf{b_1}$ is naturally split into two simpler translations $\mathbf{b_2} + \mathbf{b_3}$, which are the Burgers' vectors associated with two partial dislocations.

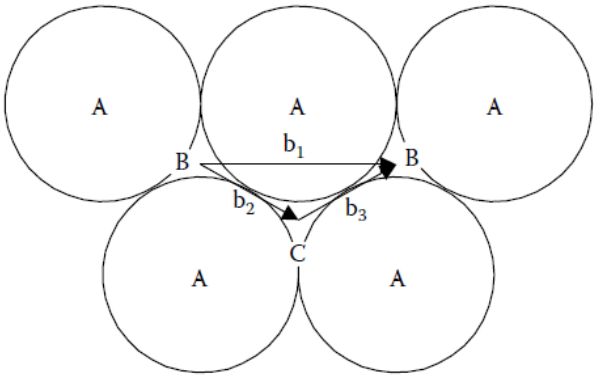

Figure I.14 Schematic drawing of glide on a (111) plane by a perfect dislocation (b_1) and by partial dislocations (b_2 and b_3) (Ayers 2007)

In diamond crystals as Si and SiGe alloys, perfect 60° dislocations may dissociate into 90° and 30° partial dislocations. This necessitates the generation of a stacking fault between the two partial dislocations. This dissociation depends critically on strain and lattice temperature.

I.3.c.iv. Twins

Another type of planar defect resulting from a change in the stacking sequence is the twin. In diamond crystals, twinning occurs almost exclusively on {111} planes. Using the previous stacking notation, a twin boundary in a diamond crystal may be denoted a ABCABACBA. As illustrated in **Figure I.15**, the normal crystal and its twin share a single plane of atoms (the twinning plane or composition plane) with a reflection symmetry around the twinning plane. Twinning involves a change in the long-range order of the crystal; it therefore cannot result

from s simple insertion or removal of an atomic plane, as in stacking faults. Therefore, twins cannot be created by the glide of dislocations. Instead, twinning occurs during crystal growth.

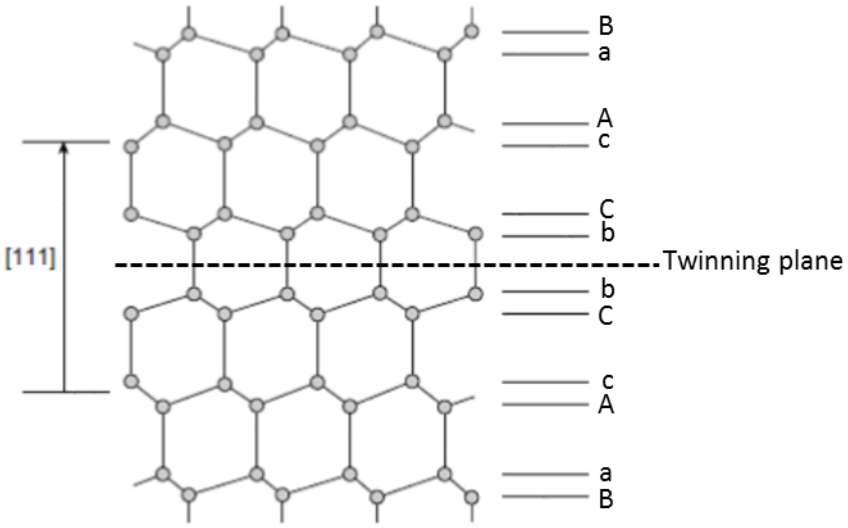

Figure I.15 (10-1) projection of the diamond-cubic lattice showing a twinning defect

At the twinning plane there is a change in crystal orientation, and for diamond structures, twinning occurs about a (111) plane. If the original growth plane was (001), then the surface of the twinned crystal is the (221) plane. Additional twinning may bring the surface to various {221} planes or back to the (001). The (111) twinning plane is always inclined by 54.7° to the (001) surface (Ayers 2007)(Runyan 1965).

It was experimentally shown that strained SiGe layers grown on (111) and (110) Si surfaces are much more susceptible to twin formation compared with growth on (001) Si surfaces (Kuan and Iyer 1991).

I.4. s-SOI technology and SiGe virtual substrates

Several theoretical studies (Fischetti and Laux 1996)(Takagi et al. 1996)(Roldán et al. 1996)(Cressler 2008) have predicted electron and hole mobility enhancements in tensile strained Si. **Figure I.16** illustrates the effect of biaxial tensile stress on the energy bands in Si. In the conduction band of silicon, biaxial tensile strain splits the six-fold degeneracy in the Δ_6-valleys, and lowers the two-fold degenerate perpendicular Δ_2-valleys with respect to the four-fold in-plane Δ_4-valleys in the energy space. Such energy splitting suppresses intervalley carrier scattering between the two-fold and four-fold degenerate valleys, and causes preferential occupation of the two-fold valleys where the in-plane conduction mass is lower. These two effects combine and yield increased electron mobility in strained Si. Similarly, strain splits the valence band degeneracy between the heavy and light hole bands (HH and LH). The resulting

band deformation effectively lowers the in-plane conduction mass, and the splitting suppresses interband scattering between the two bands, improving the in-plane hole mobility.

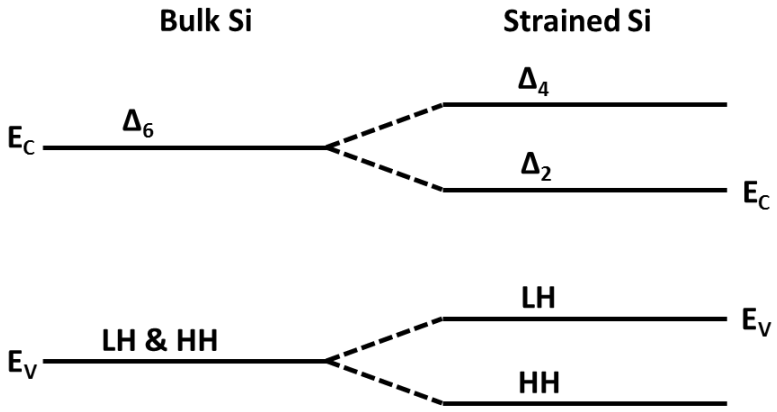

Figure I.16 Schematic illustration of the effects of biaxial tensile stress on the energy bands in Si

Silicon-On-Insulator (SOI) technology consists of a thin layer of Si separated from the host Si substrate by a buried oxide layer (BOX). This technology has received an enormous amount of attention due to its potential to prevent short channel effects and leakage current via the substrate. The process of reference for the fabrication of SOI substrates is the SmartCut™ technology (Bruel et al. 1997) developed by CEA-Leti and commercialized by SOITEC (**Figure I.17**): The donor Si wafer is oxidized, followed by an ionic implantation of hydrogen at a controlled depth. The wafer is then flipped and bonded onto another Si substrate. An anneal step is realized to form cavities in the implanted zone, which creates micro-cracks and finally induce a splitting of the first wafer into 2 parts: A Si layer on top of the BOX and the rest of the substrate, which can be recycled. A surface polishing is performed on the thin transferred silicon layer to obtain a flat SOI wafer, in the end.

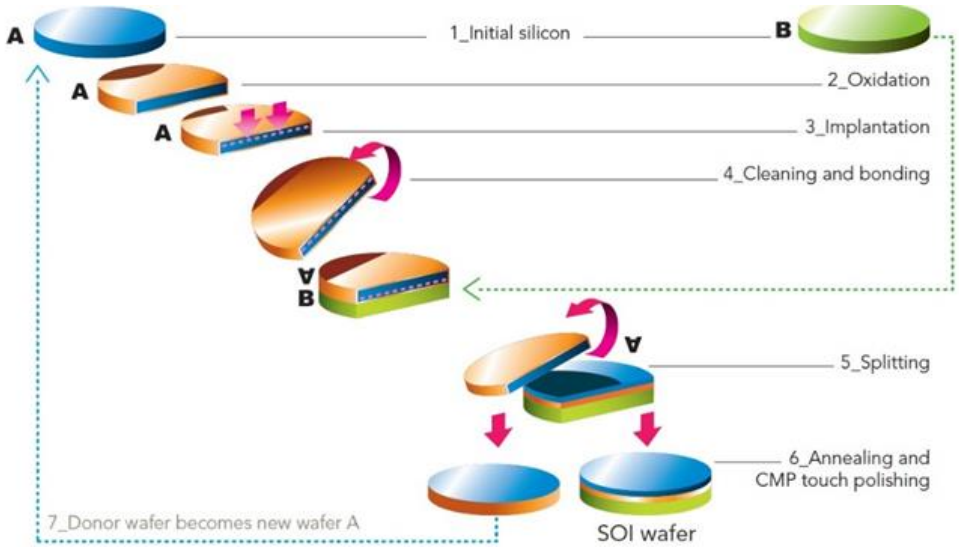

Figure I.17 the Smartcut™ technology (illustration from SOITEC)

It is also possible to combine the benefits described above of strained silicon with SOI to produce strained-Silicon On Insulator (s-SOI) wafers. Using such substrates can improve CMOS circuits: The nMOS transistor benefits from a high electron mobility strained-Si channel, while the pMOS transistor can be made with s-Si or compressed $Si_{1-x}Ge_x$ (grown on top) to increase hole mobility even more.

One method to obtain strained Si relies on the use of $Si_{1-x}Ge_x$ virtual substrate (VS). As illustrated in **Figure I.18**, an almost fully relaxed $Si_{1-x}Ge_x$ layer deposited by epitaxy on a silicon substrate is used for the pseudomorphic growth of a tensile-strained iSi layer on top. The layer of Si is thin enough to be below the critical thickness for plastic relaxation. Its in-plane lattice parameter is therefore that of the relaxed $Si_{1-x}Ge_x$ layer beneath, resulting in tensile strain.

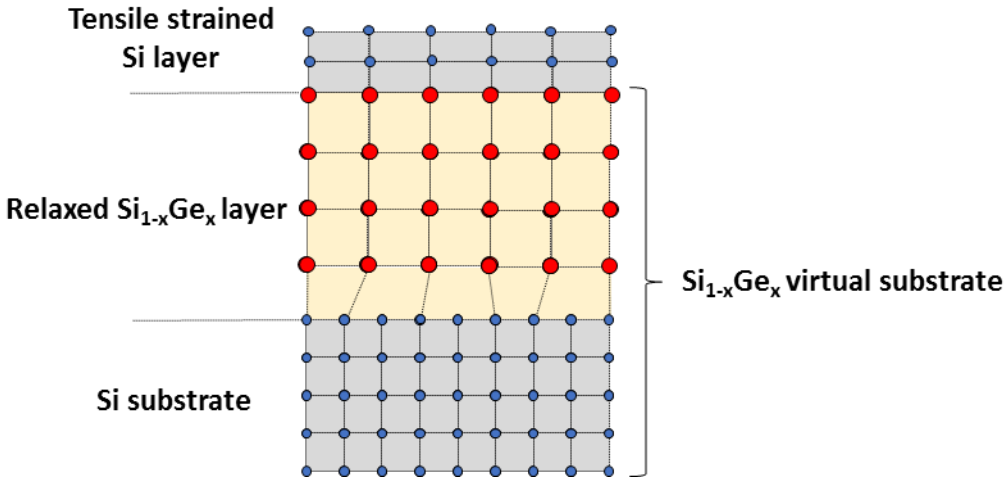

Figure I.18 Schematic illustration of a tensile strained Si layer grown on a $Si_{1-x}Ge_x$ virtual substrate

Measurements made by Munguía et al. (Munguía et al. 2008) on s-SOI 20%, s-SOI 30%, and s-SOI 40% (the % corresponds to the Ge percentage of the SiGe VS underneath) samples, confirmed the theoretical calculations of strain induced indirect band gap shrinkage in strained Si. Further experimental work by Leitz et al (Leitz et al. 2002) showed an enhancement of electron mobility in strained silicon starting from 10% of Ge in the $Si_{1-x}Ge_x$ layer and saturating, with a x 1.8 gain, for Ge concentration greater than 20%. For hole mobility, the enhancement starts for 25% Ge and reaches a gain of 2.2 for concentration greater than 40%. Despite the great potential of s-SOI, however, obtaining s-Si layer is not an easy task: The quality of the virtual substrate of $Si_{1-x}Ge_x$ has a critical impact on the s-Si layer.

I.5. SiGe defect engineering

The formation of relaxed layers, i.e. SiGe virtual substrates, involves the generation of misfit dislocations at the interface between SiGe and the Si substrate underneath, which is

always accompanied by (i) the generation of threading dislocations extending all the way to the SiGe surface and (ii) some surface roughness (i.e. a cross-hatch along the <110> directions). Many efforts, therefore, have been made to create SiGe relaxed crystals as perfect as possible, with a focus on the minimization of the threading dislocations density and surface roughness, as these factors define the practical usability of the SiGe virtual substrate. Since a direct growth of a constant composition SiGe layer on a Si substrate results in a huge density of threading dislocation and a large surface roughness, a variety of fabrication methods have been proposed and developed. Defect engineering in thick SiGe buffers usually relies on the reduction or the confinement of defects in sacrificial regions (in the bulk or at the bottom of the buffers). Other approaches, such as nano-heteroepitaxy, aim at preventing the introduction of dislocations in the first place.

I.5.a. Usual growth strategies

I.5.a.i. Direct growth

The easiest way to obtain a relaxed layer of $Si_{1-x}Ge_x$ on a silicon substrate is to grow the layer directly on the substrate (**Figure I.19**). Historically, the first relaxed layers of $Si_{1-x}Ge_x$ on silicon were obtained that way. The strain accumulated in a SiGe film grown on a Si substrate can be relieved by introducing misfit dislocations at the interface between the SiGe and the Si substrate as described above. Hence, a larger strain requires a denser array of misfit dislocations to be fully plastically relaxed. Misfit dislocations gliding at the same interface strongly interact with each other (Freund 1990)(Schwarz 1998). Dislocation motion is highly impeded by this interaction, resulting in threading segments extending to the surface. When the mismatch is relatively high, a large number of misfit dislocations must participate in the relaxation and many interaction events take place, resulting in a large density of threading dislocations in the film. In contrast, films with lower mismatches can be grown with a relatively small density of threading dislocations. Experimentally, the growth of SiGe films with lattice mismatches larger than ~1% with Si resulted in threading dislocation densities (TDD) exceeding 10^8 cm^{-2} (Fitzgerald et al. 1992)(Mooney et al. 1993). In addition, obtaining high degrees of relaxation with this method involve the deposition of very thick layers (several microns).

Figure I.19 Schematic illustration of $Si_{1-x}Ge_x$ layer grown directly on a Si substrate

I.5.a.ii. Graded buffer

A compositionally graded buffer consists of inserting a series of SiGe intermediate layers, with the Ge concentration gradually increasing with the thickness (**Figure I.20**). The idea is to increase the mismatch strain step by step in order to avoid having highly mismatched hetero interfaces. This way, the dislocations accommodating the lattice parameter difference between the substrate and the top layer are distributed over the thickness of the graded region. Since the dislocations are not attracted to a single interface in the compositionally graded film, they have a greater freedom to move on different planes and reach, if the temperature and therefore their velocity is high enough, the edges of the wafers.

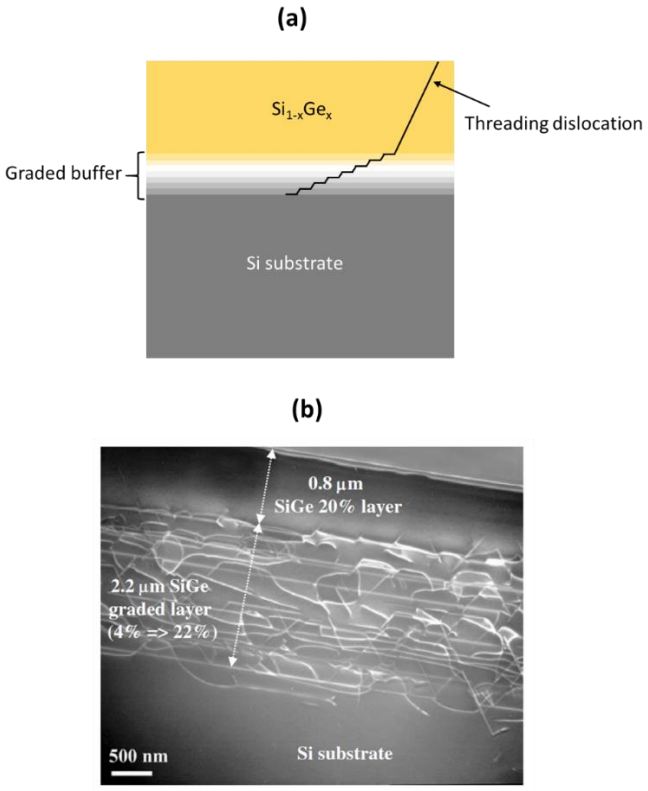

Figure I.20 (a) Schematic illustration of $Si_{1-x}Ge_x$ layer grown with a graded buffer strategy and (b) cross-sectional TEM image of a linearly graded virtual substrate. Note the strong curving by the linearly graded layer of the misfit dislocations, drastically diminishing the threading dislocation density inside the constant composition layer. (Hartmann et al. 2004)

In the compositionally graded region, Ge concentration is gradually increased, either continuously or in steps. A typical grading rate is ~10%/ µm, i.e. the Ge composition is increased by 10% with 1 µm thickness. This graded region, in which most of the misfit dislocations are confined, is capped by a uniform composition SiGe layer with a thickness of ~1 µm, typically (Shiraki and Sakai 2010). The later has typically a degree of strain relaxation in the 96% - 100% range for Ge contents in the 20%-50% range. Such a configuration results in a much lower density of threading dislocations than that of the same constant composition

film grown directly on Si(001). Indeed, a threading dislocation density around 10^6 cm^{-2} is typically obtained in state-of-the-art buffers (Fitzgerald et al. 1991)(Hartmann et al. 2004). This TDD depends on the growth temperature, the grading rate and, to a lesser extent, on the Ge concentration in the top layer.

However, severe surface roughness, with cross-hatch patterns, were seen since the beginning of research on SiGe graded buffers (Fitzgerald et al. 1992) (Hsu et al. 1992)(Shiryaev et al. 1994). The surface root mean square roughness and the Z range associated with 20 µm * 20 µm AFM images of state-of-the-art SiGe VS with a Ge content around 25% are typically in the 2-3 nm and 20-30 nm range, respectively. The crosshatch pattern consists of periodic surface undulations along orthogonal <110> directions (**Figure I.21**). Since those directions are the same as those of misfit dislocations formed in graded regions, it is highly likely that the misfit dislocations are responsible for the roughness formation. Fitzgerald et al. have shown that such cross-hatch patterns are due to the strain fields in the epilayers caused by an inhomogeneous distribution of misfit dislocations (Fitzgerald et al. 1992). However, a different mechanism was also proposed, by which surface steps arising from single and multiple 60° dislocations at the film–substrate interface directly influenced the surface morphology of films (Lutz et al. 1995). A strong correlation between surface roughening and threading dislocation density was seen in some papers, usually when the growth temperature was not high enough. The higher the final Ge concentration was, the higher the threading dislocation density was, despite the use of the same grading rate. The combination of strain fields from underlying multiple misfit dislocations and the resultant surface roughness blocked the motion of threading dislocations, resulting in dislocation pileups (Fitzgerald and Samavedam 1997).

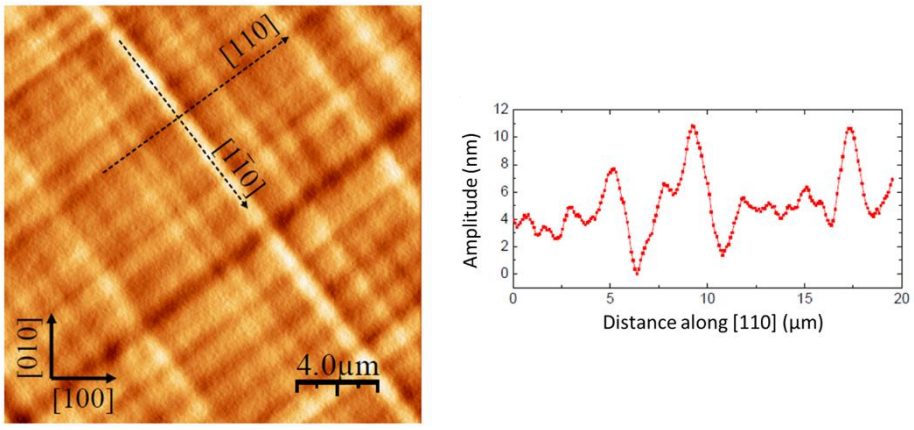

Figure I.21 20 x 20 µm²AFM scan of a relaxed SiGe layer grown on a Si substrate. Image sides are along the <100> directions (left) and a surface amplitude profile (for the same layer) along one of the <110> directions (right) (Bogumilowicz 2005)

Although the compositionally graded buffer method has been the most effective way of reducing the threading dislocation density, it has several drawbacks from the device application point of view. One is that the growth of very thick SiGe layers, more than several µm, is needed to efficiently reduce the TDD. The large thickness is time and material consuming, and can cause some bowing issues (**Figure I.22**) due to differences in thermal expansion coefficients between Si and Ge and the growth of the SiGe strain relaxed buffers on

one side only of wafers (Hartmann et al. 2010). In addition, due to the narrower bandgap and lower thermal conductivity of SiGe compared to Si, increased off-leak currents and self-heating effects in MOS devices could be caused by the larger SiGe thickness. Besides, the large surface roughness requires some Chemical Mechanical Polishing to recover flat surfaces. Moreover, there is an inhomogeneous strain field due to a non-uniform distribution of misfit dislocations close to the surface even after the growth of a thick constant composition layer planarized later on (Sawano et al. 2003) (K. Sawano et al. 2005).

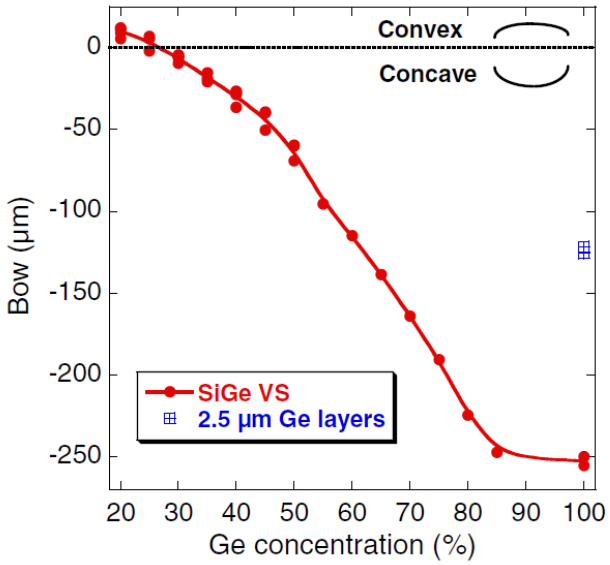

Figure I.22 Wafer bowing as a function of the Ge content of the top layer of SiGe VS or for pure Ge thick layers grown directly on Si. A positive (a negative) value of the bow means that the wafer is convex (concave) (Hartmann et al. 2010)

I.5.a.iii. Low temperature buffer

Low temperature (LT) buffers were initially proposed as a response to the high thickness required by the graded buffer strategy. The low temperature buffer normally consists of a Si buffer layer grown on a Si substrate at low temperature (LT-Si), with a SiGe layer grown on top at higher temperatures (**Figure I.23**). Since surface migration of Si adatoms is largely restricted due to the low growth temperature, point defects are induced in the LT-Si layer. During the SiGe growth that follows, dislocation generation is accelerated as point defects act as low energy sites for dislocation nucleation. Under optimal conditions, the LT-Si layer confines dislocations and prevents threading dislocations from extending too much towards the surface. Important growth parameters to be optimized are the growth temperature and the thickness of the LT-Si layer. The temperature range has to be low enough to generate a high-density of point defects but high enough to result in crystal growth on top. Typical growth temperatures and LT-Si thicknesses required to have high-quality SiGe buffers are 350–450°C and 50–200 nm, respectively.

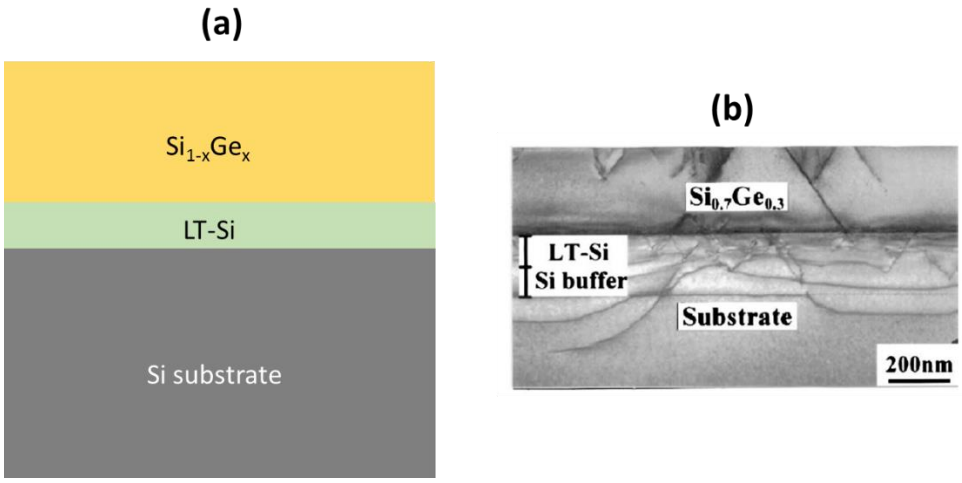

Figure I.23 (a)Schematic of $Si_{1-x}Ge_x$ layer grown with a low temperature buffer strategy and (b) XTEM image of a $Si_{0.7}Ge_{0.3}$ films grown on LT-Si buffer layer (Lee et al. 2002)

The LT buffer method was first applied to SiGe buffer fabrication by Chen et al. in 1996 (Chen et al. 1996). They grew a 50 nm thick LT-Si layer at 400°C and subsequent 300 nm of $Si_{0.76}Ge_{0.24}$ at 550°C, which resulted in a threading dislocation density of ~10^6 cm^{-2}. This first attempt was successful and the growth parameters used were almost optimal.

However, The LT method is not suitable for industrial CVD, as LT growth is difficult due to very low growth rates. In addition, the TDD obtained in the end is still not as low as that of the graded technique.

I.5.a.iv. Ion implantation buffer

The ion-implantation method was introduced to overcome the industrial drawback of the LT buffer method. It relies on the same principle of introducing a defective layer for the formation of SiGe buffers with enhanced strain relaxation and low threading dislocation density. The fabrication procedure usually consists of ion implantation with a peak beneath the pseudomorphic SiGe layer and thermal annealing later on for the promotion of strain relaxation (**Figure I.24**). Ion-implantation defects act as dislocation nucleation sites, which lower the misfit dislocation nucleation energy. Providing more misfit dislocations leads to a higher degree of relaxation compared to the growth without such implantation-induced defects. Since dislocations end at the defective regions, strain relaxation is expected to occur without increasing the threading dislocation density.

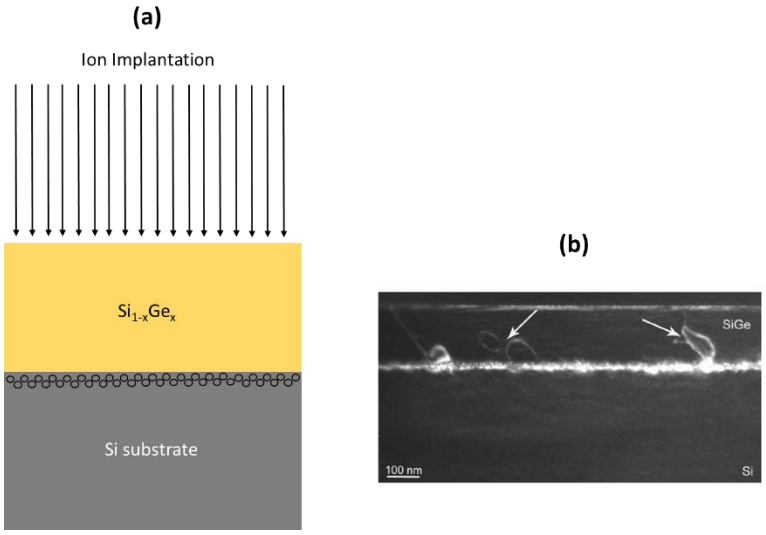

Figure I.24 (a) Schematic illustration of $Si_{1-x}Ge_x$ layer grown with an ion implantation buffer strategy and (b) XTEM image of a SiGe layer after Si^+ implantation and annealing (residual dislocation loops in the SiGe layer are marked by white arrows) (Buca et al. 2009)

In contrast to the LT method, the growth system does not matter for the ion-implantation method, which does not require low-temperature growth. This compatibility with CVD growth makes the ion-implantation method very suitable for mass production. Moreover, defect states created by ion implantation are highly controllable compared to the LT buffer method, since they are determined by conditions of the ex-situ ion-implantation process independently of the growth conditions. Implantation-induced defects are also quite stable at elevated temperatures, whereas it is important to conserve point defects induced by LT growth during the SiGe growth at higher temperatures.

Although this approach sounds promising, the ion-implantation technique results in defect densities which are still quite high (around 10^6 cm^{-2}) (Luysberg et al. 2002) (Cai et al. 2004) (Buca et al. 2009) compared with the graded method.

I.5.b. Nano-heteroepitaxy

In the previous section, three major fabrication techniques for SiGe virtual substrates have been described. The graded buffer method is more advantageous for the purpose of reducing the threading dislocation density. With surface planarization via CMP, almost ideal SiGe virtual substrates with low defect densities are nowadays available for a wide range of Ge concentrations. The only unsolved problem is its large thickness, which is indispensable for this method (the lower grading rate is, the lower the TDD will be => 3 µm thick SiGe VS for 20% of Ge, typically). The strain field fluctuation on the SiGe surface is also problematic. The other two techniques have been shown to facilitate dislocation nucleation by means of intentionally introducing nucleation sources via low-temperature growth or ion bombardment. However, although the issue of the thickness can be overcome by these methods, the TDD is still not as low as that of the graded technique.

In this section, we will present an exploratory method called nano-heteroepitaxy. Instead of removing or annihilating existing defects, this technique is based on a new paradigm: preventing the introduction of defects in the first place. This technique also has the promise of extremely rapid strain relaxation, eliminating the need for very thick SiGe layers.

I.5.b.i. Concept

Nano-heteroepitaxy is a selective epitaxial growth carried out on a substrate that has been patterned to have nanometer-scale seed pads. This may be achieved by etching windows through a dielectric mask. Typically, lateral epitaxial growth proceeds from the seed pads until the coalescence of the growing islands yields a complete layer of the heteroepitaxial material. In this approach, an additional degree of freedom for strain relaxation is introduced which is critical for this technique to work.

As shown in **Figure I.25**, the only stress-relief mechanism for a planar layer is vertical deformation (a), which defines a critical thickness for dislocation formation, as discussed above. In the case of nano-heteroepitaxy the stress can also be relieved by lateral deformation (b) in the epitaxial layer along with vertical (c) and lateral (d) deformations in the substrate mesas.

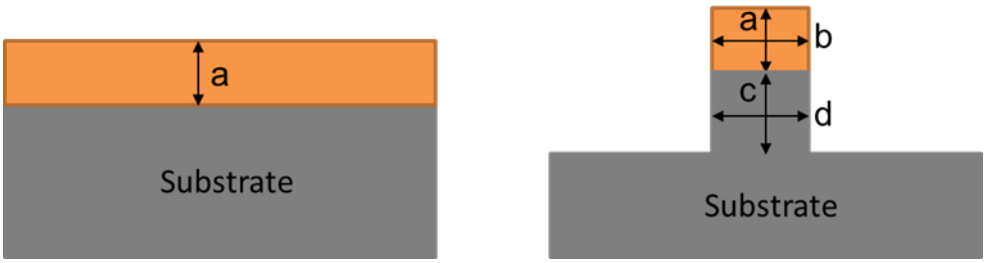

Figure I.25 Stress-relief mechanisms available in a conventional planar heteroepitaxy sample (left) and in nano-heteroepitaxy islands (right)

In the following sections of this literature review, we will first outline some theoretical models of strain relaxation in heteroepitaxial layers on nano-patterned substrates. Then, we will present a state of the art of heteroepitaxy on patterned substrates.

I.5.b.ii. Theory

Nano-heteroepitaxy on a Noncompliant Substrate

Luryi and Suhir (Luryi and Suhir 1986) developed the first theoretical model for strain in nano-heteroepitaxial materials. They assumed that the lattice-mismatched hetero-epitaxial

material makes rigid contact with a noncompliant substrate exclusively at round seed pads having a diameter 2l, as shown in **Figure I.26**.

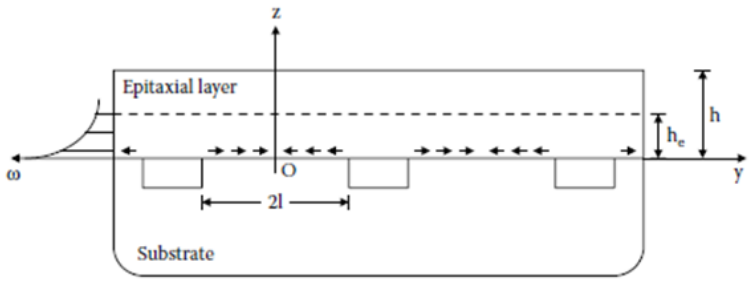

Figure I.26 Nano-heteroepitaxial growth on a patterned substrate. The substrate has been patterned with round seed pads having a diameter 2l. The y-axis lies in the plane of the interface. The z-axis is perpendicular to the substrate and passes through the center of this seed pad. The heteroepitaxial layer may coalesce into a single layer by lateral growth, as shown. The total thickness of the heteroepitaxial layer is h. The strain energy profile ω , for the pad mid cross section is shown on the left (Ayers 2007) (Luryi and Suhir 1986)

Here, the y-axis lies in the plane of the interface along one of the two high symmetry directions (with the assumption that pads are arrayed in a square). The z-axis is perpendicular to the substrate and passes through the center of a seed pad. The figure shows a heteroepitaxial layer that has coalesced into a single layer by lateral growth, and the total thickness of the heteroepitaxial layer is h. It is assumed that the areas between the seed pads are sufficiently wide and that there is no interference of strain fields from adjacent pads. In this situation, if the substrate is unstrained, then the in-plane stress in the epitaxial growth is given by:

$$\sigma_y = f\frac{E}{1-v}\chi(y,z)e^{-\frac{\pi z}{2l}} \qquad \textbf{E.q. I.7}$$

where f f is the lattice mismatch strain, E is the Young's modulus, v is the Poisson ratio, and the function χ, which characterizes the lateral stress distribution, is given by

$$\chi(y,z) = 1 - \frac{\cosh(ky)}{\cosh(kl)} \;\; for\; z \le h_e \; and \; \chi(y,z) = 1 \; for \; z \ge h_e \qquad \textbf{E.q. I.8}$$

where h_e is the effective range for the stress in the z direction, to be determined below, and the interfacial compliance parameter k is given by

$$k = \left[\frac{3}{2}\frac{1-v}{1+v}\right]^{1/2}\frac{1}{h_e} = \frac{\zeta}{h_e} \qquad \textbf{E.q. I.9}$$

The strain energy density per unit volume is

$$\omega(y,z) = \frac{1-v}{E}{\sigma_y}^2 \qquad \textbf{E.q. I.10}$$

It is the highest at y=0. The strain energy per unit area may be found by integrating over the thickness of the epitaxial layer and takes on a maximum value at y=0, which is

$$E_s = \int_0^h \omega(0,z)dz = \frac{E}{1-v}f^2 h_e \qquad \textbf{E.q. I.11}$$

In this calculation, there is little contribution from $z > h_e$. It is therefore a good approximation to use the form of χ for $z \leq h_e$. The right-hand side of **E.q I.11** defines the characteristic thickness h_e, which is then given implicitly by

$$h_e = h\left(\left(1 - \operatorname{sech}\left(\frac{\zeta l}{h_e}\right)\right)^2 \left(1 - e^{-\frac{\pi h}{l}}\right)\frac{l}{\pi h}\right) = h\left[(\varphi\left(\frac{l}{h}\right)^2\right] \qquad \textbf{E.q. I.12}$$

The right-hand side of this equation defines the reduction factor ϕ(l/h). For l>>h, ϕ → 1 asymptotically, but for l<<h, ϕ ∝ (l/h)$^{1/2}$. In other words, $h_e \approx h$ for l>>h, and for l<<h

$$h_e \approx \frac{\xi^2 l}{\pi} \qquad \textbf{E.q. I.13}$$

Following People and Bean (People and Bean 1985), the real energy density E_d associated with a single linear dislocation located at a distance h from the free surface of the film is

$$E_d = \frac{Gb^2}{10\pi a\sqrt{2}} \ln\frac{h}{b} \qquad \textbf{E.q. I.14}$$

where G = E/2(1+v) is the shear modulus of the film material, b is the Burgers' vector of the dislocation and a is the bulk lattice constant of the alloy film

To find l_{max}, the maximum pad half diameter for which no dislocation is generated for a layer in the l<<h case, we equate **E.q. I.11** and **E.q. I.14**, substitute h by l in **E.q. I.14** and use **E.q. I.13** to find

$$\frac{(\xi f)^2}{\pi} l_{max} = \frac{1-v}{1+v}\frac{b^2}{20\pi a\sqrt{2}} \ln\left(\frac{l_{max}}{b}\right) \qquad \textbf{E.q. I.15}$$

For an $Si_{1-x}Ge_x$ alloys with a content x of Ge, f = 0.042x, $\xi = 0.89$, $v = 0.27$, b = 4Å and a = <a(x)> = 5.54Å. This yields $l_{max}(x)$ in Å by the equation

$$x^2 l_{max} = 42\ ln\left(\frac{l_{max}}{4}\right) \qquad \textbf{E.q. I.16}$$

l_{max} as a function of the Ge concentration x is drawn in **Figure I.27**.

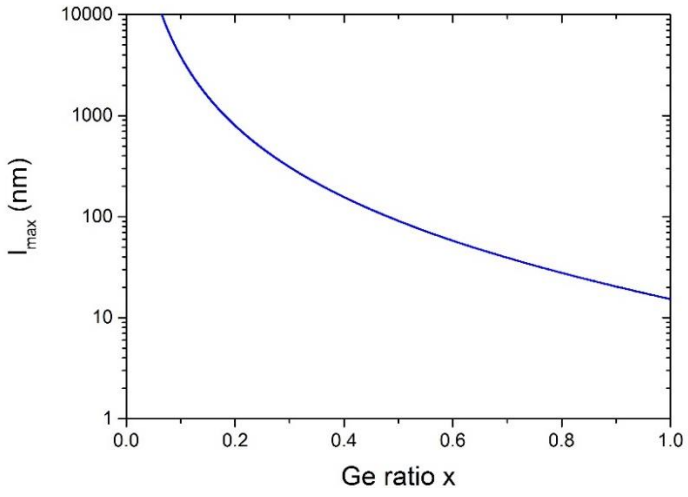

Figure I.27 Maximum pad radius to avoid dislocation formation as function of the Ge ratio x in $Si_{1-x}Ge_x$ for growth on a non-compliant silicon substrate

We can also draw the following table of l_{max} values for discrete Ge concentrations

Ge ratio x in $Si_{1-x}Ge_x$	l_{max} (nm)	Pad diameter $2l_{max}$ (nm)
0.2	800	1600
0.4	160	320
0.6	60	120
0.8	28	56
1	16	32

Table I.1 Maximum pad radius to avoid dislocation formation for a variety of the Ge contents in $Si_{1-x}Ge_x$ for growth on non-compliant silicon

Nano-heteroepitaxy with a Compliant Substrate

Zubia and Hersee (Zubia and Hersee 1999) extended this theory to include the effect of substrate compliance and named the approach nano-heteroepitaxy. Here, the strain is shared between the substrate (pillar) and the epitaxial layer. If the epitaxial layer is grown coherently (without misfit dislocations) on a compliant substrate with lattice mismatch strain f, then the substrate and epitaxial layer will be strained in an opposite sense, such that

$$\varepsilon_{epi} - \varepsilon_{sub} = f \qquad \textbf{E.q. I.17}$$

where ε_{epi} and ε_{sub} are the in-plane strains in the epitaxial layer and substrate, respectively. If we neglect the bending stresses, the force balance in the structure dictates that

$$\sigma_{epi}\, h_{epi} + \sigma_{sub}\, h_{sub} = 0 \qquad \textbf{E.q. I.18}$$

where h_{epi} and h_{sub} are the thicknesses of the epitaxial layer and substrate (or rather the height of the pillar in our case), respectively, and σ_{epi} and σ_{sub} are the corresponding in-plane stresses. Due to the biaxial nature of the stress, the stress–strain relationships are

$$\sigma_{epi} = \frac{E_{epi}}{1-\nu_{epi}}\,\varepsilon_{epi} \qquad \textbf{E.q. I.19}$$

$$\sigma_{sub} = \frac{E_{sub}}{1-\nu_{sub}}\,\varepsilon_{sub} \qquad \textbf{E.q. I.20}$$

where E_{epi} and E_{sub} are the Young's moduli and ε_{epi} and ε_{sub} are the Poisson ratios. The simultaneous solution of these three equations yields

$$\varepsilon_{epi} = \frac{f}{1+\left(K\frac{h_{epi}}{h_{sub}}\right)} \qquad \textbf{E.q. I.21}$$

$$\varepsilon_{sub} = \frac{-f}{1+\left(\frac{1}{K}\frac{h_{sub}}{h_{epi}}\right)} \qquad \textbf{E.q. I.22}$$

Now, combining the compliant substrate theory with the model of Luryi and Suhir, we have

$$\sigma_{epi} = \varepsilon_{epi}\frac{E_{epi}}{1-v_{epi}}\chi(y,z)e^{-\frac{\pi z}{2l}} \qquad \textbf{E.q. I.23}$$

The in-plane strain in the nano-heteroepitaxial material is given by

$$\varepsilon_{epi} = \frac{f}{1+\left(K\frac{1-\exp(-\frac{\pi h_{epi}}{2l})}{1-\exp(-\frac{\pi h_{sub}}{2l})}\right)} \qquad \textbf{E.q. I.24}$$

And the l_{max} relationship becomes

$$\left(\frac{f}{1+\left(K\frac{1-\exp(-\frac{\pi h_{epi}}{2l})}{1-\exp(-\frac{\pi h_{sub}}{2l})}\right)}\right)^2 \frac{\xi^2}{\pi} l_{max} = \frac{1-v}{1+v}\frac{b^2}{20\pi a\sqrt{2}}\ln\left(\frac{l_{max}}{b}\right) \qquad \textbf{E.q. I.25}$$

Let us consider $Si_{1-x}Ge_x$ alloys with a Ge content x on Si compliant pads with [100] Young modulus $E_{epi} = 130.2 - 28.1x$ [GPa] and $E_{sub} = 130.2$ [GPa] (Levinshteĭn et al. 2001). By making the assumption that $h_{epi} = h_{sub}$ in the pillar, the l_{max} equation in Å becomes

$$\left(\frac{0.042x}{1+\left(\frac{130.2-28.1x}{130.2}\right)}\right)^2 l_{max} = 0.074\ln\left(\frac{l_{max}}{4}\right) \qquad \textbf{E.q. I.26}$$

Solving this equation for a pure germanium (x=1) yields l_{max} = 70nm which is higher than l_{max} = 16nm when the compliancy is not considered. This means that the compliancy in the pads compliancy significantly reduces the constraints on pad size.

l_{max} as a function of Ge ratio x for compliance as well as Luryi and Suhir theory is drawn in *Figure I.28*.

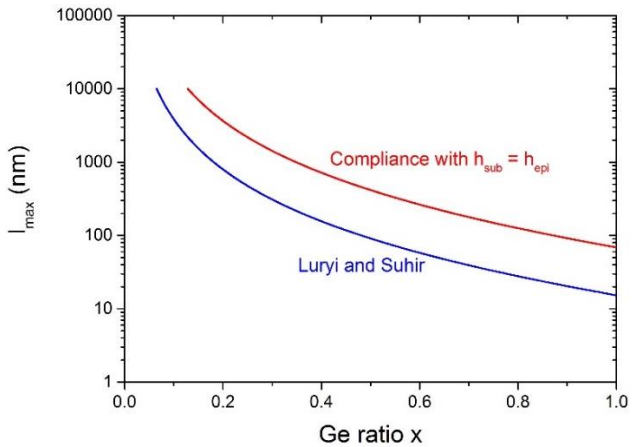

Figure I.28 Maximum pad radius to avoid dislocation formation as function of the Ge ratio x in $Si_{1-x}Ge_x$ for compliant silicon pads (red) and values coming for Luryi and Suhir theory (non-compliant substrate) (blue)

We can also draw the following table of l_{max} values for usual Ge ratios considering compliance as well as Luryi and Suhir's theory

Ge ratio x in $Si_{1-x}Ge_x$	l_{max} (nm) Luryi and Suhir	l_{max} (nm) Compliance
0,2	800	3600
0,4	160	720
0,6	60	265
0,8	28	125
1	16	70

Table I.2 Maximum pad radius to avoid dislocation formation for different Ge ratios considering compliance as well as Luryi and Suhir theory

I.5.b.iii. State of the art

Dislocation reduction/elimination by reduced area epitaxy in the SiGe/Si system was verified by several studies (Fitzgerald et al. 1989) (Fitzgerald et al. 1990) (Noble et al. 1990) (Nishida et al. 1992) (Stoica and Vescan 1993) (Holländer et al. 1997). For instance, defect free growth of 280 nm thick $Si_{0.81}Ge_{0.19}$ was claimed by Fitzgerald et al (Fitzgerald et al. 1990) on 70 µm wide mesas patterned in a Si substrate. This result seems inconsistent as 70 µm wide mesas are, for $Si_{0.81}Ge_{0.19}$, outside the theoretical limits fixed by Luryi and Suhir model (Luryi and Suhir 1986). These studies give some insight about the advantages of proceeding with the growth on patterned substrates. However, they do not allow to verify the nano-heteroepitaxy concept since the growth is performed exclusively on the mesas structures and no coalescence process is tested.

It is worth noting that Luryi and Suhir assume perfect coalescence between epitaxial nano-crystals and full relaxation of $Si_{1-x}Ge_x$ outside of the nano-pillars surface area. Still, an important issue is the coalescence of laterally overgrown crystals to form a large area film. This has been extensively investigated when fabricating SOI substrates thanks to selective epitaxial overgrowth of silicon on seeds surrounded by SiO_2 (Kitajima et al. 1989). Stacking faults and twins were identified as the main type of defects. Other studies more closely oriented towards Ge epitaxial lateral overgrowth (Langdo et al. 2000) (Li et al. 2003) (Leonhardt et al. 2011) (Kim et al. 2014) (Salvalaglio et al. 2015) showed the same type of planar defects occurring at the coalescence front. Equally, a study by Hikavyy et al (Hikavyy et al. 2014) on Si and SiGe fin merging showed the presence of similar defects.

In 2007, Lee et al (Lee et al. 2007) explored a novel substrate patterning technique for heteroepitaxial growth of Ge on Si templates. This technique is based on PS-PMMA diblock copolymer patterning creating a two dimensional array of 10 nm diameter holes with 20 nm spacing as illustrated in **Figure I.29**. These patterns correspond perfectly to a nano-

heteroepitaxy approach in terms of geometry and dimensions. In their study, two cases were considered: 1) Si nano-patterned templates and 2) 30 nm thick SiO_2 templates patterned on Si wafer for selective epitaxial growth of Ge in holes. A growth of 300 nm of Ge was performed. Results show that surface roughness was improved for growth on nano-patterned templates compared to growth on planar substrates. Further characterizations showed a defects density of ~10^6 cm^{-2} for the nano-patterned substrates and a density of ~10^7 cm^{-2} for the planar substrate. Eventually, the authors did not go further in the analysis of the defects generated with this approach.

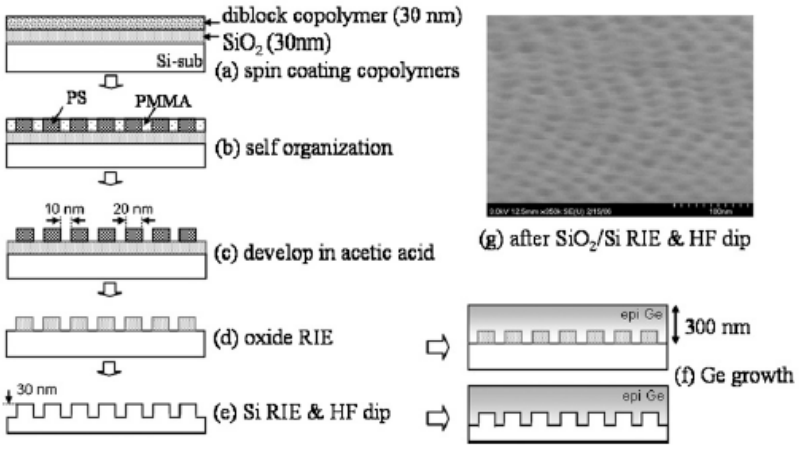

Figure I.29 Schematic fabrication procedure of Ge heteroepitaxial growth on a nano-patterned template (Lee et al. 2007)

To the best of our knowledge, no other study corresponding to the nano-heteroepitaxy approach (in terms of geometry and dimensions) and dealing with Si, Ge or SiGe related materials has been published to date.

I.6. Conclusion

The first part of this chapter was dedicated to the basic properties of SiGe alloys, with crystallographic structure and alloy miscibility shown. An overview of SiGe heteroepitaxy on Si has been presented, with several concepts introduced such as epitaxy growth modes, strain relaxation and crystalline defects.

The second part focused on the context of this work which demands high quality SiGe virtual substrates. Common SiGe defect engineering strategies were described, and the theoretical foundations of the nano-heteroepitaxy approach were provided as well as a brief state of the art.

In the following chapters, we will investigate the nano-heteroepitaxy approach in an industrial epitaxial growth tool, with new integration schemes, pattern sizes and materials compared to prior works. We will also provide an in-depth morphological and structural analysis of the nano-pillar seeds and layers, leading to a better understanding of the nano-heteroepitaxy mechanisms.

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CHAPTER II:
Integration, growth and characterization

Contents of chapter II

II.1. Introduction

The concept and theoretical models of nano-heteroepitaxy have been introduced in Chapter I. The main idea is to carry out an epitaxial growth on a patterned substrate with nanometer-scale seed pillars. This way, growth fronts from individual nano-pillars coalesce to form a complete 2D layer. This selective growth may be achieved by etching windows through a masking material. A robust nano-template fabrication scheme was therefore implemented to meet nano-heteroepitaxy conceptual and theoretical requirements.

In the first part of chapter II, the nano-template integration scheme will be introduced with a specific focus on the lithography, surface preparation and epitaxial growth steps. Diblock copolymer patterning will be described, followed by mainstream wet and dry surface preparations used before SiGe epitaxy. A detailed overview of SiGe epitaxy by Chemical Vapor Deposition will then be given.

The different characterization methods used during the PhD will be exposed in the second part of this chapter. The related physical concepts will be presented and the experimental characterization tools described. A clear distinction will be made between morphological (surface, shape) and structural (composition, relaxation and defectivity) characterization methods.

II.2. Nano-template integration scheme

As illustrated in **Figure II.1**, a nano-template integration scheme was specifically designed for the nano-heteroepiatxy of SiGe alloys. It starts from slightly p-type doped nominally on-axis 300 mm bulk Si(001) wafers. A masking layer a few tens of nm thick is then deposited to serve as a template for lithography. Next, a diblock copolymer patterning is performed followed by an etching step and resist stripping, resulting in cylindrical cavities with a few tens of nanometers diameters and a hexagonal compact configuration. The masking material nature and thickness as well as the nano-template dimensions will be described at the beginning of each experimental chapter, as these were varied for different experiments. In the following sections, we will describe more precisely three important technological steps: the diblock copolymer patterning, the surface preparation preceding epitaxy and the epitaxial technique used for the selective epitaxial growth of SiGe alloys.

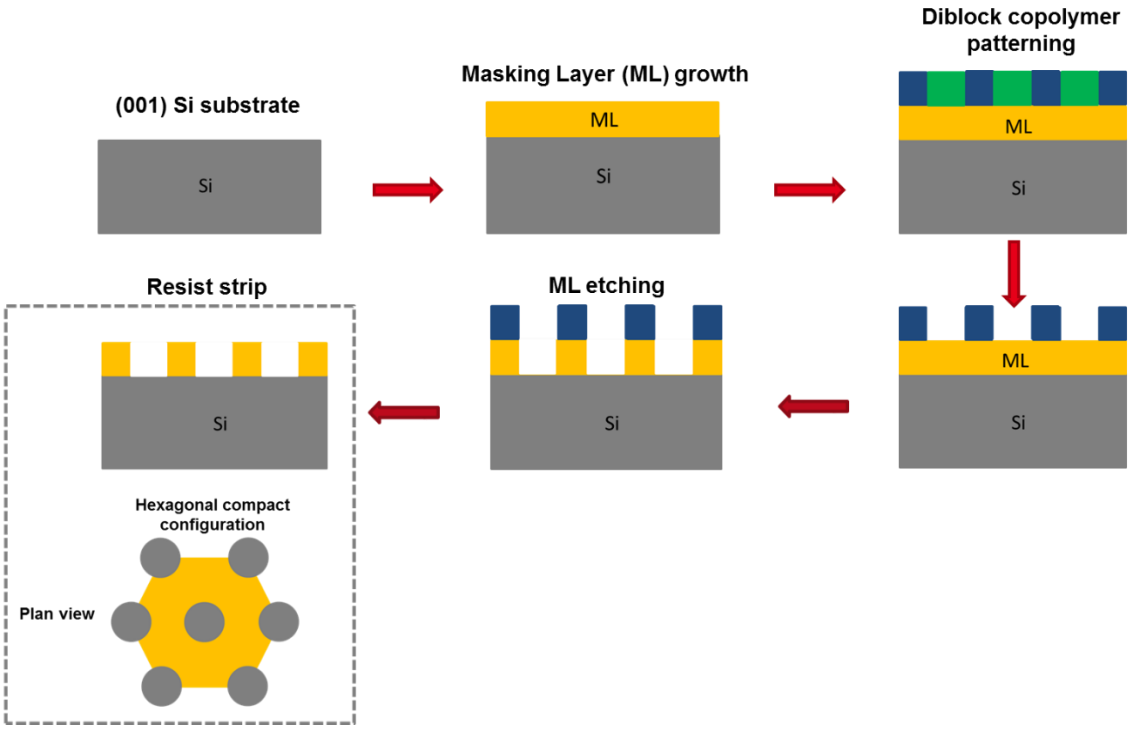

Figure II.1 Nano-template integration scheme

II.2.a. Diblock copolymer patterning

Different block-copolymers have been studied for sub-10 nm patterning. Polystyrene-block-poly(methyl methacrylate)(PS-b-PMMA) is commonly used for block-copolymer patterning given its well-known properties and its easy synthesis (Tiron et al. 2012) (Chevalier et al. 2013). Proportions of PS and PMMA on the block-copolymer determine pattern shape (Hamley 2004), and lamellar or cylindrical PMMA patterns in a PS matrix can be created (Segalman 2005).

PS-b-PMMA was used in our experiments to create cylindrical nano-cavities for the nano-heteroepitaxy of SiGe alloys. The surface of the masking layer is modified to be PS or PMMA attractive. PS/PMMA bloc copolymers are then dispensed on the surface, followed by an annealing step to achieve self-assembling. During this step, PMMA forms vertical cylinders surrounded by PS all over the masking layer surface. Next, the PMMA is removed with a solvent and the remaining PS is used as a mask to etch the hard mask layer required for selective epitaxy. After etching the resist is removed. At the end of this sequence, the hard mask layer contains cylindrical cavities with a nanoscale diameter which will be used as a template for the nano-heteroepitaxy experiments.

PS and PMMA solutions, provided by Arkema® under the tradename Nanostrength® EO, were spin-coated then annealed on a Sokudo Duo™ track.

As an advanced patterning technique already available at CEA-LETI, diblock copolymer patterning with a pitch of either 35 nm or 43 nm was used for SiGe nano-heteroepitaxy. The purpose of this PhD being the study and characterization of the growth step, no further developments were made on the lithographic process itself.

II.2.b. Surface preparation

A key technological step before any kind of epitaxy is the surface preparation of the substrate. Epitaxy should duplicate the crystalline structure of the substrate into the layer, and so the epitaxy quality can be significantly impacted by the condition of the substrate surface (presence or not of amorphous silicon oxide layers, polymers or etching residues). Depending on the toolset available for surface preparation and the nature of the substrate itself, several strategies may be used to obtain contamination-free surfaces. In our configuration, the starting point is a nano-patterned Si substrate, commonly with SiO_2 used as the hard mask. This means that our substrate cannot withstand high temperatures H_2 in-situ bakes (typically higher than 1050°C for 1 minute; 1100°C for 2 minutes as the CEA-LETI standard) in order to remove the 0.8-1 nm thick layer of native or chemical oxide, which is initially present on the surface. Instead, the following sequence is typically used (Hartmann 2017):

1) A "HF-last" wet treatment (Abbadie et al. 2004) is used to remove the native oxide. The wafer is dipped in hydrofluoric acid diluted in deionized and de-oxygenated water (dilution typically between 0.2 and 1 %) to remove the surface SiO_2. The dissolution reaction is as follows:

   $$SiO_2 + 4HF \rightarrow 2H^+ + SiF_6^{2-} + 2H_2O$$ (Bühler et al. 1997)

   The etch rate of thermal SiO_2 (the most type of SiO_2) is of the order of 1.2 to 1.4 nm/min for 0.2% HF. During the final step, the wafer is rinsed in deionized and deoxygenated water to remove all traces of HF. The wafer is then dried by for instance isopropyl alcohol vapors, before being loaded as quickly as possible into the load-lock chambers of the epitaxy tool, in an inert atmosphere (purified N_2). After such a wet cleaning, approximately 85% of the Si dangling bonds are occupied by hydrogen atoms. The remaining 15% are mainly occupied by fluorine atoms as well as oxygen and carbon contaminants (Meyerson et al. 1990) (Trucks et al. 1990)
2) A H_2 in-situ bake then takes place at a lower temperature to remove all O, F or C surface contaminants. A surface perfectly passivated by hydrogen atoms is then obtained which is ideal for epitaxy.

An "HF-last" surface is only stable for a few dozens of minutes up to a couple of hours (before the re-growth of a native oxide a few Å thick can be detected by spectroscopic ellipsometry). Minimizing the time between a "HF-Last" wet cleaning and the loading of wafers inside chambers purged with high purity inert gases (such as N_2) is thus mandatory (Wostyn et al. 2014). More and more industrial cluster tools have nowadays in-situ pre-clean chambers that

utilize plasmas to convert native oxide into salts which are sublimated at low temperatures. This way, re-oxidation phenomena and deleterious Q-times are avoided. In this thesis, remote plasma using NH_3 and NF_3 (the so-called "Siconi®" process) was alternatively used for silicon surface preparation (Yang et al. 2010) (Labrot et al. 2016) (Raynal et al. 2018). Exposure to a NH_3/NF_3 remote plasma (followed by a low temperature salt sublimation step at T = 180 °C) was performed at 3 Torr in a controlled atmosphere (H_2, He, Ar) Siconi® chamber (illustrated in **Figure II.2**) connected to an Applied Materials cluster tool. In the case of SiO_2, Siconi chemical reactions are the following:

1) Precursor transformation into etchants in a remote plasma cavity:

$$NF_3 + NH_3 \rightarrow NH_4F + NH_4F.HF$$

2) SiO_2 transformation into a salt at ~30 °C:

$$NH_4F \text{ or } NH_4F.HF + SiO_2 \rightarrow (NH_4)_2SiF_6(solid) + H_2O$$

3) Salt sublimation at T = 180 °C

$$(NH_4)_2SiF_6(solid) \rightarrow SiF_4(gas) + 2NH_3(gas) + 2HF(gas)$$

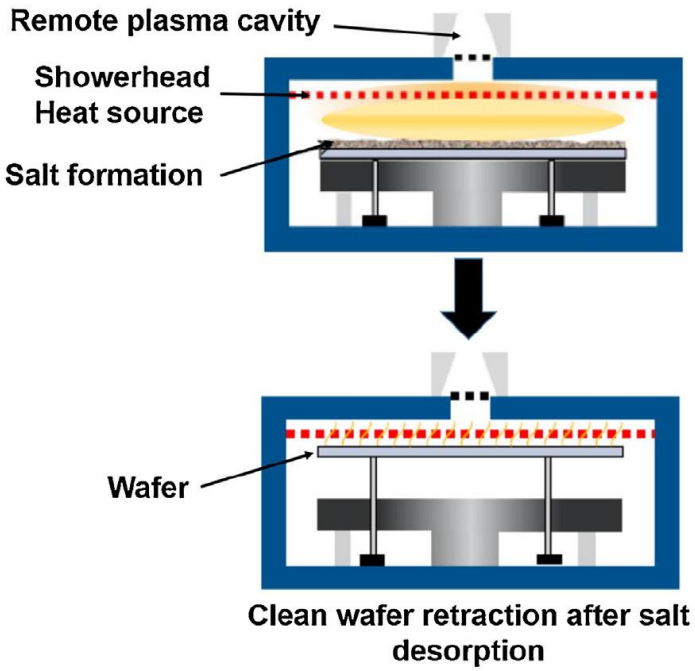

Figure II.2 Siconi plasma clean process (Labrot et al. 2016)

Wet surface preparations were otherwise performed in a 300 mm single-wafer DNS SU 3100 tool.

II.2.c. SiGe epitaxial growth

The development of SiGe epitaxial growth techniques has been highly competitive. Historically, two major techniques were used for the growth of SiGe alloys: Molecular Beam Epitaxy (MBE) and Chemical Vapor Deposition (CVD). MBE is an ultra-high-vacuum technique involving atomic or molecular beams hitting a heated single-crystal substrate on which the epitaxial layers grow. CVD growth is accomplished by flowing gaseous precursors over a heated single-crystal substrate, where epitaxial growth occurs. A large range of pressure may be used and a carrier gas usually makes up most of the flow in the reactor. Each growth technique has advantages and disadvantages, but CVD has been widely adopted by the industry. In fact, CVD has a number of appealing features that make it particularly suitable for manufacturing:

- Use of gaseous precursors instead of solid sources in MBE
- Cleanliness of gases
- Chemistry flexibility
- Process flexibility in terms of temperature and pressure range

In this section, the Si(001) surface condition before epitaxy will be first described then we will present some basic CVD mechanisms as well as the CVD industrial tool used during this PhD thesis.

II.2.c.i. Surface reconstruction

Si substrates with a (001) oriented surface are the most commonly used wafers in the semiconductor industry thanks to superior electronic transport properties and a stable thermal oxide. The atomic configuration on a (001) surface is presented in **Figure II.3**.

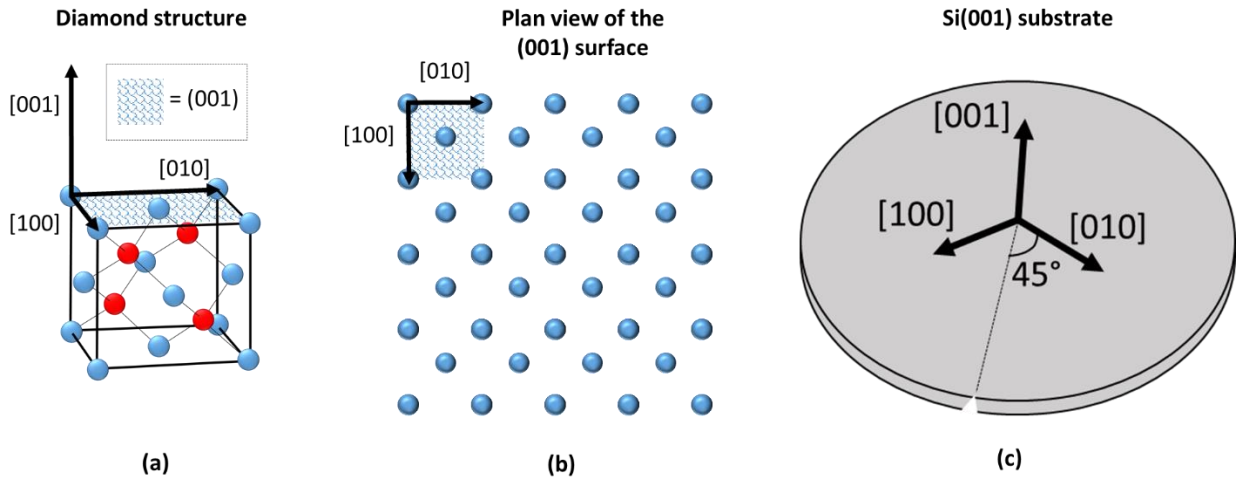

Figure II.3(a) (001) surface in the diamond structure (b) plan view of the (001) surface and (c) Si(001) substrate orientation

The {001} surfaces correspond to the faces of the lattice cube, as illustrated by the meshed upper face of **Figure II.3(a)**. **Figure II.3(b)** shows a plan view of the (001) surface. The spacing between atoms along the <001> crystallographic directions corresponds to the silicon lattice parameter. The distance between atoms is the lowest along the <110> directions. The <100> directions are at 45° on each side of a straight line connecting the center of the substrate to a notch (one of the two <110> directions), as shown in **Figure II.3(c)**.

In the diamond structure, each atom has a coordination number of 4 in a tetrahedral geometry. This means that, on a (001) surface, each Si atom has two dangling bonds. Clearly, such a structure is thermodynamically unstable and the surface of Si(001) will undergo surface reconstruction to achieve a lower energy state. The most stable surface reconstructions for Si (001) are the 2x1 (1x2) reconstructions (Mönch 1979). This surface reconstruction creates π-bonds between two dangling bonds of nearby Si atoms (as represented in **Figure II.4(a)**). These π-bonds are created on each terrace either in the parallel (2x1) or perpendicular (1x2) direction to surface steps (illustrated in **Figure II.4(b)**). The density of dangling bonds is thus lowered by a factor of two as one dangling bond per atom is involved in the reconstruction process. The associated surface free energy is thus also divided by two.

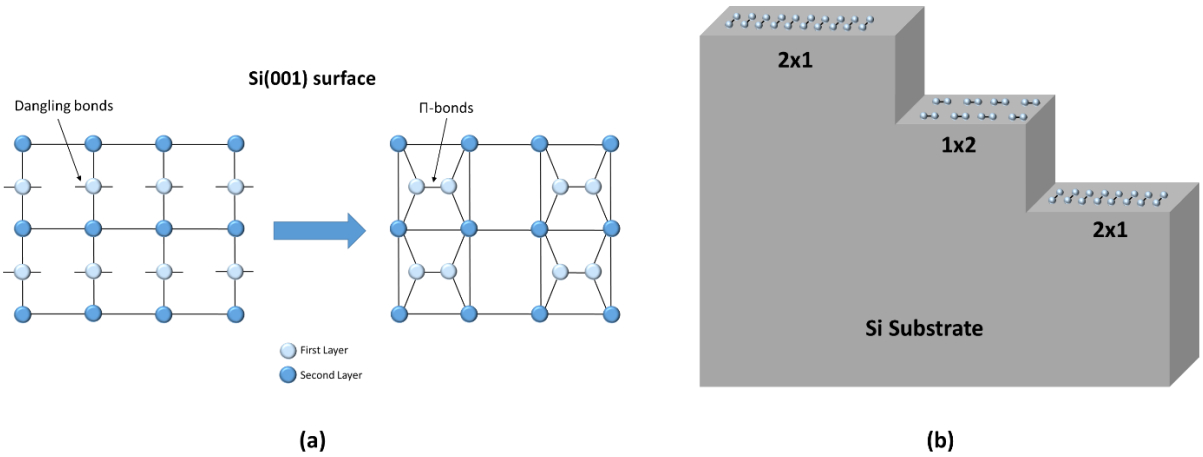

Figure II.4 (a) Si(001) 2x1(1x2) reconstruction process and (b) description of the 2x1 and 1x2 Si(001) reconstructions

Chemical vapor growth depends strongly on the adsorption/desorption processes onto free surface bonds at low temperatures. Surface reconstruction has most likely a strong impact on CVD growth kinetics.

II.2.c.ii. CVD growth

The main problem in studies of CVD kinetics is the complexity of the deposition process (Park and Sudarshan 2001). The difficulty arises not only from the various steps of the CVD process but also from the temperature and concentration gradients, geometric effects, and

gas flow patterns in the reaction zones. Exact kinetic analysis is therefore usually not possible as the kinetic data are reactor dependent.

Figure II.5 shows a simple description of seven steps occuring during a CVD process. These steps include:

1. Transport of reactant gases into the reaction chamber
2. Formation of intermediate reactants form from reactant gases
3. Transport of reactant gases or intermediate reactants to the substrate by convection and diffusion phenomena
4. Absorption of gases onto the heated substrate surface
5. Single or multi-step reactions at the substrate surface (decomposition and recombination) and incorporation into solid film
6. Desorption of product gases from the substrate surface
7. Forced exit of product gases from the system

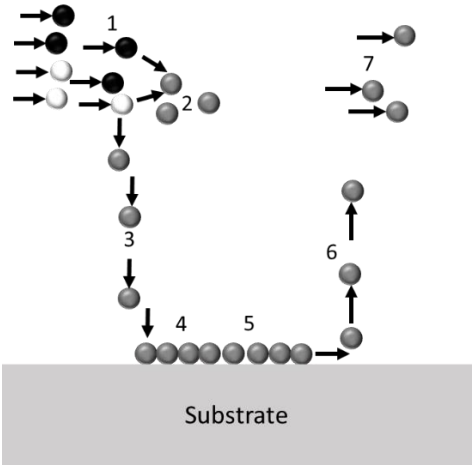

Figure II.5 Schematic diagram of the mechanistic steps that occur during a CVD process

In this model, the steps can be classified into two categories, mass transport (1,3 and 7) and surface reaction steps (2,4,5, and 6). The slowest of these steps determines if the process is mass transport or surface reaction limited. At lower temperatures, the deposition rate is generally surface reaction limited. As the temperature increases, the surface reaction rate rises exponentially, resulting in a mass transport limited regime because transport becomes the slowest step.

Numerous studies on the kinetics and mechanisms of $Si_{1-x}Ge_x$ CVD growth have been made (Greve 1993) (Dutartre et al. 1993) (Hartmann et al. 2002). These studies provide useful information such as activation energies and limiting steps of deposition reactions which are important for the understanding of deposition processes. For instance, it is well known that hydrogen desorption is the limiting step at low temperature for the SiH_4/GeH_4 system. When dealing with the SiH_2Cl_2/GeH_4 system on a CVD tool similar to the one used in this thesis, both high temperature (HT)– transport limited (Bogumilowicz et al. 2005) and low temperature (LT) – surface limited growth regimes (Hartmann 2007) have been identified when growing Si/SiGe heterostructures. The activation energies (associated with the exponential increase with T of

the $Si_{1-x}Ge_x$ growth rate) fall down from the Si - H bond energy (47 kcal mol.-1) down to values close to the Ge - H bond energy (37 kcal. mol.-1) as the Ge content increases.

SiGe growth model

Suh and Lee (Suh and Lee 2000) have proposed a simple growth model for SiGe which has exhibited a very good agreement with experimental data. This model is based on the chemical dissociation of SiH_2Cl_2 and GeH_4 gaseous precursors under the most probable decomposition pathways: $SiH_2Cl_2 \rightarrow SiCl_2 + H_2$ and $GeH_4 \rightarrow GeH_2 + H_2$

Therefore, we can write the following reaction schemes:

- For dichlorosilane:

  $SiH_2Cl_2(g) + v \rightarrow SiH_2Cl_2(s) + nGe(s) \rightarrow Si(s)$

  $SiH_2Cl_2(g) \leftrightarrow SiCl_2(g) + H_2(g)$

  $SiCl_2(g) + v \rightarrow SiCl_2(s) + nGe(s) \rightarrow Si(s)$

- For germane:

  $GeH_4(g) + v \rightarrow GeH_4(s) \rightarrow Ge(s)$

  $GeH_4(g) \leftrightarrow GeH_2(g) + H_2(g)$

  $GeH_2(g) + v \rightarrow GeH_2(s) \rightarrow Ge(s)$

Where v is the vacant site on the surface, g indicates the gas phase and s indicates the adsorption. Under the assumption that the adsorption of HCl and H_2 are negligible (compared with the ones of Si and Ge adspecies), the Si incorporation into films is here assumed to be based on the desorption of Cl atoms. There are two possible ways for a Cl atom to desorb from the surface. One is the direct desorption by breaking bond with Si and the other is the desorption from a Ge atom by migrating to the neighboring Ge site due to the high activation barrier involved in desorbing directly from the Si atom. These are competing processes and the mediation of Ge in Cl desorption in the reactions can be viewed as an additional pathway to direct desorption from Si. In this light, n may be allowed to take values between 0 and 1, which reflects the extent to which the Cl desorption contributes through migrating to neighboring Ge site. The Ge composition x in the film is given by:

$$x = \frac{R(Ge)}{R(Si)+R(Ge)} \qquad \textbf{Eq II.1}$$

Where $R(Si)$ and $R(Ge)$ are the growth rates of Si and Ge sites, respectively. They can be expressed as a function of the chemical reaction constant of each GeH_4 / SiH_2Cl_2 possible decomposition pathway. This leads to the following formulation of the Ge composition x:

$$\frac{x^n}{1-x} = A\frac{P(GeH_4)}{P(SiH_2Cl_2)} \quad \textbf{Eq II.2}$$

Where A is the product of the chemical reaction constants. It may differ for different reactor geometry and source-gas composition. $\frac{P(GeH_4)}{P(SiH_2Cl_2)}$ is the partial pressure ratio. **Eq. II.2** is assumed to be valid in the intermediate temperature range (600 - 900°C) and for operating pressure P in the 10 – 100 Torr range. The best fit with experimental data has been obtained by Suh and Lee assuming n = 1. This is definitely an overestimation of the "real" Ge participation to Cl desorption but it leads to:

$$\frac{x^2}{1-x} = A\frac{P(GeH_4)}{P(SiH_2Cl_2)} \quad \textbf{Eq II.3}$$

Finally, a more empirical model for Ge incorporation has been proposed by Tomasini et al. (Tomasini et al. 2006). This model does not make any assumption about the chemical growth mechanism and fits rather well with experimental data obtained in the 350 - 600°C temperature range (for high Ge content $Si_{1-x}Ge_x$ alloys: x = 0.48 - 0.8). The relationship obtained is rather close to that obtained by Suh et al.:

$$\left(\frac{x}{1-x}\right)^2 = B\frac{P(GeH_4)}{P(SiH_2Cl_2)} \quad \textbf{Eq II.4}$$

Loading effects

When using CVD systems, variations of SiGe growth rates and Ge contents can occur on patterned wafers. Such variations are generally called "loading effects" and are defined as follows:

- **Global loading effects**: Increases of SiGe growth rates and slight increase of the Ge content that occur when switching from a blanket to a patterned Si wafer. The diffusion of adatoms on the dielectrics covered regions towards the Si windows, which act as "sinks", lead to such variations. The overall Si coverage on patterned wafers will mainly dictate the magnitude of such an increase. Additional top surface undulations can also happen, arising from elastic relaxation phenomena, when switching from blanket to patterned wafers.

- **Local loading effects**: Growth rate discrepancies obtained on patterned wafers as a function of the window size and environment. Schematically, the smaller and the more isolated the window will be, the higher the SiGe growth rate will be.

The overall consequence is that, each time a new mask is used, loading effects will have to be recalibrated. Both global and local loading effects have been investigated in the literature (Ito et al. 1995) (Bodnar et al. 1997) (Menon et al. 2001).

II.2.c.iii. Epsilon 3200

Mainframe

An ASM Epsilon 3200 single-wafer epitaxy tool, manufactured by ASM International, was used to grow $Si_{1-x}Ge_x$ layers on nano-patterned 300 mm Si wafers during this work. As illustrated in **Figure II.6**, the mainframe is divided into 3 zones: Front End Interface (FEI), Transfer chamber and Epitaxy chamber.

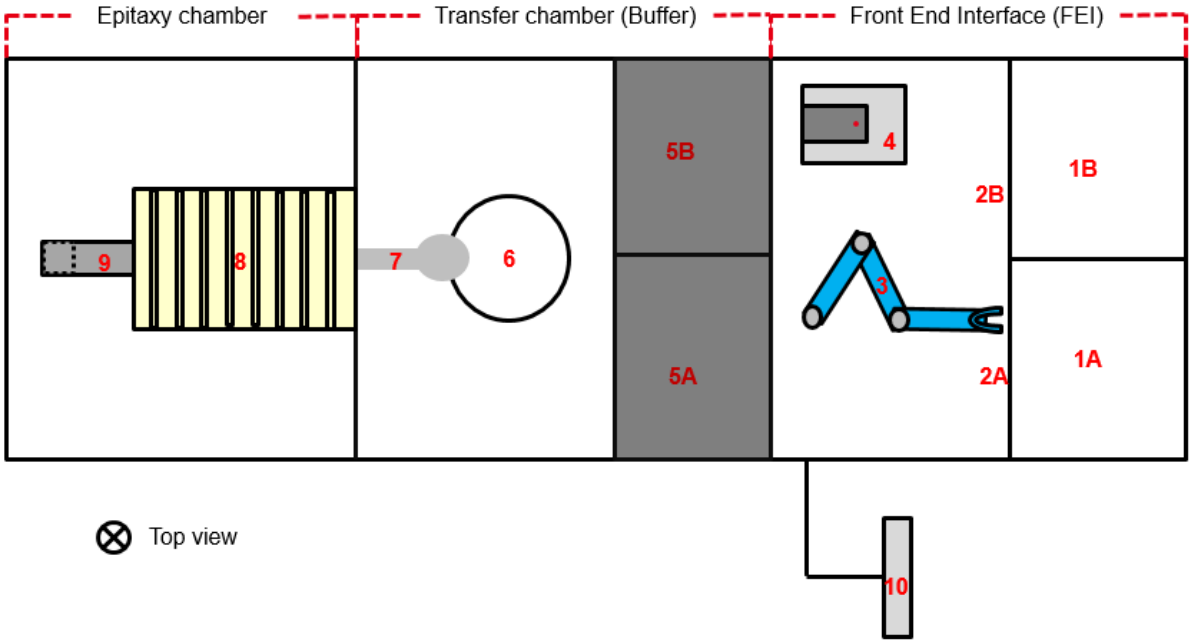

Figure II.6 Top view schematic of the ASM Epsilon 3200 mainframe

The FEI controls wafer load/unload. It contains 2 docks **(1A, 1B)** to hold and lock the wafer carrier (also known as FOUP - Front Opening Unified Pods) into the load ports **(2A, 2B)**. Two FOUPs can be loaded at the same time. A robotic arm **(3)** is used to transfer wafers from the FOUPs into the tool. Wafers alignment is performed by a rotating platform and a laser detecting the notch position **(4)**.

The wafer is then transferred into loadlocks **(5A, 5B)**, which can store up to 25 wafers during the process cycle. Once the wafers are loaded, the vacuum loadlock pump removes oxygen and moisture by pumping down the loadlock and backfilling with N_2. After 3 purge cycles, the wafers are kept under ultra-pure and therefore inert nitrogen ambient at atmospheric pressure. This avoids re-oxidation of wafers before epitaxy. Selected wafers **(6)** can be transferred one after the other into the single wafer epitaxy chamber using a Bernoulli wand **(7)**, which relies on the Bernoulli air flow principle. A high velocity air stream has a low static pressure. The wand is designed with a number of gas outlet holes on its lower surface. Under

high pressure gas jet, a high velocity flow pattern is created near the lower surface and thus reduces its local pressure. When it approaches the wafer, the difference between local and atmospheric pressure generates a lift force, pushing the wafer towards the wand. Simultaneously, the flow pattern creates a force on the outward direction, combined with the wafer's own weight to balance the lift force. The wafer is thus suspended without contact, avoiding damage and contamination.

The epitaxy process takes place inside the epitaxy chamber **(8)** with post process gases evacuated in the exhaust **(9)**. After growth, the wafer is unloaded into the transfer chamber, moving into the loadlock, and finally back to the FOUP.

The epitaxial recipes and selected process can be chosen and modified via the control interface **(10)**: It allows users to write/modify recipes, control on-going process, detect errors etc.

Before describing more precisely the epitaxy chamber, we will note the presence of peripherals which are necessary for the proper tool functioning, such as:

- Various pumps in the basement (for the epitaxy chamber, the transfer chamber and the load-locks)
- A burning/scrubbing system for the gases used for growth, etching or cleaning steps. Such system is located in the basement downstream of the pumps
- Gas cabinets containing the various gas bottles
- A pressure-lowering cabinet for the various gases used
- The electrical power / electronics cabinet

Epitaxy chamber

The epitaxy chamber used for chemical vapor deposition can operate at a broad range of pressures ranging from Atmospheric (760 Torr) to Reduced Pressures (as low as 5 Torr, typically). Such chambers are commonly referred as RP-CVD (Reduced Pressure - Chemical Vapor Deposition). Its functional temperature spans the 400°C - 1100°C range, allowing low and high temperature epitaxy. A schematic view of the process module and the chamber components are shown in **Figure II.7(a)** and **Figure II.7(b)**, respectively. Thanks to its stability at high temperatures, transparency and low thermal conductivity, quartz is the material of choice for the chamber walls. Chamber cooling occurs via the circulation of water and air around the quartz walls.

A number of gas sources used in the ASM Epsilon 3200 are listed below:

- Carrier gases: N_2, H_2
- Gas sources for $Si_{1-x}Ge_x$ epitaxy: SiH_4 (Silane), SiH_2Cl_2 (Dichlorosilane –DCS), Si_2H_6 (Disilane) and GeH_4 (Germane):

- Doping gas sources: PH_3 (Phosphine) for n-type doping / B_2H_6 (Diborane) for p-type doping
- Etching gas: HCl is used to clean the chamber walls between each growth. It is also used to enhance the selectivity when performing selective epitaxial growth and to modify the Ge content in $Si_{1-x}Ge_x$ films.

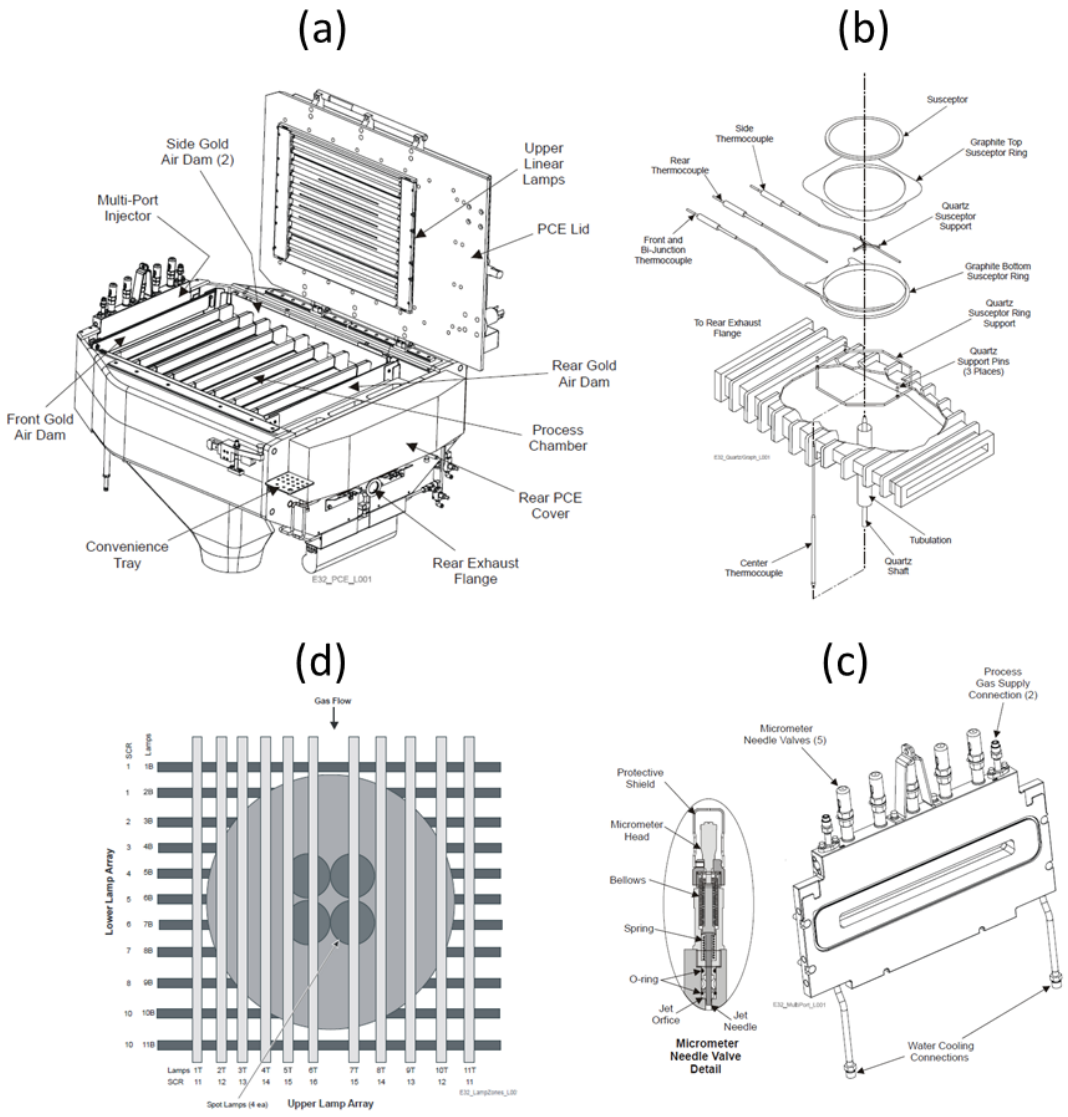

Figure II.7 (a) Process module components and assemblies (b) Process chamber components (c) Multi-port injector flange and (d) Lamp array assembly [Epsilon® 3200 System Operator Manual]

The gas distribution system is designed with ultrapurity standards and allows precise gas injection onto the wafer with short switching transients. A multi-port injector flange (**Figure II.7(c)**) is located at the front of the reactor section and serves as the point of entry for process and purge gases. The reactive gas is mixed with carrier gas before being injected in the epitaxy chamber in a laminar fashion. Five micrometer needle valves flow adjusters are used to tune the laminar flow. Gas molecules diffuse towards the wafer under a gradient of concentration

between the flow and the substrate, then decompose thermally on the wafer surface as described above. During growth, the wafer is placed on a SiC coated graphite susceptor that rotates (typically at 35 rpm) to improve film spatial thickness uniformity. Wafers are radiantly heated from both sides by external tungsten halogen lamps. Top and bottom heating minimizes any differences between the wafer and the susceptor, improving temperature uniformity and control. Similarly, radiative heating can be adjusted along the wafer radius to tune the radial uniformity. 22 lamps and 4 spots (**Figure II.7(d)**) are used to heat the wafer uniformly, 11 lamps at the top and 11 lamps + 4 spots at the bottom of the chamber. The temperature is controlled with 4 thermocouples (embedded in graphite pre-heating components or close to the center of the susceptor) located at the center, side, front (upstream), and rear (downstream) of the susceptor.

II.3. Characterization techniques

The morphological and structural properties of SiGe based heterostructures grown using RP-CVD can be studied using various characterization techniques. Here are listed some of the data that should be acquired:

- Surface condition, shape
- Layer thickness
- Film composition
- Strain and relaxation degree
- Crystal defectivity

Another distinction can also be made between in-line characterizations (which are integrated in a mainstream production line and which are non-destructive) and off-line characterizations (contaminant and/or destructive).

II.3.a. Morphological analysis

II.3.a.i. Atomic force microscopy

Atomic force microscopy (AFM) operates by measuring the Van Der Waals and electrostatic forces between a probe and the sample. These forces depends on the nature of the surface topology and of the type of material present on the surface. The AFM principle is illustrated in **Figure II.8**. The instrument consists of a cantilever with a sharp tip mounted at its end. The cantilever is usually made of silicon, silicon oxide or silicon nitride. The cantilever is connected to a piezoelectric crystal which induces tip oscillations. For topographic imaging,

the tip is brought into continuous or intermittent contact with the sample and scanned across the sample surface. Piezoelectric scanners translate the sample under the tip. The variations of the tip position are measured by the reflection of a laser spot on the backside of the tip. This reflection is detected by a four-segment position sensitive photodiode and converted into current signal variations.

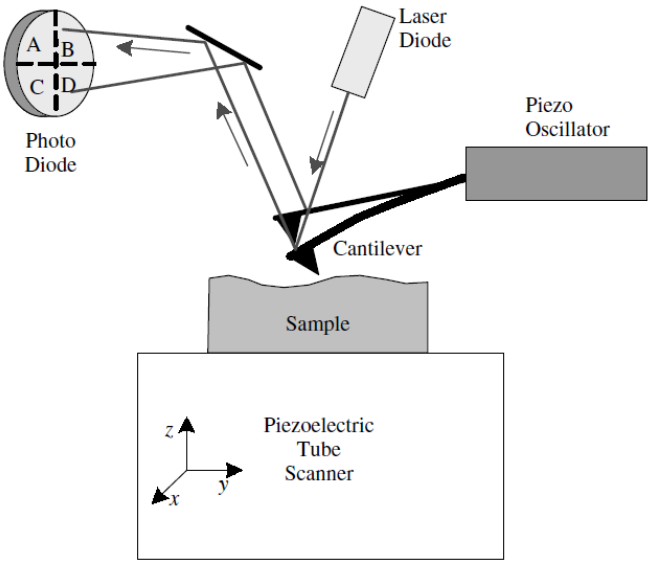

Figure II.8 Schematic illustration of an atomic force microscope (Schroder 2005)

AFMs can operate in several modes. Tapping mode imaging overcomes the limitations of the conventional scanning modes by alternately placing the tip in contact with the surface to provide high resolution and then lifting the tip off the surface to avoid dragging the tip across the surface. It is implemented in the air by oscillating the cantilever near but not at the cantilever's resonant frequency. The piezo motion causes the cantilever to oscillate when the tip does not contact the surface. The oscillating tip is then moved toward the surface until it begins to lightly touch, or "tap" the surface. During scanning, the vertically oscillating tip alternately contacts the surface and lifts off, generally at a frequency of 50 to 500 kHz. As the oscillating cantilever contacts the surface intermittently, energy loss caused by the tip contacting the surface reduces the oscillation amplitude that is then used to identify and measure surface features. When the tip passes over a bump in the surface, the cantilever has less room to oscillate and the amplitude of oscillation decreases. Conversely, when the tip passes over a depression, the cantilever has more room to oscillate and the amplitude increases approaching the maximum free air amplitude. The oscillation amplitude of the tip is measured and a feedback loop adjusts the tip-sample separation maintaining a constant amplitude and force on the sample. The adjustment of the tip-sample separation, either by moving the sample or the oscillating head, is then the data which is translated as "height" or Z-topology in AFM images.

AFM image quality is a strong function of the curved shape of the tip used, with a radius of curvature typically 5-10 nanometers. Tapping mode atomic force microscopy measurements

were carried out in a Fast-scan Bruker tool. X-Y scan size range is from 1 x 1 µm² to 20 x 20 µm². Z topology can be measured from 0.5 nm up to 2 µm.

Root Mean Square roughness (rms) and Z-Range (ZR) values are usually deduced from AFM measurements. They are defined as follows:

$$rms = \sqrt{\frac{\sum_{i=1}^{n}(Z_i - \bar{Z})}{N}} \quad \textbf{Eq II.5}$$

Where rms is the Root Mean Square roughness, N is the number of image points, Z_i is the height for the ith point and $\bar{Z}$ is the average height for all image points.

$$ZR = Z_{max} - Z_{min} \quad \textbf{Eq II.6}$$

Where Z_{max} is the maximal height for all image points and Z_{min} the lowest.

II.3.a.ii. Scanning spreading resistance microscopy

Scanning Spreading Resistance Microscopy (SSRM), based on atomic force microscopy, uses a small conductive tip to measure the local spreading resistance (see **Figure II.9**). The resistance is measured between a sharp conductive tip and a large back surface contact. A precisely controlled force is used while the tip is scanned over the sample. The SSRM equipment is based on a standard commercially available AFM equipment. A conductive cantilever with a highly-doped ion-implanted diamond tip is used as a resistance probe. Diamond protects the tip from deformation due to the rather high loads (~50–100 µN) required to penetrate the layer and make a good electrical contact. Coating the tip with a thin tungsten layer improves the conductivity.

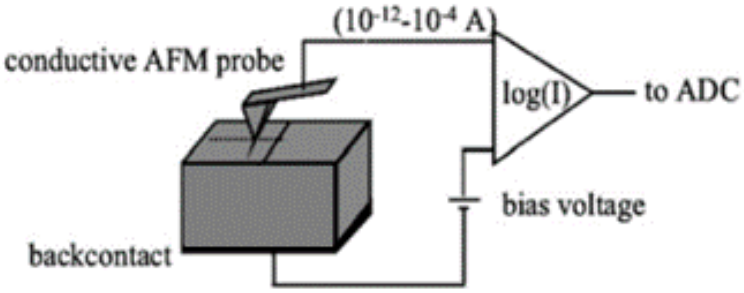

Figure II.9 Principle of an SSRM measurement. A voltage is applied between a conductive AFM tip and a back contact. The measured current gives the spreading resistance (Kalinin and Gruverman 2007)

Contact mode SSRM measurements were conducted on a Bruker Dimension Icon SSRM-HR platform using a diamond probe form IMEC CAMS. Sample bias was fixed at -1 V and the electrical contact was obtained using a silver lacquer.

II.3.a.iii. Scanning electron microscopy

The image in a Scanning Electron Microscope (SEM) is produced by scanning, under high vacuum, the sample with a focused electron beam and detecting the secondary and/or backscattered electrons. As shown in **Figure II.** 10, a scanning electron microscope consists of an electron gun, a lens system, scanning coils, an electron collector, and a cathode ray display tube (CRT). The electron energy is typically 10–30 keV for most samples, but for insulating samples the energy can be as low as several hundred eV. The use of electrons has two main advantages over optical microscopes: much larger magnifications are possible since electron wavelengths are much smaller than photon wavelengths and the field depth is much higher.

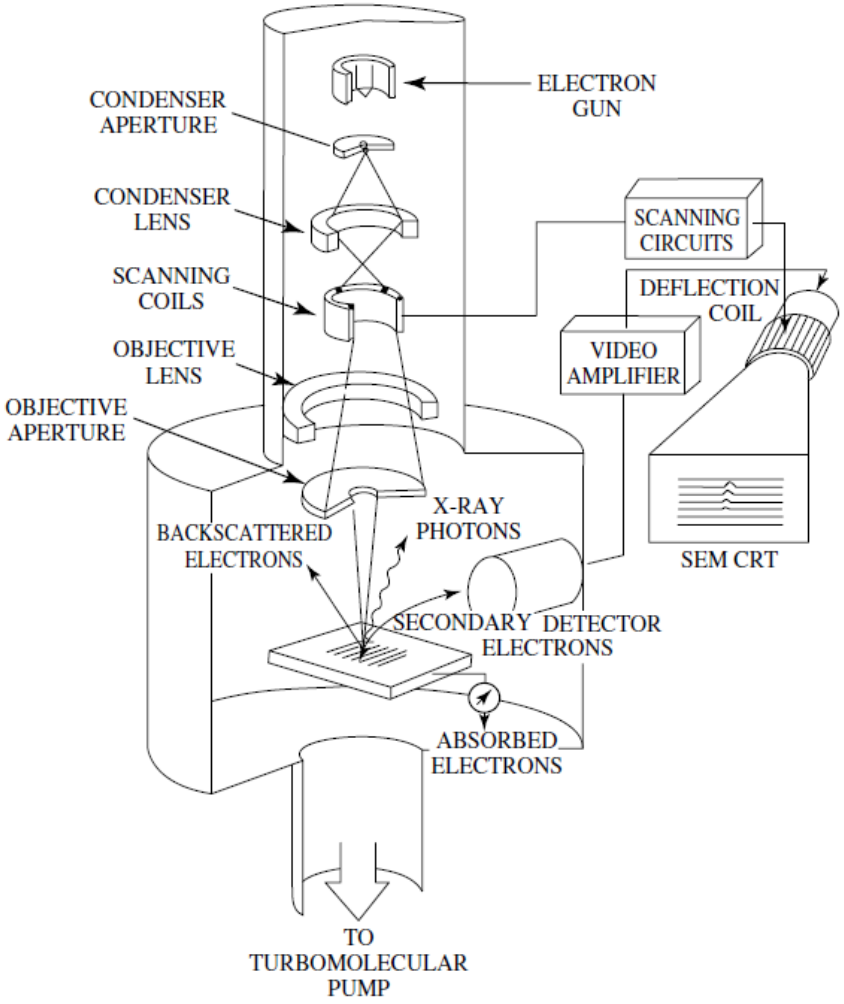

Figure II. 10 Schematic of a scanning electron microscope (Schroder 2005)

During this PhD, a CG4000 CD-SEM from Hitachi was used for plan-view imaging. For cross sectional imaging, a Hitachi 5500 and a Merlin ZEISS microscope were used.

II.3.b. Structural analysis

II.3.b.i. High resolution X-ray diffraction

High-resolution X-ray diffraction (HRXRD) is important for the structural characterization of heteroepitaxial layers, yielding lattice constants, strains, crystallographic orientation and defect densities.

Diffraction from a three-dimensional crystal is the constructive interference of waves scattered by the atoms in the lattice. A necessary condition for diffraction is that the path length difference for beams scattered by different atoms is an integral multiple of the x-ray wavelength. This condition is given by the Bragg equation for diffraction which may be understood with the aid of **Figure II.11**.

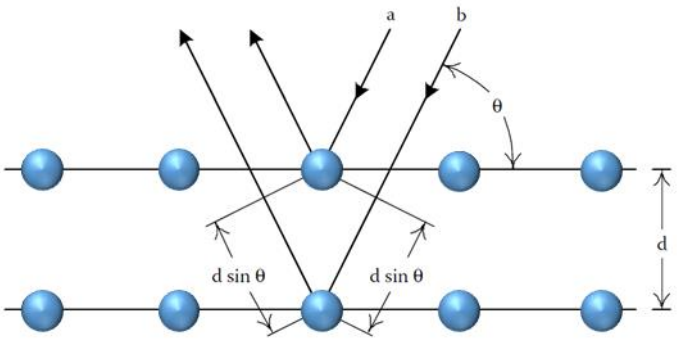

Figure II.11 Schematic illustration of the Bragg condition for diffraction

An x-ray beam is incident on a set of crystal planes with a d separation d. If the angles of incidence and reflection are equal to θ, the path difference Δ between beams a and b is 2dsin θ. The condition for constructive interference is Δ = nλ, where n is an integer and λ is the x-ray wavelength. Thus, the condition for diffraction is the Bragg equation

$$2d\ sin\ \theta = n\lambda \qquad \textbf{Eq II.7}$$

Where n is the order of the reflection and θ is the Bragg angle.

For a diamond crystal with lattice constant a, the spacing of the (hkl) planes is

$$d(hkl) = \frac{a}{\sqrt{h^2+k^2+l^2}} \qquad \textbf{Eq II.8}$$

The hkl Bragg angle is then

$$\theta(hkl) = sin^{-1}\left(\frac{\lambda}{2a\sqrt{h^2+k^2+l^2}}\right) \qquad \textbf{Eq II.9}$$

Thus, measurements of the Bragg angle gives access to the inter-atomic spacing for a given (hkl) plane.

A delta peak will be associated with a perfect and infinite crystal, with a perfectly monochromatic and parallel X-Ray beam which is not attenuated within the material. For thin epitaxial layers, such a model cannot be used. Finite layer thickness will indeed induce some broadening of the X-Ray diffraction peaks (Herman and Sitter 1996) according to the Sherrer's formulation:

$$\beta_{1/2} = \frac{0.9\lambda}{2t\ cos\theta} \qquad \textbf{Eq II.10}$$

Where $\beta_{1/2}$ is the full width at half maximum (FWHM) of the X-Ray peak, λ is the X-ray wavelength, t is the layer thickness and θ is the Bragg angle.

For real crystals, the volume diffracting coherently decreases due to the finite crystal thickness and to the X-Ray beam attenuation within the layer. Experimentally, a broadening of diffraction points occurs in the reciprocal space. The attenuation of the X-Ray beam (1), the distribution of the diffracted intensity in reciprocal space (2) and the associated X-Ray diffraction profiles (3) are shown in **Figure II.12** for ideal infinite (a), semi-infinite (b), and finite (c) crystals:

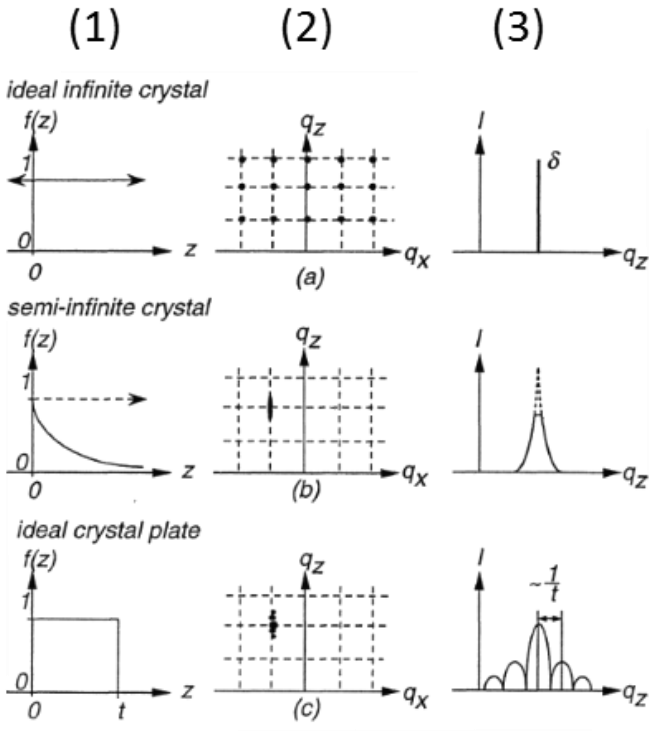

Figure II.12 Attenuations of the X-Ray beams (1), distributions of the diffracted intensities in reciprocal space (2) and associated X-Ray diffraction profiles (3) for ideal infinite (a), semi-infinite (b), and finite crystals (c) (Herman and Sitter 1996)

For an ideal infinite crystal (a), the diffracted intensity is only localized on reciprocal space nodes. The associated Bragg peaks are narrow localized functions. For a semi-finite crystal (b),

the X-Ray beam attenuation leads to a broadening of the diffracted intensity around reciprocal space nodes. An increase of the Full Width at Half Maximum (FWHM) of the associated X-Ray peak is also shown.

Finally, for a finite layer (c), under the assumption that the X-Ray attenuation is weak in thin semiconductors materials, additional diffraction points are observed near the reciprocal space nodes. Thickness fringes are usually commonly seen near Bragg's peaks in X-Ray Diffraction profiles, and the layer thickness can be deduced from the angular spacing of fringes and the width of the layer XRD peak, using the appropriate formalism. Standard tool configuration used for SiGe HRXRD measurements during the thesis will now be described.

Description of the Panalytical High-Resolution X-ray diffractometer

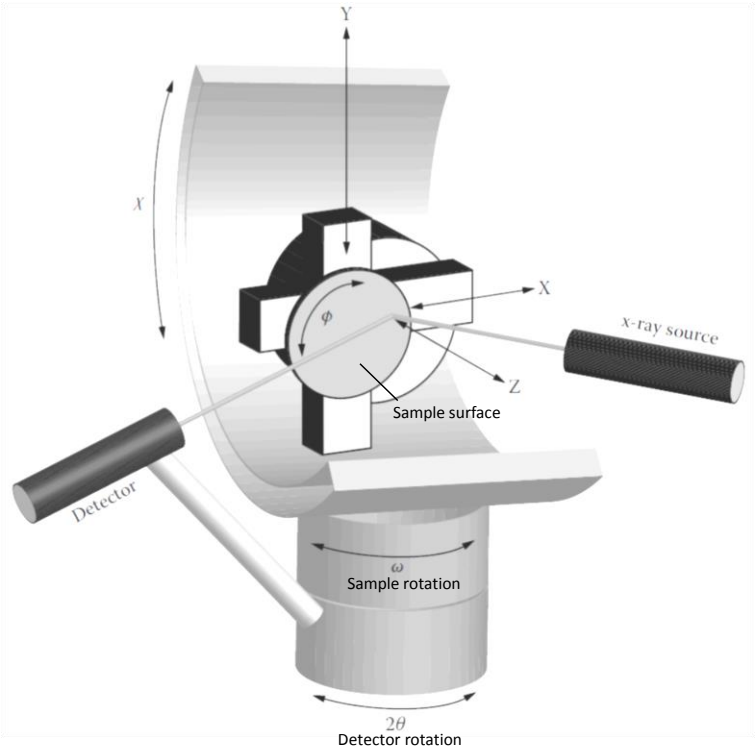

Figure II.13 Description of an X-Ray Diffraction tool. Displacements and rotation angles in various space directions are indicated.(Bowen and Tanner 2006)

X-ray measurements require an x-ray source, a beam conditioner to control wavelength and the divergence of the input beam and a goniometer to manipulate the sample. A detector is placed to measure the scattered intensity, with often a detector collimator to limit the divergence of the output beam that is measured. Such a standard set-up is illustrated with the associated displacements and rotation angles in *Figure II.13*.

HRXRD data usually measures scattered X-ray intensity as a function of omega and/or 2theta angles (see **Figure II.14**). The incident angle omega is defined between the X-ray source and the sample. The diffracted angle 2theta is defined between the incident beam and detector angle.

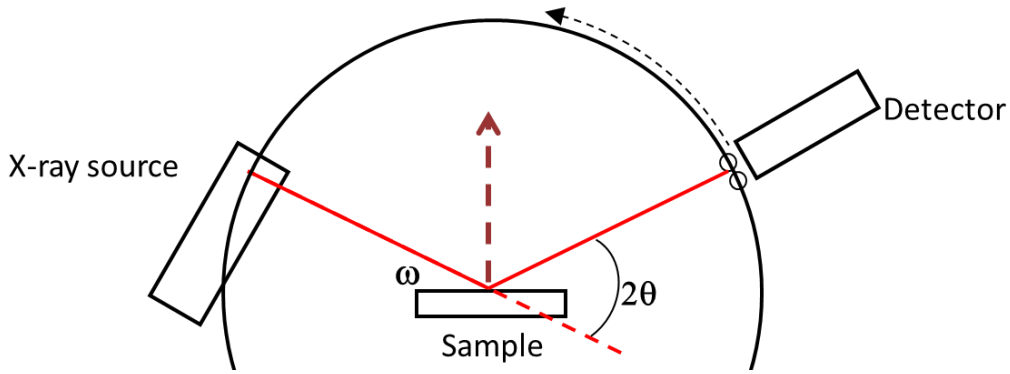

Figure II.14 Schematic illustration of a HRXRD scan

Different types of scans can be performed with a HRXRD setup:

- A rocking curve or omega scan is a plot of X-ray intensity vs. omega without changing 2theta.
- A detector scan or 2theta scan plots X-ray intensity vs. 2theta without changing omega.
- A coupled scan or omega/2theta scan is a plot of scattered X-ray intensity vs 2theta, but omega also changes in a way that is linked to 2theta so that $\omega = \frac{1}{2} * 2\theta + offset$. The scan is called symmetric when the offset = 0 (the reflecting lattice planes are parallel to the surface) and asymmetric when offset ≠ 0.
  → The coupled scan is used to measure the Bragg diffraction angle.

Under Bragg law conditions, variations of the X-Ray wavelength and of the Bragg incident angle determine the ability of X-Ray diffraction to measure very small inter-atomic distances. The relationship between these parameters is usually given by the differential Bragg's law:

$$\frac{\Delta d}{d} = \frac{\Delta \lambda}{\lambda} - \frac{\Delta \theta}{tan\theta} \qquad \textbf{Eq II.11}$$

The X Pert Pro Panalytical High-Resolution X-Ray Diffractometer (tool used during this PhD) uses a 4-crystal Ge (220) Bartels monochromator. This 5-crystal or double axis configuration is illustrated in **Figure II.15**.

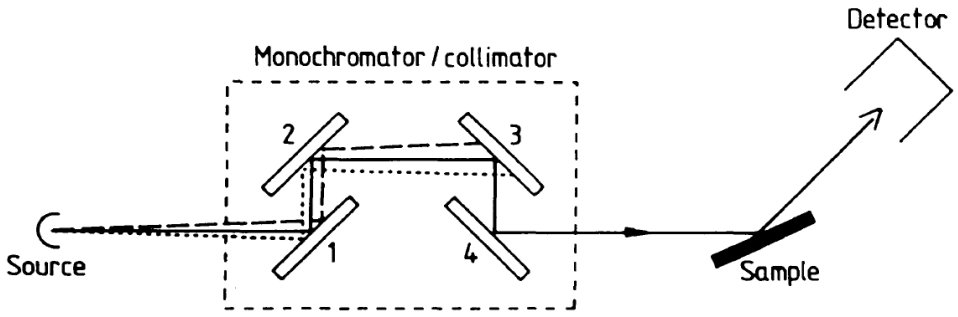

Figure II.15 Description of the 5-crystal configuration). A slit collimator is usually placed in front of the detector. 1 and 2 (3 and 4) crystals are coming from the same Ge monocrystal.(Bauer and Richter 1996)

In such a configuration, the angular and wavelength dispersion of the X-Ray beam coming from the source is filtered by the four reflections in the Bartels monochromator. A monochromatic and parallel beam is obtained at its exit, with roughly 25% of the intensity of the CuKα_1 peak at 1.5406 Å being selected.

A double-axis system uses an open detector and therefore integrates the scattering from the specimen over all angles within its aperture. While this is quick and convenient, details such as interference fringes or narrow peaks can be lost or blurred. This ambiguity can be removed by using the 7-crystal or triple-axis configuration shown in **Figure II.16**.

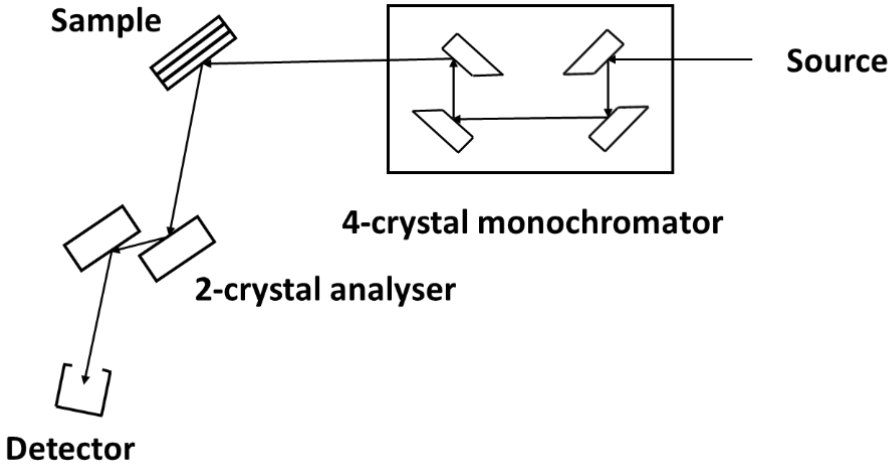

Figure II.16 Description of the 7-crystal configuration (Bauer and Richter 1996)

The use of a 2 bounces analyzer in front of the detector, oriented to a selected Bragg angle, provides a method for analyzing the angular dependence of the scatter from the sample with a much higher resolution. An asymmetrically cut Ge crystal set for the 220 reflection can provide an acceptance angle as low as 35 arc sec with the Cu Kα1 radiation, while an asymmetric Si crystal under similar conditions will typically yield 15 arc sec.

Experimental measurement procedures

➔ Omega/2theta scans around the (004) and (224) diffraction orders:

The lattice mismatch between a SiGe layer and a Si substrate will lead to variations of the in-plane $a_{SiGe}^{//}$ and perpendicular $a_{SiGe}^{\perp}$ lattice parameters of the layer as a function of strain. Determination of such parameters by HRXRD gives access to the Ge composition and degree of strain relaxation of the studied SiGe layers.

The inter-atomic distance d_{hkl} in cubic crystals is linked to the (hkl) Miller indexes and to the in-plane and perpendicular lattice parameters $a_{SiGe}^{//}$ and $a_{SiGe}^{\perp}$ through:

$$\frac{1}{d_{hkl}} = \frac{(h^2+k^2)}{{a_{SiGe}^{//}}^2} + \frac{l^2}{{a_{SiGe}^{\perp}}^2} \quad \textbf{Eq II.12}$$

Using the Bragg law (**Eq II.7**) with the previous equation, we obtain:

$$\frac{4sin^2(\theta_{hkl})}{\lambda^2} = \frac{(h^2+k^2)}{{a_{SiGe}^{//}}^2} + \frac{l^2}{{a_{SiGe}^{\perp}}^2} \quad \textbf{Eq II.13}$$

In addition, the angle φ_{hkl} between the [001] growth direction and the (hkl) diffracting planes is defined as follows in a tetragonal distorted crystal:

$$\frac{1}{cos^2\varphi_{hkl}} = \frac{{a_{SiGe}^{\perp}}^2}{l^2}\left(\frac{h^2+k^2}{{a_{SiGe}^{//}}^2} + \frac{l^2}{{a_{SiGe}^{\perp}}^2}\right) \quad \textbf{Eq II.14}$$

Combining **Eq II.13** and **Eq II.14** we can compute $a_{SiGe}^{\perp}$ and $a_{SiGe}^{//}$ of the SiGe layer:

$$a_{SiGe}^{\perp} = \frac{\lambda l}{2\sin(\theta_{hkl})\cos(\varphi_{hkl})} \quad \textbf{Eq II.15}$$

$$a_{SiGe}^{//} = \frac{\lambda}{2\sin(\theta_{hkl})\cos(\varphi_{hkl})}\sqrt{h^2+k^2} \quad \textbf{Eq II.16}$$

Combining **Eq II.15** and **Eq II.16**, we obtain the following expression for $a_{SiGe}^{//}$:

$$a_{SiGe}^{//} = \frac{\lambda\sqrt{h^2+k^2}}{\sqrt{{a_{SiGe}^{\perp}}^2\sin^2(\theta_{hkl}) - l^2\lambda^2}}\, a_{SiGe}^{\perp} \quad \textbf{Eq II.17}$$

Thus, we can determine $a_{SiGe}^{//}$ as function of $a_{SiGe}^{\perp}$. For a (224) diffraction order, the previous expression becomes:

$$a_{SiGe}^{//} = \frac{\lambda\sqrt{2}}{\sqrt{{a_{SiGe}^{\perp}}^2\sin^2(\theta_{224}^{Si}+\Delta\omega_{224}) - 4\lambda^2}}\, a_{SiGe}^{\perp} \quad \textbf{Eq II.18}$$

With θ_{224}^{Si} the Si (224) Bragg angle and $\Delta\omega_{224}$ the angular difference between the Si and SiGe peaks.

In practice, $a_{SiGe}^{\perp}$ is first determined with an omega/2theta scan around the (004) diffraction order. Then, an omega/2theta scan around the (224) diffraction order is performed giving access to $a_{SiGe}^{//}$.

Once $a_{SiGe}^{\perp}$ and $a_{SiGe}^{//}$ have been determined, the bulk SiGe lattice parameter a_{SiGe} can be deduced from the following equation:

$$a_{SiGe} = \frac{1-\nu}{1+\nu}a_{SiGe}^{\perp} + \frac{2\nu}{1+\nu}a_{SiGe}^{//} \quad \textbf{Eq II.19}$$

The poisson ratio ν of the SiGe layer is given by a linear interpolation between the Si and Ge poisson ratios, $\nu_{Si} = 0.278$ and $\nu_{Ge} = 0.271$, respectively. The Ge content can then be determined using the deviation from Vegard's law.

Finally, the degree of strain relaxation is given by:

$$R = \frac{a^{//}_{SiGe} - a_{Si}}{a_{SiGe} - a_{Si}} \qquad \textbf{Eq II.20}$$

➔ Omega scans around the (004) diffraction orders:

The broadening of the SiGe peak around the (004) diffraction order can be measured with an Omega scan. The width of the SiGe layer peak around the (004) diffraction order can be linked to a density of defects. Assuming that the defects in the layer are only threading dislocations, we can use the Ayers formula (Ayers 1994):

$$D = \frac{\beta^2}{4.68 b^2} \qquad \textbf{Eq II.21}$$

to estimate D, the Threading Dislocations Density (TDD) from β, the Full width at half maximum (FWHM) of the peak, b being the modulus of the Burgers vector surrounding individual dislocations.

➔ Reciprocal space mapping:

Reciprocal Space Mapping (RSM) is a powerful tool used in the triple-axis mode to map the scattering from Si/SiGe heterostructures. In the reciprocal space, real space planes are represented by reciprocal lattice points. The different areas probed in the reciprocal space using different scan modes are shown in **Figure II.17** for a [001] oriented lattice.

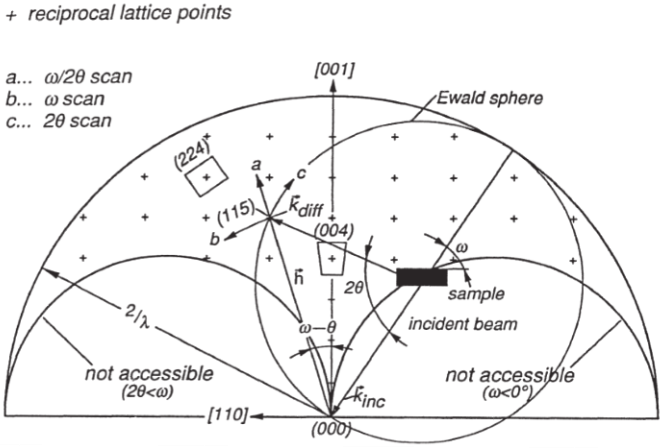

Figure II.17 Representation of the measurements modes "a": omega/2theta scan, "b": omega scan and "c": 2theta scan in the reciprocal space for a fully relaxed (001) cubic crystal. Limits for the accessibility are the maximum diffractometer angle and the Laue zones (ω < 0 and 2ϑ < ω) (Herman and Sitter 1996)

An RSM can be constructed by recording a number of omega/2theta (or 2theta) scans for different omega positions of the sample. These two-dimensional measurements contain additional information on the semiconductor structures compared with what is accessible by

one-dimensional scan curves: in particular strain or mismatch may be distinguished from tilt or mosaic spread. From the geometry of the reciprocal lattice and the Ewald construction, the conversion of a peak intensity position (ω,2θ) in reciprocal space coordinates is given by (Bauer and Richter 1996) (Sluis 1993) :

$$q^{//} = \frac{2}{\lambda}\sin(\theta)\sin(\omega - \theta) \quad \textbf{Eq II.22}$$

$$q^{\perp} = \frac{2}{\lambda}\sin(\theta)\cos(\omega - \theta) \quad \textbf{Eq II.23}$$

Where $q^{//}$ and $q^{\perp}$ (also referred as q_x and q_z) are respectively the in-plane and perpendicular reciprocal space coordinates.

If a (224) RSM is measured on a (001) Si substrate with a SiGe layer, the lattice parameters of the layer are then calculated from

$$q^{//} = \frac{2\sqrt{2}}{a^{//}_{SiGe}} \quad \textbf{Eq II.24}$$

$$q^{\perp} = \frac{4}{a^{\perp}_{SiGe}} \quad \textbf{Eq II.25}$$

(004) and (224) RSM have been used during the PhD for the structural analysis of SiGe layers using a fully automated D8 Fabline X-Ray diffractometer from Bruker. The SiGe nano-pillars were also characterized using RSM measurements around the (224) order performed on a Panalytical X'Pert diffractometer. RSM measurements around the in-plane (220) order were conducted on a Rigaku Smartlab diffractometer.

II.3.b.ii. Transmission electron microscopy

A schematic of a transmission electron microscope is shown in **Figure II.18**. Electrons from an electron gun are accelerated to high voltages (typically 100 to 400 kV) and focused on the sample by the condenser lenses. The sample is placed on a small copper grid a few mm in diameter. The static beam has a diameter of a few microns. The sample must be sufficiently thin (a few tens to a few hundred nm) to be transparent to electrons. The transmitted and forward scattered electrons form a diffraction pattern in the back focal plane and a magnified image in the image plane. With additional lenses, either the image or the diffraction pattern is projected onto a fluorescent screen for viewing or electronic or photographic recording. The ability to form a diffraction pattern yields structural information.

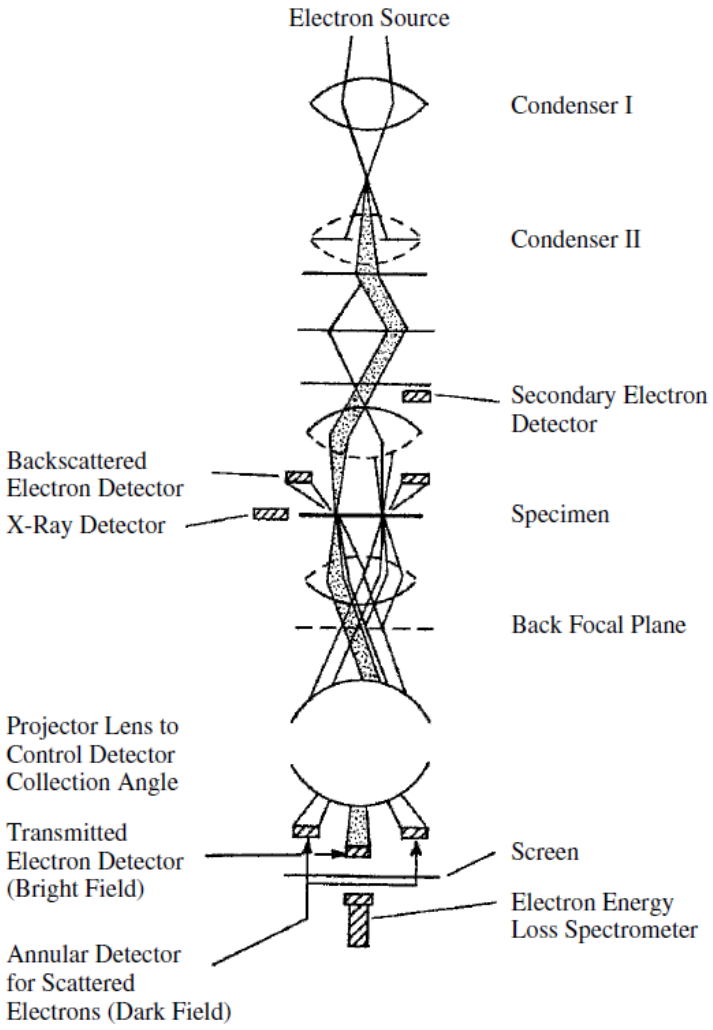

Figure II.18 Schematic of a transmission electron microscope (Schroder 2005)

The three primary imaging modes are bright-field, dark-field, and high-resolution microscopy. Image contrast does not depend very much on absorption, as it does in optical transmission microscopy, but rather on scattering and diffraction of electrons in the sample. Images formed with only the transmitted electrons are bright-field images and those formed with a specific diffracted beam are dark-field images. Few electrons are absorbed in the sample. Absorbed electrons lead to sample heating.

High resolution TEM (HRTEM) gives structural information on the atomic size level, known as lattice imaging, and has become very important for interface analysis. In lattice imaging, a number of different diffracted beams are combined to give an interference image. Crystalline defects (dislocations, stacking faults, twins etc.) can be seen and the thickness of individual layers precisely determined.

Cross-sectional TEM imaging was carried out in a JEOL 3010 microscope.

II.4. Conclusion

In this second chapter, a nano-template process flow specifically designed for the study of SiGe nano-heteroepitaxy have first of all been described. Diblock copolymer lithography, an important technological step in our integration flow, was presented. We also introduced the surface preparation schemes typically used prior to SiGe epitaxy. Surface oxide was removed thanks to ex-situ “HF-Last” wet cleanings or in-situ remote plasma Siconi processes, followed by an in-situ H_2 bake (to remove the remaining O atoms on the surface). A specific emphasis was made on the selective epitaxial growth of SiGe by chemical vapor deposition, which is the main subject of this PhD thesis. Si surface condition before epitaxy, CVD mechanisms and RPCVD tool operations were explained.

The main morphological and structural characterization methods were described afterwards, with a special focus on AFM and HRXRD techniques which have extensively used for the analysis of SiGe based nanostructures and layers. Techniques such as SSRM and HRTEM were otherwise very handy for defectivity investigation. The operating principles and different formalisms used during the PhD were detailed.

Defining a proper integration scheme for the nano-template fabrication and finding the right characterization methods allowed us to investigate SiGe nano-heteroepitaxy in various configurations. First experimental results related to SiGe nano-heteroepitaxy on Si and SiGe nano-pillars will now be detailed in chapter III.

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CHAPTER III:
SiGe nano-heteroepitaxy on Si and SiGe nano-pillars

Contents of chapter III

III.1. Introduction

The main objective of this first experimental study was to achieve a smooth and fully strain relaxed $Si_{0.75}Ge_{0.25}$ layer with a thickness of only a few hundreds of nm. When grown on blanket Si wafers, a 200 nm thick $Si_{0.75}Ge_{0.25}$ layer is expected to be fully compressively strained (Hartmann et al. 2011). A promising method to have a fully relaxed $Si_{0.75}Ge_{0.25}$ layer of that thickness is heteroepitaxial growth on nano-patterned SiO_2 templates.

In the pioneering work of Lee et Al. (Lee et al. 2007), Ge epitaxial growth was carried out on a patterned substrate with nanometre-scale seed pillars. Growth fronts from individual nano-pillars coalesced to form a complete 2D layer. The major advantage with this approach is the introduction of additional freedom for strain relaxation thanks to nano-pillars. Another original work from Lee et Al (Lee et al. 2006) showed that SiGe epitaxial growth is improved with the reduction of the pattern size.

In this first chapter, we propose to investigate the nano-heteroepitaxy approach using an industrial tool as well as a new integration scheme, pattern size and materials compared to prior works. We also provide an in-depth morphological and structural analysis of the SiGe nano-pillars and layers leading to a better understanding of the nano-heteroepitaxy mechanisms. An original process flow has thus been used to fabricate SiO_2 based nano-templates, and the nano-heteroepitaxy of 2D SiGe layers on these templates has then been investigated using Si and SiGe nano-pillar seeds.

III.2. Experimental details

III.2.a. Nano-template features

As described in **Figure III.1**, the substrate patterning process flow starts from slightly p-type doped nominally on-axis 300 mm bulk Si(001) wafers. A 20 nm thick thermal SiO_2 layer is then grown to serve as a template for lithography. Next, a diblock copolymer patterning is performed followed by a SiO_2 etching step giving cylindrical cavities of 20 nm diameter and 15 nm spacing in a closely packed hexagonal configuration as shown in **Figure III.2**.

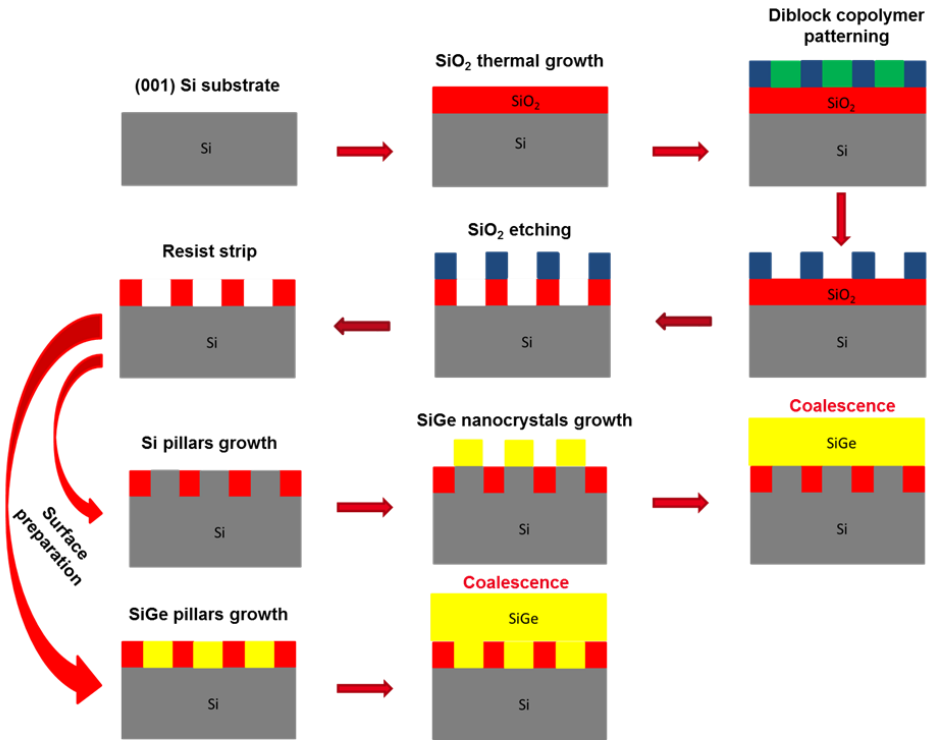


Figure III.1 SiO_2 nano-template fabrication process flow and SiGe nano-heteroepitaxy integration schemes

Surface preparation before nano-pillars growth is a critical step for this process flow since an "HF-last" wet cleaning did not allow us to grow selectively Si or SiGe nano-pillars. The solution to this problem consisted in using a dry Siconi process which uses a NH_3/NF_3 remote plasma to convert native oxides into salts that are sublimated at low temperature (Yang et al. 2010)(Raynal et al. 2018).

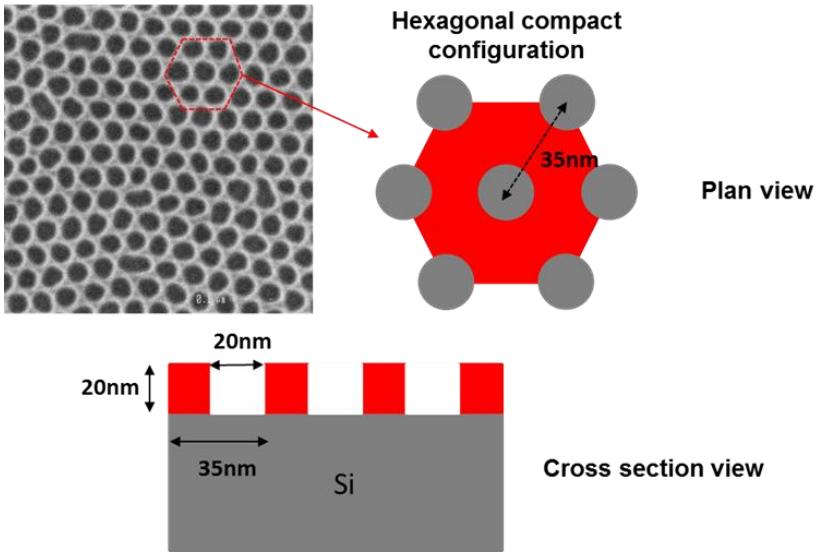


Figure III.2 Plan view SEM image of the oxide mask (top right) with a plan view schematic of the hexagonal compact configuration defined by the diblock copolymer patterning (top left) and cross sectional schematic of the oxide nano-template (bottom).

III.2.b. Growth conditions

We used two integration schemes, the first consisted in selectively growing Si nano-pillars followed by thick SiGe layers, and the second in selectively growing SiGe nano-pillars followed by thick SiGe layers with the same Ge content. The 300 mm Epsilon 3200 Reduced Pressure – Chemical Vapour Deposition tool from ASM America was used to that end, with the growth pressure kept at 20 Torr. SiH_2Cl_2 and GeH_4 were used as Si and Ge gaseous precursors, respectively. The purified H_2 carrier gas flow, several tens of litres per minute, was not altered throughout the experiments. Temperatures, mole fractions and growth rates of the various processes used for Si and SiGe growth are provided in **Table III.1**.

Si			
Growth temperature (°C)	$[SiH_2Cl_2]/[H_2]$	$[HCl]/[H_2]$	Growth rate (nm/min)
850	0.003	0.0015	60
SiGe			
Growth temperature (°C)	$[SiH_2Cl_2]/[H_2]$	$[GeH_4]/[H_2]$	Growth rate (nm/min)
650	0.003	0.00015	6
700	0.003	0.00023	20
750	0.003	0.0003	95
800	0.003	0.0003	120

Table III.1 Temperatures, mole fractions and growth rates of the processes used for Si and SiGe growth.

III.2.c. Sample characterization

The thick SiGe layers were characterised by X-Ray Diffraction (XRD). Ge concentrations and macroscopic degrees of strain relaxation were extracted from Reciprocal Space Mappings (RSM) around the (004) and (224) orders using an automated D8-Fabline X-ray Diffractometer from Bruker. The SiGe nano-pillars were characterised by XRD using RSM measurements around the (224) order performed on a Panalytical X'Pert diffractometer. RSM measurements around the in-plane (220) order were conducted on a Rigaku Smartlab diffractometer. Tapping mode Atomic Force Microscopy (AFM) measurements were carried out on a Fast-Scan Bruker platform. In terms of Scanning Electron Microscopy (SEM), a CG4000 CD-SEM from Hitachi has been used for plan-view imaging and a Hitachi 5500 along with Merlin ZEISS microscope have been used for cross sectional imaging. Cross-sectional Transmission Electron Microscopy (TEM) was carried out in a JEOL 3010 microscope operating at 300 keV. Nearly parallel sidewall

TEM lamella were prepared in the <110> directions using a Strata Focus Ion beam microscope from FEI and a precision ion polishing system PIPS II from Gatan.

III.3. Experimental results

III.3.a. Si nano-pillars growth

Si nano-pillars 20 nm high were grown using a selective epitaxial process based on SiH_2Cl_2, HCl and H_2 (Fitch 1994)(Regolini et al. 1989)(Hartmann et al. 2003). The growth temperature was fixed to 850°C. **Figure III.3** shows a 2x2 µm^2 AFM image of the Si nano-pillars. The moderate height distribution might be due to an inhomogeneous exposition of the nano-cavities to gas flow during growth or to slight differences in the size of the nano-cavities. Randomly oriented domains in the nano-pillar pattern (delimited by white dotted lines) are also noticed. They are due to the lithography process used, which was not Direct Self-Assembly (DSA). The structural properties of the nano-pillars are important for nano-heteroepitaxy as they are the starting point from which the crystal is originating. Defects in these structures may have an impact on the final layer.

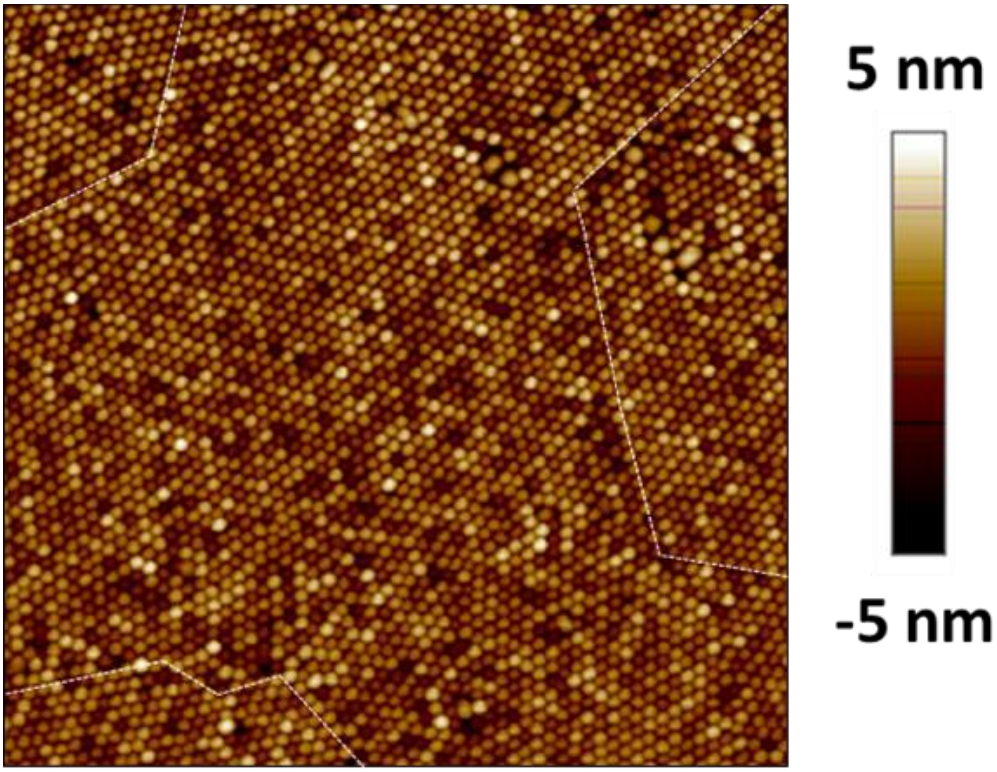


Figure III.3 2x2 µm^2 AFM image of 20 nm high Si nano-pillars grown at 850°C. White dotted lines delimit randomly oriented domains in the nano-pillar pattern. Image sides are along the <100> directions

A tilted SEM view of these pillars is shown in **Figure III.4**, where the faceting of the Si nano-pillars is clearly visible. The resolution of the image does not allow a precise indexing of the crystallographic planes, but it seems that nano-pillars have a truncated pyramidal shape with a square base, as shown schematically in the inset of **Figure III.4**. The crystallographic planes on the pyramid sidewalls seem to be {111} planes, while the planes on the top of the truncated pyramids are (001).

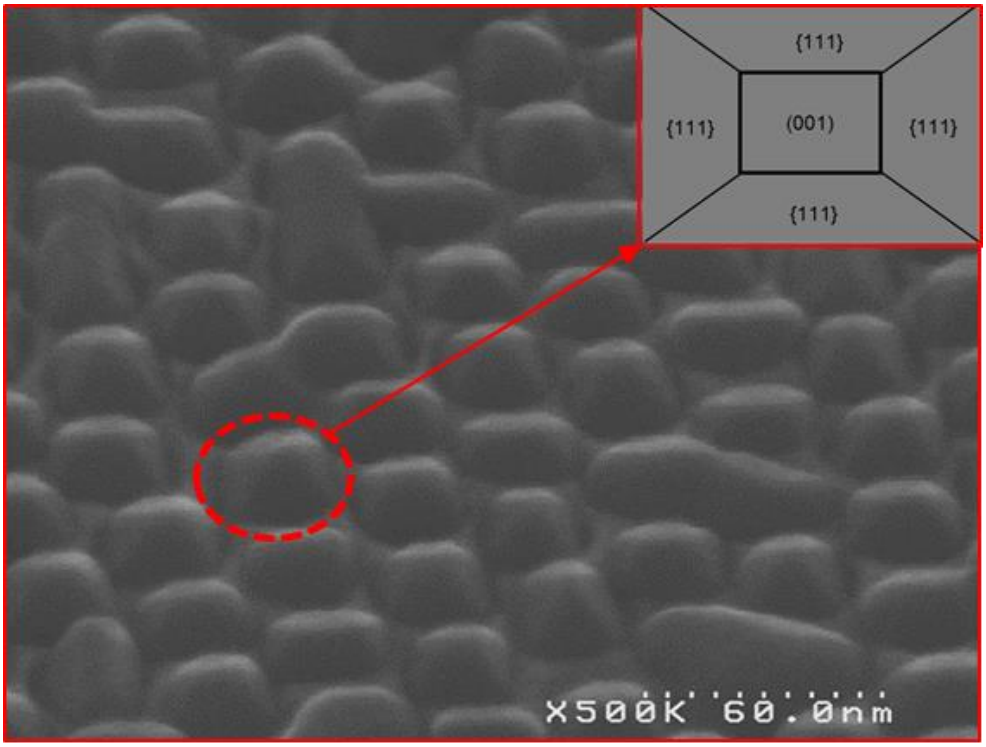


Figure III.4 Tilted SEM view of 20 nm high Si nano-pillars grown at 850°C with a schematic of suggested facets

III.3.b. SiGe nano-heteroepitaxy on Si nano-pillars

Having produced highly uniform silicon nano-pillars, we then studied the influence of the growth temperature of thick SiGe layers on these nano-pillars. 200 nm thick SiGe layers with a targeted Ge content of 25% were selectively grown at 650°C, 700°C, 750°C and 800°C with GeH_4, SiH_2Cl_2 and H_2 (Bodnar et al. 1997)(Hartmann et al. 2002)(Hartmann et al. 2012). **Figure III.5** shows 2x2 μm^2 AFM scans performed on the various samples and the corresponding surface Root Mean Square (RMS) roughness. The surface is relatively smooth at 650 and 700°C. The surface becomes increasingly rougher at 750°C and especially 800°C, and this is reflected in a higher RMS roughness for these higher temperature layers.

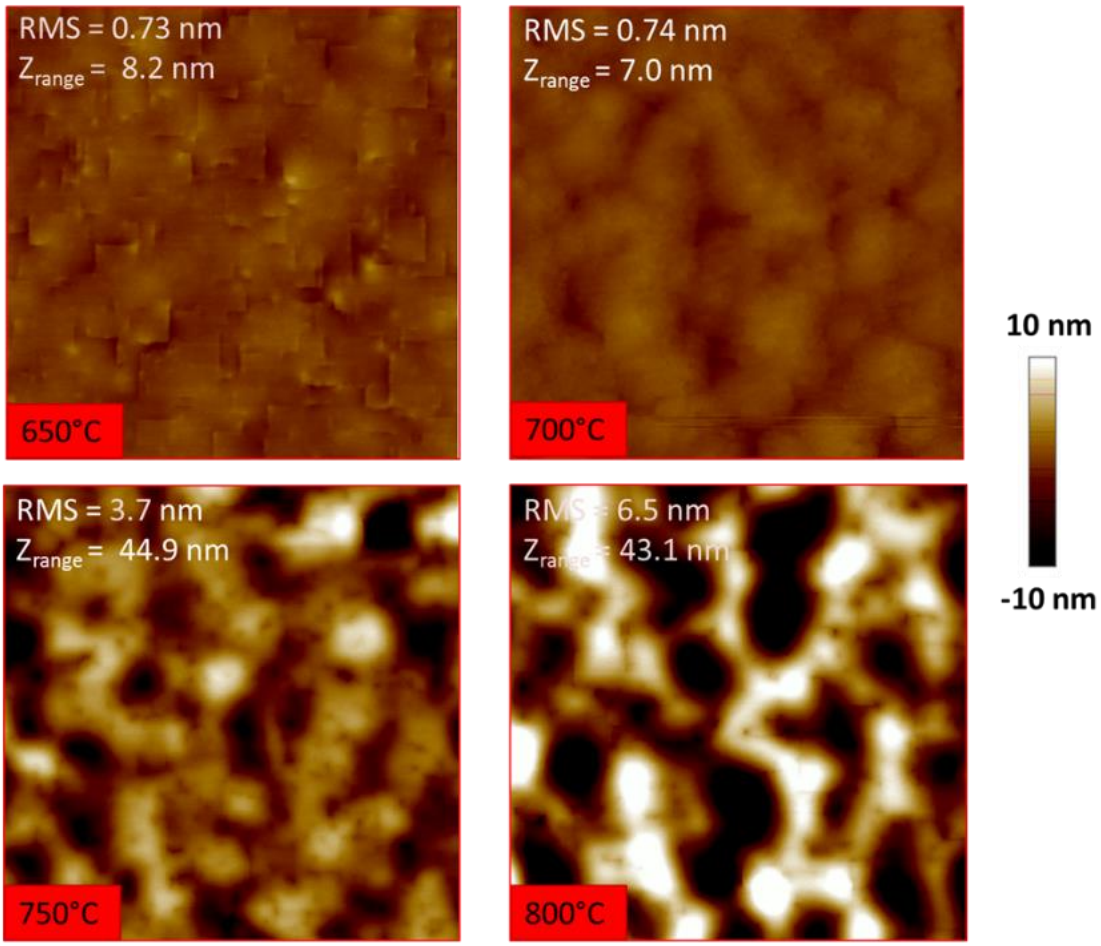


Figure III.5 2x2 µm² AFM scans of ~ 200 nm thick $Si_{0.75}Ge_{0.25}$ layers grown at different temperatures on Si nano-pillars and corresponding RMS roughness and Z range (= $Z_{max.} - Z_{min.}$) values. Image sides are along the <110> directions.

XRD reciprocal space maps of the samples grown at 650°C and 700°C are presented in **Figure III.6**. The position of the SiGe spot in the reciprocal space maps allows us to extract the Ge concentration and the macroscopic degree of strain relaxation *R* of the SiGe layer:

$$R = \frac{a_{SiGe}^{//} - a_{Si}}{a_{SiGe}^{bulk} - a_{Si}} \qquad \textbf{E.q. III.1}$$

where $a_{SiGe}^{//}$, a_{SiGe}^{bulk} and a_{Si} are the in-plane lattice parameter of SiGe, the bulk unstrained parameter of SiGe and the Si lattice parameter, respectively. We also observed a deformation of the (004) and (224) diffraction spots of the SiGe layers in a direction normal to a straight line connecting the Si spot to the origin of the reciprocal space. The dimensions of the SiGe layer spot around the (004) diffraction order can be related to a density of defects. If we assume that the defects in the layer are only threading dislocations, we could use the Ayers formula (Ayers 1994), i.e.

$$\mathrm{D} = \frac{\beta^2}{4.68 b^2} \qquad \textbf{E.q. III.2}$$

to extract D, the Threading Dislocations Density (TDD) from β, the Full width at half maximum (FWHM) of spots in that perpendicular direction, b being the modulus of the Burgers vector surrounding individual dislocations.

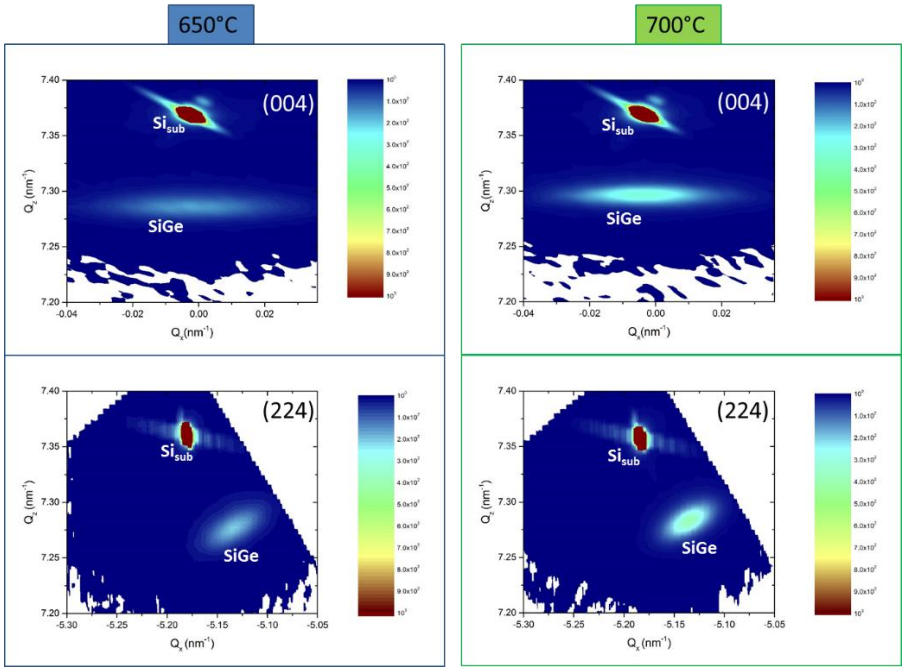


Figure III.6 (004) and (224) X-Ray Diffraction Reciprocal Space Maps of SiGe layers grown at 650°C (left) and 700°C (right) on Si nano-pillars.

However, the angular broadening could be induced by the bending of atomic planes due to strain in the nano-pillars. Thus, it was decided not to compute defect density but to consider the FWHM as a qualitative measure of the layer quality. The in-plane and out-of-plane lattice parameters, Ge content, relaxation, and peak width for the layers at 650°C and 700°C are shown data in **Table III.2**.

SiGe layer growth temperature (°C)	In-plane lattice constant (Å)	Out-of-plane lattice constant (Å)	Ge concentration (%)	Degree of relaxation (%)	FWHM (arcsec)
650	5.479	5.493	27.2	85.6	1149
700	5.481	5.486	25.8	94.8	895

Table III.2 In-plane and out-of-plane lattice parameters, Ge content, macroscopic degree of strain relaxation and FWHM of SiGe layers with Si nano-pillars grown at 650 and 700°C

The Ge content is higher than the targeted 25% for both layers (from blanket growth kinetics data), which is likely due to loading effects (Ito et al. 1995). The SiGe layers are also highly relaxed, which is likely due to nano-heteroepitaxy. By contrast, a 200 nm thick $Si_{0.75}Ge_{0.25}$ layer would be fully compressively strained when grown at 650°C on blanket Si (Hartmann et al. 2011). The SiGe layer grown at 700°C presents a smaller peak width than the one grown at 650°C. The layer quality is thus improved at 700°C.

Cross-sectional TEM observations were performed on SiGe layers grown at 700°C which had the smoothest surface and the smallest FWHM. **Figure III.7** shows an image taken using the High Angle Annular Dark Field detector, where brighter contrast is related to higher atomic mass. In the other images, Energy-dispersive X-ray spectroscopy (EDX) has been used, to highlight the atomic concentrations of Si, O and Ge.

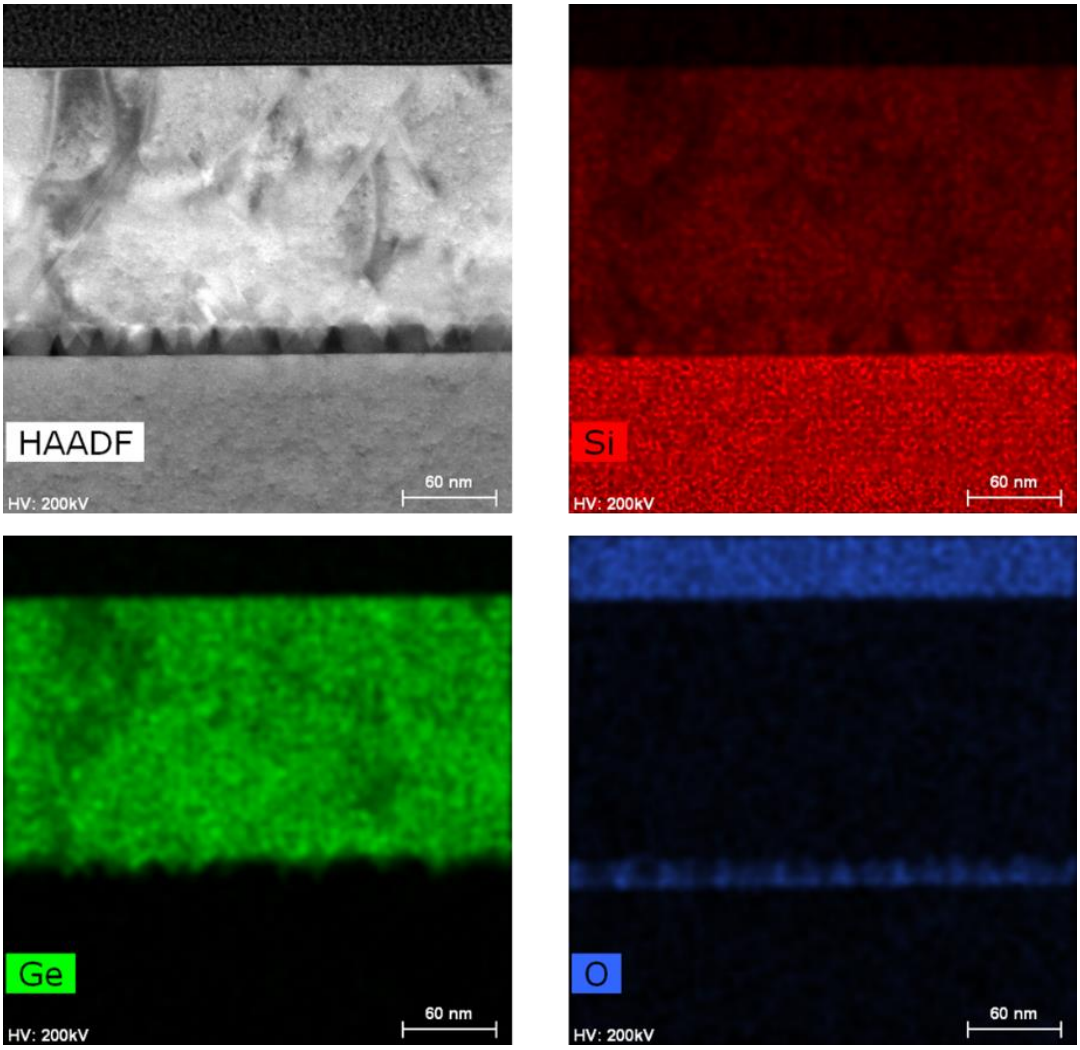


Figure III.7 Cross-sectional TEM image of the entire thickness of SiGe layer grown at 700°C on Si nano-pillars acquired with the HAADF detector (top left) and other images where the same area is imaged by TEM EDX, with different elements highlighted: Si (red), O (blue) and Ge (green).

The higher magnification TEM image in **Figure III.8** shows more precisely the interfaces between the silicon pillars and the SiGe layer. Si nano-pillars kept their truncated pyramid shape upon SiGe capping. The SiO_2 walls separating them are triangular due to the surface preparation used prior to epitaxy (Siconi etches SiO_2 isotropically). The TEM image suggests that nucleation of defects such as twins and stacking faults starts at the interface between the silicon pillars and the SiGe layer on top, usually just above the SiO_2 wall. There is almost one defect per pillar although it appears on larger field images that some pillars are free of defects. However, the TEM image remains difficult to interpret because of projection effects and the very small size of the nano-objects observed, which are smaller than the thickness of a typical lamella.

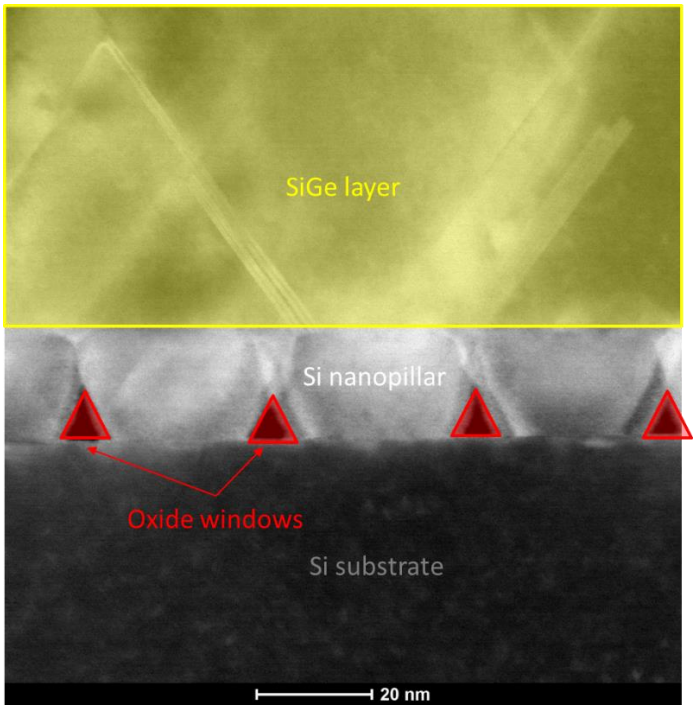


Figure III.8 Cross-sectional TEM image of SiGe layer grown at 700°C on Si nano-pillars showing the entire structure with the Si substrate, the oxide windows and the SiGe layer with defects.

III.3.c. SiGe nano-pillars growth

The use of SiGe nano-pillars was investigated in order to improve the quality of thick, coalesced SiGe layers grown on top. SiGe nano-pillars 20 nm high with a targeted Ge content of 25% were grown at 650°C and 700°C using a selective epitaxial process based on GeH_4, SiH_2Cl_2 and H_2 (Bodnar et al. 1997)(Hartmann et al. 2002)(Hartmann et al. 2012). The growth conditions were calibrated using blanket growth on silicon, to have the same Ge content and height of the pillars. **Figure III.9** shows tilted SEM images (left) and 1x1 µm² AFM scans (right) with the same z-scale. There is little difference between 650°C and 700°C, with all pillars being well defined and uniform.

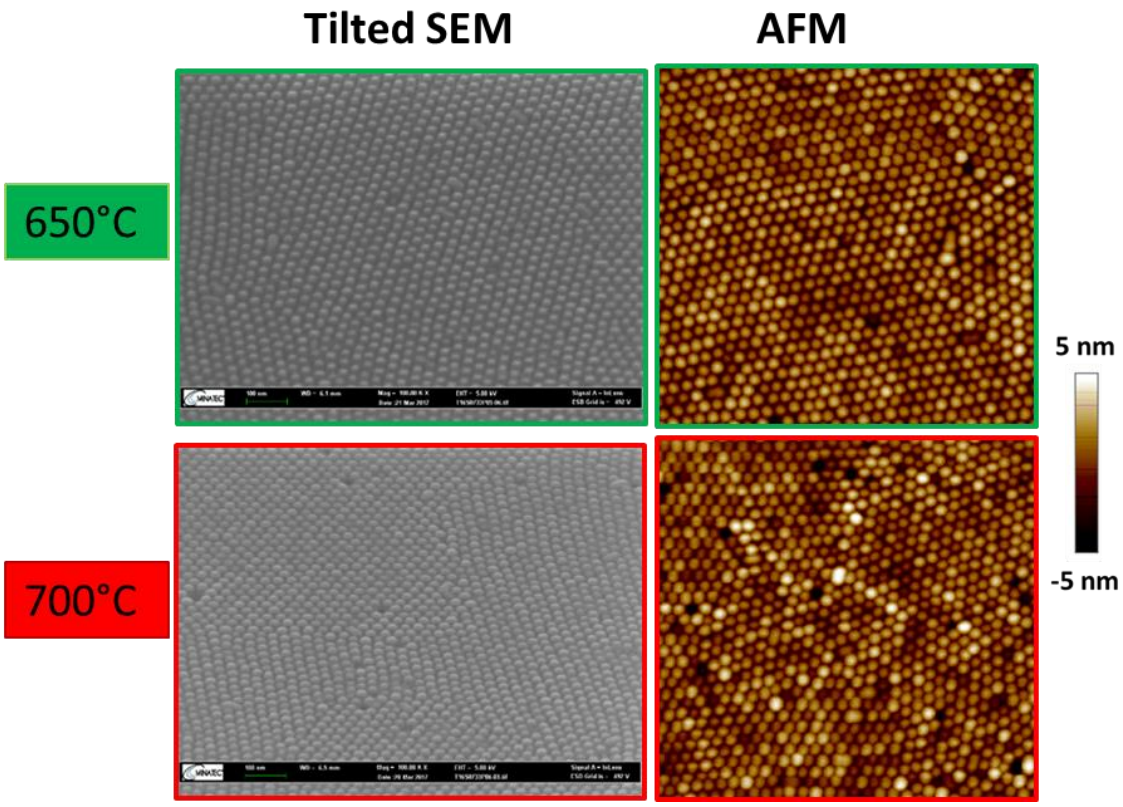


Figure III.9 1x1 µm² AFM scans (right) and tilted SEM images (left) of SiGe nano-pillars grown at 650°C and 700°C. AFM mage sides are along the <110> directions

These pillars were then analysed with in-plane XRD around the (220), and the reciprocal space maps generated are shown in **Figure III.10**. Fringes are clearly present on the RSMs. The fringe spacing corresponds to 35 nm in the in-plane direction, i.e. the pillar spacing just after lithography.

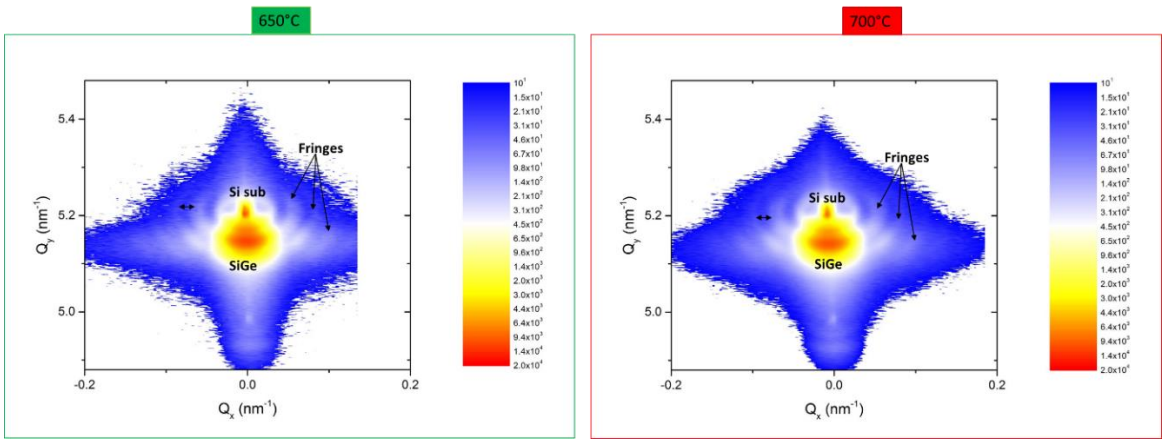
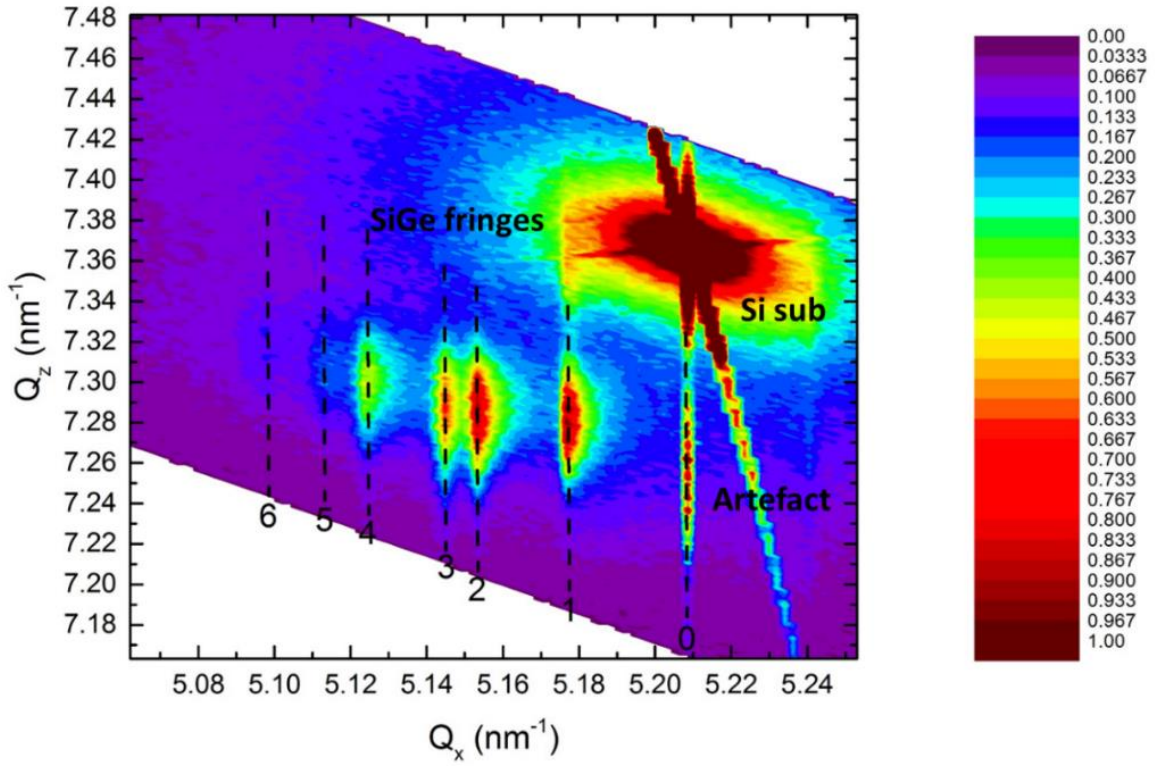


Figure III.10 (220) in-plane RSM measurements of SiGe nano-pillars grown at 650°C and 700°C.

For the sample at 650°C, an XRD RSM was acquired around the (224) out-of-plane reflection, as shown in **Figure III.11**. It should be noted that the large diagonal lines and the dotted

vertical lines are measurement artefacts. We see clearly the fringes corresponding to different spacings between nano-pillars. With the geometric analysis shown below the image, we confirm that those fringes are due to the mask, with a spacing very close to the 35 nm nominal pitch. However, due to these fringes, it was not possible to track strain or Ge content variations during growth.



Fringe number	Q_x (nm^{-1})	$d(hk) = \frac{1}{Qx(0) - Qx(n)}$ (nm)	hk (hexagonal copolymer network)		Pitch= $d(hk)\left[(h^2 + k^2 + hk)\frac{4}{3}\right]^{1/2}$ (nm)
			h	k	
0	5.209	---	0	0	---
1	5.177	31.52	1	0	36.4
2	5.153	17.97	1	1	35.9
3	5.145	15.56	2	0	35.9
4	5.124	11.83	1	2	36.1
5	5.112	10.36	3	0	35.9
6	5.097	8.92	2	2	35.7

Figure III.11 (224) RSM measurement of SiGe nano-pillars grown at 650°C (top) and table showing the position of SiGe fringes corresponding to different spacings between nano-pillars (bottom).

III.3.d. SiGe nano-heteroepitaxy on SiGe nano-pillars

After these developments on SiGe pillars, we grew our reference 200 nm thick SiGe 25% layer at 700°C on SiGe nano-pillars selectively grown at 650 and 700°C as in the previous experiment (Bodnar et al. 1997)(Hartmann et al. 2002)(Hartmann et al. 2012). **Figure III.12** shows that the SiGe layers are relatively smooth.

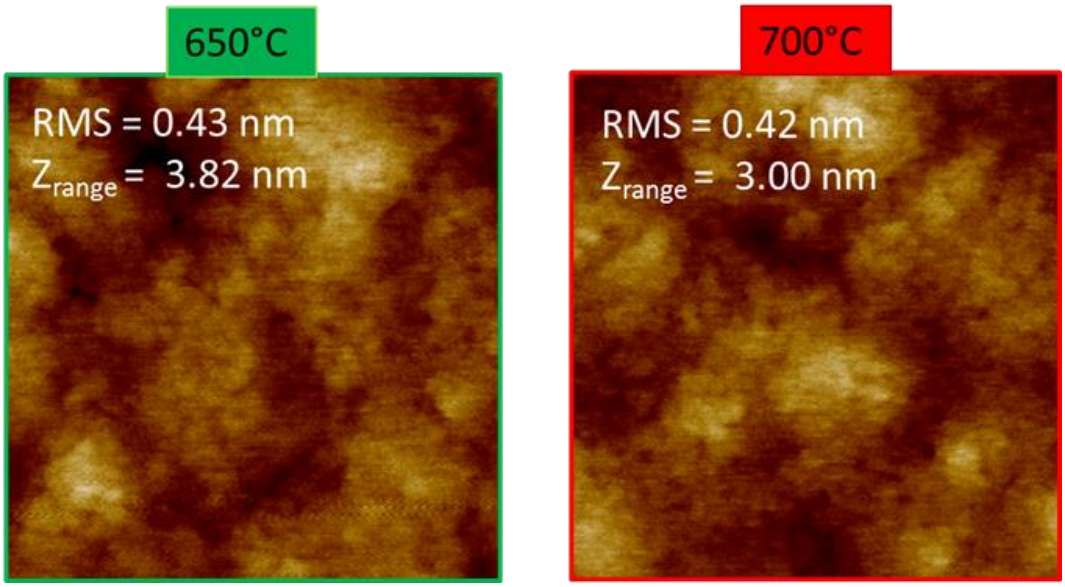


Figure III.12 1x1 µm² AFM images of the SiGe layers grown on SiGe nano-pillars at different temperatures and corresponding RMS roughness and Z range values. Image sides are along the <110> directions.

XRD reciprocal space maps around the (004) and (224) peaks of these samples are shown in **Figure III.13**, with the in-plane and out-of-plane lattice parameters, Ge content, relaxation, and peak width listed in **Table III.3**.

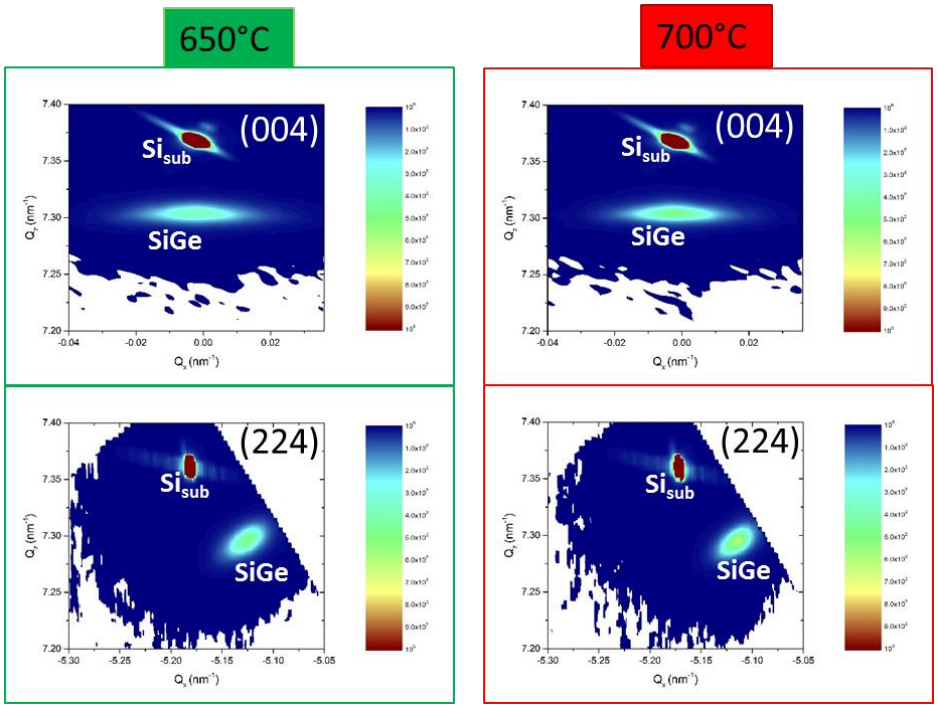


Figure III.13 (004) and (224) X-Ray Diffraction Reciprocal Space Maps of SiGe layers grown at 650°C and 700°C on SiGe nano-pillars.

SiGe nano-pillars growth temperature (°C)	In-plane lattice constant (Å)	Out-of-plane lattice constant (Å)	Ge concentration (%)	Degree of relaxation (%)	FWHM (arcsec)
650	5.488	5.480	25.4	109	684
700	5.489	5.479	25.5	111	557

Table III.3 In-plane and out-of-plane lattice parameters, Ge content, macroscopic degree of strain relaxation and FWHM of SiGe layers with SiGe nano-pillars grown at 650 and 700°C

The Ge concentrations obtained are close to the 25% aimed for. Once again, high values of relaxation are obtained with the nano-heteroepitaxy approach. The samples with SiGe nano-pillars at 650°C and 700°C are tensile strained (i.e. with $R > 100\%$), with a degree of relaxation around 110%. When we compute the relaxation degree of the tensile strained layer $R = \frac{(a^{//}_{SiGe} - a_{Si\,TG})}{(a^{Bulk}_{SiGe\,TG} - a_{Si\,TG})}$, where $a^{Bulk}_{SiGe\,TG}$ and $a_{Si\,TG}$ are the unstrained parameter of SiGe and the Si lattice parameter at a growth temperature of 650°C or 700°C, it gives values around 100% ($a^{Bulk}_{SiGe\,TG}$ and $a_{Si\,TG}$ were taken from (Reeber and Wang 1996)). This means that the layers are fully relaxed at growth temperature. When cooling to room temperature, tensile strain is added to the layers due to thermal expansion mismatch. The lowest FWHM (557 arcseconds) is obtained for the sample with SiGe nano-pillars grown at 700°C. This value is lower than that with Si nano-pillars, which means that SiGe nano-pillars are beneficial in terms of layer quality.

TEM observations were performed on the sample with the lowest FWHM (i.e. the one with SiGe nano-pillars grown at 700°C), in order to have some insight into the nature of crystalline defects in such stacks.

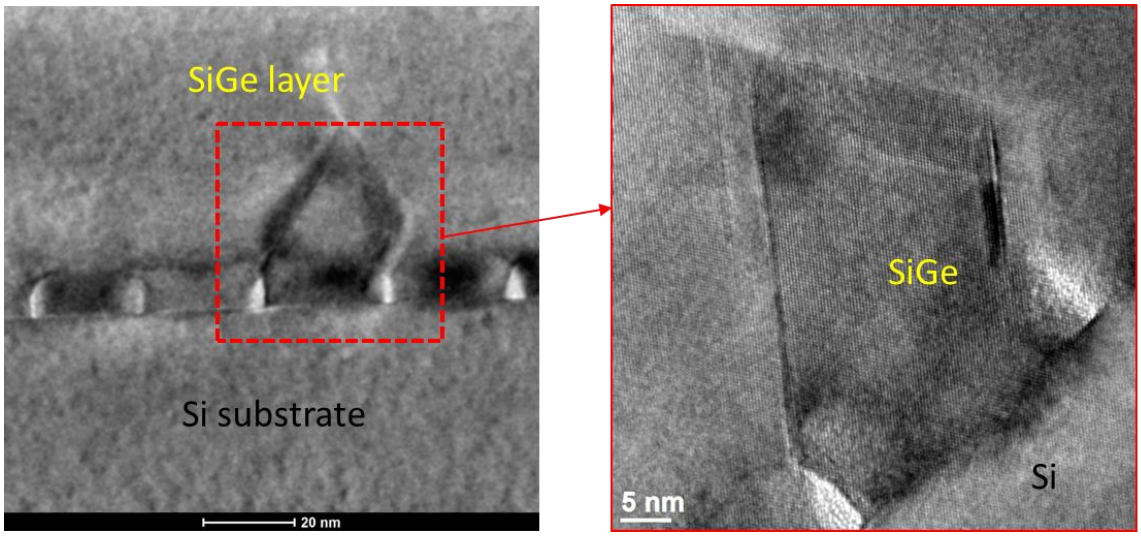


Figure III.14 Cross-sectional TEM images of SiGe nano-pillars and 2D layer grown at 700°C on top.

Analysis of the TEM image in **Figure III.14** suggests that, as before, SiO_2 walls separating nano-pillars have a triangular shape due to the isotropic oxide etching during the Siconi surface preparation prior to epitaxy. Defects such as stacking faults or twins nucleating at the top of the SiO_2 walls are comparable to defects seen with Si nano-pillars, meaning that the nature of the nano-pillars has no major impact on defects type.

We appear to have very similar defect generation mechanisms for Si and SiGe nano-pillars (from a one-to-one comparison of TEM images) which could be due to one of the following factors:

- The growth of SiGe on the {111} facets of pillars may be favorable to the formation of twin defects as discussed in Ref. (Kuan and Iyer 1991).
- Defects may be created during growth front coalescence above the oxide mask.
- The thermal stress generated by the oxide mask during growth could also be a source of defects (Leonhardt et al. 2011).

III.4. Conclusion

We have studied the nano-heteroepitaxy of SiGe layers on Si and SiGe nano-pillars. An integration scheme based on diblock copolymer patterning was used in order to have a fairly regular nanometer-size oxide template for growth. The selective epitaxy of Si nano-pillars was first investigated. A fully selective process was obtained with the use of a surface preparation using a NH_3/NF_3-based remote plasma. For SiGe, the same high quality of nano-pillars was achieved for temperatures between 650°C and 700°C. A homogeneous process in terms of nano-pillars height was achieved for Si and SiGe nano-pillars. In-plane (220) and (224) RSM showed fringes which were characteristic of the geometrical configuration of the nano-template, showing that the mask was highly oriented and of good quality.

Smooth SiGe surfaces and high degrees of strain relaxation were obtained in the 650-700°C temperature range for SiGe layers. XRD and TEM characterization showed that the SiGe layers had defects, however. The use of SiGe instead of Si nano-pillars resulted in higher quality layers, especially when growth was conducted at 700°C.

TEM imaging showed that defect generation typically occurred at the interface between pillars and bulk SiGe, above the SiO_2 mask. This suggested that defects were generated by:

- Growth on Si{111} facets resulting in twin formation
- The coalescence process itself
- Thermal stress generated by the oxide mask during growth which may cause defect generation.

In next chapter, the second hypothesis will be verified by a study of the coalescence process at the very early growth stages.

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CHAPTER IV:
Investigation of SiGe nano-pillars coalescence

Contents of chapter IV

IV.1. Introduction

In the previous chapter, we have shown that nano-heteroepitaxy yielded smooth and fully relaxed SiGe layers with a thickness of only a few hundreds of nm, which could then be used as templates for tensile strained Si layers. However, the generation of defects such as stacking faults or twins was inherent to the process itself regardless of the nature of the nano-pillars (Si or SiGe).

Several studies dealing with epitaxial lateral overgrowth (Langdo et al. 2000) (Leonhardt et al. 2011), aspect ratio trapping (Ghosh et al. 2011) (Kim et al. 2014) and 3D heteroepitaxy (Salvalaglio et al. 2015) (Skibitzki et al. 2016) of Ge films on patterned Si substrates showed the same type of planar defects occurring at the coalescence front. Another work on Si and SiGe fin merging showed the presence of the same defects (Hikavyy et al. 2014). It is therefore likely that these defects occur during the coalescence process itself, during which adjacent pillars merge in order to form a 2D layer.

To the best of our knowledge, a study of the coalescence process at the very early stages of growth, especially in tens of nm wide, with closely packed holes has not previously been conducted, hence the novelty of the current study. In this chapter, we investigate the behavior of SiGe 25% pillars grown on our SiO_2 based nano-template, characterizing them at different stages of the coalescence process.

IV.2. Experimental details

IV.2.a. Nano-template features

As shown in **Figure IV.1**, we used a substrate patterning process flow inspired from the previous study. It starts with slightly p-type doped, nominally on-axis 300 mm bulk Si(001) on which 20 nm thick thermal SiO_2 layer is deposited. Next, a diblock copolymer patterning is performed followed by a SiO_2 etching step yielding cylindrical cavities with a 20 nm diameter and a 15 nm spacing in a closely packed hexagonal configuration. Surface preparation before nano-pillars growth is a critical step for this process flow since a “HF-last” wet cleaning did not allow us to selectively grow SiGe nano-pillars. The solution to this problem consisted in using a dry Siconi treatment (with a NH_3/NF_3 remote plasma used to convert native oxides into salts that were sublimated at low temperature) (Yang et al. 2010) (Raynal et al. 2018).

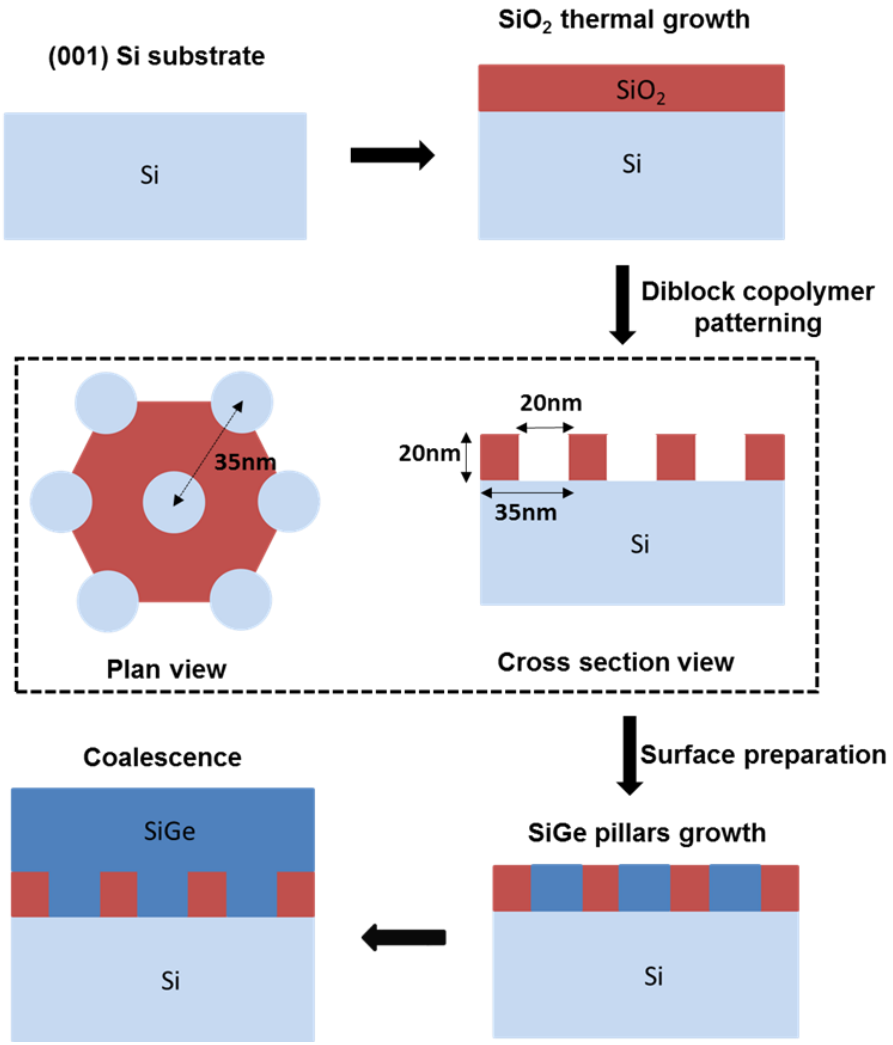

Figure IV.1 SiO_2 nano-template fabrication process flow and SiGe 25% nano-heteroepitaxy integration scheme.

IV.2.b. Growth conditions

SiGe nano-pillars of different thicknesses were then selectively grown. The thickness was estimated from the growth time using the growth rate of SiGe obtained on a blanket Si (001) wafer. The 300 mm Epsilon 3200 Reduced Pressure – Chemical Vapor Deposition tool from ASM America was used for the growth, with the pressure kept at 20 Torr and SiH_2Cl_2 and GeH_4 used as Si and Ge gaseous precursors respectively. The purified H_2 carrier gas flow, several tens of liters per minute, was not altered during the experiments. 20, 25, 30 and 35 nm high SiGe nano-pillars with a targeted Ge content of 25% were selectively grown at 700°C, 20 Torr with $[SiH_2Cl_2]/[H_2]$=0.003 and $[GeH_4]/[H_2]$=0.00023 mass-flow ratios. The growth conditions were those used to obtain the best quality coalesced SiGe layers on SiGe nano-pillars. The resulting growth rate was 20 nm/min.

IV.2.c. Sample characterization

The SiGe nano-pillars were characterized by X-Ray Diffraction (XRD) which allowed us to calculate the Ge concentration and the macroscopic degree of strain relaxation from conventional Omega-2Theta scans around the (004) and (224) orders. These XRD measurements were performed using a Panalytical X'Pert tool with a copper anticathode as the X-Ray source, a 4 bounce symmetric Ge(220) Bartels monochromator and wide slits in front of the detector. Tapping mode Atomic Force Microscopy (AFM) measurements were carried out on a Bruker Dimension FastScan platform and contact mode Scanning Spreading Resistance Microscopy (SSRM) measurements were conducted on a Bruker Dimension Icon SSRM-HR platform using a diamond probe form IMEC CAMS. Sample bias was fixed at -1 V and the electrical contact was obtained using a silver lacquer. Finally, cross-sectional Transmission Electron Microscopy (TEM) was carried out in a JEOL 3010 microscope operating at 300 keV. Nearly parallel sidewall TEM lamellae were prepared in the <110> directions using a Precision Ion Polishing System PIPS II from Gatan.

IV.3. Experimental results

IV.3.a. AFM

Figure IV.2 shows 1x1 μm^2 AFM scans of SiGe nano-pillars at different thicknesses. These AFM scans were performed at the center of each sample after epitaxy and show a clear evolution of the coalescence as the thickness increases. SiGe nano-pillars 20 nm thick are well ordered and homogeneous in terms of height and diameter, as previously seen using this process. The dark spots at 20 nm could be pillar growth filled well below the oxide wall due to delayed growth. These dark spots might also be empty sites due to mask defects or imperfect surface preparation. At 25 nm, a few nano-pillars start to coalesce with their neighbors, resulting in some randomly located nano-pillars with a higher diameter. However, the majority of nano-pillars have not yet coalesced. A thickness of 30 nm yields a higher coalescence degree where the majority of nano-pillars have merged and their mean diameter is higher. In addition, we note that coalesced nano-pillars are not only cylindrical as before but have various shapes. However, there are still some nano-pillars which have the same size and shape as in the previous two samples, i.e. which have not coalesced. For 35 nm growth, all the initial nano-pillars have now coalesced and the conglomerates take various shapes and sizes. The dark spots at 35 nm might be due to growth depletion in sites adjacent to coalesced structures.

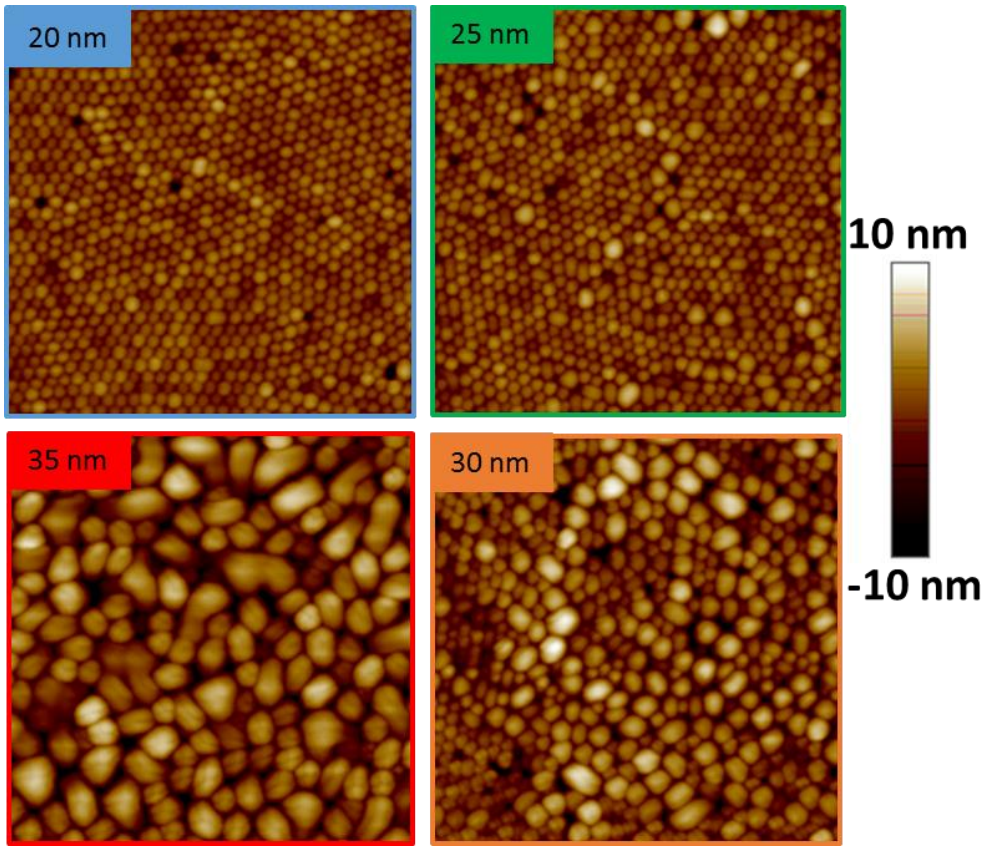

Figure IV.2 1 x 1 µm² AFM scans of SiGe nano-pillars growth at 20 nm (blue), 25 nm (green), 30 nm (orange) and 35 nm (red). Image sides are along the <110> directions.

In order to quantify the coalescence of SiGe nano-pillars, a particle analysis of the AFM scans was performed using the Nanoscope Analysis software from Bruker. **Figure IV.3** shows the number of grains and the mean value of grain diameter as a function of SiGe nano-pillar thickness. As expected, the average grain size increases and the number of grains decreases as the SiGe thickness increases.

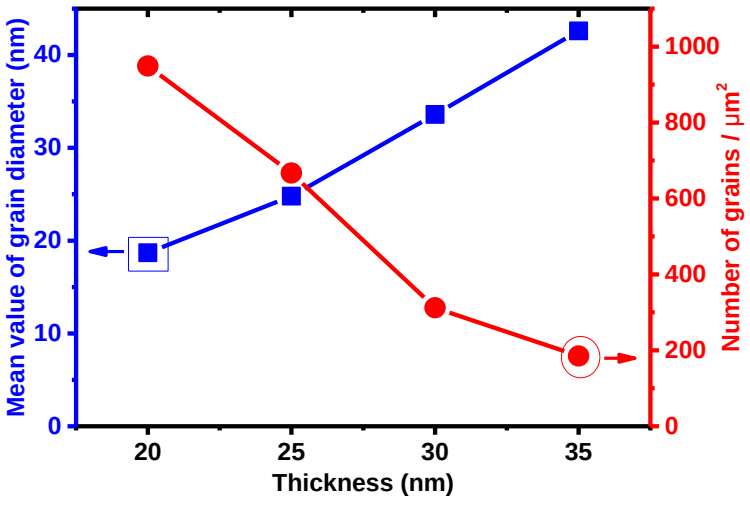

Figure IV.3 Number of grains (red) and mean value of grain diameter (blue) as function of thickness.

We can consider a degree of coalescence, where:

$$Degree\ of\ coalescence = \frac{1}{number\ of\ grains\ on\ a\ 1x1\ \mu m^2\ AFM\ image} \qquad \textbf{E.q. IV.1}$$

A value of 1 would correspond to a full coalescence, where the 1x1 µm^2 scan contains only one grain. As shown in **Figure IV.4**, fitting the experimental data with an exponential curve would yield full coalescence after the growth of ~80 nm of SiGe. In other experiments, we have seen that the coalescence was not fully complete at 60 nm, but was coalesced before 220 nm, so this is a coherent result.

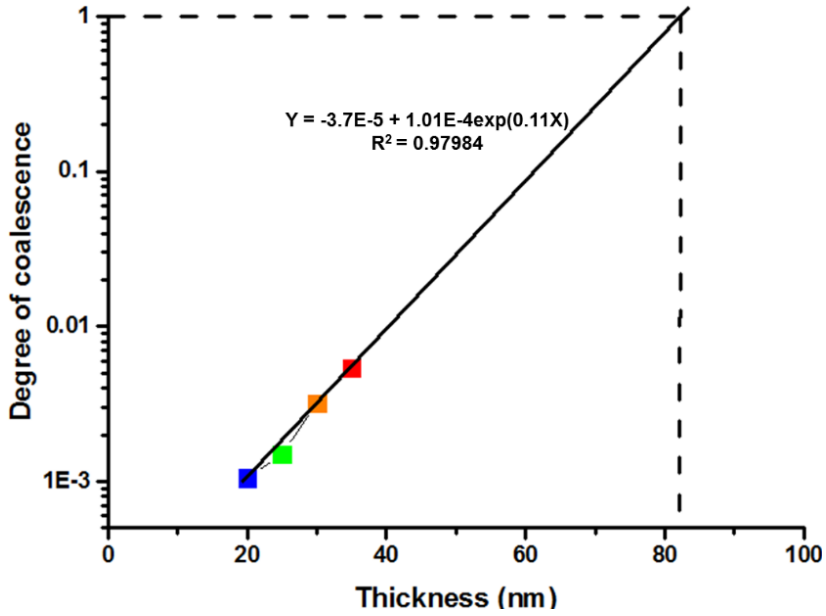

Figure IV.4 Degree of coalescence versus growth thickness. The extrapolation curve allows us to predict full coalescence across a 1x1 µm² area at ~80 nm.

IV.3.b. XRD

The Omega-2Theta scans around the (004) and (224) diffraction orders for the 4 samples are shown in **Figure IV.5**. The Si (004) peak is clearly visible at 34.56°. In the grazing incidence configuration, the Si (224) peak is located at 8.75°. Due to the small amount of material that diffracted, the SiGe peak intensity was weak and therefore hard to measure accurately. A 1° slit was used for (004) measurements, which gave the best trade-off in terms of peak resolution and intensity. For the (224) XRD order, the intensity was even lower and so the angular position of the SiGe peak was even harder to pinpoint. Despite this difficulties, we used Gaussian fits to estimate the SiGe peak position. By analyzing the (004) and (224) Omega-2Theta scans, we can calculate the Ge concentration and the macroscopic degree of strain relaxation R of the SiGe layer, where

$$R = \frac{a_{SiGe}^{//} - a_{Si}}{a_{SiGe}^{bulk} - a_{Si}}$$ **E.q. IV.2**

and $a_{SiGe}^{//}$, a_{SiGe}^{bulk} and a_{Si} are the in-plane lattice parameter of SiGe, the bulk, unstrained parameter of SiGe and the Si lattice parameter, respectively.

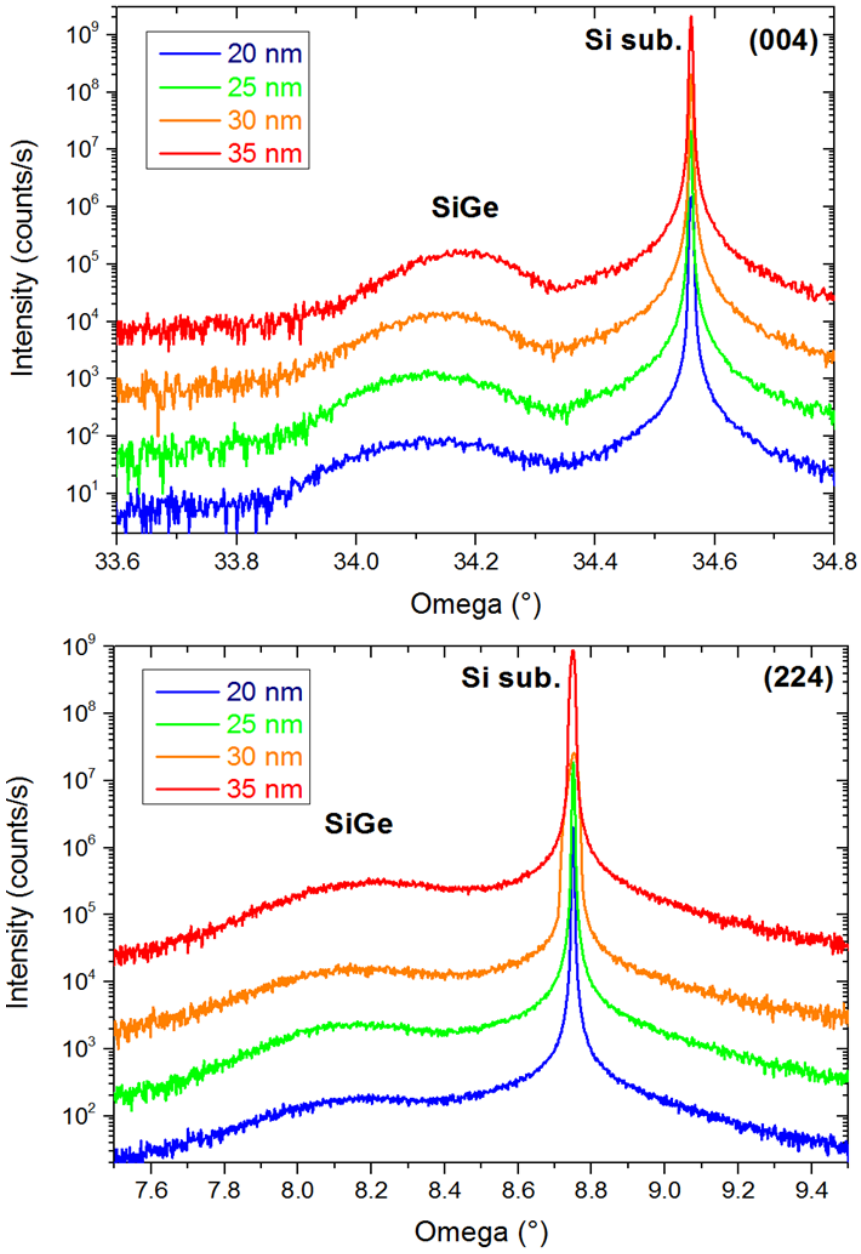

Figure IV.5 Omega-2Theta scans around the (004) (top) and (224) (bottom) XRD orders for the 20 nm (blue), 25 nm (green), 30 nm (orange) and 35 nm (red) samples..

The Ge content and relaxation degree of the nano-pillars at different thicknesses are shown in **Figure IV.6**. As expected, the average degree of strain relaxation of the nano-pillars increases with the thickness, from 71% for 20 nm high pillars up to 91% for 35 nm high pillars. As the nano-pillars grow, they emerge from the nano-cavities and a very fast relaxation is

favored. In terms of Ge content, it is roughly constant at around 25% for the four samples grown.

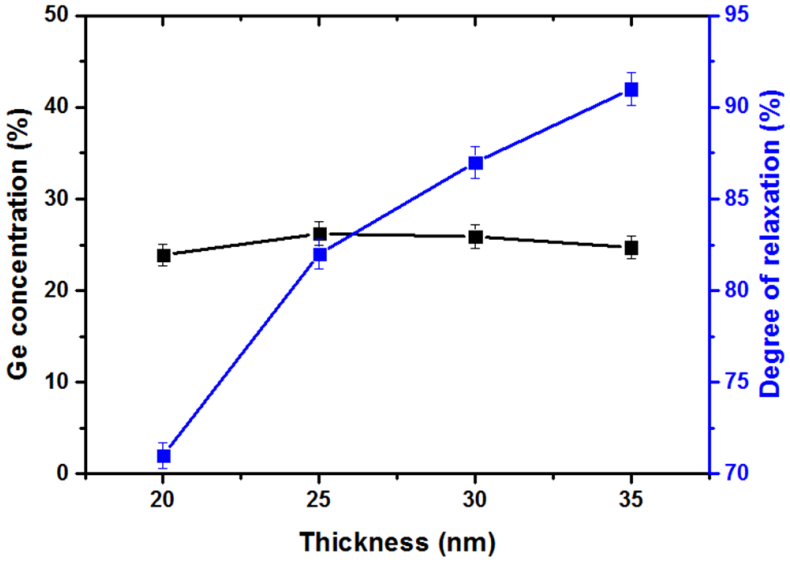

Figure IV.6 Ge concentration (black) and macroscopic degree of strain relaxation (blue) of the SiGe nano-pillars at 20, 25, 30 and 35 nm.

IV.3.c. SSRM

SSRM was used to investigate defect generation in our samples. This scanning probe microscopy technique measures electrical resistance by applying a bias voltage to the scanned material and collecting the current through a conducting tip, in order to calculate the resistance of the layer. The electrical properties of the layers are likely to change as the defect density changes, and so this technique should help identify individual grains where defects are generated.

Two samples were analyzed using this technique, those with 20 nm and 35 nm high SiGe nano-pillars. Samples were scanned in contact mode using a -1 V bias voltage and a diamond tip. **Figure IV.7** shows 200 x 200 nm^2 SSRM images of the two samples. As expected, the oxide mask is more resistive (in green) than the nano-pillars (in purple). The very good SSRM resolution enables us to distinguish individual nano-pillars which are very uniform from the electrical point of view when their height is 20 nm (left image). For the 35 nm sample (right), there are local resistivity variations within coalescing nano-pillars with the presence of electrical domains marked by striations (indicated by white arrows) inside each set of coalescing nano-pillars. This could be an indicator of structural defects due to coalescence but it has not yet been possible to confirm this.

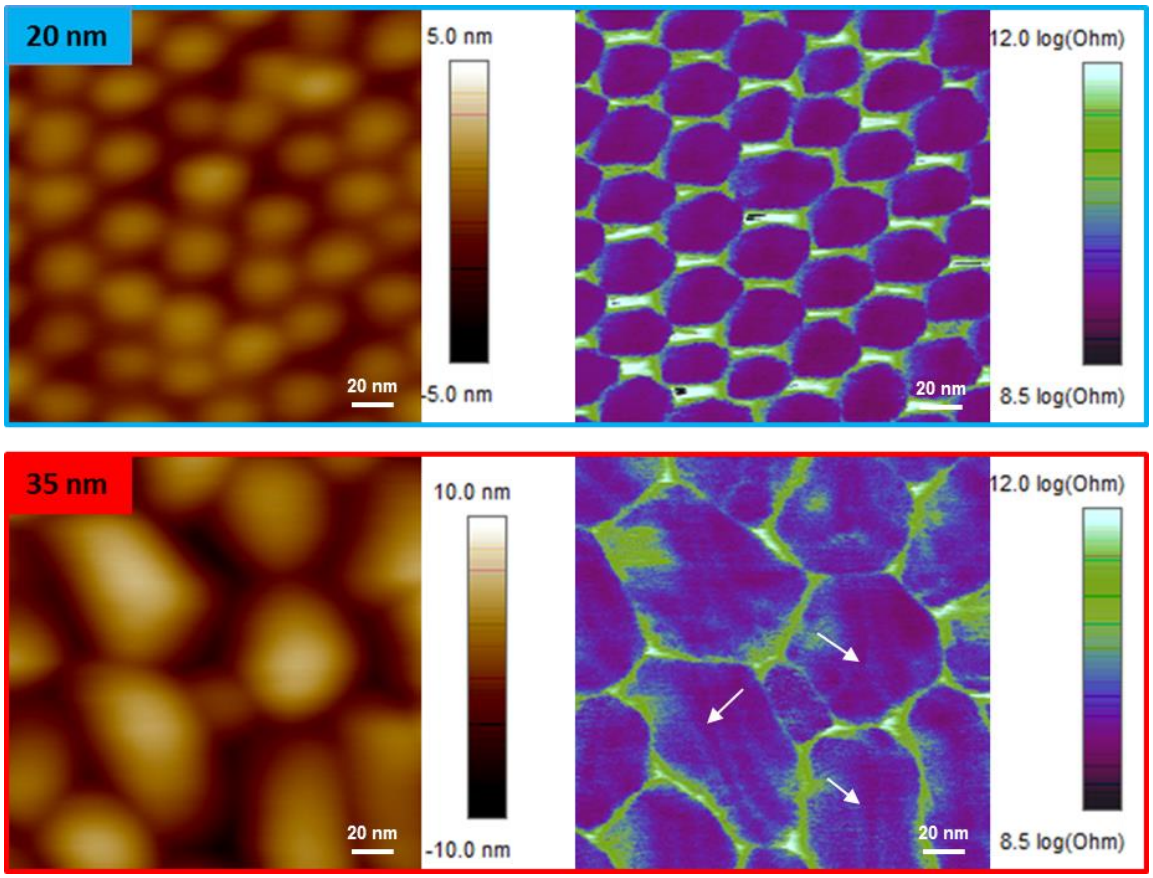

Figure IV.7 200 x 200 nm² SSRM images of SiGe nano-pillar growths at 20 nm and 35 nm. Height scans are shown on the left and electrical scans are presented on the right. Image sides are along the <110> directions.

IV.3.d. TEM

Figure IV.8 shows a collection of cross-sectional high resolution TEM images of various SiGe nano-pillars at 20 nm thickness. None of the 12 nano-pillars imaged show any crystalline defects. This is coherent with the SSRM images which showed that the electrical resistance of the pillars was very uniform, i.e. that they were most likely defect-free. The nano-pillars exhibit faceting which is specific to SiGe selective epitaxial growth (Pribat et al. 2009), with {111} facets clearly visible on the sidewalls of the nano-pillars. This faceting may be detrimental for further growth in terms of defects generation, as growth on SiGe {111} planes has a tendency to encourage the formation of twins (Kuan and Iyer 1991).

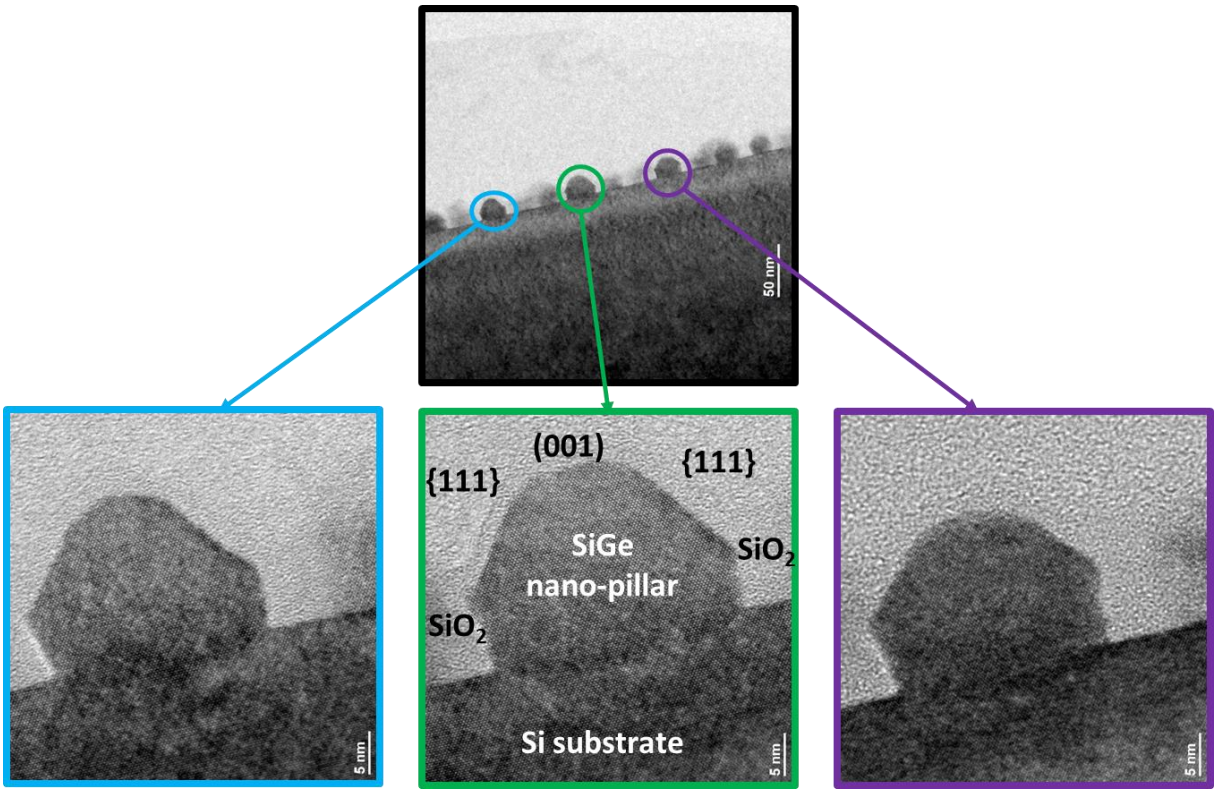

Figure IV.8 High resolution TEM pictures of SiGe nano-pillars growth at 20 nm

High resolution TEM images of partly coalesced, 35 nm high SiGe pillars are shown in **Figure IV.9**. Faceting is lost with coalescence. Coalesced nano-pillars have indeed rounded shapes. This is probably due to surface energy lowering and elastic strain relaxation. Although 20 nm nano-pillars reach their maximum height in the center between the oxide walls, 35 nm coalesced grains have their top right above the oxide walls. This could be due to diffusion at the coalescence fronts. Indeed, the diffusion length at the growth temperature is most likely higher than the pattern size, as shown by Vescan et al (Vescan et al. 1994) and Kamins et al (Kamins et al. 1992).

Several coalescence schemes can be distinguished. The blue-framed image (bottom right) shows defect-free coalescence. The green-framed image (top right) shows coalescence with the presence of a stacking fault at the top of a grain. The red-framed images (top left) show coalescence with stacking faults starting at the summit of the oxide sidewall, and this is the most common configuration. Those stacking faults might be due to the oxide pattern, which is not perfectly regular and symmetric, resulting in an uneven merging of nano-pillar crystallographic planes. These defects may also be due to the coalescence process itself as the interplanar spacing of two merging fronts may not be equivalent (different degrees of strain relaxation between individual nano-pillars, for instance). Finally, the purple-framed images show coalescence with the presence of twinning defects after merging. This might be linked to the SiGe nano-pillars faceting as discussed above.

Junctions between adjacent grains in coalesced nano-pillars are dislocations-free. There are also no dislocations at the interface between the Si substrate and SiGe nano-pillars (thanks to

additional degrees of freedom allowing elastic strain relaxation).The only defects seen at the junctions of adjacent grains are planar defects such as stacking faults and twins. We suggest that the striations seen in the SSRM images may be an electrical manifestation of structural defects such as stacking faults and twins in the coalesced nano-pillars, but this would have to be confirmed with further experiments.

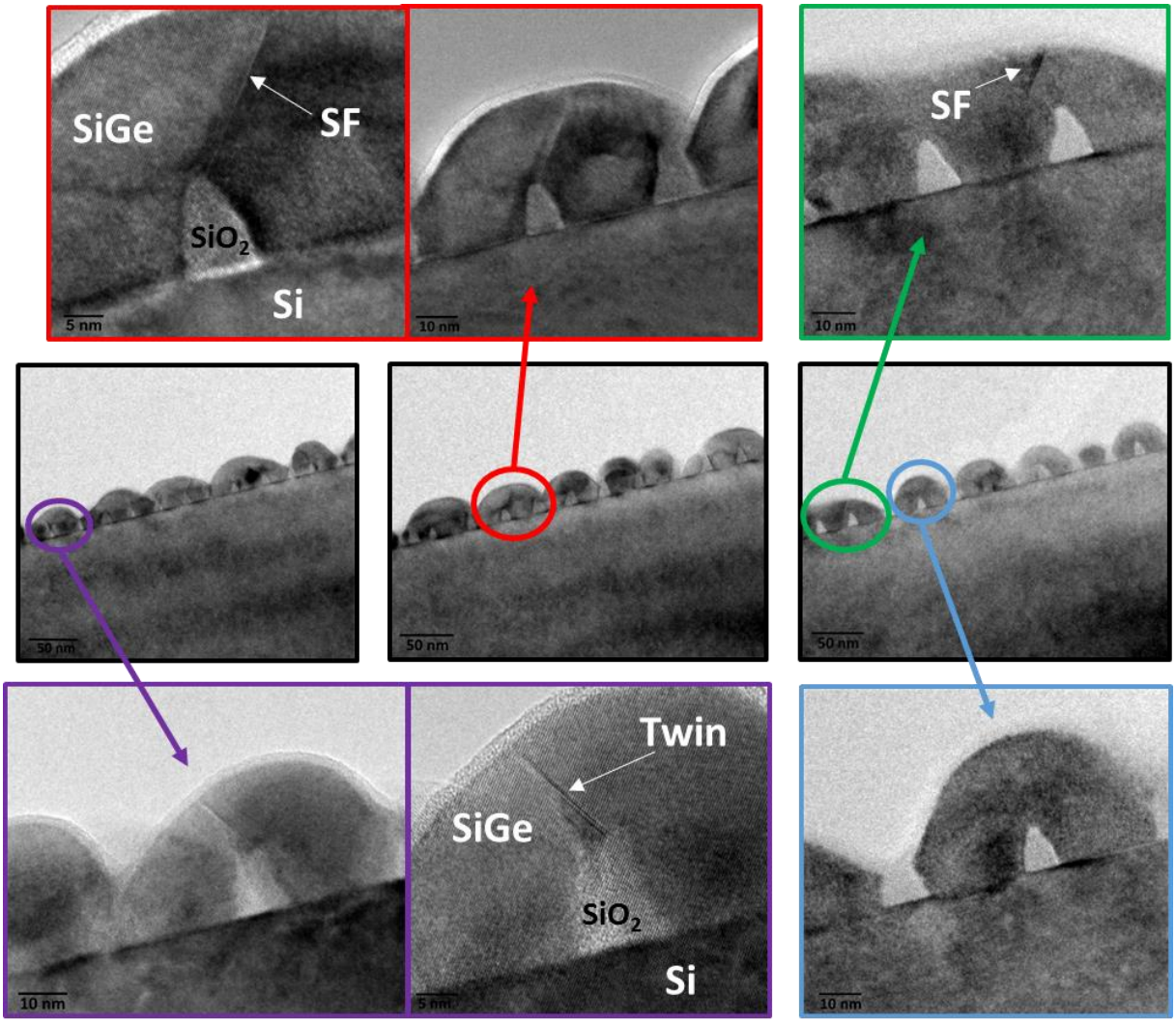

Figure IV.9 Collection of high resolution TEM pictures of SiGe nano-pillars growth at 35 nm.

IV.4. Discussion on defects generation

Besides the defects generation hypothesis given in the previous section, various explanations were provided in other references. Langdo et al (Langdo et al. 2000) investigated the “epitaxial necking” of Ge on SiO_2/Si substrates in 100 nm wide holes. The presence of stacking faults and twins at the merging fronts was attributed to an insufficient time for adatoms to reach stable atomic arrangements because of complex faceting and/or oxide

surface roughness. Another possible explanation was that during growth front coalescence, Ge atoms had to bridge the distance between holes over the SiO_2/Si substrate, which was not necessarily an integral number of Ge unit cells. This results in strain which then causes the generation of defects in the coalescence region. Other studies by Leonhardt et al (Leonhardt et al. 2011) and Ghosh et al (Ghosh et al. 2011) showed the presence of stacking faults and twins after the aspect ratio trapping of Ge layers. Finite element modeling showed that the tensile stress was high in the fraction of the Ge film facing the top corner of the SiO_2 template after cooling from growth temperature to room temperature. These high stress regions were where defects were observed, and so it was suggested that these defects were generated due to the thermal mismatch stress during cooling after growth.

IV.5. Conclusion

We have studied the coalescence of SiGe nano-pillars using an integration scheme based on diblock copolymer patterning in order to have a nanometer-sized oxide template. SiGe 25% nano-pillars 20 to 35 nm high were selectively grown with a chlorinated chemistry, and a Siconi NH_3/NF_3-based remote plasma treatment was used to correctly prepare the template for epitaxy.

SiGe nano-pillars merging was first examined with AFM and the evolution in terms of grain shape, number and diameter was tracked. Starting at 30 nm, grains took various shapes depending on the number of merging nano-pillars, making the coalescence process heterogeneous. As expected, the average grain size increased and the number of grains decreased as the deposited thickness increased. A plot of the coalescence degree (i.e. the inverse of the number of grains) as a function of thickness enabled us to predict full coalescence at ~80 nm.

Using XRD, we found that relaxation increased with the thickness, reaching a value as high as 91% for 35 nm thick, partly coalesced pillars, confirming that growth from nano-cavities resulted in a very fast relaxation. There was no change in chemical composition across this range of thicknesses.

SSRM demonstrated a good sensitivity concerning the electrical activity of the nano-pillars. At 20 nm, the electrical distinction between nano-pillars and the oxide mask was straightforward and the electrical resistance of those pillars was very uniform. At 35 nm, we detected local resistivity variations within coalescing nano-pillars, which was likely due to different electrical behaviour of structural defects.

Finally, TEM was used to investigate structural defect generation during coalescence. TEM imaging of the 20 nm sample showed facetted and defect free nano-pillars. The analysis of the 35 nm samples showed various cases ranging from defect free nano-pillars merging to the generation of stacking faults and twinning at the early stages of coalescence. A correlation between SSRM and TEM was drawn, paving the way towards the use of SSRM as a fast and efficient way of identifying coalescence defects.

Besides coalescence, defects generation mechanisms in SiGe nano-heteroepitaxy seem to be intimately related to the nano-template as well (thermal mismatch stress, oxide surface roughness, etc.). This is why we decided to investigate the nano-template impact on SiGe nano-heteroepitaxy in the next chapter.

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CHAPTER V:
Investigation of the nano-template

Contents of chapter V

V.1. Introduction

In chapter III, we were able to obtain smooth and fully strain relaxed $Si_{0.75}Ge_{0.25}$ layers with a thickness of only 200 nm using heteroepitaxial growth on nano-patterned SiO_2 templates. However, the resulting SiGe layers presented planar defects such as stacking faults and twins. In the previous chapter, we showed that these types of defects were appearing at the very early coalescence stages. The oxide nano-template might be implicated in the defect generation due to surface roughness (Langdo et al. 2000) or the thermal stress generated during cooling down (Leonhardt et al. 2011). In this chapter, we wanted to measure the impact of the nano-template on the SiGe layer quality by exploring three strategies:

- Use of a different pitch size mask
- Oxide mask removal after SiGe nano-pillars growth
- Use of strain free SiN as masking material instead of SiO_2

An original process flow has thus been used to fabricate SiO_2 and SiN based nano-templates, and the nano-heteroepitaxy of 2D SiGe layers on these templates has then been investigated.

V.2. Experimental details

V.2.a. Nano-template features

As described in **Figure V.1**, the substrate patterning process flow starts from slightly p-type doped nominally on-axis 300 mm bulk Si(001) wafers. A 20 nm thick thermal SiO_2 or SiN layer is then deposited to serve as a template for lithography. Next, a diblock copolymer patterning is performed followed by an etching step giving cylindrical cavities with a 20 nm mean diameter and 23 nm spacing in a closely packed hexagonal configuration, giving a pitch of 43 nm, as shown in **Figure V.2**. Surface preparation before nano-pillars growth was critical as a straightforward “HF-last” wet cleaning did not produce selectively grown SiGe nano-pillars. Instead, the following wet cleaning sequence was used: a dip in Ozonized water followed by a dip in diluted HF and finally a wafer drying. Such a solution was more flexible than Siconi NH_3/NF_3-based remote plasma, which was mandatory for 35 nm pitch size masks.

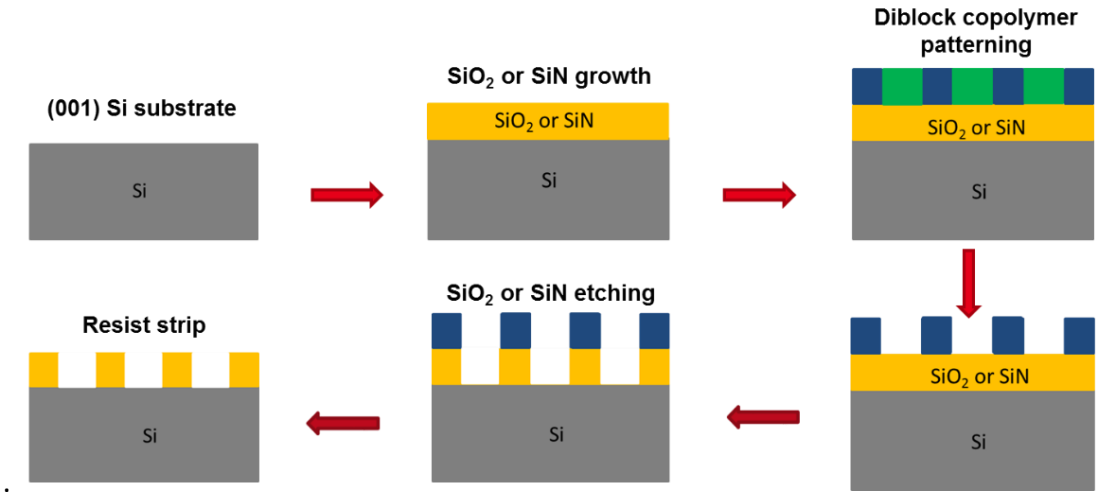

Figure V.1 Nano-template fabrication process flow.

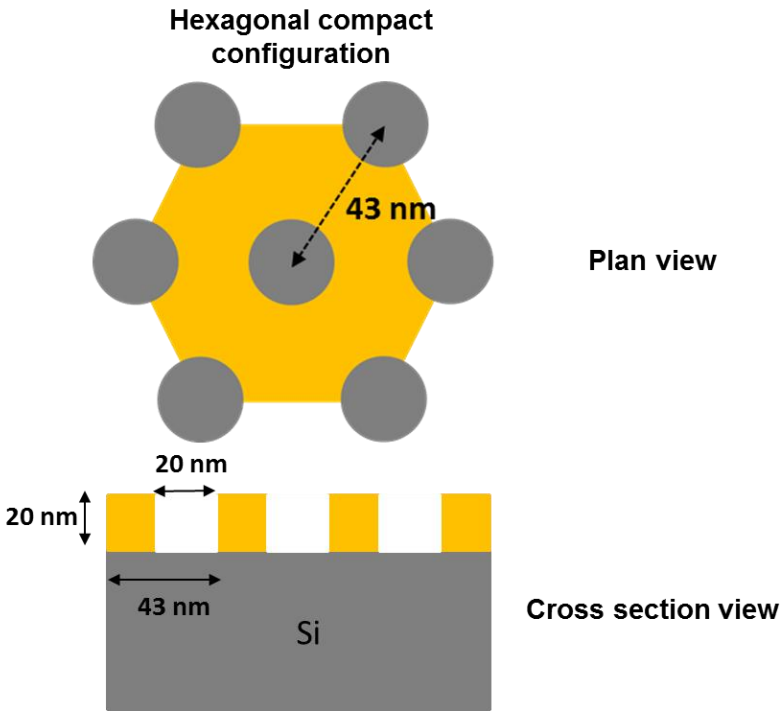

Figure V.2 Plan view schematics of the hexagonal compact configuration defined by the diblock copolymer patterning (top) and cross sectional schematics of the nano-template (bottom)

V.2.b. Growth conditions

We used three integration schemes illustrated in **Figure V.3**. The first consisted in selectively growing SiGe nano-pillars in the Si windows of an oxide mask followed by a thick SiGe layer with the same Ge content. The second consisted in removing the oxide mask after the growth of SiGe nano-pillars, followed by the growth of a thick SiGe layer with the same Ge

content. The third growth scheme was the same as the first one except replacing the SiO_2 mask with a strain free SiN mask.

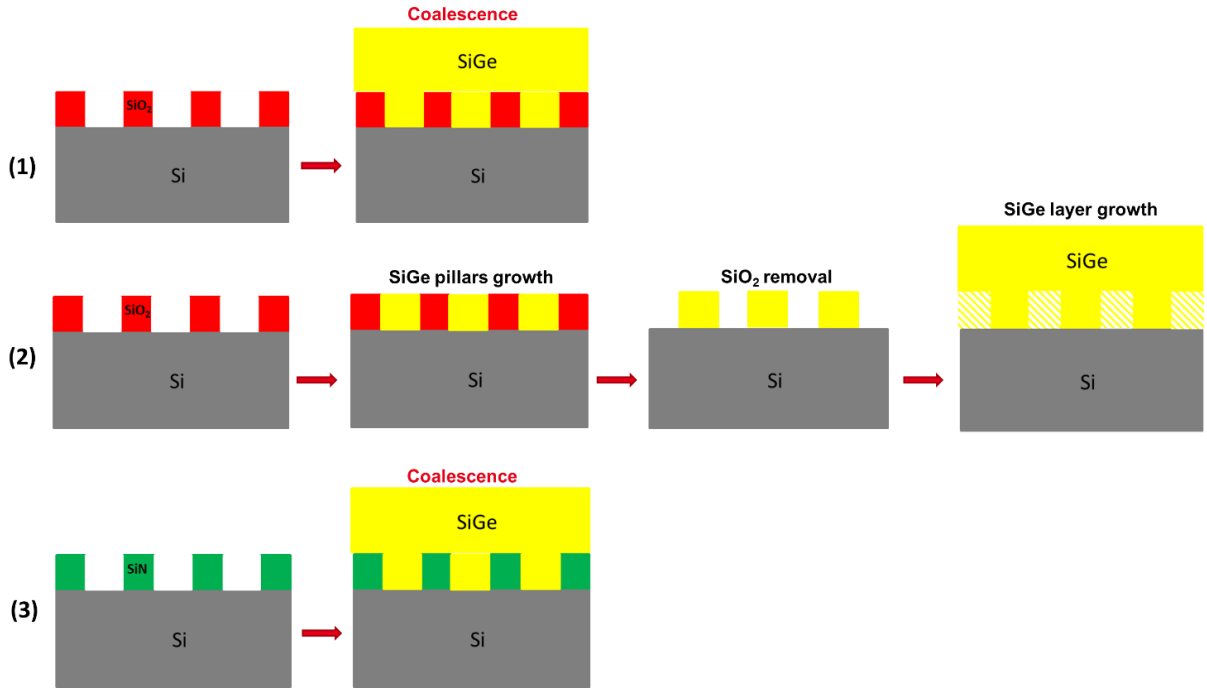

Figure V.3 SiGe nano-heteroepitaxy integration schemes: (1) Growth on a higher pitch size mask of 43 nm (2) Growth without oxide mask (3) Growth with SiN as masking material

Growth occurred at 20 Torr on the 300 mm Epsilon 3200 Reduced Pressure – Chemical Vapour Deposition tool from ASM America, with SiH_2Cl_2 and GeH_4 as Si and Ge gaseous precursors, respectively. The purified H_2 carrier gas flow, several tens of litres per minute, was not altered throughout the experiments. The process used for SiGe growth was performed at 700°C with $[SiH_2Cl_2]/[H_2]=0.003$ and $[GeH_4]/[H_2]=0.00023$. The obtained growth rate was 20 nm/min. This epitaxial process was originally designed for 2D layers growth on Si (001) bulk wafers. This means that the diffusion is favored between nano-pillars during growth. Indeed, the diffusion length at the growth temperature is most likely higher than the pitch size, as shown by Vescan et al (Vescan et al. 1994) and Kamins et al. (Kamins et al. 1992). This means that nucleation on the dielectric and consequently a polycrystalline film formation are not to be expected.

V.2.c. Sample characterization

The thick SiGe layers were characterised by X-Ray Diffraction (XRD), with Ge concentrations and macroscopic degrees of strain relaxation extracted from conventional Omega-2Theta scans around the (004) and (224) orders. A Panalytical X'Pert tool with a copper anticathode as the X-Ray source, a 4 bounce symmetric Ge(220) Bartels monochromator and

wide slits in front of the detector was used for these XRD experiments. Tapping mode Atomic Force Microscopy (AFM) measurements were carried out on a Bruker Dimension FastScan platform. Finally, cross-sectional Transmission Electron Microscopy (TEM) carried out in a JEOL 3010 microscope operating at 300 keV. Nearly parallel sidewall TEM lamella were prepared in one of the <110> directions using a Strata Focus Ion beam microscope from FEI.

V.3. Experimental results

V.3.a. Pitch size effect

In order to validate the 43nm pitch mask, SiGe nano-pillars 20 nm high with a targeted Ge content of 25% were first grown at 700°C using a selective epitaxial process based on GeH_4, SiH_2Cl_2 and H_2 (Bodnar et al. 1997)(Hartmann et al. 2002)(Hartmann et al. 2012). **Figure V.4** shows 1x1 μm^2 AFM scans of nano-pillars grown on the 43 nm pitch mask along with nano-pillars grown on the 35 nm pitch size mask with the same process. In both cases, growth is selective and nano-pillars are clearly defined. The growth performed on the higher pitch size mask has a more uniform nano-pillars height distribution, likely due to the less extreme mask dimensions.

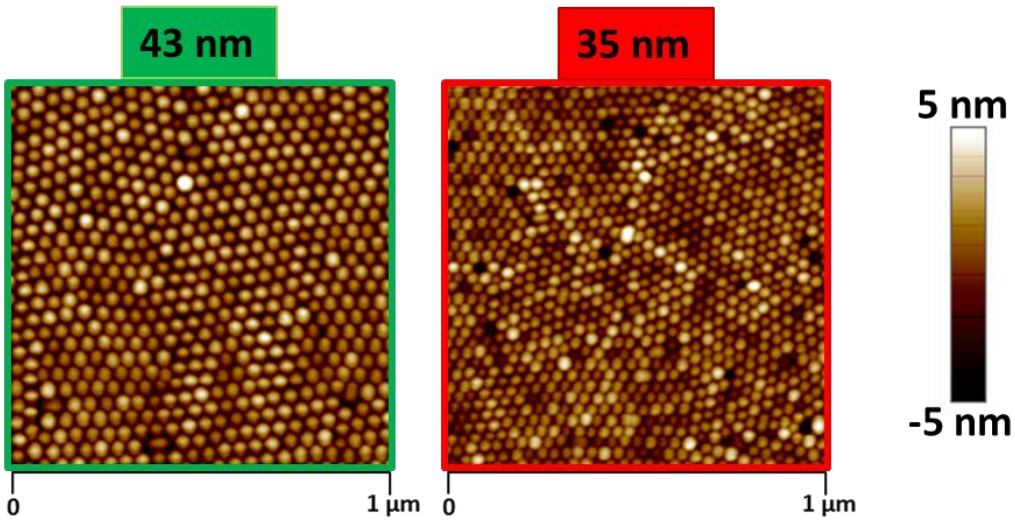

Figure V.4 1x1 μm^2 AFM scans of SiGe nano-pillars grown at 700°C on the 43 (left) and 35 (right) nm pitch size masks. AFM image sides are along the <100> directions.

After checking the validity of our selective epitaxial growth process on the 43 nm pitch mask, we performed the growth of our reference 200 nm thick SiGe 25% layer at 700°C on top of 20 nm SiGe nano-pillars selectively grown at the same temperature. **Figure V.5** shows 1x1 μm^2 AFM scans of the layers grown on different pitch size masks and the corresponding surface

Root Mean Square (RMS) roughness. The layers have a similar roughness, with the 43 nm pitch yielding a slightly improved morphology.

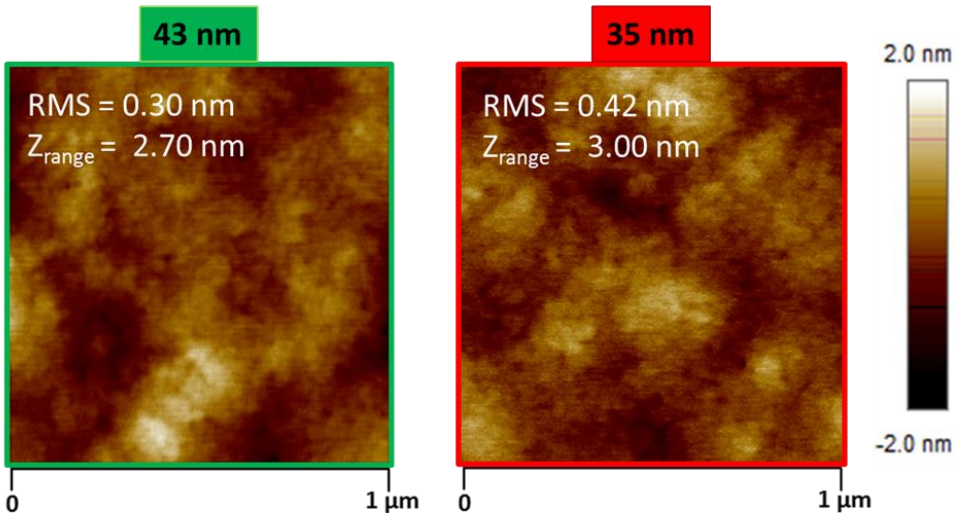

Figure V.5 1x1 µm² AFM scans of 220 nm thick $Si_{0.75}Ge_{0.25}$ layers grown on different pitch size masks and corresponding RMS roughness and Z range values. AFM image sides are along the <100> directions.

To further characterize these layers, we performed Omega-2Theta scans around the (004) and (224) orders of the samples grown on different pitch size masks. The position of the SiGe peak in those scans enabled us to extract the Ge concentration and the macroscopic degree of strain relaxation *R* of the SiGe layer given by:

$$R = \frac{a_{SiGe}^{//} - a_{Si}}{a_{SiGe}^{bulk} - a_{Si}} \qquad \textbf{E.q. V.1}$$

where $a_{SiGe}^{//}$, a_{SiGe}^{bulk} and a_{Si} were the in-plane lattice parameter of SiGe, the bulk unstrained parameter of SiGe and the Si lattice parameter, respectively. We also measured the broadening of the SiGe peak around the (004) diffraction order thanks to Omega scans. The width of the SiGe layer peak around the (004) diffraction order can be related to a density of defects. Assuming that the defects in the layer are only threading dislocations, we can use the Ayers formula (Ayers 1994), i.e.

$$\mathrm{D} = \frac{\beta^2}{4.68 b^2} \qquad \textbf{E.q. V.2}$$

to extract D, the Threading Dislocations Density (TDD) from β, the Full width at half maximum (FWHM) of the peak, b being the modulus of the Burgers vector surrounding individual dislocations. However, the angular broadening could be induced by the bending of atomic planes due to strain in the nano-pillars, therefore it was decided not to calculate defect density but to consider the FWHM as a qualitative measure of the layer quality (the lower the FWHM, the higher the quality). The Ge content, relaxation degree and peak width for the studied layers are shown data in **Table V.1**. The Ge content, is slightly higher than the targeted 25% for both layers (from blanket growth kinetics data), which is likely due to loading effects (Ito et al. 1995). The SiGe layers are also highly relaxed, which is due to nano-heteroepitaxy, with

a degree of relaxation greater than 100% due to the difference in coefficient of thermal expansion between SiGe and silicon. If we calculate the degree of relaxation at growth temperature, we find a value very close to 100% for both sizes of mask pitch. The SiGe layers grown on both the 43 nm pitch and the 35 nm pitch also have similar peak widths, and so the layer quality can be considered equivalent. Thus the increased mask pitch has little effect on the layers grown, but moving to a higher pitch size offers more flexibility in terms of surface preparation (wet surface treatment instead of NH_3/NF_3 remote plasma Siconi).

Mask pitch size (nm)	Ge concentration (%)	Degree of relaxation (%)	FWHM (arcsec)
35	25.5	111	557
43	25.9	110	619

Table V.1 Ge concentration, macroscopic degree of strain relaxation and FWHM of 220nm thick $Si_{0.75}Ge_{0.25}$ layers grown on 43 and 35 nm pitch size masks.

V.3.b. Mask removal impact

One hypothesis for the generation of defects in nano-heteroepitaxy was that this is caused by the thermal stress generated by the oxide mask during growth. This was explored with a mask free growth scheme, and later with a stress free SiN mask. For the mask free growth, the oxide mask was removed with an HF 2% based wet etching after completing the selective growth of 20 nm high SiGe nano-pillars with a targeted Ge content of 25% at 700°C. Next, our reference 200 nm thick SiGe 25% layer was grown at 700°C preceded by an in-situ H_2 bake at 850°C to remove any surface contamination (Hartmann et al. 2008)(Abbadie et al. 2004). **Figure V.6** shows different size AFM images of layers grown without an oxide mask, where we see that the surface is rough, with a z-range of 40 nm. This may be because growth is not originating solely from the SiGe nano-pillars but also from the Si substrate, or because the 850°C H_2 bake used prior to the growth of the thick SiGe layer might have roughened the starting surface (elastic strain relaxation and possibly dewetting).

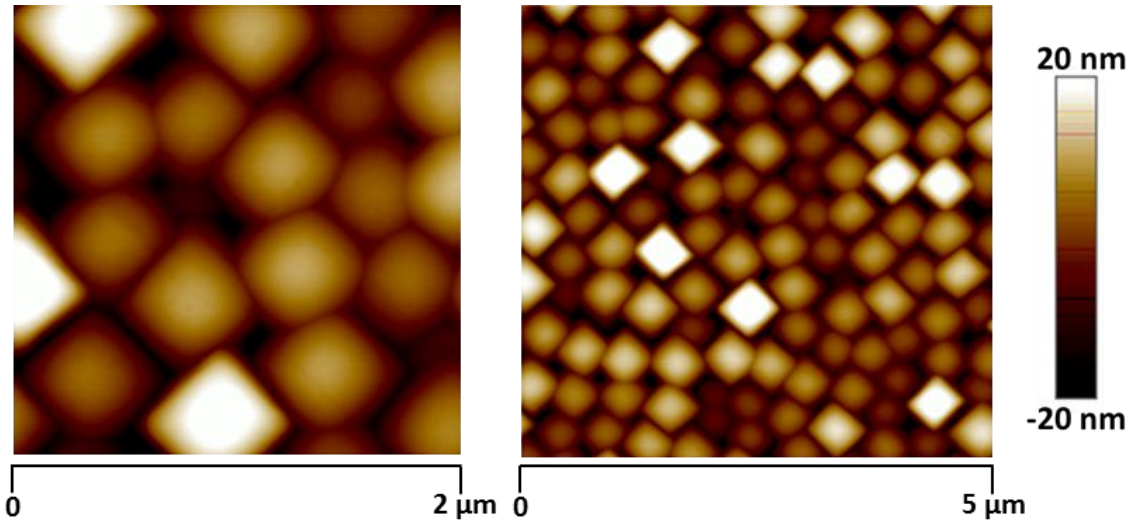

Figure V.6 2x2 and 5x5 µm² AFM scans of a 220 nm thick $Si_{0.75}Ge_{0.25}$ layer grown without mask. AFM image sides are along the <100> directions.

In order to verify these hypotheses, we examined two growth schemes:

1. Growth without mask on bulk silicon wafers in two separate steps (i.e. the wafer was taken out of the epitaxy chamber between the 20 nm and the 200 nm SiGe layer growths);
2. Growth on oxide nano-patterned mask in two steps as described just above (i.e. nano-pillar selective epitaxial growth, oxide removal, coalesced SiGe layer growth).

In addition, the 120s H_2 bake at 20 Torr performed before the second part of the growth was performed at either 700°C or 850°C. **Figure V.7, Figure V.8 and Figure V.9** show AFM scans performed on intermediate (after 20 nm growth followed by bake) and full SiGe layers (after 200 nm growth) for the various growth schemes and different bake temperatures. Z-range and RMS values extracted from the AFM scans of full SiGe layers are displayed in **Figure V.10**.

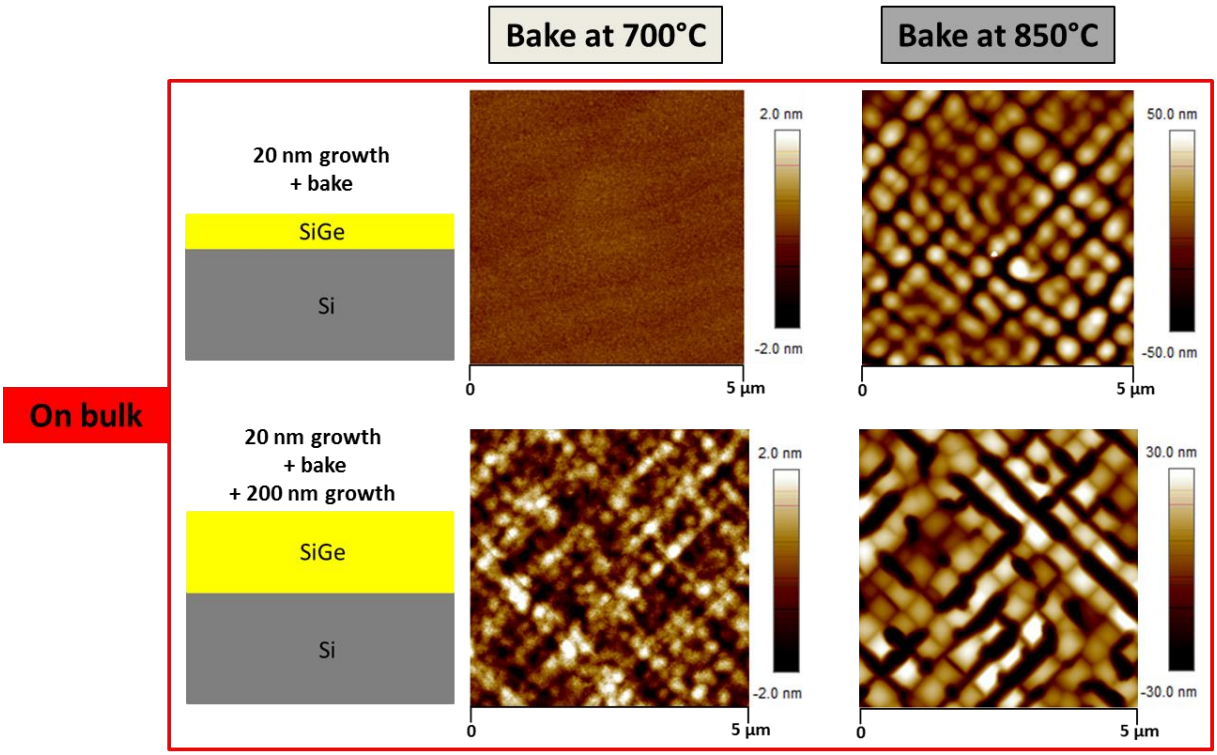

Figure V.7 AFM scans of $Si_{0.75}Ge_{0.25}$ layers grown on bulk Si at two stages: (i) after 20 nm growth then a H_2 bake and (ii) after 20 nm growth, a H_2 bake then another growth of 200nm of SiGe. Two intermediary H_2 bake temperatures were probed: 700°C and 850°C. AFM image sides are along the <100> directions.

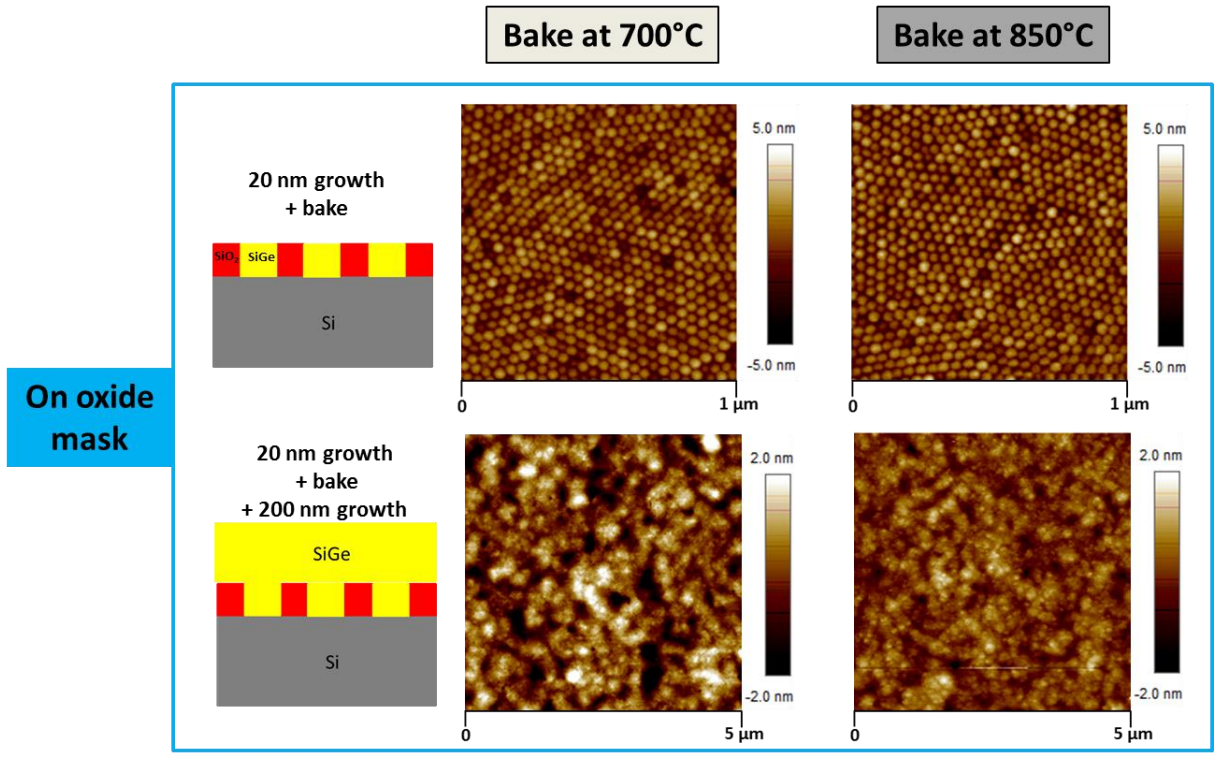

Figure V.8 AFM scans of $Si_{0.75}Ge_{0.25}$ layers grown on an oxide mask at two stages: (i) after 20 nm selective growth then a H_2 bake and (ii) after 20 nm selective growth, a H_2 bake then another growth of 200nm of SiGe. Two intermediary H_2 bake temperatures were probed: 700°C and 850°C. AFM mage sides are along the <100> directions.

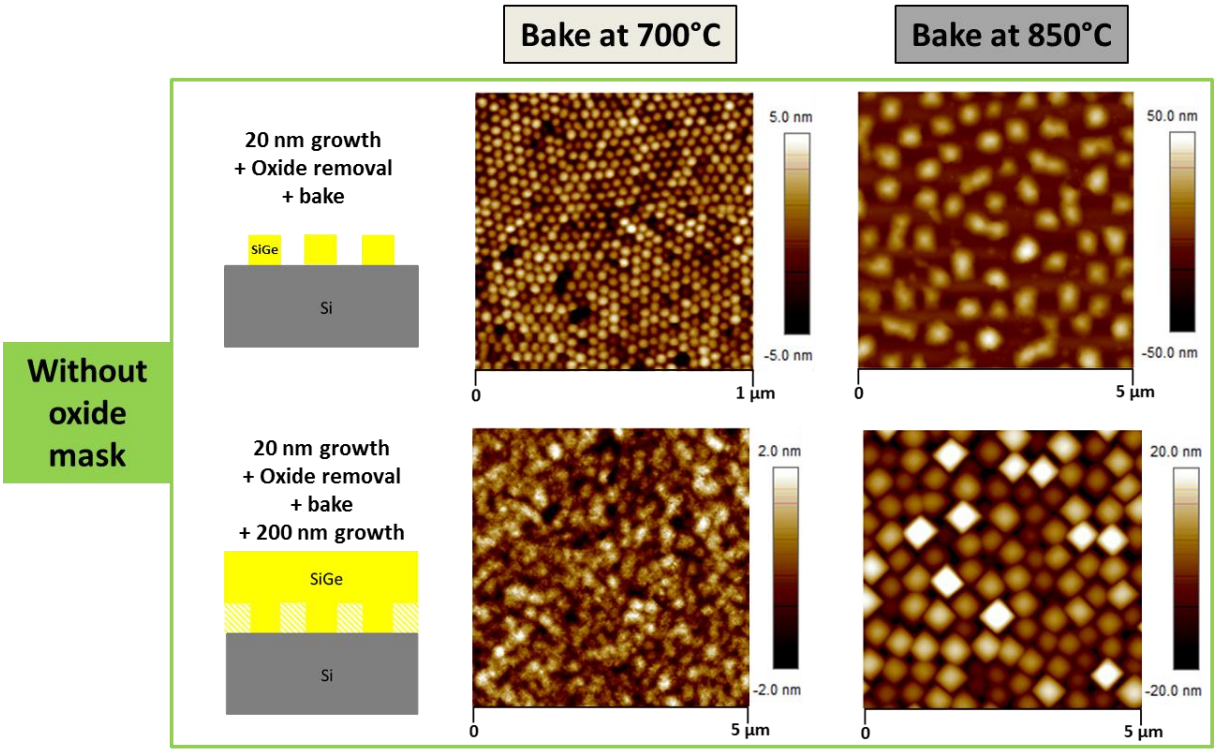

Figure V.9 AFM scans of $Si_{0.75}Ge_{0.25}$ layers grown on an oxide mask which was removed after the first epitaxy at two stages: (i) after 20 nm selective growth, the removal of the oxide mask then a H_2 bake and (ii) after 20 nm selective growth, the removal of the oxide mask, a H_2 bake then another growth of 200nm of SiGe. Two intermediary H_2 bake temperatures were probed: 700°C and 850°C.AFM mage sides are along the <100> directions.

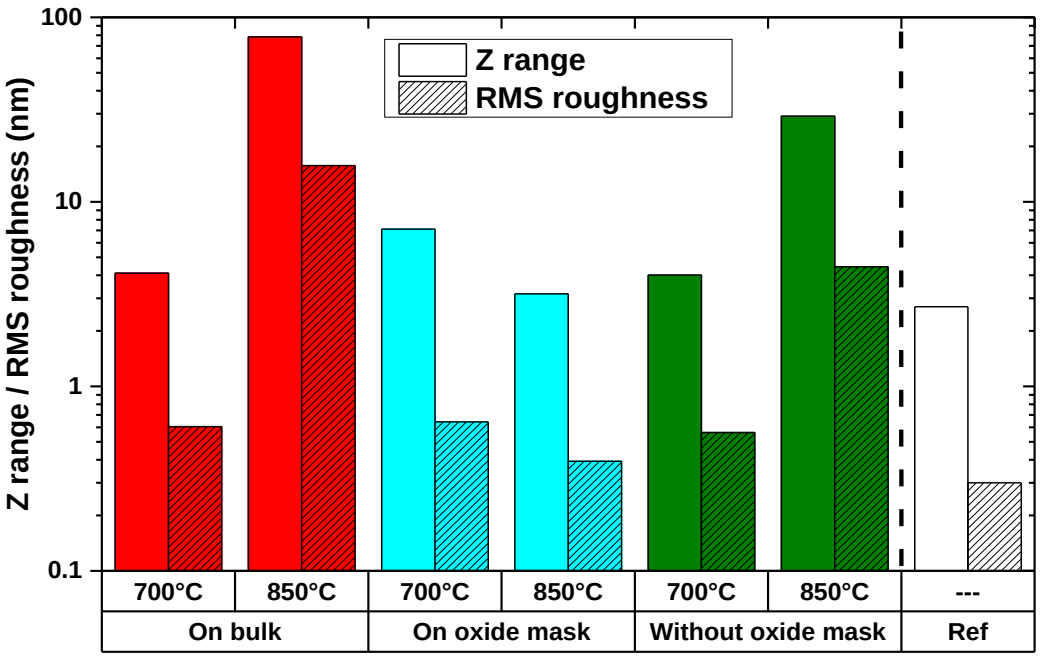

Figure V.10 Z-range and RMS values extracted from the AFM scans of full (i.e. 220 nm thick) $Si_{0.75}Ge_{0.25}$ layers.

We see that samples with a 700°C bake have very similar roughness, although growth on bulk silicon starts to show some 3D structuring on the full SiGe layers. This is logical, as we are approaching the critical thickness for elastic relaxation at that temperature (Hartmann et al. 2011). With bakes at 850°C, SiGe films grown in two steps on a blanket Si substrate or on nano-pillars with the oxide mask removed are very rough. The z-scale for these AFM images has been increased by a factor of 10 to 40-60 nm compared to the layers with a 700°C bake. This roughening is due to the coalescence of grains or an elastic relaxation of the 2D film into large <110> cubic islands prior to the resumption of growth. By contrast, growth on nano-pillars with an oxide mask results in very similar morphologies after 700°C or 850°C H_2 bakes and close to that of a same thickness layer grown in one run only ("Ref." in **Figure V.10**). The SiO_2 mask stops nano-pillars from merging into larger objects during high temperature bakes and therefore epitaxial re-growth is unaffected.

X-ray diffraction was performed on the 200 nm thick SiGe layers using triple axis Omega-2Theta scans around the (004) and (224) diffraction orders, and omega-scans around the (004) to examine the composition, strain and quality of the films, with a summary of the analyses shown in **Table V.2**. We see that there is little change in the germanium content across the samples, but there are significant changes in the peak width and the relaxation of the layers. The layers grown on nano-pillars with a SiO_2 mask have the highest levels of strain relaxation and the narrowest peak widths. With other geometries, growth is either totally or partly occurring on the bulk silicon substrate and the thick films are less relaxed. The removal of the mask therefore neither improves the quality of the layers, nor increases the relaxation and so there is no benefit to this strategy.

Growth Scheme	Bake Temperature (°C)	Ge concentration (%)	Degree of relaxation (%)	FWHM (arcsec)
On bulk	700	25	74	972
	850	23.5	72	932
On oxide mask	700	25.4	109	720
	850	25.8	108	633
Without oxide mask	700	25.6	78	936
	850	23.2	61	1022

Table V.2 Ge concentration, macroscopic degree of strain relaxation and FWHM of 220nm thick $Si_{0.76}Ge_{0.24}$ layers grown according to the various schemes explored.

V.3.c. Masking material effect

As described above, we have also tested a strain free SiN mask as SiN has a similar thermal expansion coefficient than silicon and is therefore less likely to generate defects due to thermal strain during the cooling-down of the wafer after growth (Maeda and Ikeda 1998). SiGe nano-pillars 20 nm high with a targeted Ge content of 25% were grown at 700°C with the selective epitaxial process based on GeH_4, SiH_2Cl_2 and H_2 (Bodnar et al. 1997)(Hartmann et al. 2002)(Hartmann et al. 2012) using an SiN mask with 43 nm pitch. A stronger wet surface treatment based on 2% HF diluted solution was necessary to ensure high quality growth, perhaps due to residual SiN at the bottom of the cavities. **Figure V.11** shows a 2x2 μm^2 AFM scan of the nano-pillars grown on this SiN mask, showing a regular uniform array of SiGe nano-pillars very similar to that found with a SiO_2 mask (**Figure V.4, Figure V.8 and Figure V.9**).

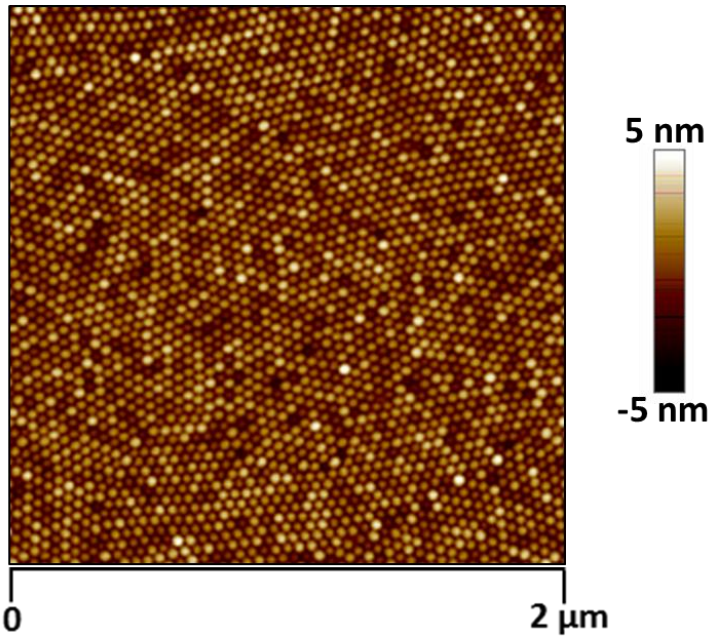

Figure V.11 2x2 µm² AFM scan of SiGe nano-pillars grown on the SiN mask. AFM mage sides are along the <100> directions.

The reference 220 nm thick SiGe 25% layer was then grown at 700°C on the SiN mask, with AFM scans shown in **Figure V.12** and XRD analysis in **Table V.3**. The AFM scans show that the layer grown on the nitride mask is slightly rougher than that grown on the oxide mask, but is otherwise very similar.

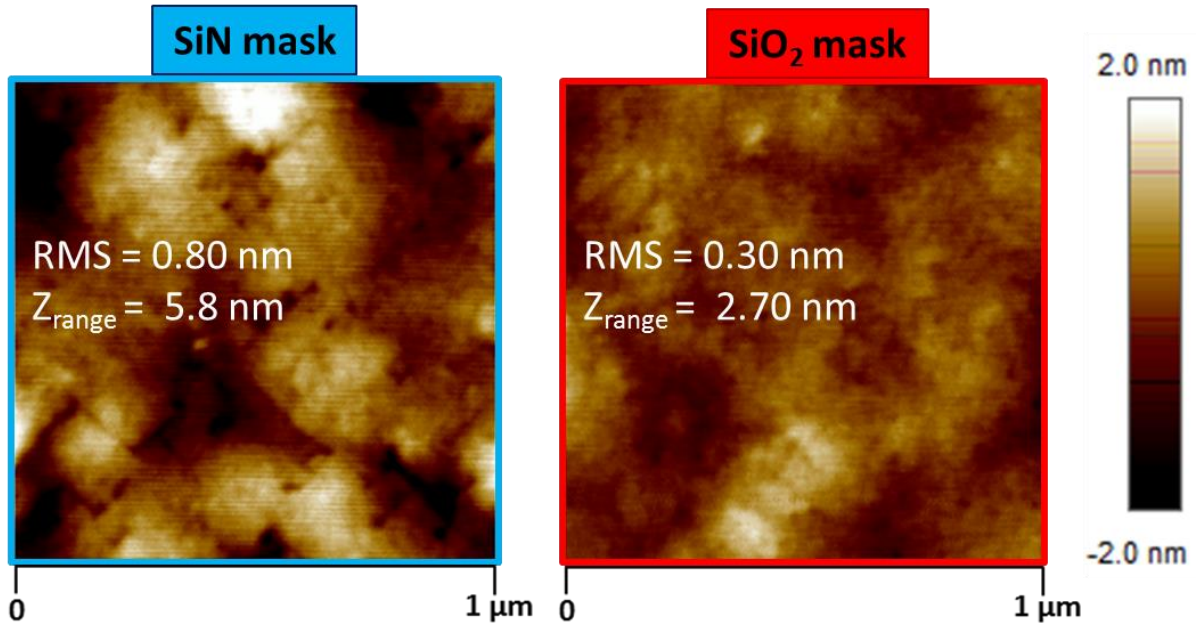

Figure V.12 1x1 µm² AFM scans of 220 nm thick $Si_{0.75}Ge_{0.25}$ layers grown on nitride and oxide masks with corresponding RMS roughness and Z range values. AFM mage sides are along the <100> directions.

XRD data on both samples are equivalent in terms of composition, strain and FWHM. The layers are neither improved nor degraded by switching to a SiN mask, and so according the integration, either could be used. These results imply that the thermal stress from cooling to room temperature using an oxide mask is not the principal effect driving the generation of defects in the nano-heteroepitaxy of SiGe layers.

Mask nature	Ge concentration (%)	Degree of relaxation (%)	FWHM (arcsec)
SiN	25.4	109	662
SiO_2	25.9	110	619

Table V.3 Ge concentration, macroscopic degree of strain relaxation and FWHM of 220 nm thick $Si_{0.75}Ge_{0.25}$ layers grown with the SiN and SiO_2 masks.

To better understand this defect generation, cross-sectional TEM observations were performed on samples with SiN and SiO_2 masks. Analysis of the TEM images in **Figure V.13** suggests that nitride walls separating nano-pillars have a shape closer to the desired integration scheme compared to the triangular shape obtained with oxide walls. The latter was due to the isotropic oxide etching during the Siconi surface preparation prior to epitaxy. Defects such as stacking faults or twins nucleating at the top of the SiN walls are comparable to defects seen with SiO_2 walls, meaning that the nature of the mask has no major impact on defects type. It also reinforces the XRD data showing that thermal stress generated by the mask during growth is not a source of defects. The TEM pictures also show that the silicon was

over etched during the SiN etching step. However, this does not affect the initial growth since no defects are visible at the interface between the Si substrate and the SiGe nano-pillars.

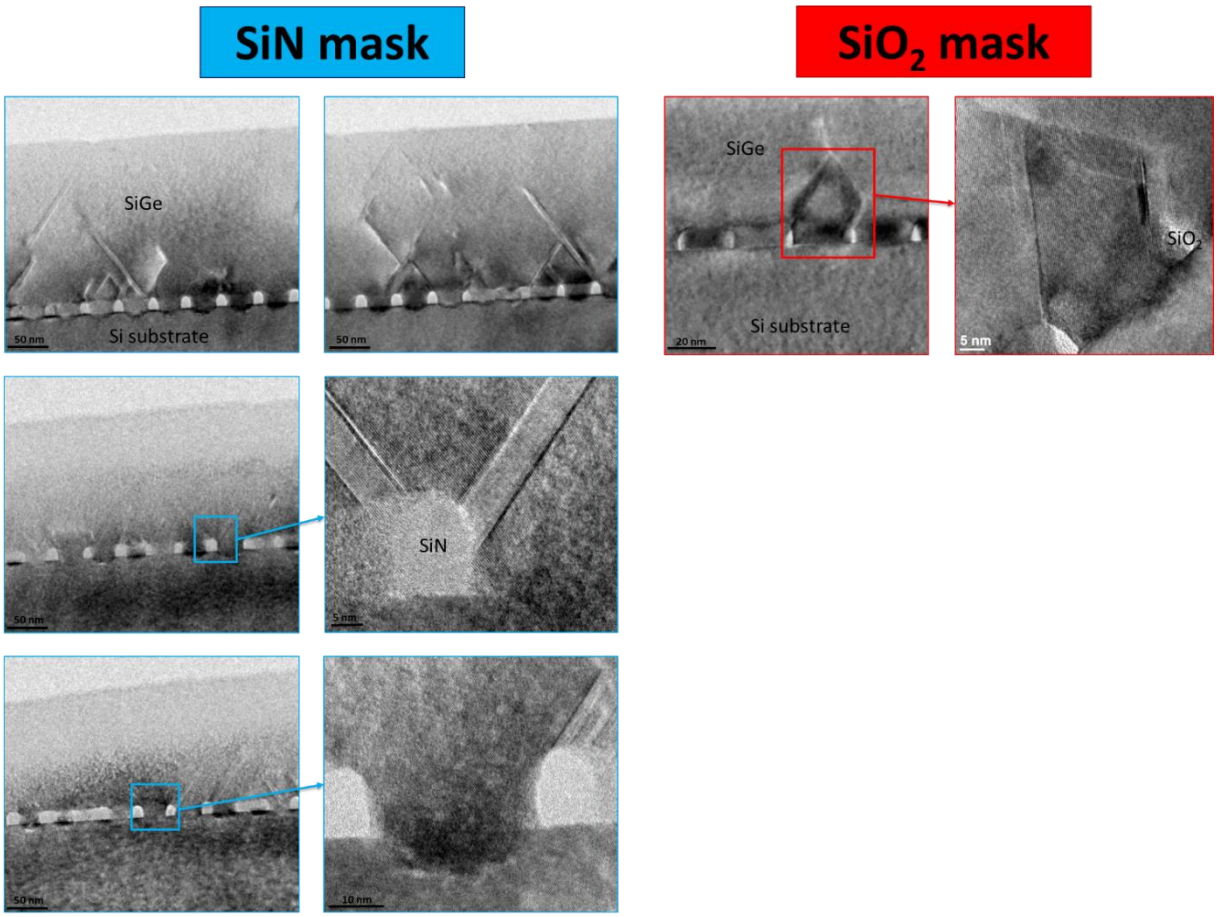

Figure V.13 Collection of high resolution cross-sectional TEM pictures of a 220 nm thick $Si_{0.75}Ge_{0.25}$ layer grown at 700°C on SiN and SiO_2 masks.

Very similar defect generation mechanisms are at play with oxide and nitride masks (from a one-to-one comparison of TEM images) which could be due to one of the following factors:

- The growth of SiGe on the {111} facets of pillars may be favorable to the formation of defects, as discussed in Ref. (Kuan and Iyer 1991).
- Defects are created during growth front coalescence above the mask

V.4. Conclusion

We have studied the impact of the mask on the nano-heteroepitaxy of SiGe layers on SiGe nano-pillars. A process flow based on diblock copolymer patterning was used in order to have a regular nanometer-size template for growth. The impact of mask pitch size on growth was

first of all investigated. A fully selective process was obtained at 700°C on the 43 nm pitch size mask with the use beforehand of a surface preparation based on a mainstream Ozone/HF wet treatment (instead of a more exotic Siconi NH_3/NF_3-based remote plasma which was mandatory for the 35 nm pitch size mask). SiGe layers on both pitch sizes were equivalent in terms of compositional and structural features. The higher pitch size mask is thus providing more flexibility in terms of surface preparation, without impacting the growth quality.

Suspecting that defect nucleation may be caused by the thermal stress generated by the presence of the oxide mask, a mask-free growth approach was also explored, along with a stress free SiN mask. First, the oxide mask was removed after the selective growth of SiGe nano-pillars, followed by the growth of a thick SiGe blanket layer with the same Ge content. Results showed a degraded surface morphology due to the 850°C bake preceding the 200 nm thick SiGe layer growth, while even with a bake at only 700°C, the layer quality was degraded, and the layers less relaxed. The removal of the mask therefore showed no benefit for our layers.

The use of a SiN mask instead of a SiO_2 one is less likely to generate defects due to strain during the cooling down of the wafer after growth due to the good matching of coefficient of thermal expansion between SiN and silicon. Selective and uniform SiGe nano-pillars were obtained on this new mask, and AFM and XRD results indicated that SiGe layer growth on this new mask was similar to the one on the oxide mask. In terms of defectivity, TEM imaging showed that the nature of the mask had no impact on defects type, proving that thermal stress generated by the mask during growth is not a source of defects. As the SiN has no effect on the growth, this could be used as an alternative integration scheme.

These results leave us with two possible mechanisms for defect generation:

- Growth on {111} facets resulting in twin formation (Kuan and Iyer 1991)
- The coalescence process itself

The studies completed so far about SiGe nano-heteroepitaxy allowed us to have a global overview on the advantages and limitations of such a technique. The defect generation mechanisms were evaluated. Defects creation at the coalescence front seem to be inherent to the process no matter the growth or mask conditions used. In chapter VI, the nano-heteroepitaxy approach is tested on a different material: pure Ge.

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CHAPTER VI:
Ge nano-heteroepitaxy

Contents of chapter VI

VI.1. Introduction

Several schemes were explored in the literature to obtain thick, good crystalline quality Ge layers, such as a low temperature/high temperature approach followed by a cyclic anneal (Hartmann et al. 2005) which yielded flat, slightly tensile strained thick Ge layers with threading dislocation densities around 10^7 cm^{-2}. Other methods based on epitaxial lateral overgrowth (Langdo et al. 2000)(Leonhardt et al. 2011), aspect ratio trapping (Ghosh et al. 2011)(Kim et al. 2014) and 3D heteroepitaxy (Salvalaglio et al. 2015)(Skibitzki et al. 2016) of Ge films on patterned Si substrates showed promising results thanks to defects blocking against sidewalls or their containment in certain directions. However, some planar defects still remained at the coalescence fronts for these growth methods. Another interesting method is to perform a heteroepitaxy of Ge in nanometer-size Si windows surrounded by SiO_2. Lee et al (Lee et al. 2007) succeeded in obtaining high quality Ge layers using nano-heteroepitaxy but did not go further in the analysis of the defects generated with that approach.

In previous studies, we were able to obtain smooth, fully strain relaxed $Si_{0.75}Ge_{0.25}$ layers with heteroepitaxial growth in nanometer-size Si windows surrounded by SiO_2 or SiN. However, planar defects such as stacking faults and twins were present in such 2D layers. In this chapter, we wanted to test this growth approach on Ge and provide an in-depth analysis of any defects generated.

An original process flow has thus been used to fabricate SiO_2 based nano-templates. The nano-heteroepitaxy of 2D Ge layers on these templates has then been investigated and compared to growth on blanket Si.

VI.2. Experimental details

VI.2.a. Nano-template features

As described in **Figure VI.1**, the substrate patterning process flow started from slightly p-type doped, nominally on-axis 300 mm bulk Si(001) wafers. A 20 nm thick thermal SiO_2 layer was grown to serve as a template for lithography. Next, a diblock copolymer patterning was performed followed by an etching step giving cylindrical cavities with ~ 20 nm diameter and ~ 23 nm spacing in a closely packed hexagonal configuration, as shown in **Figure VI.2**. An ozone wet treatment followed by a dip in HF, a rinse and finally a drying were used to prepare the surface before nano-pillar growth.

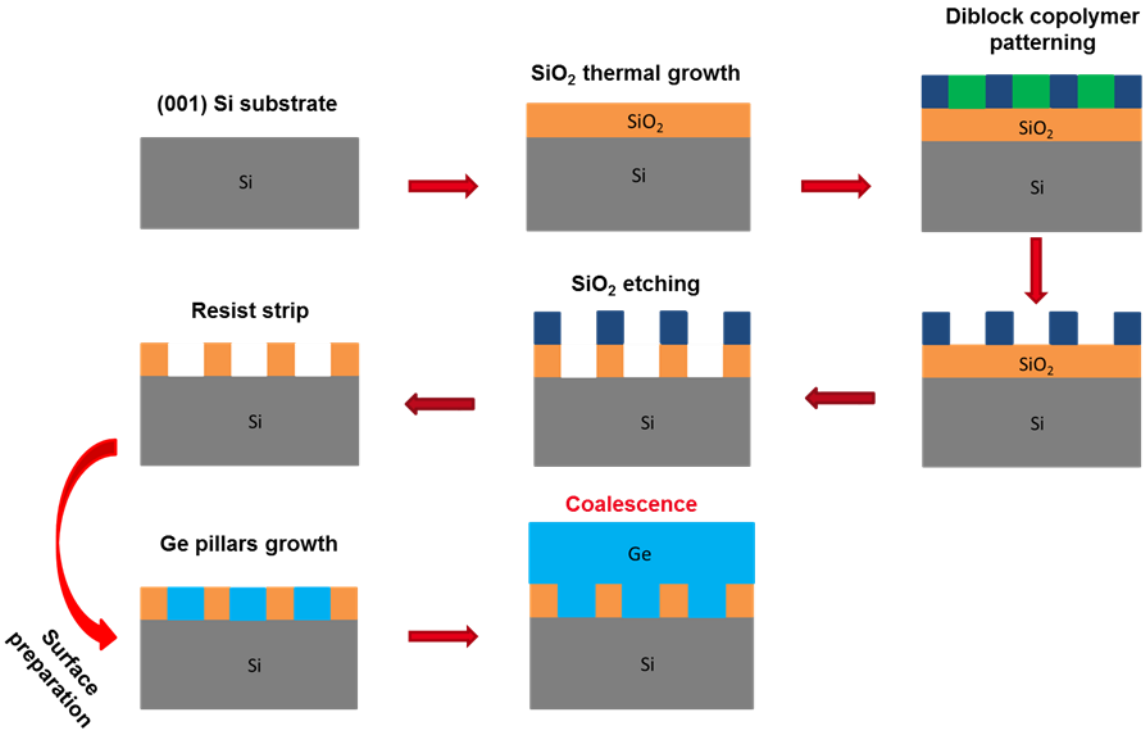

Figure VI.1 SiO_2 nano-template fabrication process flow and Ge nano-heteroepitaxy integration scheme.

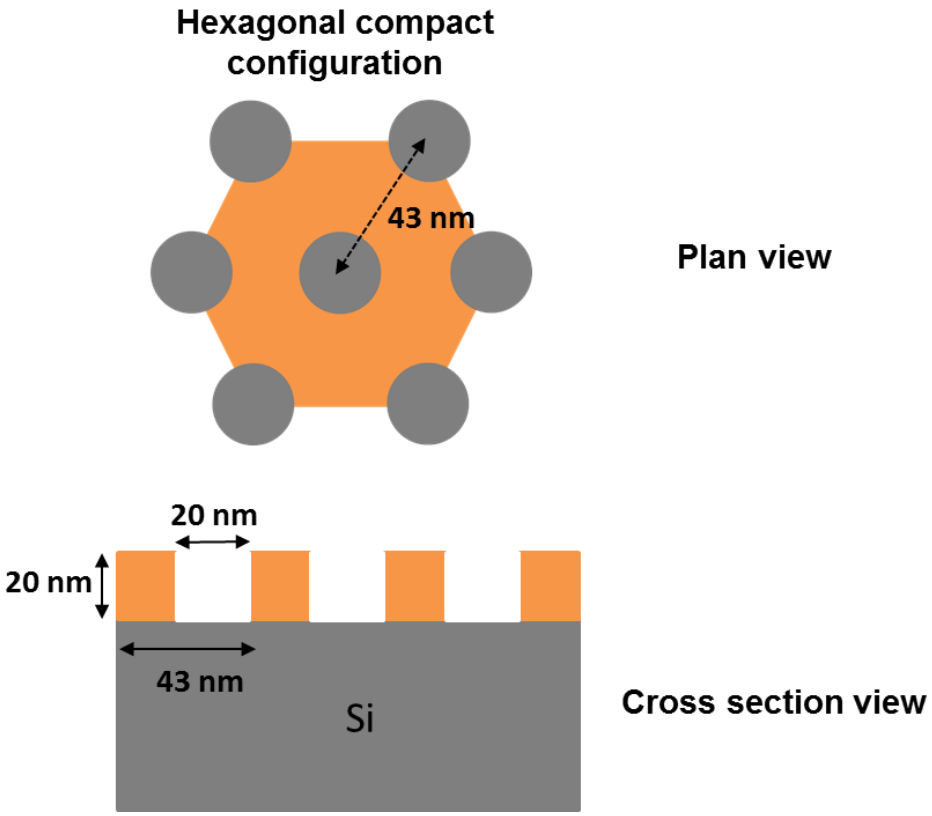

Figure VI.2 Plan view schematics of the hexagonal compact configuration defined by the diblock copolymer patterning (top) and cross sectional schematics of the oxide nano-template (bottom).

VI.2.b. Growth conditions

The growth of various thicknesses of Ge nano-pillars was explored for the validation of the growth selectivity and an evaluation of the coalescence process. Thicknesses were deduced from the growth rate of Ge layers on blanket Si (001) wafers. Thick Ge layers were then grown on bulk Si and on nano-patterned substrates to compare the two approaches. The 300 mm Epsilon 3200 Reduced Pressure – Chemical Vapour Deposition tool from ASM America was used to that end, with the growth pressure kept at 90 Torr. GeH_4 was used as the Ge gaseous precursor. The purified H_2 carrier gas flow, several tens of litres per minute, was not altered throughout the experiments. Temperatures, mole fractions and growth rates of the various processes used for Ge growth are provided in **Table VI.1**.

Growth temperature (°C)	$[GeH_4]/[H_2]$	Growth rate (nm/min)
400	0.001	10
600		78
650	0.00056	45

Table VI.1 Temperature, mole fraction and growth rate of the processes used for Ge growth (at 90 Torr with GeH_4).

VI.2.c. Sample characterization

Ge samples were characterised by X-Ray Diffraction (XRD) using a Panalytical X'Pert tool with a copper anticathode as the X-Ray source, a 4 bounce symmetric Ge(220) Bartels monochromator and wide slits in front of the detector. Macroscopic degrees of strain relaxation were extracted from conventional Omega-2Theta scans around the (004) XRD order. Tapping mode Atomic Force Microscopy (AFM) measurements were carried out on a Bruker Dimension FastScan platform. Finally, cross-sectional Transmission Electron Microscopy (TEM) carried out in a JEOL 3010 microscope operating at 300 keV. Cross-section TEM lamella were prepared using mechanical polishing followed by Ar^+ ion thinning in a Gatan ion polishing system, Pips II. This method has the great advantage to provide large areas observable in the TEM, areas obtained in a bevel way, with variable thicknesses from few nanometers near the hole, up to 100 to 300 nm. Thinnest areas are suited for high resolution electron microscopy and precise nano-pillars views, and relatively thicker zones allowed to qualify the entire Ge layer in terms of defects.

VI.3. Experimental results

VI.3.a. Ge nano-pillars

Based on early studies on the RP-CVD of Ge on bulk Si(001) (Hartmann et al. 2004)(Hartmann et al. 2005)(Hartmann et al. 2010), Ge pillars nominally 20, 25, 30, 35 and 40 nm high were grown at 400°C in the Si windows of our nm-size template. AFM images of these samples are shown in **Figure VI.3.** The growth scheme is different from that seen with SiGe nano-pillars, as no nano-pillar can be distinguished for up to 30 nm of growth, implying that there is a delay in the growth of Ge in the nano-cavities. At 35 nm, nano-pillars can be clearly identified, but they are not as homogeneous and well-defined as the previously studied 20 nm high SiGe nano-pillars. After 40 nm growth, Ge nano-pillars start to partially coalesce, with individual pillars combining to form larger islands.

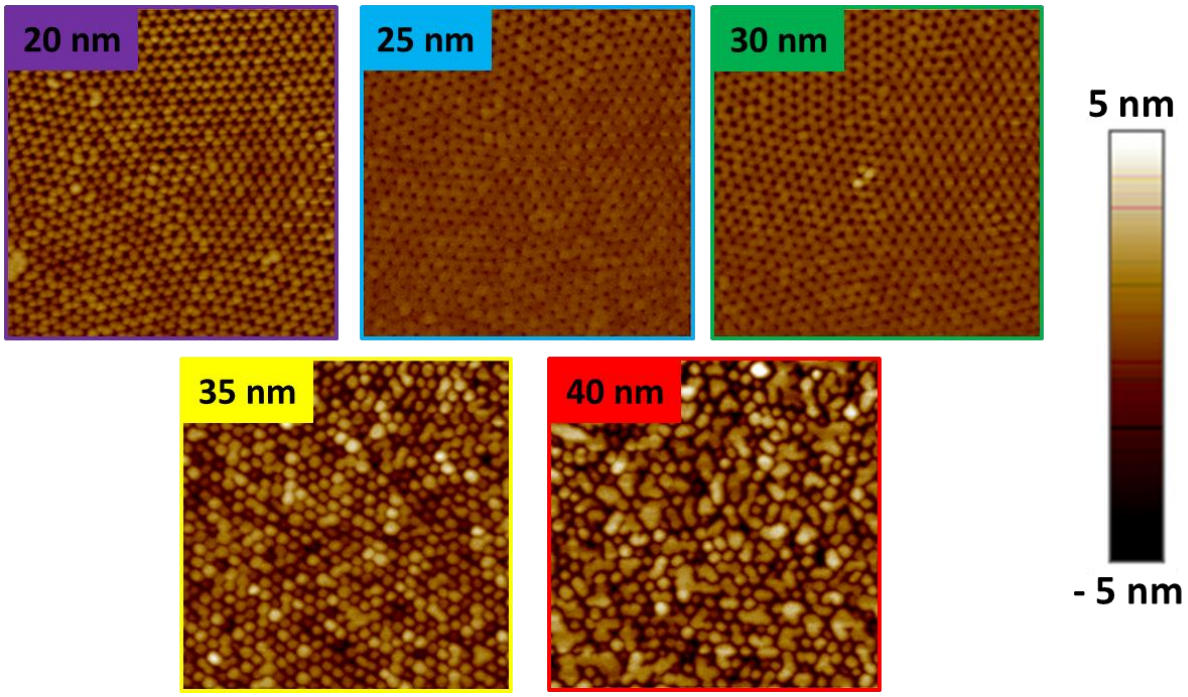

Figure VI.3 1 x 1 µm² AFM scans of Ge nano-pillars grown at 400°C with nominally 20 nm (purple), 25 nm (blue), 30 nm (green), 35 nm (yellow) and 40 nm (red) of Ge deposited. Image sides are along the <110> directions.

Samples were also analysed by XRD. Omega-2theta scans around the (004) order were used together with Bragg's law to extract the lattice parameter in the growth direction $a_{SiGe}^{\perp}$ from the angular position of the Ge peak. Knowing the relationship linking the Ge layer in-plane and perpendicular lattice parameters, we can calculate the macroscopic degree of strain relaxation R of the Ge layer, where

$$R = \frac{a_{Ge}^{//} - a_{Si}}{a_{Ge}^{bulk} - a_{Si}}$$ **E.q. VI.1**

and $a_{Ge}^{//}$, a_{Ge}^{bulk} and a_{Si} are the in-plane lattice parameter of the Ge layer, the bulk, unstrained Ge lattice parameter and the Si lattice parameter, respectively. The presence (or not) of the Ge peak and the degree of strain relaxation of the nano-pillars are given in **Table VI.2** for different nominal thicknesses. The absence of Ge peaks for samples with nominally 20, 25 and 30 nm confirms the delayed Ge growth. As expected, the samples with 35 and 40 nm of Ge are fully relaxed.

Nominal Ge thickness (nm)	Ge XRD peak	Degree of strain relaxation (%)
20	No	-
25	No	-
30	No	-
35	Yes	97
40	Yes	98

Table VI.2 XRD results for Ge nano-pillar samples grown at 400°C.

In order to achieve homogeneous and well defined Ge nano-pillars at 20 nm (as for SiGe nano-pillars), we increased the growth temperature from 400°C to 600°C and grew nano-pillars with nominally 20, 30 and 40 nm of Ge. The AFM scans of these samples in **Figure VI.4** show that the 20 nm Ge nano-pillars are well ordered and homogeneous in terms of height and diameter. For the other samples, a similar coalescence to that seen with SiGe occurs, with a few nano-pillars starting to coalesce with their neighbours at 30 nm, resulting in some randomly located nano-pillars with a higher diameter. For 40 nm growth, all the initial nano-pillars have coalesced and the agglomerates have various shapes and sizes.

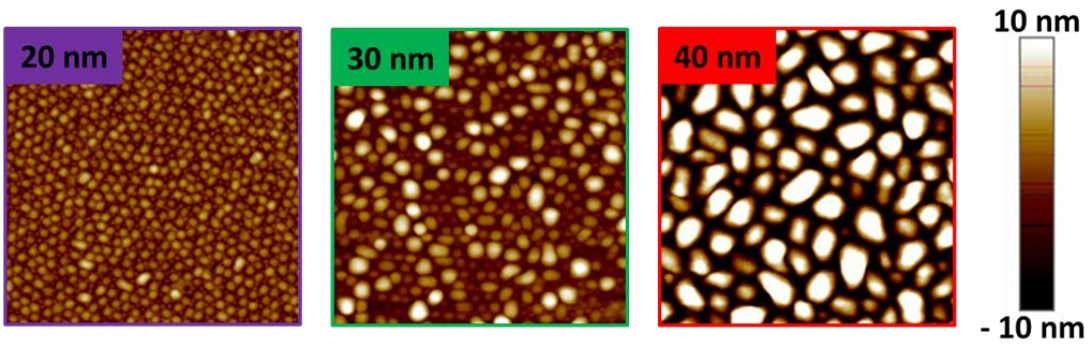

Figure VI.4 1 x 1 µm² AFM scans of Ge nano-pillars grown at 600°C with nominally 20 nm (purple), 30 nm (green) and 40 nm (red) of Ge deposited. Image sides are along the <110> directions.

Omega-2Theta scans around the (004) diffraction order for the 3 samples are shown in **Figure VI.5.**

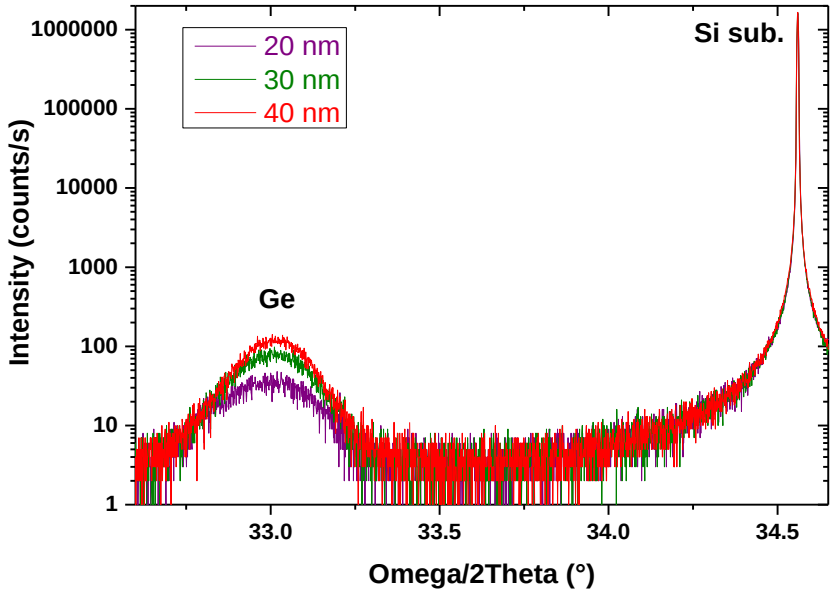

Figure VI.5 Omega-2Theta scans around the (004) XRD order for the 20 nm (purple), 30 nm (green) and 40 nm (red) samples.

We find from XRD that all the samples are fully relaxed, with a slight tensile strain starting at 30 nm, as listed in **Table VI.3**. This is probably related to the difference in thermal expansion coefficient between Si and Ge, which will add strain during the cool-down to room temperature after growth (Hartmann et al. 2004).

Thickness (nm)	Degree of strain relaxation (%)
20	100
30	101
40	101

Table VI.3 XRD results for Ge nano-pillar samples grown at 600°C.

Cross-sectional TEM observations were performed on the 20 nm high Ge nano-pillars grown at 600°C to have more insight about their structural properties. **Figure VI.6** shows high resolution TEM images of Ge nano-pillars at 20 nm nominal thickness where we see faceting which is specific to Ge selective epitaxial growth (Park et al. 2008), with {113} facets clearly visible on top of the nano-pillars. Unlike SiGe nano-pillars, some of the Ge nano-pillars show some extended defects starting at the interface with the Si substrate. The periodic contrast in the interface between the Ge nano-pillars and the Si substrate is likely due to a regular array

of 90° edge dislocations. This is expected, as the critical thickness of Ge on silicon is very low (4 nm, typically), and the pillars are too large to accommodate all the strain without generating misfit dislocations (Luryi and Suhir 1986). There is a dark spot, and thus an edge type dislocation every 10 nm, which is also seen for the growth of germanium on blanket silicon (Hartmann et al. 2004).

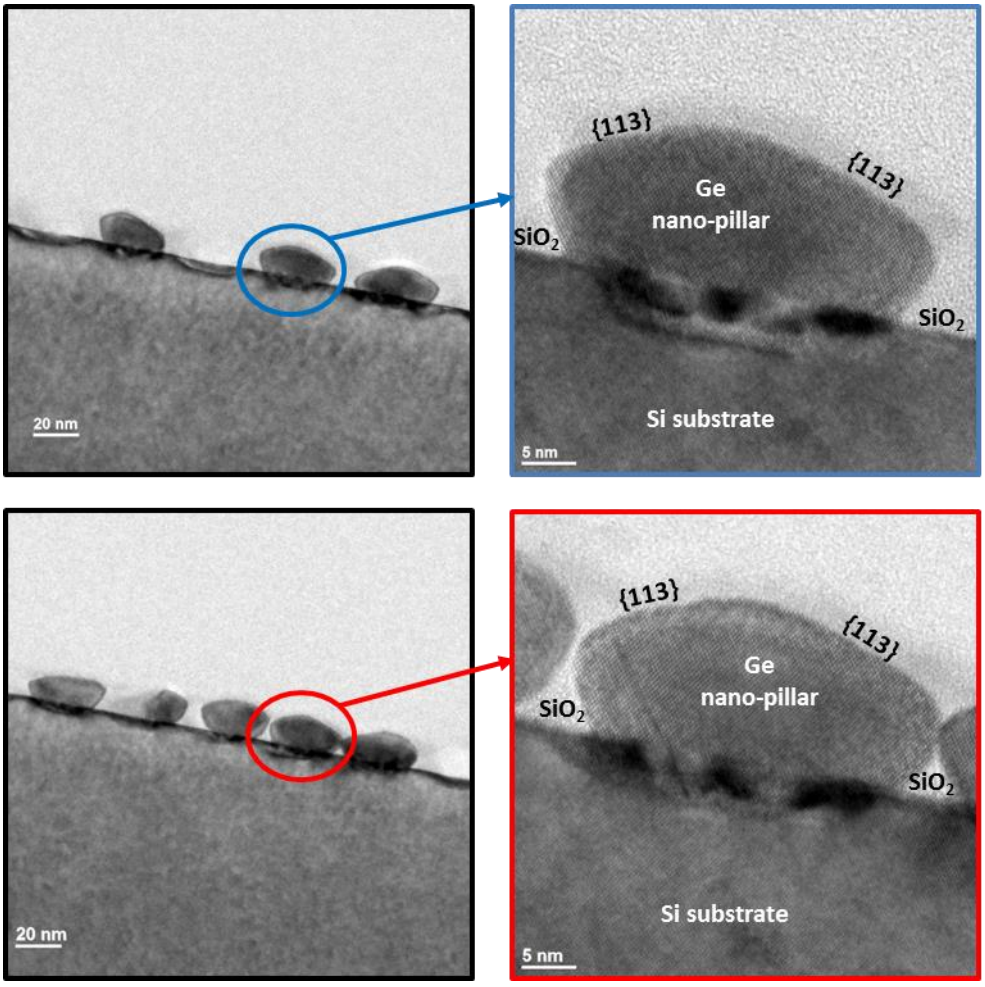

Figure VI.6 High resolution TEM pictures of 20 nm high Ge nano-pillars grown at 600°C

VI.3.b Ge thick coalesced layers

Using a low temperature/high temperature strategy (which is the most widely used method for the epitaxy of Ge layers on bulk Si(001)), we have grown Ge layers 600, 1050 and 1500 nm thick on nano-patterned and bulk Si(001) substrates. The process started with the growth of 150 nm at 400°C followed by a 10 s thermal anneal at 750°C for surface smoothening. The low temperature step is at 400°C despite the delay seen for nano-pillar growth. This choice was made for several reasons :(i) 400°C is the temperature typically used on blanket wafers, (ii) we were not really concerned by the growth delay seen above, as we grew a nominal thickness of 150 nm of Ge, and (iii) Ge nano-pillars were uniform for 35 nm of

Ge and started to coalesce properly after 40 nm of growth (bottom image of **Figure VI.3**). The remainder of the Ge layer was grown at 650°C followed by three thermal cycles (under H_2). Each cycle consisted of a 10 s anneal at 850°C followed by a ramping-down to 650°C, a 10 s step at 650°C and a ramping-up to 850°C. This thermal cycling typically reduces the threading dislocations density in the Ge layer by a factor of 3 to 5.

Figure VI.7 shows AFM scans of the samples, where we see that the Ge layers grown on bulk Si(001) substrates are much smoother than those grown on nano-patterned substrates (the z-scale is very different between the two sets of samples). It seems that the thick Ge layers grown on nano-cavities have not completely coalesced yet, with the presence of micrometric-size holes.

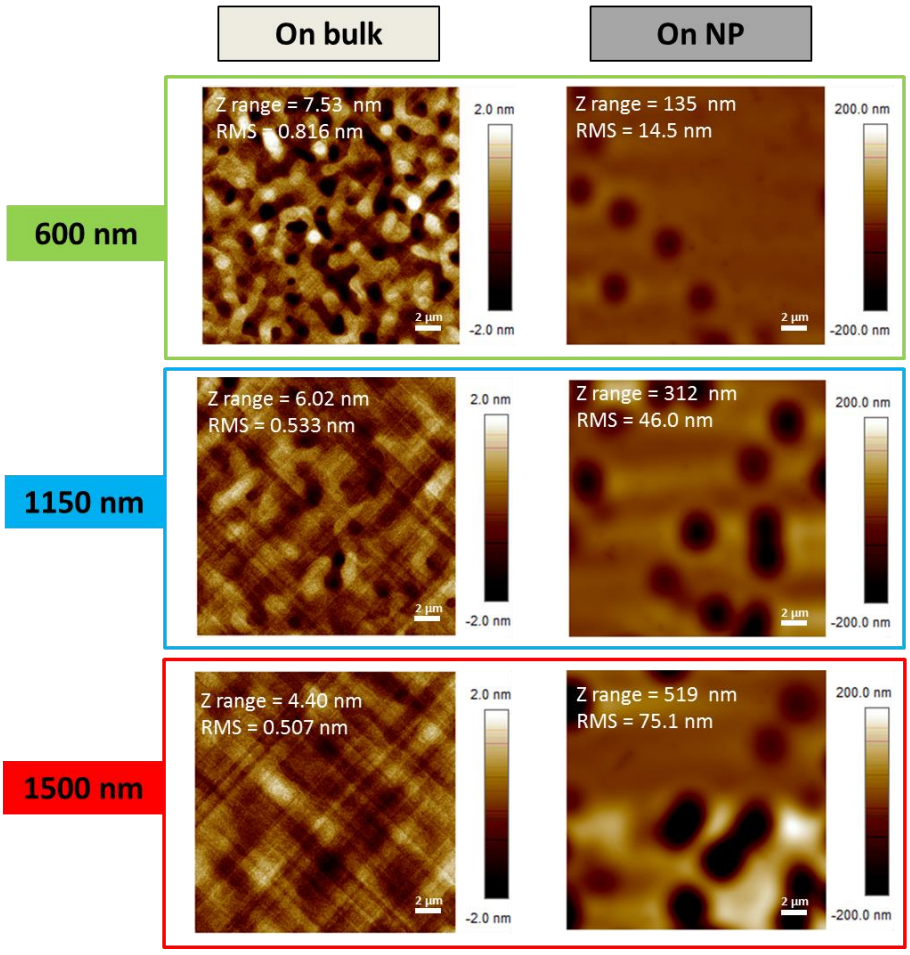

Figure VI.7 20 x 20 µm² AFM scans of 600, 1150 and 1500 nm thick Ge layers grown on bulk and nano-patterned (NP) substrates. Image sides are along the <100> directions.

We measured the width of the Ge (004) reflection by XRD along the in-plane direction (i.e. q_x), which can be related to a density of defects. If we assume that the defects in the layer are only threading dislocations, we can use the Ayers' formula (Ayers 1994), i.e.

$$D = \frac{\beta^2}{4.68 b^2} \qquad \textbf{E.q. VI.2}$$

to extract D, the Threading Dislocations Density (TDD) from β, the Full width at half maximum (FWHM) of spots in the q_x direction, b being the modulus of the Burgers vector surrounding individual dislocations. However, angular broadening may be induced by the bending of atomic planes due to strain in the nano-pillars, and thus, it was decided not to calculate defect density but to consider the FWHM as a qualitative measure of the layer quality. Omega-2Theta scans around the (004) diffraction order for all the samples are shown in **Figure VI.8** and Omega scans centred on the Ge peak around the (004) diffraction order for all the samples are shown in **Figure VI.9**.

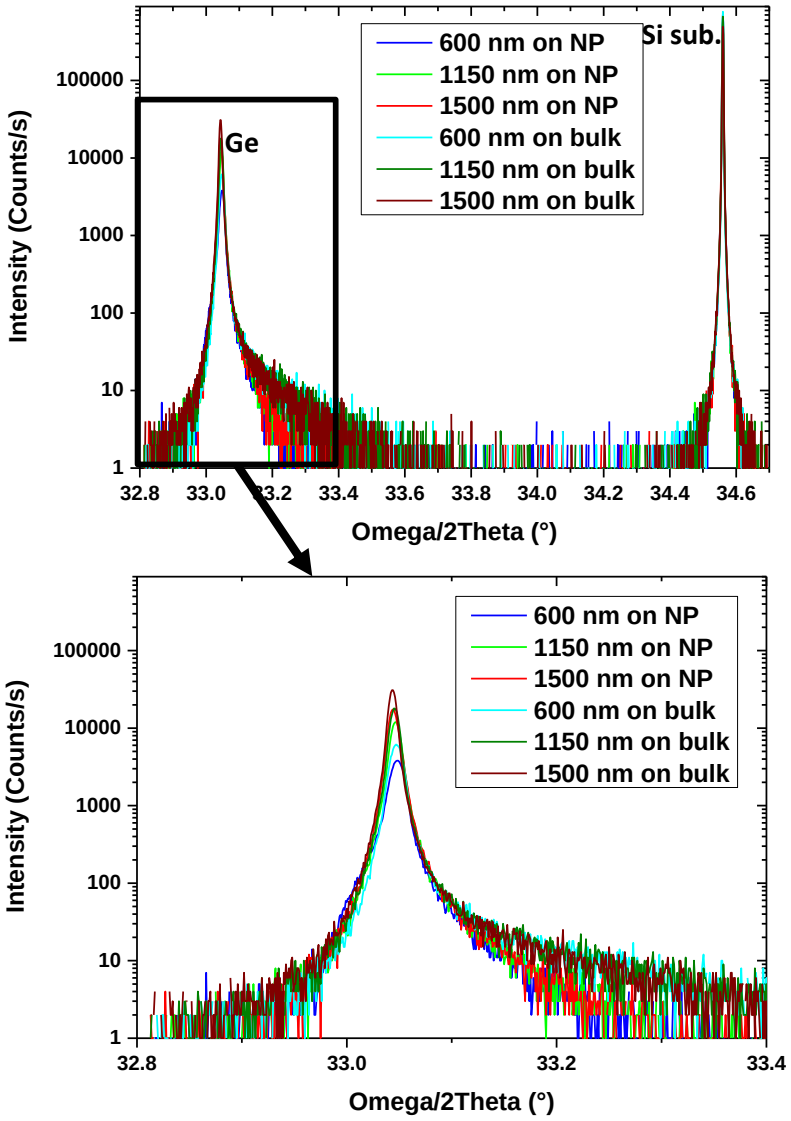

Figure VI.8 Omega-2Theta scans around the (004) XRD order for the 600, 1150 and 1500 nm Ge samples grown on bulk and nano-patterned substrates.

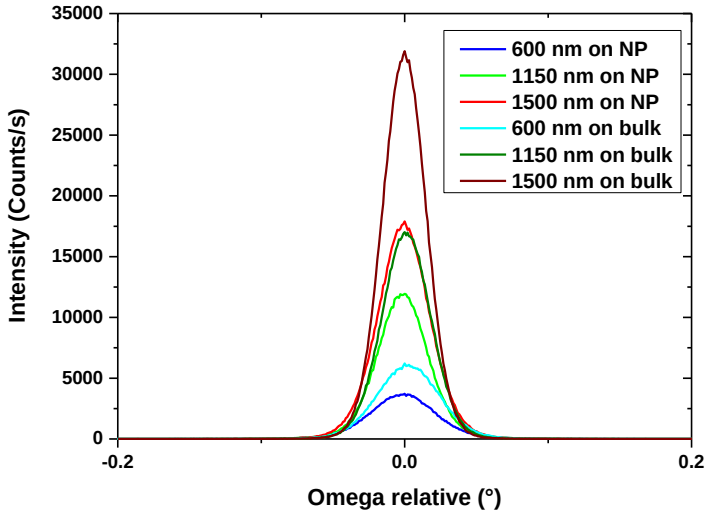

Figure VI.9 Omega scans around the (004) XRD order Ge peak for the 600, 1150 and 1500 nm Ge samples grown on bulk and nano-patterned substrates.

The relaxation degree and FWHM of the layers at different thicknesses are given in **Table VI.4**. Ge layers grown on bulk and nano-patterned substrates have similar relaxation degrees and FWHM. This suggests that, in contrast to SiGe layers, the defect density is dominated by the generation of edge type dislocations at the silicon-germanium interface, with no clear impact of the coalescence process itself.

Thickness (nm)	Wafer type	Degree of strain relaxation (%)	FWHM (arcsec)
600	Bulk	104	183
	NP	105	190
1050	Bulk	104	143
	NP	104	149
1500	Bulk	104	128
	NP	104	152

Table VI.4 XRD results for 600, 1150 and 1500 nm thick Ge layers grown with a low temperature/high temperature approach on bulk Si(001) and nano-patterned (NP) substrates.

Cross-sectional TEM observations were performed on the 600 nm coalesced Ge layer in order to evaluate the defect generation mechanisms. Analysis of the TEM images in **Figure VI.10** suggests that Ge coalescence results in the same type of defects (twins and stacking faults) starting at the top (purple frame) and edges (red frame) of the oxide walls as well as the interface between the Si substrate and the Ge layer (blue frame). This is quite similar to what

was obtained for SiGe, but these defects do not have a significant effect on the XRD FWHM, perhaps due to easier recombination of defects in Ge versus SiGe.

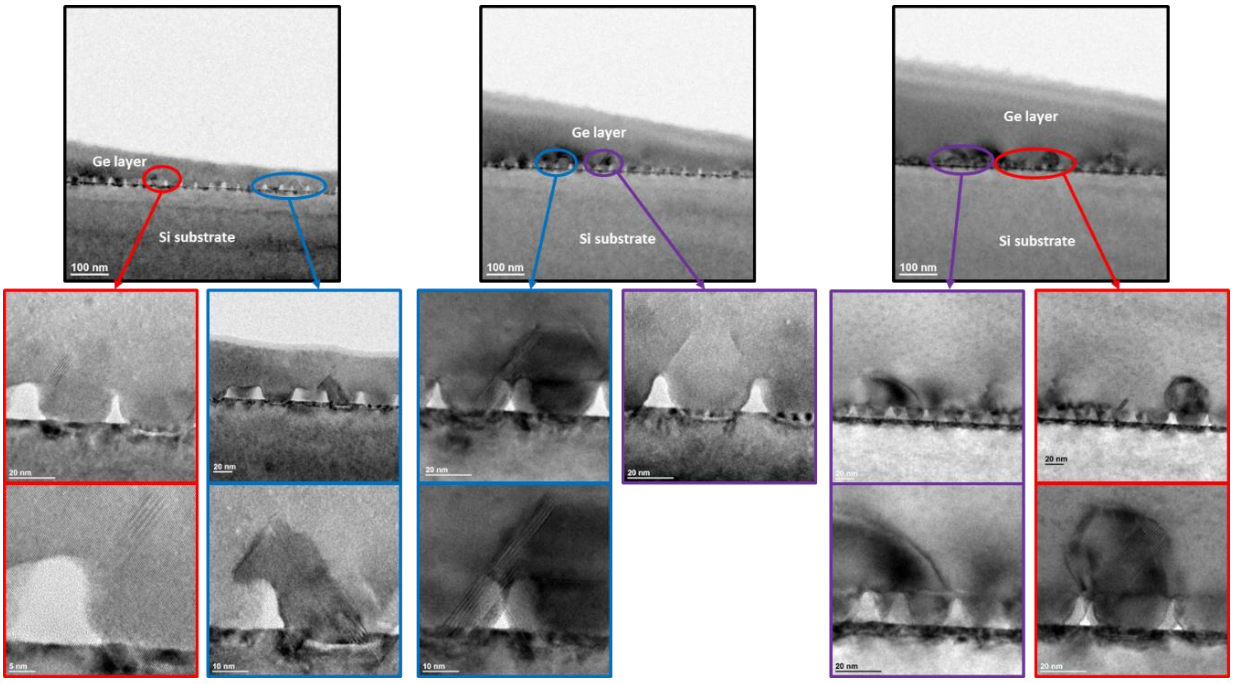

Figure VI.10 High resolution TEM images of a 600 nm thick coalesced Ge layer.

VI.4. Conclusion

We have studied the epitaxy of Ge layers on Ge nano-pillars (grown themselves on Si(001)) using a process flow based on diblock copolymer patterning in order to have a fairly regular nanometer-size oxide template for growth. Ge nano-pillars growth was first investigated, with a delayed Ge growth found at 400°C. Nano-pillars obtained after the growth of 35 nm of Ge were not as homogeneous and well-defined as the 20 nm high SiGe nano-pillars investigated previously. Raising the growth temperature to 600°C yielded a highly selective and uniform process, with homogeneous and well defined Ge nano-pillars for a nominal growth thickness of 20 nm. The expected nano-pillar coalescence scheme was also observed at this growth temperature. TEM imaging of the 20 nm sample grown at 600°C showed facetted Ge nano-pillars, with numerous 90° edge dislocations at the Ge/Si interface as expected given the low critical thickness of Ge on silicon (4 nm, typically) and the 20 nm nano-pillar width.

Ge thick layers were then grown with a low temperature/high temperature strategy on bulk and nano-patterned substrates for a benchmark of the nano-heteroepitaxy approach. AFM showed micrometric-size holes at the surface for the Ge layers grown on nano-patterned substrates which might be due to an incomplete coalescence of the thick Ge layers, while the Ge layers on silicon were very smooth. TEM analysis of a 600 nm thick Ge layer grown on Ge nano-pillars suggests that coalescence results in planar defects such as twins and stacking faults starting at the oxide walls, as found for SiGe pillars in previous studies, in addition to edge dislocations at the Ge/Si interface. Despite these morphological differences, similar structural properties (in terms of degree of strain relaxation and Full Width at Half Maximum

of the Ge spot along the in-plane direction) were inferred from XRD for layers grown on nano-patterned and bulk substrates.

VI.5. Bibliography of Chapter VI

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General conclusion

SiGe nano-heteroepitaxy, a new growth approach based on selective epitaxy on nano-patterned substrates have been explored in this PhD thesis. The context of this work being strained silicon-on-insulator technology, the main idea was to grow a SiGe virtual substrate using a method that offers additional degrees of strain relaxation compared with classical approaches such as linear graded buffer strategies. The first step towards SiGe nano-heteroepitaxy consisted in optimizing a nano-template fabrication scheme based on diblock copolymer patterning. Using an industrial Reduced-Pressure Chemical Vapor Deposition tool, SiGe nano-heteroepitaxy growth on these templates was then explored.

We first studied the nano-heteroepitaxy of SiGe layers on Si and SiGe nano-pillars. Diblock copolymer patterning was used to have a fairly regular nanometer-size oxide template for growth. The selective epitaxy of Si nano-pillars was first investigated. A fully selective and homogeneous process in terms of height was obtained thanks to NH_3/NF_3-based remote plasma preparation, beforehand. For SiGe, the same high quality of nano-pillars was achieved for temperatures between 650°C and 700°C. In-plane (220) and (224) RSM showed fringes which were characteristic of the geometrical configuration of the nano-template, showing that the mask was highly oriented and of good quality. Smooth surfaces and high degrees of strain relaxation were obtained in the 650-700°C temperature range for SiGe layers. However, XRD and TEM characterization showed that the SiGe layers had defects. The use of SiGe instead of Si nano-pillars resulted in higher quality layers, notably when growth was conducted at 700°C. TEM imaging showed that planar defects such as stacking faults and twins typically occurred at the interface between pillars and bulk SiGe, above the SiO_2 mask. Three hypotheses were made concerning such defect generation: (i) growth on Si{111} facets resulting in twin formation (ii) the coalescence process itself (iii) thermal stress generated by the oxide mask during growth which may have caused defect generation.

We have then investigated SiGe nano-pillars coalescence at the early growth stages to evaluate previous hypotheses. $Si_{0.75}Ge_{0.25}$ nano-pillars 20 to 35 nm high were selectively grown with a chlorinated chemistry. SiGe nano-pillars merging was first examined with AFM and the evolution in terms of grain shape, number and diameter was tracked. Starting at 30 nm, grains took various shapes depending on the number of merging nano-pillars, making the coalescence process heterogeneous. As expected, the average grain size increased and the number of grains decreased as the deposited thickness increased. A plot of the coalescence degree (i.e. the inverse of the number of grains) as a function of thickness enabled us to predict full coalescence at ~80 nm. Using XRD, we found that relaxation increased with the thickness, reaching a value as high as 91% for 35 nm thick, partly coalesced pillars, confirming that growth from nano-cavities resulted in a very fast relaxation. There was no change in chemical composition across this range of thicknesses. SSRM demonstrated a good sensitivity concerning the electrical activity of the nano-pillars. At 20 nm, the electrical distinction between nano-pillars and the oxide mask was straightforward and the electrical resistance of

those pillars was very uniform. At 35 nm, we detected local resistivity variations within coalescing nano-pillars, which may be due to different electrical behaviour of structural defects. Finally, TEM was used to investigate structural defect generation during coalescence. TEM imaging of the 20 nm sample showed facetted and defect free nano-pillars. The analysis of the 35 nm samples showed various cases ranging from defect free nano-pillars merging to the generation of stacking faults and twinning at the early stages of coalescence

We also analysed the impact of the mask on the nano-heteroepitaxy of SiGe layers on SiGe nano-pillars. The impact of mask pitch size on growth was first of all investigated. A fully selective process was obtained at 700°C on a 43 nm pitch size mask with surface preparation before growth based on a mainstream Ozone/HF wet treatment (instead of a more exotic Siconi NH_3/NF_3-based remote plasma which was mandatory for a 35 nm pitch size mask). SiGe layers on both pitch sizes were equivalent in terms of compositional and structural features. The larger pitch size mask therefore provided more flexibility in terms of surface preparation, without impacting the growth quality. Suspecting that defect nucleation may be caused by the thermal stress generated by the presence of the oxide mask, a mask-free growth approach was also explored, along with a stress free SiN mask. First, the oxide mask was removed after the selective growth of SiGe nano-pillars, followed by the growth of a thick SiGe blanket layer with the same Ge content. Results showed a degraded surface morphology due to the 850°C H_2 bake preceding the 200 nm thick SiGe layer growth (at 700°C). Even with a bake at only 700°C, the layer quality was degraded, and layers less relaxed. The removal of the mask therefore showed no benefit for our layers. The use of a SiN for the mask instead of SiO_2 was less likely to generate defects due to strain during the cooling down of the wafer after growth due to the good matching of the coefficients of thermal expansion between SiN and silicon. Selective and uniform SiGe nano-pillars were obtained on this new mask, and AFM and XRD measurements indicated that SiGe layer growth on this new mask was similar to the one on the oxide mask. In terms of defectivity, TEM imaging showed that the nature of the mask had no clear impact on defect type, proving that thermal stress generated by the mask during growth was not the main source of defects. As the SiN has no effect on the growth, this could be used as an alternative integration scheme. These results leave us with two possible mechanisms for defect generation: (i) growth on {111} facets resulting in twin formation and (ii) the coalescence process itself.

Finally the nano-heteroepitaxy approach was tested on pure Ge. Ge nano-pillars growth was first investigated, with a delayed Ge growth found at 400°C. Nano-pillars obtained after the growth of 35 nm of Ge were not as homogeneous and well-defined as the 20 nm high SiGe nano-pillars previously investigated. Raising the growth temperature to 600°C yielded a highly selective and uniform process, with homogeneous and well defined Ge nano-pillars for a nominal growth thickness of 20 nm. The expected nano-pillar coalescence scheme was also observed at this growth temperature. TEM imaging of the 20 nm sample grown at 600°C showed facetted Ge nano-pillars, with numerous 90° edge dislocations at the Ge/Si interface. Ge thick layers were then grown with a low temperature/high temperature strategy on bulk and nano-patterned substrates for a benchmark of the nano-heteroepitaxy approach. AFM showed micrometric-size holes at the surface for Ge layers grown on nano-patterned substrates which might be due to an incomplete coalescence of the thick Ge layers, while the

Ge layers on silicon were very smooth. TEM analysis of a 600 nm thick Ge layer grown on Ge nano-pillars suggested that coalescence resulted in planar defects such as twins and stacking faults starting at the oxide walls (as for SiGe pillars in previous studies), in addition to edge dislocations at the Ge/Si interface. Despite these morphological differences, similar structural properties (in terms of degree of strain relaxation and Full Width at Half Maximum of the Ge spot along the in-plane direction) were inferred from XRD for layers grown on nano-patterned and bulk substrates.

As targeted during this PhD thesis, the nano-heteroepitaxy approach is interesting in order to obtain smooth surfaces and fast relaxations on not so highly mismatched materials such as SiGe 25% on Si. No misfit dislocations were generated in SiGe nano-pillars thanks to elastic strain relaxation allowed by the three-dimensional localized growth. Yet, planar defects such as stacking faults and twins are inherently generated at the coalescence fronts. The prospect of a defect free growth could be therefore imagined in a scheme where the coalescence is very well-controlled. On the other hand, integration of highly mismatched materials such as Ge and GaAs with this approach would necessitate first to redesign the nano-template with much more aggressive dimensions in order to meet the theoretical requirements for nano-pillars elastic strain relaxation.

In view of these conclusions, a major perspective is to improve the quality of SiGe layers grown by nano-heteroepitaxy. Several strategies could be explored in order to reduce coalescence related planar defects.

One could think of an alternative growth process with a higher temperature and HCl chemistry. The higher temperature is motivated by the fact that a higher atom mobility would be expected to improve matter distribution between nano-pillars and facilitate high quality pillar merging. HCl could be added in order to have a slower and more controllable coalescence process, through a preferential etching of defects. This path was actually explored and no significant benefits were evidenced.

Laser annealing seems to be a promising method for defects curing. This is why a study based on Ultraviolet Nanosecond Laser Annealing (UV-NLA, XeCl laser, 308 nm wavelength, 145 ns FWHM pulse duration) was initiated on SiGe layers grown on nano-patterned substrates to see if there was any impact on defects. Detailed X-ray diffraction analysis was performed on laser annealed SiGe samples. Results showed that the most interesting configuration to explore for defects curing was low energies (surface melt onset energies). For high energies, Ge segregation was observed.

Using a highly ordered e-beam lithography based patterning with other diameters and pitches could also be beneficial in terms of SiGe layer quality. An e-beam defined mask was therefore created, and base wafers produced. Growth of SiGe layers of different thicknesses was performed. Samples are currently being characterized. This should help understanding the effect of geometry on the growth and coalescence of SiGe layers, with a more regular patterning compared to our standard co-polymer masks.

ANNEX I:
Extended abstract in French
Résumé étendu en Français

Introduction

Nous vivons à une époque connectée où l'analyse et l'échange de quantités énormes de données se fait par un large réseau d'objets connectés. Ordinateurs, smartphones, tablettes, montres connectées et assistants virtuels etc. sont le fruit d'avancées technologiques depuis le milieu des années 1900. En effet, un long chemin a été parcouru depuis la mise en évidence d'un effet transistor par Bardeen et Brattain en 1947 aux dernières annonces de TSMC concernant « le nœud technologique 5 nm ». La meilleure illustration de ces avancées technologiques est la loi de Moore, qui a prédit un doublement de la densité des transistors tous les 12 à 18 mois et ceci pendant plusieurs décennies. Tout au long de ce parcours technologique, le silicium a su s'imposer comme un élément clé. Grâce à la stabilité de son oxyde, sa facilité de fabrication et son abondance naturelle, il est au cœur d'une technologie mature et extrêmement évoluée.

La loi de Moore ainsi que la technologie silicium ont donc parcouru un long chemin ensemble. Cependant, au fur et à mesure que les transistors réduisent en taille, des problèmes électroniques auparavant insignifiants deviennent extrêmement critiques. L'un de ces problèmes est l'important courant de fuite généré par les effets de canaux courts. Il a donc fallu réfléchir à plusieurs solutions afin de limiter ces effets. Parmi ces éléments d'amélioration des performances se trouve le silicium contraint en tension couplé à la technologie SOI (Silicon-on-Insulator) de substrats Silicium sur Isolant.

Le silicium n'est intuitivement pas le semi-conducteur idéal d'un point de vue structure du bande ou mobilité des électrons ou trous. La mobilité des porteurs de charge dans le silicium est en effet relativement faible comparée à celle d'autres matériaux comme le Ge ou les composés III-V. Toutefois, l'intégration de ces matériaux alternatifs sur technologie silicium s'avère laborieuse.

Le silicium contraint en tension est une bonne alternative afin d'accroître la mobilité des porteurs de charge. Une des méthodes utilisées pour contraindre le silicium en tension consiste à faire croître une couche de Si au-dessus d'un substrat virtuel de SiGe (couche de SiGe totalement relaxée obtenue par épitaxie sur un substrat de silicium). Il est donc évident que la qualité du substrat virtuel de SiGe aura un impact critique sur la couche de Si contraint. Du fait du désaccord de paramètre de maille entre la couche SiGe et le substrat massif de Si, la qualité de la couche SiGe dépendra fortement de la relaxation des contraintes lors du procédé de croissance par épitaxie. Plusieurs schémas de croissance ont été explorées afin d'obtenir des substrats virtuels de SiGe de bonne qualité. Par exemple, les techniques de type « buffer » avec gradient de concentration en Ge permettent de produire des couches SiGe parfaitement relaxées et de haute qualité. Cependant, les couches obtenues par cette méthode sont très épaisses (plusieurs microns) ce qui peut être préjudiciable en termes de coût (temps de croissance, consommation de gaz, etc.) et de courbures de plaque (en particuliers pour les plaques de diamètre 300 mm).

Durant cette thèse, nous avons exploré un nouveau paradigme pour la croissance de couches SiGe relaxées sur Si. Appelée nano-hétéroépitaxie, cette méthode a été mis en théorie pour la première fois en 1986 par Luryi et Suhir (Luryi and Suhir 1986) des laboratoires BELL. L'idée générale est de fournir à la matière des degrés supplémentaires de relaxation élastiques des contraintes en démarrant la croissance à partir de nano-piliers de taille nanométrique. Ces dernières années, au LETI, plusieurs développements axés sur la lithographie à base de copolymères à bloc ont vu le jour. En l'occurrence, ce type de lithographie permet de créer des nanostructures dont les dimensions répondent aux spécifications théoriques de Luryi et Suhir. C'est ainsi que ce projet a été initié où il a d'abord été question de définir un schéma d'intégration basé sur la lithographie à copolymères à bloc permettant de fabriquer les structures nanométriques de départ. Par la suite, la nano-hétéroépitaxie de couches SiGe a été explorée par dépôt chimique en phase vapeur à pression réduite (20 Torr) ou RP-CVD (Reduced Pressure Chemical Vapor Deposition) dans un bâti industriel d'épitaxie 300 mm.

Ces travaux de thèse comprennent 4 études faisant office de chapitres expérimentaux :

I. Une première étude portant sur la nano-hétéroépitaxie de couches SiGe suivant deux schémas d'intégration différents : un premier schéma avec nano-piliers de Si et un second schéma avec nano-piliers SiGe. Pour les deux approches, nous nous sommes tous d'abord intéressé à la croissance sélective des nano-piliers et ensuite à l'étude de couches SiGe coalescées à partir de ces nano-piliers.

II. Une seconde étude où l'on s'est intéressé à la coalescence de nano-piliers de SiGe. L'idée était d'étudier le phénomène de coalescence aux tous premiers stades de la croissance cristalline et suivre la création de défauts.

III. Une troisième étude pour connaître l'impact du masque sur la nano-hétéroépitaxie de couches SiGe. Les différents paramètres étudiés ont été la taille du masque, sa présence (ou pas) ainsi que la nature du matériau dont il est formé.

IV. Une dernière étude, où l'approche par nano-hétéroépitaxie a été étendue à un nouveau matériau : le germanium pur. Comme pour le SiGe, nous avons tous d'abord étudié la croissance de nano-piliers de Ge. Par la suite, L'approche a été évaluée en effectuant une comparaison entre croissance de couches Ge par nano-hétéroépitaxie et croissance de couches Ge sur substrats Si massifs.

I. Nano-hétéroépitaxie de films SiGe sur nano-piliers Si et SiGe

L'objectif de cette première étude était de réaliser par nano-hétéroépitaxie des couches de $Si_{0.75}Ge_{0.25}$ de 200 nm qui soient entièrement relaxées. On notera qu'une couche $Si_{0.75}Ge_{0.25}$ de 200 nm d'épaisseur épitaxiée sur substrat massif de Si est totalement contrainte (Hartmann et al. 2011).

Pour cette première étude, nous nous sommes basés sur le schéma d'intégration représenté en **Figure I.1.** Ce dernier engendre un masque d'oxyde nano-structuré avec une configuration hexagonale compacte (**Figure I.2**) définie par la lithographie à copolymère à bloc.

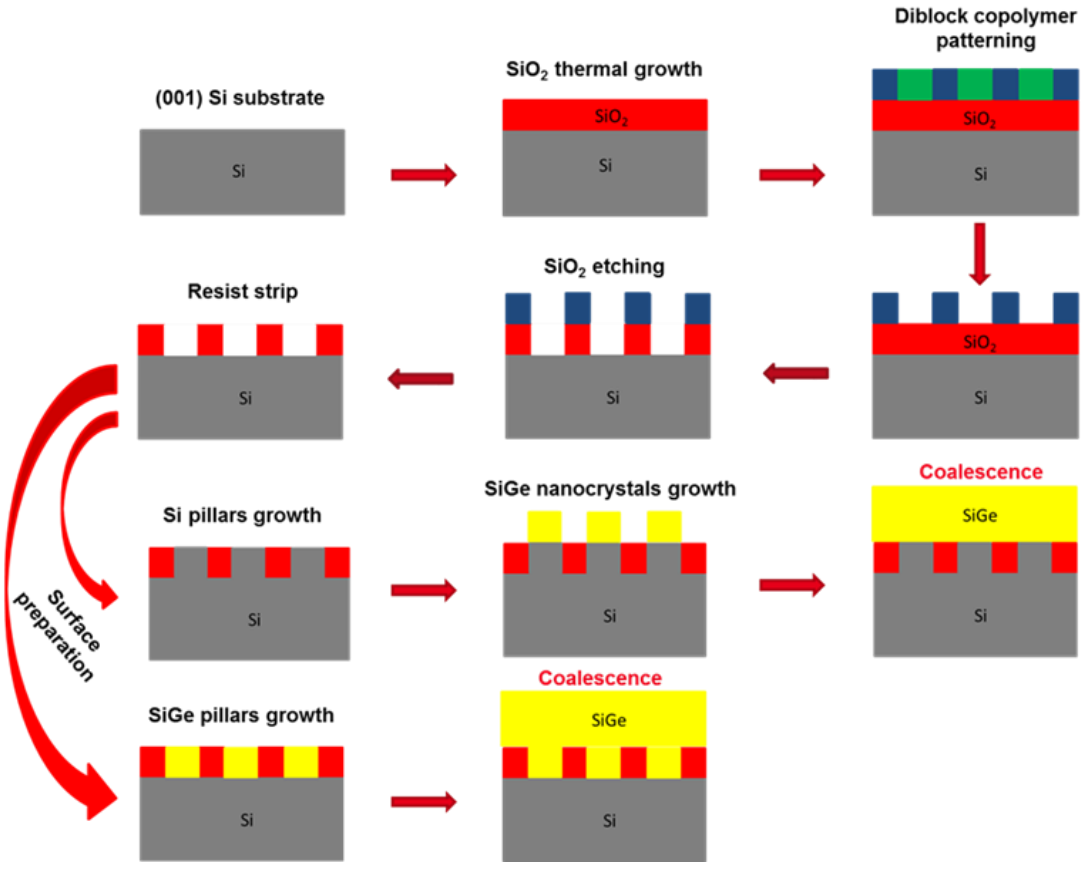

Figure I.1 Processus de fabrication du masque en oxyde nano-structuré et schémas d'intégration pour la nano-hétéroépitaxie de SiGe

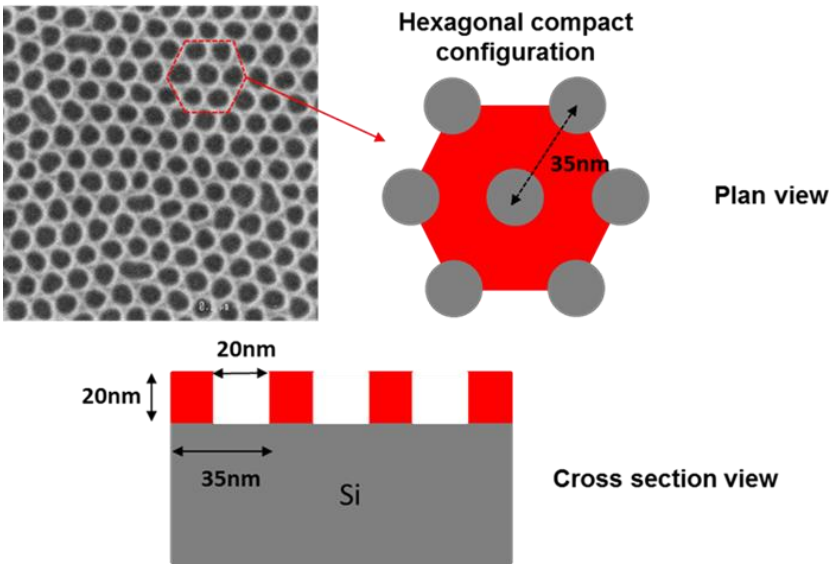

Figure I.2 Image en Microscopie Electronique à Balayage (en vue de dessus) du masque d'oxyde (en haut à droite) avec un schéma de la configuration hexagonale compacte définie par le motif du copolymère à bloc (en haut à gauche) et un schéma en coupe transversale du masque d'oxyde (en bas)

La préparation de surface précédant la croissance des nano-piliers a été une étape critique dans ce schéma d'intégration puisqu'un nettoyage par voie humide « HF-last » ne nous a pas permis de croitre sélectivement des nano-piliers de Si ou SiGe. La solution à ce problème a été d'utiliser un procédé de nettoyage Siconi mettant en oeuvre un plasma déporté à base de NH_3/NF_3 pour convertir l'oxyde natif en sels d'oxyde sublimés à basse température (Yang et al. 2010).

Nous avons utilisé deux approches différentes pour la croissance de couches SiGe par nano-hétéroépitaxie. Une première qui consiste à épitaxier de manière sélective des nano-piliers de Si suivi de la croissance de couches SiGe coalescées et une seconde qui consiste à déposer d'abord des nano-piliers de SiGe, suivi de couches SiGe coalescées. Pour cela, nous avons utilisé un bâti d'épitaxie ASM Epsilon 3200 à une pression de croissance constante fixée à 20 Torr. Le SiH_2Cl_2 et le GeH_4 ont été respectivement utilisés comme précurseurs gazeux de Si et Ge. Le débit du gaz vecteur : H_2 purifié, de plusieurs dizaines de litres par minute, n'a pas été modifié lors des différentes croissances.

La croissance de nano-piliers de Si de 20 nm de hauteur a été réalisée à l'aide d'un procédé sélectif à base de SiH_2Cl_2, HCl et H_2 (Hartmann et al. 2003). La température de croissance a été fixée à 850°C. Une image en Microscopie à Force Atomique (AFM) des nano-piliers de Si en 2x2 μm^2 est représentée en **Figure I.3.** La distribution observée en termes de hauteur des nano-piliers est forcément dû à l'exposition hétérogène des nano-cavités aux flux de gaz.

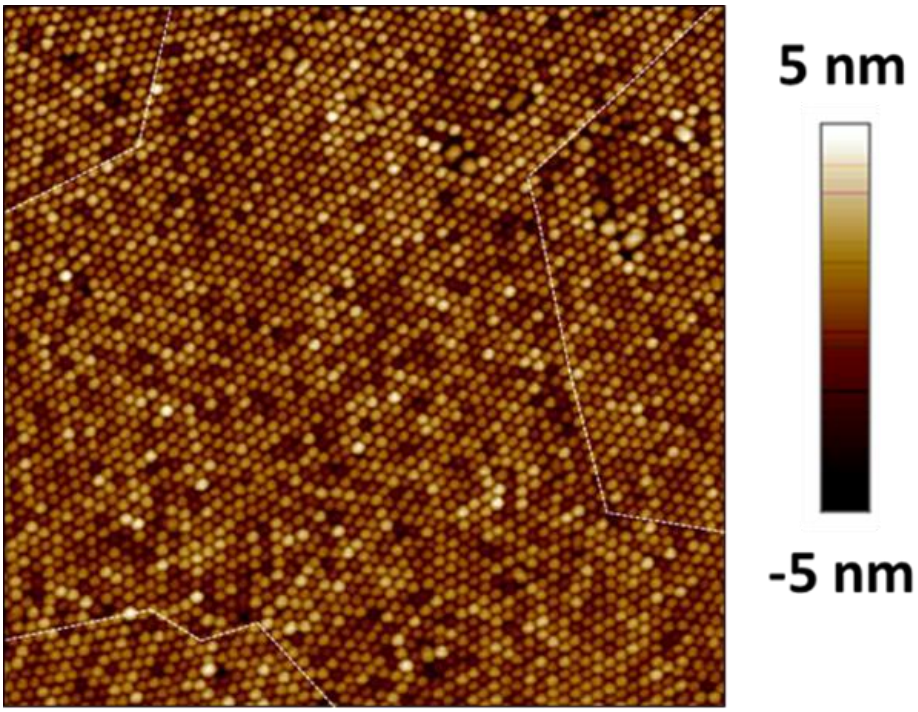

Figure I.3 Image AFM de taille 2x2 µm² représentant les nano-piliers de Si

Une image MEB en vue incliné de ces mêmes nano-piliers est montrée en **Figure I.4** où leur facettage est clairement visible. Malgré la limitation de la résolution de l'image MEB, il semble que la forme des piliers est principalement pyramidale, avec une base carrée, et un sommet parfois tronqué. Dans ce cas, le plan cristallin au sommet de la pyramide est selon toutes probabilités un plan (001). Les plans des faces de la pyramide devraient être des plans {111}.

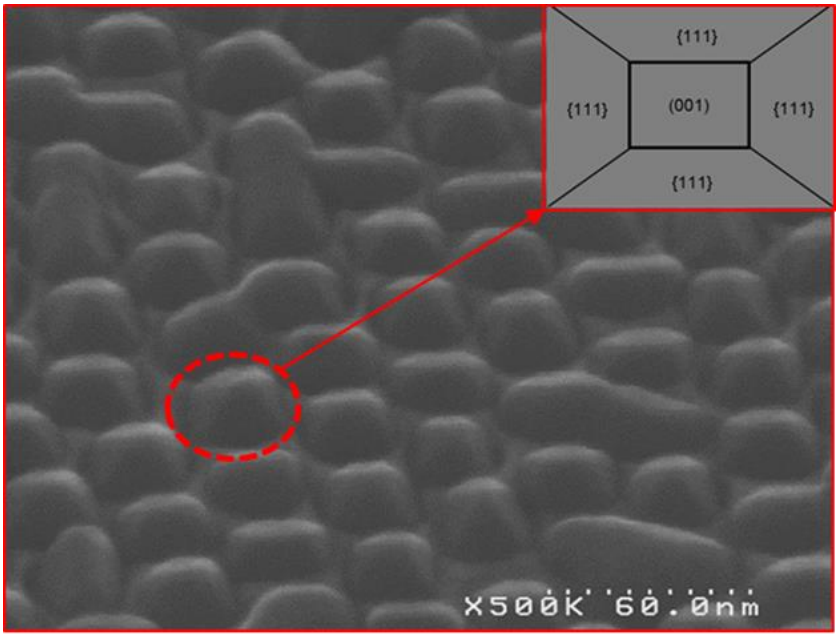

Figure I.4 Image MEB en vue inclinée d'une surface recouverte de nano-piliers de silicium avec un schéma suggérant les plans du facettage

Ayant obtenu des nano-piliers de Si d'une certaine homogénéité, nous avons ensuite étudié l'impact de la température de croissance de couches SiGe sur ces nano-piliers. La croissance de couches SiGe 25% avec une épaisseur visée de 200 nm a été réalisée à 650°C, 700°C, 750°C et 800°C avec du GeH_4, du SiH_2Cl_2 et de l'H_2 (Hartmann et al. 2002). Les analyses AFM ont montré que les couches présentant les surfaces les plus lisses étaient celle réalisées aux plus basses températures, c'est-à-dire à 650°C et 700°C. Ces couches présentant les surfaces les plus lisses ont été caractérisées par Diffraction de Rayons X. Le pourcentage de Ge, le degré de relaxation des contraintes ainsi que la largeur à mi-hauteur de ces couches sont retranscrits dans le **Tableau I.1**.

SiGe layer growth temperature (°C)	Ge concentration (%)	Degree of relaxation (%)	FWHM (arcsec)
650	27.2	85.6	1149
700	25.8	94.8	895

Tableau I.1 Pourcentage de Ge, degré de relaxation et largeur à mi-hauteur des pics en DRX pour des couches SiGe de 200 nm d'épaisseur épitaxiées à 650°C et 700°C sur nano-piliers de Si

Le pourcentage en Ge supérieure aux 25% visés pour les deux couches (d'après les cinétiques de croissance sur substrat de Si massif) est probablement dû aux effets de charge (Ito et al. 1995). Les couches de SiGe sont hautement relaxées grâce notamment à la nouvelle approche utilisée. La couche de SiGe à 700°C présente une largeur à mi-hauteur inférieure à celle à 650°C. La qualité de la couche est ainsi meilleure à 700°C.

Une observation en Microscopie Electronique en Transmission (MET) en section transverse montrée en **Figure I.5** a été réalisée sur la couche de SiGe épitaxiée à 700°C présentant la surface la plus lisse ainsi que la meilleure qualité. Les nano-piliers de Si ont conservé leur forme de pyramide tronquée. Les murs d'oxydes qui les séparent sont triangulaires en raison de la préparation de surface utilisée avant épitaxie (la Siconi grave l'oxyde de façon isotrope). L'image MET suggère que la nucléation de défauts planaires tels que les macles et les défauts d'empilement commence à l'interface entre les piliers de Si et la couche de SiGe, généralement juste au-dessus des murs d'oxyde. Il y a presque un défaut par pilier, bien qu'il semble, sur des images à plus grand champ, que certains piliers soient exempts de défauts. Cependant, l'image MET reste difficile à interpréter en raison des effets de projection et de la très petite taille des nano-objets observés, qui sont inférieurs à l'épaisseur typique d'une lamelle.

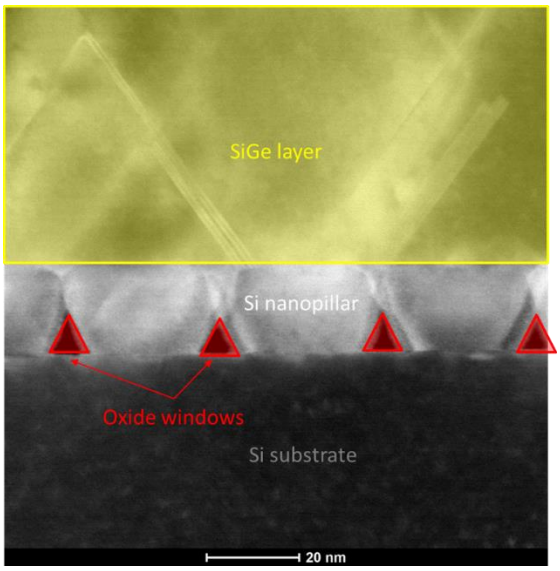

Figure I.5 Image MET en section transversale d'une couche de SiGe épitaxée à 700°C sur des nano-piliers en Si, montrant l'ensemble de la structure avec le substrat en Si, les fenêtres délimitées par des murs en oxyde et la couche de SiGe présentant des défauts.

L'utilisation de nano-piliers de SiGe a été également étudiée. La croissance de nano-piliers de $Si_{0.75}Ge_{0.25}$ de 20 nm de haut a été réalisé à 650°C et 700°C à l'aide d'un procédé sélectif à base de SiH_2Cl_2, GeH_4 et H_2 (Hartmann et al. 2003). Les conditions de croissance ont été calibrées afin d'avoir le même contenu en Ge et la même hauteur pour les piliers. La **Figure I.6** montre les images MEB en vue inclinées (à gauche) et les balayages AFM 1x1 µm² (à droite). Tous les piliers étant bien définis et uniformes, il y a peu de différence entre les croissances à 650°C et 700°C.

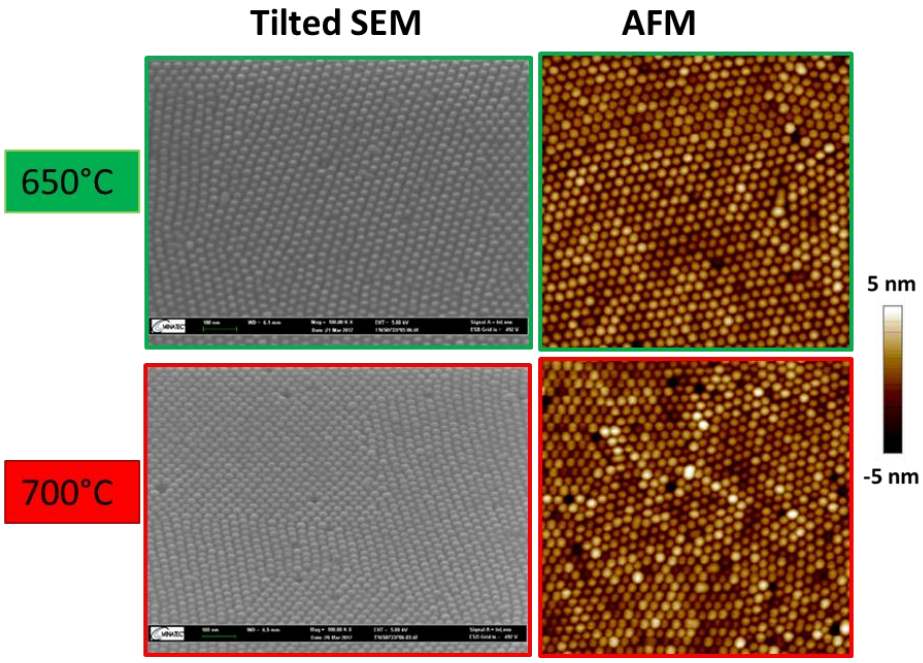

Figure I.6 Scans AFM 1x1 µm² (à droite) et images MEB en vue inclinée (à gauche) de nano-piliers SiGe à 650 et 700 ° C. Les côtés des mages AFM se trouvent dans les <110> directions

Après ces développements sur les nano-piliers de SiGe, nous avons réalisé la croissance de notre couche $Si_{0.75}Ge_{0.25}$ référence de 200nm à 700°C sur ces nano-piliers de SiGe à 650 et 700°C. La **Figure I.7** montre que les couches de SiGe obtenues sont relativement lisses.

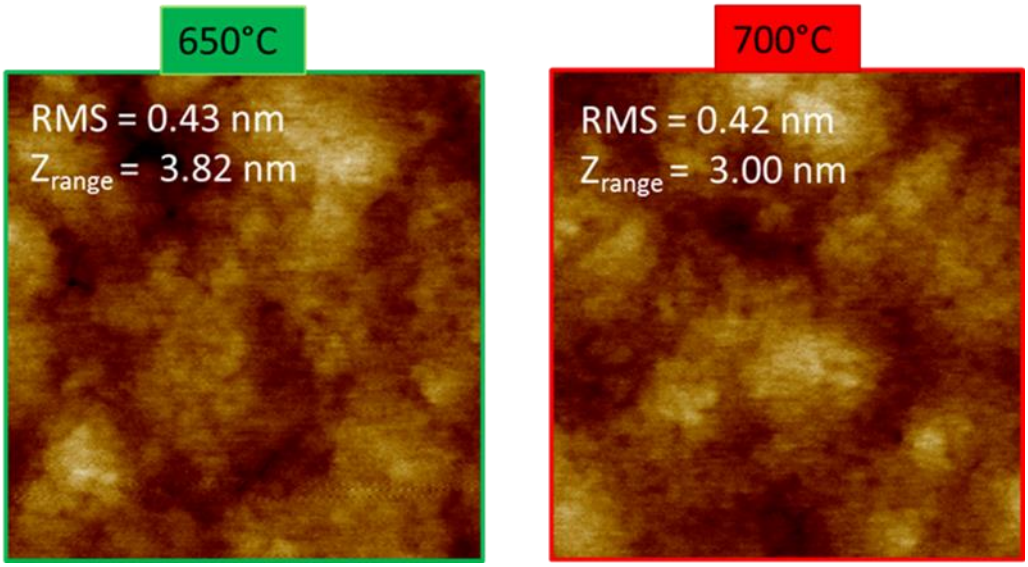

Figure I.7 Images AFM 1x1 µm² des couches de SiGe réalisés sur des nano-piliers de SiGe faits à différentes températures avec les valeurs correspondantes de rugosité Root Mean Square et de plage en Z.

Ces couches ont été caractérisées par DRX. Le pourcentage de Ge, le degré de relaxation des contraintes ainsi que la largeur à mi-hauteur de ces couches en DRX sont retranscrits dans le **Tableau I.2.**

SiGe nano-pillars growth temperature (°C)	Ge concentration (%)	Degree of relaxation (%)	FWHM (arcsec)
650	25.4	109	684
700	25.5	111	557

Tableau I.2 Pourcentage de Ge, degré de relaxation et largeur à mi-hauteur en DRX des couches SiGe sur nano-piliers de SiGe

Les concentrations en Ge obtenues sont proches des 25% visés. Encore une fois, des valeurs élevées de relaxation sont obtenues avec l'approche par nano-hétéroépitaxie. Les échantillons contenant des nano-piliers SiGe à 650 ° C et à 700 ° C sont soumis à une contrainte de tension (c'est-à-dire avec R> 100%), avec un degré de relaxation d'environ 110%. Lors du refroidissement après croissance, une contrainte en tension est ajoutée aux couches en raison d'un désaccord de paramètres de dilatation thermique. La largeur à mi-hauteur la plus basse

(557 arcsec) est obtenue pour l'échantillon avec des nano-piliers SiGe à 700°C. Cette valeur est inférieure à celle des nano-piliers Si, ce qui signifie que les nano-piliers SiGe sont bénéfiques en termes de qualité des couches.

Des observations MET ont été effectuées sur l'échantillon présentant la largeur à mi-hauteur la plus basse (c'est-à-dire celui avec les nano-piliers SiGe à 700°C), afin de mieux comprendre la nature des défauts cristallins dans ces empilements.

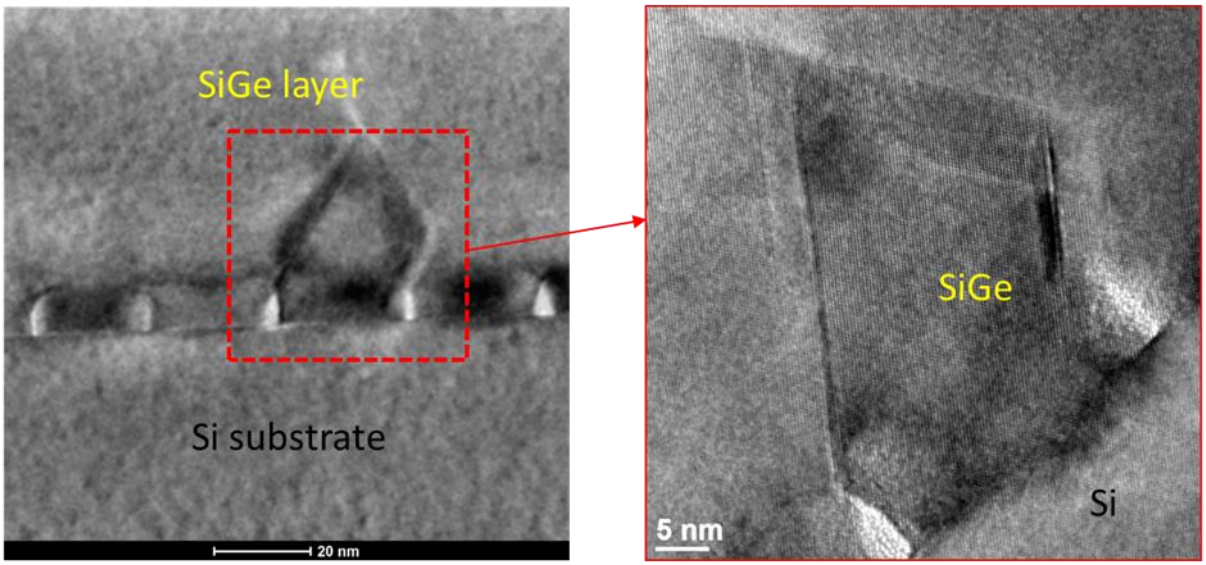

Figure I.8 5 Image MET en section transversale d'une couche de SiGe déposée sur des nano-piliers en SiGe (tout à 700°C).

L'image MET de la **Figure I.8** suggère que, comme précédemment, les murs de SiO_2 séparant les nano-piliers ont une forme triangulaire en raison de la gravure isotrope de l'oxyde isotrope lors de la préparation de surface de type Siconi avant l'épitaxie. Les défauts tels que les fautes d'empilement ou macles au sommet des murs de SiO_2 sont comparables aux défauts observés sur les couches avec nano-piliers en Si. Cela signifie que la nature des nano-piliers n'a pas d'impact majeur sur le type de défauts.

Nous avons donc des mécanismes de génération de défauts très similaires pour les nano-piliers Si et SiGe, ce qui pourrait être dû à l'une des hypothèses suivantes:

- La croissance de SiGe sur les facettes {111} des piliers peut provoquer la formation de défauts de type macles, comme indiqué dans la réf. (Kuan and Iyer 1991).

- Des défauts peuvent être créés lors de la croissance au niveau des fronts de croissance au-dessus du masque d'oxyde.

- La contrainte thermique générée par le masque d'oxyde pendant la croissance pourrait également être une source de défauts (Leonhardt et al. 2011).

II. Coalescence de nano-piliers SiGe

Une étude sur la coalescence de nano-piliers SiGe a été initiée afin de mieux comprendre les différents mécanismes liés à ce phénomène, mais aussi pour vérifier l'une des hypothèses précédentes concernant la génération de défauts.

Pour cette étude, nous avons gardé le même schéma d'intégration utilisé précédemment. Des nano-piliers SiGe de différentes épaisseurs ont ensuite été déposés sélectivement. L'épaisseur a été estimée à partir de la vitesse de croissance de couches SiGe obtenu sur un substrat massif de Si (001). Pour cela, nous avons utilisé un bâti d'épitaxie ASM Epsilon 3200 à une pression de croissance constante fixée à 20 Torr. Le SiH_2Cl_2 et le GeH_4 ont été respectivement utilisés comme précurseurs gazeux de Si et Ge. Le débit du gaz vecteur : H_2 purifié, de plusieurs dizaines de litres par minute, n'a pas été modifié lors des différentes croissances. Des nano-piliers de SiGe de hauteur 20, 25, 30 et 35 nm avec un pourcentage en Ge ciblée de 25% ont été déposés sélectivement à 700 ° C avec les rapports de flux suivants : $[SiH_2Cl_2]/[H_2]$ = 0,003 et $[GeH_4]/[H_2]$ = 0,00023) (Hartmann et al. 2002). Les conditions de croissance étaient celles utilisées pour obtenir les couches de SiGe coalescées avec la meilleure qualité sur des nano-piliers de SiGe. La vitesse de croissance résultant était de 20 nm/min.

La **Figure II.1** montre d'images AFM de 1x1 μm^2 de nano-piliers SiGe de différentes épaisseurs. Ces images AFM ont été effectuées au centre de chaque plaque et montrent une évolution de la coalescence au fur et à mesure que l'épaisseur augmente. Les nano-piliers de 20 nm d'épaisseur de SiGe sont bien ordonnés et homogènes en hauteur et en diamètre, comme vu précédemment avec ce procédé. À 25 nm, quelques nanopiliers commencent à fusionner avec leurs voisins, ce qui donne des grains de diamètre supérieur. Cependant, la majorité des nano-piliers n'a pas encore fusionné. Une épaisseur de 30 nm donne un degré de coalescence plus élevé, dans la mesure où la majorité des nano-piliers ont fusionné et le diamètre moyen des grains est plus élevé. De plus, nous notons que les nano-piliers coalescés sont non seulement cylindriques, mais de formes différentes. Cependant, il reste encore des nano-piliers qui ont la même taille et la même forme que dans les deux échantillons précédents, c'est-à-dire qui n'ont pas encore fusionné. Pour une croissance de 35 nm, tous les nano-piliers initiaux ont maintenant fusionné et les conglomérats prennent différentes formes et tailles.

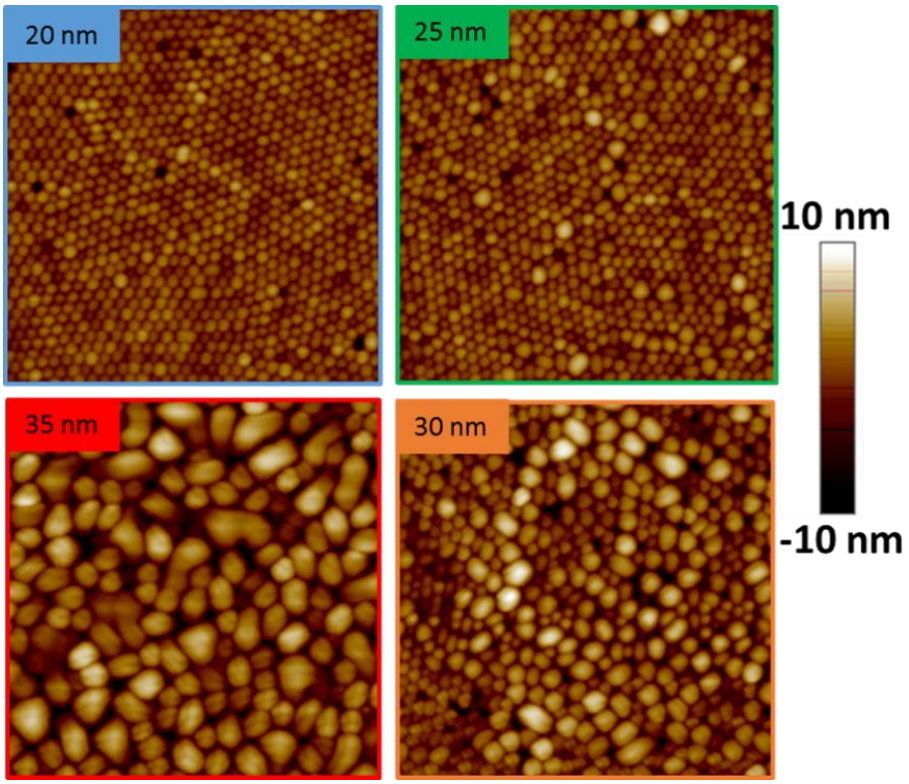

Figure II.1 Images AFM 1 x 1 µm² de nano-piliers SiGe à 20 nm (bleu), 25 nm (vert), 30 nm (orange) et 35 nm (rouge)

Ces échantillons ont été caractérisés aussi par DRX. Le pourcentage de Ge et le degré de relaxation des contraintes sont retranscrits dans la **Figure II.2**.

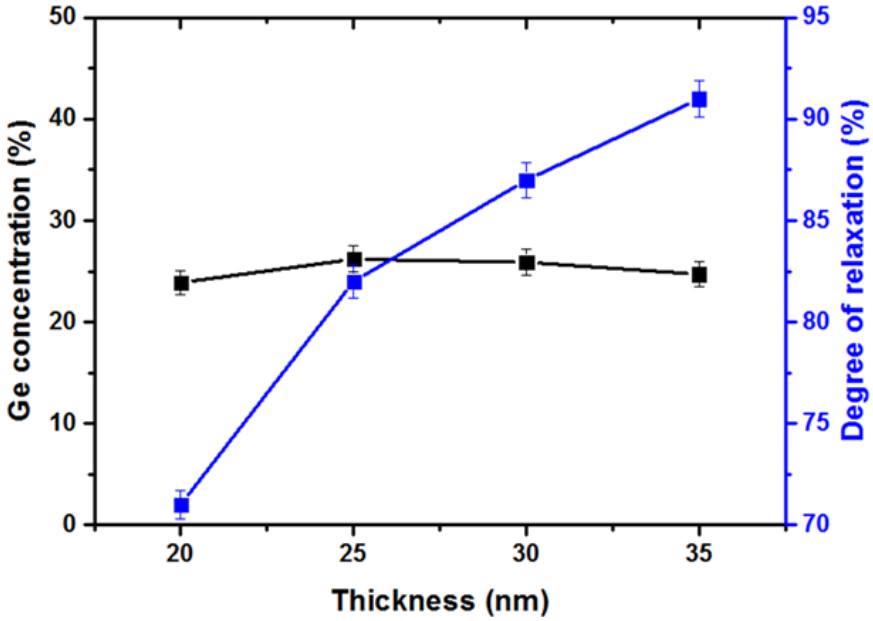

Figure II.2 Concentration en Ge (noir) et degré de relaxation de contrainte (bleu) des nano-piliers SiGe à 20, 25, 30 et 35 nm.

Comme on pouvait s'y attendre, le degré de relaxation des contraintes des nano-piliers augmente avec l'épaisseur, passant de 71% pour les piliers de 20 nm à 91% pour les piliers de 35 nm. Au fur et à mesure que les nano-piliers augmentent en taille, ils émergent des nano-cavités et une relaxation élastique très rapide des contraintes est favorisée. En termes de concentration en Ge, elle est à peu près constante, à environ 25% pour les quatre échantillons étudiés.

La Scanning Spreading Resistance Microscopy (SSRM) a été utilisée pour étudier la génération de défauts dans nos échantillons. Cette technique de microscopie mesure la résistance électrique de l'échantillon en lui appliquant une tension de polarisation et en collectant le courant à travers une pointe conductrice. Vu que les propriétés électriques des couches sont susceptibles de changer avec la densité de défauts, cette technique devrait aider à identifier les grains de coalescence comportant des défauts.

Les échantillons analysés avec cette technique sont ceux contenant des nano-piliers SiGe à 20 et 35 nm. Les échantillons ont été balayés en mode contact en utilisant une tension de polarisation de -1 V et une pointe en diamant. La **Figure II.3** montre des images SSRM de 200 x 200 nm^2 des deux échantillons. Comme prévu, le masque en oxyde est plus résistant (en vert) que les nano-piliers (en violet). La très bonne résolution de la SSRM nous permet de distinguer les nano-piliers de 20 nm qui sont très uniformes d'un point de vue électrique (image de gauche). Pour l'échantillon de 35 nm (image de droite), il existe des variations de résistivité locales dans les grains formés par les nano-piliers coalescés, avec la présence de domaines électriques marqués par des stries (indiquées par des flèches blanches). Cela pourrait être un indicateur de défauts de coalescence.

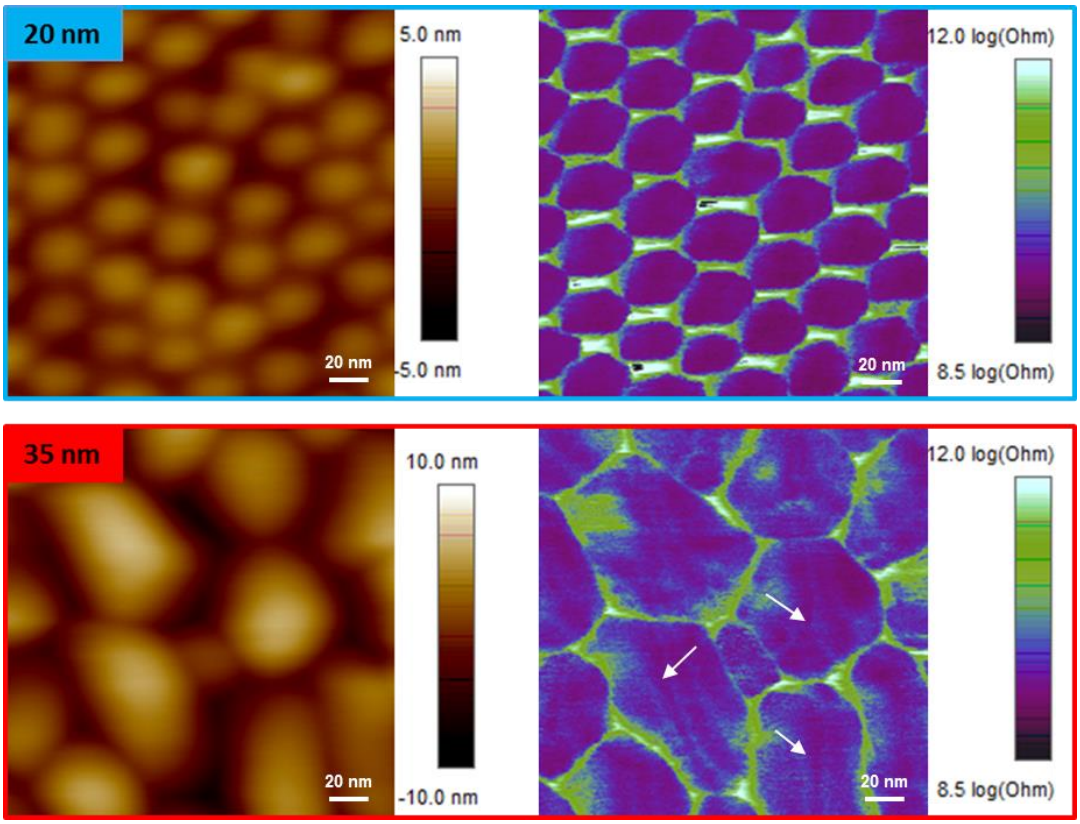

Figure II.3 Images SSRM 200 x 200 nm² de nano-piliers SiGe à 20 nm et 35 nm. Les balayages en hauteur sont montrés à gauche et les balayages électriques sont présentés à droite.

La **Figure II.4** montre une collection d'images MET haute résolution en section transversale de divers nano-piliers de SiGe à 20 nm d'épaisseur. Aucun des 12 nano-piliers imagés ne présente de défauts cristallins. Ceci est cohérent avec les images SSRM qui ont montré que la résistance électrique des piliers était très uniforme, i.e. qu'ils étaient probablement exempts de défauts. Les nano-piliers présentent des facettes spécifiques à la croissance épitaxiale sélective de SiGe (Pribat et al. 2009), avec des facettes {111} bien visibles sur les flancs des nano-piliers. Cette formation de facettes peut être préjudiciable à la croissance ultérieure en termes de génération de défauts. En effet, la croissance sur des plans SiGe {111} peut provoquer la formation de macles (Kuan and Iyer 1991).

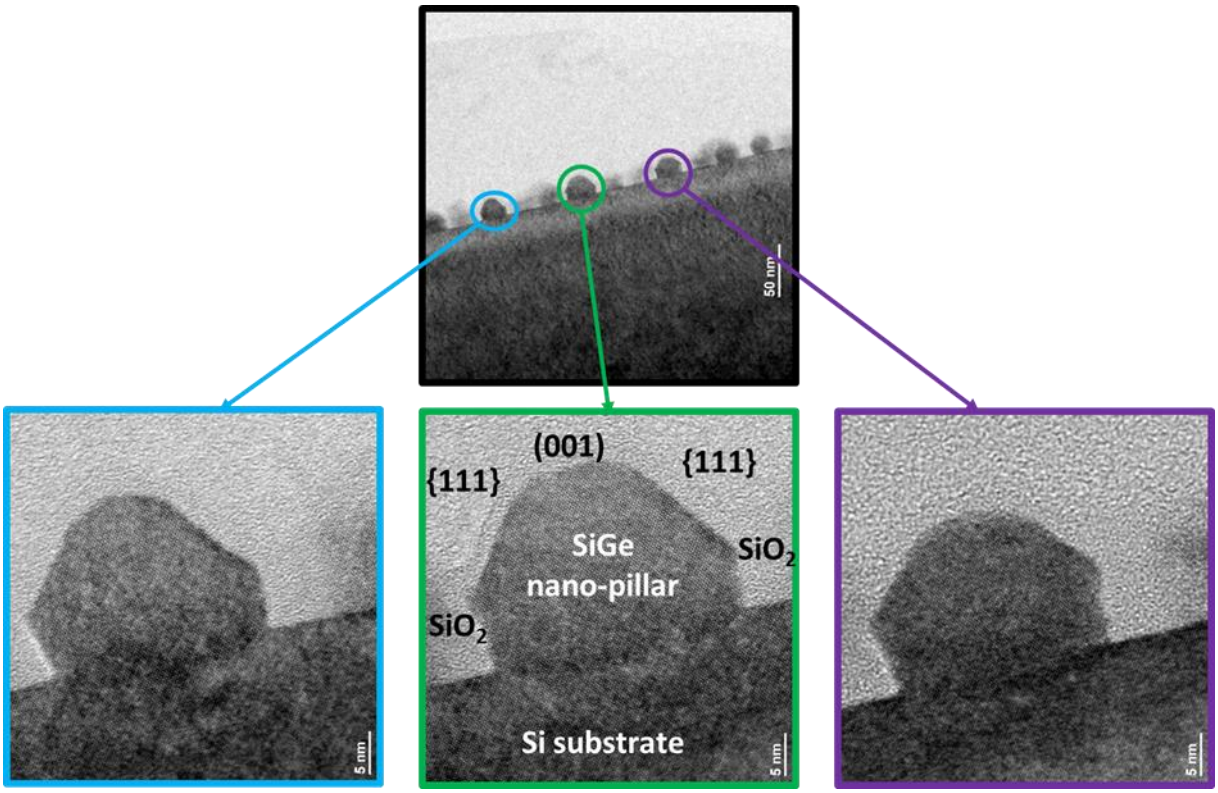

Figure II.4 Images MET haute résolution de nano-piliers SiGe à 20 nm

Des images MET à haute résolution de nano-piliers SiGe partiellement coalescés à 35 nm sont représentées en **Figure II.5**. Plusieurs schémas de coalescence peuvent être distingués. L'image en bleu (en bas à droite) montre une coalescence sans défaut. L'image en vert (en haut à droite) montre une coalescence avec la présence d'une faute d'empilement en haut d'un grain. Les images en rouge (en haut à gauche) montrent une coalescence avec une faute d'empilement commençant au sommet du mur d'oxyde. Il s'agit de la configuration la plus courante. Ces fautes d'empilement pourraient être dus au motif de l'oxyde, qui n'est pas parfaitement régulier ni symétrique, ce qui entraîne une fusion imparfaite des plans cristallographiques des nano-piliers. Ces défauts peuvent également être dus au processus de coalescence lui-même, l'espacement interplanaire dans deux fronts distincts pouvant être différent. Enfin, les images en violet montrent une coalescence avec la présence d'une macle. Ceci pourrait être lié aux facettes des nano-piliers SiGe, comme indiqué ci-dessus. Les jonctions entre les nano-piliers coalescés sont exemptes de dislocations. Il n'y a pas non plus de dislocations à l'interface entre le substrat de Si et les nano-piliers de SiGe (grâce à des degrés de liberté supplémentaires permettant une relaxation élastique des contraintes emmagasinées). Les seuls défauts observés aux jonctions des nano-piliers sont des défauts planaires de type faute d'empilement et macle. Nous suggérons que les stries observées sur les images SSRM sont peut-être une manifestation électrique de défauts structurels tels que les fautes d'empilement et macles dans les nano-piliers coalescés, mais cela devrait être confirmé par d'autres essais.

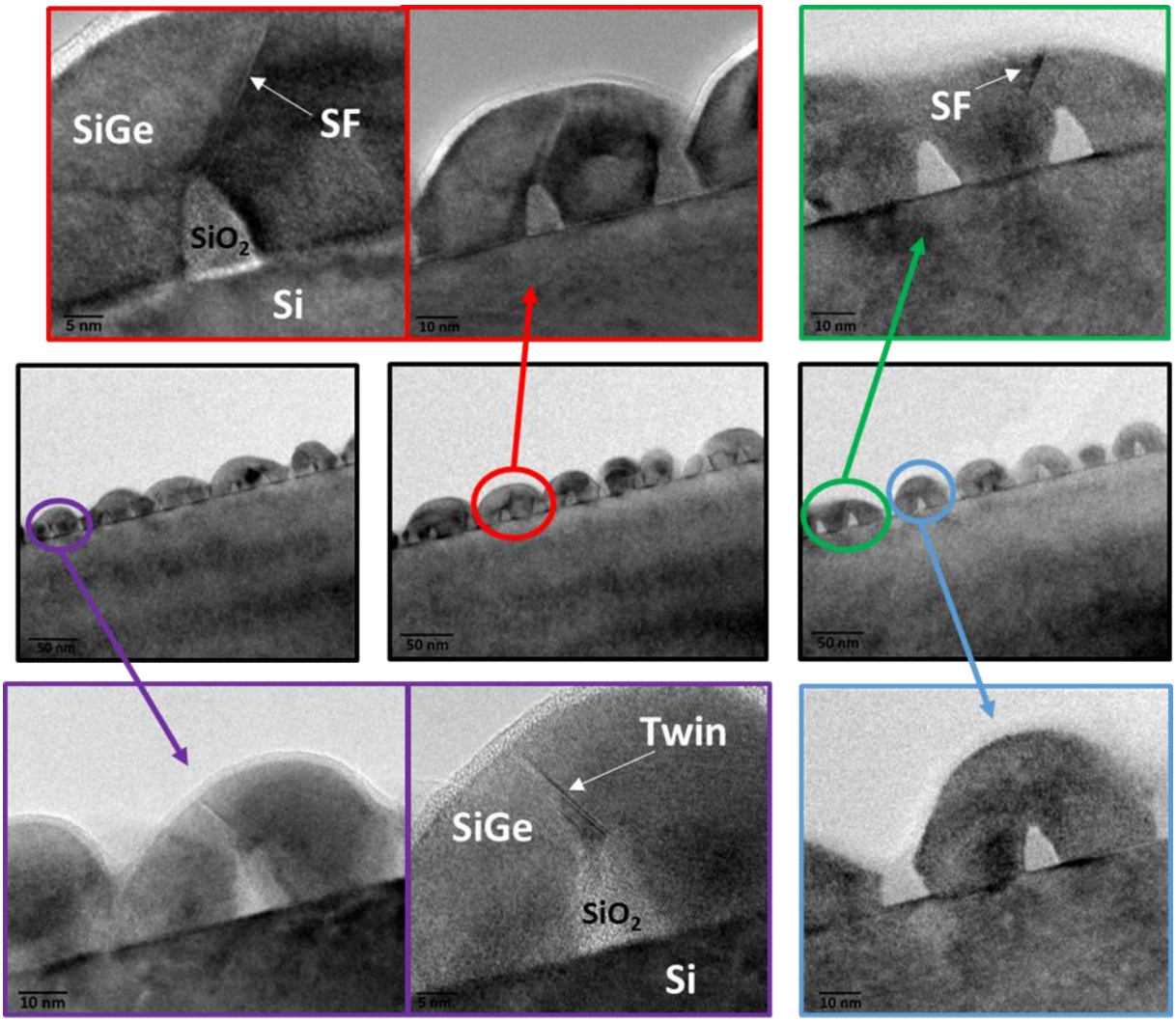

Figure II.5 Images MET haute résolution de nano-piliers SiGe à 35 nm

III. Impact du masque sur la nano-hétéroépitaxie de couches SiGe

L'objectif de cette étude était d'évaluer l'impact du masque sur la nano-hétéroépitaxie couches SiGe. Pour cela nous avons exploré 3 stratégies schématisés en **Figure III.1** :

- Utilisation d'un masque d'oxyde de taille différente (**Figure III.2**)
- Retrait du masque d'oxyde après la croissance des nano-piliers SiGe
- Utilisation d'un SiN sans contrainte comme matériau de masquage au lieu du SiO_2

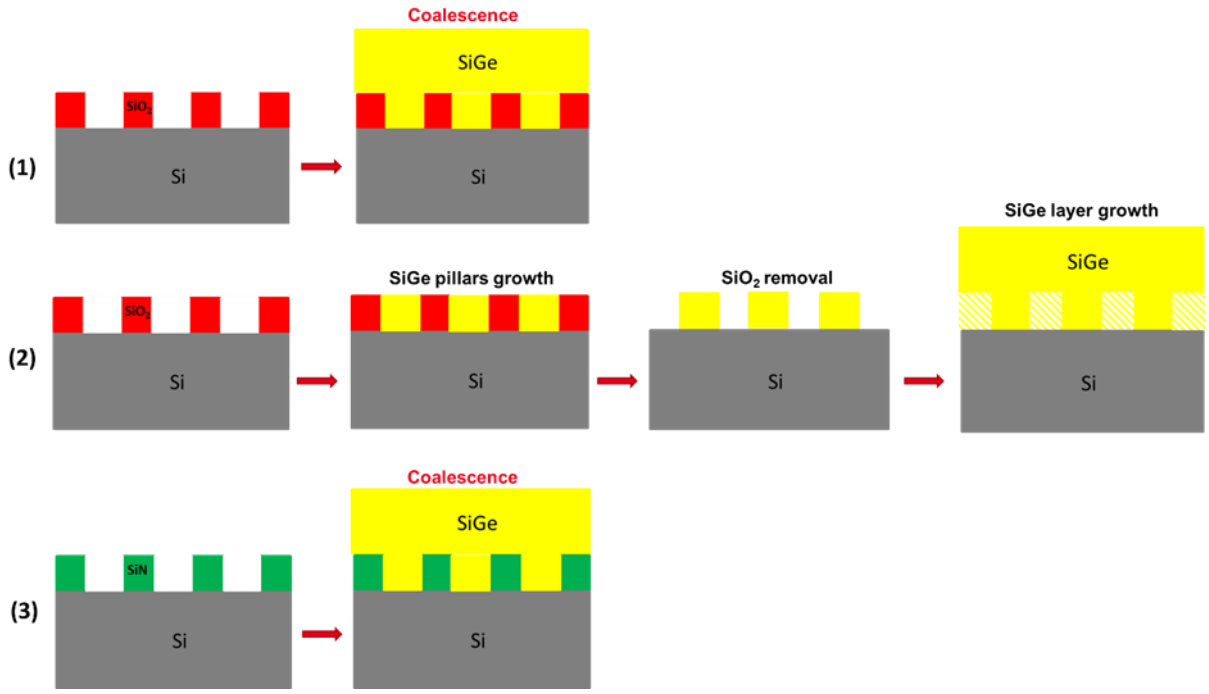

Figure III.1 Schémas d'intégration pour l'étude de l'impact du masque sur la nano-hétéroépitaxie de couches SiGe: (1) Croissance avec un masque de taille différente (2) Croissance sans masque (3) Croissance avec masque SiN

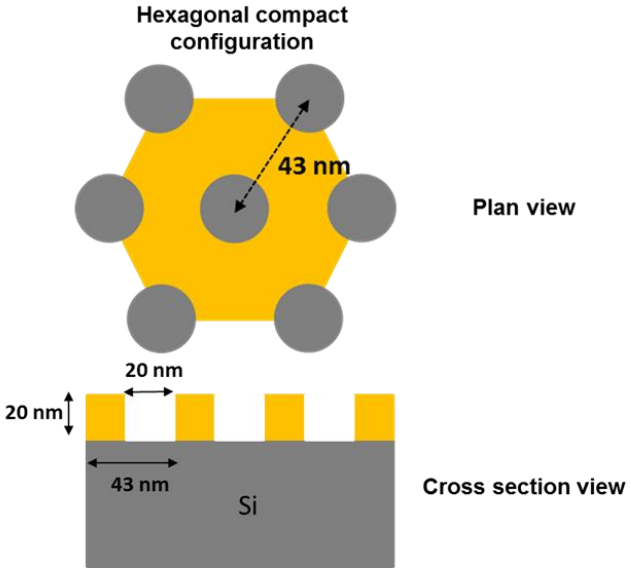

Figure III.2 Schéma en vue de dessus de la configuration hexagonale compacte définie par une lithographie de type copolymère à bloc (en haut à gauche) et schéma en coupe transversale du nouveau masque avec une période de 43 nm (en bas)

La préparation de surface précédant la croissance des nano-piliers a été une étape critique puisqu'un nettoyage par voie humide « HF-last » ne nous permettait pas, sur masques avec une période de 35 nm, d'épitaxier sélectivement des nano-piliers SiGe. Pour le nouveau masque d'oxyde avec une période de 43 nm, la séquence de nettoyage humide suivante a été utilisée: une immersion dans de l'eau ozonisée suivie d'une immersion dans du HF dilué et enfin un séchage. Une telle solution était plus flexible que la Siconi qui était nécessaire pour les masques avec une période de 35 nm.

Afin de valider le nouveau masque avec période de 43nm, des nano-piliers de SiGe de 20 nm et d'une concentration en Ge ciblée de 25% ont d'abord été déposé à 700 ° C au moyen du procédé sélectif à base de GeH_4, SiH_2Cl_2 et H_2 utilisé précédemment (Hartmann et al. 2002). La **Figure III.3** montre des images AFM 1x1 μm^2 des nano-piliers SiGe déposés sur le masque 43 nm ainsi que sur le masque 35 nm en utilisant le même procédé. Dans les deux cas, la croissance est sélective et les nano-piliers sont clairement définis. La croissance réalisée sur le masque de taille plus élevée présente une distribution de hauteur de nano-piliers plus uniforme, probablement en raison des dimensions moins extrêmes du masque.

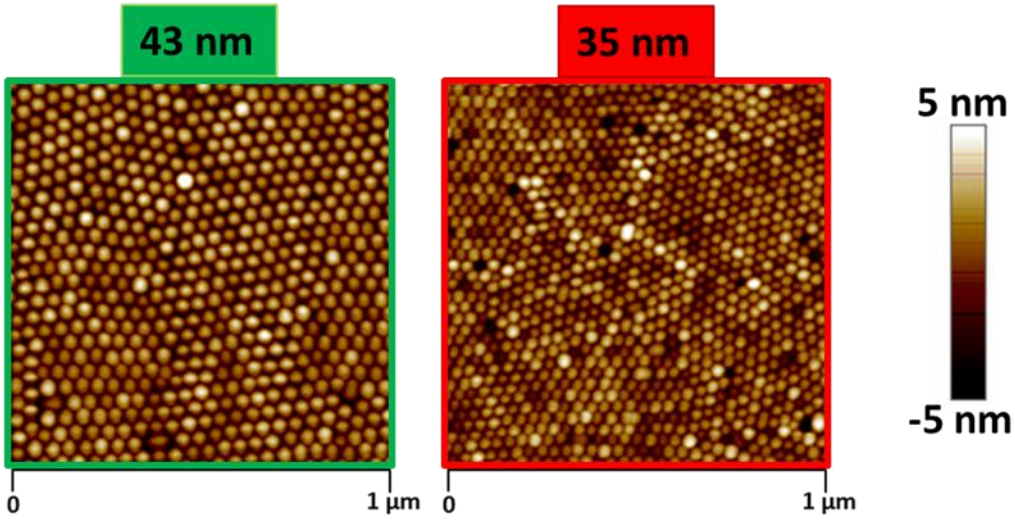

Figure III.3 Images AFM 1x1 µm² de nano-piliers SiGe déposés à 700 ° C sur les masques de période 43 nm (à gauche) et 35 nm (à droite)

Après avoir vérifié la sélectivité de notre procédé de croissance sur le nouveau masque, nous avons effectué le dépôt à 700°C de notre couche référence de SiGe 25% d'une épaisseur de 200 nm sur les nano-piliers de SiGe de 20 nm déposé à la même température. Les analyses AFM des couches réalisées sur des masques de tailles différentes montrent que Les couches sont relativement lisses avec le masque de 43 nm donnant une morphologie légèrement améliorée.

Ces couches ont été caractérisées par DRX. Le pourcentage de Ge, le degré de relaxation des contraintes ainsi que la largeur à mi-hauteur des pics associés à ces couches sont retranscrits dans le **Tableau III.1**

Mask pitch size (nm)	Ge concentration (%)	Degree of relaxation (%)	FWHM (arcsec)
35	25.5	111	557
43	25.9	110	619

Tableau III.1 Concentration en Ge, degré de relaxation des contraintes et largeur à mi-hauteur des pics associés aux couches de $Si_{0.75}Ge_{0.25}$ de 220 nm d'épaisseur déposées à 700°C sur des masques avec des périodes de 43 et 35 nm.

Le pourcentage en Ge, proche de 26% sur masque 43% et à 25.5% sur masque 35 nm, est légèrement supérieure aux 25% visés sur substrat Si exempts de motifs. Ceci est probablement dû à des effets de charge (Ito et al. 1995). Les couches de SiGe sont hautement relaxées, avec un degré de relaxation supérieur à 100% dû à la différence de coefficient d'expansion thermique entre le SiGe et le Si. Ainsi, l'augmentation de la taille du masque a peu d'effet sur les couches déposées. Cependant, le passage à une taille de masque supérieure offre plus de souplesse en termes de préparation de surface (traitement de surface humide standard au lieu de la Siconi).

Une des hypothèses de génération de défauts lors de la nano-hétéroépitaxie de couches SiGe porte sur la contrainte thermique générée par le masque d'oxyde pendant la croissance. Nous avons voulu vérifier cela expérimentalement, d'abord avec une stratégie de croissance sans masque et par la suite avec un masque SiN sans contraintes.

Pour la croissance sans masque, le masque d'oxyde a été enlevé avec une gravure humide à base de HF 2% juste après la croissance sélective à 700°C de nano-piliers $Si_{0.75}Ge_{0.25}$ à 20 nm. Ensuite, notre couche de référence SiGe à 25% d'épaisseur 200 nm a été déposé à 700 ° C, précédée d'un recuit H_2 in situ à 850 ° C afin d'éliminer toute contamination de surface (Hartmann et al. 2008) (Abbadie et al. 2004). La **Figure III.4** montre des images AFM de tailles différentes d'une couche SiGe déposée sans masque d'oxyde. La surface présente une morphologie atypique et particulièrement rugueuse. Elle est organisée en grains avec une plage de variation en hauteur de 40 nm.

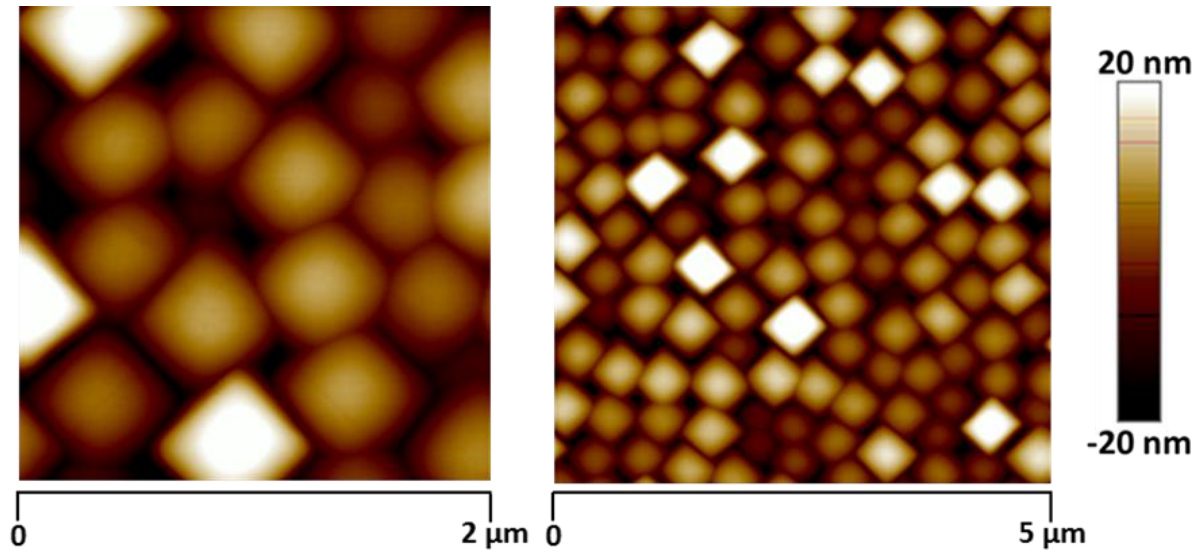

Figure III.4 Images AFM 2x2 et 5x5 µm² d'une couche de $Si_{0.75}Ge_{0.25}$ de 220 nm déposée sans masque

Une investigation a été menée dont les résultats sont présentés en **Figure III.5**. Nous nous sommes rendu compte que cela était dû au recuit à 850°C sous H_2 utilisée avant la croissance de la couche épaisse de SiGe. Sous l'effet du recuit à 850°C, les nano-piliers de SiGe se réorganisaient en grains de tailles supérieurs. Pour un recuit inférieur à 700°C, les nano-piliers de SiGe demeurent stable. Par conséquent, la couche réalisée à partir de ces nano-piliers est relativement lisse.

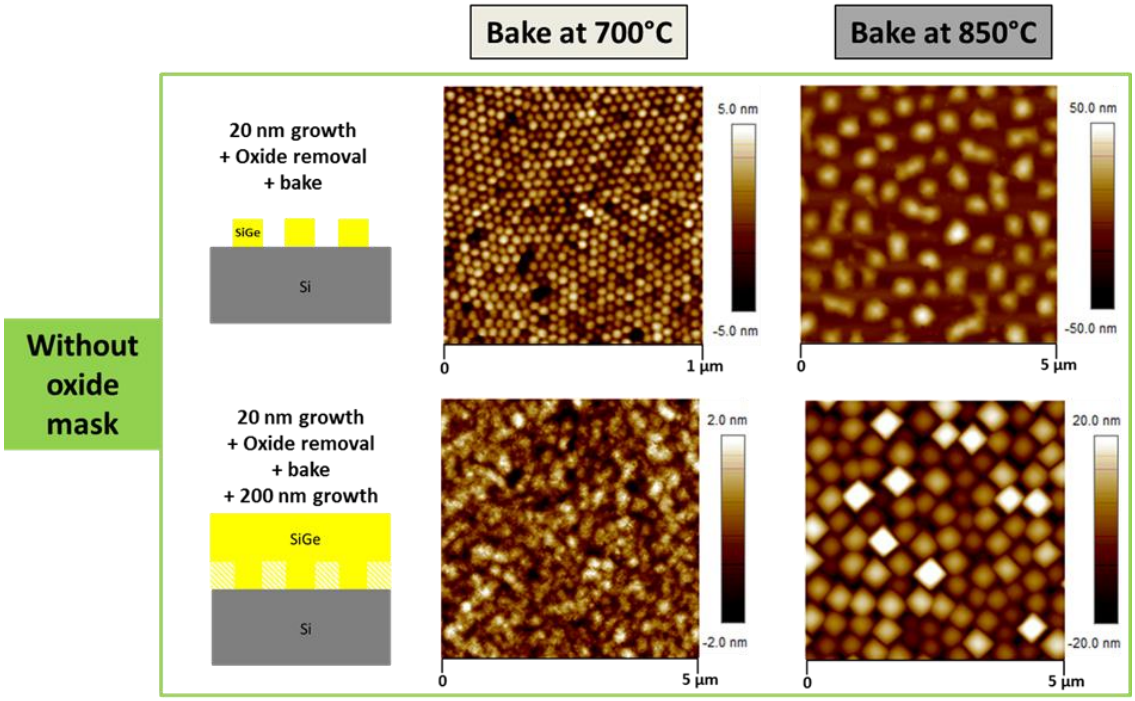

Figure III.5 Images AFM de couches de $Si_{0.75}Ge_{0.25}$ déposées sur un masque d'oxyde retiré après la première épitaxie en deux phases: (i) après une croissance sélective de nano-piliers de 20 nm de haut, le retrait du masque d'oxyde puis un recuit sous H_2 et (ii) après 20 nm de croissance sélective, l'élimination du masque d'oxyde, un recuit sous H_2 puis une autre croissance de 200 nm de SiGe. Deux températures de recuit intermédiaire ont été testées : 700°C et 850°C.

Ces couches déposées sans masque ont été caractérisées par DRX en comparaison avec la couche de référence déposée avec masque d'oxyde étudié précédemment. Le pourcentage de Ge, le degré de relaxation des contraintes ainsi que la largeur à mi-hauteur des pics associés à ces couches sont retranscrits dans le **Tableau III.2**.

Growth Scheme	Bake Temperature (°C)	Ge concentration (%)	Degree of relaxation (%)	FWHM (arcsec)
Reference With oxide mask	-	25.9	110	619
Without oxide mask	700	25.6	78	936
	850	23.2	61	1022

Tableau III.2 Concentration en Ge, degré de relaxation des contraintes et largeur à mi-hauteur des pics associés aux couches de $Si_{0.75}Ge_{0.25}$ de 220 nm d'épaisseur déposées suivant les différents schémas mentionnés.

Avec un schéma sans masque, la croissance se produit partiellement sur le substrat de silicium. Les couches épaisses se retrouvent moins relaxées que la couche de référence faite avec masque. Par ailleurs, la largeur à mi-hauteur en DRX des couches épitaxiées sans masque est supérieur à celle de la couche référence faite avec masque. Le retrait du masque n'améliore

donc ni la qualité des couches, ni la relaxation. Cette stratégie de croissance ne représente donc guère d'intérêt.

Nous avons également testé un masque en SiN sans contrainte car celui-ci a un coefficient de dilatation thermique similaire à celui du Si (Maeda and Ikeda 1998). Afin de valider le nouveau masque avec SiN, des nano-piliers de SiGe de 20 nm et d'une concentration en Ge ciblée de 25% ont d'abord été déposé à 700°C au moyen du procédé sélectif à base de GeH_4, SiH_2Cl_2 et H_2 utilisé précédemment (Hartmann et al. 2002). Une préparation de surface humide plus agressive à base de HF 2% a été nécessaire pour garantir une croissance de haute qualité, peut-être en raison de la présence de SiN résiduel au fond des cavités. La **Figure III.6** montre une image AFM de 2x2 μm^2 des nano-piliers SiGe déposés dans le nouveau masque à base de SiN. On obtient un ensemble uniforme et régulier de nano-piliers de SiGe similaire à ce qui a pu être obtenu avec le masque d'oxyde (voir **Figure III.3)**

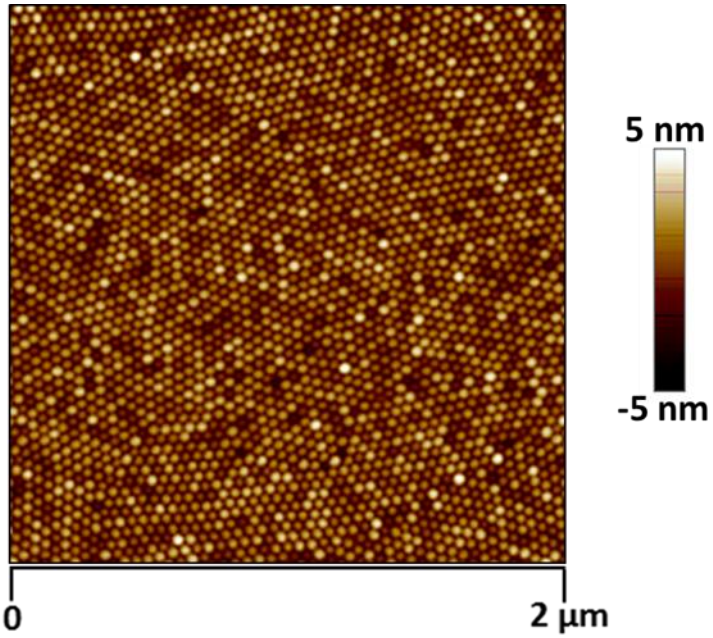

Figure III.6 Image AFM 2x2 µm2 de nano-piliers SiGe déposés à 700 ° C sur masque SiN

Après avoir vérifié la sélectivité de notre procédé de croissance sur masque SiN, nous avons effectué le dépôt à 700°C de notre couche référence de SiGe 25% d'une épaisseur de 200 nm sur des nano-piliers de SiGe de 20 nm déposé à la même température. Une comparaison a été faite avec la croissance sur masque oxyde avec les images AFM présentés en **Figure III.7** et l'analyse DRX en **Tableau III.3**. Les analyses AFM montrent que la couche formée sur le masque en nitrure est légèrement plus rugueuse que celle formée sur le masque en oxyde, mais est par ailleurs très similaire.

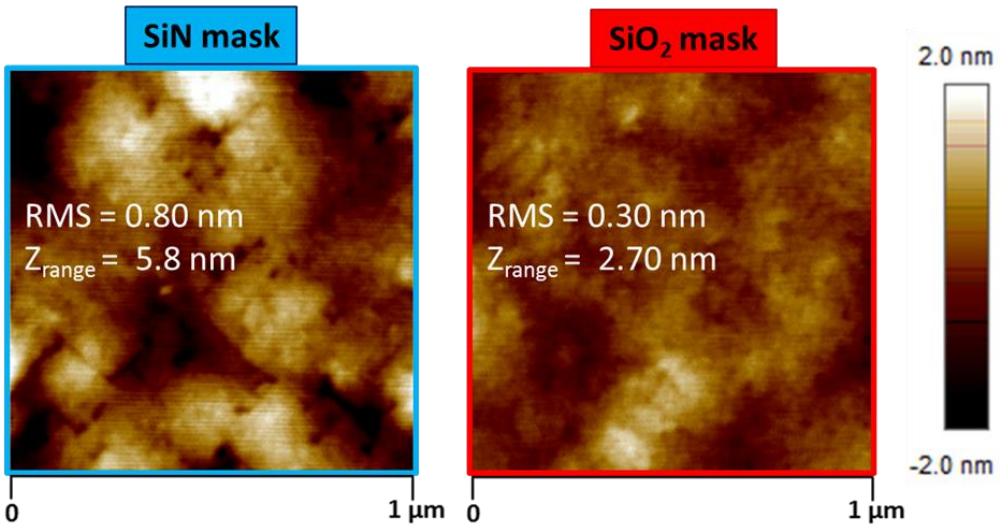

Figure III.7 Images AFM 1x1 µm² de couches $Si_{0.75}Ge_{0.25}$ de 220 nm déposées sur masques nitrure et oxyde avec valeurs correspondantes de rugosité RMS et de plage en hauteur Z.

D'après les données DRX, les deux échantillons sont équivalents en termes de composition, de contrainte et de largeur à mi-hauteur des pics. Ces résultats laissent donc penser que la contrainte thermique due au refroidissement après croissance n'est pas l'effet principal entrainant la génération de défauts lors de la nano-hétéroépitaxie de couches de SiGe.

Mask nature	Ge concentration (%)	Degree of relaxation (%)	FWHM (arcsec)
SiN	25.4	109	662
SiO_2	25.9	110	619

Tableau III.3 Concentration en Ge, degré de relaxation des contraintes et largeur à mi-hauteur des pics DRX associés aux couches de $Si_{0.75}Ge_{0.25}$ de 220 nm d'épaisseur déposées sur des masques nitrure et oxyde

Pour mieux comprendre cette génération de défauts, des observations MET en section transverse ont été effectuées sur des échantillons avec masques SiN et SiO_2. L'analyse des images MET de la **Figure III.8** suggère que les murs en nitrure séparant les nano-piliers ont une forme plus proche du schéma d'intégration souhaité par rapport à la forme triangulaire obtenue avec des parois en oxyde. Cette dernière était due à la gravure isotrope de l'oxyde lors de la préparation de la surface de type Siconi avant épitaxie. Les défauts tels que les fautes d'empilement ou les macles au sommet des murs de SiN sont comparables aux défauts observés avec les murs en SiO_2, ce qui signifie que la nature du masque n'a pas d'impact majeur sur le type de défauts. Cela renforce également le fait que les contraintes thermiques générées par le masque pendant la croissance ne sont pas une source de défauts. Les images MET montrent également une sur-gravure au niveau du Si de l'étape de gravure SiN. Cependant, cela n'affecte pas la croissance initiale car aucun défaut n'est visible à l'interface entre le substrat de Si et les nano-piliers de SiGe.

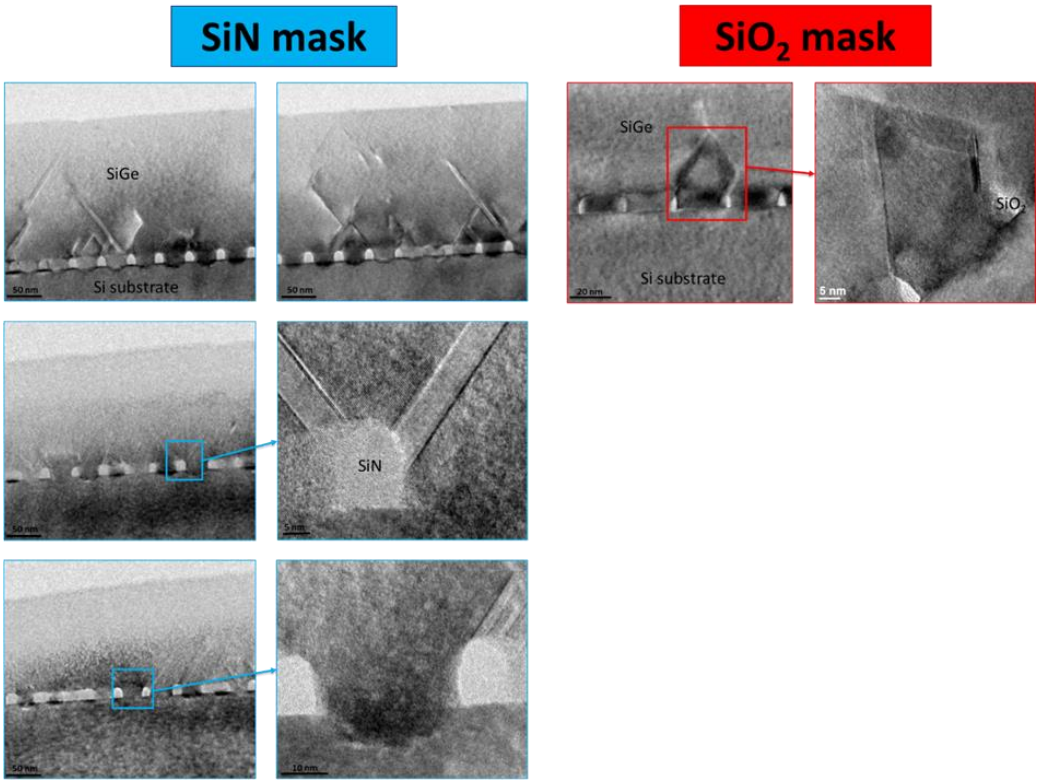

Figure III.8 Collection d'images MET haute résolution en section transverse de couches de $Si_{0.75}Ge_{0.25}$ de 220 nm d'épaisseur, déposées à 700 ° C sur des masques SiN et SiO_2.

IV. Nano-hétéroépitaxie de films Ge

Cette dernière étude porte sur l'évaluation de la nano-hétéroépitaxie pour un nouveau matériau : le Ge pur. Un des aspects importants de cette étude est de voir comment la nature du matériau déposé peut impacter la défectivité.

Pour cette étude, nous nous sommes basés sur le schéma d'intégration représenté en **Figure IV.1**. Ce schéma fait appel à un masque d'oxyde nano-structuré de période 43 nm comme utilisé précédemment.

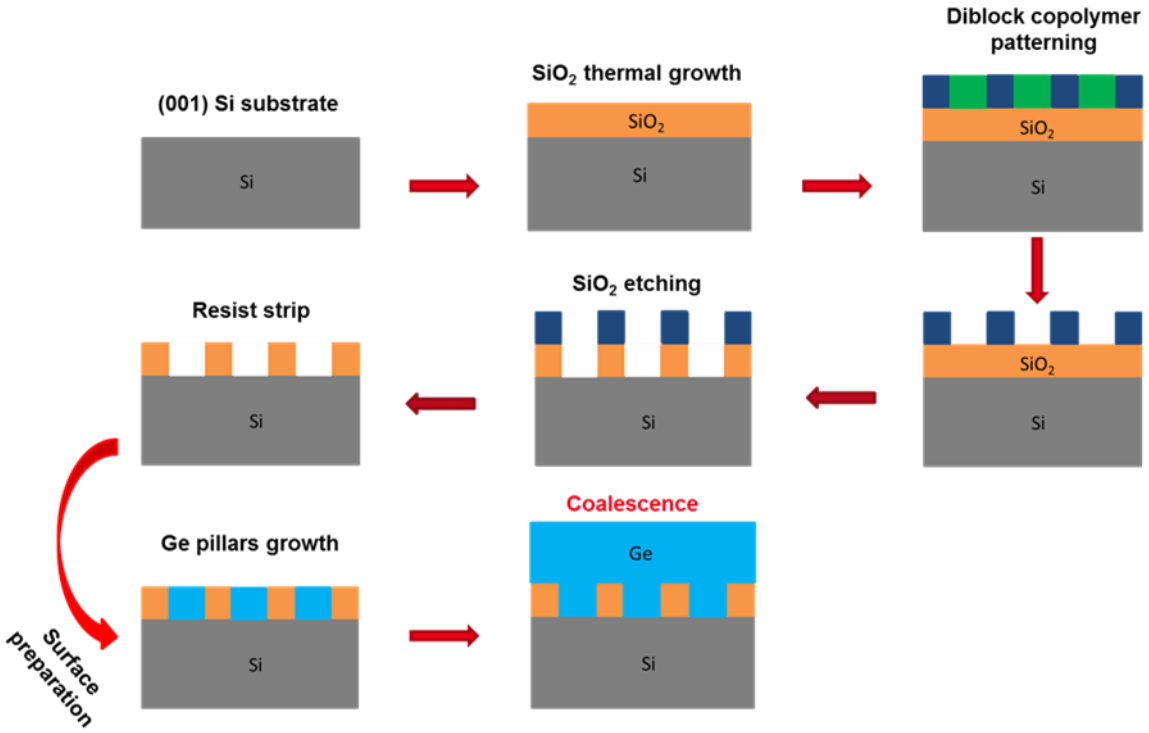

Figure IV.1 schéma d'intégration pour la nano-hétéroépitaxie de Ge

La croissance de nano-piliers de Ge de différentes épaisseurs a été d'abord explorée afin de valider la sélectivité de la croissance et d'évaluer le phénomène de coalescence. Les épaisseurs ont été déduites de vitesses de croissance de couches de Ge déposée sur des plaques de Si (001) massif. Des couches épaisses de Ge ont ensuite été déposées sur des substrats Si massifs ainsi que des substrats nano-structurés afin de comparer les deux approches. À cet effet, nous avons utilisé un bâti d'épitaxie ASM Epsilon 3200 à une pression de croissance fixée à 90 Torr. Le GeH_4 a été utilisé comme précurseur gazeux de Ge. Le débit du gaz vecteur : H_2 purifié, de plusieurs dizaines de litres par minute, n'a pas été modifié lors des différentes croissances. Le Tableau IV.1 résume les températures, les rapports de flux ainsi que et les vitesses de croissance des divers procédés utilisés pour la croissance de Ge.

Growth temperature (°C)	$[GeH_4]/[H_2]$	Growth rate (nm/min)
400	0.001	10
600		78
650	0.00056	45

Tableau IV.1 Température, rapport de flux et vitesse de croissance des procédés utilisés pour la croissance du Ge (à 90 torr avec du GeH_4).

Des piliers de Ge de nominalement 20, 25, 30, 35 et 40 nm d'épaisseur ont été déposés à 400°C dans les fenêtres en Si de taille nanométrique. Les images AFM de ces échantillons sont présentées **Figure VI.2**. Le schéma de croissance est différent de celui observé avec les nano-piliers SiGe. Aucun nano-pilier ne peut être distingué pour une croissance allant jusqu'à 30 nm, ce qui implique un retard dans la croissance de Ge dans les nano-cavités. À 35 nm, les nano-piliers peuvent être clairement identifiés, mais ils ne sont pas aussi homogènes et bien définis que les nano-piliers de SiGe à 20 nm étudiés précédemment. À 40 nm, les nano-piliers de Ge commencent à coalescer partiellement. Le retard de croissance jusqu'à 30 nm a été confirmé par l'absence de pics Ge en mesures DRX. Comme prévu, les mesures DRX montrent que les échantillons à 35 nm et 40 nm sont totalement relaxées.

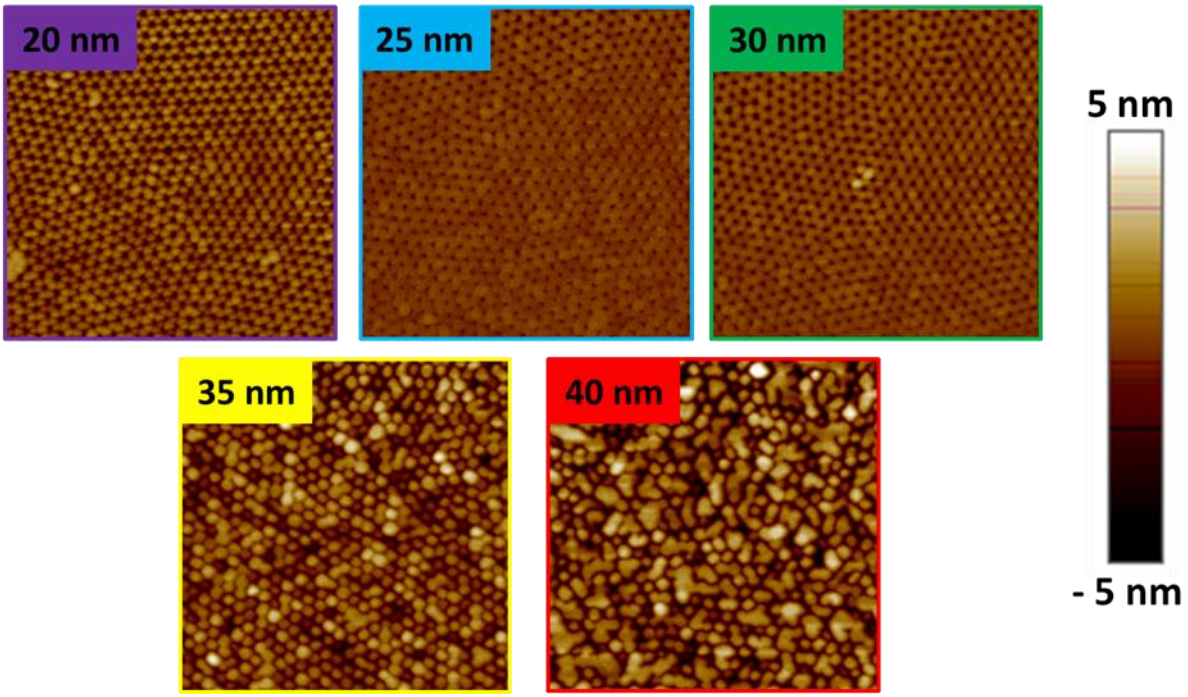

Figure IV.2 Images AFM 1 x 1 µm² de nano-piliers de Ge déposés à 400 ° C avec des épaisseurs nominales de 20 nm (violet), 25 nm (bleu), 30 nm (vert), 35 nm (jaune) et 40 nm (rouge)

Afin de réaliser une croissance de nano-piliers bien définis à 20 nm (comme pour les nano-piliers de SiGe), la vitesse de croissance a été augmentée de 400°C à 600°C et des piliers de Ge nominalement 20, 30 et 40 nm d'épaisseur ont été déposés. Les images AFM de ces échantillons présentés en **Figure IV.3** montrent des nano-piliers de Ge à 20 nm bien définis et homogènes en terme de taille. On obtient aussi un schéma de coalescence similaire à celui des nano-piliers de SiGe avec quelques nano-piliers de Ge à 30 nm qui ont commencé à fusionner avec leurs voisins. A 40 nm, tous les nano-piliers initiaux ont fusionné et les conglomérats prennent différentes formes et tailles.

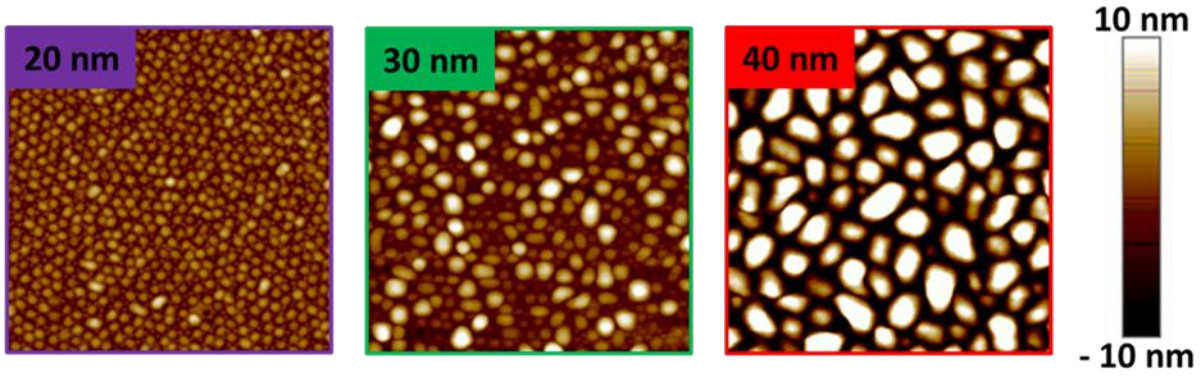

Figure IV.3 Images AFM 1 x 1 µm² de nano-piliers de Ge déposés à 600 ° C avec des épaisseurs nominales de 20 nm (violet), 30 nm (vert) et 40 nm (rouge)

Ces échantillons ont été caractérisés par DRX. Les degrés de relaxation des contraintes de ces échantillons sont retranscrits dans le **Tableau IV.1.** Comme prévu, les échantillons sont tous relaxés. Une légère contrainte en tension apparait à partir de 30 nm. Cela est probablement dû à la différence de coefficient d'expansion thermique entre le Ge et le Si qui rajoute de la contrainte lors du refroidissement de la température après croissance.

Thickness (nm)	Degree of strain relaxation (%)
20	100
30	101
40	101

Tableau IV.1 Degrés de relaxation des contraintes pour des nano-piliers de Ge déposées à 600°C

Pour mieux comprendre leurs propriétés structurelles, des observations MET en section transverse présentées en Figure **IV.4** ont été effectuées sur les nano-piliers de Ge à 20 nm déposés à 600°C. Les images MET en haute résolution des nano-piliers de Ge montrent un facettage caractéristique à la croissance épitaxiale sélective de Ge (Park et al. 2008), avec des

facettes {113} clairement visibles en surface des nano-piliers. Contrairement aux nano-piliers de SiGe, certains des nano-piliers de Ge présentent des défauts étendus commençant à l'interface avec le substrat de Si. Le contraste périodique à l'interface entre les nano-piliers de Ge et le substrat de Si est probablement dû à un réseau régulier de dislocations coins. Ceci est tout à fait logique car l'épaisseur critique du Ge sur silicium est très faible (4 nm, généralement) et les piliers sont trop grands pour supporter la contrainte sans générer de dislocations (Luryi et Suhir, 1986). Il existe un contraste, et donc une dislocation coin tous les 10 nm à peu près. Ceci est également observé pour la croissance de germanium sur silicium massif (Hartmann et al. 2004).

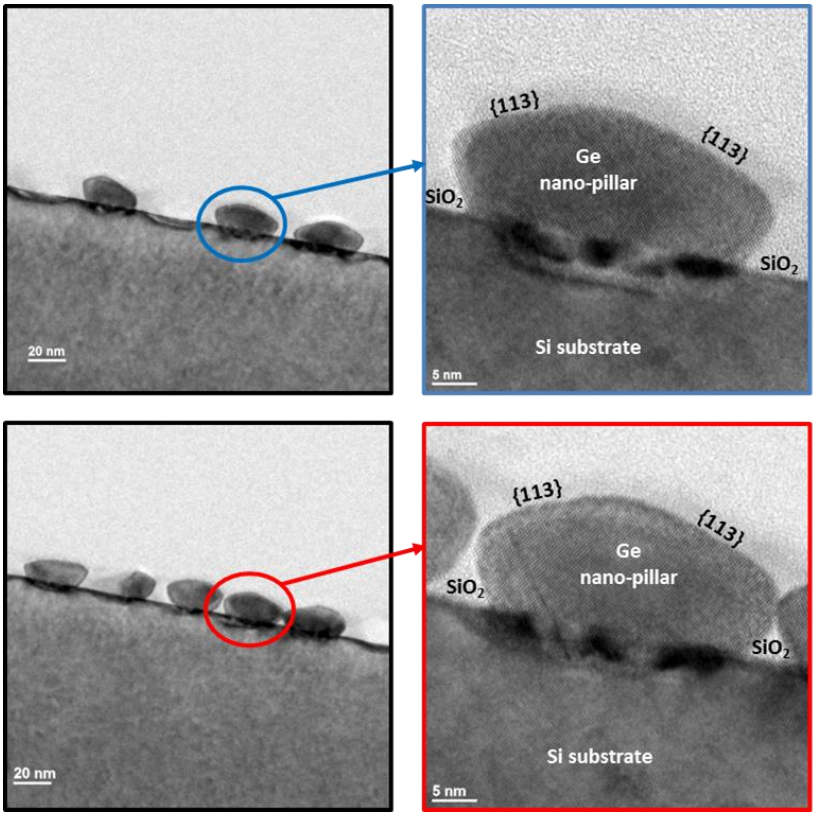

Figure IV.4 Images MET en hautes résolutions de nano-piliers de Ge de 20 nm déposés à 600°C

La croissance de couches Ge de 600, 1050 et 1500 nm d'épaisseur a été réalisée sur substrats Si massifs ainsi que sur substrats nano-structurés. Pour cela, nous avons utilisé une approche basse température/haute température, qui est la méthode la plus largement utilisée pour la réalisation de couches Ge sur substrats Si massifs. Cette approche commence par une croissance de 150 nm à 400°C suivi d'un recuit de 10 secondes à 750°C pour lisser la surface. L'étape de croissance à basse température est maintenue à 400°C malgré le retard observé pour la croissance des nano-piliers. Ce choix a été motivé pour les raisons suivantes: (i) 400°C est la température généralement utilisée sur substrat massif de Si, (ii) Le retard de croissance n'est pas réellement ressenti car une épaisseur nominale de 150 nm de Ge a été épitaxiée, et (iii) Les nano-piliers de Ge étaient plutôt uniformes pour 35 nm de Ge et commençaient à coalescer correctement après une croissance de 40 nm. Le reste de la couche de Ge a été

déposée à 650 ° C, suivi de trois cycles thermiques (sous H_2). Chaque cycle consiste en un recuit de 10 secondes à 850 ° C, suivi d'une descente de température à 650 ° C, d'une étape de 10 secondes à 650°C et d'une remontée en température jusqu'à 850°C. Ce cyclage thermique réduit généralement d'un facteur 3 à 5 la densité de dislocations émergentes dans la couche de Ge.

Les images AFM de ces échantillons sont représentées en **Figure IV.5**. Les couches de Ge déposées sur substrats massifs sont beaucoup plus lisses que celles déposées sur substrats nano-structurés (l'échelle en hauteur z est très différente entre les deux ensembles d'échantillons). Avec la présence de trous de taille micrométriques, Il semble que les couches épaisses de Ge déposées à partir nano-cavités n'aient pas encore coalescées complétement.

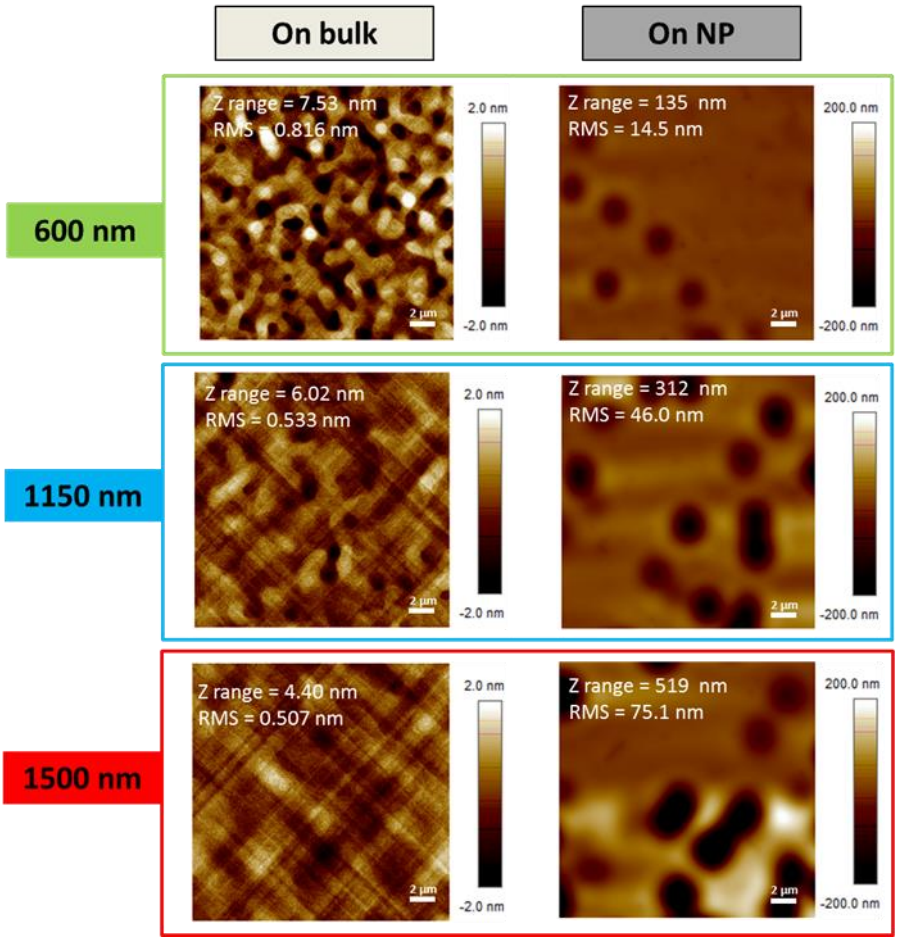

Figure IV.5 Images AFM 20 x 20 µm² de couches de Ge à 600, 1150 et 1500 nm d'épaisseur réalisées sur substrats et nano-structurés (NP)

Ces échantillons ont été caractérisés par DRX. Le degré de relaxation des contraintes ainsi que la largeur à mi-hauteur de ces couches sont retranscrits dans le **Tableau IV.2**. Les couches de Ge déposées sur substrats massifs et nano-structurés présentes des valeurs de degrés de relaxation et des largeurs à mi-hauteur très similaires. Cela suggère que, contrairement aux couches de SiGe, la densité de défauts est dominée par la génération de dislocations coins à l'interface silicium-germanium, sans impact clair du phénomène de coalescence.

Thickness (nm)	Wafer type	Degree of strain relaxation (%)	FWHM (arcsec)
600	Bulk	104	183
	NP	105	190
1050	Bulk	104	143
	NP	104	149
1500	Bulk	104	128
	NP	104	152

Tableau IV.2 Résultats DRX obtenus sur des couches de Ge de 600, 1150 et 1500 nm d'épaisseur déposées avec une approche basse température / haute température des substrats massifs et nano-structurés (NP).

Des observations MET en section transverse ont été effectuées sur la couche de Ge coalescée à 600 nm afin d'évaluer les mécanismes de génération de défauts. L'analyse des images MET de la **Figure IV.6** suggère que la coalescence de Ge génère le même type de défauts (mâcles et fautes d'empilement) commençant au sommet (cadre violet) et aux bords (cadre rouge) des murs en oxyde ainsi qu'à l'interface entre le substrat de Si et la couche de Ge (cadre bleu). Ceci est assez similaire à ce qui a été obtenu pour les couches de SiGe. Cependant, ces défauts n'ont pas d'effet significatif sur la largeur à mi-hauteur en DRX. Ceci peut-être en raison d'une meilleure recombinaison des défauts dans le Ge par rapport au SiGe.

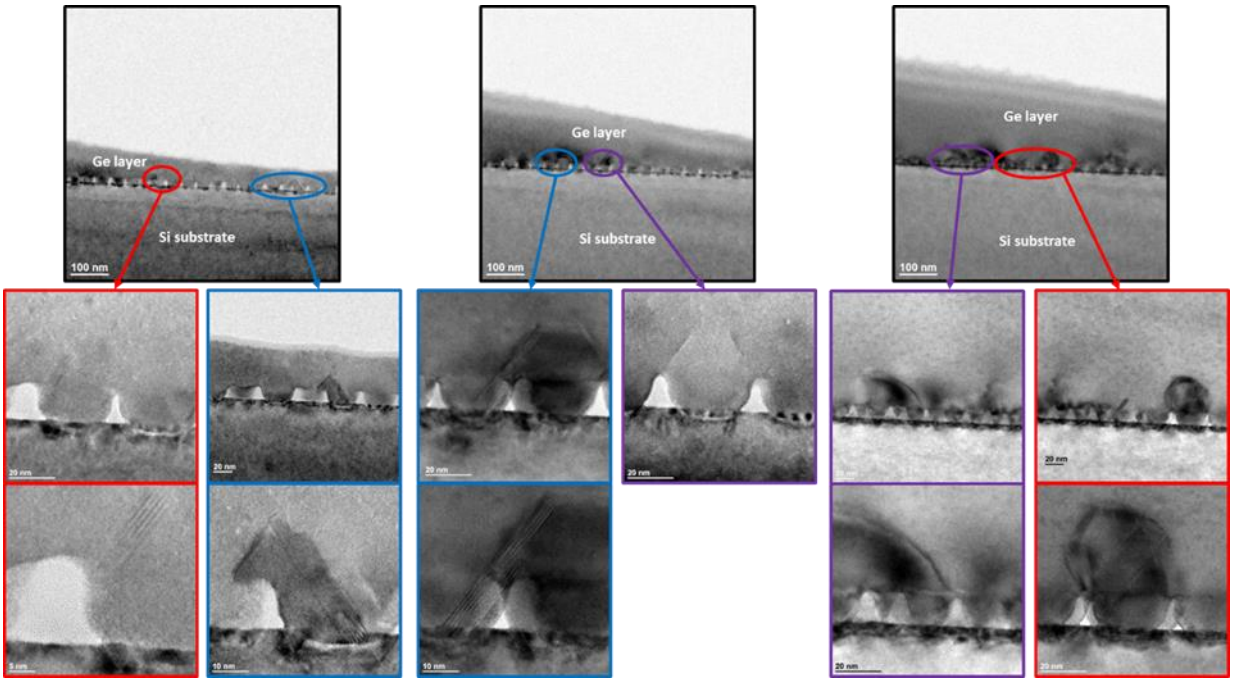

Figure IV.6 Images MET en haute résolution d'une couche de Ge coalescée à 600 nm d'épaisseur

Conclusion

La nano-hétéroépitaxie, nouvelle approche de croissance épitaxiale à partir de substrats nano-structurés, a été explorée durant cette thèse. Le contexte de ce travail étant le silicium contraint, l'idée principale était d'obtenir un substrat virtuel fin de SiGe en s'appuyant sur une méthode qui offre des degrés supplémentaires de relaxation des contraintes par rapport aux approches classiques telles que les rampes en concentration en Ge. Il a donc fallu d'abord concevoir un schéma de fabrication de substrats nano-structurés basé sur la lithographie de copolymères à blocs. La croissance de couches SiGe par nano-hétéroépitaxie a ensuite été explorée sous divers angles à l'aide d'un bâti industriel de dépôt chimique en phase vapeur à pression réduite.

Dans un premier temps, nous avons étudié la nano-hétéroépitaxie de couches SiGe sur deux types de nano-piliers : Si et SiGe. Le schéma d'intégration conçu, basé sur la lithographie à copolymères à bloc, a permis d'obtenir un masque d'oxyde de taille nanométrique avec une configuration hexagonale compacte. L'épitaxie sélective des nano-piliers en Si a été étudiée en premier lieu. Un procédé sélectif et homogène en terme de hauteur des nano-piliers, a été obtenu grâce à l'utilisation d'une préparation de surface de type Siconi (plasma déporté de NH_3 / NF_3). Pour les nano-piliers en SiGe, un procédé similaire a été obtenu pour des températures de croissance comprises entre 650°C et 700°C. Les couches de SiGe réalisées par la suite sur ces nano-piliers de Si et SiGe présentaient des surfaces lisses et des degrés élevés de relaxation des contraintes. Cependant, Les caractérisations DRX et MET ont montré que ces couches présentaient des défauts. Elles ont démontré par ailleurs que l'utilisation de nano-piliers de SiGe permettait d'obtenir des couches de meilleure qualité. En termes de défectivité, les couches présentaient des fautes d'empilement et des macles partant généralement de l'interface entre les piliers et la couche de SiGe et juste au-dessus des murs d'oxyde. Trois hypothèses ont été émises concernant cette génération de défauts: (i) la croissance sur les facettes {111} des nano-piliers pouvant générer des macles (ii) le processus de coalescence des nano-piliers et (iii) la contrainte thermique générée par le masque d'oxyde pendant la croissance.

Nous avons ensuite étudié la coalescence de nano-piliers SiGe aux premiers stades de la croissance afin d'évaluer une des hypothèses précédentes. Des nano-piliers $Si_{0.75}Ge_{0.25}$ de 20 à 35 nm de hauteur ont été déposés sélectivement à l'aide d'une chimie chlorée. La coalescence des nano-piliers a d'abord été examinée en AFM. À partir de 30 nm, les grains de coalescences prennent différentes formes en fonction du nombre de nano-piliers coalescées, ce qui rend le processus de coalescence assez hétérogène. En utilisant la DRX, nous avons constaté que la relaxation des contraintes augmentait avec l'épaisseur, atteignant des valeurs à 91% pour des piliers partiellement coalescés d'une épaisseur de 35 nm seulement. Ceci confirme que la croissance à partir de nano-cavités entraine une relaxation très rapide des contraintes présentes dans le film SiGe. En termes de composition chimique, aucune variation n'a été enregistrée pour cette gamme d'épaisseurs. La SSRM a permis de mesurer l'activité électrique des nano-piliers. À 20 nm, la distinction électrique entre les nano-piliers et le masque en oxyde était évidente et la résistance électrique des piliers était très uniforme. À 35

nm, des variations de résistivité locale ont été détectées au sein des grains de nano-piliers coalescées. Ceci pourrait indiquer la présence de défauts cristallins au sein de ces structures. Enfin, des images MET ont été réalisés afin d'étudier la génération de défauts cristallins lors de la coalescence. L'imagerie MET de l'échantillon à 20 nm a montré des nano-piliers facettés et exempts de défauts. L'analyse de l'échantillon à 35 nm a montré plusieurs cas de figure allant de la coalescence sans défauts à la génération de fautes d'empilement et de macles aux premiers stades de la coalescence.

L'impact du masque sur la nano-hétéroépitaxie de couches SiGe a également fait l'objet d'une étude. L'impact de la taille du masque a d'abord été étudié. Nous sommes ainsi passés d'un masque de période 35 nm à un masque de période 43 nm avec des murs d'oxydes un peu plus larges. Un procédé sélectif d'épitaxie a été obtenu à 700 ° C sur le nouveau masque avec l'utilisation au préalable d'une préparation de surface humide standard ozone/HF (au lieu de la Siconi qui était nécessaire pour le masque de 35 nm). Les couches de SiGe obtenues sur le nouveau masque étaient équivalentes en termes de de composition et de structure à celles du masque initial. Un masque de taille plus élevée offre ainsi plus de flexibilité en termes de préparation de la surface, sans impact sur la qualité des couches. Afin de répondre à la problématique liée à la contrainte thermique générée par la présence du masque en oxyde, une approche de croissance sans masque a été explorée en plus de l'utilisation d'un masque en SiN sans contrainte. Pour ce faire, le masque d'oxyde a été retiré après la croissance sélective de nano-piliers de SiGe, suivi de la croissance d'une couche de SiGe ayant la même concentration en Ge. Les résultats ont montré une morphologie de surface dégradée en raison du recuit à 850°C précédant la croissance de la couche de SiGe de 200 nm d'épaisseur. Avec un recuit à seulement 700°C, la couche obtenue était bien lisse ; cependant, elle était moins relaxée et présentait une largeur à mi-hauteur supérieure à celle obtenue avec présence d'un masque. Le retrait du masque ne présente donc aucun avantage pour nos couches. L'usage d'un masque en SiN a également été testé. Du fait de la bonne adéquation de coefficient de dilatation thermique entre SiN et silicium, un masque SiN était moins susceptible de générer des contraintes dues au refroidissement post croissance. Un procédé sélectif a été obtenu sur ce nouveau masque, et les résultats AFM et DRX ont indiqué que les couches SiGe réalisées sur le masque en nitrure étaient similaires à celles obtenues sur le masque en oxyde. En termes de défectivité, l'imagerie MET a montré que la nature du masque n'avait aucun impact sur le type de défauts, ce qui prouve aussi que la contrainte thermique générée par le masque pendant la croissance n'est pas une source de défauts.

Enfin, l'approche par nano-hétéroépitaxie a été testée sur du Ge pur. La croissance des nano-piliers de Ge a d'abord été étudiée. Les résultats ont montré une croissance retardée de nano-piliers de Ge à 400°C. Les nano-piliers obtenus après la croissance nominale de 35 nm n'étaient pas aussi homogènes et bien définis que les nano-piliers à 20 nm de SiGe étudié précédemment. Le fait d'augmenter la température de croissance à 600°C a permis d'obtenir un procédé hautement sélectif et uniforme, avec des nano-piliers de Ge homogènes et bien définis pour une épaisseur de croissance nominale de 20 nm. Un schéma de coalescence standard des nano-piliers a également été observé à cette température de croissance. L'imagerie MET de l'échantillon de 20 nm déposé à 600°C a montré des nano-piliers de Ge à facettes, avec de nombreuses dislocations coins à l'interface Ge/Si. Des couches épaisses de

Ge ont ensuite été déposées à l'aide d'une stratégie basse température/haute température sur substrats Si massifs ainsi que sur substrats nano-structurés, à des fins de comparaison. Alors que les couches de Ge sur silicium étaient très lisses, l'analyse AFM a montré des trous de taille micrométrique à la surface des couches Ge déposés sur substrats nano-structurés. Ceci pourrait être dû à une coalescence incomplète des couches de Ge. L'analyse MET d'une couche Ge de 600 nm déposée sur substrat nano-structuré suggère que la coalescence entraîne des défauts planaires de type macle et fautes d'empilement commençant aux murs d'oxyde (comme en SiGe). De plus, des dislocations coins sont présentes à l'interface Ge/Si. Malgré ces différences morphologiques, des propriétés structurelles similaires (en termes de degré de relaxation des contraintes et de largeur à mi-hauteur) ont été déduites des analyses DRX pour les couches déposées sur substrats nano-structurés et substrats massifs.

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ANNEX II:
Valorization

✓ Articles in peer-reviewed journals:

1. M. Mastari, M. Charles, Y. Bogumilowicz, Q.M. Thai, P. Pimenta-Barros, M. Argoud, A.M. Papon, P. Gergaud, D. Landru, Y. Kim, J.M. Hartmann, *SiGe nano-heteroepitaxy on Si and SiGe nano-pillars*, Nanotechnology. 29 (2018) 275702.

2. M. Mastari, M. Charles, Y. Bogumilowicz, P. Pimenta-Barros, M. Argoud, R. Tiron, A.M. Papon, D. Muyard, N. Chevalier, D. Landru, Y. Kim, J.M. Hartmann, *Nano-Heteroepitaxy: An Investigation of SiGe Pillars Coalescence*, ECS J. Solid State Sci. Technol. 8 (2019) P180–P185.

3. M. Mastari, M. Charles, P. Pimenta-Barros, M. Argoud, R. Tiron, A.M. Papon, D. Landru, Y. Kim, O. Kononchuck, J.M. Hartmann, *SiGe nano-heteroepitaxy: An investigation of the nano-template*, J. Cryst. Growth. 527 (2019) 125232.

4. M. Mastari, M. Charles, P. Pimenta-Barros, M. Argoud, R. Tiron, A.M. Papon, D. Muyard, N. Chevalier, D. Landru, Y. Kim, O. Kononchuck, J.M. Hartmann, *Ge nano-heteroepitaxy: from nano-pillars to thick coalesced layers*, Submitted

✓ Conference proceedings:

M. Mastari, M. Charles, Y. Bogumilowicz, P. Pimenta-Barros, M. Argoud, R. Tiron, A.-M. Papon, D. Muyard, N. Chevalier, D. Landru, Y. Kim, J.-M. Hartmann, *Nano-Heteroepitaxy: An Investigation of SiGe Nano-Pillars Coalescence*, ECS Trans. 86 (2018) 249–258.

✓ Oral presentations in international conferences:

1. *SiGe nano-heteroepitaxy on Si and SiGe nano-pillars*, **M. Mastari, M. Charles, Y. Bogumilowicz, Q.M. Thai, P. Pimenta-Barros, M. Argoud, A.M. Papon, P. Gergaud, D. Landru, Y. Kim, O. Kononchuck, J.M. Hartmann**, 1st Joint ISTDM / ICSI 2018 Conference [9th International SiGe Technology and Device Meeting (ISTDM) / 11th International Conference on Silicon Epitaxy and Heterostructures (ICSI)], Potsdam (Germany) 2018.

2. *Nano-Heteroepitaxy: An Investigation of SiGe Nano-Pillars Coalescence*, **M. Mastari, M. Charles, Y. Bogumilowicz, P. Pimenta-Barros, M. Argoud, R. Tiron, A.-M. Papon, D. Muyard, N. Chevalier, D. Landru, Y. Kim, J.-M. Hartmann**, AiMES 2018 ECS and SMEQ Joint International Meeting, Cancun (Mexico) 2018.

3. *SiGe nano-heteroepitaxy: An investigation of the nano-template*, **M. Mastari, M. Charles, P. Pimenta-Barros, M. Argoud, R. Tiron, A.M. Papon, D. Landru, Y. Kim, O. Kononchuck, J.M. Hartmann**, 2nd Joint ISTDM / ICSI 2019 Conference [10th International SiGe Technology and Device Meeting (ISTDM) / 12th International Conference on Silicon Epitaxy and Heterostructures (ICSI)], Madison-Wisconsin (USA) 2019.

4. *Ge nano-heteroepitaxy: from nano-pillars to thick coalesced layers* **M. Mastari, M. Charles, P. Pimenta-Barros, M. Argoud, R. Tiron, A.M. Papon, N. Chevalier, D. Landru, Y. Kim, O. Kononchuck, J.M. Hartmann**, 2019 E-MRS Fall Meeting, Warsaw (Poland) 2019.

✓ Awards:

Best Student Presentation Award for *"Nano-Heteroepitaxy: An Investigation of SiGe Nano-Pillars Coalescence"* AiMES 2018 ECS and SMEQ Joint International Meeting, Cancun (Mexico) 2018.

TITLE: Growth and characterization of SiGe alloys on nanometer-size structures for microelectronics applications

Nano-heteroepitaxy is a promising approach for the growth of high quality, thin and fully strain relaxed SiGe layers (for strained Si devices). First theorized by Luryi and Suhir, the idea is to start the growth from sufficiently small nano-pillars so that the layer can relax faster, elastically, and then coalesce without generating additional defects. In this PhD, an integration scheme based on diblock copolymer patterning was used to fabricate nanometer-sized templates, on which SiGe nano-heteroepitaxy was explored using a 300 mm industrial Reduced Pressure-Chemical Vapor Deposition tool. $Si_{0.75}Ge_{0.25}$ nano-heteroepitaxy on Si and $Si_{0.75}Ge_{0.25}$ nano-pillars was first studied. Results showed highly selective and uniform processes based on a chlorinated chemistry for the epitaxial growth of 20 nm high Si and $Si_{0.75}Ge_{0.25}$ nano-pillars. Smooth surfaces and full strain relaxation were obtained in the 650-700°C range for 200 nm thick $Si_{0.75}Ge_{0.25}$ layers grown both types of nano-pillars. However, planar defects (twins and stacking faults) were identified as occurring during the coalescence process. Therefore, $Si_{0.75}Ge_{0.25}$ nano-pillars coalescence was investigated. The evolution in terms of grain shape, size and number was examined, with individual pillars merging into larger grains for thicknesses above 30 nm. High degrees of macroscopic strain relaxation were obtained at the different stages of nano-pillars merging. Defects such as stacking faults and twins appeared at the early stages of nano-pillars coalescence. The impact of the nano-template used for the nano-heteroepitaxy of $Si_{0.75}Ge_{0.25}$ layers was also evaluated. Various integration schemes were designed in order to measure the impact of pitch, the presence (or not) of the nano-template during coalescence and the nature of the masking material itself. Results showed more flexibility in terms of surface preparation with higher pitch size nano-templates. Removal of the nano-template did not improve the relaxation of coalesced layers. Changing the nature of masking material in the nano-template (SiO_2 versus strain free SiN) proved that the thermal stress generated during growth was not a source of defects. The nano-heteroepitaxy approach was extended to pure Ge. Results showed a highly selective and uniform process for the epitaxial growth of Ge nano-pillars at 600°C. A degraded surface morphology, with otherwise similar structural properties, were obtained for 2D Ge layers grown on Ge nano-pillars compared with growth on bulk Si. Usual coalescence related defects were once again found.

KEYWORDS : nano-heteroepitaxy, reduced pressure – chemical vapor deposition; selective epitaxial growth, patterned substrates, SiGe alloys, crystalline defects.

TITRE: Croissance et caractérisation d'alliages SiGe sur des structures de tailles nanométriques pour des applications en micro-électronique

La nano-hétéroépitaxie est une approche innovante pour la croissance de couches minces de SiGe totalement relaxées et de bonne qualité (pour des dispositifs à base de Si contraint). Mise en théorie par Luryi et Suhir, l'idée est de commencer la croissance à partir de nano-piliers suffisamment petits pour que la couche puisse se relaxer rapidement et de manière élastique, puis coalescer sans générer de défauts. Dans cette thèse, un schéma d'intégration basé sur la lithographie à copolymère à bloc a été utilisé afin de fabriquer des masques de taille nanométrique, sur lesquels la nano-hétéroépitaxie de SiGe a été explorée à l'aide d'un bâti industriel 300 mm de dépôt chimique en phase vapeur à pression réduite. La nano-hétéroépitaxie de couches $Si_{0.75}Ge_{0.25}$ sur nano-piliers Si et $Si_{0.75}Ge_{0.25}$ a d'abord été étudiée. Des procédés hautement sélectifs et uniformes à base de chimie chlorée ont été développés pour la croissance de nano-piliers Si et $Si_{0.75}Ge_{0.25}$ faisant 20 nm d'épaisseur. Des surfaces lisses et une relaxation totale des contraintes ont été obtenues dans la plage de 650 à 700°C pour des couches de 200 nm de $Si_{0.75}Ge_{0.25}$ déposées sur les deux types de nano-piliers. Cependant, des défauts planaires (macles et fautes d'empilement) dont l'origine pourrait être le processus de coalescence, ont été identifiés. Par conséquent, la coalescence de nano-piliers $Si_{0.75}Ge_{0.25}$ a été étudiée. L'évolution en termes de forme, de taille et de nombre de grains formés par la coalescence a été examinée. Des degrés élevés de relaxation des contraintes ont été obtenus aux différents stades de la coalescence des nano-piliers. Les défauts de type fautes d'empilement et macles sont apparus aux premiers stades de la coalescence. L'impact du masque utilisé pour la nano-hétéroépitaxie des couches de $Si_{0.75}Ge_{0.25}$ a également été évalué. Différents schémas d'intégration ont été conçus pour mesurer l'impact de la taille, la présence (ou non) du masque lors de la coalescence ainsi que le matériau de masquage. Les résultats ont montré plus de flexibilité en termes de préparation de surface avec un masque de taille plus élevée. La relaxation des couches a été dégradée par l'absence de masque. Le changement de matériau de masquage (SiN sans contrainte au lieu de SiO_2) a démontré que la contrainte thermique générée par le masque lors de la croissance n'était pas une source de défauts. L'approche par nano-hétéroépitaxie a également été testée sur Ge pur. Un procédé hautement sélectif et uniforme à 600°C a été développé pour la croissance de nano-piliers de Ge. Une morphologie de surface dégradée, avec des propriétés structurelles assez similaires, ont été obtenus pour des couches Ge déposées sur substrats masqués par rapport à des couches Ge déposées sur Si massif. Les défauts habituels liés à la coalescence ont de nouveau été retrouvés.

MOTS CLES : nano-hétéroépitaxie, dépôt chimique en phase vapeur à pression réduite, croissance épitaxiale sélective, substrats masqués, alliages SiGe, défauts cristallins.