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Axel Pic

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Numerical and experimental investigations of self-heating phenomena in 3D Hybrid Bonding imaging technologies

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Abstract

English

In this PhD thesis, self-heating phenomena are studied for guiding the design of next-generation 3D Integrated Circuits (ICs). By means of experimental and numerical investigations, associated heat dissipation in 3D Hybrid Bonding imagers is analyzed and the impact of the resulting temperature rise is evaluated. First, in order to develop accurate models, the thermal properties of materials used in ICs are to be determined. Different dielectric thin films involving oxides, nitrides, and low-k compounds are investigated. To do so, Scanning Thermal Microscopy (SThM) and the 3ω electrothermal method, sensitive to low and large effective thermal conductivity, are implemented. In a second step, finite-element models of 3D ICs are developed. A numerical method involving homogenization and a multiscale approach is proposed to overcome the large aspect ratios inherent in microelectronics. The numerical procedure is validated by comparing calculations and experimental measurements performed with SThM, resistive thermometry and infrared microscopy on a simplified Hybrid Bonding test chip. It is shown that heat dissipation is mainly limited by the heat sink conductance and the losses through air. Finally, numerical and experimental studies are performed on fully-functional 3D Hybrid Bonding imagers. The temperature field is measured with SThM and compared with finite-element computations at the die surface. The numerical results show that the temperature of the pixel surface is equal to that of the imager Front-End-Of-Line. The influence of the temperature rise on the optical performance of the imager is deduced from the analysis. The study also allows assessing the various numerical and experimental methods for characterizing heat dissipation in microelectronics.

French

Dans cette thèse, les phénomènes d'auto-échauffement ont été étudié pour guider la conception de circuits intégrés 3D de nouvelle génération. Grâce à des études expérimentales et numériques, la dissipation thermique dans des imageurs 3D par collage hybride a été analysée et l'impact de l'augmentation de température résultante a été évalué. Premièrement, afin de développer des modèles précis, les propriétés thermiques des matériaux utilisés dans les circuits intégrés ont dû être déterminées. Différents films minces diélectriques impliquant des oxydes, des nitrures et des composés low-k ont été étudiés. Pour ce faire, la microscopie thermique à sonde locale (SThM) et la méthode électrothermique 3ω, sensibles à la conductivité thermique effective faible et élevée, ont été mises en œuvre. Dans un deuxième temps, des modèles éléments finis de circuits intégrés 3D ont été développés. Une méthode numérique nécessitant homogénéisations et approches multi-échelles a été proposée pour surmonter des grands rapports de forme inhérents à la microélectronique. La procédure numérique a été validée en comparant les calculs et les mesures expérimentales effectuées par SThM, la thermométrie résistive et la microscopie infrarouge sur une puce de test par collage hybride simplifiée. Il a été montré que la dissipation de chaleur est principalement limitée par la conductance du puit thermique ainsi que les pertes par l'air. Enfin, des études numériques et expérimentales ont été réalisées sur des imageurs 3D par collage hybride fonctionnels. Le champ de température a été mesuré par SThM et comparé aux calculs par éléments finis à la surface de la matrice. Les résultats numériques ont montré que la température de la surface des pixels est égale à celle du Front-End-Of-Line de l'imageur. L'influence de l'échauffement sur les performances optiques de l'imageur a été déduite de cette analyse. Cette étude a permis également d'évaluer les différentes méthodes numériques et expérimentales pour la caractérisation de la dissipation de chaleur en microélectronique.

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Nomenclature

Abbreviation	Term
AC	Alternating Current
AFM	Atomic Force Microscopy
AMM	Acoustic Mismatch Model
BEOL	Back-End-Of-Line
BL	Bottom Left
BR	Bottom Right
CCD	Charge Coupled Device
CCM	Conductivity Contrast Mode
CD	Critical Dimension
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical and Mechanical Planarization
DBI	Direct Bond Interconnect
DC	Direct Current
DMM	Diffuse Mismatch Model
DTI	Deep Trench Isolation
EMA	Effective Medium Approximation
EUV	Extreme Ultraviolet
FD	Floating Diffusion
FE	Finite Element
FEA	Finite Element Analysis
FEM	Finite Element Method
FEOL	Front-End-Of-Line
FDM	Finite Difference Method
FinFET	Fin Field Effect Transistor
FWHM	Full Width at Half Maximum
HB	Hybrid Bonding
IC	Integrated Circuit
IMG	Imager
InSb	Indium Antimonide
IR	Infrared
LIA	Lock-In Amplifier
LMC	Lattice Monte Carlo
MC	Monte Carlo
MD	Molecular Dynamics
MEMS	Microelectromechanical System
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MTTF	Mean Time To Failure

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NA	Numerical Aperture
NMOS	N-channel MOSFET
PCB	Printed Circuit Board
PMOS	P-channel MOSFET
PPD	Pinned Photodiode
PTAT	Proportional To Absolute Temperature
RF	Radio-Frequency
RGB	Red, Green, Blue
RH	Relative Humidity
SEM	Scanning Electron Microscopy
SoC	System-on-Chip
SOI	Silicon-On-Insulator
SNR	Signal-to-Noise Ratio
SThM	Scanning Thermal Microscopy
STI	Shallow Trench Isolation
TBC	Thermal Boundary Conductance
TBR	Thermal Boundary Resistance
TCM	Temperature Contrast Mode
TCR	Temperature Coefficient of Resistance
TEC	Thermal Expansion Coefficient
TG	Transfer Gate
TIM	Thermal Interface Material
TL	Top Left
TR	Top Right
TSV	Through Silicon Via
TTI	Thermoreflectance Thermal Imaging
ULK	Ultra Low-k
USG	Undoped Silicon Glass
UV	Ultraviolet
WB	Wire Bonding
1D	One-Dimensional
2D	Two-Dimensional
3D	Three-Dimensional

Symbol	**Unit**	**Description**
b	m	Heater half-width
D	$m.s^{-2}$	Thermal diffusivity
E	eV	Energy
f	s^{-1}	Frequency
G	$W.K^{-1}$	Conductance
$G_{contact}$	$W.K^{-1}$	Contact conductance
g_{sink}	$W.m^{-2}.K^{-1}$	Heat sink conductance
G_{solid}	$W.K^{-1}$	Solid-solid conductance

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G_{water}	$W.K^{-1}$	Water meniscus conductance
g_{wb}	$W.m^{-2}.K^{-1}$	Wire bonding conductance
h_{air}	$W.m^{-2}.K^{-1}$	Air losses coefficient
h_{rad}	$W.m^{-2}.K^{-1}$	Radiative losses coefficient
I	A	Current
J	$A.m^{-2}$	Current density
k	$W.m^{-1}.K^{-1}$	Thermal conductivity
k_b	$m^2.kg.s^{-2}.K^{-1}$	Boltzmann constant
k_{eff}	$W.m^{-1}.K^{-1}$	Effective thermal conductivity
P	W	Power
q	C	Electron charge
Q	$W.m^{-2}$	Heat flux density
R	Ω	Electrical resistance
R_{th}	$K.m^2.W^{-1}$	Thermal resistance
S	m^2	Surface
T	K	Temperature
V	V	Voltage

Greek letter	**Unit**	**Description**
α	K^{-1}	Temperature coefficient of resistance
ΔT	K	Temperature difference
ΔR	Ω	Electrical resistance difference
ΔV	V	Voltage difference
ε	1	Emissivity
ħ	J.s	Normalized Planck constant
λ	m	Wavelength
□	m	Mean free path
ω	$rad.s^{-1}$	Angular frequency
φ	rad	Phase
ϕ	W	Heat flux
σ	$W.m^{-2}.K^{-4}$	Stefan-Boltzmann constant
θ	K	Temperature rise

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Introduction

In this PhD thesis, self-heating phenomena are studied in 3D Integrated Circuit (IC) architectures. Here, we are interested more particularly in the 3D Hybrid Bonding (HB) technology for imagers in the context of their emergence in commercial devices. Indeed, in such architectures, the imager part (top chip) is located just above the control part (bottom chip), and the temperature of pixels is therefore expected to increase due to closeness with the heat sources. The pixel performance being strongly dependent on the temperature, the thermal behavior of 3D HB object needs to be perfectly understood and controlled to avoid performance drifts. In addition, the thermal stress associated to thermal gradients and local thermal expansion can also be detrimental to operation of the device. This is why it is important today to be able to determine a priori the thermal behavior of the associated ICs. Due to the specificity of a 3D object (versus a 2D one), the study focus on dedicated test chips and close-to-commercial devices of the current generation. Note that in contrast to many thermal studies, we are not investigating the hot spot (heat source) itself, but its impact on the temperature distribution and on the performance of components located further away.

In order to provide an accurate description of this problem, the thermal characteristics of the materials involved need first to be determined. At the submicron scale, numerous issues arise such as thermal properties characterization or thin film effects (interfacial resistance). This task, and those specificities intrinsically related to the microelectronic domain, will be also addressed in this work.

This report is made of four chapters and a conclusion section. Chapters 2-4 are the original contributions involving both entangled experimental and numerical tasks, while the first chapter provides an overview of key elements required for the understanding of the document. The contents of the chapters are detailed below.

In the first chapter, a state of the art of the influence of temperature on ICs is established in order to provide an overview of the specific issues in microelectronics. After having detailed the specificities of the recent imaging technologies, the thermal impact on various phenomenon such as electromigration, thermomechanical stress or dark current variation are presented. Hence, the performance of the chip, whether in terms of reliability or quality, is significantly impacted by the temperature. In the case of 3D HB imagers, this is all the more true for the optical performance of the pixel array.

Before investigating the thermal behavior of a 3D object, materials need first to be characterized. This work is described in the second chapter. Various dielectric thin films involving oxides, nitrides, and low-k compounds are evaluated. These materials and samples are chosen because they are the main components of the structure of an electronic chip for both the Front-End-Of-Line (FEOL) and the Back-End-Of-Line (BEOL). In order to characterize the thermal properties of our materials, two different electrothermal methods are implemented: Scanning Thermal Microscopy (SThM) and the 3ω method. SThM is a contact probe technique that allows to obtain a thermal signal at sub-micrometric scale. It allows to measure thermal variables/parameters such as temperatures, thermal conductivities or phase transition temperature for example. In SThM, the interpretation of the experimental data remains challenging. In order to allow quantitative data analysis, the heat transfer mechanisms between the probe and the sample are modelled by means of FE method involving heuristic parameters determined on physical basis. SThM measurements are performed with two types of probes: the palladium nano-probe and the Wollaston micro-probe. Concerning the 3ω method, it is a four-probe electrothermal method designed to measure the thermal conductivity of bulk materials

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and thin films. 3ω devices are patterned by a photolithography process in clean room on top of the samples and heated with an alternating current. The effective thermal conductivity of the sample is deduced from the temperature rise of the wire. All the dielectric materials are investigated with these two techniques. The pros and cons of each method will be compared and discussed.

Chapter 3 aims to develop and validate a relevant approach of numerical modelling by FE for the prediction of the thermal behavior of 3D HB chips. A specific test chip used for the investigation of thermal issues, called M3EM, is detailed. The M3EM chip has been co-developed by ST Microelectronics and CEA LETI in order to quantify the efficiency of the HB fabrication process in terms of heat management. Embedded heaters and sensors (copper serpentines) located in the BEOL generate heat by Joule effect across the stack in order to represent the power generation of the functional blocks (i.e. power supply, memory signal treatment …) in real chips. In order to apply the FE method to the M3EM chip, a numerical method involving homogenization and a multiscale approach is proposed to overcome the issue raised by the large aspect ratios inherent to microelectronics. This procedure is validated by comparing calculations and experimental measurements performed with SThM, resistive thermometry and infrared microscopy on the M3EM test chip. The advantages and drawbacks of each method are described.

In chapter 4, the focus is on the thermal behavior of the 3D HB imager technology. To do so, methods and approaches, validated in the previous chapter, are applied on two different electronic chips. The first one, called FLAMINGO, is an analog test chip with an inactive pixel matrix and embedded electrothermal test structures. This chip was designed to validate the whole process and assembly flow in terms of mechanical reliability. The second chip, called 93D, is a demonstrator with an active pixel matrix. Both chips were therefore designed for different objectives and, thus, have different added value in the frame of this work. In a first step, the FEOL and BEOL structures of these two chips are detailed. In a second step, the FLAMINGO chip is used to study the thermal behavior of the pixel. SThM measurements are implemented to validate the numerical analysis at the pixel array level. In a third step, the optical performances with regard to the temperature field are evaluated thanks to the 93D demonstrator by means of PTAT sensors and pixel dark current performance. This allows experimental quantification of self-heating phenomena in true devices in terms of optical performances for different use cases, both in the static and dynamic regimes.

Finally, the main conclusions of this work are summarized in the last section. Some observations useful for the next generation of devices and the future method development are highlighted.

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Chapter 1. 3D Hybrid Bonding imagers: context and challenges

This chapter aims to provide the main ideas regarding 3D Hybrid Bonding (HB) imagers (IMG) and the thermal challenges related to this new technology. It therefore provides key ingredients for the following of the manuscript, however it does not address in depth all aspects, which can be found elsewhere with an improved level of detail (references are given). More precisely, here the technology is first detailed from a functional and manufacturing point of view. The 3D integration, the hybrid bonding and the pinned photodiode principle are explained in short. In a second step, an inventory of some key thermal constraints induced by the new technology is drawn, involving in particular thermomechanical stress, dark current generation and electromigration. Finally, different numerical and experimental methods for the characterization of heating and its impact on devices are briefly presented. Among all the methods available in the literature, some will be retained for use in this PhD work and applied in the following chapters.

I. 3D hybrid bonding technologies

In this section, the 3D HB IMG technology is detailed in three parts. First, a general description of the integrated circuit technology is provided. Then, the principle of 3D integration and the hybrid bonding technology are explained. Finally, the imaging technology architecture, embedded in the 3D stack, is detailed.

I.1. Integrated circuits

Here, some very fundamentals about integrated circuits (IC) structure are recalled. Considering only the chip, an IC can be divided in two parts: the Front-End-Of-Line (FEOL) and the Back-End-Of-Line (BEOL).

I.1.A. General trends in microelectronics

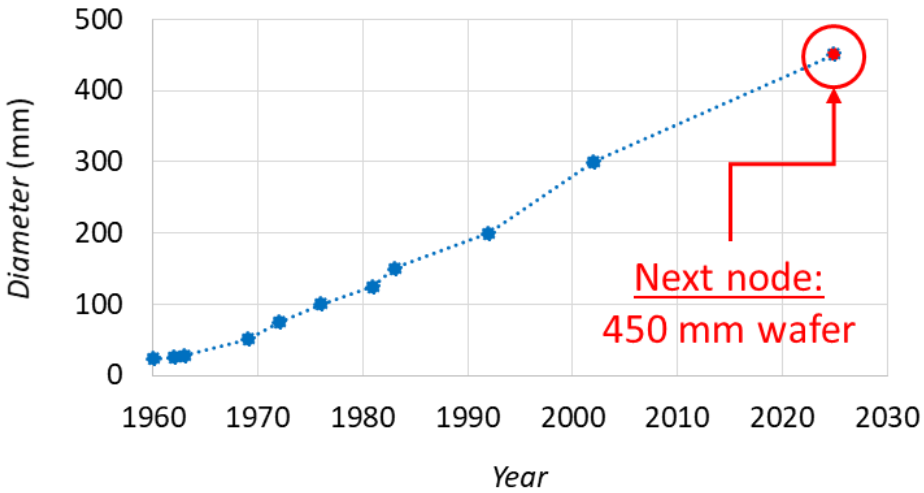

Figure 1.1: Wafer diameter increase during the last decades [7].

In electronics, the substrate (called also “wafer”) [1] is a thin slice of semiconductor, e.g. silicon, germanium or gallium arsenide, depending on the technology. The bulk silicon wafer is the oldest technology but remains a staple of the microelectronic industry: it is used in many microelectronic

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technologies. Its thickness is typically about 0.7 mm. Si wafers are usually made of single-crystal silicon fabricated with the Czochralski process [2]. During the last few years, the development of microelectronics has seen the emergence of a new type of wafer: the Silicon-On-Insulator (SOI) substrate [3]. The SOI technology refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrate. This allows among other advantages to reduce parasitic capacitance in transistors and therefore increase electrical performance [4]. The choice of the insulator depends on the application. In the majority of cases, sapphire and silicon dioxide are used for high-performance radio frequency (RF) and microelectronics devices, respectively [5]. More generally speaking, the constant evolution of the Metal-Oxide-Semiconductor (MOS) technology has been driven during the last four decades by Moore and More than Moore's law which assess that the density of components roughly double every two years [6]. In addition to improving substrate technologies, the microelectronic industry has continually sought to increase the diameter of wafers, which allows them to consistently reduce the manufacturing cost per transistor. A schematic of the wafer size increases in the last decades is shown in Figure 1.1 [7].

I.1.B. Front-End-Of-Line

In this section, the principle of the Front-End-Of-Line (FEOL) is explained at both MOS Field-Effect Transistor (FET) and die levels.

I.1.B.a. MOSFET principle

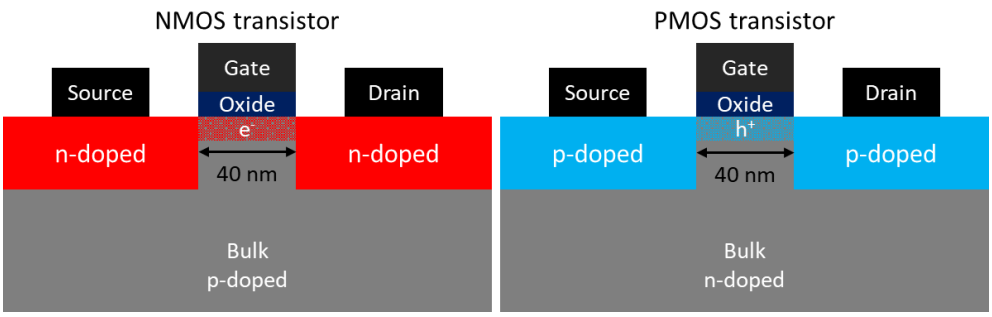

Figure 1.2: Schematic of the PMOS and NMOS of the CMOS40 technology.

The Front-End-Of-Line (FEOL) is the first portion of IC fabrication where the individual transistors are patterned in the semiconductor. The technologies used in this thesis are based on MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor). The MOSFET technology is used in both digital logic and analog circuits such as microcontrollers, memory and CMOS sensors for example [8]. The principle of the MOSFET is detailed in Figure 1.2. The electrical current flowing from the source to the drain is controlled electrically by the voltage applied on the gate. In the case of the n-doped CMOS transistor (NMOS), powering the gate generates an electron channel in the substrate. Conversely, without powering the gate, the transistor is like an open circuit. In the case of the PMOS transistor, the principle is the same with a channel of holes. Note that a technology name (i.e. CMOS40 in this thesis) refers to the gate length in nanometers.

I.1.B.b. FEOL processing

FEOL processing refers to the formation of the transistors directly in the silicon substrate. The FEOL surface engineering consists in different consecutive steps:

(i) growing the gate dielectric (usually silicon dioxide) with dry oxidation. The dry oxidation is usually used to form thin oxides in a device structure because of its good Si-SiO_2 interface characteristics [9];

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(ii) patterning the sources and drain regions with the photolithography process. This procedure combines several steps in sequence: cleaning, preparation, photoresist application, exposure and developing, etching and photoresist removal [10];

(iii) ionic implantation [11] and diffusion [12] of the dopants to obtain the desired electrical field in the MOSFET channel.

Considering that the length of the gate is directly related to the transistor density in the substrate, manufacturing techniques have been constantly improved to reduce the dimension of the gate. Lithography has been one of the key drivers for the semiconductor industry. Roughly half of the density improvements have been derived from improvement in lithography [13]. Indeed, the minimum feature size (critical dimension) CD is equal to:

$$CD = \frac{k_1}{n}\frac{\lambda}{NA}, \tag{1.1}$$

where λ is the wavelength of light used, NA (~ 1) is the numerical aperture of the lens, n is the index of refraction and k_1 (~ 0.4) is a coefficient that encapsulates process-related factors. Modern processes use UV light ($\lambda = 193$ nm from an Argon-Fluoride laser), which makes it possible to pattern details of the order of 80 nm [14, 15]. To get down to 50 nm, the last lens and silicon are immersed in ultra-pure water. Water having a refractive index equal to 1.44, the wavelength of the light that propagates there is divided by all, which improves the resolution by 30 to 40%. The next generation of lithography will use extreme ultraviolet (EUV), at around 13 nm leading ideally to critical dimensions of the order of a few nanometers. However, the limit of lithography seems to be reached because the use of X-rays is not possible due to physical constraints [16]. Nowadays, the latest technologies released in the market are below 22 nm (Intel, TSMC…).

I.1.C. Back-End-Of-Line

The Back-End-Of-Line (BEOL) is the second level of an ICs fabrication where the transistors are interconnected together via metal wires on several levels. A schematic of the BEOL is detailed in Figure 1.3. The BEOL structure includes:

(i) tungsten contacts (on transistor source, drain and gate). Tungsten is chosen because it is less sensitive to electromigration. This is in particular very important for the finest lines where the current density can be as high as 10^6 A.cm^{-2} [17, 18];

(ii) insulating layers (dielectrics). These layers need low-k dielectric constant in order to avoid parasitic RC coupling between the metal layers [19, 20];

(iii) barriers (silicon nitride, silicon carbo-nitride…) which avoid the diffusion of the copper atoms of the metallic levels in the layers of oxide [21];

(iv) metal levels and vias. In the case of recent technologies, copper is used for the metal levels of the BEOL due to its low electrical resistivity [22];

(v) a capping layer made of silicon nitride preventing contamination and humidity to enter into the BEOL [23];

(vi) bonding sites for chip-to-package connections (wire bonding, bumps…) with aluminum contacts [24].

In BEOL part of fabrication stage contacts (pads), interconnect wires, vias and dielectric structures are formed (see Figure 1.3). For modern IC process, up to 10 metal layers can be stacked in the BEOL.

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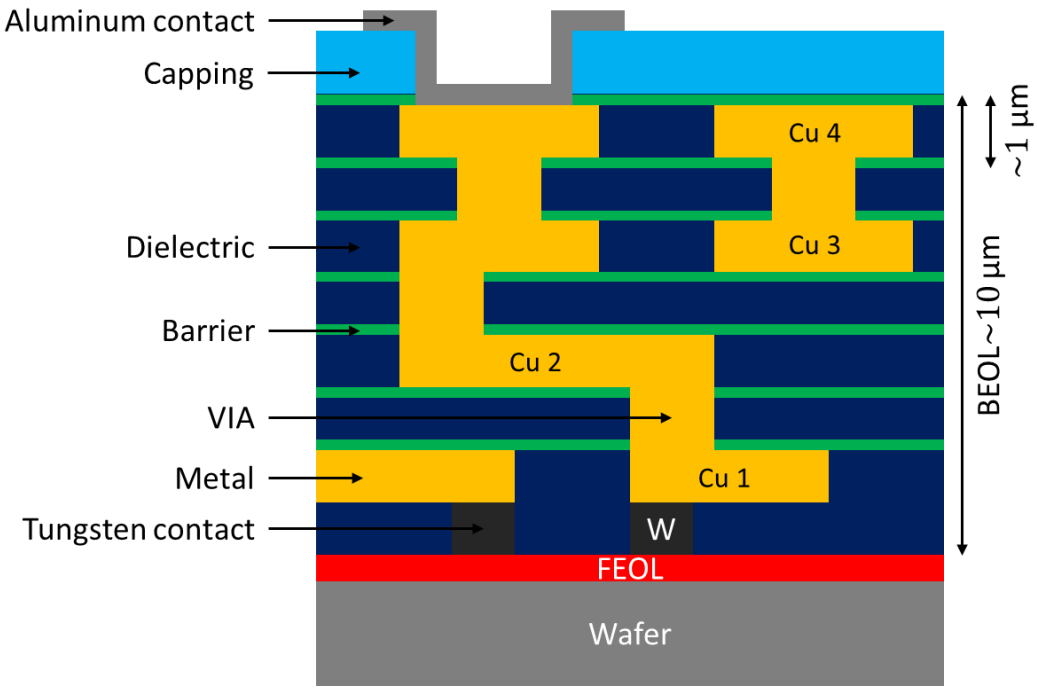

Figure 1.3: Cross section schematic of the BEOL structure (not to scale).

I.2. 3D integration for ICs

In this section, the 3D Hybrid Bonding technology is detailed. First, the principle of 3D integration is explained. Then, two different 3D integration technologies are detailed: Through Silicon Via (TSV) and Hybrid Bonding (HB).

I.2.A. 3D integration principle

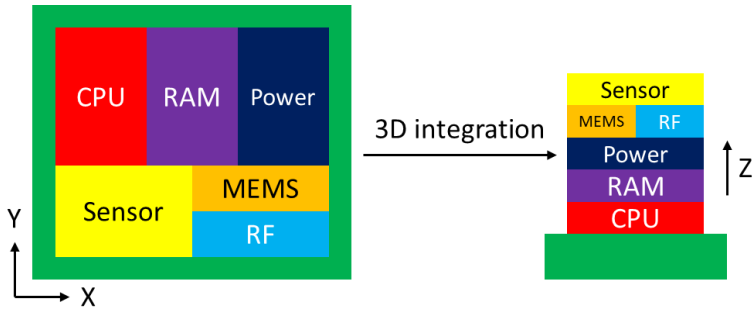

Figure 1.4: 3D stacking principle for heterogeneous integration.

Technological limitations induced by transistors size reduction having been reached, the development of 3D integration has therefore emerged. The principle of 3D integration is explained in Figure 1.4. Different functional devices (sensor, MEMS, power management, memory…) are stacked together in the vertical direction. 3D integration is also called “heterogeneous integration” [25, 26].

3D integration is particularly interesting for imaging applications. Indeed, in the conventional approach, the logic elements are located at the periphery of the pixel matrix (2D floorplan). Large die size, poor time constant and similar technology for both imager and digital components are the main drawbacks of such integration. All these limitations are resolved by means of the 3D integration: digital blocks are located below the pixel matrix, the signal treatment is improved and advanced digital technology can be used.

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I.2.B. 3D integration technologies

The two most common technologies for 3D integration are presented here: the Through Silicon Via (TSV) and the Hybrid Bonding (HB) technologies. The advantages and drawbacks of these two technologies are compared.

I.2.B.a. Through Silicon Via

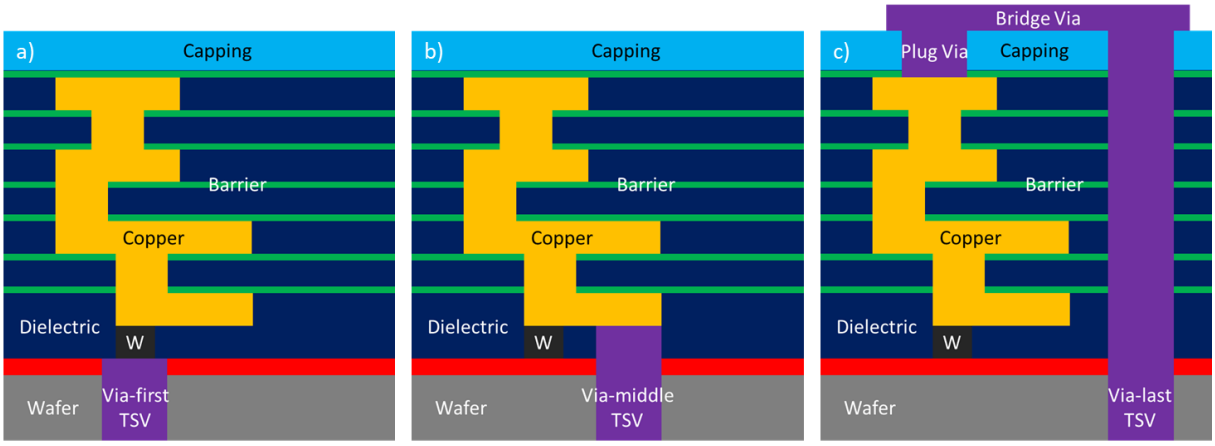

Figure 1.5: Schematic of TSV structure with a) via-first, b) via-middle and c) via-last.

A Through Silicon Via (TSV) is a vertical electrical connection that crosses completely a silicon die [27]. A schematic of TSV structures is shown in Figure 1.5. TSVs have some advantages for the semiconductor industry dealing with 3D integration: power, area and time are better compared with conventional interconnects such as wire bonding, ball bonding… [28]. Such integration uses similar process steps to the BEOL stack. Three different types of TSVs exist:

(i) via-first TSVs fabricated before FEOL manufacturing;

(ii) via-middle TSVs fabricated between FEOL and BEOL manufacturing;

(iii) via-last TSVs fabricated after BEOL manufacturing.

I.2.B.b. Hybrid Bonding

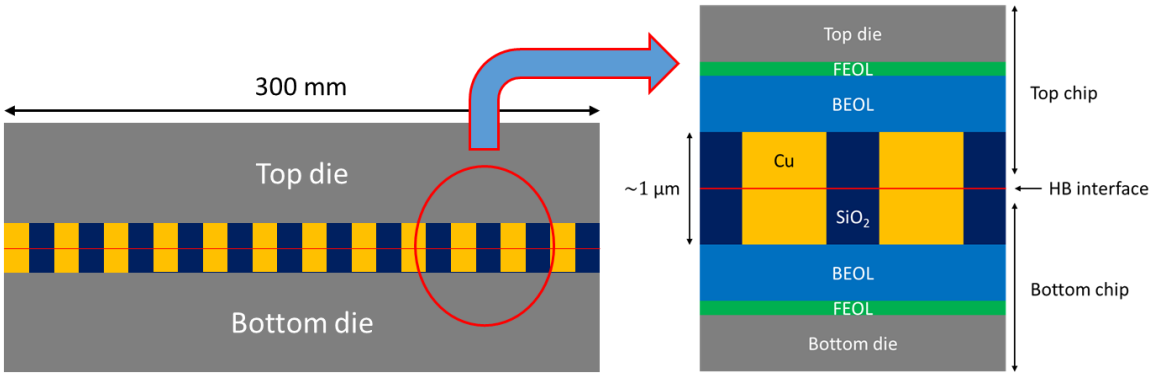

Figure 1.6: Cross section schematic of the 3D Hybrid Bonding integration.

In the context of heterogeneous integration, another technology has become unavoidable in recent years: Hybrid Bonding (HB) [29]. The principle of HB is detailed in Figure 1.6. It is a permanent bond performed at the wafer scale that combines a dielectric bond with embedded metal to form interconnections. It has become known in the industry as Direct Bond Interconnect (DBI). HB can offer

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high via density, good alignment and high bonding strength with stress-free hermetic-sealed bonding structure [30]. In addition, various low-temperature HB techniques allow saving thermal budget as much as possible [31]. Contrary to TSV integration, this one requires the development of new steps in the process flow as shown in Figure 1.7. Further details and challenges related to this specific process can be found in [32] for example.

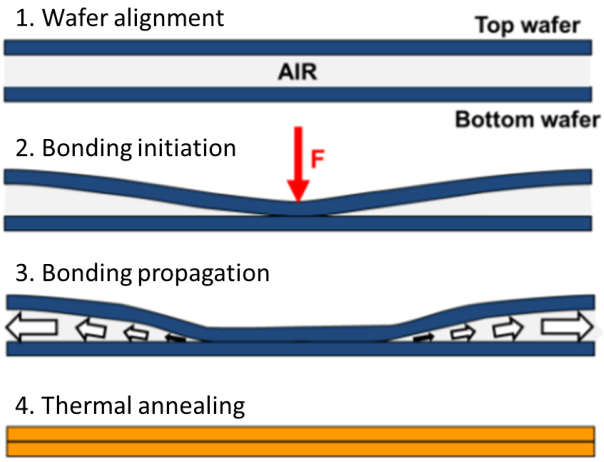

Figure 1.7: Schematic of the Hybrid Bonding process flow [32].

I.2.B.c. Comparison between TSV and HB

Some advantages and drawbacks of the TSV and HB technologies are summarized in Table 1.1. Hybrid bonding giving many advantages [33-37], this technology has quickly expanded.

	TSV	HB
Advantages	Process reliability Cost fabrication	Low thermal budget High bonding energies Wafer/die-wafer bonding Thin pitch (< 15 µm) Low RC delay
Drawbacks	Electromigration Thermomechanical stress High thermal budget	Surface preparation Thermomechanical stress

Table 1.1: Advantages and drawbacks of the TSV and HB technologies [33-37].

I.3. Imaging technology

The current PhD thesis is especially concerned with devices for imaging. The two most common technologies for imaging are presented below: the Complementary Metal Oxide Semiconductor (CMOS) and the Charge Coupled Device (CCD) technologies. The advantages and drawbacks of these two technologies are compared.

I.3.A. CMOS image sensor

The principle of the photodiode, which is the fundamental brick of CMOS image sensors, is described first. Then, the architecture of the CMOS image sensor technology is detailed.

I.3.A.a. Pinned photodiode

A pinned photodiode (PPD) is a PN junction or PIN structure. When a photon of sufficient energy hits the diode, an electron-hole pair is created. This mechanism is also called photoelectric effect (see simplified schematic in Figure 1.8).

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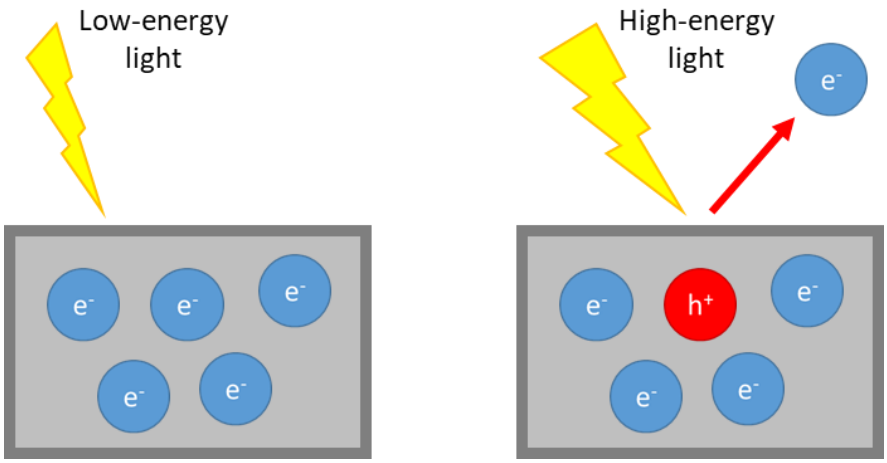

Figure 1.8: Principle of the photoelectric effect [38].

If the photon is absorbed in the junction's depletion region, or up to one diffusion length away from it, the electron-hole pair is separated by the electric field of the depletion region. The hole moves toward the anode and the electron moves toward the cathode. A photocurrent is produced. The principle of the PN junction of the photodiode is explained in Figure 1.9. To first order, for a given spectral distribution, the photocurrent is proportional to the irradiance [39]. The photodiode can be used in two different modes:

(i) the photovoltaic mode is defined under zero bias. The photocurrent flows out of the anode through a short circuit to the cathode. This mode exploits the photovoltaic effect, which is the basis for solar cells;

(ii) the photoconductive mode when used in reversed bias. The response time is reduced because the additional reverse bias increases the width of the depletion layer, which increases the region with an electric field that will collect electrons quickly.

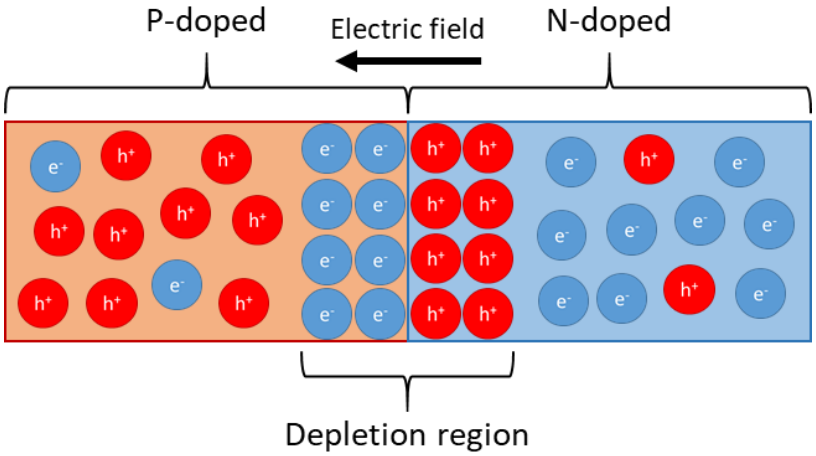

Figure 1.9: Depletion region at the PN junction of the photodiode following [40].

I.3.A.b. Pinned photodiode embedded in CMOS image sensor

A schematic of the PPD pixel is shown in Figure 1.10. The PPD is associated with a Transfer Gate (TG), which isolates the PPD from the Floating Diffusion (FD) during light integration (V_{TG} off) and enables electron transfer from the PPD to the FD for the readout of the output charge (V_{TG} on). The Shallow Trenches for Isolation (STIs) are used to isolate the CMOS transistors from each other.

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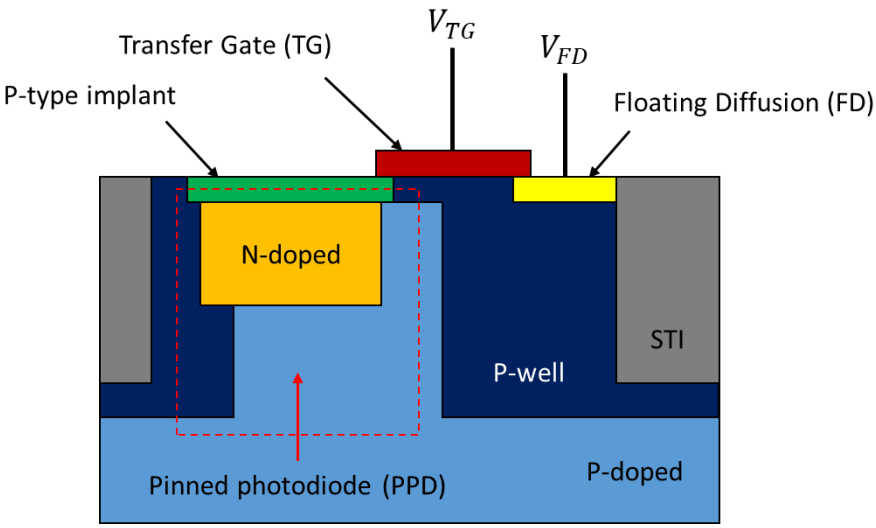

Figure 1.10: Structure of a PPD CMOS pixel for p-doped silicon [41].

I.3.B. CCD image sensor

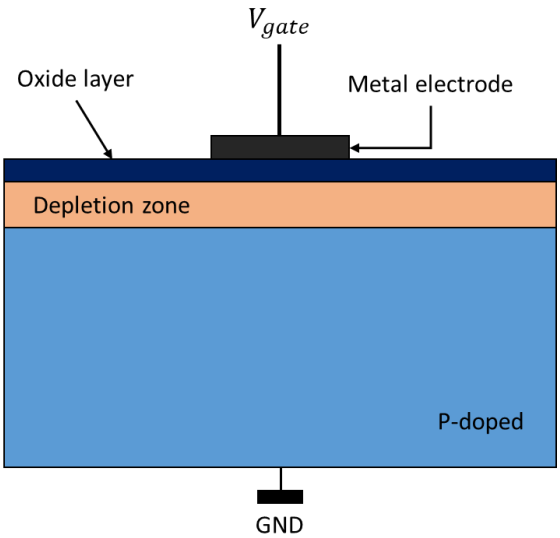

Figure 1.11: Structure of a CCD pixel for p-doped silicon [42].

The CCD image sensor technology is based on the Metal Oxide Semiconductor (MOS) capacitor as shown in Figure 1.11. If a photon, with a sufficient energy, is absorbed in the depletion zone, an electron-hole pair is created. The electron remains in the depletion zone while the hole moves toward the substrate. The amount of negative charge (electrons) that can be collected is proportional to the applied voltage, the oxide thickness and the surface area of the gate. The total number of electrons that can be stored is called “well capacity”. When the wavelength increases, photons are absorbed at increasing depths. This notably limits the response to high wavelengths. Currently, available sensors can function from far infrared to X-rays.

I.3.C. Comparison between CCD and CMOS imagers

Key advantages and drawbacks of the CCD and CMOS image sensors are summarized in Table 1.2. Another design has been developed: the hybrid CCD/CMOS architecture consisting of CMOS readout integrated circuits that are bump bonded to a CCD imaging substrate has emerged. This technology has been adapted to silicon-based detector technology to mix the benefits of both CCD and CMOS imagers [44].

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	CCD	CMOS
Advantages	Low-noise images	Low power consumption Cost fabrication Fast readout
Drawbacks	High power consumption Cost fabrication Electrostatic discharge vulnerable	Light sensitivity

Table 1.2: Advantages and drawbacks of the CCD and CMOS technologies [43].

I.4. Conclusions on 3D HB imager technology

This brief analysis of the architectures used for imagers shows us that the 3D hybrid bonding integration will allow a high increase in integration density in next-generation ICs. A schematic of the global 3D Hybrid Bonding imager architecture is shown in Figure 1.12. This is especially due to the very low pitch (< 15 µm) of interconnections that can be reach with the DBI. However, for imager applications, the logic is located just below the matrix pixel. The power dissipated by the digital components and the volume reduction raise many challenges regarding thermal dissipation. An analysis is made in the next section.

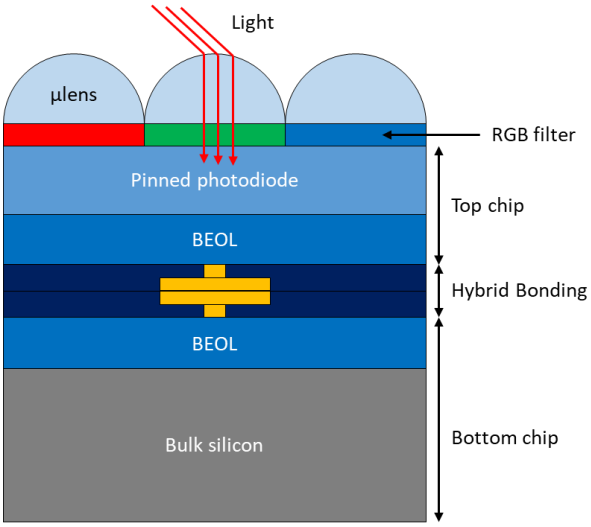

Figure 1.12: Structure of the 3D Back-Side-Illumination Hybrid Bonding imager.

II. Thermal issues in ICs related to 3D hybrid bonding imagers

Miniaturization in the field of electronics packaging, coupled with faster circuits dissipating higher power, have increased the heat fluxes in microelectronic devices. One of the key problems is to dissipate the heat generated by the device to meet the thermal requirements for an optimal performance and reliability. Thus, power to be dissipated ranges from 5W to 300W for mobile or desktop processors, respectively [45, 46]. This section aims to present various impacts related to the effect of temperature in the 3D Hybrid Bonding imagers. Many detrimental phenomena related to thermal parameters are possible, but the focus is here on three temperature-related issues: thermomechanical stress, electromigration and optical noise.

II.1. Thermomechanical stress

At the BEOL level, the stress is detrimental, acting on yield loss, mostly during manufacturing but also during operation. In this section, the cause of thermomechanical stress is explained and different stress failure mechanisms are reviewed.

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II.1.A. Principle of thermomechanical stress

Mechanical stress can be driven by a wide range of distinct causes like temperature gradients for example. In thermomechanics, the deformation of the material is calculated as follows:

$$\varepsilon_{th} = \alpha_{th}\Delta T, \tag{1.2}$$

where ε_{th} is the thermal strain, α_{th} is the Thermal Expansion Coefficient (TEC) and ΔT is the temperature rise. ε_{th} and α_{th} are tensors but can be considered as scalars for isotropic media. As an example, the TEC of bulk silicon is equal to 2.56 μK^{-1} [47]. This effect is even more important in microelectronics since, as depicted previously, numerous materials with their own TEC are used, which can lead to different expansions in materials in contact. Thus, a thermal hot spot, thermal gradient or even high temperature may induce additional thermo-mechanical stress within the die and increase the risk of failure.

II.1.B. Failure mechanisms

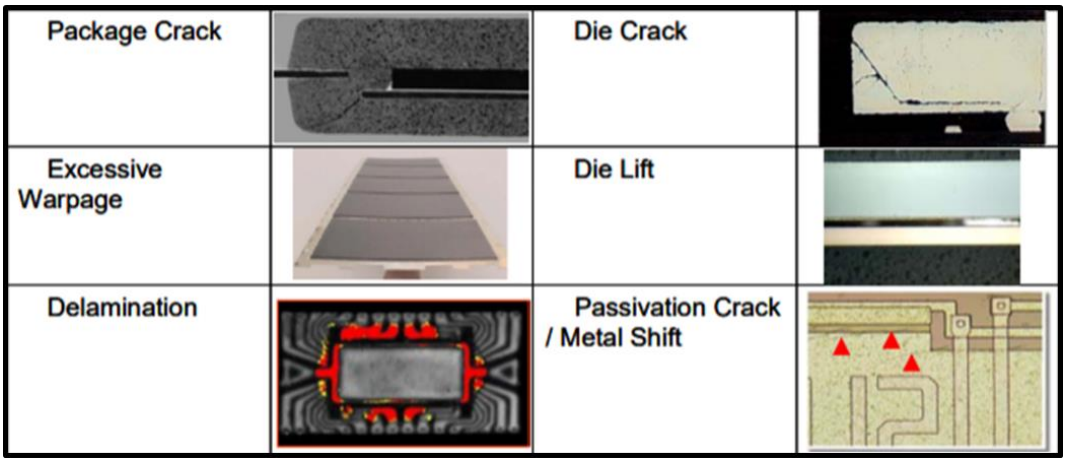

Figure 1.13: Examples of thermomechanical failure in ICs [48].

In microelectronics, many kinds of thermomechanical failure can appear. Figure 1.13 shows pictures and examples of typical ones at several locations inside the chip [48]. Stress-related failures, particularly delamination and cracking in dielectrics, are nowadays determined as one of the key limitation for integration. Such failures are liable to occur at several process steps and in distinct chip regions.

II.2. Optical constraints in imagers

In this section, two optical constraints in imagers are underlined: dark current generation and the reset noise. They participate in the reduction of the signal-to-noise ratio (SNR) and must be decreased as much as possible.

II.2.A. Dark current offset in pinned photodiode

Dark current is the electric current that flows through photosensitive devices such as photodiodes in absence of illumination. It consists of the charges generated in the detector when no external radiation is entering the detector [49]. The dark current generates an offset of the PPD output which reduces the pixel SNR. It is referred to as reverse bias leakage current in non-optical devices and is present in all diodes. Physically, the dark current is due to the random generation of electron-hole pairs in the depletion region of the PPD. The charge generation rate is related to the specific properties and

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temperature of the depletion region. Indeed, the higher the thermal energy of the medium, the more likely the photoelectric phenomenon is. The thermal energy in the medium is

$$E = k_b T, \tag{1.3}$$

where k_b is the Boltzmann constant and T the temperature of the depletion region. Dark current is one of the main sources for noise in image sensors such as CCD or CMOS. An example of the temperature influence on the dark current intensity is shown in Figure 1.14 [50]. The dark current must be accounted for by calibration if a photodiode is expected to provide an accurate optical power measurement. In particular, if temperature gradients are present, knowing the dark current value at any point of the pixel matrix is not always an easy task.

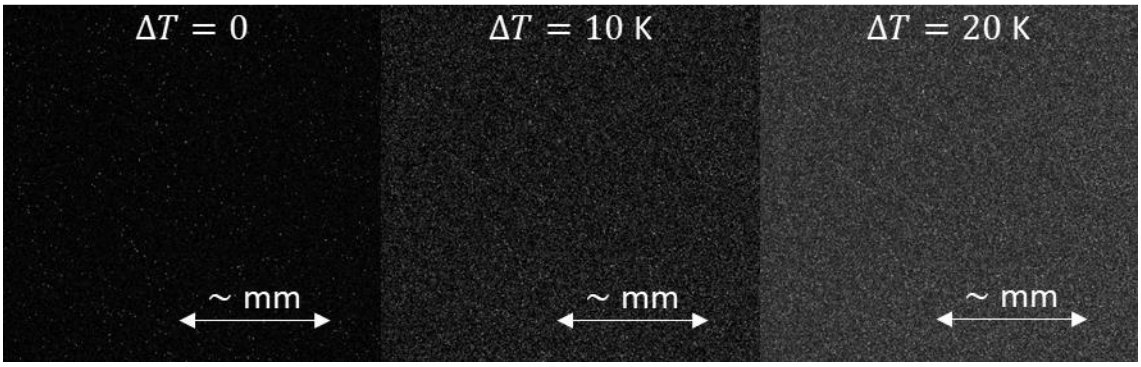

Figure 1.14: Dark current intensity (arbitrary unit) as a function of the temperature rise in an IC [50].

II.2.B. Reset thermal noise

Another type of thermal noise, called the reset noise, has become a limiting factor in pixel performance [51, 52]. It is even more important as the CMOS image sensor size decreases. The reset operation aims to provide a reference to compare to the number of electron-hole pairs generated by the photoelectric effect. The reset noise is generated by the thermal noise that causes voltage variations in the reset level of the pixel. The reset noise affects the pixel SNR especially in low-illumination conditions. The thermal reset noise is

$$\bar{V} = \frac{k_b T}{2C}, \tag{1.4}$$

where $\bar{V}$ is the mean value of the output noise voltage and C is the junction capacity of the PPD. Other thermal noises such as readout noise, integration noise and shot noise are present in CCD and CMOS imagers. These thermal noises are detailed for instance by Tian and Boukhayma [53, 54]. It is all the more important as the temperature of the photodiode is large.

II.3. Electromigration

In this section, the principle of the electromigration is explained. Then, the induced failures generated in ICs are detailed and illustrated.

II.3.A. Principle of electromigration

Electromigration is the transport of material caused by the gradual movement of the ions in a conductor due to the collisions between conducting electrons and metal ions. The principle of electromigration is explained in Figure 1.15. In an ideal conductor, the electrons moving through it would not collide ions and electromigration would not occur. In a real conductors, electromigration occurs due to the interactions between the electrons and the lattice structure.

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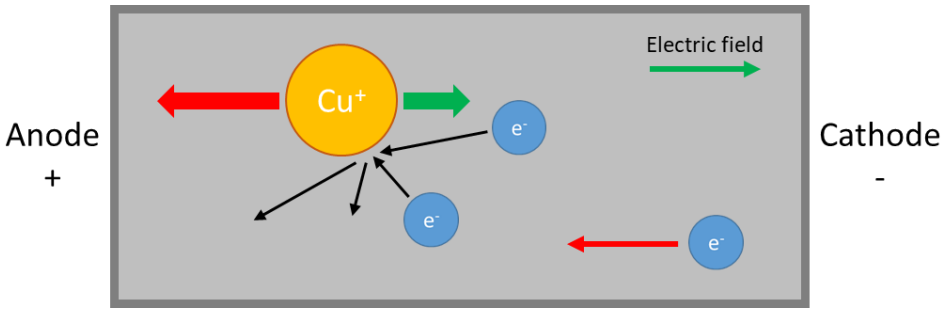

Figure 1.15: Electromigration due to momentum transfer from the electrons to the atoms.

II.3.B. Electromigration failure mechanisms

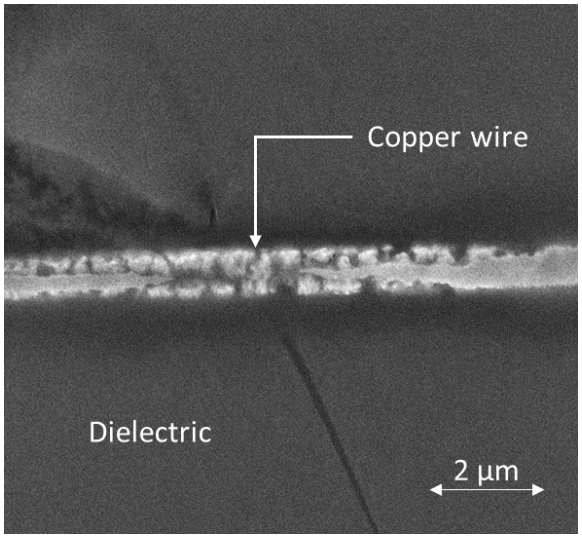

Figure 1.16: SEM image of a failure caused by electromigration.

Usually, the amount of momentum imparted by the conducting electrons (low mass) is not enough to displace the ions. However, in high-power situations, many electrons hit the ions with a force that becomes significant. This accelerates the process of electromigration by moving the ions far from their initial lattice position. High current density increases the number of electron-ion collisions and hence the electromigration phenomenon. At the end of the 1960s, J.R. Black developed an empirical model to estimate the Mean Time To Failure (MTTF) of a wire, taking electromigration into consideration [55, 56]. The empirical formula of MTTF is

$$MTTF = \frac{A}{J_n} \exp\left(\frac{E_a}{k_b T}\right), \tag{1.5}$$

where A is a constant based on the cross-sectional area of the interconnect, J is the current density normal to the electron flux direction, E_a is the activation energy and n is a scaling factor (usually set to 2 according to Black). The temperature of the conductor affects strongly the MTTF of the interconnections. The Black model has become very popular in the industry of microelectronics. However, as interconnect technology advances at the nanometer scale, Black's equation is no longer valid. In ICs, electromigration occurs in the metal interconnects of the BEOL level. Electromigration is enhanced by high-current densities ($J > 10^6$ A.cm^{-2}) in the interconnections, and can lead to eventual failures. As the structure size in electronics such as ICs decreases, the practical significance of this effect increases. A Scanning Electron Microscopy (SEM) image of a failure caused by electromigration in a copper interconnection is shown in Figure 1.16.

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II.4. Conclusions on thermal issues

This short review of the thermal issues in ICs and especially in 3D HB imagers has shown that temperature may has a significant impact on the quality and reliability of microelectronic devices. Optical performance and/or device integrity may be impacted by such phenomena. It is therefore important to characterize the device temperature in order to reduce the temperature-related constraints applied on it. An analysis of the way to perform such characterizations is made in the next section.

III. Thermal management for integrated circuits

In this section, different techniques used for heat dissipation in microelectronics are first detailed. Then, temperature characterization techniques in ICs, with both embedded sensors and with microscopy techniques, are addressed. Finally, a brief overview is dedicated to available numerical methods used to get access to thermal parameters that are key for heat dissipation in microelectronic devices.

III.1. Passive dissipation techniques for electronics

The need of novel heat dissipation techniques is driven by the increase of high power-generation ICs. In the next section, the traditional heatsink architecture is detailed. Then, innovation requirements for Thermal Interface Materials (TIMs) are mentioned. Finally, recent developments for thermal characterization in electronics are addressed.

III.1.A. Traditional approach: the heat sink

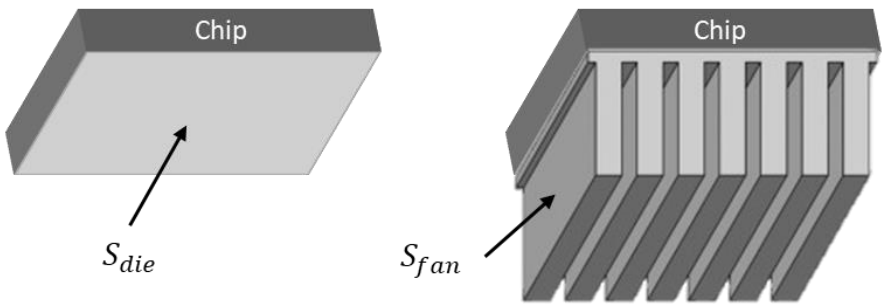

Figure 1.17: Principle of air-cooling and geometry of the fans.

A heat sink transfers thermal energy from a higher temperature device to a lower temperature fluid medium. The usual fluid medium is air. The heat sink is included in the design stage to disperse heat. It is generally acknowledged that traditional air-cooling techniques are about to reach their limits for heat dissipation of high-power applications. With standard heat sink constituted of fins (as shown in Figure 1.17) a maximum effective heat transfer coefficient of approximately 150 $W.m^{-2}.K^{-1}$ can be reached [57]. The idea is to increase the surface of exchange between the metallic fins and the fluid (S_{fan}) to dissipate more energy compared to the surface of the chip (S_{die}). Heat transfer between the fins and air takes usually place by natural convection, however fans can be used to enforce higher heat convection coefficients.

III.1.B. Thermal interface material

In all applications, thermal dissipation from the device heat sources occurs first by means of energy travelling via thermal conduction to the surfaces exposed to the cooling fluid before being evacuated. For example, as shown in Figure 1.18, heat must be conducted from the chip to the heat sink before it can be rejected to air. TIMs are used to enhance thermal conduction from the chip to the heat sink.

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TIM is the main cause of increased junction temperature in many electronics devices. A study has shown that in high-end microelectronics that uses a TIM to mount a heats ink to an electronic device, up to 60% of the total thermal resistance is due to the TIM [59]. TIMs are one of the key areas that require research and development to decrease the junction temperature [60, 61]. Figure 1.19, although a bit dated, shows the historical gap between the power dissipated by the chips and the thermal conductivity of the TIMs. The development of new, highly conductive TIM is complicated due to multiple properties required. The TIM must provide:

(i) a high thermal conductivity;

(ii) be mechanically stable in high moisture environments;

(iii) provide mechanical stress relief for inherent device to heat sink CTE differences;

(iv) provide electrical insulation of the device and the heat sink.

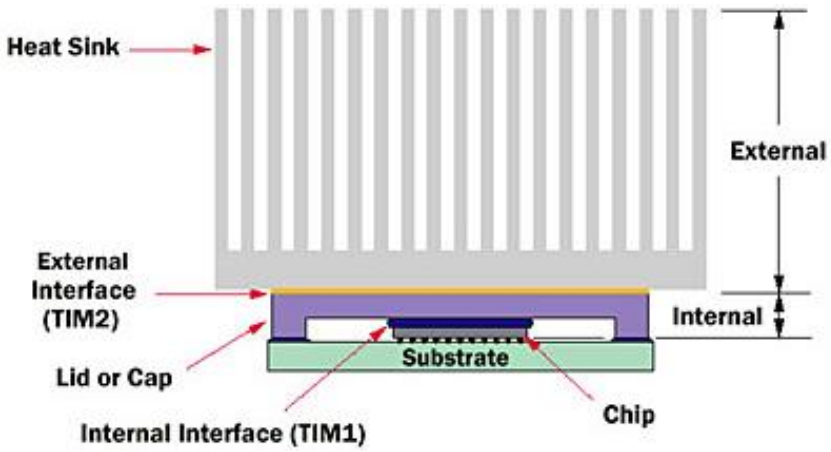

Figure 1.18: Chip/package with thermal conduction path to heat sink via TIMs [58].

A thinner TIM would reduce thermal resistance but would decrease CTE-induced stress relief as well. Metal particles would offer higher conductivity than silica particles, often used in TIMS, but would cause electrical short-circuits and failures. Because of all these material restrictions, moderate progress has been made in the past ten years to improve effective thermal conductivity of TIMs. This is one reason why electronic companies and assemblers aim at inovative materials and structures for heat sinks.

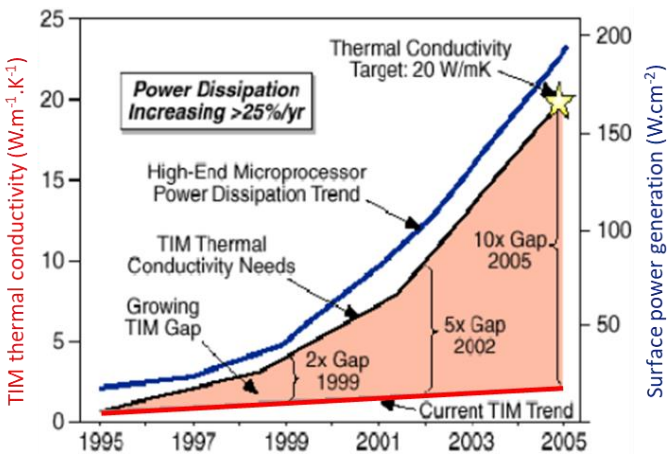

Figure 1.19: Gap between chip power generation and TIM thermal conductivity [59], from a historical perspective.

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III.1.C. Recent developments

Non-standard fans and dedicated heat sinks for CPU cooling are expected to increase the power dissipation in comparison to standard heat sinks. Some new initiatives have emerged to extend the capabilities of air-cooling, for example piezoelectric fans [62], which are actively excited in order to increase the air motion by means of forced convection, and microchannels [63-65]. Microchannels, patterned into the heat sink metal, are heat pipes that increase strongly effective conduction. However, they may require space and cannot be included in all applications. Note that all these innovative cooling techniques can only be effective if the heat transfer through the TIM is efficient, i.e. the TIM has a low thermal resistance.

III.2. Experimental thermal characterization

In order to propose thermal optimization of ICs, the temperature field of a chip is first to be measured with good accuracy. In this section, various methods for experimental characterization of temperature in ICs are briefly presented. First, embedded sensors used in test chips are detailed. Then, different microscopy techniques are mentioned.

III.2.A. Embedded sensors in ICs

In this section, embedded sensors that are typically used in microelectronic test chips and in this work are briefly described, in particular thermoresistive measurements performed with an electrical resistance. Then, the diode temperature sensor and the ring oscillator are tackled. Additional information will be given in the next chapters. Note that this list is not exhaustive and other thermal sensors could be used in appropriate situations [66].

III.2.A.a. Electrical resistance

In resistive thermometry, an electrical resistance is used to probe the temperature. The electrical resistance of the probe (often metals) varies as a function of temperature as follows:

$$R(T) = R(T_0)(1 + \alpha \Delta T), \tag{1.6}$$

where R is the electrical resistance of the metal and T is its temperature. R_0 is the electrical resistance at a temperature of reference T_0. α is the temperature coefficient of resistance (TCR) and is characteristic of each material. The value of the TCR is usually of the order of a few 10^{-3} K. In our microelectronic test samples, metal serpentines are integrated into the BEOL to allow temperature measurements at different locations of the die. The thermoresistive measurements and a test chip using copper serpentine are detailed in Chapter 3.

III.2.A.b. Diode

A diode, which is a PN junction, obeys the Shockley equation:

$$I_D = I_S \left(\exp\left(\frac{qV}{k_b T}\right) - 1 \right), \tag{1.7}$$

where V is the applied voltage, q is the electron charge, and I_S is the reverse saturation current of the diode. As the temperature T increases, the exponential factor decreases. However, an increase in T causes I_S to increase since $I_S \propto n_i^2$ where

$$n_i^2 = N_C N_V \exp\left(-\frac{E_g}{2k_b T}\right), \tag{1.8}$$

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is the intrinsic carrier concentration of the material. N_C and N_V are the densities of states for the p and n dopants [67]. The net result is that, for the same applied voltage, the diode current is higher at a higher temperature. An example of I-V curve is shown in Figure 1.20.

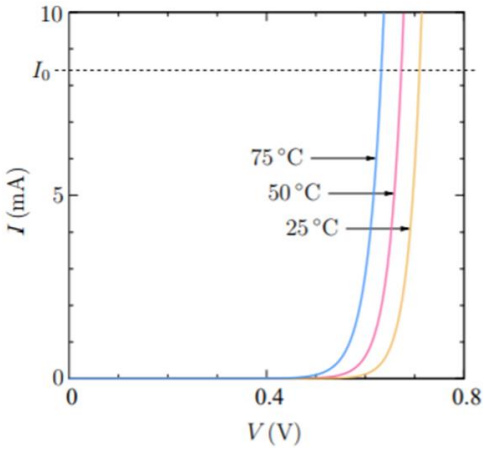

Figure 1.20: I-V curve of a silicon diode under forward bias as a function of temperature [67].

III.2.A.c. Ring-oscillator based thermal sensor

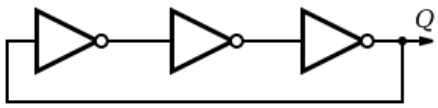

Figure 1.21: Schematic of a simple 3-inverter ring-oscillator [69].

Essentially, a thermal sensor based on ring oscillators is a closed loop with an odd number of inverters. A schematic of a simple 3-inverter ring oscillator is shown in Figure 1.21. A time base counter activates the circuit during a short period of time, capturing the oscillation frequency. Practical rings require between 5 and 25 inverters [68]. Each sensor implementation must be calibrated using a temperature-controlled furnace. The frequency of oscillation f_{ring} is calculated as follows [70]:

$$f_{ring} = \frac{1}{2n\tau_d}, \tag{1.9}$$

where n is the number of inverter and τ_d is the time delay of the inverter. The time delay τ_d is a function of the temperature and the voltage as shown in Figure 1.22. The analytical expression of the time delay τ_d is given by M.M. Mansour in [71].

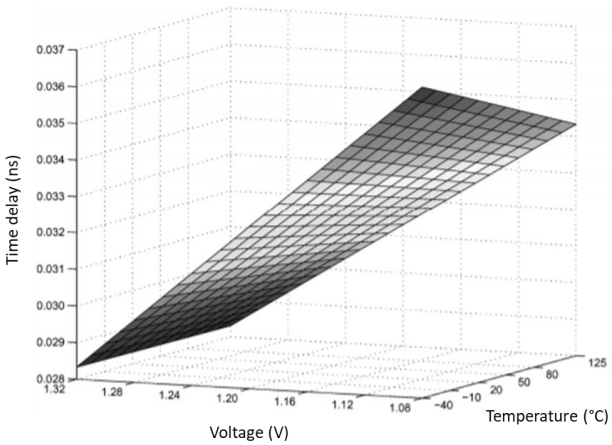

Figure 1.22: Relationship between time delay, temperature and voltage for an inverter [70].

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III.2.B. Microscopy techniques for spatial resolution

In this section, microscopy techniques that can be used for thermal characterization in microelectronics are detailed according to their spatial resolution, with first infrared (IR) thermography, which is a widespread technique (resolution of ~10 micrometers). Then, the established Thermoreflectance Thermal Imaging (TTI) technique, with a spatial resolution of the order of half a micron, is addressed. It is an example of technique where visible light is used. Other optical microscopy techniques, like Raman thermography, exist [72, 73] and are limited in the same way in spatial resolution. Addressing them in an exhaustive list is beyond the scope of the present work. Finally, Scanning Thermal Microscopy (SThM), which can reach a spatial resolution of few tens of nanometers in principle, and is not an optical technique, is introduced.

III.2.B.a. Infrared thermography

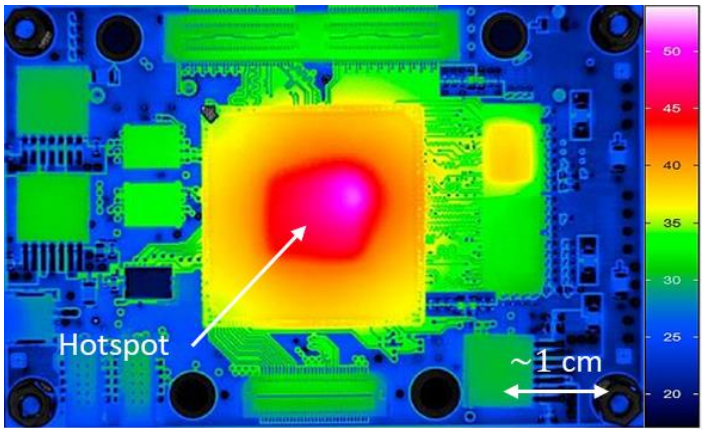

Figure 1.23: IR microscopy image of a hotspot in a SoC system [75].

Infrared (IR) thermography, also called IR microscopy, allows to measure the temperature of a medium with a spatial resolution of the order of the wavelength, i.e. down to a few microns [74]. An image realized with IR microscopy is shown in Figure 1.23 [75]. The quantity of IR photons emitted by the medium is related with its temperature. However, the emissivity of the sample has to be calibrated first as a function of temperature. With the IR microscopy, it is possible to see through a silicon wafer (silicon is transparent to IR photons) to analyze if patterns line up on the front and back sides of a wafer. It allows wafer bonds to be checked and determine if alignment has shifted during the bonding process. While silicon is transparent, oxide is more absorptive thereby appearing darker, and metal block the IR. IR microscopy has been applied to some samples in this work and is explained in more detail in Chapter 3.

III.2.B.b. Thermoreflectance thermal imaging

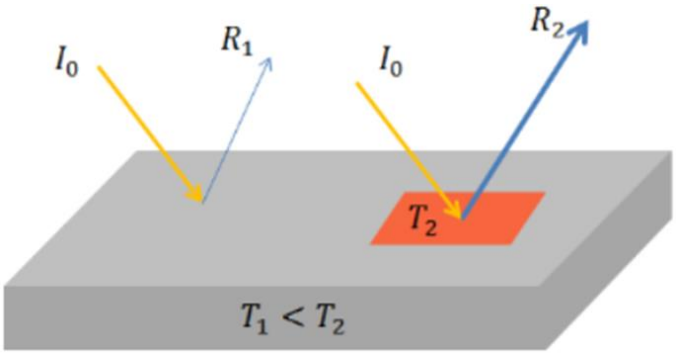

Figure 1.24: Change of the intensity (reflectivity) due to the temperature [77].

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Thermoreflectance Thermal Imaging (TTI) is another optical microscopy technique that provides temperature contrast (gradients), by analyzing the optical reflectance of the inspected surfaces. Among others TTI is employed for:

(i) non-contact 2D temperature mapping with a submicrometric spatial resolution;

(ii) failure analyses and testing of microelectronic devices;

(iii) the visualisation of high-speed thermal transients with a temporal resolution equal to 100 µs approximately;

(iv) temperature resolution under 0.1 K [76].

The principle of TTI is illustrated in Figure 1.24. When the sample is illuminated the intensity of the reflected beam depends on the local temperature of the irradiated zone [77-78]. The linear effect of temperature on the surface reflectivity of a sample is equal to [79]:

$$\frac{\Delta R}{R} = \left(\frac{1}{R}\frac{dR}{dT}\right)\Delta T = \aleph \Delta T, \tag{1.10}$$

where R is the reflectivity, ΔT is the temperature elevation and $\aleph$ is the thermoreflectance constant. Thus, hotpots, as the red square parts in Figure 1.25, increase the intensity of the reflected beam. Therefore, the accurate analysis of the reflected beam at the selected areas provides a thermal map of the device surface. The spatial resolution is related to the optical wavelength that is used and is therefore close to few hundreds of nanometers at best. A major drawback of TTI, in a similar way as other optical techniques, is related to the transparency of some materials. The examples listed previously show that TTI is a key technique for inspection in microelectronics and novel techniques will certainly have to be benchmarked against it.

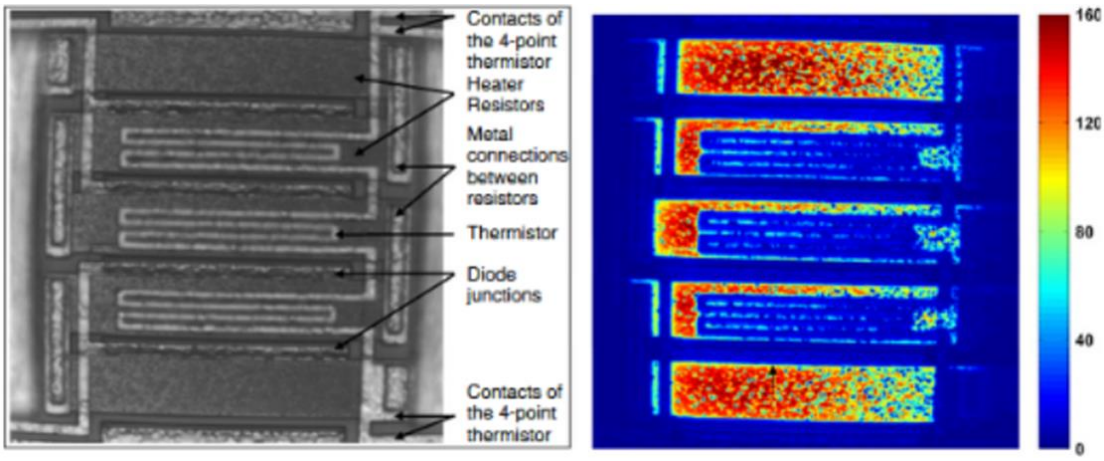

Figure 1.25: a) Optical and b) thermoreflectance image of heating resistor [77].

III.2.B.c. Scanning thermal microscopy

Scanning Thermal Microscopy (SThM) is a non-destructive contact probe technique based on Atomic Force Microscopy (AFM) that allows obtaining a thermal signal at sub-micrometric scale [80]. It allows to measure thermal variables such as temperature for example. Most of the time, the experimental data have to be interpreted by means of a numerical modelling of the thermal system, because the thermal probe do not have simple geometry which can be modeled easily (for instance analytically). The SThM setup and associated electrical circuit are used during this PhD thesis. An image acquired by SThM is shown in Figure 1 26 [81]. The probe used in SThM allows the determination of the temperature at the tip apex by measuring the probe electrical resistance. This measurement is based

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on resistive thermometry. The spatial resolution is expected to reach the sub-100 nm regime in the best conditions and the technique is possible also for transparent materials. The principle of SThM is further explained in Chapter 2.

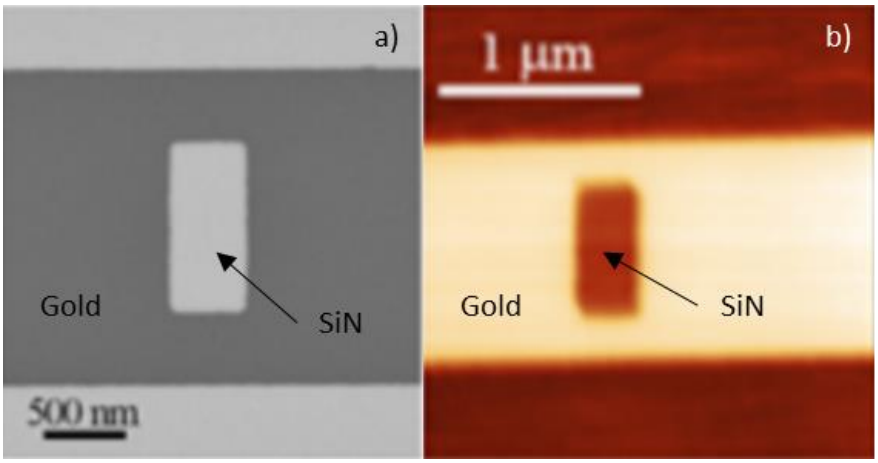

Figure 26: a) SEM image of SiN pattern. b) SThM thermal map of SiN pattern [81].

III.2.C. Summary of available techniques and selection

Various techniques can be used for thermal characterization. In this work, two functions are targeted:

(i) Simulate a dissipation source: To do so, embedded metallic serpentines are selected due to their simplicity and their ability to simulate also heat sources in the volume of the IC stack. Chapter 3 and 4 will especially deal with such dual heaters/sensors;

(ii) Thermal mapping: In order to map the temperature fields at the millimeter scale, IR microscopy will be used (see Chapter 3). However, it does not allow for surface temperature measurements when the surface is made of silicon and SThM will therefore be selected for surface temperature measurements. Comparison between the two techniques will be analyzed.

Note that similar functionalities will be used to characterize the thermal materials properties. Hence, the 3ω method, an electro-thermal method in the AC regime also based on resistive thermometry (see Section III.2.A.), and SThM will be applied in Chapter 2 for measurements of thermal conductivities and thermal boundary resistances. In addition, thermal images will be obtained both by IR thermography and SThM in Chapter 3.

The present work constitutes therefore a benchmark of SThM with respects to other more-established characterization techniques. Finally, let us note that diode characteristics depending on temperature will also be measured, when possible.

III.3. Numerical analysis of heat transfer

Developing virtual performance and reliability predictive techniques has become essential for the development of microelectronic systems. This is especially true for high-power devices. An overview of current predictive numerical methodologies is drawn. In addition, we note that it is not possible to get access experimentally to the whole temperature distribution as only temperature at surfaces or on averages over some volumes can be experimentally measured. Reconstructing the whole temperature distribution requires mixing experimental data and some numerical or analytical procedures. We first review briefly simulation techniques for heat transport at small scale.

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III.3.A. Computation of thermal conductivity

III.3.A.a. Thin films and bulk material scale

Figure 1.27.a) shows experimental data where one can observe the reduction of thermal conductivity as a function of the film thickness. The temperature dependence of thermal conductivity weakens when the film thickness is decreased, as shown in Figure 1.27.b) [82]. Analytical expressions for the computation of thermal conductivity are often considered [83], based on the dispersion curves and the knowledge of the relaxation times. In confined materials, the size-limited relaxation times can be included, allowing for the determination of size-dependent thermal conductivity. A review of such approach is explained by G. Chen in [84] or M. Massoud in his PhD thesis [85].

Often, the Boltzmann Transport Equation (BTE) for phonons is used for determining the size-dependent effective thermal conductivity. Indeed, it governs the motion of electrons and phonons at mesoscopic scale. Among others, the Monte-Carlo (MC) method can be used to solve the BTE. The main idea behind the MC method is that the results are computed based on repeated random sampling and statistical analysis. MC simulations are typically characterized by a large number of unknown parameters, many of which are difficult to obtain experimentally. MC simulation is often used to characterize the phonon transport [82], for instance in composite materials [86, 87]. However, these approaches are possible only for materials with thickness larger than 5-10 nm.

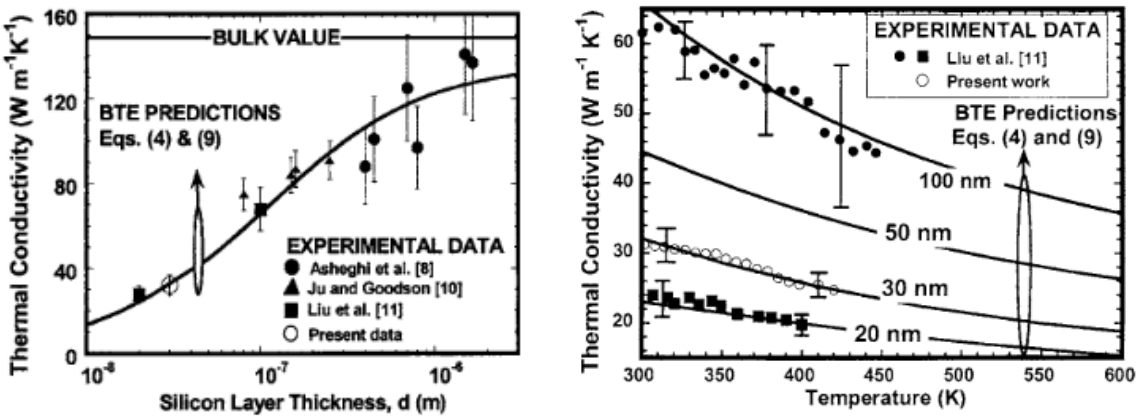

Figure 1.27: a) Effective thermal conductivity of a silicon thin film as a function of its thickness. b) Thermal conductivity of a silicon thin film as a function of temperature [85].

III.3.A.b. Atomic scale computations

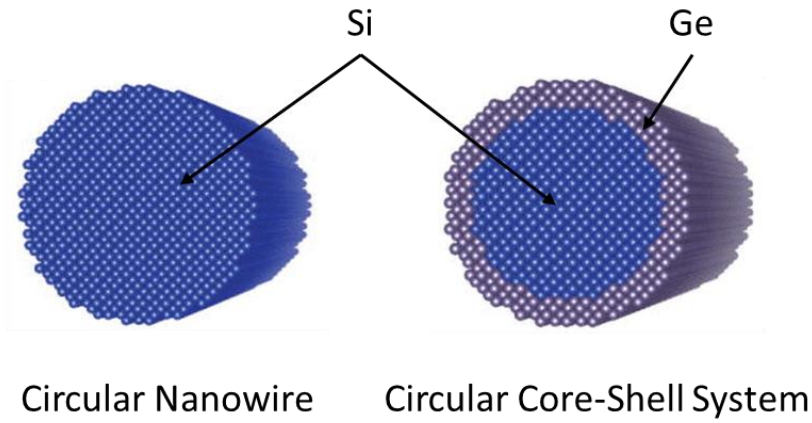

Figure 1.28: 3D MD for determination Si/Ge wire thermal conductivity [88].

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In order to determine the trends in thermal conductivity of material and/or heterogeneous structures as a function of size or temperature, Molecular Dynamics (MD) is possible for non-metallic crystals. MD is a computer simulation method for studying the physical movements of atoms and molecules, which are allowed to interact for a fixed period of time, giving a view of the dynamic evolution of the system. In the most common version, the trajectories of atoms and molecules are determined by solving Newton's equations of motion for a system of interacting particles, where forces between the particles and their potential energies are often calculated using interatomic potentials or molecular mechanics force fields. The thermal conductivity of heterogeneous structures like silicon nanowires can be calculated with MD. A MD model of a Si/Ge nanowire is shown in Figure 1.28 [88]. For example, the simulated thermal conductivities of nanowires with square cross sections are found to be about two orders of magnitude smaller than those of bulk silicon crystals in a wide range of temperatures (200–500 K) for both rigid and free boundary conditions [89]. The MD method is very time consuming and requires significant computational power. Currently the sizes that can be simulated stay small, probably at best (100 nm)^3. In addition, the coupling with electron-related phenomena is often difficult. While MD is promising, it will not be considered in the present work.

III.3.B. Thermal boundary resistance calculation

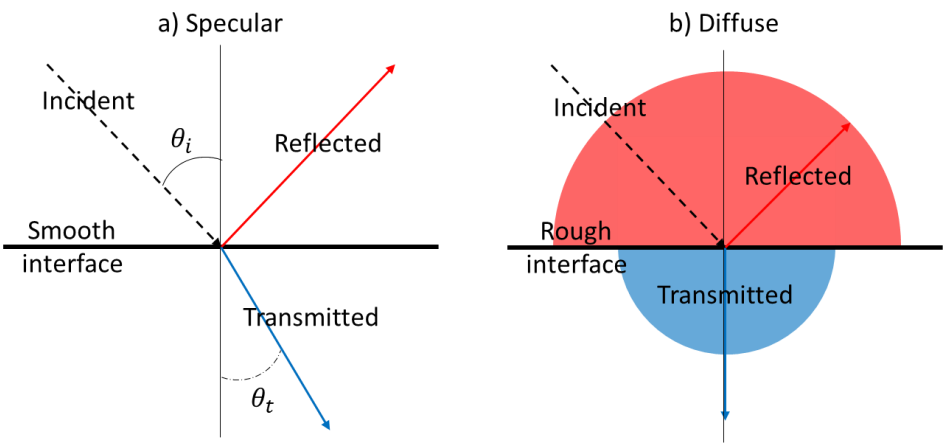

Figure 1.29: Principle of the a) Acoustic and b) Diffuse Mismatch Models.

The thermal boundary resistance (TBR) between two materials, which is the resistance associated to temperature jumps at boundaries, can be computed by Molecular Dynamics, where it is often powerful. In this PhD thesis, TBRs are calculated using the semi-analytical Acoustic Mismatch Model (AMM) and Diffuse Mismatch Model (DMM). AMM and DMM are specifically dedicated to the calculation of TBRs between two media. The principles of AMM and DMM are explained in Figure 1.29. The phonon transmission at the interface can be specular or diffuse. The transmission coefficient is given by Cheeke et al. and Swartz and Pohl in [90, 91] for AMM and DMM, respectively. Here, the dispersion relation of each material is considered, which is an improvement over the usual AMM and DMM (often used at low temperature in the past). Amorphous materials are considered in the frame of the Debye model.

III.3.C. Full temperature fields

In the context of the resolution of partial differential equations, especially in microelectronics about 3D integration technologies, the Finite Difference Model (FDM) and the Finite Element Model (FEM) are often used to solve problems of heat dissipation [92-96]. Finite Element Analysis (FEA) is one of the key tools used by engineers to solve numerically physical and mathematical problems and is chosen in this PhD thesis. As many numerical methods, it is characterized by a variational formulation (Galerkin

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methods), a discretization strategy, one or more solution algorithms and post-processing procedures. To solve the problem, the large system domain is meshed, here into smaller domains called finite elements. The FEM models are used in microelectronics to calculate heat transfer, mechanical stress and electrothermal effects in chips architectures.

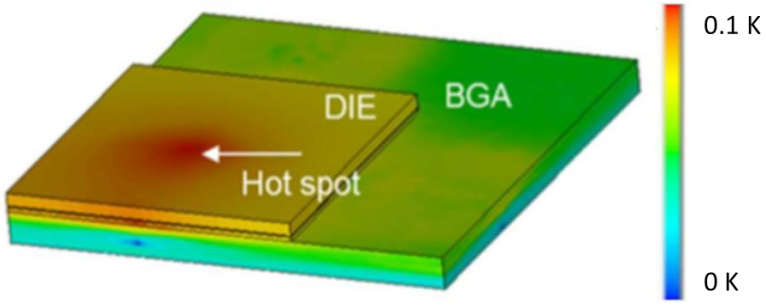

Figure 1.30: FEM calculations of the temperature rise at the package level [92].

A FEM model of the temperature field at the BEOL and die levels is shown in Figure 1.30 [92]. For FEM consisting of geometries with large aspect ratios (i.e. large number of finite elements), a multiscale modelling strategy is required to reduce the computational time. The principle of the FEM multiscale modelling strategy is explained in Chapter 3. This allows, among other things, to calculate temperature gradients and thermomechanical stress in a TSV. An example is illustrated in Figure 1.31 [93].

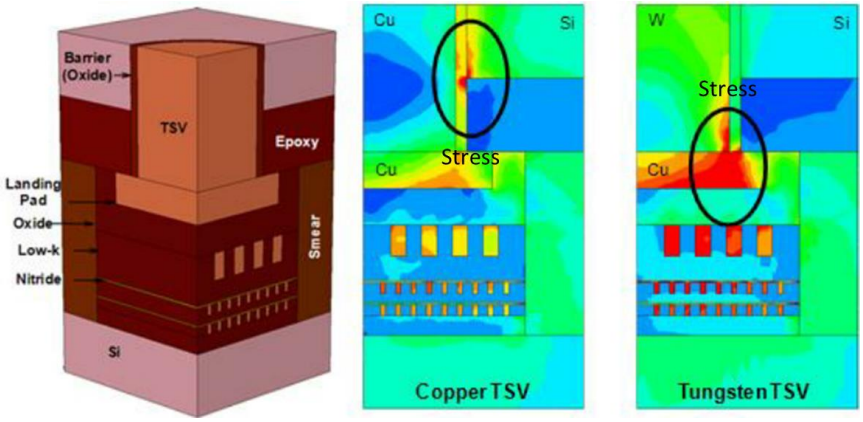

Figure 1.31: FEM model for the calculation of mechanical stress in a TSV [93].

III.3.D. Conclusion on the simulation methods and selection

FEM with the simulation package COMSOL is selected in this thesis, due to the possibility of multiphysics coupling (numerous libraries of data are included) and the previous works both at ST and at CETHIL. However, only macroscopic parameters can be included, so particular caution will be paid to the selection of the parameters such as thermal conductivity and thermal boundary resistance (TBR) in the following work. In particular, TBR will be computed directly at the phonon level (see Chapter 2) before being included in the FEM simulations.

IV. Summary

In this chapter, the main trends of microelectronics and some process flows have been reviewed briefly. The 3D integration scheme provides new capabilities in terms of integration and miniaturization. The imager technology is a good candidate for this kind of integration. The pixel matrix and digital components can thus be stacked to reduce the die footprint and improve performance. However, thermal phenomena in such object are of primary importance. Indeed, the decrease in

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volume coupled with a constantly increasing power induces many challenges to limiting the temperature rise. On top of these issues, optical performance is highly sensitive to temperature variations. In that context, some general solutions for heat dissipation at the package level have been introduced.

This PhD work falls in that context. The thermal behavior of 3D IMG ICs, being a sensitive item, needs to be perfectly understood and controlled to be optimized. Note that the scale of the current study is limited to that of the BEOL, i.e. over a micrometer. Thus, the transistor scale will not be discussed but only considered as a power source.

The first step of this work is to properly evaluate the thermal properties of our materials. This task is developed in the next chapter. Experimental methods will be described and the main materials embedded in the BEOL will be characterized. In a second step, the numerical methods will be investigated in Chapter 3. Their accuracies and relevancies will be discussed and validated by means of comparisons with experimental observations performed on dedicated test chips. Finally, the methods and the know-how developed in Chapter 2 and Chapter 3 will be applied to investigate two specific 3D IMG ICs. Among others, the thermal gradient and the possibility of hot spot on the surface, will be investigated to analyze the impact on the pixel thermal behavior.

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V. Bibliography

[1] P.A. Laplante, Comprehensive Dictionary of Electrical Engineering, 2nd edition, Page 739, 2005.

[2] J. Czochralski, A new method for the measurement of the crystallization rate of metals, Zeitschrift für Physikalische Chemie, Volume 92, Pages 219-221, 1918.

[3] S.L. Partridge, Silicon-on-insulator technology, IEEE Proceedings I – Solid State and Electron Devices, Volume 133, Issue 3, Pages 66-76, 1986.

[4] G.K. Celler, Frontiers of silicon-on-insulator, Journal of Applied Physics, Volume 93, Issue 9, Page 4955, 2003.

[5] A. Marshall and S. Natarajan, SOI Design: Analog, Memory and Digital Techniques, 2002.

[6] R.C. Leachman et al., Economic Analysis of wafer Fabrication, Proceeding of T-ASE, Volume 4, Issue 4, Pages 501-512, 2007.

[7] C.F. Chien et al, Economic Analysis of 450mm Wafer Migration, Symposium on Semiconductor Manufacturing, 2007.

[8] E.R. Fossum, CMOS image sensors: electronic camera-on-a-chip, Transactions on Electron Devices, Volume 44, Issue 10, Pages 1689-1698, 1997.

[9] H.Z. Massoud et al, Thermal Oxidation of Silicon in Dry Oxygen Growth-Rate Enhancement in the Thin Regime, Journal of The Electrochemical Society, Volume 132, Issue 11, Pages 2685-2693 , 1985.

[10] R.C. Jaeger, Lithography, Introduction to Microelectronic Fabrication, 2nd Edition, 2002.

[11] A.J. Armini et al., Non-mass-analyzed Ion Implantation Equipment for High Volume Solar Cell Production, Proceeding of PVSC, Pages 895-899, 1982.

[12] A. Litty, Conception, fabrication, caractérisation et modélisation de transistors MOSFET haute tension en technologie avancée SOI (Silicon-On-Insulator), PhD thesis, Université Grenoble-Alpes, 2006.

[13] L.R. Harriott, Limits of Lithography, Proceeding of IEEE, Volume 89, Issue 3, 2001.

[14] M. Rothschild et al., Photolithography at 193 nm, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, Volume 10, Issue 6, Page 2989, 1992.

[15] R.D. Allen et al., Photoresist for 193-nm lithography, IBM Journal of Research and Development, Volume 41, Issue 1, Pages 95-104, 1997.

[16] R.H. Stulen et al., 13-nm extreme ultraviolet lithography, Journal of Selected Topics in Quantum Electronics, Volume 1, Issue 3, Pages 970-975, 1995.

[17] J. Tao et al., Electromigration Reliability of Tungsten and Aluminum Vias and Improvements Under AC Current Stress, IEEE Transactions on Electron Devices, Volume 40, Issue 8, Pages 1398-1405, 1993.

[18] V. Kamineni et al., Tungsten and cobalt metallization: A material study for MOL local interconnects, Proceeding of IITC/AMC, 2016.

[19] D. Shamiryan et al., Low-k dielectric materials, Materials Today, Volume 7, Issue 1, Pages 34-39, 2004.

[20] P.S. Raja and R.J. Daniel, Low-K Dielectrics for Nanoscale MOSFETS, Procedia Engineering, Volume 38, Pages 2048-2052, 2012.

[21] F. Wolny, Reduced metal contamination from crucible and coating using a silicon nitride based diffusion barrier for the growth of cast quasi-single crystalline silicon ingots, Journal of Crystal Growth, Volume 514, Pages 49-53, 2019.

[22] C.K. Hu et al., Copper interconnection integration and reliability, Thin Solid Films, Volume 262, Issues 1-2, Pages 84-92, 1995.

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[23] A. Paduthol et al., Impact of different capping layers on carrier injection efficiency between amorphous and crystalline silicon measured using photoluminescence, Solar Energy Materials and Solar Cells, Volume 187, Pages 55-60, 2018.

[24] X. Yu and K. Weide, A study of the thermal- electrical- and mechanical influence on degradation in an aluminum-pad structure, Microelectronics Reliability, Volume 37, Issues 10-11, Pages 1545-1548, 1997.

[25] P. Garrou et al., Handbook of 3D Integration, Volume 1: Technology and Applications of 3D Integrated Circuits, Pages 1-11, 2011.

[26] J.U. Knickerbocker et al., Three-dimensional silicon integration, IMB Journal of Research and Development, Volume 52, Issue 6, Pages 553-569, 2008.

[27] K. Salah, TSV-Based 3D Integration Fabrication Technologies: An Overview, Symposium of IDT, 2014.

[28] H.K. Kung and C.L. Hsieh, A theoretical study to improve wire sag of ultra-long wire bond loops for 3D/MCM packaging, Microelectronics Reliability, Volume 78, Pages 272-279, 2017.

[29] C.T. Ko et al., Wafer-to-Wafer Hybrid Bonding Technology for 3D IC, Proceeding of ESTC, 2010.

[30] C.T. Ko and K.N. Chen, Wafer-level bonding/stacking technology for 3D integration, Microelectronic Reliability, Volume 50, Pages 481-488, 2010.

[31] C.T. Ko and K.N. Chen, Low temperature bonding technology for 3D integration, Microelectronics Reliability, Volume 52, Pages 302-311, 2012.

[32] C. Sart et al., Numerical and Experimental Investigations on the Hybrid Bonding of Cu/SiO_2 Patterned Surfaces using a Cohesive Zone, Proceeding of EuroSimE, 2016.

[33] T. Sakuishi et al., Advantage of direct etching method and process integration for TSV reliability, Proceeding of ICEP, 2015.

[34] Y.C. Tan et al., Electromigration performance of Through Silicon Via (TSV) – A modeling approach, Microelectronic Reliability, Volume 50, Pages 1336-1340, 2010.

[35] K. Xia et al., Modeling simplification for thermal mechanical stress analysis of TSV interposer stack, Microelectronic Reliability, Volume 96, Pages 46-50, 2019.

[36] L. Di Cioccio et al., An Overview of Patterned Metal/Dielectric Surface Bonding: Mechanism, Alignment and Characterization, Journal of The Electrochemical Society, Volume 158, Issue 6, Pages 81-86, 2011.

[37] C. Sart et al., Cu/SiO_2 Hybrid Bonding: Finite Element Modeling and Experimental Characterization, Proceeding of ESTC, 2016.

[38] M. Kumar, Le Grand Roman de la physique quantique, Flammarion, Page 636, 2012.

[39] H. Häberlin, Photovoltaics: System Design and Practice, John Wiley & Sons, 2012.

[40] R.F. Pierret, Semiconductor Device Fundamentals, 2nd Edition, Pages 209-216, 1996.

[41] A. Pelamatti, Estimation and modeling of key parameters of pinned photodiode CMOS image sensors for high temporal resolution applications, PhD Thesis, Université de Toulouse, 2015.

[42] G.C. Holst, CCD ARRAYS, CAMERAS, and DISPPLAYS, 2nd Edition, SPIE Optical Engineering Press, 1996.

[43] P. Magnan, Detection of visible photons in CCD and CMOS: A comparative view, Nuclear Instrument and Methods in Physics Research, Volume 504, Pages 199-212, 2003.

[44] X. Liu et al., CCD/CMOS Hybrid FPA for Low Light Level Imaging, Infrared and Photoelectric Imagers and Detector Devices, Proceeding of SPIE, 2005.

[45] H. Eslampour et al., Thermally enhanced and thin IP chip packages for Tablet processor applications, Proceeding of ECTC, 2013.

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[46] T.L. Phan et al., Integrated vapor chamber heat spreader for high power processors, Proceeding of ICEP, 2014.

[47] P. Becker et al., The lattice parameter of highly pure silicon single crystals, Zeitschrift für Physik, Volume 48, Issue 1, Page 17, 1982.

[48] V. Fiori, How do Mechanics and Thermo mechanics affect microelectronic products: Some residual stress and strain effects, investigations and industrial management, PhD Thesis, 2010.

[49] P. Merken and R. Vandersmissen, Dark Current and influence of target emissivity, Photonics & Imaging Technology, Pages 11-14, 2016.

[50] R.N. Clark, On-Sensor Dark Current Suppression Technology Dark Frames Are No Longer Necessary, website: www.clarkvision.com, 2016.

[51] B. Pain et al., Analysis and enhancement of low-light level performance of photodiode-type CMOS active pixel imagers operated with sub-threshold reset, Proceeding of CCDAIS, 1999.

[52] J. Lai and A. Nathan, Reset noise in active pixel image sensors, Journal of Vacuum Science and Technology A, Volume 22, Issue 3, Pages 987-990, 2004.

[53] H. Tian, Noise analysis in CMOS image sensors, Thesis, Stanford University, 2000.

[54] A. Boukhayma et al., Temporal Readout Noise Analysis and Reduction Techniques for Low-Light CMOS Image Sensors, Transactions on Electron Devices, Volume 63, Issue 1, Pages 72-78, 2015.

[55] J.R. Black, Electromigration – A brief Survey and Some Recent Results, Transaction of Electron Devices, Volume 16, Issue 4, Pages 338-347, 1969.

[56] S.R. Wilson et al., Handbook of multilevel metallization for integrated circuits, 1st Edition, Materials, technology and applications, Page 607, 1993.

[57] L. Micheli et al., Performance, limits and economic perspectives for passive cooling of High Concentrator Photovoltaics, Solar Energy Materials and Solar Cells, Volume 153, Pages 164-178, 2016.

[58] C.J.M. Lasance, Technical Data, ElectronicsCooling, website: www.electronics-cooling.com 1997.

[59] S.S. Tonapi et al., An overview of thermal management for next generation microelectronic devices, Proceeding of ASMC 2003.

[60] J. Xu and T.S. Fisher, Enhancement of thermal interface materials with carbon nanotube arrays, International Journal of Heat and Mass Transfer, Volume 49, Issues 9-10, Pages 1658-1666, 2006.

[61] A. Yu et al., Graphite Nanoplatelet-Epoxy Composite Thermal Interface Materials, The Journal of Physical Chemistry C, Volume 111, Issue 21, Pages 7565-7569, 2007.

[62] T. Acikalin et al., Experimental Investigation of the Thermal Performance of Piezoelectric Fans, Heat Transfer Engineering, Volume 25, Issue 1, Pages 4-14, 2004.

[63] S. Garimella and C. Sobhan, Transport in Microchannels – A Critical Review, Annalytical Review of Heat Transfer, Volume 13, Pages 1-50, 2001.

[64] S. Kandilikar and H. Upadhye, Extending the Heat Flux Limit With Enhanced Microchannels in Direct Single-Phase Cooling of Computer Chips, Proceeding of SEMI-THERM, 2005.

[65] E. Colgan et al., A Practical Implenentation of Silicon Microchannel Coolers for High Power Chips, Proceeding of SEMI-THERM, 2003.

[66] D.L. Blackburn, Temperature measurements of semiconductor devices – a review, Proceeding of SEMI-THERM, 2004.

[67] M.B. Patil, Diode as a Temperature Sensor, Indian Institute of Technology Bombay, 1992.

[68] J.J.L. Franco and E. Boemo, Ring oscillators as thermal sensors in FPGAs: Experiments in low voltage, Proceeding of SPL, 2010.

[69] M.K. Mandal and B.C. Sarkar, Ring oscillators: Characteristics and applications, Indian Journal of Pure & Applied Physics, Volume 48, Pages 136-145, 2010.

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[70] A. Dasdan and I. Hom, Handling Inverted Temperature Dependence in Static Timing Analysis, Transactions on Design Automation of Electronic Systems, Volume 11, Issue 2, Pages 306-324, 2006.

[71] M. Kuball and J.W. Pomeroy, A Review of Raman Thermography for Electronic and Opto-Electronic Device Measurement With Submicron Spatial and Nanosecond Temporal Resolution, Transactions on Device and Materials Reliability, Volume 16, Issue 4, Pages 667-684, 2016.

[72] G.S. Doerk et al., Single Nanowire Thermal Conductivity Measurements by Raman Thermography, ACS Nano, Volume 4, Issue 8, Pages 4908-4914, 2010.

[73] J.C.H. Phang et al., A review of near infrared photon emission microscopy and spectroscopy, Proceeding of IPFA, 2005.

[74] InfraTec Inc, Infrared Thermography in Electronics and Electrical Industry, website: www.infratec-infrared.com, 2019.

[75] J. Christoffersen and A. Shakoui, Thermal measurements of active semiconductor micro-structures acquired through the substrate using near IR thermoreflectance, Microelectronics Journal, Volume 35, Issue 10; Pages 791-796, 2004.

[76] J. Christoffersen et al., Thermoreflectance Thermal Imaging as thermal characterization technique for microelectronics, Applied Physics, Volume 39, Pages 4153-4166, 2006.

[77] J. Christoffersen and A. Shakouri, Thermoreflectance based thermal microscope, Review of Scientific Instruments, Volume 76, Issue 2, Page 1063, 2005.

[78] S. Gomes et al., Scanning thermal microscopy: A review, Physica Status Solidi, Volume 212, Issue 3, 2015.

[79] Y. Ge et al., Dimension- and shape-dependent thermal transport in nano-patterned thin films investigated by scanning thermal microscopy, Nanotechnology, Volume 28, Issue 48, Pages 1-13, 2017.

[80] S. Sarikurt et al., Tailoring thermal conductivity of silicon/germanium nanowires utilizing core-shell architecture, Journal of Applied Physics, Volume 119, Page 155101, 2016.

[81] S.G. Volz and G. Chen, Molecular dynamics simulation of thermal conductivity of silicon nanowires, Applied Physics Letters, Volume 75, Page 2056, 1999.

[82] J.D.N. Cheeke and H.E. Hebral, Analysis of heat transfer between solids at low temperatures, Canadian Journal of Physics, Volume 54, Pages 1749-1771, 1976.

[83] M.S. Jeng et al., Monte Carlo Simulation of the Thermal Conductivity and Phonon Transport in Nanocomposites, Proceeding of ASME, 2005.

[84] G. Chen, Nanoscale Energy Transport and Conversion: A Parallel Treatment of Electrons, Molecules, Phonons, and Photons, 1st Edition, MIT-Pappalardo Series in Engineering, 2005.

[85] Z. Cheng et al., Lattice Monte Carlo simulation of thermal conductivity in composite materials, Proceeding of HEFAT, 2014.

[86] E.T. Swartz and R.O. Pohl, Thermal boundary resistance, Reviews of Modern Physics, Volume 61, Issue 3, Pages 605-668, 1989.

[87] Y. Shen et al., Finite difference schemes for heat conduction analysis in integrated circuit design and manufacturing, International Journal of Circuit Theory and Applications, Volume 39, Issue 9, Pages 905-921, 2011.

[88] H.C. Chien et al., Thermal Evaluation and Analyses of 3D IC Integration SiP with TSVs for Network System Applications, Proceeding of ECTC, 2012.

[89] A. Todri, A Study of Tapered 3-D TSVs for Power and Thermal Integrity, Transaction on Very Large Scale Integration Systems, Volume 21, Issue 2, Pages 306-319, 2013.

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[90] L. Choobineh and A. Jain, Analytical Solution for Steady-State and Transient Temperature Fields in Vertically Stacked 3-D Integrated Circuits, Transactions on Components, Packaging and Manufacturing Technology, Volume 2, Issue 12, Pages 2031-2039, 2012.

[91] J.H. Lau and T.G. Yue, Thermal management of 3D IC integration with TSV (through silicon via), Proceeding of ECTC, 2009.

[92] G. Garegnani et al., Numerical analysis of thermal effects in SOI MOSFET flip-chip packages: multi-scale studies on isolated transistors and global simulations, Proceeding of ESTC, 2016.

[93] X. Xu and A. Karmarkar, 3D TCAD modeling of stress management in through silicon via (TSV) stacks, Proceeding of AIP, Pages 53-66, 2011.

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Chapter 2. Thermal characterization of materials typically used in microelectronics

In this chapter, the aim is to determine the thermal properties of different materials used in three-dimensional imagers (IMG3D). To do so, two different techniques will be used and compared: Scanning Thermal Microscopy (SThM) and 3ω method. The materials will be described first, then the SThM technique will be applied with both nano and micro probes and finally, the 3ω method will be used for some samples.

I. Materials and associated samples

In this thesis, different materials, all used and developed at STMicroelectronics clean rooms, have been selected. These materials are used at different steps during the process of fabrication of the chip. First, the samples used in the Front-End-Of-Line (FEOL) will be introduced and then, the Back-End-Of-Line (BEOL) samples will be detailed.

I.1. Front-End-Of-Line

I.1.A. Bulk silicon sample

The bulk silicon substrate, used for a lot of microelectronics technologies is also called a wafer. All the wafers used in STMicroelectronics have the same following characteristics: their thickness is about 750 µm and they are all single-crystal silicon with p-doping (approximately 10^{15} atom.cm^{-3}) fabricated with the Czochralski process [1]. Considering these properties, the thermal conductivity of the silicon bulk is estimated to be 148 W.m^{-1}.K^{-1} [2].

I.1.B. Silicon-on-Insulator sample

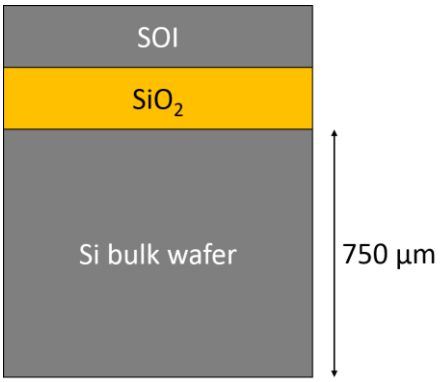

Figure 2.1: Schematics of the cross section of the SOI technology deposited on a silicon wafer.

Besides 3D technologies, Silicon-On-Insulator (SOI) technologies have seen considerable progress in the development of high-performance devices [3]. However, some questions remain regarding their thermal performance. The SOI film is a layer of single-crystal silicon which is grown above a silicon dioxide layer. It allows significant advantages in terms of performance and consumption of semiconductor circuits without increasing the process flow much (compared to other technologies such as FinFET for example). Silicon transistors with nanometer channel length can also be realized by means of the SOI technology (<14 nm) [4]. The SOI samples used in this work are presented in Figure 2.1 and Table 2.1. MEMC and SOITEC samples have identical sizes but they are produced by different suppliers.

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Sample	SOI thickness (nm)	SiO_2 thickness (nm)
PIC25	310	720
MEMC	160	400
SOITEC	160	400
FDSOI	12	25

Table 2.1: Characteristics of the different SOI samples used in this work.

I.2. Back-End-Of-Line

The materials used in the interconnection levels have to face thermomechanical [5] and electrical issues [6]. The BEOL samples are detailed in Figure 2.2 and Table 2.2. The thicknesses are chosen to be representative of the layers which are present in the real electronic devices. Two thicknesses are used for each material in order to interpret the thermal property of the layer in terms of both interface and volume characteristics of the sample.

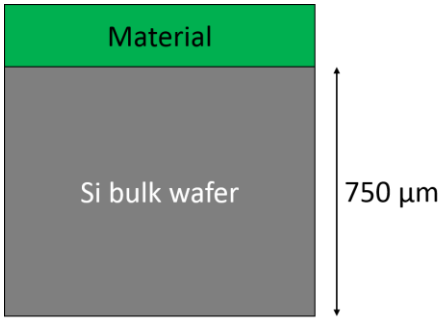

Figure 2.2: Schematics of the cross section of a thin-layer material deposited on a silicon wafer.

Sample	Material	Thickness (nm)
USG 2900	SiO_2	290
USG 5400	SiO_2	540
SiN 300	SiN	30
SiN 600	SiN	60
SiCN 350	SiCN	35
SiCN 600	SiCN	60
BD1 3300	SiCOH	330
BD1 5600	SiCOH	560
ULK 1250	Porous SiO_2	125
ULK 2400	Porous SiO_2	240

Table 2.2: Characteristics of the different samples used in this work.

II. Characterization by Scanning Thermal Microscopy

For the characterization of the thermal conductivity of thin films, different techniques are available, for example thermoresistive or thermo-optical methods [7-9]. Indeed, according to the sample dimension or the expected range of thermal conductivity, the best technique will differ. We decided first to focus on SThM technique. First, the principle of the SThM technique will be explained and then the results obtained with two different probes will be analyzed.

II.1. Scanning Thermal Microscopy technique

SThM is a contact probe technique that allows to obtain a thermal signal at sub-micrometric scale. It allows measurement of thermal variables/parameters such as temperature, thermal conductivity or phase transition temperature for example. In SThM, qualitative analyses are performed quickly but the

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interpretation of the experimental data remains challenging. Indeed, in order to allow quantitative data analysis, the understanding of the heat transfer mechanisms between the probe and the sample still needs deep investigations. Most of the time, the experimental data are interpreted by means of a numerical model of the thermal system. The SThM setup and its electrical circuit used during the thesis are presented below.

II.1.A. Setup for SThM

SThM is a technique based on Atomic Force Microscopy (AFM). It is a non-destructive technique that allows the characterization of sample materials with high spatial resolution. A schematic of SThM is presented in Figure 2.3. The probe used in SThM allows determining the temperature at the tip apex by measuring the probe electrical resistance. This measurement is based on the material thermoresistive property:

$$\Delta R = R_0 \alpha \Delta T, \tag{2.1}$$

$$\Delta T = T - T_0, \tag{2.2}$$

$$\Delta R = R - R_0, \tag{2.3}$$

where R and R_0 are the electrical resistances of the probe respectively at ambient temperature T and reference one T_0, and $\alpha = \frac{1}{R}\frac{dR}{dT}$ is the probe temperature coefficient of electrical resistivity (TCR). The value of the electrical resistance T_0 and its TCR α are determined experimentally to determine the probe temperature with good accuracy. The technique can be used in two different modes. In the temperature contrast mode (TCM), low current in the probe is used to map the temperature at the surface of samples, which varies due to additional heat sources in the sample. In the conductivity contrast mode (CCM), a high current is supplied to the probe to inject a heat flux into the sample. The probe is therefore the heater and also the sensor. The CCM will be used here to determine effective thermal conductivities of our samples. The experiments are performed with different probes set on a NT-MDT AFM.

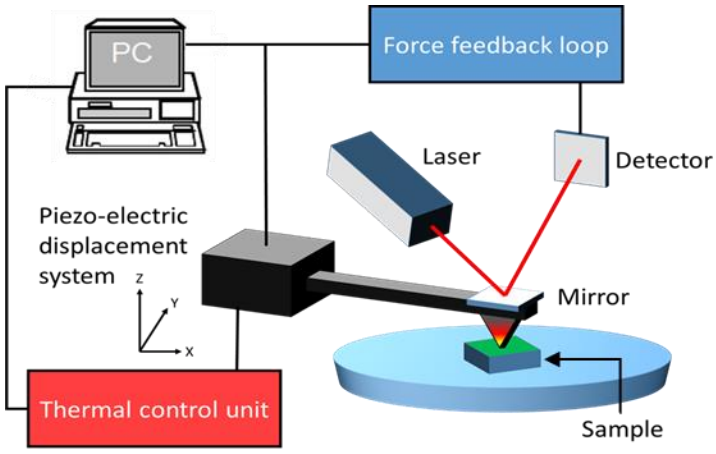

Figure 2.3: Principle of a scanning thermal microscope.

II.1.B. Measurement method

To characterize the thermal conductivity of the sample, a large current is supplied in the electrical resistance and generates heat by Joule effect. Heat dissipates into the sample when the probe is in contact with the sample surface as shown in Figure 2.4. First, the electrical resistance is measured far from the sample, so heat dissipation occurs only due to heat conduction in the cantilever and losses through air. In a second step, the electrical resistance is measured with the tip apex in contact with

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the sample. In this second case, part of the Joule-heated generated power is dissipated into the sample and losses in the air are suppressed (no air convection between the tip and the sample). The variation of the electrical resistance at the probe apex ΔR_{sample} is characteristic of the effective thermal conductivity of the sample:

$$\Delta R_{sample} = R_{far} - R_{sample}, \tag{2.4}$$

where R_{far} is the resistance of the probe out of contact in air or in vacuum and R_{sample} is the resistance of the probe in contact with the sample. The variation of resistance measured on each sample is normalized by the same measurement done on a reference sample. The thermal signal f is therefore:

$$f(sample) = \frac{\Delta R_{sample}}{\Delta R_{silicon}}, \tag{2.5}$$

where $\Delta R_{silicon}$ is the variation of the electrical resistance at the probe apex for a bulk silicon wafer.

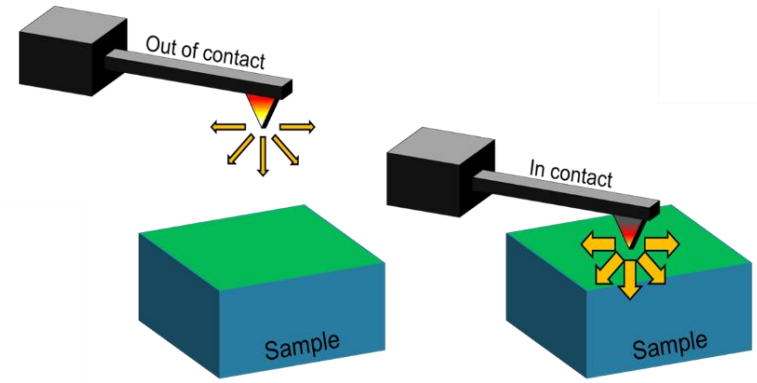

Figure 2.4: Method of measurement in SThM

II.1.C. Electrical circuit

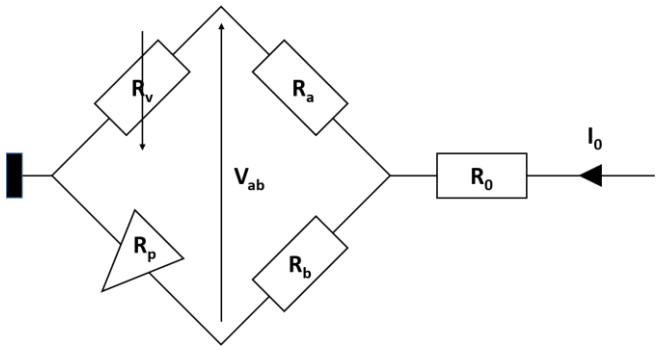

Figure 2.5: Electrical circuit of the Wheatstone bridge.

Considering that the typical values of TCRs for thermoresistive materials are comprised between a few 10^{-4} and a few 10^{-3} K^{-1}, a high precision is mandatory for the measurement of the ratio between ΔR and R_0. The measurements of probe electrical resistances are operated using a balanced Wheatstone bridge under ambient conditions ($T_{room} = 27$ °C and relative humidity $RH = 40\%$). The electrical setup is presented in Figure 2.5. In our setup, R_0 is equal to 100 Ω and allows to measure the current, R_a and R_b are as large as possible (usually a few thousands of ohms), R_p the resistance of the electrical resistance of the probe and R_v a variable resistance chosen to equilibrate the bridge, i.e. to have the voltage V_{ab} equal to 0 V at room temperature. In this work, an additional amplifier with gain $G_{amplifier}$

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equal to 500 is added on the voltage V_{ab} to improve the sensitivity of the measurement of the resistance of the probe R_p.

II.2. Characterization with the palladium nano-probe

Details on the palladium nano-probe will be provided, then the experimental data and their numerical interpretation by Finite Element Modelling (FEM) will be described. Finally, the performances of the SThM technique with palladium nano-probe will be summarized.

II.2.A. Palladium nano-probe

The experiments are performed with the palladium nano-probe, which involves an AFM probe with a Si_3N_4 cantilever. The metallic wires are made of palladium and the apex radius of curvature is smaller than 100 nm. This very small probe allows measurement with a high spatial resolution. A Scanning Electron Microscopy (SEM) image of the probe is shown in Figure 2.6.

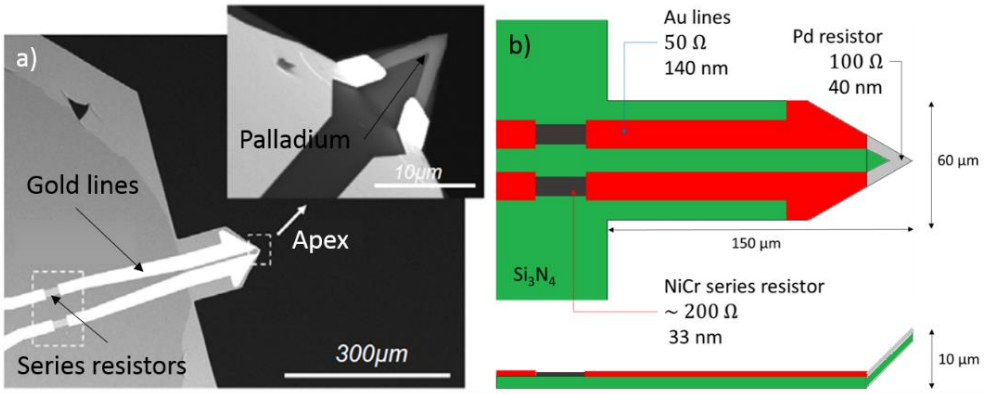

Figure 2.6: a) SEM image [D. Renahy, 2016] and b) geometry of the palladium nano-probe.

II.2.B. Experimental measurement

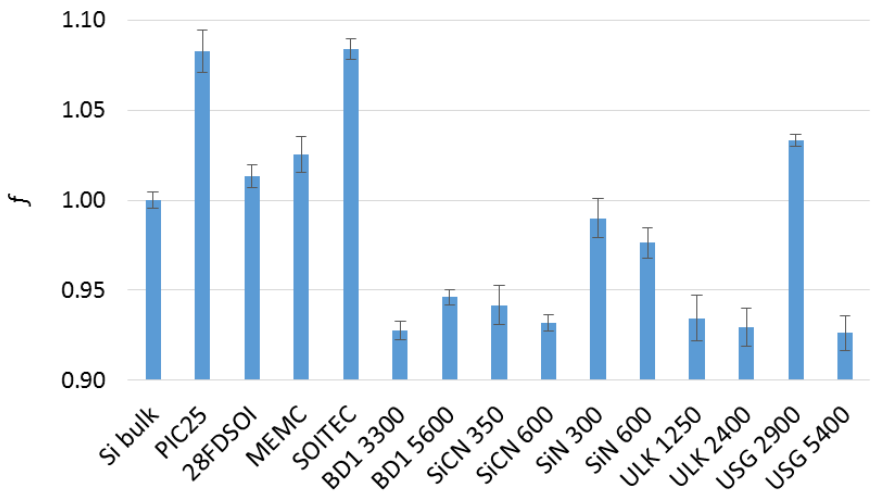

Figure 2.7: Thermal signal f with the palladium nano-probe for different samples.

During these measurements, a current $I = 1$ mA is feeding the probe. Considering a resistance of palladium equal to 100 Ω approximately, the Joule power generated is equal to 10 mW. With these experimental conditions, the decrease of electrical resistance of the probe can be easily measured between far-from-contact and contact modes. The experimental data are shown in Figure 2.7. One can notice that the thermal signal is measured higher than 1 for some samples, which is not expected since

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the silicon reference is supposed to provide the largest signal of all these samples. This is due to a thermal drift not measured experimentally in this study. In the future, the reference signal will be measured just before and right after each sample. However, all the measurements of thermal signal *f* are characteristic of the sample in contact with the probe. In order to interpret these measurements, a model needs to be developed. In our case, a Finite Element Method is chosen. This model will be developed in order to determine the effective thermal conductivity of each sample.

II.2.C. Numerical modelling by FEM

In this part, the modelling of the probe-sample system will be detailed. First, the thermoresistive properties of the palladium probe and its environment will be characterized, then the probe-sample contact interactions will be studied. Finally, the physics of the heat flow at the tip-sample contact will be explained, studied and integrated in the global FEM model.

II.2.C.a. Determination of metal thermoresistive properties

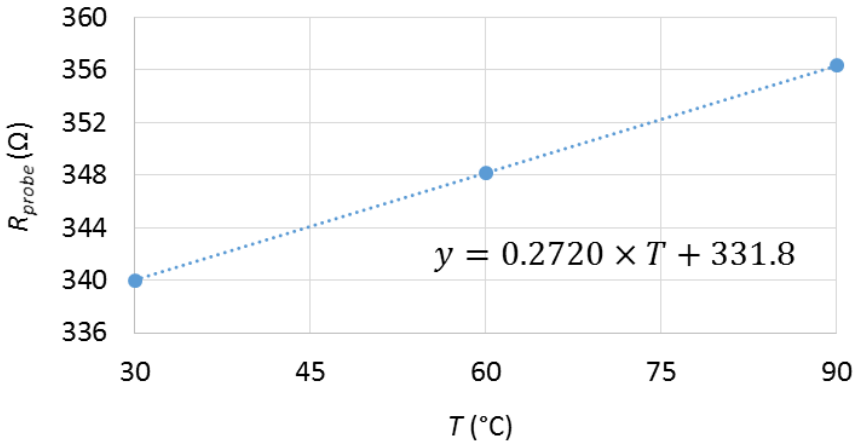

Figure 2.8: Measurement and determination of the probe resistance and TCR respectively.

Figure 2.6 shows that three different metals are involved: palladium (Pd), gold (Au) and nichrome (NiCr). In order to quantify the electrical resistance and TCR of each metal, we observe that the resistances are in series:

$$R_{0probe} = \sum_i R_{0i}, \tag{2.6}$$

$$R_{0probe} \times \alpha_{probe} = \sum_i R_{0i} \times \alpha_i, \tag{2.7}$$

$$i = Pd, Au, NiCr$$

where R_0 is resistance at room temperature and α is the TCR of the probe and each metal, respectively. The resistance of the probe R_{probe} is measured at different temperatures in a thermal furnace in Figure 2.8. R_{0probe} is measured equal to 340 Ω and R_{0Au} and R_{0Pd} are taken from the manufacturer data. α_{probe} is also measured, while α_{Pd} and α_{NiCr} are given by E. Puyoo [10]. Considering Eq. (2.6) and Eq. (2.7), we are able to get the data summarized in Table 2.3.

	Probe	**Pd**	**NiCr**	**Au**
R_0 (Ω)	340	100	190	50
ΔR_0 (Ω)	0	10	20	10
(10^{-3} K^{-1})α	0.82	1.20	0.24	2.2
(10^{-3} K^{-1})$\Delta\alpha$	0	0.01	0.01	0.3

Table 2.3: Summary of material thermoresistive properties.

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II.2.C.b. *Characterization of the thermal environment of the probe*

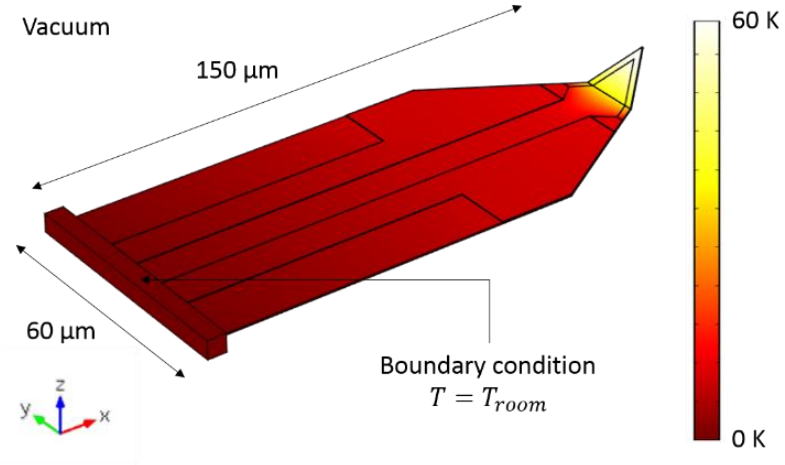

Figure 2.9: FEM modelling of the probe temperature rise far from contact in vacuum.

Initially, the cantilever thermal conductivity k_{SiN} is unknown. To solve this issue, the FEM model of the cantilever including k_{SiN} is fitted to match the experimental apex temperature as shown in Figure 2.9. The thermal resistances between materials are neglected and will be taken into account in k_{SiN}. The experiment is performed under vacuum conditions ($P < 0.2$ mbar) to avoid heat transfer through air. k_{SiN} is found equal to 2.93 W.m^{-1}.K^{-1} which is in good agreement with [11].

Second, by fitting the previous model under ambient conditions, heat losses through air can be determined. The heat loss coefficient (h_{air}) is found to be equal to 4500 W.m^{-2}.K^{-1}, which is in good agreement with the values obtained by A. M. Massoud [12]. In addition, an analytical study is performed to determine potential losses by radiation. Indeed, at the first order, the emittance can be approximated like a heat flux boundary condition h_{rad}:

$$h_{rad} = 4\sigma\varepsilon_s T_{room}^3, \tag{2.8}$$

where T_{room} is the room temperature equal to 300 K, ε_s is the emissivity between 0 and 1 and σ is the Stefan-Boltzmann constant equal to 56.7 nW.m^{-2}.K^{-4}. In this condition, h_{rad} is below 5.7 W.m^{-2}.K^{-1} and can be neglected in comparison with the heat losses through air. One can note that this analysis is neglecting sub-wavelength effects and near-field contributions. Some more accurate analysis will be performed later.

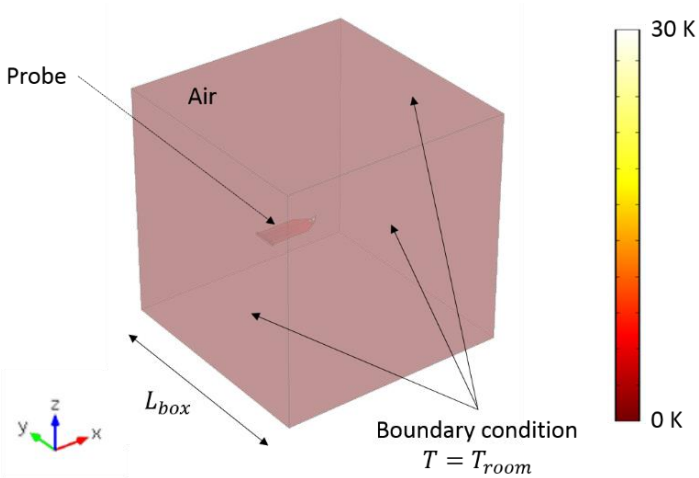

Figure 2.10: Temperature rise in the probe with the air domain and surface boundary condition.

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Finally, we underline that the heat flux lost in the environment due to air convection at the tip surface can be represented as a diffusive air domain surrounding the tip [12]. The air convection, which is very difficult to simulate numerically, is replaced by an equivalent conduction mechanism into a domain of width L_{box} equal to 4 mm. The domain is centered on the tip apex and boundary condition on its faces is a fixed temperature set at T_{room} (see Figure 2.10). With this procedure, the thermal balance is kept conserved. Considering the right properties of the metals and silicon nitride cantilever, and the description of the heat losses through air by an equivalent air domain, the environment of the probe far from contact is totally described. We will now take into account the influence of the contact between the probe and the sample on the heat path and its associated ballistic effects.

II.2.C.c. Probe-sample contact characterization

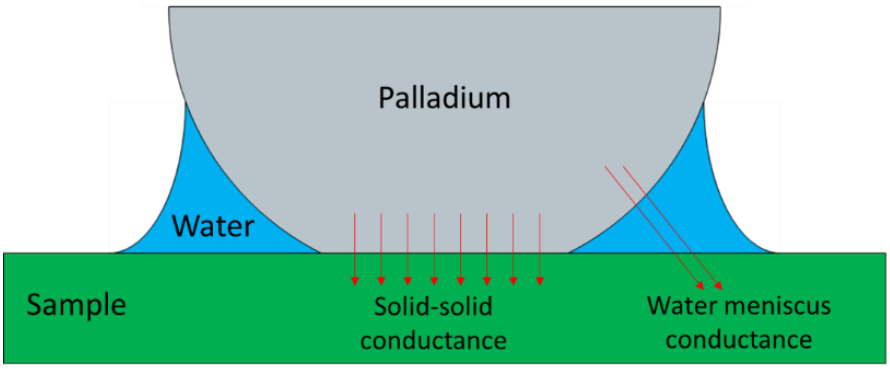

Figure 2.11: Probe-sample thermal interactions in contact mode [14]

Various heat transfer mechanisms coexist at the palladium nano-probe contact [8, 9, 12-14] and have to be taken into account. The contact conductance at the tip apex in Figure 2.11 is estimated analytically. The conductance of the contact $G_{contact}$ is therefore:

$$G_{contact} = G_{solid} + \frac{1}{\frac{1}{G_{p/w}} + \frac{1}{G_{water}} + \frac{1}{G_{w/s}}}, \tag{2.9}$$

where G_{solid}, $G_{p/w}$ and $G_{w/s}$ are the palladium/sample, palladium/water and water/sample interface conductances, respectively. G_{water} is the conductance of the water meniscus. All these conductances are estimated below.

<u>Water meniscus conductance</u>

On the one hand, the conductance of the water G_{water} can be estimated analytically following Assy et al. [8, 14]. In order to perform all the calculations, the contact angle of water on each material is needed. Two different setups have been used at STMicroelectronics and at CETHIL and show similar results. Figure 2.12 shows the test bench for the measurement of the water drop contact angle θ_c. The measured values of θ_c and G_{water} for each surface material are summarized in Table 2.4.

Material	θ_c (°)	$\pm\Delta\theta_c$ (°)	G_{water} (nW.K^{-1})	$\pm\Delta G_{water}$ (‰)
Silicon	25	5	41.0	3.8
BD1	33	4	31.8	2.4
SiCN	60	3	120	1.4
SiN	18	6	87.4	5.5
ULK	53	3	57.4	1.4
USG	24	5	75.1	3.8

Table 2.4: Contact angle measurements and calculated water conductance per surface material.

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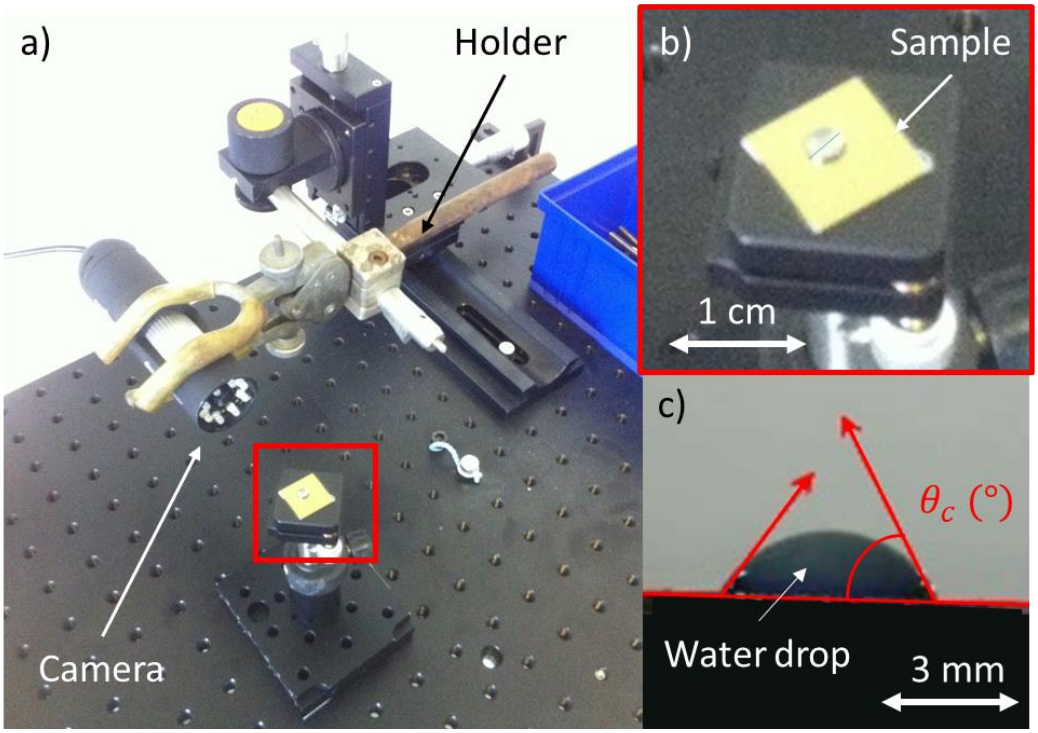

Figure 2.12: a) Test bench for the measurement of the contact angle. b) Optical image of the drop on the sample. c) Optical image of the water drop and its associated contact angle.

Thermal boundary conductances (TBC)

The different TBC G_{solid}, $G_{p/w}$ and $G_{w/s}$ are estimated with both the Acoustic and Diffuse Mismatch Models (AMM and DMM) [15, 16]. The Debye model is used for amorphous materials, while transverse modes are suppressed for liquids. The principle of the AMM and DMM theories is explained in Chapter 1 Section III.3.B.

An estimation for $G_{p/w}$, $G_{w/s}$ and G_{solid} is available for each sample surface. In this study, the radius of curvature of the probe is estimated to 100 nm. In addition, the tip-sample contact area has a radius estimated to 10 nm following [8]. AMM and DMM models allow to calculate respectively the minimum and maximum interface conductance (see Table 2.5).

Material	$G_{p/w}$ (nW.K^{-1})		$G_{w/s}$ (nW.K^{-1})		G_{solid} (nW.K^{-1})	
	AMM	DMM	AMM	DMM	AMM	DMM
Silicon	26.5	110	0.669	1.16	82.4	173
BD1	-	-	-	-	-	-
SiCN	-	-	-	-	-	-
SiN	40.3	168	0.266	1.29	60.5	124
ULK	-	-	-	-	-	-
USG	37.8	154	1.94	3.13	114	231

Table 2.5: Values of interface conductance calculated with AMM and DMM theories.

Unfortunately, due to a lack of information in the literature, the dispersion diagram of the BD1, ULK and SiCN materials are not available. Their interface conductances cannot be calculated but their values will be considered to be of the same order as that the values calculated for the other materials (USG, SiN and Silicon). It could be interesting to verify this assumption in the future. The global tip-sample contact conductances are summarized in Table 2.6. In summary, all the contact conductance $G_{contact}$ can be reasonably considered between 60 and 300 nW.K^{-1} for all our samples.

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Material	$G_{contact}$ (nW.K^{-1})	
	Minimum	Maximum
Silicon	83.1	174
BD1	-	-
SiCN	-	-
SiN	60.7	125
ULK	-	-
USG	116	234

Table 2.6: TBC calculated with [8] and with AMM/DMM theories.

II.2.C.d. Probe-sample contact modelling

The probe-sample thermal interaction consists of two contributions: the contact and the ballistic air transfer conductances associated to the tip-sample contact. These two contributions are taken into account and implemented in the FEM model.

Modelling of the contact conductance in FEM

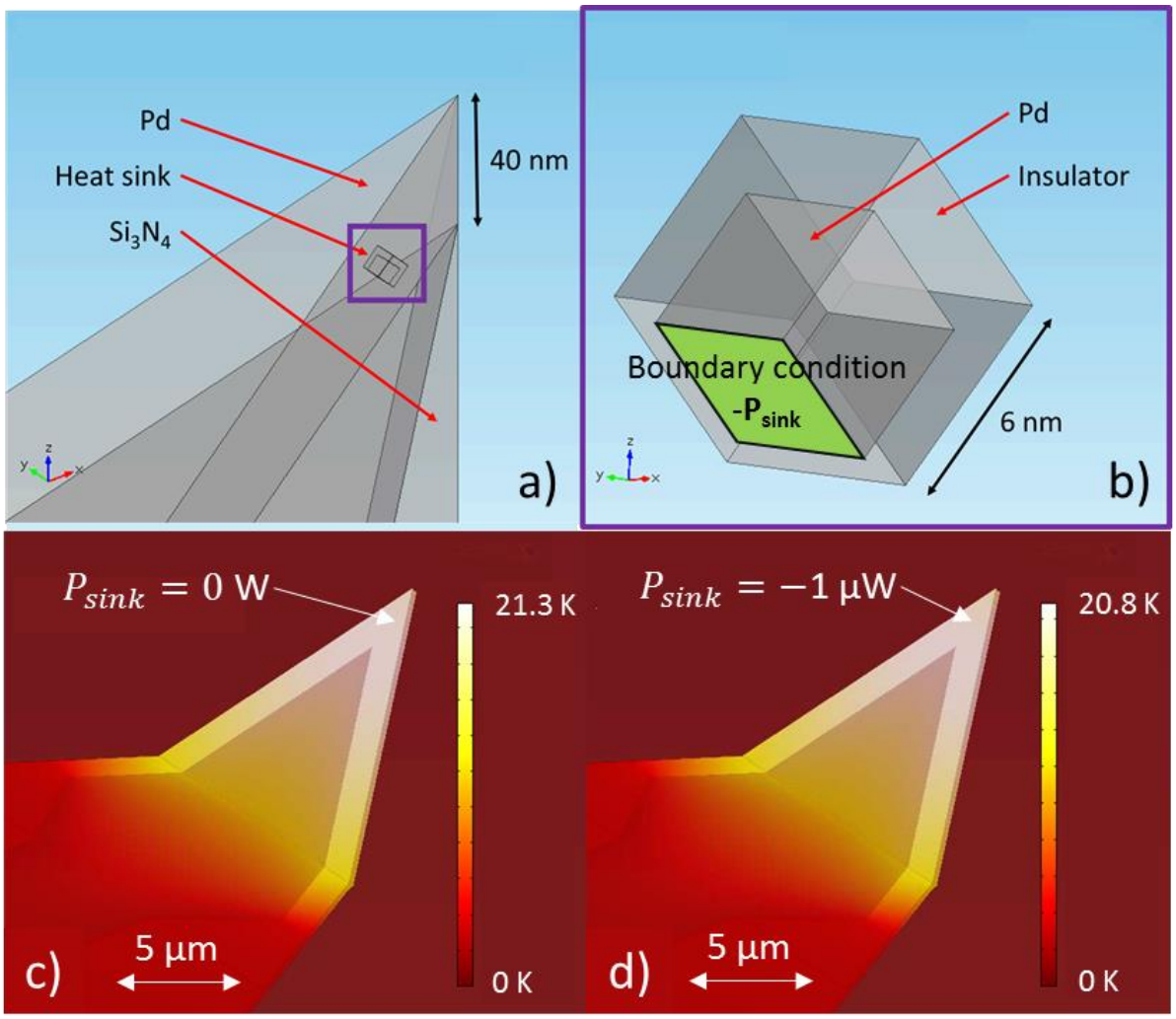

Figure 2.13: a) Geometry of the palladium nano-probe apex. b) Heat sink geometry. c) ΔT_{apex} with P_{sink} equal to 0 W. d) ΔT_{apex} with P_{sink} equal to -1 µW.

$G_{contact}$ is modelled numerically by adding a heat sink at the probe apex as shown in Figure 2.13.a) and Figure 2.13.b). In contact mode, the heat sink allows the generation of a temperature drop at the

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tip apex equivalent to the one which is actually created by the contact conductance between the tip and the sample. The relation is:

$$P_{sink} = -G_{contact} \times \Delta T_{apex}, \tag{2.10}$$

$$\Delta T_{apex} = T_{apex} - T_{surface}, \tag{2.11}$$

where P_{sink} is the power into the sink set as a boundary condition, T_{apex} is the temperature at the probe apex and $T_{surface}$ is the temperature at the sample surface just below the tip. As $G_{contact}$ is characteristic of each surface material, P_{sink} is fitted for each surface material. An ideal insulator ($k_{insulator} = 0$ W.m^{-1}.K^{-1}) is surrounding five faces of the cubic sink to force the flux coming from the probe to be dissipated in the sink, and not that from the sample (see Figure 2.13.b)). Figure 2.13 shows the impact of the sink on the tip temperature field: a variation of 0.5 K is observed for the maximal temperature in this example. It was verified that the sink size does not influence this temperature drop.

Ballistic heat conduction in FEM

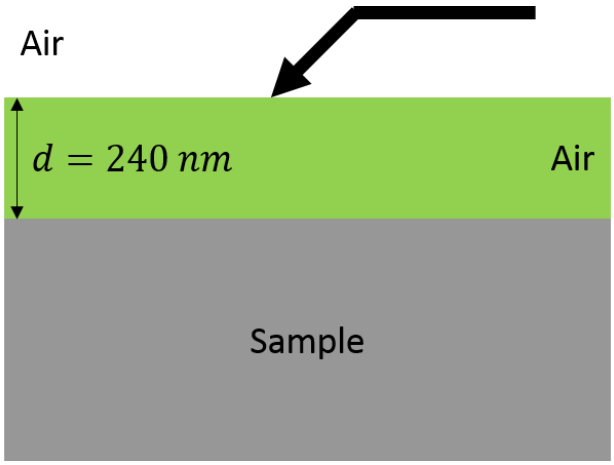

Figure 2.14: Modelling of the thermal ballistic resistance in FEM.

Following Shi and Majumdar [13], ballistic heat conduction takes place for reduced sizes, therefore especially at the tip-sample contact with the palladium probe. A layer of air between the tip and the sample surface can replace the thermal resistance associated to the ballistic limitation of heat transport [12] (see Figure 2.14). The thickness of this layer is calculated with:

$$d = 4\Lambda_{air}, \tag{2.12}$$

where d is the thickness of the air layer and Λ_{air} is the mean free path of air equal to 60 nm [13]. The thickness of the layer of air is equal to 240 nm in ambient air. While this assumption is reasonable for the locally-flat Wollaston probe, it might be questionable for the palladium probe. In [13], the authors had to consider an additional geometrical factor γ to include the fact that the tip and the substrate are not two parallel plates. In the present study with the palladium probe, γ is taken equal to 1 considering the tip apex to be locally-flat like the Wollaston probe. This assumption is evaluated in the thesis of E. Guen with the help of A. Alkurdi.

In summary, the palladium probe has been first characterized with its environment. Then, the tip-sample contact has been evaluated with the contact conductance and the ballistic effect. Finally, all these constraints are implemented in the FEM modelling. Now that all properties and interactions have been quantified, the experimental data can be interpreted in terms of thermal conductivities.

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II.2.D. Results and discussion

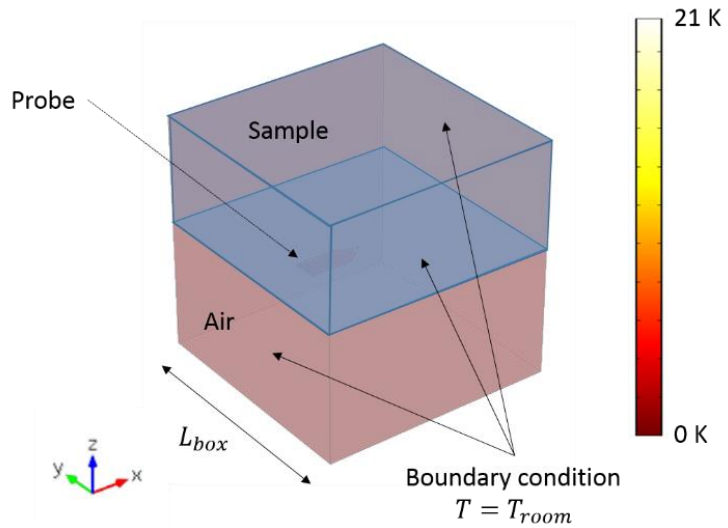

Figure 2.15: Temperature rise of the probe contacting a sample.

Before determining the thermal conductivities of the samples, the sensitivity of the probe needs to be evaluated. The probe is put in contact with the sample numerically to represent the real physical system as shown in Figure 2.15.

II.2.D.a. Sensitivity of thermal signal measurements on bulk sample

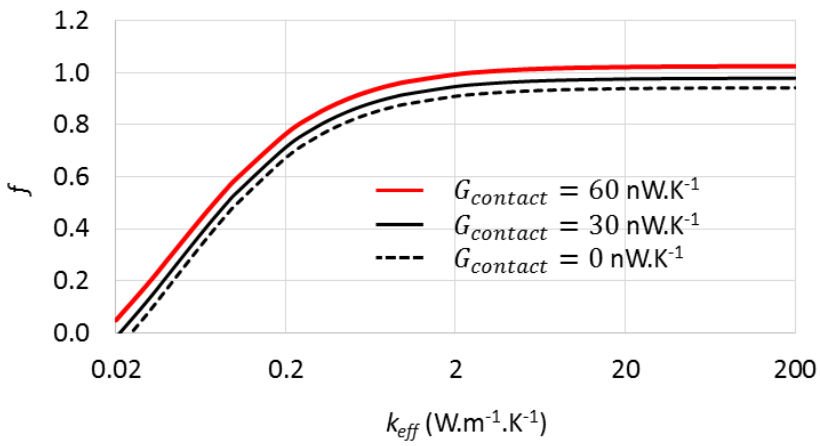

Figure 2.16: Impact of the effective thermal conductivity k_{eff} and the contact conductance $G_{contact}$ on the thermal signal f measured in SThM with the palladium nano-probe.

In this section, the sensitivity of the palladium probe in thermal signal f is investigated. To simplify the study, the probe is set in contact with a simple bulk sample of thickness 750 µm. Figure 2.16 shows the variations of f as a function of contact conductance $G_{contact}$ and sample thermal conductivity k_{eff}. Three different regimes can be observed. The first one takes place where the effective thermal conductivity k_{eff} is lower than 1 W.m^{-1}.K^{-1}. In this region, the variations of f are mainly due to k_{eff}. The second region is defined where k_{eff} is larger than 10 W.m^{-1}.K^{-1} and where the variations of f are mainly due to $G_{contact}$. Finally, the third region, where k_{eff} is between 1 and 10 W.m^{-1}.K^{-1}, is sensitive to both k_{eff} and $G_{contact}$. This study shows that for samples with large effective thermal conductivity, the contact between the probe and the sample can be characterized while the effective thermal conductivity cannot be determined. Conversely, for very low effective thermal conductivity samples,

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the characterization of the contact is not mandatory. Considering the constraints on the accuracy of $G_{contact}$, the values of f measured by SThM on USG and SiN will be analyzed.

II.2.D.b. Determination of the thermal conductivity of thin films

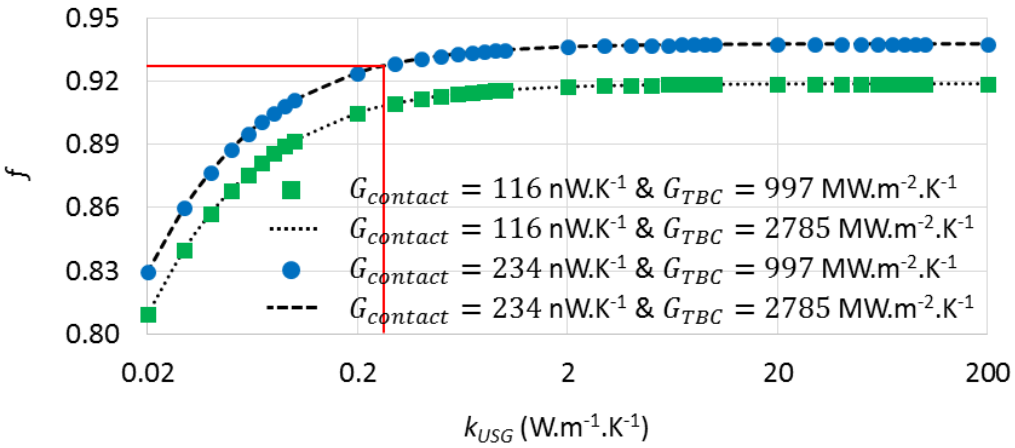

Figure 2.17: Thermal signal f as a function of the contact conductance $G_{contact}$, the TBC G_{TBC} and the thermal conductivity of the USG layer k_{USG} for USG 5400 sample.

For samples with stacked films deposited on bulk silicon, the TBC between the layers are taken into account. Following Cheeke et al. [15] and Swartz and Pohl [16] the TBC of all surfaces are calculated with the AMM and DMM similarly to Section II.2.C.c. For each interface, the value of G_{TBC} is set as a boundary condition on the interface between the layers. The TBC are summarized in Table 2.7.

Interface	G_{TBC} (MW.m^{-2}.K^{-1})	
	AMM	DMM
SiN/Si	1673	631
USG/Si	2785	997

Table 2.7: Values of TBC calculated with AMM and DMM.

Figure 2.17 shows the variation of f as a function of three parameters for the sample USG 5400: the thermal conductivity of the silicon dioxide layer k_{USG}, the contact conductance of the probe on the silicon dioxide $G_{contact}$ and the conductance of the interface USG/Si G_{TBC}. It is shown that the uncertainty on G_{TBC} has no effect because a variation of G_{TBC} from 997 to 2785 MW.m^{-2}.K^{-1} generates only a very small variation of k_{USG} (not observable). The effect of TBC is then neglected at the USG/Si interface in USG 5400. Most importantly, Figure 2.18 shows an important impact of $G_{contact}$ on the value of f. For silicon dioxide, $G_{contact}$ is calculated to be 116 and 234 nW.K^{-1} respectively with AMM and DMM, which are considered to provide lower and upper boundaries. A variation of f equal to 0.0188 is induced by the inaccuracy on $G_{contact}$. With this uncertainty on $G_{contact}$, it is not possible to determine an exact value of the thermal conductivity of the silicon dioxide layer. It is found that k_{USG} is larger than 0.25 W.m^{-1}.K^{-1}, which is expected.

The same study is performed with the SiN 300 sample. The contact conductance $G_{contact}$ of the probe on the SiN surface is calculated to be located between 61 and 124 nW.K^{-1}, which leads to similar conclusion: the contact conductance drives the probe temperature. Furthermore, the uncertainty on the value of G_{TBC} has no effect on the determination of k_{SiN} because a variation of G_{TBC} from 631 to 1673 MW.m^{-2}.K^{-1} do not generate a measurable variation of f. As a consequence, the thermal conductivity of the silicon nitride cannot be determined by the FEM model without knowing the exact value of $G_{contact}$. It is only possible to state that k_{SiN} is larger than 0.3 W.m^{-1}.K^{-1}.

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II.2.D.c. Conclusion on nano-probe SThM technique

The palladium nano-probe characteristics allow us to observe three different regimes. The first one is where the effective thermal conductivity k_{eff} is lower than 1 W.m^{-1}.K^{-1}. In this region, the probe response is sensitive to k_{eff}. The second region is where k_{eff} is larger than 10 W.m^{-1}.K^{-1} and where the probe is sensitive to $G_{contact}$. Finally the third region, where k_{eff} is between 1 and 10 W.m^{-1}.K^{-1}, is that where the probe is sensitive to both k_{eff} and $G_{contact}$. Currently, the palladium probe seems adapted only for the characterization of very low k_{eff} samples.

In order to improve the accuracy of the measurements, the contact has to be characterized in details, or the probe dimensions should be larger to reduce the dependency on the tip-sample thermal conductance at the contact. In the current analysis, the surface roughness of the sample was neglected, because the materials are supposed to be very flat. For other types of materials, roughness could have an impact. It could then be measured by the AFM technique, but a theory including the effect should also be developed in addition. Moreover, for very thin films like USG 5400 or SiN 300, all TBC need to be determined with lower uncertainties to allow for an accurate determination of the thermal conductivities of the thin layers. This should be done by taking into account the electron-phonon coupling in addition to the calculation of the TBC with AMM and DMM theories.

II.3. Characterization with PtRh micro-probe

Based on previous results, another probe will be presented here: the platinum-rhodium (PtRh) micro-probe, also called Wollaston probe. Such a probe is expected to be more relevant for our materials. The experimental data including a comparison with calibration samples will be analyzed. Finally, the performance of the SThM technique with the Wollaston probe will be summarized.

II.3.A. The Wollaston micro-probe

The experiments are now performed with the Wollaston probe, which involves a PtRh ($Pt_{90}Rh_{10}$ alloy) filament at the end of a silver wire. This probe allows measurement with a submicrometric resolution. A SEM image of the probe is shown in Figure 2.18.

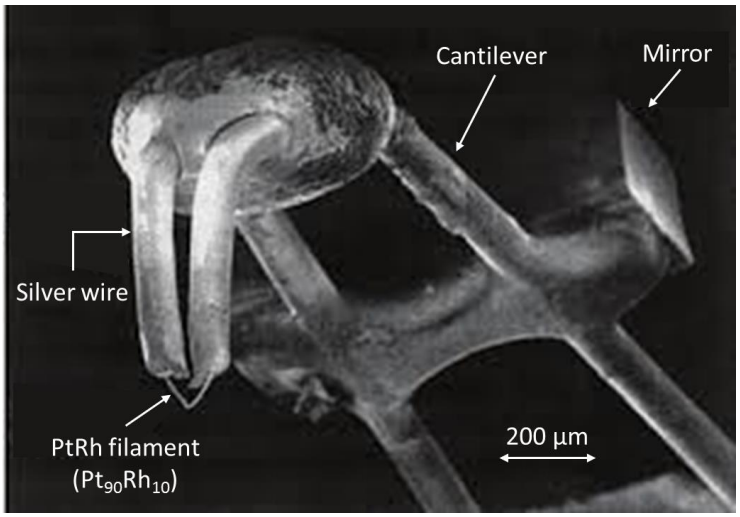

Figure 2.18: SEM image of the Wollaston probe [17].

II.3.B. Experimental measurement

During these measurements, a current equal to 50 mA is supplied into the probe. Considering an electrical resistance of PtRh equal to 2 Ω, the joule power generated in the filament is equal to 5 mW.

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With these experimental conditions, the decrease of electrical resistance ΔR_{sample} of the probe can be easily measured between far-from-contact and contact modes. Figure 2.19 shows the experimental data. The uncertainty on the measurement of the thermal signal is due to that of the measurement of the probe resistance. This electronic noise can be calculated as follows:

$$\Delta f = \frac{2\Delta V}{G_{amplifier} I_{probe}} \left(\frac{1}{\Delta R_{sample}} + \frac{1}{\Delta R_{silicon}} \right), \tag{2.13}$$

where ΔV is the uncertainty on the measurement of the voltage and I_{probe} is the current in the probe. In our study case, ΔV is equal to 1 µV. $\Delta R_{silicon}$ is the decrease of electrical resistance of the probe on a reference sample of bulk silicon. All these measurements of the thermal signal f are characteristic of the sample in contact with the probe. In order to be interpreted, these measurements need to be compared to experimental data performed on calibrated samples. This will allow to determine the effective thermal conductivity of the samples.

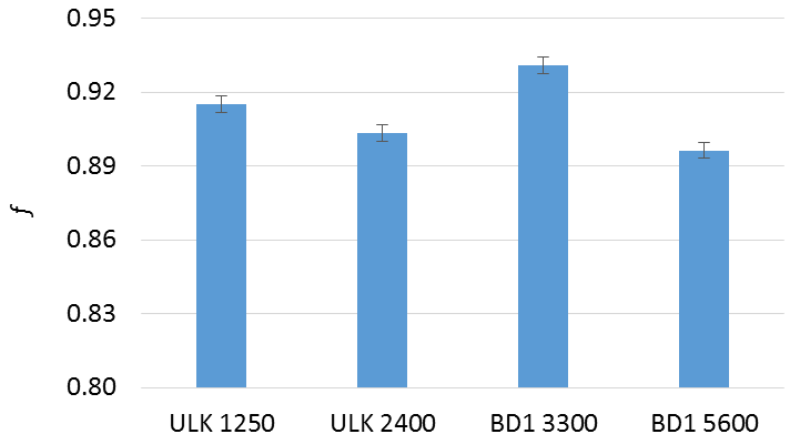

Figure 2.19: Thermal signal as a function of the sample measured with Wollaston probe.

II.3.C. Analysis of the experimental results and numerical reproduction

In this section, the thermal signal measured on ULK and BD1 samples will be compared to reference samples. The effective thermal conductivity of our samples will be deduced and finally, the effective thermal conductivity of the layers of ULK and BD1 will be determined with the help of FEM. The methodology here is different from the one used with the palladium probe (Section II.2.) because the reference samples were not available at that time.

II.3.C.a. Calibration of the Wollaston thermal signal

Sample	k_{eff}	f
PMMA	0.187	0.5162
POM-C	0.329	0.6162
Glass	1.11	0.8434
SiO_2	1.28	0.8390
ZrO_2	1.95	0.9137
TiO_2	9.15	0.9742
Silicon	148	1.0000

Table 2.8: Measurement of the thermal signal with the Wollaston probe on calibration samples.

In order to be interpreted with reliability, the previous measurements done on ULK and BD1 samples are compared to an entire set of reference samples. The reference samples have the same surface

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roughness (out-of-plane RMS < 5 nm) and their thermal conductivities are already characterized. The measurements with the Wollaston probe on the reference samples are used as calibration points. Table 2.8 summarizes the measurements on the reference samples. In order to be used on the entire range of effective thermal conductivities, the calibration points are fitted analytically following E. Guen:

$$f(k_{eff}) = \frac{A}{1+\frac{B}{k_{eff}}} + C. \tag{2.14}$$

A, B and C are found equal to 0.8026, 0.2957 W.m^{-1}.K^{-1} and -0.2011 respectively. Figure 2.20 shows the fit of the calibration points over the whole range of effective thermal conductivities. The standard deviation $\sigma_{calibration}$ between the fitted line and the thermal signal of the reference samples is found equal to 8.77‰.

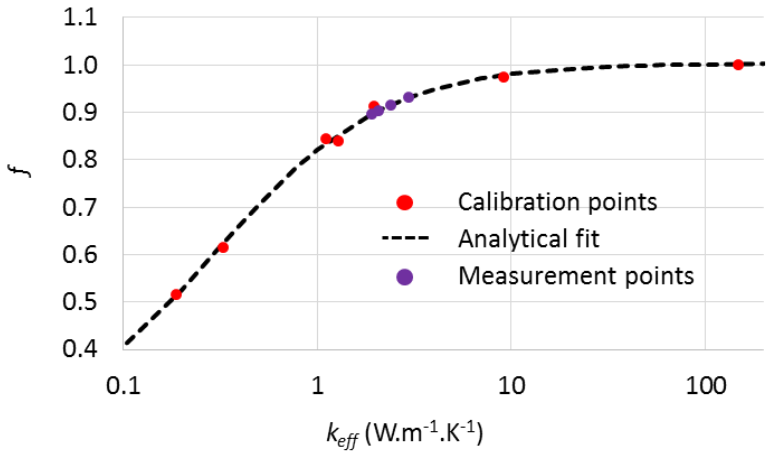

Figure 2.20: Thermal signal as a function of the sample effective thermal conductivity.

II.3.C.b. Determination of sample effective thermal conductivity

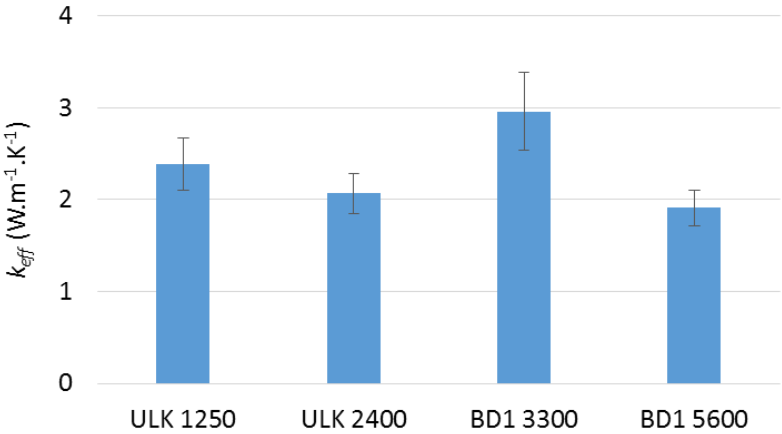

Figure 2.21: Determined equivalent thermal conductivity for ULK and BD1 samples.

The calibration curve allows to determine the effective thermal conductivities of our ULK and BD1 samples, as shown in Figure 2.21. The uncertainty on k_{eff} is noted Δk_{eff}. It is due to the uncertainty of the fitted curve $\sigma_{calibration}$. In this case:

$$\Delta k_{eff} = \frac{\sigma_{calibration}(k_{eff}+B)^2}{A(k_{eff}+B)-Ak_{eff}}. \tag{2.15}$$

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We have now to focus on the numerical modelling of the probe-sample system in order to deduce the effective conductivity of each layer at the sample surface from the effective thermal conductivity of the film/substrate system.

II.3.C.c. Wollaston-sample system modelling by FEM

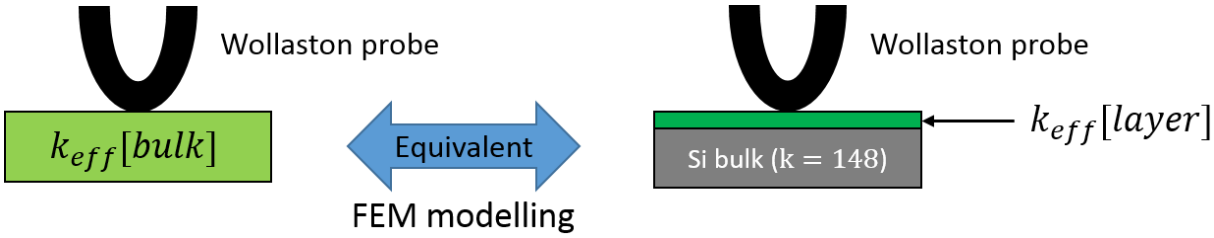

Figure 2.22: Principle of the FEM modelling objective with Wollaston probe

A FEM simulation is used to deduce the k_{eff} of the layer from the equivalent k_{eff} measured with the calibration curve. The principle of the FEM modelling is explain in Figure 2.22. The effective thermal conductivity of the layer is adjusted numerically to fit the temperature rise generated in the PtRh filament for a bulk sample which has the effective thermal conductivity calculated in Figure 2.21. First, the probe is modelled in its thermal environment, then the tip-sample contact is implemented numerically and finally, the contact effect is characterized experimentally. This is detailed in the following.

<u>Modelling of the Wollaston probe environment</u>

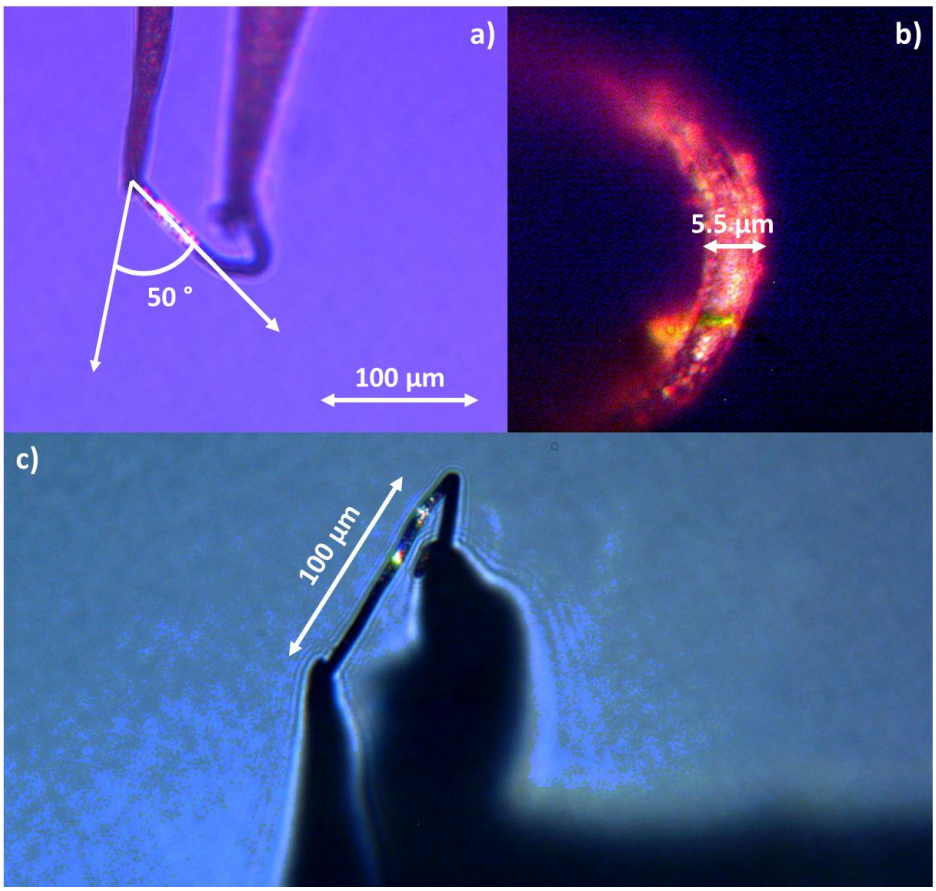

Figure 2.23: Optical microscopy images of the Wollaston probe. a) Measurement of the tilt angle of the filament. b) Measurement of the filament diameter. c) Measurement of the filament length.

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In order to interpret the experimental data f measured with the Wollaston probe, the same method as that with the palladium probe is chosen. An FEM model of the probe-sample system is developed to reproduce the variation of temperature of the probe between far-from-contact and contact modes. The model of the probe has been developed by A. M. Massoud [12] and improved by A. Alkurdi. A characterization of the geometry of the probe is needed to be taken into account in the FEM model. Figure 2.23 shows images of the Wollaston probe. The probe chosen has a platinum wire with a length $L_{filament}$ equal to 200±20 µm, a diameter $D_{filament}$ equal to 5.5±0.5 µm and a tilt angle $\theta_{filament}$ equal to 50±5° (see Figure 2.24). Actually, in the FEM model, the tilt angle is chosen equal to 65° due to 15° of tilt between the sample and the probe holder. Considering the filament, its resistance and the Joule power are calculated as follows:

$$R_{filament} = \frac{4\rho_{pt}L_{filament}}{\pi D_{filament}^2}, \tag{2.16}$$

$$P_{heat} = R_{filament}I_{probe}^2, \tag{2.17}$$

where ρ_{pt} is the resistivity of the platinum equal to 19.3 µΩ.cm at room temperature, $R_{filament}$ is the resistance of the wire and P_{heat} is the power generated by Joule effect.

Finally, like the analysis made on the palladium probe, the losses in the air are estimated. The heat loss coefficient h_{air} is equal to 3000 W.m^{-1}.K^{-1} for the Wollaston probe [19, 20] (see section II.2.C.b.). In order to model the heat loss through air in FEM, the Wollaston probe is set at the center of an air domain of 2000 µm width as shown in Figure 2.24. The conductance to the cantilever $G_{cantilever}$ is fitted with the experimental temperature in air. The applied current is 50 mA. The temperature rise of the wire has to be modelled now at the sample contact.

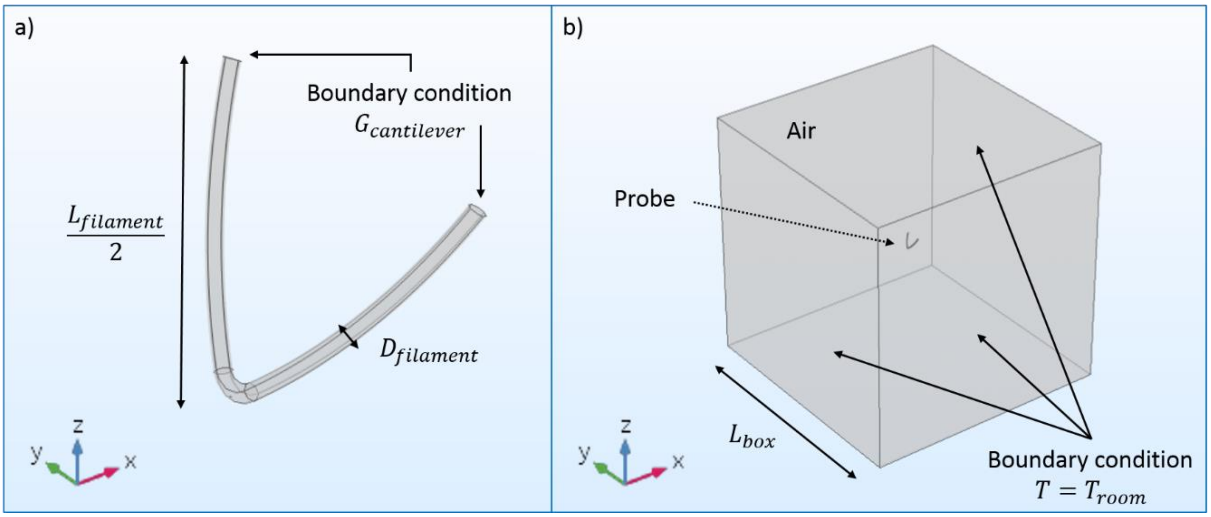

Figure 2.24: a) Modelling of the Wollaston filament with diameter $D_{filament}$ and length $L_{filament}$. b) Convective losses implement in FEM by an air domain L_{box} of 2000 µm width

<u>Modelling of the tip-sample contact</u>

In the simulations, $G_{contact}$ is modelled numerically by a heat sink at the probe apex as shown in Figure 2.25. In contact mode, the heat sink generates a temperature drop at the tip apex equivalent to the one which is actually created by the contact conductance between the tip and the sample. P_{sink} is the power into the sink set as a boundary condition. An ideal insulator ($k_{insulator} = 0$) is surrounding the heat sink to force the flux coming from the probe to be dissipated in the sink, and not that from the sample. This sink needs further calibration.

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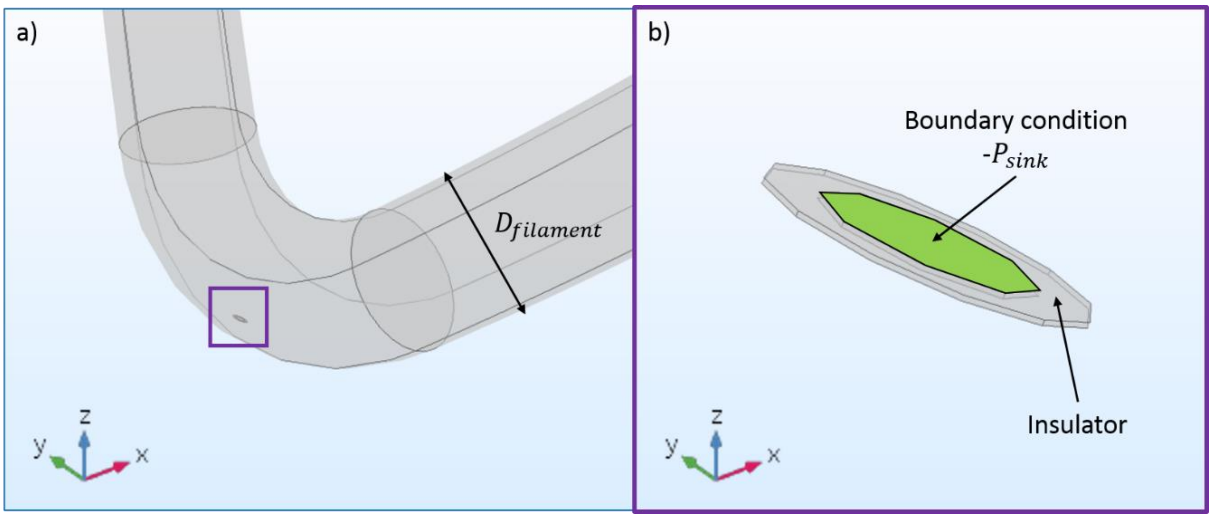

Figure 2.25: Modelling of the contact conductance in FEM. a) Shape of the platinum filament. b) Shape of the heat sink at the probe apex surrounded by thermal insulator

<u>Calibration of the contact heat path effect</u>

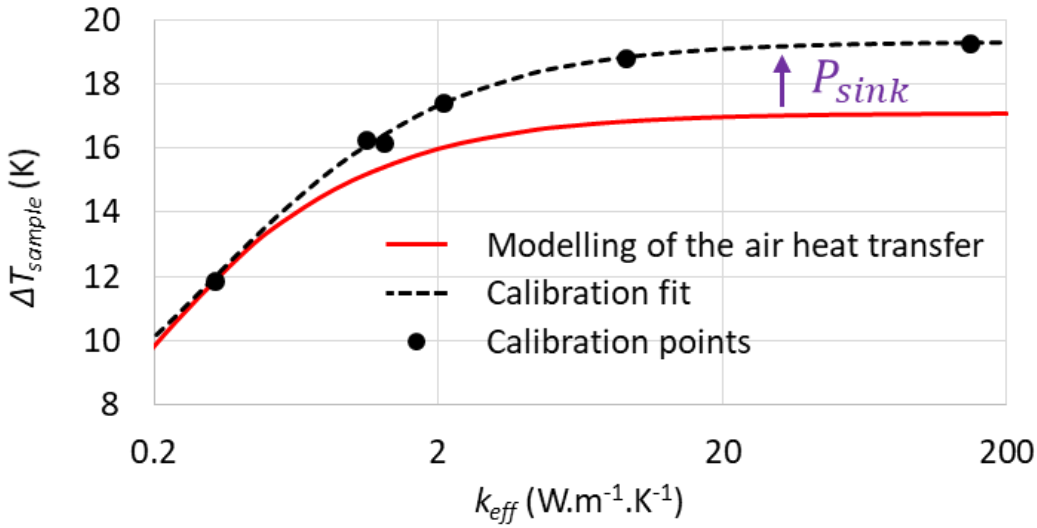

Figure 2.26: Comparison of the temperature rise between calibration curve and numerical modelling without the tip-sample contact effect in terms of k_{eff} [12].

Figure 2.26 shows the variation of temperature $\Delta T_{sample} = T_{air} - T_{sample}$ calculated numerically without taking into account the contact effect (red line). Only the air heat transfer is calculated with $P_{sink} = 0$. In addition, the temperature rise measured experimentally with the calibration samples is shown and fitted (black dashed line).

The power of the heat sink P_{sink} is fitted at each effective thermal conductivity to match the numerical elevation of temperature with the experimental curve. Figure 2.27 shows the fit of P_{sink} which is only needed between 1 and 4 W.m^{-1}.K^{-1} because it is the range of equivalent thermal conductivities for our ULK and BD1 samples (as can be reminded from Figure 2.21). The probe and its interactions with the environment and the sample are fully described. The effective properties of each layer is now to be determined as a function of the experimental measurements.

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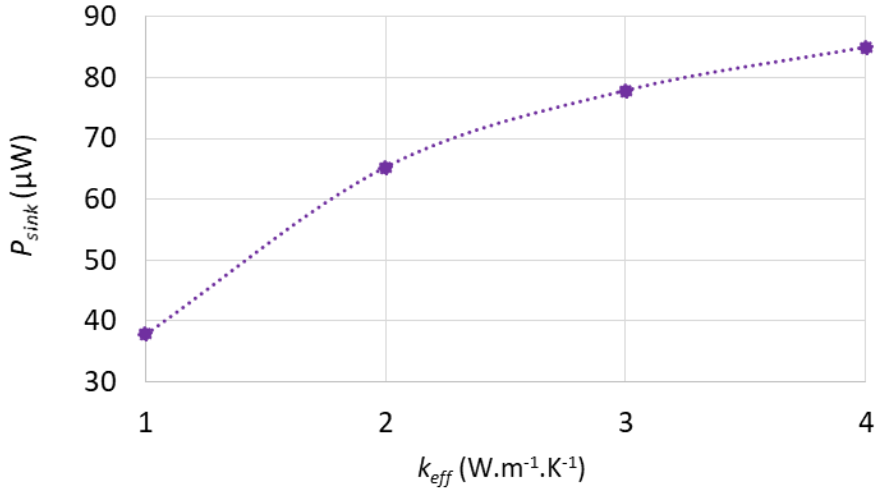

Figure 2.27: Power P_{sink} representing the tip-sample contact conductance for effective thermal conductivities k_{eff} between 1 and 4 W.m^{-1}.K^{-1}.

II.3.D. Results and discussion

In this section, the effective thermal conductivity of the top thin films of ULK and BD1 samples are to be deduced. Finally, a conclusion will be drawn on the capabilities of the SThM technique with the Wollaston probe.

II.3.D.a. Determination of the thermal conductivities of the thin films

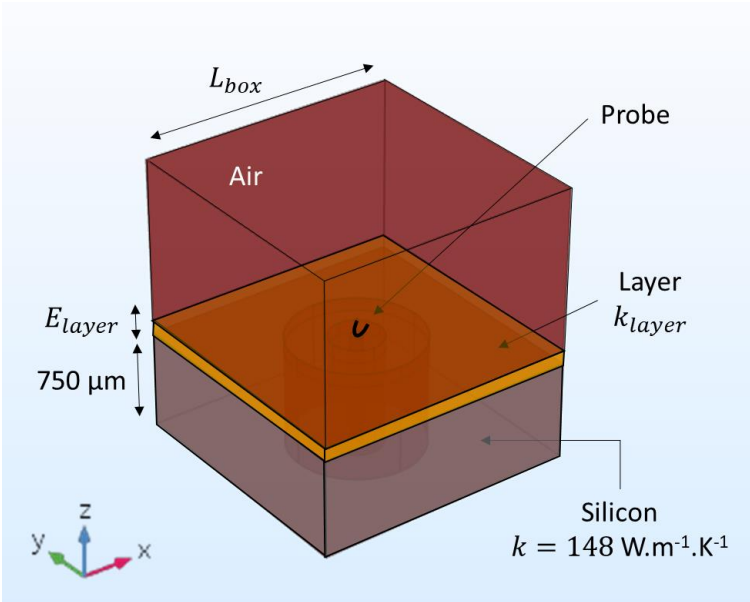

Figure 2.28: FEM modelling of the Wollaston probe in contact with a layer-on-substrate sample.

In order to interpret the thermal signal f measured experimentally as a function of the effective thermal conductivity of the layer, the probe is set in contact with the real sample in the FEM modelling [21]. Figure 2.28 shows the elevation of temperature modelled with the additional surface layer. The model of the Wollaston probe developed by A. Assy and A. Alkurdi has been broadened for the layers. One or two additional layers can be added at the bulk surface.

For each sample, the values of effective thermal conductivities are fitted. The results are shown in Figure 2.29. In addition, the heat transport in the film can be considered as 1D. Indeed, an equal

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temperature rise is reached with a boundary layer at the bulk surface with the boundary resistance calculated as follows:

$$R_{th} = \frac{E_{layer}}{k_{layer}}, \tag{2.18}$$

where E_{layer} and k_{layer} are respectively the thickness and the effective thermal conductivity of the layer on top of the silicon substrate.

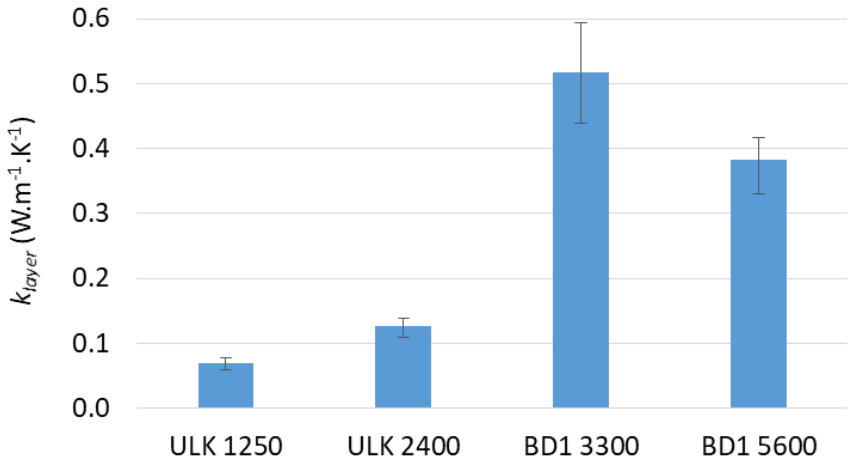

Figure 2.29: SThM measurements of the effective thermal conductivity for ULK and BD1 samples

II.3.D.b. Conclusion on Wollaston probe SThM technique

To conclude, the effective thermal conductivities of ULK and BD1 samples have been measured with SThM technique with the Wollaston probe. First, the experimental setup needs calibration. To do so, an entire set of calibration samples are needed. Second, the equivalent thermal conductivity of each sample is calculated analytically. Finally, the property of each surface layer is fitted with the FEM model from the experimental data.

In SThM with Wollaston probe, the accuracy of the measurement is limited by the precision of the fit of the reference sample. In order to improve the calibration curve, two methods could be used:

(i) calibrate the experimental setup with more reference samples in the range of interest;

(ii) use calibration samples of same surface material and roughness to avoid their influence on the thermal signal is even better [22].

II.4. Conclusion on SThM technique

	Palladium nano-probe	**Wollaston micro-probe**
Model calibration	✓ Contact calibration with AMM/DMM theories J. D. N. Cheeke [16]	✓ Contact calibration with reference samples A. M. Massoud [13]
Spatial resolution	✓✓ Submicrometric	✓ Micrometric
Sample Characterization	✕ Bulk materials with $k_{eff} \ll 1$ W.m^{-1}.K^{-1}	✓ Bulk & thin films with $k_{eff} \ll 1$ W.m^{-1}.K^{-1}

Table 2.9: Comparison between palladium nano-probe and Wollaston capabilities.

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Table 2.9 summarizes the advantages and drawbacks of the SThM technique with both palladium nano-probe and Wollaston micro-probe. Measurement are to be done later with the 3ω method to estimate the accuracy of the SThM technique.

III. Thermal characterization with the 3ω method

The 3ω method, designed for the measurement of the thermal conductivity of bulk materials and thin films, is also a thermoresistive technique. In this section, the principle of the 3ω method will be explained and the experimental results will be described.

III.1. Principle of the 3ω method

In this section, the principle of the 3ω method is explained. First, the mechanism of heating for the 3ω setup will be described analytically. Then, the interpretation of heat temperature elevation will be presented.

III.1.A. Signal and heater temperature elevation

The 3ω method is a four-probe electrothermal method designed to measure the thermal conductivity of bulk materials and thin films [23-27]. The resistance of the metallic line is

$$R = R_0(1 + \alpha\Delta T), \tag{2.19}$$

where R_0 is the heater resistance and α is the TCR of the resistance in K^{-1}. Figure 2.30 shows a schematics of the 3ω method. b is the half-width of the wire. An AC current of frequency f is injected though the 3ω setup between the I^+ and I^- branches. This AC current is

$$I(t) = I_0\cos(\omega t), \tag{2.20}$$

where ω is the angular frequency $\omega = 2\pi f$ and I_0 is the amplitude of the current passing into the metallic line. The metallic wire generates heat due to Joule effect. This power is

$$P(t) = RI^2(t). \tag{2.21}$$

The power P can be written as follows:

$$P = \frac{1}{2}I_0^2R_0\big(1 + \cos(2\omega t)\big). \tag{2.22}$$

The power generated by the heater has two components: the AC component P_{AC} that depends on 2ω and the constant component P_{DC} which is independent of frequency.

$$\begin{cases} P_{AC}(t) = \dfrac{1}{2}I_0^2R_0\cos(2\omega t) \\ P_{DC} = \dfrac{1}{2}I_0^2R_0 \end{cases}. \tag{2.23}$$

Because of the linearity between the temperature rise of the heater and its resistance, the temperature of the sample can be divided in two components: the DC component which does not depend on the frequency and the AC component which depends on 2ω. The elevation of temperature of the wire can be expressed as

$$\Delta T(t) = \theta_{DC} + |\theta_{2\omega}|cos(2\omega t + \varphi_{2\omega}), \tag{2.24}$$

where $\varphi_{2\omega}$ is a phase due to the lag between the temperature and the flux, $|\theta_{2\omega}|$ is the amplitude of the temperature rise generated by the AC power P_{AC} and θ_{DC} is the amplitude of the temperature rise

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generated by the DC power P_{DC}. Considering Eq. (2.19) and Eq. (2.24), the resistance of the metallic line is

$$R(t) = R_0 + R_0\alpha\theta_{DC} + R_0\alpha|\theta_{2\omega}|cos(2\omega t + \varphi_{2\omega}), \tag{2.25}$$

As a consequence, the resistance of the heater is modulated at 2ω. Considering Ohm's law, the voltage drop measured between V^- and V^+ branches results from the multiplication of the heater resistance (Eq. (2.25)) by the input current (Eq. (2.20)). The voltage is then:

$$V(t) = R_0 I_0 \left[(1 + \alpha\theta_{DC})cos(\omega t) + \frac{\alpha|\theta_{2\omega}|cos(\omega t - \varphi_{2\omega})}{2} + \frac{\alpha|\theta_{2\omega}|cos(3\omega t + \varphi_{2\omega})}{2}\right], \tag{2.26}$$

In the above expression, the voltage at 1ω is based on the DC resistance of the heater and the components θ_{DC} and $\theta_{2\omega}$. Measuring the voltage signal at 3ω is challenging because it is smaller by three order of magnitude of the first voltage signal 1ω due to the low value of α ($\approx 10^{-3}$ K^{-1}). However, the 3ω voltage is directly proportional to the temperature oscillation at 2ω. The voltage $V_{3\omega}$ of the wire is measured with a lock-in amplifier (LIA) set-up, which can also be used as bridge to remove a large $V_{1\omega}$ before measuring the third harmonic voltage. Consequently, the third harmonic component leads us to the values of $\theta_{2\omega}$ and $\varphi_{2\omega}$ as

$$V_{3\omega} = \frac{1}{2}\alpha R_0 I_0 cos(3\omega t + \varphi_{2\omega}), \tag{2.27}$$

$$|V_{3\omega}| = \frac{1}{2}V_0\alpha|\theta_{2\omega}| \quad \text{and} \quad arg(V_{3\omega}) = \varphi_{2\omega}, \tag{2.28}$$

where $V_0 = R_0 I_0$ is close to the amplitude of the voltage in the metallic wire at 1ω. Both the third harmonic voltage $V_{3\omega}$ and $\theta_{2\omega}$ have an in-phase (real) and out-of-phase (imaginary) parts. The temperature amplitude of the heater can then be measured as:

$$|\theta_{2\omega}| = \frac{2|V_{3\omega}|}{\alpha R_0 I_0} \approx \frac{2|V_{3\omega}|}{\alpha|V_{1\omega}|}. \tag{2.29}$$

The measurement of the $V_{3\omega}$ voltage allows us to calculate the elevation of temperature $\theta_{2\omega}$. We can now focus on the interpretation of the temperature rise of the wire $\theta_{2\omega}$ as a function of the properties of the sample below the heater.

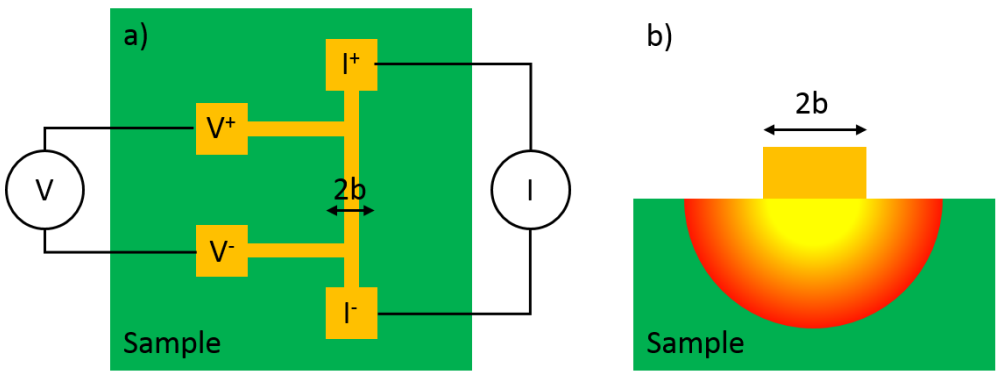

Figure 2.30: Principle of the 3ω method. a) Top view of the four-probe electronic setup. b) Cross section of the heater which is the metallic line.

III.1.B. Interpretation of heater temperature elevation

The heater temperature rise is due to thermal resistance to the heat flux in the sample. The influence of the substrate and the surface layer will be estimated in the following.

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III.1.B.a. Thermal conductivity of the substrate

In order to relate the elevation of temperature $\theta_{2\omega}$ with the thermal properties of the sample, the system is reduced to a 2D problem. To do so the following condition needs to be set [28, 29]:

$$L \geq 200b, \tag{2.30}$$

where L is the length of the heater (between branches V^- and V^+, see Figure 2.30.a)). Then, following Borca-Tasciuc et al. [24], the temperature rise $\theta_{2\omega}$ is for bulk samples:

$$\theta_{2\omega} = -\frac{P_0}{2\pi Lk}\left[ln(2\omega) + \frac{1}{2}ln\left(\frac{b^2}{D}\right) - 2\xi\right] - i\frac{P_0}{4Lk}, \tag{2.31}$$

where $P_0 = R_0 I_0^2$, D is the diffusivity of the substrate (equal to 88 µm².s^{-1} for silicon [29]), ξ is a constant equal to 0.923 [31, 32] and k is the thermal conductivity of the substrate. In this case, the real part of the temperature oscillation decays logarithmically with respect to the excitation frequency 2ω and the imaginary part is constant. The thermal conductivity of the substrate can therefore be determined from both real and imaginary part. Experimentally, it is more reliable to consider the real part of the measured data [23]. To do so, Eq. (2.31) can be written in terms of measurable quantities:

$$V_{3\omega} = -\frac{V_0^3\alpha}{4\pi LkR_0}\left[ln(2\omega) + \frac{1}{2}ln\left(\frac{b^2}{D}\right) - 2\xi\right] - i\frac{V_0^3\alpha}{8\pi LkR_0}. \tag{2.32}$$

The linear relation between the third harmonic voltage and the logarithm of the excitation frequency 2ω allows to calculate the slope, which is

$$slope = \frac{d(R(V_{3\omega}))}{d(ln(2\omega))} = \frac{V_0^3\alpha}{4\pi LkR_0}. \tag{2.33}$$

The thermal conductivity of the substrate k can therefore be calculated with the equation:

$$k = \frac{V_0^3\alpha}{4\pi LR_0 slope}. \tag{2.34}$$

The measurement of the slope of the real part of the $V_{3\omega}$ as a function of the logarithm of the excitation frequency allows to determine the thermal conductivity of the substrate. We can now focus on the determination of the thermal conductivity of the layer at the sample surface.

III.1.B.b. Thermal conductivity of the surface layer

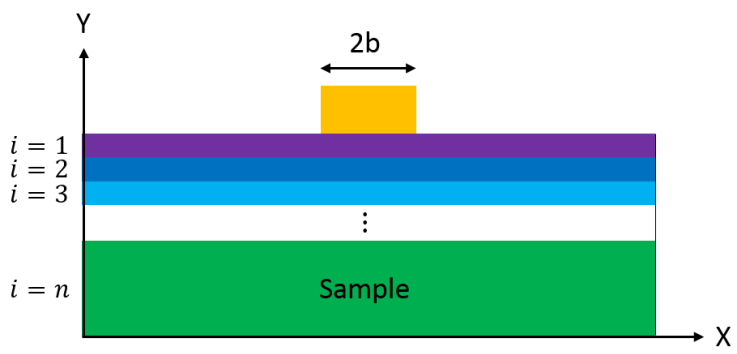

Figure 2.31: Cross section of the 3ω device on a real multilayer sample.

In the previous part, the 2ω harmonic temperature rise of a heater deposited on an infinite isotropic substrate has been determined. Now, a real multilayer system is considered. Its temperature oscillation has to be determined. Figure 2.31 shows the real system and its geometry. A general solution using integral Fourier transform [33, 34] has been developed by Borca-Tasciuc et al. to

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describe the 2D heat conduction across a multilayer system. In this model, the derivation is based on a two-dimensional heat conduction model across the system and a uniform heat flux boundary condition between the heater and the top film [23]. The temperature rise of the heater is then:

$$\Delta T = \Delta T_S + \Delta T_F, \tag{2.35}$$

where ΔT_S and ΔT_F are the temperature rises due to the substrate and the thin film respectively [30]. This assumption is reasonable when the penetration depth of the thermal wave is larger than the thickness of the thin film. Considering a thin film of thickness E_F and effective thermal conductivity k_F, the temperature rise ΔT_F can be associated to a thermal resistance R_F as:

$$R_F = \frac{E_F}{2bLk_F} \quad \text{and} \quad \Delta T_F = \frac{P_0}{R_F} = \frac{P_0}{2bL}\frac{E_F}{k_F}, \tag{2.36}$$

Figure 2.32 shows the comparison between the temperature rise calculated for a bulk substrate sample and a monolayer sample of low thickness with the 3ω method. In the Figure 2.32, the injected power P_0 is equal to 200 mW, the half-width b of the wire is equal to 5 µm and its length L is equal to 1.33 mm. In addition, the top layer has been chosen arbitrary with a thermal conductivity k_F equal to 1.5 W.m^{-1}.K^{-1} and a thickness E_F equal to 10 nm. For each sample in this work, the temperature rise $\theta_{2\omega}$ is measured by means of the 3ω method. First, the slope of the curve allows to determine the thermal conductivity of the substrate. Then, the variation of temperature ΔT_F allows to determine the effective thermal conductivity of the thin film. The electronic test bench which allows the acquisition of the experimental data will be detailed in the next section.

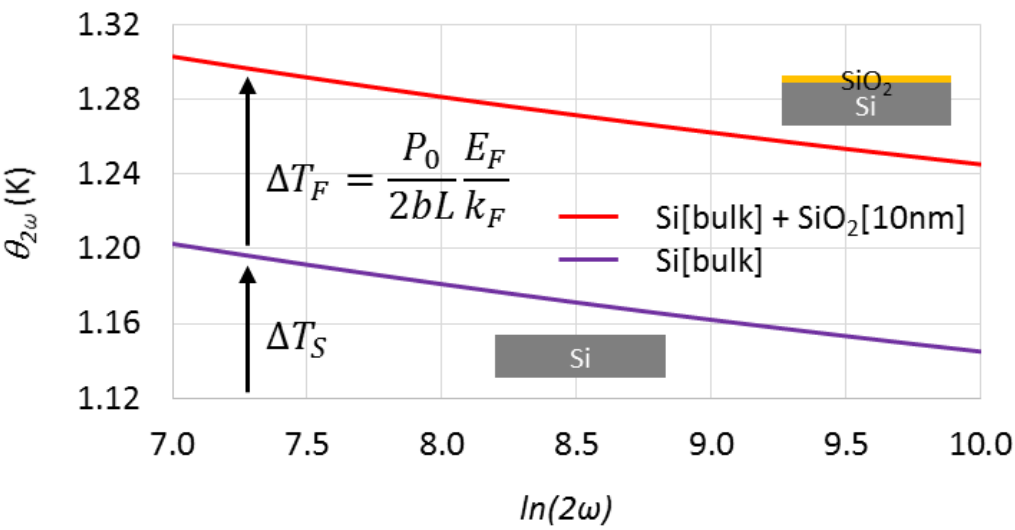

Figure 2.32: Influence of the surface layer on a bulk silicon sample on the temperature rise calculated following Borca-Tasciuc et al. [24].

III.2. Characterization of the 3ω setup

The 3ω method requires to fabricate the metallic devices on top of our samples. In this section, the device and the electronic circuit used for the measurement are implemented.

III.2.A. Fabrication and characterization of the 3ω heater

In order to perform accurate measurements in 3ω method, every single device has to be fully characterized. To do so, first, the fabrication process of the heater will be explained. Then, the geometry of the heater will be characterized. Finally, its TCR will be measured.

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III.2.A.a. Fabrication process by photolithography

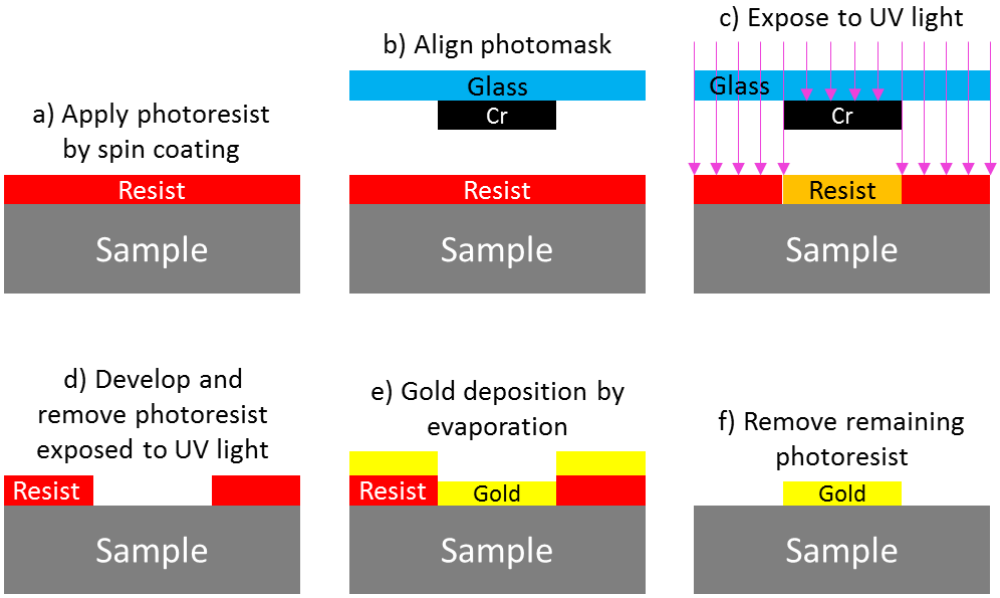

Figure 2.33: Fabrication steps for the deposition of the 3ω device in clean room.

To fabricate our four-probe structures, the photolithography process is chosen. It is a process used in microfabrication to pattern parts of a thin film or the bulk of a substrate. A single iteration of photolithography combines several steps in sequence. Figure 2.33 shows lithography steps. The photolithography process is realized in clean room to avoid contaminations on the surface of the materials. In this study, one 3ω device is deposited on each sample available. In our case, a negative photoresist is used. The illuminated zone of the resist is removed before the deposition of gold by evaporation as shown in Figure 2.33.

III.2.A.b. Characterization of the heater geometry

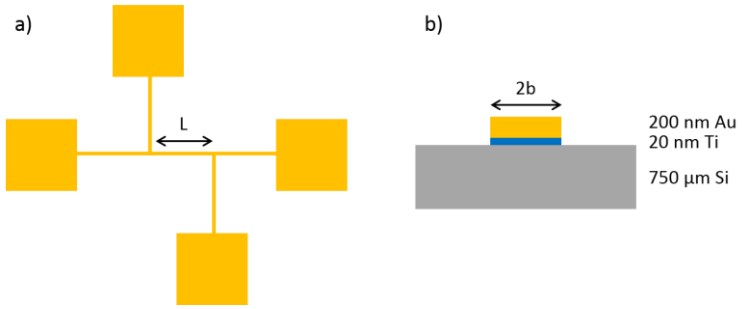

Figure 2.34: Geometry of the heater for 3ω measurements.
a) Top view of the heater geometry. b) Cross section of the metallic line.

In photolithography, the pattern realized on the sample surface is determined by the pattern of the chromium mask (see Figure 2.33.b)). In our case, a mask already used by W. Jaber in his PhD Thesis [28, 29] has been reused. Figure 2.34 shows the geometry of the heater. In the case of the deposition of gold on top of a substrate, a buffer layer of titanium is added at the gold/sample interface. This 20 nm thick layer of titanium promotes the adhesion of the gold on the sample surface.

The thermal conductivity of the substrate k and the layer k_F are calculated with Eq. (2.34) and Eq. (2.36). We can see that both k and k_F are depending on the length and the half-width of the heater

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L and b respectively. It is therefore mandatory to measure the dimensions of the heater every time to keep a good accuracy on the determination of k and k_F. In this study:

$$L = 1330 \pm \Delta L \quad \text{and} \quad b = 5.5 \pm \Delta b, \tag{2.37}$$

where ΔL and Δb are the uncertainties on the measurement in optical microscopy of the wire length an half-width respectively. The uncertainties can be estimated and are equal to 10 µm and 0.1 µm for ΔL and Δb respectively.

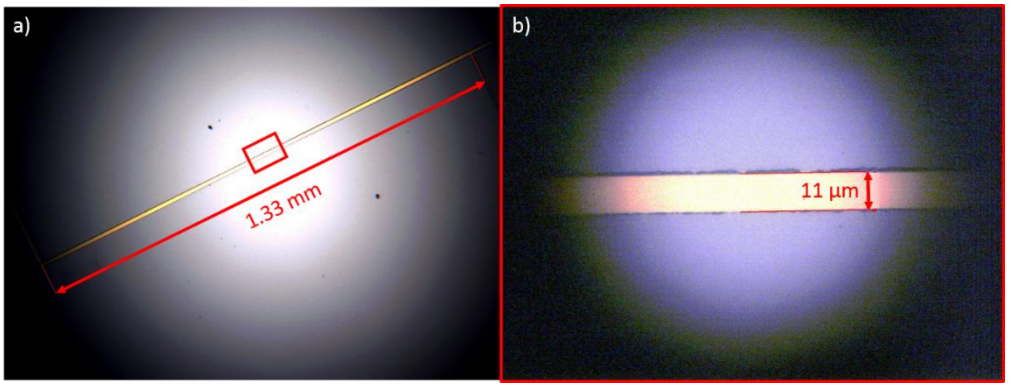

Figure 2.35: Optical microscope images of the 3ω heater. a) Measurement of the length L of the heater equal to 1.33 mm. b) Measurement of the width $2b$ of the wire equal to 11 µm

Figure 2.35 shows optical microscopy images of the metallic line. The sides of the wire are not perfectly flat. This could be due to the use of a single layer of resist which does not have an undercut profile. In our case, we decided to not repeat the fabrication process due to time constraints.

III.2.A.c. Measurement of the heater thermal coefficient of resistance

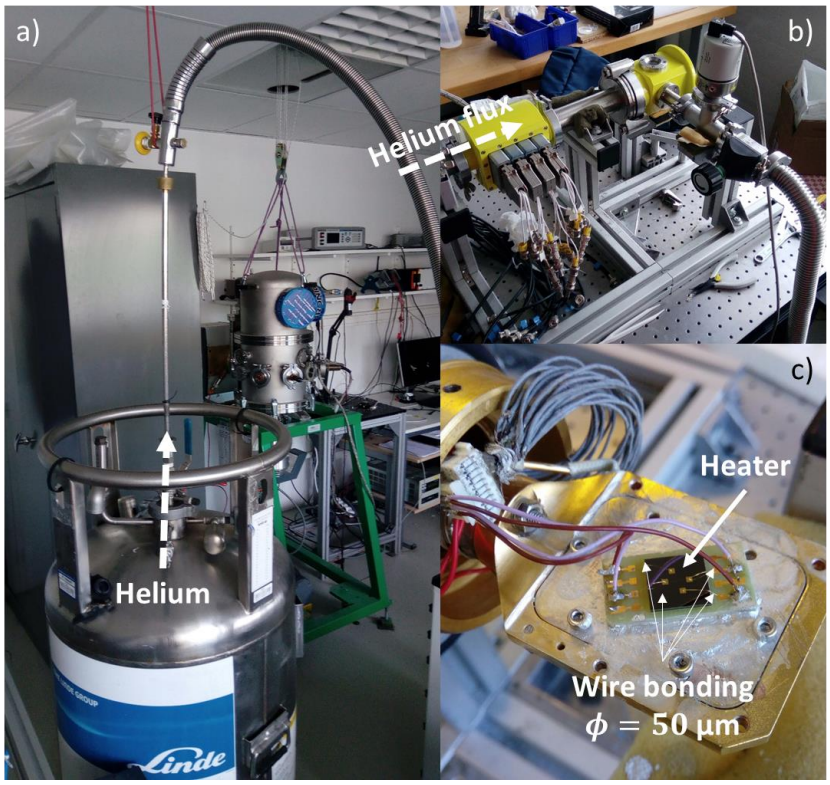

Figure 2.36: 3ω setup with a) helium Dewar to allow low temperature measurements, b) cryostat for measurements under vacuum and c) sample holder with wire bonding connections

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The geometric parameters L and b have been measured using optical microscopy. A parameter is still to be determined: the TCR α of the heater. In order to measure the TCR of the wire, the 3ω setup has been set into a cryostat as shown in Figure 2.36. The cryostat is filled with liquid helium. It allows to reach low temperatures and measure the resistance of the heater between 150 K and 300 K. Note that helium was chosen for practical purposes in this work, but is not all required for those moderate temperatures. In addition, the measurements are done under secondary vacuum to force the heat flux to cross the sample ($P \leq 10^{-4}$ mbar). Figure 2.36.c) shows also that the 3ω device is connected to the electronic circuit with wire bonding.

Gold wire bonding with a diameter of 50 µm is chosen here. The bonding was performed at CIME Nanotech by I. Feng. The measurements of TCR are done only on SiCN 350, SiCN 600 and SiN 300 samples due to very long times of thermalization of the heater, the substrate and the holder. The results are provided in Figure 2.37.

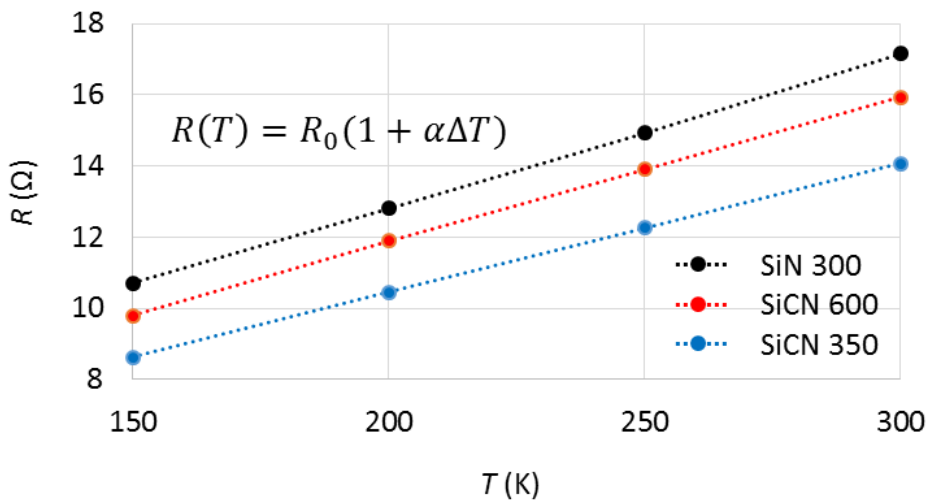

Figure 2.37: Electrical resistance for SiCN 350, SiCN 600 and SiN 300 samples as a function of the temperature inside the cryostat.

Considering these measurements, for each sample, the resistance R_0 extrapolated at $T = 300$ K and the TCR α are determined. The values are summarized in the Table 2.10. We find that the TCR α is

$$\alpha = 2.58 \times 10^{-3} \pm \Delta\alpha, \tag{2.38}$$

where $\Delta\alpha$ is the uncertainty on the measurement of the wire TCR. Here, the uncertainty can be estimated to be equal to 1.36% approximately.

	$R_0\alpha$ (10^{-2} Ω.K^{-1})	R_0 (Ω)	α (10^{-3} K^{-1})
SiCN 350	3.62	13.89	2.61
SiCN 600	4.09	15.74	2.60
SiN 300	4.30	16.90	2.54

Table 2.10: TCR α and resistance R_0 for SiCN 350, SiCN 600 and SiN 300 samples.

III.2.B. Presentation of the electronic circuit for 3ω method

An electronic circuit is implemented in order to acquire the voltage $V_{3\omega}$ and therefore the temperature oscillations $\theta_{2\omega}$. All the measurements are done under controlled environment. The pressure is maintained below 10^{-4} mbar by a turbo pump and the temperature inside the cryostat is set to 300 K. The electronic circuit is presented in Figure 2.38. The electrical signals $V_{3\omega}$ and V_0 are measured by lock-in amplifiers (7265 DSP) on the heater pads. Likewise, the same parameters $V_{3\omega}^{test}$ and V_0^{test} are

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measured on a reference resistance R_{test}. $V_{3\omega}^{test}$ being indeed a few orders of magnitude lower than $V_{3\omega}$, the temperature rise measured in the circuit is corresponding only to the temperature rise of the metallic line of the heater.

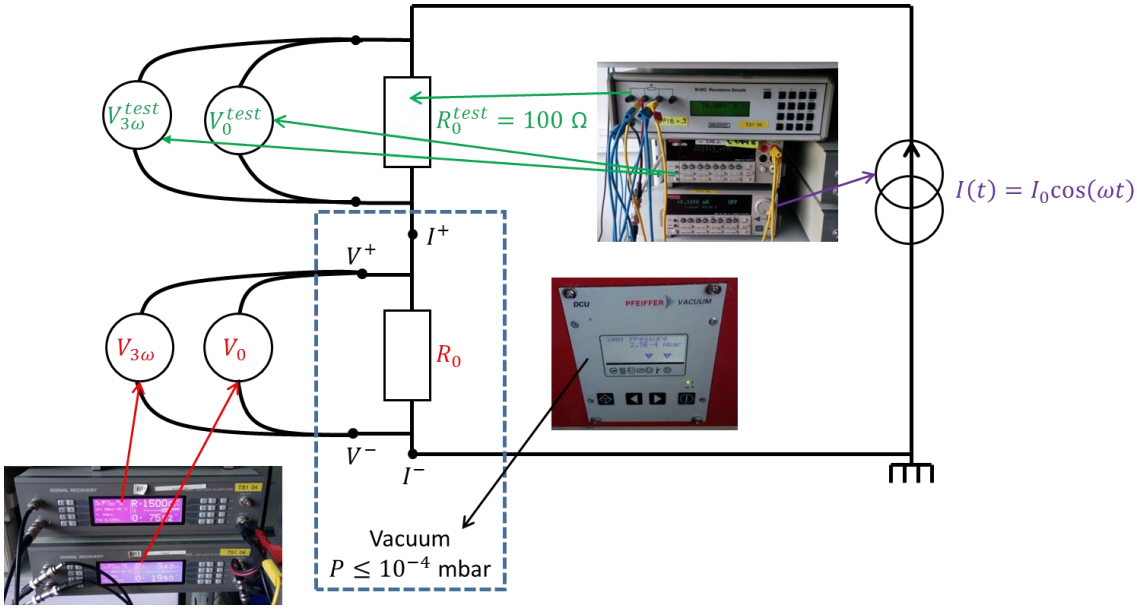

Figure 2.38: Schematics of the electronic circuit for the measurement of the heater temperature oscillations $\theta_{2\omega}$ in the 3ω method.

III.3. Sample characterization with the 3ω method

In this section, the measurements realized on our samples are detailed. Then, these measurements are interpreted in terms of the thermal conductivities of the substrate and the layer. Finally, the results are discussed.

III.3.A. Frequency-domain measurements of the temperature oscillation

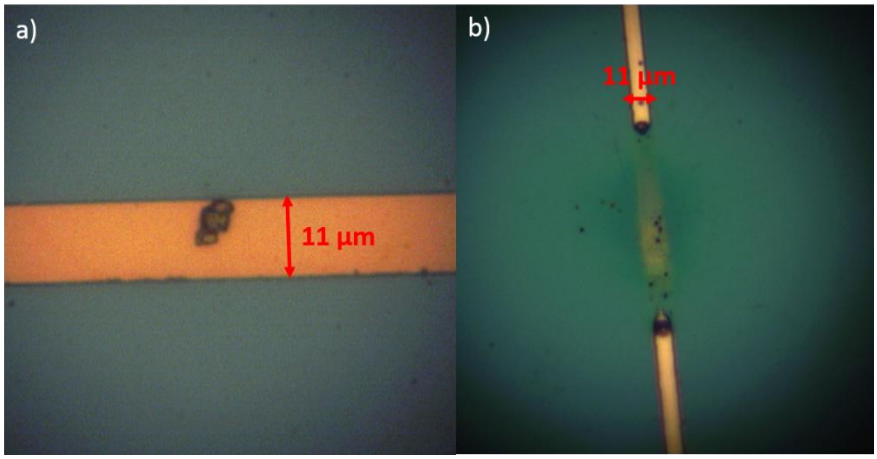

Figure 2.39: Optical microscopy image of a 3ω heater with fabrication process problems. a) Inhomogeneity of metal density. b) Break of the metallic line.

We did not manage to obtain useable 3ω heater device for silicon bulk, SOI, BD1 and ULK samples due to fabrication issues. The fabrication was not repeated due to time constraints. Figure 2.39 shows typical problems of fabrication that prevent using the 3ω device. Note that solutions are known to avoid such issues and this is not an intrinsic limitation of the method.

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For the remaining samples (SiCN, SiN and USG), the measurement results can be found in Figure 2.40. Here the temperature rises $\theta_{2\omega}$ are normalized by the injected Joule power. The dashed line represents the modelling of the temperature rise $\theta_{2\omega}/P_0$ for an ideal silicon substrate without surface layer. It is calculated following Borca-Tasciuc et al. [24] for a heater of 1.33 mm length and 11 µm width.

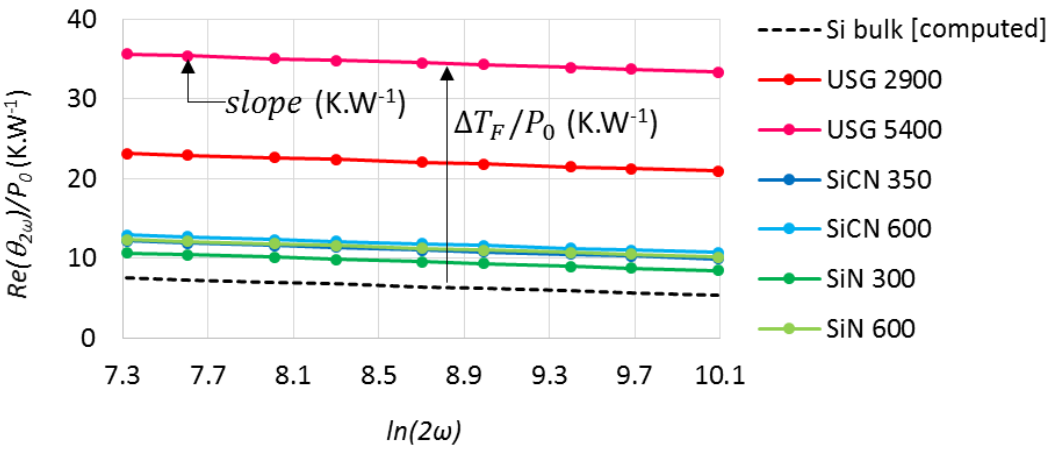

Figure 2.40: Temperature rise $\theta_{2\omega}/P_0$ measured by the 3ω method for USG, SiCN and SiN samples.

III.3.B. Thermal conductivities determination

In this section, we will determine first the thermal conductivity of the substrate for each sample. Then, the effective thermal conductivity of each layer will be deduced.

III.3.B.a. Substrate thermal conductivities

	slope **(K.W^{-1})**	***k*** **(W.m^{-1}.K^{-1})**
Si bulk	-0.802	148.0
USG 2900	-0.798	148.8
USG 5400	-0.812	146.2
SiCN 350	-0.800	148.4
SiCN 600	-0.800	148.3
SiN 300	-0.806	147.3
SiN 600	-0.798	148.8

Table 2.11: Substrate thermal conductivity determined with 3ω method.

Eq. (2.34) allows the experimental slopes to be related to the thermal conductivities of the substrate k. Table 2.11 summarizes the slopes and k for each sample. The determined thermal conductivities k of the substrates are close to 148 W.m^{-1}.K^{-1} for all samples. This is in good agreement with the expected values of k because all the thin layers have been deposited on a bulk silicon wafer. This will allow us to be confident in the following analyze of the temperature rises $\Delta T_F/P_0$ for the determination of the effective thermal conductivities of the thin layers k.

III.3.B.b. Layer effective thermal conductivity

Eq. (2.36) allows us to deduce from the experimental temperature rises the effective thermal conductivity of the layer k_F. Table 2.12 summarizes the values of $\Delta T_F/P_0$ and k_F for each monolayer sample used in this study and the associated uncertainty. Furthermore, it is possible to estimate the accuracy of the determination of the effective thermal conductivity of a layer. We need to take into account the uncertainty on the characterization of the length of the heater ΔL, the half-width of the heater Δb and the temperature rise $\Delta(\Delta T_F/P_0)$ as follows:

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$$\frac{\Delta k_F}{k_F} = \sqrt{\left(\frac{\Delta b}{b}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta(\Delta T_F)}{\Delta T_F}\right)^2}, \quad (2.39)$$

The uncertainty on the determination of the effective thermal conductivity of the layer is found to be lower than 2%. The 3ω method appears to be very accurate in order to determine the effective thermal conductivity of a thin layer on the top surface of a silicon substrate.

	$\Delta T_F/P_0$	$\Delta(\Delta T_F/P_0)$	k_F
	K.W^{-1}	‰	W.m^{-1}.K^{-1}
USG 2900	15.6	1.1	1.24
USG 5400	28.1	1.3	1.31
SiCN 350	4.61	1.9	0.52
SiCN 600	5.36	1.2	0.76
SiN 300	3.12	3.3	0.66
SiN 600	4.82	2.9	0.85

Table 2.12: Layer effective thermal conductivity determined with 3ω method.

III.3.C. Results and discussion

In this section, the aim is to determine the influence of the medium and the interfaces in the global thermal resistance of the thin layers. Then, a conclusion on the 3ω method is drawn.

III.3.C.a. Thermal resistance of the thin films

In the case of a thin layer on top of a silicon substrate, the thermal resistance of the thin film R_{th} can be defined as follows:

$$R_{th} = \frac{E_F}{k_F}, \quad (2.40)$$

$$R_{th} = \frac{1}{G_{TBC}} + \frac{E_F}{k_{medium}}, \quad (2.41)$$

where G_{TBC} is the TBC generated by the interfaces surrounding the layer and k_{medium} is the intrinsic thermal conductivity of the material of the layer. With two different thicknesses of a thin film material, it is therefore possible to determine G_{TBC} and k_{medium}. Provided k_{medium} does not vary, which is the case for amorphous and low-thermal conductivity materials. However, better results could be achieved with even-more material thicknesses. Table 2.13 gives the results.

	k_{medium}	Δk_{medium}	G_{TBC}	ΔG_{TBC}
	W.m^{-1}.K^{-1}	W.m^{-1}.K^{-1}	MW.m^{-2}.K^{-1}	MW.m^{-2}.K^{-1}
USG	1.5	0.04	25	0.7
SiCN	2.3	0.3	19	2.5
SiN	1.3	0.1	50	3.8

Table 2.13: Intrinsic thermal conductivities and TBC for USG, SiCN and SiN materials.

III.3.C.b. Conclusion on the 3ω method

For each sample studied with the 3ω method, the values of intrinsic thermal conductivities and TBC are determined, as shown in Figure 2.41. The values of intrinsic thermal conductivities are in good agreement with the literature [32-36]. For very thin layers (SiCN and SiN), the thermal resistance is mainly due to the TBCs whereas for the thicker layer (USG), it is mainly due to the effect of the medium. It is also important to see that the TBC measured with the 3ω method are one order of magnitude lower than the values calculated in AMM and DMM [17]. It could be due to the TBC of the titanium

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layer and could be interesting to analyze in the future. Notably, it is not the first time that TBC measurement are lower than predictions [37].

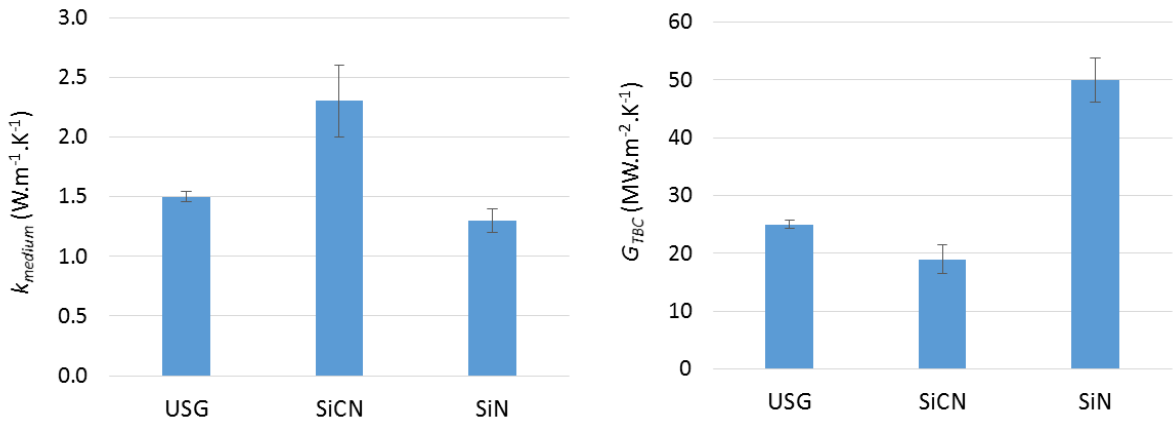

Figure 2.41: Measurement with the 3ω method for USG, SiCN and SiN samples. a) Intrinsic thermal conductivity. b) Thermal boundary conductance.

The 3ω method is difficult to implement on a large number of samples. The manufacturing yield being moderate, this method is time-consuming in terms of fabrication and device characterization. However, the thermal conductivity characterization of thin films can be done with very good accuracy. The advantages and drawbacks of the 3ω method are summarized in Table 2.14.

	3ω method
Model calibration	✕ Heater geometry and TCR characterization (D. G. Cahill [22])
Spatial resolution	✕ No spatial resolution
Sample Characterization	✓✓ Bulk & thin films with low & high k

Table 2.14: Capabilities of the 3ω method.

IV. Discussion

IV.1. Sample effective thermal conductivities

	SThM Wollaston	**3ω method**	**Literature**
USG 2900	-	1.21-1.24	1.23-1.36 [32, 36]
USG 5400	-	1.32-1.35	1.33-1.42 [32, 36]
SiN 300	-	0.68-0.70	0.59-0.80 [32, 35]
SiN 600	-	0.89-0.91	0.66-1.10 [32, 35]
SiCN 350	-	0.50-0.52	-
SiCN 600	-	0.74-0.76	-
BD1 3300	0.44-0.59	-	0.35-0.61 [39, 40]
BD1 5600	0.33-0.42	-	0.35-0.61 [39, 40]
ULK 1250	0.06-0.08	-	0.07-0.13 [38]
ULK 2400	0.11-0.14	-	0.08-0.16 [38]

Table 2.15: Comparison between measurements (SThM with Wollaston probe and 3ω method) and literature for the effective thermal conductivity of USG, SiN, SiCN, BD1 and ULK thin films.

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Table 2.15 summarizes the thermal conductivities measured by SThM and 3ω method. One can notice that the thermal conductivities measured experimentally are in good agreement with the literature for both SThM and 3ω method. The small differences measured with the Wollaston probe could be due to the calibration in the low-k range which is made by using polymers, and not bond materials.

IV.2. Advantages and drawbacks of the SThM and the 3ω method

The characterization of various thin films materials has been possible with the SThM and the 3ω method. However, the characterization method was chosen according to the studied material. It is therefore necessary to have an estimation of the thermal properties of the material in order to be able to choose the appropriate method effectively. Table 2.16 summarizes the advantages and drawbacks of the SThM and the 3ω method for the measurement of the effective thermal conductivity.

	3ω method	**SThM technique**	
		Palladium nano-probe	Wollaston micro-probe
Sample preparation	✕ Clean room process: photolithography	✓✓ No preparation	✓✓ No preparation
Model calibration	✕ Heater geometry and TCR characterization (D. G. Cahill [24])	✓ Contact calibration with AMM/DMM theories J. D. N. Cheeke [16]	✓ Contact calibration with reference samples A. M. Massoud [13]
Spatial resolution	✕ No spatial resolution	✓✓ Submicrometric	✓ Micrometric
Sample Characterization	✓✓ Bulk & thin films with low & high k	✕ Bulk materials with $k \ll 1$ W.m^{-1}.K^{-1}	✓ Bulk & thin films with $k \ll 1$ W.m^{-1}.K^{-1}

Table 2.16: Summary of the advantages and drawbacks for each characterization technique.

V. Conclusion

In this chapter, two different thermoresistive techniques have been used for the thermal characterization of thin layer materials: Scanning Thermal Microscopy and the 3ω method. The SThM technique has been implemented with two different probes:

(i) the palladium nano-probe;

(ii) the Wollaston micro-probe.

In the case of the palladium nano-probe, it has been shown that the SThM technique does not allow the characterization of the samples with effective thermal conductivity higher than 1 W.m^{-1}.K^{-1}. This is mainly due to the uncertainty on the characterization of the thermal contact between the probe and the sample. Unfortunately, for the thin layers available in this work, their effective thermal conductivity revealed to be too large to be characterized with good accuracy.

In the case of the Wollaston micro-probe, the thermal signal measured with the probe was fitted on reference samples. The comparison between the thermal signal measured on thin layer samples and the calibration fit allowed us to determine their effective thermal conductivity. Finally, the property of each surface layer was determined by using an FEM model of the probe-sample system. In the case of the measurements realized on ULK and BD1 samples, their effective thermal conductivities were found close to typical values of the literature [38-40].

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Finally, the 3ω method was implemented in terms of fabrication and experimental characterization. This is a thermoresistive technique designed for the measurement of the thermal conductivity of bulk materials and thin films. The measurements have been realized only on USG, SiN and SiCN thin films samples due to fabrication issues and time constraints. The measurements of intrinsic thermal conductivities were found to be in good agreement with the literature [32-36]. The advantages and drawbacks of each technique have been determined. The thermal conductivities of the BD1 and ULK samples could be subject to further investigations, especially with the 3ω method in order to validate the SThM experimental data acquired with the Wollaston micro-probe.

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VI. Bibliography

[1] J. Czochralski, A new method for the measurement of the crystallization rate of metals, Zeitschrift für Physikalische Chemie, Volume 92, Pages 219-221, 1918.

[2] M. Asheghi et al., Thermal conduction in doped single-crystal solicon films, Journal of Applied Physics, Volume 91, Issue 8, Pages 5079-5088, 2002.

[3] S.L. Partridge, Silicon-on-insulator technology, IEEE Proceedings I – Solid State and Electron Devices, Volume 133, Issue 3, Pages 66-76, 1986.

[4] G.K. Celler et al., Frontiers of silicon-on-insulator, Journal of applied Physics, Volume 93, Issue 9, Pages 4955, 2003.

[5] V. Gonda et al, Prediction of thermos-mechanical integrity of wafer backend processes, Microelectronics Reliability, Volume 44, Pages 2011-2017, 2004.

[6] M. Pathak et al., Electromigration Modeling and Full-chip Reliability Analysis for BEOL Interconnect in TSV-based 3D ICs, IEEE/ACM International conference on Computer-Aided Design, Pages 555-562, 2011.

[7] T.M. Tritt, Thermal Conductivity: Theory, Properties, and Applications, Springer Science & Business Media, Pages 205-234, 2005.

[8] A. Assy, Development of two technics for thermal characterization of materials: Scanning Thermal Microscopy (SThM) and 2ω method, PhD Thesis, INSA de Lyon, 2015.

[9] G.A. Antonelli et al., Characterization of mechanical and thermal properties using ultrafast optical metrology, MRS Bulletin, Volume 31, Issue 8, Pages 607-613, 2006.

[10] E. Puyoo, Caractérisation thermique de nanofils de silicium pour des applications à la thermoélectricité, PhD Thesis, Université Bordeaux 1, 2010.

[11] N. Stojanovic et al., Thin-Film Thermal Conductivity Measurement Using Microelectrothermal Test Structures and Finite-Element-Model-Based Data Analysis, Journal of Microelectromechanical Systems, Volume 16, Issue 5, Pages 1269-1275, 2007.

[12] A.M. Massoud, Experimental characterization of heat transfer in nanostructured silicon-based materials, PhD Thesis, INSA de Lyon, 2016.

[13] L. Shi and A. Majumdar, Thermal transport mechanism at nanoscale point contact, ASME Journal of Heat Transfer, Volume 124, Issue 2, Pages 329-337, 2002.

[14] A. Assy et al., Heat Transfer Mechanisms Quantified at Submicron Scales in Scanning Thermal Microscopy, Proceeding of THERMINIC, 2015.

[15] J.D.N. Cheeke et al., Analysis of heat transfer between solids at low temperatures, Canadian Journal of Physics, Volume 54, Pages 1759-1771, 1976.

[16] E.T. Swart and R.O. Pohl, Thermal boundary resistance, Reviews of Modern Physics, Volume 61, Issue 3, 1989.

[17] Nanotechnology Solutions Partner, Scanning Thermal Microscopy (SThM): High Spatial and Thermal Resolution Microscopy by the XE-series Innovations, Pages 127-129.

[18] E. Guen, Nanocontact thermique et paramètre d'influence en microscopie thermique à sonde locale, PhD Thesis, INSA de Lyon, 2019.

[19] L.D. Carlos and F. Palacio, Thermometry at the Nanoscale: Techniques and Selected Applications, RSC Nanoscience & Nanotechnology,

[20] P.O. Chapuis, Contribution à l'étude des transferts thermiques à l'échelle nanométrique : interaction pointe-surface, PhD Thesis, Université de Lyon, 2007.

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[21] A. Alkurdi et al., Ballistic air conduction between nano to micro-objects and a flat plane, Poster at EUROTHERM, 2018.

[22] E. Guen et al., Analysis of heat conduction in confined structures by means of scanning thermal microscopy, Proceeding of JMC, 2018.

[23] D.G. Cahill, Thermal conductivity measurement from 30 to 750 K: the 3ω method, Review of Scientific Instruments, Volume 61, Page 802, 1990.

[24] T. Borca-Tasciuc et al., Data reduction in 3ω method for thin-film thermal conductivity determination, Review of Scientific Instruments, Volume 72, Page 2139, 2001.

[25] D. De Koninck, Thermal Conductivity Measurements Using the 3-Omega Technique: Application to Power Harvesting Microsystems, PhD Thesis, McGill University, 2008.

[26] J.Y. Duquesne et al., Analytical solutions of the heat diffusion equation for 3ω method geometry, Journal of Applied Physics, Volume 108, Page 86104, 2010.

[27] A. Jain and K.E. Goodson, Measurement of the thermal conductivity and heat capacity of freestanding shape memory thin films using the 3ω method, Journal of Heat Transfer, Volume 130, Page 102402, 2008.

[28] W. Jaber, Phonon heat conduction probed by means of an electro-thermal method involving deposited micro and nanowires, PhD thesis, Université de Lyon, 2016.

[29] W. Jaber and P.O. Chapuis, Non-diealities in the 3ω method for thermal characterization in the low- and high-frequency regimes, AIP Advances, Volume 8, Issue 4, Pages 1-13, 2018.

[30] W. Parker et al., A Flash Method of Determining Thermal Diffusivity, Heat Capacity and Thermal Conductivity, Journal of Applied Physics, Volume 32, Issue 9, Pages 1679-1684, 1961.

[31] I. Moon et al., The 3ω technique for measuring dynamic specific heat and thermal conductivity of a liquid or solid, Review of Scientific Instruments, Volume 67, Issue 29, 1996.

[32] S.M. Lee and D.G. Cahill, Heat transport in thin dielectric films, Journal of Applied Physics, Volume 81, Page 2590, 1997.

[33] J.H. Kim et al., Application of the three omega thermal conductivity measurement method to a film on a substrate of finite thickness, Journal of Applied Physics, Volume 86, Page 3959, 1999.

[34] A. Feldman, Algorithm for solution of the thermal diffusion equation in a stratified medium with a modulated heating source, High Temperatures. High Temperatures, Volume 31, Page 293, 1999.

[35] M. Bogner et al., Differential 3ω method for measuring thermal conductivity of AlN and Si_3N_4 thin films, Thin Solid Films, Volume 591, Pages 267-270, 2015.

[36] T. Yamane et al., Measurement of thermal conductivity of silicon dioxide thin films using a 3ω method, Journal of Applied Physics, Volume 91, Page 9772, 2002.

[37] A. Al Mohtar et al., Thickness-dependent thermal properties of amorphous insulating thin films measured by photoreflectance microscopy, Thin Solid Films, Volume 642, Pages 157-162, 2017.

[38] A. Delan et al., Thermal conductivity of ultra low-k dielectrics, Microelectronic Engineering, Volume 70, Issues 2-4, Pages 280-284, 2003.

[39] F. Chen et al., Measurements of effective thermal conductivity for advanced interconnect structures with various composite low-k dielectrics, Proceeding of IRPS, 2004.

[40] D. Ney et al., Analytical extraction of thermal conductivities of low k dielectrics for advanced technologies, Proceeding of IIRW, 2004.

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Chapter 3. Heat transfer modelling for Integrated Circuits and experimental validation

In this chapter, the aim is to develop a relevant approach of numerical modelling by Finite Element to allow the prediction of the thermal behavior of 3D hybrid bonding chips [1, 4]. First, a specific test chip, developed for the investigation of thermal issues, will be detailed. Then, a methodology of numerical modelling will be developed. Finally, the numerical calculations will be compared to experimental data acquired on M3EM test chip by means of SThM and Infrared (IR) thermometry.

I. 3D hybrid bonding test chip for thermal investigations

In this section, a strategy for the modelling of an electronic chip will be developed. To do so, a test chip will be used as a reference for the development of a FEM model. A test chip called M3EM has been designed to help understanding the heating phenomena in 3D integrated circuits (3D ICs). ST and CEA LETI have co-developed this test chip in order to quantify the efficiency of the HB fabrication process in terms of heat management.

I.1. Structure of the 3D hybrid bonding test chip M3EM

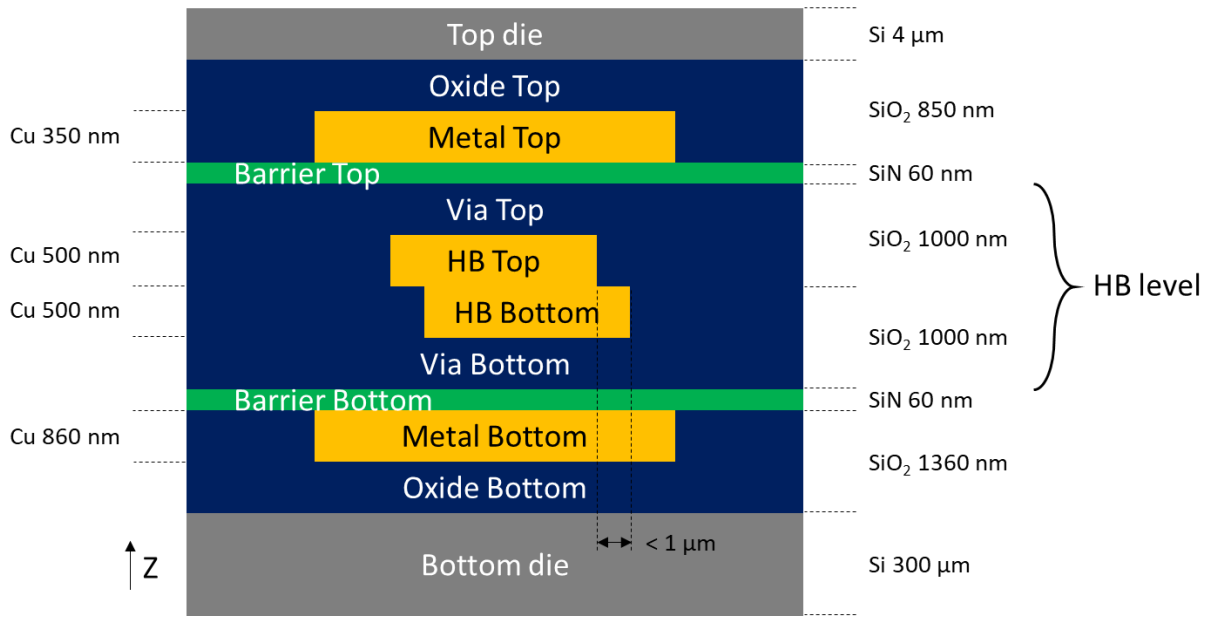

Figure 3.1: Schematic of the cross section of the test chip M3EM.

As first step, M3EM was used to characterize the influence of the package and the heat spreader on heat dissipation [5, 6]. Here, it will be used as a reference for the calibration and validation of the future FE model. Figure 3.1 shows the cross section of M3EM. It is important to notice that M3EM is a passive device without FEOL. As a consequence, in order to still generate a heat flux, copper serpentine have been embedded in the *Metal Bottom* and *Metal Top* layers to act as Joule heaters. *Metal Bottom* and *Metal Top* are therefore used to represent the equivalent FEOL power generation.

I.2. Design of the metal layers

In order to generate heat into the stack, only the *Metal Bottom* level is used. Copper serpentines have been embedded in the *Metal Bottom* to generate heat by Joule effect. The small right heater is chosen

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because being small, it will generate larger thermal gradients. In addition, the size and power generation of the small right heater are representative of heating structures in commercial chips [7]. Figure 3.2 shows the patterns of the copper lines. The metal serpentine in Figure 3.2.b) consists of a fine wire highly resistive electrically and access lines whose section has been multiplied in order to reduce the electrical resistance. The Joule power generation is therefore considered located in the small right heater and not in the access lines.

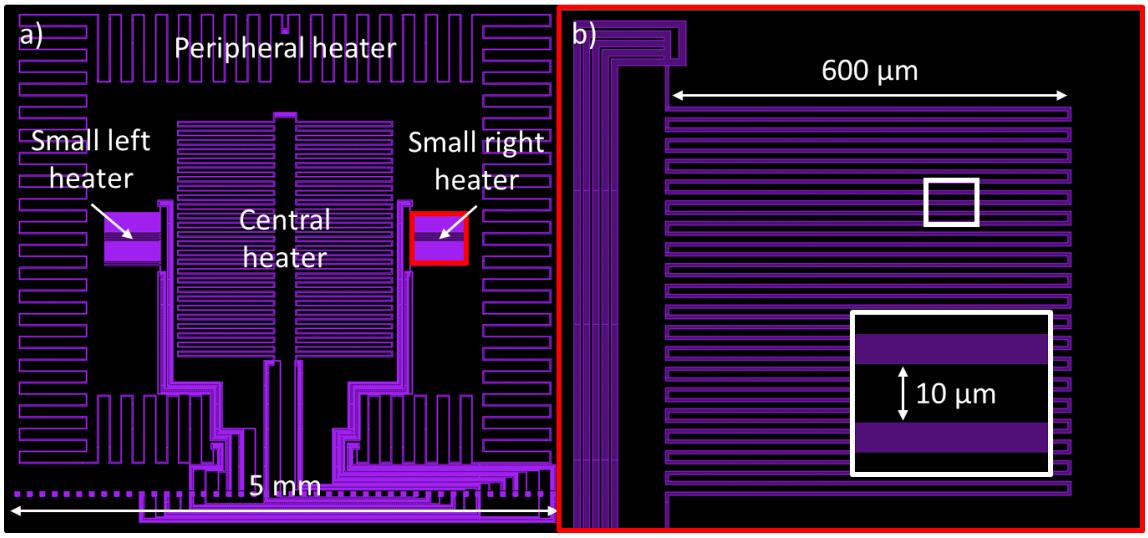

Figure 3.2: Design of the Metal Bottom level of M3EM. a) Heating elements with serpentine resistance. b) Geometry of the small right heater with an insert on a copper line.

Copper dummies are added in the silicon dioxide matrix all around the copper lines. This structures are added to avoid fabrication process issues, especially during Chemical and Mechanical Planarization (CMP) and ensure sufficient copper density. Figure 3.3 shows the geometry of the dummies. The dummies of the *Metal Top* layer are identical to the dummies of the *Metal Bottom* layer.

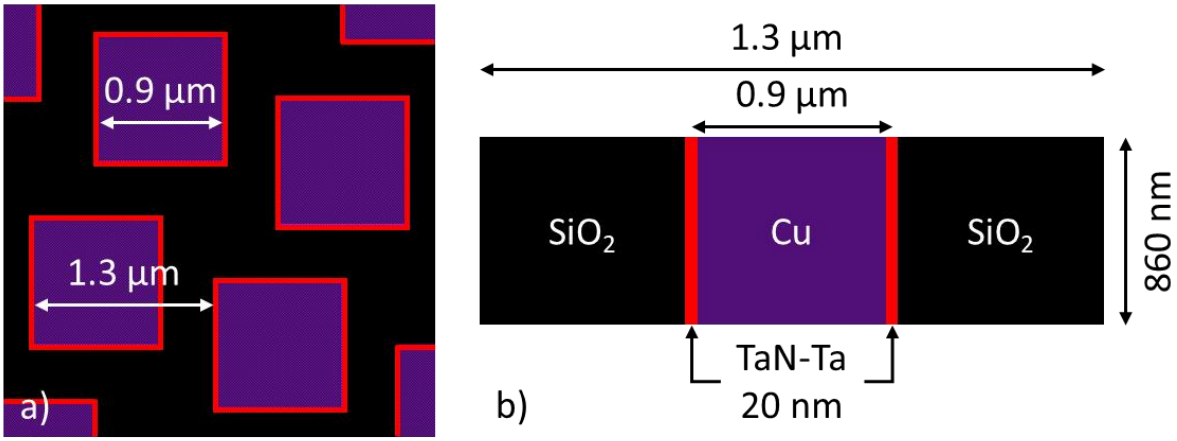

Figure 3.3: Geometry of the copper dummies into the silicon dioxide matrix.
a) Top view of the dummies. b) Cross section of one dummy.

I.3. Description of the hybrid bonding structure

In the case of the HB layer, the copper pattern covers the entire surface of the layer. Figure 3.4 shows the geometry of the HB pads. In our study, the misalignment between the bottom and the top part of the HB layer will be neglected (see Figure 3.1).

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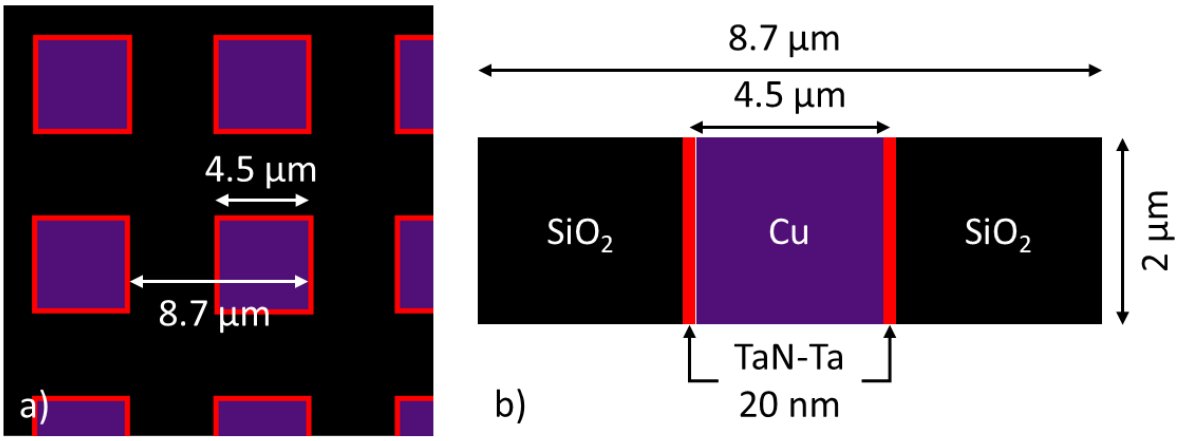

Figure 3.4: Geometry of the hybrid bonding layer. a) Top view of the hybrid bonding pads. b) Cross section of one hybrid bonding pad.

II. Numerical modelling of multilayer electronic device

II.1. Numerical modelling issues for ICs

In this study, numerical modelling by FEM is chosen. The idea is to develop a model of the chip in its thermal environment to estimate the elevation of temperature generated by the heating elements. This simulation could be used in the future to analyze the effect of different parameters (thermal properties, geometry, thermal boundary resistances…) on heat dissipation. Here, the heating element is the small right heater located in the *Metal Bottom* level (see Figure 3.2). The issues we are facing will be detailed first, and then, the strategy implemented in FEM will be explained.

II.1.A. Meshing issues in FEM for multilayer devices

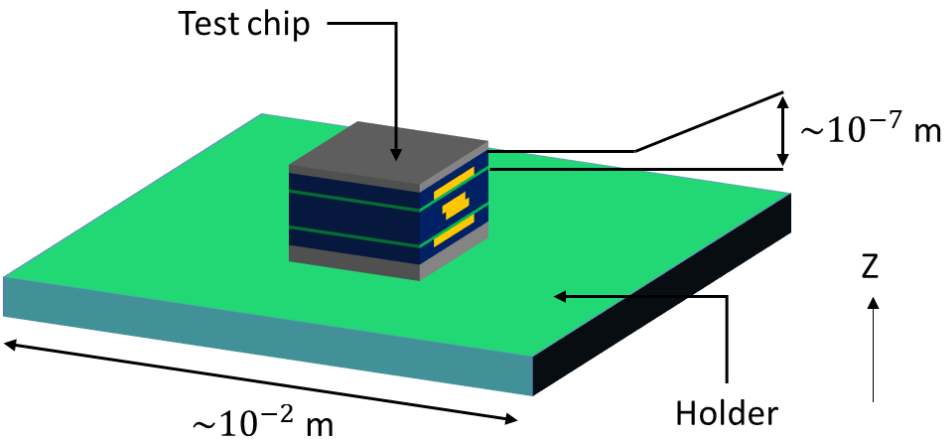

Figure 3.5: Aspect ratio between the layer thicknesses and the setup dimension.

In the field of computational sciences, and especially with FEM, the quality of the output data are strongly related to the mesh quality. Basically, in first approximation, the maximum size of the finite elements need to be smaller than the minimum characteristic length of the geometry of interest. The large aspect ratio between the smallest dimensions (~few nanometers) and the centimetric size of the setup Figure 3.5 leads to very high element number [8, 9]. For such geometries, the aspect ratio turns to be higher than 10^5. An accurate FEM model would need at least a hundred million elements. Being too high to be computed in a decent time, the number of elements has to be reduced. To do so, the structure of the BEOL will be homogenized.

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II.1.B. Homogenization methods for heterogeneous media

In the case of a heterogeneous medium, the homogenization of the thermal conductivity can be performed according different theories. Among them, three different homogenization methods are considered: first, the Maxwell-Garnett and Maxwell-Bruggeman models, and finally the parallel and series thermal conductance model.

II.1.B.a. Maxwell-Garnett model

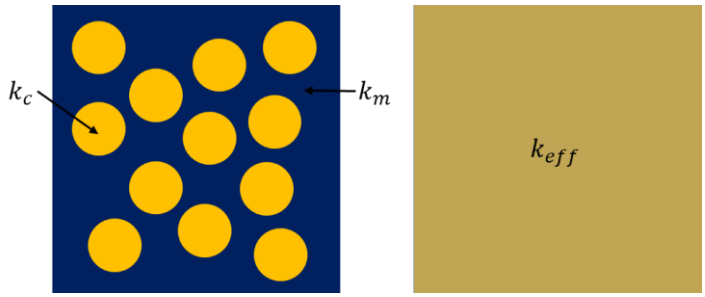

Figure 3.6: Representation of EMA with Maxwell-Garnett model.

Several models have been developed to take into account the shape of the inclusions, their anisotropy, their orientation as well as the interactions between them and with the matrix. The Maxwell-Garnett model is one of them. It accounts for the shape of the inclusions, always in the case of an isotropic and homogeneous dispersion. This model is valid for moderate volume fraction (up to 20%) because inclusions are considered isolated from each other [10]. The effective medium approximation (EMA) developed by Maxwell-Garnett is based on the concept shown in Figure 3.6. In 3D, the expression of the effective thermal conductivity k_{eff} according to Maxwell-Garnett is

$$k_{eff} = k_m \frac{k_c+2k_m+2x(k_c-k_m)}{k_c+2k_m-x(k_c-k_m)}, \tag{3.1}$$

where x and k_c are the volume fraction and the thermal conductivity of the spheres. k_m is the thermal conductivity of the matrix.

II.1.B.b. Maxwell-Bruggeman model

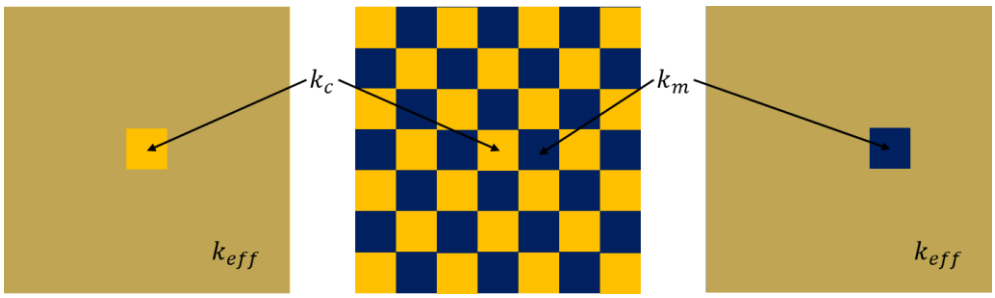

Figure 3.7: Representation of EMA with Maxwell-Bruggeman model.

The effective medium approximation (EMA) developed by Bruggeman is based on the concept shown in Figure 3.7. A volume fraction x of thermal conductivity k_c is included in a medium of effective thermal conductivity k_{eff}. Equivalently, a volume fraction $(1-x)$ of thermal conductivity k_m is included in the medium of effective thermal conductivity k_{eff}. The expression of the effective thermal conductivity k_{eff} according to Bruggeman is

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$$x\left[\frac{k_c-k_{eff}}{k_c+(d-1)k_{eff}}\right]+(1-x)\left[\frac{k_m-k_{eff}}{k_m+(d-1)k_{eff}}\right]=0, \quad (3.2)$$

where d represents the dimensionality of the system. This approach is symmetrical so that the two constituents have an equivalent contribution. If the ratio $k_c/k_m \gg 1$, this model provides a percolation threshold for 30% of its conductive phase volume fraction. This model is particularly suitable for disordered heterogeneous media consisting of conductive spheres in an insulating matrix [11].

II.1.B.c. Parallel and series thermal conductance

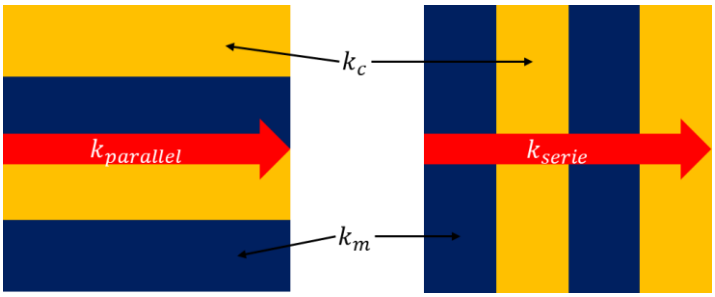

Figure 3.8: Representation of EMA with parallel and series thermal conductance.

The parallel and series thermal conductance modeling consist in representing the composite as a stack of insulating and conductive layers. It is based on the concept shown in Figure 3.8. By establishing the analogy with an electrical circuit, the structure is associated with resistances in series or in parallel depending on the direction of the heat flux, perpendicular or parallel to the interfaces.

$$k_{serie}=\frac{1}{\sum\frac{x_i}{k_i}}, \quad (3.3)$$

$$k_{parallel}=\sum x_i k_i, \quad (3.4)$$

where x_i the volume fraction and k_i the thermal conductivity of each material, respectively. These models are representative of the thermal conductivity of composites in the case of a strongly oriented structure [12].

II.2. Thermal conductivity homogenization for ICs

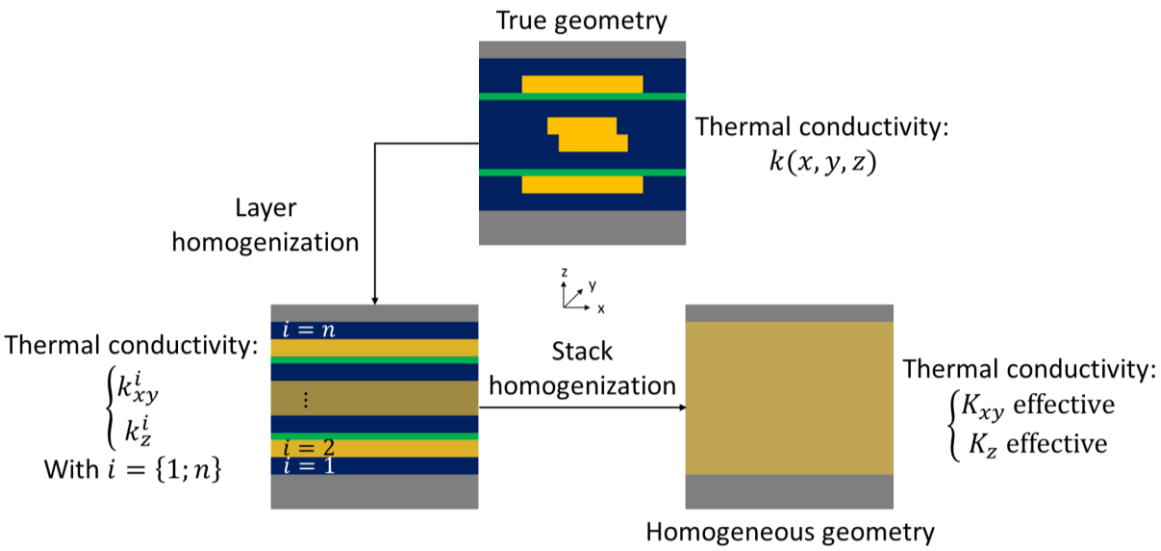

Figure 3.9: Homogenization strategy for a multilayer structure like M3EM.

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In the case of an electronic chip, a multiscale homogenization strategy is chosen. First of all, the thermal conductivity of each layer will be homogenized. Then, considering that the number of layers remains important (twelve layers for the simple test chip M3EM), the homogenization of the thermal conductivity will be extended to the entire stack of the chip. Figure 3.9 shows the principle of the homogenization steps used for M3EM. $k(x, y, z)$ is the general spatial thermal conductivity of the real stack. k_{xy}^{i} and k_{z}^{i} are respectively the in-plane and out-of-plane effective thermal conductivities for each layer. K_{xy} and K_{z} are respectively the in-plane and out-of-plane effective thermal conductivities of the entire stack.

II.2.A. Homogenization of thermal conductivity in the metallic layers

For the metal layers of M3EM (*Metal Bottom*, *Metal Top* and *HB*) with heterogeneous structures, an effective thermal conductivity will be calculated in both in-plane and cross-plane directions.

II.2.A.a. In-plane thermal conductivity

A model of effective medium is used to homogenize the in-plane thermal conductivity of the metal levels (*Metal Bottom*, *Metal Top* and *HB*). The FEM model presented in Figure 3.10 allows calculating the value of thermal conductivity in the in-plane direction k_{xy}. This model suits perfectly this study case because the structure of the metal layer is heterogeneous and fully periodic (see Figure 3.3 and Figure 3.4). A temperature gradient is set over the sub-domain considered by imposing a fixed temperature ΔT_x, and the flux ϕ_x is calculated numerically. The effective in-plane thermal conductivity k_{xy} is therefore calculated with:

$$G = \frac{\phi_x}{\Delta T_x}, \tag{3.5}$$

$$k_{xy} = G\frac{L}{S}, \tag{3.6}$$

where L is the length of the cell (equal to the pitch of the dummies) and S the surface area normal to the heat flux. The thermal conductivity of silicon dioxide (k_{SiO_2}) is set to 1.3 W.m^{-1}.K^{-1} (see Chapter II and [13]). The thermal conductivities of copper (k_{Cu}) and of the Ta-TaN layer (k_{TaNTa}) are estimated from their electrical resistivities (2 and 70 µΩ.cm, respectively) by applying the Wiedemann-Franz law [14]. k_{Cu} and k_{TaNTa} are found equal to 330 and 9.5 W.m^{-1}.K^{-1}, respectively. Here, the thermal boundary resistances between materials can be neglected because the layer is mainly constituted of silicon dioxide, which is a thermal insulator.

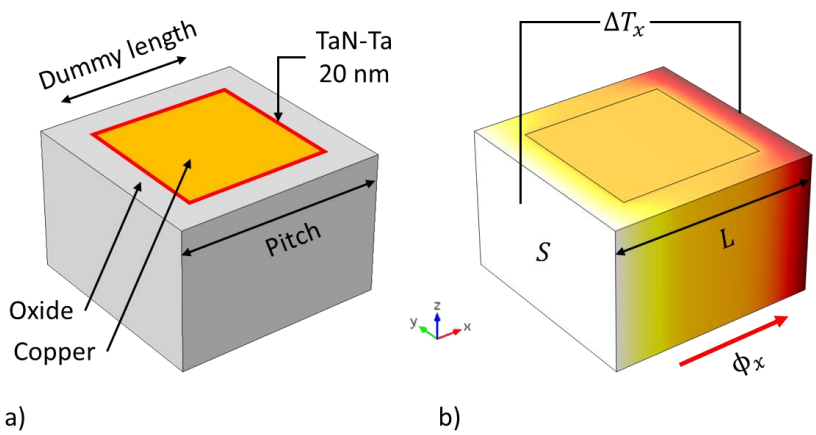

Figure 3.10: Homogenization of the in-plane thermal conductivity in metal levels. a) Geometry of the unit cell with the dummy. b) Calculation of the effective in-plane thermal conductivity.

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II.2.A.b. Cross-plane thermal conductivity

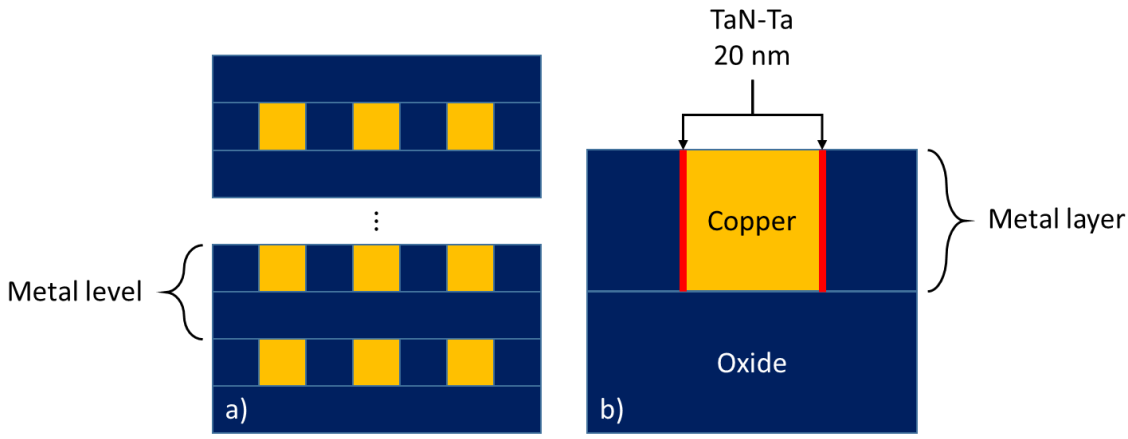

Figure 3.11: a) Schematic of the BEOL cross section in ICs. b) Zoom on the periodic unit cell.

In order to homogenize the cross-plane thermal conductivity of the metal levels (*Metal Bottom*, *Metal Top* and *HB*) a model of effective medium has been used. In this case, the stack of the chip will be considered as a heterogeneous periodic medium in the z direction. A schematic of the stack is presented in Figure 3.11. For commercial chips, with more than ten metal levels, the periodic assumption is therefore even more relevant. However, in the case of M3EM chip with only four metal levels, this should be acceptable in first approximation and could be subject to further investigations. The FEM model presented in Figure 3.12 allows calculating the value of thermal conductivity in the cross-plane direction k_z for each single metal level. A temperature gradient is set over the sub-domain considered by imposing a fixed temperature ΔT_z, and the flux ϕ_z is calculated numerically. The effective cross-plane thermal conductivity k_z is therefore calculated with:

$$G = \frac{\phi_z}{\Delta T_z}, \tag{3.7}$$

$$k_z = G\frac{L}{S}, \tag{3.8}$$

where L is the length of the cell (equal to the layer thickness) and S the surface area normal to the heat flux (pitch squared). Moreover, the effective thermal conductivities k_{xy} and k_z do not depend on the number of cells modelled in FEM.

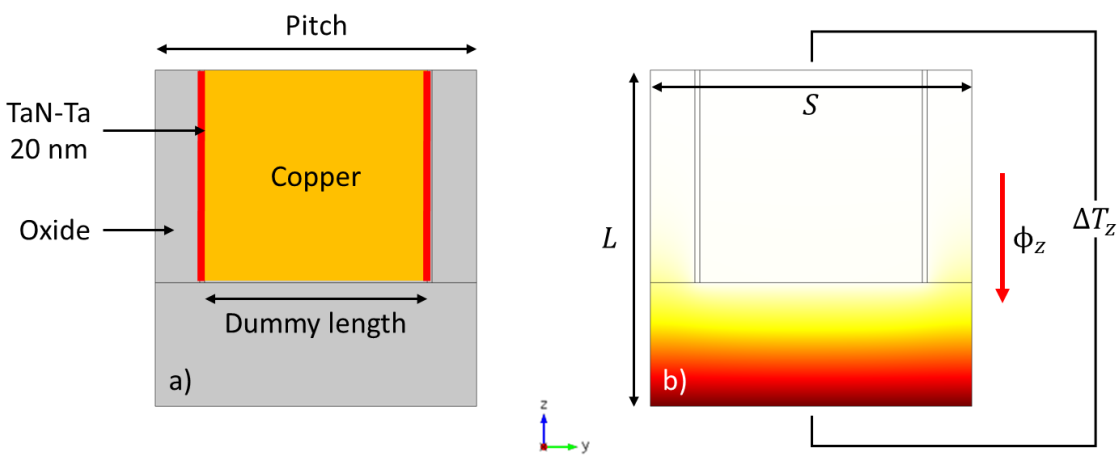

Figure 3.12: Homogenization of the cross-plane thermal conductivity in metal level. a) Geometry of the unit cell with the dummy. b) Calculation of the effective cross-plane thermal conductivity.

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II.2.A.c. Summary of homogenized-layer thermal conductivities

The homogenized properties of the different layers are summarized in Table 3.1. Note that the impact of Thermal Boundary Resistances (TBR) is negligible here in the xy and z directions, since many oxide layers already thermally-resistive are present in the structure. Here the thermal conductivity of the barriers (silicon nitride) is taken equal to 0.85 W.m^{-1}.K^{-1} (see Chapter II and [15]).

Layer	Dummies	Level	NUMERICAL		ANALYTICAL	
			k_{xy}	k_z	k_{xy}	k_z
			W.m^{-1}.K^{-1}	W.m^{-1}.K^{-1}	W.m^{-1}.K^{-1}	W.m^{-1}.K^{-1}
Oxide Top	✕	Metal Top	2.76	2.03	2.49	2.20
Metal Top	✓					
Barrier Top	✕	Barrier Top	0.85	0.85	0.85	0.85
Via Top	✕	HB	2.23	1.72	2.00	2.56
HB Top	✓					
HB Bottom	✓					
Via Bottom	✕					
Barrier Bottom	✕	Barrier Bottom	0.85	0.85	0.85	0.85
Metal Bottom	✓	Metal Bottom	3.16	3.23	3.12	3.50
Oxide Bottom	✕					

Table 3.1: Homogenization of in-plane and cross-plane thermal conductivities for the levels of M3EM with numerical and analytical procedures.

II.2.B. Homogenization of thermal conductivity in the BEOL layers

	NUMERICAL	ANALYTICAL
K_{xy} (W.m^{-1}.K^{-1})	2.6	2.4
K_z (W.m^{-1}.K^{-1})	2.0	2.6

Table 3.2: Homogenized in-plane and cross-plane thermal conductivities for M3EM BEOL with numerical and analytical procedures.

In the case of the BEOL, the floorplans of the metal levels show very ordered structures (schematic in Figure 3.11) with regular copper dummies. Maxwell-Garnett and Maxwell-Bruggeman models are therefore not suitable for the EMA of the metal levels of M3EM. Consequently, in the next parts, the EMA strategy will be based on the parallel and series thermal conductance model. The relevance of this model will be validated later. Considering a model of parallel and series thermal conductance, it is possible to evaluate the global effective thermal conductivities of the entire stack in the in-plane and out-of-plane directions K_{xy} and K_z respectively as follows:

$$K_{xy}.\sum E_i = \sum k_{xy}^i.E_i, \tag{3.9}$$

$$\sum \frac{E_i}{k_z^i} = \frac{\sum E_i}{K_z}, \tag{3.10}$$

$$i = \{1; \mathrm{n}\},$$

where E_i is the thickness of each level. n is the number of level. The total in-plane and cross-plane thermal conductivities K_{xy} and K_z are summarized in Table 3.2 for both numerical and analytical methods. These values are somewhat low, highlighting:

(i) the low copper density in the via layers;

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(ii) that the chip could not be kept at room temperature under operation and would undergo clear heating;

(iii) the effective thermal conductivity of the BEOL is almost isotropic.

II.3. FEM modelling of the chip environment

In this section, the modelling of the chip and its environment will be specified. First, the geometry and the boundary conditions will be detailed. Then, the influence of the wire bonding on the heat dissipation will be modelled. Finally, the model will be calibrated with experimental thermoresistive measurement.

II.3.A. Geometry and boundary conditions

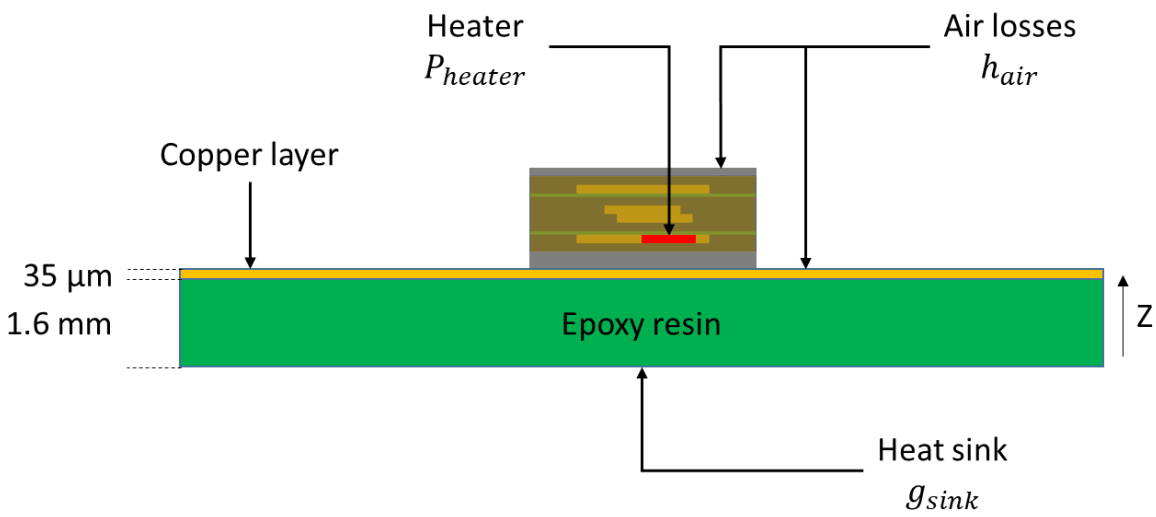

Figure 3.13: Geometry and boundary conditions considered for M3EM FEM model.

Figure 3.13 shows the geometry and the boundary conditions in the case of the M3EM analysis. P_{heater} is the Joule power generated by the small heater right. The thermal conductance per unit area h_{air} is set as boundary conditions to represent both the heat losses through air and through thermal radiation. A single parameter is used. Finally, the thermal conductance per unit area g_{sink} is characteristic of the heat dissipation towards the substrate holder of the chip. In this study, the M3EM chip is set on a PCB. The PCB is made with a 1.6 mm thick epoxy resin (FR4) layer covered by a 35 µm thick copper layer. The resin thermal conductivity is taken equal to 0.34 $W.m^{-1}.K^{-1}$ following [16]. The copper thermal conductivity is taken equal to the bulk thermal conductivity (390 $W.m^{-1}.K^{-1}$ following [17]) because the thickness of the layer is much larger than the mean free path of the heat carrier in copper (equal to 39 nm following [17]). Here, the Joule power P_{heater} is set to 500 mW in order to represent realistic cases.

II.3.B. Numerical modelling of the wire bonding

For a better accuracy of thermal modelling one needs to account for the impact of the wire bonding on the heat path. In our case, twelve wires of 25 µm diameter D_{wb} are bonded with a pitch of 130 µm on the top die surface. Figure 3.14 shows the positions of the wiring. Numerically, the bonding areas are simulated as local discs of diameter 25 µm with a heat transfer coefficient g_{wb}. Considering the wire as a long wire linking the top die surface at one end and the heat sink at its other extremity, g_{wb} takes the following expressions:

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$$g_{wb} = \frac{k_{Al}}{L_{wb}} \text{ in vacuum,} \tag{3.11}$$

$$g_{wb} = \sqrt{\frac{4h_{air}k_{Al}}{D_{wb}}} \text{ in air,} \tag{3.12}$$

where k_{Al} is the thermal conductivity of the aluminum wire bonding equal to 237 W.m^{-1}.K^{-1} [18], h_{air} is the heat exchange coefficient (describing air losses and thermal radiation) and L_{wb} is the length of the wire equal to 7.5 mm. These expressions are obtained from heat diffusion and the fin equation, respectively. h_{air} is calculated to 454 W.m^{-2}.K^{-1} following [19]. For each bonding wire a boundary condition g_{wb} is set at 31.6 and 131 kW.m^{-2}.K^{-1} in vacuum and air, respectively. Considering these values of g_{wb} much higher than the thermal transfer through air, the wire bonding generates a heat path which could be interesting to be used for thermal optimization.

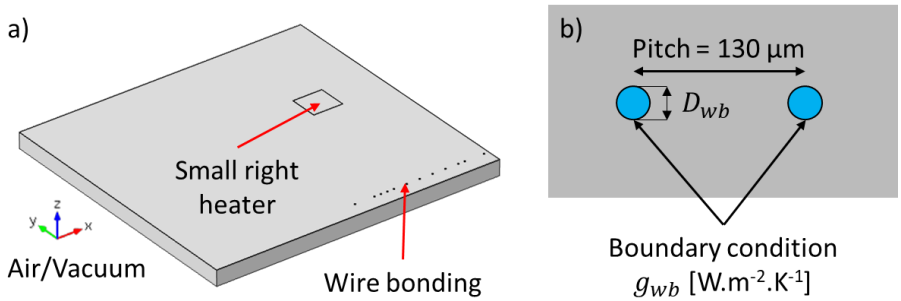

Figure 3.14: a) Wire bonding positions on the top die surface.
b) Disc of heat transfer coefficient g_{wb} set as boundary condition with a pitch of 130 µm.

II.3.C. Model calibration with thermoresistive measurement

In this section, the two last unknown parameters are determined to match the real thermal environment of the chip. The heat sink conductance g_{sink} and the heat loss coefficient h_{air}. To do so, thermoresistive measurements are used.

II.3.C.a. Heat sink conductance

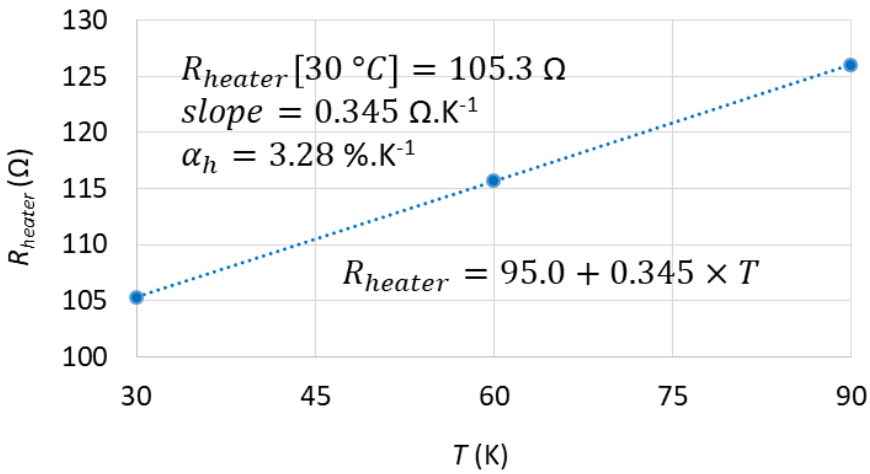

Figure 3.15: Measurement of the small right heater resistance as a function of temperature.

To evaluate the heat sink conductance g_{sink}, a resistive thermometry experiment with the serpentine small right heater is done under vacuum conditions. Consequently, the effect of the air losses are eliminated, and compared with the FEM simulations performed as a function of g_{sink}. The M3EM chip is heated on a hot plate between 30 °C and 90 °C. The heater temperature is measured as follows:

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$$\Delta R = R_{heater}\alpha_h \Delta T, \tag{3.13}$$

where α_h is the TCR of the heater this time, ΔR the variation of resistance of the heater and ΔT the variation of temperature of the heater due to Joule heating. α_h is measured equal to 0.328 %.K^{-1} (see Figure 3.15) and ΔR is measured to be 31.1±1.2 Ω, leading to an average temperature increase ΔT equal to 90±3.5 K. The experiment is reproduced numerically, neglecting the impact of thermal radiation in first approximation. Thermal radiation effects are estimated in Section III.2.B. As a consequence, the value of the heat loss coefficient h_{air} is set to zero in the FEM model. Figure 3.16 indicates the sensitivity of the heater temperature to g_{sink}. With the aforementioned assumptions, g_{sink} is found close to 340 W.m^{-2}.K^{-1}. This value is quite low, indicating a loose thermal contact with the substrate.

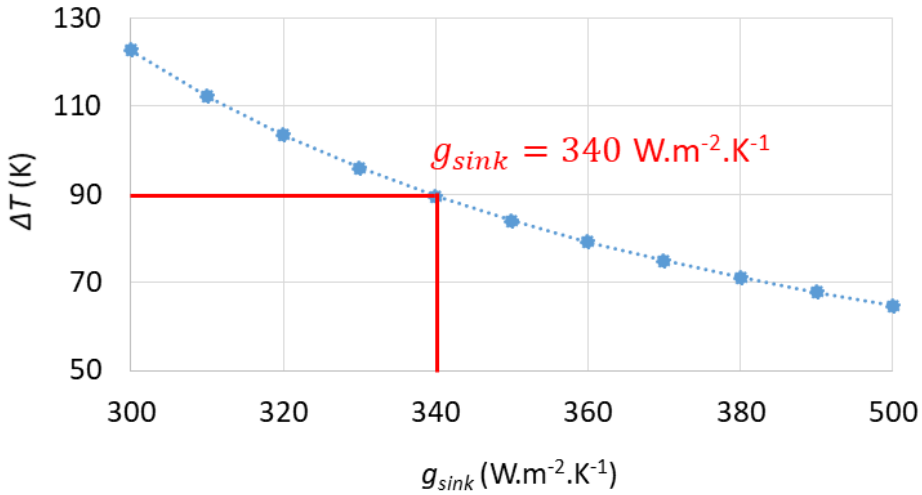

Figure 3.16: Heater average temperature as a function of the heat sink conductance.

II.3.C.b. Heat loss coefficient

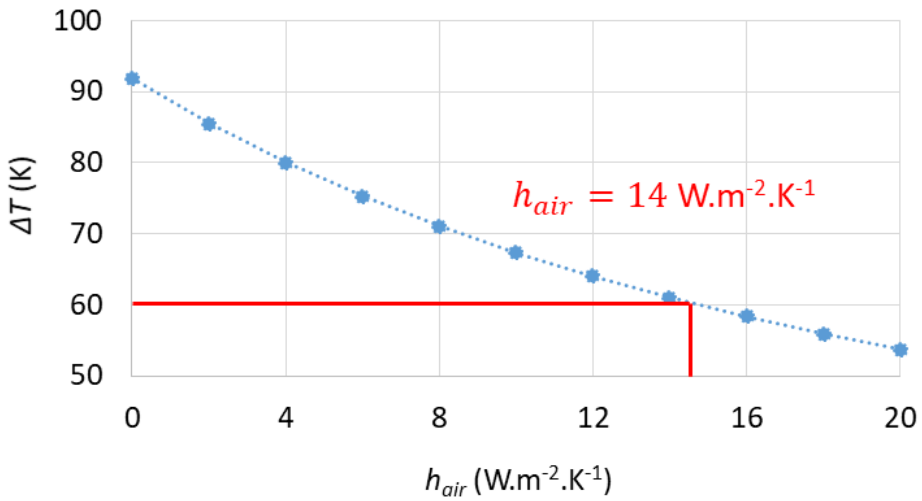

Figure 3.17: Heater average temperature as a function of the heat loss coefficient.

The same methodology is applied under ambient conditions, once the heat sink conductance has been obtained. The measurement performed under air at atmospheric pressure allows determining the heat loss coefficient h_{air} as shown by Figure 3.17. The heater average temperature is this time equal to 60±2.3 K, leading to a value of h_{air} equal to 14 W.m^{-2}.K^{-1}. This value is in good agreement with the previous results shown in [6].

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II.4. Numerical results and discussion

In this section, the temperature field in the chip will be calculated with the FEM homogenized model. The consistency of the homogenization method will be assessed from these numerical data. A multiscale approach will be used to evaluate the temperature close to the heating element. Finally, a discussion will be made on the results obtained by FEM.

II.4.A. Temperature field calculated with homogenized BEOL

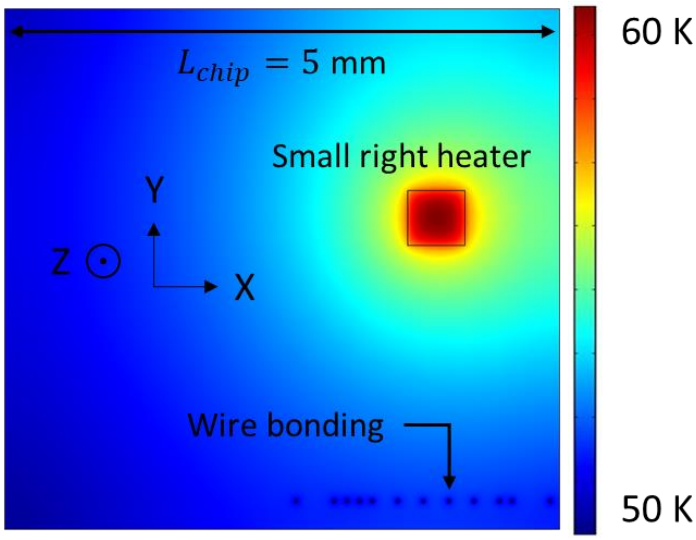

Figure 3.18: Chip surface temperature rise calculated with homogenized BEOL.

The temperature rise is calculated for an input Joule power P_{heater} equal to 500 mW. Figure 3.18 shows the temperature field calculated on the surface of the top die of M3EM chip. Here, the maximum temperature elevation is calculated equal to 60 K at the center of the heater. The minimum temperature elevation is calculated equal to 50 K. One can notice that for this typical case of use, the thermal gradients are low.

We are not interested only in the top die surface temperature. The temperature depth profile, especially at the FEOL and BEOL levels, is important. Figure 3.19 shows the temperature profile in the z direction at the center of the small right heater. Figure 3.19.b) shows that the variation of temperature into the BEOL is lower than 1 K. The BEOL can be considered thermalized in first approximation in the z direction.

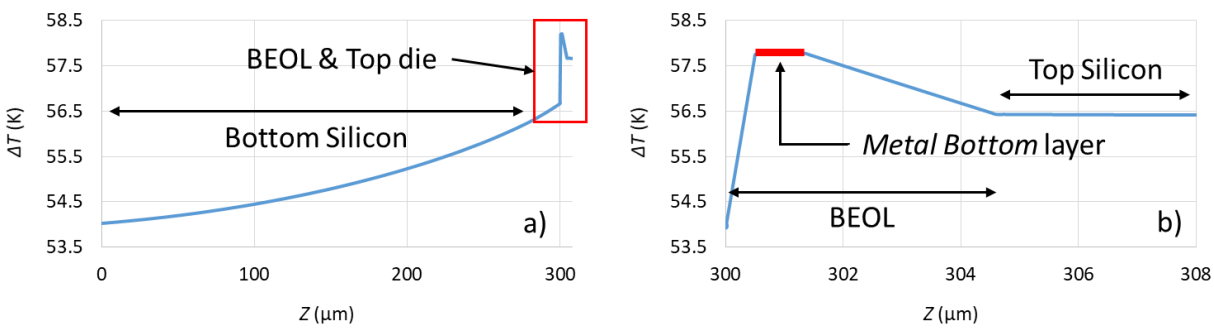

Figure 3.19: a) Temperature rise at the center of the heater as a function of the depth.
b) Insert on the temperature rise inside the BEOL and the top die.

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II.4.B. Consistency of the homogenization procedure

Figure 3.20 represents a schematic of the Joule power distribution in the cross section of M3EM. ϕ_{top} and ϕ_{bottom} are the heat flux projection on the top and bottom side of the BEOL, respectively. Here, ϕ_{top} is equal to 22.5 mW and ϕ_{bottom} is equal to 470 mW. The sum of the fluxes $\phi_{top} + \phi_{bottom}$ represents 97.5% of the total Joule power P_{heater}. In the layers above and below the heater, the flux can thus be easily considered vertical. The parallel and series thermal conductance model is therefore well suited for the homogenization of the BEOL layers. This phenomenon is due to:

(i) the large aspect ratio of the small right heater (square of 600x600 µm² in the xy plane for a thickness equal to 860 nm in the z direction);

(ii) the large thermal conductivity of the silicon dies in comparison of the BEOL. The silicon dies are acting as heat sinks, driving the heat fluxes vertically.

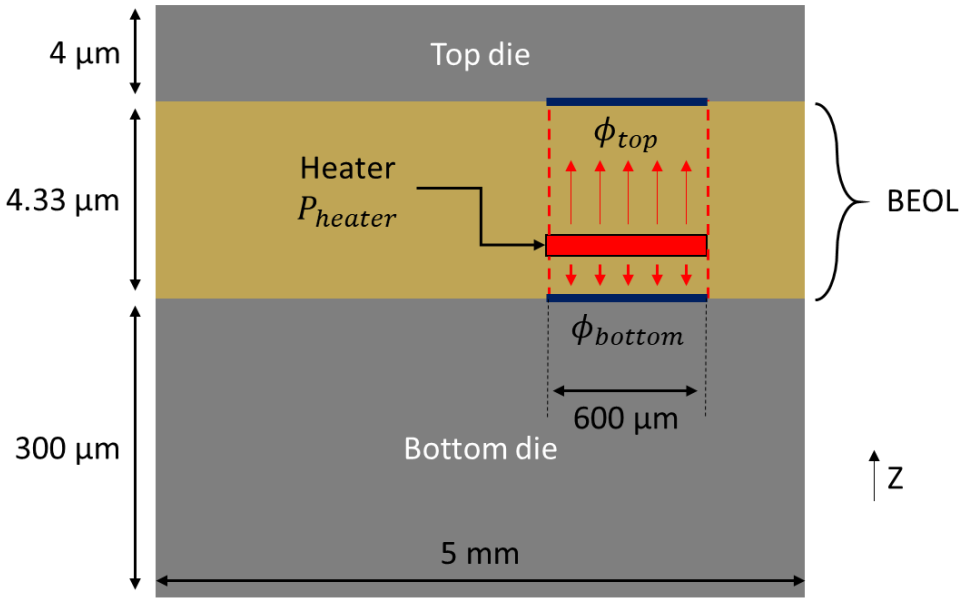

Figure 3.20: Schematic of the heat flux distribution surrounding the BEOL.

II.4.C. Temperature of the heating serpentine

With the homogenized BEOL, the temperature of the stack has been calculated. We emphasize that such model is relevant far from the heating element and as long as the scale of study is large compared to the size of homogenization. To access the temperature of the heater, which is the location of interest, a multiscale FEM modelling is to be applied. First, the strategy of the multiscale modelling, where the copper serpentine is the subdomain of geometry, will be explained. Then the field of temperature close to the heat source will be determined.

II.4.C.a. Multiscale modelling strategy

In order to acquire the temperature field close to the heat source, its explicit thermal environment needs to be modelled. The geometry and the boundary conditions of the FEM model are shown in Figure 3.21.a). Where G_{up} and G_{down} are the thermal conductance coefficients set as boundary conditions on the upper and lower side of the *Metal Bottom* layer, respectively. G_{up} and G_{down} are determined from the global homogenized FEM model (see Figure 3.14).

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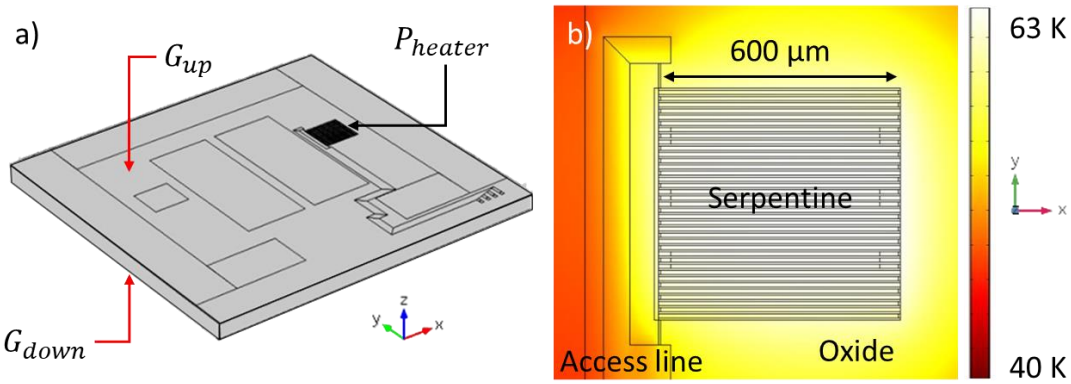

Figure 3.21: a) Explicit geometry of the Metal Bottom layer for multiscale FEM modelling. b) Temperature rise of the small right heater in the Metal Bottom layer of M3EM.

II.4.C.b. Heat source temperature field

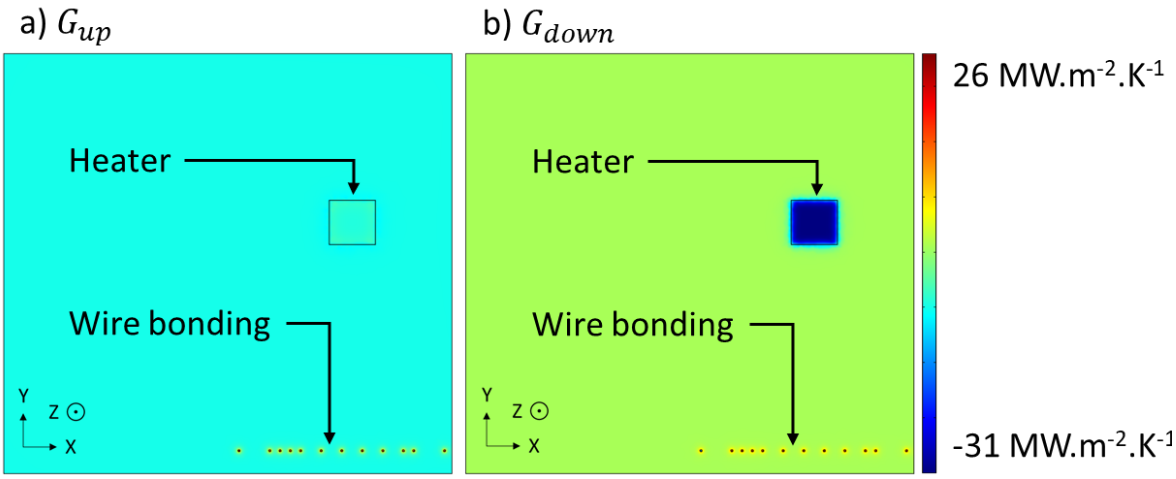

Figure 3.22: Calculation of the up and down thermal conductance coefficients in FEM.

The conductances G_{up} and G_{down} are calculated from the global homogenized model as follows:

$$G_{up} = \frac{\phi_{up}}{\Delta T}, \tag{3.14}$$

$$G_{down} = \frac{\phi_{down}}{\Delta T}, \tag{3.15}$$

where ϕ_{up} is the vertical boundary heat flux going upward in the top die and ϕ_{down} is the vertical boundary heat flux going downward in the bottom die. The calculations of G_{up} and G_{down} are shown in Figure 3.22. The temperature field close to the heat source, can therefore be determined with better accuracy. The temperature field into the small right heater is shown in Figure 3.21.b). The heat flux distribution is summarized in Table 3.3.

Heat path	Power	
	mW	%
Total	500	100
Sink	483	96.6
Air	13.6	2.7
Wire bonding	3.4	0.7

Table 3.3: Summary of the heat flux distribution.

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II.4.C.c. Discussion

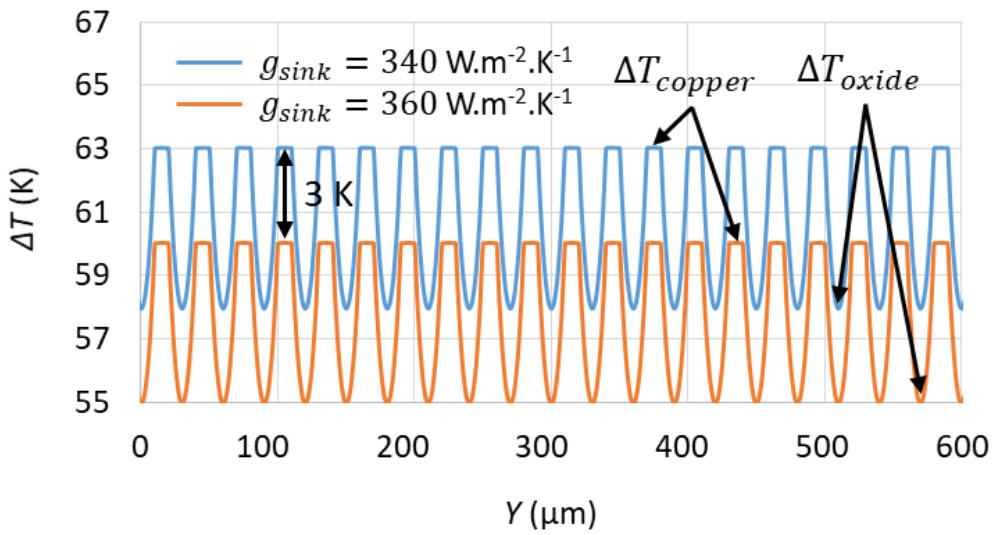

Figure 3.23: Temperature profile along the Y axis, at the middle of the heater.

The temperature of the heat source is calculated with the multiscale FEM modelling. Figure 3.23 shows the temperature rise of the heater over a straight line along the Y axis at the center of the small right heater. ΔT_{copper} and ΔT_{oxide} are the temperature rises of the copper line and the dioxide matrix inside the heater, respectively. The temperature drops are due to the sharp variations of thermal conductivity between the lines of copper and the silicon dioxide matrix. As a reminder, the calibration of the homogenized FEM model was done assuming the heater temperature constant. The heater temperature rise was fitted equal to 60±2.3 K based on thermoresistive measurements (Section II.3.C.). However, Figure 3.23 shows that the actual temperature rise of the copper ΔT_{copper} is equal to 63 K. An error on the calibration of g_{sink} was induced previously because the heater temperature was underestimated. The 3 K temperature difference has been corrected by increasing the value of g_{sink} from 340 to 360 W.m^{-2}.K^{-1}.

III. Experimental characterization of M3EM thermal behavior

In this section, the numerical modelling results will be compared to experimental data obtained on the test chip M3EM. First, the experimental holder that allows the measurements will be described. Then, the temperature measurements will be performed by means of two different techniques: Infrared (IR) thermometry and Scanning Thermal Microscopy (SThM). The possibilities and constraints of each method will be described.

III.1. Description of the experimental holder

In order to perform measurements, the M3EM chip had to be connected and integrated to a homemade electronic circuit inside the SThM and IR machines. First, the connection process of the chip will be described and then the electronic circuit for the chip power supply will be detailed.

III.1.A. Electrical connection of the chip

The chip needs to be connected with the electrical circuit. To do so, a PCB has been designed to hold the chip during power supply. The PCB and the wire bonding to the chip will be described in the following section.

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III.1.A.a. Fabrication of a PCB holder

A PCB has been developed at CETHIL to allow for the electric power supply of the chip. A schematic of the PCB is presented in Figure 3.24. The shape of the PCB is chosen by taking into account the dimensions and weight constraints of the SThM (NT-MDT). The weight of the PCB needs to be lower than 10 g to avoid damaging the piezo element and the current density in the copper lines needs to be lower than 10^6 A.cm^{-2} to avoid electromigration issues following [20-22]. In our case, the current density in the copper lines can be calculated as follows:

$$J = \frac{I_{heat}}{S}. \tag{3.16}$$

I_{heat} is the current, S is the section perpendicular to the electron flux and J is the current density. Here, the lines have been designed with a thickness of 35 µm and a width of 300 µm. By considering a maximum current I equal to 1 A, the current density J stays lower than 10^4 A.cm^{-2}.

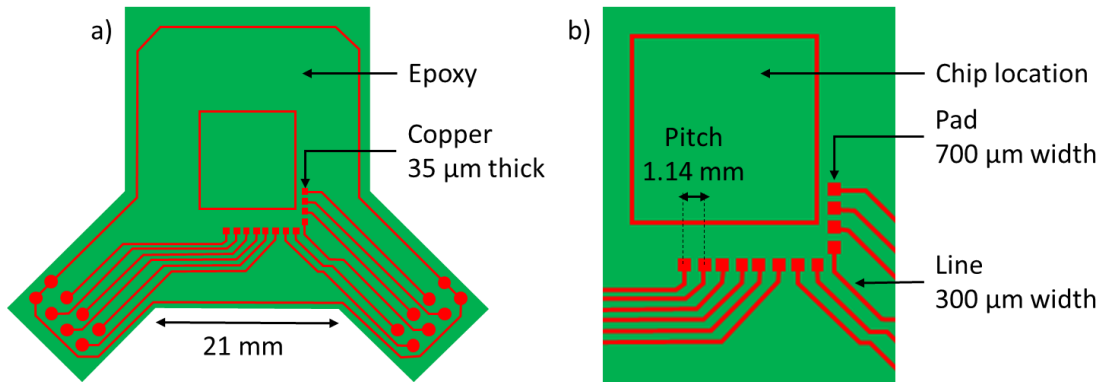

Figure 3.24: Floorplan of the PCB for chip alimentation. a) PCB geometry. b) Pads characteristics.

III.1.A.b. Wire bonding connections

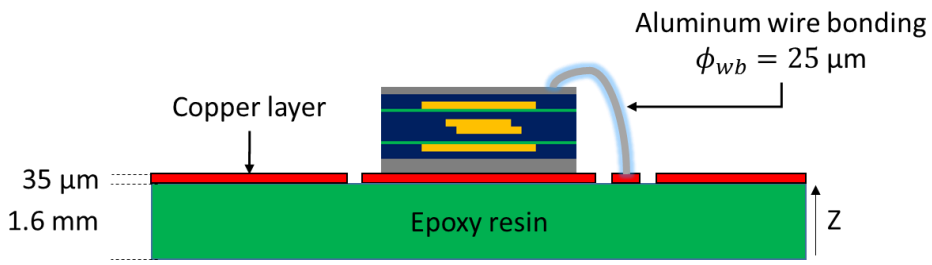

Figure 3.25: Schematic of the wire bonding between M3EM and the PCB.

The chip is connected to the PCB by means of wire bonding. Figure 3.25 shows a schematic of the bonding between the chip and the PCB. The pads on the surface of M3EM have a pitch of 130 µm. Aluminum wire bonding with a diameter ϕ_{wb} equal to 25 µm are chosen. The bonding were made by I. Pheng in the CIME Nanotech laboratory (Grenoble). The wire wedge bonding process has been used. It utilizes ultrasonic energy and pressure to create a bond between the wire and the bond pad. The most predominant process for wedge bonding is an ambient temperature bonding, where aluminum is used to make the interconnection between the die and the PCB. This “welding process” deforms the wire into a flat elongated shape of a wedge. Unlike ball bonding, although more time consuming, the wedge bonding process allows welding at low temperatures without risking damaging the chip. The wire bonding realized on M3EM chip by wedge bonding process are shown in Figure 3.26.

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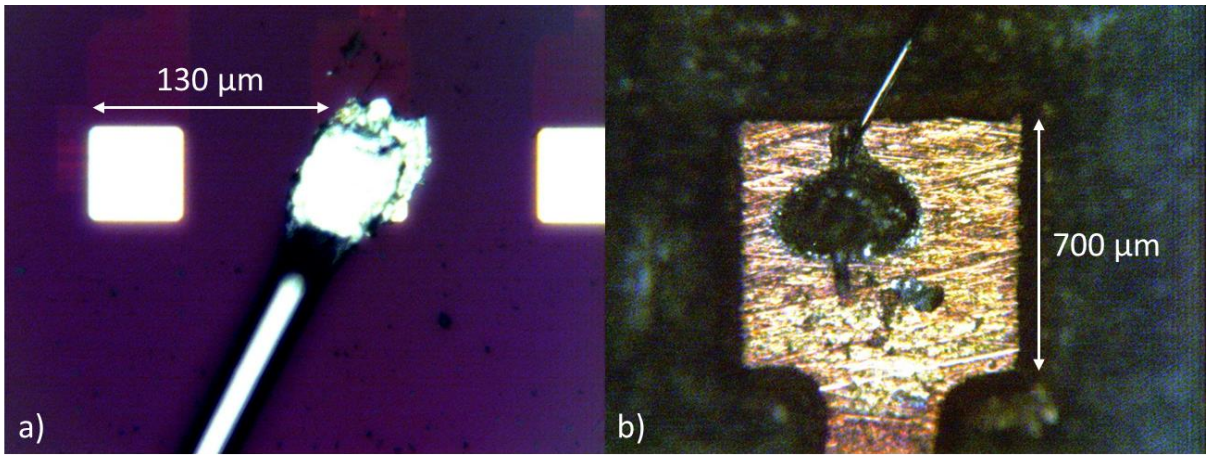

Figure 3.26: Optical microscopy image of the wedge wire bonding realized at CIME Nanotech with a) aluminum pad on top die surface and b) copper pad on epoxy surface.

III.1.B. Electrical circuit of power supply

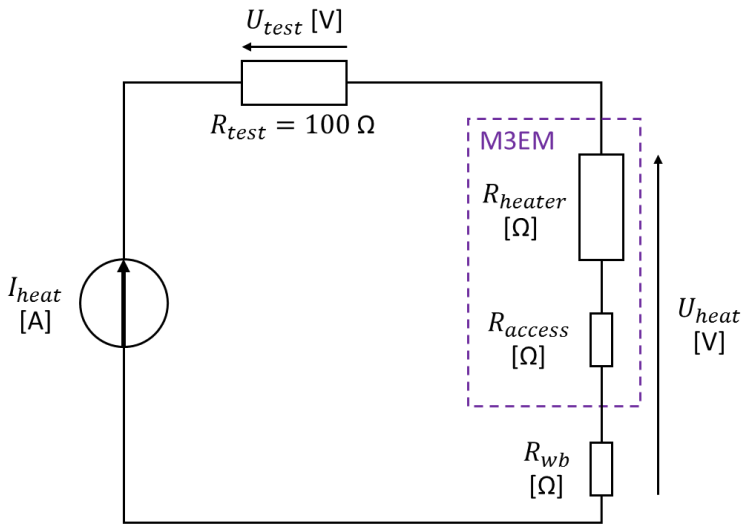

Figure 3.27: Power supply electrical circuit of the test chip M3EM.

Figure 3.27 is a schematic of the electronic circuit for the alimentation of the test chip. R_{heater}, R_{access} and R_{wb} are the electrical resistances of the small right heater, the access lines to the heater (in the *Metal Bottom* level of M3EM chip) and the electrical resistance of the wire bonding, respectively. The electrical resistance of the wire bonding is equal to

$$R_{wb} = \frac{4L_{wb}}{\sigma_{wb}\pi\phi_{wb}}, \tag{3.17}$$

where L_{wb} is the length of the wire bonding and σ_{wb} is the electrical conductivity of the wire. σ_{wb} being equal to 37.7 MS.m^{-1} for the aluminum [23] and L_{wb} being equal to 7.5 mm approximately, the resistance of the wire bonding R_{wb} is equal to 0.41 Ω which is negligible in comparison with R_{heater} (equal to 100 Ω approximately). In addition, the electrical resistance of the access lines can also be neglected in comparison with R_{heater}. Indeed, the width of the access line is much wider than the heater wire and the length of the access line is much shorter than the length of the heater wire (see Figure 3.4). The electrical resistance R_{access} is therefore negligible in comparison with R_{heater}. The M3EM chip is put in series with a test resistance R_{test}. The power generated by the heater element P_{heat} can therefore be estimated as follows:

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$$U_{test} = R_{test} I_{heat}, \tag{3.18}$$

$$P_{heater} \approx U_{heat} I_{heat}. \tag{3.19}$$

III.2. Characterization by means of Infrared thermometry

In this section, the temperature of the M3EM chip will be determined with the Infrared (IR) thermometry technique. First, the principle of IR thermometry will be explained. Then, the emissivity of the M3EM structure will be calibrated experimentally. This calibration will be compared to analytical calculations. Finally, the temperature measurements acquired on M3EM will be analyzed.

III.2.A. The IR thermometry technique

In order to describe to IR thermometry technique, the principle of the IR thermometry will be explained and the experimental setup (THEMOS-1000) will be detailed.

III.2.A.a. Principle of IR thermometry

Energy is emitted by all objects having a temperature greater than absolute zero. The intensity of the energy emitted by the object depends on different parameters (see Figure 3.28):

Temperature: The energy radiated increases as the object becomes hotter, permitting measurement of temperature by measurement of the emitted energy, particularly the radiation in the infrared portion of the spectrum of emitted radiation.

Wavelength: The intensity of radiated energy depends on the wavelength, based on Planck's law [24].

Emissivity: Emissivity is defined as the ratio of the energy radiated by an object at a given temperature to the energy emitted by a perfect blackbody at the same temperature. The emissivity of a blackbody is equal to 1. All values of emissivity are between 0 and 1 and are a function of the wavelength.

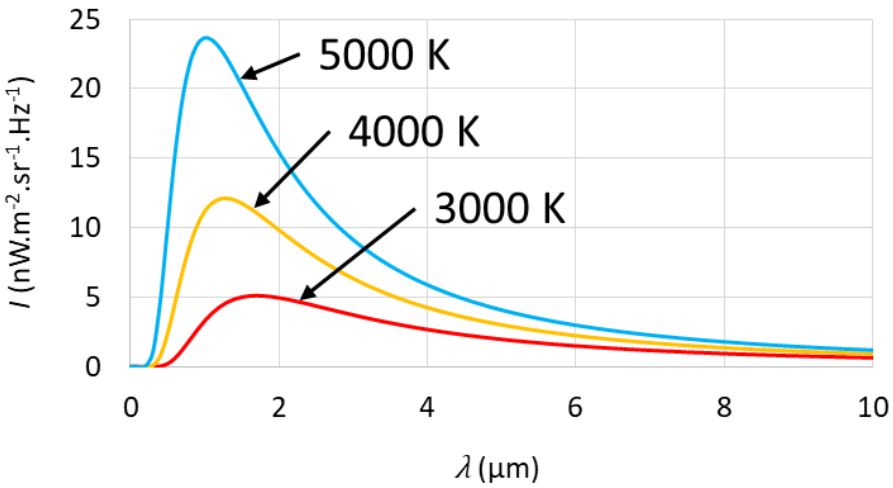

Figure 3.28: Spectral radiance I calculated with Planck's law for a blackbody emission as a function of the temperature and the wavelength λ.

III.2.A.b. THEMOS-1000 setup

Magnification	Numerical aperture	Working distance
0.8	0.13	22 mm
4	0.52	25 mm
15	0.71	15 mm

Table 3.4: Specifications of the three different IR lenses.

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The THEMOS-1000 is an IR thermometry device developed by HAMAMATSU. Figure 3.29 details the setup. The InSb detector allows measurements in the infrared spectral range with wavelengths from 3.7 to 5.2 µm. The intensity of the radiated energy is measured by the InSb camera via dedicated optics. Three different IR lenses are available. Their properties are summarized in Table 3.4. In order to interpret correctly the measurement of the intensity of the emitted energy as a function of temperature, the emissivity of the sample has to be determined over the entire spectral range of the InSb camera.

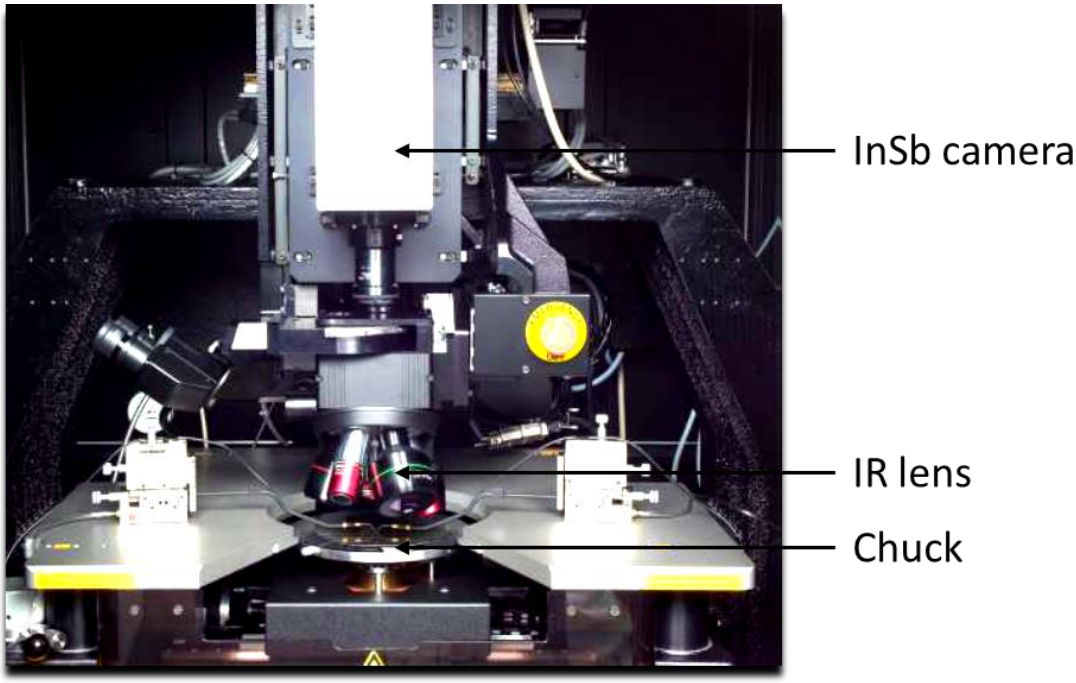

Figure 3.29: Picture of the IR thermometer THEMOS-1000.

III.2.B. IR thermometry measurements

In this section, the emissivity of M3EM will be measured experimentally. This measurement, realized on the THEMOS, will be used to determine the surface temperature of the chip.

III.2.B.a. Emissivity measurement

The emissivity measurement applied on M3EM chip is detailed. First, the calibration procedure of the THEMOS-1000 device is explained.

<u>Emissivity calibration:</u>

The principle of the calibration is explained in Figure 3.30. Q_e and Q_{bb} are the energies from the environment and the black body, respectively. T_s is the temperature of the sample which is controlled by a hot plate under the sample holder. The energy collected by the InSb camera Q_{InSb} for a sample heated at temperature T_s is equal to

$$Q_{InSb}[T_s] = \varepsilon Q_{bb}[T_s] + (1-\varepsilon)Q_e. \tag{3.20}$$

In order to characterize the emissivity of the chip, the energy collected by the InSb camera is measured at two different temperatures T_{s1} and T_{s2}. The collected energy is equal to

$$Q_{InSb}[T_{s1}] = \varepsilon Q_{bb}[T_{s1}] + (1-\varepsilon)Q_e, \tag{3.21}$$

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$$Q_{InSb}[T_{s2}] = \varepsilon Q_{bb}[T_{s2}] + (1-\varepsilon)Q_e. \tag{3.22}$$

The emissivity of the sample ε is therefore calculated as follows:

$$\varepsilon = \frac{Q_{InSb}[T_{s2}] - Q_{InSb}[T_{s1}]}{Q_{bb}[T_{S2}] - Q_{bb}[T_{S1}]}. \tag{3.23}$$

It is implicitly assumed that ε does not depends on temperature in the range $[T_{s1}, T_{s2}]$.

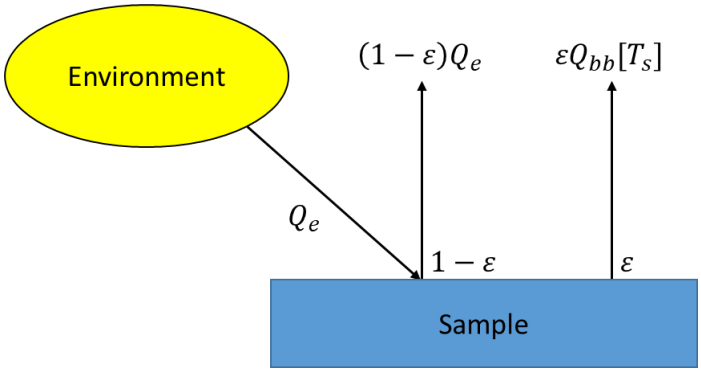

Figure 3.30: Principle of the emissivity calibration with IR thermometry.

<u>Emissivity measurement:</u>

The collected energy Q_{InSb} is measured experimentally at two different temperatures T_{s1} and T_{s2}, 30 °C and 80 °C respectively, with the 0.8 lens magnification. A thermocouple is used to probe the sample temperature. The emissivity calibration is shown in Figure 3.31. One can see that the emissivity of the M3EM chip ε_{M3EM} is equal to 0.45 approximately over almost all surface of the chip. This allows to consider that the emissivity is well determined by this calibration procedure. The silicon top die being transparent to IR in the range 3.7-5.2 µm, the *Metal Top* level is being imaged. However, in some places where the metal density is not homogeneous (white lines in Figure 3.31), the emissivity changes sharply. The EMA model used previously is no longer valid in this places. The temperature cannot be determined accurately at these locations by the IR setup.

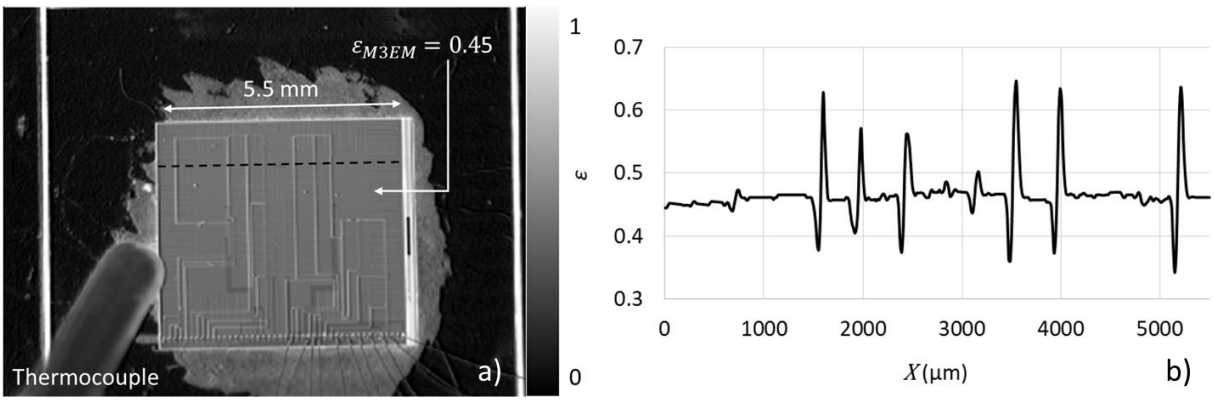

Figure 3.31: a) Emissivity measured with InSb camera on M3EM surface. b) Profile along dashed line.

III.2.B.b. Top die surface temperature

Figure 3.32 presents the IR thermometry measurement. The hotspot at the small right heater location is well highlighted. The maximum temperature rise at the center of the heater is measured to be 63 K approximately. Considering the imprecision of the measurement due to the metal density variation (dark lines on Figure 3.31), these results will be compared to a temperature mapping performed with Scanning Thermal Microscopy technique.

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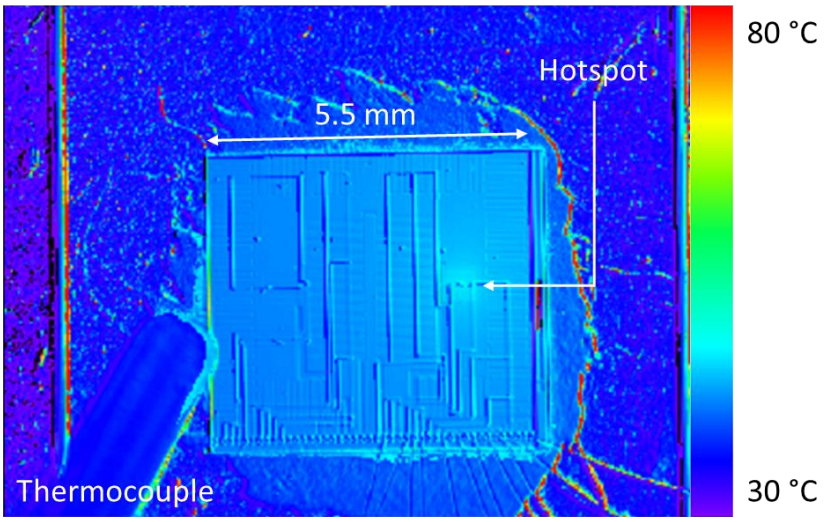

Figure 3.32: Temperature rise measured with IR thermometry on M3EM surface.

III.3. Thermometry by means of Scanning Thermal Microscopy

In order to measure the surface temperature of the chip with the SThM technique, the probe is used in temperature contrast mode (TCM). A low current in the probe is used to map the temperature at the surface of samples, which varies due to additional heat sources in the sample. The probe does not heat the sample. The same experimental setup is used in Chapter 2. However, in SThM, the temperature measured is the temperature of the probe and not the temperature of the surface. In order to interpret the experimental data as a function of the surface temperature, a thermometry coefficient relating the surface temperature and the probe temperature is calculated numerically for both the palladium nano-probe and the Wollaston micro-probe. Once done, temperature can be determined along a line on the surface of M3EM chip.

III.3.A. FEM modelling of thermometry coefficient

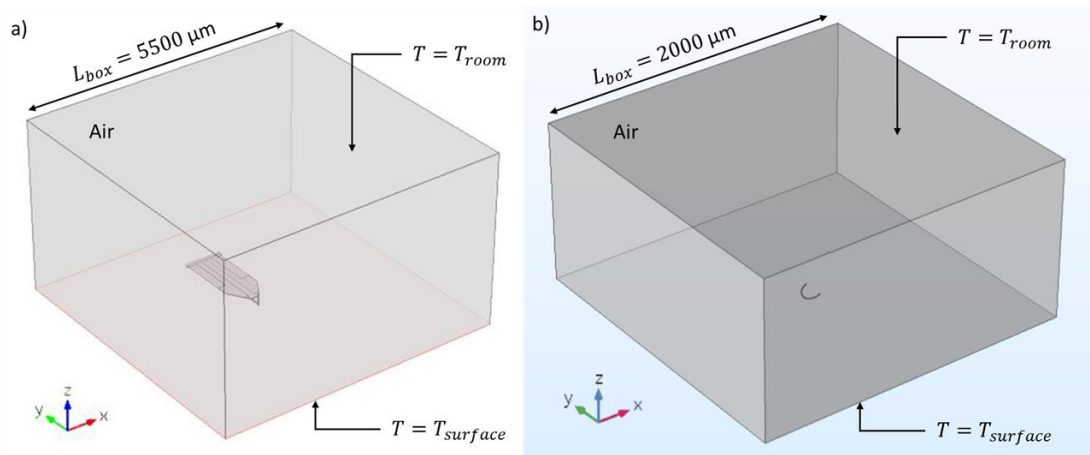

Figure 3.33: Thermometry coefficient determination by FEM modelling for a) palladium nano-probe and b) Wollaston micro-probe.

The thermometry coefficient C is defined as follows:

$$C = \frac{\Delta T_{probe}}{\Delta T_{surface}}, \tag{3.24}$$

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where ΔT_{probe} and $\Delta T_{surface}$ are the temperature rises of the probe electrical resistance and the surface in contact with the probe, respectively. The FEM models developed in Chapter 2 for the modelling of the tip-sample contact thermal transfer have been reused to determine numerically the thermometry coefficient of the palladium nano-probe and the Wollaston micro-probe. Figure 3.33 shows the modelling of the probe and the associated boundary conditions. In the same way, the heat losses though air and radiative transfer are represented by an air domain above the surface and surrounding the probe. In these models, the temperature of the surface set as a boundary condition, is considered constant. This assumption is particularly valid if the thermal gradient at the surface is small. It is well verified in the case of M3EM where the size of the small right heater (600 µm wide) is much larger than the size of the probe apex (<100 nm for the palladium nano-probe and ~5 µm for the Wollaston micro-probe). Conversely, for large thermal gradients, this assumption could be subject to further investigations. The thermometry coefficient C of the palladium nano-probe and the Wollaston micro-probe are calculated to be equal to 50.2±1.3% and 29.7±0.7%, respectively.

III.3.B. Temperature mapping with SThM

During the measurement of temperature with SThM, a low current is used to detect the variation of temperature of the probe. First, the sensitivity of both probes will be determined as a function of the injected current. Second, the procedure of measurement will be explained. Finally, the surface temperature will be deduced.

III.3.B.a. Sensitivity of the probes to the injected current

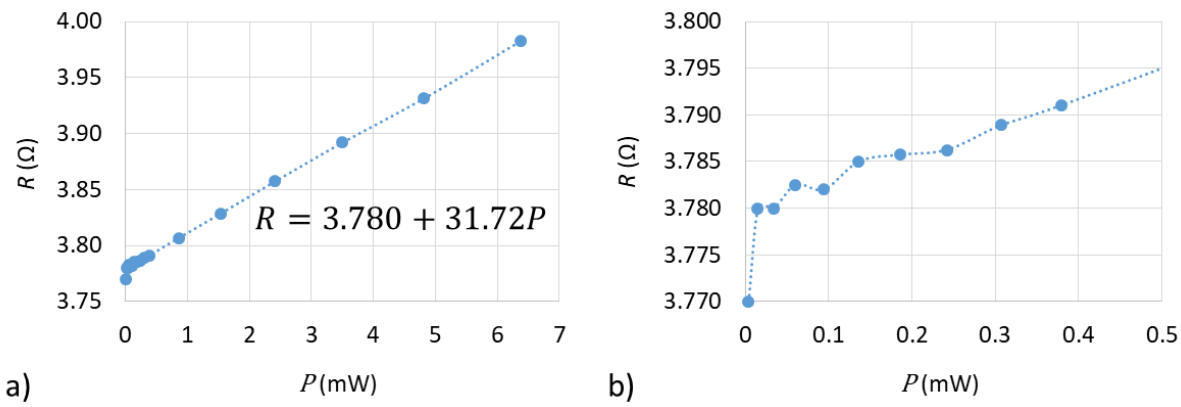

Figure 3.34: Variation of electrical resistance as a function of the injected Joule power for the Wollaston micro-probe for a) large electrical current and b) low electrical current.

In order to perform accurate temperature measurements, the probe needs to be supplied with an electric current I large enough for the temperature variations to be measurable. Figure 3.34 shows the sensitivity of the Wollaston probe electrical resistance R as a function of the injected Joule power P. One can see that the electrical resistance depends significantly on the Joule power only for power higher than 1 mW. In this case, the minimum current I_{min} can therefore be determined with:

$$I_{min} = \sqrt{\frac{P_{min}}{R}}, \tag{3.25}$$

where P_{min} is the minimum necessary Joule power and R is the electrical resistance of the probe. In the following studies, the injected current I will be taken slightly larger than I_{min} to stay clearly out of the noise. ΔT_{probe} is the temperature rise of the probe induced by the power supply. The data are summarized in Table 3.5.

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Probe	P_{min} (µW)	R_0 (Ω)	I_{min} (mA)	I (mA)	ΔT_{probe} (K)
Wollaston	1000	2	16	20	9.0
Palladium	10	100	0.18	0.2	1.6

Table 3.5: Sensitivity to the injected current for both palladium and Wollaston probes.

III.3.B.b. Procedure of temperature measurements

The points of temperature measurements on the surface of the chip are shown in Figure 3.35. The surface temperature rise measured at each point is therefore calculated as follows:

$$\Delta T_{surface} = \frac{R-R_0}{\alpha C R_0}, \tag{3.26}$$

where R_0 is the electrical resistance of the probe at room temperature, α is the TCR of the probe and C is the thermometry coefficient of the probe (calculated by FEM in Section III.3.A.). In the following section, the resistance of reference R_0 will be measured far from the contact, where the probe is not heated by the sample. The measurement of R_0 at the beginning and at the end of the experiment allows to detect a possible slow thermal drift or an unwanted contamination of the tip.

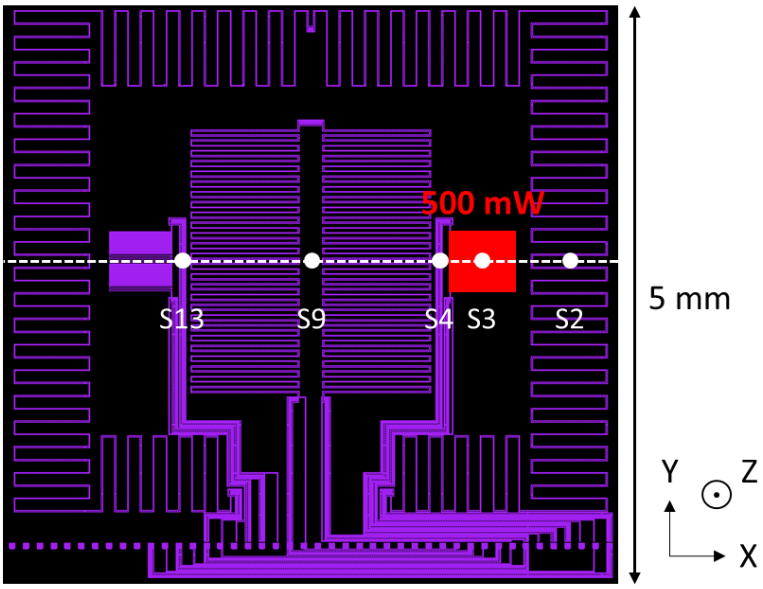

Figure 3.35: Position of the points of measurements on the M3EM chip.

III.3.B.c. Impact of the probe on the temperature field

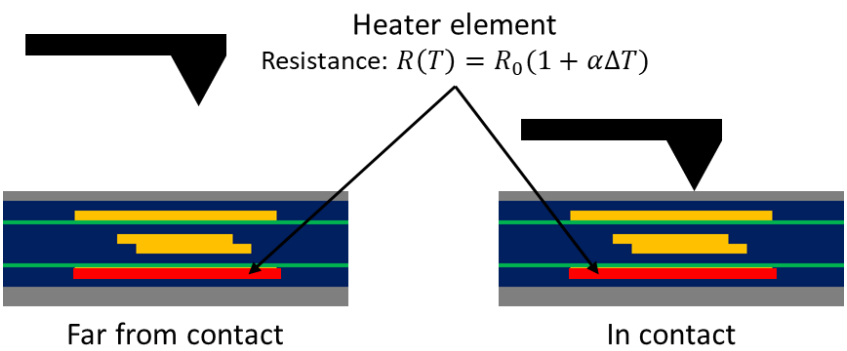

Figure 3.36: Characterization of the probe impact on the temperature field of M3EM.

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In this condition of use of the SThM technique, it is very important to know if the probe modifies the temperature field generated by the heater. In the case of a probe in contact with the chip, the probe acts as a heat sink on the top die surface. The temperature drop generated by the probe has to be quantified. The principle of the measurement is shown in Figure 3.36. In the case of M3EM, the resistance of the heater remains steady for both the palladium nano-probe and the Wollaston micro-probe. It means that the temperature of the heater does not decrease when the tip approaches the chip. The SThM technique is not invasive because the heat sink is negligible in comparison with the thermal conductance toward the chip holder. It has been proven by W. Zhao that this is not always the case, especially for very small active samples [25].

III.3.B.d. Conclusion on SThM temperature mapping

The comparison between the measurements of surface temperature in SThM for both the palladium probe and the Wollaston probe is shown in Figure 3.37. The uncertainty on the $\Delta T_{surface}$ measurement is due to the uncertainty on the measurement of the electrical resistance R_0. Here, the value of R_0 is taken equal to 2±0.3 and 100±10 Ω for the palladium nano-probe and the Wollaston micro-probe, respectively. Indeed, R_0 is associated to the active part of the probe which is smaller than the electrical resistance of the probe. R_0 is difficult to determine because:

(i) the exact length and diameter of the platinum wire for the Wollaston micro-probe is hard to measure by optical microscopy;

(ii) the geometry of the palladium resistance at the tip apex of the palladium nano-probe varies according to the probe.

However, one can see that the temperature variations measured in SThM are similar for both the palladium nano-probe and the Wollaston micro-probe. In this condition of use, the SThM technique can provide a temperature mapping over centimetric distances with a precision up to 3 K. It is important to mention that in the case of SThM with the palladium nano-probe, measurements on large temperature surfaces are time consuming (a few hours). The thermomechanical strain on the tip are such that it bends. The tip-sample contact is then difficult to maintain during the all procedure.

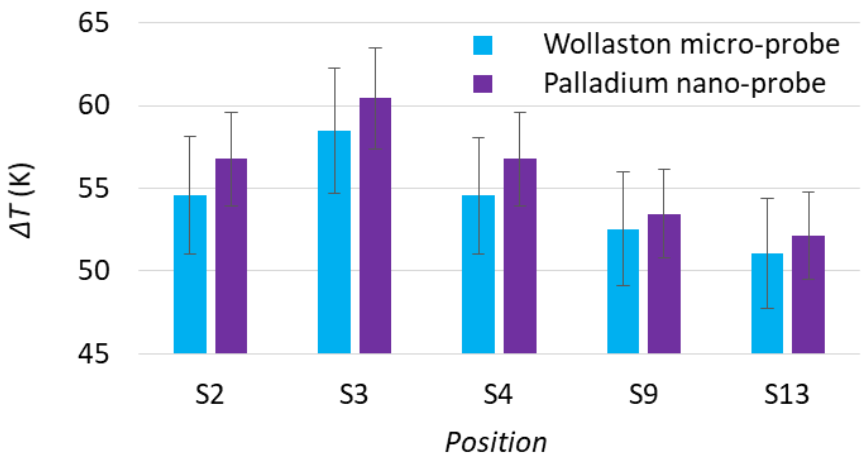

Figure 3.37: SThM surface temperature mapping with palladium and Wollaston probes.

IV. Discussion

Here, the experimental results and the numerical modelling of the chip heat dissipation is compared first. Then, the relevance and the accuracy of the FEM model is interpreted. Finally, the influence of different parameters is estimated numerically and experimentally.

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IV.1. Comparison between modelling and experimental data

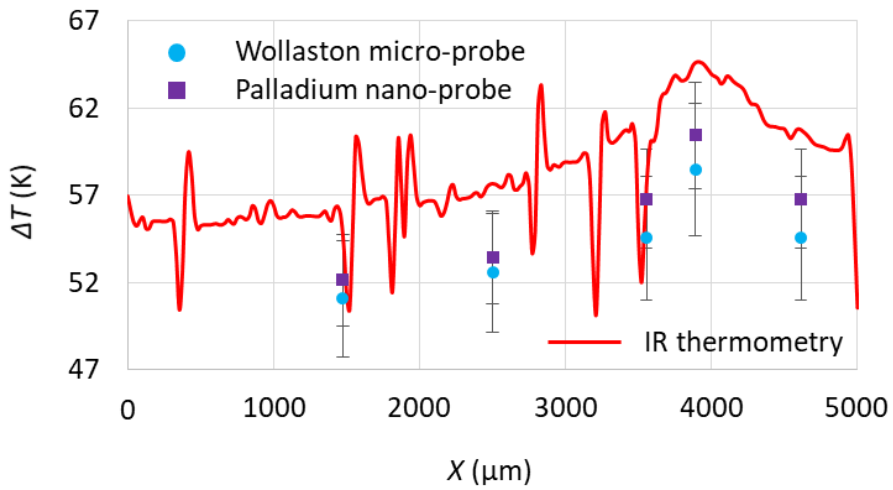

Figure 3.38: Surface temperature rise for M3EM measured by SThM and IR thermometry.

The surface temperature rise $\Delta T_{surface}$ measured with the SThM and the IR techniques are compared together in Figure 3.38. The data are acquired on the top die surface following the line in Figure 3.36. Here, the value of the electrical resistance R_0 is taken equal to 2 and 100 Ω for the palladium nano-probe and the Wollaston micro-probe, respectively. The IR measurement reveals additional peaks which are artifacts due to the high metal density close to the copper lines of the metal levels. Although the temperatures measured are different with each technique, the temperature profile seem to be similar. In order to match the SThM and the IR measurements, the value of R_0 is fitted equal to 1.8 and 93 Ω for the Wollaston and the palladium probe, respectively. In addition, the IR profile has been filtered to remove the peaks. The SThM and IR measurements (filtered by moving average) are compared to the FEM modelling in Figure 3.39. We can see that the FEM model and the experimental measurement are in very good agreement together. This model will be used later to analyze the influence of different physical parameter on heat dissipation in the case of the M3EM test chip.

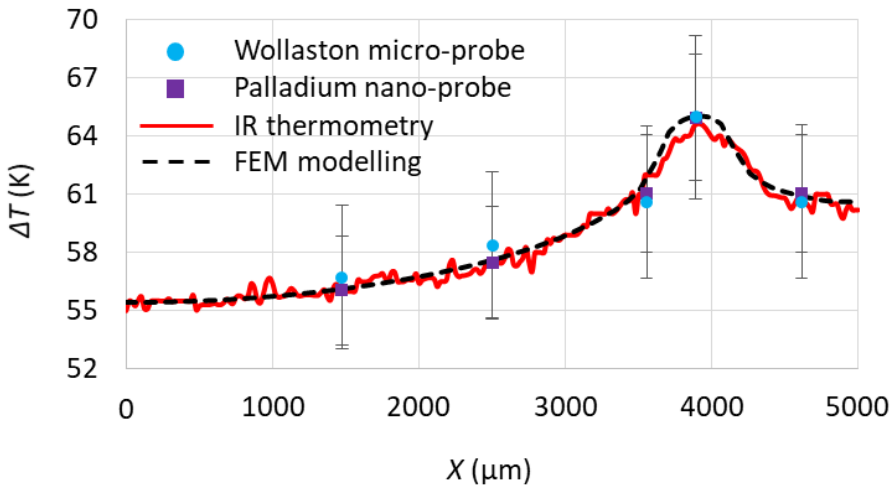

Figure 3.39: Temperature rise calculated in FEM and measured with SThM and IR thermometry.

IV.2. Influence of various experimental parameters

The influence of different physical parameters is determined numerically. First, the radiative heat transfer is considered in the FEM model. Then, the impact of the thermal boundary conductances (TBCs) between layers is quantified. Finally, different BEOL homogenization methods are compared.

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IV.2.A. Radiative heat transfer

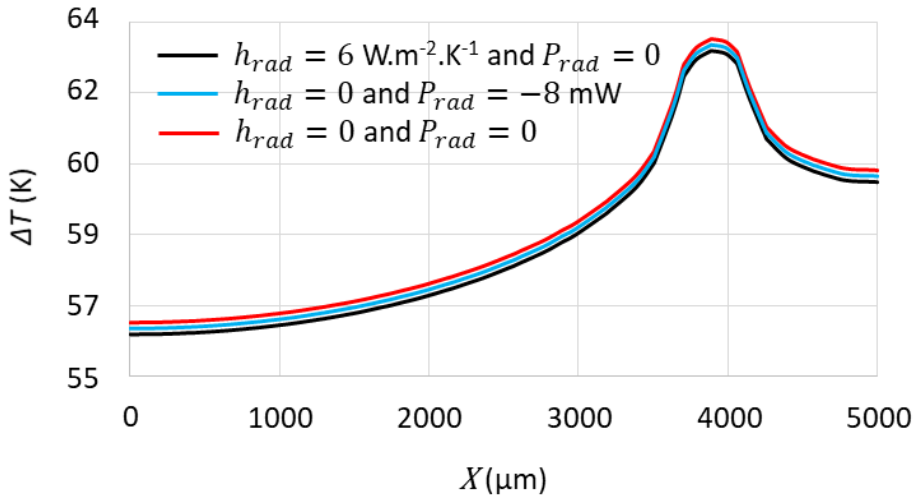

Figure 3.40: Effect of radiative heat transfer. Modelling by a TBC h_{rad} and a heat sink P_{rad}.

It is noticeable that with this FEM model, the hotspot is well characterized numerically. However, the radiative heat transfer has been neglected until now. In order to consider the radiative heat losses, especially during the calibration of g_{sink} under vacuum, an additional thermal boundary conductance h_{rad} is added all over the top surface of the chip. h_{rad} is calculated as follows at the first order:

$$h_{rad} = 4\sigma\varepsilon_{M3EM}T_{room}^3, \tag{3.27}$$

where T_{room} is the room temperature taken equal to 300 K. ε_{M3EM} is the emissivity of the chip between 0 and 1 and σ is the Stefan-Boltzmann constant equal to 56.7 nW.m^{-2}.K^{-4}. In this condition, h_{rad} is between 0 and 6 W.m^{-2}.K^{-1}. Considering the radiative heat losses h_{rad} equal to 6 W.m^{-2}.K^{-1}, g_{sink} is therefore determined to fit the temperature rises of the heater (in vacuum and air). g_{sink} is found equal to 354 W.m^{-2}.K^{-1} (instead of 360 W.m^{-2}.K^{-1}). The heat flux distribution is summarized in Table 3.6 with and without taking into account the radiative heat transfer. It is important to notice that the radiative heat losses have been modelled by a surface boundary condition even if the chip is emitting energy on its entire volume. Figure 3.40 shows that radiative losses can be modelled in the same way by a thermal boundary conductance h_{rad} and a heat sink P_{rad} in the BEOL with P_{rad} calculated as follows:

$$P_{rad} = -h_{rad}S_{chip}\Delta T_{BEOL}, \tag{3.28}$$

where S_{chip} is the surface of the chip in the xy plane and ΔT_{BEOL} is the average temperature rise of the BEOL. $P_{rad} = -8$ mW for an emissivity of the chip equal to 1. The radiative heat losses have therefore no influence on the temperature field of the chip. In the future, the radiative heat losses coefficient h_{rad} will be included in the fit parameter g_{sink}.

Heat path	h_{rad} = 0 W.m^{-2}.K^{-1}		h_{rad} = 6 W.m^{-2}.K^{-1}	
	mW	%	mW	%
Total	500	100	500	100
Sink	483	96.6	475	95.0
Air	13.6	2.7	13.6	2.7
Wire bonding	3.4	0.7	3.4	0.7
Radiation	0	0	8.0	1.6

Table 3.6: Summary of the heat flux distribution.

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IV.2.B. Thermal boundary conductances

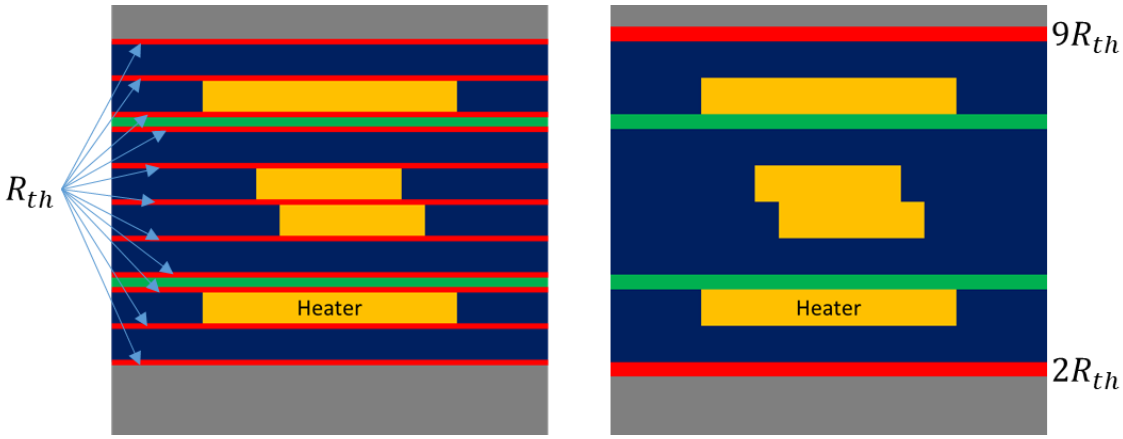

Figure 3.41: Schematic of M3EM cross section with a) location of the TBRs in the stack and b) equivalent FEM modelling with boundary conditions.

In fact, the stack of layers of ICs consists of a multitude of interfaces. These interfaces, thermally resistive, have been neglected previously in the calculation of the effective thermal conductivity of the BEOL (see Section II.2.A.). Here, the influence of the TBRs will be evaluated in the case of the M3EM chip. The TBR R_{th} is usually of the order of 2.10^{-8} K.m².W^{-1} between oxides and nitrides [14]. In order to take into account the TBRs in the FEM modelling, additional thermal boundary conditions have been added on the top and on the bottom surface of the BEOL. A schematic of the boundary conditions is shown in Figure 3.41. It is important to notice that the TBRs can be represented by two different boundary conditions because the heat flux has been proven to be mainly oriented in the z direction. The influence of the TBR R_{th} is shown in Figure 3.42. The parametric study performed on R_{th} allows to demonstrate that the temperature rise generated by the TBRs is equal to 70 mK in our study case where R_{th} is equal to 2.10^{-8} K.m².W^{-1}. It is good to note that even for a higher value of R_{th} equal to 2.10^{-7} K.m².W^{-1}, the temperature rise due to the TBRs remains lower than 700 mK. In the next parts, it will be coherent to neglect the effect of the TBRs on heat dissipation.

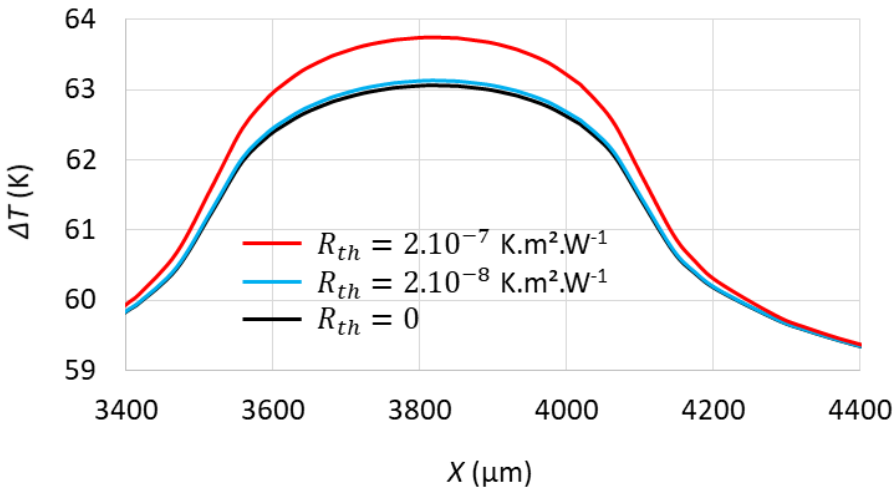

Figure 3.42: Influence of the TBR R_{th} on the temperature field calculated in FEM.

IV.2.C. BEOL homogenization method

In this section, the impact of the homogenization method will be quantified. Three different EMA models are described in Section II.1.B. In the case of M3EM, the volume fraction of copper x is equal

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to 19.6%, the thermal conductivity of the matrix k_m and of the copper k_c are equal to 1.3 and 330 W.m^{-1}.K^{-1} [13, 14] , respectively. The effective thermal conductivity k_{eff} of the BEOL is determined following Eq. (3.1) and Eq. (3.2). k_{eff} is found equal to 3.1 and 2.2 W.m^{-1}.K^{-1} with Maxwell-Garnett and Maxwel-Bruggeman EMA models, respectively. The values of thermal conductivity k_x, k_y and k_z homogenized in the directions x, y and z are summarized in Table 3.7.

EMA model	k_x (W.m^{-1}.K^{-1})	k_y (W.m^{-1}.K^{-1})	k_z (W.m^{-1}.K^{-1})
Parallel and series	2.6	2.6	2.0
Maxwell-Bruggeman	3.1	3.1	3.1
Maxwell-Garnett	2.2	2.2	2.2

Table 3.7: Homogenized thermal conductivity for different EMA models.

Figure 3.43 shows the influence of the EMA model. We can see that whatever the EMA method chosen, the temperature rises are close, especially for the parallel and series conductances and the Maxwell-Garnett models. Furthermore, the temperature difference between the Maxwell-Bruggeman and the Maxwell-Garnett models is lower than 200 mK which can be easily neglected. In the following parts, the parallel and series conductances model will be used because it is more convenient to apply in the case of BEOL with a matrix composed of several different dielectric materials. It is important to mention that the TBRs R_{th} and the effective thermal conductivity k_{eff} of the BEOL have almost no impact on heat dissipation which is mostly driven by the boundary conductances g_{sink}, h_{rad} and h_{air}.

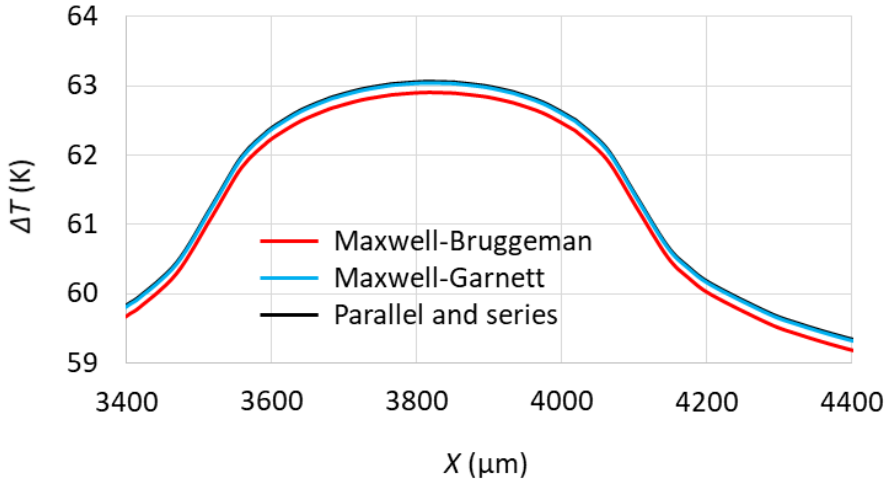

Figure 3.43: Influence of the EMA model on the temperature field calculated in FEM.

V. Conclusion

The aim was to develop a numerical model for the evaluation of the self-heating phenomena in 3D hybrid bonding architectures. To do so, the test chip M3EM has been chosen. This chip and its structure have been detailed. M3EM being a passive device, copper serpentine have been used to generate heat and represent the equivalent FEOL power generation in a commercial chip.

The FEM modelling strategy has been chosen. In order to overcome the constraints of finite element number, the thermal conductivity of the BEOL structure has been homogenized. To do so, different EMA models have been considered:

(i) parallel and series;

(ii) Maxwell-Garnett;

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(iii) Maxwell-Bruggeman.

The parallel and series thermal conductance models proved to be consistent and convenient for the modelling of the M3EM BEOL. In order to validate the FEM model, the numerical data have been compared to experimental measurements directly operated on M3EM top surface. To do so, two techniques were chosen: Scanning Thermal Microscopy and Infrared thermometry.

To measure the temperature of the chip activated in real time inside the measuring instruments, M3EM has been connected to a homemade electronic test bench. A PCB holder was developed at CETHIL to fit dimensional constraints. Using this setup, the temperature measurements were realized with SThM (palladium and Wollaston probes) and with IR thermometry (THEMOS). The temperature measurements performed with SThM and IR thermometry were in good agreement together. The numerical FEM model of the M3EM 3D HB test chip has been developed and calibrated experimentally. This model allowed to obtain the temperature field in the chip volume and over the chip surface. In the case of M3EM, it has been shown that:

(i) Heat dissipation does not depend from the EMA method used for the homogenization of the BEOL thermal conductivity.

(ii) Heat dissipation does not depend from the TBRs of the stack.

(iii) Heat dissipation is mainly driven by the surface boundary conditions (sink conductance and air losses).

Furthermore, the influence of the radiative heat losses has been added to the previous FEM model. To do so, a radiative heat transfer coefficient was calculated as a function of the chip emissivity. It has been shown that the radiative heat transfer is small and can be included in the calibration of the heat sink conductance.

In this chapter, a numerical model has been developed with FEM and calibrated with thermoresistive measurements. In the case of M3EM, the temperature calculations were validated with both SThM and IR thermometry measurements. In the future, this modelling method will be used for more complex architectures.

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VI. Bibliography

[1] R. Prieto et al., Thermal measurements on flip-chipped system-on-chip packages with heat spreader Integration, Proceeding of SEMI-THERM, 2015.

[2] T. Sakai et al., Hybrid bonding technology with Cu-Cu/adhesives for high density 2.5D/3D integration, Proceeding of PAN PACIFIC, 2016.

[3] K.N. Chen et al., Cu-Based Bonding Technology for 3D Integration Applications, Proceeding of 3DIC, 2011.

[4] C.T. Ko and K.N. Chen, Wafer-level bonding/stacking technology for 3D integration, Microelectronics Reliability, Volume 50, Pages 481-488, 2010.

[5] R. Prieto et al., Heat spreading packaging solutions for hybrid bonded 3D-ICs, Proceeding of 3DIC, 2016.

[6] J.P. Colonna et al., Carbon-based patterned heat spreaders for thermal mitigation of wire bonded packages, Proceeding of THERMINIC, 2017.

[7] K. Garg and V.S. Verma, Low Power Design Anaysis of PLL Components in Submicron Technology, Advances in Computing and Information Technology, Page 687-696, 2013.

[8] E.B. Rudnyi and J.G. Korvink, Model order reduction for large scale scale finite element engineering models, Proceeding of ECCOMAS, 2006.

[9] H. Köck et al., Electrothermal Multiscale Modeling and Simulation Concepts for Power Electronics, Journal of Power Electronics, Volume 31, Issue 4, Pages 3128-3140, 2016.

[10] J.C. Maxwell-Garnett and J. Larmor, Colours in metal glasses and in metallic films, Philisophical Transaction of the Royal Society of London, Page 385, 1904.

[11] S. Torquato, Thermal conductivity of disordered heterogeneous media from the microstructure, Reviews in Chemical Engineering, Volume 4, Page 151, 1987.

[12] K. Razeeb and E. Dalton, Advances in Nanocomposites – Synthesis, Characterization and Industrial Applications, InTech, Volume 1, 2011.

[13] H.A. Schafft et al., Thermal conductivity measurements of thin-film silicon dioxide, Proceeding of ICMTS, 1989.

[14] W. Jones and N.H. March, Theoretical Solid State Physics, Volume 1: Perfect Lattices in Equilibrium, 1973.

[15] S.M. Lee and D.G. Cahill, Heat transport in thin dielectric films, Journal of Applied Physics, Volume 81, Page 2590, 1997.

[16] F. Savar et al., PCB Glass-Fibre Laminates: Thermal Conductivity Measurements and Their Effect on Simulation, Journal of Electronic Materials, Volume 19, Issue 12, Pages 1345-1350, 1990.

[17] P. Nath and K.L. Chopra, Thermal conductivity of copper films, Thin Solid Films, Volume 20, Issue 1, Pages 53-62, 1974.

[18] C.Y. Ho et al., A Continuing Systematic Program on Data Tables of Thermophysical and Electronic Properties of Materials, TEPIAC, Volume 2, Page 145, 1979.

[19] J. Taine et al., A first course in heat transfer, Dunod, Page 288, 2011.

[20] P.C. Wang and R.G. Filippi, Electromigration threshold in copper interconnects, Applieds Physics Letters, Volume 78, Issue 23, Pages 3598-3600, 2001.

[21] J.R. Black, Electromigration – A brief Survey and Some Recent Results, Transaction of Electron Devices, Volume 16, Issue 4, Pages 338-347, 1969.

[22] S.R. Wilson et al., Handbook of multilevel metallization for integrated circuits, 1st Edition, Materials, technology and applications, Page 607, 1993.

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[23] P.D. Desai et al., Electrical Resistivity of Aluminum and Manganese, Physical and Chemical Reference Data, Volume 13, Issue 4, Pages 1131-1172, 1984.

[24] M. Planck, On the Law of Distribution of Energy in the Normal Spectrum, Annalen der Physik, Volume 4, Issue 3, Page 553, 1901.

[25] W. Zhao, Towards the Investigation of the Thermal Properties of Nano-cubes Deposited on a Membrane at High Temperature, Master thesis, INSA de Lyon, 2018.

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Chapter 4. Numerical and experimental investigations on 3D Hybrid Bonding imagers

In this chapter, the objective is to study the thermal behavior of a new type of technology: the 3D hybrid bonding imager (3D HB IMG). To do this, methods and approaches, validated in the previous chapter, will be applied on two different electronic chips. The first one, called FLAMINGO, is an analog test chip with an inactive pixel matrix. This chip was designed to validate the whole process and assembly flow in terms of mechanical reliability. The second one, called 93D, is a demonstrator with an active pixel matrix. Both chips were therefore designed for different objectives and thus, have different added-value in the frame of this work. In a first step, the structure of these two chips will be detailed. Then, the approach carried out on M3EM will be extended to FLAMINGO as well as to its matrix of pixels. Finally, the behavior of the pixel and its performances during a thermal loading will be investigated by means of the 93D device: the numerical and experimental results will then be discussed.

I. 3D hybrid bonding imagers for commercial applications

In this section, the structure of the FLAMINGO chips and the I140/I110 technologies are detailed in two parts. First, the structure of the BEOL is addressed and secondly the structure of the pixel is explained.

I.1. Structure of the interconnection levels

The entire stack of the 3D HB IMG consists of a total of three different parts as shown in Figure 4.1. In this section, each element is described:

(iii) top chip: I140/I110 technology;

(iv) hybrid bonding: copper/oxide interface;

(v) bottom chip: C40 technology.

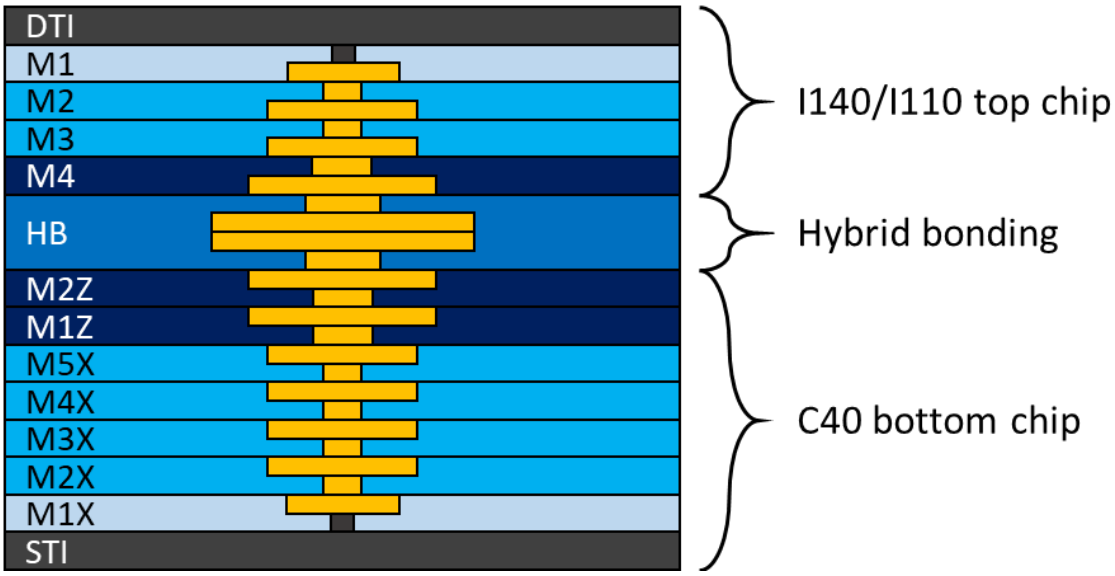

Figure 4.1: Schematic of the BEOL structure in the 3D hybrid bonding imager.

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I.1.A. C40 bottom chip

Since the FLAMINGO chip was designed to evaluate the robustness of the assembly, it is only composed by test structures such as crack detectors, stress sensors [1] and thermal sensors. These devices being quite small compared to the large die surface, up to 80%-90% of the surface has been filled with dummy structures. Moreover, the design complexity raises drastically when the pixels need to be electrically tested. Thus, due to the tight timeframe and objectives targeted, the pixel matrix was chosen as inactive. The pixel matrix is only processed to track possible delamination or cracks after thermal cycles and/or humidity storage. It allows also to monitor the thermal behavior, expected to be close to the final object (such as 93D for example).

Note that in the next sections, only the order of magnitude of dimensions are provided for confidentiality reasons. Figure 4.2 shows the geometry of the different metal levels: M1X, MiX and MiZ. It is important to note that in the same way as in the M3EM chip (Chapter 3), all the metal layers of the C40 chip have their copper fraction homogenized through copper dummies over the whole chip surface. The dummies are made of regular squares of copper with a side length of 0.9 µm and a pitch of 1.3 µm. Figure 4.3 shows the geometry of the shallow trench isolation (STI) level of the C40 bottom chip. This level allows the electrical isolation of each FEOL transistor from the other ones.

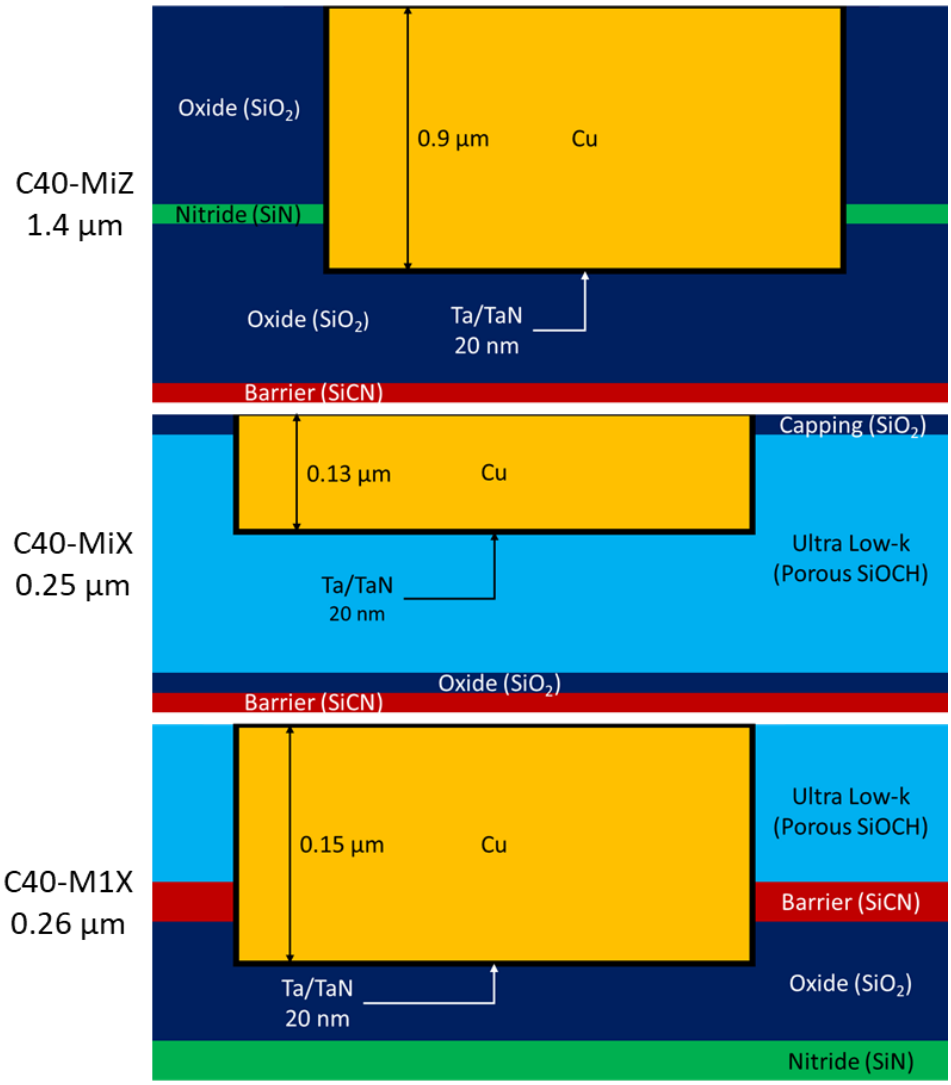

Figure 4.2: Characteristics of the different metal levels in the C40 bottom chip.

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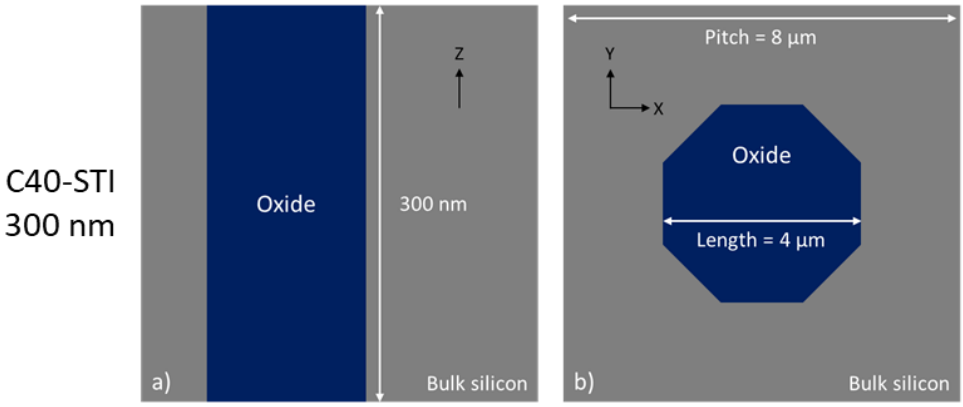

Figure 4.3: Schematic of the STI level in the C40 bottom.
a) Cross section of the STI level in the z direction. b) Floorplan of the STI in the xy plane.

I.1.B. Hybrid bonding

Figure 4.4 shows the geometry of the hybrid bonding level. As in the M3EM chip, the whole surface of the metal layer of the HB level consists of copper squares with a side length equal to 4.5 µm and a pitch equal to around 9 µm. The C40 and the I140/I110 chips are connected through copper vias but those being few (copper density under 5%), the associated metal density will be considered equal to zero. This assumption could be subject to discussion, especially close to the heating elements.

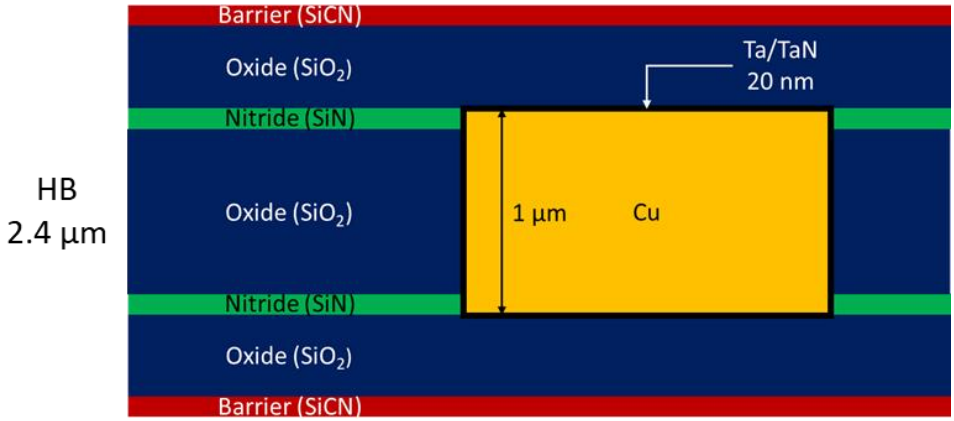

Figure 4.4: Characteristics of the hybrid bonding level for the 3D BSI.

I.1.C. I140/I110 top chip

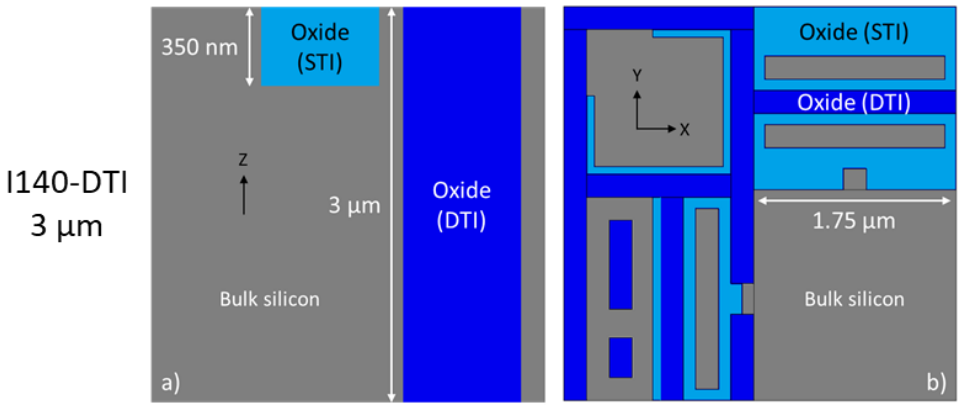

Figure 4.5: Schematic of the DTI level in the I140 top chip.
a) Cross section of the DTI level in the z direction. b) Floorplan of the DTI in the xy plane.

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Figure 4.5 shows the geometry of the deep trench isolation (DTI) level of the I140/I110 top chips. This level allows the electrical isolation of the photodiodes [2]. Figure 4.6 shows the geometry of the different metal levels: M1 to M4. As before, all the metal layers of the I140/I110 chips are filled with dummies: copper squares of 0.9 µm width and 1.3 µm of pitch.

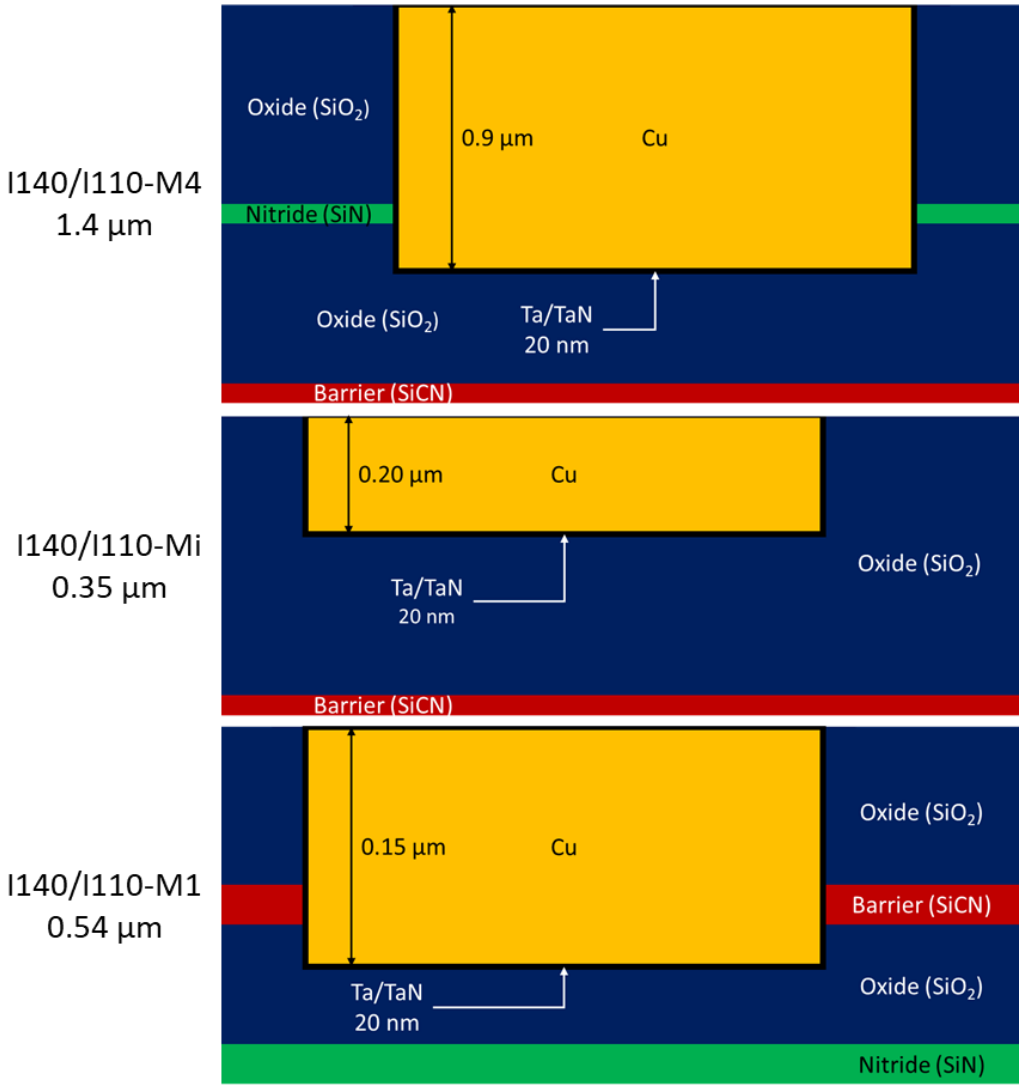

Figure 4.6: Characteristics of the different metal levels in the I140/I110 top chips.

I.2. Pixel characteristics

In this section, the multi-layer geometry of the pixel stack is detailed. Then the micro lenses on top of the I140 chip are characterized with both optical microscopy and atomic force microscopy (AFM).

I.2.A. Layers geometry

The structure of the pixel is described in Figure 4.7. Here, three different parts are highlighted from bottom to top:

(i) the multilayer structure where the photodiode (PPD) is patterned;

(ii) an optical filter RGB (red, green, blue);

(iii) the resin micro lens which concentrates the light on the PPD.

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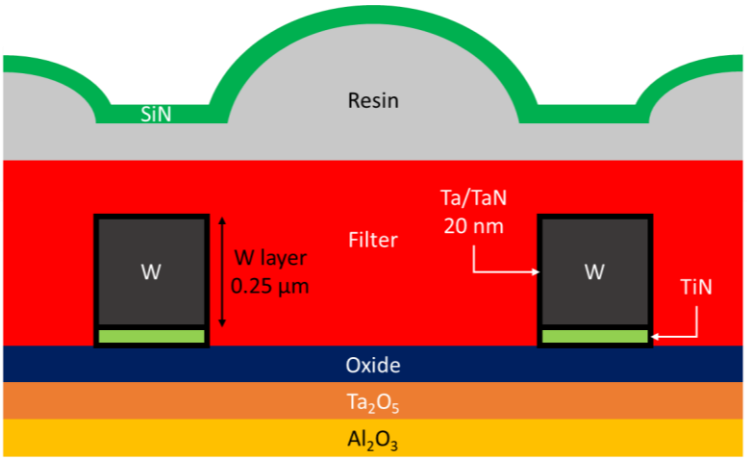

Figure 4.7: Cross section of the pixel structure for I140 top chip.

I.2.B. I140 micro lenses AFM characterization

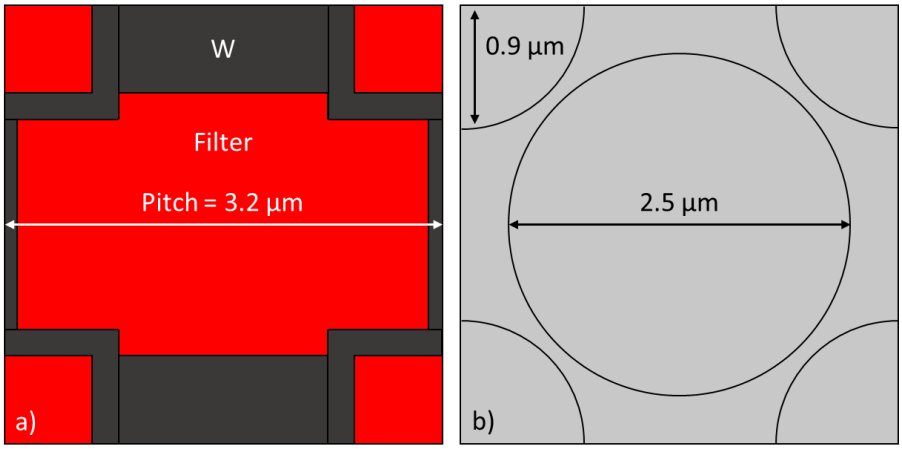

Figure 4.8: Top view of the I140 pixel geometry for a) tungsten layer and b) resin micro lenses.

Figure 4.8 shows the geometry of the tungsten layer and the micro lenses. This tungsten pattern avoids the crosstalk of photons between the photodiodes below each lens. This information gives the diameter of the lenses in the xy plane. However, the height of each micro lens remains to be determined. Indeed, after the deposition and the annealing of the resin, the geometry is not perfectly known. As a results, the surface topography of the imager is characterized experimentally by optical microscope and AFM. The results are presented in Figure 4.9. Optical microscopy allows to distinguish the big micro lenses with their associated color filters, contrarily to the small micro lenses which are more tricky to identify. Hence, additional measurement is realized with AFM nano-probe and a scanning resolution of 256x256 points over 20x20 µm². An AFM apex curvature radius of 10 nm is used for this study. Figure 4.9.b) depicts the results obtained for the small micro lens. This allows to measure the height of both small and big micro lenses which are equal to 0.6 and 1.2 µm, respectively.

The thermal conductivity of Al_2O_3, Ta_2O_5, SiO_2, SiN and TiN are taken equal to 0.90, 0.45, 1.3, 0.75 and 19 $W.m^{-1}.K^{-1}$ respectively [3-8]. The thermal conductivity of W is equal to 174 $W.m^{-1}.K^{-1}$ [9]. The resin thermal conductivity k_{resin} is taken equal to 0.34 $W.m^{-1}.K^{-1}$ [10]. The RGB filters [11] (as shown in Figure 4.9.a)), which consist of copper nanoparticles in an organic resist, can be seen as a homogeneous media with the Maxwell-Garnett EMA (Chapter 3 Section II.1.B). The thermal conductivity k_{Cu} is evaluated to 390 $W.m^{-1}.K^{-1}$ [12]. It has been shown by internal study at MATEIS laboratory (O. Merchiers) that the volumetric fraction of copper needs to be lower than 6% in order to

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filter the light at wavelengths of 460, 540 and 610 nm. The effective thermal conductivity of the filter k_{filter} is therefore estimated to be equal to 0.37±0.03 W.m^{-1}.K^{-1}. From EMA it can be shown that k_{filter} depends weakly on the TBC between the particles and the matrix because $k_{Cu}/k_{resin} \gg 1$.

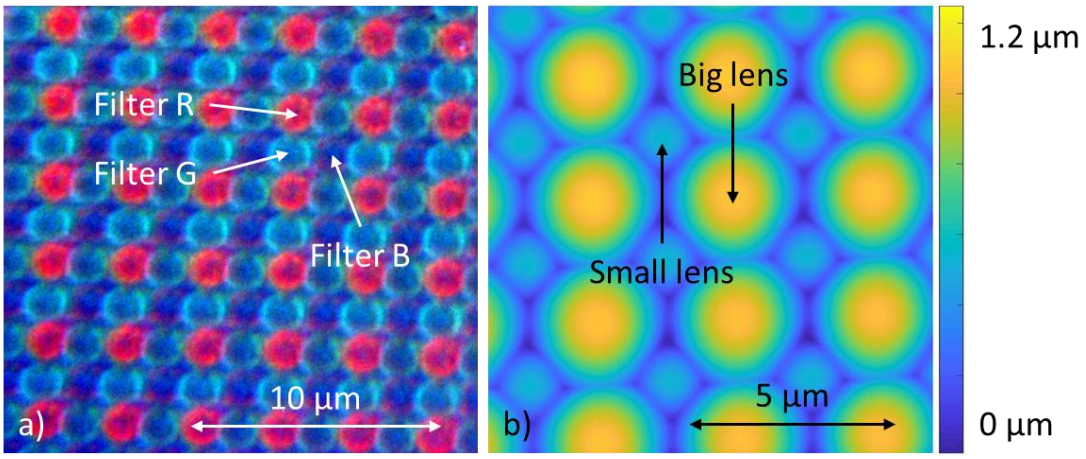

Figure 4.9: Surface characterization of the I140 imager in the xy plane.
a) Optical microscopy image of the pixel array. b) AFM topography of the pixel micro lenses.

II. Characterization at die and pixel levels: FLAMINGO test chip

In this section, the FLAMINGO 3D hybrid bonding test chip is studied. First, the dedicated embedded thermal structures are described. Then, the chip is modelled with the FEM numerical procedure developed on the M3EM test chip (Chapter 2). Additionally to the M3EM device, the thermal behavior of the pixel of the I140 chip is now studied. Finally, the numerical results are validated with the SThM measurements on the pixel matrix.

II.1. Characteristics of the embedded thermal structures

In FLAMINGO, different thermal structures are embedded in the BEOL. The specifications and the thermoresistive properties of these structures are now determined.

II.1.A. General specifications

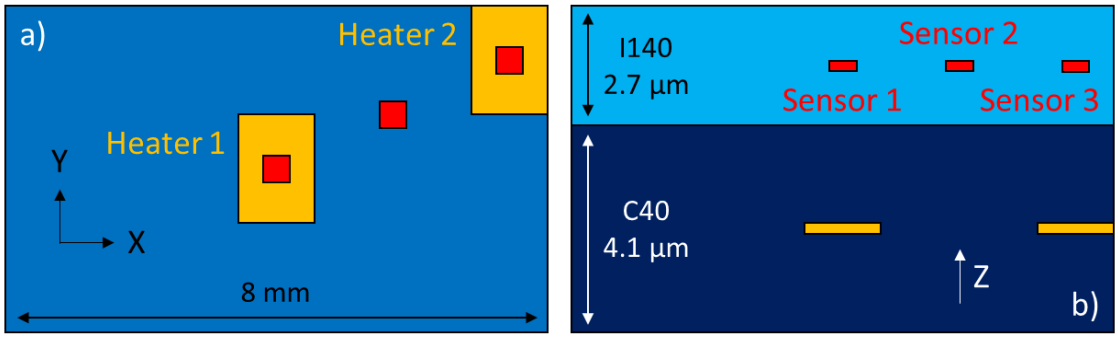

Figure 4.10: Positions of the embedded thermal structures in the FLAMINGO test chip.

Here, two different thermal structures were patterned in the M1 metal levels of chips C40 and I140, respectively. The former acts as heater while the latter aims to sense the temperature locally. Indeed, ICs (bottom die) are expected to heat up the stack (power management, image processing…). Thus the heater has been located close to the FEOL layer of C40. Besides, the objective is to evaluate the thermal impact on the pixel matrix. The sensor is hence located just beneath. The location of the metal

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serpentines is shown in Figure 4.10. The properties of the thermal structures are summarized in Table 4.1 Here, R_0 is the electrical resistance of the serpentine at room temperature.

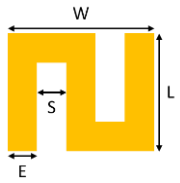
Structure	Data	Heater	Sensor
	E (µm)	4	0.09
	S (µm)	3.5	0.9
	L (µm)	140	5
	W (µm)	200	5
	R_0 (Ω)	160	80

Table 4.1: Properties of the thermal structures of FLAMINGO.

II.1.B. Serpentine TCR measurements

In order to allow future thermoresistive analysis with the equation

$$R(T) = R_0(1 + \alpha\Delta T), \tag{4.1}$$

where R is the electrical resistance of the serpentine, the TCR α of each heater and sensor needs to be characterized. To do so, the chip FLAMINGO is heated on a hot plate at different temperatures (measured with a thermocouple). The results are shown in Figure 4.11. The TCR of the heaters (M1) and the sensors (M1) are found to be equal to 0.321 and 0.316 %.K^{-1} respectively. Considering these values of TCR, the Joule heating associated with each thermal structure can be estimated as a function of the input power.

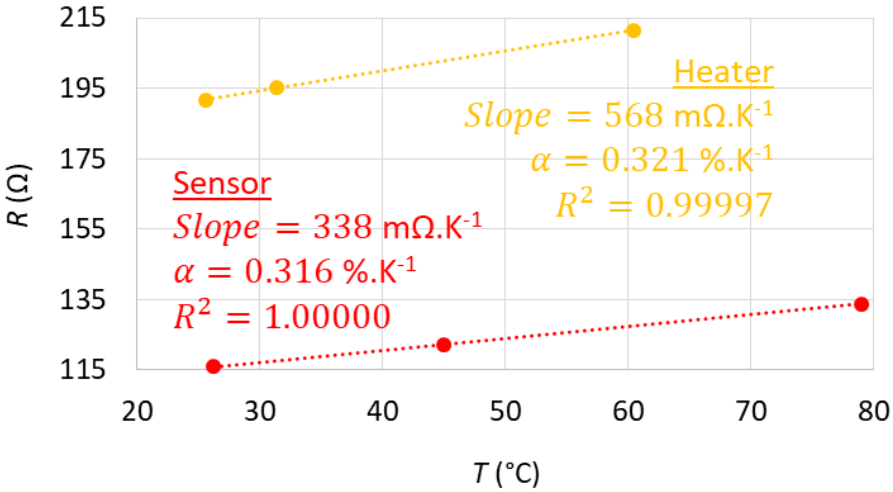


Figure 4.11: TCR measurement for the M1 levels of C40 and I140 chips respectively.

II.1.C. Joule heating of the thermal structures

For the heaters and the sensors, the resistance R of the heating element is measured as a function of the injected Joule power:

$$P = RI^2, \tag{4.2}$$

where I is the input current. Joule heating induces an elevation of temperature of the element, and consequently the power P and the resistance R are linearly dependent. Figure 4.12 shows the experimental results. It can be seen that for the heater, unlike in the case of the sensor, the temperature rise seems to be limited for injected Joule power larger than 200 mW. This is due to the presence of protective diodes at the pads which limit the current intensity in the BEOL interconnection levels of the C40 bottom chip (Electrostatic Discharge protection). Here, the maximum injected current

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is therefore limited to 45 mA. This induces constraints on the temperature rise that can be induced by the heater element. As far as the sensor is concerned, the BEOL interconnection levels of the I140 top chip does not seem to have any current limitations.

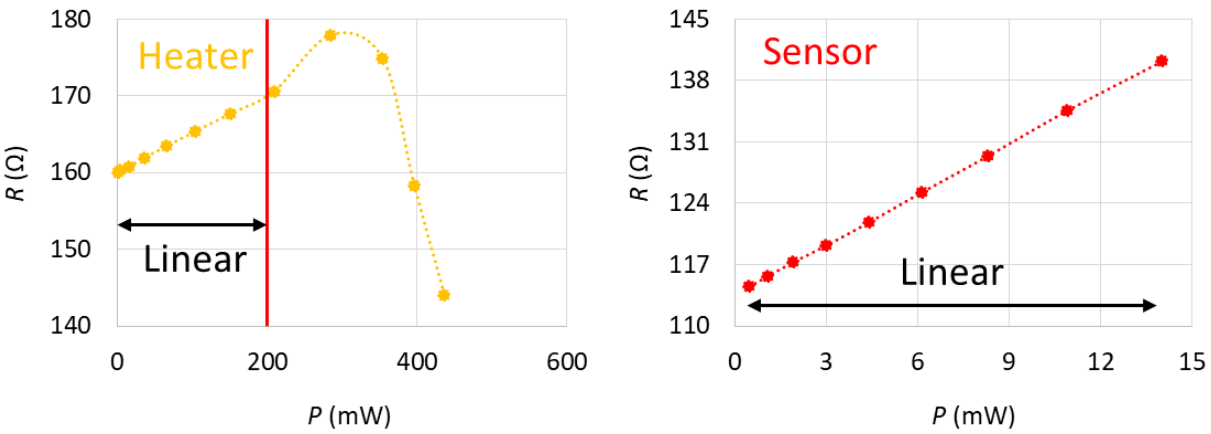

Figure 4.12: Resistance measured as a function of the injected Joule power for: a) heater in the C40 bottom chip and b) sensor in the I140 top chip.

II.2. Numerical modelling of FLAMINGO test chip

In this section, the FLAMINGO test chip is modelled by FEM. First, the BEOL is homogenized. Then, the pixel structure on top of the I140 chip is modelled and taken into account in the global FEM model of the chip and its environment. Finally, the numerical results are discussed.

II.2.A. Modelling of the BEOL for hybrid bonding ICs

The BEOL structure is homogenized with the parallel and series EMA as validated in Chapter 2. For this, the procedure involves two steps: the homogenization of each metal level and the homogenization of the global stack, successively performed.

II.2.A.a. Levels effective thermal conductivity

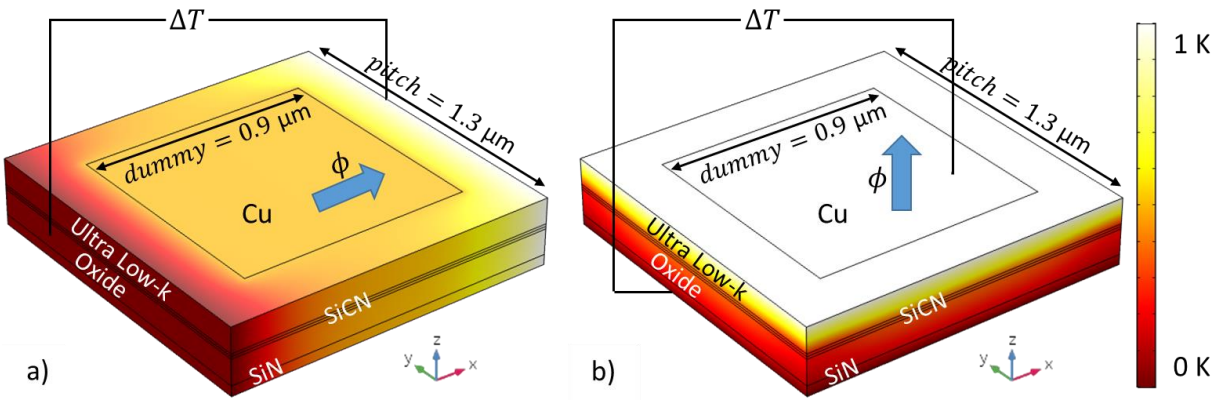

Figure 4.13: Temperature rise modeled by FEM for the homogenization of the M1X level with a) in-plane thermal and b) cross-plane conductivity homogenization.

To homogenize the thermal conductivity of each metal level, an FEM model has been developed. This model represents the unit cell of a metal level. This cell is made of one dummy and its surrounding layers. This FEM model is detailed in Figure 4.13 for the M1X level. A temperature difference ΔT is set as a boundary condition and the heat flux ϕ is calculated numerically. The effective thermal conductivity k is therefore determined as follows:

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$$k = \frac{\phi}{S}\frac{L}{\Delta T}, \tag{4.3}$$

where S is the surface of the domain perpendicular to the heat flux and L is the length of the domain parallel to the heat flux. Following [13-20], the thermal conductivities of the films of SiN, SiO_2, SiCN, Low-k and Ultra Low-k are taken equal to 0.85, 1.3, 0.6, 0.59 and 0.13 $W.m^{-1}.K^{-1}$, respectively. The uncertainties on these values are detailed in Chapter 2.

II.2.A.b. Summary of effective thermal conductivities for the various levels

The homogenized properties of the different layers k_x, k_y and k_z are summarized in Table 4.2 for the FLAMINGO chip in the three directions x, y and z. The impact of the thermal boundary conductance (TBC) is neglected here, since many layers already thermally-resistive are present in the structure. The volume fraction of copper v_{Cu} is also calculated for each level.

Level	Thickness	k_x	k_y	k_z	v_{Cu}
	µm	$W.m^{-1}.K^{-1}$	$W.m^{-1}.K^{-1}$	$W.m^{-1}.K^{-1}$	%
DTI	3.000	9.89	15.4	105	0.00
M1	0.560	2.49	2.49	1.55	7.19
M2	0.270	3.29	3.29	1.75	7.19
M3	0.420	3.28	3.28	2.05	11.5
M4	1.420	2.82	2.82	2.42	42.2
HB	2.440	2.10	2.10	1.53	30.0
M2Z	1.405	2.80	2.80	2.33	41.2
M1Z	1.405	2.80	2.80	2.33	41.2
M5X	0.250	0.83	0.83	0.31	6.23
M4X	0.250	0.83	0.83	0.31	6.23
M3X	0.250	0.83	0.83	0.31	6.23
M2X	0.250	0.83	0.83	0.31	6.23
M1X	0.260	1.90	1.90	2.67	7.19
STI	0.300	97.6	97.6	118	0.00

Table 4.2: Homogenized thermal conductivities for the levels of FLAMINGO test chip.

II.2.A.c. BEOL effective thermal conductivity

In the case of the BEOL homogenization, the same ordered structures as in M3EM (copper dummies) are present. Consequently, for the FLAMINGO test chip, the EMA strategy is based on the parallel and series thermal conductance model as well. Considering this model, it is possible to evaluate the global effective thermal conductivities of the entire stack K_x, K_y and K_z in the three directions x, y and z respectively as follows:

$$K_x.\sum E_i = \sum k_x^i.E_i, \tag{4.4}$$

$$K_y.\sum E_i = \sum k_y^i.E_i, \tag{4.5}$$

$$\sum \frac{E_i}{k_z^i} = \frac{\sum E_i}{K_z}, \tag{4.6}$$

where E_i is the thickness of each level respectively. The thermal conductivities K_x, K_y and K_z are found equal to 6.5, 7.8 and 1.7 $W.m^{-1}.K^{-1}$ respectively. Here, the total volume fraction of copper V_{Cu} can be calculated and is found to be equal to 17.0%. In the same way as for M3EM, the thermal conductivity in the z direction is low. This is mainly due to the presence of Ultra Low-k dielectric materials in the M2X to M5X metal levels of the C40 die. However, unlike M3EM, the FLAMINGO chip has higher

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thermal conductivity in the x and y directions. The in-plane heat spreading should be improved in comparison to M3EM.

II.2.B. Modelling of the pixel for 3D hybrid bonding imagers

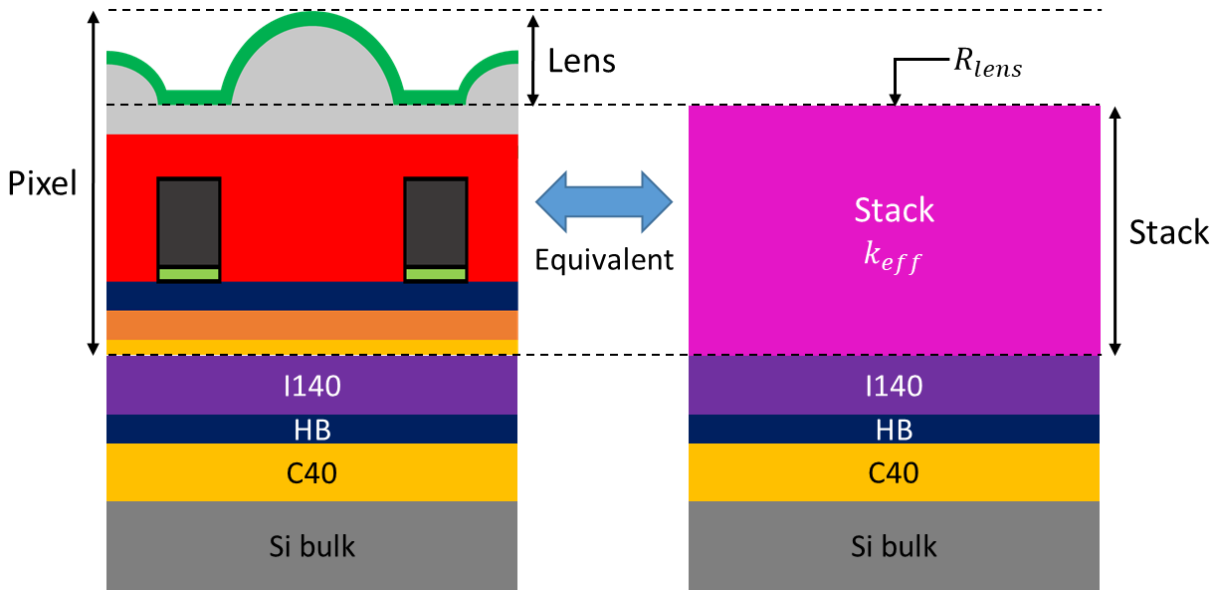

Figure 4.14: Principle of the simplification for the FEM modelling of the pixel imager. a) Full layered geometry of the pixel. b) Homogenized equivalent level.

In this section, the influence of the imager on the chip thermal behavior is taken into account numerically. To do this, the geometry of the pixel is divided in two parts: the thin layers stack and the micro lenses. First, the structure of the stack is homogenized to represent an equivalent level above the I140 top chip. Second, the micro lenses are modelled numerically and represented as an equivalent thermal boundary resistance. The principle of the numerical analysis is shown in Figure 4.14.

II.2.B.a. Homogenization of the pixel stack

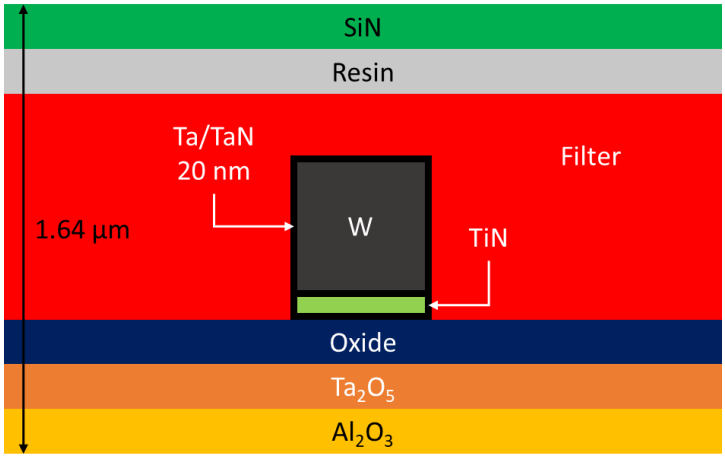

Figure 4.15: Cross section of the pixel stack without the micro lenses.

A schematic of the pixel stack without the micro lenses is shown in Figure 4.15. The pattern of the TiN/W layer can be found in Figure 4.8. The structure of the pixel being periodic in the xy directions over the imager surface, the effective thermal conductivity of the stack can be determined with the EMA method explained in Section II.2.A. for the BEOL. However, in the case of this stack, a wide range

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of thermal conductivities is used. The effective thermal conductivity must be estimated on a case-by-case basis for each direction. The equivalent level has a pitch equal to 3.2 µm and a thickness E_{stack} equal to 1.64 µm. A temperature difference $\Delta T = 1$ K is set as a boundary condition on the opposite faces of the domain in the three directions x, y and z. The heat flux density Q is then calculated numerically perpendicularly to the heat flux direction.

<u>x and y directions:</u>

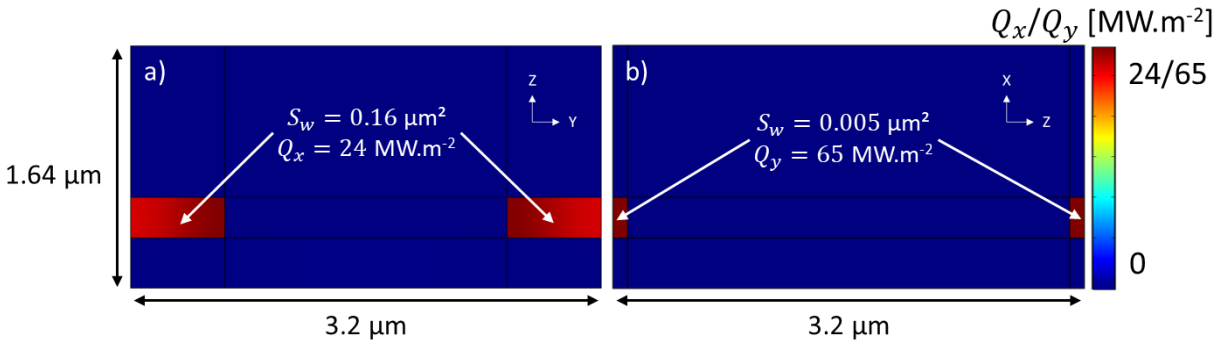

Figure 4.16: Heat flux distribution in the pixel stack along the directions x and y.

The heat flux densities Q_x and Q_y are shown in Figure 4.16 for the two directions x and y. It is noticeable that the heat flux is constrained in the tungsten lines (surface S_w) where the thermal conductivity is the higher. The in-plane effective thermal conductivities k_x and k_y are therefore calculated using the parallel EMA. k_x and k_y are found equal to 5.7 and 2.1 W.m^{-1}.K^{-1}, respectively.

<u>z direction:</u>

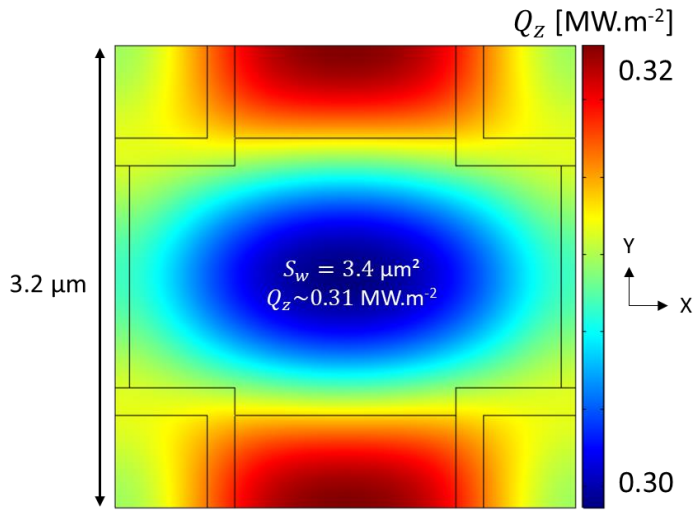

Figure 4.17: Heat flux distribution in tungsten level along the direction z.

The flux density q_z is shown in Figure 4.17 in the direction z. It is noticeable that the heat flux is almost homogeneous in the xy plane (Q_z~0.31±0.1 MW.m^{-2}). The cross-plane effective thermal conductivities k_z is therefore calculated using the series EMA. k_z is found equal to 0.51 W.m^{-1}.K^{-1}.

II.2.B.b. Micro lenses array thermal resistance

In order to determine the thermal resistance associated to the micro lenses, an FEM model of the pixel is developed considering the homogenized stack with the micro lens on top of it. The geometry of the pixel is shown in Figure 4.18.a). A thermal difference ΔT is set over the opposite surfaces of the domain

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in the in-plane and cross-plane directions. The flux distribution in the pixel is shown in Figure 4.18.b) and in Figure 4.18.c) in the in-plane and cross-plane directions, respectively.

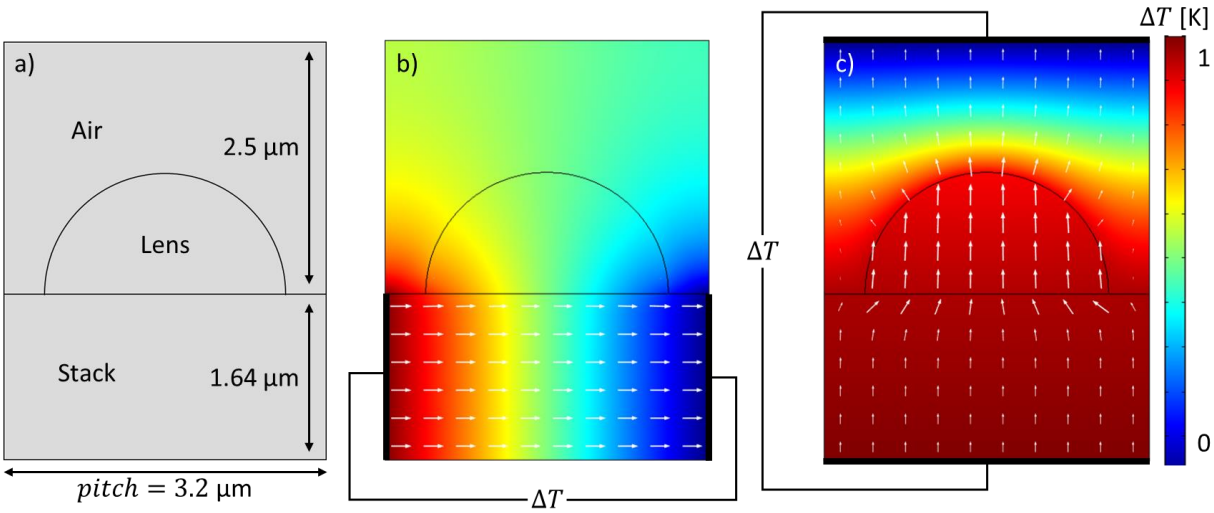

Figure 4.18: a) FEM model geometry of the pixel. Heat flux distribution in the pixel cross section with b) in-plane and c) cross-plane temperature differences.

<u>In-plane thermal resistance:</u>

Figure 4.18.b) shows that the heat flux (white arrows) is constrained in the stack of the pixel. No flux crosses the micro lens. The thermal resistance of the lens is considered equal to infinity in the in-plane directions. The thermal resistance of the lens is therefore modelled by a 1D interface resistance above the pixel stack in the z direction.

<u>Cross-plane thermal resistance:</u>

The thermal resistances of the stack and the micro lenses R_{stack} and R_{lens} in series. The resistance R_{lens} is deduced from the thermal resistance of the pixel R_{pixel} as follows:

$$R_{lens} = R_{pixel} - R_{stack}, \tag{4.7}$$

$$R_{stack} = \frac{E_{stack}}{k_z}. \tag{4.8}$$

A thermal difference ΔT is set over the top and bottom surfaces as shown in Figure 4.18.c). The resistance of the stack R_{stack} is found equal to 3.22 µK.m².W^{-1}. The heat flux density Q is calculated numerically and gives the thermal resistance of the pixel R_{pixel} with:

$$R_{pixel} = \frac{Q}{\Delta T}. \tag{4.9}$$

R_{pixel} is calculated equal to 78.6 µK.m².W^{-1}. The thermal resistance of the lens in the vertical direction is therefore equal to 75.4 µK.m².W^{-1}. It is important to mention that the flux lines have to be vertical in order to use Eq. (4.7). This is why an air domain is added above the pixel structure. Although R_{lens} takes into account of 2.5 µm of air resistance, this represents only 1‰ of the air boundary resistance δ/k_{air}, where δ is the thermal skin layer (~2.5 mm), and is negligible.

II.2.C. FEM modelling of the FLAMINGO chip

In this section, the modelling of FLAMINGO is specified. First, the geometry and the boundary conditions are detailed. Then, the model is calibrated with experimental thermoresistive measurements. It has been chosen to calibrate the simulation with this approach rather than with the

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SThM equipment. By doing so, the approach of the pixel modelling can be validated more easily. By calibrating with the SThM tool (i.e. scan of pixel top surface), the sensitivity to the pixel properties would be exerted and then, may be hidden by the calibration step.

II.2.C.a. Geometry and boundary conditions

Chip-on-PCB modelling:

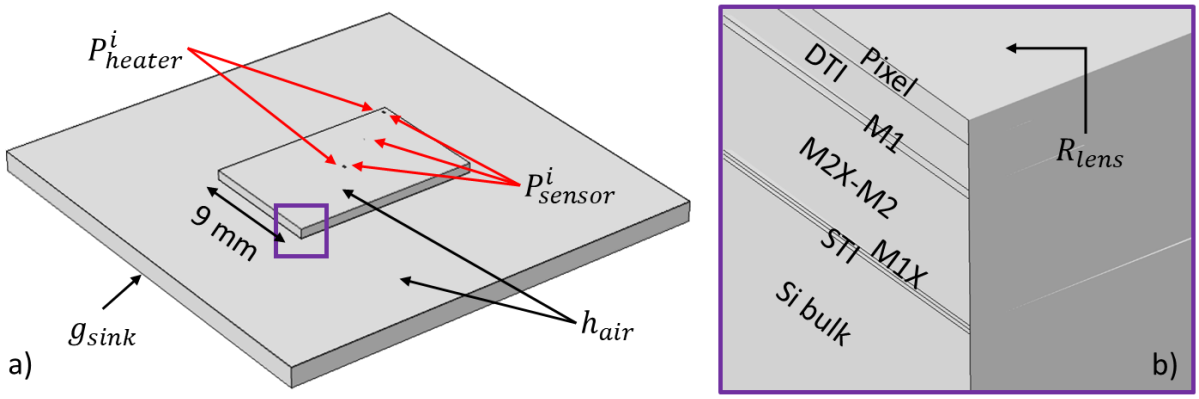

Figure 4.19: Geometry and boundary conditions considered for FLAMINGO FEM model with a) PCB and 3D HB chip and b) BEOL layers and pixel thicknesses.

Figure 4.19 shows the geometry and the boundary conditions in the case of FLAMINGO. P^i_{heater} is the Joule power generated by heaters in the M1X level of the C40 chip. P^i_{sensor} is the Joule power generated by sensors in the M1 level of the I140 chip. The thermal conductance per unit area h_{air} and g_{sink} set as boundary conditions represent both the heat losses through air and towards the substrate holder of the chip. The whole chip/holder is subject to the heat equation. In this study, the same holder than for M3EM is used (see Chapter 2). Here, at first, only the central heater is supplied with current. The injected current in the central heater is equal to 40 mA. Since the electrical resistance of the heater is equal to 180 Ω, the Joule power P^1_{heater} generated by the central heater is equal to 280 mW.

Wire bonding:

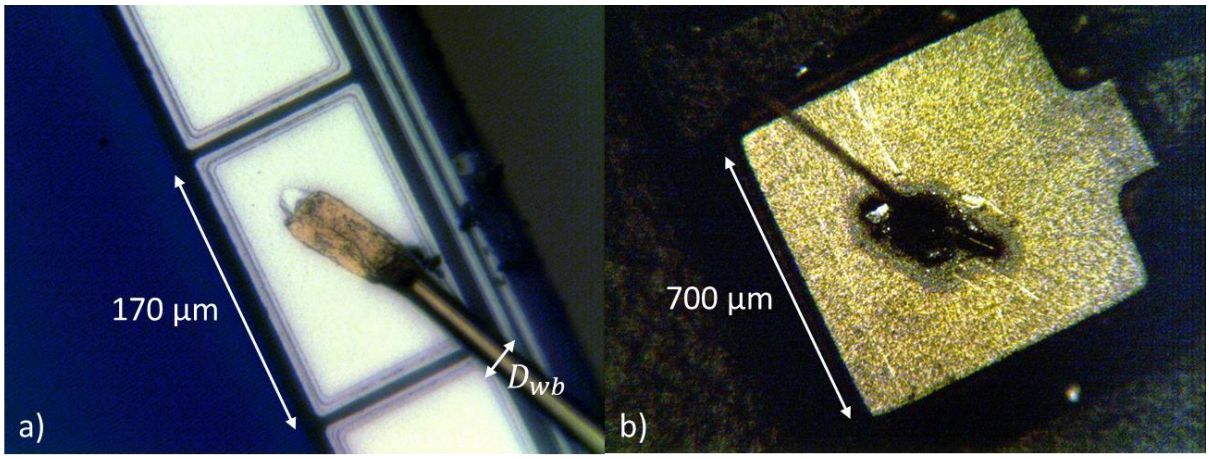

Figure 4.20: Optical microscopy image of the wedge wire bonding realized at CIME Nanotech with a) aluminum pad on top die surface and b) copper pad on epoxy surface.

The impact of the wire bonding on the heat path is taken into account in the same way as in Chapter 3. Figure 4.20 shows optical images of the wire wedge bonding realized at CIME Nanotech by I. Feng.

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Wires of 18 µm diameter are bonded with a pitch of 170 µm on the I140 top chip. Numerically, the bonding areas are simulated as local discs of diameter 18 µm with a heat transfer coefficient g_{wb}. Following [21, 22], the boundary condition g_{wb} is calculated to be equal to 23.7 and 182 kW.m^{-2}.K^{-1} in vacuum and air, respectively.

II.2.C.b. Model calibration with thermoresistive measurement

To evaluate the heat sink conductance g_{sink} and the heat loss coefficient h_{air}, the thermoresistive method developed in Chapter 3 (Section II.3.C.) will be used again. However, in addition to the use of the serpentine central heater (in M1X level) as a thermometer, the central sensor (in M1 level) will also be used at the same time.

Heat sink conductance:

	Heater	**Sensor**
BEOL level	M1X	M1
R_0 (Ω)	160±5	80±5
α (%.K^{-1})	0.321	0.316
ΔR (Ω)	17.90	8.98
ΔT (K)	34.9±1.1	35.5±2.2
g_{sink} (W.m^{-1}.K^{-1})	100±5	100±9

Table 4.3: Thermoresistive measurement of ΔT under vacuum conditions.

The heat sink conductance g_{sink} is evaluated under vacuum. Consequently, the air losses h_{air} are set to 0 in the FEM model. Here, the radiative heat losses are included in the heat sink conductance. The heater and sensor temperature elevations ΔT are measured with:

$$\Delta R_i = R_{0i}\alpha_i\Delta T_i, \tag{4.10}$$

where ΔR is the variation of electrical resistance of the central heater and central sensor, respectively due to Joule heating. α is the TCR of the M1 levels. R_0 is the resistance of the central heater and the central sensor. The variation of resistance ΔR represents the temperature rise generated by the central heater power supply with a current equal to 40 mA. The data are summarized in Table 4.3. For both central heater and sensor, the temperature rise measurements are close. It is consistent because under vacuum conditions, the entire heat flux goes down toward the sink. For the FLAMINGO chip, g_{sink} is fitted to 100 W.m^{-2}.K^{-1}. This is the 2-point measurement method that generates the uncertainty on the fit of g_{sink}. However, this value being very different to the one found for M3EM (fitted to 360 W.m^{-2}.K^{-1}), it shows that the value of g_{sink} must be calibrated for every study case. The value of heat sink conductance could depend strongly on the chip holder.

Heat loss coefficient:

	Heater	**Sensor**
BEOL level	M1X	M1
R_0 (Ω)	160±5	80±5
α (%.K^{-1})	0.321	0.316
ΔR (Ω)	4.33	1.50
ΔT (K)	8.4±0.3	5.9±0.4
h_{air} (W.m^{-1}.K^{-1})	12±2	9±2

Table 4.4: Thermoresistive measurement of ΔT under ambient conditions.

The same methodology is applied under ambient conditions, once the heat sink conductance has been obtained. The measurement performed under air at atmospheric pressure allows determination of the

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heat loss coefficient h_{air} by iterating again on the heater temperature. The temperature variation from vacuum to air measured for both central heater and central sensor leads to a value of h_{air} close to 10 W.m^{-2}.K^{-1}. Similarly, the uncertainty on the fit of h_{air} is generated by the 2-point measurement method. The data are summarized in Table 4.4.

II.2.D. Numerical results and discussion

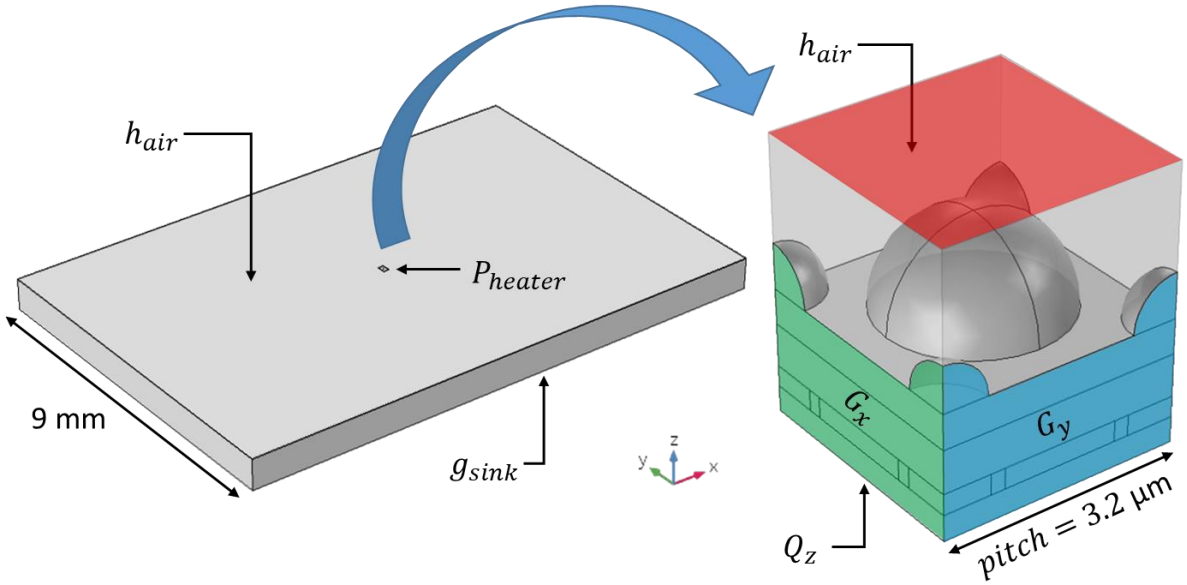

Figure 4.21: Multi-scale FEM modelling of the pixel at the center of the die.

Here, the previous numerical model developed in FEM and calibrated experimentally is used to estimate the temperature field in the FLAMINGO chip and the temperature rise in the pixel of the I140 chip. To do this, a multi-scale FEM modeling approach is chosen. The principle of the multi-scale study and the boundary conditions applied on the pixel is shown in Figure 4.21. Q_z is the inward heat flux density in W.m^{-2} set as a boundary condition on the bottom side of the pixel domain. G_x and G_y are the conductances outside the pixel in the x and y directions in W.m^{-2}.K^{-1}, respectively. G_x, G_y and Q_z are determined numerically with the global FEM model of FLAMINGO as a function of the pixel location in the xy plane. These numerical data are compared to experimental measurements, performed on the FLAMINGO top surface by means of SThM thermometry.

II.2.D.a. Temperature field at the die level

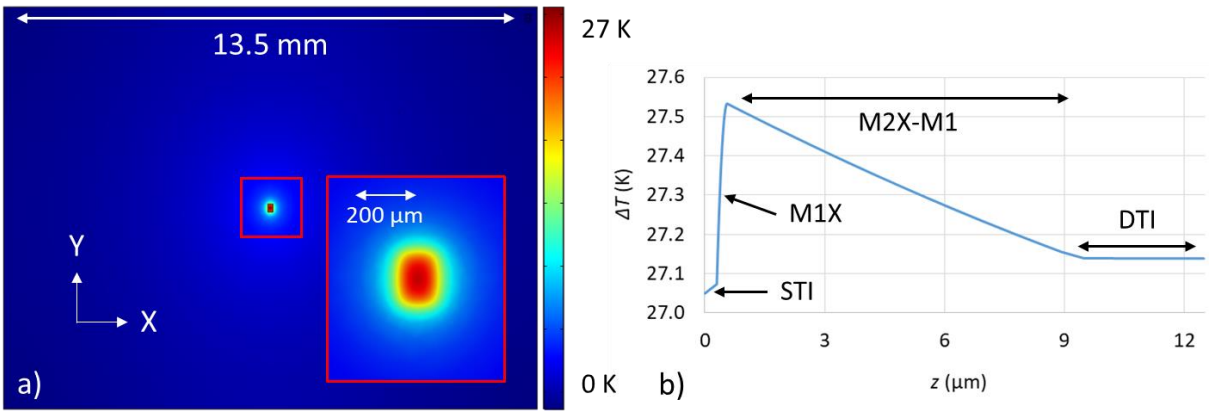

Figure 4.22: Temperature rise calculated by FEM with the FLAMINGO chip.
a) Top surface in the xy plane. b) Along the z axis in the BEOL at the center of the heater.

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The central heater generates a Joule power equal to 280 mW. Figure 4.22 shows the temperature field calculated with FEM at the surface of the FLAMINGO chip and along the z axis at the center of the central heater. The temperature rises in the central heater (M1X) and central sensor (M1), values are found to be equal to 27.3 and 27.1 K, respectively. It is interesting to note that 90.9% of the Joule power flows down in the sink while 9.1% is lost in the air. To go further, it can be seen that although the temperature is constant in the stack, the thermal gradient seems larger in the M1X level than in the rest of the chip levels.

From the FEM model of the entire stack of FLAMINGO, a numerical description of the thermal behavior of the pixel is provided in the next section.

II.2.D.b. Thermal gradient at the pixel level

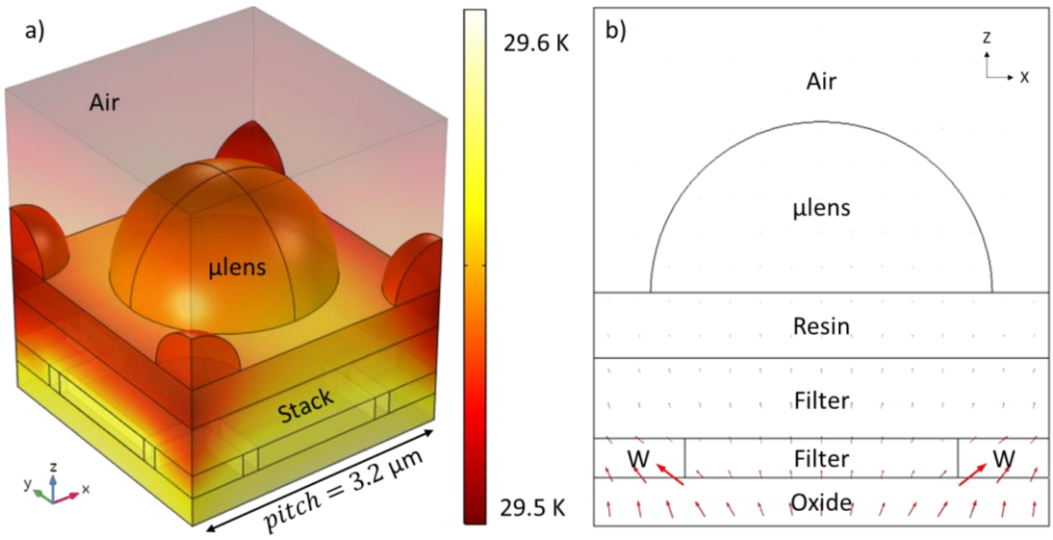

Figure 4.23: a) Temperature field and b) heat flux distribution in the xz plane calculated with multi-scale FEM approach in the pixel located at the center of the die.

The heat transfer in one pixel is determined following the multi-scale FEM approach explained in Figure 4.23. At the center of the die, G_x and G_y are equal to 192 and 34.0 W.m^{-2}.K^{-1}, respectively. Q_z is found equal to 7.15 kW.m^{-2}. The numerical calculations are shown in Figure 4.23. One can see that the pixel temperature is almost homogeneous in the stack with a low heat flux (under 0.1 K.µm^{-1}) mainly located in the tungsten layer where the cross-plane effective thermal conductivity is larger. The surface temperature of the micro lenses is therefore equal to the I140 chip temperature. The impact of different heating scenarios on the pixel array can be therefore estimated easily with the FEM model of the FLAMINGO chip at the die level.

II.2.D.c. Optimization of heat dissipation

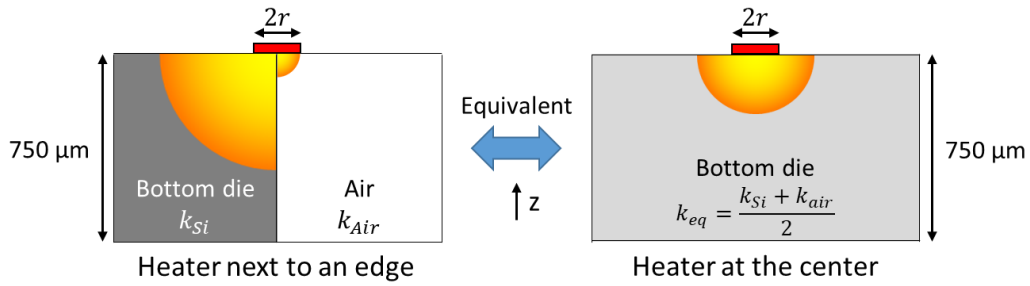

Figure 4.24: Equivalence of heat dissipation ability between a heater on an edge and at the center of the chip when k_{eq} is equal to $k_{Si}/2$ approximatly.

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Since the corner heater was not functional in the test chip, in this section, a numerical study is proposed to estimate the impact of the chip sides on the temperature dissipation. A parametric study is developed as a function of the distance D_x between the chip edge and the center of the heater. The principle and the results of the study are detailed in Figure 4.24. The temperature of the sensor (M1 level) is calculated numerically. The heater temperature is equal to 33.1 K when the serpentine is at the center of the die and 27.1 K when the serpentine is next to the edge of the chip. This dissipation phenomena is explained in Figure 4.25. The result is shown in Figure 4.24.b) where the red line and the orange dashed line intercept with a temperature rise equal to 33.1 K. The more the heater is centered with respect to the chip, the more the heat dissipation is improved. This statement would need to be reanalyzed if wires are bonded close to the heat source.

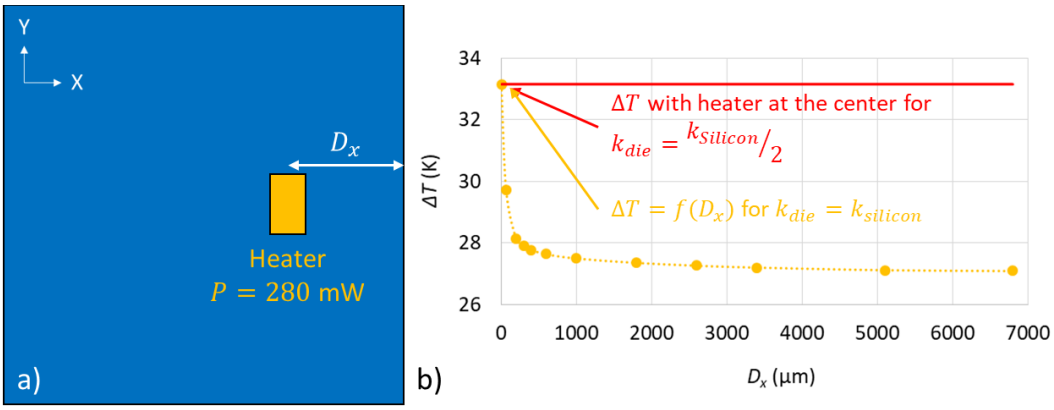

Figure 4.25: Heat dissipation as a function of the distance between the edge and the heater. a) Variable of the parametric study and b) temperature rise calculated on FLAMINGO chip.

II.3. Experimental characterization by means of SThM

In this section, the FLAMINGO chip is used for the experimental characterization of complex 3D hybrid bonded imagers. The SThM technique is used in temperature measurement mode in order to quantify the temperature rise on top of the pixel matrix. First, the experimental setup is described. Then, the surface temperature of the pixel matrix is measured by means of the Wollaston micro-probe under several conditions of use of the chip.

II.3.A. Description of the experimental setup

II.3.A.a. Chip holder improvement

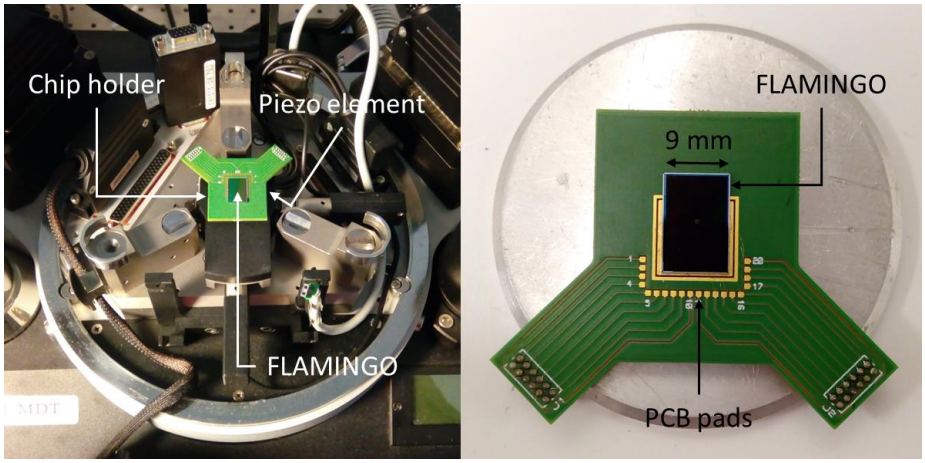

Figure 4.26: Experimental setup for the SThM thermometry on FLAMINGO chip. a) Chip holder inside the MT-MDT SThM. b) Zoom on the chip holder geometry.

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In order to perform SThM measurements when the FLAMINGO chip is electrically supplied, the chip has been connected and integrated into a homemade electronic circuit inside the NT-MDT device. The new chip holder and the electronic circuit are detailed.

The chip holder developed in the CETHIL (Chapter 3 Section III.1.) has been improved to allow the connection of more pads. The last version of the chip holder is shown in Figure 4.26. The wedge bonding technique was used by I. Feng at CIME Nanotech for FLAMINGO. The wire bonding are made of aluminum with a diameter equal to 18 µm and a length equal to 1 mm approximately. A microscopy image of the wire bonding is shown in Figure 4.20.

II.3.A.b. Electrical connection of the chip

A schematic of the electronic circuit is shown in Figure 4.27. The heaters and sensors, in the M1 levels respectively, are set in series with a current supply. A two-point measurement method is used to determine the electrical resistance of the thermoresistive elements. The access resistance R_{access} and the wire bonding resistance R_{wb} are considered negligible in comparison to the resistances R_{heater} and R_{sensor} equal to 160 and 80 Ω, respectively.

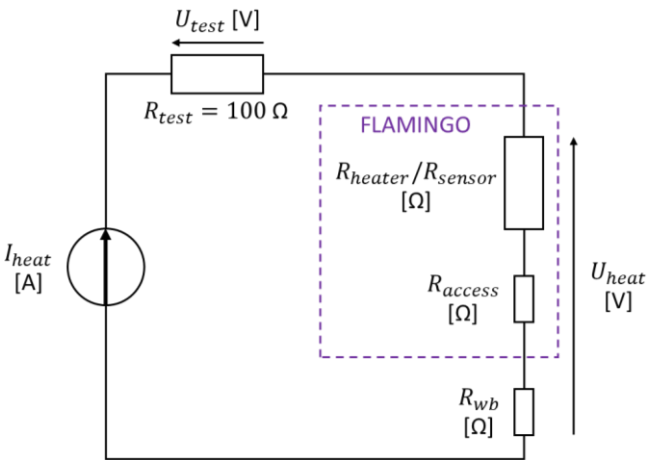

Figure 4.27: Power supply and electrical circuit of the 3D HB chip FLAMINGO.

II.3.B. Description of the heating study cases

	Case 1: Heater supply	**Case 2: Sensor supply**
Heating element	Central heater	Corner sensor
R_0 (Ω)	160	80
ΔR (Ω)	13.6	7.5
I_{heat} (mA)	40.0	10.0
P_{heat} (mW)	278	8.75

Table 4.5: Summary of experimental conditions for the following study cases.

The experimental conditions of power supply are described in Table 4.5. The experiments are performed under ambient conditions. In this study in SThM, the Wollaston micro-probe is used and set in a Wheatstone bridge. The electrical setup is described in Figure 4.28. The resistances R_1, R_a and R_b are taken equals to 100, 1000 and 1000 Ω, respectively. The variable resistance R_v is equal to 1.4 Ω. The resistance R_0 of the Wollaston wire at room temperature is calculated as follows:

$$R_0 = \frac{4\rho_{Pt}L}{\pi D^2}, \tag{4.11}$$

where ρ_{Pt} is the electrical resistivity of the platinum equal to 0.193 µΩ.m, L is the length of the Wollaston wire measured equal to 200±20 µm and D is the diameter of the Wollaston wire measured

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equal to 4.5±0.5 µm. The resistance R_0 is therefore calculated to be equal to 2.6±0.8 Ω. The characterization of the Wollaston probe is detailed more widely in Chapter 2 Section II.3. The Wheatstone bridge is supplied with an electric current I_0 of 40 mA. The current in the probe is therefore equal to 20 mA. The current is chosen higher than 10 mA to ensure that the tip is sensitive to the temperature variations on the FLAMINGO surface. A gain G equal to 500 is applied to V_{ab} to allow accurate measurements of temperature variations. The probe temperature rise ΔT_p is calculated as follows:

$$V_{ab} = G(R_p - R_v)\frac{I_0}{2}, \tag{4.12}$$

$$\Delta R_p = R_0 \alpha_p \Delta T_p, \tag{4.13}$$

where ΔR_p is the variation of resistance of the Wollaston wire, α_p is the TCR of the Wollaston wire equal to 0.166 %.K^{-1} and ΔT_p is the temperature rise of the Wollaston wire. The temperature uncertainty is then:

$$\delta[\Delta T_p] = \frac{2\delta V_{ab}}{G R_p \alpha_p I_0}, \tag{4.14}$$

The temperature uncertainty $\delta[\Delta T_p]$ is equal to 55 mK with these experimental conditions.

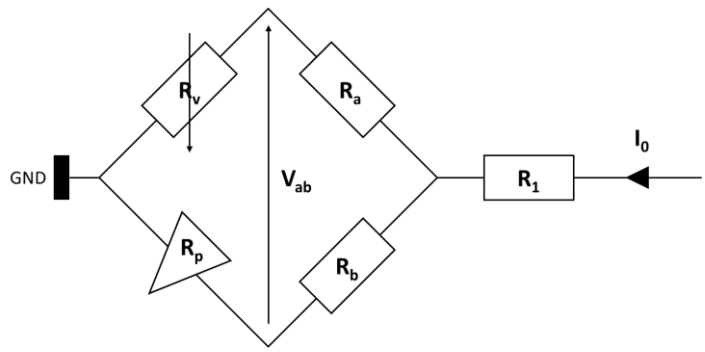

Figure 4.28: Wheatstone bridge setup for SThM measurements.

II.3.C. SThM thermometry with Wollaston micro-probe

In this section, two different analyses are performed with the SThM thermometry on the pixel matrix of the FLAMINGO chip. First, with a large heating scenario, the heater structure (C40 side) is supplied and then, with a hotspot heating scenario, the sensor serpentine (I140 side) is used as a heater element. The latter scenario is not representative of a true user case of the current device but allows additional correlations and thus, validating the robustness of the proposed approach.

II.3.C.a. Heater supply in M1X level

In order to measure the surface temperature of the pixel matrix above the central heater, a method of mapping is chosen. Each point is measured separately on an arbitrarily defined grid (array of 7x7 points) because the matrix surface is too large to be scanned by the piezo element. A schematic of the grid is shown in Figure 4.29.a). The scanning direction of the surface is represented by the red arrow. The grid of points has a surface area equal to 600x600 µm² and a pitch equal to 100 µm. During the measurement with the heater supplied, a voltage of reference V_{drift} is measured at the same location in the center of the grid. The voltage V_{drift} is measured between each line (every 7 points) and represents the thermal drift as a function of the time. The thermal drift V_{drift} is shown in Figure 4.29.b). The variations of voltage ΔV_{ab} generated by the temperature rise of the Wollaston filament ΔT_p are related as follows:

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$$\Delta V_{ab} = V_{ab} - V_{drift}(t), \tag{4.15}$$

$$\Delta V_{ab} = G I_p R_0 \alpha_p \Delta T_p, \tag{4.16}$$

where I_p is the current crossing the probe , ΔT_p and ΔT_s are the temperature rise of the probe and the surface, respectively. The experimental data acquired on the pixel surface with heater supply are shown in Figure 4.30. The thermometry coefficient of the Wollaston probe is taken equal to 29.7% (see Chapter 3). The hotspot is well highlighted on both V_{ab} and ΔT_p images. In this case, the thermal drift, lower than 10 mV, represents a variation of room temperature lower than 120 mK. The influence of the thermal drift is therefore neglected in comparison with the temperature variations of a few kelvins that are generated on the 600x600 µm² surface area.

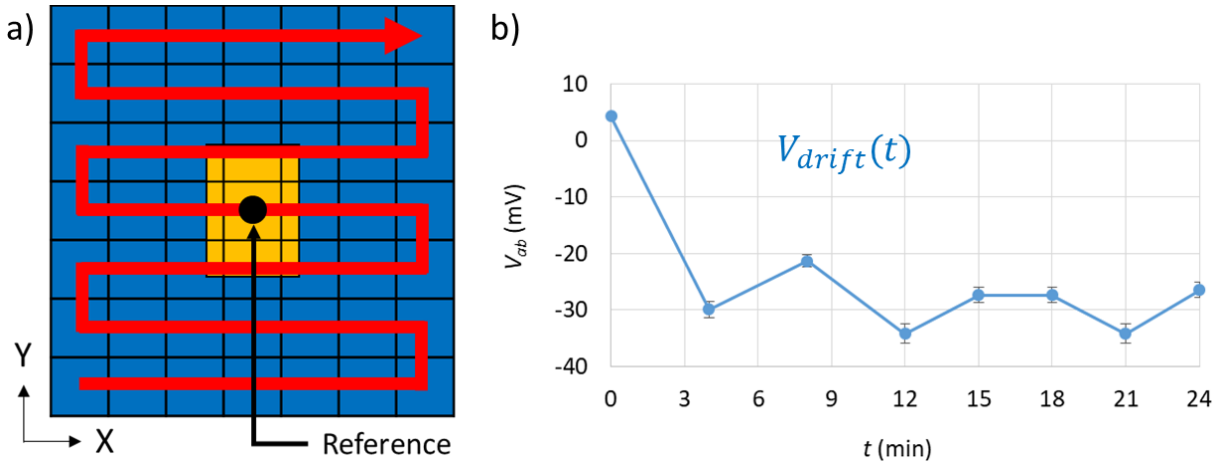

Figure 4.29: a) Points array and scanning direction for mapping thermometry.
b) Drift characterization as a function of the measurement time.

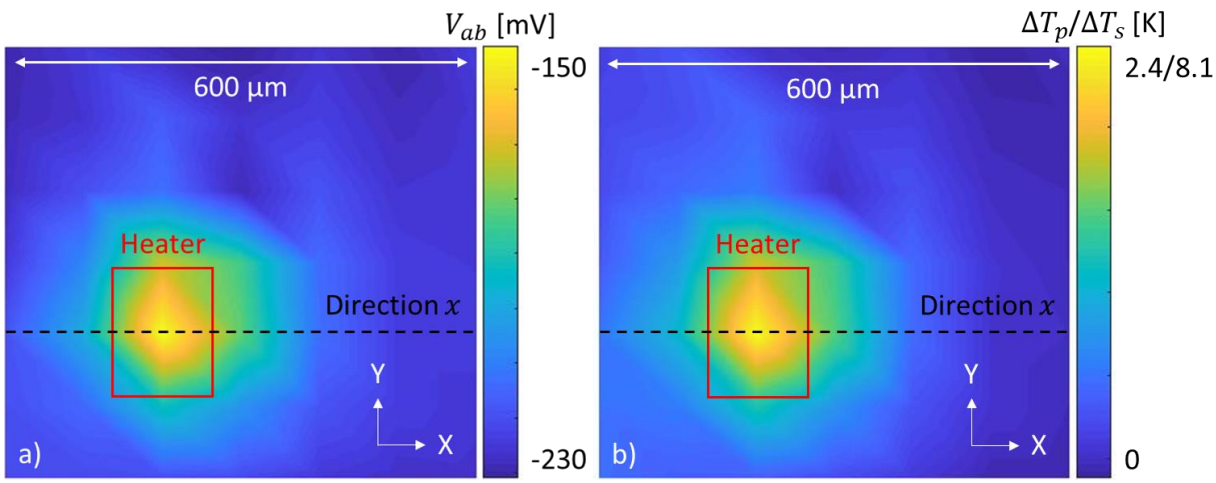

Figure 4.30: Thermometry mapping measurement. a) Raw data of voltage V_{ab}.
b) Filament and surface temperature rise ΔT_p and ΔT_s taking into account the thermal drift V_{drift}.

II.3.C.b. Sensor supply in M1 level

In order to measure the surface temperature of the pixel matrix above the corner sensor, a method of imaging is chosen. The points are measured together on an arbitrarily defined grid: an array of 128x128 points. The scanning direction of the surface is detailed in Figure 4.31.a). The grid of all the points has a surface area equal to 120x120 µm² and a pixel size equal to 925 nm. The time to thermalize for the Wollaston probe being equal to 4 ms [23], one point is taken every 20 ms. The voltage of reference

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V_{drift} cannot be measured far from the sensor. As a consequence, the voltage V_{drift} is measured between each line (every 128 points) at room temperature and represents the thermal drift (contaminations at the tip apex) as a function of the scanning line. V_{drift} is shown in Figure 4.31.b). This assumption is possible if the temperature rise is supposed to be negligible at the image side. The experimental data acquired on the pixel surface with sensor supply are shown in Figure 4.32. The V_{ab} image in Figure 4.32.a) is noisy. In this case, the thermal drift, equal to 200 mV, represents temperature variations equal to 600 mK which cannot be neglected in comparison to the temperature variations. The influence of the thermal drift V_{drift} will be considered for the calculation of the filament temperature rise ΔT_p following Eq. (4.15) and Eq. (4.16). ΔT_p is shown in Figure 4.32.b).

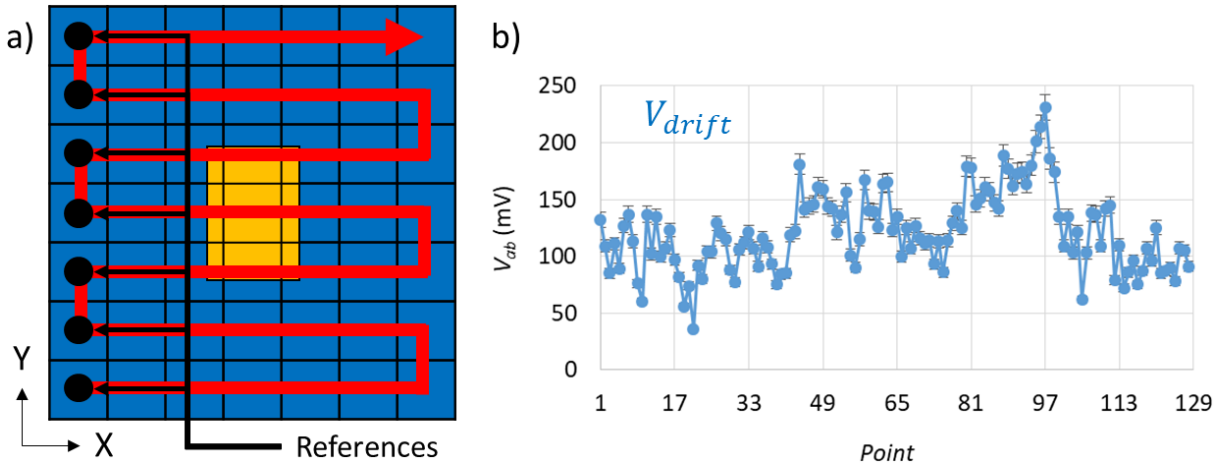

Figure 4.31: a) Points array and scanning direction for imaging thermometry.
b) Drift characterization as a function of the point of reference.

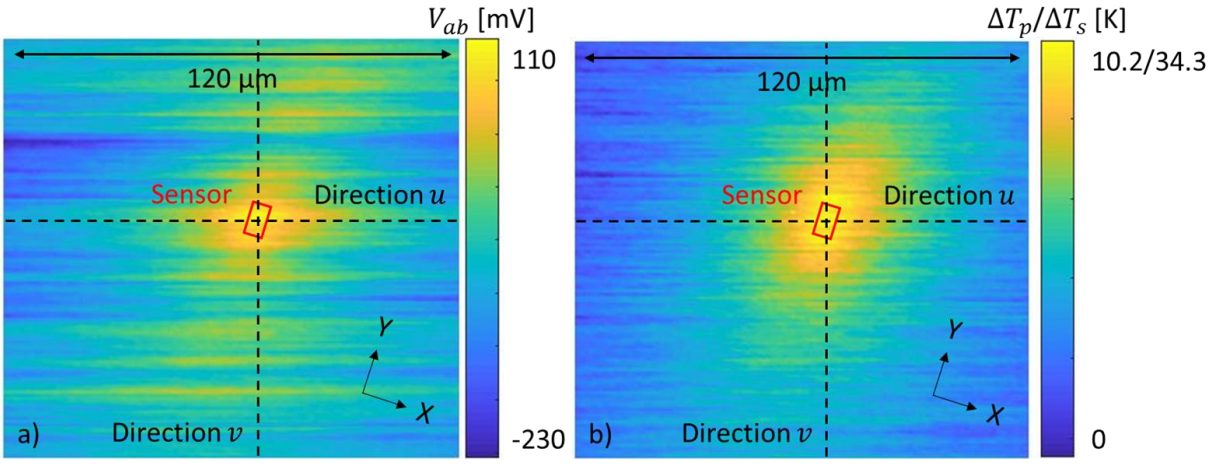

Figure 4.32: Thermometry imaging measurement. a) Raw data of voltage V_{ab}.
b) Filament and surface temperature rise ΔT_p and ΔT_s taking into account the thermal drift V_{drift}.

II.3.D. Correlation between experimental and numerical results

In this section, the experimental temperature measurement is compared with the FEM modelling of the FLAMINGO chip for both cases: heater and sensor supply. The thermometry coefficient of the Wollaston probe is taken equal to 29.7% as demonstrated in Chapter 3. For the following SThM measurements, the uncertainties are related to the uncertainty on the electrical resistance R_0 of the Wollaston filament.

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Case 1: Heater supply

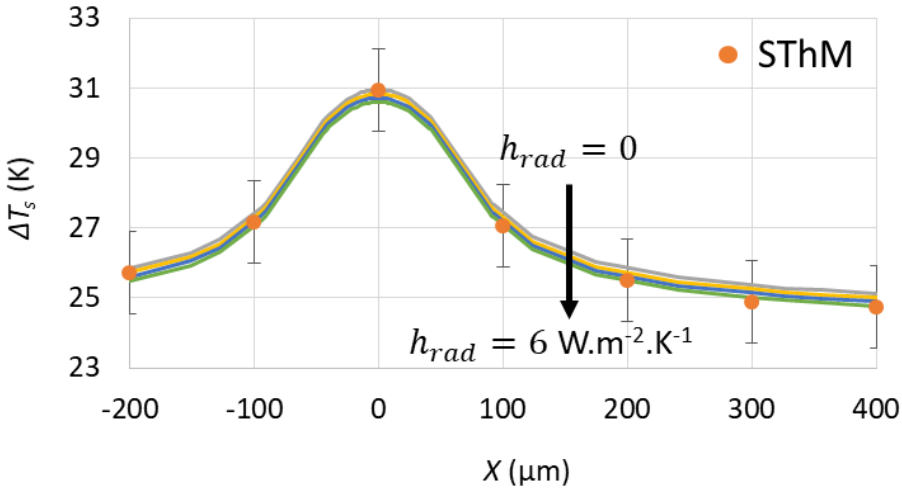

Figure 4.33: FEM calculations as a function of h_{rad} and SThM mapping measurement performed with the Wollaston probe for center heater supply at the pixel matrix surface.

The surface temperature ΔT_s calculated by FEM along the x direction at the center of the central heater is compared to the SThM measurements. A numerical study is made as a function of the radiative heat transfer with h_{rad} from 0 to 6 W.m^{-2}.K^{-1}, where h_{rad} represents the emissivity of the FLAMINGO chip at room temperature (between 0 and 1). The value of h_{rad} is taken into account during the calibration under vacuum and so varies the value of g_{sink}. The study is shown in Figure 4.33. Here, the electrical resistance of the Wollaston filament R_0 is fitted equal to 3 Ω. It can be seen that the FEM calculations and the SThM measurement are in good agreement whatever the value of the radiative heat transfer coefficient h_{rad}. In the following section, the radiative heat losses will be neglected and h_{rad} will be set to 0.

Case 2: Sensor supply

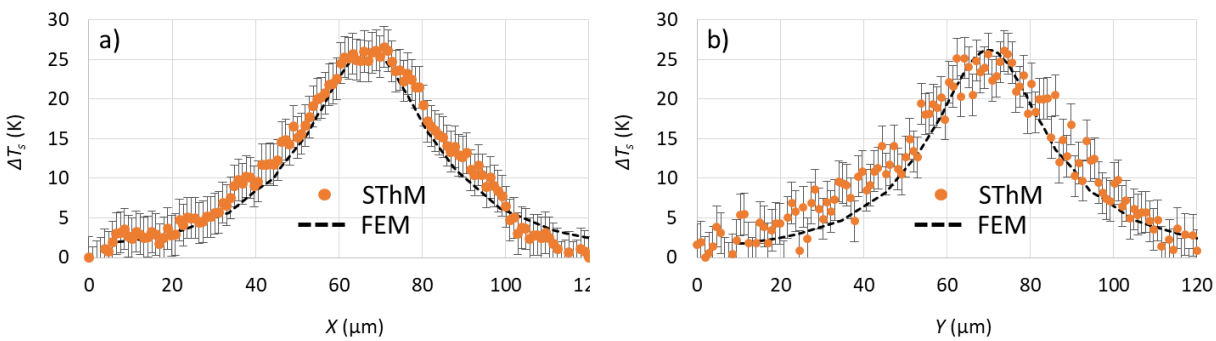

Figure 4.34: Comparison between FEM calculations and SThM imaging performed with the Wollaston probe for corner sensor supply in a) u direction and b) v direction.

The surface temperature ΔT_s calculated by FEM along the u and v directions above the corner sensor is compared to the SThM measurements with the electrical resistance of the Wollaston filament R_0 kept equal to 3 Ω. The comparison is shown in Figure 4.34. A small difference of gradient is visible between the SThM imaging and the FEM model. This must be due to the calculation of the drift V_{drift}, considering the temperature rise equal to 0 on the edges of the image, which is not exactly the case. In addition, it has to be noticed that in SThM, the noise is higher when the profile is taken perpendicularly to the scanning direction (see Figure 4.34.b)). However, the numerical calculation and

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the SThM measurements are in good agreement together. It validates that the numerical procedure developed previously on M3EM is also relevant for the prediction of the self-heating phenomena in complex 3D HB imagers.

II.3.E. Results and discussion

The FLAMINGO test chip has been used to characterize the heat transfer at both die and pixel levels. Embedded elements, i.e. the heaters and sensors of the M1 levels of the C40 and I140 chips, have been used to generate heat. Before concluding on the FLAMINGO thermal behavior, it is necessary to remind the fundamental effects of the boundary conditions on the thermal results in the steady state. The device is thermally driven by the boundary conditions. In that frame, the results should be always analyzed in light of the experimental conditions (setup detailed in Section II.3.A.).

II.3.E.a. Characterization with embedded sensors

The temperature rises generated by the heating elements are summarized in Table 4.6. ΔT_{M1X} and ΔT_{M1} are the thermoresistive measurement of temperature rise in the M1X and M1 levels, respectively. One can notice that the temperature elevations are lower than 30 K for this current technology. Indeed, pad protection diodes limit the current injection into the thermal structures. Although measurable, thermal effects could be more easily demonstrated without this technological limitation. It can nevertheless be noted that the thermal gradient in the BEOL is small (under 3 K) which gives little margin for the reduction of the temperature with the optimization of the BEOL structure.

	Case 1: Heater supply	**Case 2: Sensor supply**
BEOL level	M1X	M1
I_{heat} (mA)	40.0	10.0
P_{heat} (mW)	280	8.8
ΔT_{M1X} (K)	26.5±1.1	-
ΔT_{M1} (K)	29.6±2.2	29.7±2.2

Table 4.6: Thermoresistive temperature rises measurement with FLAMINGO test chip.

II.3.E.b. Characterization with SThM technique

By using the FLAMINGO chip, the advantages and drawbacks of the SThM technique could be highlighted. It has been shown in particular that SThM thermometry can be used to measure the temperature rise of a surface and the thermal gradients. The temperature rises and gradients linked to the heat source are summarized in Table 4.7. ΔT_{SThM} is the temperature rise measurement at the pixel array surface and σ_{SThM} is the width at half-height of the temperature profile. It is important to note that the SThM method (mapping or imaging) must be chosen regarding the expected thermal gradient in order to obtain an accurate temperature measurement.

	Case 1: Heater supply	**Case 2: Sensor supply**
BEOL level	M1X	M1
I_{heat} (mA)	40.0	10.0
P_{heat} (mW)	280	8.8
Method	Mapping	Imaging
Surface (µm²)	600x600	120x120
ΔT_{SThM} (K)	31±1	26±2
σ_{SThM} (µm)	170±20	40±5

Table 4.7: SThM temperature rises measurement on I140 pixel array surface.

In the next section, the study of thermal dissipation for 3D hybrid bonding imagers will be extended to a commercial chip called 93D. This device will be used to estimate among other things:

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(i) the influence of the temperature on the optical performances of the pixel matrix;

(ii) the transient effects and the dynamic response of the pixel of the I110 imager.

III. Transient effects: optical performances for 93D chip

In this section, a study is performed on the 93D demonstrator. First, the structure and the characteristics of the 93D chip is described. Then, the self-heating phenomenon is quantified experimentally in terms of optical performances in different cases (static and dynamic).

III.1. Description of the 93D demonstrator

The structure of the 93D demonstrator is now described. First, general specifications are indicated and then the thermal structures embedded in the bottom and bottom chips are detailed.

III.1.A. General specifications

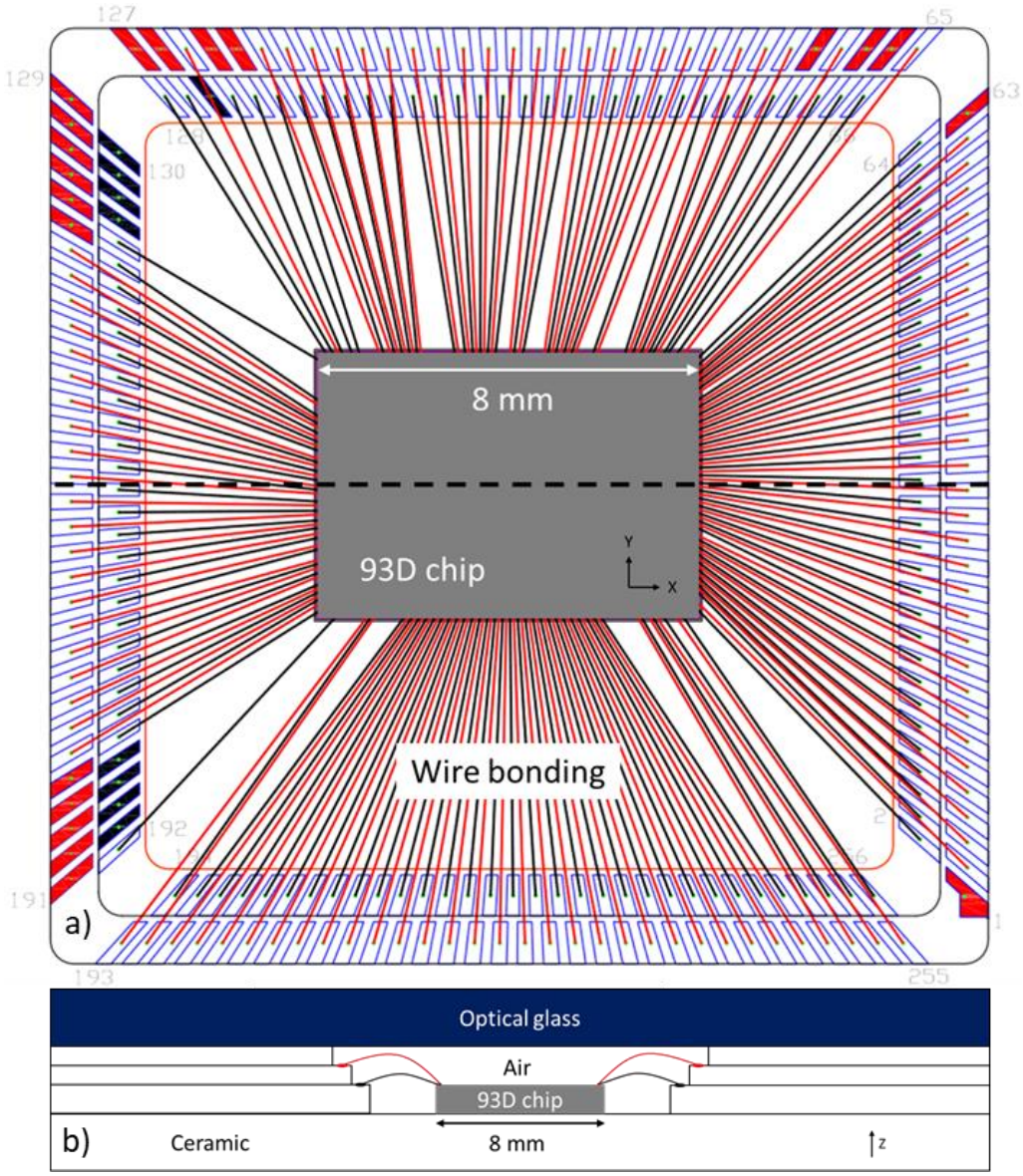

Figure 4.35: Schematic of the 93D demonstrator. a) In-plane geometry of the chip with the wire bonding location. b) Cross-section of the chip and the ceramic package.

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The 93D chip is a 3D hybrid bonded back-side imager with the same structure as the FLAMINGO chip. It is composed of two chips: the C40 bottom chip and the I110 top chip. However, it differs from FLAMINGO in the sense that the 93D chip is a demonstrator. It aims to demonstrate the know-how of STMicroelectronics for 3D HB IMG objects. It is a fully-functional chip. On our side, it introduces an object which is much more complicated to test (complex test program and board test) and simulate (complicated circuitry). Hence, and as described further, some of the methods described previously could not be used for this chip (SThM approach, modelling….). However, its main advantage is to provide some interesting information on the optical performances at the pixel side (active matrix) and in a transient regime.

The 93D chip being active, the Joule power is generated at the FEOL level by functional blocks consisting of transistors and not anymore resistive heaters. Moreover, unlike FLAMINGO, the 93D chip is provided entirely packaged. A schematic of the 93D demonstrator and the package is shown in Figure 4.35. It is important to mention that a ceramic package which has a good heat sink [24] was chosen to limit the heating phenomena. The following study, carried out in a favorable case, could be used as a reference for more constrained cases of use.

III.1.B. Embedded thermal structures

In this section, the thermal structures are detailed. In the 93D chip, all the heaters and sensors have been embedded in the bottom chip of the 3D HB IMG: the C40 chip. First, the floorplan of the C40 FEOL is described. Then, the working principles of the heater and sensor structures are analyzed.

III.1.B.a. Design of the C40 FEOL

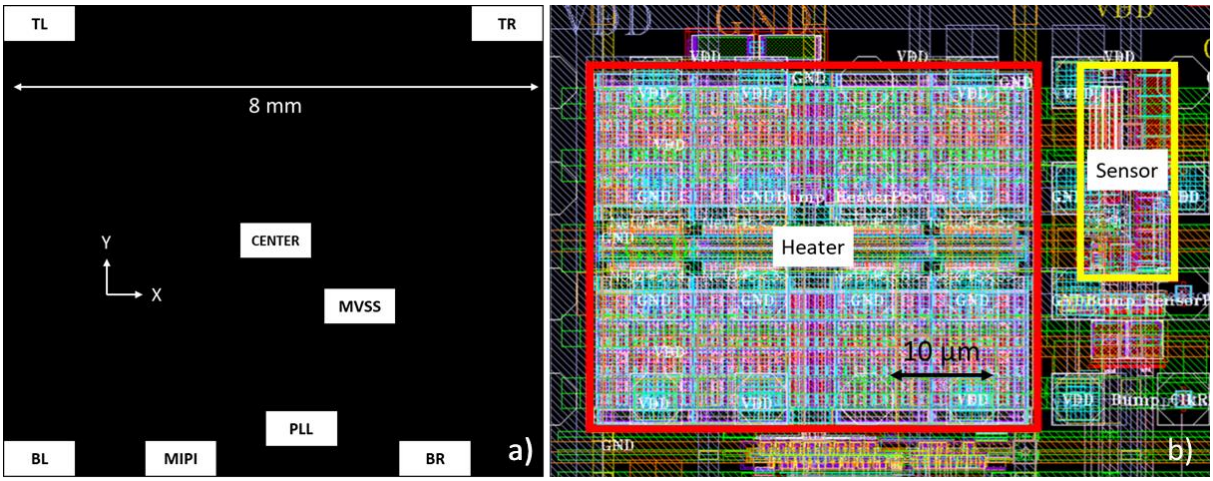

Figure 4.36: a) Location and b) geometry of the thermal structures in the C40 FEOL.

In the 93D demonstrator, 8 thermal structures have been embedded in the FEOL level of the C40 bottom chip. The location and the geometry of the thermal structures are shown in Figure 4.36. The thermal structures embedded in the 93D demonstrator are all identical. These structures are made of two parts: the heater and the sensor. The heater and the sensor have a surface area equal to 43x35 µm² and 9x20 µm², respectively. Numerous additional functional active blocks are present in the C40 FEOL (power management, data processing, memory…). These functional blocks are therefore generating a heat of their own. The corresponding powers depends on the user case predefined by designers (face recognition for instance). It is also difficult to identify precisely the origin of the power dissipated since they are not limited to a rectangular source domain, in contrary to M3EM or FLAMINGO chips.

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III.1.B.b. Heater and sensor structures

Heater:

One heater contains 8 cells (each one is made with a grid of transistors) designed to drain 6.25mA each approximately when working under 1V supply. The heat flux generated by the transistors depends on temperature and supply voltage. The power generated according to the different experimental parameters for this type of heater is given by the supplier (CEA LETI). The power generation is detailed in Figure 4.37. In our case, the supply voltage is set to 1.08 V. The power generation of the heater is therefore equal to 60±5 mW.

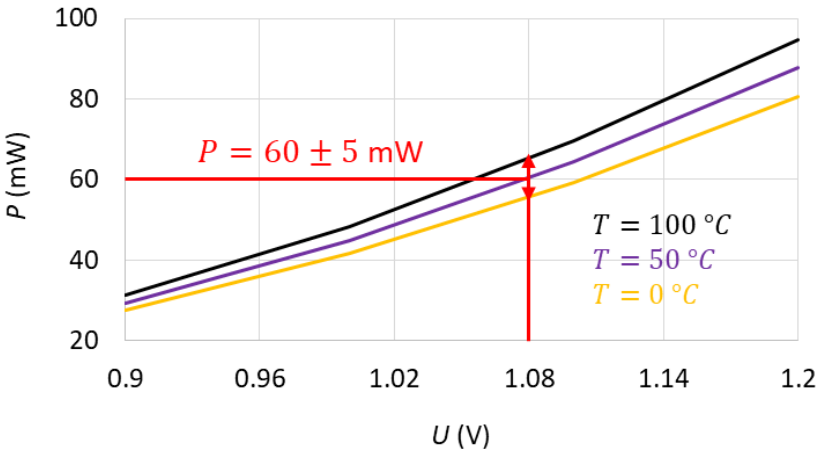

Figure 4.37: Heater power generation as a function of the voltage supply and the temperature.

Sensor:

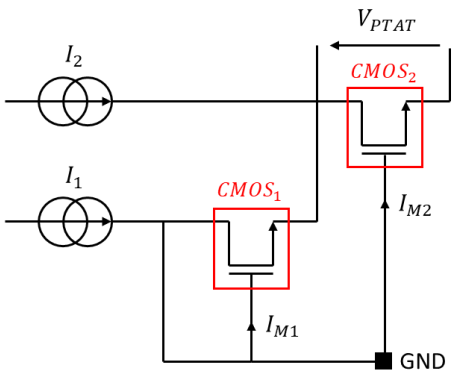

Figure 4.38: Schematic of the PTAT sensor concept [25].

PTAT (Proportional Temperature Absolute Temperature) sensors [25] are used for the temperature measurements. A schematic of PTAT sensor is shown in Figure 4.38. This technology is made of two CMOS transistors and current sources. The output voltage V_{PTAT} is given as follows [26]:

$$V_{PTAT} = T\frac{k_b}{q}\ln(1 + \frac{I_{M1}+I_{M2}}{I_{M1}}\frac{W_{M1}}{L_{M1}}\frac{L_{M2}}{W_{M2}}), \tag{4.17}$$

where T is the temperature, k_b is the Boltzmann constant equal to 1.38×10^{-23} J.K^{-1}, q is the electron charge equal to 1.6×10^{-19} C, W is the MOS channel width and L is the MOS channel length. I_{M1} and I_{M2} are the currents flowing in the $CMOS_1$ and $CMOS_2$ transistors, respectively. On the basis of Eq. (4.17), it is clear that the output voltage is proportional to temperature. A PTAT sensor generates a Joule power lower than 200 µW [26], much smaller than the power generation of the heater (equal to 60 mW approximately). The self-heating of the sensors is therefore negligible.

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III.2. Experimental characterization of the 93D chip

In this section, the thermal behavior of the 93D chip is characterized experimentally. Note that due to the complexity of the device, experiments have been done in collaboration with the test team located at ST Grenoble. Thus, board test and program were done by this team. First, the heat dissipation of the 93D demonstrator is estimated with the PTAT sensors. Then, the optical performances of the I110 imager are monitored to evaluate the impact of the temperature and the thermal gradient.

III.2.A. Measurement of the heat dissipation with PTAT sensors

In this section, the PTAT sensors are used to quantify both the temperature elevation generated by the heaters and the thermal time constants associated to the 93D demonstrator.

III.2.A.a. Heater generated temperature rise

PTAT sensor	TL	TR	BR	BL	CENTER	MIPI	PLL	MVSS
ΔT_{heater} (K)	6±1	8±1	7±1	7±1	8±1	6±1	6±1	6±1

Table 4.8: Heater temperature rise measured at steady state with PTAT sensor.

The temperature rise ΔT_{PTAT} for each thermal structure is measured in the FEOL level of the C40 bottom chip. The temperature rise ΔT_{PTAT} can be expressed as follows:

$$\Delta T_{PTAT} = \Delta T_{heater} + \Delta T_{FEOL}, \tag{4.18}$$

where ΔT_{heater} is the temperature rise generated by the heater activation and ΔT_{FEOL} is the temperature rise generated by the functional bocks of the FEOL (power supply, memory, signal treatment…) close to the PTAT sensor. The study is done under ambient conditions with the FLAMINGO chip power supply. The temperature rise ΔT_{heater} is determined at steady state by subtracting data with and without the heaters being supplied. The experimental results are summarized in Table 4.8. The precision of the PTAT sensor output is equal to +/-1 K. The temperature elevation generated by the heater activation is found equal to 7±0.4 K.

III.2.A.b. 93D demonstrator thermal time constants

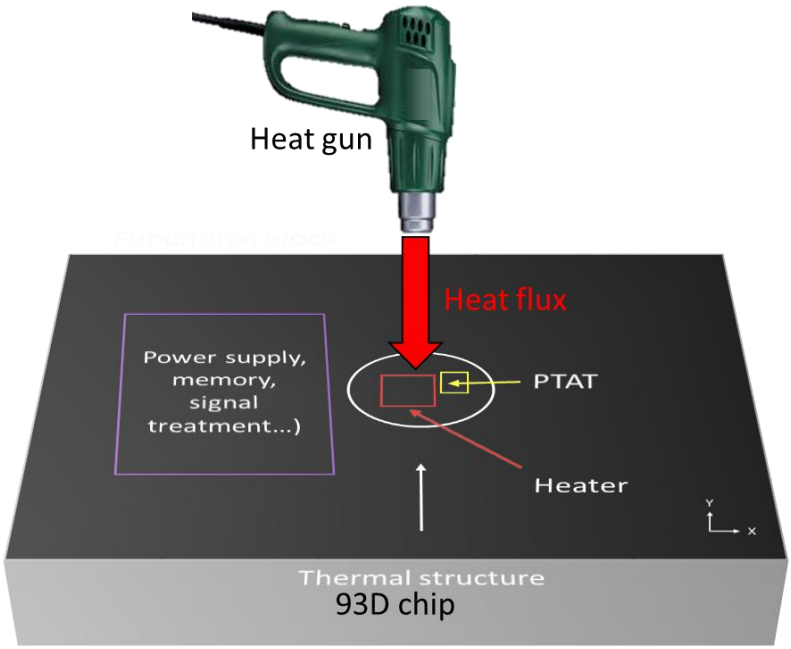

Figure 4.39: Schematic of the PTAT sensor temperature rise generated by the functional blocks (power supply, memory, signal treatment…), the heater elements and the heat gun.

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In order to observe the influence of the temperature at the chip/package level, an additional temperature rise is to be generated. The 93D demonstrator being too large to be placed in a thermal furnace, the full system is heated with a heat gun as shown in Figure 4.39. The total temperature rise measured with a PTAT sensor is therefore equal to

$$\Delta T_{PTAT} = \Delta T_{heater} + \Delta T_{FEOL} + \Delta T_{gun}, \tag{4.19}$$

where ΔT_{gun} is the temperature rise generated with the heat gun. The chip/package system is heated with a heat gun above 130 °C. The 93D chip is activated without heater supply. The measurement is triggered while the chip and package return to room temperature. The results are shown in Figure 4.40. Two characteristic time constants are highlighted for the 93D demonstrator. The temperature can be fitted as follows

$$\Delta T(t) = \Delta T_{FEOL} + \theta_{die} e^{\frac{-t}{\tau_{die}}} + \theta_{package} e^{\frac{-t}{\tau_{package}}}, \tag{4.20}$$

where τ_{die} and $\tau_{package}$ are the time constants related to heat dissipation in the die and the package, equal to 5.0 and 220 s, respectively. θ_{die} and $\theta_{package}$ are the amplitudes of the temperature in the die and package, equal to 6 and 78 K, respectively. The temperature rise generated by the functional bocks of the FEOL at steady state ΔT_{FEOL} is found equal to 24 K.

The temperature is fitted with exponential functions. Although inexact, the results are close to the theory of heat conduction that uses integral exponential functions (erf like functions) [27]. With L the characteristic length and D the diffusivity, the time constants τ of the system is equal to L^2/D. For the 93D demonstrator, L is equal to 1 and 20 cm and D is equal to 10^{-4} and 10^{-6} m².s^{-1} for the die and package, respectively. The experimental results are found in good agreement with these theoretical estimations.

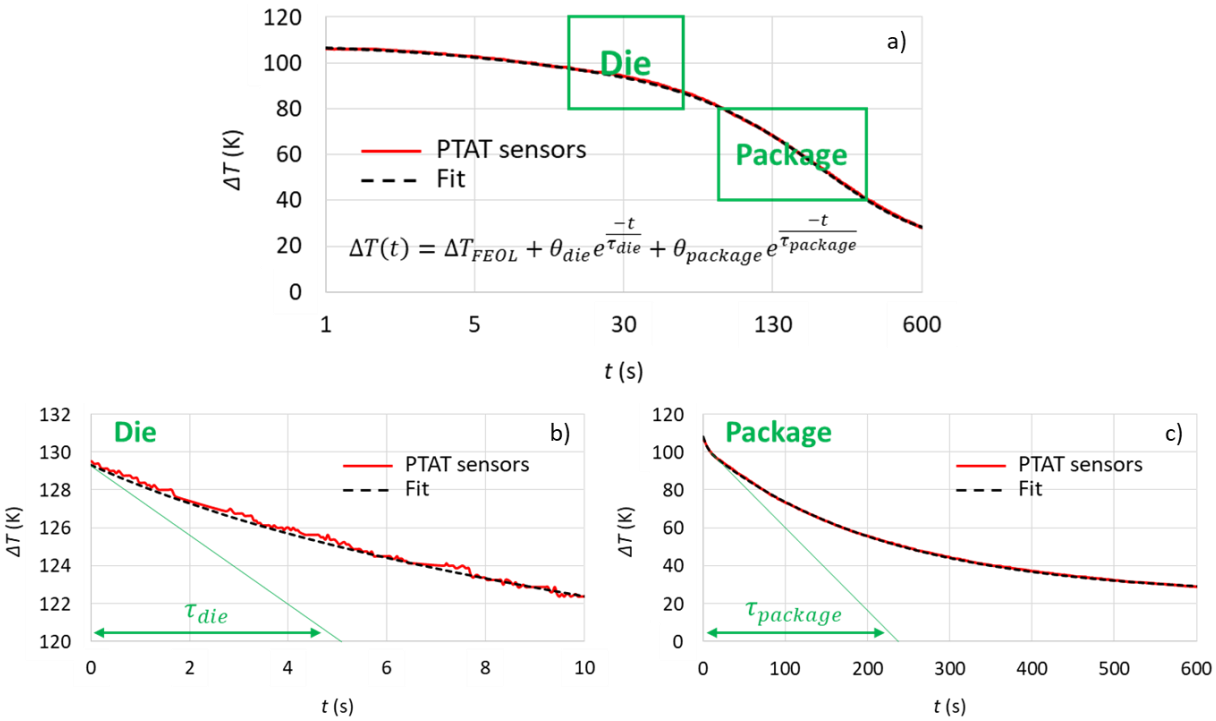

Figure 4.40: Thermalization of the 93D demonstrator. a) Fit of the PTAT sensor temperature with exponential functions. Determination of the b) die and c) package time constants.

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III.2.B. Optical performance: effect of temperature

In this section, we focus on a new way to characterize the surface temperature of the 93D chip. Indeed, the chip 93D being encapsulated in a ceramic package, it is impossible to use a method of surface microscopy such as the SThM technique for example. However, since the pixel array is active, it can be used as a temperature sensor above the I140 chip. First, the thermal response of the pixels will be determined in the dark. Then, the pixel matrix will be used to measure the temperature rise generated by the heaters of the C40 chip.

III.2.B.a. Pinned photodiode dark current calibration

In order to use each pinned photodiode (PPD) [28, 29] as a thermal sensor, the dark current [30] of each pixel is calibrated as a function of temperature. The dark current is the photodiode current generated without illumination. The dark current depends strongly on temperature [31] and is therefore a noise that must be as small as possible to obtain sufficient signal-to-noise ratio (SNR). In order to calibrate the dark current, the 93D demonstrator is covered to avoid any illumination. The average dark current of the pixel array is measured as a function of the PTAT sensors temperature. The calibration curve is shown in Figure 4.41. The photodiode output (proportional to the photodiode current) in the dark for each pixel, termed the code, represents the dark current intensity. It is related to the technological characteristics of the pinned photodiode (size, doping…). In this case, in the exponential regime (above 80 °C) the code doubles every 7.7 K (fitted numerically). Indeed, at high temperatures, the electrons in the valence band become excited into the conduction band. This phenomena is explained by Widenhorn in [32] with the following equation:

$$I_{dark} = I_{dep} + I_{diff}, \tag{4.21}$$

where I_{dark} is the dark current, I_{dep} is the depletion current and I_{diff} is the diffusion current. Indeed, at high temperature, I_{dark} is mainly driven by the diffusion with I_{diff} depending strongly on temperature. Conversely, at low temperature in the nonlinear regime (under 80 °C), the dark current is driven by the depletion current and depends weakly on temperature.

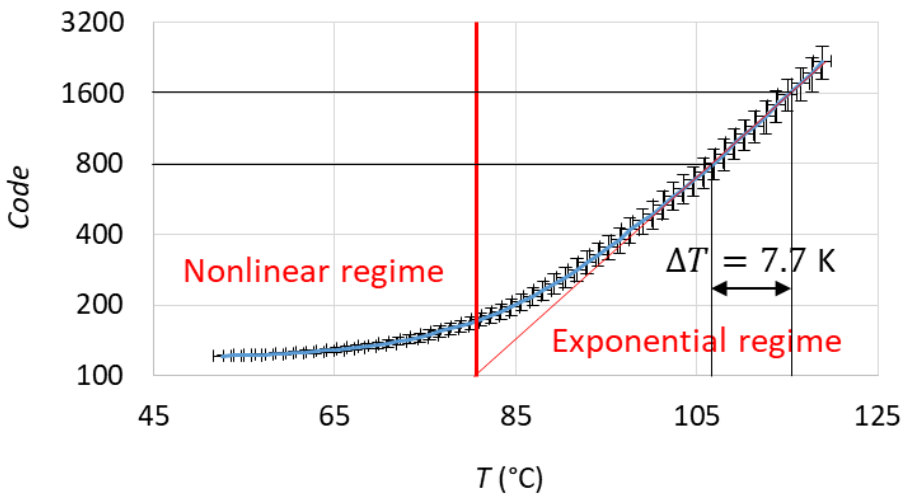

Figure 4.41: Dark current as a function of the temperature measured by the PTAT sensors.

III.2.B.b. Temperature field measured with pixel matrix

In this study, the 93D demonstrator is maintained at 120 °C with the heat gun in order to allow measurements by the pixel array in its temperature sensitivity range. The heaters TL, TR, BL, BR and CENTER are activated together. The intensity of the dark current is acquired with the pixel array. The

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temperature of each pixel is determined with respect to the dark current value. The experimental measurements are shown in Figure 4.42. The temperature rise above each heater is well highlighted by the measurement with the pixel matrix. It is measured equal to 7 K approximately, which is in good agreement with the measurements performed with the PTAT sensors. The validity of the approach with the pixel matrix is therefore proved in the case of steady-state heating which leads to a spatial resolution of 1.75 µm. The full width at half maximum of the temperature profile is determined equal to 100±20 µm. For reminder, the heater dimensions are equal to 35x43 µm²

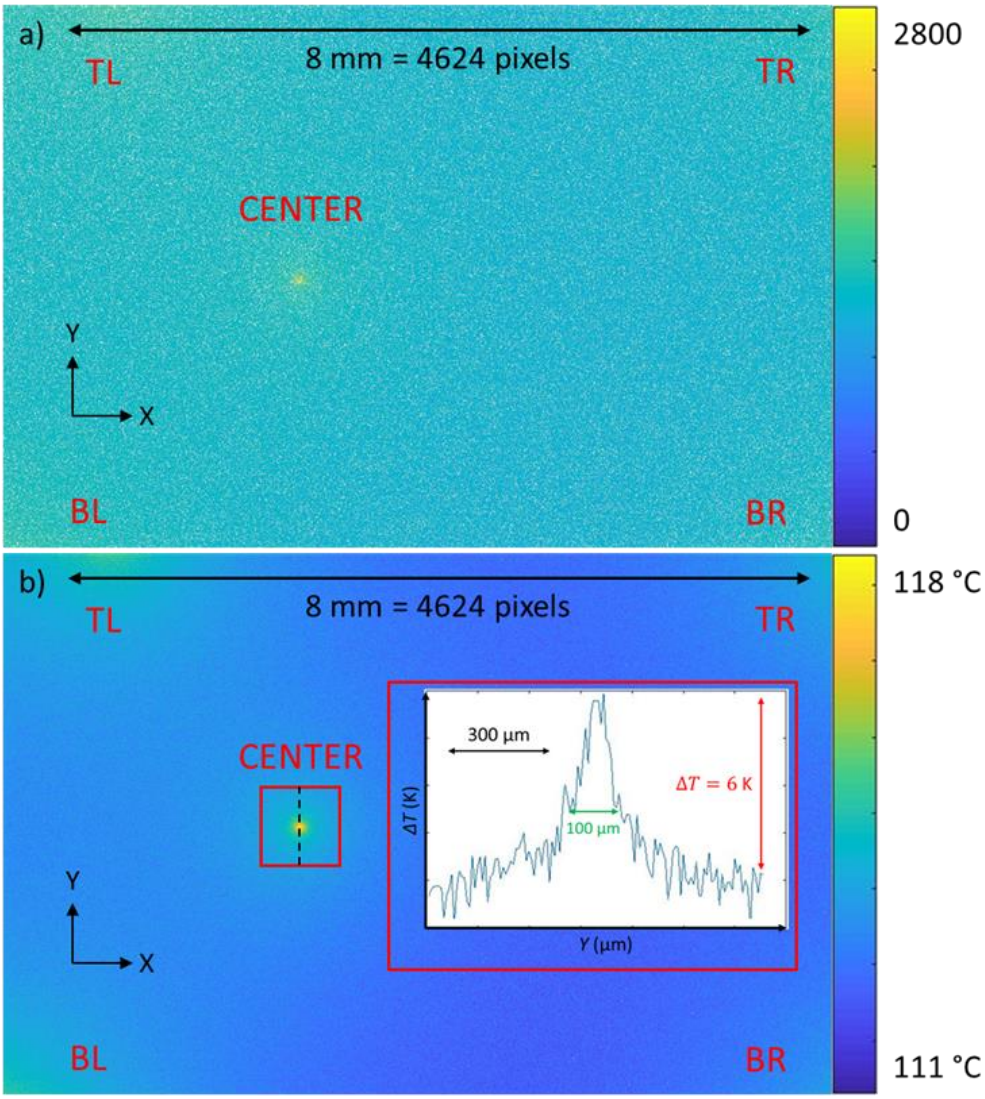

Figure 4.42: Measurement with the pixel matrix of the 93D chip of a) the dark current intensity and b) the deduced surface temperature.

III.2.B.c. Transient analysis of heat dissipation in the pixel matrix

Here, in the same way, the demonstrator 93D is maintained at 120 °C with a heat gun. The CENTER heater, previously activated, is turned off between frame N and frame N+1. The thermal signal of the pixels above the heater CENTER is monitored in real time with a frame rate equal to 30 Hz (maximum value available). Figure 4.43 shows the temperature rise above the heater CENTER as a function of the time. Note that the steady state is reached between 33 and 67 ms. Indeed, the signal measured in frame N+2 represents only the thermal noise which is equal to 0.8 K. Unfortunately, the frame rate of the pixels cannot be increased. It is only possible to state that the characteristic time constant of the

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pixel is of the order of a few tens of milliseconds for the 93D demonstrator. Subsequently, the FEM modelling will be used to see if it is possible to reproduce numerically the transient phenomena and observe the time constant.

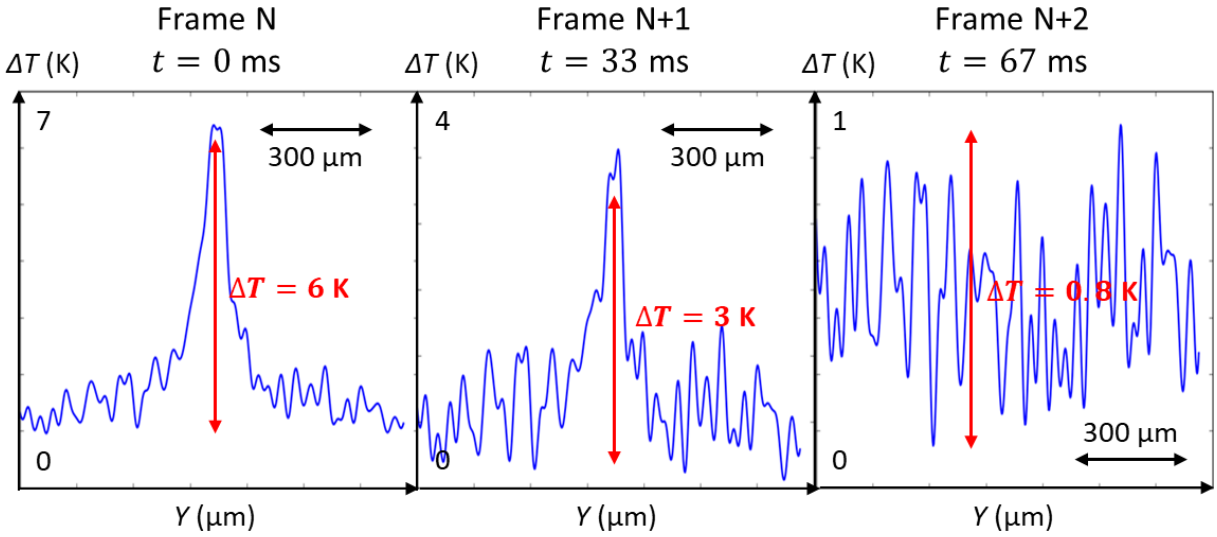

Figure 4.43: Transient behavior toward thermalization measured with the pixel matrix of the 93D chip at a frame rate of 30 Hz.

IV. Transient effect: preliminary numerical investigations

In this section, the experimental characterizations of the transient self-heating effects of the 93D chip is compared with dedicated modelling. The 93D demonstrator is modelled with FEM following the procedure developed in Chapter 3. Then, a numerical study is performed to calculate transient dissipation at both pixel and die levels.

IV.1. FEM modelling of the 93D demonstrator

In this section, the transient thermal behavior of the 93D demonstrator is modelled by means of FEM. The previous numerical modelling strategy developed for the stationary studies is used as a basis for the modelling of transient heat dissipation. First, the geometry and the boundary conditions are detailed. Then, the FEM model is calibrated and validated at steady state.

IV.1.A. Geometry and boundary conditions

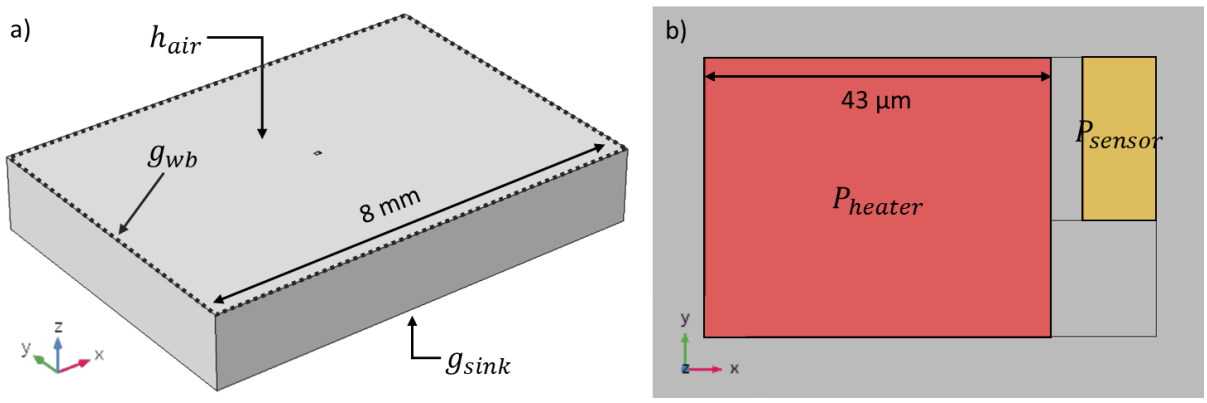

Figure 4.44: a) Geometry and boundary conditions applied on 93D chip FEM model.
b) Boundary heat source generated by the thermal structure in the FEOL.

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The FEM model of the 93D chip is developed on the same principle as that of the FLAMINGO chip (Section II.2.). The boundary conditions are summarized in Figure 4.44. The heat source P_{heater}, equal to 60±5 mW, is set as a surface boundary condition between the STI level and the BEOL and located in M1X level. In this FEM model, the diffusivity of the silicon, silicon dioxide and copper are taken equal to 88, 0.83 and 117 µm².s^{-1} [33, 34], respectively. The BEOL is homogenized with the parallel and series conductance as for the FLAMINGO chip. Considering gold wire bonding with a diameter of 45 µm, the conductance of the bonding g_{wb} is set to 113 kW.m^{-2}.K^{-1} (Chapter 3 Section II.3.B.).

IV.1.B. Calibration of the 93D chip FEM model

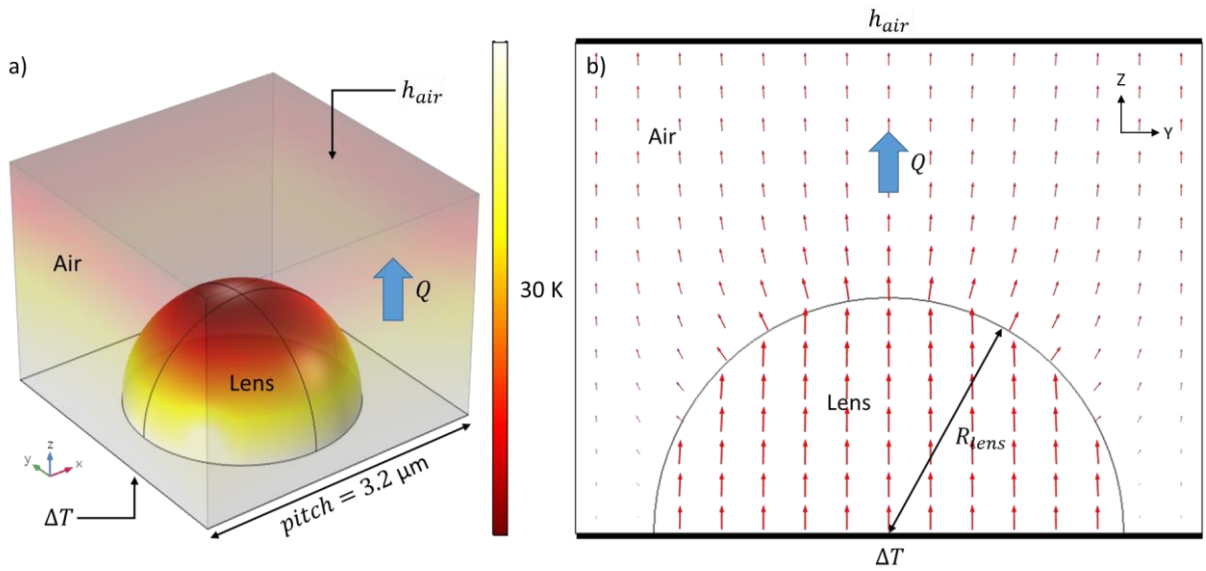

Figure 4.45: FEM modelling of the roughness effect on heat transfer through air. a) Geometry of the roughness (micro lens) and boundary conditions. b) Heat flux distribution in the yz plane.

The heat sink g_{sink} and the air losses h_{air} need to be determined experimentally as a function of the PTAT sensor temperature (equal to 7±0.4 K under ambient conditions). However, the 93D chip being encapsulated, it is impossible to measure the PTAT sensor temperature under vacuum. The air losses coefficient h_{air} is then assumed constant with respect to FLAMINGO and M3EM chips. This assumption, valid in the case where the heat transfer through air does not depend on roughness, is demonstrated with the FEM model shown in Figure 4.45. The heat flux Q is found equal to 3.0728 and 3.0720 nW with and without the lens, respectively. Indeed, whatever the size of the roughness, the heat flux going into air remains constant. h_{air} is therefore taken equal to 10±2 W.m^{-2}.K^{-1}.

The heat sink coefficient g_{sink}, fitted equal to 420±20 W.m^{-1}.K^{-1}, is larger than the values found for M3EM and FLAMINGO chips. This large heat dissipation is explained by the ceramic package which is highly thermally conductive. Indeed, 97.7% of the Joule power goes down in the sink while only 2.3% dissipates though air. The boundary conditions are summarized in Table 4.9.

Heat path	Boundary condition
Heater power	$P_{heater} = 60 \pm 5$ mW
Heat sink	$g_{sink} = 420 \pm 20$ W.m^{-2}.K^{-1}
Air losses	$h_{air} = 10 \pm 2$ W.m^{-2}.K^{-1}
Wire bonding	$g_{wb} = 113 \pm 6$ kW.m^{-2}.K^{-1}

Table 4.9: Boundary conditions for 93D chip FEM modelling.

The temperature profile along the y direction above the heater CENTER is calculated numerically and compared with the measurements performed with the pixel matrix. The results are detailed in

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Figure 4.46. It can be seen that the temperature profile from the FEM modelling matches well the experimental measurements at steady state. Subsequently, the 93D demonstrator will be used to carry out a dynamic study of heat dissipation within the pixel matrix.

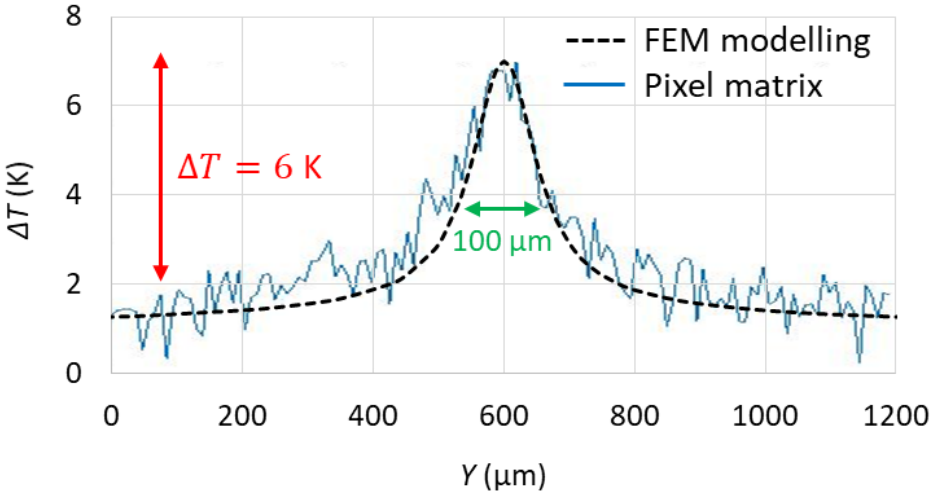

Figure 4.46: Temperature profile from the measurements with the pixel matrix at steady state along the y direction above the heater CENTER and comparison with the FEM modelling.

IV.2. Numerical analysis of transient heat dissipation

In this section, a numerical analysis of transient heat dissipation is carried out with FEM modelling. It aims to determine the pixel relaxation time and the transient temperature field at the pixel array level. This numerical study is performed under the same conditions as those used experimentally.

IV.2.A. Calculation of the pixel relaxation time

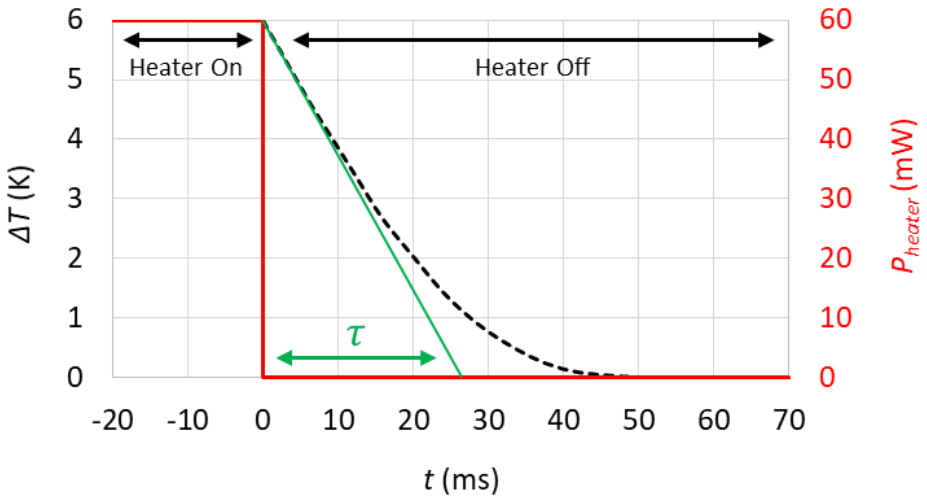

Figure 4.47: Transient temperature evolution calculated with FEM on the pixel array surface as a function of time after switching off the heater CENTER.

In order to represent the experimental conditions of the Section III.2.B.c., the power generated by the heater element P_{heater} is now a function of time. P_{heater} is set to 60 mW when $t \leq 0$ and $P_{heater} = 0$ when $t > 0$. Here, it is assumed that the heater is turned off instantly i.e. with a time constant equal to 0. The temperature amplitude above the heater CENTER is calculated in Figure 4.47 as a function of time. The time constant of the switching off of the heater CENTER τ is found equal to 25 ms. In addition, it can be seen that the temperature amplitude decays in 40 ms. Considering L_{die} the characteristic

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length of the bottom die (equal to 750 µm) and D_{die} the diffusivity of the bottom die (equal to 88 µm².s^{-1}), a time constant τ of the system L_{die}^2/D_{die} is found approximately equal to 60 ms. The FEM model is therefore in fair agreement with the measurements of transient heat dissipation. Furthermore, this analysis shows that the dynamics of the pixel is directly related to the thickness of the bottom die. The thinner the bottom die, the faster the thermal response of the pixel.

IV.2.B. Transient temperature field at the pixel array level

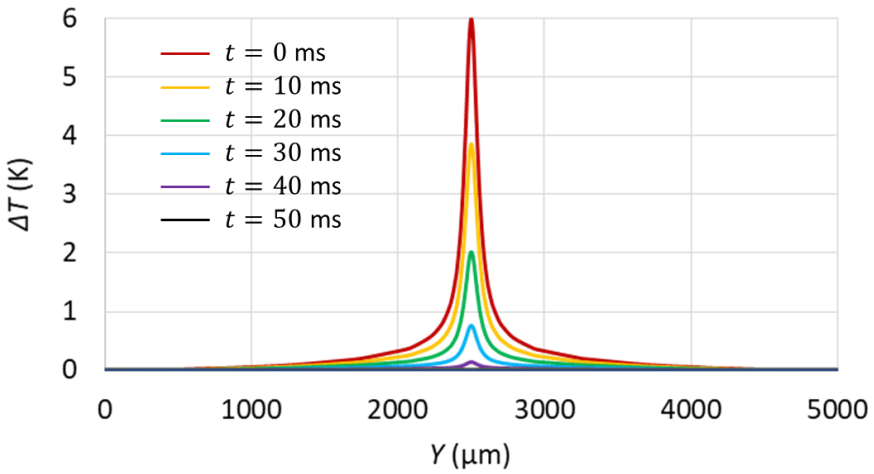

Figure 4.48: Transient temperature profile calculated with FEM on the pixel array surface along the y direction after switching off the CENTER heater.

The transient FEM modelling of the 93D chip is used to calculate the heat dissipation at the level of the pixel array. The temperature field is calculated between 0 and 50 ms along the y direction after having switched off the heater. The temperature rise profile above the heater CENTER is shown in Figure 4.48 as a function of the time. For each time step, the temperature amplitude and the full width at half maximum (FWHM) can in principle be calculated according to Green's functions [27].

In addition, in the case of transient heat transfer modelling, the domain size is fixed by the temperature accuracy constraints. For the 93D chip, the computed domain area S_{die} (in the xy plan) can be reasonably limited to a lower die surface. The difference of temperature calculated between $S_{die} = 40$ mm² and $S_{die} = 1$ mm² is shown in Figure 4.48. With a reduced computed domain area S_{die}, the temperature difference is found under 0.3 K which represent an error of under 5%.

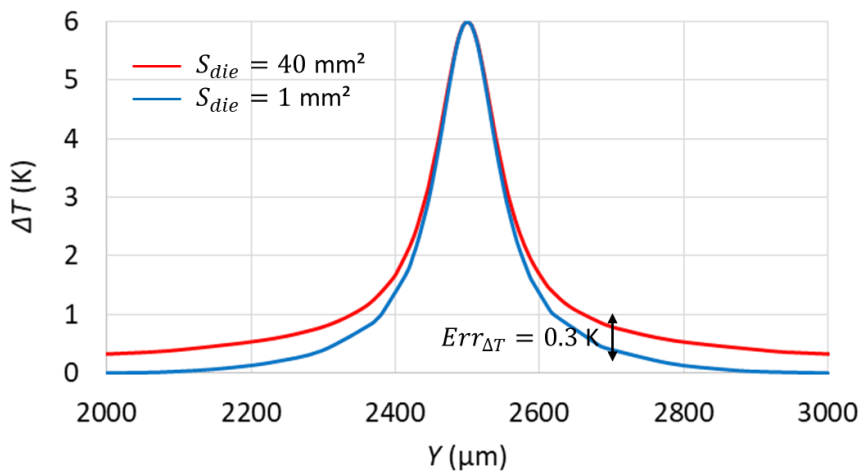

Figure 4.49: Temperature profiles calculated with FEM on the pixel array surface along the y direction above the heater CENTER. Comparison between $S_{die} = 40$ mm² and $S_{die} = 1$ mm² at $t = 0$.

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IV.3. Discussion

A quite fair agreement is found between experimental and numerical results. The order of magnitude is well respected and trends are similar. Once again, this can be explained by the boundaries conditions which drive the thermal behavior of the package. Moreover, the large difference in terms of material diffusivity allows to evaluate more easily the main trends in a transient regime. These preliminary results give thus good confidence for further investigations.

Generally speaking, the signal processing (face or object recognition...) is a highly transient phenomenon and it may be interesting to evaluate the thermal field in such regime. By considering only steady state, results may tend to be overestimated and consequently, limiting design capabilities. Transient simulation may provide results more consistent with the reality.

V. Conclusion

		FLAMINGO	93D
BEOL	Pixel matrix Top chip Bottom chip	Inactive I140 C40	Active I110 C40
Heater	Level Technology Power Surface	C40-M1 Copper serpentine 280±10 mW 140x200 µm²	C40-FEOL Grid of transistors 60±5 mW 43x35 µm²
Sensor	Level Technology Power Surface	I140-M1 Copper serpentine 9±0.3 mW 5x9 µm²	C40-FEOL PTAT sensor < 200 µW 9x20 µm²
Heat path	Sink Air	90.9% 9.1%	97.7% 2.3%

Table 4.10: Properties of the FLAMINGO and 93D chips.

In this chapter, two complex 3D HB imagers have been studied: the FLAMINGO and the 93D chips. The BEOL and the thermal structures of the chips have been described for both FLAMINGO and 93D chips (see Table 4.10).

First, the FLAMINGO test chip has allowed characterizing the heat transfer at both die and pixel levels. The heaters and sensors of the M1 levels of the C40 and I140 chips are used to generate heat dissipation across the stack. The FEM modelling of the FLAMINGO test chip has revealed that:

(i) temperature is mainly driven by the losses though air and the heat sink conductance at steady state. Radiation seems negligible for heat dissipation;

(ii) the temperature of the pixel is equal to the temperature of the BEOL;

(iii) the temperature pattern generated on the pixel array is almost three times larger than the heater width (located in the C40 FEOL) due to heat spreading in the BEOL;

(iv) the temperature measurements in the M1 and M1X levels being close, it shows that the HB interfaces do not play a significant role on heat dissipation.

Finally, by means of the FLAMINGO chip, it has been shown that the SThM technique (with the Wollaston micro-probe) can be used to perform thermometry measurement on an active sample at both millimeter and micrometer scales with the mapping and imaging methods, respectively.

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A final study has been performed on the 93D chip. It has been chosen to characterize the optical performances of the pixel according to the temperature variations. The pixel output signal in the dark (dark current) has been calibrated as a function of temperature. The pixel matrix could be used as a thermal sensor with a spatial resolution equal to 1.75 µm. This has allowed to highlight that:

(i) the dissipation time constants associated to the die and the package of 93D are found equal to 5 and 220 s, respectively;

(ii) the thermal dynamics of the pixel is mainly limited by the bottom die thickness. The thinner the bottom die, the faster the pixel dynamic can be;

(iii) Fair agreement with simple numerical approach.

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VI. Bibliography

[1] C. Sart, Thermomechanical Simulations and Experiments on 3D Stacking for Imaging, PhD thesis, Université Grenoble-Alpes, 2019.

[2] Y. Kitamura et al., Suppression of Crosstalk by Using Backside Deep Trench Isolation for 1.12µm Backside Illuminated CMOS Image Sensor, International Electron Devices Meeting, 2012.

[3] F. Bondu and J.Y. Vinet, Mirror thermal noise in interferometric gravitational-wave detectors, Physics Letters A, Volume 198, Issue 2, Pages 74-78, 1995.

[4] E. Welsch et al., Absolute Measurement of Thermophysical and Optical Thin-Film Properties by Photothermal Methods for the Investigation of Laser Damage, International Journal of Thermophysics, Volume 20, Issue 3, Pages 965-976, 1999.

[5] M.M. Fejer et al., Thermoelastic dissipation in inhomogeneous media: loss measurements and displacement noise in coated test masses for interferometric gravitational wave detectors, Physical Review D, Volume 70, Issue 8, Pages 1-19, 2004.

[6] Z.L. Wu et al., Absorption and thermal conductivity of oxide thin films measured by photothermal displacement and reflectance methods, Applied Optics, Volume 32, Issue 28, Pages 5660-5665, 1993.

[7] A. Sood et al., Thermal Characterization of Nanostructured Superlattices of TiN/TaN: Applications as Electrodes in Phase Change Memory, Proceeding of ITHERM, 2014.

[8] S.M. Lee and D.G. Cahill, Heat transport in thin dielectric films, Journal of Applied Physics, Volume 81, Page 2590, 1997.

[9] S.H. Lee et al., Thermal conductivity of tungsten-copper composites, Thermochimica Acta, Volume 542, Pages 2-5, 2012.

[10] F. Savar et al., PCB Glass-Fibre Laminates: Thermal Conductivity Measurements and Their Effect on Simulation, Journal of Electronic Materials, Volume 19, Issue 12, Pages 1345-1350, 1990.

[11] R. Girard-Desprolet, Plasmon-based spectral filtering with metallic nanostructures for CMOS image sensors, PhD Thesis, Université Grenoble-Alpes, 2015.

[12] P. Nath and K.L. Chopra, Thermal conductivity of copper films, Thin Solid Films, Volume 20, Issue 1, Pages 53-62, 1974.

[13] J.H. Kim et al., Application of the three omega thermal conductivity measurement method to a film on a substrate of finite thickness, Journal of Applied Physics, Volume 86, Page 3959, 1999.

[14] A. Feldman, Algorithm for solution of the thermal diffusion equation in a stratified medium with a modulated heating source, High Temperatures. High Temperatures, Volume 31, Page 293, 1999.

[15] M. Bogner et al., Differential 3ω method for measuring thermal conductivity of AlN and Si_3N_4 thin films, Thin Solid Films, Volume 591, Pages 267-270, 2015.

[16] T. Yamane et al., Measurement of thermal conductivity of silicon dioxide thin films using a 3ω method, Journal of Applied Physics, Volume 91, Page 9772, 2002.

[17] A. Al Mohtar et al., Thickness-dependent thermal properties of amorphous insulating thin films measured by photoreflectance microscopy, Thin Solid Films, Volume 642, Pages 157-162, 2017.

[18] A. Delan et al., Thermal conductivity of ultra low-k dielectrics, Microelectronic Engineering, Volume 70, Issues 2-4, Pages 280-284, 2003.

[19] F. Chen et al., Measurements of effective thermal conductivity for advanced interconnect structures with various composite low-k dielectrics, Proceeding of IRPS, 2004.

[20] D. Ney et al., Analytical extraction of thermal conductivities of low k dielectrics for advanced technologies, Proceeding of IIRW, 2004.

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[21] C.Y. Ho et al., A Continuing Systematic Program on Data Tables of Thermophysical and Electronic Properties of Materials, TEPIAC, Volume 2, Page 145, 1979.

[22] J. Taine et al., A first course in heat transfer, Dunod, Page 288, 2011.

[23] P.O. Chapuis, Contribution à l'étude des transferts thermiques à l'échelle nanométrique : interaction pointe-surface, PhD thesis, Ecole Centrale Paris, 2007.

[24] P.G. Reddy and N. Gupta, Material Selection for Microelectronic Heat Sink: An Application of the Ashby Approach, Materials and Design, Volume 31, Issue 1, Pages 113-117, 2010.

[25] M. Szermer and A. Napieralski, The PTAT sensors in CMOS technology, Proceeding of CAS, 2005.

[26] G.C.M. Meijer, Thermal sensors based on transistors, Sensors and Actuators, Volume 10, Issues 1-2, Pages 103-125, 1986.

[27] D.W. Hahn and M.N. Özisik, Heat Conduction, 3rd Edition, Use of Green's function for solution of heat conduction problems, Pages 300-349, 2012.

[28] A. Pelamatti, Estimation and modeling of key design parameters of pinned photodiode CMOS image sensors for high temporal resolution applications, PhD thesis, Université de Toulouse, 2015.

[29] E.R. Fossum and D.B. Hondongwa, A Review of the Pinned Photodiode for CCD and CMOS Image Sensors, IEEE Journal of the Electron Devices Society, Volume 2, Issue 3, Pages 33-43, 2014.

[30] N. Teranishi, Dark Current and White Blemish in Image Sensors, Proceeding of VLSI-TSA, 2013.

[31] A. Sellai, Temperature Dependence of Dark Current in a Si-pin Photodiode, Proceeding of ICSE, 2008.

[32] R. Widenhorn et al., Temperature dependence of dark current in a CCD, Proceedings of SPIE, 2002.

[33] W. Jaber and P.O. Chapuis, Non-diealities in the 3ω method for thermal characterization in the low- and high-frequency regimes, AIP Advances, Volume 8, Issue 4, Pages 1-13, 2018.

[34] V. Casalegno et al., Measurement of thermal properties of a ceramic/metal joint by laser flash method, Journal of Nuclear Materials, Volume 407, Issue 2, Pages 83-87, 2010.

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Conclusions and prospects

We first recall the main points addressed in this manuscript and then indicate some directions for future work.

In the first chapter, a brief state of the art in microelectronic fields related to the topics of this thesis, i.e. hybrid bonding and imagers, has been sketched up. In a first step, the general structure of an electronic chip, the physical principles of the transistor and the photodiode (PPD) have been introduced. In addition, the methods and materials for the interconnection of transistors have been also introduced. In particular, a focus has been made on the three-dimensional hybrid bonding imagers (3D HB IMG). The principle of 3D integration involving 3D Back-Side-Illumination and the hybrid bonding (HB) technology, where two chips are connected, have been underlined. Finally, two imaging technologies based on Complementary Metal Oxide Semiconductors (CMOS) and Charge Coupled Devices (CCD), embedded in 3D stacks of ICs, have been detailed. Today, the HB technology and CMOS image sensors have become widespread and require in-depth thermal studies to optimize their performances. In a second step, an inventory of the thermal constraints induced in these technologies has been drawn. Different temperature-related issues such as thermomechanical stress, dark current increase and electromigration have been detailed. Finally, various numerical and experimental methods for the characterization of the thermal behavior of integrated circuits (ICs) have been introduced. Among all these methods, a selection has been made for use in this PhD work.

In Chapter 2, two different thermoresistive techniques have been used for the thermal characterization of thin-film based materials: Scanning Thermal Microscopy (SThM) and the 3ω method. The SThM technique has been implemented with two different probes: the palladium nano-probe and the Wollaston micro-probe. It has been shown that the characterization of wafer-large samples with thermal conductivity higher than 1 $W.m^{-1}.K^{-1}$ is not possible with the SThM palladium nano-probe. This is due to the uncertainty on the characterization of the thermal contact between the probe and the sample. Unfortunately, for the thin layers available in this work, their effective thermal conductivities has revealed to be too large to be characterized with acceptable accuracy. The Wollaston micro-probe has been used in a second step, with a technique where the thermal signal measured with the probe is first calibrated as a function of the thermal conductivity of reference samples. The comparison between the thermal signal measured on thin-layer samples and the calibration has allowed determination of their effective thermal conductivities which are found equal to 0.6 and 0.1 $W.m^{-1}.K^{-1}$ for the BD1 and ULK samples, respectively. Finally, the property of each layer has been deduced by using a Finite Element Method (FEM) model of the probe-sample system. In the case of the measurements realized on low-k samples, their effective thermal conductivities have been found close to typical values of literature. In order to confirm certain values, the 3ω method has been implemented, which requires first fabrication (photolithography in clean room) of devices before experimental characterization can be performed. Measurements have been realized on SiO_2, SiN and SiCN materials, and the intrinsic thermal conductivities have been found to be in excellent agreement with the literature. The advantages and drawbacks of each technique could be evaluated as a result of all the characterizations. The 3ω method is very accurate but time consuming whereas the SThM technique, although less accurate, is much faster to implement.

In the third chapter, a numerical approach has been developed to evaluate the self-heating phenomena in 3D HB architectures. To do so, a test chip has been first considered. This chip is a passive device with copper serpentines that generate heat to represent an equivalent to the power generation in the Front-End-Of-Line (FEOL) of a commercial chip. FEM modelling has been chosen to obtain the

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whole temperature field in the chip. In order to overcome the FEM mesh constraints related to large aspect ratios and maintaining computational demand at reasonable cost, the thermal conductivity of the Back-End-Of-Line (BEOL) structure has been homogenized. Various EMA models have been considered: parallel and series fluxes, Maxwell-Garnett and Maxwell-Bruggeman. Interestingly, it has been found that thermal boundary resistances can be neglected in the BEOL materials since their impact is small in front of the thermally-insulating layers. The parallel and series thermal conductance models have proven to be consistent and convenient for the modelling of the BEOL. In order to validate the FEM model, the numerical data have been compared to experimental measurements directly operated on the chip top surface. To do so, two techniques, SThM and infrared (IR) thermometry, were chosen. In order to measure the temperature of the chip activated in real time inside the measuring instruments, a homemade electronic test bench involving a PCB holder has been developed. Using this setup, temperature measurements have been realized with SThM (both palladium and Wollaston probes) and with IR thermometry (THEMOS instrument). The temperature measurements performed with SThM and IR thermometry have been found in agreement within an uncertainty of 2 K and the SThM thermometry coefficient, the ratio of the measured tip temperature to the surface temperature, has been found to be equal to 0.50 and 0.30 for the palladium and Wollaston probes, respectively. A numerical FEM model of the 3D HB test chip has been developed and calibrated experimentally, allowing the temperature field in the chip volume and over the chip surface to be obtained. This has allowed showing that heat dissipation is limited due to the difficulty of dissipating heat though the sink, with a weak thermal conductance of few hundreds of $W.m^{-2}.K^{-1}$, and the losses through air, limited to about 10 $W.m^{-2}.K^{-1}$. The influence of the radiative heat losses have been considered also by calculating them as a function of the chip emissivity, but the radiative heat transfer is moderate and can be therefore included in the heat sink conductance. For this test chip, the temperature calculations have been validated experimentally with both SThM and IR thermometry measurements at the die level. Hence, the relevancy of such numerical strategy has been confirmed and gives confidence for next studies.

In Chapter 4, two new 3D HB imagers (respectively FLAMINGO and 93D) have been studied, involving successive cases where the pixels are inactive (test chip) or active (chip close to commercial device). The level of complexity of the BEOL and the thermal structures of the chips is higher in these imagers, which has required a detailed description. The FLAMINGO test chip has allowed characterizing heat dissipation at both die and pixel levels. The test resistive elements acting as heaters and sensors have been embedded in a metal level (M1) of the two chips connected by HB (C40 and I140 chips) in order to generate heat dissipation across the stack. The FEM modelling of the test chip has revealed that the BEOL temperature is homogeneous in the z direction with a very weak thermal gradient, which leaves little margin for the optimization of the temperature field within the BEOL materials. Again, it has been found that the heater temperature is mainly due to the bottlenecks associated to the heat sink conductance and the air losses at steady state. On the experimental side, it has been shown that the SThM technique (with the Wollaston micro-probe) can be used to perform thermometry measurement on an active sample at both millimeter and micrometer scales by means of tip motion with millimeter-size motors (“mapping”) and usual piezoscanning (“imaging”), respectively. A final study has been performed on the 93D chip to characterize the optical performances of the pixel, with an activated pixel array (unlike FLAMINGO). The pixel output signal in the dark (dark current) has been calibrated as a function of temperature. The pixel matrix has been used as a thermal sensor with a pixel-limited spatial resolution equal to 1.75 µm. This has allowed highlighting that for a BEOL temperature higher than 80 °C, the temperature rises generated by the FEOL heating elements have a significant impact on the image quality. In addition, it has been shown that the thermal dynamics of the pixel is mainly limited by the bottom die thickness. The thinner the bottom die, the faster the pixel dynamic can be.

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The next generation of imagers, with potential reduced pixel size and even more compact heat sources associated with logic and memory, will benefit from the current analysis. It is key to note that the temperature field is not necessarily perfectly homogeneous due to the environment of the pixel matrix: care should be paid to the design and positions of the surrounding elements. In favorable cases, as when connecting pads are located close to the matrix, these can decrease temperature locally.

In the future, thanks to the experimental developments of this PhD thesis, the SThM and 3ω method could be used more efficiently in order to continue the characterization of specific materials. For example, determining the static and transient properties of inhomogeneous materials involved in ICs and electronic packages, such as Thermal Interface Materials (TIMs), would allow more accurate steady-state and transient heat transfer modelling at the die and package levels. Indeed, since the heat flux is mainly dissipated toward the sink, the thermal properties of TIMs will have to be considered imperatively to calculate a reliable temperature field in the chip and in the package. This is all the more important in the case of 3D hybrid bonding imagers where the heat flow must be evacuated toward the sink to protect the performance and reliability of the pixel matrix.

An important challenge of microelectronics is to understand heat dissipation and hotspot effects at the scale of the FEOL, especially at the scale of the transistor. A coupled analysis between the experimental techniques and the numerical models developed in Chapter 3 could help in this direction. In particular, the SThM technique could be used to probe the surface temperature of a test device with optimized spatial resolution. Measurements with probes with a very small radius of curvature could be performed under vacuum conditions, as already done by some colleagues at IBM. The Si-doped nano-probe could be used for this purpose, and extended for measurements from the transistor level to the package level as developed in this thesis. It is important to note that for measurements at the nanometer scale, the tip-sample thermal contact must be characterized and the influence of the probe (e.g. heat sink effect) needs to be quantified. Thermoreflectance Thermal Imaging (TTI) technique could also be implemented, because of its better spatial resolution than infrared microscopy, in order to benchmark the capability of SThM. These experimental results could be used as references for the calibration of models at the transistor scale, where FEM is known to be limited. The FEM “macroscopic” models already developed in this PhD thesis at the level of the die would allow determine the loadings (boundary conditions: temperature and flux densities) which are necessary for the calculations of the temperature field at the mean-free path scale in multiscale modelling. It would be possible to develop innovative hybrid numerical models, mixing FE analysis and Boltzmann Transport Equation (BTE) resolutions.

The present analysis is mostly devoted to 3D hybrid bonding imager applications but the methods can be applied for many more applications, such as 3D TSV chips, 2D high-power technologies or Silicon-on-Chip (SoC) devices.

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Appendix: Acoustic and Diffuse Mismatch Models for Thermal Boundary Conductances

The Acoustic Mismatch Model (AMM) and the Diffuse Mismatch Model (DMM) have been traditionally used to calculate the Thermal Boundary Conductance (TBC) at interfaces [1]. In this Appendix, first, the principle of a TBC is explained. Then, the key parameters playing a role in TBCs are highlighted, and it is shown that they can be obtained from the phononic dispersion diagrams of the two media of the interface. Finally, the calculation of the TBC is detailed considering both the acoustic and diffuse phonon transmission at the interface. Conditions of applications of these theories are finally discussed.

Thermal boundary conductance

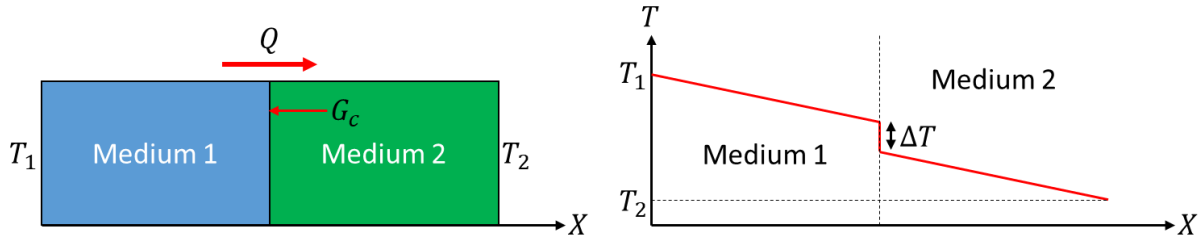

Figure A.32: Pictorial explanation of a thermal boundary conductance.

At the boundary between two media in perfect contact, an additional thermal conductance, not linked to a certain volume and called thermal boundary conductance (TBC), is often to be taken into account. A schematic of a TBC is shown in Figure A.1. At interfaces, the flux is always conserved, but temperature is not necessarily continuous despite the perfectness of the contact. A variation of temperature ΔT between both sides of the boundary can therefore be observed, related to the flux Q crossing the boundary, as follows

$$Q = G_c \Delta T, \tag{A.1}$$

where G_c is the TBC. G_c characterizes the capacity of the phonons of medium 1 to cross the boundary and to enter into medium 2. The influence of the boundary conductance (also called Kapitza conductance often, especially at interfaces between a liquid and solid) is all the greater as the bulk conductances are large. This has been highlighted by Pollak and Frederking in [2, 3].

Ingredients: Vibrational density of states and group velocities

Considering the heat transport as a phonon transport across the boundary, G_c is defined with

$$G_c = \lim_{\Delta T \to 0} \frac{Q}{\Delta T}. \tag{A.2}$$

G_c can be calculated as follows:

$$G_c = \sum_p \int_0^{\frac{\pi}{2}} d\theta \int_0^{2\pi} \sin\theta \, d\varphi \int_0^{\omega} d\omega . V_{gp}(\omega,\theta,\varphi) \cos\theta . \frac{D_{sp}(\omega,\theta,\varphi)}{4\pi} . \hbar\omega . \frac{\partial f(\omega,T)}{\partial T} \tau_{12p}(\omega,\varphi,\theta), \tag{A.3}$$

where θ and φ are the angles of incidence of the phonon (θ is the angle with the normal to the boundary) , ω is the angular frequency and $\hbar\omega$ is therefore the energy of a phonon mode, V_g is the

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group velocity and D_s is the density of states of the phonon in the medium 1. The sum is over the polarizations p and $f(\omega, T)$ is the Bose-Einstein equilibrium distribution function. A key ingredient in this formula is τ_{12}, the transmission coefficient at the interface between the medium 1 and medium 2 that will be detailed in the last section with the AMM and DMM theories. In the following, we restrict ourselves to isotropic media, where $V_g(\omega, \theta, \varphi) = V_g(\omega)$ and $D_s(\omega, \theta, \varphi) = D_s(\omega)$.

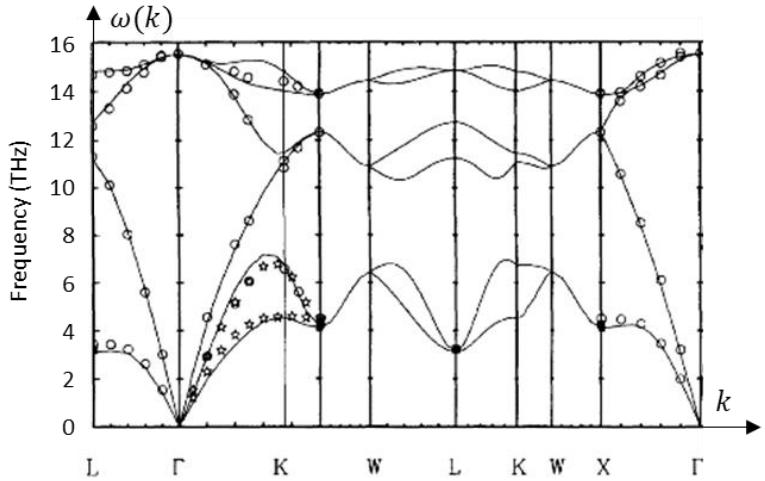

Figure A.33: Phonon dispersion relation for bulk silicon [4].

In Eq. (A.3), V_g and D_s are required for calculating G_c. These parameters are determined from the dispersion relations of each material. The atomic phonon dispersion of silicon, which is not isotropic, is shown in Figure A.2 [4]. As we have restricted ourselves to isotropic media, we consider the dispersion along ΓX and suppose it to be valid for all directions. It can be shown that the error committed over the volume of the Brillouin zone is small. For each polarization, the group velocity V_g is calculated from the dispersion relation by means of

$$V_g(k) = \frac{d\omega(k)}{dk}, \tag{A.4}$$

where k is the wave vector. Often, the phonon dispersion relation is approximated by a linear relationship (Debye approximation). This is accurate for wave vectors close to the center of the Brillouin zone, but deviates from the true result for wave vectors near the zone edges. Here, the real phonon dispersion is taken into account over the entire Brillouin zone (along the ΓX axis). The density of states D_s is then deduced as follows

$$D_s(\omega) = \frac{3}{2\pi}\frac{k^2}{V_g(k)}, \tag{A.5}$$

These calculations can be carried out for all the phonon modes: TA (transverse acoustic) and LA (longitudinal acoustic) ones, but also for the TO (transverse optic) and LO (longitudinal optic) ones. The results for silicon are shown in Figure A.3 for the acoustic modes, which are those considered for heat conduction (optical modes will be neglected in the following). Here the experimental dispersions have been fitted to quadratic laws with the restriction that the group velocity cannot change sign (which is the case for materials used in Chapter 2). This induces a van Hove singularity (which is integrable) for the TA mode as seen in Figure A.3.b).

Considering V_g and D_s calculated for the two media in contact, the transmission coefficient τ_{12} at the boundary is to be defined to determine the conductance G_c.

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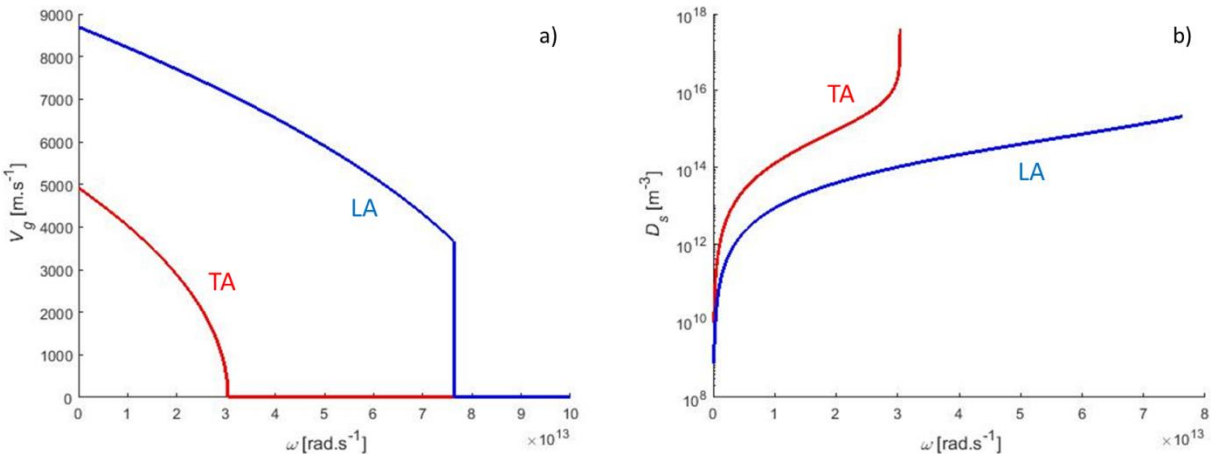

Figure A.34: Calculation of a) group velocities and b) densities of states for both TA and LA phonon modes of propagation in silicon as a function of the circular frequency.

Phonon transmission coefficient

The phonon transport through a boundary can take place in various ways, and so the transmission coefficient τ_{12} can be estimated with various models. In this work, τ_{12} is computed from the two following models:

(i) Acoustic Mismatch Model (AMM): the phonon wavelength is estimated much larger than the microscopic details of the interface (including the atomic lattice size) and the interface between the two materials is supposed perfectly flat. The transmission is "specular".

(ii) Diffuse Mismatch Model (DMM): the phonon wavelength is of the same order as the characteristic lengths of the interface, i.e. the out-of-plane root mean square deviation to the average plane of the interface, the transverse correlation length of the microscopic details of the interface, which are two parameters related to roughness, or simply the atomic lattice size. This model assimilates the interface as so rough that one cannot distinguishes phonons reflected by the interface and those transmitted. The transmission is called "diffuse".

The principle of the AMM and DMM theories is explained in Chapter 1 Section III.3. The relevance of using AMM and DMM for the calculation of TBC has been well highlighted by Cheeke et al. in [5] and Swartz and Pohl in [6]. The computation of the transmission coefficient τ_{12} in both AMM and DMM theories is further detailed in the next section.

Acoustic Mismatch Model

All the phonons are specularly scattered or transmitted at the interface. The transmission coefficient is calculated at each incident angle and for the three polarizations modes l (longitudinal), t_1 (transverse horizontal) and t_2 (transverse vertical). In isotropic solids, the polarizations t_1 and t_2 are degenerated. The transmission coefficients in amplitude are calculated with acoustic Fresnel equations respecting the two conditions of velocity and stress continuity at the interface. The equations are precisely described by G. Chen and can be found in [7]. For example, the transmission coefficient between t_2 modes $\tau_{12}[t_2 \rightarrow t_2]$ is calculated as follows

$$\tau_{12}[t_2 \rightarrow t_2] = \left|\frac{2\rho_1 V_g^1 \cos\theta_1}{\rho_1 V_g^1 \cos\theta_1 + \rho_2 V_g^2 \cos\theta_2}\right|^2 \frac{\rho_2 V_g^2 \cos\theta_2}{\rho_1 V_g^1 \cos\theta_1}, \quad \text{(A.6)}$$

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$$\sin\theta_1 = \frac{\rho_1 V_g^1}{\rho_2 V_g^2}\sin\theta_2 = \sin\theta, \tag{A.7}$$

where ρ_i is the density and θ_i is the angle of incidence of the phonon for each medium. For all polarizations, the transmission coefficient calculated in AMM are given in Figure A.4 for the silicon/germanium interface. It is interesting to observe that there is strong angle dependence in this model. Note that simplified versions of the AMM coefficients due to Khalatnikov [8] are usually applied in literature (see e.g. [9-11]). Here, in order to maintain the angle, frequency and polarization dependence, the coefficients have been calculated following Cheeke et al. [5] within the full theory. In the Debye approximation, the TBC G_c is found equal to 283 MW.m^{-2}.K^{-1} at 300 K.

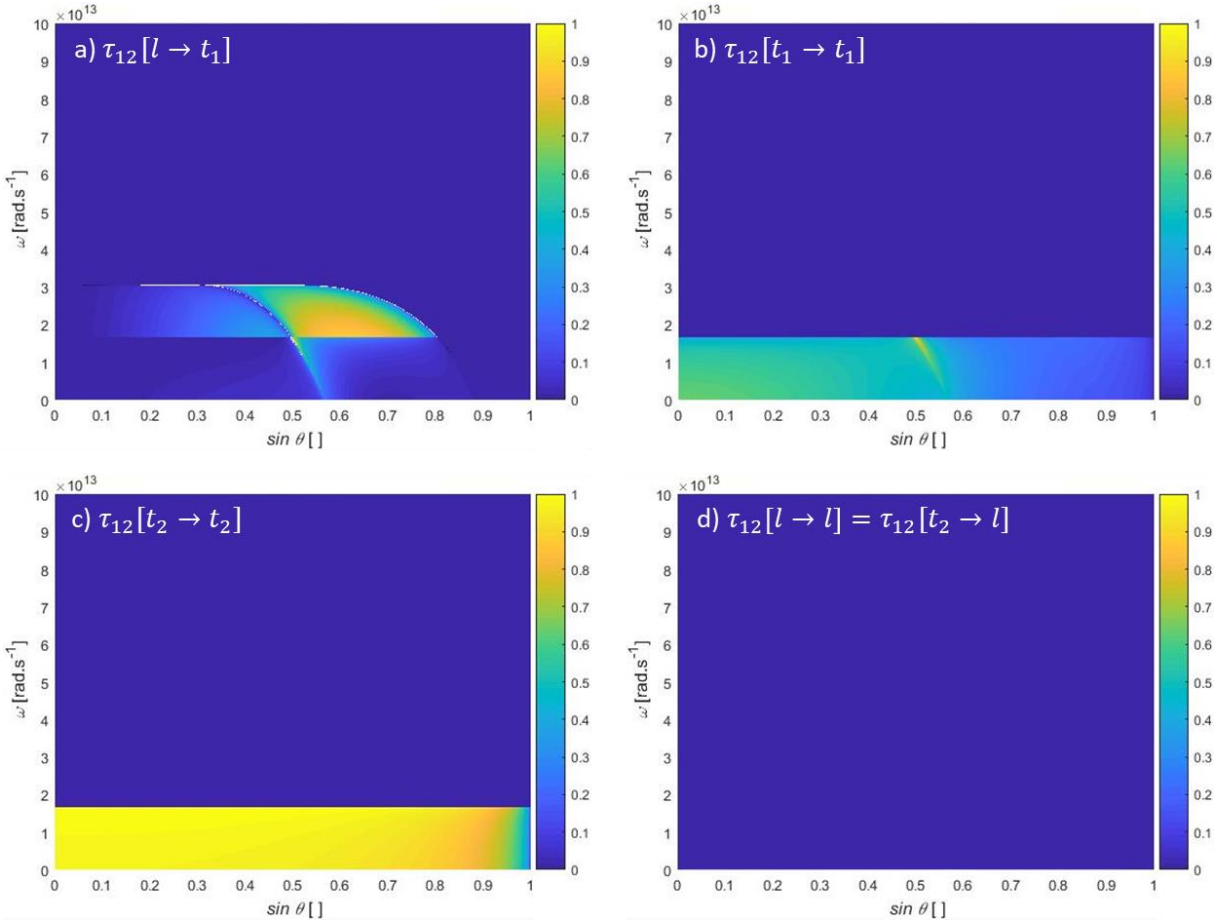

Figure A.35: Transmission coefficient between silicon and germanium calculated in AMM as a function of the incident angle and the circular frequency for each polarization.

Diffuse Mismatch Model

All the phonons are diffusely scattered at the interface. The transmission coefficient is calculated at each frequency and for the three polarizations l, t_1, and t_2. In isotropic solids, the polarization modes t_1 and t_2 are degenerated. τ_{12} is calculated as follows:

$$\tau_{12}(\omega) = \frac{\sum_p V_g^1(\omega) D_s^1(\omega)}{\sum_p V_g^1(\omega) D_s^1(\omega) + \sum_p V_g^2(\omega) D_s^2(\omega)}, \tag{A.8}$$

$$p = l, t_1, t_2,$$

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where V_g^i and D_s^i are respectively the group velocity and the density of states in the medium i. An example of transmission coefficient calculated in DMM is given in Figure A.5 for the silicon/germanium interface. The TBC G_c is found equal to 346 MW.m^{-2}.K^{-1}.

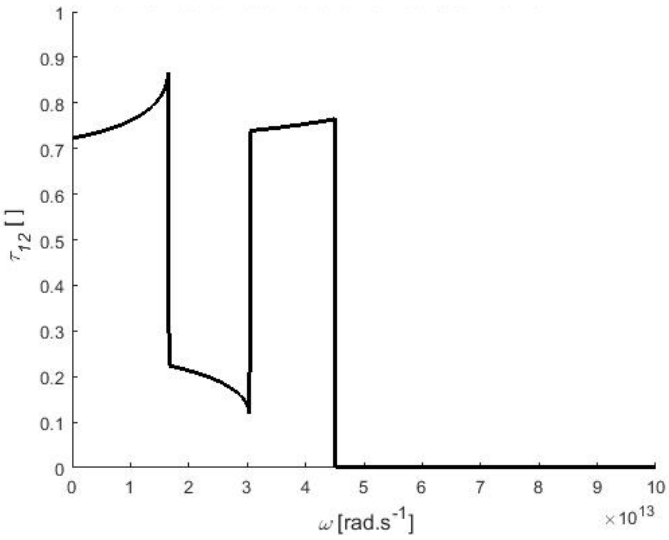

Figure A.36: Transmission coefficient between silicon and germanium calculated in DMM as a function of the circular frequency.

Application to non-crystalline media

The velocities and densities of phonon states can be determined according to the previous paths only if the dispersion diagrams are well defined. For amorphous or liquid materials, further assumptions are required.

For amorphous solids, the dispersion is not well defined if the frequency becomes larger than that associated to the Ioffe-Regel criterion (relaxation time faster than inverse frequency, i.e. oscillation period, see [12]). While it is possible to determine a vibrational density of states (as was shown for instance from molecular dynamics), it is not the case anymore for the group velocity. To avoid such issue, a linear Debye dispersion for the materials is considered for amorphous solids, both for the longitudinal and transverse modes (that have different velocities). This allows following the procedures described below both for the AMM and DMM theories. An estimation of a TBC can be obtained as result.

In order to determine a thermal boundary conductance between a solid and a liquid (called Kapitza conductance), the AMM and DMM theories can be used. Liquids are assumed without transverse polarization, having only one longitudinal polarization. The group velocity of the longitudinal polarization in liquid is assumed to be the speed of sound, i.e. the dispersion is supposed linear. To determine the Kapitza conductance, the principle is the same as the one explained for solids in contact but the transverse group velocities of the liquid are set to zero in order to account only for the longitudinal polarization.

Finally, let us mention that interfaces involving metals need in principle to be treated also in a different way, where the electron-phonon coupling in both materials and across the boundary are taken into account. This has not been the case in the present work, where only phonon/vibrational contributions were handled.

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Bibliography

[1] P. Reddy et al., Diffuse mismatch model of thermal boundary conductance using exact phonon dispersion, Applied Physics Letters, Volume 87, Issue 21, Page 1063, 2005.

[2] G.L. Pollak, Kapitza Resistance, Reviews of Modern Physics, Volume 41, Issue 1, Page 48, 1969.

[3] T.H.K. Frederking, Chemical Engineering Process Symposium, Volume 64, Issue 87, Page 21, 1968.

[4] S. Wei and M.Y. Chou, Phonon dispersion of silicon and germanium from first-principles calculations, Physical Review B: Condensed Matter and Materials Physics, Volume 50, Issue 4, Pages 2221-2226, 1994.

[5] J.D.N. Cheeke et al., Analysis of heat transfer between solids at low temperatures, Canadian Journal of Physics, Volume 54, Pages 1749-1771, 1976.

[6] E.T. Swartz and R.O. Pohl, Thermal boundary resistance, Reviews of Modern Physics, Volume 61, Issue 3, Pages 605-658, 1989.

[7] G. Chen, Nanoscale Energy Transport and Conversion: A Parallel Treatment of Electrons, Molecules, Phonons, and Photons, 1st Edition, Pages 178-185, 2005.

[8] I.M. Khalatnikov, An introduction to the theory of superfluidity, Nuclear Physics, Volume 78, Issue 3, Page 694, 1966.

[9] B.V. Budaev and D.B. Body, An extension of Khalatnikov's theory of Kapitsa thermal resistance, Annalen der Physik, Volume 523, Issue 3, Pages 208-225, 2010.

[10] R.E. Peterson and A.C. Anderson, Acoustic-mismatch model of the Kapitza resistance, Physics Letters A, Volume 40, Issue 4, Pages 317-319, 1972.

[11] R. Prasher, Acoustic mismatch model for thermal contact resistance of van der Waals contacts, Applied Physics Letters, Volume 94, Issue 4, Pages 1-3, 2009.

[12] S.E. Skipetrov and I.M. Sokolov, Ioffe-Regel criterion for Anderson localization in the model of resonant point scatterers, Physical Review B, Volume 98, Issue 6, Pages 1-8, 2018.

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DATE DE SOUTENANCE : 04/09/2019

PRENOMS : Axel, Pierre-Louis

TITRE : Numerical and experimental investigations of self-heating phenomena in 3D Hybrid Bonding imaging technologies

NATURE : Doctorat

NUMERO D'ORDRE : 2019LYSEI054

ECOLE DOCTORALE : MEGA de Lyon

SPECIALITE : Energétique/Thermique

RESUME : In this PhD thesis, self-heating phenomena are studied for guiding the design of next-generation 3D Integrated Circuits (ICs). By means of experimental and numerical investigations, associated heat dissipation in 3D Hybrid Bonding imager sis analyzed and the impact of the resulting temperature rise is evaluated. First, in order to develop accurate models, the thermal properties of materials used in ICs are to be determined. Different dielectric thin films involving oxides, nitrides, and low-k compounds are investigated. To do so, Scanning Thermal Microscopy (SThM) and the 3ω electrothermal method, sensitive to low and large effective thermal conductivity, are implemented. In a second step, finite-element models of 3D ICs are developed. A numerical method involving homogenization and a multiscale approach is proposed to overcome the large aspect ratios inherent in microelectronics. The numerical procedure is validated by comparing calculations and experimental measurements performed with SThM, resistive thermometry and infrared microscopy on a simplified Hybrid Bonding test chip. It is shown that heat dissipation is mainly limited by the heat sink conductance and the losses through air. Finally, numerical and experimental studies are performed on fully-functional 3D Hybrid Bonding imagers. The temperature field is measured with SThM and compared with finite-element computations at the die surface. The numerical results show that the temperature of the pixel surface is equal to that of the imager Front-End-Of-Line. The influence of the temperature rise on the optical performance of the imager is deduced from the analysis. The study also allows assessing the various numerical and experimental methods for characterizing heat dissipation in microelectronics.

MOTS-CLES : physics, thermal, nanoscience, microelectronic, integrated circuits, 3D, hybrid bonding, imager, temperature, thermal conductivity, heat transfer, thermal boundary resistance, thermal boundary conductance, Kapitza resistance, silicon dioxide, nitride, low-k, heat dissipation, hotspot, electromigration, cooling, scanning thermal microscopy, SThM, palladium, Wollaston, 3ω, infrared, thermoresistive, heater, sensor, Back-End-of-Line, BEOL, Front-End-of-Line, FEOL, photodiode, pixel, dark current, finite element modelling, FEM, multiscale, Acoustic Mismatch Model, AMM, Diffuse Mismatch Model, DMM.

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