Conception de déphaseurs de type réflectif millimétriques avec des moyens de test basé sur l'oscillation

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Design of mm-wave Reflection-Type Phase Shifters with Oscillation-Based Test capabilities

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“Aye, I suppose I could stay up that late”

James Clerk Maxwell

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INTRODUCTION

Phase shifters are devices used to change the relative phase of an RF signal without, ideally, modifying its magnitude or shape. Such devices can induce a fixed phase shift or a tunable one, which, in its turn, can be continuous or discrete. In the early years of electronics as we know them today, phase shifters were used to adjust the phase of a current to exactly oppose the interfering electromotive force (E. M. F) of transformers [1], enhancing their performance. However, they were rapidly adopted in the field of wireless communications for their capacity of directing the beam in the context of a phased array system [2]. A phased array, whose block diagram is depicted in Figure 1, is a system primarily composed by a set of n phase shifters receiving an RF signal with an input phase of φ_0, where each of them outputs an RF signal with a φ_i phase. The output signal of those phase shifters is subsequently fed into an antenna array that generates a beam pointing at a given spatial direction. The direction of the beam is a function of the relative phase shift existing between the RF signals feeding the antennas in the system. If tunable phase shifters are used and operated through a control signal (e.g. a control voltage V_{ctrl}), the generated beam can be steered to point at different spatial directions. Phased arrays lead to greater directivity and enhanced Signal-to-Noise Ratio (SNR), when compared to a traditional quasi-omnidirectional antenna. However, back in the 1930s, complicated and extremely cumbersome mechanical systems involving pulleys and ropes were used to steer the beam in the desired direction [3].

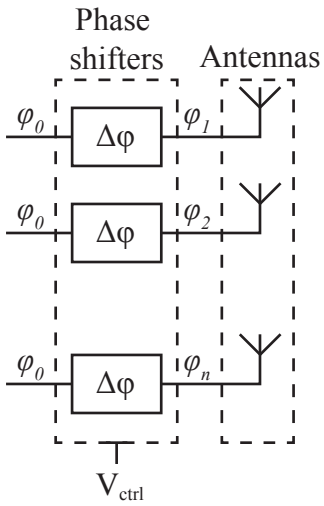

Figure 1 Block diagram of a phased array.

Next, with the advent of integrated circuits in the late 1950s and the development of integrated Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) the first integrated phase shifters were reported in the literature [4]. Nowadays, with the current spread of wireless communications in every aspect of our life (e.g. IoT, 5G, Wi-Fi…) phase shifters within a phased array are not only interesting because of the improved SNR but also because they lead to reduced power consumption, when compared to a quasi-omnidirectional antenna. This is a pretty straightforward effect: when the directivity of a beam is increased, a lesser amount of emitted power is required for an equal received power of a line-of-sight transmission. This is particularly interesting in the current scenario, where larger bandwidths are required to fulfill the ever-increasing data-rate demand. The desired increase in bandwidth can be achieved through an increase of the transceiver working frequency (in the mm-wave band). However, on-silicon transceivers working at greater frequencies struggle to deliver a great power output due to their proximity to the maximum operational frequency of transistors, f_{max}. For these reasons, such systems seem an unavoidable architecture in the future wireless telecommunication transceivers.

Tunable phase shifters can be built as passive or active devices. As a tunable phase shifter generally requires a control DC voltage, any of them can strictly be considered as passive devices. However, for this classification, let us use a looser sense for the *passive* category as it is generally understood. A tunable passive phase shifter is a type of phase shifter whose energy consumption is exclusively limited to the undesired leakage of the elements composing it.

Silicon-integrated passive phase shifters can be classified into three main categories: (i) switched-type, (ii) loaded-type and (iii) reflection-type. Switched-type phase shifters [5]–[7] use switching elements (e.g., transistors or diodes) to choose among different signal paths presenting particular phase shifts. This kind of phase shifters can be built using lumped elements (i.e., capacitors and inductors), as shown in Figure 2.a, or using transmission lines as shown in Figure 2.b.

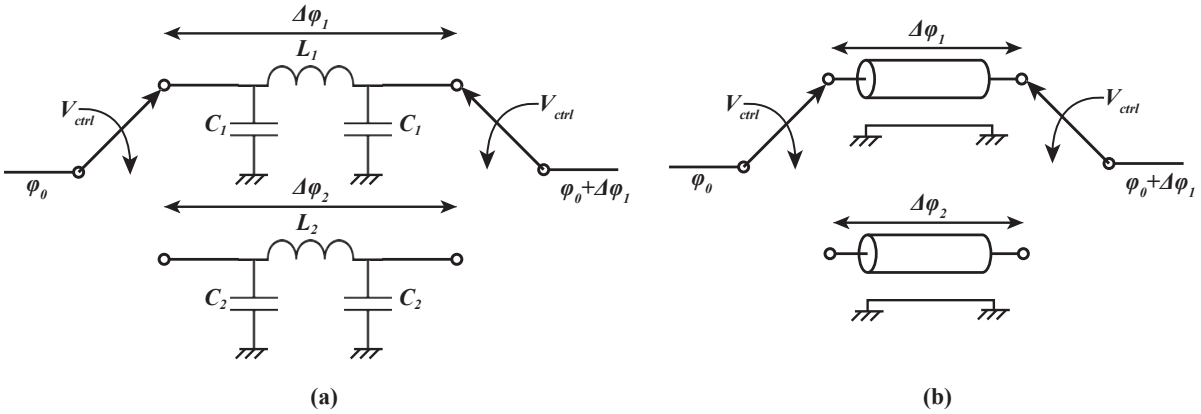

Figure 2 Examples of switched-type phase shifters based on: (a) two lumped-element cells and (b) two transmission lines.

Switched-type phase shifters present a discretely stepped phase shift at its output. The number of phase shifts that they can induce is a function to the number of cells they contain. It is straightforward to see that the main drawback of these systems is their area overhead when aiming at coarse phase shift steps. In addition, at mm-waves the performance of switches introduces important losses in the system of around 1.5 to 2 dB per switch [8], [9].

Another kind of phase shifter is the so-called loaded-type phase shifters [10]. This kind device, as depicted in Figure 3, can be built using lumped elements or transmission lines. The phase of the output is usually modulated in a continuous manner using integrated varactors. Moreover, replacing the varactors, switching elements as MOSFETs or PIN diodes can be used to switch between a set of reactances. Thus, obtaining a discrete phase shift [11].

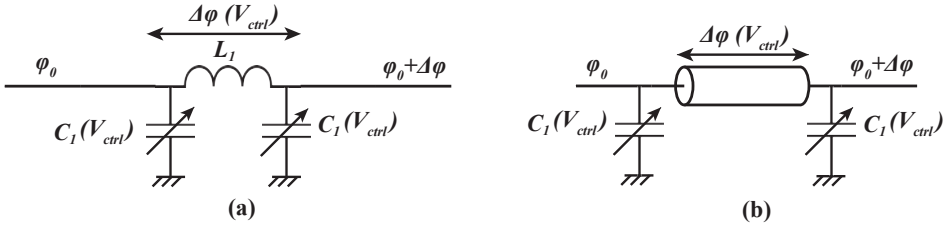

Figure 3 Examples of loaded-type phase shifters based on: (a) lumped elements and (b) transmission lines.

The loaded-line phase shifters have the advantage of allowing a continuous tuning of the output phase. However, the impedance seen at the input/output of these devices is greatly affected by the capacitance variation of the tunable device (e.g., varactor). Hence, for highly-tunable phase shifters poor return loss is obtained.

The last kind of widely used integrated phase shifters are the so-called Reflection-Type Phase Shifters (RTPS). These phase shifters are composed by two blocks: (i) a 3-dB coupler and (ii) a highly-reflective load placed at the coupled ports of the coupler. Figure 4 presents an RTPS using a 3-dB

coupler whose coupled ports are located at ports 2 and 3. In these ports, tunable loads are placed in order to reflect the signal back to the output port 4.

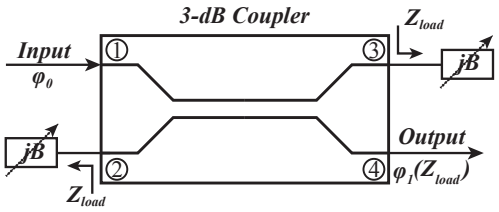

Figure 4 Reflection-type phase shifter using a 3-dB coupler whose coupled ports are located at ports 2 and 3.

These phase shifters, when integrated together with a highly-directive coupler have the advantage of presenting a return loss close to the directivity of the used coupler for any load impedance Z_{load}. For this reason, when using highly-directive coupler, this system presents low return loss in a wide band, making this architecture attractive for wideband applications. In addition, they allow to present a continuous phase tuning. However, the design of high-performance integrated 3-dB couplers and varactors at mm-wave frequencies remains an issue. In this manuscript, RTPS is the architecture-of-choice for the design of mm-wave phase shifters.

Phase shifters, as any other electronic device, are subject to manufacturing imperfections due to process variations and spot defects, such a short-circuit. In addition, these devices suffer from aging. These issues lead to a drift in the performance or, ultimately, to an inability of performing the phase shifting function. To assess the performance of these devices at the end of a production chain, functional test is carried out by foundries. However, note that the block diagram of a complete phased array, presented in Figure 1, is complex and composed of several phase shifters. Hence, functional test, usually consists in the evaluation of the whole phased array. In this scenario, it is hard to determine which phase shifter is eventually malfunctioning. Thus, any calibration scheme becomes difficult or just too complicated to carry out. Moreover, direct functional test is usually carried out at the end of the production chain. Hence, the aging of these devices is usually assessed by aging models and not by actual on-field measurements. Finally, the cost of functional test represents up to 50% of the manufacturing cost of a modern mobile System-On-Chip (SOC) [12]. In this scenario, Built-In Self-Test (BIST) approaches appear as a great solution, eventually leading to self-testability, self-calibration and self-healing schemes.

This manuscript presents the design and measurement results of a BIST approach based on the so-called Oscillation-Based Test technique.

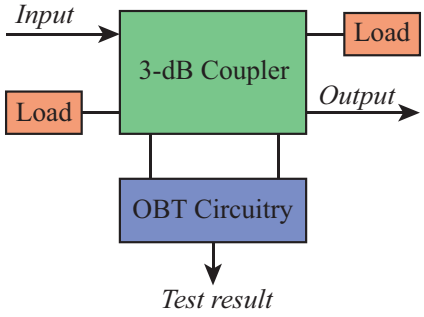

Figure 5 Block diagram of an RTPS with OBT circuitry.

This thesis discusses the design, practical implementation and measurement of every element in the block diagram presented in Figure 5 (i.e., 3-dB couplers, reflective loads, their combination for the RTPS design and the OBT circuitry for its test) in the context of on-silicon mm-wave phase shifters.

In order to study the elements presented in Figure 5, then the OBT as a whole, the present manuscript is divided into four Chapters and a conclusion. First, Chapter I describes the theory, practical design of mm-wave coupled-lines 3-dB couplers. The design of these couplers is based on the slow-wave concept, and the Coupled Slow-wave CoPlanar Waveguides topology is used. In this Chapter, a

thorough analysis of these couplers is carried out and a parametric electrical model is proposed together with the methodology to calculate the elements in the proposed model. Finally, on-silicon measurements of two 3-dB couplers are presented.

Next, Chapter II discusses the theory and requirements of varactors in the context of RTPS design. In addition, it also presents the current limitations of varactors in the mm-wave frequency band. For this reason, two innovative varactor topologies are proposed together with their measurements.

Then, Chapter III builds on the theory and practical measurements discussed in Chapters I and II, for the design of mm-wave RTPS. In this Chapter, the theory behind this architecture is presented. Then, three practical implementations of mm-wave RTPS are proposed and on-chip measurements are presented for two of them.

Chapter IV presents the theory and practical implementation of OBT for mm-wave phase shifters. In addition, the Chapter discusses silicon measurements showing that OBT is a viable technique for testing mm-wave RTPS. At the end of this Chapter, a possible extension is discussed, which eventually enables a BIST approach for the testing of mm-wave phased arrays, using OBT. The results presented in this Chapter open the door to on-chip self-calibration and self-testing schemes.

Chapter I

3-dB Couplers

Couplers are 4-port electronic devices that split the input signal into two waves with a certain power ratio between them. Broadly speaking any pair of 2-port elements in a circuit sharing an electromagnetic coupling could be considered as a coupler using this definition. However, this definition can be improved if the coupler is required to have isolation (i.e., a port of the coupler presents, ideally, a null amount of power). In this case, the coupler is said to be directive. For the sake of simplicity, all couplers discussed in this document are considered to be directive. Often, directivity is achieved for particular phase shifts between their high-power outputs, usually being $\pi/2$ (i.e., quadrature coupler) or π radians. Couplers are important blocks in RF applications, such as measurement systems (e.g. in Vector Network Analyzers), I/Q modulation, power splitting/combining, phase shifting… A special case of couplers is the 3-dB coupler, where the input signal is evenly divided between its two output ports. Quadrature 3-dB couplers can be classified into two main topologies: (i) the hybrid (or branch-line) coupler [13] and (ii) the coupled-lines coupler [14]. Even-though other topologies such as Lange Couplers [15] or Riblet short-slot couplers [16] exist, they will not be discussed in this manuscript as they are less suitable for integrated technologies. Finally, couplers can be built as symmetric or asymmetric devices. In this document, only symmetric couplers are considered.

This chapter is organized as follows, section I.1 presents the hybrid coupler architecture. Next, in section I.2 the advantages of the coupled-lines for the design of mm-wave are discussed. In addition, the theoretical basis for the understanding of this architecture is provided together with the state-of-the-art implementations of this architecture. Then, the CS-CPW architecture and its distributed electrical model is presented together with an analytical method for their simulation. Moreover, two practical implementations of the CS-CPW architecture are presented. Finally, the chapter is concluded in section I.3.

I.1. Hybrid couplers

The 3-dB hybrid coupler, whose architecture is depicted in Figure I-1.a, is composed of four transmission lines forming a square-like shape with a surface of around $\lambda_G^2/16$, where λ_G is the guided wavelength of the signal. If the ports are defined as in Figure I-1 and an ideal coupler is considered, an input at port 1 is then evenly split between ports 3 and 4, leading to a -3-dB power level at these outputs as compared with port 1. In addition, as this is a quadrature coupler, these two outputs, at the central frequency, present a 90º phase shift between them as seen from the input port.

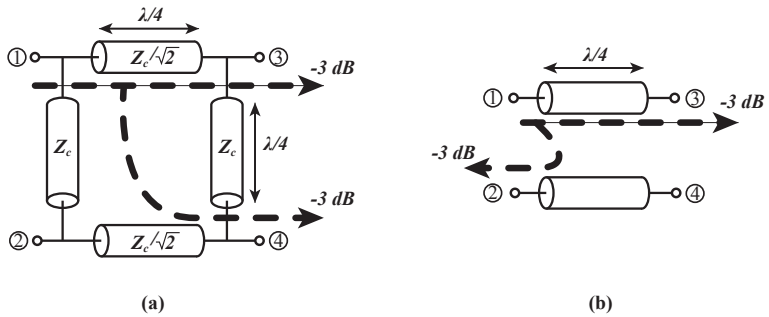

Figure I-1 Main architectures of ideal 3-dB couplers: (a) Hybrid-coupler and (b) Coupled-lines backward coupler.

The S-Parameter matrix of an ideal 3-dB hybrid coupler at its central frequency, f_0, with the ports numbered as in Figure I-1.a, is defined as:

$$[S] = -\frac{1}{\sqrt{2}}\begin{bmatrix} 0 & 0 & j & 1 \\ 0 & 0 & 1 & j \\ j & 1 & 0 & 0 \\ 1 & j & 0 & 0 \end{bmatrix}. \tag{I-1}$$

Hence, at the central frequency, an ideal hybrid-coupler shows a null return-loss and infinite isolation. In addition, the phase shift between its through and coupled ports (i.e., $\angle S_{31} - \angle S_{41}$) is equal to 90º. However, for wideband applications, the analysis of this coupler at its central frequency does not provide with enough information. In order to show broadband behavior, Figure I-2.a presents the S-Parameters of an ideal hybrid coupler with a f_0 of 100 GHz, from DC to 200 GHz. Figure I-2.a displays the magnitude of the S-Parameters as seen from port 1 and Figure I-2.b presents the phase shift between the through and coupled ports.

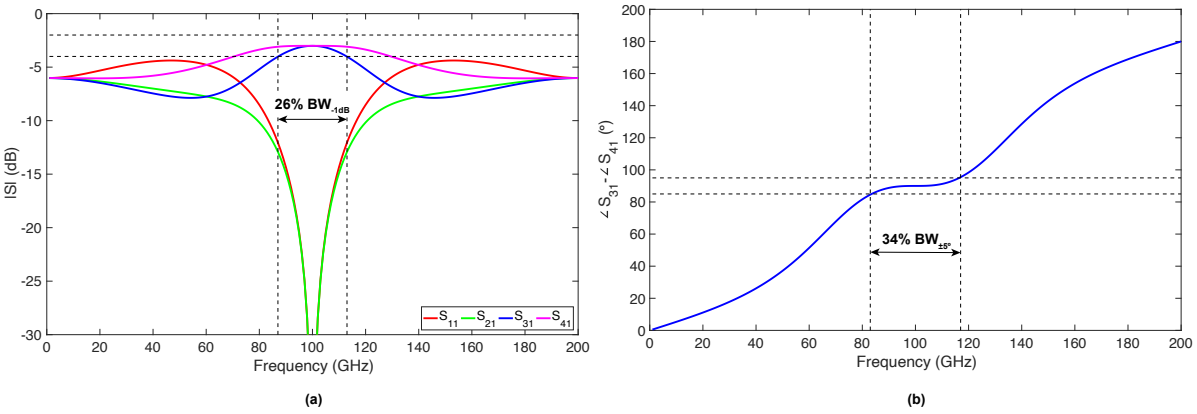

Figure I-2 S-Parameters of a 100-GHz ideal hybrid coupler vs frequency. (a) Magnitude (b) Phase difference at the outputs.

Although this coupler presents the advantage of having a relatively easy implementation in any given technology, its use in wideband applications is quite limited. One of the drawbacks comes from the fact that the coupled and the through port change their output power levels with different frequential slopes, when moving away from f_0. Systems needing a tight power imbalance might suffer from this issue. For instance, if the bandwidth of such a coupler is analyzed with the criterion of -1 dB at the through port, this coupler shows a 26% bandwidth. On the other hand, some systems are not so sensitive to a magnitude imbalance but are sensitive to a phase imbalance at the output (e.g. an I/Q modulator where the magnitude imbalance is dealt upstream). In this case, as shown in Figure I-2.b, the bandwidth is also quite limited. For instance, if the criterion of $\pm$5º is used, such a coupler shows a bandwidth of 34%. In addition, this coupler does not present any DC isolation between any of its ports, which can be

an issue for some active circuits. Finally, even if in this work only 3-dB couplers are discussed, it is worth mentioning that the use of branch-line couplers for loose coupling levels is quite limited due to the very high impedances needed for their implementation.

I.2. Coupled-lines coupler

I.2.1. Principle of the backward-wave coupler

The other popular approach for the design of 3-dB couplers is the coupled-line topology. This topology and its use for directional couplers was first published in 1922 [17]. The topology of these devices is presented in Figure I-1.b. In Figure I-1.b, a so-called backward-wave is used for illustration purposes. Note that the footprint of these couplers is well-below that of hybrid couplers as the width of the strips and their spacing is usually much smaller than $\lambda/4$. Coupled-line couplers come in three families: (i) forward-wave, (ii) backward-wave and (iii) transdirectional. This classification is established regarding where the isolated port is located as compared to the input port. The symbolic representations of these three coupler families is shown in Figure I-3. Hence, the forward-wave coupler, backward-wave coupler, and transdirectional coupler present high isolation at port 2, port 4, port 3, respectively.

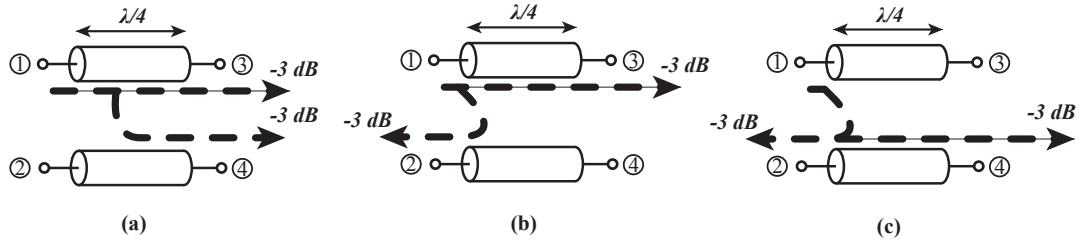

Figure I-3 Coupled-lines coupler families: (a) forward-wave, (b) backward-wave, and (c) transdirectional.

Forward-wave couplers require very different even- and odd-mode propagation velocities [14], which is not so easily achievable with quasi-TEM lines. However, if particular layouts are considered [18], this kind of couplers can be all the same implemented. On the other hand, transdirectional couplers require very different electric and magnetic coupling coefficients, and thus usually require periodical capacitive loading between the strips [19], making them less attractive for applications or technologies where the Quality-factor (Q-factor) of lumped elements is low (e.g. integrated technologies in the mm-wave band). Finally, backward-wave couplers need equal propagation velocities for their even- and odd-modes. Most of the quasi-TEM transmission lines structures used in integrated circuits (i.e., microstrip and CPWs) are close to this consideration. For this reason, backward-wave couplers are the most used coupled-lines coupler topology.

At the central frequency, an ideal 3-dB coupled-lines backward-wave coupler has the following S-parameter matrix:

$$[S] = \frac{1}{\sqrt{2}}\begin{bmatrix} 0 & 1 & -j & 0 \\ 1 & 0 & 0 & -j \\ -j & 0 & 0 & 0 \\ 0 & -j & 1 & 1 \end{bmatrix}. \quad \text{(I-2)}$$

However, as for the hybrid-coupler, when considering wideband applications, it is interesting to evaluate the frequency response of these couplers. Figure I-4 presents the S-Parameter frequency response of an ideal 3-dB backward-wave coupler with a f_0 of 100 GHz. In Figure I-4.a, the magnitude of the S-Parameters is shown, while in Figure I-4 the phase shift between the coupled and through ports $\angle S_{21} - \angle S_{31}$ is shown. Note that, as compared to the branch-line coupler, the -1-dB bandwidth is much larger, equal to almost 80%. In addition, when moving away from the central frequency, both coupled and through ports show similar slopes in the opposite directions. This facilitates the magnitude

imbalance correction in circuits sensitive to this issue. Furthermore, an ideal backward-wave coupler presents perfect matching and infinite isolation at any frequency. Finally, the phase shift seen from the input between the coupled and through port of an ideal backward-wave coupler is constant and equal to 90º throughout the whole frequency spectrum. This makes this type of couplers ideal for wideband balanced mixers, I/Q modulators…

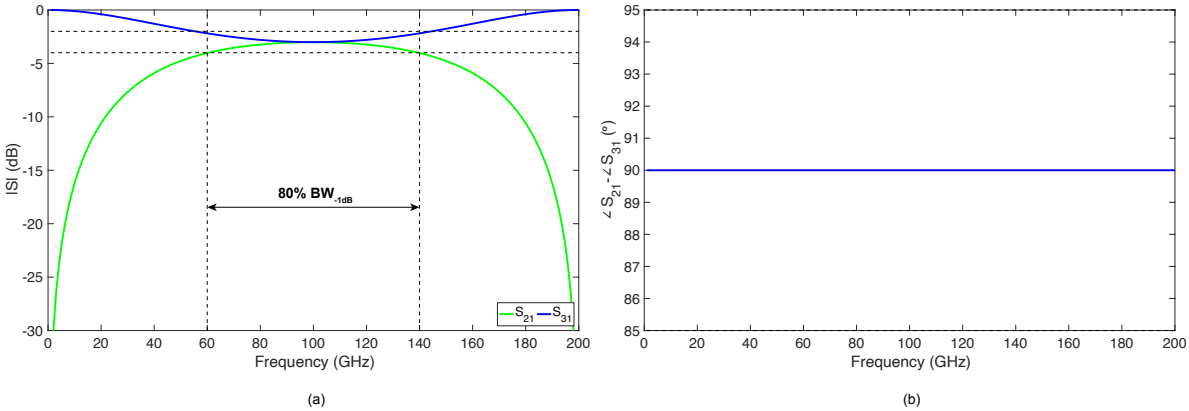

Figure I-4 S-Parameters of a 100-GHz ideal backward-wave coupled lines coupler. (a) Magnitude (b) Phase difference at the outputs.

In order to further understand the frequency responses shown in Figure I-4, let us carry out a modal analysis of a backward-wave coupler evenly loaded at its outputs by a Z_0 impedance. A modal analysis of a coupler is performed by dividing the coupler along the axis of symmetry in its length. Through this operation, a 2-port system is obtained. Finally, a magnetic wall (equivalent to an open-circuit) is placed for the even-mode analysis and an electric wall (equivalent to a short-circuit) is placed for the odd-mode analysis. These considerations are shown in Figure I-5 for lossless transmission lines showing characteristic impedances and propagation constants Z_{ce}, Z_{co}, β_e and β_o for the even- and odd-modes, respectively.

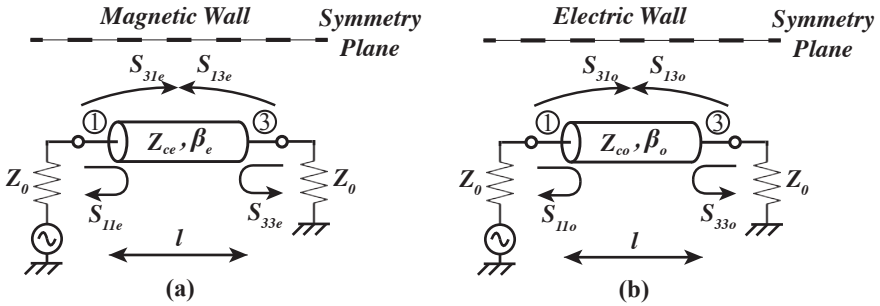

Figure I-5 Modal analysis schematics of ideal coupled-lines: (a) even-mode and (b) odd-mode.

These lossless subsystems can be represented by means of the ABCD matrixes for the even- and odd-modes, respectively:

$$ABCD_e = \begin{bmatrix} \cos(\beta_e \cdot l) & jZ_{ce}\sin(\beta_e \cdot l) \\ \dfrac{j\sin(\beta_e \cdot l)}{Z_{ce}} & \cos(\beta_e \cdot l) \end{bmatrix}$$
$$ABCD_o = \begin{bmatrix} \cos(\beta_o \cdot l) & jZ_{co}\sin(\beta_o \cdot l) \\ \dfrac{j\sin(\beta_o \cdot l)}{Z_{co}} & \cos(\beta_o \cdot l) \end{bmatrix} \quad \text{(I-3)}$$

In such a system, the reflection coefficients at the input, Γ_i, at the output, Γ_o, and the transmission coefficient, T, can be calculated using the ABCD matrix as follows:

$$\Gamma_i = \frac{A + B/Z_0 - CZ_0 - D}{A + B/Z_0 + CZ_0 - D}$$
$$\Gamma_o = \frac{-A + B/Z_0 - CZ_0 + D}{A + B/Z_0 + CZ_0 - D} \quad \text{(I-4)}$$
$$T = \frac{2}{A + B/Z_0 + CZ_0 - D}$$

As introduced earlier, in order to obtain an ideal backward-wave coupler, equal phase velocity for the even- and odd-modes is required, this leads to equal propagation constants, β, for both modes:

$$\beta = \beta_e = \beta_o. \quad \text{(I-5)}$$

In addition to the previous considerations, it can be demonstrated that an ideal backward-wave coupler also requires these conditions [14]:

$$S_{11e} = -S_{11o}$$
$$S_{33e} = -S_{33o} \quad \text{(I-6)}$$
$$S_{13e} = S_{13o}$$

where S_{ije} and S_{ijo} represent the S_{ij} parameter for the even- and odd-modes, respectively.

Under the conditions of (I-5), (I-6), considering an ideal symmetrical coupler and (I-4), its reflection S-Parameters can be written as:

$$S_{11e} = S_{33e} = \frac{j\left(\frac{Z_{ce}}{Z_0} - \frac{Z_0}{Z_{ce}}\right)\sin(\beta l)}{2\cos(\beta l) + j\left(\frac{Z_{ce}}{Z_0} + \frac{Z_0}{Z_{ce}}\right)\sin(\beta l)} \quad \text{(I-7)}$$

and

$$S_{11o} = S_{33o} = \frac{j\left(\frac{Z_{co}}{Z_0} - \frac{Z_0}{Z_{co}}\right)\sin(\beta l)}{2\cos(\beta l) + j\left(\frac{Z_{co}}{Z_0} + \frac{Z_0}{Z_{co}}\right)\sin(\beta l)}. \quad \text{(I-8)}$$

Close analysis to (I-7) and (I-8) leads to the conclusion that for a coupler, where:

$$Z_{ce}Z_{co} = Z_0^2, \quad \text{(I-9)}$$

the conditions $S_{11e} = -S_{11o}$ and $S_{33e} = -S_{33o}$ hold for any electrical length $\theta = \beta l$. Hence, for a coupler where the condition $Z_{ce}Z_{co} = Z_0^2$ holds throughout frequency (i.e., no dispersion), infinite matching to a load Z_0 can be expected at all frequencies.

Next, using (I-4) the transmission parameters can be calculated as follows:

$$S_{13e} = S_{31e} = \frac{2}{2\cos(\beta l) + j\left(\frac{Z_{ce}}{Z_0} + \frac{Z_0}{Z_{ce}}\right)\sin(\beta l)} \quad \text{(I-10)}$$

and

$$S_{12o} = S_{21o} = \frac{2}{2\cos(\beta l) + j\left(\frac{Z_{co}}{Z_0} + \frac{Z_0}{Z_{co}}\right)\sin(\beta l)}. \tag{I-11}$$

Note that when (I-9) holds, the condition $S_{12e} = S_{12o}$ does too. Hence, the conditions for the realization of a backward-wave coupler are achieved. At this point, the modal analysis is completed and the mixed-mode scattering parameters (S_{ij}) can be now calculated using:

$$\begin{aligned} S_{11} &= \frac{S_{11e} + S_{11o}}{2} \\ S_{31} &= \frac{S_{31e} + S_{31o}}{2} \\ S_{21} &= \frac{S_{11e} - S_{11o}}{2} \\ S_{41} &= \frac{S_{31e} - S_{31o}}{2} \end{aligned} \tag{I-12}$$

Note that when (I-9) holds, $S_{41} = 0$. Hence, for non-dispersive even- and odd-mode characteristic impedances, infinite isolation can be expected for all frequencies. Note that the same condition is required for both, a null return loss and infinite isolation. Thus, these couplers show similar power levels at their isolated port and return loss.

In its turn, S_{21} and S_{31} can be written as:

$$S_{31} = \frac{2}{2\cos(\beta l) + j\left(\frac{Z_{ce}}{Z_0} + \frac{Z_{co}}{Z_0}\right)\sin(\beta l)} \tag{I-13}$$

and

$$S_{21} = \frac{j\left(\frac{Z_{ce}}{Z_0} + \frac{Z_{co}}{Z_0}\right)\sin(\beta l)}{2\cos(\beta l) + j\left(\frac{Z_{ce}}{Z_0} + \frac{Z_{co}}{Z_0}\right)\sin(\beta l)}. \tag{I-14}$$

If the condition in (I-9) is satisfied and $\theta = \beta l$ is considered, equations (I-13) and (I-14) can be further simplified to:

$$S_{31} = \frac{\sqrt{1-k^2}}{\sqrt{1-k^2}\cos(\theta) + j\sin(\theta)} \tag{I-15}$$

and

$$S_{21} = \frac{jk\sin(\theta)}{\sqrt{1-k^2}\cos(\theta) + j\sin(\theta)}, \tag{I-16}$$

where

$$k = \frac{Z_{ce} - Z_{co}}{Z_{ce} + Z_{co}} \tag{I-17}$$

represents the so-called coupling coefficient.

Close investigation to (I-17) shows that a maximum amount of power is transmitted to port 2 when $\theta = (2k+1)\frac{\pi}{2}$. Hence, a directional backward-coupler shows its maximum coupling for lines with a physical length, l, of $\lambda_g/4$ (disregarding higher-order occurrences of the same phenomena).

Considering $\theta = \frac{\pi}{2}$ (i.e., central frequency of the coupler), the scattering parameter matrix can now be rewritten as:

$$[S] = \begin{bmatrix} 0 & k & -j\sqrt{1-k^2} & 0 \\ k & 0 & 0 & -j\sqrt{1-k^2} \\ -j\sqrt{1-k^2} & 0 & 0 & k \\ 0 & -j\sqrt{1-k^2} & k & 0 \end{bmatrix}, \quad \text{(I-18)}$$

which, for the case of a 3-dB coupler (i.e., $k = \sqrt{1/2}$), can be simplified to (I-2).

To summarize, ideal coupled-line couplers show superior performance than ideal hybrid couplers in wideband applications thanks to its nature. Three main factors lead to this reasoning: (i) they present a null return loss and infinite matching throughout the whole frequency spectrum, (ii) their layout versatility is superior as the isolated port (and hence the coupled ports) can be changed by using forward-wave, backward-wave or transdirectional couplers and (iii) their size is reduced.

I.2.2. State-of-the-art of mm-wave coupled-lines directional couplers

The interest of coupled-lines couplers and their theory were discussed in the previous section. However, any practical implementation of an integrated 3-dB coupler was presented. Since most of the classical transmission lines used in any integrated process present quasi-TEM propagation (i.e., microstrip and CoPlanar Waveguides, CPW), the design of backward-wave couplers is often privileged due to their close propagation velocities for their even- and odd-modes.

Integrated processes have a multilayered Back-End-of-Line (BEOL), where the lower metallic levels are usually thin metals used for digital routing and the upper levels are thicker metals used for power routing and passive devices design, as their added thickness leads to lower metallic losses. However, the different metallic layers are surrounded by dielectric materials (e.g. silicon-dioxide, SiO_2) and usually covered with the so-called *passivation layer*, which protects the BEOL from the exterior environment. All these layers, and especially the passivation layer located above the thick metals, have different relative dielectric constants (ε_r), leading to a divergence in the propagation velocity of the even- and odd-modes, $v_{\varphi e}$ and $v_{\varphi o}$, respectively. Even though this difference is usually insufficient to lead to the design of forward-wave couplers, it is enough to greatly impact the matching and isolation of the backward-wave coupler, as the condition in (I-5) is not hold.

Moreover, most of the integrated technologies have stringent design rules that forbid the placement of metal strips in very close proximity (i.e., generally below 1-2 µm). This leads to insufficient electromagnetic coupling between strips, for classical coupled transmission lines. For this reason, 3-dB coupling is often achieved through the use of the so-called broadside structure. A broadside coupler, as depicted in Figure I-6, is usually designed using the two upper metals of the BEOL, which are the thickest ones. The vertical spacing between these two metal layers, h, is usually inferior to the lateral limitations of the design rules. Hence, higher electromagnetic coupling can be achieved. However, this further increases the difference between $v_{\varphi e}$ and $v_{\varphi o}$. In addition, such a structure is highly non-symmetrical as the characteristic impedances presented by each strip are different. Hence, when these couplers are evenly loaded at their outputs, achieving low return loss is a cumbersome issue.

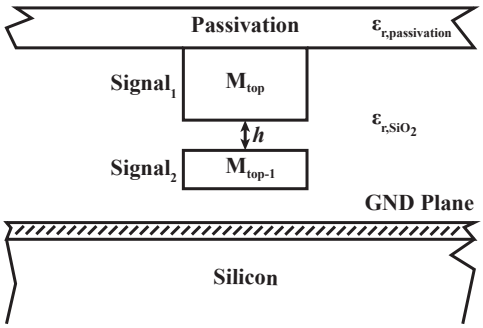

Figure I-6 Cross-section of a broadside microstrip coupler.

Table I-I presents some of the most recent state-of-the-art couplers at mm-waves.

TABLE I-I STATE-OF-THE-ART INTEGRATED MM-WAVE 3-DB COUPLERS.

Ref.	[20]	[21]	[22]	[23]	[24]	[25]***
Tech.	35-nm GaAs	130-nm BiCMOS	180-nm CMOS	0.35-µm BiCMOS	65-nm CMOS	55-nm BiCMOS
Topology	Broadside	SL-Broadside	Meandered CCS CL	Meandered Broadside	*Braided* CS-CPW	CS-CPW
Frequency (GHz)	270	60	40	75	90	60
Through (dB)	3.9	3.9	4.5	4	3.5	3.3
Coupling (dB)	4.1	3.8	4.5	4	4.4	3.5
Return Loss (dB)	>13	>25	>13	>15	>18	29
Isolation (dB)	>17	>25	>18	17***	-	28
1-dB BW (GHz)	51†	34	20	30	55	-
±3º BW (GHz)	51‡	47**	10	30	>60	-
Size* (λ^2)	0.013	0.003	0.005	-	0.001	0.003

*Free-space wavelength †-0.5 dB BW ‡±1.4º BW **±1º BW ***Simulation only

The works reported in [20]–[23] use broadside couplers. In [20], authors use the coupled Grounded CPWs (GCPWs) architecture in a MMIC featuring a BenzoCylcoButene (BCB) layer in its BEOL. Such a layer allows the design of high-Q passive devices, leading to reduced losses. However, as introduced earlier, limited isolation and return loss are achieved due to different phase velocities for the even- and odd-modes.

The work reported in [21] presents a Semi-Lumped (SL) broadside microstrip coupler, the coupled strips being loaded with inductors and capacitors. Even-though this approach helps to maintain the stability of the coupler and reduce its physical dimensions, a rapid degradation of its performance can be observed above around 70 GHz. Above this frequency, the coupler has a behavior greatly differing from the one observed in an ideal coupler (i.e., steady decrease of the coupling while the isolation and return loss are maintained).

Authors in [22] report a meandered Complementary-Conducting-Strip Coupled Line (CCS CL). The CCS CL is a structure similar to a traditional coupled microstrip line, whose ground plane has been altered by performing openings in it. Although this approach is sufficient to ensure an even coupling between both strips, limited isolation and return loss are reported. Moreover, the openings allow the electromagnetic field to penetrate the silicon, resulting in the greatest losses of the considered couplers. Finally, the coupler still results in a relatively large footprint.

The work in [23] presents a classical broadside microstrip coupler. This work allows evaluating the performance of such a structure in an integrated environment at a moderate mm-wave frequency. Even though the footprint of this structure is not reported, limited isolation and return loss are observed.

In [24], the Coupled Slow-wave CoPlanar Waveguide (CS-CPW) is used for the design of the 3-dB coupler. However, the coupled signal strips were *braided* to achieve greater coupling, leading to a relatively high return loss due to the complexity of the structure. In addition, the isolation of the coupler is not reported but is expected to show a similar response to the return loss, as seen in the other couplers. However, note that the miniaturization achieved in this coupler thanks to the slow-wave effect is remarkably high as well as the relative bandwidths (i.e., -1 dB and $\pm$3º).

Finally, the work in [25], where the CS-CPW architecture was reported for the first time, presents a balanced coupler (i.e., low magnitude imbalance) with great isolation and low return loss. Even though the relative bandwidths were not reported in that article and only simulations were presented, the great isolation and low return loss indicate similar propagation velocities for the even- and odd-modes. Hence, large relative bandwidths can be expected. For this reason, in this thesis, the CS-CPW architecture as presented in [25], is the chosen architecture for the implementation of coupled-line couplers.

I.2.3. CS-CPW architecture

CS-CPWs are based on the slow-wave concept, first presented in [26] for CPW architectures. The slow-wave transmission lines integrate periodic metallic structures aiming to rise the linear capacitance of the transmission line, C_l, without practically modifying its linear inductance, L_l, as compared to the classical structure. Hence, with the rise of C_l, the propagation velocity (v_φ) is decreased:

$$v_\varphi = \frac{1}{\sqrt{L_l C_l}}. \tag{I-19}$$

Thus, when aiming to design a transmission line with a given electrical length θ at a given angular frequency ω, the required physical length of the structure, l, is reduced thanks to the increase of the propagation constant β:

$$\theta = \beta l = \frac{\omega}{v_\varphi} l. \tag{I-20}$$

In addition, provided that the addition of the floating shield does not increase the attenuation constant α, the Quality-factor (Q-factor) of the transmission line defined in [27] is also increased:

$$Q = \frac{1}{2}\frac{\beta}{\alpha}. \tag{I-21}$$

For CPWs, the integration of a floating shield composed of the so-called fingers (or ribbons) placed perpendicularly to the propagation direction, leads to a Slow-wave CPW (S-CPW). Figure I-7 presents the S-CPW architecture and the geometrical parameters that define it.

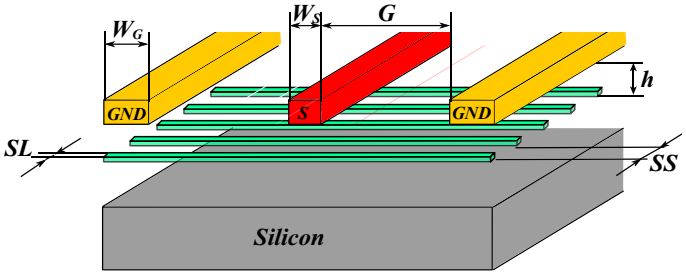

Figure I-7 S-CPW architecture.

Figure I-8a presents the electric field around the conductors of a cross-sectioned S-CPW. Note that the electric field is captured between the signal/ground strips and the floating shield below. In addition to the length reduction achieved through the slow-wave effect, the use of the floating shield also prevents the electric field from going to the lossy silicon substrate, which can lead to an

improvement of α when compared to a classical CPW, as shown in [28]. Finally, the magnetic field behaves as in a classical CPW, as shown in Figure I-8b.

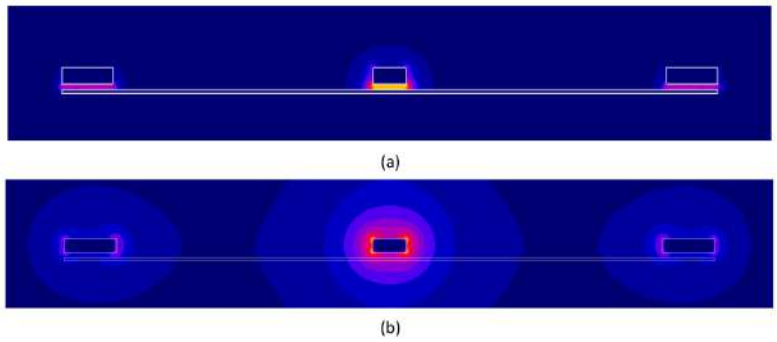

Figure I-8 Field distribution around an S-CPW from [28]. *(a) Electric field. (b) Magnetic field.*

The first proposal of an electrical model for integrated S-CPWs was given in [29]. In that article, authors proposed to substitute the classical RLCG model [30] by an RLRC model, as in integrated circuits the quality of the SiO_2 layers tends to present very low losses (i.e., $\tan(\delta_{SiO_2}) \approx 0$). However, the resistance of the fingers has to be accounted for proper modelling. This proposal was subsequently followed by a parametrical model presented in [31], where the authors gave a detailed methodology for the capacitance calculation in a S-CPW. Thanks to the quasi-TEM propagation hold in an S-CPW, the analysis of capacitance and inductance calculations can be carried out separately.

As mentioned earlier in this manuscript, CS-CPWs were first proposed in [25]. In that article, authors presented the structure together with three shielding topologies, which will be discussed later in this manuscript.

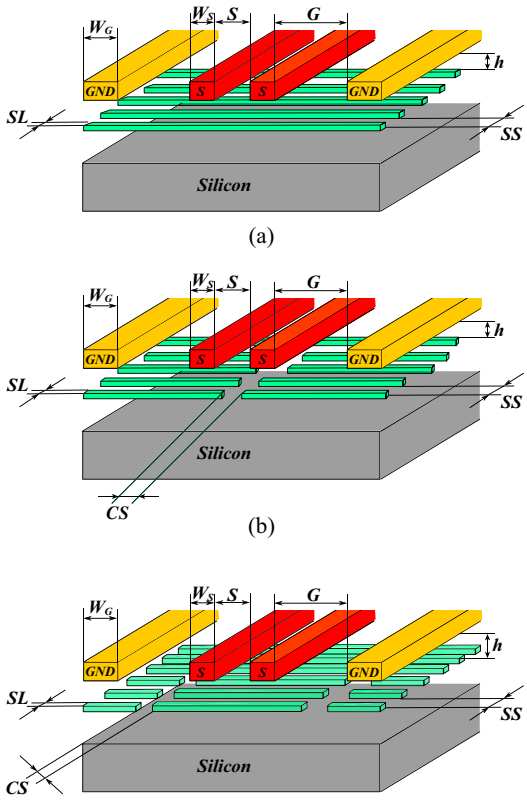

Figure I-9 CS-CPW architecture with: (a) Uncut shielding, (b) Center-Cut (CC) shielding, and (c) Side-Cut (SC) shielding.

In the case of CS-CPWs, as compared to an S-CPW, the shielding presents another advantage beyond the miniaturization brought by the slow-wave effect. As discussed earlier, couplers in integrated BEOLs suffer from poor coupling between coplanar strips due to the design rules. For this reason, many couplers in integrated technologies are designed using a broadside architecture. However, the use of a floating shielding underneath helps raising the coupling between the two signal strips, as shown in Figure I-9. In addition, the confinement of the electric field between the signal/ground strips and the floating shield helps for the equalization of the even- and odd- modes, leading to greater directivity and bandwidth, as compared with broadside microstrip couplers. These features, together with the fact that the structure and its three shielding topologies (i.e., uncut shielding, Center-Cut shielding and Side-Cut shielding), shown in Figure I-9, allow a great degree of flexibility to synthesize high-coupling couplers (i.e., 3-dB couplers) or low-coupling couplers, make this structure of great interest.

Nevertheless, even if the interest of this structure for the design of integrated coupled-lines couplers is clear, the simulation of such a structure in a 3D EM simulator (e.g. ANSYS HFSS) is a cumbersome issue. Simulation of CS-CPWs takes a considerable amount of computer Random Access Memory (RAM) and computational power, leading to simulations that take in the order of 6-8 hours[1]. For instance, authors in [32] were forced to split the simulation of a CS-CPW between its even- and odd-modes due to RAM issues in a 32 GB system. In this scenario, the use of this structure for industrial purposes is of reduced interest due to the long simulation and optimization times. For this reason, the definition of a fully parametric model, able to simulate the structure with reduced time is a subject of major interest in the field of coupled-line coupler design. This issue will be dealt with in the following sections, with the development of a model based on the RLRC model described in [29] for S-CPWs.

I.2.3.1. Lossless model of a CS-CPW

As introduced earlier, an extra degree of freedom was introduced in [25] with three shielding topologies, namely (i) uncut, (ii) center-cut (CC) and (iii) side-cut (SC). In CC topology, a *cut* is performed on the center of the fingers composing the floating shield. On the other hand, in a SC shielding, a *cut* is performed at the sides of the fingers (see Figure I-9). Finally, in an uncut shielding, the floating fingers are not cut. These topologies allow the designer to tune the electric coupling coefficient of the structure, k_C, without modifying its magnetic coupling coefficient, k_L [ref 16?].

In a first approximation, let us consider ideal CS-CPWs (i.e., lossless) and a negligible coupling between signal and ground strips. The latter consideration is realistic as in most of the coupler implementations, the distance between the strips and the floating shield h is smaller than the gap between the signal and ground strips, G. Finally, let us also consider that G is below 100 µm, where propagation in the fingers starts showing dispersion in the effective dielectric constant of S-CPWs [33]. With these considerations, the distributed model elementary cells (i.e., considering an elementary length δl) of the structure for each of the shield topologies can be defined as in Figure I-10.

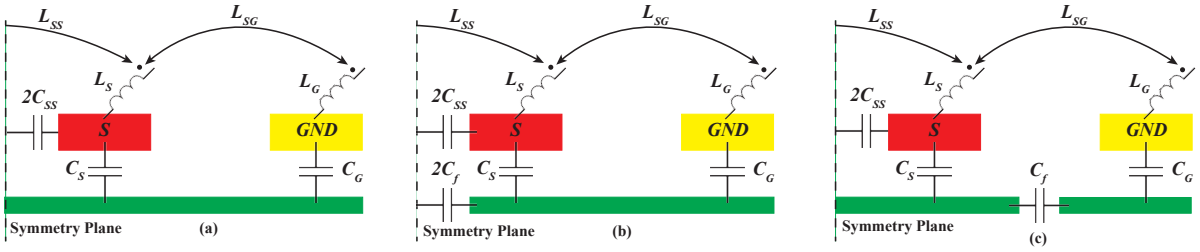

Figure I-10 Distributed model elementary cell of a lossless CS-CPW with central structure symmetry with (a) uncut shield, (b) CC-shielding, and (c) SC-shielding.

Using these models, a modal analysis can be carried out to determine k_L and k_C along with the even- and odd-mode characteristic impedances, Z_{even} and Z_{odd}, respectively. For the even-modal analysis a magnetic wall (equivalent to an open circuit) is placed on the symmetry plane of Figure I-10,

[1] Intel Xeon E5-1660 v4 @ 3.2 GHz with 120 GB of RAM.

while for the analysis of the odd-mode an electrical wall (equivalent to a short circuit) is placed in this plane.

The coupling coefficients were first described in [34] as a method to evaluate the even- and odd-mode propagating velocities. In that paper, k_L was described as follows:

$$k_L = \frac{L_{even} - L_{odd}}{L_{even} + L_{odd}}, \tag{I-22}$$

where L_{even} and L_{odd} represent the overall inductance of the even- and odd-modes, respectively.

Similarly, the electric coupling coefficient k_C was defined using the overall capacitance of the even- and odd-modes, C_{even} and C_{odd}, respectively:

$$k_C = \frac{C_{even} - C_{odd}}{C_{even} + C_{odd}}. \tag{I-23}$$

Provided that the even- and odd-mode propagation velocities, $v_{\varphi e}$ and $v_{\varphi o}$, can be expressed as:

$$v_{\varphi e} = \frac{1}{\sqrt{L_{even} C_{even}}} \tag{I-24}$$

and:

$$v_{\varphi o} = \frac{1}{\sqrt{L_{odd} C_{odd}}}, \tag{I-25}$$

it can be shown that in order to hold the condition (I-5) the two coupling coefficients must be equal:

$$k_L = k_C. \tag{I-26}$$

Finally, the even- and odd-mode characteristic impedances in a lossless CS-CPW can be calculated as follows:

$$Z_{even/odd} = \sqrt{\frac{L_{even/odd}}{C_{even/odd}}}. \tag{I-27}$$

Next, let us analyze the coupling coefficients in a CS-CPW architecture.

a) Magnetic coupling

Using the definition of the magnetic coupling coefficient in (I-22) together with the models proposed in Figure I-10, the even- and odd-mode inductances can be computed as follows:

$$\begin{matrix} L_{even} = L_S + L_G - 2L_{SG} + L_{SS} \\ L_{odd} = L_S + L_G - 2L_{SG} - L_{SS} \end{matrix}, \tag{I-28}$$

which leads to a k_L under the form below:

$$k_L = \frac{L_{SS}}{L_S + L_G - 2L_{SG}}. \tag{I-29}$$

Using the models proposed in Figure I-10, it is straightforward to see that the shielding topology has a negligible impact on k_L as the magnetic behavior of the CS-CPW is unperturbed by the presence

of a floating shield (see Figure I-8). This is an interesting feature of CS-CPWs as the shape and topology of the floating shield allows to tune independently k_C from k_L as we will demonstrate subsequently.

b) Electric coupling for CS-CPWs with uncut shield

For the computation of the electric coupling coefficient the same boundary conditions proposed above for the modal analysis are used. Hence:

$$C_{even} = \frac{C_S C_G}{C_S + C_G} \tag{I-30}$$

and

$$C_{odd} = 2C_{SS} + C_S. \tag{I-31}$$

Note that only C_{even} is a function of C_G and that only C_{odd} is a function of C_{SS}. Therefore, variation on the geometrical parameters affecting only one of these capacitances (e.g. W_G and S, respectively), allows the independent tuning of C_{even} and C_{odd}, and thus tuning of k_c.

c) Electric coupling for CS-CPWs with CC-shield

In the case of a CC-shield, the model in Figure I-10b should be considered. In this architecture, the *cut* realized in the center of the structure creates a capacitance, C_f, between the split parts of the fingers at each side of the symmetry plane. Without loss of generality, similar boundary conditions can be used for the evaluation of the even- and odd-mode capacitances. These considerations lead to an even-mode capacitance as in (I-30) for the uncut case. On the other hand, the odd-mode capacitance is now expressed as:

$$C_{odd} = 2C_{SS} + \frac{C_s(2C_f + C_G)}{C_S + 2C_f + C_G}. \tag{I-32}$$

It is straightforward to show that in (I-32), as compared to the expression in (I-31), the term C_S has been replaced by the equivalent capacitance formed by C_S in series with $2C_f + C_G$. Thus, the value of C_{odd} in a CS-CPW with CC-shielding is lowered, as compared to the uncut case. This yields to a modified k_C and a greater odd-mode characteristic impedance. However, as C_{even} and k_L are unmodified, the even-mode characteristic impedance remains the same as the uncut CS-CPW.

d) Electric coupling for CS-CPWs with SC-shield

In a CS-CPW with a SC-shield, *cuts* are performed in the fingers at the middle of the signal to ground gap, G. Hence, the model in Figure I-10c has to be considered. In this scenario, the even-mode capacitance is expressed as:

$$C_{even} = \frac{C_S C_f C_G}{(C_S C_G) + (C_S C_f) + (C_f C_G)}, \tag{I-33}$$

while C_{odd} is calculated as in (I-31).

In the case of the SC-shielding, the even-mode capacitance is reduced as compared to the uncut case. For the latter, C_{even} is calculated as the series configuration of C_S and C_G, as shown in (I-30), whereas for SC-shielding, C_{even} is the equivalent capacitance of the series configuration of C_S, C_f and C_G. Hence, (I-33) inevitably leads to a lower value than (I-30). As a result, the CS-shielded CS-CPWs presents a lower even-mode capacitance, a modified k_C and a greater Z_{even}. The odd-mode characteristic is the same as the uncut case.

To summarize, the previous analysis shows that, for a given lateral dimension of the CS-CPW (i.e., given W_S, S, G, and W_G), the different shielding topologies allow to tune k_C, Z_{even} and Z_{odd} independently from k_L. The expressions for the magnetic coupling coefficient, C_{even} and C_{odd}, for the three considered shielding topologies are summarized in Table I-II.

TABLE I-II SUMMARY OF THE AND EXPRESSIONS.

Shield	Uncut	CC	SC
k_L	$\frac{L_{SS}}{L_S + L_G - 2L_{SG}}$		
C_{even}	$\frac{C_S C_G}{C_S + C_G}$	$\frac{C_S C_G}{C_S + C_G}$	$\frac{C_S C_f C_G}{(C_S C_G) + (C_S C_f) + (C_f C_G)}$
C_{odd}	$2C_{SS} + C_S$	$2C_{SS} + \frac{Cs(2C_f + C_G)}{C_S + 2C_f + C_G}$	$2C_{SS} + C_S$

Note that for all the shielding topologies, C_{odd} is always greater than C_{even}.

Based on the expressions given in Table I-II, a comparison on k_L, k_C, C_{even}, C_{odd}, Z_{even} and Z_{odd} can be carried out, as compared to the uncut case. This comparison is presented in Table I-III, where the symbol → stands for an unchanged parameter, ↗ stands for an increase of the parameter and ↘ represents a decrease in the parameter, as compared to the uncut case.

TABLE I-III SUMMARY OF THE k_L, C_{even}, C_{odd}, k_C, Z_{even} AND Z_{odd} BEHAVIOR FOR THE CC- AND SC-SHIELD TOPOLOGIES

Shield	k_L	C_{even}	C_{odd}	$\lvert k_C \rvert$	Z_{even}	Z_{odd}
CC	→	→	↘	↘	→	↗
CS	→	↘	→	↗	↗	→

Even though the expressions carried out in this section and summarized in Table I-II and Table I-III help to understand the behavior of the structure, a lossy model is needed for proper design of CS-CPWs. This is the purpose of the next section.

I.2.3.2. Lossy model of a CS-CPW

The lossless model presented in Figure I-10 can be extended to a model accounting for losses when resistive effects are added. For the sake of simplicity, radiation and dielectric losses are not considered. This assumption is valid for structures with a physical length below λ_G and integrated in a high-Q dielectric, as for CS-CPWs in an integrated technology. Hence, the model proposed hereby is an extension of the model in Figure I-10, where the metallic losses in all the conductors of a CS-CPW is accounted for. The model of a lossy CS-CPW is presented in Figure I-11.

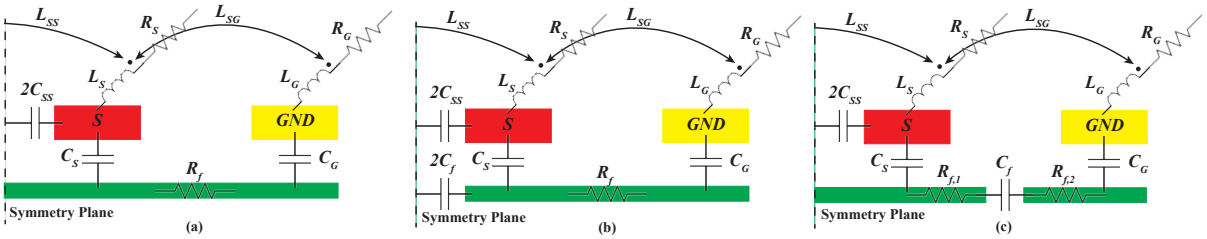

Figure I-11 Distributed model elementary cell of a lossy CS-CPW with (a) uncut shield, (b) CC-shielding, and (c) SC-shielding.

Note that even at the upper-end of mm-wave frequencies, the capacitances in the model can be computed using a quasi-static approach, since their dimensions are always very small as compared to

the guided wavelength. However, resistances and inductances suffer from frequency-dependent phenomena (e.g. skin-effect). For this reason, a model accounting for the frequency dependence of these elements has to be developed.

Next, a detailed methodology for the computation of the values of each model element is detailed. As the CS-CPW is supposed to hold a quasi-TEM propagation, inductances and resistances can be calculated separately from capacitances.

I.2.3.3. Capacitance computation

Accurate parametrical modeling of transmission lines is a subject that has vastly been discussed in the literature for many transmission line architectures. This issue can be addressed using: (i) an empirical approach or (ii) an analytical approach. The first approach is merely an exercise of data fitting. Even though this methodology can yield good results when similar structures are considered, it is difficult to assess when the fitting will fail to predict the actual physics. Hence, a restricted validity domain has to be established for a low-error outcome, which is often limited to single or similar technologies. On the other hand, analytical models have the advantage of having well-defined premises that allow to formally define validity boundaries for the model.

In that context, authors in [31] proposed a fully-parametrical model for S-CPWs. The main novelty of the work is the linear capacitance calculation. For this purpose, the authors defined four capacitive regions around the signal strip (i.e., *plate*, *angle*, *fringe* and *up*). These regions are shown in Figure I-12.

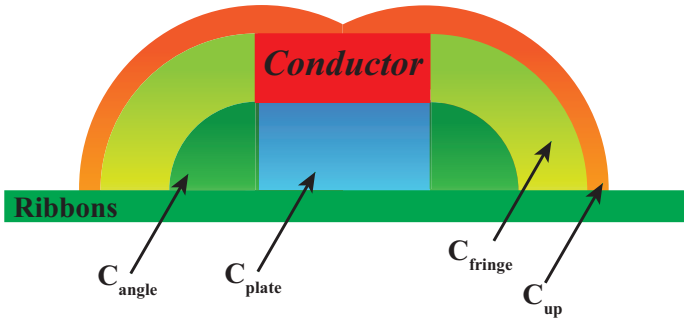

Figure I-12 Capacitive regions around a S-CPW strip, as defined in [31].

Next, field-line *paths* were defined in each of the regions. For instance, in the *plate* region, the field-lines follow straight-line *paths*, in the *fringe* regions field lines follow circular *paths*... Using these definitions, the capacitance for each of the infinitesimal field-lines constituting these regions can be calculated thanks to the expression of the parallel-plate capacitance C_{pp}:

$$C_{pp} = \varepsilon_0 \varepsilon_r \frac{l \cdot W}{d}, \tag{I-34}$$

where ε_0 is the dielectric constant in vacuum, ε_r is the relative dielectric constant of the medium where the electric field is confined, and l and W are the length and the width of the structure, respectively. Finally, d represents the distance between the two extremes of the electric field *path*.

If d in equation (I-34) is substituted with the *length* of the electric field *path* in each of the regions, $d_{region}(\delta W)$, the capacitance in each region, C_{region}, can be obtained as:

$$C_{region} = \varepsilon_0 \varepsilon_r l \int_0^{W_r} \frac{\delta W}{d_{region}(\delta W)}, \tag{I-35}$$

where W_r is the width of the region (e.g. the thickness of the *Strip* for the fringe region).

Using (I-35) and the expressions of $d_{region}(\delta W)$ given in [31], the magnitude of the capacitances for an S-CPW or a CS-CPW can be determined. However, for a CS-CPW electric coupling between the central strips is of major importance for the accurate modelling of these structures. In [31],

the case of signal and ground strips placed in a close configuration was discussed. In that article, authors showed that the equations proposed for the calculation of the capacitance between signal/ground strips to the floating shield could be easily adapted to account for the electric coupling between coplanar strips. However, the case of strips placed in a very close configuration (i.e., $d/2 < h$, where d is the distance between the coplanar strips and h is the distance between the strips and the fingers) was not thoroughly addressed.

In a CS-CPW, when aiming for a tight coupling, the signal strips can be placed in such a way that $S/2 < h$. In that scenario considering the electric field *paths* as in [31], it is straightforward to notice that some part of the electric field is shared between the lower plate of the signal strips, creating C_{down}, as depicted in Figure I-13. In this scenario, C'_{plate} can no longer be calculated as in (I-34); it has to be calculated as:

$$\begin{aligned} C'_{plate} &= \varepsilon_0 \varepsilon_r \frac{l(W_S - W'_S)}{h} && \forall\, W_S \geq W'_S \\ C'_{plate} &= 0 && \forall\, W_S < W'_S \end{aligned}, \tag{I-36}$$

where $W'_S = h - S/2$.

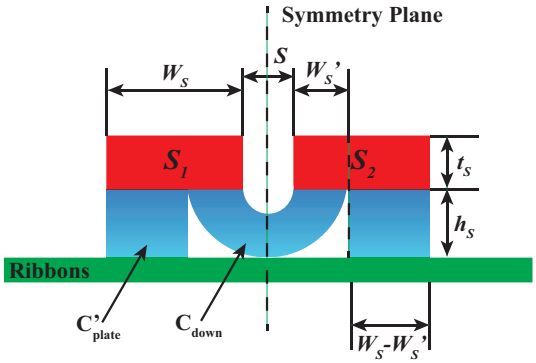

Figure I-13 New electric field distribution, as compared to [31]*, for very close signal strips. Even though other capacitance regions exist, only the modified regions (as compared to*[31]*) are shown for clarity purposes.*

The equation in (I-36) leads to more accurate computation of C_{SS} and C_S, which were underestimated and overestimated, respectively, using the methodology described in [31]. In addition, the work in [31] lacked the explicit description of the capacitance existing between the two parts of a *cut* finger. However, the methodology given in that article can be easily adapted for the calculation of C_f in the case of a CC- or SC-shield in a CS-CPW.

I.2.3.4. Resistance and inductance computation

As introduced earlier in this document, frequency-dependent phenomena have to be accounted for accurate modeling of passive devices in integrated technologies. In an integrated transmission line, the frequency-dependence is mainly reported on the behavior of the magnetic field, inducing effects such as eddy currents or skin effect, with consequences in the ohmic losses and inductive behavior of passive devices.

Let us consider the Ampere's law with Maxwell's addition [35] in vacuum:

$$\oint_{\delta\Sigma} \mathbf{B} \cdot \mathrm{d}\boldsymbol{l} = \mu_0 \left(\iint_{\Sigma} \mathbf{J} \cdot \mathrm{d}\mathbf{S} + \varepsilon_0 \frac{\mathrm{d}}{\mathrm{d}t} \iint_{\Sigma} \mathbf{E} \cdot \mathrm{d}\mathbf{S} \right), \tag{I-37}$$

where in its left-side **B** is the magnetic field, $\delta\Sigma$ is the boundary curve of the surface Σ, $\boldsymbol{l}$ is the length of $\delta\Sigma$. On the right-side μ_0 is the vacuum permeability, **J** represents the current density, **S** is the surface area normal to Σ, ε_0 is the vacuum permittivity, **E** denotes the electric field and t represents the time. This equation reveals that a magnetic field is induced by a current $\mathbf{I} = \iint_{\Sigma} \mathbf{J} \cdot \mathrm{d}\mathbf{S}$ and an eventually time-varying electric field **E**. However, the Maxwell-Faraday equation in [35] for a vacuum:

$$\oint_{\delta\Sigma} \mathbf{E} \cdot \mathrm{d}\boldsymbol{l} = \frac{\mathrm{d}}{\mathrm{d}t} \iint_{\Sigma} \mathbf{B} \cdot \mathrm{d}\mathbf{S}, \tag{I-38}$$

shows that a time-varying magnetic-field also induces an electric field.

The interdependence of (I-37) and (I-38) makes the calculation of the electromagnetic field around an electrically long conductor practically impossible for any conductor shape in any integrated technology. In other words, an exact closed-form formula for the electromagnetic field around an integrated transmission line is practically impossible to obtain.

For this reason, Finite Element Methods (FEM) are used to compute these fields around a conductor. In a FEM approach, the device is subdivided (meshed) into elementary cells. These cells are small as compared to the guided wavelength. Hence, any propagation is hold within the cell. In this scenario, the electromagnetic fields can now be computed and a frequency-dependent response of the structure can now be obtained. Many commercial software, such as ANSYS HFSS, Momentum, EM Pro…, feature FEM for electromagnetic fields calculus. However, when dealing with complex structures such as CS-CPWs, the simulation time is rapidly a limitation for fast optimization, thus requiring the development of alternative modeling approaches.

On the other hand, when the topology of a distributed electrical model of a transmission line is known, their simulation can be approached in an alternative way: quasi-static simulation. Quasi-static simulation assumes that either $\frac{\mathrm{d}}{\mathrm{d}t} \iint_{\Sigma} \mathbf{B} \cdot \mathrm{d}\mathbf{S} \approx 0$ in (I-38) or that $\frac{\mathrm{d}}{\mathrm{d}t} \iint_{\Sigma} \mathbf{E} \cdot \mathrm{d}\mathbf{S} \approx 0$ in (I-37), leading to an electro-quasi-static (EQS) or a magneto-quasi-static (MQS) approach, respectively. As the computation of the capacitances of the electrical model in Figure I-11 is performed as detailed in the previous section, an MQS approach is considered for the computation of the inductances and resistances.

In an MQS approach, the displacement current $\frac{\mathrm{d}}{\mathrm{d}t} \iint_{\Sigma} \mathbf{E} \cdot \mathrm{d}\mathbf{S}$ is considered to be negligible. However, when the frequencies or electrical lengths are much smaller than the guided wavelength, this is a realistic consideration. Under this criterion, the magnetic field is only determined by the current circulating within the structure. However, the magnetic induction between neighboring conductors leading to proximity and skin effects are still considered as (I-38) is kept unchanged.

Many approaches can be taken to implement a FEM using an MQS criterion. However, C. R. Paul gave one of the most straightforward methodologies in [36]. A similar methodology to the one proposed by Paul has already been used in some works reporting transmission line modeling in integrated technologies [37]. However, authors in [37] used an unidimensional mesh (i.e., meshing along the width of their transmission line) for the modeling of their transmission lines. Even though unidimensional meshes can lead to good results at low frequencies and for conductors whose width/thickness is much greater than its thickness/width, its performance is rapidly degraded when the frequency increases.

a) Mesh definition

In this work, a two-dimensional mesh is used for increased accuracy. In order to illustrate the used mesh, let us consider the signal and ground conductors of a CS-CPW with an elementary length $\delta l = SS + SL$, which corresponds to a period of the CS-CPW, as depicted in Figure I-14a.

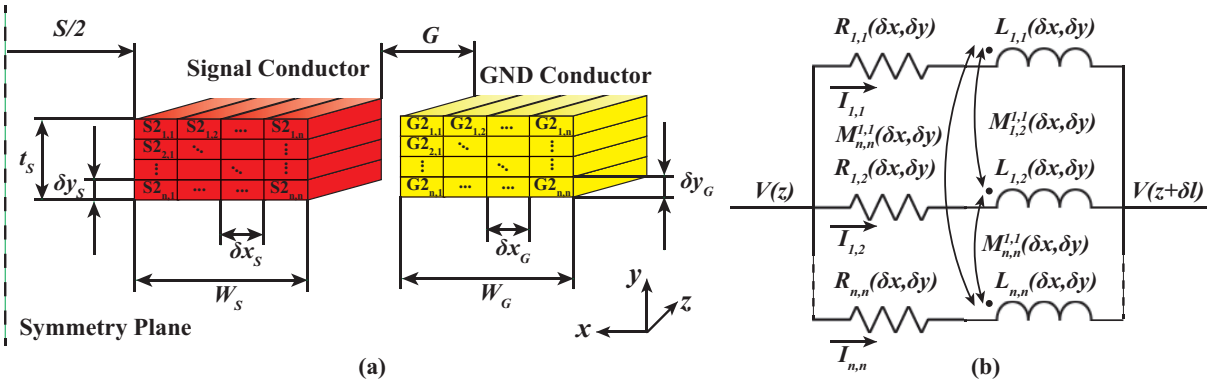

Figure I-14 (a) Example of a two-dimensional mesh for a CS-CPW structure. (b) Lumped-elements considered inside a conductor. The mutual inductances between mesh cells in different conductors are not depicted for clarity purposes.

In this work, the faces of each conductor (i.e., parts of the conductors in the *x*-*y* plane) are meshed using n^2 cells (n cells in the *x*-direction and n cells in the *y*-direction). Leading to cells shaped as quadrangular prisms. Considering a symmetrical CS-CPW, this leads to ground (signal) conductors with elements of the mesh having a height of δy_G (δy_S) and a width of δx_G (δx_S), respectively. Using this mesh, $\delta y_{G/S}$ and $\delta y_{G/S}$ can be defined as:

$$\begin{aligned} \delta x_{G/S} &= W_{G/S}/n \\ \delta y_{G/S} &= t_S/n \end{aligned} \quad . \tag{I-39}$$

Next, with the consideration that the voltage across the face of each conductor is constant as in [36] and a lossy conductor, a schematic similar to the one depicted in Figure I-14b is obtained. In [36], each element of the mesh is considered to be composed by a series association of a resistance and an inductance with a mutual inductance to every other inductance in the system.

b) Impedance matrix definition

Once the mesh has been defined, the next step is to calculate the impedance matrix $\boldsymbol{Z}$. The impedance matrix is defined as follows:

$$\boldsymbol{V} = \boldsymbol{Z}\boldsymbol{I}, \tag{I-40}$$

where $\boldsymbol{V}$ is the voltage on the face of each conductor and $\boldsymbol{I}$ is the current flowing through each conductor. In the case of a CS-CPW (i.e., a structure with four conductors) this can be expanded into:

$$\begin{bmatrix} V_{GND} \\ V_{S1} \\ V_{S2} \\ V_{GND} \end{bmatrix} = \begin{bmatrix} Z_{GND} & j\omega M_{S1}^{GND} & j\omega M_{S2}^{GND} & j\omega M_{GND}^{GND} \\ j\omega M_{GND}^{S1} & Z_{S1} & j\omega M_{S2}^{S1} & j\omega M_{GND}^{S1} \\ j\omega M_{GND}^{S2} & j\omega M_{S1}^{S2} & Z_{S2} & j\omega M_{GND}^{S2} \\ j\omega M_{GND}^{GND} & j\omega M_{S1}^{GND} & j\omega M_{S2}^{GND} & Z_{GND} \end{bmatrix} \cdot \begin{bmatrix} I_{GND} \\ I_{S1} \\ I_{S2} \\ I_{GND} \end{bmatrix}, \tag{I-41}$$

where Z_i is the impedance of the i-th conductor, M_j^i is the partial mutual inductance between the i-th and the j-th conductors, ω the angular frequency, V_i and I_i the voltage at the face and through the i-th conductor, respectively.

At this point $\boldsymbol{Z}$ and $\boldsymbol{I}$ are unknown matrixes since $j\omega M_j^i$ and $Z_i = R_i + j\omega L_i$, where R_i and L_i are the series resistance and partial self-inductance of the i-th conductor, respectively, have frequency-dependent magnitudes.

Next, using the mesh defined in the previous section, each diagonal element of the $\boldsymbol{Z}$ matrix, $\boldsymbol{Z_i}$, is redefined using a quasi-static analysis of the elements of the mesh that define it and hence, expanded into a $n^2 \cdot n^2$ square matrix. This leads to:

$$\boldsymbol{Z_i} = \begin{bmatrix} R_{1,1} + j\omega L_{1,1} & \cdots & j\omega M_{n,n}^{1,1} \\ \vdots & \ddots & \vdots \\ j\omega M_{1,1}^{n,n} & \cdots & R_{n,n} + j\omega L_{n,n} \end{bmatrix}, \tag{I-42}$$

where $R_{k,m}$ and $L_{k,m}$ are the DC-resistance and DC-partial self-inductance of the element in the k-th row and the m-th column of the mesh. $M_{o,p}^{k,m}$ is the quasi-static value of the mutual inductance between the elements in the k-th row and the m-th column and in the o-th row and the p-th column, respectively. The DC-resistance is classically calculated as:

$$R_{DC} = \frac{\delta l}{\sigma \cdot \delta x \cdot \delta y}. \tag{I-43}$$

The value of the partial self- and mutual-inductance can be calculated using equations (8) and (9) in [38]. Paul proposes to use [39] for this purpose. However, the authors of the present document found [38] to be more numerically stable.

Finally, the elements outside the diagonal of $\boldsymbol{Z}$, $j\omega\boldsymbol{M_j^i}$, are in their turn $n^2 \cdot n^2$ square matrixes containing the partial mutual inductances between the elements of the mesh in the i-th and j-th conductors.

At this point, all the scalars in $\boldsymbol{Z}$ can be substituted by their matrixes, obtained through the previous analysis, leading to the meshed impedance matrix $\boldsymbol{Z^m}$, a $4n^2 \cdot 4n^2$ square matrix. $\boldsymbol{V_i^m}$ is the column matrix containing the voltage at the face of each mesh element in the conductor i. Hence, in the absence of propagation across the face of the conductor, $\boldsymbol{V_i^m}$ is a column vector with a single value. On the other hand, $\boldsymbol{I_i^m}$ is redefined as a column vector containing the currents flowing through each element of the i-th conductor, which are unknown and different, as depicted in Figure I-14b.

c) Admittance matrix derivation

The meshed admittance matrix, $\boldsymbol{Y^m}$,can be defined as:

$$\boldsymbol{I^m} = \boldsymbol{Y^m} \cdot \boldsymbol{V^m}, \tag{I-44}$$

where $\boldsymbol{Y^m} = (\boldsymbol{Z^m})^{-1}$, with an expanded form

$$\begin{bmatrix} \boldsymbol{I_{GND}^m} \\ \boldsymbol{I_{S1}^m} \\ \boldsymbol{I_{S2}^m} \\ \boldsymbol{I_{GND}^m} \end{bmatrix} = \begin{bmatrix} \boldsymbol{Y_{11}^m} & \boldsymbol{Y_{12}^m} & \boldsymbol{Y_{13}^m} & \boldsymbol{Y_{14}^m} \\ \boldsymbol{Y_{21}^m} & \boldsymbol{Y_{22}^m} & \boldsymbol{Y_{23}^m} & \boldsymbol{Y_{24}^m} \\ \boldsymbol{Y_{31}^m} & \boldsymbol{Y_{32}^m} & \boldsymbol{Y_{33}^m} & \boldsymbol{Y_{34}^m} \\ \boldsymbol{Y_{41}^m} & \boldsymbol{Y_{42}^m} & \boldsymbol{Y_{43}^m} & \boldsymbol{Y_{44}^m} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{V_{GND}^m} \\ \boldsymbol{V_{S1}^m} \\ \boldsymbol{V_{S2}^m} \\ \boldsymbol{V_{GND}^m} \end{bmatrix}. \tag{I-45}$$

At this point in the method, the conductor voltages $\boldsymbol{V_i^m}$ can be defined and the current distribution within the structure conductors $\boldsymbol{I_i^m}$ can be studied. For instance, specific excitations such as the common (i.e., $\boldsymbol{V_{S1}^m} = \boldsymbol{V_{S2}^m}$) or the differential (i.e., $\boldsymbol{V_{S1}^m} = -\boldsymbol{V_{S2}^m}$) can be defined. This is particularly interesting as it allows investigating possible flaws in a given CS-CPW (e.g. concentration of current in a lower-conductivity metal). To illustrate this, let us consider a CS-CPW with given geometry and a common-mode excitation. Hence, $\boldsymbol{V_{S1}^m} = \boldsymbol{V_{S2}^m} = \boldsymbol{1}$ and $\boldsymbol{V_{GND}^m} = \boldsymbol{0}$. Considering this, Figure I-15a plots the distribution of the normalized current magnitude in a cross-section of the structure at DC frequencies. Note that the current is equally distributed through the surface of both signal conductors and no current is induced in the ground strips, as for the induction of a current, a time-varying magnetic field is required (I-38). On the other hand, Figure I-15b displays the normalized current magnitude of the same structure at 100 GHz. Note that $t_S/2 \gg W_{S/G}$, thus the current crowds the upper and lower parts of the signal strips. In addition, due to the proximity effects and the considered

excitations, the current mostly crowds the outermost part of the signal strips. Finally, magnetic induction can be seen at the ground strips as an effect of the time-varying magnetic field.

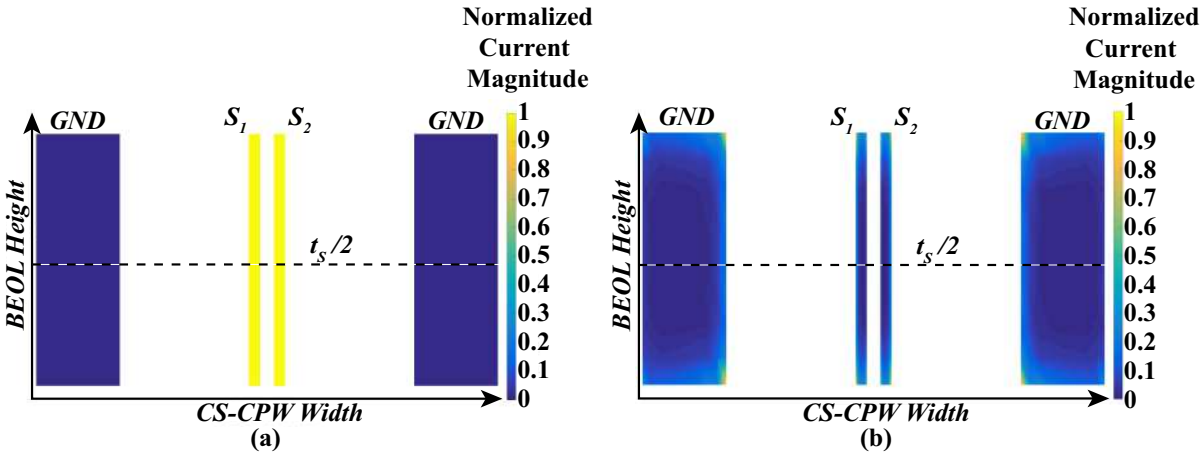

Figure I-15 Normalized current distribution in a CS-CPW with a common-mode excitation at (a) DC and (b) 100 GHz.

Then, the equivalent admittance of each conductor can be calculated as:

$$Y_{ij} = \sum^{n}\sum^{n} \boldsymbol{Y_{ij}^{m}}. \tag{I-46}$$

Next, the matrixes $\boldsymbol{Y_{ij}^{m}}$ (I-45) can be substituted with the scalar values obtained in (I-46) leading to the admittance matrix:

$$\begin{bmatrix} I_{GND} \\ I_{S1} \\ I_{S2} \\ I_{GND} \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \cdot \begin{bmatrix} V_{GND} \\ V_{S1} \\ V_{S2} \\ V_{GND} \end{bmatrix}. \tag{I-47}$$

d) Reduction of the matrix dimension

Both ground strips are assumed to be connected at the same voltage. Hence, a reduced admittance matrix, $\boldsymbol{Y^{r}}$,can be defined as:

$$\begin{bmatrix} I_{S1} \\ I_{S2} \\ 2I_{GND} \end{bmatrix} = \overbrace{\begin{bmatrix} Y_{22} & Y_{23} & Y_{21}+Y_{24} \\ Y_{32} & Y_{33} & Y_{31}+Y_{34} \\ Y_{12}+Y_{42} & Y_{13}+Y_{43} & Y_{11}+Y_{14}+Y_{41}+Y_{44} \end{bmatrix}}^{\boldsymbol{Y^{r}}} \cdot \begin{bmatrix} V_{S1} \\ V_{S2} \\ V_{GND} \end{bmatrix} \tag{I-48}$$

Finally, the reduced impedance matrix $\boldsymbol{Z^{r}}$ can be calculated as $\boldsymbol{Z^{r}} = (\boldsymbol{Y^{r}})^{-1}$, leading to:

$$\begin{bmatrix} V_{S1} \\ V_{S2} \\ V_{GND} \end{bmatrix} = \overbrace{\begin{bmatrix} Z_{S1} & j\omega M_{S2}^{S1} & j\omega M_{GND,p}^{S1} \\ j\omega M_{S1}^{S2} & Z_{S2} & j\omega M_{GND,p}^{S2} \\ j\omega M_{S1}^{GND,p} & j\omega M_{S2}^{GND,p} & Z_{GND,p} \end{bmatrix}}^{\boldsymbol{Z^{r}}} \begin{bmatrix} I_{S1} \\ I_{S2} \\ 2I_{GND} \end{bmatrix} \tag{I-49}$$

where Z_i is a complex value of the form $R_i + j\omega L_i$, where R_i and L_i are the resistance and partial self-inductance of the i-th conductor, respectively. M_j^i is the partial mutual-inductance between conductors i and j.

Note that after all these calculations, the resistances, partial self- and mutual-inductances now consider the frequency effects (e.g., skin effect) and proximity effects, as explained in [36].

e) Calculation of reduced model parameters

The reduction of the model leads to a simplification of the model in Figure I-11. Now, with the reduced model obtained in (I-49), only one ground strip is needed. This leads to the distributed model in Figure I-16.

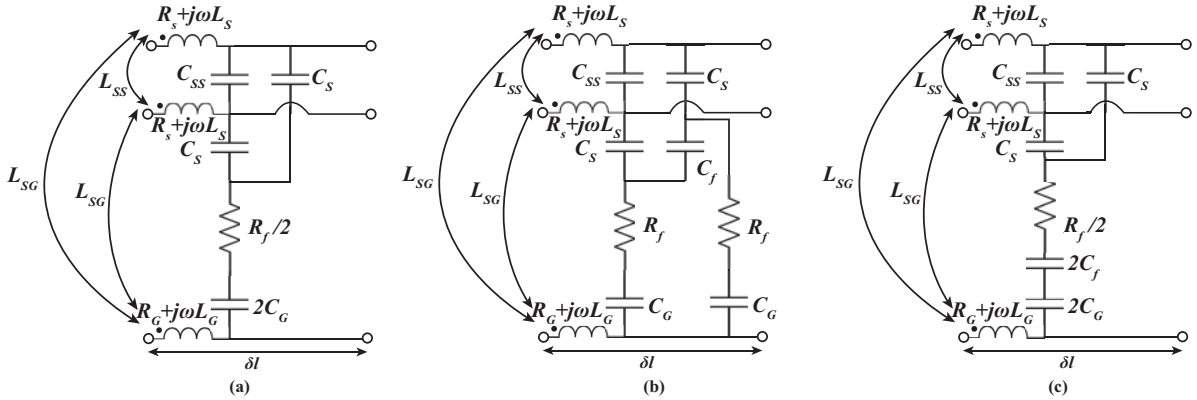

Figure I-16 Reduced distributed model of a lossy CS-CPW with an elementary length of with (a) uncut shield, (b) CC-shield and (c) SC-shield.

The value of the model parameters is calculated as follows. The capacitors are calculated using the methodology presented in [31] together with the new developments considered above. The signal and ground strips resistance ($R_{S/G}$) is calculated as $\Re(Z_{S/G})$, the signal and ground partial self-inductance ($L_{S/G}$) is calculated as $\Im(Z_{S/G})/\omega$ in (I-49). Finally, the partial mutual-inductance between signal or ground strips ($L_{SS/SG}$) is calculated as $\Im(j\omega M^{S}_{S/G,p})/\omega$ in (I-49). The resistance and inductance of the floating shield ribbons could also be calculated using a similar methodology to the one described in the present section. However, the designer might use thin layers for the integration of the floating shield, as they lead to reduced losses linked to eddy currents [28]. Hence, their resistance can be approximated using equation (I-43). However, the methodology described hereby may be applied without loss of generality.

The technique discussed in this section was applied to CS-CPWs. However, the number and shape of the mesh and/or conductors can be changed without loss of generality. Hence, this is a valid approach to analyze the magnetic interaction of n electrically short conductors.

I.2.4. Versatility of CS-CPWs

Using the method described above for the computation of the capacitances, resistances and inductances of the model, together with the equations (I-22) to (I-33), charts for k_L, k_C and Z_C can be built for a given technology. Charts containing this information are quite valuable for the designer as they allow narrowing down the range of geometries yielding the desired value for these parameters.

To illustrate this point as well as the possibilities offered by CS-CPWs in a given technology, some variations of the geometry of a CS-CPW were performed on the STM 55-nm BiCMOS technology. The considered technology has an ideal 8-metal BEOL for the integration of CS-CPWs, its BEOL features an ultra-thick metal 8 (ideal for passive circuits design and power routing), thick metals 6 and 7, and thin metals 1 to 5 (ideal for digital circuitry routing). A conceptual representation of the BEOL of this technology is shown in Figure I-17. Even though the BEOL in this technology is favorable to the design of CS-CPWs, similar BEOLs can be found in many other technologies.

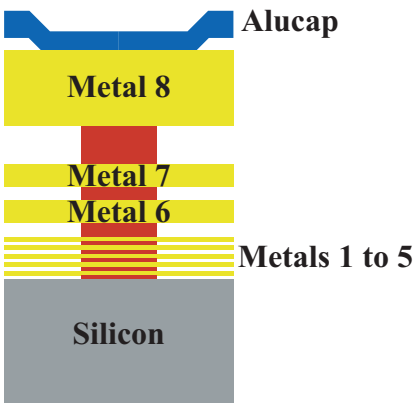

Figure I-17 Conceptual representation of the STM 55-nm BEOL.

In this study, a stack composed of metal 7 and metal 8 was used for the signal and ground strips. The floating shield was placed on metal 5, leading to a distance between signal/ground strips to the floating shield h of around 2 µm. In this context, S and W_G were fixed to 2 and 15 µm, respectively. SS and SL were fixed to 0.5 µm. Finally, for the SC- and CC-shielded structures, CS was fixed to 2 µm.

As a case-study example, in this configuration, we varied the ratios G/S and W_S/h in the ranges from 10 to 70 and 1 to 13, respectively. The operation frequency was set to 100 GHz. The derived $|k_C|$, Z_C and $|k_L|$ are plotted in Figure I-18a, Figure I-18b and Figure I-18c, respectively. Z_C is calculated as:

$$Z_C = \sqrt{Z_{even} \cdot Z_{odd}}. \tag{I-50}$$

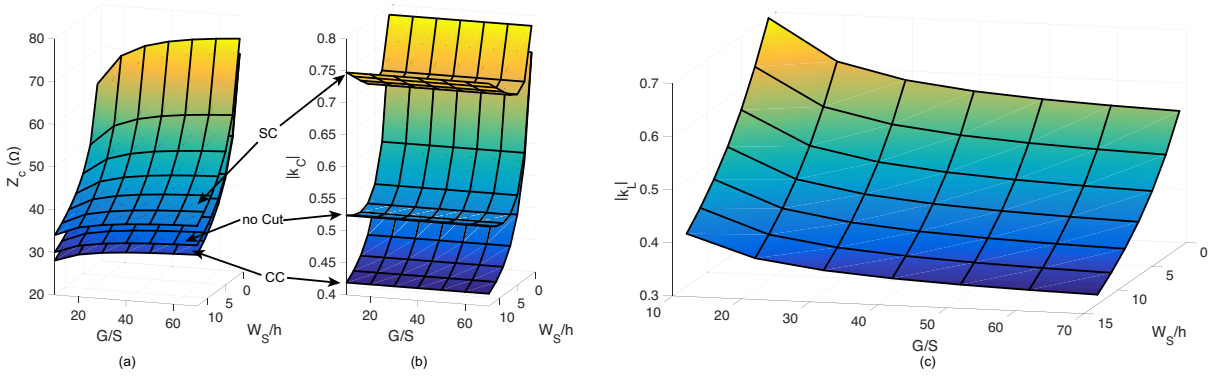

Figure I-18 (a) Characteristic impedance, (b) $|k_C|$ and (c) $|k_L|$ of a CS-CPW for the uncut, SC- and CC-floating shield. S=2µm, W_G=15 µm, SS=SL=0.5 µm, and CS=2 µm.

Note that $|k_L|$ has a singular value for a given geometry regardless of the shielding used as discussed earlier.

Some simple conclusions can be carried out from the charts in Figure I-18. Note that some of the conclusions discussed here depend on the relative magnitude between the model parameters (i.e., the considered geometries). Even though this prevents from enouncing universal rules for the CS-CPW design, the charts allow illustrating the behavior of the structure in a conventional BEOL using realistic dimensions.

First, in Figure I-18b, the electric coupling does not depend on the variation of G as long as this dimension is large enough to prevent a direct coupling between the signal and ground strips (which is the case for our study). Second, the electric coupling decreases with W_S for the CC-shielding case. This can easily be explained by the fact that C_{even} increases more rapidly than C_{odd}, the value of the latter being dominated by $2C_{SS}$. On the other hand, for the uncut and SC-shielding cases, the electric coupling coefficient first decreases and then increases with W_S/h. This is especially remarkable for the SC-shielding case. For the uncut shielding, this can be explained by the fact that for a very narrow strip

(i.e., small W_S/h ratio), the value of the even-mode capacitance is almost C_S. When the value of C_S starts increasing with W_S/h, C_{even} increases more rapidly than C_{odd}, leading to a decrease of $|k_C|$. However, if W_S/h further increases, the value of C_{even} is rapidly limited by the value of C_G, while C_{odd} continues to increase, leading to an increase of $|k_C|$. A similar reasoning can be followed to analyze the behavior of $|k_C|$ for the SC-shielding case. In this case, C_G is in series with C_f, making the change in the slope of $|k_C|$ happen for smaller values of W_S/h.

The behavior of the magnetic coupling coefficient can be analyzed in the same way. When G/S increases, the partial self-inductance of the signal strips (L_S) increases because the magnetic flux increases, and the partial-mutual inductance between signal and ground strips (L_{GS}) decreases due to the increased distance between those strips. On the other hand, the signal-to-signal partial mutual-inductance (L_{SS}) does not change according to G/S ratio. Based on these considerations, from equation (I-29) it can be derived that an increase of G/S leads to a decrease of $|k_L|$. On the other hand, the increase of W_S/h also leads to a decrease of the magnetic coupling coefficient. This can be easily explained by the fact that the signal-to-signal partial-mutual inductance decreases more rapidly than L_S, while L_G and L_{GS} are practically unmodified by the variation of W_S/h. Hence, this leads to a decrease of $|k_L|$ with W_S/h.

Finally, the charts in Figure I-18 show that it is possible to vary independently k_C and k_L, for a given value of Z_c. Thus, the intrinsic versatility of CS-CPWs with the added degrees of freedom brought by the variations in the shielding topologies present an ideal structure for the design of integrated couplers.

I.2.5. Application to mm-wave couplers

In this section, the design in the STM 55-nm BiCMOS technology and measurement of two 3-dB mm-wave backward CS-CPW-based couplers are presented. A first coupler is designed at 120 GHz, and a second at 185 GHz, respectively. As introduced earlier, design rules in modern CMOS/BiCMOS technologies limit the achievable coupling when strips are placed in a coplanar configuration. For instance, in the considered technology, for wide coplanar strips, the minimum distance in between two strips cannot allow achieving couplings higher than of 11 dB [25], when considering classical coupled microstrip lines. In this scenario, 3-dB couplers using coupled microstrip lines must be designed using a broadside architecture. However, limited isolation and relatively high return loss are achieved through this configuration, as discussed in section I.2.2.

a) Model-based design procedure for a 3-dB coupler

An ideal 3-dB coupler at its central frequency presents a coupling coefficient, k, of $1/\sqrt{2}$, as shown in (I-18). The coupling coefficient is equal to the magnitude of S_{31}, following the numeration used in this document. In its turn, k can be expressed as a function of the electric and magnetic coupling coefficients:

$$k = \frac{\sqrt{\left(\frac{1+k_L}{1-k_L}\right)\left(\frac{1-k_C}{1+k_C}\right)} - 1}{\sqrt{\left(\frac{1+k_L}{1-k_L}\right)\left(\frac{1-k_C}{1+k_C}\right)} + 1} \tag{I-51}$$

However, k is only an image of the power transmitted from the input to the coupled output, disregarding the directivity and characteristic impedance of the coupler. As previously discussed, great isolation is achieved in a backward coupler when (I-5) holds. Hence, it can be demonstrated that for (I-5) to hold, equal magnetic and electric coupling are required for a 3-dB coupler, leading to:

$$k = k_L = k_C = \frac{1}{\sqrt{2}} \approx 0.7. \tag{I-52}$$

Using the charts presented in the previous section, it is straightforward to see that for the design of a 3-dB coupler, the SC-shield yields a greater range of lateral dimensions for which (I-52) holds. Hence, this shield topology was chosen. Once the space of possible dimensions was narrowed down to a few possibilities, a model-based optimization was performed to obtain the dimensions giving the best performance. Finally, model-based results were validated by EM simulation with good agreement.

Model-based optimization showed that the optimum point in this technology is achieved using metals 7 and 8 connected through the maximum amount of vias allowed by the technology, to reduce the resistive losses. The model revealed that the use of fingers placed in the thin metal 5 leads to a relatively high slow-wave effect, leading to miniaturization, while reducing undesired eddy currents [40].

b) 120-GHz 3-dB coupler

The 3-dB coupler with a central frequency of 120 GHz was designed using the above considerations, leading to a length of 255 µm with the overall dimensions given in Table I-IV.

TABLE I-IV LATERAL DIMENSIONS OF THE 120-GHZ COUPLER.

W_S (µm)	S (µm)	G (µm)	W_G (µm)	$SS = SL$ (µm)	CS (µm)
2	1.8	20	15	0.5	2

The microphotograph of the 120-GHz 3-dB coupler is shown in Figure I-19 together with the measurement reference planes after a multimode TRL (Thru-Reflect-Line) calibration [41].

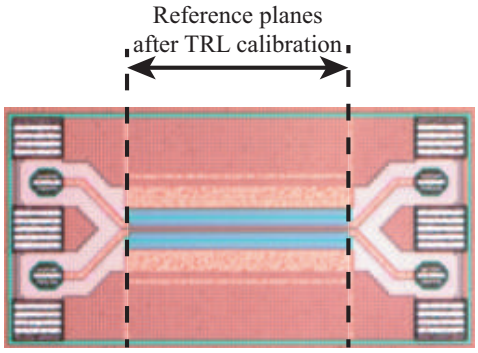

Figure I-19 Microphotograph of the 120-GHz 3-dB coupler and the reference planes after multimode TRL calibration.

The coupler was measured using an Anritsu VectorStar ME7838A4 4-ports Vector Network Analyzer (VNA), from 1 GHz to 145 GHz. A first-tier LRRM (Line-Reflect-Reflect-Match) calibration [42] was performed on a Formfactor 138-356 ISS (Impedance Standard Substrate) to set the reference planes at the probe tips. Subsequently, as a second-tier calibration, an on-wafer multimode TRL calibration [41] was performed in order to set the reference planes at the input/output of the coupler, as shown in Figure I-19.

A TRL calibration uses three calibration standards (i.e., Thru, Reflect, and Line). The main advantage of this calibration is that it allows positioning the reference planes at a given distance of the Device-Under-Test (DUT), usually the most interesting being at its input ports. For a reference plane at the input ports of the DUT, the Thru standard is built using the same access to the DUT. The Line standard is designed using the Thru accesses and a transmission line of a given electrical length θ_L and a given characteristic impedance Z_L placed between the input and output ports of the Thru. For the sake of simplicity, let us call this *middle* transmission line Offset Line. Finally, the Thru standard can be realized using any topology with the only condition of presenting a high reflection coefficient, Γ.

In addition, the TRL is a very relativistic calibration in comparison to other calibration methods such as the widely-used SOLT (Short-Open-Load-Thru), where all calibration standards responses are considered to be known. In a TRL, the only parameter which is assumed to be known is the characteristic impedance of the Offset Line, Z_L. However, in order to achieve a good calibration, the aforementioned impedance has to be properly measured by the Vector Network Analyzer (VNA). For this to happen, θ_L must be sufficient in order to distinguish Line and Thru standards despite the noise of the VNA and has to be sufficiently small to avoid the resonances appearing for $\theta_L = n\pi$. Hence, this practically limits the TRL calibration within a frequency band fixed by θ_L. In practice, as a rule-of-thumb with modern VNAs, the TRL calibration is valid for those frequencies where $10° < \theta_L < 170°$. In this work, the Line and Thru standards lengths were set to 850 µm and 300 µm, respectively. This leads to θ_L equal to 90º at 85 GHz. Hence, calibration is accurate in the 10-145 GHz band. The width of the strips was set to 7.7 µm and their spacing to 2 µm, leading to an even- and odd-mode characteristic impedance equal to 75 Ω and 25 Ω, respectively. These dimensions were chosen as they allow using the same access lines for the coupler, while presenting sufficiently similar phase velocities for the Line even- and odd-modes to avoid undesired resonances in the band of interest. Hence, following the expression in (I-50) the S-parameters after the on-wafer TRL are calibrated to 43 Ω. A subsequent renormalization was numerically performed to obtain S-parameters referenced at a 50-Ω impedance.

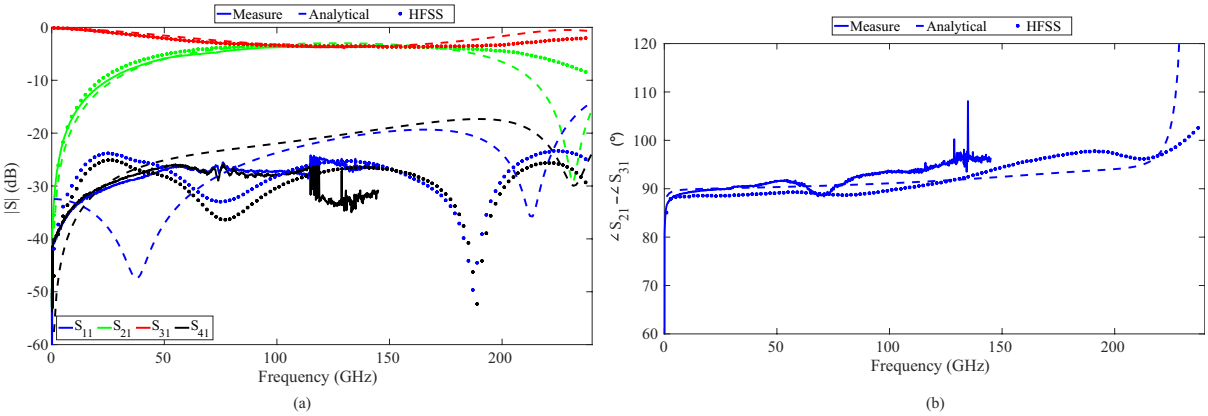

Figure I-20 (a) S-parameters magnitude of the 120-GHz 3-dB coupler: measurements (solid lines), analytical model (dashed lines), and 3D EM simulations (dots). (b) Phase difference between the through port (i.e., port 3) and the coupled port (i.e., port 2) seen from the input (i.e., port 1) of the 120-GHz coupler. measurements (solid lines), analytical model (dashed lines), and 3D EM simulations (dots).

Figure I-20a shows the magnitude of the S-parameters for the measurement (solid-line), analytical model (dashed-line) and 3D EM simulations (dots). Even though measurements could only be carried out up to 145 GHz, model-based and 3D EM simulation-based results are shown up to 240 GHz for comparison purposes. Some discontinuities are observed in the isolation (S_{41}) and return loss measurements (S_{11}); these resonances appeared after the second-tier calibration. Regarding the measurement results, at 120 GHz the coupler shows -3.7 dB at the through port, -3.6 dB at the coupled port, a return loss and an isolation of around 30 dB. At this frequency, the analytical model predicts -3.6 dB at the through port, -3 dB at the coupled port and around 22 dB of isolation and return loss. Finally, the 3D EM simulation predicted -3.6 dB at the through port, -3.5 dB at the coupled port and around 26 dB of isolation and return loss, in a good agreement with the measurement results and the proposed analytical model.

Above 180 GHz it can be observed that the EM simulation and the model-based results diverge. This can be easily explained by a difference in the magnitude of some of the parameters in the distributed model, which make the coupler resonate at a lower frequency than the one given by EM simulation.

Figure I-20b shows the phase difference between the through port and the coupled port seen from the input (i.e., $\angle S_{31} - \angle S_{21}$), for the measurement (solid-line), model- (dashed-line) and EM-based (dots) datasets. At 120 GHz, the phase difference between these two ports is around 94º, with almost a flat curve throughout most of the measured frequency band. The maximum error in the

measurement (as compared to ideal case of 90°) is 7°. Note that in Figure I-20b, the model-based results show an overall better agreement with the measurement results, as compared to the EM-based results. Again, the resonance at the frequency for which the coupler reaches an electrical length of $\lambda_G/2$, where λ_G is the guided electrical length, can be observed around 230 GHz, leading to disagreement between the EM- and model-based data sets.

Finally, Figure I-21 shows the even-, odd-, and mixed-mode characteristic impedance of the measured (solid-line), EM- (dots) and model-based (dashed-line) data sets. These characteristic impedances could be measured thanks to the use of a 4-ports VNA.

The agreement between measurement (solid-line), model- (dashed-line) and EM-based (dots) results is very good for the odd-mode characteristic impedance over the whole bandwidth, from DC to 145 GHz. On the contrary, the agreement for the even-mode characteristic impedance is less good, with a difference of 10 to 15% between the measurement, model- and EM-based results. Consequently, the difference on the mixed-mode impedance is of the order of 5 to 8%.

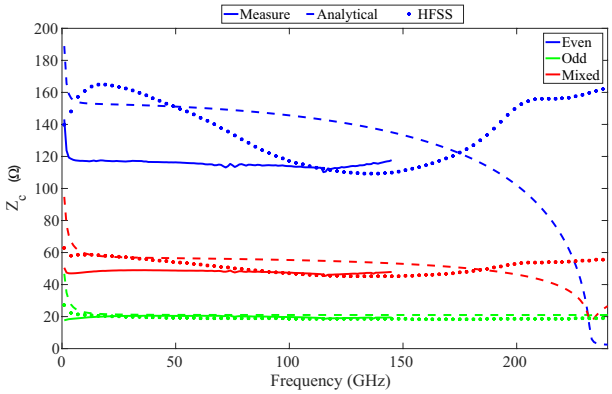

Figure I-21 Even-, odd- and mixed-mode characteristic impedances for the three considered datasets for the 120-GHz coupler. Measurement, analytical model, and 3D EM simulation results are represented as solid-lines, dashed lines and dots, respectively.

c) 185-GHz 3-dB coupler

Beyond demonstrating the feasibility of the proposed design methodology, our second case study has been designed with the additional goal of demonstrating the feasibility and performance of the CS-CPW structure for the upper end of the mm-wave band. For the 185-GHz coupler case study, the design methodology was similar to that used for the 120-GHz coupler. The length of the 185-GHz coupler is 140 µm, the other dimensions being given in Table I-V. The same metal layers as for the 120-GHz coupler were used for the ground and signal strips as well as for the floating ribbons. Finally, a cut of 2 µm was also performed on the side of the floating ribbons, in a SC-shielding configuration.

TABLE I-V LATERAL DIMENSIONS OF THE 185-GHZ COUPLER.

W_S (µm)	S (µm)	G (µm)	W_G (µm)	$SS = SL$ (µm)	CS (µm)
2	2.4	20	15	0.5	2

The measurement of the 185-GHz coupler was performed with a 4-ports VNA up to 145 GHz, and with a 2-ports VNA above 145 GHz. From 1 GHz to 145 GHz, the 185-GHz coupler was measured using 4-ports setup on an Anritsu VectorStar ME7838A4 Vector Network Analyzer (VNA) with a first-tier LRRM calibration and a second-tier on-wafer multimode TRL calibration, as for the 120-GHz coupler. The microphotograph of the fabricated device used for this measurement, together with the reference planes after TRL calibration is shown in Figure I-22.

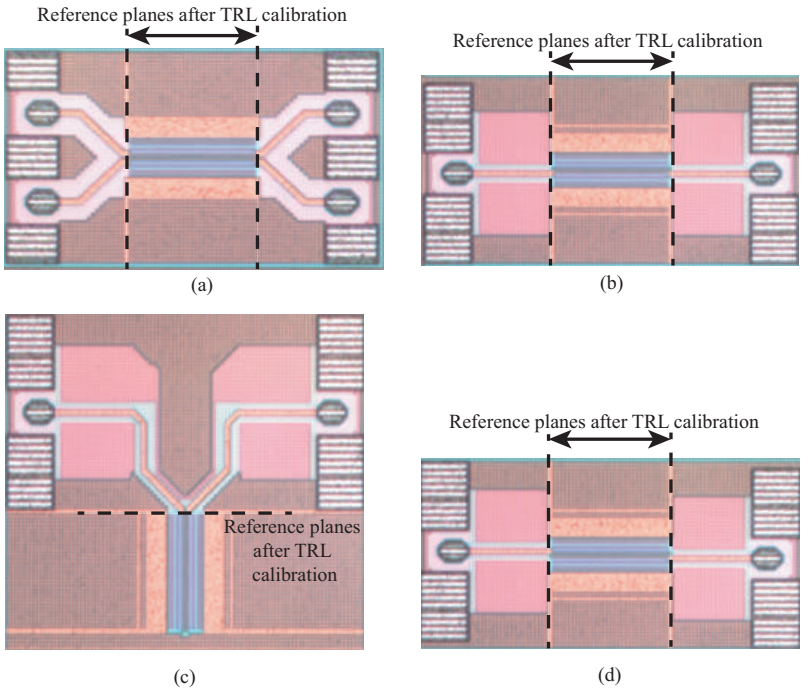

Figure I-22 Microphotographs of the 185-GHz coupler and the reference planes after TRL calibration for: (a) 4-ports measurement, (b) 2-ports measurement of the Thru, (c) 2-ports measurement of the coupling, and (c) 2-ports measurement of the isolation.

Measurements from 140 GHz up to 220 GHz were performed at IEMN as 2-ports measurements using an Oleson extender associated to a R&S VNA. For each of the measurements, a first-tier LRRM calibration was performed on a commercial ISS substrate and a subsequent 2-ports second-tier TRL [43] calibration was carried out in order to set the reference planes at the input/output of the coupler. The 2-ports TRL was performed on a Line of length 520 µm and a Thru of length 200 µm, leading to θ_L of 105° at 140 GHz and 165° at 220 GHz. Z_L was set to 50 Ω, leading to measured S-parameters referenced to this impedance.

In order to characterize the 185-GHz coupler above 140 GHz, three circuits were fabricated, each circuit making it possible to measure two S-parameters among four. For each measurement, the two ports that are not being measured were loaded with 50-Ω on-wafer loads. Figure I-22b, I-21c and I-21d show the three circuits that were used to measure the S-parameters of the 185-GHz coupler at the through, coupled and isolation ports, respectively.

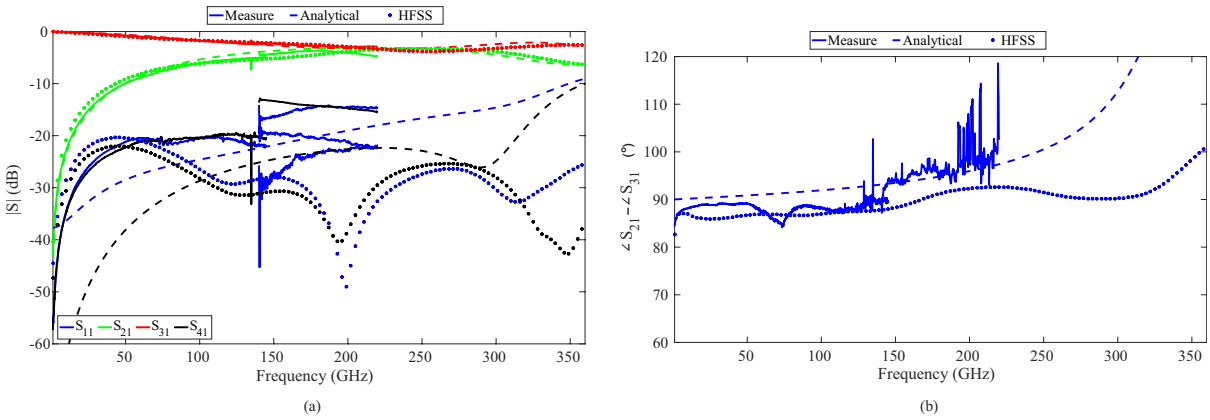

Figure I-23 (a) S-parameters magnitude of the 185-GHz 3-dB Coupler. Measurement is represented as solid-lines, the analytical model results are plotted using dashed lines and the 3D EM simulation results are the depicted as dots. (b) 15 Phase difference between the through port (i.e., port 3) and the coupled port (i.e., port 2) seen from the input (i.e., port 1) of the 185-GHz coupler.

Figure I-23a shows the measured (solid-line), EM- (dots) and model-based (dashed-line) S-parameters of the coupler from 1 GHz up to 360 GHz (up to 220 GHz for measurement data). Note that, in the 140-220 GHz band, for the measurement results, three sets of $|S_{11}|$ are plotted. These correspond to the return loss of each of the three measurements performed in this band.

In the 1-145 GHz band, all three data sets show very good agreement. Beyond, the measurements continuity between this band and the 140-220 GHz band is not very good for the return loss and the isolation ($|S_{41}|$). This can be easily explained due to the parasitic effects of the on-wafer loads. The validity of this hypothesis can be easily seen for the return loss. When considering a symmetrical passive structure, symmetry in its S-Parameters is also expected. For example, when the measurement of the isolation is performed, if the on-wafer load presents some reactive parasitic, some signal is transmitted from the input to the theoretically isolated port, similarly to the working principle of Reflection-Type Phase Shifters (RTPS). Even though these effects impact all the measured S-parameters of the coupler, those parameters whose magnitude is smaller (i.e., return loss and isolation), suffer from a greater relative deviation. This is why the three return loss curves measured on the 140-220 GHz band vary by more than 10 dB between them. Hence, with a 4-ports measurement, where all ports are 50 Ω, better isolation and return loss could be expected. At 185 GHz, the measured, EM- and model-based results show a coupling of 3.7, 4.2 and 3.2 dB, respectively. The through port presents -2.9, -2.6 and -3.1 dB for the measurement, EM- and model-based results, respectively. The EM- and model-based isolation (return loss) are 20 dB (23 dB) and 37 dB (37 dB), respectively.

Next, in the 220-360 GHz band, the through and coupled S-parameters present good agreement between the analytical model and the 3D EM simulations. However, as for the previous 120-GHz coupler, the isolation and return loss between these datasets diverge when considering frequencies for which the coupler electrical length gets closer to $\lambda_G/2$. This is especially remarkable above 300 GHz.

Figure I-23b displays the phase difference between the through and coupled ports seen from the input, for the measurement (solid-line), EM- (dots) and model-based (dashed-line) datasets. The agreement between measurement, EM- and model-based results is very good. At 185 GHz, the phase difference is equal to 95°, 95° and 91° for measurement, EM- and model-based results.

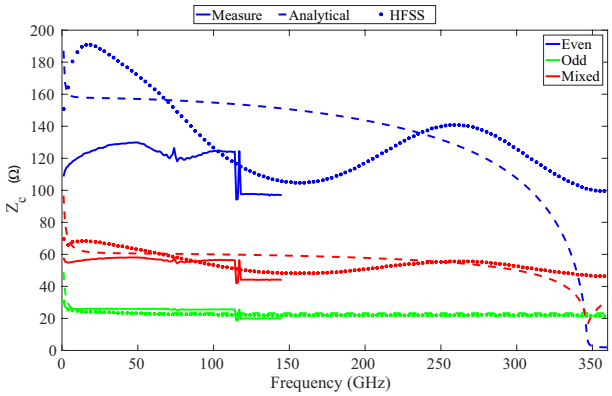

Figure I-24 Even-, odd- and mixed-mode characteristic impedances for the three considered datasets for the 185-GHz coupler, extracted from measured (solid-line), HFSS- (dots) and model-based (dashed-line) S-parameters.

In Figure I-24, the odd-, even- and mixed-mode characteristic impedances are shown. As for the 120-GHz coupler, the agreement between measurement (solid-line), model- (dashed-line) and EM-based (dots) results is very good for the odd-mode characteristic impedance, from DC to 145 GHz. On the contrary, the agreement for the even-mode characteristic impedance is limited, with a difference of 10 to 15% between the measurement, EM- and model-based results. Consequently, the difference on the mixed-mode impedance is of the order of 5 to 8%.

I.2.6. Comparison to the state-of-the-art

To put the performance of the measured couplers into perspective, we present a direct comparison between our experimental results and state-of-the-art designs in the literature. Table I-VI summarizes this comparison with the

state-of-the-art couplers presented in Table I-I.

TABLE I-VI COMPARISON TO THE STATE-OF-THE-ART MM-WAVE COUPLED-LINE COUPLERS.

Ref.	**This work**	**This work**	[20]	[21]	[22]	[23]	[24]	[25]***
Tech.	**55-nm BiCMOS**	**55-nm BiCMOS**	35-nm GaAs	130-nm BiCMOS	180-nm CMOS	0.35-µm BiCMOS	65-nm CMOS	55-nm BiCMOS
Topology	**CS-CPW**	**CS-CPW**	Broadside	SL-Broadside	Meandered CCS CL	Meandered Broadside	*Braided* CS-CPW	CS-CPW
Frequency (GHz)	**120**	**185**	270	60	40	75	90	60
Through (dB)	**3.7**	**2.9**	3.9	3.9	4.5	4	3.5	3.3
Coupling (dB)	**3.6**	**3.7**	4.1	3.8	4.5	4	4.4	3.5
Return Loss (dB)	**>25**	**>15**‡	>13	>25	>13	>15	>18	29
Isolation (dB)	**>25**	**>15**	>17	>25	>18	17***	-	28
1-dB BW (GHz)	**110**†	**80**†	51†	34	20	30	55	-
±3º BW (GHz)	**180**†	**75**†	51‡	47**	10	30	>60	-
Size* (λ^2)	**0.003**	**0.0045**	0.013	0.003	0.005	-	0.001	0.003

†Analytical model considered for the upper-band calculation ‡Worst-case *Free-space wavelength ††-0.5 dB BW ‡‡±1.4º BW **±1º BW ***Simulation

The 120-GHz coupler presented in this work shows the best matching and isolation over an ultra-wideband among all the couplers considered in Table I-VI. In addition, the 120-GHz coupler presents one of the lowest magnitude imbalance between its through and coupled ports. If a bandwidth defined at 1 dB from the maximum coupling level is considered, the 120-GHz coupler presents a bandwidth as high as 110 GHz, the upper-end of this bandwidth being estimated from the analytical model simulation. Using the same considerations, if a bandwidth at ±3º is considered regarding its central frequency, this coupler presents around 180 GHz of bandwidth.

The 185-GHz coupler, even though better results may be expected from a 4-port characterization, presents a magnitude imbalance of 0.8 dB, which is of the same order of magnitude as the coupler reported in [24]. In addition, it presents an isolation and return loss also comparable to the other couplers.

To further compare with other coupler topologies, i.e., not based on coupled-lines, state-of-the-art branch-line couplers were also considered for to be compared with the designed couplers. The results of this comparison are summarized in Table I-VII.

TABLE I-VII COMPARISON TO THE STATE-OF-THE-ART BRANCH-LINE COUPLERS.

Ref.	**This work**	**This work**	[44]	[45]	[46]	[47]
Tech.	**55-nm BiCMOS**	**55-nm BiCMOS**	130-nm BiCMOS	130-nm BiCMOS	90-nm CMOS	22-nm CMOS
Topology	**CS-CPW**	**CS-CPW**	Meander	QLQC	EC-CPW	SW-MS
Frequency (GHz)	**120**	**185**	60	62	62	60
Through (dB)	**3.7**	**2.9**	4	3.8	4.8	4.5
Coupling (dB)	**3.6**	**3.7**	5	4.1	5.5	5.3
Return Loss (dB)	**>25**	**>15**‡	15	13	22	18
Isolation (dB)	**>25**	**>15**	14	13	17	22
1-dB BW (GHz)	**110**†	**80**†	-	4	6.5	32
±3º BW (GHz)	**180**†	**75**†	19**	10.5	9	14
Size* (λ^2)	**0.003**	**0.0045**	0.001	0.0015	0.004	0.0027

†Analytical model considered for the upper-band calculation ‡Worst-case *Free-space wavelength **±2º BW

Authors in [44] show a coupled-line Lange coupler at 60 GHz using meandered lines to reduce the area overhead. In [45], two Quasi-Lumped Quadrature Couplers (QLQC) (i.e., hybrid couplers loaded by lumped components) are presented. The capacitors load the transmission lines conforming the hybrid couplers, artificially increasing their effective dielectric constant, thus leading to an area overhead reduction. In [46] it is reported a similar approach to [44] and [45]. In [46], the transmission lines are loaded with Metal-Insulator-Metal (MIM) capacitors as well as meandered to achieve a reduction in the area overhead. Finally, in [47] is reported a hybrid coupler at 60 GHz using a meandering technique together with Slow-Wave MicroStrip lines (SW-MS) to further decrease the surface.

The overall superior performance, especially in terms of bandwidth, between coupled-line couplers and branch-line couplers can be seen by comparing Table I-VI and Table I-VII results. The 120-GHz coupler shows the best matching, isolation and lowest magnitude imbalance among all the couplers considered in Table I-VII. On the other hand, the 185-GHz coupler presents a low magnitude imbalance of 0.8 dB, which is of the same order of magnitude as the other reported couplers. In addition, it presents an isolation and return loss also comparable to the other couplers.

To summarize, two CS-CPW-based coupled-line couplers were presented, which report the highest central frequencies ever reported in the CMOS and BiCMOS literature. Moreover, they present better or state-of-the-art performance, with comparable sizes to other existing mm-wave couplers thanks to the use of slow-wave propagation. These results validate the robustness of the CS-CPW structure for the design of mm-wave couplers.

I.3. Conclusions

In this chapter, the theoretical background of hybrid and coupled-line couplers has been discussed, focusing on the backward-wave coupled line couplers. The intrinsic advantages of the coupled-lines couplers against its hybrid couplers counterparts has been discussed. In addition, the technological issues for the integration of directive 3-dB couplers were presented. In this scenario, CS-CPWs were shown to be a very good candidate due to their many degrees of freedom, enabling fine tuning of the propagation velocities of the even- and odd-mode independently, thanks to different

shielding topologies available. Then, distributed electrical models were proposed for each of the shielding topologies.

Next, a detailed methodology was presented for the implementation of an analytical model aiming to simulate the performance of these couplers in a much faster way than a 3D-EM simulator. Afterwards, using the proposed distributed models and the analytical analysis, some charts were plotted in the STM 55-nm BiCMOS technology showing the versatility of the CS-CPWs in an integrated technology.

Then, two 3-dB CS-CPW-based backward-wave couplers were designed using the analytical model with central frequencies of 120 GHz and 185 GHz, respectively. Measurement, EM simulation and model-based simulation results show good agreement for the designed couplers.

Finally, the presented couplers were compared to the state-of-the-art mm-wave couplers showing very good performance, as well as reduced dimensions thanks to the slow-wave effect.

Chapter II

VARACTORS

In Chapter I, the design of the 3-dB couplers was presented. The next key element in the RTPS architecture are varactors. These lumped elements allow the RTPS to be tunable. Varactors are, by definition, 2-port electronic devices that present a variable capacitance. These devices are found in many applications, either for performing necessary RF functions, such as tuning of VCOs [48], phase-shift control, in particular to build beam-steering systems allowing to compensate the increase of path-loss in free space [49], [50], or for calibration purposes, [51], [52] etc.

The performance of a varactor is mostly defined using three metrics: (i) the tuning ratio, which is expressed as the ratio between the maximum and minimum capacitances (C_{max}/C_{min}), (ii) the Quality-factor (Q-factor), a metric relating the magnitudes of the reactance and resistance of the device, and (iii) the linearity. High tuning range, high Q-factor and highly linear tunable devices are required for state-of-the-art applications. However, these three parameters appear as a trade-off, and the Q-factor of varactors tends to decrease with the working frequency (as for most of passive lumped elements). In this scenario, the design of novel devices with high tuning range and high Q-factor is a key issue in the mm-wave frequency bands. As for most of tunable electronic devices, the varactor capacitance can be tuned using two main approaches: (i) mechanically or (ii) electrically.

Much like most of the tunable components used in the end of the 19th century, varactors were born as mechanically-tuned devices. Generally, the variation of capacitance obtained for these mechanically-tuned elements is achieved through the modification of the capacitor shape. For instance, in [53], authors report the invention of Korda, which was the first form of a mechanically-tuned varactor in an air dielectric. The device consisted in semicircular metal plates, which were alternatively connected to each of the two electrodes of the capacitance. Through the turning of a shaft, the overlapping ratio between the semicircular plates could be modified and hence, the capacitance of the device. A more modern form of mechanical varactors is found nowadays with Microelectromechanical Systems (MEMS). Even though some MEMS are activated using an electric signal, the operation through which the capacitance is varied still relies on a mechanical force. MEMS are found in some applications in the current electronic devices, such as gyroscopes and accelerometers. However, their compatibility with standard CMOS/BiCMOS processes, size and durability still remains an issue. Hence, in the present document, only silicon-based devices will be discussed.

On the other hand, electrically-tuned varactors are found in countless applications and contexts. Their reduced size and, most importantly, their high-compatibility with CMOS/BiCMOS technologies (and even III-V technologies) makes them a perfect candidate for direct use in modern consumer applications. Silicon-based varactors were born hand-to-hand with the first silicon-based transistors (as natural devices in a bipolar transistor) and their direct use for tuning applications started even before the advent of the MOSFET [54]. Unlike MEMS, these are solid-state devices. Hence, the variation in the capacitance is achieved through the tuning of the energy levels in semiconductor materials. Within this operation mode, a first broad classification can be done into two categories: (i) diodes and (ii)

Metal-Oxide-Semiconductor Field-Effect Transistor-based (MOSFET-based). Diodes are formed by two semiconductor materials and their capacitance is varied by tuning the width of the depletion region in between them using a DC-voltage. On the contrary, a DC-voltage applied at the gate of a MOSFET controls the concentration of charge carriers in its channel, and hence its capacitance. This first classification is important as it divides the varactors under the condition whether a DC current can pass through the device or not (disregarding breakdown voltage and leakage). As it will be discussed later, in a given technology, devices that under certain biasing voltages allow a *desired* current flow between the two electrodes of the varactor (i.e., diodes) tend to suffer from an overall greater *undesired* leakage, as compared to the MOSFET-based varactors.

This chapter is organized as follows, section 1 presents a behavioral description of on-silicon varactors integrated using: (i) PN junctions, and (ii) MOSFETs. Next, in section 2, a more in-depth analysis among the MOSFET-based varactors is carried out. The MOSFET-based varactors are classified into two main topologies: (i) Accumulation-mode MOS (A-MOS), and (ii) Inversion-mode MOS (I-MOS) varactors. A behavioral description of these topologies described in this section. Then, a discussion on the circuitry needed for the practical implementation of these devices as well as the frequency behavior of their Q-factor is carried out. In this section, it is shown that at the upper-band of the mm-wave frequencies, I-MOS shows a better behavior and that the needed circuitry for its practical implementation is simple, when thin-oxide devices are considered. Based on these conclusions two demonstrators are implemented in the 55-nm STM BiCMOS technology: (i) a classical I-MOS varactor, and (ii) a Common-Source MOSFET acting as a varactor. As explained in the introduction of this manuscript, this thesis aims at the design of high-performance mm-wave phase shifters. In these frequencies, as stated earlier in this document, the Q-factor of traditional A-MOS varactors is quite limited. Hence, innovative varactor topologies must be investigated. Finally, in section 3, the main conclusions of this chapter are drawn.

II.1. Junction-based varactors

As introduced earlier, diode varactors are built using a junction between one semiconductor and another or more materials, which in their turn can be semiconductors. Several categories of these diodes have been reported in the literature (e.g., Schottky, Zener, avalanche, PIN…), depending on the nature of the materials used. For the sake of simplicity and because they are natural devices in any CMOS/BiCMOS technology and thus found in any silicon-based technology, only PN junctions will be considered in the present document.

A PN junction is composed by two types of semiconductors that have been doped to present an excess (i.e., N-type) or a lack of electrons (i.e., excess of holes, leading to a P-type), as compared to the natural state of the semiconductor (e.g., silicon). Through the application of a DC voltage, the number of electrons/holes present in each semiconductor type can be controlled to further increase or reduce the difference in charge carriers between them. Figure II-1a depicts a physical implementation, symbol and port nomenclature of a PN diode.

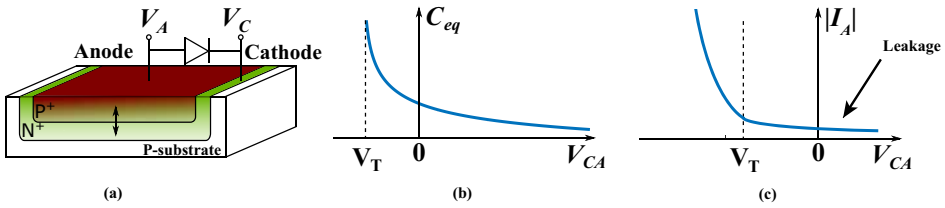

Figure II-1 (a) PN junction and its symbolic representation as a diode. The arrows depict the movement of the charge carriers when the voltage difference between cathode and anode (V_{CA}) increases. (b) Capacitance versus V_{CA}. (c) Magnitude of the I_A current versus V_{CA}.

First, let us discuss the crowding of the semiconductors composing the diode with electrons/holes as a function of the voltage difference between cathode and anode, V_{CA}. For the sake of simplicity, the P-substrate and the N-type semiconductor are considered to have an electric potential of 0 V. In such a device, when $V_{CA} = 0$, the mobile carriers close to the junction diffuse, creating a

depletion region near the PN interface. If a bias voltage $V_{CA} < 0$ is applied, the PN junction is said to be forward biased. Under this consideration, as compared to the unbiased state, the holes in the P region and the electrons in the N region are pushed to the interface, thus reducing the width of the depletion zone. For bias voltages $V_{CA} < V_T$, where V_T is the threshold voltage of the junction, the depletion region becomes thin enough to allow conduction across the PN interface. For voltages $V_{CA} > 0$, the junction is biased in the so-called reverse bias. The holes in the P region (electrons in the N region) are pulled away from the junction, thus increasing the width of the depletion region (until the diode breaks down or enters in avalanche conduction).

From an electrical point of view, for biasing voltages $V_{CA} > V_T$ the PN junction can be modelled as a variable capacitance. The magnitude of voltage V_{CA} controls the width of the depletion region and hence the value of the junction capacitance. If the equivalent capacitance, C_{eq}, is considered as follows:

$$C_{eq} = \frac{-1}{\Im(Z_{eq}) \cdot \omega}, \tag{II-1}$$

where, Z_{eq} is the input impedance seen from the anode and ω the angular frequency, the magnitude of C_{eq} as a function of V_{CA} can be plotted. Figure II-1b depicts this relationship.

Note that for a reverse bias where $V_{CA} \approx V_T$, a very high variation of C_{eq} is obtained. However, in this operating region, two main issues appear. First, the leakage current for $V_{CA} \approx V_T$ is not negligible. An ideal diode, would show null leakage for $V_{CA} > V_T$ and a vertical asymptote at the threshold voltage. Thus, behaving like an ideal open- (short-) circuit for $V_{CA} > V_T$ ($V_{CA} \leq V_T$). However, on-silicon diodes are far from ideal devices. When diodes are operated near V_T, the depletion zone is very small. Hence, conduction paths are created in some regions of the junction due to doping inhomogeneity, leading to leakage currents that lower the Q-factor of these devices. The inverse relationship between leakage currents and V_{CA} is shown in Figure II-1c. As perfect doping homogeneity is never achieved in integrated technologies, these devices show leakage currents even for great values of V_{CA}.

As a second issue, the application of high-power RF signals when the diode is backward-biased near its threshold voltage results in high-power harmonics due to self-biasing issues. The large signal modulates the width of the depletion region. Note that C_{eq} presents a great slope under this biasing condition. In fact, devices under this configuration are used for frequency multipliers, which are systems requiring highly-nonlinear loads [55].

Hence, when highly linear devices are required (e.g., in an emitting chain), these two issues usually favor a biasing of these devices of $V_{CA} \gg V_T$, limiting the tuning range of these devices.

In addition, the overall Q-factor of these devices is often limited by their accesses (e.g. buried collector). To summarize, even though these devices represent a simple solution for the integration of varactors, their intrinsic trade-offs generally make them a less interesting option than their MOSFET-based counterparts [56].

II.2. MOSFET-based varactors

MOSFETs are, as their name indicates, field-effect transistors. These devices rely on the electric field confined between their gate and n/p-well to tune the characteristics of the channel between their drain and source ports. Hence, MOSFETs are by nature devices that rely on capacitive effects to operated. Let us consider an n-MOS with its drain (D), source (S) and body (B) connected together as shown in Figure II-2.

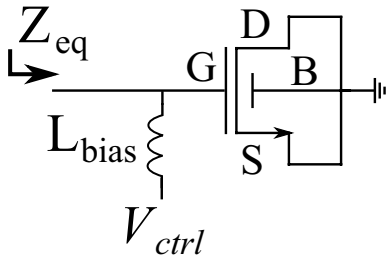

Figure II-2 nMOS with D, S and B connected together.

Such a device performs as a variable capacitance between its gate (G) and B (i.e., D and S) ports, whose value is a function of the voltage difference between body and gate accesses (V_{BG}). In Figure II-2, V_{BG} is equal to $-V_{ctrl}$, which is applied through an ideal biasing inductance L_{bias} placed at gate level. Such a device can work in the accumulation mode for $V_{BG} > V_T$, where V_T is the threshold voltage of the transistor, when the voltage difference between the bulk silicon and the gate of the transistor is positive and high enough to allow charge carriers to move freely. This device can also work in the inversion mode, where an inversion channel with mobile electrons builds up, for $V_{BG} < -V_T$. Between these two regions, the depletion region takes place, where there are very few charge carriers at the gate oxide interface. These operating regions together with the equivalent capacitance are plotted in Figure II-3.

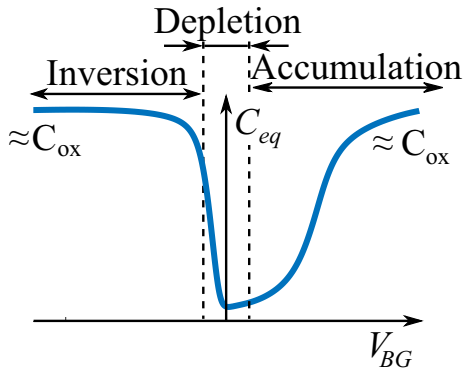

Figure II-3 Input capacitance versus V_{BG}

The maximum capacitance of these varactors in the strong-accumulation (i.e., $V_{BG} >> V_T$) and strong-inversion (i.e., $V_{BG} << -V_T$) regions is approximated to to $C_{ox} = \epsilon_{ox} \cdot S/t_{ox}$ (neglecting second-order effects such as the quantum capacitance that slightly reduces this maximum value), where ϵ_{ox} is the oxide dielectric constant, S the channel area and t_{ox} the oxide thickness.

Note that in such a device, the origin of leakage currents is manly restricted to the gate oxide. For silicon-based technologies, this oxide is usually formed using SiO_2. Silicon dioxide is an insulating material and hence, theoretically, no leakage should be observed. However, in real devices, the gate oxide contains impurities that lead to undesired leakage. On the other hand, as compared to PN junctions, the material within the electric field is confined is a natural dielectric. Hence, its leakage is relatively constant for any V_{ctrl}. In such an architecture, the losses are mainly due to interconnections to the BEOL and the resistivity of the channel, drain/source implants and gate.

Modern CMOS/BiCMOS technologies tend to reduce the gate oxide thickness of MOSFETs as it leads to a reduction in the voltage needed to drive these transistors. This is a pretty straightforward effect; thicker gate oxides separate further apart the gate and the channel regions. Hence, a greater amount of charge is needed at gate level to drive the channel. Reducing t_{ox} has two main effects, (i) the reduction of the transistor consumption as it can be driven with lower voltages, and (ii) the increase of the transistor transit frequencies, f_T, as it allows the reduction of the gate length. Transistors in advanced technologies have oxide thicknesses in the order of 1 nm. On the other hand, the reduction of the gate oxide thickness leads to greater leakage. For this reason, many MOS-based varactors use thick-oxide topologies to reach acceptable leakage.

Note that the topology in Figure II-3 is interesting for single-ended varactors, as one port is always connected to the bulk silicon. However, many applications require varactors with two operative ports (e.g., VCOs). In this scenario, variations of the topology presented Figure II-2 can be envisioned, leading to Accumulation-mode MOS (A-MOS) and Inversion-mode MOS (I-MOS) varactors.

II.2.1. A-MOS varactors

A-MOS varactors are built from traditional MOS transistors with a variation in drain/source doping to ensure that they operate either in depletion or accumulation modes, never entering in the inversion mode. Such doping variations usually consist in N^+-drain/source implants in an N^--well. Figure II-4 displays the topology of an A-MOS varactor.

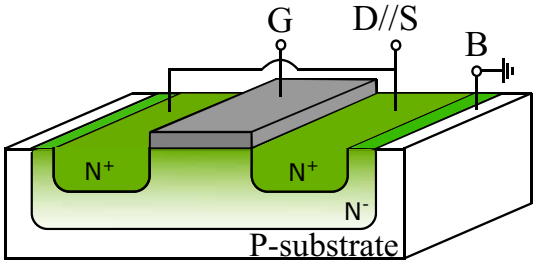

Figure II-4 A-MOS varactor physical implementation.

For the sake of simplicity, let us name the ports of the A-MOS as if it was a traditional transistor (i.e., gate (G), drain (D), source (S), and body (B)). When the B of such device is connected to the ground, its D and S ports are connected together and a control voltage is applied to G, the device acts as a varactor between its G and D ports. The equivalent capacitance seen from D level, as a function of the voltage difference between G and D, $V_{G,DS}$, is displayed in Figure II-5.

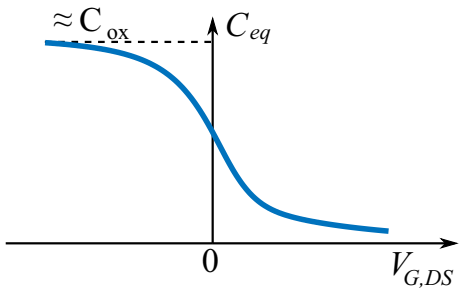

Figure II-5 Capacitance of an A-MOS varactor at D//S level versus $V_{G,DS}$.

These devices present a large tuning range and low parasitic resistance [56]–[58]. However, they require a differential voltage between their ports that usually goes from $-V_{DD}/2$ to $+V_{DD}/2$, for devices integrated using the typical oxide thickness of the technology, or $-V_{DD}$ to $+V_{DD}$ for devices designed using a thicker oxide. The voltages needed to drive a thick-oxide A-MOS are merely illustrative as it depends on the oxide thickness available in the technology. However, note that the increase of the oxide thickness is inversely related to the capacitance per unit of gate surface. Hence, very thick oxides are not usually available in the technology as they lead to large footprints. In the present document, let us consider that thick-oxide devices have voltage ratings of $2 \cdot V_{DD}$.

II.2.2. I-MOS varactors

I-MOS varactors are based on classical nMOS or pMOS transistors. When the drain and the source are connected together, the body is connected to the ground (to V_{DD}, for the pMOS-based I-MOS) and a control voltage is applied to the gate, this configuration leads to an equivalent variable capacitance between its D and G ports, as for the A-MOS. This configuration is depicted in Figure II-6.

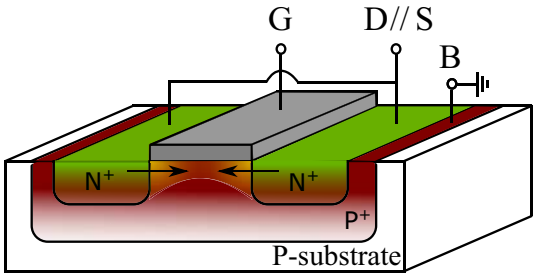

Figure II-6 n-MOS-based I-MOS varactor physical implementation.

The effective capacitance at gate level, calculated as in (II-1), is a function of the voltage difference between the gate and the drain ($V_{G,DS}$), as shown in Figure II-7. For an n-MOS-based I-MOS varactor, when $V_{G,DS}$ is equal to 0 V, the channel is not formed and the intrinsic effective capacitance is minimal. Under this biasing condition, the intrinsic effective capacitance is mostly determined by the gate capacitance to the source, drain and bulk silicon (C_{GD}, C_{GS} and C_{GB}, respectively). As $V_{G,DS}$ increases, electrons from the N^+ D//S implants recombine with the holes present in the P^+ well, creating a channel. When $V_{G,DS} = V_T$ the channel is fully formed and allows the current between D and S. However, in the implementation of an I-MOS diode, these terminals are connected together. Hence, a null current flow exists between those ports. On the other hand, the formation of the channel is key for the understanding of the capacitance variation shown in Figure II-7. As the transistor is driven into deeper inversion (i.e., $V_{G,DS} \gg V_T$) more free charges are concentrated in the channel, leading to a greater C_{eq}. Finally, for deep inversion, the number of free charges in the channel saturates. Hence, the equivalent capacitance of the I-MOS varactor, as for its A-MOS counterpart, reaches a maximum approximately equal to C_{ox}.

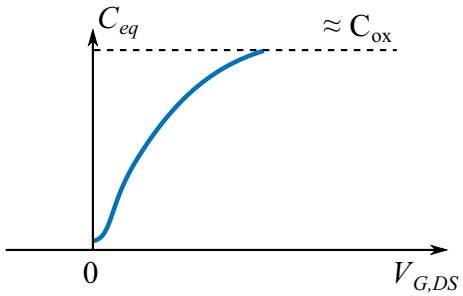

Figure II-7 Capacitance versus $V_{G,DS}$ of an n-MOS-based I-MOS varactor.

At RF frequencies, I-MOS varactors show similar performance as their A-MOS counterparts in terms of capacitance variation, overhead area and Q-factor [56], [58]–[60]. As a disadvantage, the sensitivity of I-MOS to the control voltage is greater than its A-MOS counterparts, especially to those integrated using the thick-oxide. This may lead to self-biasing issues (i.e., non-linearities) when a large signal is applied.

II.2.3. A-MOS versus I-MOS architectures

As discussed in the previous section, A-MOS and I-MOS varactors are operated similarly. In this section, a more in-depth discussion regarding their operation and behavior is carried out. In particular, two topics are discussed: (i) the biasing circuitry needed to drive these varactors and (ii) the Q-factor behavior vs frequency.

II.2.3.1. Biasing circuitry

For this comparison purposes, let us consider a thick-oxide A-MOS varactor and an I-MOS varactor. Figure II-8a and Figure II-8b show the required biasing/decoupling circuits needed to operate the I-MOS and A-MOS architectures, respectively. For the A-MOS varactor, the designer has to choose between integrating extra circuitry to generate negative V_{ctrl} voltages or designing two biasing networks, one for V_{ctrl} and one for V_{ref}, as depicted in Figure II-8b. Figure II-8c displays the

capacitance variation versus V_{ctrl}. Three cases were considered: (i) a thick-oxide A-MOS with $V_{ref} = V_{DD}$ applied to one of its ports, (ii) a thick-oxide A-MOS with $V_{ref} = 0$ (i.e., only the Biasing circuit,ctrl is required) and (iii) an I-MOS. Note that the I-MOS varactor could have been designed with a thick gate oxide. In that case, the conclusions in this section should be reconsidered.

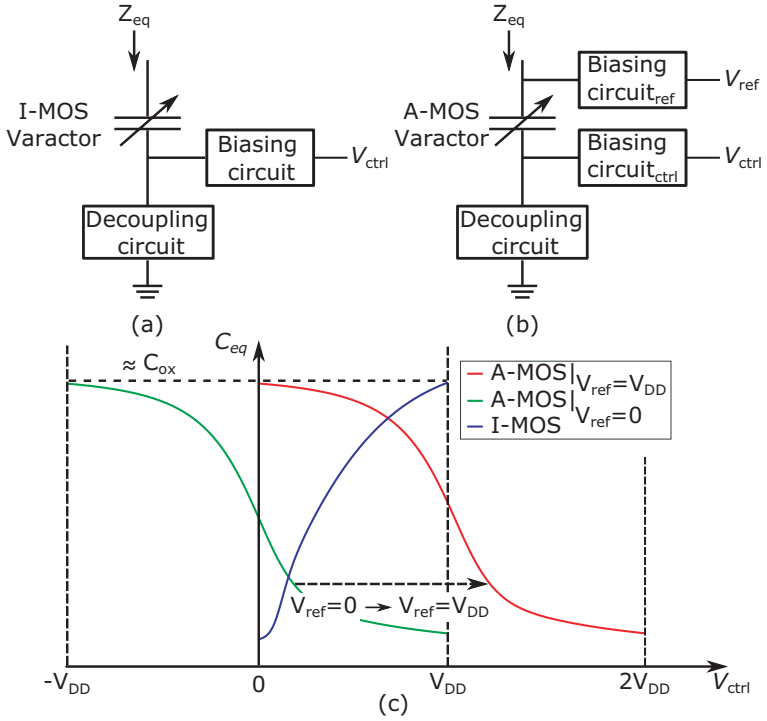

Figure II-8 (a) I-MOS varactor and the biasing/decoupling circuits needed for its operation. (b) A-MOS varactor and the biasing/decoupling circuits needed for its operation. (c) Capacitance versus V_{ctrl} for: (i) a thick-oxide A-MOS varactor with $V_{ref} = 0$ V (i.e., only Biasing Circuit,ctrl is necessary) (in Green), (ii) a thick-oxide A-MOS varactor with $V_{ref} = V_{DD}$ (in Red) and (iii) an I-MOS varactor (in Blue).

First, note that I-MOS and A-MOS varactors exhibit almost the same capacitance tuning ratio. For the I-MOS case, only one biasing circuit is required and the applied control voltage, V_{ctrl}, ranges from 0 to V_{DD}. For the A-MOS where $V_{ref} = V_{DD}$ is applied on one of the varactor's ports ($V_{DD}/2$ for the typical-oxide architecture), the other varactor port must be fed with positive V_{ctrl} voltages. Thus, in this case, the A-MOS needs two biasing circuits. Moreover, in the case of a thick-oxide A-MOS, extra circuitry has to be integrated to generate $2 \cdot V_{DD}$. For an A-MOS with $V_{ref} = 0$, only one biasing circuit is required. However, extra circuitry has to be integrated to generate on-chip negative V_{ctrl} voltages. In any case, these issues lead to a greater area overhead, consumption and even a decrease of the varactor performance when two biasing circuits have to be integrated. In addition, integrating devices with a thick oxide often requires additional steps during the manufacturing process. Contrarily, I-MOS varactors are based on classical MOS transistors.

II.2.3.2. Q-factor

As introduced earlier, the Q-factor is a metric that relates the effective reactance and the effective resistance of lumped elements. Generally, this metric is expressed as follows:

$$Q = \frac{|\Im(Z_{eq})|}{\Re(Z_{eq})} \tag{II-2}$$

where Z_{eq} stands for the equivalent impedance seen at the input of the DUT.

The Q-factor of lumped elements at mm-waves is critical due to its low value. This is especially true for capacitors. For instance, let us consider a lossy capacitance, which for the sake of simplicity,

can be modelled using a very simple series RC model. For such a device its Q-factor can be expressed as:

$$Q = \frac{1}{RC\omega}, \tag{II-3}$$

where ω is the angular frequency.

The Q-factor decreases with a $1/f$ slope. It is evident that this is a very simplistic approach, as integrated capacitors include parasitic inductive effects, coupling to the bulk silicon, skin effect… However, it serves as a very rough approximation to show why the Q-factor of capacitors is greatly impacted as the frequency increases.

In order to compare the performance of A-MOS and I-MOS varactors in terms of Q-factor vs frequency, let us consider a practical example with an A-MOS and an I-MOS designed and simulated using the PSP compact models in the STM BiCMOS 55-nm technology Process Design Kit (PDK). For a fair comparison, same capacitance tuning ratio (C_{max}/C_{min}) equal to 4.5 and same C_{min} were considered for both devices at 200 GHz. This was achieved using an A-MOS varactor with two fingers and a total length and width of 531 nm and 3.33 μm, respectively. In order to match the capacitance variation of the A-MOS, the I-MOS was also designed with two fingers and a total length and width of 1.6 μm and 7.47 μm, respectively. Note that the required area for the I-MOS is greater than for the A-MOS. However, this tends to be negligible regarding the size of the circuits in which these devices are integrated. For the sake of simplicity, ideal elements to perform biasing functions were considered to focus on the intrinsic capabilities of the varactors. Figure II-9 shows a schematic-level simulation of the effective capacitance of these varactors at 50, 100, 150, 200, and 250 GHz, calculated as in (II-1).

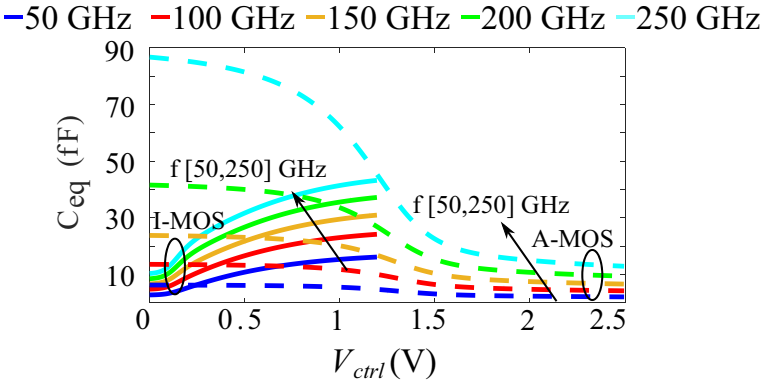

Figure II-9 Equivalent capacitance of the considered A-MOS and I-MOS varactors in the STM 55-nm BiCMOS technology at 50, 100, 150, 200, and 250 GHz.

Note that, even if both capacitances were set to an equal magnitude at 200 GHz, both varactors present different boundary values at the rest of considered frequencies. This can be easily explained by the fact that neither the geometry or the nature of these varactors is the same. Hence, nor is the nature and magnitude of their parasitics. In this scenario, the frequency dispersion suffered by each device is different too.

On the other hand, Figure II-10 shows a schematic-level simulation of the Q-factor, calculated as in (II-2), of these varactors for the same range of frequencies.

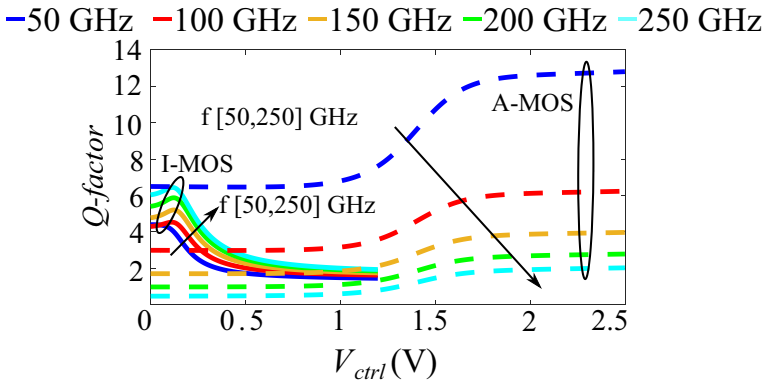

Figure II-10 Q-factor of the considered A-MOS and I-MOS varactors in the STM 55-nm BiCMOS technology at 50, 100, 150, 200, and 250 GHz.

In Figure II-10, the Q-factor of the I-MOS varactor slightly increases with frequency while it decreases for the A-MOS varactor. Both devices have the same Q-factor around 120 GHz. This particular frequency only makes sense for the considered geometries and technology, but it has the interest to provide an order of magnitude. Note that, for the higher-end of the mm-wave band the reported simulations are frequency-extrapolated since the PDK is not fully mature at these high frequencies. It is evident that the A-MOS varactor is a better design option below about 50 GHz. On the other hand, above 150 GHz the I-MOS clearly exhibits a superior performance. Between these two frequencies, other factors (e.g. model maturity, area overhead, biasing circuitry…) than the Q-factor only should be considered to achieve a fair comparison.

The conclusion carried out from Figure II-9 and Figure II-10 is clear for frequencies below 50 GHz and above 150 GHz. However, it is difficult to compare one frequency to another due to the fact that different Q-factor and capacitance ratio are observed. For this reason, we propose to use the following Figure-of-Merit (FoM):

$$FoM = Q \cdot \left(\frac{C_{max}}{C_{min}}\right). \tag{II-4}$$

This metric allows evaluating the well-known trade-off between capacitance variation and Q-factor of a varactor. Figure II-11 shows the FoM obtained for the considered I-MOS and A-MOS at 50, 100, 150, 200 and 250 GHz, respectively. This FoM shows that, for a given capacitance ratio, above around 150 GHz the FoM of the I-MOS varactor is better than the A-MOS one as expected from Figure II-10.

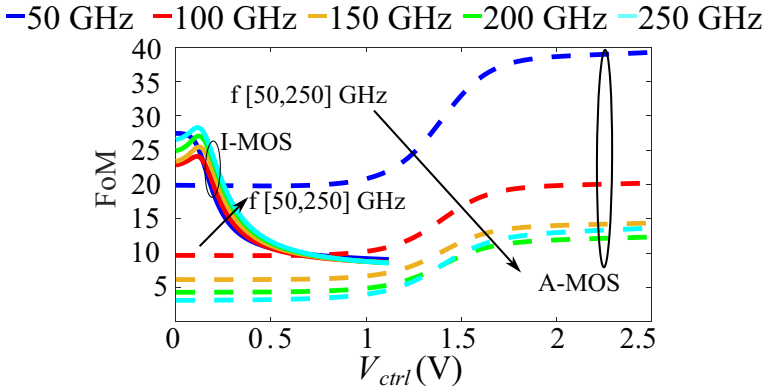

Figure II-11 FoM of the considered A-MOS and I-MOS varactors in the STM 55-nm BiCMOS technology at 50, 100, 150, 200, and 250 GHz.

The conclusions drawn in this section are largely technology dependent. However, a main tendency is noticed when comparing A-MOS and I-MOS varactors: thin-oxide I-MOS varactors need simpler biasing circuitry and show a *stable* Q-factor over frequency. On the other hand, A-MOS varactors tend to have a Q-factor decreasing with frequency.

II.2.4. State-of-the-art silicon-based mm-Wave varactors

Here, the conclusions carried out in the previous section are put into perspective. For this purpose, the most recent silicon-based mm-Wave varactors are presented in Table II-I.

TABLE II-I STATE-OF-THE-ART SILICON-BASED MM-WAVE VARACTORS

Reference	Technology	Topology	Frequency (GHz)	Q-factor	C_{max}/C_{min}	FoM
[57]	28-nm FDSOI	A-MOS	100	10	1.4	14
[61]	130-nm CMOS	A-MOS	60	9	2	18
[62]	130-nm CMOS	A-MOS	50	5	2	10
[63]	130-nm CMOS	A-MOS	24	100†	1.6	160

† Q-factor at silicon-level (i.e., without interconnections to the BEOL).

In [57], authors propose a classical thick-oxide A-MOS varactor in the hybrid region (standard bulk silicon) of the STM 28-nm FDSOI technology. In addition, authors propose a physics-based small signal model. The particularity of this work, in comparison to the rest of considered articles in Table II-I, is that it presents the measurements up to the highest frequencies.

The work in [61] presents an *island-gate* varactor thick-oxide A-MOS varactor. *Island-gate* transistors (varactors) are devices that are built in a concentric shape (i.e., the source is completely surrounded by the gate, which in its turn, is surrounded by the drain). Their work was subsequently extended in [62], where a more detailed analysis of this structure is provided. Using this topology, the authors report the greatest tuning range among the considered mm-wave varactors. Note that a significant drop in the Q-factor is observed in the work presented in [62] as compared to [61]. The former work aims at accurately characterizing the varactor and its working principle while the latter targets the design of a high Q-factor varactor. Nevertheless, these works present varactors with Q-factors of 5 and 9 at moderate mm-wave frequencies (i.e., 50 and 60 GHz), respectively.

Finally, [63] provides the measurement and design of a thick-oxide A-MOS varactor. Even though the provided results are not strictly in the mm-wave band, they are close enough to be considered. Note that this work reports a strikingly high Q-factor. This can be easily explained thanks to the fact that no interconnection to the BEOL is considered. In the article, authors proposed a very simple small-signal model. Then, the intrinsic Q-factor is reported for what they claim to be intrinsic device. Hence, a much lower Q-factor can be expected when considering a varactor connected to the BEOL of the technology.

Note that all the papers considered in Table II-I present thick-oxide A-MOS varactors. In all these works, the frequency-decreasing Q-factor reported in section II.2.3.2 is observed. However, as introduced in section, I-MOS varactors become interesting at higher frequencies. The lack of interest in the I-MOS topologies can probably be explained by the fact that mm-wave applications on silicon technologies is a relatively recent subject of study. In addition, I-MOS varactors only become important at the upper-end of the mm-wave band, where applications are still rare. Hence, A-MOS varactors are more suited for most of the applications reported in the literature. Nevertheless, given the results observed in II.2.3 it is worth to explore the capabilities of varactors based on MOSFETS operating in an inversion regime at mm-wave frequencies.

In the next section, two topologies for the implementation of n-MOS-based I-MOS varactors are studied: (i) a conventional I-MOS topology, as presented in II.2.2, and (ii) nMOS transistor in a common-source configuration.

II.2.5. I-MOS implementations

II.2.5.1. Classical I-MOS

In order to verify the tendencies observed in the previous section, a classical I-MOS varactor was designed and characterized. The considered varactor architecture is shown in Figure II-12.

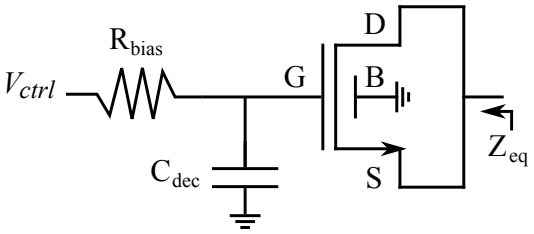

Figure II-12 Classical I-MOS considered architecture.

The proposed classical I-MOS varactor requires a biasing circuit to apply a DC voltage to its gate. The biasing circuitry must allow to tune the varactor without, ideally, interfering with the RF signal. This circuit is composed by a resistor and a capacitance, R_{bias} and C_{dec}, respectively. Since the varactor is voltage-controlled through the gate, the DC biasing can be implemented with a high-value resistor R_{bias}, which presents a high impedance to RF signals. Other architectures to apply V_{ctrl}, such as inductors or quarter-wave length transmission lines could be used. However, a resistor presents the best solution for wide-band operation and low area overhead, which is the goal in this Chapter as wideband characterization is performed. In addition, a high-value capacitance, C_{dec}, is used for decoupling purposes. However, it is worth mentioning that in a practical implementation, where most of the applications aim at narrower frequency bands than the ones explored hereby, a narrow-band biasing circuit using non-resistive elements would likely report better results. The proposed I-MOS varactor uses a traditional n-MOSFET, and the control voltage varies from 0 V to V_{DD}. Note that, due to the high operating frequencies, the capacitance and resistor composing the biasing circuit cannot be treated as ideal elements. These devices include parasitic effects that are non-negligible at mm-waves. In this case study, the effects of the biasing circuit itself within the varactor model were included.

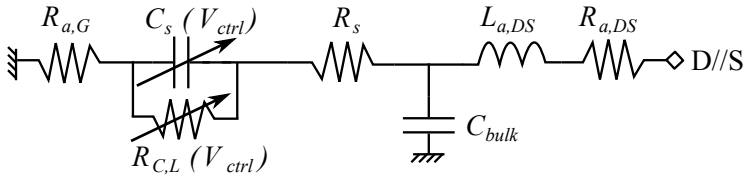

Figure II-13 Proposed small-signal model for the classical I-MOS varactor.

A simple circuit model, depicted in Figure II-13, was developed to describe the behavior of the proposed device. The model is composed of a resistance $R_{a,DS}$ and an inductance $L_{a,DS}$ at drain/source level, corresponding to the resistance and inductance of the access from the top metal layer to the active region, respectively. C_{bulk} models the electrical coupling from the access interconnections and drain/source implants to the bulk silicon. R_s models the resistance of the contact and N^+ implants (i.e., drain and source). $R_{C,L}$ models the leakage, as well as the resistance of the channel. C_s models the capacitive coupling between the channel, drain and source to the gate of the MOSFET. Finally, $R_{a,G}$ models the resistance at gate level together with the parasitic resistance of the decoupling capacitance, C_{dec}. Note that the ohmic losses and parasitic capacitance occurring in the biasing circuit are embedded into $R_{a,G}$ and C_s. For the sake of simplicity but also to achieve a physics-based model, only C_s and $R_{C,L}$ depend on the tuning voltage V_{ctrl}.

a) Measurement Results

For a proof of concept, an I-MOS varactor with a large tuning ratio C_{max}/C_{min} was designed, C_{max} and C_{min} being calculated as in (1), for the two extreme biasing voltages. As the standard

impedance of RF circuits in typical applications is 50 Ω, a varactor is efficient in a circuit when its equivalent impedance is not too far from -j·50 Ω. Hence the size of the varactor was chosen so that C_{max} and C_{min} surround -j·50 Ω impedance at a working frequency of 190 GHz, i.e., $\frac{1}{C_{min}\cdot\omega} > 50\ \Omega > \frac{1}{C_{max}\cdot\omega}$.

Finally, the I-MOS varactor was designed to obtain a capacitance ratio of 4.4 along with C_{min} equal to 8 fF, leading to $\frac{1}{C_{min}\cdot\omega} = 105\ \Omega$ and $\frac{1}{C_{max}\cdot\omega} = 24\ \Omega$, at 190 GHz. The layout was optimized to maintain the greatest Q-factor while minimally reducing the tuning range. After a post-layout simulation, the transistor showed a C_{min} of 13 fF and a reduction of the tuning ratio to 3.2, due to parasitic capacitances. These values were obtained with a standard nMOS transistor with a width of 7.47 μm, a length of 1.6 μm and two fingers. Note that, the gate length of the designed I-MOS varactor makes it suitable for larger technology nodes. A high-resistivity polysilicon resistor was considered to achieve a DC-resistor R_{bias} equal to 90 kΩ. This value was achieved using two 180 kΩ resistors connected in a parallel configuration. Thanks to the high-resistivity polysilicon layer embedded in this technology, such high values could be achieved with resistors with a width and length of 0.9 μm and 27 μm, respectively. The decoupling capacitance C_{dec} was implemented using two Metal-Oxide-Metal (MOM) capacitors, connected in a parallel configuration, to achieve a value of 200 fF. These capacitances represent an areaof 81 μm^2 each. They exhibit a -j4.1 Ω impedance at 190 GHz, which is a compromise between a quasi-short circuit and moderate area overhead. Larger capacitances would lead to a better ground connection for the RF signal. However, due to their larger size, the magnitude of their parasitics would also be larger, possibly masking the performance of the proposed I-MOS with self-resonances appearing at lower frequencies.

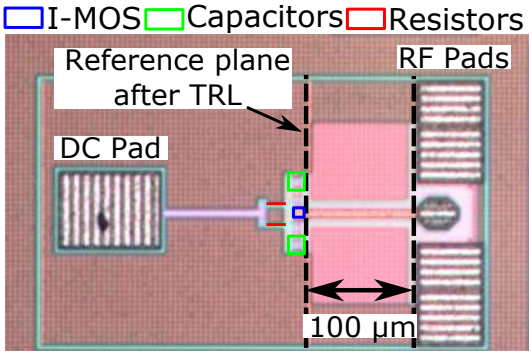

Figure II-14 Micrograph of the fabricated classical I-MOS.

The proposed device was measured using three different Vector Network Analyzers (VNAs): (i) an Anritsu VectorStar ME7838A4, from 1 GHz to 140 GHz, (ii) an Oleson extender associated to a R&S VNA, from 140 to 220 GHz, and (iii) a R&S extender associated to a R&S VNA from 220 to 325 GHz. An on-wafer Thru-Reflect-Line (TRL) calibration [43] was performed to eliminate the effect of the pads and the 100-μm microstrip feeding lines. A micrograph of the fabricated circuit is shown in Figure II-14 together with the reference planes after the TRL calibration. On the other hand, Figure II-15 shows a 3D view of the considered I-MOS.

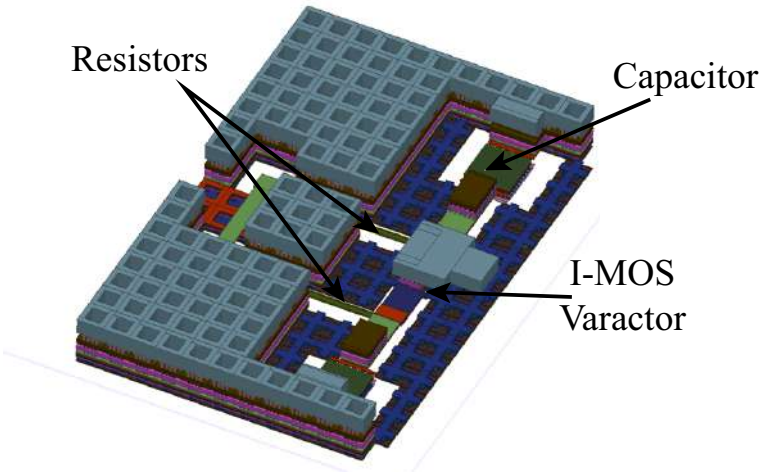

Figure II-15 3D layout view of the fabricated classical I-MOS and the decoupling circuitry.

Due to the wide frequency band considered in this work, two 50-Ω Line standards of different lengths, Line_1 and Line_2, respectively, were integrated on-wafer. Line_1 and Line_2 were designed using a microstrip line. Their extra lengths (as compared to the Thru standard) were set to 350 μm and 170 μm, respectively. Line_1 was used to perform the calibration from 1 GHz to 140 GHz whereas Line_2 was used for the 140 GHz to 325 GHz band. Line_1 exhibits an extra electrical length of 0.8° at 1 GHz and 109° at 140 GHz. On the other hand, Line_2 exhibits an extra electrical length of 53° at 140 GHz and 123° at 325 GHz. Note that, while the extra electrical length of Line_2 provides with enough margin to ensure proper reading of the Line's characteristic impedance, this is not applicable for the Line_1. Below 1 GHz, Line_1 has an electrical length that is close to the sensitivity of the used VNA, which is around 0.06 °, and the measurements close to this frequency were certainly affected by a non-ideal calibration. Nevertheless, the two-Line approach ensures almost complete coverage throughout the measured frequency band.

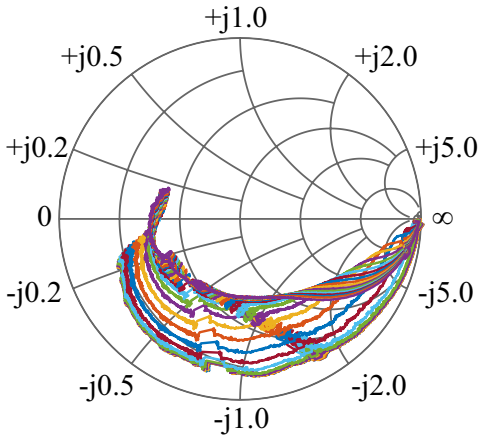

Figure II-16 Measured S_{11} in the 1-325 GHz band as a function of V_{ctrl}.

Figure II-16 presents a Smith's chart of S_{11} after TRL calibration. It displays 25 traces corresponding to the V_{ctrl} tuning voltage in steps of 50 mV, from 0 to 1.2 V. At 190 GHz, S_{11} magnitude varies from -1.2 dB to -6.9 dB and its phase varies from -80° to -144°, respectively.

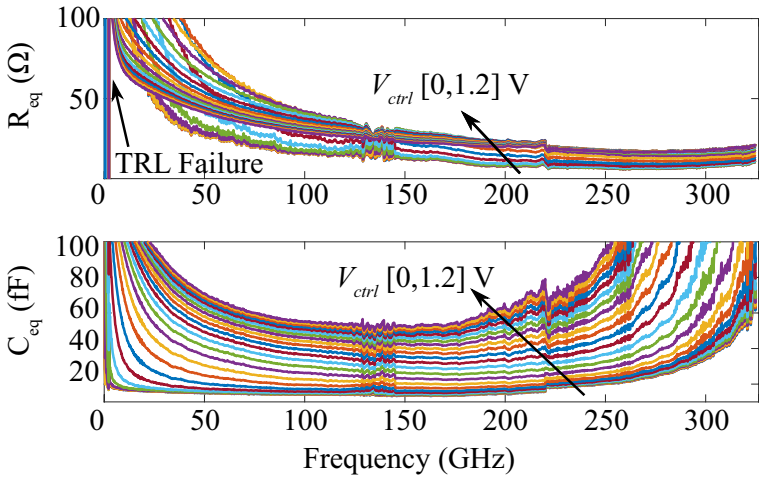

Figure II-17 Measured R_{eq} and C_{eq} in the 1-325 GHz band as a function of V_{ctrl}.

Figure II-17 displays the series equivalent capacitance and resistance, C_{eq} and R_{eq}, throughout the 1 GHz to 325 GHz frequency band for a V_{ctrl} step of 50 mV. The equivalent series capacitance was calculated as in (1). On the other hand, the equivalent series resistance reduces to $R_{eq} = \Re(Z_{eq})$. Around 1 GHz, the vertical traces on R_{eq} indicate that the TRL is no longer valid since the sensitivity becomes really poor. Note that beyond 250 GHz, C_{eq} shows a dispersive behavior. This is due to the fact that (1) is a calculation of the equivalent capacitance. Hence, when using this equation near resonances, the equivalent capacitance tends to the infinity, since $\Im(Z_{eq}) \to 0$.

At 190 GHz, the measured varactor presents an overall equivalent capacitance varying from 13 fF to 54 fF. The average slope is equal to 26 aF/mV, presenting low sensitivity to the biasing voltage variations, since C_s has a low sensitivity to the tuning range, as it will be shown at the end of this section. This is interesting for practical applications.

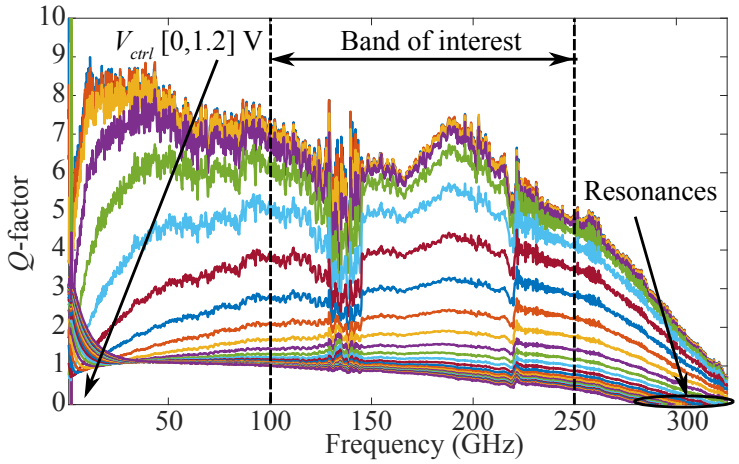

Figure II-18 Measured Q-factor in the 1-325 GHz band as a function of V_{ctrl}.

Figure II-18 shows the extracted Q-factor for different values of V_{ctrl} in the 1 GHz to 325 GHz frequency band. The Q-factor is relatively flat throughout the 140-220 GHz band, reaching a maximum value of 7 around 190 GHz. Above 190 GHz, the Q-factor decreases, and resonances appear beyond 290 GHz, thus the extraction of C_{eq} above the resonance frequency would lead to negative values. Below 190 GHz, the effect of the relatively-low quality factor of C_{dec} in series with the I-MOS varactor limits the increase of its Q-factor. This can be easily explained by the degradation of the MOM capacitor quality factor at mm-wave frequencies. For instance, at 140 GHz, the measured quality factor of a MOM capacitor in this technology is around 10 [64]. Thus, it can be expected a quality factor around 20 at 70 GHz. At 70 GHz, the maximum measured Q-factor of the varactor is around 8, which means that the intrinsic varactor's Q-factor, disregarding the MOM capacitance, is around 14. On the other hand, for

frequencies below 50 GHz, the low Q-factor shown in Figure II-18 can only be explained by a low value of the intrinsic varactor's Q-factor, since the quality factor of C_{dec} is much higher.

b) Empirical model

In order to integrate the developed varactor into a conventional design flow, an empirical model was developed by fitting the small signal model proposed in Figure II-13 to the measurement results. The varactor presents an $R_{a,DS}$ and $L_{a,DS}$ of 0.5 Ω and 7.5 pH, respectively. R_s is equal to 12 Ω. C_{bulk} and $R_{a,G}$ are equal to 6 fF and 8 Ω, respectively.

The variation of $R_{C,L}$ and C_S as a function of the control voltage V_{ctrl} was modeled by empirically fitting the measurements using standard regression functions. $R_{C,L}$ was coded using a 4^{th}-order Gaussian and C_s was coded using a 3^{rd}-order Fourier's series.

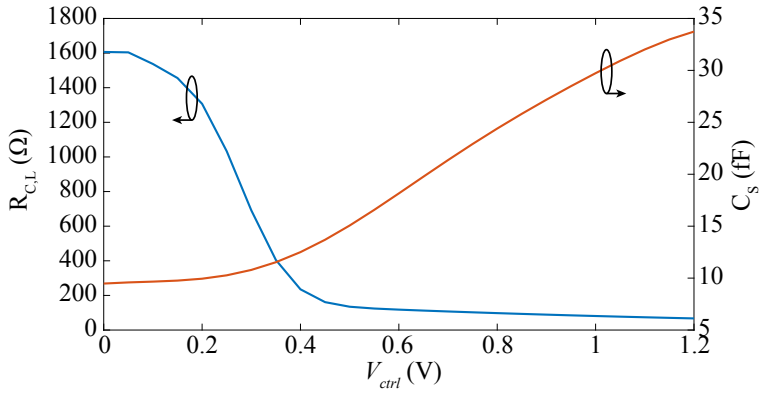

Figure II-19 Modeled variation of $R_{C,L}$ and C_s versus V_{ctrl}.

The modeled variation of $R_{C,L}$ and C_s versus V_{ctrl} is plotted in Figure II-19. $R_{C,L}$ ranges between 1.6 kΩ and 67 Ω, and C_s ranges from 9 to 34 fF. The behavior of these parameters is consistent with the expected electrical response of the structure. When the V_{ctrl} is low, the channel is not formed and only the losses from leakage currents are present, thus leading to a high-value resistor and a low-value capacitance. As the V_{ctrl} increases, the channel begins to form, thus increasing the capacitance between drain/source and gate. The formation of the channel with the increase of V_{ctrl} leads to a decrease of $R_{C,L}$, thus increasing the losses.

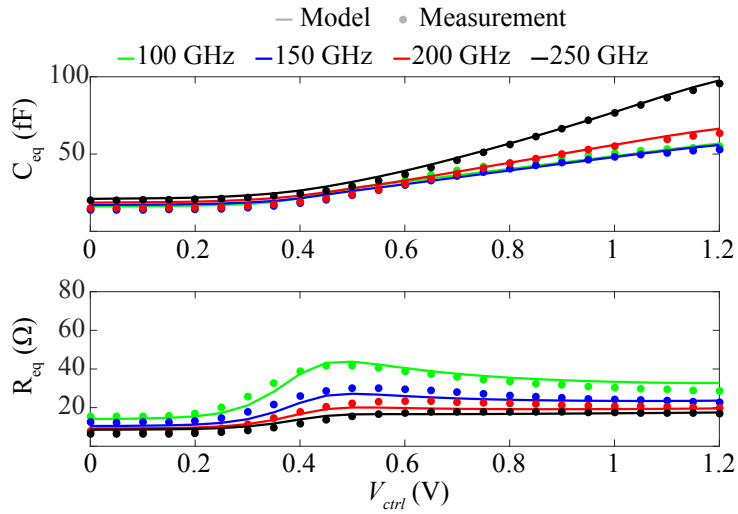

Figure II-20 Measured and modeled C_{eq} and R_{eq} variation at 60, 100, 150, 200, and 250 GHz as a function of V_{ctrl}.

In Figure II-20, the values of R_{eq} and C_{eq} extracted from measurements are compared to the electrical model proposed in Figure II-13 for working frequencies equal to 100, 150, 200 and 250 GHz, respectively. A good agreement between measurement results and model is observed for frequencies above 100 GHz. Below this frequency, the model shows some disagreement for the estimation of R_{eq}. This can be easily explained as none of the model elements include frequency dependent behaviors. Hence, frequency-dependent effects such as the skin effect or the Non-Quasi-Static (NQS) effect, which were present when the model parameters were optimized between 100 GHz and 250 GHz, will overestimate e.g. the losses at lower frequencies. However, developing a small-signal model the between 1 to 325 GHz is out of scope for this manuscript.

c) Discussion on the NQS effects on C_S

NQS (Non-Quasi Static) effects appear when the channel of a transistor can no longer be considered as a lumped-element (i.e., its length is not negligible as compared to the guided wavelength). The presented I-MOS varactor, with a gate length of 1.6 µm, certainly suffers from NQS effects as it was characterized beyond its f_{max}. Even though the analytical calculation of the magnitude of these effects is out of the scope of this manuscript, a discussion can be open.

For frequencies well below f_{max}, where the NQS effect can be neglected, the channel can be modelled as an RC network. At these frequencies, with the increase of the channel length (L), R_{eq} and $C_{eq,max}$ increase due to the increased resistivity and effective surface of the channel, respectively. On the other hand, $C_{eq,min}$ only slightly varies with the increase of the channel, given that this value is practically fixed by the gate-drain, gate-source and gate-bulk capacitance. Hence, the tuning range of C_{eq} is increased with the increase of L due to the fact that the channel formation is spread over a long channel, allowing a great modulation of this equivalent capacitance.

In the model given in Figure II-13, this phenomenon leads to an increase in the maximum value of C_s (i.e., in its tuning range) and a decrease of $R_{C,L}$, as it is placed in a parallel configuration to C_s. Overall, this leads to a decrease of the Q-factor of the I-MOS varactor.

On the other hand, the frequency dependence of the gate capacitance (i.e., which partly constitutes C_S) is a subject that has been discussed in the literature [65]. Analytical and experimental data show a decrease of the maximum value of this capacitance with frequency, when NQS effects are accounted for. This translates into a reduction of $C_{s,max}$ in our model as frequency increases.

However, in [65], authors point out that bulk and gate resistance play a major role in the frequency behavior of C_s. This is due to charge inertia and gate resistance effects. The reader may note that this is a very technologically dependent parameter (e.g. shape of the transistor, nature and concentration of the dopant species, design rules for interconnections…). Hence, it is difficult to provide valuable Q-factor and C_{eq} guidelines for the reader as a function of L in any given technology.

II.2.5.2. Common-source nMOS varactor

In order to further investigate the behavior of MOSFETs in an inversion regime as a varactor topology, a second device was designed: an n-type MOSFET in a common-source configuration. This device was characterized in the 1 GHz to 145 GHz frequency band, allowing its use for the design of mm-wave phase shifters with working frequencies beyond 100 GHz. Let us call this topology Common-Source MOS varactor (CS-MOS). nMOS transistors in such a configuration are widely used in many RF functions (e.g., amplification, switching…). In most of these applications, the capacitance of transistors is seen as an undesired parasitic.

As introduced earlier in this chapter, MOSFETs rely on capacitive effects for their operation. For instance, Figure II-21 displays the main capacitances found in a long-channel MOSFET, when source-drain capacitance, C_{DS}, is neglected, which can only be considered in devices featuring a long channel. Hence, for modern technology nodes, this capacitance must be considered. However, the aim of Figure II-21 is merely illustrative.

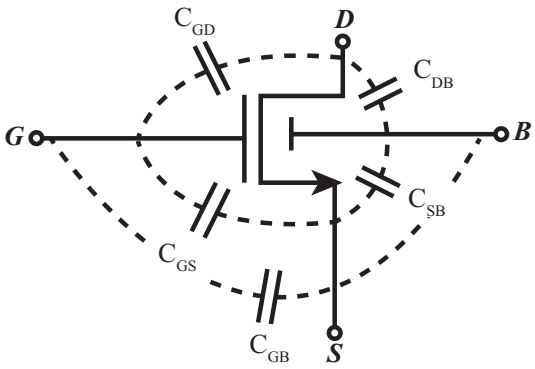

Figure II-21 Main capacitances in a long-channel MOSFET.

In most of the systems including MOSFETs, the designer aims to reduce the magnitude of these capacitances by optimizing the circuit layout. However, this is only an issue when aiming to use the transistor in a classical manner (e.g., for amplification or switching purposes).

It is the opposite when the device is analyzed using a varactor approach. Capacitances shown in Figure II-21 are a function of the transistor geometry and its biasing conditions; hence the device can lead to interesting varactors.

a) Geometry optimization

Modern multi-finger transistors present geometries that are mostly defined by three parameters: (i) total width (W), (ii) length (L), and (iii) number of fingers (N_f). While N_f is very helpful for transistor and layout optimization, W and L are the parameters that mostly dictate the overall transistor behavior. Hence, these two parameters should be considered first for the varactor design.

As introduced above, the values of the capacitances depicted in Figure II-22 are defined by the geometry of the transistor and its biasing conditions. The geometry (W, L, number of contacts on the gate, shape of the access…) of the transistor defines the fixed part (i.e., minimal magnitude of the capacitance) of the capacitances while the biasing conditions define the variable part of these capacitances. The variation of these capacitances, when the transistor is driven in an inversion-mode, can mainly be attributed to the channel formation, similarly to the behavior of the I-MOS described in section II.2.2.

Here, the goal is to investigate topologies leading to a high tuning ratio. To carry out a simple analysis, let us consider a one-finger n-MOS transistor, as depicted in Figure II-22.

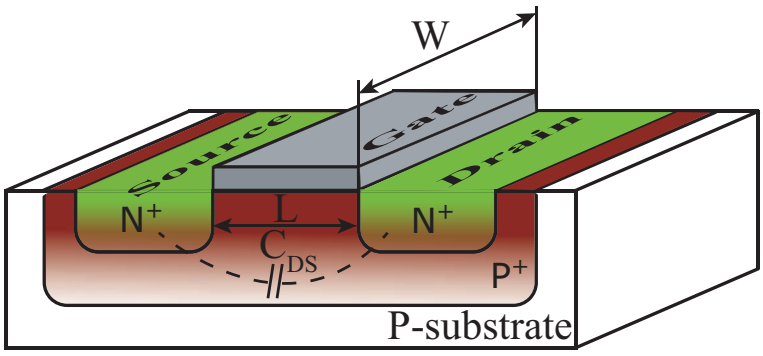

Figure II-22 3D view of an n-MOS transistor.

In such a device, as L reduces, C_{DS} increases. For short-channel transistors (i.e., L in the order of some nanometers), C_{DS} can no longer be neglected as it becomes of the same order of magnitude as the other capacitances depicted in Figure II-21. However, note that C_{DS} is placed in a parallel configuration to the transistor channel, which is the source of the main capacitance variation. Hence, to achieve a maximum variation C_{DS} has to be reduced.

The exact expression of this capacitance is geometry dependent and becomes extremely complicated for multi-finger topologies. However, if Figure II-22 is considered, a simple proportionality relationship can be defined as:

$$C_{DS} \propto \frac{W}{L} \tag{II-5}$$

Hence, in order to reduce C_{DS}, and thus increase the varactor tunability, the W/L ratio has to be reduced. On the other hand, the channel resistance is inversely proportional to the W/L ratio. This leads to a trade-off between the tuning ratio and the Q-factor of these devices.

b) Proposed architecture

Considering the conclusions carried out in the previous section, it was decided to explore the capabilities of nMOS transistors to perform as transistors when placed in a common-source configuration. This is the first time that such topology is reported in the literature for the design of on-silicon mm-wave varactors.

Again, the STM 55-nm BiCMOS technology was considered for the design. The gate length of the transistor was set to 9 µm while W and N_f were optimized to improve the Q-factor while maintaining a tuning ratio (C_{max}/C_{min}) above 7. An L of 9 µm was chosen as it is the maximum gate length that is characterized in the considered technology.

Under these conditions, the optimization process led to a transistor with an N_f of 2 and a total W of 15.3 µm. In multi-finger technologies, even values of N_f lead to an unequal number of drains and sources. For instance, the considered N_f led to a transistor with two drains and one source. Figure II-23 shows the schematic view of the designed CS-MOS. Note that a large resistor R_b was placed at gate level for biasing purposes. As the CS-MOS is voltage-driven, the resistor is only necessary to present an open-circuit for the RF signal at gate level. The resistor was designed using the high-resistivity polysilicon layer present in the considered technology with a width and length of 0.9 and 27 µm, respectively. This geometry led to an R_b with a resistance of 180 kΩ. Note that this biasing architecture is not suitable for noise-sensitive systems. Again, this architecture presents the advantage of allowing wideband characterization or its implementation in wideband systems. However, for narrow-band systems or applications, a biasing network constituted by reactive elements (

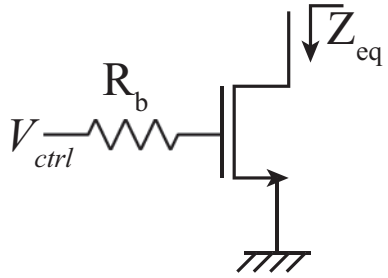

Figure II-23 Schematic view of the designed CS-MOS.

The transistor was designed using the geometry described above and the layout was optimized so that the interconnections present minimal parasitic capacitances. The optimization of the layout was done by means of the so-called RLCK parasitic extractions. RLCK extractions account for the resistance (R), inductance (L), capacitance (C) and mutual inductance (K) present in the circuit interconnections. Simulations were carried out with a DC voltage at drain-level (V_D) of 0 V and a biasing voltage, V_{ctrl}, between 0 and 1.2 V. Figure II-24 shows the post-layout simulation of R_{eq} as a function of V_{ctrl} in the 1-145 GHz band, where $R_{eq} = \Re(Z_{eq})$. Note that, at a given frequency, R_{eq} is inversely related to V_{ctrl}. This is an expectable result as the main contributor to the value of R_{eq} is the channel resistivity. As V_{ctrl} increases, the channel is formed, thus reducing its resistivity. At 100 GHz, R_{eq} presents a value between 5 and 7 Ω.

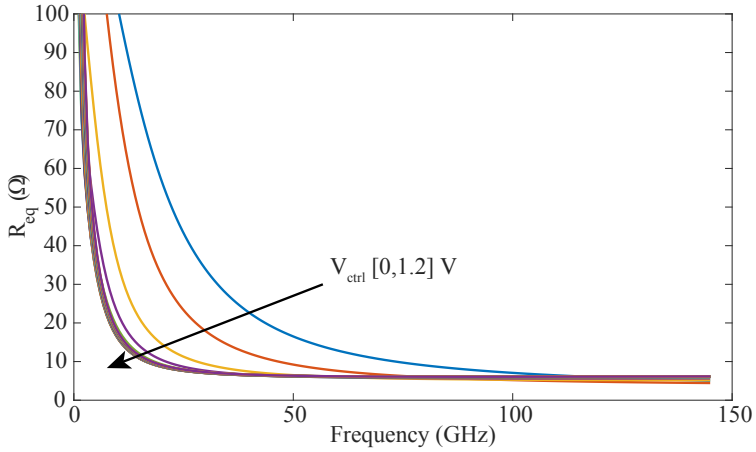

Figure II-24 Simulated R_{eq} as a function of V_{ctrl} for the CS-MOS architecture.

Next, Figure II-25 displays the magnitude of C_{eq}, calculated as in (II-1), as a function of V_{ctrl} in the 1-145 GHz frequency band. As expected, this magnitude has a direct relationship with V_{ctrl}. As introduced before, this magnitude is mostly modulated by the channel formation. Hence, the value of C_{eq} increases with V_{ctrl}. At 100 GHz, the value of C_{eq} is comprised between 26 and 200 fF, leading to a tuning ratio of 7.7.

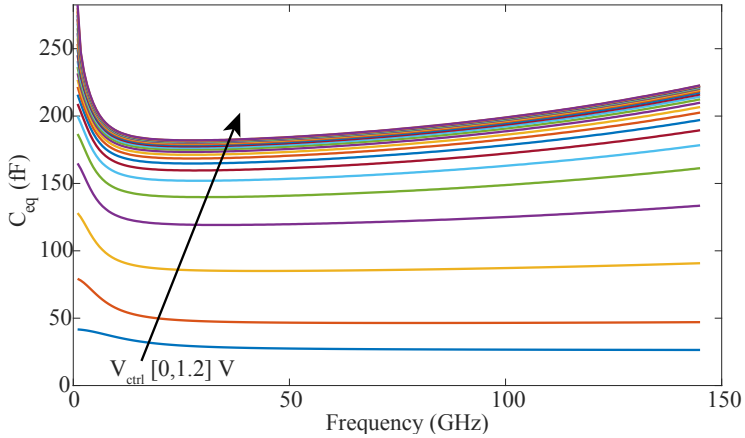

Figure II-25 Simulated C_{eq} as a function of V_{ctrl} for the CS-MOS architecture.

Finally, the Q-factor of the considered structure is plotted in Figure II-26. At 100 GHz, the considered CS-MOS presents a Q-factor between 1 and 8. While being true that the minimum Q-factor is quite reduced, note that on-silicon varactors with such a capacitance variation have never been reported in the literature. Hence, this architecture could open the door to innovative approaches for wide tuning-range applications.

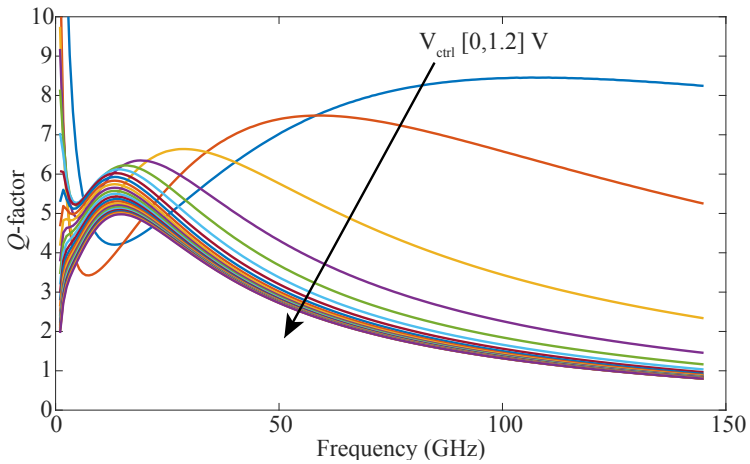

Figure II-26 Simulated Q-factor as a function of V_{ctrl} for the CS-MOS architecture.

c) Discussion on the model validity

As introduced previously, in RF transistors are mostly used for amplification or switching purposes. In these designs, the designer avoids transistors with large intrinsic capacitances as they shunt the transistor, reducing their f_T and f_{max}. However, these capacitances are present and must be considered. For this reason, foundries with advanced technological nodes integrate high-frequency effects (e.g., NQS effect) in their Process Design Kit (PDK) to help the designers to better account for these effects when designing close to the transistor limits.

Note that here, the transistor length was set to 10 µm, leading to a sub-GHz f_{max}. Hence, the working frequency of the CS-MOS is largely beyond this value. The validity of the models is quite limited in this mode of operation, as the models were not designed for transistors operating in these conditions (i.e., beyond f_{max}).

d) Measurement Results

The designed CS-MOS varactor was measured in the 1-145 GHz band using an Anritsu VectorStar ME7838A4 VNA. A first-tier LRRM [42] calibration was performed on a commercial Impedance Standard Substrate (ISS) setting the reference plane at the probe tips. Then, a subsequent second-tier TRL calibration [43] was performed, setting the reference plane at the input of the CS-MOS. Figure II-27 shows the micrograph of the fabricated device together with the reference plane after the TRL calibration.

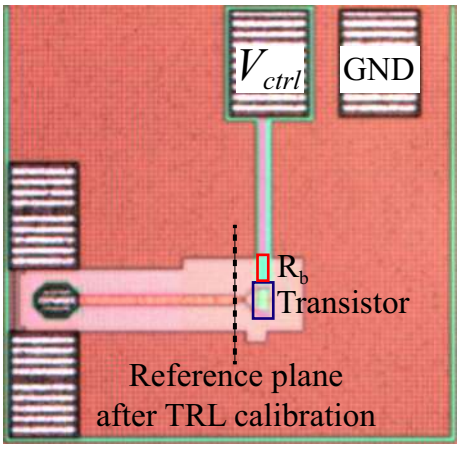

Figure II-27 Micrograph of the fabricated varactor.

The TRL calibration was performed using a 50-Ω Line standard presenting an offset length of 350 µm, as compared to the Thru standard. Hence, at 1 GHz and 145 GHz, the electrical length difference between these two standards is around 1º and 120º, respectively. Note that the quality of the TRL calibration below 10 GHz (i.e., where the difference between the electrical length of the Line and Thru standards is below 10º) might be poor. However, a good-quality calibration can be expected for the rest of the frequency spectrum.

Note that in the considered architecture, by means of V_{ctrl} and a DC voltage applied to the transistor drain, V_D, the transistor can be biased either in the so-called *cut-off, triode* or *saturation* regions. Hence, the behavior of the CS-MOS was also explored in these regions. In the measurement setup, the voltage V_D was applied using the bias-tee integrated in the VNA. Figure II-28 presents the measured S_{11} as a function of V_{ctrl} and $V_{DS} = V_D$ at 25, 50, 75, 100 and 125 GHz.

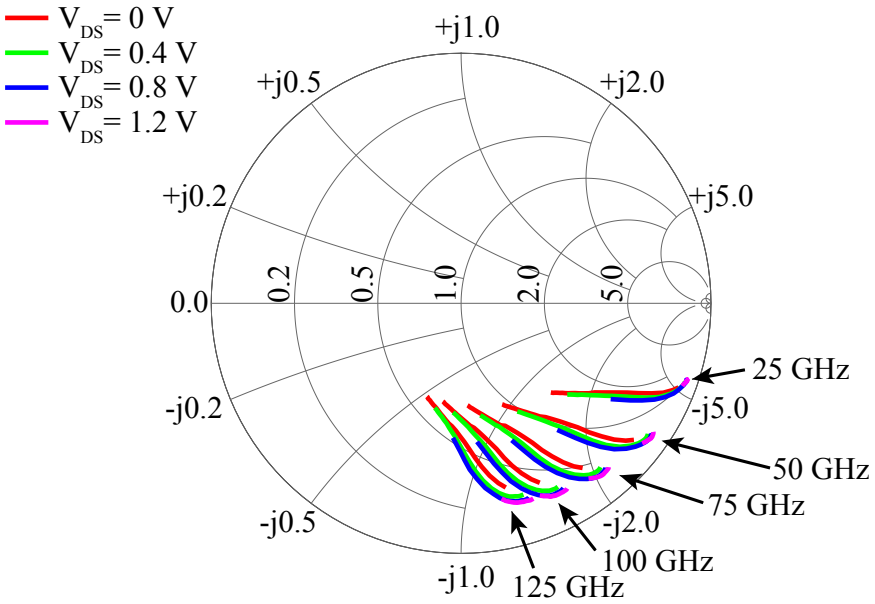

Figure II-28 Measured S_{11} as a function of V_{ctrl} and V_{DS} at 25, 50, 75, 100, and 125 GHz.

Note that when V_{DS} increases, the tuning range is reduced. This is due to the fact that when this voltage increases, the range of gate voltages (V_{ctrl}) for which the transistor operates in the saturation region is also increased. As compared to the I-MOS varactor presented above, which could only operate in the *cut-off* and *triode* regions, this transistor can be drive in the *saturation* region. When the transistor is driven in *saturation*, the channel is no longer homogeneous beneath the gate. As V_{DS} increases, the channel is deformed, thus resulting in a pinch-off effect [66]. In this scenario, the charge carriers concentrate in the drain terminal, as it presents a greater voltage. Hence, the gate to channel capacitance is mostly concentrated near the drain terminal. As V_{DS} further increases, the pinch-off effect is further enhanced, thus reducing the effective surface of the channel and thus reducing the maximum synthesizable capacitance.

However, note that as the transistor is biased under this condition, the Q-factor of the transistor is increased (i.e., the curves in Figure II-28 are located nearer to the Smith's chart boundary). This can be easily explained by the fact that as the pinch-off effect is enhanced the channel effective length is reduced, leading to a reduced channel resistance. On the other hand, when $V_{DS} > 0$ and $V_{ctrl} = V_{GS} > V_T$ a DC current flows from the drain to the source of the transistor. Hence, the device cannot be considered as a passive device. For instance, the considered CS-MOS reached a maximum current flow of 330 µA when $V_{DS} = V_{ctrl} = 1.2\ V$, leading to a power consumption of nearly 400 µW.

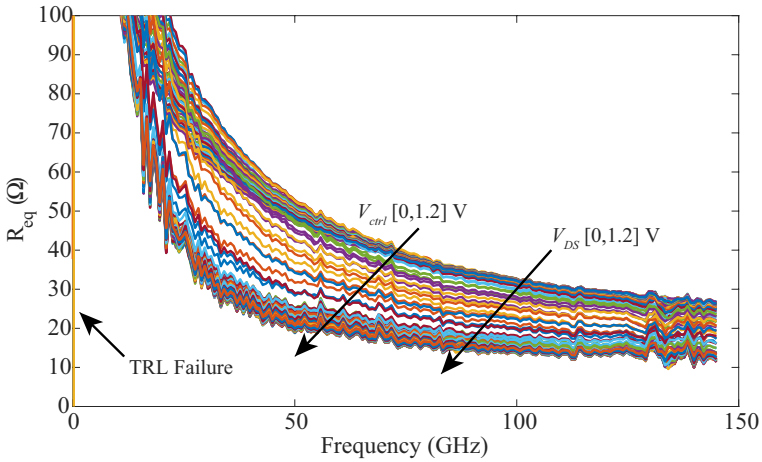

Figure II-29 Measured R_{eq} as a function of V_{ctrl} and V_{DS} in the 1-145 GHz band.

Figure II-29 displays the measured R_{eq} for the considered CS-MOS architecture in the 1-145 GHz frequency band as a function of V_{ctrl} and V_{DS}. As expected, R_{eq} is reduced as V_{ctrl} and/or V_{DS} increase. However, when compared to Figure II-24 a great difference is observed. For instance, let us consider the 100-GHz frequency. At that frequency, simulations reported a value of R_{eq} between 5 and 7 Ω, whereas measurements report an equivalent resistance ranging between 13 and 32 Ω. This can be explained by the inaccuracy of the PDK models beyond the transistor f_{max} as discussed above in section II.2.5.2.c).

Next, Figure II-30 shows the equivalent capacitance C_{eq} as a function of V_{ctrl} and V_{DS} in the 1-145 GHz frequency band. As expected, its magnitude increases with V_{ctrl} and decreases with V_{DS}. Note that when $V_{DS} = 0$ V the minimum value at 100 GHz is 22 fF, very similar to the minimum value obtained through post-layout simulation (i.e., 26 fF). However, at 100 GHz, post-layout simulations reported a maximum value of C_{eq} around 200 fF, whereas measurement-based results report a maximum value of 53 fF. In this scenario the tuning-range of the varactor is reduced to 2.6, much lower as compared to the 7.7 tuning range expected from post-layout simulations. The tuning range can be further increased when $V_{DS} > 0$. In that case, the magnitude of $C_{eq,min}$ can be further reduced to 19 fF at the expense of a DC power consumption. In that scenario, the tuning range is increased to 2.8. In this case, the magnitude of the complex impedance seen at the input of the CS-MOS varactor, Z_{eq}, is between 84 and 30 Ω. Similarly to the discussion carried out for R_{eq}, the difference between post-layout simulations and measurement results can only be attributed to the transistor model. The comparison between schematic-level and post-layout simulations show that the interconnections have a low impact on the expected tuning-range. Hence, the large tuning-range announced by the post-layout simulations is not attributable to an extraction artifact.

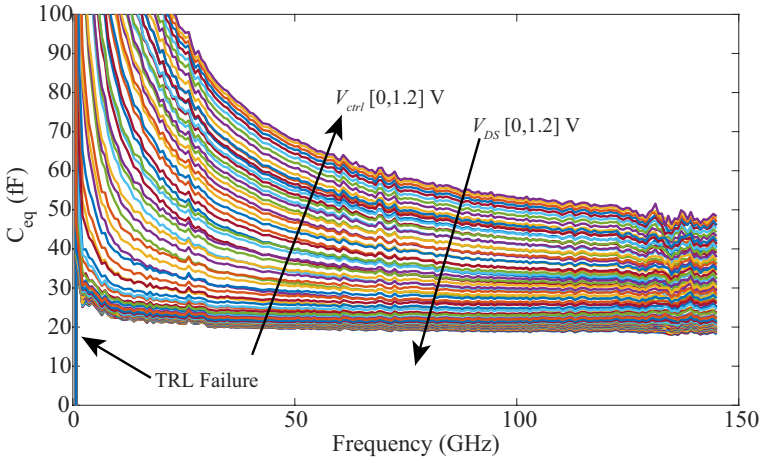

Figure II-30 Measured C_{eq} as a function of V_{ctrl} and V_{DS} in the 1-145 GHz band.

Finally, Figure II-31 shows the measured Q-factor as a function of V_{ctrl} and V_{DS}. Contrarily to the I-MOS, the Q-factor of the CS-MOS shows a greater frequency-dependence, as already observed in Figure II-26. At 100 GHz, the measured CS-MOS shows a minimum and maximum Q-factor of 1 and 6, respectively. Note that the minimum Q-factor extracted from simulation and measurement results is very similar. However, the magnitude leading to this result is very different. In the simulation-based results, for frequencies beyond around 80 GHz, the R_{eq} magnitude shows a low-variation with V_{ctrl} and a low magnitude. Hence, the low magnitude of the Q-factor seen in Figure II-26 comes from the large magnitude achieved by C_{eq}, as shown in Figure II-25. On the other hand, the measured CS-MOS shows a more reduced tuning-ratio while presenting greater values of R_{eq}. Hence, in the measurement-based results, the reduced Q-factor can be mostly attributed to resistive effects.

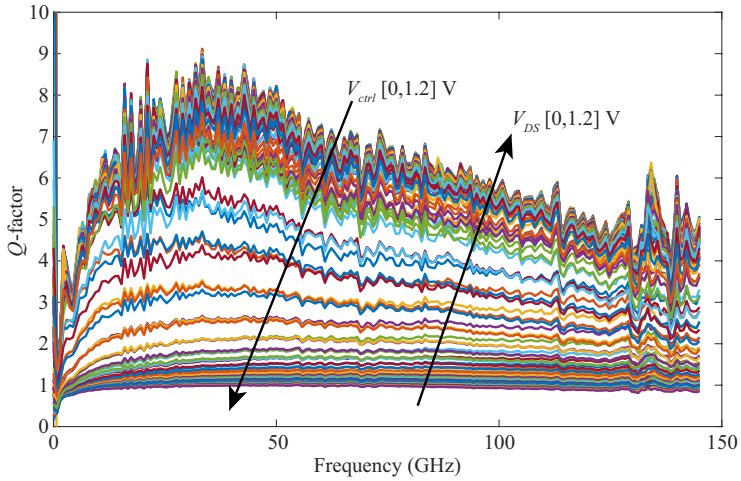

Figure II-31 Measured Q-factor as a function of V_{ctrl} and V_{DS} in the 1-145 GHz band.

To summarize, in this section the CS-MOS varactor was presented. The difference between post-layout simulation and measurement-based results is rather large. However, this could be expected as discussed earlier, due to the fact that most transistors models are not built for operation beyond the transistor f_{max}. However, measurement results show that this architecture is still quite competitive when compared to the transistors integrated in the same technology. For instance, let us consider the A-MOS transistor reported in section II.2.3. At 100 GHz, the simulated A-MOS reported a tuning range of around 3 and a maximum Q-factor of 6. Similar results are obtained using the CS-MOS architecture.

II.2.5.3. Comparison to the state-of-the-art

Two different varactor topologies have been discussed in the previous sections: (i) the I-MOS and (ii) the CS-MOS. To put the obtained results into perspective, Table II-II compares the reported results with the references already given in Table II-I.

TABLE II-II COMPARISON WITH THE STATE-OF-THE-ART MM-WAVE VARACTORS

Reference	Technology	Topology	Frequency (GHz)	Q-factor	C_{max}/C_{min}	FoM	P_{max} (μW)
[57]	28-nm FDSOI	A-MOS	100	10	1.4	14	0
[61]	130-nm CMOS	A-MOS	60	9	2	18	0
[62]	130-nm CMOS	A-MOS	50	5	2	10	0
[63]	130-nm CMOS	A-MOS	24	100†	1.6	160	0
This work	**55-nm BiCMOS**	**I-MOS**	**190**	**7**	**4.2**	**29**	**0**
This work	**55-nm BiCMOS**	**CS-MOS**	**100**	**6**	**2.8**	**17**	**400**
This work‡	**55-nm BiCMOS**	**CS-MOS**	**100**	**4**	**2.6**	**10**	**0**

† Q-factor at silicon-level (i.e., without interconnections to the BEOL). ‡$V_{DS} = 0$ V

First, note that measurement results for both varactors have been reported up to 145 GHz and 325 GHz for the CS-MOS and I-MOS architectures, respectively. To the best of my knowledge this is the first time that silicon-based results are reported up to those frequencies. In addition, an innovative CS-MOS architecture was explored.

The I-MOS varactor shows the greatest tuning range among the considered varactors. In addition, it shows second-to-best FoM, only overtaken by the varactor presented in [63]. However, it is important to note that the authors in [63] only report the intrinsic behavior of the varactor, without accounting for the interconnections to the BEOL, which would certainly lower the reported quality factor, due to resistive effects. Moreover, the results in [63] were obtained at a much lower frequency of 24 GHz, where higher Q-factor can be obtained, as explained at the beginning of this chapter.

Next, the CS-MOS is reported two times in Table II-II depending whether it is driven as a passive (i.e., $V_{DS} = 0$ V) or an active device. As a passive device, the maximum Q-factor is equal to 4 with a tuning range of 2.6, leading to a FoM of 10. On the other hand, when driven as an active device (i.e., $V_{DS} \geq 0$ V) the Q-factor achieves a maximum value of 6 while showing a tuning-range of 2.8, leading to a FoM of 17. In any case, the CS-MOS shows the greatest tuning range, only overpassed by the I-MOS architecture reported in this manuscript. However, it is important to note that when the CS-MOS is driven as an active device DC power is consumed.

II.3. Conclusions

In this chapter, the predominant architectures for the implementation of varactors on CMOS/BiCMOS were discussed. First, a behavioral description of the varactors based PN-junctions, A-MOS and the I-MOS architectures was carried out.

Next, the advantages of the I-MOS over the A-MOS were discussed. Reported results showed that the I-MOS varactors reported better results on the upper mm-wave frequency band, when compared to A-MOS varactors. Under this observation, authors decided to develop two architectures to exploit the capabilities of MOSFETs driven in inversion-mode to perform as varactors: (i) a classical I-MOS and (ii) the so-called CS-MOS architecture.

Then, two demonstrators were fabricated in the 55-nm STM BiCMOS technology. The I-MOS varactor was measured from 1 to 325 GHz. On the other hand, the CS-MOS varactor was measured from 1 to 145 GHz. TRL calibrations were performed on both devices to set the reference planes at the input of the actual DUT, leading to accurate characterization.

First, the I-MOS confirmed the relative stability of its Q-factor along the frequency spectrum, as observed in simulation. This device reported a Q-factor of 7 at 190 GHz and a tuning ratio of 4.2, leading to the greatest tuning-ratio among the considered varactors.

Next, the CS-MOS architecture reported a Q-factor of 4 and 6 at 100 GHz, depending whereas it operates as a passive or active varactor. The tuning-ratio at this frequency is equal to 2.6 and 2.8, respectively, depending on the considerations above. When operating as an active varactor, the CS-MOS architecture reported a consumption of 400 μW.

The measurements carried out in this chapter report the widest characterization of on-silicon varactors up to date. Both analyzed architectures show very competitive performance, as compared with the other considered varactors. In addition, the CS-MOS architecture was proposed for the first time as a viable topology for the design of on-silicon varactors. Even though the measured performance of this architecture is reduced, when compared with the PDK simulations, further optimization could be done when employing a model that better accounts for long-channel effects (e.g., NQS effects). Nevertheless, the obtained results can serve as a baseline to show the capabilities of the structure.

Chapter III

RTPS

The Reflection-Type Phase Shifters (RTPS) is the architecture chosen for the implementation of the phase-shifting function in this manuscript. As discussed in the Introduction of this manuscript, this architecture is very interesting for phase shifters aiming to provide with a continuous tuning of the output signal. The RTPS architecture is based on a relatively old concept. For instance, the first report of this architecture dates from the 60s [67]. Several types of phase shifters exist in the literature. Among passive phase shifters, the RTPS presents many advantages as discussed earlier in this manuscript, it is why it was decided to study this type of phase shifter.

An RTPS is composed of a 3-dB coupler (e.g. coupled-lines or branch-line coupler) and a highly-reflective load (e.g., varactors). Chapter I describes the available topologies in an integrated technology for the implementation of a 3-dB coupler with particular attention to the Coupled Slow-wave CoPlanar Waveguide (CS-CPW) topology, a kind of coupled-lines coupler. Then, in Chapter II the main varactor topologies, which are compatible with CMOS/BiCMOS processes, are discussed. Three main varactor families are investigated: (i) PN-junctions, (ii) A-MOS varactors, and (iii) I-MOS varactors. In this chapter, the theory and practical implementations of integrated mm-wave RTPS are described. The topology chosen for the implementation of the 3-dB couplers is the CS-CPW. These couplers are integrated together with varactors, in particular, A-MOS and I-MOS varactors. For more consistency with the rest of the manuscript, all the RTPS implementations presented in this Chapter were fabricated in the STM 55-nm BiCMOS technology.

The main goal of the three demonstrators presented in this Chapter was to explore innovative architectures for mm-wave RTPS. For instance, a first 60-GHz RTPS is presented, including Built-In Self-Test capabilities, which will be discussed in the next Chapter. Moreover, a 120-GHz RTPS is explored using I-MOS varactors. In this particular case, the authors aim to explore the capabilities of the RTPS architecture at high mm-wave frequencies together with the use of an innovative varactor architecture. In addition, another 120-GHz RTPS is presented using CS-MOS varactors. In that case, the authors aim at the exploration of another varactor architecture. This RTPS includes two control voltages, allowing a performance optimization.

This Chapter is divided as follows: in section 1, the theoretical basis and equations for the RTPS architecture are derived. Next, section 2 presents the current state-of-the-art mm-wave on-silicon RTPS architectures. Then, section 3 presents three main implementations of RTPS: (i) a 60-GHz RTPS with A-MOS varactors, (ii) a 120-GHz RTPS with I-MOS varactors, and (iii) a 120-GHz with CS-MOS varactors. In section 3, the presented RTPS are compared with the current RTPS literature. Finally, section 4 draws the main conclusions of this chapter.

III.1. Theoretical basis

First, in order to understand the basic operation of the RTPS architecture the equations describing its working principle must be discussed. For the sake of simplification, let us consider a backward-wave lossless coupler presenting a characteristic impedance Z_0 at each port and an infinite isolation. The coupler is then loaded at its through and coupled outputs with complex loads presenting an impedance Z_{load}. Finally, let us consider the input and output waves, a_i and b_i, where i represents the i-th port of the coupler, as depicted in Figure III-1.

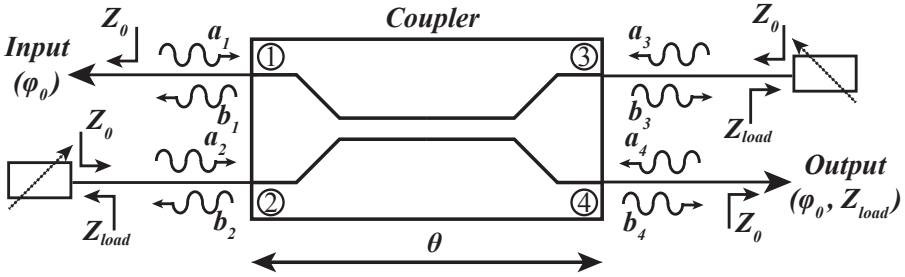

Figure III-1 Ideal RTPS with input and output waves at its ports.

Using these considerations, a wave analysis can be carried out. First let us write the S-Parameters of the coupler alone:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} 0 & S_{21} & S_{31} & 0 \\ S_{21} & 0 & 0 & S_{31} \\ S_{31} & 0 & 0 & S_{21} \\ 0 & S_{31} & S_{21} & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix}. \tag{III-1}$$

Hence,

$$\begin{cases} b_1 = S_{21}a_2 + S_{31}a_3 \\ b_2 = S_{21}a_1 + S_{31}a_4 \\ b_3 = S_{31}a_1 + S_{21}a_4 \\ b_1 = S_{31}a_2 + S_{21}a_3 \end{cases} \tag{III-2}$$

However, if perfect matching is considered, $a_4 = 0$. Hence,

$$\begin{cases} b_1 = S_{21}a_2 + S_{31}a_3 \\ b_2 = S_{21}a_1 \\ b_3 = S_{31}a_1 \\ b_4 = S_{31}a_2 + S_{21}a_3 \end{cases} \tag{III-3}$$

Now, let us consider the reflection coefficient at the interface between the loads and the coupler (i.e., ports 2 and 3). The reflection coefficient Γ_L can be written as:

$$\Gamma_L = \frac{Z_{load} - Z_0}{Z_{load} + Z_0}. \tag{III-4}$$

Hence,

$$a_2 = \Gamma_L \cdot b_2 \tag{III-5}$$

and

$$a_3 = \Gamma_L \cdot b_3 \tag{III-6}$$

Then, a_2 and b_3 in (III-3) can be substituted by (III-5) and (III-6), leading to:

$$\begin{cases} b_1 = S_{21} \cdot \Gamma_L \cdot b_2 + S_{31} \cdot \Gamma_L \cdot b_3 \\ b_2 = S_{21} a_1 \\ b_3 = S_{31} a_1 \\ b_4 = S_{31} \cdot \Gamma_L \cdot b_2 + S_{21} \cdot \Gamma_L \cdot b_3 \end{cases} \quad \text{(III-7)}$$

Substituting the expressions of b_2 and b_3 in (III-7) into the expressions of b_1 and b_4 in (III-7) yields:

$$b_1 = \Gamma_L (S_{21}^2 + S_{31}^2) a_1, \quad \text{(III-8)}$$

and

$$b_4 = (2\Gamma_L \cdot S_{31} \cdot S_{21}) a_1. \quad \text{(III-9)}$$

Hence, S_{11} can be expressed as:

$$S_{11} = \frac{b_1}{a_1} = \Gamma_L (S_{21}^2 + S_{31}^2), \quad \text{(III-10)}$$

and S_{41} as:

$$S_{41} = \frac{b_4}{a_1} = 2\Gamma_L \cdot S_{31} \cdot S_{21}. \quad \text{(III-11)}$$

As demonstrated in Chapter 1, the expression of S_{21} in a lossless, perfectly-matched coupler is:

$$S_{21} = \frac{jk \sin(\theta)}{\sqrt{1-k^2}\cos(\theta) + j\sin(\theta)}, \quad \text{(III-12)}$$

where θ represents the electrical length of the coupler and k the coupling coefficient. On the other hand, the expression of S_{31}, in a coupler under these considerations, was demonstrated to be:

$$S_{31} = \frac{\sqrt{1-k^2}}{\sqrt{1-k^2}\cos(\theta) + j\sin(\theta)} \quad \text{(III-13)}$$

In these expressions k can also be substituted by:

$$k = \frac{Z_{Ce} - Z_{Co}}{Z_{Ce} + Z_{Co}} \quad \text{(III-14)}$$

where Z_{ce} and Z_{co} represent the even- and odd-mode characteristic impedances.

Finally, it is worth to recall that the mixed-mode characteristic impedance of the coupler Z_C, which in this case is assumed to be equal to Z_0, can be expressed as:

$$Z_C = Z_0 = \sqrt{Z_{Ce} \cdot Z_{Co}} \quad \text{(III-15)}$$

If a 3-dB backward-wave coupler is considered, then:

$$k = \frac{1}{\sqrt{2}} \quad \text{(III-16)}$$

and analyzed at its central frequency, where:

$$\theta = \pi/2 \text{ radians}. \quad \text{(III-17)}$$

Then,

$$S_{11} = 0. \tag{III-18}$$

Hence, at the central frequency, the considered RTPS presents perfect matching. On the other hand,

$$S_{41} = -j \cdot \Gamma. \tag{III-19}$$

Thus, in order to have a lossless RTPS (i.e., $|S_{41}| = 1$) this condition must hold:

$$|\Gamma| = 1 \tag{III-20}$$

If Z_0 is considered to be a purely real impedance, the condition in (III-20) holds when:

$$\begin{cases} \Re(Z_{load}) = 0 \\ \Re(Z_{load}) = \infty \end{cases} \quad \forall\, \Im(Z_{load}) = [-\infty, \infty] \tag{III-21}$$

On the other hand, a transmission zero is reached when $Z_{load} = Z_0$.

Note that (III-19) can also lead to an output gain when $|\Gamma| > 1$ (i.e., active load, when Z_0 is purely real). Interestingly, to the best of my knowledge, this property of 3-dB couplers has never been used to realize a kind of active RTPS.

III.1.1. Frequential analysis

The theoretical demonstration carried out above showed the working principle of the RTPS architecture at the frequency for which the 3-dB coupler has an electrical length $\theta = \pi/2$. However, it is interesting to analyze the behavior of an RTPS as a function of θ (i.e., equivalent to a normalized frequency analysis) and $|\Gamma_L|$. For the sake of simplification, let us use the same considerations above. First, let us analyze the behavior of the reflection coefficient at the input of the system (S_{11}) for θ ranging between 0 and π radians, and $|\Gamma|$ between 0 and 1.

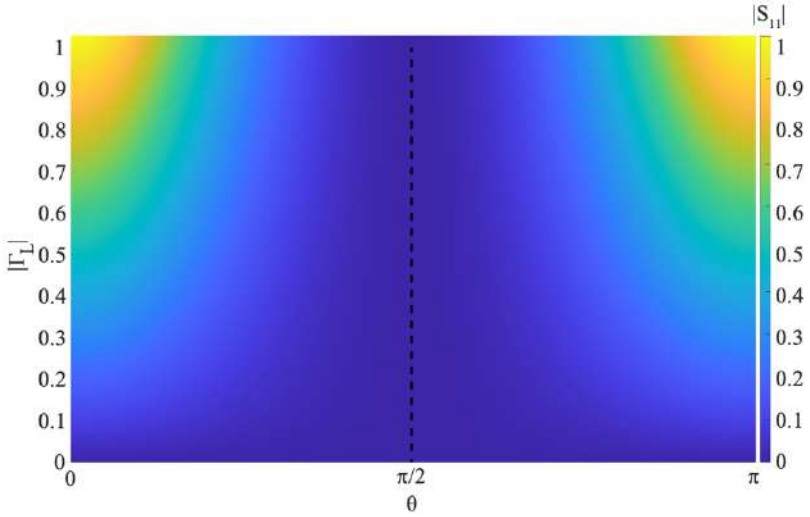

Figure III-2 $|S_{11}|$ as a function of θ and $|\Gamma_L|$.

In Chapter I, it was demonstrated that a backward-wave coupled-lines-based coupler presented a null return loss in the whole frequency spectrum whenever:

$$\beta_e = \beta_o = \beta, \tag{III-22}$$

and (III-15) hold, where β_e, β_o, and β represent the even-, odd-, and mixed-mode phase constants.

However, note that the magnitude of S_{11} is only equal to 0 for any value of $|\Gamma_L|$ when $\theta = \pi/2$ (i.e., at the coupler central frequency), as shown in Figure III-2. Hence, although the considered coupler presents an infinite bandwidth, the RTPS presents a limited bandwidth. On the other hand, the relative bandwidth is still quite large and suitable for many wideband applications.

Next, let us carry out a similar analysis for $|S_{41}|$. For this purpose, the same variations of θ and $|\Gamma_L|$ were considered. Figure III-3 depicts the results of this analysis.

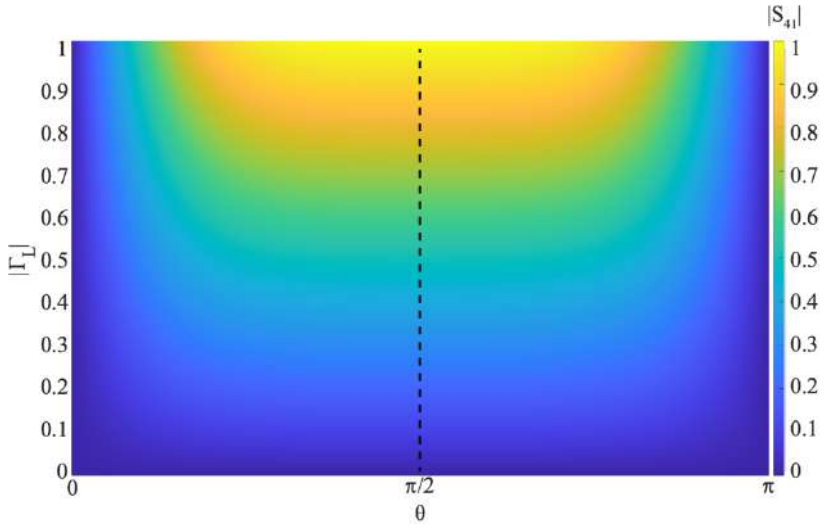

Figure III-3 $|S_{41}|$ *as a function of* θ *and* $|\Gamma_L|$.

Figure III-3 shows that a transmission maximum is achieved when $|\Gamma_L| = 1$ and $\theta = \pi/2$. When a coupler with a real characteristic impedance is considered, (III-21) must hold to achieve a unitary magnitude of Γ_L.

Note that, when an ideal coupler is considered, the central frequency of the coupler clearly matches the RTPS return loss minimum (i.e., darkest-blue zone in the middle of Figure III-2). However, most of the high-performance RTPS reported in the literature show two return loss minima (e.g., [68]). To explain this phenomenon, let us derive the relationship of Z_{Ce} and Z_{Co} as a function of k, when perfect matching is considered:

$$Z_{Ce} = Z_0\sqrt{\frac{1+k}{1-k}} \qquad Z_{Co} = Z_0\sqrt{\frac{1-k}{1+k}} \tag{III-23}$$

Then, let us carry out the same analysis as above while considering a perfectly-matched coupler showing an over-coupling (i.e., $k > 1/\sqrt{2}$) of 0.1, i.e., $k = 0.1 + 1/\sqrt{2}$. In this scenario, the coupler presents two return loss minima, as shown in Figure III-4.

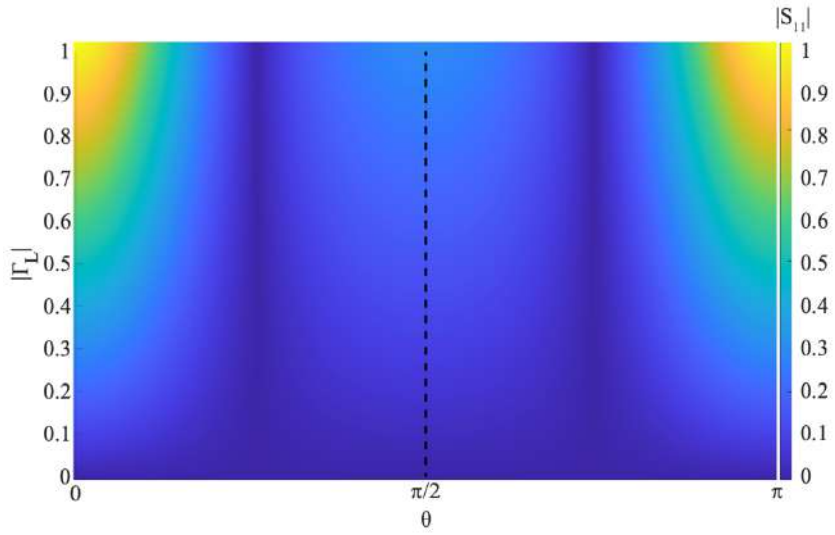

Figure III-4 $|S_{11}|$ as a function of θ and $|\Gamma_L|$ when $k = 0.1 + 1/\sqrt{2}$ (i.e., 1.9 dB).

The two transmission maxima are still seen at the same frequencies for which the coupler presents the θ leading to the reflection minima shown in Figure III-4. This result is shown in Figure III-5.

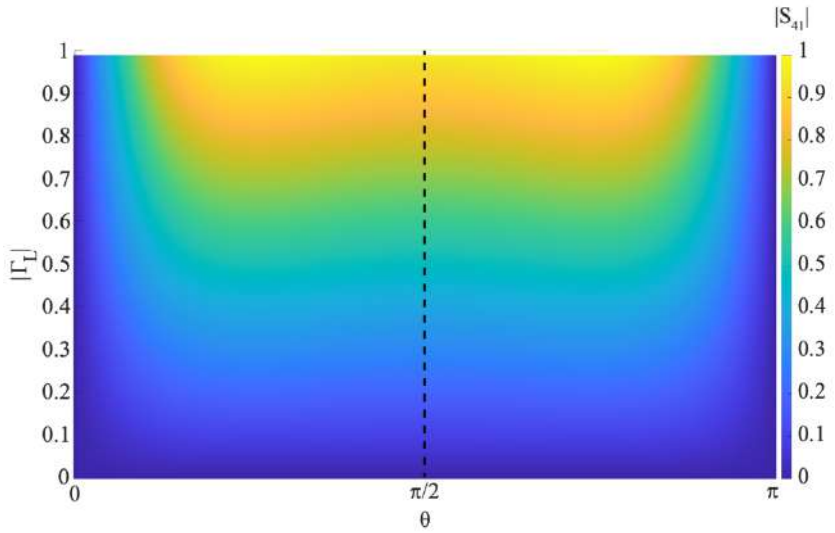

Figure III-5 $|S_{41}|$ as a function of θ and $|\Gamma_L|$ when $k = 0.1 + 1/\sqrt{2}$ (i.e., 1.9 dB).

Note that, in both cases, the bandwidth has been increased. Hence, the design of slightly over-coupled 3-dB couplers can extend the band of the RTPS. Usually, this appears as a result of the impossibility to obtain a k that is exactly equal to $1/\sqrt{2}$. On the other hand, couplers with $k < 1/\sqrt{2}$ only lead to a lower overall magnitude of S_{41}.

In this section, the basic working principles of the RTPS topology have been discussed. In the next section, the main mm-wave on-silicon implementations of the RTPS architecture will be analyzed.

III.2. State-of-the-art RTPS

Table III-I presents the state-of-the-art mm-wave RTPS integrated on silicon-based technologies reported in the current literature. RTPS topologies presenting a discrete or continuous tuning of the phase are considered. This table also presents the figure-of-merit (FoM) of the considered RTPS, which is calculated as follows:

$$FoM = \frac{\Delta\varphi \ \ [^\circ]}{IL_{max}\ [dB]} \tag{III-24}$$

where $\Delta\varphi$ represents the maximum phase shift (i.e., $\varphi_{max} - \varphi_{min}$) and IL_{max} the maximum insertion loss for the considered $\Delta\varphi$. Up to here, S_{41} represented the insertion loss of the RTPS as it was consistent with the analysis carried out above. However, for the rest of the document, the insertion loss of the RTPS will be labelled as S_{21} for more consistency with the number of accessible ports in an RTPS.

Finally, the power consumption, area overhead and relative bandwidth (RBW) are also given in this table.

TABLE III-I STATE-OF-THE-ART MM-WAVE ON-SILICON RTPS

Ref.	Technology	Frequency (GHz)	RBW† (%)	$\Delta\varphi$/resolution (º)	$\lvert S_{21}\rvert$ (dB)	RL (dB)	FoM* (º/dB)	Area (mm^2)	Power consuption (mW)
[69]	55-nm BiCMOS	30-50	50	60/cont$^+$.	2.8-5	>10	12	0.18	0
[70]	65-nm CMOS	26-30	14‡	360/11.25	6.8-9.2	>5	45	0.16	0
[71]	65-nm CMOS	54-66	20**	90/11.25	5.7-7.9	>12	11	0.034	0
[72]	45-nm SOI CMOS	28-29	3.5	340/2.8	2-20	>7	20	0.18	-
[73]	65-nm CMOS	26-32	17#	379/cont.	7-11	>15	41	0.076	0
[74]	90-nm CMOS	57-64	11#	190/cont.	6-11	>15	18	0.027	0
[75]	130-nm BiCMOS	59-62	5	367/cont.	9.2-10.3	>10	35.6	0.16	0

†For RL > 10 dB; *At the central frequency; ‡For RL > 5 dB; **For RL > 12 dB; #For RL > 15 dB; $^+$continuous

In order to better understand the current approaches for the design of on-silicon mm-wave RTPS, let us analyze the works presented above. The work in [69] presents an RTPS with a central frequency of 40 GHz with 60º phase shift integrated in the STM 55-nm BiCMOS technology. In this paper, a 3-dB coupler using the CS-CPW architecture is used. As discussed in chapter I, this architecture helps equalizing the even- and odd- mode propagation constants, leading to very wideband couplers. Hence, this work presents the greatest RBW among the considered works.

Next, [70] uses a lumped-element coupler using CLC (capacitor-inductor-capacitor) π-networks, leading to a discrete 360º phase shift with 11.25º of resolution. Both varactors of the π-network used to load the coupler are integrated using different varactors controlled by separate biasing voltages (e.g., V_{c1} and V_{c2}). The dimensions of the CLC network were optimized so as to obtain a given phase shift with multiple combinations of V_{c1} and V_{c2}. Then, the combinations of these biasing voltages that lead to the lowest insertion loss are chosen. Using this approach, authors obtain the greatest FoM among the considered RTPS.

In [71], authors present a RTPS with 11.25º resolution around 60 GHz. The 3-dB coupler is integrated using a lumped-element transformer-type architecture. Three biasing voltages allow to choose between different loads, which provide either 11.25º, 22.5º or 45º (i.e., a 3-bit system). The permutation of these loads allows the coverage of a 90º phase shift. Note that the use of lumped-

elements leads to a very reduced footprint. However, their limited performance at those frequencies leads to the lowest FoM among the considered architectures.

In the brief presented in [72], a 7-bits RTPS architecture is described, presenting 340º phase shift (i.e., a resolution of 2.8º). The described topology, frequency band and footprint is very similar to the work presented in [70]. However, the much finer resolution leads to an increase in the insertion loss and thus, a reduction of the FoM.

Next, authors in [73] describe two RTPS topologies presenting 360º of phase shift. Both architectures use the same coupled-lines broadside microstrip 3-dB coupler. However, their loads are integrated using a single varactor or two varactors. As both architectures lead to similar performance, only the double-varactor architecture is considered here. This architecture needs two biasing voltages. In this work, similarly to [70] and [72], both biasing voltages are varied, a given phase shift is obtained for several combinations of the control voltages. Then, the subset of control voltages leading to the lowest insertion loss is chosen. Using this approach, the authors reach a sub-degree resolution. Hence, this work can be considered as continuous-tuning. Note that the FoM is almost equal to the one obtained in [70], while presenting a much greater resolution and reduced footprint.

Authors in [74] present a continuous-tuning RTPS with 190º phase shift capabilities. A MOS switch is used to create an artificially-tuned inductance. The 3-dB coupler is integrated using microstrip lines in a broadside configuration. This work reports the most compact architecture among the considered works, with a footprint of only 0.027 mm^2.

Finally, the work in [75] describes an RTPS with 367º phase shift. Each of the loads of the 3-dB coupler are composed of a complex network containing two varactors, three inductors and a transformer. A parametric analysis of the load is carried out, similarly to [70], [72], [73]. Then, the biasing voltages for each of the two varactors composing the load are chosen in order to achieve different goals (i.e., minimum insertion loss or minimum magnitude imbalance). Good performance is reported at the central frequency. However, the system shows a limited bandwidth. The measurement results of the 3-dB coupler show its very limited performance over a large bandwidth. Hence, the limited bandwidth of the whole RTPS can be explained by the limited performance of the coupler.

In this manuscript, four different designs RTPS designs will be presented. For instance, the 60-GHz coupler uses very similar architecture to [69]. The 120-GHz coupler with I-MOS varactors aims to increase the overall phase shift through the use of I-MOS varactors, while using a relatively similar architecture to [69]. Finally, the 120-GHz aims to reach the 360º phase shift using CS-MOS varactors. In latter architectures, two biasing voltages are used and the combinations leading to reduced losses are chosen, similarly to the works in [70], [72], [73], [75].

III.3. Implemented mm-Wave RTPS

In order to show the capabilities of the RTPS topology, four of these systems were designed in the STM 55-nm BiCMOS technology. In this section, the practical implementation and measurement results of the designed couplers are discussed. All of the considered RTPS in this section were designed using varactors as tuning elements. However, different varactor topologies were considered to better illustrate their trade-offs. In addition, different frequency bands are addressed in order to show the capabilities of RTPS in a large frequency band.

The couplers were designed with the CS-CPW architecture, described in Chapter I. On the other hand, the different varactor topologies used in these designs were discussed in Chapter II.

III.3.1. 60-GHz RTPS with A-MOS varactors

The first RTPS was designed with an operating frequency of 60 GHz. In this case, Accumulation-mode MOS (A-MOS) varactors were used. In addition to the phase-shifting capabilities, this system also integrates circuitry for Built-In Self-Test (BIST) applications. More precisely, circuitry aiming to perform the so-called Oscillation-Based Test (OBT). The nature and measurement results of the OBT circuitry will be discussed in Chapter IV of this manuscript. For the sake of clarity, in this

chapter the impact and design of the OBT will be omitted. Figure III-6 shows a block representation of the 60-GHz RTPS.

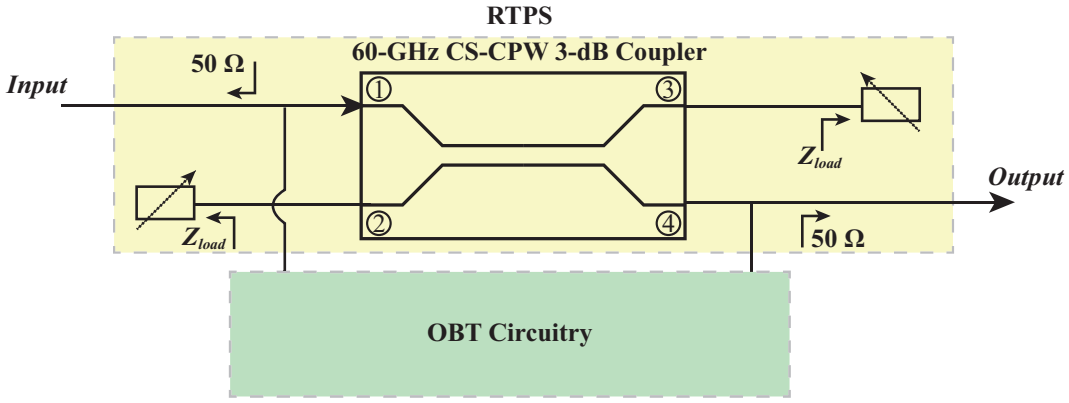

Figure III-6 Block representation of the 60-GHz RTPS with the OBT circuitry.

Next, let us analyze the different elements forming the 60-GHz RTPS.

III.3.1.1. Coupler Design

As previously introduced, the coupler was designed using the CS-CPW architecture. The coupler was designed using metals 7 and 8 for the signal and ground strips. These metal layers were stacked using the maximum via density allowed by the technology mimicking a solid conductor. On the other hand, the floating shield was placed in the 5th layer. The physical dimensions that define the geometry of the coupler are given in Table III-II.

TABLE III-II PHYSICAL DIMENSIONS OF THE 60-GHZ 3-DB COUPLER.

W_S	S	W_G	G	SS	SL	CS	Length
12 µm	5 µm	12 µm	79 µm	0.5 µm	0.5 µm	2 µm	420 µm

The chosen geometry led to a total footprint of 0.09 mm^2. Figure III-7 shows a micrograph of the fabricated device with the feeding lines from the coupler to the 50-µm-pitch GSGSG pads.

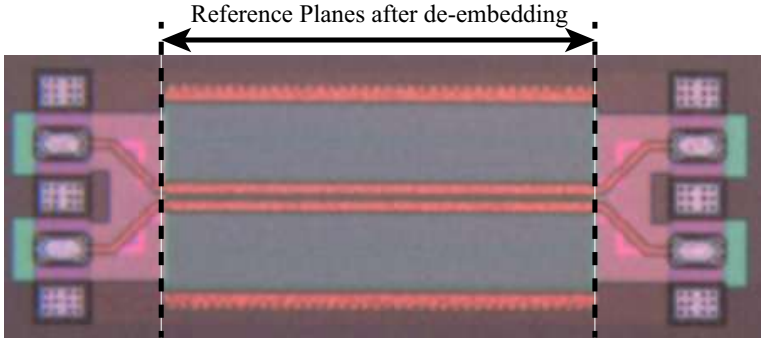

Figure III-7 Micrograph of the fabricated 60-GHz 3-dB coupler.

The coupler was measured using an Anritsu VectorStar ME7838A4 4-ports Vector Network Analyzer (VNA), from 1 GHz to 100 GHz. An LRRM calibration [42] was performed on a Formfactor 138-356 ISS (Impedance Standard Substrate) to set the reference at the probe tips. Figure III-8 displays the measured S-Parameters magnitude of the fabricated coupler. At 60 GHz, the through and coupled ports present an insertion loss of 3.2 dB and 3.7 dB, respectively. The isolation and return-loss are equal to 11 dB and 20 dB, respectively. Note that the measured coupler presents a poor isolation, as compared to the simulation. This can be explained by uneven propagation constants for the even- and odd-modes. More advanced simulation techniques were used for the rest of the realized couplers, as described in

Chapter I of this manuscript, which led to an overall better performance. However, the coupler presents sufficiently good performance to be used as a building-block for an RTPS.

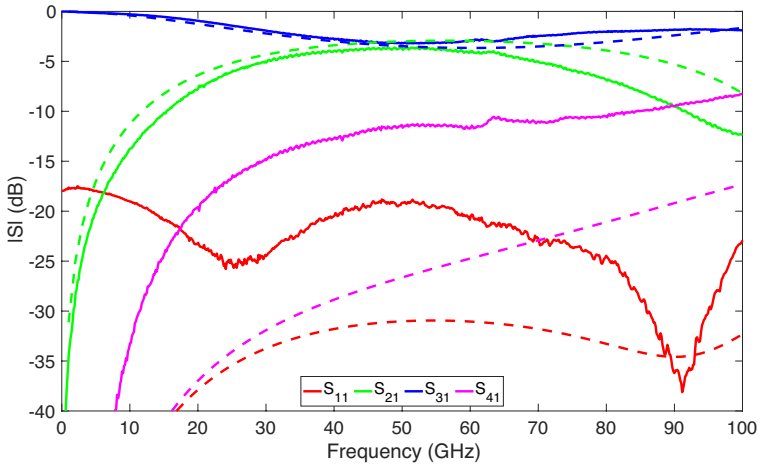

Figure III-8 Measured (solid-line) and simulated (dashed-line) S-Parameter magnitude of the 60-GHz 3-dB coupler

Figure III-9 displays the measured and simulated phase difference at the coupled and through ports, as seen from the input port as solid- and dashed-lines, respectively. At 60-GHz the phase difference is equal to 92º. However, note that above around 75 GHz, strong drift is observed in the phase difference. Again, this can be explained by unequal propagation constants for the even- and odd-modes.

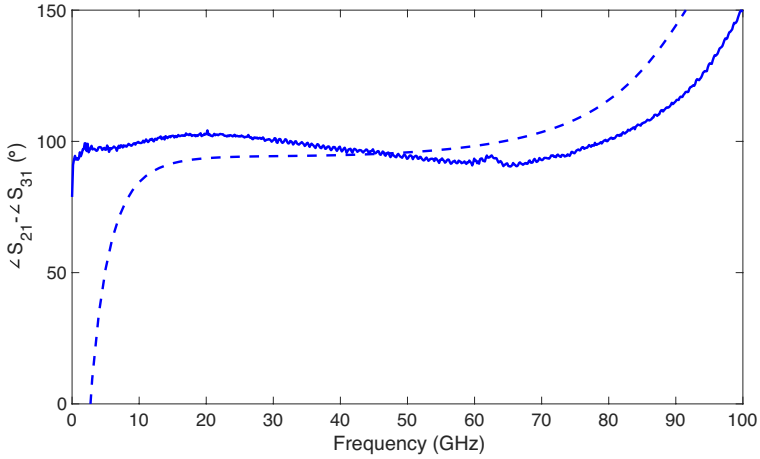

Figure III-9 Measured (solid-line) and simulated (dashed-line) phase difference of the 60-GHz 3-dB coupler.

To summarize, the proposed 3-dB coupler presents good performance for an RTPS application at 60 GHz. At this frequency, the relatively balanced distribution of the power between the through and coupled outputs, together with a low return loss and a 90º phase shift between its outputs present a coupler adapted for this purpose. Next, let us analyze the varying loads connected to the coupler to realize the RTPS.

III.3.1.2. Load Design

As introduced above, the loads were designed using thick-oxide A-MOS varactors. The models of these varactors are embedded in the Process Design Kit (PDK) of the STM 55-nm BiCMOS technology. Figure III-10 shows a schematic-view of the 60-GHz RTPS load.

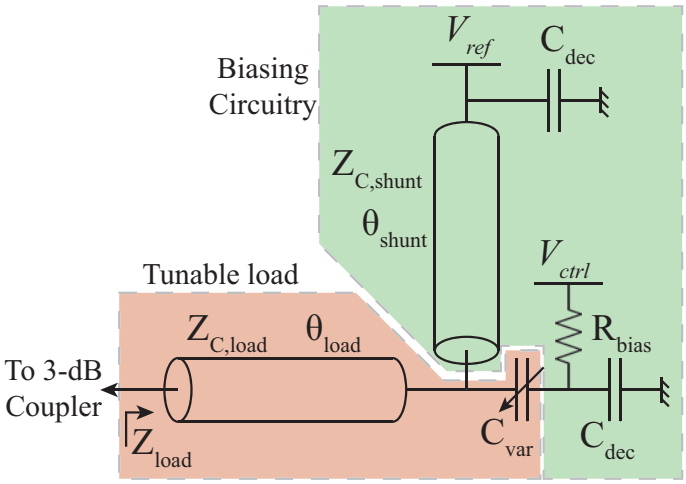

Figure III-10 Schematic view of the 60-GHz RTPS load.

a) Biasing circuitry

The thick-oxide A-MOS varactors used in this design require a total voltage difference of 2.5 V between their ports to operate at their full range. As explained in Chapter II, this can be solved with two approaches, either the control voltage V_{ctrl} in Figure III-10 operates between -1.25 to 1.25 V or a reference voltage V_{ref} is applied, setting the other port to a fixed voltage of 1.2 V. In this configuration, V_{ctrl} operates the varactor by setting its voltage between 0 and 2.5 V. In this RTPS, the second approach was chosen since it was also more convenient for the OBT circuitry. This approach has the advantage of operating the A-MOS using only positive voltages. Nevertheless, it requires to introduce additional biasing circuitry for V_{ref}. Note that the biasing circuitry of V_{ctrl} consists only of a large-value resistor, R_{bias}. In a conventional RTPS, a similar approach could be taken for the design of the V_{ref} biasing circuitry. However, using a large-value resistor limits the DC-power that can be delivered through this net. In our system, integrating the OBT circuitry, DC-power has to be delivered by V_{ref}. Hence, a 60-GHz quarter-wavelength microstrip line (i.e., at 60 GHz, $\theta_{shunt} = \pi/2$) was used and terminated with an RF short-circuit (i.e., large decoupling capacitor C_{dec}). These considerations led to a microstrip with a physical length of 610 µm and a width of 0.54 µm, which leads to a characteristic impedance of around 80 Ω. A high characteristic impedance was used for this purpose as the bandwidth for which these transmission lines present a high input impedance is larger than lines of lower impedance. Finally, the decoupling capacitance was integrated using the Metal-Oxide-Metal (MOM) technology and a value of around 2 pF, showing an imaginary impedance of around -1.4 Ω, close to an RF short-circuit. Another decoupling capacitance is placed to avoid a short-circuit between V_{ctrl} and the ground. This capacitance was designed using the same architecture and geometry as for the C_{dec} placed to short-circuit the quarter-wavelength stub for V_{ref}.

b) Tunable load

The actual tuning circuit is composed of a microstrip line and the varactor C_{var}. The capacitance C_{dec} placed in a series connection with C_{var} will be ignored as the capacitive value seen at the input of the load is mostly determined by C_{var}, which presents a much lower capacitance than C_{dec}.

A transmission line was placed before the varactor to increase the effective tuning ratio of C_{var}. For instance, let us consider an electrically-short transmission line in a series connection with a varactor presenting minimal and maximal capacitances C_{min} and C_{max}, respectively. When a transmission line is electrically short, it can be approximated by an inductance, L. In this scenario, if the varactor is terminated by a short circuit, the equivalent capacitance (C_{eq}) of series circuit can be written as:

$$C_{eq} = \frac{-1}{\Im(Z_{load})\omega} = \frac{C_{var}}{1 - LC_{var}\omega^2}. \qquad \forall\, LC_{var}\omega^2 < 1 \tag{III-25}$$

Next, the tuning ratio $C_{eq,max}/C_{eq,min}$, for the maximal and minimal varactor capacitances C_{max} and C_{min}, of the equivalent capacitance in (III-25) can be written as:

$$\frac{C_{eq,max}}{C_{eq,min}} = \frac{C_{max}}{1 - LC_{max}\omega^2} \cdot \frac{1 - LC_{min}\omega^2}{C_{min}}, \tag{III-26}$$

which can be further rearranged to:

$$\frac{C_{eq,max}}{C_{eq,min}} = \frac{C_{max}}{C_{min}} \cdot \frac{1 - LC_{min}\omega^2}{1 - LC_{max}\omega^2}. \tag{III-27}$$

Hence, if the values of L and C_{max} are chosen in such a way that $LC_{max}\omega^2 < 1$ (i.e., below their resonance frequency) (III-27) yields a greater capacitance variation than the one obtained by the stand-alone varactor (i.e., which is equal to C_{max}/C_{min}).

This effect can be also seen when characterizing varactors up to very high frequencies. Most of the varactors present inductive effects at their inputs, as a result of the metallic connections to the BEOL. For instance, the I-MOS presented in Chapter II presents a remarkable increase of the tuning ratio above around 230 GHz, as a result of the input inductance.

In the considered circuit, the transmission line used for this purpose was optimized with a characteristic impedance $Z_{C,load}$ of 50 Ω and an electrical length of 8.1º, achieved using a microstrip line of 55 µm.

c) Simulation results

The A-MOS varactors were designed using 3 thick-oxide varactors in a parallel configuration. Each of the varactor contained 4 A-MOS cells composed by 2 fingers with a width and a length of 2.5 µm and 55 nm, respectively. Figure III-11 shows a simulation at 60-GHz of the input resistance of the schematic shown in Figure III-11 as a function of V_{ctrl}. The equivalent input capacitance is calculated as in (III-25), while the equivalent input resistance is calculated as $\Re(Z_{load})$.

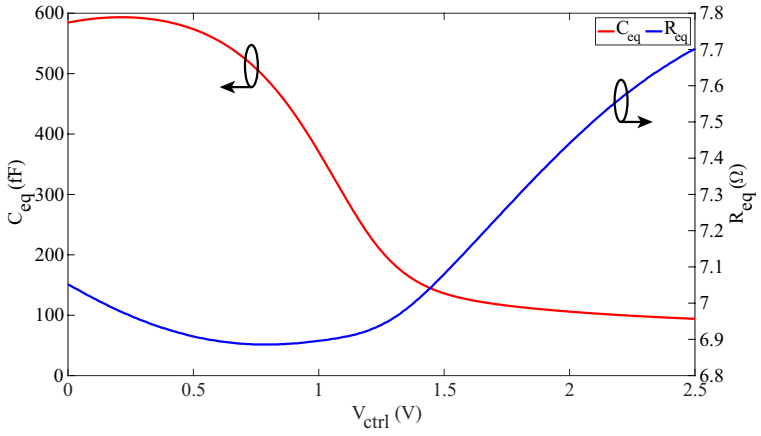

Figure III-11 Simulated input equivalent resistance R_{eq} and capacitance C_{eq} of the 60-GHz RTPS load.

Note that the results presented in Figure III-11 include the biasing circuitry as well as the decoupling capacitor. Using the results of C_{eq} and R_{eq}, the Q-factor at the input of the load can be calculated as:

$$Q = \frac{-\Im(Z_{load})}{\Re(Z_{load})}, \tag{III-28}$$

Figure III-12 shows the Q-factor simulation results for the 60-GHz RTPS load. Note that the Q-factor is limited as compared to other A-MOS varactors in the same frequency range. This can easily be explained by the fact that a whole circuit with biasing circuitry, decoupling capacitances and an input transmission line is considered. Nevertheless, the load shows a tuning ratio of 6. It can be easily observed that the reported tuning ratio greatly overpasses all the A-MOS varactors presented in Chapter II. For instance, the chosen A-MOS varactor alone, with its biasing circuitry, would present a tuning ratio of 3.5 and a Q-factor between 1.6 and 4.5. The larger tuning range is achieved thanks to the use of the input transmission line, as explained above.

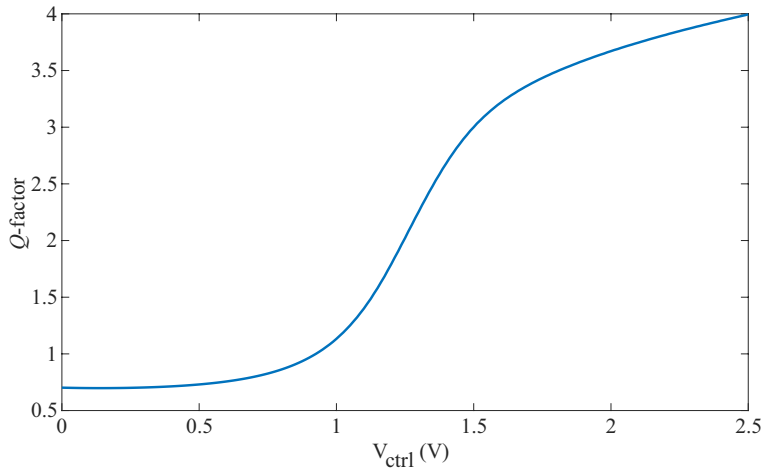

Figure III-12 Simulated input equivalent Q-factor of the 60-GHz RTPS load.

III.3.1.3. Measurement results

The 60-GHz RTPS was measured using an Anritsu VectorStar ME7838A4 4-ports VNA, from 1 GHz to 100 GHz. A first-tier LRRM calibration was performed on a Formfactor 138-356 ISS (Impedance Standard Substrate) to set the reference at the probe tips. Then, a second-tier TRL [43] was performed to set the reference planes at the input of the DUT. For the TRL calibration, a 50-Ω Line standard with an offset length, as compared to the Thru standard, of 350 µm was used. This offset length gives an offset electrical length of 7.5º at 10 GHz and 75º at 100 GHz. Hence, this TRL calibration can be considered accurate in the 10-100 GHz frequency band. Figure III-13 shows a micrograph of the fabricated 60-GHz RTPS with its OBT circuitry.

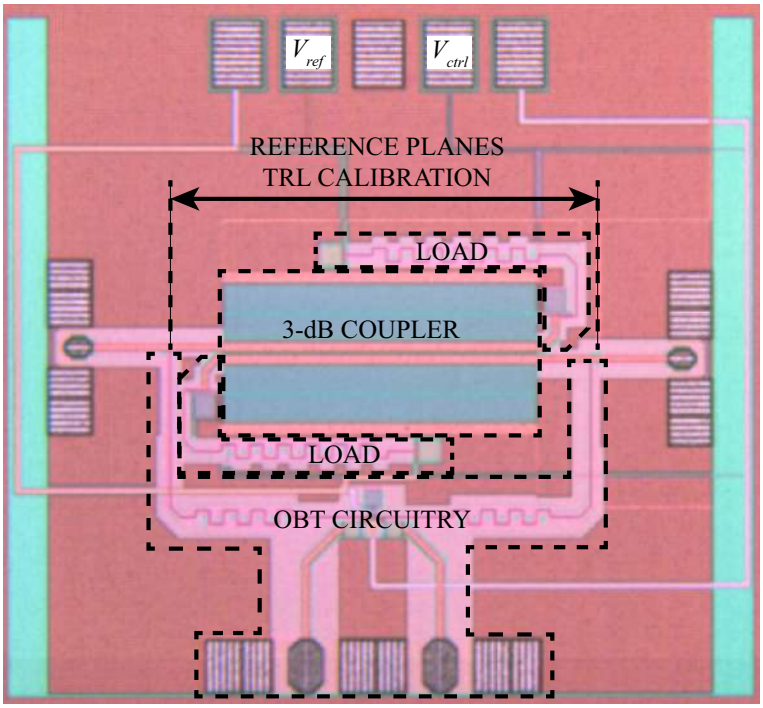

Figure III-13 Micrograph of the 60-GHz RTPS and its OBT circuitry.

The core of the RTPS (i.e., coupler and loads) presents a footprint of 0.19 mm^2. Note that the quarter-wavelength microstrip lines used for V_{ref} have been meandered around the coupler in order to reduce their footprint.

Figure III-14 shows the magnitude of S_{11} and S_{21} at 60 GHz for $V_{ref} = 1.2$ V and $V_{ctrl} = [0 - 1.9]$ V. Note that the biasing voltage range to achieve a full-range capacitance variation is $[0 - 2.5]$ V. However, a probe broke and measurements could not be performed for $V_{ctrl} > 1.9$ V. Hence, measurement results are shown only up to this voltage. At this frequency, the return and insertion loss present a minimal and maximal magnitude of 14 and 4.9 dB, respectively. Note that the insertion loss is relatively flat, leading to a limited insertion loss magnitude imbalance of 0.8 dB.

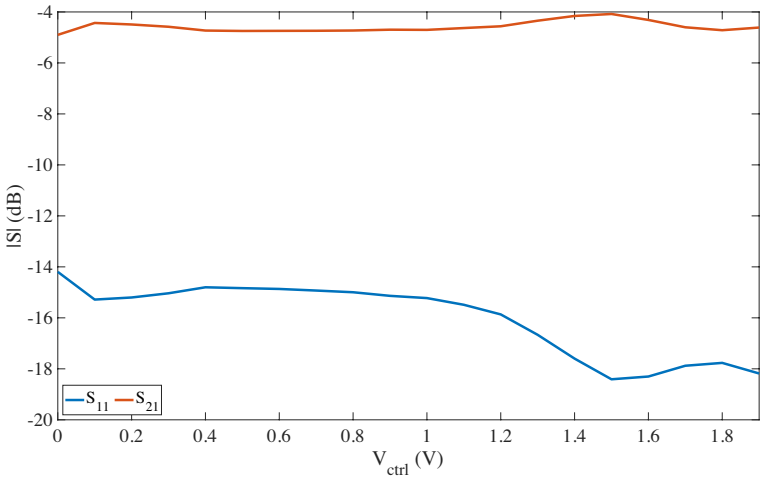

Figure III-14 Measured S-Parameter magnitude at 60 GHz when $V_{ref} = 1.2$ V and $V_{ctrl} = [0, 1.9]$ V.

Next, Figure III-15 shows the measured phase shift at 60 GHz as a function of V_{ctrl}. At this frequency, the system presents a phase shift of 32º. It can be clearly seen that for $V_{ctrl} > 1.9$ V a greater phase shift can be expected. As a guideline, simulation results predict around 40º degrees of phase shift. However, only measurements up to 1.9 V are shown for the reasons explained above.

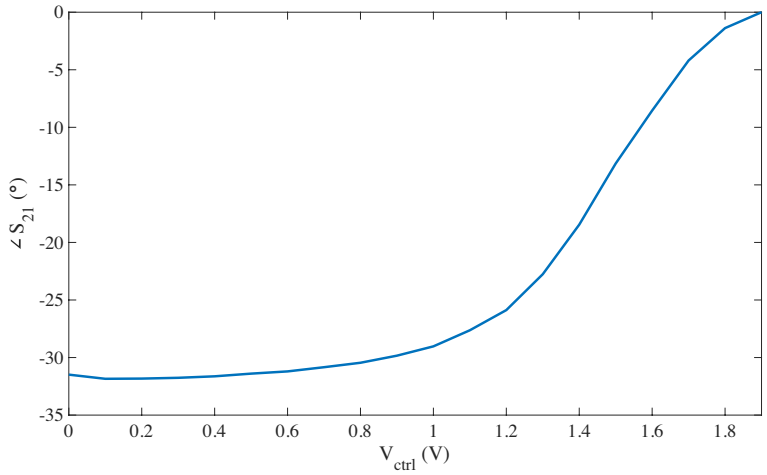

Figure III-15 Measured phase shift at 60 GHz when $V_{ref} = 1.2$ V and $V_{ctrl} = [0, 1.9]$ V.

Figure III-16 shows the magnitude of S_{11} and S_{21} in the 1-100 GHz frequency band when $V_{ref} = 1.2$ V and $V_{ctrl} = [0 - 1.9]$ V. When a 10-dB return loss limit is considered for the evaluation of the bandwidth, the measured RTPS has a bandwidth of 35 GHz, from 50 to 85 GHz (i.e., 58% of relative bandwidth, as compared to its central frequency). In this band, the system shows an insertion loss between 3.8 and 10 dB. Worst-case losses are located around 85 GHz, where both coupler and load are further away from their central frequency. Note that below 40 GHz a particular behavior is observed for the S-Parameters, this is due to the introduction of the OBT circuitry, discussed later in Chapter IV.

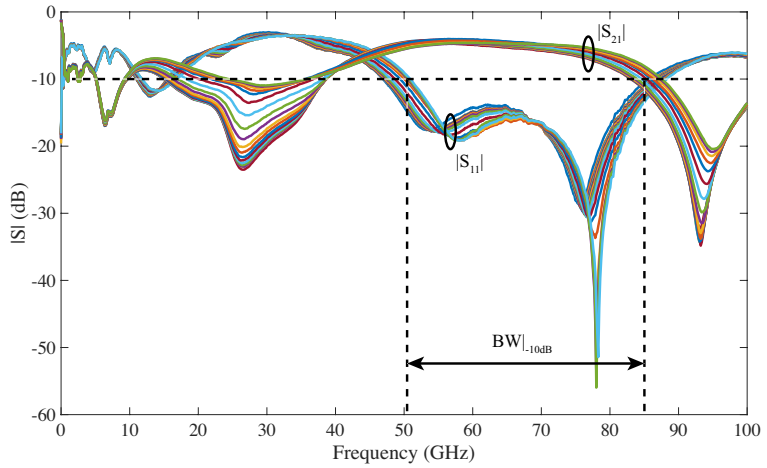

Figure III-16 Measured S-Parameter magnitude of the 60-GHz RTPS in the 1-100 GHz frequency band when $V_{ref} = 1.2$ V and $V_{ctrl} = [0, 1.9]$ V.

Figure III-17 displays the phase shift of the 60-GHz RTPS in the 1-100 GHz frequency band when $V_{ref} = 1.2$ V and $V_{ctrl} = [0, 1.9]$ V. Again, for frequencies below 40 GHz, the phase shift shows an erratic behavior due to the OBT circuitry. Note that this is not an important issue as this is observed well below the operating band of the system.

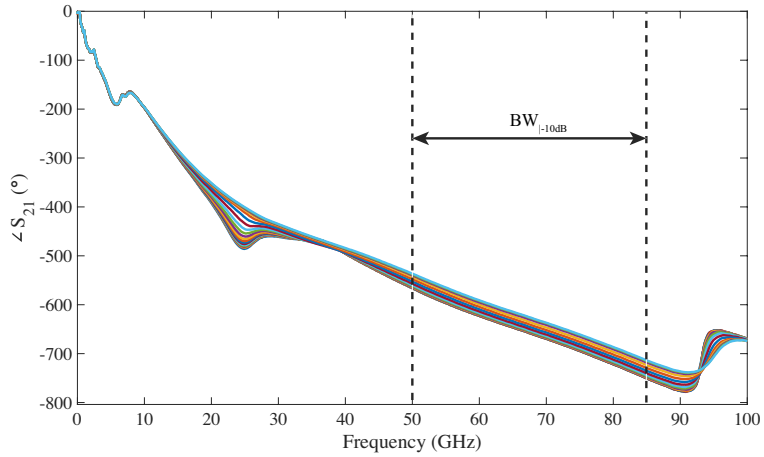

Figure III-17 Measured phase shift of the 60-GHz RTPS in the 1-100 GHz frequency band when $V_{ref} = 1.2$ V and $V_{ctrl} = [0, 1.9]$ V.

Finally, Figure III-18 presents the maximum achievable phase shift, $\Delta\angle S_{21}$, within the considered bandwidth. At 50 GHz, the system shows a $\Delta\angle S_{21}$ of 30º while at 80 GHz, the system achieves a $\Delta\angle S_{21}$ of 35º.

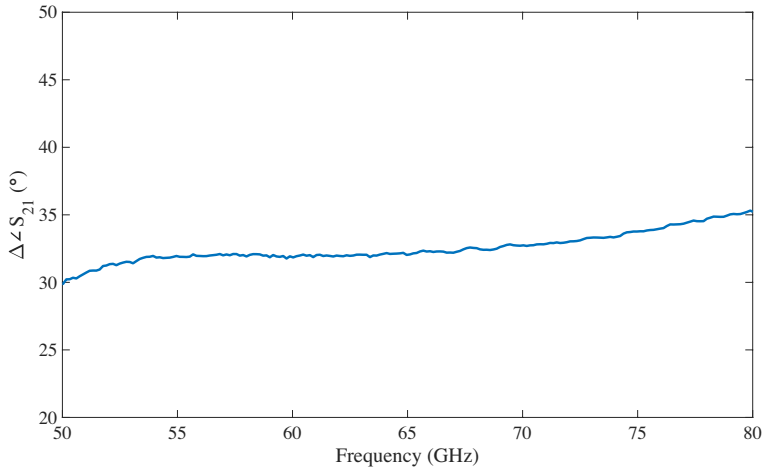

Figure III-18 Measured $\Delta\angle S_{21}$ of the 60-GHz RTPS in the 50-80 GHz frequency band when $V_{ref} = 1.2$ V and $V_{ctrl} = [0, 1.9]$ V.

To summarize, in this section, the design and measurement of a 60-GHz RTPs was presented. Results show a system with a 58% relative bandwidth, with a limited magnitude imbalance of 0.9 dB. At 60 GHz, the system presents 32º of phase shift and maximal losses of 4.9 dB, leading to a FoM of around 7 °/dB. This work shows very similar results to those obtained in [69], which was integrated using a similar topology in the same technology. Note that a slight improvement in the $\Delta\angle S_{21}$ and in the FoM is expected when the full biasing voltage range is considered.

III.3.2. 120-GHz RTPS with I-MOS varactors

An additional RTPS system was designed using the I-MOS architecture presented in Chapter II and the 120-GHz 3-dB coupler presented in Chapter I. Figure III-19 displays the block representation of the 120-GHz RTPS with I-MOS varactors.

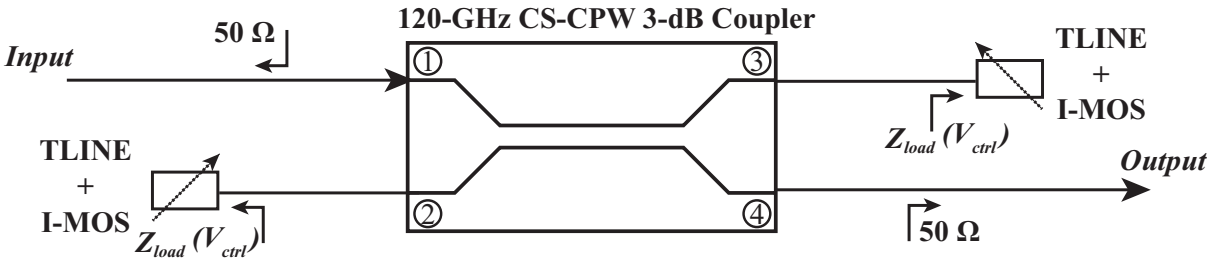

Figure III-19 Block representation of the 120-GHz RTPS with I-MOS varactors.

Figure III-20 presents a micrograph of the fabricated 120-GHz RTPS with the I-MOS loads. Note that the reflective loads placed at ports 2 and 3 of the coupler are composed of the I-MOS varactor presented in Section II connected in a series configuration with a microstrip line, similar to the 60-GHz RTPS previously presented in the previous section. The system was optimized to present a large phase shift variation, leading to a microstrip line with a length of 150 µm and a width of 1.8 µm. This leads to a characteristic impedance of 75 Ω, and at 120 GHz, an electrical length of 45º, respectively. Note that the microstrip line was bent, in a u-shape, leading to a more reduced footprint of only 0.065 mm^2.

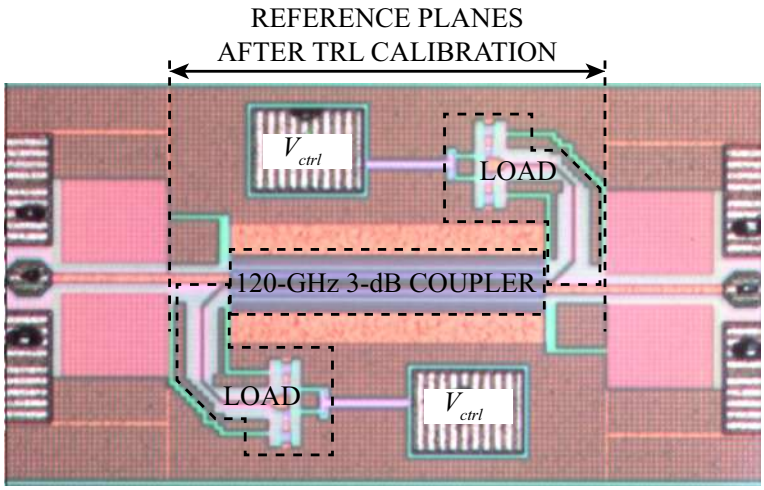

Figure III-20 Micrograph of the fabricated 120-GHz RTPS with I-MOS varactors.

III.3.2.1. Measurement results

The 120-GHz RTPS with I-MOS varactors was characterized from 1 GHz to 220 GHz. Two different VNAs were used for this purpose: (i) an Anritsu VectorStar ME7838A4, from 1 GHz to 145 GHz, and (ii) an Oleson extender associated to a R&S VNA, from 140 to 220 GHz[2]. A first-tier LRRM calibration was performed in both cases using commercial calibration substrates. Then, a second-tier TRL calibration was performed setting the reference planes at the input of the DUT, as shown in Figure III-20. Two Line standards were used for the TRL calibration, a 50-Ω Line standard with an offset length (as compared to the Thru standard) of 350 µm was used for the 1 to 140 GHz band. This Line shows an electrical length of 0.8º at 1 GHz and 109º at 140 GHz. A second 50-Ω Line standard was used in the 140 to 220 GHz band with an offset length of 170 µm, which represents an electrical length of 53º at 140 GHz and 83º at 220 GHz. In this configuration, calibration can be considered as accurate above around 10 GHz.

First, let us analyze the behavior of $|S_{21}|$ and $\angle S_{21}$ at 120 GHz, shown in Figure III-21. At this frequency, the measured insertion loss ranges between 3.3 dB and 12.7 dB, while the maximal phase shift is 91º, resulting in a FoM of 7.2 º/dB. At the same frequency, post-layout simulation reports a

[2] Authors would like to thank Sylvie Lepilliet and Christophe Gaquière, from the IEMN laboratory in Lille, for their time and support in the measurements throughout the 140 to 220 GHz band.

phase shift of 110º and an insertion loss ranging between 3.8 and 4.3 dB, which led to a FoM of around 26 º/dB.

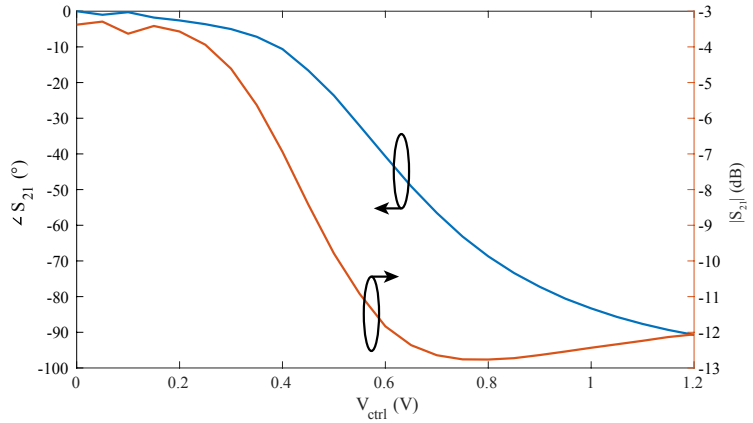

Figure III-21 Measured responses of the normalized $\angle S_{21}$ and $|S_{21}|$ at 120 GHz as a function of V_{ctrl}.

Figure III-22 presents the measurement results of the RTPS from 1GHz to 220 GHz, for $V_{ctrl} = [0, 1.2]$ V. If the bandwidth is defined for those frequencies were the return loss is greater than 10 dB, the system shows a very wide bandwidth of 115 GHz, from 45 GHz to 160 GHz. Hence, the system presents a relative bandwidth of nearly 96%. On the other hand, note that the insertion loss is very high for certain values of V_{ctrl}, strongly disagreeing with post-layout simulations. In the considered bandwidth, the system shows a maximal and minimal insertion loss of 17 and 1.7 dB, respectively. In its turn, post-layout simulation shows a similar bandwidth and behavior of $|S_{11}|$, whereas insertion loss is comprised within the 2.3 to 4.6 dB range. Disagreement between post-layout simulation and measurement was expectable since, as explained in Chapter II, the PDK simulation and the measurement results also diverged for the I-MOS architecture.

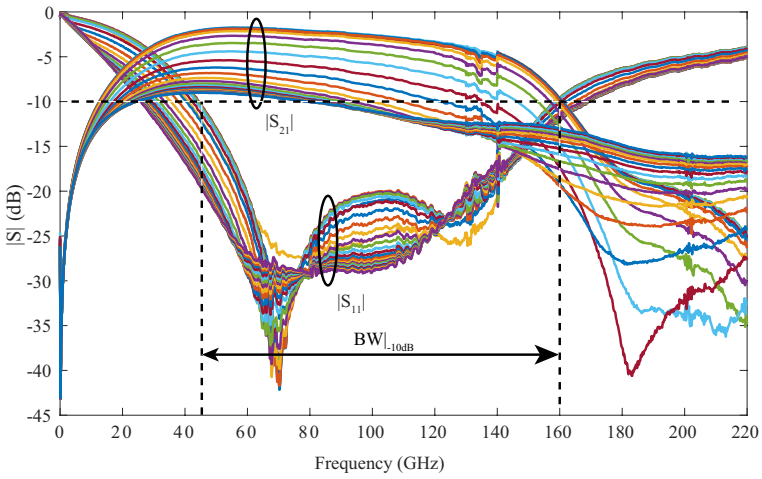

Figure III-22 Measured S-Parameter magnitude of the RTPS loaded by I-MOS varactors for different values of V_{ctrl}.

On the other hand, Figure III-23 shows the phase shift throughout the considered frequency band for different values of V_{ctrl}. Through the considered bandwidth, the system shows a phase shift comprised in the 55º to 115º range. Post-layout simulation reports a phase shift ranging between 75º and 130º, in the same frequency band. Hence, here again limited agreement is reached between these two datasets.

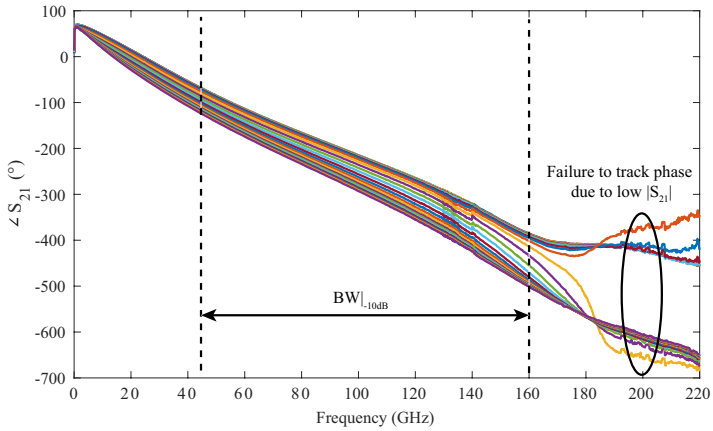

Figure III-23 Measured phase shift of the RTPS loaded by I-MOS varactors for different values of V_{ctrl}.

Finally, Figure III-24 shows the measured $\Delta\angle S_{21}$ in the 45-160 GHz band. Note that its response follows a quite linear relationship with the frequency. This can easily be explained due to the fact that the microstrip line placed at the load input is electrically long. Hence, leading to dispersion in $\Delta\angle S_{21}$ throughout the considered frequency band.

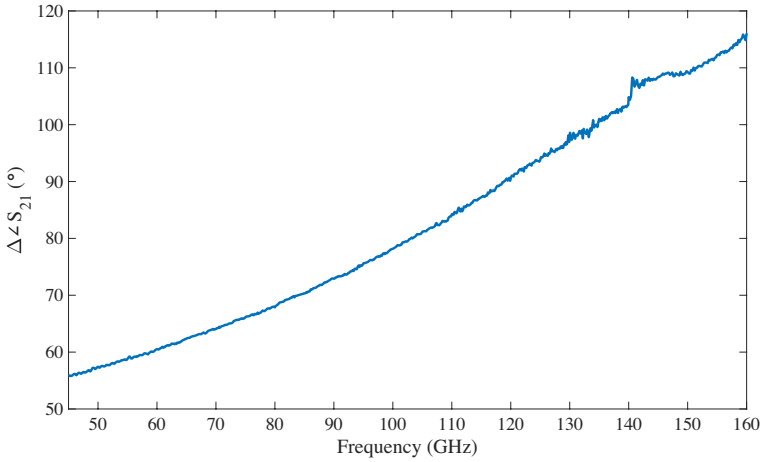

Figure III-24 Measured $\Delta\angle S_{21}$ of the 120-GHz RTPS in the 45-160 GHz frequency band.

In the next paragraphs, an accurate analysis of the system losses is carried out. Then, the utility of C_{max}/C_{min} and varactor Q-factor as figures-of-merit for varactors in the context of an RTPS is discussed and alternative $FoMs$ are proposed.

Note that the used coupler, whose measurements were discussed in Chapter I, is quite close to an ideal coupler. Hence, the equations presented in section III.1 can be applied without loss of generality. Equation (III-19) shows that for an ideal coupler, the behavior of S_{21} is solely dictated by the reflection coefficient. Thus, most of the losses of the system come from the load. To prove this, let us consider the I-MOS measurements presented in chapter II in a series configuration with a PDK microstrip line with a width and length of 1.8 µm and 150 µm, mimicking the load of the RTPS presented hereby.

Electrical simulation allowed to extract the fundamental parameters of the considered transmission line (i.e., complex propagation γ and characteristic impedance Z_C). Next, the simulated behavior of the microstrip line was combined with the measured behavior of the I-MOS varactor using the well-known formula of a lossy transmission line terminated by a load Z_L (i.e., the I-MOS varactor in this case):

$$Z_{load} = Z_C \frac{Z_L + Z_C \tanh(\gamma \cdot l)}{Z_C + Z_L \tanh(\gamma \cdot l)} \quad \text{(III-29)}$$

where l represents the length of the considered transmission line (i.e., 150 µm in this case) and Z_{load} represents the input impedance seen at the input of the transmission line terminated by Z_L. Then, the reflection coefficient, Γ (S_{load}), at the input of the load can be calculated as:

$$\Gamma = S_{load} = \frac{Z_{load} - Z_{coupler}}{Z_{load} + Z_{coupler}} \quad \text{(III-30)}$$

where $Z_{coupler}$ represents the characteristic impedance of the coupler. In our case, as shown in Chapter I, the coupler shows very low return loss throughout a wideband. Hence, $Z_{coupler}$ can be considered to be equal to the reference impedance (i.e., 50 Ω).

Using the above considerations, Figure III-25 plots the measured phase and magnitude of the reflection coefficient at the interface between the coupler and the load S_{load} at 120 GHz. In this graph, the phase presents a variation of 95º, very close to the 91º phase shit measured for the RTPS. In its turn, the magnitude of S_{11} is comprised between 2.6 and 9.5 dB, close to the insertion loss presented by the RTPS, which is comprised between 3.3 and 12.7 dB. Hence, the quasi-totality of the RTPS losses can be explained by the low magnitude of Γ.

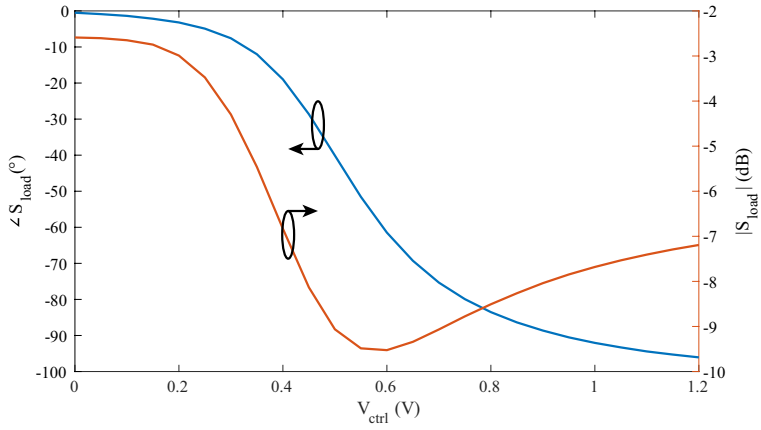

Figure III-25 Measured magnitude and normalized phase of S_{load} at 120 GHz as a function of V_{ctrl}.

Figure III-26 shows the Smith-chart representation of the measured S_{load} at 100, 120 and 140 GHz, showing that the magnitude and phase shift variation as a function of V_{ctrl} remain relatively stable throughout a wide frequency band. Hence, great insertion loss is expected over a wideband, as shown by the measurements.

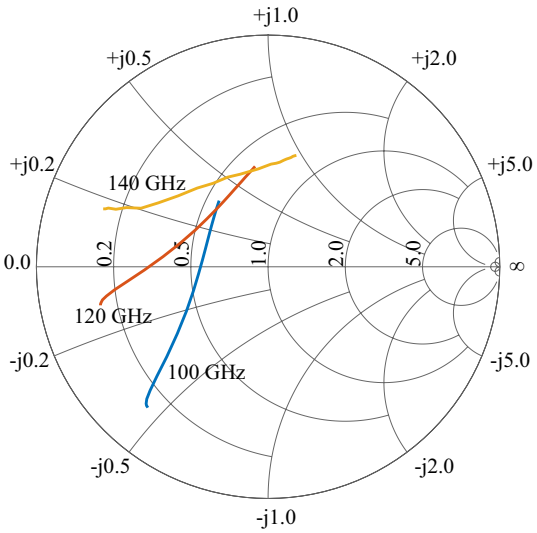

Figure III-26 Smith-chart representation of the measured S_{load} at 100, 120 and 140 GHz.

III.3.2.2. Discussion on the FoM metrics for RTPS

It is obvious that here, the insufficient model accuracy led to the choice of a non-optimal I-MOS geometry that, in its turn, led to these poor results. However, reader might find counterintuitive the fact that both, coupler and varactor show good performance, while yielding a very lossy RTPS. For instance, the considered I-MOS presents a measured maximum Q-factor of 7, as shown in Chapter II, much higher than the one shown by the A-MOS used to implement the 60-GHz RTPS. In addition, the coupler used hereby presents greater performance than the one used for the 60-GHz RTPS.

Thanks to the analysis carried out above, it was shown that most of the system losses were attributable to the varactor. In order to better understand how a higher Q-factor varactor can lead to greater losses as compared to one with a lower Q-factor, let us analyze the Q-factor expression of a passive device presenting an input impedance equal to Z_{load}:

$$Q = \frac{\Im(Z_{load})}{\Re(Z_{load})}, \tag{III-31}$$

Note that in the expression above, only the impedance of the varactor itself intervenes. However, S_{21} in an ideal RTPS is a function of Γ, which relates Z_{load} and the coupler characteristic impedance, Z_0, as shown in (III-4). Hence, it is straightforward to notice that the Q-factor in (III-31) is not a suitable figure-of-merit for varactors in an RTPS system, since S_{21} depends on the difference between Z_{load} and Z_0, not only the Q-factor calculated from Z_{load}. In the worst case, if $Z_{load} = Z_0$, then $S_{21} = 0$, i.e., infinite insertion loss.

To better illustrate this fact, let us consider two lossy RTPS loads, which can be represented using a simple RC circuit in a series configuration. Each of the loads presents a tuning ratio C_{max}/C_{min} of 2. The first load presents an equivalent capacitance ranging between 10 and 20 fF, while the second load presents an equivalent capacitance in the 20 to 40 fF range. The first load presents an equivalent resistance of 5 Ω, while the second load presents an equivalent resistance of 2.5 Ω.

If the Q-factor of these loads is analyzed as in (III-31), both loads appear to be equivalent in terms of Q-factor. However, let us consider the reflection coefficient, Γ, of these loads at the arbitrary frequency of 200 GHz when connected to a 50-Ω load. Figure III-27 shows the phase of Γ at 200 GHz as a function of the normalized capacitance, for the considered loads. Note that the first load, presents a phase variation of 38º, while the second load presents a phase variation of 33º. Hence, even though both loads present the same tuning ratio, different ∠Γ are obtained.

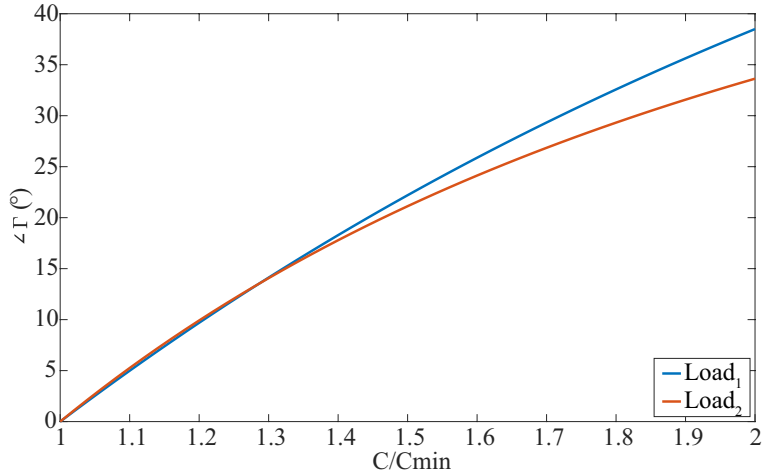

Figure III-27 Normalized phase of Γ at 200 GHz as a function of the normalized capacitance.

Next, let us carry out a similar analysis for the magnitude of Γ. The results of this analysis are depicted in Figure III-28. Again, even though both loads show an equivalent Q-factor, their reflection coefficients differ.

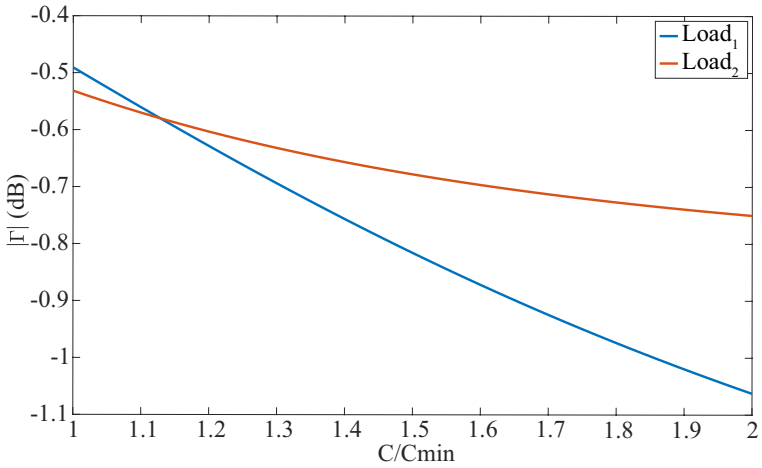

Figure III-28 Magnitude of Γ at 200 GHz as a function of the normalized capacitance.

Under these considerations it is clear that, even though the Q-factor and the tuning ratio of varactors is a good metric to reveal the intrinsic performance of varactors, it is not well-suited for its direct use in the RTPS design. As Γ, which ultimately defines the insertion loss of an RTPS, is a *relative* metric (i.e., relates Z_0 and Z_{load}), the Q-factor and tuning ratio of varactors must not be used directly as a figure-of-merit since they only describe the performance of the varactor as compared to itself.

Indeed, varactors are always reported by their tuning ratio and Q-factor in the literature, which are the most suited metrics to describe its intrinsic performance. In this scenario, the designer can use Q-factor and tuning ratio as metrics to choose among different varactor architectures. However, the sizing of the varactor must be done regarding Γ.

For this reason, a new figure-of-merit for the comparison of varactors in an RTPS architecture is proposed hereby:

$$FoM_{load} = \frac{(\angle\Gamma_{\max} - \angle\Gamma_{\min})\ [^\circ]}{|\Gamma_{\min}|\ [dB]} \tag{III-32}$$

The FoM_{load} proposed above is very similar to the FoM of a phase shifter given in (III-24). Actually, for an RTPS integrated using an ideal 3-dB coupler, (III-32) is equal to (III-24). Hence, the FoM_{load} in (III-32) can help to rapidly optimize the load of an RTPS system.

To summarize, in this section, a 120-GHz RTPS with I-MOS varactors was presented. Even though great discrepancy exists between simulation-based results and measurement-based results due to the divergence between PDK models of the I-MOS varactor and its measurements, the performance of the architecture could be easily enhanced with improved varactor modelling. In addition, a new FoM for varactors in an RTPS is proposed to better evaluate their performance in such a system.

III.3.3. 120-GHz RTPS with CS-MOS varactors

A third RTPS was integrated using the 120-GHz coupler presented in Section I. However, in this case the CS-MOS varactor architecture presented in Section II was used for the design of the load in Figure III-19. The architecture used as a load is depicted in Figure III-29.

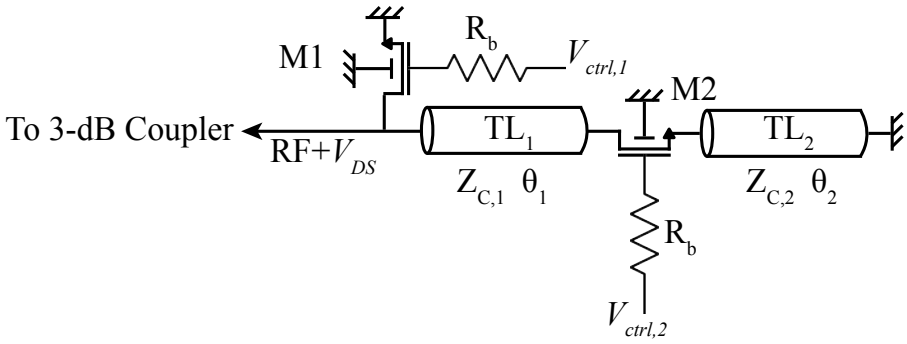

Figure III-29 Load architecture using CS-MOS varactors.

This load architecture used two n-MOS transistors, $M1$ and $M2$, operating as CS-MOS varactors, together with two microstrip lines, TL_1 and TL_2. Note that $M2$ is not in a common-source configuration from an RF point of view. However, even though presenting a source degeneration with TL_2, its source is grounded at DC level. Each of the varactors is controlled using an independent control voltage, $V_{ctrl,1}$ and $V_{ctrl,2}$, applied through a large-value biasing resistance R_b. Additionally, a DC-voltage, V_{DS}, is applied at drain-level of both transistors. As it will be discussed in the following paragraphs, due to the complexity of the load with two control voltages, many phase shift values can be obtained through several $V_{ctrl,1}$ and $V_{ctrl,2}$. Hence, the system can be optimized for certain performance goals. In the case considered herein, the system will be optimized to present reduced losses. However, other specification goals could be envisioned (e.g., minimum magnitude imbalance or return loss).

The load was optimized for the RTPS to present a phase shift as high as 360º with minimum insertion loss. This was achieved with a geometry for $M1$ of 9 µm of length and 15.3 µm of width, split into two fingers. The optimization process led to a geometry of $M2$ of 9 µm of length, and 9.9 µm of width, split into five fingers. The biasing resistors R_b were designed using the high-resistivity polysilicon layer with a length of 27 µm and a width of 0.9 µm, leading to a resistance of 190 kΩ. Finally, the length and width of TL_1 (TL_2) were optimized to 135 (99) and 0.54 (16.2) µm, respectively. This geometry led to a footprint of 0.1 mm^2. A micrograph of the fabricated device is shown in Figure III-30.

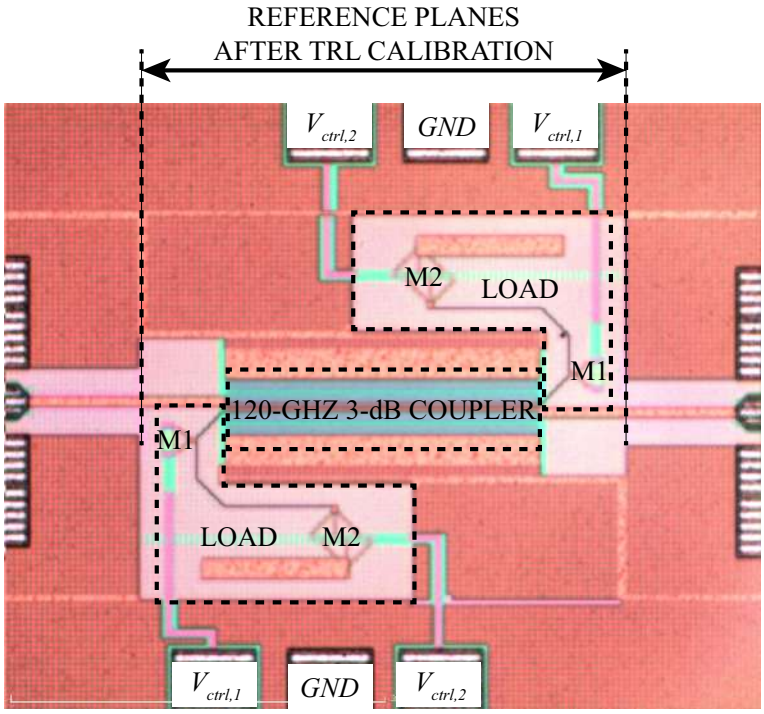

Figure III-30 Micrograph of the 120-GHz RTPS with CS-MOS loads.

III.3.3.1. Simulation results

The proposed RTPS was fabricated in the STM 55-nm BiCMOS technology. However, measurements could not be carried out yet. Hence, only simulation-based results are presented in this manuscript. The V_{DS} voltage was set to 0.4 V and the control voltages $V_{ctrl,1}$ and $V_{ctrl,2}$ were varied between 0 and 1.2 V in steps of 10 mV. Under these biasing conditions, the system shows a maximum DC-power consumption of 0.2 µW, which can be considered as negligible.

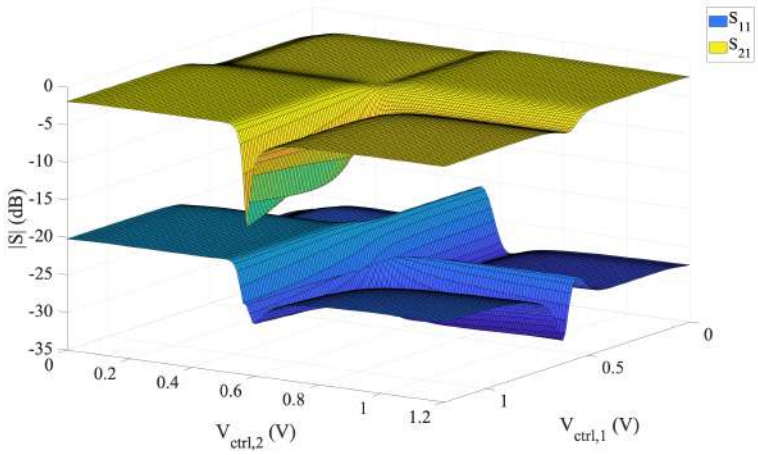

Figure III-31 S-Parameters magnitude at 120 GHz as a function of $V_{ctrl,1}$ and $V_{ctrl,2}$.

Figure III-31 presents the simulated S-Parameters magnitude at 120 GHz. At this frequency, insertion loss of the RTPS is comprised between 1.7 and 15.4 dB, depending on the way that is used, i.e., the combination of $V_{ctrl,1}$ and $V_{ctrl,2}$. On the other hand, the return loss is comprised between 20 and 32 dB. Note that the return loss is very low in any case. This can be easily explained by the good performance of the coupler. As shown in Figure III-2, an RTPS integrated using an ideal coupler presents perfect matching at its central frequency regardless of the load used.

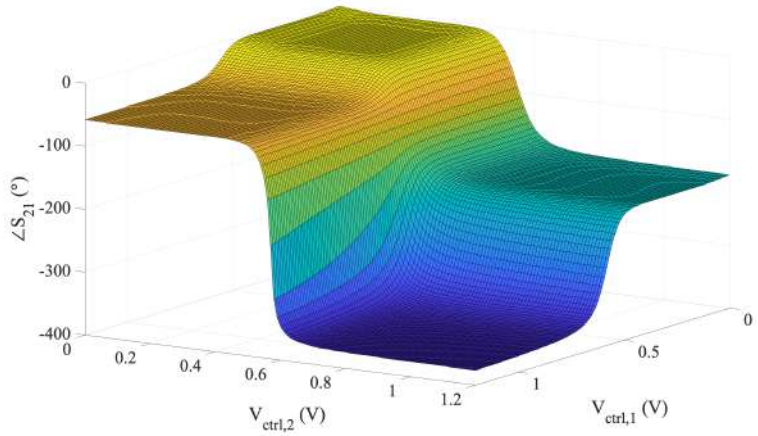

Figure III-32 Normalized phase shift at 120 GHz as a function of $V_{ctrl,1}$ and $V_{ctrl,2}$.

Next, Figure III-32 presents the normalized phase shift at 120 GHz as a function of $V_{ctrl,1}$ and $V_{ctrl,2}$. At this frequency, the system presents a maximum phase shift of 376º, leading to a FoM of 24 º/dB.

As discussed before, same phase shift values can be achieved through different combinations of $V_{ctrl,1}$ and $V_{ctrl,2}$. In this scenario, the designer can set a certain resolution for the system considering the needs of the application where the RTPS is used in. Next, certain goals for the S-Parameters magnitude can be chosen. For instance, minimum insertion loss, minimum magnitude imbalance, or minimum return loss can be envisioned. In this work, as introduced above, minimum insertion loss was chosen as the optimization criterion. Subsequently, the $V_{ctrl,1}$ and $V_{ctrl,2}$ combinations that lead to the

best results according to the chosen optimization criterion can be chosen and their values saved in a lookup table. A resolution of 1° was also considered. This resolution together with the minimum insertion loss criterion led to the results shown in Figure III-33, which displays the S-Parameters magnitude and phase shift as a function of the lookup table state, at 120 GHz.

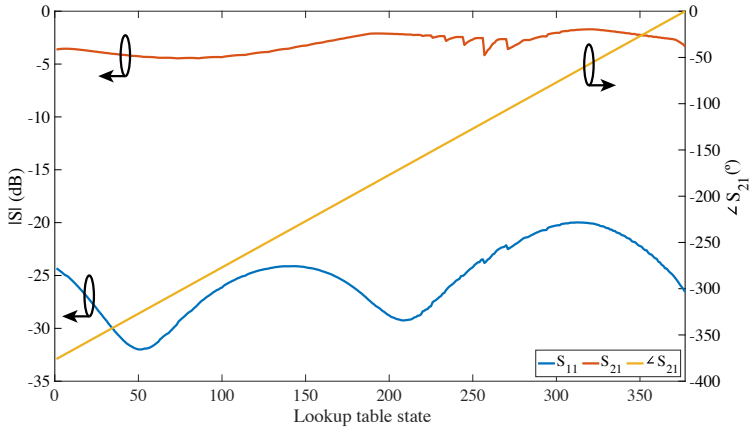

Figure III-33 S-Parameter magnitude and phase shift as a function of the lookup table state.

The optimized insertion loss is comprised between 1.7 and 4.5 dB. On the other hand, the optimization process led to a return loss comprised between 20 and 32 dB, as for the non-optimized results. Hence, through the optimization process, an improvement of the FoM is achieved. In this case, the FoM is of 84 °/dB. Hence, an improvement by 3.5 times is achieved, as compared to the non-optimized scenario. Note that an increase of the resolution might require a decrease of the control voltages step size (i.e., 10 mV were considered in this case) and might lead to a lower FoM. On the other hand, a decrease of the resolution might lead to improved performance and an eventual increase of the step size. In this work, a step of 10 mV was chosen as it can easily be implemented using on-chip digital circuitry while providing a high resolution (i.e., 1°).

Next, Figure III-34 presents the S_{11} magnitude in the 1-220 GHz band for the considered $V_{ctrl,1}$ and $V_{ctrl,2}$ combinations. On the other hand, Figure III-35 displays the S_{21} magnitude in the 1-220 GHz band for the considered $V_{ctrl,1}$ and $V_{ctrl,2}$ combinations. First, note that a similar behavior of the return loss is observed, as compared to the 120-GHz RTPS with I-MOS varactors, with a large bandwidth. This was expected as the same coupler was used in both circuits.

Note that several insertion loss maxima are observed throughout the considered frequency band, for different $V_{ctrl,1}$ and $V_{ctrl,2}$ combinations. Hence, the optimum values for the minimum insertion loss criterion yield an optimized behavior over a narrow band. For instance, the combination of these biasing voltages that led to an optimized system at 120 GHz, may lead to greater losses when moving away from this frequency. However, if the RTPS is designed to be integrated within a large-band system, several lookup tables can be built for different working frequencies.

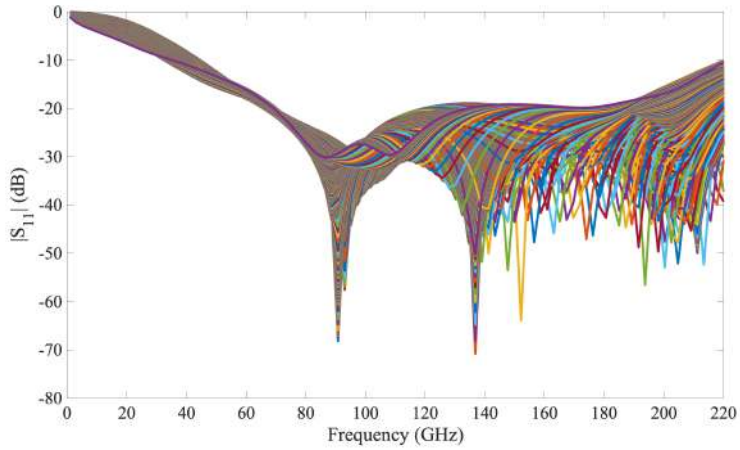

Figure III-34 Simulated S_{11} magnitude of the CS-MOS-loaded 120-GHz RTPS in the 1 GHz-220 GHz frequency band as a function of the $V_{ctrl,1}$ and $V_{ctrl,2}$ voltages.

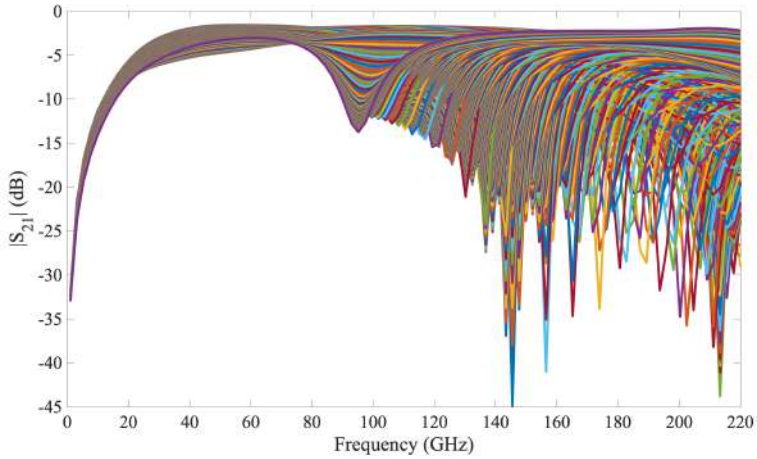

Figure III-35 Simulated S_{21} magnitude of the CS-MOS-loaded 120-GHz RTPS in the 1 GHz-220 GHz frequency band as a function of the $V_{ctrl,1}$ and $V_{ctrl,2}$ voltages.

Finally, Figure III-36 presents the simulated phase shift in the 1-220 GHz frequency band for different combinations of $V_{ctrl,1}$ and $V_{ctrl,2}$. The phase shift variation is higher than 360° from 120 GHz to 220 GHz. Above around 140 GHz, some issues with the phase correction are observed. Note that this is merely a numerical issue leading to $+\pi$ discontinuities.

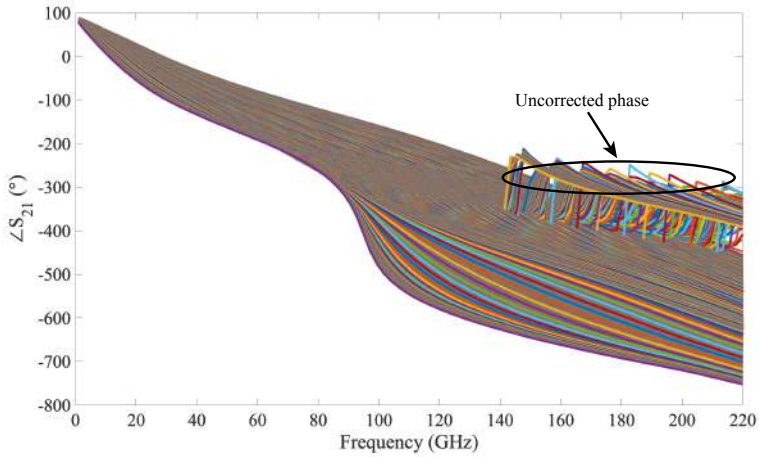

Figure III-36 Simulated phase shift of the CS-MOS-loaded 120-GHz RTPS in the 1-220 GHz frequency band as a function of some $V_{ctrl,1}$ and $V_{ctrl,2}$ voltages.

To summarize, in this section a 120-GHz RTPS was presented. Prior to optimization, the system shows a FoM of 24 °/dB. However, thanks to the approach using two independently controlled CS-MOS varactors an optimization process led to an improved FoM of 84 °/dB. As introduced in the previous chapter, the CS-MOS measured behavior differs from the PDK predicted performance for this device. Hence, a different performance may be expected from the actual measured RTPS. However, these simulation results are encouraging enough to consider the proposed architecture as a viable solution for the implementation of advanced integrated RTPS.

III.4. State-of-the-art comparison

To put the presented results into perspective let us compare the considered RTPS architectures with the current literature. For this purpose, let us consider the state-of-the-art RTPS presented in Table III-I together with the RTPS discussed in this chapter. These results are summarized in Table III-III.

TABLE III-III COMPARISON WITH STATE-OF-THE-ART MM-WAVE ON-SILICON RTPS

Ref.	Technology	Frequency (GHz)	RBW† (%)	$\Delta\varphi$/resolution (°)	$\lvert S_{21}\rvert$ (dB)	RL (dB)	FoM* (°/dB)	Area (mm^2)	Power consuption (mW)
[69]	55-nm BiCMOS	30-50	50	60/cont.	2.8-5	>10	12	0.18	0
[70]	65-nm CMOS	26-30	14‡	360/11.25	6.8-9.2	>5	45	0.16	0
[71]	65-nm CMOS	54-66	20**	90/11.25	5.7-7.9	>12	11	0.034	0
[72]	45-nm SOI CMOS	28-29	3.5	340/2.8	2-20	>7	20	0.18	-
[73]	65-nm CMOS	26-32	17#	379/cont.	7-11	>15	41	0.076	0
[74]	90-nm CMOS	57-64	11#	190/cont.	6-11	>15	18	0.027	0
[75]	130-nm BiCMOS	59-62	5	367/cont.	9.2-10.3	>10	35.6	0.16	0
This work	**55-nm BiCMOS**	**50-85**	**58**	**32/cont.**	**4.1-4.9**	**>10**	**7**	**0.19**	**0**
This work	**55-nm BiCMOS**	**45-160**	**96**	**92/cont.**	**3.3-12.7**	**>10**	**7**	**0.065**	**0**

†For RL > 10 dB *At the central frequency ‡For RL > 5 dB **For RL > 12 dB #For RL > 15 dB

First, note that the presented RTPS show the widest Relative BandWidth (RBW) among all the considered works. This is achieved thanks to the high-performance CS-CPW-based 3-dB couplers used for their design. This is especially remarkable for both of the 120-GHz RTPS discussed in this chapter. Additionally, even though the use of CS-CPW yields wide couplers, the longitudinal miniaturization achieved thanks to the slow-wave effect leads to footprints that are comparable with all the considered counterparts.

The 60-GHz RTPS presents the lowest insertion loss variation. However, the relatively low quality of the used 3-dB coupler led to a quite reduced FoM. The performance of this RTPS could be

easily improved through the use of a higher-quality 3-dB coupler, which could be designed using the methodology described in Chapter I.

The 120-GHz RTPS with I-MOS varactors presents a much greater phase shift with a quite reduced footprint. However, due to the I-MOS model inaccuracy, the insertion loss reaches very large values, decreasing its FoM. Even though the I-MOS architecture can lead to quite large varactor Q-factor, as shown in Chapter II, Γ must be correctly optimized to reduce the RTPS insertion loss. For sure, correct modelling of the I-MOS varactor and optimization of the load topology, including the transmission line optimization, could lead to a great performance RTPS.

Finally, the 120-GHz RTPS using CS-MOS loads presents 371º of maximum phase shift, a moderate magnitude imbalance and a very promising FoM. This performance is achieved with a reduced area overhead of 0.1 mm^2. Note that both 120-GHz RTPS share the same high-performance coupler, leading to very large RBW. Even though very few applications require such bandwidths, this is still an interesting feature as it allows to reuse the same device for applications working at different frequencies. Nevertheless, this architecture has not been added to Table III-III because it relies on simulations while the rest of the considered RTPS were measured.

III.5. Conclusions

In this chapter the theory, current state-of-the-art and practical implementations of mm-waves on-silicon RTPS was discussed. In the first section of this chapter, the fundamental theory is exposed, and the behavioral equations derived. In addition, the behavior of RTPS throughout the frequency spectrum is analyzed.

Then, section III.2 presents the current state-of-the-art on-silicon mm-wave RTPS. Several works concerning this topics have been reported in the literature. However, the reader may note that there have been major advancements in the field during the recent years. This denotes the current interest of the RF community in such devices development. Moreover, many of the high-performance RTPS discussed in this section have different design approaches (e.g., discrete or continuous tuning, single varactor loads versus complex multi-element loads, active or passive loads, distributed or lumped-elements couplers …). Hence, showing that this is an open research field where consensus over the best design approach has not been reached.

In this scenario, three different RTPSs were designed and measured. Their architecture and measurement results were discussed in section 3. All of the presented RTPS in this section were designed with a high degree of innovation. For instance, the 60-GHz RTPS includes BIST circuitry to perform the so-called OBT. Next, both 120-GHz RTPS were designed using innovative varactors (i.e., I-MOS and CS-MOS). In addition, the latter were designed in, to the best of authors' knowledge, the highest frequency ever reported in on-silicon RTPS.

The 60-GHz RTPS performance is quite limited. However, the design flaws are clearly identified and design techniques are discussed in Chapters I and II of this manuscript to improve its performance. Next, the 120-GHz RTPS with I-MOS loads also presents limited performance. Again, the design flaws, which in this case are explained thanks to the PDK model maturity, are identified and design guidelines are given to improve this RTPS performance.

Finally, a 120-GHz RTPS simulated with CS-MOS varactors presents very promising results. However, only simulation-based results are presented. Note that the measurements of the CS-MOS varactor presented in Chapter II, show a great divergence, as compared to the simulation-based results. Hence, divergence between the simulated RTPS and the measured RTPS is expectable. Again, increased model maturity for this kind of applications will increase the degree of confidence regarding simulation. Nevertheless, the design could easily be adapted to other transistor geometries without loss of generality.

Chapter IV

OSCILLATION-BASED TEST FOR RTPS

Reliability has been an issue since the advent of modern electronics. Any electronic circuit is subject to aging and manufacturing imperfections (i.e., fabrication defects and process variations). Thus, test and calibration are required to identify faulty systems and eventually bring them into the required specifications. The most direct test approach is the so-called functional test, that is aimed at measuring the DUT performance. Usually, functional test in the production line relies on expensive Automated Test Equipment (ATE) that excite each Device Under Test (DUT) with an appropriate set of test sequences, acquire the test responses and compute the DUT specifications. However, as systems grow more complex and its performance increases, the test cost greatly increases requiring lengthy test procedures and expensive high-performance ATEs. For instance, the testing cost of a modern mobile phone System-on-Chip (SoC) may represent more than 50% of its overall manufacturing cost [12]. Reducing the test cost is a major issue in the semiconductor industry.

Moreover, a complete SoC transceiver is composed of several devices of very different nature (e.g., mixers, amplifiers, oscillators, power unit, digital logic…). The first limitation of direct testing within this context lays on the fact that usually there is no access from the outside to the input /ouput ports of internal building blocks, so usually only system-level measurements are possible.

In this context, Built-In Self-Test (BIST) techniques appear as a solution for these issues. BIST aims at the integration of some of the ATE test capabilities within the DUT, in such a way that the device becomes self-testable. This approach leads to a test cost reduction as the functionalities needed in the ATE can be relaxed. In a way, BIST techniques reduce test cost by taking test into account during the design stage. In an ideal scenario a dedicated BIST could be designed together with each element of the DUT in a Design-for-Test (DfT) flow, making it possible to accurately characterize their performance, without the need of an external tester. Although efficient BIST techniques have been developed for digital circuits, based on fault models and structural tests, nowadays there is no general solution for analog, mixed-signal, and RF circuits. Instead, wide variety of different BIST approaches have been presented in the last years, each solution targeting a particular circuits family.

In this Chapter, we explore the application of the so-called Oscillation-Based Test (OBT) technique as a viable possibility for the on-chip testing of mm-wave phase shifters, with particular attention to the RTPS topology. In addition to enabling the substitution of the functional test performed at the end of the production line, OBT allows in-field testing (i.e., while the DUT is in operating environment). This is an advantage when compared to classical tests at the end of the production line, as it allows to perform in-field calibration and assessment of the aging of the device. This Chapter is organized as follows: first, section 1 discusses the current approaches for testing integrated phase shifters and phased arrays. Next, section 2 presents the working principle of the Oscillation-Based Test (OBT) in the context of mm-wave RTPS. In section 3, the practical implementation and post-layout simulation results of the OBT circuitry in a 60-GHz RTPS are presented. Then, section 4 describes

measurement results of the designed RTPS with OBT circuitry. Section 5 presents a proposal for a possible extension of the proposed OBT technique in the context of a complete phased array system, where several phase shifters are present. Finally, section 6 draws the main conclusions of this Chapter.

IV.1. Test for phased arrays and phase shifters

A variety of test techniques have been proposed for the characterization of phased arrays and phase shifters. In this line, the works in [76]–[78] propose direct functional test techniques based on the excitation of the phased array with an external radiofrequency wave and the processing of the array response. The contact-less characterization procedures described in [77], [78] are not suitable for production line testing since they require manual adjustment and a long measurement time using dedicated test equipment. On the other hand, in [76] a simplification of contact-less tests allows measuring under near-field conditions, reducing this way the physical size of the test setup.

BIST strategies for phased arrays have been also proposed in [79]–[83]. In [80]–[82], a practical system-level test for phased arrays in an RF system is demonstrated: it allows characterizing and calibrating phase and amplitude inaccuracies in each individual channel of the array. The proposed test circuitry requires the integration (or re-use) of a frequency synthesizer for exciting the different channels in the array and a dedicated receiver block to extract the test information from the response signals. In the same line, the work in [79] proposes a system-level BIST and calibration circuitry for the phased array of a receiver section. BIST circuitry makes use of an LC oscillator for test stimulus generation and a simplified receiver consisting in a mixer in a homodyne configuration for test response acquisition.

The approach in [83] takes advantage of code-modulation techniques for multiplexing different test signals into orthogonal codes that are then applied to the phased array under test. An on-chip demodulator is then used to recover the test information of each individual channel.

In this Chapter, we propose to adapt the classic Oscillation-Based Test (OBT) technique to enable self-test applications for integrated mm-wave phase shifters. OBT, firstly introduced in [84] and further developed in [11-13] for the test of analog and mixed-signal circuits, consists in reconfiguring the DUT into an oscillator, in such a way that the parameters of the resulting oscillation (i.e., frequency, amplitude) are directly correlated to the DUT functionality and/or performance.

In particular, in this chapter we will explore the possibility of characterizing the phase-shift introduced by an integrated mm-wave phase-shifter by measuring its oscillation characteristics when it is reconfigured into an oscillator. Compared to the previously discussed test strategies, enabling OBT for phase shifters has a two key advantages:

1) The need of a dedicated test stimulus generator is eliminated since the DUT itself generates the test signal.

2) The interpretation of the test results is simplified since the phase shift introduced by the phase shifter is naturally encoded in the amplitude and frequency of the resulting oscillation.

IV.2. Theoretical basis

In this section, the theoretical basis of the OBT, as well as the considerations for its practical implementation within a mm-wave RTPS are discussed.

OBT was first introduced as a structural Design-for-Test (DfT) approach based on reconfiguring the DUT as an oscillator. The key idea behind OBT is that any defect in the DUT would have an impact in the frequency of the resulting oscillator. This test technique has been extended to a wide variety of analog and mixed-signal applications, including the static test of Analog-to-Digital Converters [85], testing analog integrated filters [86], testing Dual-Tone Multi-Frequency receivers [87], etc.

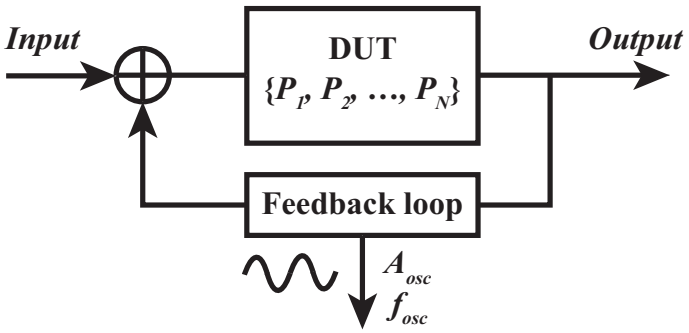

Figure IV-1 Block diagram of a DUT with dedicated circuitry (i.e., feedback loop) for OBT purposes.

Figure IV-1 displays the block diagram of a DUT with N performances $P_1, P_2, \dots, P_N$. The DUT is connected to a feedback loop that, when turned on, sets the system into an oscillatory state with an oscillation amplitude and frequency A_{osc} and f_{osc}, respectively. The key principle in this technique is that A_{osc} and f_{osc} are correlated to one or multiple DUT performances. Hence, if the correlation between a given performance, P_i, and the oscillation characteristics are known, the former can be determined with the measurement of the latter. This approach is known as predictive OBT.

Adapting the OBT principles to phase shifters requires to reconfigure the phase shifter itself into an oscillator in test mode, in such a way that any imperfection that may cause a deviation of the intended phase shift, would cause as well a deviation of the oscillation characteristics (i.e., frequency and/or amplitude).

At a given frequency, an RTPS, or any other passive electronic circuit, can be mathematically seen as an RLC network. For instance, let us consider a lossy RTPS whose phase shift is tuned by a control voltage V_{ctrl}. Such a system, introduces a phase shift φ_{RTPS}, which is a function of V_{ctrl}. At any given frequency, this system can be mathematically represented as an RLC network composed by the equivalent resistance, inductance, capacitance, R_{eq}, L_{eq} and C_{eq}, respectively. In such mathematical representation, R_{eq} accounts for the ohmic losses, and L_{eq} and C_{eq} represent the inductive and capacitive behavior of, in this case, the RTPS. The elements composing the RLC network, are in its turn tuned by the V_{ctrl} voltage. The described equivalence between a lossy RTPS and an RLC network is depicted in Figure IV-2.

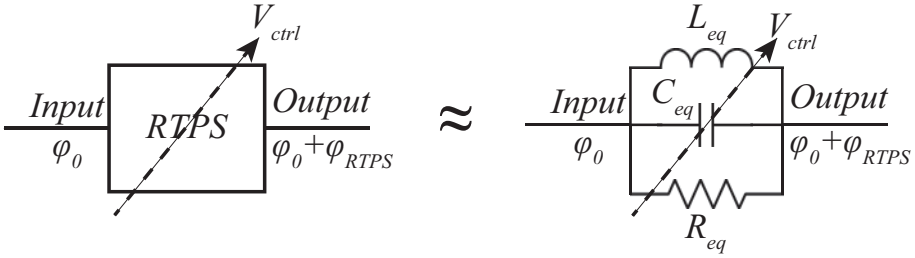

Figure IV-2 Mathematical equivalence between a lossy RTPS tuned by a control voltage (V_{ctrl}) and a variable RLC network at a given frequency.

The impedance of the RLC network, Z_{RTPS}, at a given angular frequency ω can be expressed as follows:

$$Z_{RTPS} = \frac{L_{eq}^2 \cdot R_{eq} \cdot \omega^2 + j(L_{eq} \cdot R_{eq}^2 \cdot \omega - C_{eq} \cdot L_{eq}^2 \cdot R_{eq}^2 \cdot \omega^3)}{C_{eq}^2 \cdot L_{eq}^2 \cdot R_{eq}^2 \cdot \omega^4 + \omega^2 (L_{eq}^2 - 2 \cdot C_{eq} \cdot L_{eq} \cdot R_{eq}^2) + R_{eq}} \quad \text{(IV-1)}$$

which can be simplified to

$$Z_{RTPS} = \frac{-j \cdot \omega \cdot L_{eq}}{L_{eq} \cdot C_{eq} \cdot \omega^2 - 1} \quad \text{(IV-2)}$$

when $R_{eq} \rightarrow \infty$ (i.e., lossless RTPS).

Note that an RLC network is a circuit potentially capable of sustaining oscillations if a closed loop is created to compensate the electrical losses in the network. Figure IV-3 displays the equivalent circuit of an RTPS in a closed loop configuration achieved through a feedback network, represented with a negative resistor $\mathrm{R_{neg}}$. The considered closed loop presents a total phase shift β.

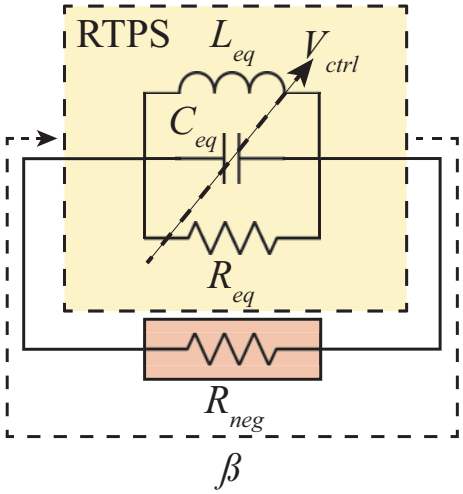

Figure IV-3 Equivalent circuit of an RTPS in a closed-loop configuration. The loop presents a phase shift of β and the feedback network modelled as a negative resistor R_{neg}.

The system depicted in Figure IV-3 will sustain oscillations if the Barkhausen's criteria [88] holds. Hence, the system will sustain oscillations when:

- The loop gain is equal to unity in absolute magnitude, i.e., $\left|R_{neg} \cdot Z(j\omega_0)^2\right| = 1$
- The phase shift around the loop is zero or an integer multiple of 2π, i.e., $\beta = \angle R_{neg} \cdot Z(j\omega_0) = 2\pi n, n = 0, 1, 2 \ldots$

where $Z(j\omega_0)$ represents the impedance of the RLC tank at the angular frequency and ω_0 represents the angular frequency at which the system oscillates

$$Z(j\omega_0) = \frac{L_{eq}^2 \cdot R \cdot \omega_0^2}{C_{eq}^2 \cdot L_{eq}^2 \cdot R_{eq}^2 \cdot \omega_0^4 + \omega_0^2 (L_{eq}^2 - 2 \cdot C_{eq} \cdot L_{eq} \cdot R_{eq}^2) + R_{eq}} \tag{IV-3}$$

and ω_0 represents the angular frequency at which the system oscillates. At ω_0, the RLC network presents a null phase shift. Hence, oscillation is achieved if the feedback loop, in its turn, introduces a null phase shift (or an integer multiple of 2π). Thus, in this scenario, the oscillation frequency F_{osc} can be expressed as:

$$F_{osc} = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{L_{eq} C_{eq}}} \tag{IV-4}$$

Knowing that the phase shift at the output of the RTPS is, by definition, a function of L_{eq} and C_{eq}, a correlation exists between phase shift and oscillation frequency, as shown in (IV-4).

Note that the Barkhausen criteria requires that the total loop phase shift is zero or an integer multiple of 2π. This criterion stablishes no relationship between the working frequency of the DUT itself and F_{osc}. Hence, F_{osc} is determined by the topology, geometry and tuning ratio of the DUT. In this scenario, the oscillation frequency is expected to be different to the working frequency of the DUT. In practice, F_{osc} can be much lower than the central frequency of the RTPS. This is a key feature of the proposed technique as it greatly facilitates its measurement.

A feedback loop presenting a null phase shift (or an integer multiple of 2π) at F_{osc} only satisfies the second Barkhausen criterion. Real mm-wave passive RTPS are lossy elements, in this scenario, a

Cross-Coupled Pair (XCP) of nMOS transistors is a perfect candidate for the implementation of a loop able to compensate the losses of the tank. The resulting system would then resemble a classical voltage-control oscillator (VCO) that employs the RTPS as resonator tank.

IV.2.1.VCO design: an overview

The performance goals in this work are different from a classical VCO. Nevertheless, the methodology and theory behind the on-chip OBT circuitry presented hereby and VCOs is very similar. In the context of OBT as a BIST tool:

- Consumption is a major concern rather than power output, especially for designs aimed at on-line (i.e., during operation) testing. Power output has only to be sufficiently large for proper frequency and amplitude readout.
- The resonant tank (i.e., DUT) is imposed. Hence, the resonant frequency is mostly given by the DUT.
- The system has to present enough frequency or amplitude variation to allow achieving a correlation between them and the DUT tunability. However, large Frequency Tuning Ratio (FTR) is not necessary.
- Phase noise is a minor issue, as long as proper readout of the resonant frequency and amplitude remains possible.

A classical VCO uses an LC tank as the resonant feedforward element in the loop and a feedback network represented by a transconductance R_{neg}, similarly to Figure IV-3. Usually, the capacitive part of the tank is integrated thanks to the use of varactors, for tunability purposes. Due to the finite Q-factor of the inductor and varactors, the LC tank suffers from energy dissipation, which are represented as a resistance in parallel to the LC tank (i.e., R_{eq} in Figure IV-3). Hence, similarly to passive RTPS, the feedback loop has to compensate the losses in the resonator and present a null phase shift (or an integer multiple of 2π).

As introduced before, a perfect candidate for this function is an XCP. Indeed, this is a widely used architecture for the design of the feedback loop of VCOs based on LC tanks [48]. The transconductance of the XCP can be mathematically approximated as a resistor with a negative value, R_{neg}, which is connected in a parallel configuration to the RLC tank.

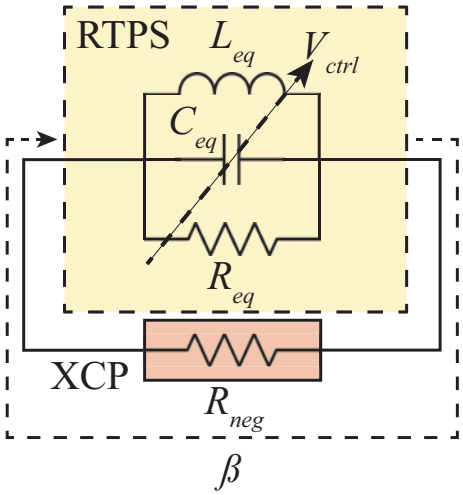

Figure IV-4 Equivalent circuit of an RTPS in a closed-loop configuration through an XCP. The cross-coupled pair is represented by an equivalent resistor R_{neg}.

In this case, at ω_0, the admittance of the closed loop at the resonance frequency can be further rewritten as:

$$Y(j\omega_0) = \frac{1}{R_{eq}} + \frac{1}{R_{neg}} = \frac{R_{eq} + R_{neg}}{R_{eq} \cdot R_{neg}}. \quad \text{(IV-5)}$$

The system presented in Figure IV-4 presents a unitary gain when $Y(j\omega_0) = 0$. This consideration leads to,

$$Y(j\omega_0) = 0 \rightarrow R_{eq} = -R_{neg}. \tag{IV-6}$$

As R_{eq} represents ohmic losses, its magnitude is greater than one. Hence, R_{neg} must present a negative R_{eq} value to achieve a unitary gain in the loop. Note that for $R_{neg} < 0$ and $|R_{neg}| < R_{eq}$ $Y(j\omega_0) < 0$, leading to, ideally, an oscillation constantly amplified in time.

Next, let us demonstrate that a cross-coupled pair behaves as a negative resistor. An XCP can be practically implemented by connecting two nMOS transistors in the configuration shown in Figure IV-5. In this representation, a current source generating an I_S current is also considered as most oscillator topologies include this function to control the current flowing in the tank and achieve steady oscillations. Then, as both transistors are biased in their saturation region by the differential voltage V_X, they can be represented as dependent current sources, as depicted in Figure IV-5. Note that here, for the sake of simplicity, the output resistance of the transistors, r_0, is not considered as its product by the transconductance g_m is considered much bigger than the unity (i.e., $g_m \cdot r_0 \gg 1$).

In the saturation region, these transistors show a transconductance g_m, which can then be mathematically approximated by a voltage-dependent current source with a value $V_{GS} \cdot g_m$, where V_{GS} is the gate to source voltage drop of each transistor. First, note that $V_{GS,1} = V_{DS,2}$ and vice versa, where V_{DS} represents the drain to source voltage drop. Thus, transistors in an XCP configuration behave as interdependent current sources. Next, let us assume that $V_S \approx 0$ V. Hence, as depicted in the mathematical simplification in Figure IV-5, the current sources take the value $\pm g_m \cdot V_X$.

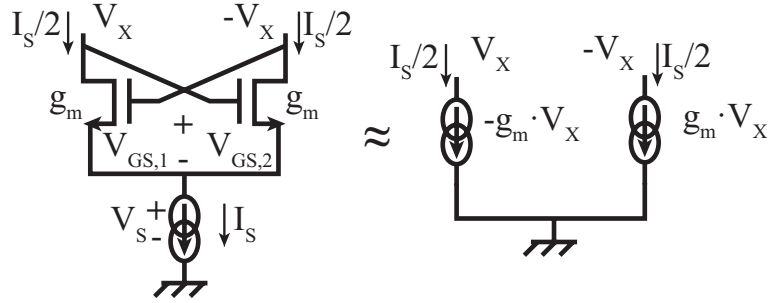

Figure IV-5 Cross-coupled pair and its simplification as a pair of dependent current sources.

Note that an XCP is a differential circuit. In this scenario, the total voltage drop (V_{XCP}) across the XCP is of $2V_X$. While the total current (I_{XCP}) through the left (right) arm is of $-g_m \cdot V_X$ ($g_m \cdot V_X$). Hence:

$$\frac{V_{XCP}}{I_{XCP}} = R_{XCP} = \frac{2 \cdot V_X}{-g_m \cdot V_X} = \frac{-2}{g_m} \tag{IV-7}$$

As g_m is the transconductance of the transistor (i.e., a positive value), the value of R_{XCP} is negative. For nomenclature consistency, in the following paragraphs $R_{XCP} = R_{neg}$.

However, the approximation carried out using Figure IV-5 neglects all parasitic effects in the transistor. In this work, as high frequencies are targeted, these effects must be accounted for. As a first approximation, the total differential capacitance, as seen from the drains of the transistors, of the XCP can be demonstrated to be under the form:

$$C_{XCP} = \frac{1}{2}C_{DB} + \frac{1}{2}C_{GS} + 2 \cdot C_{GD} \tag{IV-8}$$

Note that expression (IV-8) is not complete, as many other parasitic will impact the design of the XCP. However, it is useful to show that only the transistor parasitics are already sufficient to generate an imaginary part in the impedance of the XCP.

With these considerations the tank in Figure IV-4 can be expanded into the more accurate form shown in Figure IV-6.

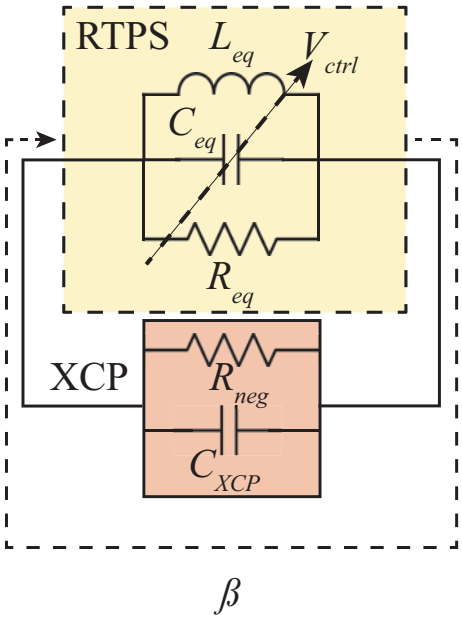

Figure IV-6 Equivalent circuit of an RTPS in a closed-loop configuration through an XCP. The cross-coupled pair is represented by an equivalent resistor R_{neg} and a capacitance C_{XCP}.

In a standard VCO, C_{XCP} has two undesired effects: (i) reduces the FTR and (ii) reduces the oscillation frequency of the system, F_{osc}. In the present system aiming at OBT, these two parameters have a relatively low importance. The reduction in the FTR is tolerable, as long as the desired sensitivity between phase shift and oscillation frequency is achieved. The second effect, is indeed beneficial in an OBT test scenario. As stated before, lower frequencies are easier to measure and thus, the constraints for the external test equipment and circuitry can be relaxed.

To summarize, in this section the correlation existing between the phase shift of an RTPS and its oscillation characteristics in an OBT environment have been demonstrated. Then the basis of the OBT circuitry design used hereby have been presented via the VCO design methodology. Even though a VCO and the OBT circuitry presented in this manuscript might share the same architecture, the design goals are different and in general, more relaxed for the OBT. The goal differences have been also discussed in this paragraph.

IV.3. Practical implementation

A demonstrator was built using the 55-nm BiCMOS technology. As a DUT, the 60-GHz RTPS presented in the previous Chapter was used. Figure IV-7 shows the schematic representation of the considered DUT and the additional circuitry added for the OBT. In the following paragraphs, the design of each colored region in Figure IV-7 will be detailed.

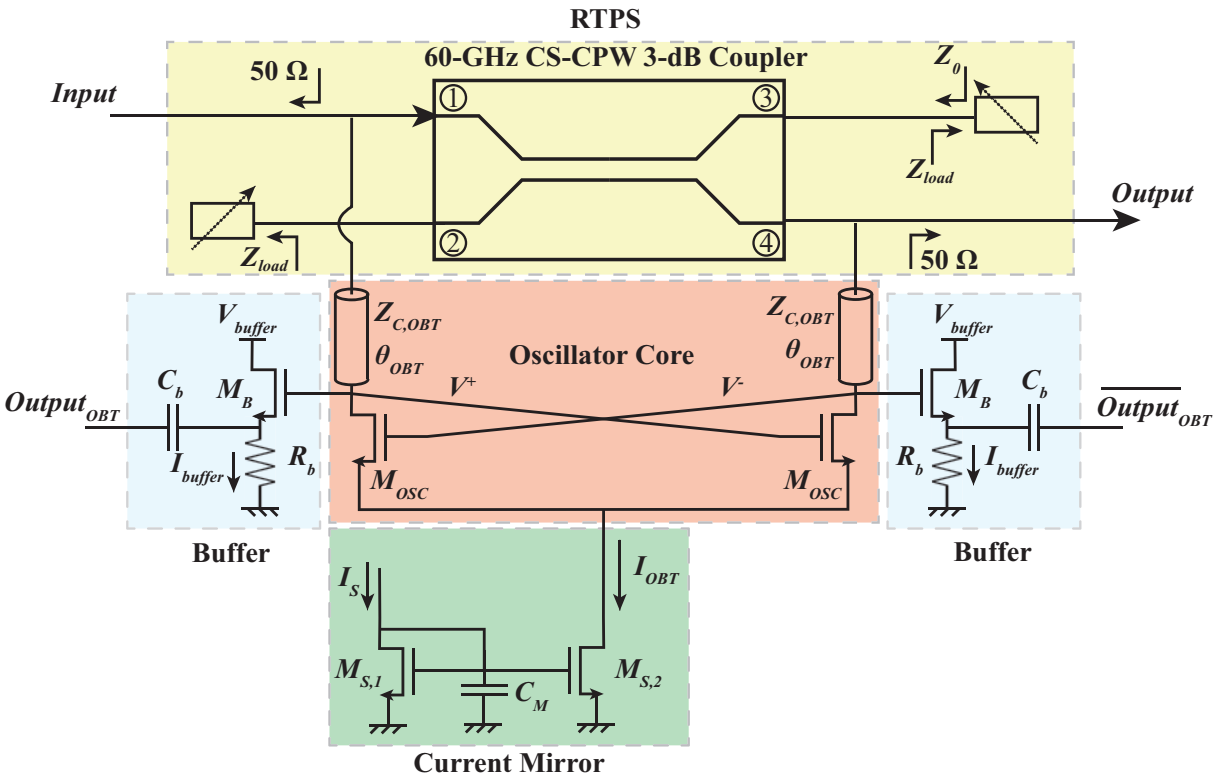

Figure IV-7 Schematic representation of the manufactured 60-GHz RTPS with OBT circuitry.

IV.3.1.RTPS as an LC-tank

The design, physical implementation and measurement results of the 60-GHz RTPS were detailed in the previous Chapter. Hence, in this chapter we only discuss its performance as a case study for the proposed OBT technique.

As explained above, the oscillation frequency in an OBT environment is mostly determined by the DUT. Hence, for the OBT as a BIST approach to be viable, the natural oscillation frequency of the DUT must fall into a frequency range at which the transistors of the used technology are capable of generating an oscillation.

First, let us analyze the frequency at which the considered 60-GHz RTPS can oscillate. Figure IV-8 displays the simulated magnitude of the imaginary part of the admittance, as a function of V_{ctrl} (i.e., the control voltage of the varactors), between the input and the output of the considered RTPS in the 1 to 60 GHz frequency band. Note that the XCP will introduce 2π radians of phase shift. Hence, oscillations might occur for the frequencies where $|\Im(Y_{eq})| = 0$, according to the Barkhausen criteria. These regions are delimited by vertical dashed lines.

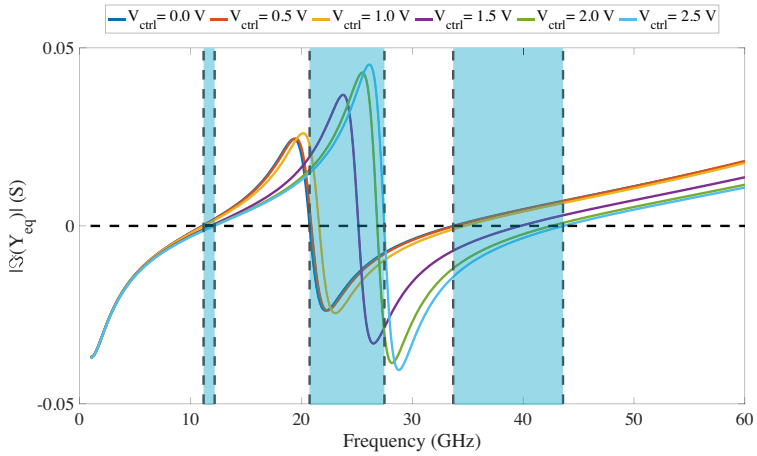

Figure IV-8 Simulated imaginary part of the RTPS admittance as a function of V_{ctrl} in the 1 to 60 GHz frequency band. Possible oscillation regions are highlighted in light blue.

In Figure IV-8 three clear regions, where $|\Im(Y_{eq})| = 0$ are observed. The first region is comprised between 11 and 12 GHz. The second region is comprised around 20 and 27 GHz. Finally, the third region is located between 34 and 44 GHz. However, this graph only provides information about the phase criterion in the Barkhausen criteria. For oscillations to occur, the equivalent resistance, R_{eq}, in these frequencies must be compensated. Again, for the OBT as a BIST approach to be viable, the regions where the technology transistors can compensate the losses must be considered, as integrated transistors do not have an infinite gain.

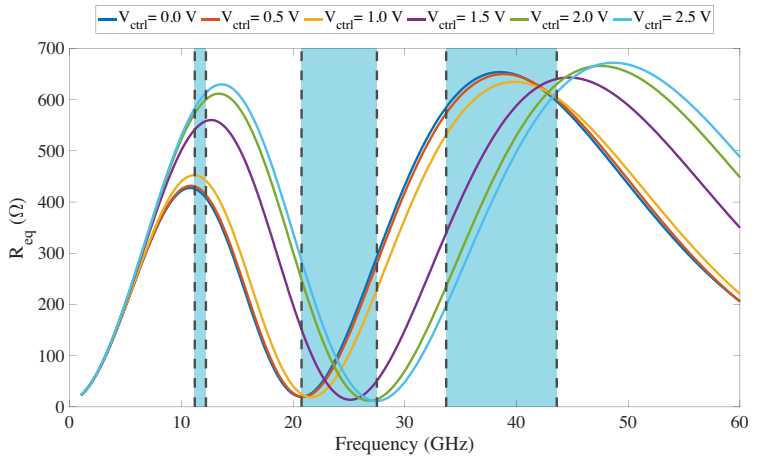

Figure IV-9 Simulated R_{eq} of the RTPS admittance as a function of V_{ctrl} in the 1 to 60 GHz frequency band. Possible oscillation regions are highlighted in light blue.

Figure IV-9 displays the simulated R_{eq} of the considered RTPS as a function of V_{ctrl} in the 1 to 60 GHz band. The three bands that were identified in Figure IV-8 as potential oscillation regions are also separated using vertical dashed lines. The first and third band (i.e., 11-12 GHz, and 34-44 GHz) show large R_{eq} values, while the second band (i.e., 20-27 GHz) shows reduced R_{eq} values. Here, it is important to remember that for oscillation to occur the condition $|R_{neg}| \leq R_{eq}$ and that smaller R_{neg} magnitudes demand greater g_m values, as shown in (IV-7). Hence, the second region is not suitable for oscillation as it would demand unachievable magnitudes of g_m in current integrated technologies.

In this scenario, only the first and third regions are suitable for a practical implementation. In any case, when dealing with a test application, the lowest frequency is more interesting as it facilitates the measurement. In this case, the first oscillation shows an FTR of 1 GHz, more than sufficient to carry out an accurate indirect measurement of the phase shift presented by the RTPS.

IV.3.2.OBT circuitry

The next key element in the OBT approach proposed hereby is the oscillator core. The considered oscillator core was built using two nMOS transistors (M_{OSC}) and two microstrip transmission lines, presenting a characteristic impedance and electrical length at 60 GHz of $Z_{C,OBT}$ and θ_{OBT}, respectively.

IV.3.2.1. Cross-coupled pair

The main element in the oscillator core are the two matched nMOS transistors. These transistors, as explained above allow to generate an equivalent function to a negative resistor. This block is defined by two main figures, its negative resistance, R_{neg}, and its capacitive parasitics. The transistors were designed using a total width of 23.4 µm, spread over 20 fingers and a gate length of 55 nm.

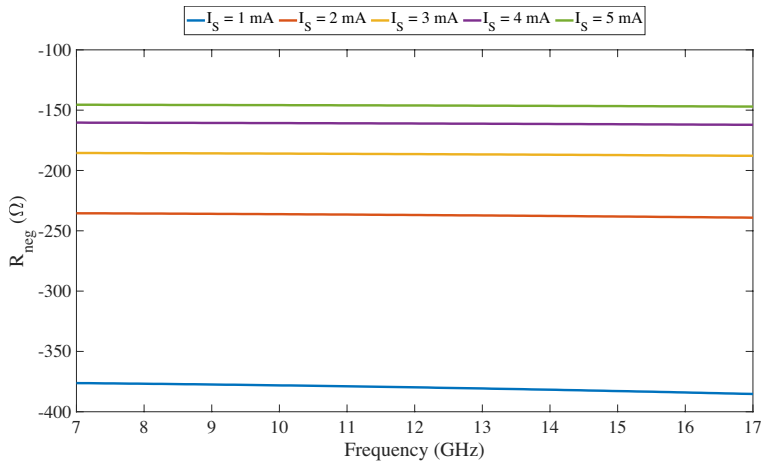

Figure IV-10 Simulated R_{neg} generated by the designed XCP.

Figure IV-10 shows the post-layout R_{neg} simulation as a function of a DC current I_S applied at the source of the transistors M_{OSC}. The equivalent resistance of the RTPS, as seen from the XCP in the 11-12 GHz band, took values in the 400-600 Ω range. Hence, according to Figure IV-10, the proposed XCP should be able to achieve oscillations for any biasing current greater than 1 mA as $|R_{neg}| < 400$ Ω. Any value of $|R_{neg}|$ larger than 400 Ω would result in some or complete lack of oscillations, depending on the V_{ctrl} state. Note that the XCP was designed with enough g_m margin to counteract any additional losses between the simulated and fabricated circuit.

As introduced before, another important parameter of cross-coupled pairs is their parasitic capacitance. In the context of the OBT, this element is relatively less important, when compared with large FTR VCOs, as the tuning range is not the main goal provided that it remains sufficient for the targeted OBT sensitivity. However, as OBT is an intrusive test technique, any parasitics added by the test circuitry may impact the performance of the DUT.

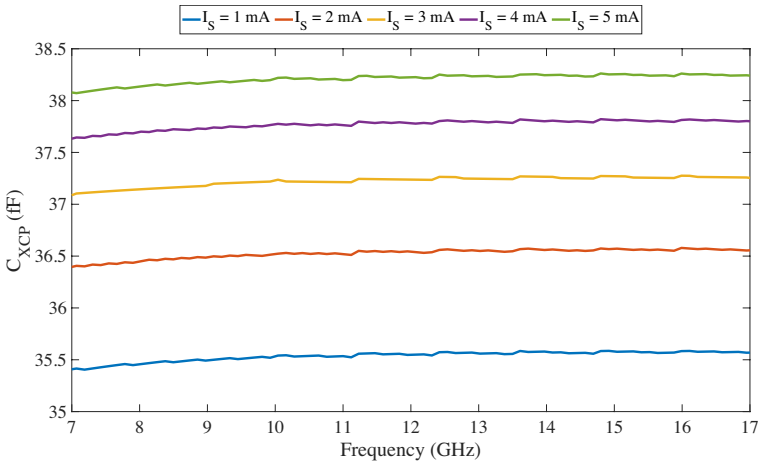

Figure IV-11 Simulated C_{XCP} generated by the designed XCP.

Figure IV-11 presents the post-layout simulation of the equivalent capacitance of the designed XCP, C_{XCP}. At the frequency where oscillations are expected to occur (i.e., 11-12 GHz), the XCP presents around 37 fF of capacitance. Note that the C_{XCP} value is also slightly tuned using the biasing voltage I_S. However, only a small variation of around $\pm$4% is observed.

Finally, in an OBT application with dedicated circuitry integrated on-chip with the DUT, the impact of the added circuitry has to be carefully assessed. Figure IV-12 displays the post-layout simulation of the R_{neg} and C_{XCP} in the 40 to 80 GHz frequency band for $I_S = 0$ mA (i.e., with the OBT circuitry is turned off).

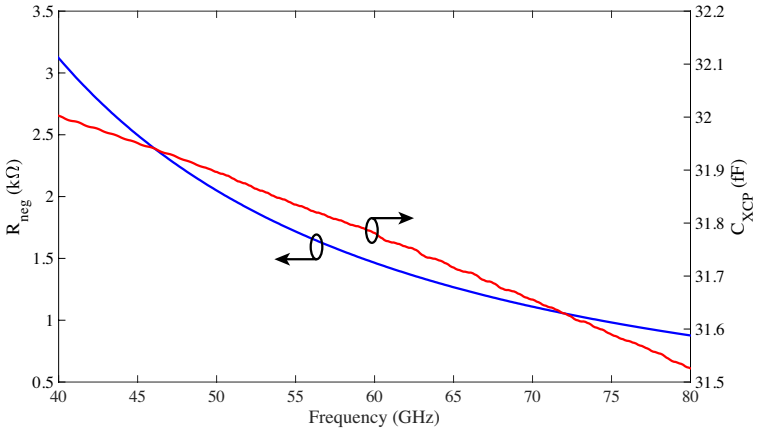

Figure IV-12 Simulated R_{neg} and C_{XCP} in the 40 to 80 GHz frequency band, for $I_S = 0$ mA.

Figure IV-12 presents the results of the XCP in its OFF-state at the RTPS working frequency. The presented results are of major interest, in order to assess the impact of the added circuitry on the DUT performance. Note that, in this case, R_{neg} presents a positive magnitude, as no current is flowing through the XCP. At 60 GHz, R_{neg} presents a magnitude around 1.5 kΩ. On the other hand, its parasitic capacitance at 60 GHz is around 32 fF.

IV.3.2.2. Current mirror

As introduced before, in practical VCO implementations a current source is usually placed at M_{OSC} source level. The current source allows to control the current flowing into the tank, and thus, achieving steady oscillations.

In this work, a simple current source was designed using two nMOS transistors. It is well-known that the current mirror architecture chosen for the implementation of the current source allows to obtain a ratio of currents circulating on each transistor, depending on the ratio $\alpha = \frac{L_1 \cdot W_2}{L_2 \cdot W_1}$, where W_1

(W_2) and L_1 (L_2) represent the gate width and length of the $M_{S,1}$ ($M_{S,2}$) transistor. This strategy can be used to reduce the system DC current consumption with ratios $\alpha > 1$. However, in the presented design both transistors were designed using the same geometry. Hence, $\alpha = 1$ was obtained using two nMOS transistors with 55 nm of gate length and 45 µm of width spread over 10 fingers. Additionally, a 1-pF MOM capacitor, C_M was placed at gate level of $M_{S,1}$ and $M_{S,2}$ to help filter the low-frequency noise.

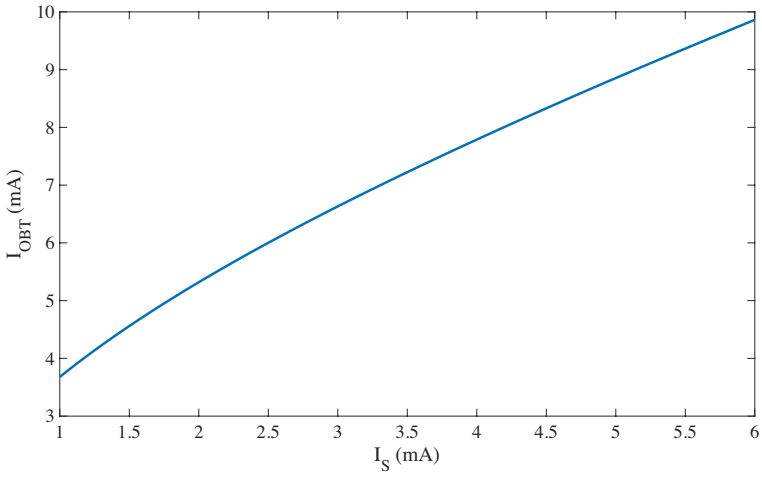

Figure IV-13 Simulated I_{OBT} as a function of I_S with $V_{DS} = 1.2$ V for $M_{S,2}$.

Figure IV-13 shows a post-layout simulation of the DC-current flowing through $M_{S,2}$ as a function of I_{OBT}, when its $V_{DS} = 1.2$ V.

IV.3.2.3. Buffer

In this case study, the oscillations are measured using an external spectrum analyzer. Hence, an isolating stage is required to avoid the direct loading of the system with the spectrum analyzer. For this purpose, a buffering stage was designed.

The proposed buffer is composed of a nMOS transistor (M_B) whose source is connected to an RC network. This system has to achieve three main goals: (i) isolate its output and the oscillator loop, (ii) maximize the power output to a 50-Ω spectrum analyzer, and (iii) present a low capacitance at 60-GHz to minimize perturbations to the RTPS.

The first goal is mostly achieved by the design of the M_B transistor. In this case, the transistor was designed with a total width of 9 µm spread over 5 fingers and a gate-length of 55 nm. Next, the second goal is achieved with the whole buffer network. The transistor dictates the gain achieved by the buffering stage, while the RC network set the output impedance close to 50 Ω, when considered together with M_B, and filtrates the DC voltage.

The RC network was designed using a polysilicon resistor R_B with a width of 0.54 µm and a length of 5.9 µm, presenting a resistance of 190 Ω. Then, the capacitor C_B was designed using a MOM architecture leading to 1 pF. The MOM capacitor was subsequently connected to a 50-Ω microstrip transmission line with a length of 171 µm, which allows to connect the capacitor to the probing pad. Note that the used resistor will lead to added noise in the oscillation. However, as explained before, noise is not an issue on this application, as long as it does not mask the oscillation characteristics.

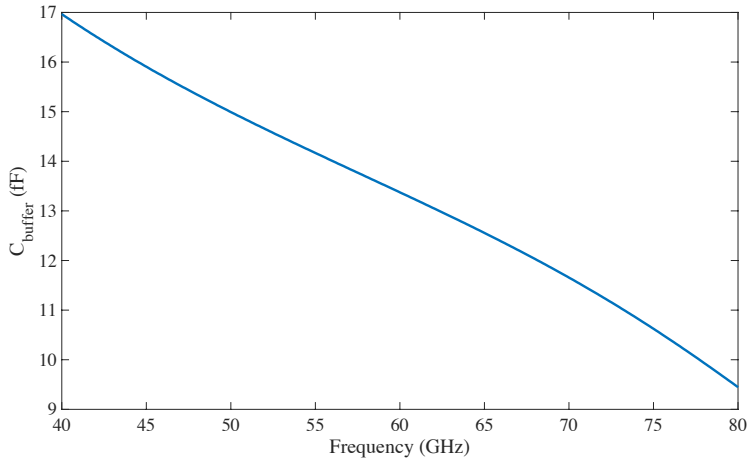

Figure IV-14 Simulated input capacitance of the buffer in the 40 to 80 GHz frequency band.

Figure IV-14 presents the post-layout simulation of the input capacitance of the buffering stage in the 40 to 80 GHz frequency band. At 60 GHz, the buffer presents an input capacitance of 13 fF (i.e., $-j \cdot 190\ \Omega$ at 60 GHz). In this work, as the OBT circuitry is designed for testing purposes, this is the most critical performance. It is of capital importance that the OBT circuitry does not degrade significantly the functionality and performance of the DUT. Once this is achieved, the buffer has to present sufficient isolation, gain and 50-Ω matching to allow proper frequency readout.

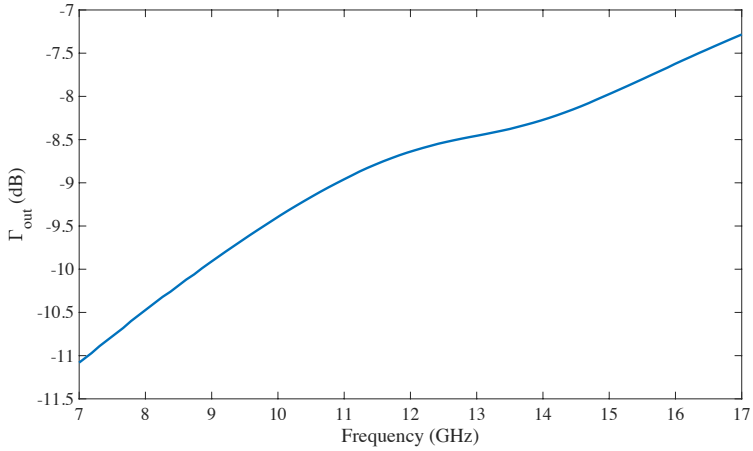

Figure IV-15 Simulated reflection coefficient at the output of the buffer in the 7 to 17 GHz band.

Figure IV-15 displays the post-layout simulation of the reflection coefficient at the output of the buffer stage. In the 11-12 GHz band (i.e., the expected oscillation frequency) the reflection coefficient is around -9 dB. Note that this is a quite large value. However, this is not an issue as sufficient power is transmitted to the output, as it will be demonstrated in the following sections.

IV.3.2.4. Oscillator core transmission lines

Finally, two microstrip transmission lines were used to interconnect the DUT and the OBT circuitry presented above. These transmission lines have two main objectives: (i) connect the input and the output of the RTPS, which are physically far apart (i.e., the length of the 3-dB coupler, which is around 420 µm at 60 GHz), and (ii) isolate the OBT circuitry from the RTPS when the RTPS is in normal operation.

Ideally, when the RF signal of the RTPS in normal operation mode reaches the intersection between these transmission lines and the RTPS, the impedance at the input of the transmission line must be infinite (i.e., open-circuit), to minimally impact the RTPS performance. However, at the same time, these transmission lines will now participate in the RLC tank seen by the OBT circuitry. Hence, their

geometry must be carefully chosen so as to achieve a trade-off between the isolation of the RTPS and the needed performance of the rest of the OBT circuitry.

This condition is achieved with high-impedance transmission lines whose length is roughly $\lambda_G/4$ at the central frequency of the RTPS (i.e., 60 GHz). In this design, these lines were designed using a width of 0.54 µm and a length of 585 µm, roughly leading to a characteristic impedance $Z_{C,OBT}$ of 75 Ω and an electrical length at 60 GHz, θ_{OBT}, of 85º. Their size was optimized regarding the trade-off existing between the equivalent resistance seen by the XCP, R_{eq}, at the resonant frequency and the impact on the RTPS.

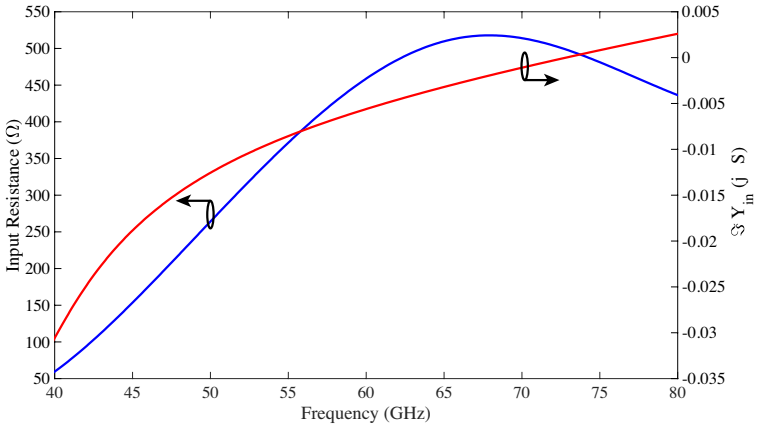

Figure IV-16 Simulated resistance and imaginary part of the admittance seen at the input of the transmission lines placed between the XCP and the RTPS for $V_{buffer} = 0$ V and $I_S = 0$ mA (i.e., OBT circuitry in OFF-state).

Figure IV-16 displays a post-layout simulation of the input resistance seen at the junction between the RTPS and the quarter-wavelength transmission lines when $V_{buffer} = 0$ V and $I_S = 0$ mA, in the 40 to 80 GHz frequency band. At 60 GHz, and throughout the whole considered band, the imaginary part of its admittance is quite reduced (i.e., around $-5\,j \cdot mS$) and the input resistance, calculated as $\Re(Y_{in}^{-1})$, shows a rather large value of 460 Ω at 60 GHz. Hence, the added OBT circuitry practically behaves as an open circuit.

Next, let us evaluate the same performance with the OBT circuitry in the ON-state (i.e., test-mode). For this purpose, let us set $V_{buffer} = 1.2\ V$ and $I_S = 2\ mA$. Figure IV-17 presents a post-layout simulation of the same performances shown in Figure IV-16, with the biasing considerations leading to an ON-state of the OBT circuitry.

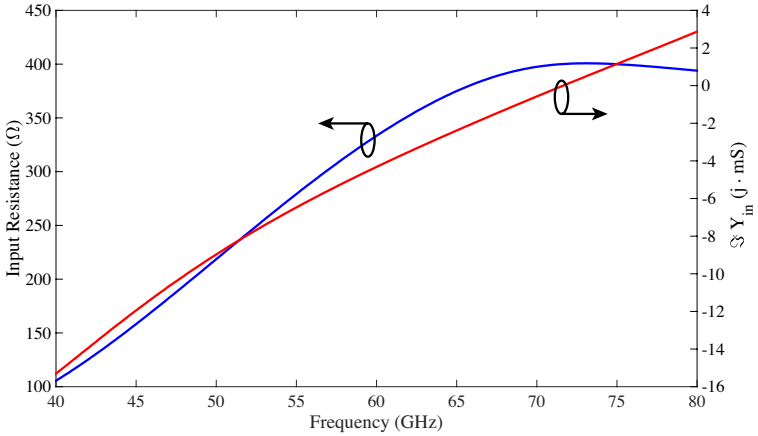

Figure IV-17 Simulated resistance and imaginary part of the admittance seen at the input of the transmission lines placed between the XCP and the RTPS for $V_{buffer} = 1.2\ V$ and $I_S = 2\ mA$ (i.e., OBT circuitry in ON-state).

Note that, above 55 GHz, the input resistance is larger than 300 Ω (i.e., around 6 times the impedance of the RTPS). On the other hand, the imaginary part of the input impedance is in the order of some mS throughout the whole considered band. Hence, for frequencies above 55 GHz, good isolation between the RTPS and the OBT circuitry can be expected. This is a very interesting feature, since it allows an on-line test strategy. It is important to remember here that the oscillation frequency is expected to occur in the 11-12 GHz band, while the RTPS has a central frequency of 60 GHz. Nevertheless, on-line testing will introduce oscillations in the same RF path as the signal being received/transmitted. In this case, as the oscillation frequency is far from the central frequency of the DUT and probably the whole system, the oscillation will be naturally filtered throughout the reception/transmission chain. However, an on-line testing approach must carefully consider the whole system as the introduced oscillations might have other undesired effects, such as reducing the SNR, adding distortion, setting amplifiers into oscillation, etc.

It is interesting to notice that the proposed test architecture does not need of the integration of switches . This is extremely beneficial for many reasons: (i) the leakage and insertion loss of mm-wave switches is relatively high, with losses around 1.5-3 dB in current integrated technologies [89]. (ii) the added design complexity and biasing circuitry. The low performance of mm-wave switches is a critical issue for the proposed OBT approach, as the losses in the switches might require a very low R_{neg} to set the system into oscillation.

To summarize, the different parts composing the OBT circuitry have been presented. However, the added circuitry might have an impact on the RTPS. In addition, the OBT circuitry may also impact the performance of the RTPS as a resonant tank, due to the added parasitics. The next section discusses the impact of the OBT circuitry on the RTPS performance as well as its performance as a resonant tank.

IV.3.2.5. Impact of the OBT circuitry

a) RTPS as a phase shifter

One of the main limitations of BIST techniques tapping into internal circuit nodes is their potential impact on the DUT performance. In this line, Figure IV-18 displays a post-layout simulation comparison of the proposed RTPS performances at 60 GHz as a function of V_{ctrl}. The compared performances account for the RTPS without (solid-line) and with (dashed-line) the OBT circuitry.

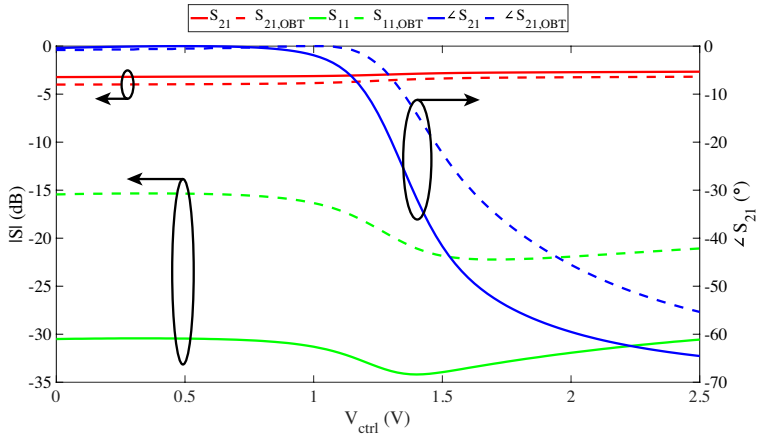

Figure IV-18 Simulation of the RTPS performance without (solid-line) and with (dashed-line) the OBT circuitry at 60 GHz.

Due to the added circuitry, the RTPS shows a maximum insertion loss degradation of 0.8 dB. On the other hand, the return loss is increased by 15 to 10 dB, depending on the V_{ctrl} value. However, its value remains below 15 dB for any V_{ctrl}. Hence, the impact on the matching of the RTPS is very limited. Finally, the RTPS without the OBT circuitry shows a maximum phase shift, $\Delta\varphi$, of 65º, while the $\Delta\varphi$, when the OBT circuitry is added, is reduced to 55º. Hence, the FoM for the RTPS passes from 20 º/dB to 14 º/dB, when the OBT circuitry is added.

Post-layout simulations show that the impact added by the OBT circuitry is quite contained. As compared to the RTPS characterization measurements shown in the previous Chapter, the insertion and return loss show very good agreement. On the other hand, in the measurement the $\Delta\varphi$ was reduced by 10º, as compared to the post-layout simulations presented hereby. This can easily be explained by the difference observed between the EM simulations of the 3-dB coupler and its measurement. Most probably by the observed difference between the simulated and measured impedance of the 60-GHz 3-dB coupler. Note that different impedances can lead to equal return loss. On the other hand, as explained in the previous Chapter, the $\angle S_{21}$ is dictated by the relative impedances of the load and the 3-dB coupler, which could easily explain the drift in the simulated and measured $\Delta\varphi$. As it will be shown later, this theory is supported by the measurement results obtained with the OBT circuitry.

b) RTPS as an RLC tank

Next, as additional circuitry has been added (i.e., XCP, buffers, current mirror and transmission lines), the performance of the RTPS as an RLC tank has been modified due to the presence of these elements. Hence, the magnitude of the elements in the RLC tank has also been altered. In this scenario, the characteristics of the RLC tank must be evaluated again to ensure that the system is still capable of performing oscillations.

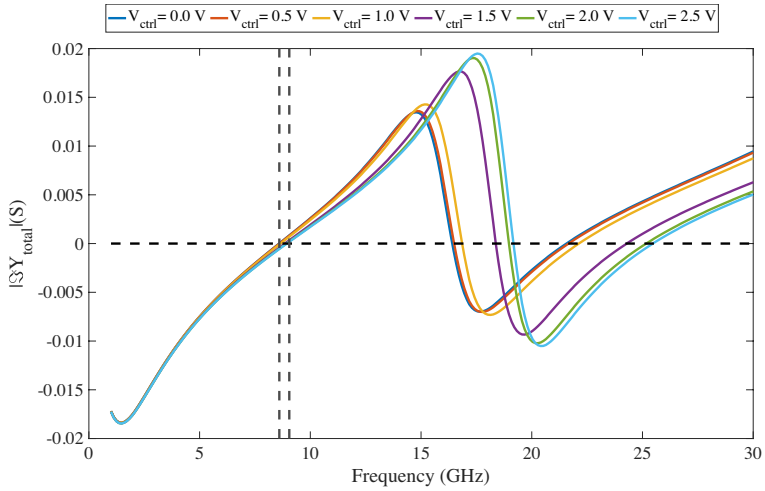

Figure IV-19 Simulated imaginary part of the admittance of the complete closed loop when $I_S = 2$ mA and $V_{buffer} = 1.2$ V in the 1 to 30 GHz frequency band.

Figure IV-19 shows post-layout simulation of the imaginary part of the complete closed loop system for $I_S = 2$ mA and $V_{buffer} = 1.2$ V (i.e., OBT circuitry in the ON-state). With these considerations, the XCP is performing as a -240 Ω resistor R_{neg}, as shown in Figure IV-10. Note that, again, the considered system shows a null imaginary part in three regions (i.e., 8.7 to 9 GHz, 16 to 19 GHz, and 21 to 25 GHz). Hence, the phase criterion among the Barkhausen criteria holds in these regions. Note that the first region is surrounded by vertical dashed lines.

However, for oscillations to occur, the total gain in the closed loop must be equal or greater than the unity. For this purpose, let us evaluate the total resistance of the closed loop system using the above considerations. Figure IV-20 displays the total equivalent resistance of the closed loop system, R_{eq}, for $I_S = 2$ mA and $V_{buffer} = 1.2$ V. Note that, as expected from the RTPS as an RLC tank simulation, in the second region (i.e., from 16 to 19 GHz) the equivalent resistance of the RTPS is too low for the XCP to compensate it. Hence, the total equivalent resistance in these frequency range is above 0 (i.e., total closed loop gain below unity), leading to a non-oscillating system in this frequency range. On the other hand, for the first and third regions (i.e., 8.7 to 9 GHz, and 21 to 25 GHz) the total closed loop shows a negative resistance, leading to both of the Barkhausen criteria being held for these

frequency ranges. Hence, the system is expected to simultaneously oscillate in these frequencies, leading to a multi-tone oscillator.

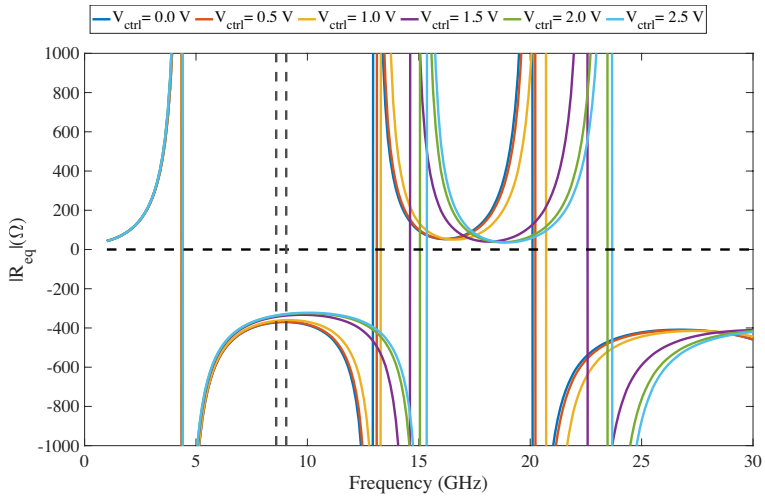

Figure IV-20 Simulated R_{eq} of the complete closed loop when $I_S = 2$ mA and $V_{buffer} = 1.2$ V in the 1 to 30 GHz frequency band

The post-layout simulation of the magnitude and central frequencies of the oscillations at the output of one of the system buffers as a function of V_{ctrl} is shown in Figure IV-21. As expected from Figure IV-19 and Figure IV-20, the system central frequencies of the closed loop system occur in the 8.7 to 9 GHz frequency range. In these frequencies, the system outputs a power between -21 and -23 dBm on a 50-Ω load. Hence, comparing Figure IV-21 and Figure IV-18, a clear correlation between the RTPS phase shift and its oscillation frequency and power output are observed. Simulation also reports an oscillation in the 21 to 25 GHz frequency band. However, as this band was not measured, these results are omitted for the sake of clarity.

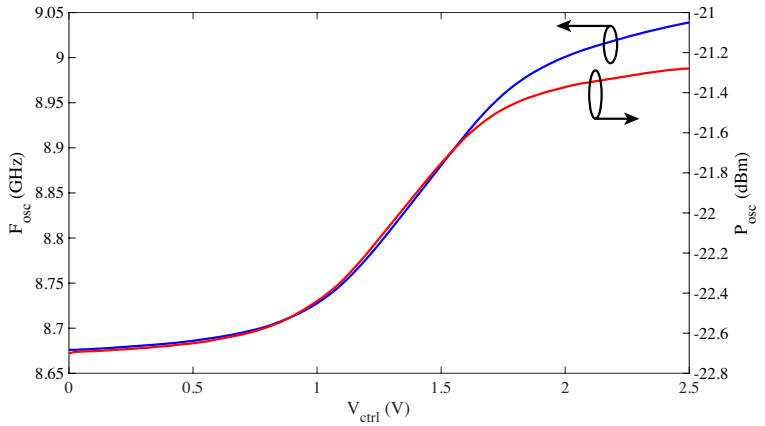

Figure IV-21 Simulated oscillation amplitude and power at the output of one of the buffers as a function of V_{ctrl}.

To summarize, in this section the design methodology, goals and results for the OBT circuitry of a 60-GHz RTPS were described. In addition, the existing correlation between the oscillation characteristics (i.e., power and frequency) and the RTPS phase shift were demonstrated.

IV.4. Measurement results

In order to demonstrate the feasibility and performance of the proposed test technique, a proof-of-concept prototype was built in the STM 55-nm technology. The proposed OBT circuitry was integrated together with a 60-GHz RTPS, whose performance was presented in the previous Chapter. Figure IV-22 presents a micrograph of the fabricated RTPS and the OBT circuitry around it. The total

surface of the proposed circuit is of 0.22 mm^2, leading to an area overhead of only 0.03 mm^2 (i.e., 16% increase), as compared to the stand-alone RTPS.

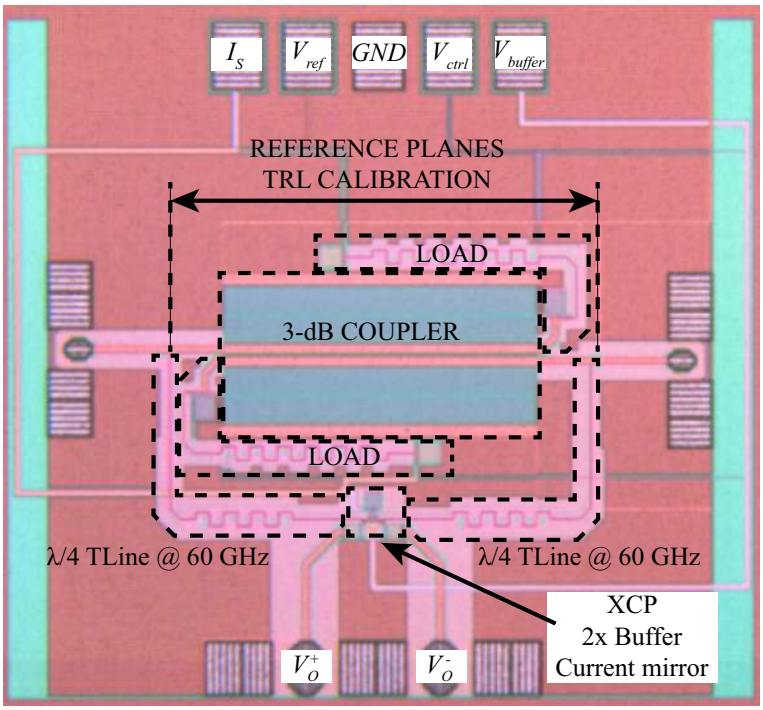

Figure IV-22 Micrograph of the fabricated RTPS and the OBT circuitry.

The oscillation characteristics were measured using an HP 8562A spectrum analyzer, which allows to cover the 9 kHz to 18 GHz frequency band. However, the employed spectrum analyzer only allows single-ended measurements. For increased setup symmetry, the untested port (V_O^-) was loaded using an off-chip 50-Ω load. Finally, the biasing voltages applied in the pads located at the top of Figure IV-22, were provided using an off-chip battery system with large capacitive values for noise decoupling purposes. For the measurement results presented subsequently, $V_{ref} = V_{buffer} = 1.2$ V, and $I_S = 2$ mA.

Figure IV-23 displays the output power of the oscillations measured at the V_O^+ port, as a function of V_{ctrl}. Note that measurements with V_{ctrl} values up to 1.9 V are shown, as explained in the previous Chapter, practical issues impeded the measurement in the full V_{ctrl} range .The power of the oscillations ranges between -26.5 and -31.5 dBm, with a total power imbalance of 5 dBm, which is relatively greater than the power imbalance of 2 dBm expected in the post-layout simulations shown in Figure IV-21. Nevertheless, agreement between post-layout simulation and measurement remains good, considering that the loss in the cables connecting the DUT and the spectrum analyzer was not de-embedded. Note that the power output is relatively low. On the other hand, it is far from the noise floor of most modern spectrum analyzers and thus can be easily measured. However, the buffering stage could be redesigned if greater power levels were needed.

However, note that the power output appears to be highly non-linear. This magnitude mostly relies on the losses in the complete loop. Comparing the expected insertion loss of the RTPS, shown in Figure IV-18 with the measured insertion loss shown in the previous Chapter, the insertion loss of the RTPS also appears to have a non-linear behavior. Hence, the non-linearity of the output power can easily be explained by the non-linearity of the insertion loss as a function of V_{ctrl}.

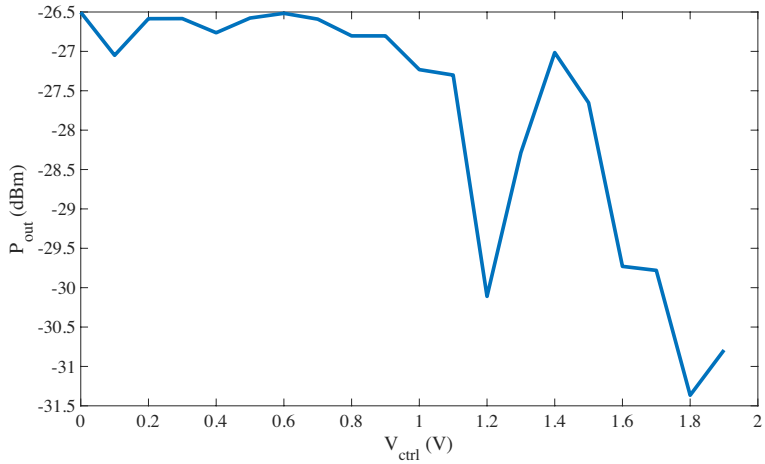

Figure IV-23 Measured output power at the V_O^+ port as a function of V_{ctrl}.

Next, Figure IV-24 shows the measured phase shift of the RTPS at 60 GHz when the OBT circuity is in its OFF-state and the OBT oscillation frequency, both as a function of the RTPS control voltage. First, note that the correlation existing between both is clearly seen in this figure. The oscillation frequency ranges between 10.8 and 10.9 GHz, leading to an FTR of 100 MHz. On the other hand, the post-layout simulation results reported oscillation frequencies in the 8.7 to 9 GHz. Hence, a shift of around 2 GHz is observed together with a reduction of the FTR of around 200 MHz. Again, the difference observed between simulation and measurement can probably be assumed to be the result of the inaccurate simulation results of the 60-GHz 3-dB coupler.

Nevertheless, the FTR remains sufficient for proper central frequency readout, as shown by Figure IV-24, where no noise is observed in the presented frequency measurements. Next, even though a slight increase between the expected and measured oscillation frequencies, these oscillations occur at around 6 times lower frequencies than the central frequency of the RTPS, which greatly facilitates the measurement of the oscillation frequency.

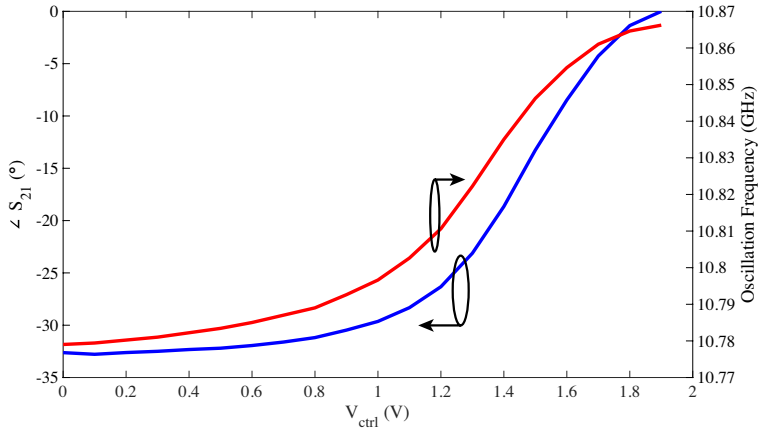

Figure IV-24 Measured $\angle S_{21}$ of the RTPS at 60 GHz and F_{osc} at the V_O^+ port as a function of V_{ctrl}.

Finally, the goal of the proposed OBT approach is to create a correlation between the oscillation frequency and the DUT performance, which in this case is the phase shift. The correlation, as explained before, can be used for testing purposes and eventual subsequent calibrations, substituting the traditional direct functional test. Figure IV-25 presents the measured correlation between the $\angle S_{21}$ and the oscillation frequency.

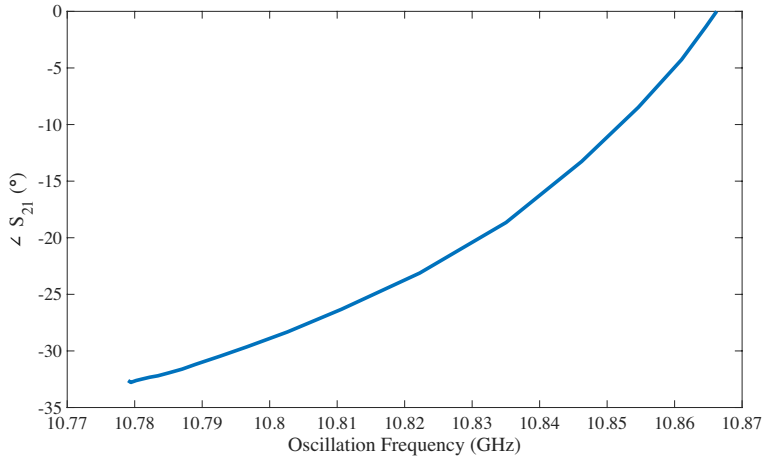

Figure IV-25 Measured correlation between the oscillation frequency and the 60-GHz $\angle S_{21}$.

Hence, Figure IV-25 demonstrates the possibility of determining the phase shift of a 60-GHz RTPS with the measurement of the oscillation frequency achieved by the OBT circuitry embedded together with the considered RTPS.

To summarize, in this section measurements of the oscillation characteristics of the considered RTPS with its OBT dedicated circuitry were reported. The presented results show the possibility of determining the phase shift of the RTPS with the measurement of its oscillation performances.

IV.4.1.Discussion on on-line testing

Finally, as introduced before, the low frequencies (as compared to the central frequency of the RTPS) at which the oscillations occur open the door to the so-called on-line testing. On-line testing aims at the test of the DUT while it is under normal working conditions. In this case, on-line testing would be performed while the phase shifter is being actuated for phase shifting purposes. This testing scheme has to be carefully evaluated as the signal being transmitted by the RTPS will contain some of the oscillation characteristics. Hence, some telecommunication protocols might suffer from this issue.

For the measurements presented above, the pads corresponding to the input and output of the RTPS (right and left pads of Figure IV-22) were left unconnected. This is a realistic approach as most of the circuits in an RF transceiver show a great return loss outside their central frequency.

However, in a transceiver the impedances of the other devices surrounding the RTPS are part of the equivalent RLC tank. For RTPS integrated in a complete transceiver and willing to use an on-line testing scheme the impact of the other circuitry must be carefully evaluated.

Figure IV-26 shows the post-layout simulation of the oscillation frequency and power output for the considered closed-loop system, when the input and output ports of the RTPS are loaded by 50 Ω. This is a possible scenario in an ultra-wideband system. Even though the results shown in Figure IV-26 are merely illustrative, as the impedances in the input and output of the RTPS depend on the system where the RTPS is embedded, they show the great dependence of the oscillation characteristics on the value of these impedances.

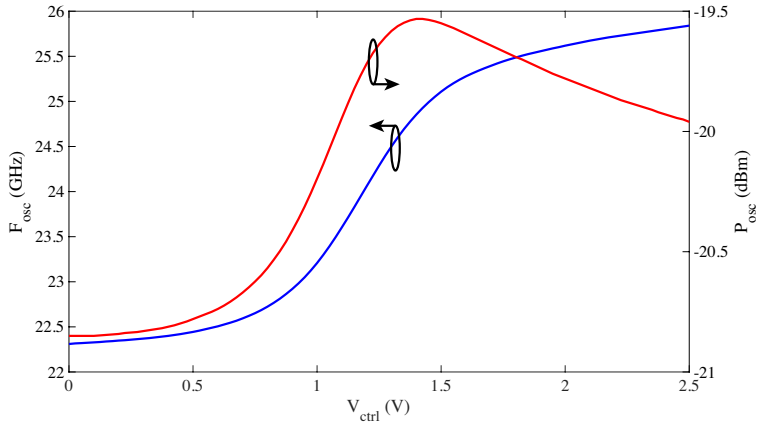

Figure IV-26 Simulated oscillation amplitude and power at the output of one of the buffers as a function of V_{ctrl} in an on-line testing approach.

Nevertheless, using the design procedure described above, the system can be easily set into oscillation, enabling an on-line testing methodology.

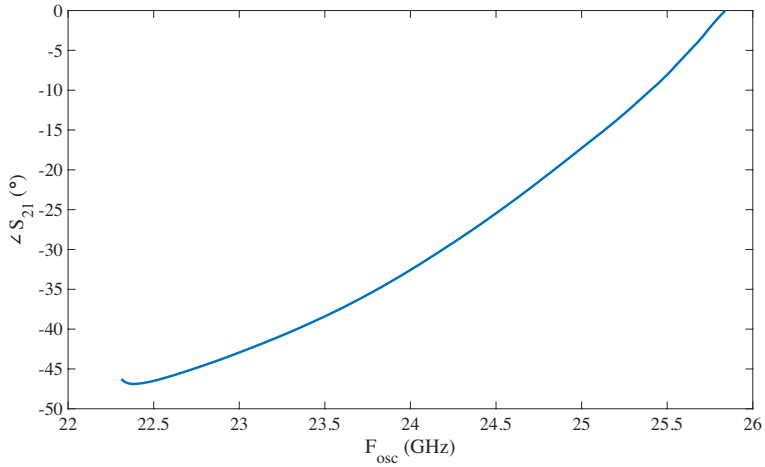

Figure IV-27 Simulated correlation between the oscillation frequency and the 60-GHz $\angle S_{21}$ in an on-line testing approach.

Finally, Figure IV-27 depicts the simulated correlation between the RTPS phase shift at 60 GHz and its oscillation frequency, F_{osc} in an on-line testing scheme. Hence, demonstrating that this approach is also capable of accurately predicting the phase shift of the RTPS through the measurement of the oscillation frequency outputted by the OBT circuitry.

IV.5. OBT for complete phased arrays

The previous sections have presented the design, and simulation and measurement results of an OBT approach for mm-wave RTPS. However, in a phased array system, the actual important parameter is the relative phase shift existing between two neighboring phase shifters rather than the actual phase shift introduced by each phase shifter. To avoid nomenclature issues, let us name the relative phase shift between two neighboring phase shifters, i and j, as $\Delta\varphi_{ij}$. The relative phase difference is defined as:

$$\Delta\varphi_{ij} = \varphi_i - \varphi_j, \tag{IV-9}$$

where φ_i (φ_j) represents the phase shift introduced by the i-th (j-th) phase shifter.

As it was demonstrated earlier, the oscillation frequency of an RTPS, $F_{osc,RTPS}$, in an OBT test scheme is a function its phase shift, φ_{RTPS}. Hence, $\Delta\varphi_{ij}$ must also be a function of the difference in the frequency of oscillation between the i-th and j-th RTPS, $\Delta F_{i,j}$:

$$F_{osc,RTPS}(\varphi_{RTPS}) \rightarrow \Delta F_{i,j}(\Delta\varphi_{ij}) \tag{IV-10}$$

In order to integrate the hypothesis (IV-10) as an on-chip solution, some additional circuitry is needed. A good candidate to perform the down-conversion needed in (IV-10) are multipliers. It is well known that an ideal multiplier outputs a signal with two tones f_{out} in the form:

$$f_{out} = f_i \pm f_j \tag{IV-11}$$

if f_1 and f_2 are the single-tone input signals of the considered multiplier.

Note that the designed OBT circuitry has a differential output. Hence, single-ended multipliers can be connected in a scheme similar to the one proposed in Figure IV-28. Note that the proposed architecture in this Figure is extendable to a phased array with an n number of phase shifters.

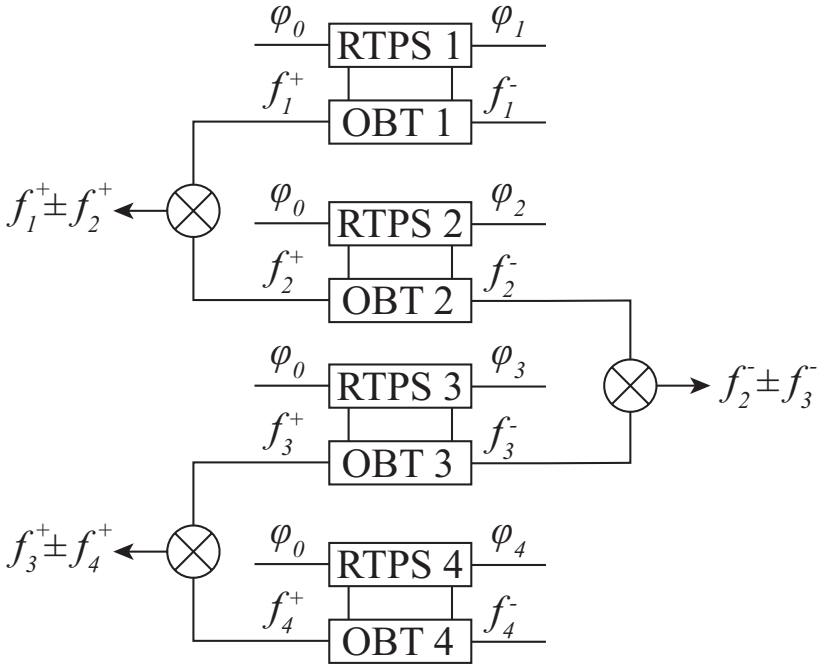

Figure IV-28 Phased array with 4 RTPS with OBT circuitry and multipliers attached to them.

In order to evaluate the performance of the scheme proposed above, let us consider the measured RTPS under an off-line test approach and ideal multipliers. In this scenario, if only the lower frequency difference outputted by the multipliers is considered for measurement easiness, the function representing the relationship between the frequency difference between two neighboring phase shifters and their relative phase shifts can be represented as in Figure IV-29.

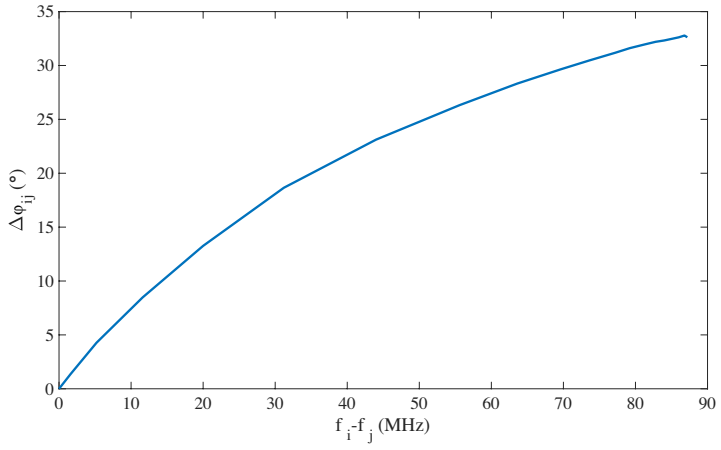

Figure IV-29 Simulated relative phase shift and frequency difference at the output of the multiplier connecting the OBT circuitry of two neighboring phase shifters.

Note that the presented curve in Figure IV-29 shows that the relative phase shift between two neighboring phase shifters can be easily calculated with the measurement of the difference in the frequency outputted by their OBT circuitry. This curve presented in Figure IV-29 presents a slope varying between 0.1 º/MHz and 0.85 º/MHz. Hence, with this approach, the relative phase shift between two neighboring RTPS can be characterized with a resolution of 1º with a measurement setup achieving 1 MHz resolution, within a frequency span from around 0 to 90 MHz. However, note that the presented OBT outputs a relatively low power signal (i.e., around -20 dBm). Hence, in order to adopt this approach, some kind of power amplification might be required to allow driving the multiplier stage.

In this scenario, due to the relaxed needs in the measurement setup. An on-chip measurement system could be envisioned adding self-calibration and self-healing capabilities to the presented RTPS architecture.

IV.6. Conclusions

This Chapter explores the application of the OBT methodology to an integrated mm-wave phase shifter. The basic theory, design methodology and measurement results were illustrated on a case study consiting in a 60-GHz RTPS with OBT capabilities. To the best of the authors' knowledge, this is the first time that the OBT technique is employed for testing mm-wave integrated circuits.

The presented results show a clear correlation between the outputted frequency by the OBT circuitry and the phase shift performed by the RTPS in an off-line testing scheme. These results enable the OBT technique for the testing of mm-wave RTPS. In addition, the simulated results in an on-line testing scheme are also presented, showing the performance of the proposed approach when this kind of testing scheme is used.

Finally, a possible extension of the proposed approach for BIST applications in the context of a complete phased array is also proposed.

ADDITIONAL WORK & PERSPECTIVES

This manuscript was only able to grasp a part of all the work carried out during these three years. Thanks to the close collaboration with STMicroelectronics and the great access to the 55-nm BiCMOS technology, for which I would like to thank again Cédric Durand and Daniel Gloria, many other subjects in the mm-wave domain could be explored. The additionally explored subjects can be classified into three main categories: (i) miniaturization of passive devices, (ii) switching architectures, and (iii) calibration and measurement. I present a brief description of the works having been carried out alongside the works presented in the manuscript, and also some perspectives to this work.

In the first category, alternative slow-wave topologies were proposed, such as meandered S-CPWs or slow-wave topologies taking advantage of the 3D geometry of the BEOL. In addition, alternative resonating structures were designed using slow-wave CPS.

In the second category, some switching architectures were designed in the form of classical Single-Pole Double-Throw (SPDT) switches or as innovative architectures such as the Thru-Load system.

Finally, in the third category I could bring my interest to measurement uncertainties calibration techniques, especially with special regard to the on-wafer TRL. Some statistical models were derived in the context of measurement and TRL calibration, which aim to help the designer assessing the measurement uncertainty as well as for calibration compaction purposes. Some of the works described in this paragraph have been or are awaiting publication from international conferences, where the principle or a fraction of the work has been published. In the future, together with the people involved in these projects, we plan to extend the results and the understanding of the principles behind these works and hence propose more thorough and extensive publications.

Concerning the perspectives of the work presented in this manuscript, the work concerning the CS-CPWs can be extended for the design of more complex elements such as baluns (e.g., Marchand balun), tanks for VCOs, and directional couplers for on-chip testing architectures such as integrated VCOs or for BIST approaches. In addition, I plan to continue investigating the innovative approaches for the design of varactors presented in Chapter II. These architectures, which as pointed out in this manuscript, lack of robust high-frequency models due to their unorthodoxy. However, even with a non-optimal modelling of these devices, competitive varactor topologies were achieved. Hence, it is worth to continue its investigation and implementation on tunable circuits for tunability or calibration purposes. Finally, the presented OBT approach for mm-wave phase shifters must be completed. In this line, I plan to design some additional circuitry for a complete phased array OBT. This system, as pointed out in Chapter IV, will most likely integrate multipliers to obtain the frequency difference between the different phase shifters integrating the phased array, which will eventually be correlated to the phase difference between the neighboring phase shifters. Nevertheless, other possible approaches without mixers have been envisioned. For instance, it is well-known that in a phased array one of the ports of all phase shifters share an electrical connection to a single node, which will likely be connected to a PA or a Low-Noise Amplifier (LNA). In this context, let us consider two RTPS (e.g., $RTPS_1$ and $RTPS_2$) of the phased array, which are set into oscillation. With these considerations, a certain amount of the oscillation signal form $RTPS_1$ might inject to the $RTPS_2$ OBT circuitry (i.e., an XCP) and vice-versa. If sufficient power from one RTPS reaches the other, self-mixing can occur at the OBT circuitry level. In this case, both phase shifters would output their self-resonant frequencies, the self-resonant frequency of the other RTPS, and, most importantly, the frequency difference between their self-resonances, which might be correlated to their phase difference, as explained in Chapter IV. This is a particularly interesting approach as no extra circuitry, in addition to the elements presented in this manuscript, would be required. However, as introduced before, sufficient power has to leak to $RTPS_1$ from $RTPS_2$ to lock its oscillations into this mode of operation. Hence, for this approach, more accurate modelling of the OBT circuitry is required.

GENERAL CONCLUSIONS

The work in this thesis has presented the design and measurement of each of the blocks needed for the design of mm-wave RTPS ("Reflection Type Phase Shifter"). In addition, the design and practical implementation of the circuitry needed for the implementation of OBT ("Oscillation Based test") in these devices has been discussed and measurements have been carried out. Throughout the whole manuscript, all the presented measurements where performed on the STM SiGe 55-nm technology.

First, in Chapter I, the theory behind the design and characterization of mm-wave 3-dB coupled-lines couplers was presented. In that part of the manuscript, some coupled-line topologies, in particular the broadside couplers, were described. However, their limited performance makes it a less interesting approach for the design of mm-wave on-silicon 3-dB couplers. The CS-CPW topology was favored due to its great degree of flexibility and high compatibility with integrated technologies. In that Chapter, a distributed model for this architecture was also proposed, accounting for the different shielding topologies that can be used. In addition, a detailed methodology for the calculation of the elements composing the model was also described, based on previous work carried out in the modelling of slow-wave transmission lines. As a proof-of-concept two 3-dB couplers were designed with central frequencies of 120- and 185-GHz, respectively. The reported performance of the fabricated couplers greatly agrees with the proposed analytical model as well as with the electromagnetic simulations. In addition, these devices show state-of-the-art performance, great level of integration and superior performance to most of the current reported literature.

Chapter II discussed the current available options for the integration of varactors in current integrated technologies. Many topologies, such as A-MOS and diode varactors were presented. However, as this manuscript focused on the design of high-frequency devices, new approaches were also proposed. In this line, I-MOS varactors, which are not an innovative architecture, were studied. The innovation here was to bring these devices in the mm-wave band. Historically, A-MOS varactors have been preferred over I-MOS varactors due to their greater performance in lower frequency bands. However, as it was demonstrated in this document through an on-silicon characterization of an I-MOS varactor, the performance of the proposed I-MOS can overpass the A-MOS varactors performance. Then, an innovative topology, named CS-MOS, was proposed. It consists in exploring the behavior of a long-gate nMOS transistor in a common-source configuration acting as a varactor. The results obtained for this architecture showed that this is also a viable solution for the implementation of mm-wave varactors. Nevertheless, it is important to point out that both devices (i.e., I-MOS and CS-MOS) fabricated using these architectures use a long-gate geometry. Hence, their operational frequency is beyond their f_{max}. In this scenario, their models were relatively inaccurate as this application was not considered by the manufacturer. Still, the measured performance shows that they could potentially be good candidates for varactor implementation in the mm-wave band and thus some effort should be put in that direction, with an effort to develop accurate models based on Technology Computer-Aided Design (TCAD) modelling.

Then, Chapter III combined the results and theory presented in the previous Chapters for the design of mm-wave RTPS. First, an introduction to the general theory behind this architecture was laid out. Then, the design methodology, on-wafer measurements or simulation results of three mm-wave RTPS were presented. The three presented RTPS were designed with different performance goals, architectures and working frequencies. For instance, a first 60-GHz RTPS was presented using the A-MOS varactors provided by the technology. Then, a 120-GHz RTPS using I-MOS varactors was described. Finally, a 120-GHz RTPS using CS-MOS varactors was also presented. The two first RTPS were fully characterized by measurements, while the last one was only validated by simulation. The 60-GHz phase shifter was designed in a more conservative way showing good agreement with the simulation. However, the 120-GHz RTPS with I-MOS varactors greatly differed from the simulation, due to the inaccuracy of the varactor model. The same effect may be observed for the 120-GHz phase shifter with CS-MOS varactors as the characterization of some of its varactors showed that these devices also differ from simulation results. Nevertheless, as pointed out above, even though is beyond the scope

of this work, a more accurate exploration of these varactors may lead to state-of-the-art mm-wave RTPS when combined with high-performance 3-dB couplers, as may be obtained through the use of the CS-CPW architecture.

Finally, Chapter IV presented an approach for BIST applications in the context of mm-wave RTPS, the OBT. First, the general theory behind OBT in this context was discussed. Then, general theory for the design of VCOs was also presented, as it serves as a baseline for the design of the OBT circuitry. Even though the ultimate goal of these two circuits is to perform distinct functions in a transceiver, their proximity in terms of design flow, makes VCOs a good example to explain the process of designing OBT circuitry for a mm-wave RTPS. Nonetheless, the differences in performance goals between these two circuits were also discussed. Then, the presented theory served as the basis for the presentation of the design of OBT circuitry for the 60-GHz RTPS introduced in Chapter III. This designed circuit was subsequently fabricated and measured. Measurement results report a great degree of correlation between the frequency outputted by the OBT circuitry and the phase shift introduced by the RTPS. This result demonstrated for the first time the viability of OBT as a suitable BIST approach in the context of mm-wave RTPS. At the end of Chapter IV, a possible circuit scheme for the implementation of OBT in a complete phased array was also proposed.

To summarize, in this manuscript, most of the aspects of the design of mm-wave RTPS and even testing techniques have been discussed. In addition, most of the presented devices were backed-up with silicon measurements allowing to compare with the simulated results. This is especially important for OBT, CS-MOS, I-MOS, and the RTPS designed using these varactors, as they represent architectural or conceptual novelties, when compared to the current literature. Even though some of these results differ from their expected behavior, their performance shows that they are interesting paths to study in the field of mm-wave frequencies.

LIST OF PUBLICATIONS

Publications

- **M. Margalef-Rovira**, J. Lugo-Alvarez, A. Bautista, L. Vincent, S. Lepilliet, A. A. Saadi, F. Podevin, M. J. Barragan, E. Pistono, S. Bourdel, C. Gaquière, and P. Ferrari, "Design of mm-wave Slow-wave Coupled Coplanar Waveguides", in *IEEE Transactions on Microwave Theory and Techniques*. *Under review (Major revisions).*

- **M. Margalef-Rovira**, A. A. Saadi, L. Vincent, S. Lepilliet, C. Gaquière, D. Gloria, C. Durand, M. J. Barragan, E. Pistono, S. Bourdel, and P. Ferrari, "Highly Tunable High-Q Inversion-Mode MOS Varactor in the 1–325-GHz Band", in *IEEE Transactions on Electron Devices*, vol. 67, no. 6, pp. 2263-2269, June 2020, doi: 10.1109/TED.2020.2989726.

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- **M. Margalef-Rovira**, O. Occello, A. A. Saadi, M. J. Barragan, C. Gaquiere, E. Pistono, S. Bourdel, and P. Ferrari, “A 30-GHz compact resonator structure based on Folded Slow-wave CoPlanar Waveguides on a 55-nm BiCMOS technology”, *2019 7th Advanced Electromagnetics Symposium (AES)*, Lisbon, Portugal, 2019.

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Titre : Conception de déphaseurs de type réflectif millimétriques avec des moyens de test à base d'oscillation

Résumé : Ce travail porte sur la conception de déphaseurs de type réflectif (RTPS – « Reflection Type Phase Shifter ») en technologie BiCMOS STM 55 nm en bande millimétrique, avec une technique de calibrage basée sur la mesure d'une fréquence issue d'un VCO (OBT – « Oscillation Based Test »). Dans un premier temps, la théorie et les mises en œuvre pratiques des coupleurs 3-dB sont discutées. Une attention particulière est portée à la topologie du guide d'onde coplanaire couplé à ondes lentes (CS-CPW), en raison de ses bonnes performances. En utilisant cette topologie, la mesure de deux coupleurs 3-dB fonctionnant respectivement à 120 GHz et 185 GHz est décrite.

Ensuite, les technologies existantes de varactors intégrés sont discutées. Les résultats des mesures sont présentés pour un varactor MOS en mode inversion (I-MOS) de 1 GHz à 325 GHz. Une architecture de varactor basée sur un MOS en source commune (CS-MOS) est également proposée. Les résultats de mesure de 1 GHz à 145 GHz sont présentés pour cette architecture.

Puis, la théorie des RTPS est présentée et les coupleurs CS-CPW ainsi que les varactors MOS en mode d'accumulation (A-MOS), I-MOS et CS-MOS sont utilisés pour la conception de quatre déphaseurs RTPS. Les résultats de mesure et de simulation de ces déphaseurs, avec des fréquences centrales allant de 60 à 200 GHz, sont présentés.

Enfin, la théorie et les résultats de mesure de l'OBT sur un RTPS intégré fonctionnant à 60 GHz sont discutés.

Mots-clés : Coupleur, Varactor, Déphaseur, Bande millimétrique, OBT, Technologie BiCMOS

Title: Design of mm-wave Reflection-Type Phase Shifters with Oscillation-Based Test capabilities

Abstract: This work focuses on the design of on-silicon mm-wave Reflection-Type Phase Shifters (RTPS) with Oscillation-Based Test (OBT) capabilities for calibration purposes. The STM 55-nm BiCMOS is considered. First, the theory and practical implementations of 3-dB couplers is discussed. Particular attention is brought to the Coupled Slow-wave CoPlanar Waveguide (CS-CPW) topology, due to its good performance. Using this topology, the measurements of two 3-dB couplers are reported: (i) a 120-GHz, and (ii) a 185-GHz coupler.

Next, the existing topologies of integrated varactors are discussed. Measurement results are reported for an Inversion-mode MOS (I-MOS) varactor from 1 up to 325 GHz. Additionally, the Common-Source MOS (CS-MOS) varactor architecture is proposed and measurement results from 1 to 145 GHz for this architecture are reported.

Then, the theory of RTPS is presented and CS-CPW-based couplers together with Accumulation-mode MOS (A-MOS), I-MOS and CS-MOS varactors are used for the design of four RTPS. The measurement and simulation results of these RTPS, with central frequencies ranging from 60 to 200 GHz, are presented.

Finally, the theory and measurement results of the OBT on an integrated 60-GHz RTPS are discussed.

Keywords: Coupler, Varactor, Phase shifter, mm-Wave, OBT, BiCMOS technology

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