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Investigation of resistive memories for Storage Class Memory applications

Diego Alfaro Robayo

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THÈSE

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Automatique, Traitement du Signal (EEATS)

Mémoires resistives pour applications Storage Class Memory (SCM)

Investigation of resistive memories for Storage Class Memory applications

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Abstract

Investigation of Resistive Memories (ReRAM) for Storage Class Memory applications (SCM)

In classical von-Neumann architectures, processing and memory blocks are separated. Latency times for the latter are much more slower. To boost performances, memory hierarchy has been introduced to combine small, fast, but expensive technologies with large, slower, and cheaper ones. In such hierarchy, a notorious latency and storage gap can be distinguished between the lowest memory level and the highest storage one: DRAM and Flash blocks, respectively. Emerging non-volatile technologies are called to fill such gap through the so-called Storage Class Memories (SCM). Among them, Resistive Random-Access Memories (ReRAM), represent an interesting candidate to improve flash performances due to their good scalability, low-power consumption, Back-End of Line compatibility, fast writing and erasing process, and good endurance. However, several roadblocks hinder their implementation at large industrial scale, notably high variability, and low non-linearity, which avoids large crossbar arrays implementation. This thesis work explores such aspects to increase attractiveness of ReRAM technologies for SCM applications. For the former, endurance variability is addressed at the array level through various measurements over diverse stacks configurations. Results allow to study the impact of programming conditions on failure mechanisms dispersions, leading to the development of a stochastic model based on defects generation inside the resistive layer. As for the non-linearity issue, successful co-integration between best-in-class HfO_2 and $GeSeSbN$ Ovonic Threshold Selector (OTS) in 1S1R structures, is demonstrated. Hence, leakage currents compatible with 100Mb-1Gb bank size are obtained. For the first time, to our knowledge, key parameters of OTS+ReRAM systems for high-density crossbar arrays are identified and studied at the statistical level, allowing proposition of further optimizations and opening the way to a whole field of studies which include new materials and circuits to improve 1S1R performances.

Keywords: Resistive Random Access Memories (ReRAM); OxRAM; CBRAM; Ovonic Threshold Switch (OTS) selectors; 1S1R co-integrations.

Résumé

Mémoires résistives pour applications Storage Class Memory (SCM)

Dans les architectures classiques dites de Von-Neumann pour des systèmes d'information, les blocs de mémoire et de traitement sont séparés. Pour le premier, les temps d'accès sont beaucoup plus importants. Afin d'optimiser les performances, une hiérarchie de mémoire a été mise en place. Elle combine des technologies coûteuses, de petite taille, mais très performantes en termes de vitesse; avec d'autres plus larges, à bas coûts per bit, mais plus lentes. Dans une telle hiérarchie, un gap important existe en termes de temps d'accès et capacité de stockage entre les blocs de mémoire les plus bas et ceux de stockage les plus hauts (briques DRAM et FLASH, respectivement). Des technologies émergentes non-volatiles, appelées *Storage Class Memories (SCM)* sont candidates à remplir tel gap. Entre elles, les mémoires résistives vives, ReRAM, de l'abréviation anglaise pour *Resistive Random Access Memories*; représentent une alternative très intéressante grâce à leur bonne scalabilité, basse consommation, compatibilité avec la Back-End-Of-Line (BEOL), leurs temps d'écriture et lecture rapides, ainsi qu'une bonne endurance. Cependant, plusieurs obstacles empêchent leur implémentation à l'échelle industriel, notamment la haute variabilité des états résistifs et la non-linéarité réduite entre eux, ce qui limite l'implémentation des matrices mémoires larges. Ces deux aspects sont étudiés dans ces travaux de thèse. Pour la variabilité, il se trouve que l'endurance, caractéristique fondamentale vis-à-vis des applications SCM, est aussi dispersée. Ce manuscrit présente des caractérisations électriques en endurance au niveau statistique sur des matrices ReRAM de 4Kb. Plusieurs empilements mémoires furent étudiés, ainsi qu'une grande variété des conditions de programmation pour le cyclage. Il a été observé comment la valeur médiane et la déviation standard du claquage des mémoires sont principalement affectées par le RESET. Les résultats expérimentaux ont été utilisés dans la proposition d'un modèle stochastique basé sur la génération de défauts dans la couche résistive. Concernant l'autre grand axe de cette thèse, une co-intégration réussie entre une mémoire HfO_2 (1R) et un sélecteur (1S) de type *Ovonic Threshold Switch (OTS)*, a été démontrée. Les courants de fuite, obtenus grâce à l'addition de l'OTS, sont compatibles avec des matrices entre 100Mb et 1Gb. Pour la première fois, à notre connaissance, des paramètres influant sur les performances des structures 1S1R ont été étudiés au niveau statistique pour des matrices crossbar à haute densité, ainsi permettant la proposition d'optimisations futures et des nouvelles études incluant des nouveaux matériaux et circuits, pour continuer à améliorer les performances des dispositifs 1S1R.

Mots clés: Mémoires vives résistives (ReRAM); OxRAM; CBRAM; sélecteurs OTS; co-intégrations 1S1R.

Acknowledgments

"This is the end, beautiful friend. This is the end, my only friend. The end...", we hear that piece of "The End" by The Doors, while a military helicopter crosses the screen with a tropical forest burning in the background. This scene, appearing in the Francis Ford Coppola film, *Apocalypse Now*; is part of one of the most enjoyable sequences in cinema history. At least for me, it remains as a vivid memory and just now, while I am writing this acknowledgments section, it is playing in my head. I am not sure why. Maybe because they mark the final stage of this writing journey that has been the PhD manuscript. Even if it comes as the very last step, I consider saying thank you one of the most important aspects in life, so here we go.

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I think now I understand why that scene of *Apocalypse Now* was playing in my head. If you have watched the film, you will know it is part of the opening sequence. Legend goes that Francis Ford Coppola was drinking and his brain was racking as he was searching a prologue for the movie, and at some point, the answer became clear: best openings begin with an ending. I am sure the conclusion of these thesis work will be the starting point for many more interesting and exciting things to come. Thank you all.

"... So it's *yerba* and nails. What do you want the nails for?"
"I'm not sure yet," Oliveira said, confused. "Actually, I took down the can of nails and found they were all twisted. I started to straighten them out, but with all this cold, you see... It's my idea that as long as I have straight nails I'll know what to use them for."

-*Hopscotch*, Julio Cortazar, Chapter 41.

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⁽¹⁾This model is a collaboration with Prof. Damien Deleruyelle from the Nanotechnologies Institute (INL) from Lyon

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Outline

This thesis was a collaboration between the IMEP-LAHC and the CEA-Leti. The main objective was to evaluate performances of Resistive Random Access Memories (ReRAM) for Storage Class Memory (SCM) applications through in depth characterization and modeling studies. In particular, speed, endurance and consumption were addressed with an additional focus on access device co-integration, also called selector.

Chapter 1 presents a general introduction to the context and motivation that led to do this research work. Basic concepts and main emerging memory technologies as well as selector topologies are presented. Main challenges of these devices regarding SCM applications are also treated.

Chapter 2 describes the studied samples, the experimental set-ups, used structures and demonstrators, and the methodology to perform the electrical characterizations. Some process details of the analyzed structures are also presented.

With the adequate context, the introduction of the studied devices, as well as the measurement methods, Chapter 3 addresses ReRAM endurance at the array level. Through extensive characterizations, a big variety of programming conditions over considerable populations, variations on the endurance failure are analyzed. They mainly determine the influence of the SET and the RESET pulses on the maximum number of cycles ReRAMs can endure. To explain and better understand the experimental results, a stochastic model based on defect generation inside the filament and during cycling, is presented.

Chapter 4 treats integration of OTS back-end selector with HfO_2 OxRAM. OTS working principle is explained in detail. It is followed by its optimization in order to make it compatible with electric characteristics of the resistive memory. Once made, OTS+ReRAM are characterized to demonstrate functionality and to extract co-integration features. Low leakage currents measured would allow having arrays up to 1Gb size.

As for the Chapter 5, optimized structures from Chapter 4 are integrated in the Back-End-Of-Line (BEOL) of a 130nm CMOS technology. Hence, first reliability and variability studies were conducted and linked to OTS and ReRAM characteristics. Excellent device performances were obtained, notably 10^6 programming, 10^8 reading, and 10^9 read disturb cycles. A semi-analytical model is also presented in order to analyze OTS+ReRAM variability as a complement to the experimental results. Hence, future optimizations are proposed.

A final Chapter briefly synthesizes the manuscript work and presents future perspectives concerning ReRAM technologies and OTS+ReRAM co-integrations.

General Introduction

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DATA is gaining importance in our daily life. It helps us to better understand our world, to predict, to profit, to optimize, etc. A lot of verbs are possible thanks to data. The International Data Corporation estimates that more than 90% of all the data in the world has been generated since 2016 and this trend is expected to be increased by more than 300% by 2025 as presented in the chart in Figure 1.1 [1]. Private and public organizations have been increasing their capabilities of data collection making of Big Data (something that sounded futurist one decade ago) an important sector in the industry. This trend has generated passionate debates (e.g. privacy concerns) around all the information that is collected daily. Just to present two very specific examples, some people can use collected data to model temperature behavior in the pacific ocean, aiming to diminish weather negative effects on population's daily life, when phenomena such like "El Niño" [2] happen; while others can use it to manipulate voters prior to important political elections [3, 4]. As stated before, data can be used to make possible a lot of actions/verbs, even some not very ethical and controversial. Beyond all this, reality can not be denied. Only in the United States, the data market is estimated to more than US\$ 3 trillion per year and a lot of exploitations rest to be implemented [5].

HOW THE AMOUNT OF DIGITAL DATA IS INCREASING

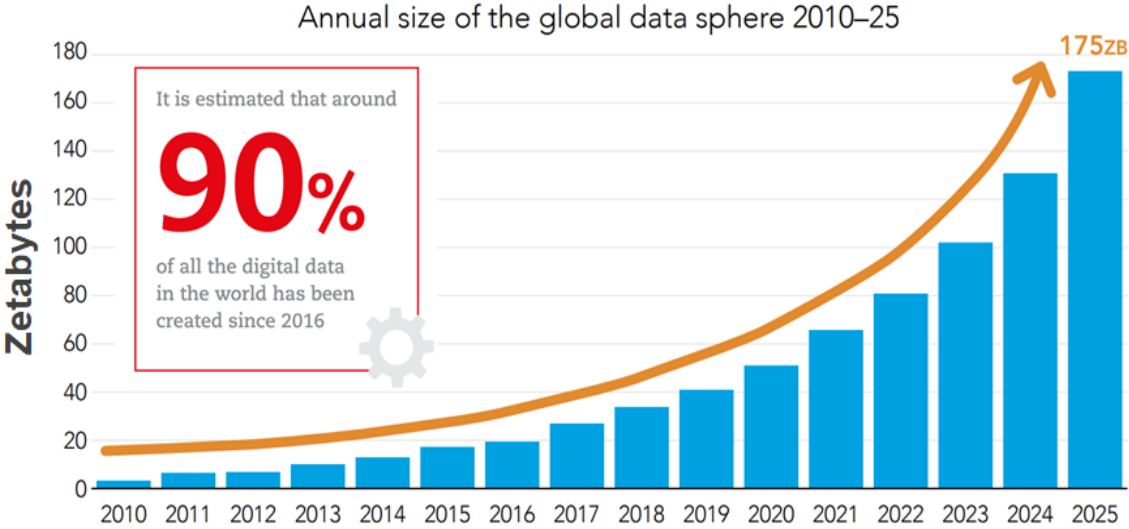


Figure 1.1: Annual size evolution of Internet data. Adapted from: [1]

All this *data-fever* as well as its manipulation is somehow possible thanks to the electronics scaling pace, observed since the transistor invention several decades ago. Thus, computing systems have evolved and more and more devices present data processing and connectivity capabilities (Internet of things-IoT) nowadays. Electronics scaling has enabled modern computing systems to perform Artificial Intelligence (AI) tasks too. For the next years, more reliable, faster and more energy efficient computing architectures will be needed, in order to meet the requirements and to profit the new opportunities that new paradigms that technologies like IoT and AI present.

One of the most critical components of computing architectures is the memory block. This chapter presents, firstly, the diagnostic of the memory market and how the various technologies existing can be destined to diverse applications such as Stand-alone embedded, and a new type called, Storage Class Memories. Precisely, emerging memory technologies will be excellent candidates for the latter. Therefore, a general overview of their diverse types is also introduced: MRAM, FeRAM, Mott-oxides based memories, PCRAM and ReRAM. Being one of the main working subjects of study in this work, a deeper diagnostic is made over the latter. For them, as well as for other emerging technologies, sneak path currents is a main issue if large memory arrays are intended to be implemented. That is the reason why, access devices to suppress such currents, also called selectors, are needed. This chapter also presents their main existing topologies, making an emphasis over the Ovonic Threshold Switching (OTS) selectors, which were co-integrated with ReRAM memories (chapter 4 and chapter 5).

1.1 Memory Context:

In a computer system, performances are dependent on the memory devices as well as the processor technology. In an ideal case, speeds should be equivalents. For a single clock cycle of the CPU, data or instructions stored in the memory should be accessed. This is not the case nowadays. Fastest off-chip memories can be until 1000 times slower than high-end processors [6]. This increasing gap, widely known as the "Memory wall" [7], has led to the optimization of the memory architectures through a memory hierarchy, aiming to reduce access latencies.

Two main technologies are used in computer memory systems: dynamic RAM (DRAM) and static RAM (SRAM). Unfortunately, a perfect memory (fast, cheap and large) does not exist, so the optimization consists in combining a small, fast memory and a large, slower but cheaper memory. The fastest one (SRAM), usually called *cache*, is placed on the same chip with the CPU and contains the most used data and instructions. On the other hand, off-chip DRAMs present higher storage capacities but their operation frequencies are much slower. Down the memory hierarchy, in a so-called tertiary level (see Figure 1.2), Hard Disk Drives (HDD) are used to store large amounts of data, which do not fit into the main memory. The cost per GB in a tertiary storage level is very low but the access time is in the order of the ms, while the access time for a cache memory is around some ns [6]. When a data/instruction is required by the processor, it's firstly searched in the cache. If data is not found in the cache, then the subsequent memory levels are examined. Thus, diverse memory technologies are used in order to optimize trade-offs among speed, consumption, cost and storage capacity [8].

According to their characteristics and applications, two types of memory markets can be distinguished:

- *Stand-alone* applications prioritize performances and storage capacity at low cost per bit. Thermal budgets and power consumption do not represent binding factors, but their optimization is always important.

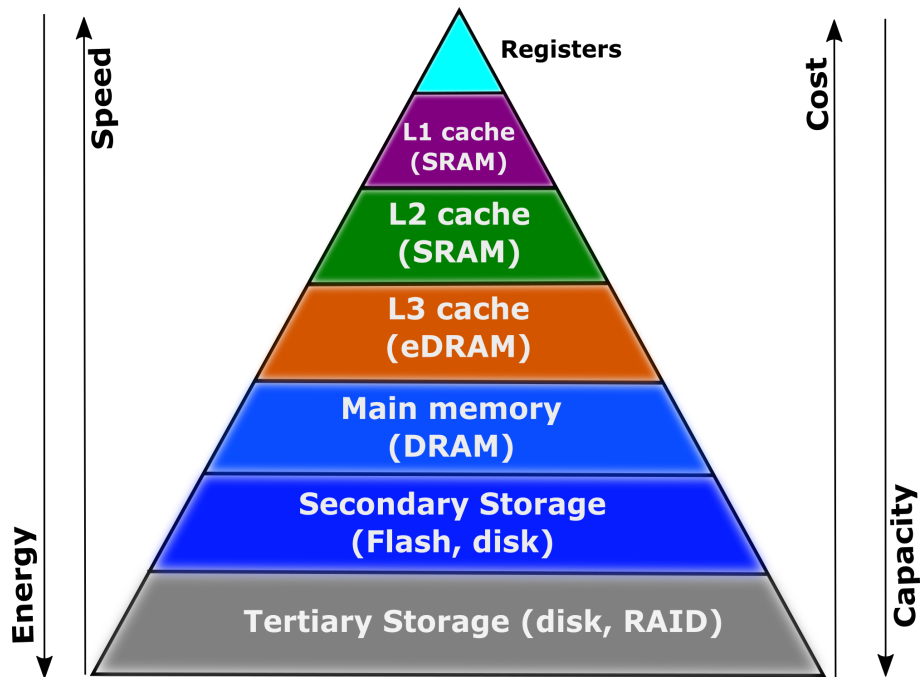


Figure 1.2: Typical memory hierarchy in a Von Neumann architecture. High performance but very costly memories are near from the CPU. On the other hand, low-cost and very much slower storage units are far from the CPU. Typical memory technologies used for every level in the hierarchy are presented too. Sources: [9, 10]

- *Embedded applications* require high speed, high thermal stability, low consumption, high security, and wide bus-width capability. In such systems *memory requirements are specific for each application*. There are mainly two types of embedded systems: Systems in Package (SiP) and Systems on Chip (SoC), which can be Micro-controllers (MCUs) used for smart cards and Microprocessors (MPUs) used in small portable devices. For the former, all the components of the electronic system are integrated in a single chip, whereas for the latter, several functional units can be built over different chips integrated into the same package [6].

Flash memories can be used for both applications. For example, and in the case of stand-alone memories, Flash and DRAM, represent about 90% of the electronic memory sales [11]. Figure 1.3 presents the market share of diverse technologies for embedded and Stand-alone applications.

Another important characteristic of memory technologies is their volatility. They can either be volatile, i.e. information stored on the device is lost once it is turned off, or non-volatile. On the memory hierarchy already presented (Figure 1.2), SRAM and DRAM are volatile memories. On the other hand, HDD and Flash topologies are non-volatile. Thanks to the exploit of mobile devices and applications, the latter has seen an important growth during the lasts lustrums. Solid State Drives (SSD), which are build using flash memories, solve some mechanical problems presented by traditional HDDs. However and for the time being, the cost per GB of SDDs can be several times higher compared with

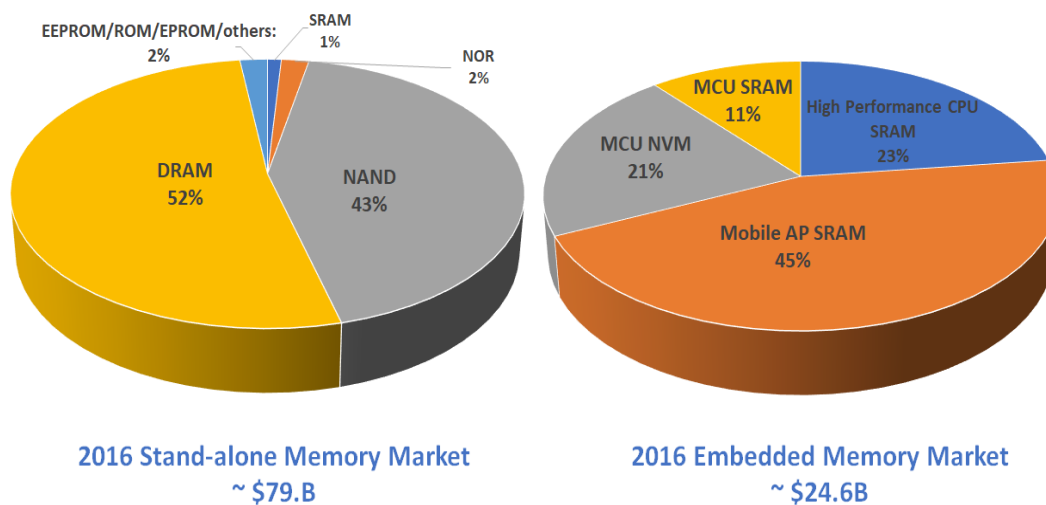


Figure 1.3: Approximative market shares in 2016 for Stand-Alone (left) and embedded applications (right). Source: [11]

HDDs [6].

Although recent 3D architectures development [12] reduces the cost per GB of Flash devices, and ensures some growth in their market share for some years; scaling of this technology faces diverse intrinsic physical issues: high operating voltage, short channel effects, high power consumption, floating gate interference, and coupling between control and floating gates; can be mentioned [13–15]. These technical issues are becoming hard to overcome with time. Therefore, interest in alternative technologies which present low power consumption, less electrons per bit, faster erasing and writing times than flash, and good scalability; has appeared since some years ago.

1.2 Storage Class Memories: a new paradigm

As previously mentioned, one of the most important problems nowadays in computing systems, is to have memory technologies fast enough to provide data at a rate adapted to the processor capabilities. A solution to this issue could be to increase the size of SRAM, but it would imply increasing the surface occupied by the cache memory into the CPU, as well as increasing fabrication costs. Similarly, and even if DRAM offers higher capability than SRAM, its main handicap is its volatility. On the other hand, non-volatile behavior is characteristic of Flash and HDD. However, access time, energy consumption and endurance of such technologies, are very poor. This situation is widely known as the *Memory bottleneck* and technologies that could fill this latency and storage gap are known in literature as Storage Class Memories (SCM) [16]. Having a high endurance, high speed, high scalability, energy efficient and non-volatile memory would represent a revolution in computer architectures.

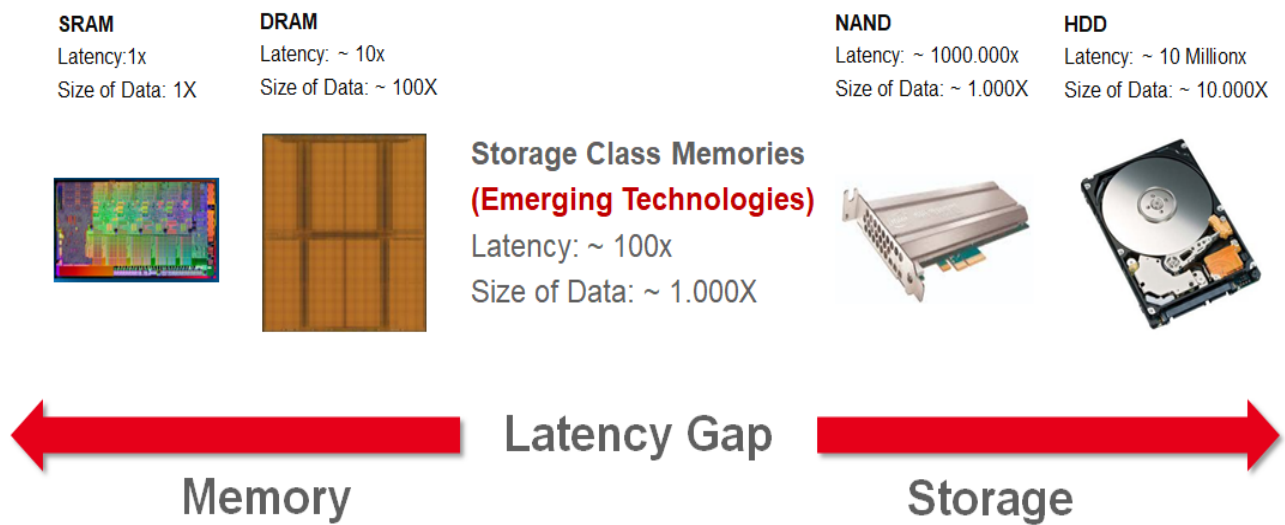


Figure 1.4: Memory hierarchy in terms of storage capacity and latency speed. Values are presented using SRAM characteristics (fastest memory technology in the market) as reference. Source: [17]

SCM, made of emerging technologies, are able to have latency speeds not so far from those one characteristics of DRAM technologies and storage capabilities equivalent to those presented by Flash technologies (see Figure 1.4). They should be able to combine the robustness and performance of SSD with the low-cost characteristics of HDD too [16].

1.3 Non-volatile Memories: emerging technologies for SCM applications

With the necessity of new technologies to solve the very well known memory bottleneck and the definition of SCM devices, this section introduces the main candidates for such applications. Each one of them, presents diverse levels of maturity, given that some factors such as high non volatility, low latencies, high endurance and low cost; represent technical challenges and demand plenty of research at the materials and system level [16]. Some of them are listed next:

- Magnetic Random Access Memories (MRAM, STT-MRAM)
- Ferroelectric Random Access Memories (FeRAM)
- Phase Change Random Access Memories (PCM or PCRAM)
- Mott-Insulators based memories
- Resistive Random Access Memories (ReRAM or RRAM), which are subdivided into

Conductive Bridging Random Access Memories and Oxide resistive Random Access Memories (OxRAM)

Specific physical working mechanisms are inherent to each one of them. They can present a resistance change as it is the case for PCRAM, MRAM, Mott-oxides and ReRAM technologies; or a polarization change as is the case for FeRAM. The ensemble is non-volatile and free of the main limitations of flash technologies: low endurance, high voltage operations and complex erase procedure [9]. Besides, they are implementable in the Back-End of Line, which makes them compatible with the most aggressive technological nodes ($<28\text{nm}$ CMOS) [18]. In the following, a short introduction to these technologies is presented.

1.3.1 MRAM

Magnetic Random Access Memories profit the magneto-resistive effect in thin films. Information is stored in the magnetization orientation of a nano-scale ferromagnetic layer. In 1996, Berger and Slonczewski studied independently the effect of an electric current flowing through a tri-layer structure to switch a nanomagnet [19, 20]. Figure 1.5(a) depicts the schematic view of a typical MRAM cell. The main component of such devices is the Magnetic Tunneling Junction (MTJ), composed of two magnetic layers, a ferromagnetic free layer (FL), and a reference layer (RL). They are separated by a tunneling barrier, which is built from an insulating material (i.e. MgO). The orientation of the magnetization of the FL is modified for the two states. On the other hand, it is permanent for the RL, which is used as a stable reference for the magnetic orientation. When the Free Layer and the Reference Layer have different orientations, the device is in the Anti-Parallel (AP) state (high resistance). For the same orientation, the device is said to be in the Parallel state, characterized by a low electrical resistance [21]. The two states are obtained using different polarization currents as shown in Figure 1.5(b). The FL state determines the MRAM resistance, its magnetoresistance or the free-layer switching fields. Such state can be known applying an electric field lower than the switching ones [22].

When electrons flow through a ferromagnetic layer (FM), spins of the electron current polarize. If thickness of the FM is adequate, polarization is preserved and therefore applied to a second layer. In the second layer, the polarized electrons of the current apply a torque on the local magnetic moment thanks to the transfer of angular momentum. Memory is switched if the torque is large enough to change the magnetic state of the FL. This behavior is known as the spin transfer torque (STT) effect. [21]. That is the reason why, these memories are called STT-RAM too.

MRAM memories present a very high endurance ($> 10^{16}$) (no atoms are moved during the writing operations as it is the case in another emerging technologies such as PCRAM or ReRAM devices), very short programming/read time ($\approx 10\text{ns}$), and good retention (>10 years retention at 220°C was recently demonstrated [24]). Besides, the power consumption is very low. Most recent developments have succeeded to achieve high density unitary cells (1 GB) integrated over aggressive CMOS nodes (28nm FDSOI technology) [25]. All

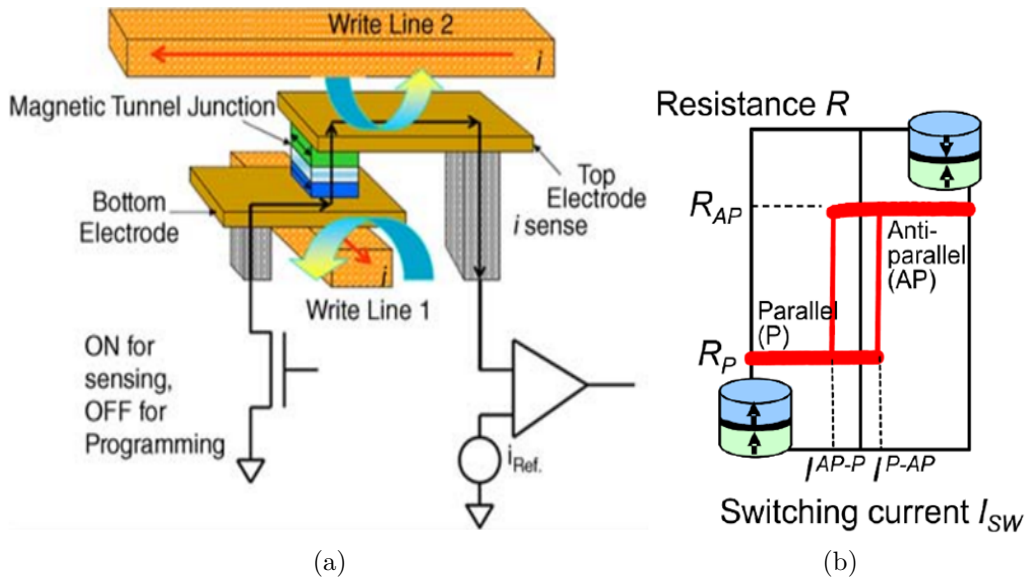


Figure 1.5: (a). Schematic view of a MRAM unitary cell. Normally composed of three layers which compose the Magnetic Tunneling Junction (MTJ): Free Layer (FL), Reference Layer (RL) and insulating layer where tunneling happens. The field is applied using the write line and profits the Spin Transfer Torque phenomenon to generate the two electric states in (b). Difference of polarity generates the Parallel (P) and the Anti-Parallel (AP) Sources: [21, 23]

these factors made of MRAM, strong candidates to replace SRAM memories. However, some issues exist: magnetic memories present large cell size, small memory window, which is the difference between the two resistive states; stack fabrications are complex and not very compatible with CMOS processing, which can degrade the magnetic layers [23].

1.3.2 FeRAM

Ferroelectric Random Access Memories combine fast read and write access of DRAM [26] also providing non-volatile capability. These technologies store information profiting polarization on ferroelectric materials. Thin ferroelectric films are sandwiched between two metallic electrodes and used as capacitors [27]. When an electric field is applied across the ferroelectric material, the states are aligned with the electric field to have the low-energy state. Analogically, the high-energy state is obtained when polarization alignment is anti-parallel to the electric field. Going from the high-energy state towards the low-energy state or vice versa produces energy as a charge and is normally called switch charge (Q_s). Therefore, two $Q(V)$ curves are obtained as a function of the polarization of the electric field applied [28]. An access transistor is used in order to sense the state of the ferroelectric film as presented in Figure 1.6(a), while the typical polarization dependence on the electric field $P(E)$ can be observed in Figure 1.6(b).

For years, the typical ferroelectric material has been Lead Zirconate Titanate (PZT) [26], but recently, other materials such as Hafnium Oxide (HfO_2) have presented ferroelec-

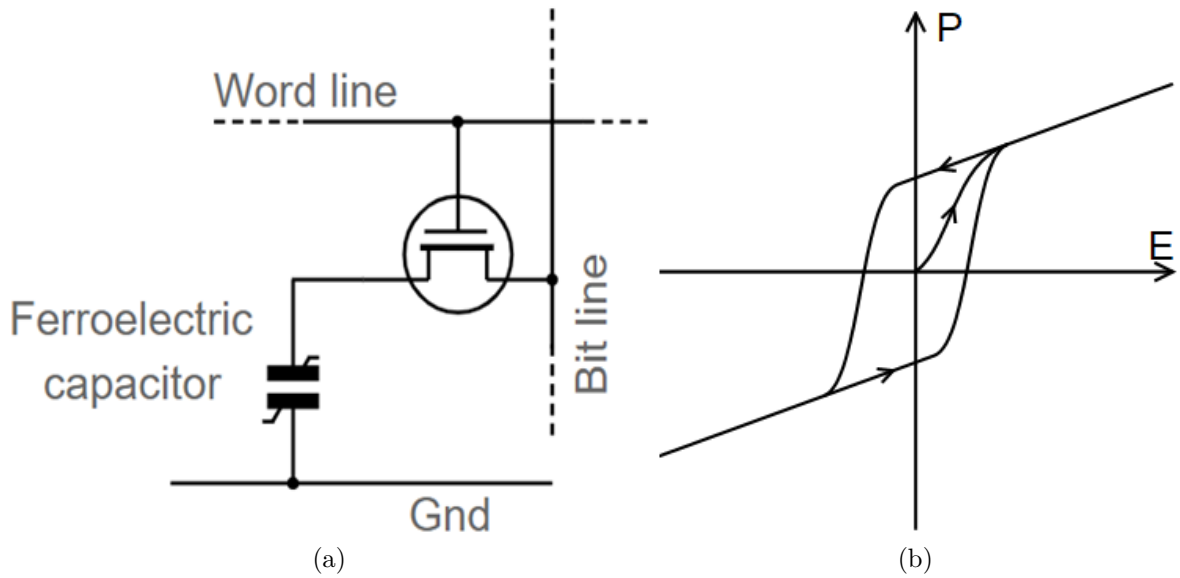


Figure 1.6: (a). Basic structure of a FeRAM cell. A ferroelectric material is used to have a ferroelectric capacitor. A transistor connected in series is used as access device. (b). Two polarization behaviors (charge hysteresis) are obtained using different electric field polarizations. Thus, two voltage levels can be sensed over the bit line during the read operation. Sources: [28]

tric behavior at some specific crystalline phases, renewing thus interest in this technology due to its CMOS compatibility [29]. Hence, three subtypes of FeRAM memories can be distinguished: capacitor based ferroelectric RAM, ferroelectric field effect transistors and ferroelectric tunnel junctions [30].

FeRAM devices endure a high number of write/erase cycles ($\approx 10^{14}$) [26] and present low power consumption. Besides, they can be considered fast technologies, given than the write/erase process is $\approx 100ns$. On the other hand, memory density is not very high due to perovskites complexity. This issue can be solved using Hafnium Oxide as ferroelectric memory as previously mentioned [30]. Another disadvantage of FeRAM devices are the reading methods, which tend to be destructive [26].

1.3.3 PCRAM

Phase-change materials profit the3 high resistivity difference between a crystalline and an amorphous state [31]. The latter is characterized for presenting a high electrical resistivity, while on the crystalline phase, a low resistivity is observed [32]. This effect was first studied by Stanford Ovshinsky in the late 1960s, paving a way for a large variety of data storage applications [33]. Hence, phase-change materials have been used for DVD and blu-ray disks. They are also used for one of the most important emerging technologies for SCM applications: Phase-Change Random Access Memories (PCM or PCRAM) [34]. Access devices such as Ovonic Threshold Switching (OTS) are fabricated using some of

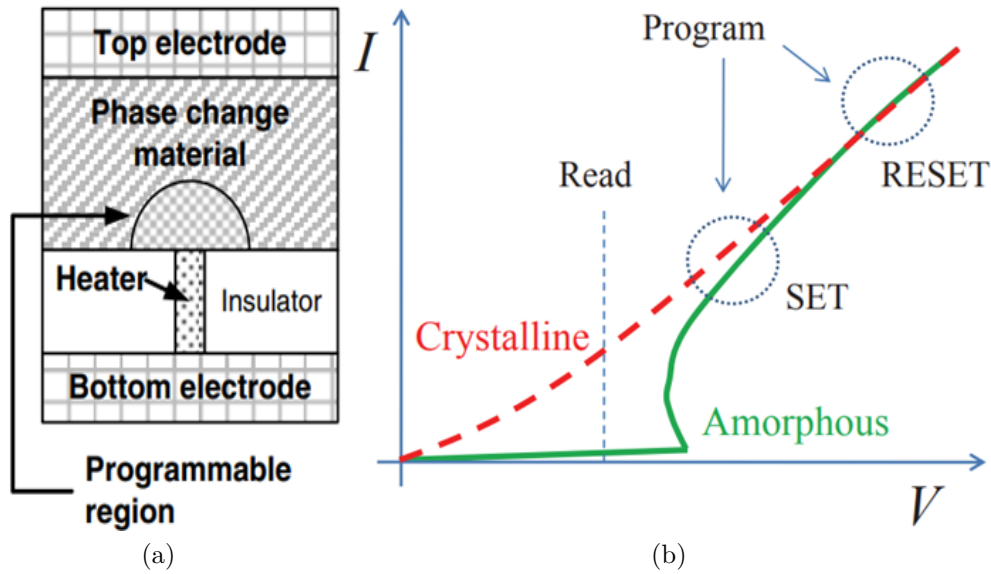


Figure 1.7: (a). Basic structure of a PCM cell. A chalcogenide material is used and resistivity changes obtained through thermal excitations are exploited in order to have a memory effect. (b) Typical I-V curve for a PCM cell. Crystalline and amorphous phases are presented as well as two programming voltages: V_{SET} (to go from the amorphous and high resistive phase to the crystalline phase which presents a high conductivity) and V_{RESET} to program the cell into the amorphous state again. Sources: [34, 35]

the traditionally phase-change materials too, with subtle differences between the working mechanisms of both devices. In subsequent sections, their importance for the emerging memory technologies world, will be treated and explained.

The assortment of materials used for PCM applications include $GeTe$, $GeSeTe_2$, $GeSbTe$ and diverse variants obtained by enrichment of doping [35]. Figure 1.7(a) presents the most-common structure for a PCM cell, called mushroom or T-cell. In there, a phase-change material is sandwiched between a top and a bottom electrode and the programming is made on a "half-dome" region. It means that the phase switching is effectively made over this small portion of the phase-change material. Such portion, called programmable or active region is located over a heater, which provides the thermal energy for the phase-switching, and concentrates the highest temperature due to the highest current density [31].

Figure 1.7(b) depicts a typical current-voltage characteristic of phase-change materials for crystalline and amorphous phases. Going from the amorphous state to the crystalline is called the SET operation, and is achieved by heating the material above its crystallization temperature. On the other hand, the RESET operation is obtained by melting the material and quenching it into the amorphous disordered state. Such processes are effectuated employing unipolar pulses. Low power pulses are used to effectuate the READ operations without losing information. SET pulses tend to have low power than the RESET ones, but imply a longer duration [35].

Precisely, high power used for RESET operations and lower programming time if they are compared with other emerging memories, constitutes the main disadvantages of PCRAM technologies [35]. However, device area miniaturization and material interface engineering are techniques used to reduce currents and power consumption for the RESET operation [36] as well as crystallization rates. As for the advantages, high endurances have been demonstrated for PCM technologies ($> 10^{11}$ programming cycles [37]) and decades of research on phase-change materials make of this one, the most mature emerging memory solution [38].

1.3.4 Mott-Insulators based memories

In 1937, De Boer and Verwey noted that the traditional electronic band theory was not enough to explain the working mechanism of many transition metal oxides, which were expected to have metallic behavior but that in reality behave as insulators [39]. It was later, in 1949, that Nevill Mott proposed a first theory to explain the electron to electron interactions that could be the reason of the insulating states [40] in the so-called Mott insulators. Besides, it has been demonstrated that Mott insulators present phase transitions with drastic changes (hysteresis) in their electrical and magnetic properties. The transitions can be triggered thanks to thermal, electrical or optical stimuli [41]. These properties have arisen the interest on such materials for memory devices applications, placing them in the emerging memory technologies likely to be used for SCM applications [41]. Same stoichiometries can present volatile [42] and non-volatile behaviors [43], with different thermodynamic driving force at different temperatures [41]. Volatility is defined by the doping, the applied current density, and the stacks symmetry [44].

Compared with another emerging memory technologies, Mott-insulators present more or less equivalent performances in terms of switching speeds and access times. On the other hand, thermal reliability (i.e. retention performances) and memory window (difference between the high resistivity and the low resistivity state), need to be improved. Many physical and reliability understanding also lack and need to be studied [41].

1.3.5 Resistive Random Access Memories

Resistive Random Access Memories (ReRAM) are based on a resistive and non-volatile switching phenomenon, which occurs in an insulator sandwiched between two metal electrodes when an electric field is applied [45, 46]. This electrical behavior was first reported in the 1960s and was largely studied until the early 1980s for memory device applications [47]. At the time being and due to unfavorable performances such as poor endurance and high operating voltage, they were abandoned until some years ago, when progress in material science allowed to have improved performances, making of these technologies an attractive candidate to replace FLASH technologies [47]. Hence, interest was refreshed with the IV hysteresis studies over perovskite oxides such as *PrCaMnO₃* [48], *SrTiO₃* [49], *SrZrO₃* [50], among others. In 2004, Samsung Electronics demonstrated NiO ReRAM array integrated with a 180nm CMOS technology [47]. It opened the door

for a new research boom over binary oxides such as TiO_2 , ZrO_2 and HfO_2 [47]. In 2008, HP labs linked the working mechanism of resistive devices to memristor theory [51]. Since then, ReRAM technologies have been one of the most studied emerging memory candidates due to its materials simplicity and the good compatibility with CMOS technologies in the back-end of line (BEOL) [52].

Resistance change in ReRAM is due to electrochemical process that allows the migration of metal cations or oxygen anions to create a conductive filament (CF). Through the application of voltage/current pulses, such filament can be created or erased inducing a resistance change of the insulator material [53]. It means that two ReRAM states are differentiated but a third one can be named in a standard operating behavior (pristine state). The three of them are presented next:

- A highly resistive state which is inherent to fresh samples and called the pristine state too. To trigger the switching behavior of the subsequent cycles, a large voltage is required in a process commonly known as "forming". Once the forming is made, a conductive filament is generated.
- The Low Resistance State (LRS) or written state occurs when a conductive filament links the two metallic electrodes. As stated before, going from the pristine state to the LRS is named forming. On the other hand, going from the erased state to the LRS implies a SET operation.
- On the High Resistance State (HRS) or erased state, the filament is removed from the insulator layer through a RESET operation.

As for the layers structure, an example of it is presented in Figure 1.8(a). It consists of at least three layers. Two electrodes: top and bottom electrode, TE and BE respectively; and a resistive layer sandwiched between them. In some cases, an inter-facial layer can be used to improve ReRAM performances [54].

1.3.5.a ReRAM classification

Resistive memories are commonly assorted according to:

- **I-V characteristics.** Two types of ReRAM can be found: bipolar or unipolar devices. Both behaviors can be appreciated in Figure 1.8(b). For an unipolar characteristic, the electrical response of the resistive memory is independent of the polarization that presents the voltage applied. Conversely, bipolar memories have an asymmetric characteristic and the polarity determines the resistive state of the ReRAM. The RESET operation occurs at the reversed polarity of the SET operation. Conventionally, the latter is assumed at the positive bias, which means that the HRS state is obtained applying negative biases.

The I-V characteristics are not intrinsic to the insulating layer used. Such behavior is determined by the electrode materials used. It means that the same oxide layer can

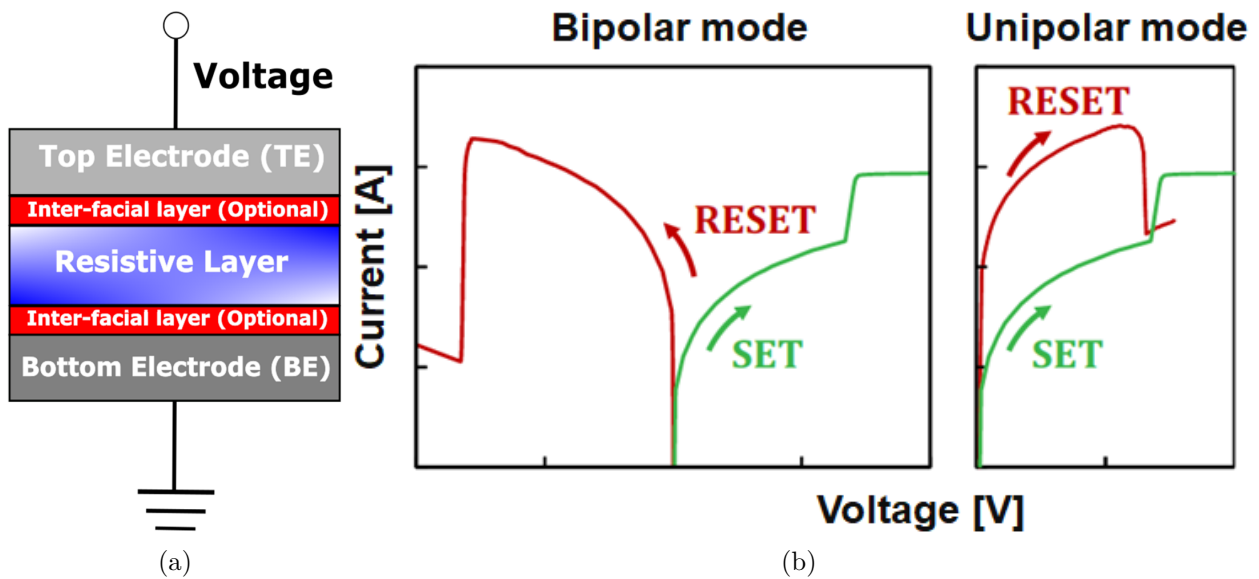


Figure 1.8: (a). Basic structure of a ReRAM cell. A resistive layer is used in order to have non-volatile resistance changes through electrical stimulus (b). Bipolar and unipolar behavior of ReRAM technologies Source: [55]

present both unipolar or bipolar switching as a function of the electrode materials used for the ReRAM stack. Unipolar behavior is obtained using noble metals such as Pt in the top and bottom electrodes. On the other hand, if oxidizable materials such as Ti and TiN are used for any electrode, a bipolar I-V characteristic is obtained [53].

Generally, unipolar ReRAM, require higher currents for the RESET voltages and present also larger variabilities than bipolar devices. This is the reason why, research and development nowadays is mainly centered in bipolar ReRAM [53].

- **Operation principle and device physics** OxRAM, CBRAM and Hybrid devices. The next subsections present more detailed explanations in agreement with this classification type.

CBRAM

Conductive Bridge RAMs are bipolar devices and their functioning is based on the electro-migration of metallic ions inside an oxide material. It implies the formation of a conductive filament composed of these metallic cations. This process (SET operation) can be divided in three consecutive steps: oxidation, migration and reduction [56, 57].

For the oxidation stage, free ions from atoms at the TE interface (see Figure 1.8(a)), are created. To achieve such oxidation reaction, the TE metal has to be electrochemically active (i.e. Ag [58], Cu [59]). Traditionally, this reaction has been linked to the Buttlerville equations [60], which are used to explain such behavior. Once the ions are created,

they begin to migrate through the resistive layer towards the BE. This migration is possible thanks to the electric field applied and can be explained through a Mott-Gurney ionic transport [61]. The resistive layers need to be chosen in order to allow the ions migration coming from the top electrode. Typical examples are: GeS_2 for Ag [62] and Al_2O_3 for copper based TE [63]. Once the ions reach the BE, they are reduced. The gradual increase of incoming ions generates that a conductive filament begins to form between the two electrodes, hence reducing the insulating gap. Once, the electric filament has grown enough to contact the BE, the cell switches into the ON-state and its conductivity is dramatically increased. The cell retains its ON-state unless an electric field of opposite bias is applied and the electrochemical dissolution of the conductive filament appears.

For the RESET process, an electrical current and an electrochemical current are present and parallel inside the device. The latter receives the name of Faradic current and is responsible of the conductive filament dissolution [57]. At this point, it is important to state that the BE material needs to be different from the TE one, in order to avoid its dissolution during the RESET operation (ions from the BE migrating towards the TE in an analogical way to the SET process). The RESET process is a thermochemical phenomenon mainly due to the high current density that appears on the CF that is being erased [64].

The whole mechanism of electro-migration of metallic ions is summarized in Figure 1.9.

OxRAM

In Oxide-based RAM (OxRAM), oxygen vacancies displacement is at the origin of the resistivity changes. These devices rely on valence and microstructural changes and can present either bipolar or unipolar behavior. As in the case of CBRAM, a conductive filament is created and erased inside the insulating layer to generate the two conductivity states. The difference is that for OxRAM memories, the filament is composed by oxygen vacancies (V_O). Most of them, use transition metal oxides such as HfO_2 , Ta_2O_5 and NiO [13, 65, 66]. The cells require rich defect materials in order to supply the oxygen vacancies. To do this, oxidizable electrodes (i.e. Hf , Ta , Ti) or depleted resistive layers in oxygen, are used [67–69].

The oxygen vacancies are first created by the forming operation which has the role to redistribute them inside the insulating layer. These vacancies are positively charged and their migration is possible thanks to electric field stimulus. Through their removal and placing inside the insulating layer in the RESET and SET operation respectively, the memory behavior is possible. The process of creating the CF is very similar to the oxides breakdown, but given its reversibility, is commonly known as a Soft Breakdown [70].

Figure 1.10, presents a summary of the main steps undergoing on a typical bipolar OxRAM. In the same way as for CBRAM devices, a high current density for the RESET process accelerates the thermal heating of the filament and its consequent destruction [71].

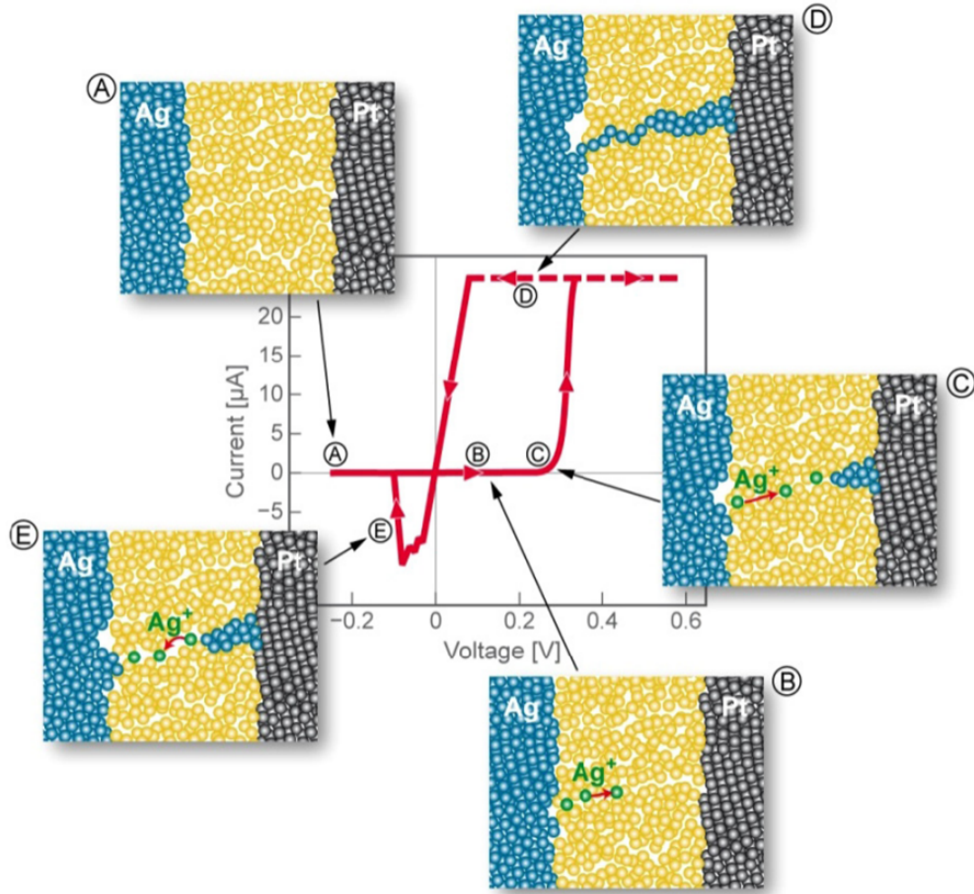


Figure 1.9: SET and RESET for CBRAM devices. Switch is based on electrochemical processes where metallic cations form non-volatile but erasable conductive filaments. Schematics shows a Ag TE and a Pt BE. Source: [57]

Hybrid devices

Hybrid ReRAM are CBRAM based memories where oxygen vacancies V_O are introduced inside the electrolyte to improve performances. In this type of memories, V_O can improve the percolation of the metallic ions inside the oxide reducing the switching voltages. A typical hybrid stack consists of a Cu TE with a HfO_2 insulating layer. Pristine resistances can be reduced, but this implies that the memory window (difference between the LRS and HRS median values) is reduced too. On the other hand, endurance can be improved [72–74].

1.3.5.b Conduction models and working mechanisms of ReRAM technologies

To understand the physical processes taking place in resistive memories, it is necessary to categorize them into the most relevant ones. These are, the conduction mechanisms in the HRS and the LRS as well as the kinetics of the switching phenomena. Such characteristics have been the traditional development axes to propose a diversity of ReRAM models. This

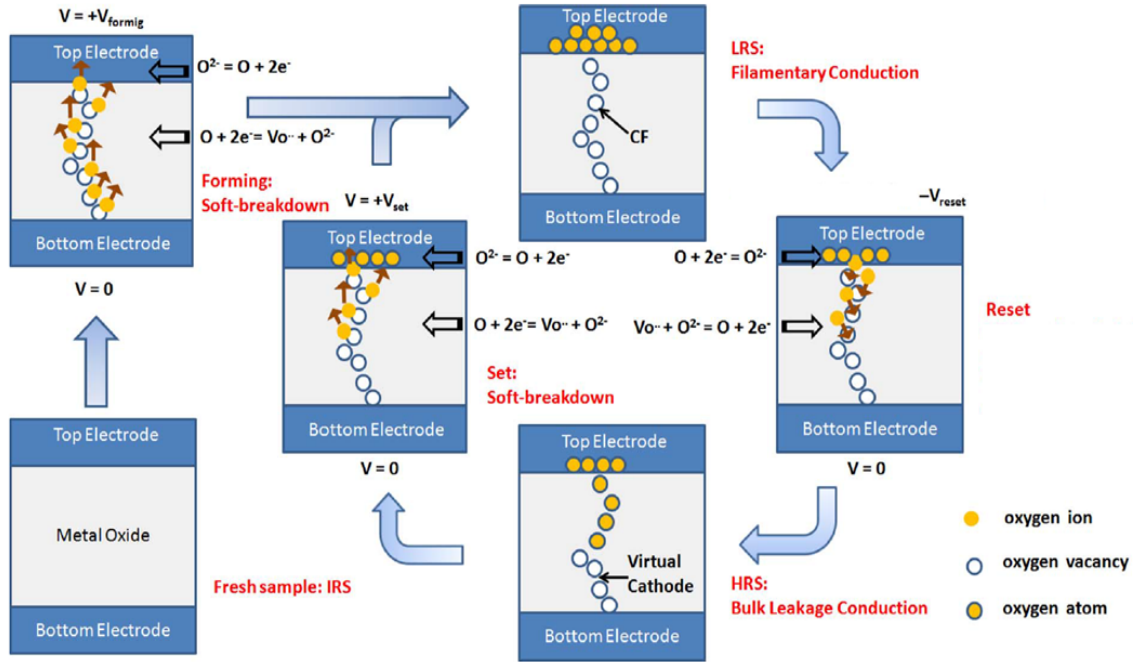


Figure 1.10: Schematic process of the switching mechanism in oxide-based RAM (OxRAM) devices. Taken from: [70]

section summarizes some of them, where evidently, the working mechanisms of OxRAM and CBRAM memories are included.

Resistive memories are based on the switching properties of dielectric films, which present specific interactions (physical processes) under electrical stimulus, with the electrodes surrounding them, in order to have non-volatile and reversible states. Such dielectric materials present insulator characteristics, with a large band gap ($> 3 eV$) and low electrical conductivity [75]. The conduction current of dielectric films when normal electric field is applied is very low. However, under high electric fields, current begins to increase, thanks to diverse conduction mechanisms. Under this scenario, it can be affirmed that dielectric materials are an extreme case of semiconductors [75].

To study the conduction current going through the dielectric film, the considered structure is extremely important. In the case of resistive memories, a MIM structure (Metal Insulator Metal) is the analyzed case. Since different materials are used for the top and bottom electrodes, asymmetry among the metal-dielectric interface barriers appears. This leads to different work functions and therefore, different *bending* between materials in order to satisfy the thermodynamic equilibrium. Band bending in turn, affects the quantum mechanical barrier shape [75].

Electronic conduction mechanisms

Resistive Memories applications can be either ionic, electronic or mixed ionic-electronic (Hybrid devices) materials [76]. Electrical conductivity changes with the states of the

resistive memory and as a function of the conduction mechanisms taking place inside the dielectric layer. They are classified between electron-limited and transport-limited or bulk-limited. For the former, the dielectric-electrode interface determines the conduction mechanisms as for the latter, they depend on the dielectric properties itself. Regardless of the resistive state, various phenomena are always present in a simultaneous way with a different balance. Such balance changes when switching occurs, depending on the electric field, voltage polarity or the temperature. However, most of the time, a dominant mechanism is present, but with switching and current densities changing, such dominant mechanism changes too. A diagram of the conduction processes is presented in Figure 1.11, while an illustration of them can be found in Figure 1.12 [75, 76]

- **Electron-limited conduction mechanisms.** As mentioned before, these kind of conduction mechanisms depend on the electrode-dielectric barrier where the most important parameter is the barrier height at such interface. Another relevant factor is the effective mass of the conduction carriers. These type of mechanisms include Schottky or thermionic emission, Fowler-Nordheim tunneling, direct tunneling and tunneling from cathode to the dielectric traps ⁽¹⁾. While current due to direct tunneling is temperature independent, that one produced by Schottky emission is very dependent on the temperature.
- **Bulk-limited conduction mechanisms.** In this case, the behavior is determined by the trap energy level of the oxide, traps spacing and density, drift mobility, density of states in the conduction band, and the dielectric relaxation time. For the bulk-limited conduction mechanisms, emission from trap to the conduction band, Poole-Frenkel emission, which is a type of Fowler-Nordheim tunneling; trap to trap hopping and tunneling from traps to anode; are included [75].

As mentioned before, for CBRAM devices, ion hopping is the dominant conduction mechanism and it is determined by the Mott-Gurney equations [61]. A characteristic field E_0 , determines the behavior of the ionic current, which can be electric field or temperature dependent [76].

In the case of OxRAM devices, several tunneling mechanisms take place. When the device is a perfect insulator (pristine state) and there is no presence of electrically active defects, conduction is governed by the direct tunneling. Once such defects are generated, through electric field application, further band bending appears and electron transmission is increased, leading to current increase. Moreover, if the barrier shape is degenerated to a triangular shape, a Fowler-Nordheim conduction regime appears. This in the case of non ultra-thin oxides ($>2\text{nm}$), where direct tunneling will be still dominant [75]. A transition can make an electron to surpass the energy barrier enhanced by temperature. In that case, a Schottky emission occurs.

⁽¹⁾A trap is a location inside a semiconductor or insulator that restricts the movement of electrons or holes. It can be a chemical impurity or an imperfection in the regular spacing of the atoms that make up the solid [77]

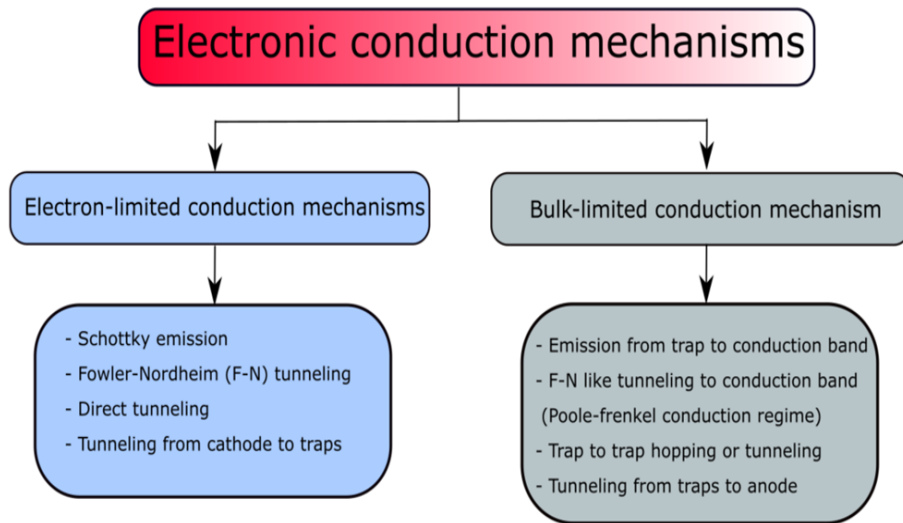


Figure 1.11: Types of conduction mechanisms taking place inside dielectric films which include ReRAM memories. Adapted from: [75]

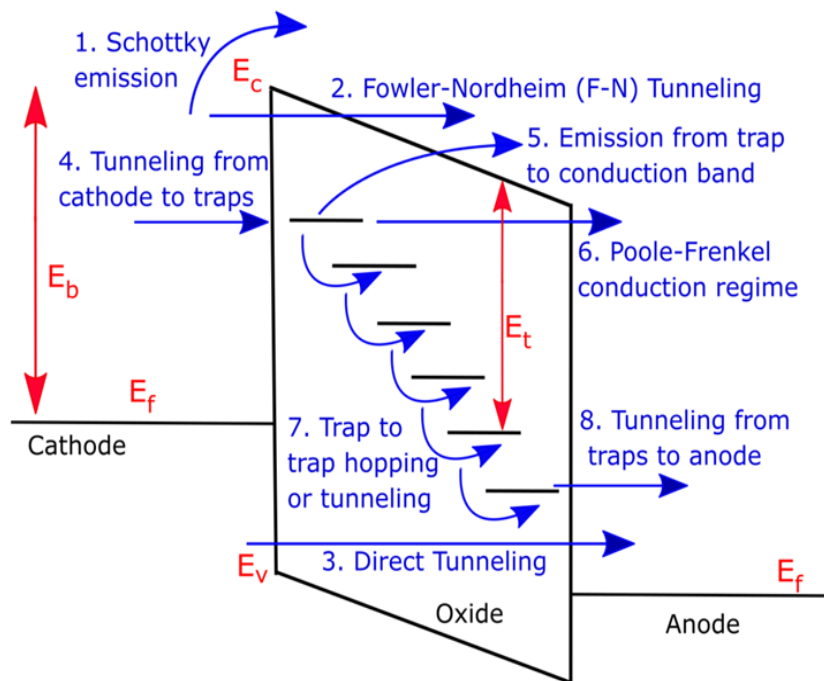


Figure 1.12: Possible conduction mechanisms taking place inside resistive memories. Adapted from: [78]

Another mechanism used to explain conduction in OxRAM devices is the Poole-Frenkel regime [79–81]. There, an electron is excited into the conduction band through a trap site. This is originated by the presence of charged defects which lower the effective barrier height seen by electrons around a specific trap [75]. This conduction regime will be used in further chapters to estimate OxRAM currents in the OFF state.

Switching process and characteristics

Understanding the switching process is essential in order to improve resistive memories reliability, to control, and to predict device scaling. Due to insufficient stability and non-efficient energy consumption of unipolar devices, bipolar ones have gained considerable attention [82]. This is the reason why, the switching explanations presented in this section are mainly focused on bipolar ReRAM. All these characteristics are most known as switching kinetics and normally two aspects are limiting for the switching processes: *ionic transport* (where the Mott-Gurney equations are an example) and *electron transfer reaction*, which occurs at the electrode-insulator interface. These two mechanisms are temperature and electric field enhanced [76].

One of the additional factors that can be rate-limiting are *phase transformations*. They can be induced by local redox reaction and ion depletion. Its velocity is depending on an activation energy and can be temperature dependent. These are some of the reasons of the switching non-linearity once local Joule heating appears.

Concerning the switching characteristics, voltages required to effectuate either RESET or SET processes are dependent on the precedent programming state. As for the switching currents, their equivalence $I_{SET} \sim I_{RESET}$ has been validated thanks to experiments as depicted in Figure 1.13(a) This empirical relation is explained by the non-linearity of the switching events, the I-V behavior of the LRS, and the weak dependence on materials properties, such as activation energies and diffusivity of the RESET switching voltage [83–85].

In the case of the SET operation, the conductive filament (CF) geometry and the chemical composition of the depleted gap, lead to a correlation between the initial state R and V_{SET} [85]. On the other hand, various set resistances can be obtained as a function of the SET current (See Figure 1.13(b)).

Moreover, switching values present a strong dependence on the applied pulses too. Diverse HRS and LRS states can be obtained modifying the pulse characteristics or the compliance current. Every switch is related to a pulse width and amplitude. For example, increasing the pulse amplitude, will require a shorter time to make the device to switch [76].

1.4 SCM: a new memory market

As presented in precedent sections, emerging memory technologies open the door to improve the general performances of computing systems through the so-called *Storage Class Memory* applications; which could mix the high performances and robustness with the low cost and storage capacities of flash memories and hard-disk drives, respectively [86]. To this end, some techniques have been historically proposed and explored. Among them, 3D integration, high parallelism of multiple memory layers, and several bits stored per cell (mostly known as multi-levels per cell MLC), can be found [16].

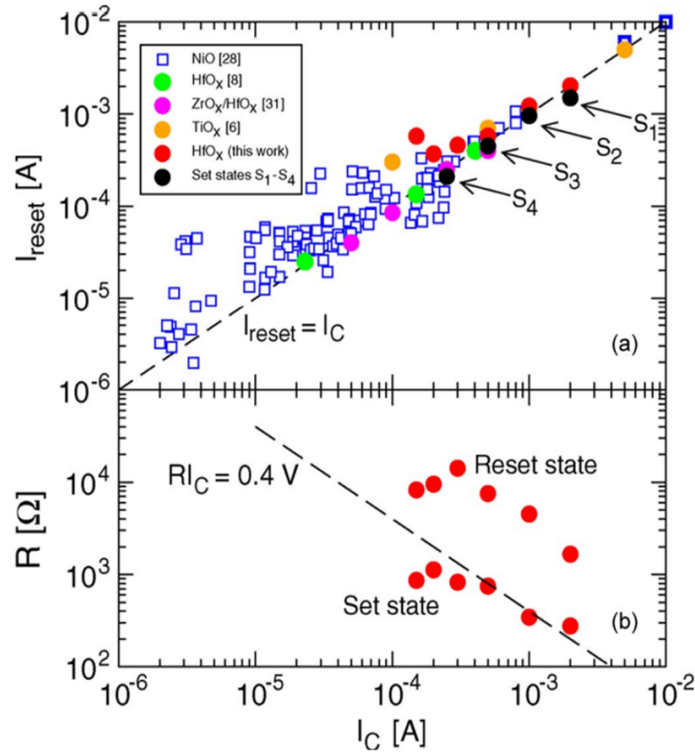


Figure 1.13: (a). Empirical demonstration of the equivalence between RESET (maximum current before switch into the OFF state) and SET current (compliance I_C). Various materials are compared (b). Set and reset resistances as a function of I_C . Compliance current determines the CF cross section, I_{RESET} and LRS/HRS values. Taken from: [85]

SCM are usually classified into two subcategories, as a function of the latency time and the storage capacity inside the memory gap between DRAM and Flash technologies:

- **Memory-type SCM [16]** The M-type SCM are latency closer to DRAM memories. They would add lower power/GB, good retention to DRAM systems, and could be used to provide full recovery from crashes or power outages. Due to its proximity to DRAM memories, high cycling endurance is required.
- **Storage-type SCM [16]** The S-type SCM applications main objective is to have similar densities to those of flash technologies, but with a much faster access time, new direct overwrite and random access capabilities. This could allow simpler and more energy efficient systems. As for the other performances such as retention, it needs to be at least equivalent.

Some of the most important requirements for both of the subcategories of SCM applications are summarized in Table 1.1. Through very specific requirements and direct comparisons with existing technologies, some conclusions can be inferred in order to know which emerging technologies are more adapted for specific applications. These *targets*, are defined in order to make of M-type and S-type real competitors and real innovations that could fill the memory gap and solve in some way, the memory bottleneck.

Table 1.1: Target device and system specifications for Storage Class Memory Applications. Taken from: [16]

Parameter	Benchmark			Target	
	HDD	NAND Flash	DRAM	Memory-type SCM	Storage-type SCM
Read/write latency	3-10 ms	$\sim 100\mu s$	<100 ns	<200 ns	1-5 μs
Endurance (cycles)	Unlimited	$10^3 - 10^5$	Unlimited	$> 10^9$	$> 10^6$
Retention	>10 yr	~ 10 yr	64ms	>5 d	~ 10 yr
ON power (W/GB)	0.003-0.005	~ 0.01 -0.04	0.4	<0.4	<0.10
Standby power (% of ON power)	~ 52 -69 %	<10%	$\sim 25\%$	<5%	<5%
Areal density	$\sim 10^{11}$ bit/cm ²	$\sim 10^{11}$ bit/cm ²	$\sim 10^9$ bit/cm ²	$>10^{10}$ bit/cm ²	$>10^{10}$ bit/cm ²
Cost (US\$/GB)	~ 0.1 -1.0	2	10	<10	<3-4

1.5 3D Architectures

Reaching high-density and low-cost per bit memories, has always been one of the most important challenges for semiconductor industries. The trend needs to be constant, in order to answer market needs. This is not the case for flash memories, where, since some years ago, a slow down of such trend has appeared, making of them one of the roadblocks in the computing systems evolution [87]. This issue is mainly caused by scaling saturation where physical problems have been found: high operating voltage, short channel effects, high power consumption, floating gate interference, and coupling between control and floating gates [13–15]. Such factors make it difficult for flash technologies to scale below 20nm half-pitch [87–89].

To continue with the high-density and low-cost trend, overcoming some of the physical issues mentioned before, traditional planar configurations are intended to evolve into 3D architectures. Since the first propositions [90–92], 3D NAND Flash memories have continued to progress until nowadays, where, for instance, up to 128 layers are stacked and capacities of 512 GB, with 3 bits/cell have been reached [93]. In order to keep competitive and a feasible alternative, this path has been undertaken by the emerging memory technologies too. In the case of interest for this thesis work, ReRAM, as well as for other candidates for SCM applications; two main approaches have been traditionally proposed. The first one of them is the *3D crosspoint*. In there, metal lines are orthogonally crossed and memory points are formed in the respective intersections [94, 95]. On the other hand, in Vertical ReRAM *VReRAM*, multilayers are formed and stacked simultaneously [96–98]. For the latter, a similar approach to the 3D stacking used for flash technologies is used [99]. Both types of 3D ReRAM architectures present $4F^2$ dimensions (minimum achievable cell size, where F is the minimum feature size [100, 101]). A schematic depicting them is presented in Figure 1.14.

From a fabrication cost perspective, Vertical ReRAM is cheaper than a crosspoint architecture. Many layers can be formed simultaneously, which makes the number of masks

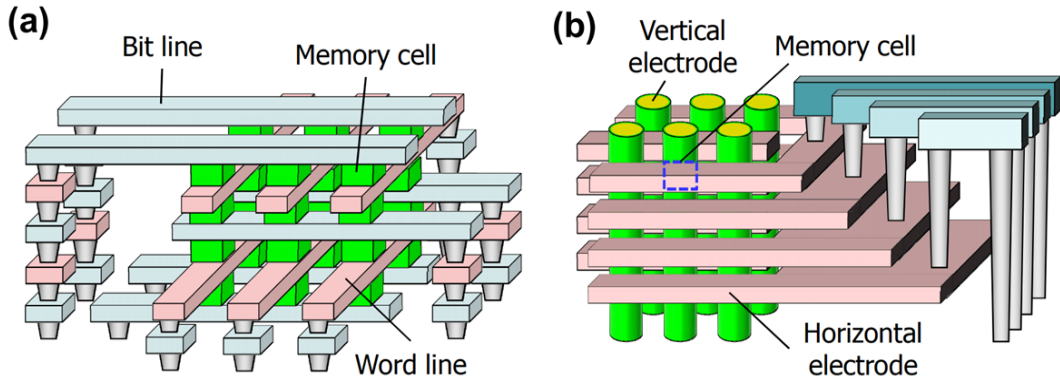


Figure 1.14: Schematics of (a). 3D crosspoint ReRAM and (b). Vertical ReRAM (VReRAM) [99]

and the process steps, independent of the cells stacked [99]. However, the use of stacking layers increases process complexity once the number of levels becomes considerably high. At some point, big uniformity and accuracy is required all along the sidewalk of the vertical structure, hence limiting available materials and deposition techniques [102].

In the case of crosspoint architectures, a higher density efficiency can be reached since peripheral circuits can be placed below the array itself. The process complexity is reduced but compared to VReRAM, fabrication costs remain higher. Expensive lithography and double patterning technology (DPT) are unavoidable for circuits implemented on the most aggressive technological nodes ($<28\text{nm}$) [99].

The most important advantage of crosspoint architectures over VReRAM ones, is the leakage current management. This characteristic is introduced and explained next.

1.5.1 Sneak path current in 3D Architectures

As observed in Figure 1.14, same metallic lines, Bit and Word lines in the case of crosspoint architectures, and vertical and horizontal electrodes in the VReRAM one, are used to connect various memory points. It means that having access to any small subset of the array, when performing reading or writing operations, implies the appearance of leakage currents coming from the non-selected devices. Therefore, in a well reliable and energy efficient system, a high non-linearity between the current flowing through selected and non-selected cells, is essential. In the case of ReRAM memories, non-linearity is the ratio between HRS and LRS currents. For most of the resistive memory stacks proposed and studied in literature, intrinsic ReRAM non-linearity is not enough if dense 3D memory arrays are wished [103]. This is the reason why, it needs to be added through a series connected device which is widely known as *selector*. It reduces the sneak path currents, hence increasing the selected to non-selected cells current ratio. Main selector devices, technical requirements, benchmarking and analysis are presented in the subsequent section. They are another key element of this thesis work given that a co-integration with ReRAM stack was developed and studied (chapter 4 and chapter 5).

In a crosspoint architecture, every intersection is a memory point, which facilitates the inclusion of series-connected embedded selector devices, implying an advantage in lateral scaling if compared to VReRAM architectures [99]. Important reduction of leakage and the capability of addressing specific memory points make of crosspoint three dimensional arrays, more energy efficient approaches. Moreover, this type of 3D architectures are likely to become important actors on the memory field, thanks to the products introduced by the Intel-Micron partnership a few years ago (See Figure 1.15). They claim to be 1000 times faster, 10 times denser, and with 1000 times more endurance than NAND flash [104]. Their introduction in the market is not expected to be a big issue. Hady *et al.* [105] ran a series of system level analysis in order to study which could be the inconveniences of using this low-latency storage memories inside actual computing systems. Some guidelines are proposed in order to ensure adaptability of software and hardware to crosspoint technologies.

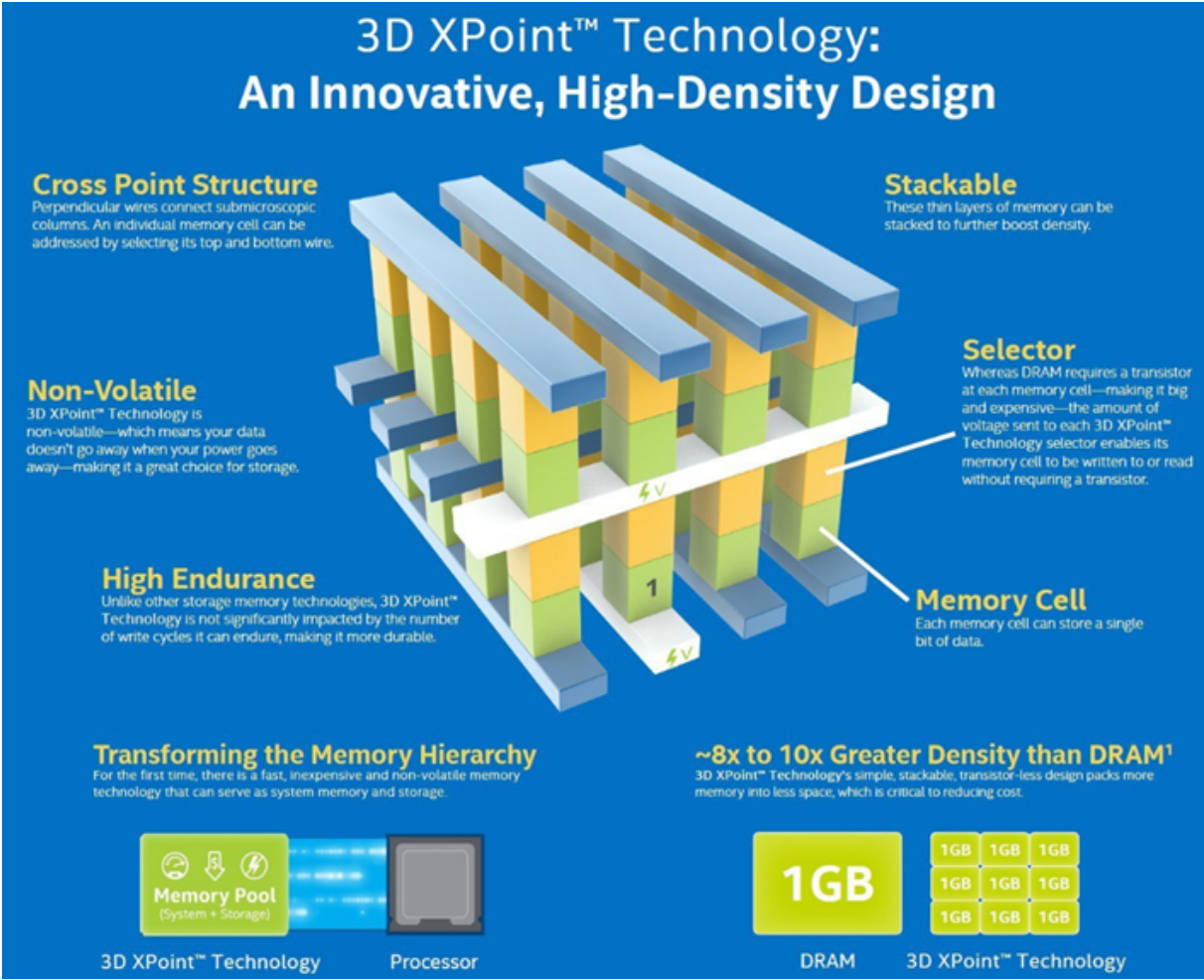


Figure 1.15: 3D X-Point (read crosspoint) technology presented by Intel/Micron in 2015. Taken from: [106]

All these reasons, make of crosspoint systems a more likely candidate to be the mainstream 3D architecture to prevail in the market for implementation of large arrays of non-volatile emerging memories. This is why, only them will be studied for the one selec-

tor one resistance (1S1R) co-integration presented and developed during this PhD work.

1.6 Selector devices for crosspoint three-dimensional systems

Thanks to a considerable number of works [107–110], the necessity of a high non-linearity (NL) for every cell in a crosspoint architecture has been extensively demonstrated. Without a strong one, it is almost impossible to implement arrays of any sizes [111]. In an ideal case, such NL should allow to access a subset inside the arrays to perform write/read operations without adding extra power coming from the unselected cells, which should remain totally unperturbed too.

There are two main methods to obtain this considerable non-linearity. First one of them consists in adding it as a request for the memory itself and developing a high non-linear memory technology. A second strategy is simply adding NL through an access or selector two-terminal device, connected in series with every NVM of the crosspoint array. Using this strategy, memory and selector can be optimized separately and co-integrated, hence representing an advantage and a disadvantage too, given that finding totally electrically and process compatible devices can be a complex task. Besides, co-integration of the two devices implies additional steps, such as expensive lithography [111].

The most elegant solution remains the first approach and some works have been developed [112–117] in that direction. However, strong NL, essential to develop very dense crosspoint arrays has not been found, without degrading, for example, other performances of the memory technologies. Using access elements is still a very good alternative to reduce leakage currents in 3D arrays. Some of the target specifications and critical characteristics for such devices are summarized next [111]:

- **High ON-state current density**

The selector device must be able to bear current densities adapted to those required to program the memory device either for the SET or the RESET processes. These currents must be in the order of several MA/cm^2 .

- **Low OFF-state leakage current**

This characteristic determines selector's capacity to reduce sneak-path currents. The unselected cells will present a leakage current equivalent to the selector OFF state current, which determines the circuit performance, the read/write margins and the power consumption. A good selector device presents a ON/OFF current ratio of several orders of magnitude and therefore, a high non-linearity. These metric is dependent of the programming current required by the memory technology as well as the polarization strategy used to read and write the memory points inside the crosspoint array. Therefore, when comparing selector technologies through NL estimations, these details are very important, given that the same conventions are

not used by all the authors.

- **Process compatibility**

In order to have multi-stack arrays, selector devices must be compatible with the back-end-of-line (BEOL) processes. Given that peripheral circuits that are ideally placed underneath the crosspoint array are needed, selector devices should be also CMOS compatible. As a consequence, materials such as Au, Pt, etc, should not be used for the selector fabrication [103]. Moreover, the thermal budget of the access device and the memory element, must be compatible too.

- **Symmetric current-voltage behavior**

Bipolar ReRAM presents better cycling reliability and are more power efficient [53]. This means that the access devices embedded with this type of resistive memories, need to be able to operate in bidirectional mode (i.e. IV curves are preferred to be symmetric).

- **Electrical compatibility with the memory cell**

Resistive memories have their own voltage and operation currents, which vary as a function of the materials used for the memory stacks. It is important that the access devices presents similar electrical characteristics in order to improve reliability and power efficiency in the crossbar array.

- **Two terminal device**

Ideally, the access device must be a two terminal one, in order to elude extra cell area that avoids achieving the minimal effective surface $4F^2$. This is the case of transistors used as selector devices, where performances are superlative, but their use implies density reduction and process complexity added [103].

- **Better performance than the memory element**

It is clear that access devices should not limit overall memory performances. That is why, characteristics such as endurance, switching speed and variability should be at less equivalent, if compared with those ones of the ReRAM.

These necessary features and the multiple non-volatile memory candidates for Storage Class Memory applications, have generated a motley assortment of selector types. A summary ⁽²⁾ presenting some of the proposed topologies is introduced next. A special focus will be made over the *Ovonic Threshold Switch* selector, which, as mentioned before, is used and studied in posterior chapters to be co-integrated with ReRAM technologies from our research group.

1.6.1 Si based

Among the silicon-based access devices, the first approach consists in using transistors, where the memory point is usually connected to the drain of it. Three terminal transis-

⁽²⁾Only bipolar selector devices are discussed

tors fill the biggest part of the target specifications enumerated previously. Besides, the capacity of regulating the saturation current through the gate voltage, enables the use of a compliance current, which can be very advantageous for emerging memory technologies such as ReRAM. In order to isolate ReRAM reliability issues inside crosspoint systems, a transistor is a very good approach to be used as selector (see chapter 3). Biggest penalties come with their usual large surfaces, and the three terminals the devices present which reduce arrays density and increase process complexity.

NPN diodes constitute an alternative as silicon-based selectors because of their two-terminal characteristic and their bipolarity [118–120]. At a zero applied bias, the potential barrier for electron transport stays at equilibrium. At a small applied voltage, the current is injection barrier limited. This is not the case for higher voltages, where the barrier is negligible [120], allowing the electrons flow between the two electrodes (See Figure 1.16(a)). The global behavior of the NPN diodes can be modeled thanks to a series-resistance or space-charge limited current behaviors [121]. An example is presented in Figure 1.16(b) obtained by Srinivasan *et al.*. There, current density in the ON state of 1 MA/cm^2 and a ON/OFF ratio of 6 orders of magnitude was obtained using epitaxially growth diodes. Moreover, threshold voltages tuning, changing the diode doping profiles, has been also demonstrated [122].

The main inconvenient with NPN diodes seems to be the high temperature required for their epitaxial growth, which is about 700°C , incompatible with the BEOL processes [111, 120].

1.6.2 Oxide tunnel barrier

Including a thin oxide or nitride layer in the memory stack aiming to increase non-linearity, has been researched as an alternative to access devices. Inspired by the NAND FLASH working principle [123], and allowing bipolar operation, used materials for their fabrication include: HfO_2 , SiO_2 , Al_2O_3 , TiO_2 and ZrO_2 . These materials, also known as high-k dielectrics, can be disposed in single or multilayer configurations. For the former, Schottky barriers can be included in the middle of one of the electrodes of the memory device. An example is presented in Figure 1.17, where a SiN_x nitride layer is sandwiched inside a TaN electrode, allowing conduction only when high bias induces band-bending inside the nitride layer.

In the case of multilayer oxide stacks, a maximum tunnel barrier height can be tuned and shifted inside the stack, in order to increase electric field sensitivity and therefore, non-linearity [125–127]. High current densities for the ON-state were demonstrated ($>10 \text{ MA/cm}^2$), with a selectivity of more than 4 decades [128] (See Figure 1.18).

1.6.3 Mixed Ionic Electronic Conduction (MIEC)

A BEOL friendly alternative [129] for access devices are the copper containing Mixed Ionic Electronic Conduction (MIEC) materials, where a big quantity of mobile copper ions move

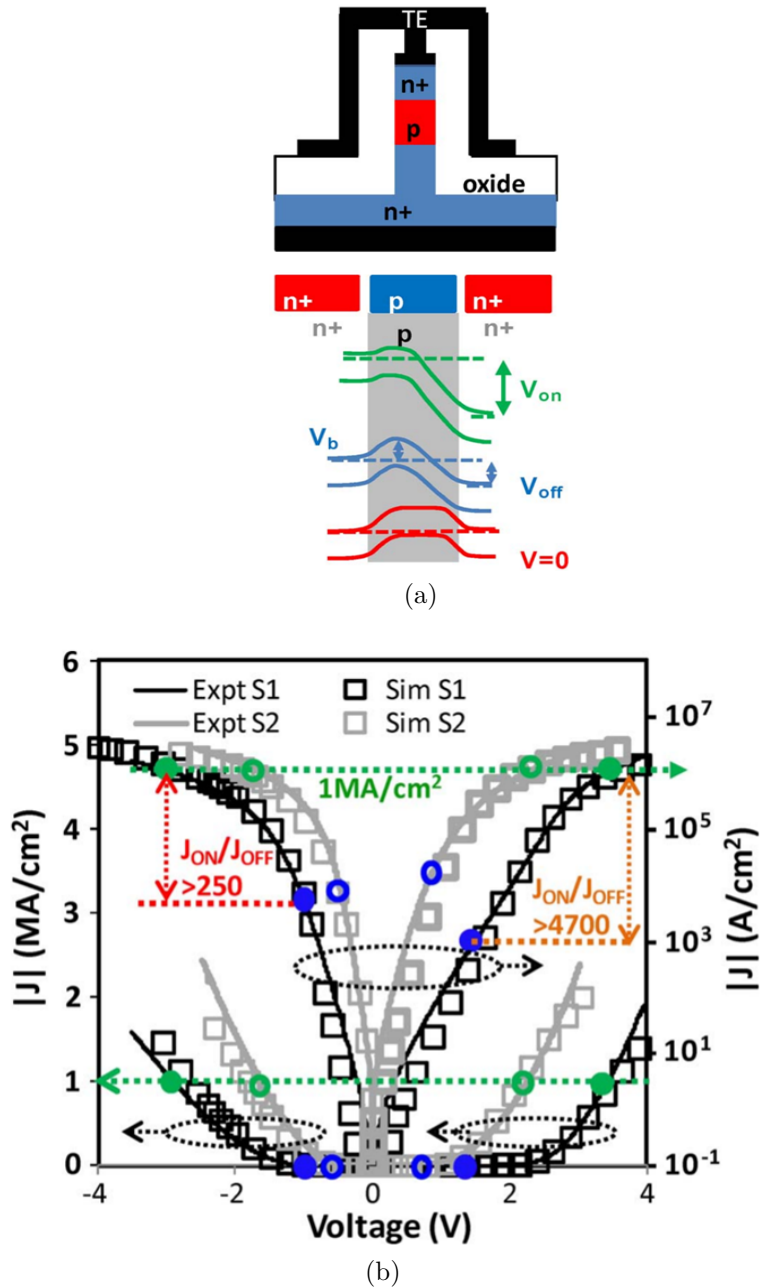


Figure 1.16: (a) Cross section and band diagrams of a two terminal bidirectional NPN junction used as access. The device allows the electrons to flow only when high electric fields are applied. (b) $|J| - V$ experimental (line) and simulated (squares) curves for two different structures S1 and S2 which two doping profiles. ON current is taken once $1MA/cm^2$ density is reached, therefore, V_{ON} is taken once I_{ON} is reached and $V_{OFF} = V_{ON}/3$. Adapted from: [120]

freely inside it and are used to have the selector effect. If a low bias is applied, Schottky barriers are likely to avoid the current flow. With the electric field increase, copper ions

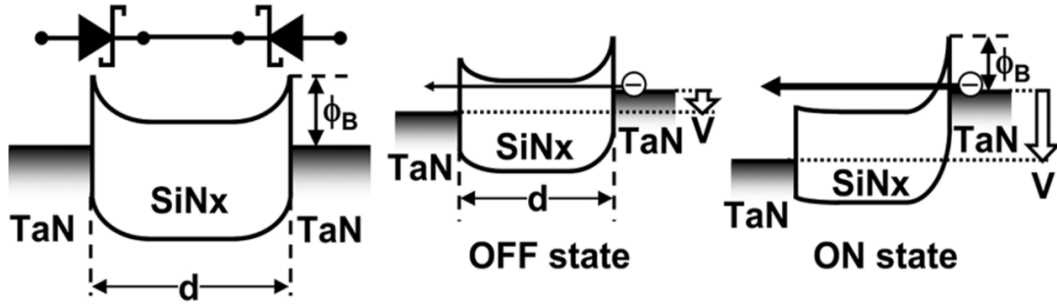


Figure 1.17: Band diagram for a single layer tunnel barrier made of SiN_x . Two back-to-back Schottky barriers allow the selector behavior. Taken from: [124]

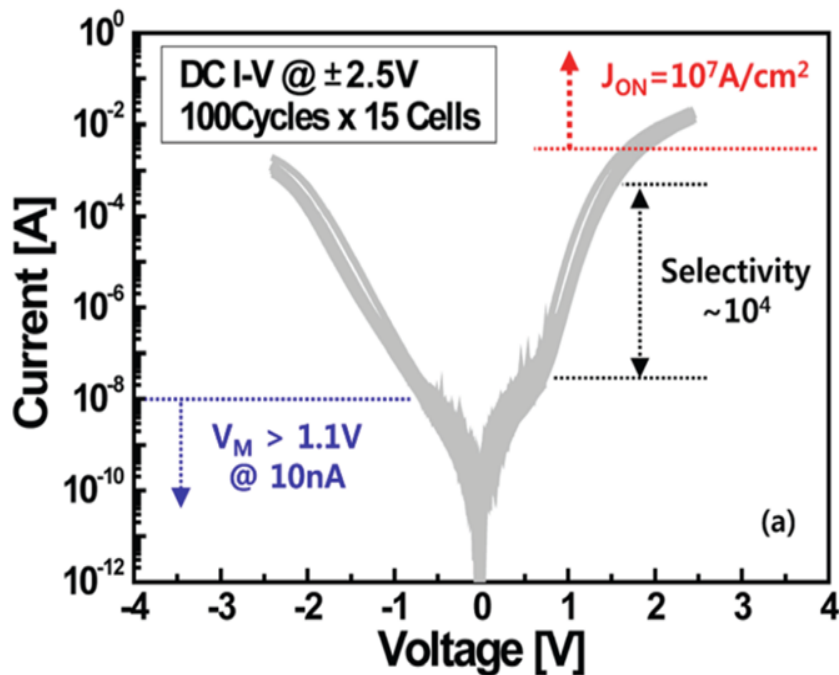


Figure 1.18: Example of the IV characteristic for a multilayer ($Ta_2O_5/TaOx/TiO_2$) oxide-based access device. The IV curve corresponds to the median value of 15 cells over 100 cycles. Taken from: [128]

and vacancies move toward the negatively and positively biased electrodes respectively, hence adjusting the interfaces and generating the exponential electronic current increase. A big portion of mobile Cu allows high current densities for the ON state of the device [130].

As depicted in Figure 1.19(a), the MIEC material is sandwiched between two electrodes where at least one of them must be non-Cu-ionizing [103]. They are built by sputter depositing into e-beam defined vias [129]. With low variability, good scalability, fabrication processes $< 400^\circ C$, and ON/OFF ratios $> 10^7$, low leakage currents ($< 10pA$), that can be held for hours, allowing millions of successive reads without affecting reliability; MIEC selectors are a very interesting approach [111] (see Figure 1.19(b)). Their main

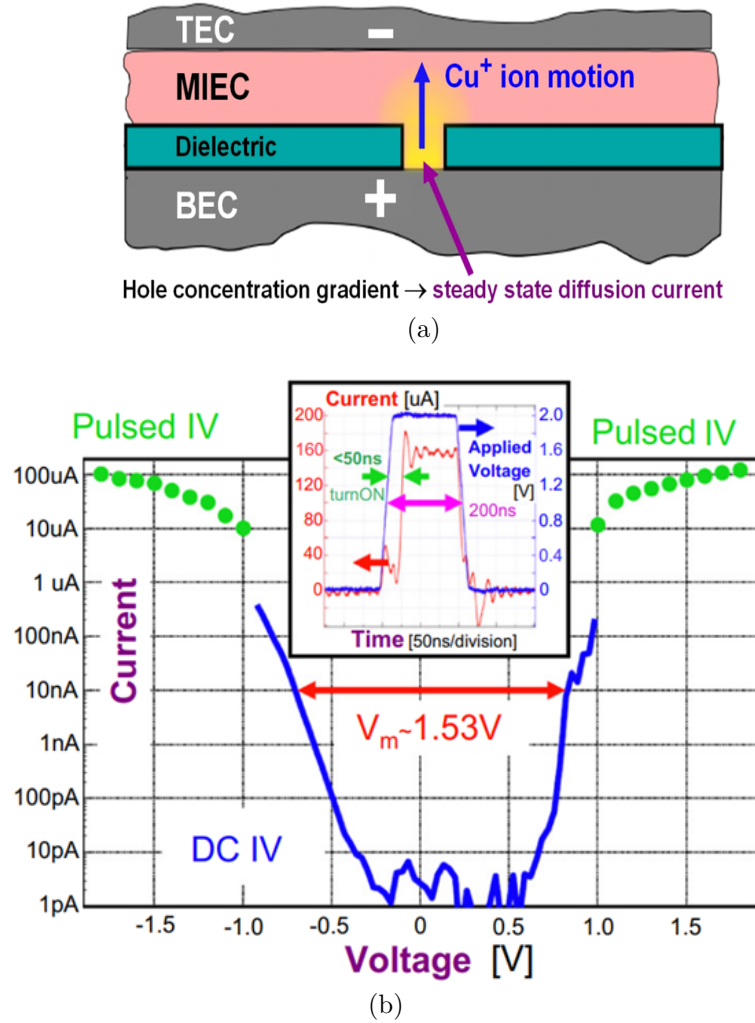


Figure 1.19: (a) Schematic of a MIEC access device. Under a high bias, electron/holes are reordered allowing a diffusion current, which increases exponentially with the electric field and allows high densities for the ON state. (b) Example of a typical IV characteristic of a MIEC material based selector. ON/OFF currents ratio is $\approx 10^7$ and $> 10\text{MA}/\text{cm}^2$ can be observed. Taken from [129] and [131]

issue seems to be endurance performances under high currents ($>100\mu\text{A}$) [129, 130]. This could be a limiting factor if they are intended to be co-integrated with ReRAM technologies, which require compliance currents around these values [72] in order to operate in an optimal way. Another inconvenient are the low turn-on voltages (Figure 1.19(b)), which could be too low to be compatible with ReRAM switching voltages, hence generating potential reliability issues. These operating voltages were demonstrated to be increased enlarging electrode thicknesses of the MIEC selectors, penalizing thus scalability [129] of the crosspoint array if multilayer implementations are intended.

1.6.4 Selector less memories

As previously mentioned, the non-linearity required to implement crosspoint arrays can be a requirement of the memory device itself. Under this scenario, the necessity of an additional access device is suppressed. This section presents a short introduction to the most common self-selected memories.

- **Complementary Resistive Switch (CRS)**

In this configuration two ReRAM are connected back to back with one common electrode [111]. First CRS memories were built using CBRAM devices [132], but another works can be listed, including metal oxide and amorphous carbon materials [69, 133, 134]. Figure 1.20(a) presents an example of a CRS stack, where two HfO_2 OXRAM memories are connected in an anti-serial way. Once the cells are formed, two states are possible: both of them in the LRS and a second case where one of them is in the HRS while the second one remains in the LRS. Given the back to back configuration, HRS for both cells is only possible for the pristine state. For the second case (HRS+LRS), CRS device presents a voltage divider characteristic where almost the totality of the applied voltage drops over the HRS ReRAM. If bias is applied with the cell in HRS receiving a positive polarity, there will be a first switch event or threshold voltage V_{th1} , appearing once the device in the HRS goes into the LRS. With both devices in the LRS, the voltage is divided and a V_{th2} is observed when the cell initially in the LRS goes into the high state (RESET). If a positive bias is applied again, a switch is not going to occur given that the cell initially in the LRS and now in the HRS, requires a negative bias to go into the LRS, because of the back to back configuration. This electrical characteristic leads to a symmetric behavior as seen in Figure 1.20(b) and the high insulating quality for low voltages is profited to reduce sneak paths in crosspoint configurations. As for the reading, a $V_{th1} < V_{READ} < V_{th2}$ is applied and the two states can be obtained depending on which cell is programmed in the HRS. CRS devices present a similar working principle as the CMOS inverter where one of the transistors is always OFF.

Concerning the disadvantages of CRS configurations, increased power consumption is inferred since higher operating voltages can be required. A second aspect, is the "ON" state (both cells in the LRS) instability [132, 135], that has traditionally been solved using an external series resistor. However, and once again, the inconvenient with this solution is increasing the write power [111]. Additional handicaps for CRS technologies worth to be mentioned are the slow programming processes (a sweep voltage must be applied in order to effectively switch the devices) and complex processing to fabricate CRS stacks. Because of these reasons, some studies were made intending to demonstrate CRS behavior in single-layer ReRAM devices [82, 137]. These configurations take advantage of the asymmetry of the reset state, modifying the depleted gap localization during operation. However, NIs obtained are not very high, hence diminishing the potential impact of these developments for 3D crosspoint architectures.

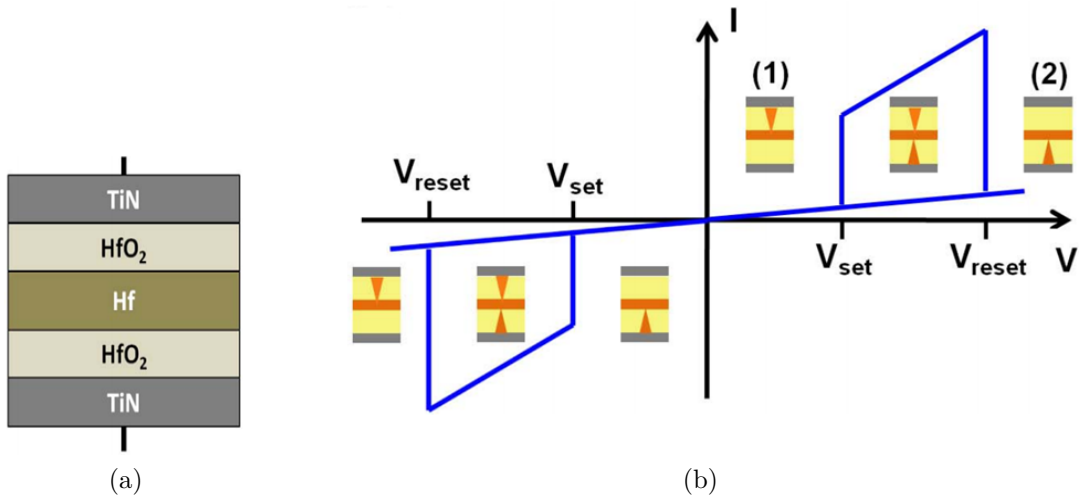


Figure 1.20: (a) Stack example of a CRS device using $TiN/HfO_2/Hf$ OXRAM. (b) Typical IV symmetric characteristic of a CRS device with its four voltages. Once the devices formed, two states are possible, the two devices in the LRS and HRS+LRS. The principle consists in alternating the CF presence inside the two anti-serially connected resistive devices. Taken from [135] and [136]

- **Hybrid Metal Insulator Transition Devices (MIT)**

This type of devices are selector less memories with a high non-linearity if compared to most traditional devices. The hybrid characteristic, comes from the fact that they present both access device and memory behaviors. Proposed solutions in literature include oxygen concentration in vanadium oxide [138] or niobium oxide films [139], $PrMnO_3$ [112], multilayer stacks using tunnel barriers [140], among others. The issue for these configurations remains the NL, which is not enough for high density 3D architectures.

1.6.5 Threshold switching

Considered among the most promising candidates for 3D crosspoint arrays, in a threshold switch access device mainly two regimes can be differentiated: a very high resistive state, profited to block sneak-path currents and a low resistive state when the bias applied over the selector device, surpasses a characteristic threshold voltage; used for the memory programming and eventually the reading process. During threshold switching, an abrupt increase of the current is appreciated. Among these type of selectors, most important topologies are Metal-Insulator Transition (MIT), Threshold Vacuum Switch (TVS), Volatile CBRAM, and Ovonic Threshold Switch (OTS). All of them are presented next.

- **Metal Insulator Transition (MIT)**

As well as applicable to self-selected memories devices, MIT materials can also be used as selectors. In this case, access elements are electrically or thermoelectrically

triggered [111]. Materials such as vanadium dioxide VO_2 have been widely studied [141]. An IV characteristic for MIT VO_2 based selector is presented in Figure 1.21. There, a NL of one order of magnitude can be appreciated and low threshold voltages are observed. The main inconvenient with VO_2 based selectors, seems to be the low transition temperature that they present. This is the reason why, some alternatives have been explored, notably NbO_2 , where thermal stability up to 160°C was demonstrated [139]. This comes with a trade-off, Non-Linearity is reduced and the threshold voltages are slightly increased.

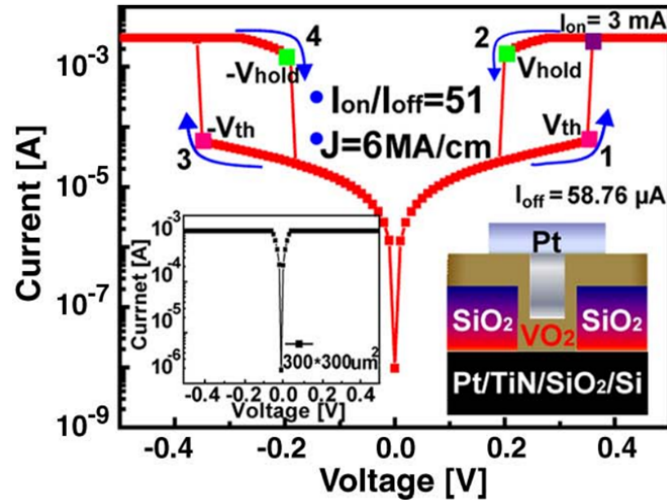


Figure 1.21: IV characteristic of a Metal Insulator Transition (MIT) selector device. The insets show the IV characteristic of the microscale device and the nanoscale structure $Pt/VO_2/Pt$. Taken from: [141]

In the case of vanadium and niobium oxides, the switching mechanism is defined by the Mott transition. These materials are also used to fabricate Mott-memories. Their volatile or non-volatile behavior is defined by the doping (Cr is widely used), the applied current density, and the stacks symmetry [44, 142]. A very interesting MIT selector was recently presented by Hennen *et al.* [42]. The $(V_{1-x}Cr_x)_2O_3$ devices show fast switching times ($< 10\text{ns}$), high stability ($< 5\%$) and $> 10^{12}$ endurance cycles. However the non-linearity for the best-case device seems to a little bit low (only two decades of margin).

- **Threshold Vacuum Switch (TVS)**

The use of vacuum gaps has been proposed as another option to obtain bidirectional access devices for 3D stackable crosspoint architectures [143]. Fulfilling the essential requirement of high density current for the ON state and low OFF current, the vacuum gaps present $\approx 1\text{nm}$ ultra-narrow thickness, formed between TiN and WO_x layers. $> 10^8\text{A}/\text{cm}^2$ current densities, $> 10^5$ decades of selectivity, and $> 10^8$ endurance cycles were demonstrated. TVS-ON behavior is explained through a combination of direct-tunneling and ohmic conduction which is limited by the series resistance of the memory technology used. For the OFF state, superposition of

direct-tunneling and non-linear conduction was suggested [143]. A priori, the main inconvenient with such devices seems to be the elaboration of the narrow vacuum gaps. For array devices it would be hardly difficult to obtain high uniformity for such thicknesses [16].

- **Volatile CBRAM**

CBRAM memories have been demonstrated to present volatile switching under certain conditions. The most notable ones are the materials used for the stacks fabrication and the applied current densities or the programming times. Most outstanding works include the use of Cu, Ag, Al, Ti., for the electrodes and materials such as SiO_x , TiO_x , AlO_x , WO_x , HfO_2 , and others, as active layers. This, and the good NL obtained, have led to propose this kind of volatile CBRAM memories as access devices [144–149]. Volatility is possible thanks to the high instability of the metallic ions that form the conductive filament as well as its small width inherent to the materials used [150, 151], which cause its dissolution once electrical stimulus is absent making the device to go into the HRS. Numerical and compact theoretical approaches have been developed, aiming to understand the fundamental mechanisms of filament formation and disruption and no so divergent from models used for non-volatile switching [152–155]. For instance, the numerical one consists in the use of thermally activated drift/diffusion and Brownian-like motion to predict the IV-characteristics of such structures.

Some examples in literature report very good performances. Even if the employed materials were not disclosed, Jo *et al.*, presented a Field Assisted Superlinear Threshold (FAST) selector [156], which seems to be a Volatile CBRAM device [157]. A selectivity of $\approx 10^{10}$, very fast switching ($\approx 5\text{mV/dec}$), $\approx 10^8$ endurance cycles and BEOL compatibility (processing temperature $<300^\circ\text{C}$) were obtained. An I-V characteristic of the FAST selector for several active layer thicknesses is presented in Figure 1.22, allowing to appreciate its impressive selectivity.

Some of the inconveniences with these access devices topology, seem to be the low dissolution time of the conductive filament and the dependence of the volatility on the applied current density for some stacks. The necessary current densities, would not be compatible with the programming currents of ReRAM devices [158]. However, volatile CBRAM configurations remain as one of the most interesting approaches for selector applications.

- **Ovonic Threshold Switching (OTS)**

The Ovonic Threshold Switching (OTS) was first studied by Stanford Ovshinsky in his seminal work [33]. In there, phase changes that lead to conductivity variations over thin films of amorphous chalcogenide alloy materials, were reported. A sudden increase on the conductivity is observed once the applied voltage surpasses a threshold voltage V_{th} . This phenomenon is commonly known as the switching event. During it, a negative differential resistance (NDR) is observed, before current stabilization into a high-conductive state (ON state). Prior to this, the OTS device presents a very high resistance (OFF state). An example of I-V bipolar characteristic is depicted in Figure 1.23. As appreciated, the ON state is kept as long

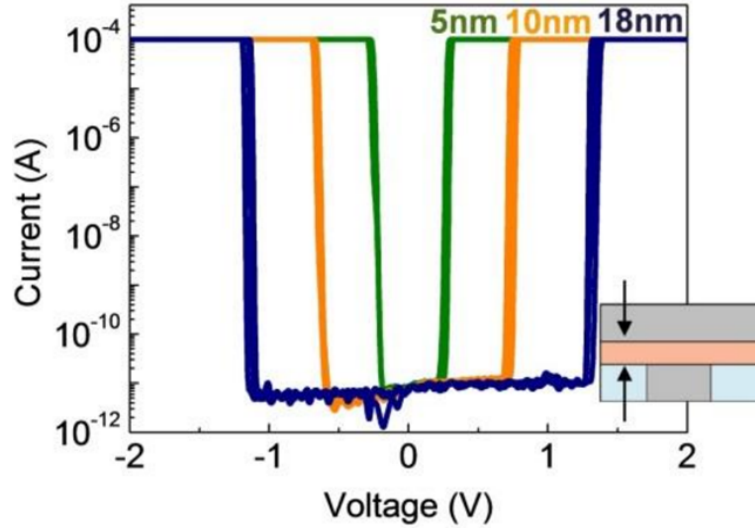


Figure 1.22: IV characteristic of a Field Assisted Superlinear Threshold (FAST) (likely to be a volatile CBRAM device [157]) for various thicknesses. Impressive selectivity ($\approx 10^{10}$) is appreciated. Taken from: [156]

as the applied voltage remains larger than a hold voltage (V_{hold}), normally lower than V_{th} . The ratio between the two conductive states, is relatively high. Besides, the switching process is fast ($\approx ns$) [111], high density ON currents are supported ($> 10MA/cm^2$), as well as high endurance cycles with low variability [159]. All this, makes of OTS access devices interesting appliances for selector devices and candidates to be co-integrated with emerging memory technologies.

Various works [161–167] exist to explain OTS switching. At this point, it is important to recall that chalcogenide materials are also included as part of the alloys that form the active layers of PCM memories. It means that most of the theories formulated to explain PCM’s working mechanism, can be adapted to understand OTS devices too. Further chapters (chapter 4 and chapter 5), provide deeper analysis and explanations of the models cited above.

1.7 Emerging memory technologies and selector devices: benchmark

So far, a general view of the main emerging memory technologies and selector devices, has been provided. **In order to elucidate the main motivations that led to produce this thesis work, general comparisons between such technologies and some state of the art, make possible the identification of the main disadvantages of ReRAM and OTS topologies.** Improvements over them, will allow to increase their attractiveness for SCM applications.

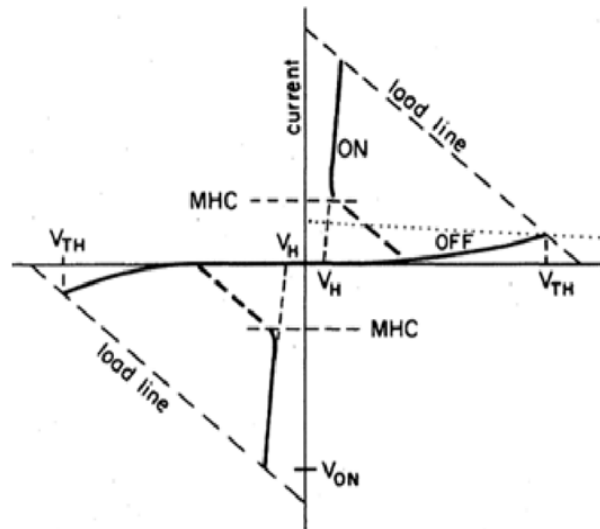


Figure 1.23: Example of IV behavior for an Ovonic Threshold Switching (OTS) selector. For low voltages, the OTS presents a very low conductance. Once the applied voltage surpasses the threshold voltage V_{th} , the device goes into a high conductive state that is kept if the electrical tension is maintained over the hold voltage V_h normally lower than V_{th} . Taken from: [33, 160]

1.7.1 SCM device candidates: comparison





































As stated in precedent sections, emerging memories require very low latencies (from hundreds of nanoseconds to some microseconds), high reliability (at least 10^6 endurance cycles), low cost per bit and low power consumption. Such characteristics determine the S-type (storage) or M-type (memory) SCM application (see Table 1.1)

When these new technologies appeared, it was thought that one of them would be able to serve for both types of SCM in the entire memory hierarchy. It was expected they became universal memories as it is the case for traditional memories. Now, it is globally accepted that it will not be possible, and that specific memory devices will be more likely to be optimized as a function of the envisaged application. Thus, application-driven technologies have been developed implying the general appearance of some trade-offs [9].

Table 1.2 summarizes the potential of the main emerging memory technologies introduced previously as a function of the key metrics for their performances. Each metric is presented qualitatively in terms of strength, medium or weakness characteristic, using green, yellow and red icons, respectively. Most of these metrics, as well as the main advantages and inconveniences for every memory type, were previously treated in section 1.3; except for ReRAM where, in the next section, and given their capital importance for this work, their potential for SCM applications is discussed.

⁽³⁾Multilevel Cells

Table 1.2: Comparison of potential for the most important emerging memory technologies for Storage Class Memory applications. Adapted from: [16]

Parameter	FeRAM	STT-MRAM	PCRAM	ReRAM
Scalability				
MLC ⁽³⁾				
3D Integration				
Fabrication cost				
Retention				
Latency				
Power				
Endurance				
Variability				

1.7.2 ReRAM for SCM applications

M-type SCM requires memory metrics to be very close to those ones of DRAM. Looking at the performances of ReRAM, if compared to other main emerging memories (e.g. STT-MRAM) (see Table 1.2), cycling endurance and latency time, make of these technologies unlikely candidates for M-type SCM. On the other hand, good scalability, non-volatility, 3D integration compatibility, back-end of line friendly, power consumption, and higher endurance cycles and latency, when compared to Flash technologies; place them in a good position for S-type SCM. Improved energy efficiency and less-area occupation with respect to widely used nowadays storage memories (HDD and SSD), could be a very interesting trade-off to take into account, given that ReRAM and in general, all the emerging memory candidates, present higher fabrication costs per-bit [16]. Even more optimized systems could implement hybrid storage structures with emerging memory technologies combined with Flash memories in a complementary way, as a species of "cache" systems, in order to improve global performances [16].

As discussed in subsection 1.3.5, ReRAM technologies present a filamentary characteristic under electrical stimuli, which makes possible the two resistive LRS and HRS states. The ion migration of oxygen vacancies or cations for OxRAM and CBRAM topologies respectively, thanks to thermally activated hopping; are the main cause of the dissolution and formation of conductive filaments. These processes are highly stochastic, leading to intrinsic variability of such technologies. Additionally, extrinsic factors such like impurities generation during oxides deposition or non-uniform thicknesses of the memory points at the array level, can be also variability sources for cycle to cycle (C2C) and device to device (D2D) performances. Hence, intrinsic and extrinsic variability imply, for instance, dispersions over the switching times, HRS and LRS values, as well as endurance cycles [168]. Therefore, variability is one of the main roadblocks, preventing ReRAM com-

mercialization [168]. For the time being, only some demonstrators have been presented [124, 169, 170], and some products are available and produced at small scale [171–174]. Materials engineering, integration architectures and operation modes (see chapter 3), need to be deeply optimized, in order to reduce it at acceptable levels. Moreover, filament size dependence on programming parameters [83, 84, 175, 176] implies that reducing operating currents with shrinking, increases dispersions of the above-mentioned features.

Besides dispersion issues, moving oxygen vacancies or metal ions through the active layer, causes a trade-off between writing speeds and data retention [16, 72] which worths to be mentioned and that could be problematic under some scenarios. Additionally, forming operation as well as its intracell variability, needs to be optimized. Under this scenario, and given the main inconveniences inherent to ReRAM devices already highlighted, research peak of interest over such technologies, is considered to be overpassed [177, 178]. This is a normal stage in a product life cycle as presented in Figure 1.24. Consideration of these technologies for S-type SCM applications, development of selector devices for crossbar arrays, and the growing interest on new paradigms such like AI and IoT (see subsection 1.7.3); are expected to renew the interest, as well as to increase their market share.

As mentioned above, reliability is one of the main roadblocks of ReRAM technologies if intended to be used for SCM applications. This is the reason why, this feature is studied and optimized at the array level, through experimental and theoretical investigations and over various stacks; in chapter 3 of this work.

1.7.3 Resistive memories for low-power applications and non-von-Neumann architectures

Volatility of traditional SRAM and DRAM memory technologies, represents an issue in terms of power management for devices where standby operation is very important and the power sources are limited, such like mobile or automotive applications. Volatile memory arrays need to stay in the ON state in order to keep the information stored in them. In the case of DRAM devices, refreshing processes are also required. A well-known method to reduce power consumption in standby mode, consists in transferring the content of the memory arrays into the non-volatile storage tiers before going into such regime. The inconvenient with this operation is the time and power consumption, needed to copy the data into, for example, Flash memories [179]. ReRAM technologies and in general, fast and low-power emerging technologies, could be used for these processes. This is why and for even more restricted power budget devices such as IoT applications, where appliances stay in sleep mode most of the time and only wake up under specific stimuli; emerging devices could be very interesting alternatives.

The dependence of the resistive states values on the programming currents and pulses duration, observed for ReRAM and previously discussed in section 1.3.5.b, could be prof-

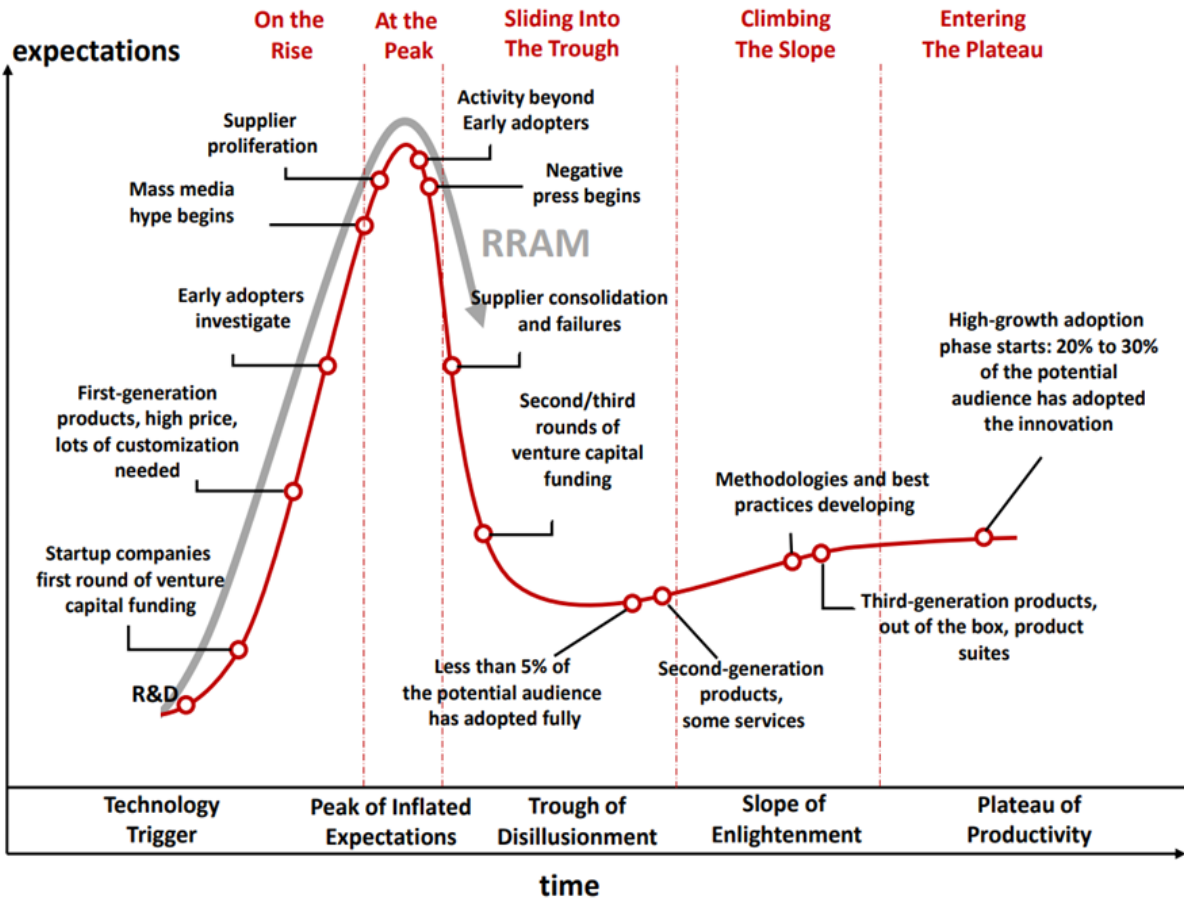


Figure 1.24: Typical maturity curve for products. Actually, ReRAM has overpassed the interest peak and goes to the so-called trough of disillusionment. Mature product characteristics are expected in the next few years with S-type, AI and IoT appliances increasing market penetration. Taken from: [178]

ited by brain-inspired or non-Von-Neumann systems ⁽⁴⁾. In them, ReRAM ⁽⁵⁾ technologies could be used to mimic synapses plasticity [180]. Hence, non-volatile *in-memory computing* capabilities would be feasible, with boolean variables being represented in terms of resistance states (*multilevel or analog approach* [181–183]) and basic/primitive logic circuits implemented using resistive memories [184]. However, resistance modulation requires a big variety of pulses shapes as well as knowledge of the precedent state of the synapse, implying complex and big surface of the peripheral circuitry. Besides, ReRAM intrinsic variability of the resistive states can hinder systems reliability [185]. Because of these issues, simpler architectures, in order to have discretized resistive levels as a

⁽⁴⁾In traditional Von-Neumann architectures, processing and memory units are separated and data constantly flows between them.

⁽⁵⁾Along with ReRAM memories, PCMs are the most used technologies for non-Von-Neumann systems. A priori, inconveniences seem to be a higher power consumption for the writing and reading operations as well as the voltage drift and latency. On the other hand, lower variability with respect to resistive memories, is an advantage for specific configurations.

function of the electrical stimuli, have been developed. A typical example is a parallel configuration where various resistive memories are used to model a synapse. Binary states (HRS and LRS) for each device, and the parallel sum of individual conductances, which produce the multilevel resistivity of the synapse, are used [186, 187], in the so-called, *binary approach*. Another solution to reduce ReRAM variability impact over neuromorphic systems performances, consists in using Convolutional Neuronal Networks (CNN) based on multilevel-like behavior with parallel devices operating in binary mode. This solution was proposed by Garbin *et al.* in [185, 188], and applied to pattern recognition systems, with demonstrated accuracies up to 98.9% taking into account C2C and D2D devices dispersions.

Although ReRAM variability seems to be an issue for classical S-type SCM and some non-von-Neuman configurations, it can be profited for applications where truly random processes are fundamental such like security, data encryption, random number generators, and machine and deep learning [179, 184].

1.7.4 Selectors benchmark

As in the case of memory topologies some of the main selector technologies features are summarized qualitatively in Table 1.3. Once again, strength, medium or weakness characteristic is represented by the green, yellow, and red icons. Reference ReRAM values are taken for their evaluation: $10MA/cm^2$ for the J_{ON} , full BEOL compatibility as well as minimum device size ($4F^2$) for the 3D compatibility; whereas maximum endurance and selectivity are wished. Hence, co-integration potential of OTS devices, best candidates along with TVS and FAST topologies according to Table 1.3; with ReRAM stacks for S-SCM applications, is shortly discussed in the next section.

Table 1.3: Comparison of the most important features for some of the treated selectors as a function of their potential. Adapted from: [111]

Selector Device	J_{ON}	Selectivity	3D compatibility	Endurance
Si transistor				
NPN diode				
Oxide Tunnel Barrier				
MIEC				
NV ⁽⁶⁾ CBRAM (FAST)				
CRS				
TVS				
MIT				
OTS				

1.7.5 OTS devices for crossbar arrays

OTS presents good endurance, 3D compatibility, high density current conduction capabilities and high NL. As mentioned before, they are among the most interesting candidates to be used as selectors.

As for the inconveniences, probably, the biggest one, is the fire/forming process (for the first switch, the threshold voltage is usually higher). This initialization step requires high energy and is not compatible with switching and forming voltages of ReRAM memories as well as with the highest operating voltages of advanced CMOS technological nodes. Therefore, larger periphery or complex algorithms could be eventually required for the initialization. Moreover, switching currents may not be compatible with ReRAM programming ones. chapter 4 and chapter 5, show how thanks to material and circuit engineering these inconveniences can be solved and OTS selectors can be successfully proposed as access devices for co-integration with OxRAM technologies. Obtained results open the way for new optimizations and applications at the materials and circuits level.

⁽⁶⁾Non-Volatile

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Studied Devices and Measurement Methods

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WITH ReRAM and OTS technologies previously introduced, as well as their importance for crossbar arrays and SCM applications, this chapter presents, in a first part, the main stacks characterized and studied during this thesis work. Then, an overview of the integration steps and structures tested is introduced. In a final stage, main electrical setups and measurements methodology are discussed. Even if various stacks are tested for both OTS and ReRAM devices, the measurement techniques are common to all of them.

2.1 Studied Devices

2.1.1 ReRAM devices

In subsection 1.3.5 three types of resistive memories were presented as a function of their operation principle and the device physics: OxRAM, CBRAM and Hybrid ReRAM. The latter, has been much less studied, but generally, they present improved cycling endurance (number of SET-RESET cycles that the devices are able to perform) and lower window margin (ratio between the HRS and LRS median values) [1–3]. Conversely, OxRAM and CBRAM topologies have been widely treated in literature. Consequently, these two main types are considered for this work, and the devices stacks for both of them are presented in Figure 2.1. They were previously developed and optimized by the CEA-Leti in precedent works [4–9].

Simplicity, good compatibility with the silicon CMOS back-end-of-line (BEOL) fabrication process, scalability down to the 10nm technological node or even lower, low programming currents, high endurances, and good retention times; are essential to ReRAM devices [10]. With further details on some of these characteristics provided later in this chapter, they have been widely demonstrated over binary oxides. In the case of OxRAM, HfO_x and TaO_x have been some of the most used alloys. The working mechanism of OxRAM devices is based on the migration of both oxygen vacancies and ions to form the conductive filament (see subsection 1.3.5 for more details). This type of ReRAMs requires rich defect materials in order to supply the vacancies. They are stacked with depleted resistive layers in oxygen or oxidizable materials (i.e. Ta , Ti) [11–13], which are used as electrodes for such configurations. Hence, all the mentioned aspects and the prior work in our research group, above mentioned, led to the choice of the $Ti/HfO_2/TiN$ stack for this thesis studies (Figure 2.1(left)).

As for the CBRAM topology, Al_2O_3 is an extensively used material for semiconductor applications, notably High-K metal gates. It implies integration compatibility with conventional fabrication processes if intended to be employed in memory technologies. Good ReRAM characteristics have also been widely demonstrated, based on creation and dissolution of a Cu-based conductive filament [6, 14, 15] (Figure 2.1(right)).

Finally, both oxides presented in Figure 2.1 are deposited using traditional deposition techniques, Atomic Layer Deposition (ALD) for HfO_2 and Physical Vapor Deposition (PVD) for Al_2O_3 . Hence, highly controllable thicknesses and uniformity at a fast pace,

are possible.

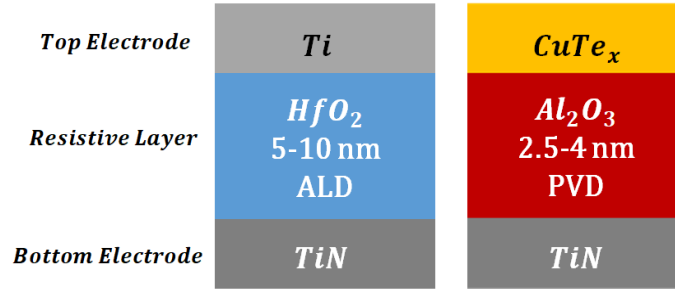


Figure 2.1: ReRAM stacks studied in this work. OxRAM memory (left) uses HfO_2 as active layer while Al_2O_3 is employed for the CBRAM topology (right).

2.1.2 OTS devices

The *Ovonic Threshold Switching* selectors used in this work are based on a $GeSeSbN$ (GSSN) chalcogenide layer. A general introduction to the diverse types of selector devices can be consulted in section 1.6, whereas further details about the optimization process (chalcogenide thickness and stoichiometries), the working mechanism, and the advantages of GSSN systems, are treated in chapter 4. As indicated in Figure 2.2, layer thicknesses varying between 5 and 25nm were considered. Analogously to ReRAM devices, OTS switching layers are sandwiched between two TiN conductive electrodes. Previous work [16] demonstrated how TiN diffusion inside the chalcogenide material, can hinder OTS performances, notably the switching voltages and the devices lifetime. To drastically reduce such diffusion, carbon layers surrounding the GSSN alloy are used. Stacks including such layers (1-3nm thicknesses) were also tested. Furthermore, magnetron sputtering without vacuum break, which is a Physical Vapor Deposition (PVD) technique; is used to deposit the OTS materials, in order to avoid surfaces oxidation.

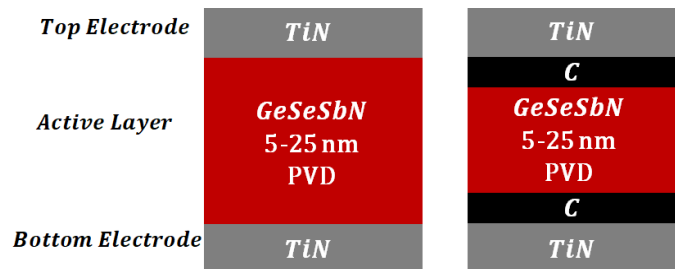


Figure 2.2: OTS stack studied in this thesis. An optimized $GeSeSbN$ chalcogenide alloy allows to have the access device functionality. Carbon electrodes influence (right) was tested after results presented in [16] with thicknesses varying between 1 and 3nm.

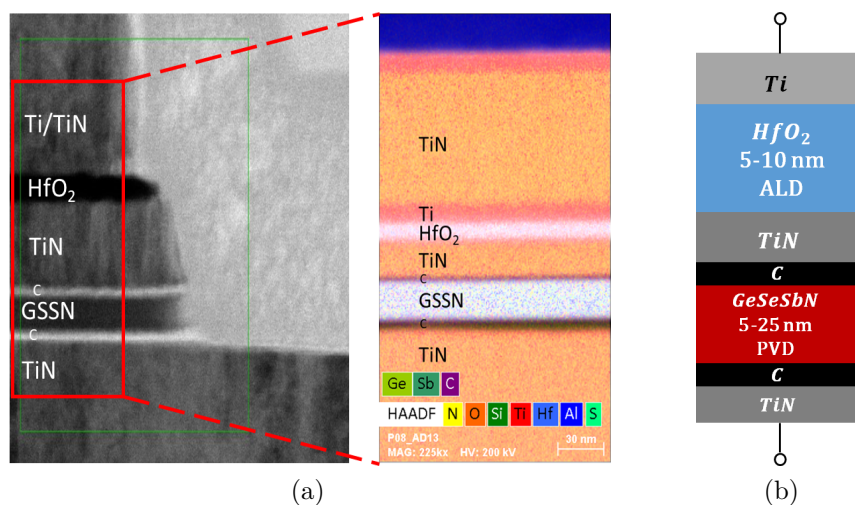


Figure 2.3: (a). Example of the TEM cross-section and EDX profile of the co-integrated OTS+OxRAM devices. A schematic of the implemented stack is presented in (b).

2.1.3 OTS+OxRAM structures

For the OTS+ReRAM (1S1R) devices, OxRAM stacks (Figure 2.1) were co-integrated with the OTS ones presented in the precedent section (Figure 2.2). A TEM cross-section and a EDX profile shown in Figure 2.3, depict an example of the implemented stack where a clearly separation among the different layers is appreciated.

Co-integration presents some challenges at the process level. Among them, etching of the stack with potential aggressive aspect ratios, may be the most important one. OTS being downside in the 1S1R structure, implies that during etching, OxRAM edges are exposed to plasmas, which can affect devices conformity.

2.2 Stacks architectures and structures

Aiming to study the electrical performances of the diverse stacks presented, mainly three types of configurations were tested: 1 Device (1D), 1 Transistor-1 Device (1T1D) and matrix arrays, with the device under test (D) standing for 1 ReRAM (1R), 1 Selector (1S), or OTS+ReRAM (1S1R). For the 1D devices, fast and cheap integration processes can be done. It allows individual verification of their functionality regardless of the influence of another devices. Inconveniences appear, once current control is necessary. External resistors or another devices such as diodes or transistors can be eventually used. However, undesired RC effects can appear as well as overshoot currents, that could damage the devices under test. Additionally, the time constant of the equivalent RC circuit, limits fast switching measurements and implies a delay between the applied voltages and the measured ones over the configuration tested [6]. This is why, the best strategy to limit the current is to co-integrate the tested device, in the BEOL, with a FEOL CMOS

Chapter 2: Studied Devices and Measurement Methods

technology (1T1D configurations). Besides the excellent control current and overshoot avoiding, transistor devices can be used as selectors for 1R systems with fast switching capabilities, as well as in arrays configurations. Moreover, the current density flowing, depends on transistors size. For all the measurements over 1T1D structures presented in this work, the channel length of the CMOS technology used is 130nm, which provides current densities sufficient to form and to operate OTS and ReRAM elements.

Tested configurations (1D, 1T1D and matrix arrays) as well as all their combinations (1R, 1S, 1S1R, 1T1R, 1T1S, 1T1S1R), were implemented over two CEA-Leti test vehicles: IRMA (1D) and MAD (Memory Advanced Demonstrator) (1D, 1T1D and matrix arrays). They are briefly introduced next:

2.2.1 IRMA mask

This test vehicle is entirely made at the CEA-Leti's clean-rooms and allows to fabricate 1D systems in a plug configuration. This mask is convenient for the first exploration stages over novel devices, that are not mature enough to be co-integrated with transistors or inside matrix arrays. Diameter of the measured wafers is 200mm and the integrated device sizes vary between 30nm and $1\mu\text{m}$ with various vias diameters also available. Two structures were mainly tested, VIA and MESA stacks, which are described later. In both cases, devices under test are deposited on top of a tungsten via and accessed through metallic copper lines. In the case of the bottom electrode, the metallic line is directly linked to the tungsten via. The TiN electrodes allow a good grip between the integrated device and such via. A schematic view of the contacts, as seen on the surface of the tested wafers, is presented in Figure 2.4. There, two patterns can be appreciated and correspond to the top and the bottom electrodes. Four pads are available to access the device. In some cases, these pads are made of TiN . Since its resistance can be high, this aspect needs to be taken into account when measuring the devices, which are located under the center point of the pattern as also indicated in Figure 2.4.

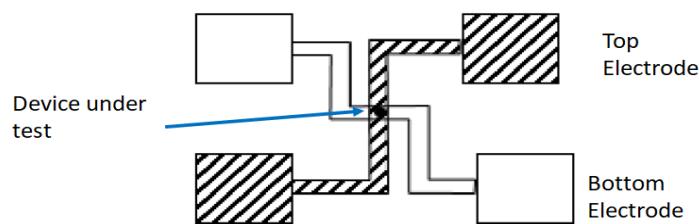


Figure 2.4: Contact Scheme of the CEA-Leti's IRMA test vehicle. The tested device (1R, 1S, 1S1R) is located under the center point of such structure with sizes varying between 30nm and $1\mu\text{m}$.

2.2.1.a VIA structure

Thanks to a simple structure with a minimized number of etching or complex patterning, fabricating VIA stacks is a fast and cheap process used in the early stages of devices

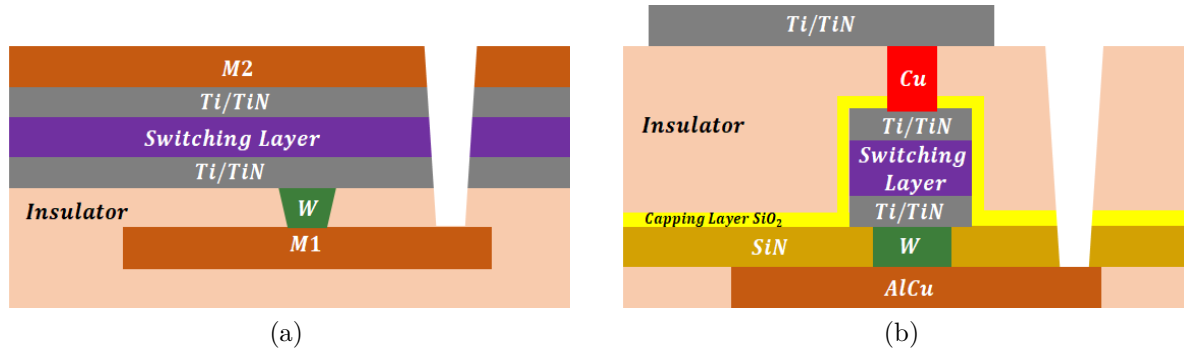


Figure 2.5: Schematic view of VIA (a) and MESA (b) structures. The switching layer can make reference to the oxide layer of a ReRAM or the chalcogenide material of an OTS. In the case of a 1S1R configuration the active layer refers to all the layers stacked between the outer TiN electrodes in Figure 2.3(b).

study in order to determine its feasibility. However, this structure is not realistic at all in terms of industrial use. In there, the metallic superior layer is directly connected to the top electrode as observed in Figure 2.5(a), where the VIA stacking is presented. Given that the top electrode is not patterned, it implies that it is common to all the devices on the wafer. On the other hand, the bottom electrode is accessed through a metallic via. Concerning the integration process, in a first stage, the inferior metal line (M1 in Figure 2.5(a)) is etched and deposited. Then, tungsten vias are connected to such metal line and filled with the bottom electrode, which is full sheet deposited as well as the switching layer (chalcogenide layer for an OTS and oxide layer for the ReRAM) and the top electrode. The final step consists in contact opening on the lowest metal line in order to have small openings to reach the bottom electrode of each device.

2.2.1.b MESA structure

In an analog way to the VIA structure, in a MESA one, the layers of the device under test are deposited over a tungsten plug connected to a bottom metal line. In the schematic reported in Figure 2.5(b), this metal line is made of an AlCu alloy. Once the layers are deposited, they are etched and capped with SiO_2 , while the remaining wells are filled with insulator materials. The etching process is able to control the device sizes which vary between 30 nm and $1\mu m$ as previously stated. Contact between electrodes and the pads on top of the wafers is made through metallic vias. A MESA structure is a more industrial-like stack if compared with a VIA type.

2.2.2 Memory Advanced Demonstrator (MAD) test vehicle

The MAD test vehicle allows the integration of the devices under test in the Back-end of Line of a CMOS technology. This is made in order to have a closer approach to real products and to improve the control of the current flowing through the devices.

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Hence, 1T1D structures can be measured, although 1D and matrix configurations are also available for measurement. In the case of 1D and 1T1D, sizes of the devices vary between 300 and 600nm, integrated on 200mm wafers as in the case of the IRMA test vehicle.

Two main stages are distinguished for the Memory Advanced Demonstrator integration flow. Firstly, the metal levels 1-4, corresponding to the FEOL, are fabricated by an external foundry using a 130nm CMOS technology, as previously mentioned. Then, the devices are deposited and etched on top of Metal 4 at the CEA-Leti clean rooms using for instance, the MESA stacking introduced in the precedent section. A schematic cross-section for a 1T1D structure can be appreciated in Figure 2.6.

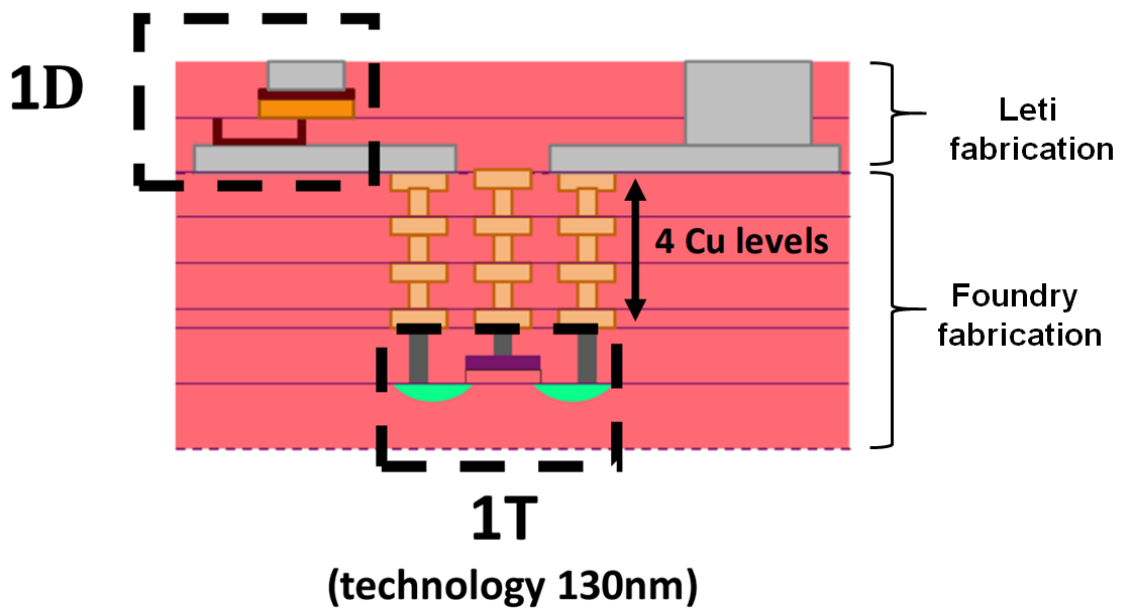


Figure 2.6: Schematic cross-section of the Memory Advanced Demonstrator (MAD) for a 1T1D device. Metal levels 1-4 are fabricated by a foundry. The devices to be tested are then deposited at the CEA-Leti on top of Metal 4.

2.2.2.a Matrix Arrays

On MAD test vehicle, sizes of the available matrices vary between 256bits and 1Mbit. In them, every device is connected to its own control transistor. Top electrodes are said to be connected to the Bit Lines (BL), whereas transistor gates are connected to the Word Lines (WL), and bottom electrodes are connected to the Source Lines (SL). Additionally, multiplexers are employed in order to address specific points inside the arrays. In this work, 4Kbits matrices were used aiming to study ReRAM reliability as it will be discussed in chapter 3. Lines of the arrays are organized in 16 WL and 256 BL and SL, as reported in Figure 2.7(a). The access to the arrays is available through 25 pads ranged in barrettes, where 8 (addressing bits) of them are dedicated to the 256 BL-SL, while 4 pads are used for the WL addressing. With two more pads used for the VDD and GND voltages, three

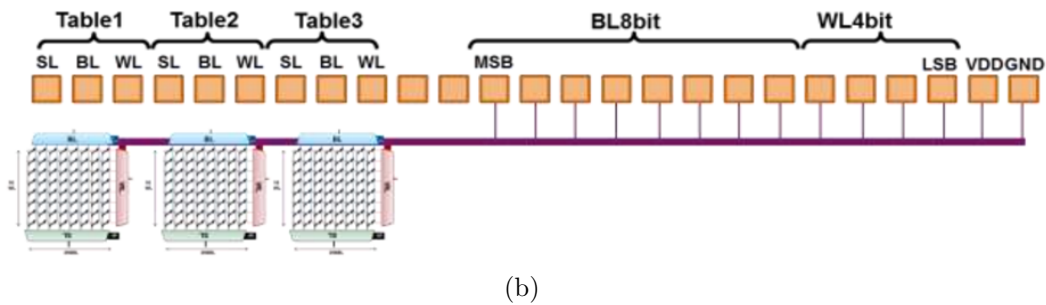
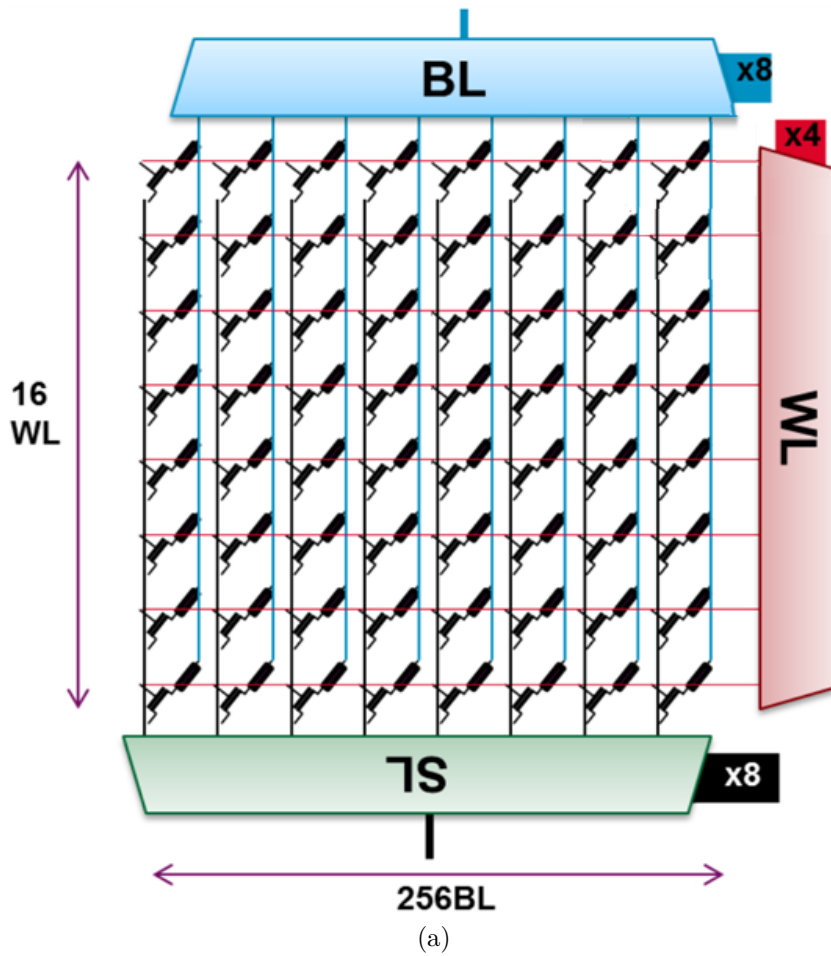


Figure 2.7: (a). 4Kbit matrix array available on MAD tet vehicle. Addressing is made through 265 BL-SL and 16 WL. Specific points of the array are accessed through multiplexers. (b). Barrette diagram over the wafer used to manage 4Kbit matrices. In this case, three arrays are available per barrette.

4Kbit matrices can be included per barrette with three pad per matrix dedicated to enable WL, BL and SL multiplexers. 2 pins over the 25 remain unused. On the contrary, the totality of them is used for bigger arrays. A diagram of the barrettes can be consulted in Figure 2.7(b).

2.3 Experimental methodology

This section presents the diverse programming modes used for the electrical characterization of the introduced stacks as well as the employed testbenches. Through them, in a first stage, feasibility of the stacks can be verified, material responses can be compared and electrical measurements can be linked to material properties or geometrical dimensions. Once devices functionality is verified, main metrics can be studied and compared with the literature. A brief introduction to some of them is presented later in this chapter. **Given that, from a general point of view, same measurement methods and metrics apply to all the stacks studied, it has been decided that, for simplicity, all the measurement examples presented in this chapter, correspond only to ReRAM characteristics.** For the OTS and OTS+ReRAM ones, they can be consulted in chapter 4 and chapter 5 of this work.

2.3.1 Measurement types

Electrical tests constitute a non-destructive strategy to evaluate performances of the studied devices. Basically, three regimes were used: quasi-static programming, pulsed programming and to a lesser degree, staircase programming, which worths to be introduced too.

2.3.1.a Quasi-static programming

Is the most basic programming mode and therefore, widely used in literature to study operational features of the devices tested. It consists in applying a ramped DC voltage over one of the electrodes and to measure the current response over the configuration analyzed (I-V characteristic). Usually, the ramp steps are slow. This is why, this regime is also called DC-mode. In the case of ReRAM and OTS devices, Forming, SET-RESET and threshold voltages values can be extracted, employing both voltage polarities. An example of bipolar ReRAM IV characteristic is reported in Figure 2.8(a). In order to know the resistive states of the devices tested, a DC constant voltage is applied and the current at that point is then extracted. Hence, resistance can be calculated through an Ohmic-law. This process is known as the reading operation. In the case of ReRAM, low magnitude V_{Read} values are used, as presented in Figure 2.8(b).

As previously stated, ramp times in quasi-static mode are slow. Therefore, this programming mode is time consuming and not optimal for lifetime tests, where a big quantity of SET-RESET or switching operations, in the case of ReRAM and OTS, respectively; need to be performed. Besides, dynamic characteristics such like switching times can not be studied using this regime. Finally, the slow time characteristic is not realistic for a device inside an industrial application, where fast speeds are required.

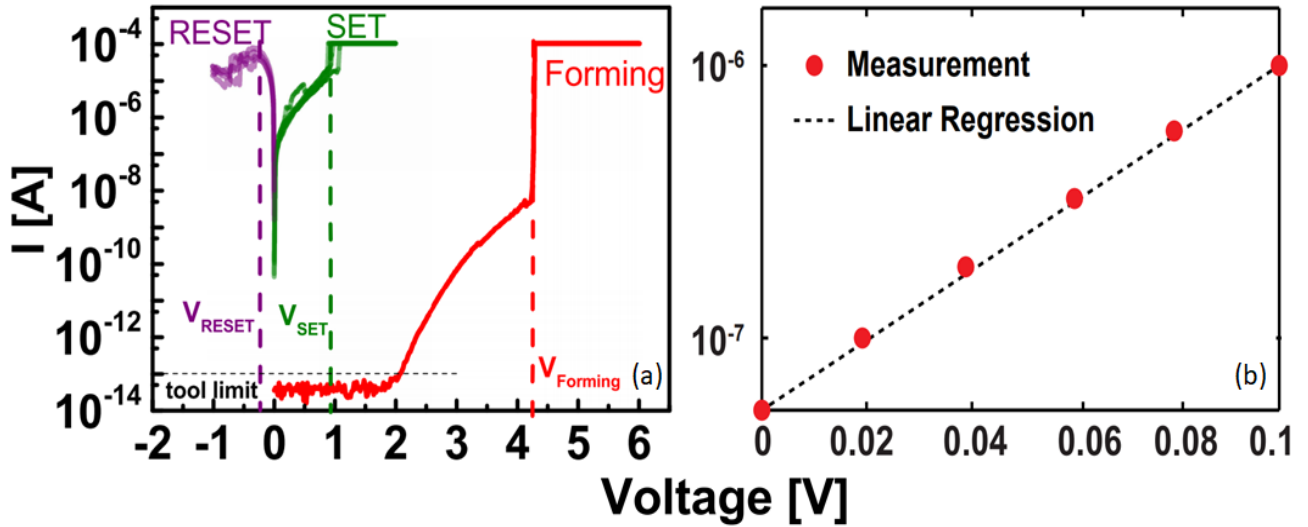


Figure 2.8: (a) IV typical characteristic in a quasi-static programming regime for a CBRAM device. SET, RESET and Forming events can be appreciated. Adapted from: [17]. (b). In the case of ReRAM devices, reading is effectuated thanks to low magnitude ramps. Linear regression and Ohmic law are employed in order to know the resistive value of the tested device. Adapted from: [18]

2.3.1.b Pulsed programming

In order to have a more industrial-like programming approach, the pulsed method or AC mode is used. In this case, dynamic characteristics at high speeds can be analyzed. Positive or negative pulses are applied to the top electrode of the devices under test. Their amplitude, width, shape and rising/fall times can be controlled. Voltage evolution as a function of time over the device under test can be followed (pulse shape), allowing the extraction of the switching values as well as the required time to reach them (see Figure 2.9(a)). Concerning the reading operation, it is normally performed after every switching pulse (Figure 2.9(b)) and consists in another pulse with a low magnitude (i.e. 100mV) and a sampling rate down to 5ns. After every read, an average value of all the individual sample points is extracted to estimate the resistive state of the device under test. Alternatively, read can be effectuated using ramp voltages as in the case of the quasi-static programming regime. However, this approach is much slower and usually is not preferred.

If reading pulses are used, some of the available testbenches are able to adapt the reading time to get reliable values. Self-adaptive reading pulse is also slow. Because of this, current calibration can be indicated at the beginning of the tests. It consists in specifying the expected current range according to the resistive states of the devices under test. For instance, if reading pulses are intended to be applied to pristine devices, current range will target much lower values than in the case of non-fresh devices.

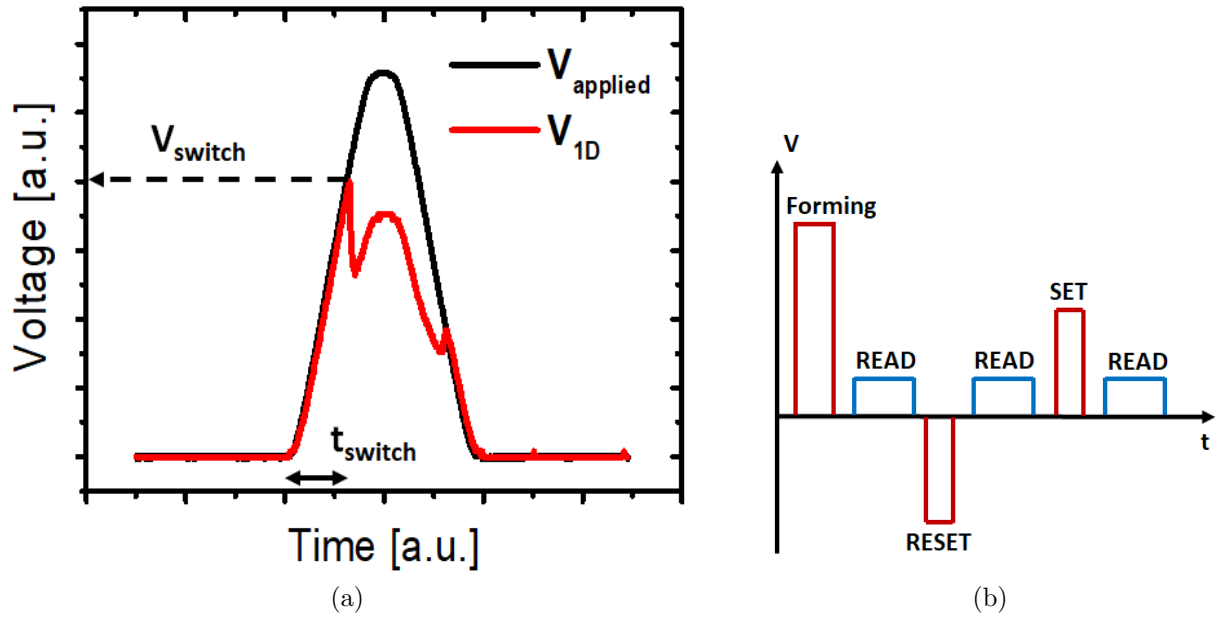


Figure 2.9: (a). Pulse programming example for a 1S1R device. This measurement type allows to study the dynamic behavior of the devices under test and notably the switching times. Rise/fall times, amplitude and pulse width can be controlled. (b). Typical pulse sequence. Normally, read pulses are applied after Forming, SET and RESET operations.

2.3.1.c Staircase programming

In the pulse example presented in Figure 2.9(a), a difference between the applied pulse amplitude and the maximum voltage required by the cell to switch, is appreciated. In cases where the current is not well controlled and if overshoot appears once the switching occurs, this difference can contribute to devices degradation. This is why, staircase pulses with short widths can be used in order to optimize energy consumption and to improve devices lifetime as well as to study switching values. As in the case of the pulsed programming, current sampling can be effectuated over the pulses plateau. An IV characteristic in pulsed mode can be reconstructed too with an adequate voltage step.

2.3.2 Testbenches setup

For the electrical measurements using the diverse programming modes over the stacks presented as well as their architectures; two testbenches were used. One for single devices (1D and 1T1D) and a second one for matrix arrays characterization.

2.3.2.a Single devices

1D and 1T1D electrical measurements in quasi-static, pulse and staircase modes were effectuated using the testbench schematised in Figure 2.10. For the DC regime, a parameter analyzer (Agilent 4156 or Keysight B1500) was in charge of producing the ramped voltage,

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in both polarities, through a Source Measure Unit (SMU). In there, every voltage step takes some milliseconds and current can be controlled by the parameter analyzer once a fixed limit is detected. This method is not optimal since overshoot voltages can not be avoided. The parameter analyzer limits the current flowing through the devices over test, once the fixed limit is surpassed.

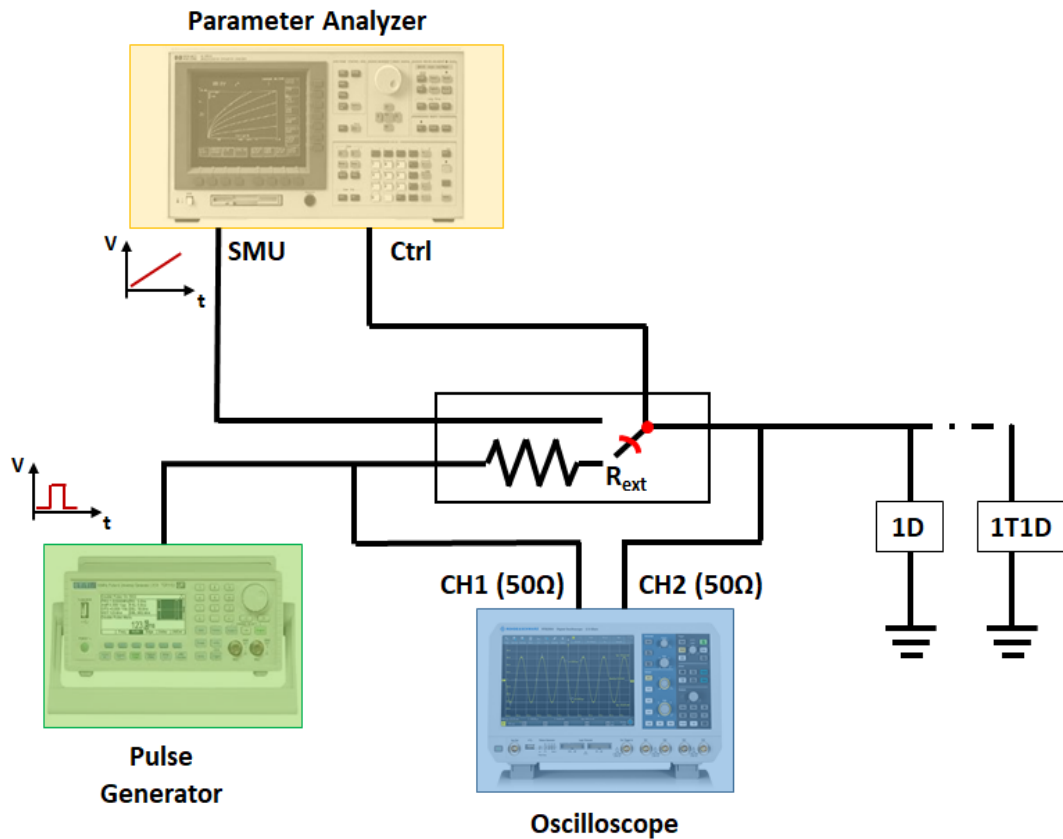


Figure 2.10: 1D and 1T1D configurations are tested thanks to a parameter analyzer (quasi-static mode) and a pulse generator (pulse mode). When transistor is absent, current can be controlled through a the parameter analyzer or a series resistor for the DC and AC regimes respectively. Adapted from: [19]

For the AC mode, pulses are produced by a pulse generator (HP8110A). An external resistor can be used to limit current for the 1D configurations under this regime. An oscilloscope is used to monitor the applied pulse shape as well as the voltage over the device as a function of the time.

2.3.2.b Matrix arrays

In the testbench dedicated to the matrix arrays characterization, analogical and digital blocks can be differentiated (see Figure 2.11). The analogical one performs the write/erase/read operations thanks to a Semiconductor Parameter Analyzer which uses a pulse generator. As for the digital block, an Arduino micro-controller is employed to

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manage the addressing of the right matrix and the selected memory points through the 25 plots previously presented in Figure 2.7(b). Once the performed operation is finished, the pulse generator sends a trigger signal to the Arduino card and it changes the addresses to effectuate a new operation. A card probe is used to connect the testbench to the barrettes over the wafer. The wafers are placed inside an Electrogas 4090 μ equipment.

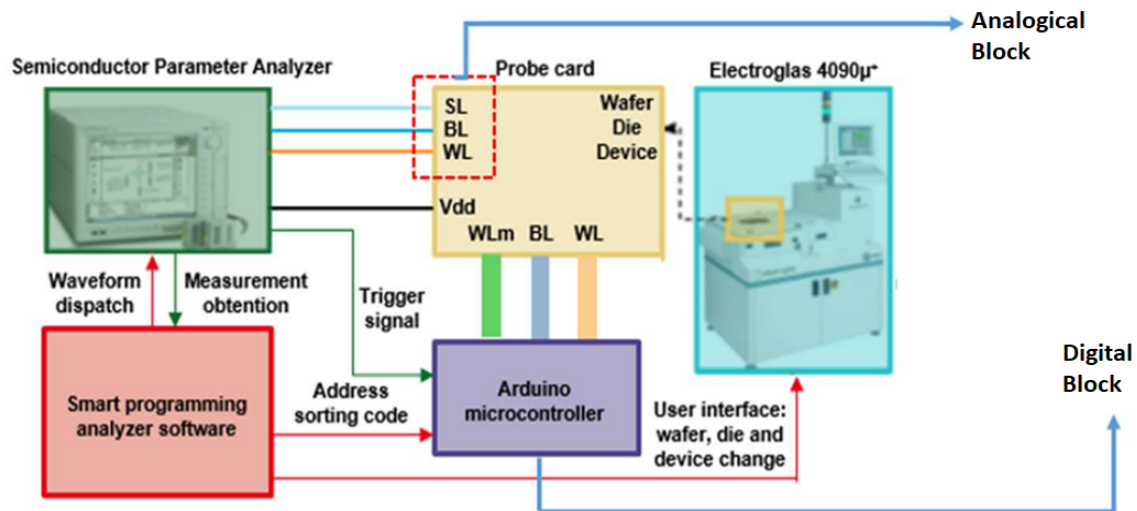


Figure 2.11: Testbench for Matrix Arrays characterizations. Pulses are managed by a Semiconductor Parameter Analyzer equipment while addressing is managed by an Arduino micro-controller. They are connected to a probe card which includes the tips to place over the barrettes on the wafer (Figure 2.7(b)). The 200mm wafers are placed inside an Electrogas 4090 μ equipment. Adapted from: [20]

2.4 Main metrics of the devices under test

- **Quasi-Static cycling**

Once functionality and the main characteristics of the devices under test are verified using the Quasi-static regime, various cycles can be effectuated in order to verify the stability of such electrical behaviors. QS tests are very destructive. This, and the long times that take the ramping voltages, do not allow a big quantity of pulses (≈ 10 in average).

- **Endurance or pulse cycling**

As stated in previous sections, pulsing is the preferred programming method for industrial products. For a ReRAM, endurance or pulse cycling consists in a succession of SET and RESET pulses. Lifetime of devices in terms of switching cycles can be extracted (see chapter 3). In the OTS case, cycling can be studied in both or single polarities, given their electrical symmetry. For 1S1R systems, endurance follows the same methodology that for 1R devices. However, and given the very low currents imposed by selectors at the typical V_{Read} used for resistive memories, new

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reading strategies need to be implemented (see chapter 4 and chapter 5 for further insights), where usually higher reading voltages are employed. To reduce the testing times when a high number of switching cycles are required (>1000), read pulses are applied in a log scale and pulse shapes responses are not extracted. As an example of such test, an endurance behavior for a 5nm HfO_2 OxRAM stack is reported in Figure 2.12.

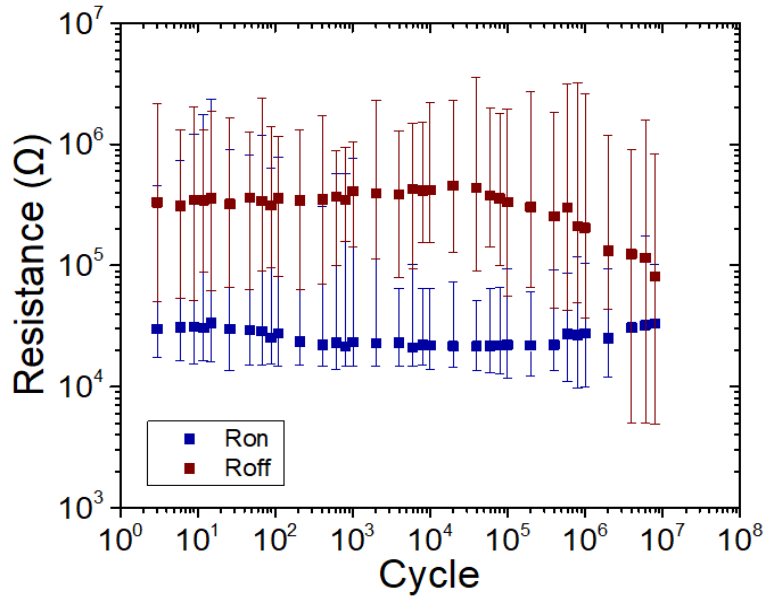


Figure 2.12: Example of endurance test for a 5nm HfO_2 stack studied in this work. Up to 10^7 cycles were applied with logarithmic lectures over 100 devices. Variability of the resistive states was highlighted in subsection 1.7.2 as the main roadblock of ReRAM technologies for SCM applications, and is observed here, through the error bars. They represent all the resistive values obtained at a specific cycle for all the devices tested. Degradation of the HRS state is also appreciated as product of cycling stress.

- **Window Margin**

This metric corresponds to the resistance or current ratio that allows to distinguish the two resistive states once V_{Read} is applied for 1R and 1S1R systems. Its reliability can be affected by the intrinsic variability of the devices as appreciated in Figure 2.12.

- **Data Retention**

Data retention refers to device capability to keep its logic programmed state with time. It is normally tested under high temperature conditions to reduce the testing time. Retention times at lower temperatures are then extrapolated using the Arrhenius law. This temperature dependence implies that every application will present specific retention requirements. Figure 2.13 presents resistive state variations of ReRAM devices programmed in HRS and LRS at 130°C with logarithmic reads. A failure retention time can be extracted for the stack tested. For the example

reported, it appears once the median value of cells initially programmed either in LRS or HRS, reaches a 25% variation.

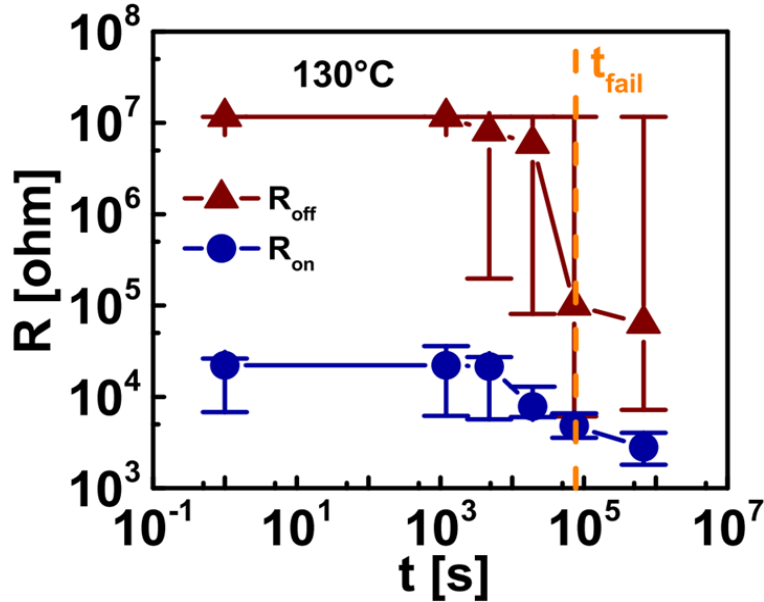


Figure 2.13: Retention curve with failure time extraction at 130°C. Taken from: [1]

For OTS devices retention refers to leakage currents and threshold voltages variations with time. This is a critical metric, given that chalcogenide materials present, for instance V_{th} drift [21].

- **Non-selected devices disturb**

In this work context, this last metric is inherent to OTS devices. In crossbar configurations, write/erase and read operations can affect the programmed states over non-selected devices. Hence, this test consists in analyzing the electrical behavior of the OTS used in the sub-threshold mode and as a function of the polarization technique chosen to operate the array (such polarization methods are treated in subsection 4.5.1). Leakage currents should remain unchanged and devices switching must be inexistent. These conditions should be kept by several orders of magnitude if compared with endurance cycling, given that reading operations are very frequent in crossbar arrays.

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Endurance Statistical Behavior of Resistive Memories Based on Experimental and Theoretical Investigation

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STORAGE Class Memory applications (SCM) are destined to fill the gap between logic and storage memories, offering non-volatility, low-power consumption, high speeds, good scalability and high density, among others. As previously discussed in section 1.4 mainly two SCM types can be distinguished: Memory (M-type) and Storage (S-type) SCM. As its name suggest it and if compared to the Memory Hierarchy previously discussed in section 1.1, M-type performances need to be closer to the lowest memory block, DRAM, whereas S-type performances could notably improve the highest storage one, Flash (see Figure 1.2 and Figure 1.4).

Among the various candidates for SCM, Phase-Change Memories (PCM), Spin-Transfer Torque Random Access Memory (STT-RAM) and both types of Resistive RAM (ReRAM), oxide based (OxRAM) and conductive bridge (CBRAM); are the most studied technologies [1]. This is mainly due to their two-terminal and Back-End-of-Line compatibility (BEOL). From a general point of view and given their higher endurance and low latency times, STT-RAM seems more adapted for M-type SCM, while scalability, 3D-integration and Multi-Level Cell capabilities, make of PCM and ReRAM more plausible alternatives for S-type SCM. This storage tendency can be confirmed in Figure 3.1, where the major industry functional test vehicles presented in the last years for these three SCM candidates, are reported. Company names as well as storage capacities and conferences where such test vehicles were presented are indicated. In the case of interest for this thesis work, ReRAM technologies up to 32Gb, were obtained by Toshiba few years ago.

As stated before, ReRAM technologies seem more adapted for S-Type SCM. They present good scalability ($< 1\mu m^2$ per unitary cell) [3], low power consumption ($< 75pJ$) [4], fast writing and erasing processes down to some ns [5]. If compared to another main candidates among emerging memories for S-type SCM applications such as PCM, ReRAM technologies present a lower power consumption as well as faster latency times. Cycling endurance up to 10^{12} SET/RESET cycles has been demonstrated in literature [6, 7]. For S-type SCM, the latter is an important figure of merit, with at least 10^6 programming cycles being required [8]. Endurance dependence on current, voltage and pulse width applied during cycling, as well as its optimization [9] even when neuromorphic applications are targeted [10], have been treated. These works have contributed to the comprehension of the mechanisms governing ReRAM endurance, as well as the main factors affecting devices lifetime. However, in order to reach a better diagnostic of the in-depth physics taking place during cycling, the trends already obtained require to be expanded to a wider variety of memory stacks and programming conditions.

Previously highlighted and treated in subsection 1.7.2, LRS and HRS highly dispersed values over the switching times and cycle to cycle variations, are one of the main road-blocks for resistive memories commercialization along with fabrication costs per bit, which remain higher when compared to those ones of widely used technologies. This is why, and even if several test vehicles as those reported in Figure 3.1, have been presented, ReRAM available products are produced at small scale and destined for niche markets. Because of this, and in order to increase attractiveness of ReRAM technologies for industrial applications and S-type SCM in terms of endurance cycles, variability studies require broader populations. Hence, stochastic nature of this phenomenon needs to be investigated. Most

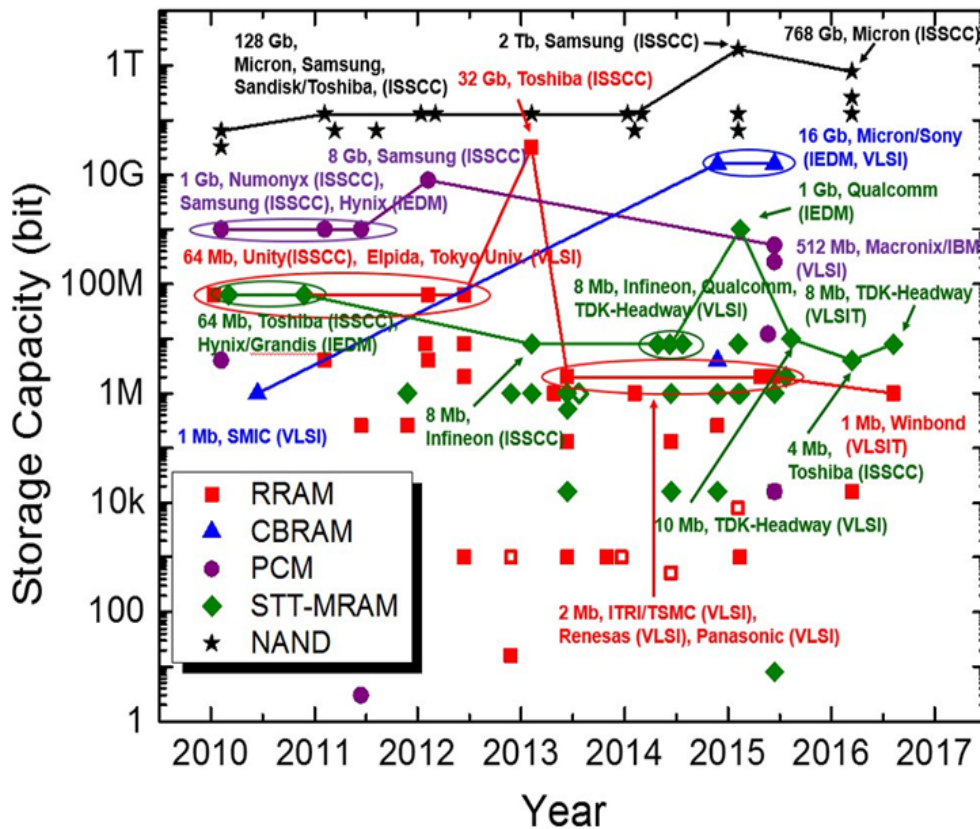


Figure 3.1: PCM, STT-RAM, ReRAM, and CBRAM, main industrial vehicles presented in the last years are summarized in terms of Storage Capacity. For the ReRAM case, up to 32Gb have been reported. Taken from: [2]

of the studies on ReRAM variability are focused on the analysis of LRS and HRS distributions [11, 12] but device to device (D2D) endurance dispersions have been barely studied. Its statistical addressing, to our knowledge, is lacking in literature. Selecting and programming methods need to be validated at the array level. Conversely, and since a modeling perspective, endurance distributions have not been yet formally studied, even if some alternatives exist, in order to understand endurance failure mechanisms and ReRAM reliability [13–15]. As far as we know, models for endurance cycling at the statistical level, are still missing too.

This chapter is intended to improve the lack of data and understanding concerning the failure mechanisms and its variability D2D. In a first stage, a diagnostic on ReRAM intrinsic dispersions and the failure mechanisms is developed through a literature overview. Next, the samples used for electrical characterization are presented. Then, all the measurements carried out in order to analyze the maximum number of cycles N_{cmax} distributions and its variability, are discussed. The results are validated over various programming conditions and technological splits. Finally, a probabilistic model is developed to understand the experimental results and based on observations extracted from ramp voltage stresses (RVS) responses, analyzed as a function of the number of programming cycles.

3.1 A general overview of ReRAM variability and failure mechanisms produced by programming cycling

3.1.1 ReRAM variability

Bipolar ReRAM is more energy-efficient and more stable than the unipolar type [16, 17]. Because of this, only the former is considered for this work, as it has been the tendency for the research and development of resistive memories during the last years [17].

Resistance difference between HRS and LRS states is explained by ion migration under electrical field stimulus. It allows the creation or dissolution of conductive filaments inside the active switching layers, composed of oxygen vacancies or metallic cations for OxRAM and CBRAM, respectively ⁽¹⁾. Switching is possible thanks to Joule heating and ions hopping through a filamentary configuration of localized states, also called defects/traps, and first generated by the forming process. These explains the higher energy levels required for FORMING operations. Prior to it, a pre-established localized states configuration is not available. The process is capital in order to define filament geometry, which determines the switching behavior for the subsequent cycles [18].

As for the forming values, area dependence has also been demonstrated and studied. With size scaling, forming voltages increase and become more dispersed as observed in Figure 3.2. These results confirm a bulk conduction mechanism for pristine devices. The tendency can be explained at the intrinsic level, as a consequence of the less available area to generate the defects that form the conductive path with device shrinking [18]. An additional aspect worth to be mentioned concerning the forming variability, is the fact that cells requiring higher forming energies in the distributions, tend to present larger switching variability for the subsequent cycles as well as a faster wear out time as demonstrated by Grossi *et al.* in [19].

The FORMING/SET operations are widely known to be soft breakdown phenomena [21, 22]. They begin with generation of defects inside the oxide layer. Then, and once a critical density of them is reached, previously nucleated defects begin to grow to link the two conductive electrodes and to generate the switching event. Their growth occurs in the direction of the electric field. Once LRS is reached, the percolated path expands laterally until voltage over it is very low (highly conductive filament) [23]. On the other hand, RESET process consists in the dissolution of some of the generated defects in order to **break** [22] or **shrink** [24] (according to divergent theories) the conductive filament and to restore the HRS. In the case of OxRAM devices, RESET is explained by the migration of the oxygen ions inside a "reservoir" in the Top Electrode (TE), back into the oxide [17] to recombine with the oxygen vacancies, whereas for the CBRAM case, some of the metallic cations are taken back into the TE thanks to an electrochemical or Faradic current [25].

⁽¹⁾For more detailed explanations on ReRAM topologies, please refer to subsection 1.3.5

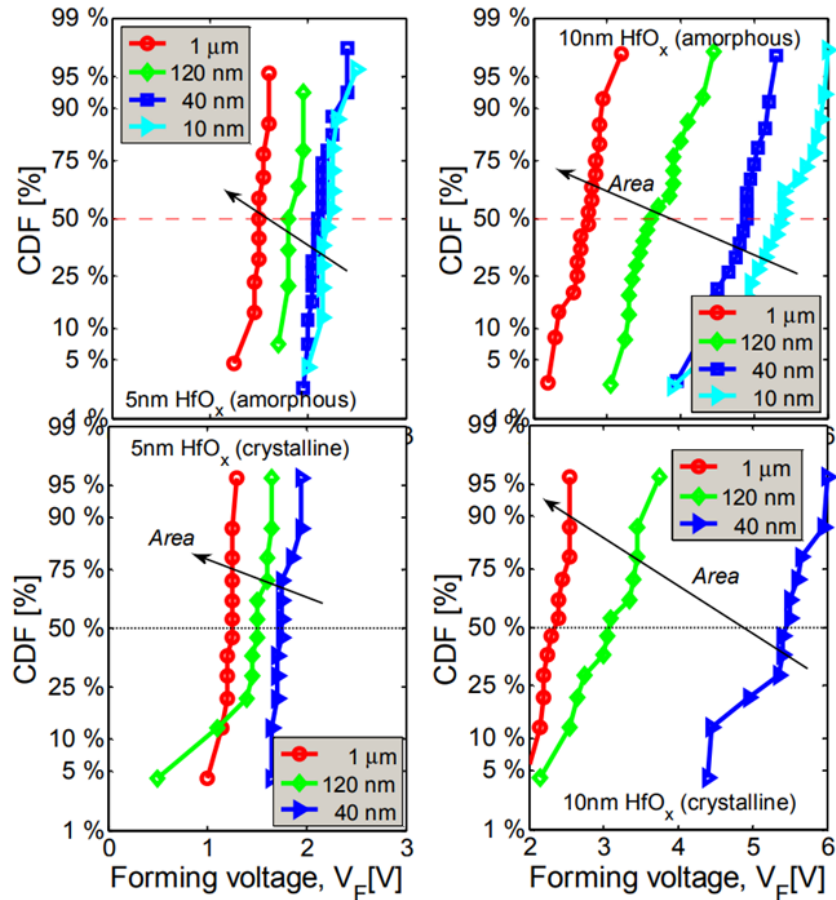


Figure 3.2: Forming voltage dispersions as a function of the device size for HfO_x 5 and 10 nm thick. Two configurations are presented, crystalline (annealed stack) and amorphous oxide. Taken from: [20]

Historically, dielectric breakdown is known to be a stochastic process [26]. As a consequence, creation and dissolution of conductive filaments by ionized defects, also are. Defects migration is a random process where parameters such like activation barriers, migration rates and positions inside the oxide layers, are usually modeled as stochastic events [22, 23]. It implies that every switch generates diverse conductive filament shapes and sizes [23], leading to different LRS and HRS values, as well as switching times. Usually, and as observed in the example in Figure 3.3, HRS is more dispersed than the LRS. This is explained by the saturation that at some point reaches the filament in the LRS, reducing variability and the effective switching area (lower percentiles of the LRS distribution). Hence, less possible paths for conduction are available once switching is reached [22, 24, 27, 28]. On the other hand, for the HRS, and accepting broken filament theory, the current level, which hardly reaches saturation, is exponentially dependent on the gap size between the residual filament and the Bottom Electrode (BE) [22, 23, 29, 30].

All the above-mentioned aspects refer to intrinsic factors and lead to C2C and D2D variability of ReRAM. Extrinsic parameters such like impurities inside the oxide layers due to lack of processes maturity, circuits designs or arrays dispositions, would increase

LRS and HRS dispersions for both C2C and D2D cases.

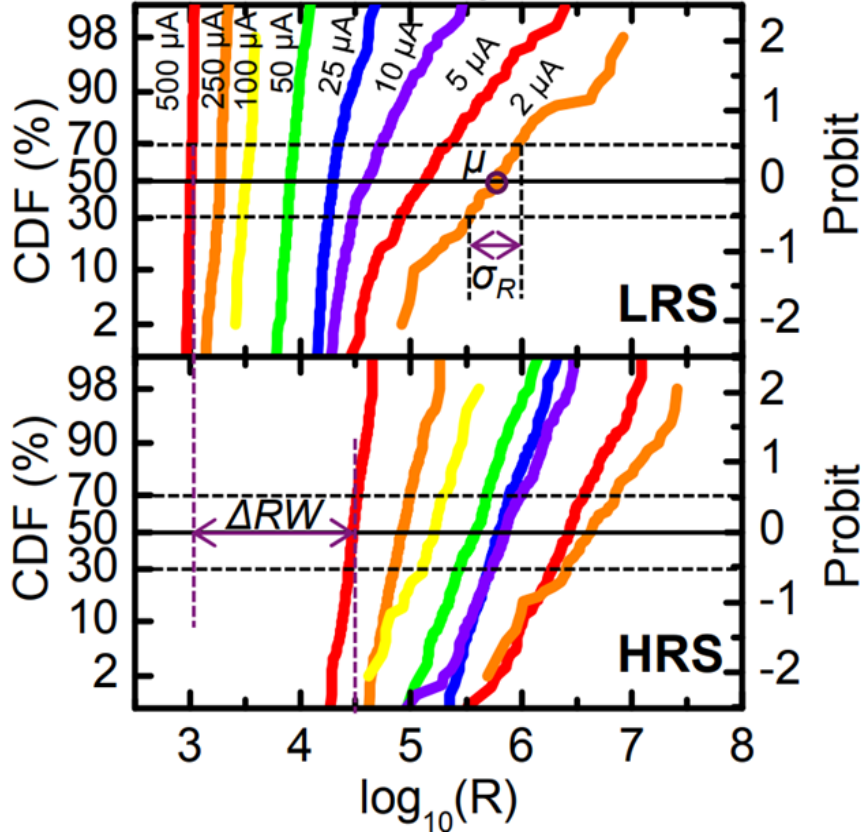


Figure 3.3: HRS and LRS Cumulative Distribution Functions (CDF) for diverse compliance currents applied to a $TiN/HfO_2/Hf/TiN$ 5nm stack. It can be appreciated how the resistive states are highly distributed and how the HRS dispersion is higher. Standard deviation and median values are also indicated as well as the Resistive Window (RW). Taken from: [24]

Further studies on the LRS and HRS distributions, explored the link between the median values μ_R and the standard deviations σ_R of such dispersions [11, 12, 23, 24, 31]. As appreciated in Figure 3.4, where various technologies from literature are compared, higher μ_R leads to increased σ_R . It has been established that, **for median values higher than $1/G_0$** , dispersions follow a log normal distribution, with $1/G_0 = 12.9K\Omega$. $G_0 = 2e^2/h$, where h is the Planck constant and e the electron charge, is the quantum conductance unit, from the QPC model, and is equivalent to the creation of a single conductive filament [12, 32, 33]. In this case, standard deviation can be estimated using the equation:

$$\sigma_R = \sqrt{G_0 \cdot \exp(-\alpha\phi) \cdot \mu_R^{1.5}} \quad [12] \quad (3.1)$$

With α being the barrier width if a parabolic longitudinal potential on the electric field direction is assumed; and ϕ standing for the barrier height. Equation 3.1 has been also compared for C2C and D2D variabilities. For resistances higher than $1/G_0$, normally

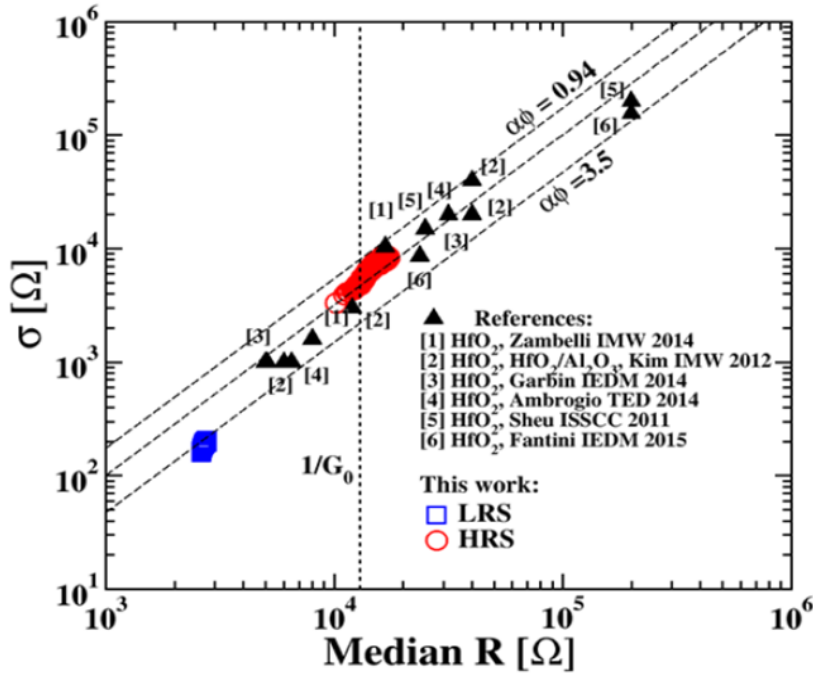


Figure 3.4: Standard deviation (σ_R) as a function of the median value (μ_R) from various works in literature. Higher μ_R imply higher dispersions quantified by σ_R . LRS and HRS values are presented. Taken from: [12]

inherent to the HRS, C2C variability is bigger [12]. This result implies lower $\phi\alpha$ factors in equation Equation 3.1 for cycled cells, which leads to suppose either barrier width or activation barrier reduction. *This hypothesis is somehow confirmed by the results of the numerical model developed later in this chapter.*

For values lower than $1/G_0$, dispersions follow a Gaussian behavior. The direct consequence of this is the steeper slope of the LRS values observed in Figure 3.4. Both Gaussian and log normal distributions for the LRS and HRS states below and above $1/G_0$, respectively, could explain the bimodal characteristic obtained for LRS dispersions [24, 34], where upper percentiles are eventually higher than $1/G_0$.

At this point, it is important to mention that even if the resistive states and switching times of resistive memories are highly variable, they present an universal behavior as already discussed in section 1.3.5.b. The ohmic regime for the LRS, implies that higher compliance currents or longer pulse widths, generate thicker filaments, which will be harder to dissolve. Analogically, the number of ions removed during RESET is also dependent on the applied energy ($E = VIt$). Higher RESET voltages imply larger gaps. One could deduce an interdependence between the LRS and HRS median values as already observed in Figure 3.3. Electrical characteristics of the precedent operation as well as the actual resistive state, could be profited in order to predict the most probable next one, as a function of the operation to perform. This aspect could be used by neuromorphic applications based on Multi-Level Cells programming as it is the case in [35].

Finally, several variability improvement strategies are possible. They include ion im-

plantation [34, 36], nanocrystals insertion inside the switching layers [37], dopant diffusion [38], or correction techniques during programming. For the latter, besides higher latency times once correction is needed for specific cells, endurance or retention degradations can be expected [39]. Moreover, if intrinsic variability of ReRAM stacks is prior quantified, applicability for specific applications is still possible [39].

3.1.2 Endurance failure mechanisms of ReRAM

With variability of switching times and resistive states of ReRAM introduced above, this section presents the failure mechanisms during cycling. A device is said to fail if after some SET/RESET cycles it is not functional anymore, i.e. the window margin is not enough to keep the ReRAM reliable. In the case of interest for this work, and as mentioned before, S-type SCM requires at least 10^6 programming cycles [8] at the array level, in order to be an interesting alternative to FLASH technologies, for whose the endurance is typically 10^5 [40]. At the cell level, promising performances up to 10^{12} cycles were demonstrated [6, 7]. This result, increases attractiveness of ReRAM for high-endurance applications like embedded [40] or neuromorphic topologies, where deep learning times are required [39].

Three main failure mechanisms have been identified [40]: resistance drift, memory stuck in HRS and in LRS. They are presented in Figure 3.5 and shortly introduced next:

- In the case of a **ReRAM stuck in the HRS**, the issue is caused by a very high current during the RESET operation, which erases a big portion of the filament. Sometimes, like in the Figure 3.5(a) case, even higher HRS values if compared with the median ones during cycling, can be observed.
- In some cases, the resistance window is lost and the resistive value of the tested cell tends to go into an intermediate value between the HRS and LRS median values as observed in Figure 3.5(b). It is the less common failure mechanism and occurs over some devices when programming conditions are near to balanced ones in terms of applied energy. Known as the **resistance drift** failure mechanism, it is thought to be caused by the stochastic nature of the creation and dissolution of conductive filaments.
- For **ReRAM stuck in LRS** this is mainly due to a high programming current during the SET operation. Applied energy during the RESET is not enough to bring back the device into the HRS (see Figure 3.5(c))

Additionally to the failure mechanisms already introduced, there is another one known as **Hard Breakdown**. In there, the memory goes into a highly conductive state and can not be RESET anymore. In [41], Barci *et al.* demonstrated that the resistance drift and the memory stuck in LRS or in HRS, are temporary writing failures (TWF) and can be solved by delivering more energy during the SET or RESET subsequent operations. Recently, Grossi *et al.* [39], showed that, at the statistical level, memory stucked in LRS or HRS occurs before the hard breakdown. It was also established, that even if such TWFs

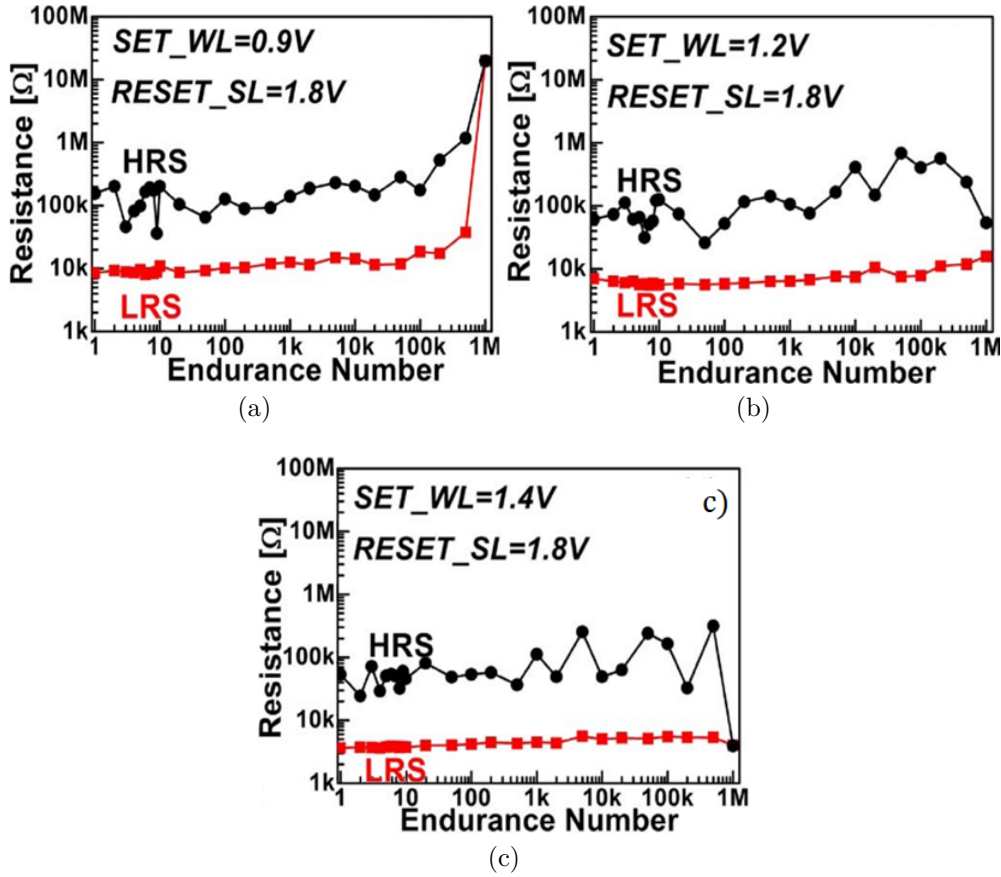


Figure 3.5: Endurance failure mechanisms: (a) HRS stuck, (b) Resistance drift to an intermediate state between LRS and HRS, and (c) LRS stuck. For the latter, the LRS value where the device sticks is usually a little bit lower than the median value observed during cycling. Once this occurs, devices are broken (Hard breakdown), and can not be RESET again. Adapted from: [40]

can be corrected, cells undergoing them, tend to endure less programming cycles. To avoid mixing between TWFs and hard breakdown cells in our statistical studies, programming and reading algorithms during cycling, were optimized in order to obviate TWFs. Hence, in this work, the hard breakdown is quantified by the maximum number of cycles N_{cmax} metric, taken once $R_{on} \approx R_{off}$. Thus, programming conditions, ReRAM technology and oxide thickness influence over reliability at the array level, can be compared.

3.2 Technological details

To widen the scope of this work, stacks for both ReRAM types were studied: the endurance measurements were performed on HfO_2/Ti OxRAM and $Al_2O_3/CuTe_x$ CBRAM, which are integrated using the Memory Advanced Demonstrator (MAD) test vehicle developed by the CEA-Leti (see subsection 2.2.2 for further details). Therefore, they are

Chapter 3: ReRAM Reliability Studies

integrated between VIA 4 and Metal 5 of a 130nm CMOS. For the results presented in this chapter, devices size was 300nm formed by DUV lithography. The transistor connected with the memory devices in a 1T1R configuration was used as selector and to control current flowing through the devices as it can be appreciated in Figure 3.6. There, an schematic of the stacks employed is also presented. For the CBRAM case, 2.5 to 4nm oxide thickness were characterized, whereas for the OxRAM devices 5 to 10nm thicknesses were used. Conventional compliance current ($100\mu A$) and pulse width ($1\mu s$), were applied for most of the reported results.

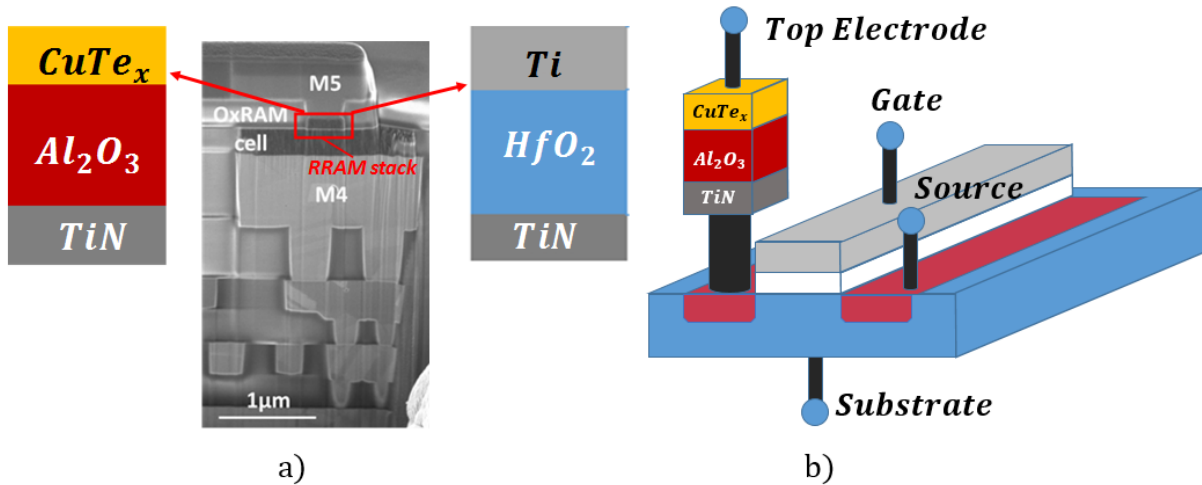


Figure 3.6: (a). TEM cross sections and schematics for the studied stacks (CBRAM $Al_2O_3/CuTe_x$, OxRAM HfO_2/Ti). (b). Schematic of the 1T1R structure used in this work.

3.3 Experimental Results

For this chapter studies, 4 kb arrays were used with a population of at least 120 cells with 10^7 SET/RESET cycles applied per programming condition tested. Read pulses (0,1 V) were employed after SET or RESET operations in logarithmic intervals, in order to know the HRS and LRS evolution along cycling, reducing test time. Using the schematics presented in Figure 3.6 as a reference, pulses are applied at the Bit Line (Top Electrode of the stressed memory) for FORMING/SET/READ processes, whereas positive voltages are applied to the Source Line in the case of RESET (source of the transistor). The Word Line (Gate of the transistor) voltage, is used to regulate the current flowing through the structures tested during Bit Line bias. For the RESET operation, the transistor gate is biased at a high voltage in such a way that series resistances are minimized and to get an acceptable window margin between the ReRAM resistive states. In order to maximize the control of the conductive filaments, a *smart procedure* is used during FORMING. It consists in incremental pulses application in order to stop them once a LRS threshold is reached [42]. To do so, reading pulses are used after every step of the incremental procedure which implies long forming times, while optimizing devices lifetime.

3.3.1 Maximum Endurance Statistics and Hard Breakdown Evidence

As introduced in subsection 3.1.2, hard breakdown or N_{cmax} is the process where LRS stuck becomes permanent after cells have been cycled a specific number of times. Once it appears, devices under test can not be RESET anymore and the read resistance is usually lower than the LRS median values obtained during the cycling, as observed in the example presented in Figure 3.7(a), where an endurance curve for a CBRAM stack is presented. The points over the curve correspond to the median values of every resistive state (LRS and HRS), while error bars refer to $\pm 1\sigma$, with σ being the standard deviation of the dispersion. For the CBRAM case, around 100 cycles are required in order to get a steady HRS median value as well as a lower standard deviation. As for the lifetime of the devices, it can be also observed that median value of 10^6 cycles is obtained, before reaching the N_{cmax} . Even if this value fulfills the endurance requirement for S-type SCM, it can be also appreciated how N_{cmax} is highly dispersed for the D2D measurement undertaken. Conversely, the OxRAM stacks (Figure 3.7(b)) present a better endurance reliability and less dispersed values for the HRS. However, the Window Margin (WM) is lower. The straightforward consequence of this, is the possibility of conducting endurance failure measurements at a more reasonable pace over CBRAM stacks for our N_{cmax} studies. This first conclusion was then confirmed running several additional tests. Because of this, and taking into account that the main objective of this chapter was to study the influence of the programming conditions over the endurance behavior at the array level, most of the results presented in this chapter, used CBRAM devices.

OxRAM devices present a lower WM (WM) during the cycling programming if compared to CBRAM, as already mentioned. As for C2C distributions, it is also observed that HRS values of CBRAM stacks are also more dispersed. This confirms, once again, the trade-off among ReRAM performances [43], i.e. retention, endurance, and WM. This is an interesting observation in terms of programming conditions. An optimal one should allow to have a clear and reliable separation between HRS and LRS, with stable states as long as possible with devices cycling. As observed, it can be difficult, given the evidenced trade-offs. Hence, best programming strategy needs to be application oriented as a function of the WM of the endurance required.

N_{cmax} dispersions can be quantified as observed in Figure 3.8, where distribution for the maximum number of cycles is extracted from Figure 3.7(a). It can be appreciated how the maximum number of cycles decreases from 10^6 for the median value to 10^5 for a 2σ quantile, equivalent to 98% of the population analyzed. The N_{cmax} behavior, shows that this metric presents a log normal law. It indicates that the number of cycles required to reach the hard breakdown, presents a normal distribution (straight line in Figure 3.8 with the N_{cmax} being in logarithmic scale).

For the following step in our studies, endurance measurements were conducted over diverse stacks including both ReRAM topologies and various thicknesses. N_{cmax} distributions for some of the tests undertaken, are reported in Figure 3.9, hence validating the same normally distributed characteristic of this metric. Given the great amount of

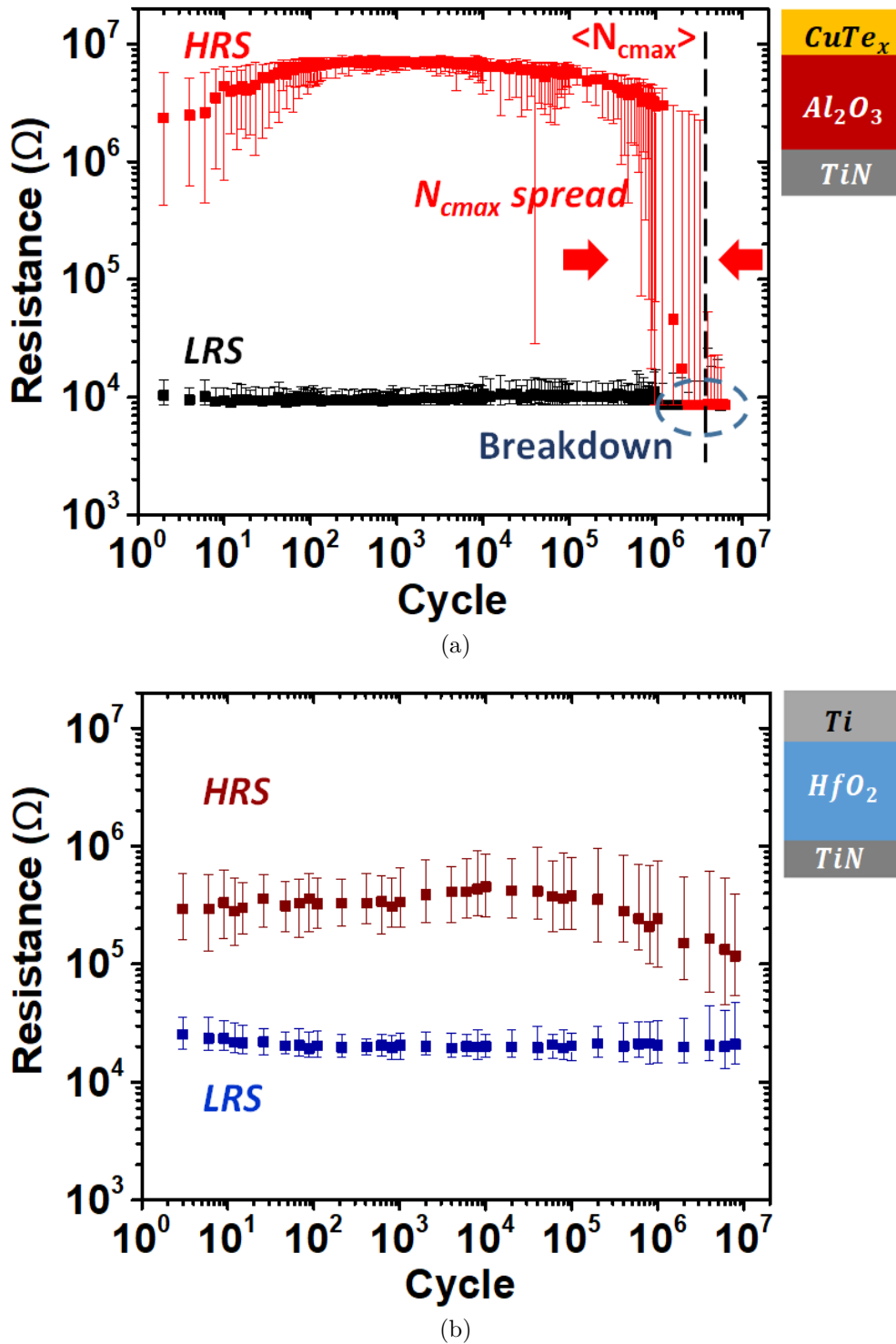


Figure 3.7: Typical ReRAM endurance characteristics for 120 cells for (a) CBRAM and (b) OxRAM. $\pm 1\sigma$ C2C dispersion (Standard deviation) is shown.

data gathered during these endurance tests, only some illustrative endurance behaviors are presented in Figure 3.9.

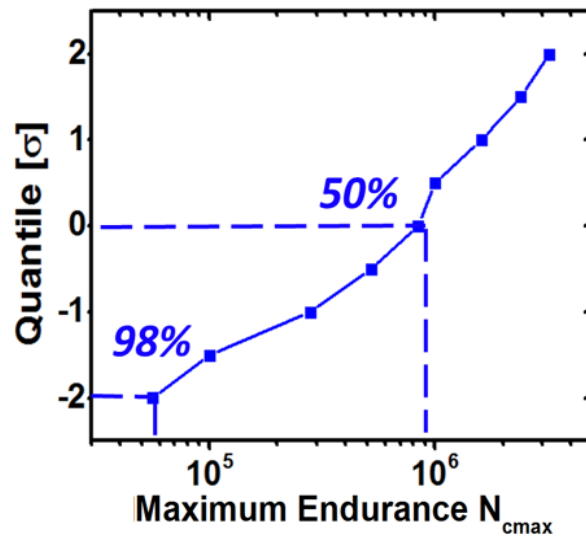


Figure 3.8: Extracted distribution of the maximum number of cycles. N_{cmax} spread is put in evidence at the array level.

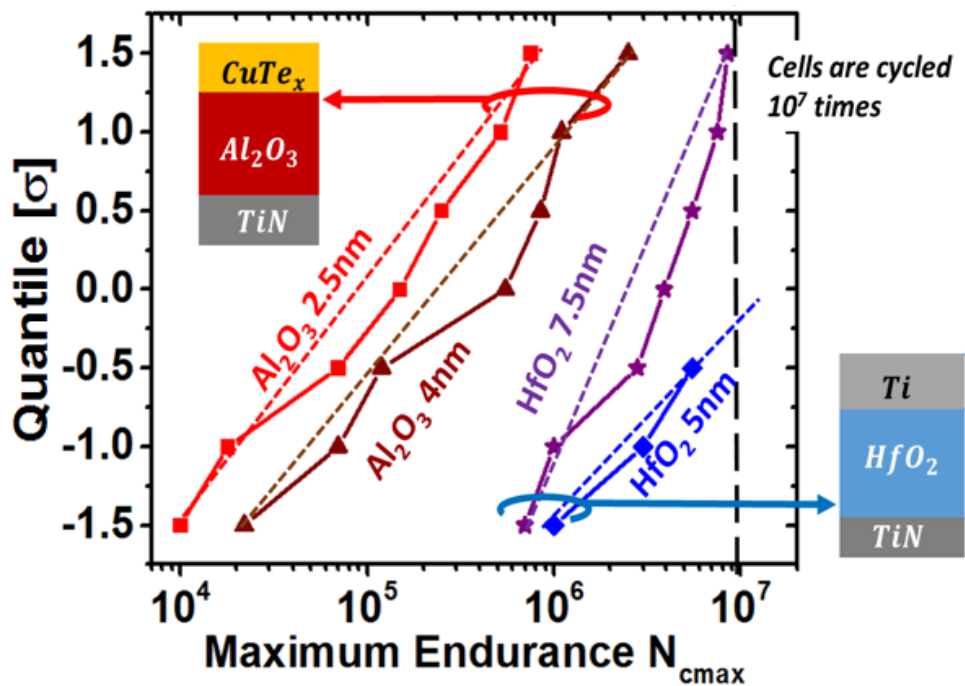


Figure 3.9: Measured maximum endurance distributions for CBRAM and OxRAM stacks for diverse programming conditions and oxide thicknesses. Log-normal law from Figure 3.8 is confirmed for any case. Besides, it can be observed how the OxRAM stacks employed in this study endure more programming cycles compared to the CBRAM ones.

3.3.2 N_{cmax} statistics as a function of the applied programming conditions

After validation of the log normal behavior of the N_{cmax} distributions, this section studies SET and RESET voltages influence over such dispersions. To do so, an $Al_2O_3/CuTe_x$ stack was selected with an oxide thickness of 3.5nm. Through a screening of SET/RESET programming conditions, degradation mechanisms as a function of the applied energy and hard breakdown dispersions can be investigated.

Firstly, V_{SET} variations were effectuated keeping V_{RESET} voltage constant. Figure 3.10(a), shows N_{cmax} distributions for several SET voltages varying from 2.8 V to 3.2 V. It is observed how SET variations do not really have influence over the N_{cmax} median values. Tails on the distributions can be appreciated for higher V_{SET} . Figure 3.10(b), presents N_{cmax} as a function of V_{SET} for various RESET voltages as well as the standard deviations from the obtained dispersions. There, tendency from Figure 3.10(a) is confirmed. To quantify the impact of V_{SET} over the distributions tails, slopes of the dispersions obtained in the previous graph as a function of the V_{SET} , are presented in Figure 3.10(c). Large SET voltages during programming cycling are found to generate more dispersed hard breakdown values. This suggests that the application of larger energy during the SET process could lead to endurance degradation of the array, given that a few cells will be broken earlier even if the N_{cmax} median value is not significantly impacted. On the other hand, higher energies applied per cycle will lead to less dispersed D2D distributions too.

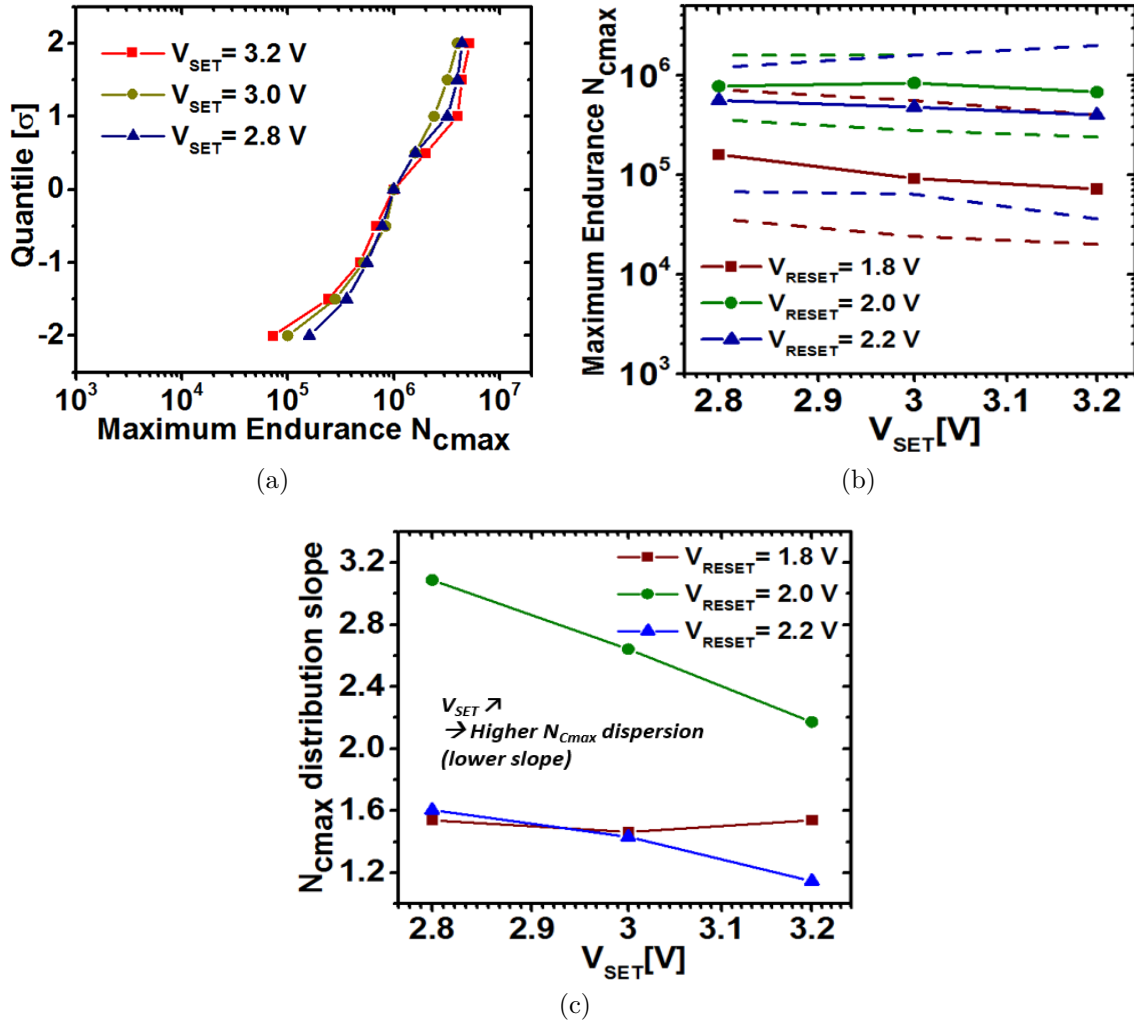


Figure 3.10: (a) Maximum number of cycles distributions for various SET voltages for a constant RESET value. (b) Maximum number of cycles as a function of V_{SET} . Dashed lines correspond to standard deviation. (c) Slope of the N_{cmax} distributions extracted from Figure 3.10(a).

Similar measurements were undertaken aiming to analyze RESET influence. Figure 3.11(a) depicts N_{cmax} distribution for various RESET voltages for fixed V_{SET} . In this case, a bell shape is observed for $\langle N_{cmax} \rangle (V_{RESET})$ as shown in Figure 3.11(b). As V_{RESET} increases, N_{cmax} first increases given a better efficiency on the filament dissolution and then decreases due to a higher stress over the dielectric that leads to earlier hard breakdown. Figure 3.11(c) presents the same trend for distribution slopes. These results are consistent with those previously presented [13, 43, 44], where it has been demonstrated that V_{RESET} has a more important influence than V_{SET} over the endurance behavior of single cells. These new results go further by not only confirming the RESET conditions influence the median N_{cmax} at the array level, but also significantly modifies the failure spread.

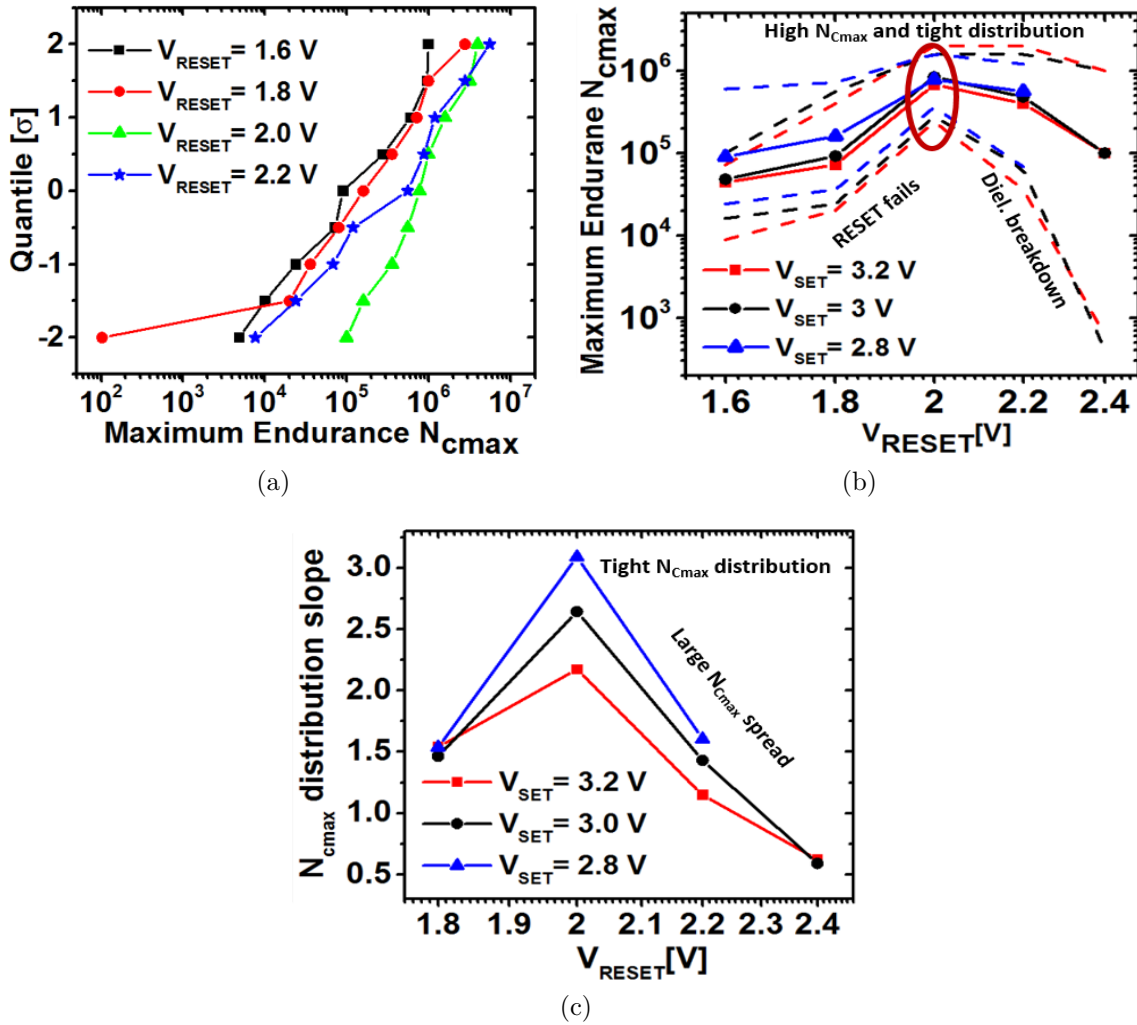


Figure 3.11: (a) Maximum number of cycles distributions for various RESET voltages for a constant SET value. (b) Maximum number of cycles as a function of V_{RESET} . Dashed lines correspond to standard deviation. (c) Slope of the N_{cmax} distributions extracted from Figure 3.11(a).

The previous conclusion concerning RESET influence over N_{cmax} median value and its dispersions, resides in the fact that, for this work, series transistor is not used during it. For every RESET operation, a big quantity of defects is intended to be removed, aiming to have the highest WM possible, hence justifying the use of a higher current density prior to the switching event. This also demonstrates the importance of an accurate current control method in order to increase ReRAM reliability. Moreover, adjusting the programming conditions is proven to be a significant parameter to optimize both cells lifetime and endurance variability. An optimized V_{RESET} allows to improve the trade-off between the endurance and the WM, as observed in Figure 3.12, where the Window Margin as a function of the N_{cmax} for a big variety of programming conditions, is presented. Best endurance performances were measured for $V_{RESET} = 2V$.

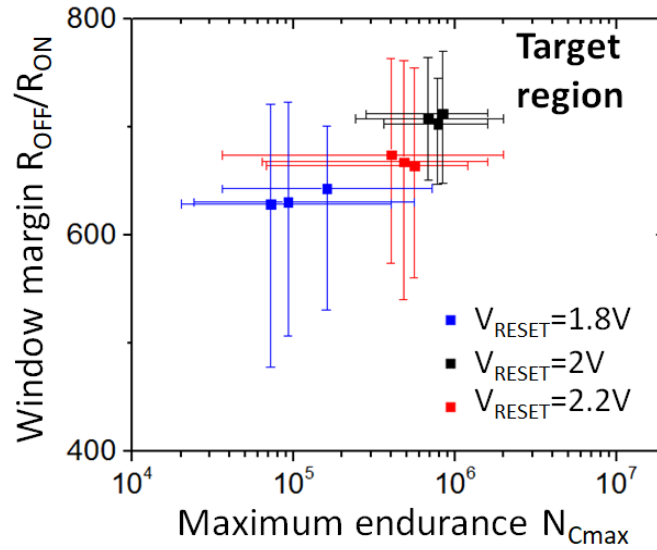


Figure 3.12: Window Margin (WM) and maximum endurance dependence for various SET and RESET conditions. Error bars correspond to the standard deviation of each programming conditions. RESET value is capital in order to get less dispersed and higher N_{Cmax}

3.3.3 Gradual Degradation Phenomenon

Switching processes have been widely studied in literature and several models to describe them were also proposed [45–47]. These studies showed that FORMING and SET events are closely related to breakdown in high-K dielectrics especially when oxides are used inside Metal-Insulator-Metal structures (MIM), as it is the case of capacitors or transistors gate oxides. Transition from the HRS to LRS is a product of oxygen vacancies (OxRAM) or metallic ions (CBRAM) that nucleate and grow to form a conductive filament [43].

Constant Voltage Stress (CVS) is the most used technique in order to extract parameters such as the Time Dependency to Dielectric Breakdown (TDDB), due to its simplicity and easiness of implementation at the circuit level. In the case of ReRAM, some studies used it to analyze the FORMING and SET operations [48]. However, this approach is long time consuming [49]. To avoid these drawbacks, Ramp Voltage Stress (RVS) was proposed in [40] to study the switching times of resistive memories. The procedure consists in increasing voltage gradually, until switching occurs, using a ramp rate defined as a constant step over a constant time step (See Figure 3.13 inset). Some models were developed to convert time and switching voltages extracted from RVS characterizations into data measured with CVS [42, 50]. Because of these reasons and given its tremendous applicability in the scope of this work, it was decided to study switching values as a function of the applied stresses (i.e. number of SET/RESET cycles) through RVS measurements. They allow the extraction of the voltage value at which the switch occurs as in an IV characteristic. An example of this, is reported in Figure 3.13, where median values for both HRS and V_{switch} are depicted. It can be appreciated how the SET (V_{switch}), degrades

with cycling after 10^5 cycles. For the reported case, a reduction of 0.4V over one decade ($10^5 - 10^6$ cycles) is observed. More importantly, the decrease begins with the decrease of the HRS, which is expected to be proportional to the gap size between the remaining conductive filament and the bottom electrode after RESET. A notable reduction is appreciated one decade before the hard breakdown occurs.

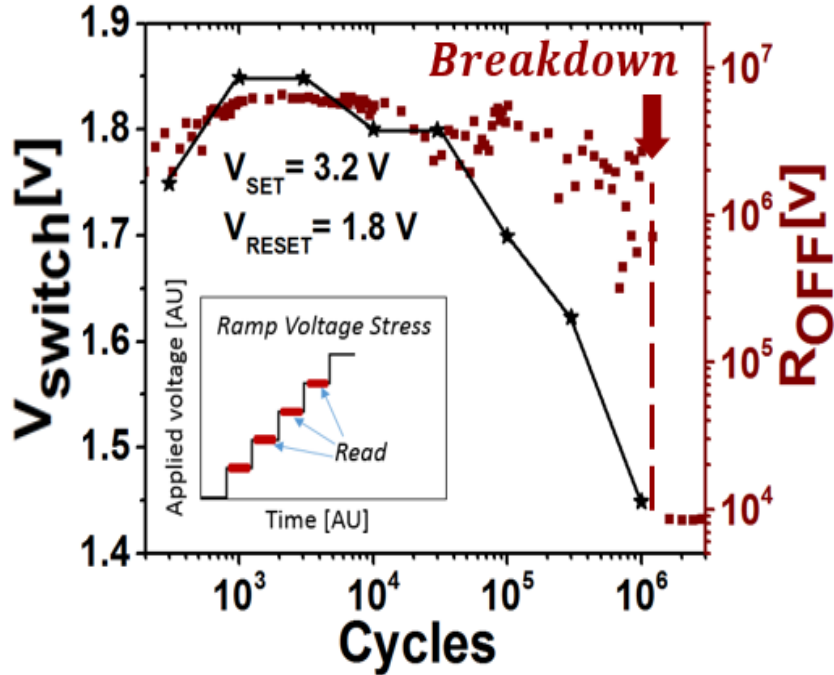
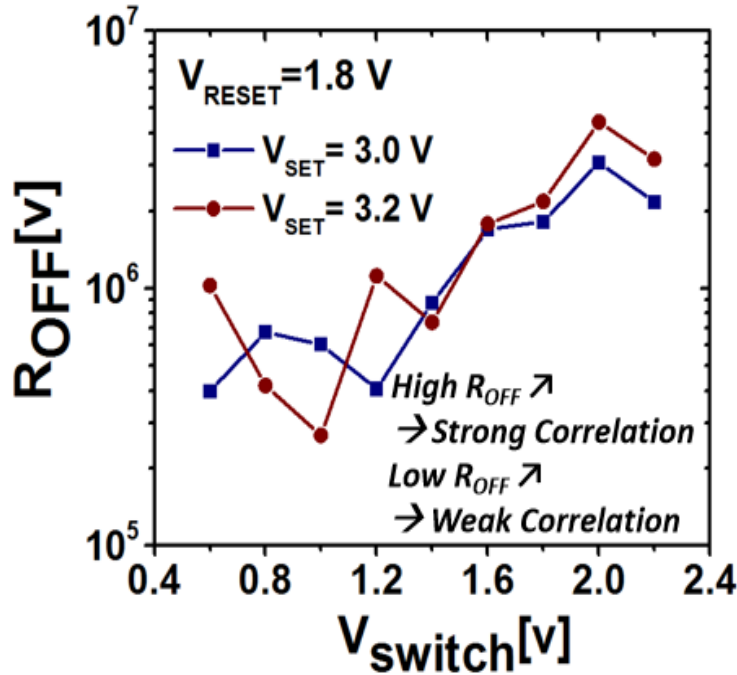


Figure 3.13: Median values of the switching voltage and R_{off} evolution during endurance using a RVS method to extract the V_{switch} for a CBRAM stack. Gradual degradation in the dielectric is showed. It means that generation of the filament is easier with cycling.

The latter observation shows the usefulness of RVS measurements in order to predict and to monitor devices degradation with cycling. Filament generation seems easier, since less energy is required, at some point. In order to establish a better insight concerning the correlation between the HRS value and V_{switch} , they were compared as presented in Figure 3.14. At a high R_{off} , R_{off} and V_{switch} are clearly correlated, whereas at low R_{off} , a mismatch appears. This is explained by the delay between V_{switch} and R_{off} as the dielectric begins to degrade.

3.4 Numerical Model

A stochastic endurance model is presented in this section, based on the experimental results from previous sections as well as those ones previously treated in literature. Although conductive path composition for OxRAM and CBRAM is not the same and implies different physical mechanisms and behaviors, the observed experimental tendencies have been validated over both ReRAM types, as it was the case with the log-normal distribution for

Figure 3.14: Correlation between R_{off} and V_{switch} .

N_{cmax} in subsection 3.3.1. Therefore, it was decided to model reliability behavior from a phenomenological point of view.

In order to gain insight on the microscopic nature of the mechanisms at stake, the strong variability of the ReRAM endurance, suggested the use of a Monte Carlo like approach. Such method, was previously validated for the switching variability to estimate HRS and LRS dispersions in [31] and is used in the same way in this work to study N_{cmax} dispersions. Moreover, *ab initio* simulations [51], led to demonstrate that complex movements of oxygen inside HfO_x lattices, can lead to the induction of different levels inside the gap, with some of them featuring large bounding energies. This could indicate that failure is a product of non-switchable states that appear inside the conductive filaments and are induced by cycling. These states present a low-probability due to the high energies required for their generation. Therefore, they can not be removed anymore, once they are created. In the case of OxRAM memories, such defects are oxygen vacancies, while for CBRAM, non-switchable states are related to metallic impurities. It means that two conductive filaments could exist inside the active layer: one consisting of switchable states, and another one of non-switchable states. Interested by the latter, only the stochastic characteristic of it and its evolution with cycling, are treated here. To do so, a constriction zone is discretized in elementary bins, corresponding to the gap between the residual filament (which is assumed to be never erased during cycling) and the bottom electrode, as shown in the schematic presented in Figure 3.15. For each SET/RESET cycle, metallic ions or oxygen vacancies for CBRAM and OxRAM, respectively, can fill or be removed from such constriction zone. With every cycle, every discretized bin, has a specific probability (usually low, which allows a higher number of cycles to reach failure),

to convert into a deep state. If the deep or non-switchable states form a percolation path, the device is assumed to have reached the hard breakdown and its N_{cmax} is extracted. Thanks to the use of diverse probabilistic laws for bins switch into deep states, N_{cmax} dispersions can be extracted and deduced from these many runs, in order to compare these simulations with the prior experimental results.

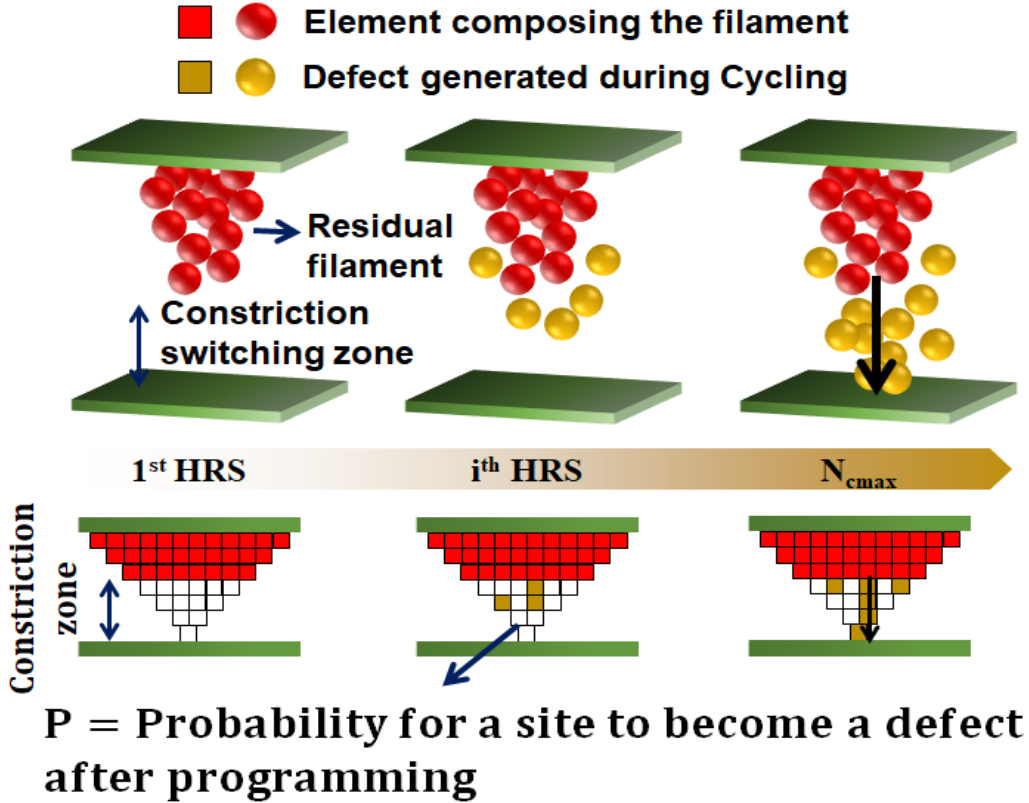


Figure 3.15: Schematics of the stochastic model developed in this section. With cycles, defects inside the gap between the bottom electrode and the residual filament, can be generated or not, through the use of a probabilistic law and volume discretization. Hence, N_{cmax} dispersions can be extracted and compared with experimental results.

Thanks to the great simplicity of this model, many degrees of freedom can be explored: geometry of the constriction, probabilistic law governing the commutation and the parameters determining such laws, as it will be observed in the next sections.

3.4.1 Geometrical considerations: constriction size and shape

Bernoulli trials were used to study the constriction zone geometry. To quicken these exploratory considerations, relatively high constant probability ($p \simeq 10^{-4}$) was chosen. For the first results presented in this subsection, N_{cmax} dispersions do not correspond to fits over experimental results.

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Historically, effective observation of the conductive filament, has been one of the biggest challenges for oxides studies [52, 53]. Consequently, comparisons between cylindrical and pyramidal shape for the constriction zone using the stochastic model, were undertaken. N_{cmax} distributions for the constant probability previously mentioned for both filament shapes are presented in Figure 3.16(a). In the case of pyramidal shapes, consistency with simulation results [54] and 3D Conductive-AFM tomographies [55], is observed. A larger variability is appreciated, more in agreement with the experimental results and tending to confirm the pyramidal characteristic of conductive filaments inside resistive memories.

For the next stage, diverse pyramidal shapes for the constriction zone were explored. Results are reported in Figure 3.16(b). It can be observed how the number of contacting bins at the bottom electrode totally change the slope of the N_{cmax} dispersions. Fewer sites at the lower part of the constriction zone, lead to higher variability. On the other hand, it is concluded that the various pyramidal shapes tested have little impact on failure distributions.

A final test for this geometric and shape considerations consisted in studying the influence of the constriction height (Figure 3.16(c)). Smaller gap sizes lead to more distributed N_{cmax} behaviors. Similar behaviors were observed in the study of dielectrics breakdown, where thin oxides present a lower slope in the Weibull distributions [26, 56]. These results show that the sites responsible for the hard breakdown in resistive memories tend to be localized and could be the explanation of observed high variability in the maximum number of cycle distributions. If the constriction size is associated with the HRS values, results obtained in Figure 3.16(c) also confirm the tendency observed in Figure 3.12, where optimized programming conditions over a CBRAM technology, led to higher and less dispersed WM and N_{cmax} , as it is the case here.

3.4.2 Probability law considerations

With important conclusions about the filament geometry, next step consisted on the study of the probability laws defining the switching of the discretized bins into non-switchable states. To do so, some models available in literature were used as inspiration, for instance, [26, 57]. In them, defects are considered to nucleate and grow, i.e. once a site becomes a non-switchable state, sites around tend to become deeper states too. To emulate this phenomenon, it was decided to include an accelerator factor to our model, additionally to the Bernoulli trials used for the previous tests. This hard breakdown acceleration factor (α) increases the switching probability (p) for the bins surrounding a switching bin. It can be justified by the fact that non-switchable states inside the mesh, can increase the local electrical field around them.

Figure 3.17(a) illustrates how in the case of a constant probability, the median value of N_{cmax} distributions are shifted without affecting dispersions slopes. On the contrary Figure 3.17(b) presents comparisons of the impact of probability laws, using either Bernoulli trials without increased switching probability for the surrounding sites, or including the acceleration factor. Once again, high probability values, in order to have faster results,

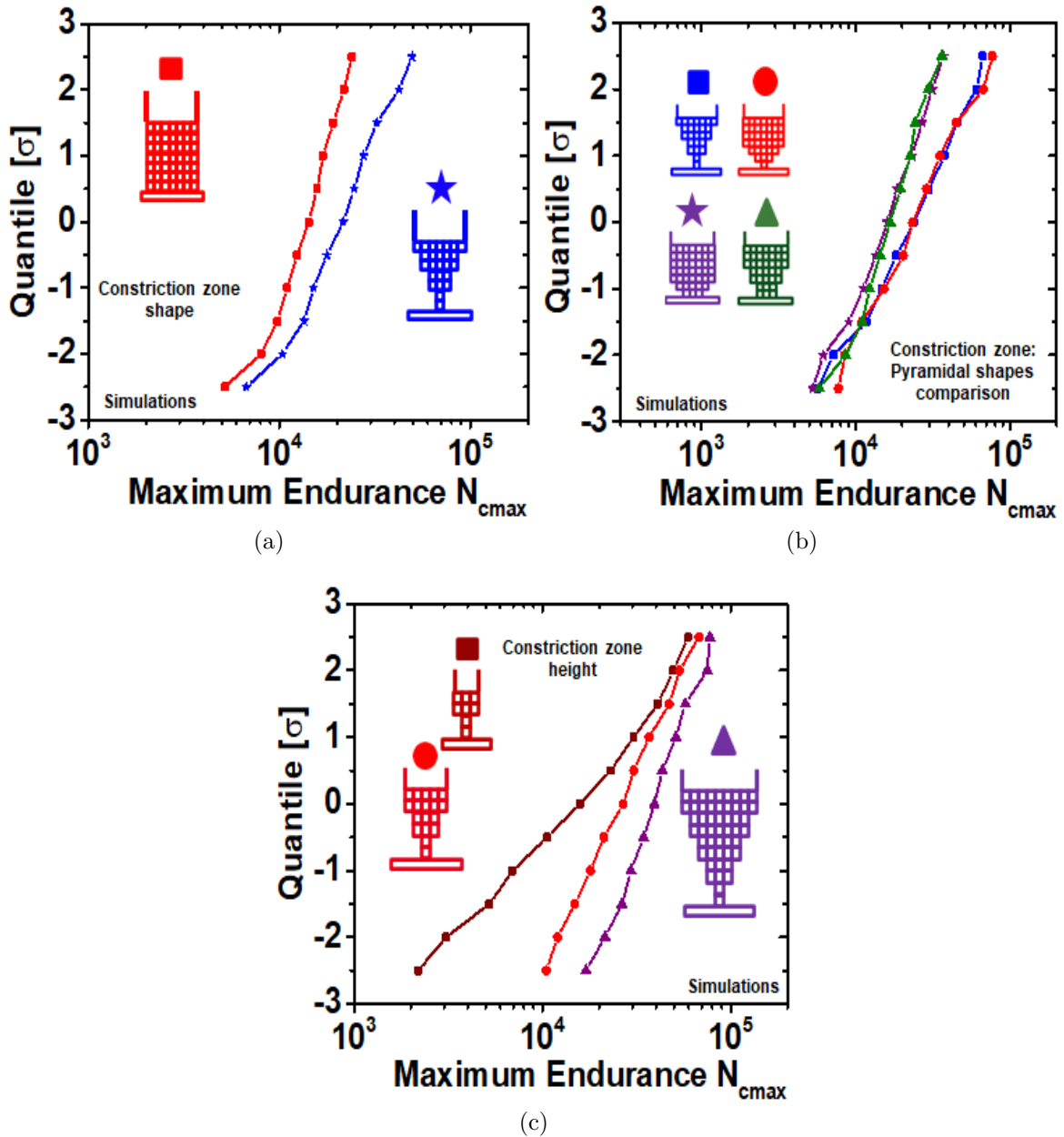


Figure 3.16: (a). Comparison between a pyramidal and a cylindrical shape for the constriction zone. Pyramidal shape presents a higher dispersion being more in agreement with experimental results. (b). Various pyramidal shapes simulations. When a small number of contact points between the Bottom Electrode and the constriction zone are used, higher dispersions are observed. Slope of the used pyramidal shape does not show an important influence on variability. (c). Constriction zone height comparison. Small ones are more likely to present higher variabilities, possibly indicating that states responsible of failure in ReRAM are highly localized.

were studied. It can be observed how N_{cmax} is dispersed over three decades for the biggest

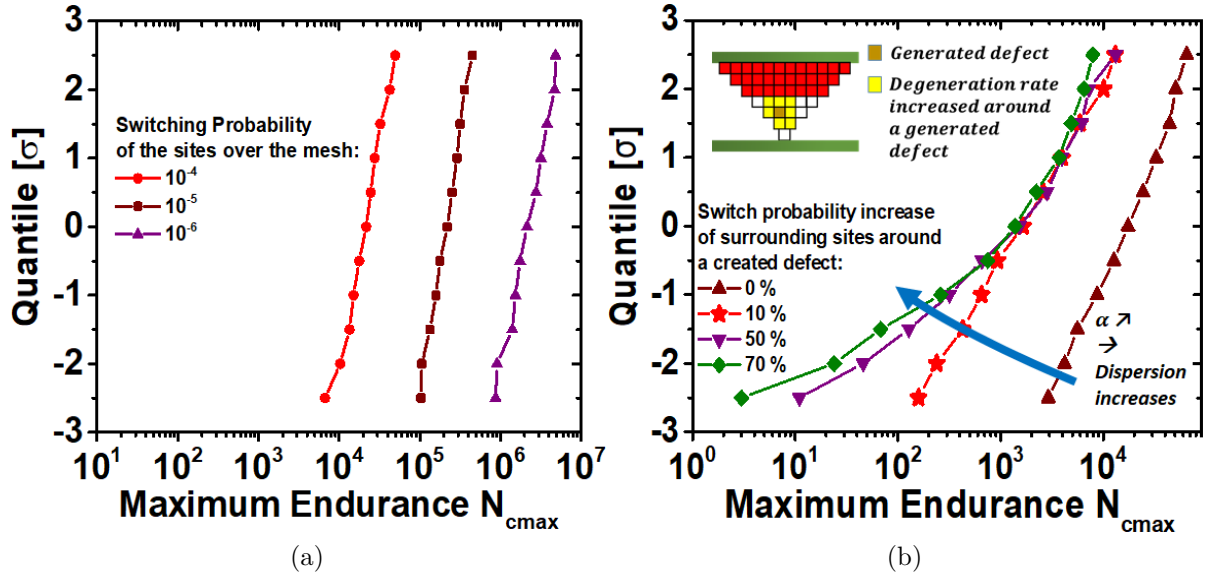


Figure 3.17: (a) Influence of switching probability at a constant value over maximum endurance distributions. (b) Influence of degeneration rate (α) which modifies switching probability of sites ($p = 1/P_{ithCycle} = 1/(P_{ithCycle-1} * \alpha)$) around a site that has switched over maximum endurance distributions.

hard breakdown accelerator as well as the median values are shifted. These results are comparable in terms of dispersion, to those obtained in the experimental section. Hence, an additional conclusion regarding the filament morphology and its evolution is extracted: defects are not generated in a totally random position, but tend to appear around previously generated non-switchable states.

3.4.3 Fitting of experimental results

Using the conclusions obtained in the previous sections regarding shape, size and probability law, fits of the experimental data are presented in this section. It was observed how under the programming conditions used for this work, where compliance current is only used in the case of the SET process, RESET has a bigger influence over N_{cmax} dispersions. Taking this into account, distributions from Figure 3.11(a), were fitted using constant degeneration rates. A distribution with a low dispersion and another more with a higher one were selected, i.e. extreme cases. However, such constant degeneration rate was not enough to fit the experimental data, even after variation of all the freedom degrees studied before, the obtained slope was always bigger if compared with that one from the most extreme case. This first result induced us to study the probability laws and to mimic a nucleation and growth for the deep states responsible of the hard breakdown, as it was discussed in the previous section. Figure 3.18, reports the fits of maximum endurance distributions using the stochastic model after choosing the right size, geometry and acceleration factor α for the sites around those ones already switched; inside the constriction

zone. Excellent agreement between simulated and measured distributions was found, allowing to observe from a phenomenological point of view the possible characteristics of the conductive filament that define N_{cmax} dispersions.

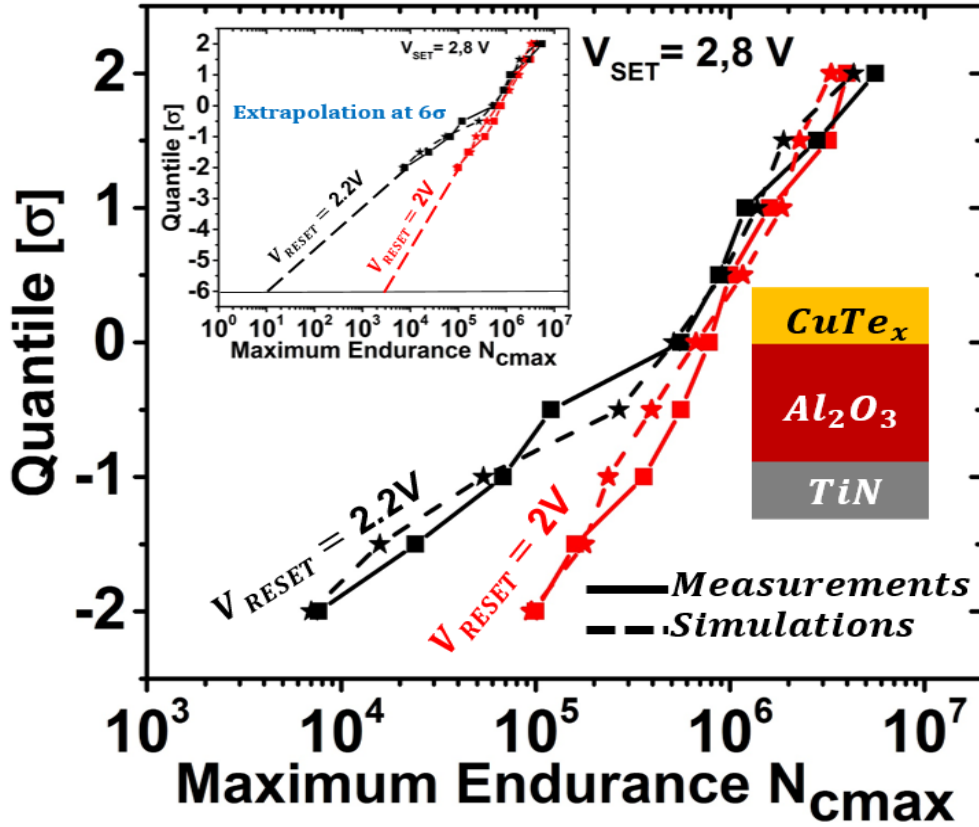


Figure 3.18: Experimental and simulated N_{cmax} distributions for $Al_2O_3/CuTe_x$ CBRAM for two different programming conditions.

Both simulated cases present two degradation factors. The biggest one corresponds to $V_{RESET} = 2.2V$. This implies that in the absence of a compliance current during the RESET process, it becomes critical and direct responsible for the clustering of non-switchable states during programming cycling. Those states cause the endurance failure and the stuck in the LRS state, corresponding to the device hard breakdown. Moreover, pyramidal shape and very localized states responsible of failure were confirmed for the constriction zone.

As stated before, 120 cells were used for every programming condition analysis. Even if larger populations were not tested, clear tendencies and important conclusions about the filament nature could be extracted. A simple extrapolation of the experimental and simulated results from Figure 3.18, allows to appreciate how an optimized voltage is a key parameter in terms of reliability of very dense arrays. For the simulated cases, extrapolation at 6σ gives barely 10 cycles for $V_{RESET} = 2.2V$, which is almost two decades lower compared to $V_{RESET} = 2V$ at 6σ (assuming an optimistic scenario where low density tails would not appear).

3.5 Conclusions and Perspectives

- Endurance reliability of resistive memories (ReRAM) was addressed at the array level allowing the introduction of the maximum number of cycles N_{cmax} . It corresponds to the hard breakdown of the oxide as a result of the programming cycling. *Its dispersions follow a log-normal law regardless the used stack.*
- Influence of the programming conditions on N_{cmax} dispersions was studied. 4kb arrays were used with a population of at least 120 cells with 10^7 SET/RESET cycles applied per programming condition tested. V_{SET} does not change the median behavior but can eventually generate some tails on the distributions. The relatively low impact of SET conditions is explained by the programming strategy chosen. During SET, current is controlled by the FEOL CMOS. On the other hand, and given that during RESET process, compliance current is not used, slight variations on V_{RESET} , degrade the N_{cmax} median value as well as the standard deviations. **Hence, RESET voltage optimization is of capital importance to improve ReRAM reliability.** Once again, same tendencies were observed for diverse stacks and both ReRAM types (OxRAM and CBRAM).
- Gradual degradation phenomenon observed on switching voltages, extracted using Ramp Voltage Stresses during cycling, **could be a failure predictor.** Moreover, some clues about the degradation mechanism can be inferred since decreasing switching values with stress could be related to lowered activation energies inside the oxide. However, much more data is needed (different thicknesses, stacks, electrodes, etc) in order to have more robust conclusions regarding these kind of experiments.
- Fits of maximum endurance distributions were obtained for the first time using a simple stochastic model. Based on deep states theory, which are responsible for the device breakdown, **large dispersions were linked to constriction zone parameters, which include constriction size, pyramidal shape and localized number of potential defect sites.** Concerning the defects, **cluster configuration was found more adequate to fit experimental results**, if compared to a merely random generation. The sum of these results hence confirm that the statistical analysis of ReRAM endurance is a key parameter in order to improve the technology towards its industrial scale production.

Results found through the stochastic modeling could be used as a basis for future models based on more physical concepts such like defects dimensions, conduction mechanisms, and electronic characteristics of the analyzed oxides.

- In this study, devices were cycled individually for every SET/RESET condition tested. Once they broke, N_{cmax} was extracted. It implied long measurement times. However, some alternatives to have faster results worth to be mentioned. Among them, temperature increase during cycling has been demonstrated to accelerate degradation [58]. Analogically to retention measurements, N_{cmax} values obtained at specific temperatures could be extrapolated at different ones through empirical

observations. A second strategy to reduce testing times could consist in simultaneously cycling and reading the whole population. Once the first devices begin to fail, one could say that cycle number at which first failures occur, correspond to the tails of the $N_{cm_{ax}}$ distribution. Evidently, large populations should be tested to get lower quantiles. They could also allow slope extraction as a function of the programming conditions applied. To do this, certainty on the tails following the main population tendencies should exist, which is not always the case for very large populations.

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Chapter 3: ReRAM Reliability Studies

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Integration of OTS based back-end selector with HfO₂ OxRAM for crosspoint arrays

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RESISTIVE Random Access Memories (ReRAM) are one of the most promising candidates for Storage Class Memory (SCM) applications. Among their advantages, compatibility with the back-end of line (BEOL), good scalability, high speed, and low power consumption can be mentioned. As for the disadvantages, high variability and low ratio between the ON and the OFF states (also known as Window Margin (WM)), which implies sneak paths appearance for 3D crosspoint architectures, are the most relevant ones. In the previous chapter, some guidelines, analysis and modeling, were provided aiming to improve and to understand ReRAM's variability. On the other hand, and in order to solve the ON/OFF ratio inconvenient, non-linearity (NL) needs to be added. Mainly two solutions for this NL issue have been traditionally proposed: a first one consists in adding it as a requirement of the memory itself. However, it leads to more complex stacks or process fabrication as well as power consumption increase (see subsection 1.6.4). Besides, increasing WM of resistive memories, usually implies degradation of other performances such as endurance or retention [1]. A second solution consists in adding NL through an external access device, also called selector (1S). This is connected in series with the memory point. Hence, memory and selector can be optimized and designed separately, and then co-integrated. Even if using this approach gives to designers and devices makers some degrees of freedom, finding electrically and process compatible memories and selector devices, without compromising performances or arrays scaling, can be a complex task too. A detailed introduction to selector devices topologies as well as to self-selected memories, can be found in section 1.6 of this work.

In order to be good candidates for co-integration with electronic memories and posterior implementation of crosspoint arrays, selector devices must fill a series of requirements. The most important ones are listed below (idem as before, a detailed explanation of these requirements is provided in section 1.6 too):

- High ON-state current density
- Low OFF-state leakage current
- Process compatibility with the ReRAM device
- Symmetric IV curve (bipolar ReRAM)
- Electrical compatibility with the memory device
- Ideally two-terminal device
- Improved performances in comparison with those ones of the resistive memory. Ideally endurance, retention, switching speed and variability.

Among the diverse selectors proposed in literature, one of the most interesting solutions are the Ovonic Threshold Switching (OTS) devices. They fulfill most of the requirements listed above. Fabricated using amorphous chalcogenide materials, they present high selectivity (ON/OFF ratio) based on two levels of conductivity: a low-conductive state (OFF-state) and a metastable high current density state (ON-state). Going from the ON

to the OFF state and vice-versa are repeatable and nondestructive phenomena, even if high electric fields are seen by devices on the ON state [2].

While ReRAM reliability was previously studied, this chapter describes the co-integration of a Ge-Sb-Se-N (GSSN) back-end selector with a HfO₂/Ti resistive memory in a 1S1R configuration. Firstly, a detailed explanation of the working mechanism and the main characteristics of OTS devices are provided. Then, GSSN composition is tuned and optimized in order to make it compatible with ReRAM electrical characteristics. This leads to the combination of low leakage current as well as low operating voltages that avoid ReRAM degradation. Afterwards, electrical characterization of 1S1R devices is performed hence quantifying 1S1R performances. More than 2 decades of difference between the ON and OFF states of the ReRAM memory were measured with low leakage currents ($\approx 1\text{nA}$) for a V/3 biasing strategy. Stability with temperature and in pulsed mode of electrical characteristics are also demonstrated. Finally, and based on the electrical performances obtained, maximum array size was calculated. Up to 1Gb sizes were estimated for the most optimistic scenarios, while 1Mb bank sizes could be obtained for the most aggressive technological nodes down to 10 nm.

4.1 OTS: general considerations and working principle

Since the first studies lead by Stanford Ovshinsky in the late 1960's [3], chalcogenide materials have found plenty of interesting data storage applications. The main ones are the optical (DVD and blu-ray technologies), non-volatile (PCM), and volatile memories (OTS devices) [4]. All of them, take advantage of the high resistivity difference and transitions between two conductive states. Additionally, these phenomena are fast and reversible. Most of the alloys used for the wide range of applications are composed by one or more chalcogen elements, such as Se and/or Te, and glass formers like Ge, As or Si. Dopants such as C and N can be added in order to improve specific electrical performances as a function of the developed application [5]. PCM or OTS behaviors are obtained depending on the alloy stoichiometries or the intensity of the electric fields applied to the devices [6]. For instance, Si% in GeTe composites is responsible for volatile or non-volatile characteristics [7]. For the OTS case, the two conductive states are specific to the amorphous phase and do not involve phase transitions that could lead to crystallization as it is the case of the *memory switching* event, inherent to PCM memories [8]. In fact, metastable bond alignment seems to be responsible for the high conductive state under electrical stimulus for the OTS devices. These metastable crystalline phases retain some similarities to the amorphous structures they were created from [8]. An interpretation to this, leads to suppose that the conductivity change, taking place in chalcogenide materials once the threshold switching occurs, is possible thanks to slight structural changes [9] as it will be explained later.

As it is the case for ReRAM, the thin film of chalcogenide alloy responsible for the OTS behavior is sandwiched between two conductive electrodes. Figure 4.1 presents a

typical IV curve for a selector. There, the main electrical parameters to be taken into account are presented. OTS devices require an initialization process called “forming” or “firing” ($V_{Forming}$), necessary to switch the device from the pristine state into the ON state. For the subsequent operations, the required voltage to reach the volatile switching from the OFF towards the ON state is called the threshold voltage (V_{th}). V_{th} is lower than $V_{Forming}$ ($\approx 30\%$ in some cases [10]). The selector switches back to the OFF state once the voltage or the current are decreased below hold current and voltage (I_{hold} and V_{hold} respectively). I_{leak} is used to quantify the selectivity and the non-linearity of the selector device. In the presented example, I_{leak} is taken at $V_{th}/3$. Interpreting I_{leak} and therefore selector selectivity, requires somehow some attention, given that this metric is dependent on the memory technology as well as the polarization strategy used to operate the crosspoint array. Additionally, not all the authors use the same conventions to determine it. Furthermore, all the presented metrics are symmetric in terms of absolute values if the voltage polarity is changed. It represents a great advantage in terms of compatibility between OTS selectors and bipolar ReRAM memories.

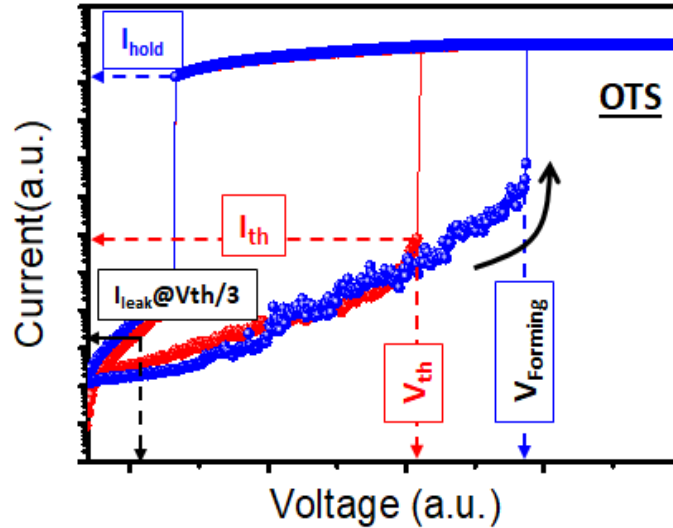


Figure 4.1: Typical current voltage characteristics for an OTS selector. Main electric metrics are indicated. Adapted from: [10]

4.1.1 Physical working mechanism of OTS selectors

Threshold switching is a fundamental aspect of OTS devices. Its complete understanding could lead to performances and reliability improvements. However, the physical mechanism behind it, has not been clarified yet, making of it a large subject of debate nowadays. Various explanations have been proposed. Since a general point of view, these approaches can be divided into two subtypes: a first one consists in a purely electronic mechanism, where carrier hopping and tunneling into higher energy trap states that once filled lead to the current increase; are responsible for the threshold switching [11, 12]. In a second one, a thermally assisted mechanism [13] leads to a local structural change causing the

formation of a metastable crystalline filament [14, 15]. Once such filament links the two electrodes of the OTS, switching appears and the device becomes highly conductive. This last approach presents switching as a structural change, whereas an electronic approach only succeeds in explaining the conduction models in each regime of the switch. Various aspects and considerations, lead us to use the crystalline filament mechanism in order to understand and to study variability of the threshold voltage V_{th} for OTS+OxRAM systems, as presented in section subsection 5.5.2 of this work.

A very complete model for the OTS effect was recently proposed by Noé *et al.* [9, 16]. Through electrical, optical, and x-ray absorption experiments, as well as *ab initio* molecular dynamics (AIMD) simulations, threshold switching is attributed to a localized change in the bonding configuration inside the chalcogenide film using metavalent bonding (MVB) [17]. Under electric-field excitation, this MVB produces de-localized or excited states. Such states present larger bond lengths, which means they become close together making tunneling easier, hence increasing carriers mobility inside the amorphous lattice [9].

Evolution of the chalcogenide structure for a GeSe alloy before⁽¹⁾ and after excitation using atomistic *ab initio* simulations is depicted in Figure 4.2 [9]. Through forced occupation of the excited electronic states to simulate the effect of the applied electric field, changes over the electronic Density of States (DoS) (Figure 4.2.a and Figure 4.2.b) and the amorphous structure itself (Figure 4.2.c and Figure 4.2.d) are appreciated [9]. For the DoS simulations, it can be observed that upon electric field excitation, the states around the fermi level E_f (very close to the valence band on chalcogenide materials), delocalize, hence surrounding such energetic level as presented in Figure 4.2.c. Through further tests, Noe *et al.* observed that the delocalization was produced along the planar motifs Ge-Se and Se-Se. Thanks to Born Effective Charges measurements, which allow to determine the responsiveness of a lattice to distortions, i.e. the chemical bond polarisability [17]; it was determined that the Ge-Se and the Se-Se bonds, tend to align. This phenomenon leads to the introduction of conductive channels around the fermi level of the material, facilitating electrons population of the conductive states.

The alignment approach was previously invoked in literature and called "resonant bonding" in order to explain phase transitions between the amorphous and the crystalline states of phase-change materials [18, 19]. The resonant bonding theory of materials, covers a wide variety of them, even beyond chalcogenide ones, such as benzene and graphene. However, Wuttig *et al.* [17], determined some differences between chalcogenide materials and the rest of the "resonant bonding" materials group. Besides, they present unique properties between covalent and metallic bonding. These observations led this group to propose "metavalent bonding" in order to replace the "resonant bonding" term, as a distinctive characteristic of chalcogenide solids. In the case of OTS devices, the main difference with the metavalent bonding of the phase-change alloys is claimed to be the metastability of the delocalized states [9, 16] that recover their strong localization once $V_{applied} < V_{hold}$.

⁽¹⁾For the MVB model, initial/before electrical excitation makes reference to devices in the pristine state.

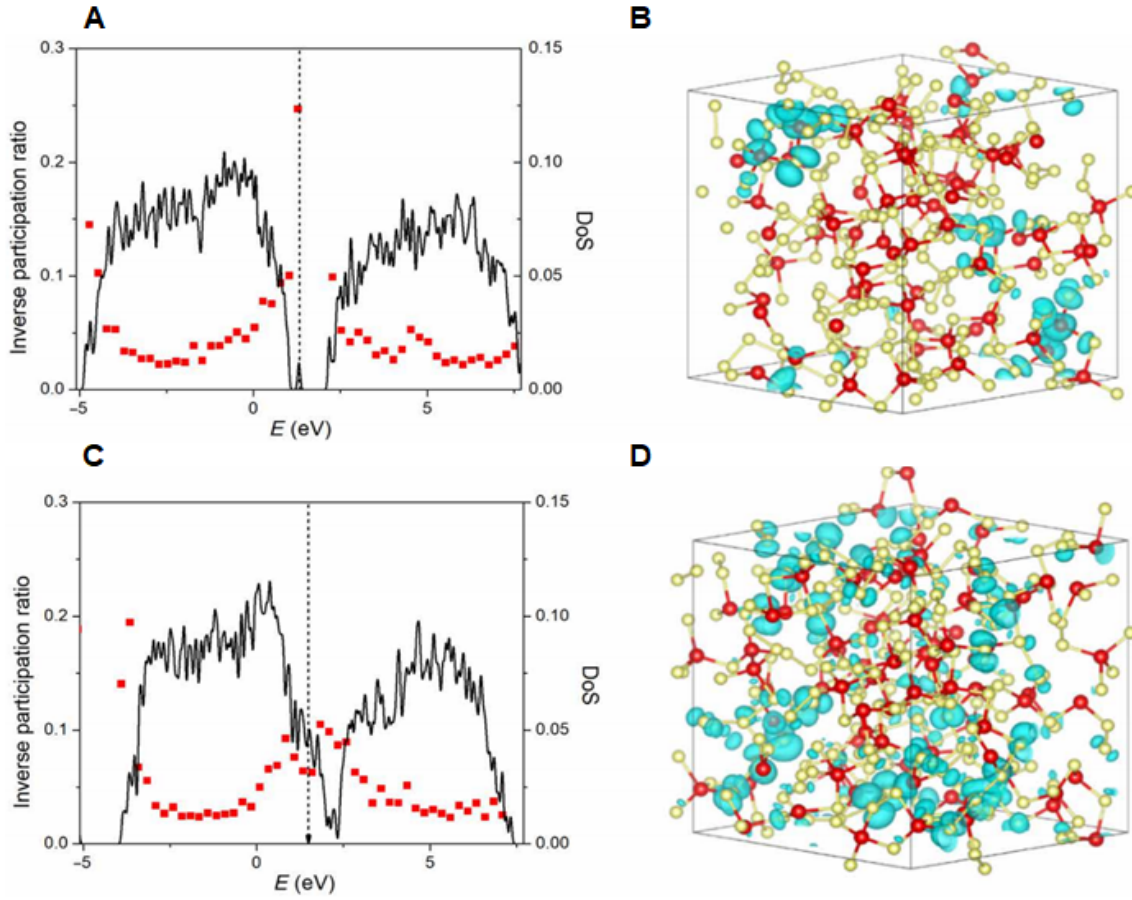


Figure 4.2: Simulations over 240 atoms and atomic composition $Ge_{72}Se_{168}$ at 300 K, allow to appreciate the evolution of the chalcogenide material before (A and B) and during electrical excitation (C and D). Electronic Density of states (DOS) (A and C), shows how the electric field produces delocalization of states around the fermi level of the material (dashed vertical lines). Hence, electrons population of the conductive states appears, allowing the threshold switch. Inverse participation ratio IPR (red squares in A and C), illustrates the large bandgap during the initial state and how upon electrical excitation its values drop. The amorphous structures (B and D), depict delocalizations using blue isosurface curves. Taken from: [9]

General agreement exists about the same nature behind switching events. It means that V_{Foming} and V_{th} are justified by the same physical mechanism [20]. In the case of the MVB model [9], it was demonstrated, thanks to Pair Distribution Functions (PDF), the existence of some structural differences between pristine state devices and formed ones for the OFF-states, as depicted in Figure 4.3. There, PDF for both GeSe and GeSeSbN using 240 atoms and atomic configurations $Ge_{72}Se_{168}$ (as in Figure 4.2) and $Ge_{55}Se_{127}Sb_{46}N_{12}$ are presented for amorphous structures, before, during and after electric stimulus. It can be observed how the pristine devices present bimodal distributions with main contributions around 2.41 and 2.57 Å, while excited and post-electrical excitation devices present unimodal characteristic with merge at 2.41Å. It is translated into lower

local energy barriers for the formed/recovered devices as well as some kind of structural relaxation towards a less amorphous structure [9, 16]. This explains lower V_{th} and higher I_{leak} values for formed devices as it will be presented through measurements in further sections of this chapter.

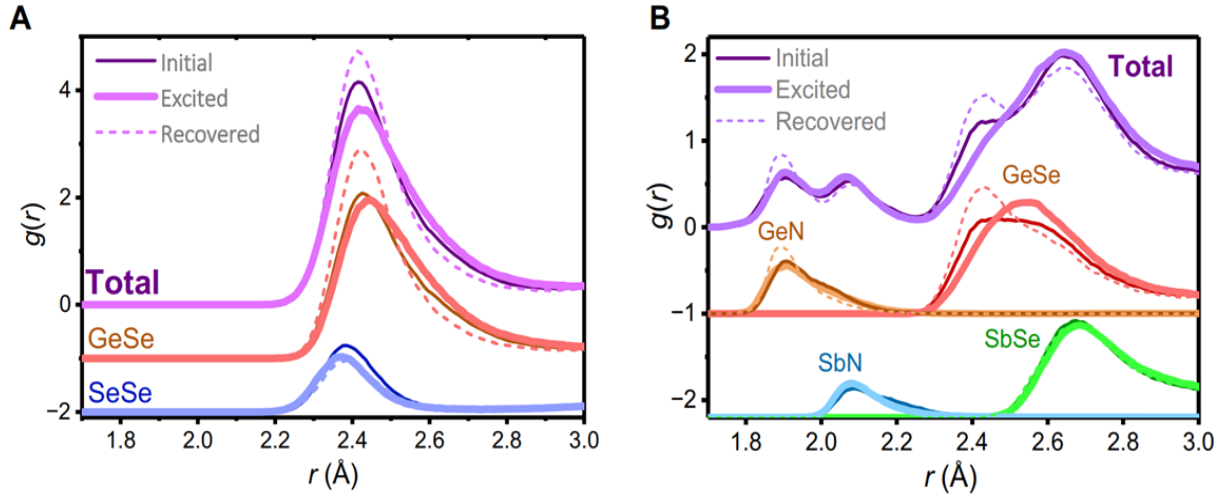


Figure 4.3: Pair Distribution Functions (PDF) for both $Ge_{72}Se_{168}$ and $Ge_{55}Se_{127}Sb_{46}N_{12}$ using 240 atoms before, during and after electrical excitation. Taken from: [9]

MVB models and experiments, with subtle differences if compared to Noe *et al.* propositions, have also been reported [21–23]. The latter, as well as the work developed by Chai *et al.* [24], present evidence to demonstrate that bonds delocalization, which reduces the bandgap allowing electrons to populate the conductive states, occurs in the form of a percolation or filamentary path. Their results mainly show that states delocalization happens along the transport direction. Additionally, V_{th} and ON/OFF currents for formed devices are demonstrated to be independent of the device size. On the contrary, pristine leakage currents present device size dependence. Similar results can be found in [25]. Moreover, experiments conducted in order to study t_{switch} behavior (the time to reach the ON state, once device current begins to dramatically increase), demonstrated Weibull distributions for such characteristic [24]. This could be linked to the Time-Dependent Dielectric Breakdown (TDDB) [26, 27], widely known in oxides, which present a filamentary characteristic.

The previous evidence would validate, the highly conductive filamentary characteristic of the threshold switching events for OTS devices [25]. The domain diameter is expected to be $\approx 3\text{nm}$ according to [28, 29]. As for the MVB approach [9], it does not exclude the metastable appearance of a crystalline filament for the high conductive state. It could be affirmed that, somehow, MVB model is an atomistic explanation to the phenomenological Metastable Nucleation Filament Model (MNFM). All these considerations were taken into account, at the moment of choosing the metastable crystalline filament approach, already mentioned, in order to study V_{th} variability for OTS+OxRAM (subsection 5.5.2) systems.

4.2 OTS devices for 3D crosspoint arrays

Without a doubt, Phase-Change Materials based memories, are the most mature and closest to market emerging technology for Storage Class Memory applications [30]. Naturally, the first 3D concept for an emerging memory and an OTS device, was proposed in 2003, using PCM memories [31]. Then, in 2009 the first PCM+OTS 3D crosspoint memory was presented [32], taking advantage of the fact that PCM and OTS are based on the same type of materials, which makes them highly compatible and easily co-integrated [33]. Because of this, a first commercial 3D crosspoint product using PCM+OTS as memory points was announced by the Intel-Micron partnership in 2015 [34]. 1000 times faster and 1000 times more endurance than NAND and 10 times denser than flash, this device is already an interesting player in the memory market. A GST material is used for the memory point and a As-doped Se-Ge-Si alloy is used for the selector device [35]. Hence, a storage capacity of 128 Gb is reached.

Even if the first 3D crosspoint implementation has been made using PCM memories, some notorious disadvantages for these technologies (already treated in chapter 1) exist: high power consumption, low power efficiency, higher working currents, and slower programming times, if compared to another emerging memory candidates; can be accounted [36]. Besides, the voltage drift characteristic of the amorphous phase, hinders implementation of neuromorphic applications based on such technologies [37]. The mentioned inconveniences as well as the prior mentioned Intel-Micron announcement, have re-boosted research in other emerging memory technologies too (ReRAM included). Under such scenario, the next challenge consists in finding the most adapted selector for co-integration with ReRAM devices. Among such access devices types, OTS devices are a very interesting candidate as treated in subsection 1.7.4. Table 4.1, presents and compares the main key metrics of some topologies found in literature. Some of them, will be studied in detail during this chapter. It can be appreciated how the GSSN OTS, constitutes an interesting alternative for 1S1R implementations. It is able to provide enough current density to program ReRAM technologies, endurance cycles and selectivity, in order to have high density arrays. Additionally, and as it will be demonstrated in further sections, V_{th} values are compatible with OxRAM electric characteristics. Maybe, the main disadvantage is the forming process, which seems to be quite high if compared with the V_{DD} of the most advanced nodes of CMOS technologies. On the contrary, such magnitudes could be eventually reached for most relaxed technologies. A first solution to overcome the high forming issue could be the use of larger transistors or amplification techniques such like cascade configurations. A priori, it should not be an issue given that only one transistor per row (or column) in the crossbar configuration is employed. With some area penalty, such circuits could be placed in the periphery under the array. However, further dimensions estimations and accurate analysis need to be performed for crossbar architectures using GSSN selectors. Moreover, and thanks to materials engineering, forming voltages can be diminished too (see section 4.3).

Chapter 4: Co-Integration of OTS+OxRAM memory for crosspoint arrays

Table 4.1: Key metrics comparison for various OTS technologies proposed in literature.
Adapted from: [38]

Metric \ Selector	Doped Chalcogenide	W/SiTe/W	NCS ⁽²⁾	BC ⁽³⁾ based OTS	AsGeSe	GeSe-AsTe	GeSeSbN (This work)
	[39]	[40]	[41]	[42]	[43]	[44]	[10, 45, 46]
J_{ON} [MA/cm ²]	1,6	10	≈ 16	10	7,9	>1	>1
Endurance	10 ⁹	10 ⁸	10 ⁷	10 ⁸	10 ¹²	10 ¹⁰	> 10 ⁹
$I_{leakage}(@V_{th}/2)$ [A]	10 ⁻¹¹	10 ⁻⁹	10 ⁻¹¹	10 ⁻⁹	10 ⁻⁹	10 ⁻¹⁰ – 10 ⁻⁸	10 ⁻¹¹
V_{th} [V]	1,6	≈ 1,2	1	≈ 3,5	2,7	1,5-4	≈ 2,2-3,2
$V_{Forming}$ [V]	N/A	1,7	N/A	N/A	4-5	3-6	4-8,5
V_{hold} [V]	0,4-0,7	≈ V_{th}	≈ V_{th}	≈ V_{th}	1,4	N/A	≈ 1-2
Selectivity	10 ⁷	10 ⁵	10 ⁷	10 ⁴ – 10 ⁵	10 ⁵	10 ⁴ – 10 ⁶	10 ⁵ – 10 ⁷

During the last years, research has been mainly centered in OTS devices, but 1S1R co-integrations have barely been explored. Not a lot of OTS+ReRAM works can be found in literature. Besides, and as a consequence of the maturity level of PCM technologies, most of the OTS materials have been designed in order to be co-integrated with such devices. An example of successful OTS+ReRAM co-integration was presented by Sony some years ago [42]. OTS reported performances are summarized in Table 4.1 (BC based OTS) and a schematic view of the co-integration is depicted in Figure 4.4. It consists in a traditional crosspoint implementation, with two decks and electrical performances claimed to operate 16 Gb density chips [47]. The selector device is a BC (Boron and Carbon) doped OTS and the ReRAM is a CBRAM which uses $CuTe_x$ as active layer.

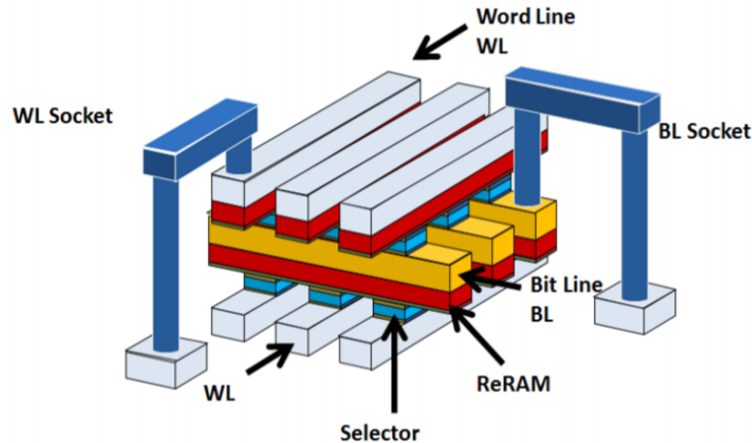


Figure 4.4: Schematic view of the OTS+CBRAM crosspoint array presented by Yasuda *et al.* Taken from: [42]

As already stated, for the time being, few 1S1R co-integrations actually exist in literature. It also implies that, regarding the technological processes, stoichiometries and materials used, even less details have been disclosed. For the moment, self-aligned approaches are used, aiming to reduce the lithographic steps in order to increase cost effectiveness of 3D crosspoint architectures. Through via patterning, 1S1R devices are connected to the

⁽²⁾New Chalcogenide Selector (the material is not disclosed)

⁽³⁾Boron Carbon (The chalcogenide material is not disclosed)

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periphery circuits in the Front End of Line (FEOL) in charge of the memory array control. To allow optimization of electrical performances, electrodes are used to separate the memory and the selector element. Precisely, this was the technique used in a recent work presented by Kim *et al.* [41] for a PCM+OTS system and which is used as co-integration example in this section. Some of the key metrics of the presented system are reported in Table 4.1(NCS). As for the main integration steps, they are depicted in Figure 4.5. In general lines, they could be expected to be used for OTS+OxRAM crosspoint systems too. The authors highlight chalcogenide materials vulnerability to conventional etching and cleaning processes for cross-point patterning in the case of restrictive CMOS nodes (<40 nm). Moreover, reducing the feature size (F), implies thinner metal lines, leading to resistivity increase and higher voltage drops over the Cu lines, hence limiting operating aspects of the arrays for the most aggressive nodes (<10 nm) [33, 48]. In that case, vias strapping to larger metal lines and smaller arrays could be used in order to keep reliability, not without impacting scalability and therefore, increasing fabrication costs per bit.

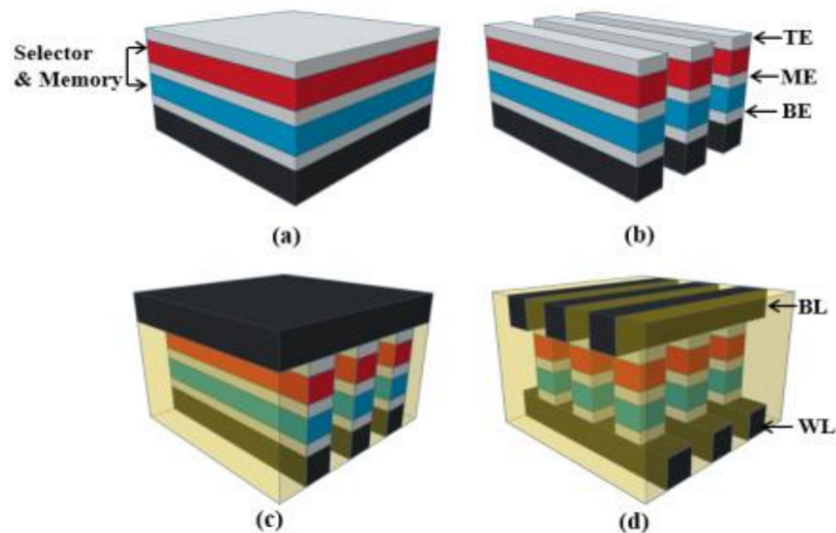


Figure 4.5: Main integration steps of a 1S1R based crosspoint architecture: (a). Blanket film deposition is made using PVD or CVD (ALD). Middle layers for WL and BL are used as well as for the electrodes surrounding either the memory or the selector device. A first patterning (b) is used in order to connect to the WL, followed by (c) a dielectric fill in and passivation using inter-layer dielectric (ILD) deposition and Chemical Mechanical Polishing (CMP). A second patterning (d), is applied in order to connect memory points to the BL. Process can be repeated for every layer of the crosspoint array and is a general approach for various emerging memory technologies. Taken from: [41]

In the context of our research group, a first $GeSe+HfO_2$ co-integration was previously studied [49]. However, high $I_{leakage}$ as well as high switching voltages were obtained, hindering its applicability for high density crosspoint arrays. Optimization process of the GeSe selector using Sb and N as dopants in order to improve OTS performances is tackled next.

4.3 OTS optimization

As mentioned in a precedent section, OTS alloys are composed by one or more chalcogen elements, such as Se and/or Te, and glass formers. Among them, Ge, Si and As can be cited as examples [5]. The latter can be used to improve metastability of the glasses against crystallization, as well as improving endurance, and reducing switching voltages [43, 44]. The main issue with this material is its toxicity, and avoiding its use is highly recommended [50], specially for applications such like biomedical ones [51]. Consequently, additional efforts aiming to obtain As-free and performing OTS devices, are necessary.

Se-rich Ge-Se based selectors can be an interesting alternative in order to overcome the As issue. They present a very low leakage current, nevertheless, their high V_{th} and low endurance behavior [52], need to be optimized. This was obtained thanks to material engineering [5, 10, 45, 53], by the CEA-Leti, adding Sb and N as dopants to the GeSe alloy. A first insight on the consequences and improvements brought by such dopants, can be observed in the quasi-static mode IV characteristic, presented in Figure 4.6. There, GeSe (GS), GeSe with 8% doping of N (GSN), $Ge_{24}Se_{56}Sb_{20}$ (GSS), and GeSeSb with 8% doping of N (GSSN); are compared [9]. As a first conclusion, GSSN presents a good compromise between V_{th} and $I_{leakage}$. It can be also observed, how they seem to be correlated (higher threshold values imply lower leakage currents). Such correlation was explored in a recent work [54], aiming to define guidelines for 3D crosspoint implementations.

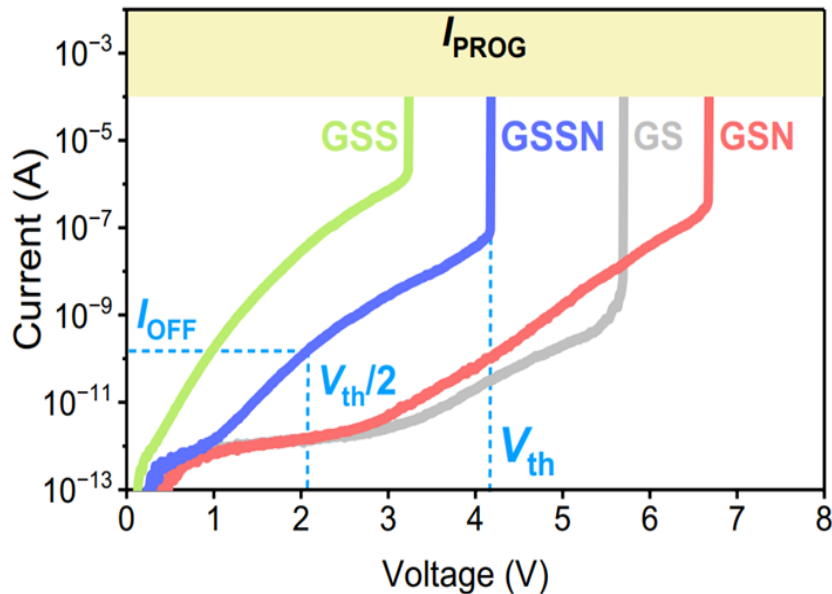


Figure 4.6: IV curve obtained for various GeSe OTS based films. The presented alloys are: GeSe, GeSeSb, GeSeN and GeSeSbN. Switching events are appreciated for every alloy and dopants effects over the basic composition GeSe are also observed. Taken from: [9]

At this point, it is important to mention the time dependence nature of the OTS threshold switching [3, 10, 55, 56]. It implies that different stress times, will generate

different values for V_{th} . Consequently, a shift between the threshold voltages obtained through DC (quasi-static) and AC (pulsed) modes is observed ($\sim +1V$). For a detailed explanation of the differences between these two measurements and the used set-ups for everyone of them, please refer to chapter 2 of this work.

With these aspects being taken into account, in the following sections, doping and thickness considerations of GSSN devices can be discussed.

4.3.1 Se-rich Ge-Se based OTS devices: doping effects

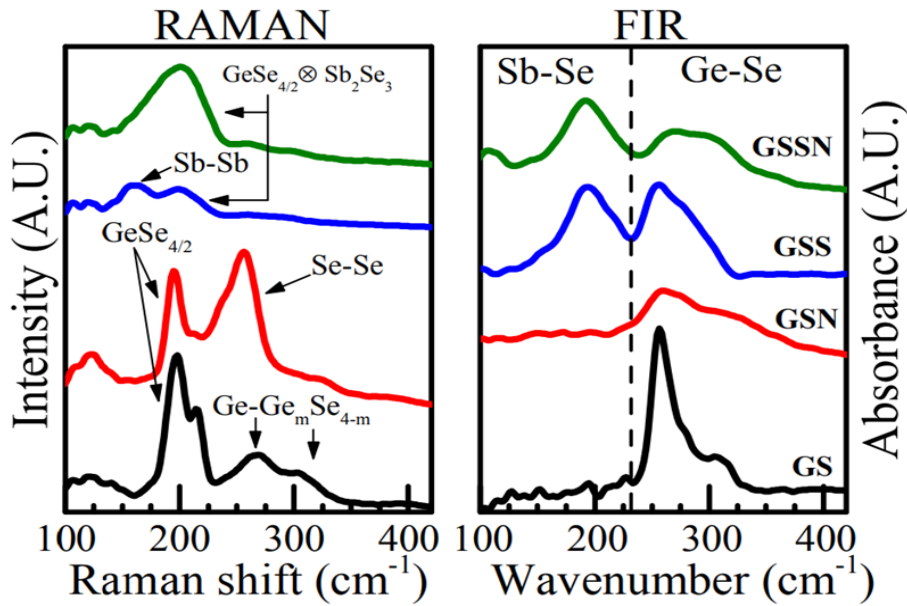


Figure 4.7: Raman and Far Infrared (FIR) absorption spectra for the four alloys studied: GS, GSS, GSN, and GSSN (This work). GS is characterized by a peak of heteropolar Ge-Se bonds. N allows the reduction of the wrong bonds Sb-Sb and Ge-Sb, which reduce V_{th} , but highly increase $I_{leakage}$ in GSS alloys. Hence, a good compromise between these two metrics was obtained for the GSSN selectors. Taken from: [53]

In order to study local structure impact of doping over the amorphous phase, Verdy *et al.* [53] performed Raman and Far Infrared (FIR) absorption spectra for the various alloys introduced in Figure 4.6. The result is presented in Figure 4.7. For the GS case, heteropolar Ge-Se bonds are dominant. In subsection 4.1.1, it was stated how this motifs were held as one of the responsables for the switching mechanism.

For the GSS case, even if Ge-Se bonds are still relevant, heteropolar bonds Sb-Se and homopolar Sb-Sb, are also present [51]. Sb-Se motifs are responsible for the induction of electronic states and the consequent bandgap reduction, which implies V_{th} decrease. The inconvenient resides in the fact that these phases tend to segregate and to crystallize. Further experiments by Noe *et al.* [9], demonstrated that for the GSS alloy, Ge-Sb bonds also appear. These phases, along with the homopolar Sb-Sb, introduce midgap states, responsible for the $I_{leakage}$ values increase. In order to avoid their appearance, N is used.

Hence, Sb-Sb and Ge-Sb bonds are replaced by Ge-N and Sb-N ones, which are more likely to be formed [9]. Conversely, Sb-Se motifs, responsible for the threshold voltage reduction are kept. This is how, GSSN keeps a very competitive leakage current and a manageable V_{th} level.

With doping effects understood and having a very likely working mechanism, splits and doping profiles of the OTS devices could be studied. At this point, it must be recalled that very complete works on GSSN selectors, were previously developed by our research group and can be consulted in [5, 10, 45, 53]. Using their results as a basis, in the following, some additional studies will be provided in order to have high compatibility, at the electrical level, between OTS and ReRAM devices.

In a first stage, effect of Sb doping over the GSSN composition was analyzed. It can be appreciated in Figure 4.8. There, and thanks to doping levels up to 20%, previous structural observations can be verified at the electrical level for $V_{Forming}$, V_{hold} , V_{th} , and $I_{leakage}$. In the case of the threshold voltage, values for both voltage polarities are presented. Even if high Sb concentrations imply degradation of the insulating capabilities of the selector devices, the effect over the forming voltage is considered to be more convenient in terms of 3D crosspoint arrays implementation. That is why, 20% Sb concentrations were chosen, for the fully integrated devices, in order to favor low operating voltages of the 1S1R devices, while keeping acceptable leakage current levels.

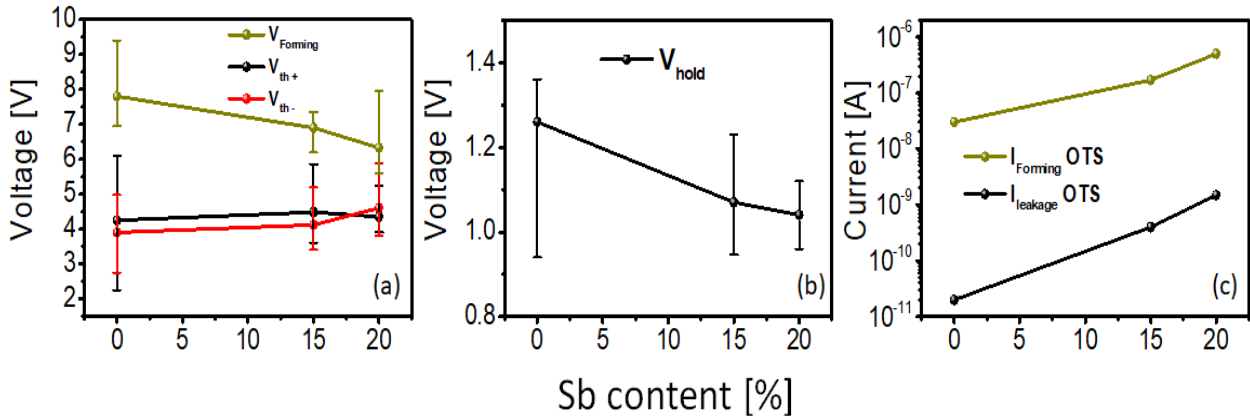


Figure 4.8: Electrical influence of the Sb doping over electrical performances of GSSN alloys. Selector thickness is 20nm for this case. (a) $V_{Forming}$, V_{th+} , and V_{th-} (threshold voltages for positive and negative biases) measured in pulsed mode versus Sb concentration in the OTS. (b) V_{hold} as a function of the Sb concentration measured in AC mode too. (c) Forming (taken at the switching voltage) and leakage currents (@ 1V) of the OTS measured in quasi-static. For all the presented results, error bars correspond to 1σ

4.3.2 GSSN thickness: influence over electrical performances

Once GSSN composition was fixed ($Ge_{24}Se_{56}Sb_{20}$ with 8% N doping), thickness effects were studied. To do so, layers varying between 10 and 25 nm thick were characterized.

Main results are presented in Figure 4.9 thanks to quasi-static measurements. It is observed how thicker layers imply higher switching voltages. It leads to higher activation barriers to create the metastable filament responsible for the switch. These results were used on the development of the Metastable Nucleation Filament Model (MNFM) in subsection 5.5.2. Moreover, thicker selectors present lower leakage currents. In order to keep good insulating capabilities 15-25 nm thicknesses were picked up for the subsequent studies.

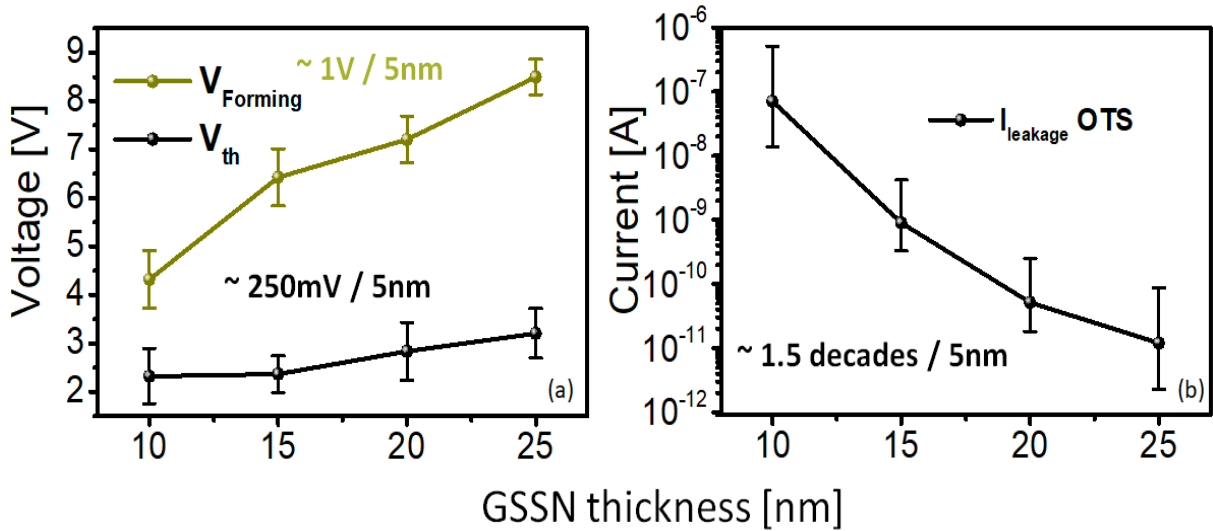


Figure 4.9: Electrical influence of the GSSN thickness. Thicknesses between 10-25 nm were characterized. (a) $V_{Forming}$ and V_{th+} voltages increase with thickness. On the other hand $I_{leakage}$ (@ 1V) (b) is lower for thicker configurations. Error bars correspond to 1σ .

4.3.3 OTS: thermal considerations

If intended to be used in a Cu BEOL, elements inside crosspoint arrays need to perform material processes below $400^\circ C$. If it is not the case, adding high thermal budget elements could lead to disturbances of the CMOS circuit periphery [57]. On the other hand, and for selector devices, they need to be stable around such temperatures to avoid segregation and/or crystallization of the chalcogenide material [45]. According to Burr *et al.* [2], the access devices must be able to withstand around 2h up to $400^\circ C$, in order to account for the wiring levels and the processes made around them.

GeSe alloys present excellent thermal stability [9]. However, and as observed previously, its electrical performances are not the best and necessity of doping is evidenced. On the other hand, introduction of Se implies appearance of unwanted Sb-Se phases, which tend to crystallize, producing poor thermal features for GSS materials. Crystal rigidity is introduced by N doping, avoiding homopolar bonds (see subsection 4.3.1), hence keeping the GSSN alloy stable and compatible with the BEOL thermal budget [53]. A final aspect, worth to be mentioned, is the use of annealing at temperatures fully compatible with the BEOL thermal budget over Se-rich Ge-Se based selectors, in order to improve its electrical

performances [45]. Annealing can lead to advantageous pattern reconfigurations, mainly Ge-N bonds for the GSSN case. As a consequence, threshold voltages can be reduced (V_{th} , $V_{Forming}$ as well as the ratio difference between them), while acceptable increase of the leakage current is observed, without affecting endurance behavior or selector operation at high temperatures (up to $150^{\circ}C$ tests were conducted) [45].

4.4 ReRAM+OTS co-integration

4.4.1 Technological details

With the right thicknesses (15-25 nm) and Sb doping (20%) for the GSSN selector, defined thanks to optimization processes, 1S1R co-integration was developed. A TEM-EDX and a HAADF view of the OTS+ReRAM devices are presented in Figure 4.10, demonstrating, from a morphology standpoint, successful co-integration of the various layers while fulfilling the BEOL thermal budget. ReRAM memory is deposited over a TiN bottom electrode using a 5nm ALD Hafnium Oxide (HfO_2) layer, combined with a PVD Ti/TiN bilayer [58]. The selector device is deposited thanks to magnetron sputtering without vacuum break aiming to avoid surfaces oxidation. Dry etch is used to define large memory dots with sizes ranging from 300 to 600 nm, without notorious effects over the electrical performances being appreciated for formed devices.

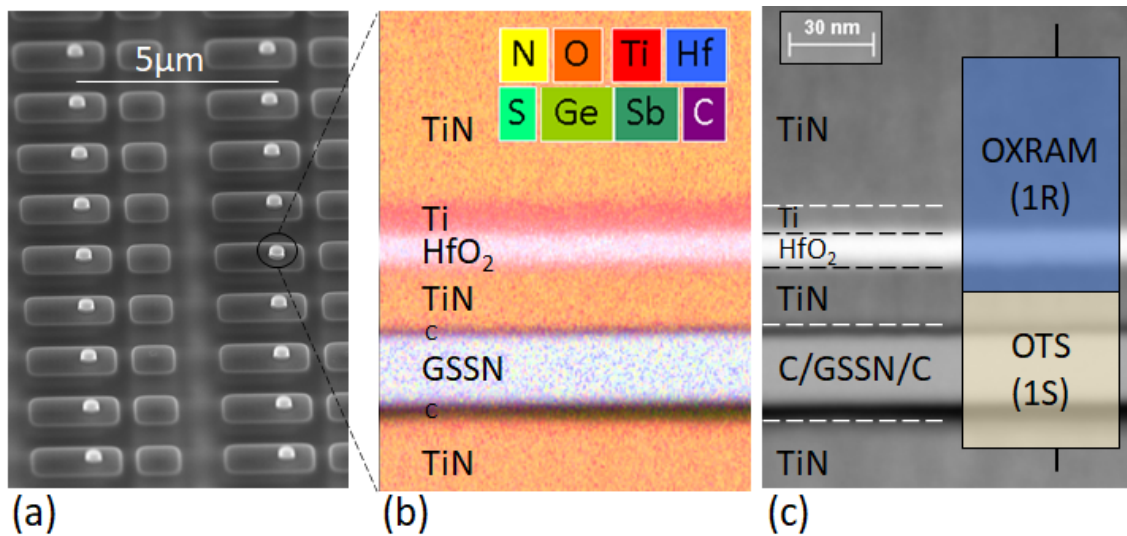


Figure 4.10: (a) SEM top view of ReRAM+OTS devices, (b, c) TEM EDX and HAADF cross sections of ReRAM+OTS 1S1R stack studied in this work.

Chalcogenide materials are vulnerable to metallic electrode diffusion [59] and oxidation [60]. In previous works [46], it was observed how Ti diffusion, induced by the electric field inside the chalcogenide alloy, and near to the GSSN/TiN interface, was responsible for degraded performances of the OTS devices, notably leakage current increase and reduced endurance. This was caused by the appearance of non-controlled crystalline $Ti - Se_2$

phases. In order to avoid such diffusion, two thin carbon electrodes ($\approx 2\text{nm}$), are used around the GSSN layer (see Figure 4.10). They are deposited by PVD, which, under the right conditions can be used to modulate carbon electrical conductivity too. The direct consequence of the introduced layer, besides leakage and endurance improvement is a slight increase of the ON state resistance of the OTS. V_{th} and $V_{Forming}$ are also bigger ($\approx 1\text{V}$). However, in the case of switching voltages as well as leakage currents, dispersions are smaller, and chalcogenide oxidation induced by air exposure at room temperature is also demonstrated to be reduced [46].

4.4.2 ReRAM+OTS switching

Electrical characterizations over the co-integrated 1S1R systems were performed. Firstly, the typical IV behavior of formed devices in the case of a positive bias for both elements (*GSSN* and *HfO₂* stacks), is recalled in Figure 4.11. As it can be observed, V_{th} of the OTS is higher than V_{SET} of the ReRAM. A voltage divider between the two devices, makes that the applied voltage drops over the most resistive element. This is the observed situation for the IV curve of the 1S1R device, presented in Figure 4.12, where the before switching current trajectory, is defined by the sub-threshold behavior of the selector.

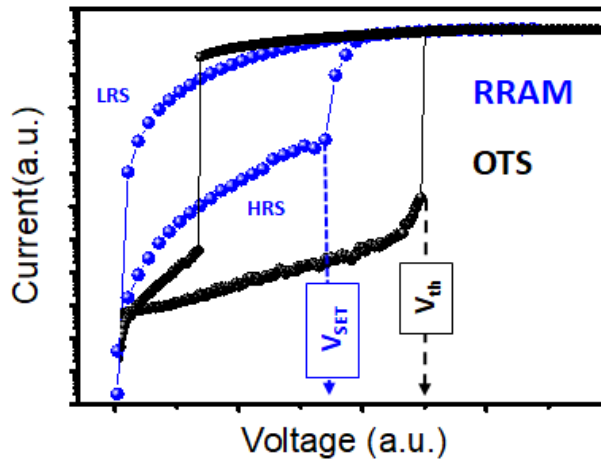


Figure 4.11: IV curve for the GSSN OTS and the *HfO₂* ReRAM devices. In the case of a 1S1R system, the almost totality of the applied voltage drops over the most resistive element, the OTS, if $V_{applied} < V_{th}$.

Given that $V_{th} > V_{SET}$ and $R_{OFFOTS} \gg R_{HRS ReRAM}$, both OTS and ReRAM memory, switch once V_{th} is reached. When this happens, the OTS becomes highly conductive and all the voltage drop is translated into the resistive memory in HRS, leading to its SET process⁽⁴⁾. On the contrary, if the ReRAM is in the LRS and for a positive polarity, once V_{th} is reached, selector goes into the ON state but the ReRAM remains at its LRS given that the RESET requires a negative bias. For this case (OTS ON and ReRAM in

⁽⁴⁾This same process applies for pristine devices: selector and memory are formed simultaneously once $V_{FormingOTS}$ is reached. This is due to $V_{FormingOTS} \gg V_{FormingReRAM}$ (for the used *GSSN* and *HfO₂ OxRAM* stacks)

LRS), voltage drop is shared by both elements. Moreover, the IV curve characteristic of the ReRAM element, implies different voltage drops as a function of its resistive state, leading to the observation of two different threshold voltages, V_{th1} (ReRAM in HRS) and V_{th2} (ReRAM in LRS), of the 1S1R system. Such difference is used to define the reading strategy of the OTS+OxRAM devices, treated in the next section. Additionally, and given that the voltage drop at I_{th2} for an OxRAM in LRS is very small (as observed in Figure 4.11), $V_{th2} \approx V_{th}$.

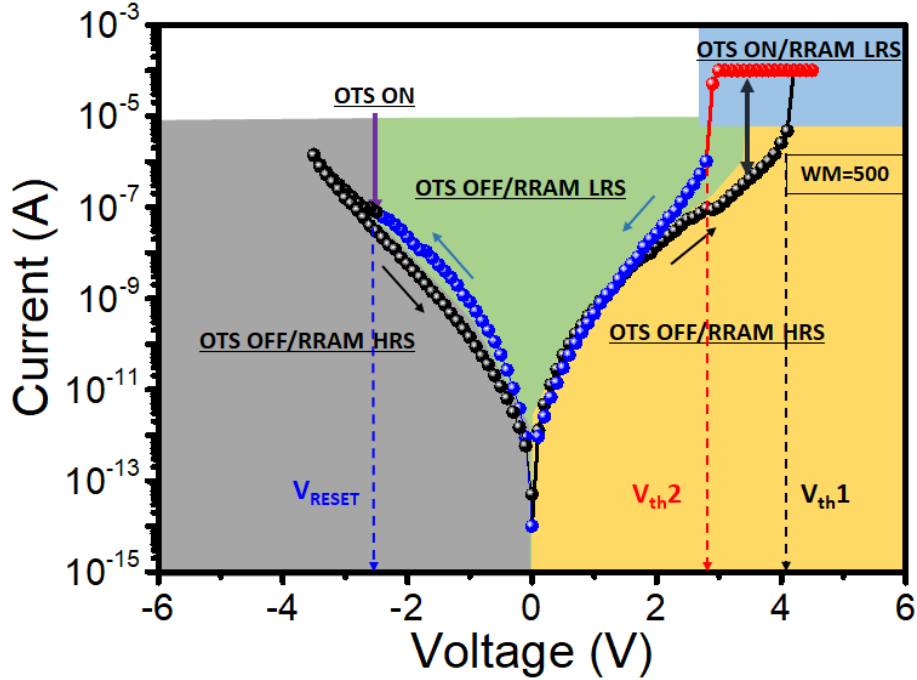


Figure 4.12: Typical IV characteristics of the co-integrated 1S1R device using a 20nm GSSN and a 5nm HfO_2 OxRAM memory. Both ReRAM and OTS states are indicated depending on the applied voltage.

If a negative bias is applied and the memory is in the LRS, OTS switches into the ON state at $|V_{th}|$ and given that $|V_{th}| > |V_{RESET}|$, RESET process is almost simultaneous to OTS switching. The current allowed by the HRS value of the ReRAM, is not enough to keep the selector in the ON state, which leads to a barely appreciable RESET switch over the 1S1R IV curve for most of the measurements, as it is the case in Figure 4.12. Its most common characteristic is a slightly reduction of the measured current (V_{RESET} in Figure 4.12), as a product of the resistance increase of the 1S1R device, caused by the OxRAM, now in the HRS.

4.4.3 Reading scheme

A pertinent reading strategy consists in being able to sense the 1S1R state without affecting data integrity (i.e., switching the memory), and without erratic reads. Based on electrical performances hypothesis, and assuming that in order to provide high NL,

Chapter 4: Co-Integration of OTS+OxRAM memory for crosspoint arrays

$R_{OTS\ OFF} \gg R_{ReRAM\ HRS}$; three different reading scenarios have been identified and summarized in Table 4.2 and Figure 4.13 respectively. They are explained next:

Table 4.2: Identified reading strategies for 1S1R devices. V_{Read} specifications are established for every case. Each strategy corresponds to non-destructive reading.

	OTS always ON		OTS always OFF		OTS ON when ReRAM in LRS [This work]	
	ReRAM LRS	ReRAM HRS	ReRAM LRS	ReRAM HRS	ReRAM LRS	ReRAM HRS
OTS state during reading	ON	ON	OFF	OFF	ON	OFF
Read R	$R_{ReRAM\ LRS}$	$R_{ReRAM\ HRS}$	$R_{OTS\ OFF}$	$R_{OTS\ OFF} + R_{ReRAM\ HRS}$	$R_{ReRAM\ LRS}$	$R_{OTS\ OFF} + R_{ReRAM\ HRS}$
V_{Read} condition	$V_{th} < V_{Read} < V_{SET\ ReRAM}$		$V_{Read} < (V_{SET\ ReRAM}, V_{th})$		$V_{th\ 2} < V_{Read} < V_{th\ 1}$	
Requirements	$V_{th} < V_{SET\ ReRAM}$		N/A		$V_{th} > V_{SET\ ReRAM}$	

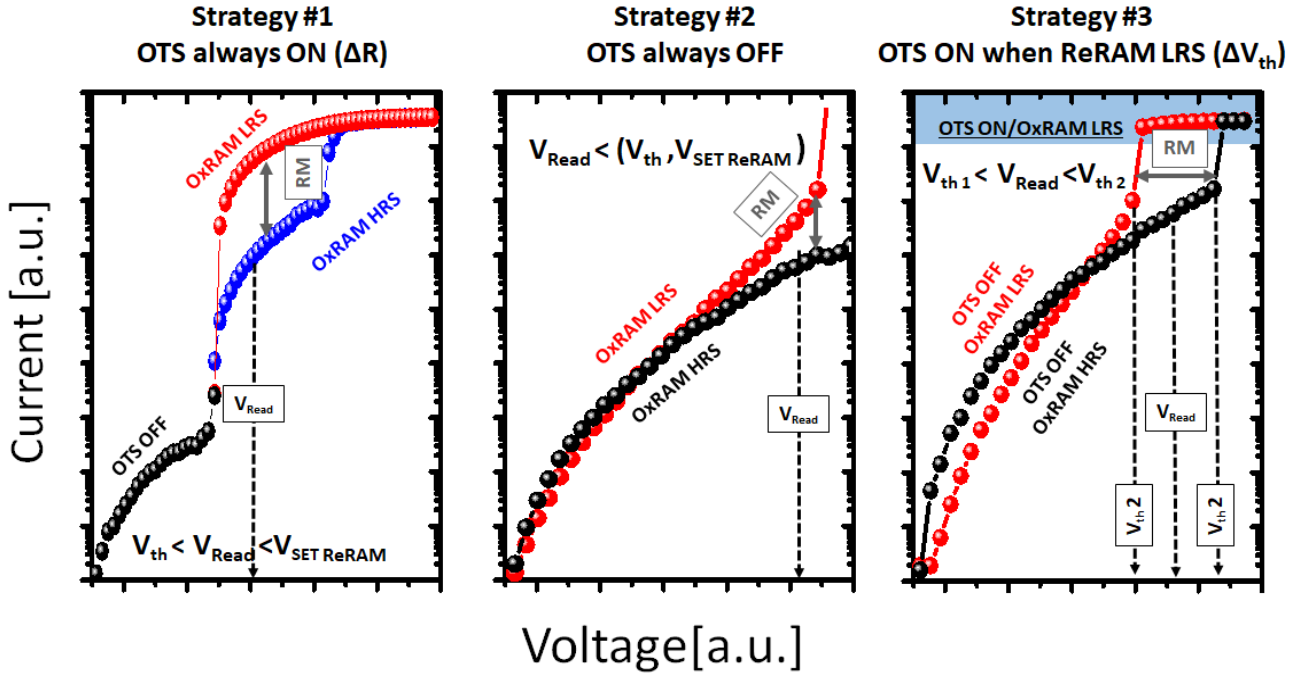


Figure 4.13: Example of the IV characteristic for the reading schemes presented in Table 4.2. Reading margin (RM) and V_{Read} conditions are specified for every case. An OTS always ON strategy requires $V_{th} < V_{SET\ ReRAM}$, while for an OTS ON when ReRAM in LRS strategy, $V_{th} > V_{SET\ ReRAM}$ is needed.

- **OTS always ON** This strategy, also known as ΔR [10], requires a low V_{th} and switching the OTS for every operation: read, SET, RESET. Besides, I_{th} and I_{hold} are required to be low in order to avoid data corruption. Although V_{th} needs to be low, non-selected cells need to be kept off for every bias strategy used to operate the array. The main consequence of this is that $V_{Bias\ non-selected\ cells} < V_{th} < V_{SET\ ReRAM}$. The read voltage is applied in the $V_{th} < V_{Read} < V_{SET\ ReRAM}$ and the read resistance corresponds to the LRS or the HRS of the memory device. This reading scheme, is not applicable to our $GSSN + HfO_2$ devices given that $V_{th} > V_{SET\ ReRAM}$.

- **OTS Always OFF** A subthreshold read (already theorized in [61]), requires a current difference caused by the resistive state of the memory element, enough appreciable to be amplified. This is the only requirement, and since a power consumption perspective, this strategy seems the best one. However, given that subthreshold currents are expected to be low ($< 1\mu A$), some amplification systems may not be sensitive enough to well differentiate the two resistive states. In the case of the $GSSN + HfO_2$ systems presented in this work, OTS always OFF reading strategy, was intended to be applied. Nevertheless, not reliable current window was obtained, because of subthreshold currents variability.
- **OTS ON when ReRAM in LRS** As discussed previously in subsection 4.4.2, if $V_{th} > V_{SET ReRAM}$ (see Figure 4.11), the voltage drop over the resistive element at I_{th} is different as a function of its resistive state. It causes a V_{th} shift, where V_{th1} corresponds to the HRS and V_{th2} to the LRS respectively. Therefore:

$$\Delta V_{th} = V_{th1} - V_{th2} = Read\ Margin(RM) \quad (4.1)$$

This can be profited in order to read the memory state, keeping data integrity. **V_{Read} is applied inside this range and the OTS switches only when the OxRAM is in the LRS.** This strategy, also known as ΔV_{th} reading scheme, has been widely proposed in literature for 1S1R systems [10, 49, 57] and given the electrical characteristics obtained in Figure 4.11, is the most convenient for the $GSSN+HfO_2$ structures. Two read currents corresponding to two different resistive states at V_{Read} , $R_{ReRAM LRS}$ and $R_{OTS OFF} + R_{ReRAM HRS}$ can be extracted and used as logic states. The first one of them is usually the compliance current defined for the 1S1R device ⁽⁵⁾. For the quasi-static measurements, the implemented setup was presented in subsection 2.3.2.a. There, current is limited by a Parameter Analyzer (Agilent 4156 or Keysight B1500) equipment.

A detailed quasi-static example for the $GSSN + HfO_2$ devices, with the most important numerical values and electrical parameters to be taken into account when applying this reading strategy, is presented in Figure 4.14. A ΔV_{th} of +1V leads to a $V_{Read} = 3.5V$. At V_{Read} , a window margin of 500 is obtained. Moreover, a current ratio of 600 between the reading current of selected and unselected devices, assuming a $V_{Read}/3$ biasing scheme, is measured in the worst case. This last feature is capital when estimations of the maximum size of crosspoint architectures employing 1S1R devices are intended to be made, as it will be the case later in this chapter.

As for the statistical distributions of the main metrics of the $GSSN+HfO_2$ systems, for a 20nm $GSSN$ and a 5nm HfO_2 , they are presented in Figure 4.15: leakage current median value of $\approx 1nA$ when OTS is OFF at $V_{Read}/3$ with $V_{th2} < V_{Read} < V_{th1}$, and a window margin of ≈ 2 decades between ON (OxRAM in LRS) and OFF (OxRAM in HRS) currents, are obtained. Switching voltages are also shown. It

⁽⁵⁾For most of the results obtained in this chapter, a typical compliance value of $100\mu A$ is used to protect the resistive memory, while reducing power consumption.

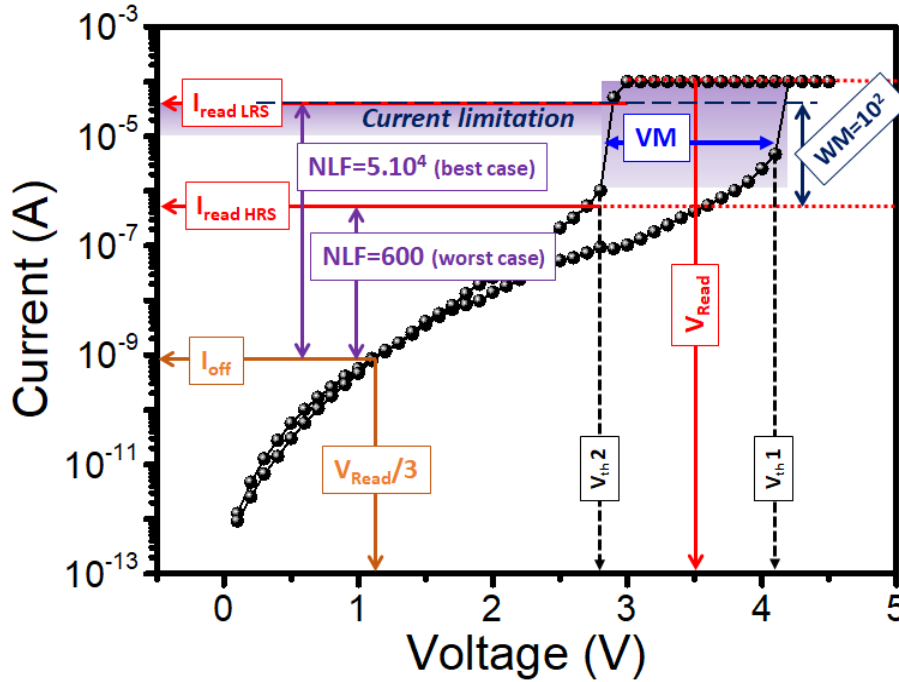


Figure 4.14: Typical IV curve of 1S1R device indicating non linear factor (NLF), reading voltage margin (RM) and resistance window margin (WM). Reading strategy number 3 from Table 4.2 is adopted.

can be observed how $|V_{th2}| \approx |V_{RESET}|$ given the symmetric behavior of the OTS device.

4.4.4 Reading margin evolution with thickness and influence over OxRAM resistive states

A first validation of the *OTS ON when ReRAM in LRS* reading strategy, consists in studying the RM over diverse GSSN thicknesses. Figure 4.16 reports median values as well as $\pm 1\sigma$ error bars for both V_{th1} and V_{th2} switching voltages. It can be appreciated how RM is kept for all the selector thicknesses used in this study (15-25nm). A bell shape behavior is a priori observed and a maximum reading margin seems to be reached for the 20nm GSSN. This could indicate a higher difference between the programmed HRS and LRS resistances. Unfortunately, the reading scheme used, does not allow to determine such values, in order to verify this hypothesis (as stated before, read currents are: the compliance current in the LRS case and that one corresponding to the $R_{OTS\ OFF} + R_{ReRAM\ HRS}$ resistance for a device in the HRS). To do so, 1T1R devices were tested, using a HfO_2 stack. Diverse pulse amplitudes were applied as well as read voltages at 0.1V allowing to correlate $V_{applied}$ to HRS and LRS states as illustrated in Figure 4.17.a. A bell shape is also observed with a maximum reading window around 2.5V in AC mode. The filamentary characteristic of ReRAM memories implies a time dependence of the switching values as in the case of OTS devices [62, 63]. If translated into DC mode

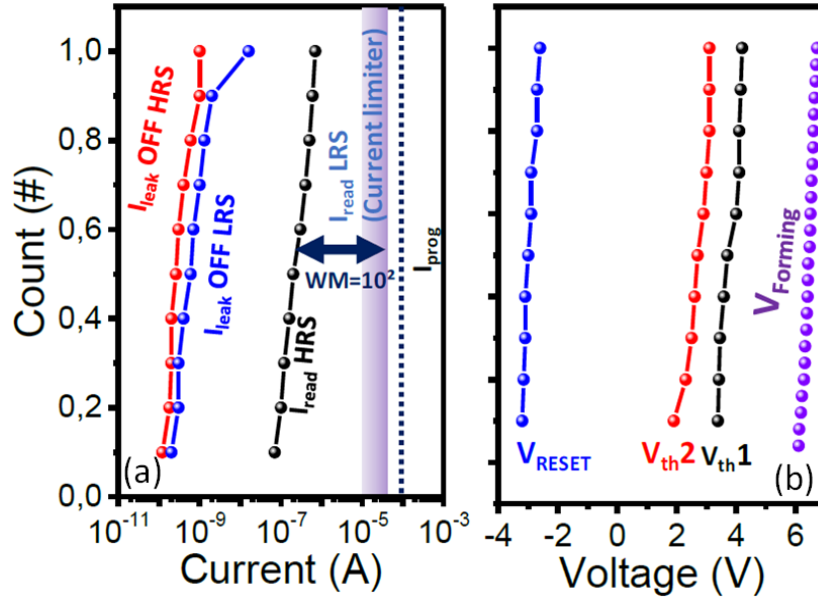


Figure 4.15: Cell to cell distributions for leakage and read currents as well as switching voltages extracted in quasi-static mode. Leakage currents are measured at $V_{Read}/3$ while two different currents are obtained as a function of the resistive state of the OxRAM at V_{Read} . For the LRS case, read current corresponds to the compliance imposed to the system. GSSN thickness is 20nm and HfO_2 is 5nm. It can be observed how $|V_{th2}| \approx |V_{RESET}| \approx V_{th}$, given that the memory in the LRS is highly conductive at I_{th} .

values, as it can be appreciated in the example in Figure 4.17.b, it can be verified how the SET voltages for the diverse HRS values, correspond more or less to the difference $V_{th1} - V_{th2}$ observed in 1S1R systems. From this, it can be concluded that the 20nm GSSN thickness allows to obtain the maximum Reading Margin thanks to a more or less optimal Window Margin between the OxRAM resistive states. This constitutes a first approach to determine the programming values of the ReRAMs co-integrated with GSSN selector devices spanning diverse thicknesses. Deeper estimations using modeling techniques are developed subsection 5.5.1.

4.4.5 Pulsed mode operation of 1S1R devices

While quasi-static measurements give information about the operation modes of 1S1R devices and the interpretation of key electrical parameters, a pulsed-mode, which is used during the operation of commercial products, gives information about the high speed dynamics of the devices. To do so, setup previously presented in subsection 2.3.2.a is used. A series resistance is added in order to limit the current flowing through the tested device. However, its use implies the appearance of unwanted RC effects if short pulses or high series resistance values are used, causing a temporal delay between applied and measured voltages, and hence hindering measurements reliability. That is why, it would be preferred to have more accurate elements acting as current limiters, as it is the case

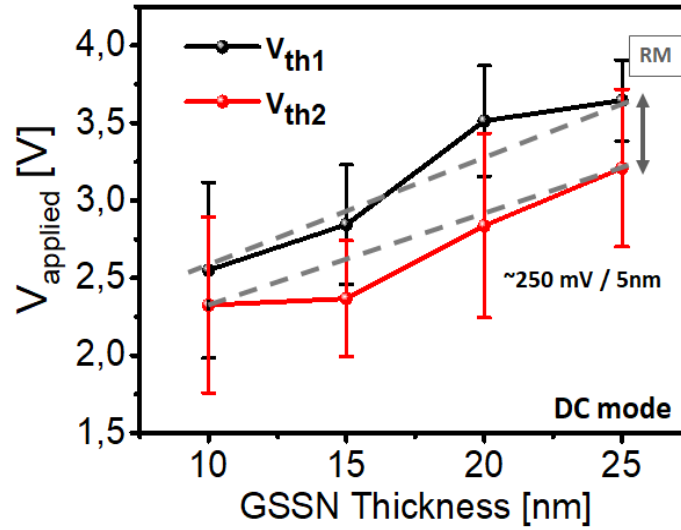


Figure 4.16: Impact of GSSN thickness on 1S1R DC switching voltage when the OxRAM is in HRS (V_{th1}) and in LRS (V_{th2}). An optimum RM seems to be reached around 20nm GSSN thickness.

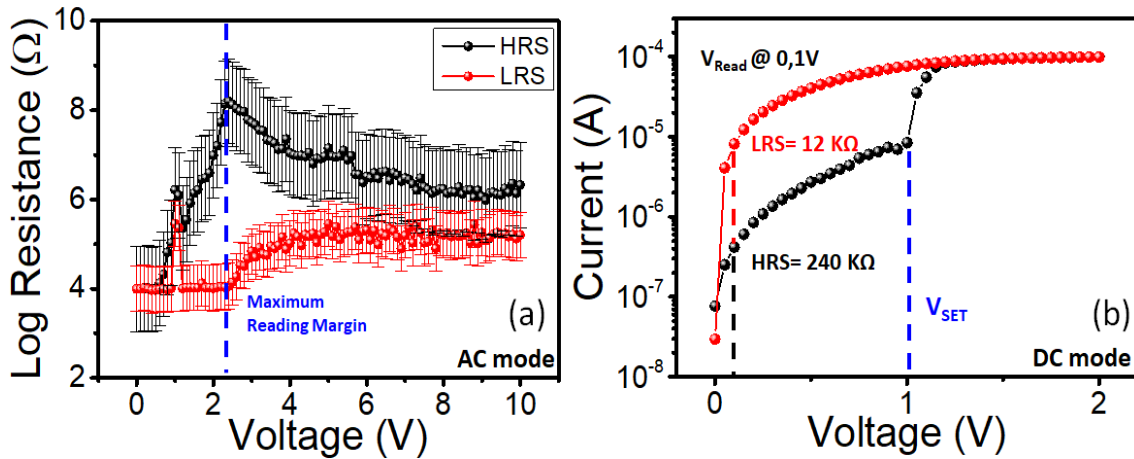


Figure 4.17: (a). 1T1R device tested for a large range of pulses amplitudes with subsequent reads at 0.1V. Evolution of the Window Margin can be appreciated with a maximum value around 2.5V. (b). IV characteristic example with the resistance values indicated for a read at 0.1V. For the same HRS value, DC SET at 1V is equivalent to more or less 1.7V in AC mode.

of transistors used for the chapter 3 studies. This devices improvement (i.e., 1T1S1R systems) was included in further stages of this work, enabling the possibility to effectuate reliability and variability studies over the 1S1R systems, which are the main core subject in chapter 5.

Pulses examples for SET and RESET processes, corresponding to positive and negative biases respectively, are presented in Figure 4.18. In there, $V_{applied}$ stands for the applied voltage to the series equivalent of the device under test (1S1R in this case) and the

external series resistor previously mentioned. The voltage drop over the tested device as well as $V_{applied}$, are monitored thanks to the use of an oscilloscope. In the case of a SET pulse (Figure 4.18.a), initially, the OxRAM is in the HRS, once V_{th1} is reached, the OTS goes into the ON state and the memory goes into the LRS. Thanks to the current limitation provided by the series resistor, it can be observed how the voltage drop over the 1S1R device is controlled. Long rise and fall times are used in order to appreciate all the electrical transitions in an optimal way. Once the voltage level goes under a certain level, the selector goes back into the OFF state at V_{hold} , which is also signaled. As for a negative bias and with an OxRAM in LRS, shorter pulses and higher series resistance values are furnished, in order to avoid HRS degradations, given that lower currents are characteristic to this memory state. This is the reason why, a RC effect, which causes a temporal shift between $V_{applied}$ and V_{1S1R} is reported in Figure 4.18.b. In a similar way to the DC behavior, once the OTS goes into the ON state at V_{th2} , the induced RESET state over the ReRAM makes the current flowing through the 1S1R system to be lower than I_{hold} , leading the selector to go back into the OFF state. The voltage difference between $V_{applied}$ and V_{1S1R} corresponds to the temporal shift already mentioned.

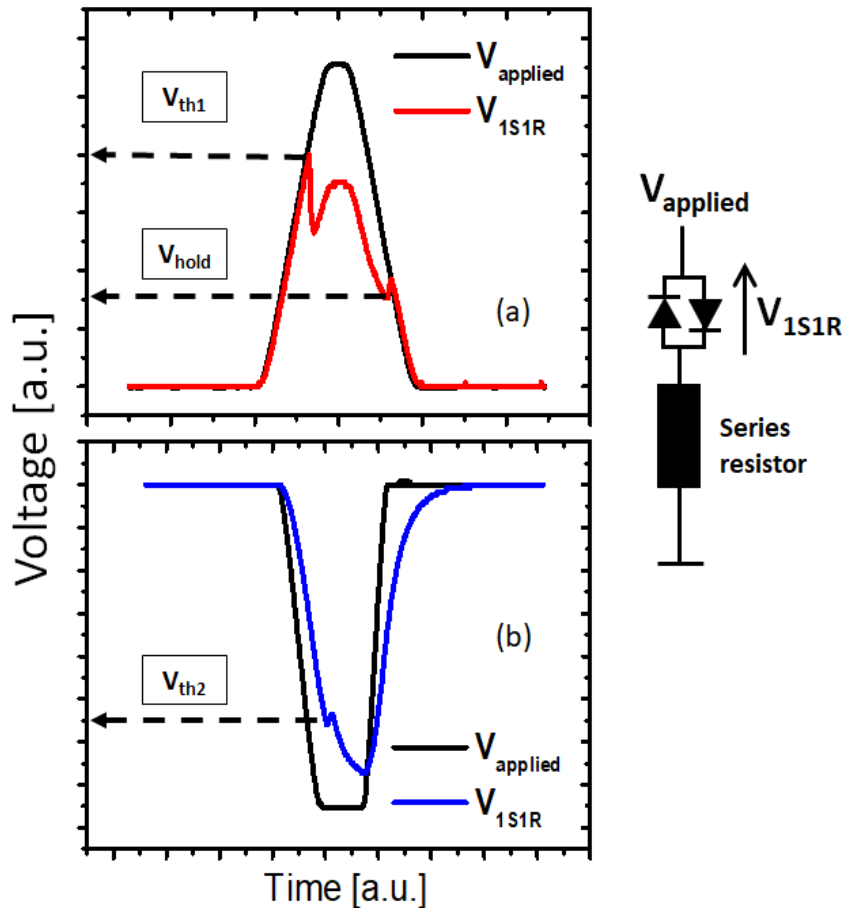


Figure 4.18: Typical pulsed measurement for 1S1R devices presenting SET and RESET pulses examples. Through it, V_{th1} (OxRAM in HRS) and V_{th2} (OxRAM in LRS) behavior can be studied. A series resistor is added and used as current limiter.

This pulse methodology and all the considered aspects, allow to study the V_{th1} and V_{th2} behavior in pulsed mode in order to verify its stability and to validate the chosen *OTS ON when ReRAM in LRS* reading strategy. An example of this, is reported in Figure 4.19 where after some pulses, a $RM \approx 1V$ is reached. As mentioned in section 4.3 introduction, higher V_{th} values are obtained in pulsed mode. In order to keep data integrity, a V_{Read} should be applied around 4.5V for a co-integration with a *GSSN* and a *HfO₂* with thicknesses of 20nm and 5 nm respectively.

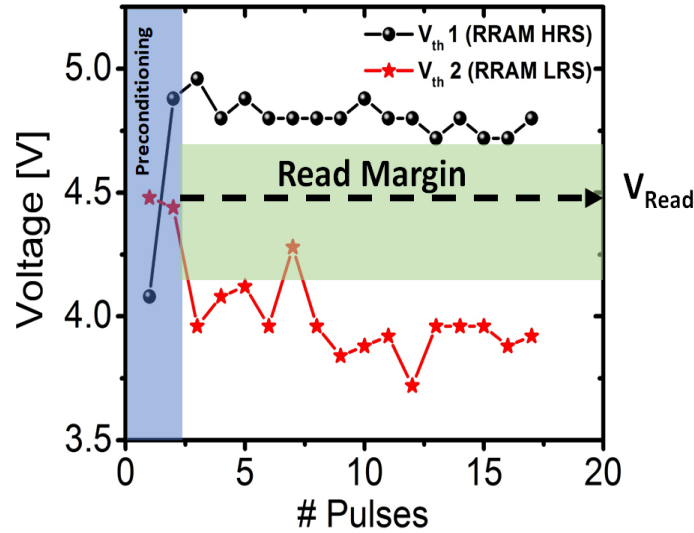


Figure 4.19: (a) V_{th1} , $|V_{th2}| \approx |V_{RESET}|$. Threshold voltages of the 1S1R device measured in pulsed mode (mean value over 10 devices). After some preconditioning pulses, RM of $\approx 1V$ is obtained (median value)

4.4.6 Temperature Stability

Some thermal aspects of selector devices were already treated in subsection 4.3.3. Another one, very well known in amorphous chalcogenides is the resistance drift [8, 37]. Resistivity tends to increase with ageing, which could lead to hinder data integrity due to a Reading Margin (RM) reduction. The process is thermally activated and this is the reason why, it is pertinent to study it at high temperatures and as a function of the elapsed time, in order accelerate and to simulate environmental conditions linked to specific applications.

Several theories can be found in literature aiming to explain resistance drift. Originally destined to be used in studies over typical PCM materials, they could be applied to provide explanations of the resistance drift of OTS alloys too. They are mainly classified into three categories [37]: drift impacted by stress [64, 65], changes in the defect density [66, 67], and changes in the disorder structure [68–72]. All of them converge into a general consensus conclusion: drift is caused by some kind of relaxation of the amorphous structure that leads to a larger energy gap and to a higher localization of the gap states, which are less responsible for conduction after material relaxation [73, 74].

At this point, it is important to clarify the difference between resistance drift thermally activated and the beneficial annealing process, prior treated in subsection 4.3.3. It resides in the fact that praised annealing procedure implies a patterning reconfiguration of some bonds as demonstrated in [45]. There, drift phenomenon was also observed for a range of temperatures. Moreover, and worth to be also mentioned, drift and crystallization imply different mechanisms too [8].

To evaluate drift occurrence in 1S1R systems and its influence over devices in the LRS and the HRS, baking at 165°C was realized. The IV characteristic before and after 20h of baking is reported in Figure 4.20.a. It is found that the drift mainly affects devices programmed in the LRS and therefore the V_{th2} value as well as the sub-threshold current, while only a slight variation of V_{th1} is measured. An acceptable RM is kept but high operating temperatures will cause RM reduction. Sub-threshold current readings were also performed and presented in Figure 4.20.b. It can be observed how leakage current at $V_{Read} = 2V$ is also kept stable with a slight decrease, which is also consequent with the drift phenomenon. A similar result, was presented by Kim *et al.* in [41] for their PCM+OTS systems, which leads to suppose that the IV characteristic drift is mainly caused by the OTS device in our OTS+OxRAM devices.

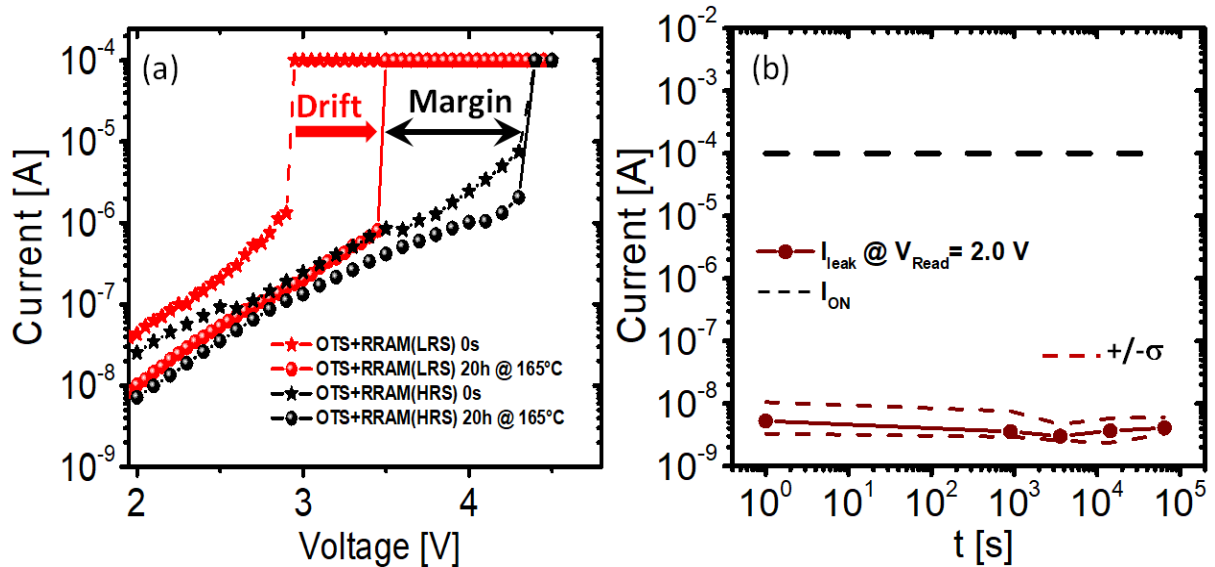


Figure 4.20: (a) IV switching characteristics of 1S1R device before (dashed line) and after (cont. line) 20h 165°C bake for ReRAM in HRS (black) and LRS (red) states. Despite LRS drift, voltage margin is maintained. (b) Time evolution of 1S1R current (dashed lines correspond to $\pm 1\sigma$ dispersion) at 165°C for ReRAM in HRS and OTS in OFF state (V_{Read} below switching). A slight decrease of leakage current is observed, which is consequent with the drift theory.

4.5 Design of 1S1R in crosspoint memory arrays

In this section, main challenges in the design of cross-point memory arrays are treated using electrical performances of $GSSN + HfO_2$ devices obtained, as a basis. Among such challenges, bias schemes, non-linearity of the used devices, voltage drop along interconnecting lines and non-selected cells; can be accounted. The area of a 1S1R device can be as small as $4F^2$ (minimum achievable cell size, where F is the minimum feature size of a technology node). Additionally, crosspoint systems can be placed above the CMOS logic in the BEOL. These two features favor memory density thanks to area occupation optimization. However, if reaching high densities is expected, energy consumption of the 3D array is essential, in the case of high performance circuits as well as portable devices where battery consumption is capital.

4.5.1 Bias Schemes

To tackle the power issue, first aspect to consider is the energy required to read, write or erase the memory points, which is dependent of the operation mode and the leakage currents coming from the non-selected devices for each one of such procedures. It could be simply said that leakages are intrinsic to the electrical characteristics of the 1S1R used technologies, but the bias schemes used to access the devices of interest, and to block the non-selected ones, have a direct influence over them too. The most common schemes are the V/2 and V/3 strategies. A depiction of them is presented in Figure 4.21. For both cases, the orthogonal Bit and Word Lines (BL and WL), are biased at the reading or SET voltage (called simply V here for clearness), and ground respectively; while for the RESET process, polarities are inversed. In any case, the non-selected WLs and BLs are connected to V/2 for the V/2 strategy, and to V/3 and 2V/3 for the V/3 scheme. This reduces the sneak path currents and consequently, the energy consumption of the array. 1S1R devices over the same BL and WL that the selected ones, experiment a V/2 or V/3 voltage drop, depending on the chosen bias scheme, hence explaining the origin of the bias scheme names. As for the rest of unselected devices, a 0V or V/3 voltage is seen, for V/2 and V/3 methods respectively. Therefore, a first conclusion can be extracted: V/2 bias scheme is more energy efficient than V/3 for big array sizes. Conversely, lower voltages, experimented by the terminals of non-selected devices in the case of a V/3 strategy, imply more immunity to data disturbance. Ciprut *et al.* [75], demonstrated that V/3 bias scheme is also better in terms of energy consumption if several bits per operation are intended to be addressed. Additionally, they proposed an hybrid bias scheme as well, in order to optimize consumption as a function of the selected cells, array size, and NL of the 1S1R devices.

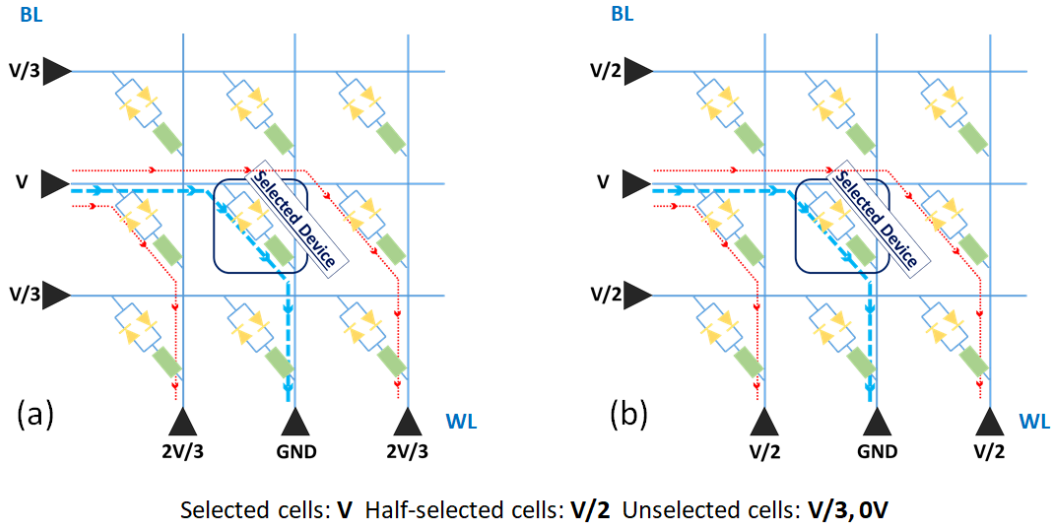


Figure 4.21: Most used bias schemes for 1S1R systems in crosspoint arrays: (a) $V/3$ and (b) $V/2$ strategies are depicted.

4.5.2 Size estimations based on sensing limit features of periphery circuits

As stated before, non-selected devices over the same selected BL and WL, experiment either a $V/2$ or $V/3$ depending on the bias scheme used. Remaining unselected ones see a $0V$ and a $V/3$ voltage drop as a function of the used strategy (see Figure 4.21). It implies more energy efficiency in the $V/2$ case given that only the devices over the same BL and WL that the selected ones, present leakage current. On the other hand, all the unselected points leak under a $V/3$ bias scheme. This leads to establish total leakage equations for both strategies as a function of the number (n) of unselected leaking cells:

$$I_{leak\ total}(V/2) = I_{leak} * (2n - 2) \quad (4.2)$$

$$I_{leak\ total}(V/3) = I_{leak} * (n^2 - 1) \quad (4.3)$$

Where I_{leak} is the measured current at $V/2$ or $V/3$ for individual 1S1R devices.

Hence, maximum size of elementary array tile⁽⁶⁾ for $GSSN + HfO_2$ based 3D crosspoint systems, that could be envisaged, based on measured leakage currents can be estimated, as reported in Figure 4.22. Leakage median values for 15 and 25nm GSSN thicknesses (see Figure 4.9.b) were used, as well as I_{OFF} median values for both thicknesses. Using a typical compliance current of $100\mu A$ for the I_{ON} current, an $I_{ON}/3$ limit was established, in order to keep data integrity if a HRS is read. The maximum size, corresponds then to the intersection between such limit and the $I_{OFF} + I_{leak\ total}$ addition,

⁽⁶⁾A tile is an independent memory bank with bitcell arrays served by its own CMOS logic circuit. Memory organization is explained more in detail later in this section

where the second term is dependent of the n unselected cells (Equation 4.2 and Equation 4.3). Naturally, and as demonstrated before, $V/2$ bias scheme allows to obtain denser arrays. Up to 1Gb tile size is estimated for 25nm GSSN thickness for a $V/2$ bias scheme.

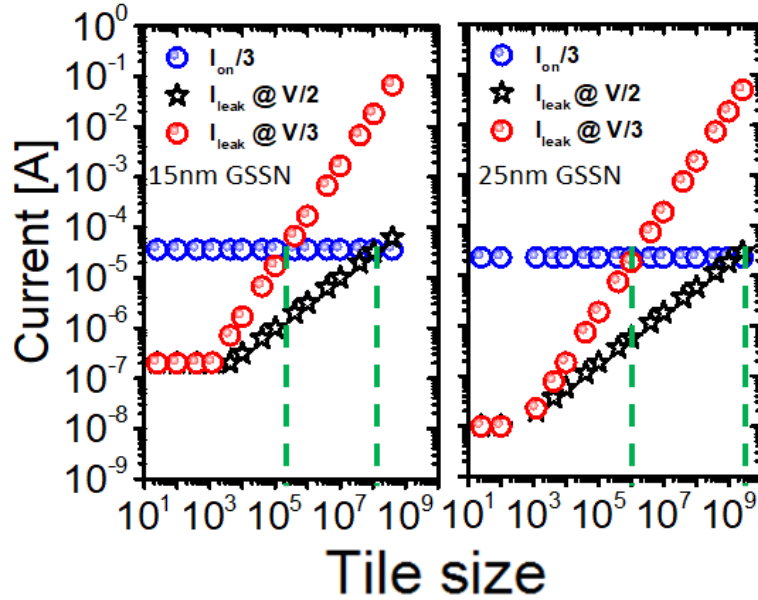


Figure 4.22: Estimations of the maximum tile sizes that can be obtained for 15nm and 25 nm GSSN based on $I_{leakage}$ measurements and using Equation 4.2 and Equation 4.3. The maximum size is reached once the cumulation of all individual leaking devices is equal to $I_{ON}/3$.

4.5.3 Size estimations limited by IR drop and periphery circuits

Besides the bias scheme and the NL of the 1S1R used technologies, defined by I_{leak} characteristics; voltage drop along interconnecting also called IR drop, needs to be considered in order to study arrays size. Already highlighted in section 4.2, this aspect gains importance with the decrease of the metal lines size and the spacing among them, given that thinner conductors imply higher resistivities. According to [76, 77], IR drop becomes critical for the sub-50nm technological nodes, because of electron scattering and interfaces between conductor and inter-metal dielectric, which cause high resistivity increases. An IR drop badly managed can result in programming fails or wrong reads due to insufficient voltages over the selected WLs and BLs. On the other hand, increasing operating voltages in order to handle the IR drop, may lead to over-stressed devices and hence, reliability decrease.

A model to estimate IR drop inside crosspoint arrays, was developed by Levisse *et al.* [77]. Using the metallic conductivity (σ_{metal}), and the metal half pitch distance (F)⁽⁷⁾, as parameters; unitary resistance of the metallic lines and columns, can be calculated as follows:

⁽⁷⁾The half pitch is the minimum spacing between two metal lines

$$R_{unit} = \sigma_{metal} \cdot \frac{L}{W \cdot H} = \frac{2 \cdot \sigma_{metal}}{AR \cdot F} \quad [77] \quad (4.4)$$

Where lines width (W) is equal to the half pitch distance (F), H stands for the height dimension, L is the shortest distance between two 1S1R points (L=2F), and AR is the ratio between height and width. A schematic view of the listed parameters is presented in Figure 4.23.

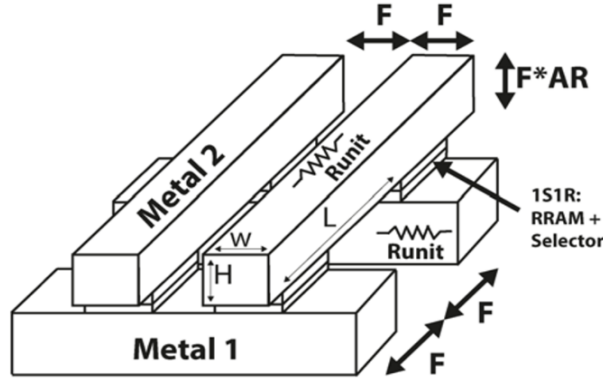


Figure 4.23: Physical schematic of a crosspoint arrays with dimensions used for IR drop estimations. Taken from: [77]

Consequently, the total voltage drop can be estimated using the equation:

$$V_{IR\ drop\ array} = R_{unit} \cdot \left((n_b + n_w) \cdot I_{prog} + \left(\frac{n_b \cdot (n_b - 1)}{2} + \frac{n_w \cdot (n_w - 1)}{2} \right) \cdot I_{leak} \right) \quad [77] \quad (4.5)$$

Whit n_b and n_w being the number of Bit and Word lines of the array, I_{prog} the programming current, assumed to be equal to the compliance in our case, and I_{leak} the leakage current for a V/2 or V/3 bias scheme.

These equations will be used below in order to calculate array sizes, taking into account the IR drop inside them and the electrical characteristics of the $GSSN + HFO_2$ systems.

As a last aspect, additional blocks, used to operate the memory array itself as well as their placing and dimensions, need to be considered too. Usually, denser arrays imply bigger peripheral circuits [78]. To avoid it, an interesting strategy consists in subdividing memories in several smaller tiles. Periphery blocks are mainly composed by: decoding and access circuits, programming circuitry, memory controller, and voltages management modules. Surface considerations for the periphery decoding and access circuits, were also proposed by Levisse *et al.* [77], and are used in this work. Since a general point of view, multiplexer and dynamic decoder circuits are dedicated for the WLs and BLs. Simultaneously, they are connected to the programming and sensing blocks, which are mainly composed by amplifier circuits. Given that inverse polarity voltages are needed to operate both BLs and WLs, pass gates (PG) are used to avoid V_T drops over the access

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transistors. These PG are composed by nMos and pMos in parallel. Operation conditions of the 1S1R cells and the technological nodes employed, determine CMOS dimensions for all the aforementioned blocks, which are expected to be located under the crosspoint arrays.

Thanks to the IR drop equations and to the periphery features, bank size limitations taking into account these two aspects for various half-pitches can be effectuated. They are presented in Figure 4.24 using a 20 nm *GSSN* thickness and 5nm for the *HfO₂* OxRAM. As mentioned above, periphery area is ideally placed in the FEOL under the crosspoint configuration. In order to define an upper limit for it, it is assumed that it should not overcome the memory array surface (i.e. maximum periphery/crosspoint surface ratio equal to 1). A smaller area, being even more profitable. The bank size is also limited by the voltage drop allowed. Typical 0.8V limit was assumed. IR drop as well as the periphery circuits are dependent on the 1S1R operation conditions, as well as the half pitches, inherent to various technology nodes. It can be observed how 1-10Mb sizes can be reached, which is much lower than the estimations obtained in subsection 4.5.2 based on I_{leak} metrics (see Figure 4.24.b.). It appears that the bank size is more limited by the technology node scaling than by the NL of the used devices itself. However, it is necessary to state that, for example, IR drop compensation techniques were not taken into account for the results reported in Figure 4.24. They are out of the scope of this work, maybe implying a pessimist scenario for the results here presented. On the other hand, multi-bit operations were neither considered, which means, that much more restrictive bank size estimations, based on I_{leak} performances, should be undertaken.

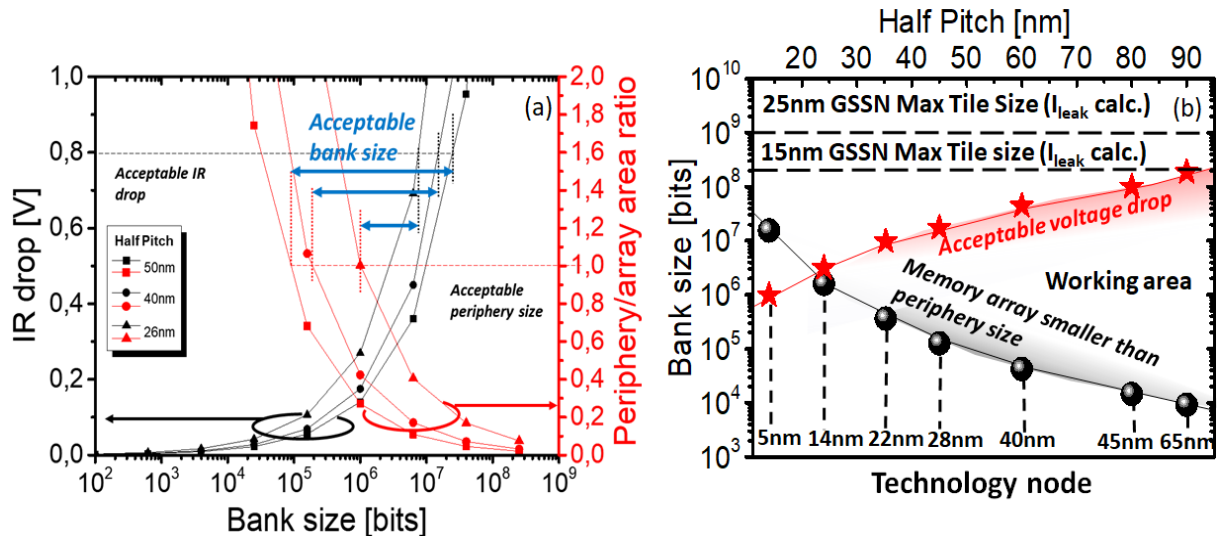


Figure 4.24: (a).**Black**: Calculated voltage drop along memory circuit as function of array tile size. Voltage drop is calculated during programming (worst case) for $I_{prog} = 100\mu A$ and I_{leak} of unselected cells from experimental data. **Red**: Estimation of the oversize of periphery under cell (with respect to memory array area). Working margin is extracted assuming $IR_{drop\ max} < 0.8V$ and no periphery oversize. (b). Evolution of bank size as a function of the technology half pitch. Working areas are defined depending on voltage drop along metal conductors, memory/periphery area ratio and I_{leak} estimations from Figure 4.22. A priori, bank size seems to be more limited by technological constraints than by NL of the 1S1R devices.

4.6 Conclusions and Perspectives

- **HfO₂/Ti** with **GeSeSbN** OTS device in 1S1R configurations were co-integrated for the first time with remarkable performances.
- Se-rich Ge-Se based selectors were optimized thanks to doping and thickness adjustments. Sb and N doping, contribute to OxRAM and OTS compatibility and improved electrical behavior. Based on electrical performances **Ge₂₄Se₅₆Sb₂₀ with 8% N doping** selectors were picked. Acceptable I_{leak} and threshold switching values were obtained for thicknesses going from **15** to **25nm**. For these dimensions, median $V_{Forming}$ from **6** to **8.5V**, V_{th} from **2.3** to **3.2V**, and I_{leak} from 10^{-9} to 10^{-11} ; were measured in quasi-static mode.
- Once *GSSN* + *HfO₂* systems were co-integrated, electrical characterization was undertaken. **5nm** thickness was used for the **OxRAM** devices. Voltage drop over the OxRAM under I_{th} once selector is switched, leads to a $\Delta V_{th} = V_{th1} - V_{th2}$ where V_{th1} and V_{th2} correspond to HRS and LRS resistive states of the OxRAM respectively. Moreover, $V_{th2} \approx V_{th} \approx |V_{RESET}|$ due to OTS symmetry and very low voltage drop over the memory in the LRS.
- ΔV_{th} allows to define a reading voltage inside this range. Hence, **during reading, OTS goes into the ON state if the OxRAM is in the LRS. A reading margin of $\approx 1V$** is kept for V_{th1} values going from **2.9** to **3.8V** (in DC mode) for the studied thicknesses, with $V_{th2} \approx V_{th}$ values, above mentioned.
- **Reading Current Margin (RM) of 500**, corresponding to the ratio between the I_{ON} (OxRAM in LRS) and I_{OFF} (OxRAM in HRS) read currents, was reached. A **non-linearity factor (NLF) of 600** was obtained for the I_{OFF}/I_{leak} ratio, with the latter taken at $V_{Read}/3$. These values were measured for a 20nm *GSSN* thickness.
- In pulsed mode, RM is kept. The time dependence of the switching events for both OTS and OxRAM devices leads to a shift respect to DC values ($\approx 1V$). **For a GSSN 20nm thickness, $V_{Read} = 4.5V$ in AC mode.**
- **Thermal stability for 20h at 165°C** was also demonstrated and acceptable RM is kept even if V_{th2} drift is observed.
- **Tile size up to 1Gb** for the 25nm *GSSN* thickness was estimated based on I_{leak} metrics. However, IR drop and periphery area considerations seem much more restrictive in terms of bank dimensions, and logically, most aggressive technological nodes, imply smaller array sizes. Multi-bit operation, as well as compensation techniques, should be considered in further studies in order to improve estimations accuracy.

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Reliability and variability of 1S1R OxRAM-OTS for high density Crossbar Integration

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⁽¹⁾This model is a collaboration with Prof. Damien Deleruyelle from the Nanotechnologies Institute (INL) from Lyon

THE last chapter, presented a successful proof of concept for co-integration of a best-in-class $GeSeSbN$ (GSSN) OTS (Ovonic Threshold Switch) selector (1S) and a HfO_2 resistive memory (1R). Through material optimization of the OTS alloy, selector and OxRAM stacks, were demonstrated to be electrically and process compatible. Thanks to remarkable performances, estimations of the applicability of $GSSN + HfO_2$ systems, for large crosspoint arrays, were presented, with expected tile sizes up to 1Gb, based on $I_{leakage}$ metrics, and for the most optimistic scenarios. If compared with some relevant works from literature [1–5] (OTS performances are compared in Table 4.1), it can be appreciated how $GSSN + HfO_2$ systems are a very interesting alternative for array implementations.

Although most of the electrical characterizations presented in chapter 4 were made in DC mode, pulse-mode operation and its respective stability were also studied thanks to the use of a series resistor, in order to limit electrical current flowing through the 1S1R devices. However, its use implies the appearance of unwanted RC effects if short pulses or high series resistance values are employed, causing a temporal delay between the applied pulses and the extracted ones (See Figure 4.18.b.). Besides, parasitic overshoot and slow time constants brought to the 1S1R by the RC effects, are not ideal in terms of power consumption and devices protection. This fact, hinders measurements reliability and increases difficulty for most of pulsed studies. Because of this, and in order to have a most real product approach, CMOS transistors were included in the FEOL of new measurement batches, aiming to optimize current control. Thanks to its use, this chapter presents additional outstanding performances to those obtained in chapter 4. More than 10^6 programming cycles, 10^8 reading and 10^9 read disturb cycles, were measured. Programming current influence over the 1S1R devices is also studied. Conversely, while promising features of 1S1R systems were showed [3, 4], no clear investigation of overall reliability and variability has been demonstrated. In this chapter, a study allowing to quantify the criticality of 1S1R features for high-density developments, is proposed. They are linked to both ReRAM and OTS characteristics and using theoretical estimations, some optimizations and future analysis are suggested. Results are also studied by means of numerical modeling (Metastable Nucleation Filament Model MNFM) and Monte Carlo simulations.

5.1 Technological Details

In the precedent chapter $Ge_{24}Se_{56}Sb_{20}$ with 8% N doping and 15-25nm thicknesses, were identified as the most promising configurations for co-integration with HfO_2 5-10nm ReRAM. For this chapter, OxRAM+OTS 1S1R structures were integrated on memory arrays on top of Metal 4 of a 130nm technology (Figure 5.1.a-b) with 300nm memory cell size. Here, OxRAM stacks are made of a TiN/10nm HfO_2 (ALD)/Ti. Once again, magnetron sputtering without vacuum break in order to avoid surfaces oxidation, was used to deposit the OTS devices. In a GSSN configuration and as explained previously, Sb-doping allows to reduce the operating voltages, while N-doping is used to stabilize the amorphous structure and to keep acceptable leakage levels (see section 4.3 for a more detailed explanation). The picked GSSN thicknesses mentioned above, can favor low

operating voltages (15nm) or high insulating capabilities (25nm). Ti diffusion inside the chalcogenide material is avoided thanks to the use of carbon electrodes around the OTS alloy (2nm thick). Figure 5.1.c and Figure 5.1.d present supplementary TEM and EDX device cross sections, showing a clear separation of the layers composing the 1S1R stack.

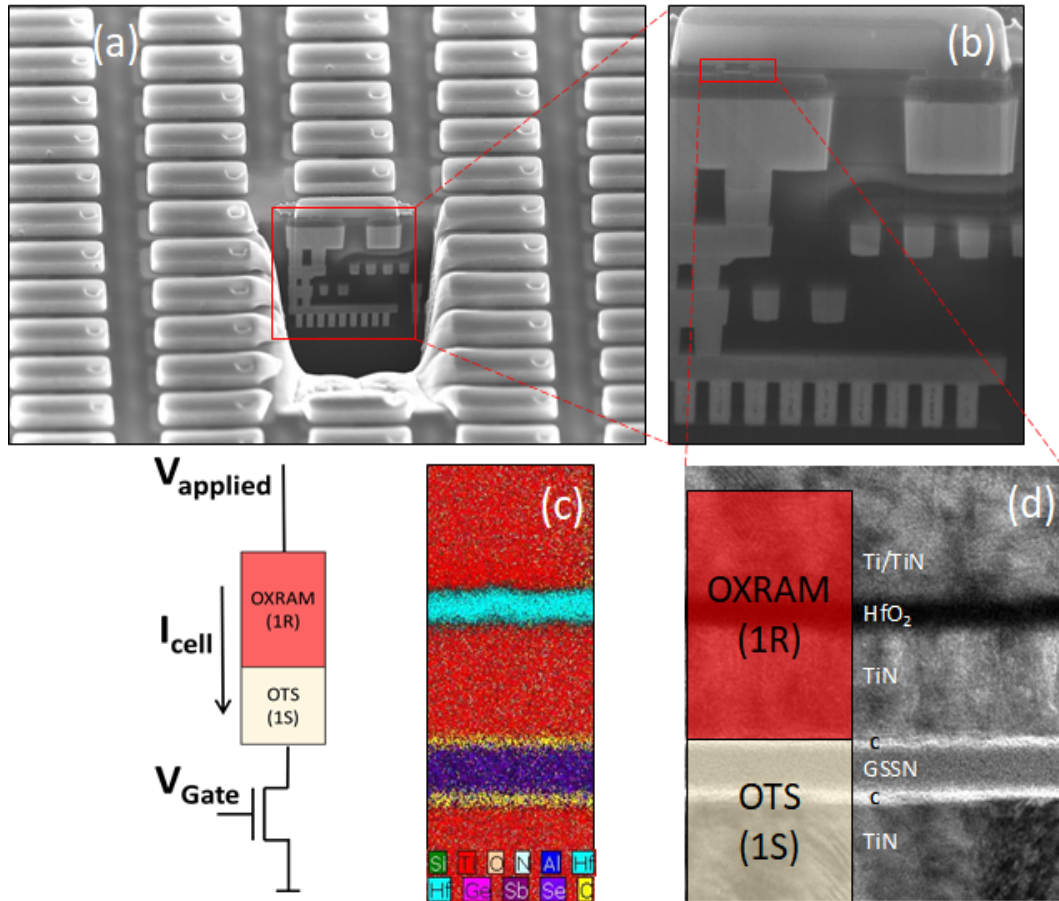


Figure 5.1: (a-b) SEM images of the 1T1S1R system showing the 1S1R stack integrated in M4 on top of FEOL transistor. The gate voltage is manipulated to regulate the current flowing through the 1S1R device. (c-d) EDX and TEM cross sections of the 1S1R stack with HfO₂/Ti OxRAM and GeSeSbN OTS.

5.2 1S1R working mechanism and switching characteristics: short recall

A typical IV behavior for a 1S1R system using a 15nm GSSN thickness is presented in Figure 5.2. The main electrical parameters already identified and explained in detail in chapter 4 for diverse GSSN stoichiometries and thicknesses, are highlighted. Both devices, OTS and OxRAM memory, require an initialization process called forming, $V_{Forming}$. OTS and OxRAM are formed simultaneously at $V_{Forming,OTS}$, which is

higher than $V_{Forming\ ReRAM}$. For the following operations, current and voltage, necessary to switch the selector device from the OFF state into the ON state are named threshold voltage and current (V_{th} and I_{th}), with $V_{th} < V_{Forming}$ and $I_{Forming} < I_{th}$. The minimum voltage and current required to keep the OTS in the ON state are called hold, V_{hold} , I_{hold} , which are normally lower than the threshold ones. In our case, OTS device presents a $V_{th} > V_{SET}, |V_{RESET}|$ of the ReRAM. This implies that both OTS and ReRAM switch simultaneously once V_{th} is reached. Once this happens, the voltage drop over the OxRAM at I_{th} is different as a function of its resistive state, which leads to a $\Delta V_{th} = V_{th1} - V_{th2}$ where V_{th1} and V_{th2} are the threshold voltages corresponding to the OxRAM in HRS and in LRS, respectively. A highly conductive memory in the LRS, leads to $V_{th} \approx V_{th2} \approx |V_{RESET}|$. Besides, ΔV_{th} is used to define the reading voltage which is applied inside this range. Current is limited thanks to the drain-source saturation determined by the applied gate voltage of the CMOS transistor, placed in the FEOL of the memory points as previously stated. *For all the results presented in this chapter, an ordinary compliance current of $100\mu A$ is used.*

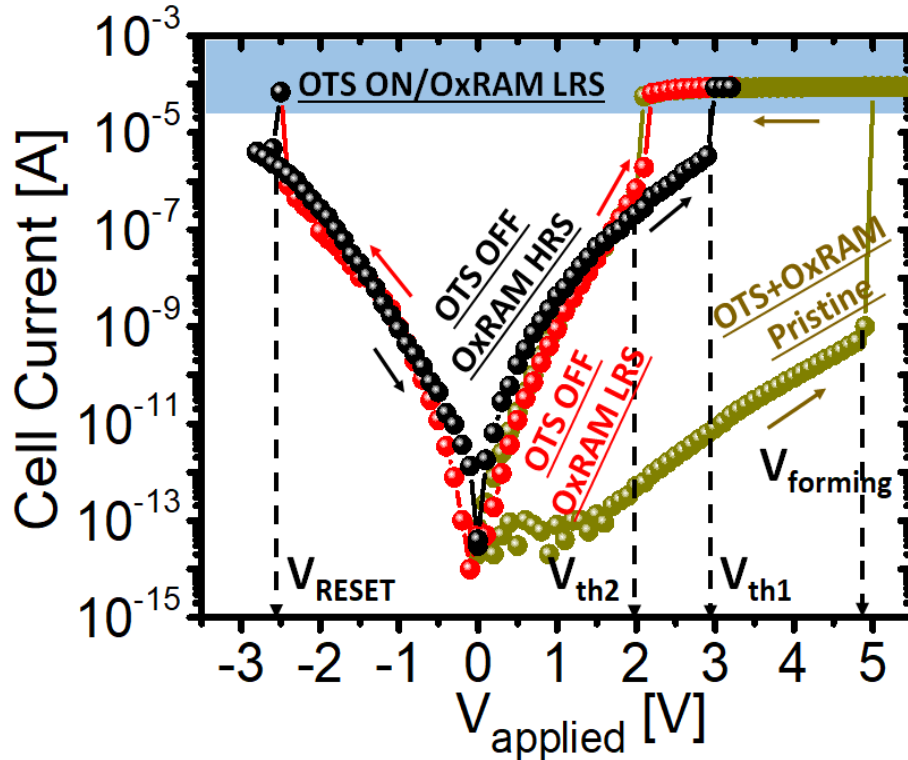


Figure 5.2: Typical IV characteristics of the 1S1R stack (GSSN 15nm) for forming, RESET, and SET operations. Programming current is controlled by a select transistor.

5.3 ON state characteristics of 1S1R systems

As a first study, and taking advantage of the added CMOS transistor, useful to well limit electrical current flowing through the 1S1R systems during the ON state; programming

current dependence was studied. Hence, insights about the voltage drop contributions and programming modes for both OTS and OxRAM, were analyzed. On state resistances were measured for various currents over 1S, 1R and 1S1R structures. In the 1R systems case, pulses with different compliance currents were applied over devices in the HRS. Subsequently, reads at 0.1V were effectuated. On the other hand, and for structures including OTS devices, two different pulse patterns were used and can be consulted in Figure 5.3.a. Results are reported in Figure 5.3.b. Interestingly, OTS and OxRAM, as well as the OTS+OxRAM devices, reach the same resistive level for the same programming currents, independently of the switching layer materials or configurations. Larger is such current, lower is the ON resistance state. The slope of this behavior leads to estimation of a constant voltage $R_{ON\ State} \cdot I_{prog} = V_{ON\ State} \approx 1.4V$, which corresponds to the ON state voltage drop over the tested structures. Such $V_{ON\ State}$, seems to be independent of the pulse amplitude or the programming current. In the case of ReRAM devices, similar results for 1R structures, without using transistors as current limiters, have been found in [6, 7]. Hence, independence of this observation regardless of the compliance method used during the SET process, can be confirmed.

Operating voltages area independence, as well as the universal $R_{ON}(I_{prog})$ behavior, have been widely linked to the filamentary characteristic of the high conductive state and its corresponding nucleation, growth and stabilization; for most of ReRAM technologies [8, 9]. According to these, $V_{ON\ State}$, is the consequence of a filamentary size reached at the end of the set transition and once current density stabilizes. Hence, results presented before, its interpretation, and some of the arguments presented in subsection 4.1.1 lead to think about a filamentary-like mechanism for OTS devices in the ON-state. However, a lot of tests, discussions and simulations need to be done in order to fully confirm this hypothesis, notably thickness and stack variations for the measurements undertaken in Figure 5.3.b. While for bipolar ReRAM, ion migration of oxygen vacancies or cations for OxRAM and CBRAM respectively, through thermally activated hopping; are responsible for the formation and dissolution of the conductive filament, in the OTS materials case, filamentary-like characteristic seems to be determined by a localized change of the bonding structures, that lead to metastable crystallization as treated in subsection 4.1.1.

If the filamentary characteristic of the high conductive state for OTS devices is finally confirmed, its understanding could lead to a more efficient programming process, optimization of the resistive programming window, variability reduction, and therefore, reliability improvements of the 1S1R devices.

Results obtained in Figure 5.3.b, indicate that, for the ON state, and in the case of 1S1R structures, the most resistive element undergoes higher voltage drop. One could affirm that, with current flowing through it, resistivity tends to decrease until it equalizes or becomes lower than that one of the other element. This process could take some transition time, until a specific current density is reached, with most resistive element being alternated, prior to stabilization over the same resistance level for both devices, when voltage drop is shared. A graphic example of this theory is presented in Figure 5.4.

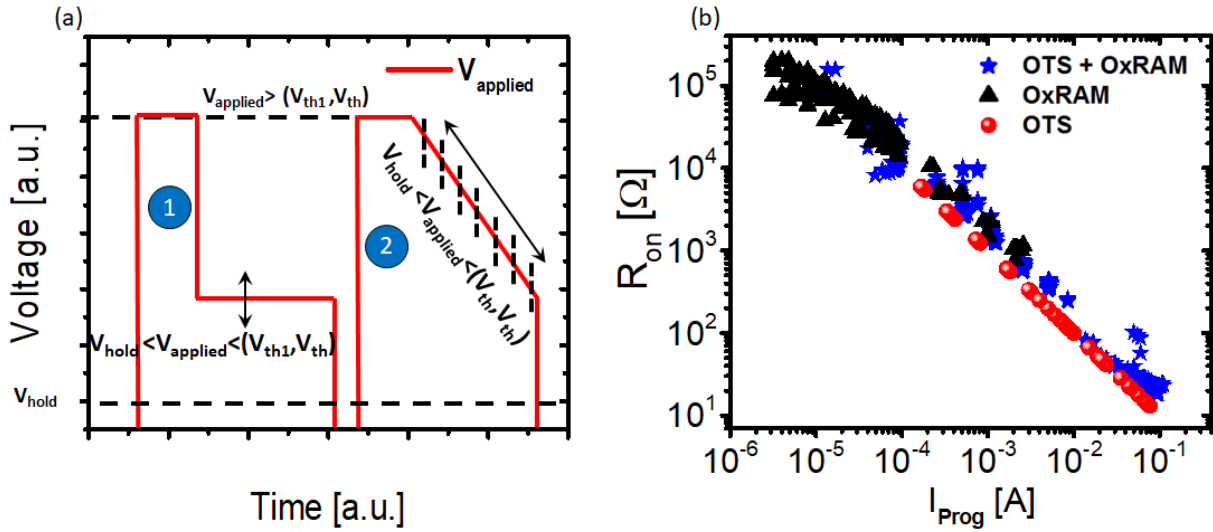


Figure 5.3: (a). Two pulse patterns are employed to study the ON state behavior of 1S and 1S1R structures. A $V_{\text{applied}} > (V_{\text{th1}}, V_{\text{th}})$ is used first for a short length, to force the OTS to go into the ON state. Then, various voltage levels (pattern 1) or pulses with slow decreasing rates (pattern 2), where $V_{\text{hold}} < V_{\text{applied}} < (V_{\text{th1}}, V_{\text{th}})$, are applied. Hence, ON resistance values for diverse programming currents are extracted. Results are presented in (b) for a 15nm *GSSN* and a 10nm *HfO₂*. OTS, OxRAM and OTS+OxRAM present the same behavior, with ON state resistance values interestingly superposing.

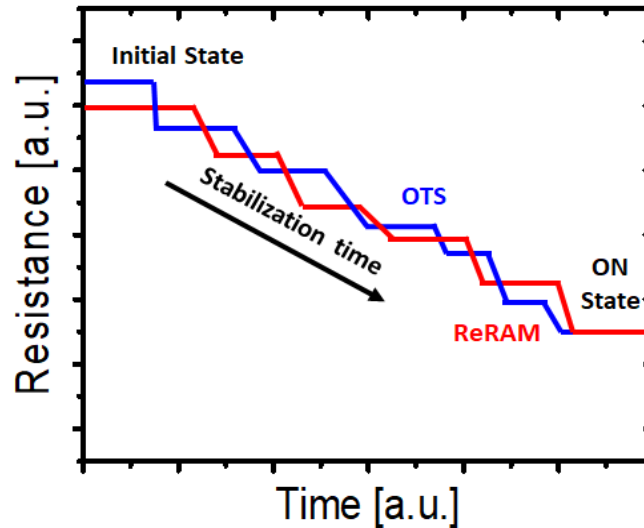


Figure 5.4: Possible explanation for the resistance evolution of OTS and OxRAM devices for the ON state and prior to stabilization, where same resistive levels are reached.

5.4 Device performances and reliability studies

With the addition of a FEOL transistor in order to control programming currents once OTS switches into the ON state, performances and reliability studies could be conducted

over 1S1R devices. The objective is to link them to the main directives necessary to properly design crosspoint arrays.

According to the electrical measurements undertaken in the precedent chapter of this work, the most convenient reading strategy was defined (see subsection 4.4.3). In there, the V_{th} shift is profited to elucidate the reading voltage range as follows:

$$V_{th2} < V_{Read} < V_{th1} \quad (5.1)$$

With V_{th2} and V_{th1} being the threshold switching values corresponding to the ReRAM in LRS and in HRS, respectively, as already depicted in Figure 5.2.

For this reading scheme, commonly known as ΔV_{th} [10–12], we have identified three key features, presented in Figure 5.5: (1) current margin at V_{Read} , also called window Margin (WM); (2) selectivity and (3) reading voltage margin (RM). In the next, each one of them is explained, quantified and studied since a statistical point of view, using 15 and 25nm *GSSN* thicknesses co-integrated with 10nm *HfO₂* stacks. Additionally, aspects affecting them are also highlighted.

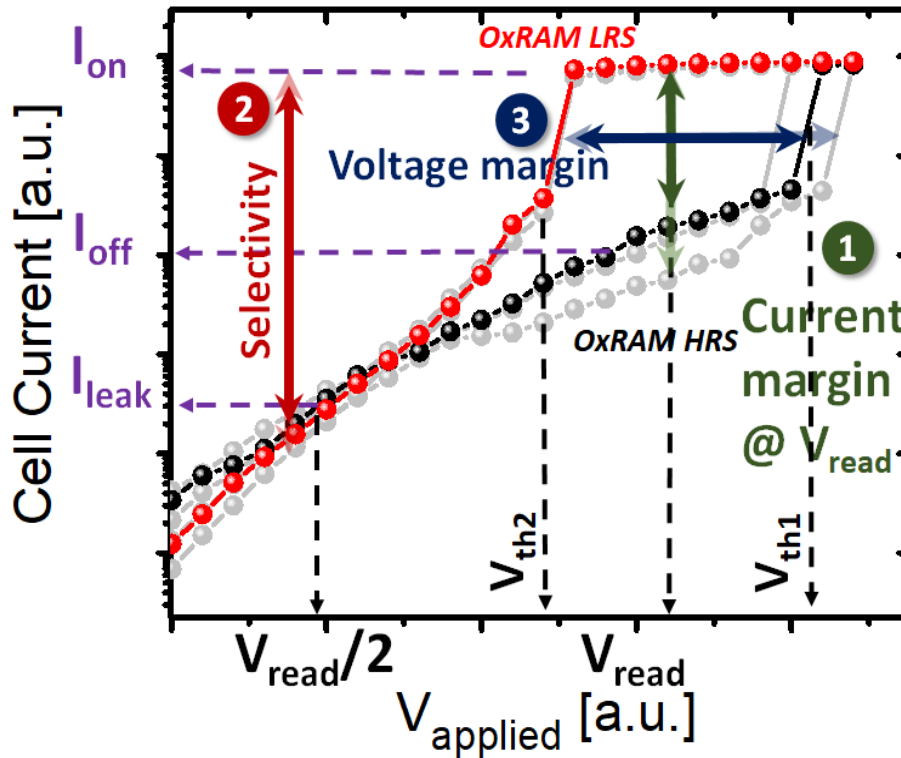


Figure 5.5: Representation of the three key features investigated in this work: current margin at V_{Read} (I_{ON}/I_{OFF}), selectivity (I_{ON}/I_{leak}), and voltage reading margin RM, $\Delta V_{th} = V_{th1} - V_{th2}$

5.4.1 Current Margin at V_{Read}

In a ΔV_{th} reading scheme, traditional HRS and LRS states obtained for 1R structures are transformed into $R_{OTS\ OFF} + R_{ReRAM\ HRS}$ and $R_{ReRAM\ LRS}$ resistance values, respectively. This implies different currents obtained for read operations named I_{ON} and I_{OFF} here (Figure 5.5). Given that, for the read voltage, OTS is switched into the ON state if the OxRAM is in LRS, with I_{ON} being equal to the compliance current. On the other hand, I_{OFF} is highly dependent of the OTS stack and the OxRAM technology characteristics. In the case of $GSSN + HfO_2$ systems, $R_{OTS\ OFF}$ at V_{Read} is much more higher than the HRS value of the OxRAM. Consequently, $I_{OFF} \approx I_{OTS\ OFF}$ at the applied read voltage.

The ratio between I_{ON} and I_{OFF} is referred as the current margin at V_{Read} . Reading cycling operations for devices programmed in the ON and OFF states were effectuated for both 15 and 25nm GSSN thicknesses and the results are reported in Figure 5.6.a. It can be observed how this margin ranges between 2 and 3 decades. Additionally, it is kept for more than 10^8 read disturb cycles. It must be mentioned that, for this case, OxRAM devices are not switched. Only successive reading operations are performed. Moreover, Figure 5.6.b, presents distributions for several devices of both current values, confirming the high stability of the current margin at V_{Read} for the GSSN thicknesses considered.

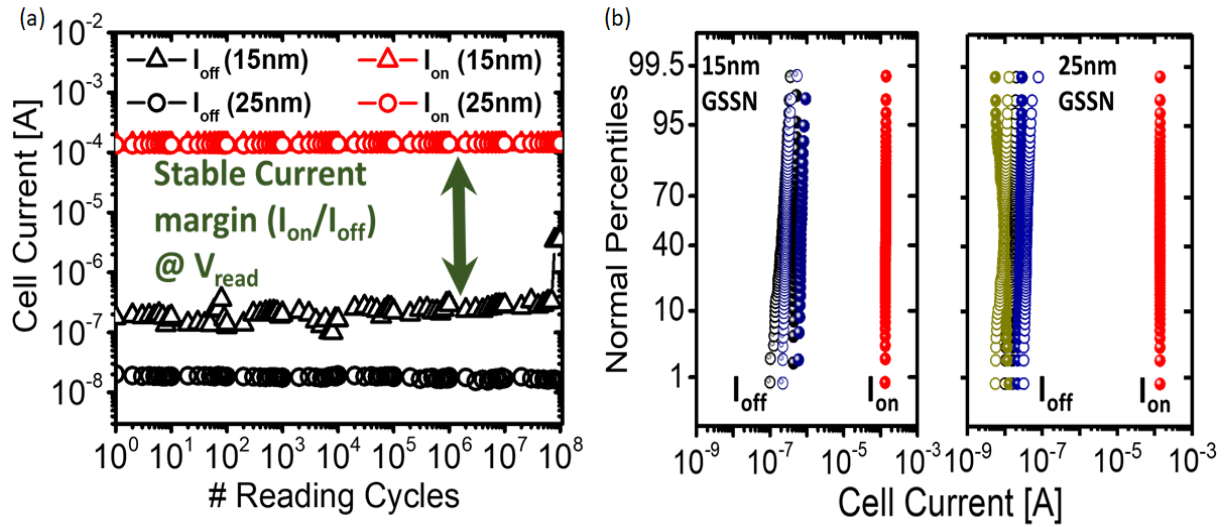


Figure 5.6: (a). Read disturb cycles over 1S1R structures for both 15 and 25nm GSSN thicknesses without memory switching. According to the reading strategy used, 1S device only switches for the devices programmed in the LRS. (b). I_{ON} and I_{OFF} distribution for both GSSN thicknesses tested in (a).

5.4.2 Selectivity

The second key parameter to take into account in order to have reliable crosspoint systems, is the selectivity of the 1S1R devices. Directly linked to the non-linearity of the OTS elements, it is defined as the I_{ON}/I_{leak} ratio with I_{leak} being the current at $V/2$ or $V/3$

depending on the bias scheme chosen to operate the crosspoint array. At this point, it is important to recall that bias schemes were treated in subsection 4.5.1 as well as the array estimation, based on I_{leak} measurements (subsection 4.5.2). Up to 1Gb sizes were obtained using this metric. However, criteria such like IR drop and periphery size need to be taken into account too (subsection 4.5.3). As a consequence, and under this scenario, bank size seems more limited by technological nodes constraints than by the non-linearity of the individual 1S1R structures.

To study selectivity, Figure 5.7.a, presents I_{ON} reference, as well as I_{OFF} and I_{leak} distributions at V_{Read} for 15 and 25nm GSSN. It can be observed how selectivity is in the order of 5 and 6 decades respectively if measured for the median values. Analogically to studies undertaken for the reading current margin at V_{Read} , Figure 5.7.b, presents read disturb cycles over several 1S1R devices with a 15nm GSSN for both I_{OFF} and I_{leak} . It can be concluded that the margin is acceptably kept for more than 10^9 read disturb cycles.

In the case of $GSSN + HfO_2$ structures, selectivity is fully dependent on the OTS electrical behavior and the compliance current chosen for the 1S1R system. More insulating OTS devices with higher NL, will imply larger projected crosspoint arrays. However, and as observed during characterization for OTS optimization in section 4.3, lower I_{leak} could lead to higher V_{th} values. This trade-off could imply more energy consumption for reading or writing operations. Furthermore, I_{leak} variability needs to be taken into account in further studies, at the moment of estimating maximum array sizes.

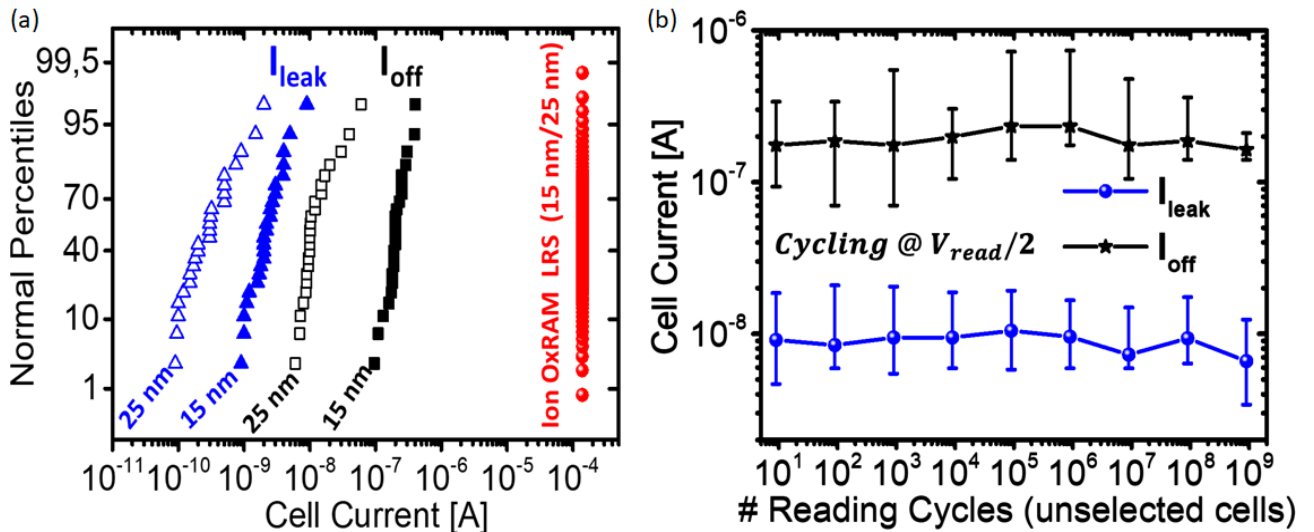


Figure 5.7: (a). I_{ON} , I_{OFF} and I_{leak} (for a $V/2$ bias scheme) distributions for both GSSN thicknesses used in this chapter. (b). Evolution of both I_{OFF} (HRS devices) and I_{leak} for V_{Read} and $V_{Read}/2$ Error bars correspond to 6 devices tested for the 15nm GSSN thickness.

5.4.3 Voltage Reading Margin (RM)

ReRAM cycling reliability has been widely studied in literature [13–16]. For instance, chapter 3 presented experimental and theoretical evidence over diverse stacks and pro-

programming conditions in order to optimize such behavior at the array level. On the other hand, and for the time being, this capital characteristic of memory technologies, has been barely studied for OTS+ReRAM devices. To our knowledge, only Yasuda *et al.* demonstrated 10^7 endurance cycles over their Boron Carbon based selector co-integrated with a $CuTe_x$ CBRAM. Additional measurements have been presented over 1S1R devices [3, 17]. However, different selector or emerging memory topologies used, make comparisons, less valid, notably because switching mechanisms of both selector and memory are based on different physical phenomena.

Additionally to the aforementioned reasons, Reading Margin (RM) and the applied V_{Read} , have a direct influence over the switching behavior and the read values of $GSSN + HfO_2$ structures. Because all of that, endurance tests over 1S1R systems need to be conducted. Results are shown in Figure 5.8.a. More than $5 \cdot 10^6$ endurance cycles are demonstrated with up to 3 decades of margin between I_{ON} and I_{OFF} for a 15nm GSSN. Some punctual reading failures appear when the read OxRAM memory state is different from the programmed one. Consequently, these failures need to be deeper studied. A first test consisted in extracting the IV characteristic over devices who had experimented endurance cycling, to analyze RM changes. An example is presented in Figure 5.8.b. There, threshold switching feature before and after 10^6 endurance stress cycles is reported. Both V_{th1} and V_{th2} suffer from voltage drift. Interestingly, and even if such values are drifted, a $RM \approx 1V$ is kept. This drift, different to that one treated in subsection 4.4.1, which was produced by temperature stress; could be linked to evolution of the resistance values programmed over the memory, as it will be observed in further sections.

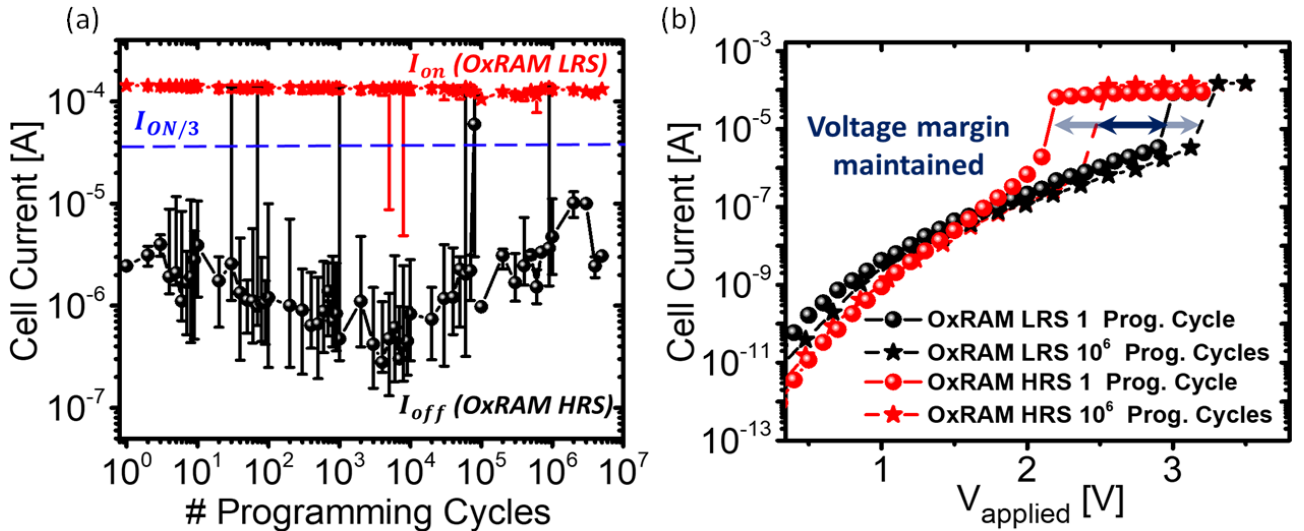


Figure 5.8: (a). Endurance characteristics of 30 1S1R structures (15nm GSSN). $t_{pulse} = 1\mu s$. Current is read at $V_{Read} = 3.4V$ in transient mode. (b). IV DC characteristic for 1S1R systems before and after endurance stress. A shift over the V_{th1} and V_{th2} events is observed, while keeping $\Delta V_{th} = V_{th1} - V_2$.

Once reading failures during cycling were identified, next step consisted in the investigation of their origin. To do so, cycle to cycle and device to device evolution of the

threshold switching values was studied. In a first stage, pulsed setup, previously presented in subsection 2.3.2.a, was used in order to follow V_{th1} and V_{th2} behavior during cycling. Figure 5.9.a reports evolution of the median value for each one of them over 30 cycles, and for 30 devices. Conversely, Figure 5.9.b shows the failure probability rate for the example from Figure 5.9.a. A very low rate is obtained for voltages around 3.3-3.4V showing again, the importance of a careful choice of V_{Read} .

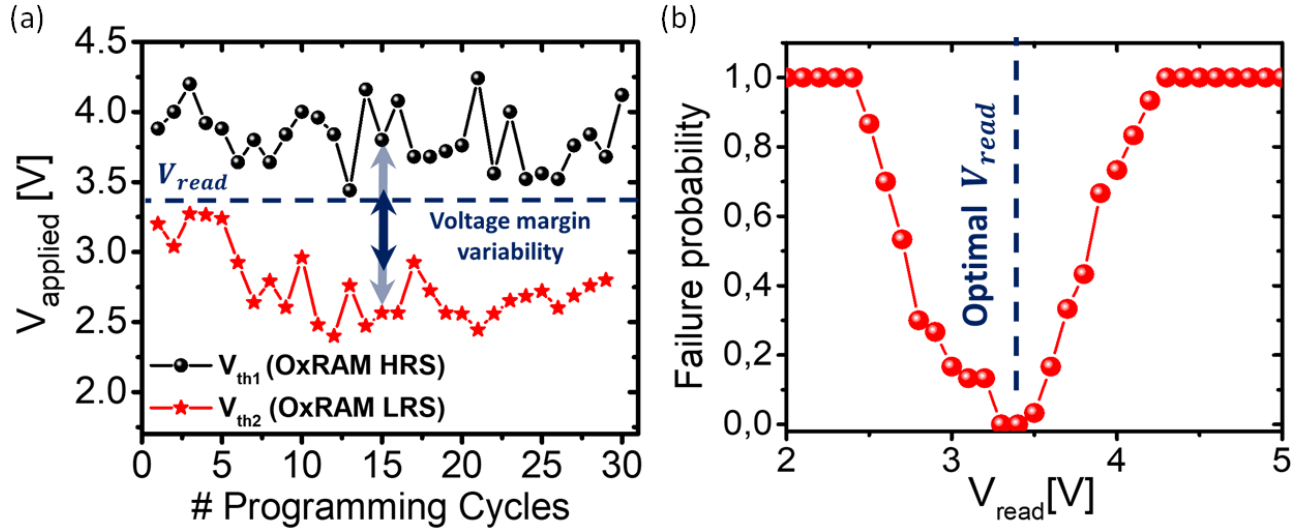


Figure 5.9: (a). V_{th1} and V_{th2} measured on SET RESET cycles on 30 1S1R cells (15 nm GSSN). (b). Probability to read a 1S1R cell in the good state depending on the reading voltage. Adjusting V_{Read} optimizes read yield.

As for the device to device distributions, V_{th1} and V_{th2} were extracted for devices previously programmed. Staircase procedures were used, in order to increase measurements reliability, given that more accurate values are obtained. A train of positive pulses was employed for V_{th1} while negative ones were applied in order to get V_{th2} values. Results are shown in Figure 5.10, with distributions for the threshold switching voltages for both 15 and 25nm GSSN. It can be observed how V_{th1} is more dispersed than V_{th2} for both thicknesses. Moreover, Figure 5.11.a depicts V_{th1} distributions for both studied thicknesses. Previous trends and selector thickness independence of such dispersions are confirmed. Higher median values if compared with those ones reported in Figure 5.10 are caused by pulse characterization with faster rising times. On the other hand, Figure 5.11.b compares V_{th1} values for a 25nm GSSN for device to device (D2D) and cycle to cycle (C2C) distributions. Same slope, leads to conclude, a priori, degradation independence of the V_{th1} dispersions.

As a conclusion for this section, all the previous results, highlight Voltage Reading Margin (RM) as the most critical feature of 1S1R systems for a ΔV_{th} reading strategy. Voltage drift caused by cycling degradation and reading failures as a consequence of V_{th1} and V_{th2} values variability, demonstrate the importance of a careful choice of V_{Read} inside ΔV_{th} range, in order to increase systems reliability. Threshold switching values variability, seems to be independent of the OTS thickness or 1S1R devices degradation.

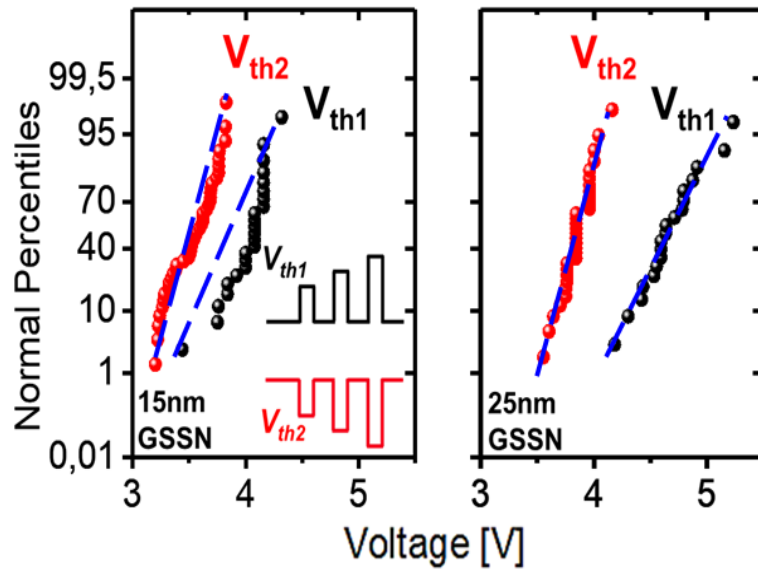


Figure 5.10: V_{th1} and V_{th2} distributions of 1S1R cells before aging for 15 and 25nm GSSN thickness. Staircase pulses are used in order to increase accuracy of the extracted values in pulsed mode given the time dependency of this phenomenon. Dashed blue lines allow to identify a larger slope for the V_{th1} distribution, linked to a larger dispersion in both cases, showing OTS thickness independence and leading to suppose OxRAM memory as responsible of this observation.

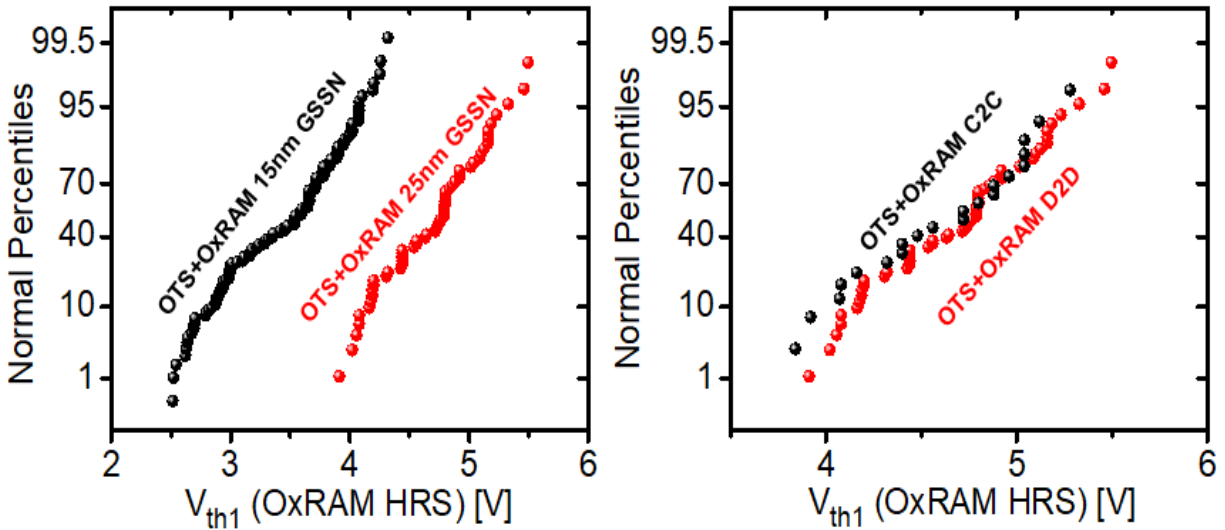


Figure 5.11: (a). V_{th1} distributions of 1S1R cells for 15nm and 25nm GSSN thickness. (b). V_{th1} Device to Device (D2D) vs Cycle to Cycle (C2C) distributions of 1S1R cells for 25nm GSSN. Degradation and thickness independence are confirmed.

This leads to suppose the OxRAM memory as the main responsible. That is why, in the following, programming resistive states of the ReRAM will be estimated and obtained through modeling. Thanks to them, optimization guidelines will be proposed.

Finally, and as a future perspective, threshold switching voltages and its evolution with cycling as a function of a big variety of programming conditions or 1S1R stacks, could be studied in order to decrease reading failures and to improve 1S1R cycling endurance.

5.5 Simulations and Discussion

5.5.1 Influence of OxRAM variability over 1S1R performances and device optimizations

In the case of $GSSN + HfO_2$ structures, applied V_{Read} gives two current values as a function of the OxRAM resistive state, $I_{ON} \approx I_{compliance}$ (OxRAM in LRS) and I_{OFF} (OxRAM in HRS), which, and given the electrical characteristics of $GSSN$ and HfO_2 devices, is equal to the current flowing through the OTS device in the OFF state at V_{Read} . The consequence of this is that the classical current values obtained from 1R configurations using low magnitude pulses (i.e. $V_{Read\ 1R} = 0.1V$), are not reachable anymore. That is why, alternative methods to know the resistance values of the LRS and the HRS states, are necessary. A first one, was proposed in subsection 4.4.5. There, OxRAM stack was characterized using a range of pulses amplitudes in order to know the resistive window evolution with $V_{applied}$ (Figure 4.17.a). The largest voltage margin, obtained for 1S1R systems with 20nm $GSSN$ thickness (Figure 4.16), was linked to an optimized window margin of the OxRAM device with ΔV_{th} being the voltage drop required to set the OxRAM in HRS once the OTS goes into the ON state. Additionally, the previous section demonstrated how the voltage reading margin (RM) was the most critical feature in terms of variability and reliability. Results in subsection 5.4.3 showed a higher dispersion for V_{th1} regardless of the selector thickness or the 1S1R degradation. Consequently, V_{th1} distribution could be correlated to the intrinsic HRS resistance variability of OxRAM memories. As a first step to corroborate this hypothesis, a Poole-Frenkel regime was used to determine the influence of the HRS values over the switching values of OTS+ReRAM systems assuming this conduction model for the OFF state of both devices [18–22]. In there, electrical conduction is defined through a current density equation, as follows:

$$J = \sigma_0 \cdot E \cdot \exp\left(\frac{-E_a}{K_b T}\right) \cdot \exp\left(\beta \cdot \sqrt{E}\right) \quad (5.2)$$

with σ_0 being the zero-field conductivity, E the electric field, E_a the activation barrier, K_b the Boltzmann constant, T the absolute temperature, and β a fitting parameter also known as the Poole-Frenkel parameter and expressed in $\sqrt{\frac{m}{V}}$ [23].

Figure 5.12.a presents a typical current voltage characteristic for a 10nm HfO_2 based ReRAM. Ohmic conduction is inherent to the LRS, while Poole-Frenkel model is to the HRS. Resistance values depicted, correspond to the current at $V = 0.1V$. If the same conduction regimes are used for an OTS+OxRAM structure, HRS resistance values can be deduced. In the example used in Figure 5.12.b, in order to have a $\Delta V_{th} = 0.6V$, a HRS around 750 $k\Omega$ will be necessary. In more detail, if a ReRAM in LRS with a typical

value of $12\text{ k}\Omega$ is assumed for the IV characteristic that leads to V_{th2} , the combination of the dark blue curve, corresponding to such LRS value, and the dashed violet curve (ReRAM in HRS), gives the purple solid line, which superposes to the IV characteristic of a $GSSN+HfO_2$ with the OxRAM in HRS. The obtained resistance values, are compatible with HfO_2/Ti window margin characteristics (Figure 4.17.a).

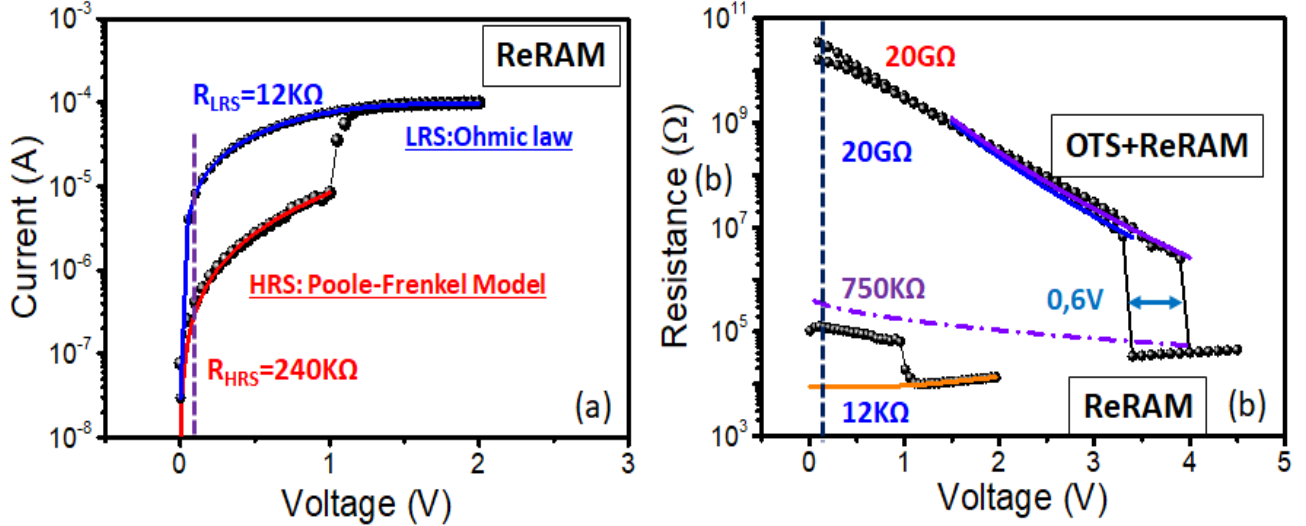


Figure 5.12: (a). IV characteristic example with the resistance values at $V=0.1\text{ V}$ indicated. An ohmic conduction is characteristic of the LRS, while a Poole-Frenkel regime is used for the HRS. (b). Using the latter for the OTS in the sub-threshold regime as well, allows to appreciate the influence of the programming state of the OxRAM memory over the V_{th1} value, essential for the ΔV_{th} reading strategy employed in this work. The IV characteristic corresponds to a $GSSN + HfO_2$ system with 20 nm selector thickness.

These estimations confirm that V_{th1} higher distribution slope is caused by the OxRAM in the HRS state, which is intrinsically more dispersed than the LRS (see chapter 3). Besides, OxRAM in LRS is highly conductive for voltages around the OTS V_{th} ones. It means that for the LRS, V_{th2} dispersion is almost exclusively dependent on the OTS intrinsic variability, while V_{th1} distribution is affected by both OTS and OxRAM in HRS state.

To quantify how HRS dispersion affects V_{th1} distribution, Poole-Frenkel curves for a typical HRS 10 nm HfO_2 distribution were estimated. Current values obtained at $V_{Read} = 0.1\text{ V}$ for 1T1R structures, are extrapolated for higher voltages. Then, voltage drops at I_{th} (median value for a given GSSN thickness) for the various HRS IV characteristics, can be deduced, as presented in Figure 5.13. Hence, the voltage drop distribution, can be added to median V_{th2} , to see its influence over V_{th1} dispersion (Figure 5.14.a). It is observed how a variation of 1 decade in the HRS value can generate a change of 1 V in the 1S1R RM. For this case, 1 decade corresponds to 2σ in the resistance dispersion. Subsequently, using the same V_{th2} median value, an identical procedure was made for various ReRAM distributions inherent to different ReRAM technologies. Result is shown in Figure 5.14.b, where HRS distribution is translated into V_{th1} dispersion. As expected, higher Window

Margin values increase 1S1R RM. More than 2V of ΔV_{th} , can be reached for hybrid HfO_2/Cu stacks. A first optimization guideline will be the use of ReRAM technologies that present higher HRS values in order to increase the RM and to reduce reading failures in OTS+ReRAM systems. However, it will be necessary to take into account the very well known trade-offs that this emerging memory technologies present [24]. Higher HRS values could lead to a reduction of retention or endurance performances.

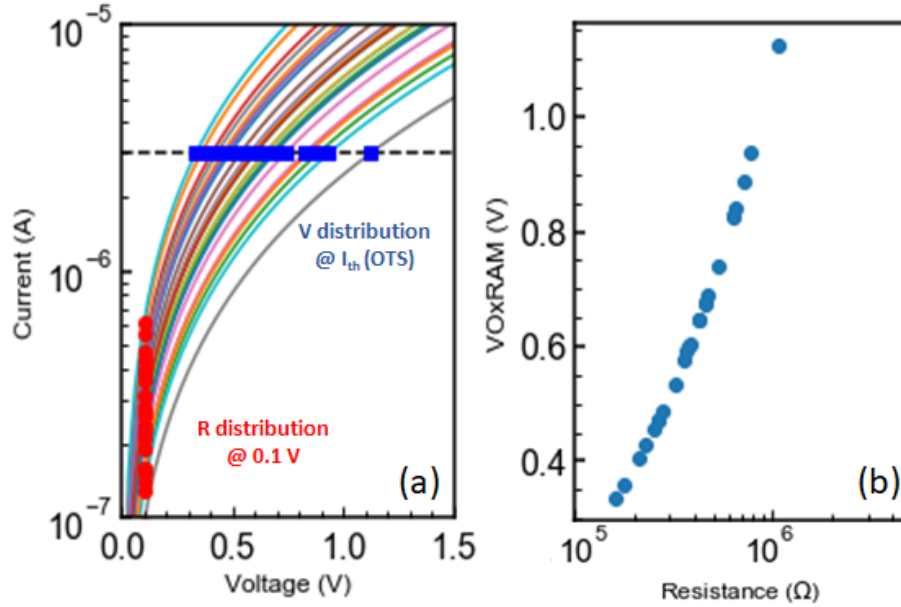


Figure 5.13: (a).IV characteristic for a HRS distribution using a HfO_2 10nm stack. Current values at 0.1V are extrapolated thanks to a Poole-Frenkel conduction regime to higher voltages. (b). Extrapolated voltage values at I_{th} median value (15nm GSSN) for the IV distribution from (a). The voltage dispersion is used to determine V_{th1} distribution based on a V_{th2} median value.

With the influence of the OxRAM HRS over the reading margin clarified, next step consisted in studying OTS influence over this same metric, previously identified as critical for the 1S1R performances. In a first stage, $V_{th1}(V_{th2})$ for the diverse GSSN thicknesses used in this study, was graphed, and voltage drop as a product of various resistance levels for every V_{th2} median values was included. Hence, the HRS resistances (read at $V = 0.1V$ for a 1R 10nm HfO_2 in DC mode), programmed by each selector thickness, can be more or less estimated as presented in Figure 5.15. Naturally, a bell shape for RM and HRS quantities is appreciated. The optimal RM obtained for a 20nm GSSN, is the product of a HRS value around $650k\Omega$ (dashed line corresponding to such value intersects the median one of that GSSN thickness). At this point, it must be recalled that thicker OTS devices, present lower $I_{leakage}$ currents, allowing implementation of larger crosspoint arrays. Conversely, the switching voltages are increased. The latter, could induce performances degradations of the resistive memory as well as power consumption increase, because of the higher operating voltages. As in the case of OxRAM stack influence over RM studies, some trade-offs need to be taken into account at the moment of choosing the OTS to be co-integrated.

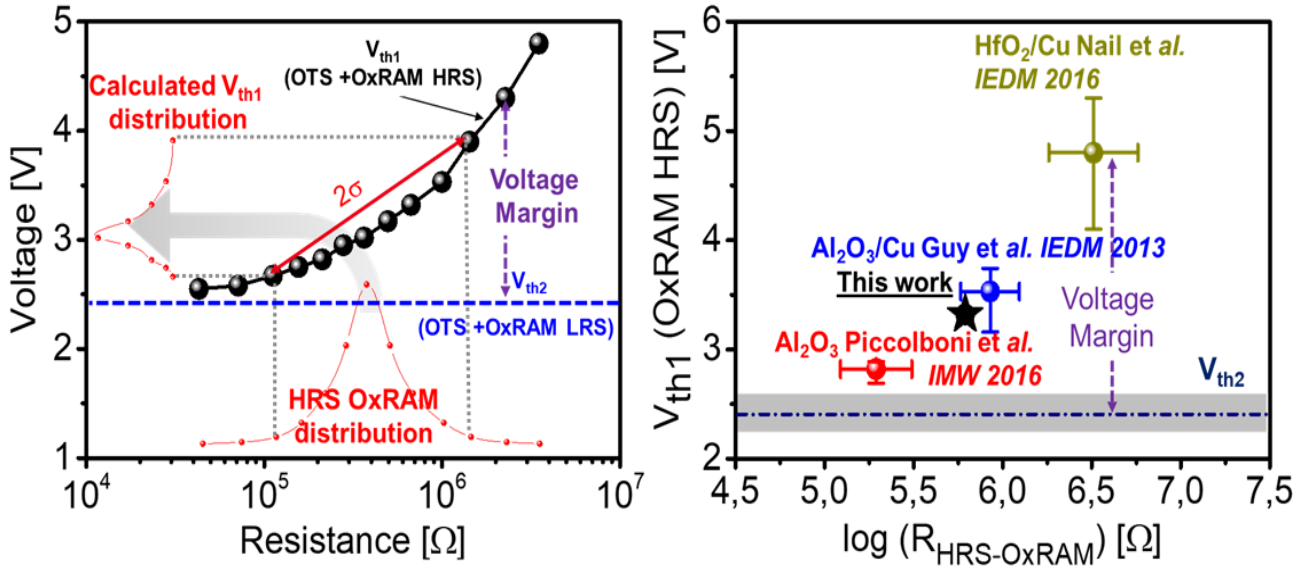


Figure 5.14: (a). Calculated V_{th1} (15nm GSSN) versus OxRAM RHRS. V_{th1} distribution (left) is calculated for each measured R_{HRS} value (down). HRS variability [25] leads to V_{th1} dispersion, reducing the voltage reading margin of 1S1R devices. (b). Impact of OxRAM R_{HRS} mean value and dispersion for various HRS dispersion for various CEA-Leti technologies [24, 26, 27], on V_{th1} value and dispersion. Analogically to (a). V_{th1} is calculated based on the voltage drop over the ReRAM once OTS goes into the ON state.

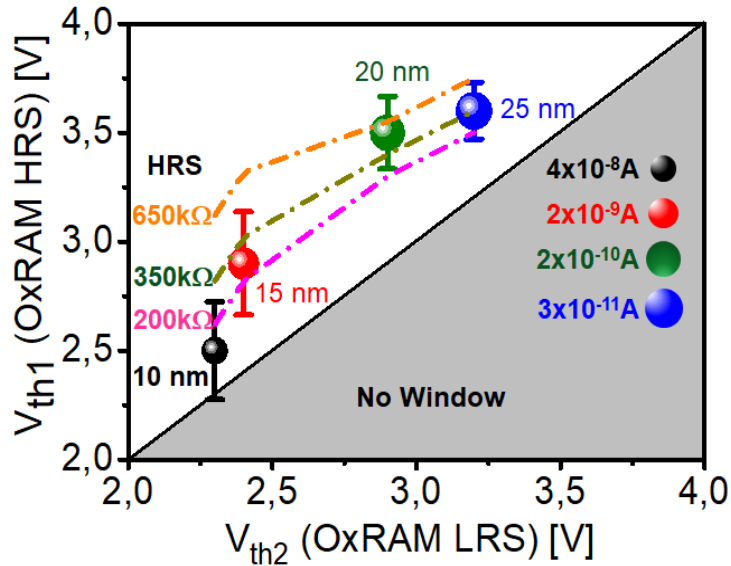


Figure 5.15: Measured V_{th1} and V_{th2} for various GSSN thicknesses. The size of the symbols represents $I_{leakage}$ values, indicated to the right. Dashed lines: calculated V_{th1} for various OxRAM RHRS allowing to estimate R_{HRS} in all cases. Acceptable voltage margin $\Delta V_{th} = V_{th1} - V_{th2}$ is achieved for sufficient R_{HRS} .

5.5.2 Semi-analytical statistical analysis of 1S1R threshold switching based on Metastable Nucleation Filament Model (MNFM) theory ⁽²⁾

Since the first proposition for the use of chalcogenide materials in electronic devices [28], the switching voltage phenomenon has been one of the milestones on the understanding of such technologies. Its importance resides in the fact that it determines the operating voltage and the speed of the system, which makes it essential in order to choose the right selector for a specific memory application. Diverse physical explanations have been developed making of it a large subject of debate nowadays. Among the various mechanisms proposed, thermal-assisted switching [29], carrier generation by impact ionization [30–32], polaron instabilities [33], and the very recent, metavalent bonding creation assisted by electric fields [34, 35]; can be accounted.

One of the most praised models was developed by Ielmini *et al.* [36, 37]. There, conduction in chalcogenide devices is the consequence of carrier hopping and tunneling into higher energy trap states. Once these traps are filled, current rises until switch occurs due to mobility increase. It means that current density is calculated as a function of energy bands distribution through the chalcogenide thickness, which implies that the electric field is non-uniform in the switching layer. According to this model, threshold voltage is a merely electronic phenomenon [37]. However, and although several approaches have assumed either electrical or thermal theories, it is difficult to separate these mechanisms [38]. There is a general agreement to classify threshold switching as an "electrothermal" phenomenon, where either thermal or electronic processes as well as all the intermediate cases can happen inside the chalcogenide materials and have direct influence over the switching voltage [30]. Most of the models previously mentioned, can be classified into such intermediate cases. Insufficient experimental evidence to disprove the wrong approaches and the interplay of different conduction mechanisms and phenomena, clearly lead to this variety of proposed solutions and actual discussions [39].

An additional and important aspect of the switching voltage study, is the explanation given to the appearance of a Negative Differential Resistance (NDR), which is observed once the device switches from the OFF state into the ON state as shown in Figure 5.16. NDR implies a voltage drop reduction over the chalcogenide based device once the conductive phase is reached. It is fundamental on the study of band distribution and the transport mechanisms of chalcogenide semiconductors [36]. Therefore, using the right equations to fit this behavior constitutes one of the most important points of the diverse models found in literature.

Another very well known approach, was proposed by Karpov *et al* [41] and it is based on the field induced nucleation and growth theory. It consists in the formation of a crystal nucleus inside a bigger amorphous volume. Once a first nucleus appears, the crystalline phase tends to grow. The main consequence of this phenomenon is the free energy increase, which reduces the nucleation barrier. Additionally, the formation of such

⁽²⁾This model is a collaboration with Prof. Damien Deleruyelle from the Nanotechnologies Institute (INL) from Lyon

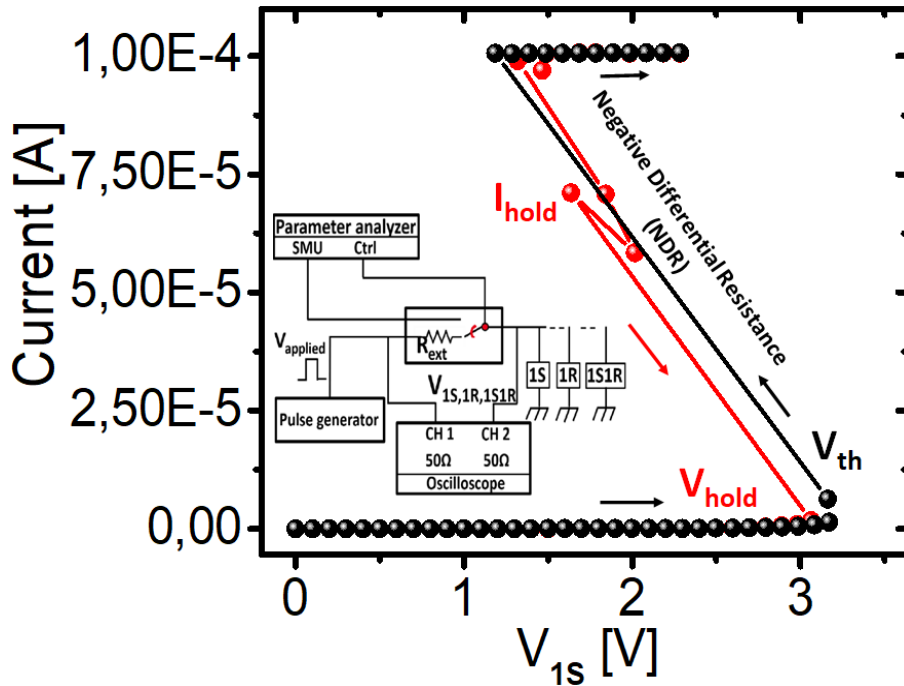


Figure 5.16: Typical OTS IV characteristic. In this case, the presented voltage corresponds to that one measured over the device V_{1S} (GSSN 25 nm). The setup used is depicted on the figure inset [40]. Switching is achieved once V_{1S} exceeds V_{th} . This transition implies the apparition of a Negative Differential Resistance (NDR) of the selector device. This is one of the key points for the theoretical comprehension of the switching phenomenon in chalcogenide based electronic devices.

crystalline nucleus implies the creation of a continuous interface. To better understand this phenomenon, nucleation and growth hypothesis is visualized in amorphous materials using laser beams and an example of this is depicted in Figure 5.17 [42].



Figure 5.17: Amorphous bit (black) with a crystal nucleus (gray) progressively growing (from left to right) due to a laser beam that increases temperature inside the amorphous bit. Due to crystal growth, the amorphous bit becomes almost completely crystallized. Nevertheless polycrystallinity is observed, caused by the different orientations of the crystalline nuclei. Taken from: [42]

Nucleation and growth was originally formulated as a likely hypothesis to explain switching by Stanford Ovshinsky in his seminal work [28]. Since then, nucleation in chalcogenide materials has been widely studied [43–48]. The simplicity of this approach, its electro-thermal character and recent works [49, 50] that seem to confirm the existence

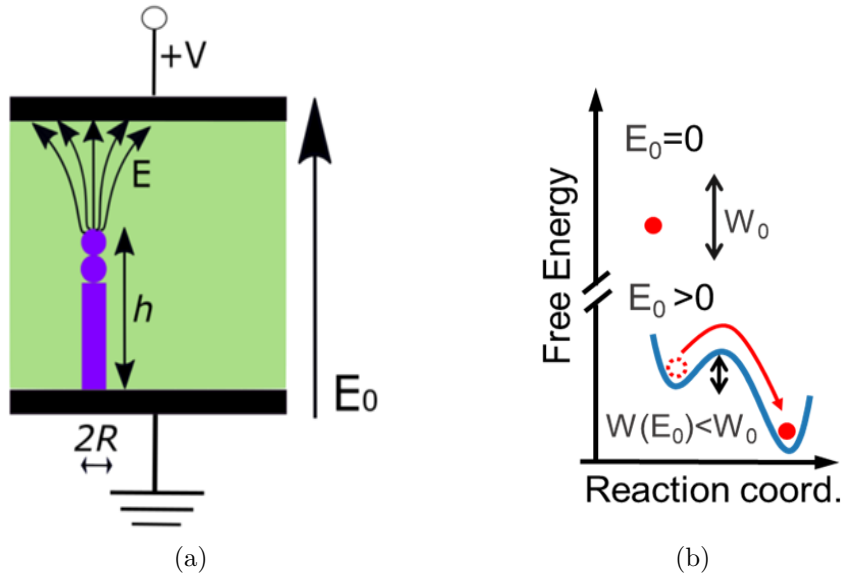


Figure 5.18: Schematic view of the semi-analytical model using a field induced nucleation theory. The model assumes that nucleation occurs upon the nucleation of successive metastable domains through the chalcogenide material. (a). The process begins with the appearing of a lightning rod like cylinder and successive smaller particles adding to its edge. Once the cylinder links the two conducting electrodes of the selector device, switch happens, hence making the device to go into the ON state [41]. (b). The nucleation barrier is diminished as spherical particles are added at the cylinder end. This explains the exponential increase of current in the OFF state.

of different electronic domains, and therefore various current densities once instabilities such as NDR inside materials appear, led us to use this model in order to study V_{th} failures analyzed in the previous section through electrical measurements. According to this theory, nucleation begins with the appearing of a "lightning rod" that concentrates the electric field through the chalcogenide material. Because of this, additional nucleated crystal particles (spherical ones can be considered, as presented in Figure 5.18(a)) are gradually added to the lightning rod end. Once the crystalline filament links the two conductive electrodes, switching occurs and this linking is responsible for the voltage drop observed in the ON state [41]. As nucleation happens, the local field E strength is decreased, thus diminishing the nucleation barrier W (See Figure 5.18(b)), necessary to add crystalline spheres at the cylinder edge (Equation 5.3):

$$W = \frac{W_0}{\left(1 + \frac{E_0^2 \varepsilon_r \varepsilon_0 R^3 \pi}{W_0}\right)^2} \quad (5.3)$$

where E_0 is the applied electric field over the selector device, ε_r the relative electrical permittivity of the chalcogenide material, and W_0 the zero-field nucleation barrier.

The nucleation time is the switching delay and is dependent of the applied electric field and therefore the nucleation barrier. It is defined as follows:

$$\tau_n = \frac{1}{\nu} \exp\left(\frac{W}{K_b T}\right) \quad (5.4)$$

with ν being the vibrational frequency of the material.

At this point, it is maybe necessary to recall that for the ON state, the selector device presents metastable structures which are responsible for the OTS volatility (see subsection 4.1.1). Besides, and since threshold switching voltage is the subject of study, only the sub-threshold current is estimated. To do so, cylinder growth over the time is defined in Equation 5.5, with h_{Cyl} being the crystal cylinder height at the instant t and ranging from 0 to h_{CylMax} , which corresponds to the chalcogenide thickness (see Figure 5.18(a)).

$$\frac{dh_{Cyl}}{dt} = \frac{h_{CylMax} - h_{Cyl}}{\tau_n} \quad (5.5)$$

The discrete resolution of the differential Equation 5.5, for the crystal cylinder height at the instant t is:

$$h_{Cyl_{i+1}} = (h_{Cyl_i} - h_{CylMax}) \cdot \exp\left(\frac{-\Delta t}{\tau_n}\right) + h_{CylMax} \quad (5.6)$$

with Δt being the time step.

Using the compact model proposed by Bocquet *et al.* [51] as inspiration, two current densities are assumed inside the selector device in order to calculate the sub-threshold current. A first one coming from the crystal cylinder (I_{Cyl}) and a second one from the remaining amorphous region (I_{Amorph}) (Equation 5.7):

$$I_{Subthres} = I_{Amorph} + I_{Cyl} \quad (5.7)$$

The crystal cylinder current presents ohmic behavior and is defined as follows:

$$I_{Cyl} = \sigma_{Cyl} \cdot \frac{V_{cyl}}{h_{Cyl}} \cdot \pi \cdot R_{Cyl}^2 \quad (5.8)$$

where σ_{Cyl} is the electrical conductivity of the crystalline cylinder and V_{Cyl} is the voltage drop over it.

As for the current density of the amorphous region, a Poole-Frenkel conduction regime is used. (Equation 5.9). Once the switching occurs (i.e. $h_{Cyl} = h_{CylMax}$), I_{Cyl} becomes the predominant current.

$$I_{Amorph} = \sigma_{Amorph} \cdot \frac{V_{applied} - V_{Cyl}}{h_{CylMax} - h_{Cyl}} \cdot (\pi \cdot R_{Cyl}^2) \cdot \exp\left(\frac{-q \left(W_0 - \sqrt{\frac{qE}{\pi \epsilon_r \epsilon_0}}\right)}{K_b T}\right) \quad (5.9)$$

with q being the elementary charge and σ_{Amorph} the conductivity for the amorphous region, which is extremely low. For simplicity, this conductivity was taken as a constant, but further studies could include a variation over it as a function of the domain height.

As stated before V_{cyl} is the voltage drop over the crystalline domain. It can be calculated using the voltage divider between the amorphous region and the domain itself, each one of them defined by its own electrical resistance as follows:

$$R_{Cyl} = \frac{1}{\sigma_{Cyl}} \cdot \frac{h_{Cyl}}{\pi \cdot R_{Cyl}^2} \quad (5.10)$$

$$R_{Amorph} = \frac{1}{\sigma_{Amorph}} \cdot \frac{h_{Cyl} - h_{CylMax}}{\pi \cdot R_{Cyl}^2} \quad (5.11)$$

Consequently,

$$V_{Cyl} = \frac{R_{Cyl}}{R_{Cyl} + R_{Amorph}} \cdot V_{applied} \quad (5.12)$$

$$V_{Cyl} = V_{applied} \cdot \frac{\frac{1}{\sigma_{Cyl}} \cdot h_{Cyl}}{\frac{1}{\sigma_{Amorph}} \cdot (h_{CylMax} - h_{Cyl}) + \frac{1}{\sigma_{cyl}} \cdot h_{Cyl}}$$

5.5.2.a Model results

Aiming to confirm the validity of the proposed model, DC curves for OTS and OTS+OxRAM systems were fitted. A summary of the physical parameters used is presented in Table 5.1

Table 5.1: Parameters used for the calculations of the Metastable Nucleation Filament Model.

Symbol	Name	Numerical Value
σ_{Cyl}	Electrical conductivity of the crystal cylinder	$5 \cdot 10^6 m \cdot S$
σ_{Amorph}	Zero-field electrical conductivity for a formed OTS	$\approx 0.275 - 0.53 \cdot 10^6 m \cdot S$ (thickness dependent)
R	Domain radius	$\approx 3nm$ [52]
h	Domain height	Max height = chalcogenide thickness
E_0	Electric field applied	
W_0	Zero-field nucleation barrier	$2.65eV$
q	Elementary charge	$1.6 \cdot 10^{-19} C$
ϵ_r	Relative permittivity	10
v	Vibrational frequency in a crystal	$1/v = 10^{-13} s$

A first result can be found in Figure 5.19. There, an example of two typical IV curves for the two selector thicknesses used in this study are depicted. An excellent fit can be observed thanks to the use of the Metastable Nucleation Filament Model (MNFM). As stated in a precedent section, only the sub-threshold current as well as the switch point are modeled. In principle, the MNFM could be used to fit the quasi-static characteristic

of the forming process too. In that case, the nucleation barrier W_0 at zero-field should be much larger.

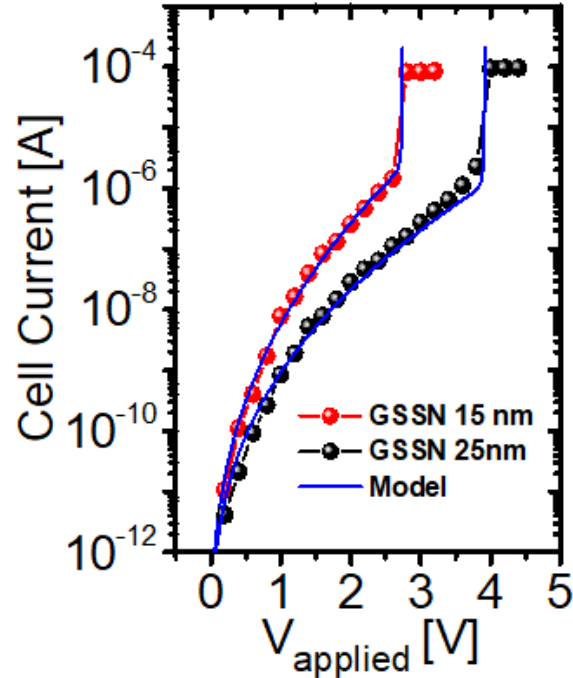


Figure 5.19: Quasi-static experimental characteristics of a GSSN selector device. Two thicknesses are presented: 25 nm and 15 nm. Model using field nucleation theory is able to fit these IV curves

The successful fitting of the sub-threshold current as well as the switching point of the OTS devices allows to study V_{th1} and V_{th2} distributions. For the latter, Monte-Carlo simulations were undertaken assuming standard deviations of 1 nm and 0.1 eV for the OTS thickness and zero-field nucleation barrier respectively. To account for the voltage drop over the resistive memory, once the selector device switches, a LRS value of 10 $K\Omega$ was used. In the case of V_{th1} , voltage drop distributions generated by HRS dispersions (subsection 5.5.1) were added to the V_{th2} distributions leading to the result presented in Figure 5.20. There, measured distributions for the 25 nm GSSN thickness are compared to calculations using the MNFM. The model presents an excellent agreement with the experimental data for both V_{th1} and V_{th2} switching values.

The validation of the assumptions made thanks to the effective modeling of threshold voltages confirms the origin of reading failures generated by V_{th1} dispersions. Two causes of variability have been therefore identified: OTS switching voltage variability and resistance values dispersions of the OxRAM memory, mostly those ones corresponding to the HRS. Same results were obtained thanks to Poole-Frenkel calculations in subsection 5.5.1.

Concerning the Metastable Nucleation Filament Model, local crystallization needs further studies. In this first approach, no insights about the localization of the crystal cylinder or the temperature increase that could act as an accelerator factor to the growth, were considered. To do so, electrical characterizations of the OTS+OxRAM devices

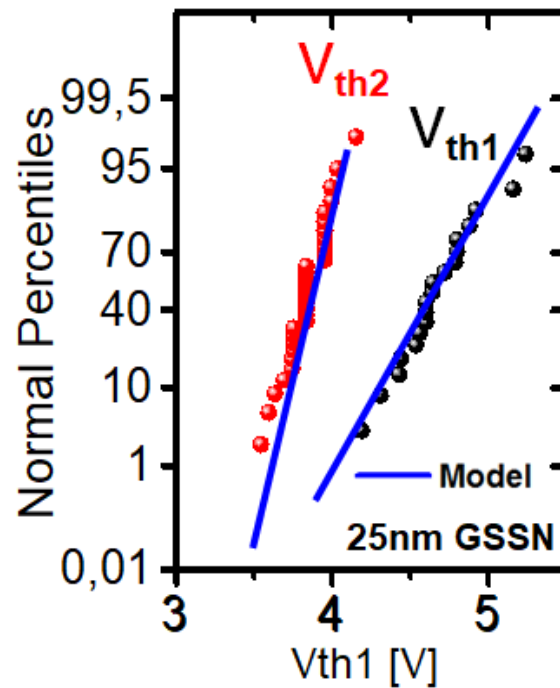


Figure 5.20: Measured and simulated V_{th2} (OxRAM in LRS) and V_{th1} (OxRAM in HRS) switching voltages for 25 nm OTS

need to be done at various temperatures. Moreover, additional works using several OTS materials and dimensions could be conducted in order to have more information about the filamentary or bulk characteristic of the switching phenomenon. Another aspect that is not studied in this first analysis, concerns the radial growth of the crystal once the switching occurs. This could be linked to the I_{ON} current increase, which presents an ohmic behavior when a compliance current method is not used.

5.6 Conclusions and Perspectives

- $GSSN + HfO_2$ reliability was investigated at the array level for the first time, to our knowledge. OTS+OxRAM systems were co-integrated on top of Metal 4 of a 130nm technology with 300nm cell size. Studied GSSN thicknesses between 15 and 25 nm and 10nm HfO_2 OxRAM were used.
- R_{ON} resistances for various programming currents over 1S, 1R and 1S1R structures, was studied. Interestingly, and for the three cases, same resistances values and the same behavior is obtained regardless of the thickness, the device size and the stacks tested, indicating an universal behavior. This observation seems to indicate a filamentary-like behavior for the conduction in the ON state of the OTS devices.

- In chapter 4, it was concluded that a ΔV_{th} reading strategy was the most adequate one according to the $GSSN + HfO_2$ electrical performances. There, $V_{th2} < V_{Read} < V_{th1}$, with V_{th1} , V_{th2} corresponding to the HRS and LRS OxRAM resistive states. In order to address variability and reliability under such scheme, in this chapter, three key features were identified: (1) Current margin at V_{Read} , equivalent to the ratio between I_{ON} (OxRAM in LRS) and I_{OFF} (OxRAM in HRS); (2) Selectivity, which is determined by the $I_{ON}/I_{leakage}$ ratio; and the (3) Voltage reading margin (RM). Under such scenario, excellent performances were achieved, confirming the importance of OTS devices not only for PCM stacks, but for another emerging-memory such like ReRAM for cross-point arrays: current margin ($\approx 10^3$) and selectivity (10^5) during more than 10^6 programming cycles and 10^8 reading cycles were demonstrated. These metrics are summarized in Table 5.2 and compared to another 1S1R systems from literature. The most important aspects affecting them are also highlighted.

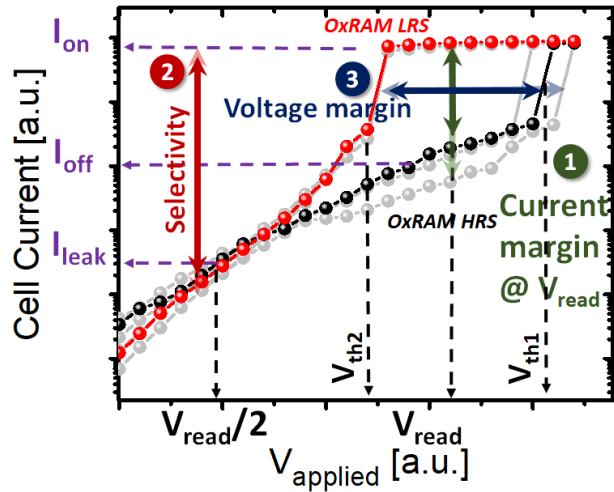


Table 5.2: $GSSN + HfO_2$ performances comparisons and associated reliability limitations

Device Feature	[17, 53]	[4]	[12]	This work	Impacted by
Selectivity I_{ON}/I_{leak}	10^6	-	100	10^6	OTS leakage
Endurance cycles	10^5	10^7	-	$5 \cdot 10^6$	ReRAM endurance
Reading cycles	10^8	10^8	10^6	10^8	OTS endurance
Current Margin I_{ON}/I_{OFF}	10^3	> 10	10	10^3	I_{Prog} , OTS I_{OFF}
Read Voltage Margin	1V	1V	1V	1V	OTS and ReRAM dispersion

- Among the three key features mentioned above and after statistical study, voltage read margin was found to be the most critical one. This is mainly caused by the high variability of the threshold voltages defining the ΔV_{th} range. Such dispersions can lead to reading failures or data integrity corruption. Consequently V_{Read} must be carefully chosen inside the reading range.
- V_{th1} presents a higher variability than V_{th2} . This phenomenon is confirmed in spite of the *GSSN* thickness or the 1S1R degradation. Through estimations based on electrical characterization of *HfO₂* stacks, the larger slope of such distributions was associated to the intrinsic HRS resistance dispersion. Consequently, higher HRS values, are expected to produce increased V_{th1} median values. On the other hand, and given that the employed OTS, determines the resistive window margin (WM) of the co-integrated ReRAM, some thicknesses or stoichiometries will be more compatible with specific OxRAM stacks, if maximization of the 1S1R, capital to the crosspoint reliability, is intended. Under such optimal scenario, classical trade-offs, well known for ReRAM technologies [24], must be also taken into account. Increased WM, could lead to endurance or retention degradation.
- Semi-analytical analysis based on a Metastable Nucleation Filament Model (MNFM) approach, confirmed the previous conclusions. V_{th2} variability can be associated to the OTS intrinsic variability, while V_{th1} is affected by both OTS and OxRAM HRS dispersions. In future works, the model could be completed, for instance, including temperature influence over the crystal growth rate as well as the radial expansion once switching occurs. 1S1R devices could be patterned with smaller dimensions in order to confirm filamentary-like conduction of the OTS high-conductive state.
- Next research subjects over OTS+ReRAM systems could include: new materials to improve device performances, notably ReRAM topologies with higher resistive window margin (CBRAM stacks could be an option); and crossbar arrays demonstrations over aggressive technological nodes, with sense amplifier and taking into account critical process steps such like memory point dimensions, stack etching and contamination materials management, in order to be closer to real implementations.

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General Conclusions and Perspectives

6.1 Conclusions

This work studied reliability of ReRAM memories for Storage Class Memory (SCM) applications. These technologies are based on the creation and dissolution of a conductive filament, that changes the resistivity of the device in a non-volatile way and therefore profit it to have the logic states. Although most of the ReRAM performances are very interesting compared with Flash technologies, two main drawbacks are identified: states variability and low non-linearity. Along with high fabrication costs per bit, these factors avoid ReRAM large scale implementation. For the first aspect, a special focus was made on endurance behavior. Memory arrays integrated in the Back-End-Of-Line of a 130nm CMOS technology, allowed the extraction of endurance failure dispersions, linked to the hard breakdown of the cells. Through a variety of programming conditions and over various memory stacks, it was found that the distributions of such failure values, defined as the maximum number of cycles (N_{cmax}), follow a log-normal law regardless of the used stack. For the programming protocol employed, it was established that SET voltage does not change the median behavior but can eventually generate some tails on the distributions. This is explained by the compliance current used during such process and controlled with the gate voltage of the CMOS transistor. On the other hand, and given that during RESET, such compliance does not exist, slight variations of V_{RESET} , degrade the N_{cmax} median value as well as the standard deviations. An optimized RESET ensures longer enduring devices and less dispersed failure.

In the second stage of the endurance studies, fits of N_{cmax} dispersions were obtained through a stochastic model. Failure was attributed to states featuring large bounding energies that generate non-switchable sites inside the conductive filament. Thus, large dispersions were linked to characteristics of the residual filament, which include its size, its shaped and a very localized number of potential defect sites. As for the defects, a nucleation and growth theory was found to be more adapted to model experimental results than random generation.

As mentioned before, low non-linearity (NL) of ReRAM devices also hinders large scale implementation. It implies the appearance of leakage currents at the array level. This is why, access devices that present high NL, are required. After a diagnostic on the

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motley of existing alternatives, Ovonic Threshold Selectors (OTS) were chosen. Previous works in our investigation group, led to the optimization of $GeSeSbN$ (1S) chalcogenide selectors. For this thesis, they were co-integrated with HfO_2 (1R) OxRAM memories in 1S1R configurations with remarkable electrical performances. As their name indicate it, OTS switches once an $I_{th}(V_{th})$ value is reached. The voltage drop over the OxRAM under I_{th} leads to a $\Delta V_{th} = V_{th1} - V_{th2}$, where V_{th1} and V_{th2} , correspond to the high and low resistive states of the ReRAM memory (LRS and HRS). As a consequence ΔV_{th} , allows to define a reading voltage inside this range. After examination of various reading alternatives, that one aforementioned was found to be the most adapted for the 1S1R systems. Tile sizes up to 1Gb in crossbar configurations were estimated based on I_{leak} metrics. However, IR drop and CMOS periphery size seem much more restrictive in terms of bank dimensions, and most aggressive technological nodes would imply smaller array sizes too.

Posterior to our first $HfO_2+GeSeSbN$ proof of concept, performances of 1S1R devices at the array level were investigated for the first time, to our knowledge. 1S1R structures were co-integrated on top of Metal 4 of a 130nm technology. Hence, variability and reliability using the ΔV_{th} were addressed through the identification of three key features: (1) Current margin at V_{Read} , (2) Selectivity and (3) Voltage margin defined by ΔV_{th} . Current margin ($\approx 10^3$) and selectivity (10^5) were kept for at least 10^6 programming cycles and 10^8 reading cycles. The most important aspects affecting such metrics were identified. The voltage margin was demonstrated to be the most critical feature in terms of 1S1R reliability. High variability of V_{th1} and V_{th2} was measured. Consequently, those high dispersed values can lead to reading failures or data integrity corruption. V_{th1} presents higher variability than V_{th2} . It was proved how such higher variability is mostly affected by the intrinsic HRS distribution.

Finally, a semi-analytical analysis based on Metastable Nucleation Filament Model (MNFM) was developed to study V_{th} values dispersion. Since a theoretical approach it was confirmed how V_{th2} dispersion is associated to the OTS intrinsic variability, while V_{th1} is affected by both OTS and OxRAM HRS dispersions.

6.2 Perspectives

As for the next stages that could be potentially undertaken to give continuity to this thesis work, once again they need to be sorted as a function of the two strands of work prior mentioned: endurance reliability and 1S1R systems. For the former, optimized and less time consuming measurement protocols, could be implemented in order to have more data for bigger populations using less characterization time. Such strategies could include increased temperature during cycling in order to accelerate devices degradation and low quantiles extraction through individual points failing respect to the quantity of cycled devices simultaneously. On the other hand, the developed stochastic model could be used as a basis for future studies including more physical notions which could include defects dimensions, conduction mechanisms involved in their generation, and electronic

Chapter 6: General Conclusions and Perspectives

characteristics of the oxides employed.

Concerning OTS+ReRAM co-integration more complete analysis need to be done in order to increase accuracy of the tiles estimations (e.g. multi-bit operation, compensation techniques, sense amplifier, forming transistors, etc). Also, ReRAM stacks with most important WM could be considered, since it could increase the ΔV_{th} range. However, classical trade-offs of ReRAM performances should be considered given that increasing resistive window margin, could lead to endurance or retention degradation. On the other hand, higher NL for the OTS devices will be always wished. Nevertheless, it was observed how lower leakage currents imply higher switching values. Thus, higher V_{th} could be less adapted for specific memory technologies in terms of devices lifetime. Moreover, the successful co-integration of $GeSeSbN + HfO_2$ devices, opens the way to full crossbar implementations using such materials and over aggressive CMOS technological nodes, with sense amplifier and taking into account critical process steps such lie stack etching.

Finally the MNFM approach chosen to analyze OTS switching behavior could be completed including temperature dependence of the switching event and radial expansion of the crystal. A lot of theoretical and experimental works need to be done in order to validate filamentary conduction hypothesis, for instance, through device size reduction.

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