Failure mechanisms implementation into SiGe HBT compact model operating close to safe operating area edges

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FAILURE MECHANISMS IMPLEMENTATION INTO SiGe HBT COMPACT MODEL OPERATING CLOSE TO SAFE-OPERATING-AREA EDGES

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Abstract - EN

In an ever-growing terahertz market, BiCMOS technologies have reached cut-off frequencies beyond 0.5 THz. These dynamic performances are achieved thanks to the current technological improvements in SiGe hetero-junction bipolar transistors (HBTs). However, these increased performances lead to a shift of the transistors bias point closer to, or even beyond, the conventional safe-operating-area (SOA). As a consequence, several parasitic physical effects are encountered such as impact-ionization or self-heating which can potentially activate failure mechanisms, hence limiting the long-term reliability of the electronic device. In the framework of this thesis, we develop an approach for the description and the modeling of hot-carrier degradation occurring in SiGe HBTs when operating near the SOA edges. The study aims to provide an in-depth characterization of transistors operating under static and dynamic operating conditions. Based on these measurements results, a compact model for the impact-ionization and the self-heating has been proposed, ultimately allowing to extend the validity domain of a commercially available compact model (HiCuM). Considering the operation as close as possible to the SOA, an aging campaign was conducted to figure out the physical origin behind such failure mechanism. As a result, it has been demonstrated that hot-carrier degradation leads to the creation of trap densities at the Si/SiO_2 interface of the emitter-base spacer which induces an additional recombination current in the base. A compact model integrating aging laws (HiCuM-AL) was developed to predict the evolution of the transistor/circuit electrical parameters through an accelerated aging factor. For ease of use in computer-aided design (CAD) tools, the aging laws have been scaled according to the geometry and architecture of the emitter-base spacer. The model has demonstrated its robustness and its accuracy for different SiGe HBT technologies under various aging conditions. In addition, a study on the reliability of several integrated circuits has been performed leading to a precise location of the most sensitive regions to the hot-carrier degradation mechanism. Thus, the HiCuM-AL model paves the way to perform circuit simulations optimizing the mm-wave circuit design not only in terms of sheer performances but also in terms of long-term reliability.

Keywords: SiGe HBT - Reliability - Compact model - Hot-carriers

Résumé - FR

Afin de répondre au marché florissant des applications térahertz, les filières BiCMOS atteignent désormais des fréquences de coupure supérieures à 0,5 THz. Ces performances dynamiques sont obtenues grâce aux améliorations technologiques apportées aux transistors bipolaires à hétérojonction (TBH) SiGe. Toutefois, cette montée en fréquence à entraîner un décalage du point de polarisation des transistors au plus proche, voir au-delà, de l'aire de sécurité de fonctionnement (SOA). En conséquence, de nombreux effets physiques parasites sont déclenchés tel que l'ionisation par impact ou bien l'auto-échauffement pouvant potentiellement activer des mécanismes de défaillance et ainsi limiter la fiabilité à long terme du transistor. Dans le cadre de cette thèse, nous proposons une approche pour la description et la modélisation de la dégradation par porteurs chauds au sein des TBH SiGe fonctionnant aux frontières de la SOA. L'étude est basée sur une caractérisation approfondie en conditions statiques et dynamiques des transistors. Du fait de ses résultats de mesures, une modélisation de l'ionisation par impact et de l'auto-échauffement a été proposé permettant d'étendre, avec précision, le domaine de validité des modèles compact commerciaux (HiCuM). Au-vu du fonctionnement aux limites de la SOA, une campagne de vieillissement a été mise en place afin de mieux cerner l'origine physique de ce mécanisme de défaillance. De ce fait, il a été démontré que la dégradation par porteurs chauds entraîne la création de densités de pièges au niveau de l'interface Si/SiO_2 de l'espaceur émetteur-base induisant un courant de recombinaison supplémentaire dans la base. Un modèle compact intégrant des lois de vieillissement (HiCuM-AL) a été développé prédisant l'évolution des paramètres électriques d'un transistor ou d'un circuit au travers d'un facteur de vieillissement accéléré. Afin de facilier son utilisation dans des outils de conception assistée par ordinateur (CAO), les lois de vieillissement ont été adaptées en fonction de la géométrie et de l'archictecture de l'espaceur émetteur-base. Le modèle a démontré sa robustesse et sa précision pour plusieurs technologies de TBH SiGe et, ce, pour différentes conditions de vieillissement. De plus, une étude de la fiabilité de plusieurs architectures de circuits intégrés a été réalisé menant à une localisation précise des régions les plus sensibles au mécanisme de dégradation par porteurs chauds. Le modèle HiCuM-AL ouvre ainsi la voie à des simulations optimisées pour la conception de circuits millimétriques en termes de performances, mais aussi de fiabilité à long terme.

Mots-clés: TBH SiGe - Fiabilité – Modèle compact – Porteurs chauds

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General Introduction

Since the past decade, the semiconductor market is burgeoning due to the growth of new applications in the terahertz region (100 GHz to 10 THz) of the electromagnetic spectrum. Located in between microwaves and infrared, terahertz radiations present interesting properties for security, biomedical, imaging and communication fields. Indeed, due to its high penetration skill, terahertz waves can penetrate many materials, making them an asset for non-destructive quality control. Moreover, since these radiations are non-ionizing, and, therefore, presumably non-hazardous for living organisms, several studies have been carried out to detect certain forms of cancer in humans. Finally, from a mass marketing perspective, terahertz waves are targeted for the deployment of new communication standards (6G) and for radar systems in autonomous vehicles (industry of the future). This variety of applications requires the development of active device technology that can reach high cut-off frequencies together with a high level of integration for a limited manufacturing cost.

From this perspective, SiGe hetero-junction bipolar transistors (SiGe HBTs) technology seems to be the best suited to meet the growing market demand of terahertz applications. Fully integrated in the MOS transistor manufacturing process, this technology has recently reached a maximum oscillation frequency of 700 GHz and demonstrated systems operating at 240 GHz. This increased performance is made possible thanks to a miniaturization of the devices, an increase in the collector doping and the development of innovative architectures. However, the increased frequency performances of SiGe HBTs lead to a decrease in the device breakdown voltages, thus limiting the maximum output power. In the same way, transistors reach higher and higher current densities, ultimately increasing the device intrinsic temperature.

As a consequence, transistors operate now close to the safe-operating-area edges leading to the extensive activation of what has been considered so far as second-order effects such as self-heating and impact-ionization effects. These two transport mechanisms can reduce the transistor lifetime with the activation of degradation mechanisms. In the case of SiGe HBTs, the reliability of the component is mainly limited by the hot-carrier degradation. This mechanism, initiated by impact-ionization, leads to an increase in the recombination base current and, consequently, to a decrease in the current gain of the transistor.

In this context, this PhD work thesis targets multiple objectives: first, it aims to characterize and to model the transistor electrical behavior under high voltage and current biases. This study will extend the range of validity of compact models. Secondly, it intends to develop an

aging compact model taking into account the effects of hot-carrier degradation on the transistor electrical behavior under static and dynamic operating conditions. To provide accurate simulations at circuit level, the developed model will incorporate scalable aging laws. Lastly, it tries to evaluate the robustness of several integrated circuits against hot-carrier degradation with a precise location of the most sensitive regions to such degradation, within the circuit. In other words, this thesis attempts to determine whether the hot-carrier degradation leads to a failure of the RF circuit electronic function. With respect to this issue, the thesis manuscript is organized as following.

Chapter 1: State-of-the-art of SiGe HBTs - This first chapter presents the latest literature results for the design, the modeling and the reliability of SiGe HBT technology. After providing an overview of the potential applications within the terahertz frequency range, the discussion focuses on the description of the current technological advances to reach sub-millimeter frequencies. Since these new architectures are increasingly complex, the main physical effects ruling the transistor electrical behavior are described and a stable operating regime is defined. Thereafter, the compact modeling of SiGe HBT technology is addressed together with a detailed description of HiCuM compact model. Then, a methodology to evaluate the impact of hot-carrier degradation on the transistor electrical performances is described. Finally, the chapter ends with the introduction of the technologies that were under investigations during this PhD thesis work.

Chapter 2: Compact Modeling of High Biases Mechanisms - This chapter focuses on the characterization and the compact modeling of the main transport mechanisms governing the transistor electrical behavior close to the safe-operating edges, *i.e.* the self-heating and the impact ionization. First, the HiCuM compact model limitations under elevated voltage or current biases are highlighted through several measurements and simulations. An improved modeling of the impact-ionization mechanism taking into account the strong avalanche behavior together with the current dependence of the multiplication factor is elaborated. In addition, a deep characterization of self-heating effect is performed using static, dynamic and transient measurement conditions. A physics-based electrothermal model is further developed based on the intrinsic SiGe HBT architecture. Ultimately, the developed modeling is implemented in HiCuM compact model and validated on various measurement results.

Chapter 3: Physics and Modeling of Hot-Carrier Degradation - This chapter proposes a study of the hot-carrier degradation impact on SiGe HBTs under mixed-mode stress. The first section investigates the physical origin of this degradation mechanism within the transistor architecture. Subsequently, the accelerating factors of the hot-carrier degradation are identified from aging measurement results under various operating conditions. Then, based on the reaction-diffusion theory, the discussion focuses on the development of a physics-based aging compact model applicable under both static and dynamic operating conditions. Additionally, the model formulation will be scaled according to the transistor geometrical features and architecture resulting in scalable aging laws. Last, an extraction procedure of the aging model parameters is proposed and applied on two SiGe HBT technologies.

Chapter 4: Hot-Carrier Degradation Impact on Integrated Circuits - This chapter presents the impact of hot-carrier degradation on several designs of integrated circuits (ICs). Due to its consequence on the transistor current gain, the hot-carrier degradation effect is first assessed on different current mirror architectures. Then, based on the result of the comparative study of current mirrors, the robustness of a ring oscillator is evaluated under mixed-mode stress. In the last chapter section, the reliability of a broadband amplifier is investigated using both measurement and simulation results. This last chapter is followed by a general conclusion of the thesis work.

The work reported in this manuscript takes part in an European research project, TARANTO (TowARds Advanced bicmos NanoTechnology platforms for rf to the applicatiOns). This project targets to develop the next BiCMOS technology towards THz range with maximum oscillation frequency of 600 GHz and an integration within high-density CMOS processes from either Infineon (90 nm) or ST Microelectronics (28 nm). The research workflow is divided in three main working packages (WP) : Technology (WP1), Modeling/Characterization (WP2) and Design/System Test (WP3). This dissertation is included inside the second working package with a special focus on the compact modeling and reliability of active devices.

Chapter 1

State-of-the-art of SiGe HBTs

Contents

1.1 Introduction

This chapter provides an overview of the latest advances in SiGe hetero-junction bipolar transistors (HBT) in terms of architecture, modeling and reliability. The terahertz waves properties and the future applications in this frequency band are reported. The subsequent section focuses on an analysis of novel SiGe HBT architectures developed by the semi-conductor foundry to meet the requirements of high frequencies. These increased dynamic performances leads to a shift of the transistor static operating conditions to higher current densities. As a consequence, the transistor electrical behavior is dominated by which has been considered so far as second-order effects that need to be further detailed. In line with these considerations, the modeling of the device operation is discussed based on a brief history of compact models. To address the specific case of SiGe HBT reliability under forward normal operation, the mixed-mode degradation occurring in those devices is described. Finally, the SiGe HBT technologies under investigation in this manuscript are introduced.

1.2 Terahertz radiations

1.2.1 Properties

The sub-millimeter waves, named the terahertz radiations, extends from 100 GHz to 10 THz and occupy an intermediate position between the microwave and the optical domain as illustrated in figure 1.1. The lack of availability of THz sources and detectors has been long called the THz-gap. Today, this gap is closing as next generation sources and detectors become steadily available on both electronic and photonic side [1]. SiGe HBT technologies are part of this effort to reduce the THz-gap with a significant increase in frequency performance over the last decades [2]. This technology, which is fully integrated into the MOS process fabrication, offers high performance in terms of frequency, current gain and noise figure for a reduced manufacturing cost compared to III-V based technologies. For all these reasons, the SiGe HBT technology already addresses the requirements for millimeter and sub-millimeter wave applications.

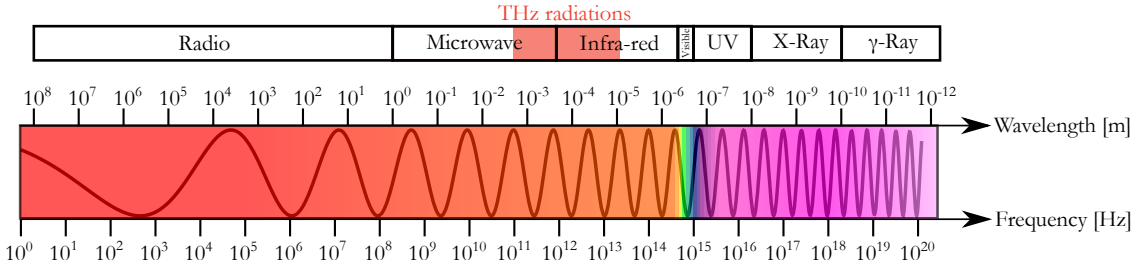


Figure 1.1: Location of the terahertz radiations within the electromagnetic spectrum.

Due to the large attenuation of nearly 1000 dB of the THz signal (see figure 1.2) for water

and water-rich materials (such as biological tissues or earth atmosphere), this particular frequency band is not suitable for long-range communication applications. However, thanks to their strong penetration skill, terahertz waves potentially allow seeing through many non-conductive materials such as skin, clothes, paper, wood or plastics [3]. This feature is shared with the microwaves on the lower end of the spectrum. Moreover, THz waves are low-energy and non-ionizing (1 THz corresponds to a photon energy of 4.1 meV, *i.e.* significantly less than the thermal activation energy at room temperature) which makes them highly suitable for the biomedical field [4]. A brief overview of the potential applications is presented below.

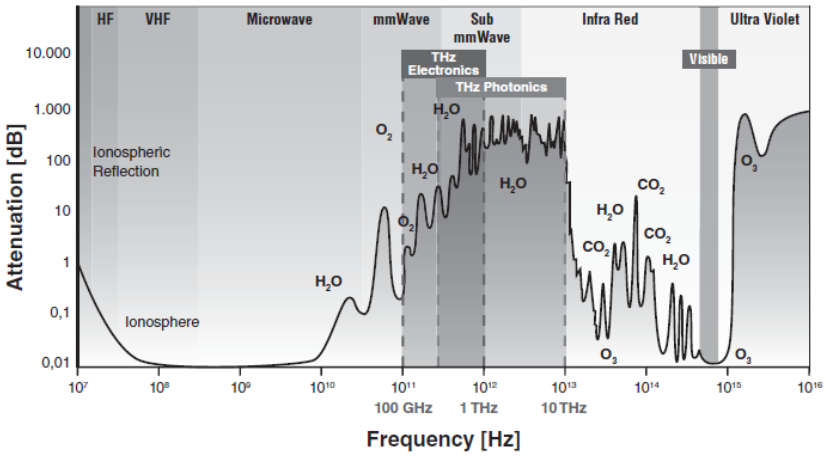


Figure 1.2: Atmospheric absorption as a function of the signal frequency taken from [4].

1.2.2 Applications

The applications of THz waves can be subdivided into three main categories: communication, radar and imaging/sensing areas, as illustrated in figure 1.3.

High-speed communication

While the fifth generation of wireless communications (5G) is being built out for the millimeter wave spectrum, the prospects for a new generation (6G) of networks and wireless applications are already being considered [6]. This communication standard will be located in the 100 GHz to 1 THz frequency bands where data rates beyond 100 Gbps could be achieved [7]. For now, the THz communication technology is moving quickly with the development of fast transmitter/transceiver with 100 Gbps data transmission rate at 287 GHz [8] for example. A quick overview of the last improvements in this field is proposed in table 1.1.

Radar

As for wireless communications, the large bandwidth offered by THz waves represents an asset for radar systems since it improves the overall range resolution. With two allocated frequency

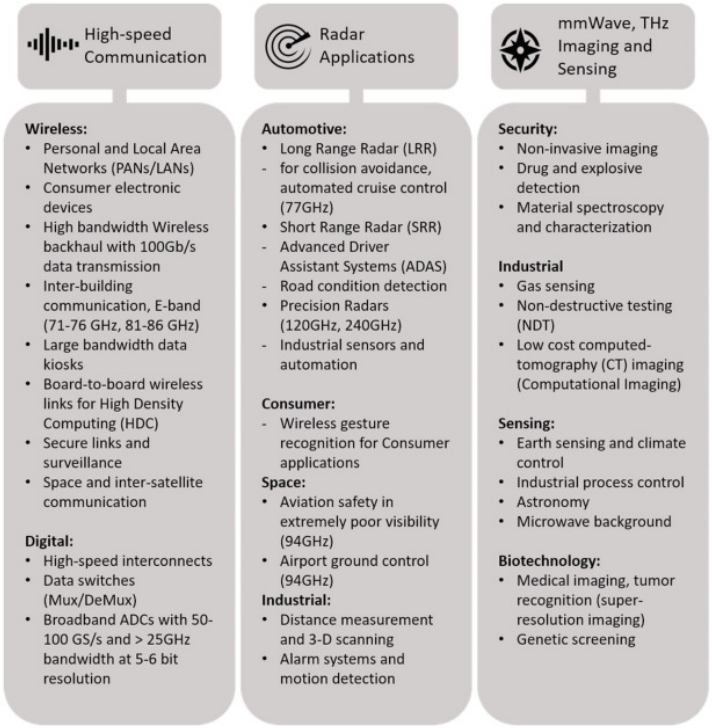


Figure 1.3: Potential applications for silicon integrated mm-wave and THz circuits taken from [5].

Ref	Year	Frequency [GHz]	Tx/Rx	Data [Gbps]	Distance
[9]	2010	120	Tx	10	5.8 km
[10]	2012	300	Tx	24	50 cm
[11]	2013	237.5	Tx	100	20 m
[12]	2017	300	Tx	56	5 cm
[13]	2018	225 - 255	Tx/Rx	65	100 cm
[8]	2018	287	Tx/Rx	100	2.22 m
[14]	2019	300	Tx/Rx	80	3 cm

Table 1.1: Wireless communication links within the terahertz frequency range.

bands (76-77 GHz and 79-81 GHz), high-frequency radars are commercially used for automotive applications. Mainly considered for Advance Driver Assist Systems (ADAS), these automotive radars are already developed but can be further improved in terms of performances [5]. Within the THz frequency range (120 GHz and 240 GHz), radar-based measurement systems are becoming an alternative to conventional measurement ones especially in the industrial measurements field under harsh conditions [15] such as in blast furnaces [16] or tank level probing [17].

Imaging and sensing

A lot of materials feature a unique spectral signature, especially in the THz frequency range. Therefore, based on a spectroscopy approach, the presence of specific chemicals or allergens

in food, drink or air may be sensed. As a non-destructive testing technique, THz waves could be further use for quality control in the food package chain [18] or for air pollution monitoring [19]. Moreover, the specific properties of THz radiations have enhanced the investigations in the biomedical domain, notably, for the recognition of normal tissues and tumors for the breast cancer [20], as sketched in figure 1.4.

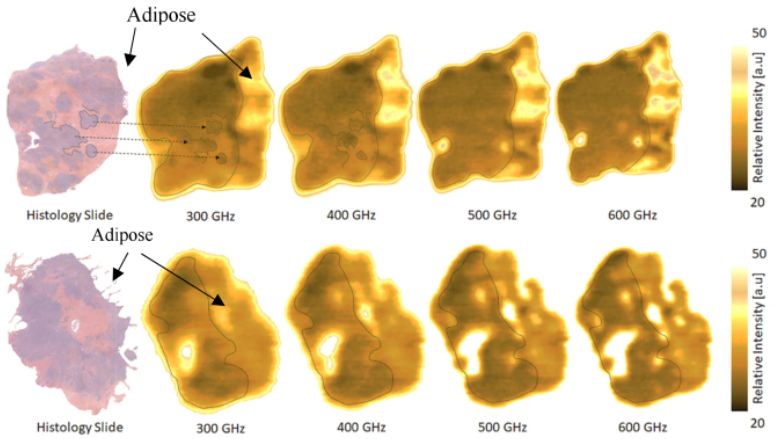


Figure 1.4: Histology image and terahertz image of breast cancer taken from [20].

1.3 Technology

1.3.1 Figures of merit

Depending on power and/or speed properties, several electrical quantities are used to define the static and dynamic performances of an HBT technology. They are commonly mentioned as figures-of-merit (f.o.m). A brief definition and associated equations are given hereafter.

Transit frequency, f_t

The transit frequency, f_t, is defined as the frequency at which the small-signal current gain (h_{21}) of the transistor is equal to unity, *i.e.* $h_{21}(f_T) = 0$ dB. The expression of the transit frequency is derived from the hybrid-π model [21] leading to equation (1.1)

$$f_t = \frac{1}{2\pi(\tau_F + \frac{1}{g_m}(C_{BE} + C_{BC}) + C_{BC}(R_E + R_C))} \tag{1.1}$$

where τ_F is the forward transit time, g_m is the device transconductance and C_{BE}, C_{BC}, R_E and R_C are respectively base-collector and base-emitter capacitances, emitter and collector resistances.

Maximum oscillation frequency, f_{max}

The maximum oscillation frequency, f_{max}, is defined as the frequency at which the unilateral power gain (U) of the transistor falls to unity, *i.e.* $U(f_{max}) = 0$ dB. It can also be expressed as

an approximation of the transit frequency together with some parasitic components: the base resistance, R_B, and the base-collector junction capacitance, C_{BC} [21]. The expression is given in equation (1.2).

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_B C_{BC}}} \tag{1.2}$$

Current gain, β

In the common-emitter configuration, the current gain, β, is expressed as in equation (1.3) where I_B is the base current and I_C is the collector current.

$$\beta = \frac{I_C}{I_B} \tag{1.3}$$

Collector-emitter breakdown voltage, BV_{CEO}

The collector-emitter breakdown voltage, BV_{CEO}, is defined as the breakdown voltage in the common-emitter configuration with the base in an open circuit configuration. This parameter specifies the maximum supply voltage that can be applied between the collector and the emitter limiting the maximum available output power of the transistor.

Collector-base breakdown voltage, BV_{CBO}

The collector-base breakdown voltage, BV_{CBO}, is defined as the breakdown voltage in the common-base configuration with the emitter in an open circuit configuration. An empirical relation between the two breakdown voltages is expressed as in equation (1.4) [21] where n is a material and doping dependent factor.

$$BV_{CEO} = \frac{BV_{CBO}}{\beta^{1/n}} \tag{1.4}$$

This expression shows that the collector-emitter breakdown voltage, BV_{CEO}, is inversely proportional to the common emitter gain of the transistor. Accordingly, a trade-off between these two parameters must be reached since a maximum gain and a maximum breakdown voltage cannot be obtained simultaneously. Moreover, the discrepancy between the two breakdown voltages is increased with increasing current gain.

1.3.2 Device architectures

The schematic cross-section presented in figure 1.5 indicates the main regions of SiGe HBT architecture. The surge for higher dynamic performances is achieved while minimizing the

access resistances to the intrinsic transistor regions (R_E, R_C and R_B) together with low contributions of the extrinsic device regions capacitances (C_{BE} and C_{BC}) [5]. In light of these considerations, several architectures have been developed by the semi-conductor foundry and are further discussed below.

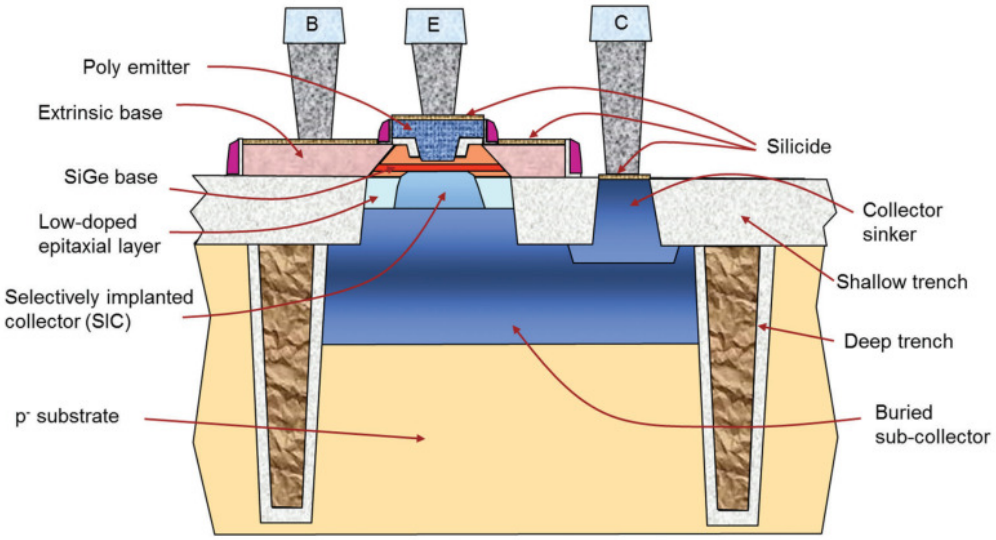


Figure 1.5: Schematic cross-section of a high-speed SiGe HBT taken from [5].

DPSA-SEG

The simplest self-alignment approach corresponds to the Double-Polysilicon Self-Aligned or DPSA architecture with a selective epitaxial growth (SEG) of the base [22]. As only one lithographic step is required for intrinsic transistor definition, this architecture is highly compatible with BiCMOS technology platform as demonstrated by ST Microelectronics [23] in 2014, Infineon [24] in 2015 and NXP [25] in 2016. One particular attractive feature is the formation of the link between the intrinsic and the extrinsic base during the growth of the intrinsic base. However, dynamic performance limits are pointed out since the intrinsic-to-extrinsic base resistance cannot be optimized independently of the intrinsic base [26]. Therefore, this architecture is no longer suitable for future BiCMOS generation targeting higher dynamic performances since f_{max} is limited to 400 GHz.

DPSA-SEG with EBL

One way to overcome the limitations of DPSA-SEG architecture is to use an epitaxial base link (EBL). In this fabrication process, the extrinsic base region is formed by SEG of B-doped silicon after emitter structuring. The improved architecture is compared to the classical DSPA-SEG HBT one in figure 1.6.

A direct comparison of EBL HBT performances against standard DPSA-SEG approach has been addressed based on identical collector designs, transistor layouts, and measurement conditions

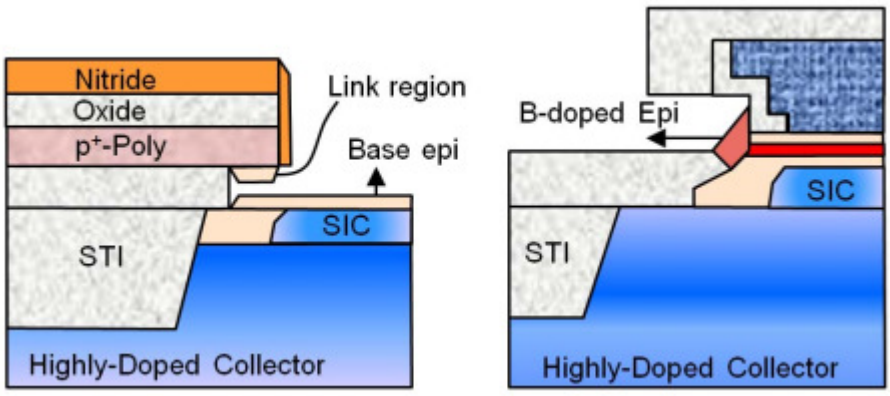


Figure 1.6: Schematic flow of the selective epitaxial growth of the base link region in both DSPA (left) and EBL (right) processes taken from [22].

during the european DOTSEVEN project [27]. An overview of the f.o.m is provided in table 1.2 for: (i) an EBL HBT architecture from a joint study of IHP/Infineon [28], (ii) an EBL BiCMOS technology from Infineon [29] and (iii) a conventional DPSA architecture from ST Microelectronics [23]. It is observed a loss in performance for the integrated architecture in a BiCMOS fabrication process flow which could be explained by an increased thermal budget for Infineon compared to IHP technology one. Moreover, a decrease from 5.5 V to 4.8 V of the second breakdown voltage, BV_{CBO}, can be pointed out between the two architectures which drastically limits the transistor bias range.

	Unit	Infineon/IHP [28]	Infineon [29]	ST Microelectronics [23]
Architecture		EBL	EBL	DPSA-SEG
Technology		Bipolar-Only	BiCMOS	BiCMOS
W_E x L_E	μm^2	0.13 x 2.69	0.12 x 2.69	0.10 x 4.9
f_T	GHz	300	240	326
f_{MAX}	GHz	500	500	376
J_C (at peak f_T)	$mA/\mu m^2$	17	11	19
Gate delay	ps	1.83	1.94	2.34
BV_{CEO}	V	1.5	1.7	1.5
BV_{CBO}	V	4.8	4.9	5.4

Table 1.2: Figures of merit comparison between EBL HBTs architectures (implemented or not in a BiCMOS flow) and a standard DPSA architecture. The table is reproduced from [5].

DPSA-NSEG with EEB

The search for a simultaneous low R_B and C_{BC} has led to develop the investigation on self-aligned architecture with non-selective growth of the base (NSEG). The process features are: (i) the creation of elevated extrinsic base (EEB) regions allowing to reduce the extrinsic base resistance, R_{BX}, (ii) the formation of the device structure in one active area without shallow-trench isolation (STI) between the emitter and the collector contacts leading to a reduced collector resistance, R_C, and a small collector-substrate junction area and (iii) the device isolation without

deep trenches resulting in a discounted process complexity and improved heat dissipation [5]. The schematic cross section of this HBT architecture is shown in figure 1.7.

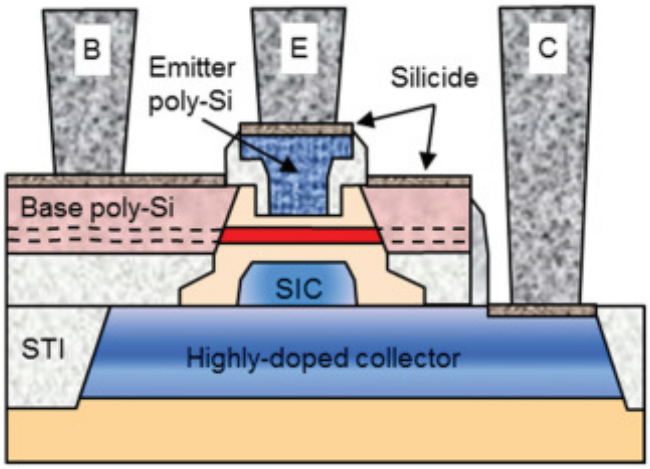


Figure 1.7: Schematic cross section of an NSEG HBT with elevated extrinsic base (EEB) regions taken from [5].

In a similar approach, table 1.3 provides a comparison of the f.o.m between the EBL HBT architecture [28] presented here before and the bipolar [30] and BiCMOS [22] technology based on an EEB architecture. From this table, one observes major improvements in dynamic performances with f_T/f_{MAX} over 505/720 GHz for the bipolar-only technology. The costs of these improvements are an increase of the peak collector current density (from 17 mA/μm^2 for EBL architecture to 32-34 mA/μm^2 for EEB one) and a decrease to 3.2-3.7 V for the second breakdown voltage, further limiting the voltage value for transistor biasing. These high current levels lead to the activation of increasingly complex physical mechanisms in the transistor as it will be further discussed in the following section.

	Unit	IHP [30]	IHP [22]	Infineon/IHP [28]
Architecture		EEB	EEB	EBL
Technology		Bipolar-Only	BiCMOS	Bipolar-Only
W_E x L_E	μm^2	0.105 x 1	0.11 x 1	0.13 x 2.69
f_T	GHz	505	470	300
f_{MAX}	GHz	720	610	500
J_C (at peak f_T)	mA/μm^2	34	32	17
Gate delay	ps	1.34	1.50	1.83
BV_{CEO}	V	1.6	1.5	1.5
BV_{CBO}	V	3.2	3.7	4.8

Table 1.3: Figures of merit comparison between EEB HBTs architectures (implemented or not in a BiCMOS flow) and an EBL architecture. The table is reproduced from [22].

1.4 Device operation

1.4.1 Physical mechanisms

The increasing complexity of SiGe HBT architectures to obtain ever shrinking dimensions leads to the emergence of what has been so far considered as second-order mechanisms that affect the electrical behavior of the transistors, especially at high injection levels. The main physical effects limiting the device operation under high voltage or current biases are presented below.

Avalanche

The avalanche effect is triggered by the impact-ionization mechanism occurring in the base-collector space charge region (BC-SCR). Under a high electric field, an electron can gain sufficient energy to generate an electron-hole pair by collision with Si atoms within the depletion region. The subsequent electron thereby created can itself lead to the generation of another electron-hole pair and initiate the avalanche effect, as illustrated in figure 1.8.

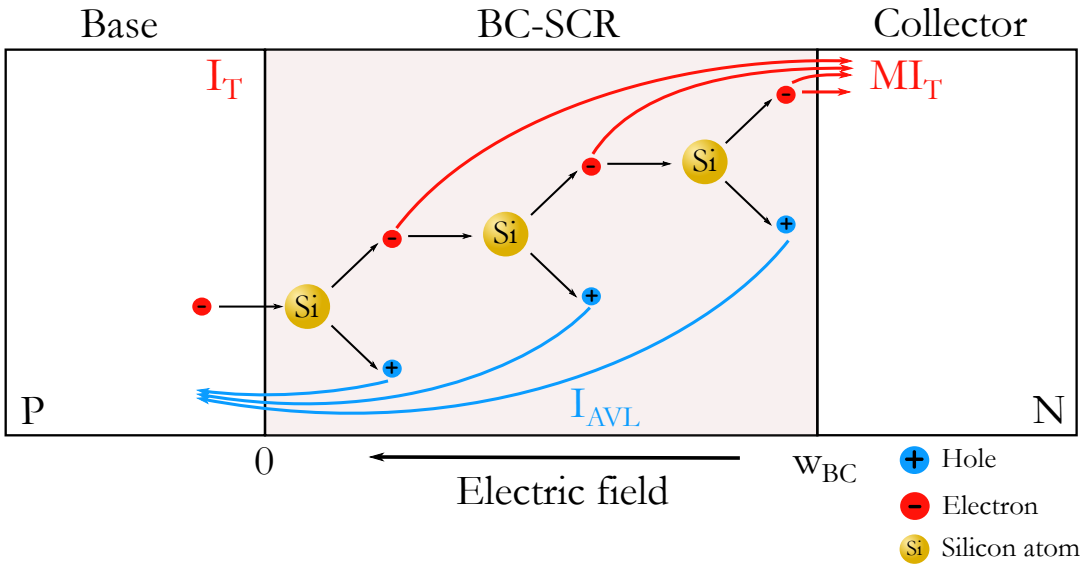


Figure 1.8: Creation of electron-hole pairs within the BC-SCR due to the impact ionization mechanism.

Those additional carriers induce an hole current, denoted as I_{AVL}, flowing from the collector to the base terminal. One way to quantify the number of created electron-hole pair is to consider a multiplication factor, M, which is defined as the ratio between the current at the collector node resulting from the avalanche process divided by the initial injected current or transfer current (I_T) [31].

$$M = \frac{I_T + I_{AVL}}{I_T} \tag{1.5}$$

The avalanche effect can be easily observed from either the base current (see figure 1.9a) or the multiplication factor (see figure 1.9b) evolution according to V_{CB}. Below the first breakdown

voltage, BV_{CEO}, the base current is positive and the multiplication factor is close to 1 indicating no avalanche effect. However, beyond BV_{CEO}, the base current becomes negative and the multiplication factor is larger than 1 highlighting the presence of impact-ionization mechanism within the BC-SCR. For voltages close to the second breakdown voltage, BV_{CBO}, the multiplication factor tends to infinity which leads to the transistor catastrophic failure.

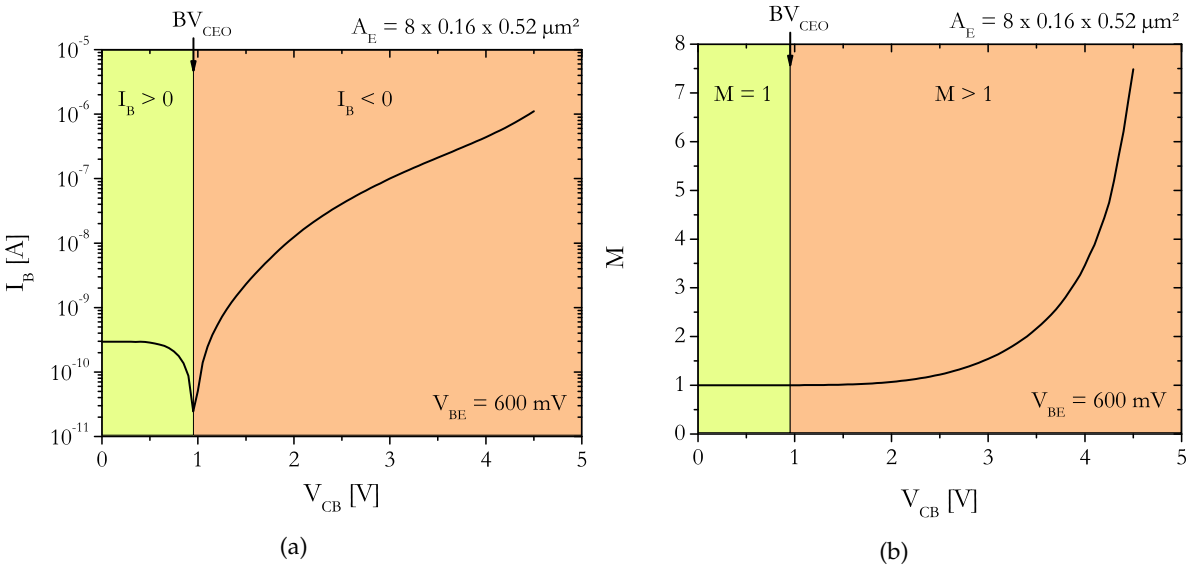


Figure 1.9: (a) I_B and (b) M evolution according to V_{CB} highlighting the avalanche behavior.

Self-heating

In SiGe HBTs, an increase of the voltage or current bias results in higher power dissipation, and, consequently, to an increase in the device temperature. Moreover, for HBT devices, the collector current features a positive temperature coefficient. Therefore, under a constant V_{BE} bias, the thermal feedback causes the increase of I_C as a function of V_{CE}, as observed in figure 1.10a. On the contrary, the self-heating effect leads to a decrease in I_C values for a fixed I_B bias, as shown in figure 1.10b. These two curves were obtained using the HiCuM compact model, further described in section 1.5.2, with the self-heating effect activated (red curve) or disabled (black curve).

The device temperature rise, under static operating conditions, is calculated according to equation (1.6) [32].

$$\Delta T = T_j - T_{amb} = P_{diss} R_{TH} \tag{1.6}$$

where T_j is the junction temperature, T_{amb} is the ambient temperature, R_{TH} is the thermal resistance and P_{diss} is the device dissipated power.

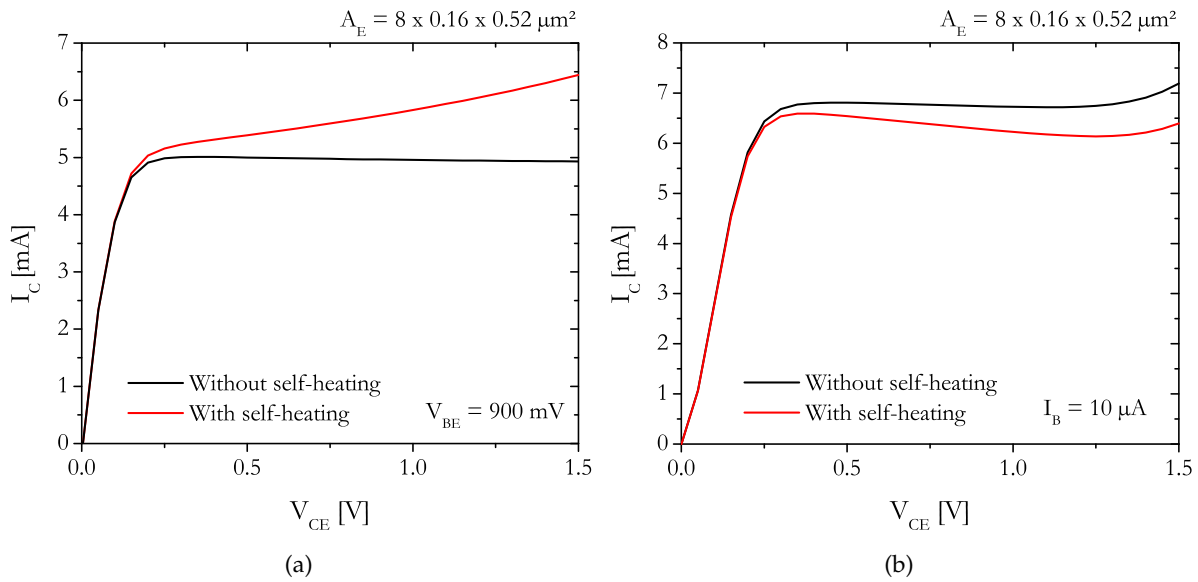


Figure 1.10: Output characteristics under (a) a constant V_{BE} bias and (b) a constant I_B bias with and without self-heating effect.

Base push-out

The base push-out or Kirk effect [33] leads to an increase of the forward transit time, and consequently, to a drop in the transit frequency at high current densities, as illustrated in figure 1.11.

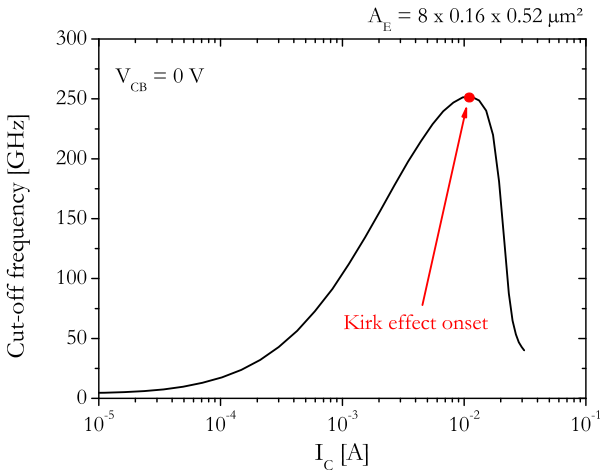


Figure 1.11: Evolution of the transit frequency according to the collector current depicting the Kirk effect onset at high current densities.

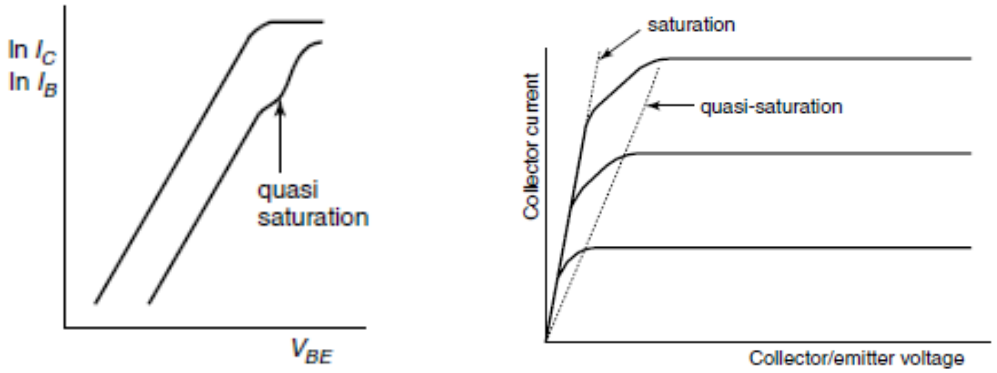
This effect occurs when the mobile charge in the BC-SCR becomes greater than the fixed ionized charge which leads to the spreading of the neutral base region towards the collector at high current densities [21]. The critical current for the Kirk effect onset is given by,

$$I_{LIM} = qA_E N_{dc} v_{sat} \tag{1.7}$$

where A_E is the emitter area, N_{dc} is the collector doping level and v_{sat} is the saturation velocity of electrons. To enhance the dynamic performances of SiGe HBTs, the Kirk effect must be repel to higher current densities requesting an increased collector doping which causes a significant degradation of the breakdown voltages.

Quasi-saturation

The quasi-saturation effect occurs at high-injections due to the internal collector resistance [21] of the transistor. An increased of the collector current leads to a large voltage drop across the collector resistance, which, thereby, causes the forward biasing of the BC junction. On the forward Gummel plot from figure 1.12a, a kink on the base current indicates the onset of quasi-saturation. Meanwhile, on the output characteristic from figure 1.12b, the quasi-saturation region is observed at low collector-emitter voltages, where the forward biasing of the BC junction can occur.



(a) (b)

Figure 1.12: (a) Forward Gummel and (b) output characteristic showing the quasi-saturation effect taken from [21].

1.4.2 Stable Operation Regime

The surge for higher dynamic performances results in a increasingly restriction of the DC operating conditions of SiGe HBTs. For this reason, a stable operation regime (SOR) allows to define the voltage and current ranges for which the transistor operates without catastrophic failure [31]. Depending on the measurement configurations (constant V_{BE} setup, constant I_B steup or constant I_E setup), the boundaries of this regime could shift but are still related to the impact-ionization mechanism [34], as presented in figure 1.13a.

Constant I_B setup In the constant I_B operation mode, the SOR is mostly limited by the first breakdown voltage, BV_{CEO}, defined for an open base configuration. For voltages larger than BV_{CEO}, the avalanche coefficient, M, tends to infinity leading to a sharp increase of the collector current, I_C, as observed on the black curve of figure 1.13a. A biasing beyond the BV_{CEO} will directly result to the transistor destruction. Note that, in the case of high-speed transistors, *i.e.*

for a high collector doping concentration, there is a shift of the BV_{CEO} to higher voltages due to the self-heating and the multiplication factor decrease at high currents [35]. Due to the rare use of the open base configuration in circuit designs, this limitation using BV_{CEO} is not relevant.

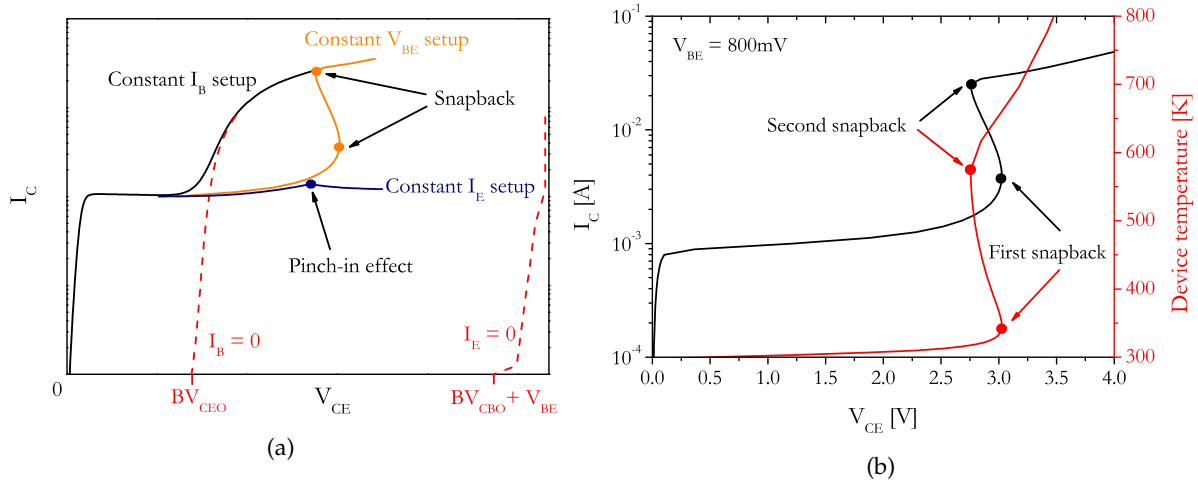


Figure 1.13: (a) Influence of the measurements configurations on a HBT output characteristic and (b) Device junction temperature for a constant V_{BE} setup.

Constant I_E setup The constant I_E setup configuration is more frequently used, especially in high-speed circuits with amplifier stages. This operation mode is first limited by the second breakdown voltage, BV_{CBO}, at low current densities due to an infinite avalanche current that causes the transistor catastrophic failure. At moderate emitter current densities, the pinch-in effect occurs as reported on the blue curve of figure 1.13a. This mechanism translates an abrupt pinch of the emitter current at the emitter center resulting in an instability of the collector current [36].

Constant V_{BE} setup Finally, in the constant V_{BE} operation mode, the output voltage is restricted by (i) the BV_{CBO} at low V_{BE}, (ii) the pinch-in effect at moderate V_{BE} and (iii) the snap-back mechanism at high V_{BE}. The first two limitations are shared with the I_E setup configuration while the last one, the snap-back mechanism, only occurs in this particular operation mode. This effect is depicted on the orange curve of figure 1.13a where three collector current values can be obtained for a given V_{BE}/V_{CE} resulting in electrical instabilities. In [37], the snap-back mechanism is associated to the voltage drop across the series resistances at high current densities. Moreover, since this mechanism is related to the avalanche and self-heating effects [37], the device temperature is also depicted in figure 1.13b together with the collector current behavior. One observes that the snap-back mechanism leads to extreme temperatures, up to 300 °C, especially approaching the second fly-back locus. These temperatures can lead to reliability issues such as electro-migration, dopant out-diffusion and, globally speaking, to device performance degradation [37]. Regarding the limitations previously defined, the corresponding stable operating regime for constant V_{BE} measurement condition is illustrated in figure 1.14.

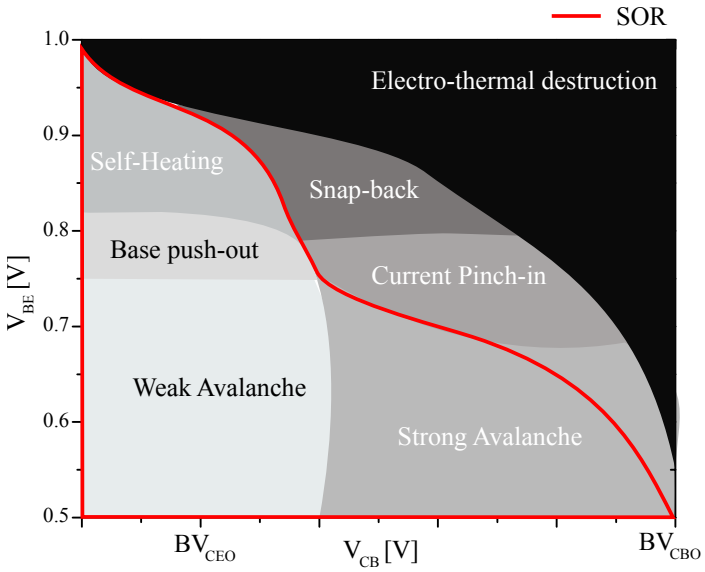


Figure 1.14: Stable Operation Regime for a constant V_{BE} setup on a high-speed SiGe HBT.

1.5 Compact modeling

1.5.1 History

A compact model is an equivalent circuit composed of discrete elements (diodes, capacitors, resistors) that are connected to each other. Each element is described by a set of analytical equations that model the device characteristics of the component based on its electrical behavior. Compared to 2D/3D numerical device simulators (such as TCAD), compact models offer an attractive trade-off between the computational efficiency and the results accuracy compared to measurements. Compact models are embedded inside a simulation framework, such as ADS, ELDO or HSPICE, providing a reliable and accurate tool for the simulation of integrated circuits.

Regarding bipolar transistors, the first compact model was published in 1954 by Ebers and Moll [38] describing the static operation of the device in forward and reverse active regime. In 1975, the SPICE Gummel-Poon (SGP) [39] was developed at the University of Berkeley and is a simplified formulation of the work of Gummel and Poon [40]. The latter were the first to introduce the generalized integral charge-control relation (GICCR) into the bipolar transistor model. Originally developed for the design of high-speed integrated circuits, the High Current Model (HiCuM) [41], [42] has emerged in 1986. Based on the GICCR, this compact model provides an accurate modeling of the transit time in all transistor operating regimes. Therefore, it has become one of the most widely used compact models in the semiconductor industry. A quick overview of this model is proposed in the next section. In a similar effort to improve the SGP model, two other compact models were introduced in the 90's: The Most Exquisit Transistor Model (MEXTRAM) by Philips [43] and the Vertical Bipolar Inter-Company (VBIC) model by Motorola [44]. Both of them are based on the Kull model [45] for the modeling of

high-injection effects in the collector. The table 1.4 provides an uptodate overview of the main physical effects considered in each compact model.

Physical effects	SGP	HiCuM/L2	MEXTRAM	VBIC
Quasi-saturation	-	√	√	√
Physic-based transit time model	-	√	√	-
BC impact-ionization	-	√	√	√
Tunneling current in the EB junction	-	√	√	-
Current crowding of the base resistance	-	√	√	-
Parasitic PNP	-	√	√	√
NQS effect	√	√	√	√
Substrate network	-	√	√	√
Self-heating	-	√	√	√
# Internal nodes	3	5	5	7
# Parameters	35	90+	65+	80+

Table 1.4: Comparison of the implemented physical effects in various bipolar transistors compact models.

1.5.2 Overview of HiCuM compact model

The HiCuM physics-based geometry-scalable compact model targets Si, SiGe and III-V material based homo- and hetero-junction bipolar transistors. There are three levels of complexity for this compact model : L0, L2 and L4 [46]. The HiCuM/L0 is a simplified version of the HiCuM/L2 model which relies on the SPICE Gummel-Poon model in term of equivalent circuit and on a reduced parameter extraction effort compared to HiCuM/L2 version [47]. On the contrary, the HiCuM/L4 model is more complex and implement distributed models to capture distributed effects such as thermal coupling or current pinch-in [48]. The equivalent circuit of the reference one, HiCuM/L2, is presented in figure 1.15.

The intrinsic transistor behavior is described by the diode currents from the BE junction (I_{jBEi}) and BC junction (I_{jBCi}), the dynamic currents resulting from the depletion charges (Q_{jCi}, Q_{jEi}) and the diffusion charges (Q_{dC}, Q_{dE}), and the controlled current source for the transfer current, I_T, which is calculated using the generalized integral charge-control relation (GICCR). Furthermore, the avalanche breakdown within the base-collector space charge region is represented by the I_{avl} controlled current source. Inside the intrinsic base region, the lateral distributed effects are modeled by the intrinsic base resistance R_{Bi}. The emitter current crowding within this region is also taking into account through the parallel capacitance C_{RBi}.

As the contribution from the intrinsic and peripheral part of the transistor are split, the carriers injection through the emitter perimeter is modeled by a depletion charge (Q_{jEp}) and a diode current (I_{jBEp}). The band-to-band tunneling current through the base-emitter space charge region is modeled by an intrinsic, I_{BEti}, or a peripheral, I_{BEtp}, contribution depending on the transistor architecture.

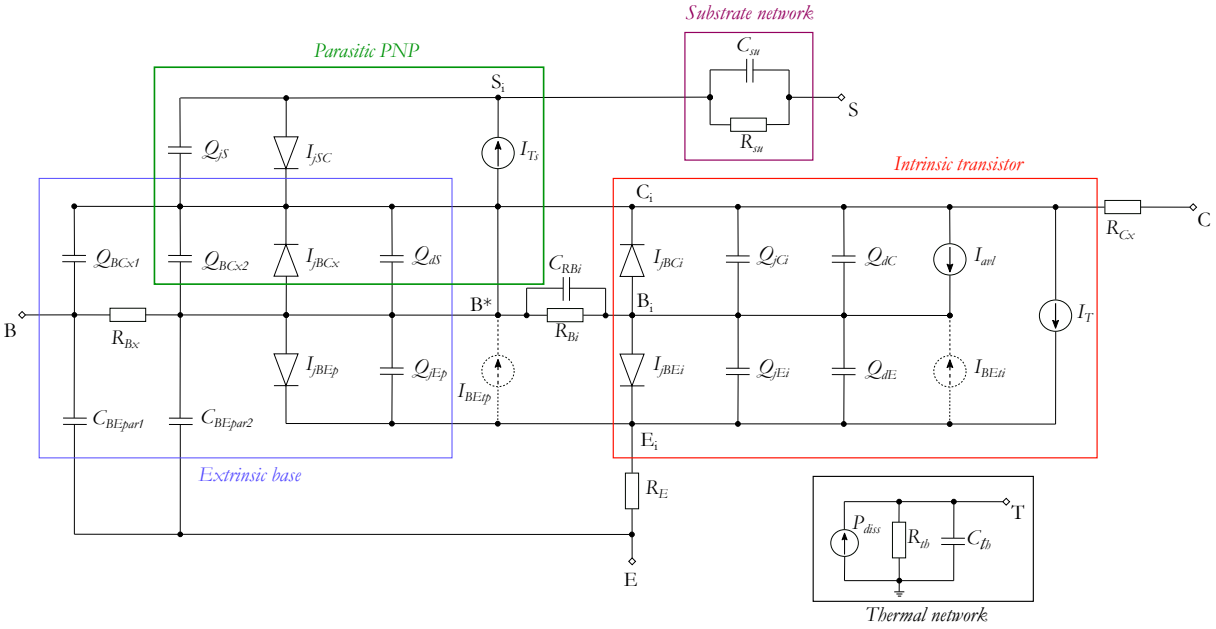


Figure 1.15: Equivalent electrical circuit of HiCuM/L2 including the electro-thermal node. Not shown are the networks for NQS effects and correlated noise.

The external BC region is represented by the junction current I_{jBCx} and the dynamic currents from the charges (Q_{BCx1}, Q_{BCx2}). These charges are split across the external base resistance (R_{Bx}) to account for distributed lateral effects at high frequencies. The external collector resistance (R_{Cx}) includes the collector contact, sinker and buried layer contributions while the emitter contact and poly-silicon resistance are represented by the emitter resistance (R_E).

The PNP parasitic transistor in the substrate is modeled by a transfer current source (I_{Ts}), a back-injection current (I_{jSC}) and a collector-substrate depletion charge (Q_{jS}). The substrate coupling effect is considered through a first-order model including a series resistance (R_{su}) and a shunt capacitance (C_{su}) resulting from the substrate permittivity influence. Another first-order model is used for electro-thermal effects accounting for the thermal resistance R_{th} and the thermal capacitance C_{th}.

1.6 Reliability issue

1.6.1 Mixed-mode stress

Within the SOR, while electrical and thermal instabilities are circumvented and catastrophic failures are avoided, it does not guarantee that the transistor will not be degraded over the time suffering from wear-out mechanisms. Therefore, a more restrictive operation region must be specified as the Safe Operating Area (SOA). Primarily introduced in 1977 [49] for bipolar transistors, the SOA can be defined as the region where the transistor works without damaging. The reduced breakdown voltages and the high current densities of SiGe HBTs leads to an increased susceptibility to hot-carrier induced failure mechanisms. As a consequence, the SOA is commonly limited by (i) the $J_{C@peak\,f_t}$ value and (ii) the BV_{CEO} value [50], as illustrated

in figure 1.16. Under a high current and voltage bias (beyond BV_{CEO}), the transistor operates under a classical mixed-mode stress which is the primary operation regime focus of this work.

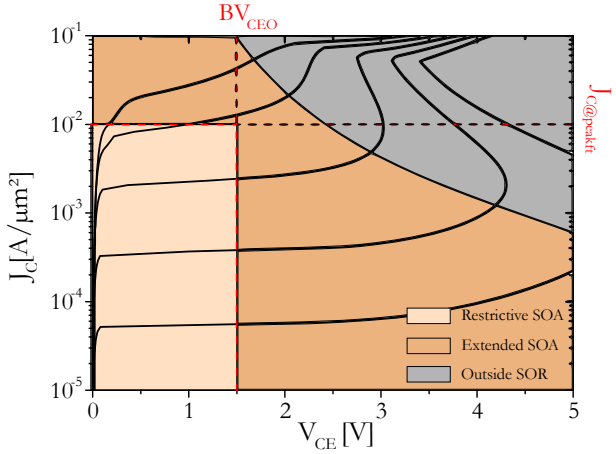


Figure 1.16: Safe Operating Area boundaries for a constant V_{BE} setup on a high-speed SiGe HBT.

The mixed-mode stress corresponds to a simultaneous bias at high J_E and at high V_{CB} [51] which results in the activation of both impact-ionization and self-heating effects. To carefully control the total injected charge, the transistors are biased under a common-base configuration with a forced J_E and V_{CB} value. Figure 1.17 presents the forward Gummel characteristic evolution according to the stress duration (up to 1000 h) for a V_{CB} = 3 V and J_E = 0.12 mA/μm^2 mixed-mode stress on a SiGe HBT device.

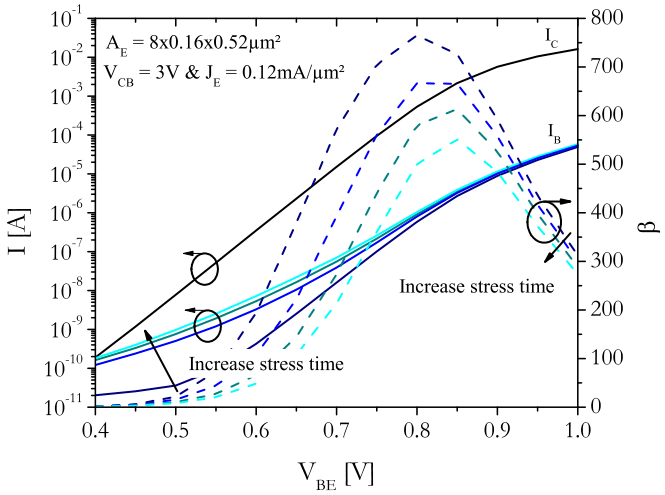


Figure 1.17: Base current and current gain β as a function of V_{BE} for a mixed-mode stress of V_{CB}=3V and J_E=0.12mA/μm^2 on a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

As observed on this plot, the mixed-mode degradation leads to an increase of the base current at low and moderation injection levels [52]–[56] through the Shockley-Read-Hall (SRH) recombination mechanism. Consequently, a large decrease of the current gain, β, from 750 to 550 at V_{BE} = 0.8 V is displayed in the same figure. Moreover, this degradation mechanism induces an increase of the low-frequency noise [57]–[59]. Under avalanche operating conditions, the

mixed-mode degradation is the result of hot-carriers creation in the BC-SCR. Those carriers can reach the transistor Si/SiO_2 interfaces and break Si-H bonds which leads to the formation of interface traps. Due to its particular consequences on the transistor electrical performances, circuit designers must be able to simulate the possible degradation at circuit level under such operating conditions. To that end, a methodology for reliability assessment is developed in the following section.

1.6.2 Methodology

In a typical work-flow, 4 months are dedicated to the process development, 2 months for the technology initial characterization and 4 months for the circuit design. Based on rigorous circuit aging tests, a design can fail to satisfy the qualification criteria which will lead to a redesign of the entire technology (from the process development to the circuit qualification). This procedure will take several months in addition to the primary duration. Therefore, in an attempt to reduce the cost and the time for the technology qualification, a dedicated methodology flow for the reliability evaluation has been developed during the last decades [60] as detailed in figure 1.18.

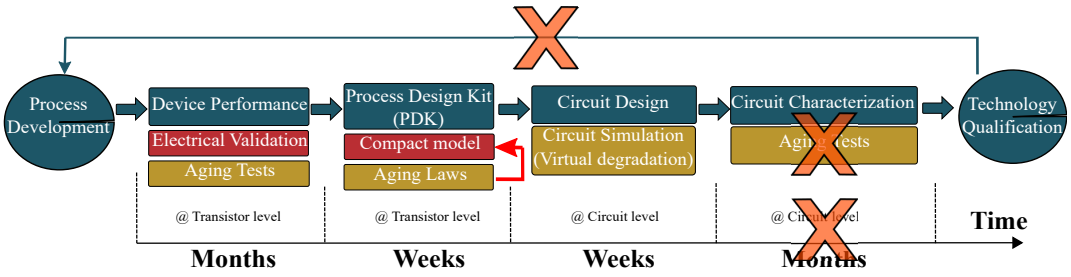


Figure 1.18: Methodology for circuit reliability prediction.

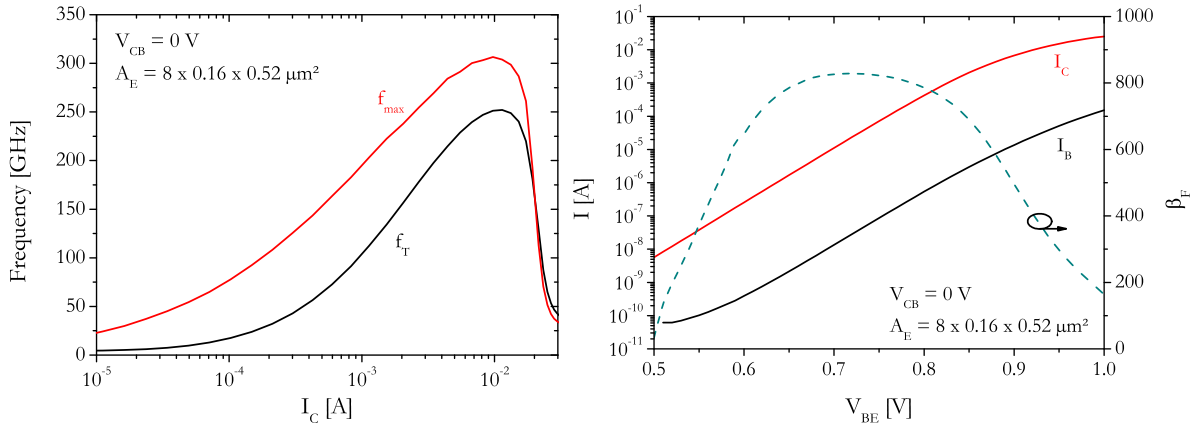
The principle involved in this methodology can be summarized as: (i) the transistors are submitted to accelerated-aging tests in order to characterize the device degradation according to the activated degradation mechanism, (ii) aging laws are derived and implemented in the HiCuM compact model based on the aging tests results and (iii) circuit simulations incorporating a virtual degradation are performed to assess the design robustness, which, thereby, allows to minimize the aging tests at circuit level. This methodology has already demonstrated its efficiency on III-V based HBT devices [60] and could further been applied on silicon-based technologies. Within the framework of this PhD thesis work, the reliability investigations are performed under mixed-mode stress on different SiGe HBT technologies.

1.7 Technologies under analysis

1.7.1 IHP Microelectronics

The technology SG13S from IHP (Innovations for High Performance) Microelectronics is based on a 130 nm SiGe BiCMOS technology node optimized for high performance targeting millimeter and sub-millimeter waves applications [61]. The back-end-of-line (BEOL) includes seven

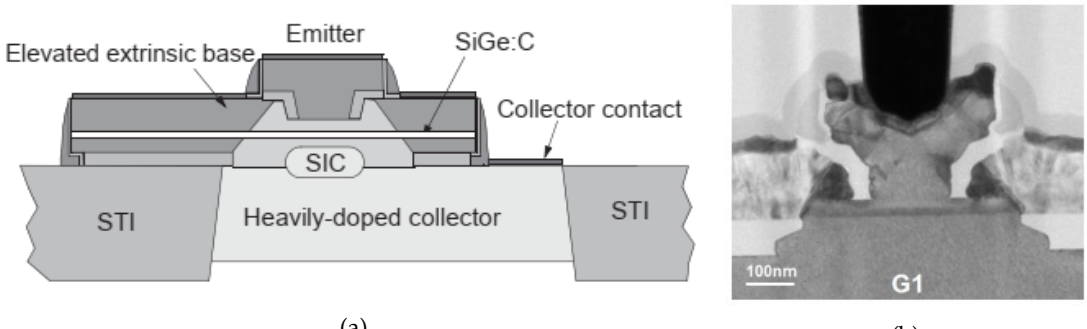
aluminum interconnect layers with two thick top metal layers of 2 μm and 3 μm and a set of passive RF components. The high-speed (HS) NPN transistors exhibits f.o.m of $f_t/f_{max}/BV_{CEO}$ of 240 GHz/ 330 GHz/ 1.7 V. Both static and dynamic characteristics are shown in figure 1.19 on a 8 x 0.16 x 0.52 μm^2 device. The peak frequency is reached for a collector current density value of 15 mA/μm^2 as reported in [62].



(a) (b)

Figure 1.19: (a) f_t and f_{max} as a function of the collector current and (b) Gummel characteristics for a high-speed transistor corresponding to SG13S technology from IHP Microelectronics.

The HBT structure is integrated in the BiCMOS flow after gate poly structuring and before the implantation of the source/drain extensions of MOS components [63]. The final structure of the HS-HBT is presented in figure 1.20a with a heavily-doped collector isolated by shallow-trench regions, a B-doped elevated extrinsic base and a As-doped crystalline emitter. A TEM cross section of the DPSA-NSEG with EEB (see section 1.3.2) architecture is displayed in figure 1.20b for an effective emitter width of 0.16 μm. As observed, the heavily-doped collector is isolated using shallow-trench regions (STI). Compared to other SiGe HBT technologies, the collector contact is not isolated from the intrinsic transistor which lead to a relaxation of the thermal constraints.



(a) (b)

Figure 1.20: (a) Schematic [64] and (b) TEM cross-section [62] for a high-speed transistor from SG13S technology.

In the context of this PhD thesis, the investigated transistor are based on a CBE configuration (1 collector, 1 base) featuring a constant emitter width of 0.12 μm, two associated emitter lengths

of 0.52 μm - 0.88 μm and multiple emitter fingers (N_X = 4 or 8).

1.7.2 ST Microelectronics

The technology BiCMOS55, also called B55, from STMicroelectronics, based on the 55 nm CMOS technology node [23], is dedicated to millimeter and sub-millimeter applications. The current technology is based on the DPSA-SEG architecture (see section 1.3.2). The BEOL includes 8 copper metal layers and 1 aluminum copping layer which is fully compatible with the existing 55 nm CMOS libraries. The technology is composed of three collector flavors: high-speed (HS), medium-voltage (MV) and high-voltage (HV) transistors. The f.o.m of each device is summarized in table 1.5.

Type	f_t [GHz]	f_{max} [GHz]	BV_{CEO} [V]	BV_{CBO} [V]
HS NPN HBTs	325	375	1.5	5.5
MV NPN HBTs	180	385	1.9	7.3
HV NPN HBTs	65	270	3.2	14.4

Table 1.5: Figures of merit for three different collector flavors from B55 technology.

In the context of this PhD thesis, only HS transistors will be investigated as their are dedicated to high-frequency applications. Compared to MV and HV devices, the HS architecture results in a higher collector doping level. The TEM cross section of an HS transistor is presented in figure 1.21 with the detailed doping type for the emitter, the base and the collector. The investigated transistors are based on a CBEBC configuration (2 collectors, 2 bases and 1 emitter).

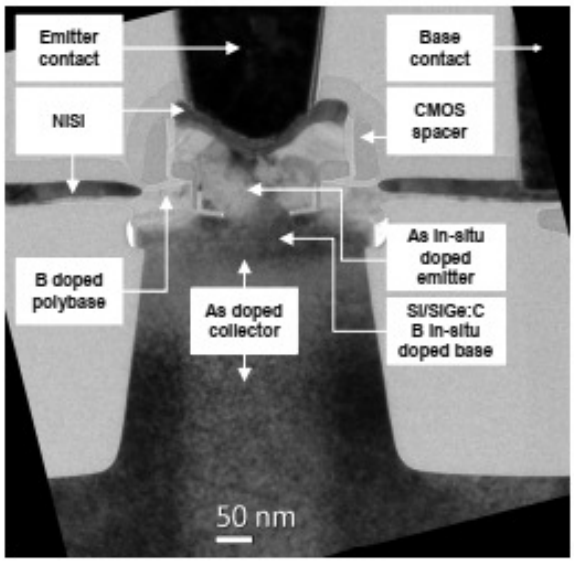


Figure 1.21: TEM cross-section of a 0.1 x 4.9 μm^2 HS SiGe HBT from B55 technology [23].

1.8 Conclusion

The first chapter outlined the basic key concepts addressed during this PhD thesis manuscript. Specifically, it was presented a survey on SiGe HBT technologies with regard to the architecture, the device operation, the compact modeling and the reliability.

In the first section, it was described the targeted applications within the terahertz frequency range. Due to its special properties, the THz waves are highly suitable for both research and industrial fields such as biomedical or high speed-communication. In this frequency domain, ranging from 100 GHz to 10 THz, SiGe HBT technologies have successfully achieved oscillation frequencies up to 700 GHz within the Taranto project. These high frequency performances are obtained thanks to the development of novel architectures.

Based on a self-alignment approach (DPSA), the current advances have been focused on a non-selective growth of the base (NSEG). This particular fabrication process has reached dynamic performances of 505/720 GHz for a bipolar-only device and of 470/610 GHz for a BiCMOS device. Due to the increased collector doping and the miniaturization of the geometry features, the peak collector current density has been drastically increased up to 30 $mA/\mu m^2$. Moreover, a decrease of the breakdown voltages has been noticed with increasing dynamic performances. As a consequence, the static operating conditions of SiGe HBTs have become steadily restricted by several physical mechanisms.

To that end, a stable-operation-regime (SOR) has been defined which identifies the voltage and current ranges for which the transistor operates without catastrophic failure. It has been shown that the SOR was mainly limited by the snap-back mechanism and the current pinch-in, both induced by the simultaneous activation of the avalanche and self-heating effects. A quick overview of these two transport mechanisms was reported together with the description of other physical effects occurring within the transistor.

Subsequently, a statement of the basic compact models used in the HBT field was presented. Due to its accurate modeling of the transistor electrical behavior, the HiCuM compact model has become one of the most widely used compact models in the semiconductor industry. Regarding the physical effects previously introduced, the HiCuM compact model implements the modeling of impact-ionization mechanism as well as the self-heating effect through an additional node.

Ultimately, the reliability issues in SiGe HBTs were discussed with the presentation of the mixed-mode stress. Since the device operation regime has been extended to higher voltage and current biases, a specific wear-out mechanism can be activated as the hot-carrier degradation leading to an increase of the base current at low injection levels. This degradation mechanism results from the activation of the impact-ionization and the self-heating effects. An accurate modeling of these two mechanisms is then required to extend the validity of compact models as it will be further discussed in the next chapter.

Chapter 2

Compact Modeling of High Biases Mechanisms

Contents

2.1 Introduction

This chapter describes the latest improvements for the compact modeling of high biases mechanisms. Based on a rigorous measurement campaign under DC and AC operating conditions, several limitations of the HiCuM compact model are highlighted for both the avalanche and the self-heating effects. Since these two transport mechanisms are dependent of the device temperature, an accurate extraction procedure for the thermal resistance is reported. Then, a formulation of the multiplication factor is presented extending the validity range up to the second breakdown voltage and for high current densities. Through the extraction of the thermal impedance, a physics-based electrothermal model is derived from the transistor physical structure. Finally, the accuracy of the developed thermal model is validated on both the frequency and the time domain measurement results.

2.2 Limitations of HiCuM compact model

At the beginning of this PhD thesis work, the available version of the HiCuM compact model (v2.34) has demonstrated its versatility over a wide range of technology [65]–[67]. However, as the compact model was originally developed for biases close to BV_{CEO}, several inaccuracies were detected at high voltages and currents [31], beyond the conventional safe-operating-area. Based on DC and AC characterizations, this section focuses on highlighting these model limitations on a SiGe HBT technology.

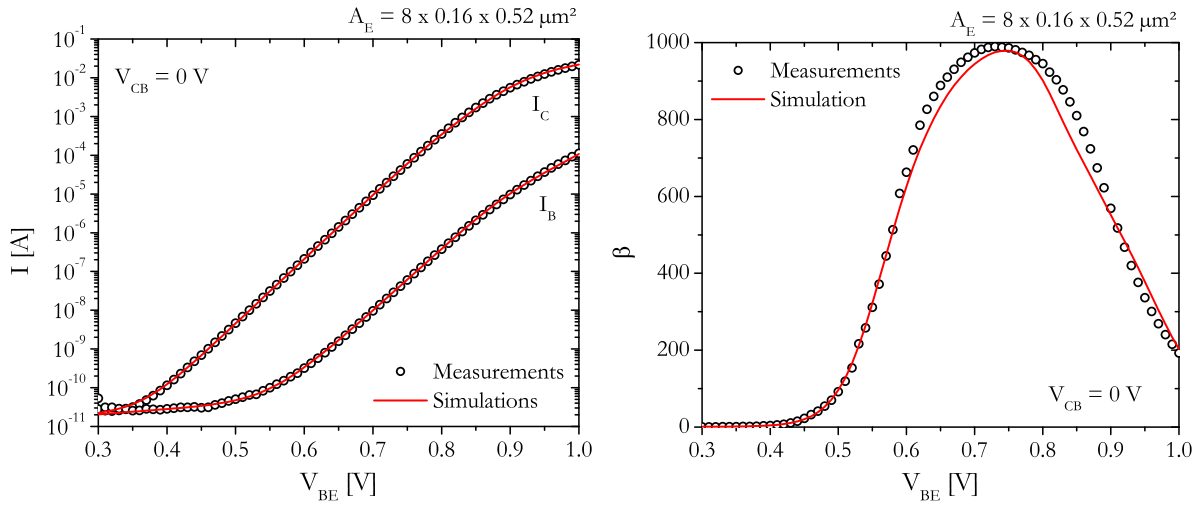


Figure 2.1: Comparison between measurements (symbols) and HiCuM/L2 simulation v2.34 (solid lines) for (a) the forward Gummel characteristic and (b) the current gain at V_{CB} = 0 V on a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

2.2.1 Preliminary assessment

Transistor models for SG13S technology from IHP Microelectronics were generated by a scalable HiCuM library provided by XMOD Technologies (which recently merged with SERMA

technology). The validity of the HiCuM/L2 (v2.34) compact model is verified on both static and dynamic characteristics for a 8 x 0.16 x 0.52 μm^2 device. In the following parts, the measurements are depicted in symbols (black) while the compact model simulation results are presented in solid lines (red).

Gummel

Forward Gummel characteristic is obtained from static measurements at V_{CB} = 0 V and for V_{BE} ranging from 0.3 V to 1 V as shown in figure 2.1a. The wide voltage range allows the effects of low and high injections levels to be observed. From this characteristic, the DC current gain is extracted as illustrated in figure 2.1b. A very good accuracy between the measurements and the simulation results is obtained for both figures.

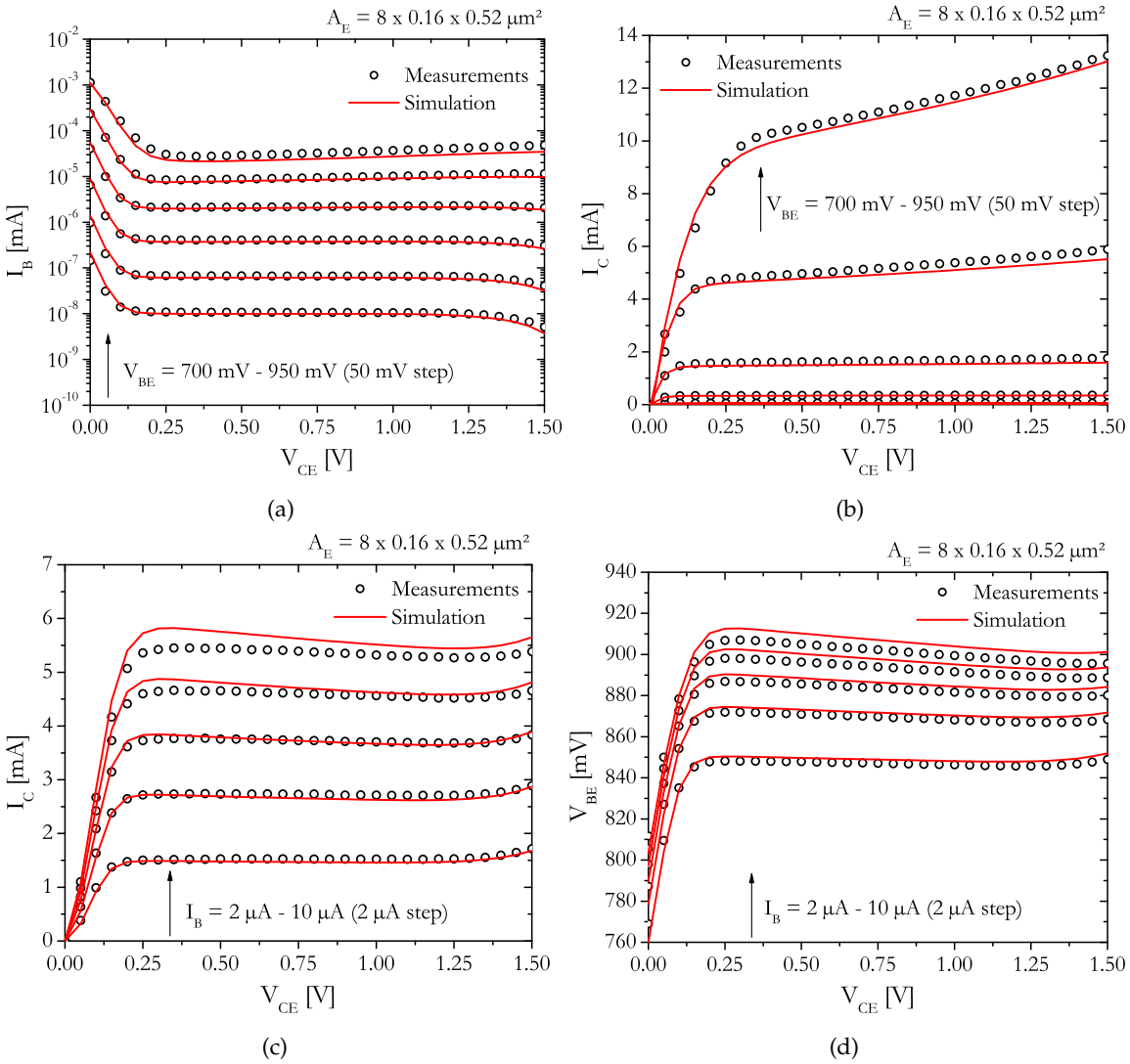


Figure 2.2: Comparison between measurements (symbols) and HiCuM/L2 v2.34 simulation (solid lines) for (a) I_B and (b) I_C as function of V_{CE} under constant V_{BE}'s bias and for (c) I_C and (d) V_B as function of V_{CE} under constant I_B's bias on a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

Output characteristics

The output characteristics allow to verify the modeling of both impact-ionization and self-heating effect for V_{CE}'s below the breakdown voltage, BV_{CEO}. As observed, a very good agreement is obtained between the measurements and the compact model simulation results for: (i) a constant V_{BE} bias as in figures 2.2a and 2.2b and (ii) a constant I_B bias as in figures 2.2c and 2.2d.

Dynamic characteristics

The transit frequency, f_T, and the maximum oscillation frequency, f_{MAX}, are extracted from AC measurements at 10 GHz for different V_{BE} values as depicted in figure 2.3a and figure 2.3b, respectively. The simulation results are in accordance with the measurements for a wide range of V_{BE}'s and V_{CE}'s operating conditions.

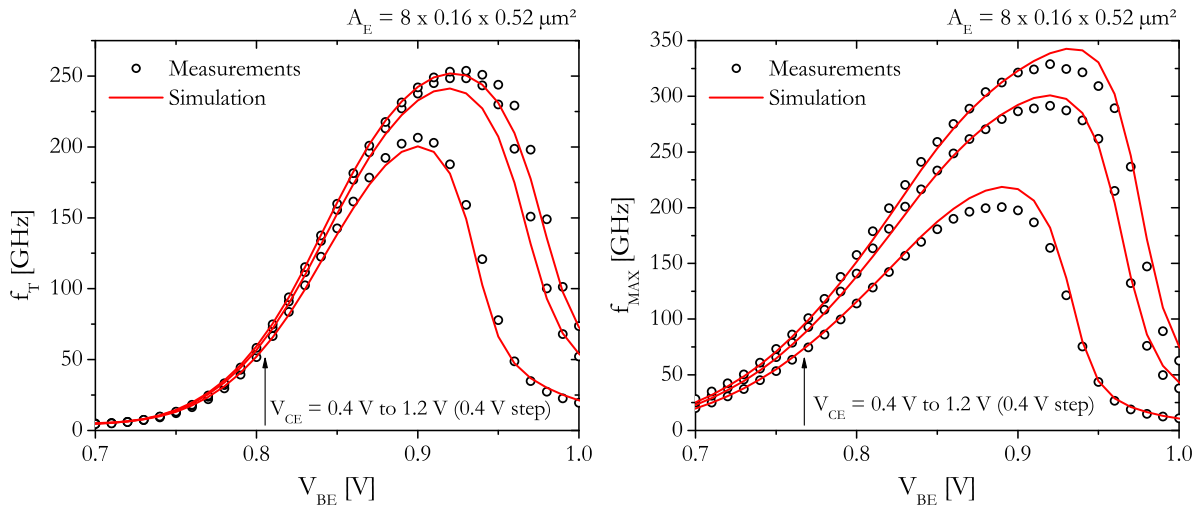


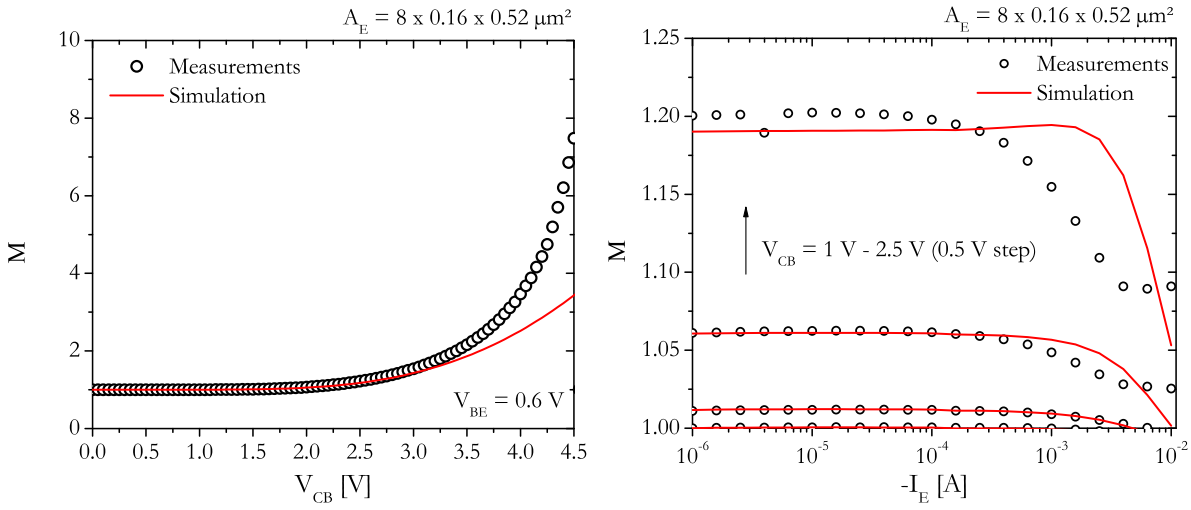
Figure 2.3: Comparison between measurements (symbols) and HiCuM/L2 simulation (solid lines) for (a) f_T and (b) f_{MAX} as function of V_{BE} at various V_{CE}'s bias on a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

Despite the excellent accuracy of the simulation results, some limitations have been observed under high biases, especially beyond BV_{CEO} [31]. Two particular carrier transports mechanisms are activated outside the conventional safe-operating-area, *i.e.* the avalanche and the self-heating effect.

2.2.2 Avalanche effect

As indicated in chapter 1, the calculation of the multiplication factor, M, allows to evaluate the intensity of the avalanche mechanism under several operating conditions. The evolution of this parameter according to the base-collector voltage is displayed in figure 2.4a for a constant V_{BE} of 0.6 V. While the multiplication factor is almost constant up to a V_{CB} value of 2 V, a drastic increase is observed above this voltage bias which is not well captured by the HiCuM

compact model simulation results. This outcome indicates the possibility of a strong avalanche mechanism not yet included in the compact model.



(a) (b)

Figure 2.4: Comparison between measurements (symbols) and HiCuM/L2 simulation v2.34 (solid lines) for the multiplication factor, M, at (a) various V_{CB} under a constant V_{BE} and (b) various I_E under constant V_{CB}'s on a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

A similar approach is performed in figure 2.4b with the evolution of the multiplication factor as function of the emitter current, I_E, for various V_{CB} values ranging from 1 V to 2.5 V. From this plot, one observes a drop in the M parameter for emitter currents bias beyond I_E = 100 μA which indicates a current dependence of the impact-ionization mechanism. While low injection currents are accurately modeled using the HiCuM compact model, a lack of validity is highlighted for high injection levels.

2.2.3 Self-heating effect

The representative parameter for the thermal behavior of active electronic components is the thermal impedance, Z_{TH}, obtained from low-frequency S-parameter measurements. In conventional HiCuM compact model, it is modeled by an equivalent single pole R-C network composed of one thermal resistance, R_{TH}, and one thermal capacitance, C_{TH}. The thermal resistance allows to estimate the temperature rise within the device under static operating conditions while the thermal capacitance is used to model the thermal AC behavior.

The simulation results of such a circuit is compared to the measurements ones on figure 2.5a for the magnitude and on figure 2.5b for the phase of the thermal impedance. One can observe that the frequency behavior of the thermal impedance is not accurately reproduced by the compact model, except for the very-low frequencies (*i.e.* where the thermal impedance reaches the thermal resistance value).

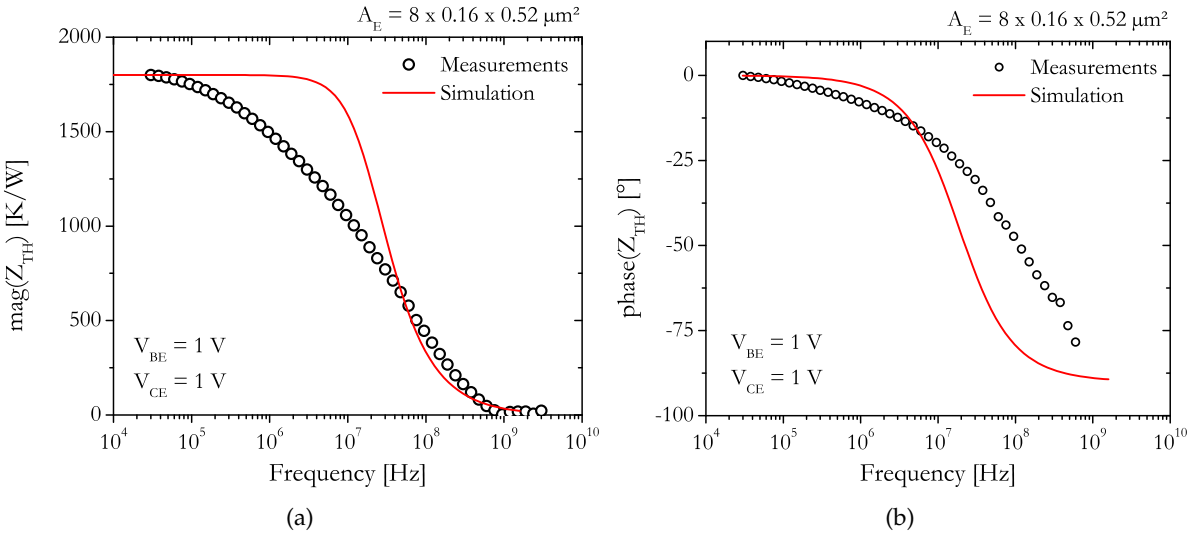


Figure 2.5: Comparison between measurements (symbols) and HiCuM/L2 simulation v2.34 (solid lines) for the thermal impedance (a) magnitude and (b) phase evolution according to the frequency on a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

Several limitations of the HiCuM compact model have been demonstrated in this section. More especially, a lack of validity for the modeling of the avalanche mechanism is pointed out for biases outside the safe-operating-area. The measurements results have shown the presence of a strong avalanche mechanism under high electric field that must be accounted for within the compact model. Moreover, a current dependence of the multiplication factor formulation has emerged leading to a roll-off of the avalanche effect at high current densities. Finally, large inaccuracies have been highlighted for the modeling of the transistor dynamic thermal behavior which, therefore, deserved to be further improved.

2.3 DC characterization of self-heating effect

The device temperature rise due to self-heating effect influences the electrical behavior of SiGe HBTs. Under static operating conditions, the device dissipated power, P_{diss}, can be easily determined according to equation (2.1).

$$P_{diss} = I_C V_{CE} + I_B V_{BE} \tag{2.1}$$

In order to calculate the device temperature rise, the thermal resistance (see equation (1.6)) must be accurately extracted from DC electrical measurements. One common approach is the use of the base-emitter voltage (V_{BE}) as a thermometer [68]. However, the scope of application is limited to low P_{diss} regime which isn't recommended for SiGe HBTs for which high current densities are standard operating conditions. Moreover, the extracted R_{TH} is overestimated since it includes the temperature variation of the series resistances (R_E and R_{Cx}) [69]. Therefore, this section will focus on the intersection technique [70] applicable at high current densities. Based on a differential approach, the effect of the temperature from other parameters

than R_{TH} is canceled. This methodology has already been tested on multiple devices from B55 technology [69] ensuring a high level of accuracy for the thermal resistance extraction together with its temperature dependence. In this section, the intersection technique is applied on four SG13S technology devices from IHP Microelectronics.

2.3.1 Methodology

Under a forward active operation mode, neglecting both the Early and the avalanche effects, the collector current, I_C, is expressed from equation (2.2) [46] taking into account its dependence on the junction temperature.

$$I_C(V_{BE}, T_j) = I_S(T_j) exp\left(\frac{qV_{BE}}{kT_j}\right) \tag{2.2}$$

where k is the Boltzmann constant, q is the electron charge and I_S is the saturation current.

Assuming two Gummel plots obtained at two different ambient temperatures ($T_{amb,1}$ and $T_{amb,2}$) and two collector-emitter voltages ($V_{CE,1}$ and $V_{CE,2}$), the intersection point of these two curves corresponds to a same I_C and V_{BE}, as illustrated in figure 2.6a. Consequently, following equation (2.2), the junction temperature at this particular point is the same for both operating conditions, as illustrated in figure 2.6b.

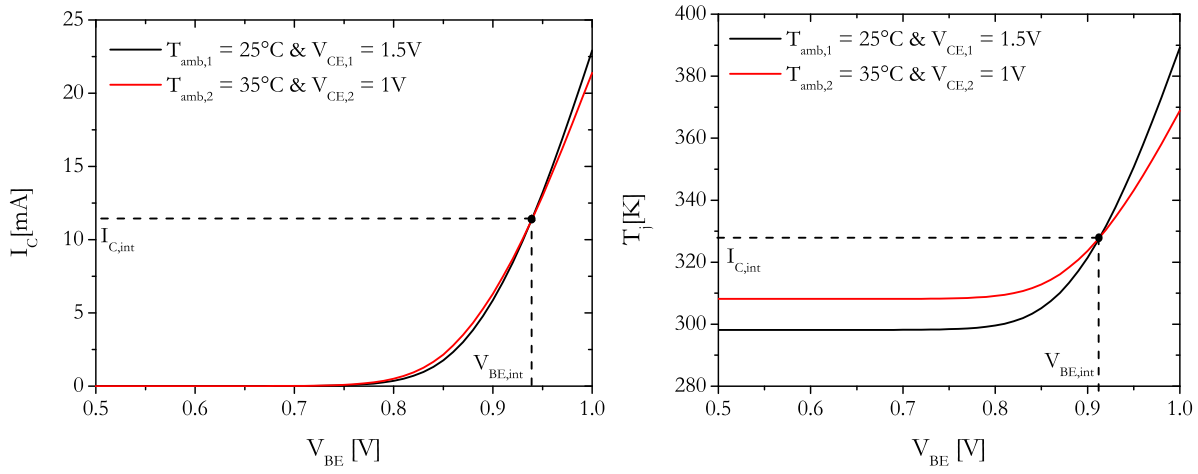


Figure 2.6: Measurement results of (a) forward Gummel behavior illustrating the intersection technique and (b) corresponding junction temperature on a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

Nevertheless, as different V_{CE}'s are used for the extraction procedure, the dissipated power is not the same between the two curves. Therefore, the junction temperature can be expressed with a set of two equations (2.3) and (2.4).

$$T_j = T_{amb,1} + P_{diss,1} R_{TH} \tag{2.3}$$

$$T_j = T_{amb,2} + P_{diss,2} R_{TH} \tag{2.4}$$

Equating (2.3) and (2.4), an expression for R_{TH} is obtained as,

$$R_{TH} = \frac{T_{amb,2} - T_{amb,1}}{P_{diss,1} - P_{diss,2}} \tag{2.5}$$

By introducing a first order form of the dissipated power, $P_{diss} = I_C V_{CE}$, equation (2.5) can be read as,

$$R_{TH} = \frac{T_{amb,2} - T_{amb,1}}{I_{C,int}(V_{CE,1} - V_{CE,2})} \tag{2.6}$$

where $I_{C,int}$ denotes the collector current value at the intersection point. The corresponding junction temperature can further be easily calculated either from equation (2.3) or (2.4).

2.3.2 Extraction results

The extraction procedure is performed on the four devices under test (DUTs) from IHP Microelectronics reported in table 2.1 where W_E is the emitter width, L_E is the emitter length, N_X is the number of emitter fingers and A_E is the emitter area.

W_E [μm]	L_E [μm]	N_X	A_E [μm^2]
0.16	0.52	4	0.33
0.16	0.88	4	0.56
0.16	0.52	8	0.67
0.16	0.88	8	1.13

Table 2.1: Geometry features for the devices under test corresponding to SG13S technology from IHP Microelectronics.

A set of ambient temperatures ranging from 15°C to 55°C with a 10°C step and for $V_{CE,1}$ = 1 V and $V_{CE,2}$ = 1.5 V is applied allowing to extract the thermal resistance evolution according to its temperature dependency. Figure 2.7a presents the extraction results on a 4 x 0.16 x 0.88 μm^2 transistor for different junction temperatures. A linear dependency between the two parameters is observed which is in accordance with the theory. Indeed, the temperature dependence of the thermal resistance in HiCuM compact model is described as,

$$R_{TH}(T) = R_{TH}(T_0)[1 + \alpha_{R_{TH}}(T_j - T_0)] \tag{2.7}$$

where $\alpha_{R_{TH}}$ is the thermal resistance proportionality coefficient and $R_{TH}(T_0)$ is the thermal resistance value at T_j=T_0 where T_0 corresponds to the temperature at which the HiCuM model

parameters are extracted. The data points from figure 2.7a are fitted with a linear function (red curve) allowing to evaluate the model parameters, $\alpha_{R_{TH}}$ and $R_{TH}(T_0)$, of equation (2.7).

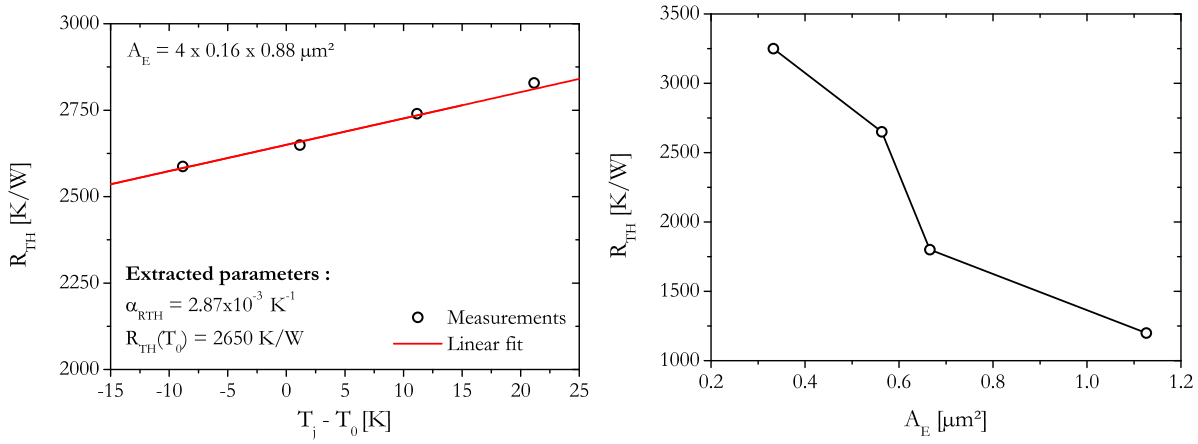


Figure 2.7: Thermal resistance evolution according to (a) the device temperature and (b) the emitter area for SG13S technology from IHP Microelectronics. The extraction is performed based on the intersection technique.

The extraction procedure is performed for different active emitter areas as depicted in figure 2.7b. The R_{TH} value increases with emitter area decrease as already reported in the literature [71]–[74]. This result demonstrates the thermal issues for highly integrated devices featuring a drastic increase of the thermal resistance, and, consequently, of the junction temperature. As a comparison, using the exact same extraction procedure, a thermal resistance value of 4100K/W was extracted in [69] for a B55 technology device from ST Microelectronics featuring $A_E = 1\ \mu m^2$. For IHP Microelectronics, regarding the results from figure 2.7b, the thermal resistance value for $A_E = 1\ \mu m^2$ can be estimated to be around 1250 K/W and 1500 K/W, which is, at least, 2.5 times lower than for ST Microelectronics. This reduced thermal budget for IHP Microelectronics is due its particular architecture which, unlike ST Microelectronics, does not integrate shallow trench isolation between the intrinsic transistor and the collector contact, as already presented in section 1.3.2 and 1.7.

2.3.3 Implementation in compact models

According to equation (2.3), the temperature rise within the device under static operating conditions can be estimated by knowing the electrical dissipated power. In HiCuM/L2, the expression of P_{diss} differs depending on a self-heating flag, FLSH [46], as

- FLSH = 0, the self-heating is turned off and the device temperature equals to the ambient temperature.
- FLSH = 1, only the most relevant dissipative elements are considered for the calculation of P_{diss} as,

$$P_{diss} = I_T V_{C'E'} + I_{AVL}(V_{DCi} - V_{B'C'}) \tag{2.8}$$

where I_T is the transfer current, I_{AVL} is the avalanche current and V_{DCi} is the internal base-collector built-in potential.

- FLSH = 2, all relevant dissipative elements (*i.e.* excluding any energy storage elements) are considered for the calculation of P_{diss} as,

$$P_{diss} = I_T V_{C'E'} + I_{AVL}(V_{DCi} - V_{B'C'}) + \sum I_{jd} V_{diode} + \sum \frac{\Delta V_n^2}{r_n} \tag{2.9}$$

where I_{jd} are the diode currents (with d=BEi,BCi,BEp,BCx,SC), V_{diode} are the respective diode voltages, r_n are the series resistances and ΔV_n are the corresponding voltages drop across those resistances (with n=Bi,Bx,E,Cx).

Regarding equations (2.8) and (2.9), the increase of the dissipated power is also influenced by the impact-ionization mechanism which increases the output collector current. Hence, a special attention must be paid to the modeling of this particular physical effect, aspect that will be developed in the upcoming section. Moreover, as highlighted in section 2.2, some voltage and current dependencies of the multiplication factor were not yet well captured by the compact modeling at the beginning of this thesis work. Therefore, an accurate formulation of this parameter is required to extend the model accuracy to higher voltage and current ranges. For the rest of the manuscript, the self-heating flag is set to FLSH = 2.

2.4 Compact modeling of avalanche effect

In section 2.2, it has been highlighted a decreased of the impact-ionization rate under medium and high injection levels which may be caused by two physical mechanisms namely the self-heating and the high-current effects. Indeed, due to the device temperature rise resulting from self-heating effect, the lattice vibration is enhanced leading to a reduced mean free path for electron and hole [75]. As a result, the carriers do not accumulate enough energy to generate electron-hole pairs by collision with Si. Moreover, under high current levels, an impact-ionization mitigation occurs which is caused by (i) a reduced internal voltage across the BC-SCR due to the voltage drop across the external collector resistance and (ii) the Kirk effect which leads to a decrease of the electric field in the BC junction [35].

Various semi-empirical formulations have been developed for the modeling of the multiplication factor describing its dependence upon the collector-base voltage V_{CB} [76]–[79]. However, in [76], [77], the impact-ionization mitigation due to self-heating or high-current effects is not accounted for. Some correction terms were included in [78] for both effects and in [79] for high-current effect only, but were not validated against measurement results. Regarding standard compact models, both the high-current and self-heating effects were recently introduced in the

latest version of the HiCuM/L2 compact model version 3.0.0 [35], [75] together with a formulation for the strong avalanche behavior presented in the previous version 2.4 [80]. The next section describes the corresponding formulation of the multiplication coefficient together with an accurate parameter extraction procedure.

2.4.1 Model formulation

In the last version of HiCuM compact model (v3.0.0), the multiplication coefficient is described as follows [35], [75], [80],

$$M - 1 = \frac{g}{1 - k_{AVL} g} \tag{2.10}$$

with

$$g_{AVL} = f_{AVL}(V_{DCi} - V_{B'C'}) e^{\frac{-q_{AVL}}{f_{HC,H} C_{jci}(V_{DCi} - V_{B'C'})}} \tag{2.11}$$

where f_{AVL} and q_{AVL} are the weak avalanche model parameters, V_{DCi} is the internal B-C built-in potential and C_{jci} is the B-C depletion capacitance, given by

$$C_{jCi} = \frac{C_{jCi0}}{(1 - \frac{V_{BC}}{V_{DCi}})^{z_{Ci}}} \tag{2.12}$$

The k_{AVL} parameter modeling the strong avalanche behavior has been introduced in [80]. Note that the strong avalanche behavior can be turned off by setting $k_{AVL} = 0$. The improved formulation has further been implemented in HiCuM/L2 compact model (v2.4). Figure 2.8a presents a comparison between the measurements (symbols) obtained on a 8 x 0.16 x 0.52 μm^2 device from IHP Microelectronics and the compact model simulation results (solid lines) of the base current and the multiplication factor using the strong avalanche modeling. The new model version demonstrates an excellent accuracy up to BV_{CBO}. The $f_{HC,H}$ parameter allows to model the high current effects on the multiplication coefficient and takes into account the electric field profile [35]. The implemented expression in HiCuM/L2 v3.0.0 is given in [75],

$$f_{HC,C} = \sqrt{s_M \ln\left[\exp\left(\frac{C_{jCi}/C_{jCi0}}{s_M}\right) - 2 + 2\cosh\left(\frac{1 - I_T/I_{LIMeff}}{s_M}\right)\right]} \tag{2.13}$$

where s_M is a smoothing factor (ranging from 0 to 1) needed to link the low and high-current formulations of the multiplication factor and I_{LIMeff} is the current and depth dependent limit current to the Kirk effect onset, expressed as

$$I_{LIMeff} = h_{CAVL} I_{LIM} + h_{VDAVL} I_T \tag{2.14}$$

where h_{CAVL} accounts for the collector doping profile influence on I_{LIM} and h_{VDAVL} accounts for the injection level influence on the avalanche. Note that the high current effects can be disabled by setting $f_{HC,C}$ = 1. Figure 2.8b presents a comparison between the measurements (symbols) and the compact model simulation results (solid lines) of the base current and the multiplication factor using the current dependent formulation of the multiplication coefficient. An improved accuracy is obtained with the new model version (v.3.0.0) compared to the former one (v2.4.0) for moderate and high current levels. Now that the formulation of the multiplication factor is improved at high voltages (through the strong avalanche mechanism) and high currents (through the current dependence of the avalanche effect), an extraction procedure dedicated to the avalanche model parameters has to be settled.

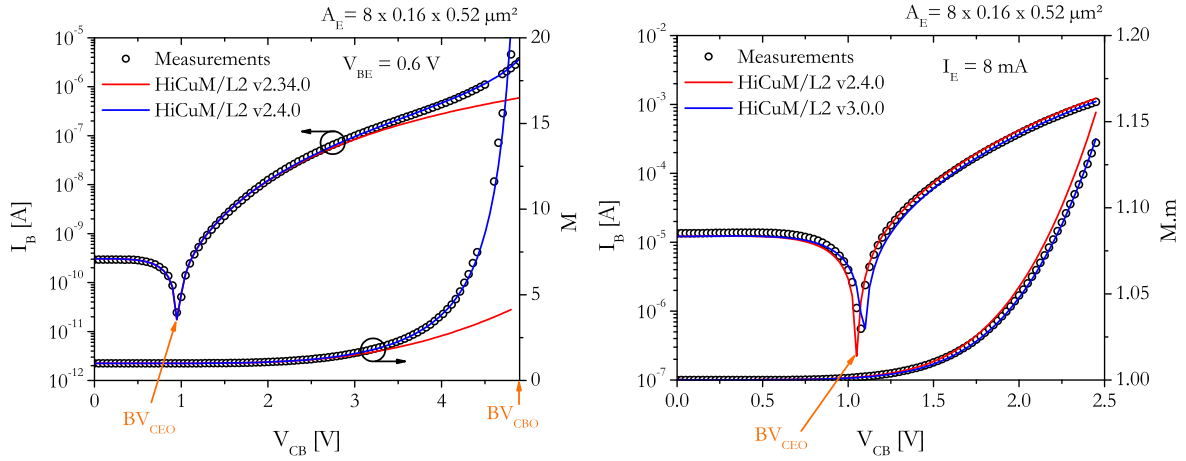


Figure 2.8: Comparison between measurements (symbols) and compact model simulation results (solid lines) of (a) HiCuM/L2 v2.34 (in red) and v2.4.0 (in blue) at V_{BE} = 0.6 V and (b) HiCuM/L2 v2.4.0 (in red) and v3.0.0 (in blue) at I_E = 8 mA for the base current and the multiplication factor on a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

2.4.2 Parameter extraction

The parameter extraction flow is detailed in figure 2.9 [31] which relies on the preliminary accurate extraction of the other HiCuM compact model parameters [81]–[84]. Concerning the avalanche model parameters, the extraction procedure is divided into three main parts: (i) the weak avalanche parameters, f_{AVL} and q_{AVL}, and their related thermal coefficients, AL_{FAV}, AL_{QAV}, (ii) the strong avalanche parameter, k_{AVL} together with its thermal coefficient, AL_{QAV} and (iii) the high current avalanche parameters, h_{CAVL} and h_{VDAVL}. The parameter extraction is detailed for a 8 x 0.16 x 0.52 μm^2 device from IHP Microelectronics SG13S technology.

Weak avalanche parameters

Since the weak avalanche only occurs at voltage close to the BV_{CEO}, the strong avalanche is not activated and is consequently disabled (k_{AVL} = 0) for the extraction of the weak avalanche parameters. Moreover, the high current effects are neglected (*i.e.* $f_{HC,H}$ = 1) since the parameter

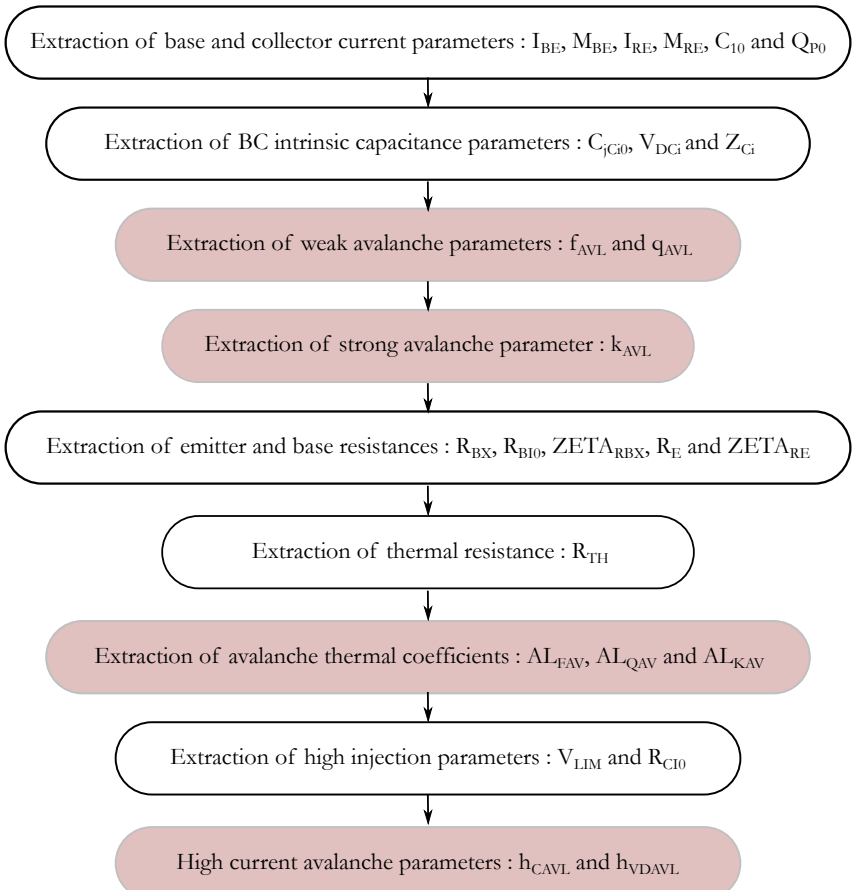


Figure 2.9: Extraction flow the avalanche related parameters reproduced from [31].

extraction is performed for low injection levels. The range of extraction for f_{AVL} and q_{AVL} parameters is detailed in figure 2.10a and is limited to low and moderate V_{CB} values. Assuming that at low current densities, the V_{BC} is close to $V_{B'C'}$, the logarithm form of equation 2.10 leads to,

$$\ln\left(\frac{M-1}{V_{DCi}-V_{BC}}\right) = \ln\left(f_{AVL}\right) - \frac{q_{AVL}(V_{DCi}-V_{BC})}{C_{jci0}V_{DCi}^{z_{Ci}}} \tag{2.15}$$

where C_{jCi0} is the zero-bias and z_{Ci} is the exponent factor of the base-collector capacitance. Since, equation (2.15) presents a linear dependency, the parameters f_{AVL} and q_{AVL} are extracted respectively from the intercept and the slope of the linear regression as illustrated in figure 2.10b.

Moreover, the two weak avalanche model parameters exhibit a conventional temperature dependence which is expressed as,

$$X_{AVL}(T) = X_{AVL}(T_0)e^{AL_{XAV}(T-T_0)} \tag{2.16}$$

where X_{AVL} is the term that represents the weak avalanche parameters (f_{AVL} and q_{AVL}), T_0 is the

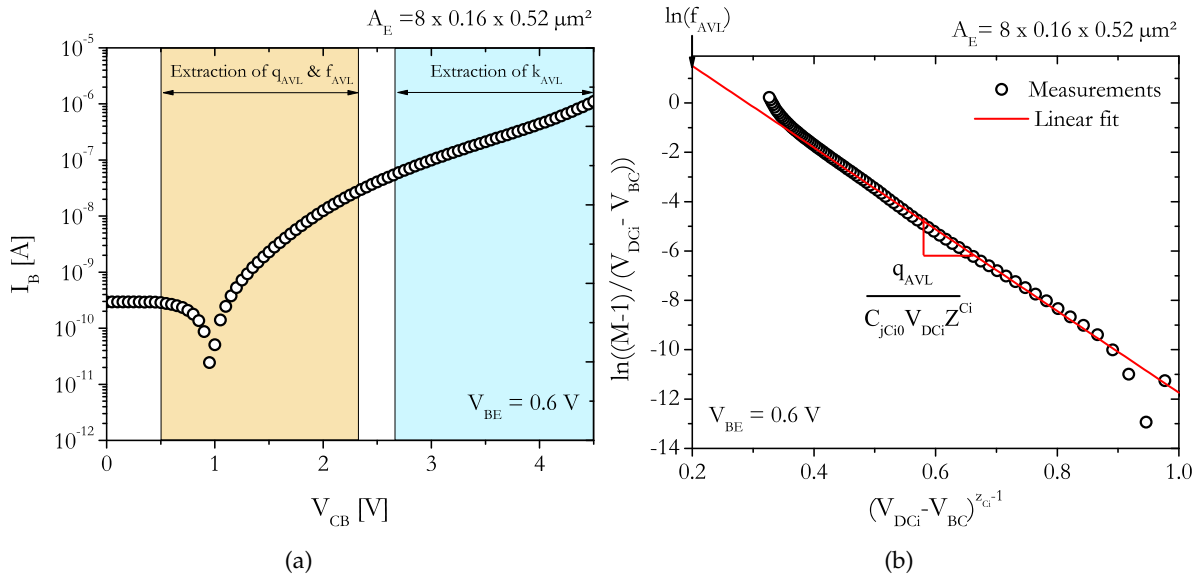


Figure 2.10: Illustration of the extraction (a) range and (b) methodology for the weak avalanche parameters (f_{AVL} and q_{AVL}) on a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

reference extraction temperature (T_0 = 27 °C) and AL_{XAV} is the related thermal coefficient. The extraction procedure is therefore repeated for different ambient temperatures ranging from [-25°C;100] °C with a 25°C step. Then, the logarithm form of equation (2.16) (see equation (2.17)) is plotted according to the temperature evolution for f_{AVL} parameter in figure 2.11a and q_{AVL} parameter in figure 2.11b. The thermal coefficients of the weak avalanche parameters is directly extracted from the slope of the linear fitting function.

$$\ln(X_{AVL}(T)) = \ln(X_{AVL}(T_0)) + AL_{XAV}(T - T_0) \tag{2.17}$$

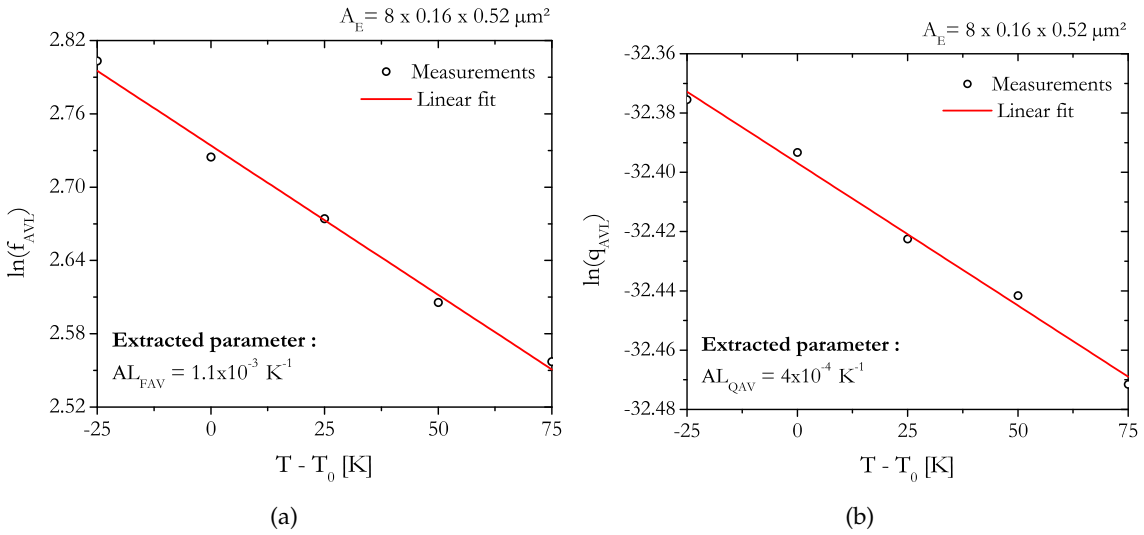


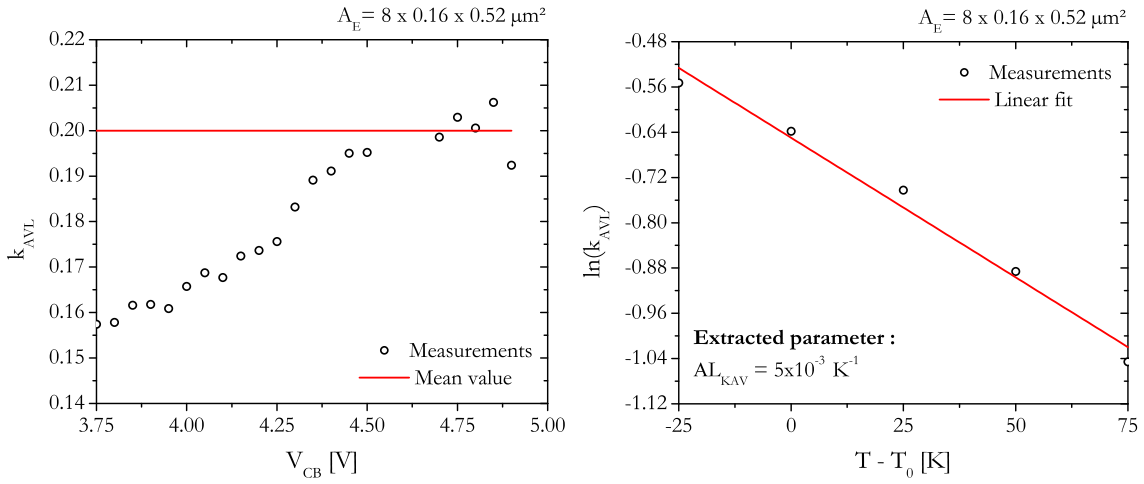
Figure 2.11: Thermal coefficient extraction for (a) f_{AVL} and (b) q_{AVL} parameters for a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

Strong avalanche parameters

Next, knowing the weak avalanche parameters, the strong avalanche one can be extracted according to equation (2.18) for V_{CB} close to the BV_{CBO}.

$$k_{AVL} = \frac{1}{g} - \frac{1}{M-1} \tag{2.18}$$

The extraction procedure of k_{AVL} is displayed in figure 2.12a where it reaches a constant value for V_{CB} values ranging from 4.7 V to 5 V. Therefore, a mean value of 0.2 is extracted for the selected extraction range. The evolution of k_{AVL} according to the temperature is depicted in figure 2.12b where a negative dependence is observed for the technology under test in the temperature range of -25°C to 100°C.



(a) (b)

Figure 2.12: (a) k_{AVL} extraction result and (b) associated thermal coefficient for a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

Avalanche current dependency

The extraction procedure for the avalanche current dependency model is more complicated than for the weak and strong avalanche one due to the the multiple occurrence of second-order phenomena such as self-heating. Therefore, due to the self-heating impact on the electrical characteristics, it is recommended to perform an optimization procedure using the Levenberg-Marquardt algorithm for h_{CAVL} and h_{VDAVL} parameters based on a constant I_E setup configuration [75].

2.4.3 Simulation results

Figure 2.13 presents the base current evolution according to the collector-base voltage under various operating conditions which allows to evaluate the model accuracy on various devices from SG13S technology from IHP Microelectronics. Note that, to avoid a transistor catastrophic

failure, a current compliance has been set up during the measurement campaign on both the base and the collector current.

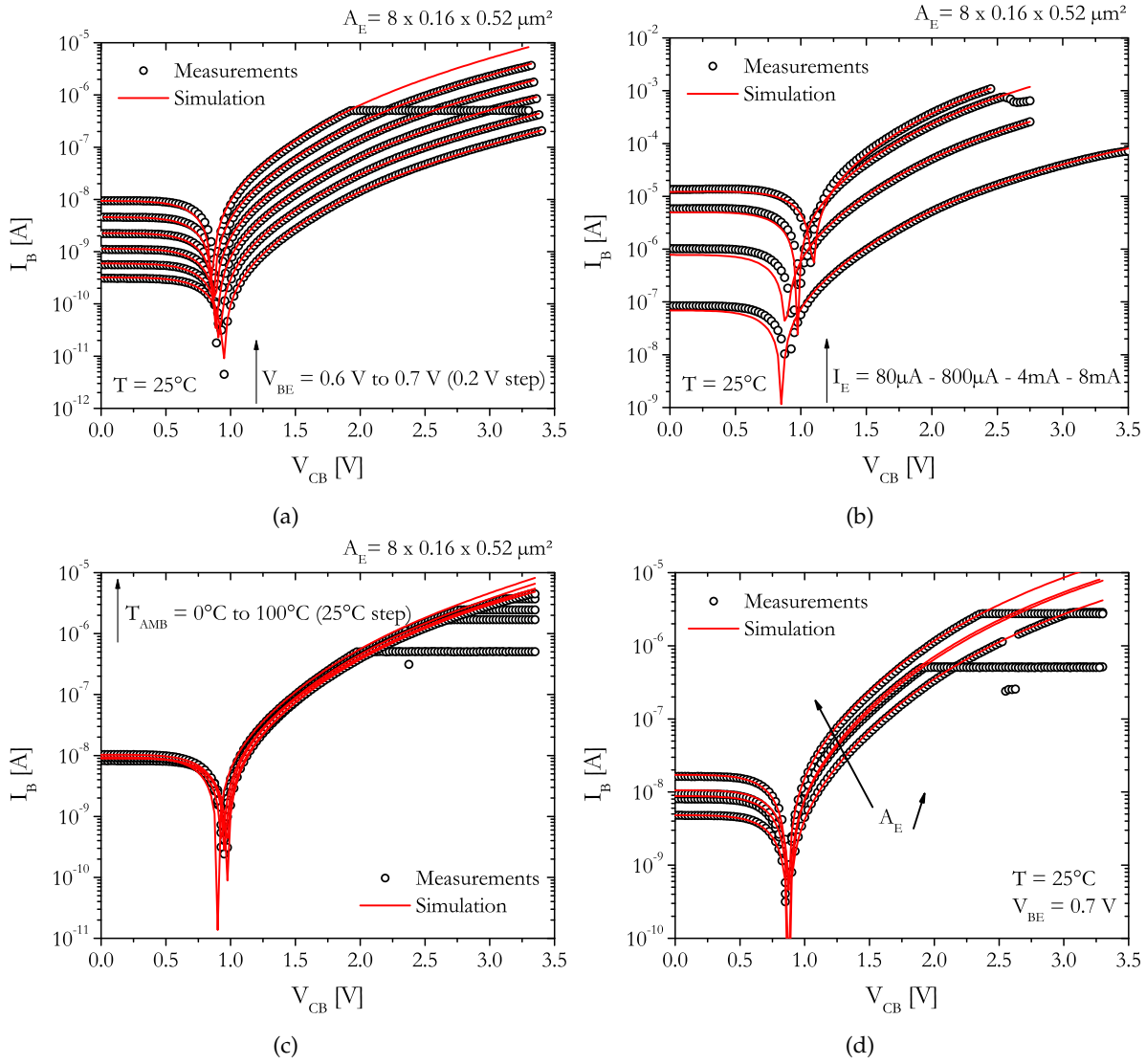


Figure 2.13: Compact model simulations results (solid lines) vs measurements (symbols) for I_B evolution according to V_{CB} at (a) various V_{BE} values, (b) various I_E values, (c) various T_{AMB} and (d) various emitter dimensions corresponding to SG13S technology from IHP Microelectronics. A current compliance is used to avoid the transistor destruction.

A good agreement between compact model simulation results and measurements is depicted in figure 2.13a for V_{BE} values ranging from 0.6 V to 0.7 V and for V_{CB} values up to 3.5 V. This result highlights an accurate modeling of the strong avalanche behavior. Then, the DUT is tested under various I_E ranging from low injection levels (80 μA) to high injection ones (8 mA) as shown in figure 2.13b. A good prediction of the base current evolution is also obtained under these operating conditions. In figure 2.13c, the temperature dependence of the avalanche mechanism is also well captured for ambient temperatures ranging from 0°C to 100°C. Finally, the model formulation is verified on various emitter dimensions (see table 2.1 for the geometry

features) for a V_{BE} value of 0.7 V. A good agreement between the measurements and the simulation results is obtained for the four DUTs area ensuring the scalability of the multiplication coefficient parameter extraction.

2.5 AC characterization of self-heating effect

The dynamic thermal behavior must be investigated in order to predict the temperature rise within the transistor according to the input frequency [78]. At high frequencies, above the thermal cut-off frequency (f_{TH}), the temperature is determined by the static power dissipation obtained under DC operating conditions. In this region, the device behavior is only dominated by its electrical characteristics. At low frequencies, below f_{TH}, the junction temperature varies according to the dissipated power, leading to a harmonic electrothermal feedback. Accordingly, the low-frequency range behavior is dominated by the dynamic self-heating where the device thermal impedance, Z_{TH}, can be extracted from low-frequency S-parameters measurements. Several approaches to extract the thermal impedance are reported in the literature derived from Y [85]–[88] or H-parameters [89]–[91]. In this section, the study focuses on the thermal impedance extraction from Y-parameters.

2.5.1 Methodology

The methodology presented below is close from the one reported in [87], [92]. The currents of the base (I_B) and the collector (I_C) terminals can be considered as functions of the base-emitter voltage (V_{BE}), the collector-emitter voltage (V_{CE}) and the operating temperature (T).

$$\begin{aligned} I_B &= F_1(V_{BE}, V_{CE}, T) \\ I_C &= F_2(V_{BE}, V_{CE}, T) \end{aligned} \tag{2.19}$$

The expression of the operating temperature is given in equation (2.20) where T_{amb} is the ambient temperature, R_{TH} is the thermal resistance and P_{dc} is the dissipated electrical power in DC operating conditions calculated as $P_{dc} = I_C V_{CE} + I_B V_{BE}$ (the contribution of the series resistance are neglected) [87].

$$T = T_{amb} + P_{dc} R_{TH} \tag{2.20}$$

Under a small signal excitation around the dc bias point, the total base (collector) current is given as $I_B + \Delta i_b$ ($I_C + \Delta i_c$) and the base (collector) voltage is given as $V_{BE} + \Delta v_{be}$ ($V_{CE} + \Delta v_{ce}$). The small-signal increments Δi_b and Δi_c to their corresponding values can be expressed as in equation (2.21) omitting the temperature dependence associated with the small-signal capacitances.

$$\begin{aligned}\Delta i_b &= Y_{11}|_{V_{CE},T}\,\Delta v_{be} + Y_{12}|_{V_{BE},T}\,\Delta v_{ce} + \left.\frac{\delta I_B}{\delta T}\right|_{V_{BE},V_{CE}} \Delta t \\ \Delta i_c &= Y_{21}|_{V_{CE},T}\,\Delta v_{be} + Y_{22}|_{V_{BE},T}\,\Delta v_{ce} + \left.\frac{\delta I_C}{\delta T}\right|_{V_{BE},V_{CE}} \Delta t\end{aligned} \tag{2.21}$$

where Y_{11}, Y_{12}, Y_{21} and Y_{22} denote the isothermal values of the Y-parameters evaluated at fixed DC bias. The change in the device operating temperature under a small-signal operation is given as [46]

$$\Delta t = Z_{TH}(\omega)\Delta p \tag{2.22}$$

where Z_{TH} is the thermal impedance, ω is the angular frequency and Δp is the small-signal increment to P_{dc}. Therefore, the total junction temperature can be calculated as,

$$T_j = T + \Delta t = T_{amb} + P_{dc}R_{TH} + \Delta p Z_{TH}(\omega) \tag{2.23}$$

The overall dissipated power P_{diss} is expressed as,

$$\begin{aligned}P_{diss} = (I_C + Re\{\Delta i_c\})(V_{CE} + \Delta v_{ce}) + (I_B + Re\{\Delta i_b\})(V_{BE} + \Delta v_{be}) \\ P_{diss} = P_{dc} + \Delta p\end{aligned} \tag{2.24}$$

where

$$\Delta p = I_C\Delta v_{ce} + I_B\Delta v_{be} + V_{CE}Re\{\Delta i_c\} + V_{BE}Re\{\Delta i_b\} \tag{2.25}$$

The products $\mathrm{Re}\{\Delta i_c\}\Delta v_{ce}$ and $\mathrm{Re}\{\Delta i_b\}\Delta v_{be}$ in equation (2.24) are ignored as their contribution to (2.25) is minor. The expressions of $\mathrm{Re}\{\Delta i_c\}$ and $\mathrm{Re}\{\Delta i_b\}$ are derived from equation (2.21) as

$$\begin{aligned}Re\{\Delta i_b\} &= \frac{\delta I_B}{\delta V_{BE}}\Delta v_{be} + \frac{\delta I_B}{\delta V_{CE}}\Delta v_{ce} + \frac{\delta I_B}{\delta T}\Delta t \\ Re\{\Delta i_c\} &= \frac{\delta I_C}{\delta V_{BE}}\Delta v_{be} + \frac{\delta I_C}{\delta V_{CE}}\Delta v_{ce} + \frac{\delta I_C}{\delta T}\Delta t\end{aligned} \tag{2.26}$$

As presented in [85], [87], [88], the thermal impedance is extracted from Y-parameters measurement, more especially, from Y_{22} parameter since it is the most affected by self-heating (compared to the other Y-parameters) and also ensure reliable extraction at high frequencies. Considering $\Delta v_{be} = 0$, the Y_{22} parameter is derived from equation (2.21) as

$$Y_{22}(\omega) = Y_{22}|_{V_{BE},T} + \left.\frac{\delta I_C}{\delta T}\right|_{V_{BE},V_{CE}} \frac{\Delta t}{\Delta v_{ce}} \tag{2.27}$$

To obtain $\Delta t/\Delta v_{ce}$, equation (2.26) is substituted in (2.25) with $\Delta v_{be} = 0$ leading to an expression of Δp as

$$\Delta p = \Delta v_{ce}\left(I_C + V_{CE}\frac{\delta I_C}{\delta V_{CE}} + V_{BE}\frac{\delta I_B}{\delta V_{CE}}\right) + \Delta t\left(V_{CE}\frac{\delta I_C}{\delta T} + V_{BE}\frac{\delta I_B}{\delta T}\right) \tag{2.28}$$

Equation (2.28) is incorporated in equation (2.22) leading to an expression of the thermal admittance $Y_{TH}(\omega) = 1/Z_{TH}(\omega)$ as

$$Y_{TH}(\omega) = \frac{\Delta v_{ce}}{\Delta t}\left(I_C + V_{CE}\frac{\delta I_C}{\delta V_{CE}} + V_{BE}\frac{\delta I_B}{\delta V_{CE}}\right) + V_{CE}\frac{\delta I_C}{\delta T} + V_{BE}\frac{\delta I_B}{\delta T} \tag{2.29}$$

Replacing $\Delta vce/\Delta t$ according to equation (2.27) and neglecting the last two terms of (2.29) [87], the thermal impedance expresses as

$$Z_{TH}(\omega) = \frac{Y_{22}(\omega) - Y_{22}|_{V_{BE},T}}{\frac{\delta I_C}{\delta T}\left(I_C + V_{CE}\frac{\delta I_C}{\delta V_{CE}} + V_{BE}\frac{\delta I_B}{\delta V_{CE}}\right)} \tag{2.30}$$

For an angular frequency $\omega \to 0$, $Z_{TH}(\omega) \to R_{TH}$. Therefore, the thermal impedance can be written depending on the thermal resistance value as,

$$Z_{TH}(\omega) = R_{TH}\frac{Y_{22}(\omega) - Y_{22}^{AC}}{Y_{22}^{DC} - Y_{22}^{AC}}\frac{I_C + V_{BE}Y_{12}^{DC} + V_{CE}Y_{22}^{DC}}{I_C + V_{BE}Y_{12}(\omega) + V_{CE}Y_{22}(\omega)} \tag{2.31}$$

where $Y_{22}^{ac} = Y_{22}|_{V_{BE},T}$ corresponds to the isothermal value of Y_{22} parameter and Y_{12}^{dc} (Y_{22}^{dc}) is the value of Y_{12} (Y_{22}) parameter evaluated at $\omega \to 0$.

2.5.2 Low-frequency S-parameters measurement

In order to extract the thermal impedance according to the methodology presented in the previous section, low-frequency S-parameters measurements are performed using a semiconductor parameter analyzer, HP 4155, to set the DC bias points and a vector network analyzer, Agilent E5061B (5 Hz-3 GHz), for the RF input power as illustrated in figure 2.14. Bias tees (with a corresponding bandwidth between 30 kHz and 3 GHz) are added at the base and the collector terminal to couple both RF and DC bias. A standard SOLT calibration is used with an RF input power of -30 dBm followed by an open-short de-embedding procedure. Since it is only desired to observe the self-heating effect, the DC bias point is settled at V_{BE} = V_{CE} = 1 V to neutralize the impact ionization mechanism.

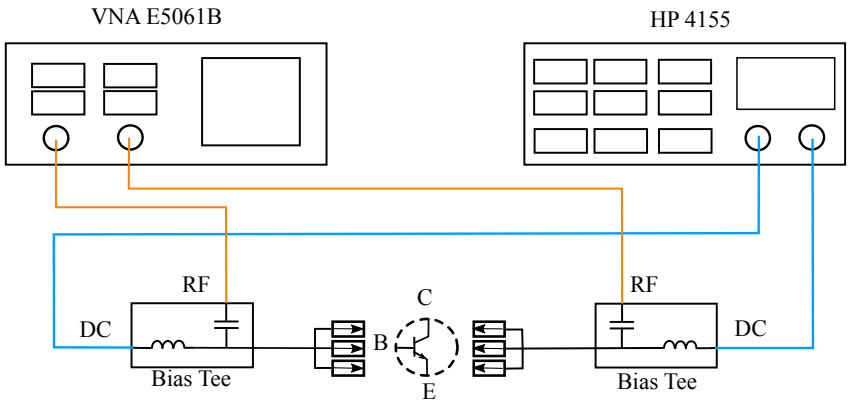


Figure 2.14: Low-frequency S-parameters measurement bench.

Once the S-parameters are converted to Y-parameters, the isothermal value of Y_{22}, Y_{22}^{AC}, from equation (2.31) is extracted following the procedure described in [93]. This method consists in fitting the AC isothermal region with a power function for both real and imaginary part of Y_{22} parameter as presented in figure 2.15. Hence, Y_{22}^{AC}, can be calculated according to the equation (2.32). The parameters Y_{12}^{DC} (respectively Y_{22}^{DC}) of equation (2.31) can be calculated from the derivative of the I_B vs. V_{CE} (respectively I_C vs V_{CE}) output characteristic at constant V_{BE}. The thermal resistance is extracted following the procedure presented in section 2.3. Having determined all these parameters, the thermal impedance, Z_{TH}, can be extracted for each transistor.

$$Y_{22}^{ac} = a_1 f^{b_1} + j a_2 f^{b_2} \tag{2.32}$$

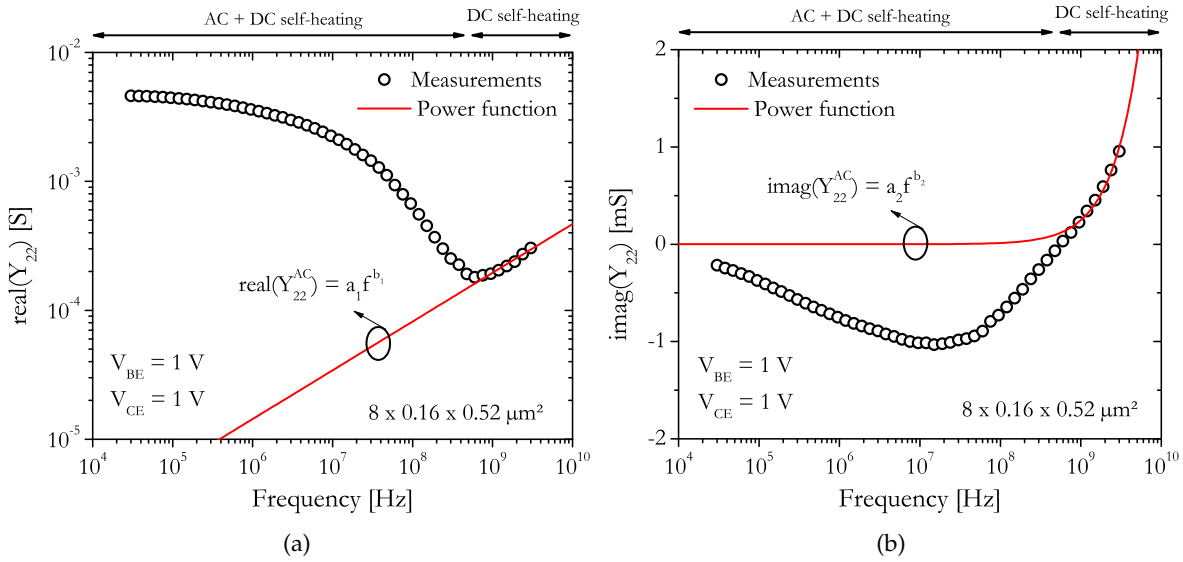


Figure 2.15: (a) Real and (b) imaginary part of Y_{22} with the corresponding extrapolation to extract the isothermal values using a power function for a 8 x 0.16 x 0.52 μm^2 device corresponding to SG13S technology from IHP Microelectronics.

The extracted thermal impedance following equation (2.31) is depicted in figure 2.16a for the magnitude and 2.16b for the phase. Regarding the magnitude frequency evolution, the thermal

impedance is equal to the thermal resistance for very-low frequencies while it tends to 0 K/W as one approaches the thermal cut-off frequency (around 100 MHz). On its side, the phase evolves from 0° at low-frequencies to a maximum shift of -75° near the thermal cut-off frequency.

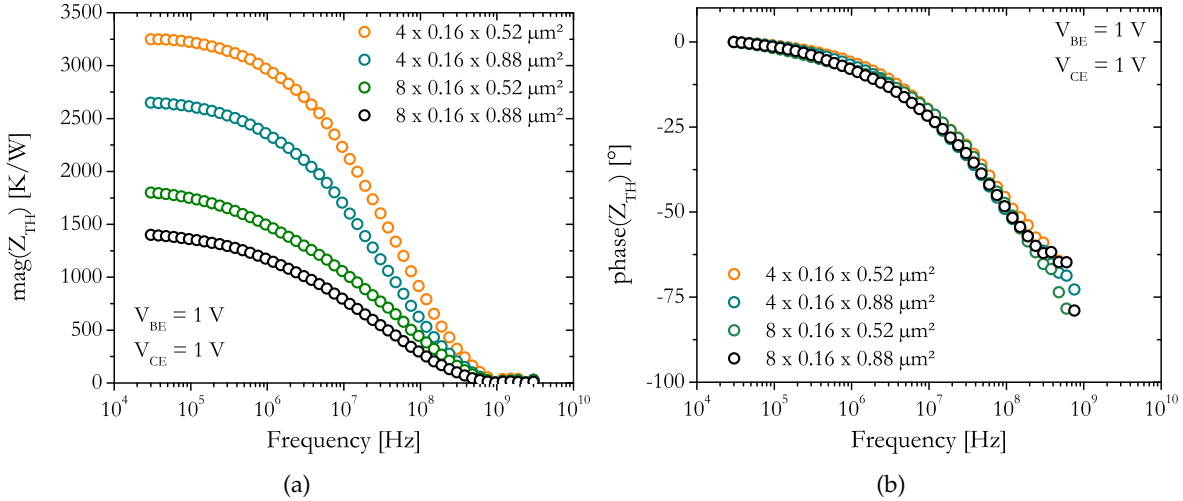


Figure 2.16: Extraction results for (a) the magnitude and (b) the phase of Z_{TH} for different emitter geometries corresponding to SG13S technology from IHP Microelectronics.

As presented in section 2.2.3, the single pole network electrothermal modeling from HiCuM compact modeling is not accurate enough to capture the dynamic self-heating effect. Therefore, for better accuracy, a more complex thermal model is required such as Foster network, Cauer network or recursive network. A comparison of the performance of these topologies is presented in [85] where it is shown that the recursive thermal model is the most accurate one. Therefore, a more detailed presentation of this electrothermal model is performed in the following section.

2.5.3 Recursive network

The heat flow analogy can be represented by the superposition of N subsections [94], each of them composed of one R-C network. In order to ensure a limited increase of the CPU simulation time while providing a sufficient enough model accuracy, the recursive network is designed with three poles as shown in figure 2.17.

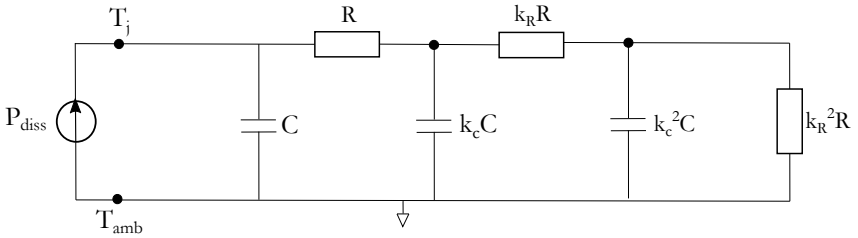


Figure 2.17: Electrical equivalent circuit of the recursive electrothermal network.

The corresponding thermal resistance, R, and thermal capacitance, C, of the first segment are calculated as,

$$R = \frac{R_{TH}}{1 + k_R + k_R^2}$$
$$C = C_{TH}\left(1 + \frac{1}{k_C} + \frac{1}{k_C^2}\right) \tag{2.33}$$

where k_R and k_C are scaling factors. While the thermal resistance is obtained from DC temperature controlled measurements as presented in section 2.3, the thermal capacitance is extracted from the imaginary part of the thermal impedance. The extracted values for both parameters are displayed in table 2.2 for all geometries from the IHP Microelectronics technology under investigation.

Device [μm^2]	R_{TH} [K/W]	C_{TH} [pJ/K]
4 x 0.16 x 0.52	3250	2.1
4 x 0.16 x 0.88	2650	3.2
8 x 0.16 x 0.52	1800	4.7
8 x 0.16 x 0.88	1200	6.0

Table 2.2: Extracted thermal resistance and capacitance for different emitter geometries corresponding to SG13S technology from IHP Microelectronics.

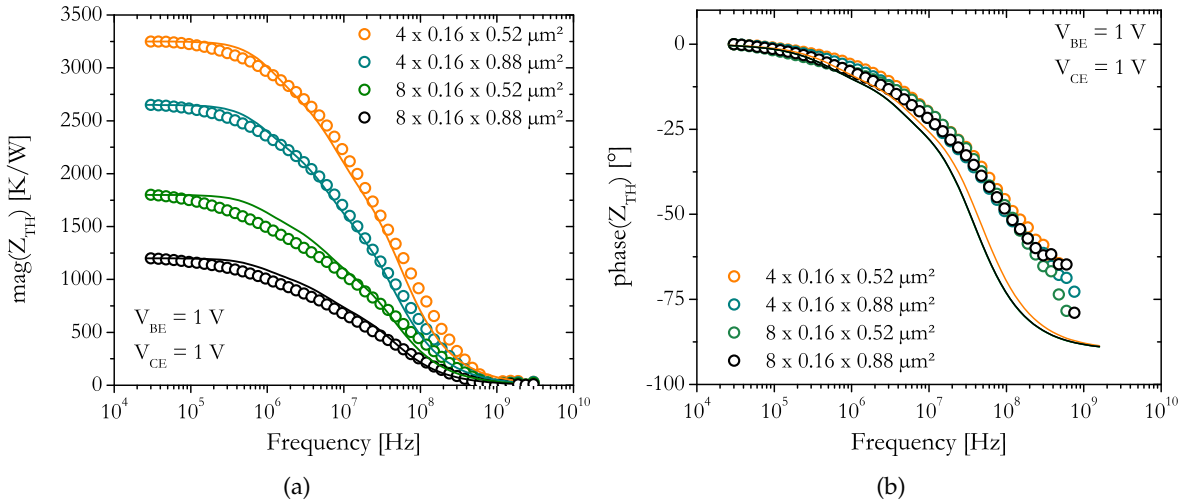


Figure 2.18: Comparison between measurements (symbols) and recursive network simulation (solid lines) for (a) the magnitude and (b) the phase of Z_{TH} for different emitter geometries corresponding to SG13S technology from IHP Microelectronics.

The simulated electrothermal model results are compared to the measurements ones in figure 2.18a for the magnitude and 2.18b for the phase where a good accuracy is achieved for both parameters compared to the single pole network results. The discrepancies observed for the phase at frequencies beyond f_{TH} (around 100 MHz) are not relevant since the current simulation only takes into account the thermal behavior of the transistor. As a consequence, the equivalent electrothermal model is only effective for a frequency ranging from 0 Hz to 100

MHz. Note that the scaling factors are fixed to a constant value of $k_R = 0.6$ and $k_C = 10$ for each DUTs. Moreover, owing to its physical basis, the recursive network can be scaled according to the transistor architecture. This aspect will be further developed in the following section.

2.6 Physics-based electrothermal compact model

The propagation of heat within the transistor mainly results from the conduction mechanism [74]. In SiGe HBTs, the heat source is located at the B-C junction due to the high-power density in this region [95]. Considering an uni-dimensional diffusion, the heat flow is divided in two contributions: the front-end-of-line (FEOL), through the collector toward the substrate, and the back-end-of-line (BEOL), through the emitter metal layers, as described in figure 2.19.

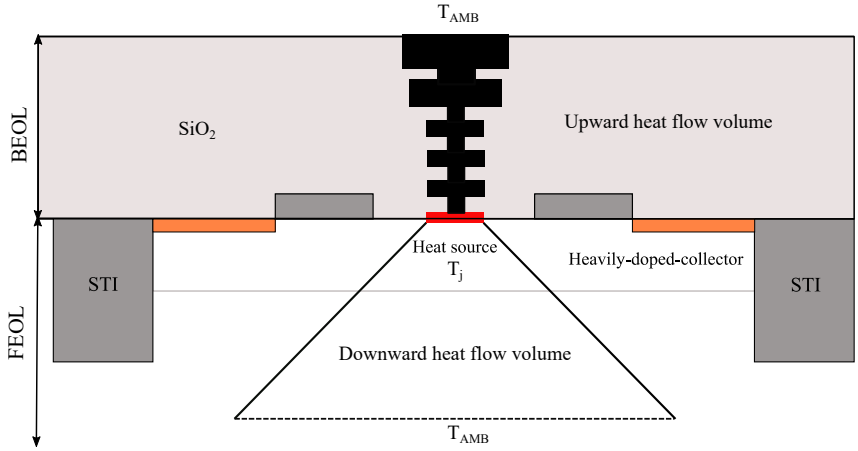


Figure 2.19: Illustration of the heat flow volume in a SiGe HBT architecture considering the BEOL metal layers. Note that the heat source is assumed to be located at the base-collector junction and the contributions from the emitter and the neutral base are neglected.

Existing electrothermal models take into account the temperature-dependent thermal conductivity with and without trench isolations [94]. Such isolation block the lateral heat flow, thus increasing the device temperature. In [96], an average thermal conductivity of silicon is used to determine the junction temperature-dependent thermal resistance while taking into account the contribution of the BEOL layers [97]. In [92], a complete thermal impedance model is developed using the downward heat flow with a heat-source located at the base-collector junction. This model allows extraction of a physical thermal network with multiple thermal time constants, specific to different regions of the transistor architecture, applicable for both frequency and time-domain analyses. In this section, a physics-based scalable electrothermal model is derived from the transistor architecture of SG13S technology from IHP Microelectronics taking into account the thermal conductivity evolution along the semi-conductor thickness.

2.6.1 Model formulation

The downward heat flow featuring a diffusion angle θ can be modeled by a superposition of N subsections leading to a distributed electro-thermal network. Each subsection is characterized

by its thermal resistance, $R_{TH,i}$, and its thermal capacitance, $C_{TH,i}$, as follows

$$R_{TH,i} = \int_{h_{i-1}}^{h_i} \frac{dz}{\kappa A_i(z)}$$
$$C_{TH,i} = \int_0^{h_i} \frac{\kappa}{\alpha} A_i(z) dz \tag{2.34}$$

where i is the subsection number ranging from 1 to N, A(z) is the cross-sectional area from the bottom side, h_i is the subsection thickness, κ(T) is the temperature-dependent thermal conductivity and α is the heat diffusion coefficient in silicon.

Heat diffusion angle

Depending on the value of the heat diffusion angle, the pyramidal downward heat flow through the device can be represented by two different scenarios as illustrated in figure 2.20.

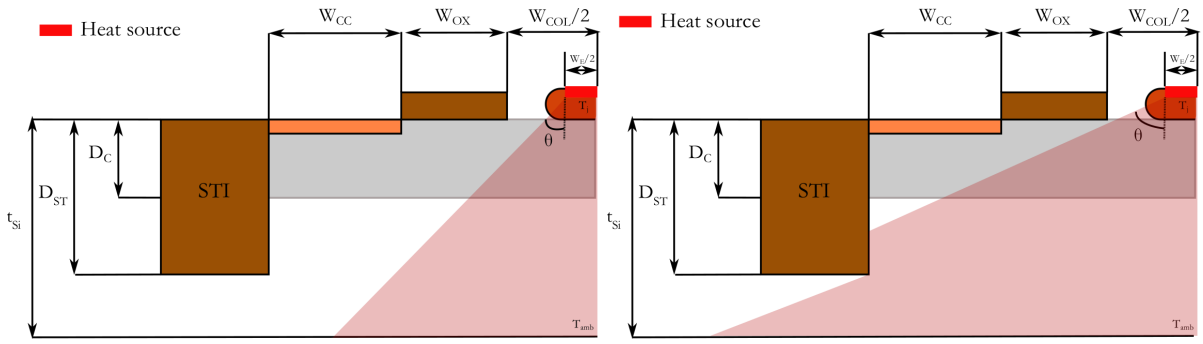


Figure 2.20: Downward heat diffusion for (a) $\theta < \theta_C$ and (b) $\theta > \theta_C$ corresponding to a half cross-section corresponding to SG13S technology from IHP Microelectronics.

The critical angle at which the heat flow changes from scenario (a) to (b) is denoted θ_C and is calculated as,

$$\theta_C = \arctan\left(\frac{W_{COL} + 2W_{CC} + 2W_{OX} - W_E}{2D_{ST}}\right) \tag{2.35}$$

where W_{COL} is the collector lateral width, W_{CC} is the collector contact width, W_{OX} is the oxide width and D_{ST} is the height of the shallow trench. For an angle $\theta < \theta_C$ (see figure 2.20a), the heat flow is not limited by the shallow trench isolation and the diffusion is pyramidal along the depth of the transistor. On the contrary, for $\theta > \theta_C$ (see figure 2.20b), the heat flow is blocked by the STI regions leading to a uniform heat diffusion in one subsection. The calculation of θ_C regarding the geometrical parameters provided by IHP Microelectronics leads to θ_C= 65°. In the literature, the heat diffusion angle is always lower than 65° [92], leading to a heat-flow scenario as depicted in figure 2.20a. For the rest of the study, the heat diffusion angle is set to 45° as proposed in [94].

Thermal conductivity considerations

In the case of SG13S technology from IHP Microelectronics, considering a heat diffusion flow as illustrated in figure 2.20a, the downward heat flow is divided into three subsections (N=3) considering the thermal conductivity of each layers: the selectively implemented collector (SiC), the heavily-doped collector and the substrate. Indeed, the material thermal conductivity value depends of its doping level or composition profile values [95]. Therefore, some reductions are considered compared to the reference substrate thermal conductivity κ_{Si}. In the selectively implemented collector (SiC), a reduction of 25% is considered on κ_{Si} due to the low doping of this region [98]. Then, in the heavily-doped collector, a large doping with N species leads to a 50% drop of the thermal conductivity [95]. Finally, the last region is located in the Si substrate with, therefore, no reduction in κ_{Si}. The values of each section thickness h_i with the corresponding thermal conductivity are summarized in table 2.3.

Subsection	Material	h_i [μm]	$\kappa_{i@300K}$ [$Wm^{-1}K^{-1}$]
1	SiC	0.08	110
2	Heavily-doped collector	0.2	75
3	Substrate	0.75	150

Table 2.3: Subsection description considering the material, the thickness and the thermal conductivity.

Moreover, the temperature dependence of κ_i [99] is given by,

$$\kappa_i(T) = \frac{1}{\kappa_a + \kappa_b T + \kappa_c T^2} \tag{2.36}$$

where coefficient κ_a, κ_b, κ_c for intrinsic Si are given as, 0.03x10^{-2} mK/W, 1.56x10^{-5} m/W, 1.65x10^{-8} m/KW, respectively [100].

2.6.2 Electrical equivalent circuit

Contribution of the FEOL

To represent the thermal impedance of the downward heat flow, a modified Foster-like thermal network is considered, as shown in figure 2.21, consisting of three thermal resistances, $R_{THF,1}$, $R_{THF,2}$, and $R_{THF,3}$, and capacitances, $C_{THF,1}$, $C_{THF,2}$, and $C_{THF,3}$. The three sets represent the three regions of the downward heat flow highlighted in the previous section: the selectively implemented collector (SiC), the heavily-doped collector, and the substrate.

Considering an average thermal conductivity [96] for each section and evaluating the integrals in equation (2.34), one can write the following expressions for the thermal resistance of the SiGe HBT structure following the approach presented in [94],

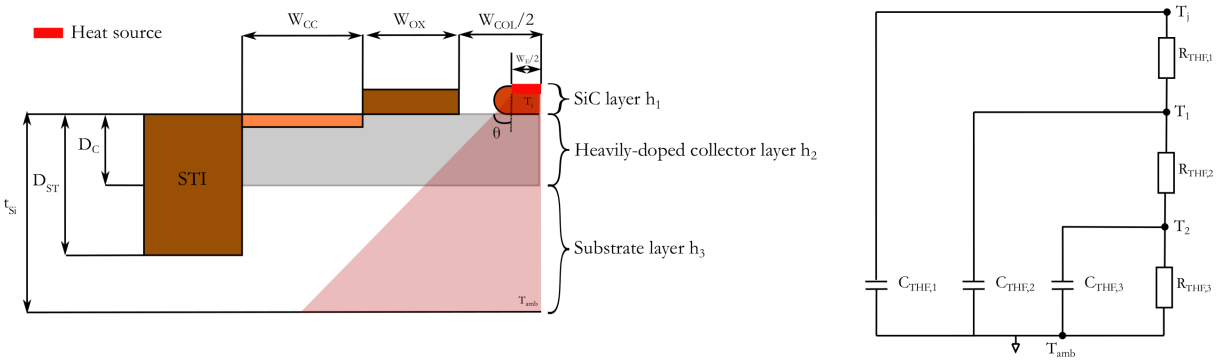


Figure 2.21: Electrical equivalent circuit of the downward heat flow for a SG13S technology from IHP Microelectronics.

$$
\begin{aligned}
R_{THF,1} &= \frac{1}{2(L_E - W_E)\kappa_1} \ln\left[\frac{L_E(W_E + 2h_1)}{W_E(L_E + 2h_1)}\right] \\
R_{THF,2} &= \frac{1}{2(L_E - W_E)\kappa_2} \ln\left[\frac{(L_E + 2h_1)(W_E + 2h_2)}{(W_E + 2h_1)(L_E + 2h_2)}\right] \\
R_{THF,3} &= \frac{1}{2(L_E - W_E)\kappa_3} \ln\left[\frac{(L_E + 2h_2)(W_E + 2h_3)}{(W_E + 2h_2)(L_E + 2h_3)}\right]
\end{aligned} \tag{2.37}
$$

Following a similar approach and using equation (2.34) one can, thereby, write the expressions of the thermal capacitances of the three regions as,

$$
\begin{aligned}
C_{THF,1} &= \frac{\kappa_1}{\alpha}\left[\frac{4}{3}h_1^3 + (L_E + W_E)h_1^2 + L_E W_E h_1\right] \\
C_{THF,2} &= \frac{\kappa_2}{\alpha}\left[\frac{4}{3}h_2^3 + (L_E + W_E + 4h_1)h_2^2 + (L_E + 2h_1)(W_E + 2h_1)h_2\right] \\
C_{THF,3} &= \frac{\kappa_3}{\alpha}\left[\frac{4}{3}h_3^3 + (L_E + W_E + 4(h_1 + h_2))h_3^2 + (L_E + 2(h_1 + h_2))(W_E + 2(h_1 + h_2))h_3\right]
\end{aligned} \tag{2.38}
$$

Contribution of the BEOL

Since the base and emitter layers are thin compared to the collector ones, the contribution from these regions is neglected in the rest of the study. The emitter metal layers (BEOL) are modeled through a thermal resistance R_{THB} which is calculated using the extracted thermal resistance R_{TH} and the calculated front-end-of-line thermal resistance R_{THF} as [97],

$$
R_{THB} = \frac{R_{THF} R_{TH}}{R_{THF} - R_{TH}} \tag{2.39}
$$

While R_{TH} is extracted according to the intersection technique (see section 2.3), the FEOL thermal resistance, R_{THF}, corresponds to the combination of each thermal resistance subsections as,

$$R_{THF} = \sum_{i=1}^{N} R_{THi} \tag{2.40}$$

Multi-fingers transistors

The model developed so far takes into account the heat diffusion for one emitter finger only. To consider multi-fingers transistor, two scaling factors, a_R and a_C, are added to the equivalent electrothermal network from figure 2.22. Since the fingers lie sufficiently away from the each other, the thermal coupling effect is neglected [101].

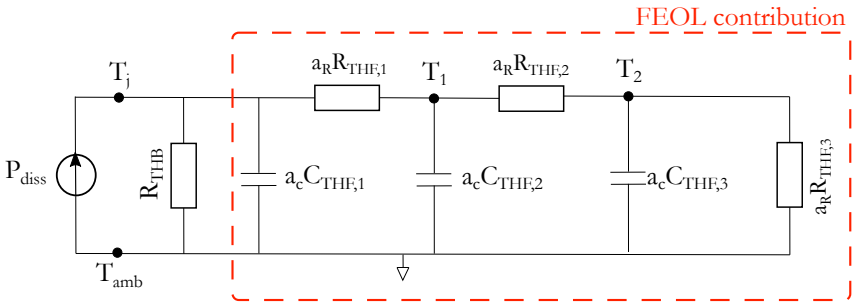


Figure 2.22: Electrical equivalent circuit of the physics-based electrothermal network.

Therefore, in the case of one-finger device, theses scaling factors are set to 1. For multi-fingers devices, the scaling factors are set to $a_R = 1/N_X$ and $a_C = 40N_X$.

2.6.3 Simulation results

The detailed values of the thermal resistances and capacitances for the three regions of the downward heat flow are shown in table 2.4, extracted using (2.37) and (2.38), for the four DUTs. As observed, the highest contribution for the thermal resistance is provided by the heavily-doped collector region due its reduced thermal conductivity.

Device [μm^2]	$R_{THF,1}$ [K/W]	$R_{THF,2}$ [K/W]	$R_{THF,3}$ [K/W]	$C_{THF,1}$ [pJ/K]	$C_{THF,2}$ [pJ/K]	$C_{THF,3}$ [nJ/K]
4 x 0.16 x 0.52	1341	1613	590	2.34	12.9	0.59
4 x 0.16 x 0.88	830	1124	477	3.72	17.9	0.70
8 x 0.16 x 0.52	671	806	295	4.67	25.7	1.18
8 x 0.16 x 0.88	415	562	239	7.44	35.9	1.40

Table 2.4: Extracted thermal resistance and capacitance for different emitter geometries corresponding to SG13S technology from IHP Microelectronics.

The extracted thermal impedance obtained in section 2.5 for the four DUTs is compared to the simulation results in figure 2.23a for the magnitude and in figure 2.23b for the phase. A

good agreement is obtained for the thermal frequency range (from 30 kHz to 100 MHz) for the four devices under test demonstrating the efficiency of the developed model. Once more, the discrepancies observed on the phase for frequencies beyond f_{TH} (around 100 MHz) are due the transistor electrical behavior which is not captured by the electrothermal network. Therefore, in order to associate both the thermal and electrical behavior of the transistor, the electrothermal network is connected to the temperature node of the HiCuM/L2 compact model.

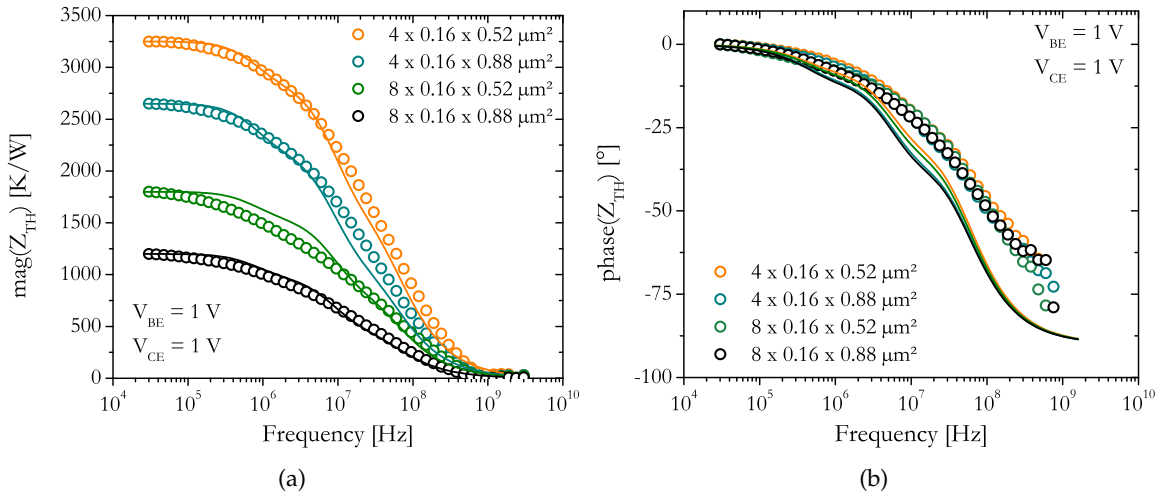


Figure 2.23: Comparison between measurements (symbols) and physics-based electrothermal model simulation (solid lines) for (a) the magnitude and (b) the phase of Z_{TH} for different emitter geometries corresponding to SG13S technology from IHP Microelectronics.

To that end, the model is validated on Y-parameters (used for thermal impedance extraction) as illustrated in figure 2.24 for Y_{12} parameter and in figure 2.25 for Y_{22} parameter over the entire operating frequency range ranging from 30 kHz to 3 GHz. As for the thermal impedance modeling, a good accuracy is achieved between the compact model simulation and the measurement results for various operating conditions. Those results indicate an accurate calculation of the device dissipated power using the HiCuM compact model.

2.7 Time domain validation

The electrothermal model developed in the previous section defines several thermal time constants for the heat diffusion mechanism in accordance with the transistor architecture. One way to validate the model accuracy is to perform pulse measurements [88]. In this measurement condition, the collector current increase due to self-heating effect can be observed together with the temperature rise [93]. Moreover, pulse measurements performed with short pulse widths allows to efficiently reduce the self-heating effect since the transistor collector current does not reach its steady-state value [102]–[104]. Therefore, transient characterization are useful to (i) extract both the thermal resistance R_{TH} and thermal capacitance C_{TH} [93], (ii) obtain isothermal data [104], [105] and (iii) extend the measured bias range towards higher voltages and current densities. In this section, the transient characterization of a SiGe HBT technology is

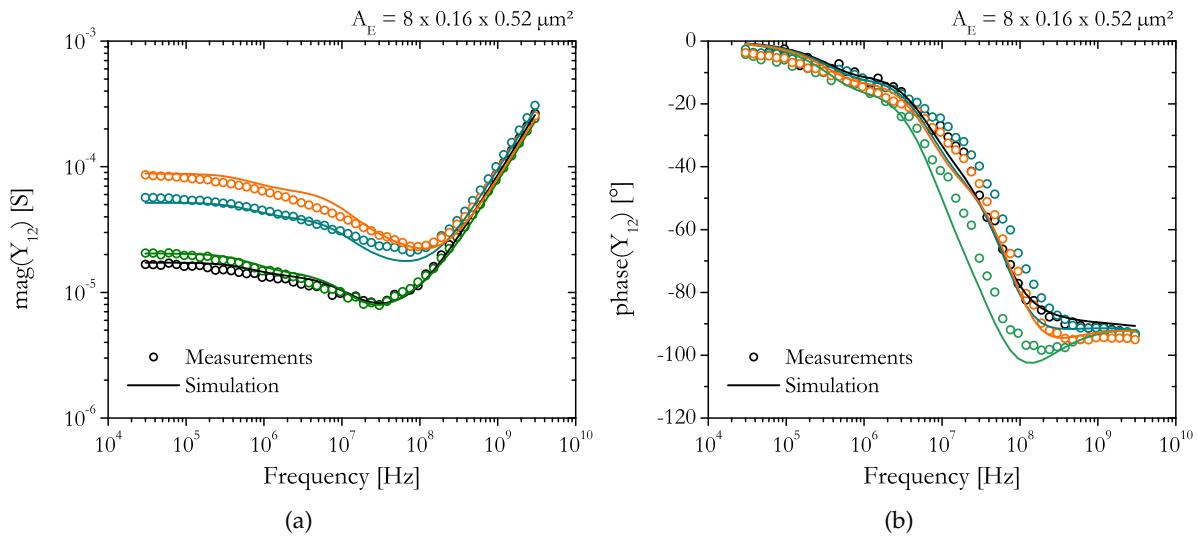


Figure 2.24: Comparison between measurements (symbols) and physics-based electrothermal model simulation (solid lines) for Y_{12} (a) magnitude and (b) phase, on a 8 x 0.16 x 0.52 μm^2 corresponding to SG13S technology from IHP Microelectronics.

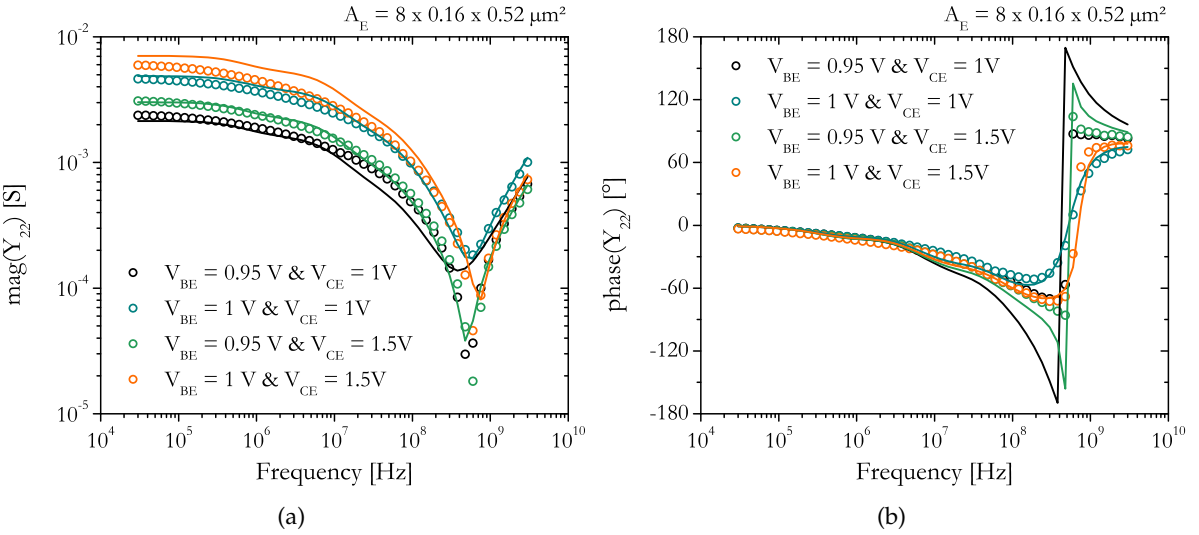


Figure 2.25: Comparison between measurements (symbols) and physics-based electrothermal model simulation (solid lines) for Y_{22} (a) magnitude and (b) phase, on a 8 x 0.16 x 0.52 μm^2 corresponding to SG13S technology from IHP Microelectronics.

performed and the measurement results are compared to transient compact model simulation results including the physics-based electrothermal model.

2.7.1 Pulse measurements

Pulse measurements were carried out with the pulsed DC analyzer Keithley 4200-SCS and consist of two pulse measurements units (PMUs) as illustrated in figure 2.26. The system generates the pulses while measuring the pulse time response. The pulse train (CH1) is directly applied to the base port of the transistor by setting the amplitude. The collector port (CH2) is biased at a constant voltage while the emitter is grounded. The PMU allows creating pulses larger than

80 ns for a minimum rise and fall times of 20 ns. Accurate measurements are obtained for a time window between 60% and 90% of the DC pulse [103].

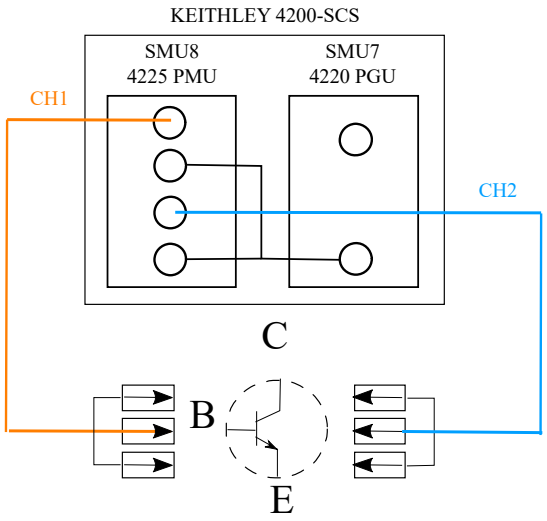


Figure 2.26: Experimental setup for pulse measurements.

2.7.2 Coaxial cable model

During pulse measurements, overshot on the collector current or voltage may appear, while a base pulse is applied [103], [106]. This is partly due to the passive elements associated with the coaxial cable and the connectors. It is therefore necessary to take into account a model featuring the coaxial cable and the connectors to properly perform the compact model simulation of HBTs under transient operation. For the pulse measurements setup, two coaxial cables were used between the base and collector ports and the pulsed DC analyzer. Therefore, a model of the coaxial cables, as depicted in figure 2.27a (shown for one single port), is added to account for test-bench simulation.

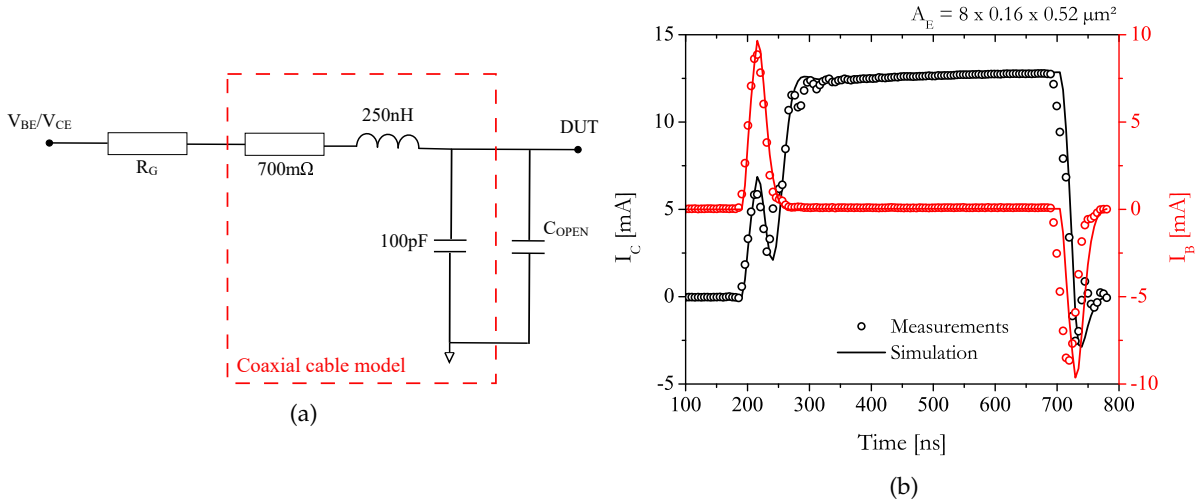


Figure 2.27: (a) Equivalent circuit model of the coaxial cables consisting of passive elements, the generator resistance R_G and device open capacitance C_{OPEN} and (b) Compact model simulation results on the base and collector current using the coaxial cable model at V_{BE} = 0.95 V and V_{CE} = 1.5 V.

The internal resistance of the pulse generator is 50 Ω for each of the base and collector ports. The values of the other components of the coaxial cable model depend on the length of the cables, and are thus adjusted accordingly during simulation. The capacitance, C_{OPEN}, corresponds to the device open capacitance and is quite low (typically, around a few fF).

Figure 2.27b presents the comparison between the pulse measurement results (symbols) of the base/collector current and the transient simulations (solid lines) including the coaxial cable model at V_{BE} = 0.95 V and V_{CE} = 1.5 V. The oscillations observed during the pulse measurements are accurately reproduce by the model for both the base and the collector current, thus validating the accuracy of the aforementioned model in the time domain.

2.7.3 Compact model simulation results

A comparison between the measured (symbols) and the simulated collector current using the single pole (red solid lines) and the physics-based (blue solid lines) thermal network is proposed in figure 2.28a for a V_{BE} = 0.95 V and V_{CE} = 1.5 V. Using the single pole thermal model, the collector current steady-state is reached after a few hundred nanoseconds. As observed, this simulation behavior is not representative of the measured evolution. On the contrary, using the physics-based thermal model, the collector current is slowly increasing according to the time evolution which is in accordance with the pulse measurement results as demonstrated in [107].

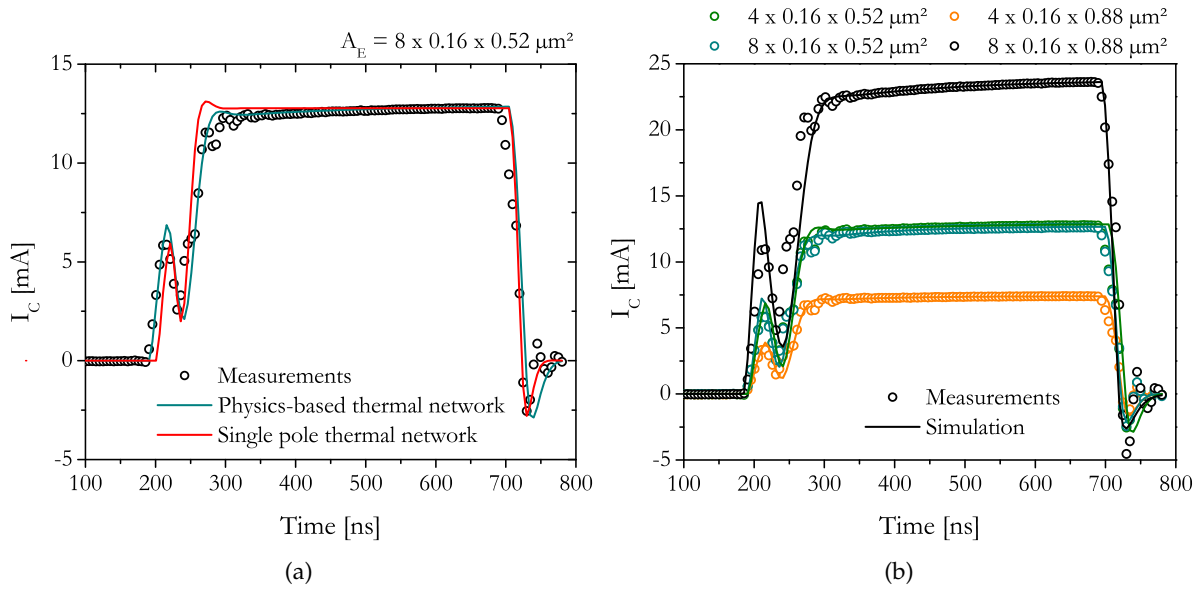


Figure 2.28: Collector current waveform (symbols) is compared to transient simulations (a) including the single pole (solid red lines) and the physics-based (solid blue lines) thermal model for a 8 x 0.16 x 0.52 μm^2 device and (b) including the physics-based (solid lines) thermal model for the four DUTs geometries corresponding to SG13S technology from IHP Microelectronics. Both figures are obtained at an operating condition of V_{BE} = 0.95 V and V_{CE} = 1.5 V.

Transient simulations were carried out with HiCuM compact model taking into account the current electrothermal model together with the coaxial cable one. The transient simulations are

performed under the bias conditions V_{BE} = 0.95 V and V_{CE} = 1.5 V for the four DUTs, with an applied pulse width of 500 ns and a pulse delay of 200 ns. Figure 2.28b shows the comparison between the transient simulations and the pulse measurements, depicting the transient behavior of the collector current, I_C. For the four geometries under investigation, the simulation using the developed thermal impedance model agrees very well with the waveform captured using pulse measurements.

2.8 Conclusion

The second chapter was dedicated to the characterization and the compact modeling of the main physical mechanisms occurring under high biases. More especially, the study has been focused on two particular transport mechanisms: the impact-ionization mechanism leading to the avalanche effect and the self-heating effect.

For the avalanche effect, several inaccuracies in HiCuM compact model have been highlighted resulting in a poor accuracy for large voltage bias (up to BV_{CBO}) and high current densities (beyond J_{LIM}). Consequently, an improved formulation of the multiplication factor has been presented which includes the modeling of the strong avalanche behavior as well as the current dependence of the mechanism. The formulation was implemented in HiCuM compact model with the addition of four model parameters: the strong avalanche parameter, k_{AVL}, together with its thermal coefficient, AL_{KAV}, and two high current parameters, h_{CAVL} and h_{VDAVL}. An accurate extraction procedure, fully scalable, was proposed and performed on a SG13S technology from IHP Microelectronics. The model has been validated on a large set of measurements under various operating conditions (at a constant V_{BE} or I_E), temperatures (ranging from 0°C to 100°C) and emitter dimensions.

On its side, the self-heating effect is commonly modeled using the single pole network from HiCuM compact model which is composed of one thermal resistance, R_{TH}, and one thermal capacitance, C_{TH}. Based on DC temperature-controlled measurements, the thermal resistance has been accurately extracted using the intersection technique on a SG13S technology from IHP Microelectronics. Using low-frequency S-parameter measurements, an extraction procedure has been reported for the thermal impedance, allowing to extract the transistor thermal capacitance. However, some discrepancies have been observed between the measurement and the simulation results for the thermal impedance under dynamic operating conditions. To improve the self-heating effect modeling, a recursive electrothermal network featuring three RC cells has been simulated and compared to the thermal impedance extraction results where a a good accuracy has been achieved for various emitter dimensions.

Moreover, based on the transistor architecture, a physics-based electrothermal model has also been developed which includes both the front-end and the back-end-of-line heat diffusion. While the back-end-of-line has been modeled using a single resistance, the front-end-of-line heat diffusion has been represented by a three poles RC network where each cells have been designed according to the thermal conductivity evolution along the transistor thickness. From

this formulation, it has been demonstrated that the heat diffusion is mostly limited by the poor thermal conductivity of the heavily-doped collector. The electrothermal model has been implemented in HiCuM compact model thermal node. The model simulation results have demonstrated a good accuracy for both the thermal impedance magnitude and phase. Furthermore, pulse measurements have been carried out to validate the model formulation under transient operating conditions. An excellent agreement has been obtained between the measurement and the transient simulation results which guarantee an accurate prediction of the transistor junction temperature over the time.

Now that the validity of HiCuM compact model is extended up to BV_{CBO} and up to high current densities, one wonders about the consequences on the transistor electrical characteristics when operating beyond the conventional safe-operating-area. A survey of the mixed-mode degradation occurring in SiGe HBT is proposed in the following chapter.

Chapter 3

Physics and Modeling of Hot-Carrier Degradation

Contents

3.1 Introduction

This chapter focuses on the description of the successive physical mechanisms leading to the base current degradation under mixed-mode stress. Based on an aging test campaign, the first section aims to locate the regions within the transistor architecture responsible from the recombination current increase. Then, a detailed description of the successive physical mechanisms leading to the base current degradation is proposed. Subsequently, a compact model including aging laws derived from the reaction-diffusion theory is reported together with associated scaling rules. An extraction procedure of the model parameters is developed and applied on various technologies confirming the versatility of the described model.

3.2 Physics of hot-carrier degradation

Si/SiO_2 interfaces are sources of defects resulting from a mismatch between the two materials, mainly caused by a deviation in the lattice parameters [108]. Therefore, those interfaces usually contain silicon dangling bonds as presented in figure 3.1a.

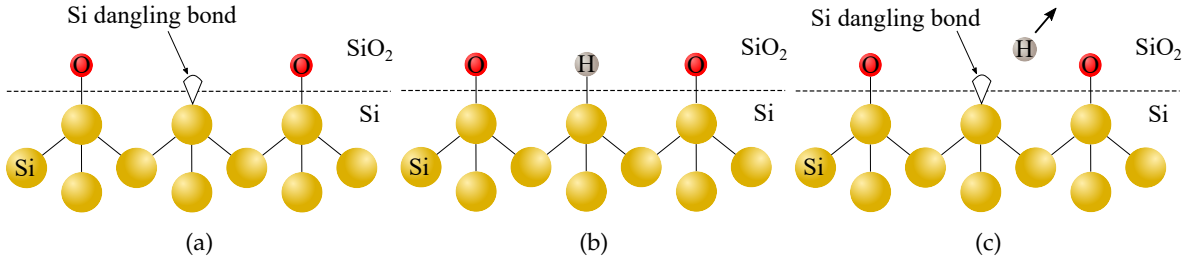


Figure 3.1: (a) Si dangling bond creation at the Si/SiO_2 interface, (b) Incorporation of hydrogen atoms for passivation of dangling bonds and (c) Interface trap carrier creation and hydrogen diffusion due to hot-carrier mechanism.

A common practice to reduce the density of traps at the interface for Si-based devices is to passivate them by incorporating hydrogen atoms, as illustrated in figure 3.1b. This operation leads to the formation of Si-H bonds, as represented by the chemical reaction from (3.1), with a binding energy of 2.3 eV to be compared with 3.1 eV for $Si\text{-}O_2$ bonds [5].

$$Si_3{\equiv}Si^{\bullet} + H^0 \longrightarrow Si_3{\equiv}Si{-}H \tag{3.1}$$

However, under high electric field, a hot-carrier can gain sufficient energy to break these passivated bonds. Therefore, the remaining Si dangling bonds acts as an interface state which can trap a carrier while the hydrogen released from the reaction diffuses away from the interface as displayed in figure 3.1c. The use of other species, such as the deuterium, instead of hydrogen atoms during the passivation treatment, can drastically reduce the density of created traps at the interface [109], [110]. However, this technique requires the use of heavy water (D_2O) during the passivation process, thus increasing the production cost [111].

3.2.1 Traps location

In SiGe HBTs, hot-carriers likely originates from impact ionization mechanism [56], [57], [112] in the base-collector space charge region (BC-SCR). Indeed, the avalanche effect causes the creation of electron-holes pairs by collision with Si atoms, as presented in chapter 1. The generated holes are further accelerated toward the base and may gain sufficient energy to initiate Si-H bond breakage in the vicinity of nearby Si/SiO_2 interfaces. The hydrogen dissociation reaction can then be expressed as in equation (3.2).

$$Si_3{\equiv}Si{-}H + h^+ \rightleftharpoons Si_3{\equiv}Si^+ + H \tag{3.2}$$

Two Si/SiO_2 interfaces likely submitted to hot-carrier degradation (HCD) have been identified in SiGe HBTs: the emitter-base spacer (E-B spacer) and the shallow trench isolation (STI), as illustrated in figure 3.2. The dissociation of Si-H bonds near these oxide interfaces due to hot-carriers leads to an additional non-ideal base current through Shockley-Read-Hall (SRH) recombination [51]. In order to discriminate the traps created at the E-B spacer from the ones created at the STI under a mixed-mode stress, two different measurements are performed on the transistor during the aging test. Under a forward bias of the emitter-base junction (*i.e.* forward Gummel plot), an increase of the base current indicates the creation of traps at the E-B spacer Si/SiO_2 interfaces. On the contrary, under a reverse bias of the base-collector junction (*i.e.* reverse Gummel plot), an increase of the base current indicates the creation of traps at the Si/SiO_2 STI interfaces [51].

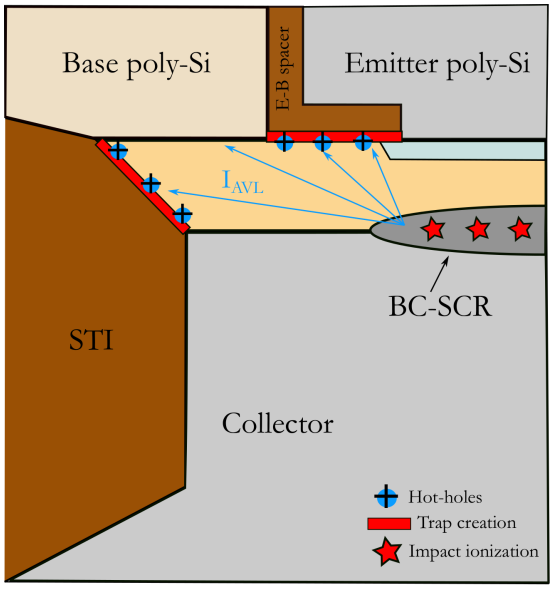


Figure 3.2: Schematic cross section of a SiGe HBT showing the Si/SiO_2 interfaces likely submitted to HCD.

A 0.42 x 5.56 µm² device from ST Microelectronics B55 technology is submitted to a mixed-mode stress of V_{CB} = 2 V and J_E = 0.35 mA/µm² during 10ks. Figure 3.3a shows the forward Gummel plot where a base current increase of [275% - 100%] is clearly identified for V_{BE} values

ranging from [0.3 V - 0.7 V]. On the contrary, figure 3.3b presents the reverse Gummel plot where a base current increase of less than 20% is observed for V_{BC} values ranging from [0.3 V - 0.7 V]. Therefore, in a SiGe HBT submitted to mixed-mode stress, traps are principally created at the E-B spacer Si/SiO_2 interfaces, corroborating the results obtained in [56], [57], [112].

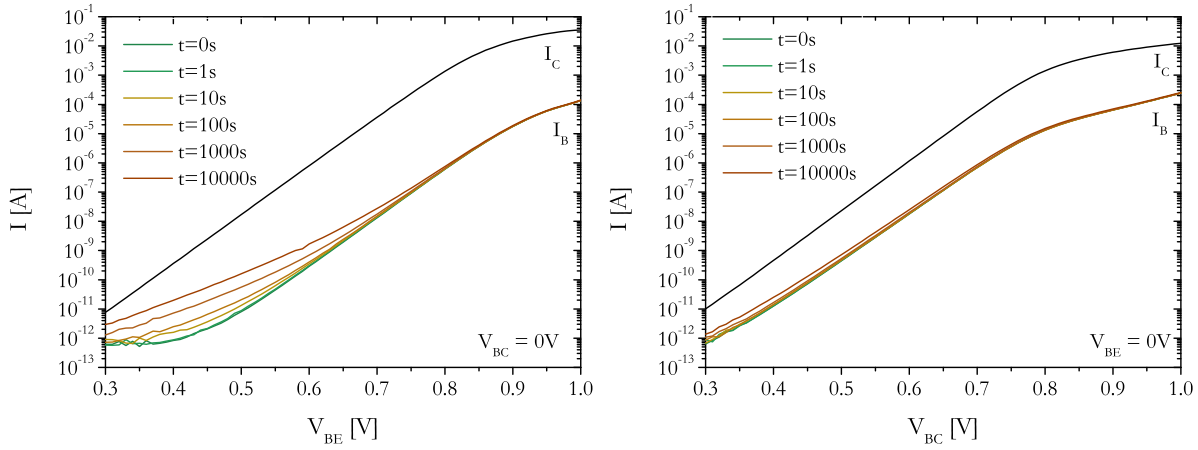


Figure 3.3: (a) Forward and (b) Reverse Gummel characteristics with increasing mixed-mode stress time (V_{CB} = 2 V and J_E = 0.35 mA/µm²) on a 0.42 x 5.56 µm² device corresponding to B55 technology from ST Microelectronics.

3.2.2 Compact model analysis

The base current evolution according to the stress duration can be investigated through the use of compact models. In the latter, based on a scalable approach, the base current is usually defined following equation (3.3) [113].

$$I_B = A_E J_{BA} + P_E J_{BP} \tag{3.3}$$

where J_{BA} is the intrinsic contribution of the base current, J_{BP} is the peripheral contribution of the base current, A_E is the emitter area and P_E is the emitter perimeter.

W [μm]	L [μm]	P_E/A_E [μm^{-1}]
0.2	5.56	22.6
0.3	5.56	11.5
0.42	5.56	7.36

Table 3.1: Drawn geometry features and effective perimeter to area ratio of devices under test corresponding to B55 technology from ST Microelectronics.

For 2D devices (emitter length larger than the emitter width), the specific parameters J_{BA} and J_{BP} are extracted from the equation (3.4).

$$\frac{I_B}{A_E} = J_{BA} + \frac{P_E}{A_E} J_{BP} \tag{3.4}$$

As an example, the normalized base current from equation (3.4) according to different P_E/A_E ratios (see table 3.1) for a forward Gummel operation at V_{BE} = 0.6 V is displayed in figure 3.4. Based on a linear regression, J_{BA} is deduced from the point of intersection of this characteristic while J_{BP} is extracted from the slope.

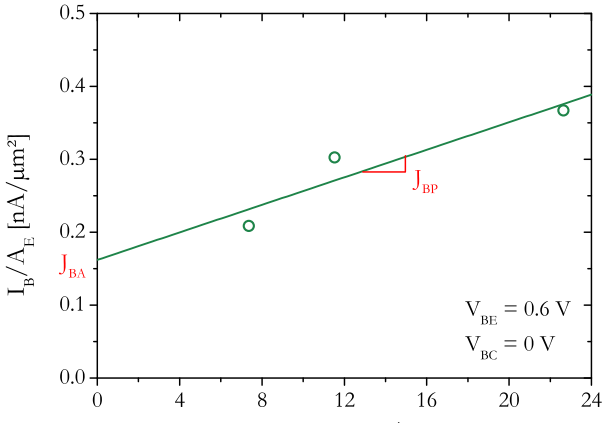
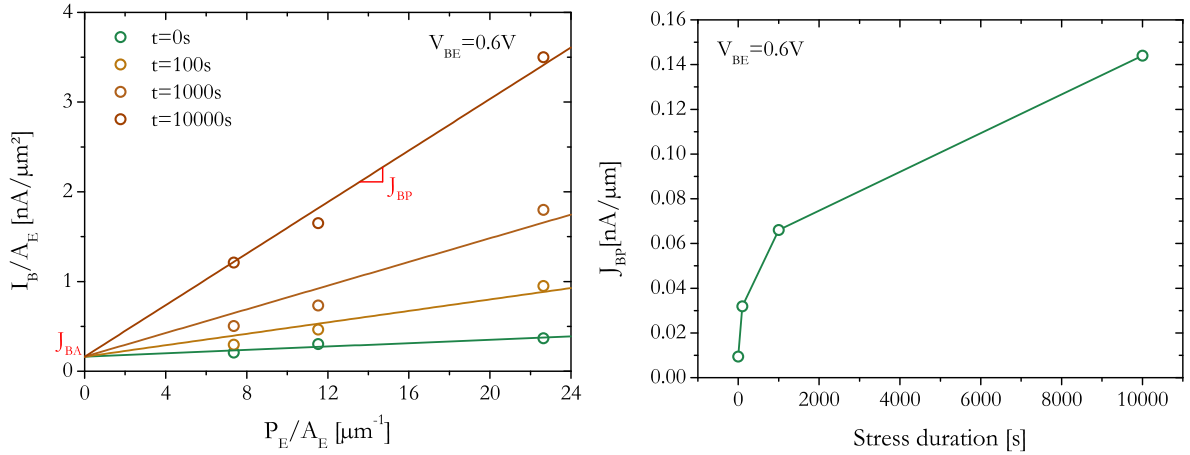


Figure 3.4: Base current density evolution according to the P_E/A_E ratios extracted at V_{BE} = 0.6 V and V_{BC} = 0 V corresponding to B55 technology from ST Microelectronics.

This extraction procedure can further be applied on different P_E/A_E ratios submitted to a mixed-mode stress of V_{CB} = 2 V and J_E = 0.35 mA/µm² during 10ks. The base current density is extracted for each device from table 3.1 and for each stress duration. The extraction results together with the linear regression are reported in figure 3.5a.



(a) (b)

Figure 3.5: (a) Base current density as a function of the P_E/A_E ratio for different stress duration extracted at V_{BE} = 0.6 V and (b) Peripheral contribution of the base current extracted from the slopes of figure 3.5a as a function of the stress duration at V_{BE} = 0.6 V corresponding to B55 technology from ST Microelectronics.

One observes on this plot that the intrinsic contribution of the base current is not modified along the stress duration (*i.e.* J_{BA} is constant). Meanwhile, the peripheral contribution, J_{BP}, is increased from 0.01 nA/µm at t = 0 s to 0.14 nA/µm at t = 10 ks, as illustrated in figure 3.5b. This result confirms the traps creation along the emitter perimeter and, therefore, possibly near the E-B spacer oxide interface.

Moreover, using HiCuM compact model, the creation of traps at the Si/SiO_2 interfaces could be associated with the modification of a single model parameter. Indeed, the peripheral part of the base current under forward operation conditions before the avalanche regime is described as [46],

$$I_{BP} = I_{BEpS} e^{\left(\frac{V_{BEi}}{M_{BEP} V_T} - 1\right)} + I_{REpS} e^{\left(\frac{V_{BEi}}{M_{REP} V_T} - 1\right)} \tag{3.5}$$

where I_{BEpS} is the peripheral B-E saturation current, M_{BEP} is the peripheral B-E current ideality factor, I_{REpS} is the peripheral B-E recombination saturation current and M_{REP} is the peripheral B-E recombination current ideality factor. Assuming that V_{BEi} is greater than few V_T, equation (3.5) reads as,

$$I_{BPn} = \frac{I_{BP}}{e^{\left(\frac{V_{BEi}}{M_{BEP} V_T} - 1\right)}} = I_{BEpS} + I_{REpS} e^{\frac{V_{BEi}}{V_T}\left(\frac{1}{M_{REP}} - \frac{1}{M_{BEP}}\right)} \tag{3.6}$$

where I_{BPn} is the normalized peripheral part of the base current.

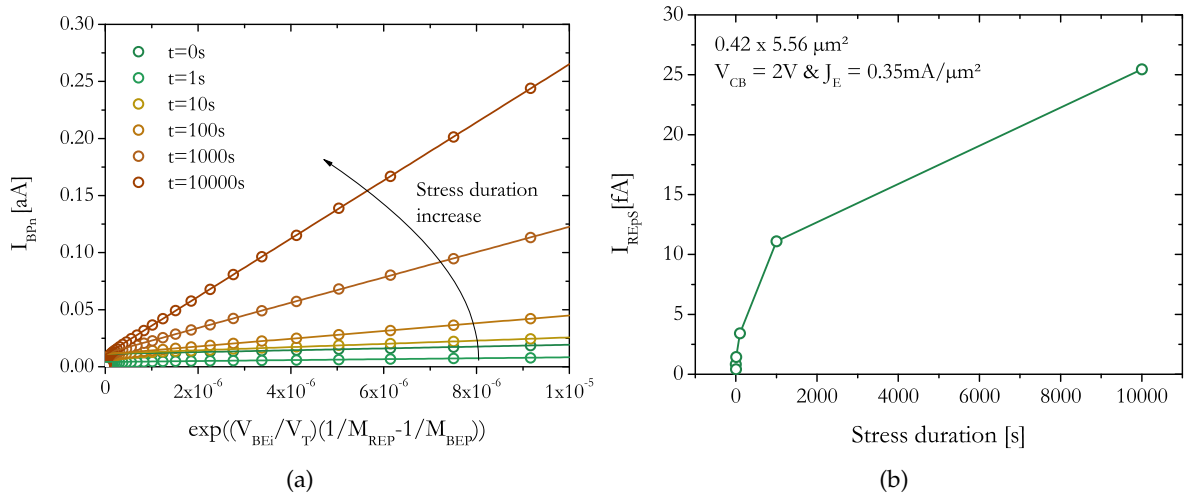


Figure 3.6: (a) Normalized peripheral part of the base current, I_{BPn}, extracted from the measurements in figure 3.3a for various stress duration and (b) I_{REpS} evolution extracted from figure 3.6a with increasing mixed-mode stress time (V_{CB} = 2 V and J_E = 0.35 mA/µm²) on a 0.42 x 5.56 µm² device corresponding to B55 technology from ST Microelectronics.

From the measurement presented in figure 3.3a, the evolution of I_{BPn} parameter, established in equation (3.6), according to $e^{\frac{V_{BEi}}{V_T}\left(\frac{1}{M_{REP}} - \frac{1}{M_{BEP}}\right)}$ is plotted in figure 3.6a. As demonstrated previously, the point of intersection of the linear regression remains constant with increasing stress

duration while, on the contrary, the slope evolution, displayed in figure 3.6b, shows a large increase over the stress duration. Therefore, the HiCuM parameter impacted by HCD, following equation (3.6), is the parameter I_{REpS}. This outcome is consistent with the results obtained in [53], [55], [114], [115].

3.2.3 TCAD simulations

The compact model parameter responsible for the base current increase has been identified in the previous section. If the assumption made from the E-B spacer trap location is verified, this parameter increase should be correlated to the density of created traps at the E-B spacer interface. Consequently, TCAD simulations are performed on a simulated structure featuring the SiGe HBT architecture from ST Microelectronics B55 technology. Traps (density N_T) are introduced at the E-B spacer interface following the distribution presented in figure 3.7.

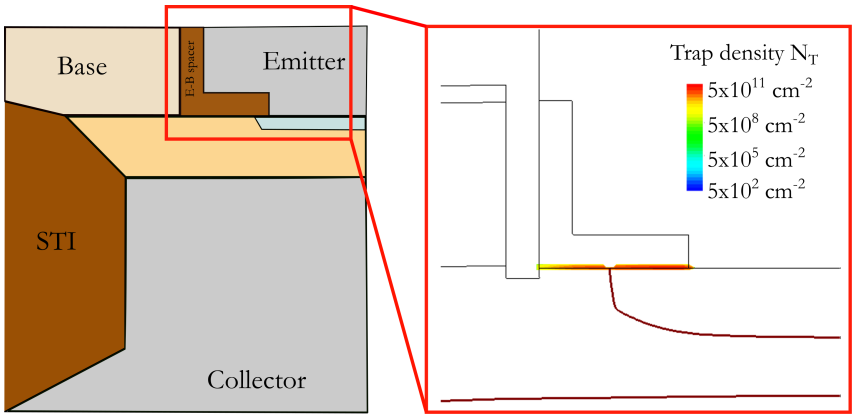


Figure 3.7: TCAD structure of a B55 technology from ST Microelectronics showing the zoom on the E-B spacer oxide where traps have been added at the Si/SiO_2 interface.

On the forward Gummel simulation results from figure 3.8a, one observes that the addition of trap density, N_T, leads to an increase of the base current at V_{BE} values ranging from [0.4 V - 0.7 V] corresponding to the expected base recombination current values. From this plot, the J_{REpS} parameter (I_{REpS} parameter normalized by P_E) increase is extracted using HiCuM compact model simulations. The extraction results are displayed in figure 3.8b for various trap densities depicting a linear relation between N_T and J_{REpS} as expressed in equation (3.7).

$$J_{REpS}(t) = \alpha N_T(t) \tag{3.7}$$

where α is the proportionality coefficient extracted from the linear regression of figure 3.8b. This formulation leads to a geometry dependent expression for I_{REpS} as presented in equation (3.8).

$$I_{REpS}(t) = \alpha P_E N_T(t) \tag{3.8}$$

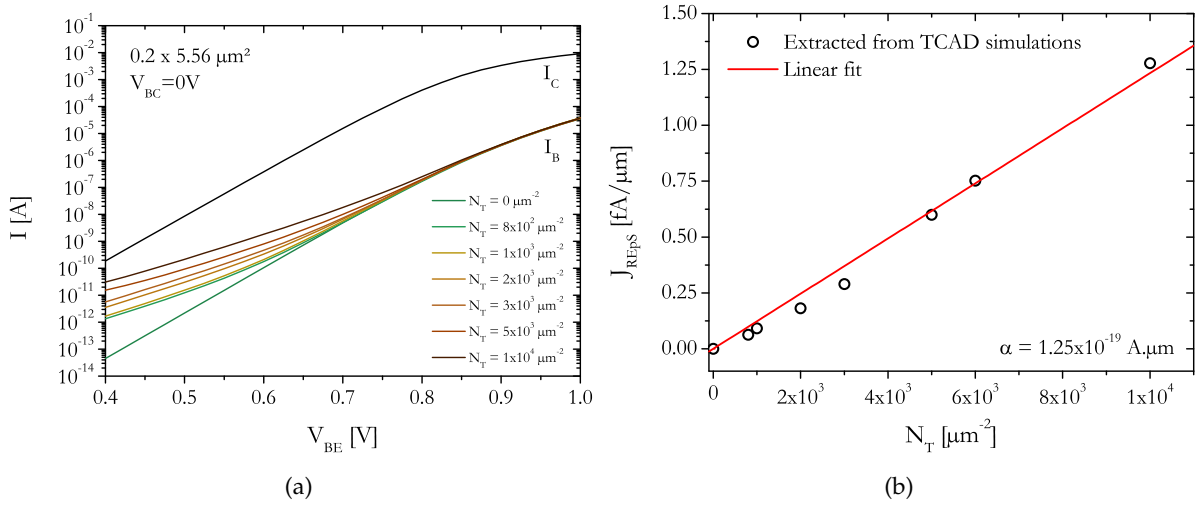


Figure 3.8: (a) TCAD simulation results for various trap densities and (b) corresponding J_{REpS} evolution allowing to extract the proportionality coefficient α representative of the relationship between the density of defects at the interface and the base recombination current density value on a B55 technology from ST Microelectronics .

From this equation, we can conclude that despite the passivation of traps by hydrogen, the density of active interface states is not equal to zero before aging tests. The density of pre-existing traps, $N_T(0)$, can further be calculated, following equation (3.8), by extracting I_{REpS} parameter before any aging procedure. For the present technology, the density of pre-existing traps is evaluated to $N_T(0) \approx 650$ µm^{-2}. This calculated value is close from the one reported in [57] which extracted an initial defect density of 600 µm^{-2} for the exact same technology. This strong correlation between the two results validates the proportionality relation between the peripheral recombination current and the trap density at the interface.

3.3 Accelerating factors

The mixed-mode degradation depends on two accelerating factors, V_{CB} and J_E, as they both determine the avalanche rate and the device junction temperature. The increase of the impact ionization rate leads to the increase of the hot-carriers density and/or their energy resulting in a higher density of created traps at the E-B spacer [36]. On the contrary, the increase of the junction temperature may have a beneficial impact as recovery effects may occur in SiGe HBTs [52]. Moreover, these two accelerating factors can trigger high-current (Kirk effect) or high-voltage mixed-mode damage (pinch-in effect) [116]. The operation within the Kirk effect region leads to a decrease of the base current degradation since the impact ionization rate is reduced [35], as introduced in the second chapter. Meanwhile, under pinch-in conditions, the HBT suffers from high electrical and thermal instabilities [37]. The correlation between the physical mechanisms and the hot-carrier degradation requires a preliminary study.

3.3.1 Time dependency

The long-term mixed-mode stress performed on SG13S technology in [52] focuses on the time evolution of the degradation. At the early stages of the degradation, the base current increase shows a power-law evolution (t^n). However, a reduction of this exponent is observed for long stress times which suggests a saturation of the degradation. This behavior is also observed on the B55 technology from ST Microelectronics as presented in figure 3.9.

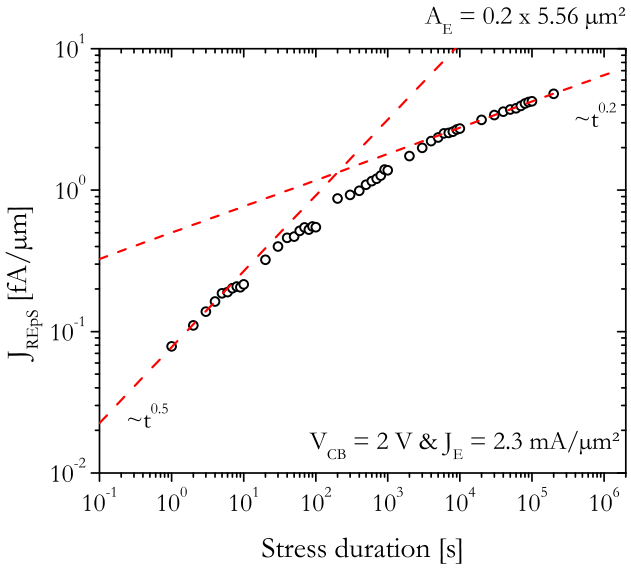


Figure 3.9: Time-exponent evolution of J_{REpS} parameter for a mixed-mode stress of V_{CB} = 2 V and J_E = 2.3 mA/µm² on a 0.2 x 5.56 µm² device corresponding to B55 technology from ST Microelectronics.

First, the base current degradation is modeled by a power-law with n = 0.5, consistent with the reported values in the literature [52], [57], [117]. Then, the time-exponent is slowly decreasing toward n = 0.2 for the last time decade (between 1 ks and 10 ks), close to the reported value in [52]. The results in [57] allows to exclude annealing as a possible reason for the slowdown of the degradation effects since the device temperature is not modified during the aging stress. The TCAD simulations demonstrates the presence of a hot spot near the EB spacer which could indicate a loss of trapped holes due to electron injection [57]. Another mechanism that could explain the time exponent reduction is the saturation of the available Si-H bonds as suggested in [54]. This last assumption is in line with the physical explanation reported in section 3.2 since the density of traps passivated by hydrogen atoms tends towards a finite value. The increase of the recombination current depends on two other mechanisms since the avalanche and the self-heating effect occur under high voltage and current biases.

3.3.2 Avalanche mechanism

The increase of the generated traps at the Si/SiO_2 interface originates from the impact ionization mechanism [36] which, therefore, depends on V_{CB} and J_E operating conditions. Investigations have been carried out to evaluate the degradation evolution depending on these two accelerating factors. Figure 3.10a shows the relative base current degradation at V_{BE} = 0.7 V for

various applied J_E under a constant V_{CB} of 2.75 V. One observes an increase of the recombination current with increasing emitter current densities resulting from a higher avalanche current within the device. However, a reduction of the degradation impact is noticed for the highest J_E due to (i) a decrease of the avalanche current at high current densities [35] (Kirk effect) as well as (ii) a higher junction temperature. Figure 3.10b shows the relative base current degradation at V_{BE} = 0.7 V for various applied V_{CB} and under a constant J_E of 0.12 mA/µm². These measurements evidence that the damage is increased with V_{CB} due to higher electric field value within the BC-SCR. Indeed, a high electric field leads to the increase of the hot-carrier average energy which causes higher damage at the E-B spacer interface [118]. These results are highlighted on various SiGe HBTs architectures [36], [52], [53], [114], [119] demonstrating that the physical phenomena is comparable for each technology.

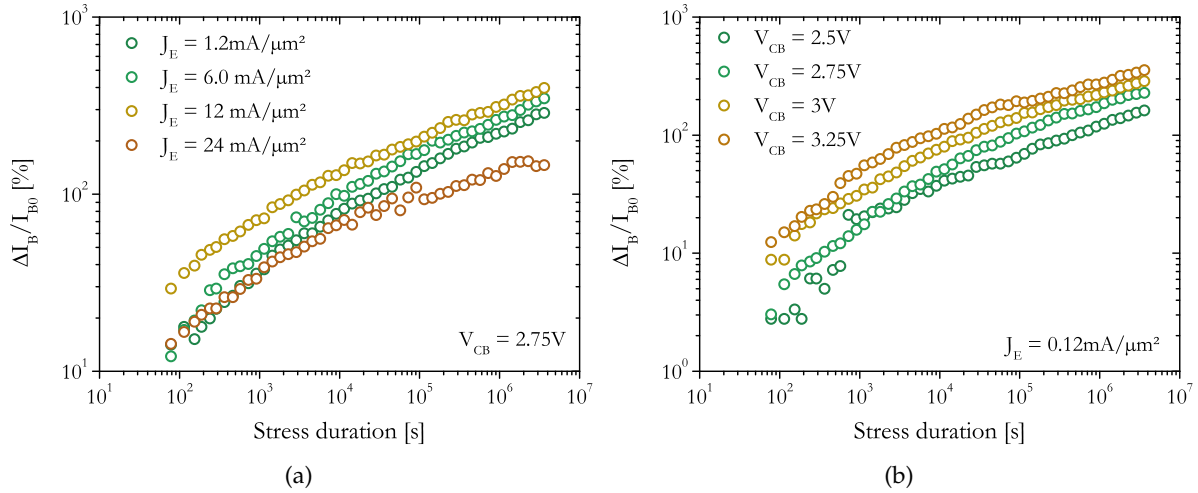


Figure 3.10: Relative base current evolution as a function of the stress duration for (a) V_{CB} = 2.75 V and various J_E and (b) J_E = 0.12 mA/µm² and various V_{CB} on a 8 x 0.16 x 0.52 µm² device corresponding to SG13S technology from IHP Microelectronics.

Figure 3.11a presents the forward Gummel characteristic evolution according to a set of three ambient temperatures equal to -40°C, -10°C and 27°C. Three devices corresponding to SG13S technology from IHP Microelectronics were submitted to a mixed-mode stress of V_{CB} = 3 V and I_E = 180 µA at those same ambient temperatures. The measurement results after one hour of stress duration are displayed in figure 3.11b for the base current and is compared to the initial characterization results. As predicted, an increase of the recombination current is observed for the three DUTs. However, it can be highlighted a larger impact of HCD on the base current for decreasing ambient temperatures. This trend implies a larger degradation of the Si/SiO_2 interface for a given low temperature. This result is consistent with the negative temperature-dependence of the avalanche effect leading to an increased trap creation rate within the BC-SCR for low temperatures.

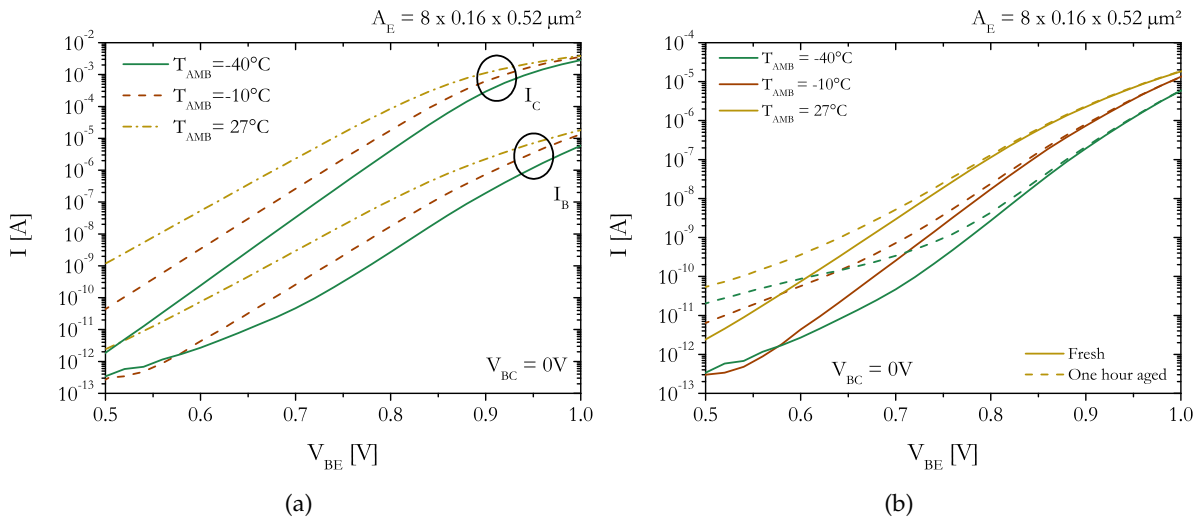


Figure 3.11: Gummel characteristics (a) without any aging procedure and (b) after one hour of mixed-mode stress (V_{CB} = 3 V and I_E = 180 µA) at different ambient temperatures (-40°C;-10°C and 27°C) on a 8 x 0.16 x 0.52 µm² device corresponding to SG13S technology from IHP Microelectronics.

3.3.3 Recovery properties

Figure 3.12a presents the evolution of the Gummel characteristic according to the stress duration for a mixed-mode stress of V_{CB} = 2.7 V and I_E = 20 mA where an increase of the recombination current can be observed. The relative base current variation at V_{BE} = 0.7 V is depicted in figure 3.12b.

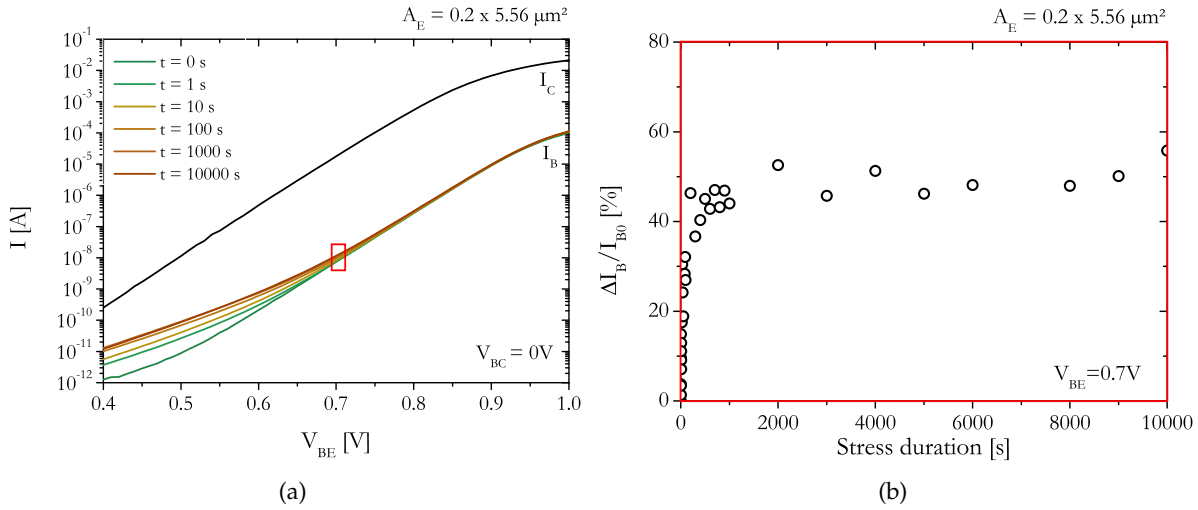


Figure 3.12: (a) Gummel characteristic and (b) relative base current evolution for a mixed-mode stress (V_{CB} = 2.7 V and I_E = 20 mA) at high junction temperature (T_j = 315°C) applied on a 0.2 x 5.56 µm² device corresponding to B55 technology from ST Microelectronics.

A maximum increase of 50% is noticed after 2000 s which is followed by a saturation of the base current variation. Due to the elevated injection current, the self-heating effect is activated under this particular mixed-mode stress resulting in a very high junction temperature of 315°C. The hot-carrier energy is reduced while increasing device temperature [120] which leads to a less

"efficient" degradation of the Si/SiO_2 interfaces. Moreover, a dynamic equilibrium between the generation and the annihilation of trap is reached leading to a reduced level of degradation on the base current.

Recovery properties can be highlighted under elevated temperatures [52] resulting from (i) the activation of self-heating effect or (ii) an increase of the ambient temperature. Figure 3.13 presents the base current and current gain evolution of an aged device submitted to an annealing treatment at 125°C during 7 hours. A partial recovery of the base current is observed which results in an increased current gain compared to the one reported after the 72 hours dynamic mixed-mode stress. The created traps during the aging phase are re-passivated by hydrogen atoms during the annealing phase meaning that the degradation is reversible providing a high junction and/or ambient temperature.

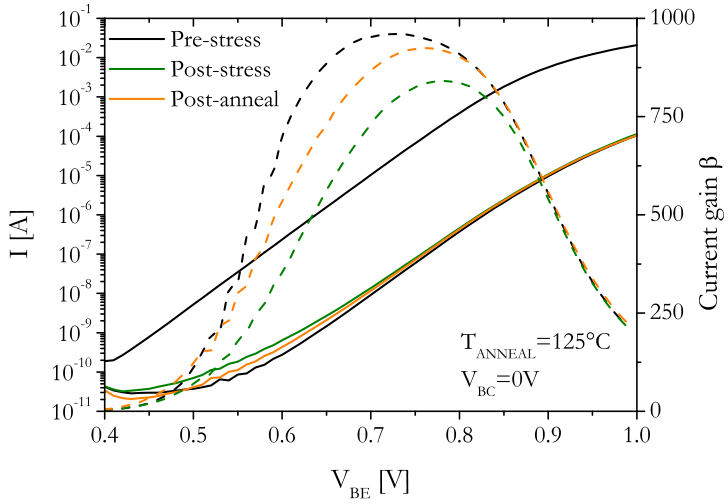
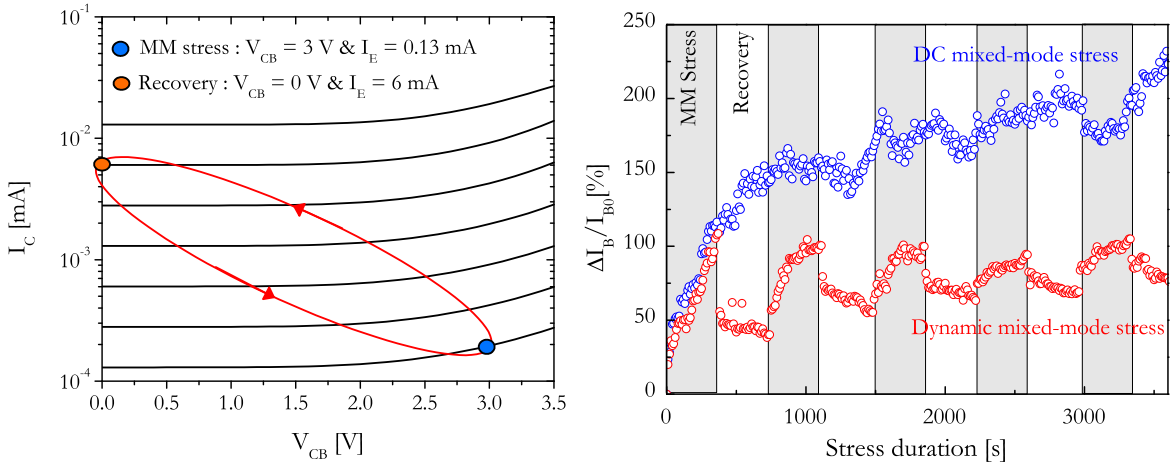


Figure 3.13: Gummel characteristics before/after an annealing treatment at 125°C on a former aged transistor corresponding to SG13S technology from IHP Microelectronics.

For now, the DUTs have only been submitted to a static mixed-mode stress leading to a monotonic increase of the recombination base current. However, in RF circuit operation, the transistor is biased under different operating conditions according to a load line resulting in a periodical activation of the avalanche and self-heating effect and vice-versa. Therefore, a toggling aging test between two extreme bias conditions is performed on a transistor as presented in figure 3.14a. During the first bias condition (MM stress), the device is biased at high V_{CB} which leads to the creation of traps at the interface due to the activation of the impact-ionization mechanism. During the second bias condition (Recovery), a large J_E is applied which increases the device junction temperature and allows to re-passivate the Si/SiO_2 interface states at the EB spacer.

A cycling of 360 s between these two bias conditions is then performed up to one hour of aging test. In addition, another device featuring the same emitter dimension is submitted to a DC mixed-mode stress (featuring V_{CB} = 3 V and I_E = 0.13 mA) during one hour. The aging measurement results are plotted in figure 3.14b for both the static mixed-mode stress condition



(a) (b)

Figure 3.14: (a) Bias conditions for dynamic mixed-mode stress and (b) relative base current evolution for this particular stress mode compared to a DC mixed-mode stress on a 8 x 0.16 x 0.52 µm² device corresponding to SG13S technology from IHP Microelectronics.

(blue curve) and the dynamic mixed-mode stress one (red curve). In the early stages of the aging test, both devices are submitted to the same stress condition resulting in a similar evolution of the base current. Then, while the degradation is increasing for the static stress condition (by means of minor variations due to the measurement conditions), partial recovery of the base current can be highlighted for the dynamic aging test during recovery phases. At the end, the measurement results reveal a reduction of the total base current degradation for the dynamic mixed-mode stress compared to the static stress condition. This outcome indicates a possible limited impact of hot-carrier degradation for RF circuit applications.

3.4 Compact modeling

Regarding the device degradation due to hot-carrier mechanism, the development of a compact model including the aging laws is necessary to predict the transistor/circuit lifetime. In SiGe HBTs, despite of the criticism in the MOS community [121], the reaction-diffusion (R-D) model is an efficient framework for HCD modeling [52], [53], [122], [123]. The R-D model gives rise to the power law modeling. However, this power law does account neither for the saturation of the degradation observed for long stress duration, nor for the initial phase when the generation process dominates, as highlighted in section 3.3. Moreover, the annihilation of traps due to the transistor junction temperature rise must be implemented in the formulation of the aging compact model. A complete analytical solution of the R-D model has been proposed in [54] but does not account for the invariance in time in case of dynamic stress.

Indeed, considering for example the scenario illustrated in figure 3.15 for the base recombination current parameter at the base-emitter periphery, I_{REpS}, extracted from measurements under a dynamic stress bias condition (switching between two stress biases). In the first time interval, the HiCuM-AL aging compact model [54] follows the actual measurements. However,

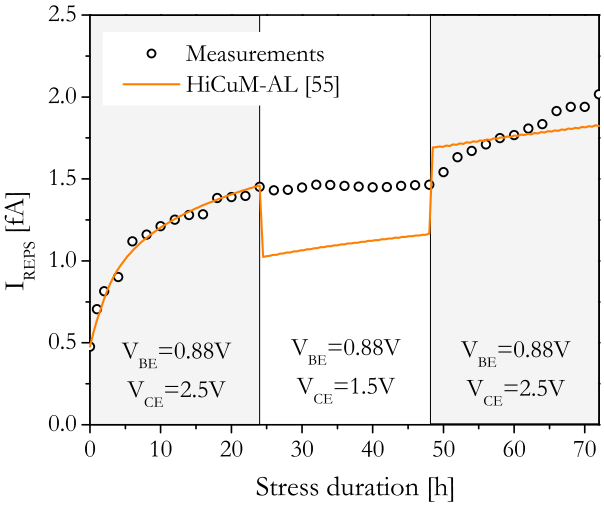


Figure 3.15: Comparison between measurements (symbols) and simulations (solid line) of the aging model proposed in [54] for a dynamic stress on a 8 x 0.16 x 0.52 µm² device corresponding to SG13S technology from IHP Microelectronics.

in the second time interval, *i.e.* under the low stress condition, the aging model calculates the degradation according to the new stress bias without retaining the final value of I_{REpS} from the first (high) stress phase, thus leading to a discontinuity compared to the measured data which shows a weak recovery under low-stress conditions. Therefore, this model is not suitable for RF circuit simulations and must be further improved.

3.4.1 Reaction-diffusion framework

As presented in section 3.2, the hot-carrier degradation is attributed to the creation of traps near the E-B spacer oxide interface. Both Si-H bond breakage at the interface and the subsequent hydrogen diffusion must be accurately modeled to capture all the time dependencies of the degradation mechanism. Generally, the reaction-diffusion theory allows to calculate the density of created traps at the Si/SiO_2 interface according to the equation (3.9).

$$\frac{dN_T}{dt} = K_F(N_F - N_T(t)) - K_R N_T(t) N_H(0,t) \tag{3.9}$$

where K_F is the trap generation rate, K_R is the trap annihilation rate, $N_T(t)$ is the density of created traps at the interface, N_F is the density of available bonds that can be broken and $N_H(0,t)$ is the density of hydrogen remaining at the Si/SiO_2 interface.

Since the traps are only located at the interface and cannot move from this location, the generation trap rate $g_T(t)$ can be described as,

$$g_T(t) = \frac{dN_T(t)}{dt} \tag{3.10}$$

The creation of a trap is directly associated with a free H atom that can diffused in the E-B spacer volume [124], hence,

$$g_T(t) = \phi_H(0,t) \tag{3.11}$$

where ϕ_H(x,t) is the flow of hydrogen which is related to the surface density following the Fick's law of diffusion [125] as,

$$\phi_H(x,t) = -D_H \frac{\delta N_H(x,t)}{\delta x} \tag{3.12}$$

where D_H is the diffusion constant of hydrogen in a material.

Adding the conservation law of hydrogen when x > 0, Fick's second law [125] is written,

$$\frac{\delta N_H(x,t)}{\delta t} - D_H \frac{\delta^2 N_H(x,t)}{\delta x^2} = 0 \tag{3.13}$$

The reaction-diffusion model has been implemented in HiCuM compact model according to the figure 3.16. With regards to the trap creation, equations (3.9), (3.10) and (3.11), can be directly embedded in a Verilog-A model as presented in [115] resulting in relations between g_T(t), ϕ_H(0,t), N_T(t) and N_H(0,t) along with their time derivatives, all of them being located at the interface (x=0). These equations interact with the electrical part of the model through K_F and K_R parameter as inputs, and through the trap density N_T as an output. The correlation between N_T and I_{REpS} parameter has been established in section 3.2.3. Therefore, compared to the implementation proposed in [115], the trap density N_T(t) is dynamically calculated using equation (3.9) while I_{REpS} parameter is determined using equation (3.8), as proposed in [119]. The second part of the system accounting for the hydrogen diffusion is modeled by the diffusion equations which cannot be directly translated in Verilog-A. However, there is no need to translate the whole equations but only to identify the relation between : N_H(0,t) and ϕ_H(0,t) [126]. To that end, the limit conditions for hydrogen diffusion model are detailed in the next section.

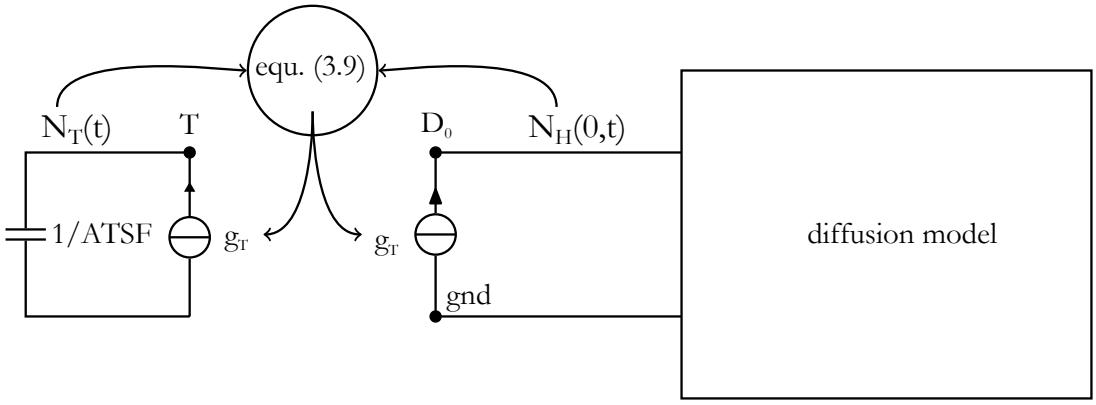


Figure 3.16: Implementation schematic of the reaction-diffusion model.

3.4.2 Limit conditions of hydrogen diffusion

In general terms, the diffusion mechanism is sketched in figure 3.17 where is considered a diffusion of free H atoms in a layer of a finite thickness L.

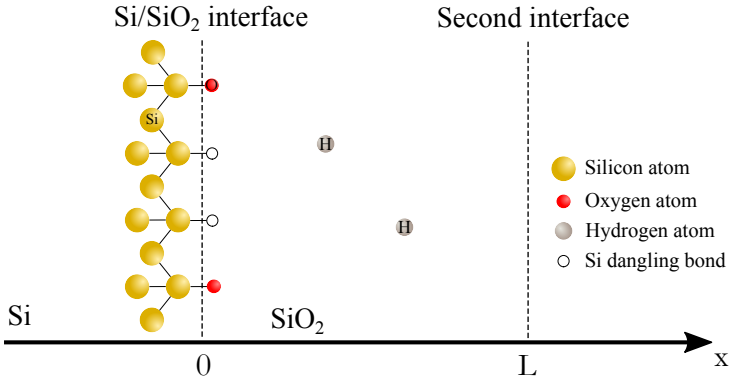


Figure 3.17: Schematic of the hydrogen diffusion considering the creation of traps at the Si/SiO_2 interface.

Therefore, some limit conditions can be formulated at the second interface : either a barrier to hydrogen, as in equation (3.14), or an open space, as in equation (3.15).

$$\phi_H(L,t) = 0 \tag{3.14}$$

$$N_H(L,t) = 0 \tag{3.15}$$

Since the diffusion equations are all linear and time-invariant, they can be translated in the frequency domain. The Fourier transform of equation (3.13) gives,

$$\frac{\delta \tilde{N}_H}{\delta x^2} - j\frac{2\pi f}{D_H}\tilde{N}_H(x,f) = 0 \tag{3.16}$$

where $\tilde{N}_H$(x,f) is the Fourier transform of N_H(x,t). The general solution of equation (3.16) is

$$\tilde{N}_H(x,f) = A_H e^{\alpha x} + B_H e^{-\alpha x} \tag{3.17}$$

with the positive real value for α equals to $(1+j)\sqrt{\frac{\pi f}{D_H}}$. The coefficients A_H and B_H are determined by limit conditions at x = 0 and x = L, respectively.

The Fourier transform of equation (3.12) gives,

$$\tilde{\phi}_H(x,f) = -D_H\frac{\delta \tilde{N}_H(x,f)}{\delta x} \tag{3.18}$$

where $\tilde{\phi}_H$(x,f) is the Fourier transform of ϕ_H(x,t). Considering the general solution expressed in equation (3.17), equation (3.18) becomes,

$$\tilde{\phi}_H(x,f) = -\alpha D_H(A_H e^{\alpha x} - B_H e^{-\alpha x}) \tag{3.19}$$

Considering the limits at x = 0, we obtain the system of equations :

$$\begin{aligned} \tilde{N}_H(0,f) &= (A_H + B_H) \\ \tilde{\phi}_H(0,f) &= -(1+j)\sqrt{\pi f D_H}(A_H - B_H) \end{aligned} \tag{3.20}$$

and at x = L :

$$\begin{aligned} \tilde{N}_H(L,f) &= (A_H e^{\alpha L} + B_H e^{-\alpha L}) \\ \tilde{\phi}_H(L,f) &= -(1+j)\sqrt{\pi f D_H}(A_H e^{\alpha L} - B_H e^{-\alpha L}) \end{aligned} \tag{3.21}$$

Accordingly, the three limit conditions of the diffusion admittance-like quantity $\tilde{Y}(0,f)$ are summarized in table 3.2 : one for very thick diffusion layer and two for finite thicknesses.

Case	Limit conditions	$\tilde{Y}(0,f) = \tilde{\phi}_H(0,f)/\tilde{N}_H(0,f)$
Semi-infinite	L $\rightarrow \infty$; A_H = 0	$(1+j)\sqrt{\pi f D_H}$
Hydrogen barrier	$\tilde{\phi}_H(L,f) = 0$	$(1+j)\sqrt{\pi f D_H} tanh((1+j)\sqrt{\pi f/D_H}L)$
Free hydrogen	$\tilde{N}_H(L,f) = 0$	$(1+j)\sqrt{\pi f D_H} coth((1+j)\sqrt{\pi f/D_H}L)$

Table 3.2: Limit conditions for hydrogen diffusion model.

The normalized representation of the admittance $\tilde{Y}(0,f)$ is displayed in figure 3.18 for these three limit conditions. The normalization is done using the quantities :

$$\begin{aligned} f_0 &= \frac{D_H}{2\pi L^2} \\ \tilde{Y}_0 &= \frac{D_H}{L} \end{aligned} \tag{3.22}$$

Identical behaviors are observed for frequencies higher than f_0 while, for lower frequencies (*i.e.* corresponding to long stress duration), differences are observed. In an electrical analogy approach, the model with hydrogen barrier plays the role of a "capacitor" while the open interface one behaves as a "resistor".

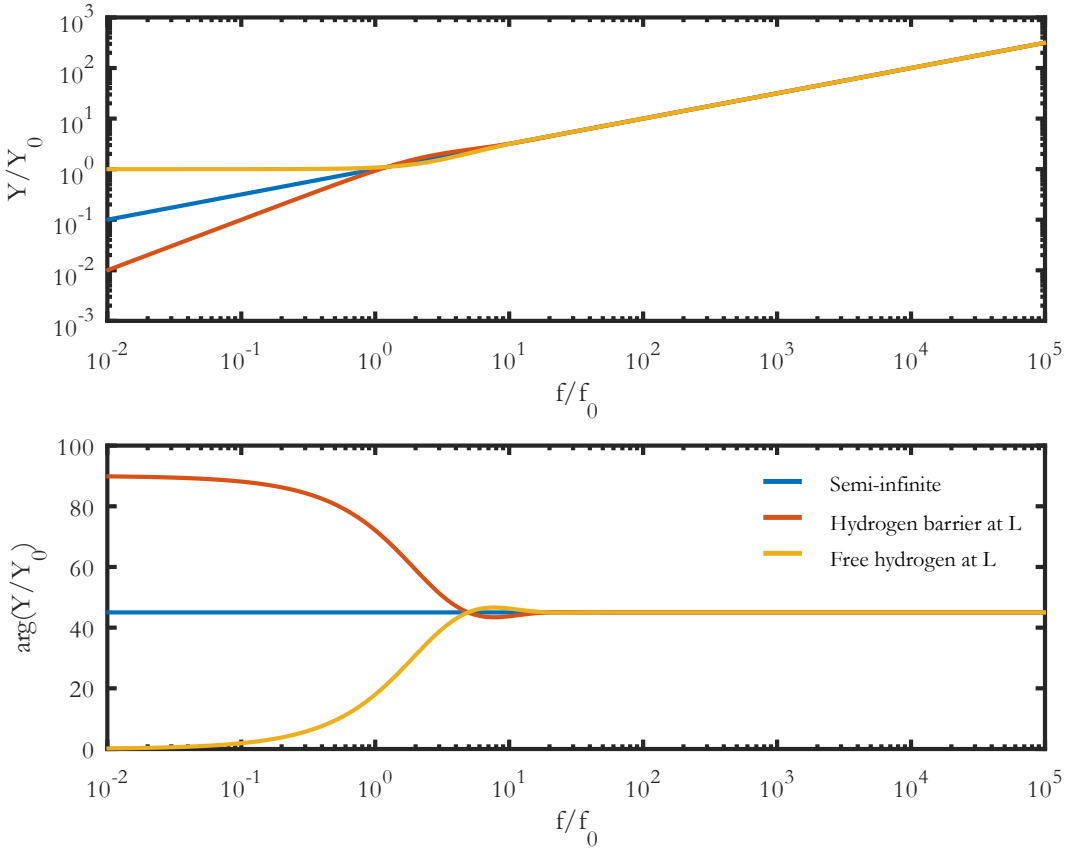


Figure 3.18: Bode-like representation of normalized admittance $\tilde{Y}(0,f) = \tilde{\phi}_H(0,f)/\tilde{N}_H(0,f)$ of diffusion for the three cases of second interface properties.

3.4.3 Diffusion compact modeling

The expression and the limit conditions of the diffusion admittance have been formulated in the previous section and can now be translated within a Spice-like circuit simulator with a limited set of nodes and variables. In order to preserve the time-invariance of the equations, only the time derivatives will appear in the electrical model. Since the distributed partial derivative are forbidden in compact model as space derivation isn't possible, the equations will be replaced by a finite set of first order differential equation equivalent to a resistor-capacitor (R-C) network [126]. Like in the case of the thermal analysis [107], the physical system is modeled by an R-C ladder network as presented in figure 3.19. It is composed of N resistances and N capacitances followed by an optional terminal conductance G.

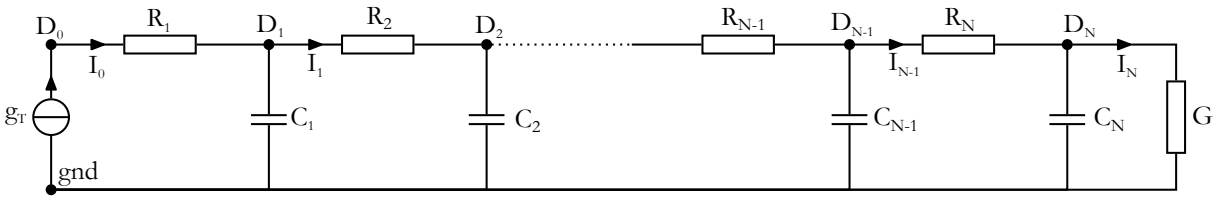


Figure 3.19: Architecture of the R-C ladder model of diffusion equation system.

For an easier conversion to Verilog-A model, the analogies between the hydrogen diffusion and the electrical variables are presented in table 3.3. Taking into account these analogies, the input of the circuit is the node D_0 with a corresponding voltage of $V_0 = N_H(0,t)$ and current of $I_0 = \phi_H(0,t) = g_T(t)$.

Hydrogen diffusion		Electrical	
Density	N_H in m^{-3}	Voltage	V_n in V
Hydrogen flow	ϕ_H in $m^{-2}s^{-1}$	Current	I_n in A
Hydrogen lattice diffusion barrier	R_H in $m^{-1}s$	Resistance	R_n in Ω
Hydrogen storage capacity	C_H in m	Capacitance	C_n in F

Table 3.3: Analogies between the hydrogen diffusion and the electrical model together with their corresponding units.

To limit the number of additional parameters, the values of R_n et C_n follow two geometrical sequences:

$$\begin{aligned} R_n &= R_1 \alpha_R^{n-1} \\ C_n &= C_1 \alpha_C^{n-1} \end{aligned} \tag{3.23}$$

In the frequency representation, the admittance can be introduced as $\tilde{Y}_n = \tilde{I}_n / \tilde{V}_n$ leading to the following recurrence system from equation (3.24),

$$\begin{aligned} \tilde{Y}_N &= G \\ \tilde{Y}_{n-1} &= \frac{1}{R_n + \frac{1}{j2\pi f C_n + \tilde{Y}_n}} \end{aligned} \tag{3.24}$$

Therefore, at high frequency, the network is equivalent to the single R_1 resistor. The limit frequency is then expressed as,

$$f_1 = \frac{1}{2\pi R_1 C_1} \tag{3.25}$$

By identifying $1/R_1 \approx \phi_H(0, f_1)$ for the semi-infinite exact model, we derive,

$$\begin{aligned} R_1 &\approx \frac{1}{\sqrt{2\pi f_1 D_H}} \\ C_1 &\approx R_1 D_H \end{aligned} \tag{3.26}$$

The minimum accurate frequency of the R-C model is approximated by the cut-off frequency of the last cell:

$$f_N \approx \frac{1}{2\pi R_N C_N} \tag{3.27}$$

Since only one dimension is considered for this system, along the x axis as in figure 3.17, both sequences (equation (3.23)) should feature the same common ratio α_R=α_C. The terminal conductance G is chosen to adjust the long term behavior of the model according to the nature of the second interface: either a barrier to hydrogen diffusion or an open space. In figure 3.20, both semi-infinite and R-C network model admittance are compared for different values of G. All models have identical behavior for frequencies between f_N/f_0 and f_1/f_0 following a $\sqrt{f}$ law, characteristic of diffusion mechanism. For low frequencies, the model exhibit some discrepancies due to the conductance value. For G = 0, the model acts as an hydrogen barrier modeling of the second interface while for G = $1/R_N$ or G = $100/R_N$, the model behaves as a free hydrogen modeling of the second interface.

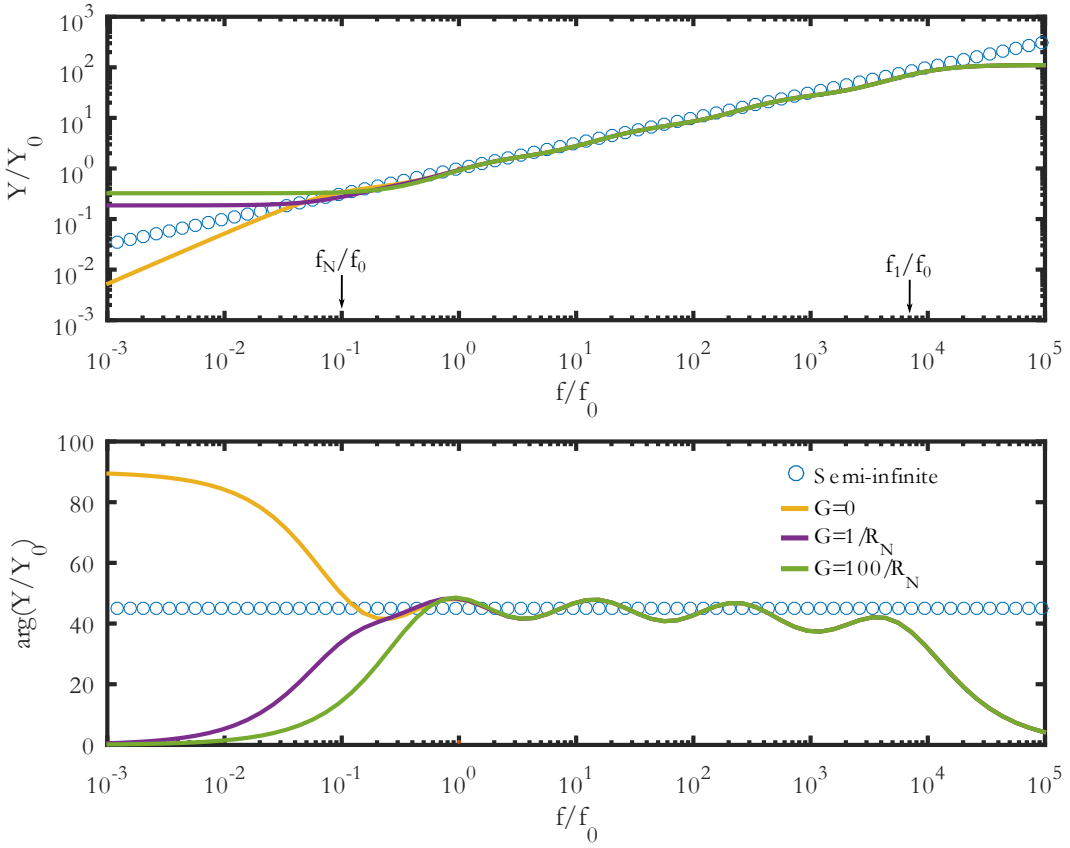


Figure 3.20: Bode-like representation of normalized admittance $\tilde{Y}(0,f) = \tilde{\phi}_H(0,f)/\tilde{N}_H(0,f)$ of the R-C ladder model for α_R=4 and N=5 compared to the semi-infinite theory.

The current model, also called HiCuM-AL v2.0 (where AL stands for Aging Laws), has been

implemented in the HiCuM compact model. The simulation results for a dynamic stress is presented in figure 3.21. Compared to the initial version of the aging compact model (HiCuM-AL), one observes that the second time interval is accurately modeled using HiCuM-AL v2.0. Therefore, it validates this improved version accounting for the time-invariance of the degradation, making it suitable for RF circuit applications. Moreover, the aging compact model, HiCuM-AL v2.0, has been tested on different SiGe HBT technologies (Infineon, ST Microelectronics and IHP Microelectronics) in [115] ensuring its versatility.

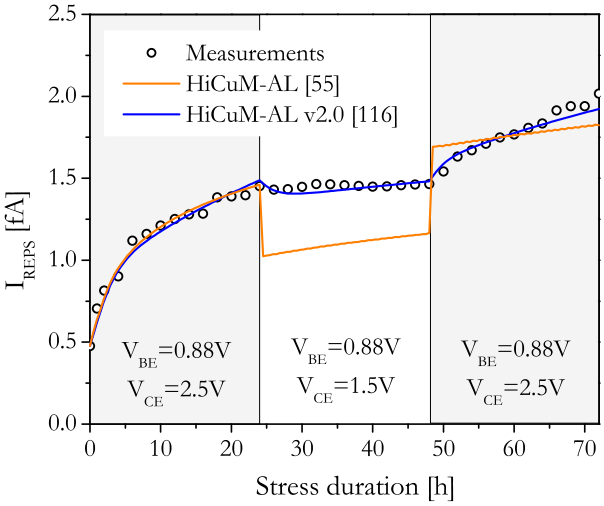


Figure 3.21: Comparison between measurements (symbols) and simulations (solid line) of the previous [54] and newly proposed [115] aging compact model for a dynamic stress on a 8 x 0.16 x 0.52 µm² device corresponding to SG13S technology from IHP Microelectronics.

3.5 Scaled formulation

In [115], some of the degradation features are SiGe HBT architecture-dependent, such as the saturation value of the aging-induced shift in the base current. Indeed, as already demonstrated in the case of HCD in MOSFET architectures [123], the degradation magnitude for SiGe HBTs should depend on the emitter dimensions [114], the Si/SiO_2 interface quality as well as the spacer morphology [119]. Through a first set of results, [112] demonstrates that the trap generation along the interface is quite uniform, meaning that the entire interface-spacer surface suffers from the bond dissociation under mixed-mode stress. Thus, the dimensions of this surface plays an important role in the evolution of the degradation. Since a circuit is usually designed using different device geometries, a scaled formulation for HCD appears to be the next requirement toward circuit reliability simulation. In [114], it was shown that the aging rate scales linearly with the device perimeter. Therefore, a geometrical device scaling has been implemented in HiCuM, through I_{REpS} parameter, based on the lucky electron model [127]. However, for highly down-scaled devices, the lucky electron model has demonstrate limitations with an overestimation of the degradation [128]. In the light of the approach proposed in section 3.4, scaling rules have been incorporated within the aging compact model according to the emitter dimensions and the E-B spacer morphology [119]. This is described hereafter.

3.5.1 Emitter-base spacer morphology

The E-B spacer morphology for B55 technology from ST Microelectronics is sketched in figure 3.22. The traps creation take place at the interface area, A_{SPACER}, which is colored in red in the 3D schematic enlarged in figure 3.22.

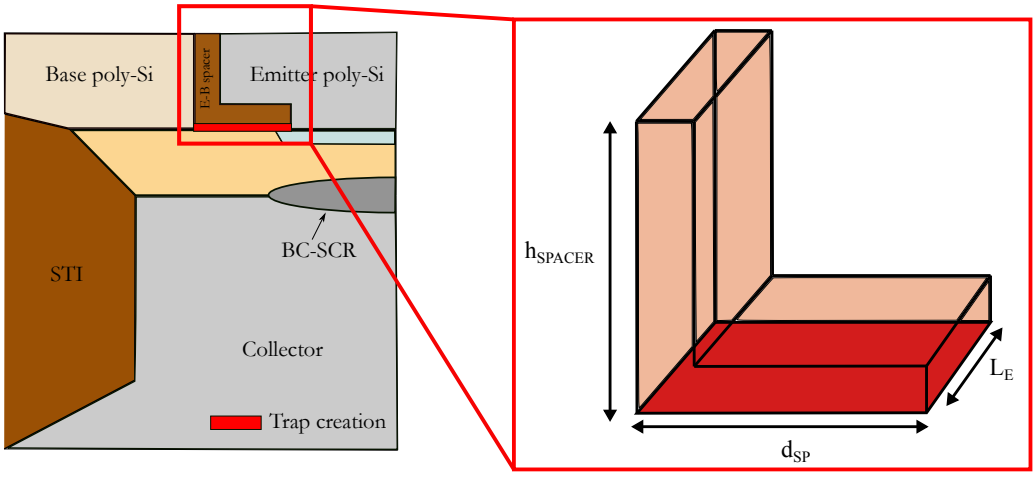


Figure 3.22: Side view of the E-B spacer corresponding to B55 technology transistor architecture from ST Microelectronics.

This parameter depends on the effective emitter length, L_E, the effective emitter width, W_E, the E-B spacer width, d_{SP}, and the number of emitter contacts, N_E. It can be expressed depending on the emitter perimeter, P_E, following equation (3.28).

$$A_{SPACER} = N_E d_{SP}(L_E + W_E + 2d_{SP}) \simeq P_E d_{SP} \tag{3.28}$$

In order to verify the scalability of the hot-carrier degradation mechanism, devices featuring different emitter perimeter are used as presented in table 3.4. Each of them are biased under the same stress condition, *e.g.* a constant V_{CB} value of 2.4 V and a constant J_E value of 231 µA/µm², leading to the same avalanche current density J_{AVL} value of 23 µA/µm² at an ambient temperature of 25°C.

W [μm]	L [μm]	P_E [μm]	A_{SPACER} [μm^2]
0.2	5.56	9.78	0.39
0.2	10	17.78	0.79
0.2	20	35.78	1.60

Table 3.4: Drawn geometry features of devices under test corresponding to B55 technology from ST Microelectronics

From the forward Gummel measurements and using the HiCuM compact model, the I_{REpS} parameter value is extracted for each device dimension and for each stress duration (from 1 s to 10 ks). The resulting plot is presented in figure 3.23a. The maximum value obtained for this

parameter at t = 10 ks is equal to 22 fA for the smallest and 80 fA for the largest geometry, respectively. The relevant information is the increase of I_{REpS} parameter according to the emitter perimeter P_E. Therefore, following equation (3.8), the density of created traps is calculated and plotted as a function of the stress duration in figure 3.23b. Interestingly, it is noticeable, from this plot, that the density of created traps, N_T, is identical for each DUTs (assuming equivalent stress conditions) implying that the degradation mechanism scales with the emitter perimeter.

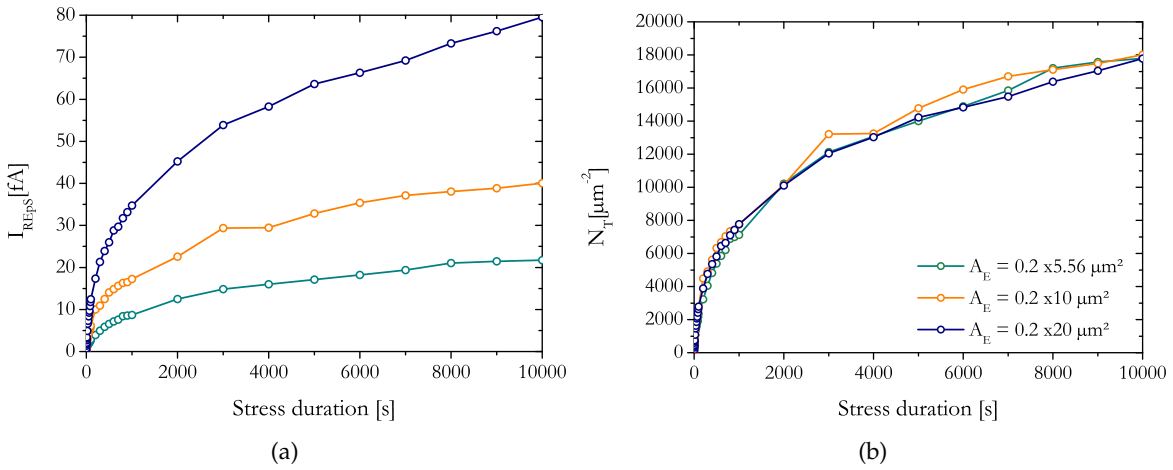


Figure 3.23: (a) Extracted I_{REpS} parameter and (b) Calculated N_T following equation (3.8) from Gummel measurements for a stress condition of V_{CB} = 2.4 V and J_E = 231 µA/µm² and for three B55 technology devices from ST Microelectronics.

3.5.2 Diffusion constant

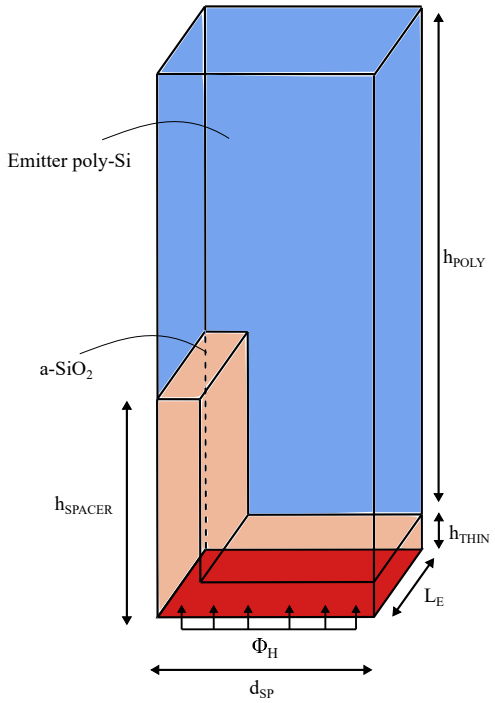
In section 3.4.2, only the diffusion within the E-B spacer oxide has been considered. However, the free H atoms could further diffuse beyond the spacer, through the emitter poly-Si, as illustrated in figure 3.24, according to the diffusion time dependency [129].

This mechanism is governed by the hydrogen diffusion coefficient, D_H, which is material dependent and follows an Arrhenius law as expressed in equation (3.29).

$$D_H = D_0 e^{-E_0/k_B T_j} \tag{3.29}$$

where E_0 is the activation energy, D_0 is the hydrogen diffusion coefficient at an infinite temperature, T_j is the device junction temperature and k_B is the Boltzmann constant.

Many results can be found in the literature for the hydrogen diffusion value in different materials. The diffusion of hydrogen in SiO_2 depends on the intrinsic nature of the material (crystalline or amorphous) [130]. Concerning poly-Si, the diffusion time depends on the doping type (N or P) and the doping level [131]. In SiGe HBTs, the E-B spacer oxide is composed of amorphous SiO_2 (a-SiO_2) where the hydrogen will diffuse faster than in crystalline silicon (c-Si) [132]. The poly-Si from the emitter is highly-doped with type N species. Consequently, the literature results summarized in table 3.5 are specific to the studied HBT architecture. Also, for



(a)

Figure 3.24: Schematic of the hydrogen diffusion volume taking into account the E-B spacer oxide and the emitter poly-Si thickness for B55 technology from ST Microelectronics.

each material, the table lists the hydrogen diffusion parameters and the corresponding diffusion length calculated from equation (3.30) with a diffusion time t_D = 1s and a temperature T = 300K.

$$L_D = \sqrt{4 D_H t_D} \tag{3.30}$$

Material	D_0 [$\mu m^2/s$]	E_a [eV]	L_D [μm] (3.30)
a-SiO_2 [133]	1x10^4	0.18	6.15
poly-Si (N-type) [131]	1x10^{-2}	0.35	2.30x10^{-4}
c-Si [132]	1x10^6	0.48	0.185

Table 3.5: State-of-the-art for hydrogen diffusion parameters in various materials and their corresponding diffusion length L_D for t_D = 1 s and T = 300 K.

From table 3.5, it is obvious that the hydrogen atoms diffuse significantly slower in the poly-Si compared to the other two materials assuming that the grain boundaries acts as efficient traps [134]. Thus, the hydrogen atoms are drastically accelerated within the thin SiO_2 layer until they reach the thicker poly-Si layer where it would be harder to diffuse further efficiently. Considering the time scale used for aging tests, the diffusion inside the spacer is not observable since it only takes a few μs to spread into a few tens of nanometers. As a consequence, only the long-term hydrogen diffusion that takes place inside the poly-Si is observed for long aging tests.

3.5.3 Ladder network scaling

Following the assumptions made in the previous section, the R-C ladder network developed in section 3.4 can be optimized following the same procedure that we have settled in [119]. Primarily, the poly-Si is not a finite barrier to hydrogen diffusion, therefore, the modeling of the second interface acts as an open space, *i.e.* the conductance G is not equal to zero. Secondly, the number of R-C cells, N, is adjusted to limit the number of additional nodes and by taking into account the desired accuracy/complexity trade-off. It was considered a division into three cells (N = 3) for the diffusion modeling as presented in figure 3.25.

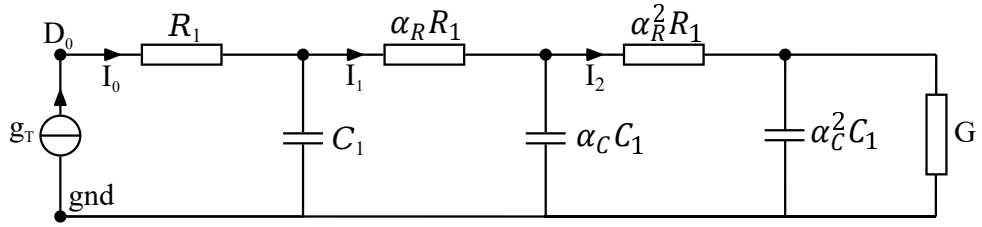


Figure 3.25: R-C ladder network for hydrogen diffusion modeling.

The resistance and capacitance of the network are calculated using equation (3.31) considering the geometrical sequences of equation (3.23).

$$\begin{aligned} C_n &= C_H \frac{\alpha_C^{n-1} - \alpha_C^n}{1 - \alpha_C^N} \\ R_n &= R_H \frac{\alpha_R^{n-1} - \alpha_R^n}{1 - \alpha_R^N} \end{aligned} \tag{3.31}$$

where C_H can be define as the storage capacity of hydrogen atoms and R_H represents the barrier to normal lattice diffusion [135]. Considering a one dimension diffusion, the two recursive factors are identical (α_R=α_C).

The equivalent diffusion volume V_{DIFF} is only composed of the emitter poly-Si leading to equation (3.32).

$$V_{DIFF} = h_{POLY} A_{SPACER} \tag{3.32}$$

Thus, following the definition of C_H parameter, a scaled formulation can be obtained as shown in equation (3.33), which depends on the volume for the diffusion of hydrogen (V_{DIFF}) and the interface trap generation surface (A_{SPACER}). Furthermore, the R_H parameter is calculated using the diffusion constant of hydrogen, D_H, in the considered material as depicted as well in equation (3.33).

$$C_H = \frac{V_{DIFF}}{A_{SPACER}} \qquad R_H = \frac{C_H}{D_H} \tag{3.33}$$

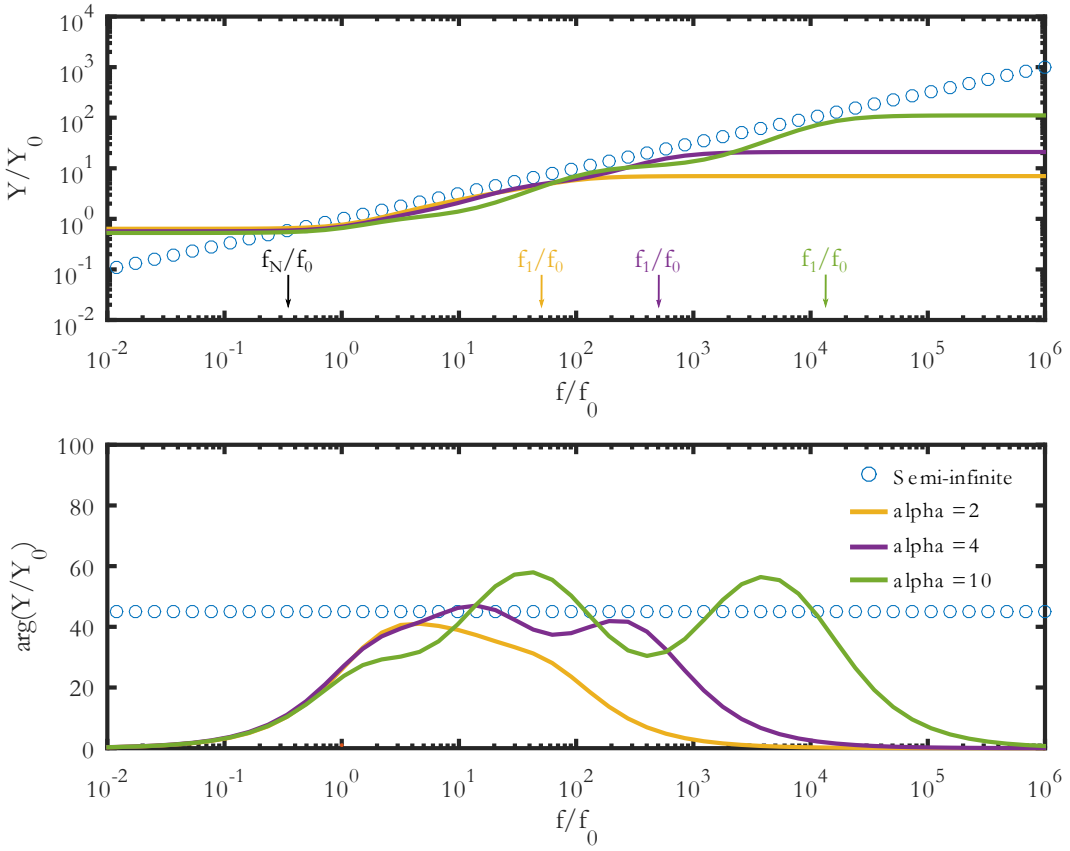


Figure 3.26: Bode-like representation of normalized admittance $\tilde{Y}(0,f) = \tilde{\phi}_H(0,f)/\tilde{N}_H(0,f)$ of the R-C ladder model for N = 3, G = $1/R_N$ and various recursive factors α compared to the semi-infinite theory.

The model parameters for hydrogen diffusion are set up following the previous assumptions and equations with N = 3 and G = $1/R_N$. Consequently, the network admittance at the interface can be compared to the semi-infinite theory as displayed in figure 3.26. Different recursive factors, $\alpha = \alpha_R = \alpha_C$, were proposed to determine the optimum value between the frequency (time) domain validity and the model accuracy. From these simulation results, the recursive factor is set to α = 4 leading to a good accuracy over three decades. The scaled formulation for the hydrogen diffusion enhance the former physic-based aging compact model (HiCuM-AL v2.0) and has been implemented into the latest HiCuM compact model version (HiCuM-AL v3.0). The proposed model is compatible with SiGe HBT device geometries and is computationally efficient for circuit simulations.

3.6 Parameter extraction

The extraction flow of the aging compact model parameters is based on an accurate methodology related to the impact-ionization mechanism and the self-heating effect. In this section, the focus is made on the remaining aging model parameters namely the trap generation rate, K_F, the trap annihilation rate, K_R, and the density of Si-H bonds at the interface, N_F. An extraction procedure on a B55 technology from ST Microelectronics is proposed in the following section which can be, of course, reproduced for other SiGe HBT technologies.

3.6.1 Density of Si-H bonds at the interface

The most reliable method to extract the density of Si-H bonds at the Si/SiO_2 interface is by measuring the recombination current before and after the hydrogen incorporation by heat treatment. Indeed, the difference between the two current levels will give information about the density of passivated traps by hydrogen atoms. However, it requires to measure several devices at different steps of the process fabrication which was not possible during this thesis. Therefore, a first estimation of this density was performed based on the literature results. While there is no available data for SiGe HBT based devices, several works were published for MOS transistors about the reduction of defects at the Si/SiO_2 interface after hydrogen passivation. The initial density of defects at the interface is evaluated around 10^6 μm^{-2} [136]. After the interface oxidation, a two decay reduction is obtained leading to a density of 10^4 μm^{-2} [137]. Finally, the hydrogen treatment allows to reached a defects density of 10^2 μm^{-2} at the Si/SiO_2 interface [136]. Consequently, for MOS transistors, the density of Si-H bonds at the interface can be estimated around 10000 μm^{-2}. This study gives us an order of comparison but is not precise enough for my thesis work.

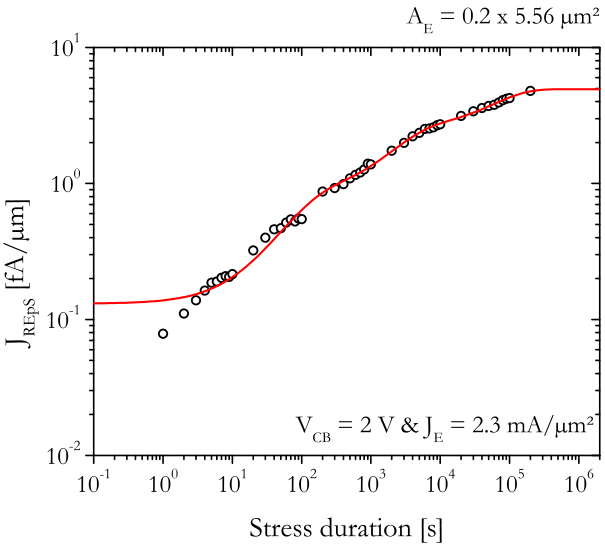


Figure 3.27: Evolution of J_{REpS} for a static condition of V_{CB} = 2 V and J_E = 2.3 mA/µm² on a 0.2 x 5.56 µm² device corresponding to B55 technology from ST Microelectronics. The data were fitted with a three poles exponential decay function to extract the density of Si-H bonds at the interface, N_F.

Consequently, the value of N_F parameter is extrapolated from long term aging stress using the final value of J_{REpS}. Indeed, as presented in section 3.3, the decline of the time power coefficient value along the stress duration has been results from the reduction of the density of available Si-H bonds at the interface. To that end, the data from a long aging stress test (2x10^5 s) have been fitted with a three poles exponential decay function, as plotted in figure 3.27 leading to a final value of J_{REpS} = 5 fA/µm for ST Microelectronics B55 technology. As a safety margin compared to the measurement results, the J_F parameter is set to J_F = 6 fA/µm. Thus, using equation (3.7), this value leads to a calculated N_F equals to 48000 μm^{-2} which is of the same order of magnitude as the literature results. Note that a more precise extraction for J_F parameter could be obtained from a very long aging test without any recovery (*i.e.* at low junction temperature close to the ambient temperature of 25°C).

3.6.2 Generation rate

The generation rate, K_F, must be extracted at the beginning of the base current degradation, when the recovery process is negligible compared to the generation one. In that case, the density of created traps is close to 0 as,

$$N_T(t) - N_T(0) \simeq 0 \tag{3.34}$$

As a consequence, equation (3.9) becomes equation (3.35).

$$\frac{d(N_T(t) - N_T(0))}{dt} = K_F(N_F - (N_T(t) - N_T(0))) - K_R N_H^0 (N_T(t) - N_T(0)) \tag{3.35}$$

Under the boundary condition of equation (3.34), a simplified form of equation (3.35) leads to,

$$\frac{dN_T(t)}{dt} = K_F N_F \tag{3.36}$$

Incorporating equation (3.7) in equation (3.37), K_F parameter can be extracted from the slope of dJ_{REpS}/dt.

$$\frac{dJ_{REpS}}{dt} = \alpha K_F N_F \tag{3.37}$$

The range of aging time for the parameter extraction is limited by defining a maximum deviation of 1% for J_{REpS} compared to its maximum value, J_F, as illustrated in figure 3.28. This condition involves in-between measurements with a short period during the aging test. In the case of the B55 technology from ST Microelectronics for instance, a measurement every second was performed during the first 10 seconds of the mixed-mode stress.

In order to propose a formulation for the generation rate according to the accelerating factors, several stress conditions were chosen as summarized in table 3.6 and in figure 3.29a. The effect

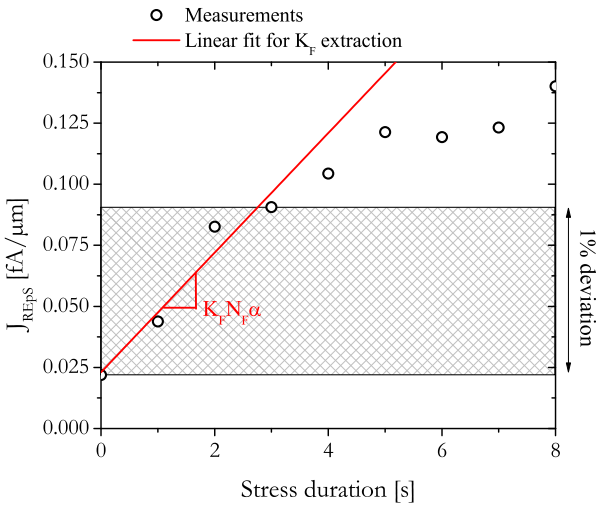


Figure 3.28: K_F extraction example for a static stress condition of V_{CB} = 2 V and J_E = 4.6 mA/µm² on a 0.2 x 5.56 µm² corresponding to B55 technology from ST Microelectronics.

of the base-collector voltage (*e.g.* the BC-SCR electric field) is studied through the stress conditions number 1 and 3. For both conditions, the emitter current density is set to 0.23 mA/µm² leading to a similar junction temperature. The influence of the emitter current density is investigated with the stress conditions number 2, 4 and 5 which are obtained for a fixed V_{CB} of 2 V. These stress conditions leads to an increase of both the junction temperature and the avalanche current. Finally, a last mixed-mode stress is performed at a large V_{CB} of 2.7 V and J_E of 47 mA/µm². This condition favors a relative high junction temperature of 315°C where a particular behavior is observed (see section 3.3). Note that all stress conditions were carefully chosen inside the SOR boundary to avoid both the pinch-in effect and the snapback mechanism.

Number	V_{CB} [V]	J_E [mA/μm^2]	T_j [°C]
1	1.5	0.23	25
2	2	0.46	27
3	2.4	0.23	25
4	2	1.2	31
5	2	4.6	50
6	2.7	47	315

Table 3.6: Details of the stress conditions depicted in figure 3.29a.

The extraction procedure of the generation rate is performed on the stress conditions presented earlier with an exception for the number 6. Indeed, for this particular condition, the base current degradation occurs during the first seconds of the aging test which could not be precisely monitored by the measurement setup. Nevertheless, the extraction results for the five other stress conditions are plotted in figure 3.29b.

As observed in section 3.3, the hot-holes are mainly accelerated by the base-collector electric field value leading to an exponential dependence of the generation rate to this parameter. On the contrary, only a fraction of the hot-carriers will reach the spacer interface and break the Si-H

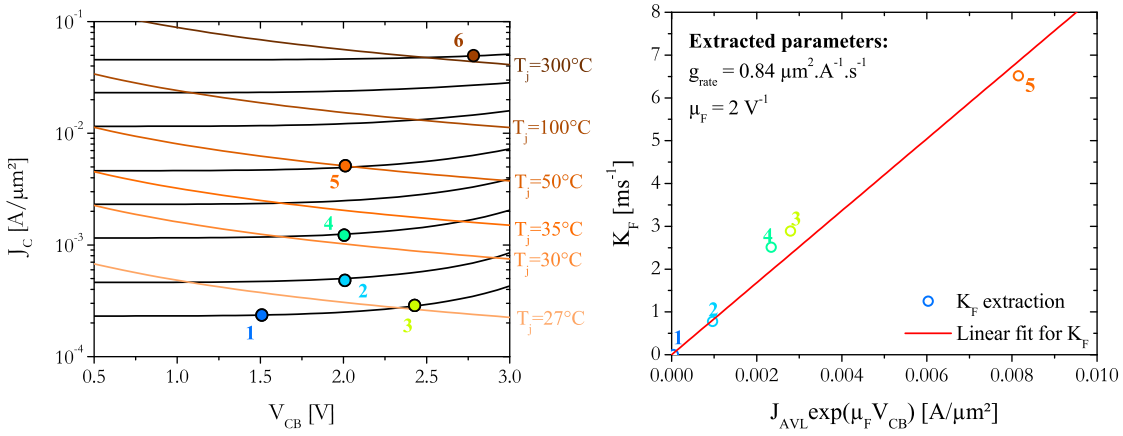


Figure 3.29: (a) J_C - V_{CB} curves illustrating the stress conditions for K_F extraction and (b) K_F extraction results with corresponding linear fit leading to equation (3.38) for five stress conditions (see figure 3.29a) on a 0.2 x 5.56 µm² corresponding to B55 technology from ST Microelectronics.

bonds. Therefore, an expression of K_F parameter is formulated in equation (3.38) as a function of the avalanche current density J_{AVL} and the internal collector-base voltage V_{CiBi},

$$K_F = g_{rate} J_{AVL} \exp(\mu_F V_{CiBi}) \tag{3.38}$$

where g_{rate} is a fitting parameter which represents a fraction of the avalanche current density and μ_F is an exponential factor which governs the acceleration of hot-carriers according to the electric-field. This expression of K_F parameter is consistent with a scaled formulation of the hot-carrier degradation. Note that the temperature dependence of both the avalanche current density and the base-collector voltage is included in HiCuM compact model which results in a suitable temperature-dependent formulation of the generation rate.

3.6.3 Trap annihilation rate

The other mechanism involved in the hot-carrier degradation is the annihilation of trap. Indeed, a re-passivation of the interface traps due to the increase of the device temperature has been highlighted in section 3.3. This temperature increase originates either from the ambient temperature increase (anneal) or from the activation of the device self-heating effect. Consequently, the second term of equation (3.9) depends on the density of hydrogen atoms available at the vicinity of the Si/SiO_2 interface as well as on trap annihilation rate through K_R.

The parameter extraction is performed using the Levenberg-Marquardt optimization algorithm with fixed values of the other aging model parameters, as presented in figure 3.30. The procedure has been repeated for different stress conditions exhibiting a large scale of junction temperature from 25°C to 315°C. The result values were fitted with an Arrhenius law as expressed by equation (3.39).

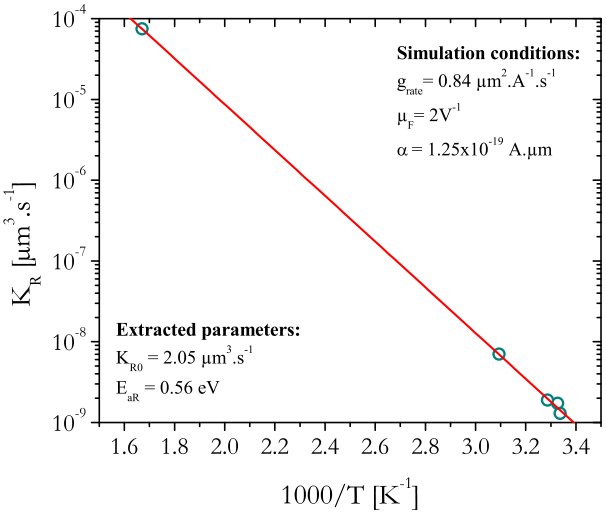


Figure 3.30: K_R extraction results for a 0.2 x 5.56µm² device corresponding to B55 technology from ST Microelectronics. The data are fitted with an Arrhenius law.

$$K_R = K_{R0} \exp\left(-\frac{E_{aR}}{kT_j}\right) \tag{3.39}$$

where T_j is the device junction temperature assessed using the single pole HiCuM thermal node (see chapter 1,section 1.5.2). An excellent fit is obtained for the trap annihilation rate allowing to accurately extract the related model parameters E_{aR}, and K_{R0}. The activation energy, E_{aR}, is extracted from the slope of the linear fit while K_{R0} is extracted from the intersection point at an infinte temperature.

3.7 Simulation results

In order to reduce the simulation time, t_{sim}, compared to the stress duration, t_{stress}, an accelerating time scale factor, ATSF, is defined. This parameter is calculated using equation (3.40) [138].

$$ATSF = \frac{t_{stress}}{t_{sim}} \tag{3.40}$$

Note that, for DC stress, the aging simulation should be performed when the transistor steady-state is reached. Consequently, the simulation time is settled according to the device thermal time constant (typically around a few hundred of nanosecond). In the following sections, the aging compact model as well as the extraction procedure accuracy set up verified for both ST Microelectronics and IHP Microelectronics technologies.

3.7.1 ST Microelectronics technology

First, the model accuracy is verified for the stress conditions displayed in figure 3.29a on a 0.2 x 5.56 µm² SiGe HBT device. The comparison between the aging measurements (symbols) and the simulations (lines) is presented in figure 3.31a where a very good accuracy is achieved for all stress conditions. These results validates the formulation of both the trap generation rate, K_F, and the temperature dependence of the annealing rate, K_R. Interestingly, the stress condition at high junction temperature (brown curve in figure 3.31a) demonstrates that the dynamic equilibrium between the trap generation and annihilation is well captured by the aging compact model.

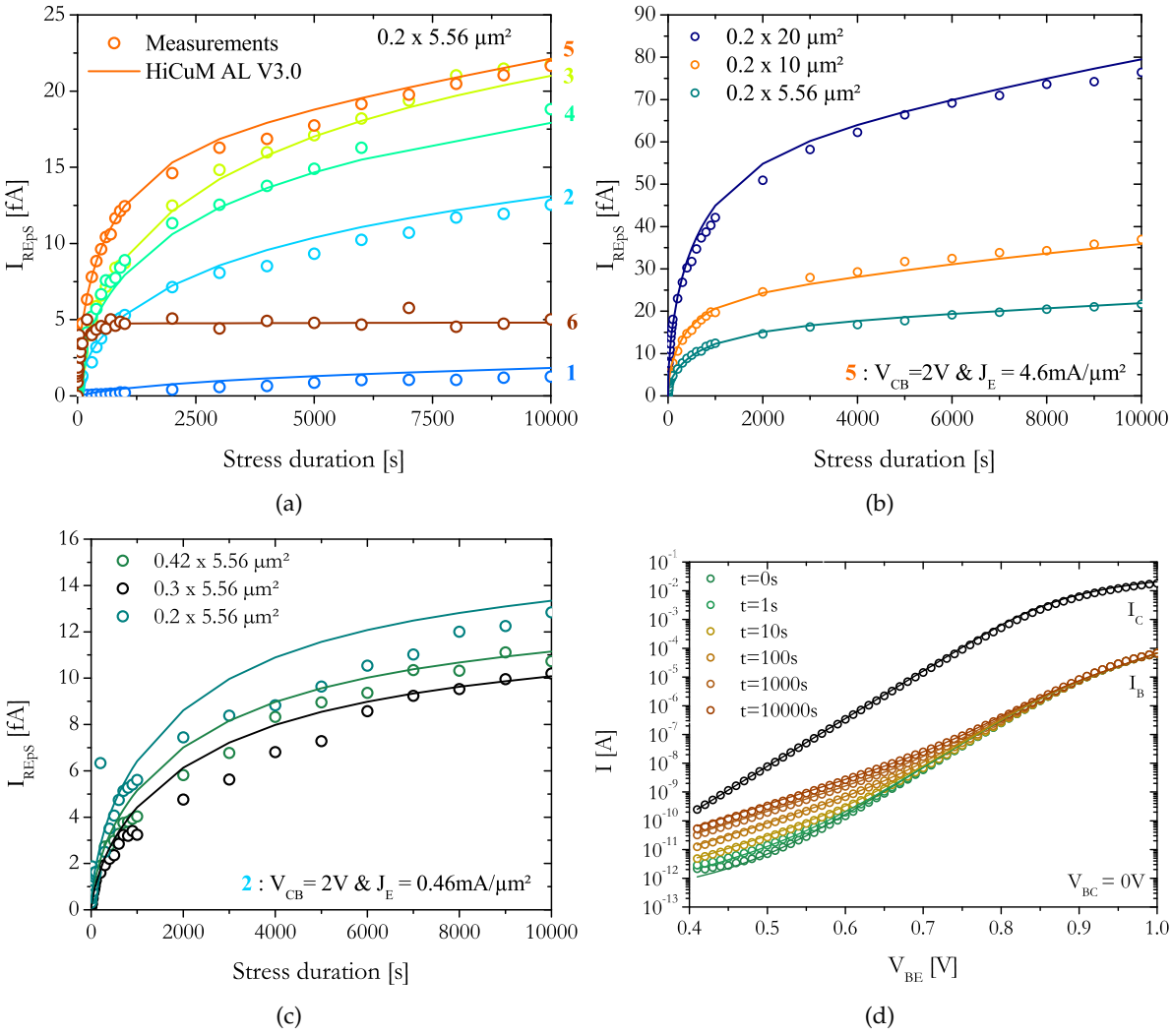


Figure 3.31: HiCuM-AL v3.0 simulations (lines) vs measurements (symbols) for I_{REpS} evolution according to the stress duration at (a) various stress conditions (see figure 3.29a), (b) various L_E, (c) various W_E and (d) Gummel evolution for a static stress condition of V_{CB} = 2 V and J_E = 4.6 mA/µm² on devices corresponding to B55 technology from ST Microelectronics.

Then, the model is validated on various devices featuring various emitter lengths from 5.56 µm to 20 µm for a constant emitter width of 0.2 µm. Each device is biased under a comparable stress condition of V_{CB} = 2 V and J_E = 4.6 mA/µm². The simulation results are displayed in

figure 3.31b and compared to the aging extraction results of I_{REpS} parameter where an excellent agreement is obtained for the three devices.

Additionally, the scalability of HiCuM-AL v3.0 compact model is tested on three emitter widths ranging from 0.2 to 0.42 µm for a constant emitter length of 5.56 µm. The three devices were submitted to a mixed-mode stress of V_{CB} = 2 V and J_E = 0.46 mA/µm². The I_{REpS} parameter evolution is presented in figure 3.31c where it can be observed a close behavior between the three devices.. The measurements results were compared to the simulated ones on the same figure and a good accuracy is achieved for all devices. The results from figure 3.31b and figure 3.31c allows to validate the scaled formulation of the aging compact model.

A final validation is performed through simulation of the Gummel plots according to the stress duration for a static stress condition of V_{CB} = 2 V and J_E = 4.6 mA/µm². The measurement and the simulation results using HiCuM-AL v3.0 are presented in figure 3.31d. Once again, the base current increase is very well predicted by the HiCuM-AL v3.0 aging compact model along the stress duration.

3.7.2 IHP technology

The extraction procedure presented in section 3.6 is repeated for IHP Microelectronics technology to validate the aging compact model versatility. As for ST Microelectronics, the HiCuM-AL v3.0 aging compact model is applied on various stress conditions on a 8 x 0.16 x 0.52 µm² device. In figure 3.32a, three devices are submitted to aging tests featuring a constant J_E of 0.12 mA/µm² and a V_{CB} value ranging from 2.5 V to 3 V. The base current simulation results exhibit a good accuracy compared to the measurement ones for the three stress conditions.

Likewise, the aging compact model is validated on stress conditions featuring different emitter current density values ranging from 0.12 to 6 mA/µm² for a constant V_{CB} of 2.75 V as observed in figure 3.32b. Equally, a good agreement between the simulation and the measurements results is obtained for all statics conditions. The versatility of the aging compact model is therefore verified thanks to accurate results for both technologies.

Moreover, figure 3.32c presents the simulation results for both the static and the dynamic mixed-mode stress already described in section 3.3. The relative base current degradation for a static condition of V_{CB} = 3 V and I_E = 0.13 mA is accurately reproduced by the simulation results. Concerning the dynamic mixed-mode stress, the recovery phases are correctly accounted for by the aging compact model with a reduction of the relative base current degradation compared to the static mixed-mode stress. Discrepancies between measurements and simulations appears for a stress duration larger than 2000 s which could be due to some measurement inaccuracies or/and a technological variability of the aging model parameters. Nevertheless, these errors are smaller than the 10% error margin commonly used by the modeling community.

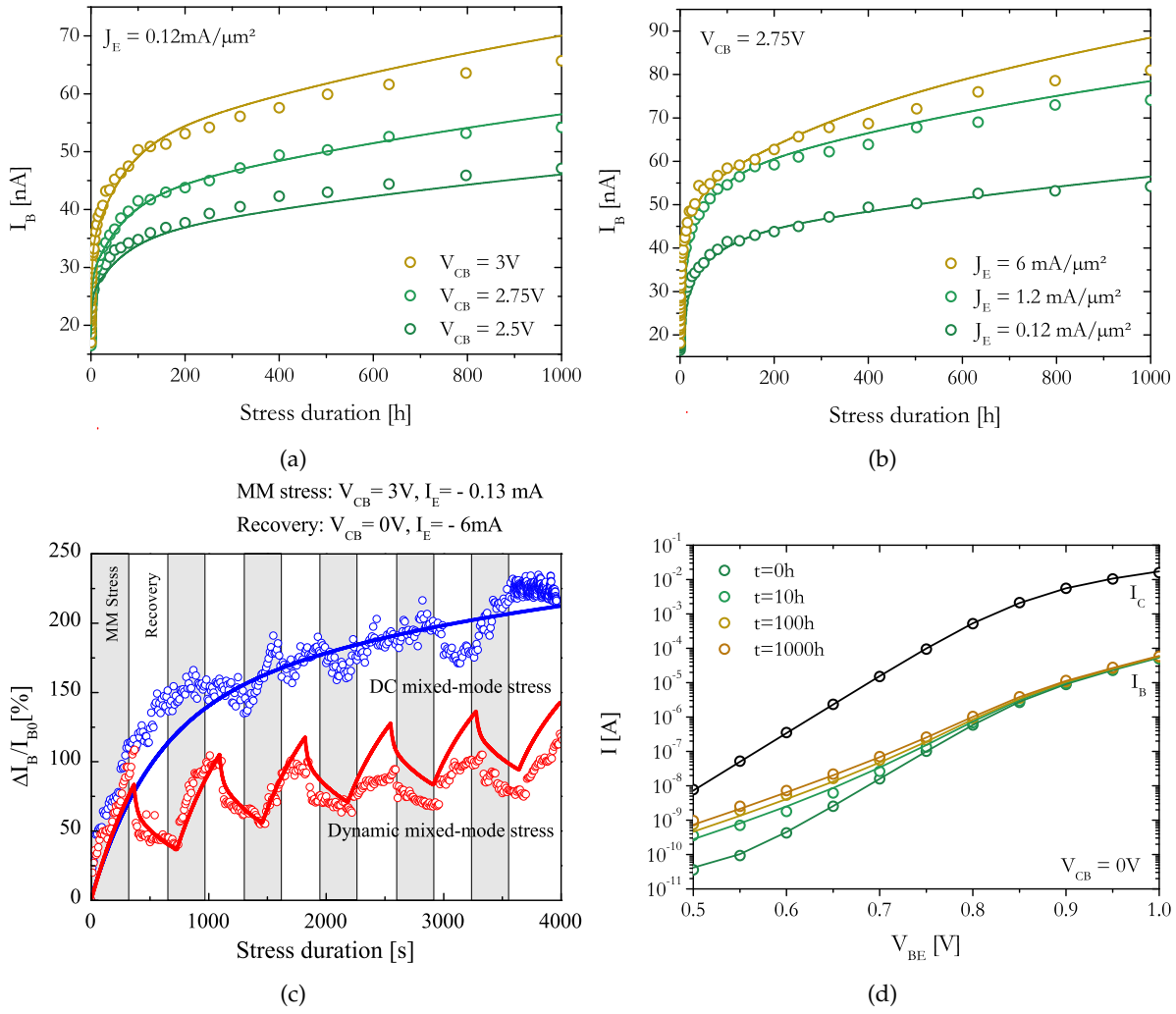


Figure 3.32: HiCuM-AL v3.0 simulations (lines) vs measurements (symbols) for I_B evolution according to the stress duration at (a) various V_{CB}, (b) various J_E, (c) under a dynamic stress condition and (d) Gummel Gummel evolution for a static stress condition of V_{CB} = 3 V and J_E = 0.12 mA/µm² on a 8 x 0.16 x 0.52 µm² device corresponding to SG13S technology from IHP Microelectronics.

Finally, a last validation is performed on Gummel characteristics for a mixed-mode stress of V_{CB} = 3 V and J_E = 0.12 mA/µm² up to 1000h of stress. The comparison between the measurements and the simulation results is depicted in figure 3.32d where the base current evolution is very well captured by the aging compact model for all stress durations.

3.8 Conclusion

The third chapter was devoted to the description and the modeling of hot-carrier degradation occurring in SiGe HBT devices under mixed-mode stress conditions. This stress mode results from a device operation close to the safe-operating-area edges where both the avalanche and the self-heating effect dominate the transistor electrical behavior.

Under such operating conditions, an increase of the base recombination current through the

Shockley-Read-Hall mechanism is reported for SiGe HBT devices. This degradation originates from the creation of hot-carriers within the base-collector space charge region due to the impact-ionization mechanism. Those carriers can reach Si/SiO_2 interfaces and dissociated the Si-H bonds initially created during the annealing treatment. Through a dedicated aging test campaign, the created interface defects, which act as traps, were located near the emitter-base spacer oxide interface. This outcome was correlated to TCAD simulation results where the addition of traps at the spacer oxide interface leads to the increase of the base recombination current. Moreover, in a compact modeling approach, the HiCuM model parameter impacted by the hot-carrier degradation has been clearly identified as the peripheral base-emitter recombination saturation current parameter, I_{REpS}. A proportionality relation between this model parameter and the density of created traps at the Si/SiO_2 interface has been established allowing to accurately associate the physical mechanism occurring in the transistor to the electrical behavior.

As the device electronic function has been altered over the time, a predictive software tool has been developed to assess the evolution of this degradation. To that end, an aging compact model has been derived from the reaction-diffusion theory adapted to SiGe HBT features. The invariance in time has been ensured thanks to the implementation of a recursive network modeling the diffusion of hydrogen within the transistor. This formulation called HiCuM-AL v2.0 has been implemented in HiCuM compact model and has demonstrated a very good accuracy for three HBT architectures from ST Microelectronics, IHP Microelectronics and Infineon. In addition, the aging compact model allows to accurately predict the base current degradation under dynamic operating conditions, making it largely suitable for RF circuit applications.

Furthermore, a scaled formulation, HiCuM-AL v3.0, of the hydrogen diffusion has been proposed based on the emitter-base spacer morphology which guarantee the model versatility in term of HBT architecture and dimensions. As a matter of fact, based on the literature results, the emitter polysilicon demonstrates a poor diffusion coefficient which indicates that the hydrogen atoms will be stored within this diffusion volume. Therefore, the diffusion model has been scaled according to the diffusion coefficient and the equivalent capacity volume of the emitter poly-silicon allowing to reduce the number of model parameters compared to the HiCuM-AL v2.0 ones.

Additionally, a reliable extraction procedure of the aging model parameters has been proposed on a B55 technology from ST Microelectronics which can be reproduce on other technologies. Especially, since the impact-ionization is responsible for hot-carriers creation, the trap generation rate expression has been adapted following the last update on the avalanche effect resulting in a geometry dependent formulation [119]. On its side, the trap annihilation rate has exhibited a dependence according to the ambient and/or junction temperature following an Arrhenius law.

The aging compact model, HiCuM-AL v3.0, together with its scaling rules has demonstrated an excellent accuracy under various stress conditions (V_{CB} values ranging from 0 V to 3 V

and I_E values ranging from 100 µA to 20 mA) as well as on various HBT architectures (ST Microelectronics and IHP Microelectronics) featuring different configurations (CBEBC and CBE), emitter widths (from 0.12 to 0.42 µm) and emitter lengths (from 0.52 to 20 µm). Owing to its physical basis, this compact model can provide accurate reliability predictions for circuits operating close or even beyond the conventional safe-operating-area. This aspect will be further discussed in the next chapter.

Chapter 4

Hot-Carrier Degradation Impact on Integrated Circuits

Contents

4.1 Introduction

This chapter presents the reliability assessment of several basic integrated circuits used for analog and RF applications based on a wide range of circuit simulations using the aging compact model presented in the previous chapter (HiCuM-AL v3.0). First, due to its extensive use in integrated circuit blocks, a study of different current mirror configurations submitted to mixed-mode stress is reported. Then, according to the previous simulation results, the robustness of a ring oscillator is investigated. Finally, in the last section, aging measurements and simulation are carried out on a broadband amplifier thus verifying the aging compact model validity for circuit applications.

4.2 Current mirrors

One of the most basic building block used in analog and RF circuits is the current mirror employed as a biasing element or an active load for amplifier stages [139]. The structure commonly provides an output current, I_{OUT}, proportional to a reference input current, I_{IN}. The basic figure of merit describing the operation of a current mirror is the transfer current ratio described in equation (4.1).

$$\eta = \frac{I_{OUT}}{I_{IN}} \tag{4.1}$$

Ideally, this factor must be independent of the supply voltage and/or temperature variations. Consequently, the current mirror output resistance, R_{OUT}, must be as large as possible in order to reduce the dependence of the output current on the output voltage. Moreover, the voltage drop across the output part of the mirror must be minimized to increase the range of output voltage for which the current-mirror output resistance is almost constant. The current gain error is defined as the difference between the copying current (*i.e.* the output current) and the referenced one (*i.e.* the input current).

From a reliability study point of view, the current mirror is an interesting study case block as its transfer current ratio depends on the transistor current gain which might be altered during hot-carrier injection (see chapter 3). Indeed, as presented in [122], the aging of a current mirror results in a decreasing transfer ratio at low and moderate input current levels. This degradation could have an impact on the circuit electrical characteristics since the biasing current, featuring current source scheme, isn't constant over the time [140]. Consequently, as a study case, an in-depth study of the reliability of current mirrors is required to assess the lifetime of analog and RF circuits. The investigations are performed on the 55nm BiCMOS technology from ST Microelectronics.

4.2.1 Architectures

The study is based on four simulated current mirror configurations: simple, cascode, Wilson and balanced Wilson, depicted in figure 4.1. Each transistor, T_1, T_2, T_3 and T_4 feature the same emitter dimensions of 0.2 x 5.56 µm². The detailed electrical characteristics of each architecture are summarized in table 4.1 including the transfer ratio, η, the input resistance, R_{in}, the output resistance, R_{out}, the minimum input voltage, $V_{in(min)}$, and the minimum output voltage, $V_{out(min)}$. The transfer ratio is detailed according to the current gain of each transistors (*i.e.* β_1 for T_1, β_2 for T_2, etc ...)

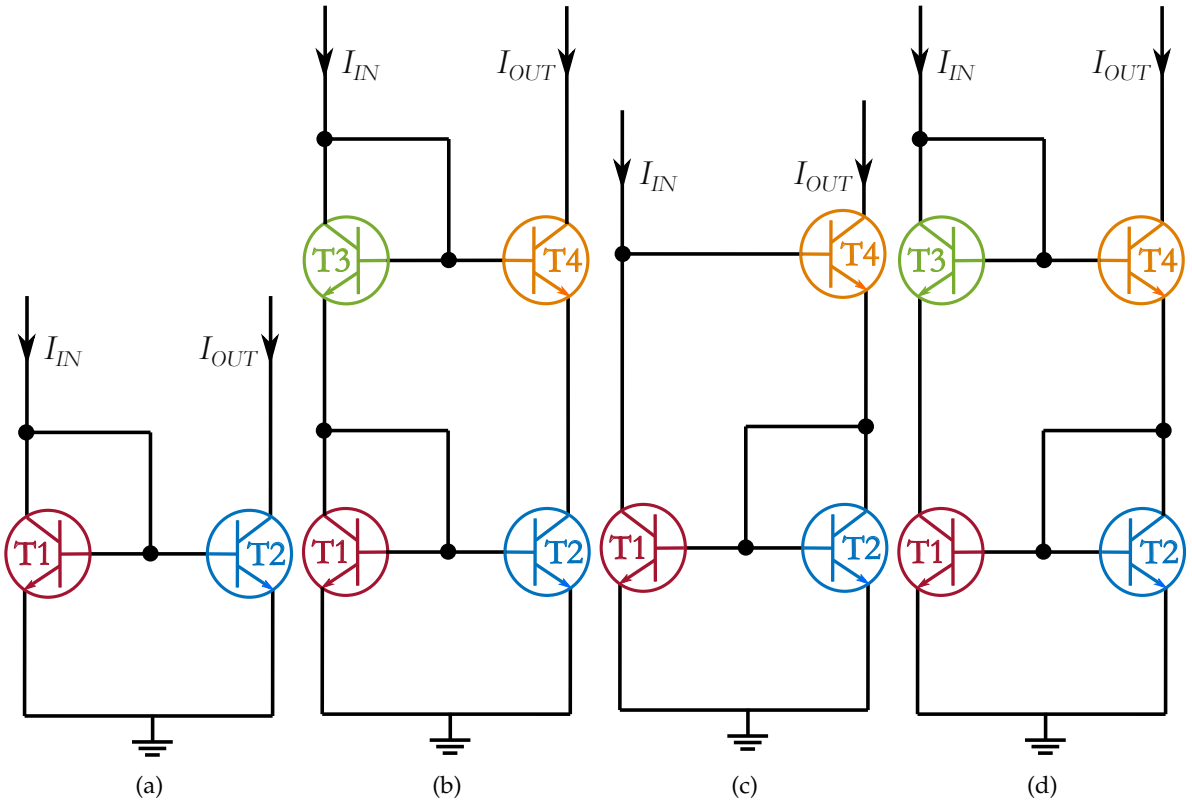


Figure 4.1: Schematic of (a) the simple, (b) the cascode, (c) the Wilson and (d) the balanced Wilson current mirrors.

Simple current mirror

The simplest form of a current mirror consists of two transistors as presented in figure 4.1a. The transistor T_1 is diode connected implying that the base-collector junction is off. Both transistors are assumed to operate in the forward-active region with infinite output resistances. The current gain error for this configuration is only due to the base current of transistors T_1 and T_2, which, thereby, causes a variation of the output current compared to the input current.

Cascode current mirror

The cascode current mirror presented in figure 4.1b features a very high output resistance. This current mirror architecture is based on a stack of two simple current mirrors (T_1 being associated with T_2 and T_3 being associated with T_4). To improve the matching, emitter resistances can be added at the bottom part of the structure.

Wilson current mirror

The Wilson current mirror presented in figure 4.1c overcomes some limitations of the cascode current mirror. Indeed, this circuit uses a negative feedback through T_2 device which reduces the base current of T_1. Consequently, the current gain error arising from finite β is reduced compared to the cascode architecture. However, a mismatch between T_1 and T_2 collector-emitter voltages appears which increases the gain error between the input current and the output current.

Balanced Wilson current mirror

The balanced Wilson current mirror presented in figure 4.1d is an improved version of the Wilson structure. In the case of balanced Wilson current mirror, the use of the symmetrical cascode transistors balances out the collector-emitter voltages of T_1 and T_2 removing any mismatch between T_1 and T_2 arising from the Early effect in T_1 transistor. Also, the current gain is no longer dependent on the imbalance between the two voltages which largely extends the linear operating range of the circuit.

Features	Simple	Cascode	Wilson	Balanced Wilson
η	$\frac{1}{1+\frac{1}{\beta_1}+\frac{1}{\beta_2}}$	$\frac{\beta_1\beta_2\beta_4}{(\beta_4+1)(\beta_1\beta_2+\beta_2+\beta_1)+\beta_1\beta_2}$	$\frac{\beta_4(A\beta_1\beta_2+\beta_1+A\beta_2)}{\beta_1\beta_2(\beta_4+1)+A\beta_1\beta_2+A\beta_1+\beta_2}$ with $A=(1+\frac{V_{CE2}-V_{CE1}}{V_{CE1}+V_A^*})$	A = 1
R_{in}	$\frac{1}{g_{m1}}$	$\frac{1}{g_{m1}}+\frac{1}{g_{m3}}$	$\frac{g_{m2}+g_{m4}}{g_{m1}g_{m4}}$	$\frac{g_{m2}+g_{m4}}{g_{m1}g_{m4}}$
R_{out}	${r_{ce2}}^{**}$	$r_{ce4}(1+g_{m4}r_{ce2})+r_{ce2}$	$\frac{g_{m4}r_{ce4}r_{ce1}r_{be4}}{2r_{ce1}+r_{be4}}$ ***	$\frac{g_{m4}r_{ce4}r_{ce1}r_{be4}}{2r_{ce1}+r_{be4}}$
$V_{in(min)}$	$V_{BE(on)}$	$2V_{BE(on)}$	$2V_{BE(on)}$	$V_{BE(on)}+V_{CE1(sat)}$
$V_{out(min)}$	$V_{CE2(sat)}$	$V_{CE4(sat)}+V_{BE(on)}$	$V_{CE4(sat)}+V_{BE(on)}$	$V_{CE4(sat)}+V_{BE(on)}$

* Early voltage
** Output resistance from the small-signal hybrid π model
*** Input resistance from the small-signal hybrid π model

Table 4.1: Current mirrors electrical characteristic equations.

4.2.2 Standard operation

The electrical performances of each current mirror architectures is evaluated under standard operating conditions (*i.e.* without the activation of the aging compact model) based on the

study proposed in [141] for MOS based current mirrors. First, the transfer current ratio, η, evolution according to the input current at V_{OUT} = 1.5 V is plotted in figure 4.2a for the four current mirror architectures. For low input currents (ranging from 1 µA to 100 µA), the four configurations achieve a transfer current ratio close to 1 ensuring a very good mirroring accuracy. However, at high currents (ranging from 100 µA to 10 mA), some discrepancies are observed on the current transfer characteristic, except for the cascode and the balanced Wilson current mirrors. The simple current mirror operates as an amplifier since the transfer ratio increases up to 2.75 for I_{IN} = 10 mA. On the contrary, for the Wilson current mirror, a drop in the transfer current ratio is observed down to 0.5 for I_{IN} = 10 mA. Therefore, for these two configurations, the mirroring accuracy is not guaranteed for operation at high currents. In order to offer a fair comparison, the electrical performance of each architecture is studied for an input current of 100 µA and an output voltage of V_{OUT} = 1.5 V. The corresponding frequency response of the transfer ratio for this operating condition is shown in figure 4.2b for the four current mirror architectures. Both the Wilson and the balanced Wilson current mirrors exhibit the largest bandwidth of 30 GHz compared to 12 GHz and 2 GHz for the simple and the cascode current mirrors, respectively. Moreover, a peaking in the frequency response of 0.36 dB is observed for the balanced Wilson configuration.

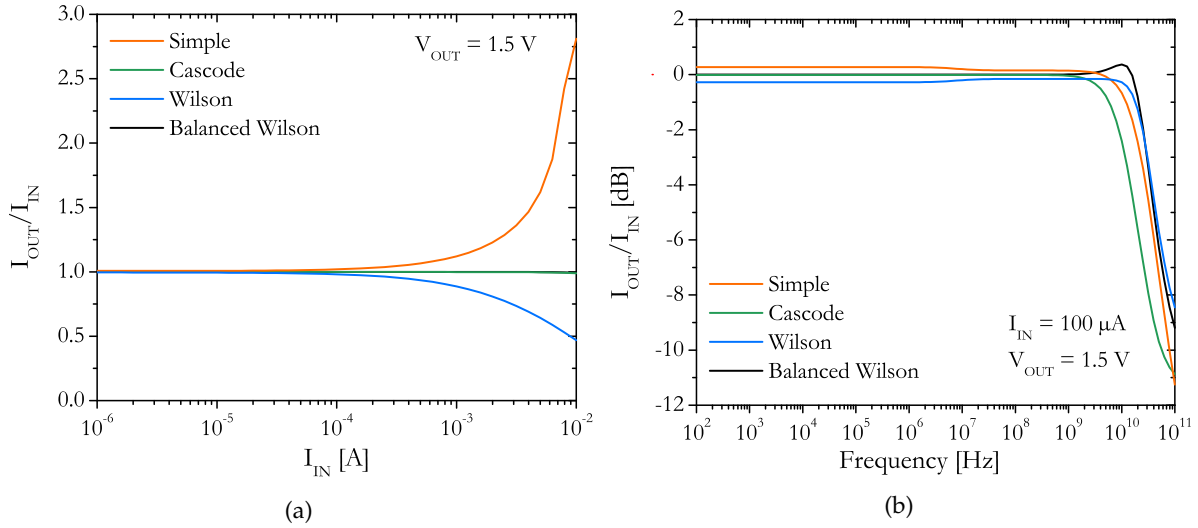


Figure 4.2: Transfer ratio evolution for V_{OUT} = 1.5 V according to (a) the input current and (b) the frequency at I_{IN} = 100 µA.

Figure 4.3a presents the evolution of the input voltage according to the input current for an output voltage of 1.5 V. This input voltage achieves values ranging from 0.5 V to 0.9 V for the simple current mirror while it is between 1 V and 1.8 V for the three other configurations. The improvements achieved in cascode, Wilson and balanced Wilson are at the cost of two times increase of the input compliance voltage compared to the simple current mirror. The frequency response of the input resistance is displayed in figure 4.3b for the four architectures at V_{OUT} = 1.5 V and I_{IN} = 100 µA. In accordance with the observations of figure 4.3a, the input resistance of the cascode, the Wilson and the balanced Wilson current mirror is higher (R_{in} = 525 Ω) than the one for the current mirror source (R_{in} = 265 Ω).

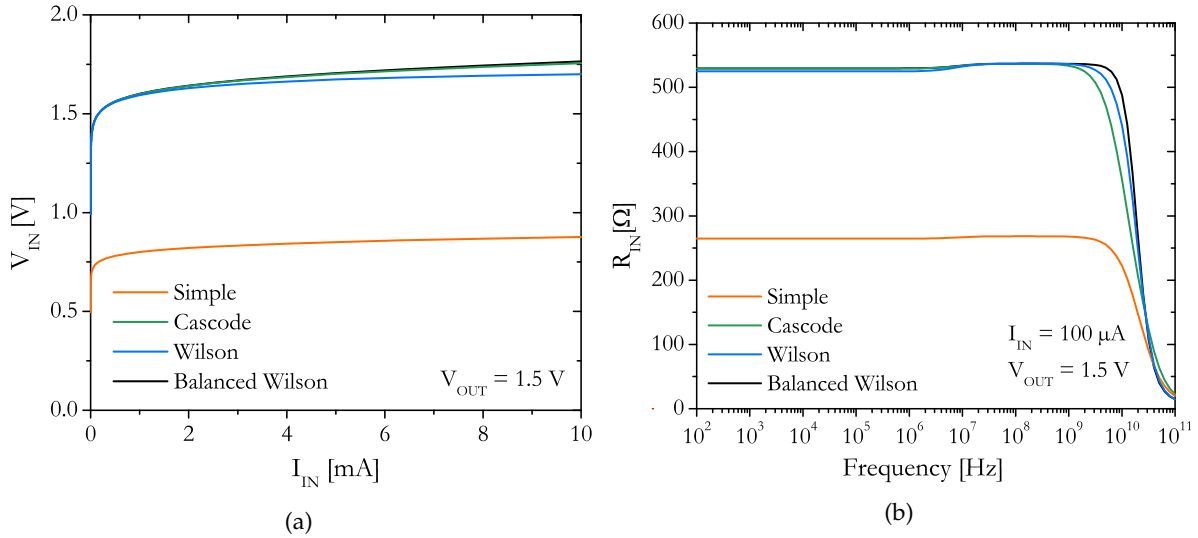


Figure 4.3: (a) Input voltage evolution according to the input current for V_{OUT} = 1.5 V and (b) Input resistance evolution according to the frequency for V_{OUT} = 1.5 V and I_{IN} = 100 µA.

Figure 4.4a illustrates the variation of the output current according to the output voltage for I_{IN}=100µA where some differences are observed between the four configurations. Due to its architecture, the simple current mirror exhibits a linear operation for V_{OUT} values ranging from 0.3 V to 1.5 V. At higher voltages, the impact ionization mechanism is activated which leads to an increase of the output current. For the three other current mirror architectures, the behavior is quite similar featuring a range of operation for V_{OUT} ranging from 0.9 V and 3 V. For higher output voltages values, as for the simple current mirror, the impact-ionization mechanism is activated. Note that, for this reason, the avalanche susceptibility threshold appears less important in the case of the cascode, the Wilson and the balanced Wilson (V_{OUT} = 4 V) than in the case of the simple current mirror one (V_{OUT} = 2 V).

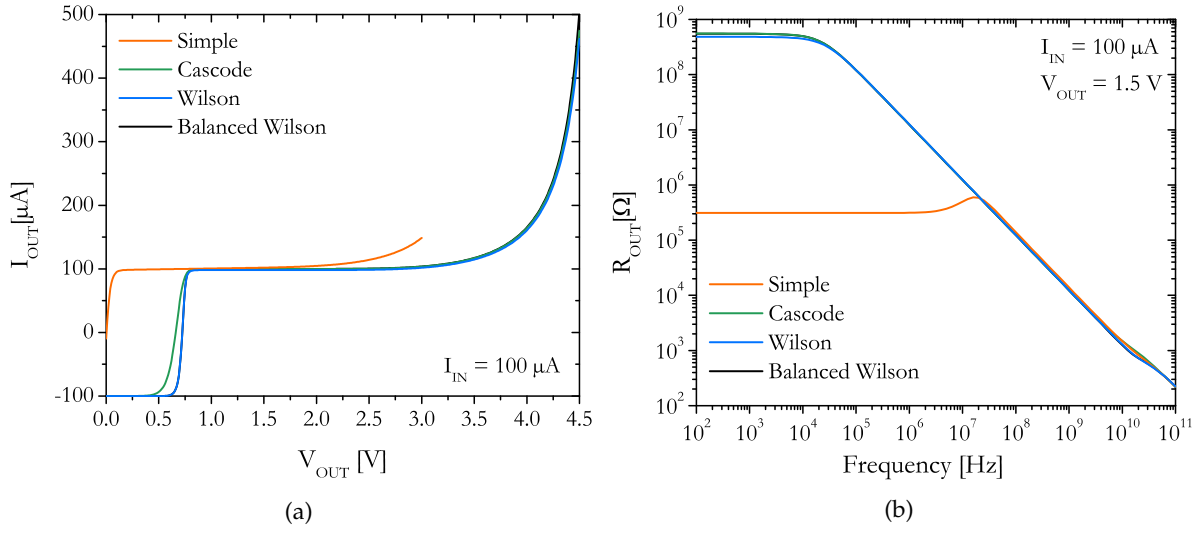


Figure 4.4: (a) Output current evolution according to the output voltage for I_{IN} = 100 µA and (b) Output resistance evolution according to the frequency for V_{OUT} = 1.5 V and I_{IN} = 100 µA.

The frequency behavior of the output resistance is plotted on figure 4.4b for the four architectures at V_{OUT} = 1.5 V and I_{IN} = 100 µA. While the output resistance is equal to 300kΩ for the simple current mirror, a higher value of this parameter is observed for the three other configurations with R_{out} = 500 MΩ. This discrepancy is consistent with the equations displayed on table 4.1.

The comparative results between the four configurations is given in table 4.2. In summary, the improvements in terms of mirroring accuracy, output resistance and bandwidth for the cascode and the balanced Wilson current mirrors compared to the Wilson and the simple current mirror ones are achieved at the cost of higher minimum input and output voltage leading to an increase of the power consumption.

	Units	Simple	Cascode	Wilson	Balanced Wilson
Mirroring accuracy[1]	-	Very poor	Very good	Poor	Very good
$V_{in(min)}$[1]	V	0.5-0.9	1-1.8	1-1.8	1-1.8
$V_{out(min)}$[1]	V	0.1-0.3	0.9-1.1	0.9	0.9-1.1
R_{IN}[2]	Ω	265	530	525	530
R_{OUT}[2]	Ω	311 k	485 M	550 M	550 M
Bandwidth[2]	Hz	12 G	30 G	2 G	30 G
Power consumed[2]	W	225 µ	297 µ	294 µ	298 µ

[1] For input current range 0 - 10 mA
[2] At input current = 100 µA

Table 4.2: Comparative results of basic current mirror architectures.

4.2.3 Reliability

The reliability analysis of each current mirror configurations is performed for a maximum stress duration of 1000 h using a transient simulation time of 10 µs (ATSF = $3.6x10^{11}$). The aging compact model, HiCuM-AL v3.0, is activated for each transistors by settling the aging flag model parameter to 1. Two particular criterion are chosen to assess the robustness of the current mirrors: the I_{REpS} parameter which represents the sensitive parameter to hot-carrier degradation in the aging compact model and dI_{OUT} which illustrates the output current variation according to the initial one (at t=0s).

Standard operating condition

First, the reliability of each configurations is evaluated under the standard operating conditions of I_{IN} = 100 µA and V_{OUT} = 1.5 V. The corresponding transistor operating conditions for each current mirror configuration is reported in figure 4.5. From this plot, one observes that only two transistors operate close to the safe-operating-area edges: the transistor T2 from the simple current mirror source and the transistor T1 from the Wilson one. Consequently, the weak avalanche mechanism is activated for both transistors due to their operation close to the BV_{CEO}.

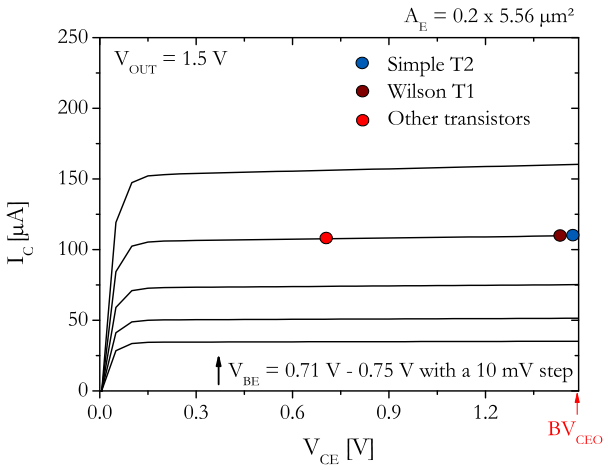


Figure 4.5: I_C vs V_{CE} output characteristics highlighting the transistors operating conditions for each current mirror configurations at V_{OUT} = 1.5 V and I_{IN} = 100 µA.

The evolution of the output current according to the stress duration is displayed in figure 4.6a for the four configurations. While the output current of the cascode and the balanced Wilson configurations does not evolve significantly over time, a variation of -1.5nA and 1.25nA is observed for the simple and the Wilson current mirror, respectively. However, regarding the transfer ratio evolution in figure 4.6b, this deviation can be neglected since it represents less than 1% of the input current.

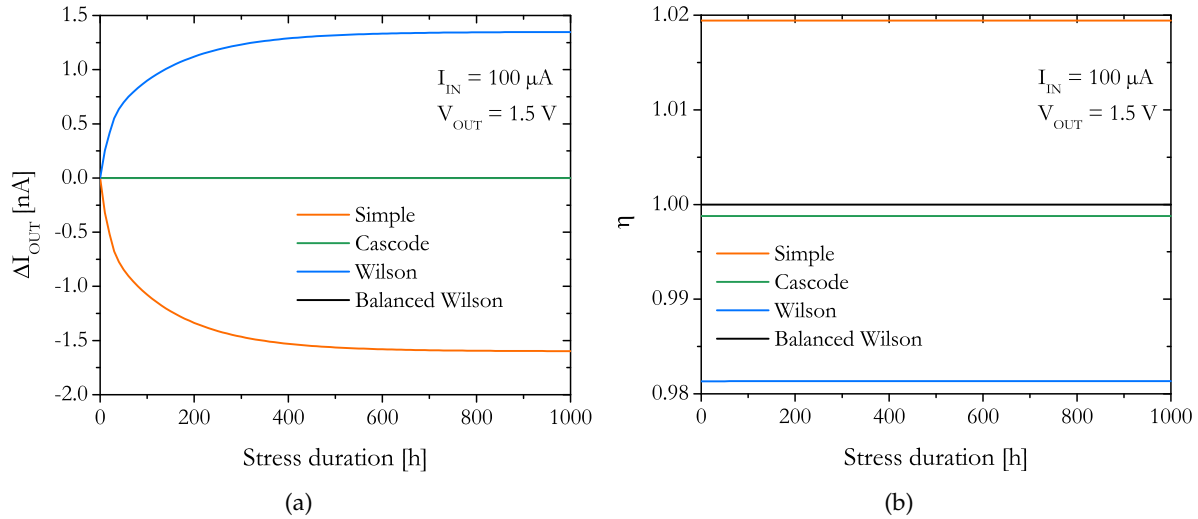


Figure 4.6: (a) Output current and (b) transfer ratio evolution according to the stress duration for I_{IN} = 100 µA and V_{OUT} = 1.5 V.

For the same operating condition, the evolution of I_{REpS} parameter of each transistor for each current mirror configurations is presented in figure 4.7 according to the stress duration. In accordance with the theory, no increase of the recombination current is observed for diode mounted transistors since the impact-ionization mechanism cannot be activated. An increase of I_{REpS} up to 1 fA can be highlighted for the transistor T_2 of the simple current mirror. Indeed, due to the operation close to the BV_{CEO} (see figure 4.5), the impact-ionization mechanism is

activated for this transistor resulting in a negative base current. Accordingly, the increase of the recombination current results in a less pronounced base current (in absolute value) which easily explained the negative shift of the output current observed in figure 4.6a. On the contrary, for the Wilson current mirror, an increased of the I_{REpS} parameter up to 0.9 fA leads to a positive shift of the output current due to a positive base current for this operating condition.

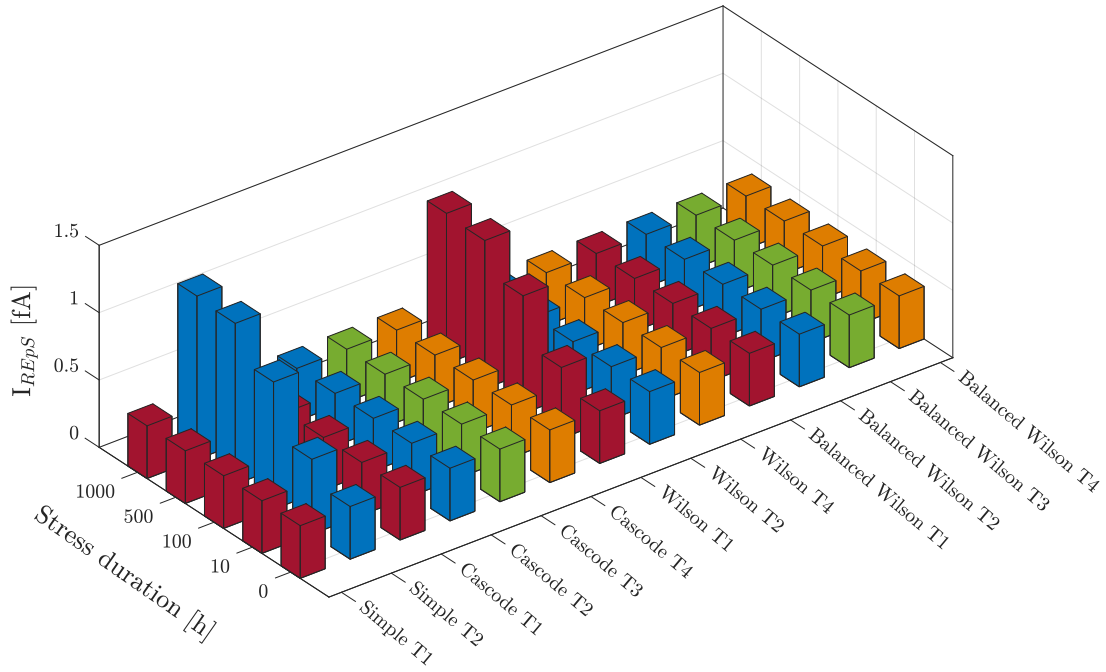


Figure 4.7: Evolution of I_{REpS} parameter according to the stress duration for the different transistors and current mirror configurations for I_{IN} = 100 µA and V_{OUT} = 1.5 V.

Mixed-mode operating condition

To assess the robustness of the current mirror configurations, the output voltage is set to 3 V while the input current is kept constant at a value of 100 µA. The corresponding transistor operating conditions for each current mirror configuration is reported in figure 4.5. From this plot, one observes that the transistor T2 from the simple current mirror operates under high strong avalanche conditions, with an equivalent V_{CB} of 2.25 V. Moreover, the output transistor (T4) of the cascode, Wilson and balanced Wilson also exhibits a large V_{CB} of 1.5 V and a V_{CE} of 2.25 V, well beyond the conventional BV_{CEO}. This particular operating condition for the current mirror configurations leads to biases likely to induce mixed-mode degradation due to the activation of the impact-ionization mechanism for several transistors.

The evolution of the output current is displayed in figure 4.9a for the four current mirror configurations. For this particular operating condition, a negative shift of the output current is observed for each configurations with a maximum variation of 110 nA in the case of the the simple current mirror and of 35 nA for the three other current mirrors. These discrepancies does not result in a significant variation of the transfer current ratio as displayed in figure 4.9b.

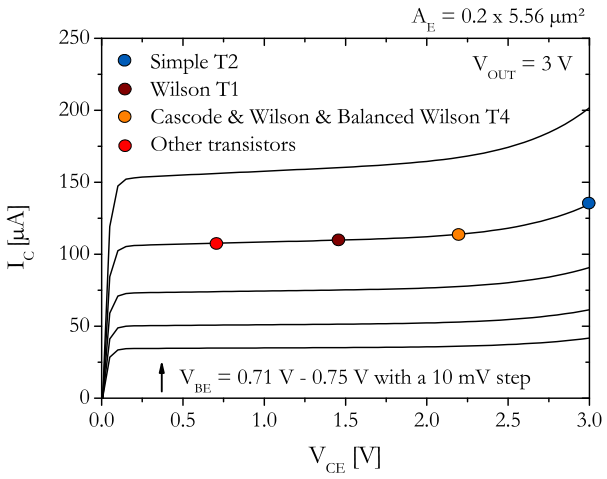


Figure 4.8: I_C vs V_{CE} output characteristics highlighting the transistors operating conditions for each current mirror configurations at V_{OUT} = 3 V and I_{IN} = 100 µA.

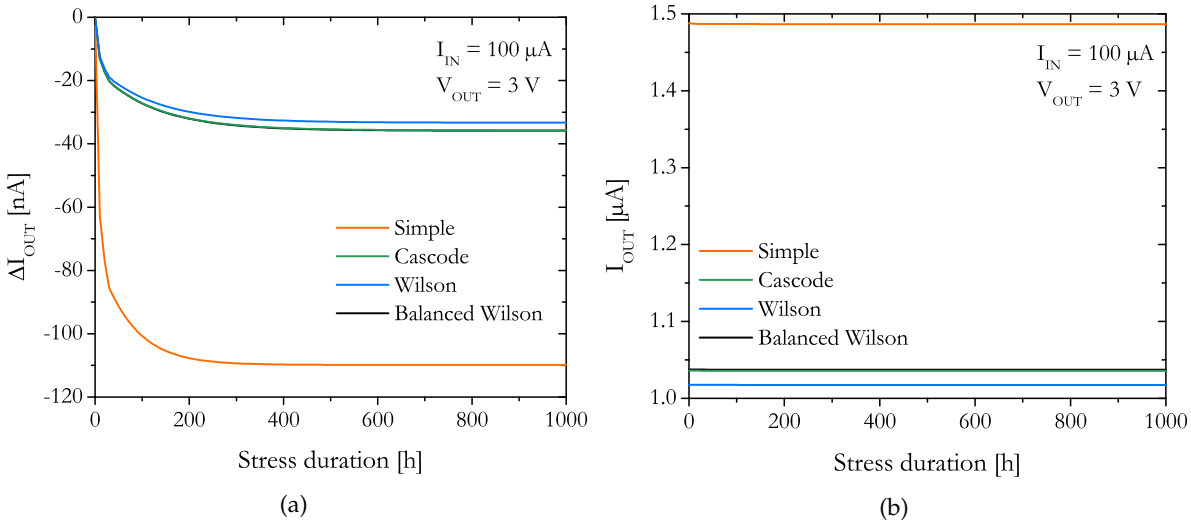


Figure 4.9: (a) Output current and (b) transfer ratio evolution according to the stress duration for I_{IN} = 100 µA and V_{OUT} = 3 V.

The deviation of the output current can be explained through the evolution of the sensitive aging compact model parameter, I_{REpS}, presented in figure 4.10 according to the stress duration for the same operating condition. One observes that only four transistors suffers from hot-carrier degradation : the transistor T_2 of the simple current mirror and the transistors T_4 of the three other configurations. This result is consistent with the bias conditions observed in figure 4.8. Due to their large V_{CB} values, all of those transistors operate under avalanche conditions implying a negative base current. In the case of the simple current mirror, the I_{REpS} parameter reaches a value of 30 fA which, thereby, increases the base current. However, even if the transistor is drastically impacted by the mixed-mode degradation, it does not influence the circuit electronic function since the transfer current ratio does not evolve over the stress duration (see figure 4.9b). For the three other configurations, cascode, Wilson and balanced Wilson, the increase of I_{REpS} parameter is limited to 10 fA for T4 transistors due to a reduced

V_{CB} value. Once more, the large degradation of the base current due to hot-carrier degradation does not impact the electronic function of the current mirror.

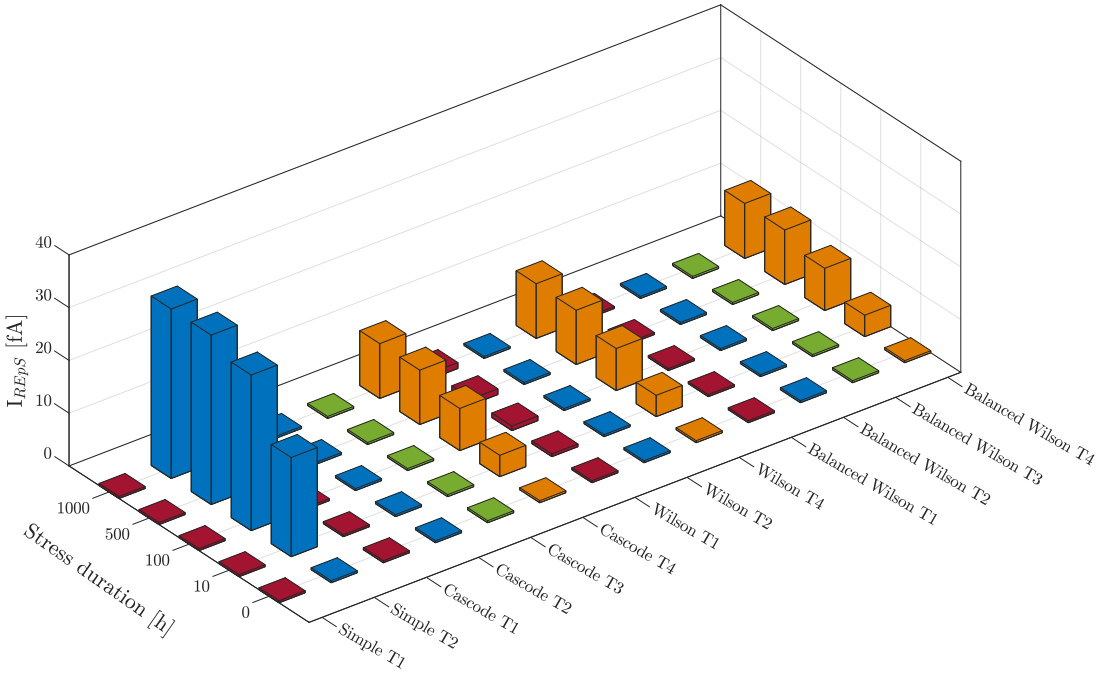


Figure 4.10: Evolution of I_{REpS} parameter according to the stress duration for the different transistors and current mirror configurations for I_{IN} = 100 µA and V_{OUT} = 3 V.

From these results, it can be concluded that the activation of hot-carrier degradation do have an impact at transistor level depending on their operating conditions but this degradation has a weak effect on the transfer current ratio of the current mirrors since its variation is less than 1%.

Injection levels

Figure 4.11 presents the evolution of the transfer current ratio according to the input current at V_{OUT} = 1.5 V for the simple current mirror, figure 4.11a and at V_{OUT} = 3 V for the three other configurations, figures 4.11b, 4.11c and 4.11d. Due to its architecture, a limited output voltage of 1.5 V for the simple current mirror is chosen to have an equivalent operating condition for each transistors. From these simulation results, one observes a maximum degradation of 0.001 for the transfer current ratio at relatively low injection levels (between 1 µA to 100 µA) while no variation is observed beyond those currents. This outcome is consistent with the results presented in [122] were a larger degradation of the transfer current ratio was exhibited for low current densities. Nevertheless, despite the increase of the recombination current, the degradation induced is minimal and does not affect the circuit electronic function. This is mainly due to the fact that current mirrors are usually designed to be independent of the transistors current gain (see table 4.1). From this table, one can calculate the variation of the transfer current ratio for a fixed variation of the transistor current gain. As an example, if we consider a 50%

variation of the T2 transistor current gain of the simple current mirror source, it leads to a 0.1% negative variation of the transfer current ratio.

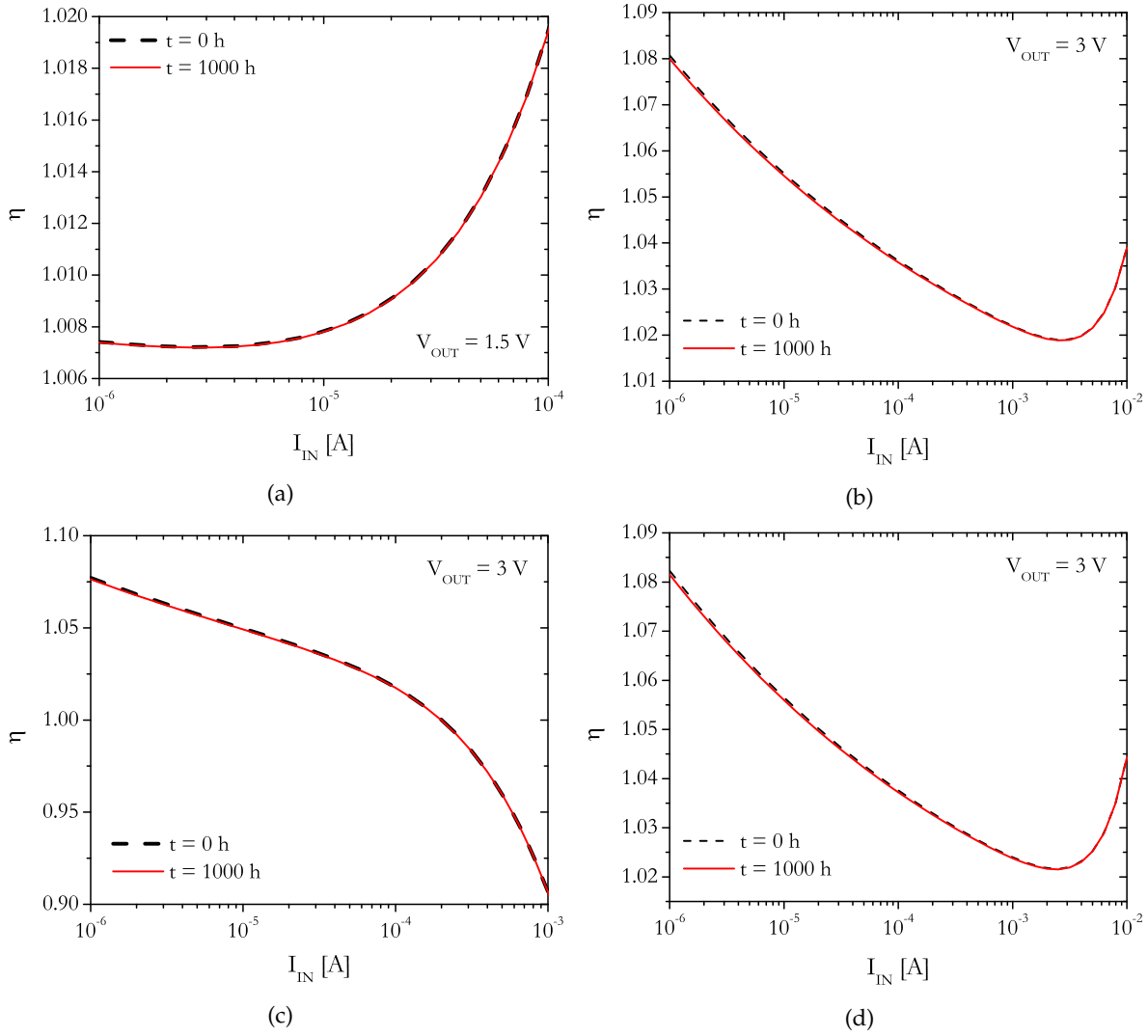


Figure 4.11: Transfer current ratio evolution according to the input current at t = 0 h and t = 1000 h for (a) the simple, (b) the cascode, (c) the Wilson and (d) the balanced Wilson current mirror.

In summary, the four current mirror configurations exhibit a very good robustness with a maximum variation of less than 1% for the transfer current ratio after 1000 h of stress duration regardless of the operating condition within the stable operation regime.

4.3 Ring oscillator

Due to its ease of integration, ring oscillators are widely implemented in phase-locked-loops (PLLs) to provide clock, data recovery or frequency synthesis in the RF field [142]. The most used architecture using bipolar transistors, is the current-mode-logic (CML) which exhibits many advantages such as high-speed symmetric operation, equal rise and fall times [143]. The CML stages connected in a ring oscillator architecture oscillates at a given frequency controlled

by a tail current. This tail current is commonly provided by a current mirror source. A shift of the biasing current could lead to a variation in the oscillation frequency. This effect has already been pointed out for MOS transistors based inverter gates [136], [144], [145] but need to be further investigated for SiGe HBT based architectures.

4.3.1 Circuit architecture

The investigated ring oscillator is a circuit composed of an odd number (N) of inverter stages where the output of each inverter is used as an input for the next one, as sketched in figure 4.12. Each stage is characterized by its delay time, τ_{CML}. Each stage corresponds to a CML inverter composed of two bipolar transistors (T_5 and T_6), two load resistances (R_L) and a current source, I_T.

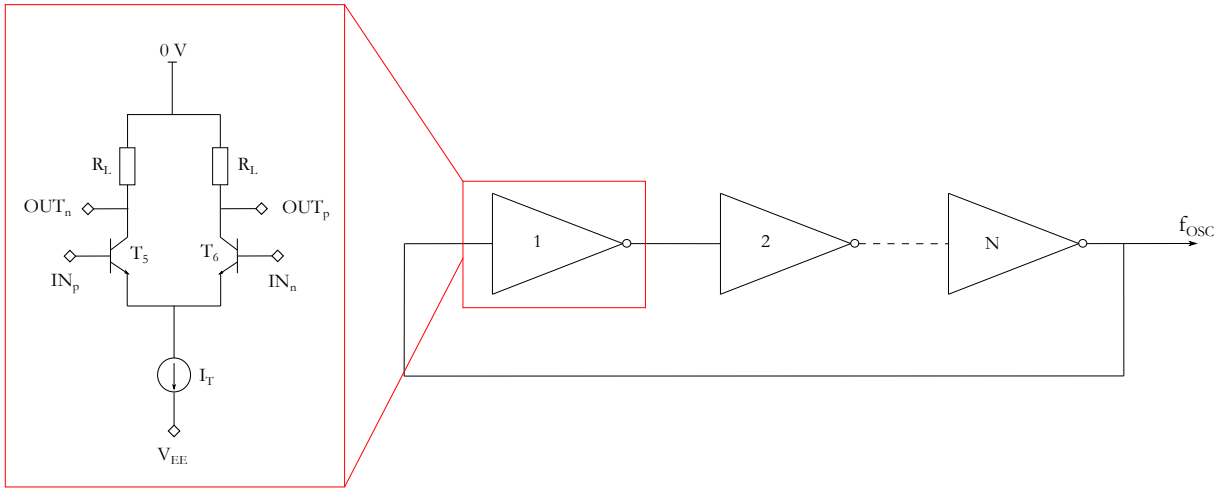


Figure 4.12: Schematic of the ring oscillator equivalent circuit together with the CML inverter architecture.

The delay time of one inverter cell is approximated by [146],

$$\tau_{CML} = \frac{\Delta V}{I_T} C_C + \frac{\Delta V}{2V_T + R_E I_T} \left[\frac{R_L + R_B}{2\pi f_T R_L} + R_B C_{jCi} \right] \tag{4.2}$$

where I_T is the tail current, C_C is the combination between the total base-collector capacitance (C_{BC}) and the total collector-substrate capacitance (C_{CS}), V_T is the thermal voltage, R_E is the emitter resistance, R_B is the base resistance, f_T is the transit frequency and C_{jCi} is the internal BC depletion capacitance. To provide a full oscillation period, the signal must go through each of the N inverters twice leading to the associated oscillation frequency of the ring oscillator,

$$f_{OSC} = \frac{1}{2N\tau_{CML}} \tag{4.3}$$

The output voltage swing, ΔV, is settled depending on the tail current, I_T, and the value of the load resistance, R_L, as depicted in equation (4.4). The output signal will, therefore, oscillate

between 0 V and -$R_L I_T$. In practical applications, this voltage swing must be large enough to accurately differentiate the zero from the one level on the eye diagram.

$$\Delta V = R_L I_T \tag{4.4}$$

Before evaluating the impact of hot-carrier degradation on the ring oscillator operation, a preliminary study of its operation is required.

4.3.2 Standard operation

In line with the previous section devoted to current mirrors, the ring oscillator is designed with a 0.2 x 5.56 µm² SiGe HBT from the 55 nm BiCMOS technology. Using an ideal current source for the tail current, one can plot the evolution of the gate delay value as a function of the tail current. The simulation results are depicted in figure 4.13a for a tail current ranging from 2 mA to 20 mA. The propagation delay for one gate reaches its minimum value of 1.8 ps for a tail current of 7 mA. This result is in accordance with the SiGe HBT transit frequency evolution as a function of the collector current displayed in figure 4.13b where the maximum frequency is obtained for the same collector current value, I_C.

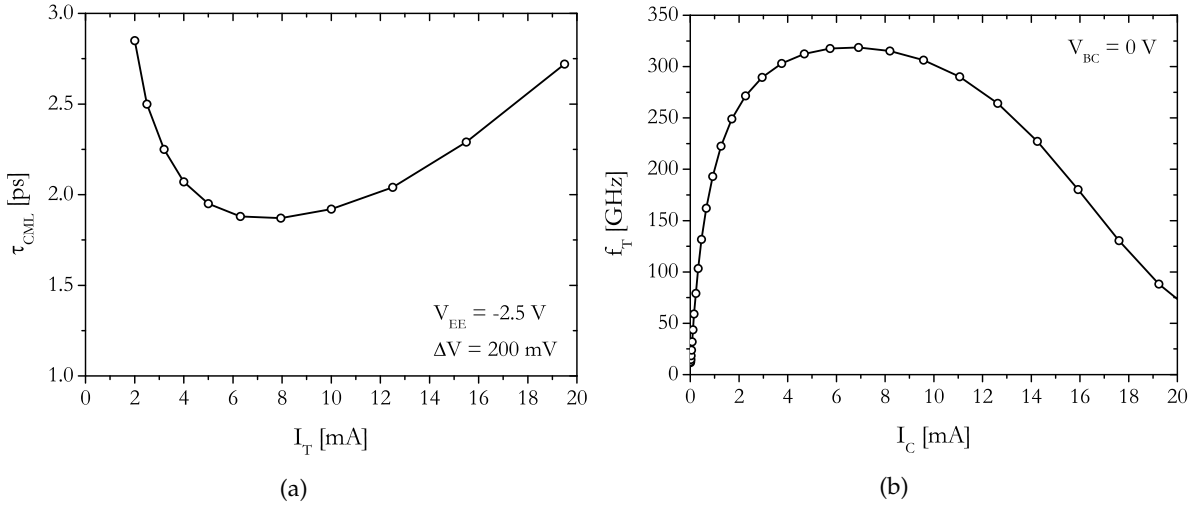


Figure 4.13: (a) Propagation gate delay τ_{CML} as a function of the tail current I_T using an ideal current source and (b) transit frequency f_T evolution according to the collector current I_C for a 0.2 x 5.56 µm² SiGe HBT device.

The differential output power spectrum is displayed in figure 4.14a for a tail current of 7 mA. In this plot, one observes a fundamental frequency at f_{OSC} = 13.3 GHz, which is in accordance with the result of equation 4.3. Moreover, the current plot allows to extract the odd order harmonic frequencies of the ring oscillator with, for example, f_3 = 39.3 GHz for the third harmonic or f_5 = 66.5 GHz for the fifth harmonic. The harmonics are detailed in figure 4.14b up to n = 15 (where n is the harmonic odd number).

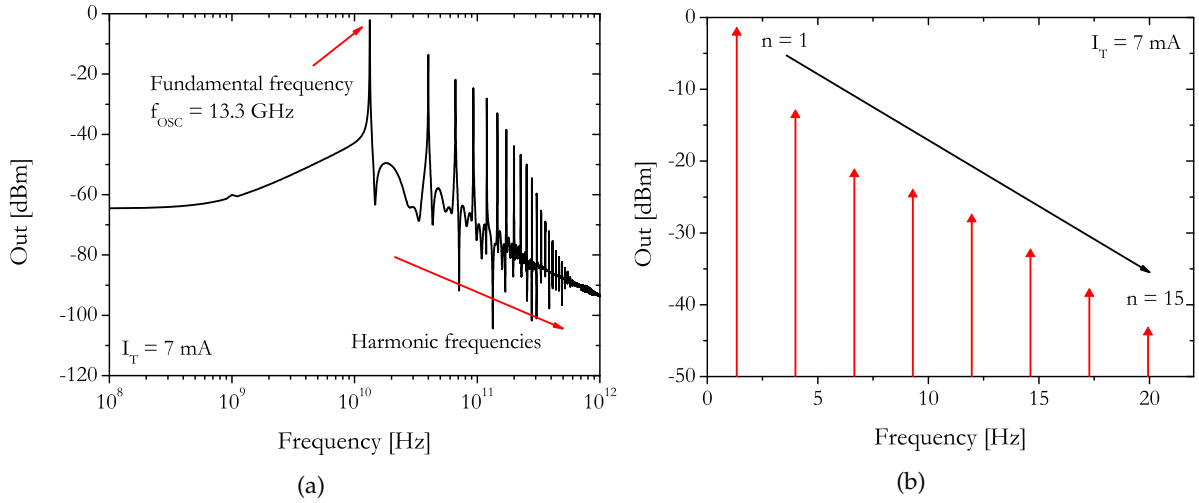


Figure 4.14: (a) Frequency power spectrum and (b) corresponding harmonic frequencies up to n = 15 of the ring oscillator for I_T = 7 mA.

Using transient simulations, the transient behavior of the ring oscillator is illustrated in figure 4.15 for both the input (black curve) and output (red curve) of the first inverter cell. As intended, an oscillation between 0 V and -200 mV is obtained with a 75 ps time period.

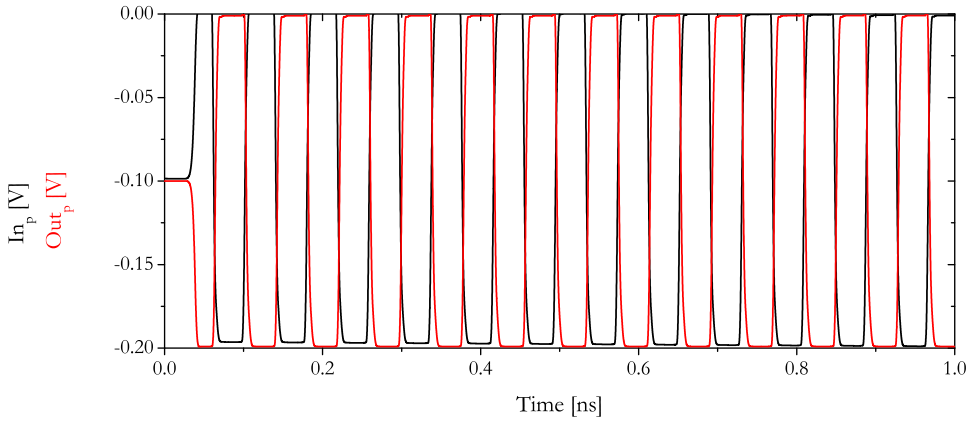


Figure 4.15: Transient evolution of the input and the output of one inverter stage.

The same result is reached by substituting the ideal current source by one of the current mirror architectures studied in the previous section. Due to its superior electrical performances (in terms of mirroring accuracy, output resistance and bandwidth) and its robustness against hot-carrier degradation, the balanced Wilson configuration is chosen to bias the inverter cells. The corresponding schematic is displayed in figure 4.16 where a bias resistance, R_{POL} is added to fix the input current. For a tail current of I_T = 7 mA and V_{EE} = -2.5 V, the bias resistance is fixed to R_{POL} = 105 Ω. Ideally, such a circuit achieves similar results to those obtained with the ideal current source, but may likely suffer from a degradation of its tail current, and accordingly, experienced a variation in its oscillation frequency.

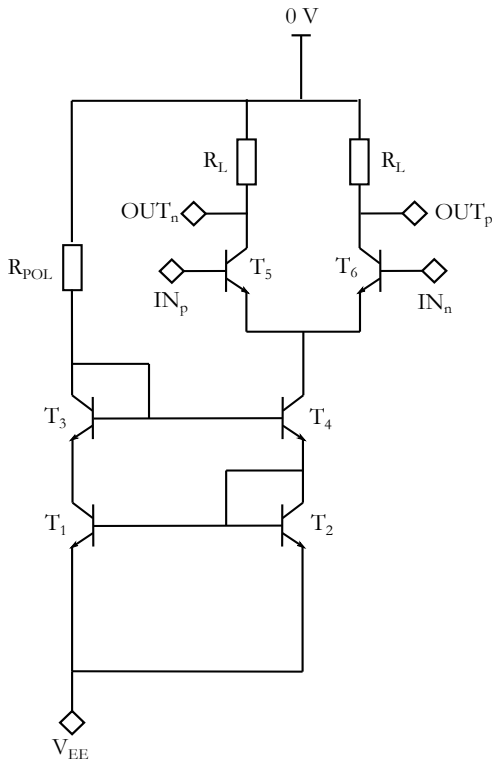


Figure 4.16: Schematic view of the CML architecture with a balanced Wilson current mirror to provide the tail current.

4.3.3 Reliability

The reliability analysis of the ring oscillator is performed for a maximum stress duration of 1000 h using a transient simulation time of 10 ns (ATSF = 3.6×10^{14}). The aging compact model, HiCuM-AL v3.0, is activated for each transistors by settling the aging flag model parameter to 1.

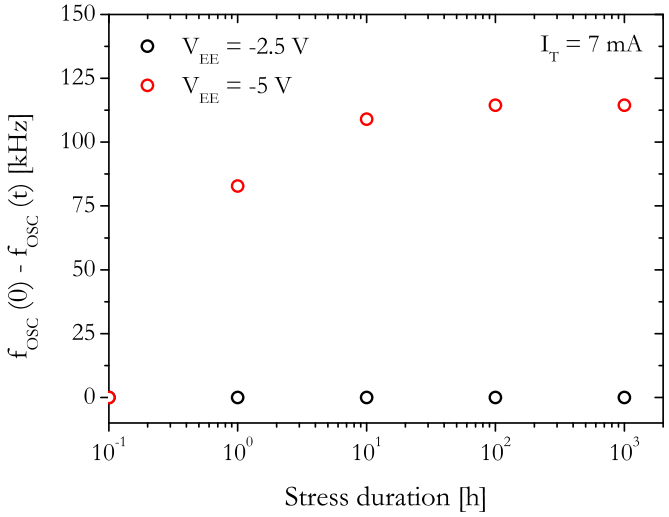


Figure 4.17: Oscillation frequency evolution according to the stress duration for V_{EE} = -2.5 V (in black symbols) and V_{EE} = -5 V (red symbols).

The tail current is fixed to I_T = 7 mA through the bias resistance, R_{POL}, of the current mirror source. The oscillation frequency evolution of the ring oscillator according to the stress duration is depicted in figure 4.17 for two supply voltages, V_{EE} = -2.5 V and V_{EE} = -5 V. While no variation of the oscillation frequency is observed for the lowest supply voltage, a 110 kHz reduction is demonstrated for V_{EE} = -5 V after 1000 h of stress. This result can be explained through the I_{REpS} parameter evolution along the stress duration of the transistor T_4 (the other transistors do not exhibit any variation of their I_{REpS} parameter). Due to a large V_{CB} value of 3 V at these terminals, the I_{REpS} parameter of T_4 transistor reaches a maximum value of 32.88 fA for V_{EE} = -5 V which induces a slight variation of the tail current, and, therefore, of the oscillation frequency. However, the observed reduction is not significant and must be compared to the circuit oscillation frequency of 13 GHz.

In brief, the simulation results are consistent with the analysis performed in section 4.2. Indeed, since the oscillation frequency is governed by the tail current, only a variation of this parameter will lead to an increase or a reduction of the oscillation frequency. However, it was shown in the previous section that the effect of hot-carrier degradation on the output current of current mirrors was negligible, more especially under high injection levels (as it is the case for ring oscillator). Consequently, even if the transistor T4 exhibits a variation of its I_{REpS} parameter, it does not lead to a reduction of the tail current, and thereby, of the oscillation frequency. Another way to induce a variation of the tail current is trough the inverter differential pair (T5 and T6 devices). However, these two transistors have an equivalent V_{CB} value oscillating between 0.2 V and -0.2 V which isn't large enough to cause a degradation of the base current.

4.4 A test vehicle: a broadband amplifier

So far, the simulation results obtained on current mirrors and ring oscillators have not be verified through actual measurement results. Therefore, to fully validate the developed aging compact model, HiCuM-AL v2.0, a test vehicle is required. The circuit is submitted to an aging test under dynamic stress with a monitoring of several electrical characteristics. In this thesis work, two test vehicles were provided by IHP Microelectronics. The first one is a voltage controlled oscillator (VCO) composed of a LC tank [147]. Both the phase noise and the oscillation frequency were monitored along the stress duration. No noticeable variation of these parameters were observed after 72 hours of aging test. The second test vehicle is an independent driver amplifier (class A) intended to be used in hybrid configuration with segmented Mach-Zehnder modulators (SEMZM) [148]. For this circuit, the monitoring along the stress duration did result in a relatively small deviation of the output supply current. The detailed analysis of the circuit variation is proposed in this following section.

4.4.1 Architecture

The broadband amplifier [148] of figure 4.18 is composed of 11 high-speed SiGe HBT from IHP SG13S technology. The circuit is a 4-port system featuring differential input (InP and InN) and

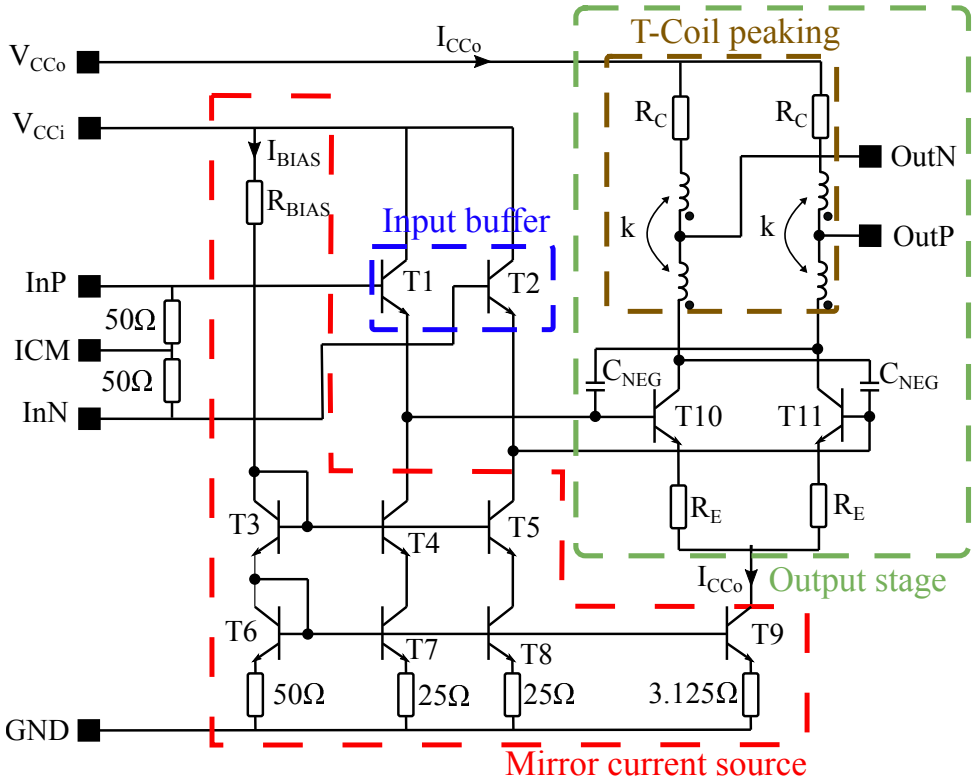


Figure 4.18: Driver amplifier schematic.

output (OutP and OutN) designed to be compatible with GSSG probes configuration. It also requires three DC supply voltages, one for the common mode, ICM, one for the input stage, V_{CCi}, and one for the output stage, V_{CCo}. In the output stage, inductive peaking implemented with T-Coil structures are used to increase the amplifier bandwidth [149]. All transistor dimensions are summarized in table 4.3 featuring multiple emitter fingers N_X with a constant emitter width W_E of 0.16 µm and a constant emitter length L_E of 0.88 µm. The factor m represents the number of transistors in parallel.

Transistors	T1 - T2	T3 - T6	T4 - T5 - T7 - T8	T9	T10 - T11
N_X	4	2	2	2	8
m	1	1	2	16	2

Table 4.3: Circuit transistor dimensions.

IHP has designed multiple versions of the driver varying from D1 to D8 configurations. Drivers (D1-D4) have been designed for a 8-segment SEMZM while (D5-D8) have been optimized for a 16-segment SEMZM. Since initially (before aging) the drivers (D1-D4) didn't behave as expected, only drivers (D5-D8) were investigated during this thesis work. The four configuration differs in the T-Coils structure and D6 configuration is the only one implementing a negative capacitance compensation, C_{NEG} [149]. The top layout of the driver chips is presented in figure 4.19.

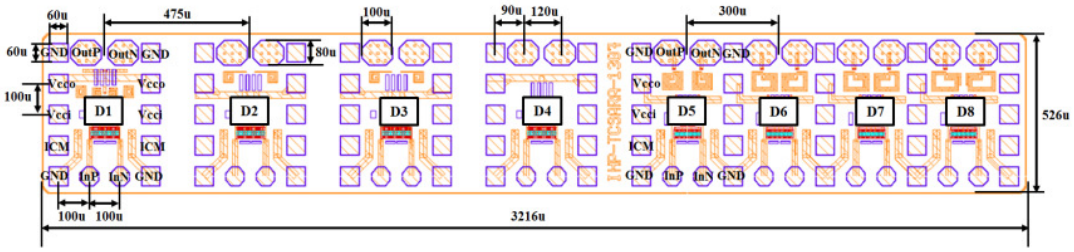


Figure 4.19: Top layout of the driver array [149].

The recommended test setup bias values for the ICs are detailed in table 4.4. The typical values for the supply voltages are used for the initial characterization.

Supply	Minimum	Typical	Maximum
V_{CCo}	-	3.7 V (32mA)	4 V
V_{CCi}	3 V	3.3 V (10mA)	3.6 V
ICM	-	3 V	-

Table 4.4: Recommended supplies for characterization.

4.4.2 Operation conditions

Initial characterization

The initial characterization is performed using a Network Analyzer E8361A in the 10MHz-67GHz frequency range and the extension N4421B to perform 4-port S-parameters measurement. SOLT calibration is achieved between 1 GHz and 40 GHz with an input power, P_{RF} of -15 dBm. The circuit supply voltages are provided by the Semiconductor Parameter Analyzer E5270. As ground pads are not available for DC supplies, an external connection is required from the external DC ground to the external RF ground of the Network Analyzer. The complete measurement bench schematic is displayed in figure 4.20.

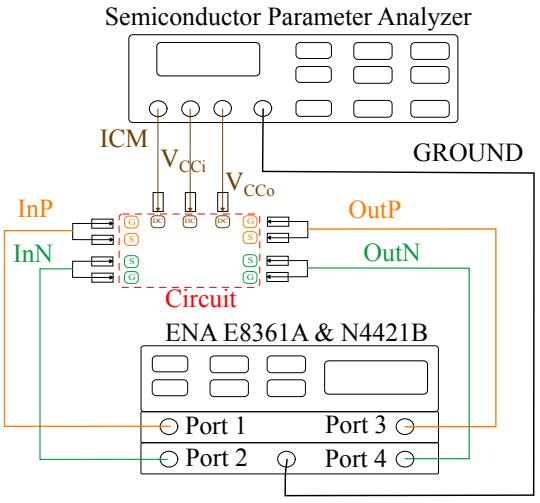


Figure 4.20: 4-port S-parameters measurement bench

Since the circuit is a 4-port system, additional calculations are required to extract the input differential reflection S_{dd11}, the forward differential transmission gain S_{dd21} and the output differential reflection S_{dd22} as summarized in the system of equations (4.5). According to figure 4.20, the first port is considered as the positive differential input (InP), the second port as the negative differential input (InN), the third port as the positive differential (OutP) output and the fourth port as the negative differential output (OutN).

$$\begin{aligned} S_{dd11} &= \frac{S_{11} - S_{12} - S_{21} + S_{22}}{2} \\ S_{dd21} &= \frac{S_{31} - S_{32} - S_{41} + S_{42}}{2} \\ S_{dd22} &= \frac{S_{33} - S_{34} - S_{43} + S_{44}}{2} \end{aligned} \tag{4.5}$$

For the initial characterization, drivers (D5-D8) were measured on five different chips to characterize the circuit variability. A comparison of the differential gain for the four configurations is displayed in figure 4.21a. The maximum gain is obtained for D8 configuration with 9.5 dB at a frequency of 25 GHz. The largest bandwidth is achieved by D5 configuration but with a relatively low transmission gain (6.5 dB at f = 28GHz). The performances of D7 circuit configuration is close to the D6 ones with a differential gain of 8.8 dB for a bandwidth of 20 GHz. For further analysis, the study will focuses on the reliability of D6 configuration as this configuration exhibits a restrained chip-to-chip technological variability compared to the other drivers. The differential coefficients, S_{dd11} and S_{dd22}, for D6 driver configuration are depicted in figure 4.21b. These two parameters exhibit values lower than -5 dB over the entire frequency range.

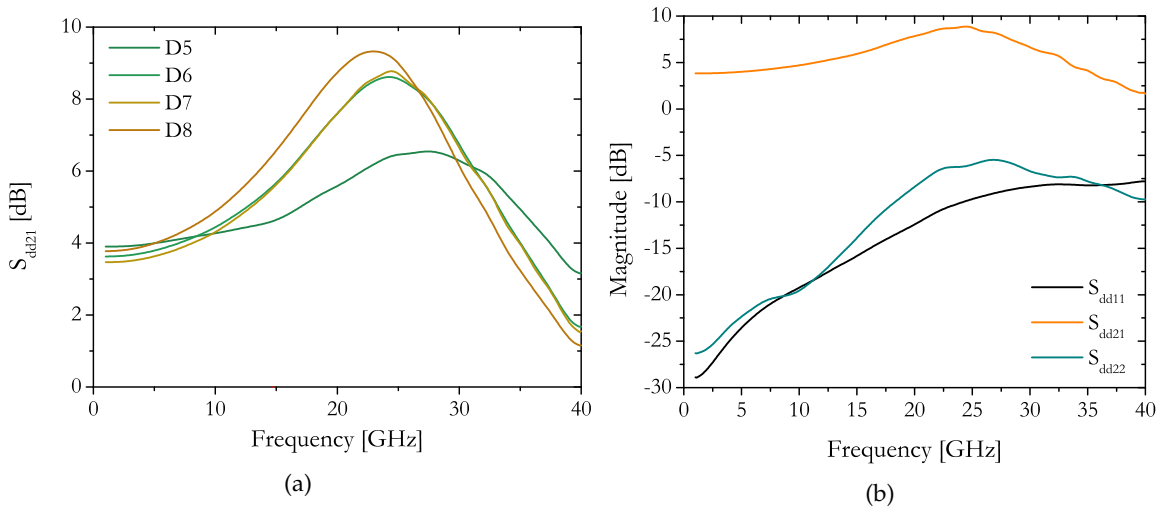


Figure 4.21: (a) Differential gain S_{dd21} for the different driver configurations (D5-D8) and (b) Differential parameters measurement results for D6 circuit configuration.

Circuit modeling

Before assessing the reliability of the circuit, it is necessary to verify that the HiCuM compact model simulation accurately reproduces the circuit operation. The differential gain can be calculated as,

$$S_{dd21}(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = -\frac{g_m R_C A(j\omega)}{(1 + g_m R_E)} \tag{4.6}$$

where g_m corresponds to the transcondutance of the output transistors (T10-T11) and A(jω) is the gain of the T-Coils structures. Due to its dependency to the output inductive peaking, an additional modeling of the T-Coils structures is required. Based on the work from [150], the equivalent schematic for the inductive peaking presented in figure 4.22a has been choosen. It is composed of a mutual inductance (L_1 and L_2) with a coupling factor, k, and a bridge capacitance, C_B. Moreover, the output pads were designed to allow for multiple wire bonds which implies a non-negligible parasitic capacitance, C_{PAD}. A comparison between the measurement and the simulation (using the associated HiCuM scalable model card) of S_{dd21} is displayed in figure 4.22b. An excellent accuracy is achieved for frequencies ranging from 1 GHz to 40 GHz, thus, validating the current modeling for the bridge T-Coils.

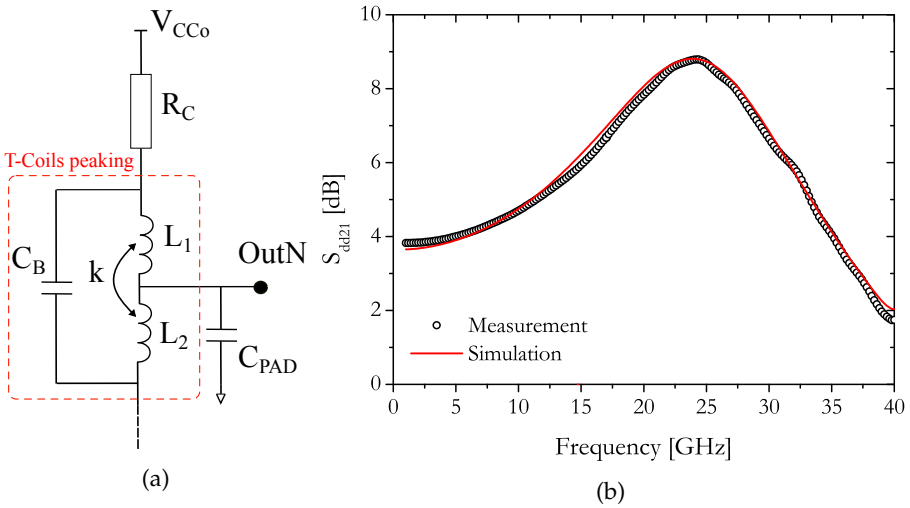


Figure 4.22: (a) T-Coils structures modeling which includes a mutual inductance with a coupling factor k, an output pad capacitance, C_{pad}, and a bridge capacitance, C_B, and (b) Comparison between measurements (symbols) and simulation (red solid line) for S_{dd21} parameter of D6 circuit configuration using HiCuM compact model.

4.4.3 Reliability

The reliability of the driver is evaluated on the D6 circuit configuration since it exhibits a limited chip-to-chip variation of the differential gain. Originally, the aging simulations were performed using the HiCuM-AL v2.0 aging compact model as detailed in [140]. However, the implementation of scaling rules within the HiCuM compact model is relevant for this particular test vehicle since the transistors feature different emitter dimensions. Consequently, the

simulation results presented below are performed using the aging compact model, HiCuM-AL v3.0, which integrates the scaling rules for hot-carrier degradation. Note that, the simulation results between the two versions only differ for the I_{REpS} parameter evolution while the analysis outcome is similar.

Aging test

A dynamic aging stress test is performed on the test vehicle by applying an input RF power of P_{RF} = -15 dBm at standard DC operating conditions, *i.e.* ICM = 3 V, V_{CCi} = 3.3 V, V_{CCo} = 3.7 V and T_{AMB} = 25°C. The corresponding operating conditions of the 11 transistors are summarized in figure 4.23. Note that, all transistors, excepted T10 and T11, are biased below the BV_{CEO} value, meaning that hot-carrier degradation, if any, will not be activated by a large electric-field for these transistors. Therefore, the degradation mechanism can only be likely activated through the current density which mean value equals to 7 mA/µm² for all transistors. In such bias conditions, both the self-heating and the weak avalanche effect may occur. Note that, the large RF power applied to the circuit leads to a voltage excursion beyond BV_{CEO} for the output transistors T10 - T11. Therefore, a larger degradation of these two transistors is expected during aging compact model simulations.

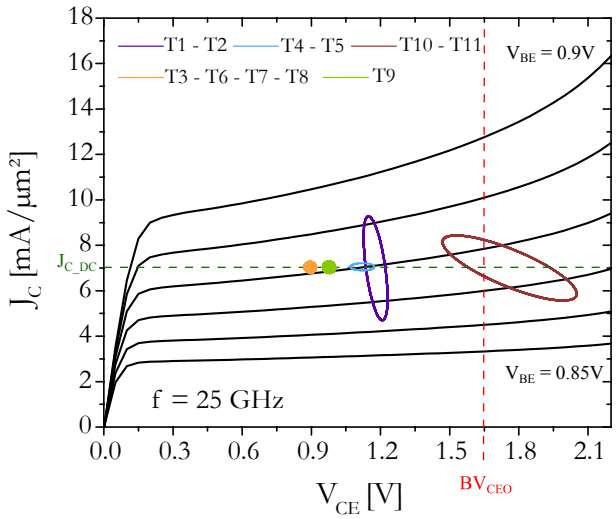


Figure 4.23: J_C vs V_{CE} output characteristics highlighting the transistors operating conditions.

During the stress measurement campaign, as presented in figure 4.24a, the differential gain evolution, S_{dd21}, exhibits a slight reduction of 0.06 dB after 50 hours of RF stress for the overall frequency range. This variation has been associated to the equipment calibration shift over the time. Thus, the circuit output figure of merit is not altered by the hot-carrier degradation. However, a degradation of the output supply current I_{CCo} is measured as shown in figure 4.24b in symbols. This variation is characterized by a 100 µA maximum reduction after 50 hours of RF stress. A deeper analysis, detailed hereafter, of the circuit operation behavior is required to point out the origin of this degradation.

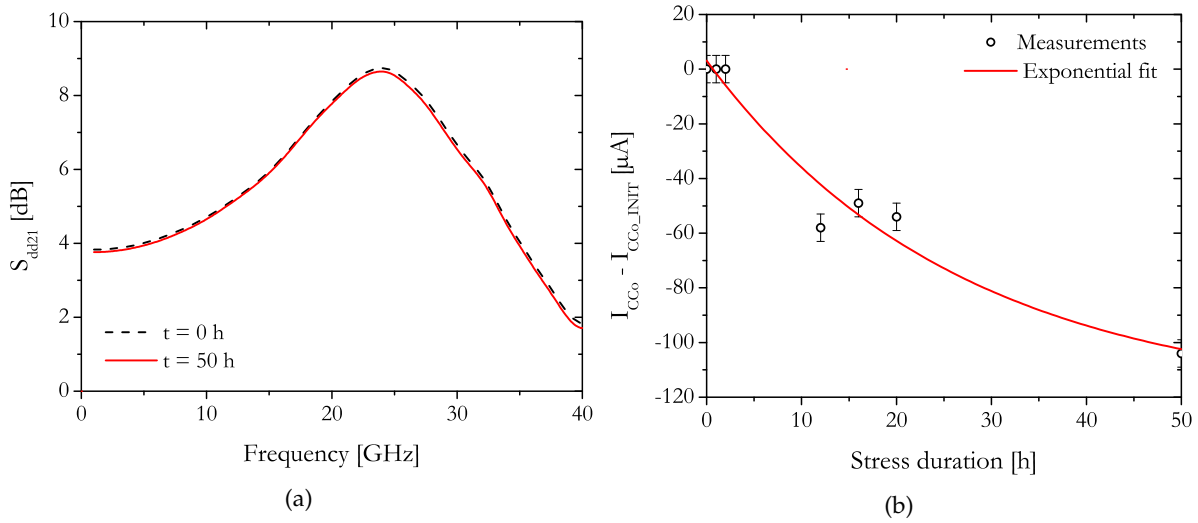


Figure 4.24: Evolution of (a) the differential gain, S_{dd21}, at t = 0 h and t = 50 h and (b) the output supply current, I_{CCo}, according to the stress duration under RF stress.

Analysis

The aging compact model sensitive parameter, I_{REpS} evolution over the stress time duration for the 11 transistors is displayed in figure 4.25 and can be explained through their respective bias conditions analysis presented in figure 4.23.

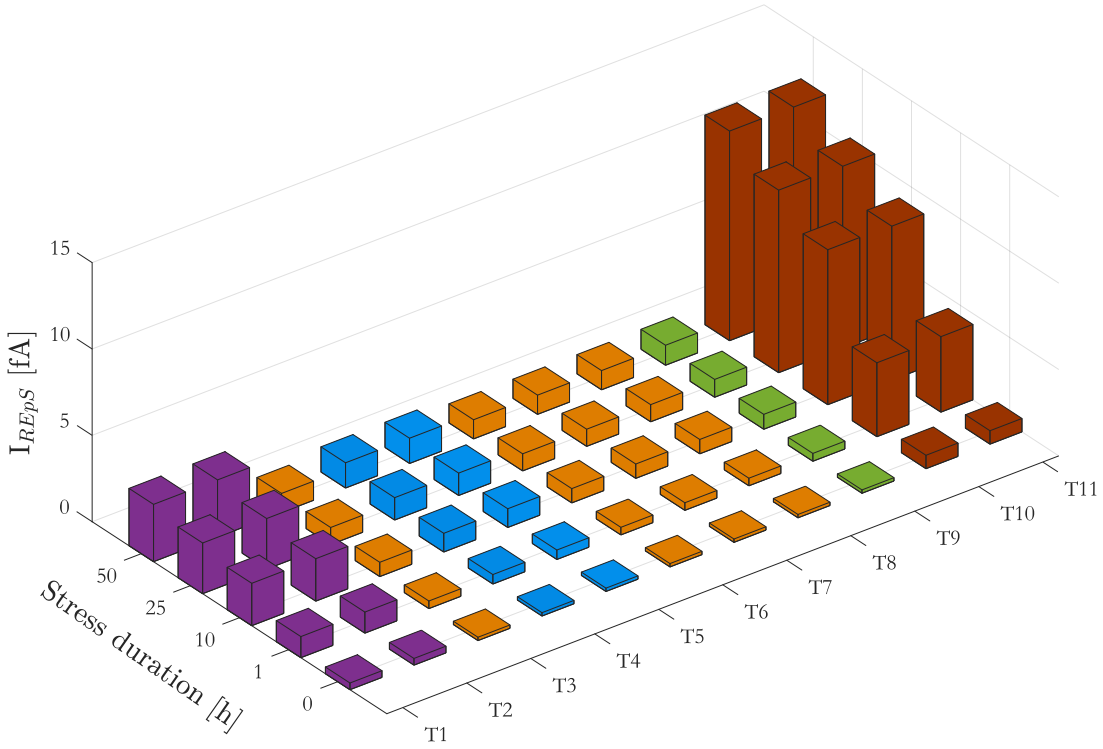


Figure 4.25: I_{REpS} parameter evolution according to the stress duration for the 11 transistors simulated with the aging compact model.

Since the current density is equivalent for each transistors ($J_{C_{dc}}$), the maximum I_{REpS} variation is due to their respective different V_{CB} values:

- for very low V_{CB} close to 0 V (*e.g.* for T3, T6, T7, T8 and T9), the maximum I_{REpS} variation is around 1.2 fA.
- for a V_{CB} of 0.25 V for transistors T4 and T5, the maximum I_{REpS} variation is equal to 1.5 fA.
- for a V_{CB} of 0.3 V for the input stage (*i.e.* T1 and T2), the maximum I_{REpS} variation is around 3.3 fA.
- for a large V_{CB} of 0.88 V for the output stage (*i.e.* T10 and T11), the maximum I_{REpS} variation is equal to 12 fA which demonstrates a specific sensitivity to hot-carrier degradation.

Figure 4.26 presents the output supply current I_{CCo} variation over the stress duration for several simulation conditions that will be further explained below. For the black curve, the aging flag was turn on for all circuit transistors leading to 80 µA reduction of the output supply current compared to its initial value. This variation is close to the one measured during the aging test (see symbols). The similar trend between the measurements and the simulation allows to validate the accuracy of the aging compact model.

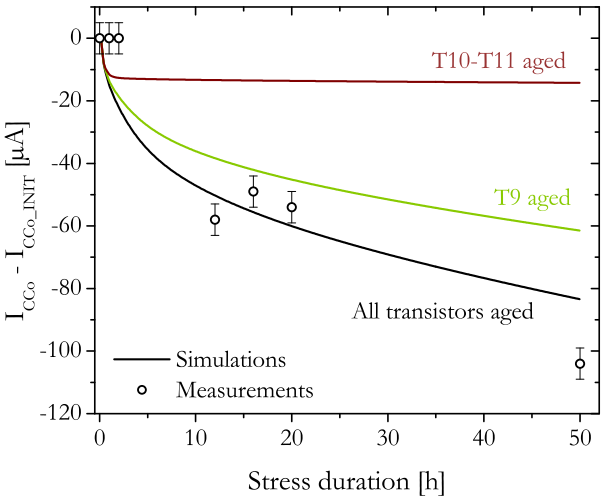


Figure 4.26: Evolution of the output supply current in measurements (symbols) and under several simulation conditions using HiCuM-AL v3.0 compact model (solid lines): with only T10- T11 transistors aging virtually activated (in brown), only T9 transistor virtually activated (in green) and all transistors aging virtually activated (in black).

In addition, through the aging flag model parameter, the aging compact model allows to precisely locate the most sensitive regions to hot-carrier degradation within the circuit. To do so, since the output transistors have demonstrated a larger increase of the recombination current, the aging flag parameter is only activated for these two devices. The simulation results are depicted on the brown curve of figure 4.26 where a variation of only 10 µA is observed along the stress duration. Therefore, it is not these two transistors that are responsible for the degradation observed on the output supply current.

This current is driven by a cascode current mirror with multiple outputs : two outputs to bias the input differential stage and one for the output stage. The simulation results from section 4.2 have already identified that the output transistor of the current mirror is the most sensitive to hot-carrier degradation. Accordingly, the aging flag parameter is only turned on for T9 transistor while it is disabled for other transistors. The corresponding simulation result is depicted on the green curve of figure 4.26 where a 60 µA maximum reduction is observed for the output supply current close to the simulation result with all transistors aged. This result indicates that the main contribution for the variation of I_{CC_0} comes from the impact of hot-carrier degradation on T9 transistor which leads to a reduction of its current gain [140].

In summary, the amplifier submitted to a dynamic stress for 50 hours have demonstrated a slight reduction of the output supply current. Thanks to the HiCuM-AL v3.0 aging compact model, an accurate prediction of the output supply current degradation is achieved. Moreover, the compact model allows to clearly identified the circuit weakest points, thus, giving the designers an opportunity to improve the circuit robustness and performances.

4.5 Conclusion

The fourth chapter was focused on the effect of hot-carrier degradation on different integrated circuits based on SiGe HBTs. Indeed, this degradation mechanism has exhibited a variation of the transistor electrical performances with an increase of the base recombination current, and consequently, a reduction of the transistor current gain.

The first integrated circuit to be analyzed is the current mirror with four architectures : the simple, the cascode, the Wilson and the balanced Wilson. A quick presentation of the architectures and the figures of merit of each configuration was reported. Then, a comparison of the electrical performances of each configuration was performed based on simulation results under static and dynamic operating conditions. This preliminary study has exhibited the increased performances in terms of mirroring accuracy, output resistance and bandwidth of both the cascode and the balanced Wilson current mirrors. Using the HiCuM-AL v3.0 aging compact model, the impact of the hot-carrier degradation on the circuit electronic function was evaluated. From these results, it has been concluded that the activation of hot-carrier degradation do have an impact at transistor level depending on their operating conditions but this degradation has a weak effect on the transfer current ratio of the current mirrors since a variation of less than 1% is observed after 1000 h of aging.

In addition, the reliability of a ring oscillator featuring 21 CML inverter cells was investigated. Designed with the 55 nm technology from ST Microelectronics, the circuit was biased using a current mirror source, more especially, the balanced Wilson architecture. Under standard bias conditions, the ring oscillator exhibits a minimum gate delay of 1.8 ps for a tail current of 8 mA and an output voltage swing of 200 mV. To evaluate the impact of hot-carrier degradation on this circuit, the aging flag model parameter was set to 1 for all transistors during an aging stress duration of 1000 h. The transient behavior of the output voltage of the aged circuit was

compared to the initial one. No variation of the tail current or the oscillation frequency was observed, which is consistent with the reported simulation results of the current mirror source.

Finally, the accuracy of the HiCuM-AL v3.0 aging compact model was validated on a circuit test vehicle from IHP Microelectronics. The circuit is a driver composed of 11 transistors featuring different number of emitter fingers and transistors in parallel. An initial characterization was performed on five different chips each of them featuring four different driver configurations. From these measurements results, the chosen test vehicle is the D6 configuration which exhibits a differential gain of 8.8 dB and a corresponding bandwidth of 20 GHz. On this particular circuit, a dynamic aging stress was performed using a large RF input power of - 15 dBm. A reduction of the output supply current of 100 µA was observed after 50 h of aging test while the variation of the differential gain was associated to a calibration shift of the measurement bench. Based on the HiCuM-AL v3.0 aging compact model, the small variation of the output supply current was attributed to the degradation of the output current mirror source. A good agreement between the aging compact model simulation and the aging test measurements results was obtained.

To conclude this chapter, the developed aging compact model has demonstrated its accuracy for the reliability evaluation of several integrated circuits. Even if an impact of hot-carrier degradation is observed at transistor level, it didn't reveal a significant effect at circuit level with a very limited variation of the associated electronic function.

General Conclusion

This work debates on the impact of hot-carrier degradation on the electronic function of integrated RF circuits. This manuscript aims to propose an aging compact model allowing to assess the robustness of SiGe HBT devices and circuits under mixed-mode stress.

In recent studies, the SiGe HBT technology has been pointed out to be strongly impacted by the hot-carrier degradation with an increase of the recombination base current at low injection levels. Consequently, it has been widely reported a significant reduction of the transistor current gain, which, thereby, can cause reliability issues.

To prevent the impact of this particular degradation mechanism on SiGe HBT devices, preliminary studies have been conducted on the impact-ionization mechanism and the self-heating effect, two physical effects that trigger the hot-carrier degradation. Regarding the impact-ionization mechanism, a characterization under static operating conditions has been carried out on a SG13S technology from IHP Microelectronics. The avalanche multiplication coefficient formulation implemented in the last version of the HiCuM compact model has been tested on this particular technology. The model includes the strong avalanche behavior as well as the high-current effects. Based on a fully scalable extraction procedure, the formulation has demonstrated an excellent accuracy up to the second breakdown voltage, BV_{CBO}, and for high current densities (beyond the Kirk effect onset). Furthermore, concerning the self-heating effect, a physics-based scalable electrothermal model has been formulated based on the transistor architecture. While the back-end-of-line heat diffusion has been modeled using a single resistance, the front-end-of-line heat diffusion has been designed using a three poles resistance-capacitance network. Each cells was scaled according to the thermal conductivity evolution along the transistor thickness. From this formulation, it has been demonstrated that the heat spreading is limited by the poor thermal conductivity of the heavily-doped-collector, thus increasing the overall device thermal resistance. The developed electrothermal model has been implemented in the HiCuM compact model thermal node instead of the single pole thermal network generally used in commercial compact models. The physics-based thermal model has exhibited an improved precision compared to the single pole network under small-signal and transient operating conditions.

Due to the transistor operation close to the safe-operating-area edges, the transistor electrical behavior is dominated by the impact-ionization mechanism and the self-heating effect. This operation close to, and even beyond, the conventional safe-operating-area can lead to the activation of the hot-carrier degradation.

To accurately model the consequences of this particular degradation mechanism, a precise explanation of the physical mechanism has been reported. During the avalanche mechanism, the hot-carriers created within the base-collector space charge region can gain sufficient energy to initiate Si-H bonds breakage close the the emitter-base spacer oxide interface. Consequently an increase of the recombination base current has been observed on SiGe HBT based devices. More specifically, based on HiCuM compact model and TCAD simulation results, the creation of traps density at the Si/O_2 interface has been correlated to the increase of a particular compact model parameter, the peripheral recombination saturation base current, I_{REpS}. From this outcome, a physic-based scalable aging compact model, HiCuM-AL v3.0, has been derived from the reaction-diffusion theory. Compared to the state-of-the-art, this model has included several aspects of the hot-carrier degradation: the generation of traps due to hot-holes, the annihilation of traps under thermal constraints and the diffusion of hydrogen atoms within the transistor. This last feature is an original concept enabling the position of hydrogen atoms to be determined over the stress duration ensuring the time-invariance of the formulation. The hydrogen diffusion has been modeled using a resistance-capacitance recursive network which can be scaled according to the SiGe HBT geometry features. An accurate extraction procedure of the aging compact model parameters has been developed and tested on two different SiGe HBT technologies featuring different emitter-base spacer architecture and emitter dimensions. An excellent accuracy was obtained under static and dynamic operating conditions for both technologies, thus demonstrating its efficiency and versatility. One interesting outcome resulting from these measurement and simulation results is the reversibility of the degradation mechanism with an observed recovery of the base current under elevated junction temperature operating conditions which is well-captured by the aging compact model.

Owing to its physical basis, the HiCuM-AL v3.0 compact model can be used to asses the reliability of integrated circuits against hot-carrier degradation under standard and/or mixed-mode operating conditions.

Several integrated circuits have been studied during this thesis work: various current mirrors, a CML ring oscillator and a broadband amplifier. For the first two circuits, designed using the 55 nm technology from ST Microelectronics, the reliability was only evaluated using simulation results. The output transistors of the four current mirror topologies (the simple, the cascode, the Wilson and the balanced Wilson) has revealed a special sensitivity to hot-carrier degradation with an increase of their corresponding I_{REpS} parameter. However, the degradation at transistor level, after 1000 h stress, didn't result in a significant variation of the transfer current ratio with less than 1% of maximum deviation under mixed-mode operating conditions. Based on these simulation results, an analysis of the ring oscillator robustness against hot-carrier degradation has been performed. The circuit has been designed using 21 CML based inverter cells with a corresponding tail current provided by a balanced Wilson current mirror. After 1000 h of stress duration, no particular evolution of the oscillation frequency was noticed. This outcome was consistent with the survey proposed on current mirrors which result in the non-variation of the circuit tail current. The simulation results obtained on the current mirrors topologies and

the ring oscillator were not correlated to measurement results allowing to validate the aging compact model accuracy at circuit level. Accordingly, a test vehicle, a driver amplifier, has been provided by IHP Microelectronics featuring 11 transistors with various emitter dimensions. The circuit was submitted to a dynamic aging stress during 50 h with a corresponding input RF power of -15 dBm at 25°C. While the overall circuit figure-of-merit, *i.e.* the differential gain, didn't exhibit a significant variation over the stress duration, a 100 µA reduction of the output supply current was monitored. Using the HiCuM-AL v3.0 aging compact model, this variation has been mainly attributed to the degradation of the output transistor of the current mirror stage. However, in agreement with the previous results, this reduction represents less than 1% of the initial output supply current equal to 32 mA which isn't large enough to induce a circuit failure.

To pursue this study, a few suggestions for further development can be made. First, to meet the circuit operation under elevated frequencies, some prospects on ultra-fast switching aging stress must be carried out. This measurement type, already performed in MOS transistors, could be performed using pulse measurement units. Due to the time-dependence of the hot-carrier degradation, the fast switching between several states could lead to particular degradation behavior. Moreover, the model developed in this manuscript must be confronted to other SiGe HBT technologies but can also be easily adapted to III-V based HBT devices. It is important to note that this manuscript did not address the low-frequency noise aspects. The accuracy of the aging compact model should be, therefore, also validated to the variation of this particular figure-of-merit. Last, but not the least, future research should focus on the adequacy between the aging compact model simulation results and the aging measurements at circuit level. Different test vehicles with different constraints in voltage, current and temperature can be investigated to verify the validity of the aging compact model. These circuits can be designed beyond the usual operating limits (*i.e.* outside the conventional safe-operating-area), but within the limits defined by the stable-operation-regime. In that particular case, resulting in a potential activation of the hot-carrier degradation, the real impact on the circuit electronic fonction could be assessed under mixed-mode operating conditions.

Author Publication List

International journals

1. **M. Couret**, M. Jaoul, F. Marc, C. Mukherjee, D. Céli, T. Zimmer and C. Maneux, *Scalable compact modeling of trap generation near the EB spacer oxide interface in SiGe HBTs*, Solid-State Electronics, Volume 169, 2020
2. C. Mukherjee, G. G. Fischer, F. Marc, **M. Couret**, T. Zimmer and C. Maneux, *A Unified Aging Compact Model for Hot Carrier Degradation under Mixed-mode and Reverse E-B stress in Complementary SiGe HBTs*, Solid-State Electronics, 2020
3. C. Mukherjee, F. Marc, **M. Couret**, G. G. Fischer, M. Jaoul, D. Céli, K. Aufinger, T. Zimmer and C. Maneux, *A physical and versatile aging compact model for hot-carrier degradation in SiGe HBTs under dynamic operating conditions*, Solid-State Electronics, Volume 163, 2020
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