Time-to-Digital Conversion based on a Self-Timed Ring Oscillator

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To my family ...

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Chapitre 1

Introduction

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1.1 Context and Motivations

Continuous progress in electronic devices and technology enables us to makes our life comfortable and convenient. This progress is due mainly to CMOS scaling, which allows deploying more and more integrated functionalities into the same chip. One simple example is the use of sensors, which are pervasive and useful in several fields. They are embedded in cars, airplanes, cellular phones, radios and countless other applications. These applications are mostly based on the time measurement of time interval or pulse width corresponding to physical events. It is also used to measure the distance for some applications as radar and geolocation. This time measurement is generally performed by devices called time-to-digital converters (TDCs). These latter convert the time into a digital value, which facilitates the data processing and its integration in digital systems.

Time-to-digital converters (TDCs) are widely used for the time measurement. They quantify the measured time interval T and provides its digital value as a function of the time resolution, which often represents the time step of the digital clock or a gate delay. The time resolution is the most important parameter, which defines the time measurement performances. It presents the sampling step and the smallest time interval that can be measured. Otherwise, many parameters can characterize and take part in the TDC performances such as its dynamic range and latency. Many applications require precise time measurement in order to quantify physical or electrical events with a digital value such as high-energy physics, time-of-flight measurement, instrumentation and satellite positioning.

The first TDCs have been designed in the 60s for time-of-flight applications in high energy physics [52]. This first generation was based on analog techniques initially developed for the time-to-amplitude converters (TAC). The second analog TDC category was based on the time stretching technique, which does not require the analog-to-digital converters (ADCs) previously used. The analog TDCs provide a high precision and a good linearity. They are suitable for short measurement ranges. Especially, they show high performances in term of time resolution.

Today, fully digital approaches are mostly used for time measurement. Such an approach takes advantage of reduced die area, power and functional complexity. Moreover, digital TDCs can easily be integrated on-chip in CMOS technology. The simplest fully digital TDC architecture is based on counting the number of edges of a reference clock signal, as shown in Fig. 1.1. The converter starts counting the number of edges from the *Start* event to the arrival of the *Stop* event. Each measurement induces a quantification error at the beginning and at the end of measured time. The total error value is function of the time resolution of the converter. The smaller is the time resolution, the precise is the converter. So, the precision will depend on the achieved time resolution t_q.

TDC structures, with an effective time resolution of few picoseconds, are also presented. In the simplest TDC architecture, the time resolution is bounded by the CMOS gate delay. Many digital TDCs have been proposed dealing with time resolution improvement, which offer a sub-gate delay resolution. However, they generally present issues related to their limited dynamic range. Alternatively, in order to overcome this limitation, architectures using interpolation scheme or multi-quantization levels have been proposed to achieve wide measurement range with a fine time resolution. Therefore, repetitive measurement are mostly required in order to ensure high precise measurements without sacrificing the TDC linearity. Therefore on-the-fly measurements on fast non-periodic signals are particularly challenging in TDC designs.

A TDC structure, simultaneously propagating more than one event, has shown further performance improvement. In fact, the propagation of several events allows considering the phase difference as a time sampling step. Thus, the gate delay is subdivided into smallest time portions considered as the time resolution. Many structures dealing with this principle have been presented in the literature. They usually propose a full custom design of their delay gates, which integrate multiple inputs in order to couple together several oscillators. Consequently, the number of coupled oscillators is the ratio by which the time resolution is divided. Despite the high resolution and the wide measurement range provided by such topologies, they require a larger chip area and eventually more power consumption.

1.2 Thesis contributions

In this work, a new approach is presented for a fully digital TDC based on a self-timed ring oscillator (STRO). In such an oscillator, several events can be initialized and propagate without

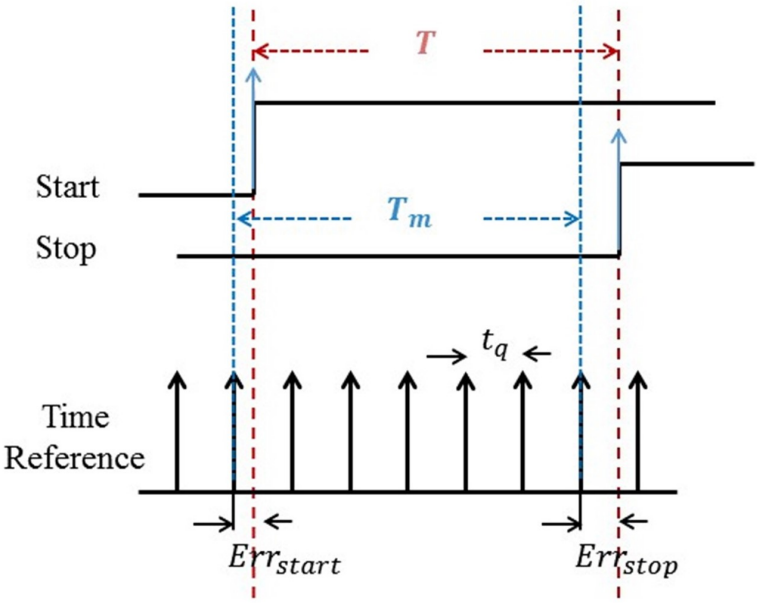

FIGURE 1.1: Digital time measurement principle.

colliding thanks to a request/handshake protocol. Due to the STRO characteristics, a regular time base is generated by exploiting its equidistant phases. Exploiting the uniform distribution of phases, a TDC architecture, adopting the STRO as a clock reference, is proposed.

The time resolution of this TDC can be accurately tuned as fine as needed by simply increasing the number of STRO stages. Its time resolution can be lower than the propagation delay of the used gates. This resolution is only limited by the noise floor of the STRO stage. Furthermore, the implementation is simple and suitable for all digital circuits. Moreover, it easily support the technology shrink. For applications requiring on-the-fly measurements with a fine resolution, the STRO-based TDC offers interesting perspectives compared to the other TDCs.

As a hardware proof-of-concept, our proposed architecture has been implemented in an Intel Cyclone IV. Then, an ASIC testchip has been designed and fabricated using CMOS AMS350 technology. The test of the circuit proves the validity of this new kind of TDCs.

This work is a first exploration of an architecture of time-to-digital converter based on self-timed ring oscillators. It is also a tight collaboration between the TIMA laboratory, *Université Grenoble Alpes (UGA)/CNRS* Grenoble, France and the STRS laboratory, *Institut National des Postes et Telecommunications (INPT)*, Rabat, Morocco. This collaboration has contributed demonstrating the efficiency of the architecture in terms of configurability. Thanks to the knowledge of the asynchronous circuits, a fully digital TDC architecture with sub-gate time resolution, wide dynamic range, for on-the-fly measurement, and without any calibration has been proposed. This work has been supported by the “Région Auvergne Rhône-Alpes” (France) grant n^o 150054650.

1.3 Thesis overview

This thesis is organized as follows :

Chapter 2 presents a literature review of different TDC architectures. It brings a detailed information about the first TDC generations based on analog techniques. Then, the recent main architectures based on digital techniques dealing with the time resolution improvement have been described. In addition, key performance metrics are given in order to examine the TDC performances.

Chapter 3 deals with self-timed ring oscillators (STROs) which are a promising solution for designing multi-phase clock generators. In STROs, the phase resolution can be adjusted as fine as desired by simply increasing its number of stages without frequency drop. Moreover, this resolution is not limited by the gate delay. In addition, different oscillation frequencies can be obtained by the same STRO depending on its initialization. In addition, the STRO phase noise analysis is also presented; $1/N$ phase noise reduction is obtained at the cost of higher power consumption when the number of stages is increased by N, and while keeping the same oscillation frequency.

The proposed STRO based time-to-digital-converter architecture is detailed in Chapter 4. Thanks to the STRO characteristics, a regular time base is generated by equidistant phases. In addition, the proposed TDC architecture allows on-the-fly time measurement on fast non-periodic signals. This new TDC architecture has been validate using precise high-level model and analog simulations using the $28\,\mathrm{nm}$ FDSOI technology from *STMicroelectronics*.

InChapter 5 and Chapter 6, two hardware proof-of-concepts of the STRO-based TDC have been respectively implemented in an FPGA Intel Cyclone IV and as an ASIC using the AMS350 CMOS technology. TDCs with different number of stages have been implemented to demonstrate the time resolution enhancement with an increased number of stages. Measurement results points out the advantages of this new TDC in terms of measurement accuracy and simplicity of implementation.

Finally, the conclusion Chapter 7 discuss the directions for our future research and the potential applications for the STRO-based TDC.

Chapitre 2

State-of-the-Art on Time-to-Digital Converters

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2.1 Introduction

Time measurement between two events is a key technique used in many fields such as high-energy physics, time-of-flight measurement, instrumentation and satellite positioning [6, 34, 48, 56, 60]. Devices called time-to-digital converters (TDCs) are widely used for precise time measurement. The time interval T to be measured is generally defined with a *Start* signal, which indicates its beginning, and a *Stop* signal, which points the end. The time conversion into a digital word (binary output code) facilitates the data processing and its integration in digital systems. Such an approach takes advantage of integrated circuits because they provide a reduced die area, low power consumption and complex functionality. Moreover, TDCs can easily be integrated on-chip in CMOS technology in a lager system.

The first generation of TDCs was based on analog techniques. They have been designed to enhance the previous technique initially developed for time measurement based on the time-to-amplitude converters (TAC) [33, 55, 61]. Recently, fully digital approaches are mostly used for time measurement. The simplest architecture of TDC is based on a timer counting the number of edges of a reference clock signal. The precision depends on the timer resolution (sampling step) by which the measurement is performed. This can be carried out by low-power and compact circuits.

Many TDC principles have been proposed in the literature as second generation of TDCs for improving the time resolution. In the simplest TDC architectures, the time resolution is bounded by a CMOS gate delay. In order to overcome this technological limitation, sub-gate delay resolution solutions have also been proposed [12, 42, 63, 68] corresponding to a TDC third generation. As a wide dynamic range of time measurement is required in many applications, dedicated architectures have been proposed. In order to achieve a wide measurement range with a fine time resolutions [76], several strategies can be employed such as interpolation schemes or multi-quantization levels. Nevertheless, while many of the proposed TDC architectures in the literature can achieve high measurement accuracy, they often require repetitive measurements. Therefore, on-the-fly measurements on fast non-periodic signals are really challenging for most of the TDCs.

This chapter provides a literature review of the main used architectures of TDCs [22]. In addition, key performance metrics are given in order to analyze the TDC performances. The chapter is organized as follows. The Section 2.2 exposes the main key performances metrics to

take into consideration in TDCs design. Section 2.3 and Section 2.4 respectively presents the main TDC architectures based on analog and digital techniques.

2.2 Time-to-Digital Converters : key performance metrics

Time-to-digital converters quantify the time between a *Start* and a *Stop* event and express their result as a digital value. Many parameters help to characterize the TDC performances. A set of parameters related to the TDC are firstly presented. Then, we discuss the linear and nonlinear imperfections of TDCs.

2.2.1 Main TDC metrics

2.2.1.1 Time resolution

The time resolution characterizes the measurement precision of a time interval T. It represents the minimal time that a TDC can correctly quantify. It is often referenced as the least significant bit (LSB). This parameter generally depends on the circuit characteristics, *i.e.*, the technology and the noise performances.

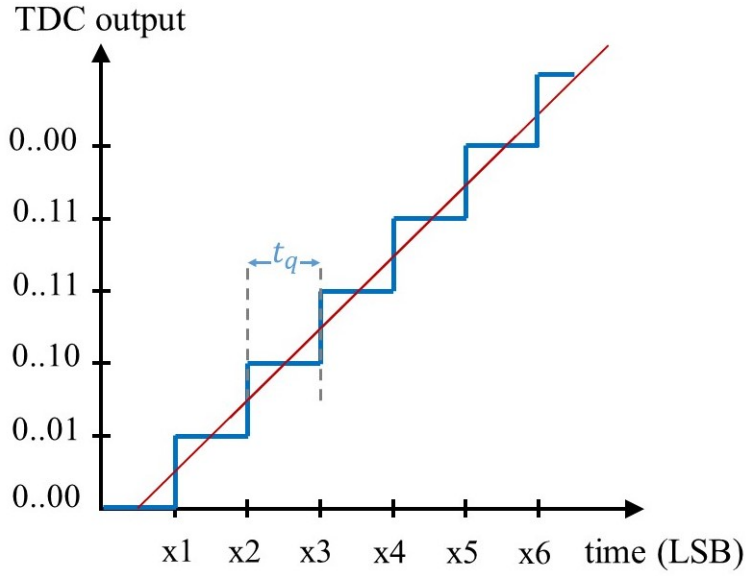

FIGURE 2.1: Example of TDC transfer curve in ideal case.

With an ideal TDC, a time equal to one LSB corresponds to the first non-zero code. Then, the TDC value is incremented for each time increment of 1 LSB. The resolution is in this case constant. The quantization characteristic is given on Fig. 2.1 for an ideal TDC in absence of any distortion. A variation lower than one LSB is coded by the same word. Thus, the transfer function is stepped curve with a step width of 1 LSB). In our study, the parameter t_q represents the time resolution.

2.2.1.2 Dynamic range

The dynamic range expresses the TDC maximal time input to correctly be quantified. For the structures using counters, this parameter is related to the number of bits of the counters. As illustration, a TDC with a 3-bit counter is presented in Fig. 2.2. The last code that this TDC is able to produce is . The time needed to show this code presents the TDC dynamic range, as shown in the figure. If we suppose that the number of bits of the TDC output is N, the dynamic range will be presented by the value 2^N.LSB [34].

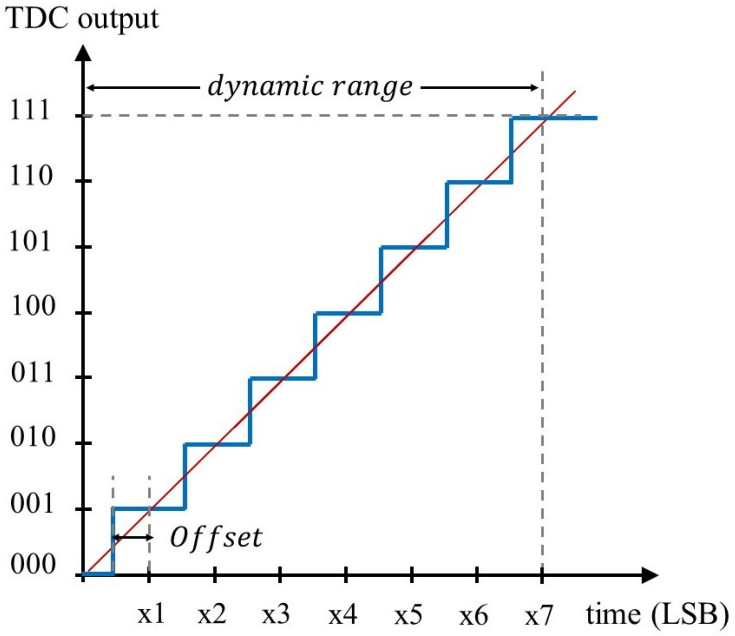

FIGURE 2.2: Example of TDC transfer curve (number of bits 3), showing the offset and the dynamic range of a TDC.

2.2.1.3 Conversion time

The conversion time is a performance parameter applied to a single measurement representing the minimal time needed for a TDC to digitize a time input into a valid digital word. This time is counted from the *Start* event as illustrated in Fig. 2.3). This value is very important for the high-speed applications for which a specific time conversion should be respected. Another parameter is the counting rate, which demonstrates how fast is the TDC conversion process. It can be required for applications such as fast image sensors.

2.2.1.4 Latency

This parameter gives information on the TDC rapidity to present a valid output. Indeed, the latency is the time needed after the *Stop* event to compute a valid digital word. This time is included in the conversion time as presented in Fig. 2.3.

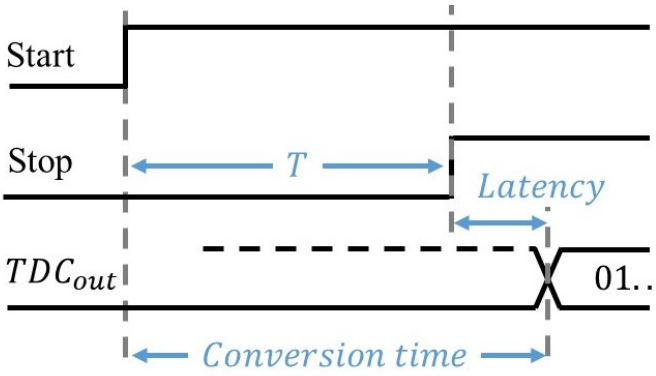

FIGURE 2.3: The conversion time principle.

2.2.2 Linear and nonlinear imperfections

The TDC imperfections can be classified into two categories. Firstly, the linear imperfections are easily detectable and not too much difficult to compensate such as the offset [34]. Contrarily, the nonlinear imperfections require advanced calibration schemes and cannot always be completely removed. The Differential and Integral nonlinearities are the most important static errors to analyze. Furthermore, if the errors are large enough, the TDC should have missing codes. This is a crucial issue affecting TDCs as illustrated in Fig. 2.4 (code i is missing).

In addition to these imperfections, noise sources like the jitter and the thermal noise can also degrade the performances of the TDC.

2.2.2.1 Offset error

The *Offset* represents a deviation of the TDC from the ideal first measurement which should be equal to 1 LSB. For $0 \leq t < LSB$, the code should be 0 until reaching a time equal to one LSB, as displayed in Fig. 2.1. The time difference between the time, t_1, where the first code 0..01 appears and the LSB present the offset error. The normalized value of this error, E_{Offset}, is expressed by :

$$E_{\text{Offset}} = \frac{t_1 - t_q}{t_q} \tag{2.1}$$

2.2.2.2 Quantization error

The conversion introduces a distortion between the digital output value and the original value. It is an inherent error related to any digital converter. Thus, the measured time interval is a function of the TDC output TDC_{out} given by :

$$T_m = \text{TDC}_{\text{out}} \times t_q + \varepsilon \tag{2.2}$$

where ε is the quantization error. The latter is generally modeled by a uniform random variable. The quantization error is the main error affecting the precision of a TDC.

2.2.2.3 Differential non-linearity (DNL)

For a specific code, the differential non-linearity corresponds to the deviation of the step width from the theoretical LSB step width. As a result, the real step width is equal to $\mathrm{LSB} + \mathrm{DNL}$ (DNL is a real number). The expression of the differential non-linearity value per one LSB describing the fluctuation effect for the code digit i is given by (2.3), where t_i represents the measured delay for the first appearance of the i^{th} step.

$$\mathrm{DNL(i)} = \frac{t_{i+1} - t_i}{\mathrm{LSB}} - 1 \tag{2.3}$$

2.2.2.4 Integral non-linearity (INL)

The integral nonlinearity (INL) is a measurement of the gap between the transfer characteristic and the straight red line in Fig. 2.4. It represents at the same time the cumulative deviation of each step from an ideal value providing a measurement of the non-linearity [34]. The INL is obtained by integrating the DNL curve. Thus, the cumulative i^{th} INL is expressed by :

$$\mathrm{INL(i)} = \sum_{k=0}^{i} \mathrm{DNL_k} \tag{2.4}$$

The INL (as the DNL) can be presented by its maximal value or by its root mean square (rms) value over all steps. They are usually normalized to be expressed in LSB.

Many architectures have been proposed in the state-of-the-art for dealing with fine time resolution. They have to ensure a large dynamic range, on-the-fly measurement and, if possible, without requiring complex calibration. Generally, it is difficult to combine all these wished properties in the same structure especially because the TDCs handle with many other parameters affecting its performance.

2.3 Analog time-to-digital converters

The first proposed architectures of the time-to-digital converters were based on the analog techniques. They are suitable for the short measurement ranges since they provide a high precision and a good linearity. The traditional structure is based on the conversion of time interval to voltage. They show high performances in term of time resolution because they are able to reach a few picoseconds [42, 69]. Moreover, these measurements are usually requiring a calibration and/or an averaging process. This first category of analog TDCs requires the use of analog-to-digital converter (ADC). Thereafter, the ADC has been removed for the second category, which

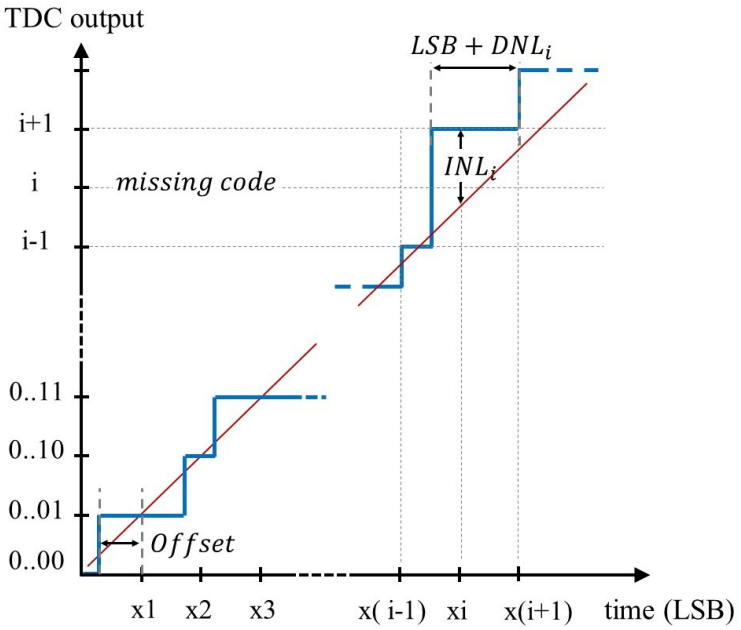

FIGURE 2.4: TDC nonlinearity example.

basically implements time stretching techniques.

2.3.1 Analog TDCs based on analog-to-digital converter

Based on a similar principle of ADCs, the classical analog approach converts into a voltage the time interval T [47,55,61,69]. Traditionally, one possible way to generate the corresponding voltage is to use an integrator, in which a capacitor is charged with a constant current source, as presented in Fig. 2.5. The integrator transforms the pulse into a voltage corresponding to the time intervals T. Then, this voltage is converted thanks to an ADC providing the digital output. The analog design constraints of the ADC limit the finest resolution t_q. Moreover, the trade-off between the resolution and the dynamic range (DR) should also be considered. A high resolution means a short time to sweep from ground to the supply voltage at the ADC input and, thus, limits the time DR. On the opposite, a large DR assumes to have a longer time to go from zero to the supply voltage (the time step increases as well). Otherwise, the dependence between these parameters can be expressed mathematically by :

$$\mathrm{DR} = 2^{N_{\mathrm{ADC}}} \cdot t_q \tag{2.5}$$

where N_{ADC} is the number of bits of the ADC and DR is the dynamic range.

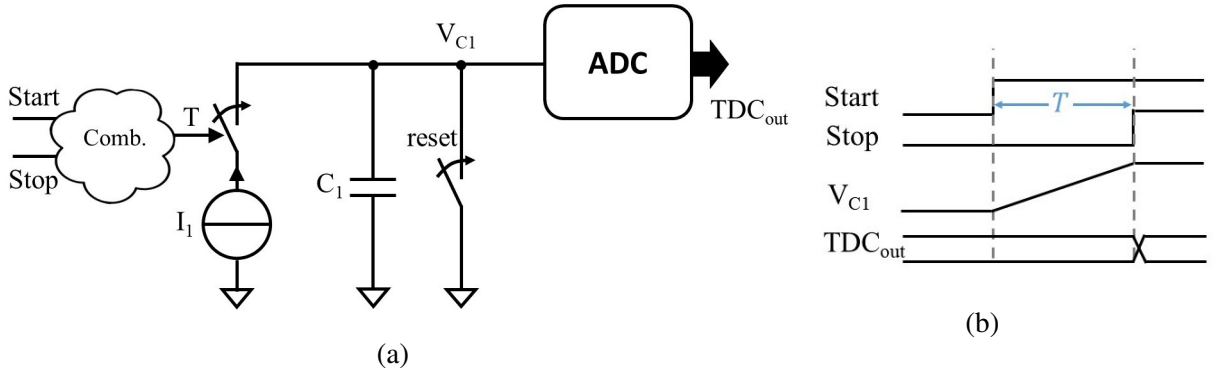

FIGURE 2.5: Analog TDC based on Analog-to-Digital converter : (a) Basic architecture, (b) timing diagram.

2.3.2 Analog time-to-digital converters with time stretching

2.3.2.1 Single integrator stretching

The most common structures of analog TDCs are based on the pulse-stretching techniques [28, 53]. In this case, no ADC is used and its limitation is eliminated. The principle is to charge the capacitor C_1 with a first current source I_1 and then to discharge it with a lower current source $I_2 = I_1/N_I$, as illustrated in Fig. 2.6a. A comparator is used to detect when the second integrator completes its discharge operation (time for zero-crossing), which corresponds to the time interval multiplied by the ratio N_I between the two current sources. A counter controlled with a stable clock reference records the number of cycles during this operation. Thanks to this architecture, as the capacitor C_1 is discharged slowly (N_I times), capturing the time with a better resolution becomes easier as the time has been stretched.

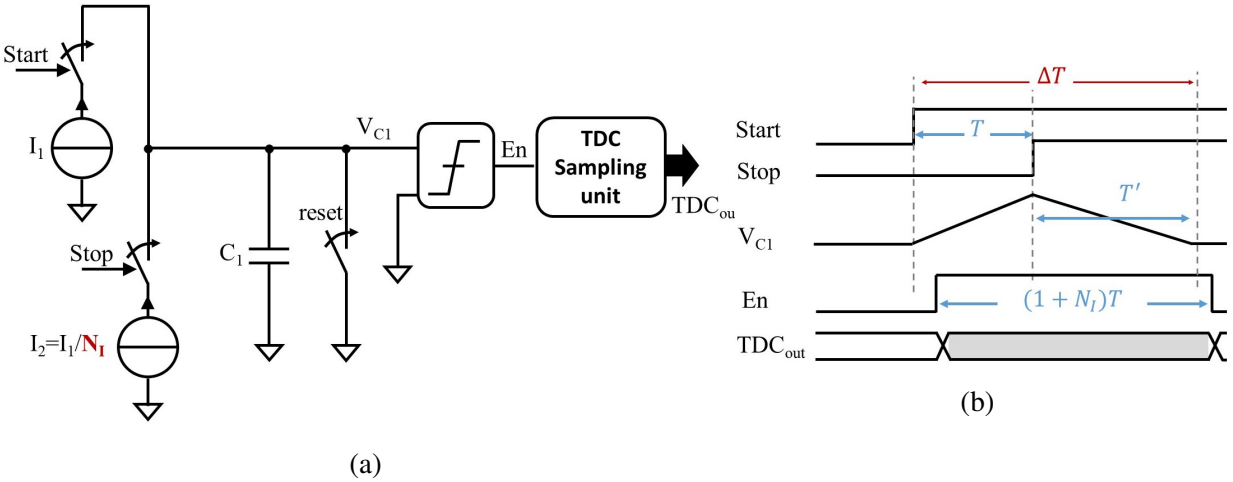

FIGURE 2.6: Analog TDC with time stretching/amplification :(a) single-slope integrator architecture (b) timing diagram.

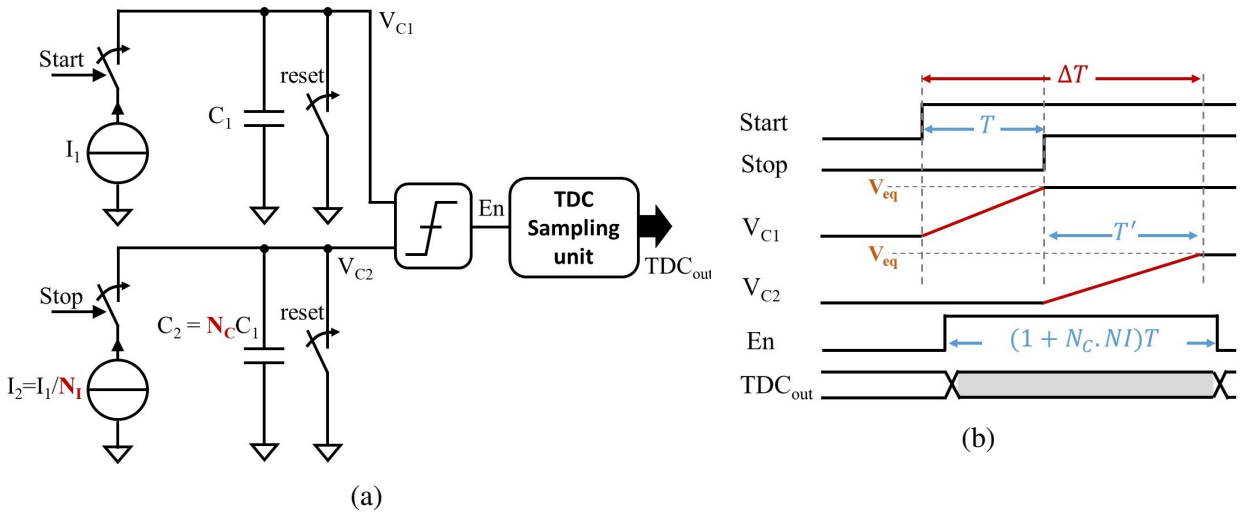

FIGURE 2.7: Analog TDC with time stretching/amplification :(a) dual-slope integrator architecture (b) timing diagram.

2.3.2.2 Dual-slope conversion

Another type of the analog TDC is based on the dual-slope time stretching approach [10,56]. This TDC is inspired from the principle of dual-slop analog-to-digital converter (ADC) with a reversed operation, which defines a voltage and integrates the unknown time T without requiring an ADC [34].

Similarly to the single-slope, the principle is to charge the first capacitor C_1 during time T with a first current source I_1 when the *Start* event is presented. This capacitor becomes floating when the *Stop* event is arrived. This latter will command a second capacitor $C_2 = N_C \cdot C_1$ to be charged with another current source I_2 during the interval time $T^{'}$. The equivalent circuit of this approach and its timing diagram are displayed in Fig. 2.7.

If I_2 is N_I times smaller than I_1 and C_2 is N_C times greater than C_1, the time resolution will be reduced by $N_I \times N_C$, presenting the stretching factor of the dual-slope conversion. We can explain this differently by considering a second integrator. So, with the arrival of the *Stop* event, the other integrator starts to integrate the process with a factor of $N_I \times N_C$ by considering the time interval T_2.

$$\Delta T = T + T^{'} = (1 + \frac{C_2 I_1}{C_1 I_2})T = (1 + N_I \times N_C)T \tag{2.6}$$

A comparator detects when the second integrator is equal to the first one because this happens exactly after $N_I \times N_C \times T$.

This approach is very attractive with a factor $N_I \times N_C$ enough large since a TDC with moderate performances can be used. It is very interesting for the resolution enhancement. One advantage compared to the single-slope is that the absolute values of devices are not relevant against the ratios N_I and N_C. Thus, stretching the time with a factor $N_I \times N_C$ is not requiring

large device values that can be implemented with basic components as presented in [53]. For design facility, controlling the capacitance ratio is easier than controlling the current source ratio since it is adjusted by simply modifying the area. However, this architecture has high power consumption and is sensitive to a temperature drift [56].

2.3.2.3 Triple-pulse time stretching

To further improve the time resolution, triple-slope stretching schemes have been proposed [41]. In this paper, a coarse counter, a single triple-slope stretcher, and a fine counter are used. In this structure, the analog approach is combined with the digital approach for time measurement. The triple-slope stretcher considers three-time intervals. In accordance with a clock reference, the interval T is divided to time interval T_m and the error quantification time intervals ΔT_{Start} and ΔT_{Stop}. A time splitter is used to feed the triple-slope stretcher with these intervals [41].

This structure has an area reduction of 40% compared with the dual-slope TDC presented in [10] since it just requires two capacitances and one comparator for its implementation. The TDC has been implemented in $350\,\mathrm{nm}$ CMOS technology. A $0.357\,\mathrm{ns}$ time resolution was obtained by using a $175\,\mathrm{MHz}$ reference clock. The structure has shown an achievement of a dynamic range of $1.46\,\mu\mathrm{s}$.

2.3.3 Conclusion

The analog TDCs are able to reach a time resolution that can only be a few picoseconds [42]. Nevertheless, they suffer from several fundamental issues. Firstly, the used current sources are sensitive to a nonlinear output and a finite output resistance. Therefore, the linearity of the TDC can be degraded especially for large dynamic ranges since the analog TDCs are known to be sensitive to a temperature drift [34]. Secondly, they are not suitable for fast applications due to limitation related to the dead time [13]. Mostly, the measurements are not feasible without calibration schemes or an averaging process. Otherwise, these TDCs require a large area due to the use of capacitors which induce more power cosumption in comparison to the digital counter part [13]. Thus, they are few suitable for the technology shrink since they require complex adaptations.

2.4 Fully Digital Time-to-Digital Converters

Fully digital techniques have been deployed to overcome the issues presented by the analog TDCs. These can be carried out by very small, low power and simple circuits. The usual architecture of a TDC is simply based on counting the number of edges on a reference clock signal or to propagate an event into a delay-line during the time interval to be measured, as illustrated in Fig. 2.8. Obviously, for an all-digital PLL (ADPLL), the analog TDC are not solicited. In this

case, the digital TDC offers a suitable solution that can be deployed as a digital phase detector [13, 34, 60]. A digital value of the phase error between the reference clock and the feedback signal is given with a configurable CMOS architecture benefiting from a small area and a low power consumption.

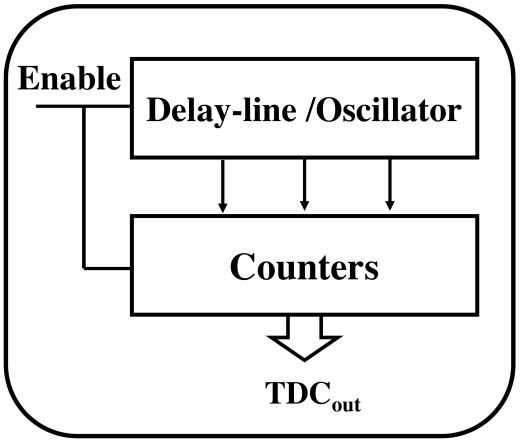

FIGURE 2.8: Generic TDC architecture.

2.4.1 TDC with gate-delay resolution

2.4.1.1 Delay-Line based TDC

A TDC with gate-delay resolution, called delay-line based TDC, is depicted in Fig. 2.9a. It is a compact architecture that has been proposed as a first fully digital solution. The line is composed of many stages of buffers or inverters [4]. Globally, the *Start* signal polarity is respected more with buffers than for inverter delays [34]. In this architecture, the *Start* signal provides an event propagating along the delay line. The arrival of the *Stop* signal triggers the registers to start copying the state of each gate output. The interpretation of the flip-flop (FF) outputs gives the measured time interval T_m. In other words, T_m corresponds to the number of stages that have propagated the *Start* signal. The measured time is defined by the thermometer code given by the output registers. The process is more explicit in Fig. 2.9b. This topology is the basis for most of the other digital TDC architectures. Admittedly, this TDC is a simple structure that can easily be integrated into an ASIC or an FPGA but at the price of moderate performances. It presents a low latency because the output can be quickly available after the arrival of the *Stop* event. However, its resolution is bounded by the CMOS gate delays ; it cannot be lower than the propagation delay of a logical gate. In addition, to cover a larger time interval, the number of stages must be duplicated as needed. Thus, the cost and power consumption will be increased. This concerns as well the maximal sampling rate, which is decreased when drastically expanding the clock tree.

Otherwise, the PVT variations affect the delay of the stages [34]. The jitter contributes to the measurement errors due to the temperature and supply voltage variations. With the accumulation of these random variations, the delay-line may present an important deviation at its end. Furthermore, the linearity could be affected by the random mismatch of the delay-line gates. Therefore, the delay-locked-lines (DLLs) are often deployed to calibrate the process variations [38]. The delay unit of the DLL is voltage-controllable, which allows locking its delay to a fraction of a reference clock whatever the variations [35].

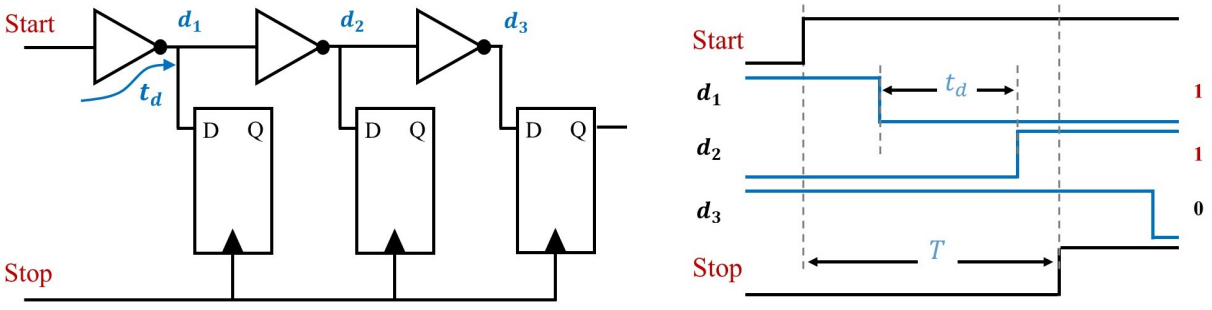

FIGURE 2.9: (a) Basic implementation of a delay-line based TDC, (b) the timing diagram.

2.4.1.2 Ring Oscillator

A simple way to overcome the limitation of the dynamic range of the delay-line TDC is to wrap the line into a ring [7,45,62,63]. This makes the inverter ring oscillator (IRO) as shown in Fig. 2.10a. Compared to the simple delay-line, each stage can be used several times. Therefore, the electrical event, which provides the time stamping, will propagate several times in the ring to cover large dynamic ranges. Moreover, a gain of power and area is obtained.

If double edge is considered, using CMOS inverters or buffers as delay gate is the same. Else, using inverters instead of buffers allows doubling the resolution [34]. However, the problem of the transition slope asymmetry related to the design of inverters, can affect the linearity of the TDC. This can be fixed via design but any process variation can produce similar problems [34].

The *Start* and *Stop* signals can be replaced with one *Enable* signal provided by a digital logic block [63]. The multiplexers are used to feed the ring with the adequate signals. However, they are source of asymmetry in the delay-chain, which increases the mismatches and affects as well the linearity performances [34]. Thus, the multiplexer was replaced by NAND gates. Similarly, counters are replacing registers to determine how many times the event looped in the ring. Therefore, the TDC output is obtained by counting the number transitions occurring during T of each delay output and summing the result to express the binary code. In this TDC, high-power consumption occurs due to the free-running mode of the IRO [13]. Otherwise, to simplify the architecture, one counter can be connected to the final stage to measure the number of cycles, for which the event has looped back, providing a coarse evaluation of the time. The

other output registers can be used to evaluate the fine measurement. As a result, a gain in area and power consumption is obtained.

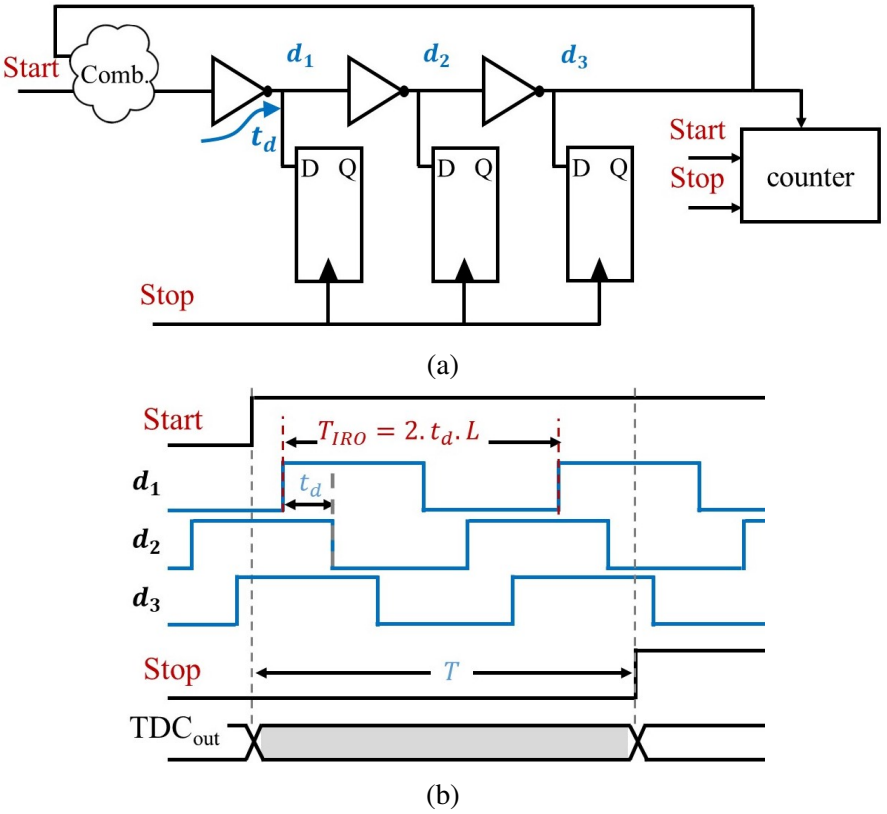

FIGURE 2.10: Inverter Ring Oscillator based TDC example and its timing diagram.

The oscillation frequency of the IRO is a function of the stages number. In this structure, every stage inverts the previous output as illustrated in Fig. 2.10b. To keep alive the oscillation, the ring requires an odd number of stages. The event that can propagate in the IRO is represented by two successive outputs '0' or '1'. Assuming that the IRO includes L stages having as propagation delay $t_q = \mathrm{INV}_{\mathrm{gate_delay}}$, the oscillation period is expressed by (2.7). The period of this oscillator is twice the number of stages by t_q since the event has to propagate twice to come back to the initial polarity [34]. The minimum number of stages to guarantee a stable oscillation is $L = 3$. For this configuration, the highest oscillation frequency is obtained according to (2.7) while the time resolution remains the same.

$$T_{RO} = 2L \times t_q \tag{2.7}$$

As in the case of simple delay-line TDC, the time resolution of the IRO-TDC cannot be lower that t_q which is fixed by the technological parameters.

Propagating many events in the same structure allows exploiting the phase difference, and thus improving the resolution. In IROs, only one event can propagate. However, in [7], a modified structure of the ring oscillator allowing to propagate two events has been proposed. The

time difference between the insertions of the two events should be well defined in order to avoid any collision between the events. The challenge for this architecture is to ensure the same oscillation period for both events. Unfortunately, since the inverters cannot guarantee the same delay per stage, this oscillator has periods that are not uniform. Indeed, the first event can propagate with a period different from the second event. Consequently, the probability that the events catch up each other is very high. Finally, the paper states that the mismatch between the stage delays can therefore be averaged out.

As known for IROs, the number of stages has to be odd to oscillate. The structure of [7] was based on even number of stages, which presented some issues. Thus, a modified structure called "Third-Harmonic Ring TDC" was proposed in the same paper [7], including an odd number of stages. It is based on the same principle while injecting one of the two events twice in different places in the ring. In this oscillator, the stages have been replaced with AND and XOR gates, which offers the advantage of a fully digital and scalable structure. In addition, the TDC presents a sub-gate delay resolution of 55.5 ps (the technology was not reported) since many events have been initialized. Notice that the measurement results have been processed by using an averaging technique, which limits the on-the-fly measurement ability.

2.4.1.3 Gated Ring Oscillator

An improved topology, called gated-ring oscillator (GRO), has been proposed to limit the power consumption due to the free running mode in IROs [45, 62, 63]. This mode is a consequence of the propagation of the timing events even if the measurement has been stopped. As shown in Fig. 2.11, the inverters are gated with an *Enable* signal to turn OFF the oscillator outside the interval measurement. In addition, the status at each inverter output is frozen and kept until the next measurement. By frozing the state of the oscillator between measurements, the quantization error is saved and transferred to the next measurement. Herafter, an averaging of the successive measurements allows limiting the accumulation error. This structure benefit from the first-order noise shaping [63].

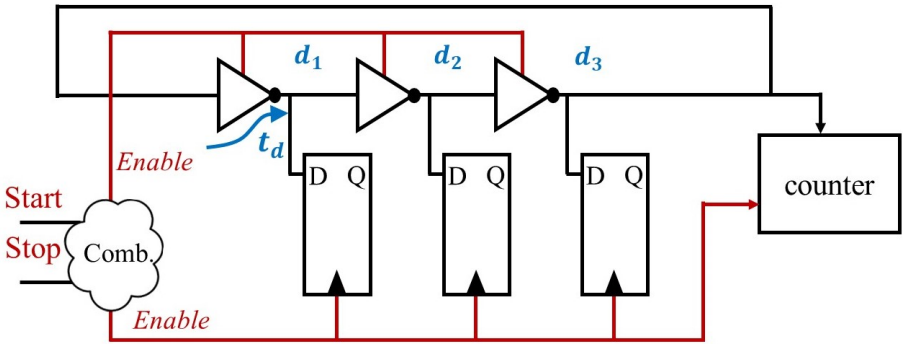

FIGURE 2.11: Gated Ring Oscillator based TDC.

The benefit from the gating technique, especially with successive measurements, is the increased effective time resolution which cannot be achieved for a simple measurement [34]. Otherwise, the time resolution of this TDC is still limited by the ring stage delay. In addition, the signal controlling the frozen state of signals should be able to stop and start the signal propagation in any state ; else the measurements will not be correct. Many techniques can be used to gate the inverter. The custom design is a simple implementation, which is based on adding transistors to the main branch of the inverter implementation [45, 63].

2.4.2 TDC with sub-gate-delay resolution

2.4.2.1 Vernier based TDC

Standard Vernier In order to overcome the gate-delay limitation, sub-gate delay resolution solution called Vernier-TDCs have been proposed [19,57]. This technique is the oldest and more documented digital TDC structure [62]. Fig. 2.12 illustrates the Vernier-TDC architecture. In this topology, the events *Start* and *Stop* propagate in two delay lines having slightly different propagation delays t_{d1} and t_{d2} ($t_{d1} < t_{d2}$). At the beginning of the measurement, they propagate with a time difference equivalent to T. Then, they start reducing slightly the time difference until they become in phase. At that point, the *Stop* signal catches the *Start* signal and the order is inverted [34]. The Vernier stage i, called the tap i, is referred to a combination of two delay gates i : one from the first line and the other from the second line. In Fig. 2.13, an example of timing diagram of the Vernier TDC is presented. In this example, the measurement of the interval T needs four taps to inverse the order of the *Start* and *Stop* signals. The output signals of the first tap start with a time difference of $T - t_q$. Then, the second one is $T - 2t_q$ and so on until the two signals are in phase. Subsequently, the number of taps to verify this condition corresponds to the TDC output, which is expressed by the resulting effective resolution $t_q = t_{d1} - t_{d2}$ smaller than the stage delay [19]. In this case, no matter the technology is used, the time resolution is sub-gate. Actually, the Vernier is deployed in many TDC architectures as it will be seen in sequel due to its fine time resolution.

As any open structure, such as the delay-line, the Vernier is not appropriate for large dynamic range measurements otherwise it presents some issues. In fact, for a maximal time interval T_{max}, a maximal number of stages $N = \frac{T_{max}}{t_q}$ is required for each line. Therefore, the time resolution enhancement will be limited by the area. In addition, the latency, which represents the most critical issue of the Vernier, depends on the length of the time interval. On the other hand, since two delay-lines are used, the jitter is duplicated and the TDC becomes more sensitive to mismatch. In addition, the delay-lines have to be well matched. Notice that it is very difficult to precisely adjust the time difference without using complex calibration schemes [13]. Finally, all the delay gates are switching many times, independently of the T length, especially with successive measurements. This increases the power consumption.

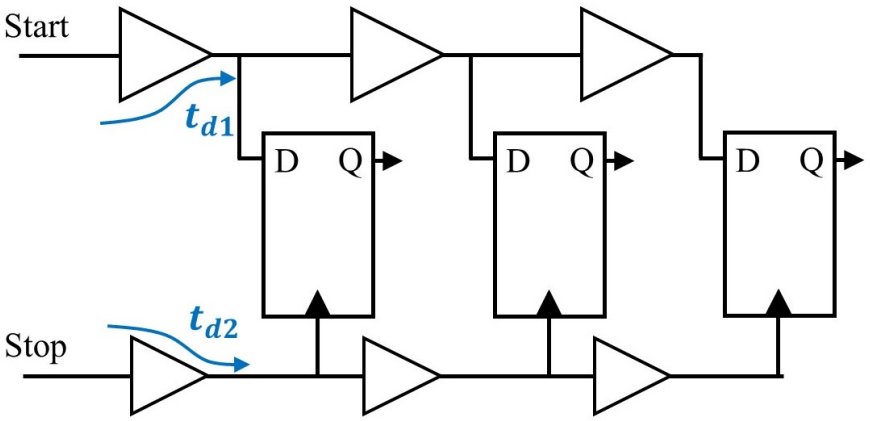

FIGURE 2.12: A Vernier delay-line TDC structure.

The possibility to inject other events on the TDC while the previous ones are propagating is possible. However, it requires additional overhead for synchronization of the measurement results [34], and it can cause glitches on the TDC output.

Two-dimension Vernier TDC An advanced topology using two orthogonal dimensions, called 2D-Vernier based TDC, has been proposed [68]. This structure increases the dynamic range and also provides extra freedom degrees for reducing the latency. It minimizes the length of the delay-lines to one third of lines used to cover the same dynamic range. Compared to the simple Vernier, the linearity of this type of TDCs is more sensitive to the delay variations. Thus, any delay variations can cause a large non-linearity.

Vernier ring oscillator TDC To exploit the sub-gate resolution given by the Vernier, hybrid techniques have been proposed using ring oscillator (RO) [79] or gated ring oscillator (GRO) [45]. The architecture of this hybrid TDC with a GRO is presented in Fig. 2.14. They keep the same principle of the Vernier by just replacing the delay-lines by ring oscillators. The loop structure allows reusing the delay-line many times. As a result, they offer a large dynamic range. As illustration, a Vernier-RO TDC is presented in [79]. In this TDC, arbiters are used to locate where the *Start* and *Stop* signals are in-phase. The measurement is processed within two types of laps, one for the rising edge and the second one with falling edge. Likely, Vernier GRO-TDC has been proposed [45] to benefit from low power consumption and first-order noise shaping mechanism.

As the standard Vernier, the principle is based on cyclic propagation of events over the taps as shown in Fig. 2.13. To make it simple, we only consider a single phase. Theoretically, the measurement of time interval T can be divided into two parts. The first coarse measurement considering the first RO having an oscillation period $T_1 = 2Lt_{d1}$, where L represents the number of stages. During T, the number of the rounds needed to count T_1 is N_1. The time residue from

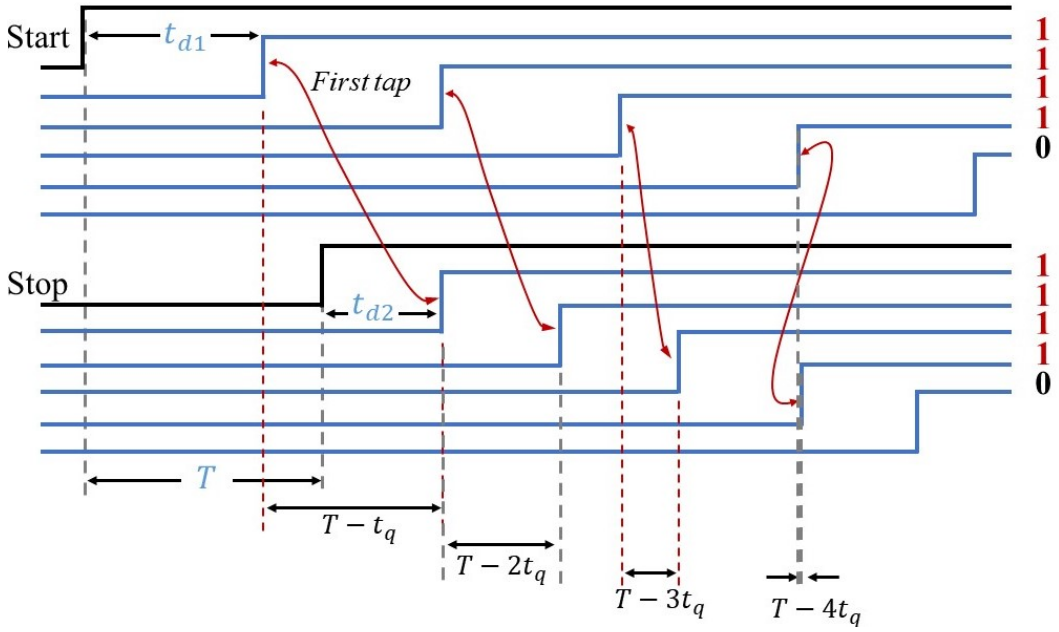

FIGURE 2.13: operating principle of the Vernier TDC.

this coarse measurement can be quantified by the time resolution t_q. Thus, we suppose that N_2 is the result of this second measurement. Therefore, the measured time interval is expressed by :

$$\begin{aligned} T_m &= N_1 T_1 + N_2 t_q \\ &= N_1 \cdot L \cdot t_{d1} + N_2 \cdot (t_{d1} - t_{d2}) \\ &= \underbrace{(N_1 \cdot L + N_2)}_{X} \cdot t_{d1} - \underbrace{N_2}_{Y} \cdot t_{d2} \end{aligned} \tag{2.8}$$

$T_m = kX - (k-1)Y$, where $k = t_{d1}/t_q$ and $k - 1 = t_{d2}/t_q$ (the resolution is given by $t_q = t_{d1} - t_{d2}$). This equivalent to a standard Vernier with a first line of X delays and a second line with Y delays, where X and Y are expressed by :

$$X = Y + L \cdot N_1 \tag{2.9}$$

The longer is L, the wider is the latency. This is explicit from the expression of X, since that for the standard Vernier, X should be equal to Y. As a result, within this architecture, a fine time resolution is achieved with large detectable ranges due to the looped structure, which allows reducing the area and power consumption compared to the standard Vernier [79]. However, when the resolution targets the picosecond level, these techniques suffer from a degradation of their linearity and are subject to the jitter accumulation [13, 45, 79].

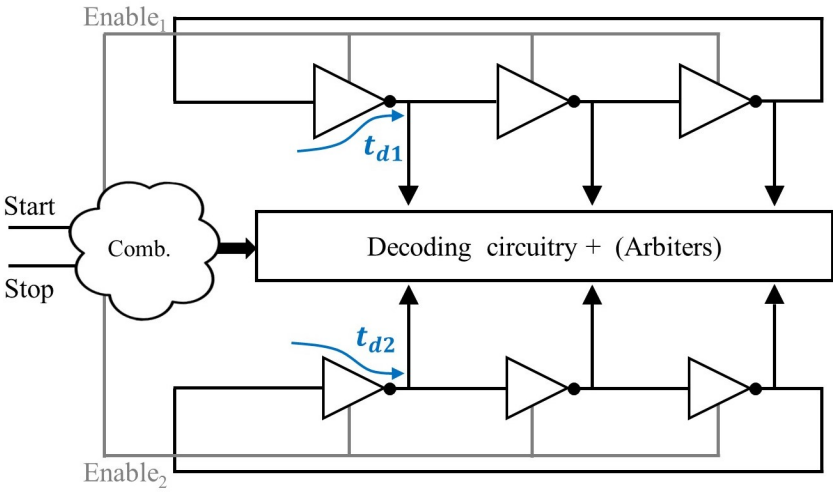

FIGURE 2.14: Vernier gated ring oscillator TDC.

Two-dimension ring oscillator Vernier TDC The 2D-RO Vernier TDC (see Fig. 2.15) has been developed to reuse delay lines and gain more performances compared to the previous structure [44, 46]. The principle is to extend the time step quantification. Instead of considering a fixed value t_q for the taps, the two dimensions offer more flexibility for interpolating steps between axis values. This is an effective solution for high resolution and reduced latency time. If only (2.8) is considered, we can appropriately chosen the value of X and Y, which can enlarge the space of possible solutions.

To explain the operating principle, we suggest taking the same example as in [46]. We consider a TDC with $L = 3$ and $T = 38t_q$. If a simple RO-vernier is applied for this configuration, the first RO will be in phase with the second one when $X = Y = 38$. According to (2.8), it can be noticed that the same result is obtained for minimal values $X = 4$ and $Y = 2$ in the case of a two dimensional approach and in case the equation of (2.9) is broken. In this situation, the successive values of axis are not used anymore because that a two dimension is included (not only delays of the diagonal line are used). In other words, the arbitration should be applied for every combination between stages of both ROs, and not only for phases with the same number of stages (regular taps are not used anymore). As a result, instead of considering a latency of $38t_{d1}$, it can be reduced to $4t_{d1}$. To combine these advantages with the first noise shaping technique, it is recommended to use a GRO (Fig. 2.15). However, such as the case of 2D-Vernier, this architecture is sensitive to delay variations and its linearity is easily degraded.

Indeed, for the first proposition [44,68], the Vernier plane was not entirely used. Despite this, the architecture offered almost three times extensions compared with the standard RO Vernier. Then, the plane was extended to be used in totality as cited in [46]. In this latter, the 2D-Vernier GRO TDC was proposed with a digital calibration and thus a time resolution of $2.2\,\mathrm{ps}$ was obtained with an implementation in $65\,\mathrm{nm}$ CMOS technology. This TDC shows a latency of $2\,\mathrm{ns}$.

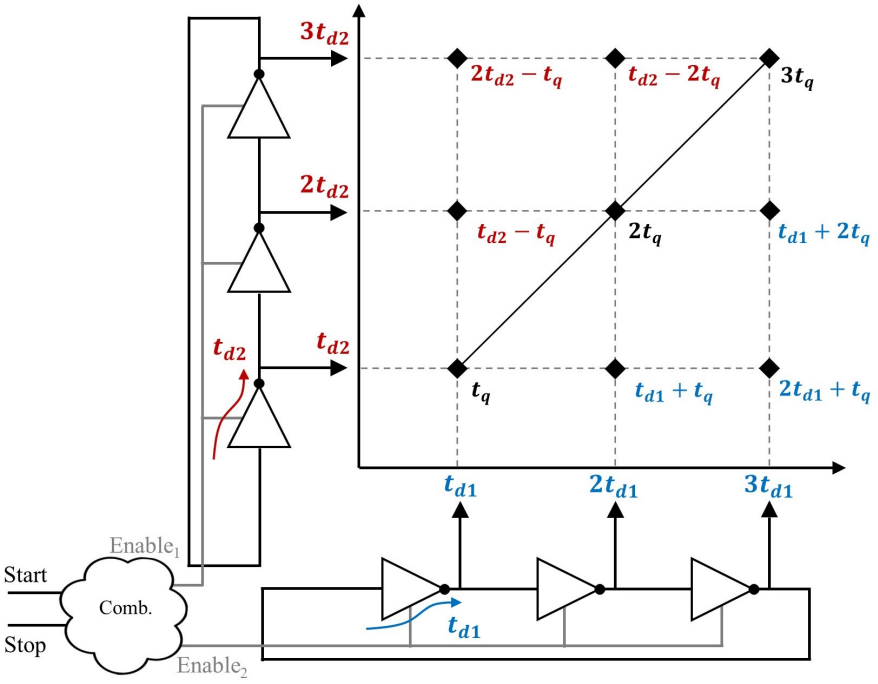

FIGURE 2.15: 3×3 2-D Vernier gated ring oscillator TDC.

2.4.2.2 TDC with interpolation technique

Generally, hybrid approaches present further interesting results. For TDCs, the interpolation allows to combine the advantages of several architectures. Mainly, the interpolation is often proposed as an alternative to cover a wider dynamic range, because the sub-gate resolution requirements tend to limit this latter. Notice that most of the proposed TDCs with interpolation are based on time stretching. These techniques require the use of at least two successive conversion schemes. Technically, the first one quantifies the coarse conversion with a wide range TDC and the second one amplifies and/or measures the residue error resulting from the previous conversion using a high resolution TDC [42, 51, 76].

Local passive interpolation The local-passive interpolation is originally based on introducing parallel resistive voltage dividers between the inputs of the delay gates and their outputs in a delay-line. The goal is to create intermediate signals. Thus, the effective delay per stage is reduced based on the averaged impedance at each output [34, 62]. A cyclic architecture is required in order to appropriately sample all the signals, which may increase the size and the circuit complexity [62]. The resistive voltage dividers can be advantageously replaced by digital gates. This technique is essentially based on the fan-out of the gates. The main issue of this TDC is that during the switching transients, the TDC can be limited by the non-linear impedances of the delay elements [63].

As an axample, a TDC with an interpolation factor of four has been implemented in a $90\,\mathrm{nm}$

CMOS technology [34]. In this local-passive TDC, 7-bit delay line is used achieving a time resolution of $4.7\,\mathrm{ps}$ at a supply voltage of $1.2\,\mathrm{V}$ and $3.9\,\mathrm{ps}$ at $1.4\,\mathrm{V}$.

Differential delay-line interpolation Similarly to the local-passive interpolation, differential delay-lines have been proposed [34, 37]. In fact, the need for stable delay gates, which is not generally trivial to implement, encourage researchers to develop techniques such as differential delay elements. This principle has been integrated in delay-lines for an interpolated TDC, which is known as parallel scaled delay technique [37]. In this example, the coarse measurement is measured using a counter and the fine measurement is assured with a DLL. In this TDC, 20 effective delay elements are used : 8 for the interpolation of the clock reference, 4 for the coarse interpolator, and 8 for the second interpolation level. The reference clock cycle is divided into 32. The TDC employs two interpolation levels : the coarse interpolator forms 16 times samples and the fine interpolator divide the input clock into 32. Therefore, the total effective interpolation ratio is 16384, which is the product of the different interpolation level ratios. The obtained time resolution using $350\,\mathrm{nm}$ CMOS technology is $12.2\,\mathrm{ps}$.

In other TDC structures using the interpolation [35, 57], the fine measurement is quantified using the Vernier structure since it remains the most attractive solution for a sub-gate time resolution. The proposed TDC in [35] achieved a time resolution of $24\,\mathrm{ps}$ to $30\,\mathrm{ps}$ for an input reference clock within $130\,\mathrm{MHz}$ to $160\,\mathrm{MHz}$ using $350\,\mathrm{nm}$ CMOS technology.

Multi-path GRO Another solution to obtain a sub-gate delay resolution is to exploit the phase difference between events propagating in different rings. Straayer *et. al.* [63] presented an architecture based on this principle using a multi-path GRO.

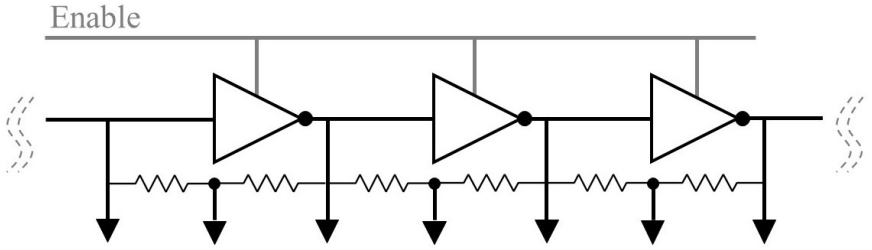

FIGURE 2.16: GRO creation of sub-gate-delay spacing using resistive ring interpolation [62].

An initial structure used in multi-phase oscillator applications, to obtain sub-gate resolution, is to use a resistor ring as displayed in Fig. 2.16. This is not the case for the GRO. It seems that the gated inverters within this oscillator maintain a current that is still present even though no signal is processed (after the gating operation). The solution to the aforementioned problem is to replace the ring of resistors with interpolate inverters [63]. The implementation of the inverter gate has been modified to include multiple inputs and a single output. These multiple inputs

allow coupling the oscillators together, which makes the oscillation more robust. This makes another possibility for creating sub-gate-delay resolution by coupling many oscillators together. Theoretically, an oscillator of L stage, coupled with other $M-1$ oscillator, will reduce the effective delay per stage by a factor of M. This architecture benefits from the first order noise shaping due to the use of the GRO. Two transistors, controlled by the *Enable* signal, are included in the inverter gate in order to ensure this gating operation.

For a minimal design goal, the proposed inverter gate in [63] has been designed with five inputs as displayed in Fig. 2.17a. Additionally, for rejection of undesirable modes, a prime value of the number of stages is recommended.

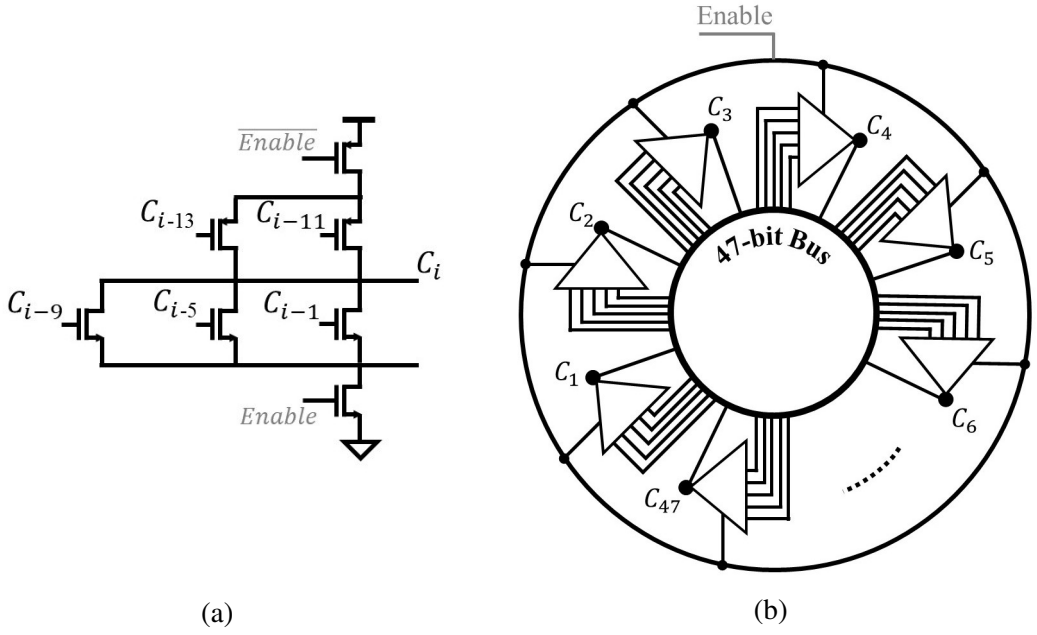

FIGURE 2.17: (a) implementation of the i^{th} delay stage, (b) Schematic of the proposed multipath GRO in [63].

Using this interpolation technique, a time base with an average resolution which is lower than the gate delay is presented. In practice, the effective time stamping is not regular : locally, the effective resolution may be either higher or lower than the gate delay. In [63], a 47-stage penta-path GRO is used as illustrated in Fig. 2.17b. For minimizing the area, the proposed inverter gate has been designed with five inputs. The average resolution is improved by over a factor of 5 compared to the basic GRO structure. The corresponding logic unit of this structure is more complicated and not obvious to design. Since the architecture requires full custom design instead of using standard cells, the transistors technology scaling is not simple and purely requires a complete TDC redesign. Moreover, getting a robust implementation with a low power consumption and a small area is really challenging, especially when the measurement of a time interval T requires a sub-gate delay resolution.

Interpolation with time variation Pulse shrinking is often an unwanted effect in TDCs because it limits the time interval [34]. Notice that some TDCs are based on this effect to get sub-gate delay resolution. For a digital approach, the slope asymmetry of each delay stage is exploited to generally reduce the pulse width. In practice, a pulse width can be generated with the rising edge of the *Start* signal and the falling edge of the *Stop* signal. As considered for the Vernier technique, the pulse width becomes smaller while propagating in the structure until that the pulse disappears at a specific position. Power and area are function of the dynamic range. This concerns as well the latency and the conversion time. Thus, this dependance on the measurement time imposes some problmes for interfacing [34]. Moreover, PVT variations are able to disturb the sampling operation, especially when the pulse becomes very small before vanishing.

Contrarily, many interpolation techniques are based on time amplification. The time interval cannot be directly amplified but the small-time residue from each tap after a coarse measurement. In fact, the time amplifiers can only amplify small time intervals due to their small dynamic range. In [42], the time interval is first quantified with a counter as a coarse measurement driven with a high-stability reference clock. Then, the remaining time of this first quantification is amplified using arbiters, used as Time Amplifier (TA). Therefore, the resolution is greatly improved. The need for an implementation of TA at each tap is necessary because the time cannot be stored directly in the time domain. This will present a critical issue related to the latency. Moreover, the time amplification cannot handle continuous time intervals, especially if arbiters are used as TA. Unlikely, the analog TAs are able to process continuous events [34]. Unfortunately, this method can yield to more complex systems. Additionally, this technique suffers from the uncertainty due to the local PVT variations, which makes it difficult to operate linearly [34].

Three-level conversion Recently, to gain an enhancement of the time resolution, the interpolation technique has been supported by an additional conversion level. Jin Wu *et. al.* propose a TDC with Three-level scheme implemented in $350\,\mathrm{nm}$ CMOS technology [76]. The first conversion (high-level) is based on counters driven by a stable clock, which ensure the wide range ($25.0\,\mathrm{ns}$). The middle-level (as fine TDC) is a dual DLL (made by primary and secondary DLL), offering a time resolution of $3.125\,\mathrm{ns}$. This resolution is defined by the eight-stage voltage-controlled delay line in the primary DLL. A Vernier implemented by the dual VCO is used as final step providing a sub-gate resolution of $390\,\mathrm{ps}$. Notice that the TDCs implemented on FPGA boards are often designed using this technique of multi-level conversion.

2.5 Conclusion

The first generation of the time-to-digital converters is based on analog techniques. The most known architecture is based on the time stretching technique, which allows benefiting from a fine time resolution. The analog TDCs are more adapted for short time measurements due to the

trade-off between the resolution and the dynamic range. Moreover, this kind of TDCs are sensitive for the temperature drift, which can affect their linearity. In addition, the analog TDCs are difficult to be adapted for a technology shrink. Thus, the digital TDCs, for which the technology shrink can be easily adopted, have been presented later. They are offering simple architectures and sub-gate resolution. Thanks to the digital circuits, a reduction in terms of area and power are obtained. On-the-fly measurements is ensured with simply using the delay lines. In accordance with a wide dynamic range, the delay-line can be looped to make an oscillator and to re-use the delay gates many times. Unfortunately, the resolution of these TDCs is limited by the gate delay. One possible solution to get sub-gate time resolution is to employ the Vernier technique. Despite the simple and fully digital architectures of these TDCs, they cannot combine a sub-gate resolution for on-the-fly measurements and wide time intervals. Advanced techniques trying to combine the advantages of each kind of the above architectures in order to reach better performances have been proposed. They are mainly adopted for dedicated applications. However, their principles often target a time resolution improvement. As example, the Vernier technique has been implemented with two-dimension structure and ring TDC, which benefits from a fine time resolution and a wide dynamic range. On the other hand, the multipath structure allows to propagate several events in a structure of interpolated oscillators. Thus, it can benefit from the time difference of the generated phases. Most of the time, TDC structures required complex calibration schemes and repetitive measurements. Therefore, a fair comparison is difficult since each structure depends on the used technology and the number of stages or gates. Even for advanced TDCs, most of the structures are not able to combine all the desired performances : sub-gate resolution, wide dynamic range, and good linearity. Unfortunately, this is not perfect, especially for the on-the-fly measurements. Fortunately, this thesis gives some trends for solving this issue.

Chapitre 3

Self-Timed Ring Oscillators and Operation Principles

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3.1 Introduction

Oscillators are basic building blocks frequently needed in various applications. They are widely used for clock generation in communication systems, microprocessors and SoCs. In communication systems, a clear trend towards the use of high-speed serial links between RF transceivers and baseband digital signal processing circuits can be seen. This kind of links often requires generating a high frequency clock able to reach high performances in terms of timing jitter and phase noise. High frequency oscillators can be typically implemented using ring structures or LC circuits.

The Inverter Ring Oscillators (IRO) is frequently used as digital oscillators. They offer easy integration within a CMOS technology and they usually often represent a hardware demonstration for new technology. They are widely used as low cost solution for many devices. Their structure is based on a simple concatenation of inverters. This latter is a well-known method to realize Time-to-digital converters (TDCs) structures in the literature. Consequently, this is a fully digital solution to generate a reference clock which can be used to sample the time intervals to be measured. However, the IROs suffer from limitation due to the time resolution which cannot be easily improved. Moreover, an inverter ring is able to maintain and propagate only one electrical transition. Indeed, having several transitions propagating at the same time is very useful for generating multi-phase clocks.

Recently, digital oscillators initially developed for controlling asynchronous circuits have been exploited for different usages such as clock generation, true random number generation and time measurement. The self-timed ring oscillators (STROs) have been deployed in many applications [15, 78] due to their many interesting features. They are indeed a promising solution for time measurement because they make possible to adjust by design the time resolution. Additionally, they allow propagating several electrical transitions in the same structure without colliding since they use a request/acknowledgement protocol. As it can be seen in the sequel, they also own the excellent robustness of the asynchronous circuits to PVT variations.

In this Chapter, a detailed presentation of the STROs is presented. The fundamental principle and basic notions of the asynchronous circuits required for understanding the STROs are firstly presented. Then, the architectural and logical behaviors are developed before presenting the temporal and frequency models that distinguish these oscillators. Further than many listed features of the STROs in this chapter, we present as well our proposition for generating a quadrature phase oscillator based on self-timed ring oscillator. Finally, a study of the phase noise in the STRO is presented.

3.2 Fundamental concepts of asynchronous logic

Sequential circuits are considered as synchronous when a clock signal controls the synchronization, and as asynchronous when a local synchronization is performed between the stages. The main purpose of this Chapter is to introduce the basic principles of asynchronous logic.

3.2.1 Synchronous logic circuits

All the stages of the synchronous circuits are synchronized by a common signal called clock signal, as shown in Fig. 3.1. This clock guarantees the simultaneous evolution of data in all logical blocks. In other words, the edge of the clock signal simultaneously triggers the states of the circuit (outputs of flip-flops), which ensures the data pacing. The structure of the synchronous circuits makes possible to model them as clocked circuits. This model is used by the majority of designers and CAD tools since it is conform to the RTL (register transfer level) specification formalism [59].

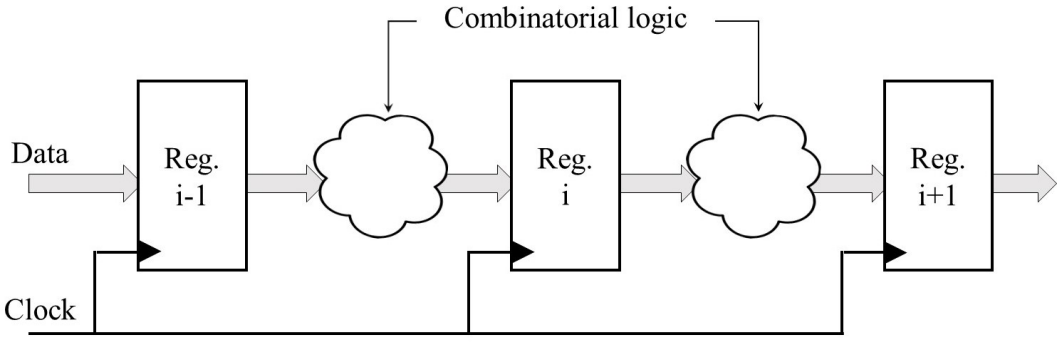

FIGURE 3.1: Digital synchronous circuit : general architecture.

The design of the combinatorial blocks is simple thanks to the synchronous circuit temporal hypothesis. This hypothesis assumes that the clock signal have an enough long period to sample to a stable state the output of all the logic stages. By contrast, this mandatory condition becomes more and more difficult to maintain in the advanced nodes. Indeed, the clock distribution has

to guaranty as much as possible the instantaneity of the sampling operation in order to avoid skew. happened at the same time for all memory blocks. In addition, the clock signal should be enough amplified so that it can be widely distributed for all flip-flops. Thus, using a large number of FFs involves a large area and high power consumption. Due to this global timing, an electromagnetic radiation related to the current absorption is produced. Moreover, the modular integration of the synchronous circuits is a real challenge for designer because it can expand the critical path which will constraint the period of the clock signal.

3.2.2 Asynchronous logic circuits

Differently, the asynchronous circuits are not based on a global and discrete clock signal for their synchronization. The input changes are responsible for changing the state of the circuit. In other words, asynchronous means that there is no prior temporal relation between events and that the synchronization is made locally in a data-driven way. The asynchronous circuits are faster than synchronous circuits because they do not have to wait for a clock pulse to trigger their outputs. Therefore, the stages illustrated in Fig. 3.2 can be simply composed by combinatorial logic and memory gates implementing the functions while the synchronization is ensured by handshake signals (Request / Acknowledgment). For the digital design, the asynchronous circuits are a suitable candidate since they combine the advantages of a better modularity, a low power consumption and lower electromagnetic interferences.

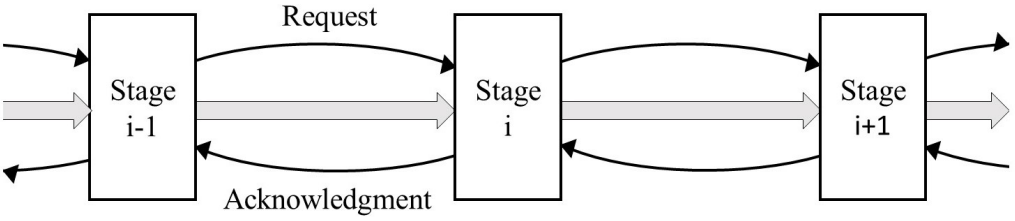

FIGURE 3.2: Digital asynchronous circuit : general architecture.

Since the synchronous circuits have to respect a minimal execution time corresponding to a global timing constraint, this is no longer the case for the asynchronous circuits. The asynchronous blocks are controlled and activated by the presence of data at their inputs so that the data transfer is locally managed.

As illustrated in Fig. 3.2, the directly connected stages independently exchange data from the others so that they can ensure a local synchronization. Every time a stage i wants to communicate with stage $i + 1$, this latter should acknowledge the communication before starting any new action from stage i. Thanks to the handshake , each synchronization is locally made.

Theoretically, the asynchronous circuits are faster compared to the synchronous ones be-

cause some of them have no timing assumption. Indeed, we don't need to consider timing margins at design time.

The asynchronous circuits can be classified as one of the following circuit classes : Huffman circuit, Speed Independent circuit (SI), Quasi-Delay-Insensitive circuit (QDI), Delta Insensitive (DI), or Micropipeline. In our case, the micropipeline circuits are used. They are based on a two-phase protocol and a bundled-data encoding. Therefore, only these concepts will be developed in the sequel.

3.2.3 Handshake protocols

Two handshake protocols are used for the asynchronous digital logic : two-phase handshake and four-phase handshake protocols. They are classified according to the number of steps involved in one communication cycle. Any action from the sender or the receiver should be acknowledged in order to ensure the synchronization.

3.2.3.1 Two-phase handshake protocol

In the two-phase protocol, also called half-handshake protocol, a communication is count for any wire transition. This means that the rising and the falling edges have the same authority. This protocol can be used for communication. It is considered as faster. As presented in Fig. 3.3, the transition from 0 to 1 count as first communication (datum n-1) and the transition from 1 to 0 count as second communication (datum n).

The sender, the stage i of Fig. 3.2, drives the request wire and sends an event when the data are valid, while the receiver (stage $i + 1$) drives the acknowledgement signal and transmits an event if the data have been used [65]. Therefore, the operating principle is managed in two steps :

— **Step1 (phase1)** :the receiver detects the request, starts a data processing, and indicates to the sender that it is able to process new requests by generating the acknowledgement.
— **Step2 (phase2)** : the sender detects the acknowledgment signal and starts sending new data if they are ready.

3.2.3.2 Four-phase handshake protocol

With the two-phase protocol, the implementation have to consider double-edge design in order to count both rising and falling edge of signals. However, for the four-phase protocol shown in Fig. 3.4, the communication considers the logic levels instead of the transitions. An invalid state separates the data validity and acknowledgment so that the signal returns to its original state at the end of each communication. Therefore this protocol is called full-handshake protocol. One consequence is that this protocol requires more transitions than the 2-phase protocol.

Indeed, a data transaction needs to complete four transitions :

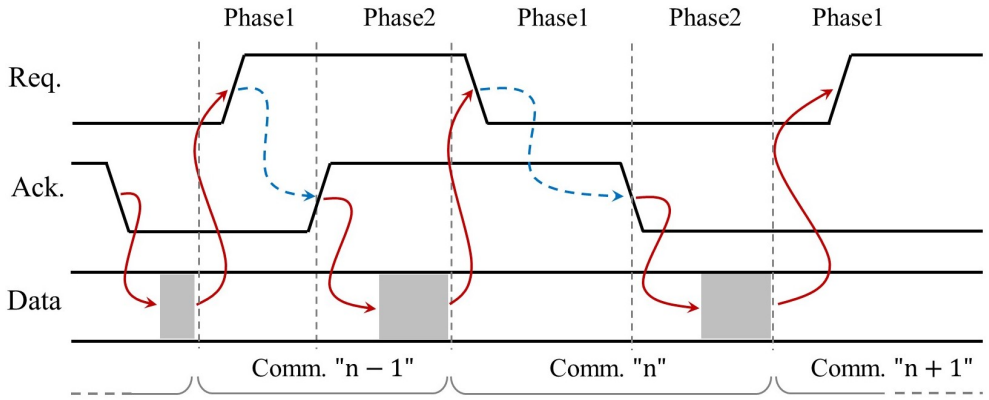

FIGURE 3.3: Two-phase protocol diagram.

— **Step1 (phase1)** : similar to step 1 of two-phase protocol.
— **Step2 (phase2)** : the sender detects the acknowledgment and resets the request (invalid data).
— **Step3 (phase3)** : since the request signal is logic low, the receiver rests the acknowledgment signal.
— **Step4 (phase4)** : the sender detects the acknowledgment rest.Thus, a new transaction can start.

Even though this protocol requires more transitions, but it is simple for implementation (more used for QDI type) and can be used for computation.

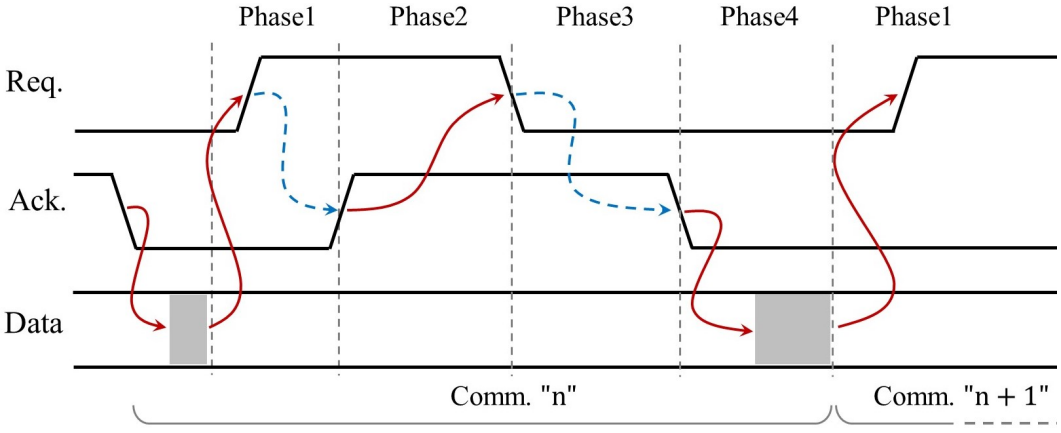

FIGURE 3.4: Four-phase protocol diagram.

3.2.4 Asynchronous data encoding

In the synchronous logic, the coding of data is implicit. However, the asynchronous logic requires embedding the data and the request signals. Depending on the protocol (2-phase or 4-

phase), we present two encoding that matches each of these protocols. As an example, we give a possible encoding based on dual-rails. The approach can of course be extended to multi-rails.

The dual-rail encoding is combining data and request signals. In practice, a wire represents the bit value '1' and the other one the bit '0'. This encoding is used with delay insensitive circuits. Usually, two dual-rail encoding types are commonly used :

— **Three-state encoding**

Three-state encoding has two valid states (10 and 01), and an invalid state corresponding to 00, as displayed in Fig. 3.5. The state 11 is not allowed. This encoding is mostly used with the four-phase protocol since the transition from one valid state to another involves going through an invalid state. This corresponds to a Return-to-Zero (RZ) protocol.

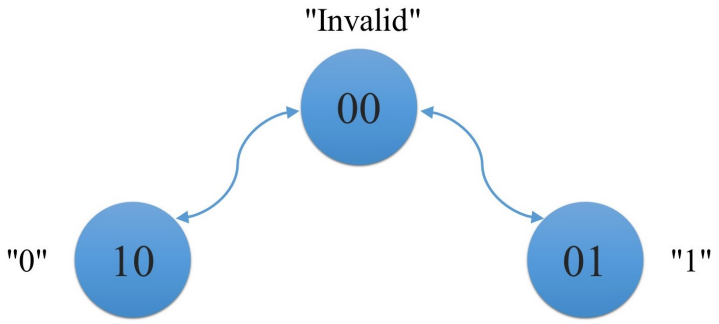

FIGURE 3.5: Three-state encoding.

— **Four-state encoding**

This encoding is also called Non-Return-to-Zero (NRZ). Unlike the previous type, the transition from a data to another does not require to transit through an invalid state. Every data transition involves a new data transaction, as shown in Fig. 3.6. This encoding is employed with the two-phase protocol.

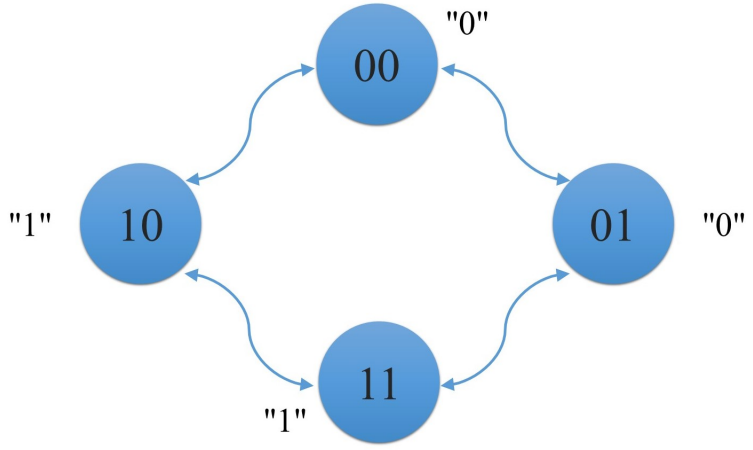

FIGURE 3.6: Four-state encoding.

3.2.5 Micropipeline

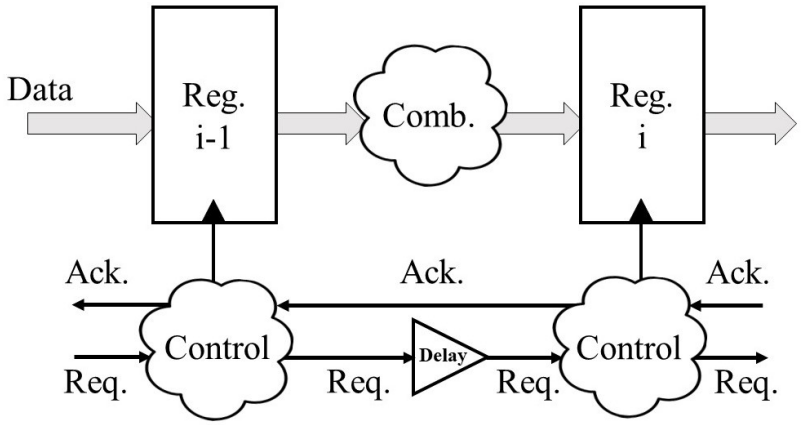

FIGURE 3.7: General structure of Micropipeline circuit.

The micropipeline technique has been initially introduced by I. E. Sutherland [65]. Micropipelines are known to be a type of the FIFO (First In First Out) control circuit based on two-phase handshake protocol. A general architecture of this circuit is presented in Fig. 3.7. In this figure, we notice that registers are controlled by local signals which represent the request signals. These signals are crossing the delay unit simultaneously with data propagation. The data sampling correctness is ensured by choosing a delay greater than the maximal data processing time.

The micropipeline structure is similar to the synchronous circuits, but the synchronization is made locally thanks to the control path (control blocks + delays), which replaces the clock tree. The circuit reacts to the signal transitions neither than states. It makes that successive operations are controlled by data tokens (notion defined in the next section). Then, the request signal propagates in the structure until it encounters an occupied stage.

3.2.6 Basic element : Muller gate (C-element)

Specific cells are needed to ensure the synchronization between signals used by the asynchronous logic. The request and acknowledgement signals have to be synchronized in order to guaranty a correct data transfer between registers and avoid data overwriting. This can be done by implementing a *rendez-vous* function in the controller. This function can be implemented with standard logic gates but at the price of a significant area overhead and speed loss. Therefore, a transistor level implementation of the function is more appropriate. This implementation is known under the names C-element or Muller gate. This Muller gate allows to drastically limit the area overhead and to improve the speed.

Fig. 3.8a and Fig. 3.8b show the symbol and truth table of a 2-input C-element. This specific gate is somehow a state-holding element as it can be noticed from its truth table. The output C is set to 0 when both inputs A and B are 0, and is set to 1 when both inputs are 1. Otherwise, it holds its output as memory of the last value. As a result, when the output C transits from 0 to 1 (or from 1 to 0), this confirms that both inputs have the same value 1 (or 0). The C-element is characterized by its forward static propagation delay D_{ff} and its reverse static propagation delay D_{rr}.

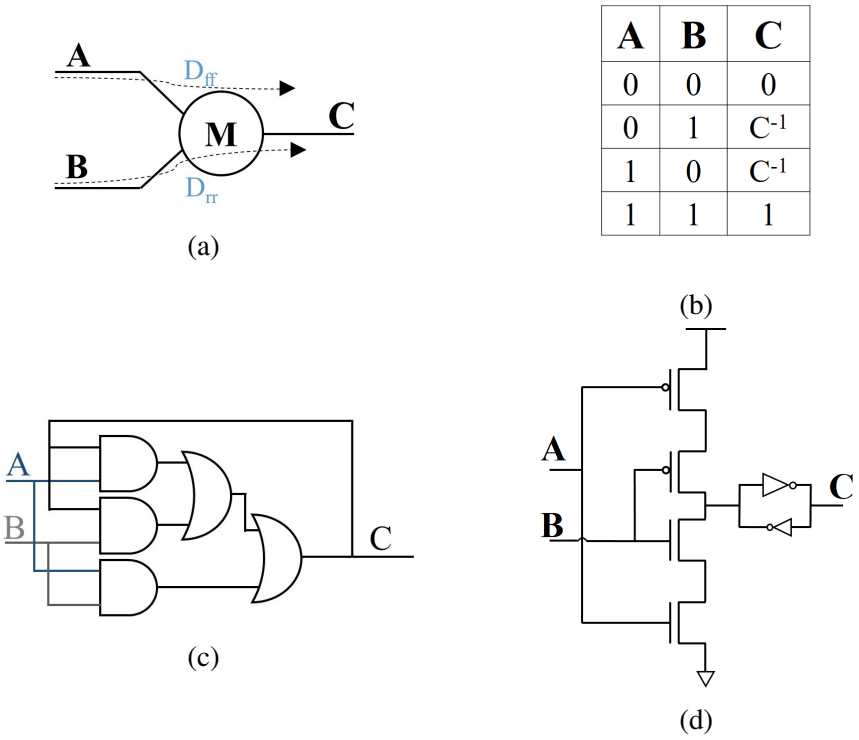

FIGURE 3.8: (a) the C-element symbol, (b) truth table of a C-element, (c) C-element implementation with standard digital gates, (d) transistor implementation of the C-element.

Usually, Design Kit (DK) libraries do not provide asynchronous standard cells such as the C-element. However, an implementation using simple combinatorial gates is possible since the output C is computed by the following equation :

$$C = A \cdot B + A \cdot C^{-1} + B \cdot C^{-1} \tag{3.1}$$

An example of a simple implementation of this gate is presented in Fig. 3.8c. Alternatively, another possible implementation can be obtained with a 3-input Majority gate (MAJ) where the output is fed back to one input.

Otherwise, a full custom version can be further used in order to optimize the gate performances. Different static implementations are possible as proposed in the literature and differ from their transistor sizing and structure. Globally, they share the structure of the dynamic C-

element (as shown on Fig. 3.8d) but the static latch is implemented differently. Extra inputs such as *Set* and *Reset* signals are frequently required for initializing the Muller gate.

The C-element implementation is typically made by two PMOS transistors and two NMOS transistors in series. It serves as a basis for several C-element structures. Additionally to this part, as it can be seen in Fig. 3.8d, two transistors are added to the dynamic implementation in order to maintain the state if inputs are different. The structure is (the two inverters) called keeper. The inverter used in the feedback loop is generally sized with smaller transistors in order to limit the feedback current. In practice this is a trade-off between the memory stability and its speed / power consumption. The weak-feedback structure, proposed by A. J. Martin [49] presented in Fig. 3.9a, looks like the dynamic structure with this additional feedback inverter maintaining the output state when inputs are different. It may cause a contention limiting the commutation. In order to overcome this problem, the conventional implementation was proposed by [65]. Four additional transistors have been added to the previous structure in order to switch off the feedback inverter when inputs show the same level. This architecture is shown in Fig. 3.9b. Another different implementation of the C-element is the symmetric illustrated in Fig. 3.9c. This type was introduced by Van Berkel in which the main transistor branch is duplicated and two other transistors are added. There are other types of C-element such the differential implementation as seen in Fig. 3.9d as example.

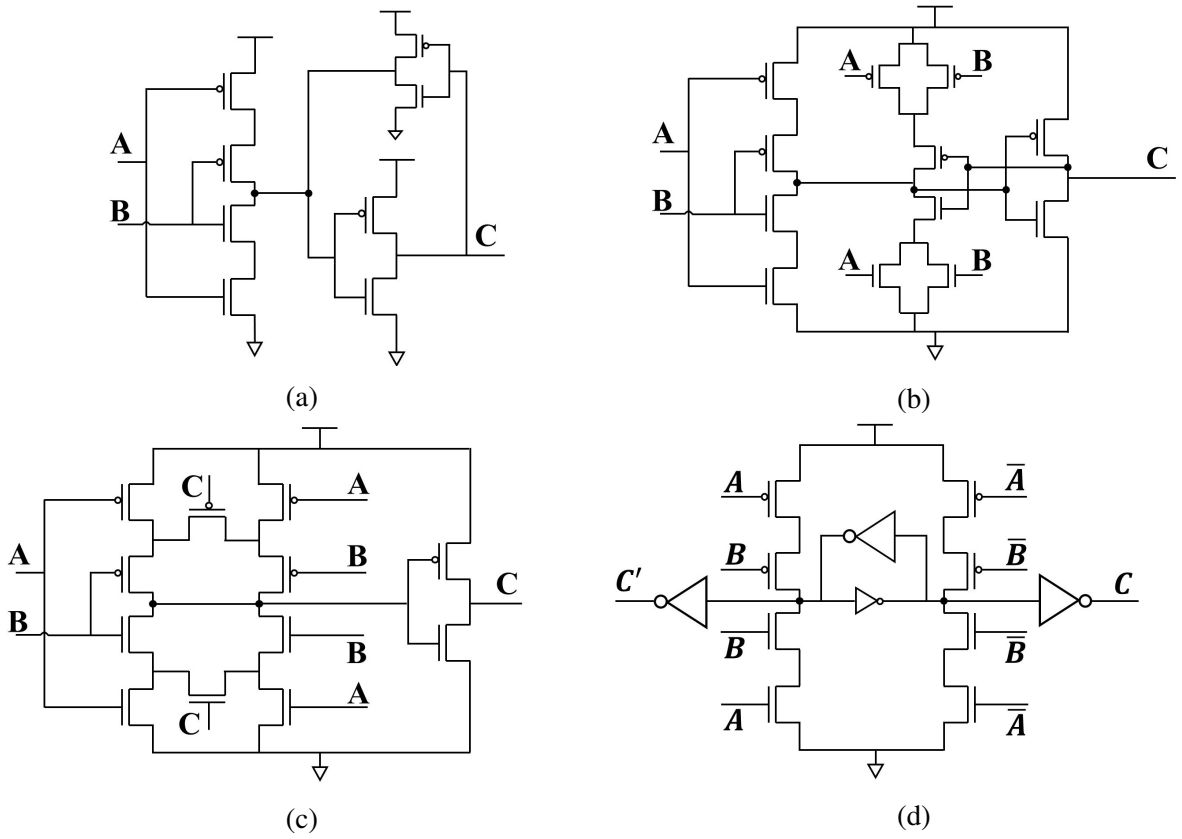

FIGURE 3.9: C-element implementations : (a) week-feedback, (b) conventional, (c) symmetric, (d) differential.

Finally, another possibility of implementation is the *analog C-element*. In fact, this implementation can be simplified and viewed as a standard cell implementation as shown in Fig. 3.10. The name comes from its output voltage, which is expected to take on a range of values and its inputs sense this same range of values [26]. The illustration can be made by standard gates but the operating function needs the analog effects. The gate architecture is simply made by inverters in addition to NANDs used for the initialization (the *Set* and *Reset* inputs). The *Set* and *Reset* signals are active low. In fact, the output C_i is forced to zero (resp. one) if the *Reset* signal goes to zero (resp. if the *Set* signal goes to zero). When the *Set* and *Reset* inputs are set to one, the output C_i in this case is defined according to the values presented by the tri-state inverters. Regarding the *Init* signal, it is used to enable and disable the tri-state inverters. The analog C-element implementation is completely symmetric, which ensure approximately the same delays D_{ff} and D_{rr} ($D_{\text{ff}} \approx D_{\text{rr}}$). This implementation is more stable to variations than any other structure of C-elements [27].

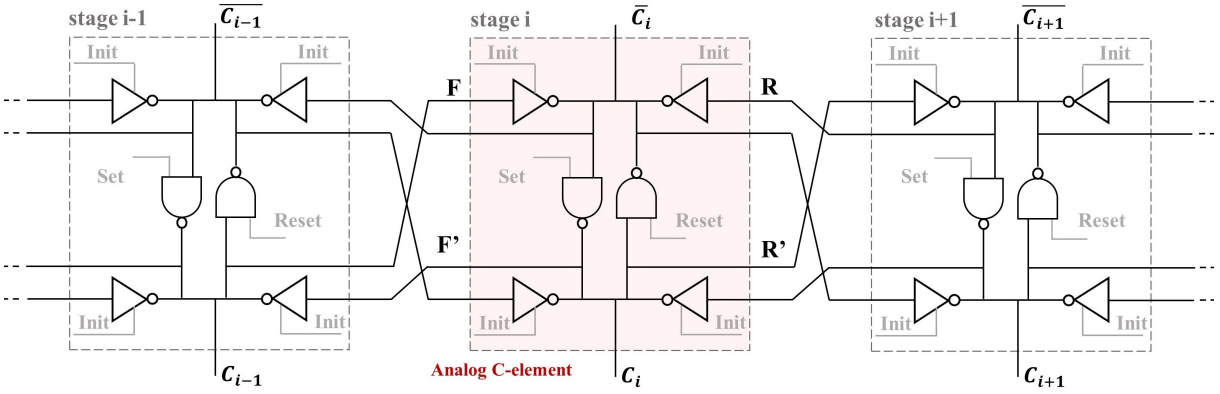

FIGURE 3.10: *Analog C-element* structure.

3.2.6.1 Charlie effect

C. E. Molnar and T. J. Chaney [8] first highlighted an electrical phenomenon leading to evenly-spacing the events in the ring. They explained the origin of the phenomenon as follows. The switching of the PMOS and NMOS transistors, used for the memory function, are at the origin of the Charlie effect. It is somehow the result of the memory effect of the C-element gate. This is due to the fact that the gate output have to switch for a while to a memory state before establishing the final logic value when the inputs have both transit with a short time space. To put it more simple, we consider the simplest C-element implementation of Fig. 3.8d. If we suppose that the output presents a transition from 0 to 1 (or inversely), this means that both inputs transit as well. Assume that events from A and B are sufficiently spaced in time, and that B arrives first, the arrival of the event from B makes the circuit ready for a possible transition on its output. As a result, the time of a transition from on the output C only depends on the

switching time of transistors controlled by the input A and by the memory circuit. Conversely, when the event from A becomes closer to that of B, it does not give enough time to the circuit to be stabilized. Thus, the transition of the output C makes more time. Consequently, we can express the Charlie effect as : *The closer are events at the input of the C-element, the longer is its propagation delay [32].*

3.2.6.2 Drafting effect

The Drafting effect is a phenomenon known for all logic gates. It concerns the gate output switching capability. Indeed, if the output switches too fast, it does not have enough time to reach *VDD* or *GND* before a new switching. As a result, this will lead to a short propagation delay. Consequently, this effect impacts as well the stage propagation delay when the output present two successive commutations.

In other words : *the shorter is the time between two successive commutations of the output C of the C-element, the shorter is its propagation delay.*

3.3 Architectural and logical bvehavior

3.3.1 Self-timed ring oscillator structure

The self-timed ring oscillator (STRO) is basically a control circuit of micropipelines that is looped back to form a ring, as proposed by [65]. As depicted in Fig. 3.11, the STRO stage is mainly made by a C-element gate in which one input is inverted. Each stage has two inputs, one F_i is forwarded from the output of the previous stage C_{i-1} and the other one R_i is connected to the output of the next stage C_{i+1}. Each stage has a forward (resp. backward) static propagation delay D_{ff} (resp. reverse static propagation delay D_{rr}), which corresponds to the delay for an event to propagate from F_i to C_i (resp. R_i to C_i). The connection between these stages makes the global STRO architecture, as depicted in Fig. 3.11 in which a number L of stages are connected.

Stages communicate data in two phases using event logic. An event is corresponding to a voltage transition. Therefore, an event on the input F_i of the stage i corresponds to a request from stage $i-1$ and the event from input R_i corresponds to the acknowledgment from stage $i+1$. The event from output C_i requests the next stage $i+1$ and acknowledges at the same time the previous stage $i-1$. As a result, several events can propagate simultaneously without colliding thanks to the request/acknowledgment protocol (two-phase handshake protocol). The number of events is set at the ring initialization, and stays invariant thanks to this handshake protocol. This step is very important for the oscillator because it conditions the ring propagation mode as mentioned in the sequel.

Fig. 3.12b shows an example of a 5-stage STRO with two propagating events. The two events propagate without colliding thanks to the request/handshake protocol. The events propa-

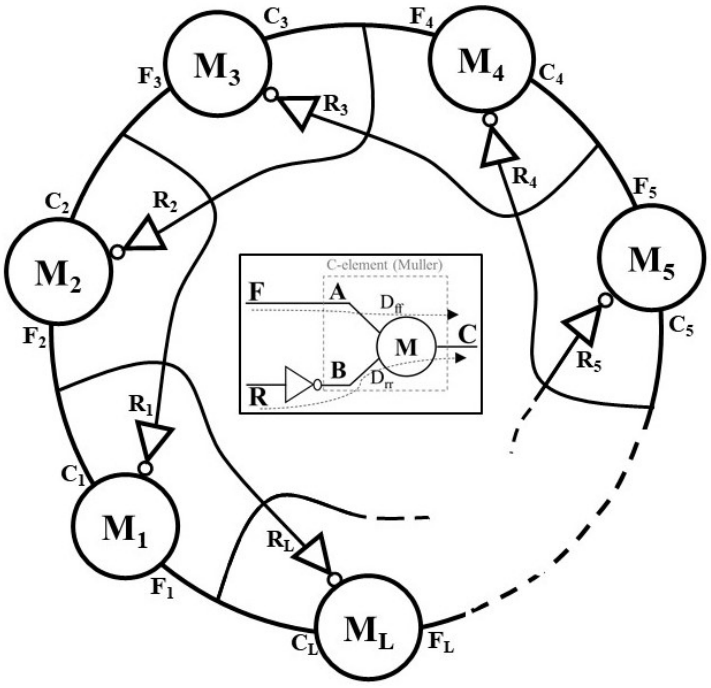

FIGURE 3.11: Global architecture of a L-stage STRO oscillator.

gate from a stage to another with a time spacing STR_{gate_delay}. The possibility of propagating several events in the same structure allows exploiting the resulted phase distribution as it can be seen later. Unlike, in the case of the inverter ring oscillator as presented in the previous chapter, multiple events can be initiated into this circuit but they end up colliding. Finally, only one event can propagate for ever in this kind of ring. Thus, only one event can propagate as shown in Fig. 3.12a in the IROs, unlike the case of the STRO.

3.3.2 Tokens and Bubbles abstraction

The STRO logical behavior can be described and modeled like a token game [32]. This is not a physical element but an abstraction that can facilitate the representation of the data circulating in the ring. A ring stage i contains a token if its output C_i differs from the output of the next stage C_{i+1} ($C_i \neq C_{i+1}$), and it contains a bubble if these two outputs are the same ($C_i = C_{i+1}$). So, a stage that contains a token means that it has a datum, while if it contains a bubble this indicates that it is free and ready to get a datum. As a result, a token propagates to the next stage if and only if it contains a bubble. In this case, the bubble propagates in the opposite direction and replaces the token, which had freed its place. As an example, in Fig. 3.13a, the stage M_2 contains a token since its output is 1 and the output of the stage M_3 is 0. This token is propagating to the stage M_3 because this latter contains a bubble. The same process is available for all the tokens in the ring, and the final state at a time $t + 1$ is illustrated in Fig. 3.13b.

Turning to the propagation process, we need to enumerate some rules. So, we denote N_{T}

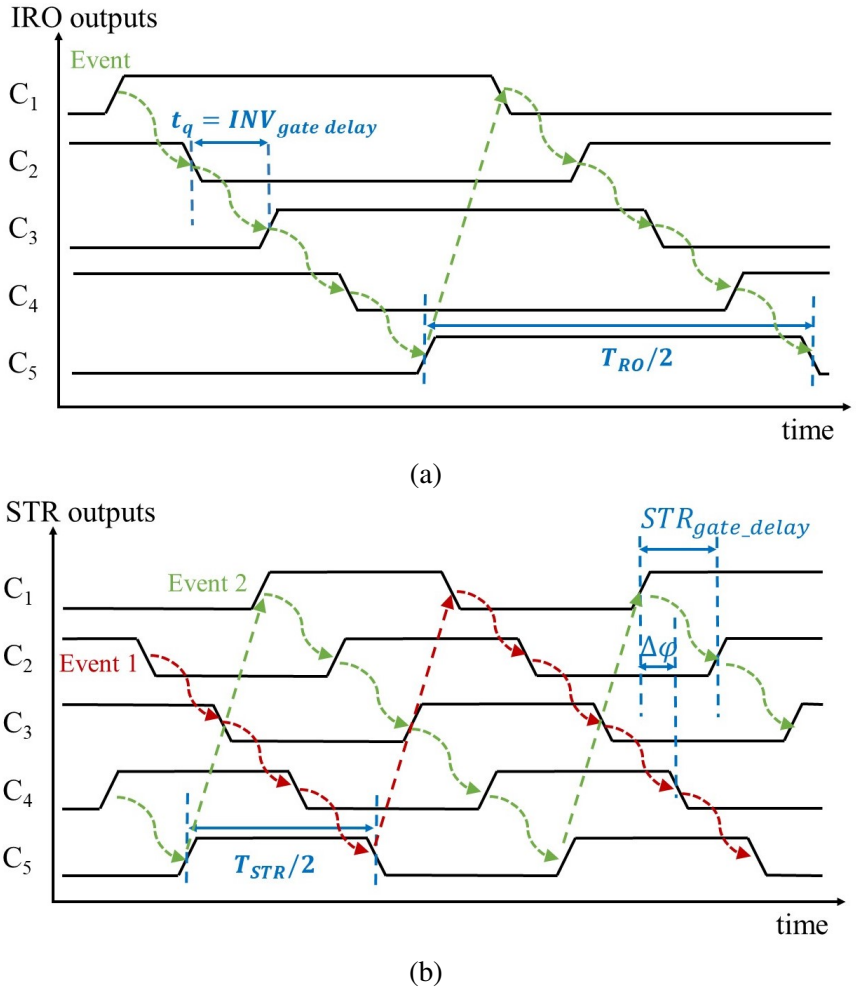

FIGURE 3.12: 5-stages (a) IRO versus (b) STRO phases diagram showing events propagation in time (example of two events propagation in the 5-stages STRO).

and N_{B}, respectively the number of tokens and bubbles in the ring, and L, the total number of the STRO stages. Firstly, each stage in the ring should contain a bubble or a token ($L = N_{\mathrm{T}} + N_{\mathrm{B}}$). Secondly, in order to ensure the propagation of events, at least one bubble should be included, so : $N_{\mathrm{B}} \geq 1$. The number of tokens should be even ($N_{\mathrm{T}} \geq 2$) because the tokens are defined according to the state of two adjacent stages and the structure is looped. This means, that according to the previous rule, the minimum number of the STRO stages is 3 ($L \geq 3$). In other words, the tokens propagate in the ring as long as there is at least one bubble and an even number of tokens in the ring.

Conventionally, in the tokens limited region in which the number of tokens is greater than the number of bubbles ($N_{\mathrm{T}} \geq N_{\mathrm{B}}$), the events are represented by the tokens. Conversely, in the bubble limited region in which the number of bubbles is greater than the number of tokens ($N_{\mathrm{B}} \geq N_{\mathrm{T}}$), the events are represented by the bubbles, as it can be seen in Fig. 3.18. To make it simple, we can consider that events correspond to tokens in the ring for our study. The propagation process can be described by a state graph representing all the intermediate event transitions.

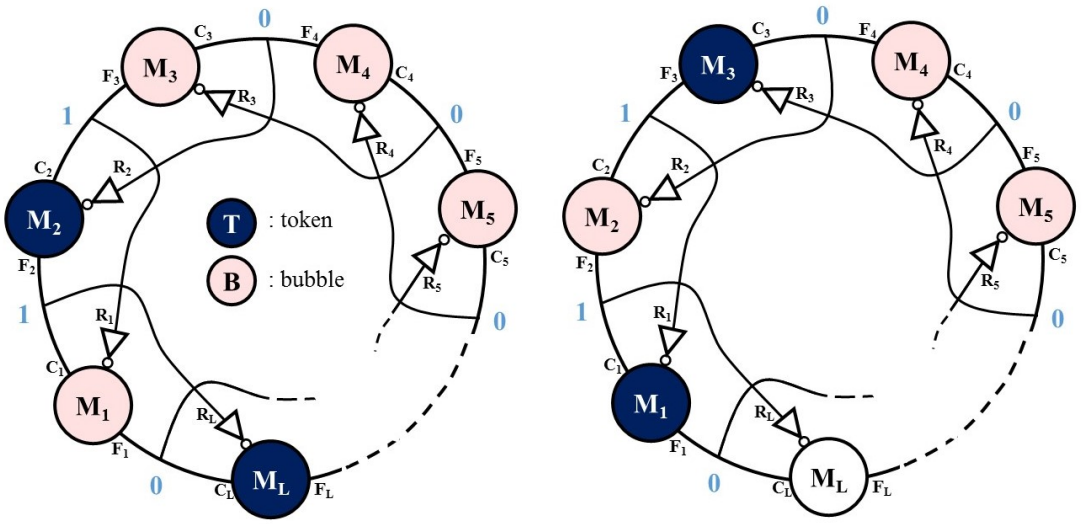

FIGURE 3.13: Tokens and bubbles propagation example : (a) a L-stage STRO state at time t, (b) the next state at time t+1.

We can also present this by sequences or vectors as explained in [32].

3.4 Temporal behavior

3.4.1 Propagation modes

Independently of the initial position of events in the ring, the STRO eventually reaches one of the following two steady states : events are either spread-up around the ring and propagate with a constant time difference (evenly-spaced oscillation mode), or they gather together and propagate as bursts (burst oscillation mode). The two modes are presented in Fig. 3.14. Generally, these steady states are related to the number of stages and the number of events in the STRO.

The initial position of tokens in this structure only influences the duration of the transient regime before the events re-arranged themselves following two propagating modes. The evenly-spaced mode corresponds to a constant separation time between the tokens and is often reached for a number of tokens around half the number of stages. The second mode, called burst mode, shows a bundled propagation of the tokens in the ring.

The oscillation mode in the steady state not only depends on the temporal parameters of the ring, *i.e.* the forward and reverse propagation delays, but also on the ring occupancy and on the strength of two analog phenomena related to the C-element gate, the Charlie and Drafting effects [26]. In the evenly-spaced oscillation mode, events propagate in the ring with a uniform time spacing. This unique behavior is due to the Charlie effect : *the closer are events at the inputs of a Muller gate, the longer is its propagation delay* [31]. Considering the adjacent stages of

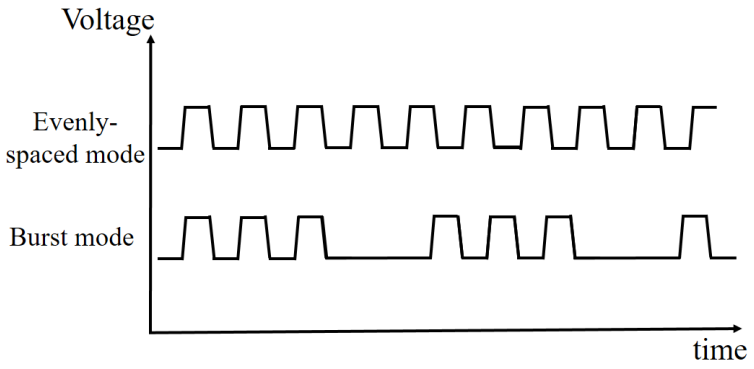

FIGURE 3.14: Propagation modes of a STRO in its steady state.

Fig. 3.13 $\{M_L, M_1, M_2\}$, M_1 is slowing down the event coming from stage M_L considering that stage M_2 has an event as well if the tokens coming from M_L and M_2 are too close. Accordingly, events in the STRO mutually push away from each other in time as they propagate in the ring. For a certain range of occupancies, this effect leads to a uniform distribution of the event timings at the ring outputs [26].

As presented before, the Drafting effect influences as well the STRO stage propagation delay when the output present two successive transitions. The event propagation is affected by this effect since it pushes events to bunch [26]. A STRO stage, which has achieved a propagation of a first event, is able to faster propagate a second event if it is enough close to the previous token. Therefore, the decreased delay results in the distance between the events (mutually closer). Consequently, the burst propagation mode is obtained in the STRO, especially if the ring presents a low number of events and a high Drafting effect.

3.4.2 Charlie and Drafting diagrams

The study of the STRO needs to establish a timing representation taking into account the Charlie and Drafting effects. The timing diagram of the stage M_i is presented in Fig. 3.15. In this figure, we define the following parameters :

— s is the half separation time between the inputs of the C-element (F and R) :

$$s = \frac{t_F - t_R}{2} \tag{3.2}$$

— y is the time between the previous output commutation and the mean input time :

$$y = \frac{t_F + t_R}{2} - t_C(i-1) = t_{mean}(i) - t_C(i-1) \tag{3.3}$$

— While D_{ff} represents the delay of the event propagating from F to C when F switches enough far from any R transitions (no Charlie effect), D_f is the direct propagation delay in the classic mode. Similarly, D_r is the reverse propagation delay in this mode.

— The variation due to the Charlie effect is represented by the following parameter which

is a function of s and y :

$$Charlie(s,y) = t_C(i) - t_{mean}(i) = t_C(i) - \frac{t_F - t_R}{2} \tag{3.4}$$

This parameter represents the time from the mean value of the event arrival time to the gate propagation time. The definition of this function requires a first study when y is fixed and s is variable. Then, the function is evaluated when s is fixed and y is variable.

Ebergen *et. al.* [20] presented the Charlie plots as a tool in order to demonstrate how data tokens distribute themselves throughout the micropipeline. Then, Winstanley *et. al.* [72] proposed an analytic model of this expression taking into account many other parameters as described in (3.7). Fig. 3.16 plotted the Charlie effect diagram in the case of y fixed. The x-axis displays the separation time s and the y-axis presents the delay as measured from this point. It proves that the delay $Charlie(s,y)$ is continuous with the parameter s. The plot is guided by two asymptotes : $s = D_{\text{rr}} - s$ when bubbles are majority and $s = D_{\text{ff}} - s$ when tokens are majority.

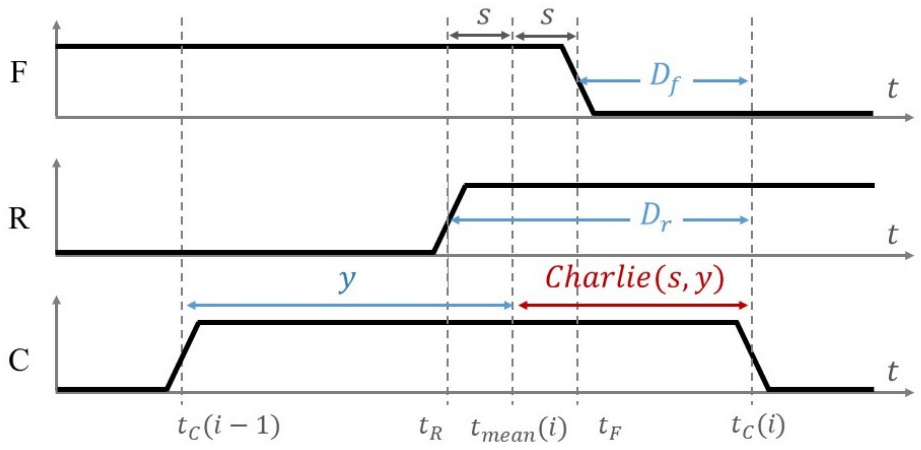

FIGURE 3.15: Timing diagram example of a STRO stage.

Noticeably, the maximum delay is obtained for a minimum time separation ($s = s_{min}$), which represents the maximum influence of the Charlie effect. D_{Charlie} is reflecting the magnitude of the Charlie effect in this extreme case.

$$Charlie(s) = \frac{D_{\text{ff}} + D_{\text{rr}}}{2} + \sqrt{{D_{\text{Charlie}}}^2 + (s - \frac{D_{\text{ff}} - D_{\text{rr}}}{2})^2} \tag{3.5}$$

By fixing the s parameter, the delay is expressed with an exponential model, which is a representation of the Drafting effect as presented by the following expression :

$$Charlie(y) = D_{\text{Drafting}} \cdot e^{-\frac{y}{t_{\text{Drafting}}}} \tag{3.6}$$

where D_{Drafting} is the Drafting effect amplitude which is a temporal parameter; and t_{Drafting} is the Drafting effect duration. The corresponding plot of this expression is presented in Fig. 3.17.

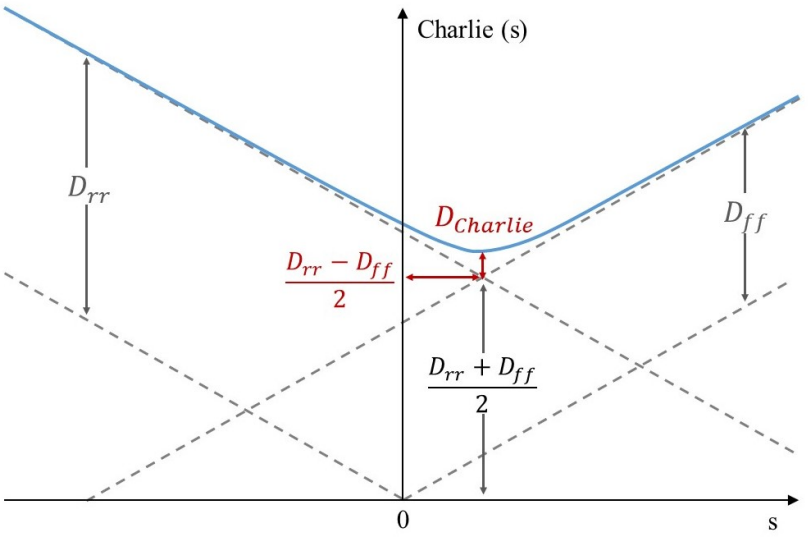

FIGURE 3.16: 2D Charlie diagram.

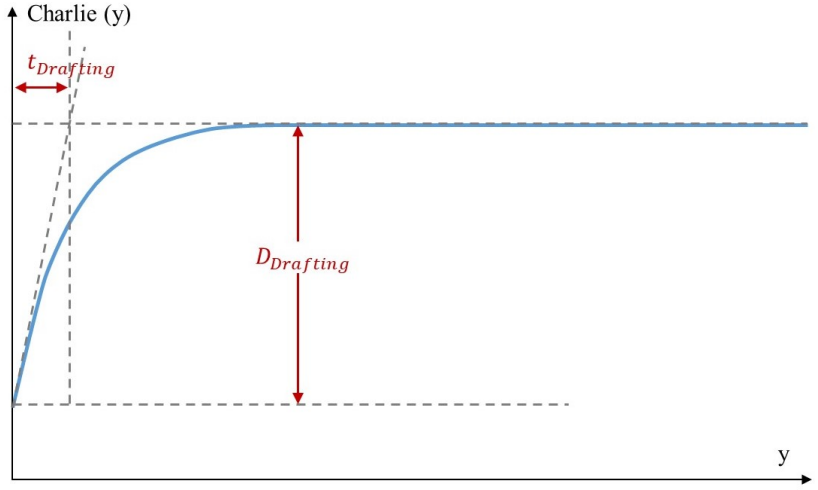

FIGURE 3.17: Drafting diagram.

The 3D Charlie diagram is a three dimension plot that merges the two studies of the $Charlie(s, y)$ formula. This model is important for the STRO study since it helps to optimize the ring at its maximum operating point. The final expression is done by :

$$Charlie(s,y) = \frac{D_{\text{ff}} + D_{\text{rr}}}{2} + \sqrt{{D_{\text{Charlie}}}^2 + (s - \frac{D_{\text{ff}} - D_{\text{rr}}}{2})^2} - D_{\text{Drafting}} \cdot e^{-\frac{y}{t_{\text{Drafting}}}} \quad (3.7)$$

Getting the appropriate value of this expression, the instantaneous transition time of the stages can be deduced using (3.4).

3.5 Frequency model

In this section, we propose to investigate the oscillation frequency given by the STRO since it represents a valuable parameter for all oscillators. For this purpose, we need to define the ring occupancy Γ as a first step. Then, we give a global estimation of the frequency typically presented by the frequency curve. Finally, we suggest a recursive formula of the oscillation period as a function of the Charlie effect.

3.5.1 Occupancy Ratio

The occupancy ratio is defined as the ratio number of events N over number of stages L, in which as highlighted before, the events can be tokens or bubbles according to the operating mode of the ring. :

$$\Gamma = \frac{N}{L} \tag{3.8}$$

The ring is operating in its tokens limited region (tokens are majority) in the case of $s \leq \frac{D_{\text{ff}} - D_{\text{rr}}}{2}$ which is equivalent to : $\Gamma/(1-\Gamma) \leq D_{\text{ff}}/D_{\text{rr}}$.

Inversely, the ring is bubble limited when $s \geq \frac{D_{\text{ff}} - D_{\text{rr}}}{2}$ which is equivalent to : $\Gamma/(1-\Gamma) \geq D_{\text{ff}}/D_{\text{rr}}$. In the sequel, we can admit that tokens are representing events in the STRO in order to simplify the study.

3.5.2 Frequency curve

The frequency of the STRO does not directly depend on its number of stages but rather on its ring occupancy Γ. The oscillation period, which is the inverse of the frequency, represents the time between two successive events propagating in a STRO stage (the ring is supposed to be in the evenly-spaced mode).

Fig. 3.18 shows a typical curve of the frequency of a STRO as a function of its occupancy, which looks like a reverse parabolic curve [5, 15, 21, 24]. The STRO oscillation frequency can be estimated by the two asymptotes denoted F_{TL} and F_{BL} in Fig. 3.18.

$F_{\text{TL}} = \frac{\Gamma}{2D_{\text{ff}}}$ when the ring operates in the token limited region, *i.e.* when $\Gamma/(1-\Gamma) \leq D_{\text{ff}}/D_{\text{rr}}$.

$F_{\text{BL}} = \frac{(1-\Gamma)}{2D_{\text{rr}}}$ when the ring operates in the bubble limited region, *i.e.* when $\Gamma/(1-\Gamma) \geq D_{\text{ff}}/D_{\text{rr}}$ [78].

As it can be noticed, the frequency increases with the number of events, and then starts dropping when the number of free stages becomes lower than the number of events with regards to the static propagation delays. The slight decline at the maximum point of the frequency curve is due to the Charlie effect that extends the gate propagation delays at its maximum [26, 32].

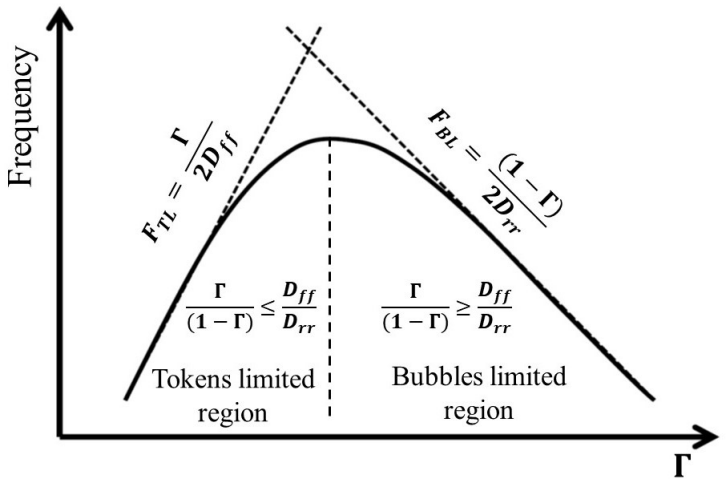

FIGURE 3.18: Frequency curve of a STRO as a function of its occupancy.

The maximum frequency is achieved when [31] :

$$\Gamma \approx \frac{D_{\mathrm{ff}}}{D_{\mathrm{ff}} + D_{\mathrm{rr}}} \tag{3.9}$$

The evenly-spaced mode is automatically achieved for occupancy ranges around Γ which satisfies (3.9). The higher is the Charlie effect, the wider can be the range of occupancy.

3.5.3 Oscillation frequency estimation

The oscillation period is determined by studying the behavioral model of the asynchronous ring which provides at the same time the frequency. A model including the STRO temporal behavior based on state graphs has been proposed in [31]. This model takes into account the two propagation modes of the ring and identifies a temporal annotation for the transitions representing the ring states. Based on analytic functions and simulation results, J. Hamon [30] proposes a recursive formula to express the oscillation period T_{STR} of a STRO. This formula is given as a function of the Charlie function :

$$T_{\mathrm{STR}} = 4 \times Charlie(\frac{(N_B - N_T)T_{\mathrm{STR}}}{4L}, \frac{T_{\mathrm{STR}}}{4}) \tag{3.10}$$

Usually, the period can be differently approximated by considering various factors. This period is nearly equal to $\frac{2D_{\mathrm{ff}}}{\Gamma}$ in the tokens limited region and equal to $\frac{2D_{\mathrm{rr}}}{(1-\Gamma)}$ in the bubbles limited region. Moreover, the minimum achievable period of a STRO is :

$$T_{\mathrm{STR}min} = 2 \times (D_{\mathrm{ff}} + D_{\mathrm{rr}}) \tag{3.11}$$

3.6 STRO Phase distribution

Multi-phase oscillators running at high frequency are often required in many applications such as communication systems. IROs are commonly used for this purpose. With IROs, if several phases are generated, an equivalent number of stages is required for the implementation. Unfortunately, this influences the oscillator frequency and may lead to an important frequency drop. This makes difficult with such an approach to implement a high frequency oscillator with a large number of phases. Moreover, the time resolution is limited by the inverter delays. As shown in Fig. 3.12a, we see that just one event is able to propagate in the IRO with this inverter delay. In other word, the minimal time resolution of the IRO is : $t_q = \mathrm{INV}_{\mathrm{gatedelay}}$. The inverter propagation delay $\mathrm{INV}_{\mathrm{gatedelay}}$ is mainly constrained by the CMOS technology. So the cascaded structure of IROs makes that the stage transitions are spaced by a time multiple of t_q. Consequently, the resulted oscillation period is expressed as follow :

$$T_{\mathrm{inv}} = 2L \times t_q \tag{3.12}$$

L represents the stages number and the number of equidistant phases in this case. According to (3.12), increasing the number of phases induces at the same time decreasing the frequency. Many techniques have been developed to improve the resolution while maintaining a high oscillation frequency [63].

Contrarily, the STRO provides a multi-phase structure allowing a simultaneous propagation of several events without colliding. In addition, the frequency does not depend on the number of stages L but rather on the occupancy ratio. As a consequence, there is no direct relation between the frequency and the number of phases.

In addition, one major consequence of the evenly-spaced oscillation mode is that the STRO provides uniformly distributed events on their output stages. This is noticeable because the minimal phase distance can be shorter than a stage delay if the number of stages is large enough. Therefore, sub-gate delay resolution is achievable with STROs. An example of a 5-stage STRO with two events uniformly propagating is displayed in Fig. 3.12b. In this example, we can notice that the phase resolution $\Delta\varphi$ is a fraction of the stage propagation delay $\mathrm{STR}_{\mathrm{gatedelay}}$ since more than one event is propagating in the ring.

In practice, a STRO is able to exhibit as many different equidistant phases as its number of stages L if the number of events and the number of stages are co-prime [26]. Therefore, the time-resolution is given by :

$$\Delta\varphi = \frac{T_{\mathrm{STR}}}{2L} \tag{3.13}$$

Otherwise, if the number of stages is not co-prime with the number of events, several stages may display the same phase in the STRO. In practice, a factor G, which represents the greatest common divisor of N and L, is used to generalize the STRO time resolution expression, as

TABLE 3.1: Analog simulation results of different structure of STROs using $65\,\mathrm{nm}$ CMOS technology

L	N_T	F_T (GHz)	Number of phases	$\Delta\varphi$ (ps)
9	4	6.41	9	17.3
21	10	6.16	21	7.7
41	20	6.02	41	4.0
81	40	5.95	81	2.0
161	80	5.91	161	1.0
201	100	5.91	201	0.8

follows :

$$\Delta\varphi = \frac{T_\mathrm{STR} \times G}{2L} \tag{3.14}$$

The STRO phase resolution can theoretically be set as fine as needed without a frequency drop. To clarify this point, we can consider the following example. Two STROs offering a different number of phases are able to maintain the same frequency by ensuring the same ratio N/L. As an example, a 21-stage STRO ($ring_1$) in $65\,\mathrm{nm}$ CMOS technology provides a maximal frequency of $6.1\,\mathrm{GHz}$ for $\Omega = 10/21$ (the ring contains 10 tokens). A similar frequency can be obtained with a STRO of 41 stages ($ring_2$) in which 20 tokens are included. $ring_2$ presents 41 different phases which is almost the double of the number presented by $ring_1$ (21 phases). Moreover, the time resolution of $ring_2$ is almost the half of the presented time resolution of $ring_1$, as shown in Table 3.1. Hence, increasing L will accordingly reduce the ring resolution. This resolution enhancement is limited by the jitter on each stage, as explained in next section.

A special case occurs for the modern radio frequency (RF) applications, which need a high frequency and low-phase noise quadrature oscillators. Normally, the simplest way to generate a multi-phase clock is to use a looped delay chain which does not guarantee a low phase noise. The IROs are deployed to generate signals in quadrature. However, the number of stages has to be even. Thus, in this case, the ring should include a swapped feedback lines to ensure the oscillation. One more simple solution is to consider the features presented by STROs. By using an even number of stages with the same number of tokens and bubbles ($N_T = N_B = L/2$), the STRO exhibits an absolute number of phases of 4 which corresponding to the irreducible ratio $\frac{L}{N_T} = \frac{4}{2}$. Obviously, a quadrature phase generation is obtained in this case. To expand this principle while reducing the phase noise of the oscillator, the number of stages can be duplicated by M [25]. In this case, the number of absolute phases is 4 (quadrature oscillator) while the total number of stages is necessarily multiple of 4 which is equal to $4 \times M$.

3.7 Phase noise analysis in STRO

In practice, the noise is present in any real oscillator. Whereas the noise in the spectrum is mainly due to the phase noise rather than the amplitude noise since the oscillator amplitude is well defined. The phase noise is related to the oscillation frequency or its harmonics. Generally, it is a result of the electrical component noises in the circuit.

3.7.1 Phase noise study for oscillators

The power spectral density of an oscillator on a log scale is presented in Fig. 3.19. The corresponding presentation of the phase noise spectrum, which is restricted to one single sideband spectral noise density, is divided to three regions : region with $1/f^3$ slope, region with $1/f^2$ slope, and region with $1/f$ slope (flicker noise). Based on this spectrum, Leeson [43] has proposed an empirical derived phase noise model of oscillators in which only half of the noise is attributed to phase noise :

$$\mathcal{L}(\Delta f) = 10 \cdot log\left(\left(\frac{2FkT_0}{P}\right)\left(\frac{f_0}{2Q\Delta f}\right)^2\right) \tag{3.15}$$

where P is the power consumption, Q is the loaded quality factor, k is the Boltzmann constant, T_0 is the absolute temperature, f_0 is the oscillator fundamental frequency, k is the Boltzmann's constant and F is a noise factor of the active device. Noticeably, the Q factor is the key element to determine the phase noise level. Thus, it is easy to jointly increase Q and P. Furthermore, Leeson assumed that the $1/f^2$ and $1/f^3$ corner occurred precisely at the $1/f$ corner of the oscillator which is not always true.

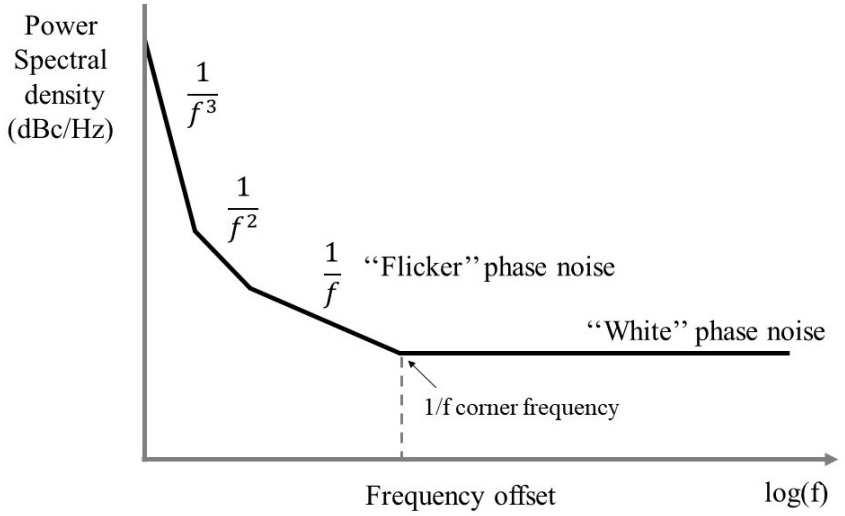

FIGURE 3.19: Oscillator phase noise vs. frequency offset.

This model has been initially developed for oscillators based on LC tank resonators and has generalized for other types of oscillators as ring oscillators [1–3, 29]. Using this approximation model allows to reduce the phase noise in oscillators. Many propositions have been developed to improve the performance of this noise for the CMOS oscillators while keeping the same figure-of-merit (FoM), which is derived from the Leeson's equation (3.15) and expressed by :

$$FoM = \mathcal{L}(\Delta f) - 20 \cdot log\left(\frac{f_0}{\Delta f}\right) + 10 \cdot log\left(\frac{P}{1mW}\right) \tag{3.16}$$

This FoM represents the phase noise normalized per $1mW$ of power consumption.

Otherwise, according to [58], the Q factor can be expressed by (3.17), which makes Leeson's model applicable to inductorless oscillators, which can be expressed as an open loop transfer function $H(j\omega) = A(\omega)\exp(j\Phi(\omega))$.

$$Q = \left(\frac{\omega_0}{2}\right) \cdot \sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\Phi}{d\omega}\right)^2} \tag{3.17}$$

In the case of the IROs, A. A. Abidi [2] has proposed a full study based on the analysis of [29] to establish the phase noise in these oscillators. The author assumes that the ring is equivalent to the current noise sources of each stage.

3.7.2 Phase noise in STRO

According to the previous study, the phase noise in an oscillator can be enhanced by improving the Q factor or the power P. Since the quality factor improvement requires complicated modifications and may change the frequency, the alternative is to improve the power by using coupled oscillators. The idea here is that M coupled oscillators consume M times more power which represents a reduction of the phase noise by M.

This phase noise improvement can be intuitively explained in the same way as in the case of coupled oscillators [58]. The oscillators are considered as $M \times L$ current noise sources in the case of coupled oscillators instead of L for the simple case. Assuming these noise sources are uncorrelated and equal in power, their sum phase noise contributions, near to integer multiple of the oscillation frequency ω_0 is reduced by M^2, whereas the noise power increases by M. Consequently, multiplying the number of stages of an STRO by M while maintaining the same occupancy ratio allows reducing the phase noise by M. In other words, a STRO of $M \times L$ stages with $M \times N_T$ tokens produces exactly the same output shape and the same frequency with a power consumption M times higher than a L-stage STRO. Hence, according to (3.15), the $M \times L$-stage STRO shows a phase noise reduced by a factor of M.

Moreover, this phase noise enhancement in STROs does not depend on any coupling quality factor. STRO stages can be considered as intrinsically coupled and their coupling factor, in

analogy to the coupled oscillators, can be considered equal to one. Obviously, the total power consumption grows M times while the FoM remains unchanged. Hence, the lower phase noise would come at the cost of a proportional higher power consumption and area. The approach to get this enhancement is to define the suitable number of stages L that offers the desired frequency and phase resolution with a FoM performance close to the theoretical limit. Then, according to this structure, the number of stages and obviously the number of tokens can be increased M times to perform the targeted phase noise at the cost of M times higher power consumption as defined by the follow equation :

$$\mathcal{L}_{M\times L}(\Delta f) = \mathcal{L}_{L}(\Delta f) - 10 \cdot log(M) \tag{3.18}$$

Due to the noise floor imposed by the high-frequency thermal noise, as displayed in Fig. 3.19, an asymptotically zero phase noise STRO cannot be unfortunately created by having a very large number of elements.

Based on the same example of the quadrature oscillator discussed in the previous section and according to (3.18), the phase noise is improved by M while conserving the same absolute number of equidistant phases of 4 due to the increased power consumption. We consider that a STRO of $L = 4$ and $N_T = 2$ produces a phase noise of $\mathcal{L}(\Delta 1\,\mathrm{MHz}) = -81.96\,\mathrm{dBc/Hz}$, a power consumption of $P = 0.62\,\mathrm{mW}$, and $\mathrm{FoM} = -164.36\,\mathrm{dBc/Hz}$. This ring generates four absolute phases. A second ring of $L = 24$ and $N_T = 12$ will show the same number of absolute phases (which is 4) and the same frequency as well ($5.0\,\mathrm{GHz}$). However, the resulted phase noise is equal to $\mathcal{L}(\Delta 1\,\mathrm{MHz}) - 10 \cdot log(6) = \mathcal{L}(\Delta 1\,\mathrm{MHz}) - 7.78 = -89.74\,\mathrm{dBc/Hz}$. More detailed informations about this phase noise inhancement is presented in our papers [24, 25].

3.7.3 Jitter in STROs

The jitter represents the undesired fluctuations in time of a signal that arises due to the phase noise. Jitter is often specified by its peak-to-peak value or the RMS value that is extracted from the zero-crossing time of the periodic signal. So, the jitter can be observed from this presentation since the signal is not strictly periodic due to noise. Jitter is relevant for oscillators because it represents another way to observe the phase noise. Based on the impulse sensitivity function (ISF), which describes how much phase shift results from applying a unit impulse at a specific time, [2, 29] proposes a global expression associating the jitter with the phase noise for ring oscillators. The study shows that the jitter mainly depends on charge/discharge current and capacitance in the ring.

As in the case of the IRO, timing variations are present in the STRO due to the local noise sources of stages (mainly white noise thanks to the high frequencies of STROs). However, the propagation of these timing variations from one stage to another is limited since the time that elapses between successive events is controlled by the evenly-spaced locking mechanism.

Furthermore, global noise sources (e.g. power supply noise) do not strongly affect the phase distance (in degrees) between successive events as they have the same impact on each event. A. Cherkaoui *et. al.* [14] analyse and measure jitter in an FPGA implementation of STROs. Experimental measurements confirmed a Gaussian distribution of the period with a standard deviation of the same order of magnitude as the standard deviation of the propagation delay of one single ring stage. This suggests that the jitter measured at the output of each STRO stage is mostly composed of the random jitter that originates from the local noise sources of the stage.

3.8 Other features of the STRO

STROs have many other interesting features as digital oscillators such as robustness against process variability, and configurability.

3.8.1 Robustness to PVT variations

STROs have a high robustness to PVT variations thanks to the Charlie effect [31]. In this study, random Gaussian variations have been attributed to the parameters of the 3D Charlie model ((3.7)). As a result, when the ring is operating at its highest point, the maximum of the Charlie's effect, it shows a high robustness to process, voltage, and temperature variations.

3.8.2 STRO as programmable oscillator

Two different strategies based on architectural solutions can be used to setup the parameters for the controllable STRO frequency. In fact, the ring is able to provide different oscillation frequencies with the same number of stages by simply changing the number of events. Additionally, it can be seen as a Programmable Self-Timed Ring (PSTR), as proposed by [78].

The first strategy is based on the variation of the number of tokens and bubbles in the ring. So, the frequency varies with the occupancy ratio Ω while keeping the same number of stages. This principle has been presented in Section 3.5, which is more explicit in the frequency curve of Fig. 3.18. To initiate the appropriate occupancy ratio, a special design of the C-element allows initializing the gate with a token or a bubble. As evoked before, the *set* and *reset* signals have to be included in this gate. The set exhibits the output to the state high and reset triggers the output C for a low state. In order to clarify this process, let consider the example of a 9-stage STRO. Assuming that the maximal frequency is obtained for $N_T = 4$, the stage can be initialized with this configuration : $BTBTBTBTB$, which is equivalent to the output values 001100110. T is referred to tokens and B to bubbles. By modifying this configuration to 001100000, two tokens are now propagating in the ring inducing a lowest frequency. Additionally, the lower frequency can be obtained for the configuration 010101010.

The second strategy is based on a controllable number of stages and not only on the number of tokens and bubbles. In [78], a programmable STRO with a very modular design using a MUX gate placed after each stage is proposed. Within this structure, the design is started with a maximal number of stages L. Then, a stage control word (SCW) is used to remove up to $L-3$ stages. Therefore, the number of stages and the frequency are configurable simultaneously, which allows a high flexibility. This structure provides an interesting range of frequencies and gives a great solution in terms of speed and power if a limited number of Muxes is used [78].

3.8.3 STRO in other applications

The jitter of events propagating in the STROs has been deployed to design true random number generators (TRNG) with a high entropy [15]. In this structure, the tunable sub-gate delay resolution is exploited for extracting random numbers. Increasing the number of stages and adjusting the number of events for the STRO produces a short enough time between two successive events to the capture of the jitter, which is in practice an interesting source of entropy. Even if this jitter magnitude is low such as a few picoseconds, the design of TRNG using STRO allows extracting the entropy from this jitter. The proposed structure has many features related to security, throughput and power consumption [15].

3.9 Conclusion

Based on simple asynchronous digital gates, called C-element, the architecture of the STRO is simple to design. This oscillator allows propagating several events simultaneously without colliding thanks to the request/acknowledgment handshake protocol. The number of these events stays invariant. The ring is modeled with a token game by which the events are initialized in the ring. The events push away in time from each other as they propagate in the ring due to the presence of the analog phenomena, namely the Charlie's effect and the Drafting effect. As a result, two steady state modes are possible : the evenly-spaced mode and the burst mode.

One important features of the STROs is that their frequency does not directly depend on the number of stages but rather on its occupancy ratio. Moreover, this frequency can be adjustable for the same STRO. Therefore, unlike the inverter ring oscillators, the frequency and the time resolution are not directly dependent. Many applications have exploited these features as TRNGs, programmable oscillators, low phase noise quadrature oscillators, etc.

The main consequence of the STRO evenly-spaced mode is that STROs can produce a uniform phase distribution. As a result, a regular time base is generated by these equidistant phases. So the time resolution between these phases can be accurately tuned as fine as needed by simply increasing the number of ring stages. The resulted equidistant phases is able to achieve sub-gate delay resolutions and can be exploited for on-the-fly time measurement on fast non-periodic

signals, as it will be detailed in the next chapter.

Chapitre 4

STRO-based TDC architecture and implementation

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4.1 Introduction

Time-to-digital converters (TDCs) are widely used for precise time measurement. TDCs with sub-gate resolution and wide dynamic range are widely required in many fields. As presented in Chapter 2, the usual architecture of a TDC is simply based on counting the number of edges of a reference clock signal during the measurement interval. They can be carried out by low-power and compact digital circuits. Many TDC principles, dealing with time resolution improvement, have been proposed in the literature. In the simplest TDC architectures, the time resolution is bounded by the CMOS gate delay. In order to overcome this technological limitation, sub-gate delay resolution solutions have been proposed, such as hybrid architectures based on the Vernier principal [19, 44–46, 68, 79]. As wide dynamic range of time measurement is also mandatory in many applications, some architectural techniques have been proposed such as interpolation schemes or multi-quantization levels to achieve wide measurement ranges with sub-gate time resolutions [42, 63, 76]. Nevertheless, while many of the TDC architectures proposed in the literature can achieve high measurement accuracy, they often require repetitive measurements. Therefore, on-the-fly measurements on fast non-periodic signals (a few tens of picoseconds) are challenging for most of TDCs.

In this thesis, we propose a new architecture of a TDC based on a self-timed ring oscillator. Thanks to the STRO characteristics, as shown in Chapter 3, a regular time base is generated by equidistant phases. The time resolution of this TDC can accurately be tuned, theoretically as fine as needed by simply increasing the number of STRO stages. In addition, the proposed TDC architecture allows on-the-fly time measurement on fast non-periodic signals. To a certain extent, it does not require multiple samples nor repetitive measurements even if the resolution is sub-gate delay.

In this chapter, the proposed TDC architecture based on STRO and its working principle are presented and discussed. Thus, the main TDC blocks of this architecture are detailed. As a proof-of-concept, our STRO-based TDC has been implemented and simulated using CMOS $28\,\mathrm{nm}$ FDSOI technology. High-level and analog simulations are detailed in the last section. Simulation results point out the advantage of this TDC in terms of measurement accuracy, even in noisy environment, and state the limit of the on-the-fly measurement according to the trade-off between jitter and time resolution.

4.2 Proposed TDC

4.2.1 STRO-based TDC principles

The proposed STRO-based TDC exploits the features of the STRO previously presented in Chapter 3. In fact, an L-stage STRO, with a number of tokens N_T co-prime with the number of stages L, provides L signals evenly distributed over its half oscillation period $T_{\mathrm{STR}}/2$. Fig. 4.1

shows the re-arranged phases of a 9-stage STRO initialized with 4 tokens. As it can be seen in this figure, for a simple edge consideration (rising or falling edge), the phases are distributed uniformly over the period T_{STR}. If both edges are considered, the phases are distributed over the half period $T_{\mathrm{STR}}/2$. This offers a periodic and regular time stamping with a resolution of $\Delta\varphi = T_{\mathrm{STR}}/2L$ that can be exploited in a TDC. The phases are not intuitively arranged in the output order. Therefore, the phase of C_i is not necessarily followed by the phase of C_{i+1}. In the case, where all phases are appropriately arranged, we can assimilate the STRO to an inverter ring oscillator (IRO), which operates with a propagation delay $\Delta\varphi$ (phases are shifted by a delay $\Delta\varphi$). The time base could be interpreted as the XOR of the outputs (presented by *C_out* signal in the figure). This time base is equivalent as a clock reference with a period that can be tuned as fine as needed by simply increasing the number of stages.

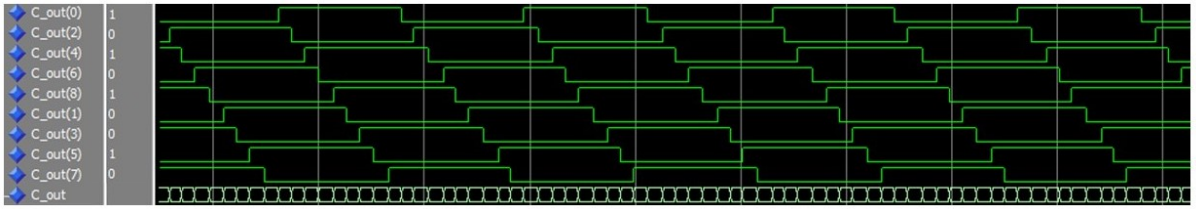

FIGURE 4.1: Re-arranged phases of a 9-stage STRO with 4 tokens.

By exploiting the L-stage STRO phases, we propose to quantify the time interval T considering both edges. Obviously, double-edge counters can easily be implemented to the output of each ring stage, as presented in Fig. 4.2. The objective for each counter is to measure the time interval T as a function of $T_{\mathrm{STR}}/2$ and then to quantify the residue time by the resolution $\Delta\varphi$. Assuming that the number of tokens is co-prime with the number of stages, the time resolution is given by $\Delta\varphi = T_{\mathrm{STR}}/2L$. The *Enable* signal brings the start and stop times of the interval T, which needs to be measured.

Let M be a coarse quantification of T with the resolution $T_{\mathrm{STR}}/2$, which verifies the following equation :

$$M \cdot \frac{T_{\mathrm{STR}}}{2} \quad \leq T \quad < (M+1) \cdot \frac{T_{\mathrm{STR}}}{2} \tag{4.1}$$

If taken individually, each STRO output provides this approximate measurement of T. Therefore, if all outputs are connected to n-bit counters as displayed in Fig. 4.2, each counter would count either M or $M+1$ events. Let k be the number of counters having the value $M+1$ (while $L-k$ counters have the value M).

As shown in Fig. 4.3, the measured time interval T_m can be expressed by (4.2) in the case of counters showing M and by (4.3) in the case of $M+1$. The measurement can be improved by aggregating the counter results in order to achieve $\Delta\varphi$ time resolution. The general expression of T_m is given by (4.4) in which M corresponds to the coarse measurement of the number of $T_{\mathrm{STR}}/2$ steps (number of rounds over the measurement), while k corresponds to the finer

measurement (corresponding to the number of phases counted after the time $M * T_{\mathrm{STR}}/2$). According to this expression, the quantification of T requires only determining the values k, M, T_{STR} and $\Delta\varphi$.

$$T_m = M \cdot \frac{T_{\mathrm{STR}}}{2} + k \cdot \Delta\varphi \tag{4.2}$$

$$T_m = (M+1) \cdot \frac{T_{\mathrm{STR}}}{2} - (L-k) \cdot \Delta\varphi \tag{4.3}$$

$$T_m = M\frac{T_{\mathrm{STR}}}{2} + k\Delta\varphi = (ML+k)\Delta\varphi \tag{4.4}$$

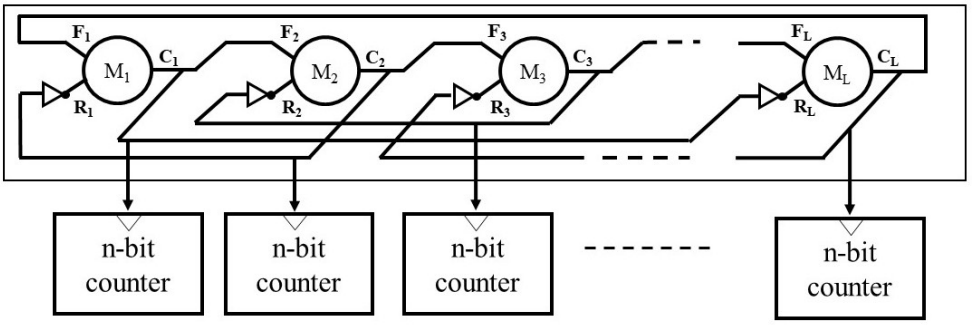

FIGURE 4.2: Basic architecture of the STRO-based TDC using only n-bit counters.

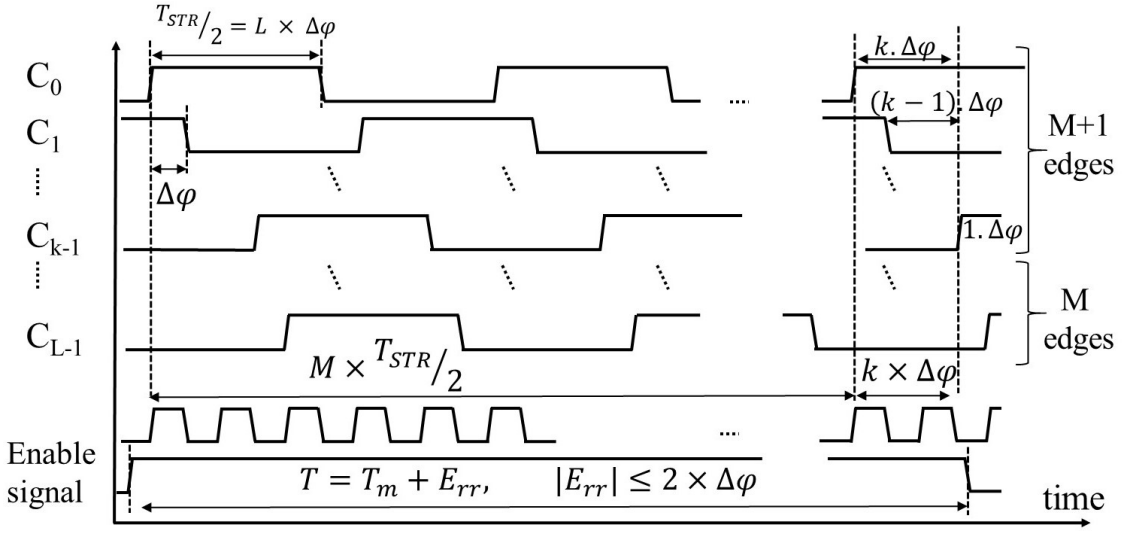

FIGURE 4.3: Time measurement diagram.

4.2.2 Global architecture

Instead of using n-bit counters for all the phases, a simple technique can be applied in order to determine the values of M and k. Therefore, we suggest firstly examining the counter outputs. Thus, let $B_k = (b_{k,0}, b_{k,1}, ..., b_{k,n-1})$, where $k \in [1, L]$, be the bit vector presenting the output of the k^{th} n-bit counter connected to the STRO output C_k. This binary value of M_k can be equal to M or $M + 1$.

To cover all the possible cases, Table 4.1 displays the binary vector M_k for both cases M and $M + 1$. The difference is globally detected for the two least significant bits (unless the state 4 which can affect sequentially the MSB). In fact, the two lower bits are presented since the difference is mostly noticed for the two lower bits (unless the state 4, which affects sequentially the MSB). We propose to represent M with the vector B_i, and $M + 1$ with the vector B_j. The parity of M can be evaluated using the bits $b_{k,1}$ ($k \in [1, L]$). B_i is even when : $b_{i,1} = b_{j,1}$ (state 1 and 2). Oppositely, B_i is odd when the two bits are different (state 3 and 4). Therefore, the second LSB bits $b_{i,1}$ and $b_{j,1}$ differ only when the LSB of M is equal to '1' (M is odd). In the sequel, we denote $LSB_1 = (b_{1,1}, b_{2,1}, ..., b_{L,1})$ the vector made by the second LSB bit of the counter outputs and $LSB_0 = (b_{1,0}, b_{2,0}, ..., b_{L,0})$ the vector made by the LSB of the counter outputs. Therefore, if at least one bit of LSB_1 is different, then M is odd, and if they are all equal, then M is even.

TABLE 4.1: Possible states for the n-bit vectors $B_k = M$ and $M_k = M + 1$.

State	M $(b_{i,n-1}, b_{i,n-2}, ..., b_{i,1}, b_{i,0})$	$M+1$ $(b_{j,n-1}, b_{j,n-2}, ..., b_{j,1}, b_{j,0})$
1	X...X00	X...X01
2	X...X10	X...X11
3	X...X01	X...X10
4	X...X11	X...X00

On the other hand, if the LSB of B_i is equal to '0' (in case M is even), the number k of counters having the value B_j is the number of the bits of the vector LSB_1 equal to '1'. Otherwise, in case B_i is odd, the number of the bits of the vector B_1 equal to '1' corresponds to the $L - k$ of counters having the value B_i (the count of zeros is the number k). In this case, k corresponds to the number of bits of the vector LSB_1 equal to '0'.

$\Rightarrow$ Hence, the hamming weight of the vector LSB_0 is used to define the value of the variable k. More explicitly, the hamming weight of LSB_0, denoted with H, is equal to k when M is even and $L - k$ when M is odd. According to the above analysis, equation (4.4) can be resolved by using a simple algorithm. Let N_v be the number of transitions counted by an arbitrary n-bit counter during the time interval T. To determine if the value N_v corresponds to M or $M+1$, we evaluate the parity of M using LSB_1. Then we compare the result with the parity of the value N_v. The value of k is determined by the hamming weight of LSB_0. The global architecture of

our proposed TDC is depicted in Fig. 4.4.

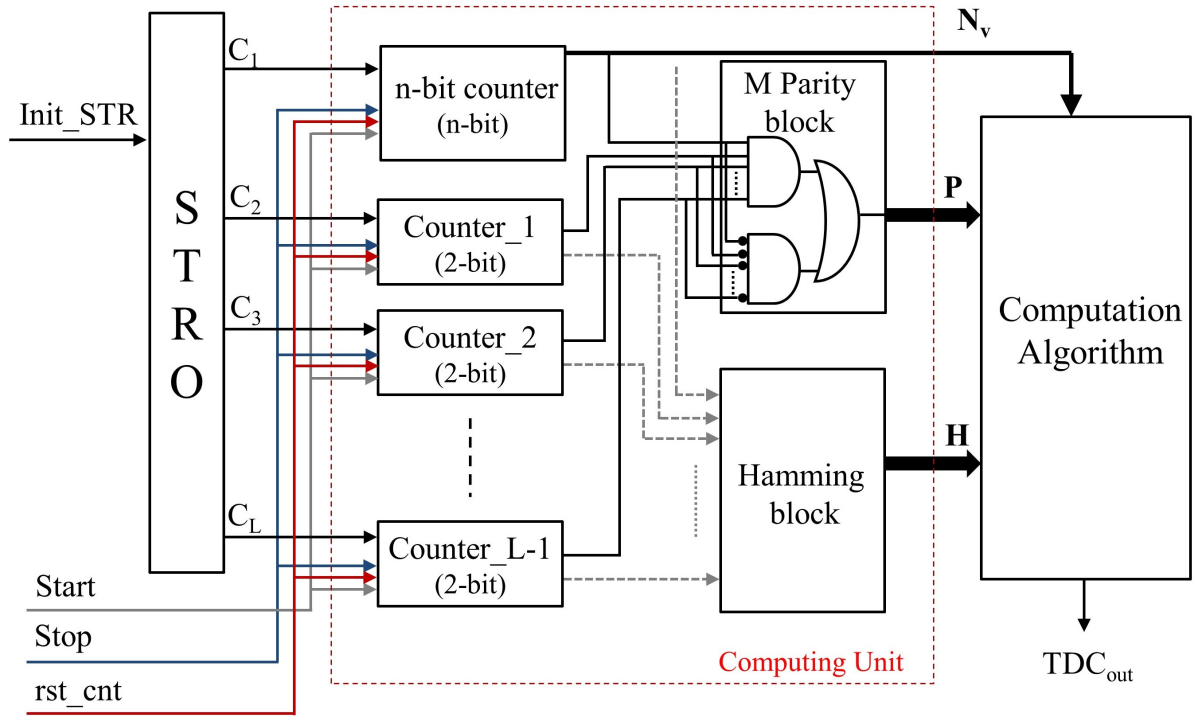

FIGURE 4.4: Proposed TDC architecture using an L-stage STRO.

In this structure, an L-stage STRO is used. The coarse conversion is carried out by an n-bit counter connected to a single STRO output. The value N_v is provided by this n-bit counter. Then, for the other $L-1$ STRO outputs, only 2-bit counters are required in order to determine both M and k. The parity of M is noted with a Boolean P, which is set to '1' if all bits of LSB_1 are identical and to '0' otherwise. This information is obtained by the M Parity block. The Hamming block uses the LSBs of the counters to compute the hamming weight H. Table 4.2 summarizes the computation algorithm of M and k as a function of N_v, P and H. The diagram given by Fig. 4.5 facilitates the understanding of the algorithm for computing the measured time. The TDC output TDC_{out} can be expressed by ((4.5)) according to the parity of N_v.

TABLE 4.2: The predicted value of M and k as a function of N_v, P and H.

	N_v odd	N_v even
P = M even	$\mathbf{M} = N_v - 1 \quad ; \mathbf{k} = H$	$\mathbf{M} = N_v \quad ; \mathbf{k} = H$
P = M odd	$\mathbf{M} = N_v \quad ; \mathbf{k} = L - H$	$\mathbf{M} = N_v - 1 \quad ; \mathbf{k} = L - H$

$$\mathrm{TDC_{out}} = \begin{cases} P[N_\mathrm{v}L+H] + \bar{P}[N_\mathrm{v}L-H] & \text{if } N_\mathrm{v} \text{ even} \\ P[(N_\mathrm{v}-1)L+H] + \bar{P}[(N_\mathrm{v}+1)L-H] & \text{if } N_\mathrm{v} \text{ odd} \end{cases} \tag{4.5}$$

Finally, given (4.4) and (4.5), the measured interval T_m can be computed by :

$T_m = \mathrm{TDC}_{out} \cdot \Delta\varphi.$

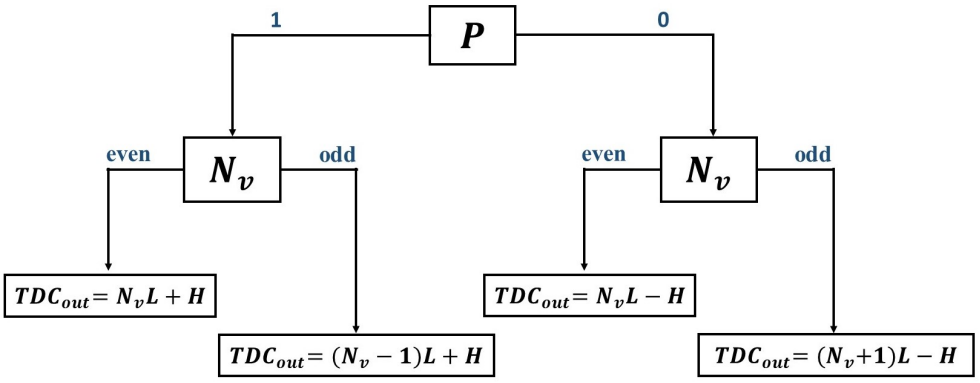

FIGURE 4.5: Computation algorithm applied to the STRO-based TDC according to the values provided by the computing unit H, P, and N_v.

4.3 STRO-based TDC readout techniques

4.3.1 Asynchronous vs. synchronous counters

Usually, two common counters are used : synchronous and asynchronous counters. The synchronous counters are operating with a common clock signal, which allows to the registers to be simultaneously triggered. They necessarily include the combinational logic. The use of this logic affects the speed performances of the counter, especially with an increased number of bits. The architecture of the synchronous counter is displayed in Fig. 4.6a in which D-type flip-flops are employed. On the other hand, the asynchronous counters are simpler since they do not require combinational logics. The circuit, as presented in Fig. 4.6b, is based on a frequency divider block. Each block output is connected to the clock input of the following block. Otherwise, they can present a problem of ripple especially in the presence of large time intervals. The harmful effect of the ripple problem over the measurement results is when the *Stop* event triggers the registers to sample the outputs exactly in the ripple region, as it can be seen in the timing diagram of Fig. 4.6c.

For a binary counter, regardless its type, the input frequency and the bit width are the most relevant parameters. The input frequency is defined as the frequency of the clock signal, which triggers this counter. The counter bit width is the number of bits for a binary representation of the counter output, noted N_{cnt}. Alternatively, it represents the number of registers of the counter. Unfortunately, these two parameters are dependent. In fact, for the same fixed time interval, the increased input frequency induces a fast counting process, which requires additional bits to represent the result.

The operating frequency (counting rate) of the counter has been reported in [36]. In the

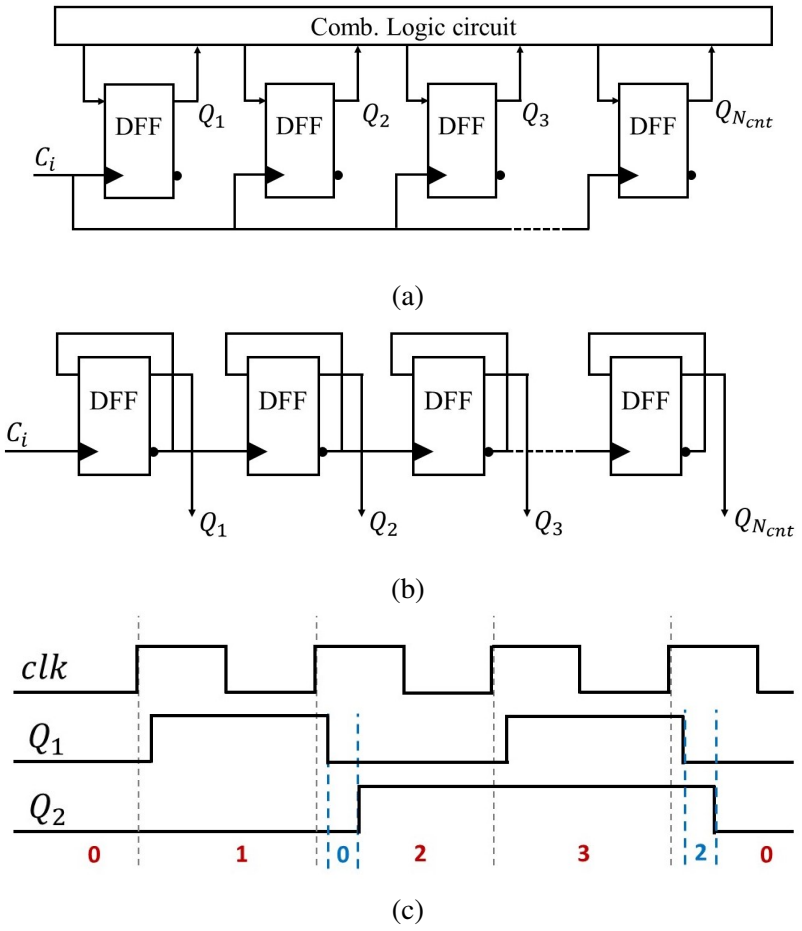

FIGURE 4.6: Counters based on D-type Flip-Flops :(a) Synchronous structure (b) Asynchronous structure, (c) timing diagram of asynchronous counter showing the ripple issue.

synchronous counter, the clock C_i drives all the flip-flops. Thus, its period should be longer than the critical path of the combinational logic. Usually, the combinational logic of the last FF is associated to the longest path for which the operating frequency F_{op} is expressed by :

$$F_{op} = \frac{1}{t_{FF} + t_{comb} \times (N_{cnt} - 2)} \tag{4.6}$$

where t_{FF} includes the setup time and propagation delays of the FFs, and t_{comb} is the mean value of the propagation delay of the combinational logic. Notice that the combinational logic at each FF input are not the same. For the asynchronous counter, this frequency is restricted to the delay t_{FF} since the input clock triggers only the first FF. In order to avoid any generated error from the counting operation, the input frequency (STRO frequency) should be smaller than the counter operating frequency. This can be a first criterion for a counter choice.

On the other hand, the value of the TDC output, corresponding to the maximal time input (the TDC dynamic range, DR), should be lower than the maximal value given by the counter. It

can be explicitly expressed by :

$$2^{N_{cnt}} > \frac{DR}{t_q} \tag{4.7}$$

Based on these conditions, a comparison has been performed between the synchronous and asynchronous counters in [36] for the case of IRO/GRO based TDC, in which the frequency depends on the time resolution. According to the targeted dynamic range, the study proposes to plot a diagram presenting the number of IRO stages as function of the number of counter bits for each counter type. This offers a compromise to choose the minimal number of bits for each kind of counters based on the targeted performances of the TDC.

4.3.1.1 The counter issues

The ripple effect is a common problem for all counters due to the cumulative propagation delays. It is more sensitive for asynchronous counters in which any new stage adds a delay to the propagation delay. Thus, this type of counters has to limit the number of stages in order to reduce this ripple effect. In [39], an asynchronous high-speed counter has been proposed. The paper proposed additional circuitry to calibrate the problem of ripple in this counter. For the coarse measurement of our proposed TDC, the influence of this ripple can be of a great importance since the counting step is the half oscillation period $T_{\mathrm{STR}}/2$.

Otherwise, another problem, due to sampling the counter outputs before ending the counting process leads to missing codes. In fact, the registers are at the origin of the TDC latency, which extends the time of response of counters. Therefore, to overcome this issue, the sampling operation have to start after that the counting process was completed.

The glitches are another issue related to the FFs. It is a consequence of the floating state at the register input, which can be produced in presence of noise (this problem is essentially encountered with the GRO). Straayer *et. al.* [62, 63] proposed to include modified buffers in order to eliminate the floating state and avoiding the glitch problem. In other words, the counter input is forced to a logical value. A de-glitch circuit, which is equivalent to the C-element gate, has been proposed to avoid double counting.

Since flip-flops are used, the counters are affected to an unavoidable and serious problem, which is the metastability. In fact, the register input might change when being captured by the clock, which violate the setup/hold time and generate a metastability state. It is an undesirable state for which the output propagation delay increases and takes an undefined time to be stabilized. Usually, synchronizers are used to compensate the effect of this phenomenon but are able not to avoid it. The most popular synchronizer implementation is made of two FFs. Fig. 4.7a shows the conventional synchronizer circuit. The principle is that if the output of the first register goes into a metastable state, the output of the second register will become metastable state if only if the output of the first FF shows an unstable state during more than one clock period. This case is fortunately rare and happens with a probability close to zero. Nevertheless, when using

very high frequencies, the probability of having a metastable state over a given period increases because of the higher number of draws (sampled data), showing that the probability is not zero. The waveforms of this phenomenon are shown in Fig. 4.7b. For a better reliability, the number of stages can be increased in case of high frequency.

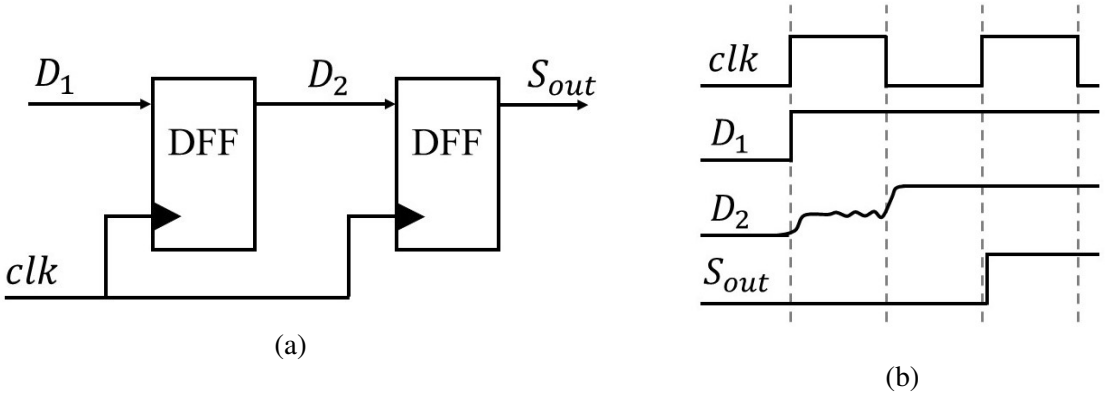

FIGURE 4.7: Two Flip-Flop synchronizer :(a) structure (b) timing diagram.

Another circuit dealing with metastability, illustrated in Fig. 4.8, is called mutual exclusion (MUTEX). This circuit allows making an exclusive selection between two signals *In_1* and *In_2* and is able to avoid metastability on its two outputs, thanks to the analog metastability filter. This has originally been developed for the request signals in the asynchronous circuits. When one of the requesting signals goes high, the selected one goes high and the other one is forced to low. Thus, a decision is made [16, 59].

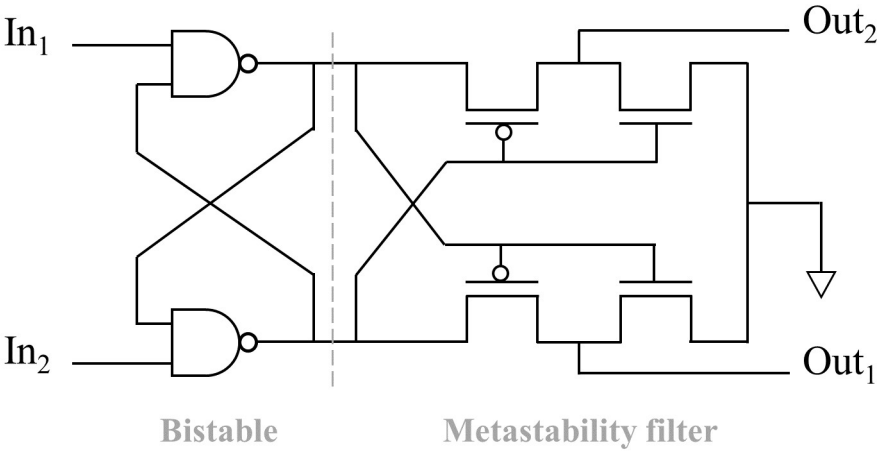

FIGURE 4.8: An example of a mutual exclusion element implementation [59].

In addition to the important latency that can be caused by the metastability phenomena, the result can be completely inaccurate when the most significant bit (MSB) is affected. Consequently, the TDC will be heavily disturbed if the n-bit counter of the architecture of Fig. 4.4 is affected by a metastability problem. Thus, the quantification error is function of $T_{\mathrm{STR}}/2$ while

it was supposed to be less than $2\Delta\varphi$. A grey encoding can be also used to minimize the metastability effect since only one bit is changing for each state.

4.3.1.2 STRO-based TDC counter implementations

The counters are of type double edge, which allows considering the rising and the falling edges of the STRO phases. The problem of metastability is more relevant for the double edge counter especially for high input frequencies. In addition, since the TSRO is rapid, the counter can be subject to the count-missing problem. A solution to the aforementioned problems is not unique and can differently be treated.

Two different structures of double-edge counter are proposed in the sequel. Based on the same principle, the n-bit and the 2-bit counters have the same implementation. All the counter flip-flops are triggered by an *rst_cnt* signal, which sets the outputs to a low state. The hit signal can be implemented separately as a *Start* and a *Stop* signals, or as one *Enable* signal for which the rising edge starts the counting process and the falling edge launches the output sampling. The integration of these signals into counters has many possibilities.

1^{st} **counter :** As a first proposition, the asynchronous counter is used. The first stage is designed as double-edge flip-flop. It is made by two XORs and two latches. In Fig. 4.9, the first latch is enabled with the high state of *Enable* signal and starts copying the C_i clock during this time interval. The second latch is inversely triggered with the inverse of the *Enable* signal. The output of the two latches are reused as reciprocal inputs of the XORs. The output of the first latch is the LSB of the counter Q_1, and then it serves to feed the next stage of the counter. The remaining stages are the standard circuit of the asynchronous counter. This counter operates correctly for medium frequencies. However, it can be a subject of metastability due to the loop of the double-edge stage in case of high frequency operations.

2^{nd} **counter :** Another solution to conceive the double-edge counter is to consider the rising and the falling edges separately. Despite the increased area, this solution is simple and prevents the problem caused by the high input frequency. The principle is to duplicate a simple counter of any type (synchronous or asynchronous) with inverted clocks as shown in Fig. 4.10. As it can be observed in this figure, the *Enable* has been replaced with the *Start* and *Stop* signals.

4.3.2 Hamming block

The LSBs B_0 of the 2-bit counters and the n-bit counter are used to compute the hamming weight H, which represents the margin value k for a finer resolution step of (4.4). The Hamming block uses the B_0 to compute the total number of ones which can be expressed by (4.8).H is

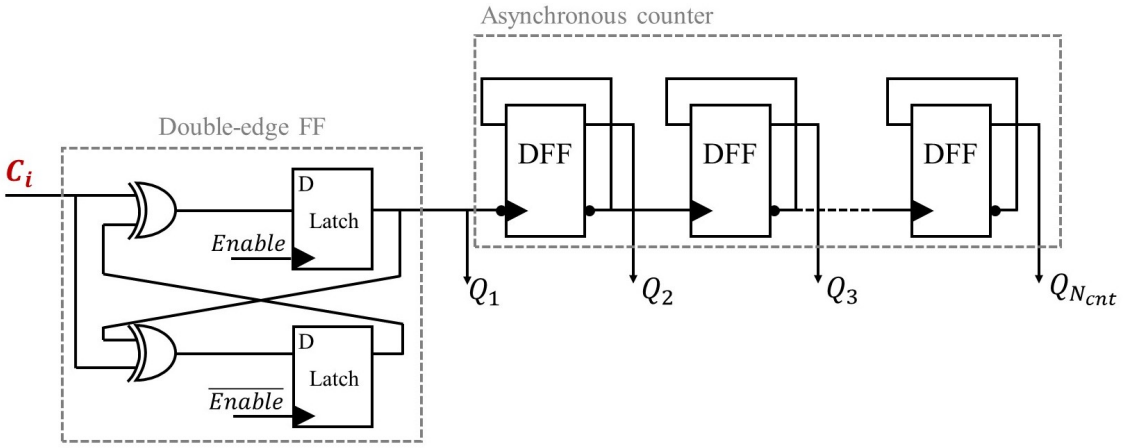

FIGURE 4.9: Example of the asynchronous double-edge counter implementation based on latches.

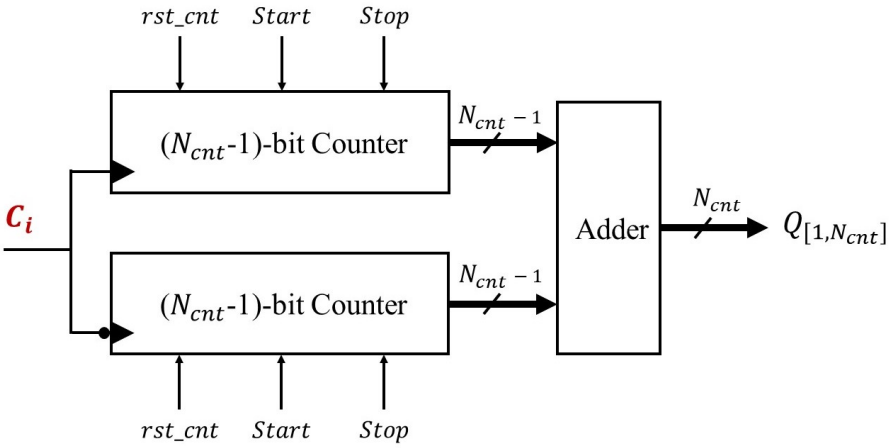

FIGURE 4.10: Combined counters for double-edge operation based on rising and falling edges.

equal to k when M is even and $L-k$ when M is odd.

$$H = \sum_{k=1}^{L} b_{0,k} \tag{4.8}$$

As an optimized implementation, we propose to use the leading-zero counting (LZC) circuit. The LZC is characterized by smaller delays and relatively smaller hardware requirement. It is originally based on the same principle of adders but with an optimized design. It supposed that the input data bits are divided into two parts. For instance, the "zeros" correspond to the left word bits and the "ones" to the right word bits ($LZC_{in} = B_0 = 00..01..11$). The main principle of LZC is to define the number of zeroes crossed from the most significant position of B_0 to reach the first one of this input data bits [50].

In the case of the STRO, the phases are not naturally arranged. Thus, they have to be re-

arranged before connecting them to the counters. Unfortunately, even though they are well sorted, the sampling instant due to the time measurement is unkown. In this case, B_0 may have four possible cases :

$$case1 : 000...000111...111$$
$$case2 : 00..0011..1100..00$$
$$case3 : 111...111000...000$$
$$case4 : \underbrace{11..1100..0011..11}_{length\ of\ L\ bits}$$

Additionally to the above cases, a vector of zeroes or ones can be obtained as well and have to be included in the study. Thus, a generic structure that can fit all these cases requires two LZC blocks.

For the $cases$ 1,2,3, B_0 is applied directly to the first LZC and the flipped order vector $B_{flip} = (b_{L,0}, b_{L-1,0}, ..., b_{1,0})$ is applied to the second LZC. The sum of both LZC outputs shows the number of zeros in B_0. The unwanted case is when all the bits are zeroes. Using the previous method for the LZC, the output result is a value of $2L$ instead of being L. Then the output should be divided by 2 if the parity of B_0 is one. The final presented value of this block should be correctly included in the final algorithm since it presents the number of zeroes instead of the ones.

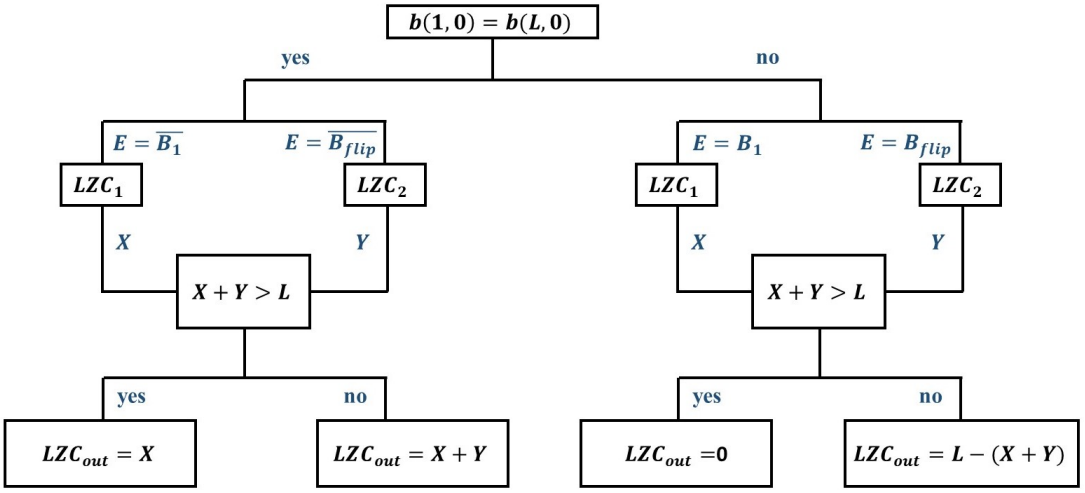

FIGURE 4.11: Algorithm of applied leading zeroes counting (LZC) block.

Otherwise, for the $case\ 4$, B_0 is firstly inverted ($\bar{B_0}$). Then, the same method previously presented is applied. However, the result of the LZC in this case is the number of "ones" in B_0. A test distinguishing the above cases is done for the first and the final bits of B_0 (comparing $b_{1,0}$ and $b_{L,0}$). In order to detect the $case\ 4$ in which the output of the parity block is the number of "ones", an output d_{11} is added taking the value '1' in this case and '0' in the others. Fig. 4.11

shows the detailed algorithm for the LZC operation.

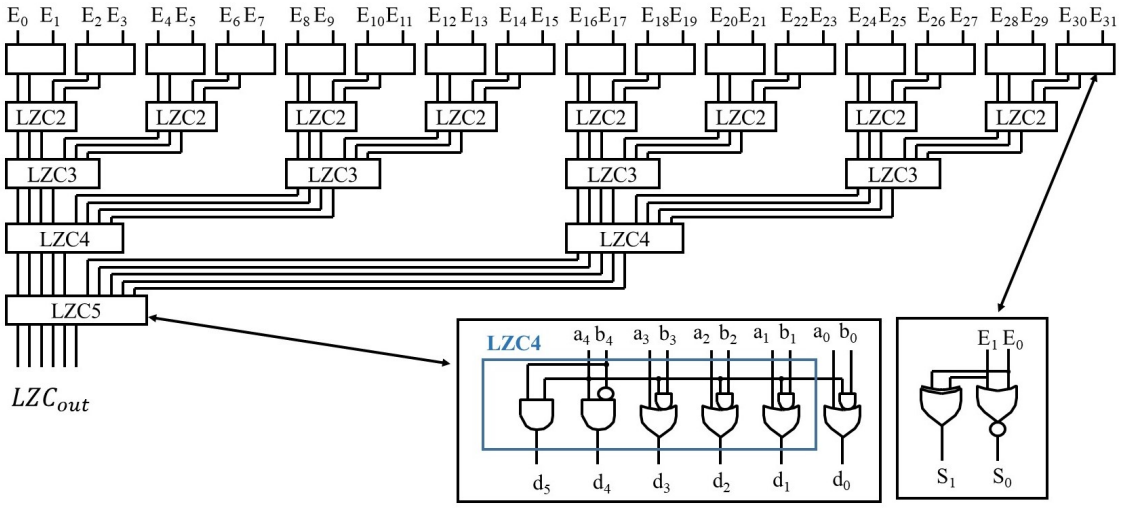

FIGURE 4.12: Example of 32 input LZC architecture with a circuit implementation for the LZC5 (8 inputs / 5 outputs).

An example of a 32-input LZC is presented in Fig. 4.12. In this figure, the LZC5 is presented but other $LZCi$ ($i \in \{2, 3, 4\}$) can be derived from this circuit. The basic element for two inputs is shown as well. This technique is faster and more reliable in time but presents a limitation when the jitter is large enough.

For a high level of jitter, a simple tree of adders based on half and full adders can be used. An adder of 32 inputs is estimated to include 83, XOR, 83 AND, and 26 OR gates with a total number of gates of 192. Similarly, the presented LZC of Fig. 4.12 has a total number of gates of 100 gate : XOR (1), NOT (16), OR (27), and AND (56). The major advantage of the simple adders is their insensitivity toward jitter and an output which defines directly the number of "ones" of the input B_0. Since the LZC should be duplicated, this solution presents a larger number of gates compared with adders. Finally, we can admit that the use of adders is the more stable implementation for the Hamming block especially when a fine time resolution is required (tens of picoseconds).

4.3.3 M Parity block

The M Parity block sets to '1' its output when its inputs are identical and to '0' otherwise. This operation allows determining the parity of M since the difference between M and $M+1$ is detectable thanks to the second LSB of each counter output as previously explained. The input of the M Parity block is formed by the MSB of the 2-bit counters and the second LSB bit $b_{1,1}$ of the n-bit counter (LSB_1 is the input of this block). Thus, the output of the M Parity block is

expressed by :

$$P = \prod_{k=1}^{L} b_{1,k} + \prod_{k=1}^{L} \bar{b_{1,k}} 4 \tag{4.9}$$

The M Parity block is a simple circuit because it requires just some combinational logic based on AND gates as illustrated Fig. 4.4.

4.3.4 Computation algorithm

The computation algorithm, which allows executing the four equations of Fig. 4.5, can be implemented in hardware either in software. A synthesized code can provide a hardware implementation of this block. Its latency is added to the global TDC latency. Alternatively, the computation of the equations can be made using FPGA or microcontroller boards in which the measurement result is directly displayed on an LCD-screen of a 7-segment display.

4.4 STRO-based TDC simulations using 28 nm FDSOI technology

4.4.1 High-level validation

4.4.1.1 Behavioral model

The high-level simulations are based on a VHDL behavioral model using dedicated libraries for modeling self-timed rings. The TIMA Asynchronous Library (TAL) has been designed at the TIMA laboratory in order to perform a complete model for asynchronous circuits. The package *charlie_function* is used to store into variables (T_a and T_b for the C-element inputs and T_z for its output) the temporal event information. Moreover, it allows computing the Charlie propagation delay as presented by (3.7). The TAL configuration makes that every Muller gate has its own probability distribution independently of the other gates. Small variations are generated around the propagation delays with these dedicated distributions. Thanks to these libraries, the Charlie and Drafting effects are correctly modeled. Furthermore, this model allows simulating the TDC behavior in a noisy environment by adding jitter on the STRO stages. Jitter is implemented using a software random number generator by generating timing variations in the STRO stages when their delays are evaluated in the simulator. The obtained distributions follow a normal distribution with a mean value corresponding to the propagation delays measured during the analog simulations and with a configurable standard deviation.

This high-level design flow is based on parameters extracted from analog simulations, which are back-annotated to the behavioral model. The following STRO-stage parameters are adjusted by users to match the used technology :

— D_{ff} and D_{rr} : the static propagation delay.
— D_{Charlie} : the Charlie effect magnitude.
— D_{Drafting} : Drafting effect amplitude.
— t_{Drafting} : Drafting effect duration.
— $Jitter_{\mathrm{var}}$: the jitter standard deviation, σ, of the propagation delay of one ring stage (*i.e.* the local jitter per ring stage).
— $Jitter_{\mathrm{seed}}$: seed for the random jitter draws.

The high-level simulations have been used to demonstrate the concepts and validate the architecture. It is a simple and a fast method to validate the architectural modifications. Moreover, it allows to estimate the time resolution and to detect the configurations matching with the STRO evenly-spaced mode. These simulations have been performed with ModelSim using parameters extracted from analog simulations performed by Virtuoso analog design environment (ADE) on a 28 nm FDSOI technology. A supply voltage of $1\,\mathrm{V}$ has been used. For an initial configuration, the extracted values are : $D_{\mathrm{ff}} = 24.3\,\mathrm{ps}$, $D_{\mathrm{rr}} = 31.0\,\mathrm{ps}$, $D_{\mathrm{Charlie}} = 5.0\,\mathrm{ps}$, $t_{\mathrm{Drafting}} = 10.0\,\mathrm{ps}$, $D_{\mathrm{Drafting}} = 10$. These temporal parameters depend on the implementation of the STRO stage. The above parameters are extracted for a non-optimized conventional C-element of Fig. 3.9b. This parameter extraction is based on the case when the oscillator is operating with a large value of s (large separation time between the inputs of the C-element), in which the dynamic propagation delays are close to the static propagation delays. Indeed, this can happen for the two cases when the ring is initialized with two tokens or only one bubble, as shown in Fig. 3.16. In fact, in the tokens limited region (one bubble in the ring), the frequency is close to the value $\gamma/2D_{\mathrm{ff}}$. In this case, the measured frequency of the ring allows to get the value of the D_{ff}. Inversely, in the bubbles limited region (only two tokens in the ring), the frequency is close to the value $(1-\gamma)/2D_{\mathrm{rr}}$. Thus, the value of D_{rr} can be obtained according to the value of the frequency.

Fig. 4.13 presents some examples of simulated STRO configurations using the high-level model. In this figure, for each STRO, a phase output is plotted for each configuration. The configurations correspond to the possible cases for an even number of tokens. From the plotted signals, we detect the configuration for which the evenly spaced mode is obtained. Moreover, the time resolution and the maximal oscillation frequency can be estimated. As previously presented, the counters provide the measurement result as P, H, and N_v variables. As example of the measurement process, we can consider a TDC of $L = 9$ stages initialized with $N_T = 4$ for the measurement of a time interval $T = 1000\,\mathrm{ns}$. The obtained oscillation period is $T_{\mathrm{STR}} = 117\,\mathrm{ps}$, which gives a time resolution of $\frac{117}{2*9} = 6.5\,\mathrm{ps}$. The variable results are : $C = 0$, $H = 8$, and $N_v = 17$. As a result, the TDC output is $\mathrm{TDC}_{out} = (17+1)*9-8 = 154$, which means a measured time of $T_m = 1001\,\mathrm{ps}$.

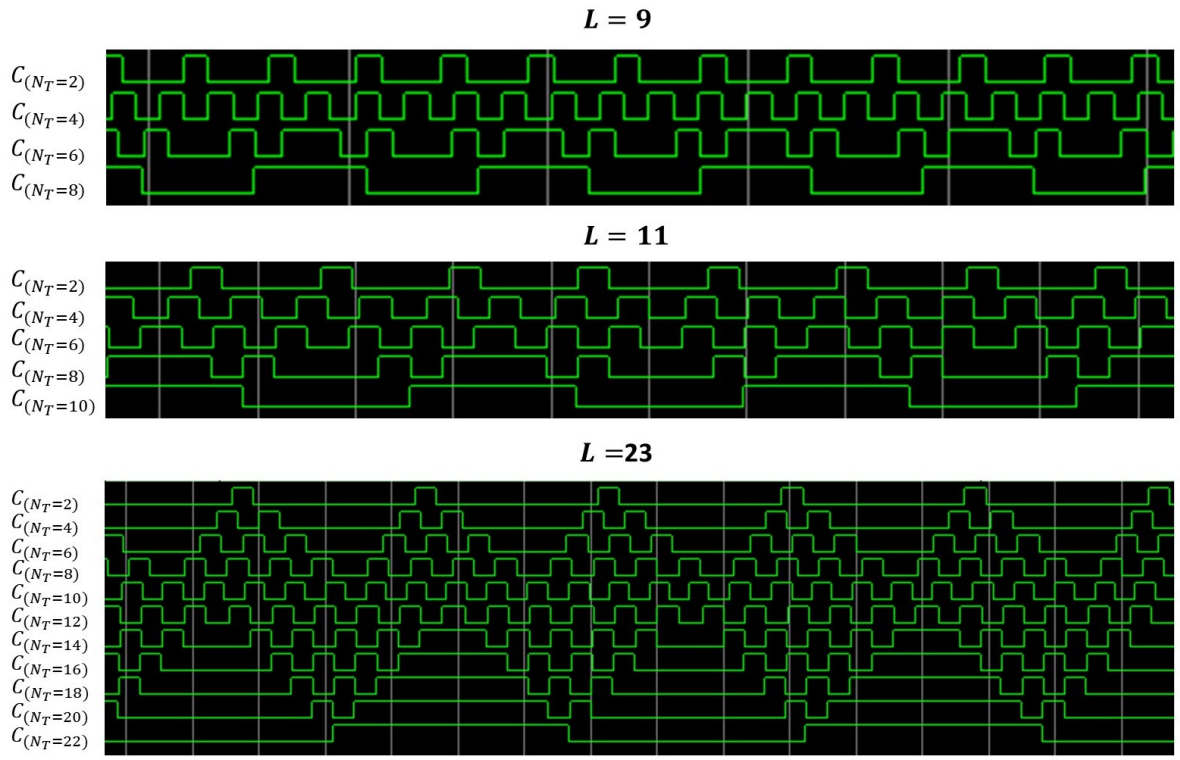

FIGURE 4.13: A phase signal presentation for each configuration with an even number of tokens for the TDCs with : $L = 9$, $L = 11$, and $L = 23$.

4.4.1.2 Noisy environment

The study of the STRO in a noisy environment has already been presented in [15], which reveals the loss of the carried jitter timing variation by events propagating in STRO. The oscillator is few disturbed by the flicker noise since it is usually working at a higher frequency. It can be neglected in the noise performance of the STRO. When the separation time between successive events gets closer to the steady regime, the timing of an event is self-regulated with a value which does not depend on dynamic parameters such as noise in the circuit [15]. The stage jitter is due to its local noise. The main result is that increasing the number of stages allows minimizing the amplitude of jitter, which converges to a noise floor. Moreover, the jitter magnitude is the same for each STRO stage, which means that there is no jitter accumulation. This indicates no noise propagation over the stages and that noise corresponds to the local stage noise. The measured jitter for the STRO is only the random local jitter. This model has been included in our behavioral model.

The TDC is simulated in this noisy environment by adding jitter to the STRO stages. As previously presented, the jitter is implemented using timing variations via $Jitter_{\text{var}}$ and $Jitter_{\text{seed}}$ variables. The obtained distributions follow a normal distribution with a mean value corresponding to the propagation delays measured during the analog simulations and with a configurable standard deviation. The previous simulated 9-stage STRO-based TDC have been used to mea-

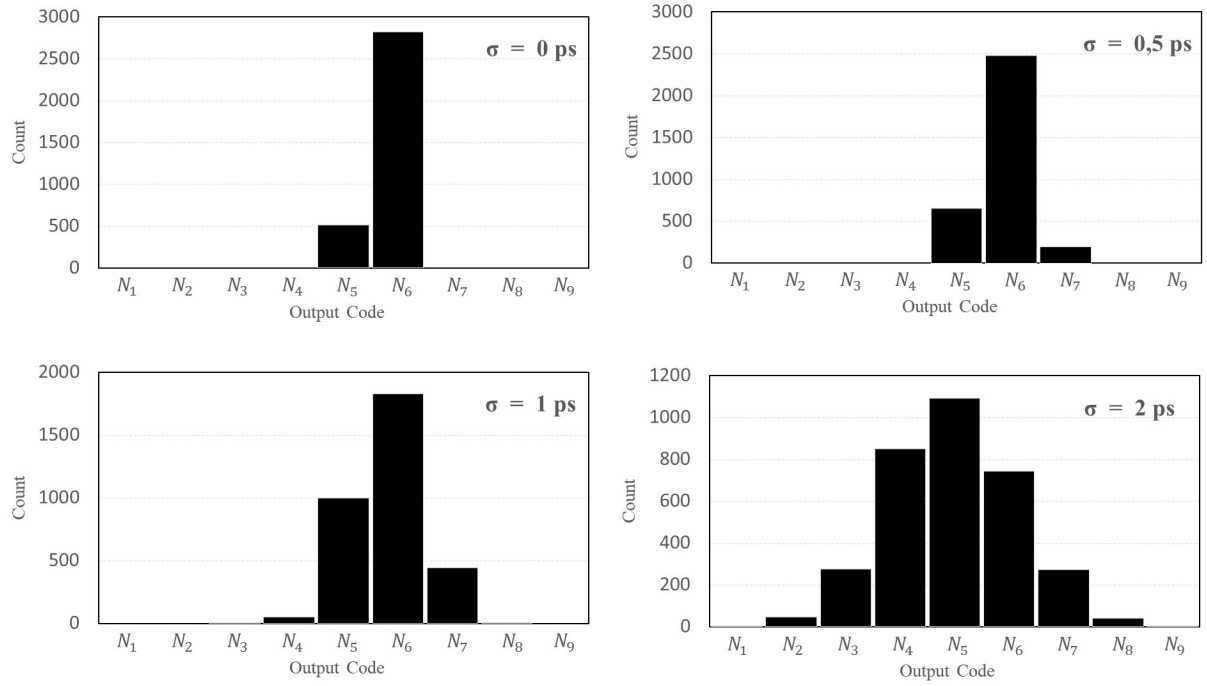

FIGURE 4.14: The TDC output distribution for a fixed time interval T with different values of $Jitter_{\text{var}}$ (the TDC characteristics : $L = 9$, $N_T = 4$, and $Jitter_{\text{seed}} = 100$).

sure an arbitrary time interval T. We fixed the value of the $Jitter_{\text{seed}}$ and measured multiple times T for different values of $Jitter_{\text{var}}$. The real value of $Jitter_{\text{var}}$ typically correspond to around 1 % of the oscillation period. Thus, Fig. 4.14 illustrates the distribution of the counts for each values of $Jitter_{\text{var}}$ chosen in {0, 0.5, 1, 2}. The value of $Jitter_{\text{var}}$ does not largely affect the distributions. The results are concentrated around two values.

Otherwise, we have evaluated the TDC output by modifying the value of $Jitter_{\text{seed}}$ for $\sigma = 1.00\,\text{ps}$. The criterion for selecting this value is the maximal value of jitter variation reported in [15]. The results draw a normal distribution, which is almost the same for the all cases, as shown in Fig. 4.15. As a result, the $Jitter_{\text{seed}}$ has no influence over the TDC results.

According to the above results, we evaluated our proposed STRO-based TDC in a noisy environment as reported in Table 4.3. In these simulations, we measured a 500 ps time interval 200 times for different resolutions $\Delta\varphi$ and for a fixed jitter standard deviation $\sigma = 1.00\,\text{ps}$. The technological parameters have been changed for which the ring stage has the following static delays : $D_{\text{ff}} = D_{\text{rr}} = 35.0\,\text{ps}$. The maximal STRO frequency is $6.13\,\text{GHz}$ ($T_{\text{STR}} = 162\,\text{ps}$). A time resolution $\Delta\varphi = 1.30\,\text{ps}$ (resp. $1.90\,\text{ps}$, $3.60\,\text{ps}$, $9.00\,\text{ps}$, $17.60\,\text{ps}$) was obtained using a 61-stage STR (resp. 41, 23, 9 and 5) with $N = 30$ (resp. $N = 20$, $N = 10$, $N = 4$, $N = 2$). The second and the third columns of Table 4.3 give the percentage of measurements, which result in errors respectively lower than $2\Delta\varphi$ and $\Delta\varphi$ [5]. $\overline{T_m}$ is the obtained mean value from the 200 samples and $\overline{|Err|}$ is the associated error.

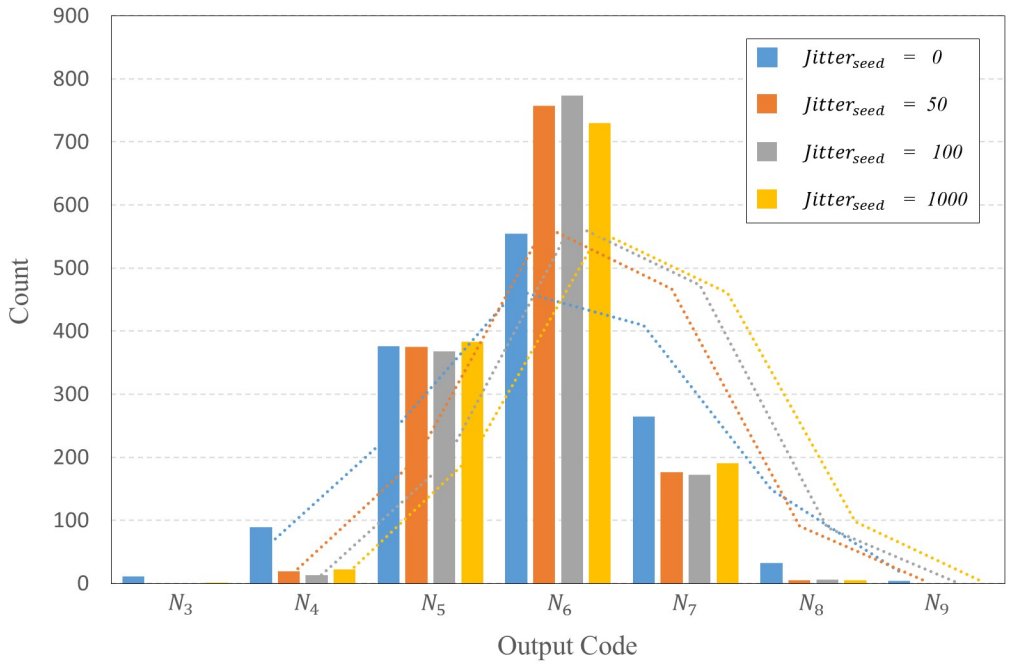

FIGURE 4.15: The TDC output distribution for variable $Jitter_{\text{seed}}$ with their trend curves ($Jitter_{\text{var}} = 1\,\text{ps}$).

As expected, the higher is the ratio $\sigma/\Delta\varphi$, the higher is the influence of noise on the results. For a ratio lower than 28%, all the measurements are correct (the error is lower than $2\Delta\varphi$). This means that on-the-fly measurements can be performed in these configurations. Conversely, for a ratio greater than 52%, only 64% of the measurements are correct. Therefore, computing a mean value using several samples is required to filter the STR noise : on-the-fly measurement is not possible anymore. This study sets the limits for on-the-fly measurement using this TDC for a resolution close to the jitter standard deviation. Fortunately, this is mitigated by the intrinsic very-low jitter in STRs [24].

TABLE 4.3: High-level simulation of a STRO-based TDC measuring a time interval $T = 500$ ps in a noisy environment for different resolutions $\Delta\varphi$, and for a fixed jitter standard deviation $\sigma = 1.00\,\text{ps}$.

L	N_T	$\Delta\varphi$	Percentage of samples with		$\overline{T_m}$	$\overline{\lvert Err\rvert}$
			$\lvert Err\rvert \leq 2\Delta\varphi$	$\lvert Err\rvert \leq \Delta\varphi$		
5	2	17.60 ps	100.0%	93.0%	498.93 ps	1.07 ps
9	4	9.00 ps	100.0%	90.5%	496.03 ps	3.96 ps
23	10	3.60 ps	67.5%	45.0%	496.48 ps	3.52 ps
41	20	1.90 ps	64.0%	34.0%	496.76 ps	3.24 ps
61	30	1.30 ps	43.5%	20.0%	497.41 ps	2.59 ps

4.4.2 Analog simulations

4.4.2.1 STRO results

As reported in Section 3.2, different CMOS implementations have been presented for the C-element gate. An appropriate architecture can be adopted according to the targeted application. The STRO stages are designed with the conventional C-element. The CMOS implementation of the conventional C-element with *Set* and *Reset* signals is shown in Fig. 4.16. The transistors N_1, N_2, N_3, P_1, P_2 and P_3 contribute to the switching of the output. The weak-feedback inverter (N_4 and P_4) is in charge of maintaining the state of the output when the C-element inputs are different. The four additional transistors N_5, N_6, P_5 and P_6 are used to disconnect this weak-feedback inverter when the inputs are equal. Whereas, N_7 and P_7 transistors allow resetting the stage with the *Reset* signal and N_8 and P_8 transistors allow setting the stage to 1 with the *Set* signal.

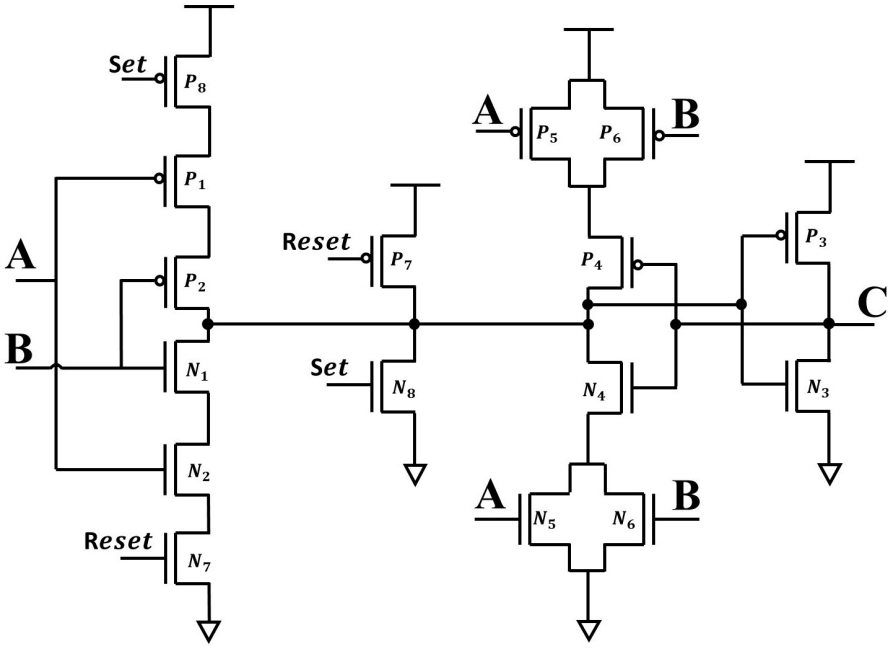

FIGURE 4.16: CMOS implementation of the conventional C-element.

For the STRO, the rising and falling transitions should have almost the same slopes. This is especially relevant for the phase noise definition since they are used to specify the impulse sensitivity function (ISF). An efficient method for sizing the Muller gate is required when designing the STRO. The logical effort, firstly introduced by I. Sutherland and B. Sproull [64] has be implied to optimize the delay in our CMOS TDC. This technique helps to correctly size the transistors of the C-element. As a result, the stage delay is optimized and the STRO oscillates faster. The speed enhancement has a consequence for the phase noise reduction and area optimization as well. In [23], a comparison for different Muller implementations in CMOS 65 nm

technology according to their frequency, power consumption, and phase noise has been done.

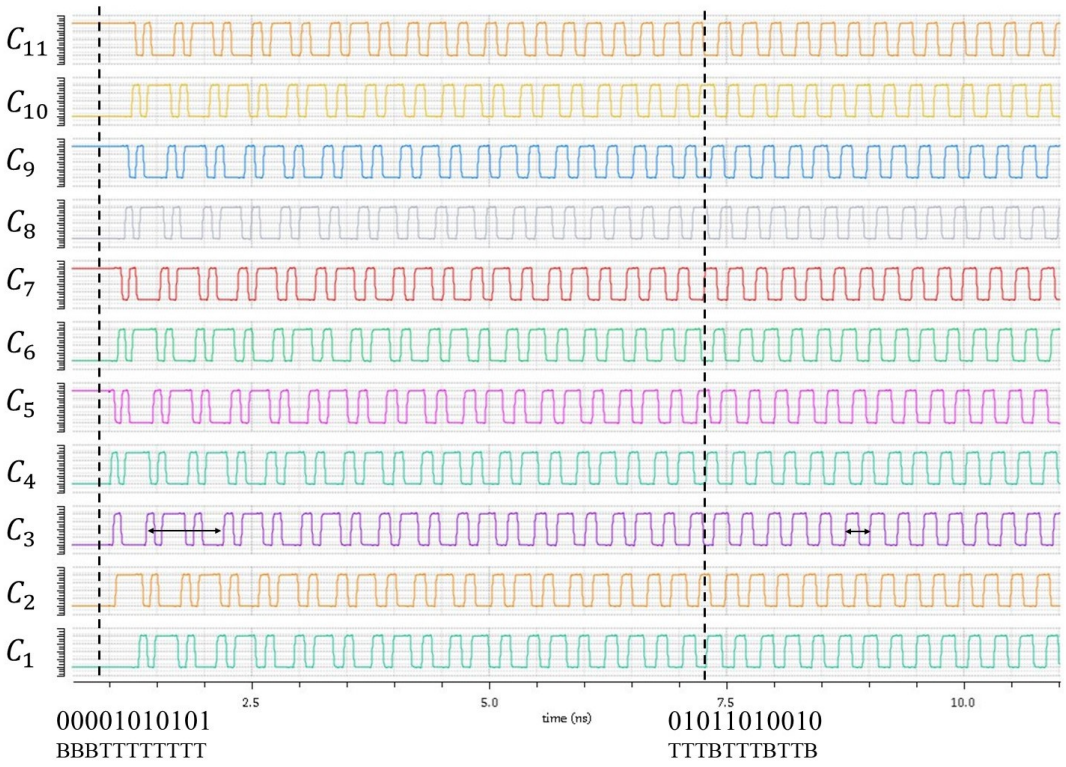

FIGURE 4.17: 11-stage STRO outputs for an initialization of 8 tokens.

A 11-stage STRO circuit based on the Muller gate of Fig. 4.16 has been simulated in 28 nm FDSOI technology. Fig. 4.17 plotted the phase outputs of this STRO initialized with 8 tokens (electrical events) for "BBBTTTTTTTT" configuration (B : "Bubble", T : "Token"), which is equivalent to initial STRO output : 00001010101. Notice that every output starts with a transient period until the events reach an evenly-spaced mode. This phenomenon is mainly due to the analog Charlie's effect that stretch the time between events to make them uniformly distributed in time while they are propagating.

In Fig. 4.18, one phase output is presented for each STRO configuration with a different possible initialization for STROs with $L \in \{9,11,23\}$. The evenly-spaced mode is obtained for all the configurations with different duty cycle for the 9-stage STRO. Unlikely, the 11-stage and 23-stage STROs have many configurations with burst mode. It is more noticeable that for the case of $L = 23$ and $N_T = 16$ the phase starts with a transient regime. Then, it changes the mode to equally spread events over the structure to be an evenly-spaced mode. However, the case of $L = 23$ and $N_T = 20$, the burst mode stills present after the transient regime.

Table 4.4 shows some study cases of the simulated STROs. The frequency value and the duty cycle are reported. For the same occupancy ratio of $\Gamma = 0.45$, the configurations ($L = 9$, $N_T = 4$) and ($L = 23$, $N_T = 10$) have the same frequency and duty cycle but a reduced time resolution. In fact, duplicating the number of stages from 9 to 23 allows to decrease the time

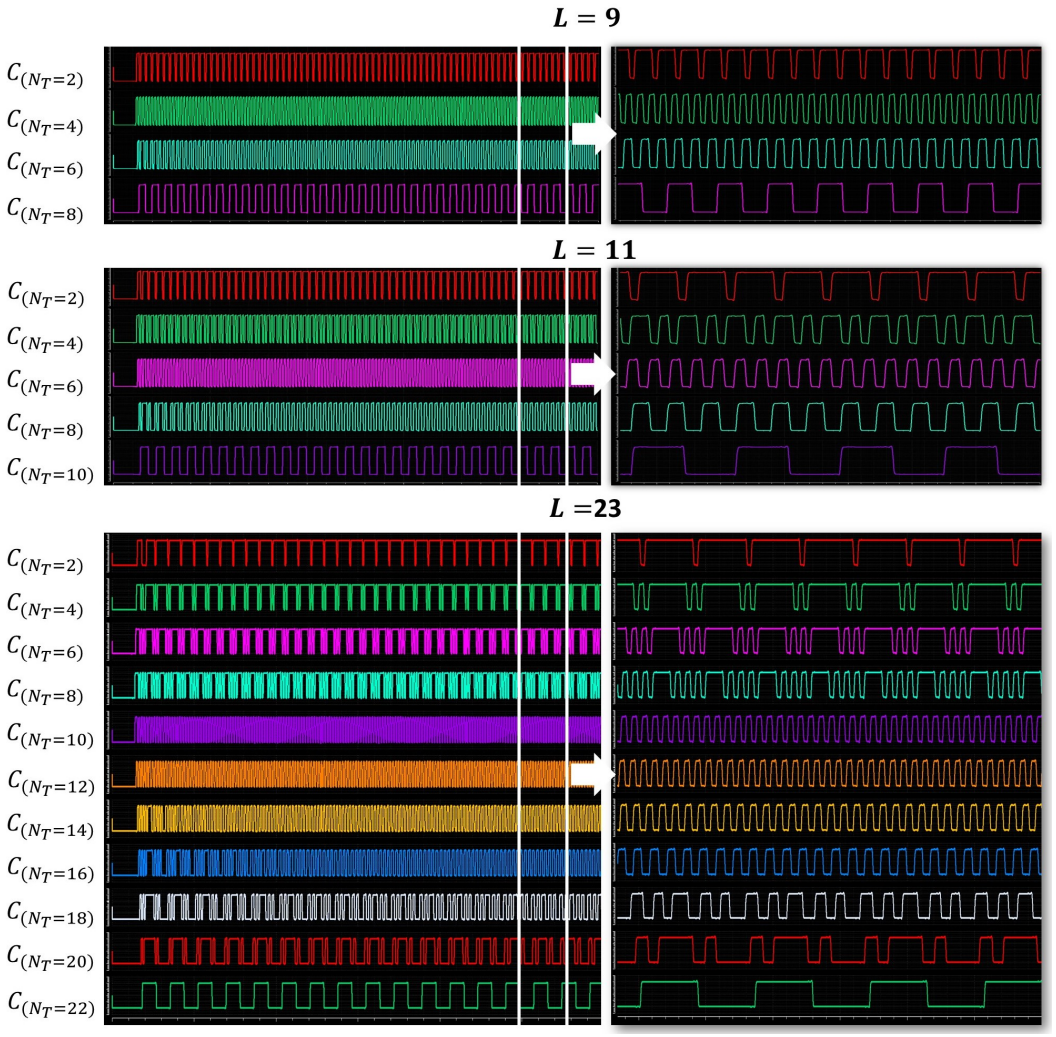

FIGURE 4.18: The phase signal for each possible configuration of an STRO with : $L = 9$, $L = 11$, and $L = 23$.

resolution by 40%. A duty cycle of 50% is obtained by using the maximum number of tokens in the STRO. A fixed time resolution of 37.1 ps has been calculated in this case. Predictably, the frequencies are different since the occupancy ratios are not the same. These configurations operate with the lowest frequency that can be reached by the STRO.

The above simulations have been used to identify the static propagation delays (D_{ff} and D_{rr}) of the implemented C-element. A possible technique to obtain these parameters is to exploit the information from the frequency curve of the STROs. Indeed, for the extreme cases (maximal number of tokens or bubbles), the oscillation frequency has almost the same value as their asymptotes. According to this, the propagation delays can be expressed by :

$$D_{\text{ff}} = \frac{1-\Gamma}{2F_{TL}}, \quad \Gamma = \frac{N_B}{L} \tag{4.10}$$

TABLE 4.4: The frequency, time resolution, and the duty cycle for different STRO configuration simulations in 28 nm FDSOI technology.

L	N_T	mode	frequency	resolution	duty cycle
9	2	evenly	$3.24\,\mathrm{GHz}$	$17.1\,\mathrm{ps}$	$74\,\%$
9	4	evenly	$6.56\,\mathrm{GHz}$	$8.50\,\mathrm{ps}$	$53\,\%$
9	6	evenly	$4.44\,\mathrm{GHz}$	$37.1\,\mathrm{ps}$	$51\,\%$
9	8	evenly	$1.49\,\mathrm{GHz}$	$37.1\,\mathrm{ps}$	$50\,\%$
11	6	evenly	$5.94\,\mathrm{GHz}$	$7.60\,\mathrm{ps}$	$51\,\%$
11	8	evenly	$3.68\,\mathrm{GHz}$	$12.5\,\mathrm{ps}$	$51\,\%$
11	10	evenly	$1.22\,\mathrm{GHz}$	$37.1\,\mathrm{ps}$	$50\,\%$
23	10	evenly	$6.46\,\mathrm{GHz}$	$3.40\,\mathrm{ps}$	$54\,\%$
23	12	evenly	$6.20\,\mathrm{GHz}$	$3.50\,\mathrm{ps}$	$52\,\%$
23	14	evenly	$5.16\,\mathrm{GHz}$	$4.20\,\mathrm{ps}$	$51\,\%$
23	16	evenly	$4.00\,\mathrm{GHz}$	$5.50\,\mathrm{ps}$	$50\,\%$
23	18	evenly	$2.90\,\mathrm{GHz}$	$7.20\,\mathrm{ps}$	$52\,\%$
23	22	evenly	$0.58\,\mathrm{GHz}$	$37.1\,\mathrm{ps}$	$50\,\%$

$$D_{\mathrm{rr}} = \frac{1-\Gamma}{2F_{BL}}, \quad \Gamma = \frac{N_T}{L} \tag{4.11}$$

Considering now the example of 9-stage STRO, the oscillation frequency for an initialization of $N_T = 2$ is $3.13\,\mathrm{GHz}$, which corresponds to the F_{BL}. As a result, the estimated value for D_{rr} is $35.5\,\mathrm{ps}$. Similarly, the estimated value of D_{ff} is $38.5\,\mathrm{ps}$ since the oscillation frequency of the STRO is $F_{TL} = 1.44\,\mathrm{GHz}$ when initializing with 8 tokens ($N_T = 8$). These values have been used for the configuration of the behavioral model presented in the previous section (Section 4.4.1). Connecting a circuit to the STRO may modify the C-element propagation delays due to the fan-out of the circuit (input/output charge). As a result, the oscillation frequency can slightly be modified. Obviously, it is important to keep the same fan-out for the STRO outputs in the TDC design.

4.4.2.2 TDC measurements

The 9-stage STRO-based TDC initialized with 4 tokens has been implemented and simulated to validate the operating principle of the proposed architecture. A time resolution of $8.9\,\mathrm{ps}$ is obtained with a frequency of $6.25\,\mathrm{GHz}$ ($T_{\mathrm{STR}} = 160\,\mathrm{ps}$) using simulations without parasitic extraction. As 4 and 9 are co-prime and (3.9) are satisfied, we get 9 different evenly-spaced phases. According to (3.13), $\Delta\varphi = T_{\mathrm{STR}}/(2 \times 9) = 8.9\,\mathrm{ps}$. If N and L are not co-prime, several outputs share the same phase. Therefore, the finest time resolution of (3.13) cannot be reached when N and L are not co-prime.

Fig. 4.19 plots the staircase of a 9-stage TDC for a resolution of $8.9\,\mathrm{ps}$ giving the TDC output against time to be measured. As it can be seen in this plot, the resulted values of the STRO-based

TDC matches with the ideal expected curve. Covering a large number of measurements, we can generate a ramp input to evaluate the linearity of the system via parameters as DNL and INL. Results reveals that DNL is $\pm 0.437\,\mathrm{LSB}$ and INL is $\pm 0.397\,\mathrm{LSB}$. As an example, Table 4.5 shows the measurement results for different interval values of the *Enable* signal. As it can be seen, the measured interval T_m is equal to the interval T with an error which does not exceed $\Delta\varphi$ ($\mid E_{rr} \mid \leq \Delta\varphi$).

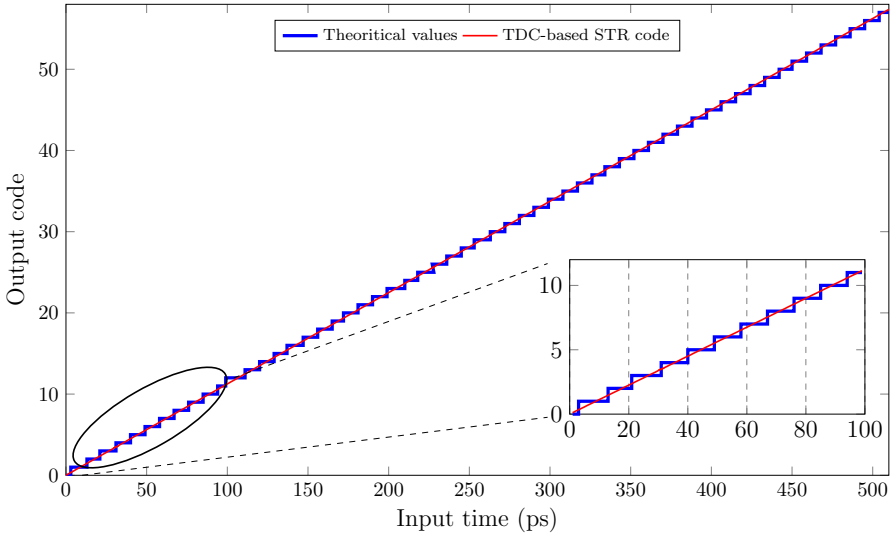

FIGURE 4.19: Simulated TDC output versus input time.

TABLE 4.5: Analog simulation results of a 9-stage STRO-based TDC using $28\,\mathrm{nm}$ FDSOI CMOS technology

T	N_v	P	H	T_m
25 ps	1	1	3	26.7 ps
50 ps	1	1	6	53.4 ps
100 ps	2	0	6	106.8 ps
200 ps	3	1	5	204.7 ps
500 ps	6	1	2	498.4 ps
1000 ps	13	1	4	996.8 ps
2000 ps	25	1	9	2002.5 ps

4.4.3 Linearity in a noisy environment

In order to strengthen the previous study of TDC linearity, we have evaluated the DNL and INL in a very noisy environment in the presence of standard deviation value $\sigma = 1.00\,\mathrm{ps}$ of STRO jitter [15]. Fig. 4.20 shows the measured DNL and INL of this TDC. It is seen that a general DNL variation range is $\pm 0.42\,[\mathrm{LSB}]$. However, peaks are occuring in some output code

ranges which reveals a global DNL value of $\pm 0.85\,[\mathrm{LSB}]$. The INL value is $0.57\,/-0.9\,[\mathrm{LSB}]$, which represents the worst case for linearity of the TDC.

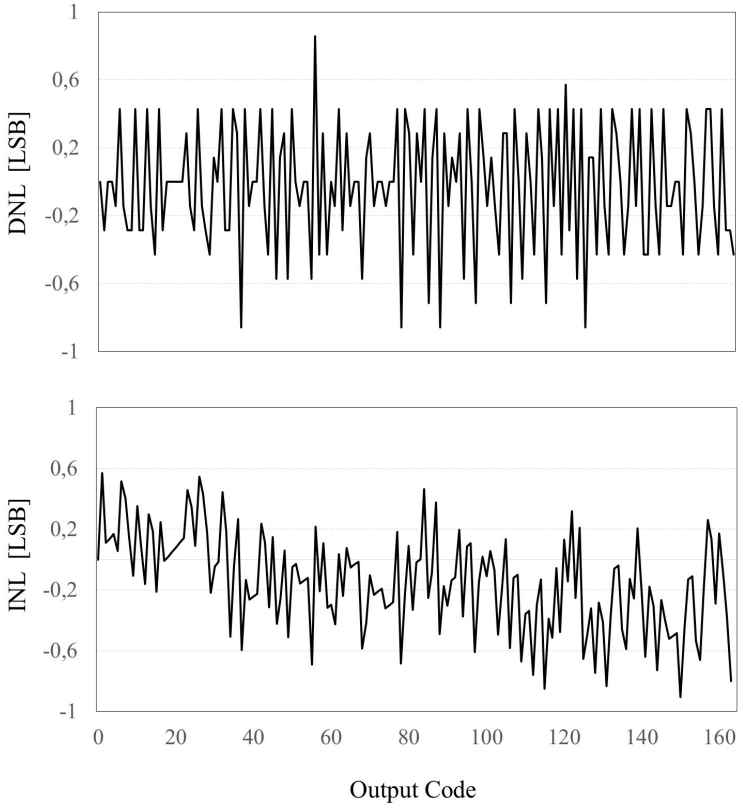

FIGURE 4.20: Simulation results of DNL and INL in the presence of the jitter (standard deviation of $1.00\,\mathrm{ps}$.

4.5 Conclusion

In this chapter, our proposed STRO-based TDC architecture and its working principle are presented and discussed. Thus, the main TDC blocks of this architecture are detailed. The Charlie's effect provides a unique feature to the STRO. This is the strength of our approach because the electrical transitions propagating into the ring become evenly-spaced after the ring was initialization. Therefore, the phase distances are particularly accurate and stable with STROs. This is comparable to an automatic calibration of the distance between the phases. No calibration is required at this level. The only limitation to the TDC precision is the stage jitter of the STRO. A sub-gate time resolution is obtained by simply increasing the number of stages. In addition, the TDC is based on a simple comprehensive measurement scheme and its implementation is straightforward.

A proof-of-concept has been implemented and simulated to validate the proposed architecture. The linearity of the TDC in a noisy environment has been considered. They confirmed the

accuracy of the measurements, which can opens new perspectives for applications requiring on-the-fly measurements with a fine resolution (*e. G.* jitter measurements and instrumentation). To further validate the proposed architecture, an FPGA implementation of this TDC is presented in the next chapter.

Chapitre 5

FPGA-based TDC validation

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5.1 Introduction

For applications, where chip fabrication is too expensive due to a limited number of items or just for prototyping, an FPGA-based approach is usually the perfect trade-off, except if high-precision timing measurements are necessary. Many literature propositions presented TDC implementations into an FPGA with interesting results. This can be an alternative for lower manufacturing cost and shorter development time.

This chapter proposes a TDC implementation in a low-cost FPGA : Intel Cyclone IV. We demonstrate that our proposed TDC is able to achieve a time resolution as fine as needed by simply increasing its number of stages, *i.e.* the number of phase outputs. Even if the achievable time resolution with an FPGA-based TDC is close to the tenths of picoseconds, the approach does not require a high frequency oscillator. The resolution is only limited by the STRO-stage noise in the FPGA. We propose a method for implementing the STRO-based TDC architecture. This architecture is slightly modified compared to that presented in the previous chapter.

As a hardware proof-of-concept, a 23-stage and 141-stage STRO-based TDC have been implemented as an illustration of the TDC with a larger and a finer time resolution. The results are obtained by a one-shot measurement without averaging. Compared with other FPGA-based TDC structures, the proposed TDC is compact and does not require complex circuitry. Measurement results are promising and points out the advantages of this new TDC in terms of measurement accuracy and simplicity of implementation.

5.2 FPGA-based TDC literature

TDCs are implemented as application-specific integrated circuits (ASIC) or field programmable gate arrays (FPGA). Most of them are integrated as an ASIC in order to benefit from the high advances of CMOS technologies and to reach fine time resolutions [7, 13, 19, 34–37, 42, 44, 44, 46, 51, 57, 63, 68, 76, 79]. Moreover, the total control of the place-and-route process contributes to limit the measured differential nonlinearity (DNL) and the integral nonlinearity (INL). However, the ASIC devices present a long development cycle. They are expensive, especially for small productions and dedicated products. Conversely, the FPGA-based TDCs benefit from lower cost due to their short development cycle. They present a good flexibility for further improvements, reconfiguration and verification. In addition to the implemented TDCs, many other digital blocks can be included in the same FPGA to perform more complex applications. They are good candidates for multichannel TDCs [11, 70] and are frequently used because they offer a good trade-off between ASIC and processor-based systems.

Most of the TDCs implemented in an FPGA are based on the dedicated carry chains, which

are a powerful resource to perform the delay line [9,17,18,54,67,73,74,80]. They adopt the same principle, which is based on a coarse measurement using n-bit counter and a fine measurement made with another technique ensuring a fine quantization step. Therefore, the FPGA-based TDC structures are simple and can be implemented in any FPGA since it is based on fast carry-logic resources.

5.2.1 Carry chain

The tapped delay line (TDL) is the most proposed TDC architecture in the literature implemented in FPGAs [11]. It is a simple architecture based on cascading stages composed of a delay element and a register. Thus, a stage can be implemented in a logic element (LE), which is composed of a look-up table (LUT) and registers. The TDL has been developed to achieve a fine resolution using techniques such as a Vernier delay line (VDL) [11,40]. It is usually driven by the system clock and employs a counter to define the coarse measurement while interpolating status of registers for the finer measurements. However, the main issue of this structure is the non-uniform delays of the stages. This required a stage fine-tuning and a calibration of the TDC. Moreover, the linearity is usually sub-optimal due to the large values of the DNL and INL. Indeed, the delays between two successive stages can dramatically increase when the structure has to cross two adjacent LABs, which is difficult to manage due to the impossibility to control the place-and-route operation (the P&R tool do it automatically). Moreover,the software optimization made by the dedicated CAD tool is able to make unwanted changes, such as removing the delays (if it is not specified) or implementing one stage over several LUTs.

5.2.2 Wave union

In order to improve the precision using the TDL technique, the wave union method has been successfully demonstrated in FPGA devices [77]. This method can improve the bin widths and reduce the uncertainty. In fact, after the coarse measurement, a set of hits are propagating in the same TDL during the residue time of the first quantification. Indeed, this method allows doubling the number of measurements many times, which allows to subdivide the ultrawide bins for each raw measurement [77]. It is similar to a physical TDL with small slices, which allows improving the measurement precision [75].

Further improvements have been done to enhance the wave union method, which has the name of wave union B. The latter is based on a ring oscillator composed of one NAND gate and one inverter. The principle stills the same as the simple wave union while duplicating the rising edge of the signal to be measured, which ensures repetitive measurements. This division is possible for wide bins available on low-end FPGAs that are not dotted with advanced processes [70]. Furthermore, this method increases the dead time [75].

An advanced version of this method, called dual-sampling method has been proposed specifically for ultra-scale FPGAs [71]. It duplicated the taps of the TDL in order to increase the precision of the measurements. Instead of propagating the hit signal into a delay line, Chen *et. al.* [11] proposes to propagate the reference clock in a series of delay elements in order to create multiple delayed clock quantization. Thus, parallel measurements can be realized. Similarly, the input signal is duplicated and delayed. The equivalent structure sounds like a two-dimension Vernier. The resolution corresponds to the cell delay by which the clocks have been delayed. A TDC has been implemented in Altera Stratix V. The phase resolution of the delayed clocks is $25\,\mathrm{ps}$ using a PLL of 5 delay elements for each clock (10 clocks). The TDC has been duplicated 5 times to average the output. Thus, 31% of the logic has been used. The RMS resolution has been reduced from $17.13\,\mathrm{ps}$ to $6.72\,\mathrm{ps}$ due to the multiplication by 5. The quantization error is present in this structure due to the non-uniform delays distributed to the clocks. Using multiple TDCs in the same FPGA reduces this error by averaging the outputs and enhances the RMS resolution at the same time. The TDC suffers from a large dead time of $19.75\,\mathrm{ns}$. The measured DNL (resp. INL) is $3.60\,\mathrm{LSB}$ (resp. $3.23\,\mathrm{LSB}$).

5.2.3 Vernier RO-based TDC

In [40], the carry chain has differently been exploited. The TDC processed the coarse measurement using 32-bit counter then the fine time measurement has been carried out by two delay lines as a Vernier structure with 63 delay elements. This Vernier demonstrated a time resolution of $200\,\mathrm{ps}$ within $10\,\mathrm{ns}$ of dynamic range. The paper states a use of 93% of the logic cells on the FPGA chip.

Based on the same principle of the Vernier, two ring oscillators using carry chains have been implemented on the TDC architecture in [17]. The ring oscillators operate with very small frequency differences. This gives a time resolution of $31\,\mathrm{ps}$ (for 53 bins and a clock period $1.667\,\mathrm{ns}$). The TDC has been implemented in Altera Stratix III.

5.2.4 Pulse shrinking method

The pulse shrinking method has been explored [66, 81]. Based on the *Start* and *Stop* signals, a pulse generator block provides a pulse for which the rising edge is the *Start* event and the falling edge is the *Stop* event. The difference between the propagation time of the rising and the falling edges in the noninverting buffers reduces the time width of the pulse after each cycle by a constant value, which is the difference between the rising and the falling times. This time difference gives the resolution of the converter. [66] proposed a cyclic structure for which this pulse propagates on the delay line while increasing the counter value until vanishing. The block diagram of this structure is displayed in Fig. 5.1. In the same paper, the authors proposed two-stage pulse shrinking TDC based on the previous approach. The time resolution has been

improved from $920.0\,\mathrm{ps}$ to $41.8\,\mathrm{ps}$.

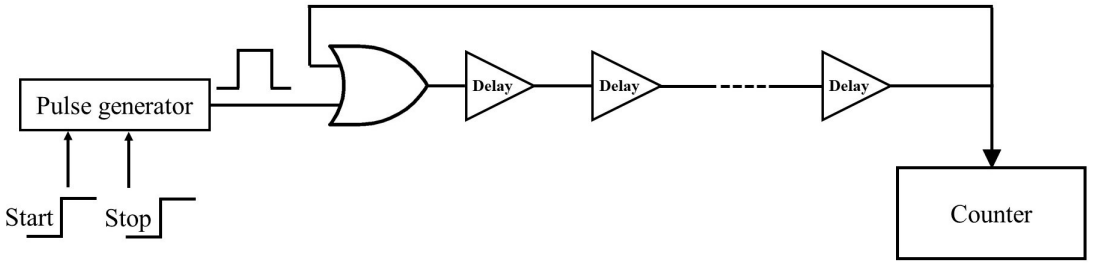

FIGURE 5.1: Block diagram of the TDC based on cyclic pulse shrinking.

A TDC combining the pulse shrinking and the Vernier structure has been proposed in [81]. The rising edge of the *Start* signal propagates on the first loop while the falling edge of the *Stop* signals propagates on the second loop as displayed in Fig. 5.2a. In order to improve the resolution and the conversion time, a two-stage method has been proposed. The corresponding timing diagram is drawn in Fig. 5.2b, showing the same principle as RO-based Vernier. In this structure, successive taps are considered until that the two lines are in phase, which allows shrinking the time interval. A time resolution of $8.5\,\mathrm{ps}$ has been achieved by implementing the TDC in the SmartFusion board of Actel.

5.2.5 Harmonic ring

The Harmonic ring has already been presented in Section 2.4. However, in the FPGA implementation the custom inverters are not feasible. The principle of this proposition is to deploy an inverter ring oscillator with odd number of stages. Three harmonics are added to the ring by forcing the output of the inverters. To ensure the oscillation with the same oscillation frequency for all harmonics, the same edge has to repeatedly go through a node with a different edge type. In other words, a falling edge crossing a node i has to go through this node with a rising transition the next time. A ring of 35 inverters was implemented in an FPGA with a time resolution of $347.0\,\mathrm{ps}$. Unfortunately, the paper does not state more information about the measurements except the time resolution.

5.2.6 Conclusions and discussions

Despite all the presented advantages, the main issue of the FPGA-based TDCs is the high nonlinearity related to their sampling clock skews and to their carry-chain non-uniform physical delays. The nonlinearity greatly affects the TDC performances. They present a nonlinearity of nearly one least significant bit (LSB) or even more compared to the ASIC-based TDCs which can achieve better linearity generally lower to one LSB [11,13]. In order to reduce this nonlinearity, techniques such as the dual-phase method have been devised [73]. Generally, careful place-

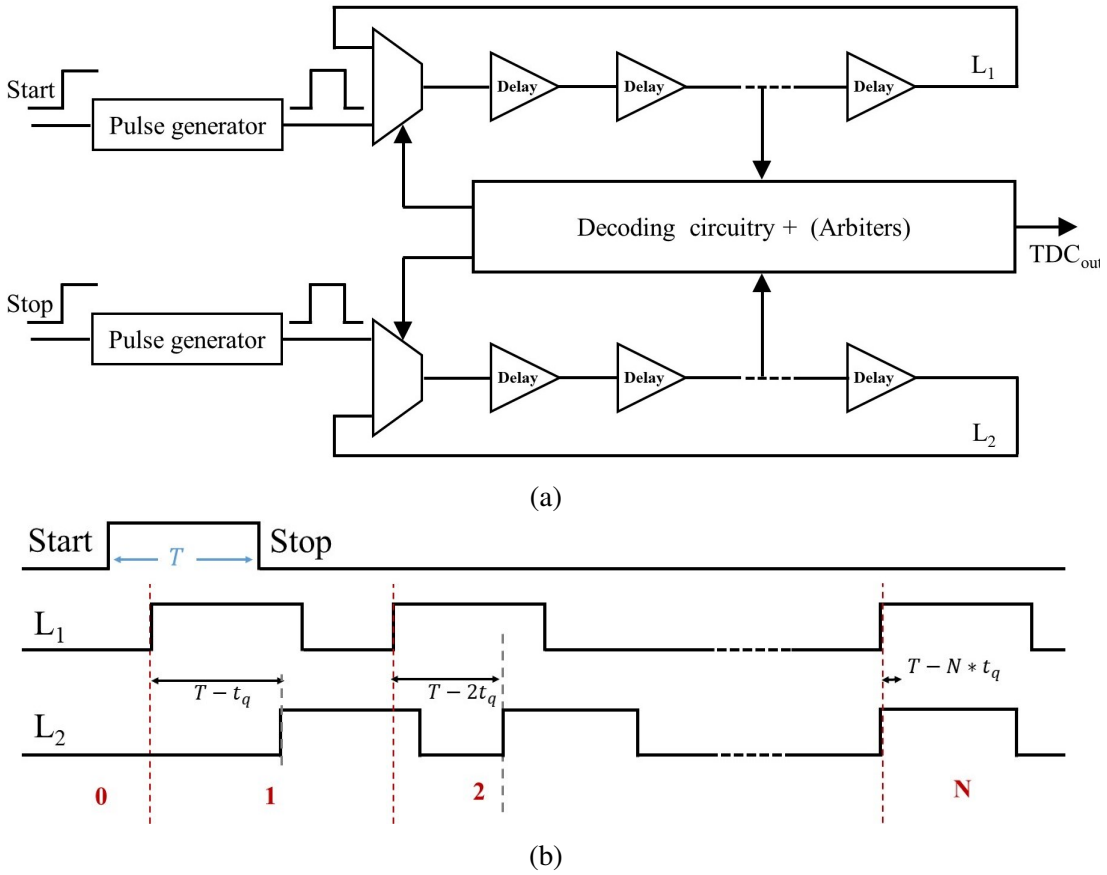

FIGURE 5.2: (a) Architecture of a Vernier-TDC based on delay line loops with shrinking method (b) timing diagram showing the operation principle of the shrinking TDC.

and-route constraints should be considered for the TDC implementation in FPGAs. Moreover, online or offline calibration processes are required to limit the effects of the static nonlinearities generated by the non-uniformity of TDLs as well as the clock distribution [13]. Moreover, all the presented structure request a calibration method even though it is not directly declared.

5.3 Architecture of the proposed TDC

5.3.1 FPGA implementation constraints

There are many different types of FPGA boards. The most known are Xilinx and Altera (subsidiary of Intel now). The FPGAs differ in the number of the configurable logic blocks (CLBs), called also logic elements (LE), which are an important specification of the FPGA. In addition, they differ in the process technology, which can provide different results in two different FPGAs for the same implemented circuit. In fact, not only the process technology can distort the study but also different responses can be obtained, due to the place-and-route tool, after every compilation in the same FPGA.

Otherwise, the supply voltage and the temperature variations, that are not usually stable, may

deteriorate the linearity of the TDC circuit. Since delays are sensitive to these environmental conditions, the measurement may be biased. The non-perfect FPGA power supply adds extra variation to the jitter, which effects as well the TDC measurement results.

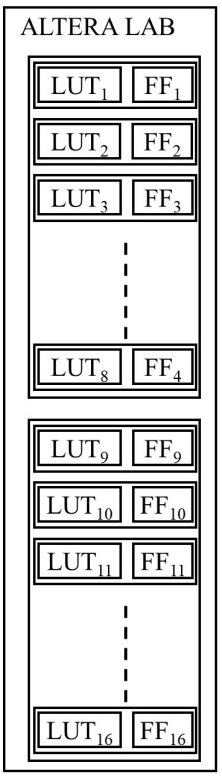

FIGURE 5.3: Intel Cyclone IV Logic Array Block (LAB) architecture.

In our case, an Intel Cyclone IV, which is considered as a low-cost hardware solution. As shown in Fig. 5.3, the used FPGA is composed by a group of LABs. Each LAB contains 16 logical cells including one look-up table (LUT) and one flip-flop. An example of the Intel Cyclone IV logical element is displayed in Fig. 5.4. A set of LABs are placed in columns. A group of columns, no more than 14 columns, are separated by digital signal processing (DSP) or memory columns.

The Quartus II synthesis tool automatically attributes stages into LABs. When stages, as delay elements, have to be close to each other, the synthesis tool may place them in different LABs with a random probability (*e. g.* a FF can be placed differently from its corresponding LUT). Therefore, the delays between these stages can be extended and generate unwanted responses. To reduce this effect, a placement constraint should be used by forcing the tool to place the stages at the right place. The Chip Planner, included in the Quartus tool, allows placing components into regions from compilation-to-compilation, which allows reducing the compilation time as well. Indeed, programming the QSF file allows placing blocks in the FPGA. This option is valuable for implementing the STRO, which is more sensitive to delays as it can be seen in the sequel.

Despite this alternative, Intel devices do not offer a routing access, which is required for controlling the FPGA routing matrix. Thus, the routing is not completely controlled. In fact, the delays between vertical routing and horizontal routing are different, and the delays between adjacent LABs are not equal. Moreover, it is hard to measure these delays directly and the simulation results are not reliable. The counters and the STRO are both timing critical parts of the TDC. Indeed, the interconnection, between the counters and the STRO outputs, has to take into account the discussed constraints in order to minimize the added delays to the STRO phases C_i.

5.3.2 STRO implementation

Conventionally, the output C of the C-element gate is modeled by the following equation :

$$C = A \cdot B + A \cdot C^{-1} + B \cdot C^{-1} \tag{5.1}$$

where C^{-1} represents the previous state of the output C. A and B are the two inputs of the C-element gate. A simple implementation using combinational logic is possible. Thus, an STRO stage can be integrated into a single LUT in the FPGA. Regarding the C-element memory function, it can be realized by connecting the output C to the input C_{loop}. Fig. 5.4 illustrates the C-element gate implementation in one LUT. Consequently, according to the FPGA LABs structure and the number of STRO stages, two structures are possible :

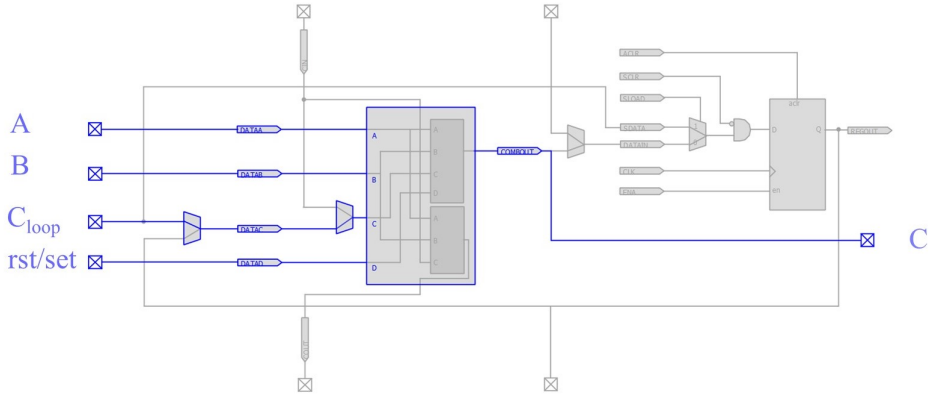

FIGURE 5.4: The implementation of the C-element into a look up table (LUT) in Intel Cyclone IV showing the logical cell of the LAB.

— The first structure integrates all the stages in the same LAB in order to minimize the propagation delay between the STRO stages. During the synthesis of the circuit, each STRO stage is assigned to one logical cell. As a LAB in Intel Cyclone IV just contains 16 logical cells (shown in Fig. 5.3), an STRO of 16 stages can be implemented in this structure. A maximal frequency of $T_{\mathrm{STR}} = 565.5\,\mathrm{MHz}$ can be achieved in this case due to the internal routing process within the same LAB.

— In the second structure, each STRO stage is assigned to different LABs in order to ensure the same propagation time for all the STRO stages. Vertical, horizontal, or loop structures are possible. A special attention should be paid to the cell placement. Indeed, if the placement is not uniform, different results from a compilation to the next one can be obtained even though the structure is kept the same.

Fig. 5.5 shows the curve of the measured frequency of a 9-stage and a 31-stage STROs as function of the tokens number and according to different structures. These results are closer to the expected response as shown in Fig. 3.18. To minimize delays, since the routing is not controlled, the programmed LABs have to be close to each other. It happens that if one connection between stages takes a longer path, this introduces a larger propagation delay for a specific stage. In this case, the frequency is impacted by this delay, and a bottleneck phenomenon can appear. This is even more noticeable with the vertical structure of Fig. 5.5b, which is essentially due to the connection between the first and last stage of the loop. It seems that this phenomenon is not restricted to the vertical structure because it is able to randomly occur due to the non-controllable routing on the FPGA.

5.3.3 The proposed TDC architecture and implementation

According to the temporal parameters of the stages implemented in the FPGA, a frequency is fixed. Therefore, as described by (3.13), the length L of the ring is defined according to the targeted time resolution. Fig. 5.6 illustrates our proposed STRO-based TDC architecture in which an STRO of L stages is used to generate the uniform distributed phases. The events in the ring are initialized using *Init_STR* signal generated by the finite state machine (FSM), which is synchronous to the internal clock of the FPGA. Two types of STRO stages are used : for the initialization, the first one sets its value to 1, and the other one resets its output to 0. In fact, when the signal *Init_STR* goes low (when the STRO starts), it triggers the stages to the initialization process. Then, when the state of the signal *Init_STR* goes back to high, the STRO begins to oscillate in a free running mode.

Two FSM states are used to generate the *Start* and *Stop* signals, spaced with a time equivalent to one clock period. In fact, to vary the time spacing between these two events, we can vary the period of the FSM clock using an external clock. Each measurement requires to reset the FSM, which only ensures a one-shot measurement.

As already presented in the previous chapter, one arbitrary STRO phase is connected to an n-bit counter and the $L-1$ others are connected to 2-bit counters. The TDC output ($\mathrm{TDC_{out}}$) is given by a data processing algorithm based on the collected data from the n-bit counter, Hamming, and M Parity blocks.

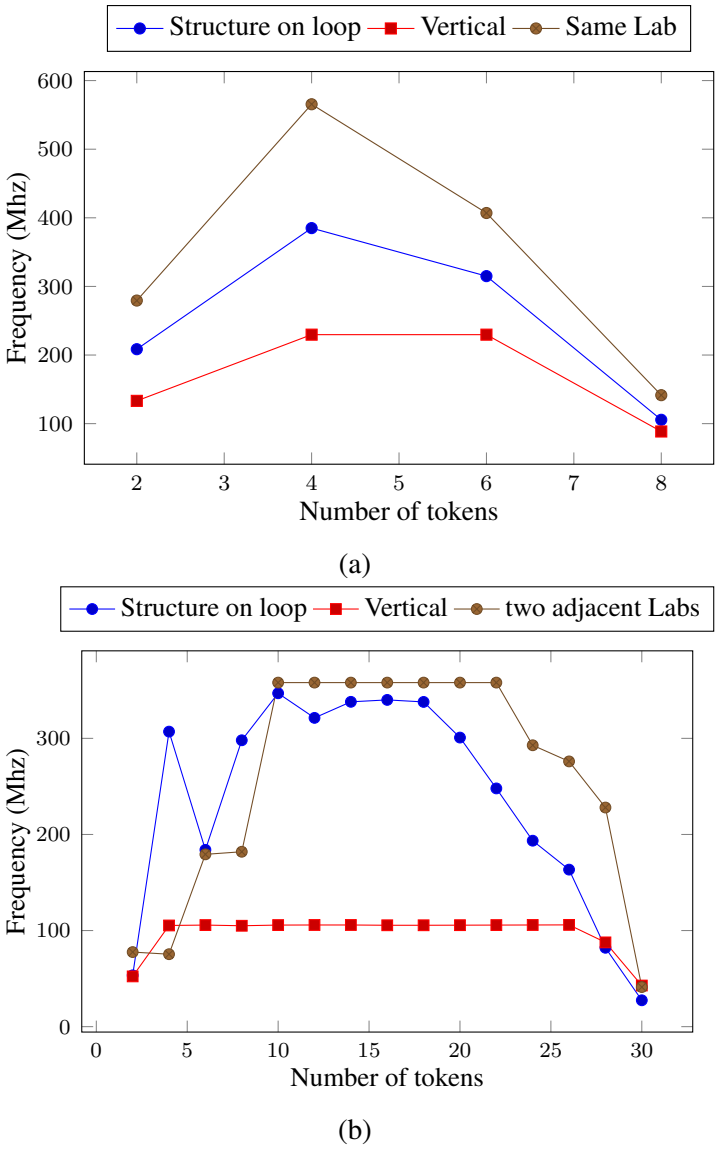

FIGURE 5.5: Measured frequency with different structures implemented in Cyclone IV FPGA for : (a) 9-stages STRO, and (b) 31-stages STRO.

5.3.3.1 Counter implementation

According to the desired dynamic range and the resources of the FPGA, the number of the counter bits can be set. Fig. 5.6 shows the proposed architecture based on an L-stage STRO oscillator with a 5-bit counter and 2-bit counters. Since we present a proof-of-concept, we chose 5 bits for the n-bit counter. On the other hand, in Intel Cyclone IV, a LAB can only accept two clock inputs, which limits the implementation optimization. In fact, each STRO stage has to be implemented with its counter in order to guarantee the same delay between the STRO stages and the counters. Unfortunately, due to the limited number of LUT in the LAB, only the loop structure can be an adequate solution. Fig. 5.7 presents a special loop structure minimizing delays between STRO stages. The used asynchronous counter does not need to be entirely im-

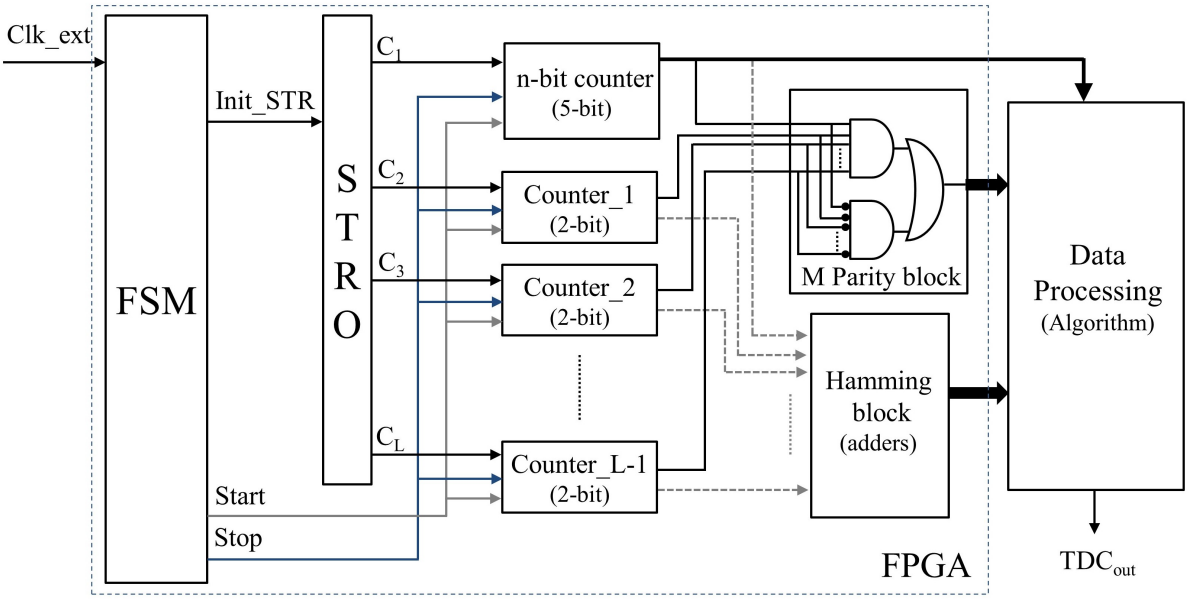

FIGURE 5.6: Composition of the proposed TDC architecture using STRO of a L stages.

plemented in the same LAB as the Muller gate : just the first bit has to be included in the same LAB and the other bits can be affected to the adjacent LABs. In order to consider both rising and falling edges, the counters have been duplicated so that one is operating with the rising edge and the other one with the falling edge. This increases the area of the proposed TDC but, at the same time, ensures a finer resolution.

The counter input frequency, which is related to the STRO frequency, is generally high than the operating frequency of the counters in the FPGA. This issue is not sufficiently discussed in the literature for similar architectures (they present lower frequencies), such as ring oscillator. In this case, the design of the counters seems to be more sensitive than the clock reference itself. To overcome the issue within the FPGA, the delay of the Muller gate has to be enlarged, which decreases the frequency. Thus, the inverted input of the Muller gate has to be designed with a long delay inverter. Otherwise, buffers can be inserted between stages. The STRO frequency is also sensitive to the fanout of their outputs. It shows a variation of the frequency for different output loads. Placing buffers between the STRO and the counters helps to compensate the fanout effect on the STRO oscillation.

5.3.3.2 Hamming and M Parity blocks

The Hamming and M Parity blocks can be made by dedicated hardware circuits, as described in the previous chapter, or left for an software implementation. In fact, viewing that hardware adders are much faster than soft ware, we simply have used adders in our implementation for the Hamming block. Likely, the M Parity block is a simple circuit because it requires just some combinatorial gates as shown in Fig. 5.6.

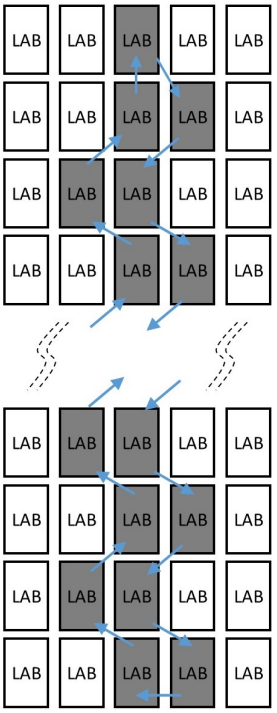

FIGURE 5.7: Implementation topology of a STRO of more than 16 stages (each stage on a single LAB).

5.4 Experimental results

5.4.1 The measurement environment

A 23-stage and 141-stage STRO-based TDCs have been implemented in the EP4CE115F29C7 Intel Cyclone IV, shown in Fig. 5.8. The $50\,\mathrm{MHz}$ on-board crystal oscillator has been used as the clock reference for the FSM (connected to the $\mathrm{Clk\_ext}$ signal). Alternatively, in order to characterize the nonlinearity of the TDC, an arbitrary waveform generator DG5072, with a maximal frequency of $70.0\,\mathrm{MHz}$, has replaced the on-board oscillator. This device generates a square wave connected to the FPGA board via a SMA connector. A standard deviation of $100.0\,\mathrm{ps}$ has been measured for this external input. For an accurate frequency measurement, Low Voltage Differential Signaling (LVDS) outputs have been used with differential oscilloscope probes. This technique aims to reduce the impact of slow input/output circuitry and parasitic effects of the output. A direct measurement of the TDC outputs is applied without any calibration process. The results are directly displayed on the 7-segment displays.

5.4.2 Measurement results

5.4.2.1 23-stage STRO-based TDC

The 23-stage STRO-based TDC has been initialized with 14 events. A theoretical time resolution of $108.7\,\mathrm{ps}$ is obtained with a frequency of $200.0\,\mathrm{MHz}$ ($T_{\mathrm{STR}} = 5.0\,\mathrm{ns}$). As 14 and 23 are

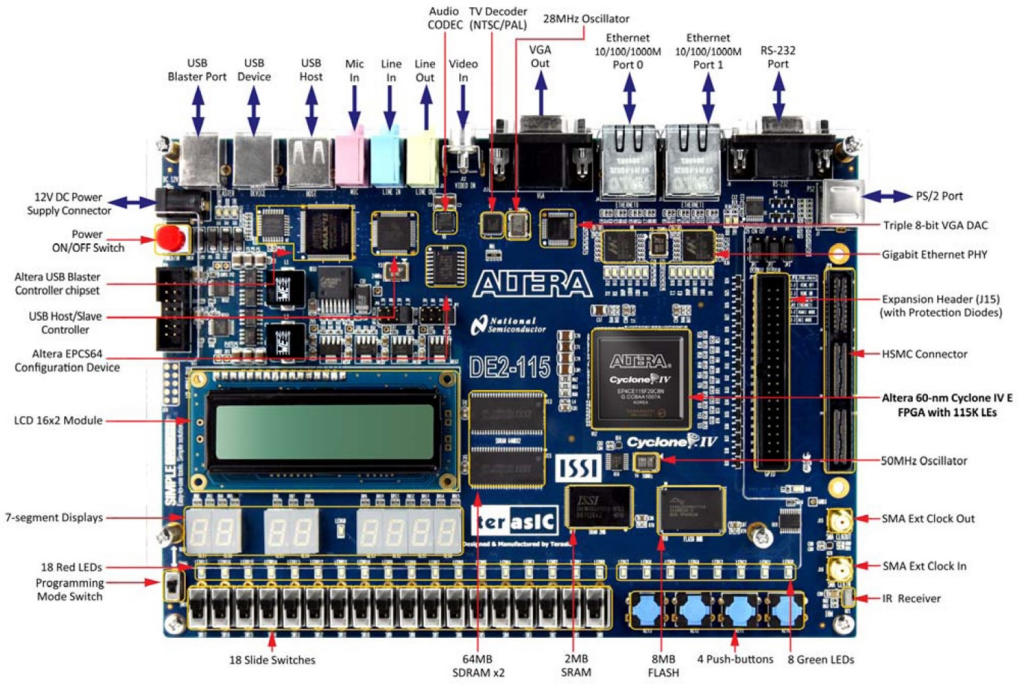

FIGURE 5.8: The top view of the DE2-115 (EP4CE115F29C7) Intel Cyclone IV board (from the user manual).

co-prime, we had 23 different evenly-spaced phases. A repetitive one-shot measurement for approximate time interval values of $9.5\,\mathrm{ns}$ and $13.0\,\mathrm{ns}$ have been done in order to characterize the TDC output. 300 measurements have been collected for each time interval. The time intervals have been defined using coaxial cables with different length.

Fig. 5.9a and Fig. 5.9c plotted the histogram of the resulted digital TDC outputs in both cases. The measured values are more concentrated around 88 for $9.5\,\mathrm{ns}$ (with a standard deviation of $1.4\,\mathrm{LSB}$) and around 119 for $13.0\,\mathrm{ns}$ (with a standard deviation of $1.6\,\mathrm{LSB}$). According to this, we can express differently the results by identifying the percentage of measurements which resulted in an error lower than $\Delta\varphi$, $2\Delta\varphi$ or greater than this. A classification according to the ratio error over the time resolution $\Delta\varphi$ reveals that more than 75% (resp. 70%) of the measurements are correct ($\|Err\| \leq 2\Delta\varphi$) and the mean value is around $9.59\,\mathrm{ns}$ (resp. $12.94\,\mathrm{ns}$) in the case of $T = 9.5\,\mathrm{ns}$ (resp. $T = 13.0\,\mathrm{ns}$). In fact, the measurement errors on the TDC output are due to many sources. One of the primary error sources, which is inherent to any converter, is the quantification error. In fact, for an ideal TDC, the input and output are related by : $T = T_m + \varepsilon$ ($-\Delta\varphi/2 \leq \varepsilon \leq \Delta\varphi/2$). Otherwise, the produced time interval T by the FSM is able to generate some timing noise due to the routing effects. Moreover, using an external clock reference may also present jitter.

In order to demonstrate the linearity of the proposed TDC, a range of measurements from 110 to 460 with a sampling step of $100\,\mathrm{ps}$ has been performed. The obtained INL plot is shown in Fig. 5.10. The implemented TDC shows an INL of $2.17\,[\mathrm{LSB}]$ and a DNL of $1.33\,[\mathrm{LSB}]$.

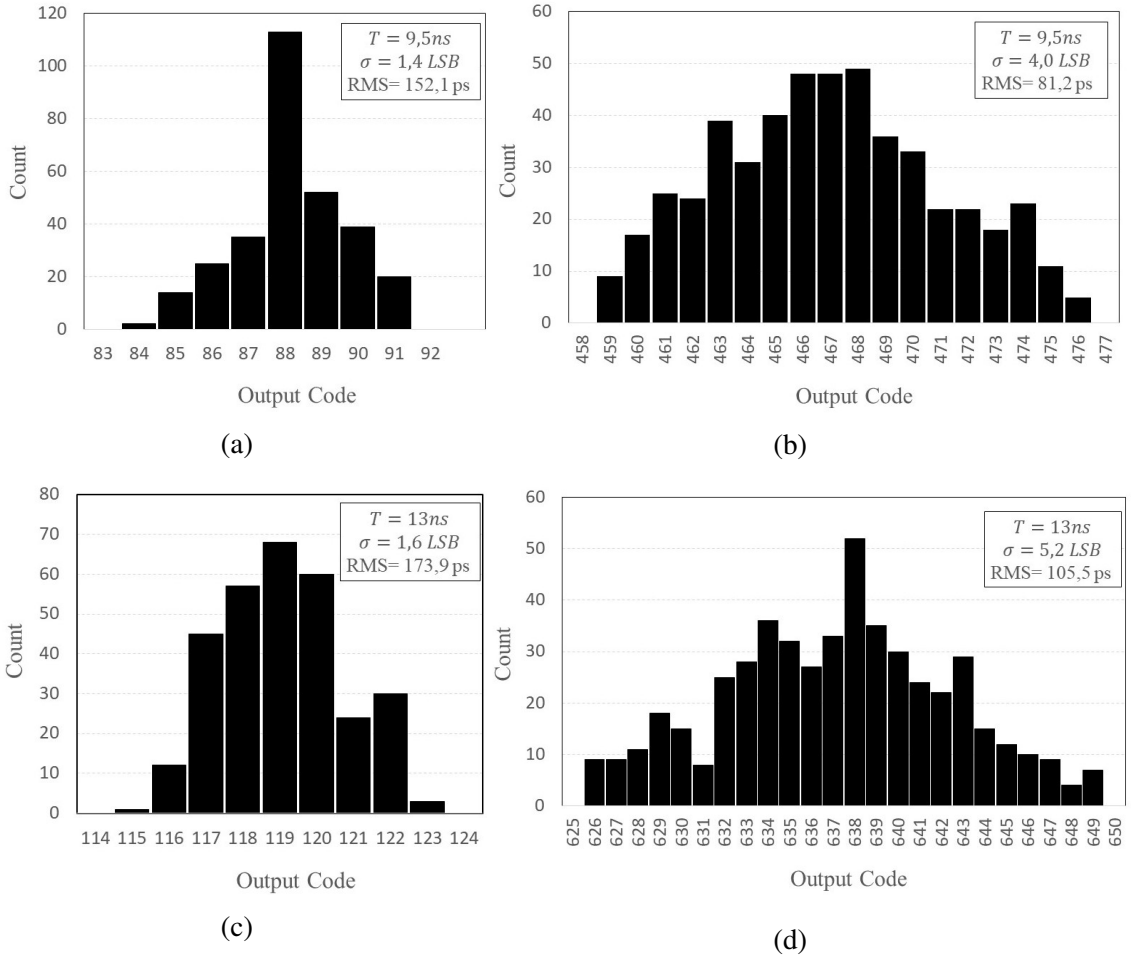

FIGURE 5.9: Histograms of the time interval measurement : 23-STRO based TDC : (a) $9.5\,\mathrm{ns}$ and (c) $13.0\,\mathrm{ns}$ / and 141-STRO based TDC : (b) $9.5\,\mathrm{ns}$ and (d) $13.0\,\mathrm{ns}$.

5.4.2.2 141-stage STRO-based TDC

As explained before, the time resolution can be reduced as fine as needed by increasing the number of stages. Thus, a 141-stage STRO-based TDC initialized with 88 events presents a theoretical time resolution of $20.3\,\mathrm{ps}$ with a frequency of $174.06\,\mathrm{MHz}$ ($T_{\mathrm{STR}} = 5.745\,\mathrm{ns}$). The STRO presents a measured jitter standard deviation of $20.0\,\mathrm{ps}$, which means with this time resolution, the TDC is operating in a noisy environment.

We measured a time interval of values $9.5\,\mathrm{ns}$ and $13.0\,\mathrm{ns}$ 500 times, shown in Fig. 5.9b and Fig. 5.9d. As expected, due to the presence of jitter with the obtained time resolution, only 50% (resp. 40%) of samples presents an error lower than $2\Delta\varphi$ for the measurement of $9.5\,\mathrm{ns}$ (resp. $13.0\,\mathrm{ns}$). Therefore, the corresponding timing uncertainty of the time interval $9.5\,\mathrm{ns}$ (resp. $13.0\,\mathrm{ns}$ measurement is $4.0\,[\mathrm{LSB}]$ (resp. $5.2\,[\mathrm{LSB}]$). However, the mean value of the 500 samples shows a high precision of measurement : it is equal to $9.51\,\mathrm{ns}$ for the measurement of $9.5\,\mathrm{ns}$ and equal to $12.98\,\mathrm{ns}$ for the measurement of $13.0\,\mathrm{ns}$.

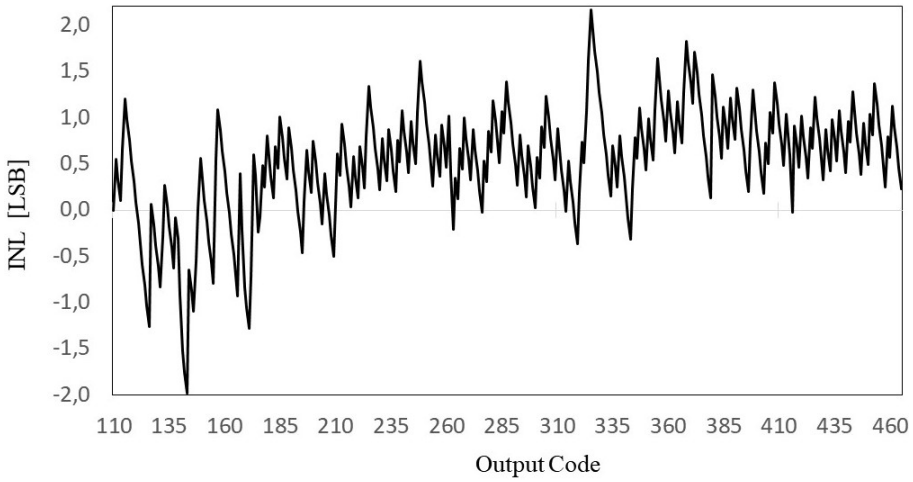

FIGURE 5.10: The 23-stage STRO-based TDC integral nonlinearity (INL).

5.4.2.3 Comparison with other TDCs

Table 5.1 presents the performance comparison of the proposed FPGA-based TDCs in the literature. All TDCs can differ for the number of the used stages, the integration of the calibration, or the FPGA performances. Our proposed TDC shows promising results even if we propose an implementation in a low-cost FPGA. The 23-stage STRO-based TDC required a total resource usage of 5864/136 (LUT/reg), including all the blocks as the FSM, algorithm block, and output display units (5% of total resources). On the other hand, the 141-stage STRO-based TDC occupied 7722/581 (LUT/reg), which presents a usage of 7% of total resources. The concept is recent and this proof-of-concept shows that it can easily be implemented in an FPGA. The STRO-based TDC offers on-line measurements. It allows a ToF capture at high repetition rate with a low circuit complexity. As a result, a performance enhancement can be obtained by controlling the place-and-route processes that have an important effect on the delays. Moreover, a high resolution with less number of stages can be obtained with an FPGA as used in [80, 81] or to extend the principle to faster and larger FPGA.

It can be noticed that the nonlinearity is not so good compared to some structures of the Table 5.1. This effect comes from the phases which are not perfectly evenly-spaced as it could be the case in an ASIC. Whereas, the proposed measurements are not performed in the same conditions and the nonlinearity of the STRO-based TDC, for the same level of resolution, is neverthless better than [54, 67, 73]. In our structure, we do not use a calibration process as it is the case for most of the presented TDCs in Table 5.1. Notice that, the usage of a calibration could lead to a better and higher precision with a reduced nonlinearity. Therefore, the proposed TDC targets small products, prototyping, or low-cost dedicated metrology applications.

TABLE 5.1: Performance summary and comparison with state-of-the-art TDCs

Reference	Year	FPGA	Architecture	Resolution (ps)	INL [LSB]	DNL [LSB]
[54]	2014	Cyclone II	carry chain	30.9	3.93	1.91
[80]	2015	Smart Fusion	TDL	63.3	0.72	0.55
[73]	2016	Virtex-6	TDL	10.0	3.93	2.00
[74]	2016	Virtex-6	Tuned-TDL	10.1	2.18	3.03
		Spartan-6		16.7	2.54	1.22
[9]	2017	Virtex-7	Tuned TDL	10.5	1.23	0.87
[82]	2017	Process 65 ns	Matrix of counters	7.40	1.57	0.74
[81]	2018	Actel-130	Two-stage delay line loop shrinking	8.50	0.91	0.36
[67]	2018	Spartan 6	TDL	26.0	2.96	1.23
This Work	2019	Cyclone IV	STRO	20.3	2.24	1.88

5.5 Conclusion

A hardware proof-of-concept implementation of our TDC has been presented using a 23-stage and 141-stage STRO-based TDCs in a low-cost FPGA. The implementation is straightforward and the results show a quite good linearity without calibration thanks to the almost evenly-spaced phase distribution. A $20.0\,\mathrm{ps}$ time resolution has been achieved using 141-stage. These results can be further improved by adding a calibration method. Moreover, thanks to the STRO unique features, this TDC architecture can achieve as fine as desired time resolution by increasing the number of stages. This TDC is only limited by the STRO stage noise in the FPGA. Furthermore, higher performances can be enhanced with recent and faster FPGAs, making it very suitable for Time-of-Flight measurement applications for instance.

Chapitre 6

STRO-based TDC prototypes

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6.1 Introduction

To further confirm and evaluate the advantages of the STRO-based TDC, an ASIC test chip has been designed and fabricated in 350 nm CMOS process. Four TDCs with different number of STRO stages have been included in this test chip. Most of the measurements are perfectly in accordance with our theoretical claims. They prove the ability of the proposed TDC architecture to enhance the time resolution by increasing the number of stages. Indeed, four TDCs with $L = 9, 23, 61,$ and 141 have been integrated in the same chip. The TDC principle was introduced in details with some preliminary measurement results in Chapter 4. This chapter presents the architecture of the fabricated test chip, details the test setup, and exposes the obtained measurement results. In fact, TDCs with $L = 9$, 23, 61, and 141 have been integrated in the same test chip. The chip includes 29 pads interfacing all the TDCs together. A 10-bit counter was

used to cover a dynamic range of $1700\,\mathrm{ns}$. The smallest TDC, with $L = 9$, samples the time intervals with a time resolution of $72.5\,\mathrm{ps}$, while a time resolution of $13.9\,\mathrm{ps}$ is obtained with the TDC of $L = 61$. Unfortunately, the 141-stage STRO based TDC cannot be exploited.

6.2 Layout of the TDC Prototype Chip

6.2.1 STRO-based TDC architecture

The global architecture of the L-stage STRO-based TDC implementation has been adapted, as illustrated in Fig. 6.1. In fact, the implementation in the $28\,\mathrm{nm}$ CMOS technology has shown a high oscillation frequency, which allows to obtain fine time resolution with a low number of stages. With the $350\,\mathrm{nm}$ CMOS technology, the frequency has been reduced due to the longer delays of the C-element. Thus, more stages are required to ensure the same time resolution.

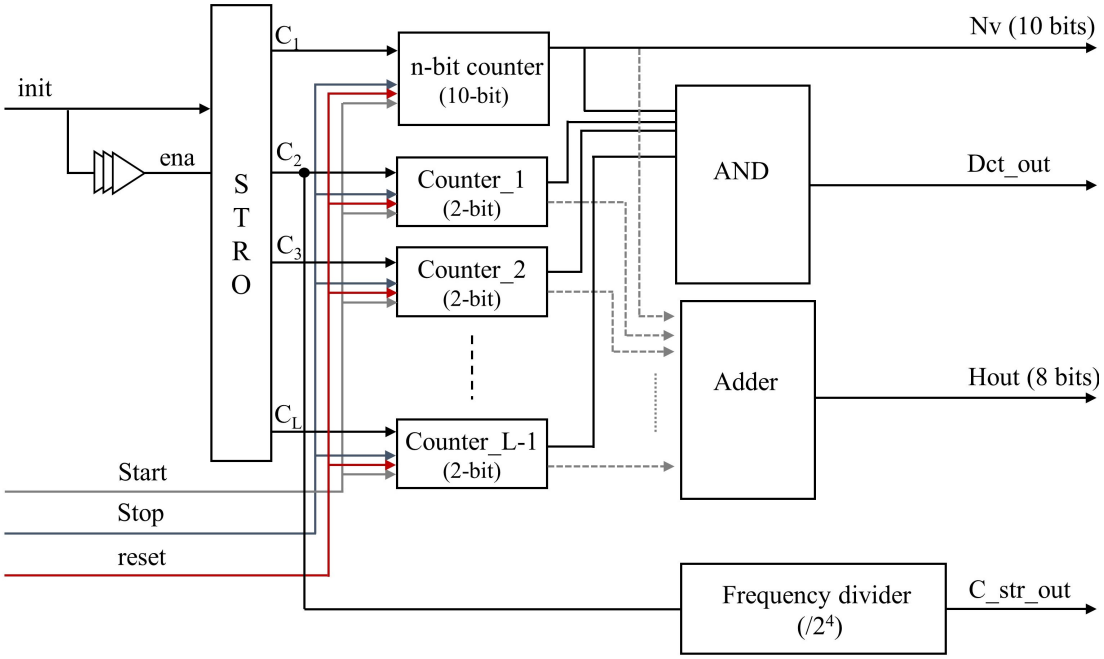


FIGURE 6.1: The global architecture of L-stage TDC for 350 nm CMOS technology implementation.

To cover several time resolution, four TDCs with different numbers of stages have been implemented in the same chip. Each TDC operates independently. According to the selected TDC, the measurement results are presented in the common outputs of the chip. The first TDC of 9 stages (with an initialization of 4 tokens) shows an estimated time resolution of $74.0\,\mathrm{ps}$. This latter is enough larger than the jitter standard deviation of the STRO. The jitter value is estimated to be between the $10.0\,\mathrm{ps}$ and $15.0\,\mathrm{ps}$. The enhancement of the time resolution around the jitter variations was adopted for the two TDCs with $L = 23$ (including 12 tokens) and $L = 61$ (with

30 tokens). The achieved time resolutions are respectively $29.6\,\mathrm{ps}$ and $13.9\,\mathrm{ps}$. The last TDC has a large number of stages to reach a time resolution of $5.0\,\mathrm{ps}$ with $L = 141$ and $N_T = 70$ operating in a high noisy environment. In the sequel, we present the detailed implementation of the TDCs.

6.2.1.1 STRO with analog C-element

The *analog C-element* topology has been chosen for the STRO-stage implementation to benefit from the symmetric topology and to simplify the connection between the stages. Thus, the same values of D_{ff} and D_{rr} are obtained. The estimated values of these propagation delays using the $350\,\mathrm{nm}$ CMOS technology are $D_{\mathrm{ff}} = D_{\mathrm{rr}} = 350ps$. Thanks to this, the maximal frequency, with maximal Charlie effect amplitude, is obtained for equal number of tokens and bubbles ($N_T = N_B \pm 1$). Therefore, for a maximal frequency, a L-stage STRO is initialized with $L/2$ events. In this case, the same frequency is obtained for each STRO of any number of stages as long as the occupancy ratio is surely equal to 1/2. Therefore, duplicating the number of STRO stages by N allows to reduce the time resolution by this factor.

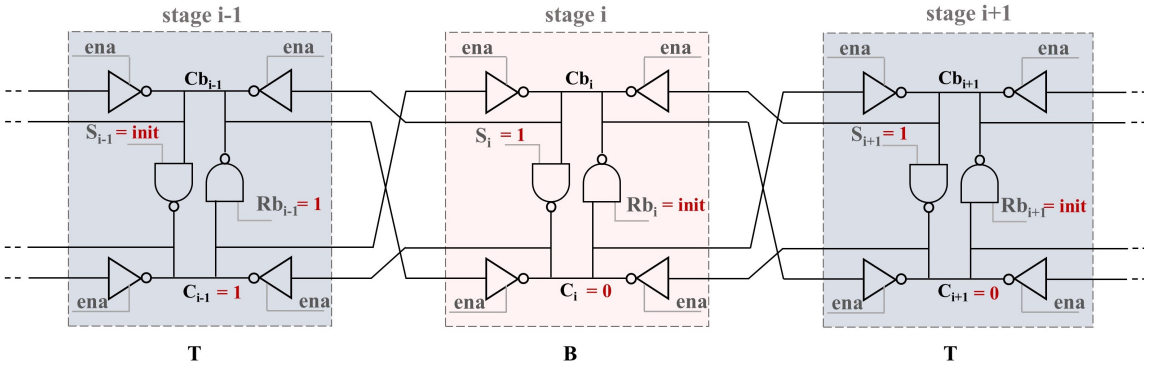


FIGURE 6.2: Three stages example from a self-timed ring oscillator with *Analog C-element* implementation given with an initialization example.

As presented in Section 3.2, the *analog C-element* has symmetric inputs and outputs. Its connectivity is displayed in Fig. 6.2. It shows the direct connection of the stage i with its adjacent stages (stage $i-1$ and stage $i+1$). In the same figure, an example of the initialization process was described. It details how to assign signal values to the inputs Rb_i and S_i in order to initialize the stage with a token or a bubble. For a fast distribution of events over the STRO, it is recommended to initialize the ring as follows : {TBTBTB..} (*e. g.*, it can correspond to an STRO output vector of {0110011..}). The inputs Rb_i and S_i allow initializing the stages. In fact, the input signals Rb_i and S_i are active low, which allows to reset (resp. to set) the stage output C_i. Only one signal *init* can be used to assign values to the initialization inputs. It can be initialized with a value "0" in order to active the inputs Rb_i and S_i, and then goes high to make stages in a free mode. An illustration is displayed in Fig. 6.2 in which the output C_{i-1} is set to "1" while C_i and C_{i+1} are set to "0". According to this, the stage $i-1$ is initialized with a token and the stage i initialized

with a bubble. In order to make the design simple, the STRO stages have been designed with a fixed initialization.

The signal *ena*, which triggers the tri-state inverters, freezes the inverter outputs during the initialization. Thus, it is only set high once the initialization is finished. The signal *ena* must be sufficiently delayed to guarantee a correct initialization. Notice that the signal *init* has the same shape, as shown in Fig. 6.3.

The *analog C-element* can easily be implemented using standard cells. However, the fan-out at each stage must correctly be sized since the ring has to be connected to the counters. In fact, for a gate output, the fan-out expresses the maximal number of inputs of the same type that can be safely connected to the gate. Indeed, the STRO frequency and duty cycle are also function of the fan-out value, since it affects the gate delays.

6.2.1.2 Counting unit implementation

The estimated minimal frequency from the simulations is about $530.0\,\mathrm{MHz}$. Thus, a 10-bit counter is implemented to cover a dynamic range of $2.0\,\mu\mathrm{s}$. The counter of Fig. 4.10 was used in this proposition. Therefore, two 9-bit counters are required : the first one is clocked with C_i and the second with Cb_i. The sum of the outputs is represented on 10 bits. The counters include Mutex circuits making a decision in case of metastability.

Otherwise, each TDC includes its own Hamming and M Parity blocks, which are simply made by adders and AND gates. The Hamming block output requires 8 bits to fit with the results for all these TDCs. We chose to implement each TDC with its own finite-state-machine (FSM) instead of using a global FSM for all the TDCs.

6.2.2 Input/Output interfaces

The finite-state-machine (FSM) has been implemented off-chip (on an FPGA). It allows generating the input signals as presented in Fig. 6.3. The *init* signal is generated by the FSM. On its arrival, *init* is delayed in order to produce the signal *ena*. The *reset* signal, generated by the FSM, allows resetting the flip-flop outputs of the counters before starting a measurement on the *Start* event. Then, the measurement is stopped by the *Stop* signal, which triggers the TDC outputs. Another *reset* signal is used to initialize the FSM, which is independent from the counter *reset* signal. *Sel*, a 2-bit signal, allows selecting the TDC we want to use. The input signals and the TDC outputs are summarized in Table 6.1.

Fig. 6.4 shows a block diagram for connecting the FSM with the chip for the test. Indeed, the use of the FSM is optional and can be replaced by other sources able to create signals such as generators.

Practically, for the 350 nm CMOS technology, the maximal input frequency allocated to the input of the pads is limited to $100.0\,\mathrm{MHz}$. Unfortunately, the STRO frequency exceeds

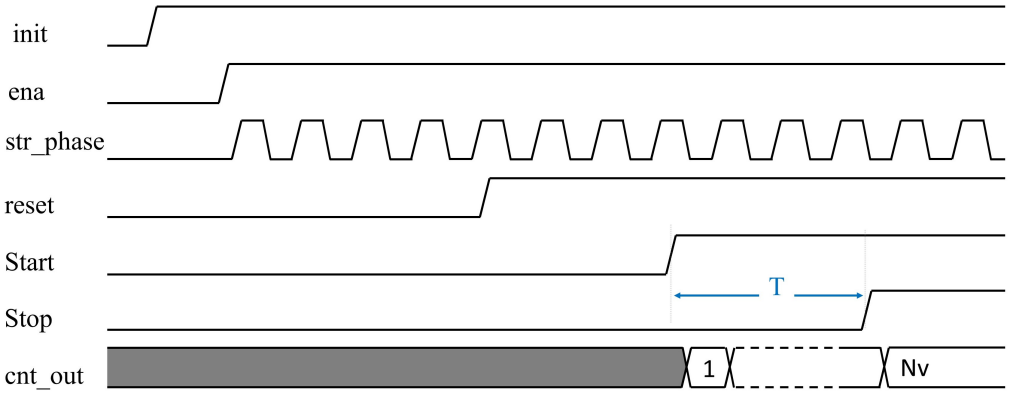


FIGURE 6.3: The chip input signals timing diagram.

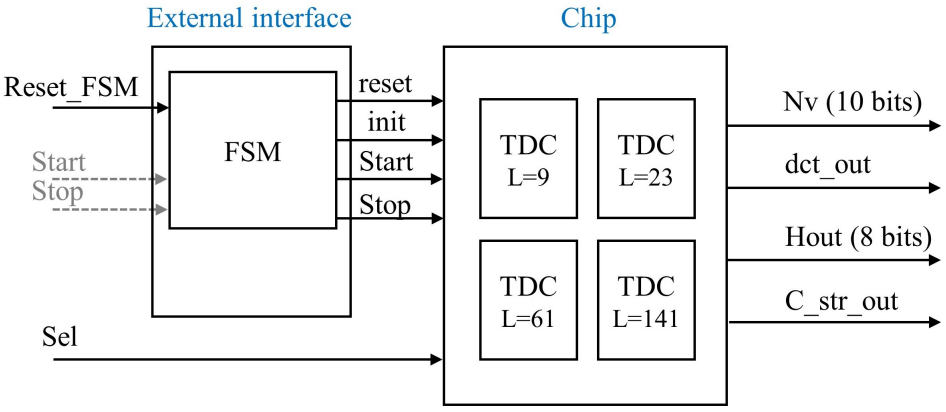


FIGURE 6.4: Block diagram of the experimental setup.

this bandwidth limitation and can further reach $850.0\,\mathrm{MHz}$, as it has been shown by simulation. Therefore, the *C_str_out* signal has to go through a frequency divider to be externally measured. A division ratio of $2^4 = 16$ has been implemented into the frequency divider. It is also possible to select the STRO phase C_2 to measure the STRO frequency for the test. This measurement is not very accurate due to the division.

6.2.3 Layout and circuit

The proposed STRO-based TDC was fabricated in the 4-metal layers CMOS 350 nm AMS technology. The prototype was designed to include the 4 TDCs together. A total number of 25 pads have been included in the circuit to interface the TDCs with the measurement tools, as schematically shown in Fig. 6.5a. The supply voltage is $3.3\,\mathrm{V}$. Supplementary power supply pads have been used for the GND and the VDD adding four extra pads to the TDC chip. Therefore, a dual-in-line (DIL) ceramic package with 40 pads has been used for packaging the chip.

A microphotograph of the four STRO-based TDC fabricated in CMOS 350 nm AMS technology is shown in Fig. 6.5b. Each TDC placement is mentioned in the figure. The size of

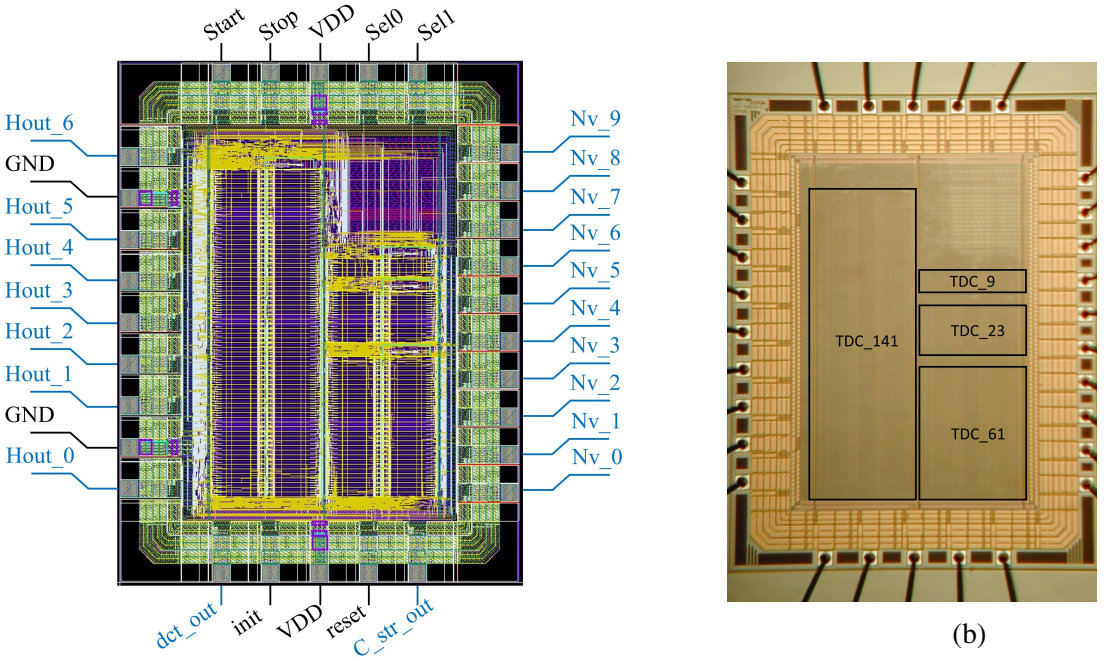
TABLE 6.1: Input/ Output interfaces : Pins description.

	Pin name	Number of bits	Description	
Inputs	*reset*	1	Counters reset signal	
	init	1	The signal to initialize and enable the STRO	
	Start	1	The event to start the time interval measurement	
	Stop	1	The event to stop the measurement	
	Sel	2	00	Selection of TDC_9 ($L = 9$)
			01	Selection of TDC_23 ($L = 23$)
			10	Selection of TDC_61 ($L = 61$)
			11	Selection of TDC_141 ($L = 141$)
Outputs	*C_str_out*	1	The STRO phase C_2 with a frequency division of 16	
	dct_out	1	The Parity block output	
	Hout	7	The Hamming block output	
	Nv	10	The 10-bit counter output	

the whole layout including the input/output pads is $2.88\,\mathrm{mm}\times 2.21\,\mathrm{mm}$. The actual core area is $3.29\,\mathrm{mm}^2$ ($2.18\,\mathrm{mm}\times 1.51\,\mathrm{mm}$). The 9-stage STRO-based TDC occupies an area of $0.181\,\mathrm{mm}\times 0.67\,\mathrm{mm}$, which presents 3.7% of the core area. The 23-stage STRO-based TDC area is $0.380\,\mathrm{mm}\times 0.67\,\mathrm{mm}$, which presents 7.7% of the core area. The 61-stage STRO-based TDC occupies 17.9% of the core area ($0.880\,\mathrm{mm}\times 0.67\,\mathrm{mm}$). Fig. 6.6 shows the photograph of the packaged circuit after reception. Finally, the 141-stage STRO-based TDC is not reported.

6.3 Measurement results

As shown in Fig. 6.4, the test setup consists of using an external interface, employed as a signal generator, and an oscilloscope. An Intel Cyclone IV FPGA was used to generate the input signals (*reset*, *Sel*, *init*, and *Start* signals). In fact, the *Start* signal was split into two pulses. The direct pulse is injected into the TDC as the *Start* signal. The second pulse is delayed by a coaxial cable and, then, injected into the TDC as the *Stop* signal. Therefore, the time made by the signal to propagate into the cable, which is related to the length of the cable, presents the time interval to be measured by the TDC. The oscilloscope allows measuring the frequency of the STRO presented by the output *C_str_out*. The other TDC digital outputs are connected to the oscilloscope with digital cables allowing to show an hexadecimal value. This value is then converted with an algorithm to express the TDC output.



(a) (b)

FIGURE 6.5: (a) the circuit layout with pads and input/output, (b) Microphotograph of the four STRO-based TDC chip.

6.3.1 9-stage STRO-based TDC

The 9-stage STRO-based TDC consumes $88.9\,\mathrm{mW}$ at room temperature ($25°$). The measured frequency by the oscilloscope is $47.89\,\mathrm{MHz}$. This value is multiplied by 16 and corresponds to an STRO frequency of $766.28\,\mathrm{MHz}$. As a result, a theoretical time resolution of $72.5\,\mathrm{ps}$ is obtained. A large number of measurements have been made in order to characterize the single-shot measurements. Thus, many hits, carried out using several coaxial cables, were analyzed in order to characterize the TDC performances. Fig. 6.7 plotted the histogram of the resulted digital TDC outputs for two different time delays : $2.95\,\mathrm{ns}$ and $12.5\,\mathrm{ns}$. The TDC shows a mean value of $2.988\,\mathrm{ns}$ with a standard deviation of $\sigma = 1.71\,\mathrm{LSB}$ for the time input $T = 2.95\,\mathrm{ns}$ representing an error of $38.0\,\mathrm{ps}$. When the input time is $T = 12.5\,\mathrm{ns}$, the measurement error is $204.0\,\mathrm{ps}$ for a mean value of $12.704\,\mathrm{ns}$ and a standard deviation of $\sigma = 2.23\,\mathrm{LSB}$. Many other input times have been measured as displayed in Table 6.2.

TABLE 6.2: Measurement summary of the 9-stage STRO based TDC presenting a time resolution of $\Delta\varphi = 72.5\,\mathrm{ps}$.

	$T = 2.95\,\mathrm{ns}$	$T = 4.30\,\mathrm{ns}$	$T = 7.78\,\mathrm{ns}$	$T = 10.7\,\mathrm{ns}$	$T = 12.5\,\mathrm{ns}$
TL	42	58	105	150	174
$T_m\ (ns)$	3.045	4.205	7.612	10.875	12.615
$T_{mean}\ (ns)$	2.988	4.248	7.612	10.778	12.704
$\|\|Err\|\|\ (ps)$	38.0	52.0	112.0	78.0	204.0
σ (LSB)	1.71	2.10	1.33	1.96	2.38

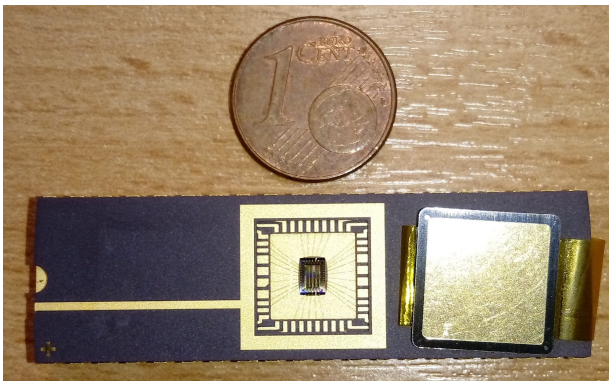


FIGURE 6.6: the test-chip photo.

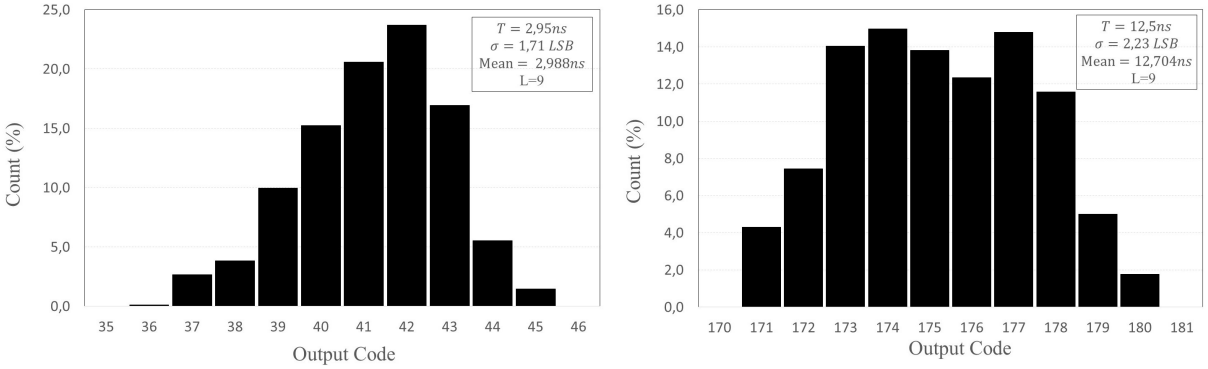


FIGURE 6.7: Measured single-shot precision of the 9-STRO based TDC when input time intervals are respectively $2.95\,\mathrm{ns}$ and $12.5\,\mathrm{ns}$.

The post-layout simulations for each case have been processed in order to validate the TDC measurement. The measured time intervals from these simulations are respectively $T_m = 3.008\,\mathrm{ns}$ and $T_m = 12.628\,\mathrm{ns}$ for the input time interval $T = 2.95\,\mathrm{ns}$ and $T = 12.5\,\mathrm{ns}$. As shown in Table 6.3, the simulated values present an error, which does not exceed $2\Delta\varphi$.

TABLE 6.3: Post-layout simulation results for the 9-stage STRO based TDC.

	$T = 2.95\,\mathrm{ns}$	$T = 4.30\,\mathrm{ns}$	$T = 7.78\,\mathrm{ns}$	$T = 10.7\,\mathrm{ns}$	$T = 12.5\,\mathrm{ns}$
$T_m\ (ns)$	3.008	4.340	7.890	10.778	12.628
$\|\|Err\|\|\ (ps)$	58.0	4.0	112.0	78.0	128.0

6.3.2 23-stage STRO-based TDC

On the other hand, the same measurements from the 23-stage STRO-based TDC have been processed. This TDC presented a power consumption of $164.6\,\mathrm{mW}$ for a frequency of $734.43\,\mathrm{MHz}$ corresponding to $\Delta\varphi = 29.6\,\mathrm{ps}$. As displayed in Fig. 6.8, the TDC shows a measurement error of $30.0\,\mathrm{ps}$ (resp. $45.0\,\mathrm{ps}$) with a mean value of $2.98\,\mathrm{ns}$ (resp. $12.545\,\mathrm{ns}$), and a standard deviation of $\sigma = 2.12\,\mathrm{LSB}$ (resp. $\sigma = 2.61\,\mathrm{LSB}$) for $T = 2.95\,\mathrm{ns}$ (resp. $T = 2.95\,\mathrm{ns}$).

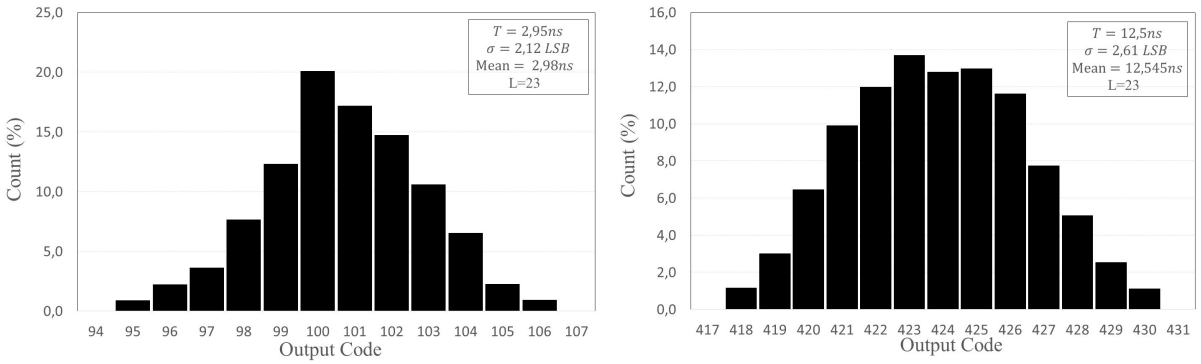


FIGURE 6.8: Measured single-shot precision of the 23-STRO based TDC when input time intervals are respectively $2.95\,\mathrm{ns}$ and $12.5\,\mathrm{ns}$.

TABLE 6.4: Measurement summary of the 23-stage STRO based TDC presenting a time resolution of $\Delta\varphi = 29.6\,\mathrm{ps}$.

	$T = 2.95\,\mathrm{ns}$	$T = 4.30\,\mathrm{ns}$	$T = 7.78\,\mathrm{ns}$	$T = 10.7\,\mathrm{ns}$	$T = 12.5\,\mathrm{ns}$
TL	100	148	264	355	423
$T_m\ (ns)$	2.960	4.380	7.814	10.508	12.520
$T_{mean}\ (ns)$	2.980	4.369	7.791	10.539	12.545
$\|Err\|\ (ps)$	30.0	69.0	291.0	160.0	45.0
σ (LSB)	2.12	2.52	2.49	2.95	2.61

TABLE 6.5: Post-layout simulation results for the 23-stage STRO based TDC.

	$T = 2.95\,\mathrm{ns}$	$T = 4.30\,\mathrm{ns}$	$T = 7.78\,\mathrm{ns}$	$T = 10.7\,\mathrm{ns}$	$T = 12.5\,\mathrm{ns}$
$T_m\ (ns)$	2.996	4.388	7.723	10.739	12.334
$\|Err\|\ (ps)$	46.0	88.0	57.0	39.0	166.0

We can notice from the post-layout simulations, presented in Table 6.5, show a quantization error lower than $100\,\mathrm{ps}$ (except for the $T = 12.5\,\mathrm{ns}$ measurement). However, the ratio of this error is larger than $1.5\,\mathrm{LSB}$ due to the lower time resolution ($\Delta\varphi = 29.0\,\mathrm{ps}$).

6.3.3 61-stage STRO based TDC

The time resolution of the 61-stage STRO-based TDC is equivalent to $\Delta\varphi = 13.9\,\mathrm{ps}$ with a measured frequency of $589.69\,\mathrm{MHz}$ and a power consumption of $365.5\,\mathrm{mW}$. The resolution of this TDC is about the jitter level of the circuits. The time measurement of the first hit shows a mean value of $2.93\,\mathrm{ns}$ with an error of $20.0\,\mathrm{ps}$ and $\sigma = 2.41\,\mathrm{LSB}$. However, the measurement of $T = 12.5\,\mathrm{ns}$ presents an important quantification error regarding the time resolution of $164.0\,\mathrm{ps}$

(the mean value is $12.336\,\mathrm{ns}$). The measurements are highly affected by the jitter, which is obvious with the higher standard deviation (noise $\sigma = 3.69\,\mathrm{LSB}$).

Since the time resolution of this TDC is almost at the same jitter level, the measurement precision is affected. The error of the measurement has reached $22\,\mathrm{LSB}$. The post-layout simulations have been used to explain this gap. They revealed that due to an error in the design, the phases are not anymore equally distributed. Thus, the jitter contributes to a non-uniform time resolution. The considered value of the time resolution in Table 6.6 is a relative value deduced from the frequency. However, even though this non-uniform time spacing, the TDC can present an approximate value of the measurement as presented by the results of the intervals $T = 2.95\,\mathrm{ns}$ and $T = 10.7\,\mathrm{ns}$.

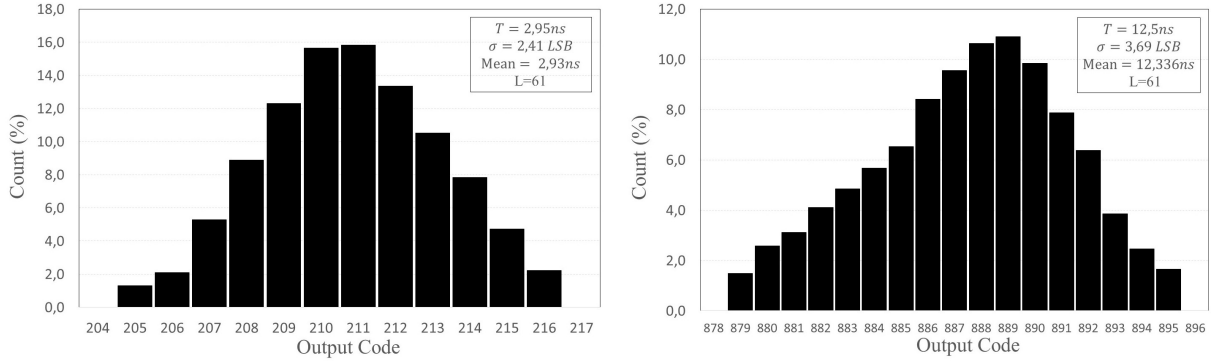


FIGURE 6.9: Measured single-shot precision of the 61-STRO based TDC when input time intervals are respectively $2.95\,\mathrm{ns}$ and $12.5\,\mathrm{ns}$.

TABLE 6.6: The test chip Measurements for the 61-stage STRO based TDC with a time resolution of $\Delta\varphi = 13.9\,\mathrm{ps}$.

	$T = 2.95\,\mathrm{ns}$	$T = 4.30\,\mathrm{ns}$	$T = 7.78\,\mathrm{ns}$	$T = 10.7\,\mathrm{ns}$	$T = 12.5\,\mathrm{ns}$
TL	211	332	522	767	889
$T_m\ (ns)$	2.932	4.614	7.255	10.661	12.357
$T_{mean}\ (ns)$	2.930	4.613	7.252	10.638	12.336
$\|\|Err\|\|\ (ps)$	20.0	313.0	247.0	61.0	163.0
σ (LSB)	2.41	2.60	2.99	3.92	3.69

6.4 Conclusion

The hardware implementation of the proposed TDC architecture using $350\,\mathrm{nm}$ CMOS technology allows us to further evaluate the performance and confirm the advantages of the proposed approach. Most of the measurements are perfectly in accordance with our theoretical claims. They prove the ability of the proposed TDC architecture to enhance the time resolution by increasing the number of stages. In fact, the proposed TDC achieves a mean standard deviation

of measurement of $1.8\,\mathrm{LSB}$ for a total number of stages of 9. For this TDC, the achieved time resolution is $72.5\,\mathrm{ps}$. Compared to the proposed TDCs in literature, according to the same equivalent number of stages, our TDC presents a fine time resolution [63]. Unfortunately, a design error occurred in the TDCs with 23 and 61 stages. Their measurement results prove the time resolution enhancement by increasing the number of stages. The 61-stage STRO based TDC was supposed to give more information when reaching a resolution close to the STRO jitter. Despite this, we have been able to exploit some measurements. According to these results, we are convinced that integrating a simple calibration of the frequency will help to improve the measurements. In our case, it is important to notice that the so-called analog Charlie's effect avoid the phase calibration, which is a strong advantage compared to TDCs requiring delay calibration. Furthermore, they can be further improved by using averaging. All these points can be considered for the next steps. Finally, we were not able to integrate the study of linearity due to the limited PhD time. This will be done in the future works.

Chapitre 7

Conclusions and Perspectives

7.1 Thesis contributions

Time-to-digital converters (TDCs) have become unavoidable in systems incorporating high precision time measurements. They are used in many application fields such as high-energy physics, metrology, telecommunications and satellite positioning. Fully digital approaches are today adopted to benefit from low-power and small circuit area. In this work, a new approach has been presented for designing a fully digital TDC for high precision time measurements. This architecture offers a fine quantification of the time interval between two unpredictable events. The proposed structure is based on a self-timed ring oscillator (STRO). The STRO stages are usually used as parts of the control path of micropipeline circuits (asynchronous circuits). The STRO interest is their very interesting analog features. They particularly offer the ability to tune the time resolution as fine as needed by just adjusting the number of stages at design time. In addition, the STRO specific analog phenomena, namely the Charlie and Drafting effects, contribute to uniformly distribute the events (electrical transitions) in time. Thus, the STRO phases are uniformly spaced in time with an output phase difference corresponding to TDC time resolution, which can be lower than the stage propagation delay (sub-gate delay). Our in-depth knowledge of these oscillators has allowed us to develop a new class of ultra-precise TDCs based on a single STRO. Furthermore, this TDC can perform on-the-fly time measurement on fast non-periodic signals, which has been proved by simulation and experimental results. These latter revealed a promising solution for precise time measurements. To the best of our knowledge, the STRO-based TDC technique presented in this thesis was the first TDC deploying the self-timed ring oscillator technique.

In this thesis, we have first studied the main TDC structures in literature in order to be able to compare them to our proposition and to highlight STRO-TDC performances as well. The first TDC generation based on analog techniques presents high precision and fine time resolution but low dynamic ranges. Moreover, since these TDCs are not well-suited for the technology shrink, they have been replaced by TDCs based on digital techniques offering a reduced die area and

a lower power consumption. Thereby, a lot of digital TDCs have been investigated targeting a sub-gate delay resolution. Most of the time, this precision depends on the delay elements, which are often difficult to design. Therefore, improved structures, mostly hybrid, have been studied in order to provide better performances. Nevertheless, the trade-off between sub-gate delay resolutions, a wide dynamic range, on-the-fly measurements, and an easy calibration is not at all trivial.

By exploring different TDC architectures in the literature, we identified that high precision can be obtained be propagating several events at the same time in a ring oscillator. Therefore, we realized that the STRO was a good candidate to build TDCs because they propagate multiple events without collision.

Developing such a technique requires fully understanding the oscillator characteristics. To this goal, we performed high-level simulations taking into consideration the technological parameters and the analog behavior of the STRO, so that they give similar results as analog simulations. A VHDL code of the STRO-based TDC has been written thanks to the TAL library (TIMA Asynchronous Library), which simulates the analog effects inside the C-elements. TDC analog simulations have been performed with Virtuoso analog design environment (ADE) in order to extract the technological parameters for the high-level simulations and to validate the TDC in an analog environment.

The simulation results using 28 nm FDSOI technology are very promising. They show :

— A full digital architecture : the STRO TDC is only designed with standard cells.
— Sub-gate delay resolution : the resolution can be tuned as fine as needed by simply increasing the number of stages. Thus, it can be much lower than the "gate-delay".
— Wide Dynamic range : thanks to its oscillator structure, the TDC dynamic range is only be limited by its counter capabilities.
— On-the-fly measurement : as the measurement process is fast and does not required averaging, on-the-fly measurement can be performed.
— Easy calibration : only the STRO frequency is required because the phases are naturally evenly-spaced because of the Charlie's effect.

We also validate the TDC in a noisy environment by including adequate parameters into the simulation. Then, we computed the integral nonlinearity (INL) and the differential nonlinearity (DNL) of the STRO-based TDC. The simulations showed a time resolution of $8.9\,\mathrm{ps}$ by simulating a TDC with only 9 stages in the FDSOI 28 nm technology from STMicroelectronics. This resolution has been enhanced to $1.3\,\mathrm{ps}$ by using 61 stages, which is very close to the level of jitter. This highlights the limitation of the resolution enhancement for an on-the-fly measurement.

As a first hardware proof-of-concept, we have implemented our proposed TDC in a low-cost FPGA Intel Cyclone IV. The main result of this experiment has proved that the STRO-based TDC is able to achieve fine time resolution by simply increasing the number of STRO stages.

We also suggested an adapted structure to the FPGAs, and applied it to two TDCs, respectively with $L = 23$ and $L = 141$ stages. Despite there is no access to the FPGA routing network, the results point out the advantages of this new architecture in terms of measurement accuracy. Moreover, we demonstrated that our proposal is achievable with low-cost commercial FPGAs, which is sufficient to open the door for a broad spectrum of applications.

We also designed an ASIC version of our TDC in the CMOS 350 nm technology from AMS. A campaign of measurements has been carried out on the 9-stage, 23-stage, and 61-stage STRO-based TDCs in order to validate the TDC performances. The achieved time resolution was respectively $72\,\mathrm{ps}$, $30\,\mathrm{ps}$, and $14\,\mathrm{ps}$. Notice that the measurements and the simulations have almost the same results although the 23-stage and 61-stage STRO-based TDCs suffer from a design error (a wire has been added by inadvertency. This probably degrades a few the analog properties of the 2 STROs).

7.2 Perspectives

This work is a proof-of-concept of a new TDC architecture based on a STRO. Further works have to be pursued to complete this thesis :

— The linearity test of the fabricated chip has not been achieved due to the lack of time. This can be realized with an equipment able to arbitrarily generate the input times. In addition, a printed circuit board (PCB) should be considered to facilitate the tests.

— Once the TDC characteristics are verified, a test of the stability of the TDC toward voltage and temperature variations should also be conducted. Such tests have been already done in previous works for STROs [31].

— The STRO-based TDC with a time resolution close to the jitter level is much trickier. Even if reducing the jitter noise is challenging, this is required to perform on-the-fly measurements with picosecond and sub-picosecond resolutions.

— Calibration techniques must be developed in order to propose a complete TDC system. Fortunately, the STRO does not require a delay calibration unit thanks to the phase distance auto-calibration ensured by the Charlie's effect. However, an absolute time calibration is needed to correctly define the value of $\Delta\varphi$. Post-processing techniques can also be valuable.

— The STRO stability for very large dynamic range is another issue. In this case, the STRO could be associated with a crystal oscillator to solve this problem. Indeed, two simple counters can be used to count the number of periods during a fixed time interval : one for the reference clock and the other for the STRO. Thus, the unknown value of T_{STR} can be precisely computed even if the interval is very large.

— Repetitive measurements can also be exploited in order to improve the TDC accuracy. For on-the-fly measurements, averaging with the results of several TDCs is feasible. In

this case, the global architecture could be enhance for integrating several STROs.

— Finally, this TDC architecture can be applied to design Analog-to-Digital Converter (ADC). Indeed, slope accurate converters could be implemented with our TDC.

Glossary

ADC Analog-to-Digital Converter.

ADPLL All Digital Phase Locked Loop.

ASIC Application-Specific Integrated Circuits.

DIL Dual-In-Line.

DK Design Kit.

DLL Delay-Locked-Line.

DNL Differential Nonlinearity.

FF Flip-Flop.

FIFO First In First Out.

FPGA Field Programmable Gate Arrays.

GRO Gated Ring Oscillator.

INL Integral Nonlinearity.

IRO Inverter Ring Oscillator.

ISF Impulse Sensitivity Function.

LAB Logic Array Block.

LE Logic Element.

LSB Least Significant Bit.

LUT Look Up Table.

LVDS Low Voltage Differential Signaling.

MUTEX MUTuel EXclusion.

PCB Printed Circuit Board.

PVT Process, Voltage, Temperature.

RTL Register Transfer Level.

SCW Stage Control Word.

SMA SubMiniature version A.

STRO Self-Timed Ring Oscillator.

TAL TIMA Asynchronous Library.

TDC Time-to-Digital Converter.

TDL Tapped Delay Line.

ToF Time-of-Flight.

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2. O. Elissati, A. Cherkaoui, **A. El-Hadbi**, S. Rieubon, and L. Fesquet, "Multi-Phase Low-Noise Digital Ring Oscillators with Sub-Gate-Delay Resolution". In *AEU International Journal of Electronics and Communications, vol. 84, pp. 74-83, 2018. doi : 10.1016/j.aeue.2017.11.022.*

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1. **A. El-Hadbi**, O. Elissati and L. Fesquet "Time-to-Digital Converters : A Literature Review and New Perspectives". In *2019 5th Conference on Event-Based Control, Communication and Signal Processing (EBCCSP'19), Vienna, Austria, May 27-29, 2019. doi :10.1109/EBCCSP.2019.8836857.*

2. O. Elissati, **A. El-Hadbi**, A. Cherkaoui, S. Rieubon, and L. Fesquet "Low Phase-Noise CMOS Quadrature Oscillator based on (N x 4)-stage Self-Timed Ring". In *2018 33rd Conference on Design of Circuits and Integrated Systems (DCIS'18), Lyon, France, November 14-16, 2018, pp. 1-5. doi :10.1109/DCIS.2018.8681473.*

3. **A. El-Hadbi**, A. Cherkaoui, O. Elissati, J. Simatic, and L. Fesquet, "On-the-fly sub-gate-delay resolution TDC based on self-timed ring : A proof of concept". In *2017 15th IEEE International New Circuits and Systems Conference (NEWCAS'17)*, Strasbourg, France, 25-28 June 2017, pp. 305-308. doi :10.1109/NEWCAS.2017.8010166. **Best Paper Award**.

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Time-to-Digital Conversion based on a Self-Timed Ring Oscillator

Abstract : Time-to-digital converters (TDCs) have become unavoidable in systems incorporating high precision time measurements. They are used in many application fields such as high-energy physics, metrology, telecommunications and satellite positioning. Fully digital approaches are today adopted to benefit from low-power and small circuit area. This thesis proposes a new TDC architecture based on a Self-Timed Ring (STR) oscillator, which is able to provide a very high resolution without averaging. Indeed, the proposed TDC virtually achieves a time resolution as fine as desired by simply increasing the STR oscillator number of stages. In fact, the STRO is a multi-phase oscillator, which is able to provide one phase per stage output. The TDC exploits these different STRO phases, which are evenly-spaced thanks to the unique analog STRO properties. Thus, a regular time base can be extracted from this STR oscillator and applied for time measurement. This thesis demonstrates the advantages of such a TDC in terms of precision, calibration, low-cost and for on-the-fly measurements. It also states the TDC limits due to the STRO jitter. After a first implementation on an FPGA, an ASIC prototype has been designed, fabricated and tested for validating this new class of TDC.

Keywords: Time-to-Digital Converter (TDC), Self-Timed ring (STR) oscillator, time measurement, on-the-fly measurement, ASIC and FPGA TDC implementations.

Conversion Temps-Numérique basée sur un Oscillateur Auto-Séquencé

Résumé : Les convertisseurs temps-numérique (TDC) sont devenus incontournables dans les systèmes intégrant une mesure très précise du temps. Ils sont utilisés dans de nombreux domaines d'application tels que la physique nucléaire, la métrologie, les télécommunications et le positionnement par satellite. Les approches entièrement numériques sont aujourd'hui adoptées pour tirer parti de la faible consommation et de la petite taille des circuits intégrés. Cette thèse propose une nouvelle architecture de TDC basée sur un oscillateur auto-séquencé (STRO), capable de fournir une très haute résolution sans nécessité de moyenner. En fait, le TDC proposé peut théoriquement atteindre une résolution temporelle aussi fine que souhaitée en augmentant simplement le nombre d'étages de l'oscillateur. En effet, le STRO est un oscillateur multi-phases pouvant fournir une phase par étage. Ainsi, ce TDC exploite les différentes phases de l'oscillateur qui sont régulièrement espacées grâce aux propriétés analogiques spécifiques des STROs. Ainsi, une base de temps peut être extraite du STRO et appliquée à la mesure du temps. Cette thèse démontre les avantages d'un tel TDC en termes de précision, de calibration et de coût réduit ainsi que ces aptitudes à effectuer des mesures à la volée. Les limites du TDC, essentiellement dues à la gigue du STRO, sont également abordées. Après une première implémentation sur FPGA, un prototype ASIC a été conçu, fabriqué et testé validant cette nouvelle classe de TDC.

Mots-clés : Convertisseur Temps-Numérique (TDC), Oscillateur Auto-Séquencé (STR), mesure du temps, mesure à la volée, implémentations d'un TDC sur ASIC et FPGA.

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