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Impact of aging on the behaviour of wild band gap power transistors, application to the efficiency of DC-DC converters

Al Mehdi Bouchour

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Pour obtenir le diplôme de doctorat

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et de Université de Abdelmalek Essaadi Tetouan**

Impact du vieillissement sur le comportement des transistors de puissance grand gap, application à l'efficacité des convertisseurs d'énergie

**Présentée et soutenue par
AL MEHDI BOUCHOUR**

Thèse soutenue publiquement le 01/12/2020
devant le jury composé de

M. Zoubir KHATIR	Directeur de recherche IFSTTAR, France	Rapporteur
M. Jamal ZBITOU	Professeur, Université Hassan Premier, Faculté des Sciences et Techniques de Settat, Maroc	Rapporteur
M. Abdeljabbar CHERKAOUI	Professeur, Université Abdelmalek Essaadi, ENSA de Tanger, Maroc	Rapporteur
M. Yassin LAAZIZ	Professeur de l'enseignement supérieure, Université Abdelmalek Essaadi, ENSA de Tanger, Maroc	Examineur
Mme. Mounira BERKANI	Maître de conférences à l'Université Paris Est Créteil UPEC, ESPE de l'académie de Créteil, France	Examineur
M. Olivier LATRY	Professeur, GPM, Université de Rouen Normandie, France	Directeur France
M. Ahmed EL OUALKADI	Professeur de l'enseignement supérieure, Université Abdelmalek Essaadi, ENSA de Tanger, Maroc	Directeur Maroc
M. Pascal DHERBECOURT	Maitre de conférences - HDR, Université de Rouen Normandie, France	Co-directeur France

Thèse dirigée par :

**M. Ahmed El Oualkadi
M. Olivier Latry
M. Pascal Dherbécourt**

**Université Abdelmalek Essaadi Tétouan, Maroc
Université de Rouen Normandie, France
Université de Rouen Normandie, France**



Centre des Etudes Doctorales :
« Sciences et Techniques de l'ingénieur »

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List of symbols

C: Capacitance of the supercapacitor [F]

C_0 : Initial value of C [F]

ESR: Equivalent Series Resistance of the supercapacitor [Ω]

ESR0: Initial value of ESR [Ω]

C_{iss} : Input capacitance [F]

C_{oss} : Output capacitance [F]

C_{rss} : Reverse transfer capacitance [F]

C_{GS} : Gate to source capacitance [F]

C_{GD} : Gate to drain capacitance [F]

C_{DS} : Drain to source capacitance [F]

D: Duty cycle

DC: Direct current

f_s : Switching frequency [Hz]

I_{DS} : Drain to source current [A]

I_{GSS} : Gate leakage current [A]

I_{DSS} : Drain leakage current [A]

I_{OUT} : Inverter output current [A]

L: Output filter inductance [H]

P_{GaN} , P_{SiC} , P_{Si} : Device power losses [Watt]

P_g : Gate power losses [Watt]

Q_g : Gate charge [C]

$R_{DS(on)}$: Drain to source on-state resistance [Ω]

g_m : Transconductance [S]

n_s : 2DEG carrier density [cm]

P_{PZ} : Piezoelectric polarization [C.cm⁻²]

P_{SP} : Spontaneous polarization [C.cm⁻²]

q: elementary charge [C]

$\sigma_{2\text{DEG}}$: 2DEG charge density [cm^{-2}]

$\sigma_{\text{AlGaIn/GaN}}$: Polarization charge density at the interface [cm^{-2}]

σ_{SURF} : Surface charge density [cm^{-2}]

T_a : Ambient temperature [$^{\circ}\text{C}$]

T_j : Junction temperature [$^{\circ}\text{C}$]

V_{GS} : Gate to source voltage [V]

V_{DS} : Drain to source voltage [V]

V_{TH} : Threshold voltage [V]

List of acronyms

2D: Two dimensions

2DEG: Two-dimensional electron gas

GaN: Gallium nitride

AlGaN: Aluminum gallium nitride

HEMT: High-electron-mobility transistor

III-V: Material being formed by elements from the 3rd and 5th column of the table of elements

DUT: Device under test

IGBT: Insulated-gate bipolar transistor

JFET: Junction gate field-effect transistor

MOSFET: Metal oxide semiconductor field-effect transistor

Si: Silicon

SiC: Silicon carbide

WBG: Wide-bandgap

SPICE: Simulation Program with Integrated Circuit Emphasis

SOA: Safe Operating Area

IGBT: Insulated-gate bipolar transistor

JFET: Junction gate field-effect transistor

MOSFET: Metal oxide semiconductor field-effect transistor

FMECA: Failure Modes, Effects and Criticality Analysis

PWM: Pulse width modulation

RF: Radio frequency

Abstract

In this thesis, we have studied the impact of aging the GaN HEMT on the power converter efficiency. For that, we have developed an experimental methodology to estimate the power losses of the GaN HEMT for switching circuit applications. The estimation of the power losses is performed by a SPICE simulation approach using a non-segmented Electro-thermal model. The developed methodology enables the estimation of both the static and dynamic power losses in power converter applications.

Additionally, we have implemented an accurate method for extracting both the intrinsic and extrinsic elements of the GaN HEMT power transistors. The experimental setup includes: Vector Network Analyzer, IVCAD measurement modules, drain and gate bias tees. The developed S-parameter setup enables the extraction of the parasitic elements of the power GaN HEMT at multiple bias conditions. The Annealing algorithm is chosen for the optimization of the model parameters. This method enables to study the effect of aging on both the parasitic elements of the GaN HEMT.

Moreover, we have investigated the aging of a 650 V, 30 A GaN HEMT power transistor under operational switching conditions. The switching stress respects the Safe Operation Area (SOA) of the tested transistor. Various types of stress are performed, such as: continuous operational switching stress, on-state, off-state and frequency step stresses. The aging campaigns lasted 1000 h and was carried out through a developed switching application with high power efficiency. During aging, several electrical characterizations were performed for monitoring both the dynamic and static characteristics of the device under test, including: pulsed I-V, leakage current, C-V, S-parameters, temporal switching measurements. The effects of this degradation on power converters are studied for both the static and dynamic characteristics of the aged GaN HEMT. Using the developed SPICE model, the conduction power losses, switching power losses, leakage current gate and drain power losses are estimated before and after of aging. The accuracy and consistent convergence of the developed SPICE model provide a good way to investigate the reliability of GaN HEMTs by simulation.

Keywords: GaN, HEMT, S-parameter, DC-DC power converters, aging, SOA, power losses.

Résumé

Ce travail de recherche s'inscrit dans la problématique de l'efficacité énergétique des convertisseurs de puissance à base des transistors GaN-HEMTs, cette thématique représente une importance primordiale pour des domaines tels que les transports, les énergies renouvelables ou encore les télécommunications.

Les travaux développés dans cette thèse se déroulent en cotutelle entre l'Université Abdelmalek Essaadi de Tétouan-Maroc et l'Université de Rouen Normandie-France, ce travail représente un intérêt réel pour les industriels internationaux et pour l'agence marocaine pour l'énergie durable au Maroc, puisqu'il traite une problématique actuelle qui est celle de la fiabilité et l'efficacité énergétique des convertisseurs de puissance. Notre travail s'inscrit donc dans le développement de la technologie électronique dans le cadre d'un partenariat Maroc-France.

Actuellement, les composants de puissance de nouvelle génération de technologie GaN (nitride de gallium) ou SiC (carbure de silicium) remplacent peu à peu les technologies usuelles à base silicium. Des modèles électriques rencontrés en littérature sont adaptés à ces composants, cependant leur intégration dans les systèmes de conversion d'énergie nécessite de connaître avec précision l'évolution de ces modèles face au stress subi, en premier lieu thermique et électrique.

Ce travail de recherche consiste dans un premier temps à étudier l'impact des dégradations sur les éléments du modèle du composant à l'étude. Puis, dans un second temps, à partir du modèle, nous analysons l'impact des dégradations sur les performances d'un convertisseur de puissance.

Concernant les applications mobiles alimentées par batterie comme les véhicules électriques, les avions « plus électriques » ou les applications photovoltaïques, une haute efficacité énergétique combinée à un poids faible et une conception compacte sont des exigences clés.

En utilisant des semi-conducteurs à grand gap comme le GaN, il est possible de travailler avec des fréquences de commutation plus élevées. Par conséquent, le volume et le poids des composants magnétiques et des condensateurs peuvent être réduits de manière significative.

En raison de leurs caractéristiques, les composants de technologie GaN constituent un choix crucial pour les convertisseurs DC-DC fonctionnant à des fréquences de commutation allant au-delà de quelques centaines de 100 kHz jusqu'au MHz.

Malgré les nombreux avantages qu'apporte la technologie GaN comparée par la technologie Si, la fiabilité doit encore être démontrée. Cela est dû d'une part à l'évolution continue du processus technologique adopté, et d'autre part en raison du manque d'information concernant les modes et les mécanismes de défaillance.

La contribution de ce travail de recherche se situe essentiellement au niveau de l'étude de l'impact du vieillissement d'un composant GaN HEMT commercial sur l'efficacité énergétique des convertisseurs DC-DC. L'étude consiste à la réalisation des tests de vieillissement en commutation dans des conditions opérationnelles de fonctionnement. Les pertes dynamiques et statiques du composant sont estimées avant et après les tests de vieillissement. Par conséquent, l'impact du vieillissement sur le rendement du convertisseur DC-DC est déterminé.

Afin de réaliser ce travail, le banc de mesure des caractéristiques courant-tension (I-V) pulsé est exploité afin d'estimer les pertes de puissance de conduction à l'état passant d'un composant GaN HEMT commercial. La caractérisation I-V en mode pulsé permet de placer le transistor sous test dans un mode de fonctionnement très proche de celui de son utilisation réelle.

La caractérisation expérimentale constitue un atout indéniable pour réussir ce projet de thèse. A ce sujet, le banc de mesure des caractéristiques capacité-tension (C-V) est exploité afin d'estimer les pertes de commutation du GaN HEMT.

La technologie des transistors GaN HEMTs représente une importance primordiale pour les applications de convertisseurs de puissance. Cependant, comme toute technologie émergente, la question de la fiabilité des transistors GaN HEMTs s'impose, car il y a peu de retour d'expérience sur cette technologie et une instabilité sur la maîtrise des processus de fabrication, notre étude s'intègre dans cette démarche de fiabilité.

Pour aborder cette problématique, nous avons réalisé des tests de vieillissement en commutation dans des conditions opérationnelles. Le comportement statique et dynamique du transistor est impacté par les dégradations physiques causées par le stress thermique et électrique.

Les objectifs de cette thèse sont :

- Étudier le vieillissement du transistor GaN HEMT 650V, 30A en conditions opérationnelles de fonctionnement.
- Réaliser plusieurs campagnes de vieillissement dans diverses conditions opérationnelles.
- Suivre l'évolution des caractéristiques dynamiques et statiques du transistor de test pendant 1000 h de vieillissement.
- Étudier les indicateurs de défaillance du GaN HEMT à partir des caractérisations expérimentales et comparer les résultats obtenus avec la littérature.
- Pour aider à répondre à ces objectifs, mettre en place au sein du laboratoire un banc expérimental d'extraction automatique des éléments parasites de transistors de puissance en utilisant des paramètres S à multiples points de polarisation.
- Mettre en œuvre une méthodologie expérimentale de mesure des caractéristiques C-V des transistors GaN HEMT.
- Concevoir un modèle SPICE précis de GaN HEMT de puissance pour les applications de convertisseurs de puissance.
- Identifier l'impact du vieillissement du GaN HEMT sur l'efficacité des convertisseurs de puissance. Ceci est d'un très grand intérêt pour les concepteurs de circuits de commutation, car il est alors possible de prendre en compte les effets de la dégradation des transistors GaN de puissance sur leurs systèmes.

Pour répondre aux objectifs, cette thèse est organisée en six chapitres :

Le chapitre 1 présente l'introduction générale. Dans ce chapitre, les challenges majeurs de la technologie GaN HEMT dans les applications de convertisseurs de puissance sont présentés. Aussi, les objectifs de ce projet de thèse sont définis et une description du plan de ce rapport de thèse est donnée.

Le chapitre 2 présente l'état de l'art des transistors de puissance GaN HEMT. Une étude du marché des convertisseurs de puissance est présentée afin de justifier le besoin des nouvelles technologies de transistors à base du GaN. De plus, ce chapitre décrit les propriétés physiques du matériau GaN ainsi que les avantages et les principales applications du GaN HEMT. Les limites des composants au Silicium et le besoin de technologies émergentes telles que : le GaN

et le SiC sont analysées dans ce chapitre. Les avantages et les principales applications des GaN HEMTs sont présentés.

Ensuite, une comparaison des performances statiques et dynamiques entre le GaN et son concurrent SiC est développée en utilisant une approche de simulation SPICE. Cette étude est suivie par la présentation des propriétés physiques du matériau GaN. La formation du gaz d'électrons bidimensionnel (2DEG) est expliquée sur la base de l'interaction d'une couche de GaN avec une couche mince de l'AlGaN.

Une description de la structure physique GaN HEMT est développée. Une étude comparative des différentes technologies du GaN HEMTs est présentée. De même, les différentes modes de défaillance du GaN HEMT dans des conditions de commutation sont synthétisées suivant une analyse AMDEC. En outre, les diverses techniques de vieillissement pour évaluer la fiabilité des GaN HEMT de puissance sont discutées. Aussi, pour l'estimation des pertes de puissance du GaN HEMT selon une approche de simulation, plusieurs modèles du GaN HEMT sont comparés aux données issues de la littérature.

Le chapitre 3 présente une méthodologie complète pour l'estimation des pertes de puissance du GaN HEMT basée sur des mesures expérimentales. Le banc de commutation et les bancs de mesure I-V et C-V sont présentés. Les caractérisations I-V pulsé, C-V et le courant de fuite sont réalisées à différentes températures variant de 5 ° C à 115 ° C par pas de 10 ° C. L'effet de la température sur les caractéristiques statiques et dynamiques du GaN HEMT est étudié et comparé aux données présentes dans la littérature. L'effet de la fréquence sur les mesures C-V est étudié.

Le modèle SPICE choisi pour le GaN HEMT présente des faibles erreurs par rapport aux mesures expérimentales. Une étude comparative du modèle électrothermique utilisé avec d'autres modèles de la littérature est réalisée. Le modèle utilisé montre une bonne convergence avec les mesures expérimentales. Aussi, le modèle prend en considération l'effet de la température ce qui permet l'estimation des pertes de puissances avec une grande précision.

Les pertes de puissance du transistor sous test sont estimées sur la base d'une approche de simulation SPICE pour les applications de convertisseur de puissance. L'évolution des pertes de conduction et de commutation est modélisée en fonction de la température variant entre 5°C et 115 °C et pour un courant de sortie variant de 0 à 20A.

Sur cette base, nous avons construit un modèle précis de pertes de puissance du GaN HEMT basé sur des mesures expérimentales. Le rendement d'un convertisseur de puissance DC-DC 30 V / 200 V à base du GaN HEMT est estimé pour une application d'énergie solaire.

La méthodologie proposée pour l'estimation des pertes de puissance sera exploitée dans le chapitre 5 pour étudier l'impact du vieillissement du GaN HEMT en condition de commutation opérationnelle sur le rendement des convertisseurs de puissance.

Le chapitre 4 présente une méthodologie expérimentale pour extraction des éléments intrinsèques et extrinsèques du GaN HEMT de puissance sur une large gamme de fréquences : de 100 kHz à 200 MHz par un pas de 100 kHz. La méthodologie de mesure des paramètres S est vérifiée sur des composants passifs, tels que : un condensateur, une inductance, une résistance et sur des composants actifs, comme : les transistors GaN HEMT et SiC MOSFET.

Après description de la procédure de calibration, l'étude de la répétabilité des mesures est effectuée. Ensuite, la mesure des résistances d'accès et des inductances ainsi que des capacités est présentée. La mesure des paramètres S est effectuée sur le GaN HEMT à la fois à l'état froid et à de multiples points de polarisation.

Le banc de mesure des paramètres S réalisé permet l'extraction automatique des paramètres parasites d'un transistor à multiples points de polarisations et utilisant l'algorithme d'optimisation « Annealing ».

La modélisation des éléments parasites de GaN HEMT est donc réalisée en utilisant l'approche de simulation des paramètres S. L'extraction des éléments parasites du GaN HEMT est réalisée avec une grande précision. Cette méthode est utilisée dans le chapitre 5 pour étudier l'effet du vieillissement du GaN HEMT dans des conditions de commutation opérationnelle sur les éléments parasites du GaN HEMT.

Dans le chapitre 5, nous présentons les effets du vieillissement du transistor de puissance GaN HEMT dans des conditions de commutation opérationnelles à fort courant et à haute tension. De telles études sont d'une grande importance, car le GaN HEMT est soumis à des conditions similaires à ce qui serait vécu dans une application réelle de convertisseurs de puissance.

De plus, pour classifier les mécanismes de dégradation du GaN HEMT pour les applications de convertisseur de puissance, nous avons réalisé plusieurs campagnes de vieillissement, à savoir : stress en commutation continue, step-stress sur la grille, sur le drain et en fréquence de commutation.

Aussi, une analyse des modes de défaillance et de leurs effets (AMDEC) du GaN HEMT pendant 1000 h de vieillissement en commutation est présentée. Au cours des campagnes de vieillissement, nous avons surveillé les changements des caractéristiques I-V, C-V et des paramètres S. Les caractéristiques électriques statiques et dynamiques du GaN HEMT sont mesurées en fonction du temps de stress et sont modélisées.

L'impact du vieillissement sur l'efficacité énergétique des convertisseurs de puissance à base de GaN HEMT est estimé pour une application d'énergie renouvelable. Les pertes de conduction et commutation sont calculées avant et après vieillissement.

Le chapitre 6 présente une conclusion générale de la thèse et les études futures possibles sur les transistors GaN HEMT de puissance. Aussi, les contributions majeures de la thèse sont définies et présentées comme suit :

- Développement d'une méthodologie d'estimation des pertes de puissance statiques et dynamiques du GaN HEMT. Cette méthode est basée sur des caractérisations expérimentales I-V pulsé, C-V et du courant de fuites. La précision et la convergence cohérente du modèle SPICE utilisé fournissent un bon moyen d'étudier l'impact du vieillissement du GaN HEMT sur le rendement des convertisseurs de puissance par une approche de simulation.
- Développement d'un banc expérimental de caractérisation des paramètres S. Ce banc permet l'extraction des éléments parasites du GaN HEMT automatiquement et à multiples points polarisation. La méthode développée pour l'extraction des paramètres intrinsèques et extrinsèques est générique et peut être appliquée à plusieurs types de composants de puissance.
- La plupart des études existantes dans la littérature concernent la fiabilité du GaN HEMT dans des conditions statiques. Ce travail étudie le vieillissement du GaN HEMT de puissance dans les conditions de commutation opérationnelles des convertisseurs de tension DC-DC.
- Le banc de vieillissement proposé permet d'étudier l'impact des électrons chauds sur le GaN HEMT à haute courant et tension avec une faible consommation d'énergie.
- Les divers types de vieillissement réalisés permettent de classifier les modes de défaillance du GaN HEMT pour chaque mode de fonctionnement dans les applications de convertisseur de puissance.

Mots clés : GaN, HEMT, paramètres S, convertisseurs de puissance DC-DC, vieillissement, SOA, pertes de puissance.

Chapter 1: Introduction

Investigating the impact of aging the power GaN HEMTs under operational switching conditions is receiving an increasing interest from research laboratories worldwide. The attention of academics and industrials on the power converters efficiency is accelerated by the impressive growth of GaN HEMTs market, due to their high superior performances compared to those of Silicon power transistors. Their applications are in various domains, such as renewable energy and high-power engineering.

The estimation of power losses with high convergence to measurements is necessary to design efficient power converters using GaN transistors. The authors in [1] have proposed an estimation of power losses based on a look-up tables of energy losses to estimate the switching losses of IGBTs. Also, the authors in [2] have estimated and compared the switching power losses of GaN HEMTs to equivalent Si devices such as IGBT and MOSFETs.

For that, an accurate model is necessary. In the literature, several behavioral models of GaN transistor have been proposed. References [3] and [4] show a simple and accurate segmented behavioral model, which include the important static parameters of the GaN HEMTs. However, these models suffer from the discontinuity of the simulated curves, because the used equations are divided into three segments according to cutoff, linear and saturation regions.

In this work, we estimate both the static and dynamic losses of power GaN HEMTs. Moreover, we used a smooth and continuous behavioral model to estimate the efficiency of DC-DC power converter circuits before and after operational switching aging.

Moreover, to validate the robustness of power GaN HEMTs, JEDEC standardized tests for Si power transistors are used [5]. However, the standardized tests for Si are not enough to guarantee the robustness of GaN transistors when they are used in power converter applications, because the reliability of GaN under switching operation is different from that of Si transistors [6]. Therefore, running GaN HEMTs power transistors under accelerated conditions would cause many non-GaN failures.

In the literature, the reliability of GaN HEMTs has been improved. Reference [7] classifies the degradation modes of GaN HEMT in switching mode DC power converter into three classes: on-state, off-state and semi-off state. According to [8], one of the major disadvantages limiting the reliability of GaN HEMTs for switching power applications is hot electron effects that occurs during the switching state. In [9], this degradation result in decreased DC and RF performance.

According to [10], it is important to study the reliability of GaN HEMT for power conversion circuits. This work presents a developed reliability methodology under operational switching conditions. The proposed aging switching bench presents high power efficiency. The effects of aging GaN HEMT transistor on a power converter application are studied by SPICE simulation approach.

The devices investigated on this thesis are based on the gallium nitride (GaN) material. GaN is a III-V compound semiconductor with various physical properties such as wide band gap, large breakdown electric field, strong mechanical and thermal stability and good heat conductivity. In this first chapter, a general overview of the GaN power devices is given. Therefore, the objectives and the outline of this research work are presented.

1.1 GaN HEMT for power converter applications

Power switching devices are used in DC-DC converters to convert voltages. In order to provide an efficient conversion, an ideal switching device should guarantee zero static and dynamic losses. The static losses are due to the parasitic resistance of the device (R_{ON}) when it is in the on-state and due to the leakage current when is in the off-state. However, the dynamic power loss is induced during the switching from the on-state to the off-state and vice versa.

Furthermore, the possibility of having a power switching device able to operate at high switching frequencies would allow to reduce the size of passive components present in today DC-DC converts, this can significantly reduce the overall converter size. Nowadays, the Si MOSFET technology is reaching the limit [11]. Hence, emergent technologies have to be considered to go beyond the limit of Si devices.

Due to the large critical electric field, the GaN material is considered to replace Si technology. The large critical electric field of the GaN is combined with the high two-dimensional electron gas (2DEG) density, which is spontaneously generated at the AlGaIn/GaN heterostructure interface, hence, with intrinsically low resistivity.

As a result, due to the high-density and low-resistivity 2DEG in comparison to the Si technology for the same current target value, AlGaIn/GaN HEMTs guarantee a smaller on-resistance with smaller overall device area. Moreover, a smaller parasitic capacitance compared to other Si devices. Only the SiC based devices appear to be able to compete with the GaN. However, the GaN has lower dynamic losses, highest density and switching frequency.

Despite the high performances of the GaN HEMT in power converter applications, this technology still has various challenges to overcome for both a wide use and highly confident in the power converter market. The GaN HEMT challenges are presented in the following.

1.1.1. Normally-off challenge

One of the challenges that the GaN technology had to overcome in order to enhance its performances on the power switching market was the creation of the GaN normally-off devices. In fact, naturally GaN transistors are normally-on devices and most of the advantages of this technology are due to the spontaneous formation of the 2DEG channel without applying any gate voltage. However, for switching applications normally-off devices are required for safety reasons. Today, various companies have commercialized normally-off devices with high operating voltage (1000 V). Their performances in term of dynamic and static losses are better than the Si devices for the same operating voltage. According to the power GaN HEMT roadmap [12], it is recommended to study the normally-off GaN HEMT technology for power converter circuits. This thesis fulfils the recommendation of the GaN power roadmap. For that, we have investigated both the reliability and the power efficiency of the p-GaN normally-off technology as required in the power converter market.

1.1.2 Power losses estimation

The estimation of the GaN HEMT losses offers to the power converter designers the possibility to estimate the power losses of GaN HEMT with high accuracy without the use of

the complex switching bench, which reduces the time to market and cost. To accurately design a power converter with GaN HEMT, it is important to calculate the power losses of the device. For that, we have presented in chapter 3 an experimental methodology for the estimation of both the static and dynamic power losses of the GaN HEMT using C-V and I-V measurement. The impact of the GaN HEMT losses on the efficiency of power converts are modelled using SPICE simulation approach. This accurate methodology enables to identify the impact of aging the GaN HEMT on the efficiency of power converts.

1.1.3. Gate driver

Another major constraint is driving the GaN high speed transistors. The studied power GaN HEMT is a GaNPX package [13] and not a standard wire-bonded, leaded packages, such as TO-220. Integrating the GaN HEMT in such package reduces parasitic inductances and optimizes switching performance. However, to design the gate driver and for the estimation of total power losses of the device, it is important to accurately evaluate the parasitic element of the device. In chapter 4, we have presented an accurate method based on the S-parameters measurements for the extraction of the GaN package parasitic resistances, capacitances and inductances.

1.1.4. Reliability challenges

Reliability is essential for the application of GaN power devices to critical electronic systems, for high voltage energy conversion, control of electrical engines, automotive electronics. However, the main challenge of GaN-HEMTs for wide commercialization, concerns the study of reliability.

The reliability of AlGaIn/GaN HEMTs can be limited by several breakdown mechanisms, which can be mainly summarized in [14] as:

- The current collapse has been one of the critical issues for GaN transistors, where the drain current is reduced and thus ON-state resistance is increased once a high drain bias is applied to a GaN transistor. The current collapse is caused by the negative charge trapping in the structure under high-voltage stress. The increase in dynamic $R_{DS(on)}$ elevates the device temperature, which in turn can result in a thermal instability and finally device destruction. The current collapse has been investigated in this thesis under operational switching conditions.
- Degradation at the gate edge: this failure mode takes place in the off-state, results in an increase of leakage current, and is accelerated by the electric field. This can be induced by trap creation and formation of conductive paths between the gate and channel.
- In hard switching conditions, GaN HEMTs may be simultaneously subject to high drain voltage and nonnegligible drain current. The electrons injected from the source are accelerated by the electric field thus becoming “hot”. The hot electrons may induce both a recoverable degradation, when they are trapped in the gate-drain access region, or a permanent degradation, if their energy is sufficient to promote the generation of lattice defects.

1.2. Thesis project description

This thesis project takes place in joint supervision between the Abdelmalek Essaadi University of Tetouan-Morocco and the University of Rouen Normandy France. The thesis research was performed in collaboration between the Laboratory for Communication Information Technologies (LabTIC) in Tangier, and the Group Laboratory for Materials Physics (GPM) in Rouen. The thesis work took place under the supervision of Mr. Olivier Latty, Mr. Ahmed El Oualkadi and Mr. Pascal Dherbecourt. During this thesis, I benefited from the PHC TOUBKAL scholarship. Also, two six-month and additional three month stays in France are funded through the PHC TOUBKAL project.

1.3. Objectives of this research work

This thesis objectives are:

- Study the aging of a 650V, 30A GaN HEMT transistors in real operating conditions.
- Perform multiple aging campaigns at various operational conditions.
- Monitor the dynamic and static characteristics of the DUT during 1000 h of aging.
- Investigate the failure mechanisms of the GaN HEMT based on experimental characterizations and compare the obtained results to the literature.
- Develop an accurate methodology for measuring both the dynamic and static power losses of the GaN HEMT in power converter applications.
- Estimate the impact of aging the GaN HEMT on the efficiency of power converters.
- Implement in the GPM laboratory an experimental bench for extracting the parasitic elements automatically of power devices using S-parameters at multi-bias.
- Develop a generic methodology for the extraction of both the intrinsic and extrinsic elements of power GaN HEMT for both at the cold state and under multiple bias conditions.
- Implement in the GPM laboratory an experimental methodology for measuring the C-V characteristics of the GaN HEMT transistors.
- Design an accurate SPICE Model of power GaN HEMT for switching circuit applications.
- Take into account the evolution of the elements of the model following aging in the simulated temporal waveform.
- Identify the impact of aging the GaN HEMT on the efficiency of power converts. This are of very high interest to circuit and system designers, as they will be eager to understand the effects of device degradation on their systems.

1.4. Outline of the thesis

This manuscript is organized as follows:

- Chapter 2 shows the state of the art concerning the GaN HEMT power transistors. Moreover, this chapter describes the fundamental properties of the GaN material as well the advantages and the major applications of the GaN HEMT power transistors.

- Chapter 3 presents a complete methodology for the estimation of the GaN HEMT power losses based on experimental measurement. The pulsed I-V, C-V and low current characterizations are performed at various temperatures: from 5 °C to 115 °C by a step of 10 °C. The power losses of the DUT are estimated based on a SPICE simulation approach for switching circuit applications. The evolution of the conduction losses and switching losses in power converter applications is modelled as a function of the junction temperature and the output current. As a result, we have built an accurate power losses model of the GaN HEMT based on experimental measurements, which include the major power losses in power converter applications. Using the extracted power losses model of the GaN HEMT, we have estimated the efficiency of a 30 V / 200 V DC-DC converter stage with GaN HEMT. The proposed methodology for the estimation of the GaN HEMT power losses is used in chapter 5 to study the impact of aging the power GaN HEMT under operational switching condition on the power converters efficiency.
- Chapter 4 presents an experimental methodology to extract parasitic elements of a packaged GaN power transistor over a wide frequency ranges: from 100 kHz to 200 MHz by a step of 100 kHz. In order to reach the best accuracy on the extraction of very low GaN device parasitics, a method based on S-parameter measurements and a specific calibration process using low-cost test fixtures are proposed. The S-parameters measurement methodology are verified on both passive components, such as: capacitor, inductor, resistor and on the tested GaN HEMT power. After detailing the calibration procedure, measurement of access resistances and inductances as well as voltage-dependent capacitances are presented. The S-parameters measurement are performed on the GaN HEMT in both the cold state and the multiple bias conditions. The non-linear model of the power GaN HEMT is extracted at multiple bias points which correspond to the power switching application load line. The modeling of parasitic elements of GaN HEMT is performed using S-parameters simulation approach. The extraction of the parasitic elements of the GaN HEMT with high accuracy using S-parameter method is used in chapter 5 to study the effect of aging the GaN HEMT under operational switching conditions on the parasitic component of the GaN HEMT.
- In chapter 5, we studied the effects of aging GaN HEMT power transistor under operational switching conditions at both high current and high voltage. Such studies are of great importance as the device is subjected to conditions similar to what would be experienced in a real application of power converters. Additionally, to separate the degradation mechanisms of the GaN HEMT in switching power converter mode, we have performed three step stress aging campaigns: frequency step stress, on-state step stress, off-state step stress. A failure mode and effects analysis (FMEA) of the GaN HEMT during 1000 h of step stress aging are presented. During the aging campaigns we have monitored the changes of the current-voltage (I-V), capacitance-voltage (C-V) and S-parameters characteristics. Both static and dynamic electrical characteristics of the devices are measured as a function of stress time and are modeled. Notably, these results are used to simulate the efficiency of a DC-DC buck converter using both fresh and aged devices.
- Chapter 6 summarizes the results presented in this thesis and possible future studies on the AlGaIn/GaN technology.

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Chapter 2: Context and state of art of GaN HEMT power transistors

2.1. Introduction

In this chapter, the state of art of the power GaN HEMT in power converter applications is discussed. Firstly, the limitations of Silicon devices and the need of emerging technology such as: GaN and SiC in the power switching market are analyzed. Also, the advantages and the major applications of the GaN HEMT devices are presented. Then, a comparison of both the static and dynamic performances between the GaN and its SiC competitor technologies is studied using a SPICE simulation approach. This is followed by presenting the physical properties of the GaN material. The formation of the two-dimensional electron gas (2DEG) is explained based on the interaction of a GaN layer with a thin layer of aluminum gallium nitride (AlGaN). Moreover, a description of the GaN HEMT physical structure is provided. Subsequently, the various degradations of power GaN HEMT under switching conditions are summarized. Furthermore, the diverse aging technics for evaluating the reliability of the GaN power devices are discussed. Finally, a brief description of the power losses modelling of the GaN HEMT is presented.

2.2. Context of the study

2.2.1. Improving energy efficiency through GaN technology

According to the international energy agency (IEA). The world energy demand rises by 1 % per year to 2040 [1]. The electrical energy consumption will increase from 47.21 % in 2018 to 68.87 % in 2040 compared to oil. As shown in **Fig. 2.1**, electricity uses grows at more than double of overall energy demand between 2000 and 2040 [2-3], confirming its place at the heart of modern economies.

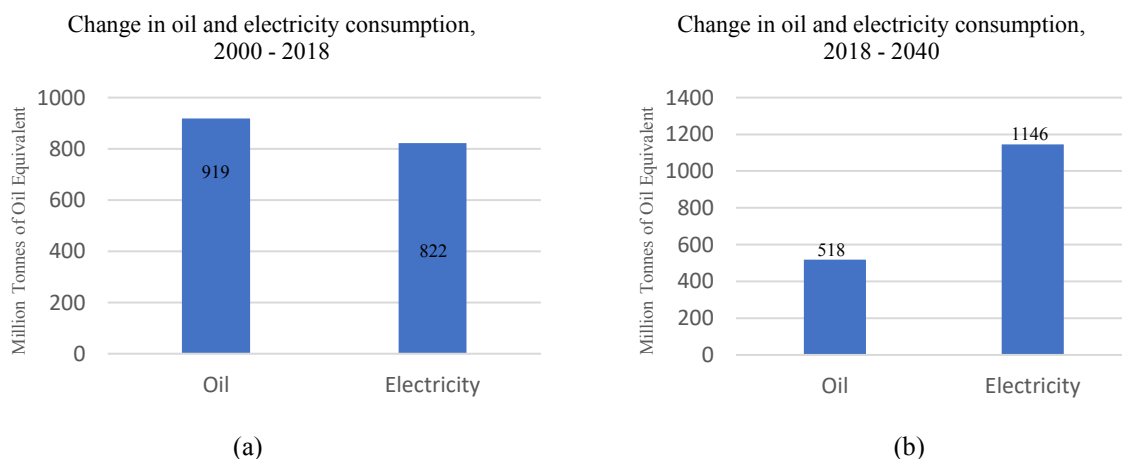


Fig. 2.1: Change in oil and electricity consumption outlook 2000-2040 [2-3].

However, 60 % of the produced electric energy is wasted before achieving the end-use stage for consumption [4]. **Fig. 2.2** shows the electric energy losses during the conversion steps of the consumption flow: production, generation, transmission until the end-use consumption. The

reduction of losses in power conversion applications is the key to improve the energy efficiency in order to ensure the increased demand of electric energy.

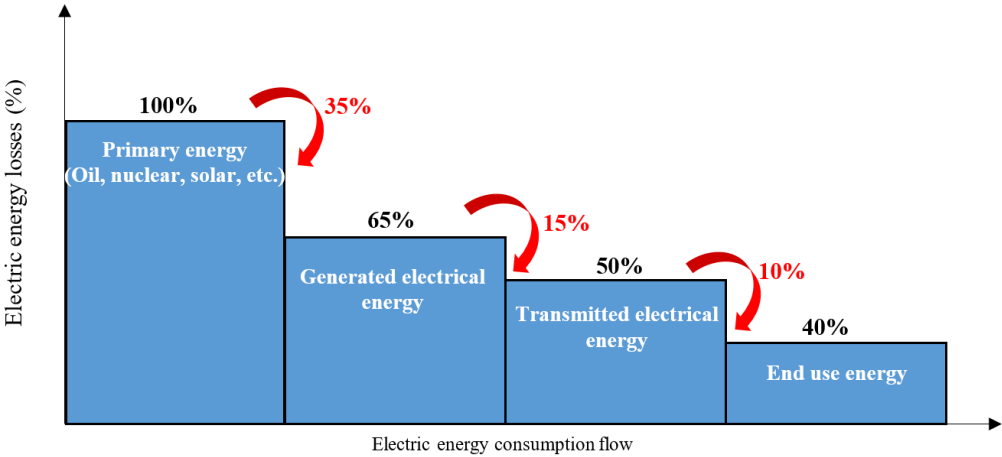


Fig. 2.2: Electric energy losses during the consumption flow [4].

Power converters are essential to ensure world electric consumption demand. They enable to distribute and use electric power, and to generate electrical energy from renewable sources (wind, solar, etc.). As shown in Fig. 2.3, power Si MOSFETs account for more than half the power loss in a buck converter application [5]. For more than five decades, power converters with silicon (Si) has been the dominant semiconductor for power electronics devices. However, today the increased demand for higher current, voltage and power density capability, as well as the need of a better energy efficiency to reduce the global energy consumption, are the driving forces to introduce new semiconductor, such as GaN technology in power electronics and to overcome the inherent limitations of Si-based devices.

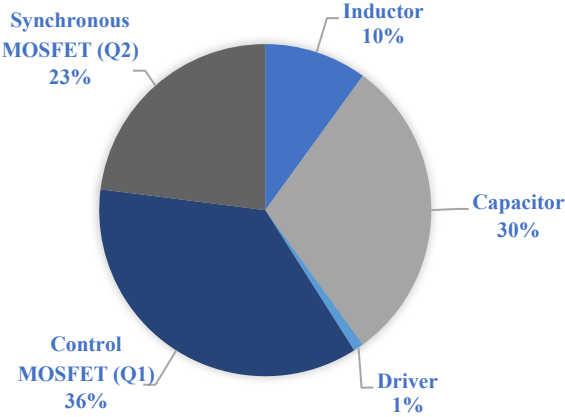


Fig. 2.3: Power losses in synchronous buck converter [5].

2.2.2. GaN power converters market

According to [6], the power GaN Market is expected to be multiplied 24 times between 2016 and 2022, from 12 million dollars in 2016 to 450 Million dollars in 2022. As illustrated in Fig. 2.4, the expansion of the GaN Market is mainly driven by the power converts applications DC-DC and AC-DC for power supply. Additional markets, including solar (PV), electric and hybrid electric vehicles (EV/HEV), are also driving forces behind this growth.

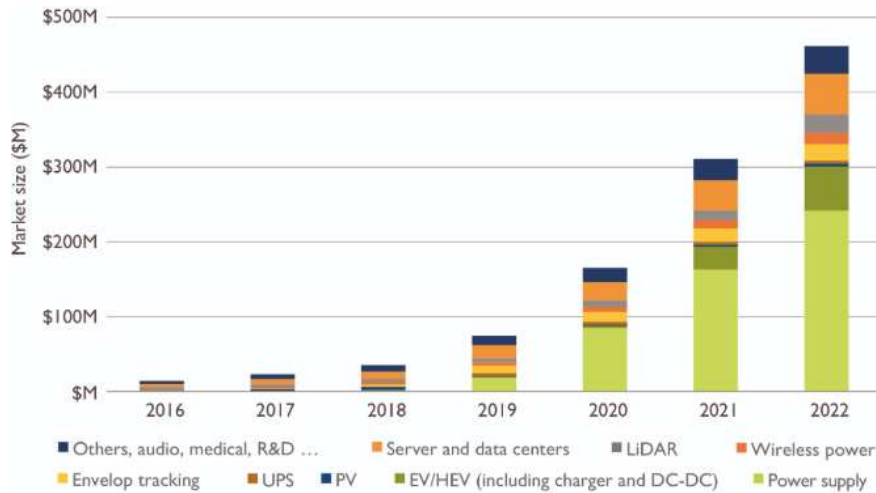


Fig. 2.4: GaN power device market by application (\$M) [6].

However, with US\$ 12 million in 2016, the GaN power market remains small compared to the US\$ 30 billion silicon power semiconductor market [7]. But the fast growth of the GaN market between the period of 2016 and 2020 is a sign for the beginning of the competition between GaN and Si markets.

To understand the reason of the fast expansion of the GaN market, we have analyzed the major GaN events that happened in the last few years. We have observed that the GaN technology has been successively achieved for a high operating voltage, high operating current, high power density, high switching frequency, and strong reliability.

In the following, we present the most relevant improvement of the GaN technology during the period between 2017 to 2020.

❖ **High voltage requirements:**

Before 2017, the GaN device market has been mainly dominated by low voltage devices < 600 V [7]. Hence, increasing the voltage capability of the GaN devices is a requirement for power system applications. In 2017, Transfom produces the first 900 V GaN product in the market for high voltage power conversion applications [8]. This product has earned the confidence of both renewable and the automotive industry since is the first GaN JEDEC and AEC-Q101 qualified. According to [9], the result of integrating this high voltage GaN product in a single-phase DC converter shows a high total efficiency of 99 %.

❖ **High current requirements:**

The high current requirements in power converters application is essential to meet the needs of systems in areas such as: electric vehicles, renewable energy, industrial motors electronics that are consuming ever more power. In 2019, Toyoda Gosei in Japan [10] has developed a vertical gallium nitride (GaN) power semiconductor device with high current operation of 100 A on a single chip. Which has doubled the electric current capacity from the previous 50 A to 100 A on a single chip. Also, in 2020, GaN System has announced world's highest current rated GaN Power transistor [11]. The emergent 120 A, 650 V GaN E-HEMT, offers much higher power levels in the automotive, industrial, and renewable energy industries.

❖ High power density requirements:

In 2018, EPC has introduced a 350 V GaN power transistor 20 times smaller than comparable silicon [12]. This 1.95 mm x 1.95 mm (3.72 mm²) product enables five times less area of power conversion circuits than a comparable silicon solution. Despite the small size of this product can handle thermal conditions more efficiently than plastic packaged MOSFETs.

Fig. 2.5 shows the size reduction of the GaN power converters compared to those with Si [13]. As shown in **Fig. 2.5 (a)**, the use of GaN power devices in designing AC power adapter enables lighter and up to quarter the current size with Si devices. In **Fig. 2.5 (b)**, the size and weight of energy storage systems with GaN for renewable energy applications is reduced 3 times compared to equivalent Si systems. **Fig. 2.5 (c)** shows power conversion module for industrial application. As shown in this figure, using GaN power devices results in power supplies that are more efficient and higher power density. This results in significant system size reductions including opportunities to integrate functions into a single system.

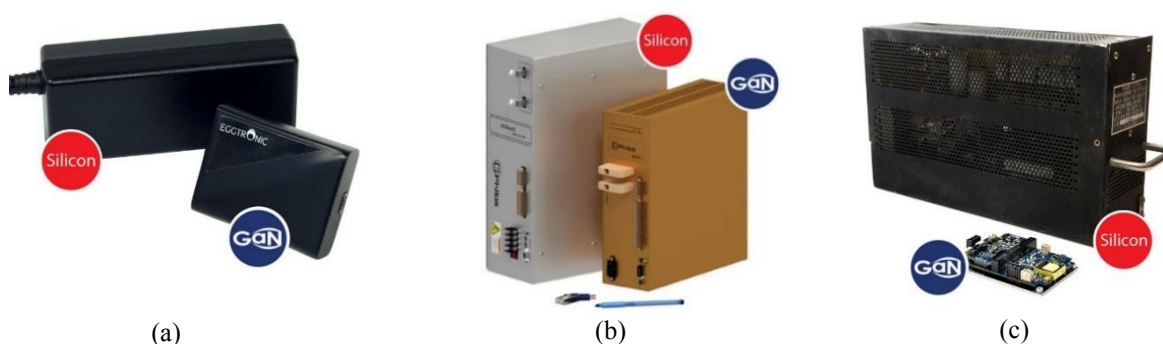


Fig. 2.5: GaN size equipment compared to Si [13]: (a) 65 W AC power adapter, (b) 1 kW ESS converter, (c) 3-Phase AC power conversion modules.

❖ High switching frequency requirements:

In 2020, 6 MHz buck converter evaluation board (GSWP050W-EVBPA) using GaN Systems 100V E-Mode GaN transistor and integrated high-speed driver [14]. This evaluation board exhibits much higher efficiencies than Si MOSFETs and exceeds performance in terms of switching speed, parasitic capacitance, switching loss, and thermal characteristics.

❖ High reliability requirements:

In 2019, the JEDEC wide bandgap power semiconductor committee publishes its first document [15]: test method for dynamic resistance of GaN HEMT for power conversion applications. This JEDEC committee establishes standards across suppliers for datasheet, qualification, and test methods for the consistent measurement of Drain-to-Source Resistance in the ON-state $R_{DS(ON)}$ encompassing dynamic effects. These dynamic effects are characteristic of GaN power FETs, and the value of the resulting measured $R_{DS(ON)}$ is method dependent.

2.2.3. GaN power converter applications

Fig. 2.6 shows the applications of Si, SiC and GaN devices in power electronics market based on power and frequency ranges. The migration from Si to WBG devices such as GaN and SiC, has been accelerated in the last few years. However, Si devices like Thyristors, IGBT and Si bipolar still be used in high power applications which do not require high switching frequency,

for example: power grid and wind energy. In the other side, SiC and GaN dominate the high frequency applications. Currently, GaN-transistors are ideal for high frequency power converts up to 1000 V, like: power supplies and audio amplifiers while SiC is rather suited for discrete devices or modules with breakdown voltages above 1000 V, such as: train transportation and photovoltaic.

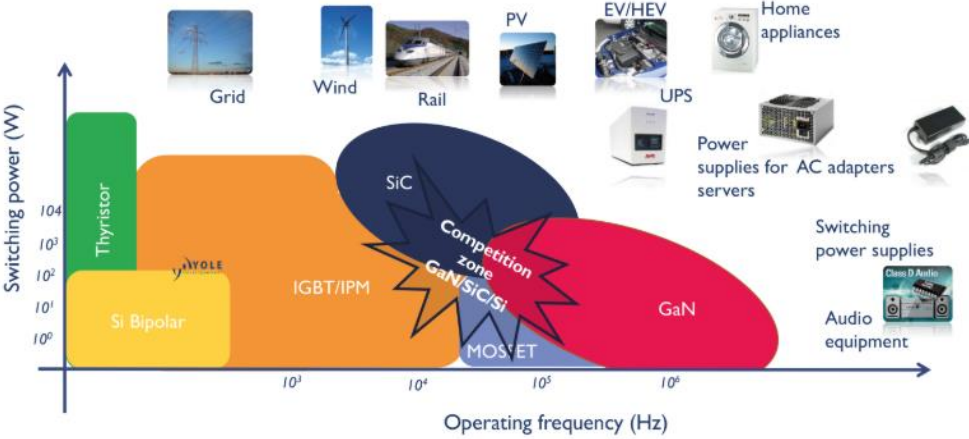


Fig. 2.6: Power vs Frequency on electronics: technology positioning in 2018 [6].

The GaN advantages in automotive, renewable energy and power converter markets are presented in the following:

❖ **Automotive GaN market:**

The number of electric and hybrid vehicles has increased rapidly in the world over the past few years and continues to accelerate. The electric vehicles market is expected to increase from 5 million electric vehicles in 2018 to reach 250 million new electric vehicles sold in 2030 [16]. The electricity consumption that accompanies that will rise from 58 TWh in 2018 to 640 TWh in 2030 [17]. That will require a new solutions of power devices to improve electricity pricing for vehicle charging, as well as new storage and efficient power converters systems.

For the automotive industry [18], GaN offers 3 times smaller power systems, 50 % power losses reduction and 20 % lower system cost. This means high performance electric vehicles with high energy efficiency and low cost. Fig. 2.7 shows the GaN advantages in the automotive applications industry.

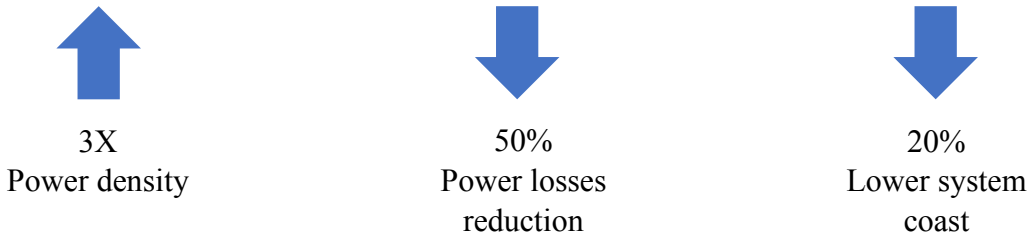


Fig. 2.7: GaN advantages in automotive applications compared to Si [18].

The GaN ability to reduce size, weight and improve electricity consumption are increasingly being used in EV and HEV applications such as chargers and power converters.

❖ Renewable energy GaN market:

Figure 2.8 shows the total renewable energy consumption outlook with projections to 2040. As can be shown, the renewable energy consumption will increase by 113.17 % between 2015 and 2040 [19]. Moreover, more than 25 % of global electricity generation is expected to come from renewable sources by 2020 [20]. This increased demand of renewable energy from 2165 trillion Megawatt-hour (MWh) in 2015 to 3845 trillion MWh in 2040, makes efficient power conversion systems with GaN devices more attractive for renewable energy industry.

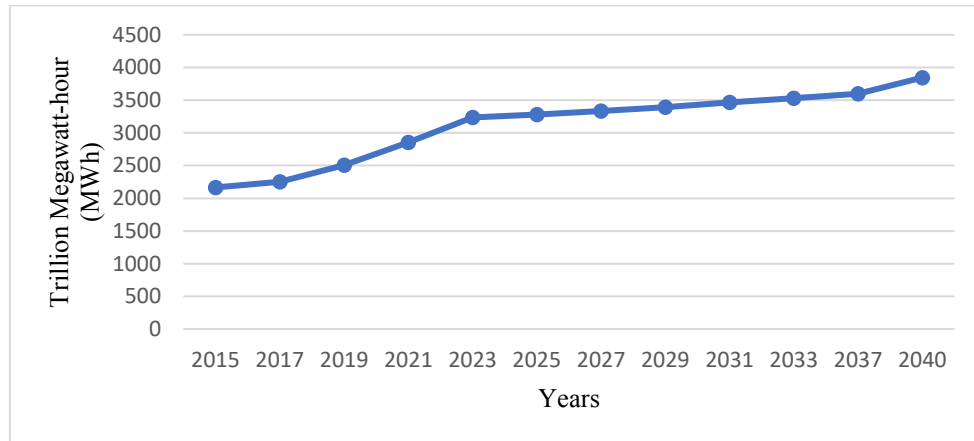


Fig. 2.8: Total renewable energy consumption outlook 2015-2040 [19].

For the renewable energy industry, GaN power transistors enable the design of simpler, lower cost, and more efficient energy storage systems that are not achievable with silicon [20]. **Fig. 2.9** shows the GaN advantages in the renewable energy industry.

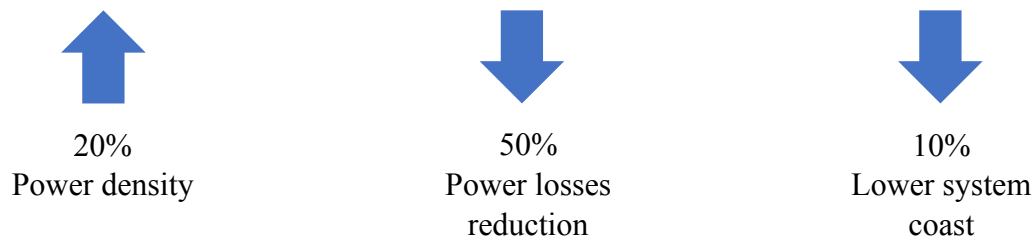


Fig. 2.9: GaN advantages in renewable energy applications [20].

❖ Energy GaN market:

Energy is the main engine for economy and the most important factor for the national security. According to the International Energy Outlook [21], the world energy demand will continue to rise up to 5% by 2040 and the natural gas and oil will still be the dominant source of energy for the next twenty years (**Fig. 2.10**). Therefore, the easy recoverable of gas and oil will be reduced, and their recovery will be from deep wells with hundreds of kilometers depth and high temperature varying from 180°C to 450°C.

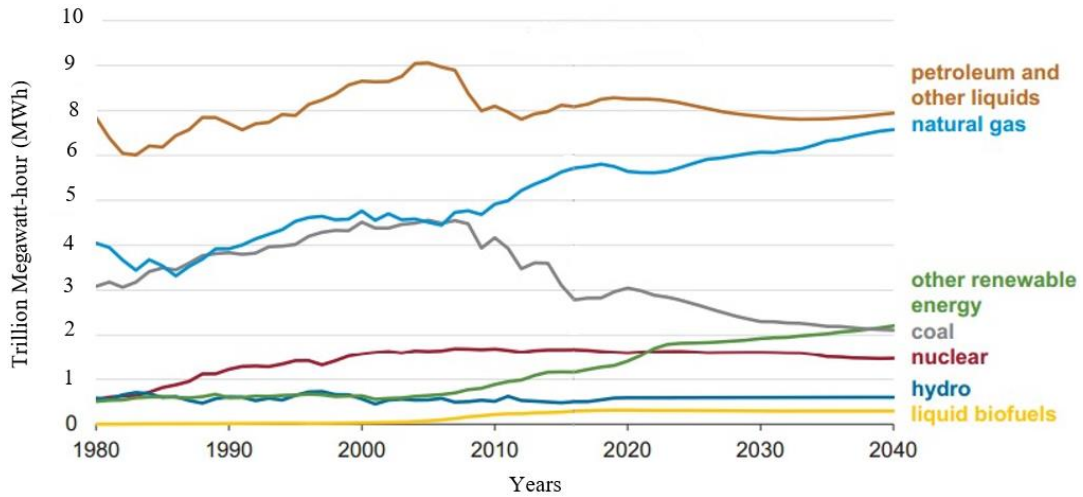


Fig. 2.10: World Energy Consumption [11].

In such a harsh, high temperature and high-pressure environment, electronic power converters based on Silicon (Si) cannot survive and the drillers have to explore these deep wells without an appropriate instrumentation. Drilling in this manner is very costly, slow and inaccurate. The GaN power converters can support high temperature and robust environment.

2.3. GaN and SiC power devices comparison

Silicon has been reached its limits and wide bandgap semiconductors will take the next step [22]. The first power device, a silicon carbide (SiC) Schottky-diode, became commercially available in 2001. Since then, also a variety of SiC switches became commercially available. Gallium nitride (GaN) emerged as another alternative wide bandgap material for power devices and the first commercial power GaN devices have been introduced to the market by EPC in 2010 [23].

In this section, we compare both the static and switching characteristics of two power transistors: GS66508P GaN HEMT from GaN SYSTEMS [24] and SCT2120AF SiC MOSFET from ROHM SEMICONDUCTOR [25]. The investigated devices have both similar breakdown voltages 650 V and maximum drain current 30 A. **Table 2.1** summarizes the electrical characteristics of the investigated transistors.

The performance of GaN and SiC transistors can be compared using the figure-of-merit (FOM). The FOM factor is calculated using (2.1) [26]:

$$FOM = R_{DS(ON)} \times Q_g \quad (2.1)$$

Where: $R_{DS(ON)}$ is the on-state resistance (Ω) and Q_g is the gate charge (nC). **Table 2.1** shows the comparison between the GaN and SiC FOM factor. As observed, the GaN HEMT FOM is 25 times lower than that of SiC MOSFET. This is due to both the low resistance and gate charge of the GaN HEMT compared to thus of SiC MOSFET. According to [27], the low FOM factor of the GaN HEMT compared to SiC MOSFET enables lower power losses, thus a high energy efficiency for power converters.

Table 2.1: Comparison of the investigated transistors characteristics of GaN HEMT and SiC MOSFET [24-25].

Parameters	GaN HEMT (GS66508P)	SiC MOSFET (SCT2120AF)
$I_{DS(max)}$ (A)	30	29
$V_{DS(max)}$ (V)	650	650
$R_{DS(ON)}$ (m Ω)	50	120
Q_g (nC)	5.8	61
FOM (Ω *nC)	0.29	7.32

In the following, we have compared using SPICE simulation both the static and dynamic characteristics of the selected GaN and SiC transistors presented in **Table 2.1**.

2.3.1. Static characteristics

The simulated I-V static characteristics of the studied GaN and SiC transistors at various temperatures varying from 25 °C to 105 °C are shown in **Fig. 2.11**. As observed, the SiC MOSFETs has a low temperature coefficient of ON resistance compared to the GaN HEMT. For the SiC MOSFET, on-resistance only increases by 12 % between 25 °C and 105 °C as shown in **Fig. 2.11**. However, the GaN HEMT on-resistance increases by 14.78 % between 25 °C and 105 °C.

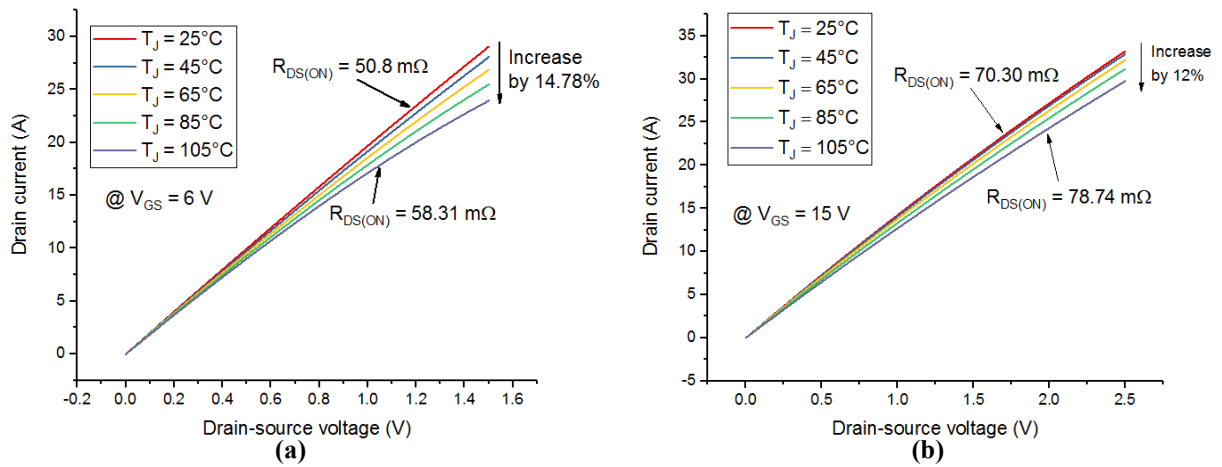


Fig. 2.11: Simulated output characteristic at various temperatures varying from 25 °C to 105 °C : (a) GaN HEMT (GS66508P) ; (b) SiC MOSFET (SCT2120AF).

From the simulated output characteristic in **Fig. 2.11**, we have calculated the R_{ON} resistance using (2.2):

$$R_{DS(ON)} = \left. \frac{V_{DS}}{I_{DS}} \right|_{V_{DS}=V} \quad (2.2)$$

Where: V_{DS} is the drain to source voltage and I_{DS} is the drain to source current. **Fig. 2.12** shows the simulated on-state resistance temperature dependence for both the GaN HEMT and SiC MOSFET. As observed, the SiC MOSFET has 35.03 % higher $R_{DS(ON)}$ than that of GaN HEMT. This enables to GaN power converter applications lower conduction losses compared to thus with SiC MOSFET.

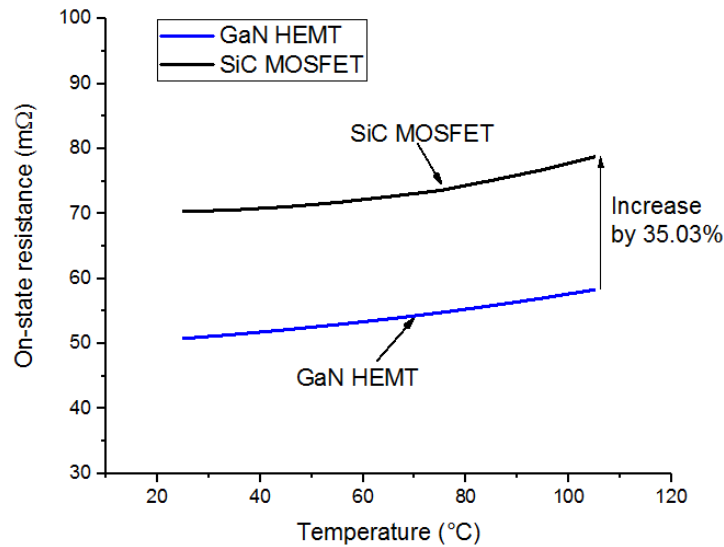


Fig. 2.12: Simulated R_{ON} comparison between GaN HEMT (GS66508P), SiC MOSFET (SCT2120AF).

By using GaN HEMT transistors in power converters, the conduction power losses are reduced 50 % than by using SiC MOSFET as shown in **Fig. 2.13**.

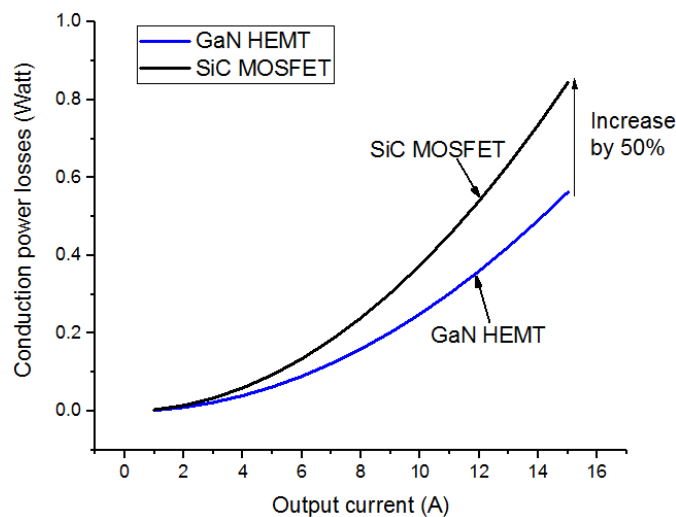


Fig. 2.13: Simulated conduction power losses comparison between GaN HEMT (GS66508P), SiC MOSFET (SCT2120AF).

To summarize this section of static characteristics, the SiC MOSFET has a lower temperature dependency of the R_{DS(ON)} resistance. However, the GaN HEMT has lower R_{DS(ON)} resistance, which enables reduced conduction power losses for power switching applications compared to SiC MOSFET.

2.3.2. Switching characteristics

The double-pulse test (DPT) has been used to compare and analyze the switching characteristics between the SiC MOSFET and GaN HEMT. A double-pulse test circuit is shown in **Fig. 2.14**. The DPT analyze enables to observe the switching transients of a the DUT without the self-heating of the device [28]. This test is done with a purely inductive load. This mode enables a similar electrical waveform on the DUT, which could exist in DC-DC power converters.

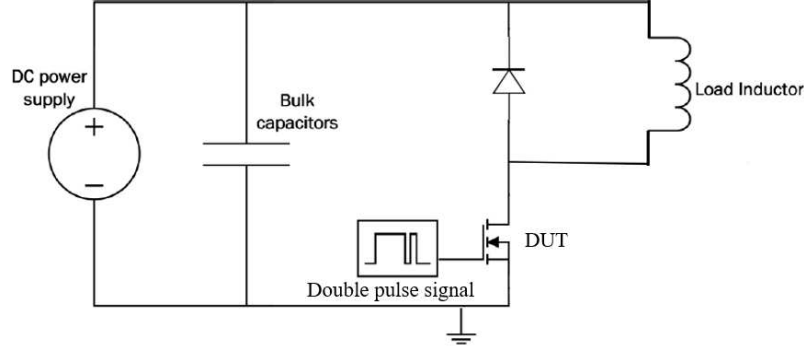


Fig. 2.14: Double-pulse setup with inductive load [28].

The first pulse turns on the DUT transistor in **Fig. 2.14** and charge a current through the inductor. The first pulse should be a wide pulse, which charges the load current to the magnitude. Then, a short break followed by a second short pulse appears.

The double pulse setup was implemented in SPICE simulator, which enables the comparison of the switching characteristics between both the studied GaN and SiC transistors. **Fig. 2.15** and **Fig. 2.16** show both the turn-off and turn-on waveforms at 400 V drain-to-source voltage and 20 A drain current for GaN HEMT and SiC MOSFET respectively. The switching losses in a power transistor depend on its turn-on (T_{ON}) and turn-off (T_{OFF}) transient times. The T_{ON} and T_{OFF} times are defined by (2.3) [29]:

$$\begin{cases} T_{ON} = t_{ri} + t_{fv} \\ T_{OFF} = t_{rv} + t_{fi} \end{cases} \quad (2.3)$$

Where t_{ri} is the current rise time and t_{fv} is the voltage fall time at turn-on. For T_{OFF} , t_{rv} is the voltage rise time and t_{fi} is the current fall time at turn-off. The rise time t_r and the fall time t_f are measured from 10 % to 90 % of the waveform switching level [29].

Based on the simulated switching waveforms in **Fig. 2.15** and **Fig. 2.16**, the T_{ON} and T_{OFF} switching times of both the GaN and SiC are calculated and presented in **Table 2.2**. As can be observed, The GaN has a lower switching time T_{ON} and T_{OFF} , which enables lower switching losses energy for power switching applications with GaN HEMT.

Table 2.2: Simulated switching time T_{ON} and T_{OFF} of GaN HEMT (GS66508P) and SiC MOSFET (SCT2120AF).

	GaN E_{OFF} T_{OFF1}	SiC E_{OFF} T_{OFF2}	GaN E_{ON} T_{ON1}	SiC E_{ON} T_{ON2}
Time width (μ s)	0.015	0.2	0.03	0.5

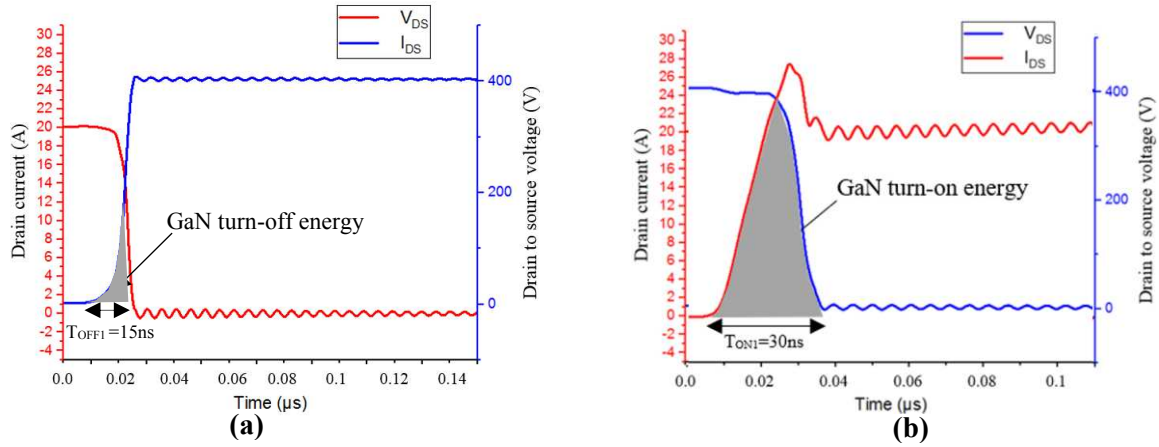


Fig. 2.15: GaN HEMT (GS66508P) drain current and voltage simulated switching waveforms at 25°C: (a) turn-off; (b) turn-on.

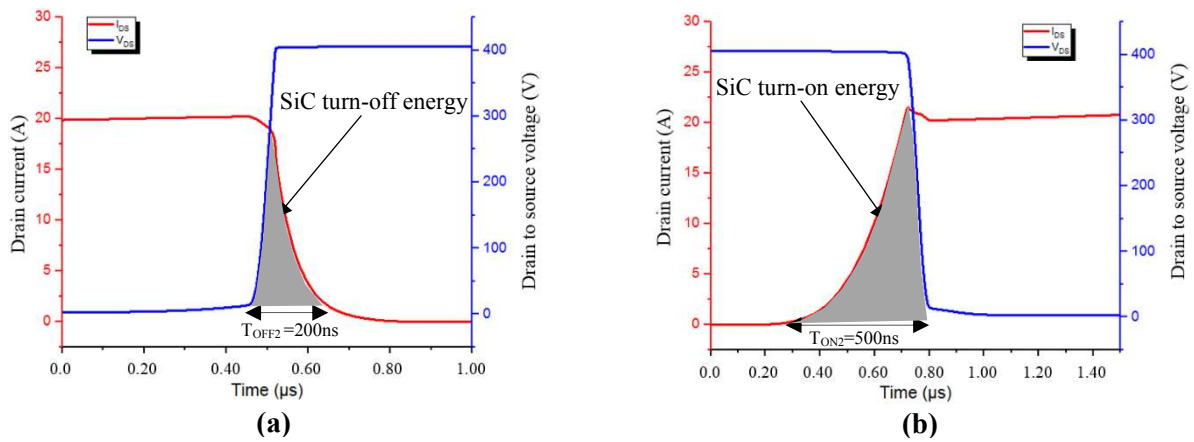


Fig. 2.16: SiC MOSFET (SCT2120AF) Drain current and voltage simulated switching waveforms at 25°C: (a) turn-off; (b) turn-on.

Fig. 2.17 shows the comparison of both the turn-on and turn-off switching losses energy between GaN HEMT and SiC MOSFET. As observed, E_{ON} losses of SiC MOSFET are 115 times higher compared to GaN HEMT. Similarly, the E_{OFF} losses of SiC MOSFET are 14 times higher compared to GaN HEMT.

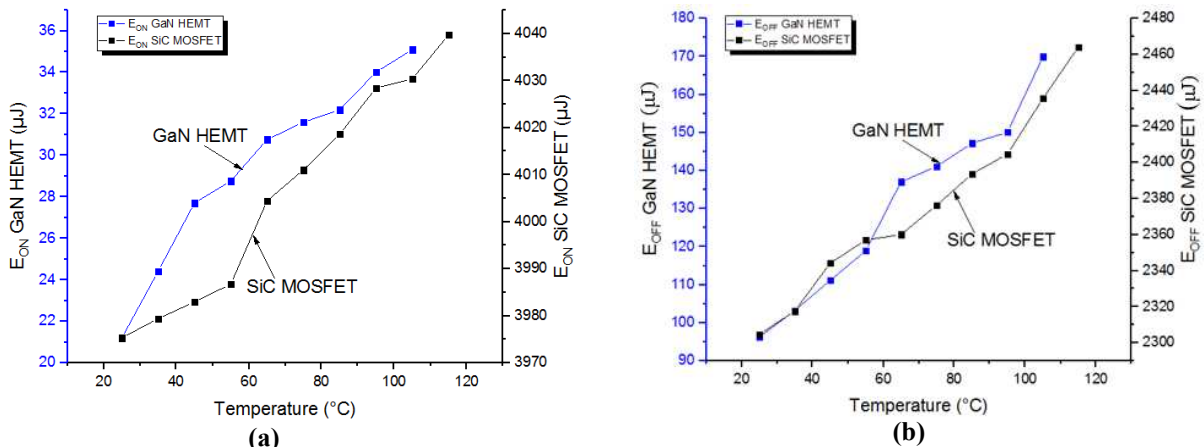


Fig. 2.17: GaN HEMT (GS66508P) and SiC MOSFET (SCT2120AF) simulated switching energy losses versus the temperature: (a) turn-on (E_{ON}); (b) turn-off (E_{OFF}).

The high turn-on and turn-off energy losses of SiC compared to GaN is due to the high switching times of the SiC MOSFET. As shown in **Table 2.2**, the GaN has lower switching times compared to SiC, which enables high energetic efficiency for GaN power switching applications.

To compare the switching losses of GaN HEMT and SiC MOSFET, we have calculated the total switching losses P_{SW} from the simulated switching I_{DS} current and V_{DS} voltage waveforms in **Fig. 2.15** and **Fig. 2.16**. P_{SW} is defined by (2.4) [29].

$$P_{SW} = P_{SW(on)} + P_{SW(off)} = \frac{1}{T_{ON}} \int_0^{T_{ON}} i_{ds} \cdot v_{ds} \cdot dt + \frac{1}{T_{OFF}} \int_0^{T_{OFF}} i_{ds} \cdot v_{ds} \cdot dt \quad (2.4)$$

Where v_{DS} and i_{DS} are the simulated drain-to-source voltage and the drain current, T_{ON} is the turn-on time and T_{OFF} is the turn-off time. The value of T_{ON} and T_{OFF} for both the GaN HEMT and the SiC MOSFET are obtained from **Table 2.2**. The evolution of the simulated switching losses for both GaN and SiC for a range of frequency varying from 50 kHz to 200 MHz is shown in **Fig. 2.18**. This interval of frequencies is very used in power switching applications. **Fig. 2.18** shows that the switching losses of SiC transistors increases by 38.46 % from 50 kHz to 200 MHz compared to GaN power transistor.

The responsible mechanism for this phenomenon is the high parasitic capacitances of the SiC compared to GaN. As shown in **Fig. 2.19**, the GaN has lower input capacitance (C_{iss}) and output capacitance (C_{oss}) compared to SiC MOSFET. This results in low switching power losses for GaN power switching applications.

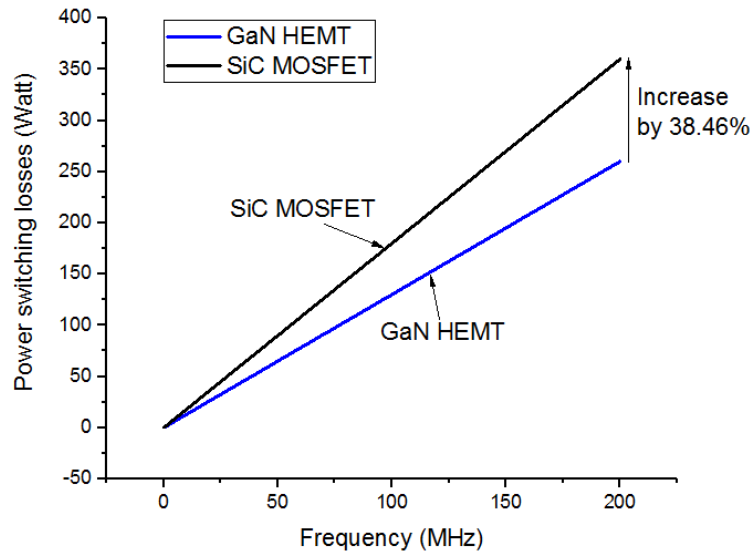


Fig. 2.18: Simulated power switching losses comparison between GaN HEMT (GS66508P), SiC MOSFET (SCT2120AF).

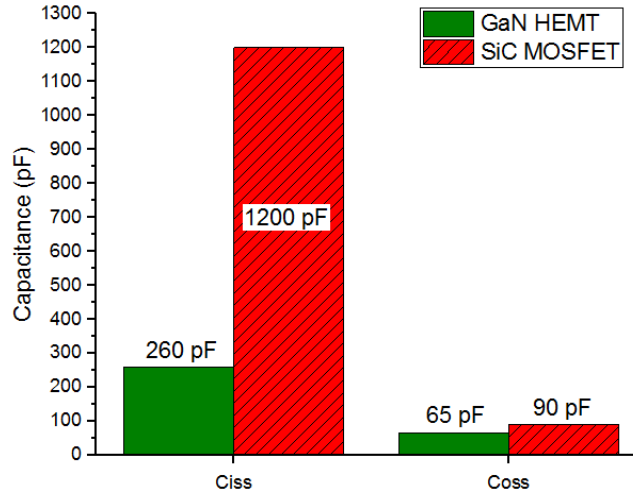


Fig. 2.19: Ciss and Coss capacitances comparison between GaN HEMT (GS66508P) and SiC MOSFET (SCT2120AF) [24-25].

In this section, we have demonstrated using SPICE simulation the high performances of the power GaN HMET in both static and dynamic characteristics compared to those of SiC MOSFET. Furthermore, we have found using SPICE simulation that the GaN has a lower switching time T_{ON} and T_{OFF} , which enables lower switching losses energy. Moreover, the GaN HEMT has a lower on-state resistance compared to the SiC MOSFET, which offers lower conduction losses energy for DC power converter applications. This makes the GaN HEMT very attractive for power switching applications market. Next, we will study the physical properties and the structure of the GaN HEMT power transistor.

2.4. Physical properties of the power GaN HEMT

To understand the origin of the GaN HEMT devices performances compared to those of SiC and Si MOSFET, we have studied in this suction the GaN material properties and compare it to the SiC and Si semiconductor materials. **Fig. 2.20 (a)** shows the on-resistance (R_{ON}) versus the BV of Si, 4H-SiC, 6H-SiC, and GaN material [30]. As shown in the limit chart, both the SiC and GaN materials have higher power performances in comparison with conventional Si material. The GaN enables low on-resistance and higher BV, which make it an attractive candidate for replacing Si power devices in power applications. **Fig. 2.20 (b)** shows the limits of the cutoff frequency and BV. As observed, the GaN combine both the high-speed and high-voltage performances compared to Si.

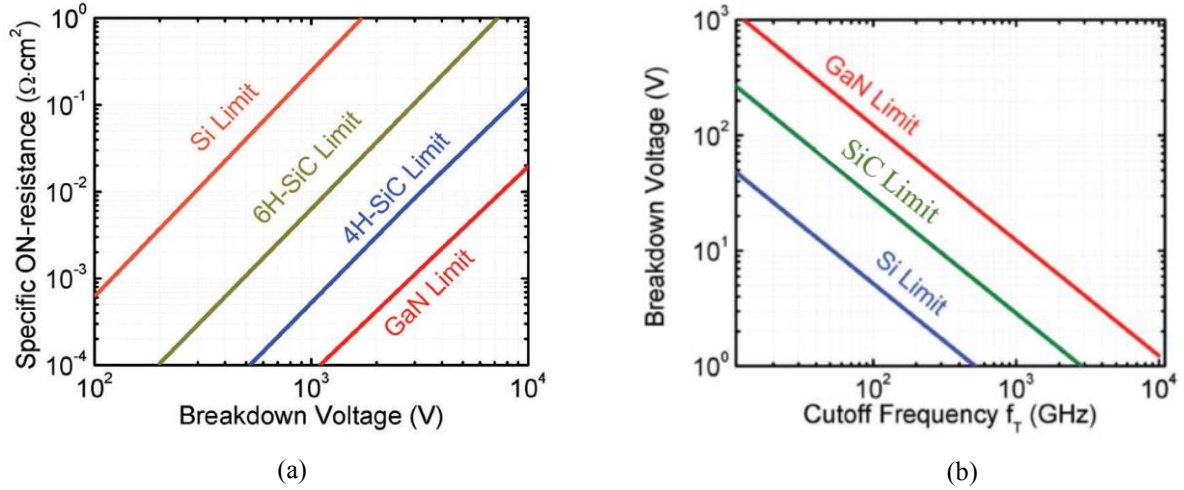


Fig. 2.20: Comparison of GaN power performances limits: (a) $R_{DS(ON)}$ versus BV (b) BV versus cutoff frequency [30].

Table 2.3 shows the five key electrical properties of three semiconductor materials Si, GaN and SiC contending for the power management market [31]. The superior physical properties of the GaN semiconductor offer a higher band gap, a higher electric breakdown field, a larger electron mobility, a lower permittivity and a good thermal conductivity, when compared to silicon (**Table 2.3**).

Table 2.3: Material properties of Si, GaN and SiC [31].

Parameter	Unit	Si	GaN	SiC
Band gap E_g	eV	1.12	3.39	3.26
Critical field E_{crit}	MV/cm	0.23	3.3	2.2
Electron mobility μ_n	cm ² /V.s	1400	1500	950
Permittivity ϵ_r		11.8	9	9.7
Thermal conductivity	W/cm.K	1.5	1.3	3.8

2.4.1. Physical properties of GaN

The GaN is a hexagonal crystalline structure named “wurtzite” (**Fig. 2.21**). This structure is very chemically stable [32], it is mechanically robust and can withstand high temperatures [33]. This crystal structure also gives GaN piezoelectric properties that lead to its ability to achieve very high conductivity compared with other semiconductor materials [34].

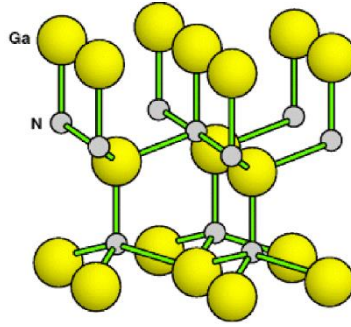


Fig. 2.21: Schematic of the wurzite GaN [32].

❖ **Spontaneous polarization:**

Since nitrogen has a higher electronegativity than gallium, Ga and N atoms have anionic (+) and cationic (-) characteristics, respectively, resulting in causing electric polarization. \vec{P}_1 , \vec{P}_2 , \vec{P}_3 and \vec{P}_4 are the internal polarization vectors of the GaN. As shown in Fig. 2.22, the noncoincident center of the positive charge and negative charge leads to spontaneous polarization [35]. And its polarization direction depends on its material growth direction.

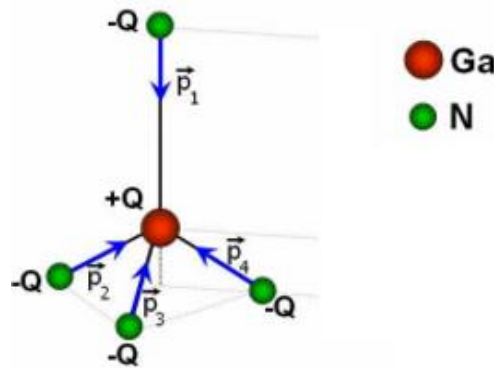


Fig. 2.22: Generation of the GaN spontaneous polarization [35].

❖ **Piezoelectric polarization:**

In addition to spontaneous polarization, piezoelectric effects were considered to be responsible for the sheet carrier densities in GaN devices. The mechanical stress inside the epitaxial layers with different lattice constants causes new type of polarization, which is referred to as piezoelectric polarization [36]. Fig. 2.23 explains how the piezoelectric polarization is caused in nitride semiconductors. As shown in the left figure, the resultant internal polarization vectors $P_1 + P_2 + P_3 + P_4$ become zero in a freestanding tetrahedral structure due to the crystal symmetry. However, when the crystal is deformed by the lattice mismatch, as shown in the right-hand side, the angle θ become widened when tensile stress is applied. Thus, the internal electric field becomes unbalanced to appear the piezoelectric field P_{PE} appears as $P_1 + P_2 + P_3 + P_4 = P_{PE}$.

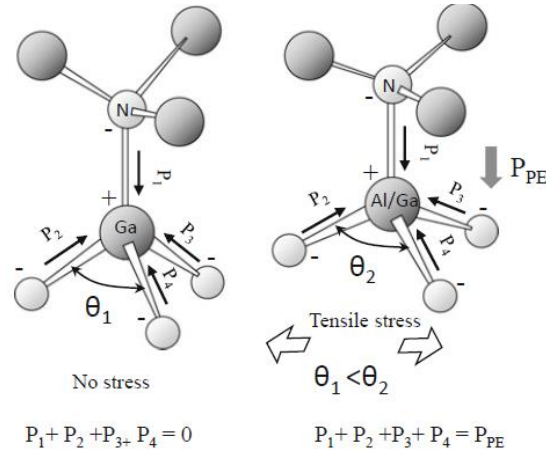


Fig. 2.23: Generation of the GaN piezoelectric polarization [36].

❖ **Heterojunction AlGaN/GaN:**

The GaN material combined both the spontaneous and piezoelectric polarizations, which lead to its ability to achieve very high conductivity compared to other semiconductor materials. The total polarization of the GaN material is given by (2.5) [36]:

$$P_{total} = P_{SP} + P_{PE} \tag{2.5}$$

Where P_{SA} is spontaneous polarization and P_{PE} is the piezoelectric polarization. **Fig. 2.24 (a)** shows the directions of the spontaneous and piezoelectric polarization for the AlGaN/GaN heterostructures. As observed, two-dimensional electron gas (2DEG) is created at the interface AlGaN/GaN. This is due to the strain-induced polarization at the interface between the two materials. A negative density of charge is created due to the gradient of polarization between the AlGaN and GaN layers defined by (2.6) [37]:

$$\sigma_{AlGaN/GaN} = \nabla P_{AlGaN/GaN} = \{P_{AlGaN}^{SP} + P_{AlGaN}^{PE}\} - \{P_{GaN}^{SP} + P_{GaN}^{PE}\} \tag{2.6}$$

As shown in the band diagram of the AlGaN/GaN heterostructure in **Fig. 2.24 (b)**. The strong piezoelectric and spontaneous polarization enables the confinement of the electrons in a deep and narrow quantum wells. This creates a two-dimensional electron gas (2DEG) with a high density of electrons at the interface AlGaN/GaN. The high concentration of electrons with very high mobility is the basis for the HEMT.

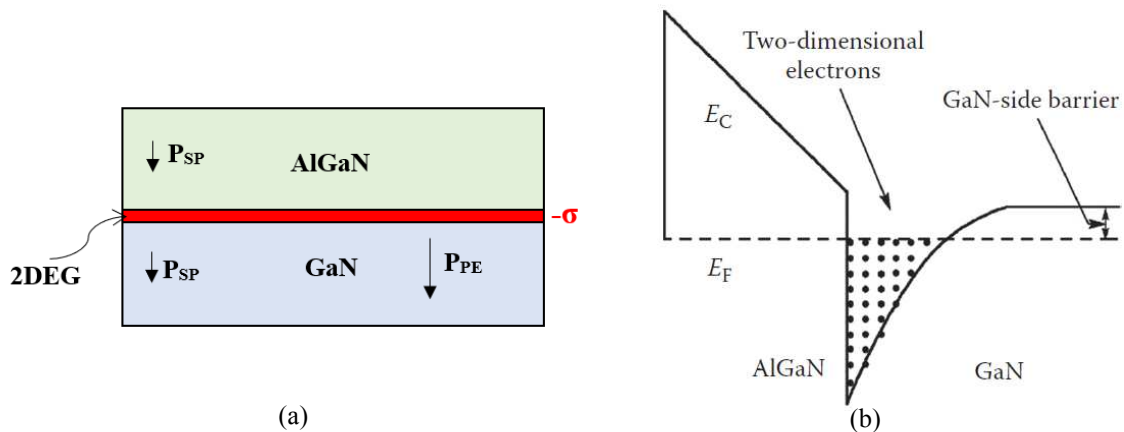


Fig. 2.24: AlGaN/GaN heterostructure: (a) cross section (b) Band diagram [37].

2.4.2. GaN HEMT normally-on structure

GaN HEMT has a heterojunction AlGaN/GaN and a GaN buffer layer deposited on a substrate and the source, gate, and drain contacts. **Fig. 2.25** shows a cross section of the GaN HEMT normally-on structure.

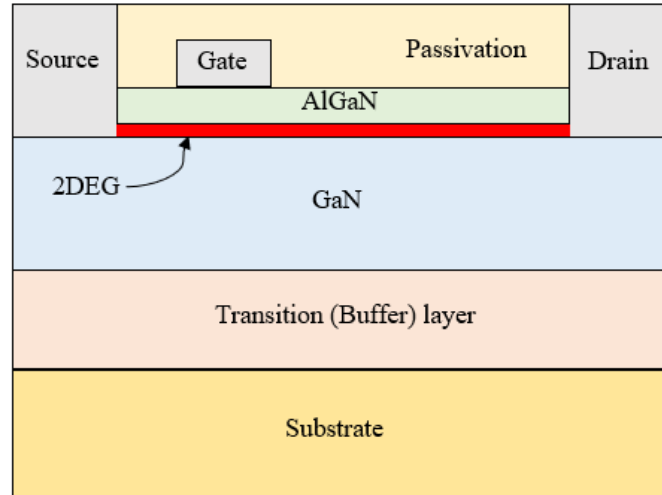


Fig. 2.25: Cross section of the GaN HEMT structure.

❖ Schottky contacts

The gate of the GaN HEMT is a Schottky contact. This gate metal with high Schottky barrier height enables a low gate leakage current in the GaN device. Ni/Au is the most widely used Schottky gate metal in GaN HEMTs due to its good thermal stability [38].

❖ Ohmic contacts

Both the drain and source of the GaN HEMT are ohmic contacts. The standard ohmic metal for GaN HEMTs is Ti/Al/Ni/Au [39]. The drain and source ohmic contacts constitute parasitic elements in the GaN HEMT, it is essential to minimize the contact resistance (R_c) in order to promote a good performance. To improve the ohmic contacts, several studies have focused on recessed ohmic contact. In [40], a recess etching by inductive coupled plasma etching (ICP) was performed before metal deposition and obtained a R_c of $0.3 \Omega\text{mm}$. Furthermore, in [41] a very low R_c of $0.26 \Omega\text{mm}$ was obtained due to direct contact between ohmic electrode and the 2DEG channel.

❖ Passivation

The passivation layer reduces the surface traps in the gate–drain access region. SiN is most commonly used for surface passivation in GaN HEMTs [42]. The effects of un-passivated devices are [43]: (1) Decrease of drain current capability; (2) Reduction of the 2DEG density (3) Activation of surface traps (4) Increase of leakage current.

❖ Heterojunction AlGaN/GaN

The principle feature of this structure is the AlGaN/GaN heterojunction. At the interface between these two layers, a layer of high-mobility electrons called “two-dimensional electron gas” (2DEG) forms as a result of spontaneous and piezoelectric polarizations of GaN material properties.

❖ Transition (Buffer) layer

The buffer layer serves to prevent injection of electrons into a substrate during high Voltage operation, thereby improving performance of the GaN transistor during high Voltage operation [44]. AlN is preferably used as a component of this transition layer [45].

❖ Substrate

The used substrate for the GaN HEMT can be Si, GaN or SiC. The criteria for substrate choice are: (1) low lattice-mismatch relative to the materials of the device layers; (2) good thermal conductivity; (3) low price per area.

Based on the literature [46-51], we have compared in **Table 2.4** the various substrate materials used for the GaN HEMTs, such as: Si, SiC and GaN substrates. As observed in **Table 2.4**, the GaN substrate still the best choice for the GaN HEMT due to its low lattice mismatch and its good thermal conductivity. However, the price of GaN substrate is very expensive compared to Si. The use of SiC as substrate for the GaN HEMT can improve its thermal performances due to its good thermal conductivity properties. Also, SiC substrate has a much smaller lattice mismatch (~3%), is in principle a more suitable substrate, but is available only in small diameters and is very expensive. At the present, the silicon is widely used as a substrate for GaN HEMT because of their commercial availability and excellent surface preparation. However, the use of Si produces high lattice-mismatch. This causes the occurrence of dislocations and cracking of the grown layer due to the lattice mismatch and the difference in the thermal expansion coefficient between GaN and the substrate. Increasing device leakage [48] and promoting metal diffusion along the dislocation sites [49].

Table 2.4: GaN HEMT substrate comparison: Si, SiC and GaN.

Substrate	Si	SiC	GaN
Advantage	❖ Low price (<100\$) [46].	❖ Good thermal conductivity [47].	❖ Low lattice mismatch [50]. ❖ Good thermal conductivity.
Challenge	<ul style="list-style-type: none"> • Poor thermal conductivity [47] • Large lattice mismatch (~16%) [51]. • Increased leakage current [48]. • Metal diffusion along dislocation sites [49]. 	<ul style="list-style-type: none"> • Existence of lattice mismatch (~3%) [51]. • High price (100\$ to 200\$) [46]. 	<ul style="list-style-type: none"> • High price (200\$) [46].

2.4.3. GaN HEMT normally-off

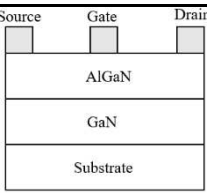
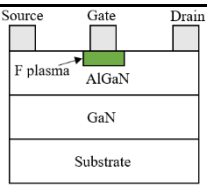
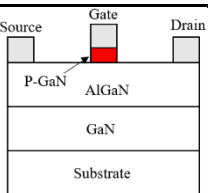
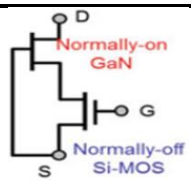






For safety reasons, the GaN HEMT used in power converters should be normally-off devices. In this way, if the gate driver fails and its output goes to zero, the HEMT switches to the off-state. If a simple AlGaN/GaN heterojunction is used to fabricate a HEMT, the device shows a normally-on behavior. Several solutions have been proposed throughout the years to achieve normally-off operation. In **Table 2.5**, we have compared based on the literature the various GaN HEMT technologies. As observed section 2.4.2, the normally-on devices have a simple structure and do not require complicated gate drive configuration. However, even when the gate bias is equal to zero volt, a current is formed in the 2DEG channel due to the spontaneous and piezoelectric polarization of the GaN material, which is not safe for power converter applications.

The implantation of fluorine ions under the gate results in normally-off behavior. However, this technic suffers from both the instability of the doped F-ions with high temperature [52] and the instability of V_{TH} over the time [53].

Cascode structure is a hybrid technology between Si MOSFET and GaN HEMT transistors, which connect a low-voltage Si MOSFET to the gate of a high-voltage GaN HEMT. This hybrid configuration, demonstrates a normally-off behavior. Moreover, the structure is compatible with existing Si gate drivers [54].

The use of a p-GaN or p-AlGaN layer on top of the AlGaN/GaN heterojunction enables a positive shift of the V_{TH} voltage ranging from 1 to 3 V with the applied gate voltage larger than 5 V.

Table 2.5: Comparison of GaN HEMT structures.

	Normally-on	F doped gate	P-type gate	Cascode
Structure				
Advantage	<ul style="list-style-type: none"> ➤ Simple structure ➤ Simple process (see section II.4.2.)	<ul style="list-style-type: none"> ➤ Positive V_{TH}. ➤ Normally-off. ➤ Lower gate leakage current. 	<ul style="list-style-type: none"> ➤ High positive V_{th} ($V_{th}>1$). ➤ Normally-off. ➤ Stable V_{TH}. ➤ Lower gate leakage current. 	<ul style="list-style-type: none"> ➤ High positive V_{TH}. ➤ Normally-off. ➤ Gate driver compatible with that of Si devices. ➤ Good reliability.
Challenge	Complex gate drive configuration. Unsafe for switching applications: current flow at $V_{GS}=0V$ [55].	Instability of doped F-ions with high temperature [52]. Instability of V_{th} over the time [53].		Limited high speed [54]. High fabrication cost.
Manufacturer	Cree [56]  MACOM [57] 	Academic project [58-59]	GaN system [60]  Panasonic [61]  EPC 	Transform [62] 

The p-GaN GaN HEMT normally-off approach is finding wide consensus within the scientific and industrial community. Nowadays, the p-GaN technology is the most attractive in the GaN HEMT market [63]. For this reason, it is important to investigate the main issues related to the stability of these devices. In the next section, we have presented the main degradation mechanisms that take place in GaN HEMT with p-GaN gate for power switching applications.

2.5. Aging of the GaN HEMT power transistors

To understand the various degradations of power GaN HEMT under switching conditions, we have performed a failure mode and effects analysis (FMEA). **Table 2.6** summarizes the most critical degradation processes that are induced by off-state, on state and semi-on state stress, along with the related failure modes. As shown in this table, the most critical failure mode is the increase of the on-state resistance ($R_{DS(On)}$) due to the trapping of hot electrons under the gate [64] and the generation of lattice defects [65]. This may induce an elevation in the device temperature due to the increase of power conduction losses generated by the on-state resistance $R_{DS(On)}$. Another critical failure mode of the GaN HEMT is the negative shift of the threshold voltage V_{TH} . This is caused by the trapping of electrons in the gate area [66]. This may induce a safety critical failure in the gate driving circuit of the power converter with GaN HEMT. The time-dependent failure mode is another issue facing the GaN HEMT power transistors. This degradation is due to the generation of short circuit paths in the GaN HEMT structure. This may increase the leakage current in the power converter circuit with GaN HEMT.

Table 2.6: The most critical failure mode and effects analysis of the GaN HEMT.

Component	Failure mode	Failure cause	Failure effect
GaN HEMT power transistor	Increase in $R_{DS(On)}$	-Trapping of hot electrons under the gate. and at the gate edge [64]. -Generation of lattice defects [65].	- Elevation in the device temperature. - High conduction power losses.
	V_{TH} shift	- Trapping/detrapping of electrons in the gate area [66].	-Normally-on behavior.
	Decrease in g_m	-Buffer trapping [67]. -Surface trapping [68].	- RF performance degradation. - Current collapse.
	Time-dependent Degradation	- Generation of source-drain current paths [69]. - Short circuits between gate and channel [70].	Increase of I_{DSS} leakage current until the vertical (drain to substrate) breakdown.
	Time-dependent gate breakdown	- Generation of defects/leakage paths in the p-GaN/AlGaIn gate stack [71].	Increase of I_{GSS} leakage current until the gate breakdown.

In the literature including the GPM laboratory, various work were performed to evaluate the reliability of the GaN power devices, including: short-circuit, HTRB, HTGB and switching stresses [72].

2.5.1. Short circuit stress

Short-circuit stresses enable to evaluate the robustness of power GaN HEMT transistors under high drain current pulses with short duration. In [73], a repetitive and non-destructive short-circuit aging test were applied on a 600 V GaN Gate Injection Transistor (GIT). The evolutions of C-V and I-V characteristics during the repetitive short-circuit tests show significant degradations before and after the test. During this test the DUT is maintained at on-state during a 4 ms short-circuit phase with the drain voltage V_{DS} equal to 35 V. After the aging test, the saturate region of $I_{DS(sat)}$ decreases obviously, which is due to the increase of the on-state resistance $R_{DS(ON)}$. Also, the C_{GS} capacitance was increased due to the charge trapping and de-trapping between the gate-source [74].

2.5.2. Static stresses: HTGB, HTRB

High Temperature Gate Bias (HTGB) and High Temperature Reverse Bias (HTRB) tests are JEDEC standards qualification tests for electronic devices [75]. During the aging, the Devices Under Test were placed in an environmental chamber which provided a constant temperature of 150 °C and in the meantime, they were bias stressed by applying a gate-source DC voltage with drain shorted to source for HTGB stress or by applying a drain-source DC voltage with gate shorted to source for HTRB stress [76].

In [72], HTRB stress experiments are performed on a power GaN HEMT to investigate the degradation phenomena. Several degradation characteristics of DC parameters such as the reduction of saturated drain current, the increase of gate leakage current and on-resistance and the shift of threshold voltage are identified. The degradation mechanism is ascribed to the trapping of electrons in the region under the gate and the access region of gate to drain. These mechanisms may significantly limit the performance of power GaN HEMTs when they are operated at high drain voltage and frequency levels [77].

In [78], the threshold voltage instability during high temperature gate bias (HTGB) test has been investigated for a power GaN HEMT. The negative threshold voltage shift, occurring at large positive gate biases, has been attributed to holes generated by impact ionization in the high-field depleted p-GaN region and accelerated toward the AlGaIn layer [79]. Authors in [80] have demonstrated the suppression of the negative V_{TH} shift by optimizing the etching and passivation of the p-GaN layer.

2.5.3. Switching stress

In [81], a switching aging stress was performed under the Safe Operating Area (SOA) of a 600 V / 30 A power GaN HEMT. The used switching bench offers a low energy consumption because no load is used. Also, it places a similar electrical waveform on DUT_M , which could exist in a large class of power management products such as DC-DC power converters. A 1000 h aging campaign has shown degradation of the DUT electrical characteristics, such as increase of $R_{DS(ON)}$, I_{DSS} and I_{GSS} . As presented in [82], these degradations are related to a self-heating activated mechanism.

In chapter 5, we have studied the aging of power GaN HEMT under operational switching conditions. We have extended our investigation of the aging of GaN HEMT not only in static characteristics but also in the dynamic aspect. For this, we have implemented both C-V and S

parameters measurements in the GPM laboratory. Also, in this work, we have studied the impact of aging the DUT in power converters application by a modeling approach.

2.6. GaN HEMT power losses modeling

Significant improvements in efficiency of power converters can be achieved due to the superior switching properties of GaN HEMT. The authors in [83] studied the efficiency of a T-type inverter with Si IGBT, SiC MOSFET and GaN HEMT at 600 V blocking voltage range.

Fig. 2.26 (a) shows the schematic of the T-Type converter and **Fig. 2.26 (b)** shows the efficiency analysis at 32 kHz for Si IGBT, SiC MOSFET and GaN HEMT. At 32 kHz, GaN HEMT brings up to 1.6 % efficiency gain and up to 0.75 % when using SiC MOSFET. This is due to the poor switching performance of Si IGBT.

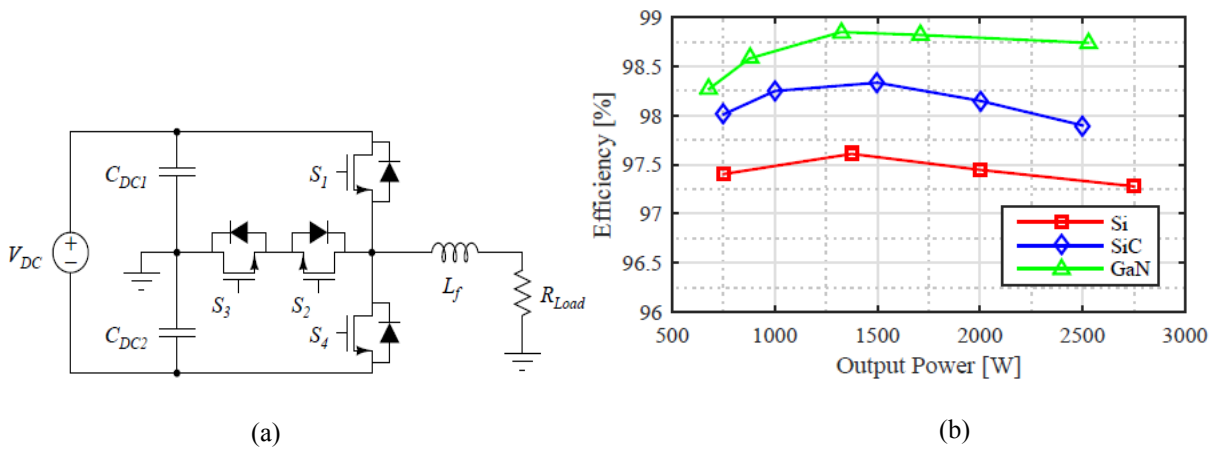


Fig. 2.26: Power converter efficiency comparison between Si IGBTs, SiC MOSFETs and GaN HEMTs: (a) T-type inverter topology (b) Efficiency comparison at 32 kHz [83].

The high efficiency of power converters with GaN HEMT are due to the GaN advantage technology over silicon devices. As shown in **Fig. 2.27**, the gate capacitance at the input of the GaN HEMT is about four times lower than for a comparable silicon-based solution [84], yielding a higher switching rate and higher efficiency as a result of reduced gate drive losses [85].

Another important benefit is low-output capacitance, which results in higher switching frequencies and helps to reduce switching losses [86]. Additionally, $R_{DS(on)}$ is about two times lower than for Si devices, resulting in lower conduction losses [87]. Finally, the use of GaN transistors enable to eliminate the integrated “body” diode. In consequence, achieving higher power efficiency by eliminating the reverse recovery loss [88].

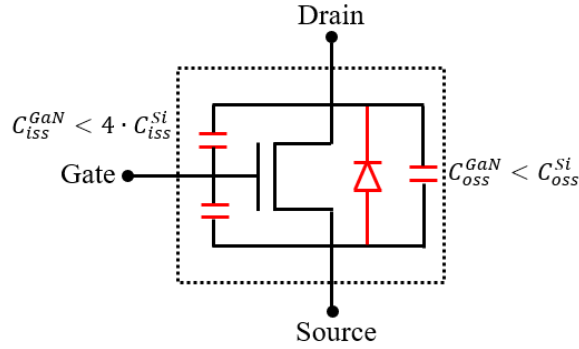


Fig. 2.27: GaN HEMT package and comparison to Si MOSFET parasitic elements [84].

2.6.1. Power losses in DC power converter

In a switching mode power converter, such as Boost DC/DC converter topology shown in Fig. 2.28 (a), the transistor is continuously switched from the off-state to the on-state and vice versa. When the transistor is in the off-state, a high voltage (up to 650 V) is applied between drain and substrate, drain and source, and between drain and gate. On the other hand, in the on-state, the gate is positively biased at voltages higher than 5-6 V (in case of normally-off transistors) and a high current (up to 30 A) flow between the drain and source. Finally, when the transistor switches from the off-state to the on-state, it crosses a semi-on condition, in which the voltage and current on the drain may be simultaneously high (grey areas in Fig. 2.28 (b)).

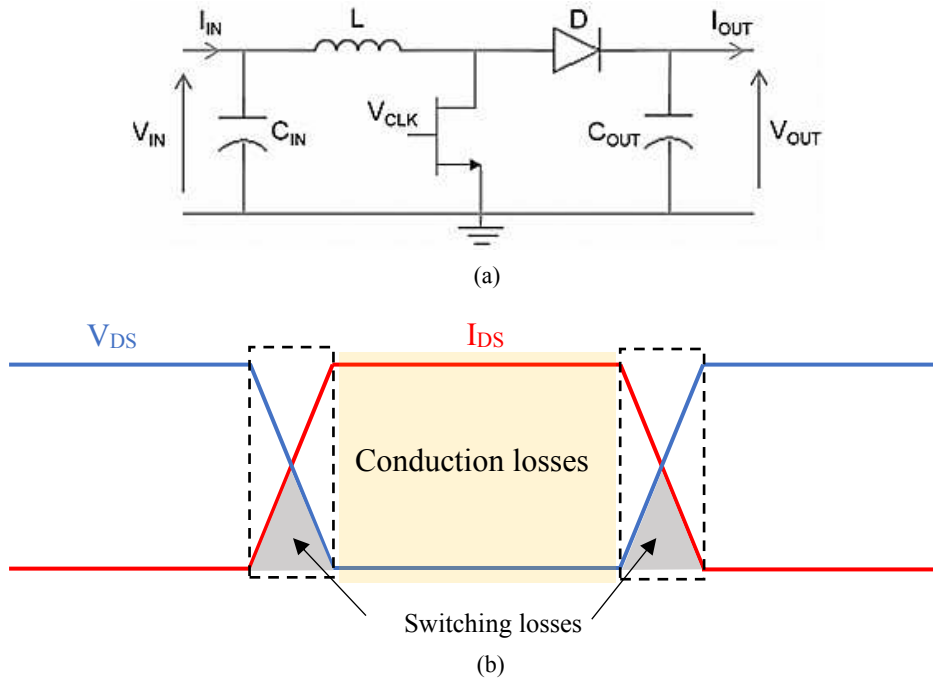


Fig. 2.28: Boost DC/DC converter: (a) Circuit schematic (b) representation of the different operating regimes of the transistor in a boost converter.

This Boost DC/DC switching application will be used in chapter 5 to evaluate the effect of aging of the GaN HEMT power transistors on the power converter efficiency. In this topology, the conduction power losses are defined in [89] by:

- Losses in the inductor: $P_L = R_L \cdot I_{IN}^2$ (2.7)

- Losses in the transistor: $P_T = R_{DS(on)} \cdot I_{IN}^2 \cdot D$ (2.8)

- Losses in the diode: $P_D = (R_D \cdot I_{IN}^2 + V_f \cdot I_{IN}) \cdot (1 - D)$ (2.9)

- Duty cycle: $D = \frac{T_{ON}}{T}$ (2.10)

The switching power losses are defined by:

- Turn-on switching losses: $P_r = 0.5 \cdot V_{OUT} \cdot I_{IN} \cdot \frac{t_r}{T}$ (2.11)

- Turn-off switching losses: $P_f = 0.5 \cdot V_{OUT} \cdot I_{IN} \cdot \frac{t_f}{T}$ (2.12)

Where R_L is the dc inductor resistance, $R_{DS(on)}$ is the transistor on-resistance, R_D is the diode series resistance, D is the duty-cycle, and V_F is the diode forward voltage. t_f and t_r are the fall and rise times of the transistor drain current, respectively, while T is the period of the control signal and T_{ON} is the on-state period. The approximate expression for the converter efficiency is given in [89] by:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_L + P_D + P_T + P_f + P_r} \quad (2.13)$$

where P_{OUT} is the output power of the converter.

2.6.2. Estimation of GaN power losses

The estimation of power losses with high convergence to measurements is necessary to design efficient power converters using GaN transistors. The authors in [90] have proposed an estimation of power losses based on a look-up tables of energy losses to estimate the switching losses of the IGBTs. Also, the authors in [91] have estimated and compared the power switching energy of GaN HEMTs to equivalent Si devices such as IGBT and MOSFETs. In chapter 3, we estimate both the static and dynamic power losses of GaN HEMTs, which are most significant in DC-DC power converter with GaN HEMT [92].

The distribution of power losses in the Boost DC/DC converter of **Fig. 2.28 (a)** with GaN HEMT transistors for $V_{IN} = 16$ V, $V_{OUT} = 34$ V and $P_{OUT} = 15$ W are shown in **Fig. 2.29** [89]. As observed, the majority of losses in the power converter are due to both the conduction losses and switching losses of the GaN HEMT.

In order to study the effect of GaN power losses on the efficiency of power converter, an efficient approach for the estimation of losses is necessary. Furthermore, the estimation of the GaN HEMT power losses offers to the power converter designers the possibility to estimate the power losses of GaN HEMT with high accuracy without the use of complex switching bench, which reduces both the time to market and cost.

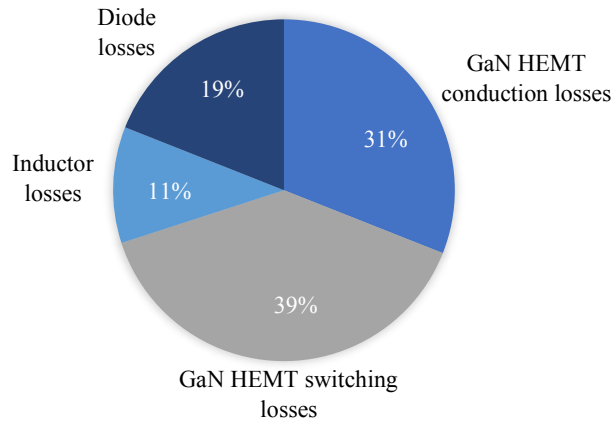


Fig. 2.29: Distribution of power losses in Boost DC/DC converter with $V_{IN} = 16$ V; $V_{OUT} = 34$ V and $P_{OUT} = 15$ W [89].

The power losses of the GaN HEMT can be estimated using SPICE simulation approach. This approach consists of building the compact model of the DUT in a SPICE simulator software, such as: LTspice, Orcad, and ADS. The SPICE model of the GaN HEMT is given in [93] and described in **Fig. 2.30**, where R_D , R_G and R_S are the parasitic resistances at the gate, drain and source, respectively. The current source i_D determines the current from drain to source, which is a function of V_{GS} and V_{DS} . C_{GS} , C_{GD} and C_{DS} are the capacitances between the gate and source, the gate and drain and the drain and source, respectively. These capacitances are nonlinear functions of V_{GS} , V_{GD} and V_{DS} .

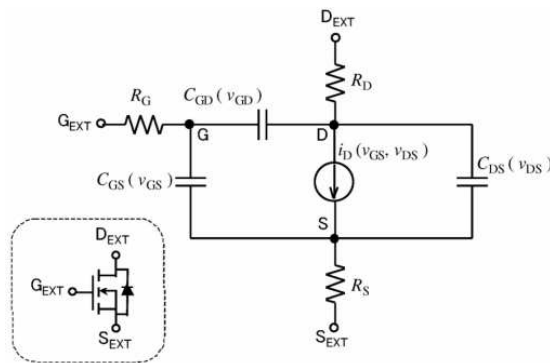


Fig. 2.30: GaN HEMT SPICE model [93].

SPICE models of the GaN-based HEMT is constructed on the basis of experimental data. Then, the static and dynamic characteristics are obtained by simulation for any power conversion switching application.

Another model that enables the estimation of the GaN HEMT power losses by simulation is the compact physical model [94]. This model includes both the current–voltage (I–V) and the charge–voltage (Q–V) formulations. **Fig. 2.31** shows the topology of the complete GaN HEMT compact model. Conduction current is represented by I_{con} between the drain and source electrodes. The capacitances are integrated into charges and used to calculate the displacement currents. Reverse conduction between gate and source is represented by I_{rev} . Forward conduction from gate to source is represented by I_{for} . The current generator I_{tun} between drain and gate represents current leakage. Finally, the current generator I_{chbd} between drain and source represents channel breakdown.

Table 2.7: Comparison of available GaN SPICE models [97].

SPICE Model	Number of parameters	Electrothermal model	Origin device context
Curtice	59	No	GaAs MESFET
Motorola Electrothermal (MET)	62	Yes	GaN HEMT
Angelov	90	Yes	GaN HEMT

2.7. Conclusion

This chapter presents the state of art of GaN HEMT power transistors in power converter applications. Firstly, it has been reported that the GaN HEMT devices satisfy the requirement of the power converter market for a high operating voltage, high operating current, high power density, high switching frequency, and strong reliability, which makes the GaN technology an attractive candidate for replacing Si power devices in power applications. However, SiC technology has always been a hot candidate for GaN in high power and high temperature applications. However, the high frequency applications are the main market of GaN and this huge market is pushing the GaN to dominate both the Si and SiC markets. Furthermore, the increased demand of efficient power conversion systems, makes the GaN devices more attractive for automotive and renewable energy industry. Next, the physical properties of the GaN semiconductor are presented and compared with those of Si and SiC. It is found that the GaN combine both the high-speed and high-voltage performances. This is followed by a description of the working principle of the AlGaIn/GaN HEMT. Moreover, a comparison of the various GaN HEMT normally-off technologies are reported. Next, the various technics for aging the GaN HEMT transistors are presented. Furthermore, the major degradations of power GaN HEMT under switching conditions are summarized. Finally, the SPICE modeling approach enables the estimation of the GaN HEMT power losses with high accuracy. The SPICE simulation tool can be used for studying the impact of the aging the GaN HEMT on the efficiency of power converter applications. In the next chapter, an experimental methodology for the estimation of the GaN HEMT power losses based on experimental static and dynamic measurements using SPICE simulation approach will be presented.

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Chapter 3: GaN HEMT power losses estimation for switching applications

3.1. Introduction

In the previous chapter, the importance of the estimation the GaN HEMT power losses for power converter application has been shown. As discussed, various SPICE models have been proposed in the literature for estimating the GaN HEMT power losses. However, these models do not take into consideration both the static and dynamic behavior of the GaN HEMT. In this chapter, a complete methodology for the estimation of the GaN HEMT power losses based on experimental measurement is proposed and described.

First, the pulsed I-V experimental setup is presented. The temperature dependency of the DUT static characteristics are discussed at various temperatures: from 5 °C to 115 °C by a step of 10 °C. The conduction power losses of the DUT is estimated based on a SPICE simulation approach for switching circuit applications. The evolution of the conduction losses is modelled as a function of both the junction temperature and output current.

Additionally, the C-V experimental setup is implemented in order to take into account the switching losses in the designed SPICE model of the GaN HEMT. The evolution of the switching losses is modelled as a function of the output current. The temperature dependence of the C-V characteristics is investigated using a Peltier heater plate in the temperature range from 5 °C to 115 °C. Moreover, the frequency dependency of the C-V measurements is carried out using HP 4192A impedance analyzer in the frequency range from 100 kHz to 10 MHz.

Next, the low current experimental bench is carried out for measuring the gate leakage current (I_{GSS}) of the GaN HEMT. The I_{GSS} current is studied at various temperatures and voltages. The gate power losses of the GaN HEMT has been modelled by measuring experimentally the gate leakage current of the DUT.

As a result, we have built an accurate power losses model of the GaN HEMT based on experimental measurements, which include the major power losses in power converter applications. This approach offers to the power converter designers the possibility to estimate the power losses of GaN HEMT with high accuracy without the use of complex switching bench, which reduces both the time to market and cost. Finally, using the extracted power losses model of the GaN HEMT, we have estimated the efficiency of a 30 V / 200 V DC-DC converter stage with GaN HEMT for a solar energy application.

3.2. Static characterization of GaN HEMT

In this section, the conduction power losses of the GaN HEMT have been estimated by modelling the static I-V characteristics of the GaN HEMT. First, the I-V experimental setup has been presented. The estimation of the conduction power losses is performed by a SPICE simulation using a non-segmented Electro-thermal model. Then, the temperature dependency of the I-V characteristic is studied from a low temperature (5°C) to a high temperature (105°C) using a Peltier heater plate. Furthermore, the modelled device is verified in a real switching

application using a developed efficient switching bench. Finally, the evolution of the GaN HEMT power losses in switching applications is modelled as a function of the temperature and output current.

3.2.1. Pulsed I-V Experiment setup

The Current-Voltage (I-V) characterization has been performed by using AMCAD pulsed I-V system [1]. The system consists of two independently operating mode: Pulsed or DC. **Fig. 3.1** shows the I-V pulsed bench with associated instruments.

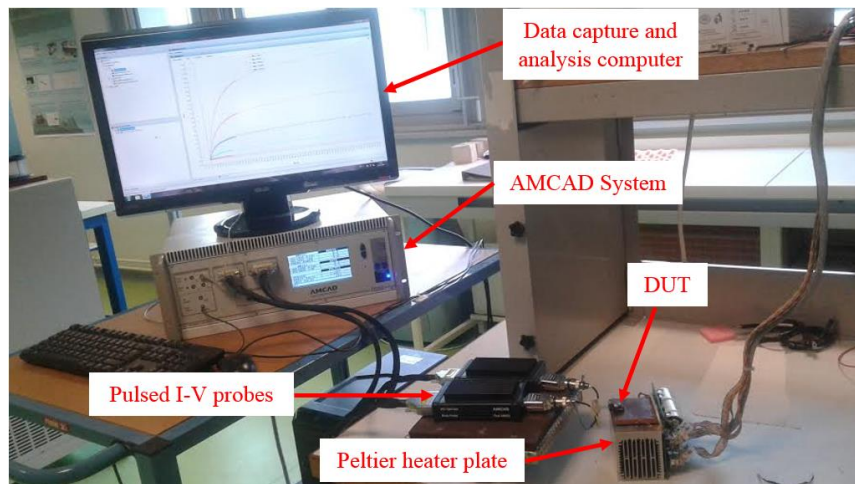


Fig. 3.1: I-V pulsed bench with associated instruments.

The I-V pulsed bench is composed of:

- AMCAD System: is the main unit;
- Data capture and analysis computer: enable the control and configuration of the AMCAD System using the IVCAD interface. Also, they offer the treatment and analysis of the measured data using integrated tools, such as: visualization of measurement, pre-treatment of data and modeling;
- Peltier heater plate: provides a uniform distribution of temperature on bottom surface of the DUT. The temperature range is between 5 °C and 150 °C.

Fig. 3.2 shows the I-V pulse chronogram. The I-V measurement is performed during T_M period (measurement window). The drain pulse is larger than the gate pulse because the drain response time is lower than the gate response time. The drain current is measured near to the end of the flat top of the transient pulse.

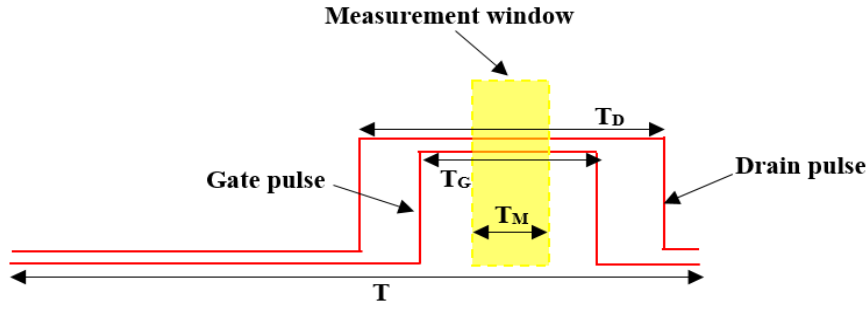


Fig. 3.2: I-V pulse chronogram.

Table 3.1 shows the used configuration of the I-V pulse timing. The measurement frequency is equal to 100 Hz. The measurement window time is equal to 0.4 μ s.

Table 3.1: I-V pulse timing.

	Gate pulse (T_G)	Drain pulse (T_D)	Measurement window (T_M)	Pulse period (T)
Time	2.5 μ s	4.0 μ s	0.4 μ s	100 ms

Pulsed I-V measurements are the most relevant characterization technique compared to conventional DC measurements [2], since they enable the elimination of both the effects of self-heating and traps during the measurement. The pulsed I-V measurements allow output characteristic (I_{DS} - V_{DS}), transfer characterization (I_{DS} - V_{GS}), characterization of thermal phenomena and trapping. The main characteristics of the AMCAD bench for pulsed I-V measurements are:

- Measurement probes 1k V / 30 A.
- Pulses less than 200 ns.
- All measurements are easy to perform, store and view with IVCAD software [3].
- Integrated measurement units provide high-bandwidth, high voltage accuracy and current measurements simultaneously: 50 MHz bandwidth, 16-bit resolution, 0.1% high accuracy, and fast acquisition.

The principle of pulsed I-V measurements is illustrated in Fig. 3.3 It consists of the I-V characteristics measured under isothermal conditions at a given polarization point, defined by its quiescent voltages V_{dsq} and V_{gsq} . To characterize the I-V network at given polarization points, both the gate and drain control voltages are pulsed from these polarization points to new instantaneous values named V_{gsi} , V_{dsi} , I_{gsi} and I_{dsi} .

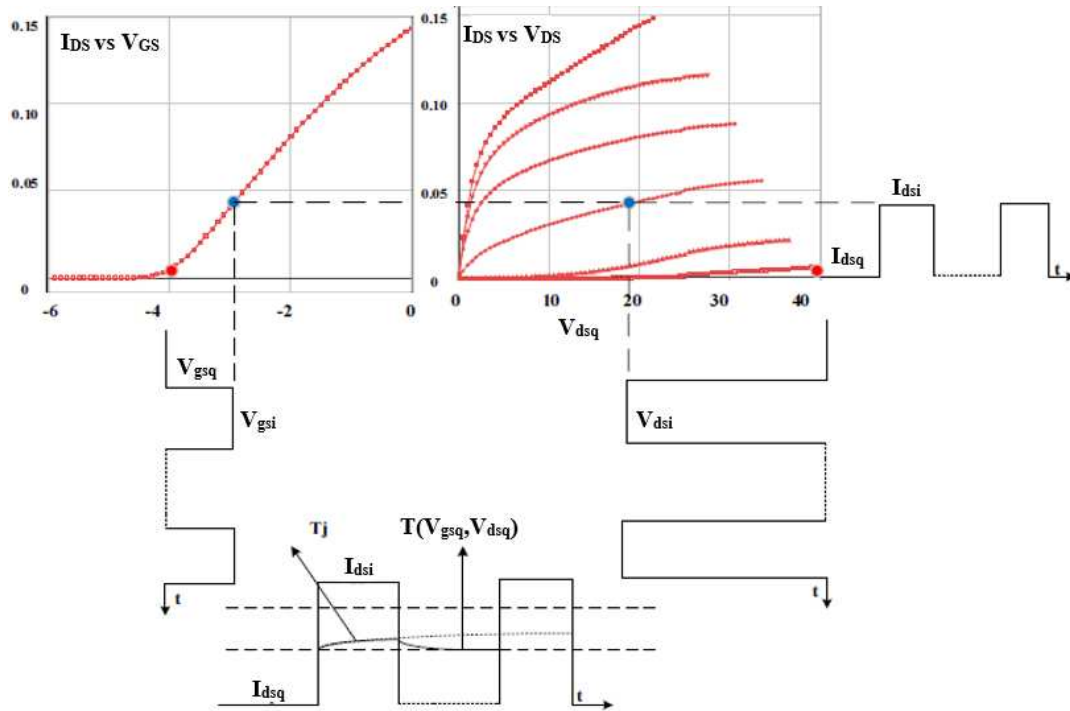


Fig. 3.3: Principle of pulsed I-V measurements.

3.2.2. Temperature dependency of GaN HEMT static characteristics

The investigation of the temperature dependency of GaN HEMT power transistors is vital to the use in power converter applications. Such an investigation is important particularly to understand the cause of deterioration of their electrical performances at elevated temperatures [4]. In this section, the I-V characteristics of a GaN HEMT power transistor at operating temperatures are studied experimentally. Moreover, the physics underlying various high-temperature operations of the I-V characteristics is discussed.

The DUT is a GS66508P from GaN Systems [5]. It is a p-type gate normally-off AlGaIn/GaN power transistor which operates in the range of 650V/30A. Fig. 3.4 shows both a bottom and top views of the used GaN transistor package. The device package allows to study the temperature dependency of the GaN HEMT characteristics from low temperature (5°C) to high temperature (105°C). Fig. 3.5 shows the p-AlGaIn gate formed over the undoped AlGaIn/GaN heterostructure [6]. The p-AlGaIn lifts up the potential at the channel, which enables normally-off operation.

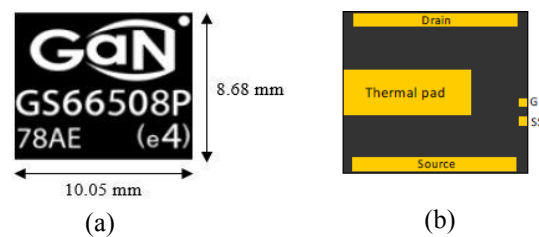


Fig. 3.4: GS66508P package [7]: (a) Top view; (b) bottom view.

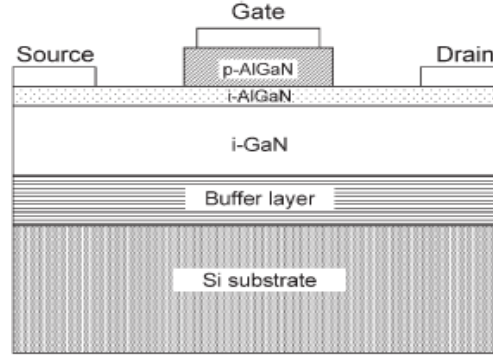


Fig. 3.5: Schematic illustration of the tested GaN HEMT power transistor structure [6].

As mentioned before, the static characterization is performed using AMCAD pulsed I-V system. The pulses setting is fixed at a pulse frequency of 100 Hz with a gate pulse duty cycle of 0.04%. A pulse width of 4 μ s is short enough to ensure iso-thermal measurement of pulsed I-V GaN HEMT characteristics. The used I-V pulsed probes have a high measurement accuracy, which is equal to ± 100 mA.

The used GaN HEMT is characterized at various temperatures ranging from 5 $^{\circ}$ C to 105 $^{\circ}$ C in order to study the effect of temperature on GaN power transistors. The temperature is fixed by a Peltier heater plate.

The measured output characteristic curves for a gate-to-source voltage (V_{GS}) equals to 6V under operating temperatures equal to 5 $^{\circ}$ C, 25 $^{\circ}$ C, 75 $^{\circ}$ C and 105 $^{\circ}$ C are shown in **Fig. 3.6 (a)**. As observed, the drain current I_D is modulated by the voltage V_{GS} . The transfer characteristic curves are obtained for a drain-source voltage (V_{DS}) equals to 2V and for various temperatures equal to 5 $^{\circ}$ C, 25 $^{\circ}$ C, 75 $^{\circ}$ C and 105 $^{\circ}$ C see **Fig. 3.6 (b)**. The tested device has the advantage of safe normally-off operation for temperature up to 105 $^{\circ}$ C.

According to the output characteristics (**Fig. 3.6 (a)**), the evolutions of the following electrical parameters are extracted: the on-state resistance ($R_{DS(ON)}$), the threshold voltage (V_{TH}). From the transfer characteristic (**Fig. 3.6 (b)**), the evolution of the transconductance g_m versus temperature is determined.

3.2.2.1. On-state resistance $R_{DS(ON)}$

The $R_{DS(ON)}$ is defined as the inverse of the slope of output characteristics in the linear region and is calculated at $V_{GS} = 6$ V by [8]:

$$R_{DS(ON)} = \left. \frac{\Delta I_D}{\Delta V_{DS}} \right|_{V_{GS}=6V, V_{DS} \rightarrow 0V}^{-1} \quad (3.1)$$

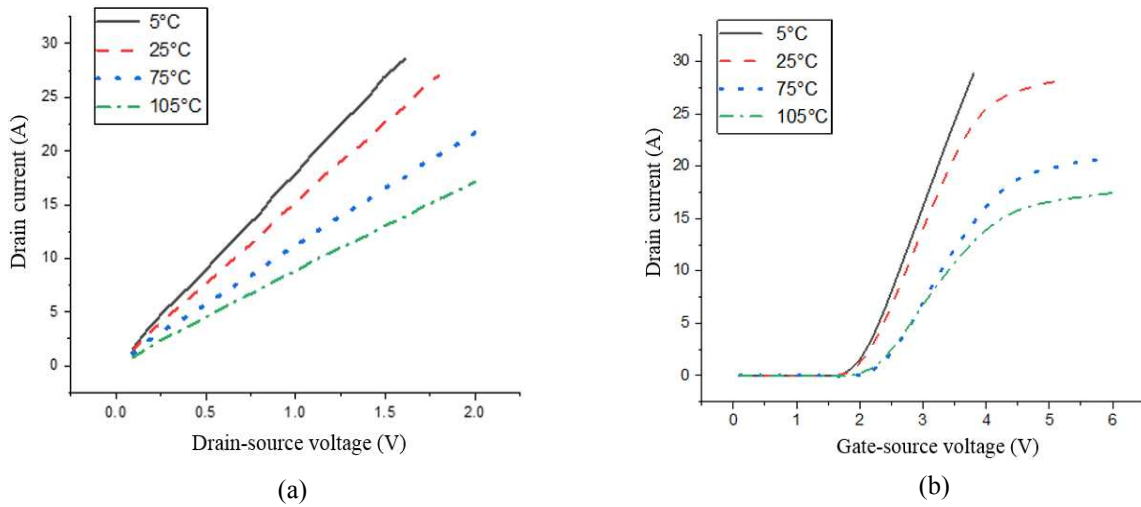


Fig. 3.6: Measured (a) Output characteristics at $V_{GS} = 6V$; (b) Transfer characteristics at $V_{DS} = 2V$ of GaN HEMT for various temperatures: 5 °C, 25 °C, 75 °C and 105 °C.

The measurement conditions of normalized $R_{DS(ON)}$ are: $V_{GS} = 6V$ and varying temperature from 5 °C to 105 °C. **Fig. 3.7** shows the variation of the normalized $R_{DS(ON)}$ versus temperature. An increasing of 180 % in on-state resistance at 105 °C can be observed compared to its value at 5 °C.

The temperature dependency of $R_{DS(ON)}$ is due to the impact of temperature on the channel between the source and gate contacts [9]. In fact, if the device temperature is raised, the low-field electron mobility in the channel is decreased [7], and a proportional increase of the channel resistance related to the drain-source resistance (R_{DS}) can be expected. This result is also confirmed in reference [10] which has suggested to use GaN HEMT transistors with higher 2-D electron gas (2DEG) channel density for enhanced performances.

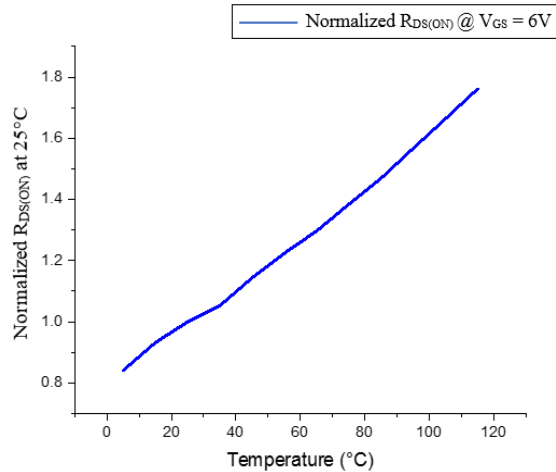


Fig. 3.7: Normalized $R_{DS(ON)}$ as a function of temperature at $V_{GS} = 6V$.

3.2.2.2 Threshold voltage (V_{TH})

The V_{TH} is extracted using Extrapolation in the Linear Region (ELR) method [11]. The temperature dependency of the extracted threshold voltage is given in **Fig. 3.8 (a)**. The threshold voltage of GaN HEMT at 105 °C decreases about 12 % compared to their values at 5 °C.

The dependency of V_{TH} on temperature is mainly due to holes injected from the metal to the p-GaN layer [12]. The injected holes are accumulated at the p-GaN/AlGaN interface. This leads to a negative shift in threshold voltage, which can also be observed in [12]. Recent studies [13] show that using hydrogen plasma treatment instead of etching technology may compensate holes in the p-GaN layer above the two-dimensional electron gas (2DEG) channel to release electrons in the 2DEG channel and form high resistivity area to reduce leakage current and increase threshold voltage stability.

3.2.2.3 Transconductance (g_m)

The g_m quantifies the drain current variation with a gate-source voltage variation while keeping the drain-source voltage constant. The transconductance g_m is defined as the maximum first derivative of the transfer characteristic in the saturation region and is calculated at $V_{DS} = 7\text{ V}$ using the following equation while V_{DS} is the bias voltage [8]:

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{DS}=7V} \quad (3.2)$$

Fig. 3.8 (b) shows the variations of the transconductance g_m as a function of temperature. The transconductance g_m at $105\text{ }^\circ\text{C}$ decreases about 58.38 % compared to their values at $5\text{ }^\circ\text{C}$. The decreasing of g_m with the increase of temperature is mainly due to the decrease of both the electron mobility in the channel and the electron velocity [14]. The decrease of the transconductance when increasing temperature is observed in [15] which has confirmed that the channel mobility decreases with the increase of temperature [16].

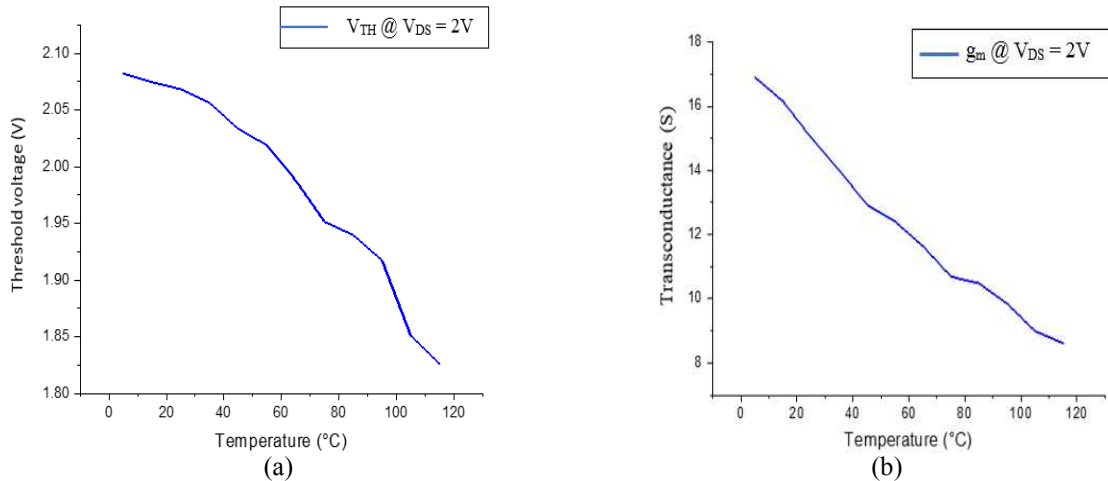


Fig. 3.8: (a) Threshold voltage; (b) Transconductance as a function of temperature at $V_{DS} = 2\text{ V}$.

3.2.3. Modeling GaN HEMTs Power Transistors

3.2.3.1. Modeling methodology

The proposed methodology for modeling power GaN HEMTs is shown in **Fig. 3.9**, which is composed of seven steps.

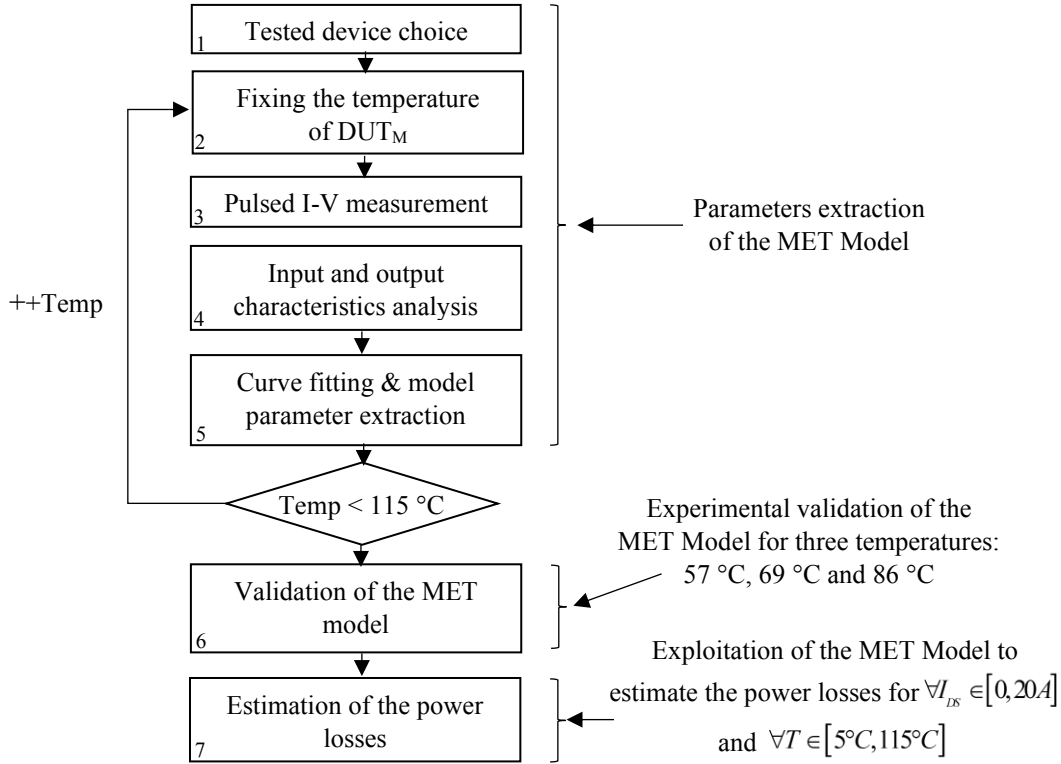


Fig. 3.9: Proposed methodology for estimating the GaN HEMT power losses.

Step 1: The first one concerns the choice of the DUT. For that, a fresh GS66508P from GaN Systems [5], which is a p-type gate normally-off AlGaN/GaN power transistor in the range of 650 V/30 A is selected.

Step 2: The second step is to fix experimentally the temperature of the DUT at 25 °C using a Peltier heater plate.

Step 3: The third step is to perform Pulsed I-V measurements using AMCAD pulsed I-V system at a pulse frequency of 100 Hz with a gate pulse duty cycle of 0.04 %. The pulse width of 4 μ s is shorted enough to ensure iso-thermal measurement of pulsed I-V GaN HEMT characteristics. The used I-V pulsed probes have a high measurement accuracy, which is equal to ± 100 mA.

Step 4: The fourth step is to import the experimental output characteristic (I_{DS} - V_{DS}) and transfer characteristic (I_{DS} - V_{GS}) to a data analyzer software, where the data will be treated and analyzed.

Step 5: The fifth step is to fit the experimental I-V static characteristic curves, then we extract the drain current model parameters. In order to develop the thermal model, we repeat the same previous stages for different temperature starting from 5 °C until we reach the maximum allowed temperature which is equal to 115 °C with a step of 10 °C.

The proposed drain current model is based on a non-segmented, smooth and continuous equation inspired from the Motorola Electro-Thermal Model (MET) developed by Curtice et al. [17] and described in [18], the specific equation is given by:

$$I_{DS} = K \cdot \log \left[1 + \exp \left(\frac{V_{GS} - b}{c} \right) \right] \cdot \frac{(m + n \cdot V_{GS}) V_{DS}}{1 + P \cdot (d + e \cdot V_{GS}) V_{DS}}, \quad V_{DS} \geq 0 \quad (3.3)$$

Where I_D is the drain to source current, V_{DS} is the drain to source voltage, V_{GS} is the gate to source voltage K is the device forward transconductance ($A \cdot V^{-1}$) parameter at $25^\circ C$, P is the output conductance (V^{-1}) at $25^\circ C$, b and c are related parameters of the transfer characteristic, while m , n , d and e are related parameters of the output characteristic. These parameters are obtained by using the Levenberg-Marquardt (L-M) algorithm [19], which is an optimization algorithm appropriate to solve non-linear equations such as Eq. (3.3).

Step 6: The sixth stage of the proposed methodology concerns the experimental validation of the electro-thermal model in a real power switching application. **Fig. 3.10 (a)** shows the schematic of the developed switching bench [20], this circuit offers a low energy consumption because no load is used. Also, it uses similar electrical waveforms on DUT_M , which could exist in a large class of power management products such as DC-DC power converters [21]. Moreover, it enables dynamic measurement of the $R_{DS(ON)}$, hence the calculation of conduction power losses. The electrical signals on DUT_M are limited by two DC supplies. A microcontroller unit [22] generates Pulse Width Modulation (PWM) signals with a frequency range from 0 to 128 kHz and a duty cycle with 1/128 resolution. The DUT_V switches with signal PWM2, the complimentary signal of PWM1 switches both DUT_M and DUT_C . The Galvanic isolated drivers separate control and power blocks [23].

The DUT_M current and voltage experimental waveforms are shown in **Fig. 3.10 (b)**. The V_{DS} voltage switches from 1.14 V to 24 V with a rise time equals to 53.46 ns and I_{DS} current switches from 0 A to 14 A with a rise time equals to 3.94 μs . The studied switching conditions have been chosen to allow the DUT_M switches in the operational switching conditions of power converters.

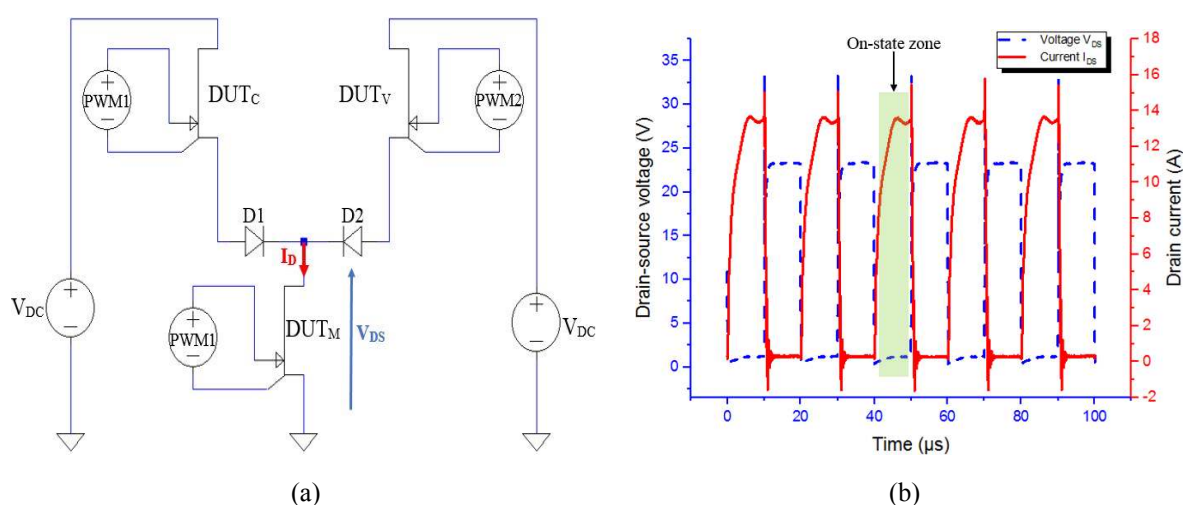


Fig. 3.10: (a) Schematic of the switching bench; (b) Current and voltage waveforms on DUT_M for switching conditions: 50 kHz, duty-cycle = 50 %, and 14 A / 24 V operating conditions.

The developed switching bench with associated instruments and power supplies are shown in **Fig. 3.11**.

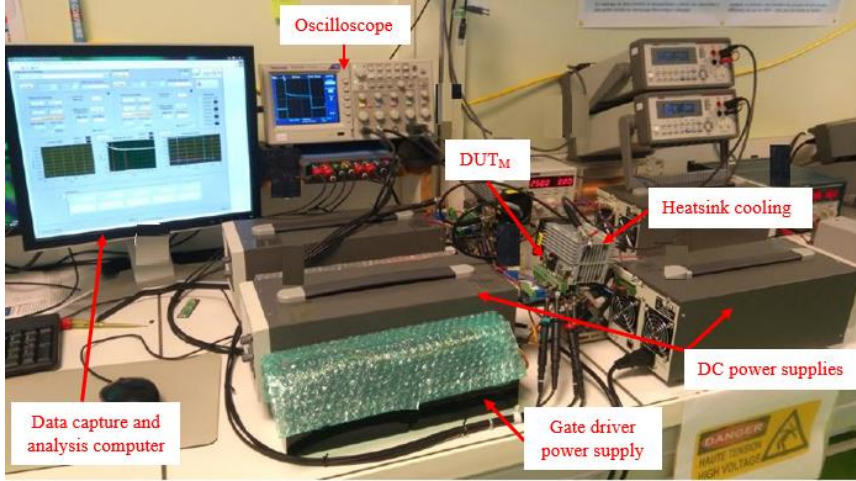


Fig. 3.11: Switching bench platform and associated instruments.

Step 7: The last stage is the estimation of the power losses of the GaN HEMT in a switching circuit application as a function of both temperature and output current.

3.2.3.2. Results and discussions

In this section, we present the results of the extracted MET model and comparisons to the literature. Also, we study the temperature dependency of the GaN HEMT and we describe the MET thermal model. The efficiency of the extracted electro-thermal model is then validated in a real switching application for three chosen temperatures: 57 °C, 69 °C and 86 °C. To evaluate the performance of the curve fitting, the error between measurements and model is given by:

$$\begin{cases} \text{Error} = \left| \frac{E - M}{E} \right| \times 100 \quad (\%) \\ \text{Mean Relative Error} = \frac{100}{n} \sum_{i=1}^n \left| \frac{E_i - M_i}{E_i} \right| \quad (\%) \end{cases} \quad (3.4)$$

Where E is the experimental value, M is the modelled value and n is the number of fitted points. The error reduction is defined as the difference between the constructor model (given by the manufacture) error and the MET model error. The equation of the drain current constructor model is given in [24] by:

$$I_{DS} = K(T) \cdot \log \left[1 + \exp \left(\frac{c_1 \cdot (V_{GS} - b)}{slp} \right) \right] \cdot \frac{V_{DS}}{1 + \max(x_0 + x_1 \cdot (V_{GS} + c_2), c_3) \cdot V_{DS}}, V_{DS} \geq 0 \quad (3.5)$$

Where c_1 , b , slp , x_0 , x_1 , c_2 and c_3 are related parameters of the output characteristic. The application of both the Levenberg-Marquardt algorithm [25] and Orthogonal Distance Regression algorithm on the constructor model did not show convergence of fitting to the experimental data. The proposed MET Model has the advantage to have less parameters compared to the constructor model.

a) *Static characteristics*

Fig. 3.12 (a) and **(b)** show the comparisons of output and transfer characteristics of GaN HEMT obtained by: constructor model (dashed lines), MET model (dot) and measurements (solid lines). **Table 3.2** summarized the static parameters comparison between measurements, constructor model and MET model. The constructor model suffers from an important mismatch compared to measurements, which produces high relative error to the static characteristics. Then, to improve simulation accuracy, we propose the electro-thermal model based on Eq. (3.3). **Table 3.3** shows the extracted static model parameters at 25 °C.

From **Table 3.2**, the MET model shows a good convergence to measurements, which enables an error reduction of $R_{DS(on)}$ by 15.2 %, g_m by 10.19 % and V_{TH} by 6.6 % compared to the constructor model static characteristics. Moreover, the mismatch between the MET model and measurements is significantly reduced compared to the constructor model as shown in **Fig. 3.13** by calculating the mean relative error of constructor model and MET model for static characteristics using Eq. (3.4). By comparing the curve fitting of the MET model with others models provided in the literature [26-27] using the mean relative error given in Eq. 3.4 (**Fig. 3.14**), we conclude that the MET model shows lower mean relative error for the output characteristic at $V_{GS} = 3\text{ V}$ and 25 °C. The accuracy of the MET SPICE model is due to the convergence of the model parameters in Eq. (3.5) with the experimental data. As observed, the MET model uses a non-segmented and smooth continuous equations to describe the static characteristic of GaN HEMT.

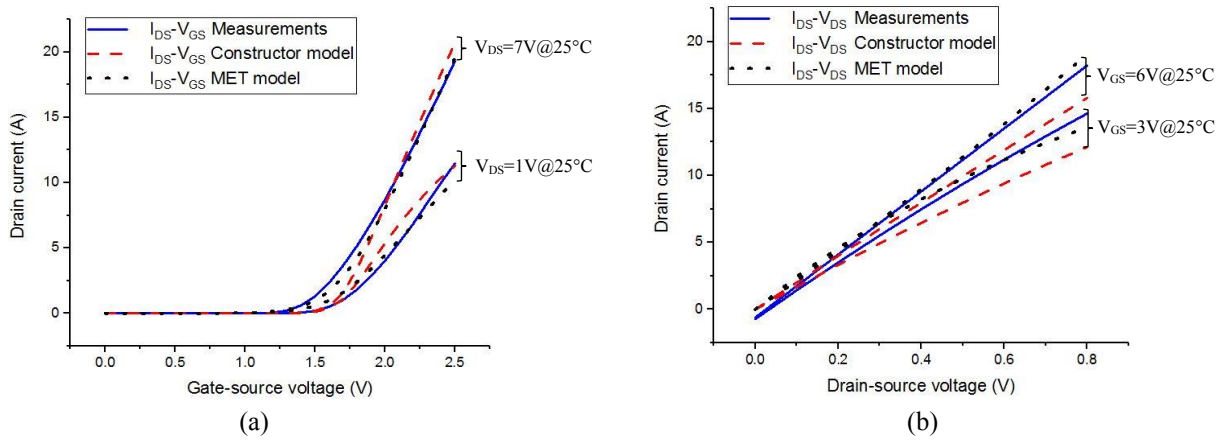


Fig. 3.12: Comparison between measurements, Constructor model and MET model: (a) Transfer characteristics (b) Output characteristics.

Table 3.2: Static parameters comparison between measurements, constructor model and MET model.

Parameter	$R_{DS(on)}$ (mΩ)	g_m (S)	$V_{GS(TH)}$ (V)
Measurements	43.26	21.58	1.82
Constructor model	50.65	25.63	1.65
Constructor model Error (%)	17.08	18.76	9.34
MET model	42.46	23.43	1.77
MET model Error (%)	1.84	8.57	2.74

Table 3.3: Extracted MET model parameters at 25°C.

Parameter	K	B	c	M	n	P	d	E
Value	1.42	1.65	0.14	8.12	-1.15	0.75	1.94	-0.35

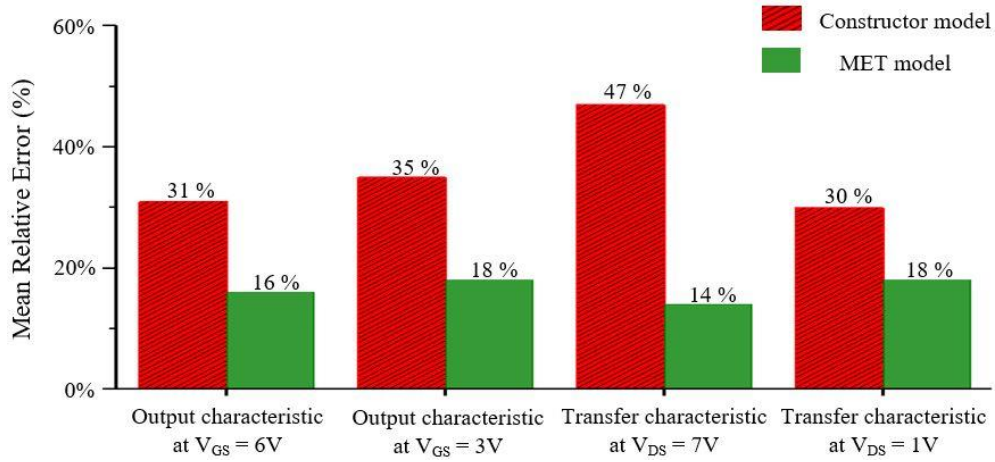


Fig. 3.13: Comparisons of Mean Relative Error between constructor model and MET model for both transfer and output static characteristics.

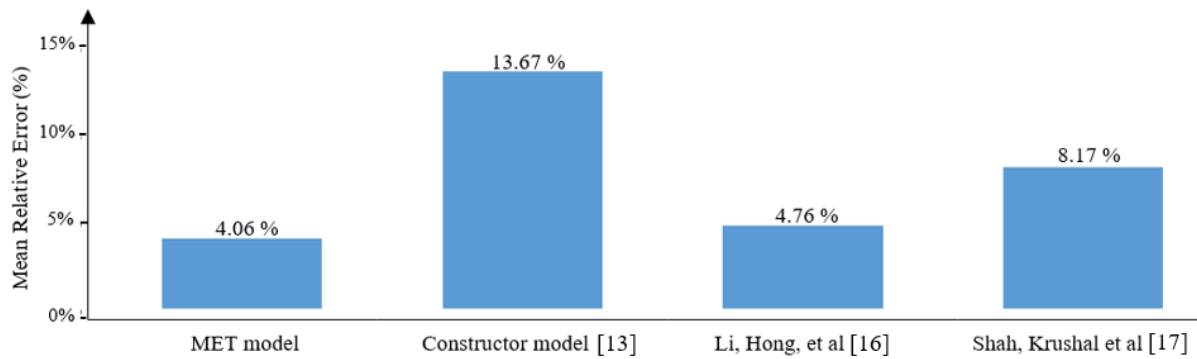


Fig. 3.14: Comparisons of Mean Relative Error between MET model, constructor static model and literature for the output characteristic at $V_{GS} = 3 V$ and 25 °C.

b) Thermal characteristics

To take into consideration the thermal behavior of the tested device in the MET model, the device model should include the temperature dependence of device parameters. However, it is observed from **Fig. 3.15 (a)** and **(b)** that the constructor thermal model suffers from high mismatch compared to measurements. We performed experimentally in **Fig. 3.16** the evolution of the device parameters K and P versus temperature. The results in **Fig. 3.16** are obtained by calculating experimentally the MET model parameters K and P at various temperatures: started from 5 °C to 105 °C by a step of 10 °C. The K and P parameters are extracted using a curve fitting of the MET model to the experimental output and transfer characteristics at each temperature. No temperature dependency was observed for others MET model parameters b , c , m , n , d and e . To overcome this mismatch of constructor thermal model, a quadratic fit of the device parameters (K and P) as a function of temperature is given in [28] by:

$$\begin{cases} K(T) = K \cdot [1 + T_{C1} \cdot (T - 25) + T_{C2} \cdot (T - 25)^2] \\ P(T) = P \cdot [1 + T_{C3} \cdot (T - 25) + T_{C4} \cdot (T - 25)^2] \end{cases} \quad (3.6)$$

Where T_{C1} , T_{C2} , T_{C3} and T_{C4} are temperature coefficients, which are extracted using Levenberg-Marquardt algorithm and given in **Table 3.4**. The K and P parameters are uniformly decreased when increasing temperature as shown in **Fig. 3.16**.

From **Fig. 3.15 (a)** and **(b)**, the MET thermal model shows a good convergence to measurements in term of temperature dependency. The MET model fit very well to measurements at two temperatures for both output and transfer characteristics.

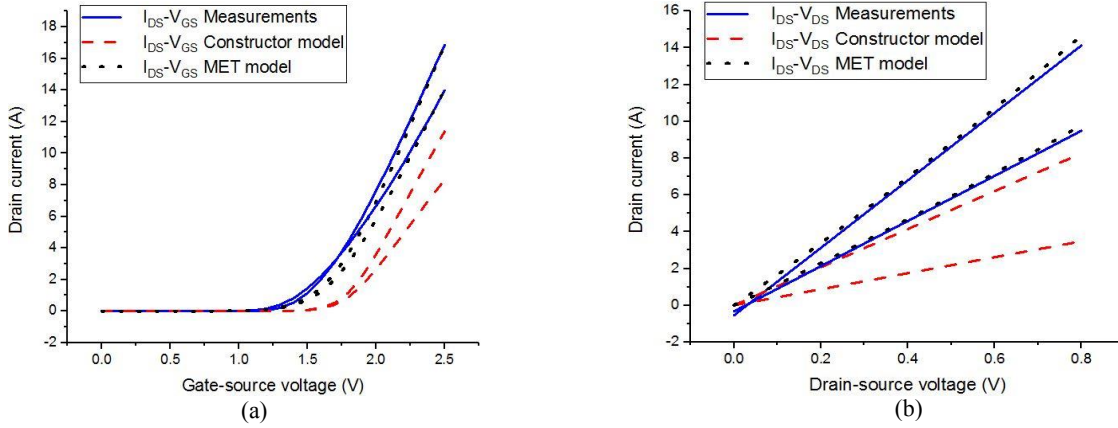


Fig. 3.15: Comparisons between MET model (dot), constructor model (dashed) and measurements (solid): (a) Transfer characteristic for $V_{DS} = 7$ V at 55 °C and 115 °C; (b) Output characteristic for $V_{GS} = 6$ V at 55 °C and 115 °C.

Table 3.4: Extracted MET thermal model temperature coefficients.

Parameter	T_{C1}	T_{C2}	T_{C3}	T_{C4}
Value	-8.02E-3	3.22E-5	-3.75E-3	4.01E-6

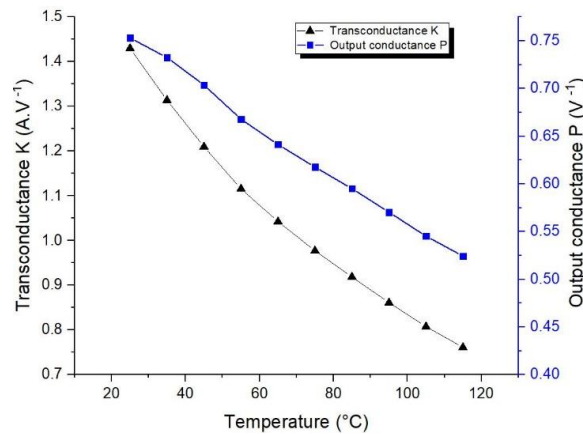


Fig. 3.16: Evolution of the device parameters K and P when varying temperature from 25 °C to 115 °C.

c) Validation of the model

In order to verify the accuracy of the extracted MET model, we implement the switching circuit of **Fig. 3.10 (a)** in the LTspice simulator under the switching conditions described in **Table 3.5**. The off-state voltage $V_{DS(OFF)}$ is chosen equal to 24 V, which is low enough to

ensure the non-effect of traps on dynamic measurements [29]. Also, the chosen frequency of 50 kHz and the duty-cycle of 50 % could be applied to a large application of power converters.

The estimation of the junction temperature T_J from measurements is necessary in order to compare the conduction power losses between measurements, MET and constructor electro-thermal models. The temperature T_J is estimated using the thermal model of DUT_M described in [30]. By using the thermal Ohm's law, we obtain:

$$T_J = P_{loss} \cdot \theta_{JA} + T_A \quad (3.7)$$

Where θ_{JA} is the total thermal resistance from junction to ambient, which is equal to 3.63 °C/W based on manufacturer datasheets and SPICE model [7], T_A is the ambient temperature fixed at 25 °C by heatsink cooling, and P_{loss} is the experimental total power loss of DUT_M over one period in watts. From measurements, P_{loss} is calculated using Eq. (3.8), T_J is calculated using Eq. (3.7), and the device parameters (K and P) that correspond to the temperature T_J are calculated using Eq. (3.6). Table 3.5 shows the calculated values of P_{loss} , T_J , K and P for the three different switching profiles.

$$P_{loss} = \frac{1}{T} \int_0^T i_{ds} \cdot v_{ds} \cdot dt \quad (3.8)$$

After ensuring that the DUT_M switches under the same electrical and thermal conditions in both experimental and simulation, a comparison of the conduction power loss (P_{Cond}) between measurements, constructor model and MET model is achieved. The P_{Cond} is defined in [31] by:

$$P_{Cond} = R_{dyn} \cdot I_D^2 \cdot D \quad (3.9)$$

The dynamic resistance (R_{dyn}) is calculated by:

$$R_{dyn} = \frac{V_{DS(ON)}}{I_{DS}} \quad (3.10)$$

Where $V_{DS(ON)}$ and I_{DS} are the drain-to-source voltage and the drain current during the on state respectively and D is the duty-cycle. From current and voltage temporal waveforms of DUT_M, the experimental and simulated power P_{Cond} for both constructor and MET models are calculated using Eq. (3.9) and shown in **Fig. 3.17** for three junction temperatures of 57 °C, 69 °C and 86 °C. A good convergence of conduction power loss was achieved using the MET model.

Table 3.6 compares the conduction losses between simulation and measurements of the tested device at three junction temperatures: 57 °C, 69 °C and 86 °C. As can be observed, the conduction power losses error between the measurements and MET model is much lower to that of the constructor model at various junction temperatures. The error reduction is defined as the difference between the constructor model error and the MET model error.

Table 3.5: Switching conditions applied to DUT_M at: $V_{DS(OFF)} = 24$ V, $f = 50$ kHz and Duty-cycle = 50 %.

Parameter	I_{DS} (A)	P_{loss} (W)	T_J (°C)	K (A.V ⁻¹)	P (V ⁻¹)
Profile 1	8	8.70	57	1.11	0.67
Profile 2	12	12.20	69	1.01	0.63
Profile 3	14	16.68	86	0.90	0.54

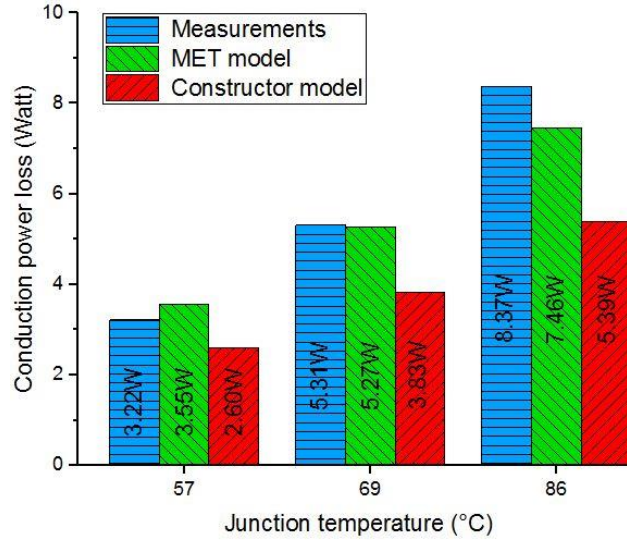


Fig. 3.17: Comparisons of conduction power loss between measurements, MET model and constructor model for three values of T_J : 57 °C, 69 °C and 86 °C.

Table 3.6: Measurements, MET model and constructor model comparisons of conduction power losses.

Conduction power loss (W)	57 °C	69 °C	86 °C
Measurements	3.22	5.31	8.37
MET model	3.55	5.27	7.46
Constructor model	2.60	3.83	5.39
Error reduction (%)	1.55	27.11	24.73

d) *Estimation of the power losses*

The conduction power losses are estimated in a switching power application. For that, we calculate by simulation the P_{Cond} of the extracted MET electrothermal model in the switching circuit of **Fig. 3.10 (a)** for $\forall I_{DS} \in [0, 20A]$ and $\forall T \in [5^\circ C, 115^\circ C]$. **Fig. 3.18 (a)** shows the evolution of the P_{Cond} for various values of I_{DS} at three temperatures: 25 °C, 65 °C and 115 °C. **Fig. 3.18 (b)** shows a 3D graphical representation of the conduction energy losses (E_{Cond}) at the following switching conditions: $f = 50$ kHz, Duty-cycle = 50 % and $V_{DS} = 200$ V.

From the results shown in **Fig. 3.18 (a)**, we estimate the conduction power losses as a function of the drain current I_{DS} and the temperature T using a second order polynomial relationship given by Eq (3.11) [32]. Also, we estimate the conduction energy losses as a function of the drain current I_{DS} and the junction temperature T_J using a 2D polynomial relationship Eq (3.12).

$$\begin{cases} P_{Cond}(I_{DS}, T) = (a_1 T^2 + a_2 T + a_3) I_{DS}^2 + (b_1 T^2 + b_2 T + b_3) I_{DS} + (c_1 T^2 + c_2 T + c_3) & (3.11) \\ E_{Cond}(I_{DS}, T_J) = z_0 + a \cdot I_{DS} + b \cdot T_J + c \cdot I_{DS}^2 + d \cdot T_J^2 + f \cdot I_{DS} \cdot T_J & (3.12) \end{cases}$$

Where a, b and c are coefficients extracted using the L-M algorithm. **Table 3.7** presents the extracted parameters of both the estimated conduction power losses $P_{Cond}(I_{DS}, T)$ and the conduction energy losses $E_{Cond}(I_{DS}, T)$.

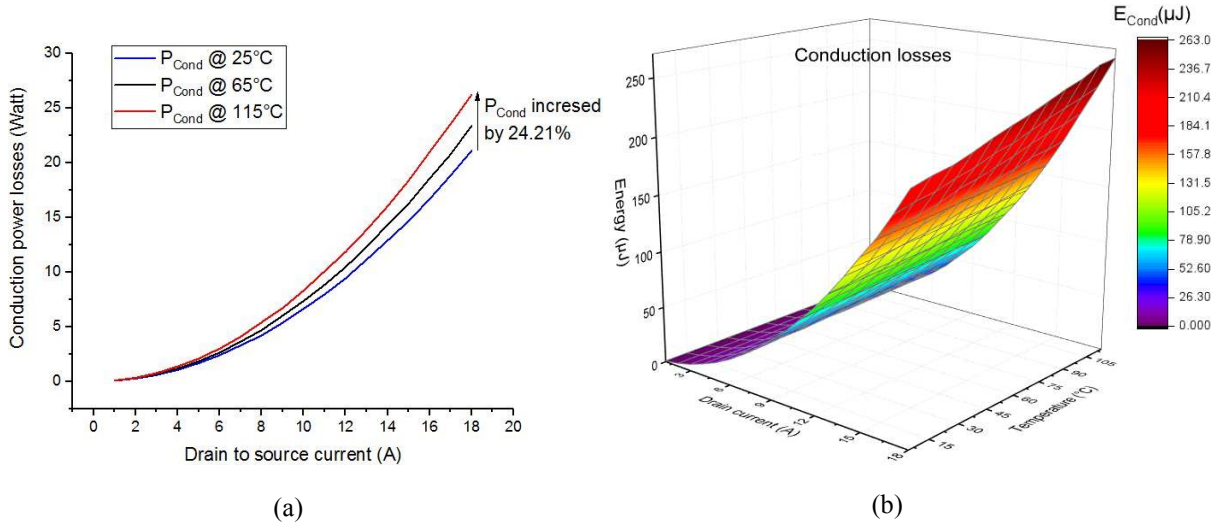


Fig. 3.18: Conduction losses estimation: (a) power losses at three temperatures: 25 °C, 65 °C and 115 °C; (b) energy losses at $f = 50$ kHz, Duty-cycle = 50 %, $V_{DS} = 200$ V.

Table 3.7: Extracted parameters of the estimated conduction power losses $P_{Cond}(I_{DS}, T)$.

Parameter	a_1	a_2	a_3	b_1	b_2	b_3	c_1	c_2
Value	8.22E-9	1.64E-4	0.05948	1.47E-6	5.67E-5	0.02813	-3.94E-6	1.49E-4
Parameter	c_3	z_0	A	b	C	d	f	
Value	-0.05323	6.63 E-3	-1.69E-3	-1.40E-4	7.00E-4	2.81E-7	3.34E-5	

To summarize, based only on experimental I-V pulsed static characterization, the proposed model of losses enables the estimation of the conduction power losses of GaN HEMT in power switching applications for a specified operational value of current and temperature.

3.3. Dynamic characterization of GaN HEMT

In this section, the switching power losses of the GaN HEMT have been estimated by modelling the dynamic C-V characteristics of the GaN HEMT. First, the C-V experimental setup has been presented. Then, both the temperature and frequency dependencies of the C-V characteristic are studied. Finally, the evolution of the power switching losses has been modelled for various values of I_{DS} .

3.3.1. C-V experimental setup

The accuracy of the developed SPICE model has been improved by modelling of dynamic characteristics in order to take into consideration the switching losses when designing power converters with GaN HEMTs. **Fig. 3.19 (a)** shows the C-V bench with the associated instruments, which include: the HP 4192A impedance analyzer, Data capture and analysis computer, Ground connector and DUT.

The HP 4192A is widely used for the measurement of the C-V characteristics of the transistors [33]. This impedance analyzer offers broad frequency range from 5 Hz to 13 MHz and it is very convenient since it can be fully computer controlled [34]. The C-V measurements were performed using HP 4192A impedance analyzer at a frequency of 1 MHz.

Prior to the C-V measurements, both calibration and initialization steps should be performed.

3.3.1.1. Calibration

The analyzer was calibrated at the short and open modes. The calibration improves the precision of measurements by eliminating the parasitic elements [35].

3.3.1.2. Initialization

Before performing the C-V measurement, the DUT is first initialized and then characterized. The device initialization process consists of passing a low current in the drain for a short period in the range of 2 seconds in order to avoid a self-heating of the device.

The proposed initializing process enables the detrapping of charge under the gate. This step allows to create a “stable” and reproducible initial state for the device. **Fig. 3.19 (b)** shows the experimental detrapping setup which consists of a DC voltage generator and both I_{DS} current and V_{DS} voltage measurements.

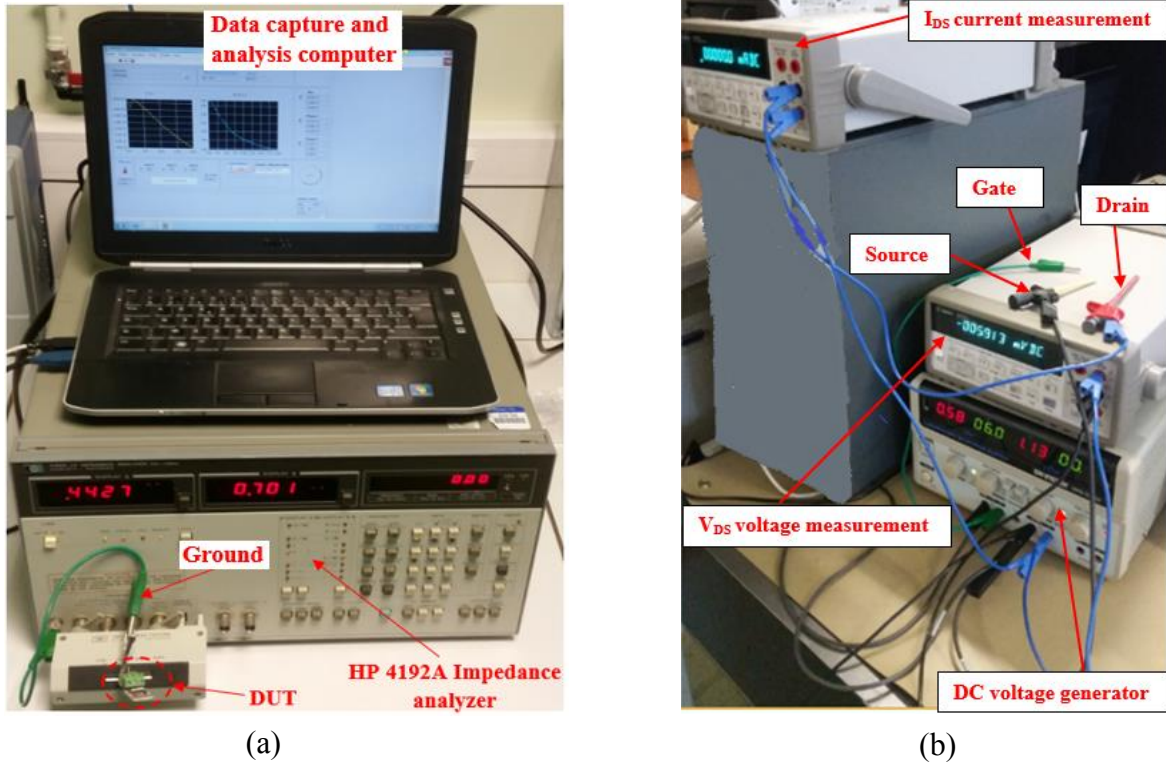


Fig. 3.19: C-V experimental setup: (a) CV bench; (b) detrapping setup.

To confirm that the detrapping method is effective and complete, we have periodically remeasured the C_{GS} - V_{GS} characteristic at room temperature for various length of time: 0, 5 min, 10 min, 15 min and 20 min. The resulting C-V measurements have been reproducible with a mean relative error equals to 2.08 %.

3.3.1.3. Measurement circuits for C_{GS} , C_{GD} and C_{DS}

The measurement circuits for C_{GS} - V_{GS} , C_{GD} - V_{GD} and C_{DS} - V_{DS} characteristics based on an impedance meter (HP4292A) are shown in Fig. 3.20. In case of C_{GS} capacitance measurement, an AC signal is injected at the gate via the high side of the impedance meter and the AC current flowing into the source is sensed at the low side of the meter, which is at ground potential. The drain is also connected to ground but the AC current into this terminal is not sensed by the meter. Thus, the impedance meter measures only C_{GS} as a function of the gate-to-source bias V_{GS} . The stray capacitances on chip (e.g. gate and source pads capacitances) are measured. These capacitances are constants and not affect the extraction process [36].

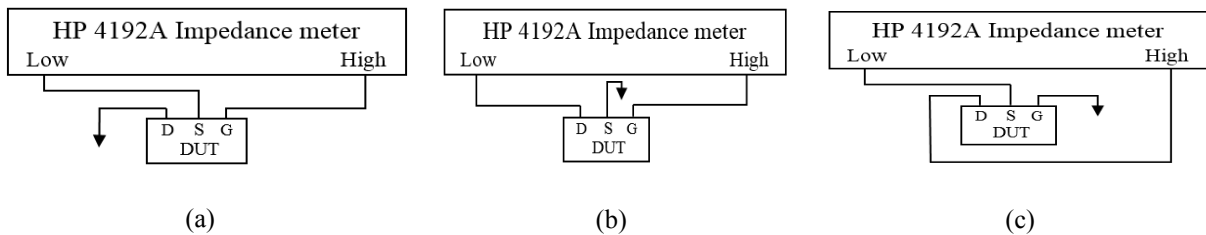


Fig. 3.20: Measurement circuit for the C-V characteristics: (a) C_{GS} - V_{GS} ; (b) C_{GD} - V_{GD} ; (c) C_{DS} - V_{DS} .

3.3.2. Temperature-dependent capacitance–voltage measurements

Understanding the temperature dependence of the GaN HEMT C-V characteristics is of a great importance to the successful design and manufacture of the devices. Thus, it is necessary to investigate the C-V characteristics over a wide temperature range in order to understand the capacitance temperature dependency and the nature of parasitic capacitances at the metal semiconductor interface [37]. For this, the forward and reverse bias C-V measurements of the GaN HEMT contacts have been performed in the temperature range from 5 °C to 115 °C. The temperature is fixed by a Peltier heater plate.

3.3.2.1. C_{GS} - V_{GS} characteristic

The C_{GS} is a measure of the variation of the gate charge Q_G with respect to V_{GS} , and is given by [38]:

$$C_{GS} = \frac{\partial Q_G}{\partial V_{GS}} \quad (3.13)$$

The maximum of $|\partial C_{GS} / \partial V_{GS}|$ corresponds to the point when Q_G is changing most rapidly due to the applied V_{GS} . This represents the onset of strong inversion in the channel 2DEG. Hence, the V_{TH} can be defined as the V_{GS} at which $|\partial C_{GS} / \partial V_{GS}|$ is maximum. **Fig. 3.21 (a)** shows the measured C_{GS} - V_{GS} plot of the tested GaN HEMT and **Fig. 3.21 (b)** shows the corresponded derivative of C_{GS} - V_{GS} plot. The extracted V_{TH} is equal to 1.3 V. As can be observed, below V_{TH} , Q_G is negligible due to the lack of electrons in the channel under the gate. Thus, C_G is also small. Above V_{TH} , C_{GS} quickly rises as electrons are induced in the 2-DEG channel. After the 2-DEG channel is fully turned-on, C_{GS} exhibits a gradual decrease as V_{GS} rises [39].

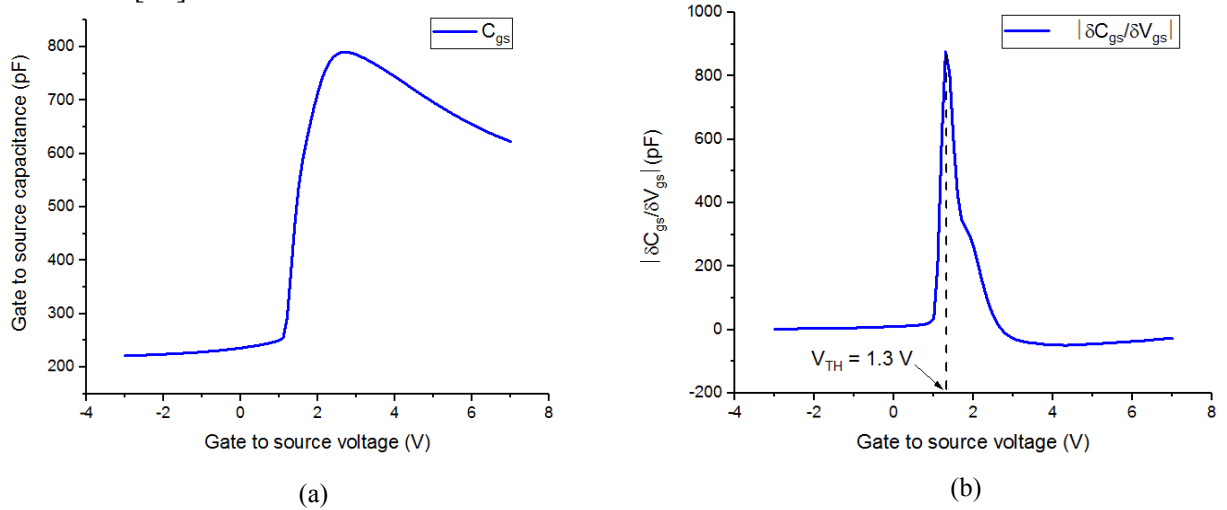


Fig. 3.21: (a) Gate to source capacitance C_{GS} ; (b) Derivative of C_{GS} - V_{GS} plot.

Fig 3.22 (a) shows the measured C_{GS} - V_{GS} characteristics versus V_{GS} , which sweeps from -3V to 7V under operating temperatures equal to 5°C, 45°C, 85°C and 115 °C. The C_{GS} is the maximum of C_{GS} capacitance at 5 °C. It is observed that the $C_{GS(Max)}$ decreases when increasing the temperature and the trends of capacitance versus voltage are similar. **Fig 3.22 (b)** shows the

variation of $C_{GS(\text{Max})}$ versus temperature. A decreasing of 8.22% in $C_{GS(\text{Max})}$ at 115°C can be observed compared to its value at 5°C.

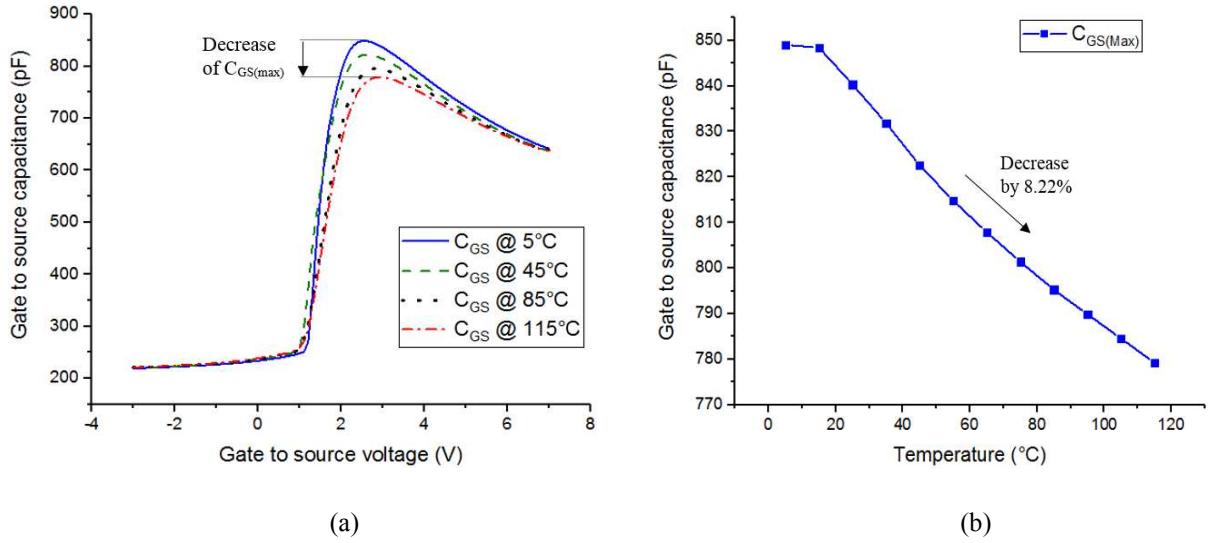


Fig. 3.22: (a) C_{GS} - V_{GS} characteristics for various temperatures: 5°C, 45°C, 85°C and 115 °C. (b) $C_{GS(\text{Max})}$ as a versus temperature.

3.3.2.2. C_{GD} - V_{GD} characteristic

The temperature dependency of the measured C_{GD} - V_{GD} under operating temperatures equal to 5°C, 45°C, 85°C and 115 °C is shown in **Fig 3.23** (a). The gate-to-drain voltage (V_{GD}) sweeps from -3V to 7V by a step of 0.1V. It is observed that C_{GD} capacitance in the inversion region of the tested GaN HEMT at 105 °C decreases when increasing the temperature. **Fig 3.23** (b) shows the variation of $C_{GD(\text{Max})}$ versus temperature. A decreasing of 9.34% in $C_{GD(\text{Max})}$ at 115°C can be observed compared to its value at 5°C.

The decrease of both the gate capacitances C_{GS} and C_{GD} when increasing the temperature is also observed in [40] and is related to the variation of Mg-doped p-GaN mobility under the Schottky contact of the GaN HEMT. The expression of the Schottky gate capacitance C_G is given by [41]:

$$C_G = \sqrt{\frac{q\epsilon_s A^2 N}{2(V_{bi} + V)}} \quad (3.14)$$

Where V_{bi} is the built-in potential, N is the carrier concentration, q is the electronic charge, A is the area of the Schottky contact, and ϵ_s is the permittivity of the semiconductor for AlGaN barrier layer.

Authors in [42] have calculated the temperature dependence of the carrier concentration N parameter. They found that the carrier concentration decreases with temperature, and the values of N vary from $2.767 \times 10^{21} \text{ cm}^{-3}$ to $1.952 \times 10^{21} \text{ cm}^{-3}$ in the temperature range from 223 K to 398 K.

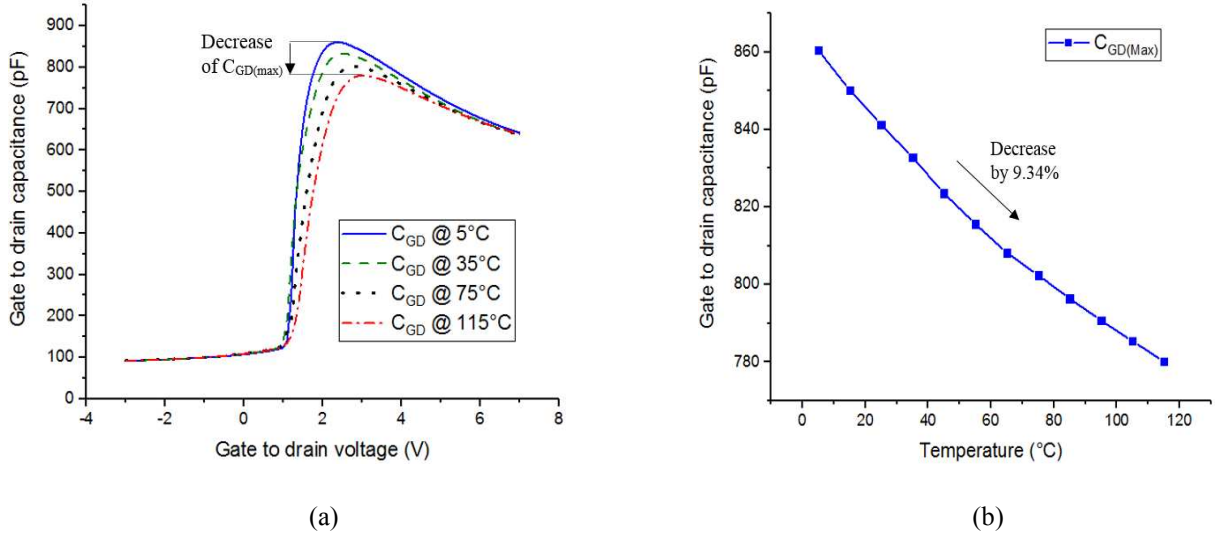


Fig. 3.23: (a) C_{GD} - V_{GD} characteristics for various temperatures: 5°C, 45°C, 85°C and 115 °C. (b) $C_{GD(Max)}$ as a versus temperature.

3.3.2.3. C_{DS} - V_{DS} characteristics

The measured C_{DS} - V_{DS} characteristics at various temperatures equal to 5°C, 45°C, 75°C and 115 °C is shown in **Fig. 3.24 (a)**. The V_{DS} sweeps from 0V to 20V by a step of 1V. As can be observed, the maximum C_{DS} capacitance increases when increasing the temperature. **Fig. 3.24 (b)** shows the variation of C_{DS} capacitance with regard to the temperature. An increasing of 0.62% in C_{DS} at 115°C can be observed compared to its value at 5°C.

According to [43], the depletion width of the AlGa_N layer affects the value of C_{DS} . Authors in [42], have observed that the depletion width of the ALGa_N layer decreases with temperature, and varies from 4.675 nm to 4.644 nm in the temperature range from 223 K to 398 K. The AlGa_N parasitic capacitance is given in [43] by:

$$C_{AlGaN} = \epsilon_0 \epsilon_{AlGaN} \frac{A}{d_{AlGaN}} \quad (3.15)$$

Where d_{AlGaN} is the depletion width of the AlGa_N layer and ϵ_0 is dielectric constant of vacuum ($\epsilon_0 = 8.85 \cdot 10^{-14}$ F/cm) and ϵ_{AlGaN} dielectric constant of the AlGa_N ($\epsilon_{AlGaN} = 8.8$).

From Eq. (3.15), the decrease of the depletion region with temperature induces a positive change of C_{DS} capacitance, which is confirmed in [43].

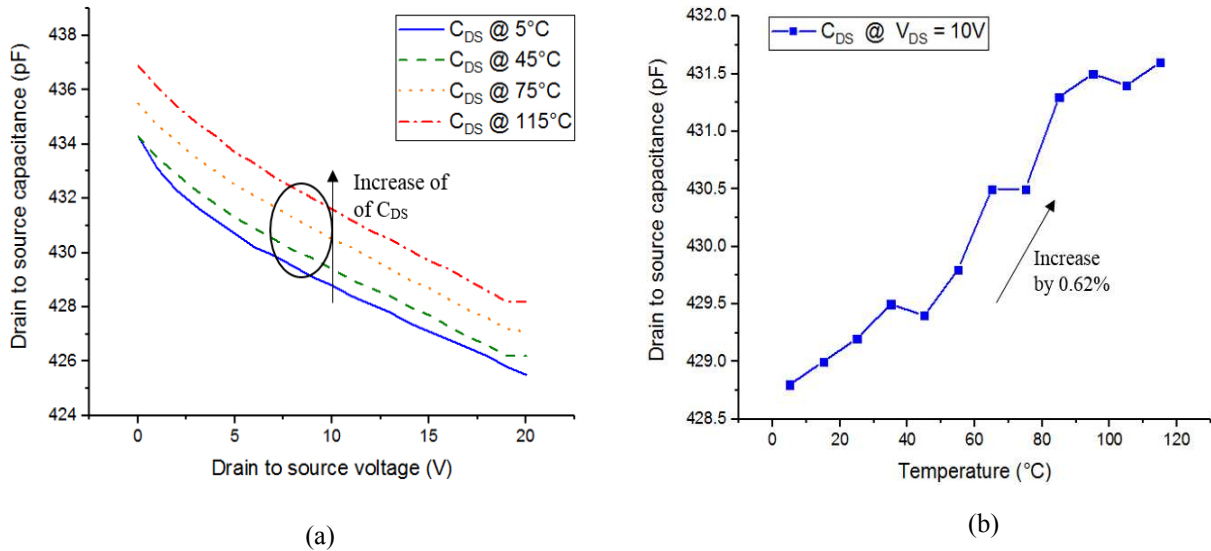


Fig. 3.24: (a) C_{DS} - V_{DS} characteristics for various temperatures: 5°C, 45°C, 85°C and 115 °C. (b) C_{DS} versus temperature at V_{DS} equals 10 V.

3.3.3. Frequency dependent of C-V measurements

With the aim to investigate the parasitic frequency-dependent switching losses, C-V measurements are carried out using HP 4192A impedance analyzer on a fresh GaN HEMT in the frequency range from 100 kHz to 10 MHz. **Fig. 3.25 (a)** shows the frequency-dependent C-V measurements. The capacitance was measured with an AC signal with amplitude of 50 mV at frequencies ranging 100 kHz, 1 MHz and 10 MHz. The gate voltage was swept from depletion (-3 V) to accumulation (7 V) by a step of 0.1 V. As can be shown in **Fig. 3.25 (a)**, the C-V characteristic of the DUT presents a frequency dependency by increasing the ac signal frequency from 1 MHz to 100 kHz. It can be noticed that the C-V characteristic in the inverse-bias ($V_{GS} < V_{TH}$) significantly increases when increasing the frequency from 100 kHz to 10 MHz. This distortion in the C-V characteristic when increasing the frequency is mainly originates from the increased gate leakage and insufficient ac-signal frequency [42]. Thus, to obtain the C-V characteristics within a wide bias range, it is necessary to boost the measurement frequency up to 1 MHz. However, when biased at forward voltages ($V_{GS} > 0$ V), the measured capacitance did not show a significant dependency on the frequency.

Fig. 3.25 (b) shows C-V characteristics measured on a tested GaN HEMT at 1 MHz and at room temperature. The data were taken for the two voltage sweep directions (the direction is marked by the arrow near each curve). As can be observed, the V_{TH} hysteresis with a shift of 0.72 V when the bias swept from -3 V to 7 V and 7 V to -3 V. According to [44], The hysteresis in the C-V measurement is induced by the charge trapped near the p-GaN interface, which induces the threshold voltage instability due to their different electron capture/emission time when measured in different directions.

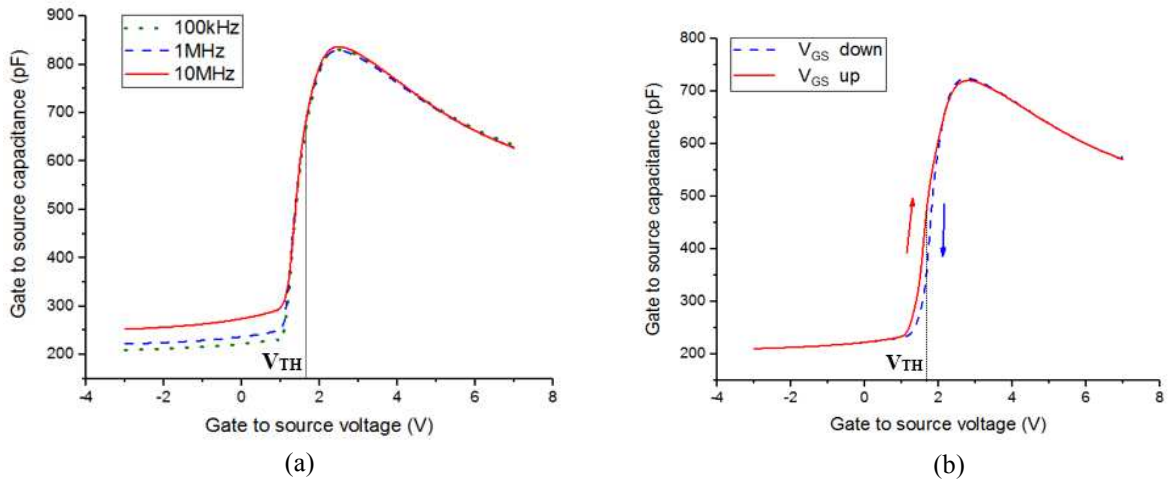


Fig. 3.25: (a) C-V-f measurements; (b) Measured C_{GS} - V_{GS} characteristics at 1 MHz and at room temperature. Solid curves correspond to the voltage sweep from negative to positive values of V_{GS} and dashed curves correspond to the opposite sweep direction.

3.3.4. C-V modeling methodology

In power transistor models, it is very important that device capacitances are modelled accurately so that switching losses and gate timing requirements of the converter can be accurately determined [45]. The modeling of the dynamic behavior of the power GaN HEMT required sensitive C-V measurements, since the GaN transistors have lower parasitic capacitances in the range of 100 pF [24] compared to Si devices which are in the range of 1000 pF [46]. This makes the GaN technology very attractive for both RF markets and power converter applications with high speed and low power switching losses. For that, an accurate dynamic model is necessary. In the literature, several capacitance models of GaN transistor have been proposed. References [47] and [48] have modelled the GaN HEMT capacitance by the series combination of a fixed capacitance, representing the oxide capacitance of a MOS gate and a SPICE model for the diode to represent the field-dependent semiconductor capacitance [49]. However, these models do not fit the C-V measurements of the studied DUT, because the C-V characteristic of the p-GaN gate HEMTs are different to that of Si MOS gate transistors, due to the Mg doper concentration under the gate of the studied GaN transistor which enables a normally-off behavior of the GaN HEMTs.

The proposed methodology for modeling the non-linear capacitance of the GaN HEMT is to extract the one-dimension model. In fact, the gate to drain capacitance C_{GD} depends only on V_{GD} voltage that will be selected close to the application range area between -3 V and 7 V. The C_{GS} depends on intrinsic V_{GS} voltage, chosen close to the application range area between -3 V and 7 V. The output Capacitance C_{DS} depend on V_{DS} voltage, selected close to the application range area between 0 V and 20 V. This approach reduces significantly the complexity of the model, and improves both the speed and convergence behavior of the simulation. The nonlinear functions chosen to fit the extracted C_{GS} , C_{GD} and C_{DS} capacitances are based on the equations given by [50].

$$\left\{ \begin{array}{l} C_{GS} = C_0^{GS} + \frac{C_1^{GS} - C_0^{GS}}{2} \left[1 + \tanh(A_{GS}(V_{GS} + V_{TH})) \right] - \frac{C_2^{GS} - C_0^{GS}}{2} \left[1 + \tanh(B_{GS}(V_{GS} + V_P)) \right] \\ C_{GD} = C_0^{GD} + \frac{C_1^{GD} - C_0^{GD}}{2} \left[1 + \tanh(A_{GD}(V_{GD} + V_{TH})) \right] - \frac{C_2^{GD}}{2} \left[1 + \tanh(B_{GD}(V_{GS} + V_P)) \right] \\ C_{DS} = C_0^{DS} \times [1 + a \cdot V_{DS} + b \cdot V_{DS}^2] \end{array} \right. \quad (3.16)$$

Where, C_0 , C_1 , C_2 , A , B are related parameters of the C_{GS} - V_{GS} and C_{GD} - V_{GD} characteristics and the V_P is the pinch-off voltage. **Fig. 3.26** shows the representation of these parameters on the C_{GS} - V_{GS} characteristic.

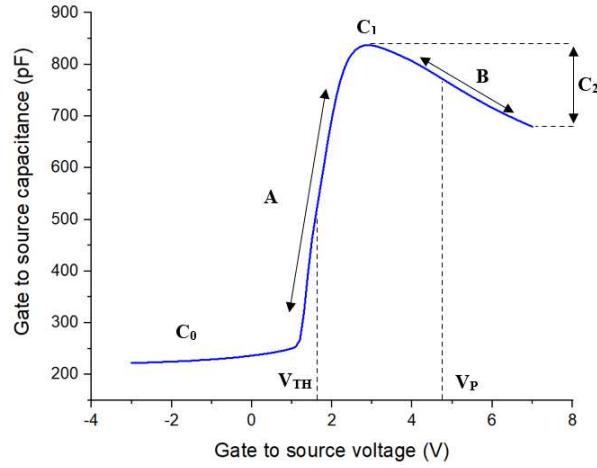


Fig. 3.26: C_{GS} capacitance model parameters.

The extrapolation of the model parameters of (Eq.3.16-3.17) is performed using the Trust-Region algorithm [51]. The initial values of the algorithm are extracted manually in order to reduce the calculation steps. **Table 3.8** shows the extracted values of the C_{GS} , C_{GD} and C_{DS} at 25 °C.

Table 3.8: Extracted values of C_{GS} , C_{GD} and C_{DS} at 25°C.

Parameters	C_0^{GS}	C_1^{GS}	A_{GS}	V_{TH}	C_2^{GS}	B_{GS}	V_P	
Value	221.5 pF	790 pF	469.22 pF/V	1.3 V	622.6 pF	-43.02 pF/V	5 V	
Parameters	C_0^{GD}	C_1^{GD}	A_{GD}	C_2^{GD}	B_{GD}	C_0^{DS}	a	B
Value	98.41pF	838.76 pF	3.001 pF/V	200.95 pF	0.63 pF/V	434.316	-1.43E-3	2.39E-5

In a SPICE simulator [52], we have simulated the modelled $C_{GS}(V_{GS})$, $C_{GD}(V_{GD})$ and $C_{DS}(V_{DS})$ capacitances. As shown in **Fig. 3.27**, the modelled capacitances fit with high convergence the measured capacitances at 25 °C. The modeling of the dynamic behavior of the

DUT, enables the estimation of the switching power losses of the GaN HEMT with high accuracy using a simulation approach.

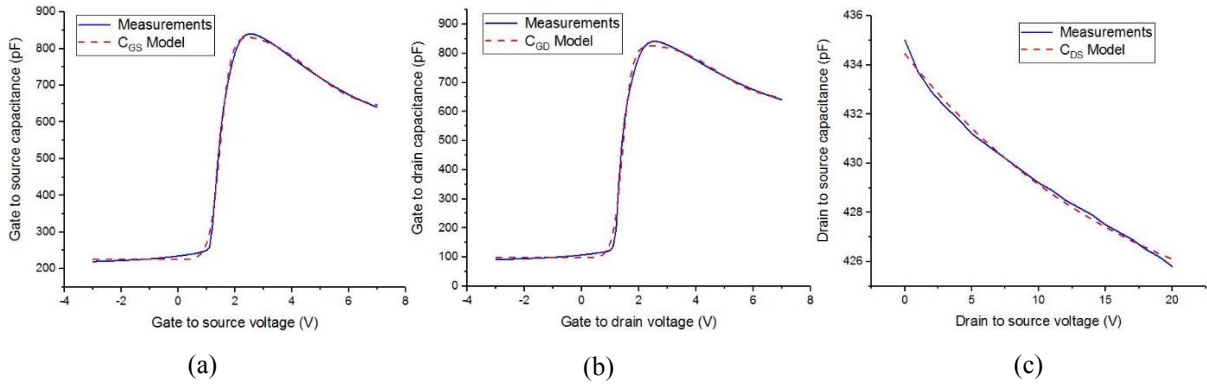


Fig. 3.27: Comparison between measured and modelled capacitances at 25 °C: (a) C_{GS} - V_{GS} ; (b) C_{GD} - V_{GD} ; (c) C_{DS} - V_{DS} .

In order to estimate the switching power losses of the GaN HEMT in a switching power application, we have implemented in a SPICE simulator the modelled static characteristic obtained in section I and parasitic capacitances of the GaN HEMT obtained in section II.

Fig. 3.28 (a) shows the GaN HEMT current and voltage simulated switching waveforms during the turn-on. The existence of both the current and voltage simultaneously during the turn-on time ($T_{SW(on)}$) generates power switching losses. Based on **Fig. 3.28 (a)**, we have calculated by simulation the power losses $P_{SW(on)}$ as a function of the drain current I_{DS} at the temperature of 25 °C by calculating the turn-on power switching losses using Eq. (3.19) [53].

$$P_{SW(on)} = \frac{1}{T_{SW(on)}} \int_0^{T_{SW(on)}} i_{ds} \cdot v_{ds} \cdot dt \quad (3.19)$$

Where, $P_{SW(on)}$ is the turn-on power switching losses in (Watt) and $T_{SW(on)}$ is the turn-on switching time. **Fig. 3.28 (b)** shows the evolution of the switching power losses $P_{SW(on)}$ as a function of drain to source current at 25 °C. The proposed model of the switching losses enables the estimation of the GaN HEMT power converter efficiency with high accuracy, by taking into consideration the effect of C-V characteristics in the GaN HEMT SPICE model.

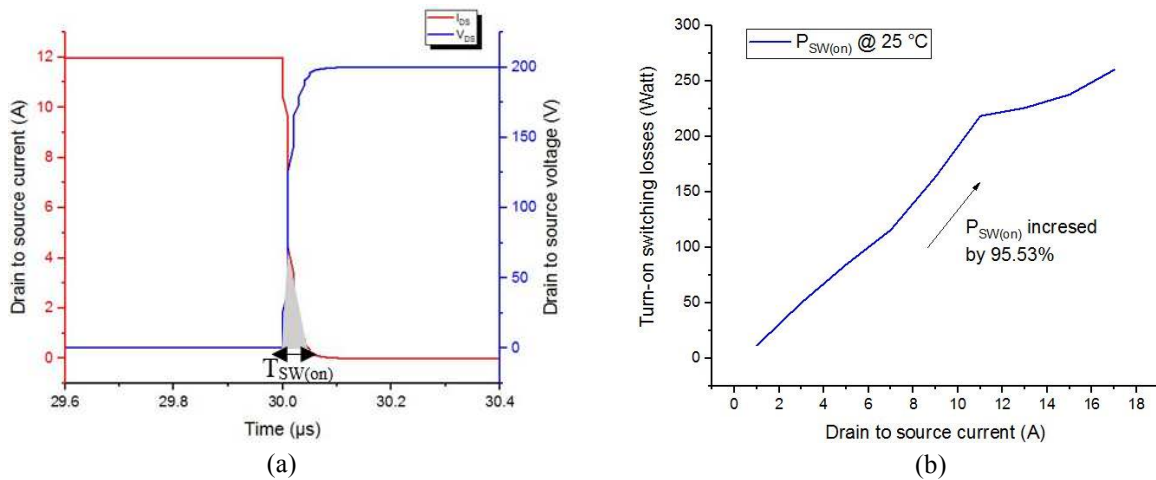


Fig. 3.28: Turn-on switching losses estimation at 25 °C, $f = 50$ kHz, Duty-cycle = 50 % and $V_{DS} = 200$ V: (a) switching times, (b) power losses.

3.4. Leakage current characteristics

In this section, the gate power losses of the GaN HEMT have been estimated by modelling the gate leakage current characteristics of the GaN HEMT. First, the low current experimental setup has been presented. Then, both the temperature and voltage dependencies of the leakage current characteristic are studied. Finally, the evolution of the gate power losses has been modelled for various values of temperature.

3.4.1. Low current experiment setup

The low current measurement was performed using Keithley 6485A SourceMeter. **Fig. 3.29** shows the leakage current bench with associated instruments, including: voltage source, Multimeter, interface circuit, measurement interface and Keithley 6485A Source meter [54].

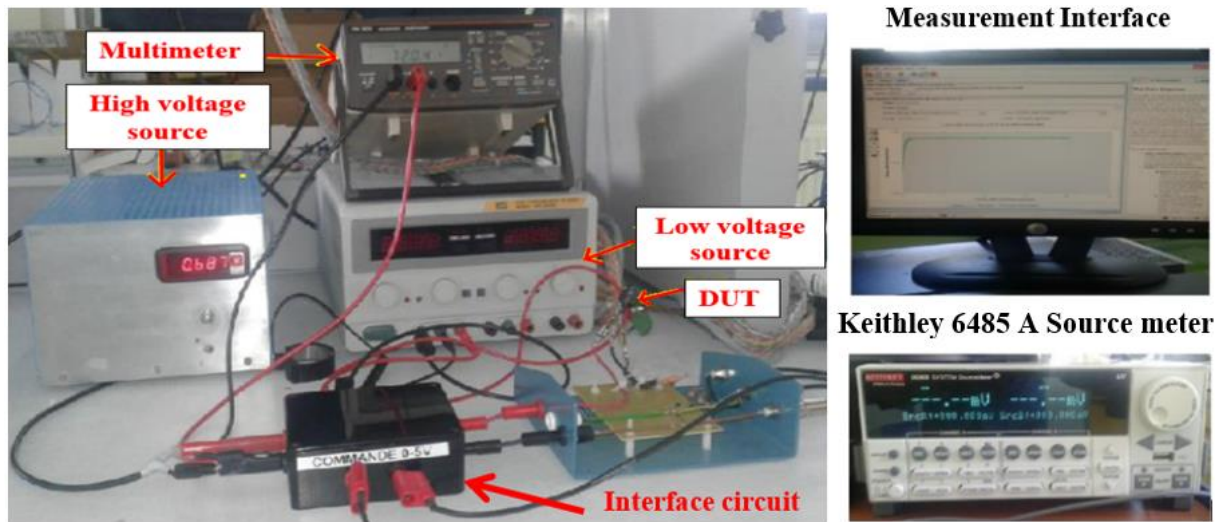


Fig. 3.29: Leakage current measurement bench.

3.4.2. Gate leakage current temperature dependency

The gate leakage current (I_{GSS}) is defined as the leakage that occurs when the specified voltage is applied across the gate and source with drain and source short-circuited. It is used to evaluate the gate blocking capacity of the device. The leakage current measurements were performed by using Keithly 6485 A SourceMeter at $V_{GS} = 6$ V and $V_{DS} = 0$ V. **Fig. 3.30 (a)** shows the evolution of the gate leakage current as a function of temperature. As shown, the current I_{GSS} is increased by 77.77 % when varying temperature from 5 °C to 105 °C. It was demonstrated in reference [55] that increasing temperature may reduce the schottky barrier height at the metal/p-GaN contact and, consequently, increase the gate leakage current. Moreover, in p-GaN/AlGaIn/ GaN heterostructure, the reduction of the Schottky barrier height at the metal/p-GaN gate enhances the tunneling of holes through the barrier [56]. Then, as highlighted by Hwang et al. [57], the enhancement of holes injection leads not only to a negative shift of the V_{TH} but also to an increase in the leakage current in p-GaN HEMT. The increase in

the leakage gate current when increasing temperature is also observed in [58], which is attributed to the lowering of the Schottky barrier height of the metal/p-GaN gate.

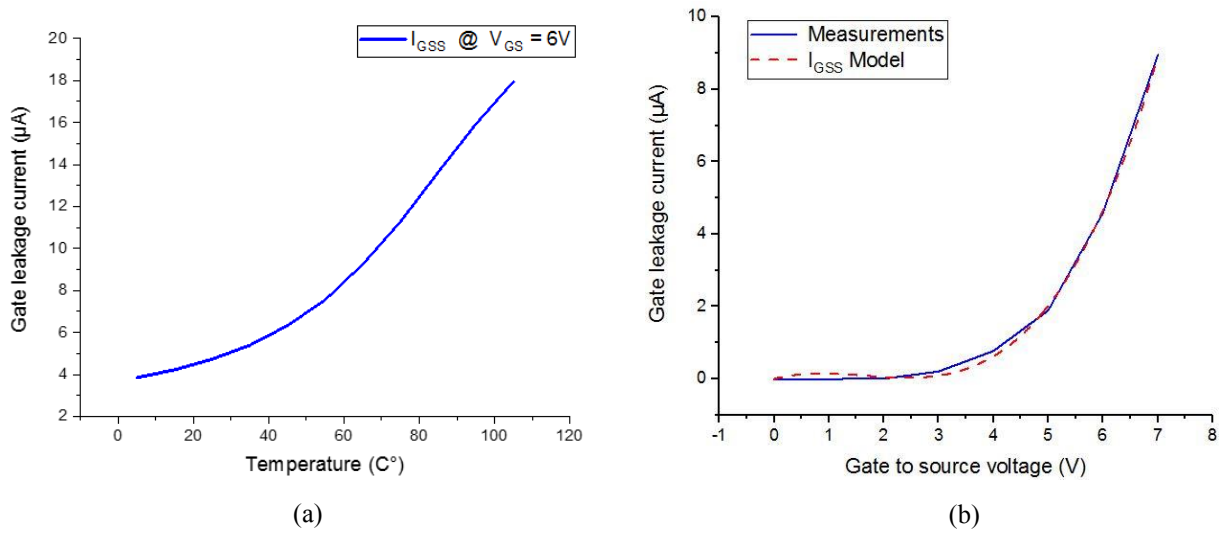


Fig. 3.30: Gate leakage current: (a) temperature dependency at $V_{GS} = 6V$; (b) I_{GSS} Model as a function of V_{GS} at $25^\circ C$.

3.4.3. Gate leakage current power estimation

To accurately estimate the efficiency of GaN HEMT power converters, it is important to calculate the gate power losses caused by the leakage current in the gate. The I_{GSS} current in GaN HEMTs can be modelled as a voltage dependent current source by [59]:

$$I_{GSS} = I_0^{GSS} \cdot (1 + a \cdot V_{GS} + b \cdot V_{GS}^2 + c \cdot V_{GS}^3) \quad (3.20)$$

Where I_0^{GSS} is the gate leakage current at $V_{GS} = 0 V$ and a, b, c are polynomial coefficients parameters of I_{GSS} current. **Table 3.9** shows the extracted values of the I_{GSS} current model of Eq. (3.20). As observed in **Fig. 3.30 (b)**, the I_{GSS} current model fit with high convergence the measurements of I_{GSS} at $25^\circ C$. Indeed, the modeling of the gate leakage current, enables the estimation of the gate power losses of the GaN HEMT with high accuracy using a simulation approach.

Table 3.9: Extracted I_{GSS} model parameters at $25^\circ C$.

Parameter	I_0^{GSS}	a	b	C
Value	4.58 μA	-0.87	0.18	-6.39E-3

The gate power loss is defined in [60] by:

$$P_{GSS} = I_{GSS} \cdot V_{GS} \quad (3.21)$$

Fig. 3.31 shows the evolution of the gate power losses as a function of temperature at $V_{GS} = 6 V$. As can be observed, the gate power losses are very low compared to the conduction

and switching losses of the GaN transistors at various junction temperatures. This result enables the estimation of the GaN power converters efficiency with high accuracy, by taking into account the gate power losses when calculating the efficiency of the power converters.

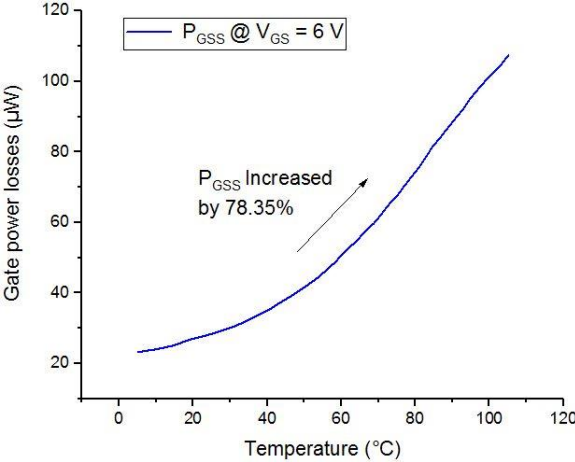


Fig. 3.31: Gate power losses estimation versus temperature at $V_{GS} = 6 V$.

3.5. Estimation of the GaN HEMT power converters efficiency

In this section, we have built an accurate power losses model of the GaN HEMT based on experimental measurements, which includes the major power losses in power switching applications: conduction power losses, switching power losses and gate power losses.

Using the extracted power losses model of the GaN HEMT, we have estimated the efficiency of a 30 V / 200 V DC-DC converter stage using the GaN HEMT. Fig. 3.32 shows a solar energy application which include a solar photovoltaic panel that produce an output voltage of 30 V. This voltage is boosted to 200 V using a power DC-DC converter for charging electrical devices in smart houses. The solar energy application shown in Fig. 3.32 is a use case example for applying the developed methodology for estimating the GaN HEMT power losses in power switching applications based on experimental measurements.

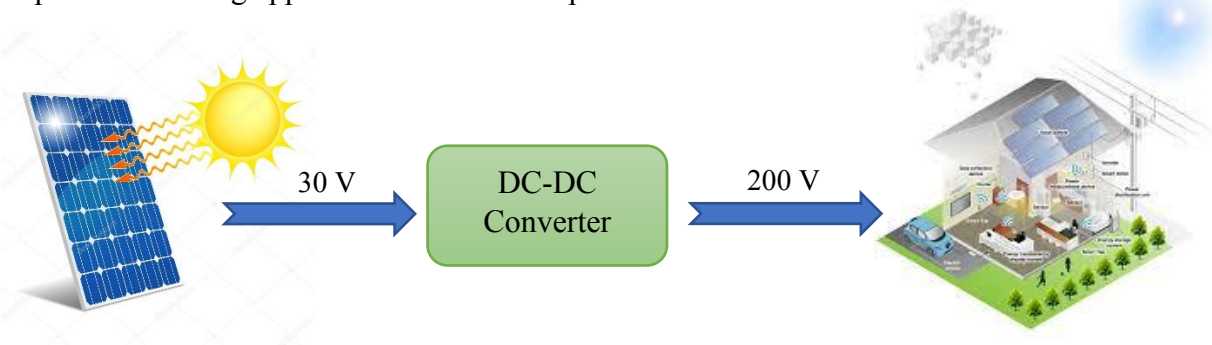


Fig. 3.32: Solar energy application with a 30V/200V DC-DC converter stage.

The power efficiency of the DC-DC power converter shown in the solar application has been investigated by calculating the power losses of each component in the DC-DC converter, including the power losses in the diode, inductor, capacitor, GaN HEMT and output load.

Fig. 3.33 shows the DC-DC converter circuit, which is a 30 V / 200 V boost converter. The DUT_M is the extracted SPICE model of the GaN HEMT.

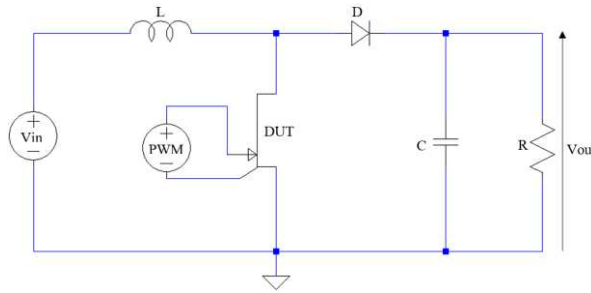


Fig. 3.33: DC-DC boost converter, with $L = 170$ mH, $C = 850$ μ F and $R = 20$ Ω , at 50 kHz switching frequency, 30 V input voltage and 200 V output voltage.

The power losses in the inductor, capacitor and diode are given respectively by [61].

$$P_L = \left(I_{out}^2 + \frac{\Delta I_L^2}{12} \right) R_L \quad (3.22)$$

$$P_C = R_C \frac{\Delta I_L^2}{12} \quad (3.23)$$

$$P_D = V_D I_{out} (1 - D) \quad (3.24)$$

Where I_{out} is the output current, ΔI_L is the inductor current ripple, which assumed equals to 30% of the maximum output current, D is the duty-cycle, R_C is the equivalent series resistance of the capacitor, equals to 30 m Ω , R_L is the equivalent series resistance of the inductor, equals to 0.2 m Ω , V_D is the forward voltage of the diode, equals to 0.7 V. **Table 3.10** summarizes the total losses and calculates the efficiency of a 30 V / 200 V DC-DC boost converter with GaN HEMT at 25°C and $I_{out} = 10$ A.

The efficiency estimation of a GaN HEMT 30 V / 200 V DC-DC boot converter versus output current is shown in **Fig. 3.34**. The average efficiency has been estimated to be equal to 92.09 %.

Similar efficiency of 92 % was obtained experimentally in [62] at an output power of 2 kW in a 400V-to-12V DC-DC converter using same tested device GaN HEMT GS66508P.

According to [62], the calculation of the power converter efficiency experimentally required important investments on equipment such as: high power DC supplies and loads. Also, running experimental power converter required high energy consumption, which is also a concern in energy efficiency, for example a 1000 hours campaign could consume as much as 20 MWh.

Table 3.10 : Total losses in DC-DC boost converter with GaN HEMT at 25°C and $I_{out} = 10$ A.

Output power	P_{out}	2000 W
Power lost in the inductor	P_L	20.05 mW
Power lost in the capacitor	P_C	22.5 mW
Power lost in the diode	P_D	1.05 W
Conduction power losses of the GaN HEMT	P_{Cond}	6.66 W
Switching power losses of the GaN HEMT	P_{SW}	163.8 W
Gate power losses of the GaN HEMT	P_{GSS}	27.91 μ W
Total power losses of the GaN HEMT	$P_{GAN} = P_{Cond} + P_{SW} + P_G$	170.46 W
Total power lost	P_{lost}	171.55 W
Input power	$P_{in} = P_{lost} + P_{out}$	2170.55 W
Efficiency	$\eta = \frac{P_{out}}{P_{in}}$	92.14 %

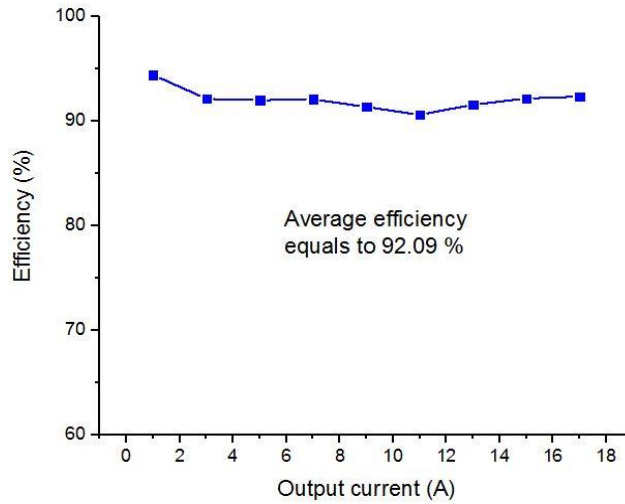


Fig. 3.34: Efficiency estimation of a GaN HEMT 30 V/ 200 V DC-DC boot converter versus I_{out} at 50 kHz and 25 °C.

3.6. Conclusion

In this chapter, an experimental method is used to estimate the power losses of the GaN HEMTs in switching applications. The proposed approach is based on experimental I-V pulsed, C-V and low current characterizations. The static characteristics of the GaN HEMT have been modelled in section 3.2. The MET drain current model has shown high convergence compared

to the experimental measurement, which enables the estimation of the power conduction losses with high accuracy. The switching power losses of the GaN HEMT have been estimated by modelling the dynamic characteristics of the GaN HEMT. The modelled C_{GS} , C_{GD} and C_{DS} capacitances show high convergence compared to the experimental measurements. The gate power losses of the GaN HEMT have been modelled by measuring experimentally the gate leakage current of the DUT. As a result of this study, both the static and dynamic power losses of the GaN HEMT can be estimated. The impact of the conduction power losses, switching power losses and gate power losses on the efficiency of power converters are modelled using SPICE simulation approach. The evolution of the GaN HEMT power efficiency in renewable energy application switching applications is modelled as a function of the output current. The accuracy and good convergence of simulation to experimental measurements provide a good way to design power converters with GaN HEMTs. Moreover, this approach offers to the power converter designers the possibility to estimate the power losses of GaN HEMT with high accuracy without the use of complex switching bench, which reduces the time to market and cost. The proposed methodology for the estimation of the GaN HEMT power losses is used in chapter 5 to study the impact of aging the power GaN HEMT under operational switching condition on the power converters efficiency. In the next chapter, The SPICE model is completed by adding the effects of the parasitic elements of the GaN HEMT. The parasitic resistances, inductances and capacitances of the DUT are extracted using S-parameters characterization.

3.7. References

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Chapter 4: Extraction of the power GaN HEMTs intrinsic and extrinsic elements using S-parameter measurements

4.1. Introduction

The GaN transistors constitute an enabling technology for efficient power conversion at switching frequencies higher than the megahertz. However, their very low switching times (a few nanoseconds) generate high disturbances by interaction with parasitic elements. Thus, in order to accurately simulate the transistor behavior in power converters and estimate the power losses, it is of great interest to accurately determine the parasitic elements of the device such as: resistances, inductances, and capacitances.

In order to investigate the impact of the high switching frequency on the power converters efficiency, parasitic elements of GaN HEMT devices should be accurately evaluated. This chapter reports the characterization of a GaN packaged power transistor using S-parameters. Because the transistor is packaged, a calibration technique is carried out using specific test fixtures designed on FR4 printed circuit board (PCB). The proposed method is suitable for a wide range of power devices.

According to [1], the finite-element analysis (FEA) is a method to estimate parasitic elements of packaged transistors. However, this method requires the knowledge of the internal transistor topology and other technological data that are not available from the manufacturer. Although, the impedance meter measurement is a well-known technique to determine parasitic elements of the device [2], it is difficult to separate different parasitic values especially if they are very low. The S-parameter measurements have shown their capability to extract the transistor parasitic elements as well as intrinsic small-signal equivalent circuit [3].

Fast switching performance of GaN power transistors is critically determined by the values of parasitic inductances and capacitances. Negative effects of these elements such as overvoltage, overcurrent, and oscillations occur during transitions [1]. Recent works used S-parameter measurements to extract the access inductances and capacitances of SiC packaged devices [4]. The authors show the capability of S-parameters to extract very low inductances and capacitances values. However, the parasitic inductances of new GaN power transistors packaging have values under the nanohenry and Miller capacitance under the picofarad. These elements still remain challenging to measure.

The access resistances play an important role in the high-frequency operation of GaN HEMT degradation [5], because they add charging and discharging delays during switching. Furthermore, the source and drain parasitic resistances are a major part of ON-state resistance. Therefore, these values must be known with a good precision to estimate conduction losses and they also must be well separated from channel resistance for accurate modeling. Several works are based on S-parameters to extract the access resistance values and their temperature dependence [6].

This chapter reports an experimental methodology to extract both intrinsic and extrinsic parasitic elements of a packaged GaN power transistor. For that, we have developed two experimental setups for the measurements of the GaN HEMT parasitic elements. The first experimental setup enables the extraction of the GaN HEMT extrinsic elements at the cold state. The second experimental setup is based on optimization algorithm and offers an automatic extraction of the intrinsic parameters of the DUT at multiple bias conditions. Furthermore, the developed experimental setups for extracting both the intrinsic and extrinsic parameters are used in the next chapter for investigating the impact of aging the GaN HEMT on the S-parameter characteristics of the DUT.

Moreover, to reach the best accuracy on the extraction of very low GaN HEMT parasitics, we have proposed a method based on S-parameter measurements and a specific calibration process using low-cost test fixtures.

After detailing the calibration procedure, measurements of access resistances and inductances as well as voltage-dependent capacitances are presented. The modeling of parasitic elements of GaN HEMT is performed using S-parameter simulation approach. The proposed method is suitable for a wide range of power devices. Furthermore, these results provide power circuit designers with a set of packaging parasitic elements to include for accurate design of power converters using GaN HEMT.

4.2. Small signal model of power GaN HEMT

Several small signal models were used for measuring the parasitic elements of the Si devices [7]. However, GaN HEMT devices shows different S-parameters characteristics due to the GaN device structure and physical properties.

In [8], An accurate small signal equivalent circuit model for power GaN HEMT at low frequency up to 200 MHz has been proposed. In this model, the parasitic elements were determined from S-parameters without the need for additional measurements or separate characterizations. Authors in [8] have demonstrated that the low frequency small signal topology is appropriate to describe the device S-parameter characteristics of power GaN HEMT up to 200 MHz.

The parasitic elements of the GaN HEMT equivalent model at low frequency ($f \leq 200$ MHz) are presented in [9] and shown in **Fig. 4.1**. The equivalent circuit can be divided into intrinsic part and extrinsic part. In the circuit, C_{pg} and C_{pd} parasitic capacitances are due to the pad connections, while C_{gs} , C_{gd} and C_{ds} respectively account for inter-electrode and cross over capacitances between gate, source and drain. L_g , L_d and L_s represent parasitic inductances due to the contacts of gate, drain and source.

Therefore, three additional resistances R_g , R_s and R_d are added into intrinsic elements for consideration of the gate leakage current. The parasitic gate, source, and drain resistances and inductances are assumed to be independent of the biasing conditions. Thus, they can be determined from the measurement under cold condition.

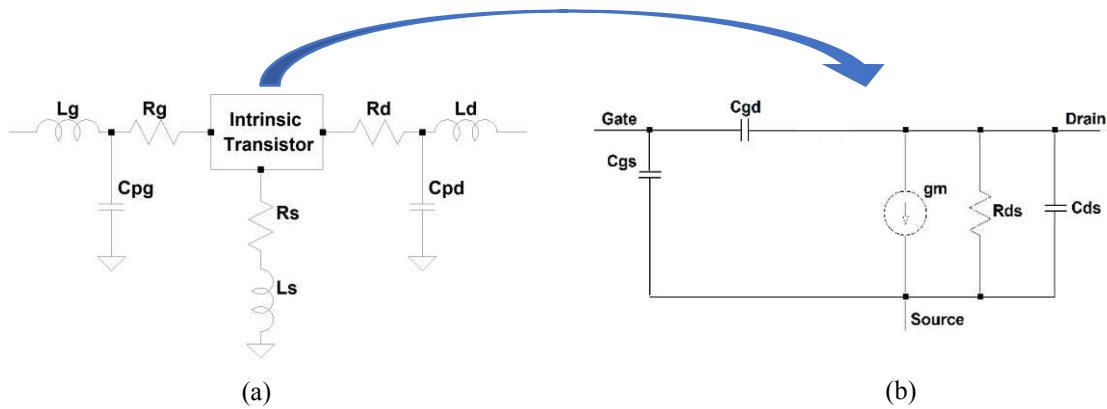


Fig. 4.1: GaN HEMT package [9]: (a) extrinsic parameters, (b) intrinsic parameters.

The proposed low frequency model is used in [10] for extracting the parasitic inductances of the power SiC MOSFET at $f \leq 200\text{MHz}$. Moreover, authors in [10] suggests that the proposed low frequency small signal model is suitable for characterizing accurate extraction of high-speed power devices parasitic inductances. In this chapter, we have used the proposed small signal topology at low frequencies in the range of $100\text{ kHz} \leq f \leq 200\text{ MHz}$ for extracting both the extrinsic and intrinsic parameters of the power GaN HEMT.

4.3. S-parameters experimental setup at the cold state

The Keysight VNA (E5080B) [11] was used to experimentally characterize the S-parameters of the GaN power HEMT. The studied frequency interval sweeps between 100 kHz and 200 MHz by a step of 100 kHz. This frequency range is widely used in various power converter applications [12].

Fig. 4.2 (a) shows the experimental setup for GaN HEMT. Before the S-parameters measurement, several preparation steps are required.

The first requirement is the development of a custom test fixture to ensure reliable and low inductance connections between the device terminals and VNA [13]. **Fig. 4.2 (b)** shows the designed printed circuit board (PCB) test fixture for interfacing the VNA to the DUT. Two 50 Ω SMA female adaptors are used.

For a good connectivity, the DUT is soldered to the test fixture. We have also designed a test fixture for TO-220 style devices (see **Fig. 4.2 (c)**), but the results were non-reproducible due to the non-stability of the connection between the TO-220 connector and the DUT pads.

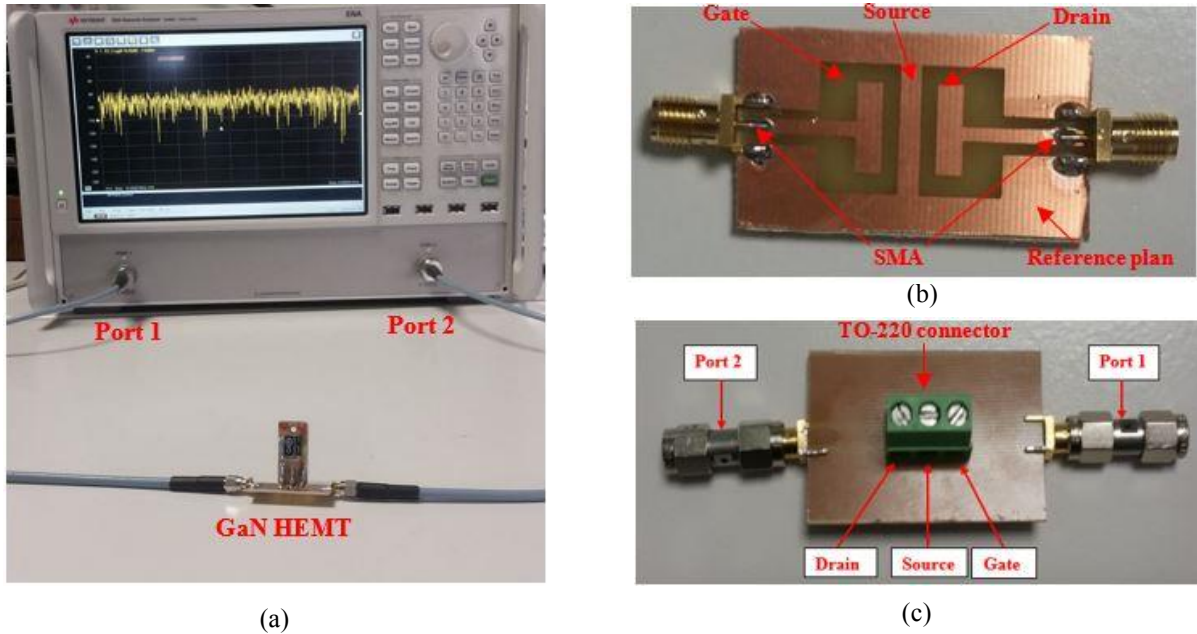


Fig. 4.2: (a) VNA measurement setup for GaN HEMT; (b) DUT test fixture; (c) Test fixture using TO-220 connector.

The second requirement is the VNA calibration. Through calibration, the VNA performs an error correction in the VNA itself and the test cables, adapters, and fixture that are between the VNA and the DUT [14]. The full two ports SOLT calibration [15] (Short-Open-Load-Through) was performed using the designed calibration Kit. This calibration enables the exclusion of the influence beyond the DUT from measurements.

4.4. Measurement verification

In the following, the verification of both the measurement repeatability and the calibration is performed in order to ensure that the S-parameter experimental setup is operational.

4.4.1. Measurement repeatability

Degradation of the VNA calibration over time is known as drift [16]. The validation of the S-parameter measurements repeatability aims to establish confidence with the user that the methods are fit for their intended purposes. **Fig. 4.3** shows the GaN HEMT Z_{11} coefficient before and after 24 h VNA measurement session. The closeness of the traces shown in this figure indicates the absence of short-term drift in the measurement setup, and thus the repeatability of the S-parameter characterizations at the cold state using the VNA.

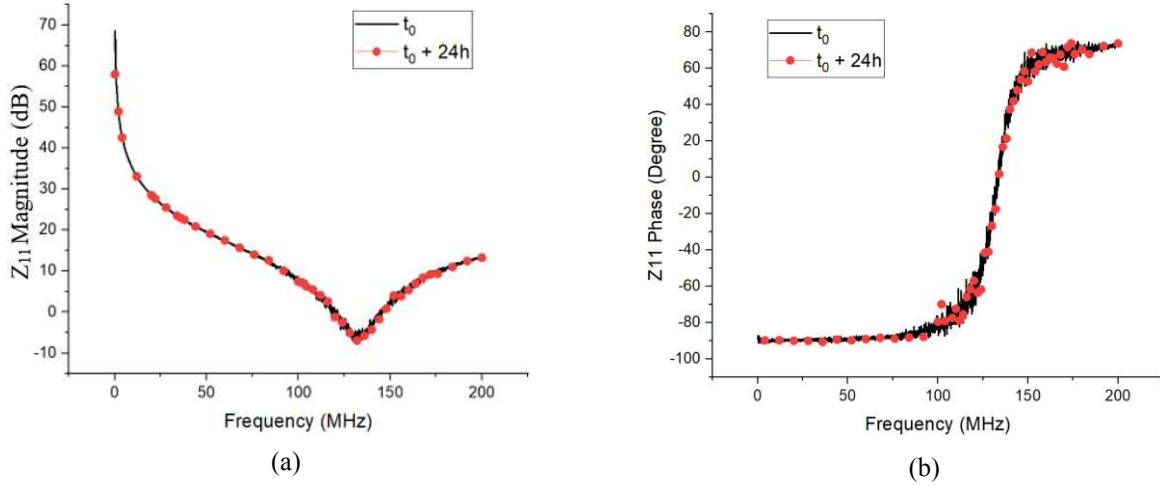


Fig. 4.3: Measured GaN HEMT Z_{11} coefficient before and after 24 hours VNA measurement session: (a) Z_{11} Magnitude and (b) Z_{11} Phase.

4.4.2. Passive component test

In order to verify the accuracy of the developed S parameter measurements, a verification test is performed using passive components: resistance of 3.25 k Ω , capacitance of 22.72 pF, inductance 56.68 μ H. The values of the resistance, capacitance and inductance are pre-measured by a the HP4192A impedance meter at 1 MHz [17]. **Table 4.1** shows a comparison between impedance meter and S-parameter measurements of the tested passive component at 1 MHz. The measured value of the tested passive component using S-parameters is closed to the measured value using the impedance analyser at 1 MHz, with a small shift. The error between the impedance meter and S-parameter measurements is due to the parasitic elements of the passive component model, which are accurately considered using S-parameter measurements [18].

Table 4.1: Comparison between impedance meter and S-parameter measurements of the tested passive component at 1 MHz: capacitance, inductance and resistance.

	Impedance meter	S-parameter	Error
Capacitance	22.72 pF	18.46 pF	18,75 %
Inductance	56.68 μ H	57.86 μ H	2.08 %
Resistance	3.25 k Ω	3.264 k Ω	0.43 %

According to [19], the S-parameters measured by a vector network analyzer (VNA) have shown their capability to extract the parasitic elements of passive components with high accuracy as well as intrinsic small-signal equivalent circuit. Compared to the impedance meter measurement method, which is not able to separate different parasitic values especially if they are very low [2]. The accuracy and good results of the S-parameters method when applied on passive components provide a good way to research the parasitic elements of power devices in order to investigate their impact on power converter application. In the next section, we apply the S-parameters method on power transistors, such as: GaN HEMT and SiC MOSFT.

As shown in this section, we have verified the measurement repeatability before and after 24 h of a VNA measurement session. Also, we have compared the value of passive component obtained from S-parameters measurements using the VNA and we compare it to those obtained from the impedance meter, including: resistor, capacitor and inductor. The results show a good convergence of measurements. In the next section, the extraction methodology of the power GaN HEMT parasitic elements is presented.

4.5. The proposed extraction methodology

The proposed methodology for extracting both the small signal model of power GaN HEMTs is shown in **Fig. 4.4**, which is composed of eight steps. The model extraction process is composed of seven steps:

Step 1: Parasitic parameters extraction at the cold state for $V_{DS} = 0$ V, $V_{GS} = 0$ V and $\forall f \in [100\text{KHz}, 200\text{MHz}]$. This step enables to define the boundaries of both the intrinsic capacitances (C_{GS} , C_{GD} , C_{DS}) and the extrinsic elements (C_{PD} , C_{PD} R_G , R_S , R_D , L_S , L_D , L_G) before launching the optimizations.

Step 2: Using the AMCAD bench, the output characteristic (I_{DS} - V_{DS}) linked with a set of S parameters are measured for $V_{DS} \in [0V, 4V]$ and $f \in [100\text{KHz}, 200\text{MHz}]$. $V_{DS} \in [0V, 4V]$ is selected in order to not exceed the allowed maximum current of the bias Tee ($I_{DS(\text{Max})} = 2$ A).

Step 3: The linear modeling process start by chosen one quiescent point Q_P from the measured output characteristic (I_{DS} - V_{DS}) linked with a set of S parameters. The selected Q_P point is chosen in order to get the linear model close to the bias point that will be used in the power switching application.

Step 4: The fourth step is to optimize the extracted model parameters. The Annealing algorithm [20] is chosen for the optimization of fitting. During the optimization process, a comparison between the model and the measurement is performed. If the convergence is not good, a new set of extrinsic and intrinsic parameters is provided, until measurement and model are consistent convergence.

Step 5: After the optimization process, the compact model of the DUT at one Q_P point of the power switching application is extracted. The extracted model parameters must respect two criteria:

- The value should be physical (no negative value);
- Intrinsic parameters are independent of the frequency. These intrinsic and extrinsic parameters should be close to the average values that have been found into the cold state in step 1 of this methodology.

Step 6: In order to validate both the extracted extrinsic and intrinsic model, an S-parameters simulation and verification are performed using S-parameters simulator.

Step 7: The selection of one quiescent point Q_P provides a higher model extraction speed, but can lead to unrealistic determination of extrinsic and intrinsic model parameters. The selection of several points forces the solution to be more realistic. The same optimization can be launched simultaneously for all the points selected.

Step 8: Once the linear model has been extracted, the nonlinear intrinsic parameters $C_{GS}(V_{GS})$, $C_{GD}(V_{GD})$ and $C_{DS}(V_{DS})$ have been extracted. The Multi-bias extraction step enables to visualize the intrinsic parameters in multi bias conditions.

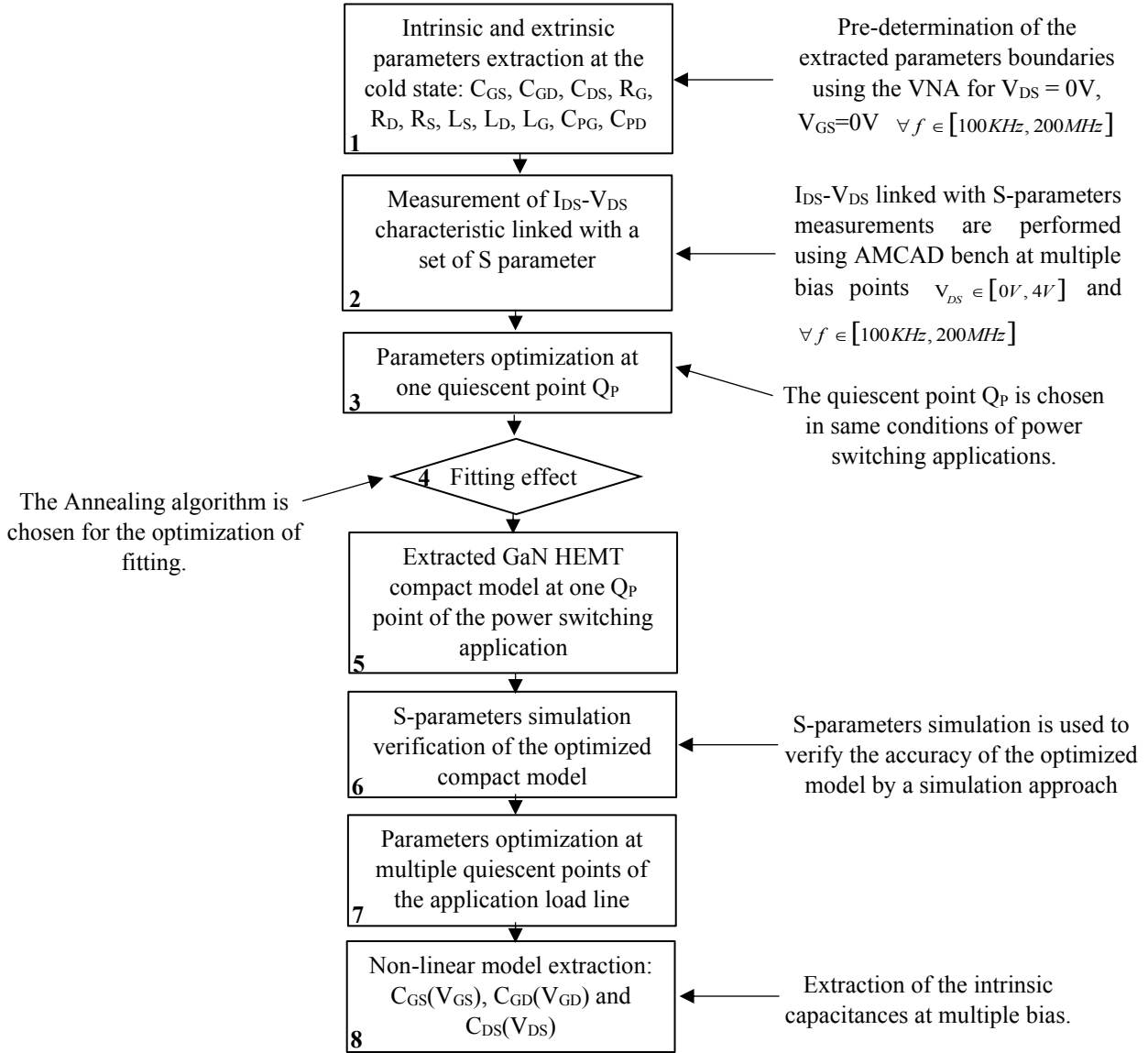


Fig. 4.4. GaN HEMT small signal model extraction methodology.

4.6. GaN HEMT S-parameters extraction

In this section, we apply the cold state ($V_{DS} = 0V$ and $V_{GS} = 0V$) S-parameters method on power GaN transistor after verification of this technic on both the calibration kit and passive components. For that, we have selected a fresh 650 V / 30 A GaN HEMT (GaN Systems GS66508P) [21]. **Fig. 4.5** shows the tested GaN HEMT mounted on the test fixture. The DUT is soldered to an Aluminium PCB, allowing more efficient conduction of heat compared to fibreglass PCB.

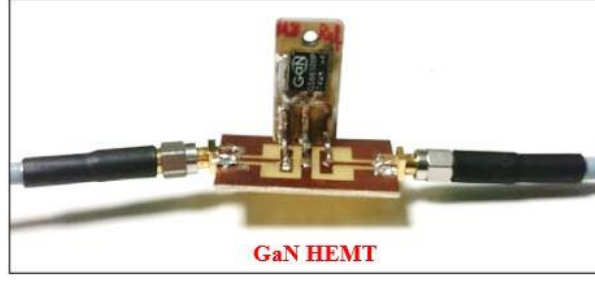


Fig. 4.5: Tested 650 V / 30 A GaN HEMT.

The VNA measurement yields S-parameters instead of Z-parameters. The conversion to Z parameters is carried out by (4.1)-(4.4) [22]. Where Z_0 is the characteristic impedance which is equal to 50Ω :

$$Z_{11}(\Omega) = \left[\frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \right] \cdot Z_0 \quad (4.1)$$

$$Z_{12}(\Omega) = \left[\frac{2S_{12}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \right] \cdot Z_0 \quad (4.2)$$

$$Z_{21}(\Omega) = \left[\frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \right] \cdot Z_0 \quad (4.3)$$

$$Z_{22}(\Omega) = \left[\frac{(1 + S_{22})(1 - S_{11}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \right] \cdot Z_0 \quad (4.4)$$

The magnitude and phases of the Z parameters are defined by (5) [23], where Z_{Re} is real part and Z_{Im} is the imaginary part of the Z parameter.

$$Z(\Omega) = \sqrt{Z_{Re}^2 + Z_{Im}^2} \quad (4.5)$$

$$Z(dB) = 20 \cdot \log(Z(\Omega)) \quad (4.6)$$

$$Z(\varphi) = \arctan\left(\frac{Z_{Im}}{Z_{Re}}\right) \quad (4.7)$$

The frequency response of the tested power GaN HEMT is shown in **Fig. 4.6**. At high frequencies ($>$ SRF) the GaN HEMT has an inductive behaviour [24]. At the SRF frequency, the DUT has a resistive behaviour. For low frequencies ($<$ SRF), the DUT has a capacitive behaviour [25]. The extracted self-resonance frequency of each parameter Z_{11} , Z_{12} , Z_{21} and Z_{22} are shown in **Table 4.2**. The non-equal SRF between Z_{11} and Z_{22} , is due to the non-symmetrical parasitic element between both the source-gate side and the drain-gate side [26].

Parasitic elements of the GaN HEMT are determined from Z-parameters plot computed from the S-parameters. The extracting of the parasitic inductances, resistances and capacitances of the GaN HEMT are presented in the next section. We start by extracting the inductance at high frequency ($= 200$ MHz). Then, we extract the parasitic resistance at the SRF frequency. We finish by extracting the parasitic capacitance at low frequency ($= 1$ MHz).

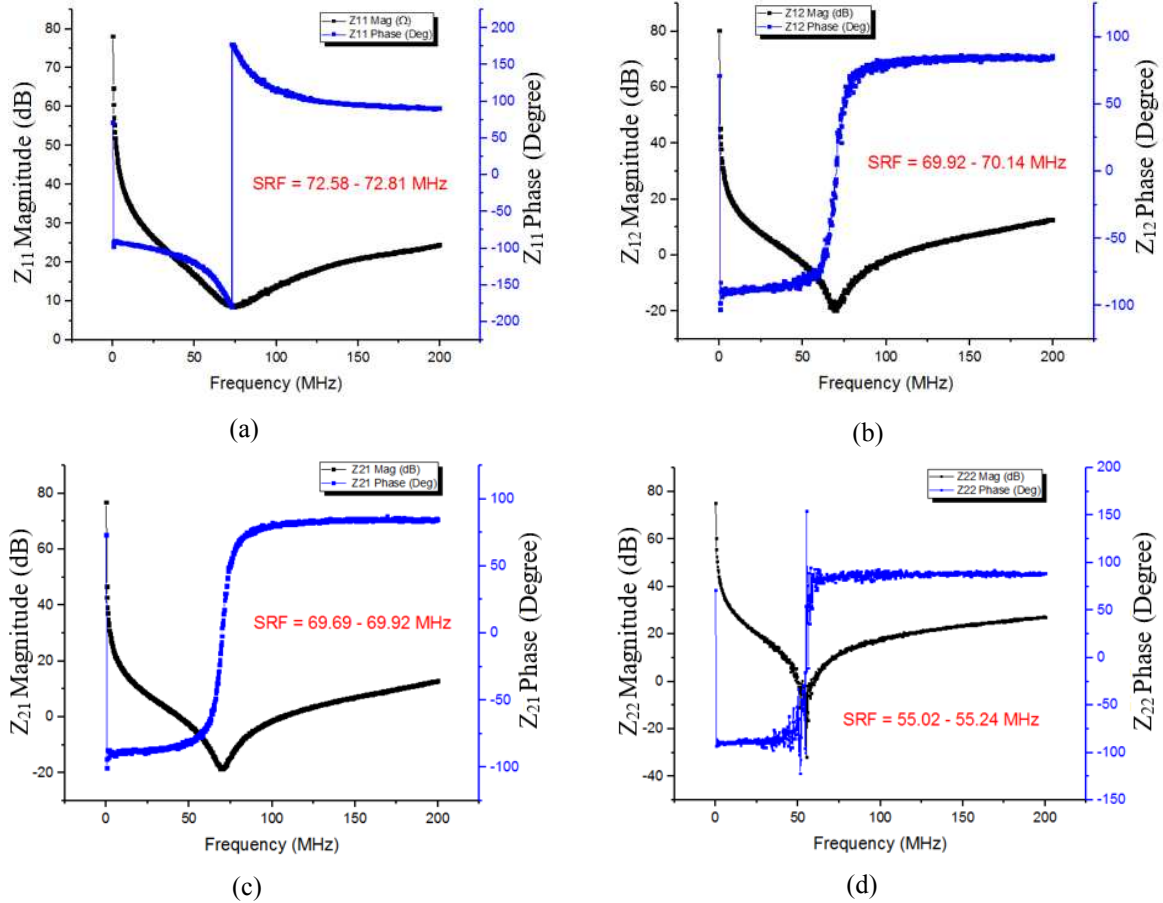


Fig. 4.6: Frequency responses of the tested power GaN HEMT for $100 \text{ kHz} < f < 200 \text{ MHz}$: (a) Z_{11} , (b) Z_{12} , (c) Z_{21} and (d) Z_{22} Magnitudes and phases.

Table 4.2: Self resonance frequency of the tested power GaN HEMT.

Z-parameters	Z_{11}	Z_{12}	Z_{21}	Z_{22}
SRF	72.58 - 72.81 MHz	69.92 - 70.14 MHz	69.69 - 69.92 MHz	55.02 - 55.24 MHz

4.6.1. Parasitic inductances

For the extraction of the parasitic inductances of GaN HEMT, we used the simplified two-port network representation of the GaN HEMT equivalent circuit for inductance extraction at high frequency ($> \text{SRF}$), as shown in **Fig. 4.7**. At high frequency, the inductor impedance dominates while the capacitances and resistances can be neglected [27].

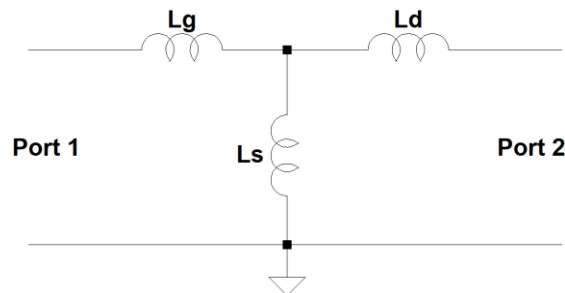


Fig. 4.7: Equivalent circuit of the DUT at high frequency [27].

The inductance effect of the DUT at high frequency for the two-port network Z-parameters are defined as follows [28]:

$$Z_{11(\text{high})} = \left. \frac{V_1}{I_1} \right|_{I_2=0} = X_{L_G} + X_{L_S} = 2\pi f \cdot (L_G + L_S) \quad (4.8)$$

$$Z_{12(\text{high})} = \left. \frac{V_1}{I_2} \right|_{I_1=0} = X_{L_S} = 2\pi f \cdot L_S \quad (4.9)$$

$$Z_{21(\text{high})} = \left. \frac{V_2}{I_1} \right|_{I_2=0} = X_{L_S} = 2\pi f \cdot L_S \quad (4.10)$$

$$Z_{22(\text{high})} = \left. \frac{V_2}{I_2} \right|_{I_1=0} = X_{L_D} + X_{L_S} = 2\pi f \cdot (L_D + L_S) \quad (4.11)$$

The extracted parasitic inductances of the tested GaN HEMT at 200 MHz are shown in **Fig. 4.8**: source inductance (L_S), gate inductance (L_G) and drain inductance (L_D). **Table 4.3** shows the measured parasitic inductances of GaN HEMT at high frequency 200 MHz. The low parasitic inductance L_S , L_G , L_D of the GaN HEMT enable best performance at high switching frequencies, which result in lower switching energy dissipation [29].

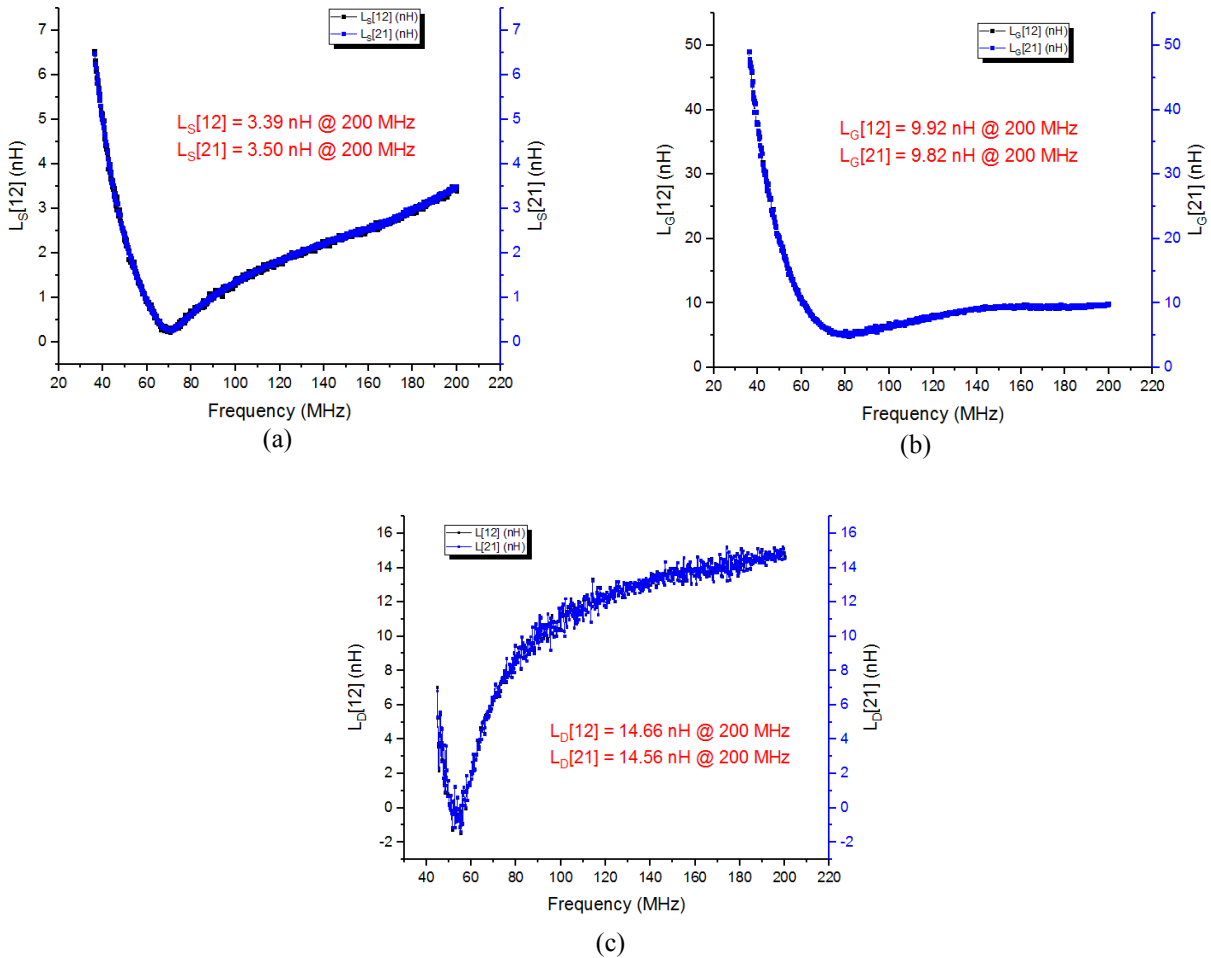


Fig. 4.8: Inductances extraction of the tested power GaN HEMT: (a) L_S , (b) L_G and (c) L_D frequency responses.

Table 4.3: GaN HEMT extracted parasitic inductances L_S , L_G and L_D at 200 MHz.

Inductances	L_S	L_G	L_D
GaN HEMT	3.44 nH @ 200 MHz	9.87H @ 200 MHz	14.66 nH @ 200 MHz

4.6.2. Intrinsic capacitances

For the extraction of the parasitic capacitances of GaN HEMT, we used the equivalent circuit of GaN HEMT at low frequency ($< \text{SRF}$) (See **Fig. 4.9**). At low frequency, the capacitor impedance dominates while the inductances and resistances can be neglected [30].

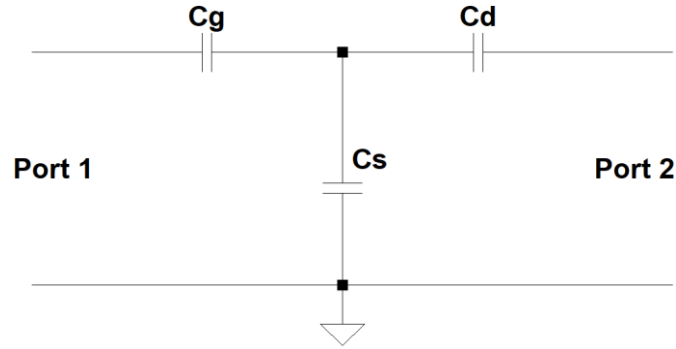


Fig. 4.9: Equivalent circuit of the DUT at low frequency using star connection [30]: C_G , C_S and C_D .

The capacitance effect of the GaN HEMT at low frequency for the two-port network Z-parameters are defined by [28]:

$$Z_{11(\text{low})} = \left. \frac{V_1}{I_1} \right|_{I_2=0} = X_{C_G} + X_{C_S} \quad (4.12)$$

$$Z_{12(\text{low})} = \left. \frac{V_1}{I_2} \right|_{I_1=0} = X_{C_S} \quad (4.13)$$

$$Z_{21(\text{low})} = \left. \frac{V_2}{I_1} \right|_{I_2=0} = X_{C_S} \quad (4.14)$$

$$Z_{22(\text{low})} = \left. \frac{V_2}{I_2} \right|_{I_1=0} = X_{C_D} + X_{C_S} \quad (4.15)$$

The conversion from star connection (**Fig. 4.9**) to delta connection (**Fig. 4.10**) enable to find the intrinsic capacitance C_{GS} , C_{GD} and C_{DS} . These capacitances are calculated by [31]:

$$X_{C_{GS}} = \frac{X_{C_G} \cdot X_{C_S} + X_{C_G} \cdot X_{C_D} + X_{C_S} \cdot X_{C_D}}{X_{C_D}} \quad (4.16)$$

$$X_{C_{GD}} = \frac{X_{C_G} \cdot X_{C_S} + X_{C_G} \cdot X_{C_D} + X_{C_S} \cdot X_{C_D}}{X_{C_S}} \quad (4.17)$$

$$X_{C_{DS}} = \frac{X_{C_G} \cdot X_{C_S} + X_{C_G} \cdot X_{C_D} + X_{C_S} \cdot X_{C_D}}{X_{C_G}} \quad (4.18)$$

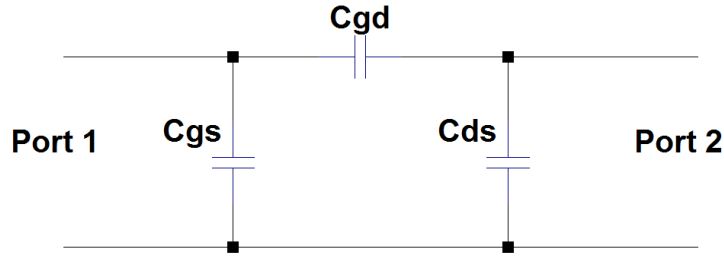
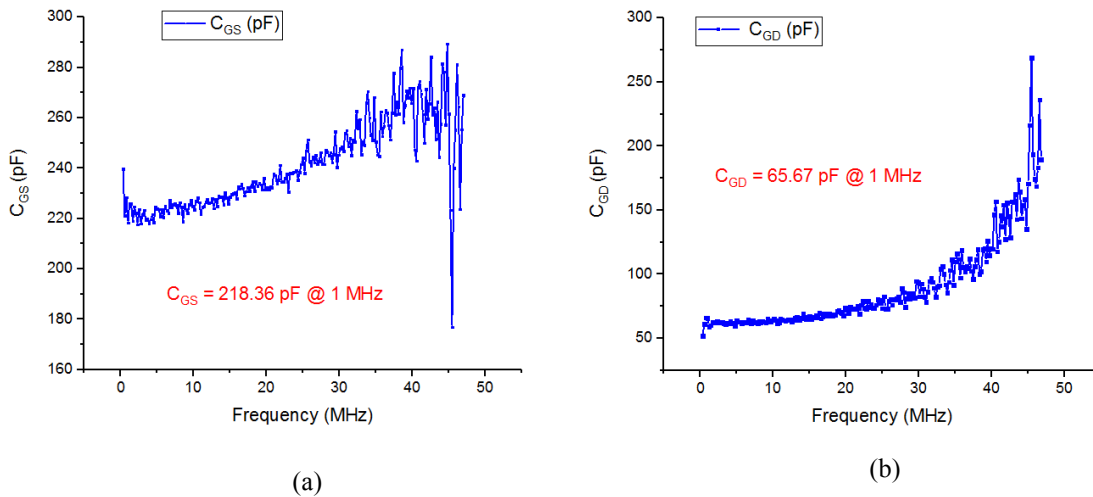
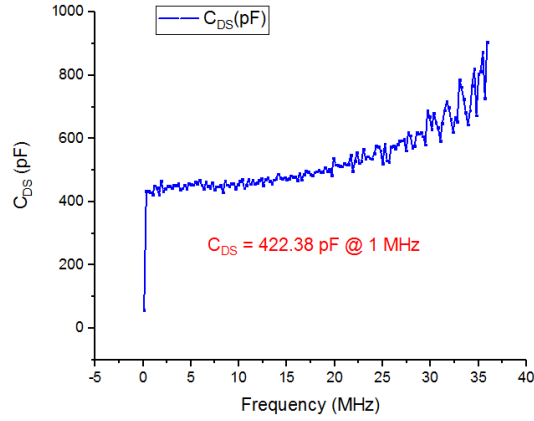


Fig. 4.10: Delta connection of the extracted capacitances [31]: C_{GS} , C_{GD} and C_{DS} .

The extracted parasitic capacitances of the GaN HEMT at 1 MHz are presented in **Fig. 4.11**: source capacitance (C_{GS}), gate capacitance (C_{GD}) and drain capacitance (C_{DS}). The measured C_{GS} is a combination of the intrinsic gate capacitance and the pad capacitance C_{PG} . Furthermore, the measured C_{DS} is a combination of the intrinsic drain capacitance and the pad capacitance C_{PD} . **Table 4.4** presents a comparison between the VNA and impedance analyzer measurements of the extracted parasitic capacitances at 1 MHz.

For the comparison, we used the same frequency of extracting the parasitic capacitances in literature [32], which is 1 MHz. Both the VNA and impedance analyzer measurements are performed at the cold state, which are $V_{GS} = 0$ V and $V_{DS} = 0$ V. The measurements with VNA are close to those performed using the impedance analyzer, with a mean error of 16.89 %. This error is due to the inability of the impedance analyzer measurement to separate different parasitic values especially if they are very low, which is the case of the GaN HEMT transistors [2]. However, S-parameters measured using a vector network analyzer (VNA), have shown their capability to extract the transistor parasitic capacitances [33].





(c)

Fig. 4.11: Capacitances extraction of the tested power GaN HEMT: (a) C_{GS} , (b) C_{GD} and C_{DS} frequency responses.

Table 4.4: GaN HEMT extracted parasitic capacitances C_{GS} , C_{GD} and C_{DS} at 1 MHz.

GaN HEMT Capacitances	C_{GS}	C_{GD}	C_{DS}
VNA measurements	218.36 pF	65.67 pF	422.38 pF
Impedance analyser measurements	236 pF	109.36 pF	436.6 pF
Error (%)	7.47 %	39.95 %	3.25 %

4.6.3. Parasitic resistances

For the extraction of the parasitic resistances of GaN HEMT, we used the equivalent circuit of the GaN HEMT at SRF frequency (See **Fig. 4.12**). At the SRF frequency in **Table 4.2**, the resistance impedance dominates while the inductances and capacitances can be neglected [34].

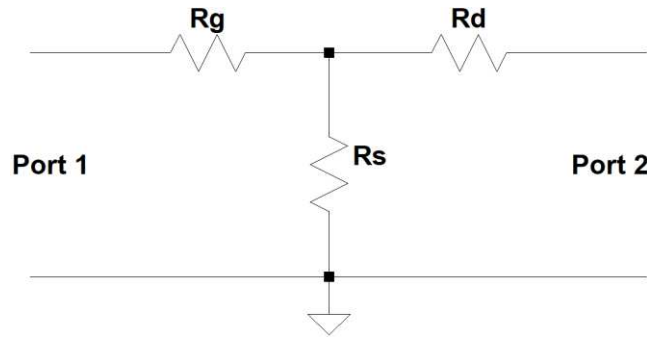


Fig. 4.12 : Equivalent circuit of the DUT at SRF frequency [34]: R_G , R_S , R_D .

The resistance effect of the GaN HEMT at SRF frequency for the two-port network Z-parameters are defined by [28]:

$$Z_{11(SRF)} = \left. \frac{V_1}{I_1} \right|_{I_2=0} = X_{R_G} + X_{R_S} = R_G + R_S \quad (4.19)$$

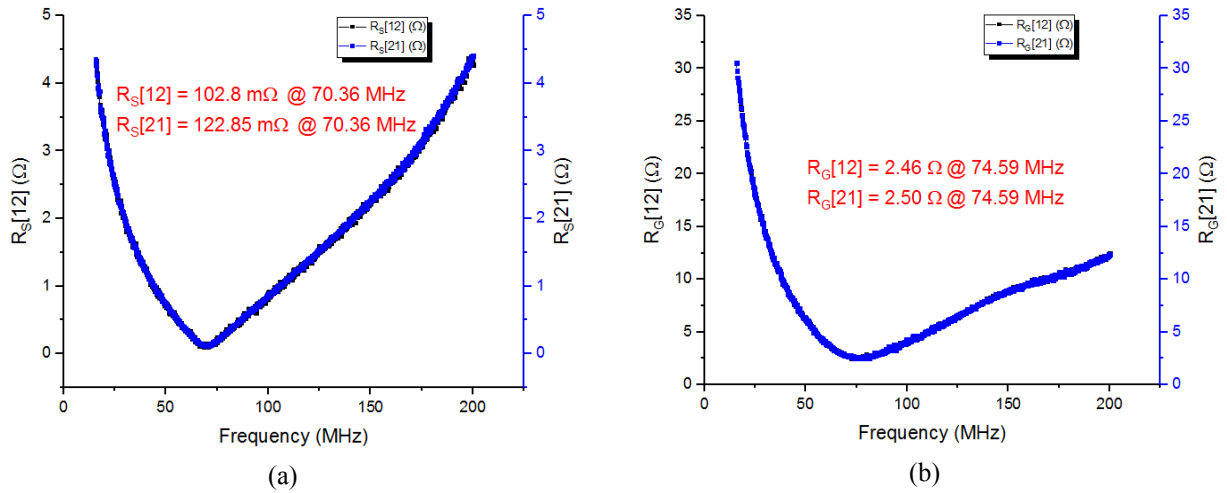
$$Z_{12(SRF)} = \left. \frac{V_1}{I_2} \right|_{I_1=0} = X_{R_S} = R_S \quad (4.20)$$

$$Z_{21(SRF)} = \left. \frac{V_2}{I_1} \right|_{I_2=0} = X_{R_S} = R_S \quad (4.21)$$

$$Z_{22(SRF)} = \left. \frac{V_2}{I_2} \right|_{I_1=0} = X_{R_D} + X_{R_S} = R_D + R_S \quad (4.22)$$

The extracted parasitic resistances of the GaN HEMT at the SRF frequency are shown in **Fig. 4.13**: source resistance (R_S), gate resistance (R_G) and drain resistance (R_D). **Table 4.5** presents the measured parasitic resistances of GaN HEMT at the corresponding SRF frequency of each parameter: R_S , R_G and R_D . The parasitic resistances R_D and R_S are connected in series with the internal channel resistance, which play a vital role in determining device conduction losses [35].

In general, the drain parasitic resistance R_D is much larger than the source parasitic resistance R_S , which is confirmed in [36]. The parasitic gate resistance R_G value has a significant impact on the switching transients for fast switching power converters [37]. It is shown in [38] that a higher gate resistance reduces the switching speed and consequently causes higher switching losses at the DUT.



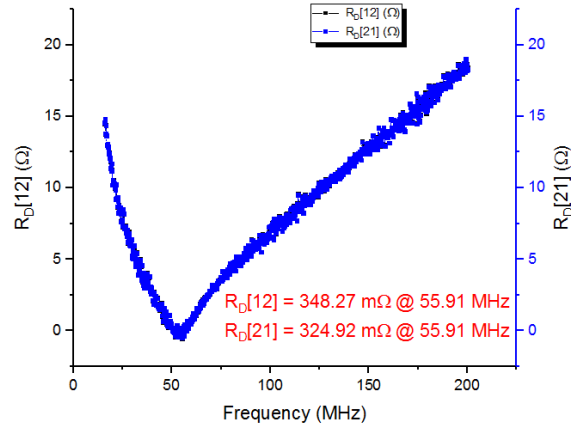


Fig. 4.13: Resistances extraction of the tested power GaN HEMT: (a) R_S , (b) R_G and (c) R_D frequency responses.

Table 4.5: GaN HEMT extracted parasitic resistances R_S , R_G and R_D at SRF frequency.

Parameters	R_S	R_G	R_D
GaN HEMT	112.82 mΩ @ 70.36 MHz	2.48 Ω @ 74.59 MHz	354.59 mΩ @ 55.91 MHz

In the next section, we have evaluated the accuracy of the used S-parameters extracting methodology for GaN HEMT by comparing the extracted parasitic parameters of a known DUT with those shown in the literature.

4.6.4. Measurement methodology verification

Authors in [39] have extracted the parasitic inductances, capacitances, and resistances of a SiC power MOSFET by measuring the S-parameters using a VNA and then convert them into Z-parameters. In order to evaluate the accuracy of our S-parameter characterization at the cold state, we have compared the extracting methodology with those presented in [39]. For that, we have selected a second generation of a 1200 V SiC (Wolfspeed's C2M0160120D). The selected Gen 2 SiC MOSFET is the same used in [39]. **Fig. 4.14** shows the tested 1200V SiC MOSFET mounted on the test fixture.



Fig. 4.14: Tested 1200 V SiC MOSFET

Table 4.7 shows a comparison between both the measurements and the literature of the extracted parasitic inductances, capacitance and resistances of the Gen 2 1200 V SiC MOSFET. The used frequency for extracting the parasitic inductances is not specified in [39]. We used

the higher frequency, which is 200 MHz. The extracting parasitic capacitances frequency is the same used in [39] which equals to 1 MHz. The parasitic resistances are extracted at SRF frequency. As observed the obtained measurements are close to those obtained in the literature. This shows the accuracy of the used S-parameters characterization for the GaN HEMT.

Table 4.6: Tested SiC MOSFET parasitic elements extraction results summarization.

Parasitic	Inductances (nH)			Capacitances (nF)			Resistances (Ω)		
	L_S	L_G	L_D	C_{GS}	C_{GD}	C_{DS}	R_G	R_S	R_D
Measurements	13.06	16.57	1.88	0.504	0.265	0.495	2.70	0.469	0.231
Literature [A9]	7.489	8.920	4.296	0.520	0.297	0.511	2.5	0.31	0.20

4.7. Multiple bias model extraction

Using the VNA we have de-embedded the parasitic elements of the GaN HEMT from the S-parameter measurements at the cold state ($V_{GS} = 0$ V, $V_{DS} = 0$ V). However, in power switching applications, the DUT is continuously switched from the off-state to the on-state and vice versa. During this operation, the DUT is subject to a high electric field.

Studies have shown that the S-parameters of the GaN HEMT are very sensitive to the applied electric field and the extracted parasitic parameters are dependent to the chosen bias point (V_{GS} , V_{DS}) [40-41]. Moreover, the GaN HEMTs are exposed to high electric field at the off-state in the power converter applications. For that, the measured S-parameters must take into account the effect of the electric field on the extraction of the device parasitic parameters.

To perform S-parameters measurements for power devices, this required extra tools and equipment [42-43], such as: power bias tees, process and control unit, drain and gate power modules, and non-linear vector network analyzers (NVNA).

In this section, we have extracted the linear model of the GaN HEMT power transistors for multiple bias points. The chosen bias points correspond to the application load line. **Fig. 4.15** shows the GaN HEMT load line on the I_{DS} - V_{DS} characteristic. The application load line goes through four bias points Q_{P1} , Q_{P2} , Q_{P3} and Q_{P4} as presented in **Table 4.8**.

Table 4.7: Load line bias points Q_{P1} , Q_{P2} , Q_{P3} and Q_{P4} .

Bias points	I_{DS}	V_{DS}	V_{GS}
Q_{P1}	13.88 μ A	1.052 V	0 V
Q_{P2}	0.48 A	0.879 V	2 V
Q_{P3}	1.786 A	0.431 V	3 V
Q_{P4}	1.842 A	0.414 V	6 V

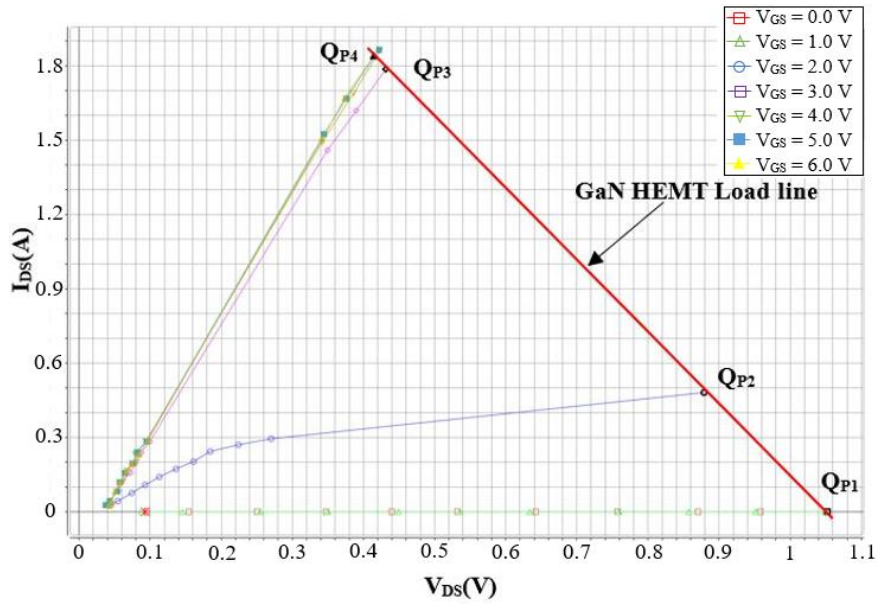


Fig. 4.15: GaN HEMT load line I_{DS} - V_{DS} characteristic.

4.7.1. Multiple bias experiment setup

The multiple bias experimental S-parameters bench is shown in Fig. 4.16, which includes: vector network analyzer, AMCAD bench, data capture and analysis computer, gate and drain bias T, gate and drain probes, test fixture. The small-signal S-parameter measurements were performed under continuous waveform (CW) operation at room temperature. Calculated S-parameters were measured at various frequencies starting from 100 kHz to 200 MHz by a step of 100 kHz.

The selected frequencies are widely used in power switching application. External bias tees were used with high drain current capability in the range of 2 A [44]. Bias conditions were set by the internal DC-voltage sources of the AMCAD bench. The Keysight E5080A ENA was used to measure the S-parameters [45]. VNA calibration of S-parameter measurements was carried out applying the SOLT technique [46], using a Keysight 85032F type N calibration kit which included open, short, thru circuits and a 50 Ω load.

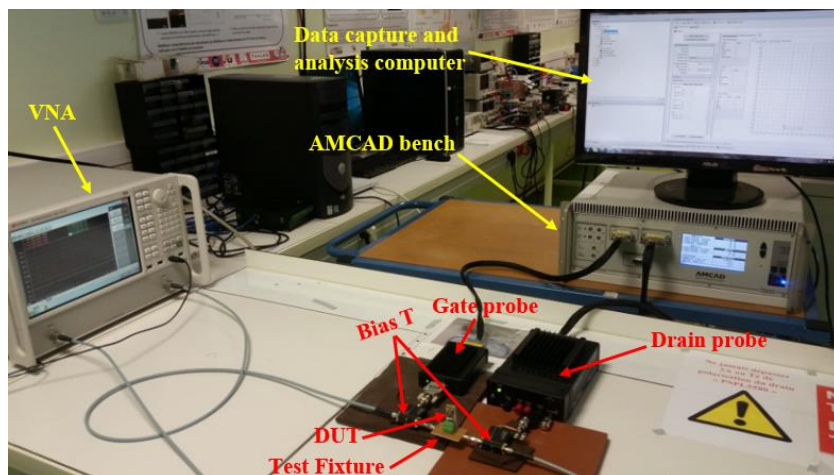


Fig. 4.16: Multiple bias S-parameters bench.

4.7.2. Linear model extraction methodology

The model adopted in this study corresponds to the conventional small-signal equivalent circuit of a field effect transistor in the saturated zone. **Fig. 4.17** shows the conventional small-signal equivalent circuit model for HEMTs [47], which can be partitioned into two parts: extrinsic and intrinsic parameters. The extrinsic elements L_G , R_G , C_{PG} , L_S , R_S , R_D , L_D , C_{PD} are independent of the biasing condition [48]. The intrinsic elements C_{GS} , C_{GD} , C_{DS} and are bias dependent [49]. The various components in the model are defined in the following list [50]: C_{PG} : gate pad capacitance, C_{PD} : drain pad capacitance, L_G : gate inductance, L_D : drain inductance, L_S : source inductance, R_G : gate resistance, R_D : drain to channel resistance, R_S : source to channel resistance.

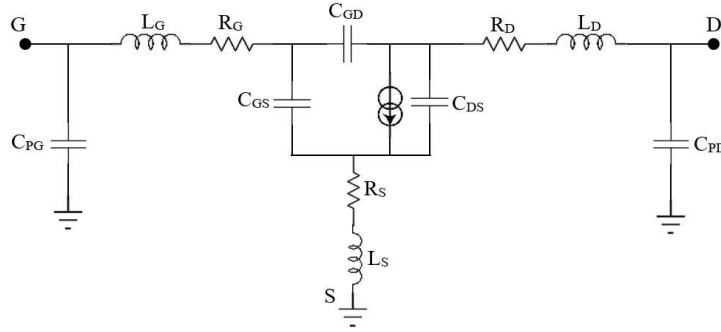


Fig. 4.17: Small signal equivalent circuit model of GaN HEMTs [47].

The Annealing algorithm [51] is chosen for the optimization of fitting. During the optimization process, a comparison between the model and the measurement is performed. If the convergence is not good, a new set of extrinsic and intrinsic parameters is provided, until measurement and model are consistent convergent. The model optimization required the specification of the parameter boundaries at the cold state for $V_{DS} = 0$ V, $V_{GS} = 0$ V. The GaN HEMT intrinsic and extrinsic parameters $\forall f \in [100\text{KHz}, 200\text{MHz}]$ are calculated in section 4.6.

Table 4.9 shows the mean value of the linear model parameters at multiple quiescent points: Q_{P1} , Q_{P2} , Q_{P3} and Q_{P4} of the GaN HEMT. For a good convergence of the extracted linear model with measurement, the value of R_D , R_G , R_S , L_D , L_S , L_G , C_{GS} , C_{GD} , C_{DS} , C_{PD} and C_{PG} are specified from the cold state parameters extracting in the previous section. The Annealing algorithm is used for the extraction of the linear model.

Table 4.8: linear model parameters of the GaN HEMT at multiple quiescent points: Q_{P1} , Q_{P2} , Q_{P3} and Q_{P4} .

Parameters	R_D	R_G	R_S	L_D	L_S	L_G
Optimized value	54.332 m Ω	723.37 m Ω	9.48 m Ω	8.068 Nh	3.17 nH	382.72 pH
Parameters	C_{PD}	C_{PG}	C_{GS}	C_{GD}	C_{DS}	
Optimized value	28.03 pF	18.549 pF	353.39 pF	12.815 pF	74.045 pF	

After extracting the GaN HEMT linear model parameters at multiple quiescent voltages, we have completed in the next section the developed model by extracting the non-linear capacitance characteristics of the GaN HEMT.

4.7.3. Non-linear intrinsic capacitance extraction

The S-parameter characterization is an accurate technique to extract the parasitic capacitances for power modules and eliminate the uncertainty and inaccuracy associated with the impedance meter measurement approach [52]. In this section, we have extracted the C_{GS} capacitance using multibias S-parameter measurements.

Fig. 4.18 shows the extracted C_{GS} at various bias points: $V_{DS} = 0$ V and V_{GS} start from 0 V to 7 V with a step of 0.1 V. As shown in this figure, we have obtained similar curves of the p-GaN HEMT that have been found in chapter 3 using C-V impedance meter.

The lower value obtained using S-parameters compared to impedance meter are due the C_{PG} and C_{PD} capacitances, which are not taken into account when using the impedance meter. This makes the measurement of parasitic capacitance using S-parameters highly accurate compared to the impedance meter.

According to the literature, the one-port configuration with shorted terminal using the impedance meter is no longer practical for the power module extraction due to the more complex structure with more parasitic capacitances [53]. Therefore, two-port extraction using S-parameters is the ideal method for power modules measurement.

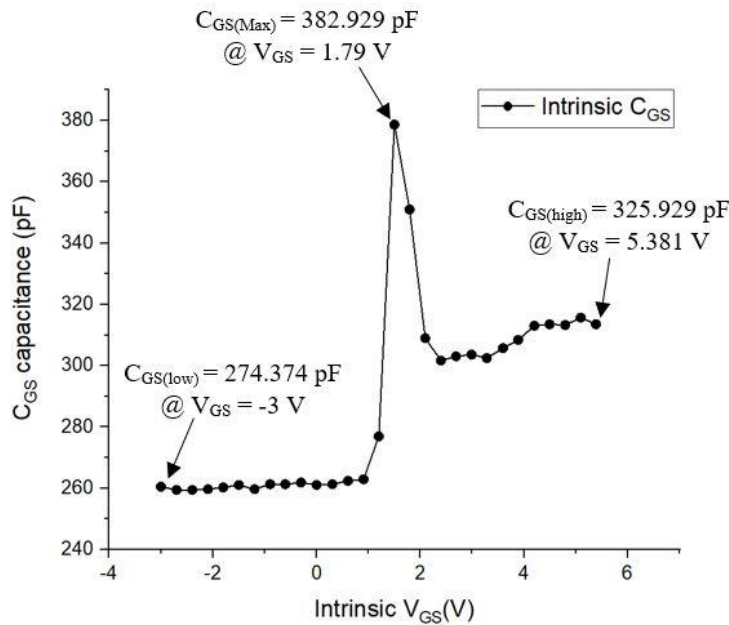


Fig. 4.18: Evolution of GaN HEMT C_{GS} intrinsic capacitance.

4.8. S-parameter modelling and simulation

To validate the extracted linear model of the tested GaN HEMT, we have simulated the equivalent circuit in frequency domain using an S-parameters circuit simulator. We have first built a small-signal equivalent circuit of a power GaN HEMT with a set of predefined parasitic inductance, capacitance, and resistance values. **Fig. 4.19** shows the simulated power GaN equivalent circuit with extracted parameters given in **Table 4.9**. The GaN HEMT circuit setup

is biased at Q_{P4} bias point, where $V_{GS} = 6$ V, $V_{DS} = 0.414$ V. The frequency domain simulation is carried out in the frequency range of 100 kHz to 200 MHz. We then run the frequency domain simulation to generate a set of S-parameters. Finally, we use the proposed approach to extract the parasitic values from these simulated S-parameters data. We then compare the extracted component values with the original predefined values to validate our derived mathematical formulas and extraction methodology.

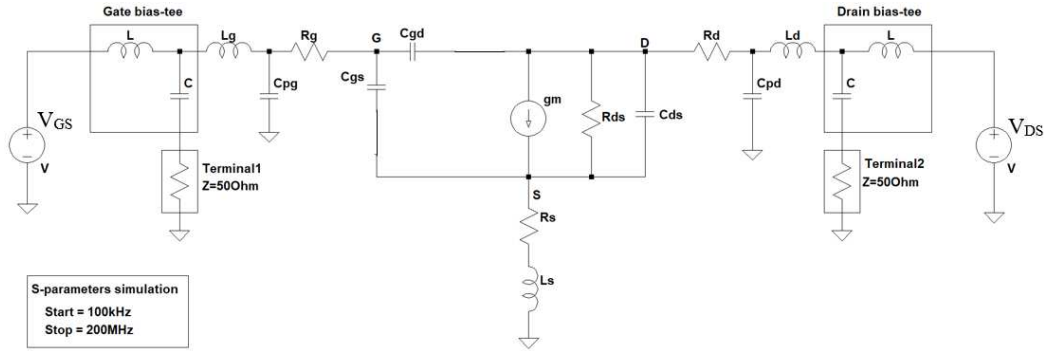


Fig. 4.19: S-parameter simulation setup at Q_{P4} bias point.

The comparison between the measured and optimized S-parameters using Annealing algorithm are shown in **Fig. 4.20** for S_{11} and S_{22} parameters and in **Fig. 4.21** for S_{12} and S_{21} parameters. The blue dashed line corresponds to the optimized S-parameters and the black line corresponds to the measured S-parameters. As can be observed, the optimized GaN HEMT model shows good convergence with measurement.

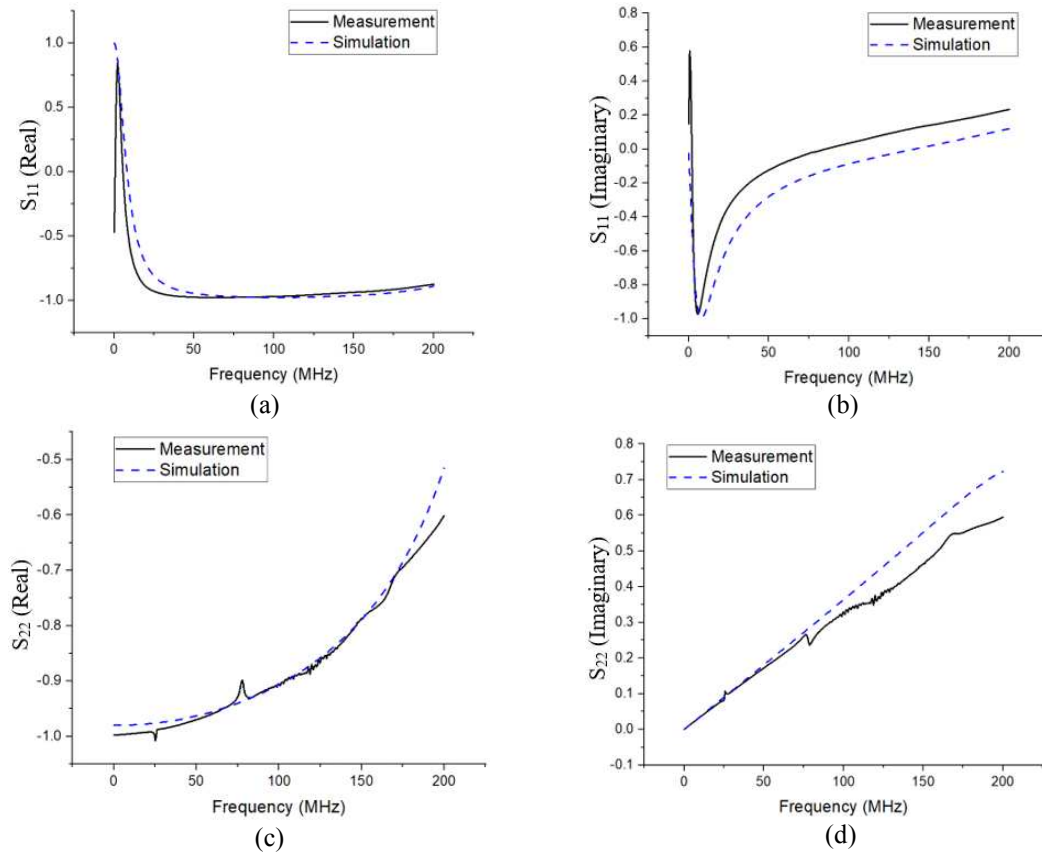


Fig. 4.20: Optimized S_{11} and S_{22} parameters for the tested GaN HEMT at Q_{P4} bias point: (a) S_{11} Real, (b) S_{11} imaginary, (c) S_{22} Real, (d) S_{22} imaginary.

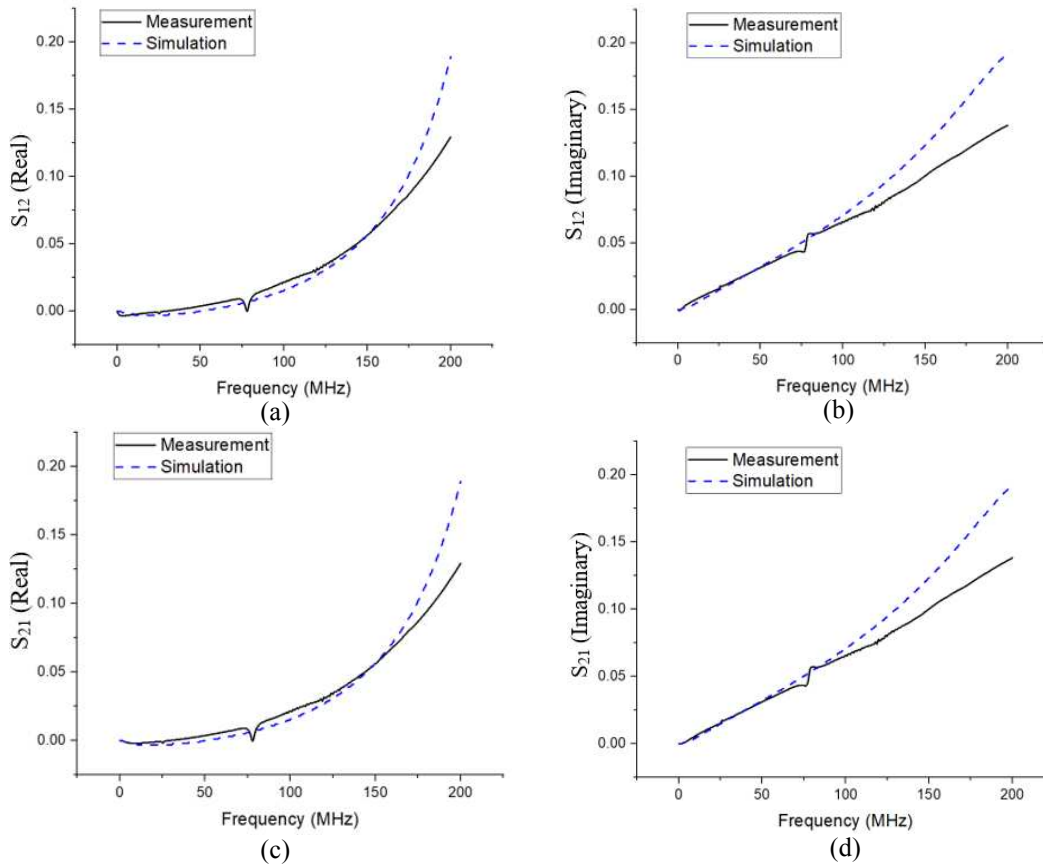


Fig. 4.21: Optimized S_{12} and S_{21} parameters for the tested GaN HEMT at Q_{P4} bias point: (a) S_{12} Real, (b) S_{12} imaginary, (c) S_{21} Real, (d) S_{21} imaginary.

From the S-parameters plots in **Fig. 4.20** and **Fig. 4.21**, we extract the parasitic component values following steps given of the extraction methodology described in section 4.5. **Table 4.10** summarizes the extracted values in comparison with the given values in the original circuit. It is noted that the extracted inductances, capacitances and resistances are reasonably accurate with the difference less than 10.61 %, giving us sufficient confidence with our proposed extraction method.

Table 4.9: Comparison between measured and simulated extracted parasitic elements of the GaN HEMT at Q_{P4} bias point.

Parameters	Measurement	Simulation	Error (%)
L_S (nH)	3.27	3.12	4.58
L_G (nH)	120.34	78.76	34.55
L_D (nH)	10.61	12.57	18.47
R_S (m Ω)	11.82	12.59	8.29
R_G (m Ω)	634.37	587.76	7.34
R_D (m Ω)	72.82	86.59	18.90
C_{GS} (pF)	317.36	318.52	0.42
C_{GD} (pF)	17.67	15.85	10.18
C_{DS} (pF)	103.38	102.43	0.91
C_{PG} (pF)	21.09	19.13	9.29
C_{PD} (pF)	30.957	29.764	3.85

4.9. Conclusion

In this chapter, an accurate methodology based on an accurate S-parameters calibration procedure is proposed to determine parasitic resistances, inductances, and capacitances of a packaged GaN power transistor. Two experimental setups have developed for the measurements of the GaN HEMT parasitic elements. The first one enables the extraction of the GaN HEMT extrinsic elements at the cold state. The second experimental setup is based on optimization algorithm and offers an automatic extraction of the intrinsic parameters of the DUT at multiple bias conditions. The obtained results show the possibility to extract very low device parasitics which may influence switching mechanisms in power converters. Good agreement is achieved between extracted values and technical data provided in the literature. Moreover, modeling equations are proposed for the nonlinear model parameters. The proposed method has the capability to be applied to any packaged GaN power transistor fabricated by different manufacturers. In this context, this method was already applied to extract SiC MOSFET parasitic elements. Furthermore, the method offers the possibility to extend the characterization to devices that have two terminals, such as: commercial inductances, capacitances and resistances. The characterization results and modeling approach presented in this chapter will be used in the next chapter to study the effect of aging the parasitic elements of GaN packaged power transistor on the efficiency and the design of power converter.

4.10. References

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Chapter 5: Aging of the GaN HEMT under safe operational conditions

5.1. Introduction

The attention of academics and industrials on reliability of GaN HEMT is accelerated by the impressive growth of GaN HEMTs market, due to their high superior performances compared to those of Silicon power transistors. Their applications are in various domains, such as green energy and RF engineering.

To validate the robustness of power GaN HEMTs transistors, JEDEC standardized tests for Si power transistors are used [1]. However, the standardized tests for Si are not enough to guarantee the robustness of GaN transistors when they are used in power converter applications, because the reliability of GaN under switching operation is different from that of Si transistors [2]. Moreover, running power GaN HEMTs under accelerated conditions would cause many non-GaN failures.

In the literature, the reliability of GaN HEMTs has been improved. Reference [3] classifies the degradation modes of GaN HEMT in switching mode DC power converter into three classes: on-state, off-state and semi-off state. According to [4], one of the major disadvantages limiting the reliability of GaN HEMTs for switching power applications is hot electron effects that occurs during the switching state. In [5], this degradation result in decreased DC and RF performance.

According to [6], it is important to study the reliability of GaN HEMT for power conversion circuits. This paper presents a developed reliability methodology under operational switching conditions. The proposed aging switching bench presents high power efficiency. The effects of aging GaN HEMT on a power converter application are studied by SPICE simulation approach.

In this chapter, we studied the effects of aging power GaN HEMT under switching conditions at both high current and voltage. Such studies are of great importance as the device is subjected to conditions similar to what would be experienced in a real application of power converters. During the aging campaign, we have monitored the changes of the current-voltage (I-V), capacitance-voltage (C-V) and S-parameters characteristics. Both static and dynamic electrical characteristics of the devices are measured as a function of stress time and are modeled. Notably, these results are used to simulate the efficiency of a DC-DC buck converter using both fresh and aged devices. The investigation of the impact of aging the GaN HEMT on the efficiency of power converts are of very high interest to circuit and system designers, as they will be eager to understand the effects of device degradation on their systems.

5.2. Aging methodology

Tested transistor is a fresh GS66508P from GaN Systems [7], which is a p-type gate normally-off AlGaIn/GaN power transistor operating in the range of 650V/30A. In the following lines, the aged GaN HEMT will be noted DUT_M. The evolution of the electrical parameters of the DUT_M from the new state to the aged state is monitored using a pulsed I-V measurements at a pulse frequency of 100 Hz and a pulse width of 4 μ s, which is short enough to ensure iso-thermal measurement of pulsed I-V GaN HEMT characteristics. Moreover, to separate trapping effects on measurements, pulsed I-V characteristics were performed at DC-bias levels $V_{GS0} = 0$ and $V_{DS0} = 0$. At this bias condition, trapping is expected to be negligible.

During aging, three DC characteristics were measured successively at the fresh state ($t = 0$), 216 h, and 720 h. The second characterizations are performed at 216 h, which is short enough

to ensure a regular aging monitoring in the infant stage [8]. The last characterization is performed after 504h before the second one so that the aging process is not interrupted and thus the degradations of the device can be detected.

Fig. 5.1 (a) shows the developed aging switching bench, which is described in [9]. The gate driver proposed in [10] has been used to drive the power GaN HEMTs. PWM1 and PWM2 are two complementary pulse width modulated signals. The proposed switching circuit enables to investigate the impact of hot electrons on GaN HEMTs with low energy consumption compared to that in [11] because no load is used. The used switching conditions presented in **Table 5.1** have been chosen to ensure that the DUT_M switches under its Safe Operating Area (SOA). As shown in **Fig. 5.1 (b)**, the developed switching bench places similar stresses on the DUT_M, which could exist in a large class of power management products such as power converters: on-state stress, semi-off state stress and off-state stress. In the on-state, DUT_M is on, I_D is equal to 10 A and V_{DS} is equal to 1.14V. In the semi-off state, DUT_M is turning-on, when both high current and high voltage exist simultaneously. In the off-state, DUT_M is off, I_D is null and V_{DS} is equal to 200 V. The current rise time is equal to 3.94 μs and the voltage rise time is equal to 53.46 ns. To ensure that the aging of the DUT_M respects the SOA, the measurements of the junction temperature T_J, I_D current and V_{DS} voltage are performed.

5.2.1. I_D current and V_{DS} voltage limitations

At the on-state, the I_D current is equal to 10A. At the off-state, the V_{DS} voltage is equal to 200 V. The choice of a high drain current (I_{DS} = 10 A) and a high drain-source voltage (200 V) enables to study both the degradations caused by thermal dissipation and that caused by high electric field.

According to the SOA of the DUT_M in [7], it can be seen that the used 10 A, 200 V pulse (see **Table 5.1**) is located beyond SOA boundary. This indicates that the pulse is placed within acceptable limits of I_D and V_{DS} given by the constructor.

5.2.2. Junction temperature limit

Under the switching conditions in **Table 5.1**, the temperature T_J is estimated using the thermal model of DUT_M package mounted on a PCB and a heatsink described in [12]. By using the thermal Ohm's law:

$$T_J = P_{tot} \cdot \theta_{JA} + T_A \quad (5.1)$$

Where θ_{JA} is the total thermal resistance from junction to ambient, which is equal to 3.63°C/W based on both manufacturer datasheets and SPICE model, T_A is the ambient temperature fixed at 25°C by heatsink cooling, and P_{tot} is the experimental total power loss of DUT_M over one period in watts, which is calculated by

$$P_{tot} = \frac{1}{T} \int_0^T i_{ds} \cdot v_{ds} \cdot dt \quad (5.2)$$

Where, T is the period, i_{ds} and v_{ds} are the instantaneous drain current and drain-source voltage, respectively.

From experimental measurements (**Fig. 5.1 (b)**), P_{tot} is equal to 16.68 W, the corresponded T_J is calculated using (1) and is equal to 86 °C, which is below the allowable T_J limit of 150°C. Once the switching conditions are fixed, the effect of aging the GaN HEMT under switching safe operational conditions can be investigated.

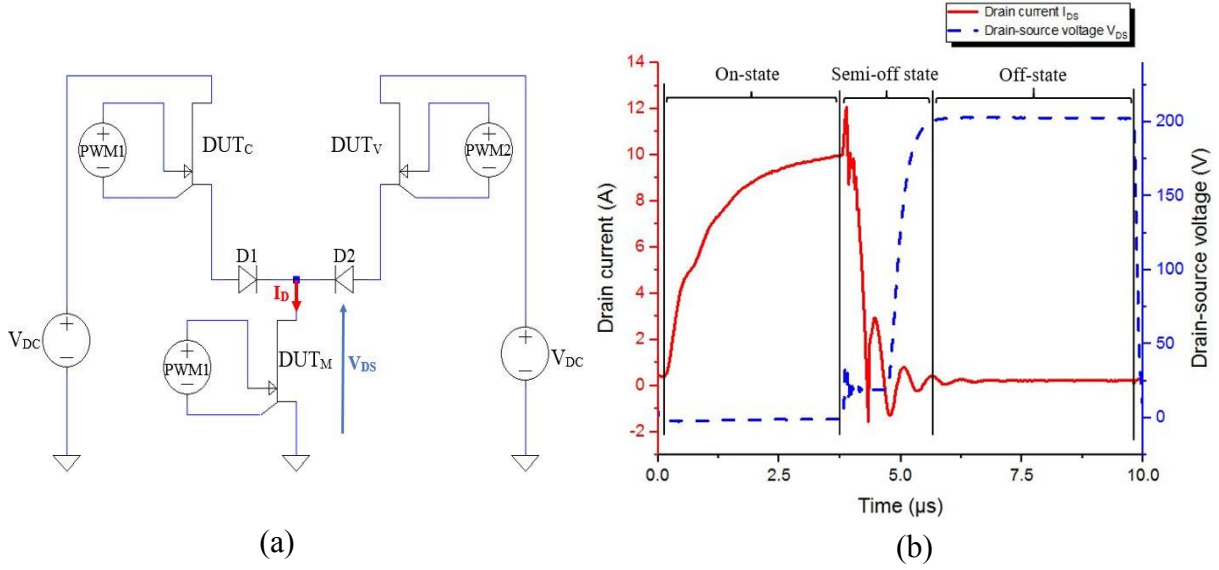


Fig. 5.1. (a) Aging switching bench; (b) I_D and V_{DS} waveforms of DUT_M over one period for switching conditions: 100 kHz, duty-cycle = 50 %, and 10 A / 200 V operating conditions.

Table 5.1: Applied switching conditions on DUT_M .

$V_{DS(OFF)}$	I_{DS}	frequency	t_{pulse}	duty-cycle
200 V	10 A	100 kHz	5 μ s	50%

5.3. Impact of aging on static characteristics

5.3.1. Static parameters degradation

The on-state resistance $R_{DS(ON)}$ is calculated in the linear region of the $I_{DS}-V_{DS}$ characteristic, using (3).

$$R_{DS(ON)} = \left. \frac{\Delta I_D}{\Delta V_{DS}} \right|_{V_{GS}=6V, V_{DS} \rightarrow 0V}^{-1} \quad (5.3)$$

Fig. 5.2 (a) shows the evolution of $R_{DS(ON)}$ during 720 h of aging under the switching conditions described in **Table 5.1**. As can be seen, $R_{DS(ON)}$ increases by 15.00% after aging. According to [13], the observed increase of $R_{DS(ON)}$ is ascribed to trapping of hot electrons in the gate–drain access region during semi-off state. The trapping of electrons in the buffer due to the off-state bias may also induce the increase of $R_{DS(ON)}$. This may lead to the increase of power conduction losses and thus the device temperature elevation, resulting in reduced power GaN HEMTs efficiency and lower DC performances.

The transconductance g_m is defined as the maximum first derivative of the input characteristic in the saturation region. **Fig. 5.2 (a)** shows the evolution of g_m during 720 h of aging under the switching conditions presented in **Table 5.1**. The resulted g_m after aging is reduced by 17.86% compared to its values before aging. The decrease in g_m is mainly due to the presence of hot electrons caused by the semi-off state, when both channel current and high electric field are present in the device [14], which could generate defects typically highest at the end of the gate on the gate–drain side [15], resulting in reduced RF performances.

The drain current I_D is determined from the measured I_{DS} - V_{DS} static characteristic at $V_{GS} = 6V$ and $V_{DS} = 0.76V$. **Fig. 5.2 (b)** shows the evolution of the current I_D during 720 h of aging under the switching conditions described in **Table 5.1**. As can be noticed, I_D decreases by 8.57 % after aging. This phenomenon is called current collapse, where I_D is reduced due to hot electrons during switching [16]. The reduction in I_D after aging can be observed in the I_D - V_{GS} static characteristic (**Fig. 5.3 (a)**). According to [17], the current collapse can be suppressed by hole injection from drain.

From **Fig. 5.3 (b)**, the existence of trapped charge after aging in the gate-drain access region is experimentally demonstrated by pulsing from various quiescent voltages ($V_{GSQ}; V_{DSQ}$): (0;0), (-8V;100V) and (-8V;300V). The exposition to both a negative V_{GSQ} and a high V_{DSQ} fosters the trapping of electrons in the drain access region of the DUT_M, while the reference condition is $V_{GSQ}=0V$ and $V_{DSQ}=0V$. Measurements were carried out at 25 °C in the dark.

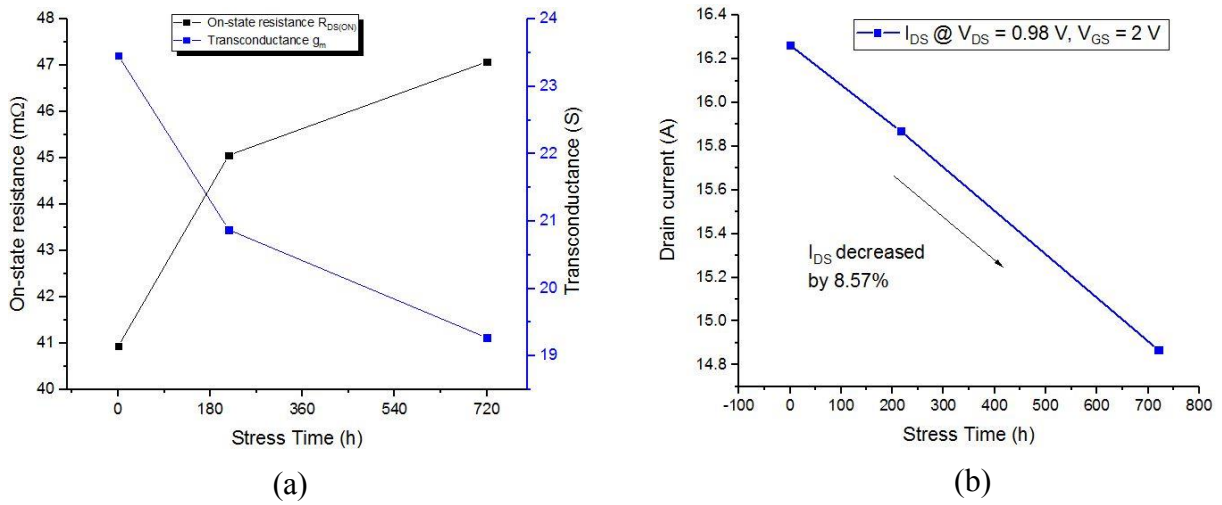


Fig. 5.2. Evolution of the static parameters during 720 h of aging: (a) $R_{DS(ON)}$ and g_m ; (b) I_{DS} at $V_{GS} = 6V$ and $V_{DS} = 0.76V$.

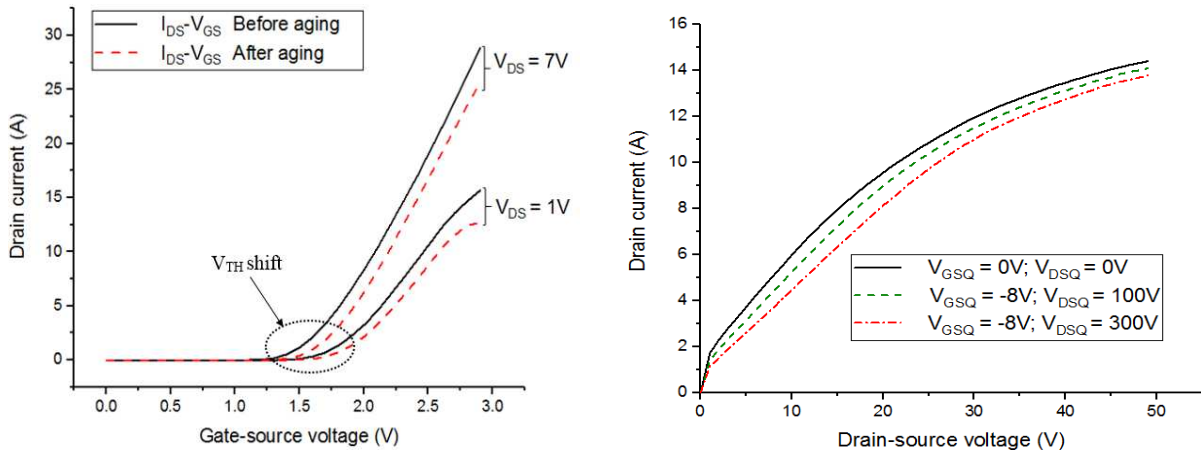


Fig. 5.3. (a) I_{DS} - V_{GS} characteristics measured at V_{DS} equals to 1V and 7V; (b) I_{DS} - V_{DS} characteristics for various quiescent bias points at 25°C in the dark.

From **Fig. 5.3 (a)**, a small shift of the threshold voltage V_{TH} is observed. Before aging V_{TH} was equal to 1.81V this value rises to 1.89 V after aging, with an increase of 4.17%. The small shift of V_{TH} voltage is also noticed in [18]. According to [19], the negative shift of V_{TH} is due

to the creation of defects under the gate caused by hot electrons during semi-off stress. In reference [20], the charge trapping at the p-GaN/AlGaN interface due to the bias-temperature instability (BTI) may also produce the shift of the V_{th} .

Moreover, a negligible increase in the gate current leakage is measured using Keithly 2636B SourceMeter, we found that I_{GSS} was equal to 11.69 μA before aging and equals to 12.08 μA after aging. The slight increase in I_{GSS} current is also confirmed in [21]. As presented in [22], the resulted degradation of I_{GSS} current is attributed to the generation of defects/leakage paths in the p-type/AlGaN gate interface due to hot electrons.

Table 5.2 summarizes the values of $R_{DS(ON)}$, g_m , I_D , V_{th} and I_{GSS} before and after 720 h of aging DUT_M under the switching conditions presented in **Table 5.1**. The re-measurement of the static parameters after a long relaxation period shows no reversibility of the phenomena. The absolute relative degradation can be calculated by

$$Degradation(\%) = \frac{(x_b - x_a)}{x_b} \quad (5.4)$$

Where x_a and x_b are the DUT_M parameter values after and before aging respectively.

Table 5.2: 720 hours aging results for DUT_M.

	$R_{DS(ON)}$ (m Ω)	g_m (S)	I_{DS} (A)	V_{th} (V)	I_{gss} (μA)
t = 0	40.93	23.46	16.26	1.81	11.69
t = 720 h	47.07	19.27	14.86	1.89	12.08
Degradation (%)	15.00	17.86	8.57	4.17	3.16

5.3.2. Static characteristics aging modeling

The proposed drain current model of DUT_M is a non-segmented, smooth and continuous equation inspired from the Motorola Electrothermal Model (MET) [23], the specific equation is shown as follows:

$$I_{DS} = K \cdot \log \left[1 + \exp \left(\frac{V_{GS} - b}{c} \right) \right] \cdot \frac{(m + n \cdot V_{GS}) V_{DS}}{1 + P \cdot (d + e \cdot V_{GS}) V_{DS}}, \quad V_{DS} \geq 0 \quad (5.5)$$

Where K is the device forward transconductance parameter at 25 °C, P is the output conductance at 25 °C, b and c are related parameters of the transfer characteristic, while m, n, d and e are related parameters of the output characteristic. The different parameters are extracted using an accurate method based on the Levenberg-Marquardt algorithm, which is described in [24].

The extracted static model parameters at 25 °C for the fresh state (t = 0) and the aged state (t = 720 h) are shown in **Table 5.3**. The modelled output and transfer characteristics of DUT_M before and after 720 h of aging are shown in **Fig. 5.4**. As can be observed, the developed aged SPICE model shows good convergence compared to experiment. The fresh and aged models of the DUT_M are implemented using LTspice simulator.

Table 5.3: Extracted Static Model Parameters at 25 °C for the Fresh State ($t = 0$) and Aged State ($t = 720$ h)

	K	P	b	c	m	n	d	e
$t=0$	2.24	0.58	1.69	0.16	6.39	-0.92	2.59	-0.44
$t=720\text{h}$	0.76	0.39	1.74	0.12	11.63	-1.68	3.21	-0.55

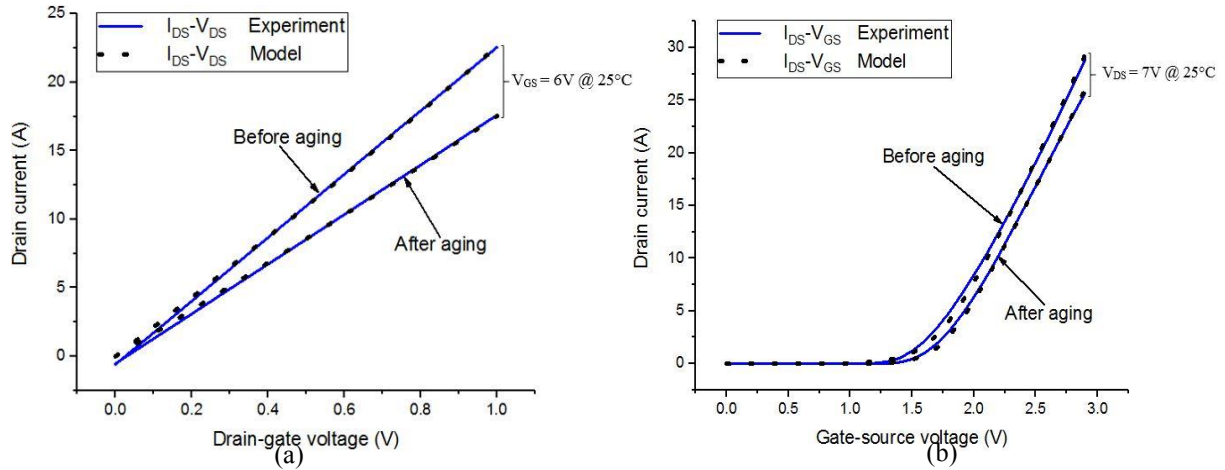


Fig. 5.4. Experiment and model: (a) Output characteristics $I_{DS}-V_{DS}$; (b) transfer characteristics $I_{DS}-V_{GS}$ before and after 720 h of aging.

5.4. Impact of aging on dynamic characteristics

To have a better understanding of the impact of aging on the dynamic behavior of the DUT, we have investigated the Capacitance-Voltage (C-V) characteristics of the p-GaN HEMT tested device as a function of the stress time. The aged C-V characteristics were modelled using a SPICE simulation tool and used to estimate the power switching losses before and after aging for a power switching application. The C-V measurements were performed using HP 4192A impedance analyzer at a frequency of 1 MHz.

5.4.1. Parasitic capacitances degradation

5.4.1.1. $C_{GS}-V_{GS}$ characteristic

Fig. 5.5 (a) shows the evolutions of $C_{GS}-V_{GS}$ characteristic before and after aging. No significant change is observed in the inversion region below the threshold voltage $V_{TH} < 1.7\text{V}$. Otherwise, a significant positive shift of the $C_{GS}-V_{GS}$ characteristic is observed in the accumulation region. Also, a slight positive shift of the threshold voltage V_{TH} can be observed. **Fig. 5.5 (b)** shows the evolution of the maximum C_{GS} capacitance during aging. The $C_{GS(\text{Max})}$ resistance is increased by 6.72 % from the fresh state to the aged state.

Authors in [25] have modelled the Mg doped concentration in the p-GaN structure using Eq (7). Based on this model, the increase of the gate capacitance profiles during aging is due to the increase in doping concentration [26].

$$N = \frac{2}{q\epsilon \frac{d(1/C^2)}{dV}} \quad (5.6)$$

Where ϵ is GaN dielectric constant, C is the measured capacitance, N is the doping concentration, q is the electron charge and V is the forward voltage used in the C_g - V_g measurement.

According to previous literature reports [27-28], we attribute this mechanism to the activation of the p-type dopant during aging, induced by the flow of a high density of carriers within the active region of the devices. To understand this interpretation, we have to consider that after the growth of a p-type layer, only part of the Magnesium acceptor atoms are electrically active, due to the fact that many Mg atoms are passivated by hydrogen, through the formation of Mg-H bonds, where the hydrogen is located at the nitrogen anti-bonding site [29-30]. To achieve a better activation of Mg, both high temperature annealing and low energy electron beam irradiation (LEEBI [31-32]) can be carried out. Even after these treatments, part of the Mg atoms can remain electrically inactive [33-34]. The increase of the gate capacitance can be responsible for efficiency loss [35].

During the off-state stress electrons can accumulate in traps, creating a virtual gate resulting in a threshold voltage shift. A leakage path can be formed at the edge of the Schottky contact, where the lateral component of the electric field is high. For very high negative voltages, additional trap states or defects near the Schottky contact can be created.

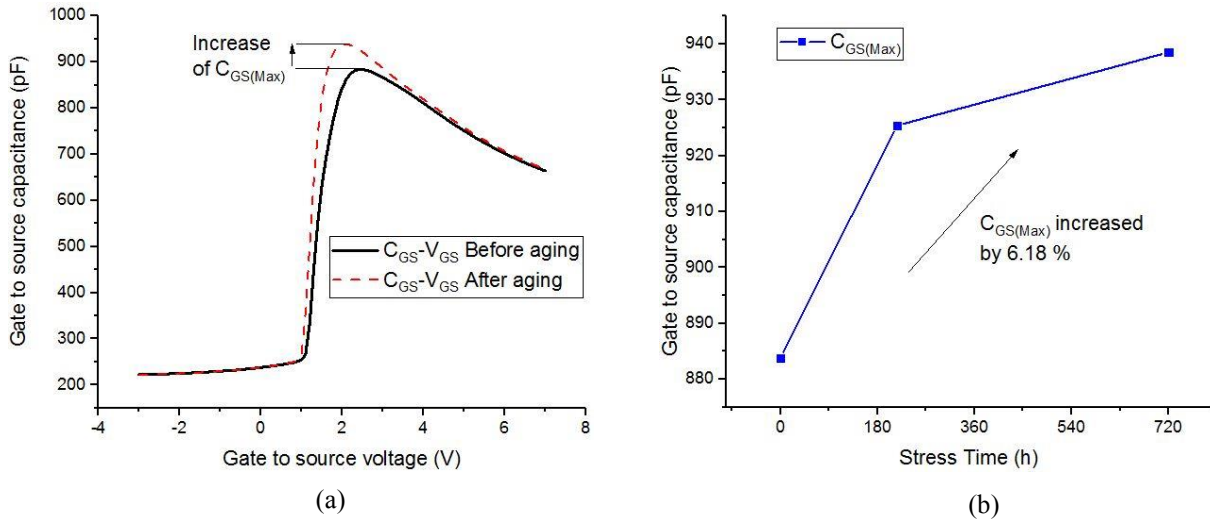


Fig. 5.5: (a) Evolution of C_{GS} - V_{GS} characteristic before and after aging; (b) Evolution of $C_{GS(Max)}$ during aging.

5.4.1.2. C_{GD} - V_{GD} characteristic

From **Fig. 5.6 (a)** the evolutions of C_{GD} - V_{GD} characteristic before and after aging is similar to those of C_{GS} - V_{GS} characteristic. The input capacitances C_{GS} and C_{GD} have not changed for a gate voltage below V_{TH} . For V_{GS} beyond V_{TH} , C_{GS} and C_{GD} show significant increase. **Fig. 5.6 (b)** shows the evolution of the maximum C_{GD} capacitance during aging. The $C_{GD(Max)}$ resistance is increased by 6.32 % from the fresh state to the aged state.

Similarly, to the variation in C_{GS} capacitance, the degradation of the C_{GD} capacitance during aging are attributed to the activation of the p-type dopant during aging [36-39]. The increase of the Mg dopant concentration in the p-GaN structure can be modelled using Eq (7). As a consequence of aging, the charge distribution in the active layer can be modified [40] due to the generation/propagation of defective states that can contribute to the degradation of the dynamic characteristics of the GaN HEMT [41]. Furthermore, A leakage path can be formed at the edge of the Schottky contact, where the lateral component of the electric field is high [42]. For high voltages additional trap states or defects near the Schottky contact can be created.

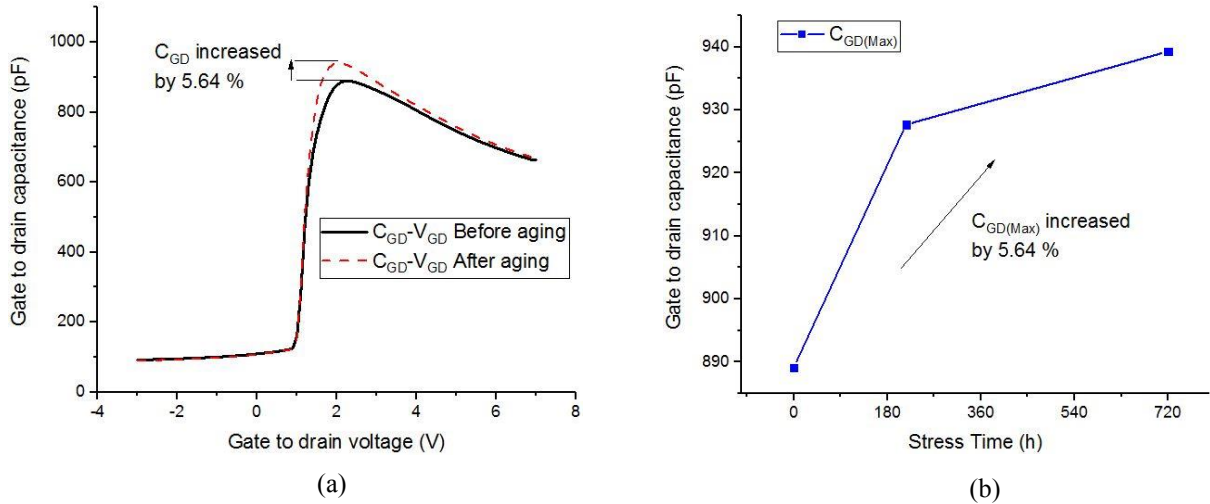


Fig. 5.6: (a) Evolution of $C_{GD}-V_{GD}$ characteristic before and after aging; (b) Evolution of $C_{GD(Max)}$ during aging.

5.4.1.3. $C_{DS}-V_{DS}$ characteristic

Fig. 5.7 (a) shows the evolution of the $C_{DS}-V_{DS}$ characteristic during aging. Compared to the input capacitances C_{GS} and C_{GD} , an opposite evolution during aging of the output capacitance is observed. **Fig. 5.7 (b)** shows the evolution of the C_{DS} capacitance at $V_{DS} = 10$ V during aging. The C_{DS} resistance is decreased by 0.90 % from the fresh state to the aged state.

This change in C_{DS} capacitance after aging was attributed to the extension of the depletion region due to the effect of the traps in the 2-dimension electron gas (2DEG) channel below the gate [43].

The additional extending depletion region could be attributed to locally ionized acceptor-like traps under the gate following the application of a 200 V stress during the off-state. The ionized traps formed a negative potential to deplete 2DEG. Using TCAD simulation it is observed in [44] that electrons were trapped into the AlGaIn layer underneath the gate edge at the drain side after the device endured high V_{DS} off-state stress. The injected electrons in the AlGaIn are trapped by acceptor-like traps. These trapped electrons caused the decrease of the 2DEG concentration [45-46]. Thus, the extension in the depletion region, which induce the decrease in $C_{DS}-V_{DS}$ characteristics.

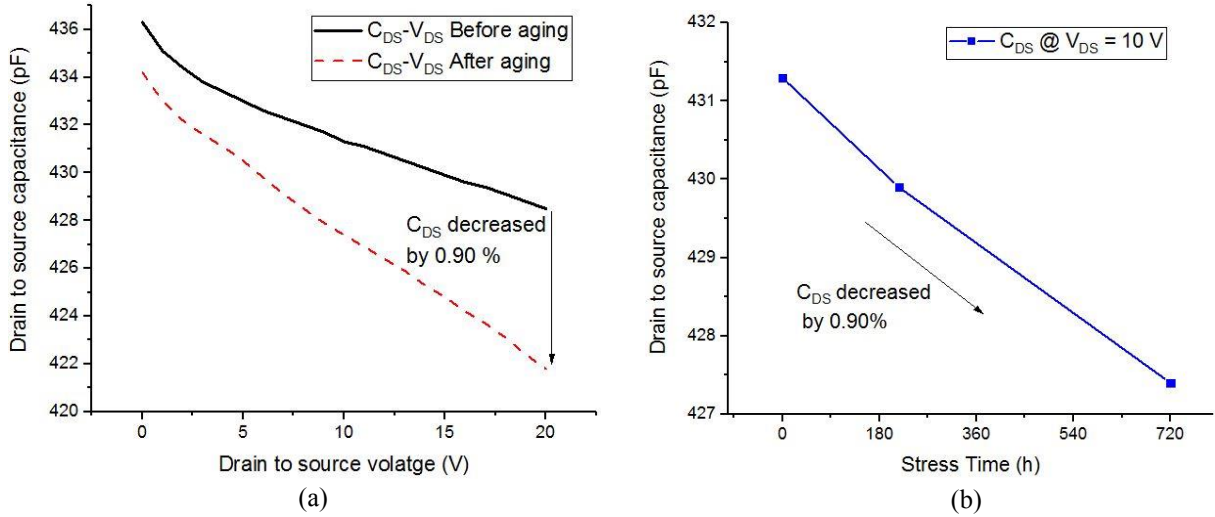


Fig. 5.7: (a) Evolution of $C_{GD}-V_{GD}$ characteristic before and after aging; (b) Evolution of C_{DS} @ $V_{DS} = 10$ V during aging.

5.4.2. Dynamic characteristics aging modeling

Using a C-V simulator, we have simulated the modelled $C_{GS}(V_{GS})$, $C_{GD}(V_{GD})$ and $C_{DS}(V_{DS})$ capacitances before and after aging. As shown in **Fig. 5.8**, the modelled capacitances fit with high convergence the measured experimental capacitances during aging. Eq. (16-17) of chapter II are used for fitting the C-V characteristics during aging. **Table 5.4** shows the extracted values of the C_{GS} , C_{GD} and C_{DS} model before and after 720 h of aging. The modeling of the dynamic behavior of the DUT during aging, enables to evaluate the impact of aging on the switching power losses of the GaN HEMT using a simulation approach.

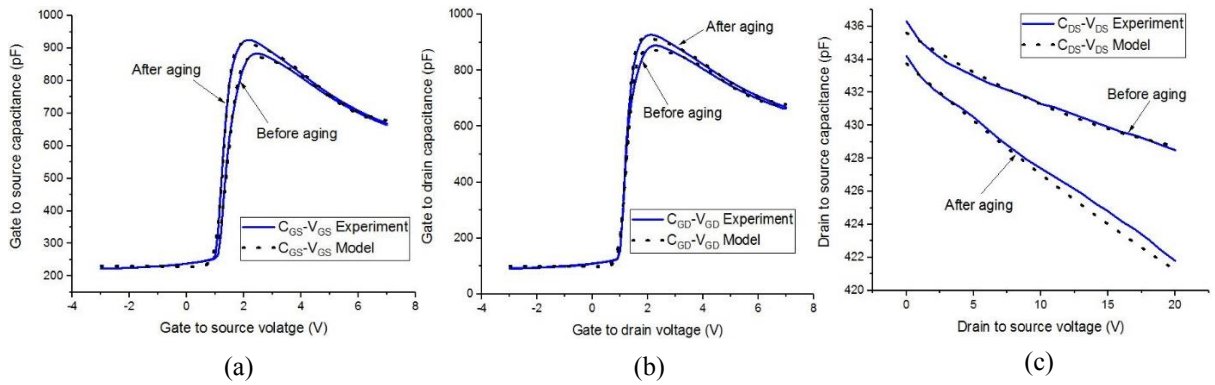


Fig. 5.8: Experiment and model before and after 720 h of aging: (a) $C_{GS}-V_{GS}$ characteristics; (b) $C_{GD}-V_{GD}$ characteristics; (c) $C_{DS}-V_{DS}$ characteristics.

Table 5.4: Extracted values of C_{GS} , C_{GD} and C_{DS} model before and after 720 h of aging.

Parameters	C_0^{GS}	C_1^{GS}	A_{GS}	V_{TH}	C_2^{GS}	B_{GS}	V_P		
t = 0	229.79 pF	896.86 pF	2.79 pF/V	1.44 V	242.61 pF	0.54 pF/V	4.61V		
t = 720 h	231.54 pF	941.32 pF	3.74 pF/V	1.28 V	280.22 pF	0.51 pF/V	4.36 V		
Parameters	C_0^{GD}	C_1^{GD}	A_{GD}	C_2^{GD}	B_{GD}	C_0^{DS}	a	b	
t = 0	99.70 pF	886.26 pF	3.53 pF/V	228.48 pF	0.59 pF/V	435.61 pF	-1.2E-3	2.06E-5	
t = 720 h	100.27pF	937.41 pF	4.14 pF/V	275.68 pF	0.52 pF/V	433.74 pF	-1.56E-3	1.04E-5	

5.5. Impact of aging on S-parameters characteristics

The evaluation of the package parasitic elements during aging is of vital importance to power switching performances of GaN HEMT power converters that operate at high frequency. In this section, we have performed an experimental S-parameters characterization before and after 720 h. Based on the measured S-parameters, we have monitored during aging the GaN HEMT parasitic inductances, resistance and capacitance. This enables to evaluate the impact of aging the GaN HEMT parasitic elements on the power efficiency of power converters. The S parameter measurements were performed using Keysight E5080B vectoral network impedance analyzer at a frequency sweep between 100 kHz and 200 MHz by a step of 100 kHz.

5.5.1. S-parameters degradation

Fig. 5.9 shows the magnitude and the phase of the four S-parameters of the device, before and after 720 h of aging.

The degradation of S12 and S21 can be explained by the decrease of transconductance (g_m) and the increase of gate to drain capacitance (C_{GD}) [47,48]. The Miller capacitance C_{GD} is composed of two parts, the p-GaN capacitance (C_{p-GaN}) and the drift region capacitance (C_{AlGaN}) [49]. The interface state generation after stress are responsible of the degradation of both g_m , C_{GD} [50]. By simulating the temperature distribution of the GaN structure using TCAD physical simulator, it is demonstrated in [51] a local hot spot in the drift after aging. The electrons are accelerated to high velocities by this high electric field. They become highly energized and should be accelerated away from their normal directional flow. These highly energized electrons may create interface states by breaking AlGaIn bonds [52] or be injected into generated surface traps (hot electron injection) at the p-GaN/AlGaIn interface [53]. The trapped electrons reduce the electric charge density and therefore the total charge in the area affected by the trapped carriers. As results, the capacitance characteristics are shifted by the trapped charges.

The S12 and S21 phase were shifted to the left after aging. This shift means that the resonant frequency SRF of the test device has been changed due “hot-carrier stressing times” [54]. As a consequence, the parasitic elements have been changed during aging. This change in parasitic elements is confirmed in **Table 5.5**.

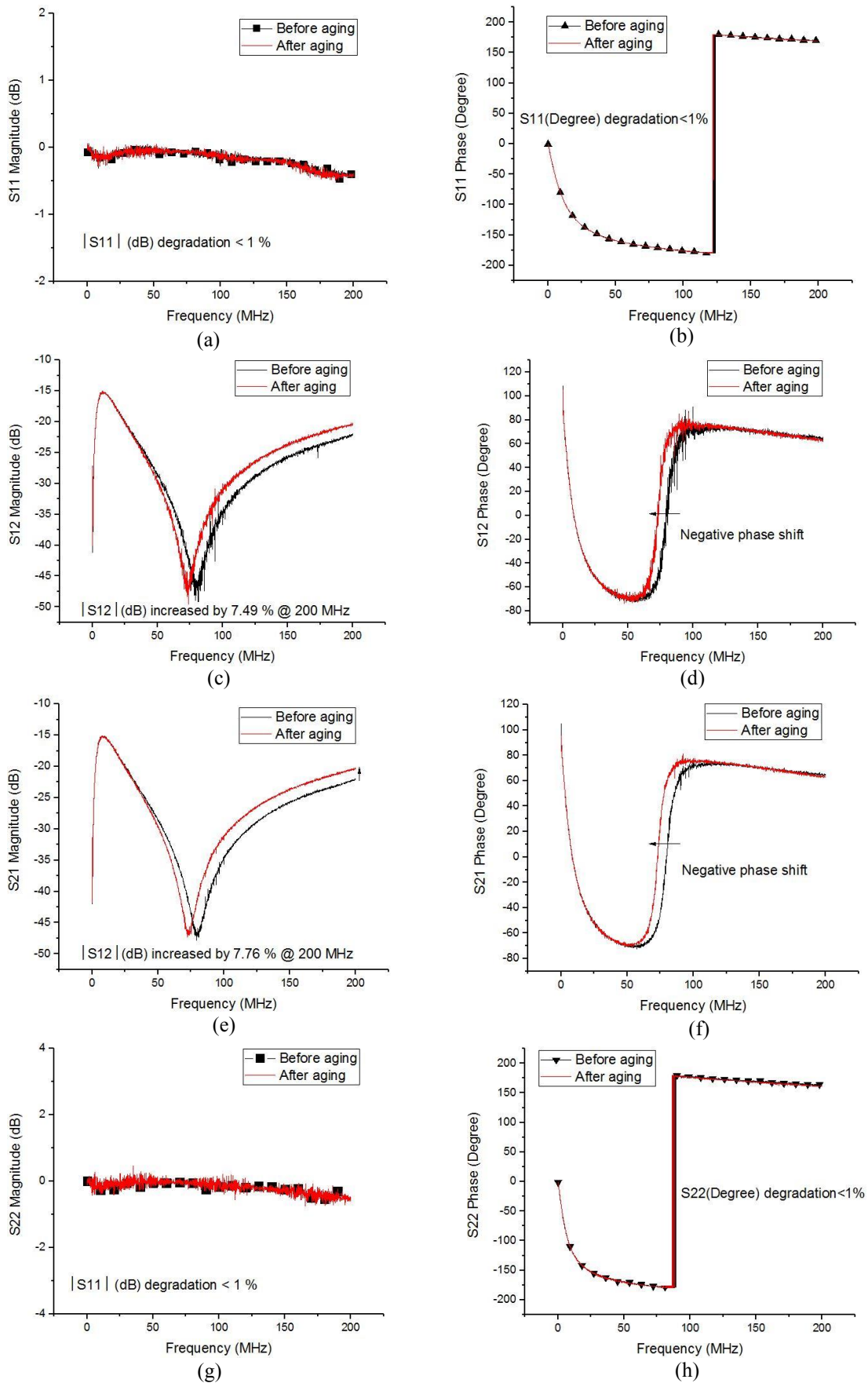


Fig. 5.9: Evolution of the S parameters during 720 h of aging: (a) S₁₁ Magnitude, (b) S₁₁ Phase, (c) S₁₂ Magnitude, (d) S₁₂ Phase, (e) S₂₁ Magnitude, (f) S₂₁ Phase, (g) S₂₂ Magnitude, (h) S₂₂ Phase.

The parasitic parameters of GaN transistor are increasingly sensitive to defects bound to the presence of charges in the p-GaN/AlGaN interface and at the drift region [55]. The hot carriers produce an additional interface trap density and trapped electron charge which results in a degradation of the parasitic elements of the device [56]. As shown in **Table 5.5**, the parasitic inductances L_g , L_s , L_d have been increased after aging. In [57] they have studied the impact of each parasitic inductance on the power efficiency of power GaN HEMTs. Based on this study, by eliminating the impact of L_d or L_g , the reduction of turn-on switching loss is negligible (around 1%). On the other hand, when the critical parasitic inductance like L_s , is removed, the turn-on switching loss will reduce significantly (around 9%).

From Table 6, the extracted parasitic capacitances C_{GS} , C_{GD} and C_{DS} using the S-parameters technics shows similar degradation to that extracted using the impedance meter in the previous section. The degradation of the GaN HEMT parasitic capacitances increases the switching power losses of the device [58]. During the turn-on transition, the energy stored in the C_{GD} and C_{DS} capacitances is discharged through the channel of the device, which generates switching loss [59].

As shown in **Table 5.5**, the parasitic resistances R_g , R_s , R_d have been increased after 750 h of aging. The increased parasitic resistances are caused by the degradation of the GaN HEMT ohmic contacts [60]. Losses in the parasitic resistances increase the conduction power losses and reduce the efficiency of power converters [61].

According to the literature [62, 63], the most probable cause of degradation for power GaN HEMT parasitic elements is attributed to hot electron-induced interface state generation and/or impact ionization.

Table 5.5: Extracted values of parasitic parameters before and after 720 h of aging.

Parameters	L_s (nH)	L_g (nH)	L_d (nH)	C_{gs} (pF)	C_{gd} (pF)	C_{ds} (pF)	R_g (m Ω)	R_s (m Ω)	R_d (m Ω)
t = 0	1.66	1.98	4.49	238.24	67.20	439.69	367.25	110.39	159.94
t = 720 h	2.02	1.93	4.96	244.68	69.23	431.12	617.4	120.25	249.67
Degradation (%)	21.68 \uparrow	2.52 \uparrow	10.46 \uparrow	2.70 \uparrow	3.02 \uparrow	1.94 \downarrow	68.11 \uparrow	8.93 \uparrow	56.10 \uparrow

5.5.2. S-parameters aging modeling

Using an S-parameters simulator, we have implemented the extracted parasitic element during aging shown in **Table 5.5** in the GaN HEMT small-signal equivalent circuit presented in chapter 3. The frequency response (S-parameters) of the aged device are simulated using Keysight Advanced Design System (ADS) high frequency circuit simulator. The modeling of the S-parameters of the DUT before and after aging, enables to evaluate the impact of aging on the RF performances of the GaN HEMT using a simulation approach. As shown in **Fig. 5.10**, the modelled S11 and S12 fit with high convergence the measured experimental S-parameters during aging.

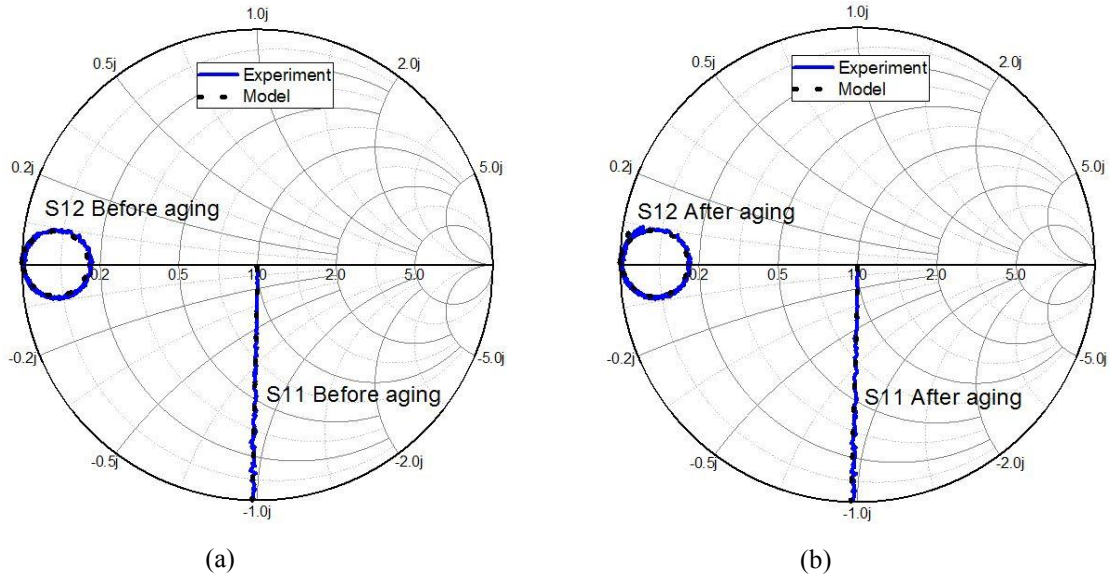


Fig. 5.10: Experiment and model of S11 and S12 parameters: (a) Before aging; (b) after 720 h of aging.

5.6. Step stress tests

To summarize, in the previous section we have performed a constant aging campaign under fixed stress conditions, which respect the SOA zone of the device. Tests at constant stress conditions required long aging time to activate the failure mechanisms [64]. In this section, we have investigated the aging of the power GaN HEMT using step stress tests. This technique is of interest because it allows us to quickly obtain aging information in weeks, rather than months of intensive activities as normally required from constant stress tests [65]. This enables to reduce test time and to assure that failures occur quickly enough. By performing two kinds of aging technics (constant stress and step stress), this enables the possibility to compare the degradation generated by different aging technics.

In a switching mode power converter, the transistor is continuously switched from the off-state to the on-state and vice versa. During this operation, the DUT are subject to three types of stresses: on-state stress; semi-on stress and off-state stress. To understand the failure modes that can be generated in each state, we have performed three step stress aging campaigns:

- Frequency step stress;
- On-state step stress;
- Off-state step stress.

Each aging campaign lasts 1000 h. The aging time of 1000 h is used by the JEDEC standard [66]. The aging is monitored every 200 hours by performing I-V, C-V and low leakage current characterizations. The characterization step of 200 h is also used in [67]. The aging campaign is monitored at the following times: 0, 200 h, 400 h, 600 h, 800 h and 1000 h.

5.6.1. Frequency stress

There is an increasing market pressure to reduce the size of power converter circuits with high reliability [68]. In order to address these needs, it is necessary to increase the switching frequency of the power switching circuits.

In this section, we have studied the effects of increasing the switching frequency on the degradation mechanism of the power GaN HEMTs.

The switching frequencies used during aging are: 100 kHz, 200 kHz, 300 kHz and 400 kHz. This frequency range is widely used in power converter applications [69]. The used frequency step stress bench is presented in **Fig. 5.1 (a)**. The PWM1 signal and its complementary PWM2 are generated by programming the Arduino board to produce complementary PWM output signals at various frequency: 100 kHz, 200 kHz, 300 kHz and 400 kHz. The switching aging conditions are: $V_{DS} = 200$ V, $I_{DS} = 10$ A and Duty-cycle = 50 %.

During the frequency step stress, we have observed similar trend of degradations that were found in the constant stress. After 200 h switching at 400 kHz, $R_{DS(on)}$ is 9.55 % higher as compared to switching at 100 kHz. The increase in dynamic $R_{DS(on)}$ is thus stronger under constant switching conditions than for a step stress switching frequency.

In literature [70,71], it is known that the GaN HEMTs often suffer from an increased dynamic on-state resistance after switching from high-bias off-state. The phenomenon is based on trapping effects [72], and the electron trapping can be found at different places in the GaN transistor, at the 2DEG interface, in the AlGaIn barrier layer or in the GaN buffer layer. This may result in increased conduction power losses of the device and an increase in temperature. **Table 5.6** summarizes the most critical degradation processes that are induced in the frequency step stress along with the related failure modes, causes and their effects on the efficiency of GaN HEMT power converters.

5.6.2. On-state stress

In energy conversion applications, it is important to have a low I_{GSS} gate leakage current to reduce on-state power losses. The purpose of performing an on-state step stress is to evaluate the degradation of the current I_{GSS} as a function of stress time.

In the on-state stress, the drain is short circuited with the source $V_{DS} = 0$ V and an increasing voltage is applied to the gate [73]. The voltages applied to the gate respect the SOA zone: 1.75 V, 3.5 V, 5.25 V and 7 V. **Fig. 5.11 (a)** shows the proposed the stress bench schematic for the on-state step stress. After every 200 h, the grid voltage is increased by a step of 1.75 V. During the aging stress $I(V)$ and $C(V)$ and low current characteristics are monitored at times: 0, 200 h, 400 h, 600 h, 800 h and 1000 h.

The investigation of the effect of high electric field on GaN HEMT is mandatory to distinguish experimentally between the degradations caused by self-heating mechanism at high current and low voltage, and those caused by high voltage switching conditions as well.

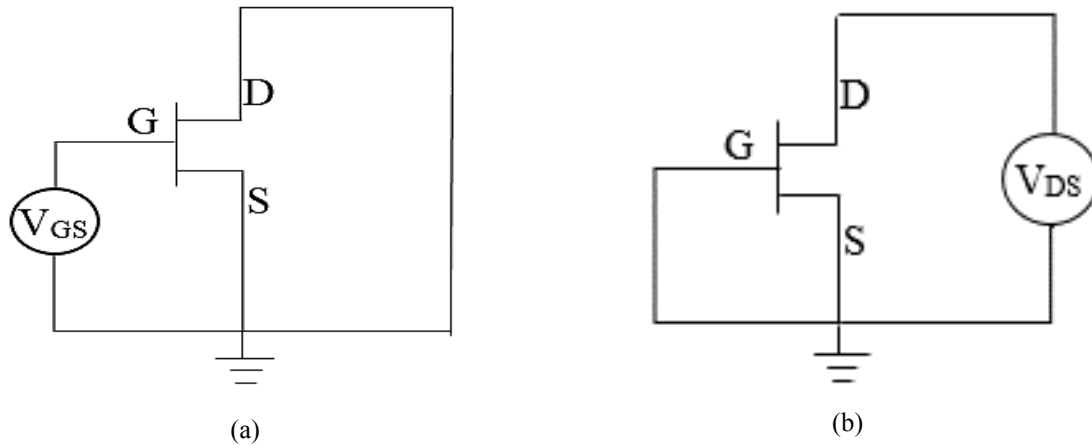


Fig. 5.11: (a) On-state stress bench, (b) Off-state step stress bench [73].

The on-state stress makes it possible to extract the degradations that may exist on the gate of the component when a positive voltage is applied. The resulted degradations after aging were: increase of the gate leakage current I_{GSS} ; negative shift of the threshold voltage V_{TH} . **Fig. 5.12** shows the evolution of the I_{GSS} current during on-state aging. The I_{GSS} current is increased by 79.62 % from the fresh state to the aged state. As observed, a non-negligible increase in the gate current leakage is measured using Keithly 2636B SourceMeter, we found that I_{GSS} was equal to 3.96 μA before aging and equals to 14.03 μA after aging. The resulted degradation of I_{GSS} current is attributed to the generation of defects/leakage paths in the p-type/AlGaN gate interface due to hot electrons [74,75]. According to [76], this may also induce a negative shift of the threshold voltage V_{TH} . **Table 5.6** summarizes the most critical degradation processes that are induced in the on-state step stress along with the related failure modes, causes and their effects on the efficiency of GaN HEMT power converters.

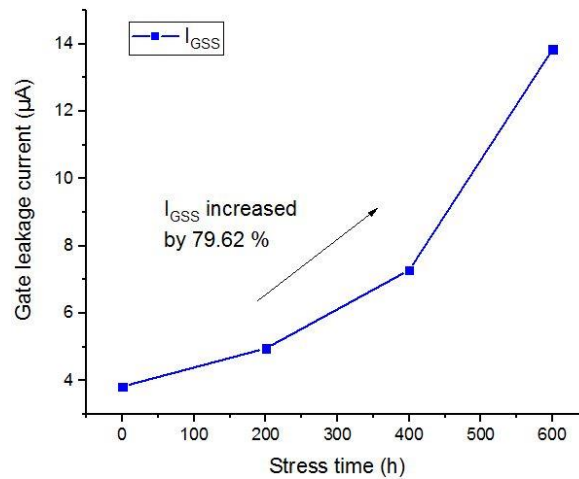


Fig. 5.12: Evolution of I_{GSS} current at $V_{GS} = 6 \text{ V}$ during on-state stress.

5.6.3. Off-state stress

In GaN HEMT power converter applications, the GaN transistors must be continuously switched from the off-state under a high drain voltage to the on-state with a gate bias. The optimization of the GaN HEMTs allows:

- Improved energy efficiency of GaN HEMT power converters by reducing power losses due to leakage currents.
- Get a wide range of voltage.

The off-state step stress enables to evaluate the degradations that may exist when the component is subjected to a high electric field. **Fig. 5.11 (b)** shows the off-state stress bench schematic.

In this type of stress, the gate is short circuited with the source $V_{GS} = 0$ V and an increasing voltage is applied to the drain. After every 200h the drain voltage is increased by a step of 100 V. The voltages applied on the drain respect the SOA zone: 100 V, 200 V, 300 V and 400 V. During aging, pulsed I (V), C (V) and low current characteristics are monitored at times: 0, 200 h, 400 h, 600 h, 800 h and 1000 h.

I_{DSS} is defined as the drain leakage current when the rated voltage is applied to the drain-source. **Fig. 5.13** shows the evolution of the I_{DSS} current during off-state aging. The I_{DSS} current is increased by 95.60 % from the fresh state to the aged state.

Using Electroluminescence microscopic analysis in [79], it is observed a severe degradation located at the drain-side gate edge when applying high electric field in the drain side region. Off-state voltage stress induced the generation of source-drain current paths [80] and short circuits between gate and channel [81].

To explain this phenomenon, electrons in the channel are accelerated by the applied electric field (i.e., drain voltage), gaining sufficient energy to cross the AlGaN barrier and getting trapped below the gate (edge) and in the gate-to-drain region [82]. This effect results in increasing of drain leakage current and drain parasitic capacitance. **Table 5.6** summarizes the most critical degradation processes that are induced in the off-state step stress along with the related failure modes, causes and their effects on the efficiency of GaN HEMT power converters.

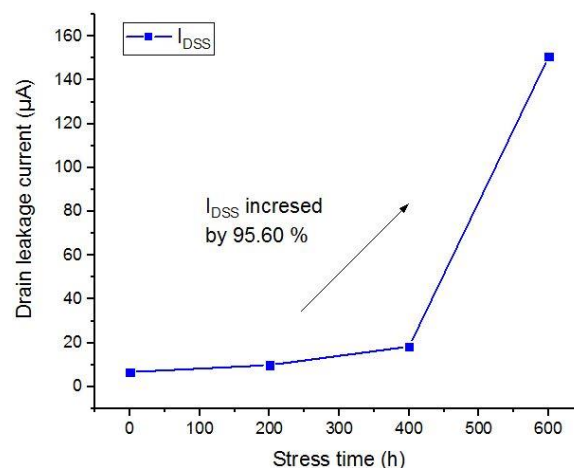


Fig. 5.13: Evolution of I_{DSS} current at $V_{DS} = 200$ V during off-state stress.

Table 5.6: Failure mode and effects analysis (FMEA) of the GaN HEMT during 1000 h of step stress aging.

STRESS TYPE	FAILURE MODE	FAILURE CAUSE	FAILURE EFFECT
Frequency step stress	<ul style="list-style-type: none"> - Increase in $R_{DS(on)}$ by 9.55%. - Decrease in $I_{DS(Max)}$ by 15.45%. - Increase in $C_{GS(MAX)}$ by 6.72%. - Increase in $C_{GD(MAX)}$ by 6.32%. - Decrease in $C_{DS(Max)}$ by 2.06%. 	<ul style="list-style-type: none"> - Trapping of hot electrons under the gate and at the gate edge [83]. - Generation of lattice defects [84]. - Buffer trapping [85]. - Surface trapping [86]. 	<ul style="list-style-type: none"> - Elevation in the device temperature. - Increase of the switching losses. - High conduction power losses. - RF performance degradation.
On-state step stress	<ul style="list-style-type: none"> - Increase in I_{GSS} gate leakage current by 79.62%. - Negative shift of the V_{TH} voltage by 12.44%. - Increase in $C_{GS(MAX)}$ by 3.81%. - Increase in $C_{GD(MAX)}$ by 4.08%. - No change in C_{DS} capacitance. 	<ul style="list-style-type: none"> - Generation of defects/leakage paths in the p-GaN/AlGaIn gate stack [60]. - Trapping/detrapping of electrons in the gate area [61]. 	<ul style="list-style-type: none"> - Increase of the gate power losses. - Normally-on behavior. - Gate breakdown.
Off-state step stress	<ul style="list-style-type: none"> - Increase in I_{DSS} drain leakage current by 95.60%. - Increase in $C_{GS(MAX)}$ by 4.62%. - Increase in $C_{GD(MAX)}$ 5.16%. - Increase in $C_{DS(Max)}$ is increased by 95.60%. 	<ul style="list-style-type: none"> - Generation of source-drain current paths [87]. - Short circuits between gate and channel [88]. 	<ul style="list-style-type: none"> - Elevation in the off-state power losses. - Drain breakdown.

5.7. Effect of aging the GaN HEMT on the efficiency of power converters

Both the static and dynamic characteristics of the GaN HEMT have been modelled by measuring experimentally the I-V, C-V, S-parameters, drain and gate leakage currents characteristics of the DUT during 720 h of aging. As a result, we have built an accurate power losses model for the aging of the GaN HEMT based on experimental measurements, which include the major power losses in power switching applications: conduction power losses (P_{Cond}), switching power losses (P_{SW}), Gate power losses (P_{GSS}), Off-state power losses (P_{DSS}). In this section, the effects of aging the GaN HEMT on power converters are studied by modeling the power losses before and after 720 h of aging.

Using the extracted power losses model of the GaN HEMT, we have estimated the impact of aging the GaN HEMT on the efficiency of a 200 V / 24 V DC-DC converter stage with GaN HEMT. **Fig. 5.14** shows a wind energy application which produces an output voltage of 200 V.

This voltage is stepped down to 24 V using a buck DC-DC converter for electric vehicle charging stations.

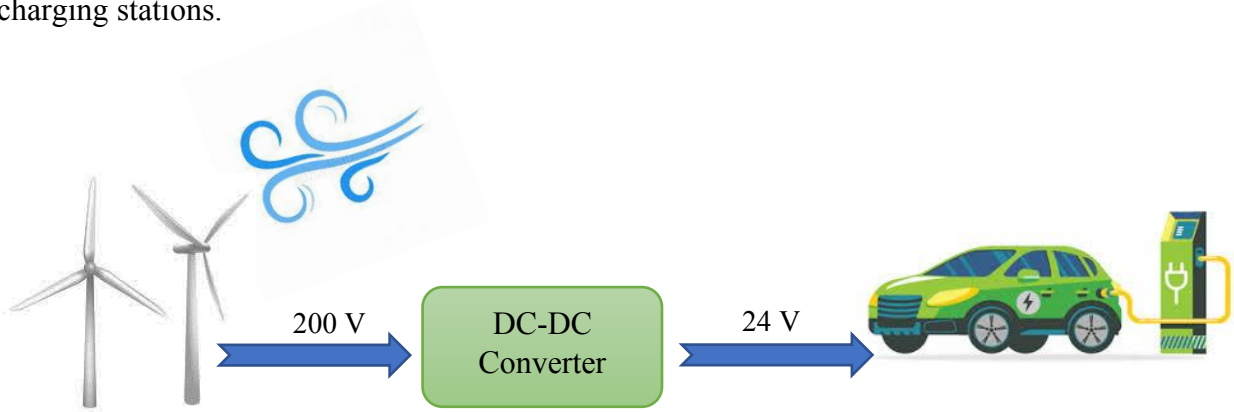


Fig. 5.14: Wind energy application with a 200 V/ 24 V DC-DC converter stage for electric vehicle charging stations.

To remain the same switching conditions of the studied aging campaign, a 200 V converter application is used. **Fig. 5.15** shows the used DC-DC converter, which is a 200 V / 24 V buck converter. The DUT_M is the SPICE model of the aged GaN HEMT.

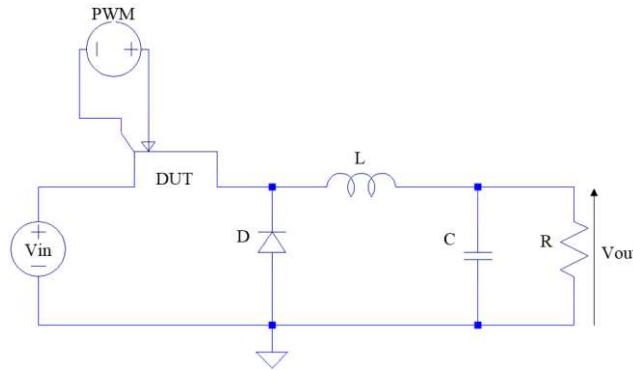


Fig. 5.15: DC-DC buck converter, with $L = 170$ mH, $C = 850$ μ F and $R = 20$ Ω , at 100 kHz switching frequency, 200 V input voltage and 24 V output voltage.

The power losses in the inductor, capacitor and diode are given respectively by the following equations [89].

$$P_L = \left(I_{out}^2 + \frac{\Delta I_L^2}{12} \right) R_L \quad (5.7)$$

$$P_C = R_C \frac{\Delta I_L^2}{12} \quad (5.8)$$

$$P_D = V_D I_{out} (1 - D) \quad (5.9)$$

Where I_{out} is the output current, ΔI_L is the inductor current ripple, which assumed equals to 30% of the maximum output current (A), D is the duty-cycle, R_C is the equivalent series resistance of the capacitor, equals to 30 m Ω , R_L is the equivalent series resistance of the inductor, equals to 0.2 m Ω , V_D is the forward voltage of the diode, equals to 0.7 V.

5.7.1. Conduction power losses aging effect

The purpose of this part is to model the aging of the DUT_M in order to evaluate the effects of aging the GaN HEMT under SOA on the power conduction losses of the DC-DC converters by a SPICE simulation approach. The conduction power losses P_C is calculated by [90]:

$$\begin{cases} P_C = \frac{1}{T_{on}} \int_{t=0}^{T_{on}} i_{ds} \cdot v_{ds} \cdot dt \\ T_{on} = \frac{d_c}{f} \end{cases} \quad (5.10)$$

Where T_{on} is the conduction time, d_c is the duty cycle and f is the frequency.

Figure 5.16 shows the measurement of P_C at three output currents in the studied DC-DC buck converter. The effect of aging the GaN HEMT in the SOA during 720 h is that it produces an increase of P_C losses after aging. The increase of P_C is due to the increase of the DUT_M on-state resistance after aging. Resulting in decreased power converter efficiency. From **Table 5.7**, an average increase of P_C equals to 7.42 % is observed between the before aging state and the after aging state for various output currents: 10 A, 12 A and 14 A.

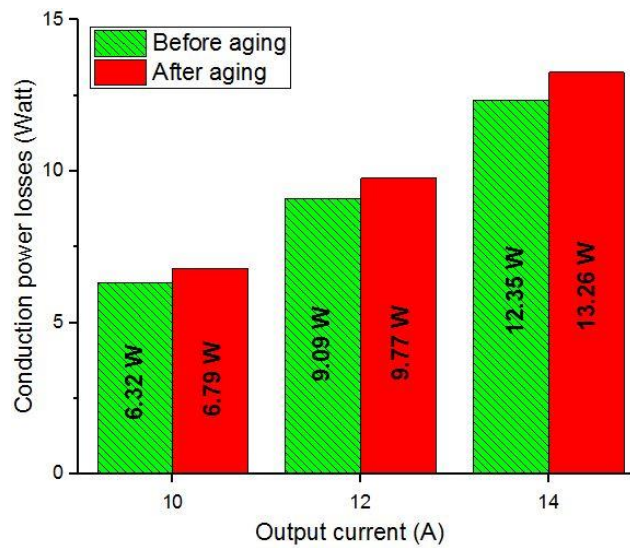


Fig. 5.16. Conduction power losses of DC-DC buck converter before and after 720 h of aging for different output current: 10 A, 12 A and 14 A.

Table 5.7: DC-DC buck converter conduction power losses, before and after 720 h of aging for output current: 10 A, 12 A and 14 A.

P_C (W)	10 A	12 A	14 A
Before aging (t=0)	6.32	9.09	12.35
After aging (t=720h)	6.79	9.77	13.26
Degradation (%)	7.43	7.48	7.36

5.7.2. Switching power losses aging effect

In order to investigate the impact of aging the GaN HEMT on the switching power losses in a switching power application, we have implemented in SPICE simulator both the modelled static characteristic obtained in section 5.3 and parasitic capacitances of the GaN HEMT obtained in section 5.4 before and after 720 h of aging. The switching power losses $P_{SW(on)}$ is calculated by [91]:

$$P_{SW(on)} = \frac{1}{T_{SW(on)}} \int_0^{T_{SW(on)}} i_{ds} \cdot v_{ds} \cdot dt \quad (19)$$

Where, $P_{SW(on)}$ is the turn-on power switching losses in (Watt) and $T_{SW(on)}$ is the turn-on switching time. **Figure 5.17** shows the measurement of switching power losses (P_{SW}) at three output currents in the studied DC-DC buck converter. From **Fig. 5.17**, the effect of aging the GaN HEMT in the SOA during 720 h is that it produces an increase of P_{SW} losses after aging. The increase of P_C is due to the degradations of the DUT_M parasitic capacitances after aging. Resulting in decreased power conversion efficiency. The average increase of P_{SW} is estimated to be equal to 7.42 % before aging state and the after aging state for various output currents: 10 A, 12 A and 14 A.

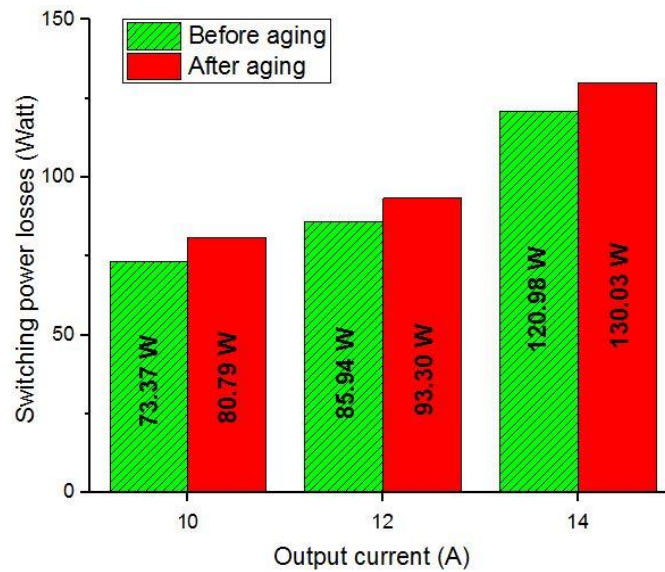


Fig. 5.17: Switching power losses of DC-DC buck converter before and after 720 h of aging for different output current: 10 A, 12 A and 14 A.

5.7.3. Gate leakage current losses aging effect

To accurately evaluate the impact of the on-state aging on the efficiency of GaN HEMT power converters, we have calculated the gate power losses caused by the gate leakage current before and after 720 h of aging. **Fig. 5.18** shows the measurement of the gate power losses (P_{GSS}) before and after 720 h of on-state aging. The effect of aging the GaN HEMT in the SOA during 720 h is that it produces an increase of gate losses after aging. This is due to the degradations generation of defects/leakage paths in the p-GaN/AlGaIn gate stack [77] and the

trapping/detrapping of electrons in the gate area [78]. Resulting in decreased power conversion efficiency. The average increase of the gate power losses is estimated to be equals to 2.62 % before aging state and after the aging state.

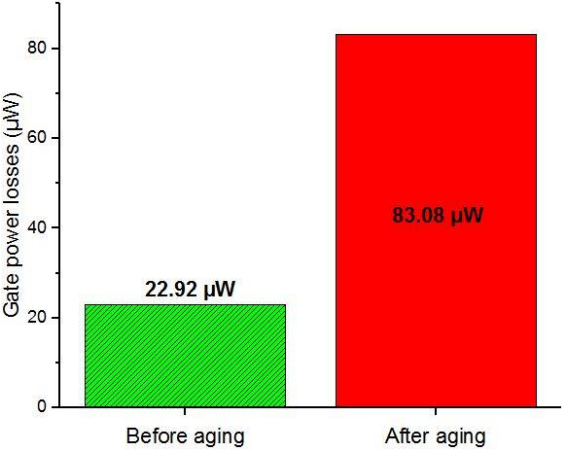


Fig. 5.18: Estimated gate power losses before and after 720 h of on-state step stress aging.

5.7.4. Drain leakage current losses aging effect

To accurately evaluate the impact of the off-state aging on the efficiency of GaN HEMT power converters, we have calculated the off-state power losses caused by the drain leakage current before and after 720 h of aging. Fig. 5.19 shows the measurement of the off-state power losses before and after 720 h of off-state aging. The effect of aging the GaN HEMT in the SOA during 720 h is that it produces an increase of off-state power losses after aging. This is due to the degradations generation of source-drain current paths [80] and short circuits between gate and channel [81]. Resulting in decreased power converter efficiency. The average increase of the gate power losses is estimated to be equal to 21.83 % before and after the aging state

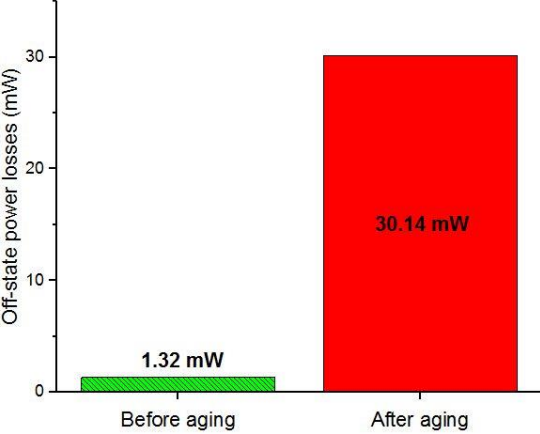


Fig. 5.19: Estimated gate power losses before and after 720 h of off-state step stress aging.

5.7.5. Efficiency aging impact

The following table summarizes the total losses and calculates the efficiency of a 200 V / 24 V DC-DC buck converter with GaN HEMT at 25 °C and 10 A.

Table 5.8: Total losses in DC-DC buck converter with GaN HEMT at 25°C, 10 A.

Power losses	Before aging	After aging
P_{out}	2000 W	2000 W
P_L	20.05 mW	20.05 mW
P_C	22.5 mW	22.5 mW
P_D	1.05 W	1.05 W
P_{Cond}	6.32 W	6.79 W
P_{SW}	73.37 W	80.79 W
P_G	22.92 μ W	83.08 μ W
P_{off}	1.32 mW	30.14 mW
$P_{GAN} = P_{Cond} + P_{SW} + P_G + P_{off}$	79.69 W	87.61 W
P_{lost}	80.78 W	88.70 W
$P_{in} = P_{lost} + P_{out}$	2080.78 W	2088.70 W
$\eta = \frac{P_{out}}{P_{in}}$	96.11 %	95.75 %

The total power losses estimation before and after aging of the GaN HEMT 200 V / 24 V DC-DC buck converter for various output currents: 10 A, 12 A and 14 A are shown in **Fig. 5.20**. The average increase in the total power losses after aging has been estimated to be equal to 8.26 %.

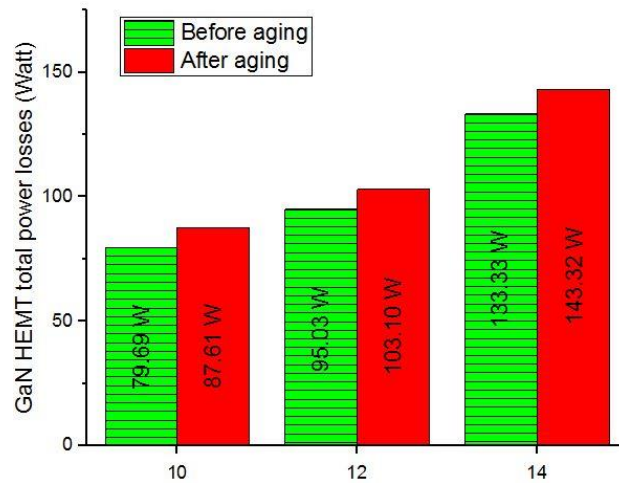


Fig. 5.20: GaN HEMT total power losses of DC-DC buck converter before and after 720 h of aging for various output current: 10 A, 12 A and 14 A.

5.8. Conclusion

This chapter investigates the reliability of power GaN HEMT under operational switching conditions, which could exist in a large class of power management products such as power converters. The switching conditions respect the safe operating area of the tested device given by the constructor, which provides a useful information about the degradation of GaN HEMT under use conditions. The proposed switching bench gives an efficient way with low power consumption to study the reliability of power GaN HEMT under switching conditions. The aging campaign lasted 720 h and it has resulted on a degradation of both the static and dynamic characteristics of the device which is attributed to the hot electron generated during the switching state. The major causes that affect the reliability of the GaN HEMT are hard switching, long time of test and high intensity of the stress. The existence of trapped charge in the gate-drain access region after aging is experimentally demonstrated by pulsing from various quiescent voltages. Moreover, we studied the effect of aging GaN HEMT on the efficiency of a DC-DC power converter by a simulation approach. It is found that the aged devices result in decreased performances of power converters.

5.9. References

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Chapter 6: Summary, conclusions and future work

6.1 Summary

This work explores the impact of aging the GaN HEMTs under operational switching conditions on the efficiency of DC-DC power converters.

As reported in chapter 1, the GaN HEMTs combine in one technology high voltage capability, large current and both high operational frequency and temperature. These features make the GaN HEMT highly suitable for power switching applications.

The state of the art of the GaN HEMT power transistors has been presented in Chapter 2. As reported in this chapter, the GaN HEMT devices satisfy the requirements of the power converter market for a high operating voltage, high operating current, high power density, high switching frequency, and strong reliability, which makes the GaN technology an attractive candidate for replacing Si devices in power applications. The physical properties of the GaN semiconductor enables both high-speed and high-voltage performances. The p-GaN HEMT normally-off structure is finding wide consensus within the scientific and industrial communities. For that, we have investigated the main issues related to the aging of these devices. Finally, the SPICE modeling approach enables the estimation of the GaN HEMT power losses with high accuracy.

In chapter 3, an experimental method is used to estimate the power losses of the GaN HEMTs in switching applications. The proposed approach is based on experimental I-V pulsed, C-V and low current characterizations. As a result of this study, both the static and dynamic power losses of the GaN HEMT are estimated. The impact of the conduction power losses, switching power losses and gate power losses on the efficiency of power converters are modelled using SPICE simulation approach. The accuracy and good convergence of simulation to experimental measurements provide a good way to design power converters with GaN HEMTs. Moreover, this approach offers to the power converter designers the possibility to estimate the power losses of GaN HEMT with high accuracy without the use of complex switching bench, which reduces both the time to market and cost.

In chapter 4, an accurate methodology based on an accurate S-parameters calibration procedure has been proposed to determine parasitic resistances, inductances, and capacitances of a packaged GaN power transistor. The obtained results show the possibility to extract very low device parasitic inductances which may influence switching mechanisms in power converters. Good agreement has been found between extracted values and technical data provided in the literature. Moreover, modeling equations are proposed for the nonlinear model parameters. The proposed method has the capability to be applied to any packaged GaN power transistor fabricated by different manufacturers. Furthermore, the method offers the possibility to extend the characterization to devices that have two terminals, such as: commercial inductances, capacitances and resistances.

Chapter 5 has investigated the reliability of GaN HEMT power transistor under operational switching conditions, which could exist in a large class of power management products such as power converters. The switching conditions respect the safe operating area of the tested device given by the constructor, which provide a useful information about the degradation of GaN HEMT transistor under use conditions. The proposed switching bench gives an efficient way to

study the reliability of power GaN HEMT under switching conditions. The aging campaign lasted 720 h and it has resulted on a degradation of both the static and dynamic characteristics of the device which is attributed to the hot electron generated during the switching state. The major causes that affect the reliability of the GaN HEMT are hard switching, long time of test and high intensity of the stress. The existence of trapped charge in the gate-drain access region after aging is experimentally demonstrated by pulsing from various quiescent voltages. Moreover, we studied the effect of aging GaN HEMT on the efficiency of a DC-DC power converter by a simulation approach. It is found that the aged devices result in decreased performances of power converters.

6.2 Conclusion

This work investigates the reliability of the GaN HEMT power transistor under operational switching conditions, which could exist in a large class of power converter applications. The switching conditions respect the safe operating area of the tested device given by the constructor, which provide a useful information about the degradation of GaN HEMT under safe optional conditions. The proposed switching bench gives an efficient way with low power consumption to study the reliability of power GaN HEMT under switching conditions. The aging campaigns lasted 1000 h and it has resulted on a degradation of the static parameters $R_{DS(ON)}$, g_m , I_D , V_{TH} and I_{GSS} which is attributed to the hot electron generated during the switching state. The existence of trapped charge in the gate-drain access region after aging is experimentally demonstrated by pulsing from various quiescent voltages. Additionally, we have monitored the evolution of the package parasitic elements during the aging of the GaN HEMT using the S-parameters method. The measurement of the S-parameters before and after aging shows the degradation of S12 and S21, which can be explained by the decrease of transconductance (g_m) and the increase of the gate to drain parasitic capacitance (C_{GD}). The change in the C_{GD} capacitance due to the trapped charges was confirmed by applying C-V measurement on the aged DUT. Using the proposed methodology in chapter 5 for the estimation of the GaN HEMT both static and dynamic power losses, we have studied the effect of aging GaN HEMT on the efficiency of a DC-DC power converter by a SPICE simulation approach.

6.3 Thesis contribution

The major contributions of this thesis are presented as follows:

- The developed methodology for estimating both the dynamic and static power losses of the GaN HEMT in power converter applications is accurate and based on experimental characterizations.
- The accuracy and consistent convergence of the developed SPICE model provide a good way to investigate the reliability of GaN HEMTs by a simulation approach.
- The developed experimental bench for S-parameters characterization enables the extraction of the parasitic elements of power devices automatically and at multi-bias.
- The extraction methodology of the intrinsic and extrinsic elements can be applied to a large class of power devices.
- Most existing studies investigate the reliability of the GaN HEMT at static conditions. This works investigates the aging of a 650V, 30A GaN HEMT power transistor under operational switching conditions of DC-DC power converters.

- The proposed aging bench enables to investigate the impact of aging the GaN HEMTs for both at high current and voltage and with low energy consumption.
- The presented modeling methodology of aging the GaN HEMT is generic and can be applied to other aging campaign for other components of various voltage ranges.
- The monitoring of the S parameters characteristic during aging enables to evaluate the impact of aging stress on the DUT packages.
- We have extended our investigation of the aging of GaN HEMT not only in static characteristics but also in the dynamic aspect.

6.4 Future work

As prospects for this study, the accuracy of the developed SPICE model can be improved by modelling of trapping effects and by modelling of dynamic characteristics in order to take into consideration the switching losses and the trapping effects when designing power converters using GaN HEMTs. Also, it is interesting to perform additional switching campaigns at various switching frequencies to study the effect of hard switching on GaN HEMT power converters. Moreover, the accuracy of the estimate efficiency can be completed by designing a DC-DC converter to calculate experimentally the impact of aging the GaN HEMT on the efficiency of power switching circuits using an experimental approach and compare it to the estimate efficiency using the SPICE approach.

List of publications and communications

Journal articles:

- **Al Mehdi Bouchour**, Ahmed El Oualkadi, Olivier Latry, Pascal Dherbecourt, Andres Echeverri. Estimation of losses of GaN HEMT in power switching applications based on experimental characterization. *Computers & Electrical Engineering*, 84, 106622. (2020)
- **Al Mehdi Bouchour**, Ahmed El Oualkadi, Pascal Dherbecourt, Olivier Latry, Andres Echeverri. Investigation of the aging of power GaN HEMT under operational switching conditions, impact on the power converters efficiency. *Microelectronics Reliability*, 100, 113403. (2019)

Peer reviewed international conferences:

- **Al Mehdi Bouchour**, Pascal Dherbecourt, Ahmed El Oualkadi, Olivier Latry. Parasitic Elements Extraction of the GaN HEMT Packaged Power Transistors based on S-parameter measurements. In 2020 International Symposium on Advanced Electrical and Communication Technologies (ISAECT) (pp. 1-6). IEEE. (2020).
- **Al Mehdi Bouchour**, Pascal Dherbecourt, Olivier Latry, Ahmed El Oualkadi. Temperature Effects of GaN HEMTs on the Design of Power Converters. In Third International Conference on Computing and Wireless Communication Systems, ICCWCS 2019. European Alliance for Innovation (EAI). (2019).
- **Al Mehdi Bouchour**, Ahmed El Oualkadi, Pascal Dherbecourt, Olivier Latry, Andres Echeverri. Investigation of the aging of power GaN HEMT under operational switching conditions, impact on the power converters efficiency. Poster presentation in the 30th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, ESREF 2019, in Toulouse (France) from September 23th to September 26th, (2019)
- Pascal Dherbecourt, Ahmed El Oualkadi, Eric Joubert, **Al Mehdi Bouchour**, Wadia Jouha, Mohamed Masmoudi, Olivier Latry. New Technologies of Power Transistors for Efficiency Increase of Power Converters: The Reliability Consideration. In ICCWCS 2019: Third International Conference on Computing and Wireless Communication Systems, ICCWCS 2019, April 24-25, 2019, Faculty of Sciences, Ibn Tofaïl University-Kénitra-Morocco (p. 131). European Alliance for Innovation. (2019).
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National communications:

- **Al Mehdi Bouchour**, Pascal Dherbecourt, Olivier Latry, Ahmed El Oualkadi, « Impact de la température et du vieillissement en conditions opérationnelles de fonctionnement sur les

transistors GaN HEMTs de puissance », Oral presentation in the « JDD'19 », UFR Sciences et Techniques, Saint Etienne du Rouvray (France), (2019).

- **Al Mehdi Bouchour**, Ahmed El Oualkadi, Pascal Dherbecourt, Olivier Latry « Etude et modélisation du comportement du GaN HEMT de puissance soumis à des contraintes thermiques et électriques », Poster in the « Ecole Thématique CNRS2019 », Fiabilité et Sûreté de Fonctionnement, FiabSurf 2019: Jun 17-21th, Saint-Pierre d'Oléron –France, 2019.