# MOSFETs SiC connectés en série : un nouveau concept de packaging et nouvelles configurations d'alimentation de commande rapprochée

Luciano Francisco Sousa Alves

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## Luciano FRANCISCO SOUSA ALVES


Thesis supervised by:
**Pierre LEFRANC,** Chair
**Pierre-Olivier JEANNIN,** Co-supervisor
**Benoît Sarrazin,** Co-supervisor

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# Series-Connected SiC-MOSFETs: A Novel Multi-Step Packaging Concept and New Gate Drive Power Supply Configurations

Thesis defended publicly «November, 5th 2020», in front of the jury composed by:

**M. Nadir IDIR**
Professor at Université de Lille, HDR, L2EP Laboratory: President
**M. Nicolas ROUGER**
Research Scientist, CNRS, HDR, Laplace Laboratory: Reviewer
**M. Cyril BUTTAY**
Research Scientist, CNRS, HDR, Ampère Laboratory: Reviewer
**M. Nicolas GINOT**
Professor at IUT Nantes, HDR, IETR Laboratory: Member
**M. Jean-Christophe CREBIER**
Research Scientist, CNRS, HDR, G2Elab laboratory: Member
**M. Pierre LEFRANC**
Associate Professor at Grenoble-INP, HDR: Supervisor
**Pierre-Olivier JEANNIN**
Associate Professor at UGA: Co-supervisor
**Benoît SARRAZIN**
Research engineer at Grenoble-INP: Co-supervisor

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## Luciano FRANCISCO SOUSA ALVES

Thèse dirigée par **Pierre LEFRANC** et
codirigée par **Pierre-Olivier JEANNIN** et **Benoît SARRAZIN**

préparée au sein du **Laboratoire de Génie Electrique de Grenoble (G2ELab)** dans **l'École Doctorale Electronique, Electrotechnique, Automatique et Traitement du Signal (EEATS)**

# Association en Série de MOSFETs SiC: Un Nouveau Concept de Packaging et Nouvelles Configurations d'Alimentation de Commande Rapprochée

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**M. Nadir IDIR**
Professor à l'Université de Lille, HDR, Laboratoire L2EP: Président
**M. Nicolas ROUGER**
Directeur de Recherche CNRS, HDR, Laboratoire LAPLACE: Rapporteur
**M. Cyril BUTTAY**
Directeur de Recherche CNRS, HDR, Laboratoire AMPERE: Rapporteur
**M. Nicolas GINOT**
Professeur à l'IUT de Nantes, HDR, Laboratoire IETR: Examinateur
**M. Jean-Christophe CREBIER**
Directeur de Recherche CNRS, HDR, Laboratoire G2Elab: Examinateur
**M. Pierre LEFRANC**
Maître de Conférences Grenoble-INP, HDR: Directeur de thèse
**Pierre-Olivier JEANNIN**
Maître de Conférences UGA: Co-encadrant
**Benoît SARRAZIN**
Ingénieur de Recherche Grenoble-INP: Co-encadrant

*The ultimate goal of science is to serve society.*

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# Abstract

This work investigates new gate drive power supply configurations and a novel multi-step packaging concept in order to improve the performances of series-connected SiC-MOSFETs. The new gate drive configurations are proposed in order to reduce noise currents that circulate in the control part of the electrical system. Furthermore, a new gate drive power supply is proposed to increase the $dv/dt$ of the switching cell. These improvements, i.e., noise current reduction and $dv/dt$ boosting, are achieved by modifying the impedance of the gate drive circuitry. The novel multi-step packaging concept is proposed in order to improve the voltage sharing performances. The proposed package geometry considers optimal dielectric isolation for each device leading to a multi-step geometry. It has a significant impact on the parasitic capacitances introduced by the packaging structure that are responsible for voltage unbalances. The new gate driver configurations and the proposed multi-step packaging concepts are introduced and analysed thanks to equivalent models and time domain simulations. Then, experimental set-ups are performed to confirm that the proposed concepts are better than traditional ones in terms of voltage balancing, switching speed and conducted EMI reduction.

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# Chapter 1
# General Introduction

## 1.1 Medium-Voltage High-Power Converter Applications

The energy transition with grid integration of distributed energy resources, motor drive systems, and data centers leads to new challenges for power generation, transmission and distribution. Hence, the medium-voltage grid and direct medium-voltage applications are becoming increasingly important. As shown in Fig. 1.1, medium-voltage high-power converters have great potential for a wide variety of medium-voltage applications, such as high-voltage direct current (HVDC), medium-voltage direct current (MVDC), smart/super/micro-grids, drives for electrical machines, medium-voltage pulse generators for plasma applications, etc [1].

The common characteristic of the mentioned applications is the search for maximizing the efficiency and output power capability of these critical systems, which can be achieved by increasing the blocking voltage of the devices or by increasing the converter output voltage. To this end, advancements in power electronic technology areas such as semiconductor devices and converter topologies have been investigated to improve the blocking voltage, power density, and efficiency, which can lower overall system cost and electricity consumption.

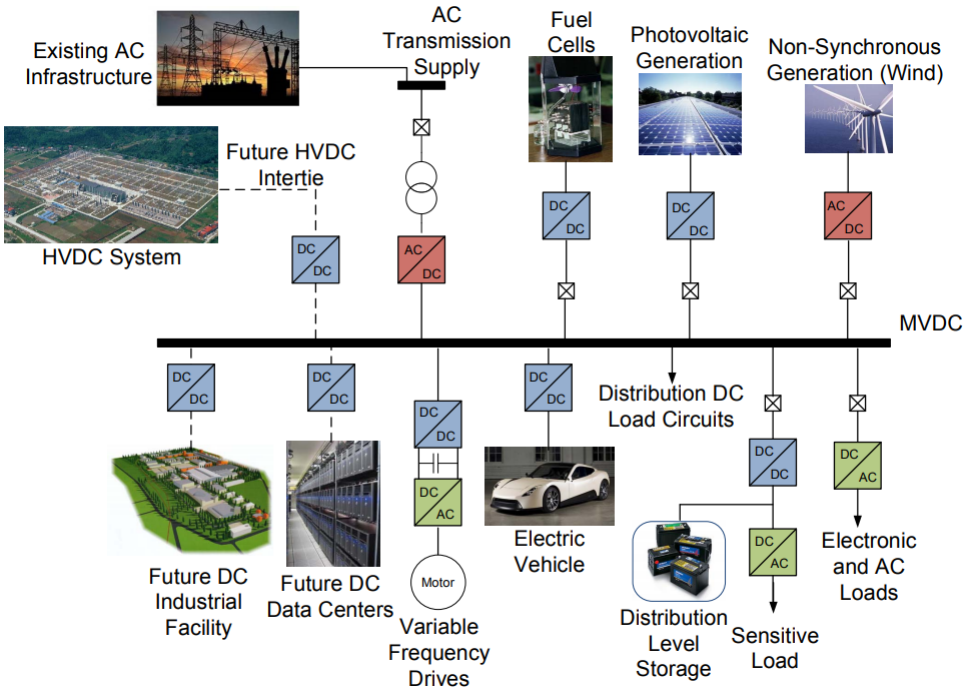



**Fig. 1.1.** Medium-voltage applications [1]

## 1.2 Methods for Achieving Higher Voltage Capability

### 1.2.1 Wide Band Gap Devices

Silicon (Si) power devices have dominated the world of power electronics in the last years, and they have proven to be efficient in a wide range of applications. But high power, high frequency and high temperature applications require more than Si can deliver. Wide Band-Gap (WBG) materials such as Silicon Carbide (SiC), Gallium Nitride (GaN), Gallium Oxide ($Ga_2O_3$) and diamond material have been intensively developed for power electronics applications due to the substantial advantages that their inherent material properties could realize at device level, such as high-breakdown voltage, high-operating electric field, high-operating temperature, high-switching frequency and low losses. In the last years, Silicon Carbide MOSFETs( Metal Oxide Semiconductor Field Effect Transistor) have started gaining significant importance in application areas of power electronics for medium-voltage, high efficiency, high switching frequencies and high temperatures applications. It is expected that the emergence of SiC-MOSFETs will allow power electronics to meet the increasing demand in utility or grid-scale applications [2]. However, today, the maximum voltage ratings of the existing commercial SiC-MOSFET are still only 1.7kV. Some higher voltage ratings, (10kV-15kV) SiC devices are tested in research laboratories [3,4]. Nowadays, series-connected and multi-level converter topologies are used to increase the blocking voltage capability for medium-voltage applications (up to 30 kV).

Maybe in the future, in the medium voltage range (up to 30 kV), WBG devices will be used to build compact and efficient power electronic converters without the need to use series-connected or multi-level converter topologies. However, it will open up new possibilities for series-connected and multi-level converter topologies in high-voltage applications over 30 kV. Single-phase and three-phase inverters will be operate directly at high and medium-voltage without the need to use a transformer.

### 1.2.2 Series-Connected Devices and Multi-level Converters

Series-connected devices and multilevel converter topologies are two effective ways of reaching higher voltage with low-voltage devices. Multilevel topologies offer outstanding features such as low common-mode voltage, low $dv/dt$ stress, and lower propagated electromagnetic interference [5]. On the other hand, using individual semiconductors in series will result in lower cost and higher efficiency. Furthermore, according to the study presented in [6], using two or more medium-voltage semiconductors in series features better on-resistance and higher current density than using a single higher voltage device. Therefore, series-connected SiC-MOSFETs is an effective way to increase the blocking voltage capabilities to answer application constraints above 1.7kV.

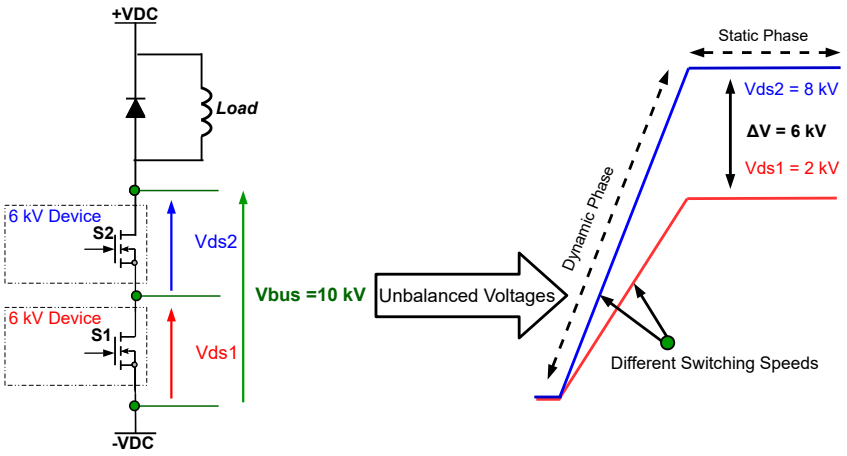



**Fig. 1.2.** Unbalanced voltages during dynamic and static phases.

## 1.3 Challenges of Series-Connected Devices

As explained in the previous section, using two or more medium-voltage semiconductors in series is an affective way of reaching higher breakdown voltage with low-voltage devices, which features better on-resistance and higher current density than using a single higher-voltage device. However, the two main problems related to the series association of power devices are the unequal voltage sharing among them, and the Common Mode current caused by the faster switching speed of the power devices. If these problems are not mitigated, it can result in damage to the switches in the stack and to the control system.

### 1.3.1 Voltage Balancing Problems

The majority of literature have attributed the unequal voltage sharing among stacked power devices to the tolerance in device parameters, package/layout parasitic components and gate signal timing delays [7–9]. If the device turn-off speeds are significantly different, the devices in the series stack that turn off faster will block more of the total dc bus voltage. For example, Fig. 1.2 shows two 6 kV series-connected devices operating under a 10 kV bus voltage. In an ideal case, the devices operate normally and safely, since during the turn-off switching each device blocks 5 kV. However, the drain-source voltages ($V_{ds1}$ and $V_{ds2}$) are unbalanced (dynamic and static phases) due to the causes mentioned above. In this case, the voltage $V_{ds2}$ across the device $S2$ exceeds its nominal value. Consequently, the device S2 could be damaged.

### 1.3.2 Common Mode Conducted EMI

The Common Mode (CM) currents that circulate in power converters can be divided in two categories: 1) the CM currents that circulate in the power part through the power

devices and the ground (through the dielectric barrier of the package) [10, 11], and 2) the CM currents that circulate in the control part through the isolation barriers of the DC-DC power supplies and signal transmission functions of the gate drivers [12,13]. Focusing on the second category, i.e., on the CM currents that circulate through the parasitic capacitances introduced by DC-DC power supplies and signal transmission functions of gate drivers, in Fig. 1.3 is defined the parasitic capacitance induced by the driver power supply, which is noted $C_{ps}$.

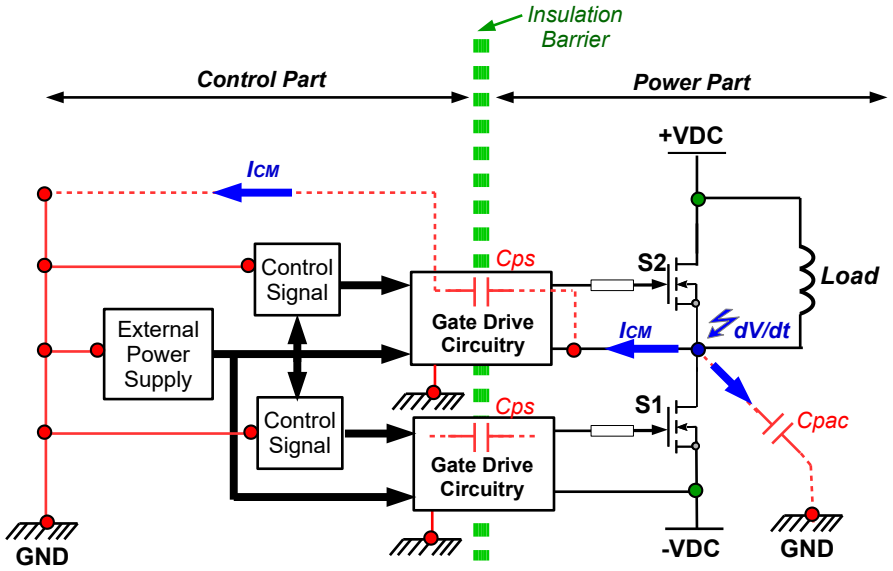



**Fig. 1.3.** Gate driver circuitry.

As can be seen, an isolated gate driver power supply is implemented in order to isolate the control part from the power part. However, isolated gate driver power supplies introduce primary to secondary parasitic capacitances ($C_{ps}$) due to the insulation barrier of the isolated DC-DC converters presented in the gate drive circuitry. As shown in Fig. 1.3, the gate driver parasitic capacitance ($C_{ps}$) has a direct connection to the middle point of the power leg that corresponds to a $dV/dt$ source. Therefore, as expressed by Eq. (1.1), the $dV/dt$ source generates CM currents that propagate to the control part through the parasitic capacitance $C_{ps}$.

$$I_{CM} = C_{ps}\frac{dV}{dt} \tag{1.1}$$

In series-connected device topologies, this problem is aggravated, since for N-devices connected in series, there are N-floating points that correspond to N-$dV/dt$ sources. Consequently, if several isolated power supplies in the driver circuitry are used, they will introduce several primary to secondary parasitic capacitances, and as a consequence several common mode currents will circulate in the control part, which can seriously disrupt and perhaps damage the system.

## 1.4 Research Motivation and Objectives

Based upon the motivations and technological challenges of series-connected devices presented in this chapter, this work proposes a comprehensive study and new solutions to solve the main problems related to the higher voltage capability achieved by series-connected low voltage SiC MOSFETs (1.2 kV nominal voltage rating per device) for medium-voltage converter applications.

In order to study the viability and effectiveness of a series-connected converter topology, one objective of this work is to propose, develop and test natural passive solutions, such new gate driver power supply and packaging configurations in order to reduce the CM current in the control side and voltage balancing problems. Finally, this research aims to investigate a novel active gate drive method in order to improve the voltage balancing across series-connected SiC-MOSFETs. To investigate the passive and active methods proposed in this work, voltage balancing, CM current reduction, and switching speed performance are experimentally tested up to four discrete 1.2 kV SiC MOSFETs in series under a total blocking voltage of 1 kV.

## 1.5 Thesis Organization

Based upon the research objectives described above, this thesis is organized as follows:

In **Chapter 2**, it is presented a comprehensive overview of series-connected SiC-MOSFETs. The factors that can influence the voltage sharing performance and the existent voltage balancing techniques are presented.

In **Chapter 3**, new gate drive power supply configurations are analysed in order to mitigate the conducted common mode (CM) currents in series-connected SiC-MOSFET applications. Furthermore, a new gate driver configuration is proposed in order to increase the $dv/dt$ of the switching cell middle point.

In **Chapter 4**, a Novel Multi-Step Packaging (MSP) concept for series-connected SiC-MOSFETs is analysed. The proposed package geometry considers optimal dielectric isolation for each device leading to a multi-step geometry. It has a significant impact on the parasitic capacitances introduced by the packaging structure that are responsible for voltage unbalances.

In **Chapter 5**, a novel active gate driver with a double active control is introduced. The proposed gate driver is based on the analysis of the state of the art presented in Chapter 2. The proposition is validated by numerical simulations. Some practical aspects are then proposed to go towards the experimental verifications.

# Chapter 2
# State-of-the-Art

In this chapter, a comprehensive overview of series-connected SiC-MOSFETs is presented. The fundamentals of the SiC-MOSFET and its switching process are essential for understanding the principles behind any natural voltage mismatch between series-connected devices. Then, an overview of factors that can influence voltage sharing performance and the existent voltage balancing techniques are discussed in the next sections.

## 2.1 Si, SiC, GaN, $Ga_2O_3$ and Diamond

In power electronics, improving the efficiency of electronic devices is crucial to reduce switching losses. Nowadays, Silicon (Si) is by far the most widely used semiconductor material for power devices. However, the intrinsic physical properties of silicon have limitations that in some domains will prevent devices based on Si material from being the candidates for the future of power electronics. As Si-based power devices are approaching their material limits, engineers and researchers have prompted a lot of efforts to find alternatives to Si-based power devices for better performances [14–16].

The search for a solution to the limitations of silicon leads to investigations of wide bandgap (WBG) semiconductors, such as Silicon Carbide (SiC), Gallium Nitride (GaN), Gallium Oxide ($Ga_2O_3$) and Diamond power devices.

Some semiconductors are classified as wide-bandgap semiconductors because of their wider bandgap. Silicon has a bandgap of 1.1 eV and is not considered as a wide bandgap semiconductor. The bandgaps of WBG semiconductors are about three times or more that of Si as can be seen in Table 2.1.

As shown in Fig. 2.1, WBG means larger breakdown field and high band gap. It results in power devices with higher breakdown voltage capabilities. With a high electric breakdown field, much higher doping levels can be achieved; thus, device layers can be made thinner at the same breakdown voltage levels. The resulting WBG semiconductor-based power have smaller drift region resistances. This means for the same breakdown voltage WBG devices offer significantly less on-resistance than Si-based devices [14, 15, 17–19].

The high-frequency switching capability or switching speed of a semiconductor is directly proportional to its drift velocity. The drift velocities of WBG materials are more than twice the drift velocity of Si; therefore, it is expected that WBG semiconductor-based power devices could be switched at higher frequencies than their Si counterparts. Moreover, higher

**Table 2.1**
Physical Properties of Silicon (Si), Silicon Carbide (4H-SiC), Gallium Nitride (GaN), $Ga_2O_3$, and Diamond [14–19].

| **Propriety** | Si | 4H-SiC | GaN | $Ga_2O_3$ | Diamond |
|---|---|---|---|---|---|
| Band Gap Energy ($eV$) | 1.1 | 3.2 | 3.4 | 4.7 | 5.50 |
| Breakdown Field ( $10^6$ $V/cm$) | 0.3 | 3.0 | 3.5 | 8.0 | 13.0 |
| Electron Mobility ($10^3$ $cm^2/V.s$) | 1.3 | 0.9 | 1.5 | 0.3 | 2.00 |
| Saturation Drift Velocity ($10^7$ $cm/s$) | 1.0 | 2.0 | 2.5 | 2.0 | 1.50 |
| Thermal Conductivity ($W/cm.k$) | 1.5 | 3.7 | 1.3 | 0.1 | 22.9 |

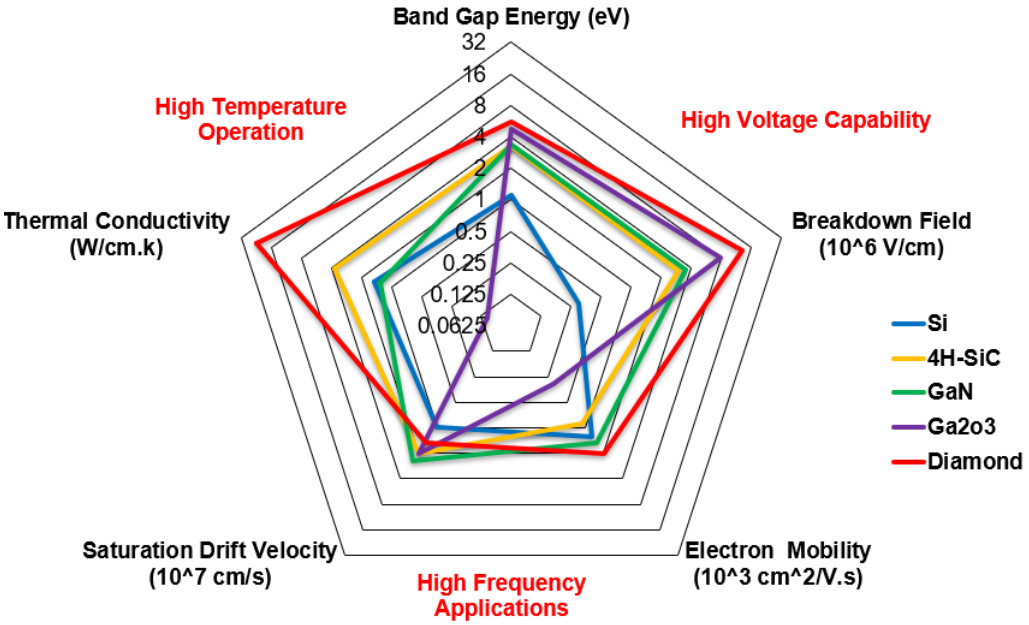



**Fig. 2.1.** Material properties comparison between Si, 4H-SiC, GaN, $Ga_2O_3$, and Diamond.

drift velocity allows charge in the depletion region of a diode to be removed faster; therefore, the reverse recovery current of WBG semiconductor based diodes is smaller, and the reverse recovery time is shorter [14, 15, 17–19].

WBG semiconductors have the advantage of high-temperature operation and more radiation hardening. As the temperature increases, the thermal energy of the electrons in the valence band increases. At a certain temperature, they have sufficient energy to move to the conduction band. This is an uncontrolled conduction that must be avoided. The temperature at which this happens is around 150°C for Si [15]. For WBG semiconductors, the bandgap energy is higher; therefore, electrons in the valence band need more thermal energy to move to the conduction band. For example, this intrinsic temperature for SiC is around 900°C. As a result, WBG semiconductors can withstand more heat and radiation without

losing their electrical characteristics. In other words, they can be used in extreme conditions where Si-based devices cannot be used.

Among the presented wide bandgap semiconductor, in the mid power range application field, GaN devices offer a higher break down field than Si devices and a better high frequency performance. The current GaN devices market is mainly dominated by devices less than 200V. 600V GaN devices are expected to take off and keep growing. While SiC is used for high-voltage applications, GaN is mainly used for low voltage.

The $Ga_2O_3$ is a currently hardly recognized wide bandgap semiconductor for power electronic application. It targets the mid to high power range. Its future development is still uncertain. Compared to SiC, the lower heat conductivity of $Ga_2O_3$ is a drawback [20].

Diamond is the wide bandgap semiconductor with the best physical properties in almost every sense with respect to power electronics. Although Diamond technology is more developed than $Ga_2O_3$, Diamond is still in maturation process [21]. Maybe in future high power applications that push all power densities and operation voltages to the upper limit, the semiconductor diamond would be the best choice.

SiC devices already offer a mature device processing technology. Its major application lies in the field of high power electronics where reliability plays a major role. In the last years, SiC-MOSFETs have been used in medium-voltage applications due to its higher voltage capability and switching performances. Nowadays, SiC-MOSFETs are the best candidate to replace Si-based IGBTs in the medium-voltage high-power converter applications [14].

## 2.2 Silicon Carbide MOSFETs

When switch mode operation of the SiC-MOSFET is considered, the goal is to switch between the ON and OFF states of the device in the shortest time possible in order to reduce switching losses. Since the practical switching times of the SiC-MOSFETs are very fast, a very small discrepancy between the switching speed of the series-connected SiC-MOSFETs can generate considerable voltage balancing problems. Therefore, to better understand the voltage sharing behaviour across the series-connected devices, it is important to understand the SiC-MOSFET fundamentals.

In Fig. 2.2 is shown a model that represents a SiC-MOSFET. As can be seen, it includes three capacitors connected between the three terminals of the device. Two of these capacitors, the $C_{gs}$ and $C_{gd}$ capacitors correspond to the actual geometry of the device while the $C_{ds}$ capacitor is the capacitance of the drain source diode of the transistor (body diode). None of the above mentioned capacitance values are defined directly in the transistor data sheets. Their values are given indirectly by the input capacitance ($C_{iss}$), reverse transfer capacitance ($C_{rss}$), and output capacitance ($C_{oss}$) values and must be calculated as shown in Eqs. (2.1),

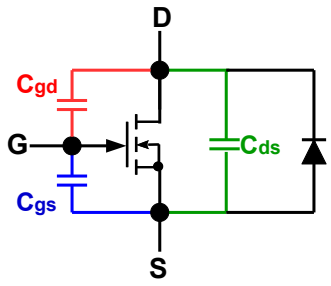



**Fig. 2.2.** SiC-MOSFET device model.

(2.2) and (2.3), respectively. Ultimately, the switching performance of the transistor is determined by how quickly the voltages can be changed across these capacitors.

$$C_{iss} = C_{gd} + C_{gs} \tag{2.1}$$

$$C_{rss} = C_{gd} \tag{2.2}$$

$$C_{oss} = C_{gd} + C_{ds} \tag{2.3}$$

The turn-ON/OFF procedures for Si and SiC MOSFETs are similar. However, there are some important specific characteristics of the SiC-MOSFETs that have to be taken into account, especially for switching control optimization and calculation methods for switching losses.

### 2.2.1 Turn-ON Procedure

The turn-ON event of the SiC-MOSFET can be divided into four intervals as depicted in Fig. 2.3.

**Time-interval 1:** in the first step, the input capacitance of the device is charged from 0 V to $V_{TH}$. During this interval most of the gate current is charging the $C_{gs}$ capacitor. A small current is flowing through the $C_{gd}$ capacitor, too. As the voltage increases at the gate terminal, the voltage across $C_{gd}$ has to be slightly reduced. This period is called the turn-on delay, because both the drain current and the drain voltage of the device remain unchanged [22, 23].

**Time-interval 2:** once the gate is charged to the threshold level ($V_{th}$), the drain current starts to conduct through the SiC-MOSFET. More current continues to rise through the SiC-MOSFET as $V_{gs}$ increases. The SiC-MOSFET is in the saturation region during this period since $V_{ds}$ is still blocking voltage [22, 23].

**Time-interval 3:** entering into the third period of the turn-on procedure the gate is already charged to the sufficient voltage ($Vplateau$) to carry the entire load current and the rectifier diode is turned off. That now allows the drain voltage to fall. Almost all the gate

current available from the driver is diverted to discharge the $C_{gd}$ capacitor to facilitate the rapid voltage change across the drain-to-source terminals. The drain current of the device stays constant since it is now limited by the DC current source [22, 23].

**Miller-plateau:** as shown in Figs. 2.3 and 2.4, an important characteristic feature of few SiC-MOSFETs is their non-flat miller plateau voltage as observed in typical silicon MOSFETs and IGBTs, which means the gate-source voltage of the SiC-MOSFET changes during the drain-source voltage fall and rise transitions instead of remaining constant. This is due to the low transconductance ($g_m$) of SiC-MOSFETs [24]. In other words, a relatively small amount of gate voltage is needed to cause a large change in the drain current.

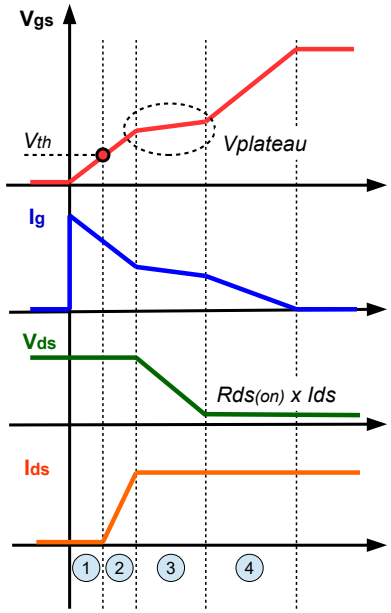



**Fig. 2.3.** Ideal turn-ON process for SiC-MOSFETs.

**Time-interval 4:** the last stage of the turn-on is to fully enhance the conducting channel of the SiC-MOSFET by applying a higher gate drive voltage. The final amplitude of $V_{gs}$ determines the ultimate on-resistance of the device during its on-time. Therefore, in this fourth interval, $V_{gs}$ is increased from $Vplateau$ to its final value. This is accomplished by charging the $C_{gs}$ and $C_{gd}$ capacitors, thus gate current is now split between the two components. While these capacitors are being charged, the drain current is still constant, and the drain-to-source voltage is slightly decreasing as the on-resistance of the device is being reduced [22, 23]. A drop voltage ($R_{ds(on)}.I_{DS}$) across the drain to source terminals is still present due the specific on-resistance.

### 2.2.2 Turn-OFF Procedure

As shown in Fig. 2.4, the description of turn-off procedure for the SiC-MOSFET transistor is similar to the turn-on steps.

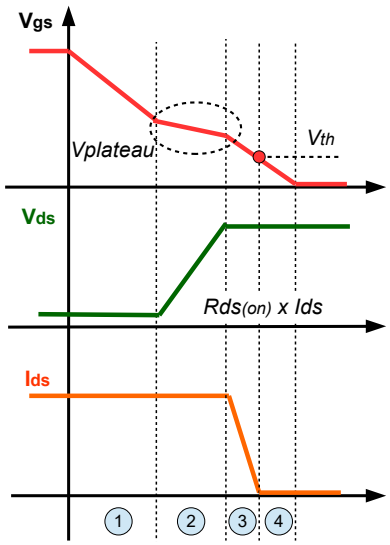



**Fig. 2.4.** Ideal turn-OFF process for SiC-MOSFETs.

**Time-interval 1:** the first time interval is required to discharge the $C_{iss}$ capacitance from its initial value to the Miller plateau level. During this time, the gate current is supplied by the $C_{iss}$ capacitor itself and it is flowing through the $C_{gs}$ and $C_{gd}$ capacitors of the SiC-MOSFET [22, 23].

**Time-interval 2:** during this time period, which corresponds to the Miller plateau in the gate voltage waveform, the $V_{ds}$ voltage rises from $R_{ds(on)}.I_{DS}$ to the final value of $V_{ds}$. The drain current of the device remain unchanged [22, 23].

**Miller-plateau:** it is important to highlight once again that an important characteristic feature of few SiC MOSFETs is their non-flat miller plateau voltage, which means the gate-source voltage of the SiC-MOSFET changes during the drain-source voltage fall and rise transitions instead of remaining constant [24].

**Time-interval 3:** the beginning of the third time interval is signified by the turn-on of the diode, thus providing an alternative path to the load current. The gate voltage resumes falling from $Vplateau$ to $V_{TH}$. The SiC-MOSFET is in linear operation and the declining gate-to-source voltage causes the drain current to decrease and reach near zero by the end of this interval [22, 23].

**Time-interval 4:** the last step of the turn-off procedure is to fully discharge the input capacitors of the device. $V_{gs}$ is further reduced until it reaches 0 V. The drain current and the drain voltage in the device are unchanged [22, 23].

As can be seen, the SiC-MOSFET switching behaviour is a function of the parasitic capacitance values, the required voltage change across them and the available gate drive current. This emphasizes that, in a switching cell with series-connected SiC-MOSFETs, even a very small discrepancy between the device characteristics can drastically impacts

the switching speed behaviour of each SiC-MOSFET, and consequently, the voltage sharing among them.

### 2.2.3 SiC-MOSFETs: Important Characteristics

**Gate-to-source voltage**: SiC-MOSFETs have a relatively low transconductance compared to Si-MOSFETs. The result is a higher gate-to-source voltage required to achieve the lowest $V_{ds}$ saturation voltage at high drain current. Si-MOSFETs achieve low $V_{ds}$ saturation at 8 V to 10 V on the gate to source. On the other hand, SiC-MOSFETs typically require a $V_{gs}$ voltage between 15 V to 20 V to achieve low $V_{ds}$ saturation. The turn-on threshold voltage of SiC-MOSFETs requires larger $V_{gs}$ transition when the SiC-MOSFET is operating as a variable resistance. The fast switching speed and low turn-on threshold of SiC-MOSFETs require a negative $V_{gs}$ level during turn-off. Depending on the device, -2 V to -5 V drive is recommended for SiC devices. Although the SiC-MOSFET parasitic $C_{gd}$ is very low, the high $V_{ds}$ $dV/dt$ during turn-off can result in coupling enough charge from the drain-to-gate capacitance to reach the threshold voltage if negative drive is not in place [14, 15].

**Shift in threshold voltage**: the good stability of gate threshold voltage, when positive gate voltage is applied for an extended period of time is an attractive feature of the SiC-MOSFET. The shift in threshold voltage is very small and it remains stable after several hours. However, when continuous negative voltage is applied to the gate for an extended period of time, the threshold shift can be larger than that caused by positive gate voltage, e.g., the threshold drops by 0.5V or more. In other words, extensive negative gate voltage can cause a significant drop in the threshold as can be seen in Fig. 2.5, where a ROHM Semiconductor SiC-MOSFET was submitted to different negative gate-to-source voltages [14, 25]. This characteristic varies from one SiC device to another.

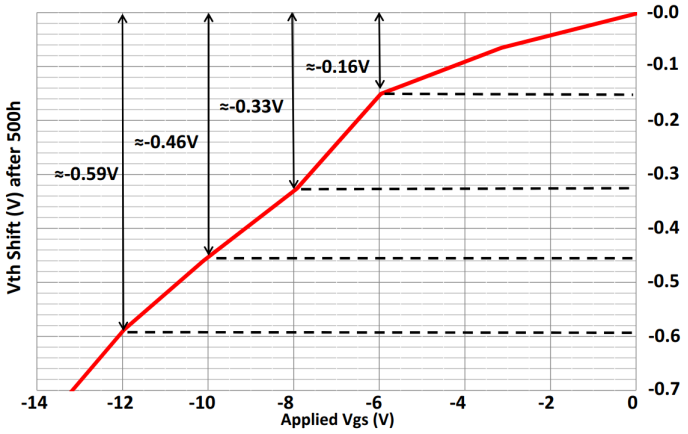



**Fig. 2.5.** Behavior of Vth = f(Vgs) after 500h of operation [14, 25].

$V_{ds}$-$I_{ds}$ **characteristics**: another characteristic of SiC-MOSFET devices is their no threshold voltage (knee) compared to IGBT devices, and their low conduction loss throughout

the entire current range when compared to Si-devices. For example, as shown in Fig. 2.6, Si-MOSFET on-resistance at 150 °C is more than twice that at room temperature, whereas SiC-MOSFET on-resistance increases only at a relatively low rate. This positive characteristic facilitates the thermal design for SiC-MOSFETs and provides low on-resistance at high temperatures [25]. This characteristic varies from one SiC device to another.

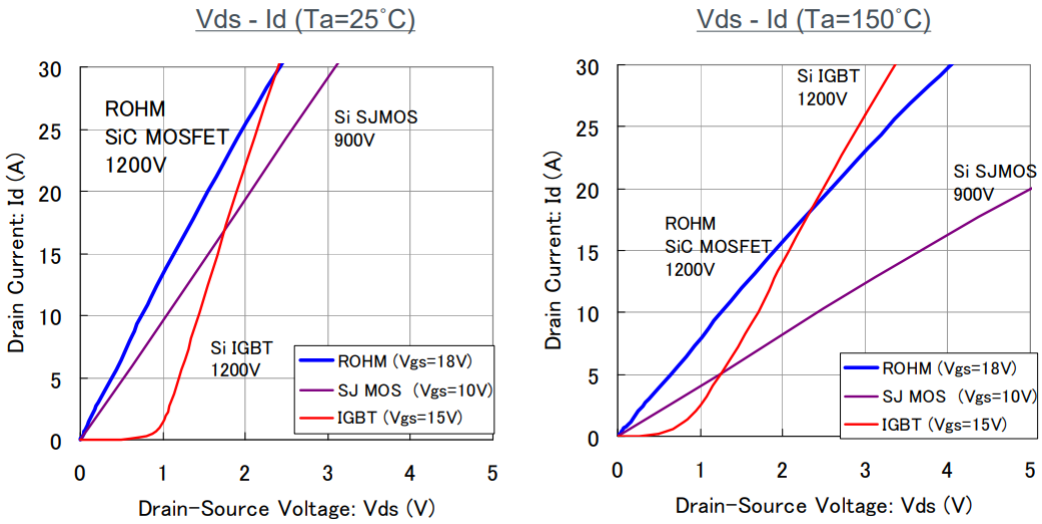



**Fig. 2.6.** $V_{ds} - I_{ds}$ characteristic for a SiC-MOSFET, Si-SJMOS and a Si-IGBT at 25 °C and 125 °C [25].

**Specific on-resistance**: SiC-MOSFET is an attractive device especially for medium power applications due to its lower conduction resistance compared to Si-MOSFET, its higher switching speed and its ability to operate at elevated temperatures [26]. In Fig. 2.7 is shown the comparison between Si and SiC-MOSFETs in terms of the specific on-resistance as a function of the breakdown voltage. The body diode of the SiC-MOSFET is a PiN diode that has 3V forward voltage drop, about 5 times that of a Si PN junction diode. However, the reverse recovery time is much smaller compared to a Si PN diode [27].

SiC-MOSFET devices present excellent characteristics and performances to be implemented in medium-voltage power converters. However, fast switching in high voltage applications may cause considerable surge voltages, spike currents, high-frequency leakage currents, and various electromagnetic interference (EMI) issues, due to high $dV/dt$ and/or $di/dt$.

In series-connected SiC-MOSFET topologies, these problems are also present. Voltage balancing and EMI reduction methods applied to Si-MOSFETs/Si-IGBTs in series require new considerations for series-connected SiC-MOSFETs.

## 2.3 Series-Connected SiC-MOSFETs

Series connection is an attractive way of reaching higher breakdown voltage with low-voltage devices as shown in Fig. 2.8, where two devices are connected in series, and driven

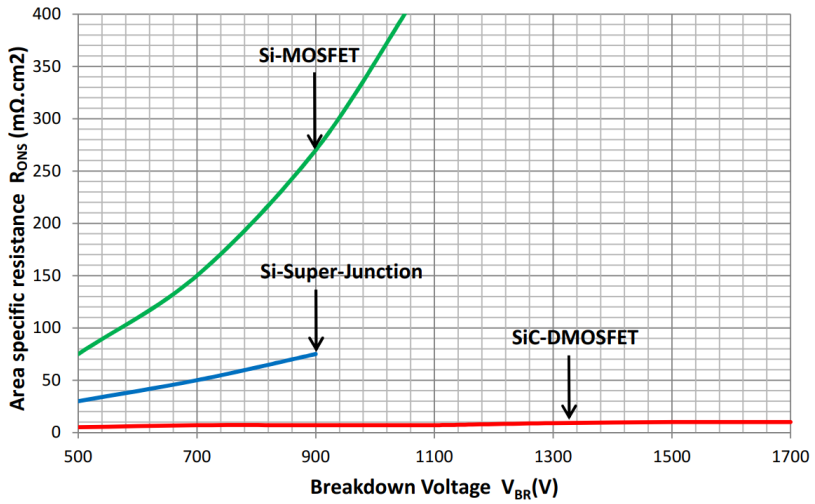



**Fig. 2.7.** On-resistance comparison between Si-MOSFET, Si-Super-Junction and SiC-DMOSFET [26].

by the same gate signal timing. As can be seen, the two devices operate as a single device, which has a total blocking voltage $V_{ds} = V_{ds1} + V_{ds2}$. Note that, the $V_{ds1}$ and $V_{ds2}$ voltages are perfectly balanced.

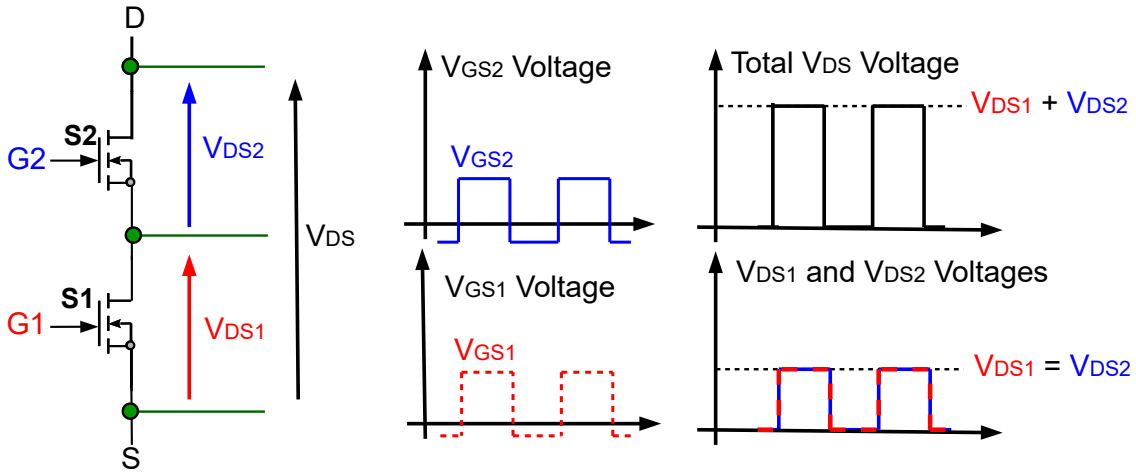



**Fig. 2.8.** Two series-connected SiC-MOSFETs operated as a single switch.

The basic principle shown in Fig. 2.8 is a completely ideal case scenario of two series-connected devices without mismatch between device leakage currents, device parameter tolerances, package and layout parasitic components, and gate signal timing delays [28–30]. In real experiments, these problems are present, which generate voltage balancing problems as shown in Fig. 2.9.

The unbalanced voltage problem during the static phase can be easily solved by placing a static resistor in parallel with each device at the drain-to-source terminals. However, some considerations have to be taken into account in the static resistor design:

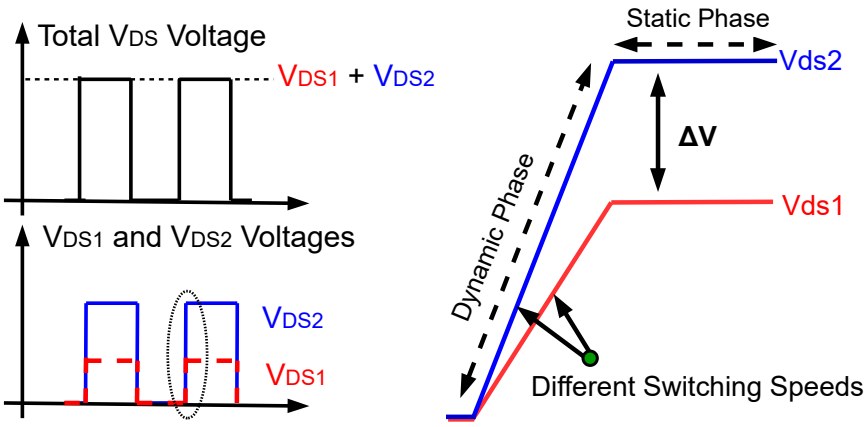



**Fig. 2.9.** Voltage Balancing Problem.

- The current through the static resistor has to be very dominant when compared to the maximum leakage current of the device provided in the device's datasheet. Otherwise, the resistor has no influence on voltage balancing.
- The switching period for the series-connected MOSFETs has to be very predominant when compared to the time constant of the parallel association between each device's output capacitance $C_{oss}$ and the static resistors. Otherwise, the $V_{ds}$ voltage of each devices will not reach the ideal static voltage before the end of the switching period.
- The power dissipation of each resistor placed in parallel with each device needs to be considered.

As mentioned, the voltage balancing problems during the dynamic switching can be caused by several different factors, such mismatched device parameter tolerances, package and layout parasitic components, and gate signal timing delays. Unlike the static phase, the dynamic phase requires more complex methods to ensure acceptable voltage sharing across the series-connected devices.

### 2.3.1 Device Parameter Tolerances, Package and Layout Parasitic Components

In Fig. 2.10 is shown an electrical scheme for two series-connected devices. The main elements that contribute to voltage balancing problems are presented as follows (for $i = 1, 2$):

- The intrinsic parasitic capacitances of the devices: $C_{gdi}$, $C_{gsi}$ and $C_{dsi}$.
- The gate resistances: $R_{gi}$.
- The gate drive voltages: $V_{dri}$.

- The parasitic capacitances introduced by the gate drive circuitry: $C_{psi}$.
- The parasitic capacitances of the packaging : $C_{paci}$.

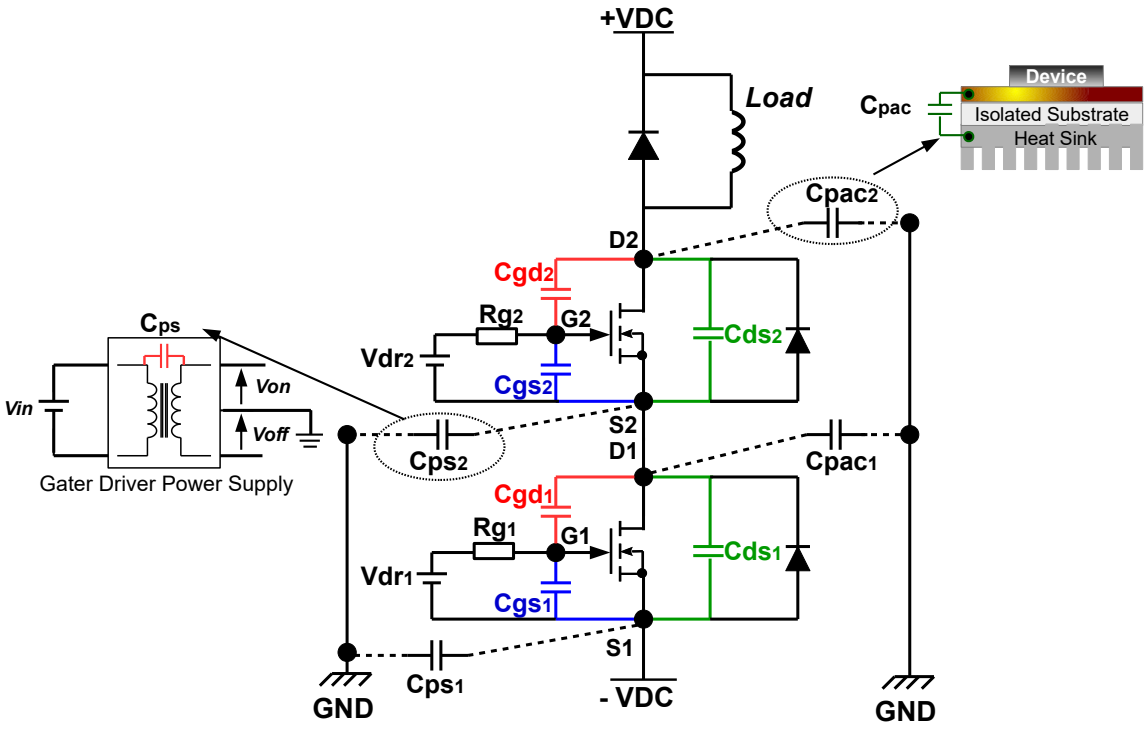



**Fig. 2.10.** Two series-connected SiC-MOSFETs and their parasitic elements.

Regarding Fig. 2.10, a simplification allows better understanding the causes of unbalanced voltages across the series-connected devices. As shown in Fig. 2.11, the parasitic capacitances shown in Fig. 2.10 can be reduced to three equivalent capacitors [31], which are expressed by Eqs. (2.4), (2.5) and (2.6). Note that, to facilitate the analysis, the gate behavior is not taken into account.

$$C_{eq1} = \frac{C_{gs1}.C_{gd1}}{C_{gs1} + C_{gd1}} + C_{ds1} + C_{pac1} + C_{ps2} \tag{2.4}$$

$$C_{eq2} = \frac{C_{gs2}.C_{gd2}}{C_{gs2} + C_{gd2}} + C_{ds2} \tag{2.5}$$

$$C_{eq3} = C_{pac2} \tag{2.6}$$

The capacitor current $I_{ceqi}$ is a function of the load current and gate driver $i$ ($V_{gsi}$ and $R_{gi}$), for $i$=1,2. Therefore, supposing that the gate drivers are identical, and the current $I_{ceq1}$ is equal to the current $I_{ceq2}$, the following equations can be written:

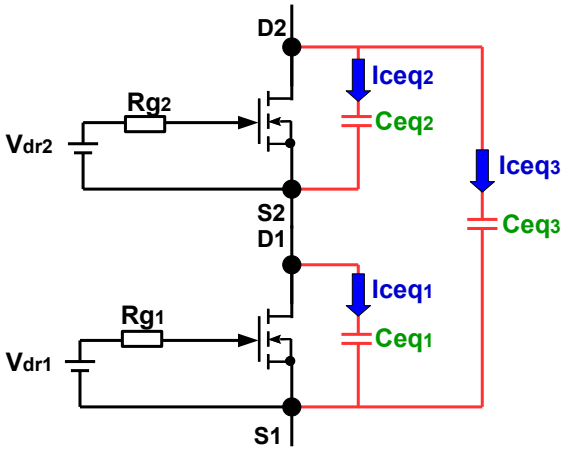



**Fig. 2.11.** Equivalent electrical scheme of two series-connected SiC-MOSFETs and their parasitic elements.

$$\frac{d_{Vds2}}{dt}.C_{eq2} = \frac{d_{Vds1}}{dt}.C_{eq1} \tag{2.7}$$

$$\frac{d_{Vds2}}{dt}.\left(\frac{C_{gs2}.C_{gd2}}{C_{gs2}+C_{gd2}} + C_{ds2}\right) = \frac{d_{Vds1}}{dt}.\left(\frac{C_{gs1}.C_{gd1}}{C_{gs1}+C_{gd1}} + C_{ds1} + C_{pac1} + C_{ps2}\right) \tag{2.8}$$

As can be seen in Eq. (2.8), the series-connected devices have different $dv/dt$ behaviours, which generate unbalanced voltages. Even though the gate drivers are perfectly identical, and there is no mismatch between the intrinsic capacitances of the devices, they have different switching speeds due the packaging/layout parasitic capacitance $C_{pac1}$, and the gate drive circuitry parasitic capacitance $C_{ps2}$. In other words, according to Eq. (2.8), the only way to achieve perfectly balanced voltages (without any compensation method) across the series-connected devices is to ensure that the following conditions are satisfied: 1) the series-connected devices have to be identical, and 2) the gate drivers/packaging/layout have to introduce no parasitic capacitances. In this case, the voltages across the devices will be perfectly balanced, unless there are gate signal timing delays, as it will be explained in the next section.

### 2.3.2 Gate Signal Timing Delays

When compared with Si-IGBTs, whose switching process lasts for several microseconds, SiC-MOSFET can finish its switching process within tens of nano-seconds [31]. However, the fast switching process means high voltage difference of $V_{ds}$ when time delay mismatch occurs between gate signals. Fig. 2.12 shows a hypothetical case where the series-connected devices have the same switching speed. However, as can be seen, the $V_{ds}$ voltages are unbalanced due the gate signal timing delays. In [32] is demonstrated that 20ns gate drive signal time

deviation of two SCT3120AL SiC-MOSFETs (650V, 21A) can trigger over 400V voltage difference under 800V DC bus voltage.

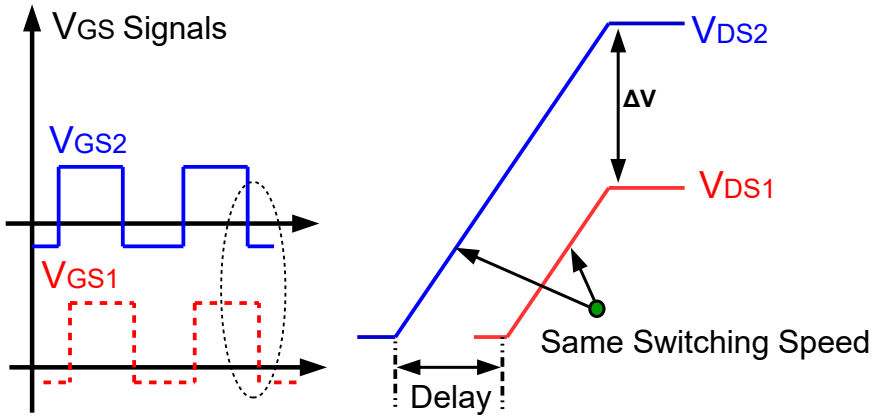



**Fig. 2.12.** Unbalanced voltage caused by gate signal timing delays.

In real experiments, all the previously mentioned causes of voltage balancing problems are present. The series-connected devices have different switching speeds and time delays between gate signals. Therefore, advanced techniques are required to mitigate voltage balancing problems in series-connected SiC-MOSFET topologies.

## 2.4 Voltage Balancing Techniques

Several voltage balancing techniques have been proposed in the literature. As shown in Fig.2.13, the most common voltage balancing methods are divided in four categories: passive snubber circuits [33–46], active voltage clamping [39, 47–49], natural self-balancing [8–10, 50, 51], and active gate control techniques [32, 45, 52–67].

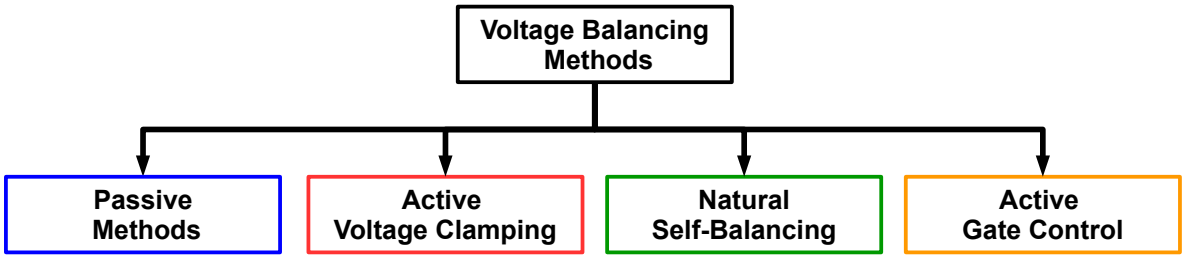



**Fig. 2.13.** Classical voltage balancing techniques.

### 2.4.1 Passive Methods

Passive voltage balancing techniques, such RC and RCD snubbers, have been developed for controlling the switching voltage transients of individual devices, and providing dynamic

voltage sharing within strings of series-connected power-semiconductors [68]. Passive snubber circuits are a common method applied for voltage balancing applications in industry due to its simple design and implementation.

In [33–35], a simple RC snubber method, as shown in Fig. 2.14(a), has been used for dynamic voltage sharing to offset the turn-off delays due to mismatch on device's characteristics and/or gate signals. Experimental switching characterizations with different values of RC snubbers are done using two 1.7 kV / 300 A series-connected SiC-MOSFET modules. The papers [33–35] propose a comprehensive characterization to find the optimal RC snubber which gives minimum voltage sharing difference, snubber losses and total semiconductor losses. The value of the snubber capacitor ($C_d$) has been selected to nullify the mismatch in the device output capacitances, and the resistance $R_d$ is selected such that the time constant of the $R_dC_d$ snubber is low enough to discharge the snubber capacitor during on time ($T_{on}$).

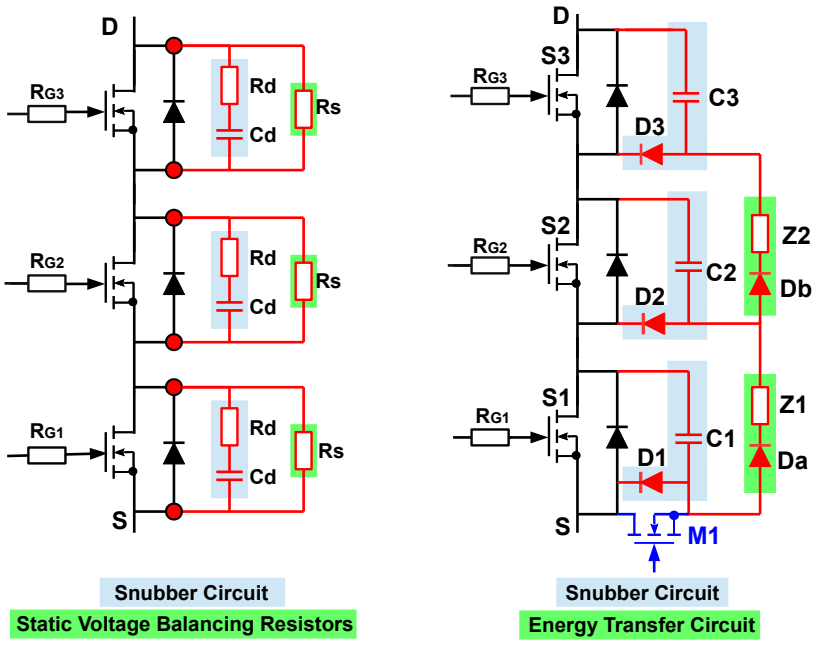



**Fig. 2.14.** Simple RC snubber method (a) [33–35] ,and snubber circuits with energy recovery capability (b) [38].

The contribution of the snubber capacitor ($C_d$) can be described as the following four functions:

- it reduces the unbalance in dynamic voltage sharing between the devices and the rate of rise of voltage across the series connected devices ($V_{ds}$) (during turn-off, $V_{ds}$ will be nearly equal between the devices, because the snubber capacitor $C_d$, is much larger than the device's output capacitance $C_{oss}$);
- it reduces the overall turn-off $dv/dt$ at the middle point of the switching cell;

- it contributes additional losses during turn-on, because the energy stored in the snubber capacitor during turn-off will be discharged in the series resistor ($R_S$) and in the device, hence the total switching losses in the device may increase compared to the switching losses without snubber.

Therefore, the optimum value of $R_dC_d$ snubber is the minimum value of $R_dC_d$ snubber value such that minimize the total switching losses in the device, and minimize differences in dynamic voltage sharing.

In [36, 37], a similar characterization is proposed with the same $RC$ snubber method. However, in [36], the study is a characterization and comparison between series-connected 15 kV SiC-IGBT devices and 15 kV SiC-MOSFET devices for medium-voltage power conversion systems. In [37] it is analyzed a detailed experimental switching characterization and continuous switching mode results for four 1.7 kV series-connected SiC-MOSFETs under a total block voltage of 3 kV. These comparison studies show that series-connected SiC-MOSFETs have significantly lower total loss compared to a single 6 kV Si-IGBT for the same current rating (78 A), and switching frequency higher 1kHz.

In Fig. 2.14(b) is shown a snubber circuit topology with energy recovery capability proposed in [38] to control the voltage sharing of three series-connected SiC-MOSFETs. The snubber circuits formed by $C_1$-$D_1$ ,$C_2$-$D_2$, and $C_3$-$D_3$ are parallel-connected across the SiC-MOSFETs. Auxiliary diodes (Da, Db) and current limiting devices ($Z_1$, $Z_2$) are also included in the proposed circuit to create energy transfer loops between different snubber capacitors. The snubber capacitors act as clamping devices in the circuit shown in Fig. 2.14(b). Whenever an over-voltage occurs across a SiC-MOSFET, its snubber diode conducts and its drain-source voltage will be clamped by the snubber capacitor. Nevertheless, the initial proposed snubber circuit can not balance the voltages across the snubber capacitors. In some conditions, the snubber capacitor voltages can rise gradually along with the switching cycles. In other words, the capacitor voltages can exceed the rated voltage of SiC MOSFETs. In order to solve this issue, the bottom snubber diode ($D_1$) is replaced by a full-controlled device ($M_1$). This improved structure provides the functions of discharging the snubber capacitors and recovering energy from snubber capacitors to the dc power supply. However, the improved snubber circuit needs a control algorithm to drive the device $M_1$ at appropriate times.

To reduce the components number and system complexity, series-connected device topologies using only one gate driver and several passive components were proposed [39–43]. In [40, 41], a compact circuit combining function of gate control and voltage balancing for series-connected SiC-MOSFETs using one standard gate driver is proposed. It uses the capacitive coupling structure technique to take advantage of the charge variation among the capacitor to achieve the driver signal control of upper side device. In other words,no auxiliary voltage sources are required to drive the upper devices and the dynamic voltages are

also balanced by snubber circuits. Fig. 2.15(a) shows the configuration of the proposed SiC switch based on two SiC-MOSFETs connected in series. Besides ensuring the static voltage sharing between two devices, the function of resistors R1 and R2 is to guarantee that the gate voltage of the SiC-MOSFET is negative. Similarly, the function of capacitors $C_1$ and $C_2$ is to combine the gate control of SiC-MOSFET S2 and the voltage sharing among S1 and S2 during switching transitions. Zener diodes $Z_{d3}$ and $Z_{d4}$ protect the gate voltage of S2 within the safe region and determine the voltage level of driving signal of S2 at the same time. Moreover, this topology costs less than the other direct driving methods considering that those methods require a separate high voltage isolated gate drive unit for every single power device. In [42] a similar method is presented. However, some modifications and improvements have been proposed, as Fig. 2.15(b) ( blue zone) shows; it is used for Solid-State Circuit Breaker (SSCB) applications. In brief, varistors $V_{ar1}$ and $V_{ar2}$ absorb the short circuit energy, and diode $D_1$ is added to the circuit to ensure S2 has reliable positive gate voltage.

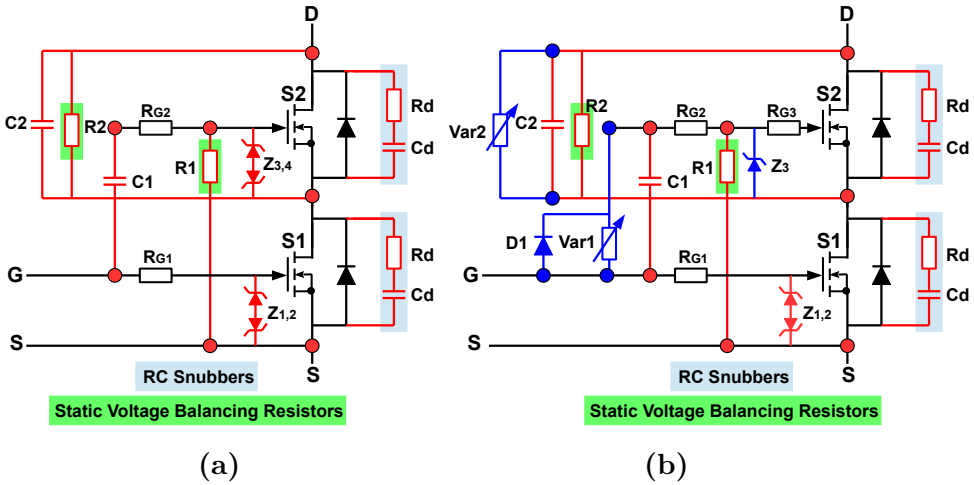



**Fig. 2.15.** Proposed series-connected topology (a) [40, 41], and its adaptation for SSCB application (b) [42].

In [44], layout considerations in terms of the electrical, thermal and insulation issues are proposed for a rated 9.6kV, 450A half-bridge module composed of eight series-connected 1.2kV SiC-MOSFETs. As shown in Fig. 2.16, a snubber realized by mutual inductance is proposed to reduced the voltage sharing mismatch across the series-connected devices. The main idea is to design an appropriate snubber layout to minimize the term $L_M - M$ in the eq. (2.9).

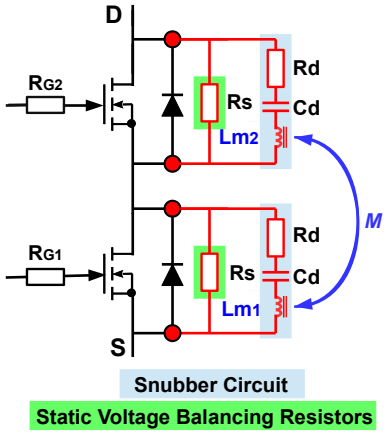



**Fig. 2.16.** Voltage balancing circuit realized by mutual inductance [44].

$$\Delta V_{ds} = (L_M - M).\frac{\Delta I_T}{dt} + \frac{1}{Cd}\int \Delta I_T.dt \tag{2.9}$$

Where $\Delta V_{ds}$ is the voltage difference between the series-connected devices, $\Delta I_T$ is the difference between the currents that flow through the snubber circuits, $L_M = L_{m1} = L_{m2}$ is the self-inductance, $M$ is the mutual inductance, and $Cd$ is the snubber capacitor.

As can be seen, passive voltage balancing methods is a simple way to achieve acceptable voltage sharing across the series-connected devices. However, in medium-voltage high-frequency applications, passive methods lead to high power loss due to the stress of higher $dv/dt$ rates on the passive components [69]. The cost and volume of the system can also be increased due the additional passive components in the snubber circuits.

### 2.4.2 Active Voltage Clamping

The main idea of active voltage clamping techniques is to clamp the $V_{gd}$ or $V_{ds}$ voltage at a reference voltage level in order to limit the $V_{ds}$ voltage across the device by acting on the gate-to-source voltage with a feedback from the drain side to the gate side. The most common clamping circuits are basically composed by capacitors, diodes and/or Zener diodes. In high-medium voltage applications, where the active clamping circuit operates, the voltage $V_{ds}$ can be expressed by Eq.(2.10).

$$V_{ds} = V_{gd} + V_{gs} = V_{Clamp} + V_{gs} \approx V_{Clamp} \tag{2.10}$$

According to Eq.(2.10), if a Zener diode, for example, is connected to gate-to-drain terminals, the $V_{ds}$ will be limited by the Zener diode voltage. In addition to the simplicity of implementation, another advantage of active voltage clamping techniques is the lack of complex analog-digital conversion circuitry and complex control system. However, if the

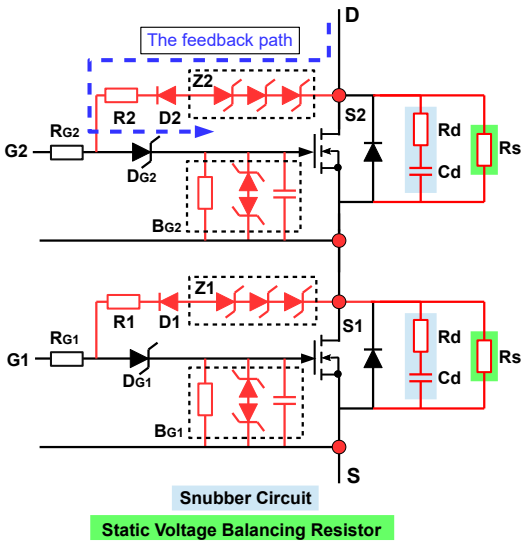



**Fig. 2.17.** Active voltage clamping method proposed in [47].

clamping circuit is not well designed, this could lead to unstable operating due to the feedback between drain and gate terminals.

In [47] is proposed a simple and reliable auxiliary active clamping circuit, which acts as a feedback on the gate terminal of series-connected SiC devices. The active clamping feedback circuit is shown in Fig. 2.17, which consists of several series-connected Zener diodes ($Z_i$), a current limiting resistor ($R_i$) and a diode ($D_i$), for i=1,2. The operation of the proposed circuit is quite simple; assuming that $V_{ds2}$ rises faster than $V_{ds1}$, when the voltage of S2 exceeds the clamping threshold value $V_Z$ ($V_{gd2} > V_{Z2}$), the series-connected Zener diodes ($Z_2$) break down, clamping $V_{ds2}$. In other word, when high voltage spike across the MOSFET exceeds the clamping voltage, the active clamping circuit conducts and injects current into the gate to prevent the MOSFETs turning off too quickly. In addition to the proposed clamp circuit, an additional RC snubber circuit is added to enable dynamic voltage balancing by limiting the $dv/dt$. The components in Fig. 2.17, such as $B_{Gi}$ and $D_{Gi}$ are used to protect/limit the $V_{gs}$ voltages and limit the value/direction of the gate current, respectively.

A similar active voltage clamping method for 1.2 kV series-connected bidirectional SiC-MOSFETs is proposed in [48] for Solid-State Circuit-Breaker(SSCB) applications. Bidirectional switches allow the SSCB to interrupt a fault current from both directions. As shown in Fig. 2.18, the active voltage clamping circuit consists of a few series-connected transient voltage suppressor diodes ($Z_1$-$Z_4$), regular diodes ($D_1$-$D_4$) and clamping resistors ($R_1$-$R_4$). The operation of the proposed circuit follows the basic idea; when the high voltage spike across the SiC-MOSFET exceeds the clamping voltage, the transient voltage suppressor (TVS) diodes clamp the $V_{gd}$ voltage to a reference level, and the clamp circuit conducts and injects current into the gate to prevent the SiC-MOSFET turning off too quickly. In Fig. 2.18, $R_S$

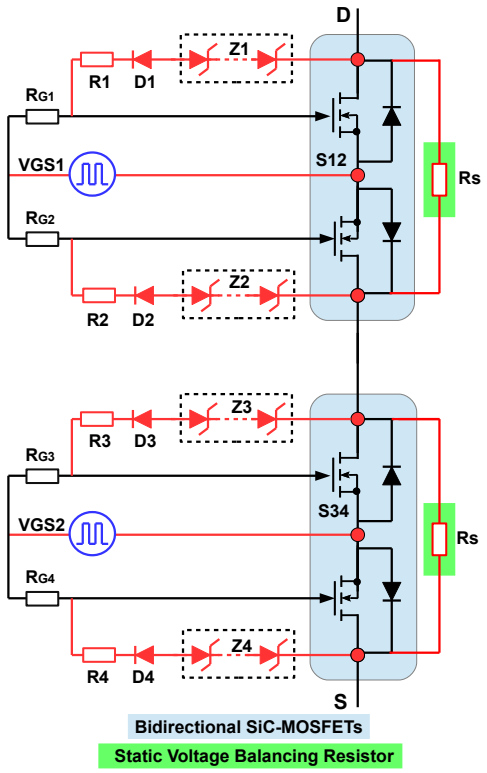



**Fig. 2.18.** Active voltage clamping method proposed in [48] for SSCB applications.

are parallel connected between the drain and source terminals for static voltage balancing, the diodes ($D_1$-$D_4$) are there to prevent current flow from gate to drain during the on state, and the resistors ($R_1$-$R_4$) limit the current through the ($Z_1$-$Z_4$) diodes to protect them from operating beyond their power rating.

Active voltage clamping is a simple technique to achieve voltage balancing across the series-connected SiC-MOSFETs. However, as explained in [48], the design of the clamp circuits requires special attention. In practice, three crucial criteria should be considered during the TVS diode selection process:

- The clamping voltage of the TVS diodes has to be lower than the breakdown voltage of the power devices.
- The response time of the TVS diode has to be fast enough to clamp $V_{ds}$ before it exceeds the device breakdown limit.
- The junction capacitance of the TVS diodes must be small enough in order to not decrease the switching speed of the devices.

The clamping voltage can be determined by Eq. (2.11) .

$$V_{ds}(Clamp) \approx V_Z + R_C.I_C \tag{2.11}$$

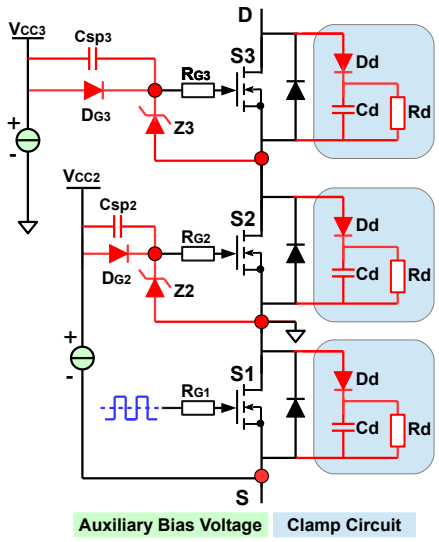



**Fig. 2.19.** Active voltage clamping method with a single external driver proposed in [39].

Where $V_{ds}(Clamp)$ is the total clamped voltage, $V_Z$i is the breakdown voltage of series-connected single diodes, and $I_C$ is the current that flows through the clamping resistor $R_C$.

In [39], a single external driver with a RCD voltage clamping is proposed to balance the $V_{ds}$ voltages of three series-parallel-connected SiC-MOSFETs. Fig. 2.19 shows the proposed circuit (the parallel branch circuit is not shown in Fig. 2.19). Each device has a corresponding RCD voltage clamping circuit used for both static and dynamic voltage balancing . The diode $D_d$ of each clamp part is a fast recovery diode used to clamp $V_{ds}$ to the voltage of the corresponding capacitor $C_d$, which is determined by the static voltage balancing ensured by the resistor $R_d$. The idea is quite simple; when a $V_{ds}$ voltage exceeds the voltage across the branch circuit $C_d//R_d$ (static voltage), the corresponding $D_d$ is directly polarized, and $V_{ds}$ is equal to the voltage of the capacitor $C_d$ clamping the voltage across the device.

Only the bottom device S1 needs an external gate driver. The upper devices (S2 and S3) require auxiliary bias voltages ($V_{CC2}$ for the middle row and $V_{CC3}$ for the top row) to provide power to drive the SiC-MOSFETs. The bias voltage $V_{CC2}$ is referred to the source terminal of S1, while $V_{CC3}$ is referred to the source terminal of S2. The single external gate drive technique takes advantage of the drain potential variation to drive the series-connected SiC-MOSFETs. For example, supposing all devices are off in Fig. 2.19, when a positive drive signal is given to the gate of the device S1, $V_{ds1}$ begins to decrease, and the potential variation on the drain terminal of the device S1 imposes the discharge of the $D_{G2}$ junction capacitance through $Z_2$. The voltages across $Z_2$ will gradually increase. When it reaches the $V_{TH}$ of the device S2, the switching process of S2 starts. In the same way, the switching process of S3 will be imposed by the drain terminal variation of the device S2. The capacitors $C_{sp3}$ and $C_{sp2}$ in Fig. 2.19 are speed-up capacitors used to optimize the switching speed of the devices.

In this kind of technique, i.e., single external drive technique, the series-connected devices

turn-on/off one after another, their transient voltages do not rise/fall at the same time (especially during the turn-off switching). It leads to different switching losses among the devices, which implies reliability and thermal issues. In any case, all three device voltages are clamped properly and the safe operation is guaranteed.

As can be seen, active voltage clamping methods are simple way to ensure an acceptable voltage sharing across the devices. However, the cost and volume of the system can be increased due the additional passive components in the clamp circuits. Moreover, some methods requires separate high-voltage rated auxiliary voltage sources to clamp each driving voltage at the desired voltage levels.

### 2.4.3 Natural Self-Balancing

The main idea of natural self-circuit methods is to use the parasitic capacitances of the switching cell to reduce the voltage unbalancing across the series-connected devices. In [50,51] a 3D packaging/layout was proposed for the first time for series-connected IGBTs.

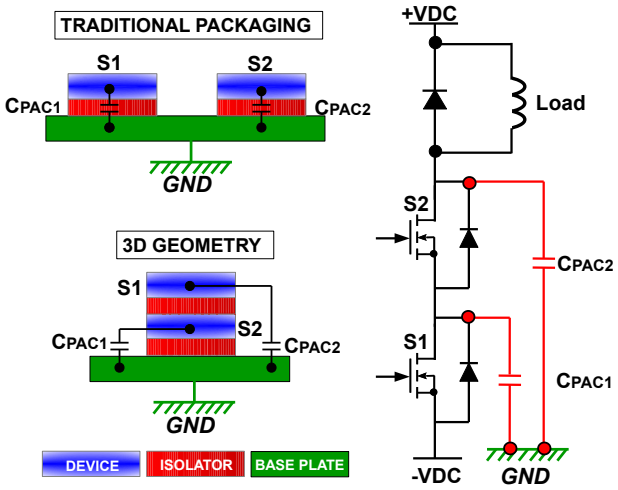



**Fig. 2.20.** 3D-geometry layout proposed in [50,51].

As shown in Fig. 2.20, the basic principle is to change the package/layout parasitic capacitance values by modifying the package/layout geometry. The geometry and its parasitic capacitance values are modified to compensate the device parameter mismatch and package/layout parasitic components.

A similar method is proposed in [10], where a multi-step packaging concept was introduced for series-connected SiC-MOSFETs. As shown in Fig. 2.21, the main idea is to change the configuration of the parasitic capacitances introduced by the packaging layout. The drain-to-ground parasitic capacitances (in the traditional packaging) are reconfigured to form equivalent drain-to-source parasitic capacitances (multi-step packaging). Therefore, the

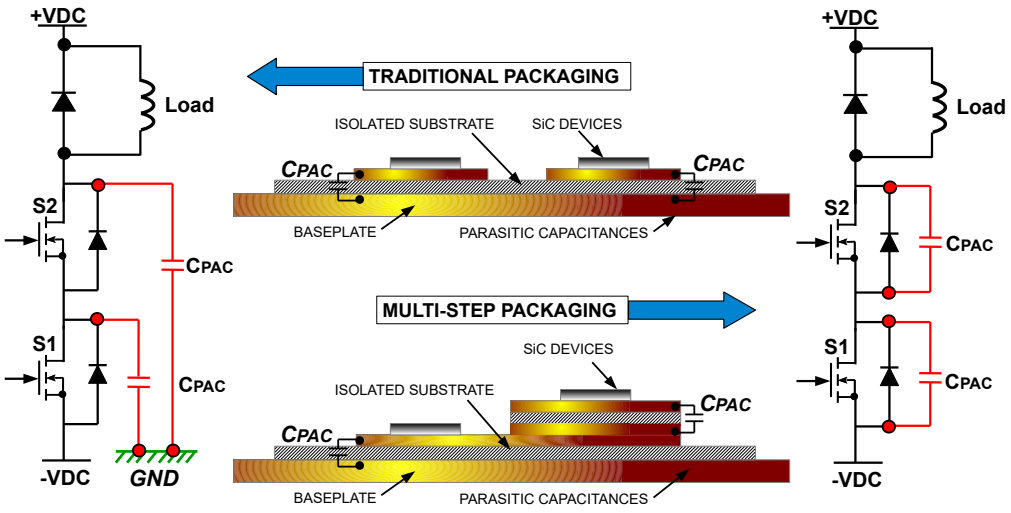



**Fig. 2.21.** Multi-step packaging concept proposed in [10].

impact of the drain-to-ground parasitic capacitances on the voltage balancing are drastically reduced.

In [9], the configuration of parasitic capacitances introduced by the gate drive circuitry are reconfigured by using the same principle addressed in [10,50,51]. Twenty new gate drive power supply configurations are investigated for four SiC-MOSFETs connected in series. Fig. 2.22 shows one of them where, differently from the traditional configuration, the gate drive power supplies are cascaded, i.e., the gate drive power supply 1 is powered by the gate drive power supply 2. In this case, the parasitic capacitance $C_{PS1}$ (in traditional configuration) is reconfigured (in the modified configuration) to form a new drain-to-source parasitic capacitance of device 2. As demonstrated and explained in [9], modifying the gate drive power supply configuration can reduce the voltage balancing problems across the series-connected devices. This technique can also mitigate the common mode current on the control side [13,70], and increase the switching speed of the series-connected devices [71].

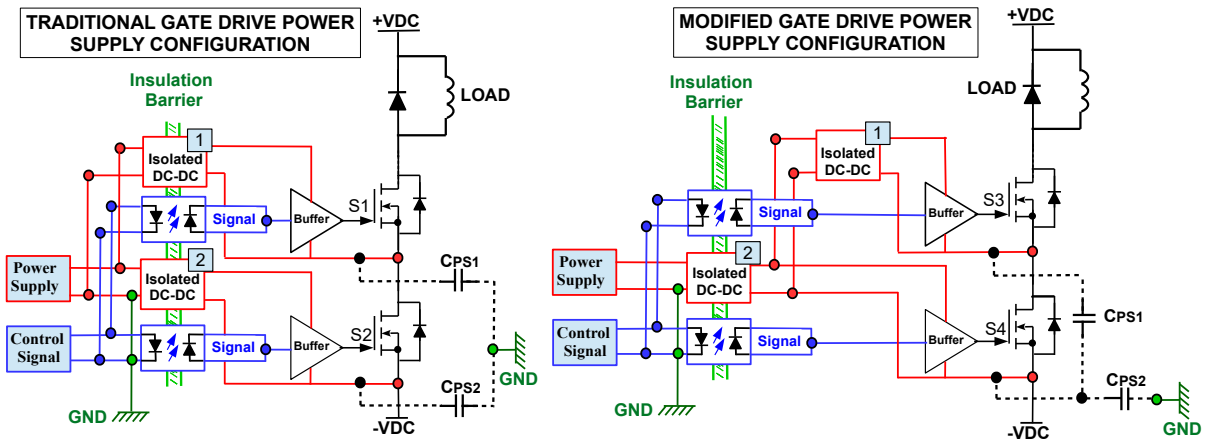



**Fig. 2.22.** Modified gate drive power supply configuration proposed in [9].

In [8] three configurations of compact high voltage SiC-MOSFET modules are proposed for a high voltage nanosecond pulse generator. The three topologies are shown in Fig. 2.23, where each configuration is represented by a specific coloured zone (A, B and C). The proposed circuits require only one external gate driver even for many series-connected devices. The capacitors $C_1$,$C_2$ and $C_3$ are used as energy storage units for the triggering pulse of every SiC-MOSFET. The main idea is to modify the configuration of these capacitors to improve the voltage balancing and switching speed of the devices. According to [8], the A-configuration presents the best performance in terms of voltage balancing.

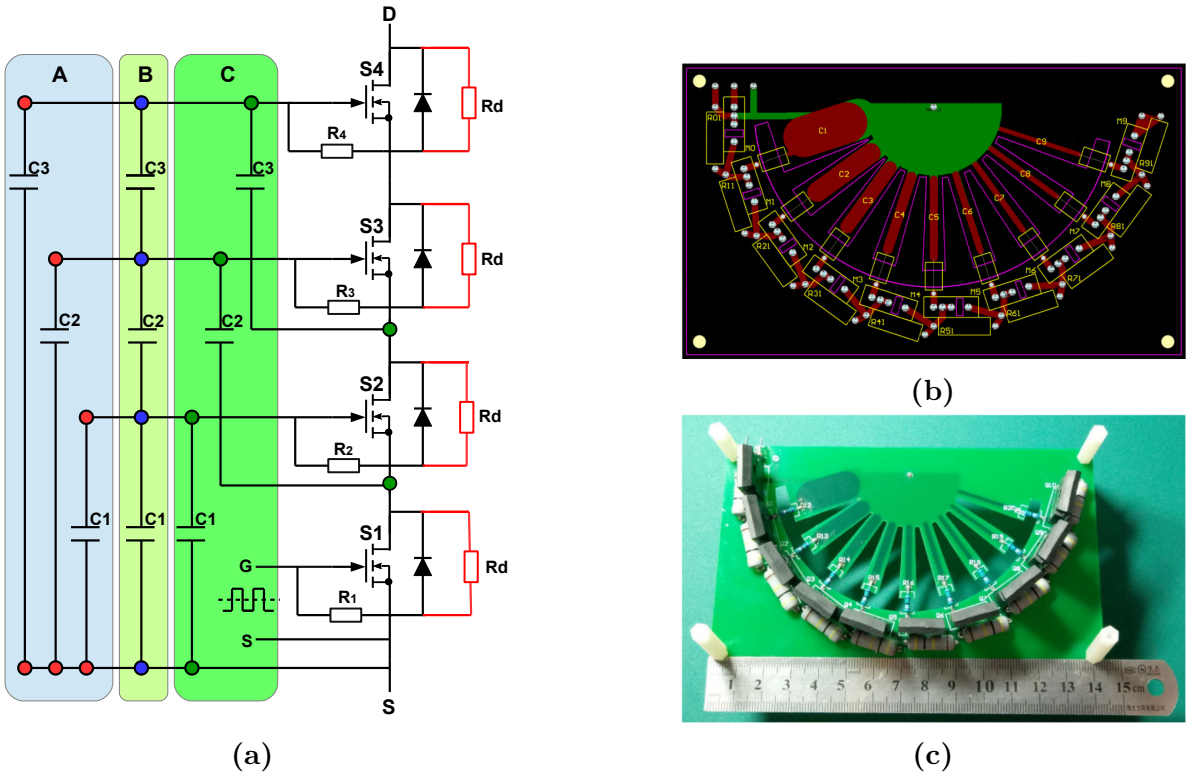



**Fig. 2.23.** Three derivative topologies for compact high voltage series-connected MOSFETs module (a), PCB layout for the A-configuration (b), and prototype of 10 kV power module (c) [8].

In the proposed circuit, the function of $R_d$ is not only to ensure the static voltage sharing among these series-connected devices, but also to act as a charging resistor for the gate capacitors. The role of $R_i$ (for $i$ =1,2,3,4) is to prevent a wrong triggering which might be induced by disturbed pulses. The main idea of the proposed method is to use the potential variation on the resistor $R_i$ to turn-on/off the series-connected devices. For example, during the turn-on transition, once the external driving signal changes into stable positive voltage level, the SiC-MOSFET S1 will turn on first. Then, the electric potential at drain electrode of S1 will fall down rapidly. Consequently, a gate-source voltage difference for S2 will be generated, due to the potential variation of $R_2$. Accordingly, the equivalent capacitor $C_{gs}$ of S2 will be charged by $C_1$. When the threshold voltage is reached, it will turn-ON immediately. Similarly, all of the series-connected SiC-MOSFETs will transit into

ON-state in sequence. In Figs. 2.23(b) and (c) are shown the proposed PCB layout and prototype for ten series-connected SiC-MOSFETs. As can be seen, it takes advantage of the layout parasitic capacitances related to the gate terminals to achieve the energy storage units $C_1$-$C_9$. Therefore, the voltage sharing performance is improved by a natural self-balancing technique without need external capacitor to achieve the energy storage units.

As can be seen, natural self-balancing methods can be implemented to optimize series-connected device topologies and reduce the voltage balancing problems. However, this kind of technique does not take into account the mismatch between the gate signals or other parameters that go beyond the packaging/layout and gate drive power supply parasitic capacitances. In other words, natural self-balancing method can not provide perfect balanced voltages. Otherwise, in order to reduce switching losses or EMI problems, natural self-balancing circuits can be applied together with other techniques, such as the methods presented in this chapter.

### 2.4.4 Active Gate Control

Active gate controls have been proposed in the literature to achieve acceptable voltage sharing across the series-connected devices [32,45,52–67]. Compared to passive techniques or voltage clamping methods, active gate control tends to provide less losses, and more compact footprint. Active gate controls can be divided in two categories: 1) gate delay control and 2) gate current control. In the first category, the main idea is to control the delay between the gate signals to mitigate the voltage unbalance. In the second category, the gate current is controlled to control the switching speeds of the devices, and get dynamic voltage balancing. The control current can be achieved directly controlling the gate current, or by controlling the gate resistances or gate voltages.

In [52,53] is proposed a method to balance the dynamic voltages among series-connected SiC-MOSFETs with high $dv/dt$ rates. As shown in Fig. 2.24(a), the main idea is to use a current mirror circuit and a small miller capacitor ($C_M$) to provide additional current to the gate of the SiC-MOSFETs at turn-off, meaning the switching speed is controlled. The circuit formed by four identical BJTs ($Q_1$-$Q_4$) is used to deflect the Miller current ($I_C$) to the gate of the top SiC-MOSFET to slow it down and improve the voltage balancing. Note that $Q_3$ and $Q_4$ form a current mirror, where $Q_4$ copies the current conducted by $Q_3$. The value of $I_c$ is a function of $V_{CTR}$. If $V_{CTR}$ is set to zero, only $Q_2$ will conduct, then, the control current $I_{GC}$ will be equal to $I_C$, resulting in the slowest turn-OFF speed for the top device. On the other hand, if $V_{CTR}$ is set to 1 p.u., the $I_C$ current will be shared between $Q_1$ and $Q_2$, and $I_{GC}$ will be negligible, resulting in the fastest (nearly original) switching speed for the top SiC-MOSFET. In this way, setting $V_{CTR}$ to an appropriate value, equal dynamic voltages can be achieved between the top and bottom SiC-MOSFETs. The $V_{ds}$ voltage

difference information provided by voltage sensors is used by a PI controller to generate the appropriate $V_{CTR}$ value.

In [54], a similar active gate control method is proposed as shown in Fig. 2.24(b). The proposed circuit uses an auxiliary circuit to control the gate currents of the devices. The circuit operation is quite simple: if $V_{CP}$ is on and $V_{CN}$ off, the auxiliary circuit will inject the control current $I_{GC}$ in the S1 gate, speeding up the device S1. On the other hand, if $V_{CP}$ is off and $V_{CN}$ on, the auxiliary circuit will extract the control current ($I_{GC}$ is negative) from the S1 gate potential slowing down the device S1. In this way, controlling $V_{CP}$ and $V_{CN}$ in an appropriate manner, the switching speed of devices can be controlled achieving balanced voltages among series-connected devices. The $V_{ds}$ voltage difference information provided by voltage sensors is used by a PI controller to control $V_{CP}$ and $V_{CN}$.

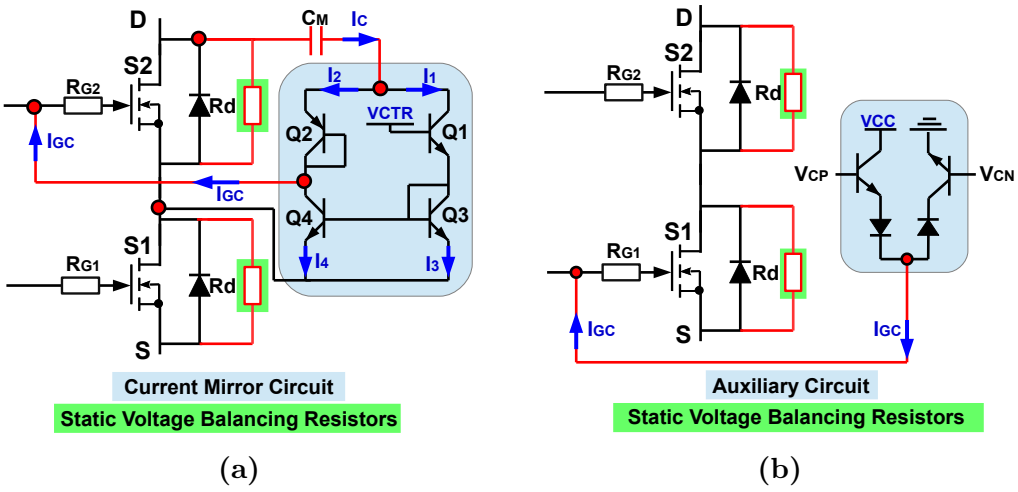



**Fig. 2.24.** Active $dv/dt$ control method for balancing voltages across stacked SiC-MOSFETs proposed in [52, 53](a), and similar active gate control proposed in [54](b).

An active gate drive control method is proposed in [55–57] with a gate resistance modulation technique for dynamic voltage sharing during the turn-off switching. As shown in Fig. 2.25(a), it consists of three resistors ($R_{on}$, $R_1$, and $R_2$) which have same resistance value ($R$) and one auxiliary switch ($M_i$, i =1,2). The main idea of the proposed circuit is to control the gate current by modulating the gate resistance, and consequently control the dynamic voltage sharing. The circuit operation is quite simple: when $M_i$ is turned on, $R_{off}$ is equal to $R_1//R_2$. When Mi is turned-off, $R_{off}$ is equal to $R_1$. Therefore, the $R_{off}$ have two different values by controlling the $M_i$. In other words, the gate current of each device and the dynamic switching process can be controlled by the switch $M_i$. In the control algorithm, the basic idea is to delay the $M_i$ activation. The switches $M_1$ and $M_2$ are activated at the beginning of the turn-off sequence. Supposing that device S2 is faster than S1 ($V_{ds2}$>$V_{ds1}$), a voltage sensor will provide this information to the control unit, and in the next switching transition, the activation of $M_2$ will be delayed, slowing down $V_{ds2}$. This process is repeated until the voltage difference between the devices reaches an acceptable value.

In [45] a similar active gate drive control technique is proposed (Fig. 2.25(b)). Compared to the one presented in Fig. 2.25(a), switches $M_{iA}$, $M_{iB}$, and $M_{iC}$ are used to generate a delay on the $V_{gs}$ voltages. For example, during the S1 turn-off transition, the delay can be achieved by the RC circuit formed by $R_{off}$-$D_{off}$-$R_{G1}$-$C_{S1}$. Basically, $V_{ds}$ and $V_{gs}$ are sensed by a separate circuit, and the $V_{ds}$ voltage mismatch information is used by logical units to generate the ($M_{iA}$, $M_{iB}$, and $M_{iC}$) signals for delaying $V_{gs}$ and mitigate the voltage unbalance.

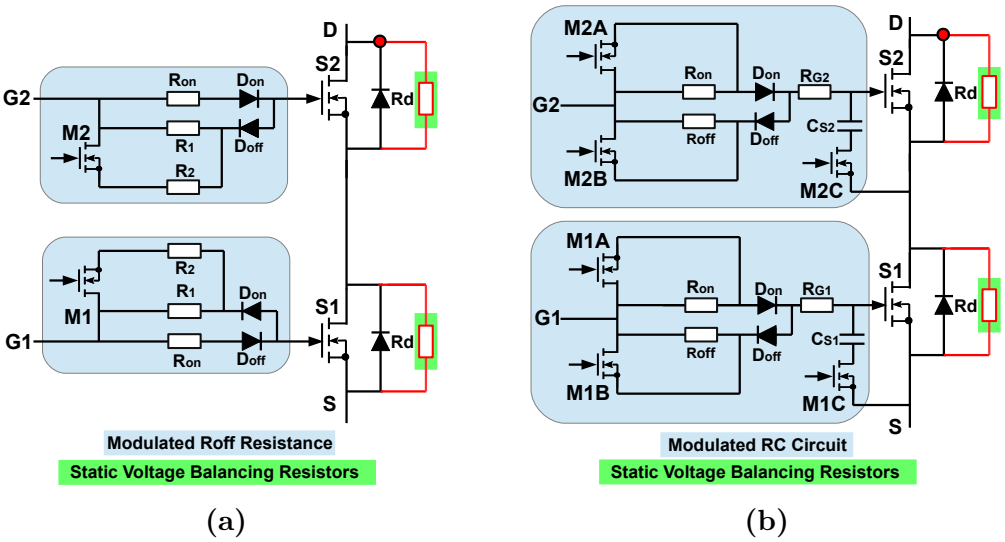



**Fig. 2.25.** Active control methods for balancing voltages across stacked SiC-MOSFETs proposed in [55–57](a), and in [45](b).

In [58] is proposed a closed loop active gate driver circuit which can control the slew rate of $V_{ds}$ at both turn-off and turn-on. As shown in Fig. 2.26(a), the proposed circuit works on the capacitive feedback current ($I_{FB}$) obtained from the feedback capacitor ($C_{FB}$) connected to the drain terminal of the series connected switches. In this approach, $I_{FB}$ represents the $dv/dt$ since $I_{FB} = C_{FB}.dv/dt$. Therefore, it is compared to a reference waveform ($dv/dt(ref)$) to generate an error signal. This error is processed by the analogue PI-controller. In the proposed technique, it is possible to use two different approaches for generating the $dv/dt$ reference for the device voltage balancing: 1) Master-slave approach for reference generation: in this case, the $dv/dt$ of one of the switches is used as $dv/dt(ref)$ for another switch. 2) Common $dv/dt$ reference: in this case, the PI controller associated with each device receives the same reference $dv/dt(ref)$ signal. If the PI controllers work properly, all the series-connected SiC-MOSFETs will have the same switching speed, and the voltage balance is achieved. The block diagram of the proposed closed loop circuit is shown in Fig. 2.26(b), where $H_{PI}(s)$, $H_{AMP}(s)$, $H_{SW}(s)$ and $H_{FB}(s)$ refer, respectively, to the transfer function of PI controller, output amplifier, SiC-MOSFET switching and positive feedback.

In [59], a capacitive coupling method is used for two series-connected SiC-MOSFETs. As shown in Fig. 2.27, only one external driver is needed in the proposed gate driver circuit.

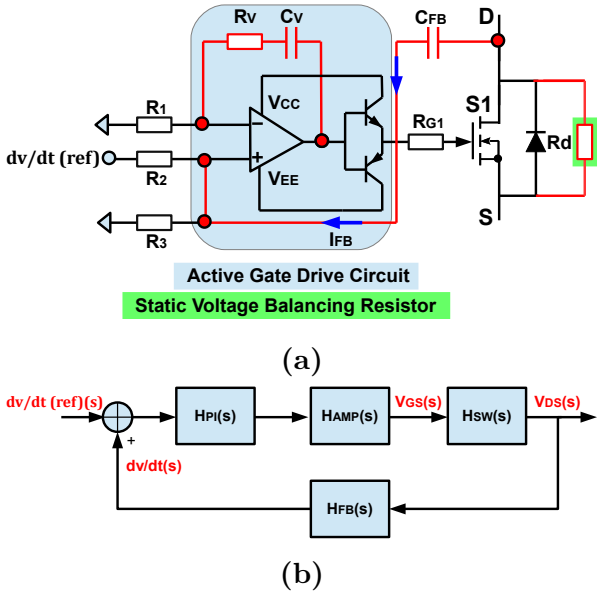



**Fig. 2.26.** Proposed closed loop active gate driver circuit (a), and its closed-loop block diagram (b) [58].

In Fig. 2.27, $R_1$ and $R_2$ are static voltage balancing resistors, $Z_2$ is a transient voltage suppressor used to the gate of S1 from overvoltage and provide a current path during the off-state, and $C_{PS}$ is a speed-up capacitor used to reduce the voltage spike during the turn-on transient. The circuit uses the energy stored in the high voltage capacitor $C_s$ to drive the SiC-MOSFET S2. For example, during the turn-off transient, when the turn-off signal occurs the $C_{iss}(C_{gd}+C_{gs})$ of S1 begins to discharge, $V_{gs1}$ starts to decrease. When S1 enters the saturation region, its drain-source voltage $V_{ds1}$ starts to rise, and the voltage on $C_S$ rises accordingly. The generated current $I_{CS}$ causes $V_{gs2}$ to drop rapidly. When the voltage across $C_S$ rises and blocks $D_2$, it produces a reverse recovery current $I_{DR}$. At this time, $I_{CS}$ and $I_{DR}$ work together to turn S1 off.

In order to balance the dynamic voltage between S1 and S2, the drive capacitor $C_S$ should provide a continuous driving force for S2 during all switching transitions. To this end, a $V_{CTR}$ and switched capacitor are added to control the driving capability of $C_S$ even under variation of the DC-bus voltage. For example, when the DC-bus voltage increases, which means that the driving capability of $C_S$ increases, the dynamic voltage imbalance will occur due to the faster turn-off of S2. At that time, setting $V_{CTR}$ appropriately to offset the increase in the driving capability of $C_S$ allows the proposed circuit to balance the dynamic voltage at turn-off transient. However, $V_{CTR}$ is limited by its range of values, i.e., in some conditions $V_{CTR}$ can not provide driving capability of $C_S$. To solve this problem, a switched capacitor is added to increase the effective range of the dynamic voltage balancing. For example, by turning-off the switch $S_{CP}$ in the switched capacitor circuit, $C_P$ is series-connected with $C_S$, and the driving capability of $C_S$ is adapted.

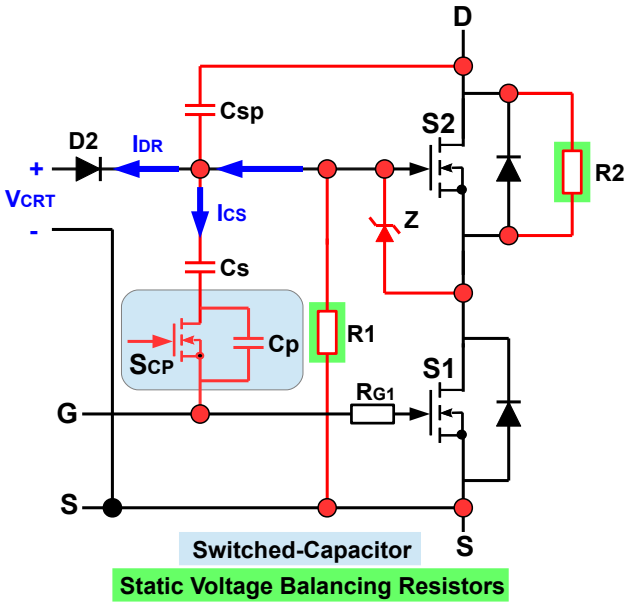



**Fig. 2.27.** Capacitive coupling method proposed in [59].

Several digital delay circuits have been proposed in the literature to adjust the gate signal timing to mitigate the voltage unbalance across series-connected devices [32, 60–65]. techniques adjust the gate-driver delay by using the $\Delta V_{ds}$ error. The widely used clock frequencies for digital circuits including DSPs and FPGAs are in the range of 10-100 MHz; hence, the minimum control cycles have durations greater than 10 ns. However, due to the faster switching speeds of the series-connected SiC-MOSFETs, the timing delay control requires a high bandwidth capable of adjusting gate signal timing in the nanosecond range.

In [61] is proposed a voltage balancing method for series-connected SiC MOSFETs at turn-off operations using a time-delay open-loop control. As shown in Fig. 2.28(a), the gate drive circuit uses an FPGA and a digital delay line to impose a delay on the $V_{gs1}$ signal. The time-delay is estimated as a function of the device parameters. In [62], a similar idea is proposed, bu tin this case the time-delay adjustment depends on the voltage unbalance value. As shown in Fig. 2.28(b), it is a closed-loop control, where the $V_{ds}$ voltages are sensed and compared. The $\Delta V_{ds}$ information is sent to the FPGA where a P controller is used to generate a delay signal as a function of $\Delta V_{ds}$. In [61, 62], the FPGA clock frequency is set to 100 MHz, which corresponds to a time control of 10 ns. To control the gate delay time within less 1 ns, a DS1023 digital delay line is used in the gate drive circuit. The digital delay line has a time resolution of 0.25 ns.

In [63] a similar method is presented. The proposed gate driver provides a closed-loop control with active time-delay method for series-connected SiC-MOSFETs as shown in the overall circuit schematic in Fig. 2.29. The main idea is to delay the drive signal to compensate the $V_{ds}$ voltage differences across the series-connected devices. For each SiC-MOSFET, a transient-voltage-suppression (TVS) diode is used for a passive overvoltage

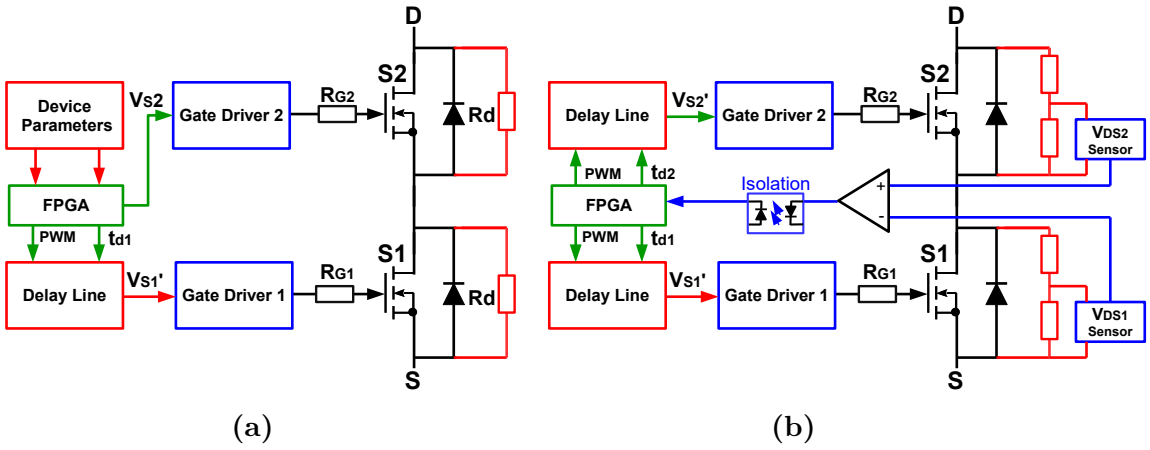



**Fig. 2.28.** Time-delay control for series-connected devices. Open-loop control [61](a), and closed loop [62](b).

protection. A RC voltage divider is used to sample the voltage $V_{ds}$ and the sampled voltage is sent to high speed AD converter through a voltage follower. The digital value of the voltage is sent into the controller with an insulation barrier (optocoupler). The main controller generates PWM pulses and computes the delay time that should be applied for each drive signal at the same time. The delay action is implemented by a silicon delay line IC rather than the controller itself. In short, after every turn-off, AD converters sample the difference between $V_{ds}$ voltages and the DSP computes the delays. Then a delay time signal is sent to the delay line ICs to compensate the gate drive signals timing deviations for the next PWM pulse. This active control discrete system needs a PI (or similar) controller to eliminate static error, and to ensure the stability analysis of the control system. The IC used in [63], DS1020S-15 manufactured by Dallas, is an 8-bit programmable delay line IC, which can delay the signal with a minimum time step of 150ps and a maximum delay time of 38.4ns.

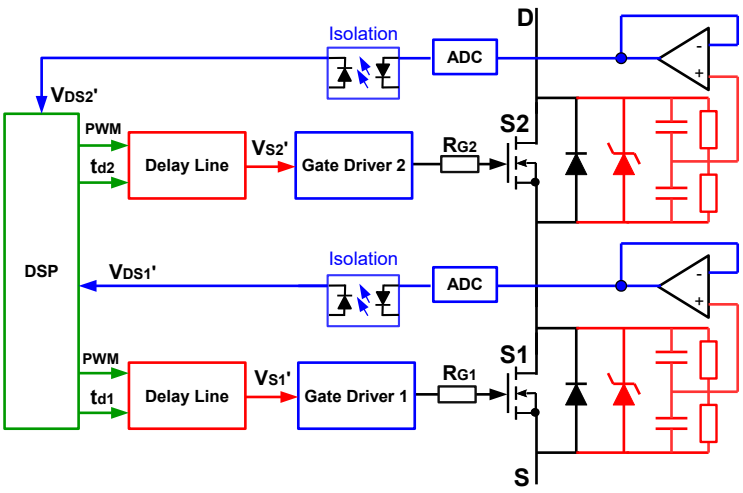



**Fig. 2.29.** Time-delay closed-loop control proposed in [63].

In [64] is proposed an active voltage balancing control by adaptively tuning the gate signal timing between series connected switches via high resolution pulse-width modulator (HRPWM) according to the feedback from online voltage unbalance monitor unit. Fig. 2.30 illustrates the proposed active voltage balancing control diagram. It consists in three functional blocks: 1) transient-voltage-suppression (TVS) diodes anti-paralleled with the series-connected switches as the passive protection; 2) a microcontroller as the actuator for active voltage balancing control; and 3) a voltage sensor unit as the feedback for active voltage balancing control. The main idea is to use the online voltage monitor unit as the feedback to generate proper delays between the gate signals. The turn-off voltage monitor unit consists in two resistor dividers and one comparator. Two resistor dividers are used to measure the $V_{ds}$ voltage across the lower series-connected switch as well as the total drain-source voltage across the lower and upper series-connected SiC-MOSFETs. Then the sensed $V_{ds}$ voltages are compared. Therefore, the $V_{ds}$ voltage relationship between the lower and upper series-connected switches can be online monitored by the microcontroller to regulate the HRPWM gate signal timing unit. For example, during the turn-off transient, if the $V_{ds}$ voltage of the lower switch is higher than the $V_{ds}$ voltage of the upper switch, the microcontroller delays the lower switch gate signal in the following turn-off switching cycle. The turn-on voltage monitor unit consists in two $V_{ds}$ boundary detection (DVBD) circuits for the lower and upper series-connected switches. The function of the DVBD circuit is to indicate whether the $V_{ds}$ voltage of each series-connected SiC-MOSFET increases during the turn-on transient.If the $V_{ds}$ voltage of one series-connected device increases during the turn-on transient, it means that the turn-on dynamic voltage is unbalanced, then the HRPWM based tunable gate signal timing unit should be activated. The proposed compensation approach always has one switching cycle control delay, thus, initially severe dynamic voltage balance issue may occur. However, the TVS diode is able to clamp the corresponding over-voltage.

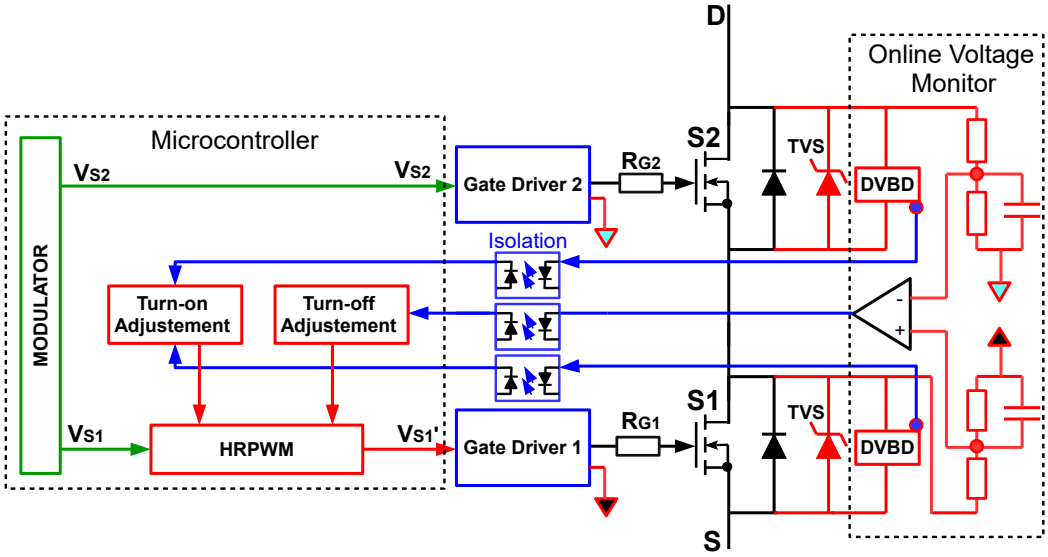



**Fig. 2.30.** Time-delay closed-loop control proposed in [64].

A method to adjust time delay using FPGA is discussed in detail in [65], . Abandoning the PI/I controller, a binary searching algorithm which takes both adjusting speed and robustness into account is adopted. In simple terms, according to the measured drain-to-source differential voltage after each turn-off transient, a binary searching algorithm is performed to find the optional number of delay steps. The binary searching algorithm with 15 delay steps is shown in Fig. 2.31, where the initial number of delay steps is set to 8. The algorithm operation is quite simple.

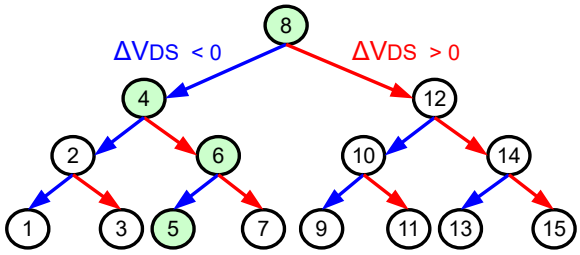



**Fig. 2.31.** Binary searching algorithm proposed in [65].

$\Delta V_{ds}$ is measured and this information is used to set the number of delay steps in the next turn-off switching. For example:

- Stage 1: The number of delay steps (N) is set to 8. Therefore, 8*(fixed step size) is imposed on the next switching turn-off.
- Stage 2: The $\Delta V_{ds}$ is measured, and it is $< 0$. Therefore, the initial N (N=8) will be reduced to 4, and a delay of 4*(fixed step size) will be applied for the next turn-off switching.
- Stage 3: After the imposed 4*(fixed step size), $\Delta V_{ds}$ is measured, and now it is $>$ 0, meaning that N = 4 is below the optimal number of delay steps. Therefore, N is increased from 4 to 6, and it will be applied for the next turn-off switching.
- Stage 4: After the imposed 6*(fixed step size), the $\Delta V_{ds}$ is measured, and now it is $<$ 0, meaning that N = 6 is above the optimal number of delay steps. Therefore, N is reduced from 6 to 5. In this case, the optimal number of delay steps is reached, and it will be applied for the next turn-off switching.

Note that, no matter the optimal number of delay steps, it is identified within four switching circles. In other words, the proposed method is insensitive to the load current, the blocking voltage, and the device parameters. Meanwhile, it has a rapid convergence speed. However, the proposed algorithm needs a proper step size to ensure the convergence. A large step size will cause an unacceptable $\Delta V_{ds}$ that will alternate between positive and negative.

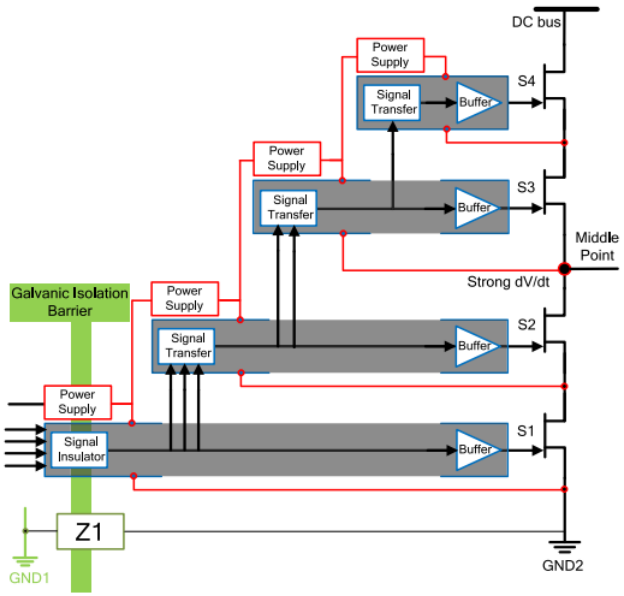



**Fig. 2.32.** Modified gate drive architecture proposed in [72].

On the other hand, a small step size results in an excellent voltage balancing. However, a small step size will slow down the voltage balancing speed. Furthermore, the step size is also limited by the digital circuit clock frequency [65].

### 2.4.5 Common Mode Conducted EMI

Compared to silicon devices, the switching speed of SiC-MOSFETs is increased to reach few 100V/ns for the drain-to-source $dv/dt$ for instance [31]. The main drawback is the increase in common mode current due to $dv/dt$ and parasitic capacitances between the power part and the control part. In terms of series-connected devices, most of the literature-only address voltage balancing problems. In other words, the electromagnetic compatibility (EMC) techniques applied for traditional converters, are also applied for series-connected device topologies. However, series-connected SiC-MOSFETs require a special attention in terms of electromagnetic interference (EMI). A specific method to mitigate the common mode conducted EMI in series-connection topologies has been addressed for the first time in [72] where the gate drivers (power supplies and signals) are cascaded as shown in Fig. 2.32.

The main idea of the proposed gate drive architecture is to modify the pathway of the common mode current on the control side. As demonstrated in [72], this technique can drastically reduce the common mode current that circulates in the control side. However, the gate drive architectures proposed in [72] are not suitable for series-connected SiC-MOSFETs since the signal units are cascaded, generating timing delays between the $V_{gs}$ signals. Therefore, it will exacerbate voltage sharing issues of the series-connected SiC-MOSFETs. Based on this

thesis work, the delay problems presented in [72] have been solved [9]. As will be explained in the next chapter, new power supply configurations have been proposed to reduce the common mode conducted EMI without degrading voltage sharing performances. Furthermore, the solutions presented in this work can also mitigate voltage balancing problems related to series-connected SiC-MOSFETs.

# Chapter 3
# New Gate Driver Architectures

In series-connected devices under very high switching speed, several $dv/dt$ sources generated at different floating points produce conducted EMI perturbations from the power part to the control part through the gate drive circuits. The capacitive propagation paths between the power and control sides have considerable impacts on the circulating current produced by high $dv/dt$. The control system can be disturbed and/or damaged by a large amount of noise current that may flow through the control parts because of the parasitic capacitances of the gate drive power supplies. Therefore, in this chapter, new gate drive power supply configurations are analysed in order to minimize the conducted common mode (CM) currents in series-connected SiC-MOSFET applications. Furthermore, a new gate driver configuration is proposed in order to increase the $dv/dt$ of the switching cell middle point.

## 3.1 Common Mode Conducted EMI Reduction

The CM currents that circulate in power converters can be divided in two categories: 1) the CM currents that circulate in the power part through the power devices and the ground (through the dielectric barrier of the package) [10,11], and 2) the CM currents that circulate in the control part through the isolation barriers of the DC-DC power supplies and signal transmission functions of gate drivers [12,13,73]. This work is focused on the second category, i.e., on the CM currents that circulate through the parasitic capacitances introduced by DC-DC power supplies and signal transmission functions of gate drivers. Fig. 3.1 shows these parasitic capacitances: 1) the parasitic capacitance introduced by the primary to secondary gate drive power supply ($C_{ps}$) and 2) the parasitic capacitance of the signal isolation ($C_{iso}$). The parasitic capacitances $C_{ps}$ and $C_{iso}$ have the same dynamic influences on the system. However, in the present work, it is considered that the capacitance $C_{iso}$ is negligible when compared to $C_{ps}$ since in the experiments, isolated signals are implemented by optical fibers.

The parasitic elements of the gate drive power supply and its connections are shown in Fig. 3.2. As can be seen, two reference potentials are presented in classical switching cells [74, 75], i.e., the ground or reference potential of the remote control circuit (VCR) and the reference potential of the power circuit (-VDC). Both VCR and -VDC are isolated from each other. Therefore, isolated supply converters are implemented in order to enable the isolation dedicated to the power supply parts. Optocouplers or optical fibers are used to isolate the paths for the control signals. Table 3.1 describes the main elements presented in

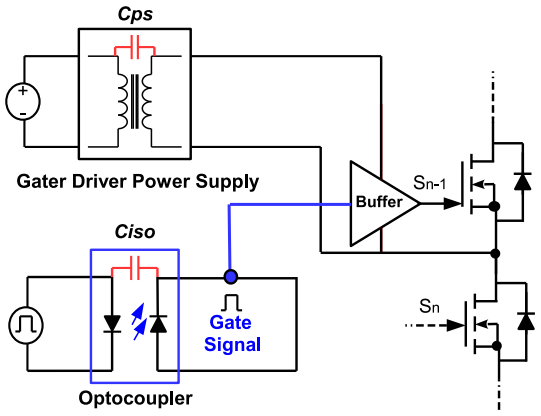



**Fig. 3.1.** Gate drive power supply and signal isolation unit parasitic capacitances.

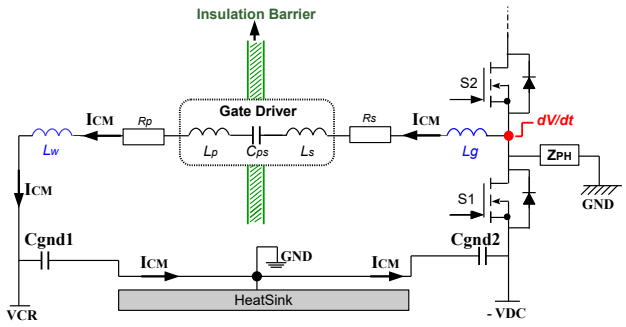



**Fig. 3.2.** Parasitic elements of the gate drive power supply and its connections.

Fig. 3.2.

To clarify the purpose of this work, Fig. 3.2 presents the common mode parasitic impedance ($ZPH$) between the middle point of each power leg and the heatsink connected to the ground of the primary side of the control circuit [76, 77]. However, this work focuses on the perturbations of the power circuit on the control side, i.e., the CM currents that circulate through the parasitic capacitances $C_{gnd1}$ and $C_{gnd2}$. The noise currents that circulate through $ZPH$ are not analysed in this work.

For security reasons, most heatsinks are attached to the ground potential of the remote control circuit (VCR), and not to -VDC. In this chapter, this consideration is also taken into account. In this case, the $C_{gnd1}$ is short-circuited, and VCR is represented by GND.

Power converter topologies with $N$ series-connected devices have $N$ floating points, which correspond to $N$ $dV/dt$ sources. Then, if isolated power supplies in the drive circuitry are used, they introduce primary to secondary parasitic capacitances ($C_{ps}$), and therefore several common mode conducted EMI pathways. As shown in Fig. 3.2, where the gate drive circuitry elements are presented, each $dV/dt$ source produces its own conducted current disturbance ($I_{CM}$) that propagates to the control parts and then through the ground. As will be explained in the next sections, the CM current is directly proportional to the switching speed of the devices, which implies that under very high $dv/dt$, the gate driver system has to be carefully

**Table 3.1**
Gate drive circuitry elements presented in Fig. 3.2

| Element | Description |
|---|---|
| $C_{ps}$ | Parasitic capacitance of the isolated DC/DC converter. |
| $C_{gnd1}$ | Parasitic capacitance between the control reference (VCR) and the ground (GND). |
| $C_{gnd2}$ | Parasitic capacitance between power reference (-VDC) and the ground (GND). |
| $L_p$ | Parasitic terminal inductance on the primary side of the gate drive power supply. |
| $L_s$ | Parasitic terminal inductance on the secondary side of the gate drive power supply. |
| $L_w$ | Parasitic inductance of the power supply on the primary side. |
| $L_g$ | Parasitic inductance of the power supply on the secondary side. |
| $R_p$ | Parasitic resistance of the power supply on the primary side. |
| $R_s$ | Parasitic resistance of the power supply on the secondary side. |
| $Z_{PH}$ | Parasitic impedance between the middle point of each power leg and the heatsink connected to the ground. |

designed and new EMI reduction techniques have to be applied in order to avoid damages caused by a large amount of noise currents in the control side.

### 3.1.1 Traditional Gate Driver Configuration (TGD)

The traditional gate driver configuration is shown in Fig. 3.3. Each isolated power supply of each gate driver is supplied by an external power supply. In this configuration, there are four sources of perturbation produced by four floating points, where three of them are directly connected their associated gate drive power supplies (isolated DC-DC blocks) that introduce parasitic capacitances ($C_{ps}$).

In the TGD configuration, the CM currents produced by the $dV/dt$ sources have to cross one isolation barrier, which is modelled by $C_{ps}$, to circulate into the control side as shown in Fig. 3.3(b). The CM currents that circulate in the control side can be estimated by using Eqs. (3.1) - (3.2), where $I_i$ is the current that flows through $C_{psi}$, $dV_{Cpsi}/dt$ is the $dv/dt$ across the parasitic capacitance $C_{psi}$ and $I_{CM}$ is the total CM current in the control side that circulates through the ground impedance $Z_{ps}$, which represents the impedance formed by $C_{gnd2}$.

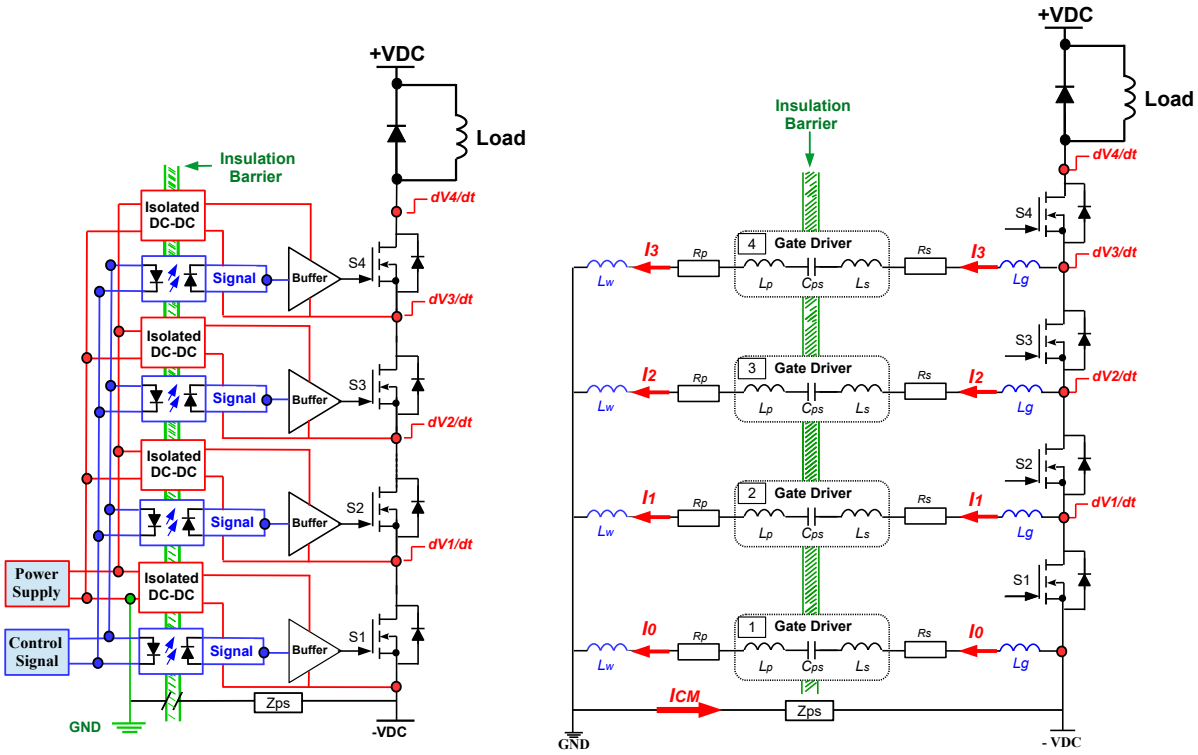



**Fig. 3.3.** TGD configuration (a) and its electrical circuit (b).

$$I_i = C_{ps}\frac{dV_{Cpsi}}{dt}, i = 0, 1, 2, 3. \tag{3.1}$$

$$I_{CM} = I_0 + I_1 + I_2 + I_3 \tag{3.2}$$

The parasitic capacitance associated to the current $I_0$, experiences an ultra-low $dv/dt$ when compared to the others. In this case, it can be supposed that $I_0$ has a very small value. Therefore, this current is not considered on the next analyses.

To estimate the CM current in the control side as a function of the switching speed of the devices, Fig. 3.4 shows a simplified TGD electrical circuit, which represents each device by a source as a function of the voltage at the middle point of the switching cell $V(t)$. Note that, it is supposed that the voltages across the devices are balanced and the gate drivers are identical. Therefore, according to the current distribution in Fig. 3.4, the CM currents can be expressed, in the *Laplace domain*, by Eqs. (3.3)-(3.5), where $V(s)$ is the voltage at the middle point of the switching cell.

$$I_3(s) = \left(\frac{3}{4}\right)\frac{V(s)}{R_p + R_s + \frac{1}{sC_{ps}} + s\left(L_s + L_p + L_w + L_g\right)} \tag{3.3}$$

$$I_2(s) = \left(\frac{2}{4}\right)\frac{V(s)}{R_p + R_s + \frac{1}{sC_{ps}} + s\left(L_s + L_p + L_w + L_g\right)} \tag{3.4}$$

$$I_1(s) = \left(\frac{1}{4}\right) \frac{V(s)}{R_p + R_s + \frac{1}{sC_{ps}} + s\left(L_s + L_p + L_w + L_g\right)} \tag{3.5}$$

Using Eqs. (3.3), (3.4) and (3.5) in the Eq. ( 3.2), the CM current in the control side can estimated by Eq. (3.6).

$$I_{CM}(s) = \left(\frac{3}{2}\right) \frac{V(s)}{R_p + R_s + \frac{1}{sC_{ps}} + s\left(L_s + L_p + L_w + L_g\right)} \tag{3.6}$$

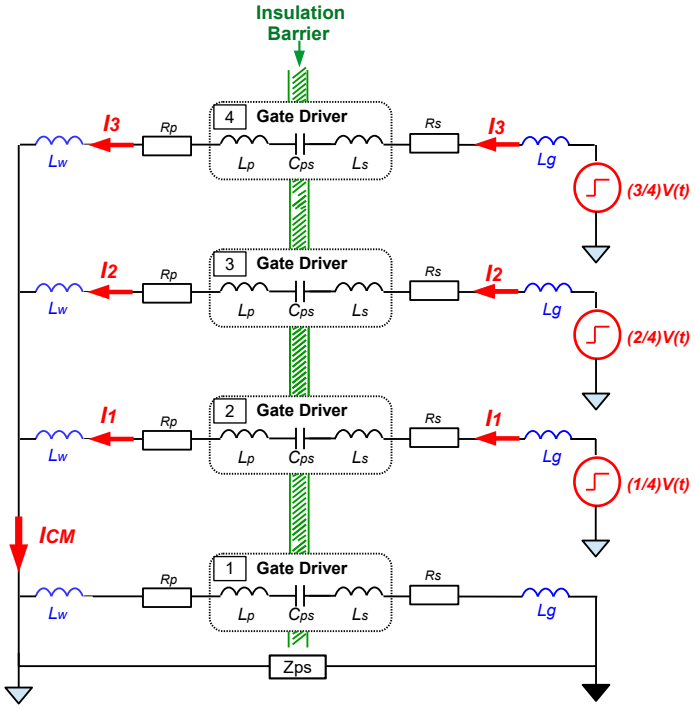



**Fig. 3.4.** Equivalent switching cell model for the TGD configuration.

The parameters in the dominator of Eq. (3.6) represent the gate drive power supply impedance, which is plotted in Fig. 3.5 for different parasitic capacitance ($Cps$). The values used to generate Fig. 3.5 are: $R_s = R_p = 0.1\ \Omega$ , $L_p = L_s = 20\ nH$, $L_w = 20nH$ and $L_g = 25\ nH$. These values, which are summarized in Table 3.2, are based on the set-up experiments and devices used in this work.

As can be seen, for frequencies of less than 200 $MHz$, the gate drive power supply impedance can be increased by reducing the $C_{ps}$ values. For very high frequencies, the impedance has a dominant inductive behaviour, and reducing $C_{ps}$ values has less and less influence on the total impedance value.

Analysing Eq. (3.6) and the results shown in Fig. 3.5, increasing the gate driver impedance by reducing the $C_{ps}$ is an effective way to reduce the CM currents in the control side.

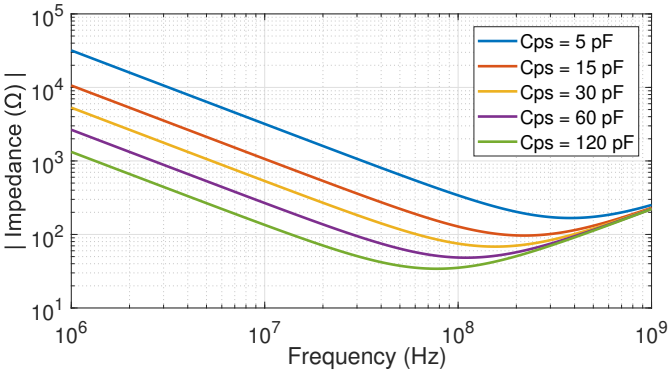



**Fig. 3.5.** Gate drive power supply impedance for different values of $C_{ps}$.

**Table 3.2**
Element values of the equivalent impedance network circuits

| Element | Value | Description |
|---|---|---|
| $C_{ps}$ | 5-120 pF | Estimated primary-secondary parasitic capacitance for the gate drive power supplies used in this work [78]. |
| $Z_M$ | 1 nF // 100 MΩ | Impedance used to concentrate and measure the noisy current in the control side. |
| $L_w$ | 20 nH | Estimated parasitic inductance of connections of the power supply on the primary side. |
| $L_p$, $L_s$ | 20 nH | Estimated primary and secondary parasitic terminal inductances of the gate drive power supplies. |
| $L_g$ | 25 nH | Estimated parasitic inductance of connections of the power supply on the secondary side. |
| $R_p$, $R_s$ | 100 mΩ | Estimated resistances of gate driver connections. |

In other words, the lower the value of $C_{ps}$, the greater the gate driver impedance, and consequently the lower the CM current in the control side. However, the lower the capacitance $C_{ps}$, the more expensive and complex is the power supply and system implementation.

Furthermore, most of commercial isolated gate drive power supplies are often rated for a common mode transient of less than 100 kV/$\mu$s [79]. Nevertheless, some WBG power devices, such as GaN transistors generate more than 100 kV/$\mu$s for the CM transition [80]. A smart solution to decrease the CM currents in the control side is to change the CM current pathway by modifying the gate drive power supply configuration as shown in the next sections.

### 3.1.2 New Modified Gate Driver Configurations

The First Modified Gate Driver configuration (1MGD) is shown in Fig. 3.6, where the gate drive power supplies are fully cascaded, i.e., the gate driver 1 (corresponding to the switch $S_1$) is directly powered by an external power supply connected to GND. The gate driver 2 is powered through gate driver 1, the gate driver 3 is powered through gate driver 2, and gate driver 4 is powered through gate driver 3. A similar technique has been proposed in [70]. However, the transfer signals are also cascaded. In this case, delays are introduced between the gate signals. This is unacceptable for short switching times. In series connection, the gate signal delays can exacerbate voltage balancing problems. In [32] it is demonstrated that a 20 ns delay between gate drive signals of two SiC-MOSFETs can trigger over 400V voltage difference under 800V DC bus voltage. Therefore, the approach proposed in [70] is not suitable for devices with fast switching speed, such as SiC and GaN devices. On the other hand, as can be seen in Fig. 3.6, in the modified gate drive power supplies proposed in this work, the control signal configuration does not change. It remains identical to the classical configuration. Therefore, the gate signals are not affected by changing the gate drive power supply configuration, and no gate signal delay is introduced in the drive circuitry.

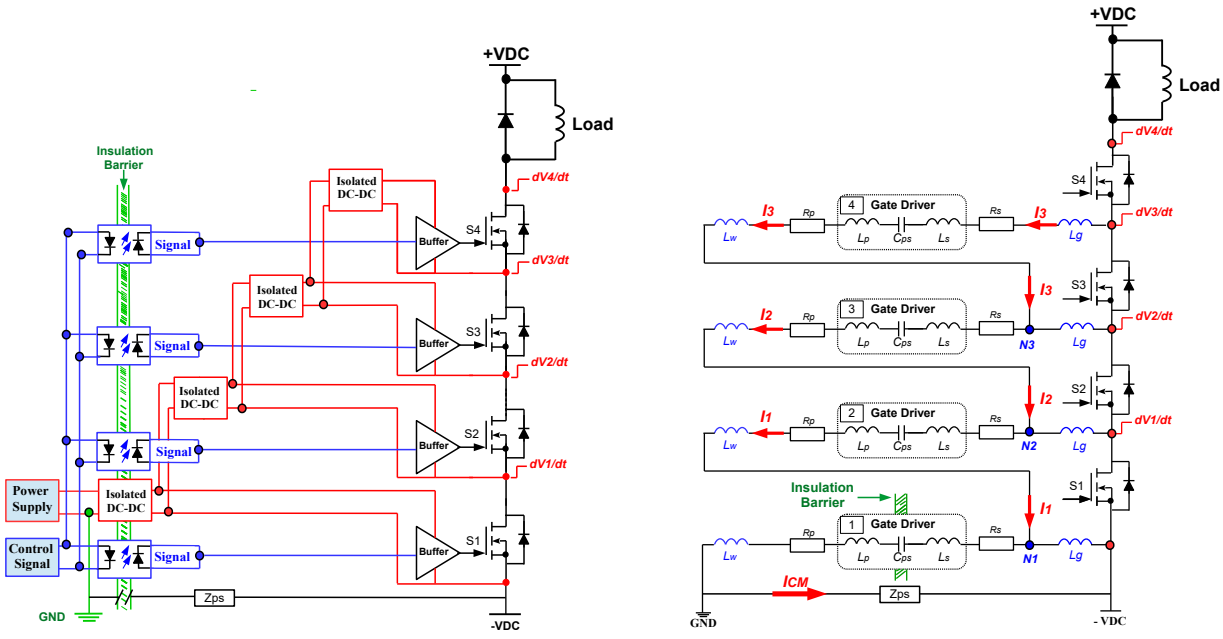



**Fig. 3.6.** 1MGD configuration (a) and its electrical circuit (b).

In the 1MGD, the CM currents produced by the $dV/dt$ sources have to cross more than one isolation barrier to circulate into the control side. As shown in Fig. 3.6(b), to circulate in the control side, the CM current $I_3$ has to cross four isolation barriers generated by the four gate drivers. Each isolation barrier provides a large impedance that forces the return of

each CM current to the power part. For example, considering the current distribution in Fig. 3.7, the current $I_1$ can be expressed as the sum of $I_{CM}$ plus $I_r$, where $I_r$ is the current that returns to the power side without circulating in the control part, and $I_{CM}$ is the total CM current that circulates in the control side. The current $I_1$ tends to take the path that has the lowest impedance. Two impedances, $Z_A$ and $Z_B$, are represented in Fig. 3.7. Therefore, if $Z_A + Z_{ps} \approx Z_A >> Z_B$, the majority of the current $I_1$ will return locally to the power side through the impedance $Z_B$.

Impedances $Z_A$ and $Z_B$ are expressed by Eqs. (3.7) and (3.8). Where $f_t$ is the equivalent transient frequency, which is approximately equal to 0.35/(rise time) [70]. The rise time of the devices analysed in this chapter (C2M0025120D) is about 32 ns. Therefore, the estimated transient frequency is approximately equal to 11 MHz.

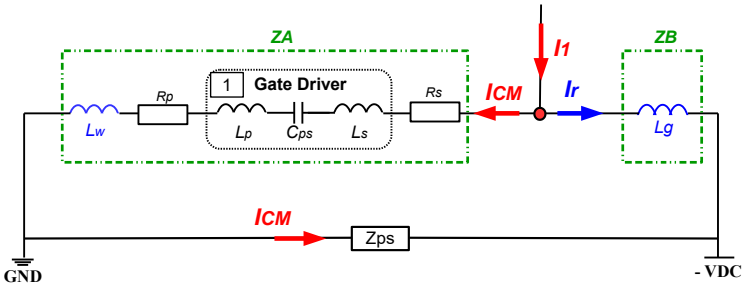



**Fig. 3.7.** Gate drive power supply impedances.

$$Z_A = R_p + R_s + \frac{1}{j2\pi f_t C_{ps}} + j2\pi f_t \left(L_s + L_p + L_w\right) \tag{3.7}$$

$$Z_B = j2\pi f_t L_g \tag{3.8}$$

Fig. 3.8 shows the relation between the absolute values of impedances $Z_A$ and $Z_B$ as a function of the frequency. As can be seen, $Z_A$ is much larger than $Z_B$ in the low-frequency range, which includes the transient frequency (11 $MHz$). The ratio between $Z_A$ and $Z_B$ is minimum at 200 MHz that is far above the transient equivalent frequency considered in this chapter. Above 200 MHz, the impedance $Z_A$ has the same behaviour as $Z_B$, i.e., $Z_A$ behaves

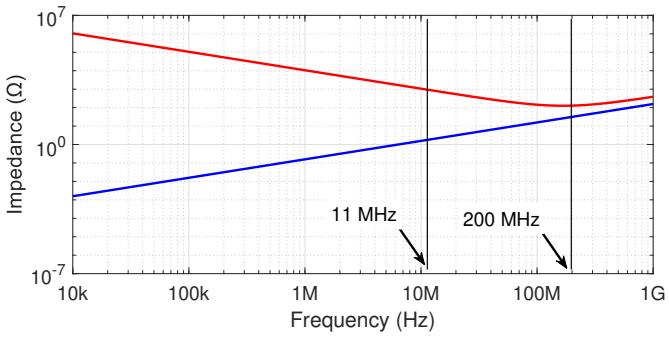



**Fig. 3.8.** $Z_A$ and $Z_B$ impedances of as a function of the frequency.

as an inductive impedance. At the transient frequency (11 $MHz$), $Z_A$ has an impedance of approximately 970 Ω, while $Z_B$ is approximately equal to 2 Ω. In other words, the majority of the current $I_1$ is deflected through the impedance $Z_B$, and therefore, the total CM current that circulates in the control side ($I_{CM}$) is drastically reduced. This analysis can be extended to the similar nodes $N_1$, $N_2$ and $N_3$ Fig. 3.6(b).

Based on the 1MGD theoretical approach presented in this section, seven gate drive power supply configurations have been investigated in this work. The main idea is to analyse new connections between the gate drive power supplies in order to reduce the CM currents in the control side. The new gate driver configurations are shown in Figs. 3.9-3.11.

Fig. 3.9(a) shows the first modified gate driver configuration (1MGD), where all gate drive power supplies are fully cascaded as already explained above. The 1MGD tends to provide a drastically CM current reduction since it provides three pathways (associated to the nodes $N_1$, $N_2$ and $N_3$) that forces the return of CM currents to the power side through the inductances $L_g$. The second modified gate driver configuration (2MGD) is shown in Fig. 3.9(b), where the gate driver 1 is powered by an external power supply, and all the other gate drivers are supplied by the gate driver 1. When compared to the TGD configuration, the 2MGD circuit tends to provide a good CM current reduction since it provides a pathway (associated to the node $N_1$) that forces the return of CM current $I_{123}$ to the power side through the inductance $L_g$.

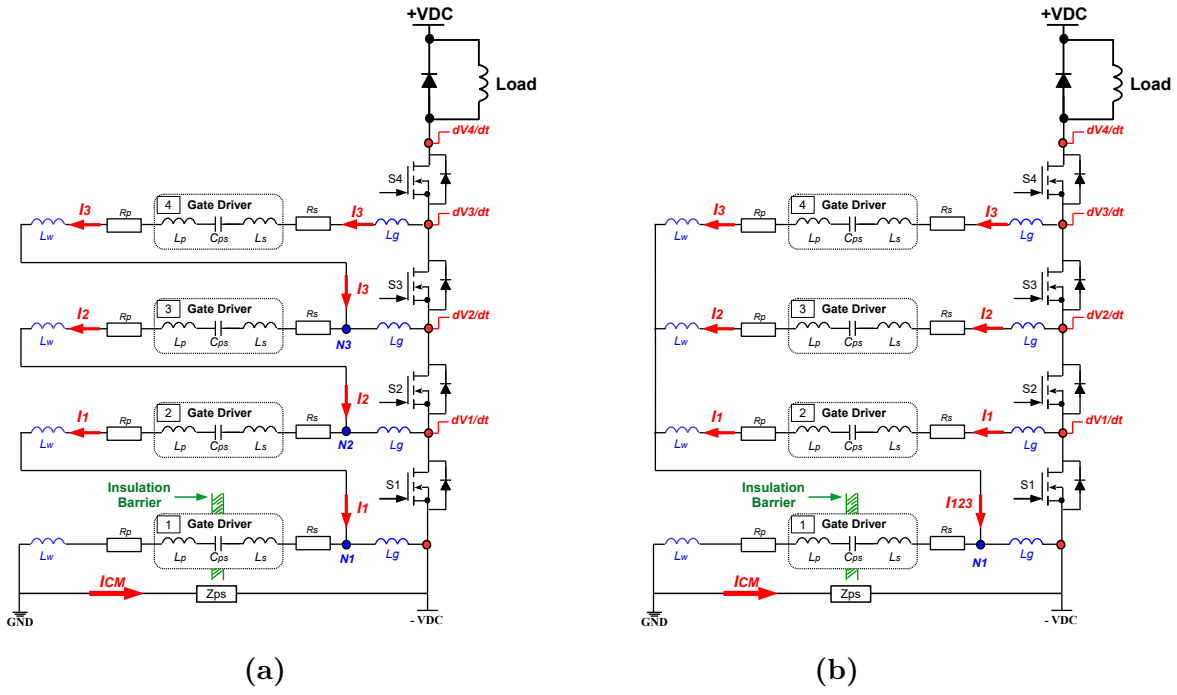
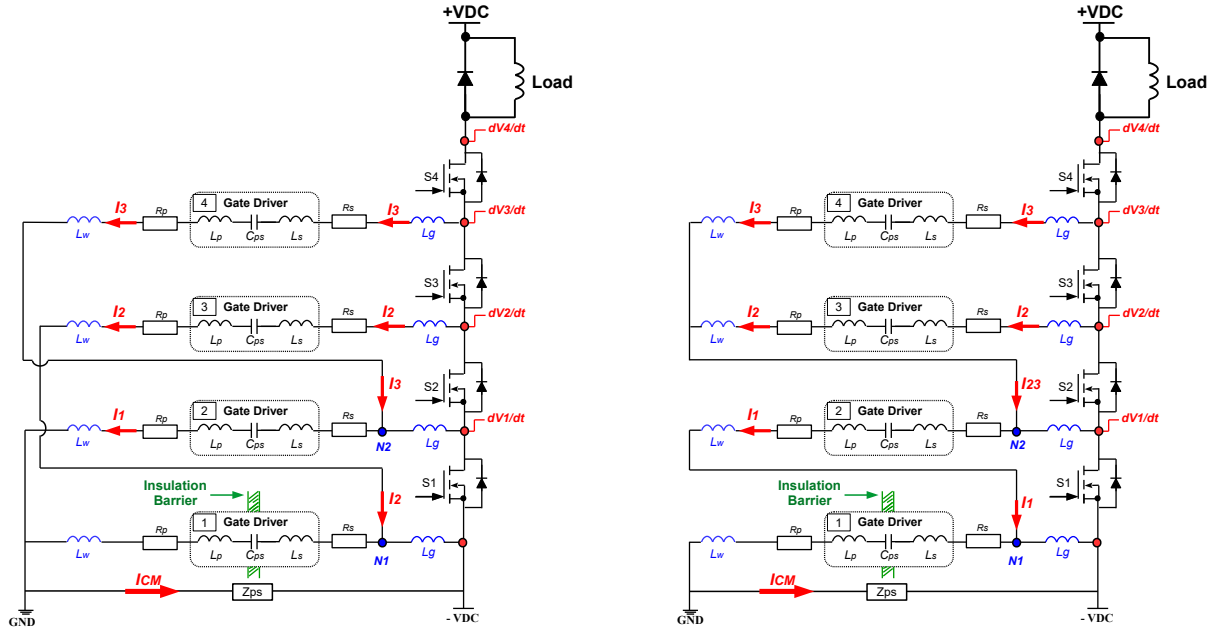



**Fig. 3.9.** Electrical schematic of 1MDG (a) and 2MGD (b) configurations.

Fig. 3.10(a) shows the third modified gate driver configuration (3MGD), where gate




**(a)** **(b)**

**Fig. 3.10.** Electrical scheme of 3MDG (a) and 4MGD (b) configurations.

drivers 1 and 2 are powered through an external power supply, gate driver 3 is supplied through gate driver 1, and gate driver 4 is supplied through gate driver 2. The 3MGD circuit provides two pathways ( associated with nodes $N_1$ and $N_2$) that forces the return of CM currents to the power side through inductances $L_g$. Similarly, as shown in Fig. 3.10(b), the fourth modified gate driver configuration (4MGD) provides two pathways (associated with nodes $N_1$ and $N_2$) that force the return of CM currents to the power side through the inductances $L_g$.

The fifth modified gate driver configuration (5MGD) is shown in Fig. 3.11(a), where gate driver 1 is powered through an external power supply, gate drivers 2 and 4 are powered through gate driver 1, and gate driver 3 is powered through gate driver 2. The 5MGD circuit provides two pathways (associated with nodes $N_1$ and $N_3$) that forces the return of CM currents to the power side through the inductances $L_g$. Similarly, as shown in Fig. 3.11(b), the sixth modified gate driver configuration (6MGD) provides two pathways (associated with nodes $N_1$ and $N_3$) that force the return of CM currents to the power side through the inductances $L_g$.

As can be seen, each proposed gate driver configuration has different characteristics of connections and equivalent gate driver impedances that can mitigate the CM current in the control side. The impacts of these characteristics on conducted CM currents are analysed in the next section by time-domain simulations.

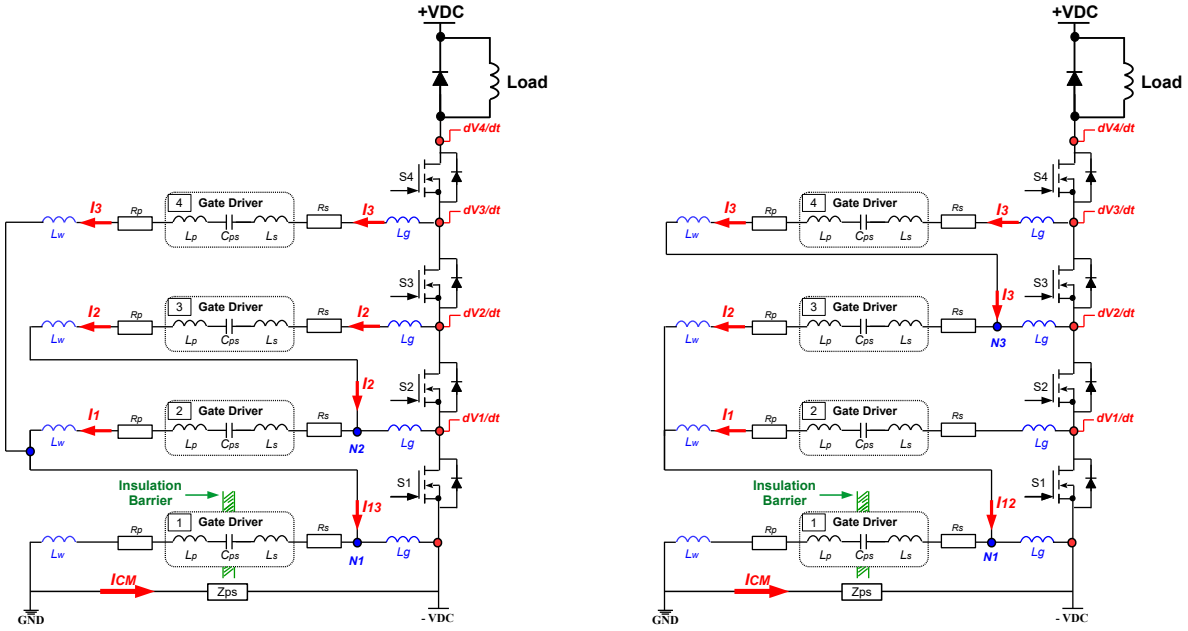



**Fig. 3.11.** Electrical circuits of 5MDG (a) and 6MGD (b) configurations.

### Theoretical Analysis and Time-domain Simulations

To analyse the gate drive power supply configurations from a theoretical point of view, electrical simulations are made in LTspice software with a Cree C2M SiC-MOSFET Spice model C2M0025120D (1200V, 90A). The main parameters used in the simulations are: 1kV DC bus voltage, 40A DC load current, gate-to-source voltages ranging from -5V to +20 V, rise time and fall time of 25 ns. The values used for the parasitic elements are the same as presented in Table 3.2.

Fig. 3.12 shows a comparison between the TGD and 1MGD configurations in terms of CM current. In the TGD configuration, a noisy current with a 6.8 A peak-to-peak value is computed at each switching transition. This current is significantly reduced in the proposed 1MGD configuration, which presents a CM current value of around 1.0 A. It means a reduction of round 85.3%. The 1MGD circuit presents the best results in term of CM current reduction since according to Fig. 3.6(b), the 1MGD provides three pathways (associated to the nodes $N_1$, $N_2$ and $N_3$) that force the return of CM currents through the inductances $L_g$.

Fig. 3.13 shows the CM currents for the TGD and 2MGD configurations. As can be seen, the CM current is reduced from 6.8 A to 2.9 A. It means a reduction of 57.3%. As expected, the 2MGD circuit has a good performance on CM current reduction. However, the 1MGD configuration still presents better performance. This is due to the fact that the 2MGD provides only one pathway (associated to the node $N_1$ in Fig. 3.9(b)) that allows the

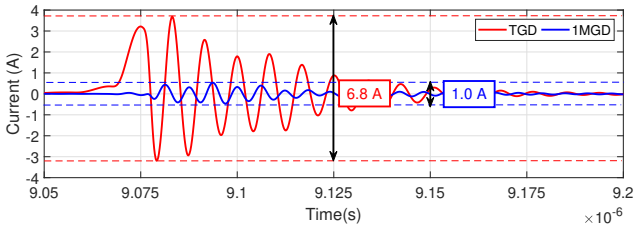



**Fig. 3.12.** CM current comparison between TGD and 1MDG configurations. Simulation Results.

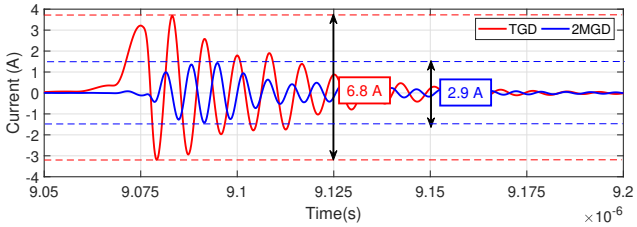



**Fig. 3.13.** CM current comparison between TGD and 2MDG configurations. Simulation Results.

return of the CM current $I_{123}$ to the power side through the inductance $L_g$.

The CM current simulation results for the 3MGD configuration are shown in Fig. 3.14. As can be seen, the CM current is reduced from 6.8 A to 3.1 A when 3MGD and TGD are compared. It means a reduction of 54.4%. Similarly to 2MGD, the 3MGD configuration also provides good conducted CM current reduction,although 3MGD is slightly worse. This is due to the fact that the currents $I_3$ and $I_2$, which are the most largest CM currents, have only one pathway to return to the power side. A part of $I_3$ can return to the control part only trough $L_g$ (associated to the node $N_2$ in Fig. 3.10(a)), and a part of $I_2$ can return to the power side only trough $L_g$ (associated with node $N_1$ in Fig. 3.10(a)). The 2MGD configuration has a similar impedance characteristic since the CM currents $I_1$, $I_2$ and $I_3$ have only one pathway to return to the power side as shown in Fig. 3.9(b). However, the current $I_1$ can not return to the power side without circulating in the control side in the 3MGD case. This explain why the 2MGD configuration is better than the 3MGD one.

Fig. 3.15 shows the simulation results for the 4MGD configuration. When compared to the TGD, the 4MGD reduces the CM current from 6.8 A to 1.7 A. It means a reduction of 75%. This large improvement is due to the low impedance associated to the node $N_2$ in Fig. 3.10(b), which allows that a part of the large CM current $I_{23}$ to return to the power side through the inductance $L_g$. Furthermore, a part of the current $I_1$ can also return to the power side through the inductance $L_g$, which is associated to the node $N_1$ in Fig. 3.10(b).

The simulation results for the 5MGD are shown in Fig. 3.16. As can be seen, the CM current is reduced from 6.8 A to 2.7 A, which represents a CM current reduction of 60.3%. As can be seen, the 5MGD provides a good conducted CM current reduction. However, the

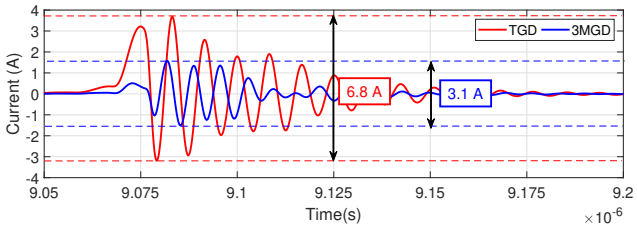



**Fig. 3.14.** CM current comparison between TGD and 3MDG configurations. Simulation Results.

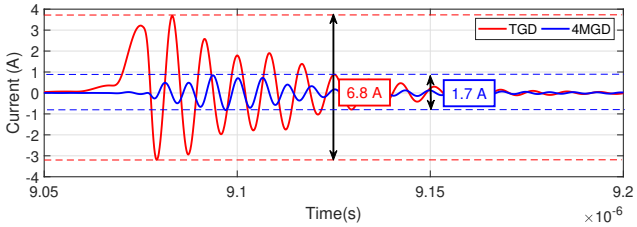



**Fig. 3.15.** CM current comparison between TGD and 4MDG configurations. Simulation Results.

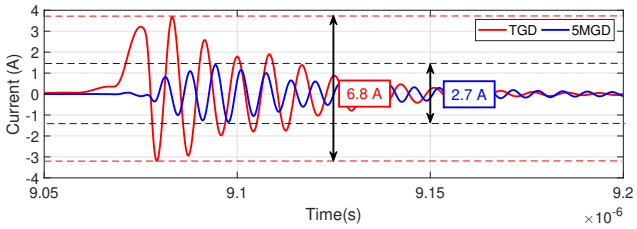



**Fig. 3.16.** CM current comparison between TGD and 5MDG configurations. Simulation Results.

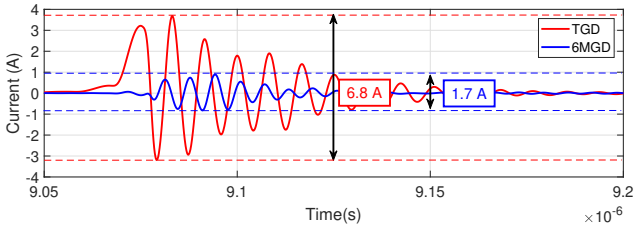



**Fig. 3.17.** CM current comparison between TGD and 6MDG configurations. Simulation Results.

large CM current $I_{13}$ in Fig. 3.11(a) has only one low impedance pathway $L_g$ (associated with node $N_1$ in Fig. 3.11(a)) to return to the power side. Note that $I_3$ is the largest CM current generated by a floating point since its associated $dv/dt$ is approximately 3 and 1.5 times larger than the $dv/dt$ associated to $S_1$ and $S_2$ drain potentials, respectively.

The results for the last analysed gate driver configuration is shown in Fig. 3.17. In the 6MGD, a CM current of around 1.7 A is presented. It means a CM current reduction of 75%. The 6MGD also provides an excellent CM current reduction. This is due to the fact that the largest CM current $I_3$ is initially decomposed by its associated node $N_3$ in Fig.

3.11(b). It means that most of current $I_3$ returns to the power side through $L_g$ right on the first connection associated to node $N_3$. Thereafter, most of the current $I_{12}$ returns to the power side through the inductance $L_g$ associated to node $N_1$.

The six new proposed gate driver configurations present better performance than TGD in terms of conducted CM current reduction. 1MGD, 4MGD and 6MGD present the best results. In these three configurations, a common characteristic can be observed: most of the largest CM current $I_3$ is returned to the power side through an inductance $L_g$ associated to a node different from the node $N_1$. For example, in Fig. 3.10(b) for the 4MGD, most of the two largest CM currents $I_3$ and $I_2$ ($I_{23}$) returns to the power side through the inductance $L_g$ associated to the node $N_2$. It means that only a small part of $I_{23}$ plus the CM current generated at $S_1$ drain potential($I_1$) continues to circulate through the power supply 2. Thereafter at node $N_1$, the current $I_1$ is also deflected to the power side through inductance $L_g$, and only a very small current circulates through power supply 1 and goes to the control side. Note that, as explained in Fig. 3.5, the driver circuitry impedance is drastically higher than the impedance of the inductance $L_g$. This is the reason why most of CM currents are deflected to the inductance $L_g$ returning to the power side.

In brief, since node $N_1$ is the node associated to the isolation barrier that mitigates the CM currents in the control side, the current that arrives at the node $N_1$ has to be the smallest possible.

### 3.1.3 Experimental Results

To validate the theoretical analysis and the simulation results, a switching cell prototype with four C2M0025120D (1200V, 90 A) silicon carbide power MOSFETs connected in series for the low side and one STMicroelectronics schottky silicon carbide diode STPSC40H12CWL for the high side is developed. The DC-DC converter implemented for each gate driver used in the experiment is a Murata MGJ6D242005SC with an isolation voltage and parasitic capacitance of 5.7 kVDC and 15 pF, respectively. Optical fibers are used to achieve high signal isolation (very low parasitic capacitance). The top and bottom view of the switching cell prototype is shown in Fig. 3.18. A bus voltage of 1 kV and a load current of 40 A are used to investigate the gate driver configurations. As no heatsink is attached to the devices, the experiments are performed in pulsed mode.

The conducted CM current that circulates in the control side is measured by adding an additional impedance $Z_M$ (10 M$\Omega$//10 nF) as shown in Fig. 3.19, where the parasitic elements of the gate driver power supply and its connections are presented. As can be seen, two reference potentials are considered, i.e., the ground reference potential of the remote control circuit (VCR) and the reference potential of the power circuit (-VDC). Both VCR and -VDC are isolated from each other. According to Fig. 3.19, the CM current circulates

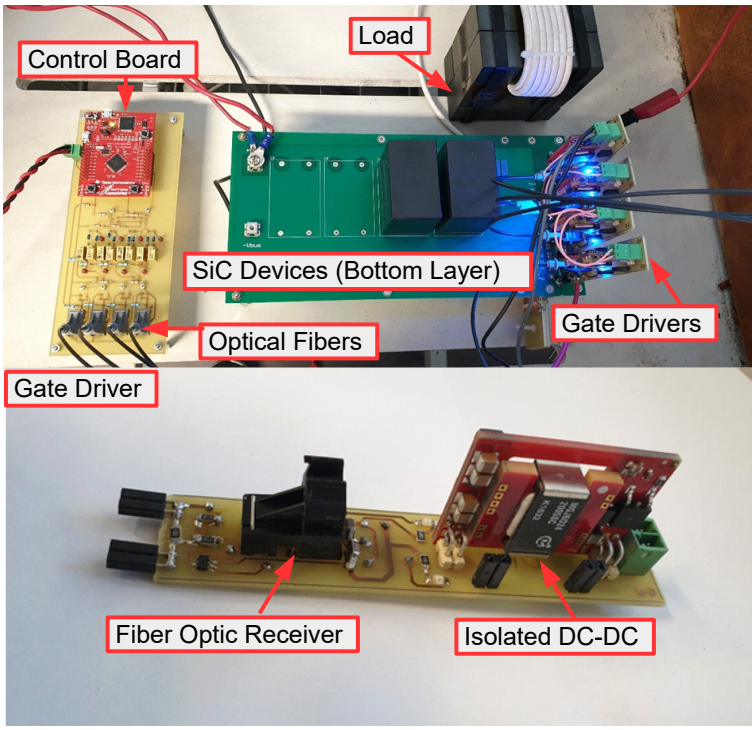



**Fig. 3.18.** Switching cell prototype of four series-connected SiC-MOSFETs.

from the power side to the control side through the gate drive parasitic capacitances $C_{ps}$. Then, the CM current circulates through $C_{gnd1}$ and $C_{gnd2}$, which are the VCR to ground and -VDC to ground parasitic capacitances, respectively. This is the natural pathway of the CM current in the control side. To measure the CM current, an additional impedance $ZM$ (characterized by a capacitor $C_{ZM} \gg C_{gnd1} + C_{gnd2}$) is connected between VCR and -VDC to concentrate and measure the noise current that circulates in the driver circuit. In other words, to facilitate the conducted EMI measurements, ZM is added to short-circuit $C_{gnd1}$ and $C_{gnd2}$. Therefore, the total amount of the common mode current in the control side circulates through $ZM$. The proposed measurement technique can be validated by simulation (LTSpice software) as shown in Fig. 3.20. In a first step, the CM current is measured without ZM, i.e., the current that circulates through $C_{gnd1}$ (1 nF) and $C_{gnd2}$ (1 nF). Then, the impedance $ZM$ characterized by a capacitor $C_{ZM}$ (10 nF) is added between VCR and -VDC. As can be seen, practically, all the CM current is deflected to $ZM$. The simulations were done for many acceptable values of $C_{gnd1}$, $C_{gnd2}$ and $C_{ZM}$, as well as for many values of load current and $dv/dt$, and all the simulation results are similar to the shown in Fig. 3.20.

### Time Domain Experimental Results

The experimental results depicted in Fig. 3.21 show the behaviour of conducted CM current that circulates in the control side in the TGD configuration. A noise current of 4.2 A peak-to-peak is measured. This value is the reference used to investigate the CM current

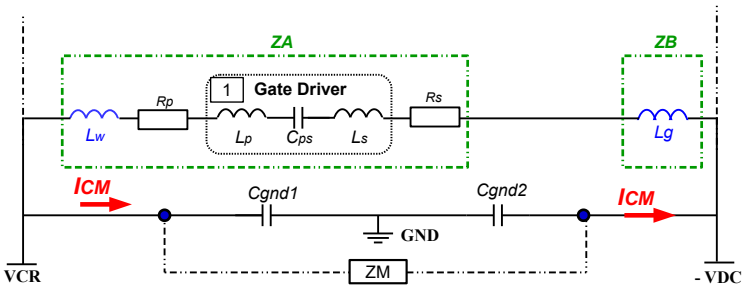



**Fig. 3.19.** Measurement method illustration.

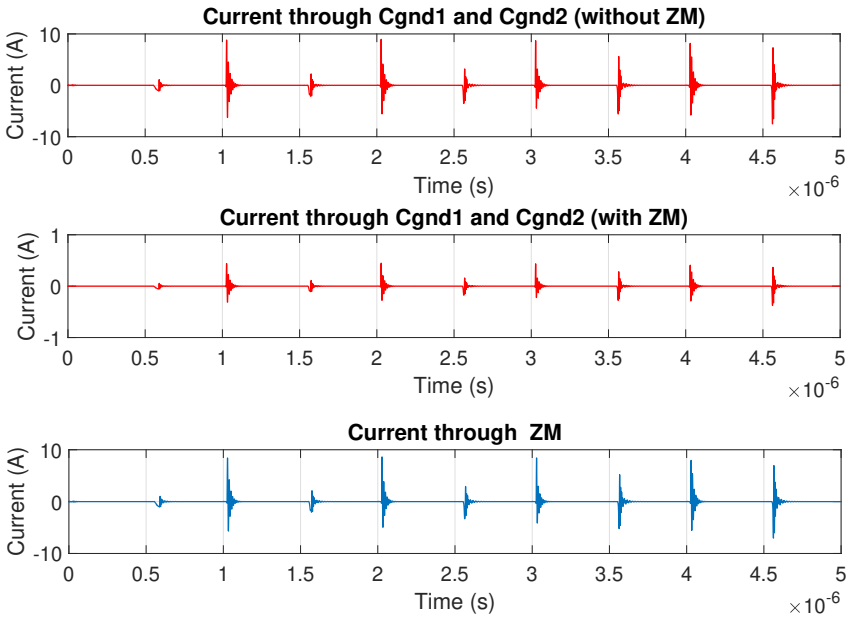



**Fig. 3.20.** CM current waveforms with and without $ZM$.

reduction in the other gate driver configurations.

The conducted CM currents in the six proposed gate driver configurations are shown in Figs. 3.22-3.27. As can be seen for the 1MGD case, a CM current of around 1.9 A is measured. Compared to the TGD configuration, 1MGD reduces the conducted CM current by 54.7 %. In the 2MGD and 3MGD configurations, CM currents of 2.1 and 2.7 $A$ are measured respectively. These results represent a CM current reduction of 50 and 35.7 %, receptively. The other three gate configurations, i.e., 4MGD, 5MGD and 6MGD present similar results between them. CM currents of 1.9 A, 1.9A and 1.8 A are measured. When compared to the TGD, it means a CM current reduction of approximately 55 %.

As can be seen, the theoretical approach developed in this chapter is validated in this section by experimental results. Some discrepancies between the simulation and experimental results can be observed. This is due to the complexity to characterize each element in the gate drive circuitry and switching cell. Furthermore, the simulation analyses are done in the case where the gate drivers are identical. However, each gate driver can introduce different

parasitic capacitances. This opens an opportunity to perform a gate driver parameters sensitive analysis in future works.

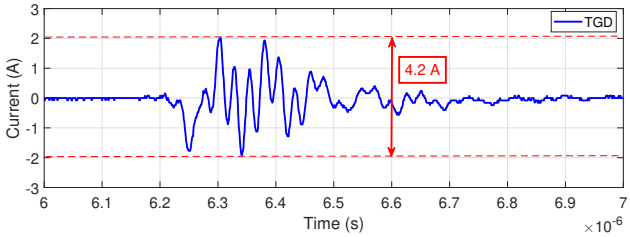



**Fig. 3.21.** CM current in the TGD configuration. Experimental Result.

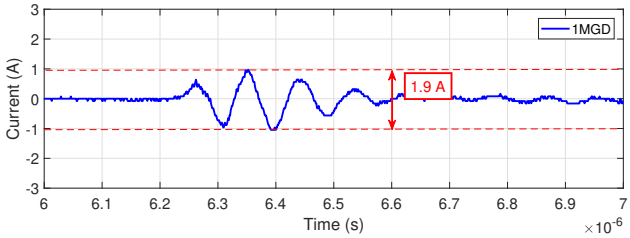



**Fig. 3.22.** CM current in the 1MDG configuration. Experimental Result.

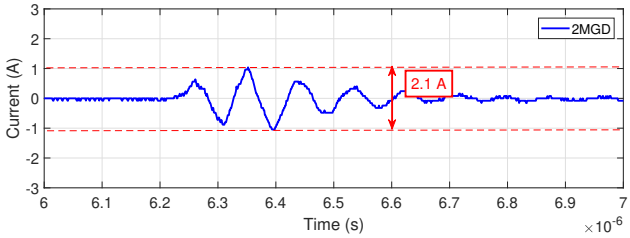



**Fig. 3.23.** CM current in the 2MDG configuration. Experimental Result

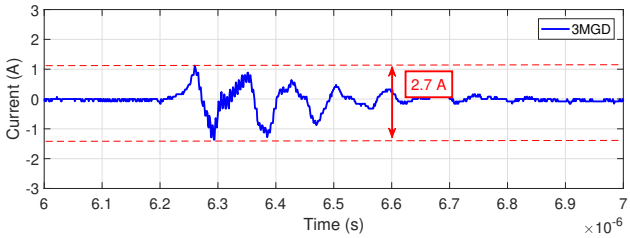



**Fig. 3.24.** CM current in the 3MDG configuration. Experimental Result

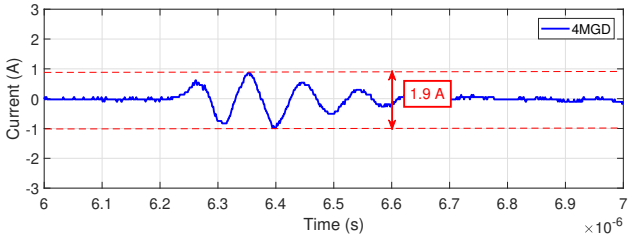



**Fig. 3.25.** CM current in the 4MDG configuration. Experimental Result

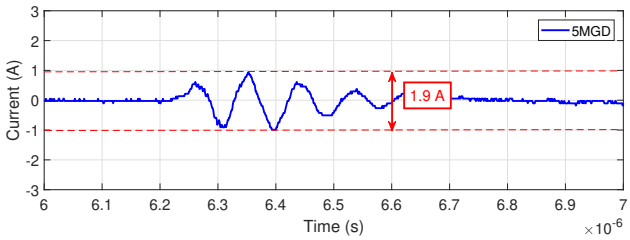



**Fig. 3.26.** CM current in the 5MDG configuration. Experimental Result

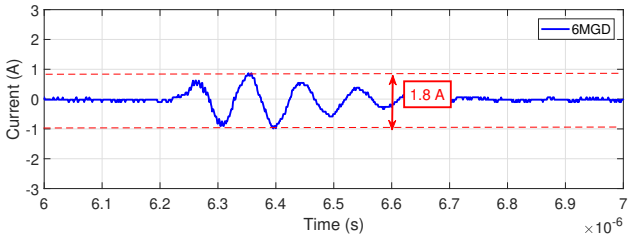



**Fig. 3.27.** CM current in the 6MDG configuration. Experimental Result.

### Frequency Domain Experimental Results

To investigate the conducted CM current reduction in the frequency domain, spectral analyses are done. The data of the common mode currents is acquired using a DSOX3024T Keysight Oscilloscope and the spectrum is calculated using MATLAB software. Note that the spectral analysis proposed in this chapter is not a standard analysis, i.e., no Line Impedance Stabilization Network (LISN) is used during the experiments. However, the proposed measurement method is useful to compare the gate driver configurations with each other. The conducted EMI spectra in the range of 20 kHz to 500 MHz is shown in Figs. 3.28-3.33.

Fig. 3.28 shows the EMI spectra for the TGD and 1MGD configurations. The proposed 1MGD configuration reduces the conducted CM noise, practically, in all 1- 8 MHz and 20 - 50 MHz ranges. The most notable improvements are $\approx$ 9dB in the 4-7 MHz range, and $\approx$ 21dB at 40 MHz. The 2MGD configuration has similar result to the 1MGD one as shown in Fig. 3.29, where the most notable improvements are also $\approx$ 9dB in 4-7 MHz range, and $\approx$ 21dB at 40 MHz.

As shown in Fig. 3.30, the 3MGD configuration provides a CM noise reduction, practically, in all 3- 8 MHz and 20 - 50 MHz ranges. The most notable improvements are $\approx$ 9dB in 4-7 MHz range, and $\approx$ 15dB at 40 MHz. Around 20 MHz, the TGD configuration presents better CM noise attenuation than the 3MGD.

The other three gate driver configurations, i.e., 4MGD, 5MGD and 6MGD provide similar CM noise current reductions in all 1-8 MHz and 20-50 MHz ranges. The most notable improvements are $\approx$ 9dB in 4-7 MHz range, and $\approx$ 21dB at 40 MHz.

As can be seen, all the proposed gate driver configurations provide a considerable CM

noise reduction. Only the 3MGD one has a worse performance than the TGD configuration around 20 MHz. In all cases, from 40MHz to 50MHz the amount of noise reduction decreases with the increasing of frequency. Furthermore, for frequencies of less than 1 MHz and more than 50 MHz, the noise reduction is not so effective.

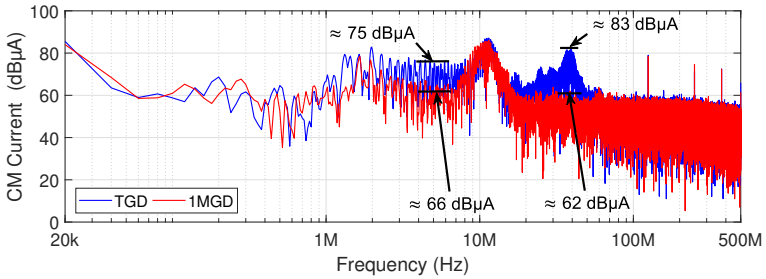



**Fig. 3.28.** Spectral CM current comparison between TGD and 1MDG configurations. Experimental Results.

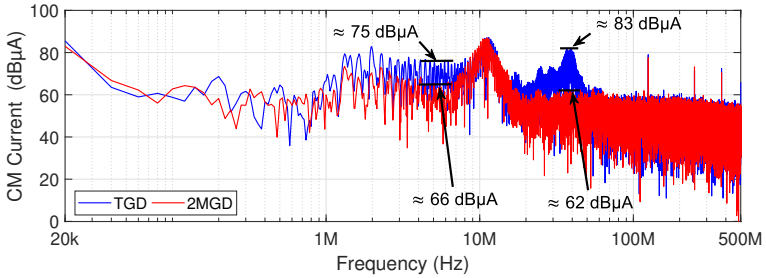



**Fig. 3.29.** Spectral CM current comparison between TGD and 2MDG configurations. Experimental Results.

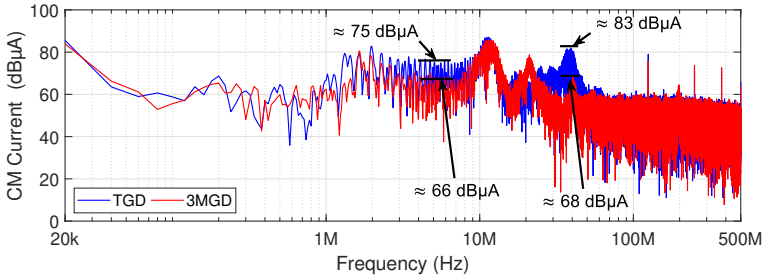



**Fig. 3.30.** Spectral CM current comparison between TGD and 3MDG configurations. Experimental Results.

It is clear that the control system could be damaged by a large amount of the noise current that may flow through the control parts if the gate drive power supplies are not taken into account in the system implantation. Efforts must be engaged not only toward the design and implementation of gate drivers but also toward the gate drive power supplies. The analytical analysis and experimental results validate the proposition of this section. Modifying the gate drive power supply configuration is an effective technique to reduce the noise current in the control part and to increase the reliability of the control system.

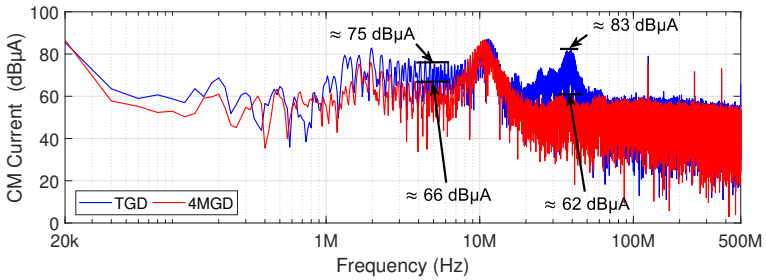



**Fig. 3.31.** Spectral CM current comparison between TGD and 4MDG configurations. Experimental Results.

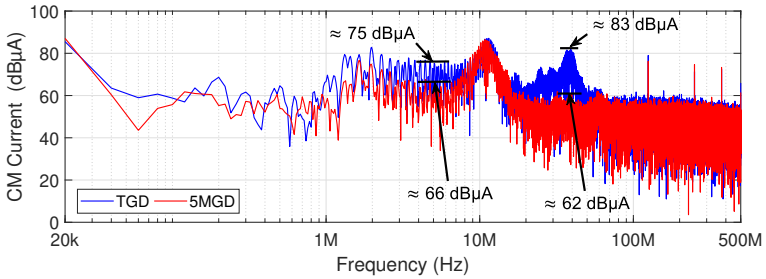



**Fig. 3.32.** Spectral CM current comparison between TGD and 5MDG configurations. Experimental Results.

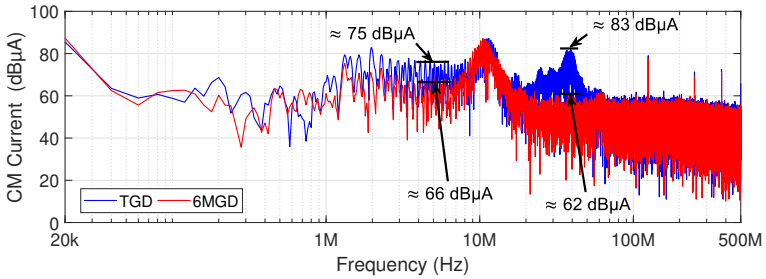



**Fig. 3.33.** Spectral CM current comparison between TGD and 6MDG configurations. Experimental Results.

For optimal design, the power rating of the DC/DC converters has to be taken into account. The advantages offered by the proposed gate drive supply configurations must be mitigated by the increased complexity and the additional power consumption due to the series-connected power supplies. The gate drive power supplies must be designed carefully since their power ratings are changing from one to another, specially for the configurations where only one gate drive power supply must supply all the other drive circuits. A deeper analysis about optimal design in terms of power rating, volume, efficiency, and parasitic currents has been addressed in [81].

## 3.2 Impact of the gate driver parasitic capacitances on the switching cell $dv/dt$

In this section, the equivalent parasitic capacitances of the TGD and new gate driver supply configurations are analysed in order to investigate their impact on the switching cell $dv/dt$. In this analysis, only the behaviour during the voltage transient across the power devices is considered with the help of simplified high frequency equivalent circuits. The main parasitic capacitances taken into account to develop the high frequency equivalent circuits (based on parasitic capacitances) are depicted in Fig. 3.34 where two MOSFETs are connected in series. Table 3.1 describes the main elements of the equivalent circuit shown in Fig. 3.34.

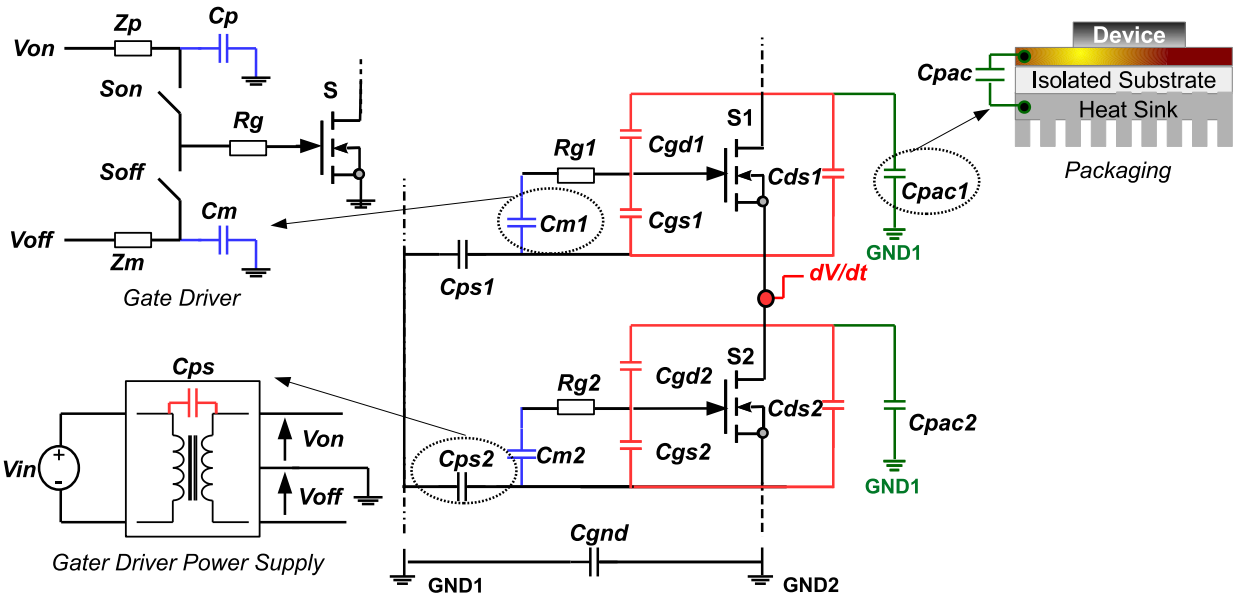



**Fig. 3.34.** Simplified capacitive model with the main parasitic capacitances.

Note that, in Fig. 3.34, the parasitic inductances and the drain and source resistances are ignored to facilitate the analytical analysis, i.e., only the parasitic capacitances are added to clarify their impacts on the dynamic behaviour of the power devices. In the analysis, it is considered that all transistors are identical, the parasitic capacitances introduced by the packaging have the same values, and all isolated gate driver power supplies have identical parasitic capacitances despite the different configurations to supply the gate drivers.

### Traditional Gate Drive Power Supply Configuration (TGD)

The traditional gate driver architecture is shown in Fig. 3.35. Each isolated power supply of each gate driver is supplied by an external power supply. In this inverter leg configuration, there are three sources of perturbation produced by three floating points. As

**Table 3.3**
Elements of the equivalent circuit shown in Fig. 3.34.

| Element | Description |
|---|---|
| $C_{ps}$ | Parasitic capacitance of the isolated DC/DC converter. |
| $C_m$ | Decoupling capacitance of the gate driver buffer for negative voltage. |
| $R_g$ | Gate resistance. |
| $C_{pac}$ | Drain-ground parasitic capacitance. |
| $C_{gd}$ | MOSFET gate-drain parasitic capacitance. |
| $C_{ds}$ | MOSFET drain-source parasitic capacitance. |
| $C_{gs}$ | MOSFET gate-source parasitic capacitance. |
| $C_{gnd}$ | Parasitic capacitance between the ground control circuit (GND1) and the ground power circuit (GND2). |

can be seen in Fig. 3.34, each floating point that has a high $dV/dt$ is directly connected to the parasitic capacitance introduced by the gate driver power supply ($C_{ps}$). As will be explained in this section, the switching speed of the devices is a function of the parasitic capacitances introduced by the gate driver circuitry.

To analyse the influence of the gate driver configuration on the $dV/dt$ of the switching cell middle point, a high frequency equivalent circuit of two pairs of series-connected transistors is shown in Fig. 3.36(a). The analysis is done when transistors $S_1$ and $S_2$ are turned-off and transistors $S_3$ and $S_4$ are turning-off. As shown in Fig. 3.36(b), the simplified high frequency equivalent circuit is obtained by short circuiting the electrodes of large capacitors/voltage supplies such as power side DC bus (VDC) and the power circuit ground (GND2) [31, 70].

As is well known, the gate current required to charge and discharge the internal gate capacitances is limited by the gate resistances. Consequently, the switching speed of the device is drastically dependent of $R_g$. The lower the gate resistance, the faster the internal gate capacitances charges, and consequently, the higher the switching speed of the transistor. In other words, $R_g$ is an important parameter that controls $dV/dt$. Therefore, to propose an analytical model that represents the maximum voltage speed of the switching cell, and in order to compare the gate driver architectures, the gate resistances are set to zero as shown in Fig. 3.36(b). Note that if the total gate resistance is zero, the gate current is large enough to cancel the Miller plateau effect. In this case, the channel current of the MOSFET could be equal to zero [82]. Consequently, the channel current source is no longer represented in Fig. 3.36(b).

With the help of the simplification process presented in [31], *i.e.*, parallel and series associations of parasitic capacitances, an equivalent high frequency electrical circuit is generated

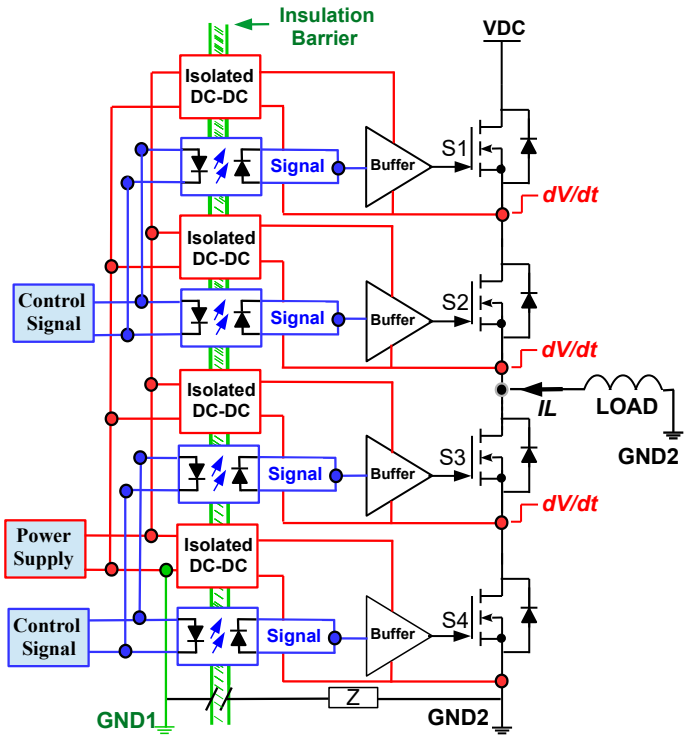



**Fig. 3.35.** Traditional Gate Driver Architecture Configuration (TGD).

as shown in Fig. 3.37.

Where:

- $C_{eq(TGD)}$ is the equivalent parasitic capacitance for the traditional gate driver architecture given by Eq. (3.9).

$$C_{eq(TGD)} = \frac{C_s^3(6k+2)+C_s^2[C_{pac}(6k^2+4k)+C_{gpac}(2k^2+4k+1)]+C_s[C_{pac}(2k^2C_{pac}+4k^2C_{gpac}+2kC_{gpac})]+k^2C_{gpac}C_{pac}^2}{C_s^2(6k+1)+C_s[C_{pac}(6k^2+2k)+C_{gpac}(2k^2+k)]+k^2C_{pac}^2+k^2C_{gpac}C_{pac}} \quad (3.9)$$

- $C_s$, expressed by Eq. (3.10), is the association between the intrinsic MOSFET capacitances and the decoupling capacitance of the buffer for negative voltage ($C_m$).

$$C_s = \frac{(C_{gs}+C_m)C_{gd}}{C_{gs}+C_m+C_{gd}} + C_{ds} \quad (3.10)$$

- $C_{gpac}$, expressed Eq. (3.11), is the parallel association between $C_{gnd}$ , $C_{pac}$, and $C_{ps}$.

$$C_{gpac} = C_{gnd} + C_{pac} + C_{ps} \quad (3.11)$$

- the $k$ $factor$, expressed by Eq. (3.12), is the ratio between $C_s$ and $C_{ps}$.

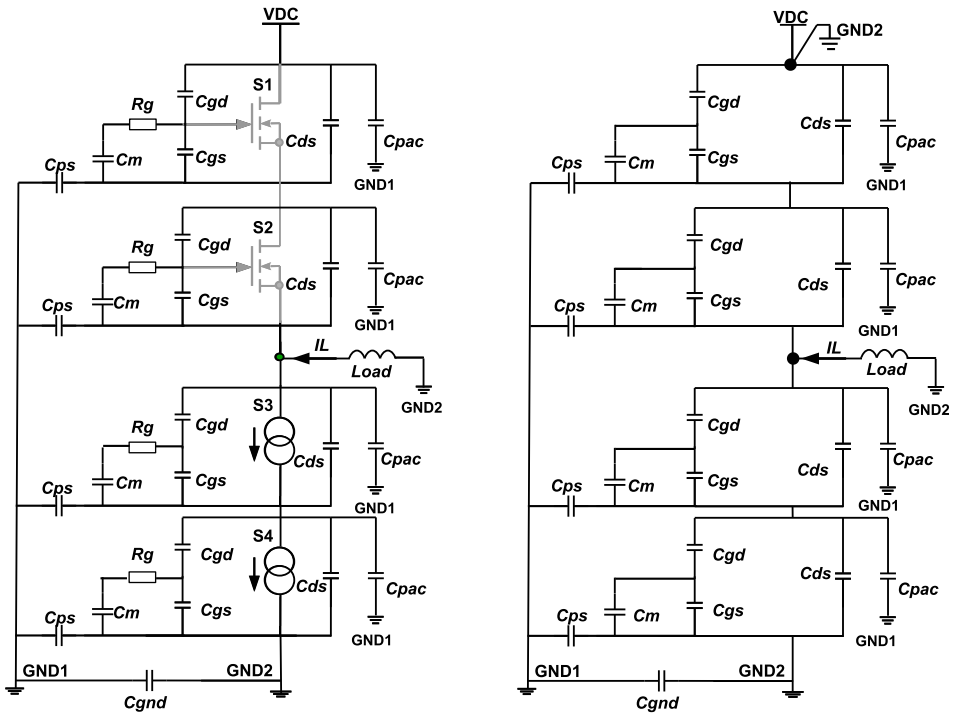



**Fig. 3.36.** TGD: high frequency (a) and simplified (b) models.

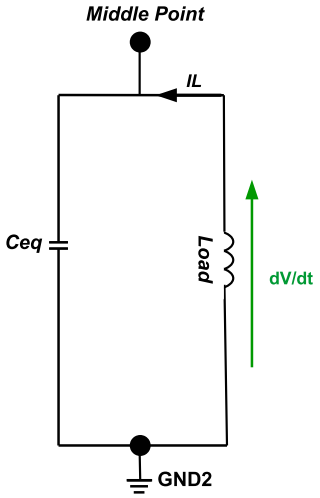



**Fig. 3.37.** Equivalent switching cell model (TGD).

$$k = \frac{C_s}{C_{ps}} \tag{3.12}$$

Now, with the equivalent model of the traditional gate driver architecture, the $dV/dt$ as a function of the equivalent parasitic capacitance for an inverter leg with two pair of MOSFETs connected in series can be expressed easily. According to Fig. 3.37, the $dV/dt$ between the output of the inverter leg (middle point MP) and the common potential reference (GND2),

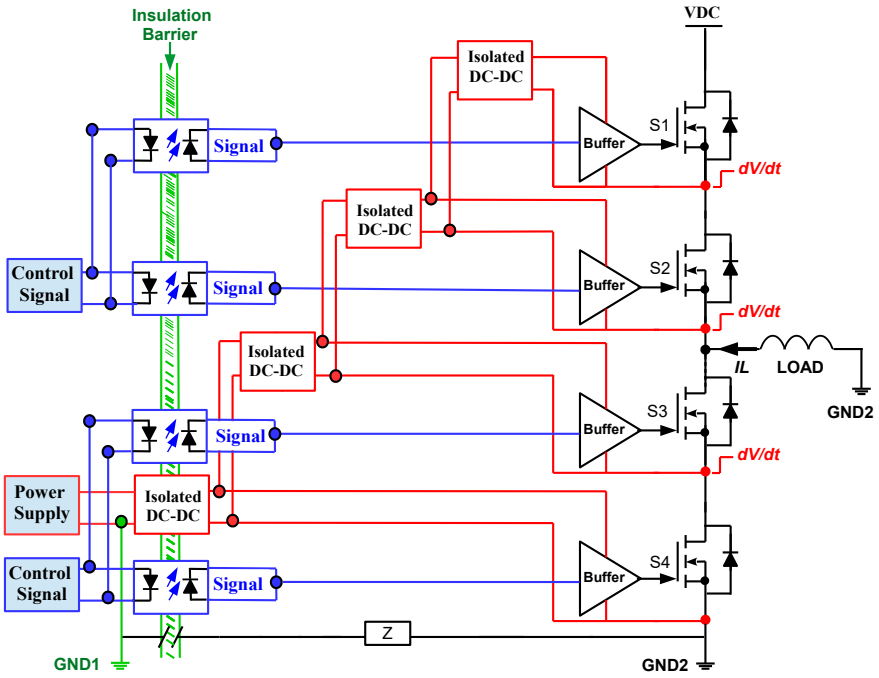



**Fig. 3.38.** Cascaded Gate Driver Configuration (CGD).

can be expressed by Eq. (3.13).

$$\frac{dv}{dt}(_{TGD}) = \frac{I_L}{C_{eq(TGD)}} \tag{3.13}$$

As can be seen, the switching speed of switching cells is a function of the equivalent parasitic capacitance. According to Eq. (3.13), the $dV/dt$ at the middle point of the switching cell can be increased by reducing the equivalent parasitic capacitance. To this end, a new gate driver power supply configuration is proposed in the next subsection.

### Cascaded Gate Drive Power Supply Configuration (CGD)

The proposed gate driver architecture is shown in Fig. 3.38. In this configuration, the power supplies are fully cascaded; only the DC/DC converter of gate driver 4 (related to the device $S_4$) is powered by an external power supply, all other isolated DC/DC converters are powered by the previous DC/DC converter. Thus, gate driver 3 is powered by gate driver 4, gate driver 2 is powered by gate driver 3, and gate driver 1 is powered by gate driver 2. Note that the control signal configuration is the same for the both gate driver architectures. The cascaded gate driver configuration (CGD) is similar to the 1MGD one presented in the section 5.1.

To analyse the impact of this architecture on the $dV/dt$ of the switching cell middle point, its equivalent electrical circuit is presented in Fig. 3.39(a). As shown in Fig. 3.39(b), the simplified high frequency equivalent circuit is achieved by short circuiting the electrodes of

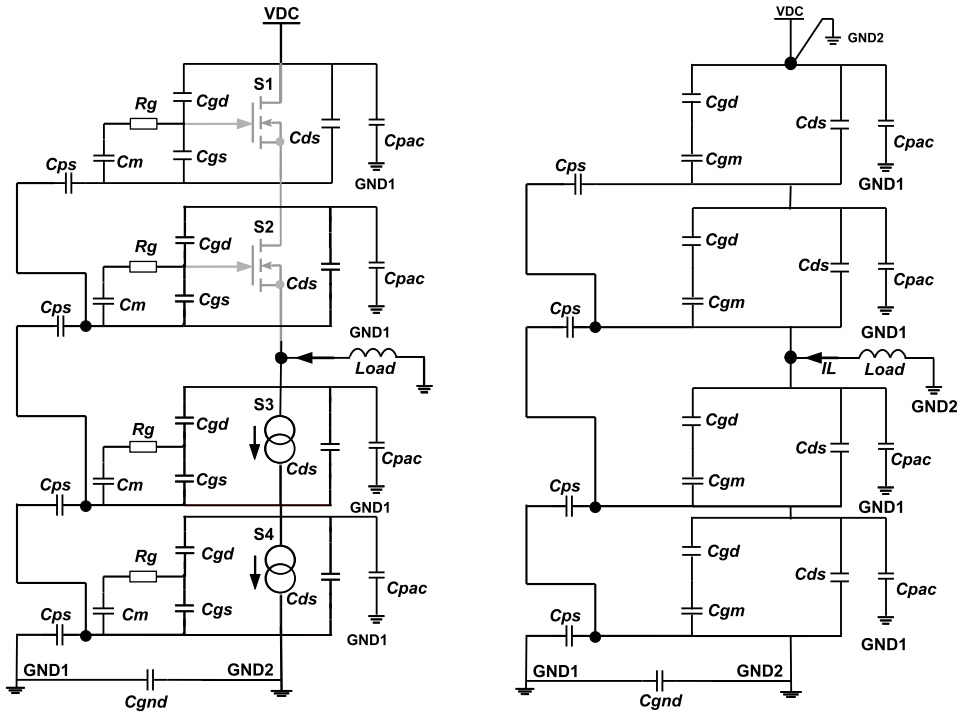



**Fig. 3.39.** CGD: high frequency (a) and simplified (b) models.

large capacitors/voltage supplies such as power side DC bus (VDC) and the ground of power circuit (GND2). As can be seen in Fig. 3.40, an equivalent high frequency electrical scheme is achieved by simplification process, *i.e.*, parallel and series associations of the parasitic capacitances. Note that the circuit shown in Fig. 3.40 is similar to the circuit shown in Fig. 3.37. However, their equivalent parasitic capacitances are expressed by different equations, i.e., Eqs. (3.9) and (3.14).

$$C_{eq(CGD)} = \frac{C_s(2k+1)}{2k} + \frac{C_{pac}}{2} \tag{3.14}$$

As can be seen, the first notable characteristic of the proposed architecture, is that its equivalent parasitic capacitance is described by a simple equation, which allows a better understanding of how these capacitances can affect the voltage balancing [9], the EMI [13,70], and the switching speed of the series connected devices [71, 83].

Eq. (3.15) gives the switching voltage speed of the middle point for the cascaded gate driver architecture.

$$\frac{dv}{dt}(_{CGD}) = \frac{I_L}{C_{eq(CGD)}} \tag{3.15}$$

Therefore, with the help of Eqs. (3.13) and (3.15), the $dv/dt$ at the middle point of the switching cell can be analysed and compared for both investigated gate driver configurations.

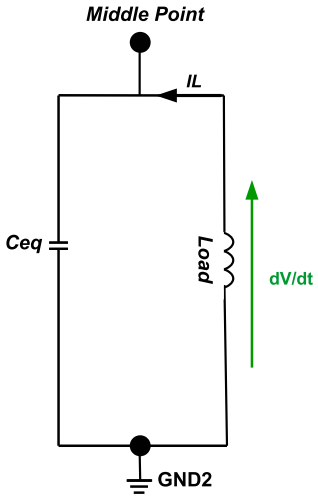



**Fig. 3.40.** Equivalent switching cell model (CGD).

### Traditional and Cascaded Gate Drive Power Supply Configurations: Analytical Analysis

Up to now, it has been considered that the parasitic capacitances of the power transistor equivalent model are constant. However, they are significantly dependent on the voltage level and significantly decrease when the drain-source voltage ($V_{ds}$) increases. For example, in the SPD02N50C3 Si power devices (500 V, 1.8 A) that are used in this work, the output capacitances ($C_{OSS}$) significantly decrease when $V_{ds}$ increases above the value of 50 V as depicted in Fig. 3.41. In other words, the $k\ factor$ ($C_s/C_{ps}$) changes during the power devices switching transition, *i.e.*, the $dV/dt$ value, during the same switching event, is not constant as was considered in analytical approach above.

To investigate the $dV/dt$ considering the $C_{OSS}$ variation, Fig. 3.42(a) shows the equivalent parasitic capacitance as a function of the $k\ factor$ for TGD and CGD. The curves in Fig. 3.42(a) are generated using Eqs. (3.9) and (3.14), and the values in Table 3.4. Note that $C_{pac}$ value is considered equal to zero, since no heatsink is used in this work. However, $C_{pac}$ can still be present due to PCB layouts, which can impacts the individual switching speed prediction of each gate driver architecture. Nevertheless, the gain on the switching speed (CGD/TGD) is practically independent of $C_{pac}$. The same can be said about the output inductor capacitance, which is not taken into account in the models.

As can be seen, the proposed CGD exhibits always the lowest global capacitance value. At $k$ =1, TGD and CGD have equivalent parasitic capacitances equal to 173 pF and 120 pF, respectively. It means that when the CGD is used, the equivalent parasitic capacitance can be reduced by 44% in relation to TGD.

To analyse the improvement on the switching speed of the CGD compare to the classical TGD architecture, even with the intrinsic parasitic capacitance variation, Eqs. (3.13) and (3.15) are used to express the equivalent parasitic capacitance ratio and the switching speed

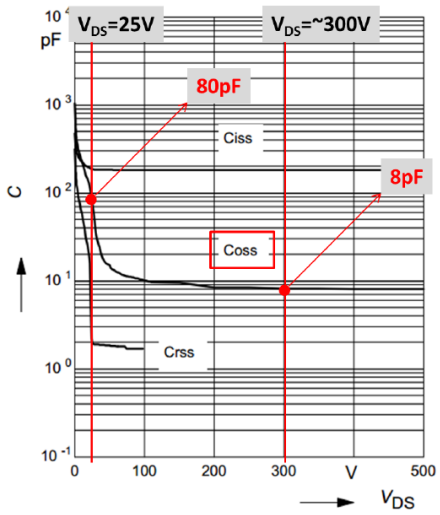



**Fig. 3.41.** $C_{oss}$ Capacitance variation as a function of drain-source voltage.

**Table 3.4**
Element values of the HF equivalent circuit.

| Element | Value | Description |
|---|---|---|
| $C_{ps}$ | 86 pF | Estimated primary-secondary parasitic capacitance for the power supply gate drivers used in this work [84]. Conditions: Vin = 15V, load = 90mA. |
| $C_m$ | 10 uF | Estimated decoupling capacitance of the gate driver buffer for negative voltage. |
| $C_{pac}$ | 0 | No heat sink is used in the experiments. Therefore, this parasitic capacitance can be neglected. |
| $C_{gd}$ | 2 pF | $C_{gd} = C_{rss}$; Gate-drain parasitic capacitance estimated from the datasheet of the devices used in this work [85]. Conditions: $V_{gs}$ = 0V, $V_{ds}$ = 25V. |
| $C_{ds}$ | 48 pF | $C_{ds} = C_{oss}$ - $C_{rss}$; Drain-source parasitic capacitance estimated from the datasheet of the devices used in this work [85]. Conditions: $V_{gs}$ = 0V, $V_{ds}$ = 25V. |
| $C_{gs}$ | 188 pF | $C_{gs} = C_{iss}$ - $C_{rss}$; Gate-source parasitic capacitance estimated from the datasheet of the devices used in this work [85]. Conditions : $V_{gs}$ = 0V, $V_{ds}$ = 25V. |
| $C_{gnd}$ | 1 nF | Estimated parasitic capacitance between the ground control circuit (GND1) and the ground power circuit (GND2). |

ratio between TGD and CGD architectures as a function of the $k$ *factor* (Fig. 3.42(b)). The values in Table 3.4 are used for both gate driver architectures.

As can be seen, the improvement on the switching speed, when CGD is used, is very significant when $k$ is around 0.4. The improvement is slightly reduced when $k$ increases,

*e.g.*, if an isolated power supply with ultra-low parasitic capacitance between the primary side and secondary side ($C_{ps}$) is used in the gate driver circuit, the $k\ factor$ ($C_s/C_{ps}$) will increase, and the gain on the switching speed will be reduced. On the other hand, when $Cs$ is very low and $C_{ps}$ is very dominant ($k\ factor < 0.4$) the gain on the switching speed is severely reduced. It means that, if $C_{ps}$ is very dominant, it will drastically slow down the switching speed of the devices, and modifying the gate driver architecture can have no effect on the switching speed of the devices. In any case, according to Fig. 3.42(b), a gain between 20% and 50% can be achieved for $k\ factors$ between 0.2 and 4. Note that in Fig. 3.42(b) the dots represent the switching speed ratio (1.43) and the equivalent parasitic capacitance ratio (0.7) for a $k\ factor$ equal to 1. As will be explained in the next section, choosing a $k\ factor$ equal to one, the presented study can be seen as a general case.

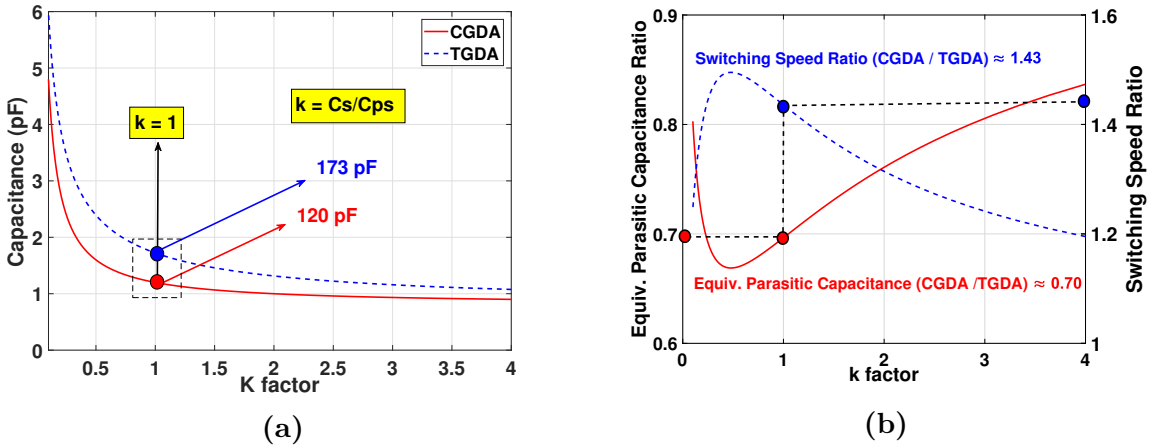



**Fig. 3.42.** Equivalent capacitances (a) and switching speed middle point and equivalent parasitic capacitance rates (b) as a function of the $k$ factor for TGD and CGD configurations.

### 3.2.1 Electrical Transient Simulations

To validate the theoretical approach, electrical simulations are made with *LTSpice* software with an *Infineon* CoolMOS Transistor Spice model SPD02N50C3 (500 V, 1.8 A). Two pair of series-connected transistors are used to form an inverter leg. The main parameter values used in the simulations are: bus voltage of 200 V, a load current of 3 A. A value of around 80 pF has been used for the parasitic capacitance $C_{ps}$, and therefore the $k\ factor$ is close to 1. No external gate resistances are used in the simulations.

Fig. 3.43 shows the simulation results of the switching speed of both gate driver architectures. As can be seen, when the TGD is used, the series-connected power devices achieve a $dV/dt$ (in relation to the middle point) of 24.3 V/ns. On the other hand, with the CGD, a faster switching speed is achieved, with a $dV/dt$ of 36.1 V/ns. Using Eqs. (3.13) and (3.15), and taking the same parameter values used in the simulations, switching speeds of

33.3 V/ns and 21.8 V/ns are calculated for the TGD and CGD, respectively. The switching speed is measured when the $V_{ds}$ voltage of each transistor is around 50 V, *i.e.*, when the middle point voltage is around 100 V. Note that the discrepancy of the simulated and the calculated results is very small.

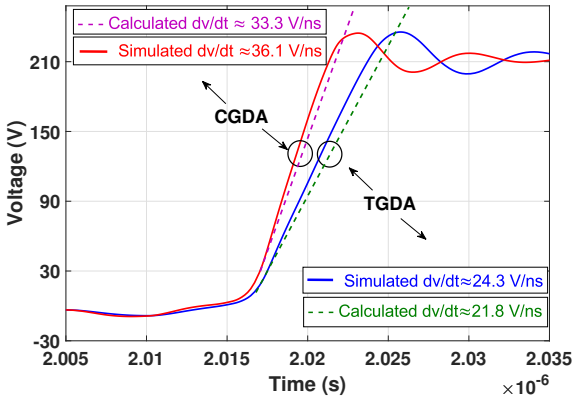


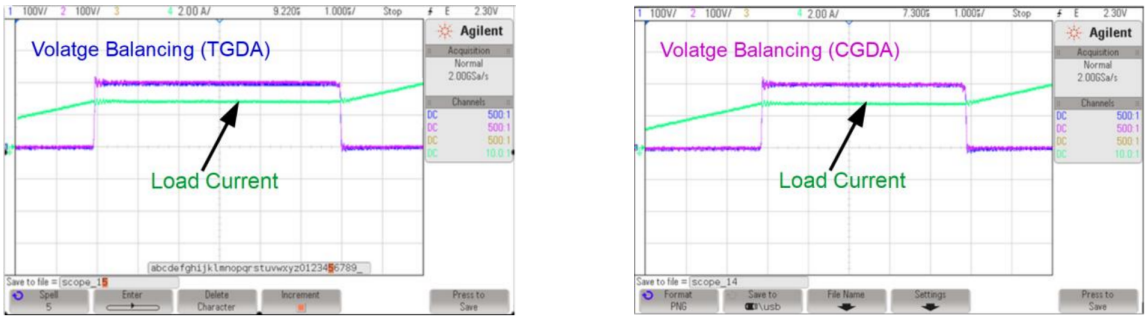

**Fig. 3.43.** Switching speed middle point as function of the gate driver architecture; simulated and calculated results.

In the experiments, identical transistors and identical gate driver power supplies with equal nominal parasitic capacitances have been used. As explained, the $k\ factor$ depends on the power device and of the gate driver DC/DC converter that are used. To ensure a general analysis, the devices are chosen to achieve a $k\ factor$ close to 1. In this case, for the same power devices used in this work (same $C_s$), if another DC/DC converter with lower parasitic capacitance ($C_{ps}$) is used, the $k\ factor$ will be greater than 1, and then the gain on the switching speed will be lower than that presented in this paper. On the other hand, for the same DC/DC converter (same $C_{ps}$), if other devices with lower intrinsic parasitic capacitance ($C_s$) are used, the $k\ factor$ will be less than 1, and then the gain on the switching speed will be greater than that presented in this work.

### 3.2.2 Experimental validations

To validate the theoretical approach developed in this chapter, the TGD and CGD prototypes have been built. In the experiments, all gate resistors are reduced to zero to maximize the switching speed of the series-connected power devices. To compare the switching speed of the devices, it is necessary to ensure that the series-connected devices are switched under the same conditions (voltage sharing performance and load current) for both gate driver architectures. Therefore, in the experiment an adaptative open loop external delay control circuit is implemented to achieve a perfect voltage sharing between the devices in the stack, i.e., the voltages across the devices are perfectly balanced for both gate driver architectures as shown in Fig. 3.44.

A DC bus of 200 V is used for practical and security reasons since no protection method (clamping techniques) or snubber circuits are used. This kind of circuit would drastically impact the switching speed of the series-connected devices, which can hinder the experimental analyses performed in this section.

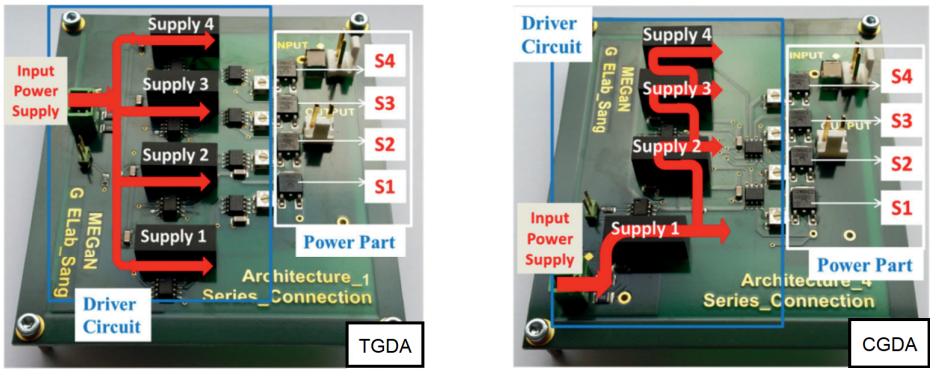



**(a)** **(b)**

**Fig. 3.44.** Experimental Vds voltage balancing waveforms for the TGD (a) and CGD (b) configurations.

The TGD and the CGD prototypes [70] are shown n Fig. 3.45. Each inverter leg is built with the classical Si CoolMOS devices SPD02N50C3 (500 V, 1.8 A) where two devices are connected in series. The IR2184 gate drivers are powered by TMA1515 DC/DC converters; four identical TMA1515 power supplies are used for both architectures. In the transistor datasheet, the nominal value for the output capacitance $C_{OSS}$ of the transistor is about 80 pF. OPTO HPCL 2211 optocouplers are used for the control signal isolation. This optocoupler introduces an ultra-low parasitic capacitance of around 0.5 pF. The TMA1515 power supply is characterized and the value of its primary-secondary parasitic capacitance is estimated at 86 pF [84]. Commercial power supplies with a smaller parasitic capacitance can be found, such as Murata Power Solutions MGJ6 series with 15 pF parasitic capacitance. However, the improvement on the switching speed can still be observed. For example, if a gate driver power supply with a parasitic capacitance of 15 pF is used, when a drain-source voltage of 100 V is achieved, ($C_{OSS}$ = 10 pF), according to the Fig. 3.41, it will give a $k\ factor$ of around 0.66, and it has an important impact on the switching speed. It is important to note that the $C_{OSS}$ of the power devices will be decreased almost 8 times when $V_{ds}$ goes from 50 V to the half of voltage of DC bus used in our experiments (100 V); the $k\ factor$ is reduced to 0.1 due to this phenomenon as shown in Fig. 3.42(b). Furthermore, fast wide band gap devices with small intrinsic parasitic capacitances can be used, and in this case, a small $k\ factor$ can be achieved.

The gate driver signal isolation units are all implemented considering the classical architecture, where the control signals are applied to the gate driver through four independent pathways. The experimental set-up and the testing conditions (load current, driving voltage, driving resistances, etc.) are kept identical for the two cases.



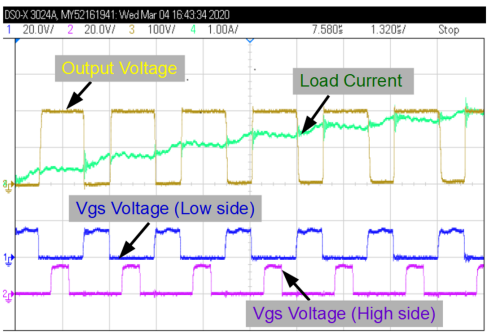

**(a)** **(b)**

**Fig. 3.45.** Traditional (a) and Cascaded (b) gate driver architectures [70].

The CGD prototype shown in Fig. 3.45(b), has been developed with the same devices and same characteristics as the TGD one. In relation to the PCB layout, just the connections between the power supplies have been modified when compared to the TGD PCB layout. In this case, it can be considered that the parasitic elements introduced by the PCB layout remain the same on both gate driver architectures.

To analyse the switching behaviour as function of the load current, a same pulse train is applied for both architectures as shown in Fig. 3.46(a). The load current has strong impacts on the dynamic behaviour of the series-connected devices since the load and the gate currents charge/discharge the capacitors of the system that dictate the dynamic behaviour of the series-connected devices. This phenomenon, i.e., the dependency of dynamic behaviour of series-connected devices on $dV/dt$ (IL) has been experimentally analysed in [12]. In the present experiments, the pulse train changes the load current from 0.285 A to 2 A with a current step of around 0.285A. The measured $dv/dt$ (max) is presented in Fig. 3.46(b). For light loads, i.e., load currents between 0.285A and 0.570A, are observed small gains on the $dv/dt$ (between 12.3% and 18.1%). In this case, as demonstrated in [82], the $dV/dt$ is limited by the power loop, where all load current is used to charge/discharge output capacitances. On the other hand, at heavy load, e.g., load current equal to 2A, a gain on the $dV/dt$ around of 41.2% can be achieved.

These experimental results confirm the analysis expecting that the gate driver supply architecture induced a significant switching speed evolution and it can be related to the global inverter leg middle point to ground parasitic capacitance. Fig. 3.47 summarizes the comparisons between the TGD and the CGD in terms of the switching speed of power devices in series connection for a load current of 3A. As can be seen, the CGD architecture can generate an improvement on the switching speed; it is boosted from 20.1 V/ns to 28.1 V/ns when a 3A load is used. It means a gain of 40% on the $dV/dt$. According to Eqs. (3.13) and (3.15), this result is consistent with the calculated result, which the switching speed is boosted from 21.8 V/ns to 33.3 V/ns, representing a gain of 52% on the switching




**(a)**

| Load Current | $dV/dt(TGDA)$ | $dV/dt(CGDA)$ | Gain |
|---|---|---|---|
| 0.285 A | 2.68 V/ns | 3.83 V/ns | 12.3 % |
| 0.570 A | 4.56 V/ns | 5.38 V/ns | 18.1 % |
| 0.855 A | 5.40 V/ns | 7.16 V/ns | 32.6 % |
| 1.140 A | 7.23 V/ns | 10.05 V/ns | 39.1 % |
| 1.425 A | 8.85 V/ns | 12.17 V/ns | 37.5 % |
| 1.710 A | 10.23 V/ns | 14.08 V/ns | 40.8 % |
| 2.000 A | 12.14 V/ns | 16.03 V/ns | 41.2 % |

**(b)**

**Fig. 3.46.** Experimental pulse train waveforms (a) and measured $dv/dt$ for TGD and CGD configurations.

speed. Similarly, the simulation results show a gain of 48% on the $dV/dt$.

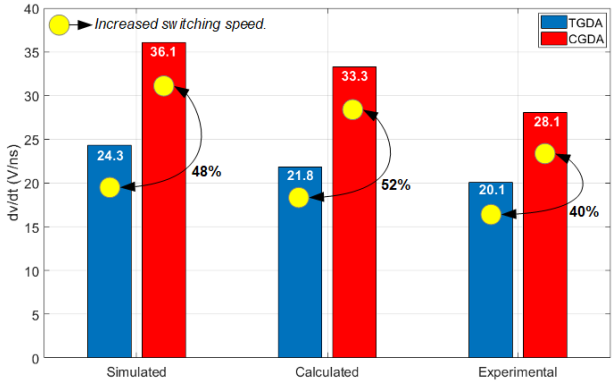



**Fig. 3.47.** Calculated, simulated and experimental maximum $dV/dt$ as a function of the gate driver architectures for $k$ $factor$ equal to 1, with a load current of 3A.

Evidently, the experimental results present a slight numerical difference caused by parasitic elements and practical factors that are not taken into account by the proposed model or by the simulations. Different characteristics between the MOSFETs (different $C_{ds}$, $C_{gd}$, and $C_{gs}$), different characteristics between the drivers (different parasitic capacitances), the parasitic capacitances introduced by the voltage probes, the small parasitic capacitance introduced by the signal isolation, etc. are the most important factors that contribute to discrepancy shown in Fig. 3.47. However, these results validate the main idea proposed in this work, *i.e.*, the $dV/dt$ on the middle point of switching cells can be boosted by cascading the gate drive power supplies as evidenced by the simulation, calculated, and experimental results.

For optimal design, the power rating of the DC/DC converters has to be taken into account. The advantages offered by the cascaded gate drive supply configuration must be mitigated by the increased complexity, volume and the additional power consumption due to the cascaded power supplies. The cascaded gate drive power supplies must be designed

carefully since their power ratings are changing from one to another, specially for the first gate drive power supply, which must be designed to supply all the other drive circuits. In terms of cost and volume, the CGD has more volume than the TGD. As analysed in [81], the CGD has 2.5 times more volume than the TGD, which also means that the CGD increases the cost compared to the TGD. However, the CGD provides less switching losses, and consequently the heatsink in the CGD will be smaller than the heatsink in the TGD. In this case, the volume and the cost will be decreased, when it is compared to the TGD. A deeper analysis about optimal design in terms of power rating, volume, efficiency, and parasitic currents has been addressed in [81].

## 3.3 Impact of the Gate Driver Configuration on Voltage Balancing: A Brief Discussion

As demonstrated in the last sections, the new gate driver configurations can reduce the conducted CM current in the control side, and increase the switching speed of the series-connected devices. To ensure that these benefits are not mitigated by the impact of the gate driver configurations on voltage balancing, a brief analysis is done in this section to investigate the impact of the gate driver configuration on the voltage balancing.

At first glance, it is normal to think that traditional gate driver architectures (TGD) are symmetrical and the new gate driver configurations can increase voltage balancing problems. However, one of the most important factors contributing to unequal dynamic voltage sharing among series-connected devices is the parasitic capacitances from gates to ground in the traditional gate drive power supply configurations [9, 12].

Consider the simplified circuit for two series-connected devices in Fig. 3.48(a), where $C_s$, expressed by Eq. 3.10, is the association between the intrinsic MOSFET capacitances and the decoupling capacitance of the buffer for negative voltage ($C_m$), and $C_{ps}$ is the parasitic capacitance introduced by the gate driver power supply. Note that, to simplify the equations and facilitate the analyses, only the parasitic capacitances ($C_s$, $C_{ps}$ and $C_{gnd}$) are considered in Fig. 3.48(a). All gate drive power supplies and all power devices are considered identical.

Redrawing the circuit shown in Fig. 3.48(a), a more simplified circuit can be achieved as shown in Fig. 3.48(b), where $C_{ab}$ and $C_{bc}$ are the equivalent parasitic capacitances between the points $a-b$ and $b-c$, respectively.

To prove that the TGD configuration causes unbalance in the voltages across series-connected devices, a simple proof by contradiction can be demonstrated. Consider the current distribution shown in Fig. 3.48(b), and the following equation:

$$I_{ab} + I_{cn2} = I_{bc} + I_{cn1} \tag{3.16}$$

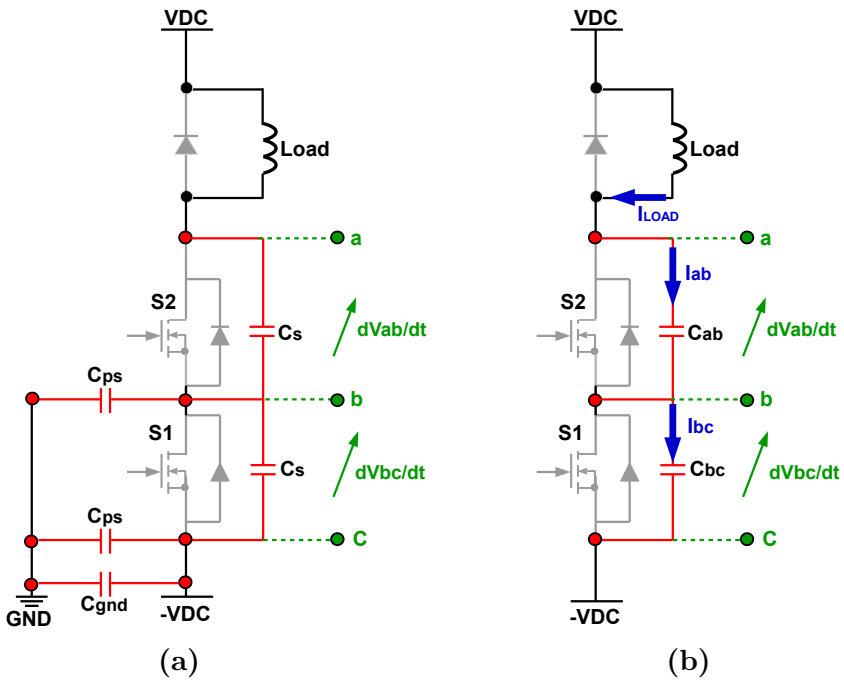



**Fig. 3.48.** Electrical circuit of two SiC-MOSFETs connected in series (a) and equivalent electrical circuit (b).

Where $I_{cni}$ is the channel current of device $i$.

If we consider that the $V_{ds}$ voltages across the devices are perfectly balanced, the following sentence can be applied:

- The devices experiment equal drain-to-source $dv_{ds}/dt$, which implies that $I_{cn2} = I_{cn1}$ since the devices are considered identical.

Therefore, it can be considered that $I_{ab} = I_{bc}$, and the following equation can be written:

$$C_{ab}\frac{dVab}{dt} = C_{bc}\frac{dVbc}{dt} \tag{3.17}$$

Where $C_{ab} = C_s$, and $C_{bc}$ is expressed by Eq. (3.18).

$$C_{bc} = C_s + \frac{(C_{ps} + C_{gnd})C_{ps}}{2C_{ps} + C_{gnd}} \tag{3.18}$$

Replacing $C_{ab}$ and $C_{bc}$ in Eq.(3.17), the switching speed relation between the two series-connected devices is achieved:

$$(C_s)\frac{dVab}{dt} = \left(C_s + \frac{(C_{ps} + C_{gnd})C_{ps}}{2C_{ps} + C_{gnd}}\right)\frac{dVbc}{dt} \tag{3.19}$$

As can be seen, the switching speed behaviour $dVs1/dt$ is different of the switching speed behaviour $dVs2/dt$, i.e., $dVs1/dt > dVs2/dt$. Therefore, according to the Eq. 3.19, in TGDA configuration, the power device $S_1$ switches faster than the power device $S_2$ introducing voltage balancing problems. On the other hand, the proposed gate drive configurations analysed in this work can reduce the unequal dynamic voltage sharing among series-connected devices as demonstrated in the next section.

### 3.3.1 Experimental Results

To investigate the impacts of the gate drive configurations on voltage balancing, a switching cell prototype with four C2 silicon carbide power MOSFETs C2M0025120D (1200V, 90A) connected in series for the low side and one STMicroelectronics schottky silicon carbide diode STPSC40H12CWL for the high side is developed. The DC-DC converter implemented for each gate driver used in the experiment is a Murata MGJ6D242005SC with an isolation voltage and parasitic capacitance of 5.7 kVDC and 15 pF, respectively. Optical fibers are used to achieve high signal isolation. A bus voltage of 1 kV and a load current of 40 A are used to investigate the gate driver configurations. As no heatsink is attached to the devices, the experiments are performed in pulse mode. The impacts caused on the voltage distribution by the proposed architectures are depicted in Figs. 3.49-3.54.

As can be seen in Fig. 3.49, if the highest voltage is taken as a comparison parameter, the 1MGD configuration has a better voltage sharing performance than TGD. The highest voltage in the TGD is approximately 400 V, while in the 1MGD it is approximately 350 V.

The configuration 2MGD has a similar behaviour to the TDG one as shown in Fig. 3.50. The upper MOSFET (blue curve) is submitted to a $V_{ds}$ voltage of around 400 V, which is far from the ideal value (250 V).

According to the Fig. 3.51, the configuration 3MGD also has a better voltage distribution than TGD, where the highest voltage in the 3MGD is approximately 380 V. Similar results are presented in the 4MGD, where the highest voltage in the 4MGD is approximately 390 V as shown in Fig. 3.52.

The configurations 5MGD and 6MGD present the best results. The highest voltages in these configurations are approximately 340 and 320 V, respectively. In addition to the better performance, in the new gate driver configurations, the upper MOSFET (blue curve) is less stressed.

As can be seen, the proposed gate drive configurations can reduce the voltage unbalancing across the series-connected devices or have similar performance to TGD in terms of voltage balancing. It means that the benefits provided by the new configurations (CM current reduction and switching speed) are not mitigated by possible voltage balancing problems

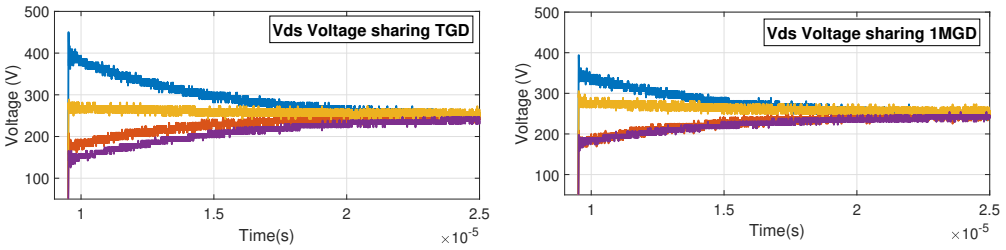



**Fig. 3.49.** Experimental voltage balancing waveforms for (a) TGD and (b) 1MGD configurations.

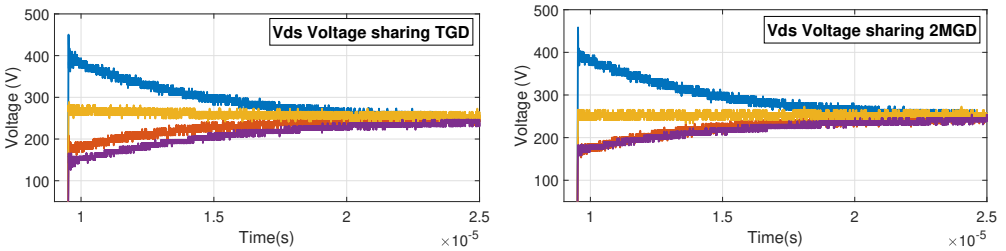



**Fig. 3.50.** Experimental voltage balancing waveforms for (a) TGD and (b) 2MGD configurations.

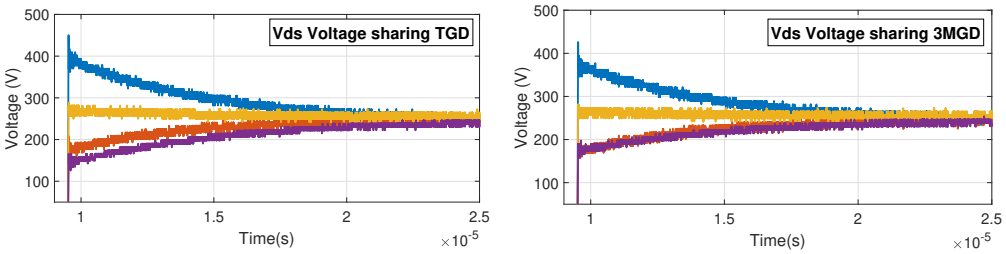



**Fig. 3.51.** Experimental voltage balancing waveforms for (a) TGD and (b) 3MGD configurations.

caused by the modification on the gate drive power supply connections.

## 3.4 Conclusion

In this chapter, six new gate drive power supply configurations are proposed to reduce the conducted EMI common mode currents. The most notable EMI reductions varies between 9-21dB, depending on frequency range and gate driver architecture. Furthermore, a cascaded gate driver configuration is presented as an effective technique to improve the switching speed of the series-connected power devices. Compared to the classical gate driver

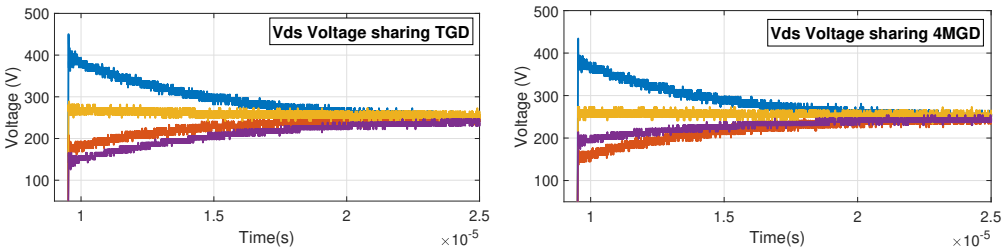



**Fig. 3.52.** Experimental voltage balancing waveforms for (a) TGD and (b) 4MGD configurations.

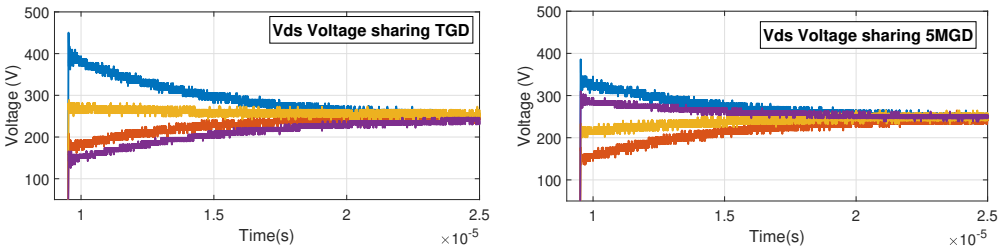



**Fig. 3.53.** Experimental voltage balancing waveforms for (a) TGD and (b) 5MGD configurations.

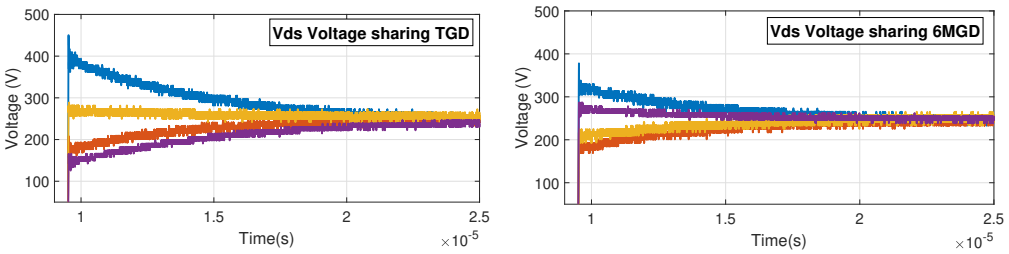



**Fig. 3.54.** Experimental voltage balancing waveforms for (a) TGD and (b) 6MGD configurations.

configuration, the cascaded one could provide an increase on the switching speed of 12-41%, depending on the load current. All the theoretical approaches were validated by simulation and experimental results, which confirm the interest of the proposed gate drivers on the EMI reduction and switching speed of power devices.

The chapter does not focus on voltage balancing problems. However, the impact of the proposed gate drivers on the voltage sharing performance is discussed in the end of the chapter. In general, the new gate drive power supply configurations can also reduce voltage balancing problems.

However, for optimal design the power rating of the DC/DC converters has to be taken into account. The advantages offered by the new gate drive power supply configurations must be mitigated by the increased complexity, volume and the additional power consumption due to the cascaded power supplies. The proposed gate drivers must be designed carefully since their power ratings are changing from one to another, specially for the first gate drive power supply, which must be designed to supply other drive circuits. A deeper analysis about optimal design in terms of power rating, volume, efficiency, and parasitic currents has been addressed in [81].

# Chapter 4
# A Novel Multi-Step Packaging Concept for Series-Connected Devices

In this chapter a Novel Multi-Step Packaging (MSP) concept for series-connected SiC-MOSFETs is analysed. The proposed package geometry considers optimal dielectric isolation for each device leading to a multi-step geometry. It has a significant impact on the parasitic capacitances introduced by the packaging structure that are responsible for voltage unbalances. The concept is introduced and analysed thanks to equivalent models and time domain simulations. Then, experimental results confirm that the proposed packaging concept is better than the traditional one in terms of voltage balancing. Furthermore, the proposed concept can improve the switching speed of the switching cell as will be explained and demonstrated in this chapter.

## 4.1 Impact of Power Module Parasitic Capacitances on Voltage Balancing

Considering high $dv/dt$ switching transients, intrinsic device parasitic and external parasitic capacitances are crucial and require careful optimization to use SiC-MOSFETs at their full potential. The most important parasitic capacitances contributing to unequal dynamic voltage sharing among series-connected devices are the ones located between each potential electrode formed by interconnection of two power devices and the ground, i.e., the parasitic capacitances introduced by the gate driver power supply ($C_{ps}$) as described in [9, 51, 52], and the drain-attached copper trace to ground parasitic capacitances ($C_{pac}$) introduced by the packaging [10, 86].

A cross section of a simplified planar package and its main elements are shown in Fig. 4.1.

The function of each element in Fig. 4.1 is briefly described as follows:

- 1) **Power semiconductors** are the most important elements in power modules, converting power from the source to the load by performing electrical ON/OFF switching. In this work, **SiC-MOSFET devices** are used to perform experimental analyses.
- 2) The **insulating substrate** provides electrical isolation and dissipation of heat generated from the devices [87]. Layers attached to the insulating substrate provide electrical connection between dies. Direct-bonded copper (DBC) substrates are used

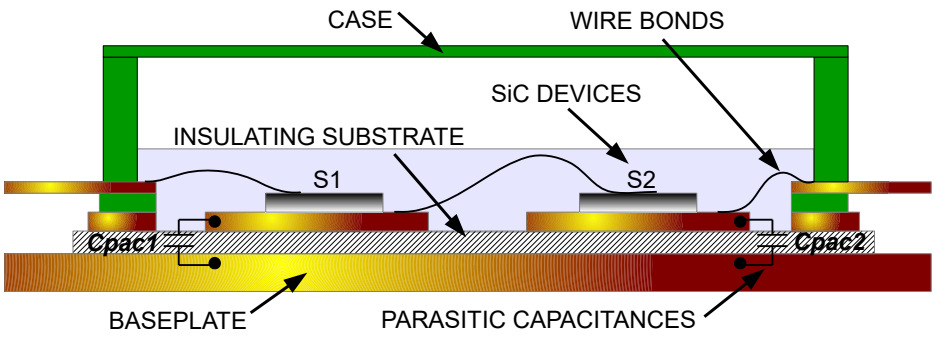



**Fig. 4.1.** Cross-section of a simplified standard 2D planar package with two dies connected in series.

for insulating substrate in conventional power modules due to their excellent properties that not only satisfy the electrical and thermal requirements but also the mechanical reliability. Popular materials for the ceramic layer sandwiched between two copper layers are $Al_2O_3$, $AlN$, $Si_2N_4$, and $BeO$ [88].

- 3) The function of **the base plate** is to provide mechanical support for the insulating substrate, and absorbing heat from the insulating substrate and transmit it to the cooling system.
- 4) The main role of the **wire bond** is to make electrical connections between the power semiconductors, conductor traces, and input/output terminals of the module.
- 5) The case protects from mechanical shocks and environmental effects.

It is important a proper design of the packaging/layout to take advantage of the full potential of the attached dies in terms of electrical performance, thermal management and robustness. However, this chapter is focused on the analysis of the impact of the parasitic capacitance $C_{pac}$ on the voltage balancing behaviour and voltage switching speed of series-connected SiC-MOSFETs. In the end of this chapter, a simplified thermal analysis is proposed.

### 4.1.1 Theoretical Analyses

In terms of voltage balancing and switching speed, the drain attached copper trace to ground parasitic capacitances ($C_{pac}$) introduced by the packaging, is critical. In Fig. 4.1, two series-connected devices are placed in a traditional planar package. Therefore, two drain attached copper trace to ground parasitic capacitances ($C_{pac1}$ and $C_{pac2}$) are introduced. In order to focus on the impact of the packaging on the dynamic voltage sharing without having to consider the impact of the gate drivers and theirs supplies, their influence will be neglected in the following analysis.

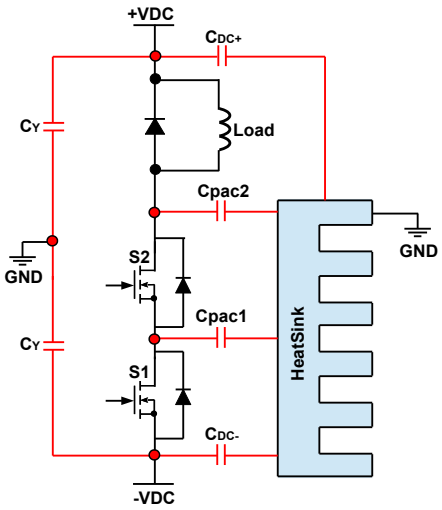



**Fig. 4.2.** Equivalent electrical circuit of two SiC-MOSFETs connected in series in a 2D planar package.

To analyse the influence of the parasitic capacitances $C_{pac}$ on the dynamic voltage unbalancing and on the switching speed behaviour of the switching cell, let's consider two SiC-MOSFETs connected in series (Fig. 4.2). $C_{pac1}$ and $C_{pac2}$ are the drain to ground (heatsink) parasitic capacitances associated to devices S1 and S2, respectively. $C_{DC+}$ and $C_{DC-}$ are the parasitic capacitances from the DC bus to the ground. During the switching period, large current spikes flow from the floating potentials nodes to the ground trough the heatsink. These currents cause EMI issues which limit the switching speed of the circuit [89,90]. In [91], it is to use Y-capacitors ($C_Y$) to suppress this EMI. $C_Y$ are usually placed between + VDC and GND, and - VDC and GND.

In traditional 2D planar packaging (Fig. 4.1), capacitors $C_{pac1}$ and $C_{pac2}$ have the same values (if copper traces are identical). However, the $dv/dt$ applied to each of them is different with respect to the position of the device in the stack. As a result, each parasitic capacitor carries a parasitic current that is getting greater and greater with the device number in the stack (starting from the bottom). As it will be underlined, these currents split, produce a voltage unbalance that needs to be mitigated. The capacitors $C_{pac}$ that generate these currents can be estimated based on the planar capacitance formula (4.1).

$$C_{pac} = \epsilon \frac{A}{d} \tag{4.1}$$

Where $\epsilon$ is the absolute permittivity of the isolated substrate, $A$ is the area of the copper trace on which the SiC device is attached, and $d$ is the distance between the copper plate and the baseplate.

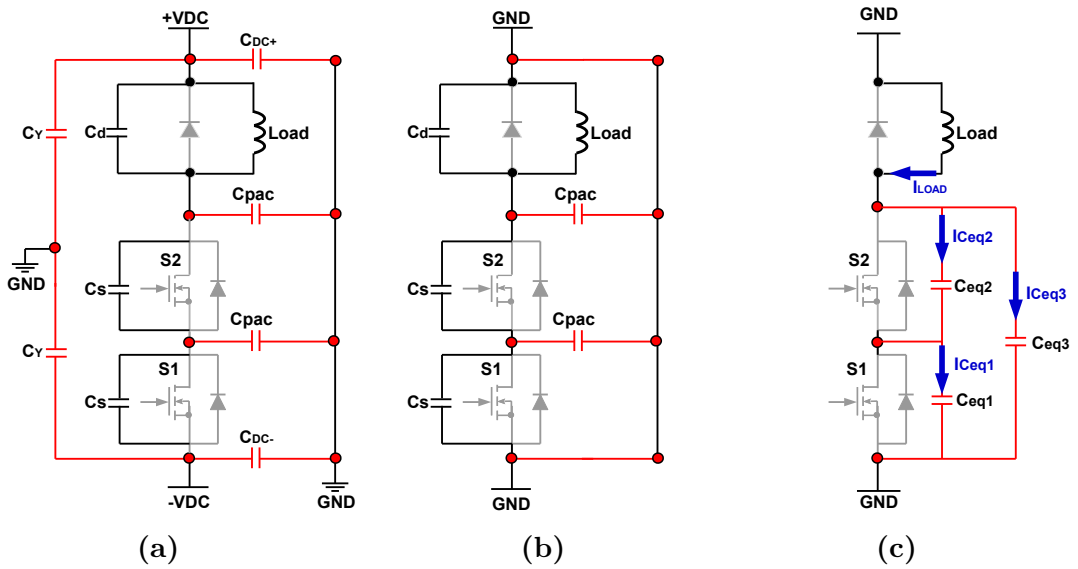



**Fig. 4.3.** Electrical circuit of two SiC-MOSFETs connected in series in a 2D planar package (a), high frequency circuit (b) and simplified electrical scheme (c).

### Analytical Analysis For Two Series-Connected SiC-MOSFETs

Considering that all SiC-MOSFETs in Fig. 4.2 are identical, and $C_{pac1} = C_{pac2} = C_{pac}$, Fig. 4.2 can be redrawn as shown in Fig. 4.3(a), where $C_d$ is the intrinsic parasitic capacitance of the diode, and $C_s$ is the equivalent parasitic capacitance of the SiC-MOSFET expressed by equation (4.2). In the following analyses, it is supposed that the series-connected SiC-MOSFETs are turning-off.

$$C_s = C_{gd} + C_{ds} \tag{4.2}$$

As shown in Fig. 4.3(b), a high frequency equivalent circuit can be simplified by short-circuiting the DC-bus terminals and $C_Y$ capacitors. Redrawing Fig. 4.3(b), a simplified high frequency equivalent scheme can be achieved as shown in Fig. 4.3(c), where $C_{eq1}$, $C_{eq2}$ and $C_{eq3}$ are equivalent drain-to-source parasitic capacitances of the devices expressed by Eqs. (4.3), (4.4) and (4.5), respectively.

$$C_{eq1} = C_s + C_{pac} \tag{4.3}$$

$$C_{eq2} = C_s \tag{4.4}$$

$$C_{eq3} = C_d + C_{pac} \tag{4.5}$$

Analysing Fig. 4.3(c), the currents that circulate through the equivalent parasitic capacitances $C_{eq1}$ and $C_{eq2}$ can be expressed by the Eqs. (4.6) and (4.7).

$$I_{Ceq1} = C_{eq1}\frac{dV_{ds1}}{dt} \tag{4.6}$$

$$I_{Ceq2} = C_{eq2}\frac{dV_{ds2}}{dt} \tag{4.7}$$

To prove that the parasitic capacitances introduced by the traditional package cause voltage unbalance across series-connected SiC-MOSFETs, a simple proof by contradiction can be presented. Consider the current distribution shown in Fig. 4.3(c), and the following equation:

$$I_{S1} + I_{Ceq1} = I_{S2} + I_{Ceq2} \tag{4.8}$$

Where $I_{Si}$ is the current that circulates through device $Si$.

If we consider that the $V_{ds}$ voltages across the devices are perfectly balanced. Therefore the following sentence can be applied:

- The currents $I_{S1}$ and $I_{S2}$ are identical since it is considered the devices are identical.

Applying this condition to Eq. (4.8), it becomes:

$$I_{Ceq1} = I_{Ceq2} = C_{eq1}\frac{dV_{ds}}{dt} = C_{eq2}\frac{dV_{ds}}{dt} \tag{4.9}$$

According to Eq. (4.9), the voltages across the series-connected devices are perfectly balanced (same $\frac{dV_{ds}}{dt}$), if and only if, $C_{eq1} = C_{eq2}$. However, according to the Eqs. (4.3) and (4.4), these parasitic capacitances are different. Note that, according to these equations, the only way to balance the voltages across the devices, is to reduce $C_{pac}$ to zero. Therefore, the power switches S1 and S2 do not have the same dynamic behaviour since their equivalent parasitic capacitances between drain and source are not equal. Note that, a hypothetical case was supposed in this analysis, i.e., even if the gate driver are perfect and there is no mismatch between the devices tolerance parameters, the parasitic capacitances introduced by the packaging/layout will increase voltage balancing problems.

Still assuming this hypothetical case, to ensure that the two series-connected devices in Fig. 4.3 have the same dynamic behaviour, $C_{eq1}$ should be equal to $C_{eq2}$. In brief, to ensure the dynamic voltage balancing, the drain-to-source equivalent capacitance of each device, in series connections, has to be identical. Otherwise, the packaging/layout can unbalance the voltages across the devices in the stack.

### Simulation Results For Two Series-Connected SiC-MOSFETs

Fig. 4.4 shows the LTSpice simulation results of the voltage sharing between two series-connected C2M0160120 SiC-MOSFET (1200 V, 19 A). The simulations are done in the hypothetical case where the gate drivers are perfect, no time delay between the gate signals and the power devices are identical. In other words, only the packaging/layout (capacitive elements) is taken into account. The series-connected devices are switched under a total blocking voltage of 1 kV and a load current of 20 A.

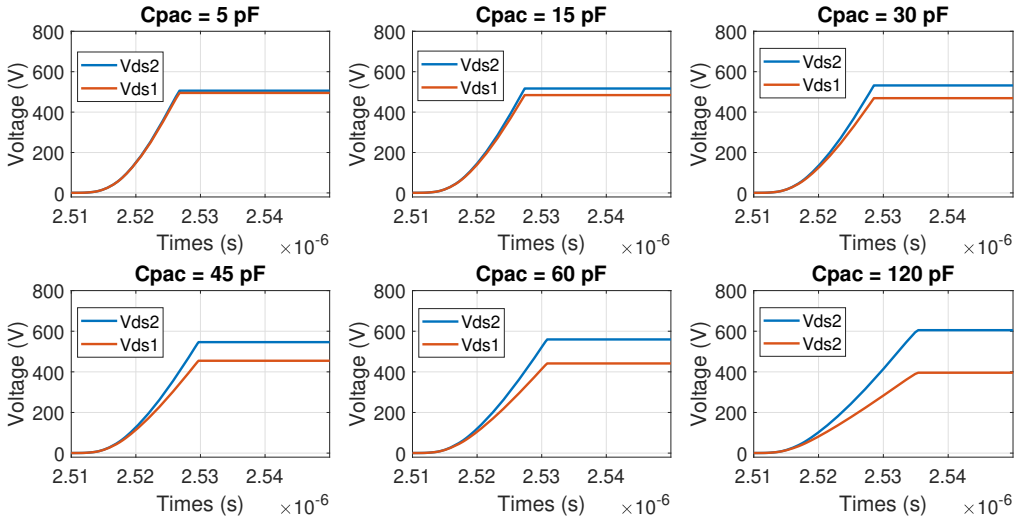



**Fig. 4.4.** Simulation results: voltage sharing between two series-connected devices as a function of $C_{pac}$.

As can be seen in Fig. 4.4, the voltage unbalancing increases as a function of the parasitic capacitance $C_{pac}$. For an ultra-low parasitic capacitance ($C_{pac} = 5$ pF), the voltage sharing across the devices is acceptable. On the other hand, for $C_{pac} = 120$ pF (practical value), the difference between the $V_{ds}$ voltages is approximately 200 $V$. Note that device S2 has the fastest switching speed, which is expected since, according to Eq. 4.4, S2 has the smallest drain-to-source equivalent parasitic capacitance. Another characteristic of classical packages/layout is their impact on the switching speed of the devices. Fig. 4.5 shows the simulation results of the $dv/dt$ of the switching cell as a function of the parasitic capacitance $C_{pac}$. As can be seen, the $dv/dt$ on the middle point is drastically reduced when $C_{pac}$ increases from 5 pF to 120 pF. As will be explained in this chapter, modify the parasitic capacitance configuration of the package/layout not only reduces the voltage unbalancing, but can also improve the switching speed of the devices.

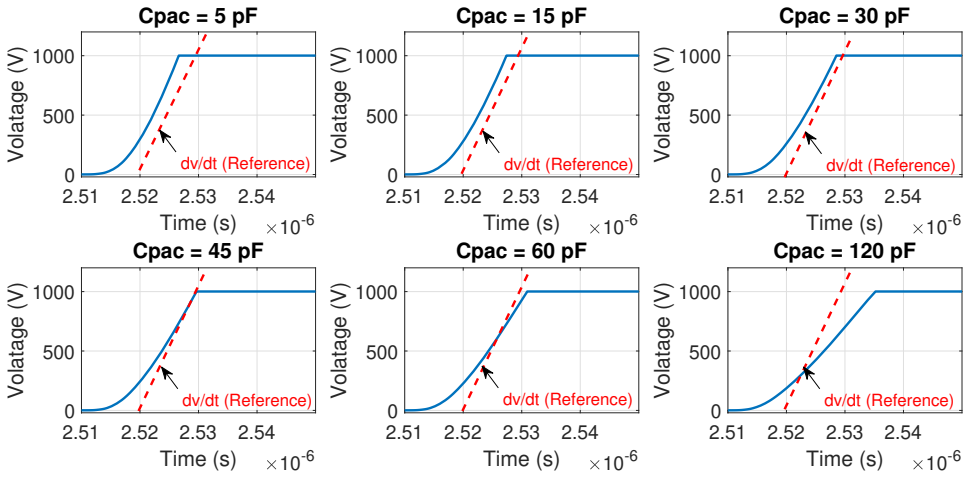



**Fig. 4.5.** Simulation results: middle point switching speed as a function of $C_{pac}$.

### Analytical Analysis For Four Series-Connected SiC-MOSFETs.

Up to now, analytical analyses have been done for only two series-connected devices to facilitate reading and understanding the concepts. However, as shown in Fig. 4.6, the models proposed in Fig. 4.3 can be extrapolated for N devices connected in series. The series-connected switching cell can be represented by one equivalent capacitor connected in parallel with each device, and another equivalent capacitor connected between the switching cell middle point and the ground. However, the more devices stacked, the more complex the analysis will be. Therefore, to make a more in-depth analysis without making reading difficult, four series-connected devices will be analysed in this chapter. Repeating the same investigation done for two devices in the stack, the equivalent parasitic capacitances for four devices connected in series and the switching cell middle point $dv/dt$ can be written as shown in Eqs. (4.10)-(4.14).

$$C_{eq1} = (C_s + C_{pac}).\frac{C_s^3 + 9.C_s^2.C_{pac} + 6.C_s.C_{pac}^2 + C_{pac}^3}{C_s^3 + 6.C_s^2.C_{pac} + 5.C_s.C_{pac}^2 + C_{pac}^3} \tag{4.10}$$

$$C_{eq2} = \frac{C_s^3 + 9.C_s^2.C_{pac} + 6.C_s.C_{pac}^2 + C_{pac}^3}{C_s^2 + 6.C_s.C_{pac} + +2.C_{pac}^2} \tag{4.11}$$

$$C_{eq3} = (C_s + C_{pac}).\frac{C_s^3 + 9.C_s^2.C_{pac} + 6.C_s.C_{pac}^2 + C_{pac}^3}{C_s^3 + 8.C_s^2.C_{pac} + 8.C_s.C_{pac}^2 + 2.C_{pac}^3} \tag{4.12}$$

$$C_{eq4} = (C_s + C_{pac}).\frac{C_s^3 + 9.C_s^2.C_{pac} + 6.C_s.C_{pac}^2 + C_{pac}^3}{C_s^3 + 9.C_s^2.C_{pac} + 9.C_s.C_{pac}^2 + 2.C_{pac}^3} \tag{4.13}$$

$$C_{eq5} = C_d \tag{4.14}$$

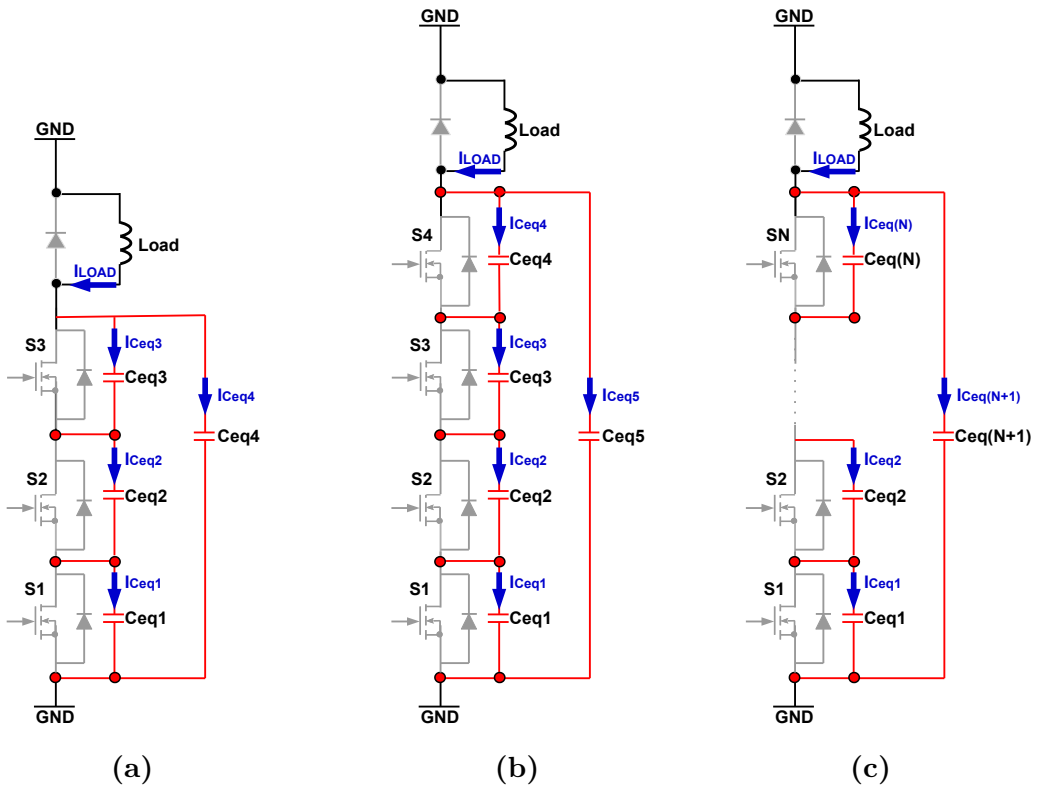



**Fig. 4.6.** Equivalent electrical circuits for 3(a), 4(b), and N-series-connected devices(c).

Fig. 4.7(a) shows the behaviour of each equivalent parasitic capacitance as a function of $C_{pac}$ for $C_s = 100\ pF$. As can be seen, the device at the top of the stack (S4) has the smallest equivalent capacitance ($C_{eq4}$) for all $C_{pac}$ values. On the other hand, the first device in the stack (S1) has the greatest equivalent capacitance ($C_{eq1}$). Note that the higher the device is positioned on the stack, the lower its drain-to-source equivalent capacitance. Therefore, the switching speed behaviour of each device is also a function of its position in the stack as shown in Fig. 4.7(b). In other words, the device at the top of the stack (S4) has the faster switching speed while S1 (the first one in the stack) has the slowest $dv/dt$. This phenomenon has been observed in experimental results presented in the literature.

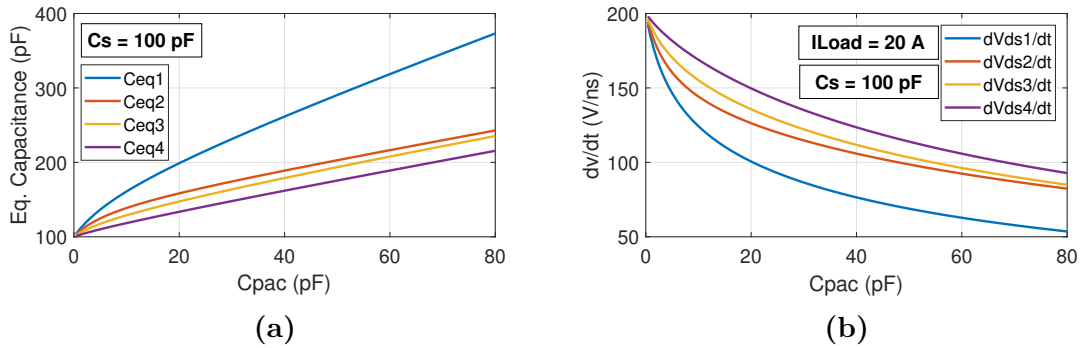



**Fig. 4.7.** Equivalent parasitic capacitances (a) and middle point $dv/dt$ (b) as a function of $C_{pac}$.

It is clear that the parasitic capacitance configuration in classical packaging/layout has strong impacts on the voltage balancing in series-connected SiC-MOSFETs. To mitigate its negative influence, two effective ways can be considered: 1) reducing the parasitic capacitance $C_{pac}$ by optimizing the packaging/layout, and 2) changing the parasitic capacitance configuration of switching cells as will be explained in the next sections.

## 4.2 Multi-Step Packaging/Layout Concept: 1st Proposition

According to the previous section, the classical packaging increases voltage balancing problems since it generates unequal drain-to-source equivalent parasitic capacitances among the series connected devices, which carry a parasitic current that is getting greater and greater with the device number in the stack (starting from the bottom). In other words, to improve voltage balancing, the equivalent parasitic capacitances $C_{eqi}$ shown in Fig. 4.6 have to be identical, allowing the series-connected devices have the same dynamic switching behaviours ($dv/dt$).

To ensure equal drain-to-source equivalent capacitance distribution among the series-connected devices, a Multi-Step Packaging (MSP) concept, shown in Fig. 4.8, is analysed in this chapter. The front and backside die-attachments are implemented in a similar way that is done in the traditional 2D planar package. As can be seen, in the MSP concept, the parasitic capacitances $C_{pac}$ are connected to the drains of the series-connected devices.

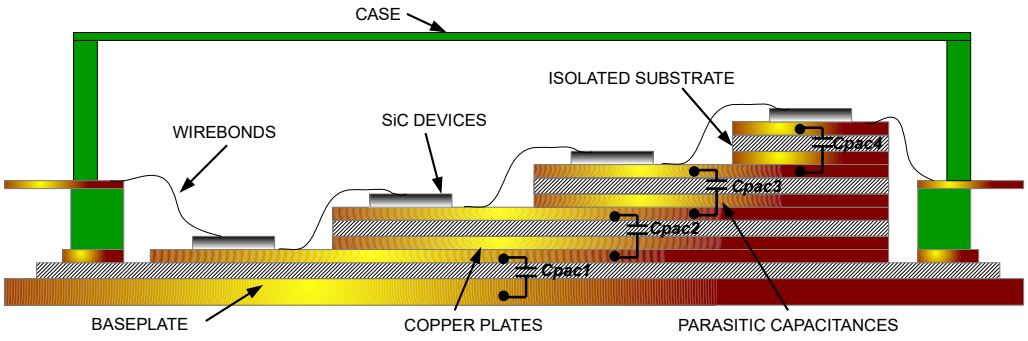



**Fig. 4.8.** Multi-Step Package concept for four series-connected SiC-MOSFETs.

The electrical circuit of the MSP is shown in Fig. 4.9(a), where it is supposed that all SiC-MOSFETs are identical, and they are turning-off. Note that in the MPS configuration the parasitic capacitances $C_{pac}$ are formed by two subsequent drain attached cooper tracers, i.e., $C_{paci}$ is a capacitance connected with drain-source terminals of the device $S_i$ (for i=2,3,4). As shown in the Fig. 4.9(b), the high frequency equivalent circuit can be simplified by short-circuiting the DC-bus terminals and $C_Y$ capacitors. Redrawing Fig. 4.9(b), a simplified high frequency equivalent circuit can be obtained as shown in Fig. 4.9(c). The equivalent drain-to-source parasitic capacitance of each device is expressed by Eqs. (4.15)-(4.16).

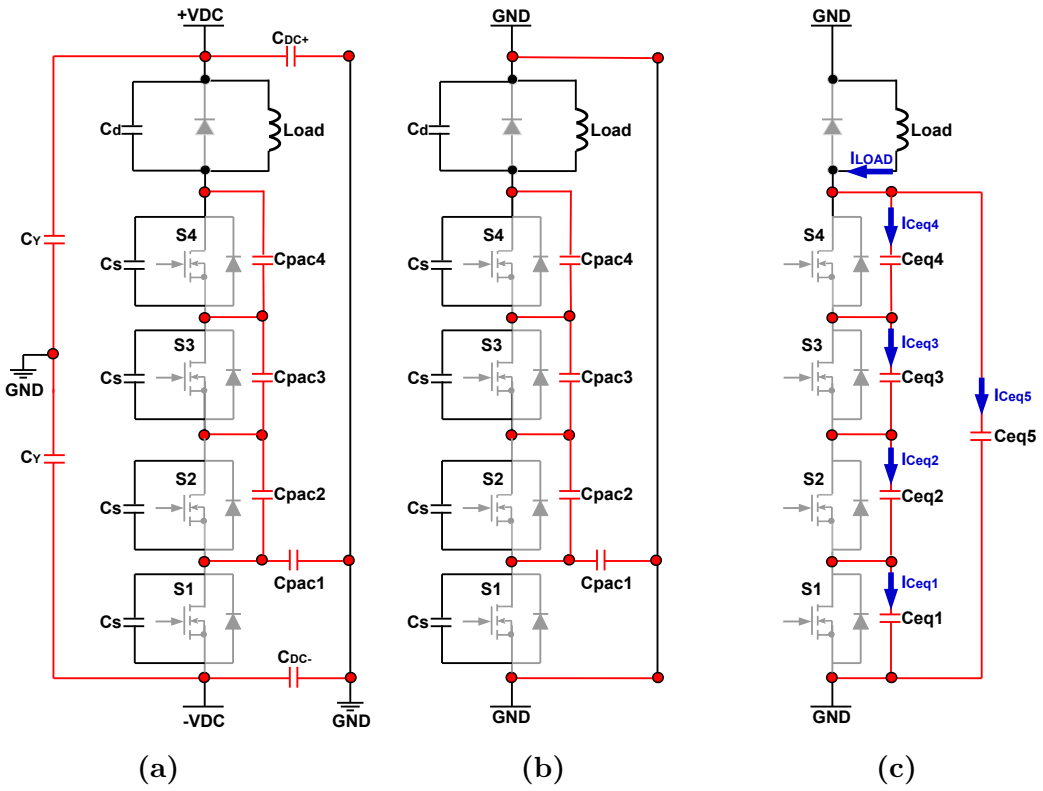



**Fig. 4.9.** Electrical circuit of four SiC-MOSFETs connected in series in the MSP package (a), high frequency circuit (b) and simplified electrical scheme (c).

$$C_{eqi} = C_s + C_{paci}, i = 1, 2, 3, 4. \tag{4.15}$$

$$C_{eq5} = C_d \tag{4.16}$$

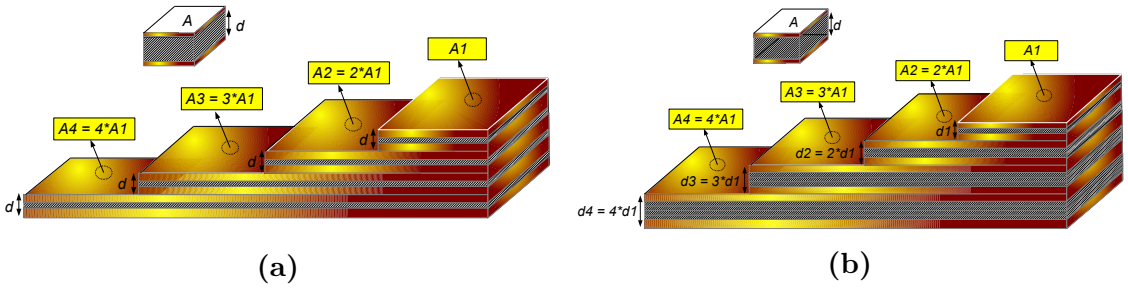
Analysing Fig. 4.9(c), the currents that circulate through the equivalent parasitic capacitances $C_{eqi}$ can be expressed by the Eqs. (4.17) and (4.18).

$$I_{Ceqi} = C_{eqi}\frac{dV_{dsi}}{dt} \tag{4.17}$$

$$I_{Ceq5} = C_{eq5}\frac{dV_{ds}}{dt} \tag{4.18}$$

To prove that the MSP package can balance the voltages, it can be supposed that the voltages across the series-connected devices in Fig. 4.9(c) are perfectly balanced, and find the $C_{pac}$ values that ensure this. Based on this assumption, it can be considered that the channel currents of series-connected devices are identical. Therefore, the following equations can be written:

$$C_{eq1}\frac{dV_{ds1}}{dt} = C_{eq2}\frac{dV_{ds2}}{dt} = C_{eq3}\frac{dV_{ds3}}{dt} = C_{eq4}\frac{dV_{ds4}}{dt} \tag{4.19}$$




**(a)** **(b)**

**Fig. 4.10.** 3D view of the proposed package concept with the same distance $d$ (a), and different distances $d$ (b).

$$(C_s + C_{pac1})\frac{dV_{ds1}}{dt} = (C_s + C_{pac2})\frac{dV_{ds2}}{dt} = (C_s + C_{pac3})\frac{dV_{ds3}}{dt} = (C_s + C_{pac4})\frac{dV_{ds4}}{dt} \quad (4.20)$$

According to Eq. (4.20), the series-connected SiC-MOSFETs can have the same switching speed behaviour if the parasitic capacitances $C_{paci}$ are identical. Therefore, to ensure an equal equivalent capacitance (drain to source) distribution among the series-connected devices, it is important to ensure that Eq. (4.21) is satisfied, i.e., once the isolated substrates are made of the same material, the ratio $\frac{A}{d}$ has to be the same for all $C_{paci}$ capacitances.

$$C_{pac} = \epsilon\frac{A}{d} = C_{pac1} = \epsilon\frac{A1}{d1} = C_{pac2} = \epsilon\frac{A2}{d2} = C_{pac3} = \epsilon\frac{A3}{d3} = C_{pac4} = \epsilon\frac{A4}{d4} \quad (4.21)$$

To this end, two 3D representations of the MSP package are shown in Fig. 4.10. Fig. 4.10(a) shows the proposed package/layout where the copper area ($A$) of each floating potential is different from the others, assuming that the dielectric material thickness ($d$) between them is the same. This simple solution induces different parasitic capacitances. Therefore, according to Eq. 4.20, the voltage balance cannot be ensured. A second geometry is shown in Fig. 4.10(b), where the thicknesses of the dielectric material layer are adapted to keep the $\frac{A}{d}$ ratio the same for all drain-to-source parasitic capacitances $C_{pac}$. Another solution is to keep the same distance ($d$) between all overlapping copper plates and the same area $A$ to ensure the same $\frac{A}{d}$ ratio for all drain-to-source parasitic capacitances $C_{pac}$.

Therefore, considering that the parasitic capacitances $C_{pac}$ have the same value for all the series-connected devices, Eq. (4.20) becomes:

$$(C_s + C_{pac})\frac{dV_{ds1}}{dt} = (C_s + C_{pac})\frac{dV_{ds2}}{dt} = (C_s + C_{pac})\frac{dV_{ds3}}{dt} = (C_s + C_{pac})\frac{dV_{ds4}}{dt} \quad (4.22)$$

In this case, the negative impacts of the packaging/layout on voltage balancing are nullified, and the stacked devices can have the same switching speed behaviour.

### Simulation Results For Four Series-Connected SiC-MOSFETs

As can be seen, since the MSP should provide the same switching speed behaviour for all the series-connected SiC-MOSFETs, the voltages across the devices should be balanced. To validate this theoretical approach, electrical simulations are made in LTSpice software with four Cree SiC-MOSFET Spice models C2M0160120 (1200V 19A), which are switched under a total blocking voltage of 1 kV and a load current of 20 A. The simulations are done in the hypothetical case where the gate drivers are perfect, no time delay between the gate signals and the power devices are identical. In other words, only the packaging/layout (capacitive elements) is taken into account. Figs. 4.11 and 4.12 show simulation results for the traditional packaging/layout (TRP) and the MSP one, respectively.

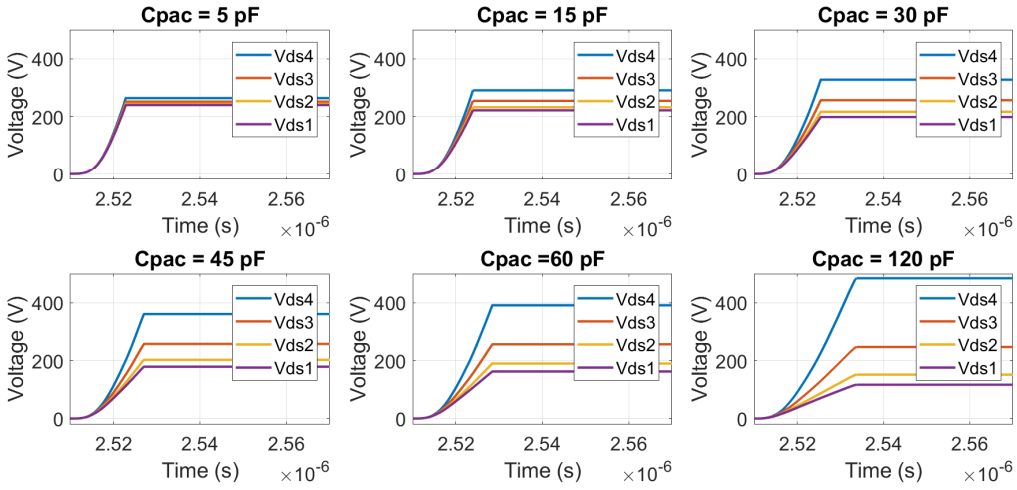



**Fig. 4.11.** TRP simulation results: voltage Sharing between four series-connected SiC-MOSFETs.

As expected, the voltage sharing in traditional packaging/layouts is drastically sensitive to the parasitic capacitances $C_{pac}$. In Fig. 4.1 for $C_{pac} = 5$ pF, an acceptable voltage balancing is presented. However, it is not a practical value, in traditional PCBs, $C_{pac}$ can reaches a few dozen $pF$ while in power modules, $C_{pac}$ can reaches a few hundred $pF$ [11]. In this case, as shown in Fig. 4.1, from $C_{pac} = 30\ pF$ to 120 $pF$, traditional packaging/layouts exacerbate voltage balancing problems. On the other hand, the MSP concept is not sensitive to $C_{pac}$ in terms of voltage sharing among the series-connected devices as shown in Fig. 4.12. Even for exacerbated values of $C_{pac}$, the bus-voltage is perfectly shared between the devices.

The switching speed is also improved in the proposed MSP concept when compared to the traditional one. Fig. 4.13 shows the $dv/dt$ as a function of $C_{pac}$ for the traditional (TRP) and MSP packages/layouts. The parasitic capacitances $C_{pac}$ drastically impact the $dv/dt$ of the switching cell. On the other hand, the MSP concept is less sensitive to $C_{pac}$. In the TRP, the currents that circulate through the parasitic capacitances $C_{pac}$ are deflected

from the switching cell to the ground or heatsink. In other words, a part of the currents that would be used to charge/discharge the device capacitances is deflected to the ground, slowing down the device switching speeds. On the other hand, in the MSP geometry, the currents that circulate through the parasitic capacitances $C_{pac}$ are returned locally to the switching cell.

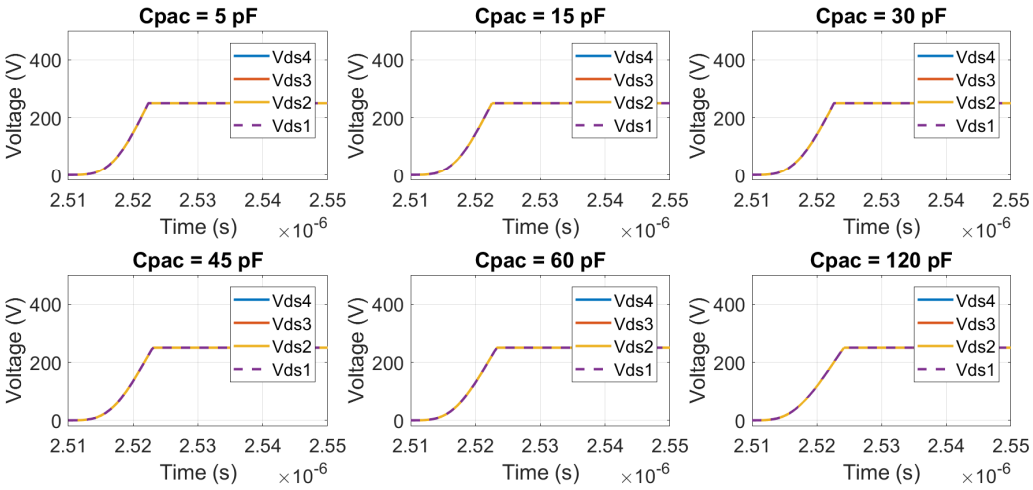



**Fig. 4.12.** MSP simulation results: voltage Sharing between four series-connected SiC-MOSFETs.

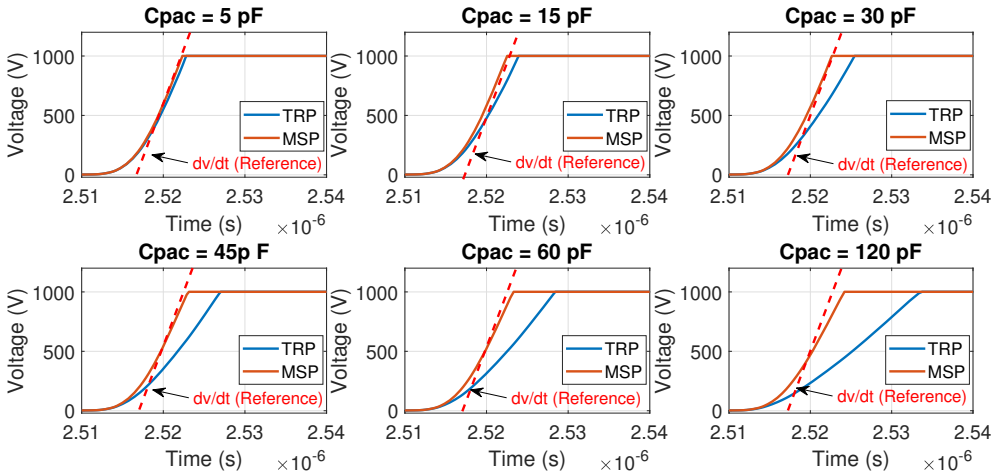



**Fig. 4.13.** Simulation results: $dv/dt$ as a function of $C_{pac}$ for TRP and MSP packages/layouts.

### Experimental Results For Four Series-Connected SiC-MOSFETs

To validate the theoretical approach, two simplified prototypes have been developed. In these prototypes, the MSP concept is emulated thanks to stacked FR4 layers to account for the package steps. Since the two packages, made out of FR4 materials are unable to

dissipate power, the series association is tested in a pulsed mode. The developed prototype meets the following requirements:

- Each copper plate that receives SiC device, has the same area, A = 10 $cm^2$.
- The FR4 dielectric thicknesses between two copper plates, are all the same, $d = 1.5$ $mm$.
- The isolated substrates are made of the same FR4 material and they have the same absolute permittivity, $\epsilon = 45$ $pF/m$.
- The measured parasitic capacitances between two copper plates are almost the same for the MSP prototype, $C_{pac} = 30$ $pF$ (discrepancy $< 5\%$ between these capacitances).
- The traditional packaging also introduces a parasitic capacitance $C_{pac}$ of 30 $pF$.

As shown in Fig. 4.14, a switching cell with four series-connected C2M0160120 SiC-MOSFETs (1200V, 19A), and one STPSC40H12CWL diode (1200V, 20A) has been used to investigate the influence of the traditional packaging and the proposed package concept on the voltage balancing and on $dv/dt$. A bus voltage of 1kV and a load current of 20A have been used in the experiments. No external drain-to-source resistor are added to provide the static voltage balancing.

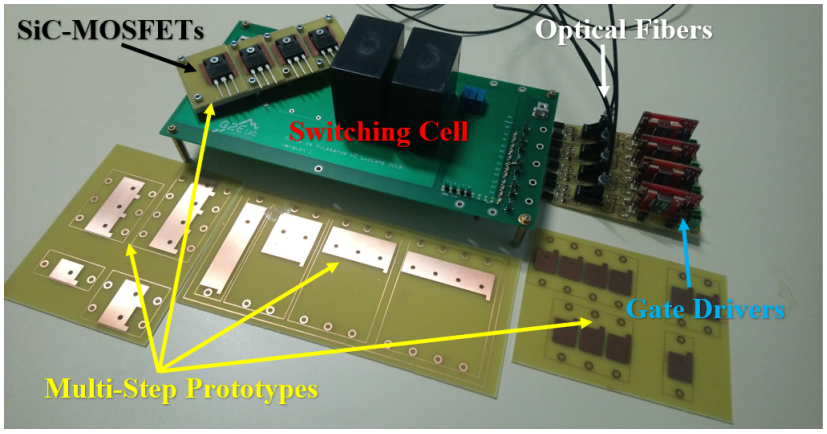



**Fig. 4.14.** Switching cell and package prototypes.

A specific calibration process is proposed to compensate the delay time and the effects of voltage probes. During this process, power devices are left with no connection to the FR4 package. In this situation, it is supposed that the parasitic capacitance $C_{pac}$ has an ultra-low value although probably still different to zero. The gate resistors and the delay times are adapted to have a perfect balancing. In this case (**CASE 1**), all effects generated by the gate drivers, voltage probes, the different characteristics between the devices, etc. are compensated. The switching speed calibration result is illustrated in Fig. 4.15. As can

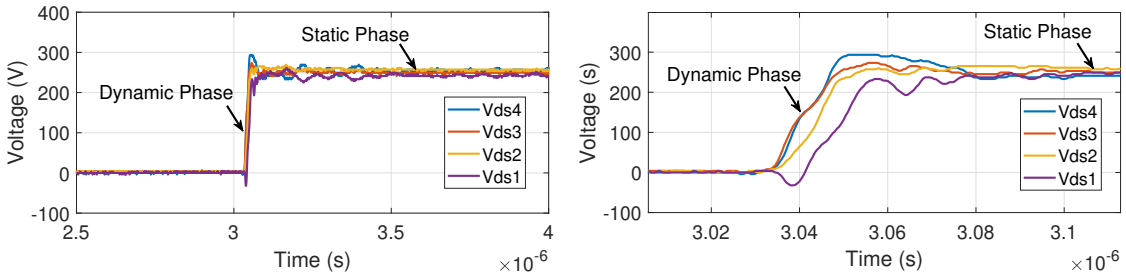



**Fig. 4.15.** Experimental results: voltage balancing achieved by the calibration process without FR4 package (a) and its zoomed view (b); CASE 1.

be seen in Fig. 4.15(a), balanced voltages of around 250V are achieved with a very small discrepancy ($< 15$ V) between them. The zoomed dynamic phase is shown in Fig. 4.15(b). As can be predicted by the models presented in this chapter, even after the calibration process, the highest device in the stack (S4) has the faster switching speed while S1 has the slowest.

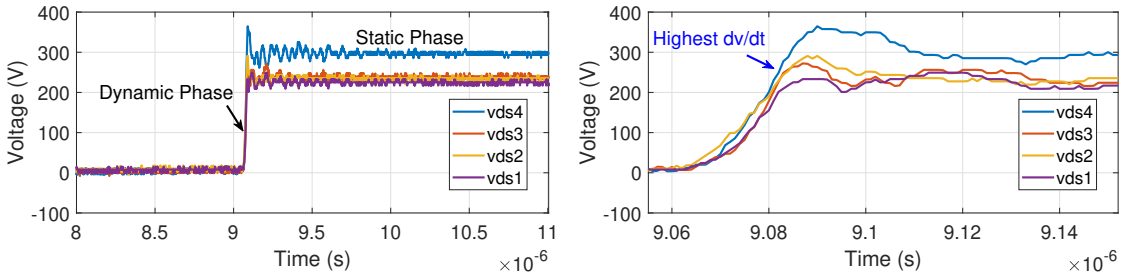



**Fig. 4.16.** Experimental results: voltage balancing after adding the traditional planar package (a) and its zoomed view (b); CASE 2.

Fig. 4.16 shows the voltage balancing across the series-connected SiC-MOSFETs when the traditional packaging is used **(CASE 2)**. As it can be seen in Fig. 4.16 (a), the parasitic capacitances introduced by the traditional planar package produce an important voltage unbalance. A considerable discrepancy of around 115 $V$ is observed between the drain-to-source voltages ($V_{ds4}$-$V_{ds1}$) across the series-connected devices. Note that the parasitic capacitance $C_{pac}$ in the traditional package prototype is only 30 $pF$. Classical power modules can introduce a few hundred $pF$, which will exacerbate voltage balancing problems. Fig. 4.16 (b) shows the zoomed dynamic switching speed of the devices. As mentioned in this chapter, the highest device on the stack takes the largest portion of the bus voltage. This phenomenon repeats itself in the present experiments where $V_{ds4}$ is approximately equal to 360 $V$, which represents approximately 44 % more than the ideal voltage (250 $V$).

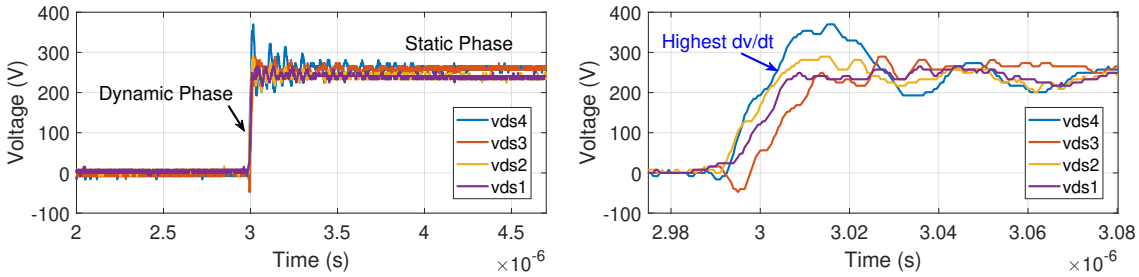



**Fig. 4.17.** Experimental results: voltage balancing after adding the proposed MSP package (a) and its zoomed view (b); CASE 3.

The experimental results for the MSP concept **(CASE 3)** are shown in Fig. 4.17. As expected, the voltage unbalancing has been drastically reduced. A small voltage discrepancy of around 31 $V$ is observed between the drain-to-source voltages across the devices. As well as in CASE 2, the highest device on the stack (S4) still takes the largest share of the DC bus voltage. However, in the **CASE 3**, the $V_{ds4}$ is approximately 265 $V$. It is within 6 % pf the ideal voltage (250 $V$). Note that in the three cases, the peak voltage during the turn-off switching is caused by the stray inductance of the switching cell. In this case, as no static resistors are used in the experiments, the discrepancy between the $V_{ds}$ voltages is measured in the static phase. The simulation results and Eqs. (4.26) and (4.27) show that the MSP concept can increase the middle point switching speed when compared to TRP.

The intrinsic parasitic capacitances of the power devices are dependent on drain and gate voltages as illustrated in Fig. 4.18 for the C2M0160120 (1200V 19A) SiC MOSFETs used here. At high voltage ratings, the output capacitance $C_{oss}$ falls dramatically; it decreases significantly when $V_{ds}$ increases,from 200 $pF$ ($V_{ds}$ = 20 $V$ ) to 47 $pF$ ($V_{ds} \geq$ 400 $V$). This is usually very characteristic of the non constant $dv/dt$ during switching transitions. To analyse the middle point switching speed of both packages, even taking into account the $C_{oss}$ variation, a $k$ factor ($C_s/C_{pac}$) is introduced in the switching speed analysis. Note that, $C_{oss} = C_s = C_{gd} + C_{ds}$.

### Turning-off dv/dt at Zero Channel Current

In this section, the $dv/dt$ is analysed in order to compare the TRP and MSP packages. An analytical model to predict the switching speed is outside the scope of this work. Therefore, to simplify the analyses and compare the packages, we will afocus on the maximum $dv/dt$ that the switching cell can reach. To this end, it is supposed that the power devices are switched very fast. In this case, their channel currents can be considered to have dropped to zero long before the drain-source voltages rise to $\frac{V_{DC}}{2}$. It can be achieved under large gate current or light load. For example, Fig. 4.19 shows the current distribution in a SiC-

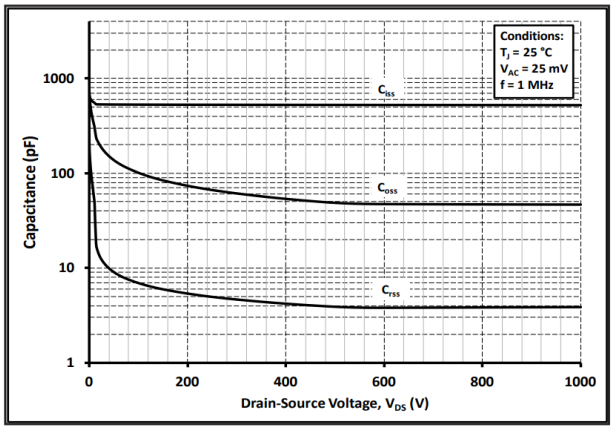



**Fig. 4.18.** Intrinsic capacitance variations as a function of drain-source voltage of SiC-MOSFETs C2M0160120 (1200V, 19A) [92].

MOSFET. During the turn-off transition, the load current can be expressed by Eq. (4.23), where $I_{CN}$ is the channel current expressed by Eq. (4.24) [93].

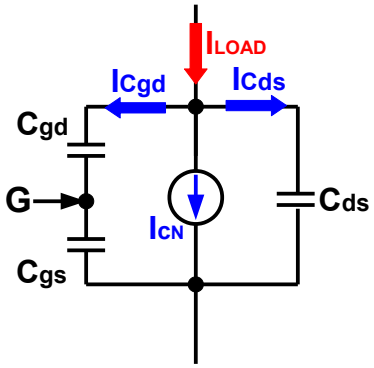



**Fig. 4.19.** Simplified SiC-MOSFET model.

$$I_{LOAD} = I_{Cgd} + I_{Cds} + I_{CN} \tag{4.23}$$

$$I_{CN} = g_f \frac{(1 + \frac{C_{ds}}{C_{gd}})(V_{DR} - V_{TH}) + R_G.I_{LOAD}}{(1 + \frac{C_{ds}}{C_{gd}}) + g_f.R_G} \tag{4.24}$$

Where $V_{DR}$ is the gate drive voltage, $V_{TH}$ and $g_f$ are, respectively, the threshold voltage and transconductance of the device.

At light loads, the $dv/dt$ is limited by the power loop, i.e., all $I_{LOAD}$ is used to charge/discharge the device output capacitances, and as a result, the channel current ($I_{CN}$) drops to 0 $A$. In other words, there is a critical load current ($I_{Lcrtical}$) that makes $I_{CN} = 0$. From Eq. (4.24), making $I_{CN} = 0$, it is possible to find the critical load current as shows Eq. (4.25). Therefore, for all load currents lower than $I_{Lcrtical}$ the channel current drops to zero.

$$I_{Lcrtical} = \frac{(C_{gd} + C_{ds})(V_{DR} - V_{TH})}{R_G C_{gd}} \tag{4.25}$$

Another way to make $I_{CN} = 0$ during the turn-off transition is to make $R_G$ tend to zero. According to Eq. (4.25), if $R_G$ tends to zero (large gate current), $I_{Lcrtical}$ tends to infinity. In this case, no matter the value of $I_{LOAD}$, it will always be less than the critical load current, making $I_{CN} = 0$.

Making $I_{CN} = 0$ is useful to investigate the maximum middle point $dv/dt$ of the switching cell: if $I_{CN} = 0$, the $dv/dt$ estimations will be exclusively a function of $I_{LOAD}$ and parasitic capacitances of the switching cell.

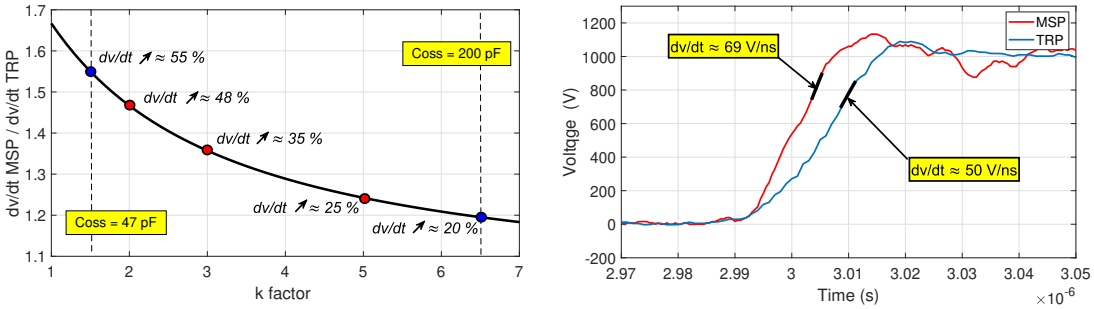
Therefore, making the channel currents of the series-connected devices equal to zero, and according to the Figs. 4.6(c) and 4.9(c), the maximum middle point $dv/dt$ for the TRP and MSP packages can be expressed by Eqs. (4.26) and (4.27), respectively.

$$\frac{dV}{dt}TRP = \frac{IL}{(C_{eq1T}//C_{eq2T})//(C_{eq3T}//C_{eq4T}) + C_{eq5T}} \tag{4.26}$$

$$\frac{dV}{dt}MSP = \frac{IL}{(C_{eq1M}//C_{eq2M})//(C_{eq3M}//C_{eq4M}) + C_{eq5M}} \tag{4.27}$$

Where $C_{eqiT}$ represents the equivalent parasitic capacitances of the traditional package, which are expressed by Eqs. (4.10)-(4.14), and $C_{eqiM}$ represents the equivalent parasitic capacitances of the MSP package, which are expressed by Eqs. (4.17)-(4.18)

The improvement on switching cell $dv/dt$ magnitude provided by the MSP when it is compared to the traditional packaging is predicted in Fig. 4.20(a). The improvement is calculated by dividing Eq. (4.27) by Eq. (4.26). This more accurate analysis shows that the MSP solution provides further benefits compared to the reference package since during the power device switching transition the $k$ factor decreases, offering better voltage balance and switching dynamics. Since variable capacitors are not easy to combine with others to simplify the equivalent circuit and that computation of equivalent capacitors is more complex, the analysis is further carried out considering capacitance charges. Considering the parasitic capacitance introduced by the package $C_{pac} = 30\ pF$ and the output capacitance of power device $C_{oss}$, their respective charge during a turn-off switching transition 0-1000V are: $Q_{pac} = 30\ nC$ and $Q_{oss} = 62.2\ nC$. It appears that the parasitic capacitance of the package increases by about 50% the amount of charge that is needed to charge all parasitic components in the equivalent circuit. Over the entire switching transition, the package parasitic elements will induce a significant reduction on $dv/dt$. It will also introduce a significant current path leading to voltage unbalance in series associations. Fig. 4.20(b) shows the experimental results for both packages in terms of $dv/dt$. As can be seen, the switching speed on the




**(a)** **(b)**

**Fig. 4.20.** Predicted $dv/dt$ improvement as a function of $k$ factor ($C_{oss}/C_{pac}$) (a), and measured $dv/dt$.

middle point of the switching cell has been boosted from 50.0 V/ns to 69 V/ns. It represents a gain of 38 % on the $dv/dt$ of the switching cell which may produce a significant gain in terms of switching losses. In the case where the power devices are left with no connection to a FR4 package, the measured $dv/dt$ is approximately 75 $V/ns$.

As can be seen, when the proposed MSP is applied for series-connected SiC-MOSFETs, it can mitigate voltage balancing problems and also improve the switching speed when compared to the classical planar packaging. Together with other voltage balancing techniques, such as clamping methods, the MSP can be applied to mitigate the voltage unbalancing, and consequently the stress and losses on the passive devices will be reduced.

The first MSP proposition is more suitable to optimise series-connected device topologies, since the gate drivers are not taken into account. In order to propose a further optimized multi-step package that takes into account the gate driver parasitic capacitances, providing better voltage sharing performance, a novel MSP package is proposed in the next section.

## 4.3 Multi-Step Packaging/Layout Concept: 2nd Proposition

In the last section, a MSP was proposed to investigate the impacts of the packaging/layout on the voltage sharing across the series-connected devices. However, the gate drivers were not taken into account, which makes this MSP concept impractical. Indeed, the parasitic capacitance introduced by the gate drive circuitry is one of the main causes of voltage unbalancing. To solve this issue, in this section a Multi-step packaging/layout (2MSP) concept is proposed to provide a more realistic solution in terms of voltage balancing. The parasitic capacitance introduced by the gate drivers are also considered.

Fig. 4.21(a) shows the classical gate drive circuitry where the parasitic capacitances introduced by DC-DC power supplies ($C_{ps}$) and signal transmission functions of gate drivers

($C_{iso}$) are highlighted. The parasitic capacitances $C_{ps}$ and $C_{iso}$ have the same dynamic influence on the system. Here, we consider that $C_{iso}$ is negligible in relation to $C_{ps}$ since in the experiments, insulation signals are implemented by optical fibers. Fig. 4.21(b) shows the parasitic elements of the gate driver power supply and its connections, where $Z_p$ and $Z_s$ are, respectively, the impedances on the primary and secondary sides of gate drivers. As can be seen, two reference potentials are presented in classical switching cells [74, 75], i.e., the ground or reference potential of the remote control circuit (GND) and the reference potential of the power circuit (-VDC). Both GND and -VDC are isolated from each other. It is important to note that for safety reasons the heatsink is attached to the reference potential of the remote control circuit (GND), not to -VDC.

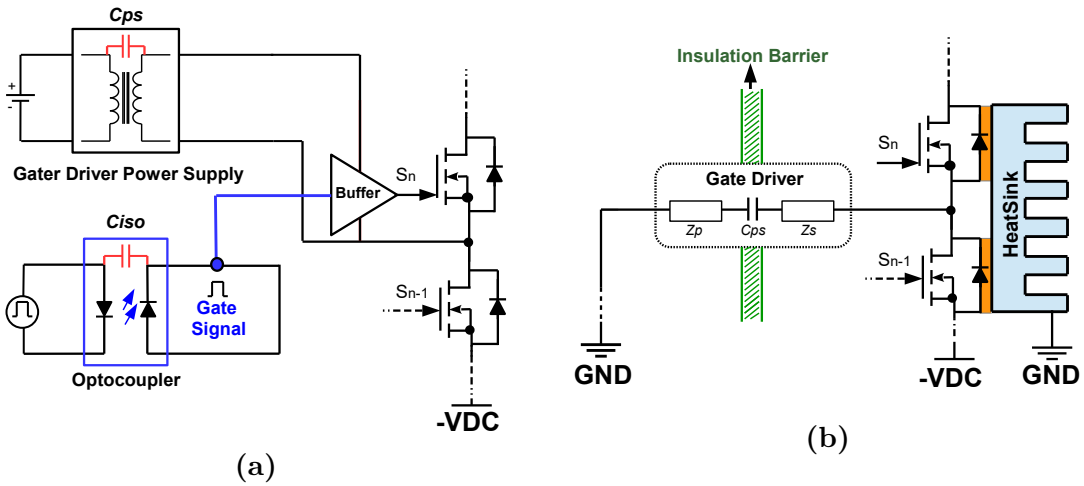



**Fig. 4.21.** Classical gate driver (a), and its parasitic elements (b).

Considering the parasitic capacitances introduced by the gate drive circuitry, a new electrical circuit for four SiC-MOSFETs connected in series is shown in Fig. 4.22, where:

- $C_{psi}$ is the parasitic capacitance introduced by the gate driver $i$, which is associated to the SiC-MOSFET $i$.
- $C_{paci}$ is the package/layout parasitic capacitance associated to the SiC-MOSFET $i$.
- $C_Y$ is the Y-capacitor usually placed between + VDC and GND, and - VDC and GND to mitigate conducted EMI noise.
- $C_d$ and $C_s$ are the intrinsic capacitances of the diodes and SiC-MOSFETs, respectively. It is supposed that the intrinsic parasitic capacitances of the power devices ($C_s$) are all identical.

In Fig. 4.22, the yellow zone represents the parasitic capacitance network introduced by the classical packaging/layout. The capacitances $C_{pac}$ are located between the drain

potential of each device and the ground potential reference of the control side (GND). The blue zone represents the gate driver parasitic capacitance network.

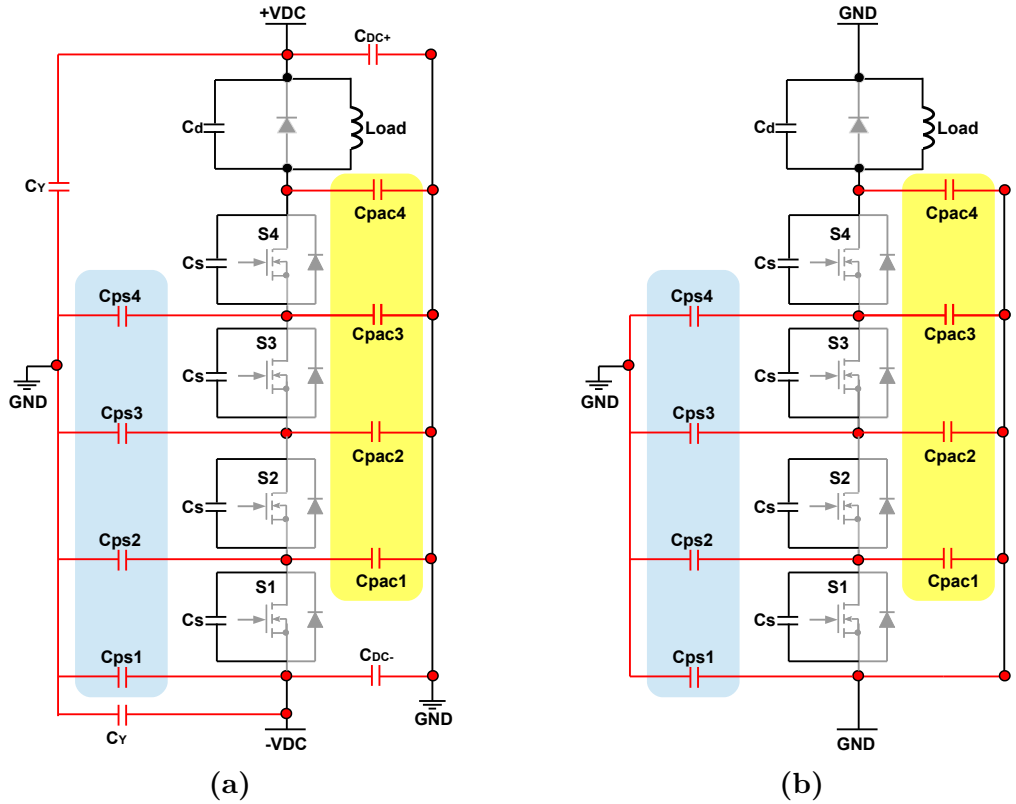



**Fig. 4.22.** Electrical circuit of classical packaging and gate drive circuitry (a), and its simplified high frequency circuit (b).

As shown in Fig. 4.22(b), a high frequency equivalent circuit can be achieved by short-circuiting the DC-bus terminals and $C_Y$ capacitors. As can be seen, two parasitic capacitance networks impact the voltage balancing, i.e., the gate driver parasitic capacitance network (blue zone), and the package/layout parasitic capacitance network (yellow zone). The parasitic capacitance $C_{ps1}$ has no influence on the high frequency behaviour of the switching cell since it is short-circuited by GND.

To prove that these parasitic capacitance networks unbalance the voltages across series-connected SiC-MOSFETs, a simple proof by contradiction can be done. Consider the current distribution shown in Fig. 4.23, and the following equations:

$$I_{s4} = I_{cn4} + I_{cs4} \tag{4.28}$$

$$I_{s4} = I_{cn3} + I_{cs3} + I_{ps4} + I_{pac3} \tag{4.29}$$

Where $I_{cni}$ it the channel current of the device $i$.

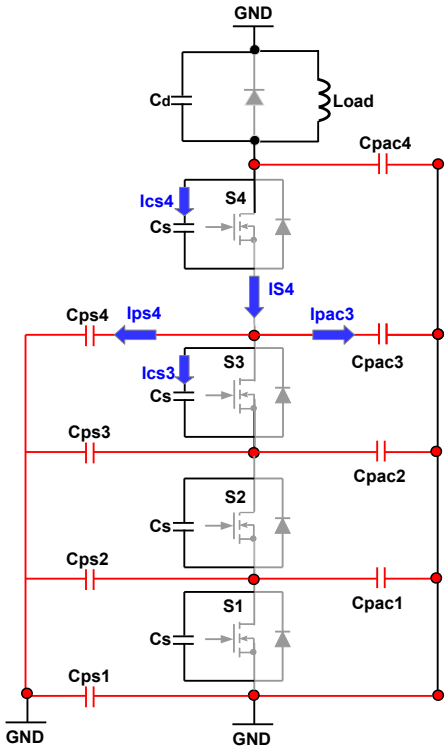



**Fig. 4.23.** Simplified electrical circuit of classical packaging and gate drive circuitry.

Applying the proof by contradiction, it can be considered that the $V_{ds}$ voltages across the devices are perfectly balanced. Therefore the following conditions can be applied:

- 1) the devices experiment equal drain-to-source $dv_{ds}/dt$. It implies that $I_{cs4} = I_{cs3} = I_{cs}$ since the devices are considered identical.
- 2) the channel currents $I_{cn3}$ and $I_{cn4}$ are identical.

Applying these conditions to Eqs. (4.28) and (4.29):

$$I_{cn4} = I_{s4} - I_{cs} \tag{4.30}$$

$$I_{cn3} = I_{s4} - I_{cs} - I_{ps4} - I_{pac3} \tag{4.31}$$

According to Eqs. (4.30) and (4.31), the second conditions is respected and the voltages across the series-connected devices are perfectly balanced, if and only if, $I_{pac3} = I_{ps4} = 0$. Unfortunately, this condition is not reachable. The same proof by contradiction can be done for the other devices in the stack to prove that even if there is no delay between the gate signals and no mismatch between device characteristics, the $V_{ds}$ voltages will be unbalanced due to the parasitic capacitances of gate driver and package/layout.

Fig. 4.24(a) shows the electrical circuit configuration of the parasitic capacitances of the Multi-Step Packaging (MSP) and gate drive circuitry. The green zone represents the parasitic

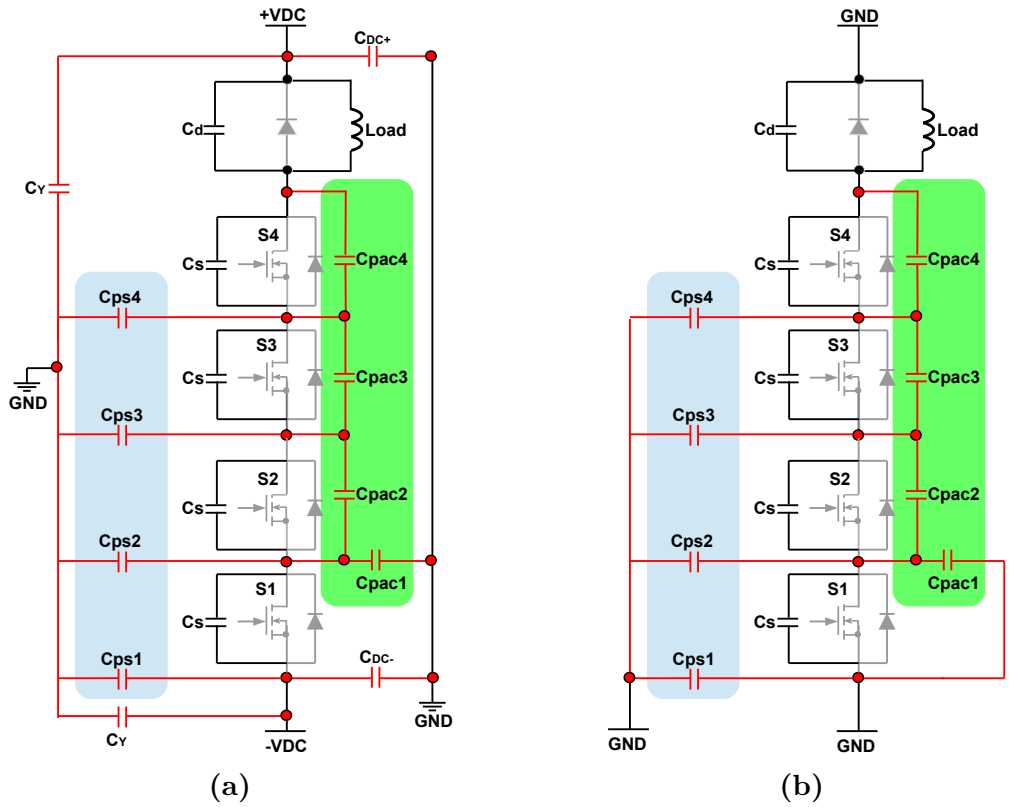



**Fig. 4.24.** Electrical circuit of MSP packaging and gate drive circuitry (a), and its simplified high frequency circuit (b).

capacitance network introduced by the MSP, where the capacitances $C_{pac}$ are located between the drain and source terminals of each device. The blue zone represents the gate driver parasitic capacitance network.

As shown in Fig. 4.24(b), a high frequency equivalent circuit can be obtained by short-circuiting the DC-bus terminals and $C_Y$ capacitors. As can be seen, two parasitic capacitance networks impact the voltage balancing, i.e., the gate driver parasitic capacitance network (blue zone), and the package/layout parasitic capacitance network (green zone). The parasitic capacitance $C_{ps1}$ has no influence on the high frequency behaviour of the switching cell since it is short-circuited by GND.

In the section **"Multi-Step Packaging/Layout Concept: 1st Proposition"** the following supposition was validated :**"if identical parasitic capacitances $C_{pac}$ are placed between drain-to-source terminals of each device it will result in a perfect voltage balancing"**. However, this validation was based on the following conditions:

- 1) The gate drivers do not introduce parasitic capacitances ($C_{ps} = 0$).
- 2) The series-connected SiC-MOSFETs are identical.
- 3) There is no delay between gate signals.

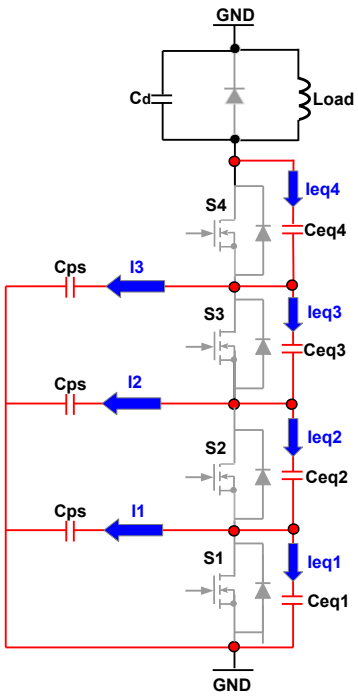



**Fig. 4.25.** Current distribution in the MSP electrical circuit.

Characterization and a careful selection of SiC-MOSFETs can reduce the mismatch between SiC-MOSFET intrinsic capacitances. Optimized gate driver circuitry can mitigate the delay between gate signals. Furthermore, active gate controls can reduce it to negligible levels. On the other hand, in the same way that $C_{pac}$, the parasitic capacitance of the isolated gate drive power supply is always present, and as demonstrated in last the chapter, it can increase voltage balancing problems. Therefore, the main idea of the 2MSP is to modify the parasitic capacitance $C_{pac}$ values to compensate the impact of the gate drive circuitry ($C_{ps}$). In this case, the impacts of $C_{pac}$ and $C_{ps}$ will be compensated by each other. To this end, consider that all the gate drivers in Fig. 4.24 are identical, i.e., $C_{ps1} = C_{ps2} = C_{ps3} = C_{ps4} = C_{ps}$. Therefore, the electrical circuit shown in Fig. 4.24(b) can be simplified as shown in Fig. 4.25, where $C_{eqi} = C_s + C_{paci}$.

To find the appropriate values of $C_{pac}$ that compensate the influence of $C_{ps}$ capacitances, it can be supposed that the voltages across the series-connected devices in Fig. 4.25 are perfectly balanced. Based on this assumption, it can be considered that:

- The SiC-MOSFET channel currents are identical.
- The drain potential of device $N$ experiments $N$-times the $\frac{dv}{dt}$ of the drain potential of the device S1.
- The series-connected devices have the same drain-to-source $\frac{dv_{ds}}{dt}$.

Therefore, according to the mentioned considerations and the current distribution shown

in Fig. 4.25, the following equations can be written:

$$I_{eq4} = I_3 + I_{eq3} = C_{ps}\left(3\frac{dV_{ds}}{dt}\right) + C_{eq3}.\frac{dV_{ds}}{dt} = C_{eq4}.\frac{dV_{ds}}{dt} \tag{4.32}$$

$$I_{eq3} = I_2 + I_{eq2} = C_{ps}\left(2\frac{dV_{ds}}{dt}\right) + C_{eq2}.\frac{dV_{ds}}{dt} = C_{eq3}.\frac{dV_{ds}}{dt} \tag{4.33}$$

$$I_{eq2} = I_1 + I_{eq1} = C_{ps}\left(\frac{dV_{ds}}{dt}\right) + C_{eq1}.\frac{dV_{ds}}{dt} = C_{eq2}.\frac{dV_{ds}}{dt} \tag{4.34}$$

From Eq. (4.34), the following equation can be written:

$$C_{eq2} = C_{ps} + C_{eq1} = C_s + C_{pac2} = C_{ps} + C_s + C_{pac1} \tag{4.35}$$

Therefore, the relation between $C_{ps}$, $C_{eq1}$ and $C_{eq2}$ can be expressed by Eq.(4.36).

$$C_{pac2} = C_{ps} + C_{pac1} \tag{4.36}$$

Eq.(4.36) is enough to find the appropriate values of $C_{pac}$ that compensate the $C_{ps}$ influence on the voltage balancing for two series-connected devices.

From Eq. (4.33), the following equation can be written:

$$C_{eq3} = 2C_{ps} + C_{eq2} = C_s + C_{pac3} = 2C_{ps} + C_s + C_{pac2} \tag{4.37}$$

Therefore, the relation between $C_{ps}$, $C_{eq2}$ and $C_{eq3}$ can be expressed by Eq.(4.38).

$$C_{pac3} = 2C_{ps} + C_{pac2} \tag{4.38}$$

Eqs.(4.36) and (4.38), can be used to find the appropriate values of $C_{pac}$ that compensate the $C_{ps}$ influence on the voltage balancing for three series-connected devices.

From Eq. (4.32), the following equation can be written:

$$C_{eq4} = 3C_{ps} + C_{eq3} = C_s + C_{pac4} = 3C_{ps} + C_s + C_{pac3} \tag{4.39}$$

Therefore, the relation between $C_{ps}$, $C_{eq3}$ and $C_{eq4}$ can be expressed by Eq.(4.40).

$$C_{pac4} = 3C_{ps} + C_{pac3} \tag{4.40}$$

Eqs.(4.36),(4.38) and (4.40), can be used to find the appropriate values of $C_{pac}$ that compensate the $C_{ps}$ influence on the voltage balancing for four series-connected devices.

According to Eqs.(4.36),(4.36) and (4.40), the mathematical recurrence, expressed by Eq. (4.41) can be written to find the appropriate values of $C_{pac}$ that compensate the $C_{ps}$ influence on the voltage balancing for N-series-connected devices.

$$C_{pacN} = (N-1)C_{ps} + C_{pac(N-1)} \tag{4.41}$$

As can be seen, it is necessary to know the values of the gate driver parasitic capacitance $C_{ps}$ and define one of the parasitic capacitances $C_{pac}$. According to Eq. (4.41), higher the position of the device in the stack, the larger its associated parasitic capacitance $C_{pac}$. Therefore, to satisfy Eq. (4.41), a novel multi-step packaging concept is proposed in the present chapter as shown in Fig. 4.26. This new packaging geometry has the following characteristics:

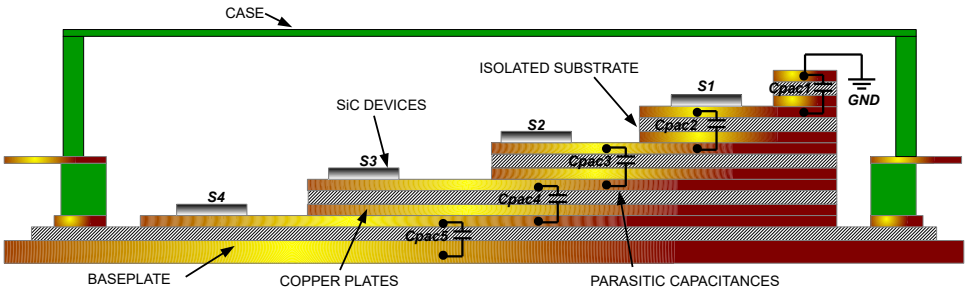



**Fig. 4.26.** Novel Proposed Multi-Step Packaging.

- Compared to the 1st MSP investigated in last section, the position of the devices is inverted, i.e., if in the electrical scheme the devices are placed in the following bottom-to-top direction S1→S2→...→SN, in the physical geometry the devices have to be placed in the inverted position SN→...→S2→S1. This is to respect Eq. (4.41), i.e., to ensure that the device connected to the highest electrical potential has the highest drain-to-source parasitic capacitance $C_{pac}$. Note that, according to Eq. (4.41), $C_{pacN} > C_{pacN-1}$ .. $C_{pac2} > C_{pac1}$.

- For N devices connected in series, it is necessary to have N+1 steps. As shown in Fig. 4.26, for four series-connected devices, five steps are implemented. The fifth stage is introduced to generate the parasitic capacitance $C_{pac1}$ between the drain attached bottom device and the ground.

- The number of parasitic capacitances introduced by the packaging is equal to N+1. As shown in Fig. 4.26 for four series-connected devices, five parasitic capacitances are introduced. The last one, i.e., $C_{pac5}$ in Fig. 4.26, has no influence on the voltage

balancing. However, $C_{pac5}$ has important impacts on the global $dv/dt$ of the switching cell and on common mode EMI emissions.

Taking a specific case of study where four series-connected devices driven by gate drivers that introduce parasitic capacitances $C_{ps}$ equal to 15 $pF$, the values of $C_{pac}$ that compensate the influence of $C_{ps}$ on voltage balancing can be found as follows:

- Number of series-connected devices N = 4.
- Choosing $C_{pac1}$ equal to 15 $pF$.
- Calculating $C_{pac2}$ (N =2) :

$$C_{pac2} = (2-1)C_{ps} + C_{pac(2-1)} \rightarrow C_{pac2} = 15pF + 15pF = 30pF \tag{4.42}$$

- Calculating $C_{pac3}$ (N =3) :

$$C_{pac3} = (3-1)C_{ps} + C_{pac(3-1)} \rightarrow C_{pac3} = 2(15)pF + 30pF = 60pF \tag{4.43}$$

- Calculating $C_{pac4}$ (N =4) :

$$C_{pac4} = (4-1)C_{ps} + C_{pac(4-1)} \rightarrow C_{pac4} = 3(15)pF + 60pF = 105pF \tag{4.44}$$

**Simulation Results For Four Series-Connected SiC-MOSFETs**

The simulation results of the classical packaging for four series-connected C2M SiC-MOSFETs C2M0080120D (1200 V, 36 A) are shown in Fig. 4.27. The simulations are done in the hypothetical case where there is no time delay between the gate signals and the power devices are identical. The gate driver parasitic capacitance are modelled as a 15 $pF$ capacitor. The series-connected devices are switched under a total blocking voltage of 1 kV and a load current of 36 A. The simulation results are performed using LTSpice software.

As can be seen, the gate drive circuitry and classical packaging increase drastically the voltage unbalance across the series-connected devices. Even for small values of $C_{pac}$, exacerbated unbalanced voltages can be reached. The voltage unbalancing is dependent on the $C_{pac}$ values. For $C_{pac} = 5\ pF$ the largest difference between the $V_{ds}$ voltages is approximately 100 $V$, while for $C_{pac} = 120\ pF$ the largest difference between the $V_{ds}$ voltages is approximately 400 $V$.

These simulation results show that **the gate driver parasitic capacitances $C_{ps}$, and the package/layout parasitic capacitances $C_{pac}$ are two of the main parasitic elements in the switching cell that contribute to unequal voltage sharing**

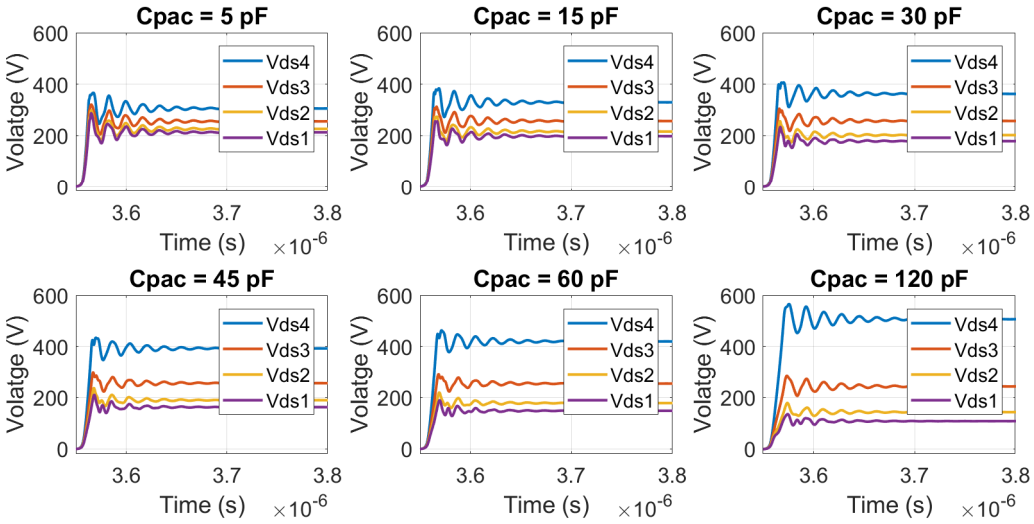



**Fig. 4.27.** Simulation results: voltage sharing between four series-connected as a function of $C_{pac}$ (classical planar package).

**between the series-connected SiC-MOSFETs**. In other words, even under identical SiC-MOSFETs and synchronised gate signals, exacerbated unbalanced voltages are introduced by the classical parasitic capacitance networks of gate drivers and packages/layouts.

Fig. 4.28 shows the simulation results of the proposed MSP, where six parasitic capacitances networks are analysed. The parasitic capacitances of the gate drive circuitry are modelled as a capacitor of 15 $pF$. Each parasitic capacitance network is calculated using Eq. (4.41). Table 4.1 shows the values used for each analysed parasitic capacitances network.

**Table 4.1.** Parasitic capacitances network values.

| $C_{ps}$ $(pF)$ | $C_{pac1}$ $(pF)$ | $C_{pac2}$ $(pF)$ | $C_{pac3}$ $(pF)$ | $C_{pac4}$ $(pF)$ |
|---|---|---|---|---|
| 15 | 2 | 17 | 47 | 92 |
| 15 | 5 | 20 | 50 | 95 |
| 15 | 10 | 25 | 55 | 100 |
| 15 | 15 | 30 | 60 | 105 |
| 15 | 30 | 45 | 75 | 120 |
| 15 | 60 | 75 | 105 | 150 |

The simulation results of Fig. 4.28 show perfectly balanced voltages across the series-connected SiC-MOSFETs for all analysed parasitic capacitance networks. It means that providing $C_{pac}$ capacitances that meet the conditions in Eq. (4.41), no matter their values the voltage balancing can be reached. This is very useful since the MSP can be designed to be as compact as possible.

The middle point $dv/dt$ of the switching cell is compared for the classical and MSP packages as shown in Figs. 4.29 and 4.30, respectively. The $dv/dt$ of both packages are compared to the same $dv/dt$ reference. As show in Fig. 4.29, the classical package/layout is

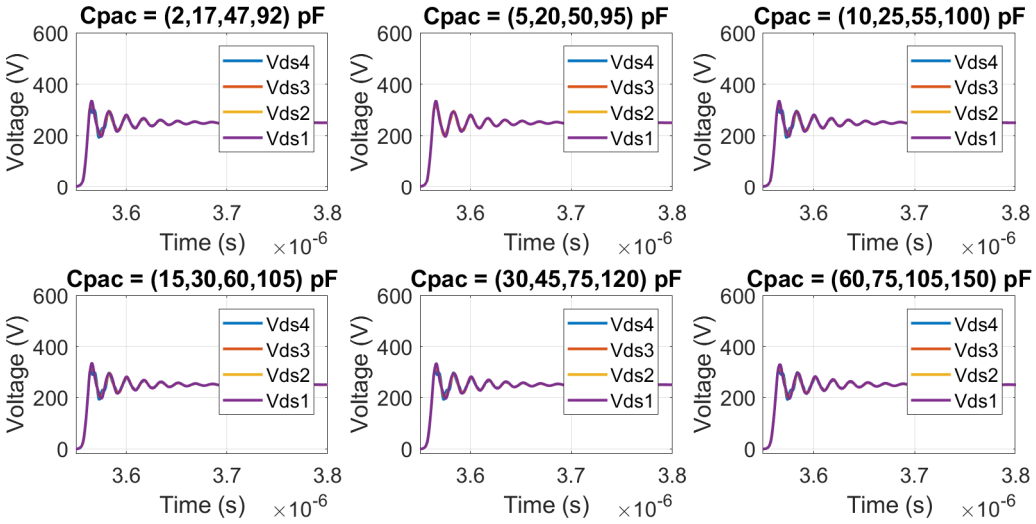



**Fig. 4.28.** Simulation results: voltage sharing between four series-connected as a function of $C_{pac}$ (proposed MSP package).

very sensitive to the parasitic capacitance $C_{pac}$. The switching speed is drastically reduced when $C_{pac}$ increases from 5 $pF$ to 120 $pF$. On the other hand, the results in Fig. 4.30 show that the MSP package is less sensitive to $C_{pac}$. In the TRP, the currents that circulate through the parasitic capacitances $C_{pac}$ are deflected from the switching cell to the ground or heatsink. In other words, a part of the currents that would be used to charge/discharge the device capacitances is deflected to the ground, slowing down the device switching speeds. On the other hand, in the MSP geometry, the currents that circulate through the parasitic capacitances $C_{pac}$ are returned locally to the switching cell, speeding up the SiC-MOSFETs.

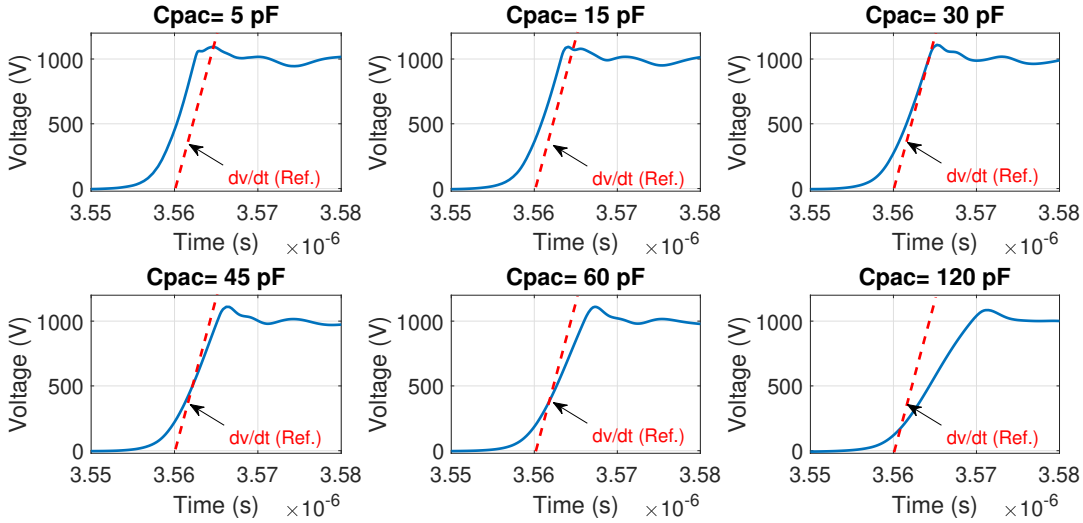



**Fig. 4.29.** Simulation results: middle point switching speed as a function of $C_{pac}$ (classical planar package).

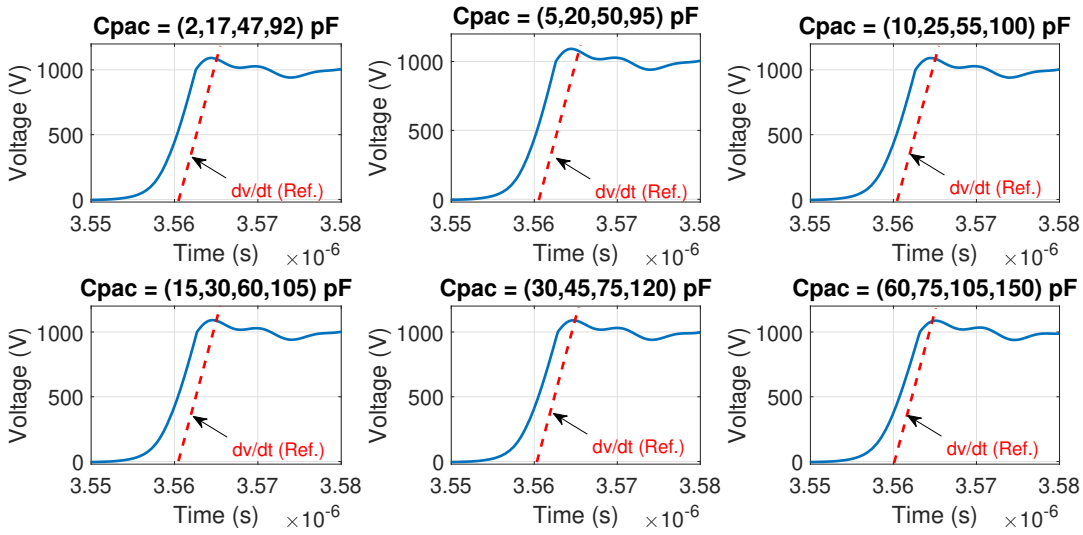



**Fig. 4.30.** Simulation results: middle point switching speed as a function of $C_{pac}$ (proposed MSP package).

### Timing Delays and Device Parameter Tolerance Sensitive Analysis

Up to now, it has been considered that there is no delay between the gate signals and no device parameter mismatch between the series-connected devices. Characterization and careful selections of SiC-MOSFETs can reduce the mismatch between their intrinsic capacitances. Optimized gate driver circuitry can mitigate the delay between gate signals. However, if these optimizations are not taken into account, it can drastically impacts the MSP performance on voltage balancing. Therefore, a sensitive analyse is done in this section to estimate the impacts of the delay between gate signals and device parameter mismatch on the proposed MSP. Only two series-connected SiC-MOSFETs are analysed. Otherwise, the sensitive analysis becomes very complex. Furthermore, the next experimental results presented in this section are based on a testing platform with two series-connected SiC-MOSFETs.

To analyse the robustness of the MSP in terms of voltage balancing the following parameters are used to perform the sensitive analysis :

- $\Delta C_{gs}$, $\Delta C_{gd}$ and $\Delta C_{ds}$. It represents the difference between the intrinsic capacitances of the series-connected devices. The values used in the analysis are based in a study performed in [61, 94].
- $\Delta R_g$. It represents the difference between the internal gate resistances of the devices. The values used in the analysis are based in a study performed in [94].
- *Delay*. It represents the delay between the gate signals.
- $\Delta T_j$. It represents the junction temperature difference between the devices. As will be

explained in this section, in MSP package each device has a different thermal resistance. Therefore, it can also impact the voltage balancing across the devices.

Two C2M0080120D SiC-MOSFETs Spice Models are used in the analysis, where the top device parameters are fixed, and the parameter variations are imposed to the bottom device. The gate resistances are initially set to 10Ω. The gate driver parasitic capacitances $C_{ps}$ are set to 15 $pF$, and the MSP parasitic capacitances $C_{pac1}$ and $C_{pac2}$ are set, respectively, to 15 and 30 $pF$. The series-connected devices are switched under a total blocking voltage of 1 kV and a load current of 36 A. The analysis is done in relation to the voltage across the top device, i.e., how much the top device voltage increases from the ideal voltage (half the bus voltage) to the final value caused by the parameter variation. The results, expressed in (%) are shown in Fig. 4.31.

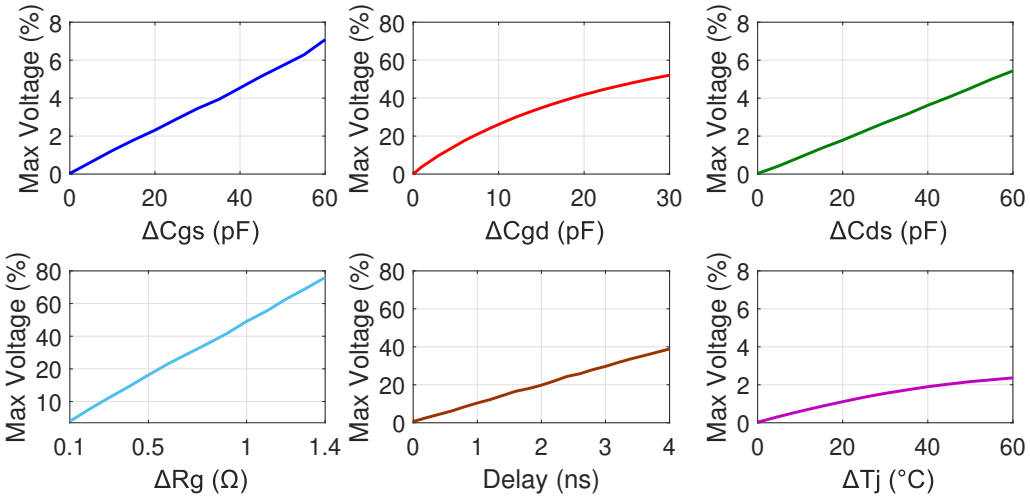



**Fig. 4.31.** Sensitive analysis results.

As can be seen, the mismatch between the intrinsic capacitances $C_{gs}$ slightly impacts the voltage balancing. Every 20 $pF$ of difference, the top device voltage increases only by 2%. The mismatch between the intrinsic capacitances $C_{ds}$ has similar impact on voltage balancing. On the other hand, the mismatch between the intrinsic capacitances $C_{gd}$ drastically increases the voltage unbalancing. For $\Delta C_{gd} = 20\ pF$ the top device voltage increases by 40%. In other words, if the bus voltage is equal to 1 kV, the top devices experiment a drain-to-source voltage of 700 $V$. This is understandable since during the switching transition (Miller Plateau, $V_{ds}$ rising/falling), the switching speed behaviour is very dependent of $C_{gd}$ , i.e., the switching speed represents the necessary time to charge/discharge $C_{gd}$.

The mismatch between internal gate resistances also drastically impacts voltage unbalancing. A $\Delta R_g = 0.5\ \Omega$ is enough to increase the top voltage device by 20%. This is understandable since the gate current required to charge and discharge the internal gate

capacitances is controlled by the gate resistances. Consequently, the switching speed of the device and the voltage balancing performance are drastically dependent of $\Delta R_g$.

The delay between gate signals also has an important influence on the voltage balancing. As can be seen in Fig. 4.31, 4 $ns$ is enough to increase the top device voltage by 40%. Therefore, optimized gate signal circuitry is required to improve the voltage balancing across the series-connected SiC-MOSFETs.

The junction temperature difference among the devices is another important parameter for the MSP package since each device in the stack has a different thermal resistance. The main device parameters that change with $T_j$ are the drain-to-source current $I_{DS}$, the drain-to-source on-state resistance $R_{DSon}$ and the threshold voltage $V_{TH}$. Between these parameters, $V_{TH}$ is the most important in relation to dynamic voltage balancing. However, according to the SiC-MOSFET C2M0080120D datasheet, the $V_{TH}$ variation as a function of $T_j$ is only 0.005 $V/°C$. This small variation is validated by simulations results as can be seen in Fig. 4.31, where even for exacerbated values of $\Delta T_j$ the top device voltage does not increase considerably, i.e., a $\Delta T_j = 40\ °C$ increases the voltage unbalancing only by 2%.

According to Fig. 4.31, $\Delta C_{gd}$, $\Delta R_g$ and $\Delta delay$ are the three most important parameters that can considerably increase voltage balancing problems. Fig. 4.32 shows the parametric analysis of these three parameters. The analysis is done for four values of $\Delta R_g$, 0.2, 0.3, 0.4 and 0.5 Ω. $\Delta C_{gd}$ is changed from 0 to 4 pF, and $\Delta delay$ from 0 to 1 $ns$. As can been, the MSP package can provide good voltage balancing if these parameters are limited according to acceptable levels of voltage unbalancing. For example, supposing that it is acceptable that the top device in the stack takes 20% more than the ideal voltage ($\frac{V_{DC}}{2}$), and $\Delta R_g$ is limited to 0.2 Ω. For $\Delta C_{gd}$ values $\leq$ 4 $pF$, and $\Delta delay$ values $\leq$ 0.4 $ns$, the top device voltage will not increase more than 20%, ensuring a good and acceptable voltage balancing across the series-connected SiC-MOSFETs.

It is important to note that, the faster the SiC-MOSFETs switch, the more the parameters impact the voltage balancing. The sensitive analysis presented here is done under hard switching operation, where the middle point switching cell reaches approximately 200 $V/ns$. In other words, for power devices that reach a $dv/dt$ less than 200 $V/ns$, these parameters have less influence, and the MSP is less sensitive to the parameter mismatches.

**Experimental Results For Two Series-Connected SiC-MOSFETs**

As shown in Fig. 4.33, a switching cell with series-connected C2M0080120D SiC-MOSFETs (1200 V, 36 A), and one diode STPSC40H12CWL (1200V, 20A) has been used to investigate the influence of the the proposed package concept on the voltage balancing under a total blocking voltage of 1 kV. The DC-DC converter implemented for each gate driver used in the experiment is a Murata MGJ6D242005SC that has a parasitic capacitance

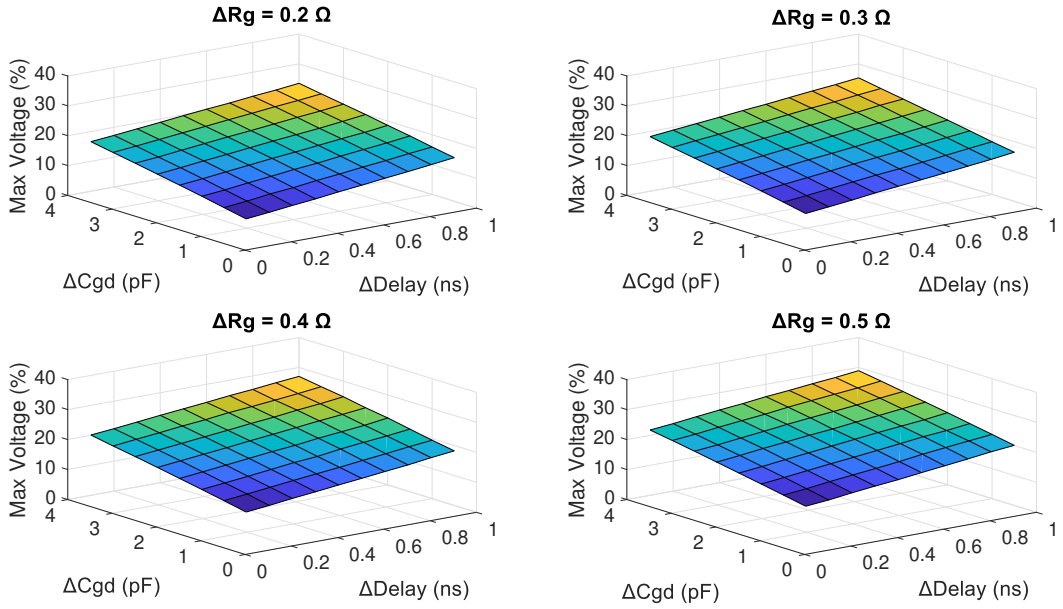



**Fig. 4.32.** Parametric analysis results as a functions of $\Delta R_g$, $\Delta C_{gd}$ and $\Delta delay$.

$C_{ps} = 15\ pF$. Optical fibers are used for signal isolation.

An external RC circuit is used to reduce the gate signal delays to low levels ($<1\ ns$). Another solution is to control the gate delay time to less than 1 ns by using a DS1023 digital delay line in the gate drive circuit. The DS1023 is an 8-bit programmable timing element where the time resolution of the digital control can be controlled by 0.25 ns.

A specific calibration process is implemented to mitigate the mismatches between the intrinsic characteristics of the devices. Under a specific operation point, the external gate resistance are adapted to compensate the mismatch between the internal gate resistances. This calibration process emulates a careful device selection to reduce device mismatch parameters. Note that the mismatch between the intrinsic device capacitances can not be mitigated due their non-linearity. During this process, power devices are left with no connection to a FR4 package. In this situation, it is supposed that the parasitic capacitance $C_{pac}$ has an ultra-low value although probably still different to zero.

To validate the theoretical approach, two simplified prototypes have been developed. In these prototypes, the 2MSP concept is emulated thanks to stacked FR4 layers to account for the package steps. Since the two packages, made out of FR4 materials are unable to dissipate power, the series association is tested in pulsed mode. The developed MSP prototype meets the following requirements:

- The copper plates to which the bottom and top SiC devices are attached, have the following areas: A (bottom device) = 5 $cm^2$ and A (top device) = 10 $cm^2$.
- The FR4 dielectric thicknesses between two copper plates, which generate each $C_{pac}$

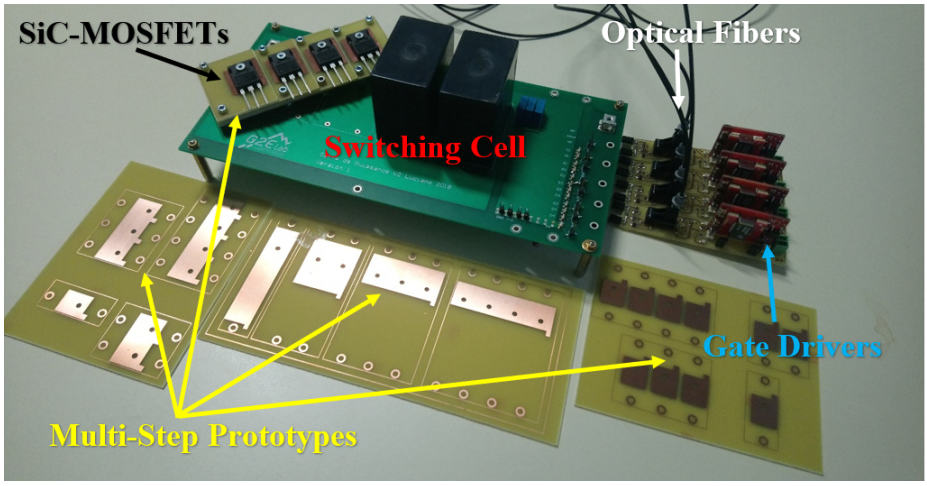



**Fig. 4.33.** Switching cell and package prototypes.

are all the same, $d = 1.5\ mm$.

- The isolated substrates are made of the same FR4 material and they have the same absolute permittivity, $\epsilon = 45\ pF/m$.
- The measured parasitic capacitances for the MSP prototype are $C_{pac1} \approx 15\ pF$ and $C_{pac2} \approx 30\ pF$.
- The traditional packaging introduces parasitic capacitances $C_{pac}$ of around 30 $pF$.

Fig. 4.34 shows the voltage balancing across power devices when the traditional packaging is used. A pulse train is applied to analyse the voltage balancing under different load currents. The pulse train changes the load current from 0 A to 40 A with a current step of around 6 A. As can be seen in Fig. 4.34, the parasitic capacitances introduced by the traditional planar package and gate drive circuitry produce an exacerbated voltage unbalancing that increases with the load current. This phenomenon is associated with the switching speed, which is directly proportional to the load current. In other words, when the load current goes up, the gate drivers and package capacitances ($C_{ps}$ and $C_{pac}$) have more and more impact on the voltage balancing. If no voltage balancing method is used, the series-connected devices can be seriously damaged.

The proposed MSP package is tested under the same conditions used toas for the traditional package. Fig. 4.35 shows the experimental results for the MSP. As can be seen, a good voltage balancing is achieved since $C_{ps}$ and $C_{pac}$ compensate each other. A very small voltage difference (30 $V$) is observed. However, analysing the voltage balancing across the series-connected SiC-MOSFETs, it can be seen that the voltage sharing has a small variation with the load current. This is due to the fact that: 1) although the gate signal delay is less than 1 $ns$, it can still cause voltage unbalance. According to the sensitivity analysis in Fig.

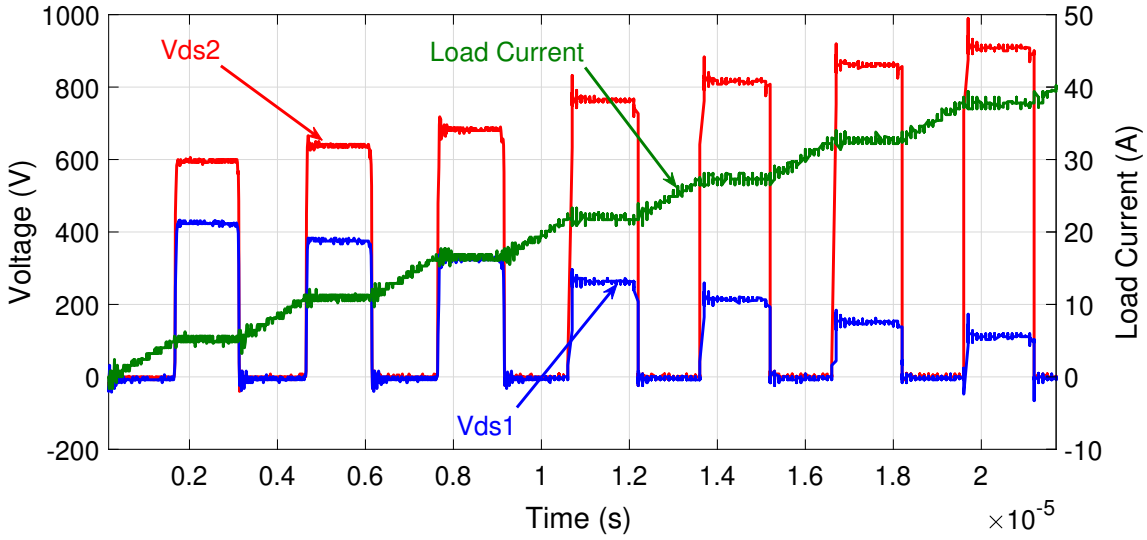



**Fig. 4.34.** Experimental results: voltage unbalancing across two series-connected SiC-MOSFETS; classical planar package.

4.31, even a gate signal delay of 1 $ns$ is enough to unbalance the voltages across the series-connected devices by 10% . 2) The mismatch between the device intrinsic capacitances. According to Fig. 4.31, the mismatch between the $C_{gd}$ capacitances has a strong impact on the voltage balancing, and a large $\Delta C_{gd}$ can override the good voltage balancing provided by the proposed package.

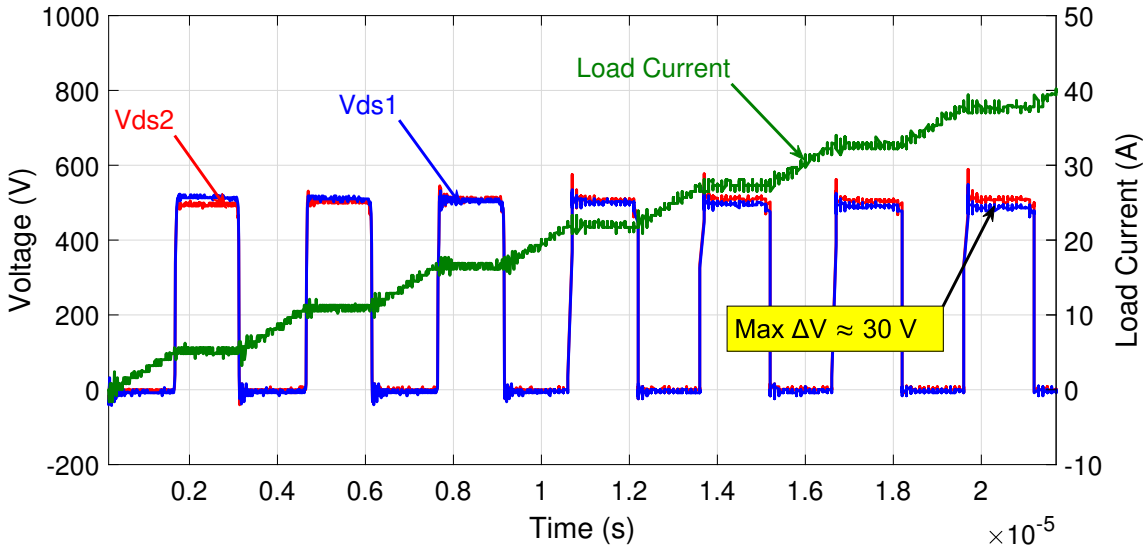



**Fig. 4.35.** Experimental results: voltage balancing across two series-connected SiC-MOSFETS; proposed MSP package.

The dynamic voltage balancing for three different values of load current, i.e., $IL$= 12, 18 and 24 $A$ i spresented in Fig. 4.36. In all cases, the two series-connected SiC-MOSFETs

have similar $dv/dt$ as predicted by the theoretical analyses presented in this chapter. Note that the mismatch between device $dv/dts$ is more visible for a load current equal to 24 $A$. At this point, the voltage unbalancing causes have more impact since the switching speed starts to increase considerably when compared to the previous switching points (IL $<$ 18 $A$). A small dynamic and static voltage difference can be observed at IL $=$ 24 $A$.

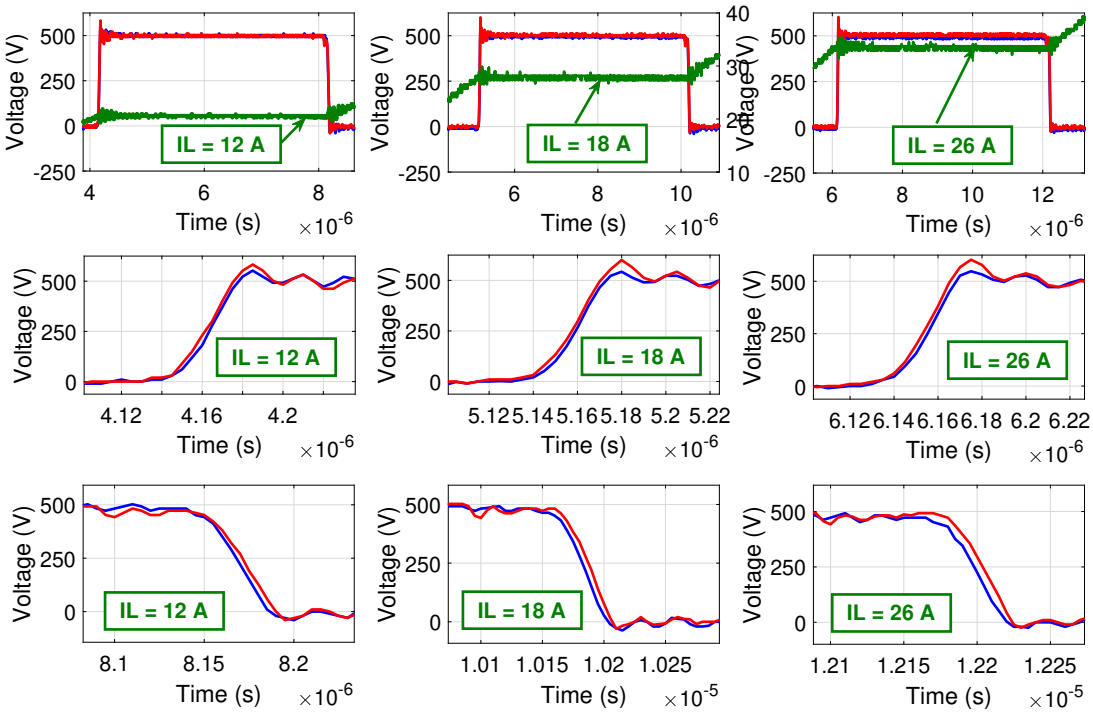



**Fig. 4.36.** Experimental results: voltage balancing across two series-connected SiC-MOSFETs as a function of the load current; proposed MSP package.

Fig. 4.37(a) shows the output waveforms as a function of a pulse train that changes the load current from 0 to 50 $A$ with a current step of around 16 $A$. Fig. 4.36(b) shows the maximum middle point $dv/dt$ as a function of the load current. As can be seen, the middle point switching cell experiments high $dv/dt$, which reach approximately 60 V/ns for $IL = 50$ $A$. According to the C2M0080120D SiC-MOSFETs (1200 V, 36 A) datasheet, the fall and rise times for each individual device are 14 and 22 $ns$ respectively. The values are based under tests with blocking voltage of 800 $V$, load current of 20 $A$ and external gate resistances of 2.5 Ω. It means that the proposed MSP package has low negative impact on the switching cell $dv/dt$ since only two "capacitors"of 15 and 30 $pF$ are added by the MSP package. Therefore, the proposed MSP is an effective way to reduce voltage balancing problems without slowing down the devices. The impact of the MSP on the $dv/dt$ depends of $C_{pac}$ values. The higher the $C_{pac}$ values, the more impact they have on the switching speed. On the other hand, high values of $C_{pac}$ increase the MSP performance in terms of voltage balancing since the mismatch between device intrinsic capacitances becomes negligible.

The MSP package is also tested under light load conditions. Fig. 4.38 shows the voltage

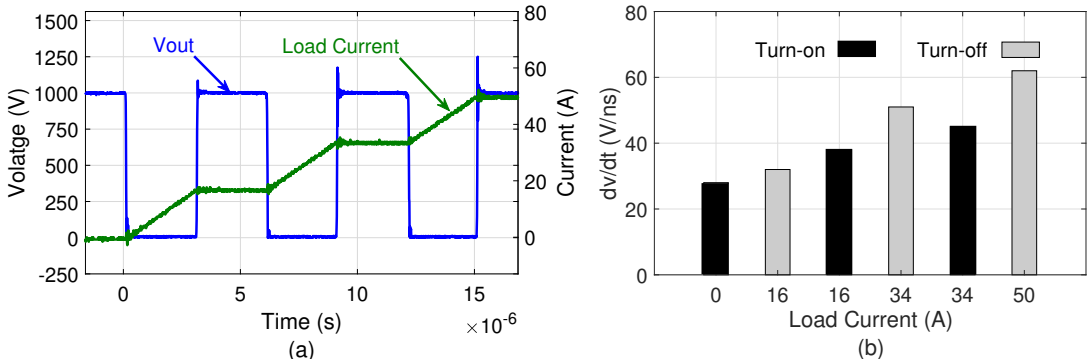



**Fig. 4.37.** Experimental results: output waveforms (a) and middle point switching speed (b) as a function of the load current; proposed MSP package.

balancing of two series-connected SiC-MOSFETs as a function of a pulse train that changes the load current from 0 to 700 $mA$. This emulates some medium-voltage (1-10 kV) low-current ($< 500$ $mA$) applications [95–99], such as high-voltage low current power supplies, pulsed discharge currents, dielectric barrier discharges, plasma pulse generator, etc.

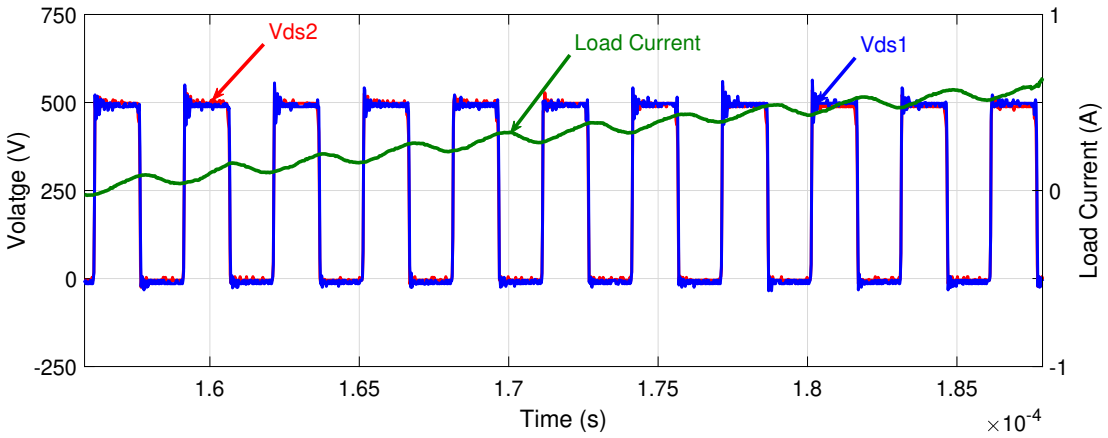



**Fig. 4.38.** Experimental results: voltage sharing performance between two series-connected at light loads.

As can be seen in Fig. 4.38, at light loads, the proposed MSP package provides even better voltage balancing than at high load currents. This phenomenon is associated to the switching speed, which is dependent on the load current. At light loads the switching speed is drastically reduced (compared to high load currents). Therefore, mismatches between device parameters, gate signals delay, etc. have less and less impact on the voltage balancing.

### 4.3.1 Comments About Thermal Management

The MSP package introduces non homogeneous propagation paths for the heat flux from each device to ambient. The addition of several dielectric layers brings an increase

of the junction to ambient thermal resistance, which produces an increase on the junction temperature $T_j$ of devices that are above the bottom device (located closer to the heat sink). This temperature increase is a function of heat flux and the characteristics of the additional dielectric layers. The lower is the dielectric layer thermal resistance, the lower will be the impact on the junction temperature. Also the lower will be the thermal resistance of the additional dielectric layer(s) with respect to the remaining thermal resistance on the pathway of the heat, the lower will be the impact of the additional layers.

A simple first order 1D thermal model can be developed to investigate this issue as shown in Fig. 4.39, where:

- $T_{jN}$ is the junction temperature of the device N, where the number 1 represents the bottom device and the numbers 2,3 and 4 represent the subsequent devices.
- $T_a$ is the ambient temperature.
- $P_s$ is the dissipation source in each device, representing the power losses, considered in this example as all equal.
- $R_{thjc}$ is the junction to case thermal resistance (mainly the die itself and the die attach).
- $R_{thcs}$ is the case to sink thermal resistance (mainly the dielectric layers).
- $R_{thsa}$ is the heatsink thermal resistance (mainly the heat sink, including thermal grease).

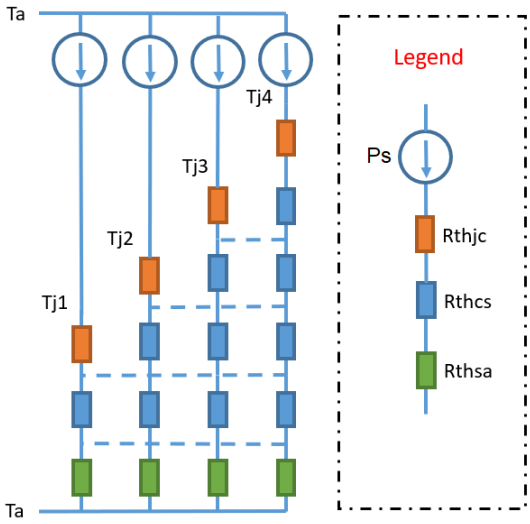



**Fig. 4.39.** MSP thermal resistance 1D model.

Based on the equivalent circuit presented in Fig. 4.39, the junction temperatures of the devices 2, 3 and 4 increase with respect to device 1 are shown in Fig. 4.40, where a

graph plots the impact of the thermal conductivity of the dielectric layer and its impact over junction temperature rise in the MSP package. Some values used to calculate the junction temperature increase among the series-connected devices are based on the datasheet of the device used in the experiments, which leads to $R_{thjc}$ of 0.1 °C/W and a cross section through the dielectric layer of 17x14 mm$^2$. The thickness of the dielectric material is considered constant and equal to 300 $\mu$m. It is also supposed that $T_a$ = 25°C and the maximum acceptable junction temperature $T_{jmax}$ is equal to 125 °C. Three dielectric materials are analysed in Fig. 4.40, and in all the cases a heat flux of 60 W is considered.

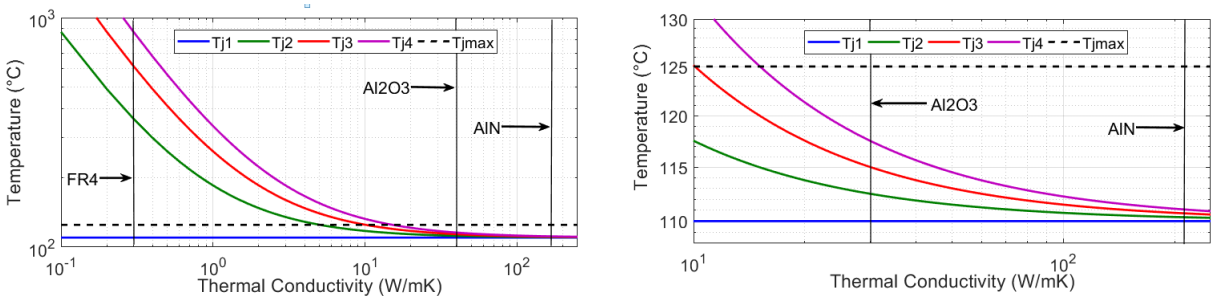



**Fig. 4.40.** Junction temperature increase among the series-connected devices as a function of the thermal conductivity(a) and its zoomed view (b) for $P_s$ = 60 W, $T_j$ = 110 °C, $T_a$ = 25 °C and $R_{thjc}$ = 0.1 °C/W.

As can be seen in Fig. 4.40(a), the temperature increase among the devices is drastically dependent on the thermal conductivity of the dielectric material ($K_T$). Considering a heat flux $P_s$ of 60 W and a dielectric composed by FR4 material, the junction temperature distribution over the four power devices is unacceptable. This is due to the very low thermal conductivity of FR4, i.e., $K_T \approx 0.3$ W/mK. However, if other dielectric materials with better thermal resistance are used, such as $AlN$ and $Al_20_3$, the junction temperature distribution over the four power devices can be drastically reduced. As shown in Fig. 4.40(b), which is a zoom of Fig. 4.40(a), considering $P_s$ equal to 60 W, a $R_{thsa}$ equal to 1.27 °C/W per device for planar design and $T_j$ = 110 °C, for Al2O3 dielectric layers ($K_T \approx 25$ W/mK), the impact on $T_{J4}$ is limited, with the temperature rise up to 10°C. In the same way, for 300$\mu$m $AlN$ dielectric layers ($K_T \approx 220$ W/mK) the impact on $T_{J4}$ is even more limited to 1°C. Taking into account the impact of $T_j$ rise on device power losses, the resulting total temperature increase is up to 15°C for $Al_20_3$ dielectric layers and 2,7°C for AlN dielectric materials.

It is important to note that these results are highly dependent on heat flux and heat sink design. However, this brief analysis shows that if the additional dielectric layers have small thermal resistances with respect to the other thermal resistance on the path of the heat flux, then, the MSP has a limited impact on the distribution of the junction temperatures $T_j$ of the devices implemented on each step of the power module. Neglecting the impact of junction temperature over component losses, if each additional dielectric layer introduces a

thermal resistance X% of the total thermal resistance from $T_j$ to $T_a$, then, the impact on $T_j$ rise per step is limited to X%. This would have a very limited impact on voltage sharing as illustrated in Figs. 4.32 and 4.31. If the junction temperature rise exceeds 5 to 10%, the impact on component losses could have to be taken into account to verify that the final junction temperature rise for each component implemented in the MSP remains below the maximum junction temperature.

### 4.3.2 Conclusion

In this chapter new package concepts to reduce the voltage unbalancing across series-connected SiC-MOSFETs are analysed. In a first step, basics and concepts are explained using mathematical analysis. The package concepts are compared to the traditional 2D planar solution in terms of voltage unbalance across the series-connected devices and dv/dt behaviour on the middle point of the switching cell. The study are performed by theoretical and experimental analyses.

The first analysed MSP package shows better performance than the classical one in terms of voltage balancing and switching speed. However, the 1st MSP does not take into account the parasitic capacitances introduced by the gate driver circuitry. In other words, the 1st MSP package is more suitable for voltage balancing and switching speed optimization. This first investigation validates the idea that the packaging capacitances have a strong impact on dynamic behaviour of the series-connected SiC-MOSFETs.

Based on the 1st MSP package, a second one is investigated in this chapter. The 2nd package takes into account the parasitic capacitance introduced by the gate driver circuitry. As expected, the 2nd MSP package shows the best performance in terms of voltage balancing and switching speed. The present study demonstrates that if the delay between gate signals and device parameter mismatch are kept small enough, the 2nd MSP package can provide an acceptable voltage sharing performance without needing other voltage balancing techniques.

However, ensuring small gate signal delay ($<$ 1ns) and acceptable device parameter mismatch is very complex. Therefore, other voltage balancing techniques should be used to ensure an acceptable voltage balancing performance even under larger gate signal delay and device parameter mismatch. To this end, a novel voltage balancing method that provides a perfect voltage balancing across the devices is proposed in the next chapter.

# Chapter 5

# A Novel Active Gate Driver for Series-Connected SiC-MOSFETs: A Proposition

In the previous chapters, a great effort was made to balance the voltage across the devices by natural techniques, i.e., by using the parasitic capacitances of the packaging and gate driver circuits. The proposed techniques have good performances in terms of voltage balancing. The voltage sharing across the series-connected SiC-MOSFETs is drastically improved by the proposed Multi-Step Packages. However, it can not provide adequate voltage balancing under exacerbated gate signal delays and/or large mismatch between the intrinsic device parasitic capacitances. The only way to achieve an acceptable voltage balancing in such conditions is to use the proposed technique in conjunction to other voltage balancing methods or other individual techniques. Snubber circuits can provide good voltage sharing performance [33–46]. However, they drastically reduce the switching speed of devices. Applying snubber circuits in conjunction to the proposed MSP would reduce the benefits of the MSP, slowing-down the switching speed of the devices increasing the switching losses. Clamping techniques can be used individually or in conjunction to the MSP package in order to protect the series-connected devices [47–49]. However, the dynamic voltages can still remain unbalanced, which means difference switching speeds across the devices, leading to thermal management and reliability problems. Active control techniques have demonstrated excellent voltage sharing performance without drastically increasing switching losses [32, 45, 52–67]. Furthermore, active controls could be applied in conjunction with MSP packages without degrading their effect on voltage balancing.

Therefore, based on the experience gained during this Ph.D. work, the author would like to propose a Novel Active Gate Driver for Series-Connected SiC-MOSFETs. A novel concept of active gate driver based on the analysis of the state of the art in the context of series-connected SiC-MOSFETs is presented in this chapter. The proposition is validated by numerical simulations. Some practical aspects are then proposed to go towards the experimental validation.

## 5.1 Introduction

The Active Gate Drive (AGD) was introduced in the 80's for IGBT turn-off protection [100, 101]. Since then, researchers have spent a significant amount of effort into the

improvement of the AGD performances. Various AGD techniques and control strategies have been proposed for Si-IGBTs or Si-MOSFETs. However, the switching transient of SiC devices can be completed in a few nano-seconds, which implies to adapt active gate drive techniques to switching speeds in the range of 10 $V/ns$ - 100 $V/ns$. The circuit schematics, the components bandwidth, the control strategy as well as timing strategy should be carefully designed. For this reason, some conventional AGDs designed for Si-IGBTs and Si-MOSFETs are not longer suitable for SiC devices. An overview introducing various driving technologies for the SiC power devices is given in [102].

In series-connected SiC-MOSFETs, the challenges remains the same, i.e., the switching speed of the devices can drastically increase voltage balancing problems. A variety of attempts have been made to achieve voltage balancing among series-connected SiC-MOSFETS by means of active gate control circuits. Two main methods are employed in the literature : 1) time-delay control techniques [32,60–65], which impose a delay to compensate the voltage unbalance, and 2) gate current control [45, 52–59, 66, 67], where the gate current is modulated to control the switching speeds of the devices achieving dynamic voltage balancing. The current can be modulated directly by controlling the gate control current, or by controlling the gate resistances or gate voltages.

However, as can be seen in Figs. 5.1-5.2, the existing methods result in different switching losses for the stacked devices, which increases reliability and thermal management issues. In Figs. 5.1-5.2, in addiction to the $V_{ds}$ delay at the beginning of switching transition, it is supposed that the devices have different switching speeds.

As shown in Fig. 5.1, if the time-delay control technique is employed the voltage unbalanced can be reduced. However, different switching speeds are still present, since the devices still have different switching time constants.

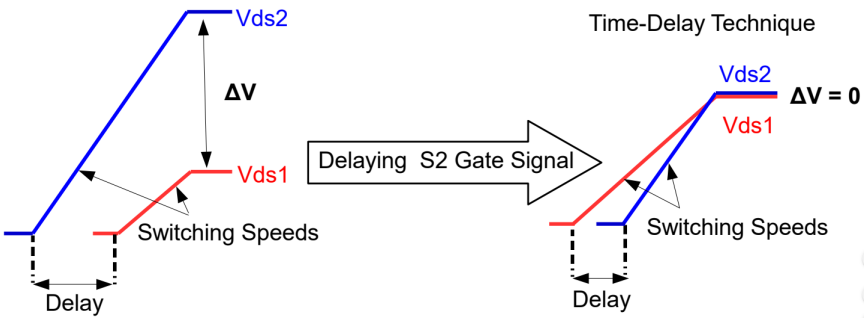



**Fig. 5.1.** Classical time-delay control technique.

In active gate current techniques the switching speeds of the devices are modified to achieve good voltage sharing among the devices. However, as shown in Fig. 5.2, the devices necessarily have different switching speeds, since the delay between the gate signals are not eliminated, which generates a delay on the $V_{ds}$ voltage rising, and consequently different

switching speeds among the series-connected SiC-MOSFETS.

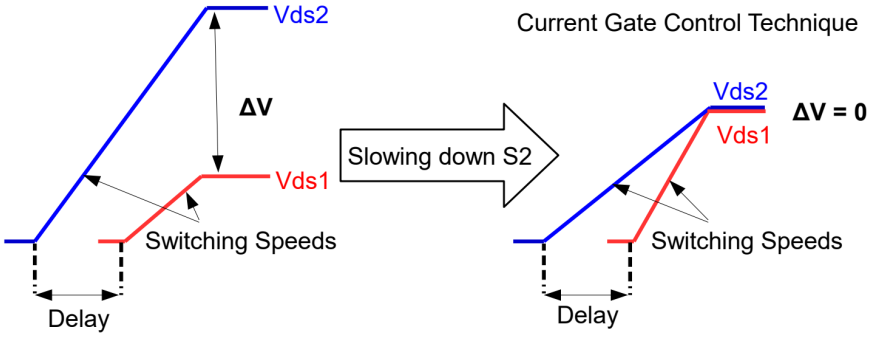



**Fig. 5.2.** Classical active gate current driver technique.

Therefore, to simultaneously balance the voltages across the series-connected SiC-MOSFETs and achieve similar switching losses, a novel active gate driver with a double active control composed by a time-delay control and a variable gate source voltage control is proposed in this chapter.

## 5.2 A Novel Active Gate Driver with a Double Active Control

The concept of the proposed active gate driver is shown in Fig. 5.3. The main idea is to use the delay and switching speed information to generate proper driving signals for the AGD in order to balance the voltages across the devices. To simplify the analyses, only the turn-off transient of two series-connected SiC devices is taken into account.

In a first step, the $V_{ds}$ voltages of the series-connected devices are compared to the same voltage reference that represents the beginning of the MOSFET switching transition ($V_d*$). For this stage, one comparator is used for each device. If the output comparators generate signals at different times, a delay will be detected and compensated by the time-delay control.

In the same way, the $V_{ds}$ voltages of the series-connected devices are compared to another voltage reference that represents the end of the MOSFET switching transition ($V_s*$). For this stage, one comparator is used for each device. If the output comparators generate signals at different times, a mismatch between the switching speeds of the devices will be detected and the variable gate source voltage will be adapted to speed-up or slow-down the switching speed devices by increasing or decreasing the turn-off gate drive voltage. Therefore, the delay between the $V_{ds}$ voltages and the difference on switching speeds of the devices will be eliminated, balancing the voltage among the stacked devices. The information about the delay and switching speed are acquired in a period N and the active gate driver acts in the period N+1.

The proposed method also takes into account the following cases:

- The voltages across the devices are unbalanced and device S1 does not reach the voltage reference $V_s*$. It implies that device S2 switches faster than S1. In this case, the turn-off gate drive voltage is increased to speed-up the S1 switching transition.
- The voltage across the devices are unbalanced and device S2 does not reach the voltage reference $V_s*$. It implies that device S1 switches faster than S2. In this case, the turn-off gate drive voltage is decreased to slow-down the S1 switching transition.
- The voltage across the devices are unbalanced and both S1 and S2 do not reach the voltage reference $V_s*$. This case is not possible since the voltage reference $V_s* < \frac{V_{bus}}{2}$, and the relation $V_{bus} = V_{s1} + V_{s2}$ is naturally satisfied.

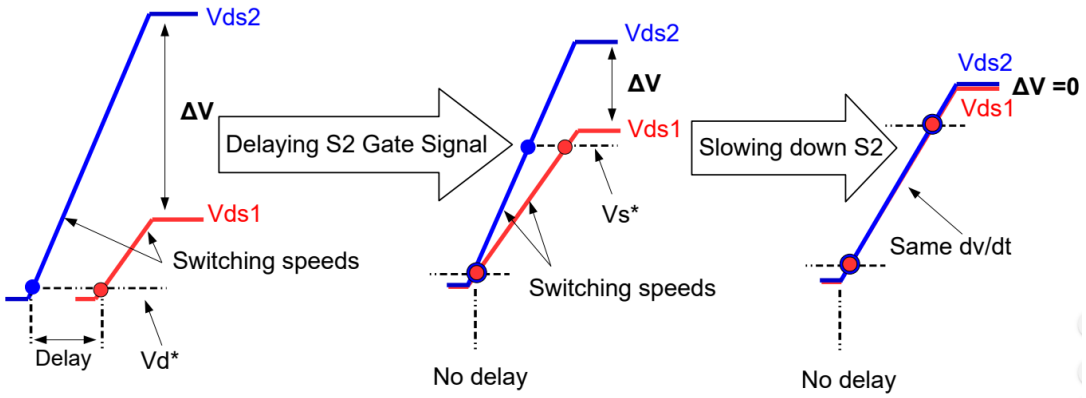



**Fig. 5.3.** Proposed active gate driver concept.

The proposed AGD is described in Fig. 5.4. The network circuits formed by $R_1$, $R_2$, $C_1$ and $C_2$ are used to measure the $V_{ds}$ voltages. The sampled voltages are compared to the reference voltages by using two comparators that are used for each device in order to acquire the switching speed and delay information. These data are sent to a Field Programmable Gate Arrays (FPGA), which generates the proper delay and variable gate source voltage commands, balancing the voltages across the series-connected SiC-MOSFETs.

### Delay Line

The FPGA is not suitable to generate the appropriate delay since the widely used clock frequencies for digital circuits including DSPs and FPGAs are in the range of 10-100 MHz; hence, the minimum control cycles have durations of greater than 10 ns. In this case, due to the faster switching speeds of the series-connected SiC-MOSFETs, the timing delay control requires a high bandwidth capable of adjusting $V_{ds}$ delay timing in the nanosecond range. Therefore, to control the gate delay time to less than 1 ns, a digital delay line must be used in the gate drive circuit. The used delay line IC can be a DS1023 8-bit programmable timing element that can generate delay steps of 250 ps [103]. Therefore, after the delay information

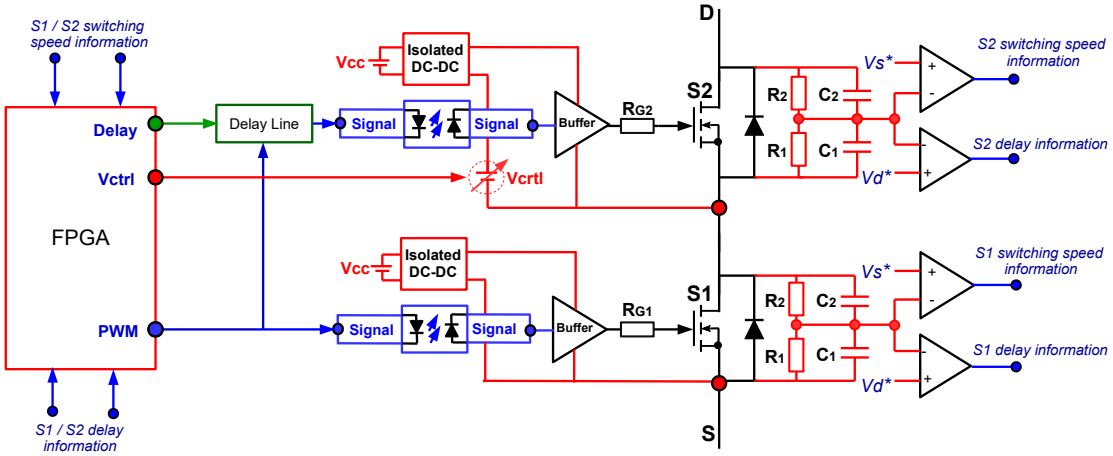



**Fig. 5.4.** Active gate driver with a double active control.

processing by the FPGA, the delay line is programmed into the cycle N to generate the proper delay for the cycle N+1.

### Switching Speed Control

Since different $dv/dt$ methodologies have different control variables, it is necessary to study how these variables affect the switching transient and quantify their effect on the switching speed. Focusing on the turn-off switching transition as shown in Fig. 5.5, four time intervals can be observed. During time interval 2, which corresponds to the Miller plateau in the gate voltage waveform, the $V_{ds}$ voltage rises from $R_{DS(on)}.IL$ to its final value . The drain current of the device remains unchanged [22, 23]. This is the most important time interval to control the $dv/dt$ of the series-connected devices. During time-interval 2, the $dv/dt$ can be approximately calculated with Eq. (5.1) [104, 105].

$$\frac{dv}{dt} = \frac{I_{g2}}{C_{gd}} = \frac{V_{miller} - V_{droff}}{C_{gd}R_g + (C_{ds} + C_{gd})/2g_{fs}} \tag{5.1}$$

Where $I_{g2}$ is the average gate current during time interval 2, $C_{gd}$ and $C_{ds}$ are, respectively, the gate-drain and drain-source device capacitances, $V_{miller}$ is the Miller voltage, $V_{droff}$ is the gate drive voltage for the turn-off transition, $R_g$ is the gate resistance and $g_{fs}$ is the transconductance.

In Eq. (5.1), all the controllable variables are marked in red. In other words, the $dv/dt$ can be controlled by $C_{gd}$, $V_{droff}$ or $R_g$. In this work, $V_{droff}$ is chosen to control the slew rate of devices due its simplicity of implementation. The variable gate voltage method consist in adjusting the gate voltage during the switching transient to control its trajectory. It has gained attention since its working principle is closely related to conventional gate drive methods. The advantage of this method over the variable resistance and variable current

source methods is the flexibility due to easier control of the voltage level. Different topologies for the variable gate voltage AGD methods are proposed in [101, 104–107].

During the control process, after the switching speed information processing by the FPGA, which controls the variable source voltage $V_{ctrl}$, the devices are slowed-down or speeded-up by modifying $V_{droff}$. It is important to note that the modification of $V_{droff}$ is done only during the switching transition ($V_{ds}$ rising). When $V_{ds}$ reaches its final value, $V_{droff}$ is set to its initial value. If $V_{droff}$ remains at its new value, it could generate false triggering.

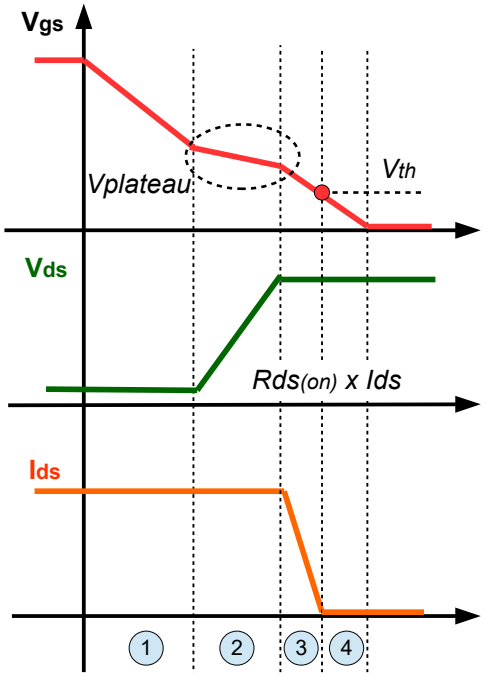



**Fig. 5.5.** Ideal turn-OFF process for SiC-MOSFETs.

### RC Voltage Divider

The network RC circuit used to sample the $V_{ds}$ voltages across the devices is shown in Fig. 5.6. It is formed by $R_1$, $C_1$, $R_2$ and $C_2$. $C_C$ is the comparator input capacitance. The resistor $R2$ is selected in terms of the maximum drain voltage, and resistor $R_1$ is selected to feature the desired gain. At the measurement point across $R_1$, a capacitor ($C_1$) is placed to buffer the measured value and remove its high frequency components. However, the addition of $C_1$ and the input parasitic capacitance $C_C$ of the comparators creates an RC circuit that can result in a very low-bandwidth measurement (several microseconds to reach steady state). For example, for a desired gain of 1/333, which correspond for example to $R_1$ = 1 kΩ and $R_2$ = 0.33 MΩ, and selecting $C_1 = 1\ nF$, the RC circuit step response that is simulated with LTspice is shown in Fig. 5.7. As can be seen, the time that the RC circuit takes to reach the steady state is approximately 5 $\mu$s. If $V_d*$ and $V_s*$ are set to 10% and

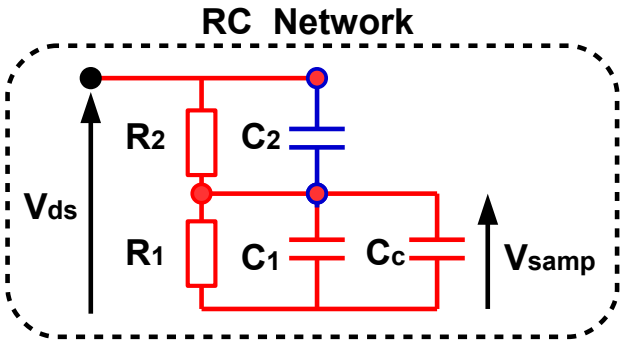



**Fig. 5.6.** RC network circuit.

90% of $\frac{V_{bus}}{2}$, it will result delays on the switching speed and delay information of 2 and 0.2 $\mu$s, respectively. Therefore, this measurement is not suitable for fast data acquisition.

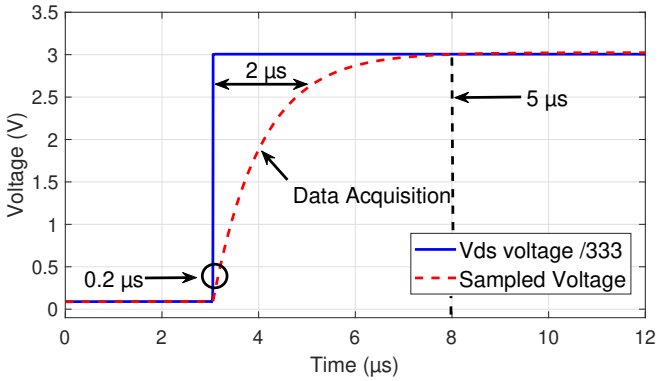



**Fig. 5.7.** Delay on the RC circuit response.

To solve this problem, $C_2$ is added on the RC circuit to create a high-bandwidth measurement, compensating the low-bandwidth measurement caused by $R_1$, $R_2$ and $C_1$. However, $C_2$ has to be well designed. If $C_2$ is very small, it can not compensate the effects of $C_1$ and $C_c$, achieving a similar response to that in Fig. 5.7. If $C_2$ is oversized, it can generate undesirable voltage spikes as shown in Fig. 5.8 for $C_2 = 1\ nF$. Furthermore, it also takes a long time to reach the steady state.

Fig. 5.9 shows RC circuit step response for the proper $C_2$ value (3 $pF$). As can be seen, no noticeable delay is introduced on switching speed and delay information. In high frequency applications, the RC network designing has more and more importance since if $C_2$ is undersized or oversized, the sampled voltage may not reach its steady state. The value of $C_2$ has to be chosen as a function of other RC network elements, i.e., $R_1$, $R_2$ $C_1$, $C_C$. Therefore, each case has to be analysed individually.

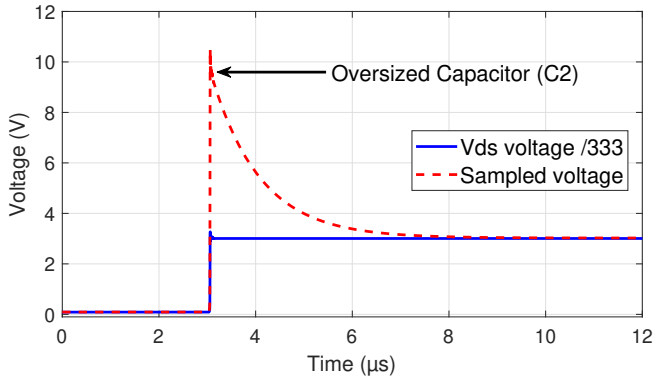



**Fig. 5.8.** RC circuit response when $C_2$ is oversized.

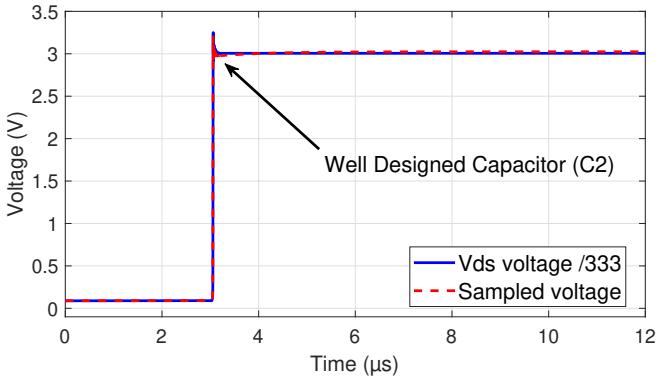



**Fig. 5.9.** Ideal RC circuit response.

### Delay and Switching Speed Control Strategies

To compensate the $V_{ds}$ delay and switching speed mismatch between the series-connected SiC-MOSFETs, a simple control strategy is proposed in this work as shown in Fig. 5.10, which is divided into two control blocks, i.e., the delay control strategy and the $dv/dt$ control strategy.

In a first step, the $V_{ds}$ voltages of both devices are sampled and compared to a specific voltage reference $(0.1 * V_{bus}/2)$, which represents the beginning of switching transition. When the $V_{ds}$ of device $SA$ reaches $0.1 * V_{bus}/2$, the output comparator $OA1$ switches from low to high, indicating the beginning of switching transition of device $SA$. In the same way, when the $V_{ds}$ of the device $SB$ reaches $0.1 * V_{bus}/2$, the output comparator $OB1$ switches from low to high. The signals provided by the comparators indicate to the FPGA the delay between the switching transition ($\Delta t1$) of the series-connected devices. When $\Delta t1 = 0$, which means that the devices start their switching transitions at the same time, the delay control does not act. When $\Delta t1 < 0$, it means that device $SA$ starts switching before than $SB$. Therefore, the delay control imposes a fixed $+Delay$ to $SB$ gate signal. When $\Delta t1 > 0$, this is the opposite, and the delay control imposes a fixed $-Delay$ to $SB$ gate signal. This delay step is incremented or decremented till $\Delta t1 = 0$.

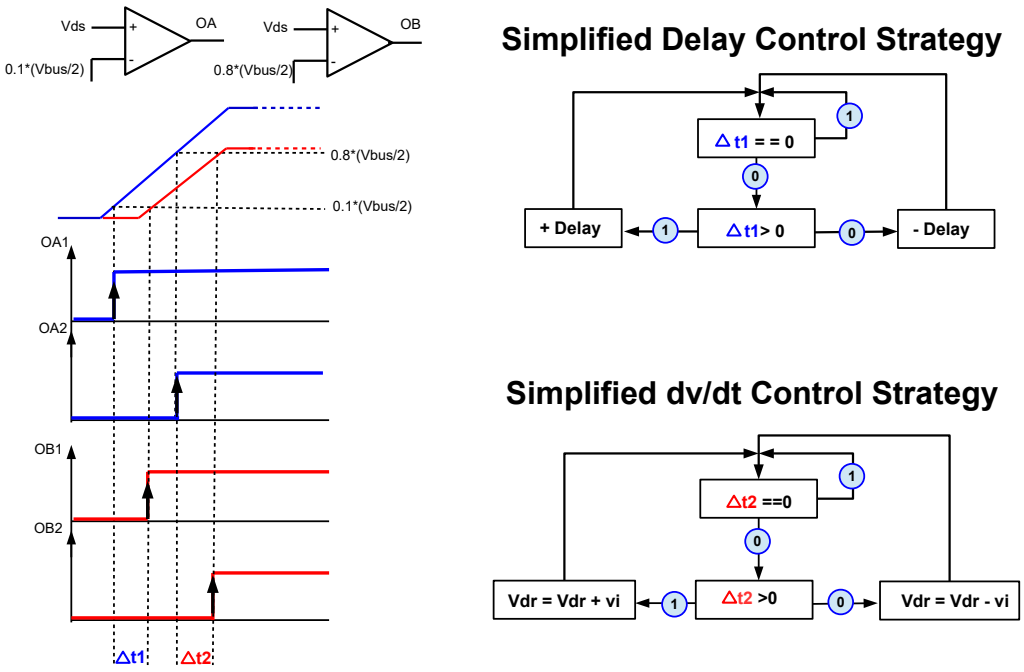



**Fig. 5.10.** Delay and $dv/dt$ control strategies.

The $dv/dt$ control strategy is similar. The $V_{ds}$ voltages of both devices are sampled and compared to a specific voltage reference $(0.8 * V_{bus}/2)$, which represents the ending of switching transition. When the $V_{ds}$ of device $SA$ reaches $0.8 * V_{bus}/2$, the output comparator $OA2$ passes from low to high, indicating the ending of switching transition of the device $SA$ (same ofr $SB$). The signals provided by the comparators indicate to the FPGA the mismatch between the device switching speed ($\Delta t2$) of the series-connected devices. When $\Delta t2 = 0$, which means that the devices end their switching transitions at the same time, the $dv/dt$ control does not act. When $\Delta t2 < 0$, it means that the device $SA$ is faster than $SB$. Therefore, the $dv/dt$ control increments the turn-off drive voltage ($V_{dr}$) of $SB$ by a fixed voltage step ($+v_i$). When $\Delta t2 > 0$, the $dv/dt$ control decrements the turn-off drive voltage ($V_{dr}$) by a fixed voltage step ($-v_i$), which is incremented or decremented till $\Delta t2 = 0$.

### Electrical Transient Simulations and Dynamic Voltage Balancing

To validate the theoretical approach, electrical simulations are made in Simulink/Matlab software. Two MOSFET surface-potential-based models are used to perform the simulations. The surface-potential-based model provides a greater level of model fidelity than the simple square-law (threshold-voltage-based) models. The surface-potential-based model includes the following effects:

- Fully non-linear capacitance models (including the non-linear Miller capacitance).
- Charge conservation inside the model, so the model can be used for charge sensitive

simulations.

- Velocity saturation and channel-length modulation.
- The intrinsic body diode.
- Reverse recovery in the body diode model.
- Temperature scaling of physical parameters.
- Dynamic self-heating, i.e., the effect of self-heating on the electrical characteristics of the device is taken into account.

The model is a minimal version of the world-standard Parameter Space Partitioning (PSP) model proposed in [108]. The PSP model parameters can be extracted from the data-sheet of a specify device. In this work, the SiC-MOSFET C2M0160120 (1200V, 19A) data-sheet parameters are used.

Two series-connected devices are used to validate the theoretical approach proposed in this chapter. The main parameters used in the simulations are : bus voltage of 1000V and a load current of 20A. In addiction to a delay of 2 $ns$ between the gate signals, to simulate different switching time constants, different gate resistances ($R_{g1}$ = 20 Ω and $R_{g2}$ = 18 Ω) and different gate drive voltages for turning-off ( $V_{droff1}$ = -4 V and $V_{droff2}$ -5V) are used.

Fig. 5.11 shows the voltage sharing behaviour for two series-connected SiC-MOSFETs without any control balancing technique. As can be seen, the voltage unbalance drastically increases with the load current ($IL$), which can damage the power devices when no balancing technique is applied.

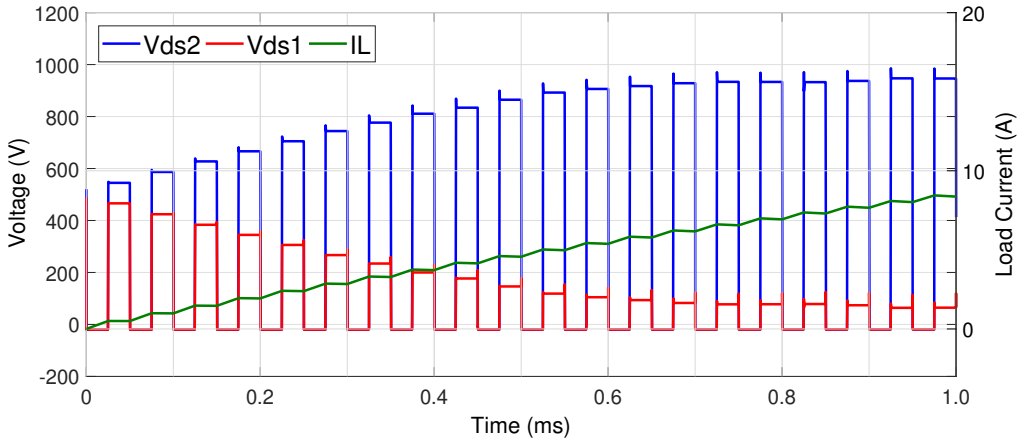



**Fig. 5.11.** Simulation result of voltage sharing performance without AGD control technique.

Fig. 5.12 shows the simulation results when the control strategies shown in Fig. 5.10 is applied, where the following control parameters are used: fixed step $Delay$ = 0.1 $ns$ and

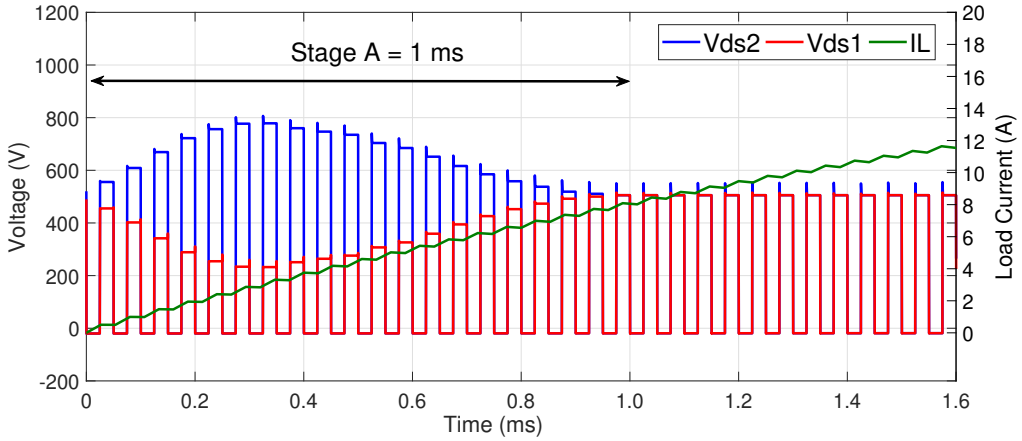



**Fig. 5.12.** Simulation result of voltage sharing performance with th proposed AGD control technique when $Delay = 0.1\ ns$ and $v_i$ =0.1 $V$.

fixed step drive voltage $vi = 0.1\ V$. As can be seen, after a period of 1 $ms$, the $V_{ds}$ voltages across the devices are perfectly balanced. During the Stage A, the control strategies try to compensate the switching dynamic behaviours of the devices. However, the device switching speeds are directly proportional to the load current, which increases the impact of $\Delta t1$ and $\Delta t2$ on the voltage balancing. When $\Delta t1$ and $\Delta t2$ start to tend towards zero, the control strategies are predominant, and the $V_{ds}$ voltages start to be balanced regardless of $IL$. The control strategies are easy to implement and provide good voltage sharing performance. However, the time to reach an acceptable voltage balance depends on the values of $Delay$ and $v_i$. If the parameter values are too small, the convergence time can be slow as shown in Fig. 5.12.

Increasing the values of $Delay$ and $v_i$ can reduce the time to reach an acceptable voltage sharing performance. However, if the they values are too large, the control may not converge as shown in Fig. 5.13, where a $Delay$ of 0.5 $ns$ and a $v_i$ of 0.5 $V$ are used.

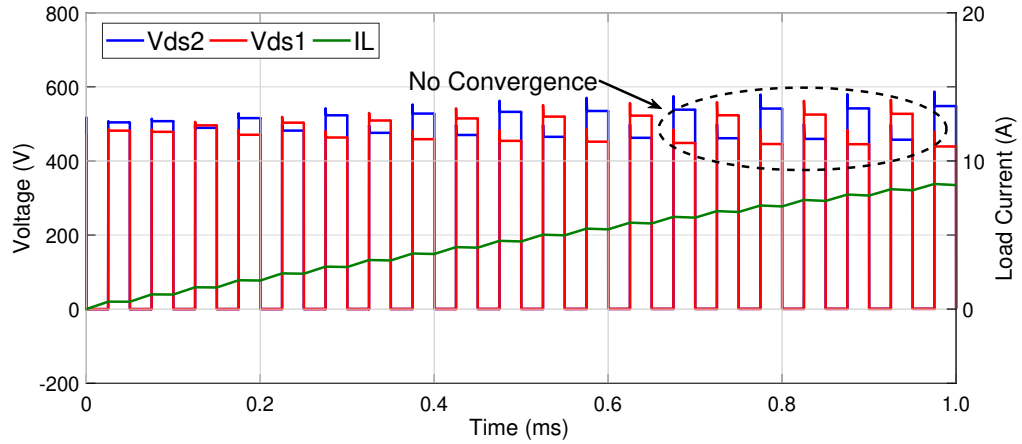



**Fig. 5.13.** Simulation result of voltage sharing performance with th proposed AGD control technique when $Delay = 0.5\ ns$ and $v_i$ =0.5 $V$.

Fig. 5.14 shows the voltage sharing performance for a *Delay* of 0.25 $ns$ and a $v_i$ of 0.25 $V$. In this case, a better voltage balancing performance is achieved when compared to the first case ($Delay = 0.5\ ns$ and $v_i = 0.5\ V$). The time to reach an acceptable voltage balancing is reduced to 0.4 $ms$.

The performance of *delay* and $dv/dt$ controls can be improved by other control techniques, such as PI controllers. PI control techniques may provide a better performance in terms of stability and convergence speed. However, this kind of method is more complex than the simple technique presented in this section. In any case, the simulation results shown in this chapter demonstrate the interest of the proposed AGD even under a simple control technique.

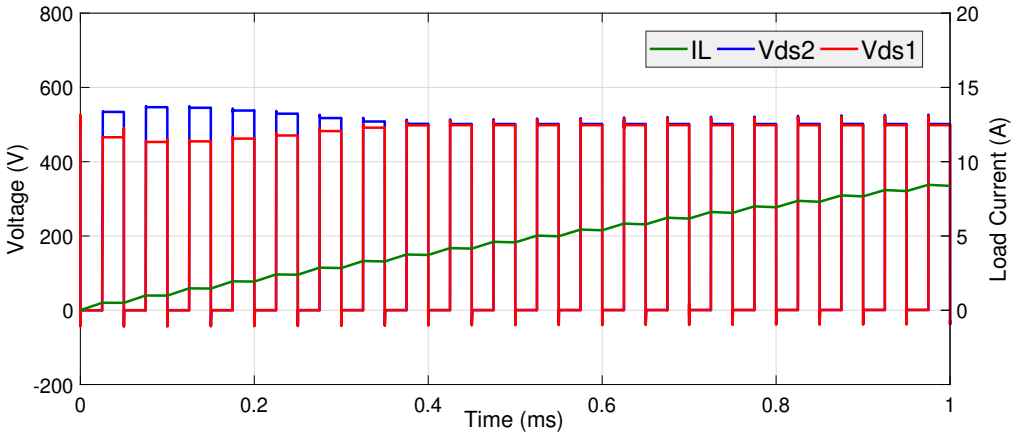



**Fig. 5.14.** Simulation result of voltage sharing performance with th proposed AGD control technique when *Delay* =0.25 $ns$ and $v_i$ =0.25 $V$.

## 5.3 Conclusion

In this chapter, a novel concept of active gate driver for series-connected SiC-MOSFETs was introduced. The proposed AGD is composed by two functionality controls, which can balance the voltages across the devices by controlling the $V_{ds}$ voltages and mitigating the delay between them at the beginning of switching transition. The originality of the proposed AGD is perfect dynamic synchronization between the voltages across the devices in the stack, which reduces thermal and reliability problems since the devices will switch with the same dynamic behaviour, generating identical switching losses per device. The proposed idea was validated by electrical simulations. The experimental set-up remains as an expectation of future works for the author or for new doctoral students who wish to contribute with the topic of series-connected devices.

# Conclusions and Perspectives

## Conclusion

In this work, new gate drive power supply configurations and a novel multi-step packaging concept are investigated in order to increase the performance of series-connected SiC-MOSFETs in terms of voltage balancing conducted EMI common mode current and switching speed. Furthermore, a novel concept of active gate driver for series-connected SiC-MOSFETs is proposed.

In chapter 2, a comprehensive overview of series-connected SiC-MOSFETs is presented. The factors that can influence the voltage sharing performance and the existing voltage balancing techniques are discussed. It is clarified that some conventional voltage balancing methods used for series-connected Si-IGBTs/Si-MOSFETs, especially the active gate control techniques, are not longer suitable for SiC devices since the switching transition of SiC devices can be completed in a few nano-seconds. This requires new circuit designs and control strategies.

In chapter 3, new gate drive power supply configurations are proposed in order to reduce EMI issues. The proposed gate drivers demonstrate considerable conducted EMI reduction when applied for four 1.2 kV series-connected devices. The EMI reduction reaches 9-21dB, depending on the frequency range and gate driver architecture. Furthermore, the cascaded gate drive power supply configuration demonstrates a considerable improvement on the switching speed of the series-connected power devices. The $dv/dt$ of the middle point switching cell is boosted by 12-41%, depending on the load current. The experimental results shown in chapter 3 confirms the effectiveness of the new gate drive power supply configurations in terms of EMI reduction and switching speed. The main drawback of the proposed gate drivers is the increased complexity, volume and the additional power consumption due to the cascaded power supplies. This problem can be aggravated when the number of devices in the stack is increased. The proposed gate drivers must be designed carefully since their power ratings change from one to another, especially for the first gate drive power supply, which must be designed to power other drive circuits.

In chapter 4, a novel Multi-Step Packaging (MSP) concept is proposed. The MSP demonstrates voltage sharing performance between two 1.2 kV series-connected SiC-MOSFETs under 1 kV total bus voltage. The steady-state difference between the $V_{ds}$ voltages remains within 3% under different load conditions (0-40 A). Furthermore, the proposed MSP also demonstrates an excellent voltage sharing performance at light loads ($< 700\ mA$). At light loads the switching speed is drastically reduced (compared to high load currents). Therefore, mismatches between device parameters, gate signals delay, etc. have less and less

impact on the voltage balancing. Furthermore, the proposed technique can be applied in conjunction with other voltage balancing methods. The author believes that the proposed packaging can be applied as a preventive solution. In this case, when the proposed MSP is applied in conjunction with clamp circuits or active gate control techniques, less stress on the passive devices and less switching losses will be present. However, this assumption must be analysed in future works. The main drawback of the MSP concept is that, the voltage sharing performance of the proposed MSP is limited by the gate signal delay and mismatch between device characteristics, which should remain at considerably low levels. Otherwise, the proposed packaging concept may not ensure a good voltage balancing across the series-connected devices, specially at heavy loads. The complexity of implementation in industrial processes and the thermal management issues are other drawbacks relates to the proposed MSP. However, from a thermal point of view, and as quickly discussed in chapter 4, if the additional dielectric layers of the proposed packaging have small thermal resistances, such as those provided by $AlN$ and $Al_20_3$ materials, the thermal management issues remain similar that those present in the classical planar packaging.

In chapter 5, a novel concept of active gate driver (AGD) is proposed. The AGD is composed by a double active control, which can balance the voltages across the devices by controlling the $V_{ds}$ switching speeds and mitigating the delay between them at the beginning of switching transition. The originality of the proposed AGD is the perfect dynamic synchronization between the voltages across the devices in the stack, which reduces thermal and reliability problems since the devices will switch with the same dynamic behaviour, generating identical switching losses per device. The proposed idea was validated by electrical simulations. The experimental set-up remains as an expectation of future works for the author or new doctoral students who wish to contribute with the topic of series-connected devices.

# Perspectives

The work presented in this thesis opens many possibilities of new ideas and improvements. The new gate driver configurations, the multi-step packaging concept and the proposed active gate driver, all have some elements to be investigated and optimized:

### New Gate Driver Architectures

- The new gate driver configurations should be compared to the traditional one in terms of gate driver power consumption, efficiency, cost, volume and reliability. None of these aspects are investigated in this work.
- More experiments must be implemented to fully investigate the gate driver configura-

tions in order to meet EMI standards for power electronics systems.

- A detailed study about the impact of gate drive power supply configurations on voltage sharing performance must be investigated. This work demonstrates (in a brief discussion) that the new configurations of gate driver architecture can reduce the voltage balancing problems. Therefore, a detailed study could find a novel gate driver architecture that further reduces the voltage unbalancing across the devices.

**Novel Multi-Step Packaging**

- The MSP concept proposed in this work should be deeply investigated. A thermal modelling would be interesting for thermal analyses. In this work, it is proposed a new concept of packaging that can considered as a starting point for more investigations.
- The EMI performance of the proposed MSP package should be investigated. May be the MSP package can also reduce the EMI issues since when compared to the traditional planar package, the parasitic capacitances are drastically modified. The drain to ground parasitic capacitances in traditional planar packages, are now relocated in the MSP package, i.e., they are located between drain and source terminal of devices. This can impact the EMC performances of the switching cell.
- More experiments must be implemented to fully investigate the MSP package in order to analyse switching losses, EMI, etc.
- A detailed study about thermal management has to be performed since the MSP package introduces non homogeneous propagation paths for the heat flux from each device to ambient.
- The MSP should be experimentally investigated in conjunction of other voltage balancing techniques, such as clamp circuits and active control methods. Voltage sharing performance, switching losses , and stress on the passive components have be investigated. Therefore, a comparison with the traditional planar package can be done.

**A Novel Active Gate Driver**

- The AGD proposed in this work has yet to be experimentally investigated. According to the analysis of existing solutions, the idea introduced in this work is novel. However, it was validated only by simulation results. The proposed AGD may present a considerable complexity of implementation since $V_{ds}$ voltages are measured during the turn-on/turn-off transitions. It implies to adapt active gate drive techniques to such switching speeds in the range of 10 $V/ns$ - 100 $V/ns$ induced by SiC-MOSFETs. The

circuit schematics, the components bandwidth, the control strategy as well as timing strategy should be carefully designed.

# Chapter 6
# Résumé en Français

## 6.1 Introduction

La transition énergétique avec l'intégration au réseau des ressources énergétiques distribuées entraîne de nouveaux défis pour la production, la transmission et la distribution d'électricité. Par conséquent, le réseau moyenne tension et les applications en courant continu haute tension (High-Voltage Direct Current - HVDC) deviennent de plus en plus importants. Les convertisseurs haute-tension et moyenne-tension ont un grand potentiel pour une grande variété d'applications, telles que le courant continu haute tension (HVDC), le courant continu moyenne tension (Medium-Voltage Direct Current - MVDC), smart / super / micro-réseau, variateurs de vitesse pour moteurs asynchrones et synchrones, générateurs d'impulsions moyenne tension pour applications plasma, etc [1].

La caractéristique commune des applications mentionnées est la recherche pour maximiser l'efficacité et la capacité de puissance de sortie de ces systèmes, ce qui peut être réalisé soit en augmentant la tension de blocage des semiconductuers de puissance soit en augmentant la tension de sortie du convertisseur. A cette fin, des progrès dans les domaines de la technologie de l'électronique de puissance tels que les semi-conducteurs et les topologies de convertisseur ont été étudiés pour augmenter la tension de blocage, la densité de puissance et l'efficacité, ce qui peut réduire le coût global du système et la consommation d'électricité.

Les semiconductuers connectés en série et les topologies de convertisseur à plusieurs niveaux sont deux moyens efficaces d'atteindre une tension plus élevée avec des semiconductuers à basse tension. Les topologies à plusieurs niveaux offrent des fonctionnalités exceptionnelles telles qu'une faible tension en mode commun, une faible contrainte $dv/dt$ et des interférences électromagnétiques propagées plus faibles [5]. D'autre part, l'utilisation de semi-conducteurs individuels en série se traduit par des coûts inférieurs et une efficacité plus élevée. Selon l'étude présentée en [6], l'utilisation de deux ou plus semi-conducteurs en série présente une meilleure résistance à l'état passant et une densité de courant plus élevée que l'utilisation d'un seul semi-conducteur avec la même tension de blocage.

## 6.2 Motivation et objectifs de la recherche

Basé sur les motivations et les défis technologiques mentionnés, ce travail propose une étude complète de nouvelles solutions pour résoudre les principaux problèmes liés à la mise en série de MOSFET SiC pour les applications dites "moyenne tension".

Afin d'étudier la viabilité et l'efficacité d'une topologie de convertisseur à base de MOSFETs SiC connectés en série, l'un des objectifs de ce travail est de proposer, développer et tester des solutions passives naturelles, telles que de nouvelles configurations d'alimentation de commande rapprochée et des nouveaux concepts de packaging. Au final, cette recherche propose une nouvelle méthode d'équilibrage actif afin de compenser les dernières imperfections et les variations paramétriques des solutions passives. Pour étudier les méthodes passives et actives proposées dans ce travail, l'équilibrage de tension, la réduction du courant de mode commun et les performances de vitesse de commutation sont analysées expérimentalement jusqu'à quatre MOSFET SiC (1,2 kV) en série sous une tension de blocage totale de 1 kV.

## 6.3 Organisation de la thèse

Sur la base des objectifs de recherche décrits ci-dessus, cette thèse est organisée comme suit:

**Chapitre 2**: il est présenté un aperçu complet des MOSFET SiC connectés en série. Les facteurs qui peuvent influencer les performances de partage de tension et les techniques existantes d'équilibrage de tension sont présentés.

**Chapitre 3**: de nouvelles configurations d'alimentation de commande rapprochée sont analysées afin de minimiser les courants conduits en mode commun dans les applications à haute vitesse de commutation. De plus, une nouvelle configuration de commande rapprochée est proposée afin d'augmenter la vitesse de commutation en tension ($dv/dt$) du point milieu de la cellule de commutation.

**Chapitre 4**: deux nouveaux concepts de packaging pour les MOSFETs SiC connectés en série sont analysés. La capacité parasite générée par les matériaux isolants des packages a un impact significatif sur le comportement dynamique de la cellule de commutation, ce qui impacte les performances d'équilibrage de tension.

**Chapitre 5**: un nouveau driver actif est introduit. La commande rapprochée proposée est basée sur l'analyse de l'état de l'art présentée au chapitre 2. La proposition est validée par des simulations numériques. Quelques aspects pratiques sont ensuite proposés pour aller vers les vérifications expérimentales.

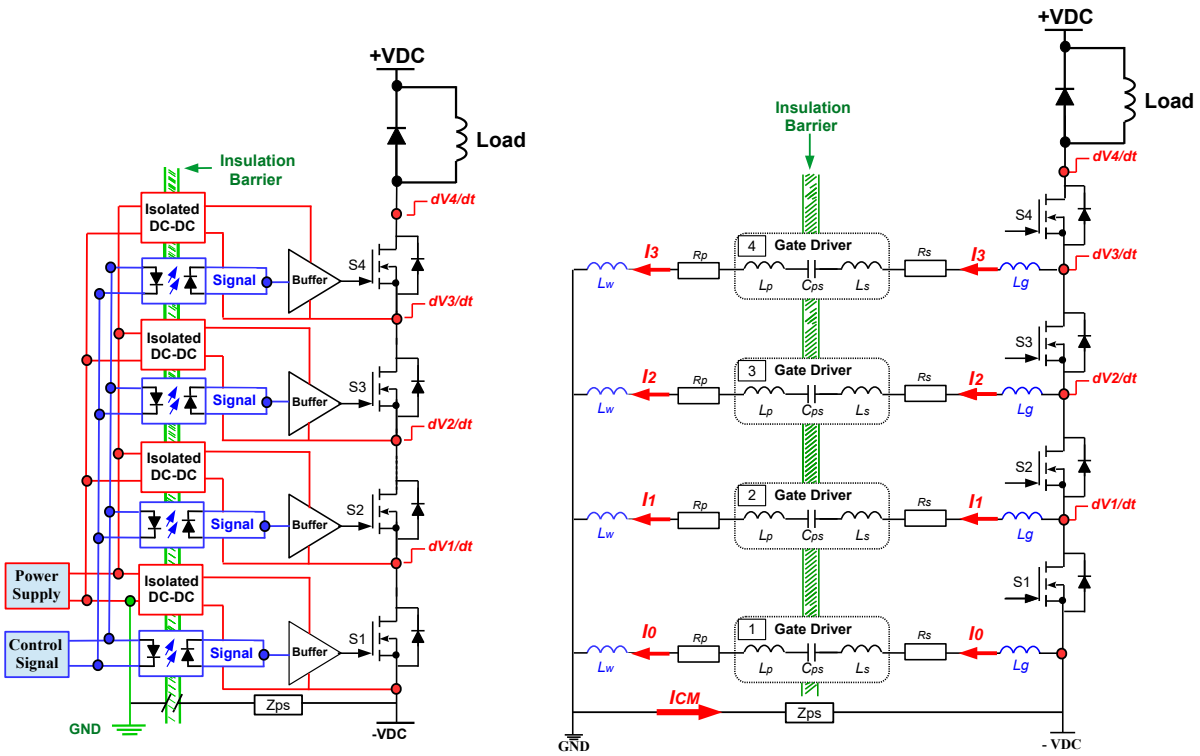
## 6.4 L'état de l'art: MOSFET SiC Connectés en Série

Au chapitre 2, un aperçu complet des semi-conducteurs connectés en série est présenté. Les principes fondamentaux du MOSFET SiC et de son processus de commutation sont essentiels pour comprendre les principes qui sous-tendent toute disparité de tension naturelle entre les semiconductuers connectés en série. Ensuite, un aperçu des facteurs qui peuvent

influencer les performances de partage de tension et les techniques existantes d'équilibrage de tension sont discutés.

## 6.5 Nouvelles configurations d'alimentation de commande rapprochée

Au chapitre 3, six nouvelles configurations de commande repprocheé sont proposées pour réduire les courants de mode commun qui circulent dans la partie de contrôle de la cellule de commutation. La configuration traditionnelle de commande rapprochée (TGD) est illustrée sur la figure 6.1, où chaque convertisseur DC-DC isolé de la commande est fournie indépendamment par une alimentation externe. Dans cette configuration, il existe quatre sources de perturbation produites par quatre points flottants, où trois d'entre eux sont directement connectés à leurs alimentations (convertisseur DC-DC isolés) qui introduisent des capacités parasites ($C_{ps}$).




**(a)** **(b)**

**Fig. 6.1.** Configuration traditionnelle de commande rapprochée (a) et son schéma électrique (b).

Dans la configuration TGD, les courants de mode commun (CM) produits par les sources $dV/dt$ doivent traverser une barrière d'isolation, qui est modélisée par $C_{ps}$, pour circuler dans la partie commande comme indiqué sur la Fig.6.1(b). Ces courants, quand ils sont élevés, peuvent endommager et perturber le système de commande.

Une solution intelligente pour réduire ces courants CM, consiste à modifier la voie du courant CM en modifiant la configuration de l'alimentation de la commande rapprochée. Une des nouvelles configurations d'alimentation de commande rapprochée est illustrée sur la Fig. 6.2, où les alimentations (DC-DC isolés) sont entièrement en cascade, c'est-à-dire que e convertisseur DC-DC 1 (correspondant au MOSFET S1) est directement alimenté par une alimentation externe connectée à la terre (GND). Le e convertisseur DC-DC 2 est alimenté par e convertisseur DC-DC 1, le e convertisseur DC-DC 3 est alimenté par le e convertisseur DC-DC 2 et lee convertisseur DC-DC 4 est alimenté par le e convertisseur DC-DC 3.

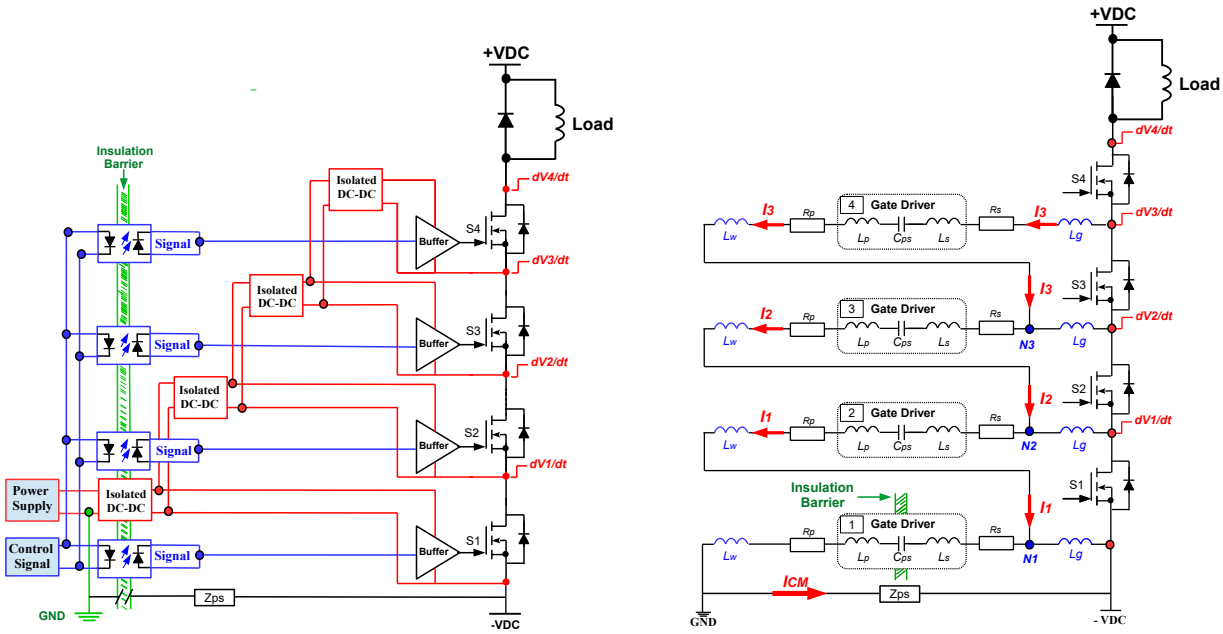



**Fig. 6.2.** Une nouvelle configurations de commande rapprochée (a) et son schéma électrique(b).

Avec cette configuration, les courants de mode cummun produits par les sources $dV/dt$ doivent traverser plus d'une barrière d'isolation pour circuler dans la partie de contrôle. Comme le montre la Fig. 6.2(b), pour circuler dans la partie de contrôle, le courant CM $I_3$ doit traverser quatre barrières d'isolation générées par les quatre DC-DC isolés. Chaque barrière d'isolation fournit une impédance élevée qui force le retour de chaque courant CM vers la partie puissance. Par exemple, en considérant la distribution de courant sur la Fig. 6.3, le courant $I_1$ peut être exprimé comme la somme de $I_{CM}$ plus $I_r$, où $I_r$ est le courant qui revient du côté puissance sans circuler dans la partie commande, et $I_{CM}$ est le courant CM total qui circule côté commande. Le courant $I_1$ a une tendance à circuler par le chemin qui a la plus faible impédance. Deux impédances, $Z_A$ et $Z_B$, sont représentées sur la Fig. 6.3. Par conséquent, si $Z_A + Z_{ps} \approx Z_A >> Z_B$, la majorité du courant $I_1$ reviendra localement à la partie de puissance via l'impédance $Z_B$.

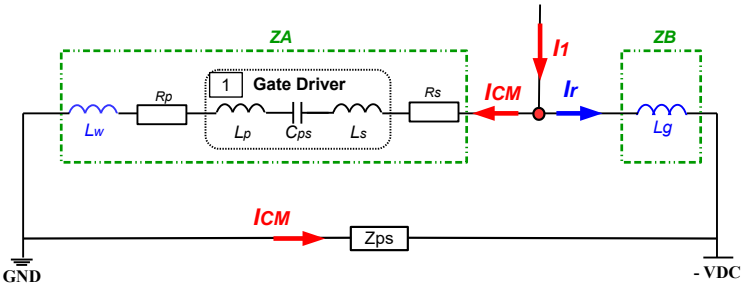



**Fig. 6.3.** Impédance du circuit de la commande rapprochée.

Les résultats expérimentaux montrent des réductions significatives de courants de mode commun. Les plus notables varient entre 9 et 21 dB, en fonction de la plage de fréquences et de la configuration de commande rapprochée.

La configuration illustrée sur la Figure 6.2, c'est un technique efficace pour améliorer la vitesse de commutation des semiconductuers connectés en série. Par rapport à la configuration classique, la configuration proposée peut fournir une augmentation sur la vitesse de commutation de 12 à 41 %, en fonction du courant de charge.

Toutes les approches théoriques sont validées par des résultats de simulation et expérimentaux, qui confirment l'intérêt des nouvelles configurations de commande rapprochée face à la réduction de courant de mode commun et la vitesse de commutation de la cellule de commutation.

Le chapitre 3 ne se concentre pas sur les problèmes d'équilibrage de tension. Cependant, l'impact des nouvelles configurations de commande rapprochées sur les performances de partage de tension est discuté à la fin du chapitre. En général, les nouvelles configurations peuvent également réduire les problèmes d'équilibrage de tension.

Pour une conception optimale, la puissance nominale des convertisseurs DC / DC isolés de la commande rapprochée doit être prise en compte. Les avantages offerts par les nouvelles configurations de commande rapprochée doivent être atténués par la complexité, le volume et la consommation d'énergie supplémentaires dus aux alimentations cascadées. Les configurations proposées doivent être conçues avec soin car leurs puissances varient de l'un à l'autre, spécialement pour le premier DC-DC isolé, qui doit être conçu pour alimenter tous les autres circuits de commande rapprochée.

## 6.6 Un Nouveau Concept de Packaging

Au chapitre 4, il est analysé deux nouveaux concepts de packaging pour réduire le déséquilibre de tension entre les MOSFET SiC connectés en série. Dans un premier temps, les bases et les concepts sont expliqués à l'aide d'une analyse mathématique. Les packagings

proposés sont comparés à la solution planaire classique en termes de déséquilibre de tension des semiconductuers connectés en série. L'étude a été réalisée par des analyses théoriques et expérimentales. Le packaging planaire classique et le nouveau concept de packaging proposés sont illustrés sur les Figures 6.4, 6.5 et 6.6, respectivement.

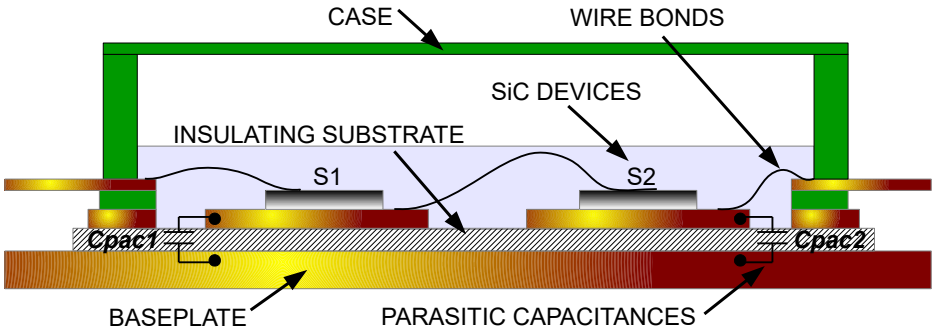



**Fig. 6.4.** Packaging classique.

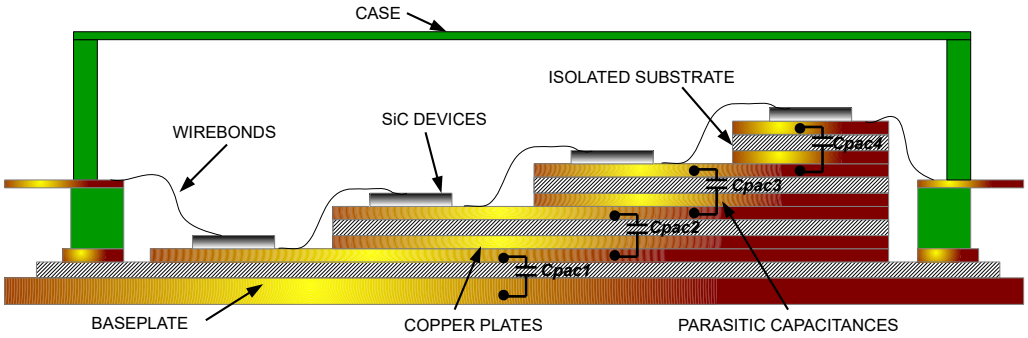



**Fig. 6.5.** Première nouvelle proposition de packaging.

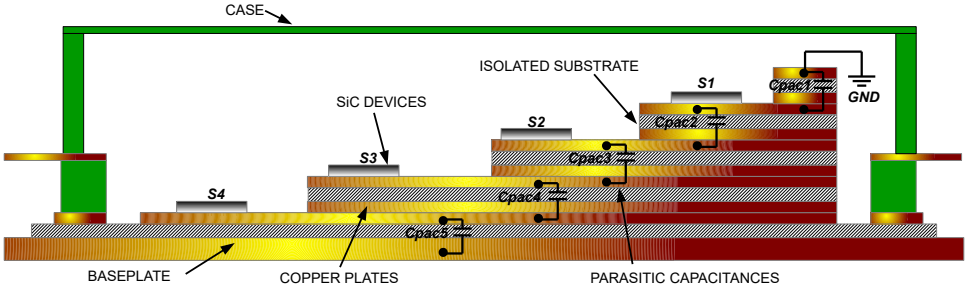



**Fig. 6.6.** Deuxième nouvelle proposition de packaging.

Le premier packaging analysé (Fig. 6.5) montre de meilleures performances que le packaging classique (Fig. 6.4) en termes d'équilibrage de tension et de vitesse de commutation. Cependant, la première proposition ne prend pas en compte les capacités parasites introduites par les circuits de commande de grille. En d'autres termes, ce packaging est plus indiqué pour optimiser l'équilibrage de tension et la vitesse de commutation. De toute façon, cette première proposition valide l'idée que les capacités parasitées du packaging ont un fort impact sur le comportement dynamique des MOSFETs SiC connectés en série.

Basé sur la première proposition de packaging, un deuxième concept est aussi étudié dans le chapitre 4. Le deuxième packaging prend en compte les capacités parasites introduites par le circuit de commande de grille. Comme prévu, parmi les packages investigués, le 2ème package (Fig. 6.6) montre les meilleures performances en termes d'équilibrage de tension et de vitesse de commutation. L'étude demontre que si le délai entre les signaux de grille et les différents caractéristiques entre les composant sont considérablement réduits, le deuxième package peux fournir une performance de partage de tension acceptable sans avoir besoin d'autres techniques d'équilibrage de tension.

Les principaux inconvénients des packagings proposés sont que les performances de partage de tension sont limitées par le retard du signal de grille et la différence entre les caractéristiques des semiconductuers , qui doivent rester à des niveaux considérablement bas. Sinon, le package proposé risque de ne pas garantir un bon équilibrage de tension entre les MOSFET SiC connectés en série. La complexité de la mise en oeuvre dans les processus industriels et les problèmes de gestion thermique sont d'autres inconvénients liés aux packages proposés. Cependant, d'un point de vue thermique, si les couches diélectriques supplémentaires du package ont de petites résistances thermiques, telles que celles fournies par les matériaux $AlN$ et $Al_20_3$, les problèmes de gestion thermique restent similaires à ceux présents dans le package planaire classique.

### 6.6.1 Nouveau Driver Actif

Au chapitre 5, un nouveau concept de driver actif (AGD) pour les MOSFET SiC connectés en série est introduit. L'AGD proposé est composé de deux degrés de liberté de contrôle, qui peuvent équilibrer les tensions entre les semiconductuers en contrôlant les tensions $V_{ds}$ et en atténuant le retard entre eux au début de la transition de commutation. L'originalité de l'AGD proposé, c'est une synchronisation dynamique entre les tensions aux bornes des MOSFETs, ce qui réduit les problèmes thermiques et de fiabilité puisque les semi-conducteurs commutent avec le même comportement dynamique, générant des pertes de commutation identiques par composant.

Le concept du driver actif (AGD) est illustré sur la Fig. 6.7. L'idée principale est d'utiliser les informations de retard entre les commutations des semiconductuers et de la vitesse de commutation pour générer des commandes appropriées pour l'AGD afin d'équilibrer les tensions aux bornes des MOSFETs SiC.

Dans une première étape, les tensions $V_{ds}$ des semiconductuers connectés en série sont comparées à la même référence de tension qui représente le début de la transition de la commutation ($V_d*$). Pour cette étape, un comparateur est utilisé pour chaque MOSFET. Si les comparateurs génèrent des signaux à des moments différents, un retard sera détecté et compensé par la commande de temporisation.

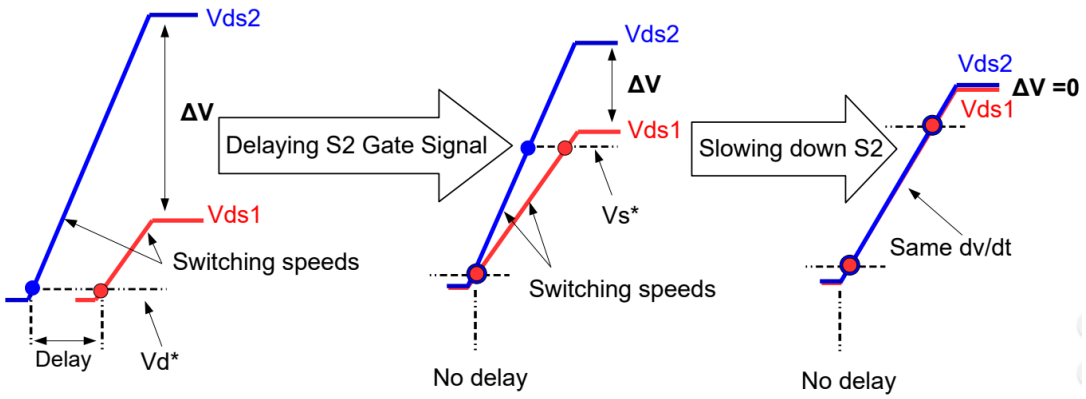



**Fig. 6.7.** Concept du driver actif proposé.

De la même manière, les tensions $V_{ds}$ des semiconductuers connectés en série sont comparées à une autre référence de tension qui représente la fin de la transition de commutation ($V_s*$). Pour cette étape, un comparateur est utilisé pour chaque MOSFET. Si les comparateurs génèrent des signaux à des moments différents, une différence entre les vitesses de commutation des MOSFETS sera détectée et la tension de la commande rapprochée sera adaptée pour accélérer ou ralentir la vitesse de commutation des semiconductuers en augmentant ou en diminuant la tension grille-source des MOSFETs. Par conséquent, le délai entre les tensions $V_{ds}$ et la différence sur les vitesses de commutation seront éliminés, équilibrant la tension entre les semiconductuers empilés.

L'AGD proposé est décrit sur la Fig. 6.8. Les circuits formés par $R1$, $R2$, $C1$ et $C2$ sont utilisés pour mesurer les tensions $V_{ds}$. Les tensions échantillonnées sont comparées aux tensions de référence en utilisant deux comparateurs afin d'acquérir les informations sur les vitesse de commutation et sur les retards. Ces données sont envoyées à un FPGA, qui génère les commandes de retard et de tension grille-source, équilibrant les tensions entre les SiC-MOSFET connectés en série.

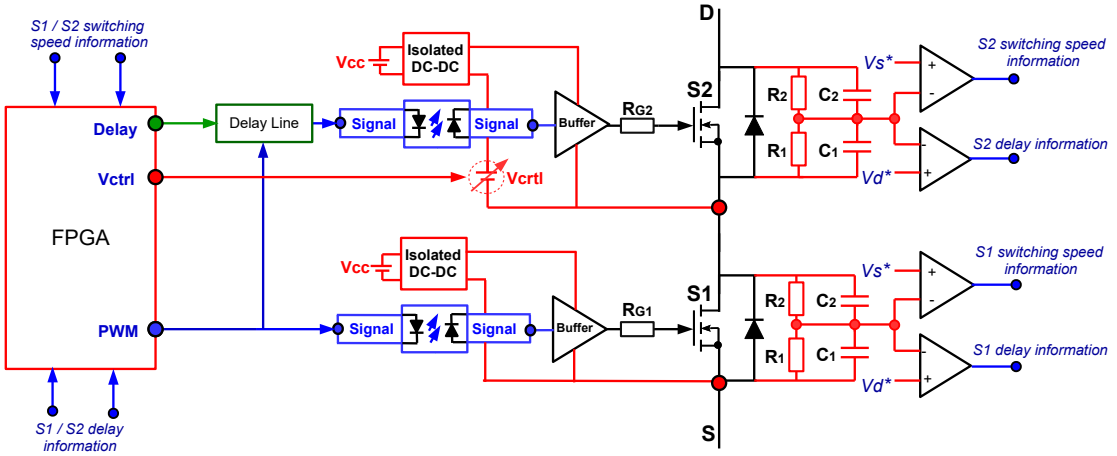



**Fig. 6.8.** Diagramme du driver actif proposé.

L'idée proposée est validée par des simulations électriques, qui présent des résultats satisfaisants. Les expériences restent pour des travaux futurs ou pour de nouveaux doctorants qui souhaitent contribuer sur le sujet des semiconducteurs connectés en série.

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