Study and realization of a data conversion chain for very high speed digital links

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THÈSE PRÉSENTÉE

POUR OBTENIR LE GRADE DE

DOCTEUR DE L'UNIVERSITÉ DE BORDEAUX

École Doctorale des Sciences de l'Ingénieur

Spécialité : Électronique

Présentée et soutenue par

David CORDOVA

Étude et réalisation d'une chaîne de conversion de données pour liaisons numériques à très haut débit

Thèse dirigée par Yann DEVAL

Préparée à MACOM Sophia Antipolis

et au Laboratoire IMS

soutenue le: 9 Décembre 2020

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Étude et réalisation d'une chaîne de conversion de données pour liaisons numériques à très haut debit.

Résumé: La demande croissante de débits de données plus élevés dans les centres de données a conduit à de nouveaux protocoles émergents (100 - 400G Ethernet et autres) dans les communications filaires. Ces protocoles favoriseront des encodages plus sophistiqués utilisant moins de bande passante de fréquence. Les exigences de vitesse devenant plus strictes, les architectures analogiques pures ne peuvent y répondre. Ainsi, un virage naturel vers des architectures à signaux mixtes est attendu.

Cette thèse propose la conception d'une architecture de récepteur basée sur un Convertisseur Analogique-Numérique (CAN). Il utilise une méthodologie de conception pour définir et valider les exigences et les spécifications des récepteurs filaires à base de silicium qui sont conformes à un fonctionnement supérieur à >100Gb/s sur des canaux de transmission avec des pertes élevées (>20dB). Un prototype en technologie 22nm CMOS FDSOI est proposé comme preuve de concept.

Mot clés: Centre de données, 100 Gigabit Ethernet, PAM4, Convertisseur Analogique-Numérique, Récepteur, Égalisation

Study and Realization of a Data Conversion Chain for Very High Speed Digital Links.

Abstract: The increasing demand of higher data rates in datacenters has led to new emerging standards (100 - 400G Ethernet and others) in wireline communications. These standards will favor more sophisticated encodings that use less frequency bandwidth. As speed requirements become more stringent, pure analog architectures can not meet them. So, a natural shift towards mixed-signal architectures is expected.

This thesis proposes the design of an ADC-based receiver architecture. It uses a design methodology to define and validate the requirements and specifications for silicon-based wireline receivers that comply with >100Gb/s operation over transmission channels with high losses (>20dB). A prototype in 22nm CMOS FDSOI technology is proposed as proof of concept.

Keywords: Datacenters, 100 Gigabit Ethernet, PAM4, Analog-to-Digital Converter, Receiver, Equalization

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Introduction

The increasing demand of higher data rates in datacenters has led to new emerging standards (200 - 400G Ethernet and others) in wireline communications. These standards will favored more sophisticated encoding schemes that require less bandwidth such as the case of PAM4. PAM4 indicates pulse-amplitude modulation with the "4" indicating four levels of pulse modulation. Its encoding uses 4 levels and reduces the bandwidth by a factor of 2. But at the price to be harder to be supported by purely analog solutions. So, a natural shift towards multi-level signaling and mixed-signal architectures is expected.

ADC-based solutions give more opportunities for speed increase. They present more robust solutions over channels with high losses (>20dB), because they can take advantage of technology scaling and most of the equalization can be implemented in the digital domain. Such ADCs are implemented using time-interleaving: identical sub-ADCs multiplexed in time, operating in parallel to achieve a higher sampling rate.

Thus, research in this area is crucial for the next-generation of wireline communication systems. Therefore, this thesis proposes the design of a PAM4 ADC-based receiver implementation with 112Gb/s data rate in 22nm CMOS FDSOI. This manuscript is composed of four chapters and organized as follows.

Chapter 1 introduces the context of high-speed digital links operating at 100Gb/s. Different aspects of wireline communications are revised such as 100 Gigabit Ethernet Standard, signal modulation, channel and equalization techniques at 100Gb/s. Then, a state-of-the-art analysis of wireline transmitters, receivers and transceivers is performed in order to identify the architectural trends and performance metrics. Finally, a set of requirements for silicon-based wireline receivers operating at 100Gb/s are defined.

Chapter 2 proposes the system analysis of an ADC-based receiver. It begins with listing the main specifications for 112Gb/s operation and choosing the appropriate channel for Long Reach applications. Then, several of the previously equalization

techniques are performed using the impulse response of the channel to evaluate them. Finally, an ADC-based receiver model is proposed and evaluated through system simulation in MATLAB Simulink.

Chapter 3 describes the design of a of 56GSample/s Time-Interleaved ADC (TI-ADC) for ADC-based wireline receivers. The first part describes the concept of TI-ADCs, the state of the art and the design considerations. The second part covers the design, clock generation and the simulation results.

Chapter 4 presents the physical implementation of an ADC-based receiver prototype in 22nm CMOS FDSOI technology. It includes the TI-ADC developed in chapter 3 and other blocks that complete the design. A testbench to perform characterization of the receiver and several aspects to improve the current design are discussed.

Chapter 1

High Speed Digital Links at 100Gb/s

Contents

In this chapter, we introduced the context of high speed digital links operating at 100Gb/s. Different aspects of wireline communications are revised such as 100 Gigabit Ethernet Standard, signal modulation, channel and equalization techniques at 100Gb/s. Then, a state-of-the-art analysis of wireline transmitters, receivers and transceivers is performed in order to identify the architectural trends and performance metrics. Finally, a set of requirements for silicon-based wireline receivers operating at 100Gb/s are defined.

1.1 Datacenters

Data centers are the backbone of today's Internet and cloud-based services and unprecedented quantity of data delivered in/between data-centers.

A data center is a collection of computing resources grouped together using communication networks to host applications and store data (see an example in Figure 1.1). A typical data-center is modeled as a multi-layer hierarchical network with thousands of low-cost commodity servers and switches as network nodes.

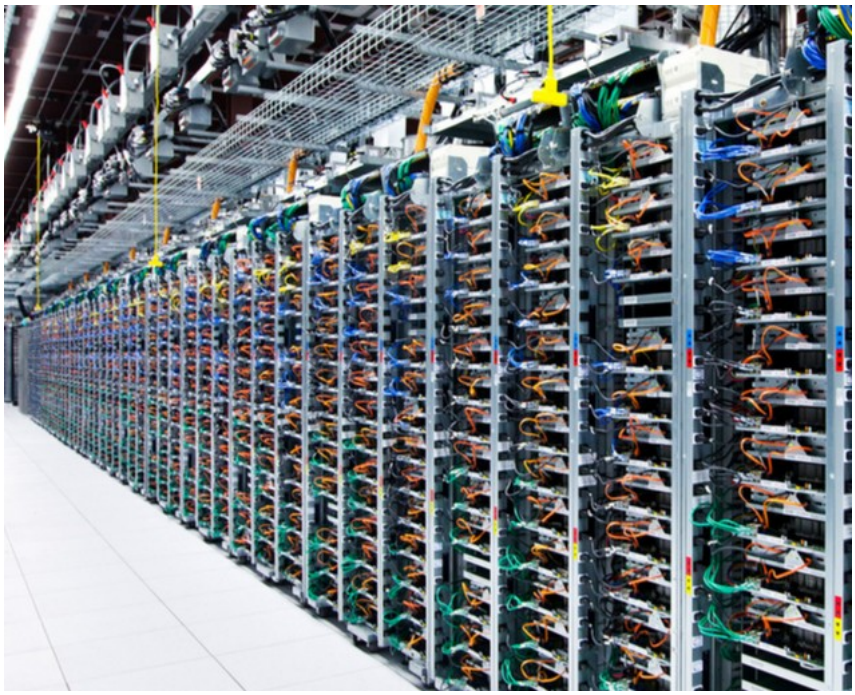


Figure 1.1: TierPoint datacenters.

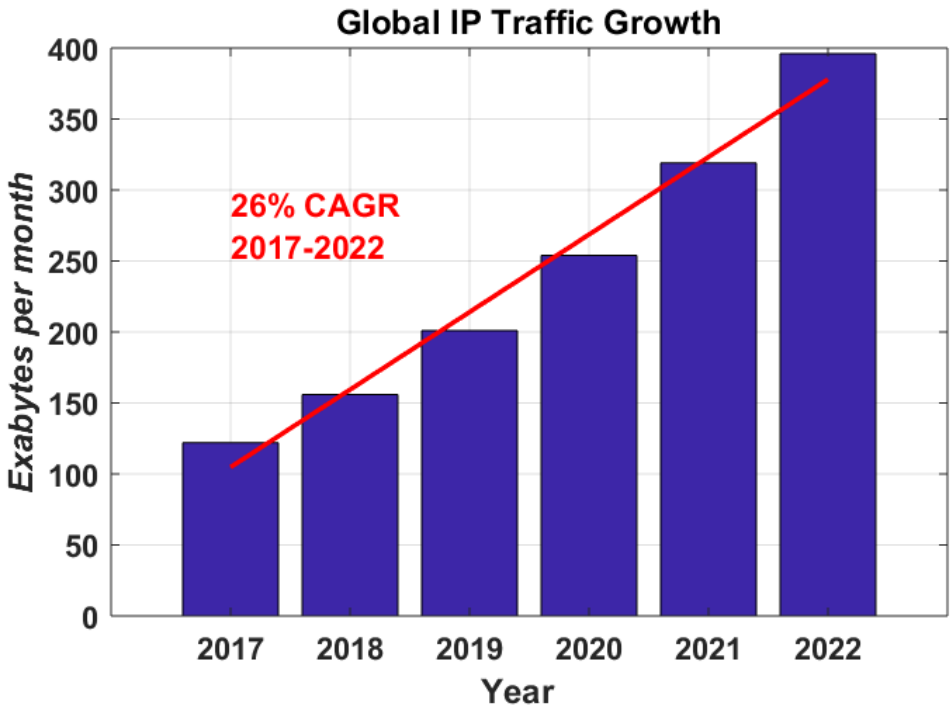


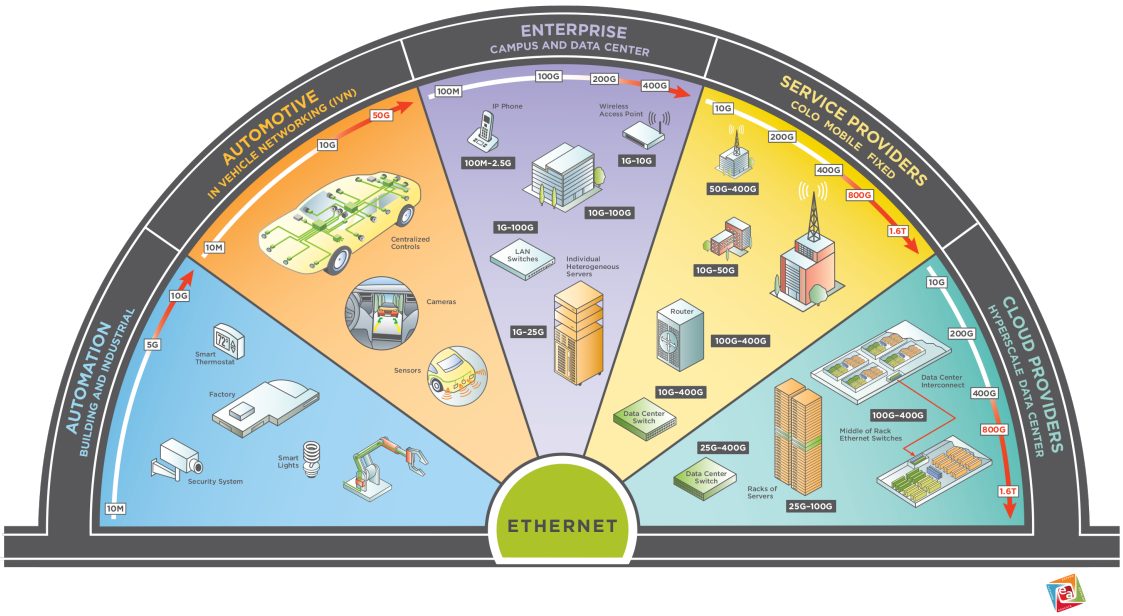
Figure 1.2: Global IP Traffic Growth [1]

The increasing complexity and sophistication of datacenter applications demands new features in the datacenter bandwidth and network. To further understand the impact that different services and applications are having on bandwidth growth, it is necessary to look at forecasted bandwidth growth. Figure 1.2 shows a forecast of Global IP Traffic Growth for the 2017 to 2022 time period, which illustrates growth from 122EB per month to 396EB[1] per month for a 26% Compound Annual Growth Rate (CAGR).

These requirements have led to considerable activity in the design and use of low-latency specialized data center fabrics such as PCI-Express based backplane interconnects, InfiniBand (IBA) [3], data center Ethernet [4].

Ethernet is a family of standards for communication over a physical media in computer networks. It is the most common technology in local area networks (LAN) and the working group IEEE 802.3 have released many standards since the first one

[1] 1EB = 1exabyte = 10^{18}bytes



Source: http://ethernetalliance.org/technology/2020-roadmap/

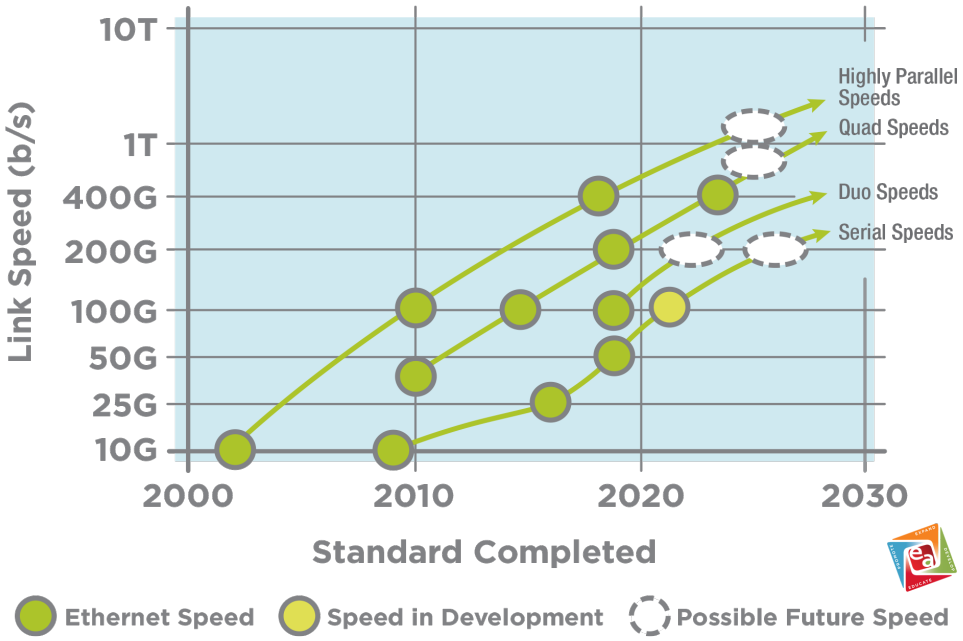
Figure 1.3: Ethernet Applications.

which was released in 1982.

The Ethernet Alliance roadmap traces Ethernet's path from 10Mb/s through present-day speeds of 1 to 400 gigabit Ethernet (GbE) and looks ahead to future speeds achieving up to 1.6 terabits Ethernet (TbE) and beyond (Figure 1.3). Figure 1.4 shows the evolution of the Ethernet speeds and possible future speeds. The forward-looking map also provides guidance into key underlying technologies current and future interfaces and the numerous application spaces where Ethernet plays a fundamental role [5].

Service providers have driven higher speed Ethernet solutions for decades. Router connections, Ethernet Passive Optical Network (EPON), client side optics for optical transport network (OTN) equipment and wired and wireless backhaul. In particular, the 5G mobile deployment is driving dramatic increases in both fronthaul and backhaul applications and continues to push Ethernet to higher rates and longer distances. The global demand by consumers for video shows no signs of changing.

Cloud providers were the first to adopt 10GbE servers on a large scale in 2010 for hyperscale data centers. With voracious appetites for applications like Artificial



Source: http://ethernetalliance.org/technology/2020-roadmap/

Figure 1.4: Ethernet Roadmap: Path to 100GbE single lane.

Intelligence (AI) and Machine Learning, hyperscale servers have moved to 25GbE and are transitioning to 50GbE and beyond. Unique networking architectures within these warehouse scale data centers have driven multiple multimode and single-mode fiber solutions at 100, 200 and 400GbE. The bandwidth demands of hyperscale data centers and service providers continue to grow exponentially, in a similar direction that blurs the lines between the two.

The ethernet standard as any wireline link over a typical communication channel can be modeled as a system shown in Figure 1.5. The link consists of a Transmitter (TX), a channel and a Receiver (RX). The data is sent by a transmitter through the channel, which consists of the Printed Circuit Board (PCB) trace, connectors and is recovered at the receiver. The data is conventionally encoded in pulse amplitudes which is referred to as Pulse Amplitude Modulation (PAM). Encoding 1 bit per symbol requires two amplitude levels and is referred to as Non-Return to Zero (NRZ) or PAM2.

For higher-rate transmissions, each pulse is substantially dispersed by the channel and InterSymbol Interference (ISI) occurs. An example of this is shown in Figure 1.5.

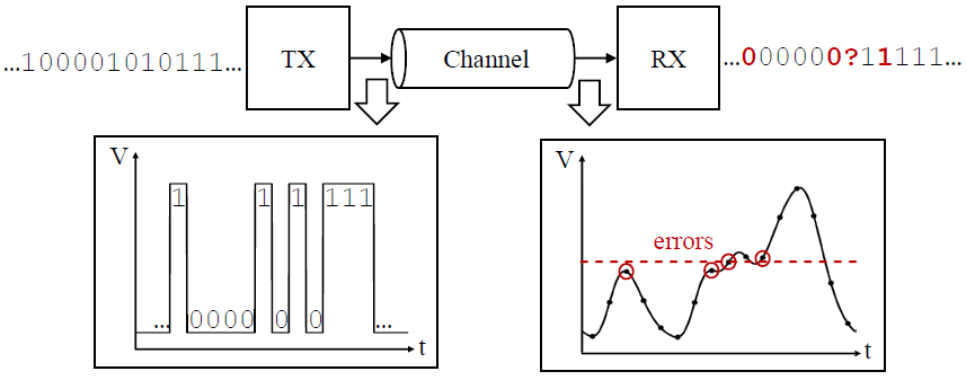


Figure 1.5: Simple link model.

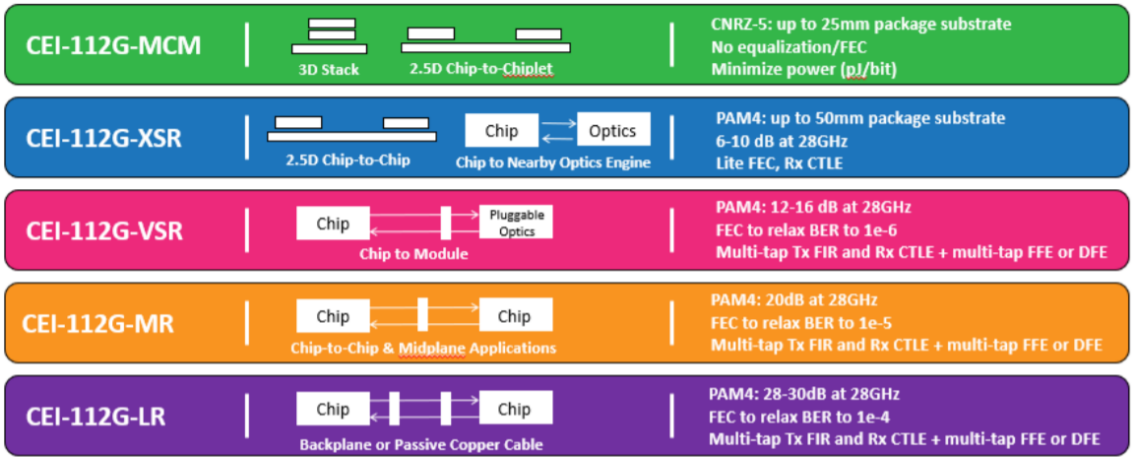
For this case, slicing without equalization results in errors in the output data. The source of the ISI is the channel loss at frequencies equal to and less than the Nyquist frequency, which becomes more problematic at higher data rates.

1.2 100 Gigabit Ethernet Standard

Today, all datacenter managers (e.g. Google, Facebook, Amazon, ...) have implemented 100 Gigabit Ethernet connectivity which consists of 4 parallel signals at 25Gb/s. The encoding of the signals is NRZ. The circuits in receivers and transmitters (optical or electrical) are well known and generally of an analog nature. The main disadvantage using this protocol is the high frequency bandwidth usage, especially up to (and even beyond) 12.5GHz.

For this reason, future standards for higher bitrate transmissions (200 - 400G Ethernet and others) will abandon NRZ in favor of more sophisticated encodings that use less frequency bandwidth. The IEEE 802.3 Ethernet Workgroup is in charge to complete the standard by fall of 2021 under the denomination IEEE 802.3ck which consists of 100, 200, and 400GbE using 100Gb/s lanes [6].

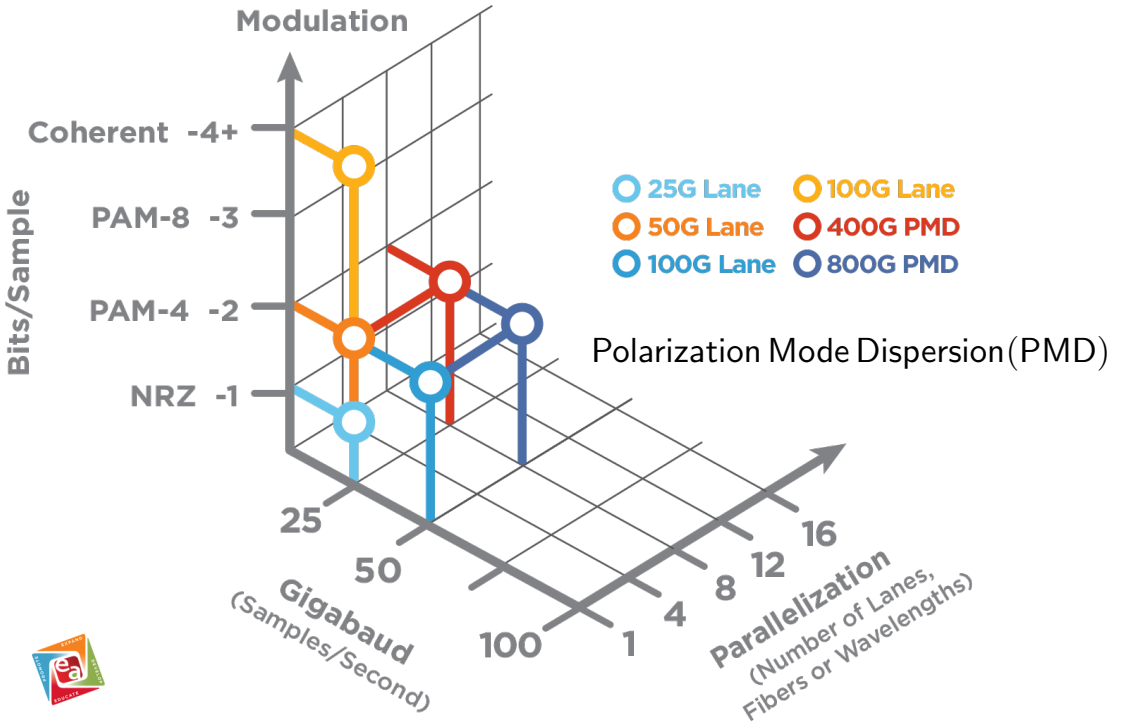
The Optical Internetworking Forum (OIF), a non-profit consortium, is also working on the Common Electrical I/O (CEI) 112G standard, which targets 112Gb/s electrical interfaces. Figure 1.6 shows the channel reach projects for CEI 112G.



- PAM4 modulation scheme becomes dominant in OIF CEI-112 Gbps interface IA
- One SerDes core might not be able to cover multiple applications from XSR to LR
- For short reach applications, simpler and lower power equalizations are desired

Source: https://www.oiforum.com/technical-work/current-work/

Figure 1.6: OIF's Common Electrical I/O (CEI) 112G reach projects.



Source: http://ethernetalliance.org/technology/2020-roadmap/

Figure 1.7: Data rate vs Parallelization for different modulation schemes.

1.2.1 PAM4 Signaling

As data rate continues to increase, 112Gb/s over single lane is on the horizon. The feasibility certainly depends on the choice of signal modulation and channel characteristics. In this section, we provide a brief introduction to 4-level Pulse Amplitude Modulation (PAM4) signaling so that basic concepts and ideas are defined.

Multi-level PAM is an emerging network signaling technology aimed to increase data traffic throughput by reducing the signaling speed. As can be seen in Figure 1.7, data rate above 100Gb/s can be implemented by means of parallelization and multi-level modulation.

PAM4 is gaining more attention in recent years as an alternative coding scheme to NRZ (binary modulation Non Return to Zero). In NRZ signaling, one bit is a symbol and has two distinct amplitude levels of '0' or '1'. Symbols are expressed in terms of baud. NRZ bitrate is equal to its symbol rate where 1Gb/s is equal to 1Gbaud.

PAM4 signaling uses four different levels, where each level corresponds to one symbol representing two bits. With two bits per symbol, the baud rate is half the bitrate. For example, 56Gbaud PAM4 is equal to 112Gbaud NRZ (112Gb/s). As such, PAM4 achieves twice as much throughput using half the bandwidth compared to NRZ. One of the most common naming convention for PAM4 signal levels is 0, 1, 2, 3, as can be seen in Figure 1.8.

In standard linear PAM4 signaling, it is possible for two transitions to happen at the same time. These transitions can cause two-bit errors per symbol. If standard PAM4 signaling is converted to gray code, the Bit Error Rate (BER) is reduced to one-bit per symbol and the overall bit error rate is cut in half. BER can be expressed as a function of the Signal-to-Noise Ratio (SNR) at the decision point:

$$\mathrm{BER}_{\mathrm{M,levels}} = \left(\frac{\mathrm{M}-1}{2\mathrm{M}}\right) \times \mathrm{erfc}\left(\sqrt{\frac{3 \cdot \mathrm{SNR}}{2(\mathrm{M}^2-1)}}\right) \tag{1.1}$$

where M is the number of distinct symbols for a given PAM modulation and erfc is the complementary error function, [7].

Compared to NRZ's two levels, PAM4 has four levels that result in 12 distinct

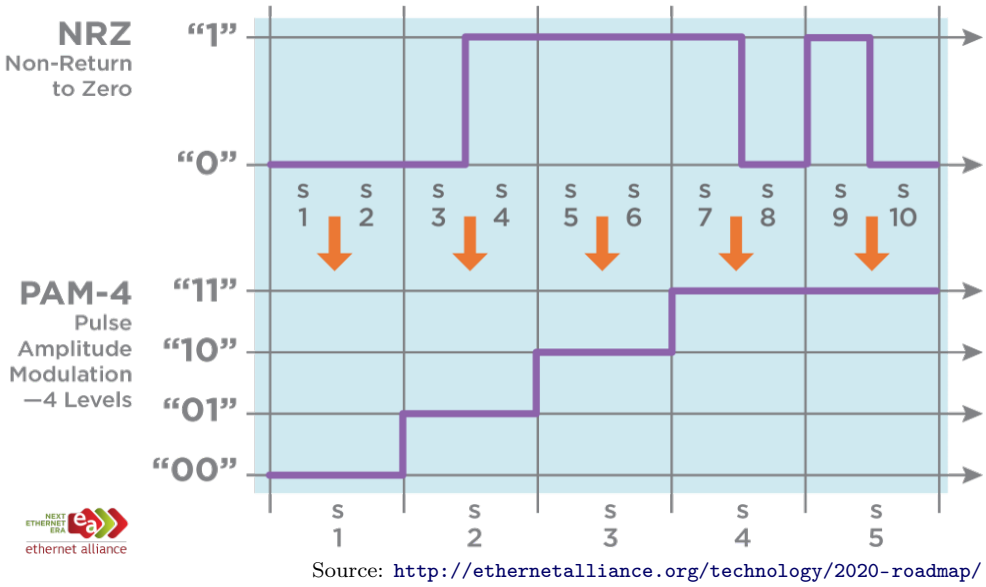


Figure 1.8: NRZ and PAM4 modulation schemes.

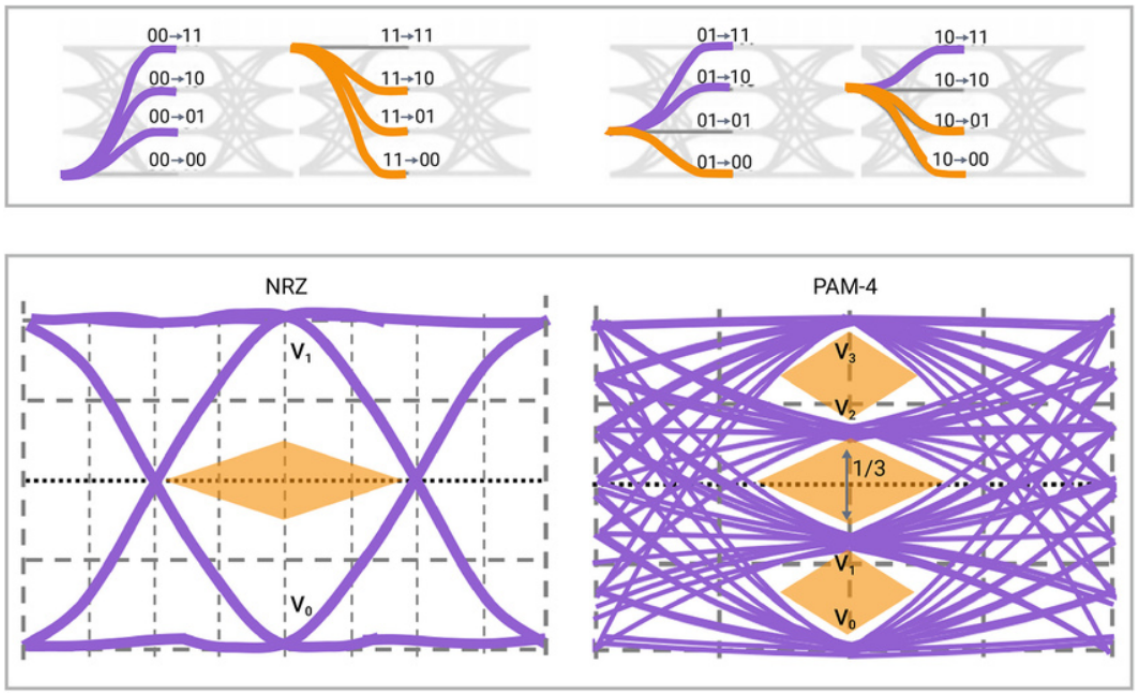


Figure 1.9: NRZ vs. PAM4 eye diagrams and symbols transition.

signal transitions. These transitions can be turned into an eye diagram (a.k.a. eye pattern) by cutting it up into segments that are two bit (or symbol) intervals long and overlaying them. An important advantage of the eye diagram over the linear signal

representation is that it shows all possible bit transitions in a compact way, as shown in Figure 1.9. From the eye diagram, it can be seen three distinct eye openings. Each eye height is 1/3 of an NRZ eye height, causing the PAM4 SNR to be degraded by over 9.5dB, which has an impact to the signal quality and introduces additional constraints in high-speed signaling.

As described above, the use of PAM4 signaling bring many advantages to overcome the bandwidth limitations of NRZ, but also bring new challenges in link-path analysis. New methodologies for PAM4 signaling have been developed in recent years, along with IEEE standard amendments and commercial tools, in response to increasing demand for higher speeds and the use of multi-level modulation schemes.

1.2.1.1 Forward Error Correction (FEC)

Forward Error Correction (FEC) is a method to control errors in transmitted data over communication channels [8, 9]. Figure 1.10 shows FEC implementation. The transmitted data is transformed into a codeword (redundant data addition) by the FEC encoder, before passing through the channel. The added redundancy allows the receiver FEC decoder to detect and correct errors that may occur. The general disadvantage of FEC is that the transmitter will send the code to the receiver no matter the code is correct or not, so a long and powerful error correction code is required which leads to an inefficient use of channel.

In practice, sophisticated codes such as the Reed–Solomon (RS) codes and the Bose–Chaudhuri–Hocquenghem (BCH) codes are used. In a typical transmission

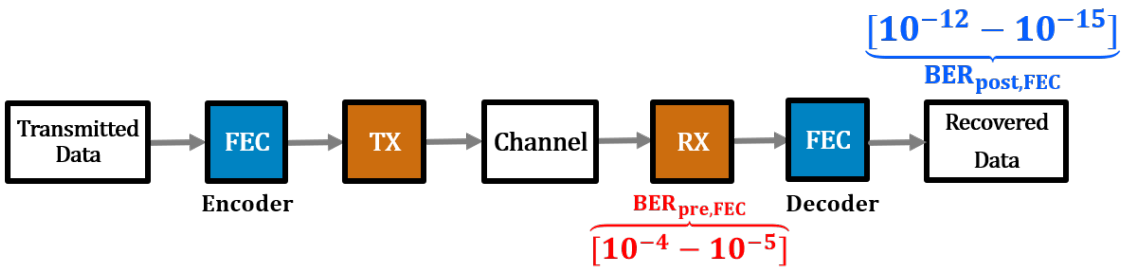


Figure 1.10: Simplified system employing FEC.

system with FEC, an incoming BER of 1×10^{-4} (i.e., BER at the output of the receiver[2]) can be boosted to 1×10^{-12} (output BER or $BER_{post,FEC}$) after error correction. This boosting means that a lower SNR requirement for the receiver can be tolerated, while maintaining the same output BER.

FEC becomes an important part of a PAM4 system solution to offset this SNR penalty, since one of the major design challenges of PAM4 signaling is the SNR penalty of PAM4 over NRZ, about 9.54dB (1/3 of the available signal).

1.2.2 Channel at 100Gb/s

A high-speed serial link is shown in Figure 1.11. Typically, it is composed of three major blocks: the transmitter, the channel and the receiver [10].

- TX serializes, modulates and sends the data through the channel to the receiver using an internal clock generated by a Phase-Locked Loop (PLL). The PLL is the time generator in a high-speed serial link. It provides a high-frequency clock for the system by multiplying the low-frequency reference clock.

- The channel is the physical link between the TX and the RX. It can be implemented using an optical fiber, a coaxial cable, a twisted pair UTP (Unshielded Twisted Pair), a PCB or a backplane. Predominantly

[2]denoted as $BER_{pre,FEC}$ or Raw BER

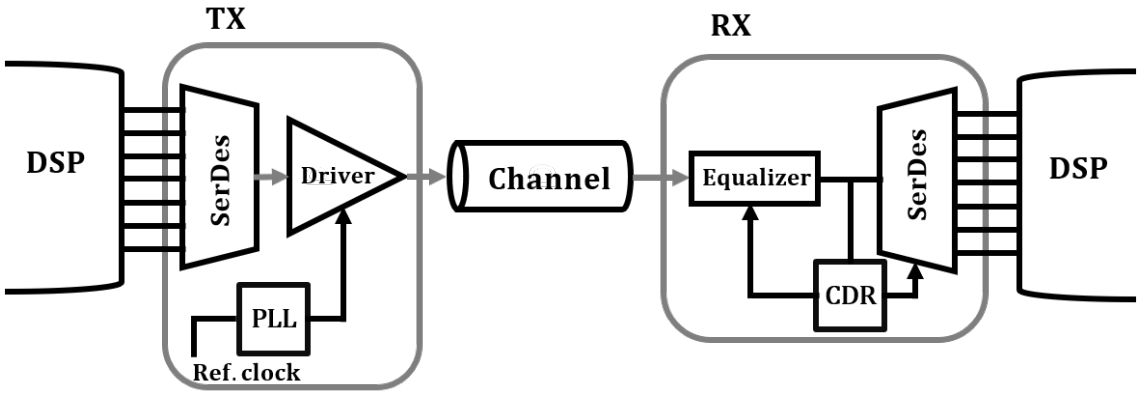


Figure 1.11: A typical high-speed serial link.

bandwidth-limited, the channel introduces loss, reflection and distortion in the upcoming data.

- The RX recovers the upcoming data performing two operations: sampling the input waveform with a clock synchronized with the data and deciding the digital value of the sampled voltage. It is convenient to generate the clock inside the receiver rather than transmit it from transmitter's PLL on a separate channel. The circuit that realizes this function is known as Clock Data Recovery (CDR). A CDR circuit incorporates a PLL and some additional circuits needed to synchronize the receiver with the incoming data stream. These timing blocks are crucial parts in a high-speed system because they provide correct spacing of transmitted data symbols and, on the receiver side, they have to sample the received signal waveforms.

As data rates steadily rise, the signal integrity of the channel becomes critical in high-speed serial link design. These signal integrity issues arise mostly due to the channel-frequency-dependent characteristics. We can identify three major problems: signal attenuation, reflection and crosstalk.

1. Signal attenuation occurs mostly due to conductor and dielectric losses. The channel presents itself as low-pass, where the attenuation is proportional to frequency. It can be characterized as the Insertion Loss (IL) of the channel.

2. The reflection is caused by impedance discontinuities or mismatches in the channel and can significantly degrade the quality of the signal. Return Loss (RL) is used to evaluate reflection.

3. Crosstalk occurs due to capacitive and inductive coupling between neighbouring transmission channels. Depending on the crosstalk location and strength, it may limit the signal transmission speed.

The combined effect of these problems creates attenuation and dispersion over the high-frequency content of the transmitted symbols sent across the channel, resulting

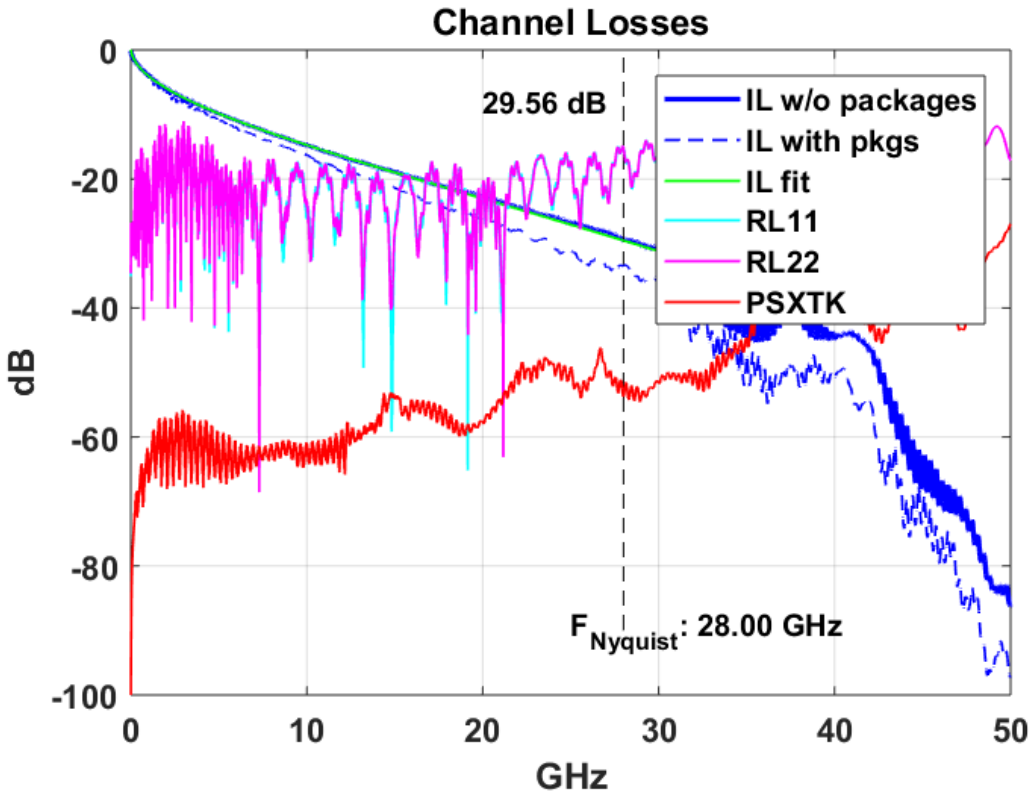


Figure 1.12: Insertion Loss (IL) for a channel intended for CEI-112G-LR.

in an attenuated received symbol energy that has been dispersed over several symbol periods. When transmitting data across the channel, energy from individual symbols will now interfere with adjacent ones and make them more difficult to detect. This ISI increases with channel loss and can completely close the received data eye diagram.

As discussed above, operating at higher data rates makes the channel loss increasing and the same channel technology may be unusable for higher throughput. Because PAM4 has half the baud rate of a NRZ signal, the Nyquist frequency (F_{NYQ}) in PAM4 is half the F_{NYQ} of NRZ for the same bitrate:

$$F_{NYQ,PAM4} = F_{NYQ,NRZ}/2 = F_{bitrate}/4 \tag{1.2}$$

The IL of a channel targeted for the CEI 112G Long Reach (LR) is shown in Figure 1.12. According to the specification the loss for 56GBaud PAM4 (112Gb/s) is between 28-30dB at Nyquist frequency of 28GHz. If NRZ were used instead of PAM4 for the same speed, the loss would be more than 30dB making it unfeasible. This key

advantage of PAM4 allows the use of existing channels and interconnects at higher bitrates without the need for doubling the baud rate and increasing the channel loss. Additionally, the impulse response can be obtained by taking the inverse Fourier Transform of the insertion loss.

To evaluate signal integrity in serial link analysis, the single pulse response is often used because:

- it gives a quick insight to the resulting eye diagram,
- it shows the effect of equalization,
- it gives insights to reflection and crosstalk,
- it helps characterize frequency-dependent loss of the channel.

Figure 1.13 shows the Channel Pulse Response (CPR). It is obtained by performing the convolution of the impulse response with a pulse of width equal to the symbol period. As can be seen the pulse energy is spread over several symbols Unit Interval (UI)s. Typically the strongest response value is assigned as the cursor (UI=0 or current UI), all the values before the cursor (UI<0) are called pre-cursors and the values after (UI>0) post-cursors. The CPR is asymmetrical over time with a long tail and dominated by post-cursors. This long tail is directly related to the low-frequency loss typical of conductor losses.

The presence of ISI is detrimental to the reception of transmitted symbols, since it tends to reduce the effective received SNR. Several ways to cancel or mitigate ISI will be addressed in the following subsection.

1.2.3 Channel Equalization

In order to compensate the losses and distortion induced by the channel, a process called equalization is employed [10, 11]. The purpose of the equalizer is to cancel ISI and extend a given channel's maximum data rate by making the cascade of the channel and the equalizer have a flat frequency response, as shown in Figure 1.14. The

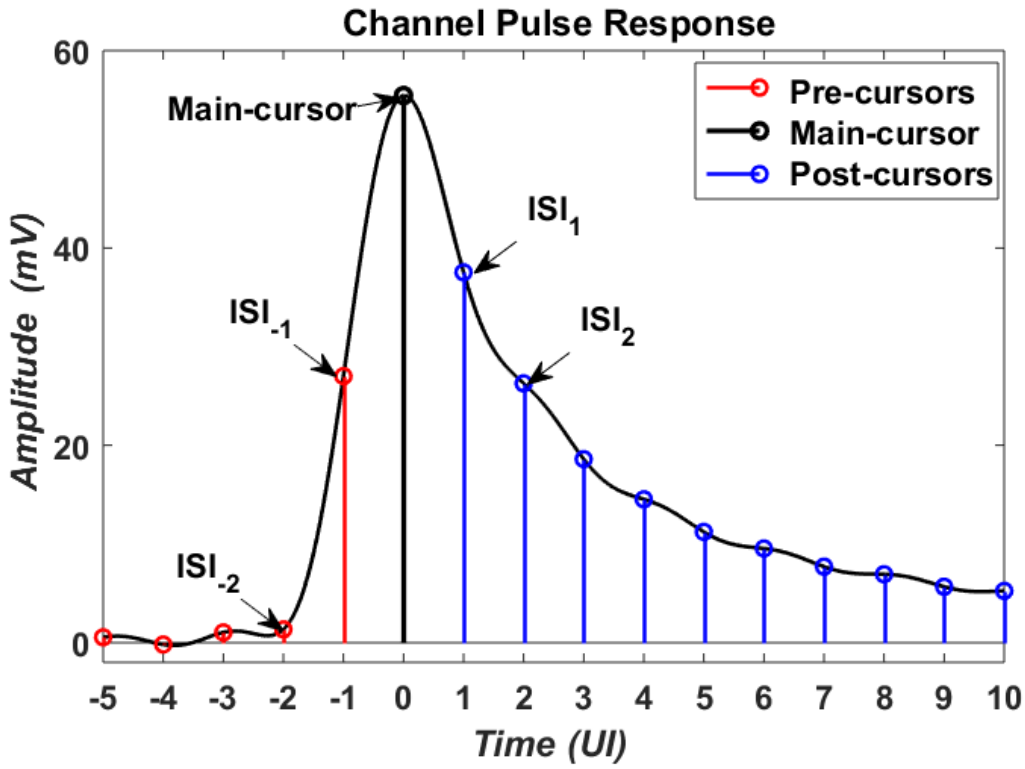


Figure 1.13: Channel Pulse Response. $A_{TX} = 1V_{pp}$, IL=30dB.

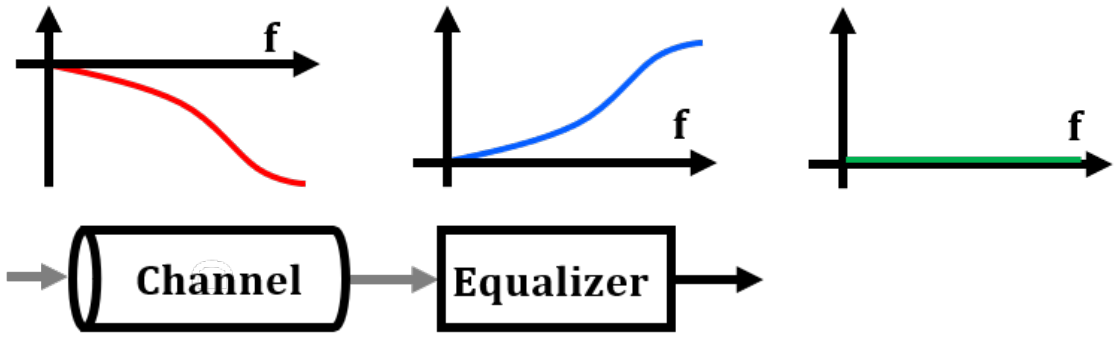


Figure 1.14: Channel Equalization in Frequency domain.

equalizer transfer function is the inverse of channel transfer function, i.e., a high pass transfer function.

Depending on the application and maximum bit rate, we can distinguish three types of equalizers:

1. Continuous Time Linear Equalizer (CTLE),

2. FeedForward Equalizer (FFE),

3. Decision Feedback Equalizer (DFE),

They can be organized in several categories, as shown in Table 1.1. The first distinction is made on the type of input signal, where we can find equalizers that work with only analog or digital signals. The second is the equalization method implementation. Equalizers can be implemented either as linear filters (both discrete and continuous-time) that attempt to flatten the channel frequency response, or as nonlinear filters that directly cancel ISI based on the received data sequence. CTLE and FFE can cancel both ISI pre- and post-cursors while DFE can only cancel ISI post-cursors.

Table 1.1: Types of equalizers

Continuous Time Linear Equalizer (CTLE)	**FeedForward Equalizer (FFE)**	**Decision Feedback Equalizer (DFE)**
Analog	Analog/Digital	Analog/Digital
Linear	Linear	Non-linear
Pre and post-cursor	Pre and post cursor	Only post-cursor
RX	TX* or RX	RX

*Need a back channel

It should be noted that distinctions made above are for equalizers on the RX side, nonetheless transmit equalization is often implemented as well. In this case, the transmitter attempts to invert the channel distortion that a data bit experiences by predistorting or shaping the pulse over several bit times, a process known as "de-emphasis".

Depending on system data rate requirements relative to channel bandwidth and the severity of potential noise sources, different combinations of transmit and/or receive equalization are employed and described in the following subsections.

1.2.3.1 Continuous Time Linear Equalizer (CTLE)

A CTLE filters the receiver input signal by either boosting high frequency content attenuated in the channel or relatively attenuating low frequency content [11]. It introduces zeros to compensate the frequency-dependent channel loss. The CTLE is generally preceded and/or followed by an Automatic Gain Control (AGC) circuit to bring the signal to the appropriate level to achieve adequate SNR and to not amplify the signal too much to go too much beyond the nonlinear range. An example of

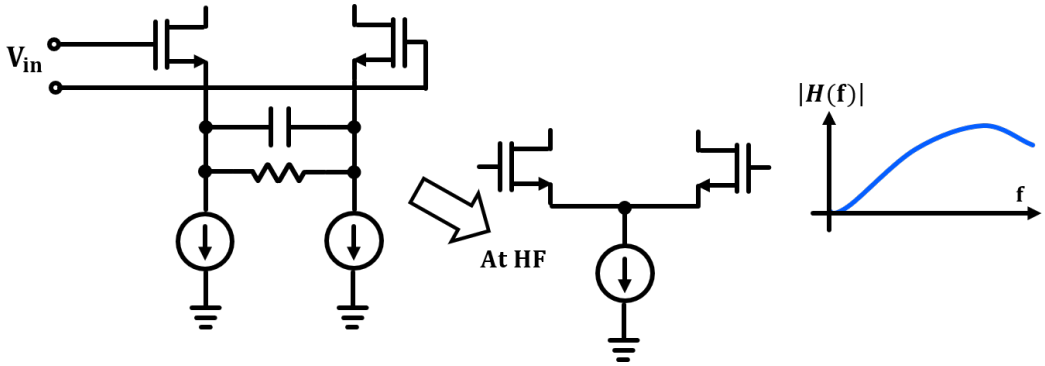


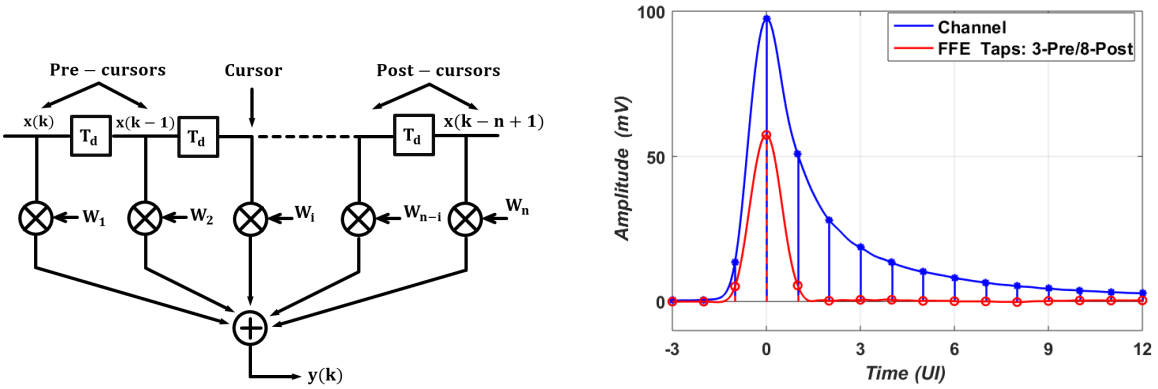
Figure 1.15: Active continuous time linear equalizer (CTLE).

CTLE implementation is shown in Figure 1.15. Here, programmable RC-degeneration in the differential amplifier creates a high-pass filter transfer function (one-zero and two-pole stage). The zero corresponds to the RC tank, the first pole caused by the finite transconductance (g_m) of the differential pair and the second pole at the output.

While this implementation is a simple and low-area solution, one issue is that the amplifier has to supply gain at frequencies close to the full signal data rate. This gain-bandwidth requirement potentially limits the maximum data rate. During the high frequency boosting of the signal, CTLE could potentially amplify noise and crosstalk depending on the required CTLE/AGC settings. This calls for more precautions using CTLE for certain applications, for example, when the environment is noisy.

1.2.3.2 FeedForward Equalizer (FFE)

The equalization capability required of time-domain equalizers in terms of number of symbol-rate taps is directly proportional to the channel ISI delay spread and the data rate. A FFE is implemented using a Finite-Impulse-Response (FIR) filter whose function is to collect the energy from a set of ISI pre-cursors and post-cursors onto the cursor [10, 11, 12].



(a) Implementation

(b) 3-precursor/8-postcursor FFE

Figure 1.16: Feedforward equalizer (FFE)

A typical FFE implementation is shown in Figure 1.16. It consists of n multipliers with a variable coefficient, *n-1* delay cells and a summing node. A FIR can generate large types of transfer function thanks to the different values of its coefficients. Usually, since the signal input multipliers is taken along the delay line, the multipliers are called "taps". The delays are interposed between the taps and each of them provides a delay T_d. In the time domain the input-output relation of the FIR is given as:

$$y(kT) = \sum_{i=1}^{n} W_i(k + 1 - i)T_d \tag{1.3}$$

One method for determining the taps is to minimize the Mean Square Error (MSE) of the equalizer output. We start calculating the error with respect to a desired output

$$E = HW - Y_{des} \tag{1.4}$$

where H represents the pulse response of the transmitted symbol and channel, W corresponds to the FFE matrix taps and Y_{des} is the desired ISI free output. Then, the error matrix norm^2 is

$$\|E\|^2 = W^T H^T H W - 2Y_{des}^T H W + Y_{des}^T Y_{des} \tag{1.5}$$

and differentiating with respect to the matrix taps, we find the taps which yield minimum error norm^2,

$$\begin{aligned} \frac{d}{dW}\|E\|^2 &= 2W^T H^T H - 2Y_{des}^T H \\ W^T H^T H &= Y_{des}^T H \end{aligned} \tag{1.6}$$

Finally solving for optimum FFE taps, leads to

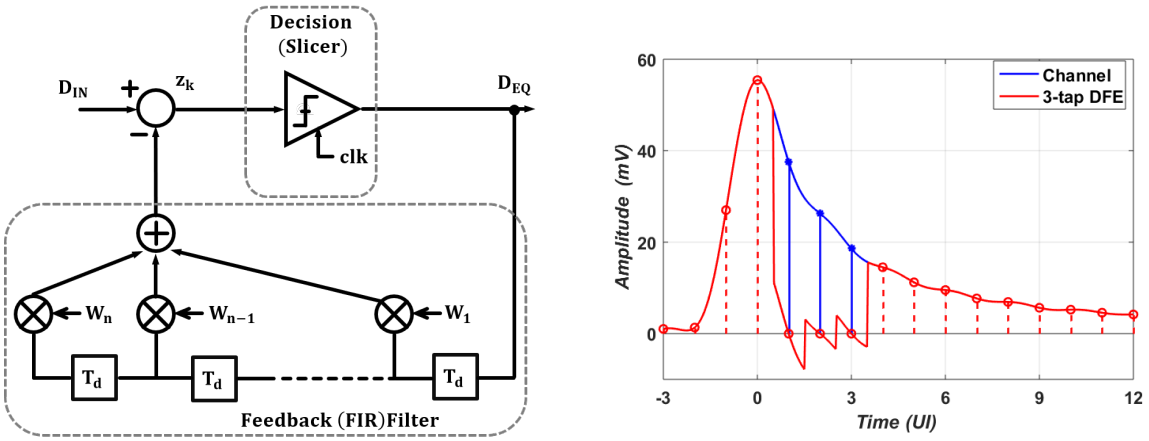
$$W_{opt} = (H^T H)^{-1} H^T Y_{des} \tag{1.7}$$

The matrix W_{opt} produces a value of "1" at the output cursor, so a normalization by the sum of the absolute values of W_{opt} is needed:

$$W_{opt,norm}(n) = \frac{W_{opt}(n)}{\sum_{i=1}^{n} |W_{opt}(n)|} \tag{1.8}$$

A FFE may be programmed to mitigate ISI from all taps pre-cursor and post-cursor. This can be achieved by implementing a FFE on the receiver-side and adaptively tuning the filter taps to a specific channel. A disadvantage of the FFE is the so-called noise enhancement [13]. For example, in trying to compensate for a channel with a low-pass response, the equalizer adapts to a high-pass response, which has the undesirable side effect of amplifying (or enhancing) high-frequency noise. The result is a reduced SNR.

The problem of noise enhancement can be eliminated by using a DFE (Figure 1.17). Unlike the aforementioned equalizers, DFE utilizes the previous decisions to estimate and cancel the ISI introduced by the channel [10, 11, 12]. The feedback filter estimates the ISI based on previous decisions and therefore, can only cancel post-cursor ISI. Since the ISI cancellation is based on previous decisions, without high frequency boost, it is inherently immune to noise enhancement. However, there is the potential for error



(a) Basic architecture (b) 3-tap DFE

Figure 1.17: Decision feedback equalizer (DFE)

propagation in a DFE if the noise is large enough for a quantized output to be wrong. Also, due to the feedback equalization structure, the DFE cannot cancel precursor ISI.

The major challenge in DFE implementation is closing timing on the first-tap feedback since this must be done in one bit period or UI, [10].

1.3 Wireline Transceivers for 100Gb/s

As the link's speed requirements become more stringent, pure analog architectures cannot meet them. So, a natural shift towards mixed-signal architectures is expected. Links based on Analog-to-Digital Converter (ADC) give more opportunities for speed augmentation because they constitute more robust solutions due to their digital nature and they scale well with process.

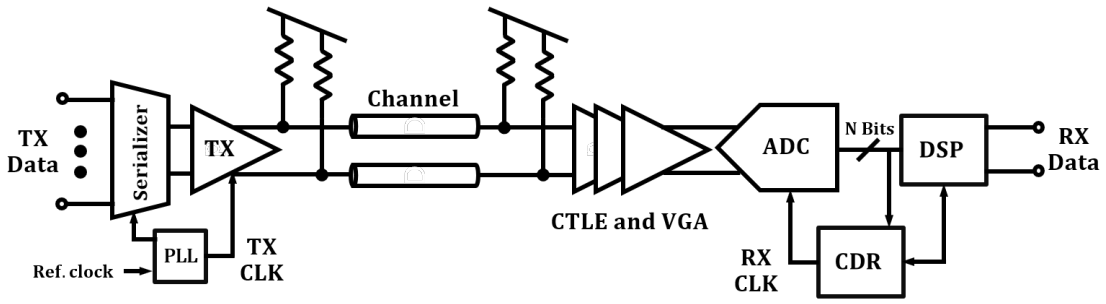


Figure 1.18: Conventional ADC-based high-speed serial link.

A typical ADC-based link is shown in Figure 1.18. Here, an Analog Front-End (AFE) performs pre-equalization and signal conditioning for the input signal, then ADC converts the pre-equalized signal into the digital domain. The Digital Signal Processing (DSP) unit typically includes FFE and DFE. The CDR loop in the receiver align the sampling clock with the received signal using a phase-tracking feedback loop.

In the following section, a review of the state-of-the-art of transmitters, receivers and transceivers operating above 100Gb/s is presented.

1.3.1 Transmitter

Typically, three main categories of transmitters can be identify:

1. Analog or Digital-to-Analog Converter (DAC) based ones,

2. Architecture, the transmitter can be implemented full-rate or with serialization (half-rate, quarter-rate),

Table 1.2: Comparison of recent published >100Gb/s PAM4/NRZ Transmitters

	[14]	[15]	[16]	[17]	[18]	[19]	[20]
Conference	VLSI 2018	ISSCC 2018	ISSCC 2018	ISSCC 2019	ISSCC 2019	ISSCC 2020	ISSCC 2020
Architecture	Quarter rate	Quarter rate	Quarter rate	Quarter rate	Quarter rate	Half rate	Quarter rate
Type	Analog	Analog	DSP-DAC	Analog	Analog	DSP-DAC	DSP-DAC
Signaling	PAM4	PAM4 /NRZ	PAM4	PAM4 /NRZ	PAM4 /NRZ	PAM4 /NRZ	NRZ
Technology	16nm FinFET	10nm CMOS	14nm CMOS	14nm FinFET	40nm CMOS	7nm FinFET	40nm CMOS
Data rate [Gb/s]	112	112	112	128	112	10-112	100
Clock Source	On-chip PLL	On-chip PLL	External	External	On-chip PLL	On-chip PLL	External
Driver Topology	SST	CML	SST	CML	SST	Soft switching	CML (tailless)
Output Swing	$1V_{pd}$	$0.75V_{pd}$	$0.92V_{pd}$	$0.6V_{pd}$	$1V_{pd}$	$1.2V_{pd}$	$0.56V_{pd}$
Tx FFE	4-tap FFE	3-tap	8-tap	3-tap FFE	4-tap	7-tap	8-tap
Efficiency [pJ/b]*	3.08	1.72	2.6	1 (112Gb/s)	3.62	1.05	6.19
Core Area [mm^2]	0.38	0.0302	0.095	0.048	0.56	0.193	0.504

*Excluding PLL

3. Output driver/combiner, it can be Current Mode Logic (CML) or Source-Series Resistance (SST). For transmitters operating above 100Gb/s, a FFE of at least 3-taps (pre-cursor, cursor and post-cursor) to compensate channel losses is required.

Table 1.2 shows the state-of-the-art of 100Gb/s transmitters. A brief description of these works pointing out their main characteristics follows.

Following the works in [14], [15], [17] and [18], we can find the classical or analog-based Tx FFE structures. All analog implementations, with the exception of [14], can support PAM4 and NRZ modulation. FFE tap reconfiguration is found in [17] and [18]. In the latter, a two-step FFE consisting of coarse tuning and fine tuning is adopted to overcome output bandwidth and power efficiency degradation. DAC-based FFE structures are implemented in [16], [19], [20]. FFE is done in the digital domain giving maximum flexibility and allowing a larger number of taps (> 7 taps).

All, with the exception of [19], employed quarter-rate architecture (clock frequency $\leq$ 16GHz) for power efficiency. For the driver topology, CML drivers are preferred for DAC-based structures. In [19], a 'soft-switching' H-bridge output driver is introduced to enable a 1.2V peak-to-peak differential output swing without exposing devices beyond breakdown voltage.

Most of the transmitters have been implemented in technology node below 16nm. The works presented in [18] and [20] aim to deliver PAM4 transmitters over 100Gb/s in 40nm CMOS to reduce costs. From this review, we can see that a trend for DAC-based structures will be favored in the future, allowing more flexible designs.

1.3.2 Receiver

As mentioned earlier, the high logic density of lower process will allow receivers relying heavily on digital signal processing (DSP), [21]. These digital receivers incorporate an ADC to digitize the received signal and perform equalization in the digital domain.

The latest works for ADC-based receivers follow the same approach (see table 1.3).

Table 1.3: Comparison of recent published >100Gb/s PAM4 Receivers

	[22]	[23]	[24]
Conference	VLSI 2018	VLSI 2019	ISSCC 2019
Architecture	ADC-based 64-Way 7-bit SAR-ADC	ADC-based 64-Way 6-bit SAR-ADC	Analog
Signaling	PAM4	PAM4	PAM4/NRZ
Technology	16nm FinFET	10nm CMOS	14nm FinFET
Data rate [Gb/s]	112	112	100
Loss@Nyq. (dB)	20 (BERT)	35 (BERT)	19.2
Equalization	CTLE 31-Tap FFE 1-tap DFE	CTLE 16-Tap FFE 1-tap DFE	8-tap Tx FFE CTLE 1-tap DFE (1+0.5D)
Pre FEC BER	2×10^{-5}	1×10^{-6}	$< 1 \times 10^{-12}$
PRBS	31	31	15
CDR	Baud rate	Baud rate	Baud rate (1+0.5D)
Efficiency [pJ/b]*	5.27	4.2	1.1
Core Area [mm^2]	0.674	0.281	0.053

*Excluding DSP

An AFE, consisting of a CTLE and gain stage, provides a "pre-equalization" and signal conditioning for a Time-Interleaved ADC (TI-ADC). The ADC samples are retimed and sent to equalization, with DSP accounting a large number of FFE taps and 1-tap DFE. In [22], a peaked source follower that uses programmable inductive peaking compensates bandwidth losses before the ADC. The pre-DSP ADC outputs are periodically stored in an on-chip 64Kb storage and read into an off-chip FPGA that performs equalization adaptations and ADC offset/gain/skew calibrations. A Q-shaping equalization in the CTLE is implemented in [23] for a tuning of 25dB gain at peak frequency of 26GHz.

One important aspect to mention is the power consumption. Usually, these ADC-based designs are power hungry reaching 500mW per lane without counting the DSP power. A low-power alternative is presented [24], where the receiver uses a CTLE combined with a 1-tap speculative DFE. Power optimization is obtained when the number of slicing levels to resolve the 1-tap PAM4 DFE speculation is reduced

Table 1.4: Comparison of recent published >100Gb/s Wireline PAM4 Transceivers

	[25]	[26]	[27]
Conference	ISSCC 2019	ISSCC 2020	ISSCC 2020
Signaling	PAM4/NRZ	PAM4	PAM4
Technology	16nm FinFET	7nm FinFET	7nm FinFET
Data rate [Gb/s]	106	112	112
Loss@Nyq. (dB)/ BER	DR4/FR4 optical	37.5@ BER=1×10^{-8}	38.9@ BER< 5×10^{-7}
TX Arch.	CML, 7-bit DAC 3-tap FIR	CML, Analog 4-tap FIR	SST, 7-bit DAC 6-tap FIR
RX Arch.	ADC-based VGA 64-Way 7-bit SAR-ADC DSP: 10 FFE	ADC-based CTLE/PGA 36-Way 7-bit SAR-ADC DSP: 31 FFE/1-DFE	ADC-based CTLE/VGA 56-Way 7-bit SAR-ADC DSP: 8-24 FFE/1-DFE
Power* [mW/lane]	900	602	460
Core Area [mm^2]	1.54	0.403	0.385

*Excluding DSP

from 12 to 8 by shaping the channel to a 1+0.5D response (h0+0.5*h0) with CTLE and Tx FFE. This receiver design can equalize a 19.2dB loss channel (with 8-tap TX FFE) while consuming 111.4mW at 100Gb/s PAM4 signaling. It can be seen that for channels with medium losses (<20dB), an analog solution presents itself as a good alternative for power saving.

1.3.3 Transceivers

We have reviewed transmitters and receivers as standalone building blocks, but ultimately both will interact with each other inside the link. Three designs operating above 100Gb/s are described, one for optical interconnections and the other two for electrical ones (Table 1.4). In terms of architecture, all receivers are ADC-based and all transmitters are analog and DAC-based, both with FFE.

A transceiver for PAM4 optical interconnections is presented in [25]. The transmitter is dual mode PAM4/NRZ DAC-based 3-tap FIR with half-rate architecture. The pre-driver adopts a resistor feedback inverter topology for a sub-UI equalizer to improve bandwidth and ISI. The receiver is composed of Variable Gain

Amplifier (VGA) followed by a 64-way 7-bit SAR-ADC. The ADC uses a 2-rank hierarchical time-interleaved sampling architecture to reduce the VGA load and the number of jitter-critical clock signals. It is fabricated in 16nm FinFET and consumes 900mW.

The transceivers for electrical connections share similar characteristics. Both are designed for LR with channel losses >30dB with ADC-based architecture in the receiver and DSP for FFE/DFE equalization. They are fabricated in 7nm FinFET.

A CML 4-tap FFE analog transmitter operating at quarter-rate is presented in [26]. It implements duty cycle and I/Q mismatch calibration to enable the use of a power-efficient CMOS 4:1 MUX. A distributed inductor peaking network is designed to compensate for >200fF device and parasitic capacitance at the current summing node. The AFE consists of a 2-stage CTLE and Programmable Gain Amplifier (PGA), both using inverter-based amplifier stages comprised of a G_m cell and inverse-G_m load (G_ml). The ADC is a 36-way TI-ADC, operating 6-by-6 sub-ADC units in a two-rank hierarchy. The DSP implements a 31-tap FFE and 1-tap DFE. This transceiver achieves a BER lower than $< 1 \times 10^{-8}$ for a channel loss of 37.59dB.

A SST 6-tap DAC-based transmitter is presented in [27]. A G_m-TIA-based topology is used for the CTLE and VGA. The ADC is a 56-way TI-ADC with 8-way T/H sampler to simplify clocking complexity, provide isolation between consecutive T/H phases and reduces CTLE loading. The DSP implements a programmable 8-24 tap FFE with a 1-tap, loop-unrolled DFE equalizer. DSP also includes a 6-tap FIR in the Tx side for de-emphasis. It is able to achieve a BER better than 5×10^{-7} with 38.9dB channel loss while consuming 460mW (TX/RX w/o DSP), the lowest power reported for 112Gb/s PAM4 LR applications.

1.4 Conclusion

This chapter has introduced the context of high speed digital links, from the current standard to equalization techniques for 100Gb/s applications. Following the state-of-the-art analysis, it seems to guarantee single lane operation at 100Gb/s and beyond. The link modules (transmitter and receiver) should meet the following requirements:

- **Multi-level signaling capabilities**, to enable an efficient usage of bandwidth,
- **Mixed signal architecture**, to take advantage of technology scaling and implement most of the equalization in the digital domain,
- **Low-power operation**, to cope with energy and power dissipation constraints.

DAC-based transmitters and ADC-based receivers appear as good candidates to provide a 100Gb/s solution. The realization of a suitable receiver that meets the requirements listed above will be conducted in the next chapter.

We propose to validate through a link system analysis, the specifications of an ADC-based receiver compatible with 100Gb/s operation.

Chapter 2

A Wireline PAM4 ADC-Based Receiver for 112Gb/s

Contents

In this chapter, the system analysis of an ADC-based receiver is implemented. It begins with listing the main specifications for 112Gb/s operation and choosing the appropriate channel for Long Reach applications. Then, several of the previously reviewed equalization techniques are performed using the impulse response of the channel to evaluate them. Finally, an ADC-based receiver model is proposed and evaluated through system simulations in MATLAB Simulink.

2.1 Link System Level methodology

A link system analysis is performed to evaluate the specifications of a wireline receiver that complies with 112Gb/s operation for Long Reach applications. Figure 2.1 presents the methodology used for the link system simulation. It is described as follows:

- An analysis of the 100GbE standard and state-of-art of wireline receivers is carried out to define the specifications and architecture,
- The channel is selected according to the IL requirements for LR applications,
- The IL, ICN and CPR are extracted from the S-paramater files of the selected channel,
- Equalization is applied to the CPR to obtain the CTLE transfer function and FFE/DFE coefficients,
- The link is built in MATLAB Simulink using the IL, ICN and CPR equalization. The model includes: transmitter, channel, receiver and crosstalk,
- Both transmitter (TX) and receiver (RX) are parameterized for more flexible analysis,
- The link is simulated for a given set of Tx/Rx parameters and bit pattern. Then, the BER is calculated from the received bit pattern,
- This simulation is repeated if there is a new set of parameters.

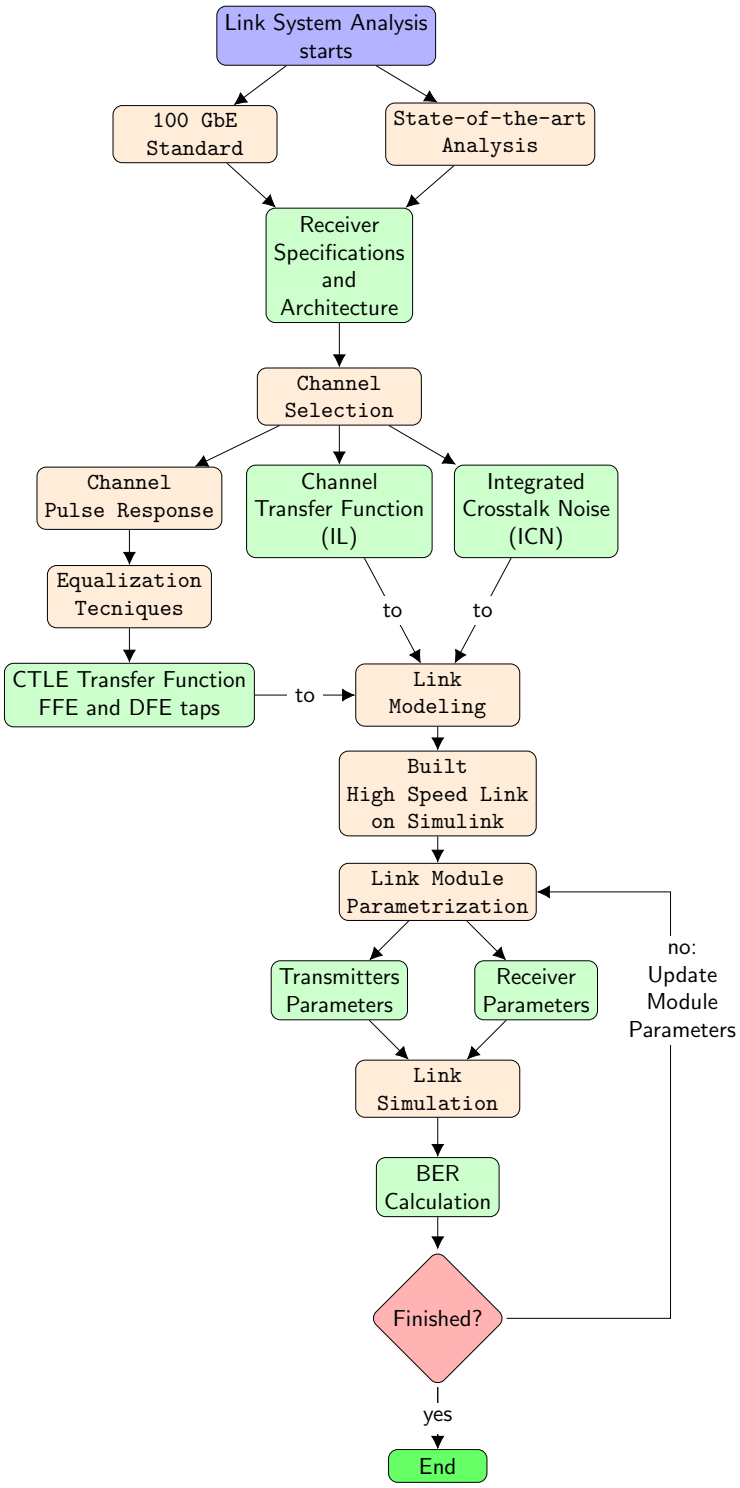


Figure 2.1: Flow chart for link system simulation.

2.2 Receiver specifications

A set of specifications for an ADC-based receiver that complies with 112Gb/s operation for Long Reach applications is proposed in Table 2.1. These specifications were based on the 100GbE standard and the state-of-the-art wireline receivers.

Table 2.1: ADC-Based Receiver Specifications for 112Gb/s

Specifications	
Data rate [Gb/s]	112
Baud rate [Gbd]	56
Signaling	PAM4
$F_{Nyquist}$ [GHz]	28
IL [dB]	∼20dB to ∼30dB @ $F_{Nyquist}$
BER	Raw: 1×10^{-4} to 1×10^{-5}, Using FEC: 1×10^{-12}
Power* [mW/lane]	< 500

*Excluding DSP

The most important features for this receiver are:

1. The use of PAM4 modulation. PAM4 signaling presents a good alternative over NRZ in terms of bandwidth efficiency,

2. The receiver is intended to compensate losses above 20dB to make it suitable for Long Reach applications,

3. The use of PAM4 signaling. It requires the use of FEC-encoding in order to relax the specifications of the receiver. A raw BER (no FEC) between [1×10^{-4} - 1×10^{-5}] is set as a constraint. FEC-enconding will reduce BER to a more suitable value of 1×10^{-12}, expected for high-speed serial links,

4. The receiver is competitive with current state-of-the-art implementations. A power target of 500mW is defined, which corresponds to the analog/mixed-signal blocks of the receiver with the exception of DSP.

One of the most important aspects in our system analysis for the ADC-based receiver is the backplane channel often referred simply as the «channel». The signal integrity of the channel defines reflection, crosstalk and loss which are the three primary factors that limit data transmission. For that reason, the selection of the channel that complies with the receivers specifications must be done considering the factors mentioned above.

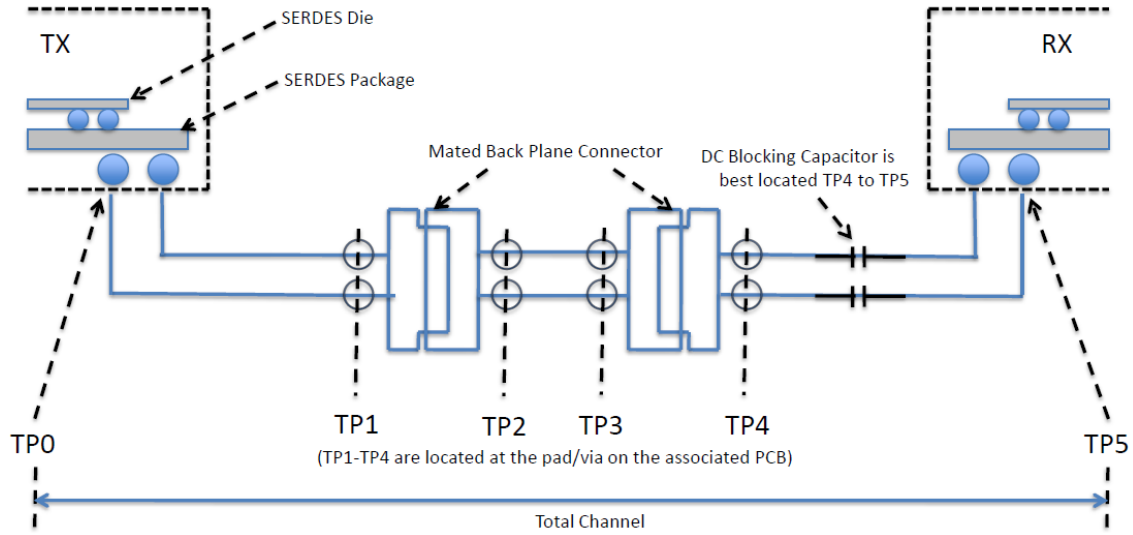
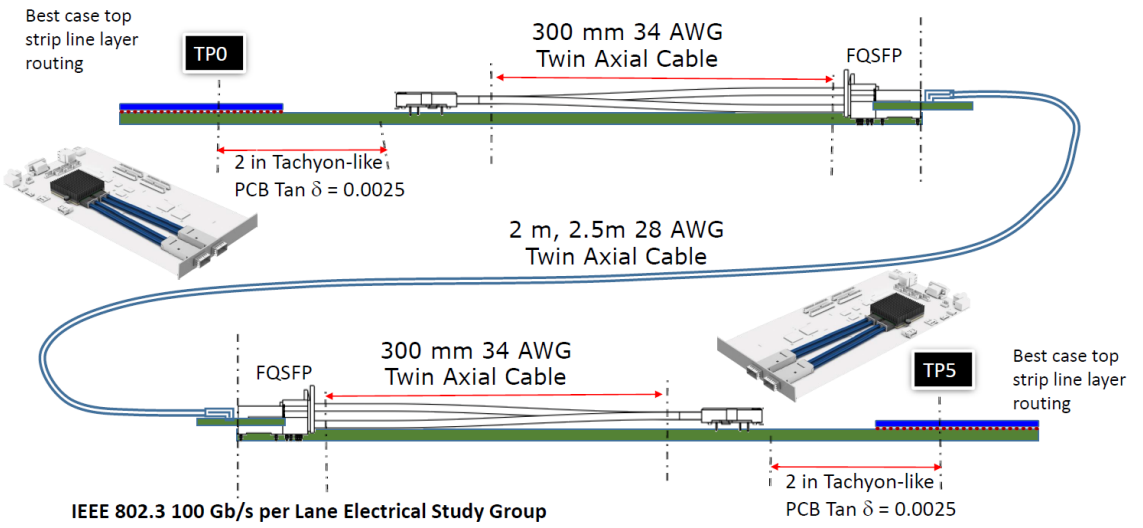


Figure 2.2: Typical Backplane Channel Diagram for 100GbE.



Source: http://www.ieee802.org/3/100GEL/public/adhoc/

Figure 2.3: Cabled Backplane Channel Set-up.

Figure 2.2 shows a typical point-to-point channel topology with cable assembly. The channel comprises the connection between the TX and RX packages (TP0 to TP5). The test point (TP) is the reference point used for the IL budget breakdown. All the losses between TP0 and TP5, due to connectors and cables, are taken into account for the channel IL. A backplane channel configuration is presented in Figure 2.3. This configuration is known as «cabled backplane». It presents lower losses compared to the traditional PCB backplane channel at high frequencies, making it suitable for 112Gb/s operation.

2.2.1 Channel selection

Following the receiver specifications, a channel was chosen to meet the IL constraint at the Nyquist Frequency. Three backplane channels proposed by the IEEE P802.3ck Task Force [6] have been listed in Table 2.2. An orthogonal backplane channel has been added for comparison between the cabled ones. The IL and ICN were calculated using the S-parameters files for a 4-port model. This file is a cascaded form of the different interconnections through the channel. The ICN represents the impact due to both near-end (NEXT) and far-end (FEXT) crosstalk.

The package must be added to complete the backplane channel model. The electrical parameters of the package must achieve stringent requirements in order to support high-speed signals. For that reason, a flexible package model with LC termination compensation has been proposed by the IEEE P802.3ck Task Force.

Table 2.2: Backplane channel for 112Gb/s

Channel	Characteristics	Configuration	IL @ $F_{Nyquist}$	FEXT NEXT	ICN
1	(1.92mm) micro via TP0, TP5 92.5Ω 30AWG: 30mm, 1m	Cabled	28.3dB	5/3	0.69mV
2	24" PCB Megtron-7N STRADA Whisper Conn.	Orthogonal	30.7dB	5/3	0.38mV
3	30AWG Flyover line: 30mm 28AWG: 2m	Cabled	29.5dB	3/4	1.55mV

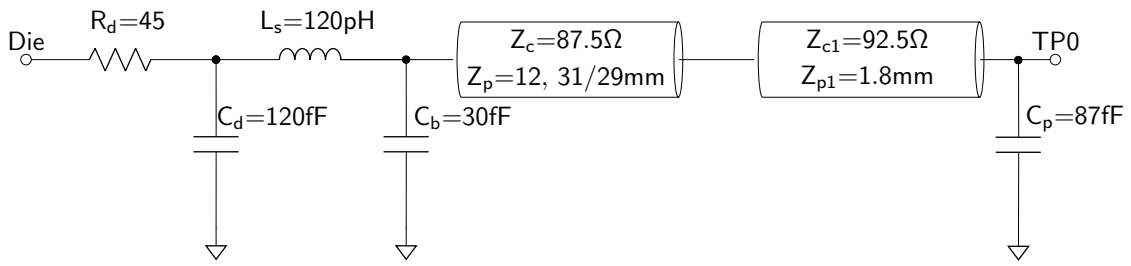


Figure 2.4: Package model.

A single-sided model is presented in Figure 2.4 and will be cascaded with the S-parameters file of the channel. To finalize, a "fitted curve" (up to half of bandwidth, i.e. Nyquist rate) is introduced to approximate the IL as a linear transfer function that will be used in MATLAB. Figure 2.5 shows the insertion loss for the three channels including the fitted version and package. We have chosen the third configuration for our system analysis, as it is the one that presents itself as the most challenging to equalize.

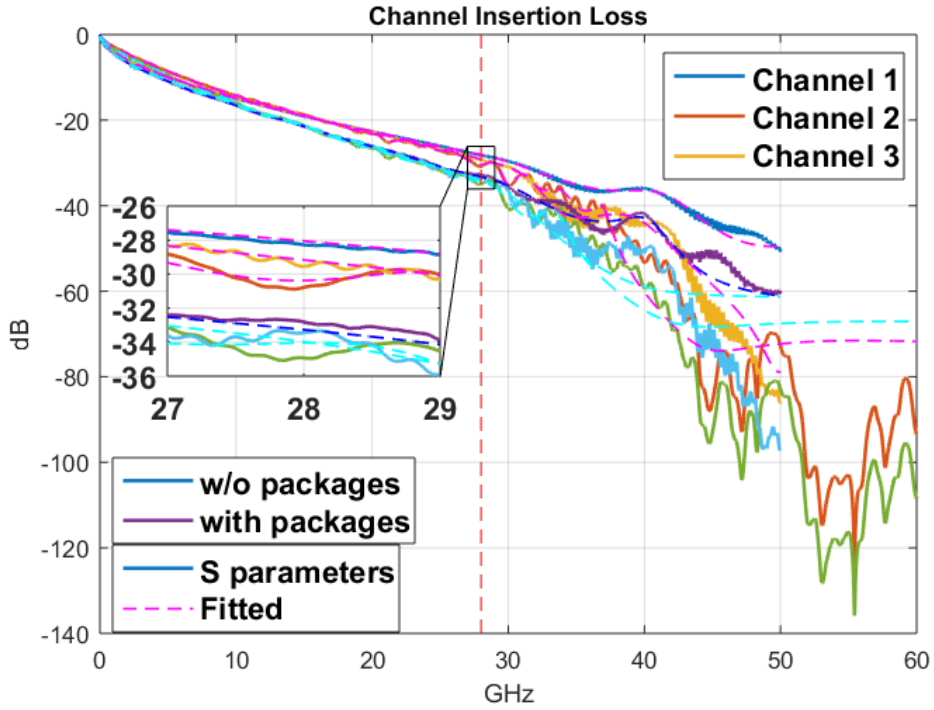


Figure 2.5: Insertion Loss for 3 different configuration channels.

2.3 Channel Equalization at 100Gb/s

After selecting the channel and extracting the pulse response, equalization is evaluated using the techniques described in subsection 1.2.3. Figure 2.6 shows conventional mixed-signal equalization blocks on both the TX and RX. The main cursor in a channel's pulse response is the signal of interest. A FFE, which is typically implemented on the TX side, normally cancels pre-cursors. The post-cursors are often taken care of by the receiver with a CTLE and DFE. The CTLE acts as high-pass filter to compensate for the channel's low-pass action. Due to the high-pass nature of CTLEs, any high frequency receiver input noise will be boosted similar to the actual signal. To avoid excessive noise amplification, DFEs pass the noise-less recovered bits through a FIR filter that matches the post-cursor portions of the channel to achieve ISI cancellation. The TX FFE can also provide some coarse equalization for post-cursors.

As both the links' speed and area requirements become more stringent, mixed-signal architectures pose significant implementation challenges. Specifically, the CTLE and the DFE's summing node are the bottlenecks.

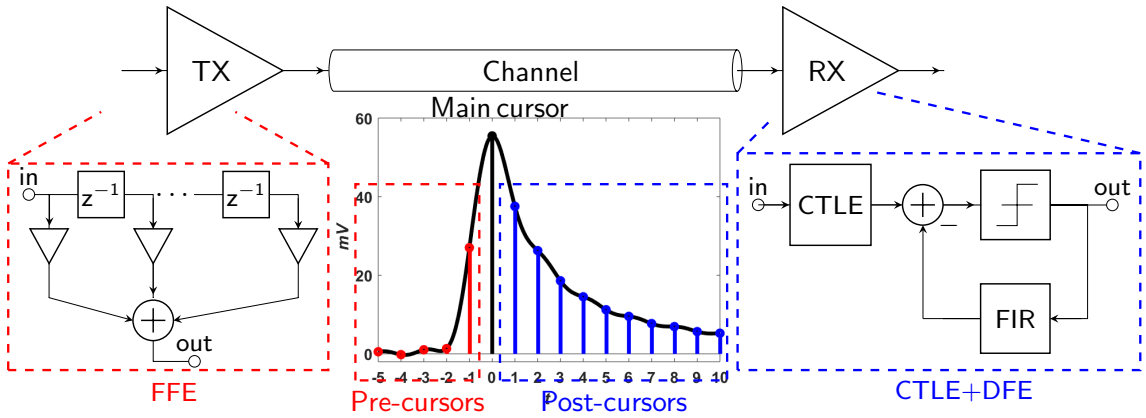


Figure 2.6: Typical equalization scheme for mixed-signal links.

2.3.1 CTLE

The first technique evaluated is the CTLE. Eq. 2.1 presents the transfer function of the CTLE. It consists of a three-poles/two-zeros system.

$$\begin{aligned} H_{CTLE(s)} &= A_{AGC} \cdot \text{prefactor} \cdot \frac{(s+\omega_{Z_1})}{(s+\omega_{P_1})(s+\omega_{P_2})} \cdot \frac{(s+\omega_{Z_{LF}})}{(s+\omega_{P_{LF}})} \\ \text{prefactor} &= \frac{P_1 P_2 P_{LF}}{Z_1 Z_{LF}} \end{aligned} \tag{2.1}$$

where A_{AGC} is the gain for automatic gain control (AGC) stage, ω_{P_1}, ω_{P_2}, ω_{Z_1} are the high frequency two-poles/one-zero that gives the characteristic boost in Nyquist, $\omega_{P_{LF}}$ and $\omega_{Z_{LF}}$ is the low frequency pole/zero pair and its function is to reduce long-tail ISI. Figure 2.7 shows the peaking gain at the Nyquist frequency for the CTLE transfer function. The poles and zeros were normalized to the baud frequency (bd=56GHz).The AGC was set 0.6 (-4.43dB) to avoid saturation at the input of the ADC. For a CTLE bandwidth $\approx p_{2,norm}$= [0.5-0.6]*bd, a peaking gain between [11-21]dB can be achieved.

The CPR with CTLE and transfer function are shown in Figure 2.8. A peak gain of 18.45dB was applied. From the equalized pulse, the suppression of the post-cursors

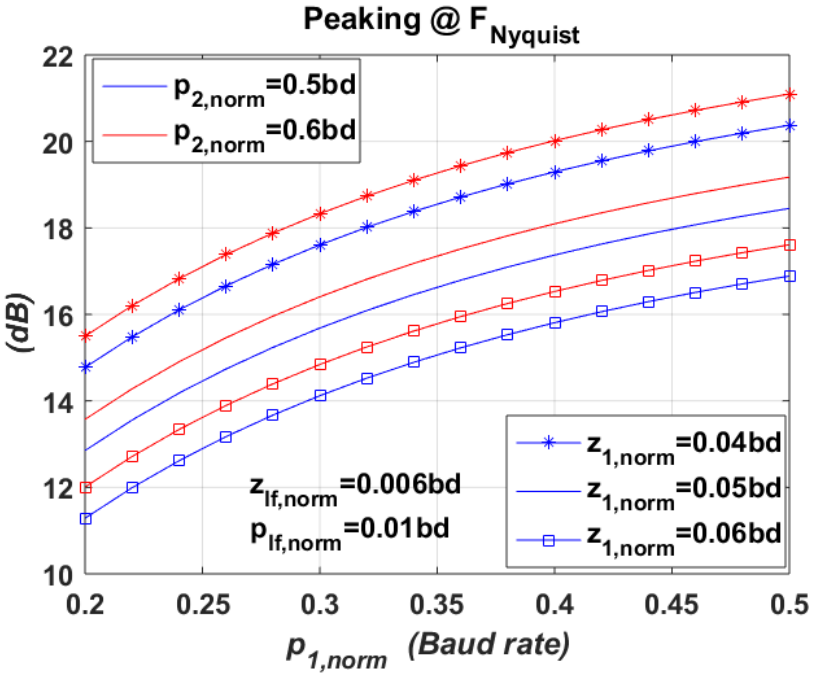


Figure 2.7: CTLE peaking gain at Nyquist: Design space.

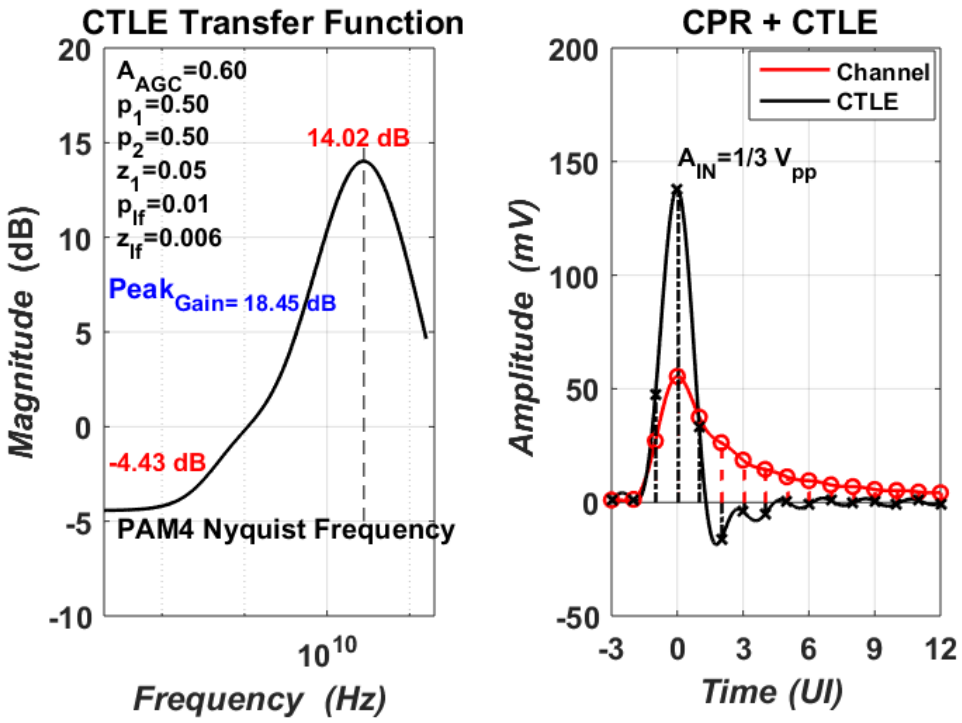


Figure 2.8: CTLE transfer function and Channel Pulse Response+CTLE.

ISIs can be observed.

2.3.2 FFE and DFE

FFE taps were calculated using the procedure described in subsection 1.2.3. For the selected channel a large number post-cursors are required. A total of 32 taps (3-precursors/28-post cursors) were assigned for this channel. Figure 2.9 shows the raw and quantized FFE taps. Quantized taps represent a bit-width FFE in the digital domain. A 3-tap DFE is also evaluated and presented as an example (Figure 2.9). As the UI time decreases, the timing constraints in the design of the DFE become more stringent and challenging to meet. Generally, a 1-tap DFE is used for very high speeds.

Figure 2.10 presents the individual and combined effect of the equalization techniques. For this particular channel, a large number of post-cursors taps are needed. In the following section, FFE and DFE will be applied to the output of the ADC.

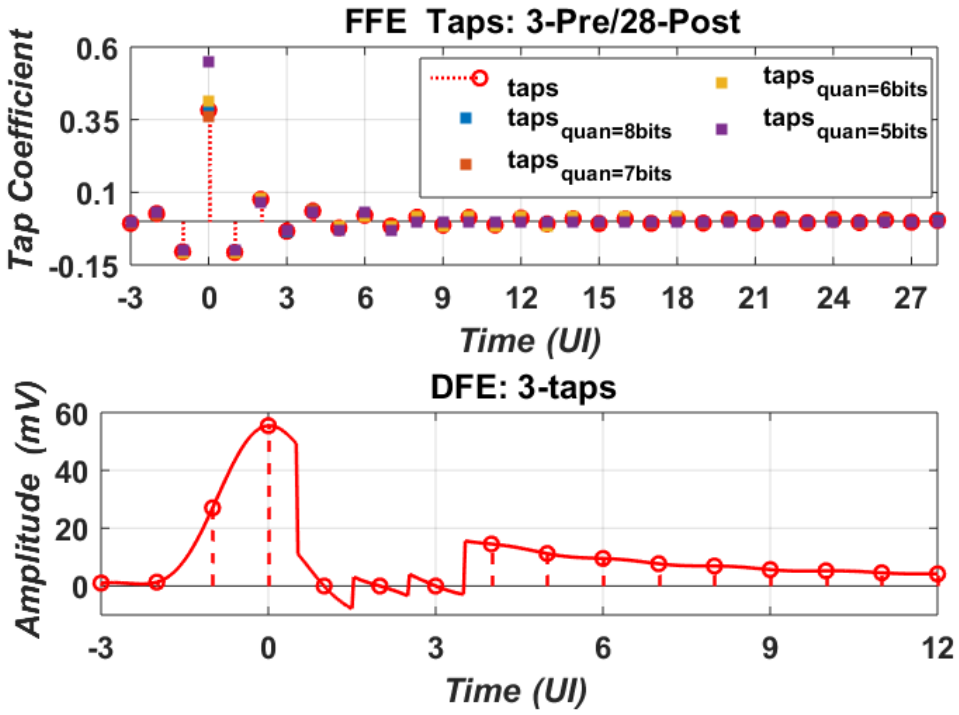


Figure 2.9: FFE and DFE Taps.

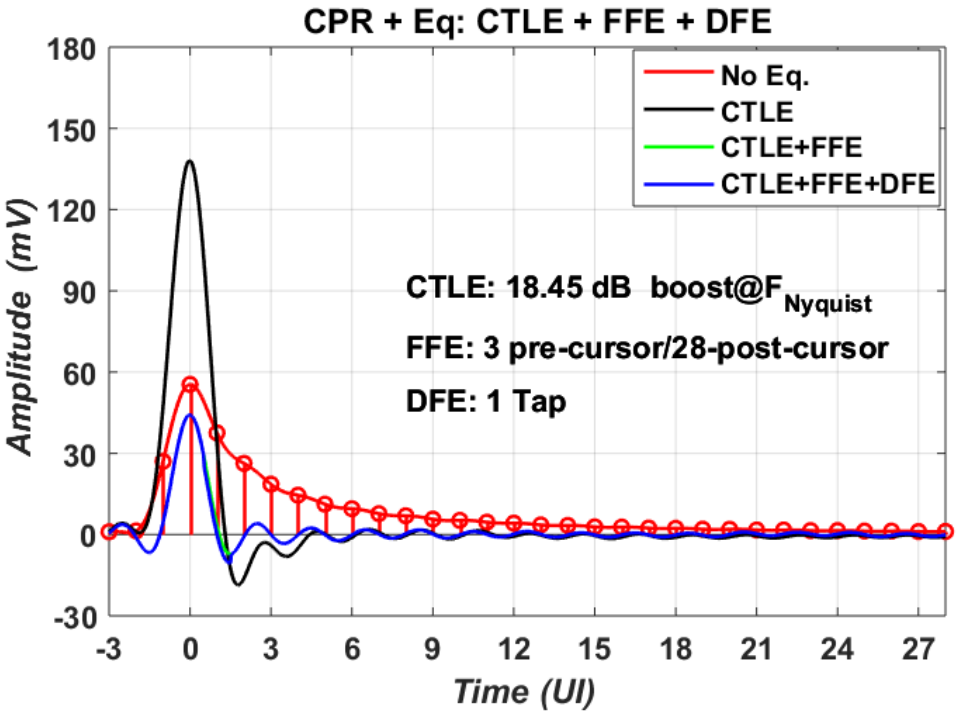


Figure 2.10: CTLE+FFE+DFE applied to the channel.

2.4 Link System Simulation

2.4.1 Link Description

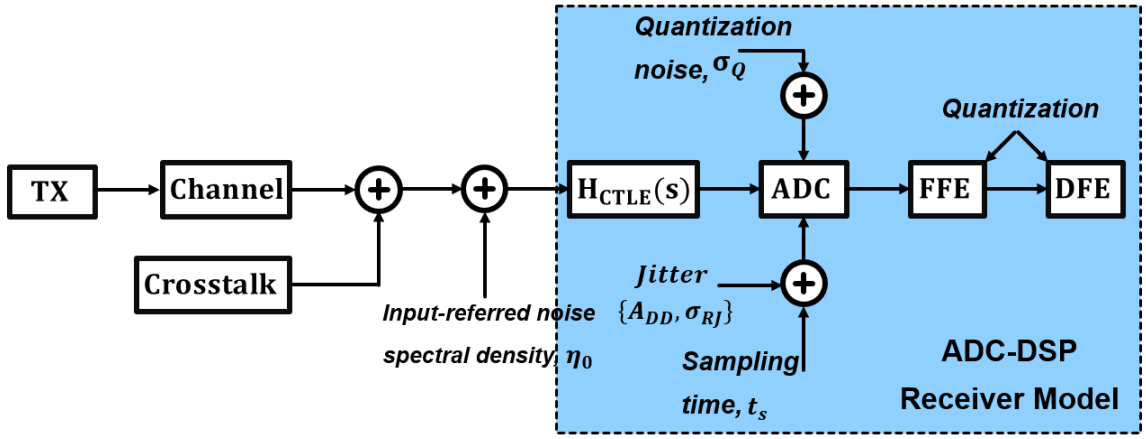


Figure 2.11: Link system diagram including ADC-based receiver.

After defining the specifications for the receiver and selecting the backplane channel, we proceeded to the link simulation in MATLAB Simulink. Figure 2.11 shows the link system diagram, which consists of the following:

- The transmitter (TX): in charge to generate the PAM4 symbols. A Pseudo Random Quaternary Sequence (PRQS) generator using Gray coding was implemented. Additionally, a 3-tap FIR filter was added for de-emphasis. Table 2.3 summarizes the TX parameters.

- The channel (CH): Represented as a rational function extracted from the S-parameters file of channel 3 (Table 2.2) including package.

- Crosstalk (XT): A noise source (ICN) that represents the impact due to both near-end and far-end crosstalk.

- The receiver (RX): A mixed-signal receiver. A CTLE and ADC represent the analog part. Including the noise based on the one-sided spectral density η_0 referred to the CTLE transfer function filter, quantization noise and jitter for

Table 2.3: Transmitter model parameters

Parameter	Symbol	Value	Unit
Test Pattern	PRQS7		
Pattern length		16,383	
PAM4 Coding	Gray		
PAM4 Amplitude	$A_{tx,pam4}$	[-0.5 $\frac{-0.5}{3}$ $\frac{0.5}{3}$ 0.5]	V
3-tap FIR filter	c(-1), c(0), c(1)		
Transmitter SNR noise (RMS)	SNR_{TX}	33	dB

Table 2.4: ADC-DSP receiver model paramaters

Parameter	Symbol	Value	Unit
CTLE Peak Gain@$F_{Nyquist}$	Pk_{Gain}	21	dB
CTLE AGC Gain	AGC_{Gain}	-4.4	dB
ADC input amplitude	A_{adc}	0.5	V
ADC resolution	N_{adc}	7	bit
Quantization Noise	σ_Q	2.3	mV
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
Random jitter	σ_{RJ}	0.01	UI
One-sided noise spectral density	η_0	8.2×10^{-9}	V^2/GHz
FFE weight bit number	N_{ffe}	10	bit
DFE weight bit number	N_{dfe}	10	bit
FFE Post Tap Number	$N_{post-ffe}$	28	
FFE Pre Tap Number	$N_{pre-ffe}$	3	
DFE Tap Number	N_b	1	
Samples per UI[1]	M	32	

[1]Relevant for PR only

the ADC. The DSP includes a FFE 32-tap FIR filter and 1-tap DFE. Both are N bit-wide. Table 2.4 lists the RX used parameters.

2.4.2 PAM4 BER calculation based on PDF estimation

The BER is used to evaluate the link's performance. To calculate the BER, we start with a Gaussian random variable (X) that has a Probability Density Function (PDF) defined by

$$p_X(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}(\frac{x-\mu}{\sigma})^2} \tag{2.2}$$

where μ and σ are the mean offset and variance, respectively. X represents a detected symbol (or bit) μ with a certain noise power σ. Figure 2.12 shows X distribution. *A* is the lower threshold that gives the probability of a right symbol detection. The area denoted by x≤A represents the probability error P(x≤A) or BER, to make a wrong symbol detection.

P(x≤A) can be calculated using the Cumulative Distribution Function (CDF)

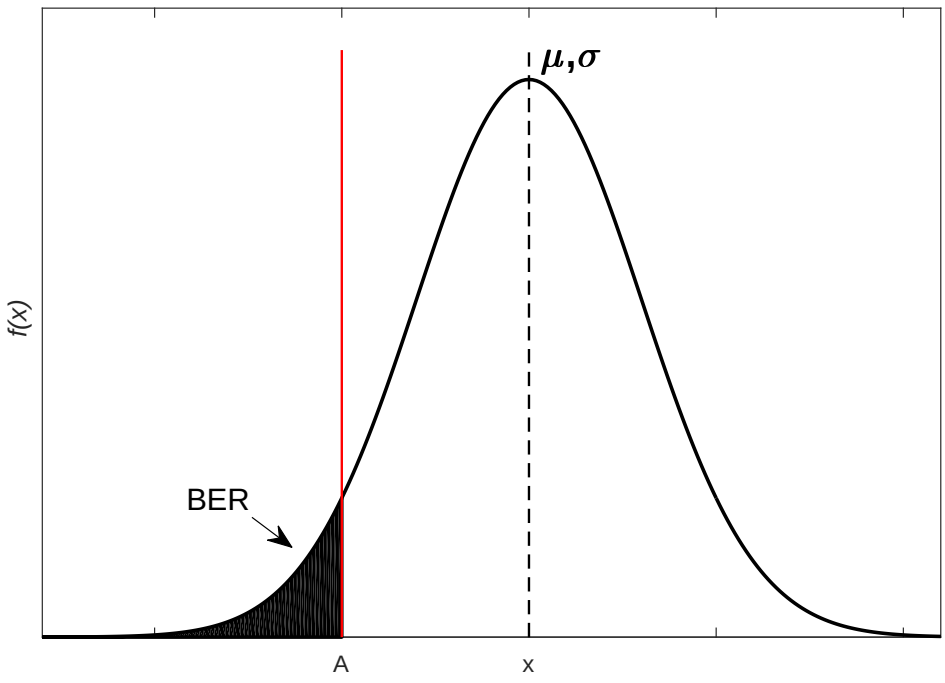


Figure 2.12: Gaussian random variable distribution and BER.

defined by

$$F_X(x) = \int_{-\infty}^{x=A} \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}(\frac{x-\mu}{\sigma})^2} dx \tag{2.3}$$

The CDF is the integral of the PDF (always, not just for Gaussian). Often the $Q(\cdot)$ function is used interchangeable with CDF for the purpose of BER estimation. $Q(\cdot)$ tells us the probability of X is greater than or equal to some number A: $P(x \geq A) = Q(A)$

$$Q(y) = \frac{1}{\sqrt{2\pi}} \int_{y=A}^{\infty} e^{-\frac{x^2}{2}} dx = 1 - F_X(y) \tag{2.4}$$

In general for a random varible X

$$\begin{aligned} P(X > x) &= Q(\frac{x-\mu}{\sigma}) \\ P(X \leq x) &= 1 - Q(\frac{x-\mu}{\sigma}) \end{aligned} \tag{2.5}$$

Another important relationship

$$Q(x) = 1 - Q(-x) \tag{2.6}$$

$Q(\cdot)$ is also closely related to the error function (erf) and complementary error function (erfc)

$$\begin{aligned} erfc(x) &= \frac{2}{\sqrt{\pi}} \int_{x}^{\infty} e^{-x^2} dx = 2Q(x\sqrt{2}) \\ Q(x) &= \frac{1}{2} erfc(\frac{x}{\sqrt{2}}) = \frac{1}{2}[1 - erf(\frac{x}{\sqrt{2}})] \end{aligned} \tag{2.7}$$

The PDF of a PAM4 signal is shown in Figure 2.13. The PAM4 levels [0, 1, 2, 3] are represented as random variables with Gaussian distribution (μ_N, σ_N). DL, DZ and DH are the slicers thresholds for the PAM4 signal detection. The area under the curves crossed-over portions gives the probability of a wrong symbol decision or Symbol Error Rate (SER).

$$\begin{aligned} SER_{PAM4} = &\frac{1}{4}P_0(x > DL) + \frac{1}{4}P_1(x \leq DL) + \frac{1}{4}P_1(x > DZ) \\ &+ \frac{1}{4}P_2(x \leq DZ) + \frac{1}{4}P_2(x > DH) + \frac{1}{4}P_3(x \leq DH) \end{aligned} \tag{2.8}$$

Applying Eqs. 2.5 and 2.6 into Eq. 2.8:

$$\begin{aligned} SER_{PAM4} = &\frac{1}{4}Q(\frac{DL-\mu_0}{\sigma_0}) + \frac{1}{4}Q(\frac{\mu_1-DL}{\sigma_1}) + \frac{1}{4}Q(\frac{DZ-\mu_1}{\sigma_1}) \\ &+\frac{1}{4}Q(\frac{\mu_2-DZ}{\sigma_2}) + \frac{1}{4}Q(\frac{DH-\mu_2}{\sigma_2}) + \frac{1}{4}Q(\frac{\mu_3-DH}{\sigma_3}) \end{aligned} \tag{2.9}$$

Eq. 2.9 can be simplified assuming PAM4 levels have the same PDF (μ, σ), DZ=0 , DL=–2μ and DH=2μ

$$SER_{PAM4} = \frac{6}{4}Q(\frac{\mu}{\sigma}) \tag{2.10}$$

the term $\frac{\mu}{\sigma}$ is related to the SNR of the receiver (SNR_{RX}). Eq. 2.10 can be expressed in terms of SNR_{RX}

$$\begin{aligned} SNR &= \frac{P_{avg,signal}}{P_{avg,noise}} = \frac{5\mu^2}{\sigma^2} \\ SER_{PAM4} &= \frac{6}{4}Q(\sqrt{\frac{SNR}{5}}) \end{aligned} \tag{2.11}$$

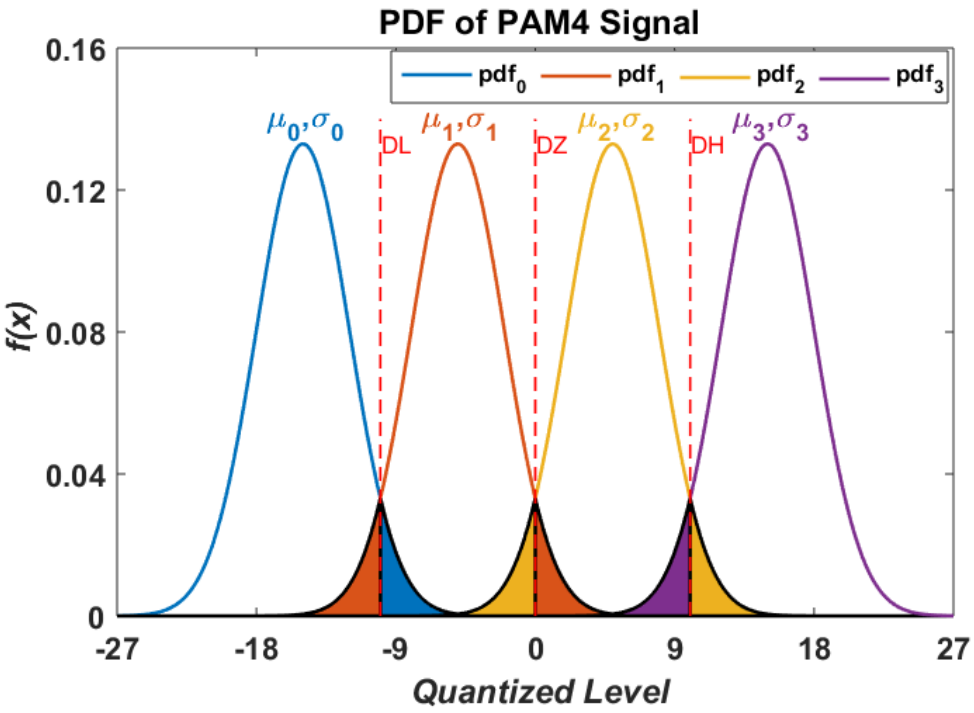


Figure 2.13: Example PDF of PAM4 ADC output signal.

BER is related to SER, but is also related to the coding scheme. Using Gray coding only one bit error per symbol is made for incorrect decisions. Thus, BER is half of SER for PAM4 signaling adopting gray coding.

$$\mathrm{BER}_{\mathrm{PAM4,gray-coding}} = \frac{\mathrm{SER}_{\mathrm{PAM4}}}{2} = \frac{3}{4}\mathrm{Q}(\sqrt{\frac{\mathrm{SNR}}{5}}) \tag{2.12}$$

This expression is the same as presented in Eq. 1.1, interchanging the function $\mathrm{Q}(\cdot)$ for *erfc*. For simplicity, the system simulations refer only to BER.

2.4.3 Simulation results

Figure 2.14 depicts the simulink model to evaluate the receiver. As described in section 1.2.2, it includes a CDR: a PLL loop extracts the clock signal from the output of the CTLE and sends it to the ADC and DSP.

The link was tested using $5{\times}10^5$ symbols with a PRQS7 pattern and noise in the transmitter. De-emphasis was not implemented because the large number of RX FFE taps is dominant in the equalization. The histograms of the channel, CTLE and ADC are shown in Figure 2.15. The CTLE performs two functions: giving a gain boosting at Nyquist and controlling gain to avoid signal clipping. The ADC quantization helps to restore some of the transmitted signal and also to define the slicers threshold (DL, DZ, DH) in the DFE. The ADC output is equalized in the digital domain using FFE and DFE. The equalized histogram is shown in Figure 2.16. FFE taps were calculated

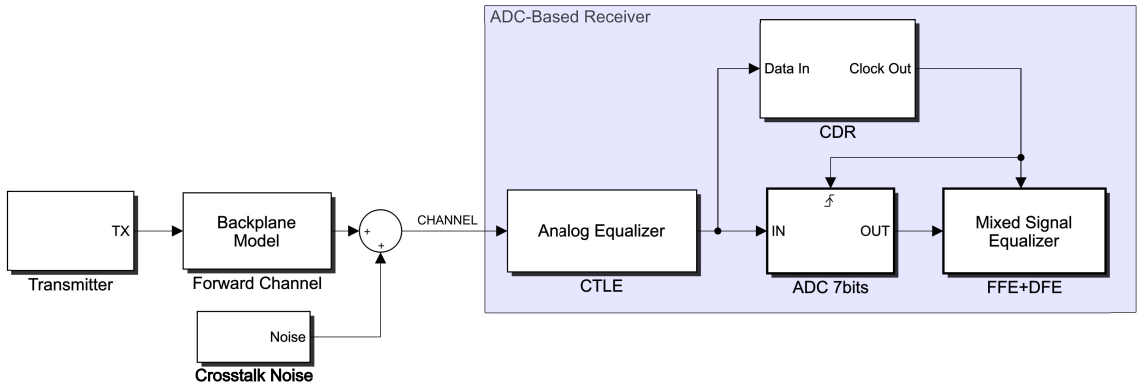


Figure 2.14: High speed serial link simulink model.

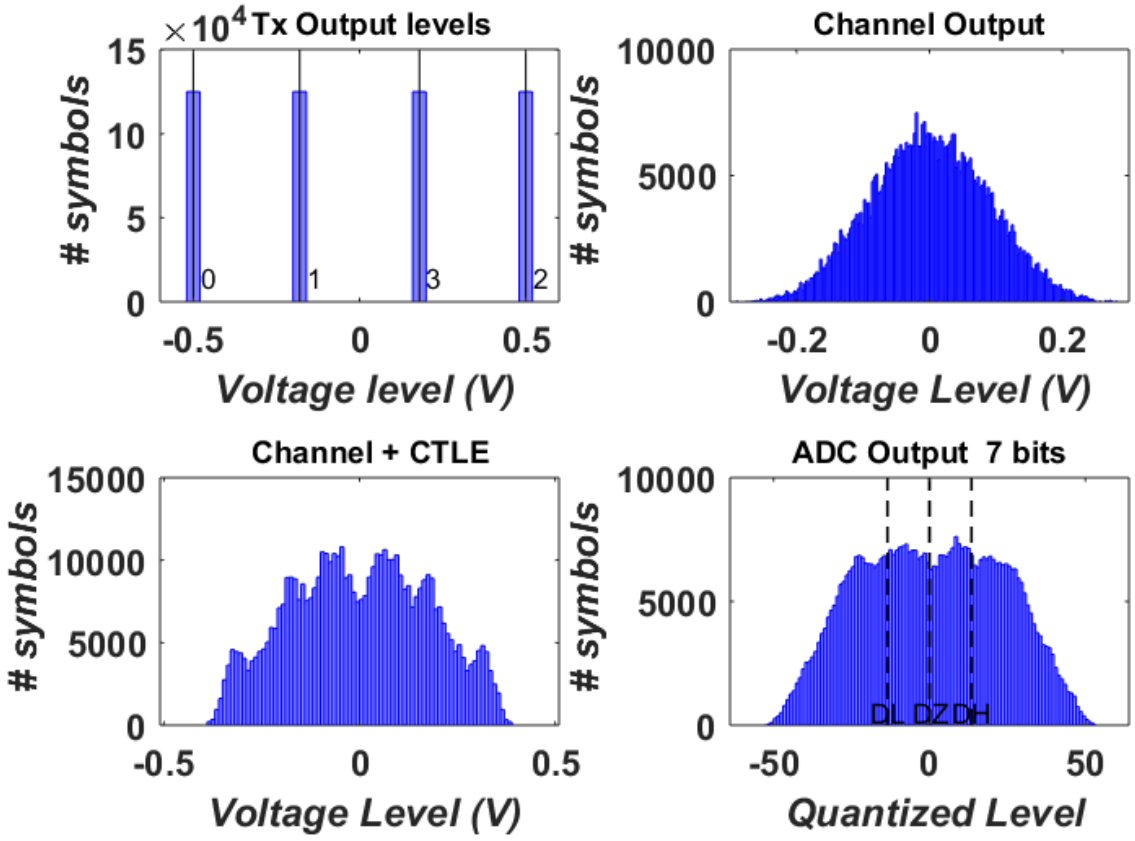


Figure 2.15: Transmitted symbols: channel, CTLE and ADC.

using 10-bit-wide operations. The output of the receiver is decoded to its correspondent PAM4 level and compared to the transmitted symbols.

The output of the receiver before decoding is presented in Figure 2.17. It can be seen that the DFE output levels fall between four distinct groups, $\text{Level}_{0,1,2,3}$, that represent the PAM4 symbols. $\text{Level}_{0,1,2,3}$ groups are created using the slicer's threshold as reference. In order to calculate the BER, each $\text{Level}_{0,1,2,3}$ group is represented as a RV (μ and σ) with a PDF extracted from the quantized values within each group. Figure 2.18 shows the PDF for each $\text{Level}_{0,1,2,3}$ with a BER calculated using Eq. 2.9.

A BER parametrization has been evaluated under two conditions:

1. Fixed CTLE peak gain and FFE weight bit number. For this condition, the impact of the number of FFE post-taps and DFE was evaluated,

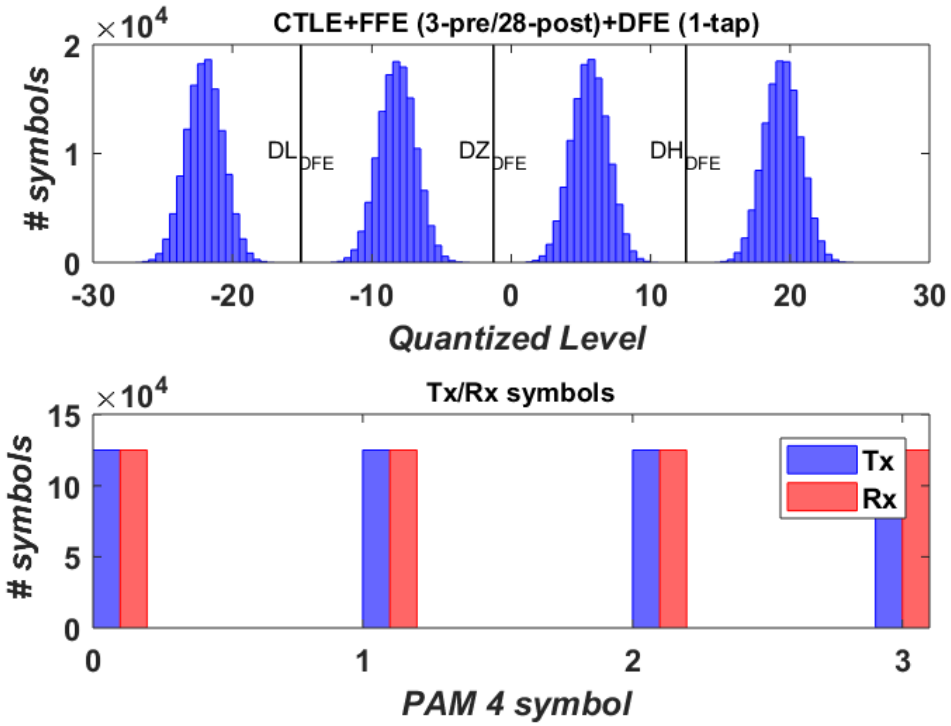


Figure 2.16: Symbols after (FFE+DFE) and comparison between TX and RX symbols.

2. Fixed FFE 3pre-/28post-taps and 1 DFE tap. Varying the CTLE peak gain and the FFE weight bit number.

The parametrization results are shown in Figure 2.19. For the first condition, DFE has an impact of two orders of magnitude on the BER and it presents linear decrements for higher number of FFE post-taps. Although FFE is enough to meet the BER specification range (1×10^{-4} to 1×10^{-5}), the receiver still will use DFE for more stringent specifications. For the second, a minimum peak gain of 19dB is necessary to comply with the BER specification range. For the FFE weight bit number, a resolution higher than 5 bits should be enough to meet the BER.

The feasibility of an ADC-based receiver that meets Long Reach (LR) applications for 112Gb/s through the selection of a physical backplane channel. A demonstration is made by performing a link system simulation.

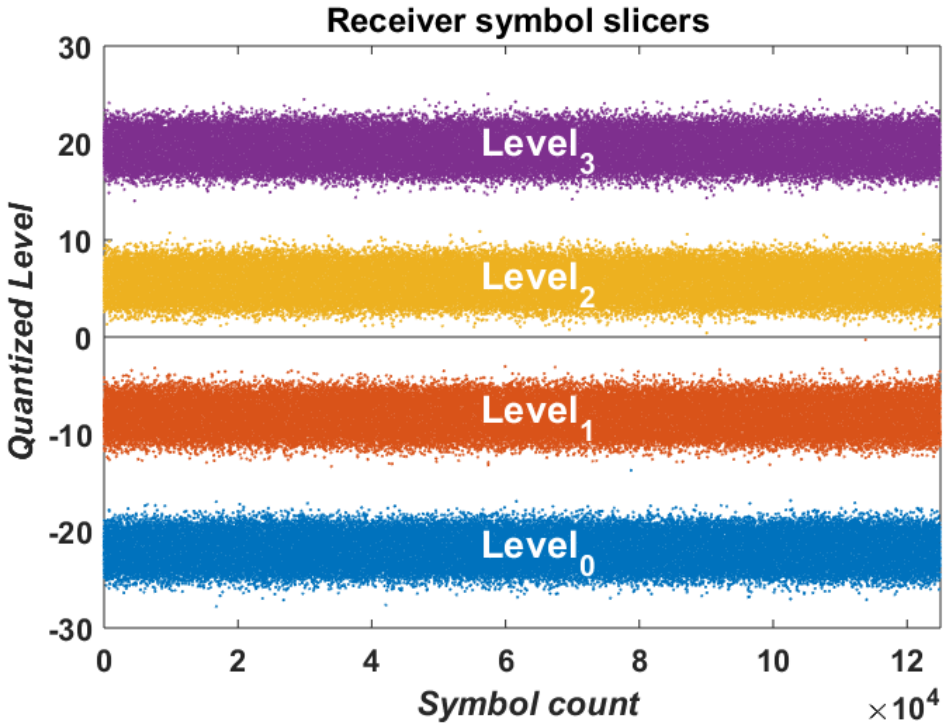


Figure 2.17: Sampled equalized symbols at the RX output.

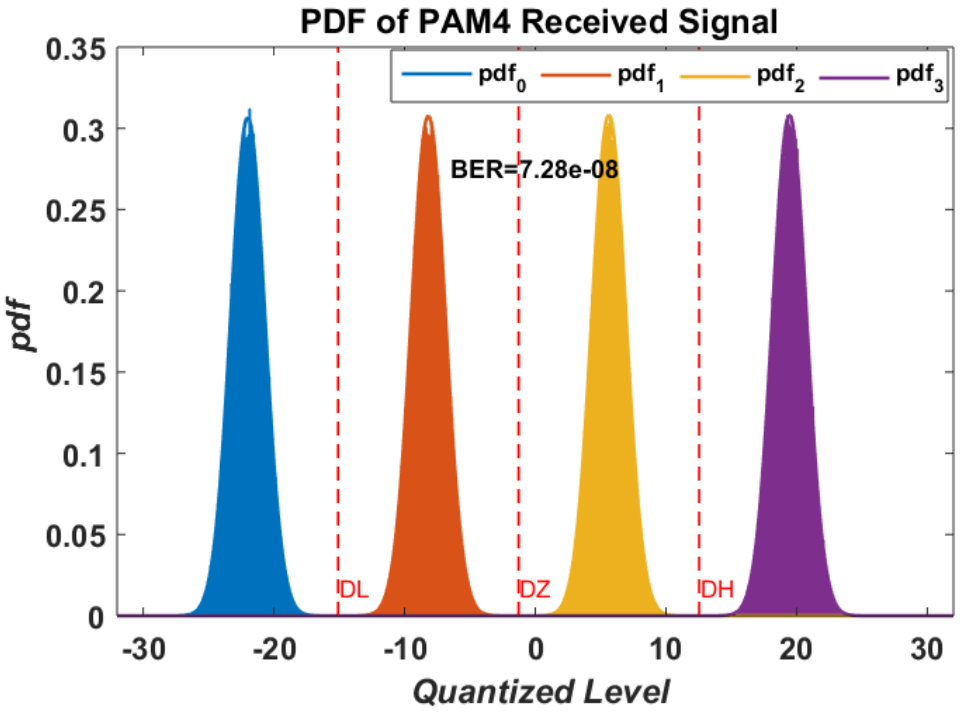


Figure 2.18: PDF of PAM4 RX output signal.

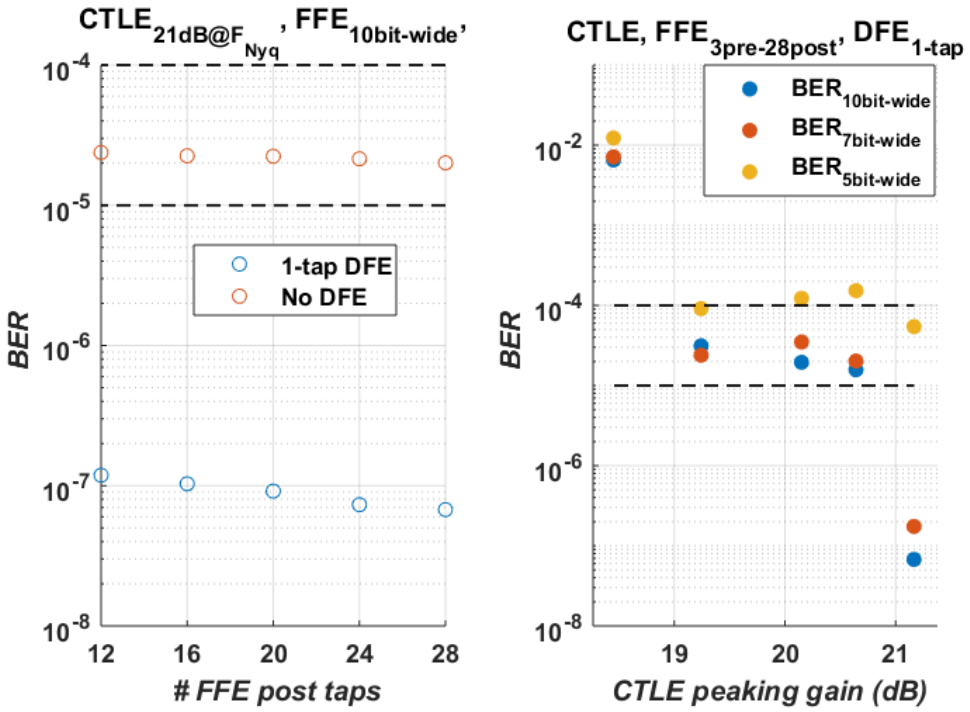


Figure 2.19: BER Parametrization: FFE post-taps and CTLE peaking gain.

2.5 Conclusion

This chapter has presented a methodology to evaluate receiver's specifications using link system analysis. A complete high-speed serial link in MATLAB Simulink was implemented for simulation. Through link simulation a wireline receiver with the following characteristics has been validated:

- **PAM4 modulation:** multi-level signaling is needed to overcome bandwidth limitation of NRZ modulation,
- **ADC-based architecture:** mixed-signals were most of the equalization is implemented in the digital domain will be the norm for speed beyond 100Gb/s,
- **CTLE:** the AFE of the receiver will require an analog equalizer for gain boosting and signal conditioning before the ADC,
- **FFE + DFE:** due to the high channel losses, a combination of long FFE taps with one-tap DFE presents the best solution to cancel ISI,
- **Long Reach applications:** the receiver is capable to equalize input data with channel losses close and up to 30dB,
- **Raw BER:** through a combination of CTLE, FFE and DFE applied to an ADC-based architecture, the BER is within the specified range of 1×10^{-4} to $1\times10\times^{-5}$.

These characteristics are compatible with the latest CMOS technologies which will allow a full-integrated solution. Chapter 3 presents the design of the core of the receiver -the ADC- and the the clock generation circuit.

Chapter 3

7b 56GS/s Hierarchical Time-Interleaved SAR ADC

Contents

This chapter presents the design of a 56GSample/s Time-Interleaved ADC for ADC-based wireline receivers. The first subsection describes the concept of TI-ADCs, state-of-the-art and same design considerations. The following subsections cover design, clock generation and simulation results.

3.1 Design Flow

Some guidelines for the design of a high-speed TI-ADC are defined. Figure 3.1 presents the TI-ADC design flow. It is described as follows:

- A theoretical revision and state-of-the-art trends on TI-ADCs is conducted,
- the design procedure is divided in: hierarchical Track-and-Hold (TH), clock generation and sub-ADC design,
- the number of TH ranks are chosen to minimize the amount of low-jitter sampling clocks. Then, the TH stages are designed,
- the sampling clocks are designed accordingly to the hierarchical TH,
- the sub-ADC resolution is calculated based on the system level SNR. Then, the architecture is chosen to complete the sub-ADC design,
- the TI-ADC is assembled and simulated. Specifications are verified to comply with the design.

3.2 Time-Interleaved ADCs

3.2.1 Fundamentals of Time-Interleaved ADCs

High-speed data converters aiming for or above 1GS/s often use a Time-Interleaved (TI) architecture [28] to achieve the highest sample rate. One method to compare the performance of ADCs is by using a Figure-Of-Merit (FOM), which is applicable on

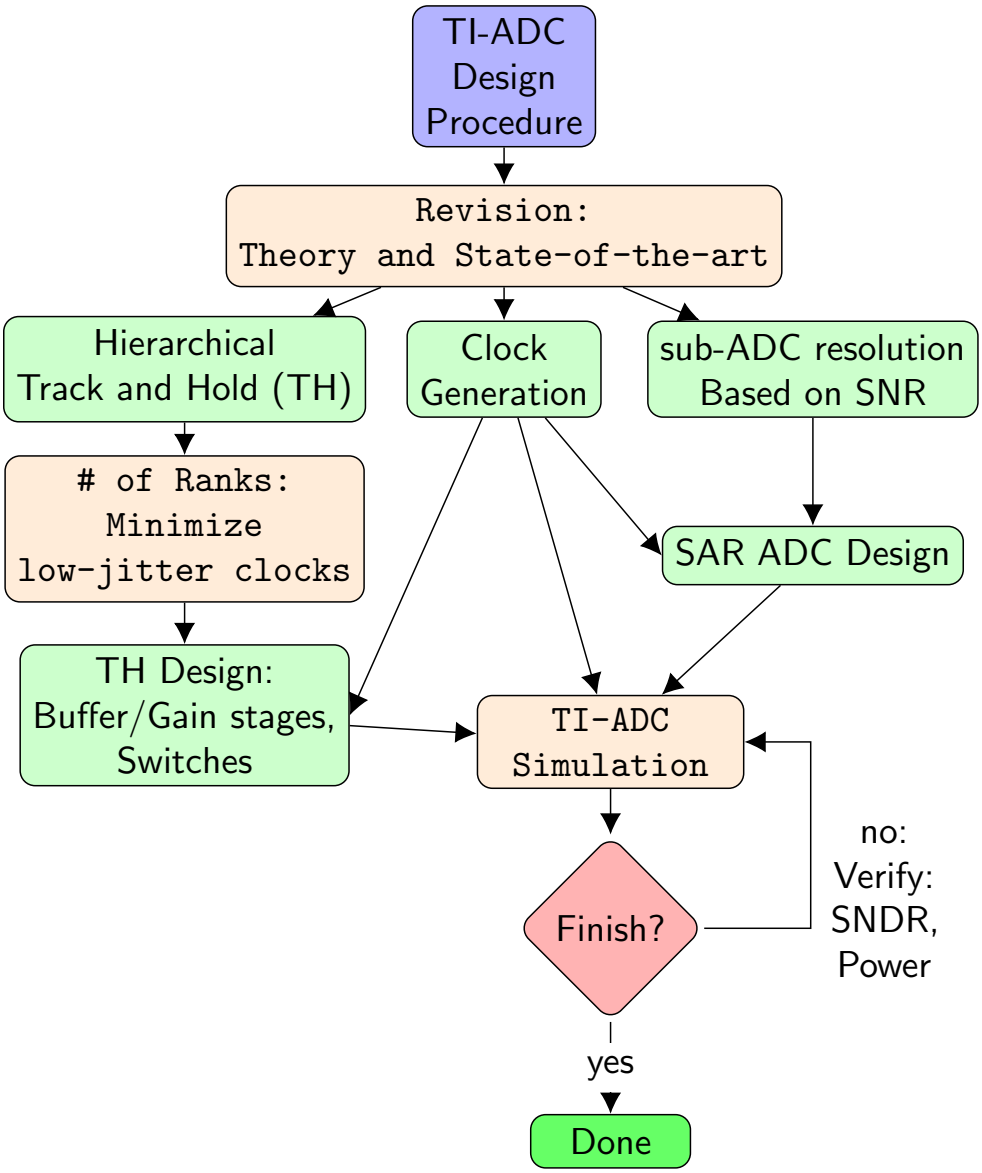


Figure 3.1: Time-Interleaved ADC design flow

all converter architectures and is used to show the ongoing trends in ADC designs. A well-used FOM is the Walden FOM (FOM_W), defined as

$$FOM_W = \frac{P}{2^{ENOB} \cdot F_S} \tag{3.1}$$

where F_S is the full sampling rate, ENOB is the effective number of bits and P is the total power consumption of the converter.

Figure 3.2 shows the FOM_W versus the Nyquist sampling rate ($f_{s,nyq}$) for all ADCs

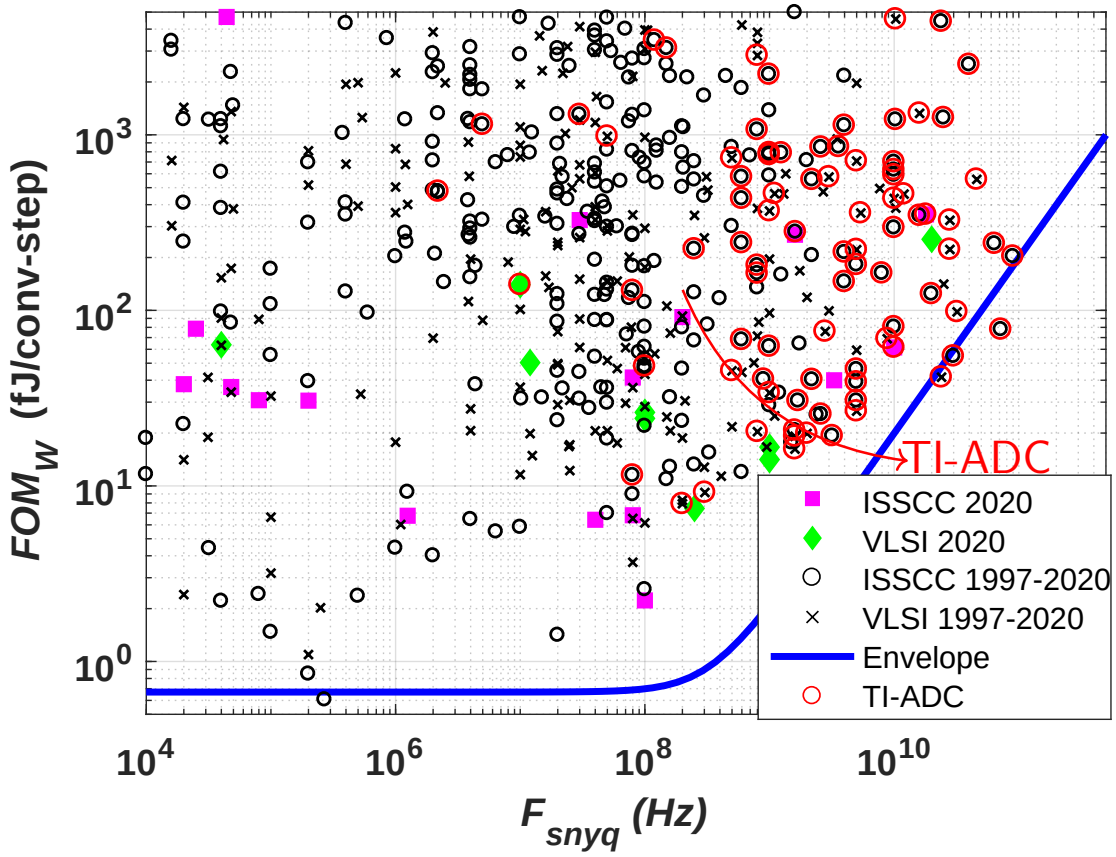


Figure 3.2: Walden FOM versus Nyquist sampling rate.

published in ISSCC and VLSI [29], [2]. ADCs implementations for $f_{s,nyq}$ above 1GHz are predominant TI architectures. The reason behind it is that TI enables more energy-efficient designs than Flash ADC.

Figure 3.3a shows an example of TI-ADC architecture. It consists of M identical sub-ADCs operating together in time-multiplexed mode. The sub-ADC in each time-interleaved path operates at a sampling frequency of F_s/M, where F_s denotes the overall equivalent sampling frequency of the whole system. A graphical representation of the clock signals in a TI-ADC is depicted in Figure 3.3b. The sampling clocks applied to each path are delayed respectively by one overall sampling period $T_s=1/F_s$, thus each subsystem samples the analog input signals in an alternative manner. By employing time-multiplexing architectures the effective sampling rate can be multiplied by the number (M) of TI paths. The main benefit of the TI architecture is that

the overall sample-rate can be very high, while the sub-ADCs only need a moderate sample-rate enabling a high power efficiency.

In principle, the operating speed of the TI-ADC can grow linearly by increasing the number of parallel ADC channels. However, various types of mismatches among different channels create modulation tones which degrade the performance of the TI-ADC, like offset, gain, timing as well as bandwidth mismatches [30],[31]. The timing-mismatch is the largest problem in high-speed TI-ADCs. All these limitations occur in the frequency domain as spurious tones and therefore degrade the Spurious Free Dynamic Range (SFDR) and the Signal-to-Noise-and-Distortion Ratio (SNDR) of the TI-ADC.

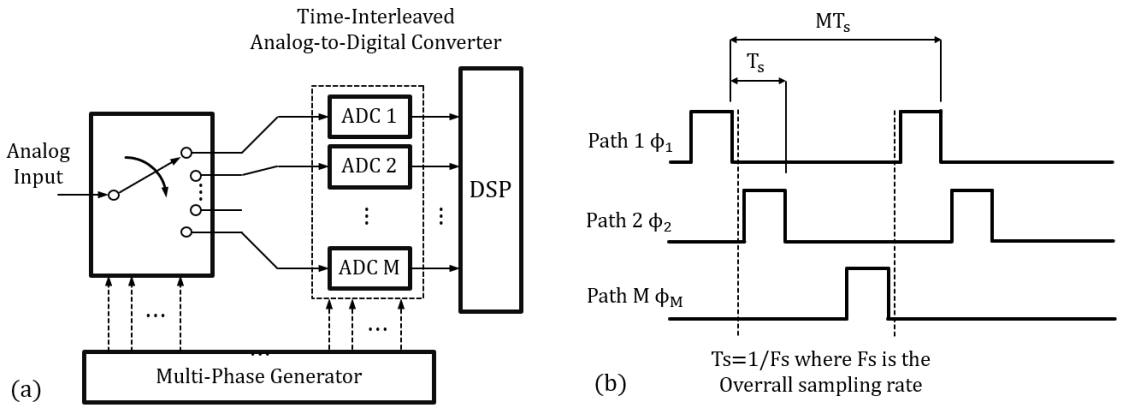


Figure 3.3: A TI-ADC: (a) The overall system architecture. (b) timing diagram.

Table 3.1: Mismatches in TI-ADCs

Mismatches		
Offset	Gain	Timing
Generates spurs		
Location dependent on number of channels	Location dependent on number of channels and input frequency	
Independent of signal amplitude	Power of spurs dependent on signal amplitude	
Independent of input frequency	Power of spurs independent of input frequency	Power of spurs dependent on input frequency

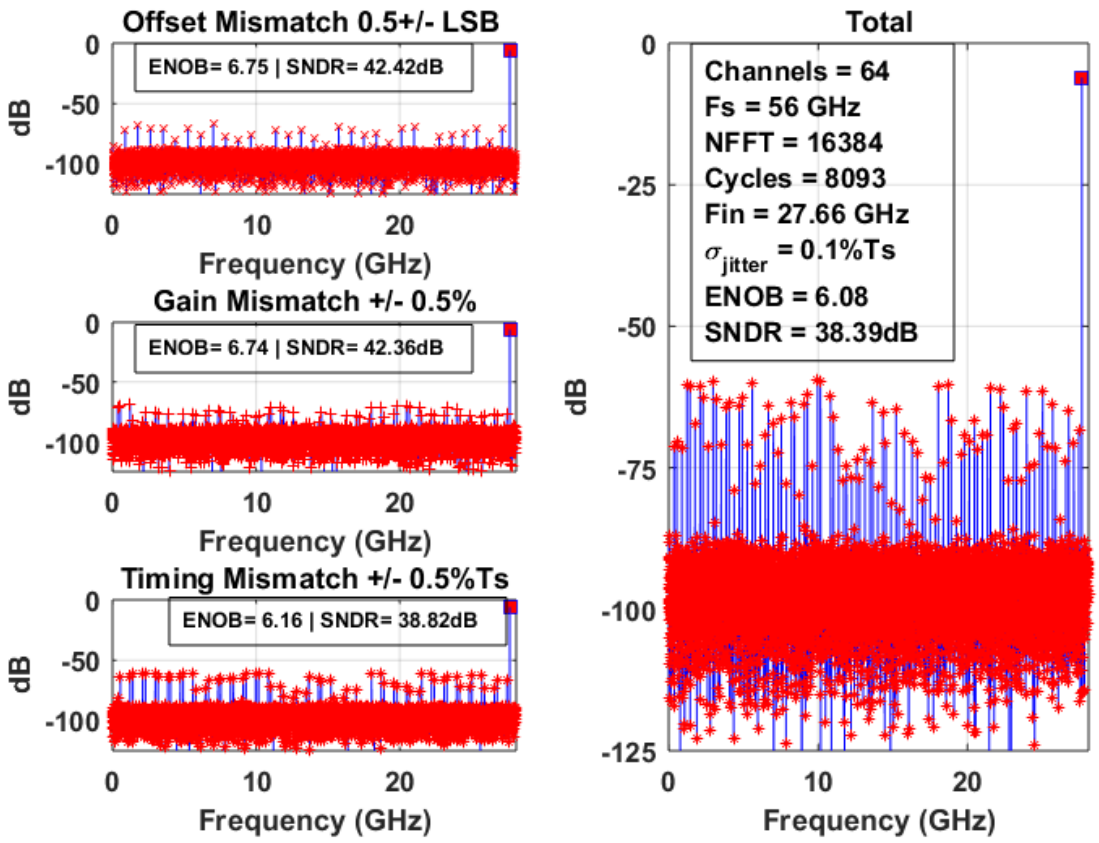


Figure 3.4: Time-interleaved ADC mismatches example: Offset, gain, timing and all mismatch errors. F_{in}=27.66GHz 16384 point FFT.

An overview of the spectral signatures of the mismatches in TI-ADCs is given in Table 3.1. A simulation of the TI-ADC (coherent sampling of a sine wave at Nyquist frequency) was performed with sampling rate F_s=56GS/s, M=64, 7-bit resolution and sampling jitter, σ_{jitter}=0.1%T_s. Offset, gain and timing mismatch were modeled as a random numbers within a pre-defined range.

The output spectrum for each individual error and combined mismatch errors is shown in Figure 3.4. Timing mismatch is the dominant error source. For this reason, special care must be taken in the clock routing and distribution.

3.2.2 Signal-to-Noise

As the ADC rounds the signal to the closest level, a triangular shaped error signal will arise. This saw-tooth signal is the fundamental quantization error and varies linearly from $+0.5A_{LSB}$ and $-0.5A_{LSB}$. The PDF is assumed constant and uniformly distributed. The quantization error power (P_Q) is determined by calculating the estimation value for the variance and yields:

$$P_Q = \frac{A_{LSB}^2}{12} = \left(\frac{\text{full} - \text{scale}}{2^N\sqrt{12}}\right)^2 \tag{3.2}$$

where A_{LSB} refers to the size of the least significant bit, "full-scale" is the analog range of the conversion and N the resolution.

Often in analog-to-digital converters sinusoidal signals are used to characterize the performance. The quantization error is related to the maximum sinusoidal signal ($A\sin(\omega t)$) that the analog-to-digital converter can handle [32]. The quantization errors of the analog-to-digital converter are considered uncorrelated. The resulting noisy spectrum is modeled as a white noise spectrum, whose power is contained between f=0 and $f=f_s/2$ and mirrored around the multiples of the sample rate.

The SNR compares the noise power in a full sine wave as

$$SNR = 10 \cdot \log_{10}\left(\frac{P_{signal}}{\text{Noise power}}\right) \tag{3.3}$$

P_Q can be used to calculate an equivalent SNR

$$\begin{aligned} P_{signal} &= \frac{1}{T}\int_{t=0}^{t=T} A^2\sin^2(\omega t)\,dt = \frac{A^2}{2} = \frac{2^{2N}A_{LSB}^2}{8} \\ SNR_{mag} &= \frac{P_{signal}}{P_Q} = \frac{3}{2}2^{2N} \\ SNR_{dB} &= 10 \cdot \log_{10}\left(\frac{3}{2}2^{2N}\right) = 1.76 + N \times 6.02dB \end{aligned} \tag{3.4}$$

Eq. 3.4 is an approximation that is often used in ADC design. It defines the maximum SNR represented by a digital word of N bits in a bandwidth of $f_s/2$.

The SNDR stands for the ratio of the signal power to all the unwanted components: quantization errors, thermal noise, distortion, timing mismatch[31].

$$SNDR = 10 \cdot \log_{10}\left(\frac{\text{Power of 1st harmonic}}{\text{Power of all unwanted components}}\right) \tag{3.5}$$

The SFDR is the distance between the signal and the largest single unwanted component, the spurious signal. In order to characterize the converter in a simple manner, the Effective Number Of Bits (ENOB) is calculated by reversing Eq. 3.4:

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02} \tag{3.6}$$

The ENOB allows an easy comparison of the real performance of an ADC. Another well-used FOM is the Schreier FOM ($\mathrm{FOM_S}$)

$$\mathrm{FOM_S} = \mathrm{SNDR} + 10 \cdot \log_{10}(\frac{\mathrm{BW}}{\mathrm{P}}) \tag{3.7}$$

which uses the SNDR, signal bandwidth (BW) and the total power consumption P.

3.2.3 ADC resolution estimation

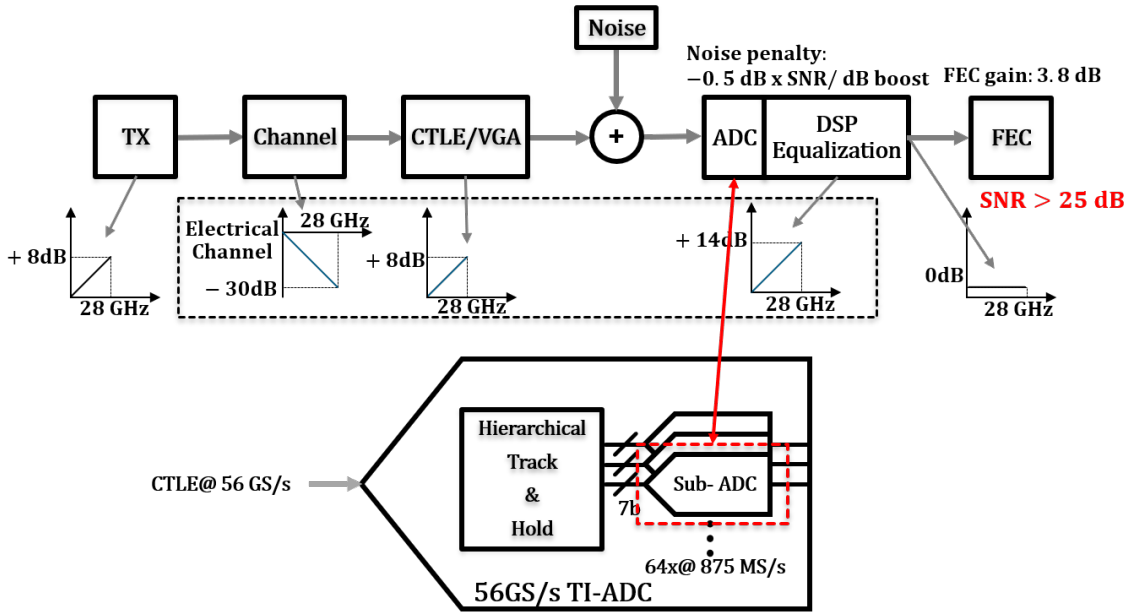


Figure 3.5: sub-ADC in a TI System.

In the previous chapter, the ADC used in the system simulation had a pre-defined resolution of 7 bits. The resolution of the TI-ADC will be calculated using the BER at the output of the receiver (pre-FEC or raw BER). Figure 3.5 depicts the link budget for an ADC-based receiver. In contrast to the model in chapter 2, the gain at Nyquist

frequency have been distributed between TX and RX, which corresponds to a more realistic implementation.

The TI-ADC is designed to meet the SNR requirements for 56GBaud PAM4 signaling. Forward Error Correction (FEC) will be used to improve link integrity and counteract physical layer level errors introduced by reduced SNR in PAM4 signaling [33].

In the previous chapter, a target pre-FEC BER range of [1×10^{-4} - 1×10^{-5}] was used. For this scenario, a BER=1×10^{-6} (adding additional margin) over 30dB loss channel was employed. We start calculating the output SNR, which corresponds to a post-FEC BER=1×10^{-15}, using Eq. 1.1[1], [7]:

$$\mathrm{BER_{post,FEC}} = 1 \times 10^{-15} = \left(\frac{3}{8}\right) \times \mathrm{erfc}\left(\sqrt{\frac{\mathrm{SNR}}{10}}\right) \qquad \mathrm{SNR} \approx 25\mathrm{dB} \tag{3.8}$$

For a FEC gain of 3.8dB, the pre-FEC BER is

$$\underbrace{25\mathrm{dB}}_{\mathrm{BER_{post,FEC}}} - \underbrace{3.8\mathrm{dB}}_{\mathrm{Gain_{FEC}}} = \underbrace{21.2\mathrm{dB}}_{\mathrm{BER_{pre,FEC}}<1\times10^{-6}} \tag{3.9}$$

The DSP equalization boost is calculated as

$$\underbrace{30\mathrm{dB}}_{\text{channel loss}} - \underbrace{8\mathrm{dB}}_{\mathrm{Tx_{gain}}} - \underbrace{8\mathrm{dB}}_{\mathrm{Rx_{gain}}} = 14\mathrm{dB} \tag{3.10}$$

Considering a SNR noise penalty of -0.5dB per dB of DSP boost and a margin of 6dB, the SNR requirement at the input of the ADC yields:

$$\mathrm{SNR_{ADC}} = \underbrace{21.2\mathrm{dB}}_{\mathrm{BER_{pre,FEC}}<1\times10^{-6}} + \underbrace{14 \times 0.5\ \mathrm{dB}}_{\mathrm{N_{o,DSP}}} + \underbrace{6\mathrm{dB}}_{\mathrm{Margin}} = 34.2\mathrm{dB} \tag{3.11}$$

Using Eq. 3.6, the ADC resolution yields to ≈ 5.4 bits. This is the minimum resolution required to meet the target BER. Our design targets a resolution of 7 bits as a trade-off of speed and power for a single-channel ADC.

[1] Eq. 2.11 can be used as well

3.3 Hierarchical TI-ADC

3.3.1 Sampling capacitor estimation

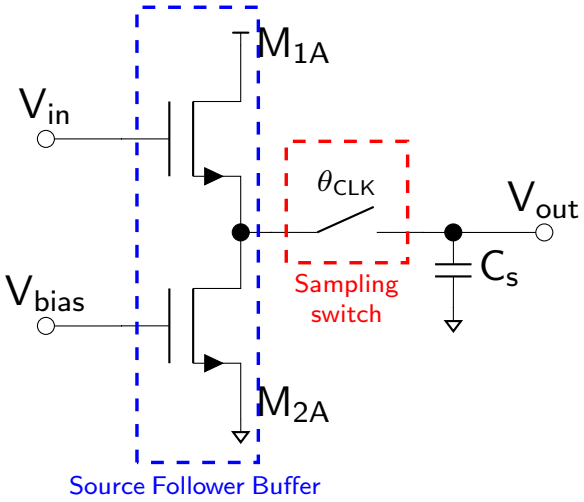


Figure 3.6: Track-and-Hold circuit: switched source follower.

A conventional TH circuit (Figure 3.6) consists of front-stage buffer combined with a series sampling switch. The front-end buffer is necessary to reduce kick-back to ADC input from the sampling. The buffer isolates the sampling capacitor from the ADC input and reduces the input capacitance of the ADC.

The voltage gain of the source voltage follower is represented as the attenuation factor A_{TT}

$$A_{TT} = \frac{g_{m1}}{g_{ms1} + g_{ds1} + g_{ds2}} \tag{3.12}$$

where g_m, g_ms and g_ds are the gate transconductance, source transconductance and drain-to-source conductance, respectively.

The sampling capacitor (C_s) is calculated from the SNR_{ADC} requirements. First, the RMS noise is calculated

$$\begin{aligned} N_{pp} &= \frac{V_{T\&H,in,pp} * A_{TT}}{SNR} = N_{RMS} * \alpha \\ N_{RMS} &= \sqrt{2 * \frac{kT}{Cs, single}} \end{aligned} \tag{3.13}$$

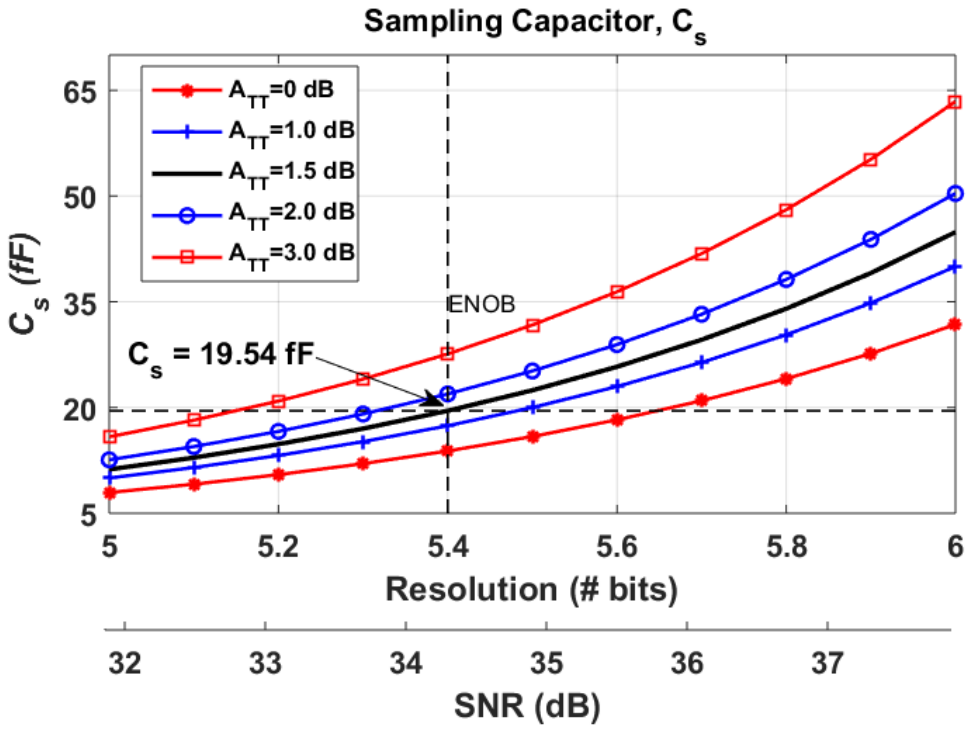


Figure 3.7: State-space design for the sampling capacitor (C_s).

where α=9.507 with a BER=1×10^{-6}. The design of the sampling capacitor is shown in Figure 3.7 for an input of 400mV_{pp}. Different values of A_{TT}, representing Process Voltage Temperature (PVT) variations, for the source voltage follower are considered. A sampling capacitor of 19.54fF with an A_{TT}=1.5dB[2] yields an equivalent resolution of 5.4 bits.

3.3.2 Direct and Inline Demux Sampling

Voltage-based TH can be categorized in direct and inline demux sampling [34], [35], [36], [37]. Both designs implement subsampling to achieve a higher Interleaved Sampling Ratio (ISR).

1. **Direct sampling**, shown in Figure 3.8(a), provides the shortest path from the input to the sampling capacitor with minimum resistance. N_1 denotes interleaving ratio as well as the total amount of sampling switches. One or more

[2]Represents a typical Source Follower Voltage Gain of 0.85 in 22nm CMOS FDSOI

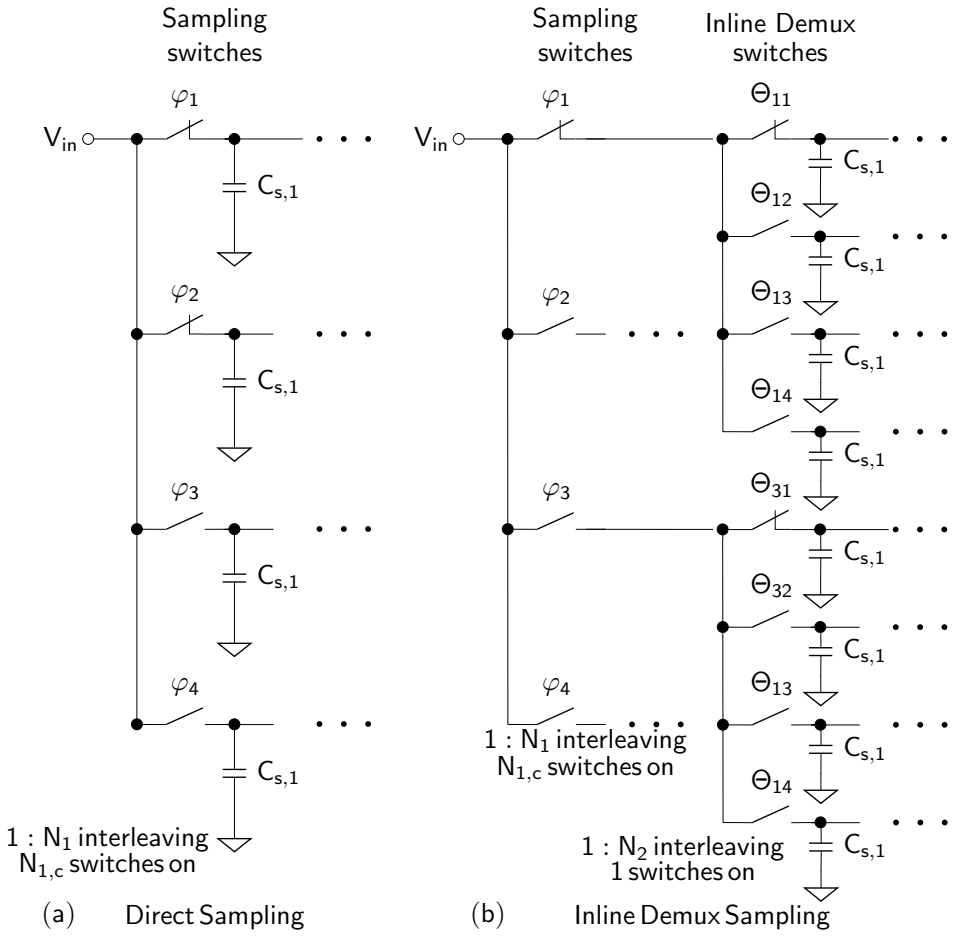


Figure 3.8: (a) Direct sampling. (b) Inline demux sampling.

of the sampling switches are closed at the same time, $N_{1,c}$. If only one switch is closed at a time, the bandwidth is the largest but the shortest sampling pulses are required. Direct sampling is very efficient for a small number of parallel switches (usually ≤ 8), as too many switches will increase the input capacitance at the input node. The sampled voltage is stored on the sampling capacitor C_S.

2. **Inline demux sampling**, shown in Figure 3.8(b), stacks two switches to reduce the number of parallel switches at the input. N_2 represents the total number of inline demux switches and $N_1 \times N_2$ is the interleaving ratio. The inline demux switch closes before the sampling switch closes and opens after the sampling switch opens. Thus, the sampling time depends only on the falling edge of the

sampling switch clock. The use of inline demux switches significantly reduces the number of timing critical clock signals.

At first glance, inline demux sampling allows higher ISR than direct sampling. To gain more insight into the advantage of one method over the other, an interleaver bandwidth analysis for the two methods was implemented. A simplified model for a cross-coupled switch is applied, as shown in Figure 3.9a. R_{on}, C_{in} and C_{out} correspond to a single switch transistor. A correction factor p is used to take into account the parasitic capacitors and resistors. The sampling capacitor is determined by the kT/C noise for the target SNDR.

Figure 3.9a, b present the RC model for the interleavers depicted in Figure 3.8. The elements of the RC circuit can be expressed by the interleaver parameters N_1, $N_{1,c}$, N_2, the switch parameters R_{on}, C_{in} and C_{out}, the total sampling capacitor C_s

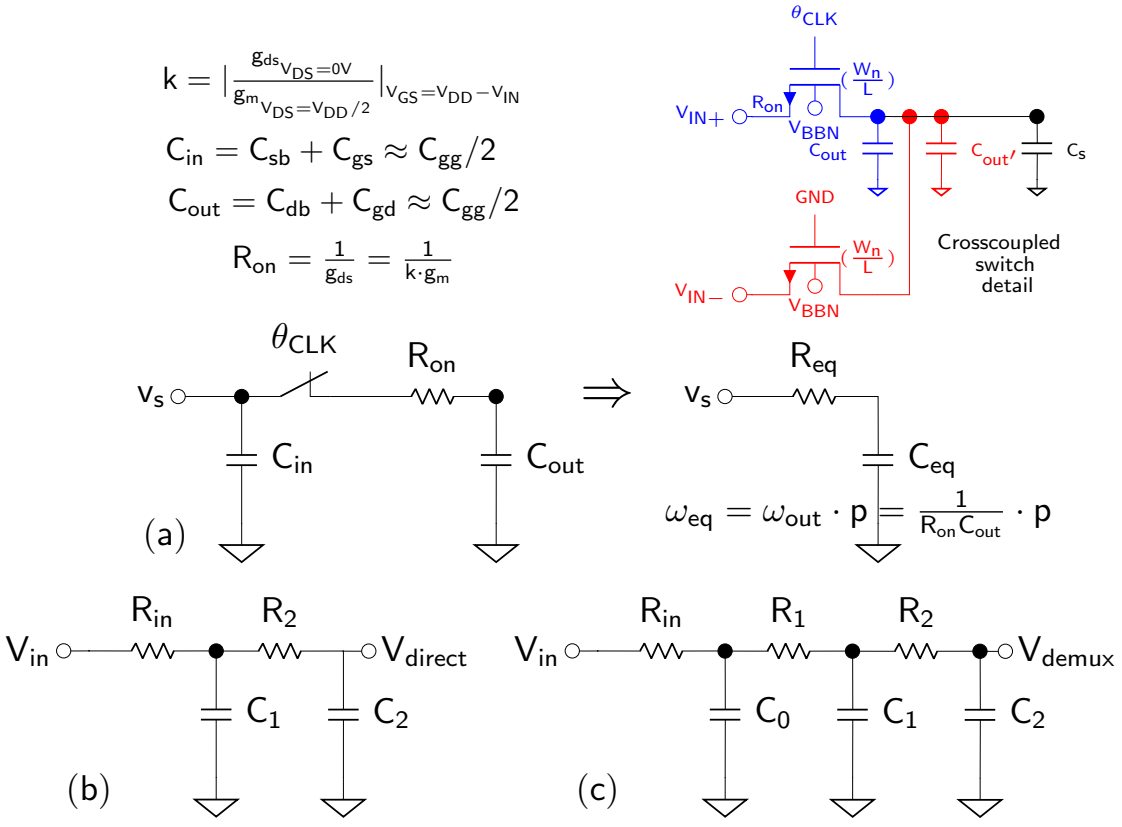


Figure 3.9: (a) Switch model and detail of parasitics. (b) RC model for Direct sampling. (c) RC model for Inline demux sampling.

Table 3.2: Interleaver parameters, transfer function, sampling and hold time.

Direct	Inline demux
R_{in} $C_0{=}N_1C_{in1}$	
	$R_1{=}R_{on1}/N_{1,c}$ $C_1{=}N_{1,c}C_{out1}+N_{1,c}N_2C_{in2}$
$R_2{=}R_{on2}/N_{1,c}$ $C_2{=}N_{1,c}(C_{out2}+C_s)$	
$H_{s,d}{=}\frac{1}{(1+sR_2C_2)(1+sR_{in}C_0)+sR_{in}C_2}$	$H_{s,i}{=}\frac{1}{((1+sR_2C_2)(1+sR_1C_1)+sR_1C_2)(1+sR_{in}C_0)+(1+sR_2C_2)sR_{in}C_1+sR_{in}C_2}$
$t_{s,pulse}$: $\Rightarrow N_{1,c}t_s$ for $N_1 \geq 2$ $t_s/2$ for $N_1 = 1$	
$t_{h,d}$: $\Rightarrow (N_1 - N_{1,c})t_s$ for $N_1 \geq 2$ $t_s/2$ for $N_1 = 1$	$t_{h,i}$: $\Rightarrow (N_1N_2 - 2N_{1,c})t_s$ for $N_1 \geq 2$ $(N_1N_2 - 1)t_s$ for $N_1 = 1$

t_s is the sampling period of the ADC

and the input resistance (R_{in}) seen from the ADC, i.e. the front-stage buffer. Table 3.2 summarizes the parameters, transfer function, sample and hold for the two sampling methods.

For a given input resistance and sampling capacitor size, the remaining degree of freedom is the architecture of the interleaver, specifically, the number of switches in each stage and their sizing. The maximum achievable 3dB bandwidth (BW_{3dB}) was obtained from the transfer function for direct and inline demux sampling up to a 32 ISR. R_{on}, C_{in} and C_{out} were optimized for the sampling switch and inline demux switch using the parameter extraction from the 22nm CMOS FDSOI PDK of GLOBALFOUNDRIES. The procedure is presented in appendix A.

Figure 3.10 shows the BW_{3dB} for the different direct and inline demux sampling configurations. The highest achievable bandwidth is always obtained for direct sampling with only one active clock at a time and ISR of 2 ($N_1/N_{1,c} = 2/1$), known also as a "Front-End sampler". The advantage of this configuration is that the sampler determines all sampling moments, avoiding timing misalignment and reducing the number of required low-jitter sampling clocks.

For higher ISRs, inline demux sampling requires less low-jitter clocks than direct sampling. A combination of both sampling methods will be applied to implement a hierarchical TI-ADC, which is described in the following subsection.

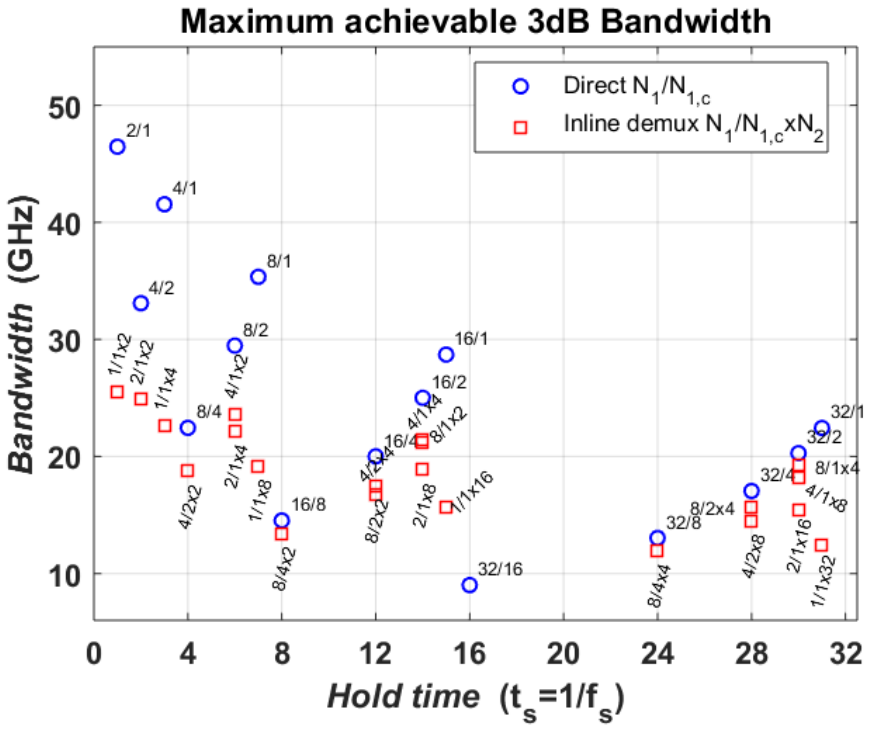


Figure 3.10: Maximum achievable 3dB bandwidth (BW_{3dB}) versus hold time for different direct sampling and inline demux sampling configurations. L = 20nm,$V_{S,D}$ = 0.35V, V_G = 0.8V, V_B = 1.8V and C_s = 20fF

3.3.3 3-Rank Hierarchical TI-ADC

In order to reduce the number of required low-jitter clocks for sampling and to avoid complicated delay calibration of multiple clock phases, a hierarchical architecture is chosen for the TH circuit [36]. Figure 3.11 shows the architecture. It implements an ISR of 64 distributed into three ranks of TH:

1. First rank is a 2-way TI TH stage at half rate (28GHz),
2. Second rank is a 8-way TI TH stage at 3.5GHz,
3. Third rank is a 4-way TI TH stage at 875MHz.

This architecture gives us the best trade-off in terms of bandwidth and number of low-jitters clocks. By using the first rank as front-end sampler at half rate, it only requires two low-jitter clocks at 28GHz or one differential. For the second and third

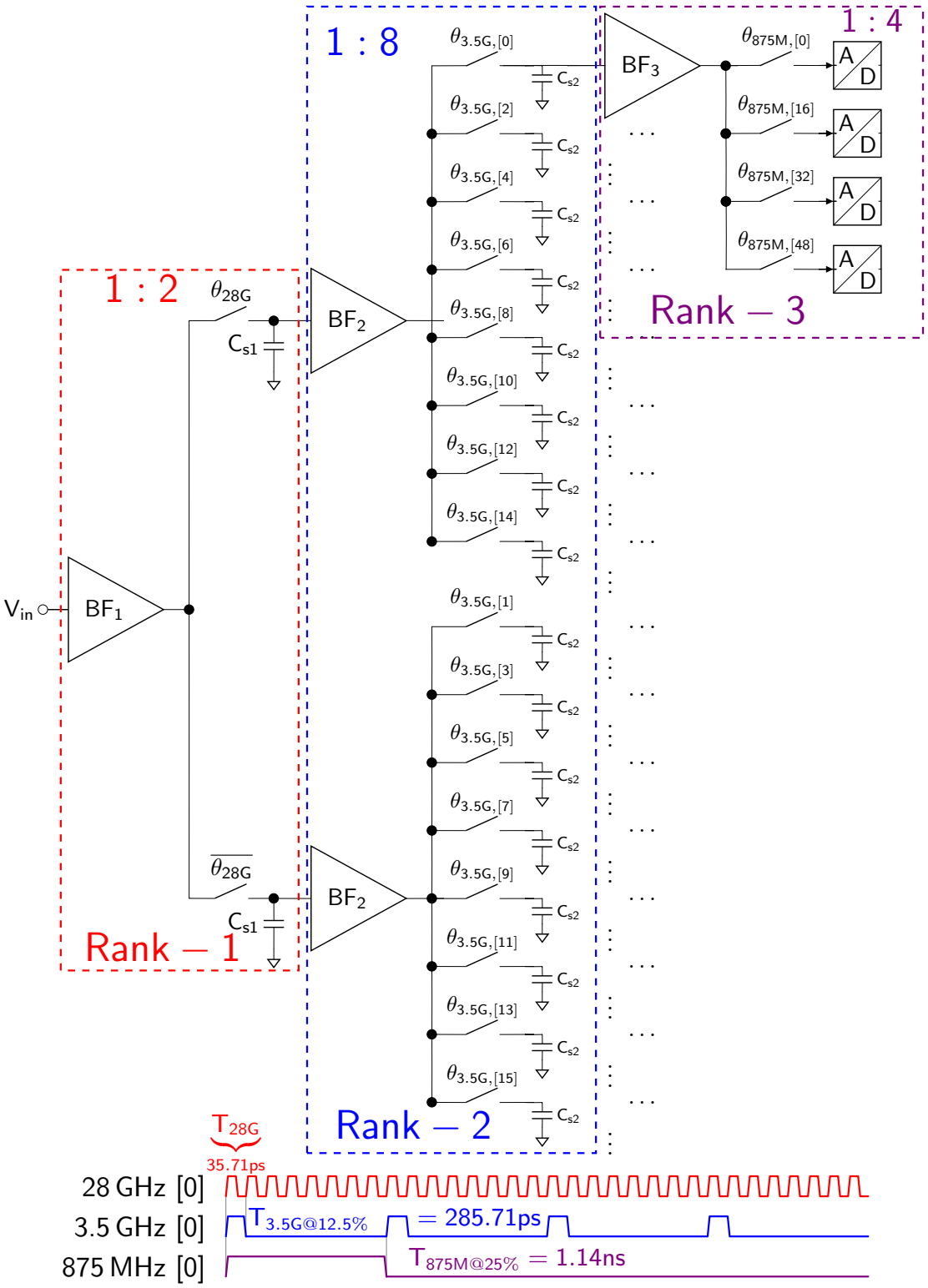


Figure 3.11: Architecture of the 3-rank hierarchical TI-ADC

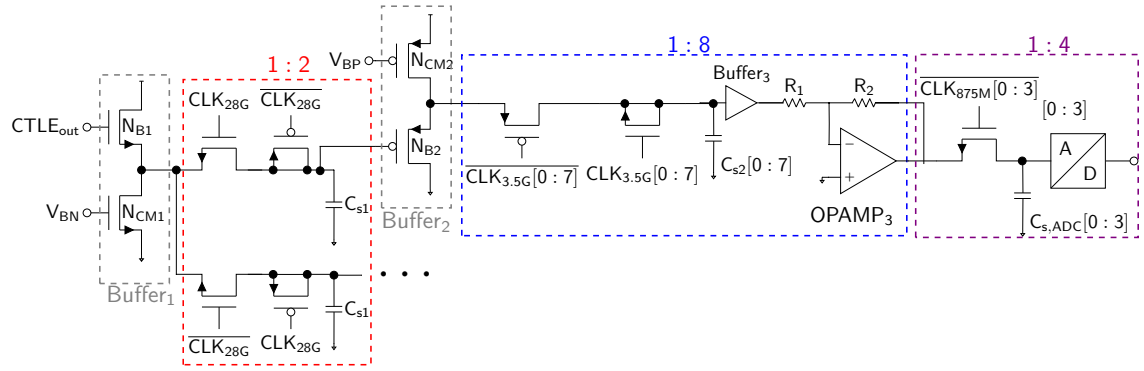


Figure 3.12: Schematic diagram of the 3-rank hierarchical TI-ADC

rank, as long as the sampling settles, the clocks are not required to be low-jitter and they can be generated by dividing the first rank clock.

The hierarchical TI-ADC circuit is shown in Figure 3.12. It has 3 ranks of TH for a total of 64 sub-ADC channels. A 2-way TI TH stage is chosen as the first stage of

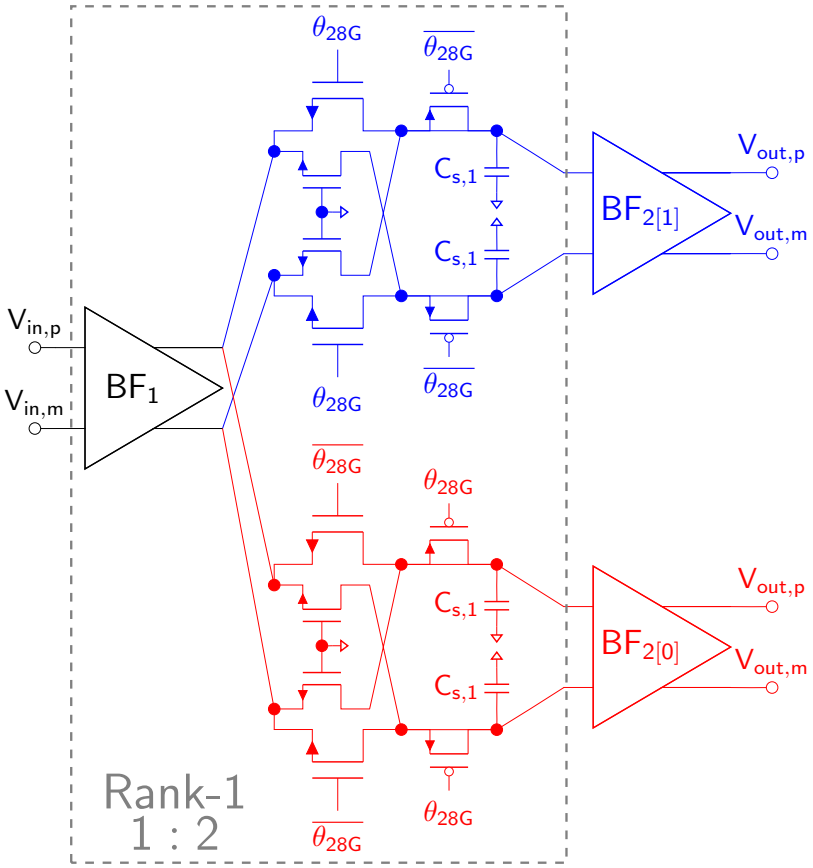


Figure 3.13: Schematic diagram of the rank-1 T&H

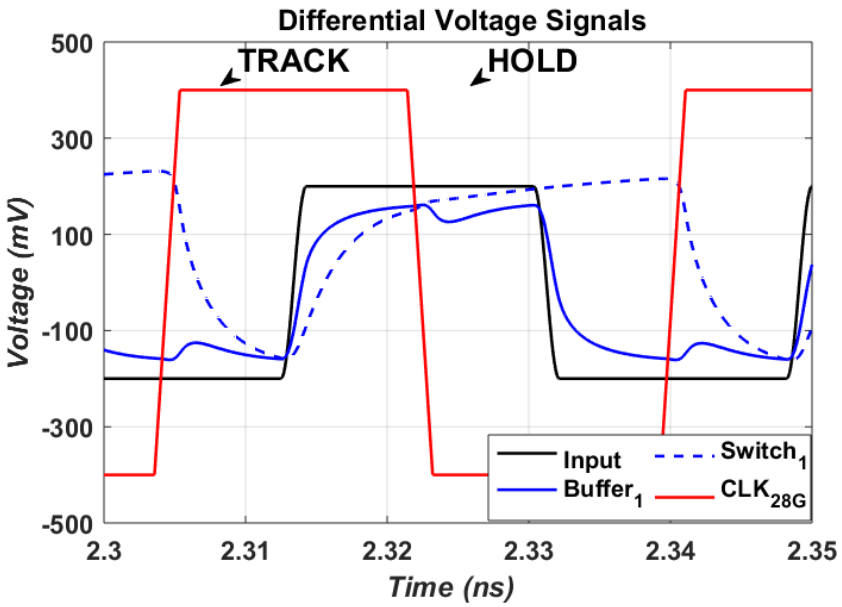


Figure 3.14: Signals of the rank-1 T&H

the hierarchical TH. A source voltage follower with cross-coupled switches shows the best trade-off between voltage headroom and linearity. As described before, rank-1 is 2-way TI TH circuit sampled at 28GHz. A passive gain is implemented using the PMOS dummy switch varying its capacitance from track to hold operation [38]. This technique allows to passively amplify the sampled signal and thus to improve the SNR.

The total sampling capacitance C_{s1} consists of the parasitics of the switches and the input capacitance of the voltage follower of rank-2. Figure 3.14 shows the track and hold operation in rank-1. The input signal is sampled at 28GHz with a sample transition in the middle of the tracking interval. The passive gain at the output of the switch is shown during the hold interval. It will improve the SNR in the following rank. The buffers used in rank-1 are source voltage followers, as shown in Figure 3.15a.

Rank-2 is an 8-way TI TH circuit sampled at 3.5GHz. The buffer used in this stage ($Buffer_2$) is a gain-boosted Flipped Voltage Follower (FVF) (as seen in Figure 3.15) [39]. The Flipped Voltage Follower (FVF) technique delivers a smaller output resistance compared to a conventional source follower. Thus, allowing a higher bandwidth for the same power consumption. The gain is achieved by cross-coupling

the NMOS transistors (M_{4A-4B}) to form a pseudo-differential common source stage. A back gate biasing control is implemented for PVT variations. The bandwidth is extended by introducing a feedback capacitor C [40]. The DC bias of the top PMOS transistors (M_{3A-3B}) is set by V_{BP} through large bias resistors.

Figure 3.12 shows the eight PMOS cross-coupled switches sampled by eight non-overlapping clock signals. To improve the isolation between rank-2 and rank-3, the output of each switch is passed through a buffer ($Buffer_3$). These buffers are scaled versions of the buffer in rank-1. The duty-cycle of the sampling clocks for rank-2 and rank-3 are set so that only 1 interleaved switch following the inter-rank buffer is closed at any given time.

Figure 3.16 shows the time diagram for the TH operation in rank-2. It starts with tracking the $Buffer_2$ output. $Buffer_3$ reads the output of the PMOS switches ($Switch_2$) and transfers it to the input of the gain stage ($OpAmp_3$) of rank-3.

The rank-3 is a 4-way TI TH circuit sampled at 875MHz. Figure 3.12 shows 4 NMOS switches, representing the TH stage of a sub-ADC unit. Each 4-way TI TH

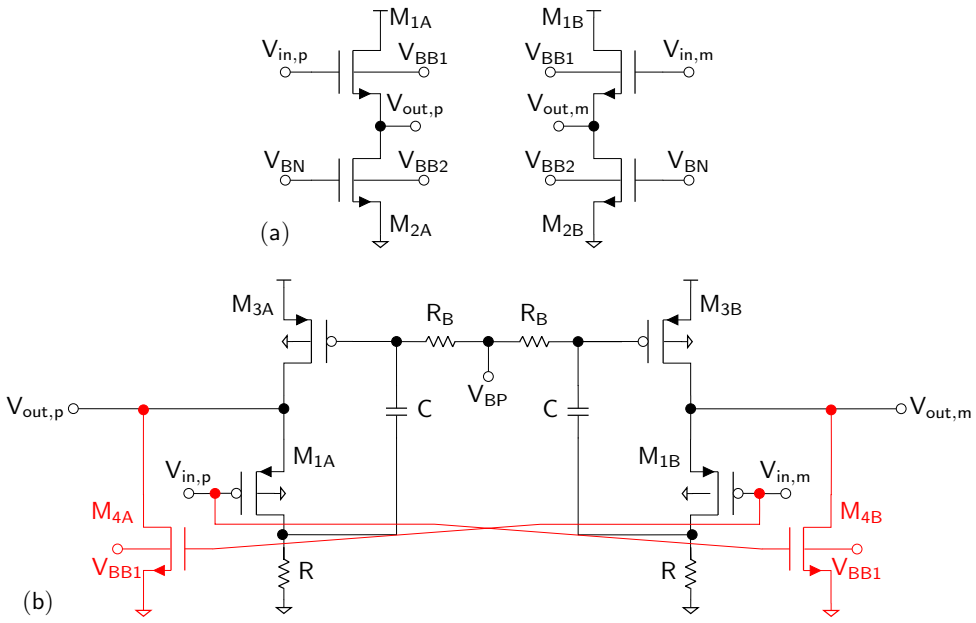


Figure 3.15: (a) Rank-1 buffer: Source Follower. (b) Rank-2 buffer: Gain-boosted Flipped Voltage Follower (FVF)

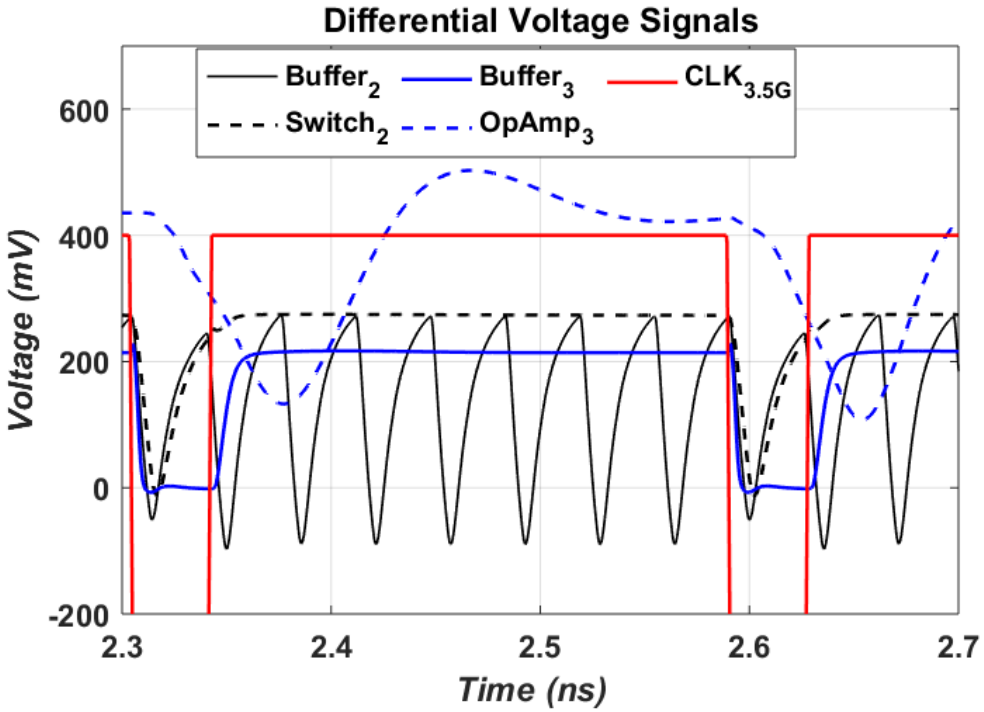


Figure 3.16: Signals of the rank-2 T&H

path is driven by a gain stage.

In order to provide a full-scale input and the correct common mode, as required by the ADC, a voltage gain stage is implemented using an OpAmp with feedback resistors (as seen in Figure 3.17a). Since the input common mode coming from Buffer_3 is not adequate for the input stage of the OpAmp, an input Common Mode Feedback (CMFB) is used to fix it to a more suitable value ($\approx$ 250mV). The combined gain of the rank-1 and rank-2 is lower than 1 ($\approx$ 0.87). Thus, a voltage gain of $\approx$2.3 is needed to bring the signal to the full scale level of the ADC. A programmable gain with +/-25% variation was implemented by adjusting the feedback resistor R_{FB}.

The schematic of the OpAmp is presented in Figure 3.17b. It consists of a low-voltage fully differential 2-stage amplifier with Miller compensation. It implements an output common mode feedback circuit to bring the DC output level to $V_{DD}/2$. Gain boosting is added to the first stage and can be digitally turned on or off. Calibration circuits for offset and output common mode are implemented using back

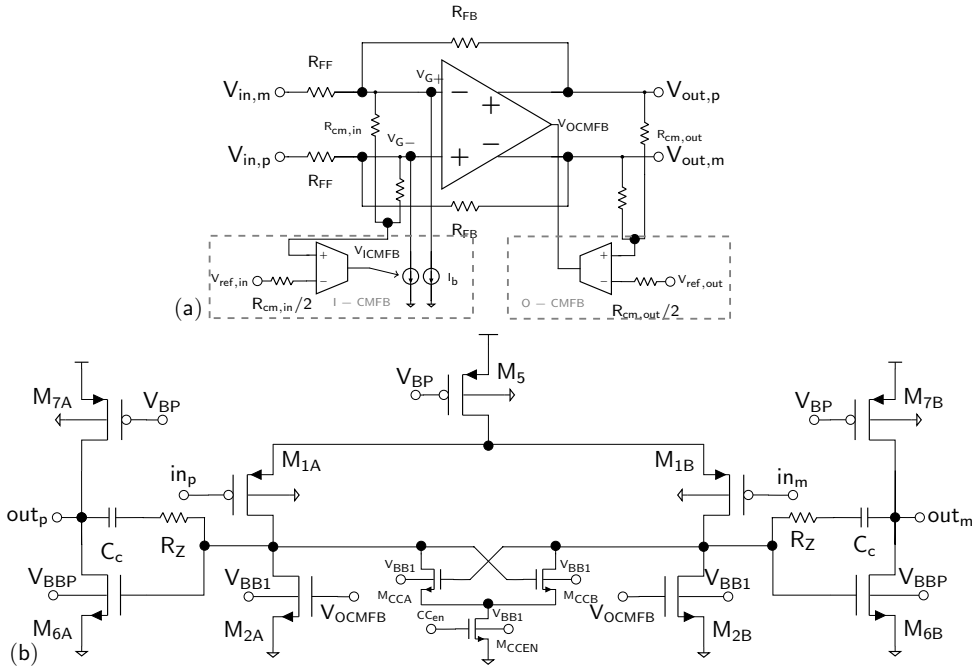


Figure 3.17: (a) Diagram of the rank-3 gain stage. (b) Fully differential two-stage OpAmp with gain enhancement.

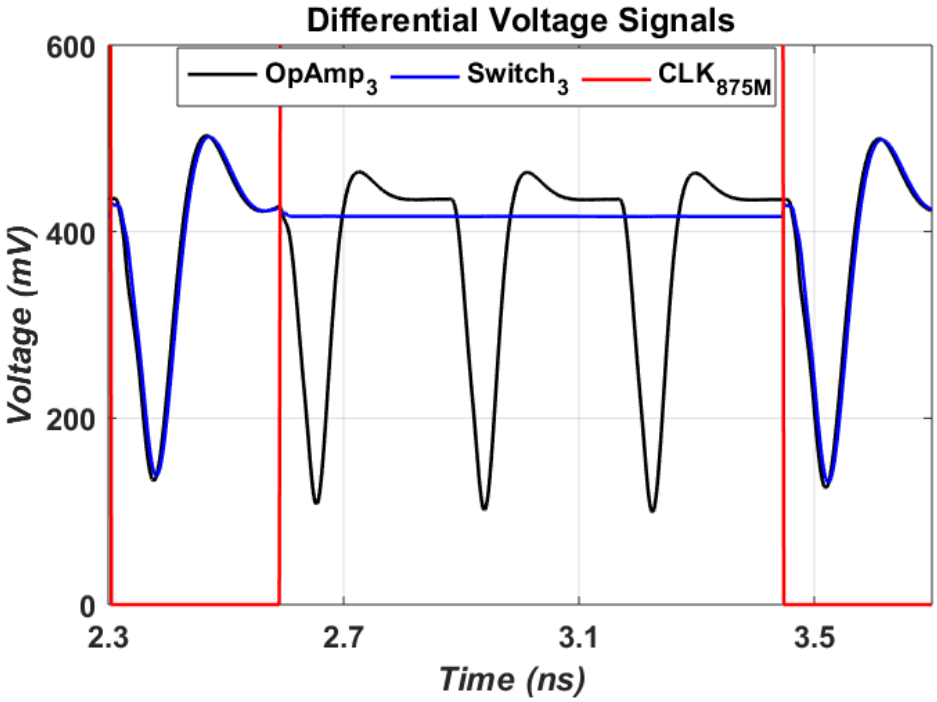


Figure 3.18: Signals of the rank-3 T&H

gate biasing. The output of the OpAmp needs to settle within the track time of the ADC ($t_{track,ADC}$=285.76ps). This requirement sets the bandwidth for the OpAmp.

Figure 3.18 shows the TH operation in rank-3. The output of the gain stage ($OpAmp_3$) is tracked by the ADC ($Switch_3$). The tracked voltage settles within the $t_{track,ADC}$ time.

In Figure 3.19 the non-linearity introduced by the buffers and gain stage is analyzed. The circuits have been designed to meet an overall variation of 1% for the entire hierarchical TH.

The BW_{3dB} and power consumption of the hierarchical TH at nominal, slow and fast corners are presented in Table 3.3. The nominal power consumption is 113.5mW, where 70% corresponds to rank-3. The rank-1 TH was designed for maximum BW_{3dB}. Figure 3.20 depicts the voltage gain in the hierarchical TH. A total voltage gain of $\approx$ 2 brings the input signal to the full scale of the ADC.

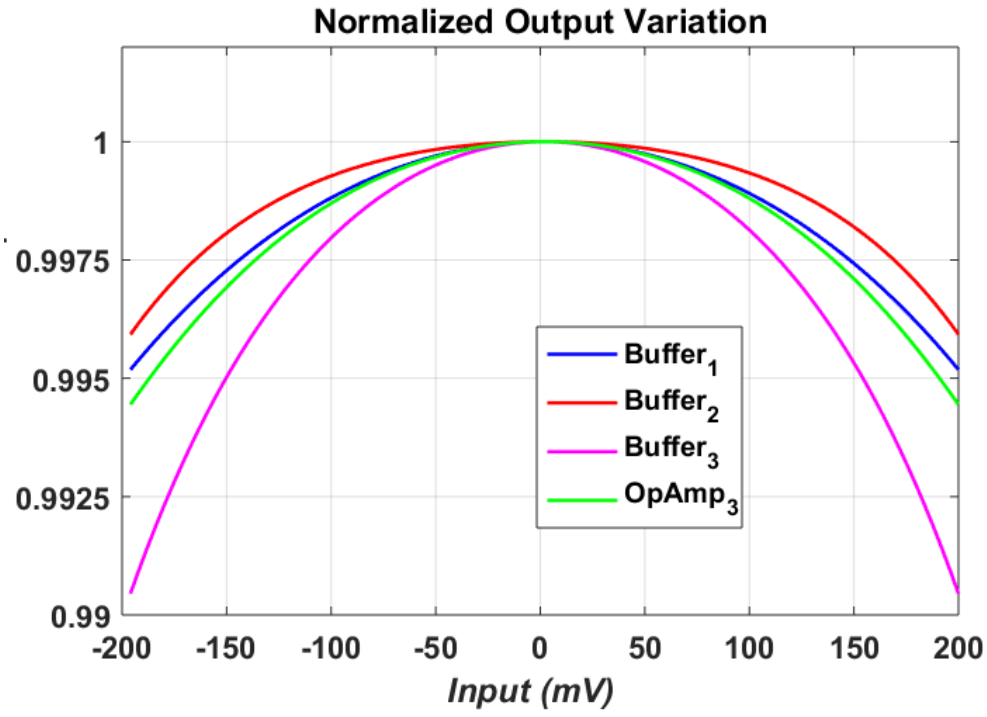


Figure 3.19: Normalized output variation between stages

Table 3.3: BW_{3dB} and Power Consumption of the Hierarchical TH

Circuit	Bandwidth (GHz)	I_{Comp} (mA)	Supply (V)	Power (mW)
$Buffer_1/Switch_1$	73.2[1] 59.2 46.9[2]	22.3[1] 22.4 22.7[2]	0.8	17.8[1] 17.9 18.2[2]
$Buffer_2$ x2	30.2[1] 25.7 21.3[2]	8.2[1] 7.5 7.2[2]	1	16.4[1] 15 14.4[2]
$Switch_2$	27.2[1] 22.3 17.6[2]			
$Buffer_3$ x16	25.6[1] 21.3 16.9[2]	2.44[1] 2.5 2.56[2]	0.8	31.2[1] 32 32.8[2]
$OpAmp_3^3$ x16	9.4[1] 7.7 5.6[2]	3.76[1] 3.8 3.9[2]	0.8	48.2[1] 48.6 49.9[2]
$Switch_{ADC}$	8.6[1] 6.4 3.8[2]			
		Total	113.6[1] 113.5 115.3[2]	

[1]Fast Corner at -40°C, [2]Slow Corner at 110°C, [3]At nominal gain

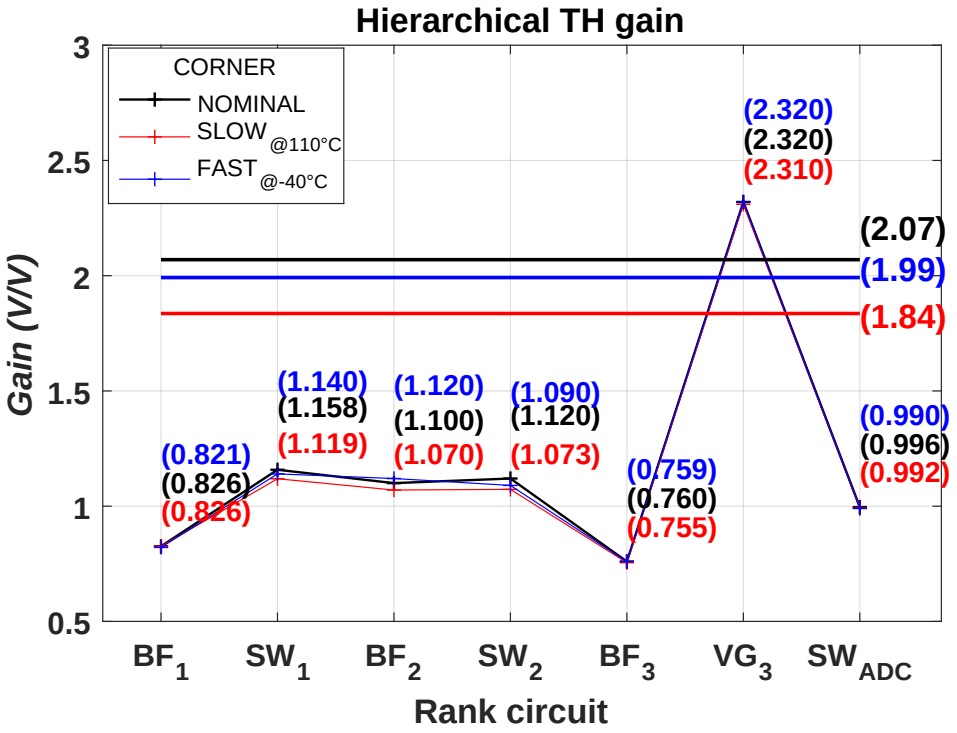


Figure 3.20: Hierarchical TH gain for nominal, slow and fast corners

3.4 Clock generation and distribution

The TI-ADC input signal is first sampled by the rank-1 sampler and the remaining rank-2 and rank-3 samplers simply function as 1-to-8 and 1-to-4 analog demultiplexors that bring the sample rate down to that of the sub-ADC. At the outputs of the hierarchical TH, the 64 TI analog samples are digitized by parallel sub-ADCs.

The TI-ADC rank-1, rank-2 and rank-3 clocks are generated from an external differential clock signal of 28GHz through a few stages of division and distribution as illustrated in Figure 3.21. The sampling clock for the rank-1 TH has a frequency of 28GHz and 50% Duty-Cycle (DC). Since the 28GHz clock is jitter-critical, it is AC-coupled from the external clock and distributed through buffers with Duty Cycle Distortion (DCD) and delay calibration. The outputs of the rank-2 TH are TI at 3.5GS/s: $3.5\text{GHz}_{[0:15]}$ are clocks generated by one Frequency Divider by 8 (FD8) with a 12.5% DC so that the rank-2 TH drives only one load capacitor at any time. Similarly, 16 Frequency Dividers by 4 (FD4), one for each rank-2 clock phase, generate the sampling clocks for the rank-3 TH, which are 64 875MHz clocks with 25% DC.

Finally, clock signal $\text{CLK}_{\text{retimer}}$ is generated to retime the TI-ADC digital outputs

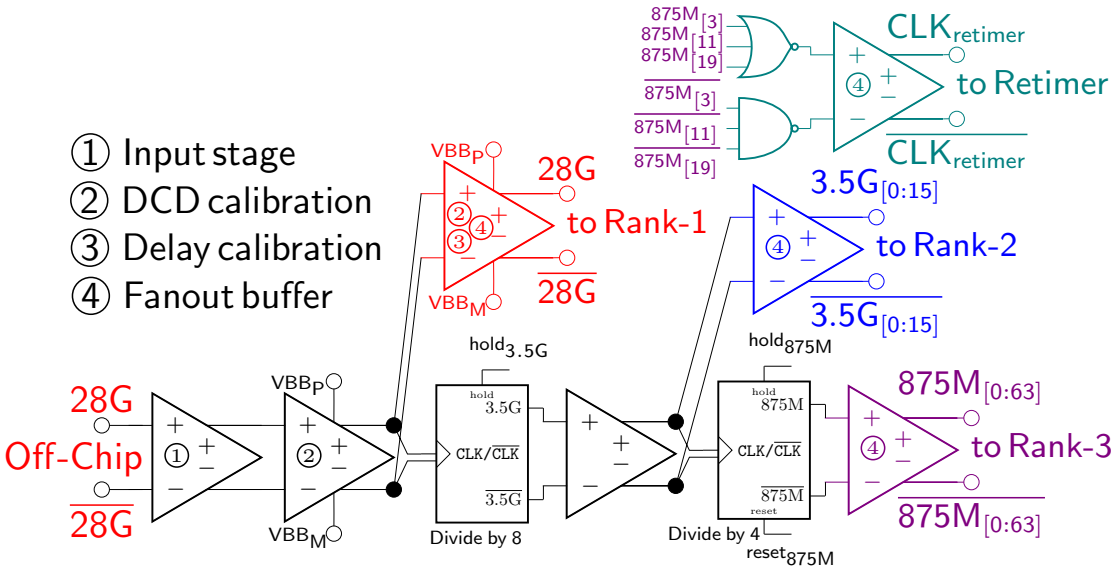


Figure 3.21: Diagram of the TI-ADC Clock generator

before sending them to the DSP unit. It is a 50% DC version of the $875M_{[3]}$ phase. This clock is also used by DSP.

The schematic of input stage is presented in Figure 3.22a. It has a 50Ω-input matching network followed by a high-speed buffer. The latter consists of an AC-coupling capacitor in series with a resistive feedback inverter for DCD suppression [41]. The buffer high-pass cutoff frequency can be relatively high (≪1/10 of the input frequency) allowing the use of a small Metal-Oxide-Metal (MOM) capacitor. A fan-out buffer and Transmission Gate (TG) with reset for clock alignment complete the input stage.

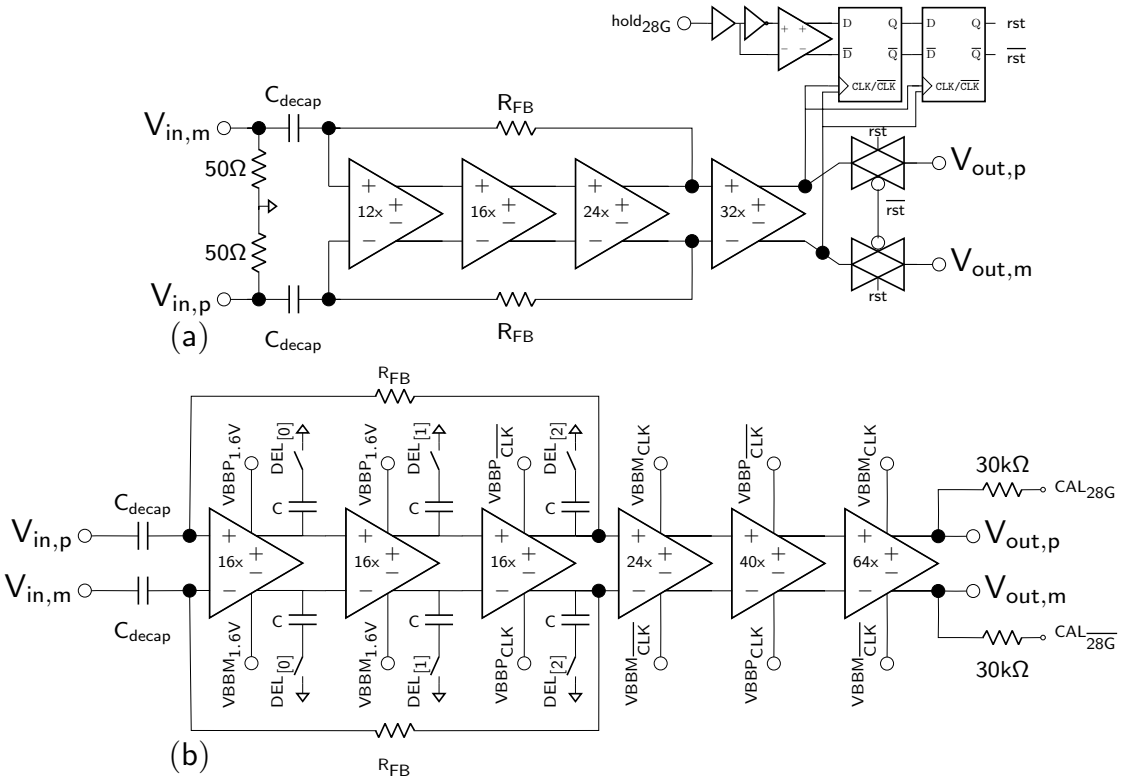


Figure 3.22: (a) Input stage. (b) Buffer with DCD and delay calibration.

The schematic of the clock buffer going to rank-1 is shown in Figure 3.22b. It consists of a high-speed buffer with DCD suppression in series with fan-out buffers. The resistive feedback inverter chain adds capacitive loads to implement a variable delay. A 3-bit control gives a total delay variation of 30%UI. The fan-out buffers have

DCD calibration. The output is sensed and calibrated to $V_{DD}/2$ by adjusting the back gate biasing voltage of the buffers. The back gate biasing calibration methodology is explained in appendix B.

The FD8 generates 16 3.5GHz clock phases with 1UI=$\frac{1}{56GHz}$ difference between phases. The circuit is shown in Figure 3.23a. It is a differential synchronous design to avoid jitter accumulation. The 12.5%DC is obtained by feedback tapping the last even phase to the input of the first Flip-Flop D (FFD). The odd phases are generated by tapping two consecutives FFDs. The schematic of FD4 is presented in Figure 3.23b. It generates 4 875MHz clock phases with 16UI difference between phases. The 25% DC is obtained in the same fashion as for FD8. The input TGs is controlled by a reset signal for clock alignment.

A detail timing diagram consisting of the sampling clocks for rank-1, rank-2, rank-3 and retimer are shown in Figure 3.24. It indicates the track, hold and conversion time TI-ADC. The sampling clocks in each rank are 1UI spaced.

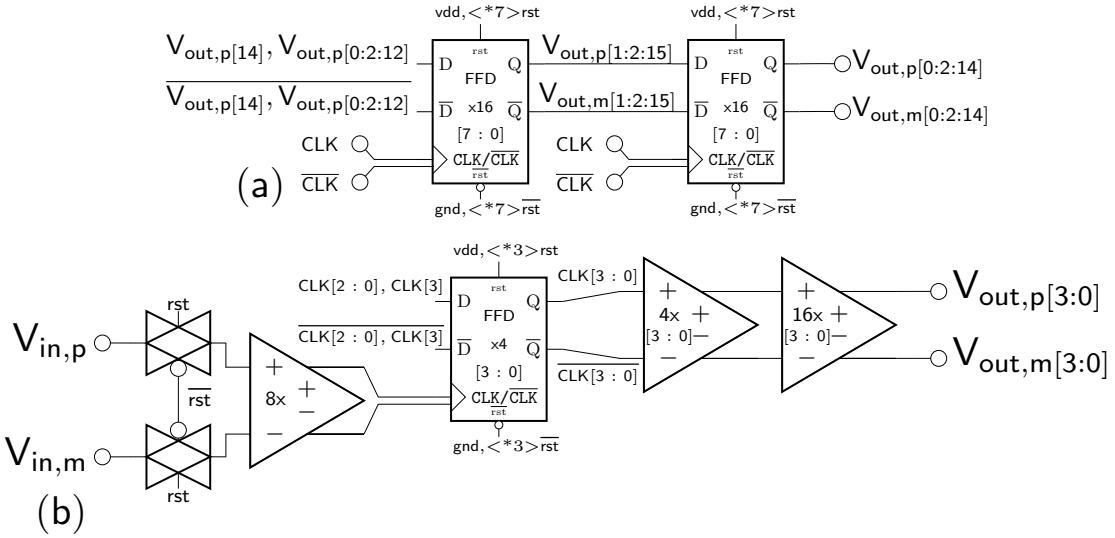


Figure 3.23: (a) FD8 with 12.5%DC. (b) FD4 with 25%DC.

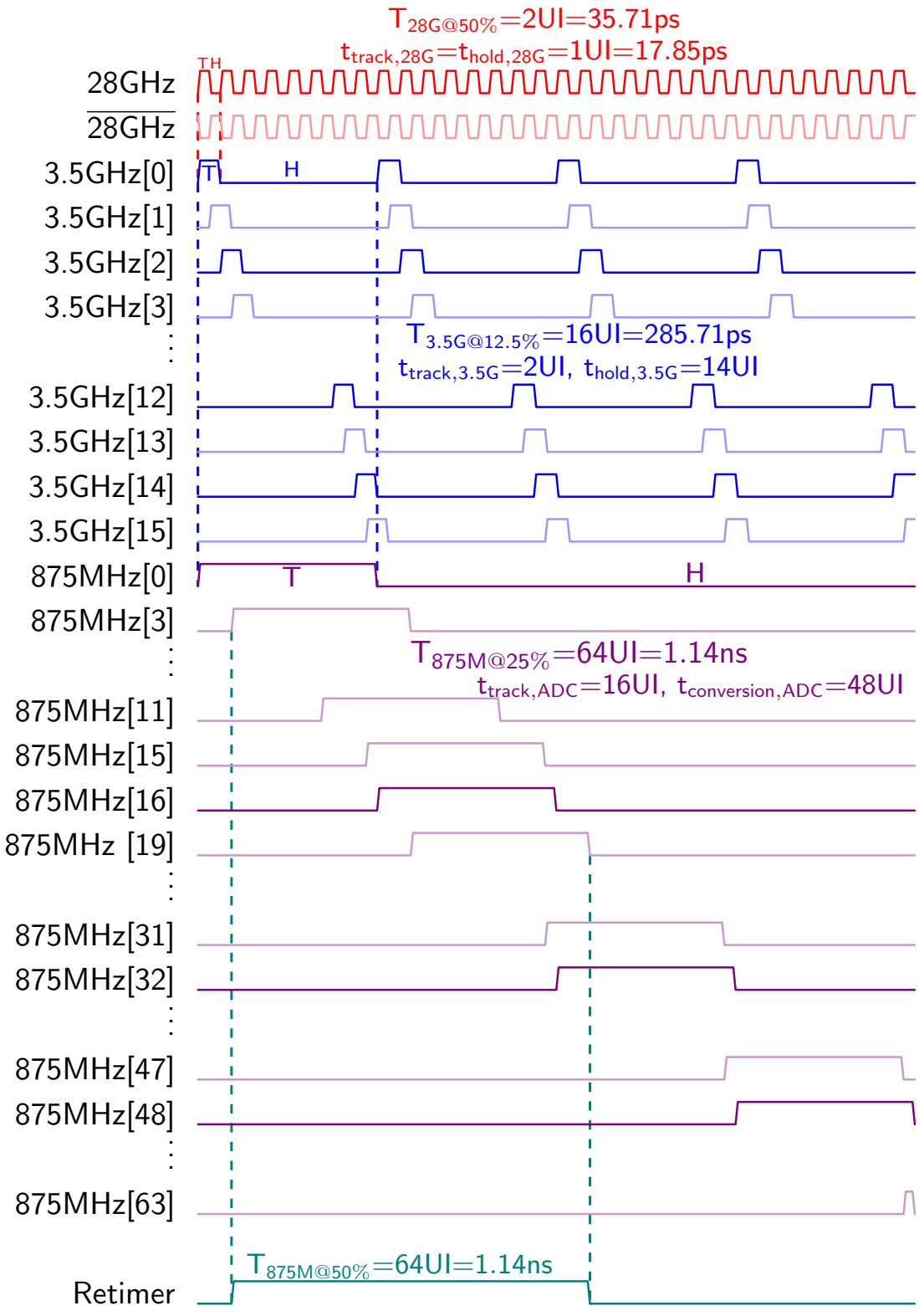


Figure 3.24: Clock generator waveforms

3.5 Sub-ADC implementation

TI-ADC is implemented using identical sub-ADCs multiplexed in time, operating in parallel to achieve a higher sampling rate, [34]. Power consumption must be optimized in the interleaved system.

3.5.1 Architecture Selection

A suitable sub-ADC architecture should not magnify the complexity and the achievable speed and resolution. The architecture selection was chosen from the energy efficiency comparison of two high-speed, medium-resolution converters: the flash ADC and SAR ADC.

An N-bit flash ADC is composed of 2^N-1 comparators, a reference resistor ladder and a thermometer-to-binary encoder as shown in Figure 3.25(a). The reference resistor ladder and thermometer-to-binary encoder energies scale roughly as 2^N but are usually less than the total comparator energy. For simplicity, the speed and structure of the comparators used in Flash and SAR ADC are assumed to be the same. Therefore, the energy per conversion for a flash ADC is

$$\begin{aligned} E_{comp} &= C_{latch} V_{DD}^2 \\ E_{flash} &= (2^N - 1) \cdot E_{comp}, \end{aligned} \tag{3.14}$$

where E_{comp} is the energy of a single comparator. C_{latch} and V_{DD} represent the total

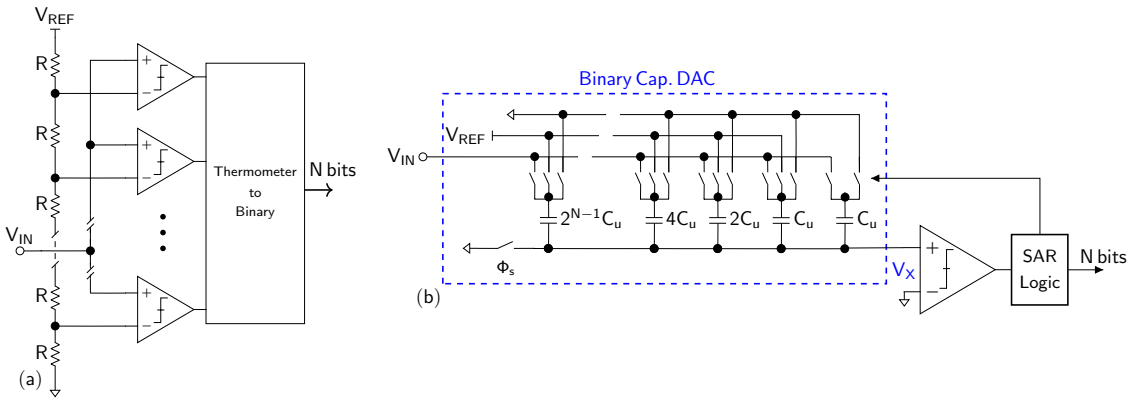


Figure 3.25: (a) Flash ADC. (b) SAR ADC with binary-weighted capacitive DAC.

switched capacitance in the comparator's latch and supply voltage, respectively.

A basic SAR ADC structure is shown in Figure 3.25(b). It consists of a comparator, a capacitive DAC and a SAR control logic. There are several switching schemes aiming to improve the energy efficiency in SAR ADCs [42]. For simplicity, the conventional switching scheme is used in this comparison. The energy per conversion of the comparator can be calculated similar to a flash ADC.

The capacitive DAC using the conventional switching scheme presents a total array energy for one conversion is

$$E_{DAC} = 2\eta 2^{(1+1/2\zeta)N} \frac{C'_u}{2^{N'/2\zeta}} (V_{DD} V_{FS}), \tag{3.15}$$

where C'_u is the process-dependent unit capacitance required for matching to the N'-bit level and is assumed to be 2.4fF in 22FDX. V_{FS} is the ADC full scale, respectively. The η[3] and γ[4] coefficients represent the DAC energy dependence on the input-signal and capacitance mismatch, respectively. The total energy consumed by the switching of the SAR logic over one conversion is

$$E_{logic} \approx N C_{SW,eq} V_{DD}^2, \tag{3.16}$$

where $C_{SW,eq}$ is the total switched capacitance in the SAR logic normalized to 1-bit level. Summing the energy of the SAR blocks, the total energy per sample conversion yields

$$E_{SAR} = E_{DAC} + (N+1) \cdot E_{comp} + E_{logic} \tag{3.17}$$

The total energy consumption of flash and SAR ADCs are compared versus a resolution range of 1 to 8 bits, as seen in Figure 3.26. At resolutions below 4 bits, a flash ADC presents lower energy compared to a SAR ADC. However, as the resolution increases the number of comparators in a flash ADC increases exponentially, while it increases linearly for a SAR ADC. Above a resolution of 6 bits, the energy efficiency of the SAR structure becomes more apparent. Based on this energy comparison, a SAR ADC is the better choice for 7-bit resolution, which is the target range for the proposed ADC-based receiver.

[3] η=0.7 is a reasonable approximation [43]

[4] γ equals 3/4 or 1/2 if the mismatch is dominated by edge effects or oxide variation, respectively.

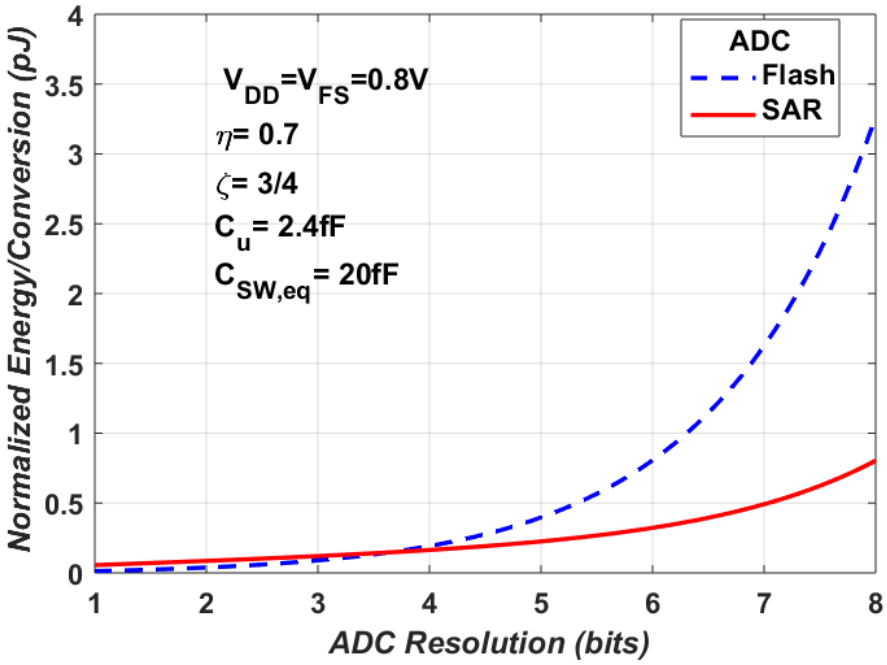


Figure 3.26: Energy comparison between SAR and Flash ADCs as a function of resolution

A very low-power 875 MS/s 7-bit Successive Approximation Register (SAR) ADC that is suitable for integration into a TI-ADC is presented. The use of an integer-based split capacitive DAC (CDAC) combined with an improvement for the Least Significant Bit (LSB) capacitor allows a substantial improvement in the SNDR. A simple and accurate calibration procedure for the ADC is presented thanks to back gate biasing.

3.5.2 Circuit Description

The proposed SAR ADC uses asynchronous design to improve the speed conversion, an integer-based split CDAC and the monotonic switching principle.

Figure 3.27a illustrates the top-level ADC architecture. The front-end TH circuit consists of a sampling bootstrapped switch with feed-through and charge-injection compensation. The sampling clock ($\Phi_{s,ADC}$), with a 25% DC, drives the TH and triggers the asynchronous internal conversion logic, which is responsible for generating the bit-cycle phases, controlling the comparator, storing its decisions and switching the CDAC. The ADC comprises two identical 6-bit CDACs to accommodate differential

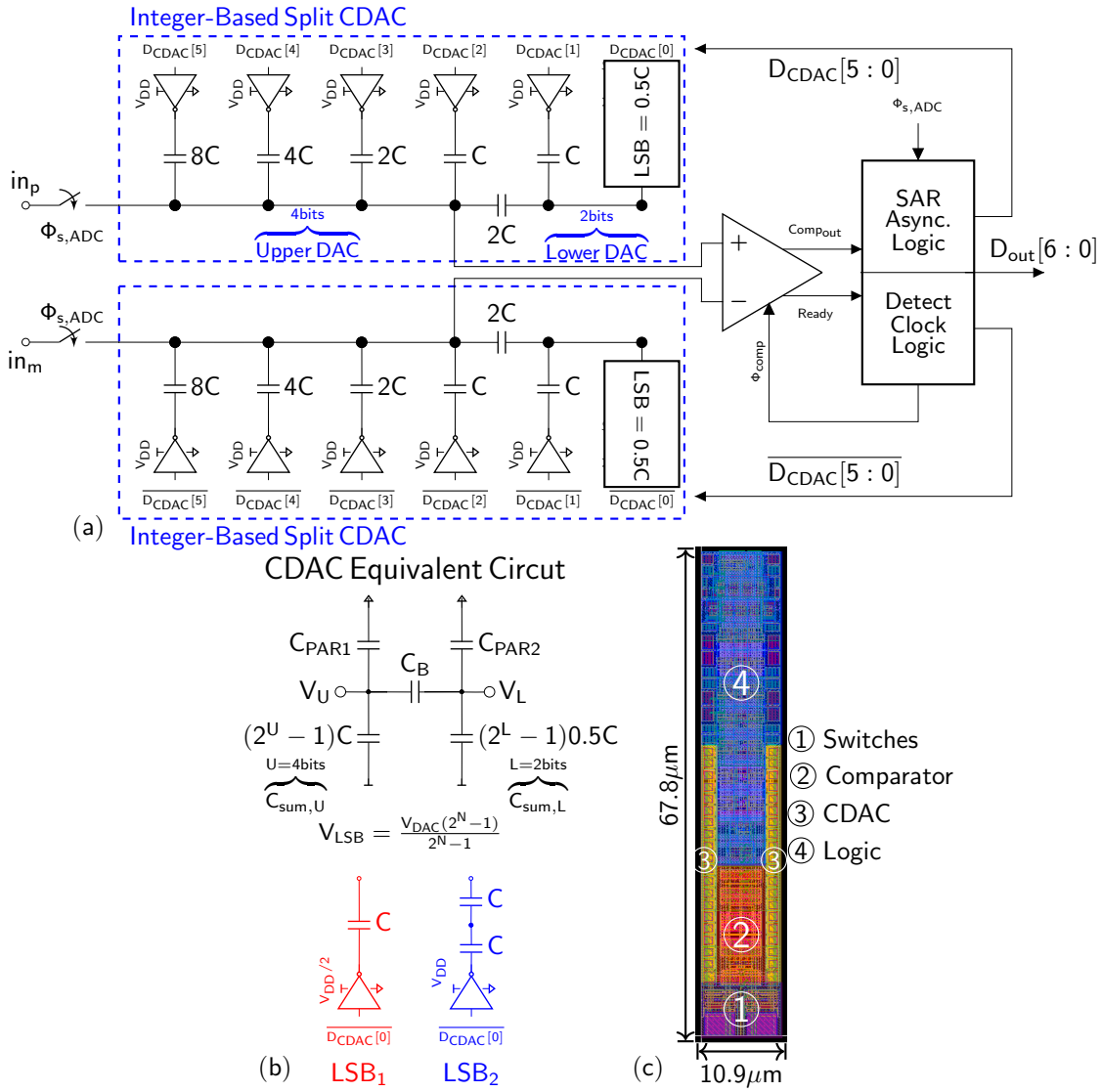


Figure 3.27: (a) Architecture of the proposed single-channel 7-bit SAR ADC. (b) LSB Capacitor Variation: LSB_1 (red) and LSB_2 (blue). (c) Layout.

operation. Since the MSB decision is the sign bit, it can be decided without changing the state of the CDAC. Thus, 6-bit CDAC - instead of 7-bit CDAC - is sufficient for this 7-bit SAR ADC design [44].

The layout was required to have a narrow form factor in the horizontal axis because of the large ISR of the TI-ADC, as seen in Figure 3.27c.

3.5.3 Capacitive DAC

The 6-bit CDAC, depicted in Fig. 3.27a, is based on an integer-based split capacitive DAC. The CDAC is divided in two sides: the lower side and the higher side of 2-bit and 4-bit, respectively. The split capacitor with a value 2C (C=unit capacitor) is placed just after the smallest unit capacitor of the 4-bit array, thus avoiding the non-linearity issues found in the common split capacitor array [45]. In the lower side, two variations for the LSB capacitor were evaluated, as shown in Figure 3.27b. Instead of switching a fraction of the unit capacitor (0.5C) during the LSB conversion by the full difference of the reference voltage, V_{REF}=V_{DD}, a unit capacitor (1C) is switched by a fraction of the reference voltage, V_{REF}=$V_{DD}/2$, which will be referred as LSB_1, [46]. The LSB_2 is implemented switching two unit capacitors (1C) in series by V_{REF}=V_{DD}.

The unit capacitors of the CDAC are designed to achieve best area efficiency using alternate-polarity metal-finger capacitors (APMOM) which offer high density, good matching characteristics and low parasitics.

For this 7-bit SAR ADC, the total capacitance of this capacitor array is $(2^{7-3} + 3)\,C$=19, [45]. A 70% area reduction compared to a conventional CDAC with monotonic switching is obtained, thus reducing settling time between conversion cycles and minimizing area and power consumption. The designed one-side total capacitance is 45.6fF, which produces an equivalent kT/C thermal noise of 301.4μV. The LSB value for a 7-bit ADC at a reference voltage of 0.8V is 6.25mV, so the thermal noise introduced by this capacitor array is not a limiting factor.

Following the equivalent circuit shown in Fig. 3.27b, the CDAC voltage (V_{DAC}) and LSB voltage (V_{LSB}) are

$$V_{DAC} = \frac{C_B(C^U_{VREF} + C^L_{VREF}) + C^U_{VREF}C_{sum,L}}{den} \cdot V_{REF} + \frac{C^U_{VREF}C_{PAR2}}{den} \cdot V_{REF} \quad (3.18)$$

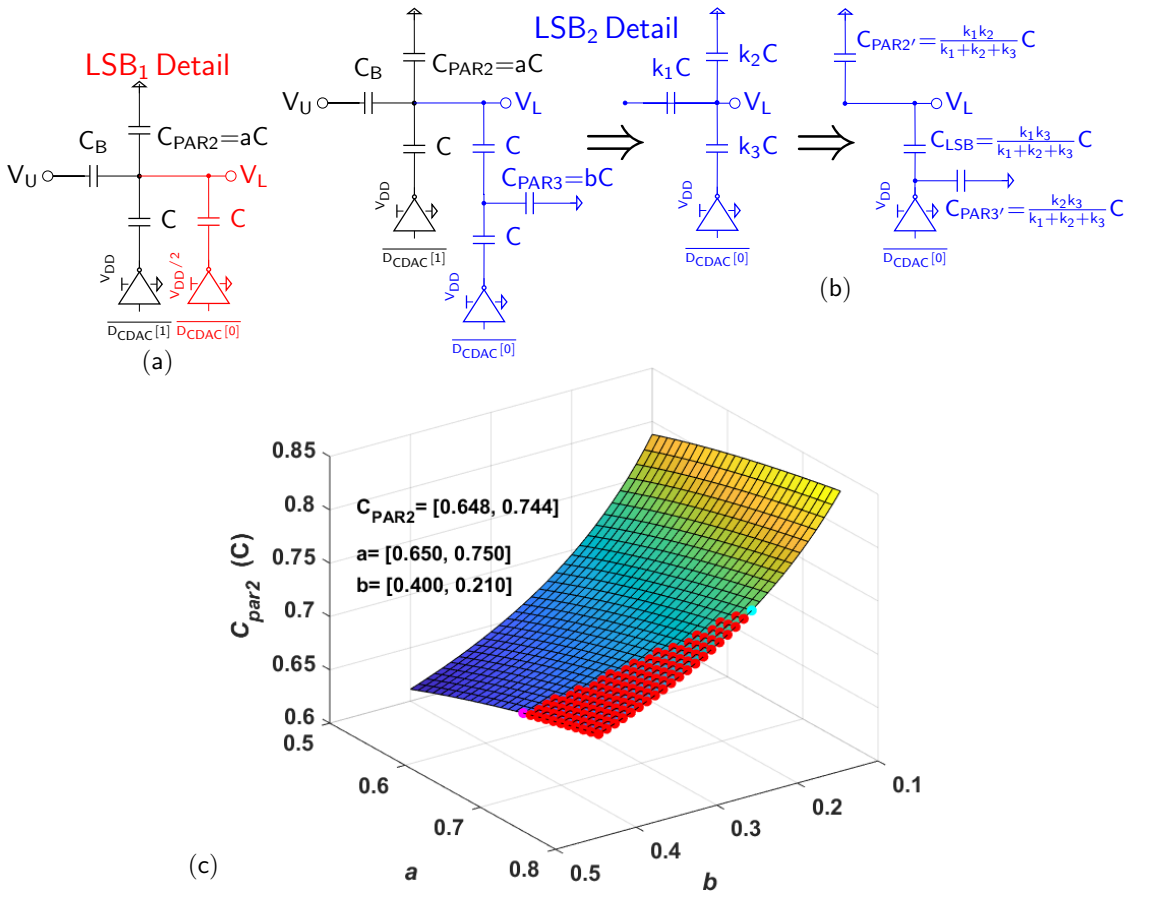


Figure 3.28: LSB equivalent circuit with parasitics: (a) LSB_1, (b) LSB_2. (c) C_{PAR2} grid for a,b values

$$V_{LSB} = \frac{V_{DAC}(2^N - 1)}{2^N - 1} = \frac{C_B(C_{sum,U} + C_{sum,L}) + C_{sum,U}C_{sum,L} + C_{sum,U}C_{PAR2}}{(2^N - 1)den} \cdot V_{REF} \quad (3.19)$$

where N=U+L, den=$(C_{sum,U} + C_{PAR1})(C_{sum,L} + C_{PAR2}) + C_B(C_{sum,U} + C_{sum,L} + C_{PAR1} + C_{PAR2})$, C_B=2C. $C_{sum,U–L}$ and $C^{U–L}_{VREF}$ denotes the total capacitance and total capacitors connected to V_{REF} in the upper and lower DACs, respectively.

The parasitic capacitance C_{PAR2} in the numerator of Eq. 3.19 contributes to a code-dependent error, degrading the DAC linearity [47]. C_{PAR2} is defined by the total parasitic capacitance of the top plates in the lower CDAC and the metal interconnection. Figure 3.28a shows the lower DAC section for the LSB_1 capacitor. C_{PAR2} is denoted as a fraction of the unit capacitor (aC). In this condition the V_{LSB}

error can be reduced by minimizing C_{PAR2} contribution.

In Figure 3.28b a variation of LSB capacitor (LSB_2) to reduce the V_{LSB} error is shown. C_{PAR2} is the same as in LSB_1, but with the addition of C_{PAR3} as the parasitic capacitance of the bottom plates of the two unit capacitors in series. C_{PAR3} is represented as a fraction of the unit capacitor (bC). Through a delta-star transformation, LSB_2 is shaped with the same arrangement as for LSB_1. Figure 3.28c shows the new value of C_{PAR2}. A range for C_{PAR3} between [0.21 0.4]C yields the reduction of C_{LSB} and C_{PAR2} simultaneously. In 22nm CMOS FDSOI, the APMOM capacitors present a parasitic ≈0.13C per capacitor yielding a value of b around 0.26.

3.5.4 Comparator

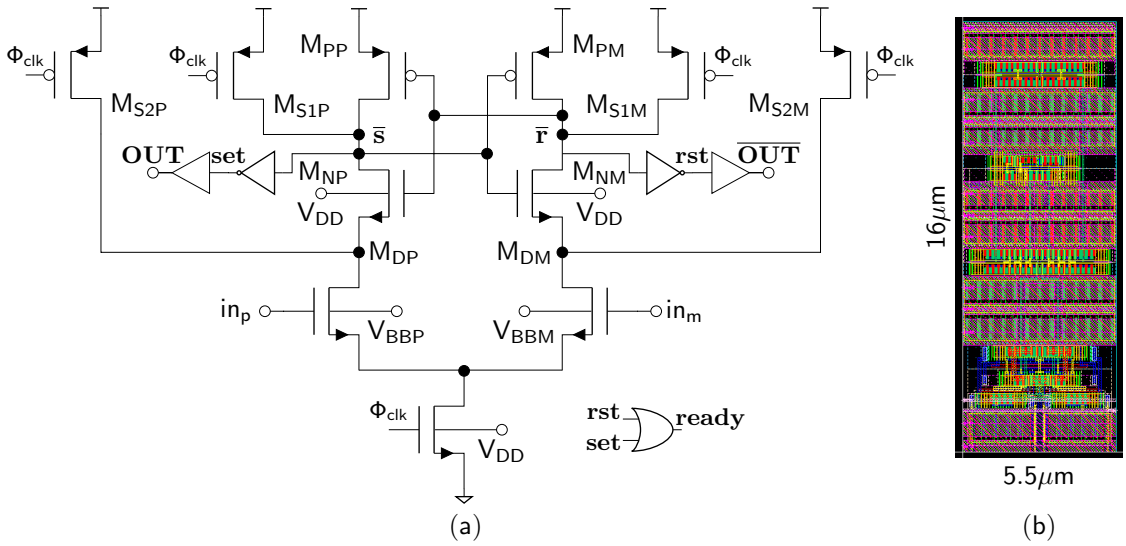


Figure 3.29: Strong ARM Comparator: (a) Schematic; (b) Layout

Since the comparator determines the accuracy and speed of the ADC, special care has to be taken for its design [48]. A strong-ARM comparator is chosen for its superior decision speed enabled by the single-stage design. It is optimized for low noise and low power.

Figure 3.29a shows the schematic. The latch regeneration forces one of the signals, *rst* and *set*, to high and the other to low, depending on the comparison result. As a

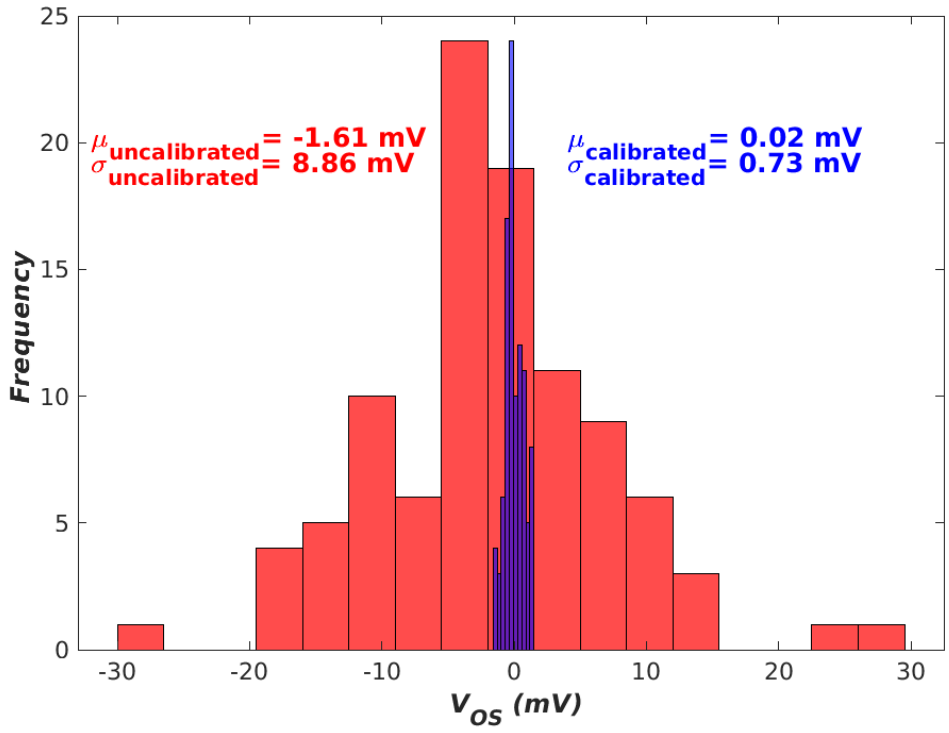


Figure 3.30: Histogram Strong ARM V_{OS}: Uncalibrated; Calibrated for 100 MC runs

result, the output of the OR gate (*ready*) is pulled high to enable the asynchronous control clock and to facilitate the progression to the next step in the SAR conversion.

The offset voltage V_{OS} introduced by the input differential pair is calibrated using a simple and accurate procedure (appendix B). The calibration operates in two phases: V_{OS} extraction and V_{OS} calibration. The extraction is a fast loop operating at the comparator's clock frequency Φ_{CLK} and follows the Smart Resettable SAR (SR-SAR) technique presented in [49]. Here, the voltage offset is calculated.

The second phase is a slow loop (below 1MHz), due to the low frequency nature of the transistor's back gate. After extracting the V_{OS}, the control block begins to adjust the threshold voltages (V_{TH}) of the differential pair through a back gate biasing DAC, which consists of a resistor ladder controlled by a 5-bit digital word.

The nominal voltage supply for the comparator is 0.8V, the same for the back gate bias at nominal operation. The ladder was designed using a resolution of 5 bits, with the back gate voltage varying between 0.4 to 0.8V. An artificial offset voltage range of

+/- 32mV ($\approx$ 2.1mV steps) was created. For example, if a negative V_{OS} is extracted, the calibration controller will only choose from the positive range to counterbalance the negative V_{OS} generated by the differential pair.

Monte Carlo (MC) Post-Layout Simulations (PLS) were performed to calculate the statistical distribution of V_{OS} and the histograms were plotted in Figure 3.30. The V_{OS} mean was zeroed and the standard deviation was reduced by a factor of 12.

3.5.5 SAR Logic

Besides the advantage of faster bit-cycle conversion, an additional benefit of asynchronous SAR logic is that it does not require an external high-frequency clock and thus saves the power needed to generate and distribute it. This is extremely important, since this ADC will be part of a time-interleaved system.

The logic of the SAR ADC can be divided into two parts: 1) the clock generation, which provides the clock for the comparator and the bit-cycle phases and 2) the state memory, in charge of controlling the CDAC based on the comparator decision in each of the bit-cycle phases (Figure 3.31). The track duration is set at 25% of the 875MHz clock period.

The clock generation combines the clock Φ_{ADC}, ready and $stop_{cycle}$ signals to generate the comparator clock (Φ_{Comp}) and bit-cycle clocks ($CLK_{p,n}$) with simple combinational logic. At the same time, a sampling *pulse* is generated from $\overline{\Phi_{ADC}}$ and its delay. This *pulse* propagates sequentially, as controlled by the $CLK_{p,n}$ signals, generating each of the bit-cycle phases (Figure 3.31). Additionally, the stop cycle signal is used to indicate the end of the conversion cycle.

The state memory part connects directly to the differential output of the comparator. A dynamic register is used as memory to optimize loop delay and enables fast settling upon comparator decision. One cell is activated during every comparison by its corresponding $bit_{cycle}[i]$ and provides $Dout_{CDAC}$ and $\overline{Dout_{CDAC}}$ as control signals for the CDAC. Finally, $Dout_{CDAC}$ is retimed by Φ_{ADC} to create the output data.

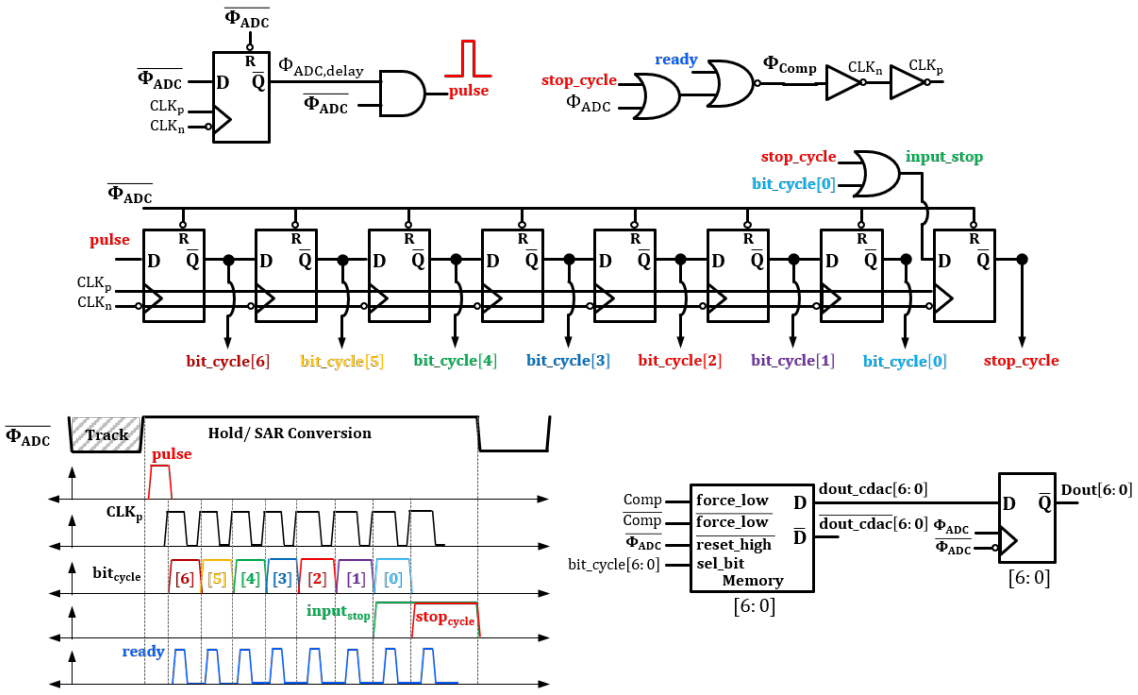


Figure 3.31: SAR Logic and timing

3.6 Simulation Results

The hierarchical TH, sub-ADC and clock generator had been designed using the 22FDX^{TM} platform in 22nm CMOS FDSOI of GLOBALFOUNDRIES, [50]. One of the most differentiated features of the 22FDX platform is the capability of effective back gate biasing. Back gate biasing applies a positive or a negative voltage to the back gate of the transistor, which allows the transistor V_{TH} to be tuned, and can be done statistically or dynamically.

3.6.1 Sub-ADC

The nominal full-scale ADC input is 800mV$_{pp,diff}$ with a common mode of 400mV. It operates from a core 0.8 V supply and simulated, under typical conditions. Power consumption is 1.65mW based on PLS results at 875MS/s. This overall power consists of 80µW for the bootstrapped input switch, 40µW for the CDAC, 0.68 mW for the comparator and 0.85mW for the phase and SAR logic, as seen in Figure 3.32.

Whereas, the calibration for the comparator was implemented to extract the V_{OS},

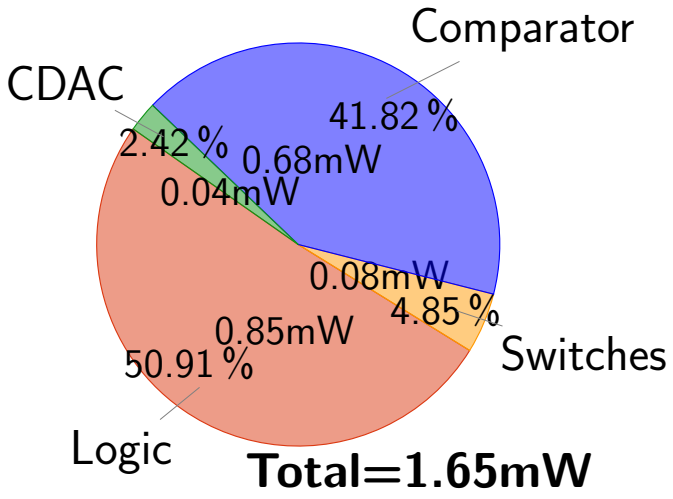


Figure 3.32: sub-ADC power consumption breakdown.

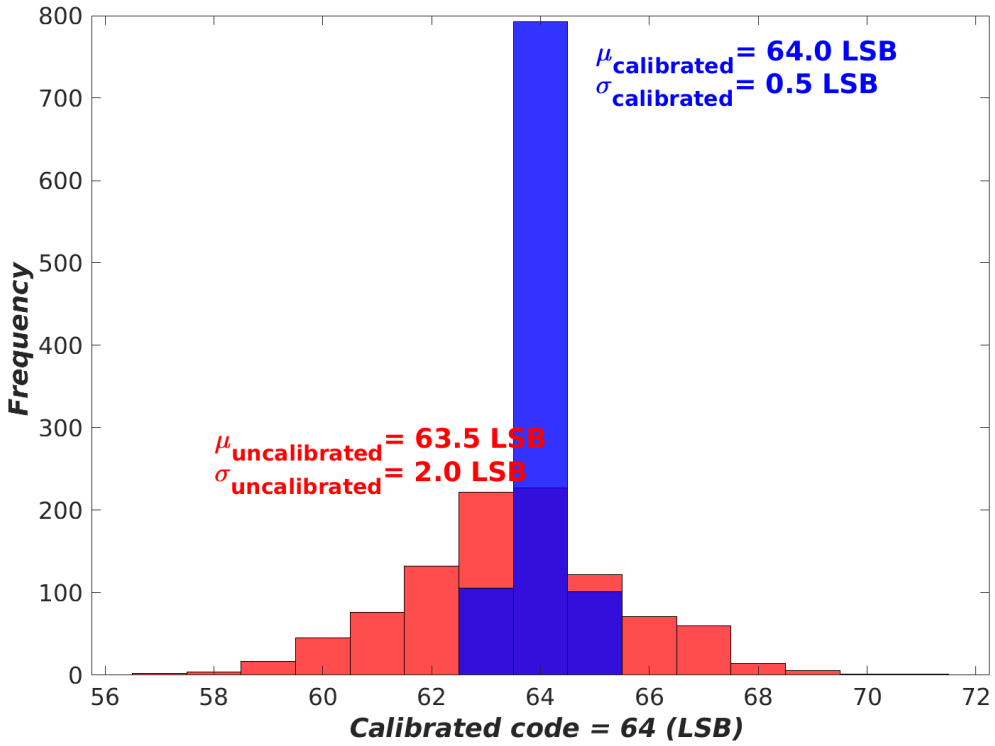


Figure 3.33: Histogram of ADC Output: Uncalibrated, Calibrated for 1000 MC runs

it can also be used to calibrate the ADC. Figure 3.33 shows the MC simulation results. The ADC was calibrated at the middle of the range (64 LSB) and a 4x reduction of the output code σ was achieved. It is worth to mention that the limiting factor for the ADC calibration is the resolution, LSB = 6.25mV (7 bits).

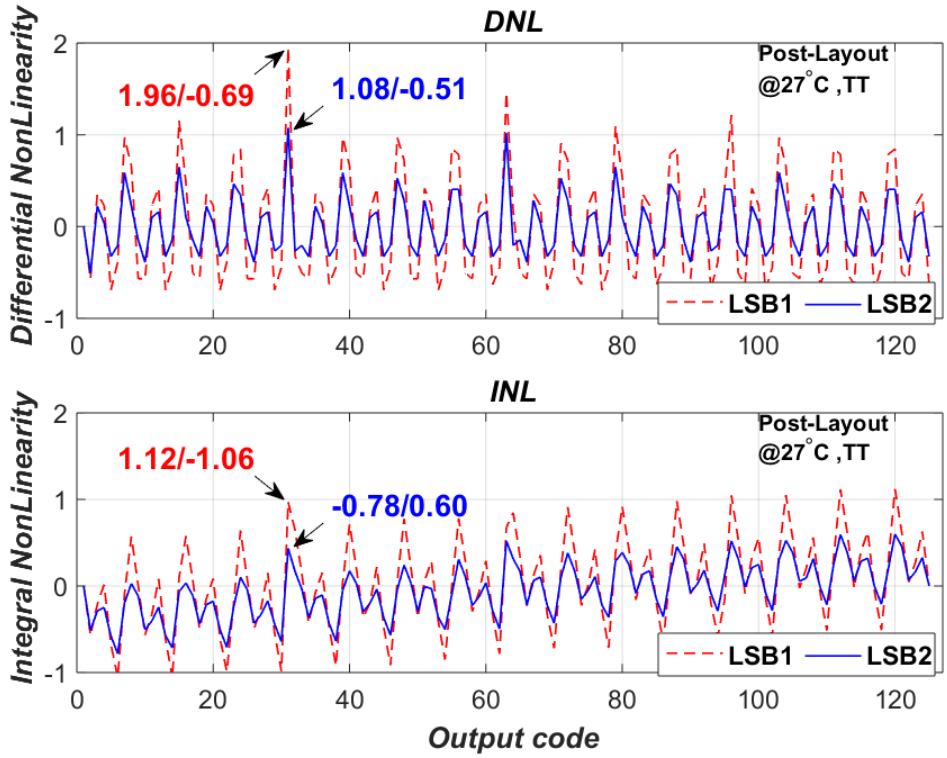


Figure 3.34: DNL and INL. LSB_1 (red) and LSB_2 (blue)

The calibration procedure for the comparator and ADC was performed at low frequency, due to the time step of the transient simulation is coarse enough to allow a much faster convergence solution. For that reason, the results for static and dynamic characteristics shown are just for nominal conditions without calibration.

The simulated Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) results at 875MS/s for a ramp up input for the two LSB capacitor versions are depicted in Figure 3.34. It can be seen that the second version (LSB_2) is more robust to implement the LSB capacitor of the lower side of the differential DAC. LSB_2 presents a DNL within 1.08/-0.51 LSB and the INL within -0.78/+0.6 LSB.

The output spectrum at 428.96MHz input frequency is shown in Figure 3.35. The ADC achieves a SNDR/SFDR of 41.46/55.01dB at Nyquist frequency for the LSB_2 version, presenting an overall improvement of 0.6ENOB with respect to the LSB_1 version, showing the advantage of the proposed modification for the LSB capacitor.

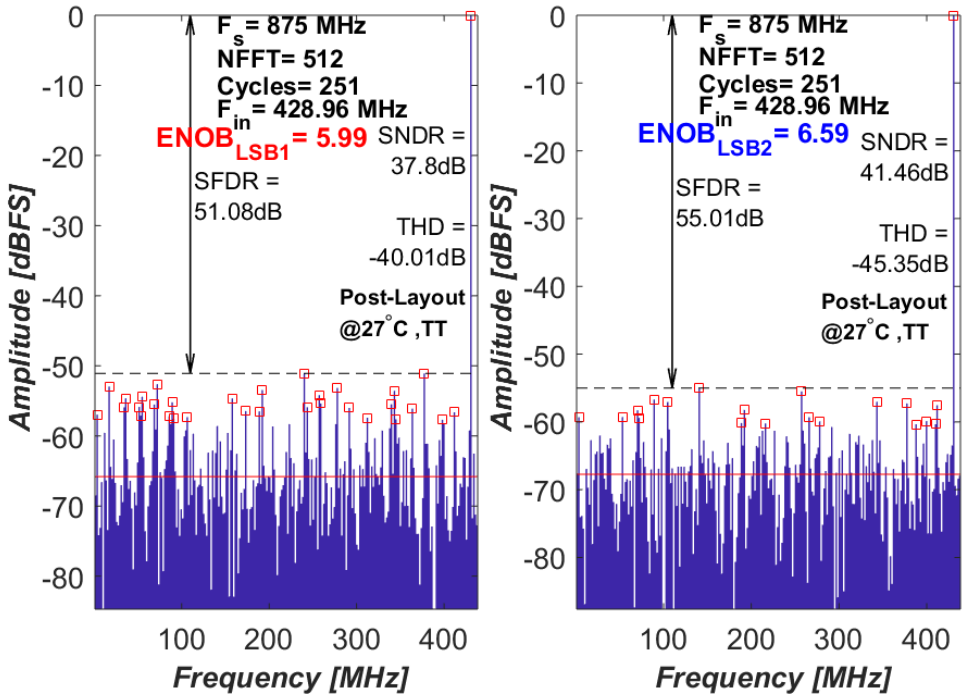


Figure 3.35: Output Spectrum with 0 dBFS signal applied at 428.96 MHz, sampling frequency is 875 MHz. LSB_1 (red) and LSB_2 (blue)

Table 3.4 shows a performance summary and comparison with recent state-of-the-art SAR ADCs of similar performance (as seen in Figure 3.36). The presented ADC achieves a comparable SNDR and lower FoM for a similar sampling rate (between 400MS/s ⇔ 1.25GS/s) and resolution (6 to 8-bit) while having a lower complexity and a smaller area.

Table 3.4: Perfomance Summary and Comparison with Single-Channel State-of-the-Art SAR ADCs

	This Work*	[51]+	[52]+	[46]+	[53]+
Technology [nm]	22nm FDSOI	28nm CMOS	65nm CMOS	32nm SOI	40nm CMOS
Architecture	SAR	SAR	2b/c SAR	2 comp. SAR	ci-SAR
Calibration	YES	NO	YES	YES	YES
Resolution [bits]	7	7	8	8	6
Supply [Volts]	0.8	1.0	1.2	1.0	1.0
Sampling Rate [GS/s]	0.875	1.25	0.4	1.2	1
Power Consumption [mW]	1.65	3.56	4.0	3.1	1.26
Active Area [mm^2]	0.00074	0.0071	0.024	0.0031	0.00058
SFDR@ Nyq. [dB]	55.01	52	53	49.8	49.7
SNDR@ Nyq. [dB]	41.46	40.1	40.4	39.3	34.6
FoM@Nyq. [fJ/conv-step]	19.5	34.4	116.9	34	28.7

+ Measured; *Post Layout

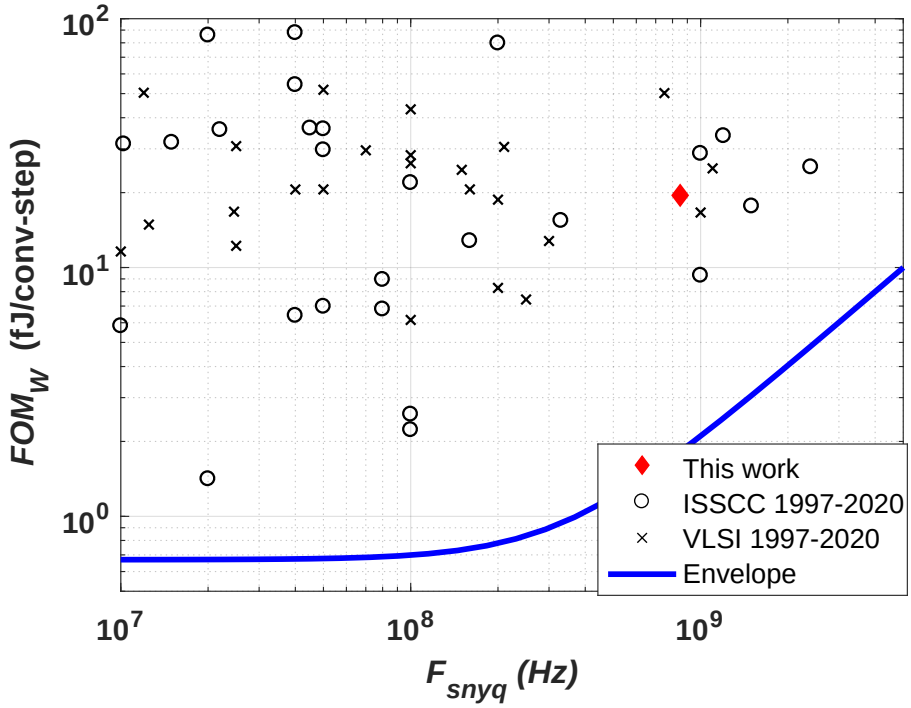


Figure 3.36: Comparison with state-of-the-art single-channel SAR based on [2]

3.6.2 TI-ADC

One of the main challenges was to simulate the hierarchical TH and the sub-ADCs in the same testbench. The sub-ADC has 1 clock domain of 875MHz. A sub-ADC transient simulation requires a time step of $t_{step,sub-ADC} < \frac{0.02}{F_{s,sub-ADC}} \approx 1UI$[5] to guarantee an error tolerance lower than 10^{-4}. The hierarchical TH requires a time step multiple of its 3 clock domains (28GHz, 3.5GHz and 875MHz). In this case, we choose the lowest multiple time $t_{step,TH} = \frac{0.02}{28GHz} = 0.01UI$ for the same accuracy. Those time steps are valid for separated simulations.

A simulation to obtain the TI-ADC dynamic parameters (SNDR, SDFR, THD) requires $t_{step,TH}$ for a simulation time of $t_{stop} = t_{s,sub-ADC} \times NFFT$[6]. For NFFT=512, data points require a total time of ≈585ns with time steps of 178.5fs[7].

This simulation could take a day or even several days depending of the desired accuracy. Instead of simulating all the blocks involved in the TI-ADC (sub-ADCs, hierarchical TH and clock generator) the following approach is taken:

- parameter extraction of the hierarchical TH, sub-ADC and clock generator relevant to the TI-ADC (resolution, non-linearity and mismatches),
- a simulink model is elaborated using the information of Table 3.5,
- parametric simulations are performed to evaluate the TI-ADC.

Table 3.5 shows the TI-ADC mismatch, static and dynamic error budget. The static (DNL and INL) and dynamic (SDFR, THD) are taken from the sub-ADC. The offset, gain error are obtained from the hierarchical TH. The timing error is taken from the clock generator. The random jitter and dual-dirac jitter are taken from a 28GHz NRZ CDR clock in 22nm CMOS FDSOI as reference.

Figure 3.37 shows the output spectrum of the SAR-ADC model. The model includes aperture jitter, DNL, INL, SFDR and THD. The model was implemented to

[5] $1UI = \frac{1}{Fs} = 17.85ps$ used as reference time unit

[6] NFFT: Number of data points in the sampling window or FFT

[7] A PLS of the sub-ADC takes ≈4h for dynamic parameters and ≈9h for static parameters to complete

Table 3.5: TI-ADC mismatch, static and dynamic error budget. Maximum Values

Parameter	Value
Random jitter (σ_{RJ})[1] (%UI)	0.34
Dual-Dirac jitter, peak (A_{DD})[1] (%UI)	1.6
DNL[2]	[0.1 0.8 1] LSB
INL[2]	[0.1 1 1.5] LSB
SFDR[2]	55dBc
2-nd Harmonic Distortion (HD2)	65dBc
3-rd Harmonic Distortion (HD3)	70dBc
Offset Error (LSB)[2]	[-0.5 0.5]
Gain Error (%FS)[3]	[-0.05 0.05]
Timing Error(%UI)[4]	[-0.05 0.05]

[1]From CDR clock at 28GHz in 22nm FDX. Typical process values
[2]Obtained from PLS
[3]Estimated from Hierarchical TH
[4]Estimated from the clock generator

match the circuit at PLS. The model allows us a great flexibility to evaluate different parameter values. The aperture jitter was modeled as a normal random variable using the random and Dual-Dirac jitter references.

The DNL/INL was modeled as a uniform random variable assuring maximum randomness. It should be noted that we are restricted to choose either of the two positive or negative values for both the DNL and INL and do not intend to involve circuit or infrastructure level properties.

The THD is modeled by defining the input frequency (F_{in}) as a variable, creating a waveform with amplitude equivalent to the i-th Harmonic Distortion (HDi) and frequency ($i \times F_{in}$) and add them up to the input. The model considers harmonics up to the HD_3 but more harmonics can be added. The SFDR is generated by creating an harmonic at the spur's frequency and applying the relevant amplitude.

Figure 3.38 presents the output spectrum of the TI-ADC model with mismatches. The model is constructed using the sub-ADC model as building block. The mismatches

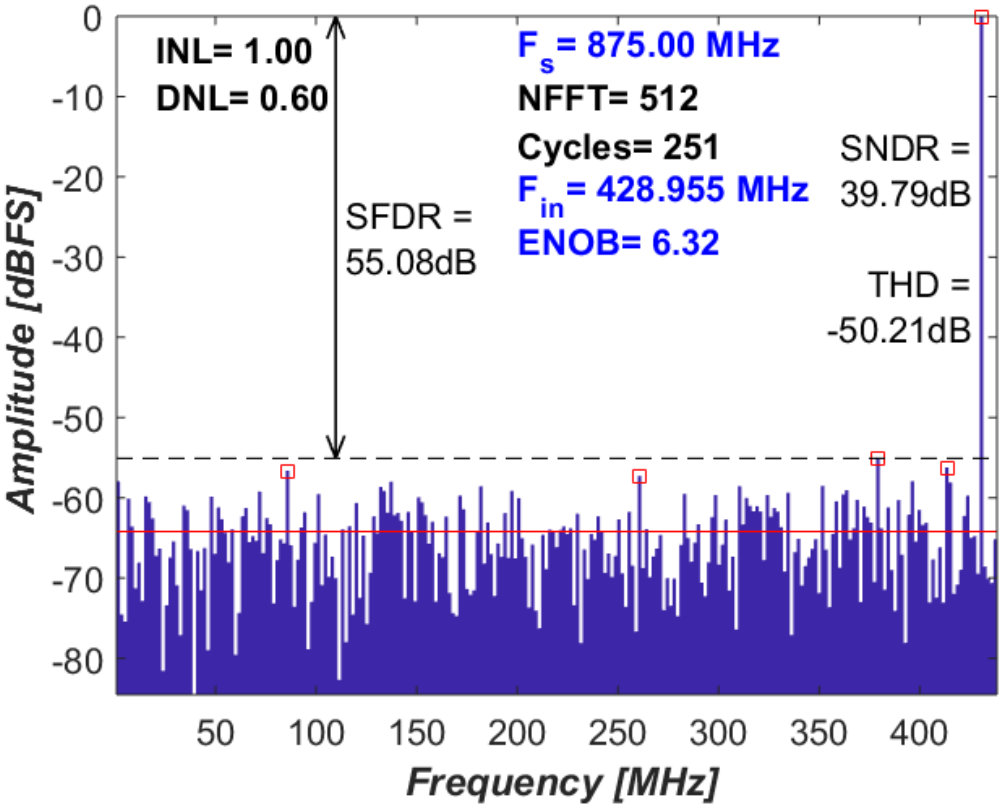


Figure 3.37: Output Spectrum for the SAR-ADC model in simulink.

are modeled as uniform random variables. The offset is obtained from the sub-ADC calibration results and represented in LSB.

The gain mismatches are estimated from hierarchical TH. The total gain variation is considered as the contribution of the 3 ranks. A gain control of (+/- 25%) in the last rank was implemented to avoid saturation at the input of the sub-ADC. The timing mismatches were represented as a percentage of 1UI and estimated from the clock generator.

The mismatch error values taken for this simulation were conservative. For that reason, the obtained SNDR of 35dB (ENOB=5.5 bits) can be considered as a good approximation of the complete TI-ADC behaviour.

A parametric simulation for the different mismatches were performed. Figure 3.40 summarizes the parametric simulation. It compares the ENOB vs DNL/INL for a

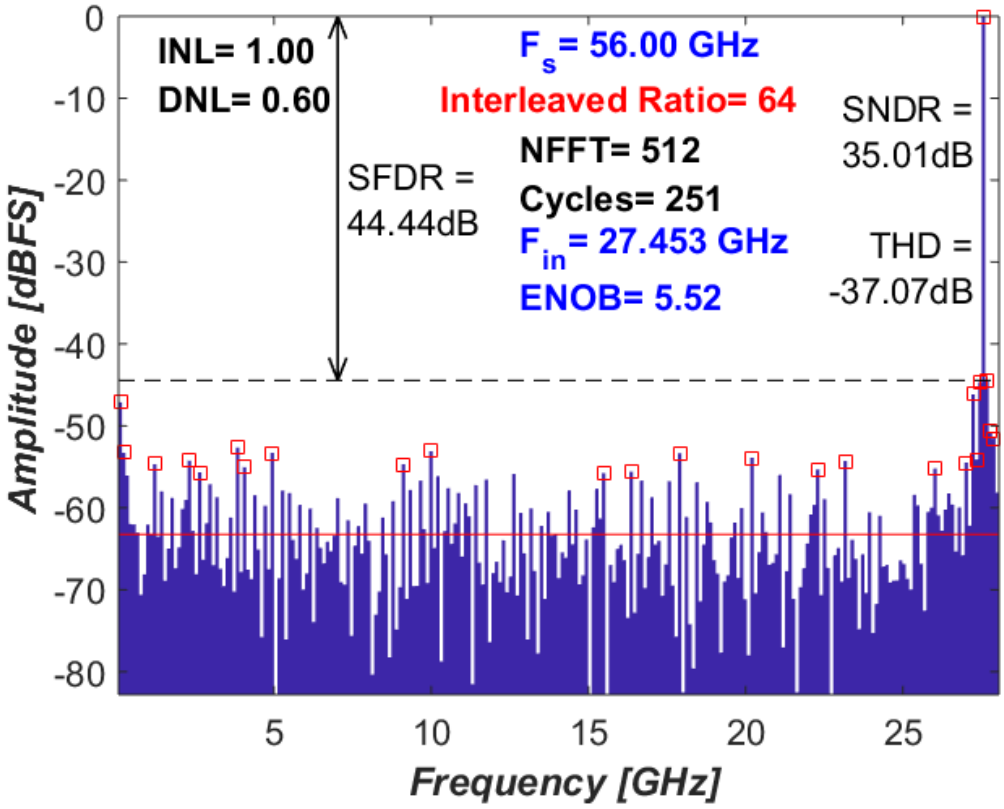


Figure 3.38: Output Spectrum for the TI-ADC model with mismatches.

mismatch parameter set up. The TI-ADC with no mismatches and the default value of DNL/INL represent the maximum achievable ENOB=5.86 bits. A more realistic case is represented by the delimited box. The actual value of the ENOB will be found in this region. Under this condition, a ENOB of 5 bits is expected for a conservative set of parameters.

The TI-ADC power consumption breakdown is shown in Figure 3.40. It consists of 113.5mW for the hierarchical TH, 105.6mW for the 64 sub-ADCs and 69.6mW for the clock generator. The circuits were designed to optimize power and the power constraint of 500mW was maintained.

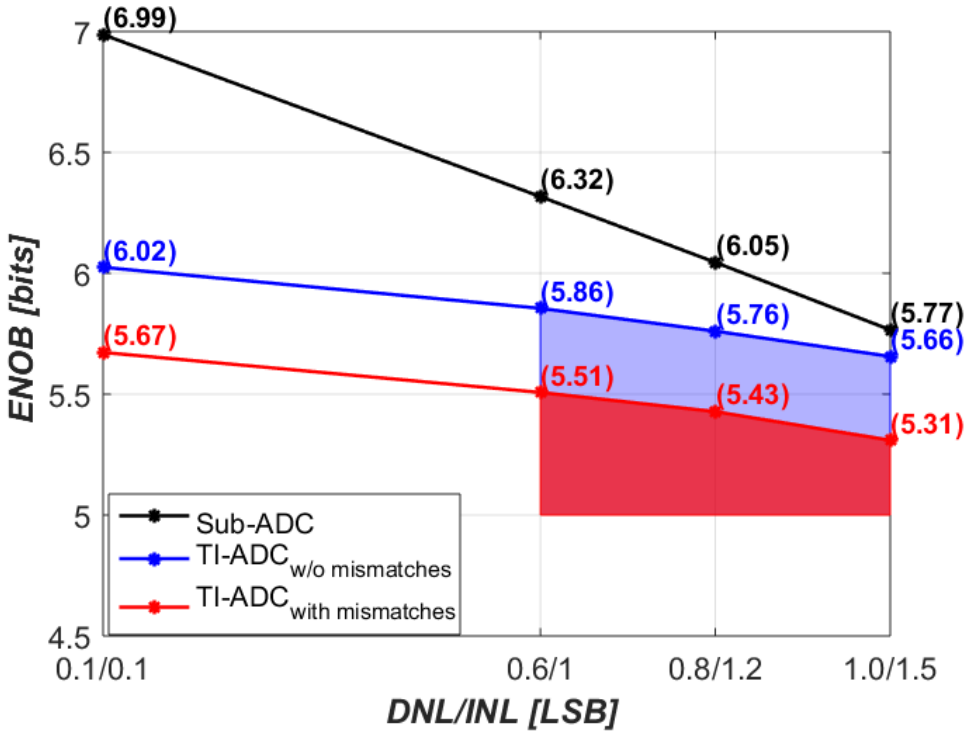


Figure 3.39: TI-ADC ENOB vs Non-linearity errors

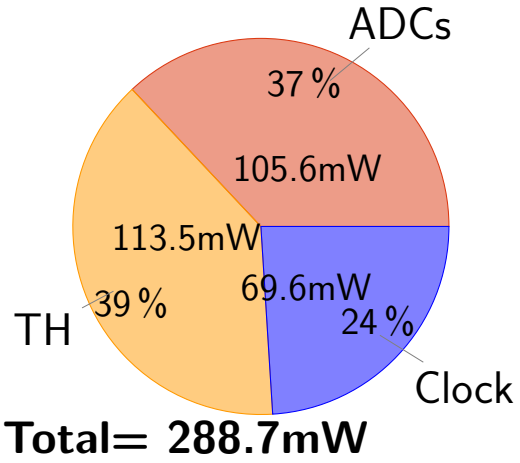


Figure 3.40: TI-ADC power consumption breakdown.

3.7 Conclusion

In this chapter, we have presented the design of a high speed TI-ADC. A design flow was introduced to breakdown the principal aspects of the design:

1. The use of hierarchical sampling can optimize the number of low-jitter clock signals and simplify the distribution of non-critical clocks,
2. The suppression and calibration of DCD have been implemented for the low-jitter clocks,
3. The design using the 22FDX^{TM} platform allows a power efficient design and flexible design through back gate biasing,
4. The designed sub-ADC design has achieved,
    - A power- and area-efficient 7-bit 875MS/s SAR ADC has been demonstrated,
    - An improvement for the CDAC LSB capacitor allows a substantial improvement in the SNDR,
    - A simple and accurate calibration procedure for the comparator and ADC is presented.
5. The TI-ADC design has demonstrated that:
    - A fast and accurate simulink model was developed to evaluate the design and speed up the simulations,
    - An ENOB above 5 bits can be expected using a conservative set of static, dynamic and mismatches parameters.

These results demonstrated an optimized TI-ADC design with medium resolution that supports 56GS/s operation.

Chapter 4

ADC-RX prototype and prospects

Contents

Chapter 4 presents the physical implementation of an ADC-based receiver prototype in 22nm CMOS FDSOI technology. It includes the TI-ADC developed in chapter 3 and other blocks that complete the design. A testbench to perform characterization of the receiver and several aspects to improve the current design are discussed.

4.1 ADC-RX prototype

4.1.1 Top-level diagram

A chip prototype called ADC-RX is prepared. Figure 4.1 shows the top-level diagram of the prototype. The design implements an ADC-based receiver consisting of:

- An AFE consisting of a CTLE for pre-equalization and gain boosting. It includes a 50Ω matching, offset and gain calibration,
- A 56GS/s 64-way 7-bit SAR TI-ADC. It includes offset and gain calibration,
- A clock generator for the TI-ADC and digital controller. It generates all the required clocks from an external signal clock of 28GHz,
- A retimer to resample the TI-ADC outputs into a single clock domain. Special considerations are taken to keep aligned the samples in the correct order,
- A 64kbits SRAM memory to store 8192 samples (7-bit per sample). The memory is made out of 16kbits from the IP provider INVECAS,
- A Digital Controller for calibration and memory control. It includes an array of registers for calibration and the I^2C protocol for off-chip interface.

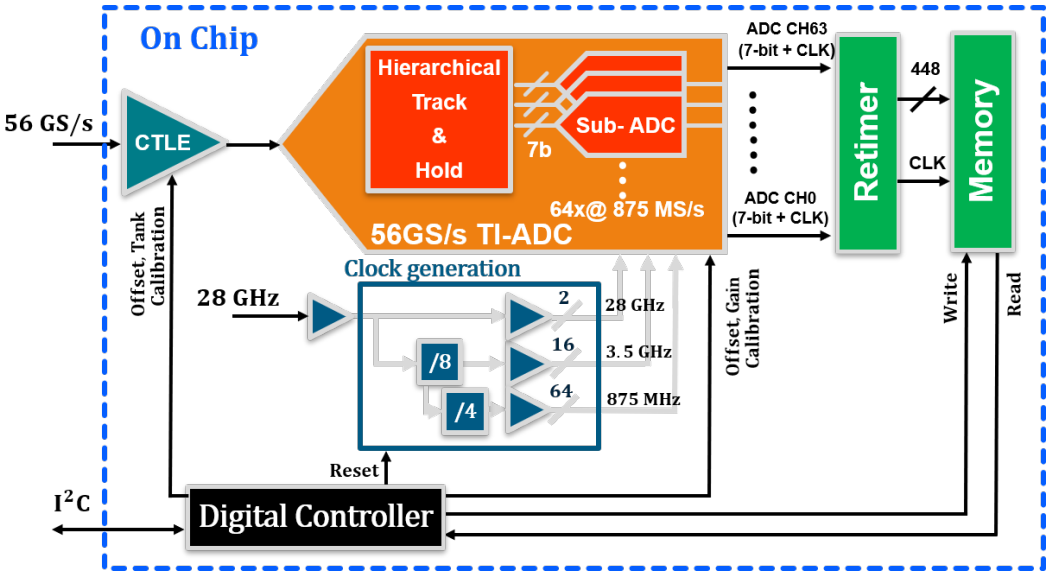


Figure 4.1: Diagram of 112 Gb/s PAM4 ADC-based receiver.

The top level diagram of AFE is shown is Figure 4.2. It is composed of 3 main blocks: a 50Ω termination, a CTLE and a back gate biasing DAC.

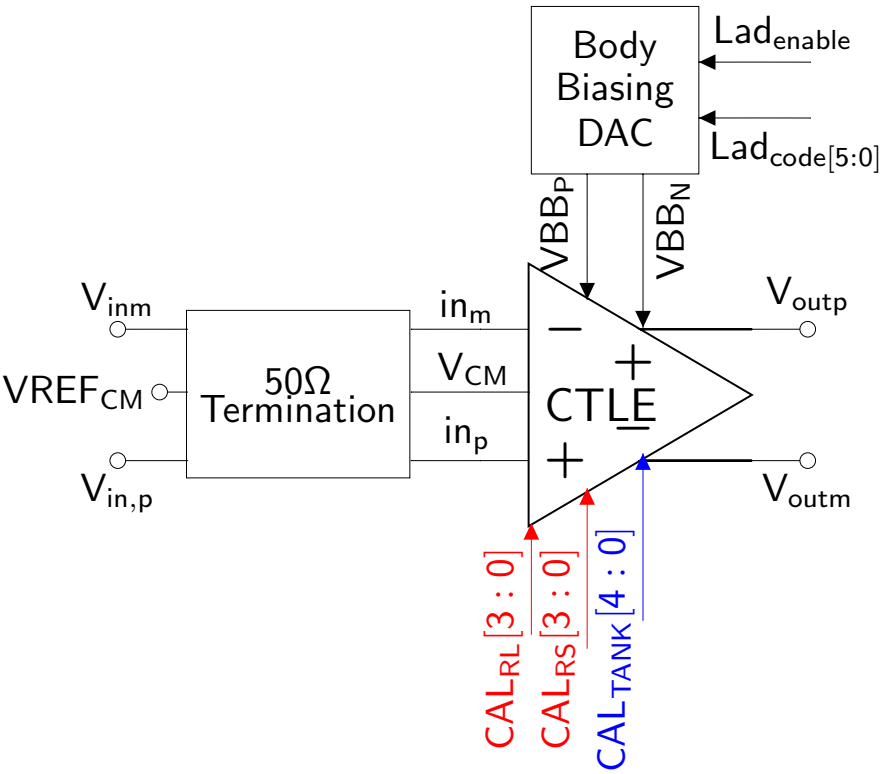


Figure 4.2: CTLE top diagram.

The 50Ω termination is an input passive matching network to compensate the parasitic capacitance from the PAD. It employs a custom built T-coil inductor for high frequency peaking (as seen in Figure 4.3a).

A CML-based CTLE stage to provide pre-equalization and signal conditioning to the input of the TI-ADC (as seen in Figure 4.3b). It uses a source degenerated differential pair to achieve high frequency peaking. It has the following features:

- An input Common Mode Feedback (CMFB) circuit to control the common mode voltage at the input,
- A programmable high-frequency peaking gain trough the load resistance R_L and source resistance (R_S) using a 4-bit word control,
- A programmable peaking frequency (28GHz) using a 5-bit RC-tank (R_{tank} and C_{tank}) and a custom built inductor load L,
- Offset mismatch calibration using back gate biasing through 5-bit resistor DAC

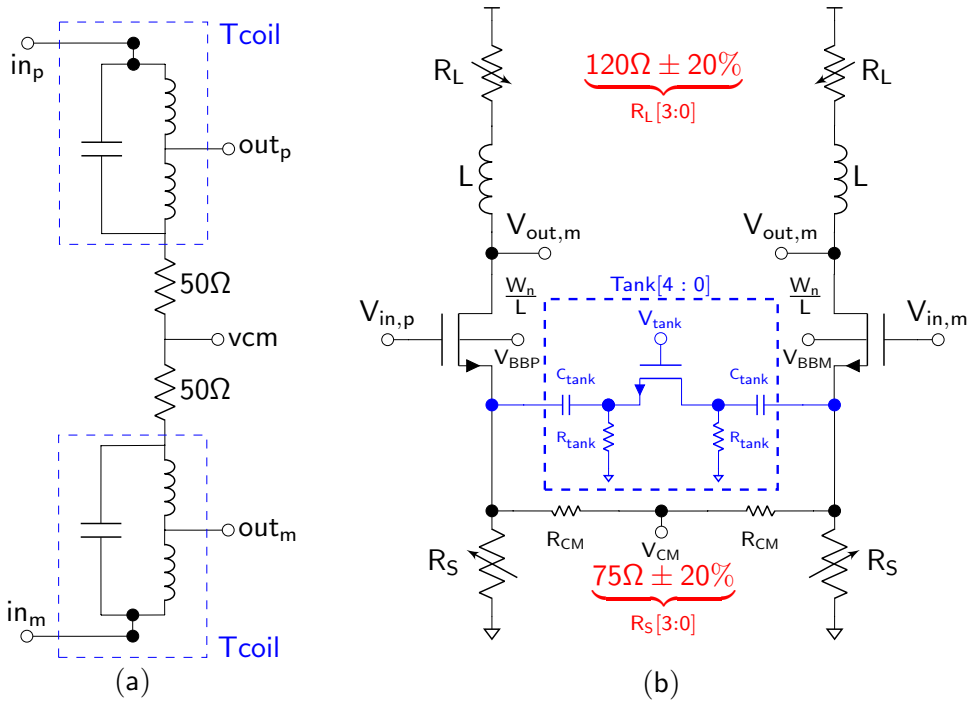


Figure 4.3: (a) 50Ω termination circuit. (b) Schematic diagram.

(see Appendix B.1.3).

- A variable supply voltage with 1V of nominal value. The CTLE output defines the input common mode of the rank-1 buffer.

The CTLE simulation parameters at nominal corner are summarized in Table 4.1. The input common mode of 0.56V is controlled by the input CMFB circuit to fix a voltage of 0.3V across the source resistors R_S. The differential pair requires a minimum V_{DS} of 450mV to keep a good linearity. This generates an output common mode of 0.75V for the input transistors of the rank-1 buffer.

Due to the fact that the CTLE was designed after the hierarchical TH, a change in the input transistors of the rank-1 buffer was required. The reason behind it was to keep the same output common mode of 0.35V for the buffers while having an increment of ≈120mV in the input common mode. The transistors were change to the standard V_t (SVT) NMOS in order to keep the same transconductance efficiency

Table 4.1: CTLE Parameters at Nominal Corner (T=27°C)

Supply	1V
Input Common Mode[1]	0.56V
Output Common Mode[2]	0.75V
Load resistance (R_L)	120Ω
Source resistance (R_S)	75Ω
Resistor Code[3]	8
Tank Code[3]	31
DC gain	-12dB
Peaking gain[4]	11.5dB
Peaking gain frequency[5]	33GHz
Power Consumption	11.5mW

[1]Controled by the input CMFB
[2]Required for linearity
[3]Default values
[4]4-bit DAC calibration
[5]5-bit DAC calibration

(g_m/I_D). Thus, the buffer speed or power consumption were not altered.

The CTLE stage was designed to have a constant-DC gain (≈-12dB) and a programmable peaking gain (up to 12.5dB) controlled by R_L and R_S. The peaking gain frequency is programmable too (up ≈41GHz) and is controlled by the RC-tank. Compared with a constant peaking gain CTLE (with programmable DC gain), the constant-DC gain CTLE can either reduce the required gain of the hierarchical TH at high-loss channels and/or improve the linearity of rank-1 buffer at low-loss channels.

Figure 4.4 presents the CTLE transfer function for the nominal, slow and fast corners for the resistor and RC tank default codes of 8 and 31, respectively. A CTLE design with minimum parameters variation is demonstrated for the worst case corners and temperature. The programmability of the peaking gain and frequency of the CTLE is shown in Figures 4.5 and 4.6, respectively. A range variation of ≈2dB with linear increment steps of 0.29dB is achieved for the peaking gain. The peaking frequency starting in 33GHz can be programmed up to 41.67GHz with linear steps of 0.27GHz.

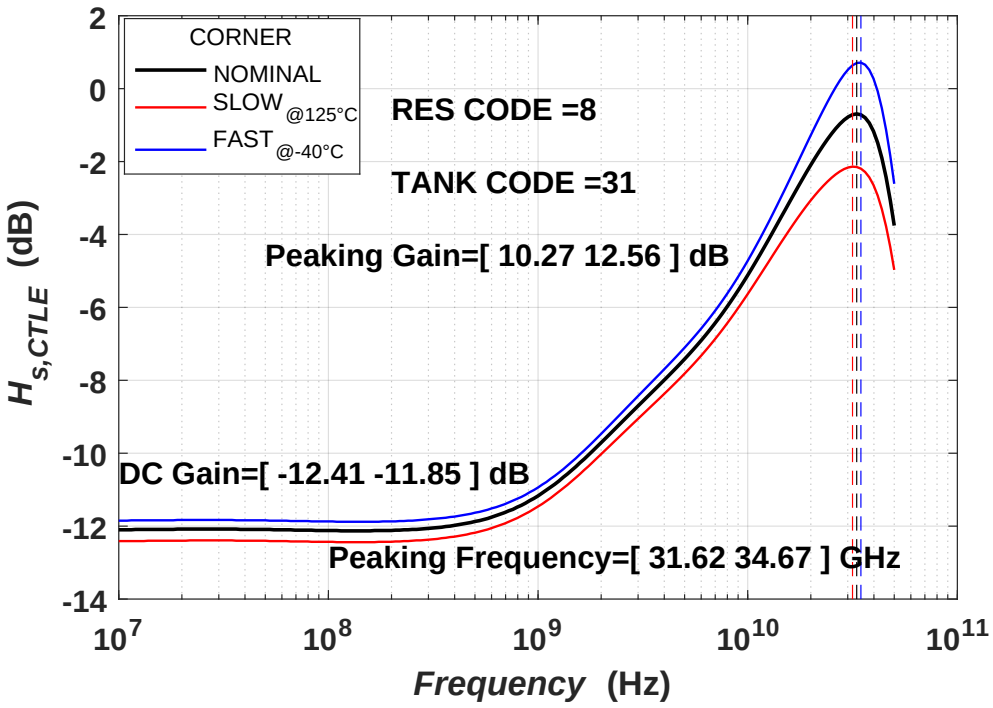


Figure 4.4: CTLE transfer function for nominal, slow and fast corners

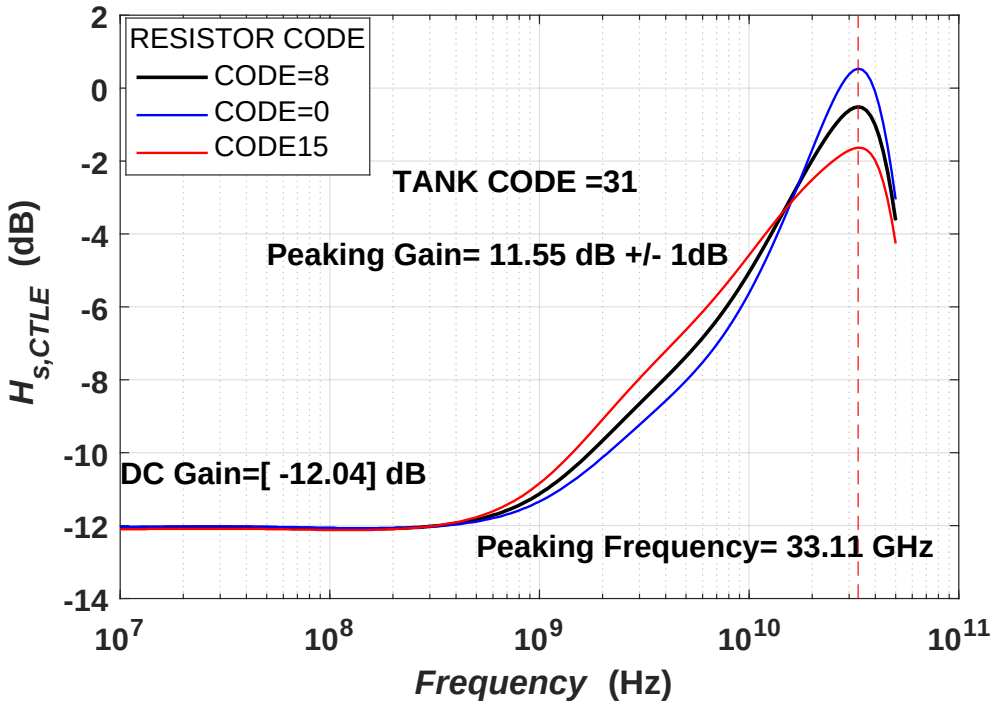


Figure 4.5: Programmability of the peaking gain

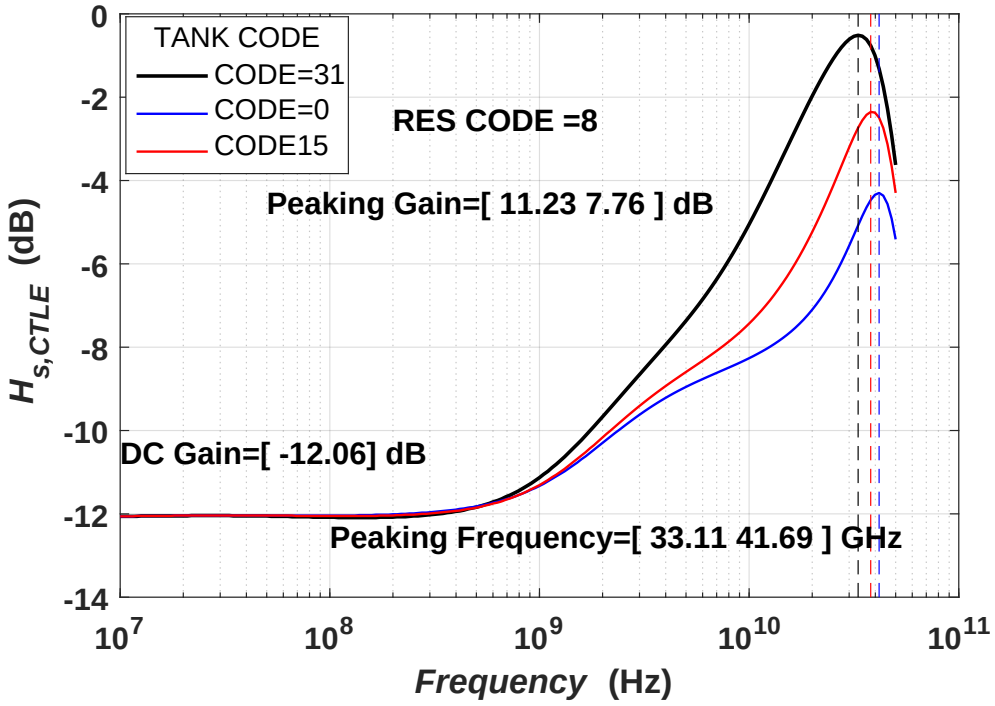


Figure 4.6: Programmability of the peaking frequency

The retimer receives the outputs from the TI-ADC and aligns the multi-phased sub-ADCs outputs into a single 875MHz clock domain. These retimed outputs are stored in a 64kbits SRAM (8912 samples/7-bit per sample). An important aspect to take in consideration is the selection of the clock phase. It will determine the order of stored samples. The ADC clock domains are spread every UI (1UI=17.86ps) and therefore cannot be resampled directly using a single clock phase. As a matter of fact, if a setup of 2UI and a hold of 1UI need to be maintained for the resampling FFD, any of the ADC clocks will violate this condition. Two cases for the retimer clock phase were evaluated.

For instance, in the first case, if using the clock of ADC[0], sampling directly the outputs of ADC 1 to 60 is possible but ADC 61, 62, 63 and 0 will be updating their samples during the aperture time of the FF. In order to mitigate this timing violation, an intermediate clock can be used to stretch the validity of these 4 ADC outputs by inserting an extra FFD and hence guarantee steady outputs when finally resampling using clock of ADC[0]. The intermediate clock domain could be anything between 2 and 60. The net result of this resampling scheme is that the sample order will become 61, 62, 63, 0, 1, ... 60. The first case using ADC[0] clock is summarized as:

- Direct samples: 1 to 60 retimed with phase [0],
- Indirect samples: 61, 62, 63 and 0 retimed with phase [0] and intermediate clock phase between [4:57],
- Retimer sample order: 61, 62, 63, 0, 1, 2 ... 57, 58, 59 and 60.

Analyzing this reshuffling, it can be shown that by selecting ADC[3] to start with, we can get the ADC samples in the right order:

- Direct samples: 4 to 63 retimed with phase [3],
- Indirect samples: 0, 1, 2 and 3 retimed with phase [3] and intermediate clock phase between [7:62],
- Retimer sample order: 0, 1, 2, 3, 4, 5 ... 60, 61, 62 and 63.

Figure 4.7 depicts the direct and indirect retiming for the ADC clock phase [3]. The clock phase going to the retimer is distributed using the clock tree presented in Figure 4.8. The clock tree is distributed through 3 stages of buffering. Each stage of buffer sees at most 4 equivalent loads. Figure 4.9 shows the time diagram for the 2 cases. A consecutive sample order can be obtained using the clock phase [3].

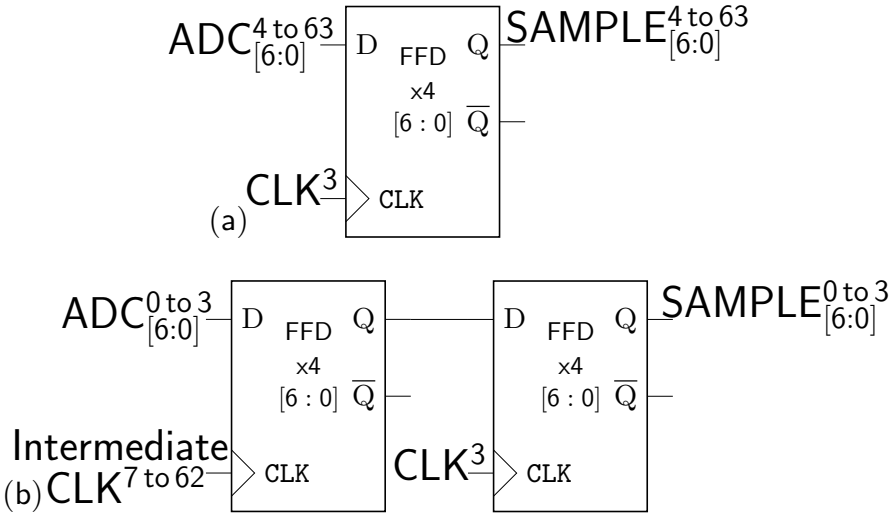


Figure 4.7: (a) Direct retiming. (b) Indirect retiming for clock phase [3]

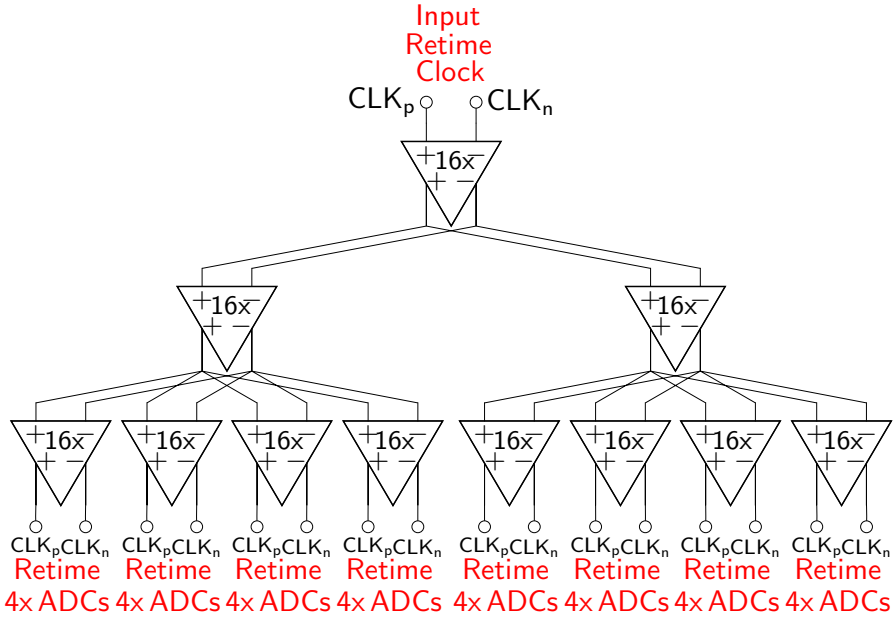


Figure 4.8: Retimer clock tree for 32x sub-ADCs.

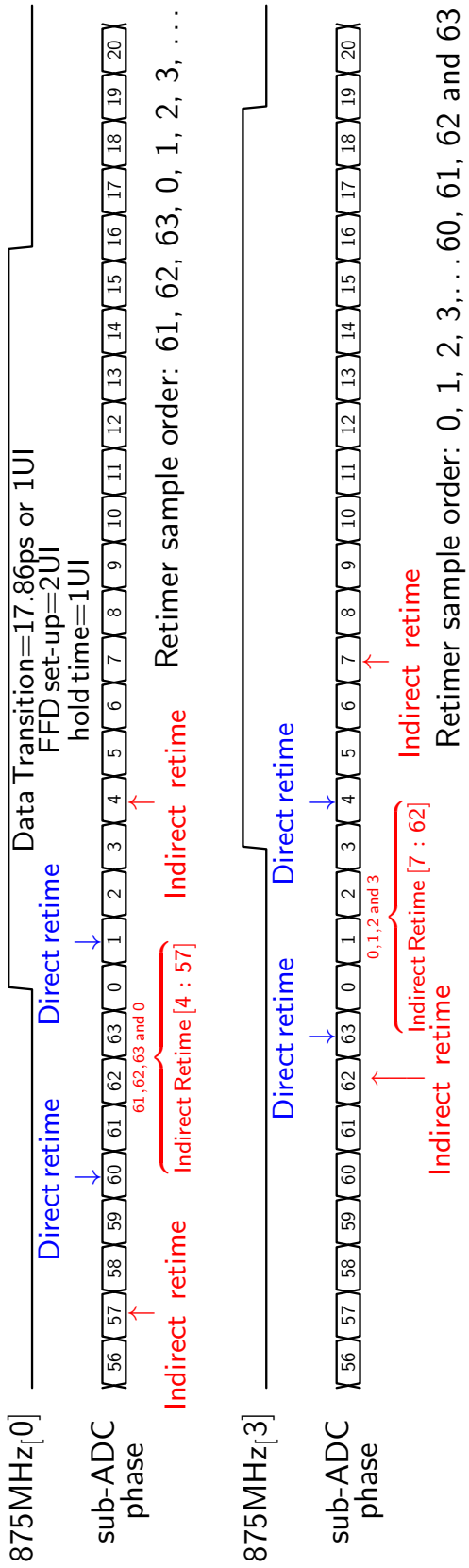


Figure 4.9: Timing Diagram of the Retimer.

4.1.2 Chip layout

In this subsection, we discuss the physical implementation of the internal blocks of the ADC-RX chip. The AFE layout is depicted in Figure 4.2. The layout is implemented to have a full symmetry on the vertical axis. It includes:

- The 50Ω termination, where the T-coil inductors occupied most of the area,
- The CTLE core includes the NMOS differential pair, R_L, R_S and the RC-tank. Closely to the 50% of area is occupied by the programmable RC-tank,
- The decoders for R_L, R_S and RC-tank. They are composed by a static logic cells which takes the input word control and enables the programmable peaking gain and frequency.

Additionally, an empty space at the output of the CTLE is left for the buffer of rank-1 to minimize interconnection routing. The complete layout occupies an active area of 99µm × 143µm and is shown in Figure 4.10.

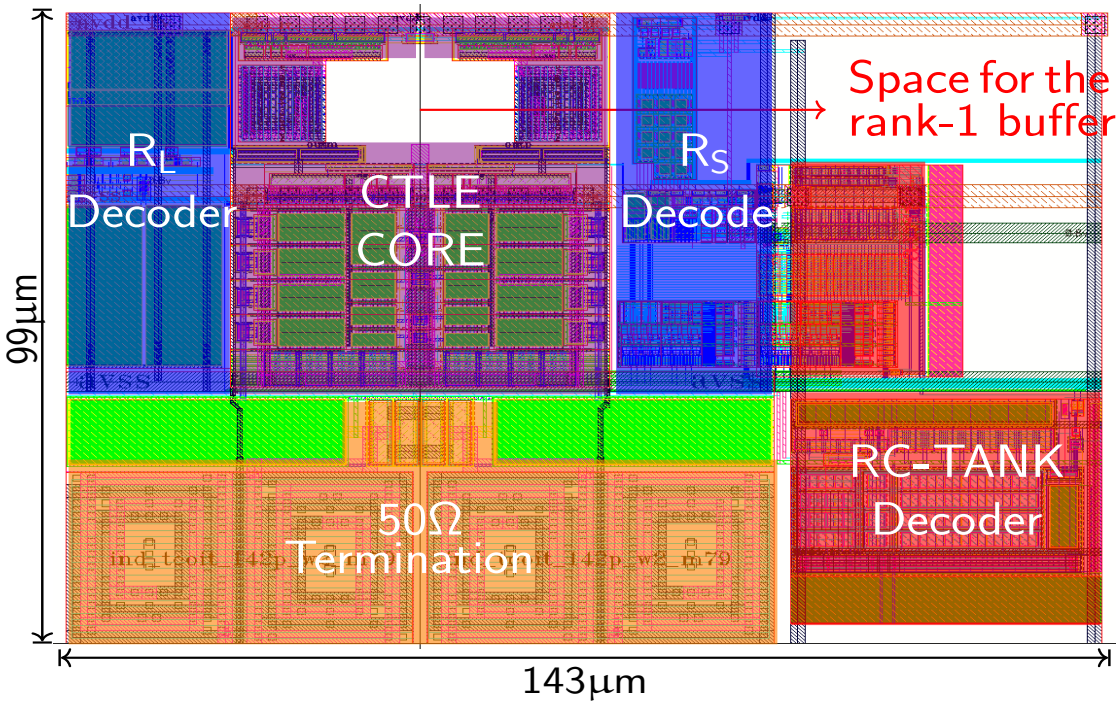


Figure 4.10: CTLE layout.

The floorplanning of the TI-ADC is presented in Figure 4.11. The layout was implemented using the following guidelines:

- The samplers, gain stages and ADCs were placed according to the clock phase in each TH rank,
- A symmetrical metal routing was implemented to guarantee the same delay between consecutive ranks,
- The even and odd clock phases were formed in 2 groups per rank. In this way the output interconnection between ranks was minimized,
- The ADCs were placed in 2 rows of 32 each in order to avoid a large metal connection to the ADCs on the sides,
- A space between the ADCs rows was reserved to the retimer and clock signal routing,
- The right side routing was reserved for high speed routing (clock signals) and the left side for low frequency routing (biasing, calibration and ATP).

The TI-ADC layout is depicted in Figure 4.12. It shows each of the 3 ranks of the hierarchical TH and the 2 rows of 32x ADCs. The calibration, current reference and Analog Test Point (ATP) signals were routed on the left side while the clock signals for each rank on the left.

The retimer and the complete TI-ADC occupy an active area of 40µm × 417µm and 296µm × 425µm, respectively.

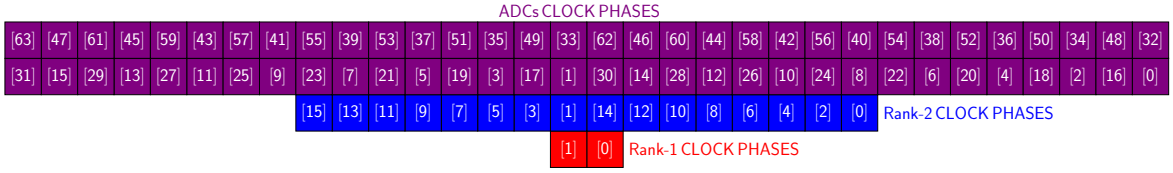


Figure 4.11: TI-ADC Floorplanning.

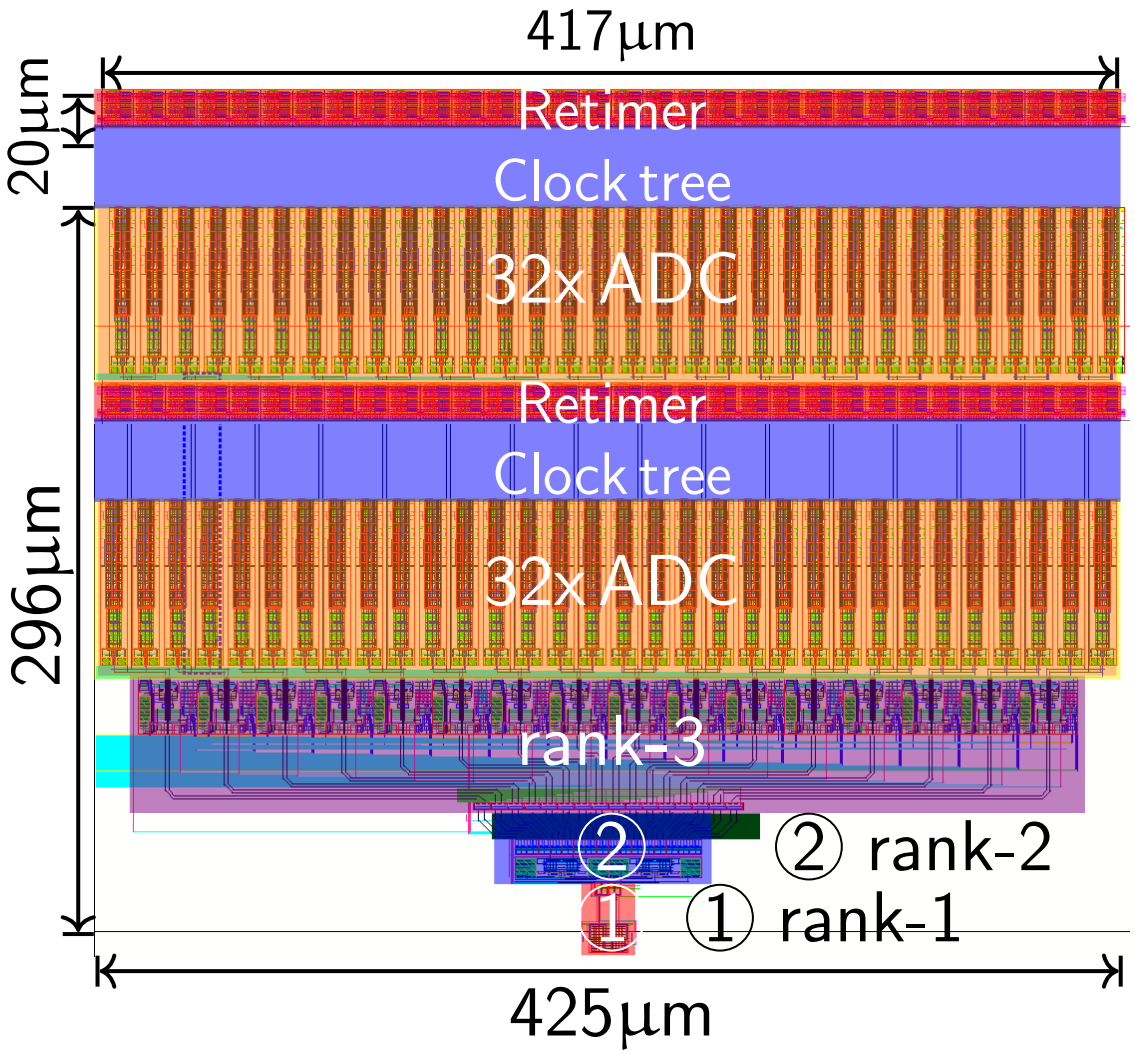


Figure 4.12: 7-bit 56GS/s 64-Way TI-ADC layout.

The clock generator layout is shown in Figure 4.13a. It occupies an active area of 88µm × 331µm. The layout was placed on the lower right side of the TI-ADC. Its position relative to the rank samplers was chosen to minimize the metal routing for the rank-1 and rank-2. Thick metals layers were used to route the clock signals going to the samplers and ADCs.

The layout floorplan was organized to leave room for routing and enable sufficient space between adjacent clock signals for parasitic coupling capacitance reduction. The clock buffers were designed to optimize delay. The parasitic capacitance load was

extracted from layout and modeled as a differential transmission line.

Figure 4.13b depicts the ADCs clock routing. The clock generator was placed to the bottom right of the TI-ADC closer to rank-1 and rank-2. Its is shown the clock distribution going to the 2 rows of 32x ADCs coming from rank-3. Special attention was taken to match all the clock routing paths to have the same parasitic routing capacitance. Thus, all paths present the same delay.

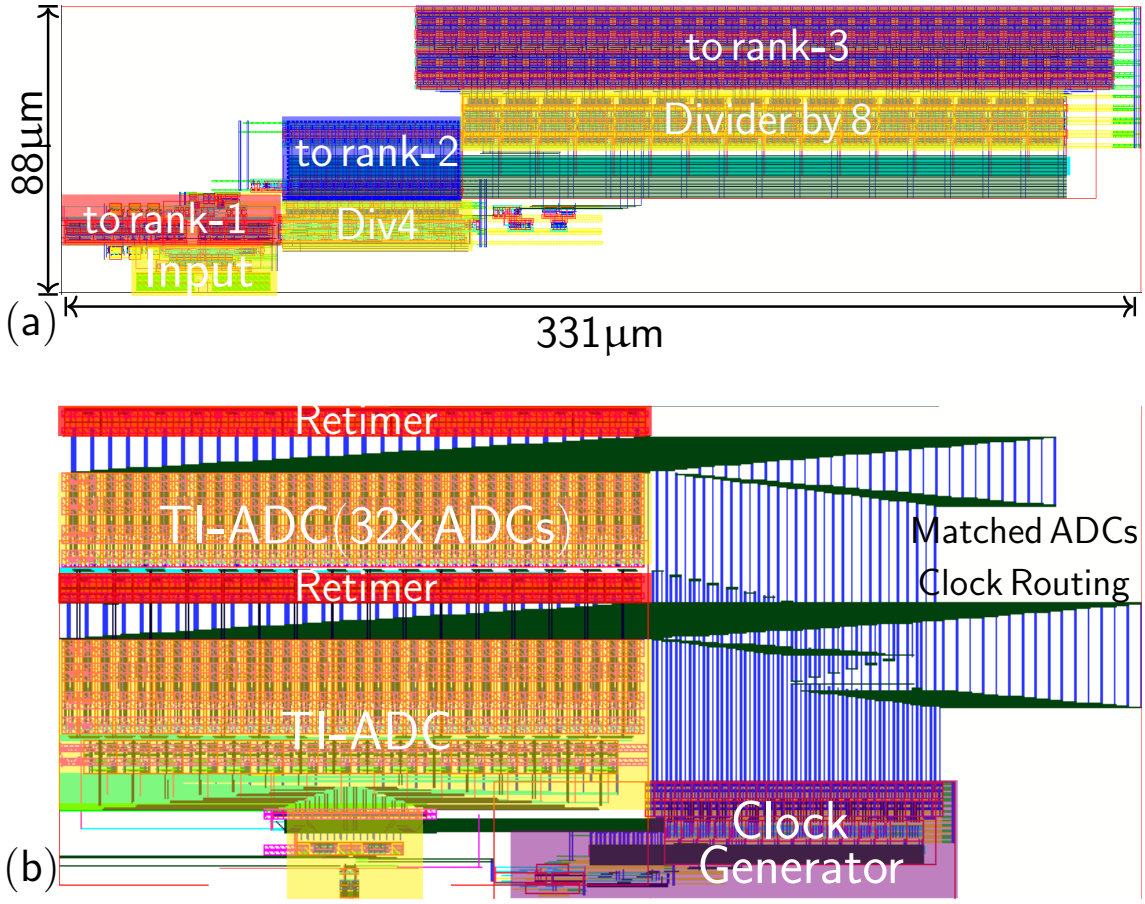


Figure 4.13: (a) Clock generator layout. (b) ADCs clock routing detail

The ADC-RX chip was implemented in 22nm CMOS FDSOI. It is composed by the following structures and characteristics:

- It is a PAD limited design with a total of 44 PADs. The aspect ratio is 1 with 11 PADs per side. The top PAD row corresponds to the I^2C interface with digital IOs. The input signal and external clock are located in the bottom row. The voltage supplies and ground are placed in the lateral pad rows,

- The biasing generates source and sink currents of 500µA, 250µA and 50µA from a low TC ($\leq$58-ppm/°C) 10µA current source reference. The current reference is generated using a sub-1V bandgap voltage reference. It occupies an active area of 218µm × 429µm,

- The calibration ladders generate the back gate biasing control. It presents 4 modes of configuration using ground, 0.8V and 1.6V references. It occupies an active area of 150µm × 175µm,

- The CTLE as pre-equalizer. It includes a common mode voltage reference V_{CM}. It occupies an active area of 118µm × 143µm,

- The TI-ADC and retimer for data conversion. They occupy an active area of 345µm × 425µm,

- The clock generator occupies an active area of 88µm × 331µm,

- A High Density Single-Port SRAM cell-based Register File Memory Compiler from INVECAS. The size is 64kbits (7 bits x 8192 is the requirement = 57.3kbits) made out of 4 units of 16kbits. It is implemented with a high density 0.11088μm^2 bit cell,

- A programmable frequency ring oscillator and Power-on-Reset (POR) unit for the digital controller. They occupy an active area of 7.5µm × 24µm and 29µm × 159µm, respectively,

- Decoupling capacitors C_{decap} to suppress high-frequency noise in power supply signals are added whenever possible in the chip.

The complete chip layout is depicted in Figure 4.14 and has a total and active area of 2.044mm^2 and 0.86mm^2, respectively.

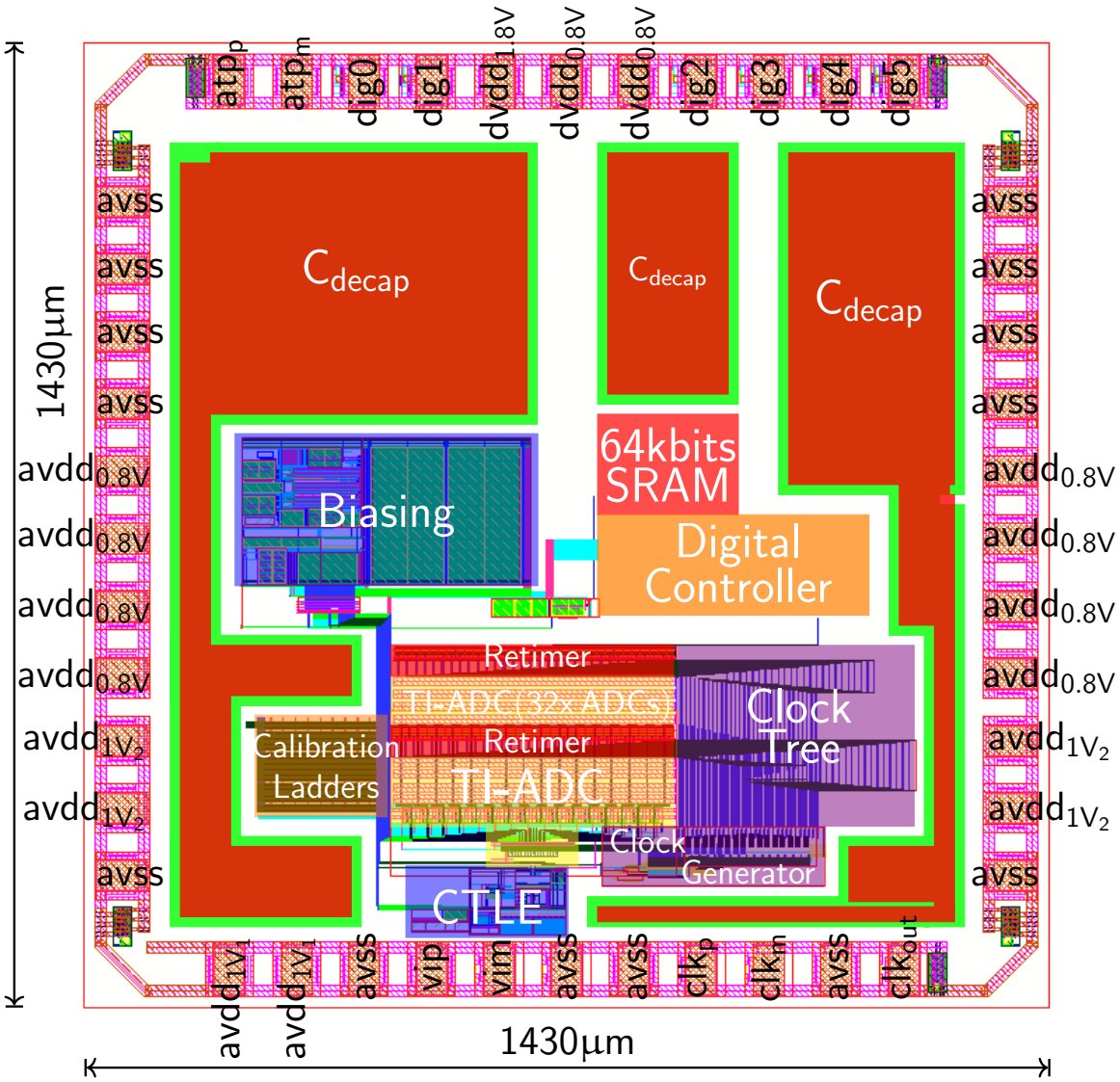


Figure 4.14: Chip layout.

4.2 Prospects

4.2.1 Chip Tapeout

The first tapeout of our ADC-based receiver will include:

- The AFE and TI-ADC with clock generator,
- Internal 64kbits memory for sample storage,
- Digital controller for calibration, memory controller and low speed serial interface to the outside (I^2C).

Figure 4.15 shows the lab setup for the chip characterization:

- An external Bit Error Rate Tester (BERT) will provide PAM4 encoded data at 56GBaud. It will also provide half rate clock at 28GHz which will be used internally to trigger the ADC in a synchronous fashion. The phase of this clock is adjustable and can be optimized externally,
- Different types of channels will be inserted between the BERT and the DUT, starting with point blank configuration (minimum loss),
- Data capture card: this microcontroller will implement the interface between the lab computer and the serial interface of the Device Under Test (DUT).

This characterization will be done:

1. At the block level, for ADC performance: measurements including DNL, INL, SNDR, SFDR, ENOB and THD before and after calibration,
2. At the system level: a full phase lock loop behavior can be implemented by controlling the phase of the BERT versus the incoming data based on a baud rate phase detector implemented off chip. DFE and FFE capabilities can be added as well and trained based on the ADC samples. Finally, the BER performance of a receiver based on this TI-ADC can be measured.

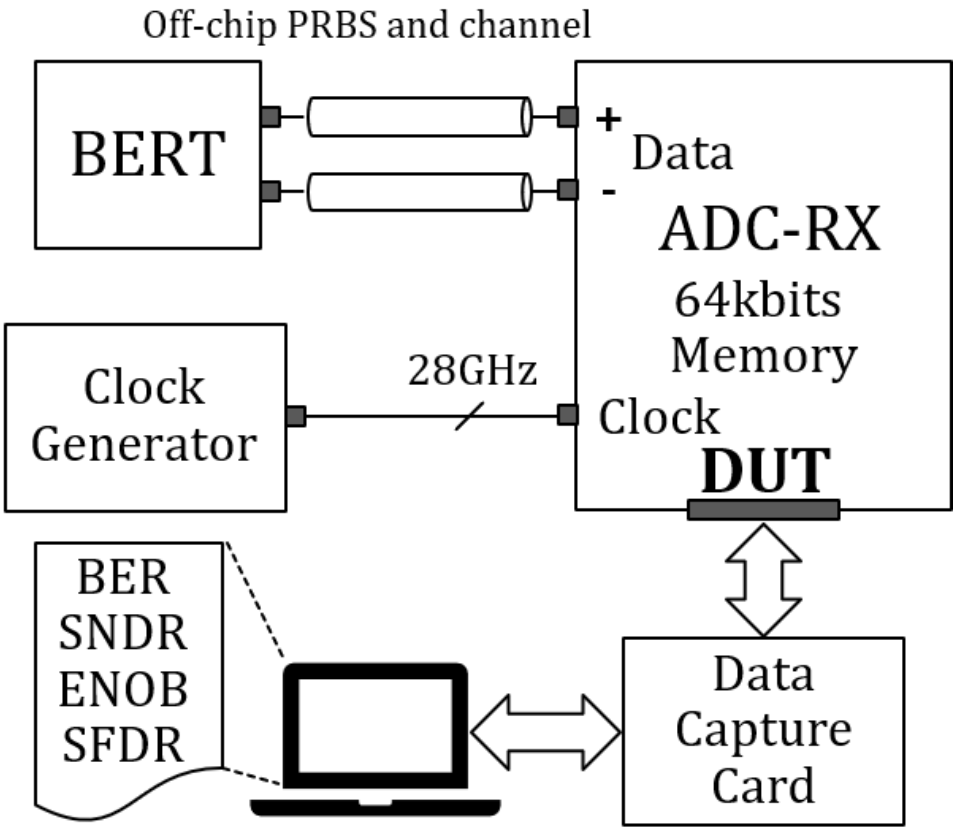


Figure 4.15: Prototype measurement set-up.

4.2.2 Speed augmentation and improvements

The next immediate standard of 100GbE for single lane operation will require a speed augmentation of 2x. The sampling frequency of our TI-ADC can be doubled to 112GS/s by increasing the ISR of rank-1. Figure 4.16 shows the modification of rank-1 to increase the ISR to 4. It will require an additional source-follower sampler[1]. This sampler should be clocked in quadrature phase relative to the original sampler.

The addition of the extra sampler has two effects on the bandwidth and functionality required by the TI-ADC. First, the input capacitance of the hierarchical TH would be doubled. Thus, a readjustment in the CTLE's output load will be needed in order to maintain the gain boosting at Nyquist frequency.

[1]The additional rank-1 circuitry introduce additional gain and offset mismatches.

The second effect is the group delay of the two source-followers samplers may no longer match. This will require a timing correction of the quadrature clock fed to the additional sampler. This correction can be implemented using a phase interpolator.

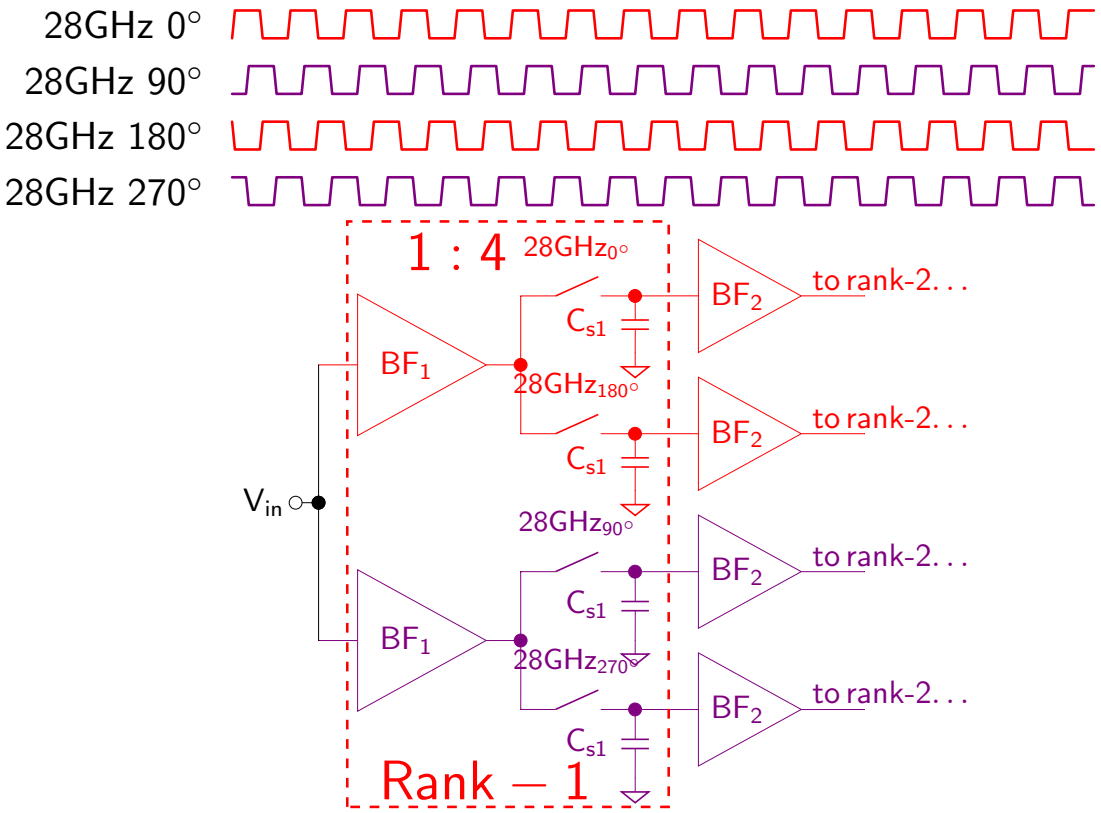


Figure 4.16: Modification of rank-1 to extend the design to 112GS/s

Power savings in the current hierarchical TH can be implemented. The power consumption of the OpAmps in the gain stage of rank-3 can be reduced by changing the direct (or Miller) compensation method. OpAmps using indirect feedback compensation technique have shown faster and low-power designs [54].

Figure 4.17 shows a new version for the OpAmp in rank-3. This topology uses split-length load devices in the first stage. The compensation capacitor C_C is connected to the internal low impedance node-A to achieve indirect compensation.

Pole splitting can be obtained with a lower value of C_C and g_{m6}. This results in a faster, more compact and lower power OpAmp when compared to the traditional Miller compensation.

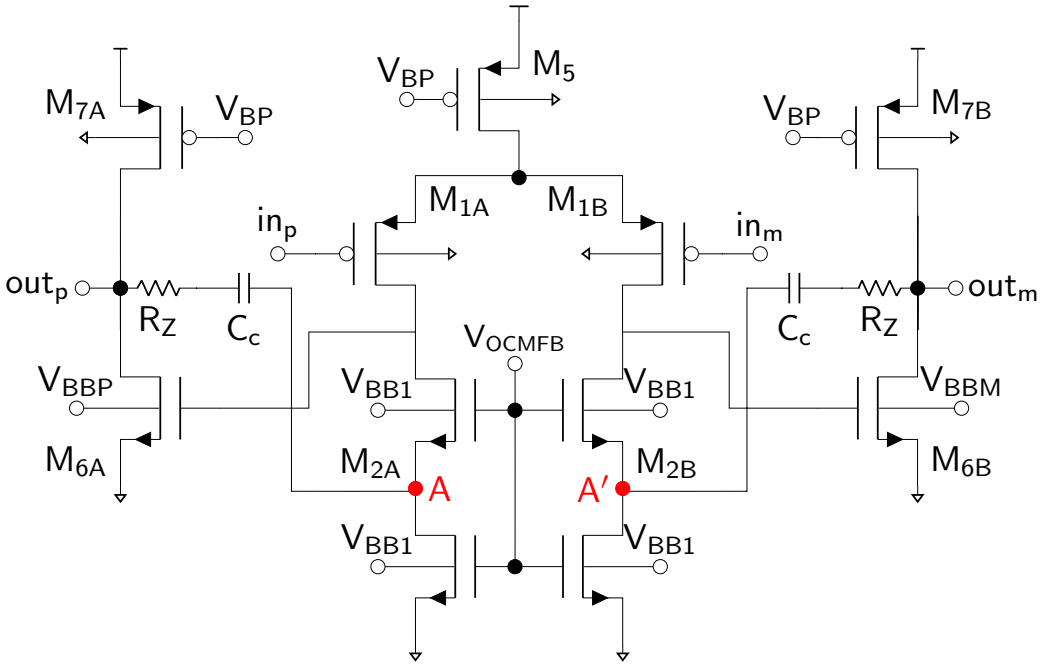


Figure 4.17: A two-stage OpAmp with indirect feedback compensation using split-length load devices.

A new version of this chip envisioned a complete redesign of the circuits in the AFE and hierarchical TH. Inverter-based circuits have shown potential for area reduction while maintaining low power. These circuits take full advantage of technology scaling. Inverters as analog transconductors have been studied in [55, 56]. Figure 4.18 shows different inverter-based circuits. Inverter-based active inductors can be used to replace the area-consuming passive inductors as well.

An inverter-based CTLE for PAM2 at 56Gb/s has been demonstrated in 16nm FinFET CMOS [57]. Recently, a 112Gb/s PAM4 LR wireline transceiver in 7nm FinFET CMOS has been published. It includes an inverter-based AFE in the receiver [26].

An inverter-based CTLE circuit is shown in Figure 4.19. It consists of a low and high gain paths and uses a feedforward coupling capacitor (C_z) to sum the currents from both paths. The DC and peaking gain are determined by the transconductance of the inverters and can be fully configurable. These circuit serves as an example for a new class of area and power efficient circuits in newer technology nodes.

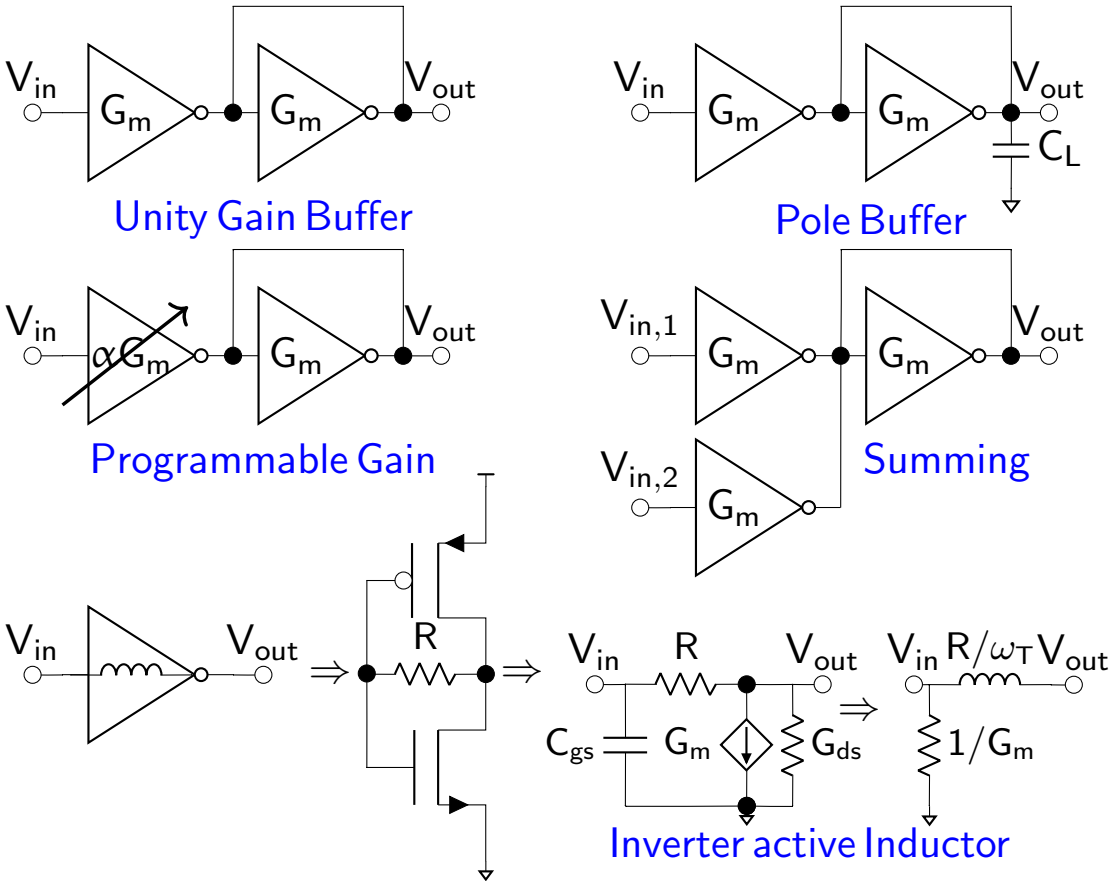


Figure 4.18: Inverter configurations for different analog blocks.

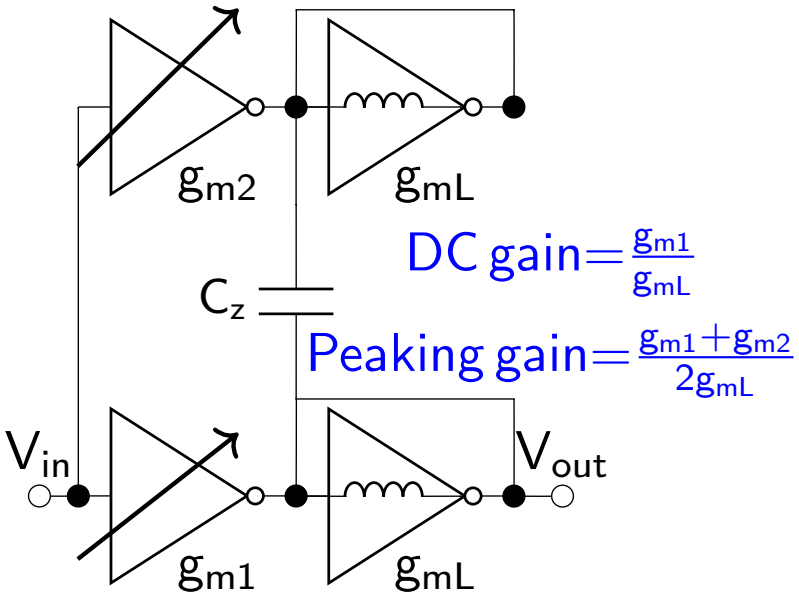


Figure 4.19: Inverter-based single ended CTLE schematic.

4.3 Conclusion

An ADC-based receiver prototype in 22nm CMOS FDSOI as proof-of-concept has been presented. The prototype includes several features such as:

- A CML-based CTLE as pre-equalizer in the AFE with peaking gain and frequency reconfiguration,
- A 56GS/s 7-bit SAR TI-ADC. It includes calibration for gain, offset and timing mismatches,
- A 64kbits SRAM to store 8192 samples (7-bit per sample),
- A digital controller unit for memory control and calibration using I^2C for off-chip interface.

Additionally, several enhancements for the current architecture have been proposed. These improvements aim to increase the total sampling frequency and reduce power consumption.

This prototype will allow us to verify our ADC-based receiver design for LR applications at 112Gb/s.

Conclusion

As mixed-signal architectures become more popular for the next-generation of high-speed serial links with >100Gb/s data rate and multi-level modulation, a specific design methodology is required. This methodology should define and validate the requirements and specifications for silicon-based wireline receivers that comply with >100Gb/s operation over transmission channels with high losses (>20dB).

A revision of the different aspects in wireline communications such as the 100 Gigabit Ethernet Standard, signal modulation, channel selection, equalization techniques and the state-of-the-art in Chapter 1 allow the definition of specifications for a PAM4 ADC-based receiver compatible with 100Gb/s operation.

Chapter 2 has presented the methodology to validate the proposed receiver's specifications using link system analysis. The transmitter, channel and receiver were modeled in MATLAB Simulink to complete the high-speed serial link. The receiver model includes an AFE, an ADC and a DSP unit for equalization. The link was tested using a PRQS sequence as a test pattern for PAM4. The BER was calculated from the output sequence of the receiver. It was demonstrated the feasibility of a PAM4 ADC-based receiver with 112Gb/s data rate and channel losses up to 30dB.

Chapter 3, the design of a 56GS/s TI-ADC in 22nm CMOS FDSOI for ADC-based wireline receivers is presented. A design flow was introduced to breakdown the key aspects of the design. The design procedure was divided in 3 parts: the hierarchical TH, the clock generation and the sub-ADC design.

The number of TH stages were chosen to minimize the number of low-jitter clocks. The circuit was designed following the transconductance efficiency (g_m/I_D) methodology using pre-computed lookup tables in MATLAB. The TH sampling clocks were designed from an external clock signal of 28GHz. A SAR ADC was chosen as sub-ADC unit for its speed and power efficiency. An improvement for the CDAC LSB capacitor implementation was described. A simple and accurate calibration methodology was introduced for the comparator and the ADC. A fast and accurate

simulink model for the TI-ADC was developed to validate the design and to speed up the simulation time. It is demonstrated a TI-ADC with 56GS/s data rate and ENOB above 5 bits using a conservative set of static, dynamic and mismatches parameters.

Chapter 4 is dedicated to the ADC-based receiver prototype in 22nm CMOS FDSOI technology. It includes a CML-based CTLE for pre-equalization, a 56GS/s 7-bit SAR TI-ADC, a 64kbits SRAM for sample storage, a digital controller for memory control and calibration using I^2C for off-chip interface. A procedure for chip characterization to evaluate the TI-ADC and BER performance is proposed. This prototype will allow the verification of the proposed ADC-based receiver at 112Gb/s.

Additionally, several enhancements for the current architecture have been proposed. These improvements aim to increase the total sampling frequency and reduce power consumption.

Publications

International Conferences

[C1] D. Cordova, W. Cops, Y. Deval, F. Rivet, H. Lapuyade, N. Nodenot and Y. Piccin, "Design Methodology for 112Gb/s PAM4 Wireline ADC-Based Receivers," in *Proc. IEEE Latin American Symposium on Circuits and Systems (LASCAS)*, Arequipa, Peru, February 2021.

[C2] D. Cordova, W. Cops, Y. Deval, F. Rivet, H. Lapuyade, N. Nodenot and Y. Piccin, "Optimized body-biasing calibration methodology for high-speed comparators in 22nm FDX," in *Proc. IEEE Latin American Symposium on Circuits and Systems (LASCAS)*, Arequipa, Peru, February 2021.

[C3] D. Cordova, W. Cops, Y. Deval, F. Rivet, H. Lapuyade, N. Nodenot and Y. Piccin, "A 0.8V 875 MS/s 7b low-power SAR ADC for ADC-Based Wireline Receivers in 22nm FDSOI," in *Proc. IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Salt Lake City, USA, October 2020.

[C4] D. Cordova, W. Cops, Y. Deval, F. Rivet, H. Lapuyade, N. Nodenot and Y. Piccin, "A Hierarchical Track and Hold Circuit for High Speed ADC-Based Receivers in 22nm FDSOI," in *Proc. IEEE International Conference on Circuits and Systems (ICECS)*, Genova, Italy, pp. 358–361, November 2019.

National Conferences

[N1] D. Cordova, Y. Deval, F. Rivet, H. Lapuyade, W. Cops, N. Nodenot and Y. Piccin, "Étude d'égalisation de canal pour liaisons numériques à 100 Gbps," in *21èmes Journées Nationales Microondes (JNM'19)*, Caen, France, May 14-17, 2019.

Appendices

Appendix A

PDK Extraction and Characterization

A Process Design Kit (PDK) was implemented using the 22FDX^{TM} platform in 22nm CMOS FDSOI of GLOBALFOUNDRIES, [50]. Which provides a second generation FD-SOI transistor, capable of providing lower power than 28nm and similar power efficiency to FinFET technology. One of the most differentiated features of the 22FDX platform is the capability of effective back gate biasing. Back gate biasing applies a positive or a negative voltage to the back gate of the transistor, which allows the transistor V_t to be tuned, and which can be done statically or dynamically.

A.1 PDK Extraction

The objective of the PDK extraction is to generate lookup tables containing all the relevant device parameters of the transistors used in our project. These "lookup tables" can then be used for systematic circuit design based on the transconductance efficiency (g_m/I_D) in MATLAB, as described in [58].

The lookup table are created through four-dimensional (L, VGS, VDS, and VBS) DC sweeps and noise analyses in Cadence Spectre. The obtained data is stored into MATLAB file (.mat). The sweeps are repeated for the available core transistors: the Super Low V_t (SLVT) NMOS and Extreme Low V_t (ELVT) PMOS. Table A.1 summarizes the device parameters for the 2 types of transistors.

In Figure A.1a depicts the g_m/I_D vs V_{GS} for the SLVT transistor. It shows the operation regions of the transistor for the nominal, slow and fast corners at -40°C, 27°C and 125°C. Figure A.1b shows the current density (I_D/W) used to size the transistor according to the circuit design requirements.

Table A.1: PDK Device Parameters

Transistor	SLVT	ELVT
Corner	Nominal, Slow and Fast	
Temperature (°C)	-40, 27 and 125	
Width per Finger (W_{nf})	[250 500 750]nm	
Fingers (nf)	[2:2:10]	
Channel length (L)	[0.02 0.06 0.1 0.15 0.2 0.5 1]µm	
Gate-to-Source Voltage (V_{GS})	[0:0.025:08]V	
Drain-to-Source Voltage (V_{DS})	[0:0.025:08]V	
Bulk-to-Source Voltage (V_{BS})	[0:0.025:08]V	

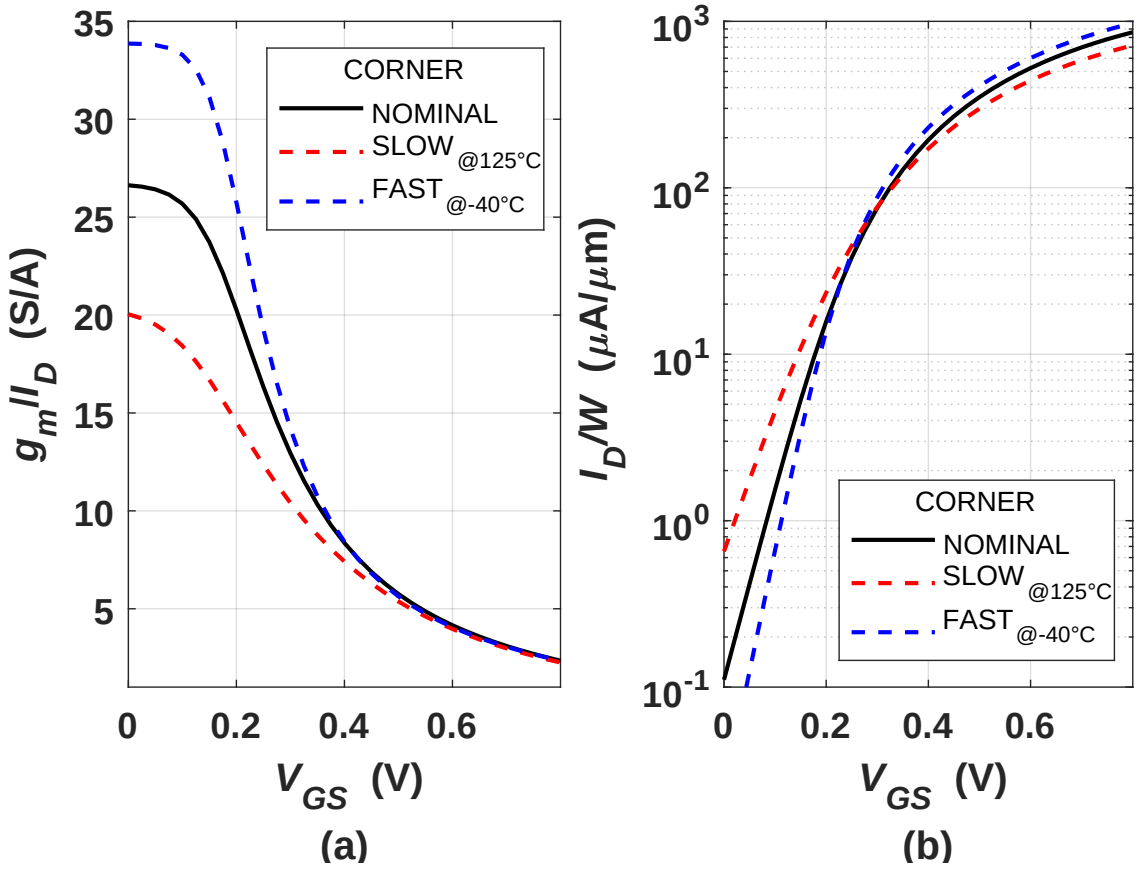


Figure A.1: (a) Transconductance efficiency and (b) Current density (I_D/W) for the SLVT transistor. $W_{total} = 10\mu m$, $L = 20nm$, $V_{DS} = 0.4V$ and $V_{BS} = 0.8V$

Usually, a FOM is established as a trade-off between thermal noise, Gain-Bandwidth product and supply current:

$$\frac{\text{Gain} \cdot \text{Bandwidth}}{\text{Input} - \text{Referred Noise Supply Current}} = \frac{\frac{f_T}{FO}}{4kT\gamma_n \frac{1}{g_m} \cdot I_D} \propto f_T \cdot \frac{g_m}{I_D} \tag{A.1}$$

where f_T is the unity gain frequency, the fan-out (FO) $=C_L/C_{gg}$, k is the Boltzmann, T is the absolute temperature in kelvins and γ_n is the thermal noise parameter.

Figure A.2 shows FOM vs g_m/I_D for different values of fan-out. The curves show an optimum bias point in the moderate inversion region between g_m/I_D= [10-12] S/A. The observed optimum can be used to minimize the power consumption in several circuits in our design.

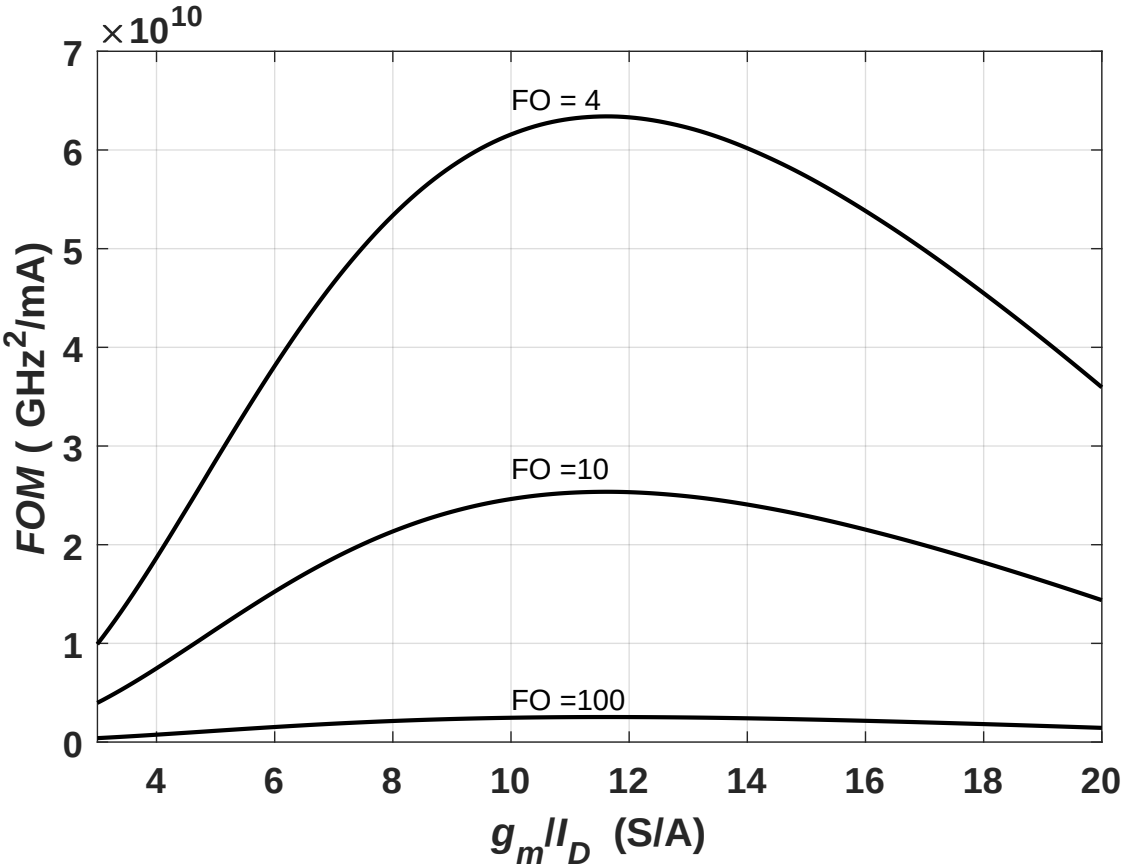


Figure A.2: FOM vs g_m/I_D for the SLVT transistor. W_{total} = 10µm, L = 20nm, V_{DS} = 0.4V and V_{BS} = 0.8V

A.2 Switch design

The design of the switches starts by characterizing a single NMOS SLVT transistor in the triode region (track mode). Figure A.3a presents the parametrization of the on-resistance r_{on}, total output capacitance c_{out} by the finger number (nf) and width per finger (W_{finger}). The unity gain frequency f_t and maximum oscillation frequency f_{max} are extracted to optimize W_{finger} for maximum bandwidth. Figure A.3b shows that a nominal value of 500 nm for W_{finger} is a trade-off between f_t and f_{max}.

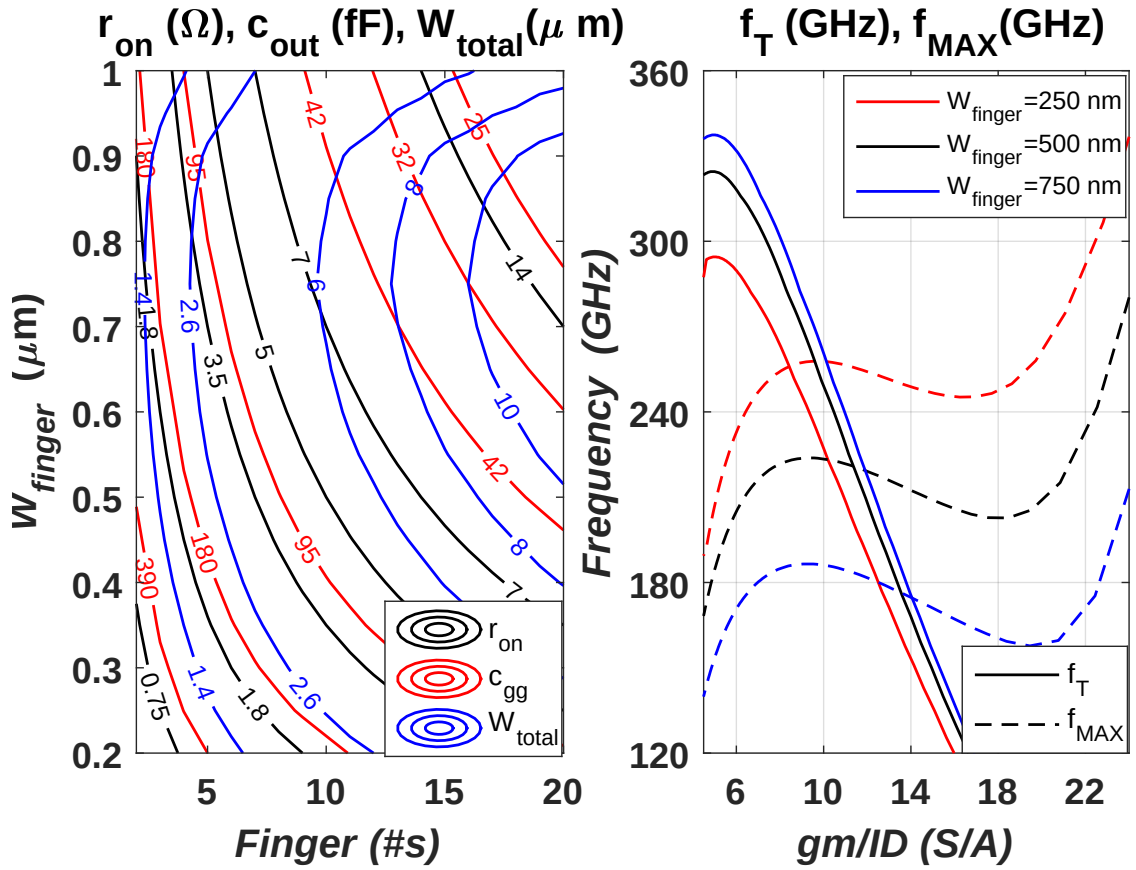


Figure A.3: r_{on}, c_{out}: L=20nm, V_S=V_D=0.35V, V_G=0.8V, V_B=1.8V. f_T, f_{MAX}: W_{total} = 1.5µm and V_{DS} = 0.4V

Cross-coupled switches are employed in the first 2 ranks of the hierarchical TH to minimize the effects of crosstalk. Figure A.4 depicts the design space for the bandwidth of a cross-coupled and simple switch sampling a C_s capacitor. A total transistor width (W_{total}) of 5µm with W_{finger}=500nm yields a bandwidth ≈ 56GHz.

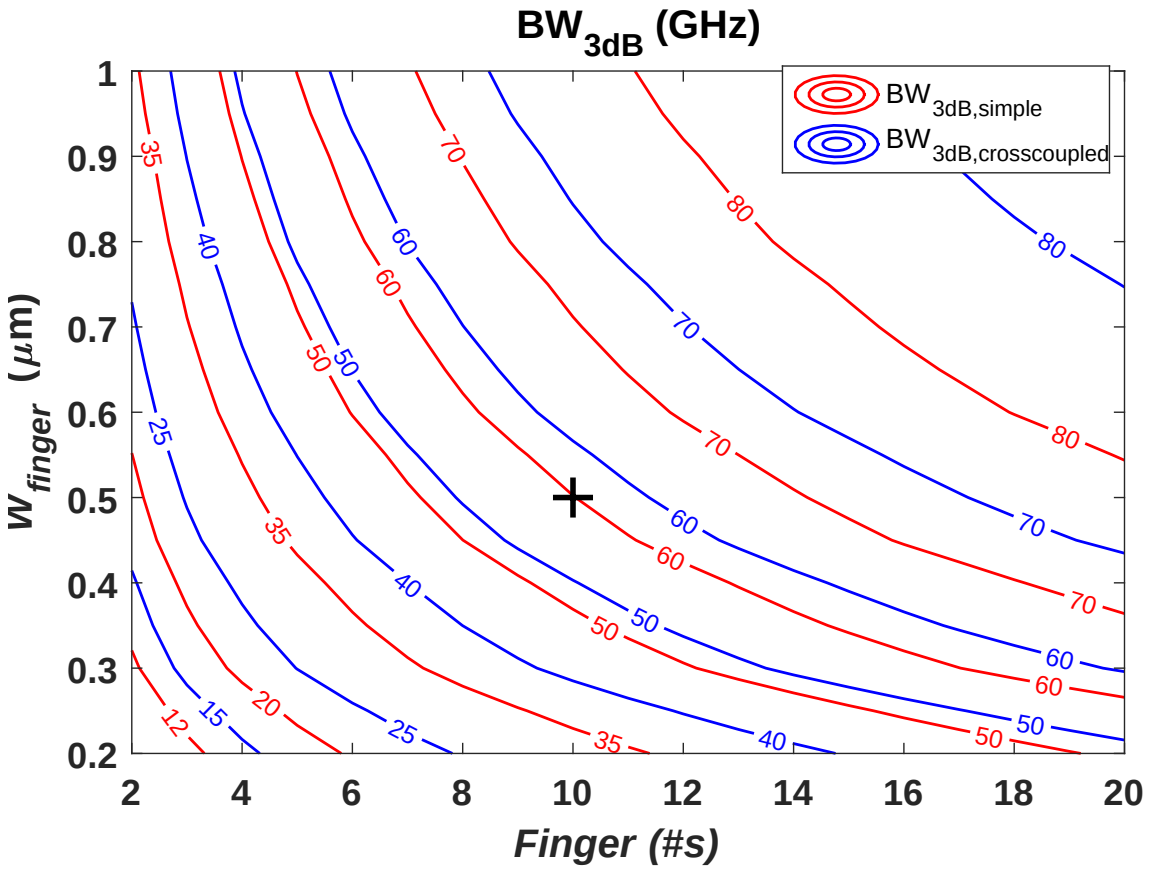


Figure A.4: 3 dB Bandwidth of a cross-coupled switch, L=20nm, V_S=V_D=0.35V, V_G=0.8V, V_B=1.8V and C_s=23fF

An optimization of the crosscoupled switch parameters (r_{on}, C_{in} and C_{out}) was performed to obtain the maximum achievable 3dB bandwidth ($BW_{3dB,opt}$) shown in subsection 3.3.2 for direct and demux sampling.

Figure A.5 presents the optimization for direct sampling for ISR=2 (N_1=2 and $N_{1,c}$=1)[1]. It shows BW_{3dB} vs the switch r_{on} yielding a $BW_{3dB,opt}$ of 46.47GHz for a r_{on}=35Ω.

The optimization for demux sampling is shown in Figure A.6. For the case condition of ISR=2 (N_1=1, $N_{1,c}$=1 and N_2=2)[2], a two-dimensional optimization is performed for the switches N_1 and N_2. It can be seen, that for a small r_{on} for N_1 and a moderate r_{on} for N_2 an optimum value of 25GHz is achieved.

[1] All N_1 switches with the same size
[2] All N_1 and N_2 switches with the same size

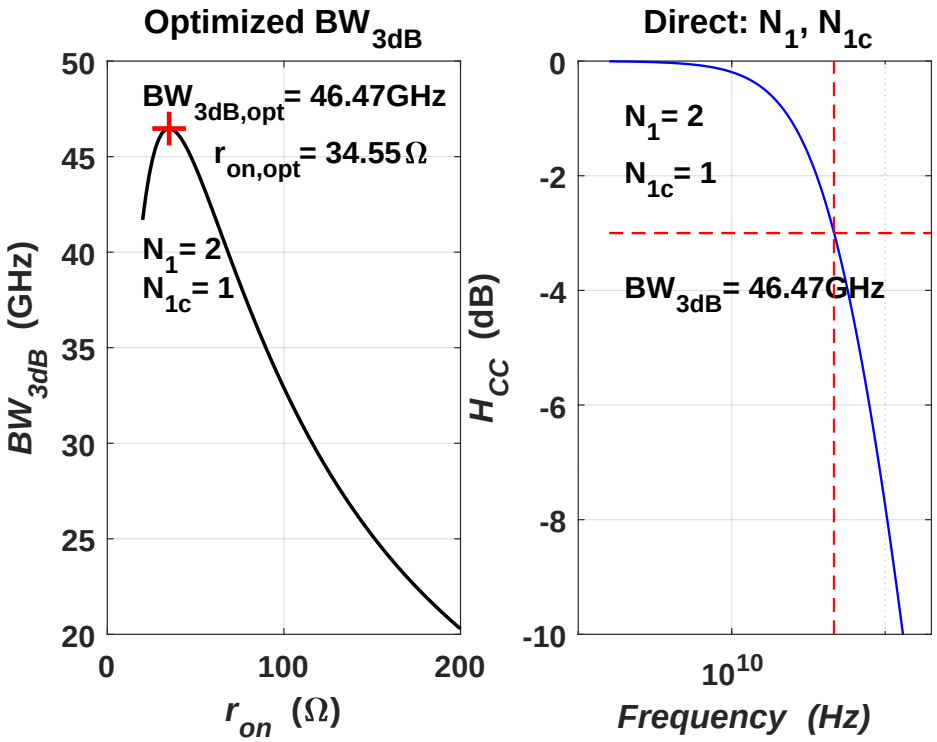


Figure A.5: Optimized 3dB Bandwidth for Direct sampling. N_1=2 and $N_{1,c}$=1

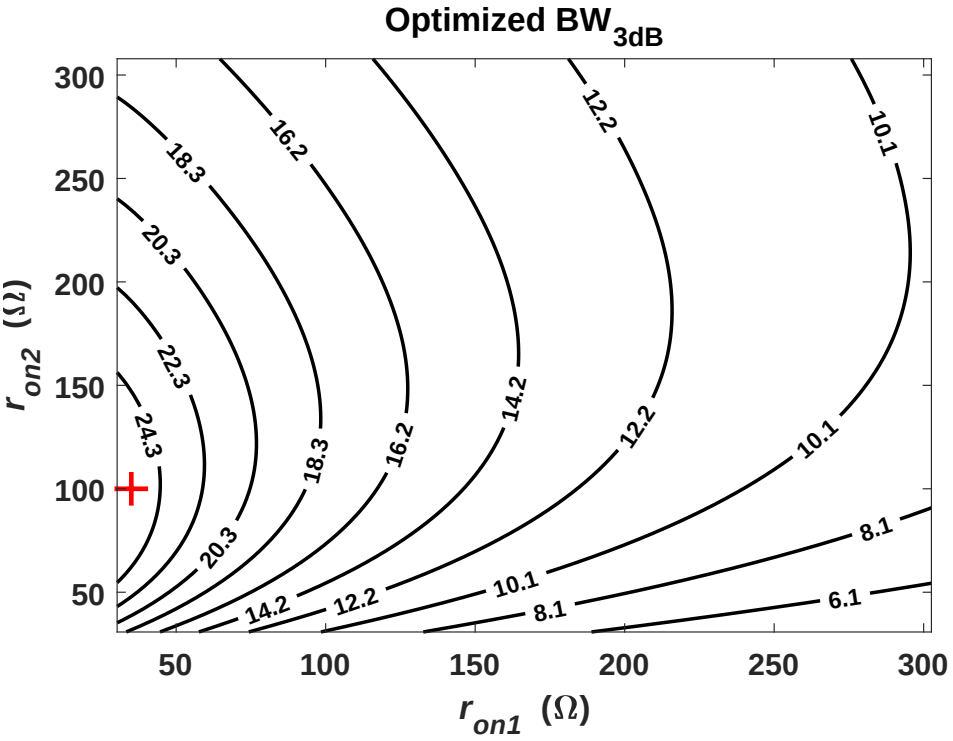


Figure A.6: Optimized 3dB Bandwidth for Demux sampling. N_1=1, $N_{1,c}$=1 and N_2=2

Appendix B

Back Gate Biasing Calibration Methodology

An optimized calibration methodology for high-speed comparators is presented. The key features of this methodology are the offset extraction technique and the back gate biasing calibration. The offset extraction technique uses a fast and accurate smart resettable successive approximation register (SR-SAR) algorithm to calculate the offset voltage (V_{OS}). The back gate biasing calibration is a simple iterative loop, where the back gate bias of the comparator's differential input pair is monotonically increased or decreased to counter balance the extracted offset voltage at each iteration.

B.1 Comparator Test Bench

The proposed back gate biasing calibration methodology is implemented using the test bench of Figure B.1. It consists of three blocks: the comparator, the back gate biasing DAC and the V_{OS} calibration control.

The control block is a Verilog-A model in charge of generating the inputs for the comparator and resistor ladder, reading out the comparator's output and adjusting the back gate biasing DAC accordingly to the calculated offset. The calibration operates in two phases: V_{OS} extraction and V_{OS} calibration. The extraction is a fast loop operating at the comparator's clock frequency Φ_{CLK} and follows the smart resettable SAR (SR-SAR) technique presented in [49]. Here, the voltage offset is calculated. The second phase is a slow loop (below 1 MHz), due to the low frequency nature of the transistor's back gate. After extracting the V_{OS}, the control block begins to change the comparator's back gate biasing until $V_{OS} \approx 0$ or a margin is reached.

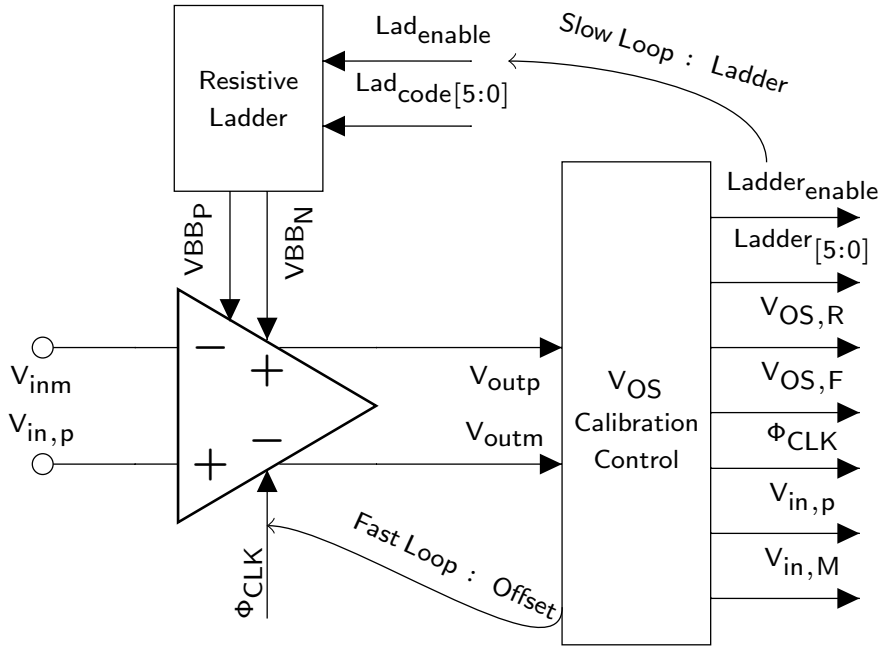


Figure B.1: Comparator testbench for back gate biasing calibration

B.1.1 Offset Extraction

The offset extraction technique SR-SAR in [49], is proposed as a fast and accurate alternative to the conventional linear search technique, which is simple and accurate but suffers from long simulation time. The SR-SAR uses a modified SAR algorithm to determine the comparator offset voltage in a much shorter time. The input of the comparator is modified to provide a quasi-monotonic stimulus. It allows a well defined crossing from low-to-high and high-to-low transitions. It yields to an accurate extraction of the rising offset (V_{OSR}) and falling offset (V_{OSF}) voltages.

Figure B.2 depicts the operation principle of the SR-SAR technique. Two search cycles (rising and falling) are performed, one cycle starting at the minimum level of the search range and the other at the maximum. In either cycle, the input goes to reset state if the next SAR value dictates a threshold crossing in a direction opposite to the one being tested. In this example, an ideal comparator with hysteresis was evaluated showing that V_{OSR} and V_{OSF} can be accurately extracted.

The number of cycles for the linear, SAR and SR-SAR techniques are given by

Table B.1. N_{BIT} is the number of bits employed in the binary search and $N_{CLK,SAR}$ is the number of clock cycles using only SAR.

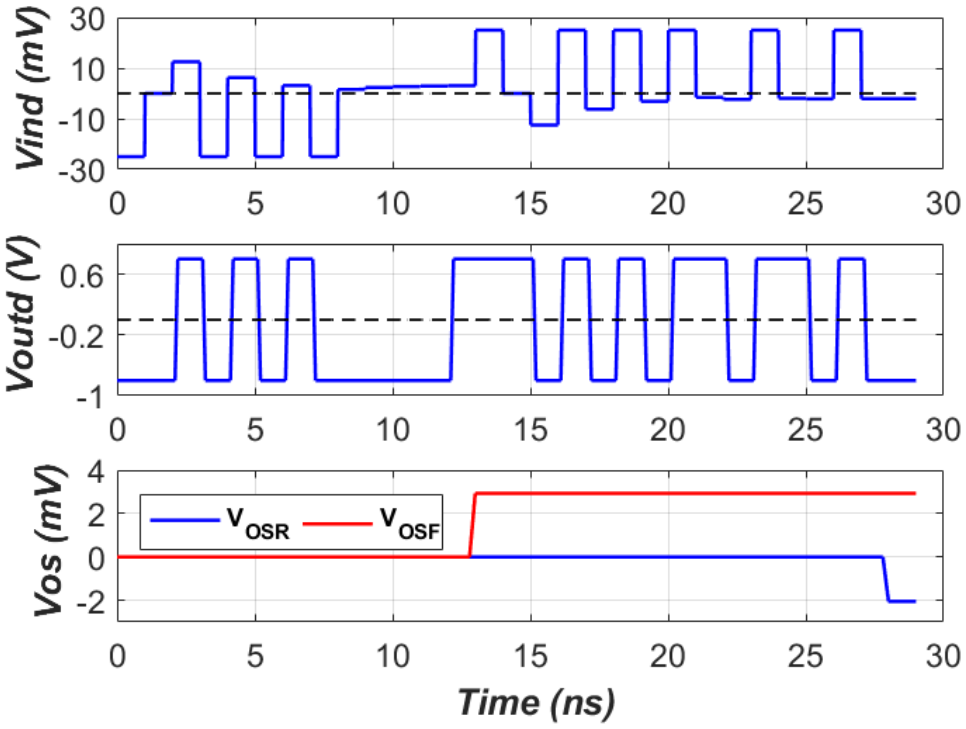


Figure B.2: Offset voltage extraction technique showing: input differential voltage (V_{ind}), output differential voltage (V_{outd}) and offset voltage (V_{OS})

Table B.1: Calibration Clock Cycles

Linear	SAR	SR-SAR
$\frac{\text{Search Range}}{\text{Search Resolution}} \cdot 2$	$2(N_{BIT}+1)$	$N_{CLK,SAR} + (N_{BIT}\text{ -1})$ $3N_{BIT}+1$

B.1.2 Comparator

The evaluated comparator is the one described in subsection 3.5.4. The offset introduced by the input differential pair will be compensated using our proposed calibration technique. Offset voltage suppression is achieved by adjusting V_{TH} in the differential pair through forward back gate biasing, which is allowed in FDSOI technology.

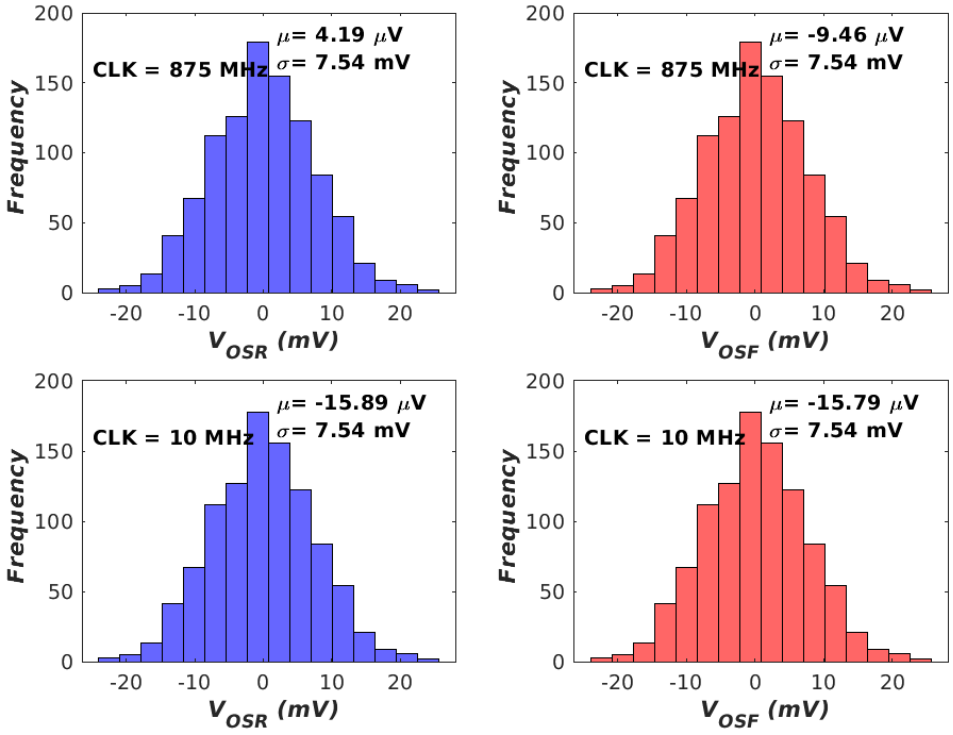


Figure B.3: Histogram Strong ARM V_{OSR} (blue) and V_{OSF} (red): CLK=875MHz and CLK=10MHz for 1000 uncalibrated MC runs

B.1.3 Back gate biasing DAC

The back gate biasing DAC consists of a resistor ladder controlled by a 5-bit digital word. In order to choose the variation range of the ladder, we need to extract the V_{OS} range of the comparator. Using Monte-Carlo (MC) simulations from the schematic, a V_{OS} range (+/-3σ) of ≈ 45mV was obtained for the nominal clock frequency of 875MHz. Additionally, the V_{OS} was extracted for a low frequency of 10MHz, as seen in Figure B.3. The reason behind it, is to reduce even further the simulation time during calibration. As can be seen, there is little contribution due to memory effect at 875MHz, allowing us to clock the comparator at a lower frequency without loosing too much accuracy. Table B.2 summarizes the MC results. A search range of +/-50mV with a resolution of 0.1mV was used.

The nominal voltage supply for the comparator is 0.8V, the same for the back gate bias at nominal operation. Figure B.4 shows the back gate bias control. The ladder

Table B.2: Schematic V_{OS} Extraction

Search range	-50 to 50mV	
Resolution	0.1mV (10 bits)	
Φ_{CLK}	875MHz	10MHz
Mean ($V_{OS,R}$)	4.19μV	-15.89μV
σ ($V_{OS,R}$)	7.542mV	7.543mV
Mean ($V_{OS,F}$)	-9.46μV	-15.79μV
σ ($V_{OS,F}$)	7.544mV	7.543mV

was designed using a resolution of 5 bits, with the back gate voltage varying between 0.4V to 0.8V. An artificial offset voltage range of +/- 32mV (≈ 2.1mV steps) was created. For example, if a negative V_{OS} is extracted, the calibration controller will only choose from the positive range to counterbalance the negative V_{OS} generated by the differential pair.

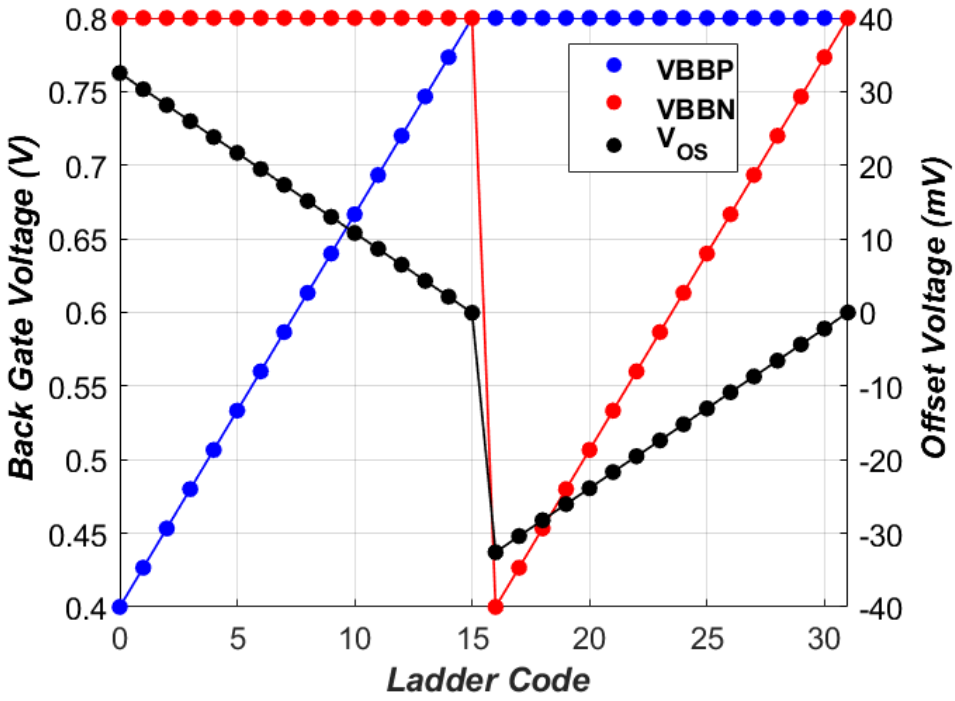


Figure B.4: Back gate biasing DAC: back gate bias and offset voltage

B.1.4 Offset Calibration

V_{OS} calibration for the comparator consists in two phases:

1. V_{OS} extraction:
   - It begins with initialization of the back gate biased DAC, ladder code=15 → V_{BBP}=V_{BBN}=0.8V,
   - After initialization V_{OSR} and V_{OSF} are extracted.
2. V_{OS} calibration:
   - V_{OSR} and V_{OSF} determine the iteration sequence for the ladder with $V_{OS,init}$=V_{OSR}=V_{OSF},
   - For $V_{OS,init}$<0, the ladder adds a positive $V_{OS,iter}$[code]>0, with the code starting at 0. For $V_{OS,init}$>0, the code starts at 16 ($V_{OS,iter}$[code]<0),
   - The back gate bias are switched to the current code value: V_{BBP}[code], V_{BBN}[code] and $V_{OS,iter}$[code] is extracted,
   - The iteration sequence continues until $V_{OS,iter}$[code]<tolerance, i.e. 1mV or the code reachs its final value.

Figure B.5 shows the time diagram of the comparator's V_{OS} calibration sequence for $V_{OS,init}$<0. The code transitions has a time step of 2.5μs and the comparator is clocked at 10MHz (T=100ns). By clocking the comparator at low frequency, the time step of the transient simulation is coarse enough to allow a much faster convergence solution.

B.2 Simulation Results

The stair-case input signal to detect the comparator's output transitions is the standard technique for comparator offset simulation. The drawback of this technique is the fine voltage step to achieve adequate precision. This simulation requires a very long simulation time for a single V_{OS} extraction and must be repeated enough times

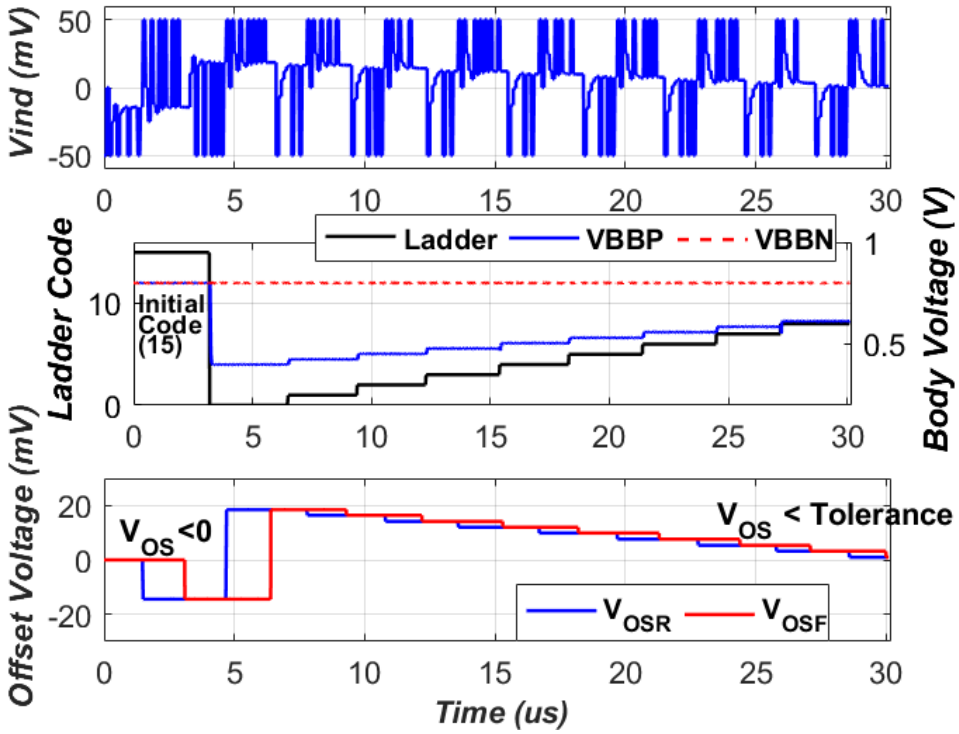


Figure B.5: Back gate biasing calibration procedure showing: input differential voltage (V_{ind}), DAC ladder code, DAC back gate voltage and offset voltage (V_{OS})

to calculate the statistical distribution of V_{OS}. Thus, the total simulation time can take several hours or more.

To evaluate the proposed calibration methodology, MC Post-Layout Simulations (PLS) were performed on the comparator using the same search range and resolution for V_{OS} extraction. Table B.3 shows results of V_{OS} for 100 MC runs for an uncalibrated and calibrated comparator. It clearly stands out the V_{OS} mean and standard deviation reduction for the calibrated comparator. The V_{OS} mean was almost zeroed and the standard deviation was reduced by a factor of 12. Another aspect to point out is the larger V_{OS} of the uncalibrated version, but this did not present any issues since the resistor ladder was designed with some margin.

The other important aspect of this methodology is the simulation time reduction. Table B.4 presents the simulation time for the V_{OS} extraction and calibration for the schematic and post-layout views of the comparator. The time saving in the design process can be seen. For a first design version (schematic) of the comparator, it can

Table B.3: Post-Layout V_{OS} Calibration.

Search range	-50 to 50mV	
Resolution	0.1mV (10 bits)	
Φ_{CLK}	10MHz	
	Uncalibrated	Calibrated
Mean (V_{OS})	-1.61mV	0.02mV
σ (V_{OS})	8.86mV	0.73mV

only take up to 40 minutes to estimate and calibrate the V_{OS} and almost 4 hours to validate the complete design with PLS results. The simulation time was reduced by a factor of 64 compared to the linear calibration technique.

Table B.4: Simulation Time Summary

V_{OS} Extraction (1000 MC runs)		V_{OS} Calibration (100 MC runs)	
Schematic	Post-Layout	Schematic	Post-Layout
24min	1h50min	16min	1h56min

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