Study and development of resistive memories for flexible electronic applications

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Abstract

The advent of flexible electronics has brought about rapid research towards sensors, bio implantable and wearable devices for assessment of diseases such as epilepsy, Parkinson's and heart attacks. Memory devices are major component in any electronic circuits, only secondary to transistors; therefore many research efforts are devoted to the development of flexible memory devices. Conductive Bridge Random Access Memories (CBRAMs) based on creation/dissolution of a metallic filament within a solid electrolyte are of great research interest because of their simple Metal Insulator Metal architecture, low-voltage capabilities, and compatibility with flexible substrates.

In this work, instead of a conventional metallic oxide or a chalcogenide layer, a biocompatible polymer - Polyethylene Oxide (PEO) – is employed as the solid electrolyte layer using water as solvent. Memory devices, consisting in Ag/PEO/Pt tri-layer stacks, were fabricated on both silicon and flexible substrates using a heterogeneous process combining physical vapour deposition and spin coating. To aim this, a systematic study on the effect of solution concentration and deposition speed on the PEO thickness is presented. SEM/EDX and AFM measurements were then conducted on devoted "nano-gap" planar structures and have revealed the formation of metallic Ag precipitates together with morphological changes of the polymer layer after resistance switching. The performance of the resistive memory devices is then assessed on silicon and flexible substrates. In particular programming voltage statistics, OFF/ON resistance ratio, endurance cycles and retention tests are performed and the effect of current compliance is analysed. The conduction mechanism in the HRS/LRS is studied on the Ag/PEO/Pt and Pt/PEO/Pt reference devices. Finally, the electrical characterization of devices on flexible substrate is performed under mechanical stress, showing promising results. Polymer-based CBRAM devices are therefore suggested as potential candidates for sustainable development of flexible memory devices.

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General Introduction

Internet of things (IoTs) with its applications in the field of health, production, security and transport is changing the dynamics of security systems, usage and control around the world. In this respect flexible electronics is expected to play a major role as it possess the advantages of using large areas and curved substrates, downscaling the resolution of fabrication of the devices, easing processability and lowering production costs. Gradually, with technological advancements many commercial products such as sensors, light emitting diodes and wearables are being part of our daily routine. Besides logic transistors, memory devices are important component of any electronic circuit. The fact that volatile memory devices categorized as SRAMs or DRAMs lose data when switching off power supplies brings non-volatile memory devices into the spotlight. Among them, Flash memories have a significant share in the market due to their high density, stability in performance and low cost. However, the disadvantages of high write voltages (>10V), low operation speed (in milli seconds), limited endurance cycles 10^3-10^5 and large leakage currents make us look beyond them.

Among the emerging non-volatile memories, Conductive Bridge Random Access Memory devices (CBRAMs) are gaining attention due to their simple architecture – Metal-Insulator-Metal (MIM), ease of process ability and scalability. Research on CBRAMs have shown exceptional properties of fast response time, possibility of multilevel data storage by modulating the compliance current, high density, low power consumption and high performance.

In this research work, we develop and study the performance of CBRAMs based on solid polymer electrolyte layer, Polyethylene oxide (PEO). After the validation of the fabrication process, the workability of the devices are reported through current-voltage characteristics in order to evaluate their retention time, endurance cycles and so on. As these devices are based on switching mechanism between ON and OFF states through a conductive filament. Planar devices with nano-gaps are fabricated to observe the filament growth. Through optical microscope, AFM, SEM and EDX measurements such

morphological changes are observed. Further, conduction mechanism studies are carried out to understand the factors influencing the charge transport in such thin films.

Finally moving towards our goal, as the use of polymer layer facilitates deposition on flexible substrates. Hence, the devices are fabricated on kapton- 125 µm. Fatigue tests are performed on the devices to study their resilience to stress. Hence, this work aims at sustainable development of CBRAMs for flexible electronic application.

Chapter 1- Non-Volatile memories for flexible electronics applications

This chapter introduces flexible electronics, which is the main context of this work. After presenting the main advantages of flexible electronics to support the deployment of the so-called "Internet of Things" infrastructure, we will expose the different technological approaches supporting its development together with current market and opportunities for growth.

We will then focus on non-volatile memories, showing how these devices can contribute to the development of smart autonomous objects. Among the large family of Non-volatile memories, emerging memories based on resistance switching are considered today as potential candidates to replace traditional Flash memories based on charge-storage. Among them, Resistive Random Access Memories (RRAM) and Conductive-Bridge Random Access Memories (CBRAM) are very promising due to their overall performances and ease of fabrication. In particular, it is shown that such kind of memories can be engineered using polymer films, which make them very appealing for flexible electronics applications.

Finally, we conclude on this chapter through a presentation of the main objectives of the PhD work.

1. Overview of flexible electronics

1.1. Why do we need flexible electronics for?

Since the 70s', the global electronics market is taking advantage from the constant progress achieved in the semiconductor industry, ruled itself by the so-called "Moore's Law" **[1]**. While moving from one technology node to the next one, downscaling the integrated devices can be leveraged through a decrease of fabrication costs (*i.e.* reduction of the circuit area) while keeping the same amount of functionalities, by increasing the computing energy efficiency while keeping the fabrication costs, or by enabling new functionalities through the integration of novel devices **[2]**. This virtuous dynamic

combining lower production costs, increased integration density, performances and functionalities has led to a growth of the electronics market through successive “waves” from analogue (1970-1980), digital (to from 1990), internet (end of the 90s) and mobile electronics (2000s).

Today, the electronic market is riding on the so-called “Internet of Things” (IoT) wave. In its broad sense, IoT designates software and hardware infrastructure making possible to connect, through the Internet, humans to any "object" lying in their physical environment. Today, it is estimated that more than 20 billions of object are connected through the IoT infrastructure (more than twice the worldwide population) and that this number is about to triple by 2025 **[3]**.

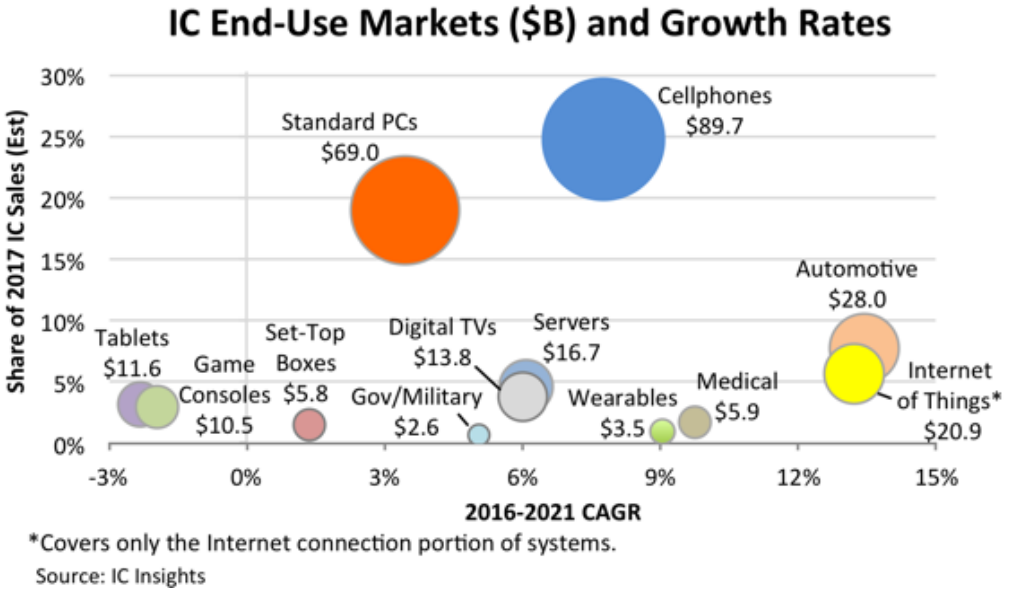


Figure 1. 1 Forecast of market share and growth rates for different sectors covered by integrated circuits between 2016 and 2021. Source : IC Insights [4]

As shown in **Figure 1. 1**, it is forecasted that IoT and automotive applications will feature the highest growth-rate until 2021 **[4]**.

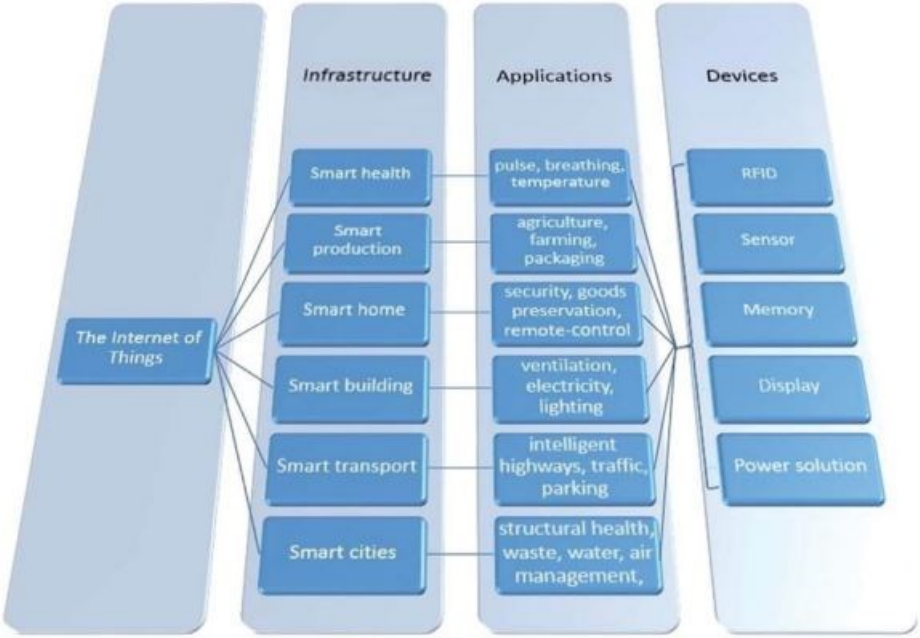


*Figure 1. 2 Illustration of the IoT infrastructure linking applications and the elementary electronic devices required for their deployment. Adapted from **[5]***

Figure 1. 2 illustrates the numerous applications that can be covered by IoT; it is shown that all current major social challenges such as health, energy, food or transport can take advantage of IoT. In addition, it is apparent that the deployment of IoT sensor nodes rely on elementary electronic devices functionalities such as data acquisition (sensor), processing (logic), **storing (memory)**, transmission (RFID) associated with power solutions **[5]**.

Even though such elementary functionalities are already available in CMOS (Complementary Metal Oxide Semiconductor) technologies, silicon-technology suffers from severe limitations regarding integration within a wide variety of "objects" of our daily life having arbitrary areas and shapes **[6]**.

Figure 1. 3 Teardown of an Apple Watch © Serie 5 showing the complex packaging of Printed Circuit Boards, electronic modules and battery interconnected through flexible connectors. Source: iFixit.com

Indeed, as illustrated in **Figure 1. 3**, most of the modern electronic systems still rely on rigid substrates (*i.e.* PCB - Printed Circuit Board) holding Integrated Circuits (ICs). This approach, suffers from limitations regarding its integration into objects featuring **large areas** and **arbitrary form factors**. Even though technological options exists to thin silicon IC and transfer them onto flexible substrates **[7]**, CMOS technologies are not naturally adapted to be integrated onto non-planar surfaces. In addition, their **fabrication cost** still remain prohibitive regarding the development of large area electronics (>10cm^2) **[8]**.

Given these limitations, **flexible electronics** can be a key-enabling technology to extend the integration of electronic functions into a wide range of objects for IoT applications together with lowering their fabrication costs. Indeed, flexible electronics can employ various affordable deposition techniques, such as inkjet printing or screen printing and does not necessarily require heavy and costly techniques such as photolithography to achieve electronic functions. In addition the use of flexible substrates such as polymer films, which are commercially available in the form of large rolls, techniques like « roll-to-roll » processing can be leveraged to elaborate electronic circuits over large areas **[9]**. Besides plastics, many other kind of substrates such as textiles**[10]** or even human skin **[11]** where demonstrated to be capable to host electronic functions strengthening therefore the interest for flexible electronics market for IoT.

1.2. Technological approaches and markets

According to the ***FLextech Alliance***[1] (international consortium of research and industrial laboratories established since 1993) *flexible electronics* covers a wide variety of fabrication techniques schematized in **Figure 1. 4** :

- **Printed Electronics** [**Figure 1. 4(a)**] functional electronics fabricated by laying conductive lines using one of several printing methods, including: screen, ink-jet, gravure, flexography and others. Often confused with printed circuit boards, which also use printing methods to connect discrete active and passive components. **Plastic Electronics** [**Figure 1. 4(b)**] refers to the fabrication of circuit or electronic functions onto plastic (i.*e.* polymer) substrates using processes not restricted to printed electronics. Vacuum deposition methods or photolithography can be then deployed on plastic substrates.
- **Flexible Electronics** [**Figure 1. 4(c)**] refers to a class of electronic devices built on conformable or stretchable substrates, usually plastic, but also metal foil, paper or glass.
- **Organic Electronics** [**Figure 1. 4(d)**] concerns the fabrication of electronic functions or devices (*i.e.* transistors, sensors, memory,…) employing organic compound or polymer films[i].
- **Flexible Hybrid Electronics (FHE)** [**Figure 1. 4(e)**] can be viewed as a synthesis of the aforementioned technologies, which can also combine silicon (CMOS) electronics. In it broad sense, FHE can be viewed as an heterogeneous integration technique taking advantage of flexible electronics for processing functionalities onto large area or arbitrary shaped substrates without sacrificing performances through the integration of silicon ICs.

[1] https://www.semi.org/en/collaborate/flextech-infohub/whatareflexibleelectronics

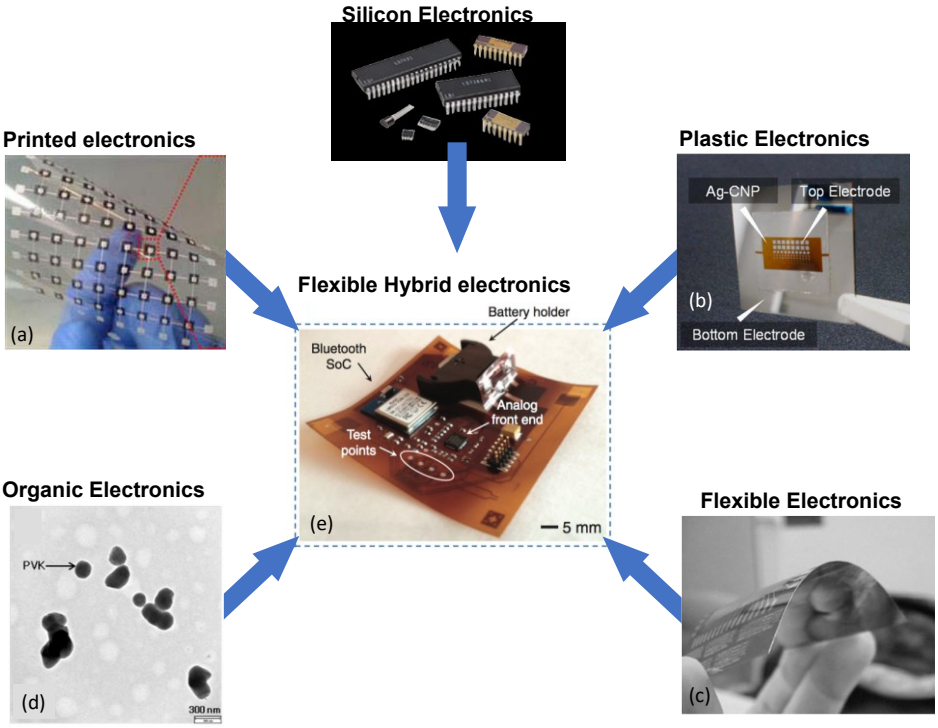
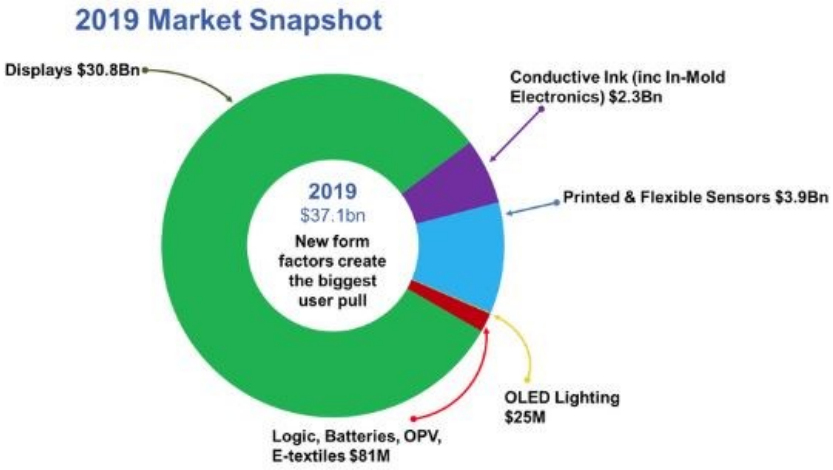


Figure 1. 4 Illustration of the various technological approaches embraced by flexible electronics in its broad sense.

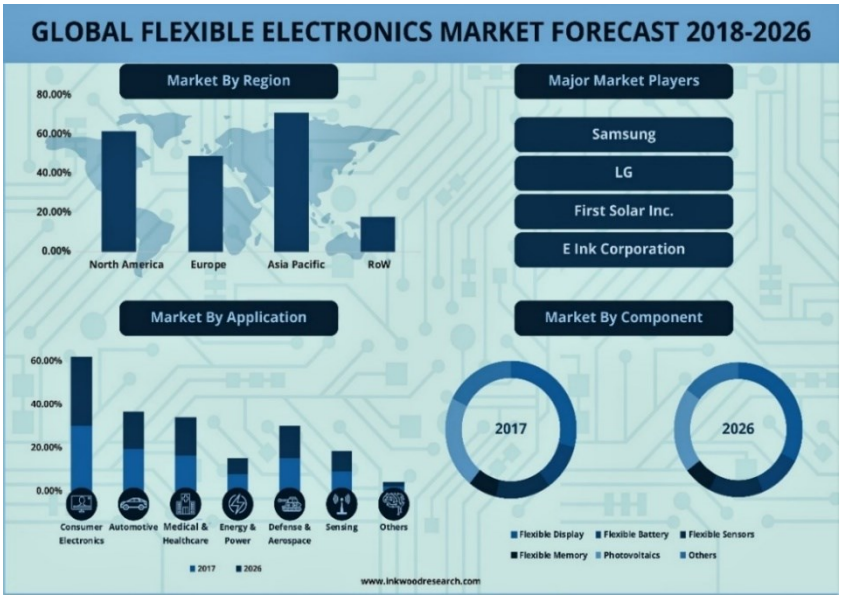
(a) **Printed Electronics**: Example of a pressure sensor fabricated printed on a flexible substrate **[12]**. (b) **Plastic Electronics** : Non-volatile Memories fabricated on kapton substrates where electrodes where achieved by photolithography **[13]**. (c) **Flexible Electronics** : TFT (Thin Film Transistors) fabricated on a flexible steel sheet **[14]**. (d) **Organic Electronics** : PVK (Poly-Vinyl Carbazole) matrix deposited on a flexible substrate containing CdSe/ZnS core-shell nanoparticles for non-volatile memories **[15]**. (e) The combination of these various techniques can be associated to the integration of silicon ICs to achieve a **Flexible Hybrid Electronics:** here an electronically designed Bluetooth enabled flexible "Smart Inhaler" **[16]**.

Figure 1. 5 shows the main market sectors of printed, flexible and organic electronics as reported by IDTechEx[2] for year 2019. This $30 billion global market is forecasted to grow to $41.2 billion in 2020 and up to $74 billion in 2030[2].

[2] https://www.idtechex.com/en/research-report/flexible-printed-and-organic-electronics-2020-2030-forecasts-technologies-markets/687



(a)



(b)

Figure 1. 5(a) Current markets of printed, flexible and organic electronics as by IDttechEx Research group. (b) Forecast by Inkwood Research of the global flexible electronics market including applications and components from 2017-2026.

Sources *: IDTechEx* ***[17]***

Inkwood Research

Regarding the main functionalities embraced by this market, it can be seen that its major components are a) **flexible displays** - such as OLEDs - Organic Light Emitting Devices devoted to the TV, mobile phone or tablets. (b) **conductive inks** - used in a wide range of applications such as In Mold Electronics **[18][19]** ; e-textiles **[9]**, RFID **[5]**,…) and (c) **printed and flexible sensors [20]**. As flexible electronics are gaining maturity, new market trends such as **wearable electronics** [**Figure 1. 6**] or **smart-packaging** applications [**Figure 1. 7**] are soon expected to be strong market sectors of flexible electronics.

Figure 1. 6 Shows an electronic skin patch - an integration of flexible and printed electronics with conventional electronics to create a wearable patch. Holst Centre predicts healthcare trends and opportunities growing doubling from 2019 to 2024[3].

Figure 1. 7 Shows a ready-to-eat meal box smart-packaging by PragmatIC[3].

2. Overview of Non-volatile Memories technologies

This section provides an overview on the main technologies of non-volatile memories. Starting from the mainstream Flash technology and their integration limits, the emerging non-volatile memories are introduced together with their physical principle. Although most of the technologies discussed here are based on semiconductor devices, this section is intended to serve as introduction of the flexible non-volatile memory technologies presented in the next section.

2.1. Volatile and Non-Volatile Memory in the semiconductor industry

Memory technologies can be broadly divided into two categories: Volatile and Non-Volatile memory (*i.e.* NVM). In volatile memory, data is instantaneously lost as soon as the power is shut down. In return, these devices are well suited for quick computation and programming given their low access time (i.e. < 10 ns). The Static (SRAMs) and Dynamic (DRAMs) are the main representatives of volatile memory. Both are respectively used as cache and main memory in computing system, the SRAM being co-integrated with the CPU while DRAM is accessed externally from dedicated modules**[21]**.

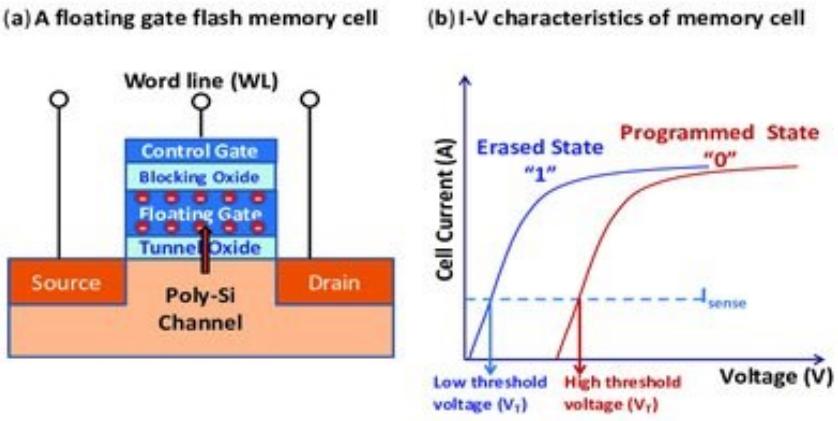


*Figure 1. 8 (a) Schematic view of a Flash memory cell and (b) its I_D (V_G) characteristics. The programming principle relies on the injection of charge to/from the floating gate from/to the silicon channel by tunneling effect. From **[22]***

Currently, Flash memory is the mainstream technology in the field on non-volatile memory. The reason for such an industrial success is the continuous downscaling of the Flash memory cell since its introduction on the market by Toshiba in the late 1980s **[23]**.

The main principle of Flash memory is depicted in **Figure 1. 8** : the cell consist of a transistor featuring an additional floating gate insulated from the silicon channel by a thin (~5-7 nm) tunnel oxide. Memory effect is achieved by charge injection from the silicon channel to the floating-gate resulting in a threshold voltage shift of the Flash memory transistor [**Figure 1. 8**].

There are two main kinds of Flash memories, depending on the cell arrangement in the memory array: NAND and NOR types. The NOR ones are used as embedded memory in microcontrollers **[21]**, while the NAND ones, due to a denser implementation are primarily found in standalone NVM modules for USB flash drives, Solid State Drives (SSD) and mobile devices (*e.g.*: smartphones and tablets). Due to its larger integration density and given the high demand for NAND Flash memory for mobile applications and SSD applications over the last decade, NAND Flash has been aggressively downscaled down to the 10 nm node as early as in 2011**[24]**.

Although Flash memory is a very attractive and mature technology, it possesses intrinsic limitations such as *single electron effects* **[25]**, *parasitic electrostatic coupling between adjacent cells* **[26]** or *Stress Induced Leakage Current* (SILC) which makes the tunnel oxide hardly scalable beyond 5 nm **[27]** which in turn results in a limited voltage scalability for both standalone and embedded applications. For these reasons Flash scaling is highly compromised beyond the 28 nm node for NOR applications and 10 nm for standalone NAND **[28]**.

2.2. Emerging Non-Volatile Memories

The scaling limits of Flash memory has stimulated intense R&D efforts in order to design *emerging non-volatile memories* over the last decades **[29][26][27]**. Given the fact that *no universal memory exists*, that would combine integration density and non-volatility of Flash together with programming speed of SRAM, a wide variety of emerging memories are still under development as schematized in **Figure 1. 9 [31]**. It can be seen that most of the alternative technologies for Flash memory exploit *resistance switching* as main physical principle instead of *charge-storage*.

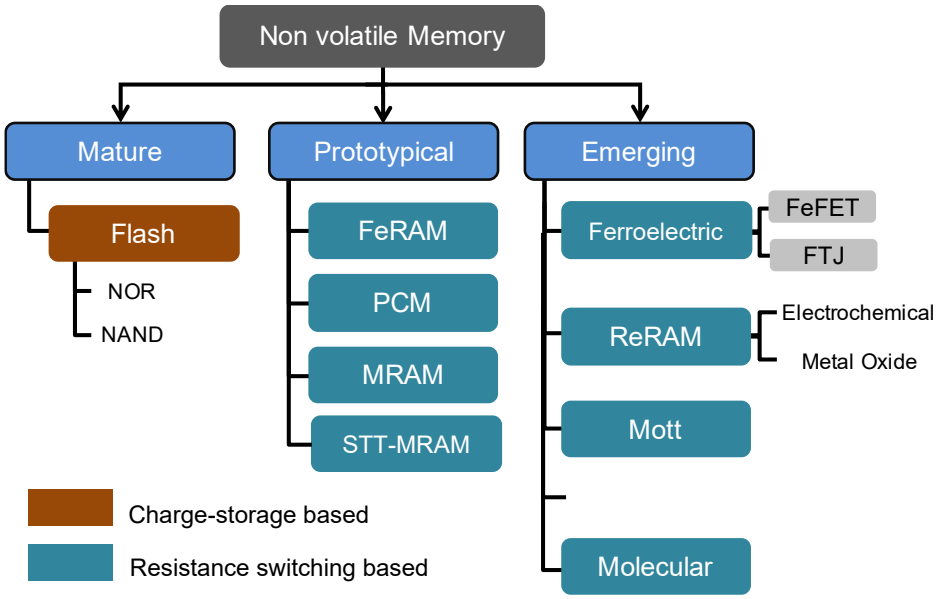


Figure 1. 9 Overview of emerging non-volatile memories sorted along their technological maturity.
*Source : ITRS 2.0 – Emerging Research Devices **[31]** (adapted)*

Given most of the flexible memories take their inspiration from the developments undertaken on semiconductor technologies **[32]**, in the following we will briefly describe the main concepts behind the main alternative technologies to Flash memory explored on flexible substrates.

2.2.a.Charge-trap Memory

During each erase/write cycle, the electrical stress degrades the tunnel oxide, generating traps within the bandgap of the tunnel oxide. This phenomenon is known as SILC (Stress Induced Leakage Current) and results in a progressive degradation of the Flash memory retention capabilities over cycling **[27]**. In order to ensure immunity to SILC, the tunnel oxide of Flash memory cannot be downscaled beyond 5-7 nm in order to ensure the 10 years data-retention criterion, resulting in a limited programming voltages scalability. In order to cope with SILC, the replacement of the continuous polysilicon floating gate by a *discrete charge-trap* layer (such as a nitride Si_3N_4 layer) was suggested in order to increase

localization of the stored charge and avoid a complete discharge of the memory cell as defects are generated within the tunnel oxide [**Figure 1. 10**].

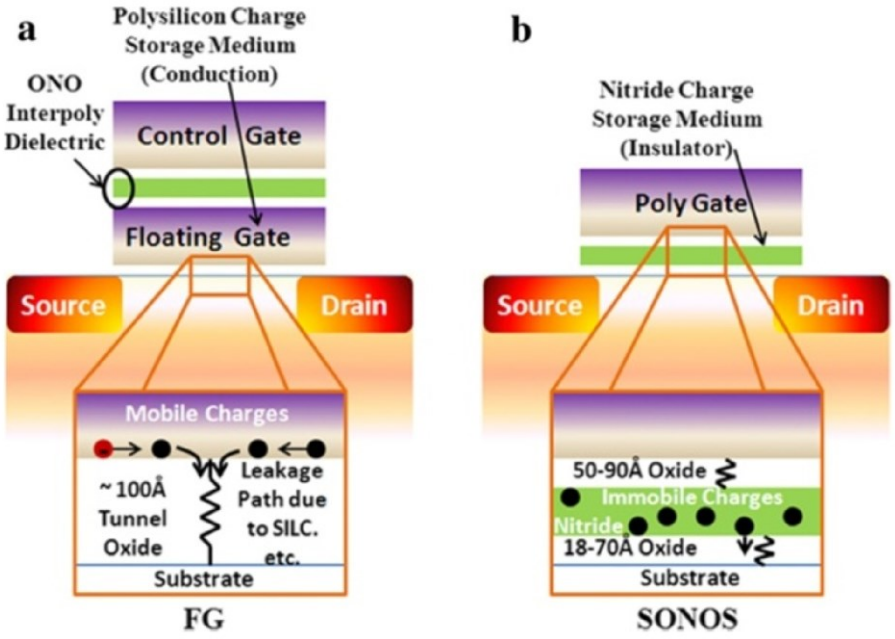
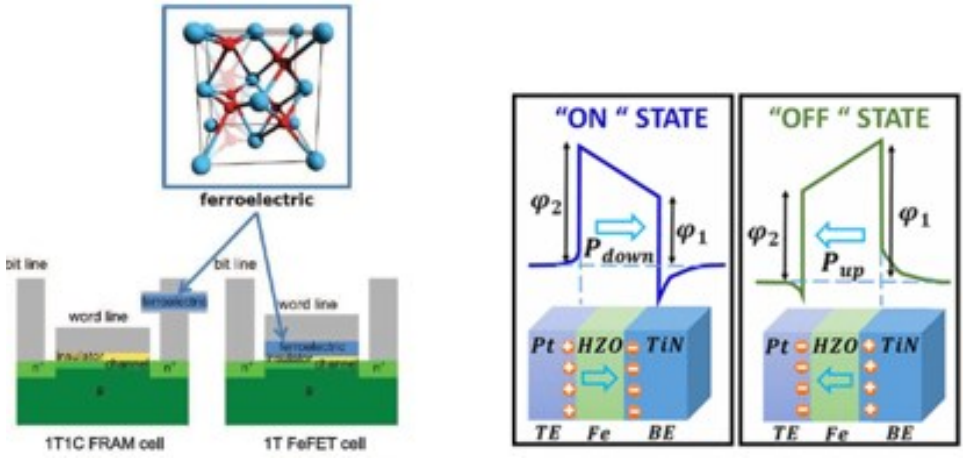


*Figure 1. 10 Schematic view of a conventional floating-gate based Flash memory cell: SILC induces early charge leakage through traps generated in the tunnel oxide. (b) Charge-trap memory concept: the polysilicon floating gate is replaced by a continuous charge-trapping layer (i.e. Silicon Nitride) in order to prevent charge leakage due to SILC. From [**29**]*

This type of memory cell is commonly referred as SONOS (Silicon Oxide Nitride Silicon) in relation with the composition of the memory gate stack **[33]**.

2.2.b. Ferroelectric RAM and emerging Ferroelectric devices

Ferroelectric memories rely on the same physical switching mechanism; switching due to the reversal of spontaneous electric polarization of a thin ferroelectric film under an electric field. Given this principle, a *FeRAM* memory cell consists in a 1 transistor-1 capacitor (1T1C) where the ferroelectric film is sandwiched within the capacitor. Reading is achieved through a current measurement achieved during the application of a voltage pulse across the ferroelectric capacitor in order to detect a polarization reversal current (reading can therefore be destructive).



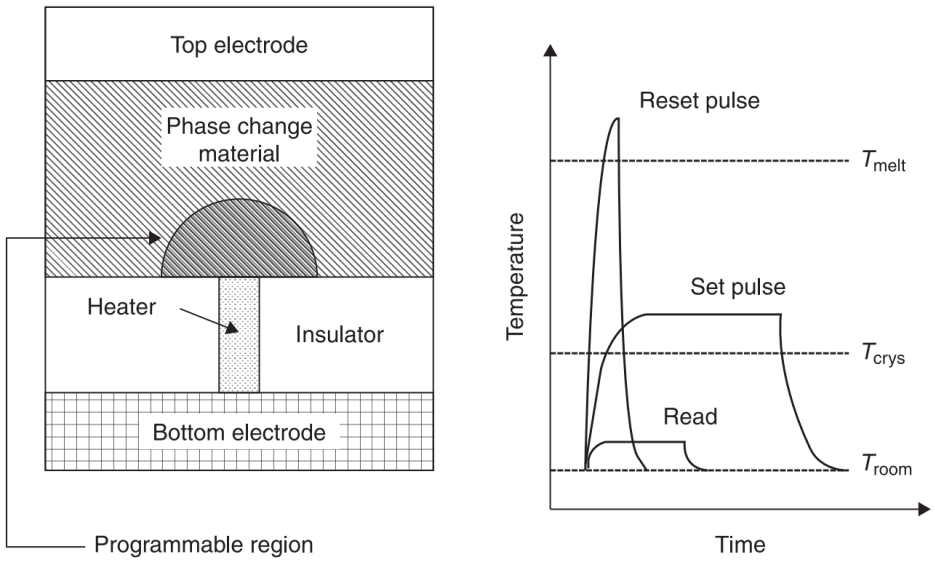
(a) (b)

Figure 1. 11. Illustration of ferroelectricity-based non-volatile memories. (a) 1T1C FeRAM and 1TFeFET and,, (b) Ferroelectric Tunnel Junction (FTJ). Adapted from ***[34]***

The first commercial prototypes of FeRAM were demonstrated in 1988 using the most common ferroelectric such as PbZrTi (PZT) and $SrBi_2Ta_2O_9$ (SBT) **[35][36]**. However, due to low coercive fields and high annealing temperatures, these materials could not be integrated beyond the 180 nm node **[37]**. The recent discovery of ferroelectricity in doped HfO_2 has renewed the interest for ferroelectric memory since 2011 **[38], [39]**. Given its excellent compatibility witch CMOS technology and it low annealing temperature (<450°C) ferroelectric HfO_2 can be integrated within the gate stack of transistors to achieve 1T *Ferroelectric FET* (1T-*FeFET*) memory cells [**Figure 1. 11**]. Another option to exploit ferroelectricity for non-volatile memory is to exploit the Tunnel Electro Resistance (TER) contrast within a Ferroelectric Tunnel Junction (FTJ) as depicted in [**Figure 1. 11**]. In this case, the barrier height modulation due to polarization reversal induces an asymmetric band bending resulting in a distinct resistance states **[40]**.

2.2.c. Phase-Change Memory (PCM)

PCM devices exploits the large electrical resistivity contrast between the amorphous and the crystalline states of chalcogenide glasses (the most commonly used alloy is $Ge_2Sb_2Te_5$, namely GST) to store binary states **[41]**. As depicted in **Figure 1. 12** the device consists of a top electrode, the chalcogenide phase change layer, and a bottom electrode. The bottom electrode contact is achieved through a confined “heater” in order to promote confinement of the current lines and therefore improved thermal heating in the vicinity of the chalcogenide/heater interface.



(a) (b)

*Figure 1. 12 Schematic cross-section of conventional PCM cell: resistance switching is due the localized reversible phase transition of a phase-change material in the vicinity of a confined "heater" contact. (b) Illustration of the temperature profile during the different operating sequences of the PCM cell. From **[41]**.*

The PCM operation is depicted in **Figure 1. 11**; during *set* the chalcogenide alloy is melted above its crystallization temperature through the application of a voltage pulse resulting in the formation of a low resistive crystalline phase. The reverse *reset* operation (i.e. crystalline to amorphous transition) is achieved through the application of a short electric pulse with a larger temperature during which the chalcogenide alloy is momentarily heated above its melting temperature and then quickly quenched into an amorphous phase with high resistivity. Finally, the resistance state of the cell is read through a voltage pulse at low voltage.

2.2.d. Resistive RAM (RRAM)

Figure 1. 13 depicts the architecture of a RRAM cell. The device consists in a simple Metal-Insulator-Metal architecture where a resistive switching layer is sandwiched between two metallic electrodes. Resistance switching is mainly observed within metallic oxides (such as TiO_2, HfO_2, Ta_2O_5) and is controlled by the creation/migration of *oxygen vacancies* due the application of an electric field across the memory cell **[29]**. Given the fact they are controlled by oxygen vacancies within a metallic oxide, RRAM are also referred as *Valence*

Change Memory or *OxRAM* (*Oxide RAM*) memories **[42][43]**. As the electric field approaches the breakdown field, oxygen ions/oxygen vacancy pairs are created and migrate across the metallic oxide. Since oxygen vacancies act as discrete electronic states within the bandgap of the oxide, a localized conduction path is initiated inducing then *Joule heating*. Finally the interplay between oxygen vacancy generation and Joule heating result in the creation of a conductive filament bridging top and bottom electrodes **[44]**.

The device is then *set* in a so-called *Low Resistance State* (*LRS*). The opposite *reset* operation is also achieved through the application of a voltage sweep (or voltage pulse) having the same or an opposite polarity leading to *unipolar* or *bipolar* operations [**Figure 1. 13**]. In this case it is the combination of Joule heating and oxygen vacancy recombination which leads to a partial breakdown of the conductive filament [**Figure 1. 13**] and restoring a *High Resistance State* (*HRS*).

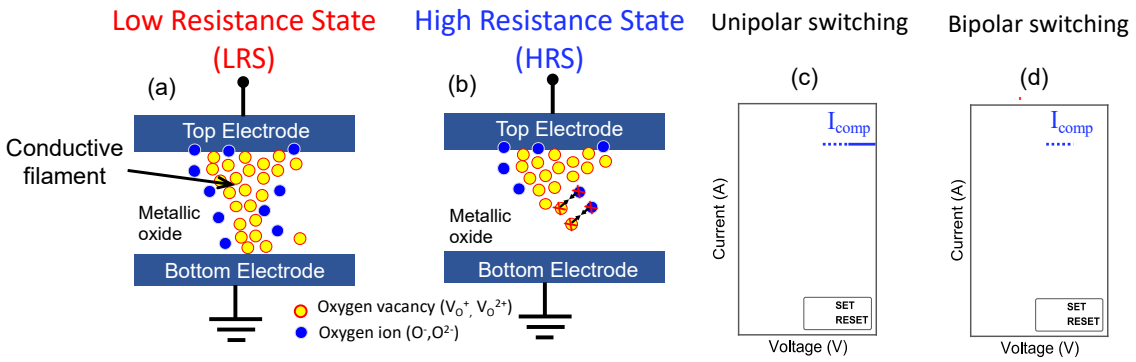


Figure 1. 13 Schematic view of a RRAM cell (a) in its Low Resistance State (HRS) and (b) High Resistance State (HRS). Resistance switching is due to the reversible creation/dissolution of an oxygen-vacancy rich conductive filament within a metallic oxide. Resistance switching can be either (c) unipolar or (d) bipolar.

It has to be noted that the first resistance switching, operated on a pristine state, is generally achieved at a higher voltage than subsequent set operations. This stage corresponds to the *forming* or *electro-forming* operation **[44], [45]**. During the *set* operation the current flow through the device has to be controlled in order to avoid an irreversible dielectric breakdown of the oxide. This current limitation can be achieved through the use of the *current compliance* (I_{comp}) of the parameter analyzer or by putting a current limiting device in series with the memory cell such as a resistor or a transistor **[46]**.

2.2.e. Conductive Bridge-RAM (CBRAM)

Conductive-Bridge RAM (CBRAM) also referred as Electro Chemical Memory (ECM) **[47]** or Programmable Metallization Cell (PMC) **[48]** can be viewed as a close technology from RRAM in the sense that they also rely on the reversible creation/dissolution of a conductive filament within an insulating material. The working principle of CBRAM devices is illustrated in **Figure 1. 14**.

The device structure consists in an insulating *Solid Electrolyte Layer* (acting as a ion-conductor layer) sandwiched between an oxidizable *Active Electrode* (*i.e.* Ag or Cu) and an (electrochemically) inert *Counter-Electrode* (e.g.: Pt) **[47]**.

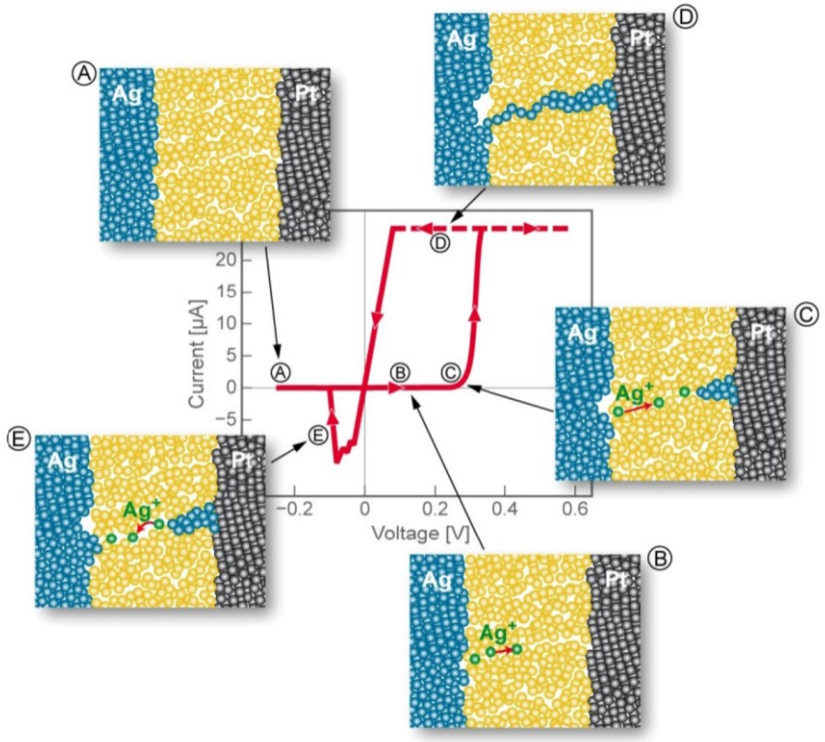


*Figure 1. 14 Typical current-voltage characteristic of a Conductive-Bridge RAM (CBRAM). Figures (A)-(E) in inset describe the elementary processes responsible for resistance switching: (A): virgin cell, (B): active electrode oxidization and cation migration. (C): Electrodeposition of metallic cations at the counter-electrode resulting in (D) the formation a metallic-rich conductive filament. (E) Oxidization of the conductive filament resulting in the opening of a gap. From **[47]**.*

Resistance switching is induced by successive elementary processes denoted from (A) to (E) in **Figure 1. 14** depending on the polarity of the applied voltage with respect to the active electrode (*i.e.* Ag or Cu).

Starting from a pristine cell [**Figure 1. 14**], the application of a positive voltage induces *anodic dissolution* of the active electrode given the following reaction [**Figure 1. 14**]:

$$A_g \rightarrow \mathrm{A_g^+} + \mathrm{e^-}$$

Due to the electric field within the solid electrolyte layer, cations migrate toward the counter-electrode (*i.e.* cathode) where they can be *electrochemically reduced* according to:

$$A_g^+ + e^- \rightarrow A_g$$

This process initiates the *growth of a conductive filament* extending from the inert toward the active electrode [**Figure 1. 14**]. Due to the increased electric field at the apex of the conductive filament and the continuous dissolution of metallic cations within the solid electrolyte, the filament grows until it reaches the active electrode, resulting in the *set* operation [**Figure 1. 14**]. The cell remains in its Low Resistance State until a sufficiently negative bias is applied to electrochemically dissolve the conductive filament during the *reset* operation [**Figure 1. 14.E**]. As for RRAM technology, a strong interplay between oxidization/reduction rates and joule heating is also expected during set and reset operations **[49]**.

If active electrodes generally consist of copper or silver, a wide variety of materials has been demonstrated for both the solid electrolyte layer and the counter-electrode **[50][51][52]**. The different classes of materials use for the solid electrolyte layer include *mixed (ion-electron) conductors* based on *chalcogenide alloys* such as (non exhaustively) Cu_2S or Ag_2S **[53]**, Ag or Cu doped $GeSe_x$ **[54][55]**, Cu-GeTe **[56]**, Ag-$Ge_2Sb_2Te_5$ **[54][55]**, *insulators* and *metallic oxides* (*e.g.* SiO_2, Al_2O_3, GdO_x)**[59][60][61]** and *polymer/biopolymer materials* such as Polyethylene Oxide **[62]–[64]**, chitosan**[65]** or aloe vera **[66]**. Note that this latter class of material is of particular interest for flexible electronics, given their inherent mechanical flexibility, processability over large areas and affordability.

3. Flexible Non-Volatile Memories

3.1. Why non-volatile memories for flexible electronics?

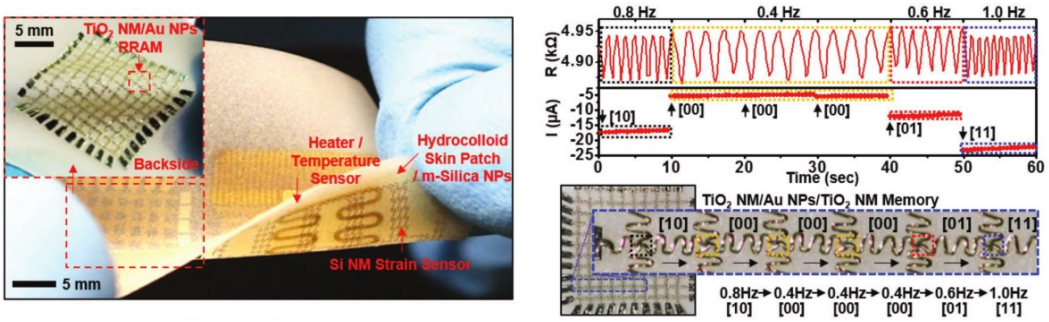
Flash Memory is the major technology in the field of non-volatile memory, due to a market highly stimulated by mobile electronics **[22]**. Today, integration densities as high as 1TB on a single die are commercially available[3]. In this context, it would seem illusory to attempt to compete with Flash technology with flexible memories for mass storage applications. However, as shown in **Table 1. 1**, *there is a need for low memory densities* from few bits to kbits for applications such as e-tickets, RFID tags **[67]** or for storing as small volume of data near a sensor for wearable devices **[68][69]**. In addition, some of these applications only require One Type Programmable (OTP) or WORM[4] type of non-volatile memories**.** *In this context, flexible non-volatile memories can be very advantageous as they could be directly processed onto the flexible substrate* without requiring additional integration steps such as soldering a Non-volatile memory module.

Parameter	Desired
Retention	**Month/Year**
Write Time	**µs to ms**
Read Time	**µs to ms**
Programming Voltage	**<24V**
Type of Memory	Strongly dependent on application **Single Use (WORM[4])** **Rewritable**
Memory Array size	Strongly dependent on application RFID : **8 to 128 bits** Smart packaging, toys, smart-cards, badges, e-tickets, wearables, sensor node : **1-64kbits**
Area	Less critical **~mm² or more**
Endurance	Strongly dependent on application **10^3 to 10^6 cycles**
Operating temperature	Archival : **-40°C to +85°C** Operating: **-20°C to +50°C**

*Table 1. 1 Main requirements for flexible non-volatile memories. Adapted from **[68]***

[3] https://news.samsung.com/global/samsung-breaks-terabyte-threshold-for-smartphone-storage-with-industrys-first-1tb-embedded-universal-flash-storage
[4] Write Once Read Many

Figure 1. 15 gives an illustration of the kind of new opportunities that can be brought by flexible non-volatile memory devices.



(a) (b)

*Figure 1. 15 Picture of a wearable skin patch for tremor analysis. The patch features strain/temperature sensors together with a heater on one side and an array of 10x10 TiO_2-based RRAM devices on the other side (see inset) (b) The oscillation frequency related to tremors, monitored by the strain sensors (top) are encoded as compliance current for programming the RRAM devices (bottom). Adapted from **[69]**.*

In this research work conducted by the Seoul National University (Korea) in association with the University of Texas at Austin (US), authors have developed a hybrid multifunctional skin patch to monitor tremor in view of treatment of Parkinson's disease **[69]**. As shown in **Figure 1. 15**, the double-sided wearable patch features an array of strain sensors, to monitor tremors, a temperature sensor, a 10x10 array of TiO_2-based RRAM and a heater. The recorded tremor frequency measured by the strain sensor [illustrated in **Figure 1. 15**] is converted into a compliance current value exploited to program the RRAM cells. Memory devices can be then read repeatedly for 10 s. As the tremor frequency reaches a critical value, drug is delivered by transdermal diffusion promoted by the heater device.

Although the overall control of the skin patch is still achieved via an external electronic system, this work illustrates that the integration of non-volatile memory devices can bring a valuable contribution to the development of smart flexible systems.

3.2. Non-volatile memories for flexible electronics

Taking their inspiration from emerging technologies exposed in the previous section, numerous research works have been devoted to the development of non-volatile flexible memories over the last years **[32][70]**. **Figure 1. 16**, issued from the review of Ghoneim *et*

al., provides an overview of the main memory technologies explored on flexible substrates **[32]**.

Besides the different NVM technologies, the authors of this review also reported on the technological approaches to achieve flexible devices which include:

- The **all-organic approach** where the entire memory device is obtained from organic materials only using fabrication techniques such as inkjet printing /spin-coating/ roll-based processes. In this context, fully printed CBRAM featuring PEDOT:PSS or Polyethylene Oxide where successfully achieved on flexible substrates **[71][63]**. Apart from memory, *organic transistors* can also be processed on the flexible substrate to achieve 1T organic memory devices such as 1TFeFET **[72]–[74]** or 1T Charge-Trap memories **[69],[70]**. With respect to the different flexible electronics approach described earlier, this approach mainly combines printed electronics together with organic and plastic electronics.
- The **Hybrid System approach** combines both organic and inorganic materials by employing a wider spectrum of fabrication processes. In addition, in order to take advantage from materials and processes issued from the semiconductor industry, the memory devices or arrays can be fabricated on a rigid carrier substrate (i.e. glass, silicon or Silicon-On-Insulator substrate) and then transferred on a flexible substrate. In this context, this approach is similar to Flexible Hybrid Electronics as described in the first section of this chapter. Following this method the Korean Institute of Science and Technology (KAIST) has successfully reported on arrays of 1Transistor-1Resistor of TiO_2-based RRAM and, more recently, Phase-Change Memory arrays on a polyestersulfone (PES) substrates **[77][78]**.

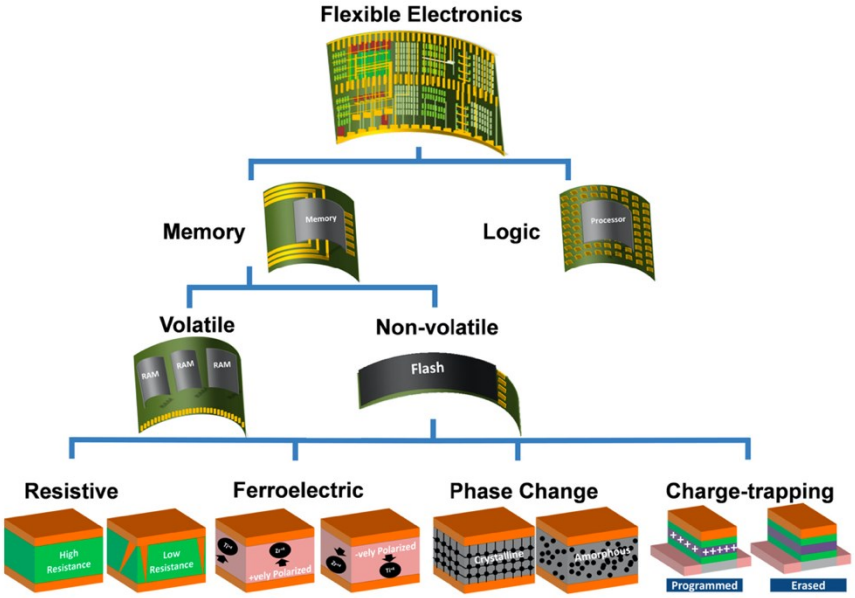


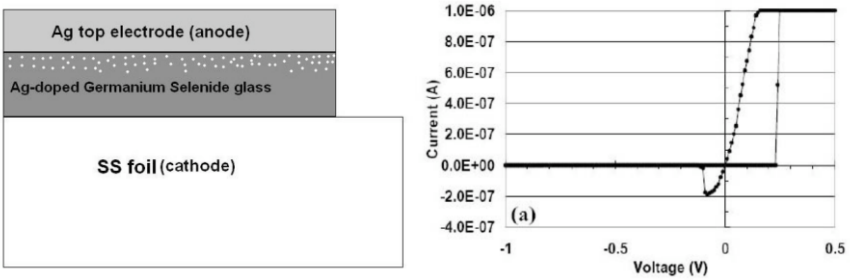
*Figure 1. 16 Overview of flexible of non-volatile memories for flexible electronics. From **[32]***

Among the wide variety of available NVM technologies and fabrication routes to achieve flexible non-volatile memories, our work has been conducted on the development of flexible CBRAM devices because of their simple MIM architecture and the wide variety of demonstrated materials. In the following, we will then present a survey of the works devoted to flexible CBRAM.

3.3. Flexible CBRAM devices

3.3.a. CBRAMs based on a chalcogenide layer

One of the pioneering work reporting flexible CBRAM devices was conducted in 2007 by Baliga *et al.* from Arizona State University **[54]**.



(a) (b)

*Figure 1. 17 (a) Schematic cross-section of the CBRAM stack reported by Baliga et al. The flexible substrate consists of a stainless-steel foil. (b) Current-Voltage characteristic evidencing resistance switching. From **[54]**.*

The device relied on a Ag-doped GeSe chalcogenide glass deposited on thin metallic stainless-steel foil [**Figure 1. 17**]. As stated by the author, chalcogenide glasses have a remarkable degree of flexibility with mechanical properties lying between oxide glasses and polymer materials making them appealing for flexible electronics. As seen in [**Figure 1. 17)**] the device exhibited unambiguous resistance switching at low voltages. The devices also demonstrated to remain functional after 3 hours of bending with a bending radius of 0.9 cm.

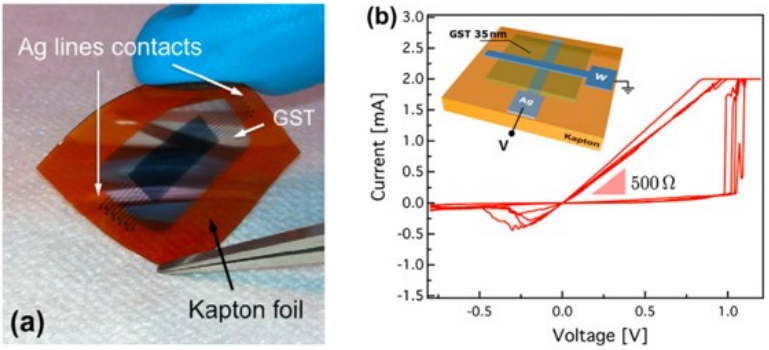


Figure 1. 18 CBRAM based on an amorphous GST ($Ge_2Sb_2Te_5$) layer on a polyimide (kapton) substrate. (b) Current-Voltage characteristics of the fabricated device.

Still based on chalcogenide layers, in 2013 a research group from Aix-Marseille University (France) reported on the fabrication of CBRAM devices employing a 35 nm-thick GST ($Ge_2Sb_2Te_5$) layer deposited by Physical Vapour Deposition (PVD). Devices were

fabricated on a polyimide flexible substrate and showed repeatable resistance switching [**Figure 1. 18**] **[58]**.

3.3.b. CBRAMs based on a polymer layer

Besides chalcogenide layers, polymer materials were also demonstrated as solid polymer electrolyte layer. In 2011 and 2012, Wu *et al.* and Mohapatra *et al.* (National Institute for Materials Science, Japan) showed that CBRAMs can be fabricated using a Polyethylene Oxide (PEO) layer as the solid polymer electrolyte (SPE) layer **[63], [64]**. In **[60]** devices based on an inkjet printed PEO layer on a polyethylene naphthalate (PEN) substrate were demonstrated [**Figure 1. 19**].

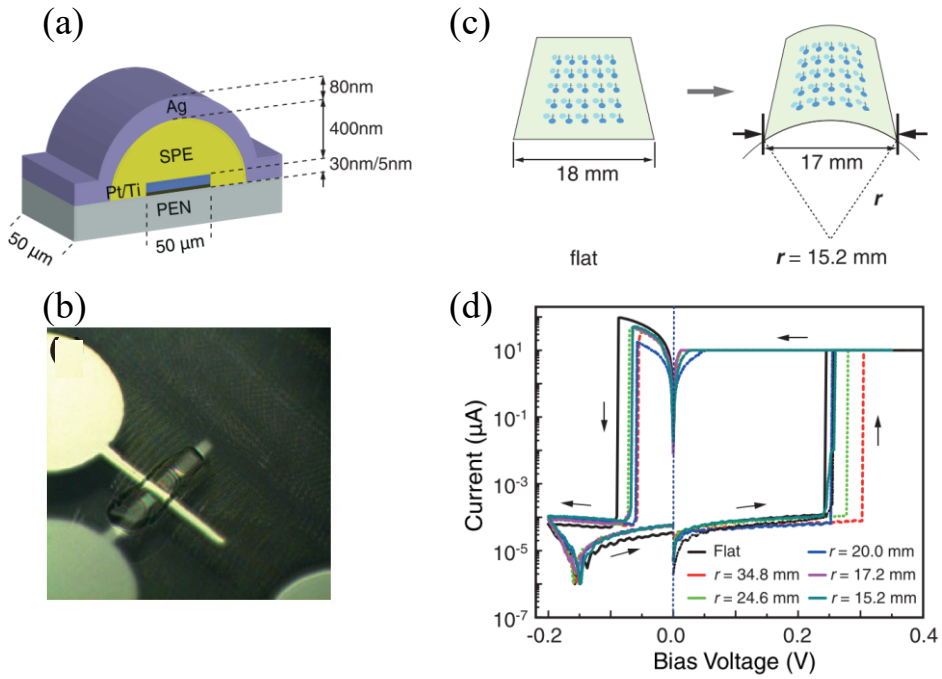


*Figure 1. 19(a) Schematic cross-section of the polymer-based CBRAM obtained by printing technique. (b) Optical view of the printed device. (c) Configuration of electrical measurements under mechanical stress and (d) corresponding current-voltage characteristics obtained at various bending radii. Adapted from **[63]**.*

In their fabrication procedure acetonitrile (ACN), which is a toxic solvent, was used for the deposition of the SPE layer. However, Wu *et al.* earlier reported that water can also be used as the solvent for PEO layer deposition **[79]**. As shown in [**Figure 1. 19** the devices were demonstrated to sustain bending radii down to 15.2 mm.

In **[64]** author reported that doping the PEO layer with $AgClO_4$ silver salts can affect both programming voltages salts and retention capabilities. For instance, by increasing the silver salt fraction mass from 1 to 3 wt. %, they observed a ~1 week retention time. However, no switching behavior was observed for salt concentrations greater than 6 wt. %. The authors attribute this phenomenon to a modification of the *crystallinity ratio* (*i.e.* ratio between the amorphous and crystalline phase) induced by doping. Indeed, cation movement within the polymer is mostly achieved along the amorphous phase through *segmental chain motion*.

In 2016, Krishnan *et. al* fabricated planar devices to observe the conductive filament growth mechanism via ex-situ Scanning Electron Microscopy (SEM) **[80], [81]**. As shown in **Figure 1. 20** dendrites or clusters of Ag within a 3 wt. % doped PEO layer (referred as Ag-PEO) were observed on the planar gap upon cycling.

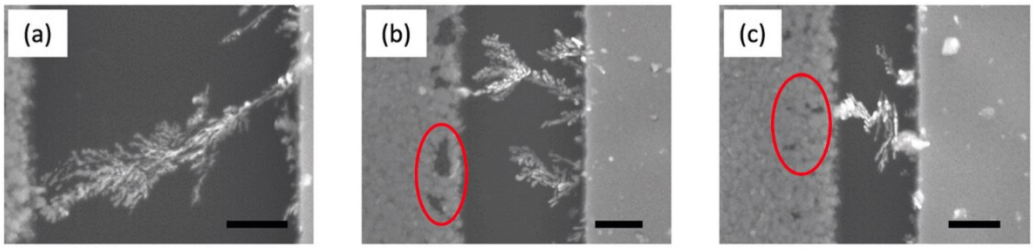


*Figure 1. 20 Ex-situ SEM images showing the morphology of the conductive filament within a Ag/Ag-PEO/Pt planar device at varied gap distance of (a) 2µm (b) 1µm and (c) 0.5µm. Filament was formed during voltage sweep performed at 2mV.s^{-1} with a 100nA compliance current. Red circles highlight the formation of voids within the Ag electrode (left). From **[81]**.*

Hence, substantial research works were conducted by Wu, Krishnan, Mohapatra *et al.* on Polyethylene oxide as solid polymer electrolyte (SPE) layer which make it clear that PEO can serve as solid electrolyte layer (SPE) to achieve flexible devices.

Table 1. 2 summarizes the main results obtained by Wu, Mohapatra and Krishnan in terms of endurance, ON/OFF ratio and retention time capabilities. It has to be mentioned that most of these work were conducted on a *silver doped PEO* layer, which was shown to strongly influence set/reset voltages **[64]**.

Parameter	Wu 2009, 2011 [64], [79]	Krishnan 2016 [80], [81]	Mohapatra 2012,2015 [63],[82]
Flexible Substrate	**No**	**No**	**Yes (PEN)**
Solvent used	Water	Acetonitrile	Acetonitrile
Typical SET voltages	0.5 to 2.5 V *	0.25 to 0.5V	0.25 to 0.5V
Typical RESET voltages	-0.5 to -3.0V *	-0.1 to -0.3V	-0.1 to -0.3V
Endurance cycles	>100	~ 1000	~100
ON/OFF ratio	10^6	10^6	10^5-10^6
Retention time	10^4-10^5 s	N/A	N/A
Doping with $AgClO_4$	Yes (1-8 wt. %)	Yes (3 wt. %)	Yes (3 wt. %)

Table 1. 2 Summary of the works on PEO based CBRAMs.
** : strongly dependent on doping $AgClO_4$ wt.%*

3.3.c. Towards flexible biopolymer-based CBRAMs

Besides their affordability and processability over large areas, which makes them of particular interest for flexible electronics applications, biocompatibility and biodegradability can also be appealing properties to achieve the sustainable development of flexible devices **[83]**.

In this context, CBRAM devices featuring biocompatible materials such as aloe-vera or chitosan were recently developed **[62][66]**. **Figure 1. 21(a)&(b)** show chitosan-based CBRAMs on PES flexible substrates and their corresponding current-voltage curves reported by Hosseini *et al.* from Pohang University of Science and Technology (Korea). In addition, in ref. **[83]** the same authors showed that using magnesium (Mg) electrodes Mg/Ag-doped chitosan/Mg memory devices could be advantageously dissolved using water as solvent as illustrated in **Figure 1. 21(c)-(f)**.

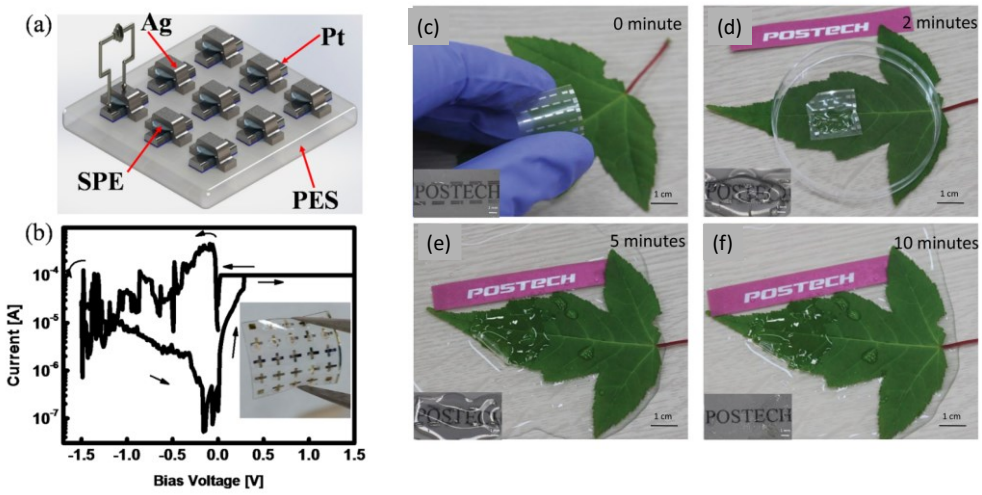


Figure 1. 21 (a) Schematic view of chitosan-based CBRAMs on PES substrates with (b) a corresponding current-voltage characteristic. (c)- (d) illustrates the progressive dissolution of the whole devices, featuring a Mg inert electrode, immersed in water. From ***[62]*** *and* ***[78]****.*

4. Chapter conclusion, research work objectives and manuscript organization

A) Conclusion

After being guided for nearly 50 years by Moore's Law, the *electronics market is now facing new challenges as it enters the Internet of Things (IoT) era*. The instrumentation of objects with arbitrary surfaces and shapes requires a paradigm shift with respect to silicon electronics.

Due to its ability to produce flexible electronic functions over large areas and at low production costs, *flexible electronics is regarded as an essential technology to meet these new challenges*. In conjunction with silicon electronics, flexible hybrid electronics is therefore forecasted to be a very promising way to support the development of IoT.

After logic, *memory is an essential component of any electronic system*. In the silicon industry, this market is currently dominated by non-volatile Flash-type memory. Due to its intensive miniaturization over the past ten years *Flash Memory is currently facing fundamental limits*, both from a physical and technological point of view. Benefiting from intensive R&D efforts to develop alternatives to Flash memory, *many emerging technologies, mainly based on resistance switching, have emerged*. Among these technologies, *RRAM and CBRAM are very promising solutions for replacing Flash memory.*

Taking their inspiration from emerging memory technologies, numerous works have demonstrated the feasibility of resistive memories on flexible. After describing the interest of non-volatile memory for flexible electronics, we showed that various approaches are currently explored to achieve flexible non-volatile memories on flexible substrates, ranging from all-organic devices, hybrid organic/inorganic devices up to more complex techniques involving transfers from rigid substrates. In this context, *we focused our approach on the fabrication of CBRAM devices*, due to (i) their simple MIM structures and the (ii) wide variety of demonstrated materials, from inorganic chalcogenide layers up to biocompatible and biodegradable polymer films as exposed in the last section of this chapter.

B) PhD Objectives and manuscript organization

The overall objective of this PhD work concerns the development of CBRAM devices for flexible electronics applications. Given the demonstrated materials for solid-electrolyte, our approach was to select *polymer materials* as they remain very appealing due to their low-cost, processability over large areas, their excellent mechanical flexibility and their capability to be tailored through molecular design or doping.

Among the wide family of polymer materials, *Polyethylene Oxide – namely PEO – was chosen* given it was already demonstrated as a valuable material for CBRAM applications. In addition, PEO is affordable and can be processed using water as solvent which makes it a good choice in view of sustainable development.

In order to expose our work, the manuscript is organized as follows:

- In **Chapter 2**, the fabrication process of CBRAM devices is exposed, including polymer solution preparation and spin-coating conditions for obtaining thin film of various thicknesses. Two distinct configurations of memory devices were fabricated: vertical and planar devices.
- In order to evaluate the electrical performance of our polymer CBRAMs, vertical devices on silicon substrates are studied in **Chapter 3**. The influence of programming conditions on set/reset voltage, resistance distribution and retention time is presented together with an analysis of conduction regimes in both LRS and HRS. This study served at a first step toward the development of a statistical model accounting for electrical variability.
- In an attempt to study morphological and chemical changes within the solid-polymer electrolytes, planar CBRAM devices featuring a thin nanogap between Ag and Pt electrodes were studied in **Chapter 4**. In particular, AFM, together ex-situ SEM with EDX (Energy Dispersive X-ray) were conducted on virgin and cycled devices.
- Finally, **Chapter 5** is devoted to the study of flexible CBRAM devices fabricated on Kapton. After electrical characterization on planar surfaces, the devices were subjected to various mechanical stresses and their performances evaluated. The study of conduction mechanisms is also presented on flexible devices together with a comparative study of CBRAM devices on flexible and silicon substrates.

5. References

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Chapter 2 - Fabrication procedure of polymer based CBRAMs

This chapter presents the fabrication processes involved in the development of the memory devices. Firstly, as Polyethylene oxide (PEO) is the main active layer of our devices, the preparation of PEO solution, its deposition and characterization by Differential Scanning Calorimetry (DSC) is exposed. Hence, this section provides the link between spin coating conditions and PEO thickness on Si/SiO_2 substrates. The PEO thickness is evaluated using a profilometer and Atomic Force Microscopy (AFM) to observe its morphology.

In the next section, the fabrication procedure of two types of CBRAM devices – namely, vertical and lateral ones – is described. The vertical ones include fabrication on silicon and flexible substrates, while the planar ones are only fabricated on silicon so as to further conduct morphological observation on these devices.

1. Solid Polymer electrolyte layer preparation & analysis

1.1. Polyethylene oxide (PEO) properties

In this work, Polyethylene oxide (PEO) is the solid polymer electrolyte used for our CBRAM devices. The structural formula is H- $(CH_2\text{-}CH_2\text{-}O)_n$ –OH. **(Figure 2.1)**

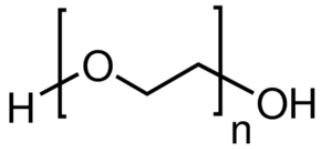

Figure 2.1 The structural formula of PEO.

Depending upon the molecular weight, PEO can be referred either as Polyethylene glycol (PEG) or PEO. PEG is mostly used if the molecular weight is less than 20,000 g/mol whereas PEO corresponds to higher molecular weights.

Polyethylene oxide has been selected as the solid polymer electrolyte because of its following properties **[1]**:

i) *Solubility*: PEO is water soluble, hence deionized water was chosen as solvent for our solid polymer electrolyte (SPE) layer **[2]**.

ii) *Biocompatible polymer*: has the possibility to be used as skin patches, wearables **[3]**.

iii) *Film forming and hydrophilicity*: enables its deposition using printing techniques as well as on flexible substrates like PEN, PET, kapton **[4]**.

iv) *Compatibility with electrodes*, MIM structures can be formed using various electrodes, like Cu, W, Pt, Ag **[1]**.

v) *Price* for 250 g PEO (Sigma Aldrich) is 125 EUR, affordable compared to other polymers as PMMA, PI: PCBM **[5]**.

Table 2. 1 provides a summary of molecular weight, melting temperature and glass transition temperature of our PEO powder (Sigma-Aldrich Chemistry):

Molecular weight (Mw) (g/mol)	600 000
Melting temperature (T_m) (°C)	65
Glass transition temperature (T_g) (°C)	-45

Table 2. 1 Properties of Polyethylene oxide

1.2. Polyethylene oxide (PEO) film preparation

Spin coating is a very simple technique for film casting on Si or flexible substrates. Depending on the physical parameters like spin speed, spin coating time and drying time, the thickness of the film can be modulated from the nanometre to the micrometre range **[6]**. In the following we describe the preparation procedures for both pure (undoped) PEO and doped PEO thin films obtained from PEO solutions.

1.2.a. Un-doped PEO solution

The general procedure for PEO solution preparation is depicted in **Figure 2. 2**. To achieve a targeted mass concentration, a controlled mass of PEO powder is added in deionized water according to:

$$m_{PEO} = c_{PEO} \cdot v_{H_2O}$$

where:

c_{PEO} is the targeted mass concentration (g/L)

v_{H_2O} is the volume of deionized water (L)

m_{PEO} is mass of PEO powder (g)

As an illustration, a pure concentration of 20 g/L is prepared by adding 1000 mg of PEO powder in 50 mL of deionized (DI) water. The solution is then kept on a hot plate at ~30°C for stirring for 20 h with a speed of 1000 rpm to completely dissolve the PEO in water [**Figure 2. 2**].

According to this procedure, PEO solutions with concentrations ranging from 10 g/L to 20 g/L were prepared from our pure PEO powder. To investigate the properties of thick standing films, thick PEO films were formed from 20 g/L PEO solution by putting 10-12 mL in a petri dish and drying in a vacuum chamber at 80° C for 19 hours. Films were measured with a digital thickness gauge and were approximately 18-20 µm.

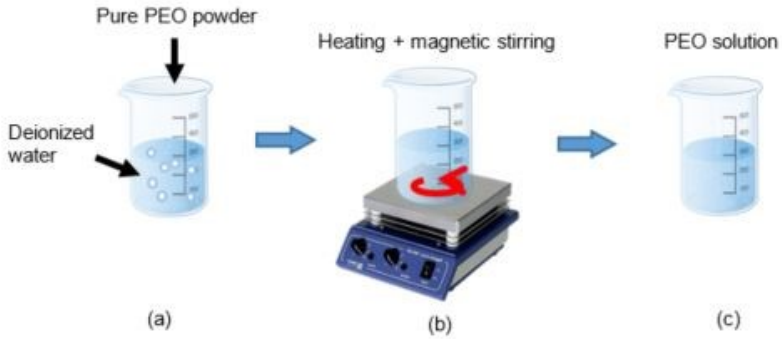

Figure 2. 2 Procedure for PEO solution preparation. (a) PEO powder is added in deionized water. (b) The solution is kept 20h on a hot plate at 30 °C with magnetic stirring to achieve (c) a complete dissolution.

1.2.b.Doped PEO solutions

Ag-doped PEO solution was prepared using PEO powder and Ag-salt powder Silver Perchlorate Hydrate (99%) - $AgClO_4.xH_2O$ (Sigma-Aldrich, Chemistry).The procedure for preparing Ag-doped PEO solutions is similar to the one depicted in the previous section but includes addition of silver salt together with PEO powder in its first step [see **Figure 2.3**].

In this section, we describe the method to prepare a PEO solution doped with a controlled Ag weight percentage (referred as x in the following).

$$x = \frac{m_{salt}}{m_{salt} + m_{PEO}}$$

$$m_{salt}(1 - x) = x\, m_{PEO}$$

$$m_{salt} = \frac{x}{1 - x} m_{PEO}$$

where: x is the weight percentage

m_{salt} is the mass of salt (g)

m_{PEO} is mass of PEO powder (g)

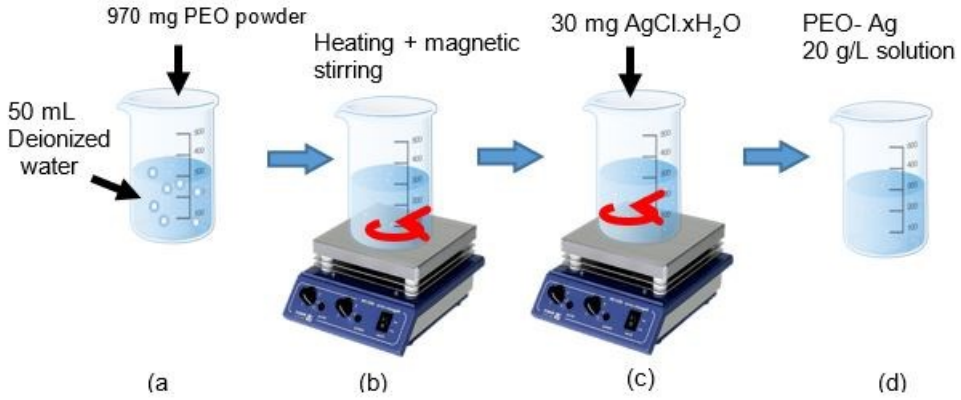

Figure 2.3 Procedure for doped PEO solution preparation. (a) PEO powder is added in deionized water. (b) The solution is heated at 30°C and magnetically stirred to achieve a complete dissolution for 20h, later for an hour, Ag salt (c) is added and stirred magnetically without heating. (d) PEO – Ag salt solution with 20 g/L concentration.

1.3. Analysis of PEO layer by Differential Scanning Calorimetry (DSC) measurements

As mentioned in **Chapter 1**, the segmental chain motion of the polymer composed of amorphous and crystalline regions is responsible for movement of ions in the polymer

matrix to form the conductive filament. Therefore, we tried to find out techniques through which the crystallinity ratio of the polymer can be evaluated **[7]**. Differential Scanning Calorimetry (DSC) is a thermo-analytical technique to measure the temperature and heat flow of a sample and a reference which can be employed to evaluate the crystallinity ratio of polymer materials.

1.3.a. Experimental setup

Differential Scanning Calorimetry measurements were done on a DSC Q20 (TA instruments) as a characterization to find out change in crystallinity ratio with thermal treatment on the polyethylene oxide layer. The experimental data analysis was done with a Universal V4.5A TA Instruments software. The setup is explained in **Appendix A**. The reference DSC capsule is calibrated with indium weight 3.25 mg, T_m 157.4° C and enthalpy change (ΔH) 27 J/g. Note that the reaction enthalpy can be obtained by DSC measurement by integrating the area of the reaction peak and the interpolated baseline between the beginning and end of the reaction.

The films featured a PEO thickness of 18 µm prepared from PEO concentration of 20 g/L, M_w – 600,000 g/mol after vacuum drying for 19h at 80°C. An aluminium hermetic capsule was used for DSC measurements for pure PEO powder. The heating temperature ramp cycle was set as 10°C/min from -70°C to 150°C.

1.3.b. DSC on thermally treated 18 µm thick PEO films

The melting point temperature (T_m) is the temperature at which the polymer crystals melt, hence during this transition, all the heat is absorbed until all the crystals are melted (associated with the latent heat of fusion). In the DSC (Exothermic reaction Up) plot, this transition (T_m) is shown as a depression. Whereas the degree of crystallinity of the polymer can be calculated as the ratio between the enthalpy change (ΔH) around the melting point temperature and the enthalpy change (ΔH) observed for 100% crystalline polymer is 188 J/g **[8]**.

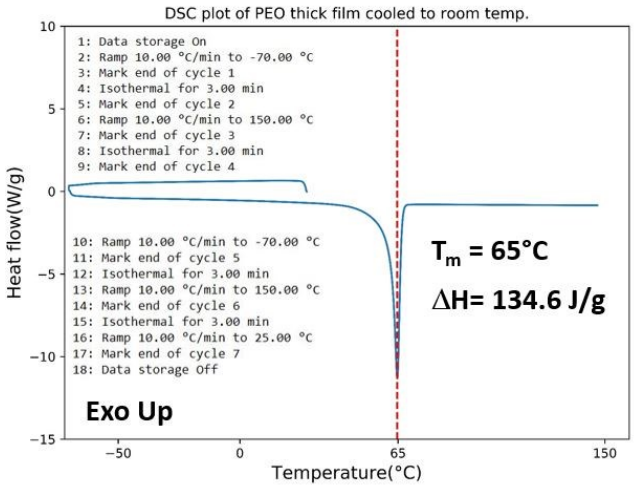

Figure 2. 4 DSC measurement plot of thick PEO film (18 µm) which is cooled to room temperature (RT). Inset shows the procedure of DSC.

Thermal treatment was done on the thick film (18 µm) PEO samples in two ways. In **Figure 2. 4** the thick film of PEO is cooled to room temperature slowly. In this case the enthalpy change is measured to be 134.6 J/g and the melting temperature 65°C. In this case the crystallinity ratio is calculated to be 71.6%.

In the second case, thermal treatment is done by cooling the thick PEO film with liquid Nitrogen as soon as it is taken out of the drying vacuum chamber. **Figure 2. 5** shows the DSC plot of the liquid N_2 cooled film. In this instance, the crystallinity ratio was calculated to be 62.5%.

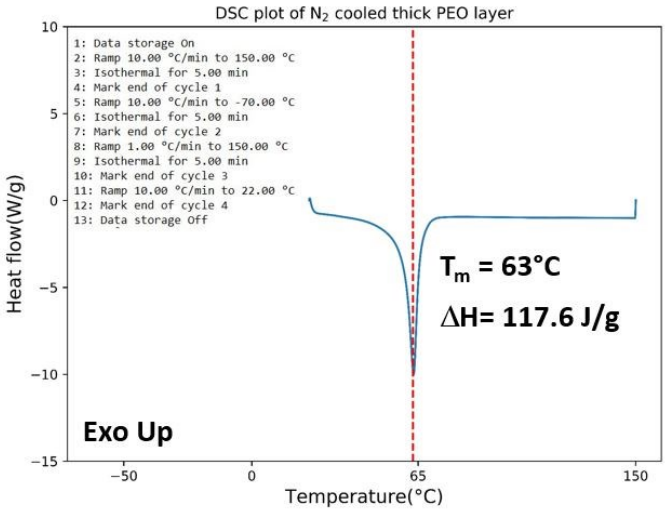

Figure 2. 5 Shows the DSC measurement plot of thick PEO film (18 µm) which is cooled immediately with liquid N_2 (77 K). Inset shows the procedure of DSC.

Hence, from the following two thermal treatment experiments:

i) Gradual cooling to room temperature (RT).

ii) Sudden cooling with liquid N_2;

It is clear that the crystallinity of the polymer film can be tuned by changing the cooling rate of the polymer just after vacuum drying of PEO. Hence, this can be inferred that the cooling rate is an important parameter to modulate the crystallinity of the PEO film. This result is in accordance with the literature, where the cooling rate affects the crystallinity either by affecting the crystallite domain size or the number of crystallites of the PEO film or both **[1] [9]**. The melting point temperature (Tm) indicates the temperature at which the polymer transits from crystalline into viscous flow state. It is an indicator to the processing conditions and the history of thermal treatment the polymer has undergone.

Confirming these results, firstly that through DSC, it is feasible to calculate the degree of crystallinity, and secondly, that cooling rate tunes crystallinity of the thick films; therefore, same procedure to calculate the degree of crystallinity is implemented on PEO films with thickness 150 nm.

However, due to constraint in deposition of 150 nm thin standing films through spin coating, and moreover its impracticality to do a DSC measurement (with a minimum required mass of 3 mg in the DSC capsule), the quantification of crystallinity ratio in thin PEO layers is far from practical and was not further undertook in this work. XRD and FTIR techniques have then been used to evaluate the crystallinity ratio. Having said that, these techniques were not successful for reasons of quantification. Hence, they are mentioned in the **Appendix B & C** respectively.

2. Thickness control of PEO layer & its morphological observation

In this work, spin coating was the deposition technique chosen to cast the active solid polymer electrolyte layer for our CBRAM devices. In the works of Krishnan *et. al*, Wu *et. al* or Mohapatra *et. al* a range of PEO thickness of 200 nm and above is mentioned; however there is no calibration plot showing the influence of spin coating parameters (such as spin speed, acceleration, time) or solution concentration on the final thickness of the PEO layer**[10]–[13][14], [15]**.

In this section, we carried out a systematic study on the influence of spin-coating parameters on the final thickness of PEO using solutions of different concentration. Consequently, the AFM, SEM images of the PEO layer are collected to check deposition and their morphology.

2.1. Influence of spin parameters coating on PEO thickness

As described in section 1.2, PEO, M_w 600,000 g/mol (Sigma Aldrich) was used to make 50 mL solutions with concentrations of 10.0 g/L, 15.0 g/L, 17.5 g/L and 20.0 g/L by stirring it overnight for 20h. After cleaning the Si/SiO_2 (750 µm/500 nm) substrates with acetone, iso-propyl alcohol (IPA), ethylene alcohol and N_2 gas, they were UV ozone treated for 20 minutes. This is done to enhance hydrophilicity of the Si/SiO_2 substrate. In the next step, PEO films were formed by spin coating (spin coater: *Polos-200*) dropping the PEO solution through 20 µm filters. Spin speeds ranging from 500 to 2000 rpm were used while the spin coating time and speed acceleration were kept constant respectively at 60 s and 1000 rpm/s.

The thickness of the deposited PEO layer was evaluated using a profilometer (Bruker Dektak XT). To aim this, an indentation on the Poly (ethylene oxide) layer was made with a scalpel at nine control points: the top, centre and the bottom parts of the substrate Si/SiO_2 (750 µm/500 nm – with an approximate substrate size of 5 cm x 5 cm. After this, a profilometer with a tip of 2 µm radius, was used to obtain the thickness profile perpendicularly to the scratched surface as shown in **Figure 2. 6** This measurement was performed over the 9 control points stated above.

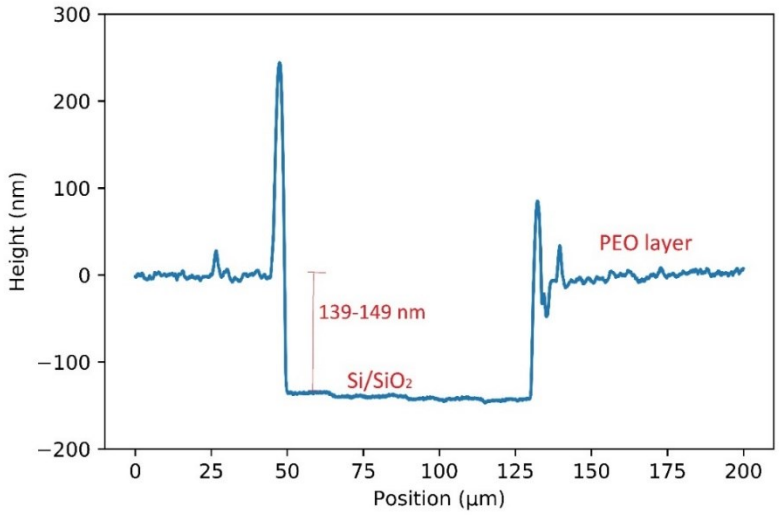

Figure 2. 6 Profilometer profile of PEO thickness, after indentation down to on the Si/SiO_2 substrate surface. Here, PEO layer thickness is measured to be 139-149 nm.

Figure 2. 7 shows the measured PEO thickness for different experimental conditions employed for spin coating. Errors bars correspond to the minimum/maximum thicknesses measured by the profilometer along the 9 control points. As depicted, the thickness can be varied from 25 nm to 225 nm for maximum spin speed of 2000 rpm and minimum concentration of 10.0 g/L, while minimum spin speed of 500 rpm and solution concentration of 20.0 g/L.

This provides a reference for further research work on this field to modulate the thickness and to identify optimal thickness value of PEO layer for CBRAM devices.

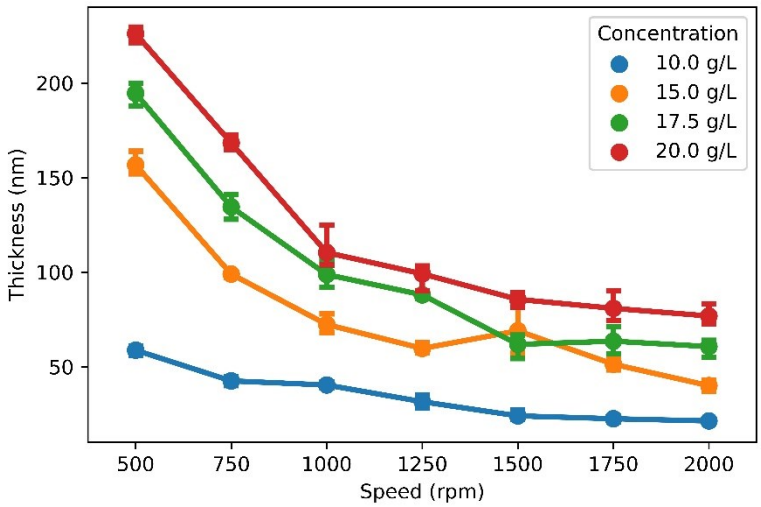

Figure 2. 7 Evolution of PEO thickness with spin coating speeds from 500 rpm to 2000 rpm with different concentration of PEO of 10.0 to 20.0 g/L.

2.2. AFM and SEM images

Atomic Force Microscopy (AFM) images of the PEO layer were taken on Bruker Dimension 3100 SPM with Electronic Nanoscope 5 Microscope used in peak force quantitative non-mechanical mode with SCANASYST tip (Silicon Nitride). Lamellar like polymer structures were observed in the topographic image as in **Figure 2. 8** with PEO with 17.5 g/L concentration deposited on Si/SiO_2 substrate with spin speed of 750 rpm.

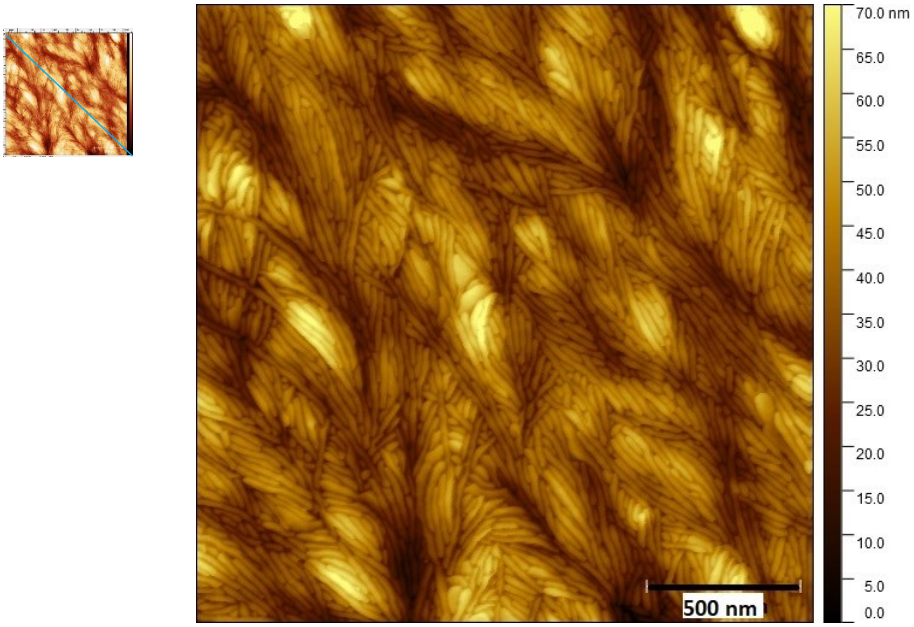

Figure 2. 8 Topographic AFM image of PEO thin film (~150 nm), deposited with 17.5 g/L PEO solution with spin speed of 750 rpm on Si/SiO_2 substrate; (inset) shows the section across which the RMS roughness is measured.

These fibril like PEO images are in correspondence to that presented by Krishnan *et al.* **[10]**.

Table 2. 2 presents the root mean square (RMS) roughness values corresponding to the PEO concentration & spin speeds. The values measured showed high roughness over a section of ~2.8 µm considering the maximum device cross section up to 100 µm.

PEO Concentration (g/L)	Spin speed (rpm)	R.M.S. Roughness (nm)
15.0	750	53
17.5	750	49
17.5	1250	50

Table 2. 2 Shows the RMS roughness values corresponding to spin speeds and PEO concentration.

Image in **Figure 2. 8** confirmed the deposition of PEO layer and hence, further steps for fabrication can be carried out. Scanning Electron Microscopy (SEM) images were also taken on Mira Tescan in backscattered mode with 5 kV voltage. Here, the SEM image is taken of 139-149 nm thick PEO layer. As seen in **Figure 2. 9** there are similar fibril like structures of the PEO polymer layer observed as in with AFM image.

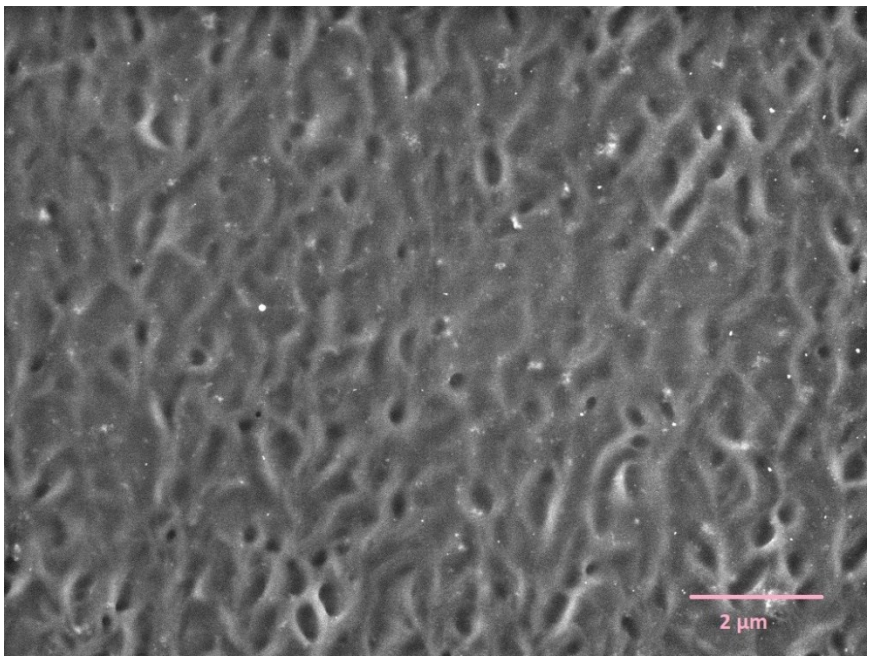

Figure 2. 9 SEM image (top view) of PEO layer deposited on Si/SiO_2.

Cross sectional SEM images were done on the deposited PEO layer, by cleaving Si/SiO_2 layer with a diamond tip pen with the same microscope on devices with 5 kV voltage and SEM magnification of 151kx. As seen in **Figure 2. 10** , the three layers- Si (750 µm), SiO_2 (500 nm) and the deposited PEO layer (140 nm) can be observed. It is conclusive from the AFM and SEM images that PEO is deposited successfully on the Si/SiO_2.

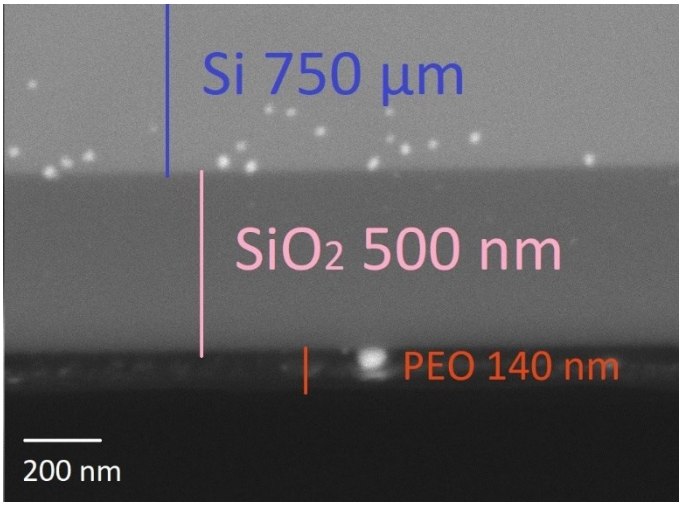

Figure 2. 10 SEM image on the cross section of vertical devices showing Si/SiO_2/PEO layer.

3. Fabrication of CBRAM devices

Two types of devices - vertical and lateral devices - were fabricated and studied in this work. Vertical devices correspond to traditional devices where all the layers (top/bottom electrodes and polymer layer) are vertically stacked, in this case the solid electrolyte layer thickness is controlled by the spin coating conditions. As explained in the following, lateral devices exploits a shading effect during evaporation of the second metallic electrode to produce a nano-gap in between the electrodes. Therefore, the virtual thickness of our solid electrolyte is independent from the deposited PEO thickness and is dictated by the nanogap length. The silicon substrate consists of Si/SiO_2 with 750 µm/500 nm respectively while kapton 125 µm was employed as flexible substrate.

3.1. Polymer based CBRAM devices on Silicon substrates

3.1.a. Vertical devices

The complete fabrication process is schematically illustrated in **Figure 2. 11**. In the present work, Platinum (Pt) is used as the bottom inert electrode, while Ag is used as top

active electrode and the solid polymer electrolyte (SPE) layer is PEO obtained by spin coating. Shadow masks used for electrode deposition and are detailed in **Appendix D**.

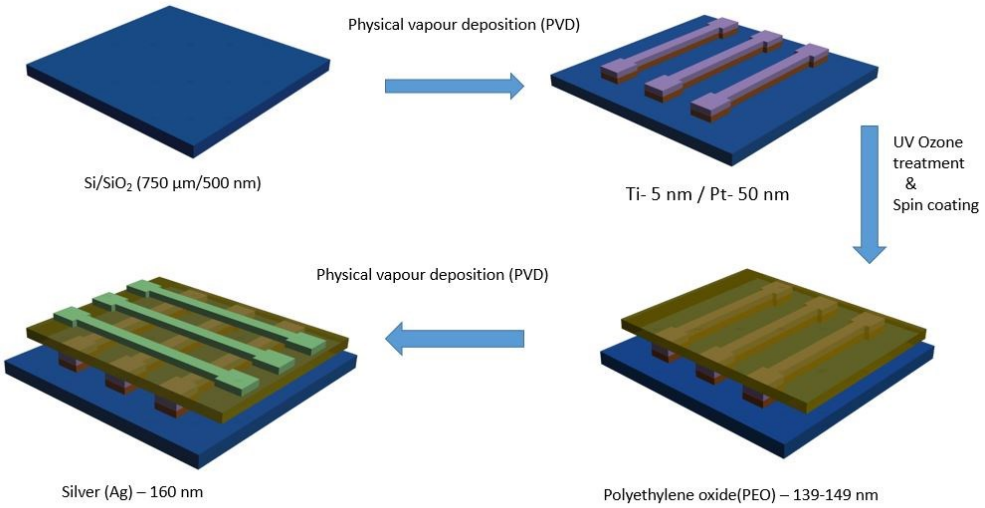

Figure 2. 11 Fabrication procedure for PEO based CBRAM devices.

- **Substrate preparation and bottom electrode deposition**

A Si-SiO_2 substrate with a thickness of Si 750 µm and SiO_2 500 nm is used. Two different masks with mask sizes 25 µm, 35 µm, 50 µm and 100 µm are used to fabricate the memory devices. Firstly, the substrate is dried with N_2 gas and thereafter, the adhesive layer Titanium (5 nm) and bottom Platinum (50 nm) electrode are deposited using the physical vapour deposition method with Edwards FL 400 e-beam evaporator. During the deposition of Platinum (Pt), the temperature of the chamber increases to 120°C, hence a controlled deposition of Pt is needed.

In the next step, the bottom electrode with the substrate is cleaned with Iso-propyl-alcohol (IPA), Ethanol and Acetone and again dried with N_2. UV-Ozone treatment of the surface is performed for 20 minutes with UVO cleaner (Model number 42A-220).

- **Solid Polymer Electrolyte layer deposition**

The PEO layer is deposited with spin coating parameters of speed 750 rpm, acceleration 1000 rpm/s and time duration 60 seconds is used to deposit the PEO with 17.5

g/L concentration and dried in a vacuum drier at 80°C for 20 hours. The spin coating conditions as described in the **section 2.1.** of this chapter are selected to obtain a specific thickness of PEO layer with an expected value between 130 and 50 nm.

- **Top electrode deposition**

The top electrode silver (Ag) is deposited by electron beam evaporation method with Alcatel equipment. The targeted thickness of Ag is 150 nm. **Figure 2. 12** shows the fabricated devices with mask 1 **(in Appendix D)** with MIM cross bars of 25 µm, 50 µm and 100 µm. The vertical lines show the bottom inert electrode (Pt) and in horizontal line top active electrode (Ag).

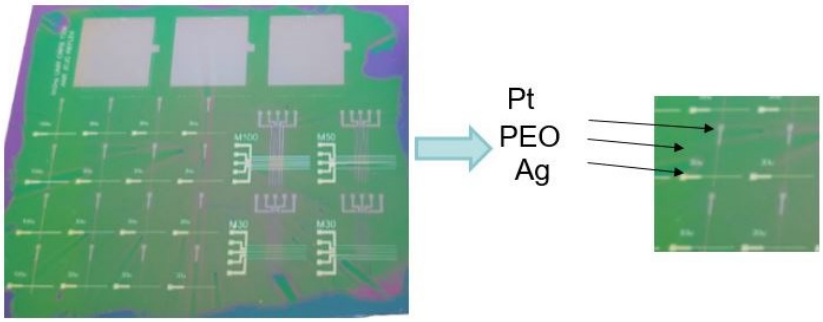

Figure 2. 12 Fabricated devices on Si/SiO_2 with bottom electrode (Pt), top electrode (Ag) and PEO layer.

3.1.b. Planar devices

As mentioned earlier, planar devices featuring a thickness with ~ 100 nm gap between the active and inert electrodes were fabricated. These structures were initially developed at INL during the PhD thesis of Daniel Thomas for Single Electron Transistors (SET) fabrication **[16]**. As detailed in **Chapter 4**, these devices were studied as they interestingly provide a direct access for doing physical/chemical analysis in the active region where the conductive(s) filament(s) are formed. For planar structures, the shadow edge evaporation technique **[16]–[18][19]**, which is a two-step patterning/evaporation process is employed. This process wide range in the material and patterning choices.

A first electrode, which can be patterned and deposited with any chosen method, is used to form a small shadow by tilting it, for depositing the second electrode. Here, the

planar structures have been realized using optical lithography and simple e-beam evaporation techniques. **Figure 2. 13** shows the schematic representation of the shadow edge technique. In order to get a planar nanogap, two successive evaporations are performed. In the first instance, a zero angle evaporation for the first electrode which is Ag- 100 nm thick, and then an oblique angle evaporation for the second one (Pd thickness 30 nm). The two parameters in which the nano-gap size depends- are i) the thickness of the first electrode and ii) on the value of the angle used for the second evaporation.

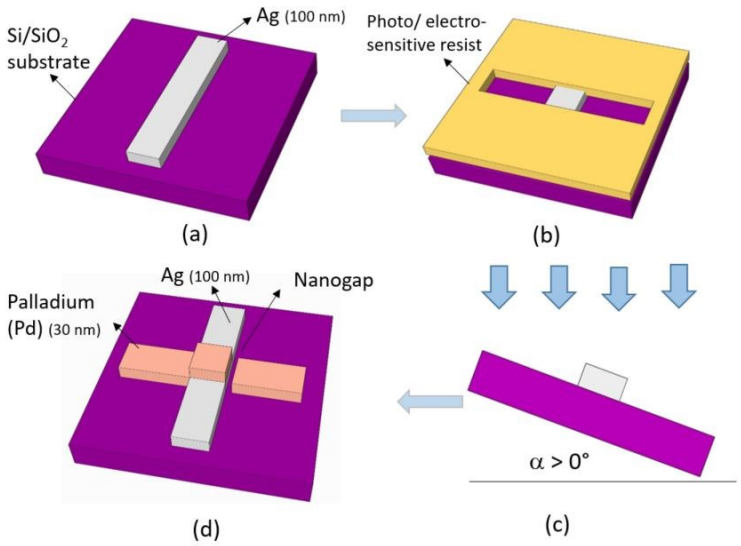

Figure 2. 13 Shows the stepwise fabrication of planar devices. Firstly, (a)-(b) the bottom electrode (Ag) is deposited and (c) then second layer of electrode (Pd) is deposited with oblique angle evaporation technique so as to form (d) a nano-gap.

Figure 2. 14 is a schematic representation of the cross section of the planar nano-gap device. With spin coating parameters of -spin speed 750 rpm, spin time 60 seconds and acceleration 1000 rpm/sec, PEO layer is deposited. In this case Palladium (Pd), also an inert material, was used instead of Platinum as inert electrode because the fabrication of planar devices with Pd has already been developed and optimized by our group (*i.e.* during the PhD thesis of Daniel Thomas).

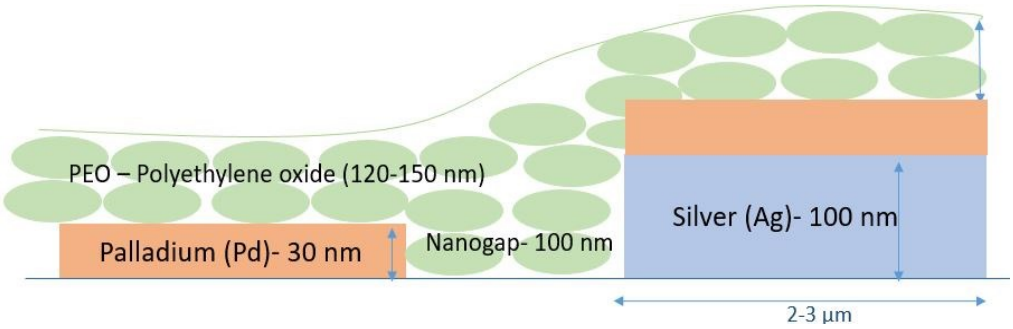

Figure 2. 14 Illustrates the cross sectional view of the planar devices, showing the inert electrode (Pd), nano gap, active electrode (Ag) and the solid polymer electrolyte layer- PEO

Micrographs are taken of the planar nano-gap structures as shown in **Figure 2. 15**. **Figure 2. 16** presents the fabricated planar devices with different widths of Pd contact electrode -2 ,4, 8, 16 µm.

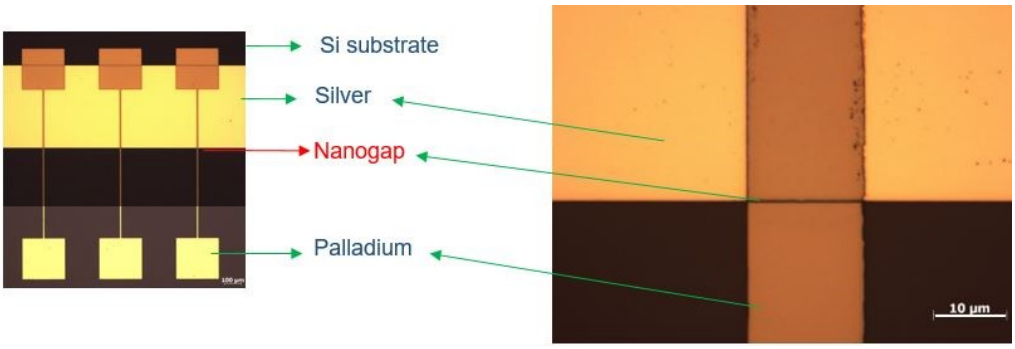

Figure 2. 15 Micrographs of the planar devices with top electrode – Palladium, nanogap and bottom active electrode – Silver on Si substrate.

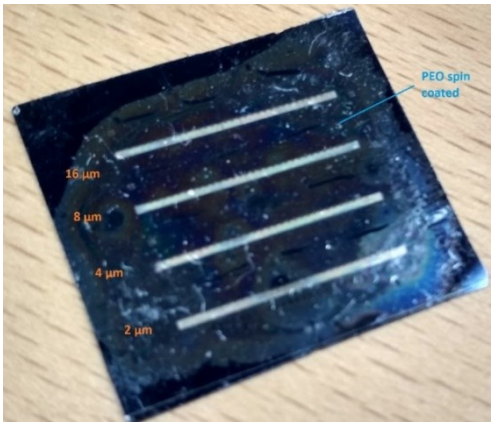

Figure 2. 16 Fabricated planar devices with four different (Pd) electrode thickness – 2 µm, 4 µm, 8 µm in four different rows with PEO layer spin coated throughout the substrate

Figure 2. 17 shows the SEM image of the electrodes with Pd, Ag and the nanogap on Si/SiO_2 with the nanogap around 100 nm as shown in **Figure 2. 18** .

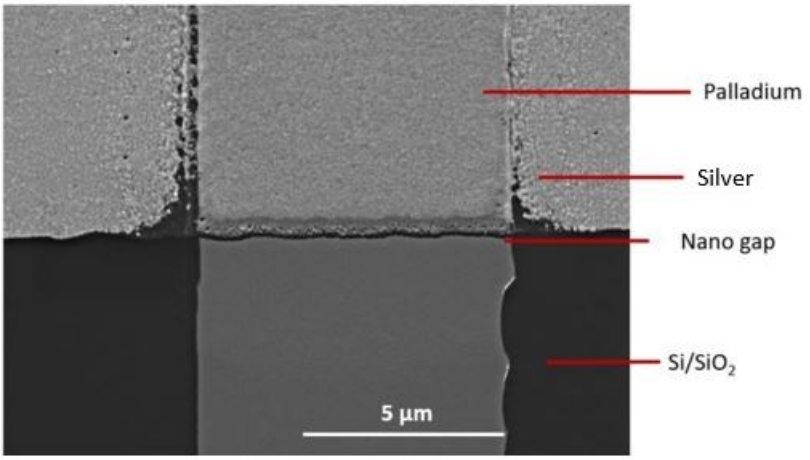

Figure 2. 17 SEM image of a device showing the inert electrode (Pd), active electrode (Ag) and Nano gap ~100 nm formed by shadow edge evaporation technique on Si/SiO_2 substrate.

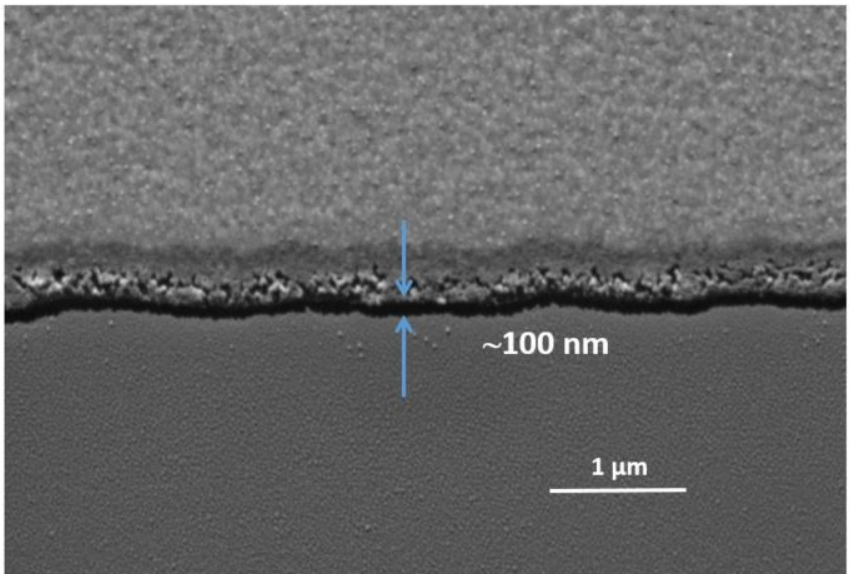

Figure 2. 18 Nano-gap on a planar device (~100 nm) realized using optical lithography and e-beam evaporation techniques.

3.2. Polymer based CBRAM devices on flexible substrates

A flexible kapton substrate (ADDEVMATERIALS- insulation & films) is taken with a thickness of 125 µm for fabrication of CBRAMs. Kapton is chosen as flexible substrate because of its properties of thermal stability, electrical insulation, resistance to chemicals, mechanical and radiation resistance **[20]**. It is then cleaned with dry N_2 gas and the adhesive layer Ti (5 nm) and bottom electrode Pt (50 nm) with physical vapour deposited. After this, with Isopropyl alcohol (IPA), acetone, ethanol and dry N_2 gas is used to clean the substrate and then UV ozone treatment is done for 20 minutes. With PEO M_w 600 000 g/mol and concentration 20 g/L is used to spin coat the solid polymer electrolyte layer of 140-160 nm using the spin coating parameters of : spin speed - 750 rpm, spin time 60 seconds and vacuum drying time of 20 h at 80°C. In the next step the top electrode (Ag) 150 nm thick is physical vapour deposited.

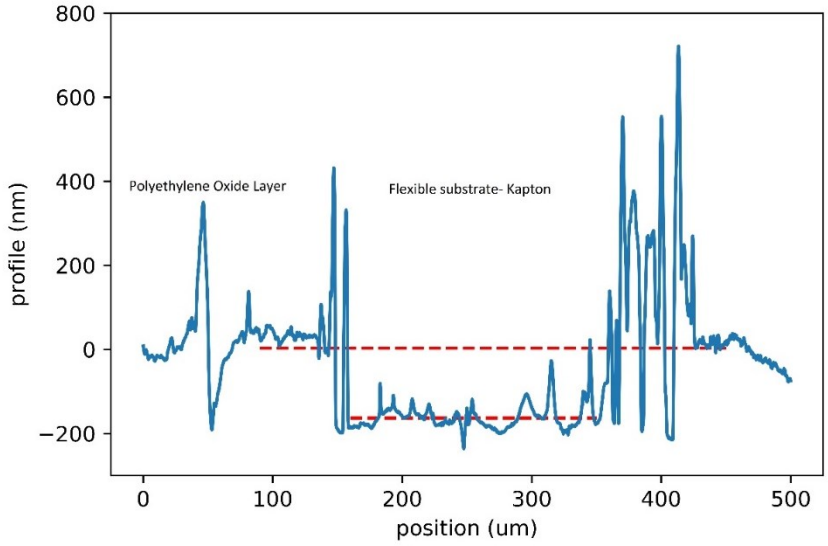

Figure 2. 19 Thickness profile of the indentation made on the solid polymer electrolyte layer- thickness 140-160 nm deposited on flexible substrate.

Figure 2. 19 presents the thickness profile of the solid polymer electrolyte layer (SPE) measured with the profilometer after making an indentation on the substrate. **Figure 2. 20** & **Figure 2. 21** illustrates schematically the fabrication process of the flexible CBRAMs and the finally fabricated device respectively.

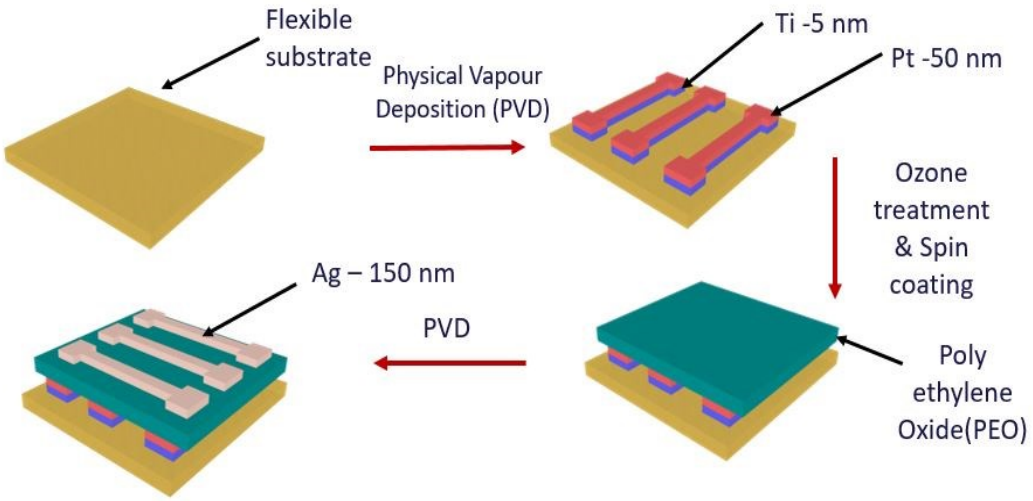

Figure 2. 20 Description of the fabrication process for memory devices on flexible substrate.

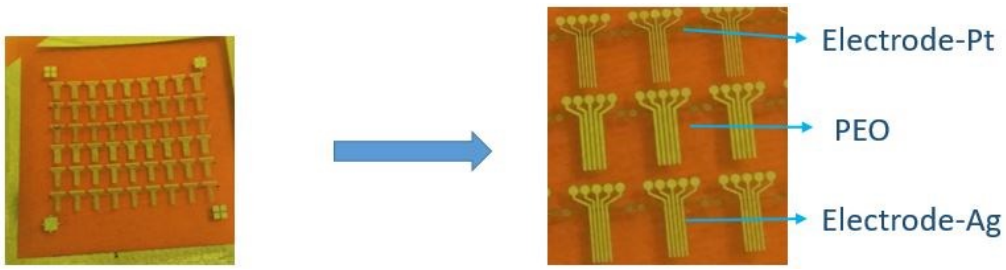

Figure 2. 21 Fabricated devices on flexible substrate showing the bottom electrode (Pt), PEO layer and top electrode (Ag).

4. Conclusion to the chapter

This chapter focusses on the preparation of the Polyethylene Oxide (PEO) solid polymer electrolyte layer and the fabrication of the CBRAM devices on silicon and flexible substrate. In the first section of the chapter, the properties of the PEO are presented, along with the detailed procedure to prepare PEO solutions for spin coating. Analysis of the PEO layer is done with Differential Scanning calorimetry (DSC).

It is then demonstrated that by varying spin coating parameters, the thickness of the PEO layer can be varied from 25 nm upto 225 nm. The morphological observation of the PEO layer is done through AFM/SEM images on the vertical and planar devices, confirming its deposition.

In the final section of the chapter, the complete fabrication procedure of the CBRAM devices is described, either on silicon and flexible substrates. On silicon substrates, both vertical and planar structures were fabricated. Vertical devices will be electrically characterized in the next chapter while planar devices will be studied in Chapter 4.

5. References

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APPENDIX A : DSC Measurements

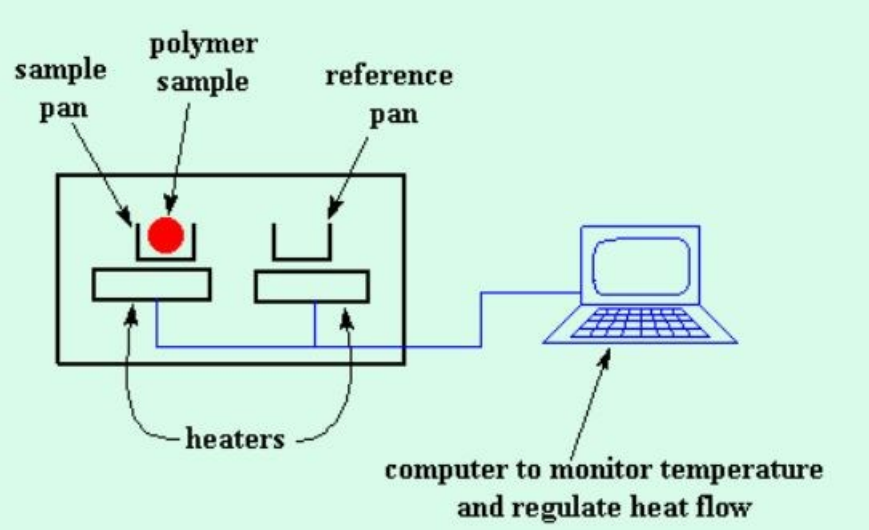


Figure A. 1 Schematically presents a setup of DSC measurements

Differential Scanning Calorimetry technique uses two pans- one with the sample and other reference (empty) to measure the heat flow in the device. In our case we use aluminim pans as thin film polymers are analysed in this case. They are placed on heaters which are heated at constant rate (10°C/min) and consequently, heat flow vrs temperature recordings are taken within a set range of temperature (-70° C to 150° C). In this case the DSC plot is an Exothermic up plot. **Figure A. 1** depicts the setup schematically **[21]**.

Surface area calculation for a 150 nm thin PEO film

On computing with the parameters of PEO, density (ρ) as $1.2x10^6$ g/m^3 and calculating the surface area required for DSC measurements is calculated for 150 nm thin film. From the equation

$$Area = \frac{Volume}{Thickness} = 135\ mm\ x135\ mm \quad for\ Thickness = 150\ nm$$

So, the size 13.5 cm x13.5 cm standing films of 150 nm thin PEO has to be deposited for DSC measurements which is not feasible.

APPENDIX B : XRD Measurements

XRD measurements are based on the constructive interference of the monochromatic X-rays and crystalline sample, satifying Bragg's law ($n\lambda = 2\ d \sin\theta$) where n is integer, λ wavelength of radiation, θ angle of diffraction and d lattice spacing in the crystalline sample. Through these measurements we try to quantify the degree of crystallinity on our films, however not successful. With X-ray Powder diffractometer consisting of an X ray tube, sample holder and an X ray detector, of x-ray radiations (alpha) $CuK_{\alpha 1}$ used are 1.5406°A is used projected on the sample. Meanwhile, as the sample and detector are rotated, the reflected X-rays are recorded. In this way, whenever the impinging X-rays satisfies the Bragg's law, it results into a constructive interference, and therefore a peak of intensity occurs. The detector placed, rotates at an angle 2θ and records this X-ray signal, and converts it into a count rate. The instrument used to maintain the angle and rotate the sample is termed as gonimeter.**Figure B. 1** & **Figure B. 2** presents the XRD setup and instrument respectively**[22]**.

The main principle of XRD is based on the constructive interference of monochromatic X-rays with the sample.

The purpose of X-Ray Diffraction measurements were two folds:

i) To verify the semi-crystalline nature of the polymer (PEO) and

ii) To get an approximation of the crystallite size of the Polyethylene oxide thick and thin films.

We used the Scherrer's equation (equation 1) in order to find the crystallite size of the PEO **[23]**.

$$\text{Crystallite size D (Å)} = \frac{K\lambda}{B\cos\theta} \qquad (1)$$

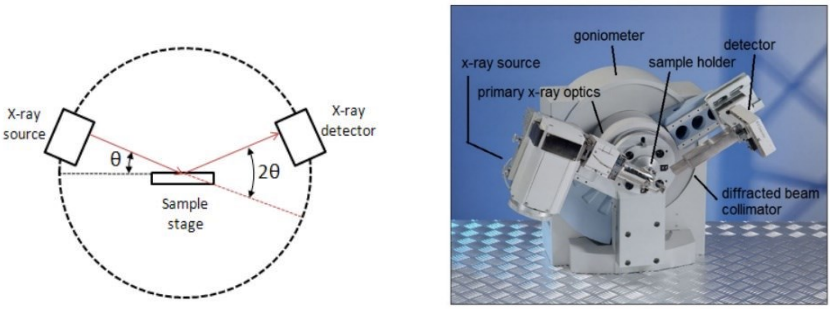


Figure B. 1 Shows the schematically setup and instrument of of X-ray powder diffractometer with X ray source, sample holder and detector respectively. (Courtesy of Malvern-PANalytical B.V.)

Where λ is the wavelength of x ray radiation in Å, K is the shape factor which is dimensionless, and B the full width at half maximum (FWHM) in radians. Generally, the value of K is taken as 0.90 **[22]**. The wavelength of x-ray radiations (alpha) $CuK_{\alpha}1$ used are 1.5406 Å. The plot of intensity (counts) versus angle (2θ) showed in **Figure B. 3** with peaks at 19.17°, 23.31° and 23.48°. These crystalline peaks of PEO originate from the ordering of polyether side chains and strong intermolecular interaction between PEO chains through hydrogen bonding**[24], [25][26]**. Total run time for the experiment was 1 hour 52 minutes. The 2 θ, d spacing values were calculated from the software as shown in the

Table B. 1.

Figure B. 2 Bruker's X-ray Diffraction D8-Discover instrument

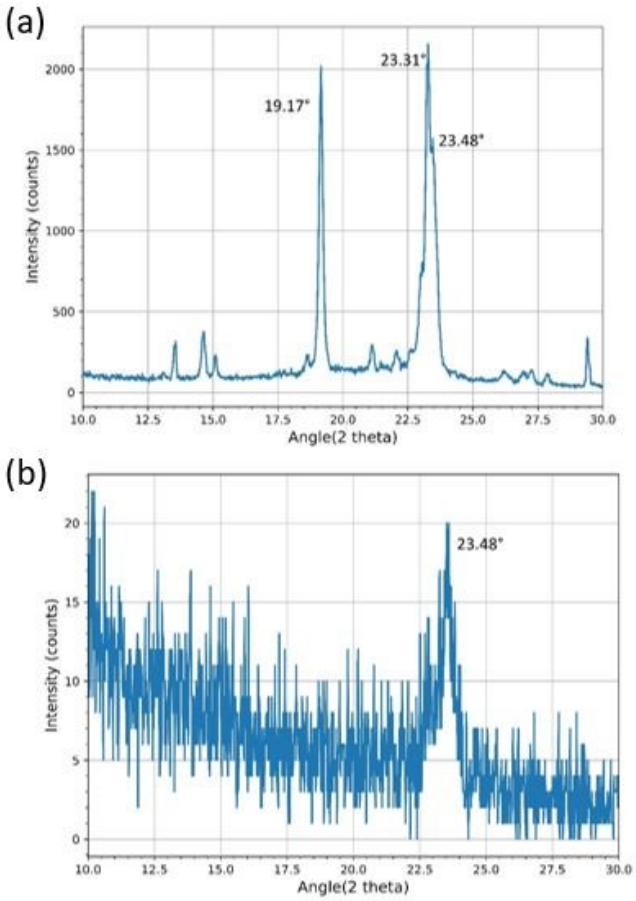


Figure B. 3 X-ray diffraction spectrum of (a) PEO 18 µm thick films (b) on thin films (150 nm).

2 θ (°)	**d(Å)**	**h,k, l**
19.17	4.625	1 2 0
23.31	3.81	0 3 2 1 3 -1
23.48	3.78	1 3 -2 2 1 -2

Table B. 1 The values of d-spacing, h, k, l corresponding 2θ values.

From the values extracted from the

Table B. 1 the crystallite size (D) was 49.5 Å with FityK software. The crystallite size depends on the thickness of the film PEO and the fabrication conditions **[23], [25], [26]** . Similarly, XRD characterization measurements were done on thin 150-nm thick PEO films on Si/SiO_2.

As seen in **Figure B. 3** as the spectrum shows the intensity peak for thin 150 nm at 23.48°. This absorption peak is not dependable for quantification of crystallite size or crystallinity. The following two reasons for it- firstly, its low intensity obtained due to the thin films to be characterized on ~150 nm thin film, its intensity peak is not reliable as it is not clearly differentiable with that of noise. Secondly, as the XRD spectrum is obtained in reflection and rather than transmission mode which is a pre-requisite of quantification of crystallinity **[27][28]**.

APPENDIX C : FTIR Measurements

Fourier Transform Infrared (FT-IR) spectroscopy is used to measure how much light a sample absorbs at each wavelength in the IR region. Appendix presents the working principle of FTIR measurements.

Since crystallinity was not quantifiable with XRD measurements Fourier Transform Infrared Spectroscopy (FTIR) measurements were performed on the thin films. Firstly, we needed to identify all the vibrational modes of Polyethylene oxide (PEO) through the FTIR spectra obtained and relating it with that in the literature. Further, the corresponding amorphous and crystalline regions in the spectra are identified. Thermal treatment is performed on the sample to visualize changes in the spectra and finally crystallinity ratio is calculated.

Experimental setup & results

The The FTIR spectroscopy was done with Nicolet iS10 **Figure C. 1** and analysed with the OMNIC software. To identify the PEO vibrational modes on the thick films of PEO were placed at the sample slot and FTIR measurement is performed in transmission mode with 32 scans. This spectrum shows peaks corresponding to PEO vibrational bonds as presented in **Figure C. 2.** After this, FTIR measurement of just the Si/SiO_2/PEO and Si/SiO_2. Thereafter, the FTIR spectra of PEO is extracted from subtracting the latter spectroscopy plot from the former one by setting the baseline for each of the spectra individually and in the OMNIC software. **Figure C. 3** shows the result of the spectroscopy of the Si/SiO_2/PEO. As the PEO layer thickness is 150 nm, the vibrational modes of all the PEO composition is not evident. **Table C. 1** shows the vibrational modes of PEO from the literature **[29]**. On comparison of the obtained spectra and the spectra in the literature, the vibration modes are identified **[30]**.

Table C. 2 lists the peaks obtained experimentally on the thick 18 μm films. With so low intensity peaks due to thin films, it is not possible to measure crystallinity ratio with this

technique. However, it can be concluded rom the FTIR spectroscopy measurements that Polyethylene oxide (PEO) film is confirmed.

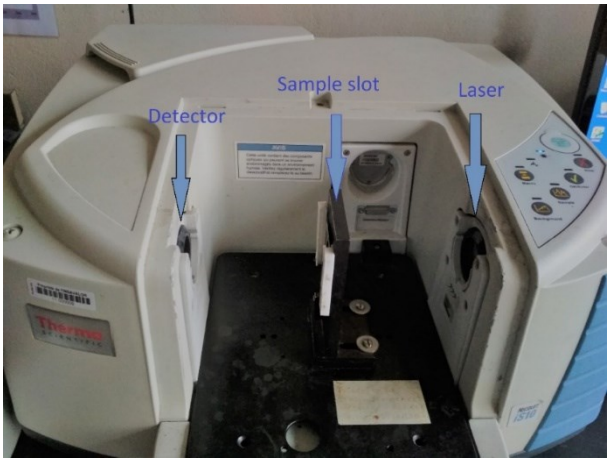


Figure C. 1 Nicolet iS5 FT-IR spectroscopy instrument showing the laser, sample slot and detector.

CH stretching 3000–2650	Overlap∥ and ⊥ vibrations	$\varepsilon\parallel \approx \varepsilon \perp$
CH bending 1500-1400	1470: ∥ 1463: ⊥	$\varepsilon\parallel \approx \varepsilon \perp$
CH_2 wagging/twisting	1343: ∥ 1359:⊥	$\varepsilon\parallel > \varepsilon \perp$
CH_2 wagging/twisting	1280 ⊥	$\varepsilon\parallel < \varepsilon \perp$
CH_2, CO rocking/stretching	1241: ∥ 1235 ⊥	$\varepsilon\parallel > \varepsilon \perp$
CH_2, CO rocking/stretching	Overlap ∥ and ⊥ 1200–990	$\varepsilon\parallel \approx \varepsilon \perp$
CH_2 rocking CO stretching	1060 ⊥	$\varepsilon\parallel < \varepsilon \perp$
CH_2 rocking CO stretching	963: ∥ 947: ⊥	$\varepsilon\parallel > \varepsilon \perp$
CO/CH_2 rocking/stretching	844: ⊥	$\varepsilon\parallel < \varepsilon \perp$

Table C. 1 Lists all the vibrational modes of Polyethylene oxide (PEO).

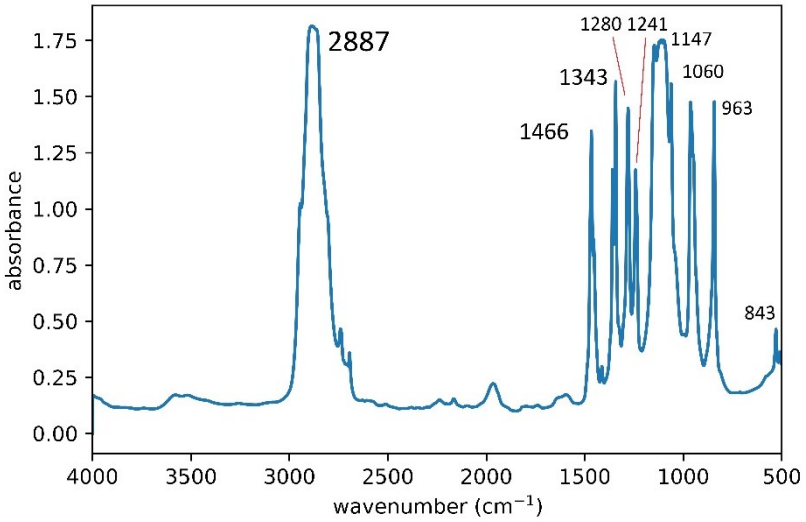


Figure C. 2 FT-IR spectra observed on 18 µm thick PEO films to identify the characteristic vibrational modes.

Peaks (cm^{-1})	Vibrational mode
2887	CH ν in O-CH_2 groups
1466	CH bending
1343	CH_2 wagging/twisting
1280	CH_2wagging/twisting
1241	CH_2, CO rocking/stretching
1147	CH_2, CO rocking/stretching
1060	CH_2 rocking CO stretching
963	CH_2 rocking CO stretching
843	CO/CH_2 rocking/ stretching

Table C. 2 Shows the peaks corresponding vibrational modes obtained experimentally from FTIR spectroscopy of 18 µm thick films.

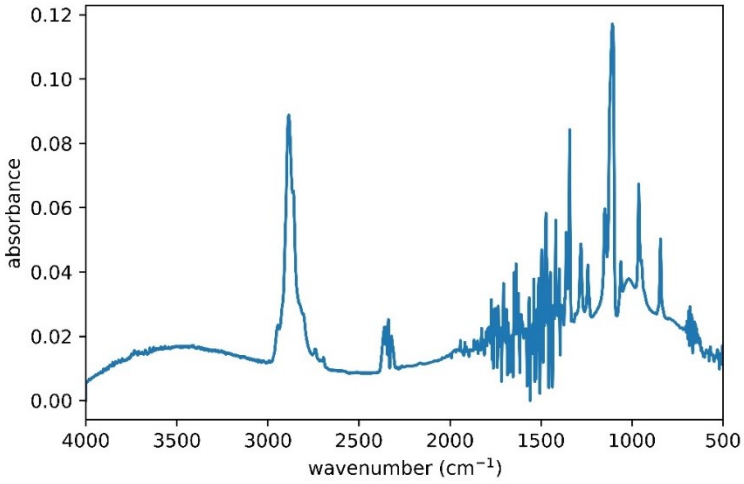


Figure C. 3 FT-IR spectra of Si/SiO_2 (175 µm/500 nm) substrate with 150 nm of PEO layer performed in transmission mode.

APPENDIX D : Shadow Masks

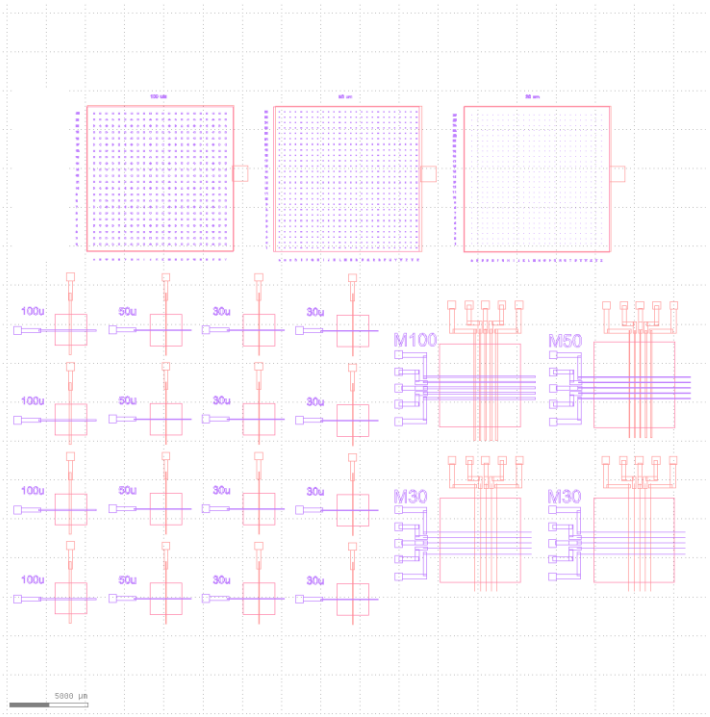


Figure D. 1 Design of Mask 1 (square devices)

Individual cross bar devices (d) :

30um*30um. ->8 d

50um*50um. -> 4 d

100um*100um -> 4 d

5*5 cross bar arrays:

100um ->1 array

50um ->1 array

30um ->2 arrays

22*22 square capacitors:

100um

50um

30um

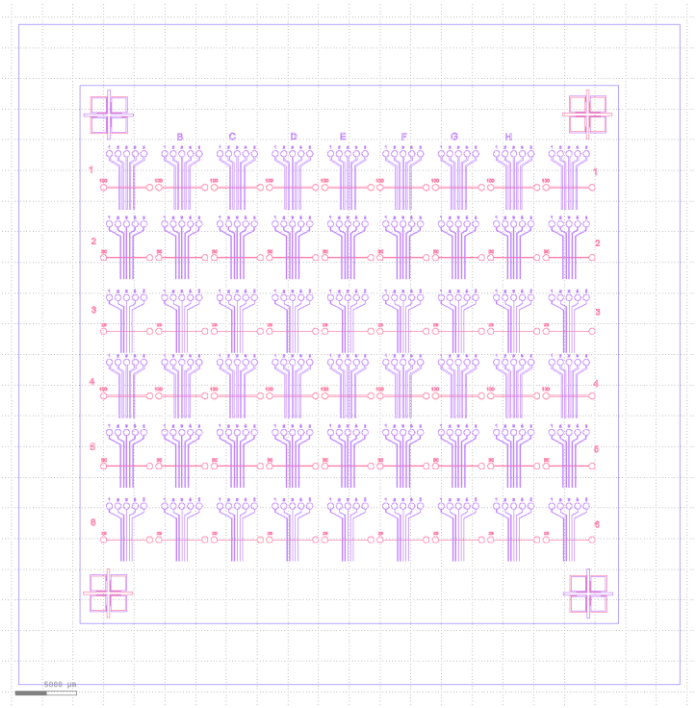


Figure D. 2 Design of Mask 2 (mini crossbar)

5x1 cross bar rows (2 series of 9 devices)

->18*5 = 90 devices of each

lines: 100um – 50um – 35um

Chapter 3 – Electrical characterization and analysis of vertical CBRAM devices

In this chapter, the electrical performances of the vertical CBRAM devices are presented. In the first section, we evidence the effect of electrodes and voltage polarity on resistance switching, confirming that our devices are controlled by CBRAM-type switching. In the second section, the electrical performances are presented at various current compliance (CC) values. Besides electrical variability, the influence of CC on programming voltage, resistance distribution and retention time is presented.

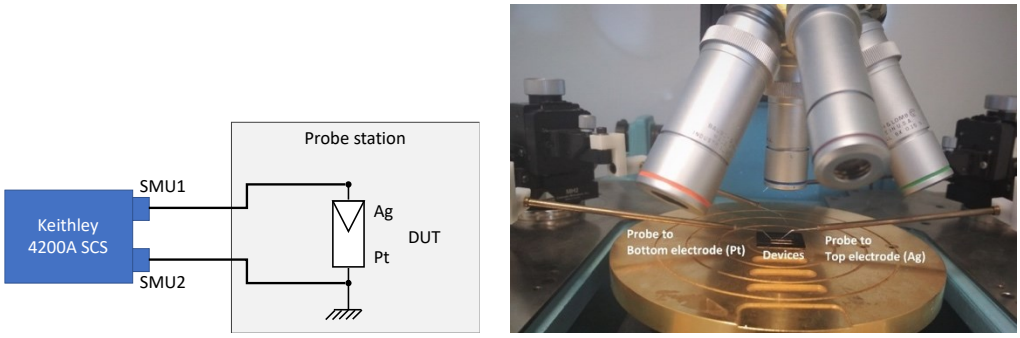
In the third section, we expose an analysis of conduction mechanisms of our devices. After investigating a reference Pt/PEO/Pt device at various temperature, an analysis of conduction mechanisms of CBRAM devices at both Low and High Resistance States is conducted.

1. Evidence of CBRAM-type switching

In this section, we first describe the experimental setup. We then compare the electrical characteristics obtained on both reference and memory devices and check the effect of voltage polarity on resistance switching. It is shown that resistance switching is in full agreement with the formation/dissolution of an Ag-rich conductive filament originated from the active Ag electrode rather than an intrinsic switching property of the polymer layer. It is also been observed that a critical thickness of the Polyethylene oxide (PEO) layer is important for working CBRAMs.

1.1. Experimental setup

Electrical characterization were performed on a probe station equipped with a Keithley 4200A SCS parameter analyzer **[1]**. One of the probes is connected to the bottom Platinum (Pt) electrode, which is grounded, while the other is connected to the top Silver (Ag) electrode to apply voltage sweeps. Since the polymer layer covers the whole sample, including bottom electrodes, a scratch has to be made through the PEO layer to contact the bottom electrode Platinum (Pt). The connection to the Keithley 4200A SCS is made through the source-measure units (SMUs). The setup is depicted in **Figure 3. 1** .



(a) (b)

Figure 3. 1 (a) Scheme of the measurement setup. (b) The devices under test (DUT) with the electrodes in contact with the probes shown in the probe station.

Throughout our studies, quasi-static (DC) IV characteristics were performed on the devices. A positive linear voltage dual sweep with a step of 0.01 V is applied up to +2.0 V for set process, whereas for reset a negative linear voltage sweep is applied up to -1.5 V for reset process. The compliance current (CC) for the set process is was varied from 10.0 µA to 1.0 mA. CC is the maximum current value which is allowed to flow through the devices to prevent it from breakdown [see **Figure 3. 2**]. In our case it is set manually.

1.2. Evidencing the role of electrodes and voltage polarity

Figure 3. 2 shows the current-voltage characteristics obtained on both, a Pt/PEO/Pt reference device and a Ag/PEO/Pt device. Both PEO layers have the same thickness of about 150 nm. It is confirmed that an Ag active electrode is necessary for switching; while the Pt/PEO/Pt reference device exhibits a symmetric I-V characteristic during the positive voltage sweep, a sudden jump up to the current compliance level is observed at 1.4 V on the Ag/PEO/Pt device during the positive voltage sweep. Conversely, sudden drop of current at -0.5 V drives the current back to its initial value. Although, reference devices where subjected to larger voltage amplitude (±5V), such switching effects were not observed. Within the voltage bias range employed in this work, polyethylene oxide (PEO) did not exhibit intrinsic switching characteristic. Hence, the set/reset switching observed in Ag/PEO/Pt devices is in agreement with the literature showing Ag dendrites observed on PEO based CBRAMs in the SEM images **[2]**.

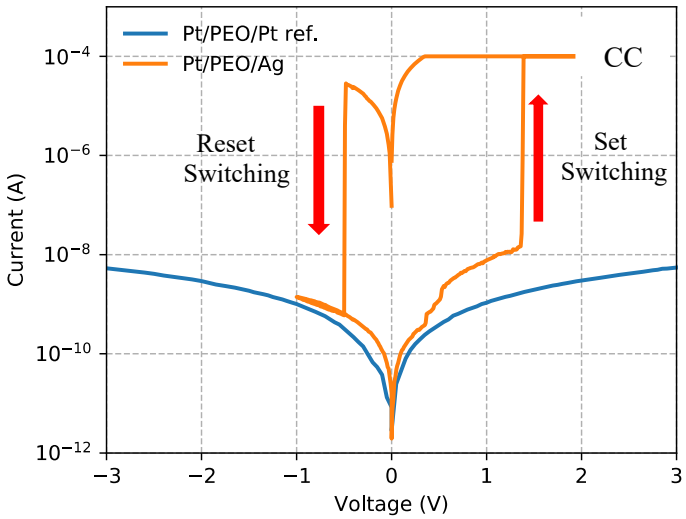


Figure 3. 2 Comparison of IV characteristics of a Pt/PEO/Ag CBRAM and a reference device featuring Pt top and bottom electrodes. The Ag electrode promotes resistance switching.

Moreover, to confirm that set (*resp.* reset) only occurs as a positive voltage bias (*i.e.* with respect to the active Ag electrode, Pt is the grounded electrode) while reset require a voltage bias of reversed polarity, five pristine memory devices were subjected successively to a negative unipolar voltage sweep followed by a positive one. As demonstrated in **Figure 3. 3** the set switching was solely observed on the application of a positive voltage bias on the Ag electrode. In conjunction with the role played by the Ag electrode [**Figure 3. 2**], this result is in line with resistance switching controlled by the growth/dissolution of an Ag-rich filament through the PEO layer as exposed in other research works based on Polyethylene oxide**[2]–[4][5], [6]**.

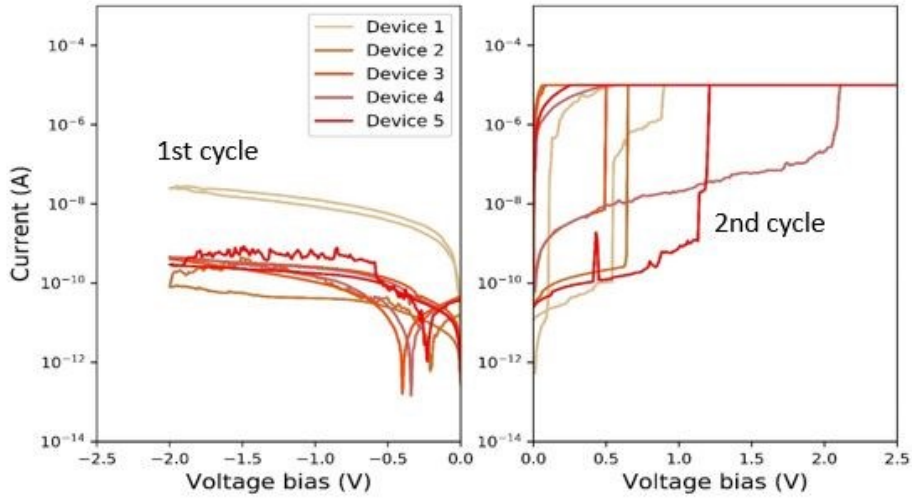
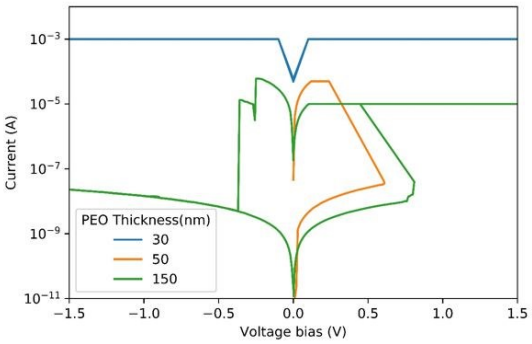


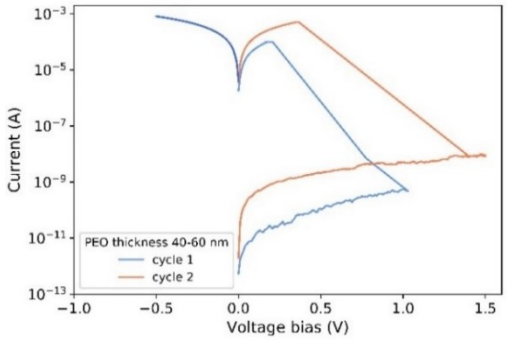
Figure 3. 3 IV characteristics of five pristine devices, firstly subjected to negative bias (on the left) and then positive bias (on the right).

1.3. Effect of PEO thickness

We compared the IV characteristics of devices with different PEO thickness. As seen in **Figure 3. 4** the devices with 30 nm PEO thickness were systematically short-circuited, while devices with 50 nm-thick PEO exhibited set switching. Moreover, it should be mentioned that 50 nm PEO thick devices showed either no reset or mostly short-circuited, after the first resistance switching [see **Figure 3. 4**].A possible reason for such phenomenon could be related to a diffusion of Ag through the thin PEO layer during e-beam evaporation. Only devices with a 150 nm-thick PEO layer were able to switch in a reversible manner between high and low resistance states. Therefore, in the following only 150 nm-thick PEO devices were studied.



(a)



(b)

Figure 3. 4 IV characteristics with (a) devices with different PEO thickness of 30, 50, 150 nm, (b) a device with 50 nm showing cycle 1 & 2.

2. Electrical performance of the devices

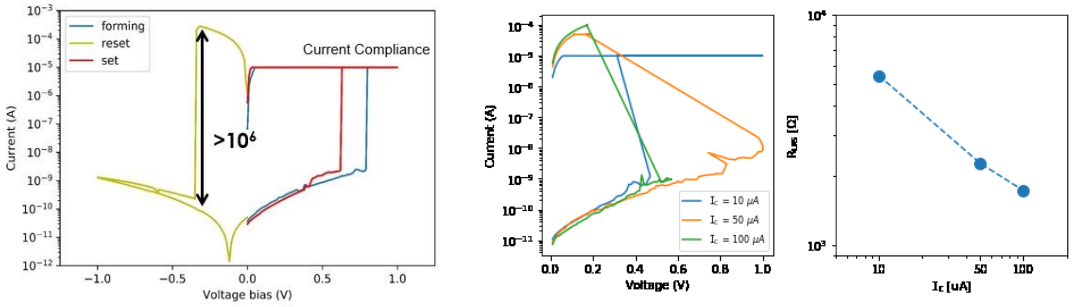
In this section, we first evidence the effect of current compliance (CC) on the memory window. Then a statistical analysis of the effect of CC during endurance cycles is presented: evolution of memory window, programming voltage. Finally, retention properties were investigated. Measurements reported in this section were obtained on Ag/PEO/Pt device featuring a 150 nm-thick PEO and an area of 30 x 30 μm^2.

The forming cycle is defined as the first cycle which is performed on the pristine state of the device. It is the first time, the filament(s) is (are) are formed, unlike in the subsequent cycles were only the weak part of the filament breaks, hence the forming cycle is generally achieved at a higher voltage than the subsequent cycles performed on the device. This is evidenced on the characterization of the devices as shown in **Figure 3. 5**, where forming is achieved at 0.75 V while the subsequent set is obtained at 0.6 V. However, as

presented later, we would show that set/reset voltages are subjected to large cycle-to-cycle variability.

2.1. Evidence of the effect of compliance current

Moreover, multilevel states are achievable by setting the compliance current at 10 µA, 50 µA, and 100 µA [shown in **Figure 3. 5**]. The devices exhibiting high OFF/ON resistance ratio >10^6 makes them potential candidates for multilevel cells with high memory density.



(a) (b)

Figure 3. 5 (a) The IV characteristics of a vertical device on Si/SiO_2 showing high OFF/ON resistance ratio >10^6 (b) Illustrates multilevel states can be achieved by setting compliance currents at 10 µA, 50 µA, 100 µA respectively, the different resistance states read at 25 mV.

2.2. Cycling at various current compliance

Set/Reset cycles were performed at current compliance levels of 10 and 100 µA. **Figure 3. 6** report the corresponding current-voltage characteristics gathering more than 300 programming cycles per current compliance level. Average I-V curves corresponding to LRS and the HRS states are shown in fluorescent green. These curves were calculated at each voltage step using the following procedure:

$$I_{av}^{LRS,HRS}(V_i) = 10^{\frac{1}{N}\sum_{k=1}^{N}\log[I(V_i)]}$$

Where $I(V_i)$ and $I_{av}^{LRS,HRS}(V_i)$ respectively correspond to the measured and average currents at voltage V_i. We can observe in the **Figure 3. 7** that the set voltages are widespread for device with CC 10 µA compared to 100 µA with reset at low voltages on the backward

sweep. This result is coherent with the work done by Nardi *et al.* that showed that the dependency of the stability of the conductive filament and set voltages on the compliance current **[7]**.

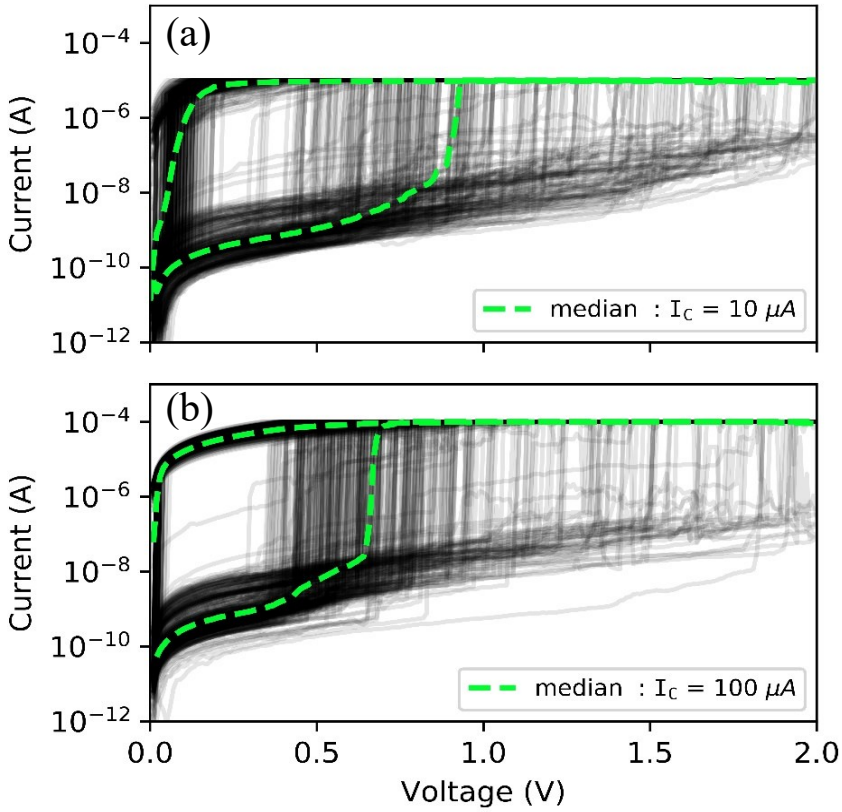
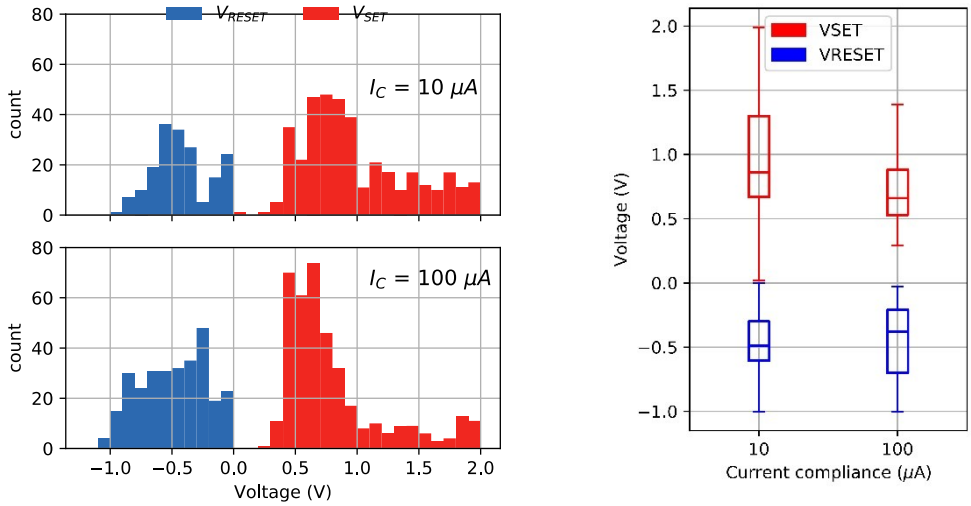


Figure 3. 6 Set cycles with compliance current of (a) 10 µA and (b) 100 µA. LRS and HRS average are computed using log scales.

2.2.a. Impact of compliance current on the programming voltages

Figure 3. 7 show the programming voltage distribution and boxplots respectively. The set voltages on these devices extended up to 2.0 V and for reset down to -1.0 V. It is illustrated that the devices work at low voltages.



(a) (b)

Figure 3. 7(a) Programming voltage distribution and (b) corresponding boxplots for 10 μA 100 μA compliance currents.

Box plots (see **Appendix F**) give a good indication of the variability of the data, in we have presented the data at two compliance currents 10 µA and 100 µA. As CC is increased, it is observed that both set and voltage decreases in absolute value. In addition, the dispersion of set voltages decreases. This can be interpreted as when we have a higher CC the filament radius increases, leading to more incorporation of Ag within the solid electrolyte which may ease successive set operations. The increase of Vreset variability with CC may be then interpreted as the larger filament more difficult to break.

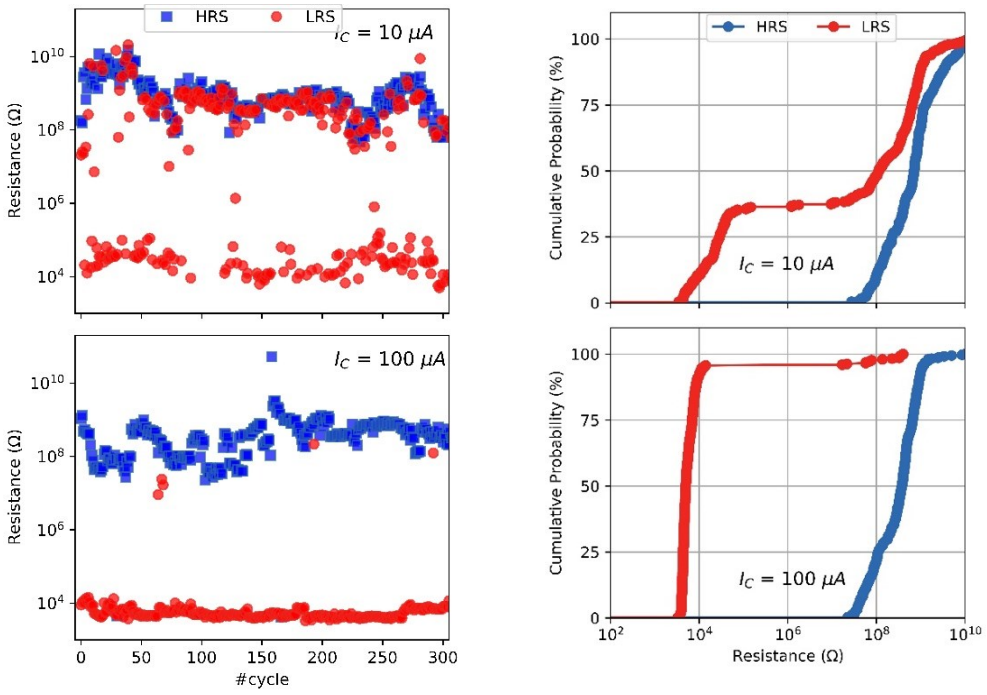
Moreover, it can be noted that the number of reset for 10 µA is less than the number of its corresponding set phenomena. This is due to the fact that lower compliance current causes early breakdown of the filament at low voltages, not requiring a negative bias for a conventional reset to occur. Hence, resulting into volatile switching (which is presented in the later section).

2.2.b. Impact of compliance current on resistance distribution

LRS and HRS resistance values were extracted at a constant voltage of 50 mV for each endurance cycle and both compliance current level. **Figure 3. 8(a)** shows the evolution

of LRS and HRS values along with cycling. In addition, the cumulative distribution function (CDF) of both LRS and HRS is reported in **Figure 3. 8(b)**.

Besides the largest electrical variability observed at lower current compliances, which is in line with the previous results observed on IV curves, the most striking feature concerns the overlap of the LRS/HRS distribution, mostly occurring at a compliance current of 10 µA. As detailed in the next section, this phenomenon is due to frequent occurrences of a volatile-type switching resulting in a spontaneous loss of the LRS as the voltage bias is lowered on the backward positive sweep.



(a) (b)

Figure 3. 8 (a) LRS and HRS along cycling and (b) cumulative distribution function at current compliance levels of 10 and 100 µA.

The large dispersion in the LRS values at a 10 µA CC [see **Figure 3. 8(b)**] accounts for the breakdown of the filament at low voltages. In order to evaluate the impact of compliance current on the LRS/HRS distribution, we have plotted in **Figure 3. 9** the boxplots of LRS/HRS distribution restricted to non-volatile switchings. The selection of data has been made by keeping only resistance switchings for which LRS measured at 50 mV resulted in a value greater than a threshold resistance equal to 1MΩ. This value has been chosen as a representative threshold value from the CDF of **Figure 3. 8(b)**. The plots of **Figure 3. 9** confirms unambiguously that increasing current compliance lowers both the LRS value together with its standard deviation.

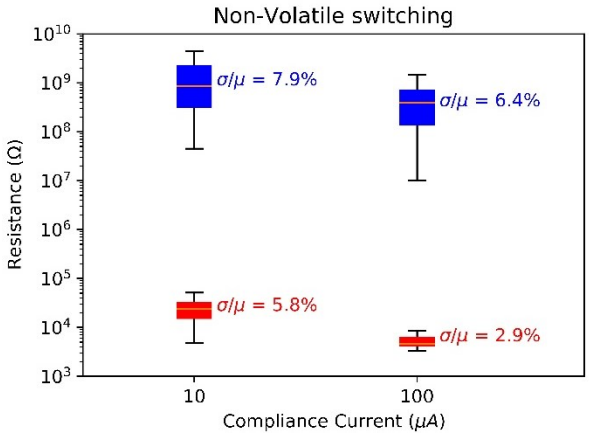


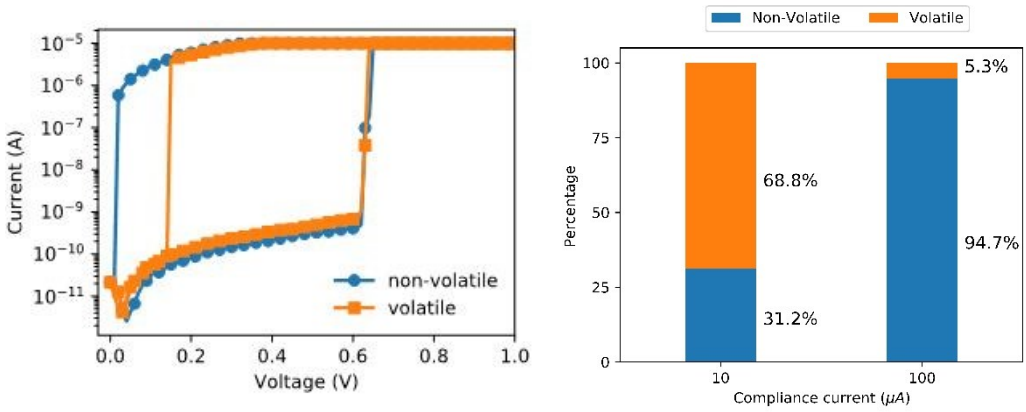
Figure 3. 9 Box plots of LRS/HRS at 10 µA and 100 µA current compliance restricted to the Non-volatile switching (RLRS>10^6 Ω). Texts in insert indicate the ratio between the standard deviation and mean value of the resistance distribution.

2.2.c.Volatile vs Non-Volatile switching

In most of the cases, for the device subjected to 10 µA compliance current and during the backward sweep from the positive voltage bias, the devices switches to the High resistance state leading to volatile switching. This phenomenon illustrated in **Figure 3. 10(a)** . The early breakdown of the conductive filament (CF) at low voltages can be related to the dependency of the CF size (area) on the compliance current (I_c) as explained in previous research works **[7], [8]**. It has been mentioned that the cross sectional area of the CF decreases with the decrease of I_c , with simulations showing that reducing the CF diameter by 5 times, decreasing the lifetime of the CF by 150 times **[7]–[10]**. Such type of volatile nature is a characteristic of surface diffusion of Ag clusters into the dielectric material **[10]**.

To evaluate this phenomenon quantitatively, we computed the set failure rate of the devices. Hence forth, a failed set can be defined as a set where the LRS value read at 50 mV has a resistance greater than the threshold resistance (R_{th}) of 1MΩ ohms. 1MΩ ohms is taken as R_{th} as this value is intermediate state between the HRS (10^8 ohms) and LRS (~10^4) states at 10 µA compliance current.

Thus, the percentage of the non-volatile and volatile switching in our devices can be calculated for each compliance current. **Figure 3. 10(b)** shows the volatile and non-volatile percentage of these CBRAMs.



(a) (b)

Figure 3. 10 (a) Depicting a failure set. (b) Showing the percentage of volatile and non-volatile switching at 10 and 100 µA respectively.

Looking closely at the current voltage characteristic of a typical volatile switching [**Figure 3. 10(a)**], we can notice that a large current drop occurs at reduced voltage biases. In the context of crossbar arrays of resistive memory, this feature could be exploited to achieve selector devices with high ON/OFF ratios **[11]**.

2.2.d.Volatile CBRAMs as selectors ?

Crossbars with numerous memory cells (often referred to as 1R structures) suffer undesired data reading and high power consumption due to sneak paths through unselected cells. An example of the selected path suppressing leakage current is shown in **Figure 3. 11**. To overcome such problems, one way is to use a transistor (1T) adjacent to the memory device. Although transistors can block the leakage current, it has problems related to its scaling. Hence, two terminal devices with a highly non-linear current-voltage characteristics (such as diodes) can therefore be associated to memory cells to suppress sneak path. These selectors devices can then suppress such leakage current in 1S-1R configuration at each cross point **[16]**.

A selector is in ON state above a threshold value of voltage with an abrupt increase in resistance, hence supplying current only to the selected cell. In a similar way in the low voltage regime, the selector returns in its OFF state below a *hold voltage* (V_{hold}), which hinders leakage current flow through the half-selected cells. Hence, selectors are important components in functioning of cross bar structures of emerging non-volatile memories.

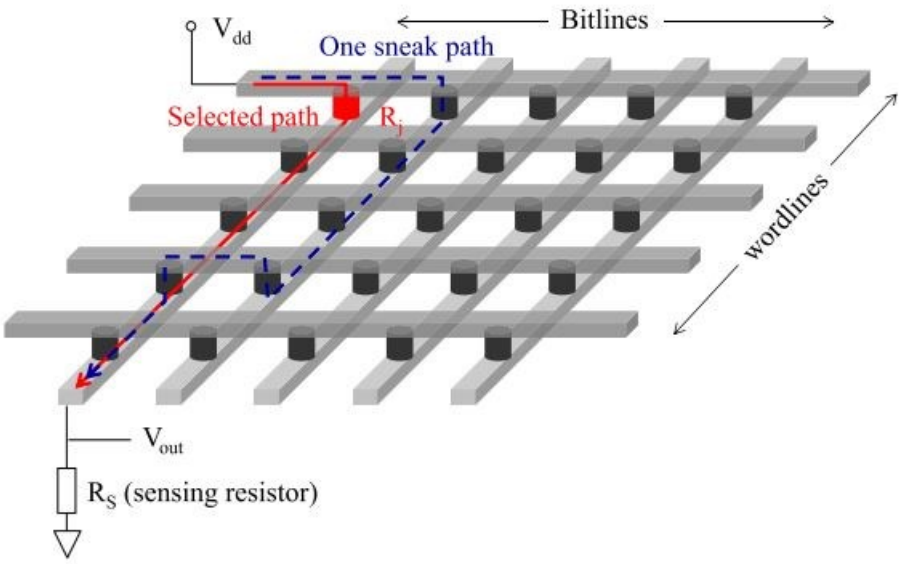
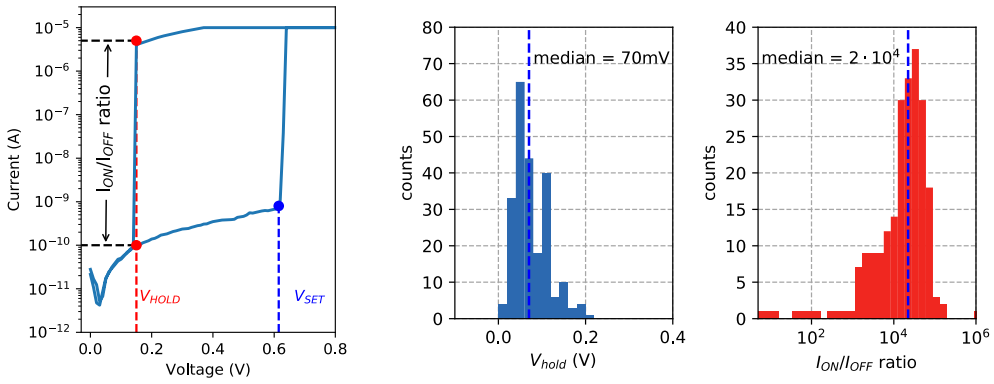


Figure 3. 11 Illustration of sneak paths in crossbar arrays.

In this context, it has been shown that volatile CBRAMs can be used as selector to suppress leakage current through the sneak paths and enable device selection. Previous work by Yoo *et al.* on HfO_2 and TiO_2 based ECMs as selectors with Ag filament showed good $I_{ON/OFF}$ ratios greater than 10^6 **[12]**. In 2017, Song *et al.* have exhibited GST based cross bar CBRAMs as selectors in 1 selector 1 resistor (1S1R) configuration **[13]**. Recently, in Aug. 2020, Banerjee *et al.* presented CBRAM based devices using Cu filament working as a selector with $I_{ON/OFF}$ ratio 3 x10^3, hence posing CBRAMs as selector devices **[14]**.

In this context, we extracted the values of *the hold voltage* (*i.e.* voltage at which the device returns in the HRS) and I_{ON}/I_{OFF} ratios as defined in **Figure 3. 12(a).** Keeping in mind that volatile switching is mostly evidenced at 10 µA, **Figure 3. 12** shows that our devices may act as selectors with a median ON/OFF ratios exceeding 10^4 and *hold voltages* (V_{hold}) lower than 200 mV.



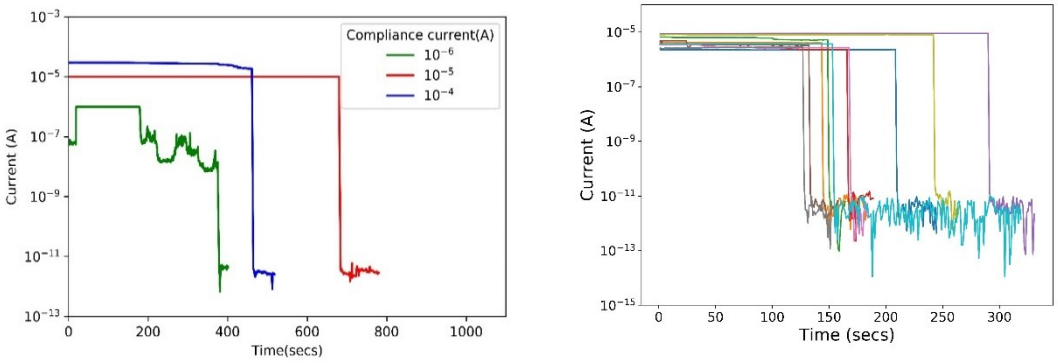
(a) (b)

Figure 3. 12 (a) Definition of hold voltage (V_{Hold}) and $I_{ON/OFF}$ ratio based on a volatile switching IV curve and (b) distribution of V_{Hold} and $I_{ON/OFF}$ achieved at a 10 µA compliance current.

2.2.e. Retention time

Among the different works reporting CBRAM devices employing PEO as solid-electrolyte, there has been few reports on their retention time studies **[5][6]**. In this work, retention tests were performed on Ag doped ($AgClO_4$) devices with concentrations from 1 to 4 wt.% under ambient atmosphere read at a constant voltage of 0.01 V after several switching cycles. The devices showed long pulses>10^4 seconds. Therefore, retention measurements were conducted using the following procedure on our pure-PEO based CBRAMs:

- Firstly, a positive IV sweep up to 1.0 V is performed to set the device at a given compliance current. Then, a current versus time measurement is recorded at a constant voltage bias of 50 mV. This procedure is then repeated for three compliance currents : 1 µA, 10 µA and 100 µA. As seen in **Figure 3. 13(a)** retention time tends to vary with the compliance current. Our devices showed LRS retention time values ranging from 120 to 750 seconds.



(a) (b)

Figure 3. 13 (a)The LRS retention time measured on a device after programming at a compliance current of 1 µA, 10 µA and 100 µA. (b) The retention time measurements taken for a compliance current of 10 µA showing variability. All the I-t measurement readings are taken at a constant voltage of 50 mV.

Electrical variability in the retention time measurements is clearly evidenced in **Figure 3. 13(b)** when written at a constant CC of 10 µA. Not only retention time varies from one measurement to the other but it can also be noticed that the initial current value – I (t=0) – is also variable, which is related to the intrinsic LRS variability. As already mentioned the CF size increases with the CC, explaining the observed tendency of increased retention time with CC.

Despite these poor results, it should be mentioned that our devices are un-optimized; indeed Wu *et al.* showed that doping of the solid polymer electrolyte layer can help achieve higher retention times $>10^4$ **[5]**. The ease of availability of Ag ions for filament formation at an optimized doping percentage of 3-weight % of $AgClO_4$ salt in PEO has exhibited such results.

2.3. Conclusion to the section

In the above section, we presented the electrical characteristics obtained on vertical CBRAMs based on PEO layers. Firstly, we showed that Ag electrode is required to achieve switching mechanism together with the application of bipolar programming voltage to set/reset the devices. These observations are in favour with resistance switching controlled by metallic Ag filaments formation/dissolution issued from the Ag active electrode rather than an intrinsic switching effect of the PEO layer.

Devices with three different nominal PEO thicknesses were fabricated : 30, 50 and 150 nm. Even if resistance switching could be found evidenced on few samples featuring a 50 nm-tick PEO layer, it is shown that only devices with an average thickness of 150 nm exhibit reversible resistance switching.

Through IV characteristics and voltage statistics, it can be concluded that the switching voltages are in the range of +2.0 V to -1.4 V with a high OFF/ON resistance ratio $> 10^4$. Endurance cycles are performed at two different compliance currents – 10 and 100 µA undergoing 321 and 390 cycles respectively. As observed, the switching of the LRS to HRS at low voltages in the backward sweep at CC of 10 µA exhibit that the devices are volatile in nature and this can be controlled by setting of the CC. However, such characteristic in our CBRAMs can be exploited as selector applications. Finally, retention time measurements on the devices show poor results and variability in their performance but it has to be mentioned that further optimization of the devices are still possible.

3. Analysis of conduction mechanisms in Pt/PEO/Pt and Ag/PEO/Pt devices

In this section, a study and analysis of conduction mechanisms in Pt/PEO/Pt is presented through temperature measurements. Then, conduction mechanisms are analysed in Ag/PEO/Pt at ambient temperature, based on the data collected during the assessment of their electrical characteristics.

3.1. Analysis of Pt/PEO/Pt devices

Current-voltage measurements were conducted on the devices in the temperature range of 230 K to 330 K, and up to voltages to ±5V as shown in **Figure 3. 14.** As observed, the devices showed symmetric IV characteristics with a dependency on temperature. To elucidate the underlying conduction mechanism, various types of conduction mechanism where investigated in the following, including Schottky, Poole-Frenkel emission, hopping and ohmic conduction.

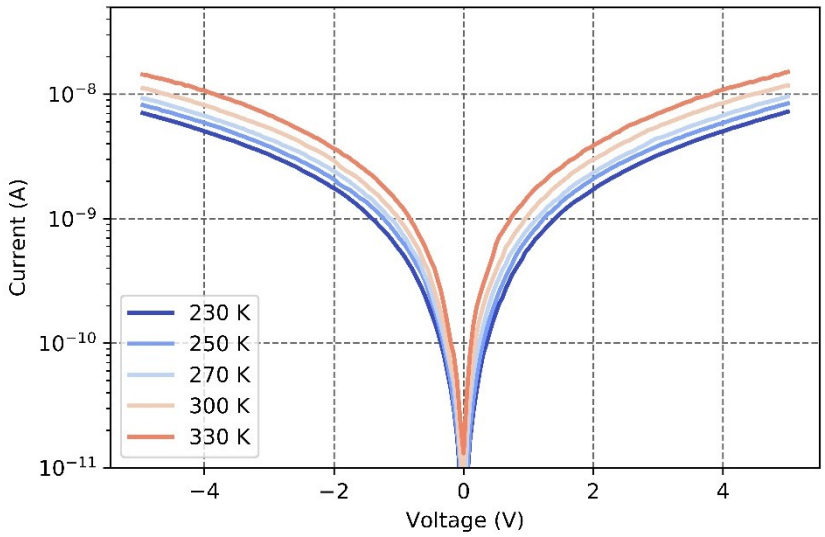


Figure 3. 14 Current-voltage measurements on Pt/PEO/Pt devices at different temperatures.

A detailed description of each type of conduction mechanism is available in **Appendix E** at the end of the manuscript.

Table 3. 1 summarizes the main equation for each conduction mechanism **[15][16]**. All experiments were conducted on a reference device featuring a 150 nm-thick PEO layer. The electric field (E) was simply deduced from the ratio between the applied voltage and the PEO thickness (150 nm).

Conduction Mechanism	J-E equation	Identification/extraction procedure
Schottky emission	$J_{sc}(E,T) = AT^2 \exp\left(-q\frac{\phi_b - \sqrt{\frac{qE}{4\pi\epsilon}}}{k_bT}\right)$ Main parameters: ϕ_b : barrier height [eV] ε: electrical permittivity [F/m]	Plot of ln (J/T^2) vs √E at various temperature. Extraction of ϕ_b : -Plot ln(J/T^2) vs q/k_bT at various voltage/electric field.
Poole-Frenkel emission	$J_{PF}(E,T) = q\mu N_c E e^{-q\frac{\phi_t - \beta\sqrt{E}}{k_bT}}$ Main parameters: ϕ_t : trap depth [eV] β : electric field barrier lowering factor[eV $m^{1/2}/V^{1/2}$]	Plot of ln(J/E) vs √E at various temp. Extraction of ϕ_t: -Plot ln (J/E) vs q/k_bT at various voltage/electric field.
Ohmic conduction	$J_{ohm}(E,T) = \sigma_0 e^{-\frac{E_a}{k_bT}} E^{\gamma}$ Main parameters: σ_o : Electrical conductivity [S/m] E_a : conductivity activation energy [eV]	Plot of ln(J) vs ln(E) at various temp Extraction of σ_o, E_a: -Plot ln(J) vs q/kbT at various voltage/electric field

Table 3. 1 Summary of the main conduction mechanism investigated in this study together with the identification and parameter extraction procedures.

3.1.a.Schottky emission

As shown in **Figure 3. 15(a)** Schottky plots exhibit a linear behaviour above 2 V. As mentioned in

Table 3. 1, it is possible to extract the Schottky barrier height ϕ_b from the slopes of Arrhenius plots (i.e. ln ($\frac{J_{SE}}{T^2}$) plotted as function of versus $\frac{q}{k_bT}$) at various voltage (respective electric field). **Figure 3. 15(b)** shows a selection of Arrhenius plots and the evolution of the extracted activation energy (E_a) as a function of √E. The value of ϕ_b is then extracted as the intercept of E_a vs. √E curve [**Figure 3. 15(c)**]. The junction barrier height is found to be 13 meV, which is lower than the expected junction barrier height of 4.79 eV from the

literature for oxide based polymers **[17]**. The junction barrier height extraction is given in the **Appendix G**. Hence, for the above mentioned reason, Schottky emission was excluded.

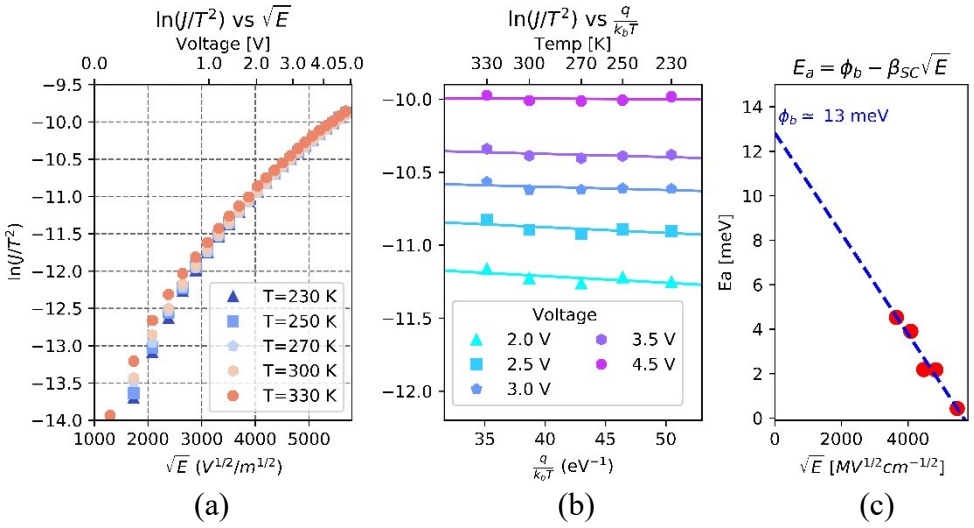
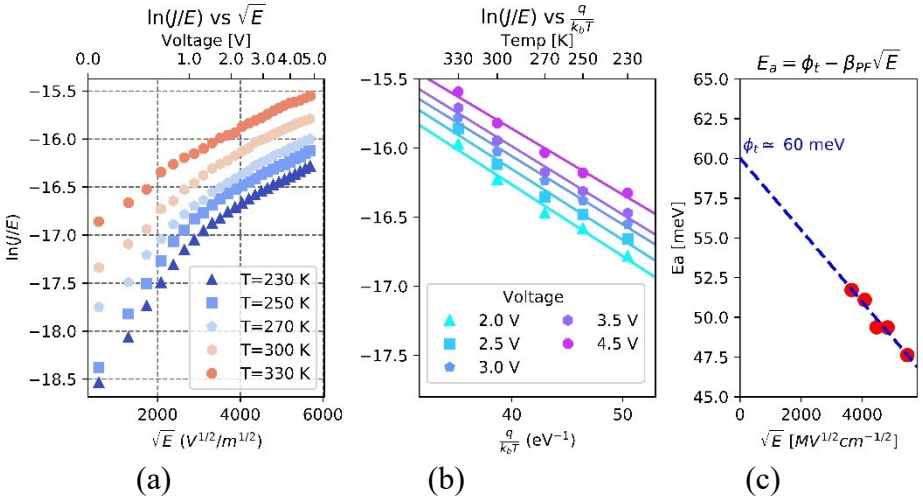


Figure 3. 15 (a) Schottky plots at various temperatures. (b) Arrhenius plots at various voltages: $ln\left(\frac{J_{SE}}{T^2}\right)$ versus $\frac{q}{k_bT}$. For each plot, the activation energy was extracted and plotted as a function of √E in (c) to extract the corresponding Schottky barrier height ϕ_b.

3.1.b.Poole Frenkel emission

Among the bulk limited conduction mechanisms, Poole Frenkel (PF) conduction mechanism is probed by plotting $\ln\left(\frac{J_{PF}}{E}\right)$ versus √E as shown in **Figure 3. 16(a)**. The PF plots show a linear behaviour at voltages of 1.5 V and above. From Arrhenius plots of $\ln\left(\frac{J_{PF}}{E}\right)$ versus $\frac{q}{k_bT}$ in **Figure 3. 16 (b) ,** an activation energy is extracted at several voltages. Following a similar methodology than presented before, a trap depths ϕ_t value can be extracted at shown **Figure 3. 16 (c)**.



(a) (b) (c)

Figure 3. 16(a) Poole Frenkel plots at various temperatures. (b) Arrhenius plots at various voltages: $ln\left(\frac{J_{PF}}{E}\right)$ versus $\frac{q}{k_bT}$. For each plot, the activation energy was extracted and plotted as a function of √E in (c) to extract the corresponding trap barrier height ϕ_t.

The extracted trap depth (ϕ_t) was found to be 60 meV which corresponds to the depth of physical defects due to conformational disorders present in the solid electrolyte layer **[18]**.

3.1.c.Low-voltage region: Ohmic conduction

Both Schottky and Poole-Frenkel emission were identified as possible conduction mechanism (with its dependency on temperatures) at voltages higher than 2 V but only Poole-Frenkel emission was consistent after the extraction of the trap barrier height. For lower voltage regions (< 2V), **Figure 3.17(a)** reveals that the current density (J) is proportional to the electric field **[19][20]**. This leads us to consider ohmic conduction in this voltage region (eq. 1):

$$J = \sigma_O e^{-\frac{E_a}{k_bT}} \cdot E \qquad (1)$$

where σ_O is a conductivity pre-factor, E_a is the conduction activation energy and E the electric field. Although we did observe a linear relationship between J and E, the slope of $\ln(J)$ *vs* E curves was slightly different from unity. For this reason, we considered eq. 4 - a modified ohmic equation, to account for conduction in this region **[21][22]**:

$$J = \sigma_O e^{-\frac{E_a}{k_bT}} \cdot E^{\gamma} \qquad (2)$$

Where γ (arbitrary units), supposedly close to 1, is a field factor used as a fitting parameter.

Upon fitting the ln $\ln(J)$ *vs* E curves of **Figure 3.17(a)** we extracted γ values and the corresponding intercept (i.e. $\ln(\sigma_O) - \frac{E_a}{k_b T}$) at each temperature value. As can be seen from **Figure 3.17 (b)** γ is almost constant with temperature with a mean value around 1.36 while an activation energy of 0.41 eV was found **Figure 3.17 (c)**]. Therefore, under these assumptions, a close to ohmic type of conduction mechanism is exhibited in the low voltage region with an low-temperature electrical conductivity extracted to be 46.4 µS/cm.

Note: The field factor can be assumed to be linked to a charge-carrier mobility as given in equation 5:

$$J = \sigma_O e^{-\frac{E_a}{k_b T}} \cdot E^{\gamma-1} \cdot E = qn\mu(E) \cdot E \qquad (3)$$

Where n is the charge carrier density and µ(E) an electric-field dependent mobility. In our case $\mu(E) \propto E^{\gamma-1} \approx E^{0.36}$. Another possibility is that the observed conduction regime is a combination of both Ohmic and Space-Charge-Limited-Current which exhibits a power 2 dependency with respect to the applied voltage (see **Appendix E**).

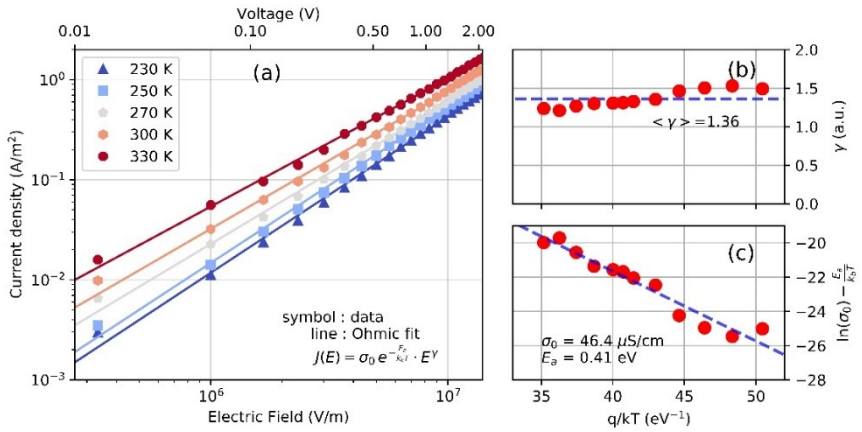


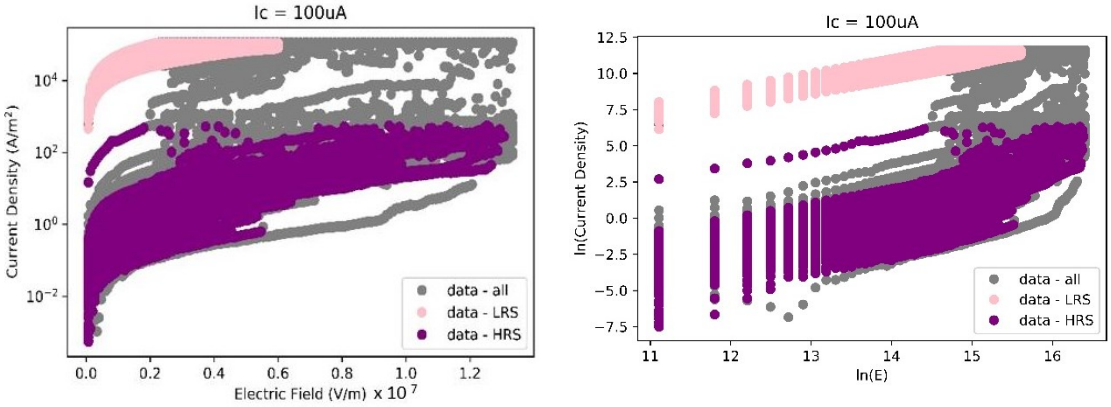
Figure 3. 17 (a) Plot of J versus E in log scale at various temperature in the low voltage region (<2 V) Solid lines correspond to fitting curves using the modified ohm's law of eq. 4. (b) Evolution of the field factor γ at various temperature extracted from the slope of curves in (a). (c) Extraction of the conductivity pre-factor (σ_O) and activation energy (E_a) from the intercept of the fitting curves in (a).

3.2. Analysis on Ag/PEO/Pt devices

Conduction mechanism was studied on Ag/PEO/Pt devices consisting in 30 x 30 µm^2 cross bar structures. In this study, more than 300 set cycles, recorded at ambient

temperature, with a set current compliance of 10 and 100 µA were considered as statistical data. As explained in the previous section, using a current compliance of 10 µA can lead to a volatile switching; in this section focus was made on non-volatile switching and volatile switching were excluded from this study. As an illustration, **Figure 3. 18(a)&(b)** show the datasets considered for the study of low and high resistance states for a 100 µA current compliance.

Although the reference Pt/PEO/Pt devices could be swept from 0 to +5V without exhibiting any resistance switching, the voltage sweeps were restricted to 2 V on the Ag/PEO/Pt devices given the low set voltages values [**Figure 3. 5**]. As shown in **Figure 3. 18** the *ln(J)* vrs *ln(E)* plots indicates a linear relationship between J and E in high resistance state. Therefore, ohmic type of conduction mechanism would be considered in this study. This assumption is easily justified for the LRS, since ohmic behavior is widely reported in CBRAM/RRAM in the LRS **[21][22][23]**.



(a) (b)

Figure 3. 18 (a) Considered data in the LRS (pink) and HRS (purple). (b) Plot of ln J versus ln E showing a linear behavior for both LRS and HRS.

Given all measurements were performed at ambient temperature, ohmic conduction will assumed using the following equation **[16]**:

$$J = \sigma \cdot E^{\gamma} \qquad (4)$$

where σ is the electrical conductivity and γ is the field factor as defined in the previous section.

The analysis procedure applied to LRS and HRS cycles is as follows: the I-V curve is fitted in log scale using eq. (4). The corresponding values of σ and γ are then collected for each cycle and plotted as histogram plots.

3.2.a. Low Resistance States (LRS)

Figure 3. 19 & **Figure 3. 20** shows the extracted distributions of σ and γ for compliance currents of 100 and 10 µA respectively. A trend line, obtained from the mean values of σ and γ is also reported in **Figure 3. 19** & **Figure 3. 20**. The histogram plots (c) of **Figure 3. 19** & **Figure 3. 20** reveal that γ values are closely distributed around 1.0, confirming that ohmic transport is prevalent in the LRS for both compliance currents.

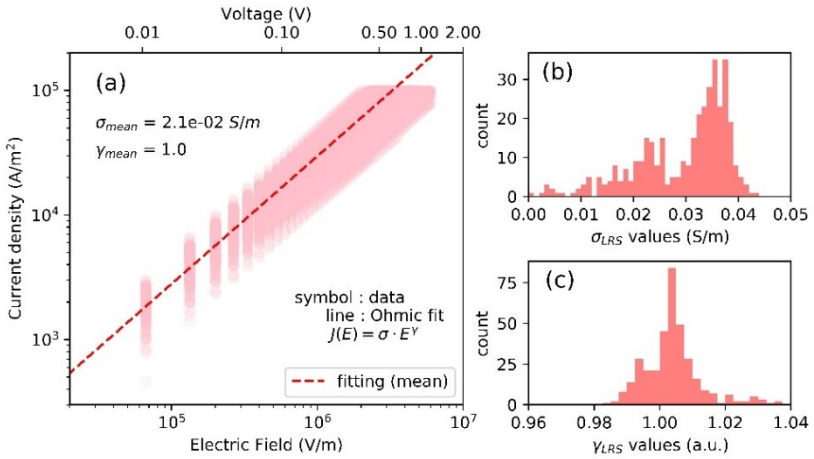


Figure 3. 19 Study of LRS at Ic=100 µA. (a) J-E plots and Ohmic fit using eq. 6 together with mean values of σ and γ extracted from histograms (b) and (c).

It is shown that the mean σ value decreases from 21 mS/m and 4.8 mS/m as the current compliance is decreased, which is consistent with the increase of the LRS resistance reported in **Figure 3. 9**.

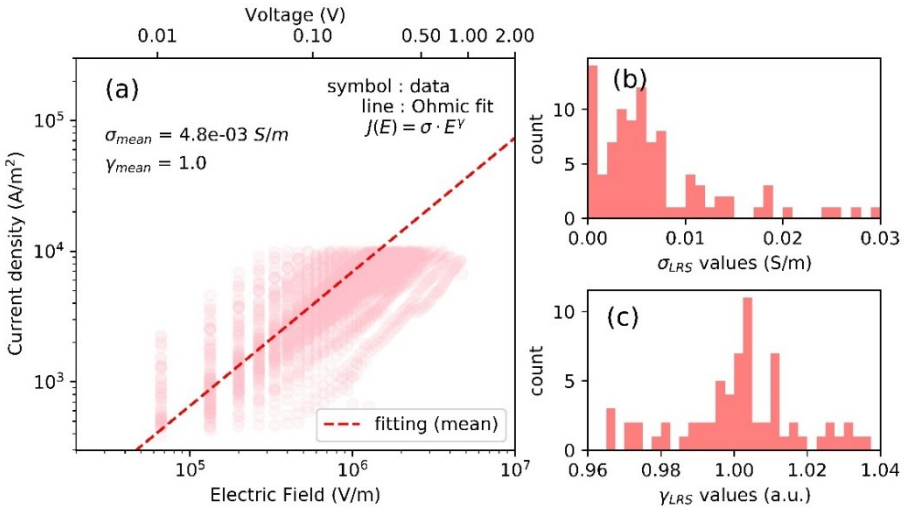


Figure 3. 20 Study of LRS at Ic =10 µA, only non-volatile switching were considered. (a) J-E plots and Ohmic fit with mean values of σ and γ extracted from histograms (b) and (c).

3.2.b. High Resistance State (HRS)

Following the same procedure, an analysis of the High Resistance state was performed; results are shown in **Figure 3. 21** & **Figure 3. 22**. In comparison with Pt-PEO-Pt device (in black fits) [in both **Figure 3. 21** & **Figure 3. 22**]. For both compliance currents the fitting parameter (γ) was found to have a close mean value (1.34 vs 1.36), while the mean electrical conductivity was found to be 10 times higher than for the reference device at 300 K (*i.e.* 0.6 nS/m, calculated from the conductivity pre-factor and the activation energy value presented in **Figure 3. 22**. Nevertheless, the electrical conductivity of the reference device falls within the distribution range of the extracted σ values in HRS.

A possible reason for such a higher electrical conductivity could be the fact that memory devices could not recover their pristine state after being reset due to a residual conductive filament or to the inclusion of Ag precipitates within the PEO layer. In addition, it has to be noticed that measurements on the reference device have been performed on a single analytical devices; in order to allow for a better comparison, one should also have also considered statistical measurements.

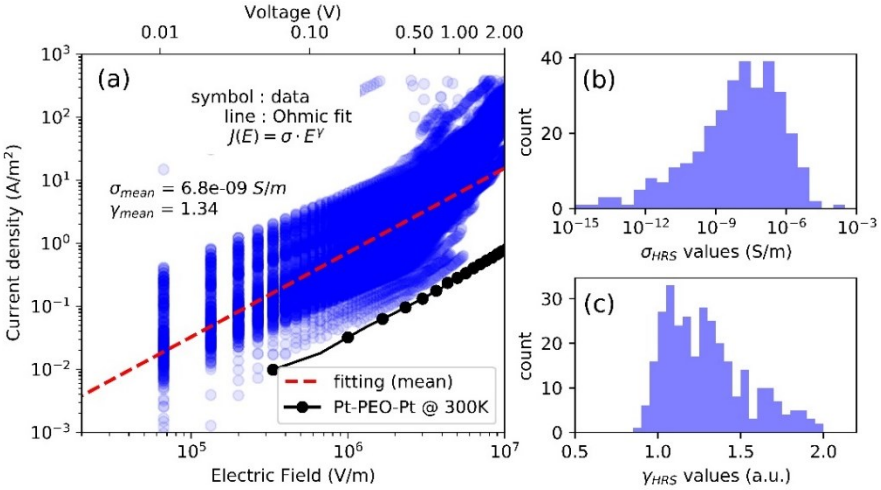


Figure 3. 21 Study of HRS for Ic =100 µA. (a) J-E plots and Ohmic fit using eq. 4 together with mean values of σ and γ extracted from histograms (b) and (c). The J-E curve of the reference Pt-PEO-Pt recorded at 300 K is shown in (a) for comparison.

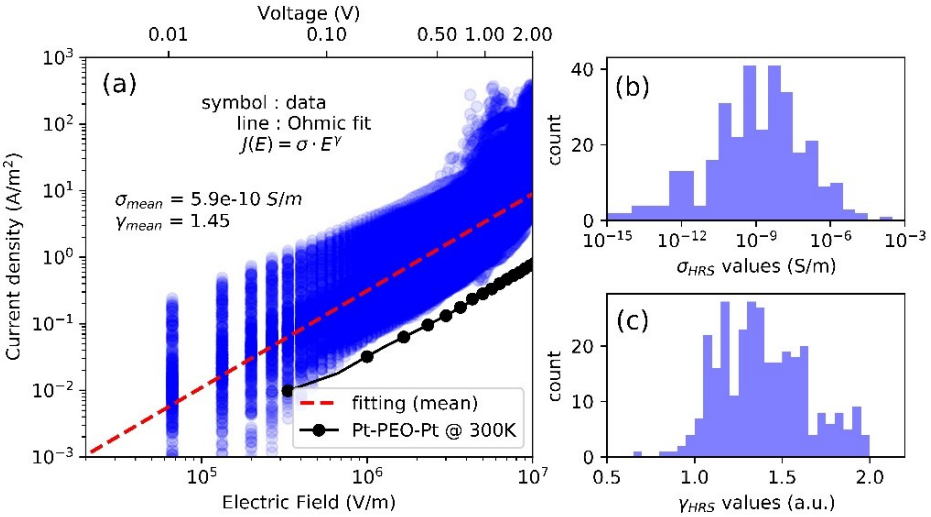


Figure 3. 22 Study of HRS for Ic=10 µA. (a) J-E plots and Ohmic fit using eq. 4 together with mean values of σ and γ extracted from histograms (b) and (c). The J-E curve of the reference Pt-PEO-Pt recorded at 300K is shown in (a) for comparison.

3.3. Conclusion

From the Pt/PEO/Pt and Ag/PEO/Pt devices, the low resistance state (LRS) and high resistance state (HRS) shows ohmic type of conduction mechanism at low voltages < 2.0 V. However, for the HRS it has to be mentioned with the fitting parameter (γ) greater than 1, a mechanism influenced by ohmic and SCLC can describe it is more precisely. **Table 3. 2** summarizes the electrical parameters extracted from our measurements.

Temperature measurements performed from 230 up to 330 K revealed Poole Frenkel (PF) emission at higher voltages (>2V) with a trap depth of 60 meV for the Pt/PEO/Pt reference device.

		Electrical parameters for ohmic conduction $J = \sigma \cdot E^{\gamma}$	
	I_{comp} (µA)	**σ**	**γ**
Pt/PEO/Pt	-	$\sigma_O = 46.4 \cdot 10^{-8} S/m$ $E_a = 0.41\ eV$ $\sigma = 0.61 \cdot 10^{-9} S/m$ @ 300K	~ 1.36
Ag/PEO/Pt (HRS)	10	$6.8 \cdot 10^{-9}\ S/m$	~ 1.34
	100	$6.1 \cdot 10^{-10}\ S/m$	~1.45
Ag/PEO/Pt (LRS)	10	$2.1 \cdot 10^{-2}\ S/m$	~ 1
	100	$4.8 \cdot 10^{-3}\ S/m$	~ 1

Table 3. 2 Summary of the identified conduction mechanisms and extracted electrical parameters in our reference Pt/PEO/Pt devices and Ag/PEO/Pt CBRAM devices for a 150 nm-thick PEO layer.

4. Conclusion to the chapter

In this chapter the electrical characterization an analysis of vertical CBRAM devices on silicon substrates was conducted. Through a comparison with reference Pt/PEO/Pt device we showed that resistance switching can be unambiguously attributed to filament creation/dissolution due to the Ag electrode and is not an intrinsic property of the PEO layer. It has been then shown that a minimal PEO thickness of 50 nm is necessary to have resistive switching, devices with lower thicknesses being short-circuited. This phenomenon may be attributed to a diffusion layer of Ag, preventing switching of devices with a thin (i.e. <50 nm) PEO layer.

Upon electrical characterization its observed, devices exhibited low set/reset voltages between +1 V to -1 V with high $R_{OFF/ON}$ ratio ~ 10^6 . Following **Table 3. 3** shows the OFF/ON resistance ratio with devices using different SPE layers.

Reference	**Polymer as active layer**	**OFF/ON resistance ratio**
Sun Y. *et al.* **[24]**	PVP and 2-Amino-5-methyl-1,3,4-thiadiazole	10^4
Ji Y. *et al.* **[25]**	PI:PCBM	10^4
Jang J. *et al.***[26]**	PI:PCBM	10^4
Sun Y. *et al.***[19]**	EMAR : CNTs	10^4
Lv W. *et al.***[20]**	PCBM :MoS_2	10^3
Machado W. S. *et al.***[27]**	PVP :PMF	10^5
This work	*Polyethylene oxide (PEO)*	*~10^6*

Table 3. 3 Summarizes the OFF/ON resistance ratio of the devices using different SPE layers.

The devices where subjected to different current compliance currents during cycling (10 and 100 µA). It was shown that lowering current compliance lead to increase variability in both LRS and HRS but also to volatile switching. Given their high OFF/ON resistance ratio, it has been shown that such volatile CBRAMs may serve as selectors with an average hold voltage of 70 mV and $I_{ON/OFF}$ ratio of 10^5. Retention time measurements showed values not exceeding 800 seconds whatever the programming conditions (1-100 µA). As stated in the literature, retention properties may be improved through doping the PEO layer with silver salts.

Finally, an analysis on the conduction mechanism in our device is proposed. Through temperature measurements, we showed that reference Pt/PEO/Pt devices exhibited Poole-Frenkel conduction at voltages >1V while a close to Ohmic conduction was evidence at lower voltages. On memory devices, statistical analysis conducted at two compliance current values revealed Ohmic conduction in LRS and a close to Ohmic regime in HRS. In that case it is suggested that conduction combines both Ohmic and Space-Charge-Limited Conduction.

5. References

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APPENDIX E: Review of Conduction Mechanisms

- **Fowler-Nordheim (F-N) and Direct tunnelling [15][16]**

Tunneling is a quantum mechanical effect. A tunnelling current occurs when electrons move through a barrier that they classically should not be able to move. It is usually dominant for thicker oxide (in 10's of nm) and high electric field **[28][29]**. The energy band diagram is shown in **Figure E. 1.**

$$J_{FN} = \frac{q^2}{8\pi h \Phi_B} E^2 \exp\left[\frac{-8\pi(2qm^*)^{0.5}}{3hE}\right]\Phi_B^{1.5} \qquad (1)$$

Where J_{FN} is the current density, m^* is electron effective mass in the polymer layer, h is Planck's constant, Φ_B is the junction barrier height, E is the applied electric field and q is the charge of an electron.

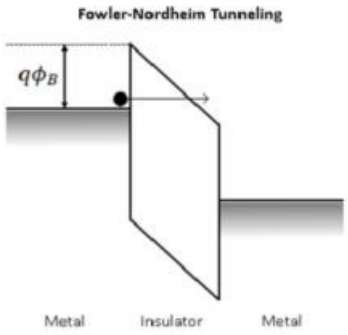


Figure E. 1 Shows the energy band diagram for Fowler-Nordheim (F-N) tunnelling.

Direct tunneling is dominant in dielectrics thinner than 3 nm and dependent upon the relative dielectric constant of the oxide layer as given by the equation **[15]**:

$$J_{DT} \approx \exp\left[\frac{-8\pi(2q)^{0.5}}{3h}\right](m^*\Phi_B)^{1.5} k.t_{polymer,eq} \qquad (2)$$

Where J_{FN} is the current density, k is the relative dielectric constant of the polymer layer and $t_{polymer,\ eq}$ is the equivalent polymer thickness. **Figure E. 2** Shows energy band diagram for direct tunneling.

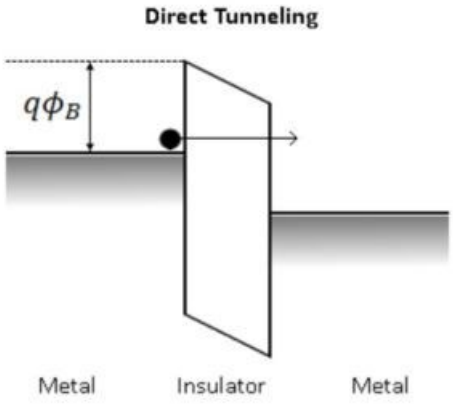


Figure E. 2 Shows energy band diagram for direct tunneling.

Fowler-Nordheim (F-N) tunneling and direct tunnelling is not applicable in these CBRAM devices as they are workable at low electric field (< 1MV/cm) **[36]** and for thicker films (> 40 nm)**[31]**.

- **Schottky Emission**

The Schottky or thermionic emission happens when thermally-activated electrons injected over the energy barrier into the conduction band of the oxide. This type of conduction mechanism in oxide especially in relative high temperature. **Figure E. 3** Schematic energy band diagram of Schottky emission in metal-insulator-metal (MIM) structures.

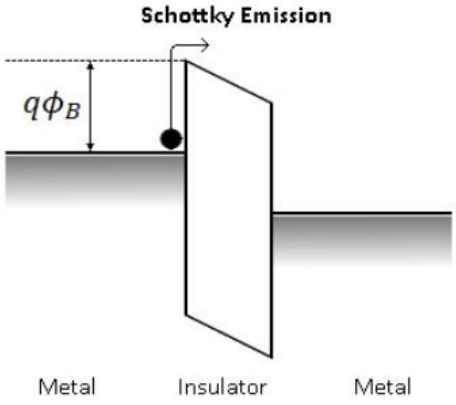


Figure E. 3 Schematic energy band diagram of Schottky emission in metal-insulator-metal (MIM) structures.

$$J_{SE} = \frac{4\pi q m^*(kT)^2}{h^3} \exp\left[\frac{-q(\Phi_B - \left(\frac{qE}{4\pi\varepsilon}\right)^{0.5}}{kT}\right] \qquad (3)$$

J_{SE} is the current density, m^* is electron effective mass in the polymer layer, h is Planck's constant, Φ_B is the junction barrier height, E is the applied electric field and q is the charge of an electron, ε is the permittivity of the polymer, T is the absolute temperature, k the Boltzmann's constant.

On simplifying & taking log (ln) the equation 3

Taking ln both sides

$$\ln\left(\frac{J_{SE}}{T^2}\right) = \ln A - \frac{q}{k_b T}(\Phi_B - \beta_{sc}\sqrt{E}),$$

where $A = \frac{4\pi q m^*(k_b)^2}{h^3}$, $\beta_{sc} = \sqrt{\frac{q}{4\pi\varepsilon}}$

Therefore a plot of ln J_{SE} versus $(E)^{0.5}$, where A is the intercept and B the slope.

- **Hopping conduction: NNH & VRH**

Nearest Neighbour Hopping (NNH): Oxide layer often contains defects known as traps. Electrons that are trapped in one trap site can hop into other nearest trap sites through

tunnelling effect **[16][31]**. **Figure E. 4** Shows the schematic for energy band diagram for NNH and VRH type of conduction mechanism.

$$J_{NNH} = \sigma_O.\exp\left[-\frac{T_O}{T}\right]. E \qquad (4)$$

Where σ_O is the electric conductivity at reference temperature T_o (in Kelvin), T is the absolute Temperature and E is the applied electric field.

Variable Range Hopping (VRH): It is a hopping conduction mechanism, in strongly disordered systems **[16]**, where electron hops into traps that are further away.

$$J_{VRH} = \sigma_O. \exp\left[-\left(\frac{T_O}{T}\right)^{0.25}\right]. E \qquad (5)$$

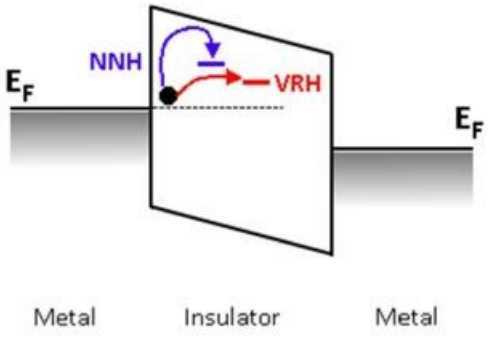


Figure E. 4 Shows the schematic for energy band diagram for NNH and VRH type of conduction mechanism.

- **Space Charge Limited Current (SCLC)**

In the Space charge limited current (SCLC) regime, the current is dominated by charge carriers injected from the contacts and the current voltage characteristics becomes quadratic ($I \sim V^2$). Here the current is limited by volume. SCLC regime can be classified into three regions: firstly, the ohmic region where $I \propto V$, in the low electric field; secondly, the region where child's law is followed where $I \propto V^2$ and in the next region there is a steep increase in the high electric field **[15][16][32][33][34]**. SCLC equation is given as follows:

$$J_{SCLC} = \frac{9}{8}\varepsilon_i \mu\theta \frac{V^\beta}{d^3} \qquad (6)$$

Where, J_{SCLC} is the current density, ε_i is the absolute permittivity of the oxide, μ is the mobility of the electrons, θ is the ratio between trapped and shallow charges, V is the voltage bias , β is the power co-efficient of V which can be 1 or 2 or greater depending on the fitting and d is the thickness of the polymer layer.

On simplification of equation 6, we get

$$\ln J_{SCLC} = \ln \alpha + \beta \ln V$$

$$\text{where } \alpha = \frac{9}{8d^3} \varepsilon_i \mu \theta$$

As observed in **Figure E. 5** SCLC mechanism was probed in Pt/PEO/Pt devices showing two regions : the ohmic region with slope of 1.1 and the second region with slope 1.7. which does not follow child's law ($I \propto V^2$). Moreover, with prominent dependency of our devices on temperature, SCLC mechanism is overruled.

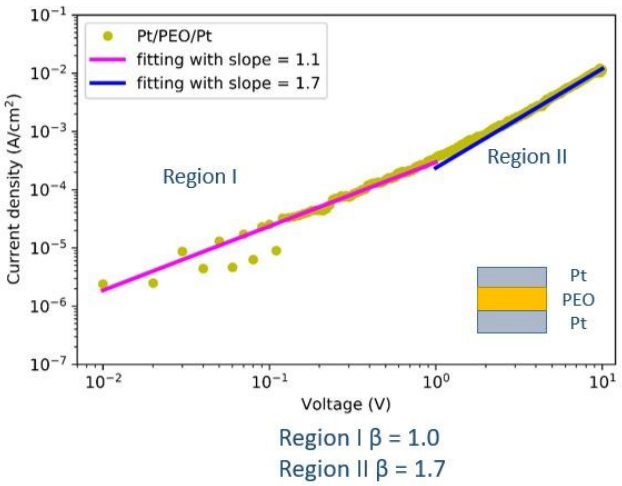


Figure E. 5 For Pt/PEO/Pt devices, two regions: region I: ohmic region in the low electric field, where I ∝V with slope 1.1, and region II: trap unfilled region with slope 1.7.

- **Poole Frenkel**

The Poole Frenkel emission happens when trapped electrons get excited into the conduction band of the oxide. The electric field decreases the Coulombic potential barrier of the

electrons and subsequently increases its probability for being thermally excited out from the traps. Generally, it is observed at high temperature and high electric field**[20][33]**. **Figure E. 6** presents the schematic diagram of Schottky emission.

$$J_{PF} = q.\mu.E.N_c.\exp\left[\frac{-q(\Phi_T-\left(\frac{qE}{4\pi\varepsilon}\right)^{0.5}}{kT}\right] \qquad (7)$$

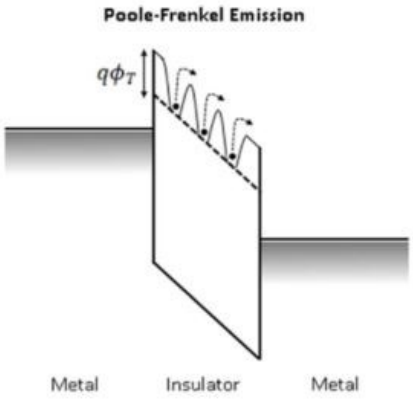


Figure E. 6 Schematic diagram of Poole Frenkel type of conduction mechanism.

On reconstructing the equation 7 and as the term

$J_{PF}= \ln(q.\mu.N_c) - \frac{q}{k_bT}\left(\Phi_T - \beta_{PF}\sqrt{E}\right)$,

where $\alpha = \ln(q.\mu.N_c)$,

$$\beta_{PF} = \sqrt{\frac{q}{\pi\varepsilon_o\varepsilon_r}}$$

In the equation α is obtained from intercept and β_{PF} from the slope of the plot between $\frac{q}{k_bT}$ versus $E^{0.5}$.

APPENDIX F: Box plots

Box plots take into account the variability of the data in the extreme positions. Firstly, the data is arranged in an ascending order. The median of the data set is represented by second quartile (Q2), here marked as median. The interquartile range (IQR) divides the data into four equal parts with Q1 and Q3 dividing the values below and above the median (Q2) into two equal halves. The whiskers make the minimum and the maximum of the data set, while outliers are the values in the data set corresponding to Q1-1.5*IQR and Q3+1.5*IQR respectively of the both extreme sides. **Figure F. 1**. explains a box plot. An example is illustrated in **Figure F. 2**.

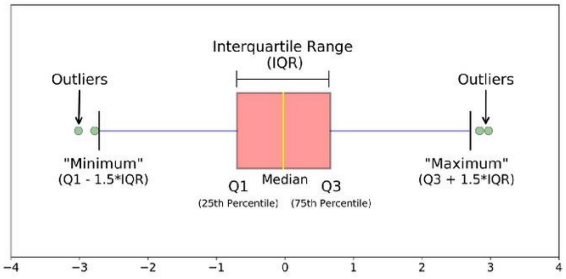


Figure F. 1 Explains the parts of a box plot.

Example: for data set :[18, 34, 76, 29, 15, 41, 46, 25, 54, 38, 20, 32, 43, 22]

Ascending order :[15, 18, 20, 25, 29, 32, 34, 38, 41, 46, 54, 76]

Median (Q2) is 32, Q1 is 22, Q3 is 43.

IQR= Q3- Q1 = 43-22 =21,

Outliers = [22- 1.5x21, 43+ 1.5x21] =[-9.5, 74.5]

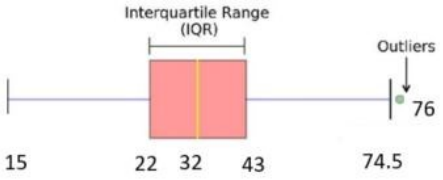


Figure F. 2 Interprets a box plot with an example.

APPENDIX G: Junction barrier height calculation

With the work

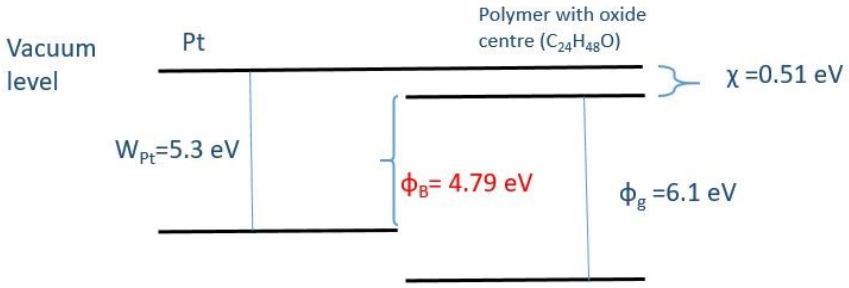


Figure G. 1 The calculation of barrier height junction of PEO based polymer

function of Pt as 5.3 eV, and as presented by Wang *et al.* , electron affinity of polymer oxides like PEO, is 0.51 eV and the band gap between the LUMO and HOMO levels is 6.1 eV, the junction barrier height (ϕ_b) is calculated to be 4.79 eV as shown in **Figure G. 1[17]**.

Chapter 4 - Study of planar CBRAM devices: electrical, physical and chemical analyses

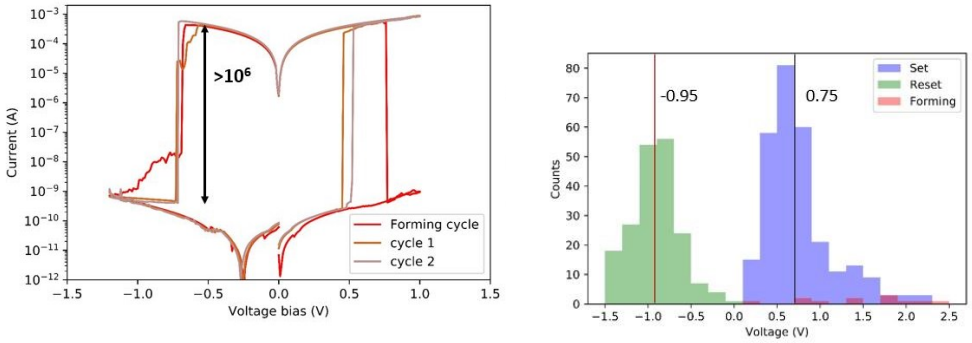
As discussed in the first chapter, the motivation to fabricate and study planar devices is to observe morphological changes on or around the nano-gap region. In the first part of this chapter, the electrical characterization of the planar devices are presented. In particular, set/reset voltage statistics, endurance capabilities together with retention were investigated with a focus on the effect of current compliance. In the second part, results on morphological/chemical observations are exposed. Examination of the nano-gap region was achieved through various microscopy techniques such as AFM and SEM-EDX to observe changes related to resistance switching in an attempt to evidence morphological and chemical changes related to resistance switching.

1. Electrical characterization

This part focusses on the IV characteristics of the planar devices with a silver (Ag) active electrode, a specific nano gap thickness of around 100 nm with deposition of Polyethylene oxide (PEO) by spin coating and Palladium (Pd) as inert electrode. Voltage bias (positive or negative) is applied on Silver (Ag), the other electrode (Pd) being grounded.

1.1. SET/RESET voltage statistics & memory window

IV characteristics on the devices are performed from 0.0 to 2.0 V or from 0.0 V to -2.0 V with a step of 0.01 V for set and reset processes respectively. **Figure 4. 1(a)** shows the IV characteristics of a planar device. The devices showed high switching OFF/ON resistance ratio of $>10^6$.



(a) (b)

Figure 4. 1 (a) IV characteristics of a planar device showing the forming, the first cycle and second cycle after forming exhibiting a high OFF/ON resistance ratio up to 10^6. (b) Forming/set and reset voltage statistics on 12 planar devices corresponding to at least 10 cycles per device.

The high memory window provided by these devices can allow multi-bit storage capacity of memories as shown by Chhatwal *et al.* where multistate can be achieved by voltage pulses or by setting of different compliance current as shown by Yang *et al.* **[1][2]**.

Further, programming voltages are reported in **Figure 4. 1(b)** collected for 12 devices, with a minimum of 10 cycles on a device. A mean set voltage of 0.75 V was found while the mean reset voltage was found to be -0.95V. The research works of Wu *et al.* and Krishnan *et al.* showed results with PEO as solid polymer electrolyte layer in CBRAMs with set/reset voltages ranging from 2.5 V to -0.5 V. These results are close from the ones found for vertical devices showing average set voltage as 0.75 V and reset as -0.50 V as presented in the first section of chapter 3.

1.2. Endurance cycles

In order to analyse the lifetime of the devices, repetitive cycles were performed. A current compliance of 1 mA is applied on the devices along with voltage sweeps from 0 to ±2.5 V. The high resistance state (HRS) and the low resistance state (LRS) are computed at a read voltage of 20 mV. Results are shown in **Figure 4. 2**

The device showed high OFF/ON resistance ratio greater than 10^5 and endurance cycles of 70 was obtained before failure (the device being stuck in the HRS showing no

switching). It should be mentioned that in this case the devices are subjected to full IV cycles inducing charge transport into the devices throughout the programming sequence and resulting to high energy dissipation and faster degradation of the devices.

To decrease the energy dissipation in the devices, pulse measurements were carried out. As illustrated in **Figure 4. 3(a)** the program/erase voltages are set at ±2.5V and read at 0.1 V. A pulse time for two seconds was used for every program/erase/read step. The performance of such measurements is reported in **Figure 4. 3(b)**. The devices showed a weak improvement in the endurance cycles up to 80 cycles, after that the devices remain stuck in the Low Resistance State.

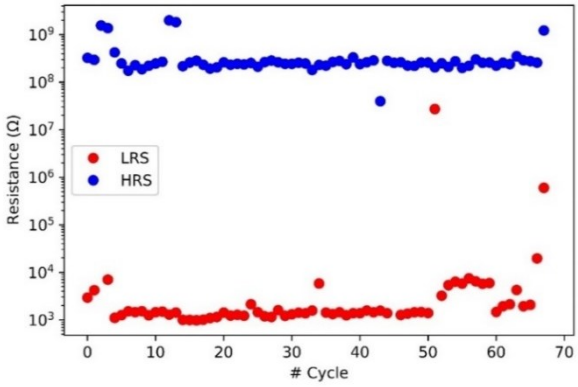
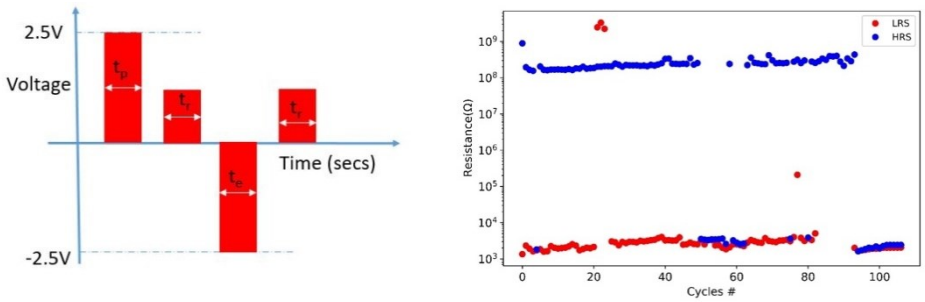


Figure 4. 2 Endurance cycles obtained during IV sweeps measurements. The devices exhibited high OFF/ON resistance ratio > 10^5 and fatigue failures after 70 cycles.

As reported in Chapter 3, vertically stacked MIM cross bars exhibited endurance test cycles > 300 along full sweep cycles each subjected to 10 and 100 µA compliance current. Among the polymers used PI: PCBM, PVP + thiadiazole used as solid polymer electrolyte with Al as electrodes have showed 200 and ~100 endurance cycles respectively**[3][4][5]**.

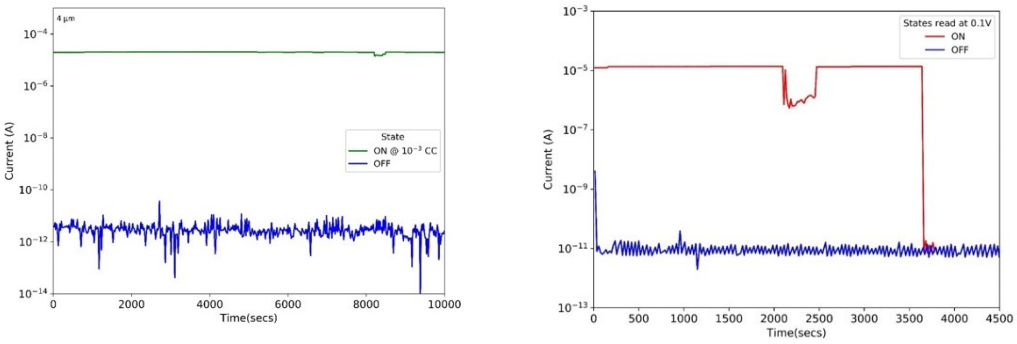


(a) (b)

Figure 4. 3 (a) Programming sequence used for pulsed measurements. The voltage pulse length is 2 sec for both set and reset. A compliance current of 1mA is used for set programming. (b) Endurance measurement results.

1.3. Retention time

For retention measurements, a set cycle was performed on the device at a certain set compliance current, subsequently the retention of current was measured with respect to the time. Following this protocol, the device was subjected to a set cycle at a compliance current of 1 mA, subsequently current versus time measurement was carried out at a constant voltage bias of 0.1 V. **Figure 4. 4(a)** depicts the best retention measurement achieved on a device.



(a) (b)

Figure 4. 4 Retention time measurement performed on two separate device (a) and (b) after programming at 1mA, showing electrical variability from one device to the other.

While vertical devices exhibited retention time measurements lower than 800 seconds, it can be seen that some planar devices can retain ON and OFF states for 10^4 seconds with a memory window of 10^6.

Figure 4. 4(b) shows another retention measurement obtained on a second device. A retention time of 3500 seconds is achieved in the same conditions. These two devices show variability in their performance.

Observing the lack of reproducibility on the retention time, statistics on the retention time at various compliance current was evaluated. Here compliance current (CC) is taken from 10 µA, 100 µA, 200 µA and 1 mA. It has to be mentioned that few readings were successful with 10 µA CC as there was an early filament breakdown at low voltages. **Figure 4. 5** presents the result of the measurements underlying the increase in the retention time together with the current compliance limit.

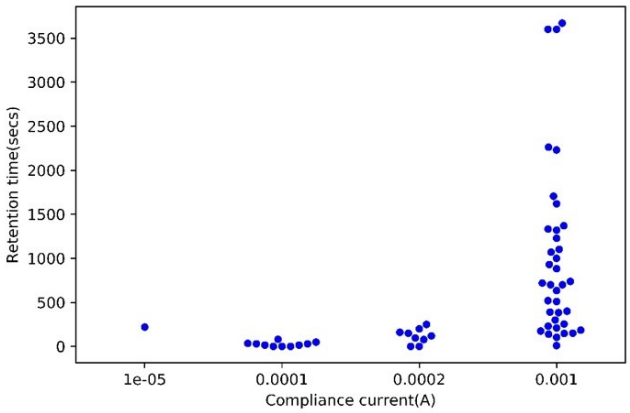


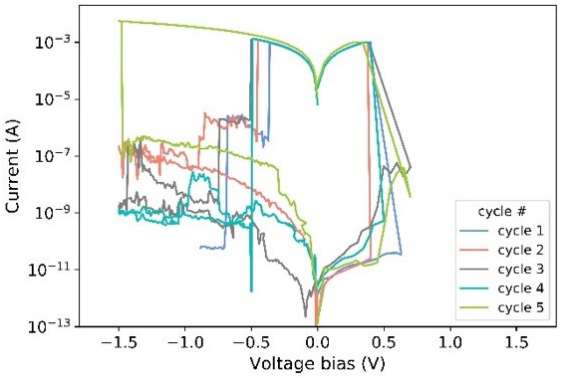
Figure 4. 5 Retention time data collected at compliance current of 10 µA, 100 µA, 200 µA and 1 mA shows that with increase in compliance current the retention time increases.

Our observations are in accordance with previous studies showing that retention time shows variability with compliance current. However, there is a tendency of having increase in the retention time with CC, which can be related with the increase in the area of the conductive filament **[6], [7]**. Moreover, data studies on resistive RAMs have also proven that retention time is stochastic in nature **[8][9]**.

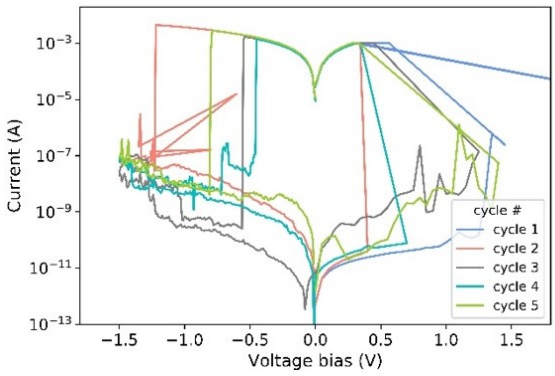
1.4. Electrical Characterization of doped devices

IV characteristics are performed on doped Polyethylene oxide (SPE) with 3 wt. % $AgClO_4.XH_2O$. A report by Wu *et al.* showed that doping of the SPE layer with Ag salt improved the retention time based on the availability on Ag ions for filament formation **[15]**. However, there are no reports on their IV characteristics. Hence, in order to study their electrical characteristics, such devices were fabricated.

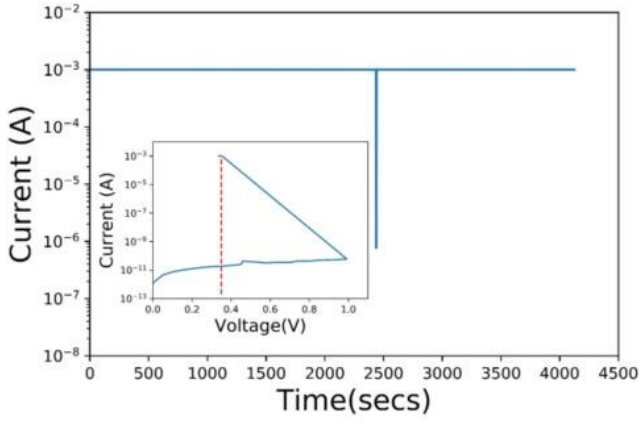
Figure 4. 6(a) & **(b)** reports the IV curves recorded on two devices (no. 17 & 19) with a set compliance current of 1 mA. It can be observed that the set switching took place at around 0.5 V for device no. 17 and at ~1.1 V for device no. 19, while the reset voltages took place within a voltage range between -0.5 and -1.5 V.



(a)



(b)



(c)

Figure 4. 6 IV characteristics of (a) device 17 & (b) device 19 with set compliance current of 1 mA. (c) Retention time measurement of a device set at a compliance current of 1 mA read at a constant voltage of 40 mV. Inset in Fig (c) shows the single set cycle performed before retention time measurement.

ON state retention time measurement was also evaluated at 1 mA compliance current, after subjecting the device to a single set cycle and at constant reading voltage of 40 mV. **Figure 4. 6(c)** shows the corresponding retention time measurement > 4000 seconds. Comparing the electrical performances of the doped and un-doped PEO CBRAMs, the switching voltages are quite similar with respect to each other. With the retention time measurement done only one time due to constraint in characterization time, the result is only indicative on the fact that the retention time increases with doping of the PEO layer. Moreover, further studies and tests would be required to conclude on the improvement on retention with doping

2. Morphological observation on planar devices

In this section, we present the morphological and chemical (EDX) observation and analysis done on the planar devices.

Firstly, observation is done on the un-doped planar devices with the help of optical microscope to visualize any changes at the surface of the Polyethylene oxide. Moving forward, devices are fabricated with silver salt-doped Polyethylene oxide (PEO) and observations are stated.

In previous research works on devices based on Polyethylene oxide (PEO) SEM images on the planar devices with gap distance at 0.5 μm, 1.0 μm, 2.0 μm, 5.6 μm and 8.0 μm are reported in order to study the mechanism of the growth of the conductive filament in the polyethylene oxide- solid polymer electrolyte (SPE) layer**[16], [17]**. Here, for the first time planar nano-gap devices with lateral nano gap sizes of ~100 nm are reported as these devices were fabricated using the shadow edge evaporation technique**[18], [19][20][21]**. The device fabrication is already discussed in **chapter 2** of this report.

2.1. Micrographs of planar un-doped devices

In an attempt to observe the microscopic changes close to the nano-gap region, images are taken on the pristine state of the devices and after cycling. **Figure 4. 10** shows the devices in pristine state (without cycling). The deposition of the solid polymer layer-Polyethylene oxide is noticeable throughout the area of the substrate with spots of dust. It is revealed through micrographs that on cycling the devices there is a morphological change taking place close to the region of the nano-gap as seen in **Figure 4. 7(b)-(f)** The protocol for cycling subjected on device no. 19 is as follows:

(i) Upto 10^{th} cycle, the CC is set at 10 μA. [**Figure 4. 7(b)-(c)**]

(ii) From 11^{th} to 25^{th} cycle, the CC is set at 100 μA . [**Figure 4. 7(d)-(f)**]

In these devices up to 10 cycles were performed at CC 10 μA; only positive set cycles were performed as on the backward sweep from +2V to 0V, there was an early reset at low voltages (~50 mV) due to volatile switching (with no requirement of negative bias to reset the device) as explained in detail in chapter 3. After 10 cycles, on applying higher CC set at 100 μA, the device has to be subjected to full set and reset cycles (+2 to -2 V) to reset it to high resistance state (HRS).

A darkening of the region in the proximity to the nano-gap can be observed which is probably due to the depletion of the Ag electrode or thermal effect or a combination of both. However, it should be inferred that there is certainly a change in region close to the nano-gap on cycling.

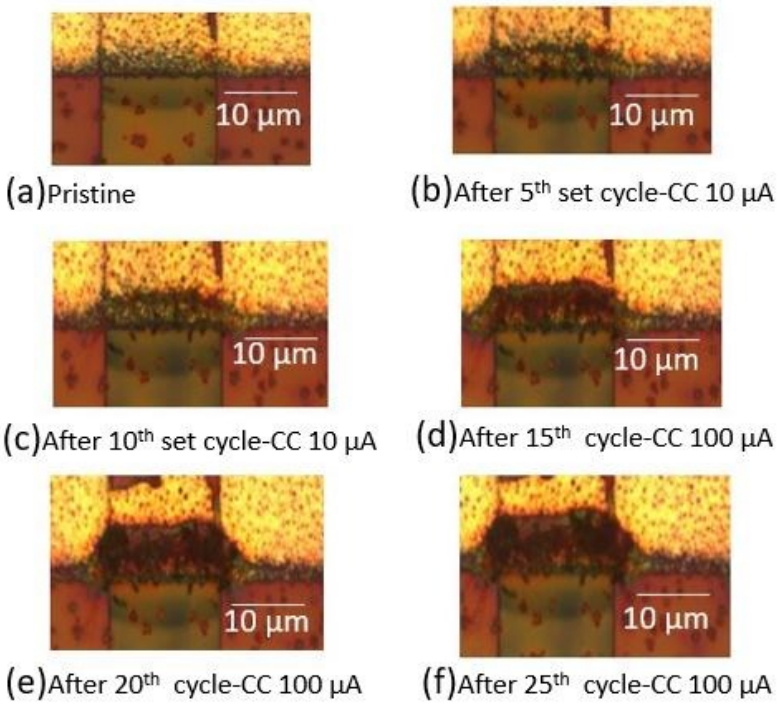


Figure 4. 7 Micrographs of device n°19 (width = 16 µm)(a) Pristine state (b) after five set cycles done at a compliance current of 10 µA; (c) after ten set cycles d) after fifteen full(set & reset) cycles (e) after twenty full cycles (f) after twenty five full cycles performed at a compliance current of 100 µA.

In an effort to visualize the effect of compliance current upon cycling of the devices, repeated cycles were performed on a device with a compliance current of 1.0 mA as shown in **Figure 4. 8(a)-(e)**. If we compare the images in **Figure 4. 7(f)**– 25 cycles with CC of 10 µA and **Figure 4. 8(d)**– 15 cycles performed at 1 mA for two different devices, it can be seen that the darkening and broadening of both the region in the proximity of the nano-gap region looks similar. The composition of the region close to the nano-gap was also studied and analysed through EDX measurement and included in the last section of this chapter.

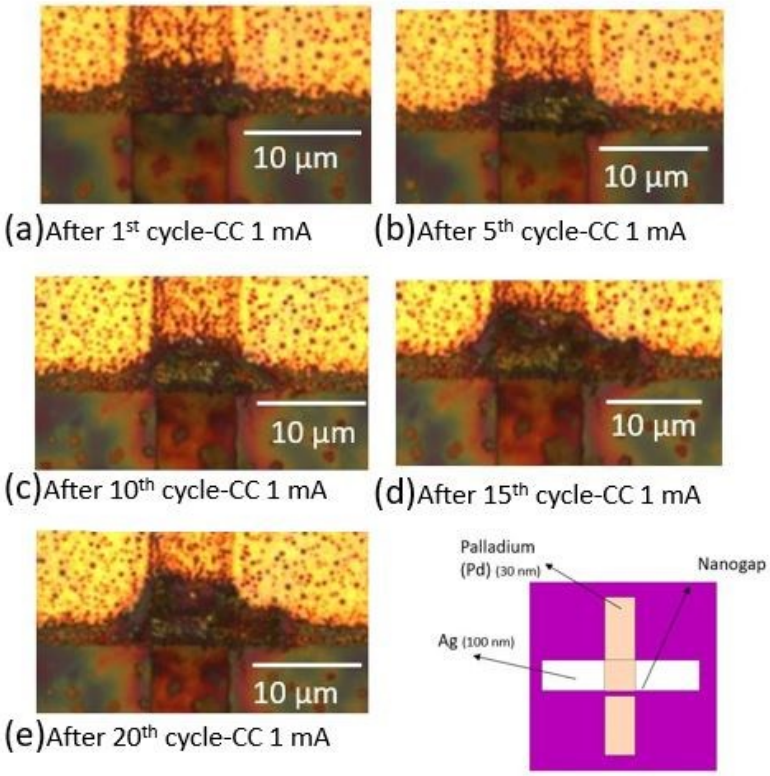


Figure 4. 8 Micrographs of device n° 14 (width = 8 µm) after (a) 1st cycle (b) 5th cycle (c) 10th cycle (d) 15th cycle and (e) 20th cycle set at a compliance current of 1 mA; also the orientation of the device is mentioned.

2.2. Micrographs of planar doped devices

In the pristine state of the doped devices, there is a pink colour change at the edges- possibly due to the formation of the compound Silver hydroxides (AgOH) which is brownish in colour. After consecutive cycles, it is observed that there is certain region of the nano-gap where the changes are prominent (in red arrows) as seen in **Figure 4. 9(b)-(e)**. It is to be noted that the device is subjected to similar number of cycles at set CC as for the un-doped devices shown in **Figure 4. 7** so as to make a comparative observation between them (doped and un-doped). The chemical analysis is shown in the EDX measurements section of this chapter.

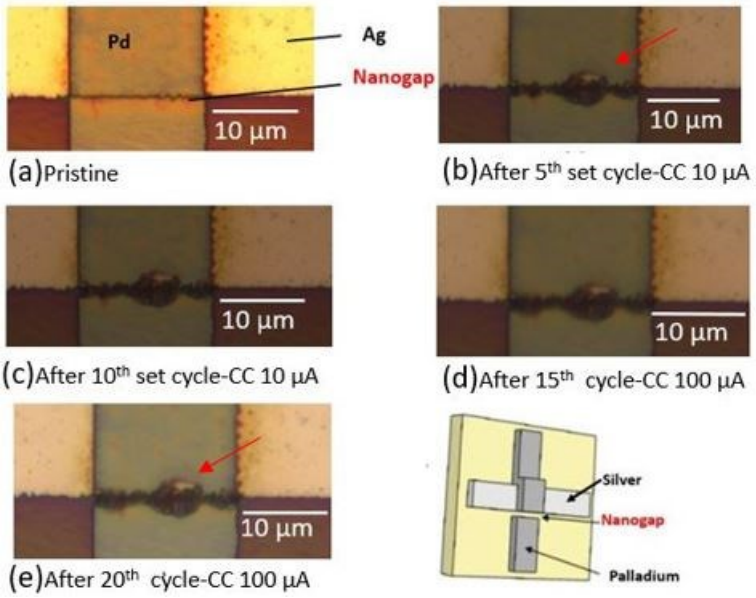


Figure 4. 9 Micrographs of a doped device (width = 16 µm) (a) in pristine state, (b) after five set cycles at a compliance current of 10 µA (c) after ten set cycles (d) after fifteen full (set-reset) cycles (set/reset) (e) after twenty full cycles at a CC of 100 µA. Also the orientation of the devices is shown.

2.3. Atomic Force Microscopy (AFM) images on planar devices

AFM images were taken close to the nano-gap region in tapping mode to visualize any morphological changes before and after cycling. The AFM observation experiment was set up on an un-doped device with a Pd counter-electrode (16 µm width). **Figure 4. 10(a)** & **(b)** shows micrograph images of the device in pristine state and after five consecutive cycles respectively, the corresponding IV curves are plotted in **Figure 4. 10(c)**. As observed in the previous section, the micrographs images show a darkening of the nano gap region after cycling.

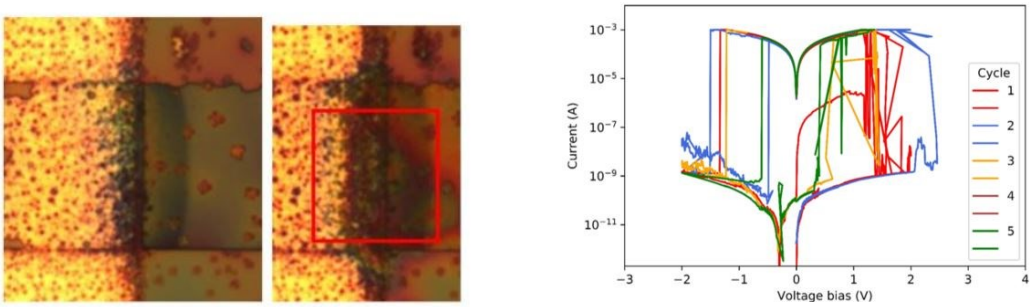


Figure 4. 10 Micrographs of device n° 11 in (a) Pristine state and (b) after five cycles and (c) corresponding IV curves.

Further, AFM topographic images and amplitude error images were taken in peak force quantitative non-mechanical mode with SCANASYST (Silicon Nitride cantilever tip) in the pristine state and after cycling of device n° 11. **Figure 4. 11(a)-(c)** show the topographic images while **Figure 4. 11(d)-(e)** corresponds to amplitude error images. The amplitude error image records signals how the tip gets deflected as it encounters topographic change. It is closely related to the topology of surface.

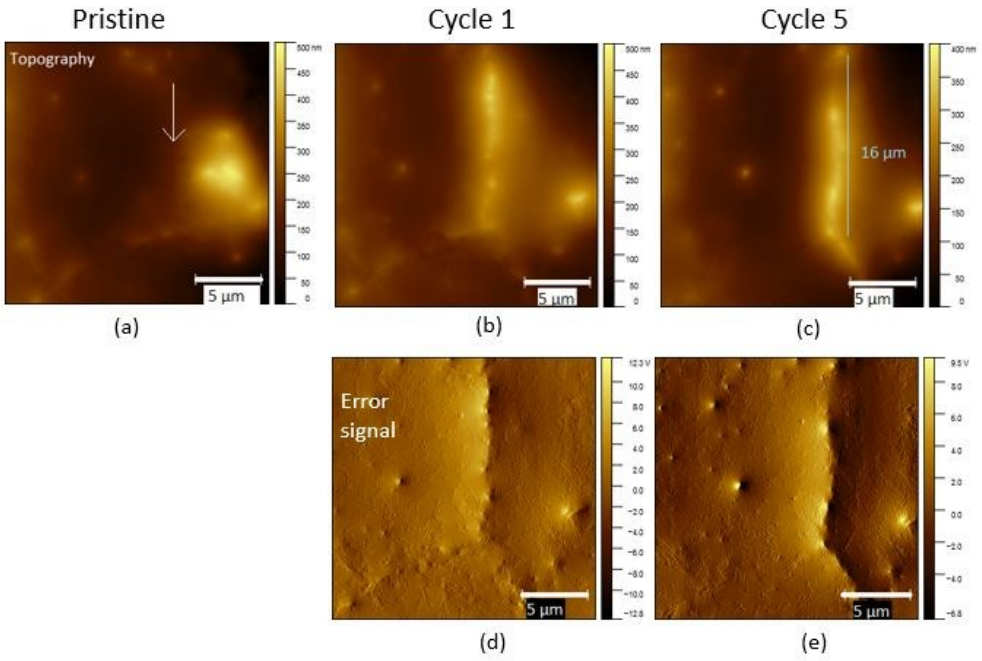


Figure 4. 11 AFM images of the nano-gap region of the device in their pristine state, after 1st cycle and after 5th cycle. (a)Topographic (d) Amplitude error images.

Through the topographic and amplitude error images a morphological change is confirmed close to the nano-gap region after cycling. The root mean square roughness of the PEO deposited on Pd is measured to be 236 nm & 154 nm before and after cycling respectively quantifying textural change. Moreover, from the AFM image in **Figure 4. 11(c)** & **(e)** it can be seen that the morphological change occurs close to the nano-gap region which is measured to be approximately 16 µm, this length corresponding to the lateral size of the Pd inert electrode.

The AFM images in **Figure 4. 11** look alike the PEO thin film morphology on CBRAMs as shown by Mohapatra *et al.***[22]**, however the morphology is different than that presented on the vertical structures [see **Figure. 2. 8, Chapter 2**]. Indeed, no fibril structure could be observed during these topographic images like before. One possible reason for such difference could be the fact that PEO in horizontal devices is deposited on top the Palladium electrode while our previous observations were achieved directly over the (Si/SiO_2) silicon substrate along with the resolution difference [500 nm in the **Figure 2. 8** and 5 µm in **Figure 4. 11**].

Finally, **Figure 4. 12(a)** & **(b)** show reconstructed 3D topographic images obtained from the height images close to the nano-gap region for the pristine and cycled device respectively. These images evidence a redistribution of the PEO layer after cycling. To conclude, the topographic images extracted from the nano-gap device shows changes after five cycles as depicted, which was not visible in the pristine state, hence this paves way to chemical analysis techniques to examine the devices.

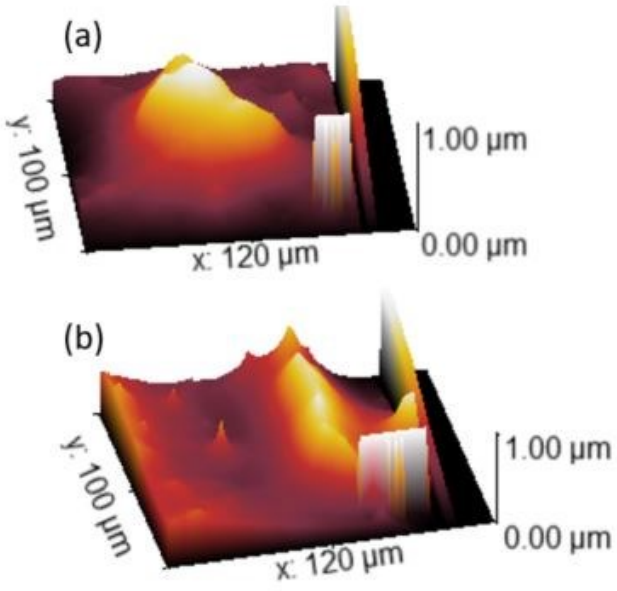


Figure 4. 12 3D topographic close to the nano-gap region (a) in pristine state (b) after cycling

3. SEM/EDX analysis

Krishnan *et al.* have successfully exploited Scanning Electron Microscope (SEM) images on PEO based planar CBRAMs to analyse their memory structures **[16], [17]** (see **Chapter 1**). In these papers, the filamentary growth of Ag is seen to be clustered type for PEO and dendrites type for Ag + PEO based planar device structures with for gap lengths of 0.5, 1 & 2 µm. Taking a reference from such studies, SEM images were performed on the devices to observe the region close to the nano-gap before and after cycling. Energy Dispersive X-Ray (EDX) measurements were simultaneously performed on the devices to chemically analyse the elements across different profiles.

3.1. Analysis of un-doped planar devices

As observed in the **Figure 4. 12** , showing the topographic images of the lateral devices, the goal is to answer the two following questions :

a) Can we observe any morphological changes close to the nano-gap region?

b) Can we identify and/or quantify the changes through chemical analysis?

3.1.a.Observation on a pristine device

The SEM and EDX images were taken on Quattro ESEM (*ThermoFisher scientific*) ultra-high resolution SEM instrument as depicted in **Figure 4. 13** and **Figure 4. 14** respectively. The lateral resolution of the SEM is 50 nm; with an accelerating voltage of 20 kV for EDX measurements.

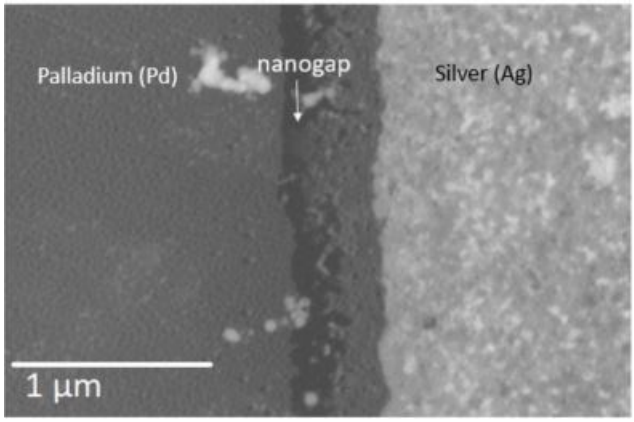


Figure 4. 13 Shows the SEM image of the device no. 16 with nano-gap device.

The SEM image along with the chemical composition in **Figure 4. 14** of the elements reveal that there is no pre-existing Ag in the nano gap region. The image shows a clear contrast between the nano-gap, the Pd and the Ag electrodes. The Ag concentration (in pink) in the region of the device can be confirmed with the EDX chemical analysis as shown in the **Figure 4. 15(f)**.

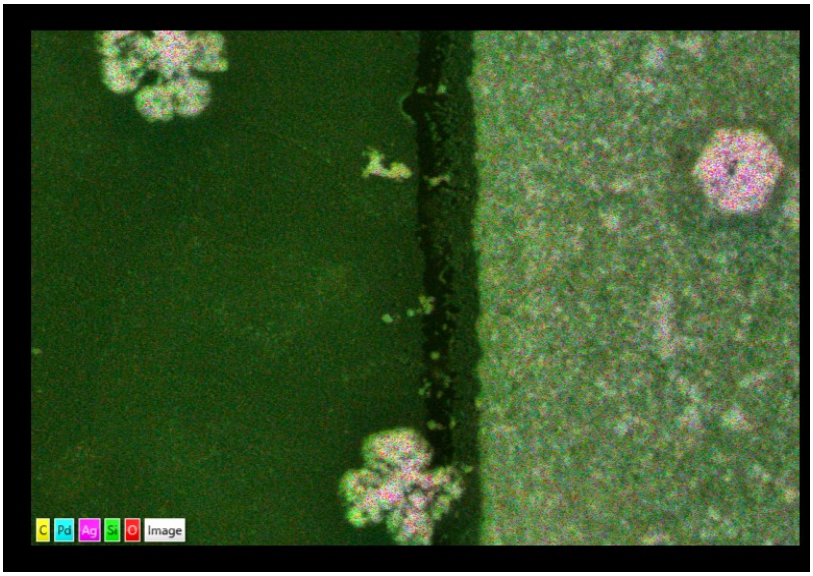


Figure 4. 14 EDX image of the pristine device with mapping of the all elements - C, Pd, Ag, Si and O.

Figure 4. 15(c) presents the Si element mapping which shows a colour demarcation due to two different electrodes on the two sides. Further, through these filtered EDX images of the device shown in the **Figure 4. 15(e)** & **(f)**, the presence of the electrodes Pd, Ag with the nano-gap is clearly visible with the colour contrasts. However, it can be seen that there are three Silver and Chloride flowers on the Pd electrode and Ag electrodes as observed in **Figure 4. 15(d)** & **(f)**. The source of Ag, Cl elements is not yet to be precisely known, but possibly can be a result of contamination from the fabrication processes or storage. However, from the images obtained here, it is confirmed that there are no silver filaments in the nano-gap region.

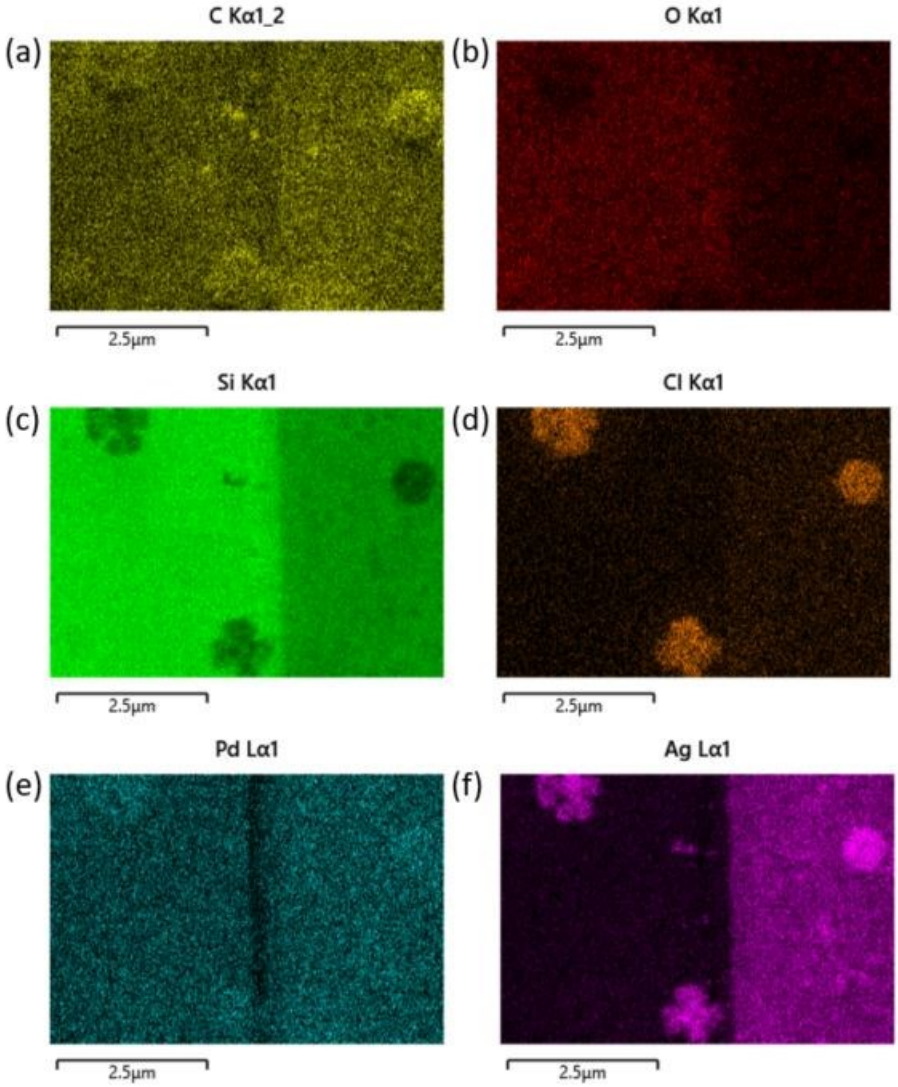


Figure 4. 15 Filtered EDX images of the pristine device no. 16 with mapping of the elements (a) Carbon-C, (b) Oxygen-O, (c) Silicon-Si, (d) Chloride-Cl, (e) Palladium (Pd) and (f) Silver (Ag).

3.1.b.Observation of cycled devices

A device (Pd electrode width 16 µm, device no. 18) featuring an un-doped PEO layer was then cycled for five IV cycles with a compliance current set at 1 mA. As shown in **Figure 4. 16(a)**, SEM image shows dendrite-like structures extending over the nano-gap

region. From Pd, Ag-filtered EDX measurements of **Figure 4. 16(b)&(c)** it is evident that those dendritic structures can be attributed to silver element,

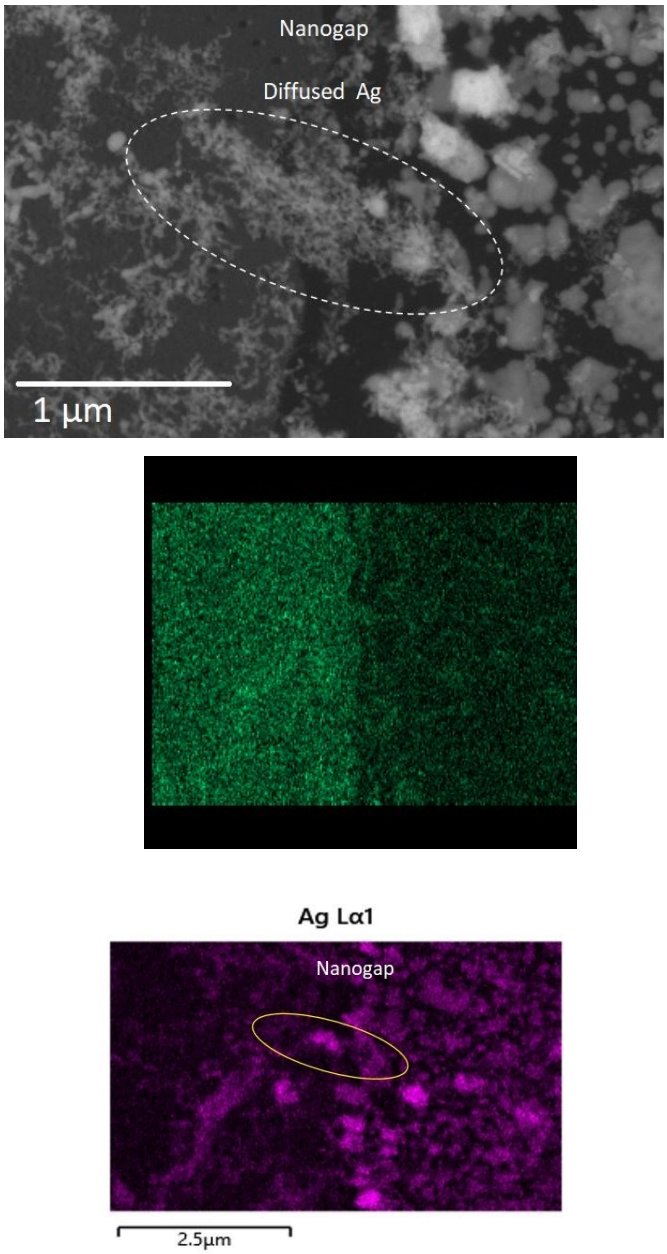


Figure 4. 16 (a)SEM image of the cycled nano-gap device no. 18 , with Ag diffused through the nanogap into the Pd electrode, filtered EDX image of the device showing (b)Palladium (Pd) (c) diffused Silver (Ag) in the nano-gap region (marked in yellow circle).

bridging the vertical Ag electrode (left) and the horizontal Pd counter-electrode (right). Similarly, diffused Ag clusters can also be seen through the nano-gap after five cycles

performed on another device (8 µm Pd electrode width) as observed in **Figure 4. 17** reconfirming the presence of Ag filament on cycling. Krishnan *et al.* in their work have shown that filament formation consists of Ag clusters which were randomly distributed throughout the PEO matrix, with connections between the electrodes at several locations **[17]**. For such devices the compliance current was set at 400 µA. In conjunction with results presented in **Chapter 3** on vertical devices evidencing ohmic type of conduction for the devices in the low resistance state (LRS), our physical and chemical analyses revealed Ag filament formation between the electrodes through the nano-gap region.

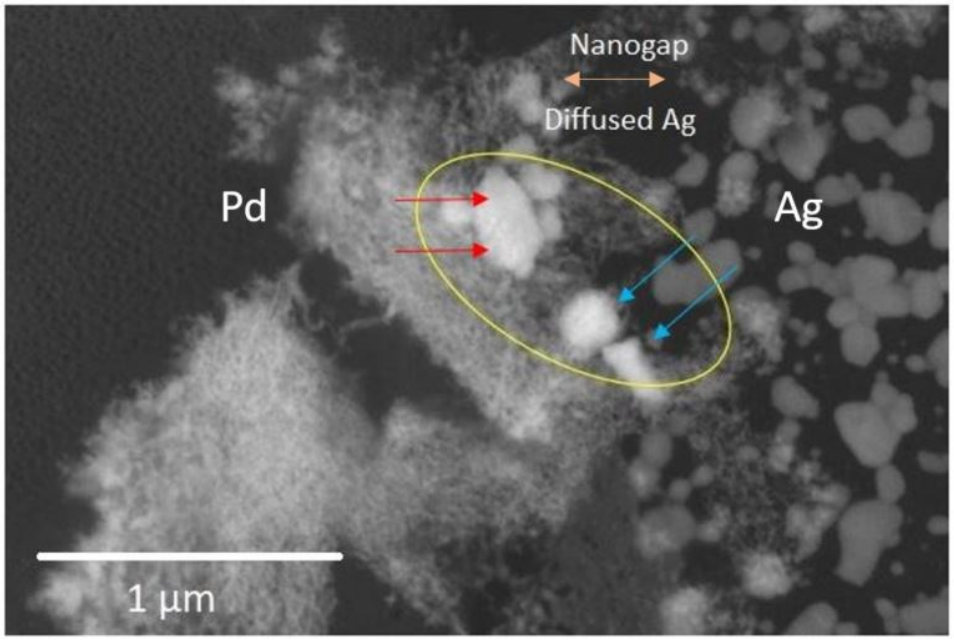


Figure 4. 17 SEM image of another cycled device no. 17, showing diffusion and clustering (red and blue arrows) through the nano-gap region.

3.2. Analysis of doped planar devices

3.2.a.Observation on a pristine device

SEM observation of a pristine Ag- doped device was done and two EDX profiles were extracted along cross-sections through the nano-gap. The chemical profile of the elements are shown in **Figure 4. 18**. From the profile, the two electrodes Ag and Pd are clearly distinguishable. Moreover, with such analysis it can be seen that the Ag concentration is very low in the nanogap region.

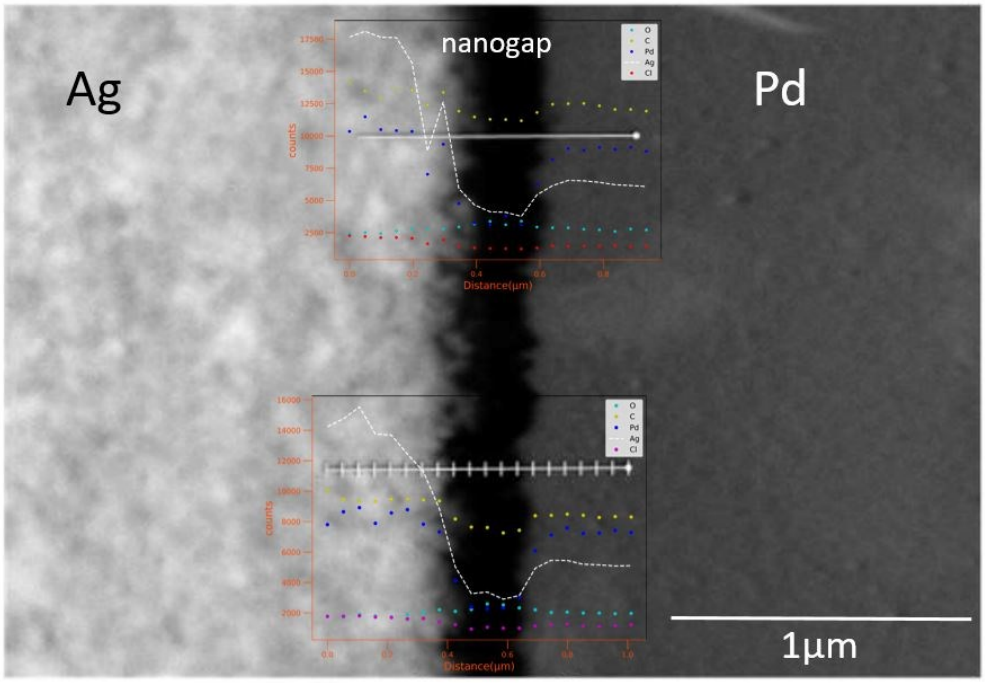


Figure 4. 18 SEM image of a pristine doped nano-gap device n° 14 along with two chemical profiles extracted from EDX measurements from the Pd electrode (left) to the Pd/Ag electrode (right) over the nano-gap region (centre).

3.2.b.Observation on cycled doped device

Current voltage measurements recorded on the doped device for five cycles are shown in **Figure 4. 19**.

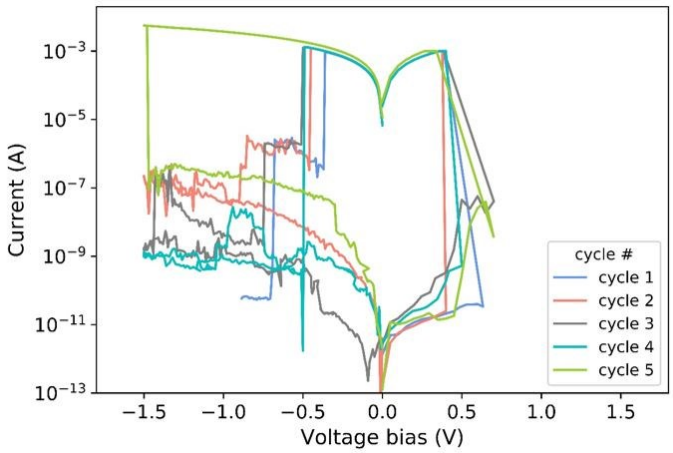


Figure 4. 19 IV curves recorded on a doped PEO nano-gap device n° 17 along with five cycles.

The corresponding SEM image was taken consecutively and is presented in **Figure 4. 20**. Interestingly, a neat dendritic structure bridging the nano-gap region was successfully observed. Upon chemical analysis, the profile in the nano-gap region confirms a spike in Ag element confirming the fact that a filamentary conduction takes place in the device.

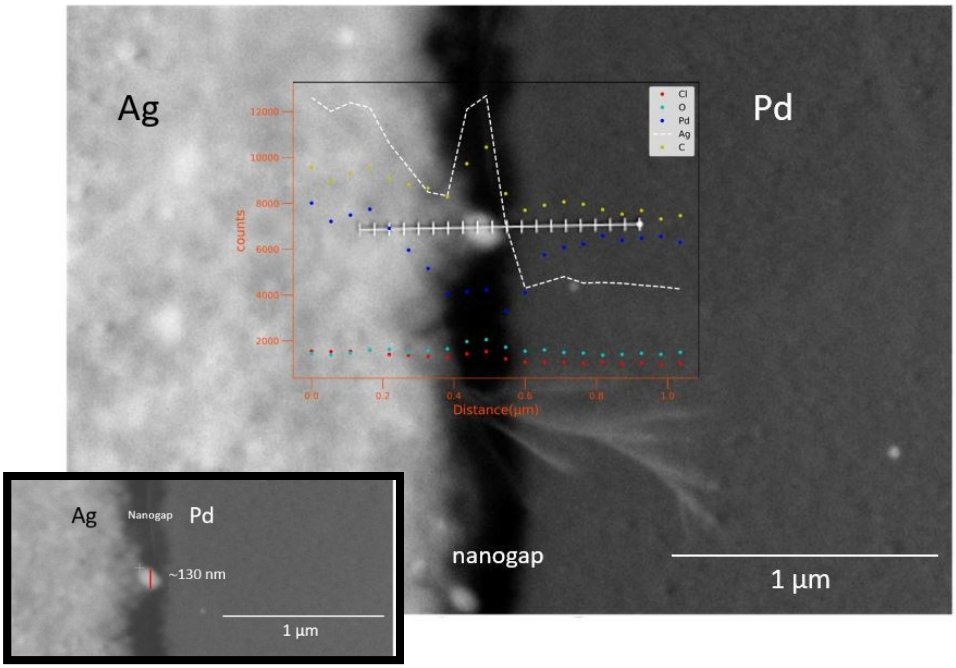


Figure 4. 20 SEM image of the cycled doped nano-gap device n° 17 along with the chemical profile of the elements in the Pd on Si, nano-gap region and the Pd& Ag on Si region. EDX profiles reveal unambiguously that and Ag dendritic structure was formed over the nano-gap region. Inset shows the filament diameter ~130 nm.

4. Conclusion to the chapter

This chapter describes the electrical performance of the nano-gap devices with respect to set/reset voltage statistics done on twelve devices. The endurance capabilities on these devices was found to be close to 70 for full IV sweep cycles and up to 80 cycles along with pulse measurements. Furthermore, by setting the compliance current at 10 µA, 100 µA and 1 mA, multilevel states can be achieved similar to that shown for vertical devices. It can also be observed that 10 µA compliance current also resulted in volatile type of switching.

As planar devices, provide us an opportunity to examine morphological changes around the region of the nano-gap device, through optical microscope, atomic force microscope, scanning electron microscope and energy dispersive X ray instruments are utilized to characterize the devices. Through the micrographs done on the un-doped and doped devices, the region in proximity to the nano-gap was analysed before and after few cycles. A darkening of the region was visualized by optical microscopy after few cycles, indicating the fact that there are certain changes occurring in the nano-gap region. A comparison is done with respect to the set compliance current and the number of cycles performed on the devices. AFM images were carried out before and after cycles equally suggest that there are changes, confirmed also through the elevation profile in the nano-gap region and its vicinity.

This leads to the examination of the nano-gap region with SEM images and EDX measurements. Through SEM images, it can be reconfirmed that there is a diffusion of silver (Ag) in the nano-gap region after cycling. EDX measurements providing the chemical analysis of the elements present in the device show that Ag is the element resulting into filamentary formation in the nano-gap region. Similarly, done on the doped nano-gap devices, through SEM and EDX measurements, the results successfully revealed dendritic Ag filament creation after cycling, demonstrating the fact that our devices are filamentary based. Chemical profile of the elements in the cross section region are provided before and after cycling.

5. References

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Chapter 5 – Polymer-based CBRAMs on flexible substrates

In this chapter, PEO-based CBRAM devices fabricated onto flexible substrates are studied. After describing the experimental setup for electrical characterization and mechanical testing, the performance of the devices- namely IV characteristics, programming voltages, endurance and retention time of the devices is presented. Since flexible substrates can be used on curved surfaces and under mechanical stress, hence results on the mechanical tests performed on the devices are also reported.

In the final section of the Chapter, a comparative study on the performances of the devices is done with respect to area, compliance current and study on conduction mechanism on flexible substrate.

1. Studied devices and experimental setup

1.1. Studied devices

The complete fabrication procedure of the flexible CBRAM devices has been described in C**hapter 2**. The thickness of the PEO layer used in the studied devices is 140-160 nm. The masks used to fabricate these devices are shown in **Appendix D- Figure D2 (Mask 2)**; they consist in cross bars of size 35x35, 50x50 & 100x100 μm^2 respectively.

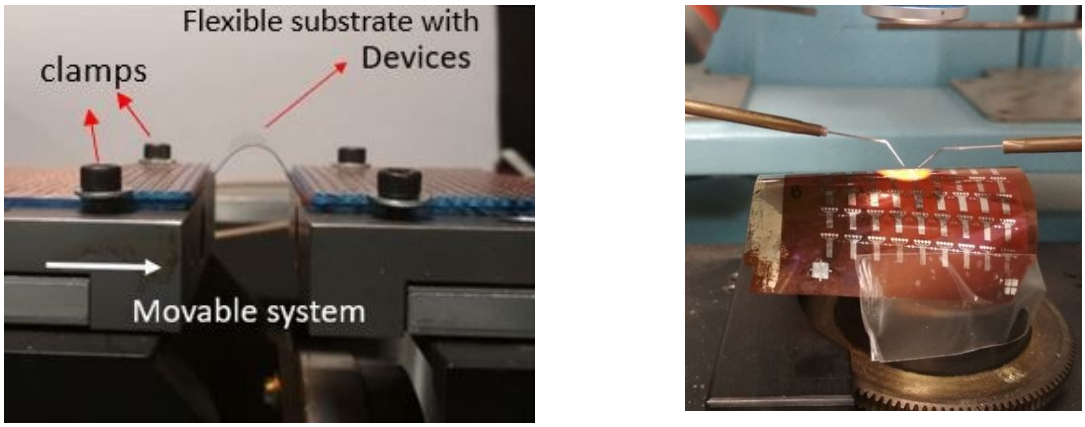
1.2. Electrical and mechanical characterization setup

As explained in chapters 2 and 3, current-voltage characteristics are performed with a Keithley 4200A SCS through voltage sweep biases from 0.0 to ±2.0 V. The compliance current was set either at 10 or 100 µA for endurance measurements. Retention time measurements were conducted in the following manner: firstly, having a single set voltage sweep at a given compliance current and then subjecting the device to current-time measurements at a constant reading voltage.

The samples were also subjected to tensile strain by mechanical bending in two different configurations: buckling and conformational contact [see **Figure 5.1(a)** & **(b)**].

i) Fatigue tests were first performed in a *buckling configuration*. The flexible substrate was clamped to one end on an immobile support and on the other end to a mobile arm of the mechanical bench. The devices can be then subjected to tensile strain through

longitudinal and periodical translations of the movable arm. The curvature radius at the centre of the bended substrate can be adjusted by setting the distance between the arms while the oscillation frequency and the number of bending cycles can be chosen independently. The fatigue test presented in this chapter was performed at a frequency of ~0.7 Hz over more than 10^4 cycles. The device fatigue is analysed through IV characteristics performed after the bending cycles. A photograph of the set up is shown in **Figure 5.1(a)**.



(a) (b)

Figure 5. 1 Setup for mechanical stress tests-(a) buckling configuration- the two ends of the substrate can be clamped to the mobile arms of the system in such a way that the devices on which the tensile strain tests to be applied is at the top of the bend. (b) Mechanical stress tests through conformational contact - showing in situ IV characterization of the devices.

2. Electrical characterization of the devices

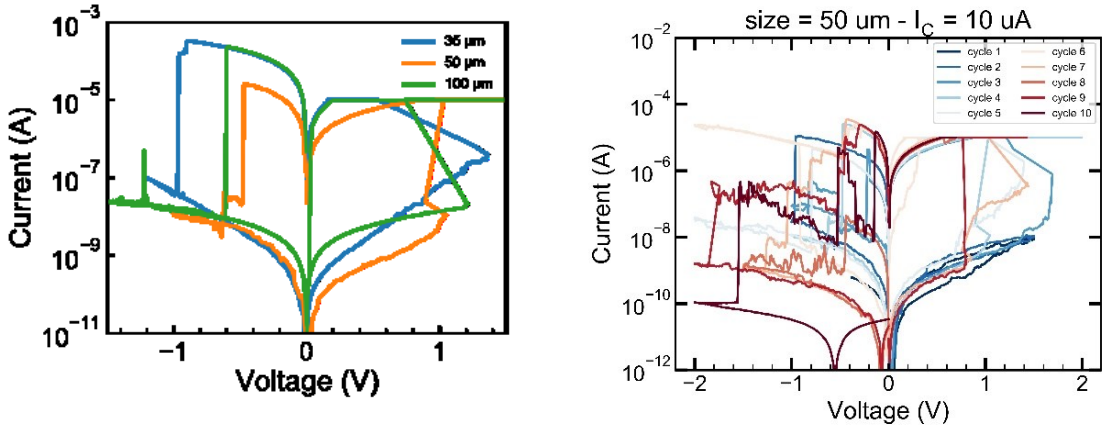
In this section, the performance of the flexible CBRAM devices are discussed with respect to set/reset voltages, endurance and retention time. Finally, the effect of area and compliance current on the devices fabricated on Si/SiO_2 and flexibles is compared through box plots.

2.1. SET/RESET voltage statistics

The current voltage measurements- Switching of the devices shown with 35x 35, 50x 50 and 100x 100 μm^2 cross bar areas shown in **Figure 5. 2(a)** with a set compliance current at 10 µA. **Figure 5. 2(b)** shows 10 set/reset cycles performed on a 50 x 50 μm^2 device with a 10 µA compliance current.

Upon cycling, multilevel switching is observed through abrupt current drops in the I-V characteristics. This phenomenon may be attributed partial ruptures of the conductive

filament, such as dendritic patterns or ramifications observed in the previous chapter (**Chapter 4, section 3.1.2.**) and in the literature **[1]**.It can also be observed that the switching cycles are not controllable from cycle to cycle and are also prone to intrinsic variability. However, switching voltages of the device are similar to those obtained on the Si/SiO_2 devices [refer **section 2. in Chapter 3**] ranging from -1.5 V to 1.8 V as compared in **Figure 5. 3** hence confirming workability at low voltages.



(a) (b)

Figure 5. 2(a) Set/reset cycles on devices of 35x35, 50x50 & 100x 100 µm²area respectively on flexible substrate, (b) shows ten consecutive cycles on a 50x 50 µm²device with CC of 10 µA.

The plots consists of 78 set and 21 reset on Si and Kapton devices each with cross bars of 30 µm and 35 µm respectively.

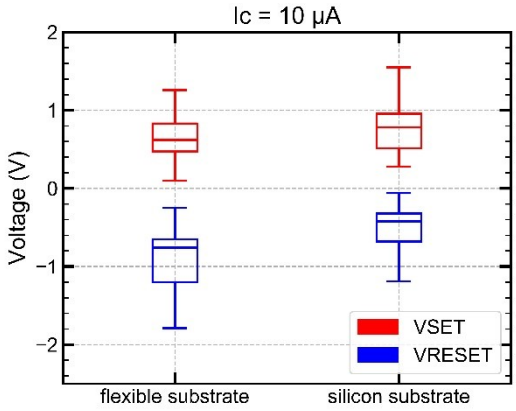


Figure 5. 3 Box plot distribution of 78 set & 21 reset voltages on six devices, each on Si and Kapton substrate with 30 & 35 µm cross bars areas respectively.

2.2. Endurance measurement and programming window

Endurance measurements were conducted on a device along full voltage-sweep cycles by applying voltage biases from 0.0 to ±2.0 V. The compliance current was set at 100 µA while the reading voltage was set to 50 mV. **Figure 5. 4** illustrates the performance of a device showing an OFF/ON resistance ratio greater than 10^4. After 300 programming/erasing cycles the OFF/ON resistance ratio decreased to 10 and the device then failed after 325 cycles due to short circuit.

Figure 5. 5 (a) & **(b)** respectively show the evolution of LRS/HRS resistances obtained during endurance cycling together with their cumulative probability plots. It is noticeable that with a100 µA compliance current, a stable ~ $3x10^4$ OFF/ON resistance ratio was achieved until the sudden drop of the HRS resistance. These results are comparable to the research work by G. Vescio *et al.* on HfO_2 based ReRAMs OFF/ON with resistance ratio >$10^3$and low voltages on flexible substrates **[2]**. These results can also be compared to our CBRAMs on silicon substrate exhibiting more than 300 cycles with a ~ 10^4 OFF/ON resistance ratio (see **Chapter 3**).

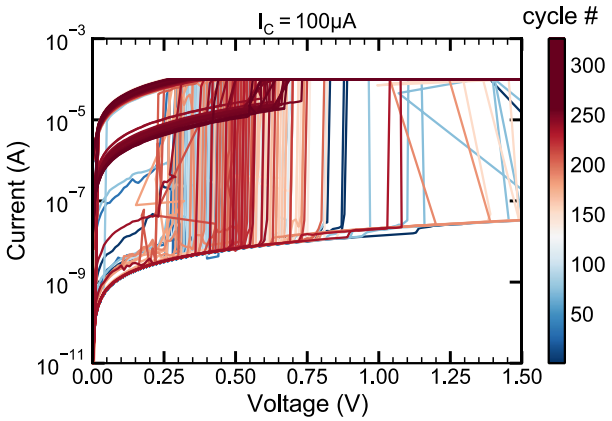


Figure 5. 4 Presents the set cycles done on the device at 100 µA compliance current on a device fabricated on Kapton.

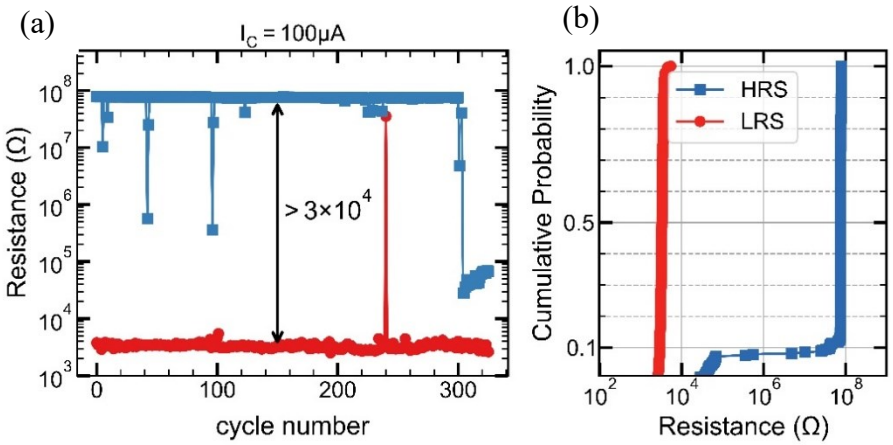


Figure 5. 5 (a) Shows the endurance cycles performed at 100 μA and (b) cumulative probability of the LRS and HRS plots showing a consistent OFF/ON resistance ratio.

Finally, with the box plot of the devices showing the ratio of standard deviation (σ) & mean (μ) value of the resistances are presented in **Figure 5. 6** at compliance current of 10 and 100 μA. The results are coherent with the fact that at 10 μA the variability of the LRS (22.8%) is higher than compared to that at 100 μA (9.8%), similar to the results on silicon [see section 3, **Chapter 3**]. Where variability parameter is presented as the ratio between the standard deviation σ over the mean value μ.

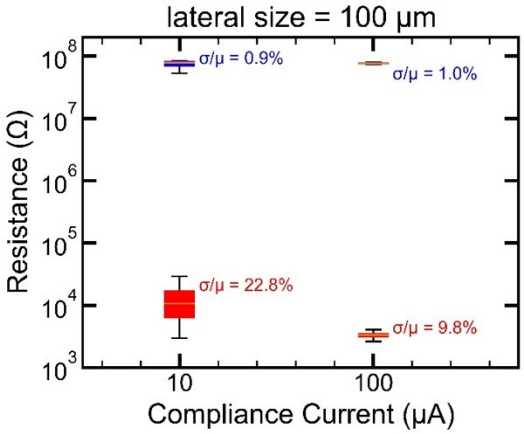


Figure 5. 6 Shows the box plot with the ratio of б/μ values at two compliance current 10 & 100 μA.

2.3. Retention time

The retention time of both LRS and HRS states was evaluated at a set compliance current of 1.0 mA. After programming the device in the LRS, a current vs time measurement is performed at a specific reading voltage biases. **Figure 5. 7**. shows the retention time measurements obtained at reading voltages from 20 up to 80 mV.

The retention time results are similar in terms of variability, to that of CBRAMs on silicon substrate [see **Chapter 3, section 2.2.5.**]. Conventionally, as expected when read at 80 mV the retention time (>2000 seconds) is higher as compared to when read at 20 mV (~600 seconds) or 60 mV (~900 seconds), however the variability in reading evidenced is when measured at 40 mV the retention time (>2000 seconds). Initially, these measurements were performed to extrapolate and find the retention time at a 0 V applied voltage. However, due to insufficient number of readings this was not achievable.

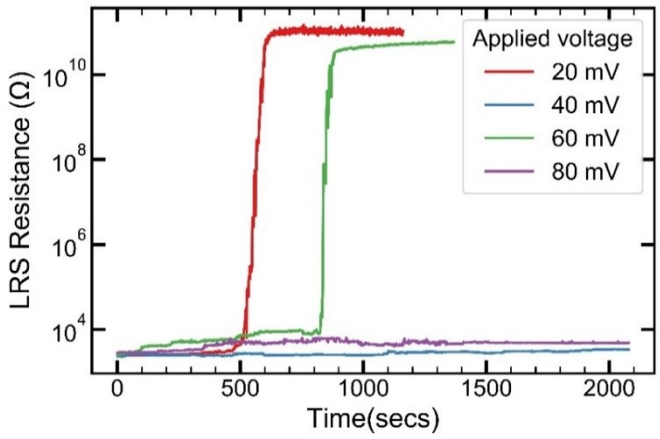


Figure 5. 7 The retention time of a device at a set compliance current of 1 mA measured at constant voltage 20, 40, 60 and 80 mV.

3. Electrical characterization under mechanical stress

3.1. Bending cycles

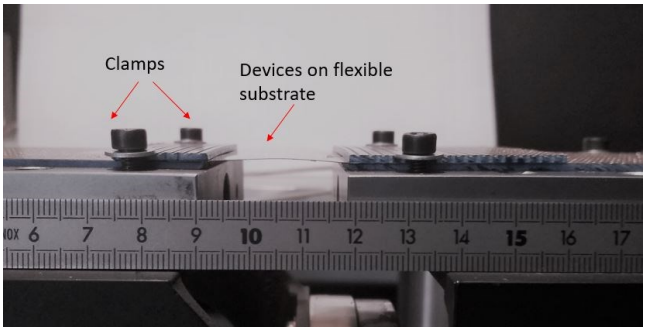
Bending tests in buckling configuration were performed to examine the fatigue of the devices. The setup is depicted in **Figure 5. 8(a)** & **(b).** The bending radius is

measured (from the centre to the edge of the curve). The bench was calibrated in our lab in 2017 by Puyoo *et. al* **[3]**. The strain % is calculated with equation (1) as

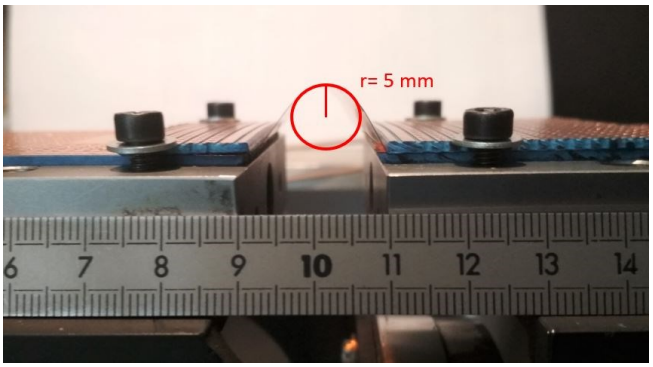
$$\varepsilon = \frac{t}{t+2r} x\ 100 \qquad (1)$$

Where ε is the strain %, t is the thickness of the flexible substrate – 125 µm, r the bending radius 5 mm **[3]**.

Here, tests were performed at a bending cycle rate of 0.7 cycle/second and a maximum strain of 1.2% at the top of the bend. Current voltage measurements were taken on flat surface after each 1st, 10th, 100th, 1000th and 10000th bending cycles.



(a)



(b)

Figure 5. 8 (a) Shows the setup for testing the bending resistance of the devices under no stress. (b) Shows the setup with measurement of the bending radius, r, when the devices subjected to maximum tensile strain.

As seen in **Figure 5. 9** the six devices show resistance to stress tests with a resistance OFF/ON ratio window greater than 10^2 even after 10^4 bending cycles. Previously, Mohapatra *et al.* reported bending cycles on PEO based devices with a maximum bend radius of 1.0 mm with a step of 0.2 mm, with a maximum compressive & tensile strain of

0.65% **[4]**. Their results illustrated very stable switching behaviour without deterioration proving the mechanical flexibility of the PEO film.

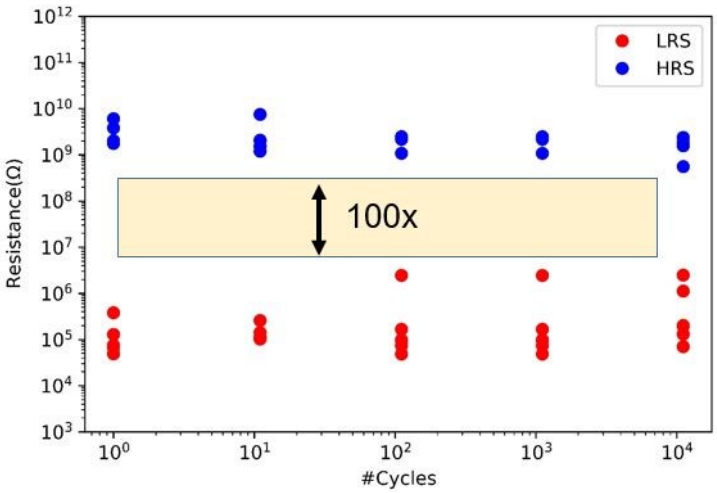
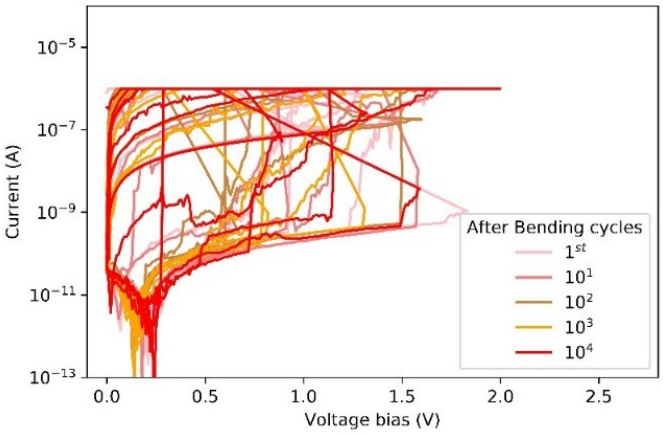
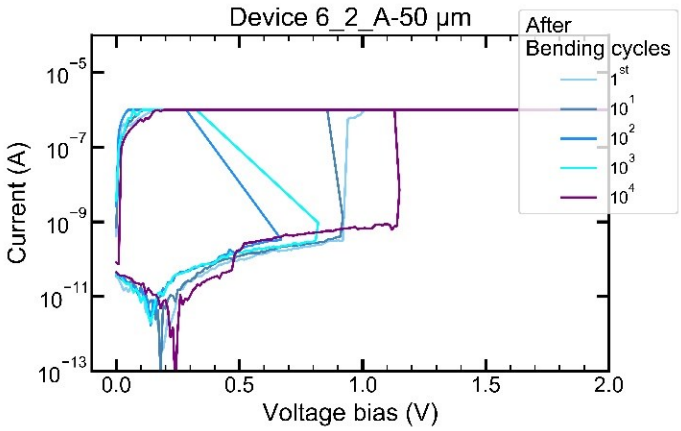


Figure 5. 9 Illustrates the bending cycles' performance on six devices, showing OFF/ON resistance ratio window of >10^2 even after 10^4 bending cycles.

Figure 5. 10(a) & **(b)** present the IV characteristics measured on all the six devices and on one of the devices respectively, after every 1st, 100th, 1000th and 10000th cycles. It can be observed that the switching voltages are low (< 1.6 V). The CC for such measurements are set at 1 µA, to prevent the devices from breakdown. Consequently, no negative voltage bias is applied to the devices to reset them as at this CC, volatile switching is observed. Additionally, low CC restrains the OFF/ON resistance ratio by limiting the LRS, which is however high (> 10^2) with a slight deterioration upon number of bending cycles.



(a)



(b)

Figure 5. 10 Presents the corresponding IV cycles for all the six devices after every 1st, 100th, 1000th, 10000th bending cycles for (a) all six devices and for (b) one device respectively.

3.2. Cell programming under mechanical bending

Stress performance of two of the devices is illustrated in **Figure 5. 11 (a)** & **(b)**, where they were characterized in situ, after 10^4 bending cycles performed on them on flat surface and bend surface respectively. The range of voltage switching varied from ±2.0 V making the devices suitable also for curved surfaces. The strain% as calculated in this case is 0.38% with equation (1) when placed in conformational contact with the bend with a diameter of 33 mm. **Figure 5. 12** presents the IV characteristics of the devices on flat and bend surface respectively. The results especially, done on bend surface show that the switching from HRS to LRS is very

consistent without deterioration in the high OFF/ON resistance ratio ~10^5. To mention that the number of set and the reset cycles are not equal because of volatile switching exhibited by the devices as the tests were performed at a CC of 10 µA [**Figure 5. 12**].

Table 5. 1 presents the number of set and reset operations performed on bend and flat surface. Remarkably, the devices showed higher non- volatility on the positive switch when characterized on the bend surface.

Programming	**Number of set**	**Avg. Set value**	**Number of reset**	**Avg. reset value**
On flat surface	27	0.85	7	-0.62
On bend surface	32	1.06	21	-0.77

Table 5. 1 Summary of the set/reset cycles of the devices on bend and flat surface.

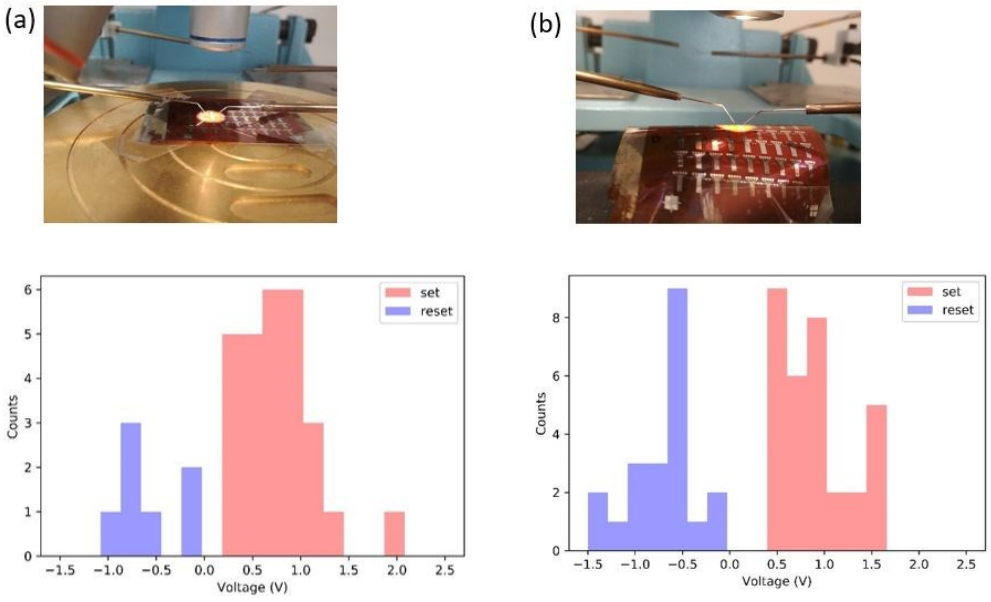


Figure 5. 11 Depicts the setup and switching voltages for IV characterization done on the (a) flat surface, (b) bend surface (diameter 33 mm) after 10^4 bending cycles performed on two of the devices.

However, only two devices were subjected to such tests, the results suggest that the devices are workable also on curved surfaces or under stress.

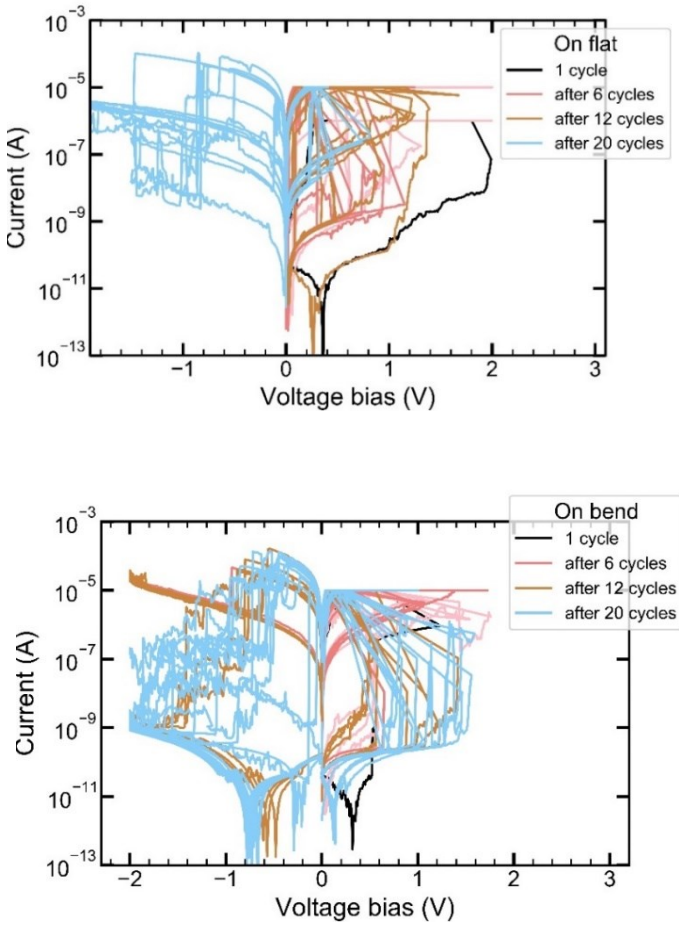


Figure 5. 12 Presents corresponding IV characterization of the two devices done on (a) flat surface -27 set, 7 reset cycles (b) on the bend surface (diameter 33 mm)- 32 set,21 reset cycles, after 10000th bending cycles performed on them.

4. Effect of area and current compliance: comparison between flexible and silicon substrates

Given that throughout this work, we have collected, electrical measurements on CBRAM of various area and fabricated on two kinds of substrate, this presents us an opportunity to compare the high and low resistance states together with set/reset voltages

for various current compliances, device area and substrates. The data collection used to perform this analysis on both CBRAMs on silicon and kapton is described in **Table 5. 2**.

		Flexible substrate (kapton)	**Si/SiO₂ substrate**
Size [µm]	**Icomp [µA]**	**# of measurements**	
35(flex. sub) 30(Si/SiO₂)	10	59	467
	100	-	351
50	10	56	95
	100	-	159
100	10	122	30
	100	282	-

Table 5. 2 Summary of measurements considered for statistical analysis

In Chapter 3, we showed that as the current compliance is decreased below 100 µA, volatile switching may occur leading to inconsistent LRS values [see **Chap. 3, Fig. 3.8, page 93**]. In the following, volatile switchings were excluded in order to focus on regular non-volatile switching.

4.1. Impact on LRS and HRS

Previous works on CBRAMs have shown dependency of high resistance state on the device area, especially for large devices (>10 µm), with the relation that the HRS scales together with the inverse of cell area **[5]**. Conversely, the resistance in LRS is mainly controlled by the current compliance, should not exhibit significant variation with respect to area**[5]**.

Figure 5. 13(a) &(b) show the evolution of both resistance states measured on flexible and silicon substrates respectively, as function of the inverse of the device area for both compliance currents. Note that boxplots corresponding to each compliance current have been voluntarily spaced horizontally to allow their comparison.

Besides electrical variability, we confirm that there is no clear tendency regarding the evolution of LRS resistance with respect to device area on either flexible or silicon substrates. Looking at the evolution of LRS at various current compliance on silicon

substrate (30 and 50 µm) and kapton (100 µm), we also observe that programming current is the main parameter governing LRS value.

Regarding the HRS, resistance values measured on silicon substrates globally scale together with the inverse of the area and for both compliance currents. Given the large size of our devices, this can be understood as the charge transport in HRS being mostly dominated by the area besides the switching region. This tendency is less evident on flexible devices, although we observe a clear increase in HRS resistance between 100 and 50 µm-width devices.

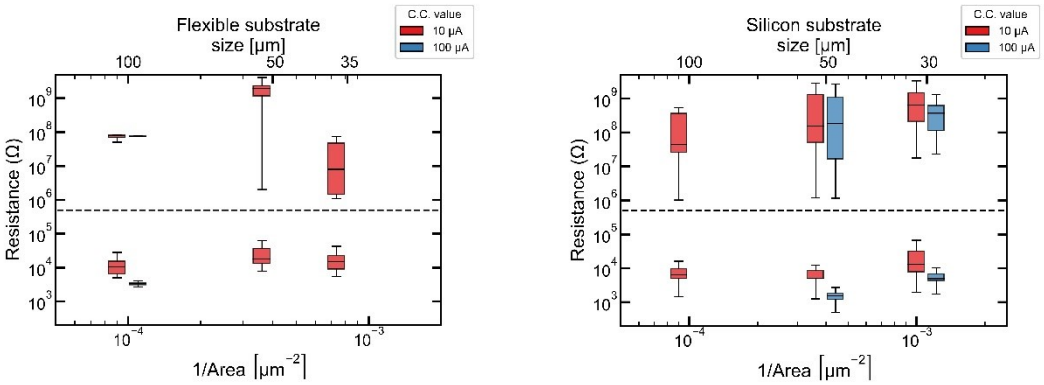


Figure 5. 13 HRS and LRS box plot for devices fabricated on (a) flexible and (b) silicon substrate for compliance current (CC) set at 10 & 100 µA.

4.2. Impact on programming voltages

The evolution of programming voltages for both types of substrates as function of the size and the device area is shown in **Figure 5. 14(a)&(b)** .We cannot observe any clear tendency regarding the evolution of the mean set voltage as a function of the device area for both substrates: the mean Vset fluctuates between 0.5 and 0.8 V for all sizes while the mean Vreset remains close to ~ -0.5 V except for 100 µm-wide devices on flexible substrates.

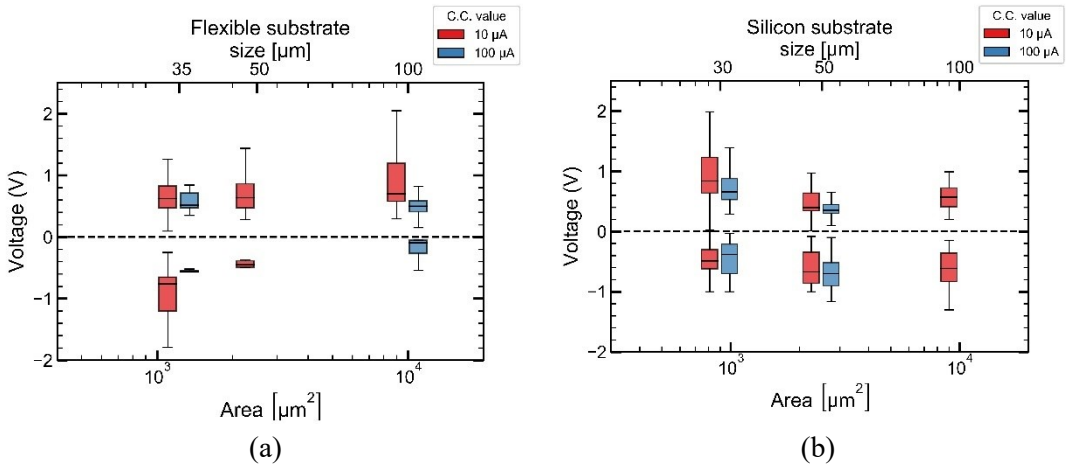


Figure 5. 14 Vset and Vreset box plot for devices fabricated on (a) flexible and (b) silicon substrate for compliance current (CC) of 10 and 100 µA.

However, it is interesting to observe in that the dependence of Vset on CC is quite evident; Vset decreases as CC increases. Hence, as already mentioned it has been shown that the radius of CF has a strong dependency on the CC, resulting in lower LRS values **[6], [7]**. A possible reason for lowering Vset at higher CC can be that the residual filament after reset is larger or features more ramifications, due to more incorporation of Ag within the solid electrolyte, therefore a lower voltage/electric field would be then required to reform the complete filament during the subsequent set operation. **Figure 5. 15** presents such a scenario.

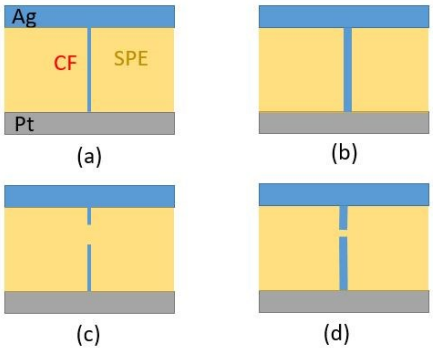


Figure 5. 15 Possible explanation for the decrease of Vset at increasing CC. CF after a set process (a) at low CC (b) at higher CC. The CF achieved at a lower CC can be more easily dissolved/broken (c) after a reset process while (d) the CF obtained at a higher CC is harder to breakdown and thus more easily reformed during the subsequent set.

5. Study of conduction mechanism in LRS and HRS

In a similar approach as analyzed in Chapter 3 (see **section 3.2., page 106**), the conduction mechanisms in LRS and HRS were also investigated for flexible devices. In this section, we have been working on consecutive LRS/HRS IV curves collected at 10 or 100 µA compliance current at ambient temperature on 100 µm-width devices. The following measurements correspond to more than 100 IV curves for each compliance current value.

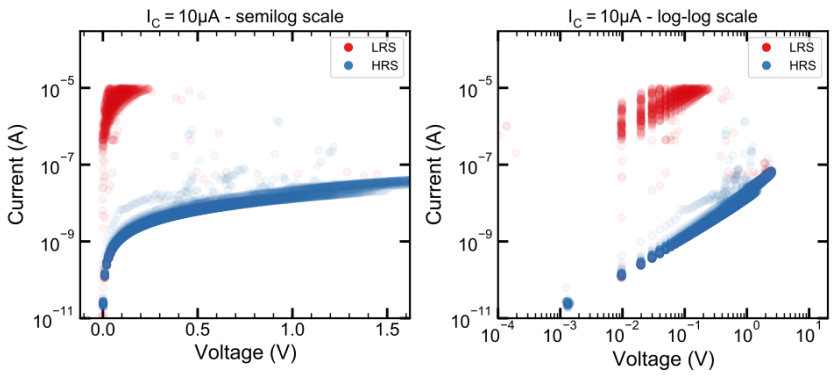
Figure 5. 16(a) & (b) shows current-voltage curves for each compliance current values both in semi-logarithmic and double logarithmic scales. Looking closely at the log-log plots, we observe a linear behavior for both in the Low and High resistance states. This result is in line with our observations on silicon substrates [see **Chapter 3**] where ohmic-type conduction was evidenced in both resistance states using the following modified ohmic-law:

$$J_{ohm}(E,T) = \sigma_0 e^{-\frac{E_a}{k_b T}} E^{\gamma} \quad (1)$$

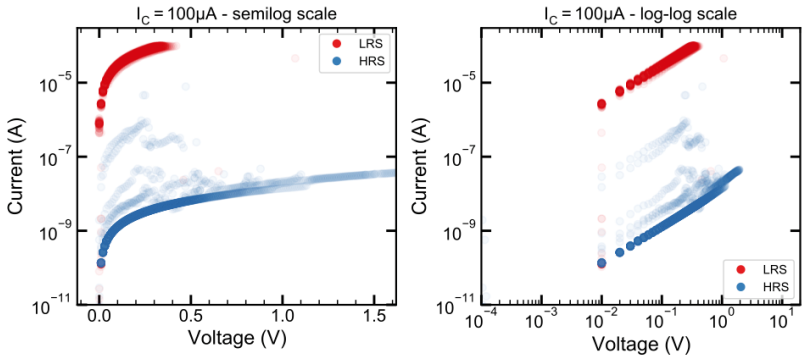
Since all our measurements were carried out at ambient temperature, a simplified version of equation (2) was used in the following:

$$J_{ohm}(E) = \sigma E^{\gamma} \quad (2)$$

Where σ now refers to the electrical conductivity at ambient temperature and γ remains the field coefficient, used as an adjustment parameter, as defined in **Chapter 3**.



(a)



(b)

Figure 5. 16 Semi-logarithmic plot (left) and double logarithmic plot (right) of current voltage measurements recorded using a (a) 10 µA and (b) 100 µA compliance current on a 100 µm-width CBRAM on flexible substrate. Each plot gathers more than 100 IV curves.

5.1. High Resistance States (HRS)

Figure 5. 17(a)-(c) presents the current density (J) vrs. electric field (E) in the HRS, together with histogram plots of the extracted conductivity (σ) and field coefficient (γ) respectively at a 100 µA CC.

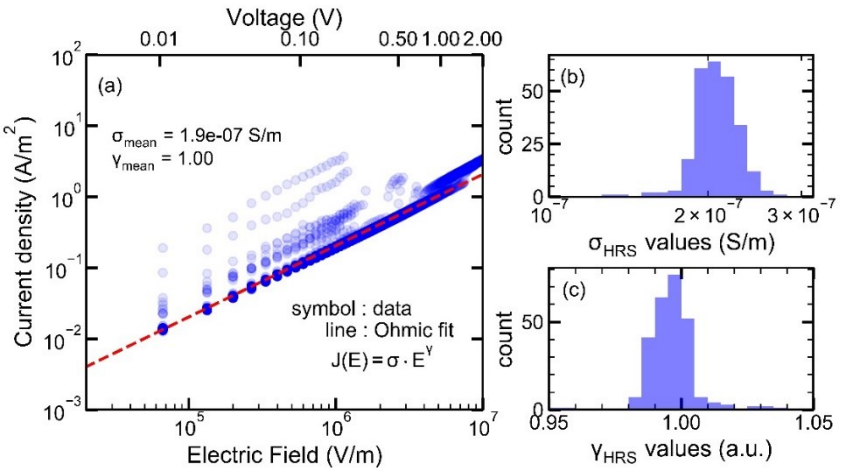


Figure 5. 17 (a) Curve fitting plot of J vrs E in the HRS at CC 100 µA corresponding, histogram plot of (b) σ values with mean 1.9 x 10^{-7} S/m (c) γ values with a mean of 1.00.

With the fitting parameter γ = 1, the devices show perfectly ohmic behaviour (I ∝V). A similar trend is observed in the HRS for 10 µA CC as shown in **Figure 5. 18(a)-(c)** in this case both the mean γ and electrical conductivity remain very close to those found at 100 µA.

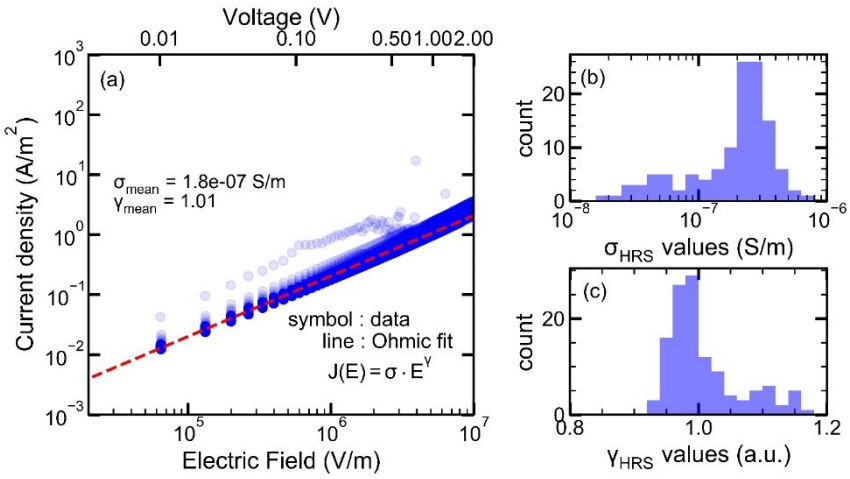


Figure 5. 18 (a) Curve fitting plot of J vrs E in the HRS at CC 10 µA corresponding, histogram plot of (b) σ values with mean 1.8 x 10^{-7} S/m (c) γ values with mean of 1.01.

5.2. Low Resistance States (LRS)

Figure 5. 19(a)-(c) shows the analysis of LRS obtained after programming at 100 µA. The devices exhibit unambiguously ohmic conduction with a field factor closely distributed around 1.0.

As the compliance current is decreased to 10 µA [**Figure 5. 20(a)-(c)**] ohmic conduction is less evident (the mean value of γ is around 1.1) and a larger variability is observed on the extracted conductivity values. This result is agreement with our observation on devices on silicon substrates where an increase in electrical variability together with a LRS resistance increase was observed as the compliance current is decreased (see **Chapter 3**).

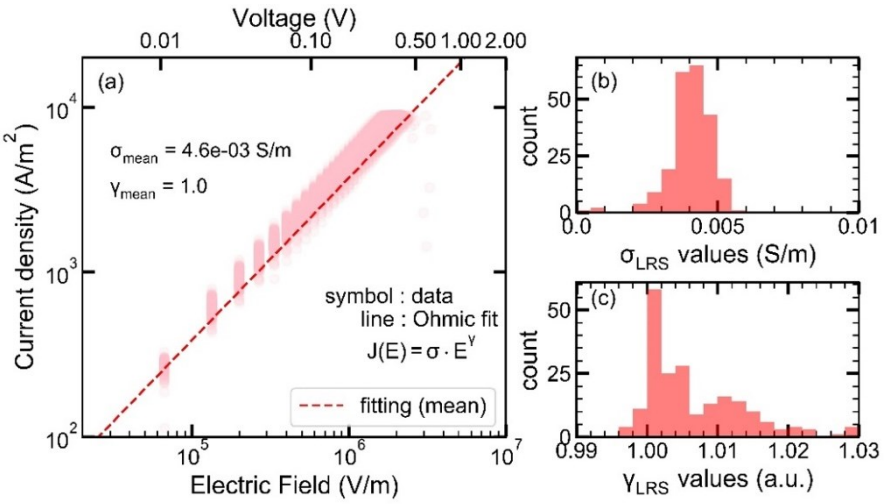


Figure 5. 19 (a) Curve fitting plot of J vrs E in the LRS at CC 100 µA corresponding, histogram plot of (b) σ values with mean 4.6 x 10^{-3} S/m (c) γ values with a mean of 1.0.

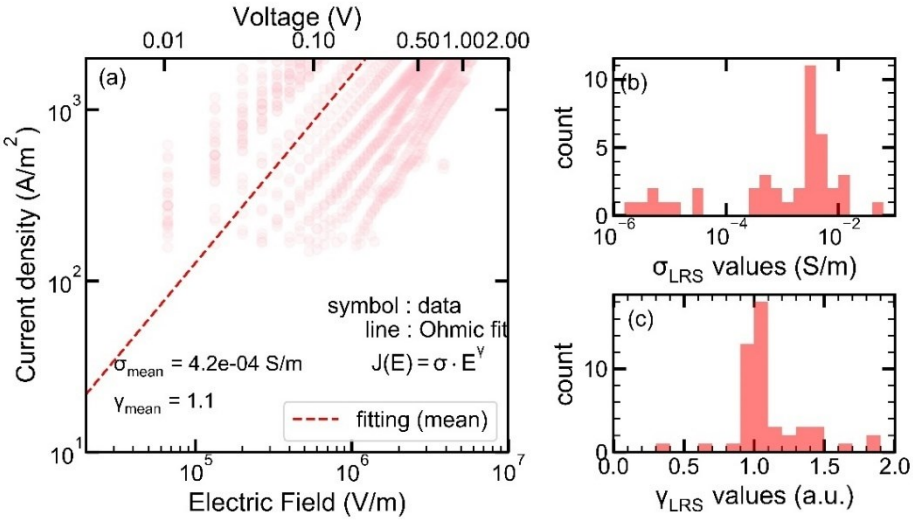


Figure 5. 20 (a) Curve fitting plot of J vrs E in the LRS at CC 10 µA corresponding, histogram plot of (b) σ values with mean 4.2 x 10^{-4} S/m (c) γ values with a mean of 1.10.

Table 5. 3 summarizes the conduction mechanism in the LRS & HRS with the values of σ & γ. The fitting parameter (γ) with a value of 1 shows perfectly ohmic conduction mechanism in the LRS the CBRAMs on both kapton & silicon substrate. For HRS, the devices are affected by the surfaces exhibiting ohmic behaviour on kapton and a mixed conduction mechanism on silicon.

		Electrical parameters for ohmic conduction $J = \sigma \cdot E^{\gamma}$			
		On kapton		**On silicon**	
	I_{comp}(µA)	**σ (S/m)**	**γ**	**σ (S/m)**	**γ**
HRS	10	$1.8 \cdot 10^{-7}$	~1.01	$6.8 \cdot 10^{-9}$	~ 1.34
	100	$1.9 \cdot 10^{-7}$	~1.00	$6.1 \cdot 10^{-10}$	~1.45
LRS	10	$4.2 \cdot 10^{-4}$	~ 1.10	$2.1 \cdot 10^{-2}$	~ 1
	100	$4.6 \cdot 10^{-3}$	~1.00	$4.8 \cdot 10^{-3}$	~ 1

Table 5. 3 Summary of the identified conduction mechanisms and extracted electrical parameters in our Ag/PEO/Pt CBRAM devices on flexible & silicon substrates for a 140 -160 and 139-149 nm thick PEO layer respectively.

6. **Conclusion to the chapter**

This chapter presents the performance of the CBRAM devices fabricated on kapton-flexible substrate. It has been illustrated that the CBRAMs on kapton showed low workable voltages, with OFF/ON resistance ratio $>10^4$. The overall switching voltages ranged from -1.5 V to +1.8 V quite similar to the CBRAMs fabricated on silicon. When subjected to the endurance tests, a device featured endurance larger than 300 cycles at 100 µA. The time for retaining the OFF/ON states were measured by applying constant voltages at 20, 40, 60, 80 mV respectively with a CC set at 1 mA, where the devices exhibited > 10^3 seconds as retention time. This low retention time is in agreement with our observations on silicon substrates.

In order to characterize the performance under mechanical stress, bending tests were performed with the bending radius set at 5.0 mm, strain % 1.2 and cycle rate at 0.657 cycle/second. The devices resisted $>10^4$ bending cycles maintaining an OFF/ON resistance ratio $>10^2$, indicative to the fact that the devices are resilient to stress. After 10^4 bending cycles, IV characteristics were performed on flat and in conformational contact on bend surface with strain of 0.38%. Promising results indicate that they can be applicable even on curved surfaces.

A comparison between CBRAMs on silicon & flexible substrates studying the LRS/HRS and set/reset voltages is presented. Our findings show that the LRS is not affected by area, while the HRS decreases with increase in area. As observed by our devices the CC influenced the set voltages - as the CC increased the Vset showed lower values. To explain this a hypothesis is presented, illustrating the fact that higher CC results into stronger CFs, hence upon reset, the breakdown of the filament is less compared to thin CF formed at lower CC. Hence, lower voltages are required to reform the devices set at higher CC.

Finally, a study of the conduction mechanism in the HRS/LRS states of these flexible devices was achieved. We showed that they followed ohmic type of conduction mechanism in LRS and a close to ohmic regime in their HRS. A summary on the conduction mechanism is presented at the end of the chapter.

7. **References**

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General conclusions and perspectives

A) General conclusion

With CBRAMs already being one of most the attractive emerging non-volatile memory technologies, through this research work, we aimed at developing those devices using sustainable materials in view of flexible electronics applications.

After underlying the numerous advantages of polymer materials for such applications, a Polyethylene Oxide (PEO) layer was selected to act as solid electrolyte layer. In **Chapter 2**, the full fabrication procedure of the CBRAMs developed throughout this work is presented. Starting from pure PEO powder, the solution preparation procedure was presented in order to produce both un-doped and silver-doped PEO solution with a controlled density and doping concentration. It is showed that water can be used as a main solvent to deposit the PEO active solid polymer electrolyte layer. A first report on the impact of spin-coating conditions on the thickness of the PEO layer with is then reported. Finally the full fabrication procedure of traditional "vertical" CBRAM devices is presented both on silicon and flexible substrates. In addition "planar" devices where fabricated by exploiting shading effect under titled evaporation with devices featuring a sub-micrometric nano-gap between the active and inert electrodes.

In **Chapter 3**, vertical CBRAM devices on silicon are electrically analysed and their performances are evaluated. It is first shown that at least a 50 nm-thick PEO film is necessary to have switching devices. This phenomenon could be attributed to a Ag diffusion layer from the top electrode and could be further checked by cross-section SEM-EDX analysis.

The effect of compliance current on the devices is then evaluated. It is shown that decreasing current compliance from 100 to 10 µA leads to an increasing LRS accompanied by increased variability and volatile-type switching. In this context, volatile CBRAM can be exploited as selector devices. Besides the observed electrical variability, retention time of our devices didn't exceed a few hundreds of seconds for programming currents within the range of 1 to 100 µA.

For the first time, we reported on the transport mechanism for PEO based CBRAMs. Temperature measurements undertook on a reference Pt/PEO/Pt devices exhibited Poole Frenkel conduction at voltages exceeding 1V while a close to Ohmic mechanism was observed below 1V. The memory devices exhibited a similar conduction mechanism in their High Resistance State (HRS) state like the reference ones whereas ohmic type of conduction mechanism is prevalent in the low resistance state (LRS). The extraction of the main electrical parameters related to the aforementioned mechanisms was performed in a statistical way at two compliance current values. This data would serve as a first building block for the elaboration of an electrical model accounting for electrical variability as discussed at the end of the chapter.

In an attempt to gain insights on the filament formation in the CBRAMs, planar devices featuring a nano-gap were fabricated and their study was exposed in **Chapter 4**. Devices with an Ag-doped or an un-doped PEO layers were firstly electrically characterized, revealing that both types of devices were functional with a large ~10^6 OFF/ON ratio. Programming voltages were within the same range than that of vertical devices, however a retention time exceeding 10^3 s was found for some of the undoped-devices/doped-devices, requiring further in depth analysis.

Optical micrographs taken after successive cycling revealed a darkened region in the vicinity of the nanogap for both type of devices. In addition, AFM measurements performed on an undoped device revealed morphological changes of the polymer layer after cycling in the same region. Finally, ex-situ SEM-EDX analysis were conducted to compare chemical profiles along the nanogap region before and after cycling. Clusters of Ag together with dendritic structures within the PEO layer were clearly visible in the nano-gap region, confirming the fact that silver filaments are formed/dissolved during the set/reset process. This is also the first report of filamentary observations on planar devices with gap lengths lower than 0.5 µm.

Finally in **Chapter 5**, CBRAM devices fabricated on a flexible substrate were analysed. Electrical performances showed that the switching voltages ranged from -1.5 V to +2.0 V, exhibited high resistance OFF/ON ratio > 10^4 and retention time in line with our observations on silicon substrates. Mechanical stress tests performed on the devices

confirmed that the devices could sustain mechanical stresses and maintained a memory window > 10^2 even after 10^4 bending cycles.

By comparing results collected on both flexible and silicon devices, it is shown that for both types of device HRS scales with area while the LRS together with its variability is mostly controlled by the compliance current. Finally the statistical analysis of conduction mechanism governing HRS and LRS states showed that flexible devices are mostly ruled by Ohmic conduction in both states.

B) Perspectives and future outlook

Optimizing the performance of our devices

Improvement of the performances of the devices, in particular the retention time, could be achieved through an appropriate *doping strategy* of the PEO layer. Evidences of such improvements were already reported in the literature. Solutions of doped-PEO were prepared to fabricated planar devices which exhibited better retention performances than our vertical devices from our first measurements. However, given the sanitary situation, we ran out of time to fabricate such doped vertical devices to compare with our present devices. In addition, conducting statistical analysis, one could also evaluate the effect of doping on electrical variability, which has not been reported to our knowledge.

In Chapter 2, we showed that the crystallinity ratio of the PEO layer can be adjusted through thermal treatments. Given that ionic motion mainly occurs along the amorphous phase of the polymer, comparing the electrical performances of devices with different thermal treatments could also lead to further performance optimization. However, the evaluation of the crystallinity ratio of thin (<1µm) still remains challenging.

Physical modelling

Based on the statistical data collected on our devices, models for electric transport in both LRS and HRS are already available. From that, it would be very interesting to develop a physical model describing both the quasi-static current-voltage characteristics and their dynamic response. To this aim, measurement such as set/reset time at varied voltage could helpful to better evaluate our devices.

Combining flexible NVM to sensors

As exposed in Chapter 1, flexible hybrid sensory patches consisting of sensor and memory unit can be fabricated to detect diseases such as Parkinson's, tremors, epilepsy. In view of moving toward such wearable flexible systems, it would be very interesting to combine our memory devices to sensors. On simple way to move in this direction, would be to use *resistive sensor* with our devices. Indeed these sensors could be used to modulate the voltage drop across our device in order to switch them beyond a threshold value. To this aim, a proof of concept should be first evaluated through circuit simulation.

Evaluation of the synaptic behaviour

Resistive memories, such as RRAM, PCM or CBRAM are also envisioned to implement artificial synapses for neuromorphic applications. To achieve this, memory devices have to feature the so-called *synaptic plasticity* where their resistance can be modulated through the application of voltage pulses. In order to evaluate the potentialities of our devices for such applications, *electrical studies have to be conducted on our devices using short programming pulses* (<1µs – 1ms range). Evaluation of the LRS retention time as function of the programming pulses frequency and/or amplitude would bring valuable information about the potential of our devices. Besides, it could open the way toward the development of synaptic circuits on flexible substrates.

Liste des travaux publiés :

PRESENTATIONS AT CONFERENCES

▪ -Oral Presentation at IEEE 14th Nanotechnology Materials and Devices Conference (NMDC19), Stockholm, Sweden on 'CBRAM Devices with a Water Casted Solid Polymer Electrolyte for Flexible Electronic Applications '. (Oct 27-30, 2019).

▪ -Oral Presentation at the 8th Advanced Functional Materials and Devices (AFMD18), Leuven, Belgium on ' Conductive bridge random access memory devices based on an eco-friendly solid polymer electrolyte'. (Aug 18-19, 2018)

▪ -Oral Presentation at 11th International Symposium on Flexible Organic Electronics (ISFOE18), Thessaloniki, Greece on ' Conductive Bridge Random Access Memory devices with Eco-friendly Solid Polymer Electrolyte for flexible electronics applications'. (July 2-5, 2018).

PUBLICATION

P. Mahato, E. Puyoo, D. Deleruyelle and S. Pruvost, "CBRAM devices with a water casted solid polymer electrolyte for flexible electronic applications," 2019 IEEE 14th Nanotechnology Materials and Devices Conference (NMDC), Stockholm, Sweden, 2019, pp. 1-5, doi: 10.1109/NMDC47361.2019.9083996.

Résume en Français

Le **chapitre 1** traite du marché actuel de l'électronique flexible, des différents secteurs qui le constituent, de ses opportunités et de son potentiel de croissance. Des statistiques ont été menées pour étudier et prévoir son marché dans le monde, concernant les applications et le domaine de l'électronique flexible.

De plus, une classification détaillée des technologies de mémoire dans l'industrie des semi-conducteurs, à la fois de type volatile et non volatile, est présentée avec les exigences actuelles et les défis auxquels ces technologies sont confrontées. Ce travail portant sur les mémoires non volatiles pour des applications électroniques flexibles: une étude des mémoires typiques sur substrats flexibles est présentée.

La dernière partie s'intéresse aux objectifs du travail de thèse dans le domaine des mémoires de type CBRAM. Le principe de fonctionnement des CBRAM, les matériaux utilisés et une étude bibliographique sont présentés ainsi que les motivations pour mener à bien ce travail. Le chapitre se termine par une conclusion.

Le **chapitre 2** présente les processus de fabrication impliqués dans le développement des dispositifs de mémoire. Tout d'abord, l'oxyde de polyéthylène (PEO) étant la principale couche active, la préparation de la solution de PEO, son dépôt et sa caractérisation sont effectués afin de valider les propriétés du PEO avec celles de la littérature. Par conséquent, cette partie établit le lien entre les conditions de revêtement par rotation et l'épaisseur de PEO sur des substrats Si / SiO2. L'épaisseur est déterminée à l'aide d'un profilomètre et d'images AFM utilisées pour confirmer la structure du dépôt de polymère.

Dans la section suivante, la procédure de fabrication de deux types de dispositifs CBRAM - verticaux et latéraux - est décrite. Grâce à des images obtenues au microscope électronique à balayage (MEB), les dispositifs de planaires fabriqués sont observés. Ce chapitre se termine par une démonstration réussie de la fabrication de dispositifs CBRAM.

Dans le **chapitre 3**, les performances électriques des dispositifs CBRAM verticaux fabriqués sur Si / SiO_2 sont caractérisées en vue de comprendre l'effet des électrodes, l'effet de l'épaisseur de PEO sur les performances du dispositif. Une fois sa faisabilité confirmée, une analyse complète des statistiques de tension de SET/RESET ainsi que sa fiabilité sont testées. Une analyse approfondie du mécanisme de conduction obtenu par ces dispositifs dans l'état de basse résistance (LRS) et l'état de haute résistance (HRS) est présentée ainsi qu'une conclusion sur les performances des dispositifs fabriqués.

Dans le **chapitre 4**, les résultats sur les dispositifs planaires sont présentés en respect avec sa caractérisation électrique - statistiques de tension SET/RESET. En outre, les résultats sur ses tests de fiabilité et l'effet du courant de conformité pour définir des états à plusieurs niveaux sont expliqués. Comme discuté précédemment, l'intérêt de fabriquer et d'étudier des dispositifs planaires est d'observer les changements morphologiques sur et autour de la région de nano-gap. Les résultats de ces observations sont démontrés dans cette partie. L'examen de la région du nano-gap est effectué par microscopie, images SEM, AFM et EDX pour illustrer les changements sur ces CBRAM à base de PEO non dopées et dopées.

Enfin au **chapitre 5**, le montage expérimental de la caractérisation électrique et des essais mécaniques des appareils est expliqué. En outre, les performances des dispositifs (caractéristiques IV, statistiques de tension, mesures d'endurance et temps de rétention des dispositifs) sont présentées.

Les substrats flexibles présentent l'avantage d'être utilisés dans des surfaces courbes et sous contrainte, d'où les résultats des tests mécaniques effectués sur les dispositifs.

Dans la dernière partie du chapitre, une étude comparative sur les performances des dispositifs est réalisée par rapport à la surface, le courant de conformité et l'étude du mécanisme de conduction sur substrat souple.

Objectifs de travail du doctorat

Mes objectifs de travail de doctorat peuvent être énoncés de la façon suivante:

i) Étude de la littérature et sélection de matériaux pour les dispositifs CBRAM

ii) Caractérisation physique et chimique de la couche SPE

iii) Validation du processus de fabrication

iv) Caractérisation électrique des dispositifs de mémoire

v) Évaluation des performances de la mémoire sous contrainte mécanique

vi) Observation morphologique du filament conducteur

vii) Modélisation physique des performances de la mémoire

i) Étude de la littérature et sélection des matériaux pour les dispositifs CBRAM.

La littérature montre que les CBRAM nécessitent trois couches: l'électrode supérieure, la couche d'électrolyte et l'électrode inférieure. Les matériaux à base de polymère peuvent être utilisés comme couche d'électrolyte polymère solide. Mohapatra *et al.* dans leurs travaux ont montré que les CBRAM flexibles peuvent être fabriqués en utilisant une couche de PEO comme couche d'électrolyte polymère solide (SPE). Ce travail a utilisé l'acétonitrile (ACN) comme solvant pour le dépôt de la couche SPE, qui est un solvant toxique. Le groupe de recherche de Wu a démontré que l'eau peut être utilisée comme solvant pour le dépôt de couche de PEO. Cela laisse à penser que l'eau peut être utilisée comme solvant, bien que ces résultats ne soient pas sur un substrat flexible. Des travaux de recherche substantiels sur l'oxyde de polyéthylène en tant que couche d'électrolyte polymère solide (SPE) ont clairement montré que le platine (Pt) peut être utilisé comme électrode inerte, le PEO comme couche d'électrolyte solide (SPE) et l'argent (Ag) comme actif électrode supérieure.

ii) Caractérisation physique et chimique de la couche SPE

L'étape suivante consiste à caractériser la couche de PEO (SPE) afin de tracer un plan d'étude de la couche en modifiant son épaisseur, sa cristallinité, son dopage et de relier son effet sur les performances des dispositifs CBRAM. Parmi les paramètres physiques, l'épaisseur de la couche de PEO présente un intérêt car ses

tensions de SET/RESET en dépendent. Surtout, que le mouvement des ions, pour former le filament conducteur, est associé au mouvement de chaîne segmentaire des régions amorphes. Il y a eu des études rigoureuses sur la conductivité ionique et le transport des ions dans les polymères PEO seuls ou greffés PEO, avec des indications sur le fait que le mouvement ionique des cations (ions) est lié aux régions amorphes / cristallines dans les films d'électrolyte polymère. Par conséquent, la cristallinité a joué un rôle très important dans le mouvement ionique. Compte tenu de cela, l'un de nos objectifs est d'étudier le rapport de cristallinité des couches minces de PEO dans les CBRAM. La diffraction des rayons X, l'infrarouge FT et la calorimétrie différentielle à balayage sont utilisées pour déterminer le rapport de cristallinité.

iii) Validation du processus de fabrication

Ainsi, comme notre objectif est de fabriquer des CBRAM en utilisant du PEO comme couche d'électrolyte polymère solide sur un substrat flexible, il est crucial de définir clairement le processus de fabrication et de le valider. Dans ce contexte, pour la préparation de la solution, son poids moléculaire (M_w), sa concentration, son temps de préparation doivent être optimisés, avec surtout la sélection du solvant (eau ou acétonitrile). Pour les paramètres de spin coating: vitesse de rotation, temps de rotation, accélération, ils doivent être déterminés avec des méthodes de traitement de surface pour avoir une bonne adhérence du PEO sur la surface. De plus, l'épaisseur des électrodes et la couche de PEO utilisées pour les expériences doivent être validées, avec un protocole défini pour la procédure de fabrication.

iv) Caractérisation électrique des dispositifs de mémoire

Les dispositifs fabriqués doivent être testés électriquement afin d'enregistrer leurs performances. Les statistiques de tension des appareils doivent être relevées. L'influence des électrodes sur les CBRAM est vérifiée, notamment pour l'électrode active. Des tests de fiabilité sont effectués à savoir le temps de rétention et des cycles d'endurance ont été menés pour tester la longévité des dispositifs. Les données obtenues peuvent être utilisées pour étudier l'effet du courant et de la zone de conformité sur les CBRAM.

v) Évaluation des performances de la mémoire sous contrainte mécanique

Comme les CBRAM flexibles présentent l'avantage d'utiliser de grandes surfaces et dans des orientations de courbure, les dispositifs doivent être soumis à des tests de contraintes mécaniques. Les performances caractéristiques de tension de courant doivent être obtenues tous les $10^{ème}$, $100^{ème}$, $1000^{ème}$ cycles et ainsi de suite pour confirmer la détérioration des dispositifs lors du test. De plus, pour un état de surface plane et pliée, la caractérisation électrique peut être réalisée pour examiner ses performances.

vi) Observation morphologique du filament conducteur

Lors de la fabrication de dispositifs planaires, outre leur caractérisation électrique, une observation morphologique du filament conducteur peut être réalisée. Très peu de travaux de recherche ont confirmé la commutation par la visualisation de la croissance du filament Ag sur les dispositifs.

vii) Modélisation physique des performances de la mémoire

Grâce aux recherches menées sur les mécanismes de transport, les performances des dispositifs peuvent être comprises. Cela peut nous aider à améliorer et à optimiser les performances des dispositifs. De plus, par la modélisation des dispositifs, leur comportement peut être compris et permettrait ainsi le couplage avec différents composants pour diverses applications.

Résume du Chapitre 2

Ce chapitre se concentre sur la caractérisation de la couche d'électrolyte polymère solide en polyoxyde d'éthylène (PEO) et la fabrication des dispositifs CBRAM sur silicium et substrat flexible.

Dans la première section du chapitre, les propriétés du PEO sont présentées, ainsi que la procédure détaillée pour former des films de PEO de 18 µm et 150 nm. L'analyse de la couche de PEO a été réalisée par les techniques de mesure suivantes : calorimétrie différentielle à balayage (DSC).

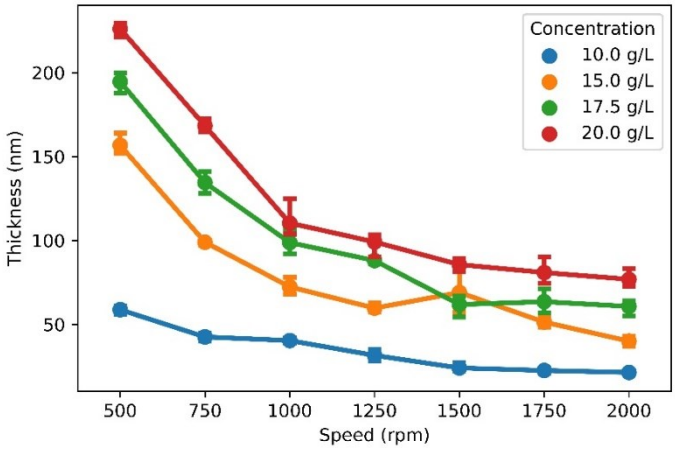


Fig R2 1 Évolution de l'épaisseur du PEO avec des vitesses de spin coating de 500 tr / min à 2000 tr / min avec différentes concentrations de PEO de 10,0 à 20,0 g / L

Il est démontré qu'avec les paramètres de revêtement par centrifugation, l'épaisseur de la couche de PEO peut varier de 25 nm à 225 nm comme on le voit dans **Fig R2 1**. L'observation morphologique de la couche PEO se fait à travers des images AFM/SEM montrant la région nano-gap et les électrodes.

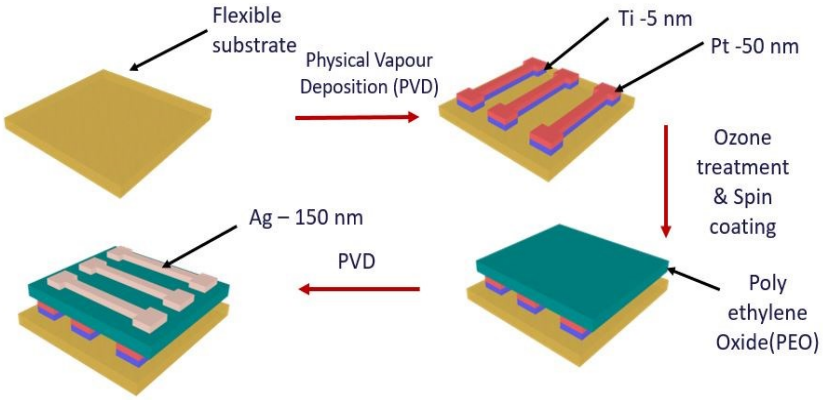


Fig R2 2 Description du processus de fabrication des dispositifs de mémoire sur substrat flexible.

Dans la dernière section du chapitre, la procédure de fabrication complète des dispositifs CBRAM sur des structures silicium verticales et planes et sur un substrat flexible **Fig R2 2** est présentée.

Résume du chapitre 3

Dans ce chapitre, le mécanisme de commutation est mis en évidence, expliquant le rôle des électrodes Ag dans la formation du filament. L'oxyde de polyéthylène (PEO) étant la principale couche active dans les dispositifs, il a été montré comment son épaisseur jouait un rôle dans les IV caractéristiques des dispositifs MIM empilés verticalement avec une épaisseur critique de 50 nm de la couche de PEO est nécessaire pour avoir commutation résistive. Lors de la caractérisation électrique observée, les dispositifs présentaient des tensions de réglage/réinitialisation faibles entre +1 et -1 V avec un rapport $R_{OFF\,/\,ON}$ élevé ~ 10^6 (**Fig R3 1**).

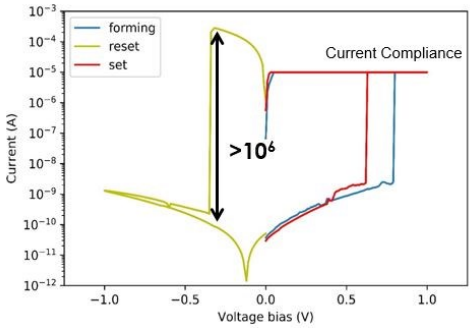
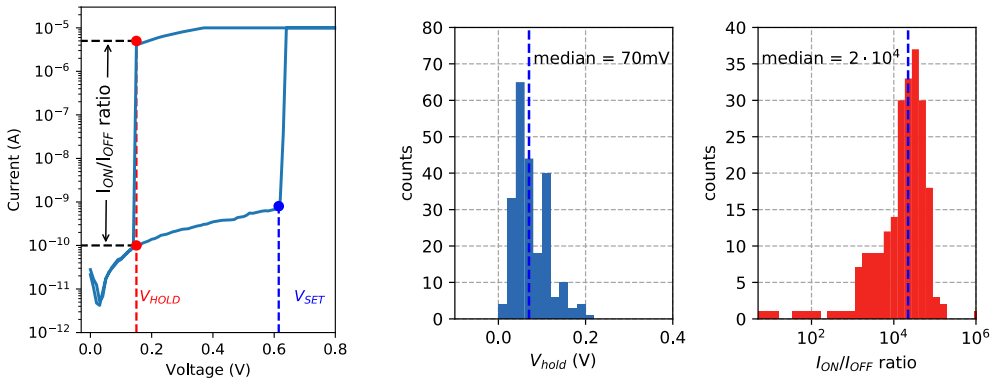


Fig R3 1 Les caractéristiques IV d'un appareil vertical sur Si / SiO_2 montrant un rapport de résistance OFF / ON élevé> 10^6

Les dispositifs, lorsqu'ils étaient soumis à différents CC, présentaient une dépendance au courant de conformité avec 10 µA CC montrant un type de commutation volatile par rapport à 100 µA. Par conséquent, il a été montré que les CBRAM peuvent également être utilisées comme sélecteurs avec une tension de maintien moyenne de 70 mV et un rapport $I_{ON / OFF}$ de 10^5 (**Fig R3 2**). Les mesures du temps de rétention ont montré des valeurs allant jusqu'à 800 secondes sur ces dispositifs non optimisés.



(a) (b)

Fig R3 2 Définition de la tension de maintien (V_{Hold}) et du rapport ION / OFF sur la base d'une courbe IV de commutation volatile et (b) de la distribution de V_{Hold} et $I_{ON / OFF}$ obtenue à un courant de conformité de 10 µA.

Dans la partie suivante, l'analyse du mécanisme de conduction dans le HRS a montré la dépendance à la température des dispositifs avec un mécanisme de transport de type Poole Frenkel prédominant. Dans le champ électrique faible, le type ohmique était prédominant (**Tableau 3R 1**).

		Electrical parameters for ohmic conduction $\mathbf{J = \sigma \cdot E^{\gamma}}$	
	I_{comp} (µA)	**σ**	**γ**
Pt/PEO/Pt	-	$\sigma_O = 46.4 \cdot 10^{-8} S/m$ $E_a = 0.41\ eV$ $\sigma = 0.61 \cdot 10^{-9} S/m$ @ 300K	~ 1.36
Ag/PEO/Pt (HRS)	10	$6.8 \cdot 10^{-9}\ S/m$	~ 1.34
	100	$6.1 \cdot 10^{-10}\ S/m$	~1.45
Ag/PEO/Pt (LRS)	10	$2.1 \cdot 10^{-2}\ S/m$	~ 1
	100	$4.8 \cdot 10^{-3}\ S/m$	~ 1

Tableau 3R 1 Résumé des mécanismes de conduction identifiés et des paramètres électriques extraits dans nos dispositifs de référence Pt / PEO / Pt et Ag / PEO / Pt CBRAM pour une couche de PEO de 150 nm d'épaisseur.

Résume du chapitre 4

Ce chapitre décrit les performances électriques des appareils nano-gap en ce qui concerne les statistiques de tension de réglage/réinitialisation effectuées sur douze appareils. Les capacités d'endurance de ces appareils se sont avérées proches de 70 pour les IV cycles complets de balayage et jusqu'à 80 cycles avec des mesures d'impulsions. De plus, en réglant le courant de conformité à 10 µA, 100 µA et 1 mA, des états multiniveaux peuvent être obtenus de la même manière que ceux indiqués pour les dispositifs verticaux. On peut également observer qu'un courant de conformité de 10 µA a également entraîné un type de commutation volatile.

Grâce aux dispositifs planaires, il est possible d'examiner les changements morphologiques autour de la région du dispositif à nano-gap, grâce à un microscope optique, un microscope à force atomique, un microscope électronique à balayage et des instruments à rayons X à dispersion d'énergie sont utilisés pour caractériser les dispositifs. Grâce aux micrographies effectuées sur les dispositifs non dopés et dopés, la région à proximité du nano-gap a été analysée avant et après quelques cycles. Un assombrissement de la région a été visualisé après quelques cycles, indiquant le fait que certains changements se produisent dans la région du nano-gap. Une comparaison est effectuée par rapport au courant de conformité réglé et au nombre de cycles effectués sur les appareils. Les images AFM sont effectuées avant et après les cycles suggèrent également qu'il y a des changements, confirmés également par le profil d'élévation dans la région du nano-gap et son voisinage **Fig R4 1**.

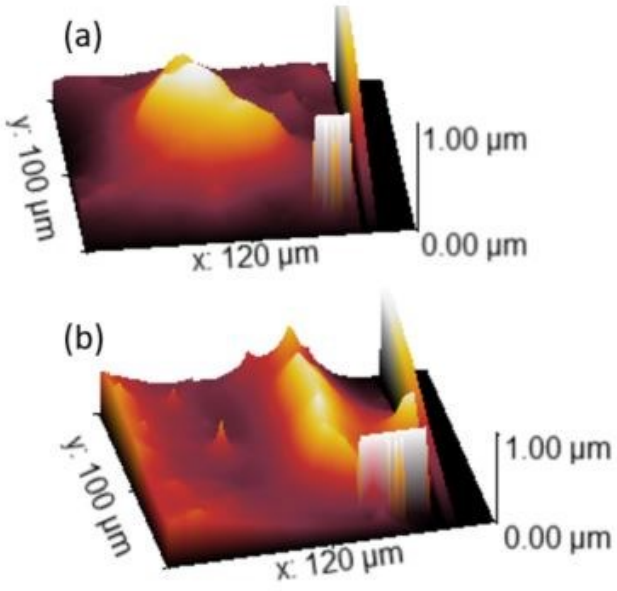


Fig R4 1 Topographie 3D proche de la région nano-gap (a) en parfait état (b) après le cyclage

Cela conduit à l'examen de la région du nano-gap avec des images SEM et des mesures EDX. Grâce aux images MEB, il peut être reconfirmé qu'il existe une diffusion d'argent (Ag) dans la région du nano-gap après le cyclage. Les mesures EDX fournissant l'analyse chimique des éléments présents dans le dispositif montrent que l'Ag est l'élément aboutissant à la formation filamentaire dans la région du nano-gap. De même, réalisés sur les dispositifs à nano-gap dopés, grâce à des mesures SEM et EDX, les résultats ont révélé avec succès la création de filaments d'Ag dendritique après le cyclage, démontrant le fait que nos dispositifs sont à base filamentaire. Le profil chimique des éléments dans la région de la section transversale est fourni avant et après le cyclage.

Comme perspectives d'avenir, les mesures de temps de rétention peuvent être effectuées sur les dispositifs dopés pour observer toute amélioration. Avec une observation in situ de la croissance filamentaire de l'Ag à chaque cycle, le

mécanisme et l'origine de la croissance filamentaire des électrodes seraient peut-être clairs **Fig R4 2** et **Fig R4 3**.

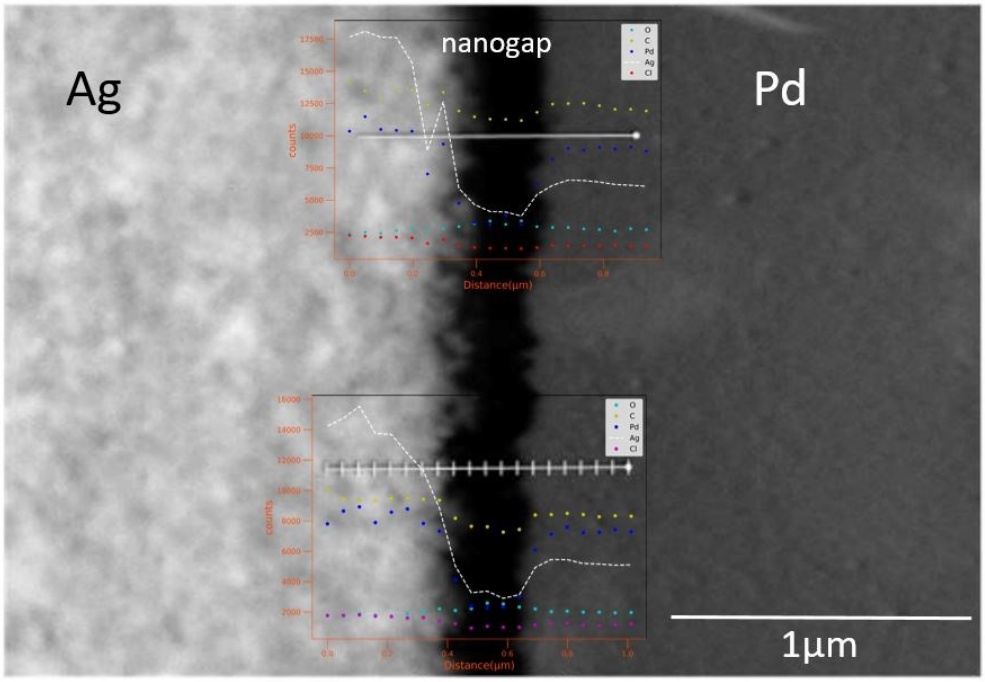


Fig R4 2 Image MEB d'un dispositif à nano-gap dopé vierge n ° 14 avec deux profils chimiques extraits des mesures EDX de l'électrode Pd (à gauche) à l'électrode Pd / Ag (à droite) sur la région du nano-gap (au centre).

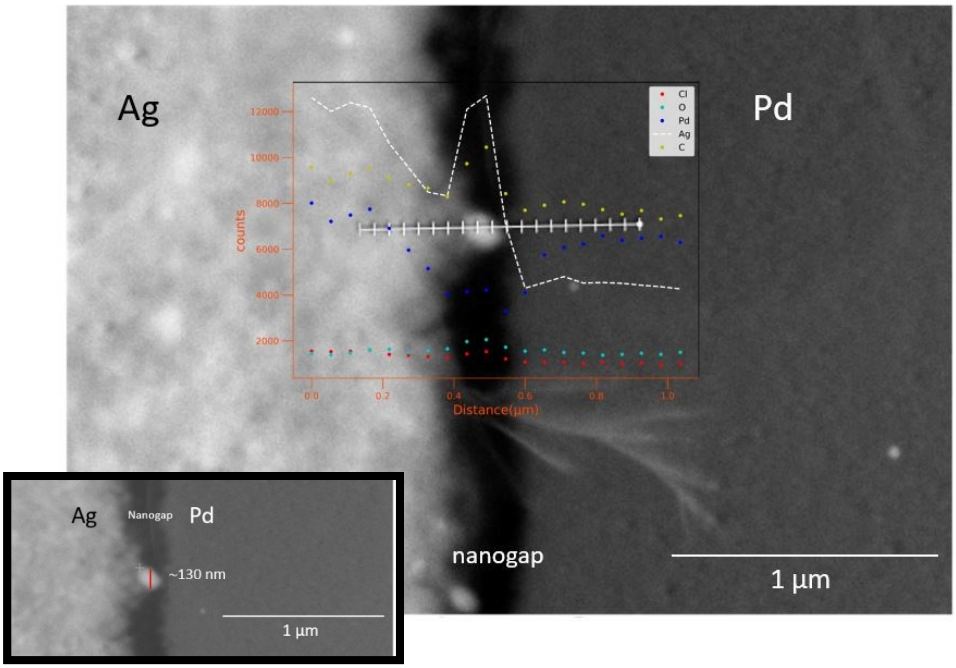


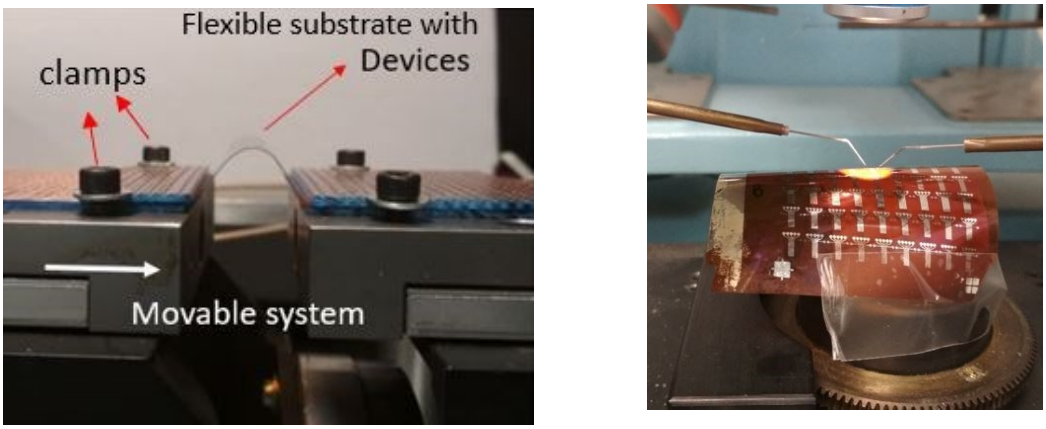
Fig R4 3 Image MEB du dispositif nano-gap dopé cyclé n ° 17 avec le profil chimique des éléments dans la région Pd sur Si, nano-gap et la région Pd & Ag sur Si. Les profils EDX révèlent sans ambiguïté que la structure dendritique et Ag s'est formée sur la région du nano-gap. L'encart montre le diamètre du filament ~ 130 nm.

Résume du chapitre 5

Dans ce chapitre, les performances, le montage expérimental, les résultats électriques sur les CBRAM en kapton sont présentés. Il a été illustré que les CBRAM sur kapton présentaient de faibles tensions utilisables, avec un rapport de résistance OFF/ON > 10^4. L'évolution de ses caractéristiques IV a offert des opportunités de les étudier comme des synapses artificielles. Les statistiques de commutation allaient de -1,5 V à +1,8 V assez similaires aux CBRAM fabriquées sur silicium. Lorsqu'il est soumis aux tests d'endurance, un appareil illustre une > 300 cycles à 100 µA. Il était évident qu'un CC plus élevé aboutissait à un état de faible résistance (LRS) plus stable. Le temps de conservation des états OFF/ON a été mesuré en appliquant des

tensions constantes à 20, 60, 80 mV respectivement avec un CC réglé à 1 mA, où les dispositifs présentaient > 1000 secondes comme temps de rétention.

Afin de caractériser les performances sous contrainte mécanique, des essais de flexion ont été réalisés avec le rayon de flexion fixé à 5,0 mm, la déformation de 1,11 % et la vitesse de cycle à 0,657 cycle/seconde. Les dispositifs ont résisté à plus de 10^4 cycles de flexion en maintenant un rapport de résistance OFF/ON 100, ce qui indique le fait que les dispositifs sont résilients aux contraintes **Fig R5 1** et **Fig R5 2**. Leurs statistiques de commutation ont également été confirmées sur une surface plane et pliée.



(a) (b)

Fig R5 1 Configuration pour les essais de contrainte mécanique - (a) configuration de flambage - les deux extrémités du substrat peuvent être fixées aux bras mobiles du système de telle sorte que les dispositifs sur lesquels les essais de déformation de traction à appliquer soient au sommet du pliez. (b) Essais de contraintes mécaniques par contact conformationnel - montrant la caractérisation IV in

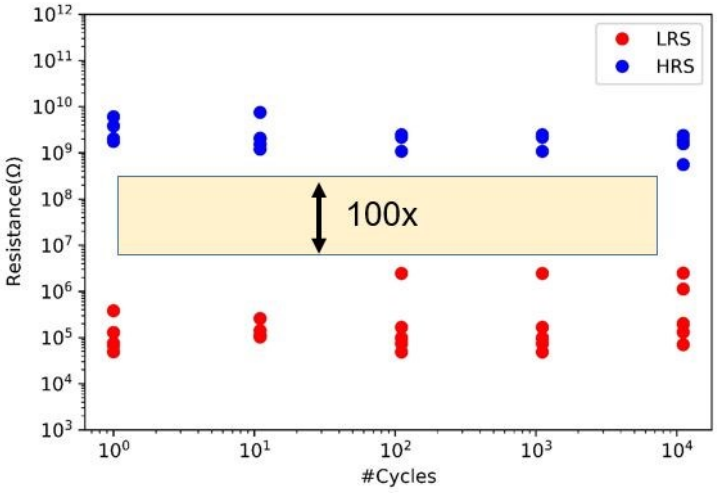


Fig R5 2 Illustre les performances des cycles de pliage sur six appareils, affichant une fenêtre de rapport de résistance OFF / ON de> 10^2 même après 10^4 cycles de pliage.

Pour étudier l'effet de la section transversale sur les appareils, leurs états HRS/LRS sont étudiés avec le calcul des statistiques de tension. Les performances ont confirmé que la zone n'a joué aucun rôle significatif dans les caractéristiques IV ou HRS/LRS.

Grâce aux statistiques HRS / LRS et de tension, il a été observé que le courant de conformité réglé affectait les performances, car le courant de conformité était faible, la variabilité de la commutation et les états LRS/HRS élevés.

Enfin, pour étudier le mécanisme de conduction dans les états HRS/LRS sur ces CBRAM fabriquées sur des substrats souples, il a été observé qu'elles suivaient un mécanisme de conduction de type ohmique avec des valeurs de γ proches de 1,0. Ceci conclut au fait que le substrat n'a aucun impact sur le mécanisme de transport.

FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : MAHATO DATE de SOUTENANCE : 14/12/2020
(avec précision du nom de jeune fille, le cas échéant)

Prénoms : Prabir

TITRE : Study and development of resistive memories for flexible electronic applications /Etude et développement de mémoires résistives pour l'électronique flexible

NATURE : Doctorat Numéro d'ordre : 2020LYSEI134

Ecole doctorale : Ecole Doctorale N° ED160- Électronique, Électrotechnique et Automatique

Spécialité : Électronique, micro et nano électronique, optique et laser

RESUME :
The advent of flexible electronics has brought about rapid research towards sensors, bio implantable and wearable devices for assessment of diseases such as epilepsy, Parkinson's and heart attacks. Memory devices are major component in any electronic circuits, only secondary to transistors, therefore many research efforts are devoted to the development of flexible memory devices. Conductive Bridge Random Access Memories (CBRAMs) based on creation/dissolution of a metallic filament within a solid electrolyte are of great research interest because of their simple Metal Insulator Metal architecture, low-voltage capabilities, and compatibility with flexible substrates.

In this work, instead of a conventional metallic oxide or a chalcogenide layer, a biocompatible polymer - Polyethylene Oxide (PEO) – is employed as the solid electrolyte layer using water as solvent. Memory devices, consisting in Ag/PEO/Pt tri-layer stacks, were fabricated on both silicon and flexible substrates using a heterogeneous process combining physical vapour deposition and spin coating. To aim this, a systematic study on the effect of solution concentration and deposition speed on the PEO thickness is presented. SEM/EDX and AFM measurements were then conducted on devoted "nano-gap" planar structures and have revealed the formation of metallic Ag precipitates together with morphological changes of the polymer layer after resistance switching. The performance of the resistive memory devices is then assessed on silicon and flexible substrates. In particular programming voltage statistics, OFF/ON resistance ratio, endurance cycles and retention tests are performed and the effect of current compliance is analysed. The conduction mechanism in the HRS/LRS is studied on the Ag/PEO/Pt and Pt/PEO/Pt reference devices. Finally, the electrical characterization of devices on flexible substrate is performed under mechanical stress, showing promising results. Polymer-based CBRAM devices are therefore suggested as potential candidates for sustainable development of flexible memory devices.

MOTS-CLÉS : Flexible electronics, resistive RAMs, solid polymer electrolyte, water, PEO, polymers

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