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THÈSE

Pour obtenir le grade de

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Présentée par

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préparée au sein du **Laboratoire Laboratoire des Technologies de la Microélectronique**
dans **l'École Doctorale Electronique, Electrotechnique, Automatique, Traitement du Signal (EEATS)**

Mécanismes de vieillissement liés à la pénétration d'humidité dans les matériaux diélectriques à faible permittivité des interconnexions.

Moisture-related ageing mechanisms of interconnects low-K dielectrics.

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Mécanismes de vieillissement liés à la pénétration d'humidité dans les matériaux diélectriques à faible permittivité des interconnexions.

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Mécanismes de vieillissement liés à la pénétration d'humidité dans les matériaux diélectriques à faible permittivité des interconnexions.

Résumé

La réduction des dimensions des dispositifs micro-électroniques élémentaires, notamment des transistors et des cellules mémoires, a permis au cours des dernières décennies d'augmenter la densité d'éléments intégrés et donc d'obtenir plus de fonctions au sein d'une même puce. Cette réduction des dimensions a notamment nécessité l'introduction de matériaux diélectriques à faible permittivité, particulièrement sensibles à l'humidité. Cette thèse détaille les propriétés électriques de tels matériaux ainsi que les conséquences de leur contamination par l'humidité sur leurs caractéristiques. Le procédé de fabrication des interconnexions à base de cuivre et de matériau à faible permittivité est détaillé puis, le matériau à faible permittivité utilisé dans les interconnexions avancées, appelé SiOC :H, est caractérisé afin d'en déterminer les principales propriétés chimiques et structurelles, nécessaires à la compréhension des phénomènes physiques menant à la dégradation des performances électriques de ces matériaux. Ensuite, une importante étape de conception et de fabrication de structures de caractérisation permettant l'étude de l'impact de la pénétration d'humidité sur les performances électriques du matériau SiOC :H est détaillée. Enfin, les résultats de caractérisations électriques effectuées sur ces structures sont présentés, permettant une compréhension des processus physiques menant à la dégradation des performances du matériau SIOC :H utilisé dans l'industrie microélectronique.

Mots-clés

Matériaux diéléctriques à faible permittivité, SiOC :H, fiabilité des matériaux diélectriques, pénétration d'humidité, courant de fuite, dégradation.

Moisture-related ageing mechanisms of interconnects low-κ dielectrics.

Abstract

Over the past decades, scaling of microelectronic chips, in particular transistors and memory cells, has allowed to increase substantially both the density of integrated circuit and integrate the number of functions offered. Such scaling required the introduction of low permittivity dielectrics, which are particularly sensitive to moisture pollution. This thesis details the dielectrics main properties and the consequences of moisture ingress in such low-permittivity dielectrics, also referred as SiOC :H dielectrics. The fabrication of low-κ/copper-based interconnects is detailed. Then, the SiOC :H dielectric material is characterised to determine its chemical and molecular structure in order to understand underlying physical phenomenon leading to the material electrical performances degradation. Then, the conception and fabrication of electrical test structures required to evaluate the impact of moisture on the electrical properties and performances of integrated SiOC :H dielectric material is presented. Finally, the results of electrical characterisations carried out on these structures provide a better understanding of physical phenomenon leading to electrical performance degradation of SiOC :H dielectric material used in the semiconductor industry.

Key words

Low permittivity dielectrics, SiOC :H, dielectric reliability, moisture ingress, leakage current, degradation.

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Contents

Glossary **ix**

General introduction **1**

1 Interconnects and dielectrics **3**
1.1 Introduction . . . 3
1.2 Modern microelectronics and Moore's law . . . 3
1.2.1 From kettles to pacemakers: chips surround us . . . 4
1.2.2 Moore's Law and interconnects . . . 4
1.3 Dielectrics . . . 5
1.3.1 Role of dielectrics in chips interconnects . . . 5
1.3.2 Low permittivity dielectrics: macroscopic and microscopic principles 6
1.3.3 Strategies to reduce the permittivity . . . 13
1.4 Interconnect reliability . . . 13
1.4.1 Interconnect failure modes . . . 14
1.4.2 Usual electrical characterisation techniques . . . 17
1.4.3 Lifetime estimation: extrapolation models . . . 22
1.5 Moisture and interconnects performances . . . 24
1.5.1 Moisture ingress modalities . . . 25
1.5.2 Moisture ingress countermeasures . . . 26
1.5.3 Interconnect performance degradation indicators . . . 26
1.6 Conclusion . . . 30

2 Integration process constraints and SiOC:H chemical structure **31**
2.1 Introduction . . . 31
2.2 The dual-damascene process . . . 31
2.2.1 Pre-Metal Dielectric . . . 32
2.2.2 SiOC:H deposition . . . 32
2.2.3 SiOC:H etch . . . 32
2.2.4 Copper diffusion barrier deposition (Ta/TaN) . . . 33
2.2.5 Copper deposition and copper grains . . . 34
2.2.6 Chemical Mechanical Polishing (CMP) . . . 34
2.2.7 Wet and dry cleans . . . 35
2.2.8 SiCN copper encapsulation and line anneal . . . 36
2.3 Passivation, encapsulation and tightness . . . 36
2.3.1 Required properties of materials used in the far BEOL . . . 36
2.3.2 Encapsulation . . . 36

2.3.3 External moisture tightness . . . 37
2.4 Process variability and SiOC:H specificity . . . 38
2.4.1 Generalities . . . 38
2.4.2 Process steps generating SiOC:H variability . . . 39
2.5 Physical characterisation of SiOC:H material . . . 41
2.5.1 Surface Photovoltage measurements . . . 41
2.5.2 Ellipsometric porosimetry and GISAXS . . . 42
2.5.3 X-ray Photoelectron Spectroscopy and TEM Energy Dispersive X-ray 45
2.5.4 FTIR and MIR spectroscopies . . . 49
2.5.5 Conclusion . . . 53

3 Electrical test structures conception, process control and optimisation 55
3.1 Introduction . . . 55
3.2 Structures design and mask set conception . . . 55
3.2.1 Structures CAD and mask set . . . 55
3.2.2 C2M and OPC principles . . . 56
3.3 Test structures detail . . . 57
3.3.1 Experimental mask set . . . 57
3.3.2 Elementary test structure . . . 58
3.3.3 Surface variations . . . 58
3.3.4 Line space variations . . . 59
3.3.5 Seal-ring . . . 59
3.4 Process control and optimisation . . . 61
3.4.1 Inline process control . . . 61
3.4.2 Process optimisation . . . 62
3.5 Test structures and multi-probing influence . . . 64
3.5.1 Context . . . 65
3.5.2 Pad tightness . . . 66
3.6 Conclusion . . . 69

4 Moisture and electrical characteristics of SiOC:H dielectric 71
4.1 Introduction . . . 71
4.2 Thermal anneals and moisture ingress acceleration methodology . . . 71
4.2.1 High temperature anneal effects . . . 72
4.2.2 Moisture-related ageing acceleration . . . 73
4.2.3 Material considerations . . . 75
4.3 SiOC:H time-to-breakdown . . . 76
4.3.1 Intrinsic SiOC:H . . . 77
4.3.2 Moisture ingress effect . . . 80
4.3.3 Breakdown point localisation . . . 81
4.4 Breakdown mechanisms study . . . 84
4.4.1 Constant Voltage Stress (CVS) . . . 84
4.4.2 Constant Current Stress (CCS) . . . 86
4.4.3 SiOC:H material considerations and consequences . . . 89
4.5 Conduction mechanism(s) . . . 89
4.5.1 Static leakage current analysis . . . 89
4.5.2 Schottky Emission and Poole-Frenkel tunnelling . . . 90

4.5.3 Moisture influence on conduction mechanisms 92
4.5.4 Triangular Voltage Sweep (TVS) 94
4.5.5 Traps in SiOC :H dielectric 99
4.6 Conclusion 102

General conclusion and perspectives **103**

Glossary

.gds file .gds extension file format. 1, 55, 56

ABS Anti-lock Braking System. 1, 4

AFM Atomic Force Microscopy. 1, xiv, 44, 103

ATE Automatic Test Equipment. 1, 18

BEOL Back-End-Of-Line. 1, xiii, xvii, 3, 5, 6, 7, 13, 14, 15, 16, 18, 19, 20, 22, 23, 25, 26, 29, 32, 35, 38, 41, 55, 56, 57, 58, 61, 68, 69, 75, 81, 92, 103, 104

C/S/C interwoven Comb-Serpentine-Comb. 1, xvii, xix, 58, 59, 62, 78, 79, 80, 81, 82, 85, 86, 87, 104

C2M CAD-to-Mask. 1, 56, 57, 61, 69, 104

CAD Computer-Aided Design. 1, xiv, 40, 55, 56, 57, 61, 84, 104

CCS Constant Current Stress. 1, xvii, 21, 22, 29, 86, 87, 88, 89, 97, 102, 105

CD Critical Dimension. 1, 39, 61, 63

CMOS Complementary Metal-Oxide Semiconductor. 1, 3

CMP Chemical-Mechanical Planarisation. 1, 14, 25, 34, 35, 38, 40, 83, 104

CVD Chemical Vapour Deposition. 1, 61

CVS Constant Voltage Stress. 1, xvii, xviii, 21, 22, 29, 77, 78, 80, 82, 84, 85, 86, 90, 99, 105

Design Rules Manual It refers to the document containing the ensemble of rules which constrain the drawing of structures/chips, in order to guaranty electrical functionality. These rules are established with the help of several parameters such as process variability, processing tools capability and reliability assessments.. 1

DRM Design Rule Manual. 1, 56, 60

EDMR Electrically Detected Magnetic Resonance. 1, 100, 106

EDX Transmission Electron Microscopy (TEM) Energy Dispersive X-ray. 1, xv, 45, 47, 48, 103

EMMI EMission MIcroscopy. 1, xviii, 93, 94, 102, 105

ERCS Exponential Ramp Current Stress. 1, 29

eV electron-Volts. 1, 92, 100

EWS Electrical Wafer Sort. 1, 2

Far BEOL Far Back-End-Of-Line. 1, 36, 37, 57, 71, 104

FEOL Front-End-Of-Line. 1, 3, 18, 26, 32, 63

FTIR Fourier Transform InfaRed. 1, xv, 9, 49, 50, 51, 52, 53, 101, 103

GISAXS Grazing-Incidence Small Angle X-ray Scattering. 1, xiv, xv, 42, 43, 44, 45, 103

Graphic Data System Misleadingly used to refer to files containing the physical description of a structure layout. It is a quasi industrial standard in the semiconductor industry. OASIS for Open Artwork System Interchange Standard is a similar format type and may replace GDS at some point. 1

HM Hard Mask. 1, xiv, 33, 35, 40

ID Impact Damage. 1, xvii, 23, 24, 77, 78, 100, 102, 103

IMD Inter-Metallic Dielectric. 1, 5, 6, 11, 17, 19

IoT Internet of Things. 1, 4, 106

ITRS International Technology Roadmap for Semiconductors. 1, 5, 7

low-κ low permittivity. 1, 2, 5, 6, 7, 13, 15, 21, 23, 24, 25, 26, 27, 30, 31, 32, 33, 34, 36, 37, 41, 45, 47, 49, 53, 55, 57, 61, 70, 71, 75, 81, 84, 89, 92, 98, 103, 104, 105, 106

LRVS Linear Ramp Voltage Stress. 1, 29

MIM Metal-Insulator-Metal. 1, 100

MIR Multiple Internal Reflections. 1, xv, xvii, 49, 50, 51, 52, 53, 75, 76, 101, 102, 103, 104, 105

MOL Middle-Of-Line. 1

MV Mega-Volts. 1, 92

OBIRCH Optical Beam-Induced Resistance CHange. 1, xvii, 82, 83

OEM Original Equipment Manufacturers. 1

OPC Optical Proximity Correction. 1, 40, 56, 57, 61, 69, 104

PARXPS Parallel Angle Resolved X-ray Photoelectron Spectroscopy. 1, xv, 46, 47, 103

PECVD Plasma-Enhanced Chemical Vapour Deposition. 1, 32, 40, 61

PF Poole-Frenkel trap-assisted tunnelling. 1, xvii, xviii, 23, 90, 91, 92, 97, 105

PL Power Law. 1, xvii, 23, 24, 77, 78, 103

PMD Pre-Metal Dielectric. 1, 32, 57

POR Process Of Reference. 1, xiv, xv, 41, 42, 43, 44, 45, 46, 47, 50, 51, 52, 75, 100

PT Parametric Test. 1, 2, 18, 26

PVD Plasma Vapour Deposition. 1, 37

R&D Research & Development. 1, 5, 7, 22

R-E Root-E. 1, xvii, 23, 24, 77, 78, 103

RH Relative Humidity. 1, xvi, 73, 74, 102

SE Schottky thermionic Emission. 1, xvii, xviii, 23, 90, 91, 92, 97, 105

SEM Scanning Electron Microscopy. 1, xiv, xvi, 39, 40, 44, 61, 67, 68, 69

SILC Stress-Induced Leakage Current. 1, 95

SPV Surface PhotoVoltage. 1, xiv, 41, 42

SSCM Standard Cubic Centimetres per Minute. 1, 32, 41

T_{BD} Time-to-Breakdown. 1, 62

TDDB Time-Dependent Dielectric Breakdown. 1, xiv, 28, 29, 34, 36

TEM Transmission Electron Microscopy. 1, xv, 48, 62, 69

TEOS TetraEthyle OrthoSilicate. 1, 32, 34, 35, 36, 48

THB Temperature Humidity Bias. 1, 73, 76

TMS TetraMethylSilane. 1, 32, 41, 46, 47, 51, 52, 104

TVS Triangular Voltage Sweep. 1, xviii, 94, 95, 96, 97, 98, 105, 106

XPS X-ray Photoelectron Spectroscopy. 1, 45, 46, 47, 100, 103

List of Figures

1.1 Moore's law, with major commercial processors names 4
1.2 Resistance-Capacitance equivalent circuit in the BEOL. 6
1.3 Schematic principle of electronic cloud polarisation event around an atom under an electrical field E. 8
1.4 Schematic principle of ionic polarisation event in an ionic crystal under an electrical field E. 9
1.5 Schematic principle of dipolar polarisation event in a dielectric under an electrical field E. 10
1.6 Schematic principle of free space charges polarisation event in a dielectric under an electrical field E. 10
1.7 Different polarizabilities mechanisms implies different frequency responses. Here schematically, ϵ refers to the material dielectric constant, and σ to its conductivity (including dielectric loss). 11
1.8 Parallel capacitance measurement model with the addition of a series resistance R_s accounting for the access resistance of the structure. 12
1.9 Frequency response of standard BEOL structure (see section 3.3 for more details) showing frequency limitation from access resistance. 13
1.10 Example of delamination and crack diffusion in a chip BEOL. 14
1.11 Example of tantalum diffusion barrier diffusion. 15
1.12 Electromigration structure and failure principle. 16
1.12.a Electromigration structure. 16
1.12.b SEM cross-section of a line after an electromigration test from Cheng et al.. A void without copper is seen on top of the via. . . . 16
1.13 Cross-section view of a catastrophic breakdown between metallic lines. . . 17
1.14 Stacked leakage current-voltage characteristics of standard interconnect structures. 18
1.15 Semi-log cumulative distribution of leakage currents measured at 15V bias. 19
1.16 Cumulative distribution of capacitances values measured at 1kHz, 200mV amplitude AC signal under 0V DC bias. 20
1.17 Cumulative distribution of serpentine resistance values measured at 2V. . . 20
1.18 CVS test and Weibull representation 21
1.18.a Example of a leakage current measurement during CVS test at 65V. 21
1.18.b Weibull distribution of time-to-breakdowns extracted from CVS tests at different voltages. 21
1.19 Voltage measurement during CCS tests at 1μA on reference structures. . . 22
1.20 Different lifetime extrapolation models fitted to experimental data points from figure 1.18.b. 24

1.21 Evolution of leakage current at 15V. 27
1.22 Capacitance evolution over time of wet structures. 27
1.23 Dissipation factor correlations with capacitance and leakage current. 28
1.23.a Dissipation factor as a function of leakage current at 15V. 28
1.23.b Dissipation factor as a function of capacitance value measured at 0v, 1kHz. 28
1.24 Moisture impact on test structure TDDB performance. 29
1.25 PT parameters and time-to-breakdown correlation plots. 30
1.25.a Time-to-breakdown as a function of capacitance value measured just before stress. 30
1.25.b Time-to-breakdown as a function of leakage current measured at 20V just before stress. 30

2.1 Etching process steps in the dual-damascene process flow. 33
2.2 Ta/TaN copper diffusion barrier deposition, copper seed, and copper electroplating in the dual-damascene process flow. 34
2.3 Chemical Mechanical Polishing process step in the dual-damascene process flow. 35
2.4 Potential consequence of poorly controlled CMP followed by high-pressure water jet during wet cleaning. 35
2.5 Schematic representation of the pad fabrication after the encapsulation step. 37
2.6 Schematic representation of the different types of variability in the semiconductor industry [104]. 38
2.7 Example of a multiple chambers tool 39
2.8 SEM view of a first layer of interconnect after HM lithography and superposed drawn metal 1 CAD layer boundaries (red). The area or the future copper lines are freed from HM. 40
2.9 SPV measurement and effect of anneal on the relative dielectric constant of as-deposited POR SiOC:H (2.9.a), and POR SiOC:H treated with a 1-hour anneal at 400°C under nitrogen(2.9.b). 42
2.9.a 42
2.9.b 42
2.10 Ellipsometric porosimetry working principle [118]. S.E. stands for Standard Ellipsometry. 42
2.11 Ellipsometric porosimetry measurements on different uncapped SiOC:H materials. 43
2.11.a Standard (POR) SiOC:H. 43
2.11.b High-O SiOC:H. 43
2.11.c High-TMS SiOC:H. 43
2.12 GISAXS working principle and porous thin film schematic response [121]. . 44
2.12.a GISAXS geometry principle. 44
2.12.b GISAXS porous thin film schematic response. 44
2.13 Topological images of uncapped POR SiOC:H materials. 44
2.13.a SEM view of the as-deposited POR SiOC:H material surface. 44
2.13.b AFM view of the as-deposited POR SiOC:H material surface. . . . 44
2.14 10h GISAXS measurements on uncapped POR SiOC:H materials. 45

2.14.a GISAXS raw signal of the as-deposited POR SiOC:H material. . . . 45
2.14.b GISAXS raw signal of the annealed POR SiOC:H material. 45
2.15 Parallel Angle Resolved XPS working principle (without any sample tilt) [127]. 46
2.16 As deposited SiOC:H materials chemical composition depth profiles measured by PARXPS. Higher angles correspond to photelectrons emitted by the sample surface. 47
2.17 TEM view of a cross-section perpendicular to the integrated copper line (top). Left: spectrum recorded at the green cross. Right: EDX profile along the orange line on the TEM view (top). 48
2.18 FTIR spectrum and evolution of as-deposited SiOC:H blanket material. . . 50
2.18.a FTIR spectrum of as deposited SiOC:H blanket material. 50
2.18.b Evolution of as-deposited SiOC:H blanket material absorbance after 497 days at room relative humidity and temperature measured with FTIR. 50
2.19 FTIR and MIR spectra of as-deposited SiOC:H blanket material. 51
2.19.a Working principle of Multiple Internal Reflections (MIR) measurement setup [135]. 51
2.19.b MIR spectrum of as deposited SiOC:H blanket material. 51
2.20 FTIR and MIR spectra of as-deposited SiOC:H blanket material. 52
2.20.a Stacked MIR spectra of three variants of the SiOC:H dielectric material deposited on silicon and capped by silicon nitride (not visible in spectrum). 52
2.20.b Stacked MIR spectra of three variants of the SiOC:H dielectric material deposited on silicon after 125 days of storage in ambient atmosphere. 52
2.21 Evolution of moisture-related peak area of three variant SiOC:H blanket materials. 53
2.21.a Evolution of moisture-related region normalised area of three uncapped SiOC:H blanket materials, stored in ambient atmosphere. . 53
2.21.b Evolution of moisture-related region normalised area of three capped SiOC:H blanket materials, stored in ambient atmosphere. 53

3.1 Main C2M boolean operations performed on CAD layout. 56
3.2 Example of OPC relevance on simple structures. 57
3.3 Schematic top view of the elementary structures. 58
3.3.a Illustration of the elementary electrical test structure. 58
3.3.b Illustration of alternated horizontal and vertical blocs. 58
3.4 Electrical test structure compatible seal-ring. 60
3.4.a Description of the seal-ring CAD layout. 60
3.4.b Perpendicular cross-section of a test structure seal-ring. 60
3.4.c Example of use of seal-ring in test structures. The dashed arrow corresponds to the cross-section in figure (b). 60
3.5 Cross section perpendicular to the copper lines of the C/S/C structure. . . 62
3.6 Cross-sections before (3.6.a) and after (3.6.b) aluminium etching correction. 63

3.6.a Perpendicular cross-section of a seal-ring, showing aluminium over etch. . . . 63
3.6.b Perpendicular cross-section of a test structure seal-ring after aluminium etching correction. . . . 63
3.7 Contact level cross-section in the same direction than the seal-ring before 3.7.a, 3.7.b and after 3.7.c the contact etch recipe shape regularity improvement. . . . 64
3.7.a Bad contact aspect before recipe modification. . . . 64
3.7.b Contact bar wiggling in seal-ring longitudinal section before recipe modification. . . . 64
3.7.c Good contact aspect after recipe optimisation. . . . 64
3.8 Percentage of dicing streets area as a function of the chip size for different street widths. . . . 65
3.9 CAD pad structure. . . . 66
3.10 Cumulative distributions of measured leakage currents at 15V for test structures having different pad widths. . . . 67
3.10.a Cumulative distributions of measured leakage currents at 15V measured on structures with 70μm-wide pads. . . . 67
3.10.b Cumulative distributions of measured leakage currents at 15V measured on structures with 30 μm-wide pads. . . . 67
3.11 Cumulative serpentine resistance 30μm-wide pads structures. . . . 67
3.12 SEM inspection of 30 μm-wide pads, showing heavily damaged pads. . . . 68
3.13 Cumulative leakage currents measured at 15V on 50μm-wide pads. . . . 68
3.14 SEM image of an important crack diving under the passivation layer of a 50μm-wide pads. . . . 69

4.1 Recovery of leakage current and time-to-breakdown by a 72 hours anneal at 300°C on moisturised test structures. . . . 72
4.1.a Leakage current distributions of test structures before and after a 72 hours anneal at 300°C. . . . 72
4.1.b Time-to-breakdown Weibull distributions of test structures before and after a 72 hours anneal at 300°C. . . . 72
4.2 Methodology applied on test and reference wafers. . . . 73
4.3 Effect of 168h of storage at 85°C/85% RH compared with room conditions. 74
4.3.a Time-to-breakdown Weibull distributions of protected test structures before and after 168h of storage at controlled conditions. . . . 74
4.3.b Time-to-breakdown Weibull distributions of unprotected test structures before and after 168h of storage at controlled conditions. . . . 74
4.4 Effect of 168h of storage at 105°C/100% RH and 2 atmospheric pressure compared with room conditions. . . . 74
4.4.a Time-to-breakdown Weibull distributions of protected test structures before and after 168h of storage at controlled conditions. . . . 74
4.4.b Time-to-breakdown Weibull distributions of unprotected test structures before and after 168h of storage at controlled conditions. . . . 74
4.5 Effect of increasing the anneal temperature on the moisture content and moisture-related absorption bands. . . . 76

4.5.a -OH bonds region normalised area evolution after respective 1 hour anneals at increasing temperatures. 76
4.5.b MIR absorption spectra after respective 1 hour anneals at increasing temperatures. 76
4.6 Median times-to-breakdown at different electrical fields along with the Root-E (R-E), Power Law (PL) and Impact Damage (ID) models respective trends. 77
4.7 R^2 values for Root-E (R-E), Power Law (PL) and Impact Damage (ID) models with backward and forward fitting. 78
4.8 Weibull plots of time-to-breakdown for different C/S/C structure lengths. . 79
4.8.a Weibull plots of time-to-breakdown for different protected C/S/C structure lengths. 79
4.8.b Superposition of Weibull plots of time-to-breakdown for different protected C/S/C structure lengths. 79
4.9 Weibull plots of time-to-breakdown for different unprotected C/S/C structure lengths after translation. Days since fab-out are indicated. 80
4.10 Optical inspection showing an extrusion of the upper BEOL layer, consequence of the temperature rise caused by the breakdown. 81
4.11 OBIRCH polarised area highlighting (green) on a S4BP test structure after dielectric breakdown. 82
4.12 Equivalent circuit after oxide breakdown. 83
4.13 Breakdown point location percentage as a function of structure length percentile. 84
4.14 Leakage current evolution during CVS tests of unpolluted test structures. . 85
4.14.a Leakage current evolution during CVS tests at different electrical fields. 85
4.14.b Leakage current evolution during 60V CVS tests performed on different C/S/C structure lengths. 85
4.15 Leakage current evolution during 60 V CVS tests of moisturised test structures. 86
4.16 Voltage evolution during CCS tests of unpolluted test structures. 87
4.16.a Voltage evolution during CCS tests on SR3BP structures at different forced currents. 87
4.16.b Voltage evolution during 250 pA CCS tests performed on different C/S/C structure lengths. 87
4.17 Equivalent capacitance integration from CCS measurements. 87
4.17.a Example of integration of CCS curve on a SR5BP test structure from figure 4.16.b 87
4.17.b Distributions of equivalent capacitances for different C/S/C structure lengths. 87
4.18 Voltage evolution during CCS tests at different currents performed on unprotected test structures. 88
4.19 Voltage evolution during CCS tests at 2nA at different temperatures performed on unprotected test structures. 89
4.20 Successive I-V characteristics from a SR3BP test structure. 90
4.21 SE and PF fitting plots. 91

4.22 SE and PF apparent activation energies. 92
4.23 Successive I-V characteristics from S3BP and SR3BP test structures (characteristics from SR3BP structures are taken from figure 4.20). 93
4.24 Emission sources spectra [155]. 94
4.25 Front side EMMI image of a S3BP structure without seal-ring. Indicated bias are applied on the serpentine while the combs are kept to a 0V potential. 94
4.26 Comparison of TVS characteristics of SR3BP structures at 25°C (a) and 60°C (b) after different hold times with a sweep speed of 0.1V/s. 96
4.26.a TVS characteristics of a SR3BP protected test structure after different hold times at 25°C. Ramp from 35V to -35V at 0.1V/s. . . . 96
4.26.b TVS characteristics of a typical SR3BP protected test structure at 60°C after different hold times. Ramp from 35V to -35V at 0.1V/s. 96
4.27 TVS characteristics of S3BP structures at 25°C (a) and 60°C (b) after different hold times with a sweep speed of 0.1V/s. 97
4.27.a 97
4.27.b 97
4.28 Double TVS sweep responses of unprotected S3BP (a) and unprotected SR3BP (b) test structures at 60°C. Ramp from 35V to -35V at 0.1V/s. . . 97
4.28.a 97
4.28.b 97
4.29 Space charges movement scenario during double TVS sweep of an unprotected S3BP test structure. 98
4.30 Transient capacitance of wet (S3BP) and reference (SR3BP) test structures under CVS. 99
4.31 Band diagram of unpolluted integrated SiOC:H dielectric under electrical bias. 101

List of Tables

2.1 Interesting chemical bonds summary table and associated literature. 49

3.1 Metal C/S/C structure length variations summary. S stands for surface. . . 59
3.2 Top metal level line space and width variations summary table. 59
3.3 Top metal level line space and width variations summary table. 62

4.1 Unsuccessful moisture ingress acceleration climatic storage conditions. . . . 75
4.2 Breakdown point bloc number for both localisation methods. 83

General introduction

"The human mind is our fundamental resource."

John F. Kennedy

Microelectronics emergence is undoubtedly one of the greatest revolutions of human history. Since its premises, in the late fifties, it has allowed capabilities almost unimaginable, from incredible computing power, artificial intelligence-enforced imaging devices in our pockets to space exploration, complex bio-chemical simulations and numerical weather prediction. Microelectronics was a key enabler of the remarkable computing soaring, increasing the chips computing power and their energy efficiency at an extraordinary pace. This technological odyssey spanning over seven decades has led chips to become an integral part of our daily life.

This broad spectrum of chips can be divided into two main categories: the first composed of comfort electronic devices where malfunction has no other consequence than user dissatisfaction, in which we can find, connected light bulbs and other smart objects, remote controls, smartphones etc. The second category is chips used in critical applications in which human life is at risk in case of device failure such as Anti-lock Braking System (ABS) in vehicles, pacemakers in medicine, or avionics for instance. Of course, the first category obeys mainly business constraints while the latter is rightly subjected to rigorous controls and demanding industrial standards. These constraints, applied at the system level, can be tackled with different strategies: subsystem redundancy, worst case operation mode lifetime estimation, and chips and software reliability amelioration. Original Equipment Manufacturers (OEM) use a combination of these strategies to strictly comply to conservative industrial standards at costs compatible with the mass market.

Therefore, for critical applications, reliability is an important aspect of chips performances. Thus, to grant microelectronics devices usability in those types of application, it is crucial for the semiconductor industry to provide reliable chips. Several decades of material studies and process Research & Development (R&D) brought the semiconductor industry to a remarkable control and understanding of the chips failure modes. Indeed, it is not difficult to find off the shelves chips with lifetimes of twenty years. Such long lifetimes are guaranteed thanks to lifetime extrapolation models that take into account physical phenomena responsible for chips degradation.

However, these models do not consider eventual moisture contamination which appears to be detrimental for chips reliability, especially those which target high reliability demanding applications such as automotive, medical or avionics. Despite moisture countermeasures are widely accepted to be efficient to prevent moisture penetration in chips

circuitry, our inability to understand the underlying phenomena leading to moisture-related electrical performance degradation of SiOC:H low-κ dielectrics materials, makes it difficult to screen along the manufacturing process as well as at Parametric Test (PT) and Electrical Wafer Sort (EWS) steps. Consequently, it is necessary to understand thoroughly the moisture-induced mechanisms at the chemical level in order to provide tools and methodologies to detect moisture as soon as possible during the manufacturing process or the chip operational life. Furthermore, to be of any use to the semiconductor industry, any material chemical modification must be correlated with electrical behavioural properties changes.

To this extent, our work focusses first on the specific properties of dielectric materials that make it particularly suitable for microelectronics insulators. Then, the integration process and the SiOC:H chemical structure is detailed, afterwards the test structures conception and optimisation are presented. Finally, electrical characteristics of the SiOC:H dielectric and the influence of moisture are studied.

Chapter 1

Interconnects and dielectrics

"Books permit us to voyage through time, to tap the wisdom of our ancestors."

Carl Sagan

1.1 Introduction

Semiconductor industry has come a long way since the first monolithic integrated circuit on silicon, abbreviated in IC by specialists, by Robert Noyce in 1959 [5] at Fairchild Semiconductors, which he co-founded in 1957. This milestone sets the starting point, not only of the semiconductor industry, but of a frantic technological odyssey bringing humankind to the digital era. It can be demonstrated that every logical operator can be decomposed in a combination of basic operators: NOT, AND and OR, into a sum of products (SoP) or a product of sums (PoS), also called sum of minterms and product of maxterms respectively [6]. In practice, NAND and NOR gates are universal as they allow to describe every logical operation [6]. These functions can be made with interconnected transistors, that are the building block of the CMOS technology, to enable complex logical operations on doped silicon substrates. In a schematic view, an IC is composed of two regions: the Front-End-Of-Line (FEOL), which contains the transistors, and the Back-End-Of-Line (BEOL) which is composed of metallic lines that connects the transistors to enable logical functionality of the circuit. In other words, FEOL and BEOL together are absolutely necessary for complex logical operations.

1.2 Modern microelectronics and Moore's law

Since the late fifties, continuous technology scaling brought microelectronics in almost every aspect of our life. This has been possible at the cost of extensive theoretical, practical and operational developments [7]. Semiconductor industry is one of the most cost intensive in the world, consequently, cost planning and industry roadmaps, such as Moore's law [8], are necessary so new process and material developments can be conducted years in advance [9].

1.2.1 From kettles to pacemakers: chips surround us

Electronic devices are more and more common in our daily life. The most visible part of how microelectronics already changed it, is telecommunications, smartphones and computing, allowing unprecedented data processing capabilities, among other things. Furthermore, even though the Internet of Things (IoT) might seem embryonic as we speak, it is rapidly emerging [10]. The IoT trend tends to make objects interact with their environment, to be controlled remotely, to self-adapt, in brief, make users lives simpler and easier. These smart devices require more and more advanced functionalities such as communication protocols, memory storage capacity or computational power. Depending on the application's constraints, one or several aspects will be favoured. For instance, a temperature settable kettle only requires modest computational power but need I/O scanning on thermal sensors outputs. Microelectronics is also rapidly expanding in automotive by engine control and Anti-lock Braking System (ABS) for instance but also in medicine where pacemaker implantations are now routine procedures worldwide [11].

1.2.2 Moore's Law and interconnects

In order to allow such continuous improvement and emergence of devices, more and more computational power and data storage density and efficiency are required [12]. They are mainly achieved by reducing the silicon footprint of the transistors. Consequently, increasing the chips capabilities is performed at the cost of extensive process studies and developments, not to mention the prohibitive cost of semiconductor industry equipment. Nonetheless, thanks to the tremendous amount of technological know-how, manpower and brain power needed from circuit design to final packaging, the semiconductor industry technology scaling follows Moore's law and thus, the semiconductor industry remains economically viable [13]. This empirical law predicts that the number of logic transistors doubles every 18 months on microprocessor chips as the industrial product historic in figure 1.1 traces it [14].

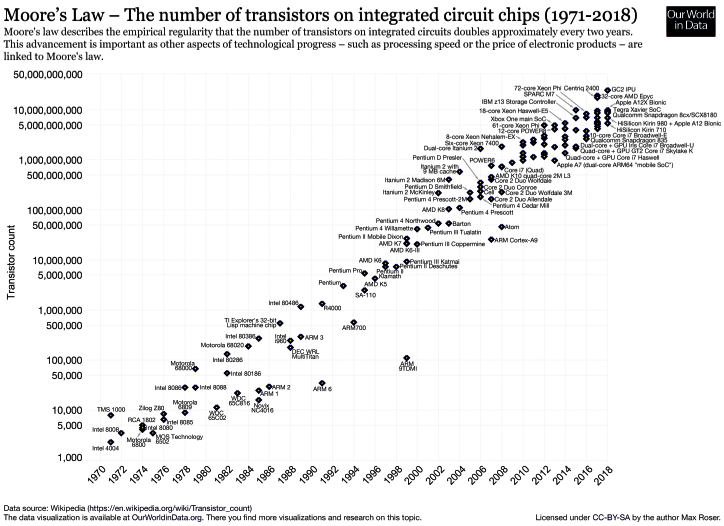


Figure 1.1: Moore's law, with major commercial processors names

In order to achieve such challenging targets, a reference roadmap lists semiconductor

near future challenges and trends such as transistor gate length, interconnect dielectric constant, metallisation materials. These reference documents, referred as International Technology Roadmap for Semiconductors (ITRS), are regularly updated with the latest technological advances by an experts group representing worldwide leading semiconductor companies. A straightforward consequence of the scaling of the transistors is the scaling of the interconnection circuitry. Indeed, interconnects and BEOL in general, had to keep the pace of the transistor shrinking. This led to significant challenges in manufacturing and material development. That is why in ITRS guidelines, dielectrics draw particular attention, and especially the need for low-κ dielectrics in the chips interconnect [9].

1.3 Dielectrics

Dielectrics materials play an important role in the semiconductor industry. Indeed, a myriad of dielectrics are needed to achieve functional chips, but some of them are of primary importance, this is the case of the dielectric that separate metallic lines, also referred as Inter-Metallic Dielectric (IMD).

1.3.1 Role of dielectrics in chips interconnects

From theory researches to manufacturing engineering, dielectrics are one of the building block of the past decades progresses of the semiconductor industry, allowing to pursue Moore's law. Dielectrics used in chips interconnects are of great importance because they have a significant impact on the chips performance. For instance, the leakage current in the BEOL could be detrimental as lines with opposite electrical potentials can run close to each other for very long distances, sometimes several millimetres. This is particularly true in large memory arrays because main memory technologies, such as Flash, require potential differences as high as 20V distributed to every memory cell to erase it [15].

Such demanding requirements were initially fulfilled by silicon dioxide, SiO_2, however 50 percent of the total power consumed by the chip was dissipated by the interconnect for the 130nm technology node [16], with an aluminium/SiO_2-based BEOL. This finding, led the industry to search for alternative materials to be used in the BEOL to enable further interconnect scaling.

In 1993, after more than a decade of intense R&D, copper/low-κ-based BEOL is brought to the market by IBM with the famous PowerPC 750 [17]. This pioneer microprocessor, originally designed to be fabricated with an aluminium/silicon dioxide-based BEOL, saw a jump of performance of 30 percent when a copper/low-κ-based BEOL was used and thus, quickly, copper/low-κ-based BEOL became the industrial norm. It is important to note that this BEOL material transition, constituted one of the major disruptions of the semiconductor industry history.

Indeed, more than a simple technological development, the introduction of copper/low-κ interconnect constituted a profound mutation in the BEOL fabrication with the introduction of the dual-damascene manufacturing process. For a cohort of reasons, such as issues of copper etch and contamination, the dual-damascene process imposes the dielectric to be etched instead of the metal, followed by metallic lines deposition. This process is described thoroughly in section 2.2. One can obviously note that throughout the manufacturing process, IMD must undergo an important series of thermal and mechanical

treatments, consequently, its properties must remain stable and exhibit the wanted low permittivity value to enable high performance chips.

1.3.2 Low permittivity dielectrics: macroscopic and microscopic principles

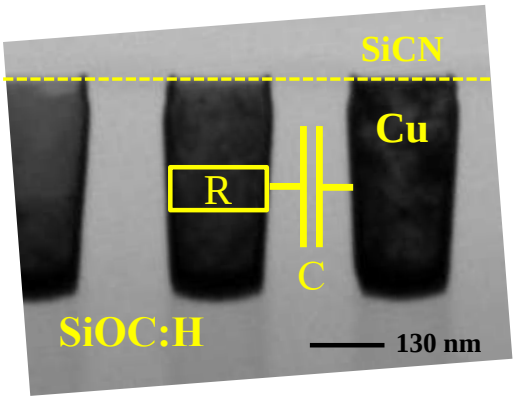
Accordingly, it is necessary to have a good understanding of these IMD materials. SiOC:H low-κ materials are relatively recent but, dielectrics are not specific to microelectronics and their properties have been studied for decades. Hence, some aspects of the dielectric theory are of particular interest in the scope of our study.

1.3.2.1 Macroscopic key parameters

Due to the fact that many dielectrics are used in the semiconductor industry, they present a wide range of macroscopic electrical behaviour. Therefore, it is needed to categorise these materials to compare them and assess their pertinence. This section will focus on relevant macroscopic parameters for IMD applications.

1.3.2.1.1 Capacitance and resistance

Firstly, BEOL metallic lines can be described using a simple resistance-capacitance model [18]. Figure 1.2 shows the provenance of the equivalent devices of the model: the resistance is due to the metallic line length, width and height and the capacitance is constituted by the dielectric material separating two metallic lines. Thus, the maximum theoretical circuit operating frequency is given by its cut-off frequency, which can be expressed as:



$$f_c = \frac{1}{R.C} \tag{1.1}$$

Figure 1.2: Resistance-Capacitance equivalent circuit in the BEOL.

Where R is the resistance of the metallic line and C is the dielectric capacitance. Hence, it is clear that chips performances would greatly benefit a line with lower resistance and a dielectric with lower capacitance. Therefore, copper replaced aluminium because of its better conductivity [18] while SiOC:H replaced standard SiO_2 due to its lower dielectric constant [19].

1.3.2.1.2 Dielectric constant

Assuming that the capacitance between two metallic lines is planar, the previous expression can be detailed as:

$$f_c = \frac{e}{R.\kappa.S} \text{ with } \kappa = \epsilon = \epsilon_r.\epsilon_0 \tag{1.2}$$

where R is the metallic lire resistance, e the space between two metallic lines, S the area of the metallic lines facing each other, κ the dielectric permittivity, ϵ_r the material relative permittivity, ϵ the material permittivity and ϵ_0 the free space permittivity. As the aim of the semiconductor industry is to increase profit by improving performances and reducing dimensions, e and S cannot be used to reduce the capacitance, hence κ must decrease to do so and to increase the cut-off frequency f_c. As one may note, vacuum permittivity is the lowest possible. Hence, minimal relative dielectric constant value is 1 for free space. Consequently, the ideal interconnect dielectric is void, also called air gaps, which are not trivial to manufacture, especially in the BEOL [20]. Therefore, to decrease the relative permittivity without using air, from the eighties, intensive R&D has been carried-out by leading-edge companies such as IBM, Motorola, Intel and their competitors to switch from the aluminium/silicon dioxide to a copper/low-κ-based BEOL now used in the industry [21]. To further reduce the relative permittivity, porous SiOC:H, often referred as ultra low-κ dielectrics, has been developed for the 65 nm technology node and below [22], [23], [24], [12].

1.3.2.1.3 Hardness and Young's modulus

An important issue encountered in the BEOL integration (see section 2.2) is the lack of mechanical resistance of low-κ dielectrics, SiOC:H is not an exception. Consequently, even though reducing the dielectric constant is crucial, low hardness and Young's modulus observed for low-κ dielectrics induces an important increase of the process complexity because of the constraints they involve. As an example, the Young's modulus of silicon dioxide is about 73 GPa while it is around 7.8 GPa for non-porous SiOC:H [25]. This has a non-negligible impact in the manufacturing, singulation, wire bonding, and packaging processes [23], [26], [27], [28]. As a consequence, lower-κ material integration slow-down is attributed to poor mechanical properties by the ITRS 2015 roadmap [9].

1.3.2.1.4 Thermal stability

In the same manner, the SiOC:H remarkable electrical properties hinge, among others, on the fact that it remains in amorphous phase [29]. Hence, its glass transition temperature, despite than higher than 450°C [30],[29], is important to consider throughout the manufacturing process flow to ensure the SiOC:H material does not crystallise. This is one of the main reasons why the thermal budget is limited (often to 400°C) during the interconnect manufacturing process.

1.3.2.2 Microscopic properties

Dielectric permittivity can also be interpreted at the microscopic level, hence it is in direct relation with the material chemical composition and characteristic structural bonds. Consequently, any pollutant might influence the electrical behaviour of a dielectric. Thus, microscopic consideration must be taken into account to understand how pollutants might influence the SiOC:H low-κ dielectric electrical behaviour.

1.3.2.2.1 Polarizability

Polarisation occurs when dielectrics submitted to an electrical field E, experience a charge distribution rearrangement: for which dipoles align with the external field. Four phenomena contribute to the global material polarizability: electronic, ionic, dipolar, and free space charges polarizability.

1.3.2.2.2 Electronic polarisation

The phenomenon occurring at the smallest scale is electronic polarisation, which corresponds to a deformation of the electronic cloud around atoms nucleus composing the dielectric material (figure 1.3). The electronic material polarizability per volume unit P_e, is given by:

$$P_e = N_e \alpha_e E = \chi_e \epsilon_0 E \tag{1.3}$$

with N_e is the number of atom per volume units, α_e the electronic polarizability, ϵ_0 the free space permittivity and χ_e the electric susceptibility of the dielectric also given by: $\chi = \epsilon_r - 1$, which in turn gives by substitution in the previous equation:

$$\epsilon_r = 1 + \frac{N_e \alpha_e}{\epsilon_0} \tag{1.4}$$

However, this expression only considers the dielectric volume as one macroscopic element submitted to an external field, which is not exactly true as it does not take into account the local field experienced by dipoles. This local field E_{local} is known as the Lorentz field and can be expressed as:

$$E_{local} = E + \frac{P_e}{3\epsilon_0} = \frac{\epsilon_r + 2}{3} E \tag{1.5}$$

Which in turns, by substitution in equation (1.3), gives finally:

$$\frac{\epsilon_r - 1}{\epsilon_r + 2} = \frac{N_e \alpha_e}{3\epsilon_0} \tag{1.6}$$

This relation, known as the Clausius-Mossotti equation, offers a direct relation between microscopic properties and dielectric constant, and allows to calculate any material dielectric constant theoretically.

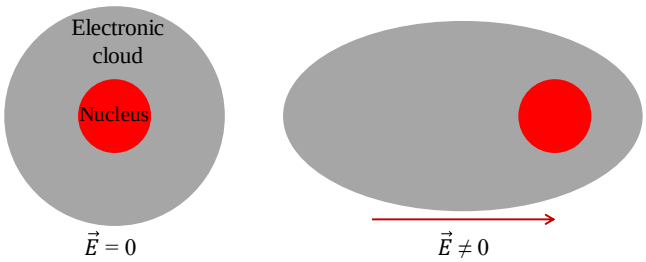


Figure 1.3: Schematic principle of electronic cloud polarisation event around an atom under an electrical field E.

1.3.2.2.3 Ionic polarisation

Ionic polarisation is the consequence of relative displacement of negative and positive ions in ionic crystals, when they are subjected to an electrical field, as illustrated in figure 1.4. This type of polarisation phenomenon is defined for charge-balanced crystals by:

$$P_i = N_i \alpha_i E_{local}$$

where α_i is the ionic polarizability per volume unit of the given molecule. Similarly to the electronic polarisation, this leads to a Clausius-Mossotti relation for ionic polarizability:

$$\frac{\epsilon_r - 1}{\epsilon_r + 2} = \frac{N_i \alpha_i}{3\epsilon_0} \tag{1.7}$$

in which N_i is the number of molecules per volume unit.

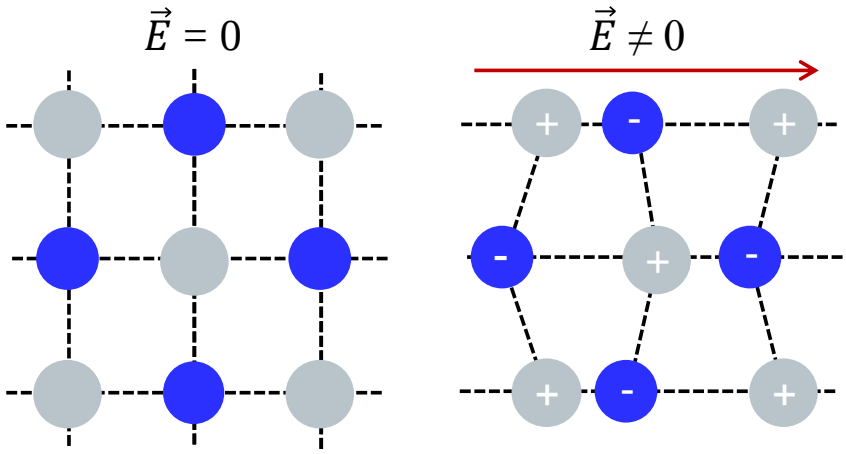


Figure 1.4: Schematic principle of ionic polarisation event in an ionic crystal under an electrical field E.

This phenomenon is common to all ionic bonds between two atoms having different electronegativities, as shown in figure 1.4, that induces a slight deformation of chemical bonds, hence of molecules, or lattices in crystals. It is worth noting that this type of polarizability, also referred as vibrational polarisation, is the physical basis of Fourier Transform InfaRed (FTIR) spectroscopy material analysis.

1.3.2.2.4 Dipolar polarisation

Some materials possess permanent dipoles (polar materials). Such permanent dipoles tend to align to the applied electric field E when their dipolar moments are randomly distributed in the absence of E field as illustrated in figure 1.5.

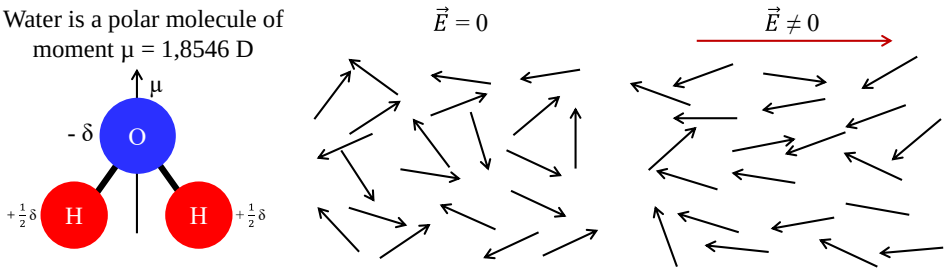


Figure 1.5: Schematic principle of dipolar polarisation event in a dielectric under an electrical field E.

The average dipolar polarizability per molecule α_d can be calculated to be:

$$\alpha_d = \frac{P_0^2}{3k_BT}$$

with k_B the Boltzmann constant, T the temperature , and $P_0$is the molecule dipole. It is worth noting that contrary to electronic and ionic polarizabilities, this type of polarizability explicitly depends on the temperature [31].

1.3.2.2.5 Space charges polarisation and remarks

A fourth type of polarizability can occur in non-ideal dielectrics: interfacial or space charge polarizability α_{sc}. Indeed, free charges in the dielectric material will migrate towards the appropriate electrode under the influence of the external E field. However, they remain in the material, blocked at the electrode interfaces and accumulate, creating macroscopic dipoles (figure 1.6). This type of polarizability is expected from non-bonded pollutants in an amorphous dielectric material.

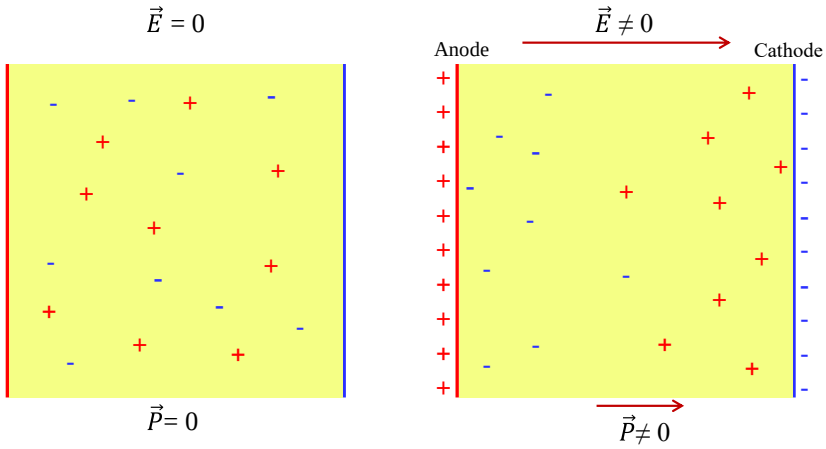


Figure 1.6: Schematic principle of free space charges polarisation event in a dielectric under an electrical field E.

To conclude, the total material polarizability α can be expressed as the sum of electronic, ionic, dipolar and space charge polarizabilities:

$$\alpha = \alpha_e + \alpha_i + \alpha_d + \alpha_{sc} \tag{1.8}$$

1.3.2.3 Capacitance frequency response

As mentioned in section 1.3.2.1.2, the dielectric capacitance is intimately linked to the dielectric constant, which is directly influenced by the material polarizability. As there are different types of polarizabilities physical root-causes acting at different scales, they are activated at different frequencies. Depending on frequency at which the dielectric is stimulated, one type of polarizability will dominantly influence the dielectric constant of the studied material. Phenomena described in the previous section (1.3.2.2) and their frequency activation domain are represented in figure 1.7, [32], [33]. It exposes the fact that for frequencies under a few tens of kHz, the material permittivity is modulated by free space charges in the dielectric. Indeed, at higher frequencies, polarisation changes are too fast to allow free space charges displacement in the material. Similar reasoning can be derived for other types of polarizabilities. For instance, electronic polarisation is characterised by a time constant of the order of the femto-second (10^{-15}s), which corresponds to very high frequencies of the order of the petahertz. Frequencies at which other types of polarizability are not fast enough to influence the material dielectric constant. At low frequencies, all types of polarizability add up on top of each other, which explains why, in a general manner, dielectric constant tends to be higher at lower frequencies.

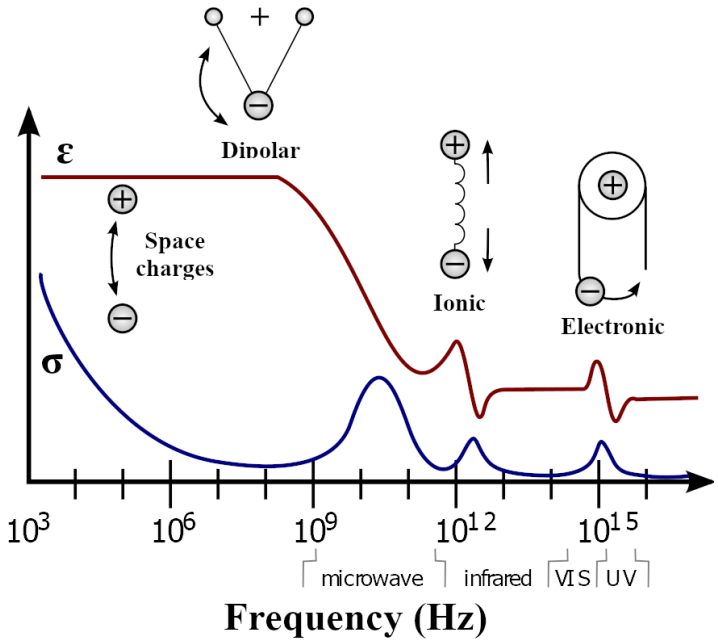


Figure 1.7: Different polarizabilities mechanisms implies different frequency responses. Here schematically, ϵ refers to the material dielectric constant, and σ to its conductivity (including dielectric loss).

As suggested by the figure 1.7 [32], at frequencies between 1kHz and a few GHz, which correspond to chip usual operation frequencies, the IMD dielectric constant is mainly due to the dielectric material ionic and electronic polarizabilities. However, at these frequencies, the IMD behaviour can be modulated by free space charges and by dipoles polarisations as their respective resonant frequencies are within the chip operational frequency range. Hence it is clear that space charges and dipolar polarizabilities must be

reduced as much as possible to guaranty a stable operation across the chip operational frequency range. This is consistent with the fact that free charge carriers associated with pollutants or defects in the dielectric material have an influence on the dielectric material polarizability, hence, on its dielectric constant, and thus on the interconnect effective capacitance [34]. That is why a study of the capacitance of the interconnect for different frequencies, despite the fact that interpretation in terms of polarizability might seems difficult at prime sight, is of interest. However, such study of the frequency response might be limited by the access resistance, R_s, of the electrical characterisation structure in the equivalent capacitance measurement shown in figure 1.8.

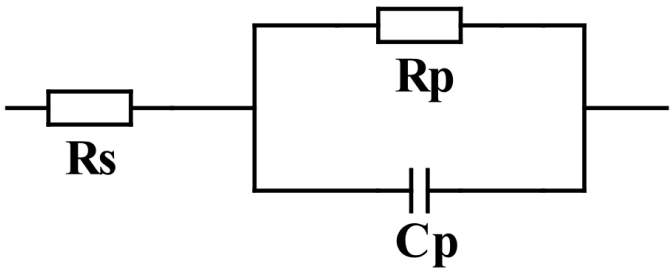


Figure 1.8: Parallel capacitance measurement model with the addition of a series resistance R_s accounting for the access resistance of the structure.

From this small-signal equivalent circuit, it is possible to compute the cut off frequency of this low-pass filter. The equivalent frequency-dependent impedance of the structure, Z, is expressed as:

$$Z = R_s + \frac{\frac{R_p}{jC_p\omega}}{R_p + \frac{1}{jC_p\omega}} \tag{1.9}$$

with j the imaginary unit and ω the pulsation. Then, the equivalent capacitance C_{eq} is given by:

$$C_{eq} = \frac{1}{1+\alpha^2\omega^2\tau^2}\left(\frac{R_p}{R_p+R_s}\right)^2 Cp \text{ with } \alpha = \frac{R_s}{R_p+R_s} \text{ and } \tau = R_pC_p \tag{1.10}$$

which gives, a cut-off frequency $f_c = \frac{1}{2\pi\alpha\tau} = \frac{1}{2\pi R_sC_p}$ (with $R_p >> R_s$). Consequently, the higher the access resistance R_s and the capacitance C_p, the lower the cut-off frequency. Figure 1.9, underlines the fact that equation 1.10 describes accurately our situation as the experimental cut-off frequency is approximately 5 kHz while the theory predicts 3 kHz. The difference observed is due to the equipment capacitance (likely a few pico-Farads) and the approximation made for the calculation of f_c: $R_p >> R_s$.

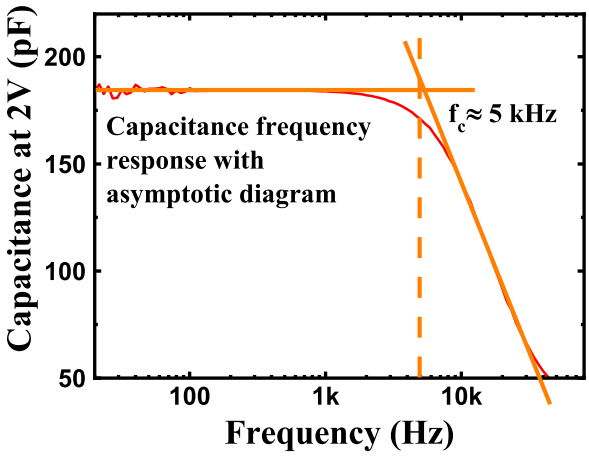


Figure 1.9: Frequency response of standard BEOL structure (see section 3.3 for more details) showing frequency limitation from access resistance.

As a consequence, for the following of our study, it has been chosen to measure the capacitance at 1kHz to avoid the influence of the series resistance on the measured values.

1.3.3 Strategies to reduce the permittivity

In order to have higher theoretical cut-off frequencies, the dielectric constant must be decreased (see section 1.3.2.1). From physical mechanisms described in section 1.3.2.2, several working principles can be derived to achieve this: choose low electronic polarizability materials to constitute the dielectric [35], decrease the electronic density [34], [25], [36], prioritise lowly polar chemical molecular structures [19], [31], [25], and obviously improve process control to reduce defects and pollutants density in the dielectric material [37], [34], [38]. These strategies must also take into account all constraints relative to the BEOL process integration as detailed in section 1.3.2.1.3 and to what extent candidate materials could be damaged by chemical and mechanical treatments occurring along the manufacturing process (see more details in section 2.2). Therefore, they have been combined to develop the SiOC:H low-κ dielectric material that is an industry standard now. This SiOC:H dielectric material has been chosen for its low permittivity, but also because it exhibits better mechanical and chemical properties than its alternatives [39]. Moreover, electrical reliability is also crucial in order to guarantee chips long-term operability.

1.4 Interconnect reliability

As the interconnect reliability is an important aspect of the chips reliability, it has been studied extensively. Several failure modes can be distinguished, hence require specific attention to contain the related issue. It is the subject of constant research and process developments, in particular with SiOC:H which demands great caution during manufacturing because of its sensitivity to external factors. Indeed, as detailed in 1.2, pristine SiOC:H dielectric material has a relative permittivity of 2.9, which is the reason why it replaced SiO_2, which has a dielectric constant of 3.9 [40]. However, despite its

tremendous electric qualities as insulator, it exhibits significant weaknesses with respect to copper diffusion, mechanical properties, and thermal stability [29].

1.4.1 Interconnect failure modes

Failures in the chips BEOL can have different root-causes that are associated with different parameters and physical phenomena. These are very diverse, hence we do not intend to provide an exhaustive overview of all BEOL failure modes but the main ones and those which are interesting in the scope of our study because of their link with SiOC:H dielectric material: delamination, copper lines electromigration, copper diffusion and, dielectric breakdown.

1.4.1.1 Delamination

Delamination can sometimes be observed after mechanical stress of the BEOL. This is the case at the die singulation step at the end of the wafer fabrication, when strong sear forces are applied to the die [26]. Similar delamination and crack can also occur after singulation during the wire bonding step [27]. This type of failure is particularly problematic because it occurs at the end of the fabrication, hence from an industrial point of view, it is very costly. It is attributed to the SiOC:H poor mechanical properties. Indeed, low Young's modulus and hardness of the SiOC:H material (see section 1.3.2.1.3 for details), induces important variations in the interconnect because SiCN and copper exhibit better rigidity, hence less damages because of mechanical stress (compressive and shear). Figure 1.10 is an example of dramatic delamination and crack diffusion in a chip BEOL provoked by wire bonding [41].

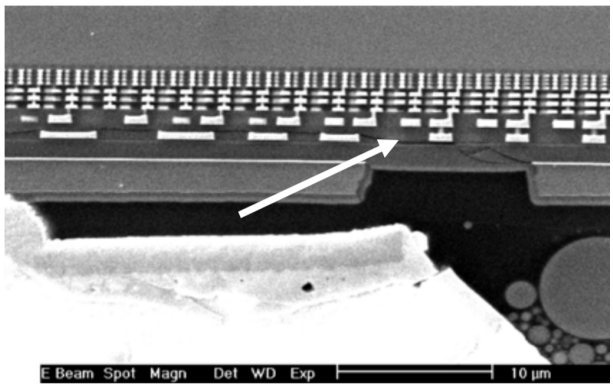


Figure 1.10: Example of delamination and crack diffusion in a chip BEOL.

Delamination is one of the main challenges of the integration of advanced dielectric materials in the interconnect [9].Containment of this failure requires a good control of the steps involving mechanical stress such as Chemical-Mechanical Planarisation (CMP) (see section 2.2 for more detail) and all steps, from wafer thinning, to packaging through dicing.

1.4.1.2 Copper and tantalum diffusion

Another failure mode, which was at the centre of the attention when low-κ/copper BEOL was introduced, is copper diffusion in the SiOC:H low-κ dielectric material [42]. Copper contamination is critical throughout the manufacturing process because copper is known to diffuse easily in the SiOC:H as exemplified by Baek et al. [43]. This results in electrically active defects in the material, strongly degrading its insulating properties between metallic lines and vias. To prevent such harmful effects, robust copper Ta/TaN diffusion barrier and SiCN capping layers are added as described in sections 2.2.4 and 2.2.8. The Ta/TaN barrier when correctly deposited prevents copper diffusion in the SiOC:H dielectric, however, non-conformal Ta/TaN bilayer might result in catastrophic copper atoms migration. Indeed, atomic copper diffusion in the dielectric results in facilitated electron conduction between two adjacent metallic lines, leading to increased power consumption, possible voltage drops across the circuit and eventually to an early breakdown. Even though this bilayer diffusion barrier is absolutely required, it increases the total line resistance, thus the thinner the better [44]. Consequently, a good control of the Ta/TaN barrier deposition process (see details in section 2.2) is required to achieve good reliability and performance. It is worth noting that moisture diffusion in the BEOL has important consequences on the Ta/TaN diffusion barrier integrity. In fact, the tantalum composing the barrier might be oxidised by moisture, then the bilayer becomes permeable to copper or even migrate in the SiOC:H [45]. The following figure 1.11 is an example of tantalum diffusion in the SiOC:H dielectric from Wu *et al.*[46].

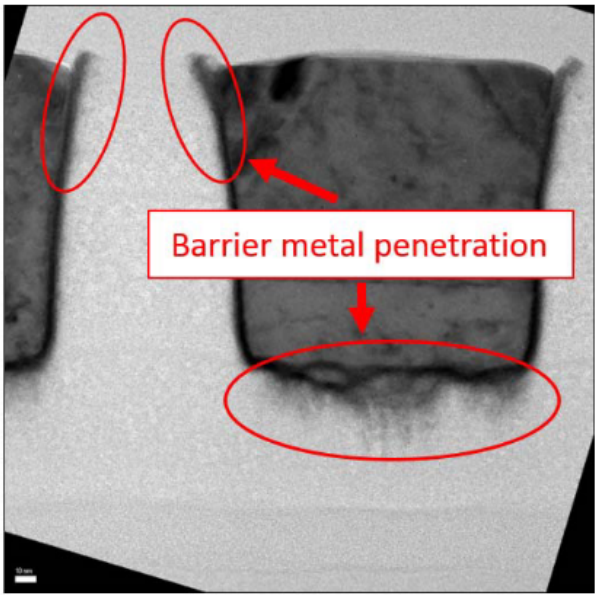
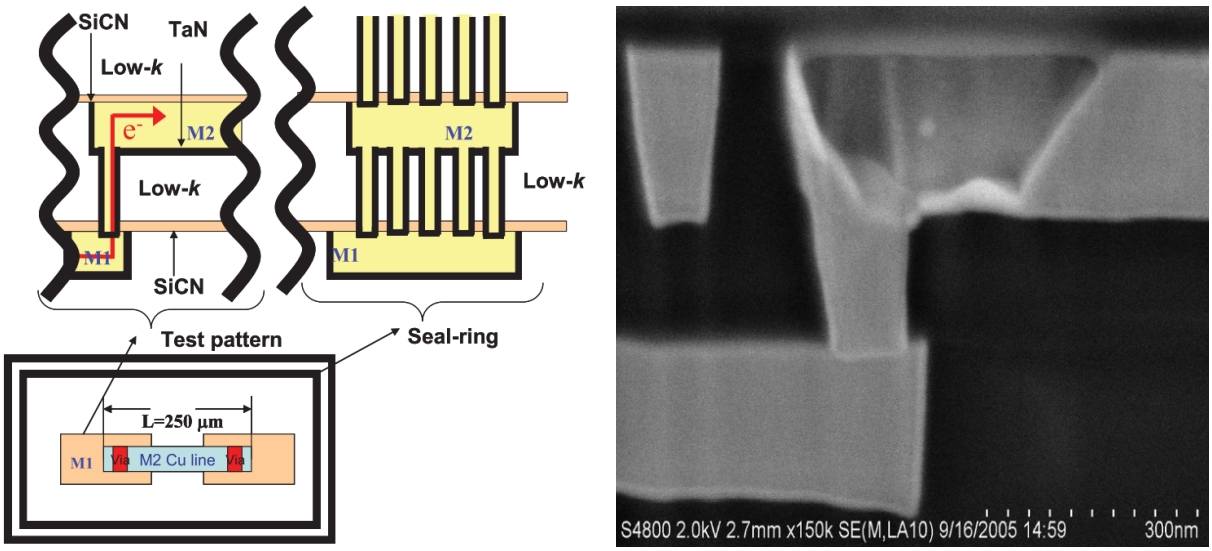


Figure 1.11: Example of tantalum diffusion barrier diffusion.

1.4.1.3 Electromigration

Electromigration is an electrical failure mode resulting from copper atom displacement in the metallic lines under the influence of an intense electron flow flowing through the metallic line [47], [48]. In fact, copper interfaces play a very important role to ensure copper adhesion robustness to other materials, such as Ta/TaN diffusion barrier,

and constitute the main factor that limit the BEOL electromigration performance [47]. Consequently, copper interface engineering and adhesion robustness improvements are the main subjects of study to augment the maximum current density limit. The chips performance in terms of electromigration is assessed thanks to dedicated structures that allow to highlight the effect of the line-to-via interface as pictured in figure 1.12.a by Cheng et al. [49].



(a) Electromigration structure.

(b) SEM cross-section of a line after an electromigration test from Cheng et al.. A void without copper is seen on top of the via.

Figure 1.12: Electromigration structure and failure principle.

As the electromigration performance depends on the adhesion strength of copper with the surrounding materials, *i.e.* Ta/TaN and SiCN mainly, they are affected by moisture diffusion at the interfaces, which are possible diffusion paths [50]. This detrimental effect of the moisture diffusion at the interfaces between copper and SiCN is known and is the main reason why electromigration test structures are protected from moisture diffusion (see section 1.5.2 for the detail of moisture diffusion countermeasures) [49]. More specifically, unprotected test structures have shorter time-to-failure than test structures protected against moisture diffusion [51].

1.4.1.4 Dielectric breakdown

Another common failure mode is the dielectric breakdown. It is the consequence of the material catastrophic failure under the influence of an electrical field applied across the dielectric material. This failure mode is regularly encountered during technology and chips development as it allows to evaluate the quality of dielectrics. Indeed, lifetime extrapolation models (detailed in 1.4.3) are used to estimate dielectrics lifetime at actual chips operating regime from accelerated tests (detailed in 1.4.2). To be more specific, state-of-the-art SiOC:H dielectrics usually experience different behaviours under electrical stress. First, some injected charges recombine or are trapped by defects within the dielectric [52].

Moreover, electrons can cross the whole dielectric material, sometimes generating new defects by electron-atom collisions [46], [53]. When the dielectric has experienced important degradation, *i.e.* when numerous defects have been generated, a conduction path, also called percolation path, is formed between the two electrodes: it is the dielectric breakdown [53]. Physical root-causes of trapping, recombination and degradation mechanisms and to a lesser extent conduction mechanisms across SiOC:H dielectrics material, leading to dielectric breakdown are still debated in the scientific community [54]. Because the breakdown generates an important destruction around the concerned zone, consequence of the sudden temperature rise producing the melting of the region, it is difficult to analyse. The following figure illustrates the extent of the damages induced by dielectric breakdown (figure 1.13) [55].

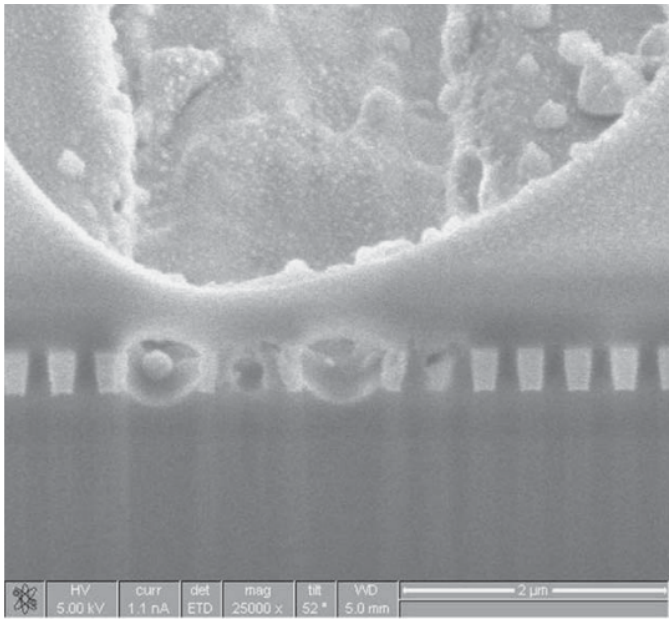


Figure 1.13: Cross-section view of a catastrophic breakdown between metallic lines.

As dielectric breakdown is induced by the application of a voltage, it is necessary to study the behaviour of the interconnect under an applied electric field in order to gather information on the dielectrics electrical mechanisms leading to breakdown. This reason alone justifies the vast diversity of electrical characterisation techniques and the constant research for more elaborated techniques.

1.4.2 Usual electrical characterisation techniques

Electrical characterisation allows to retrieve an important amount of information related to the quality and electrical performances of a material. This section details usual IMD characterisation techniques that are necessary to the following of our study, particularly in chapter 4.

1.4.2.1 Current-Voltage characteristics

Current-Voltage characterisation, abbreviated as I-V, is a very common tool for dielectric characterisation in the semiconductor industry, for material development and failure analysis for instance. Despite the fact that I-V characteristics quantitative analysis is often limited, it is a preponderant tool to spot eventual changes of conduction mechanisms across a wide range of electrical fields (explored in section 4.5). Also, it can provide information on the material electrical behaviour, which is particularly valuable in case of unexpected premature breakdown or increased leakage current. It is often used in comparing suspicious I-V characteristics with those obtained on non-impacted structures. Figure 1.14 is an example of characteristics obtained on standard BEOL structures (see section 3.3 for more details) and represented in a semi-logarithmic graph. As one can see, all plots present very similar shapes and values. Differences between plots also provides information on the fabrication quality, the smaller the dispersion, the better.

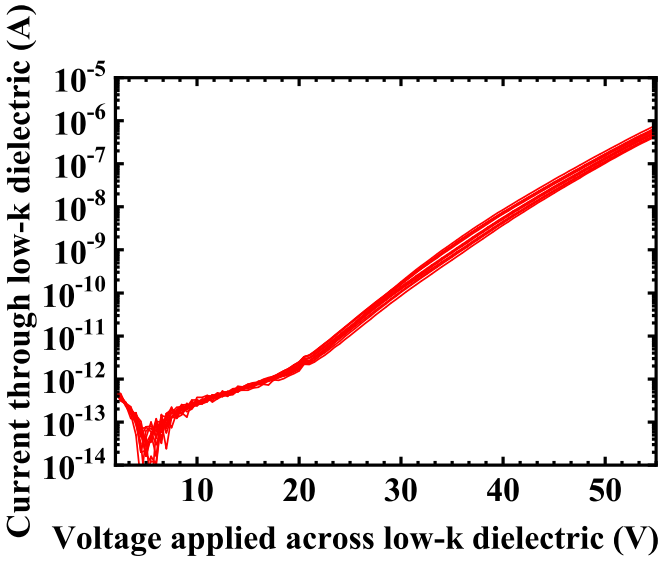


Figure 1.14: Stacked leakage current-voltage characteristics of standard interconnect structures.

1.4.2.2 Parametric tests

Parametric tests are notably used at the end of the manufacturing process in order to control the quality of the chip fabrication. Indeed, they offer a fast method to compare electrical parameters across photo-lithographic fields, wafers, and lots providing sufficient data for statistical analysis. This corresponds to a dedicated step at the end of the fabrication, purposely referred as Parametric Test (PT). In consequence, it is often performed on an Automatic Test Equipment (ATE), also called familiarly a prober. However, all photo-lithographic fields of every fabricated wafer cannot be tested as it would require an unbearable amount of test time and ATE. That is why, statistical sampling is required. Usually, only 5 photo-lithographic fields are measured per 200 mm diameter wafer in mass production, and 9 per 300 mm diameter wafer. It is worth noting that, PT step covers the whole range of electrical parameters of actual chips, including FEOL devices and obviously BEOL structures. Amongst the large number of measured parameters, some

particularly draw our attention in the scope of our study: interconnect leakage current, capacitance and resistance values.

1.4.2.2.1 Leakage current

Leakage current though the SiOC:H dielectric material is of great interest as it directly measures the performance of the dielectric as insulator at a given electrical field in the chip interconnect, which is crucial to ensure low power consumption. Leakage current measurements can be performed at different electrical bias depending on the phenomenon to be observed. Alternatively, it can also be used to track possible evolutions in the electrical performance of the IMD at a given electrical field. In our case, leakage current measurements require a high precision low noise equipment because we are studying thick low-k dielectrics that exhibit very low leakage currents. They are generally represented in cumulative distribution plots by wafer, lot or other groups as in figure 1.15, which represents a semi-log cumulative distribution of the leakage currents measured at 15V between two metallic lines in a standard SiOC:H-based BEOL structure (see section 3.3 for more details).

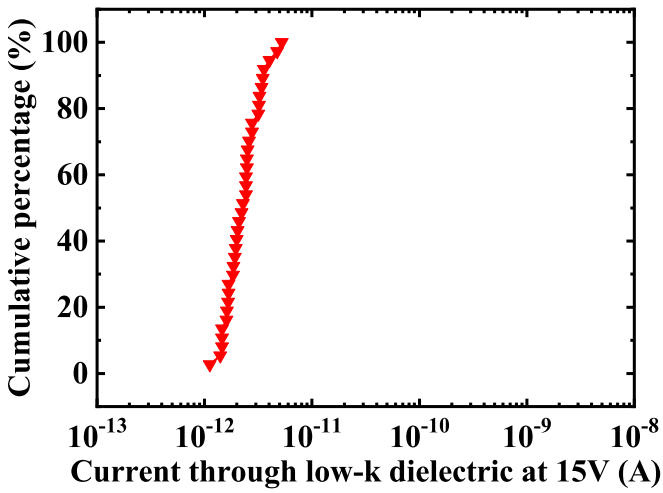


Figure 1.15: Semi-log cumulative distribution of leakage currents measured at 15V bias.

1.4.2.2.2 Capacitance

Another important parameter measured on BEOL structures, is the capacitance. Indeed, as mentioned in section 1.3.2.2, the capacitance value is linked to the dielectric macroscopic and microscopic properties. Consequently, it is a powerful indicator to evaluate the BEOL process quality and electrical performance. A lower-than-target capacitance value can sometimes be explained by a larger line-to-line spacing for instance while a higher capacitance value can be the consequence of pollutant presence in the dielectric [56], resulting in a change of microscopic properties (see section 1.3.2.2). Parametric capacitance values at a given frequency are usually analysed in similar plots than leakage currents, *i.e.* standard cumulative distributions as shown in figure 1.16. However, it is more appropriate to use linear horizontal axis as capacitance values vary of small quan-

tities for a specific measurement compared to leakage currents that can span over several decades under the influence of pollutants for instance.

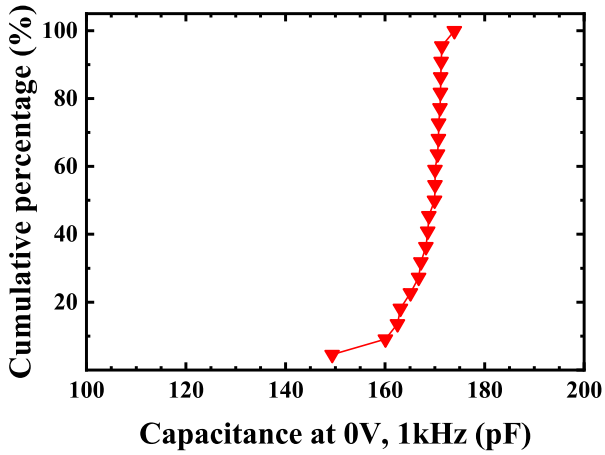


Figure 1.16: Cumulative distribution of capacitances values measured at 1kHz, 200mV amplitude AC signal under 0V DC bias.

1.4.2.2.3 Resistance

Metallic line resistance measurement is also important as it is an indicator of the interconnect well-being. It is a mean to evaluate the metal deposition process quality and eventually detect important damages such as voids in lines or metal corrosion. More specifically, the resistance change over time might be monitored to spot eventual metal degradation in the BEOL structure. Indeed, an increase of the resistance could be the indicator of metal corrosion, which in turn might explain other parameters evolutions (increased leakage current or decreased capacitance for instance). This type of parametric tests is also represented by linear cumulative distributions as shown in figure 1.17.

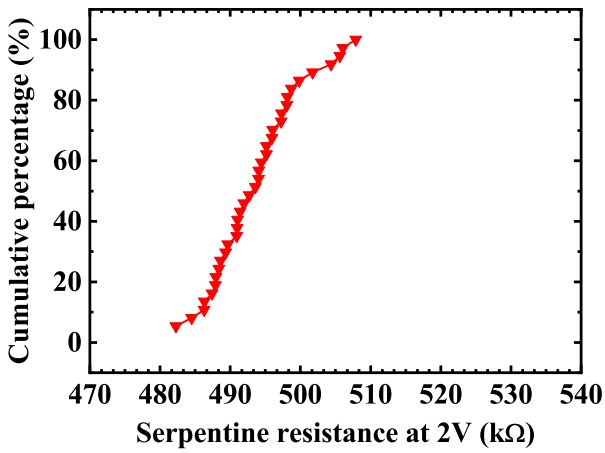
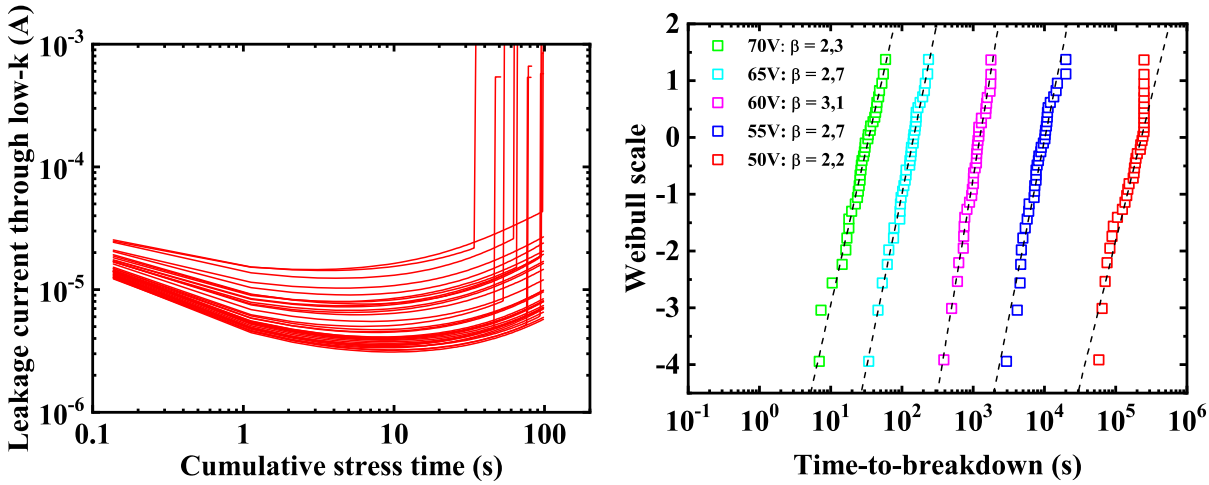


Figure 1.17: Cumulative distribution of serpentine resistance values measured at 2V.

1.4.2.3 Constant Voltage Stress

Apart from parametric tests, a very common methodology is to submit the structure to characterise to a constant voltage and measure the evolution of the leakage current over time, most of the time until breakdown occurs, indicated by a sudden and important leakage current increase. This type of measurement method is purposely called Constant Voltage Stress (CVS). Several primary parameters can be extracted from such measurements: initial leakage current, leakage current minimum, leakage current at breakdown, and obviously time-to-breakdown. All these parameters allow to compare the structures to spot those that are defective, because having very different time-to-breakdown for instance. That is one of the reasons why the time-to-breakdown is usually represented with the help of Weibull plot as it specially exhibits extreme values which are particularly important for reliability improvement or control of the interconnect structures. Hence, this methodology is extensively used for low-κ interconnect structures reliability assessment in the industry. Figure 1.18.a plots an example of the curves obtained by discrete leakage current measurements during CVS at 65V while the figure 1.18.b shows a Weibull representation of the extracted time-to-breakdown for different biases. The Weibull plot regression called the β shape factor is often used to evaluate the spread of values. High β values, corresponding to small spreads are usually expected.



(a) Example of a leakage current measurement during CVS test at 65V.

(b) Weibull distribution of time-to-breakdowns extracted from CVS tests at different voltages.

Figure 1.18: CVS test and Weibull representation

1.4.2.4 Constant Current Stress

This type of characterisation method is very similar to the CVS technique but in this method, the current is forced while the evolution of the resulting voltage is monitored which is why it is called Constant Current Stress (CCS). As the current is constant, the breakdown of the tested structure is indicated by a sudden and important voltage drop. Similarly to CVS, different parameters can be extracted: initial and maximum voltages, variation direction during stress, and obviously time-to-breakdown for instance. The voltage evolution during CCS test and associated time-to-breakdown Weibull distributions are shown in figure 1.19.

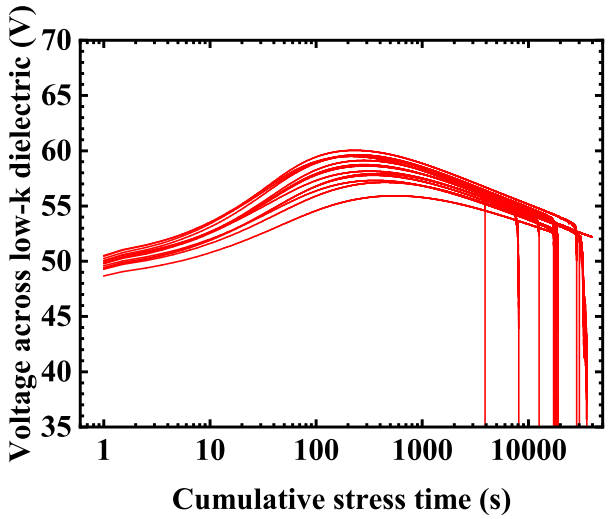


Figure 1.19: Voltage measurement during CCS tests at 1μA on reference structures.

As one can note, Weibull time-to-breakdown distributions can be extracted from CCS tests as well, meaning such distributions does not allow to distinguish the test methodology used, which is consistent with the fact that CVS and CCS are two different methodologies to evaluate the same physical phenomenon: evolution of the electrical properties under the influence of intense electron flow and electrical field, through the dielectric material [46]. These methodologies have been developed in order to study different dielectrics as some of them are more sensitive to the number of charges crossing while others are more sensitive to the voltage applied [57].

Nonetheless, Weibull distributions alone are not of any use without proper extrapolation at actual chips regime. Indeed, to assess material reliability in an acceptable range of time, despite the fact that functionality over several years and sometimes decades must be ensured, reliability tests are performed at much higher electrical fields and currents than what is actually used in chips. To this extent, appropriate extrapolation models are required.

1.4.3 Lifetime estimation: extrapolation models

Extrapolation models are extensively used in the semiconductor industry for a cohort of materials and devices. An appropriate extrapolation model is crucial in order to avoid two important pitfalls. The first one is to be too conservative leading to an actual lifetime much higher at chips operating conditions than estimated by the model. Consequences of such inability to evaluate the chip lifetime might implies to use more robust BEOL and hence, non-necessary R&D about materials and structures, hence unnecessary costs. The second pitfall that an accurate extrapolation model allows to avoid might seem even worse: chips failure happening earlier than expected, which is not acceptable in a general manner, and is particularly true for critical applications such as automotive or medical. Consequently, companies tend to use the more conservative model as there is little agreement in the scientific community about these extrapolation models. We do not intend to provide exhaustive description of all acceleration models as they are in vast number and every one of them might be the subject of extended discussions. Thus, this section will

mention and provide insights about the three main models discussed in the state-of-the-art for low-κ-based BEOL interconnects, these are the Root-E (R-E) model, the Power Law (PL) model and the Impact Damage (ID) model [58], [59].

1.4.3.1 Root-E model

Historically inherited from silicon dioxide, the Root-E (R-E) model refers to the exponential of the square-root of the applied field dependence of the time-to-breakdown originating from the assumed conduction mechanism, either Schottky thermionic Emission (SE) or Poole-Frenkel trap-assisted tunnelling (PF). In fact, several forms of R-E models have been proposed [60], [61] where the time-to-failure TTF is expressed as:

$$TTF = A_{R-E}E^n exp\left(\frac{-\beta\sqrt{E}+\phi}{k_BT}\right) \tag{1.11}$$

Where E is the applied electrical field, k_B is the Boltzmann constant, T is the temperature, ϕ the barrier height and A_{R-E}, n and β are parameters which value depends on the assumed conduction mechanism though the low-κ SiOC:H dielectric [62]. From this generic formulation, several physical root-causes have been proposed, leading to slight changes in aforementioned A_{R-E}, n, β and ϕ parameters.

1.4.3.2 Power Law model

Originally, the Power Law (PL) model has not been proposed for SiOC:H low-κ dielectrics but gate dielectrics [63]. Only recently, this model drew attention for SiOC:H lifetime extrapolation model thanks to strong correlation with characterisation data [59]. According to the PL model, the time-to-failure TTF is mathematically expressed by:

$$TTF = A_{PL}E^{-n} \tag{1.12}$$

With A_{PL} a pre-exponential constant and n the power exponent applied on the electrical field E [58], [64]. The physical root-cause proposed for this model relies on hydrogen release and its interactions with weak bonds present in the SiOC:H dielectric material, leading to defect generation [59].

1.4.3.3 Impact Damage model

Based on a similar hypothesis, the Impact Damage (ID) model proposed by Lloyd and co-workers [65] relies on energetic considerations of the injected electrons. Indeed, as explained by Lloyd in [66] the incoming electron having sufficient energy bumping in hydrogen may break weak bonds, generating carbon dangling bonds as a result. This model is expressed by:

$$TTF = A_{ID}exp\left(\frac{\alpha}{E} - \gamma_{IE}\right) \tag{1.13}$$

Where A_{ID} is a pre-exponential constant, α a characteristic dielectric property defined in the model [66] and γ_{IE} the Poole-Frenkel conduction parameter.

1.4.3.4 Comparison and remarks

These main models are difficult to compare one another, as they all seem to agree with high electrical field characterisation data, which are the most conveniently generated *i.e.* on a reasonable time scale. However, as shown in figure 1.20, they diverge at low electrical fields, which is why the choice of the most accurate model is crystallizing the debates in the scientific community. While the R-E model is the most conservative of the three, thus the less optimistic, the ID model is the least conservative.

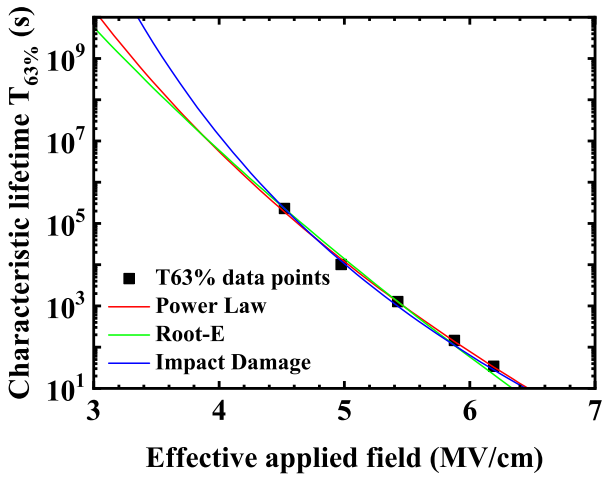


Figure 1.20: Different lifetime extrapolation models fitted to experimental data points from figure 1.18.b.

However, recent characterisation data suggest that the R-E model does not fit satisfactorily at lower electrical fields, increasing the interest for PL and ID models that are still in very good agreement at these electrical fields [58], [59]. Indeed, in practice it is very difficult to discriminate the ID and PL models from actual characterisation data as they predict very close time-to-failure for a wide range of electrical field.

It is worth noting that resort to lifetime extrapolation models in general still involves an inherent bias considering the fact that high electrical fields reliability data might be the consequence of different failure mechanisms, than those occurring at low electrical fields, *i.e.* at the chip's electrical regime. Consequently, blind extrapolation from high-field data is risky, and that is why, a good knowledge of the characterised material together with physical pictures associated with these models are crucial.

1.5 Moisture and interconnects performances

Models described in the previous section (1.4.3) are particularly useful in the case of as-processed SiOC:H low-κ dielectrics but do not take into account the influence of external pollutants in the material. One of these pollutants is extensively reported in the literature: moisture [67], [68], [53], [56], [69]. Indeed, moisture is known to affect a wide range of devices in chips, accountable for possible chips malfunction or early failure. As they are hardly predicted, it is necessary to prevent such harmful pollutants to penetrate the chip.

1.5.1 Moisture ingress modalities

As the detrimental effect of moisture is well known for a range of devices and materials, in order to prevent such contamination it is necessary to detail how moisture can penetrate the chip and how this is affected by the fabrication process. Then, critical fabrication steps and topological features are pointed out to mitigate moisture ingress in the chip.

1.5.1.1 Process-induced moisture ingress

Because SiOC:H low-κ dielectrics are particularly sensitive to moisture, contact with water is prohibited. Still, water and wet cleans are absolutely required for the fabrication process, hence SiOC:H dielectrics interfaces must remain protected against it throughout the whole fabrication process. Nonetheless, certain process steps involve an inherent risk to submit the low-κ material to moisture, which is the case of Chemical-Mechanical Planarisation (CMP) as described in section 2.2.6 for instance. Therefore, deposition thickness and CMP depth must be well mastered to avoid process-induced moisture pollution occurrence. Alternatively, mechanically traumatising steps such as wafer dicing and wire bonding can potentially provoke unwanted moisture ingress if the chip structure is mechanically damaged (cracks or delamination for instance). This aspect is thoroughly detailed in section 3.5.

1.5.1.2 Vertical diffusion

Once the wafer fabrication, described in chapter 2, is finished, wafers are supposed to be protected against moisture and other pollutants penetration from the top of the BEOL stack by passivation layers, described in section 2.3. Previous experiences have shown that integrity of these layers is crucial in order to ensure moisture does not penetrate the chip. This must be the case at every location of the die surface, including patterns and around pad structures, because a few nanometres large pathway is sufficient to allow moisture ingress. If this requirement is not fulfilled, the chip tightness to external pollutant is uncertain. It is worth noting that although preventing moisture ingress might seem straight forward for individual chip, it must also be ensured for every chip on the wafer surface, which adds to the complexity of preventing vertical moisture diffusion because of process variability (see section 2.6 for more details).

1.5.1.3 Wafer-level lateral diffusion

Unlike vertical diffusion, wafer-level lateral moisture diffusion is inherent to the BEOL architecture. Indeed, in order to avoid inter-level short circuit, important leakage current, or high capacitance, a significant distance must be kept between lines places on top of one another. Consequently, the dielectric thickness between the top of one metallic line and the bottom of the one above leaves an important diffusion path. Hence, it is decisive to consider this type of diffusion mechanism as without any countermeasure, moisture is susceptible to find its path to contaminate the SiOC:H material across the whole wafer.

1.5.2 Moisture ingress countermeasures

In the light of the moisture ingress modalities described in the previous section (1.5.1), it has been necessary to develop different strategies to contain these three modalities of moisture contamination. While the methodology to contain process-induced moisture contamination is straightforward: never let the SiOC:H dielectric material enter in contact with a wet chemistry or cleaning steps by protecting its surface with another material [70], vertical and wafer-level lateral moisture diffusion cannot be prevented in the same manner. As a consequence, vertical moisture diffusion blockage can be achieved by a strongly hydrophobic moisture diffusion barrier deposited on the whole surface of the chip. The chosen material must be compatible with the BEOL fabrication process constraints, such as keep the process temperature below 400°C. A material already used in the semiconductor industry is perfectly meeting these requirements: silicon nitride, SiN. Consequently, several SiN films are deposited at different levels to prevent moisture to diffuse from one level to another [71]. Concerning the solution to avoid lateral moisture diffusion, it is conceptually simple in the end: build metallic wall, that is moisture-tight, around the whole chip. Historically, a structure alike exists already around chips with silicon oxide-based BEOL to prevent cracks diffusion from the chip's edges that can occur during sawing [26]. Therefore, for low-κ-based BEOL, this mechanically protective structure, called seal-ring, is improved to be also perfectly tight to moisture thereby solving the lateral moisture diffusion issue [72].

Despite these countermeasures to moistures ingress, sporadic moisture-related issue may occur during technology or new product development for instance. Accordingly, these countermeasures cannot be taken as foolproof solutions, and methods are needed to evaluate their efficiency to block moisture.

1.5.3 Interconnect performance degradation indicators

As moisture affects an important range of devices in chips, numerous parameters could be used to spot eventual moisture contamination. However, the topic of our study lays the stress on the effect of moisture in SiOC:H low-κ-based BEOL. In consequence, this section will not discuss the moisture influence on Front-End-Of-Line (FEOL) devices, despite the fact that it is regularly discussed in the literature [73], [74], [75], [76], [77].

1.5.3.1 Leakage current

Leakage current though SiOC:H is an indicator of the material quality as insulator, as its role in the BEOL is to prevent charge exchange between two adjacent lines. Consequently, an increase of the leakage current between two adjacent metallic lines, hence through SiOC:H dielectric material can be attributed to material defects or pollutants facilitating the conduction of charges between the two lines. Important leakage current increase over time is often attributed to moisture pollution. Figure 1.21 is an example of leakage current increase observed on BEOL test structures (details in section 3.3). Leakage current measurements offer the advantages to be non-destructive and compatible with fast monitoring at Parametric Test (PT). Figure 1.21 underlines the fact that the leakage current of structures without protection against moisture ingress increases strongly. However, as one can note, even though the increase is significant for an important number of

structures, the whole cumulative distribution is not shifted to the higher values and some remain low over time. Consequently, it is difficult to detect moisture ingress on individual structures with leakage current measurements.

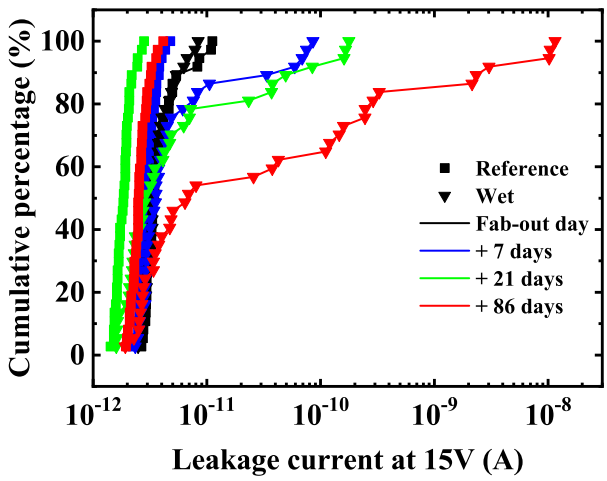


Figure 1.21: Evolution of leakage current at 15V.

1.5.3.2 Capacitance

As a consequence, other methods can be used to detect an evolution of the SiOC:H material electrical properties. Relevance of capacitance measurements is a direct consequence of the dielectric material properties, especially polarizability as presented in section 1.3. Therefore, a capacitance evolution provides immediate information on the low-κ material evolution as the only parameter susceptible to vary significantly over time is its polarizability.

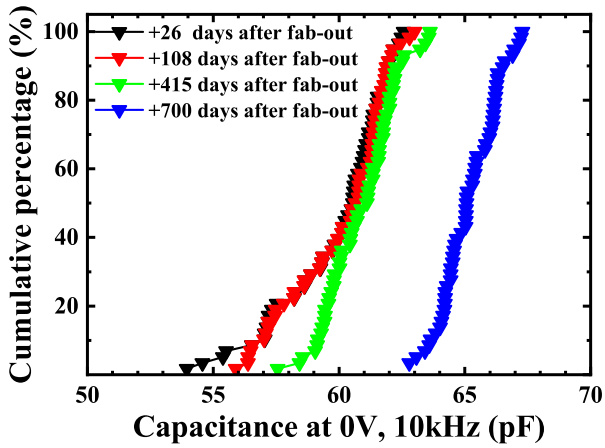
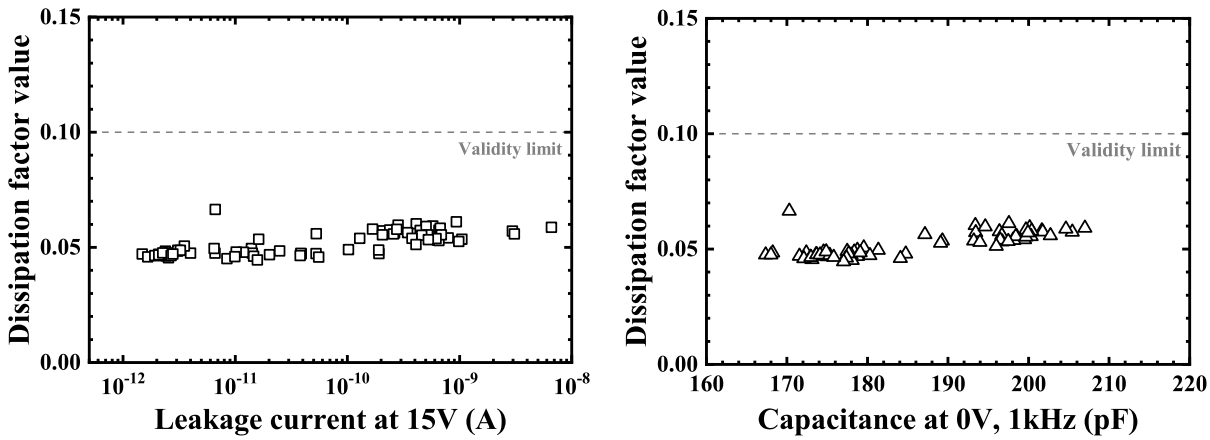


Figure 1.22: Capacitance evolution over time of wet structures.

As capacitance measurement is a complex impedance measurement (see section 1.3.2.3 for model detail), it cannot be excluded that the capacitance increase is a consequence of a measurement artefact induced by a leakage current increase. To put aside the possibility, Monsieur has shown that the dissipation factor, D, expressed as $D = \frac{G}{C.2\pi.f}$ with G the

conductance, C the measured capacitance, and f the frequency of the measurement [78], can be used as a quality assessment of the capacitance measurement. More specifically, he states that capacitance measurements are reliable as long as D remains lower than 0.1 [78]. This check has been performed on structures having leakage current spanning over three decades, and no significant change of the dissipation factor is seen (figure 1.23). Since its values remain far from the 0.1 limit, it tends to confirm that the capacitance evolution observed is not the consequence of measurement artefacts.



(a) Dissipation factor as a function of leakage current at 15V.

(b) Dissipation factor as a function of capacitance value measured at 0v, 1kHz.

Figure 1.23: Dissipation factor correlations with capacitance and leakage current.

Similarly to leakage current, capacitance measurements are non destructive. But, they would be considered as a better alternative as they do not involve an electrical stress. However, as seen on figure 1.22, the whole capacitance distribution does not shift as some values remain low over time. Consequently, capacitance measurement is not relevant to detect moisture ingress.

1.5.3.3 Time-Dependent Dielectric Breakdown

To the contrary, Time-Dependent Dielectric Breakdown (TDDB) is a very common destructive measurement. It allows direct assessment of the structure reliability through lifetime extrapolation models (see section 1.4.3 for more details). Moreover, this method is relevant for production needs as it allows to detect potential structural and fabrication-related defects such as low resistivity metallic bridges or massive copper contamination for instance. The figure 1.24 presents the dramatic impact observed on time-to-breakdown of moisturised test structures, referred as wet structures. For comparison, distribution of time-to-breakdown measured on structures without moisture (see chapter 3 for structure details) is plotted from figure 1.18.b. These Weibull plots highlight two main elements, first, breakdown of moisturised structures happened significantly earlier than on reference structures *i.e.*, protected against the effect of moisture. Secondly, the spread is dramatically larger under the influence of moisture.

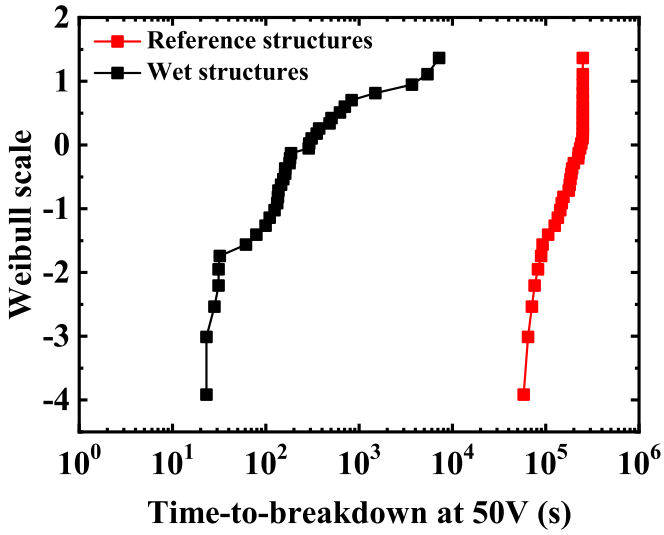
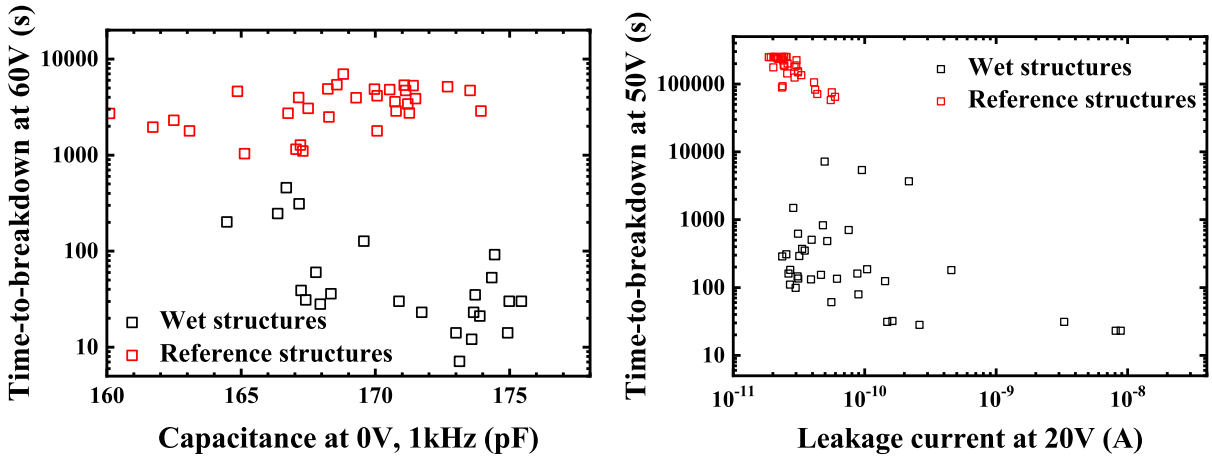


Figure 1.24: Moisture impact on test structure TDDB performance.

However, stressing the structures until breakdown is time consuming because it is usually performed by CVS or CCS (see sections 1.4.2.3 and 1.4.2.4 respectively for more details). Even though equivalent, but faster, methods such as Linear Ramp Voltage Stress (LRVS) or Exponential Ramp Current Stress (ERCS) have been rightfully developed for industrial cost optimisation, this type of methodology requires high voltages for BEOL structures and remains destructive. Consequently, it is interesting to understand how the reliability performance, here Time-Dependent Dielectric Breakdown (TDDB), is related to parametric test leakage current and capacitance values described in previous sections 1.5.3.1 and 1.5.3.2.

1.5.3.4 Correlations

Indeed, a correlation between the TDDB performance and leakage current or capacitance value would allow to easily detect chips prone to early breakdown. With this small set of parameters, two correlation plots can be produced: the time-to-breakdown as a function of the capacitance value measured before stress (figure 1.25.a) and the time-to-breakdown as function of the low electrical field leakage current measured before stress (figure 1.25.b). The former suggests there is no clear correlation between time-to-breakdown and capacitance. For instance, capacitance values of 173-175 pF correspond to times-to-breakdown spanning over a decade. Similarly, leakage current values between 50 and 100 pA correspond to times-to-breakdown spanning over two decades (figure 1.25.b). Nonetheless, it is worth noting that when leakage current is very high (> 1 nano-Ampere), the time-to-breakdown is very low (under 100s). Likewise, no clear correlation can neither be observed between time-to-breakdown and initial, minimum or maximum leakage currents during stress or other indirect parameters such as voltage or leakage current drop during stress for instance.



(a) Time-to-breakdown as a function of capacitance value measured just before stress.

(b) Time-to-breakdown as a function of leakage current measured at 20V just before stress.

Figure 1.25: PT parameters and time-to-breakdown correlation plots.

Despite the fact that leakage current and capacitance increase indicates clearly the presence of moisture on a wafer, only one parameter seems to be directly correlated with moisture contamination: the time-to-breakdown. This makes moisture detection and study particularly problematic as evaluation of moisture contamination on individual test structures or chips requires its destruction.

1.6 Conclusion

As we have seen in this first chapter, moisture consequences are dramatic at the circuit level because of interconnect performances and reliability degradations, hence it is crucial to be able to detect chips prone to moisture uptake as soon as possible along the fabrication process. But moisture degradation is not straightforward to spot at early stages. For this, it is important to understand the action of moisture at the chemical level as well as its repercussions in terms of electrical behaviour. Hence, chemical analysis or electrical analysis alone are not sufficient, that is why the present work intends to explore the effects of moisture on SiOC:H low-κ dielectric from these two different perspectives: electrical and chemical. Electrical and chemical behaviours are narrowly linked but are sensitive to different aspects of the material properties which make them complementary, even though moisture-related electrical performance degradation understanding is the prime reason for this work. In order to gather these two types of information, physical (detailed in chapter 3) and electrical (detailed in chapter 4) characterisations will be carried-out.

Chapter 2

Integration process constraints and SiOC:H chemical structure

"It is the weight, not the numbers of experiments that is to be regarded."

Isaac Newton

2.1 Introduction

Over the years, the introduction of new materials for performance improvements, as mentioned in section 1.2, and scaling brought increasing complexity to the process flow of modern microelectronic chips. Because of the strategies used to reduce the interconnect dielectric constant (see section 1.3.3), SiOC:H dielectrics, which replaced traditional SiO_2, presents peculiar mechanical properties such as weak hardness and Young's modulus and an important sensibility to chemical pollutants in general and to moisture in particular. Thus, definition of the integration process as well as the chemical structure of the SiOC:H material are of prime importance in order to study moisture-related degradation mechanisms in the interconnect. Consequently, in this chapter, the state-of-the-art manufacturing process of the interconnect, called dual-damascene, is detailed, together with an overview of the process steps generating moisture ingress and variability that affect the SiOC:H low-κ dielectric properties. Then, the chemical structure of this dielectric is studied through different physical characterisation methods.

2.2 The dual-damascene process

The inability to realise plasma-assisted etch of copper [79], unlike previously done with aluminium, induced a drastic evolution of the metallic lines patterning which has led to the development of the dual-damascene process used for copper integration. Such process differs widely from traditional metal inlaying because the dielectric stack is etched instead of the metal and then, the resulting free space is filled by metal to constitute the

chips metallic lines. Over the past decades, copper/low-κ dielectrics BEOL became an industrial standard, so did the dual-damascene process.

2.2.1 Pre-Metal Dielectric

After the fabrication of the chip Front-End-Of-Line (FEOL), i.e. transistors, memory cells etc., multiple layers are deposited on top of the whole chip in order to insulate the FEOL from the BEOL. This stack of dielectric materials is called the Pre-Metal Dielectric (PMD) and is composed of undoped, fluorine-doped and phosphorous-doped Silicate Glasses respectively referred as USG, FSG and PSG. Apart from eventual FEOL contamination issues, the PMD is needed to flatten the chip surface topology due, among others, to the difference of height between logic, high voltage and memory areas [80]. Following these silicate glasses, a TetraEthyle OrthoSilicate (TEOS) film finishes the PMD, on top of which the first layer of SiOC:H low-κ is deposited.

2.2.2 SiOC:H deposition

As the use of low-κ dielectrics is one of the main reasons for the emergence of the dual-damascene process, the control of the SiOC:H deposition process is of primary importance in order to achieve low dielectric constant. Similarly to silicon dioxide, SiOC:H low-κ dielectric is deposited with Plasma-Enhanced Chemical Vapour Deposition (PECVD) [81] but the precursor gas is TetraMethylSilane (TMS) which has the particularity to contain at the same time, high carbon and hydrogen contents to be incorporated in the produced film [82]. In our fabrication process, the TMS precursor gas is deposited under low-pressure conditions (3 to 5 Torr) at a temperature of 350°C under oxygen and slight helium gas flow [83], about 500 and 300 Standard Cubic Centimetres per Minute (SSCM) respectively. The stoichiometry of these gases must be adjusted in order to achieve a SiOC:H material with a low dielectric constant but also acceptable mechanical properties to allow the complete integration detailed in the following. In order to protect the SiOC:H dielectric material from unwanted damages which could be detrimental to its dielectric constant, a thin TEOS film is deposited *in situ* on top of it. It prevents the SiOC:H to be exposed to air and all pollutants it might comport, despite the clean room environment. It must be noted that the first level of the interconnect is specific. Indeed, the SiOC:H is deposited on top of the TEOS film of the PMD, which, as it will be detailed in section 2.2.8, changes from upper interconnect levels. Secondly, etching the first level of the interconnect is notably the most challenging etch step of the BEOL fabrication as it impacts drastically the device reliability [84] and presents the smallest spacing, as it must allow to connect analytic devices very close from each other through the thick PMD, inducing high aspect ratios [85].

2.2.3 SiOC:H etch

Once the dielectric stack is deposited as detailed in section 2.2.2, the etch step allows to create trenches that will ultimately be filled by metallic lines. Etch is often referred as one of the most challenging steps in the manufacturing process because it requires high aspect ratio between the top and the bottom (around 2 and higher) [42] of the etched

region and alignment precision. Two types of masking strategies exist: either a thin TiN layer, called Hard Mask (HM), patterned by a dedicated etch step or a photoresist resin which is patterned by insolation, also called photo-lithography. As the remaining mask (HM or resin) protects the dielectric stack of the etching chemicals, any variation in the hard mask etch or photoresist resin insolation steps would produce patterning variations. Moreover, from one level to another, every mask must be perfectly aligned to guarantee inter-level metallic lines continuity. As the HM offers better regularity for narrow patterns but involves more constraints than the photoresist resin, such as post etch cleaning, the best approach is to combine these two masking strategies by using HM for lines definition followed by photoresist resin for via definition. As picturised by figure 2.1, a HM is deposited and etched where lines will take place, on top of which, the photoresist is deposited. Once the photoresist resin is removed at the via location by lithography, the etching process is performed in two steps. First, the via is partially etched, then all the remaining masking photoresist is removed in situ to allow to etch the deep part of the via and the line using the HM to define the pattern. It must be noted that the chemistry used during via and line etch steps can be different, modifying the anisotropic properties of the corrosive gas mixture, in order to improve the via shape for instance. Also, the Bottom Anti-Reflecting Coating (BARC) helps improve the etched area sidewall roughness [86].

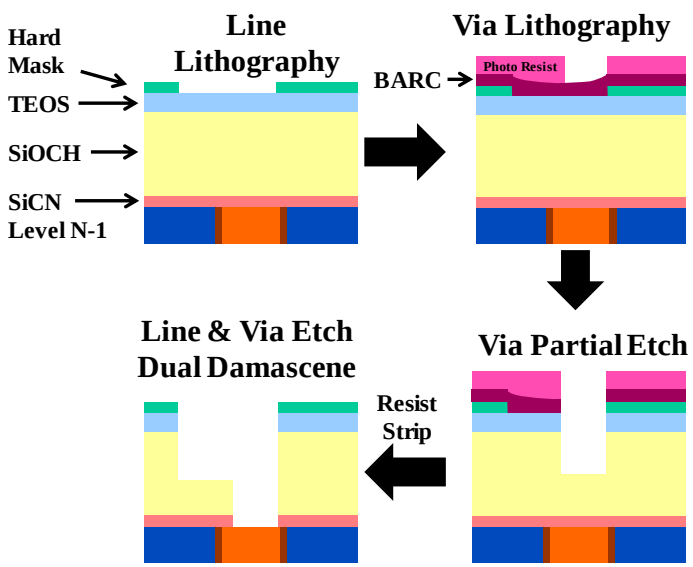


Figure 2.1: Etching process steps in the dual-damascene process flow.

2.2.4 Copper diffusion barrier deposition (Ta/TaN)

Once line and via etch is completed, another important constraint induced by the use of copper instead of aluminium, is the need of a copper diffusion barrier to prevent copper atoms to diffuse into the SiOC:H low-κ dielectric and potentially assist electron conduction from one line to an adjacent one [87]. To prevent such harmful effect, a few nanometres thick tantalum nitride (TaN) film is deposited. In order to increase the interfacial strength and reduce the line resistance, this barrier is made a bi-layer with the addition of a pure tantalum film [88]. A trade-off must be found between each layer thickness and composition and their efficiency as a copper diffusion barrier. Indeed, Kim

et Al. have shown that the higher the nitride content, the better the copper barrier efficiency [89]. However, TaN having a sheet resistance more than thrice of the pure Ta, it collides with the need for low line resistance [88].

2.2.5 Copper deposition and copper grains

On the Ta/TaN copper diffusion barrier, copper seeds are deposited by Self Ionised Plasma (SIP). It consists in a thin nucleation layer from which the copper grains grow [90]. Once the thin copper nucleation film is deposited, the wafer is submitted to a plating electrochemical bath under low pressure. The gas mixture, often composed of ionised copper and argon plasma, is submitted to a strong DC power and a smaller AC bias, usually of several kilowatts and hundreds of watts respectively. This deposition method is called SIP EnCoRe for Self Ionised Plasma Enhanced Coverage Resputtering and is mainly provided by Applied Materials [91]. It is the result of important engineering process developments. It also relies on extensive study of copper crystallographic parameters such as grain size and orientation that concluded that grain boundaries are detrimental for copper line resistance [92]. Especially, for technology nodes below 40nm, a line resistivity increase is observed and is attributed to smaller copper grains, hence more grain boundaries and higher copper residual constraint [92]. Consequently, a conformal copper seed nucleation layer deposition together with copper electroplating at controlled temperature are required to produce low resistance copper lines [92].

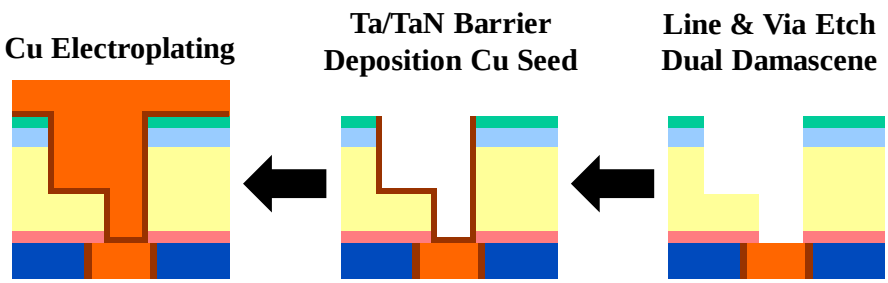


Figure 2.2: Ta/TaN copper diffusion barrier deposition, copper seed, and copper electroplating in the dual-damascene process flow.

2.2.6 Chemical Mechanical Polishing (CMP)

At the end of the copper electroplating, the wafer surface is coated with copper, hence it is necessary to remove the copper where it is not needed i.e. outside the metallic lines. Consequently, a rotating polishing pad is used with an abrasive and corrosive chemical slurry to remove the copper on the wafer surface until a targeted depth is reached which often corresponds to end the CMP in the TEOS on top of the SiOC:H low-κ dielectric material. This step is also called planarization as it allows to remove the topology of the wafer surface [79]. Moreover, as copper lines roughness can impact the interconnect TDDB performance [93], good depth precision is required to ensure no unwanted copper remains and to guarantee the integrity of the materials underneath the electroplated copper layer between the lines.

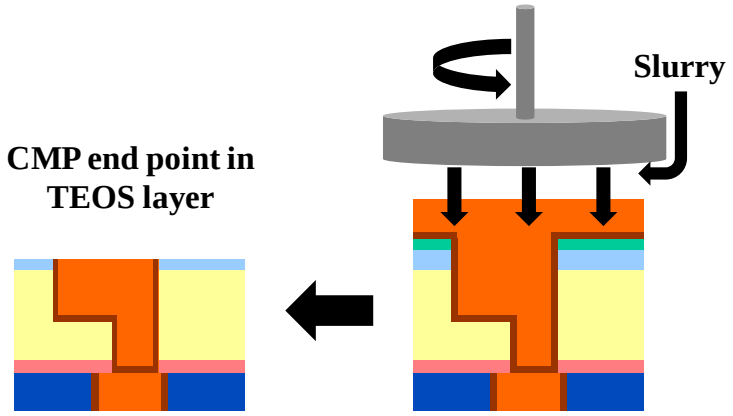


Figure 2.3: Chemical Mechanical Polishing process step in the dual-damascene process flow.

2.2.7 Wet and dry cleans

As suggested in section 2.2.3, numerous cleaning steps are needed along the fabrication, such as HM residue removal for instance. Indeed, it is necessary to scrub the wafer front-end surface in order to remove all sorts of residues or pollutants that could have an impact on subsequent process steps, hence on chips quality and performances [94]. However, to prevent unwanted material surface attack or interface degradation [94],[95], cleaning steps must be highly selective. For instance, chemistry used for photoresist resin removal must not degrade the film on top of which the photoresist resin is deposited [96]. Different contamination types can occur, each one with specific root-causes and chemical compounds involved, consequently different types of cleaning are used throughout the BEOL process: dry cleanings use pure plasma or plasma-assisted chemical reactions while liquid chemical based cleanings, referred as wet cleans, use a range of acids, and water spraying. The latter can have an important impact considering our study of moisture-related degradation mechanisms, in particular after the copper CMP step [70]. Indeed, as shown in figure 2.4, a poorly controlled CMP will expose the SiOC:H dielectric surface, because of complete TEOS consumption, and results in water jets pulverised directly on the SiOC:H, dramatically impacting it as we will discuss in section 2.4.

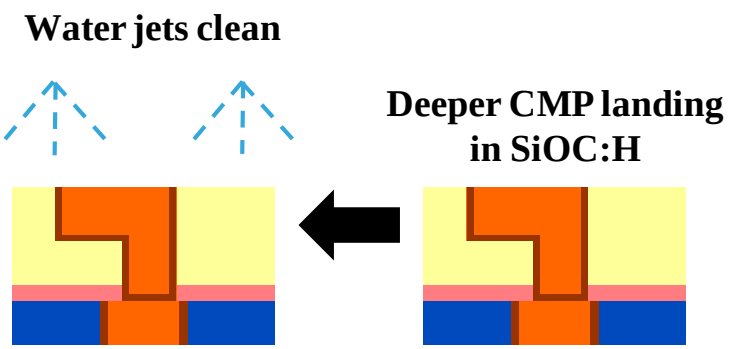


Figure 2.4: Potential consequence of poorly controlled CMP followed by high-pressure water jet during wet cleaning.

2.2.8 SiCN copper encapsulation and line anneal

On top of every copper metallic line, a SiCN film is deposited. it is often referred as the line encapsulation or capping. It prevents copper to diffuse by the top of the line, at the TEOS interface, where there is no Ta/TaN diffusion barrier (figure 2.3). Indeed, SiCN line capping greatly improves the TDDB performance of the chips interconnect [97]. Following the deposition of this SiCN capping film, a 30 minutes copper line anneal at 400°C is performed in order to reduce the copper line resistance [98]. It must be noted that this anneal is carried out at every metallisation level, hence previous levels undergo a cumulative thermal budget.

2.3 Passivation, encapsulation and tightness

The manufacturing clean room has a controlled atmosphere where the relative humidity target is 40 percent. In this manner, moisture content of the wafers environment is controlled all along the manufacturing journey. Once the fabrication of the chips is almost completed, they must be encapsulated in order to block pollution from the outside world. However, it is obvious that chips electrical connection terminals, called pads, are needed thus, draw particular attention as they must fulfil their purpose without inducing weaknesses in the chip tightness. Therefore, materials and processes used as well as the wafer topology, especially around the pads, must be tight to all sort of pollutants contained in the air, among which moisture. This ensemble passivation, encapsulation and pad is also referred as the Far BEOL and its primary goal is to protect the chip and allow electrical connectivity.

2.3.1 Required properties of materials used in the far BEOL

Consequently, materials used in the Far BEOL are chosen for their specific properties allowing to create a stack able to block different pollutants and ensure that the top of the interconnect structure is perfectly tight [72]. Additionally, these last interconnects levels are thicker than the first ones, hence they can provide a good manner of improving the chip mechanical performances, notably to counterbalance the SiOC:H low-κ dielectrics poor mechanical properties [25],[99]. This aspect must be considered to optimise subsequent process steps yields such as wafer dicing and wire bonding which induce important mechanical stresses in the chips [27].

2.3.2 Encapsulation

As it is suggested by its name, the purpose of this layer, composed of Undoped Silicon Glass (USG), often mistakenly called TetraEthyle OrthoSilicate (TEOS) in the semiconductor industry after the precursor used to deposit this silicon dioxide, is to protect the top of the interconnect stack from external pollutants. The precursor gas (TEOS) is injected in a low-pressure chamber while the wafer surface is heated. The thick SiO_2 deposited layer is the by-product of a complex pyrolytic chemical reaction occurring when TEOS molecules are heated by the wafer surface, whereas ethanol is degassed [100].

2.3.3 External moisture tightness

As stated in sections 1.5.1.2, 1.5.2, and 2.3.1, tightness to external pollutants must be ensured by the Far BEOL. This is particularly true for moisture as it is known to diffuse easily in low-κ dielectrics [56],[101],[68]. Consequently, a very modest opening in the passivation layers put in danger the chip as moisture can then diffuse through low-κ layers across the whole chip. As represented by figure 2.5, the encapsulation film is deposited on top of the final copper metallisation level. Then, openings until the upper copper metallisation level are etched at the pads location, followed by deposition of a thin Ta/TaN bi-layer, similar to the copper diffusion barrier (see section 2.2.4). Aluminium is still used in copper interconnects as last metallic level to connect to the outside world thanks to its stability to corrosion. Indeed, aluminium experiences a self-limiting surface oxidation when exposed to ambient atmosphere, making it very resistant to corrosion [102]. In fact, slightly doped aluminium is preferred, Al-Cu for instance, thanks to better electromigration performance [103]. The Al-Cu alloy (aluminium with 0.5 percent copper) deposition is usually performed by Plasma Vapour Deposition (PVD). Then, the aluminium film undergoes mask photo-lithography (similarly to dielectrics masking described in figure 2.1). Finally, it is etched by a mixture of phosphoric and nitric acids chemistry. A final nitride thick film is deposited on top of it and etched where aluminium must be accessible for electrical connection purpose, i.e. over pads. All, these steps must be perfectly controlled so that every final aluminium pattern in the chip does not induce diffusion paths. This requires very standardised design and fabrication of the chip final aluminium routing.

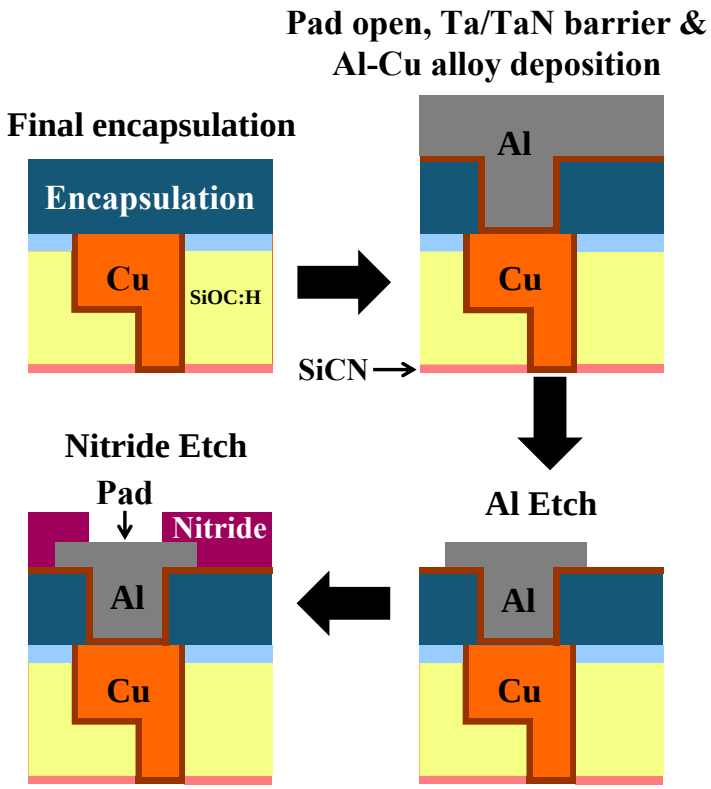


Figure 2.5: Schematic representation of the pad fabrication after the encapsulation step.

2.4 Process variability and SiOC:H specificity

Along the manufacturing process, an important number of operations is performed on each wafer in order to obtain the chips. Thereby, it requires the use of numerous equipment tools and associated handling. Obviously, several copies of every equipment are used to improve the clean room productivity and flexibility which induces machine-to-machine variability. Moreover, as clean room facilities involve consequent operating costs, its loading must be maximum, this translates into different products, sometimes different technologies, being processed by the same machine applying different recipes. Even though repeatability is at the centre of the process team attention, variability is inevitable and is continuously monitored by inline measurements and inspections.

2.4.1 Generalities

Considering the BEOL, the process variability can be divided in five categories : line-to-line on a chip, chip-to-chip on a photolithographic field, field-to-field on a wafer, wafer-to-wafer in a lot and finally lot-to-lot (figure 2.6) [104].

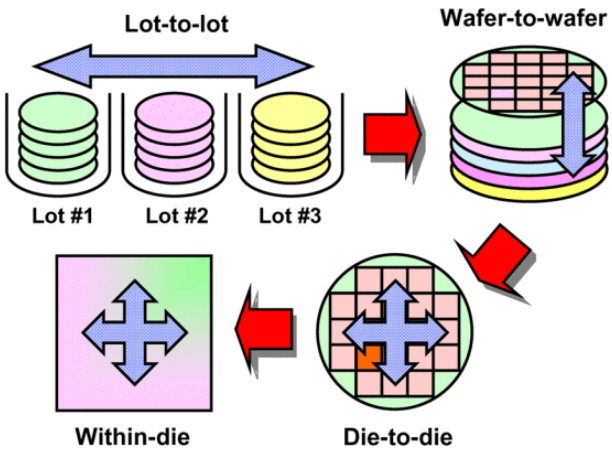


Figure 2.6: Schematic representation of the different types of variability in the semiconductor industry [104].

The line-to-line variability is mainly attributed to metal density variations across the chip area which has an impact on etch and CMP steps for instance. Dummy metal patterns are added to mitigate this type of variability [105].

The chip-to-chip variability refers to the difference that exists between the chips of the same photolithographic field, due to the neighbouring of the chip inside the field. Indeed, many elementary characterisation structures are embedded between chips for inline metrology, technology monitoring and screening needs for example, hence, each chip neighbouring is not strictly identical.

The field-to-field variability, originating, among other causes, from the radio-frequencies assisted deposition sombrero profiles together with mask alignment, are some of the main challenges when increasing the wafer diameter [106],[107],[108]. In fact, the larger the wafer, the more difficult to contain the field-to-field variability, which is one of the reason why 450 mm diameter wafers have not been adopted by the industry and might never be [109].

Wafer-to-wafer variability is the consequence of the effort to enhance the production capability and reduce costs. To this extent, tools possess multiple processing chambers (figure2.7). Processing wafers in different chambers implies a variability as all chambers of one given tool are not strictly identical. Moreover, successive process steps often involve tools with different number of chambers which can make variability even more difficult to trace.

Finally, lot-to-lot variability is mainly due to the redundant tools in the clean room. Indeed, it is very unlikely for two lots to be processed by the same tool at every process step. Furthermore, production tools are cleaned and re-calibrated every certain number of lots processed determined by the tool owner.

Figure 2.7: Example of a multiple chambers tool

Of course, combinations of aforementioned variability types occur along the manufacturing, which reduce inline measurements tolerance even further. Moreover, as technology nodes scale, it is clear that variability containment becomes a key element of technology and process development [104]. It is accountable for a non-negligible part of the manufacturing costs as it requires extensive in-line measurements, statistical analysis and constant monitoring as pointed out by Capasso et al. [110]. Indeed, variability mitigation methods include equipment regular qualification routines and preventive maintenance as well as an important number of in-line metrology steps such as Scanning Electron Microscopy (SEM), Critical Dimension (CD) inspections after insolation and etch steps, and thickness and refractive index measurements by ellipsometry after deposition steps for instance. Thus, variability is continuously monitored along the manufacturing process and out of specifications wafers are destroyed before the end of the fabrication or reprocessed if possible. In spite of this, variability remains an inescapable aspect of manufacturing which must be dealt with from device layout to memory programming algorithm development and final product specification. Error Correction Codes (ECC) are a mean to overcome cell-to-cell variability in memory arrays, crucial for 3D Flash NAND technology for instance [111].

2.4.2 Process steps generating SiOC:H variability

As seen in the section 2.2, every interconnect level is affected by an important number of process steps, involving various types of variability (2.4.1). Several of them directly impact the SiOC:H material properties. Intuitively, the deposition step of the SiOC:H by

PECVD is the first process step to generate variability because of the deposition thickness profile [106] and the slight change of gas stoichiometry from one chamber to another. Indeed, deposited thickness variations contribute to metallic line thickness variability. During the metallic line patterning, the HM must be exposed through masks by ultraviolet light, of 193 nm wavelength in our case. Mask itself and alignment variability contribute to line and via patterns modifications with respect to the original design. As shown in figure 2.8, HM corner rounding and edges roughness occur despite complex Optical Proximity Correction (OPC) [112]. Then, the etch step of the unmasked regions is another source of variability as the etch rate of plasma-assisted etching chemistry depends on the location on the wafer. As a result, metallic line profiles may be different from one field to another. Furthermore, it is well known that plasma can damage SiOC:H interfaces [113], consequently, any plasma treatment applied on unprotected SiOC:H surfaces contribute to interconnect variability. Finally, another important process step when considering SiOC:H variability is the CMP after the copper electroplating and the following scrub. Indeed, CMP is a mechanically aggressive step, required to remove excessive copper deposit, but accurate depth control is difficult to achieve. Moreover, the polishing speed depends on the location on the wafer [114]. Furthermore, the metal density has also a non-negligible impact on the polishing speed, which tends to be higher in low metal density areas. Such CMP inhomogeneity is an important driver of metallic line thickness variability which is detrimental to line resistance variability [114]. This process-induced variability is an important aspect to consider as our study will be necessary based on similar structures comparison. Hence, it is important to understand how, and to what extent, variability might have an influence on our results and thus, countermeasures similar to actual chips production are used along the manufacturing process of our wafers to keep all types of variability as low as possible (see section 3.3 for more details).

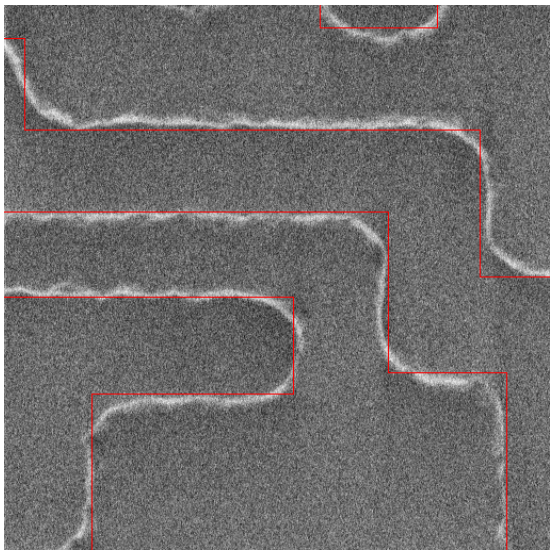


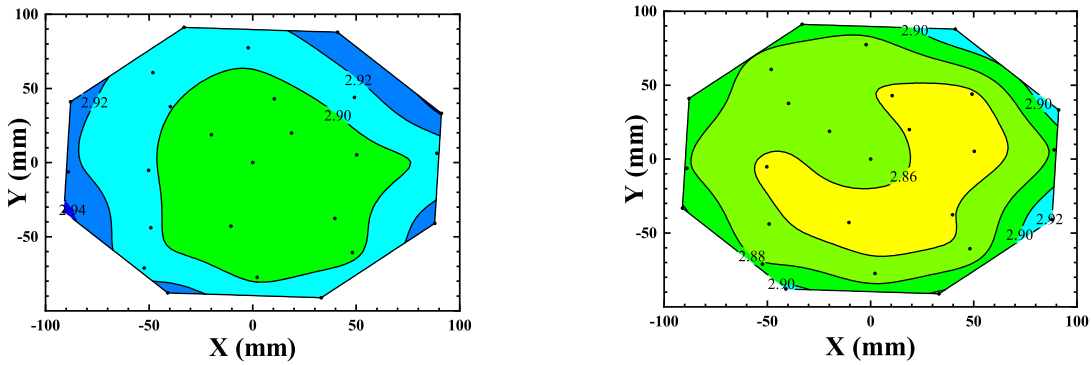
Figure 2.8: SEM view of a first layer of interconnect after HM lithography and superposed drawn metal 1 CAD layer boundaries (red). The area or the future copper lines are freed from HM.

2.5 Physical characterisation of SiOC:H material

In the scope of our study, it is very unlikely that electrical characterisation (detailed in chapter 4) alone can provide answers on the moisture chemical effect on the low-κ dielectric material to explain its peculiar electrical behaviour. Consequently, it is necessary to gather physical information on the unpolluted as well as moisturised SiOC:H material. For this reason, a set of physical analysis must be carried out in an attempt to highlight the physical root-causes of the modification of the electrical behaviour of the interconnect when moisture penetrates the chip. Accordingly, it is necessary to ensure the SiOC:H material used for such characterizations, often deposited on blanket wafers, is as close as possible to the actual SiOC:H material in the interconnect at the end of the chips fabrication. Therefore, the process steps undergone by the SiOC:H material throughout the chips fabrication must be emulated on the SiOC:H blanket material before performing physical characterisations. SiOC:H used in this section is declined in three versions: the Process Of Reference (POR), an oxygen-doped during deposition with +200 SSCM with respect to the POR, referred as High-O recipe and a TetraMethylSilane (TMS) precursor-doped during deposition with +200 SSCM with respect to the POR recipe, referred as High-TMS. These three materials have been chosen for several reasons: to understand the influence of a modification of the deposition stoichiometry on the material chemical structure and on the moisture absorption to determine which type of bonds is more favourable to moisture ingress. As mentioned in section 2.2.8, 30 minutes copper line anneals at 400°C are performed at every BEOL level during the fabrication process and may have an impact on the SiOC:H material structure [115], hence a 1-hour 400°C anneal under nitrogen is performed to mimic the thermal budget of these copper line anneals. When needed, a hydrophobic SiN capping layer is deposited on top of the SiOC:H material to protect it from moisture contamination in the vertical direction.

2.5.1 Surface Photovoltage measurements

The Surface PhotoVoltage (SPV) measurement method consists in the measurement of the voltage on the material surface, in our case SiOC:H, while it is illuminated with an UV light [116]. It is widely used in the industry for mechanical and material development. For us, it is useful to measure the relative dielectric constant, ϵ, of the SiOC:H dielectric film [116]. Colour maps in figure 2.9 underlines the fact that there is a very low dielectric-constant variability across the 200mm-diameter wafer for the POR as-deposited SiOC:H material. Also, it underlines the fact that the anneal has an impact on the material measured values, even though modest. More precisely, non-annealed and annealed SiOC:H (figures 2.9.a and 2.9.b respectively) have 2.91 and 2.88 root mean square dielectric constant respectively and similar standard deviations. These results underline that the as-deposited SiOC:H relative dielectric constant is very stable across the wafer around its reference value of 2.9.



(a) (b)

Figure 2.9: SPV measurement and effect of anneal on the relative dielectric constant of as-deposited POR SiOC:H (2.9.a), and POR SiOC:H treated with a 1-hour anneal at 400°C under nitrogen(2.9.b).

2.5.2 Ellipsometric porosimetry and GISAXS

Ellipsometric porosimetry and Grazing-Incidence Small Angle X-ray Scattering (GISAXS), are two methods for material porosity measurement. They are rather unusual characterisation techniques in the semiconductor industry.

2.5.2.1 Ellipsometric porosimetry principle and SiOC:H results

Between the two techniques, ellipsometric porosimetry can be qualified as the most straightforward as it consists in the gradual injection of toluene vapour in a vacuum chamber where the sample to characterise is placed [117]. During the toluene injection, the sample optical properties are monitored by spectroscopic ellipsometry (SE) as illustrated by figure 2.10.

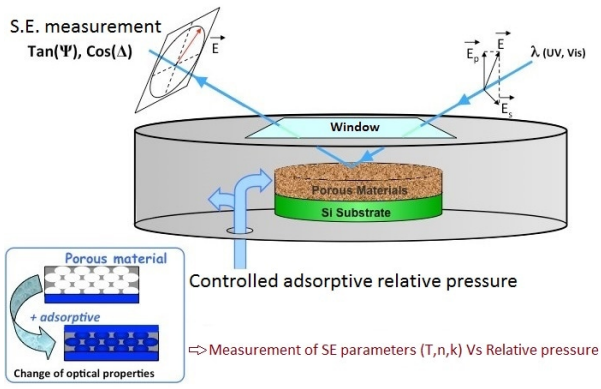
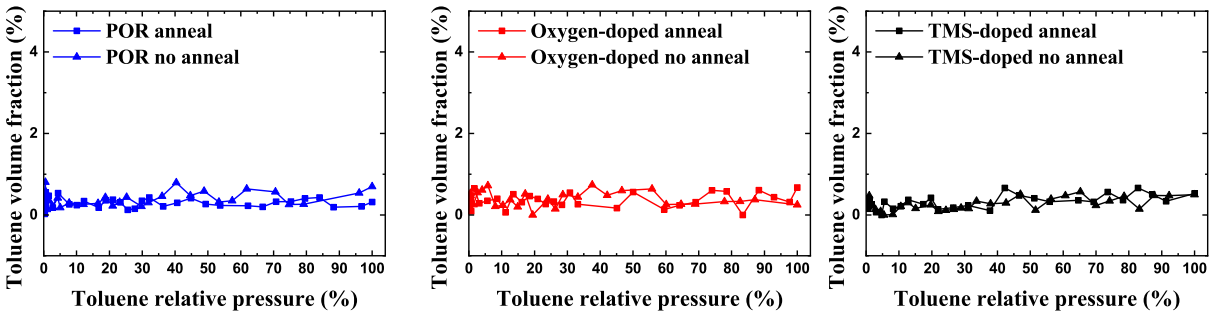


Figure 2.10: Ellipsometric porosimetry working principle [118]. S.E. stands for Standard Ellipsometry.

At the beginning of the experiment, the initial optical index of the SiOC:H material and toluene are known. Then, during the experiment, material optical index variations are measured by the detector. Based on this measure and on optical index models, the gas quantity penetrating the SiOC:H material pore network is derived, hence the pore volume [117]. The experiment has been performed on square samples of uncapped 3x3cm of High-O, High-TMS and POR materials. As the 1h-anneal at 400°C under nitrogen, slightly modifies the material dielectric constant ellipsometric porosimetry measurements have been carried out on samples with and without this anneal in order to put in light an eventual effect of the anneal on the material porosity. As we can clearly see on figure 2.11, the extracted toluene fraction in the SiOC:H samples does not increase as the toluene relative pressure increases in the chamber, whatever the sample. It indicates that no porosity is detected by the ellipsometric porosimetry method as toluene does not penetrate in any of the samples, whatever the material (High-O, High-TMS, or POR) and the thermal treatment (none or 1-hour at 400°C under nitrogen).



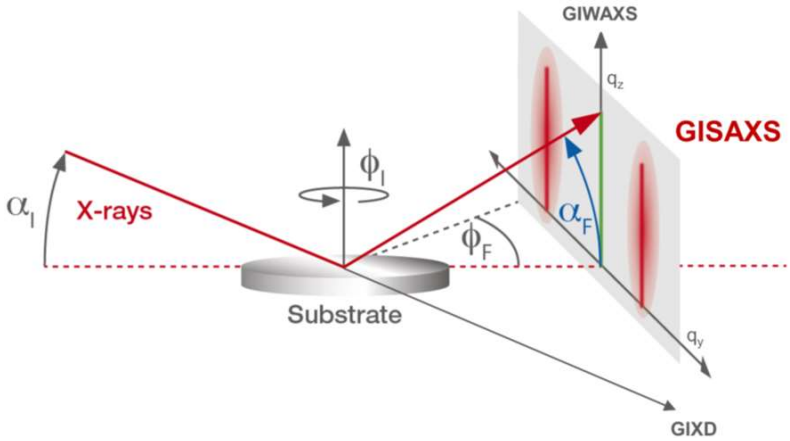
(a) Standard (POR) SiOC:H. (b) High-O SiOC:H. (c) High-TMS SiOC:H.

Figure 2.11: Ellipsometric porosimetry measurements on different uncapped SiOC:H materials.

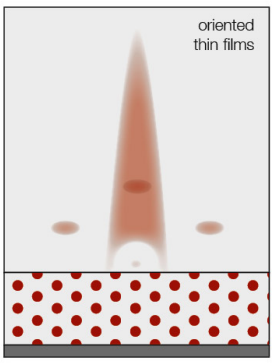
However, we are unable to conclude that there is no porosity at all as this method can only detect connected porosity with pores large enough to let toluene molecules penetrate the hypothetical porous structure. Because, toluene molecules have a size of 0.6 nm while water molecules are 0.17nm [119], moisture could penetrate pores undetected by ellipsometric porosimetry. That is why further analysis is required to allow eventual unconnected or/and smaller than 0.6nm radius porosity detection.

2.5.2.2 GISAXS principle and SiOC:H results

To this extent, the GISAXS characterisation method has been considered. It is a relatively new technique, mostly used to characterise nanostructured materials. It has the particularity to provide an averaged measure on a several microns wide spot surface and allow to retrieve structural organisation information on the material (figure 2.12.b). It is based on the small angle scattering of the incident X-ray beam by the nanostructures present in the sample [120].



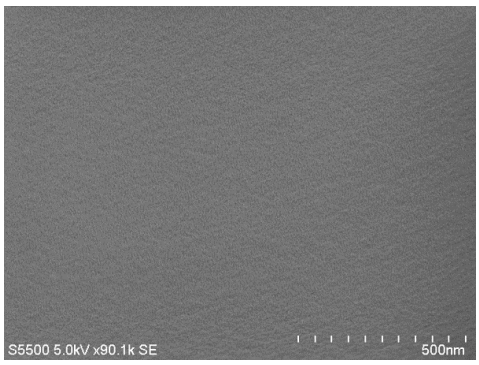
(a) GISAXS geometry principle.



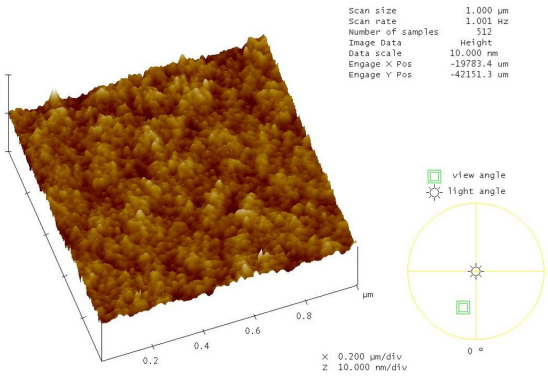
(b) GISAXS porous thin film schematic response.

Figure 2.12: GISAXS working principle and porous thin film schematic response [121].

The measurement duration depends on the material to analyse and on the X-rays light source energy. Indeed, the more reflective the material, the more important the signal detected. In our study, a copper Kα radiation of 0.15418 nm wavelength at 8048 eV source emitted by a rotating anode is illuminating the SiOC:H sample with a small incidence angle (figure 2.12.a). Our experiment required a 10h-long sensor signal accumulation because of the low reflectivity of this type of dielectrics. As suggested by preliminary SEM views of the SiOC:H material surface (figure 2.13.a), AFM scanning of a 1μmx1μm area of the SiOC:H surface, highlights the fact that the root mean square surface roughness is very low, 0.55 nm (figure 2.13.b). These observations are consistent with ellipsometric porosimetry results (figure 2.11), where no open porosity larger than 0.6 nm is detected.



(a) SEM view of the as-deposited POR SiOC:H material surface.

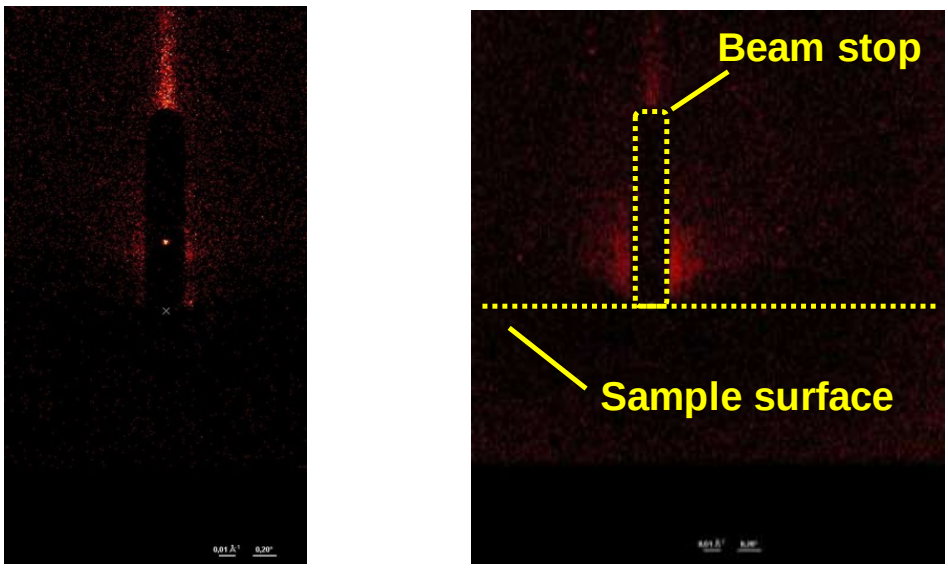


(b) AFM view of the as-deposited POR SiOC:H material surface.

Figure 2.13: Topological images of uncapped POR SiOC:H materials.

Computer-aided analysis of the GISAXS results in figure 2.14, together with visual comparison with expected porosity signature represented in figure 2.12.b and AFM images (figure 2.13.b), indicates that no pore signature is found neither in non-annealed (figure 2.14.a), nor annealed as-deposited SiOC:H materials (figure 2.14.b). These results

bring sufficient evidence to assert that our POR SiOC:H low-κ dielectric material has no porosity.



(a) GISAXS raw signal of the as-deposited POR SiOC:H material.

(b) GISAXS raw signal of the annealed POR SiOC:H material.

Figure 2.14: 10h GISAXS measurements on uncapped POR SiOC:H materials.

We thus confirmed that the POR SiOC:H considered throughout our whole study is an amorphous non-porous film. However, further analysis are required to gather information on its chemical structure. This is the aim of sections 2.5.3 and 2.5.4.

2.5.3 X-ray Photoelectron Spectroscopy and TEM Energy Dispersive X-ray

X-ray Photoelectron Spectroscopy (XPS) and Transmission Electron Microscopy (TEM) Energy Dispersive X-ray (EDX) are well-known physical characterisation techniques used by many research groups worldwide. Despite the fact that both methods can provide information on the material chemical composition, they have different applications. EDX is notably used to detect contamination and perform joint topology and material analysis [68],[61],[122] whereas XPS is often used for thin films composition analysis for instance [123]. It is worth noting that SiOC:H is composed of an important amount of hydrogen, however XPS and EDX, as an important number of characterisation methods, cannot detect it because it is a very light chemical element. Consequently, the quantifications produced by both methods have to be taken with precautions as hydrogen is considered virtually absent.

2.5.3.1 Principle of XPS and capabilities

The theoretical bedrock of the XPS technique is the famous Einstein's photoelectric effect [124]. Indeed, the studied material surface, SiOC:H in our case, is excited by X-rays, or ultraviolet light, which in turn emits electrons, called photoelectrons, whose

kinetic energy is analysed. From this measured kinetic energy, and with the incoming photon energy, the binding energy can be calculated with the following equation [125]:

$$h\nu = E_K + E_L + W$$

In which h is the Planck's constant, ν the photon frequency, E_K the photoelectron kinetic energy, E_B the photoelectron binding energy and W the photoelectron work-force. The binding energy is directly related to the electronic environment of the electron, more specifically its atomic orbital, hence the nature of the chemical element it originates from can be extracted through peaks deconvolutions [125]. In addition, it is possible to obtain a relative chemical quantification from resulting signal peaks area integration. However, because of the weak penetration depth of the UV light, the XPS technique is only sensitive to the sample surface, i.e. the first 10 nm [126]. Finally, Parallel Angle Resolved X-ray Photoelectron Spectroscopy (PARXPS) evolution allows one to discriminate the provenance depth of detected photoelectrons. This is achieved whether by tilting the sample and recording successively the photoelectrons incoming from each angle by limiting the angle acceptance, or parallel acquisition is possible for most advanced equipment having 2D detectors and particular monochromator, lens, analyser and detector arrangements [127].

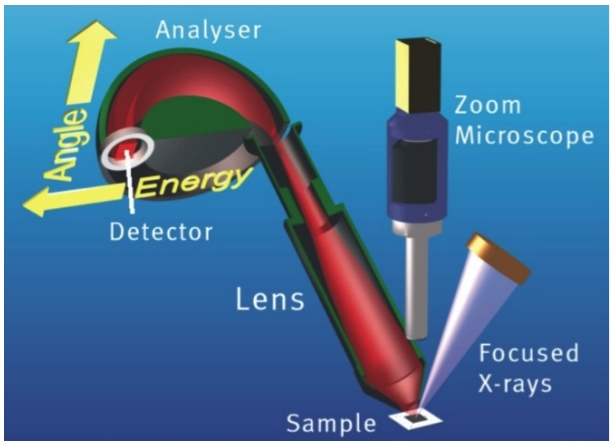


Figure 2.15: Parallel Angle Resolved XPS working principle (without any sample tilt) [127].

2.5.3.2 Carbon contamination

As the XPS technique is sensitive to first nanometres only, it is impacted by surface pollution. Amongst which carbon is often observed and has a particular impact because the material we study is composed of carbon as well. Figure 2.16 presents relative chemical composition analysis with an PARXPS of a POR, High-O and High-TMS SiOC:H blanket material. The indicated angle corresponds to the photoelectron provenance with respect to the sample normal angle. Relative quantifications are calculated, for every angle, by peak deconvolution of signals originating from carbon 1s, silicon 2p and oxygen 1s orbitals, noted C1s, Si2p and O1s respectively. As supposed intuitively, the High-O SiOC:H material contains more oxygen and fewer carbon than others. Surprisingly, POR material seems to contain more carbon and fewer oxygen than High-TMS SiOC:H. Anyway, the increased dose of TMS precursor appears to have a significant impact only on

carbon content but not on oxygen or silicon and moreover, it is only a partial picture as hydrogen is not detected and thus, this unexpected effect might be explained by the lack of data about hydrogen. Furthermore, an interesting signature can be observed: a carbon content increase for angles corresponding to the sample surface. This effect is clear for the three materials and is the signature of surface carbon contamination because samples have been stored in ambient atmosphere. Indeed, since carbon contamination is starting as soon as the samples are exposed to ambient atmosphere, it is difficult to discriminate the signal emitted by carbon contamination from the one emitted by carbon originally in the material. However, thanks to this PARXPS analysis, the bulk relative atomic percentages of our POR SiOC:H material are estimated to be 26 at. % for silicon, 41 at. % for oxygen and 33 at. % for carbon.

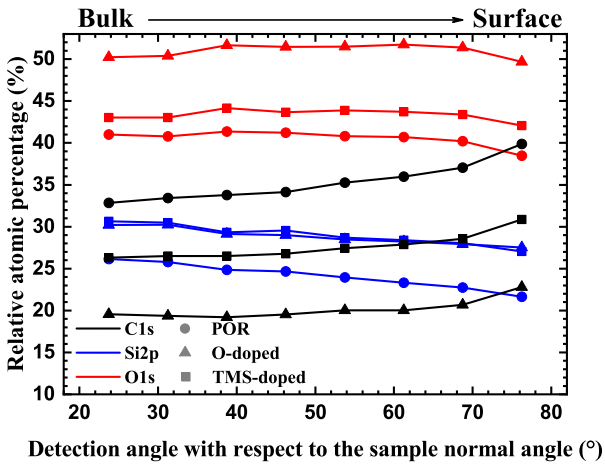


Figure 2.16: As deposited SiOC:H materials chemical composition depth profiles measured by PARXPS. Higher angles correspond to photelectrons emitted by the sample surface.

2.5.3.3 Differences between XPS and EDX

As detailed in section 2.5.3.1, with XPS, an X-ray beam is emitted and electrons are retrieved. For EDX, one can say it is the other way around. Indeed, a focused electron beam is sent through the sample which in turn produces X-rays which are analysed to obtain the binding energy. The main difference between both techniques resides in the fact that EDX can analyse several microns-thick cross sections whereas XPS is a surface analysis [126].

2.5.3.4 TEM Energy Dispersive X-ray analysis

As it is particularly suitable for contamination analysis, cross sections perpendicular to metallic lines in electrical characterisation structures (see chapter 3 for structures details and description) have been performed and a result is presented in figure 2.17. This type of analysis has only been performed on POR SiOC:H-based electrical test structures because integration of new materials requires extensive work to develop repeatable manufacturing recipes (see section 2.6 for details on variability) and thus, it was not achievable for High-O and High-TMS materials as many fabrications steps can be impacted by a change in the chemical composition of the low-κ material (see section 2.2 for more details on the

fabrication). The top picture is an image of the analysed region of an electrical structure which has been chosen because of its high leakage current (3.6 nano-Amperes at 15V). The EDX scan line is represented in orange starting from the side pointed by the yellow arrow. Consequently, the beginning of the line corresponds to 0 nanometre of the bottom right graph. The bottom left graph presents the spectrum retrieved where the red cross is positioned on the top image. A similar spectrum is extracted for each point in the scan line represented in the top image, then peak eras are extracted in each spectrum along the line. Peak eras are not directly comparable as each atom have its own signal intensity, however it is possible to determine the material composition from them. Looking at the bottom right graph, the beginning of the scan line starts in the TEOS material, as there is no carbon and the oxygen content is higher than further along the scan line. Then, a transition of composition lasting for a few tens of nanometres marks the interface with the SiOC:H dielectric and then, the composition in the SiOC:H dielectric material does not change significantly along material depth. Very similar results (results not shown here) are obtained on structures having leakage current varying at 15V from 4.3 pico- to 3.6 nano-Amperes.

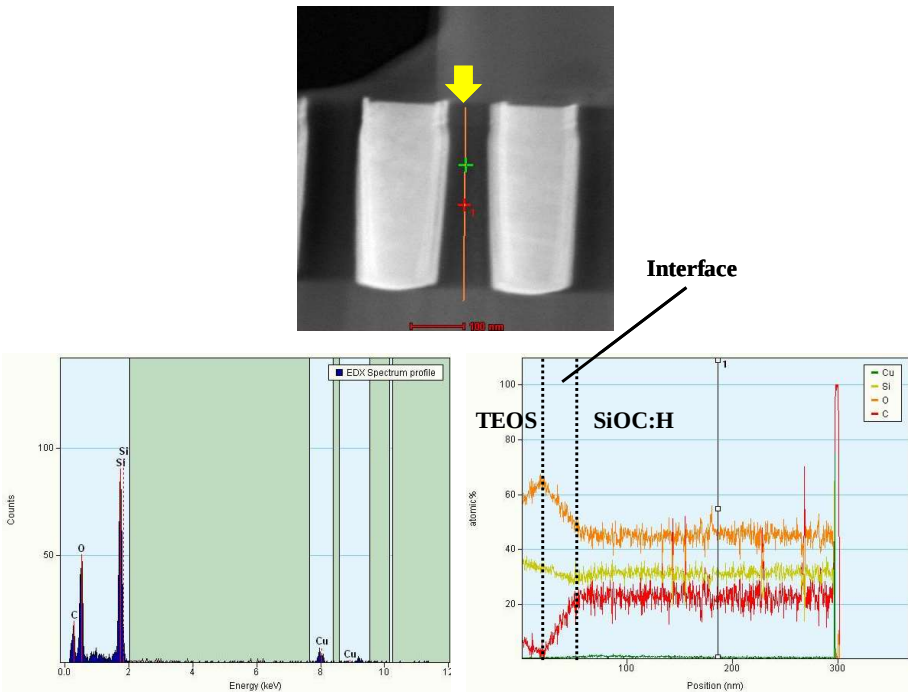


Figure 2.17: TEM view of a cross-section perpendicular to the integrated copper line (top). Left: spectrum recorded at the green cross. Right: EDX profile along the orange line on the TEM view (top).

As hydrogen is not detected, it cannot be used to detect moisture ingress, but oxygen might. However, EDX analysis did not put in light moisture contamination in the SiOC:H as oxygen concentration does not vary significantly in it. Furthermore, it is worth noting that no unexpected chemical element has been found in the SiOC:H material (see bottom left graph on figure 2.17). However, it is most likely that any slight chemical variation, which could nonetheless have important electrical effects, would be hidden by the large noise observed on the EDX signals. That is why a more sensitive technique is required to

observe the chemical impact of pollutants in the SiOC:H material.

2.5.4 FTIR and MIR spectroscopies

The Fourier Transform InfaRed (FTIR) spectroscopy, is a chemical characterisation technique widely spread. It is a powerful method to determine how a material is chemically structured. The Multiple Internal Reflections (MIR) derivative of the FTIR technique enhances further the detection sensibility by increasing the signal-to-noise ratio of the measurement but as it requires to cool the detector with liquid nitrogen, it is mostly used when FTIR results are not sufficient. Both FTIR and MIR techniques are based on the same principle: chemical bonds light absorption spectrum. Indeed, every chemical bond has different resonance frequencies for its five main types of vibration modes: stretching, rocking, wagging, bending, and twisting [128]. These resonant frequencies are detectable as they absorb light at their vibrating respective frequencies, in the infrared domain allowing to discriminate chemical bond from each other [129].

2.5.4.1 SiOC:H and moisture specific bonds

As we intend to study moisture in SiOC:H low-κ dielectric materials, it is necessary to point out absorption bands related to the material and eventual moisture-related material modifications. Aggregated data are summarised in table 2.1. This table does not intend to list exhaustively every vibration mode of every chemical bond present in the material but sufficient information to point out eventual chemical modification induced by moisture in the material.

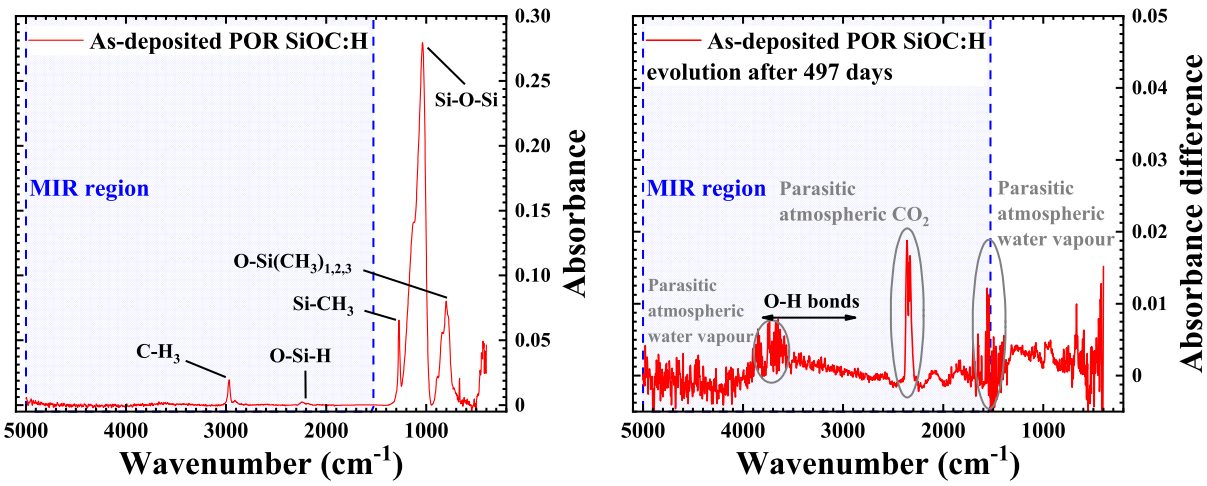
Chemical bond	**Wavenumber (cm^{-1})**	
$C-H_x$	2970	[130], [29],[113]
$O-Si-H$	2200	[130], [29], [128], [113]
$Si-CH_3$	1275	[130], [29], [128], [113]
$Si-O-Si$	1000-1200	[130], [29], [113], [128]
$O-Si(CH_3)_{1,2,3}$	700-900	[130], [29]
Moisture-related chemical bonds		
H-bonded H_2O	3300-3600	[130], [29], [113], [131]
Isolated and terminal $-OH$	3650-3800	[130], [29], [113], [131]
Hydroxyl (OH) terminals	3690	[130], [29], [113], [131]
Isolated surface silanols $Si-OH$	3750	[130], [29], [113], [131]
H-bonded $Si-OH$ in chain	3200-3650	[130], [29], [113], [131]
Parasitic chemical bonds		
Atmospheric CO_2	2300-2400	[113]
Atmospheric humidity	1400-1900	[113]
Interstitial O	1107	[113]
Substrate C	673	[113]

Table 2.1: Interesting chemical bonds summary table and associated literature.

Based on the data from table 2.1, the following of the study will lay the stress on moisture-related chemical bonds between 3000 and 3800 cm^{-1}.

2.5.4.2 FTIR and MIR spectroscopies

Figure 2.18.a is the FTIR absorption spectrum of a 500nm-thick POR SiOC:H blanket material. It clearly shows the pertinence of such technique as it allows to put into light the chemical bonds present in the blanket material, hence its chemical structure. From this spectrum, one can distinguish the SiOC:H characteristic peaks indicated in figure 2.18.a, mainly $Si-O-Si$ and CH_x. It is worth noting that it is difficult to link peak amplitude to chemical composition, or even to chemical bond ratios. Indeed, chemical bonds do not vibrate in the exact same manner: some peaks have the particularity to be very sharp, this is the case of the $C-H_3$ peak for instance, while other bonds such as $-$OH-related bonds present a broad absorption spectrum [132]. Nonetheless, it is possible to observe the evolution of peaks amplitude over time. That is why, FTIR measurements have been performed on samples over a long period of time: 497 days. As shown by the difference between the initial and the last measurement, (figure 2.18.b), the O-H bonds, synonym of moisture pollution, region seems to increase slightly but the signal and signal-to-noise ratio are too weak to provide reliable conclusions about potential moisture ingress. It is worth noting that we do not observe peaks which could originate from bonds between atoms constituting SiOC:H and other chemical elements.



(a) FTIR spectrum of as deposited SiOC:H blanket material.

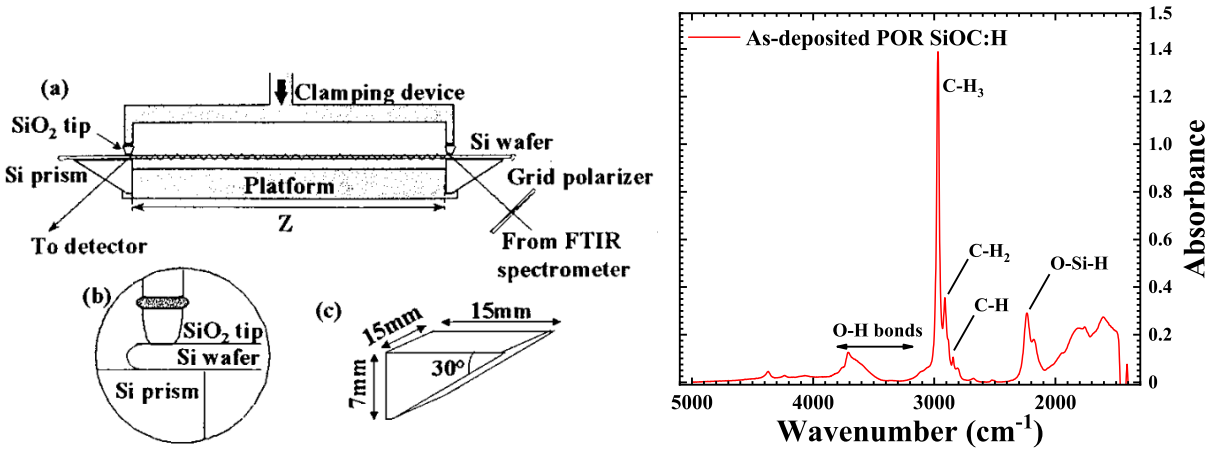
(b) Evolution of as-deposited SiOC:H blanket material absorbance after 497 days at room relative humidity and temperature measured with FTIR.

Figure 2.18: FTIR spectrum and evolution of as-deposited SiOC:H blanket material.

In order to improve the signal-to-noise ratio, Multiple Internal Reflections (MIR) is a good alternative considering the frequency domain of interest [131]. Indeed, in the FTIR method, light gets transmitted directly from the infrared light source to the detector through the analysed sample. Whereas the MIR method, as its name indicates, rests on internal reflections of the source light to cross the analysed material on a longer distance

2.19.a, increasing the signal-to-noise ratio as well as the spectrum absorption amplitude, which allows the detection of weak-absorbance chemical bonds or low concentration bonds [133],[131].

However, due to the fact that the optical beam crosses an important length of silicon, the prisms, the analysis spectrum is not as wide as FTIR. In particular, for wavenumbers lower than 2000 cm^{-1}, the signal is blinded by silicon crystal vibration modes [134]. Nonetheless, this has little impact on our study as this does not affect moisture-related chemical bonds detection, noted as O-H bonds in figures 2.18.b and 2.19.b. Moisture related-bonds are much more visible on MIR spectrum (figure 2.19.b) than on FTIR spectrum presented in figure 2.18.a. Moreover, the MIR spectrum in figure 2.19.b has been obtained only one day after deposition on a sample protected against moisture by a 20 nanometres-thick hydrophobic silicon nitride capping (not visible on the spectrum), which excludes a massive moisture ingress. This unequivocally shows that MIR is more pertinent for moisture-related chemical bonds study.



(a) Working principle of Multiple Internal Reflections (MIR) measurement setup [135].

(b) MIR spectrum of as deposited SiOC:H blanket material.

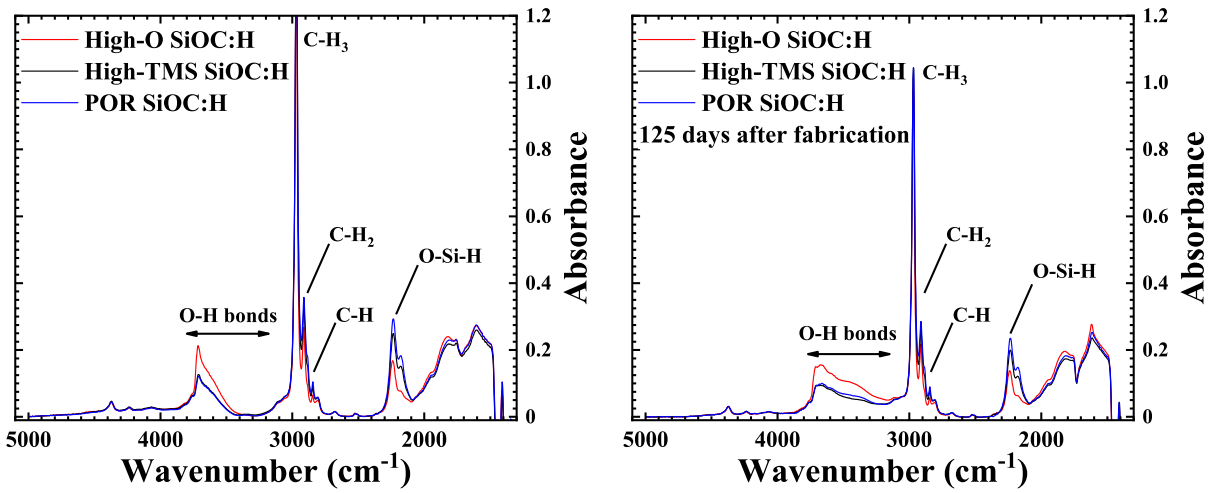
Figure 2.19: FTIR and MIR spectra of as-deposited SiOC:H blanket material.

2.5.4.3 MIR and hydroxyl groups

As explained in the previous section, the MIR technique is particularly suitable to observe moisture-related chemical bonds in SiOC:H dielectrics. Similarly to sections 2.5.3.2 and 2.5.2.1, three types of materials have been characterised with this spectroscopy technique: POR, High-O, and High-TMS (see introduction of section 2.5 for more details). Stacked plots in figure 2.20.a underline the differences generated by the variation of manufacturing recipes for silicon nitride capped samples measured only one day after the samples fabrication. More specifically, the figure 2.20.a highlights the fact that the High-O SiOC:H material has much more OH bonds than others. The sharp peak at 3700 cm^{-1} suggests $-$OH strongly bonded in the material. But it cannot be unequivocally attributed to the material itself as it could also mean this material is prone to fast moisture pollution during the very short time between dielectric and capping depositions. Alternatively, significant differences can be seen on the $O-Si-H$ peak where the High-O SiOC:H has the least while the POR has the most. This last point is interesting as it clearly shows

differences in the material $Si-O-Si$ skeleton: it is likely that the High-O SiOC:H has more $Si-O-Si$ bonds.

After 125 days of storage under ambient conditions, figure 2.20.b indicates that moisture has polluted the three SiOC:H materials, as shown by the stronger O-H bonds region. Moreover, this region has increased a lot more for the High-O SiOC:H material than for High-TMS and POR materials (figure 2.20.b), which underlines that the High-O SiOC:H material is particularly sensitive to moisture pollution.



(a) Stacked MIR spectra of three variants of the SiOC:H dielectric material deposited on silicon and capped by silicon nitride (not visible in spectrum).

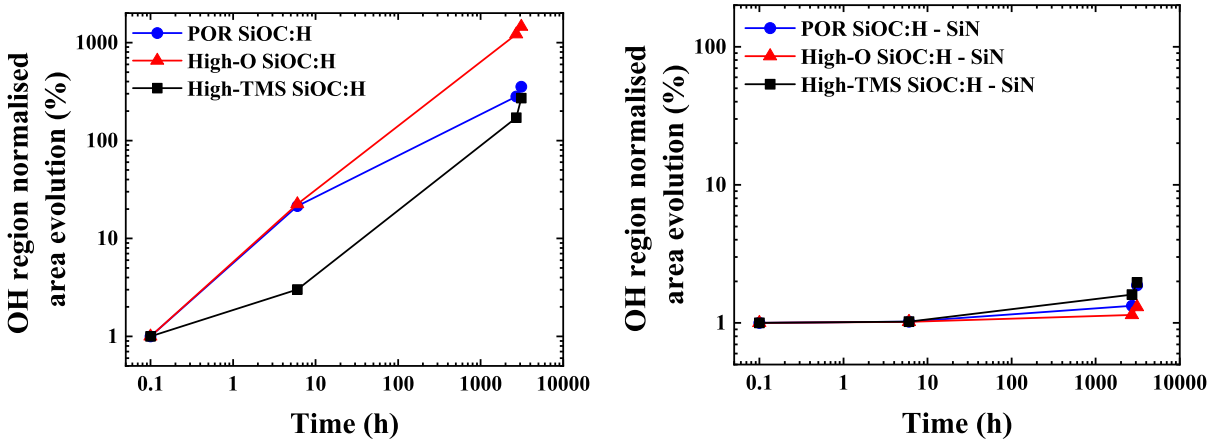
(b) Stacked MIR spectra of three variants of the SiOC:H dielectric material deposited on silicon after 125 days of storage in ambient atmosphere.

Figure 2.20: FTIR and MIR spectra of as-deposited SiOC:H blanket material.

Nonetheless, to study moisture pollution, direct comparison of first and last spectra, *i.e.* after 125 days of storage at ambient conditions, is complicated as signal amplitudes are not strictly identical. This amplitude difference is clearly visible when we look at the amplitude of CH_3 peaks. It can be due to the spacing between the two prisms which is not perfectly equal for the two measurements, in turn changing the optical length of the beam (see figure 2.19.a). Another parameter that can explain this variation is the quality of the optical coupling between the substrate and the prisms (see figure 2.19.a). However, as the concentration of CH_3 chemical bonds is constant over time in the POR SiOC:H [136], the peaks area can be normalized by the CH_3 peak amplitude to observe the evolution of the moisture-related region era.

This methodology allows to observe and quantify the increase of hydroxyl groups ($-OH$) in the SiOC:H blanket material over time such as in figure 2.21. Figure 2.21.a clearly shows that uncapped samples see dramatic moisture absorption as the normalised area increases for the three SiOC:H materials. To the contrary, the increase for samples protected by a 20 nanometre-thick silicon nitride capping, is very modest (figure 2.21.b). This suggests that moisture ingress is a least delayed for capped samples. Indeed, in presence of a silicon nitride capping, moisture cannot diffuse vertically but only from the edges of the wafer to reach the analysed region. It is worth noting that after 125 days, the uncapped High-O SiOC:H material evolution is about one decade higher than other

uncapped materials (figure 2.21.a). It is a second evidence that High-O material is more prone to moisture ingress. From this MIR analysis, several information have been drawn: firstly, it is clear that SiOC:H dielectric materials are prone to moisture ingress and that, blanket material evolution observation is possible with this technique. Secondly, even though all types of SiOC:H studied have been severely impacted by moisture ingress, the magnitude of moisture contamination is different. Indeed the High-O SiOC:H is, by far, the most vulnerable to moisture pollution. It hints that some chemical bonds play a specific role in moisture absorption by the SiOC:H. Finally, it has been shown that a 20nanometres-thick silicon nitride capping on the blanket material is particularly effective as vertical moisture ingress barrier.



(a) Evolution of moisture-related region normalised area of three uncapped SiOC:H blanket materials, stored in ambient atmosphere.

(b) Evolution of moisture-related region normalised area of three capped SiOC:H blanket materials, stored in ambient atmosphere.

Figure 2.21: Evolution of moisture-related peak area of three variant SiOC:H blanket materials.

2.5.5 Conclusion

An important amount of information has been gathered on the SiOC:H dielectric material through several chemical and physical characterisation techniques, each one having advantages and downsides. They allow to have a better understanding of the SiOC:H material chemical composition and structure.

Indeed, these analyses allowed to map essential properties of the SiOC:H low-κ dielectric material, which are crucial in order to understand chemical and electrical influence of moisture. Thereby, we confirmed experimentally that our SiOC:H has a relative dielectric constant of 2.9 without porosity, that at the chemical level it is mainly structured by CH_3 and Si-O-Si chemical bonds, and finally we confirmed it is quickly and importantly affected by carbon contamination. Moisture ingress in the SiOC:H dielectric material has been suggested by FTIR, then confirmed by MIR while no sign of other pollutant has bee evidenced. These information are required to provide physical interpretation of the peculiar electrical behaviour of structures in presence of moisture. Consequently, the aim of the following of our study is to correlate moisture-related physical and chemical phenomena and electrical behaviour of moisturised SiOC:H low-κ dielectric material. To

achieve this, dedicated electrical test structures and methodologies are required. The following chapter will focus on layout, fabrication and validation of these test structures as they are important aspects to consider because several manufacturing steps (section 2.2 for more details) together with variability, inherent to manufacturing processes (section 2.6), might play a role with respect to moisture ingress.

Chapter 3

Electrical test structures conception, process control and optimisation

"Before anything else, preparation is the key to success."

Alexander Graham Bell

3.1 Introduction

As discussed in section 2.2, the SiOC:H low-κ dielectric material undergoes an important number of process steps throughout the fabrication of the chip BEOL. Amongst them, a certain number involves direct interactions, hence potential modifications, with the SiOC:H material (section 2.4). Physical characterisation alone, is very unlikely to provide complete explanation of the material behaviour, especially under electrical fields, currents etc. Consequently, to study the electrical consequences of moisture ingress in the SiOC:H low-κ dielectric material, which is the final goal of the present study, it is necessary to integrate it in electrically addressable structures. Furthermore, these structures should be as similar as possible to the produced chip interconnects, hence they must present similar dimensions and be processed with a similar fabrication flow.

3.2 Structures design and mask set conception

In order to fabricate electrical test structures similar to final chip interconnects, it is necessary to ensure every step from structure Computer-Aided Design (CAD) to actual manufacturing is similar between the elementary electrical test structures, upon which our study will be based, and chips.

3.2.1 Structures CAD and mask set

At the very first step of test structure conception, the CAD allows to lay out metallic lines. CAD software generates files in gds format (.gds file) which represent the drawing of

the desired structure. Such software tool is usually combined with a Design Rule Manual (DRM) to ensure it is compliant with the technology node and fabrication constraints requirements for instance.

3.2.2 C2M and OPC principles

On such .gds file, Optical Proximity Correction (OPC) and CAD-to-Mask (C2M) post processing treatments are performed to take into account optical deformations inherent to the photo-lithographic process due to light diffraction and interference at the nanometre scale, which can have a significant impact on the final shape of the fabricated structures. They are pre-mask treatments as they have to be carried out before quartz-based and chrome-based mask order.

3.2.2.1 CAD-to-Mask

The CAD-to-Mask (C2M) treatment step consists in translating the CAD layout to physical masks. Indeed, different layers in the CAD layers can be merged on a mask, depending on the order of the process steps. There are also different types of masks, that will not be detailed here, determined by various parameters such as opening density, fabrication yield and cost strategy. Consequently, the C2M treatment is mainly composed of logical operation performed on every .gds file (figure 3.1).

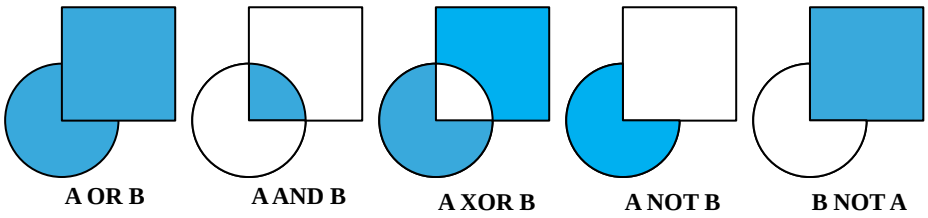


Figure 3.1: Main C2M boolean operations performed on CAD layout.

As C2M is applied on every structure on the silicon wafer, may it be an elementary test structure, a customer product, a chip seal-ring, a memory cell or a logic device, which all require different C2M algorithms, and thus, the so-called CAD markers differentiate areas corresponding to different devices. In consequence, to ensure the shapes and sizes of the elementary test structures will be similar to those in chips, it has been needed to take into account the fact that our structures will not undergo the same C2M algorithm than actual chips. In order to do this, a reverse analysis has been carried out on chips BEOL structures and comparison with elementary test structures C2M scripts has ensured that elementary test structures are as close as possible to actual chips BEOL structures. This analysis allowed to compensate at CAD level unwanted differences between chips and elementary test structures that will be studied later on. For instance, the spacing and widths of the elements composing the elementary test structure seal-ring have been resized in order to be identical to those of the chips (see section 3.3.5 for detailed seal-ring description).

3.2.2.2 Optical proximity correction

The Optical Proximity Correction (OPC) pre-mask treatment is done after the C2M. It consists in the optimisation of the mask patterns in order to allow a pattern on silicon as similar as possible to the initial CAD layout. As represented by figure 3.2, the initial CAD layout target is fed into an algorithm that simulates the insulated regions of the photoresist during photo-lithographic process step. Then, it measures the difference between the target and the simulated result. Elementary polygons composing the target layout are moved and resized in consequence to converge towards the CAD target. These steps are repeated until the convergence criteria is met.

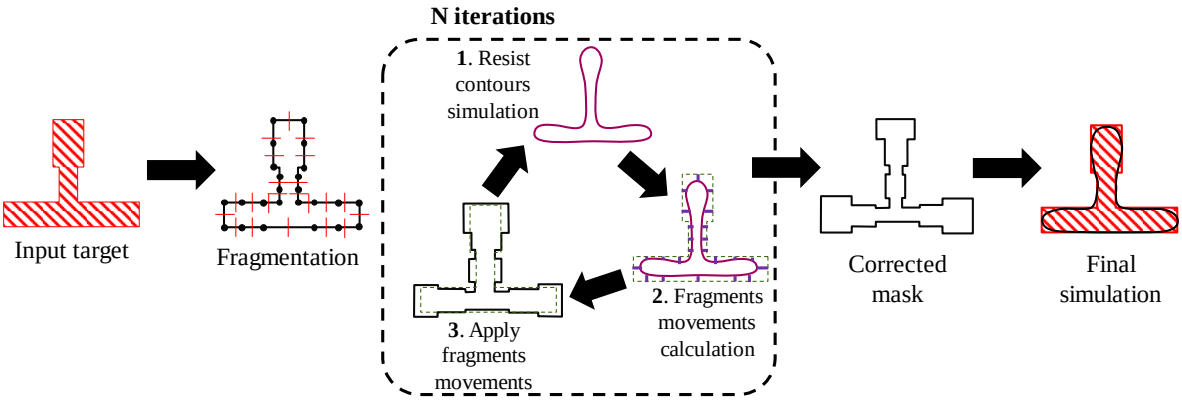


Figure 3.2: Example of OPC relevance on simple structures.

OPC has also been a valuable tool in the scope of our study to ensure unconventional elementary test structures were being fabricated with acceptable precision in our production tools. This appeared to be particularly efficient to exclude unmanufacturable structures, thus avoid potential yield losses or structures malfunction. As an example, elementary structures designed with line-to-line spacing as low as 70 nm have not been embedded because OPC models predicted they were unlikely to be functional due to lines gluing with current fabrication recipes, generating risks of defectivity.

3.3 Test structures detail

In order to study the electrical consequences of moisture on the SiOC:H low-κ dielectric material, a wide range of test structures is necessary. Indeed, different structures will allow to gather information on the moisture diffusion process, and how moisture correlates to the structures elementary parameters such as line-to-line spacing and length.

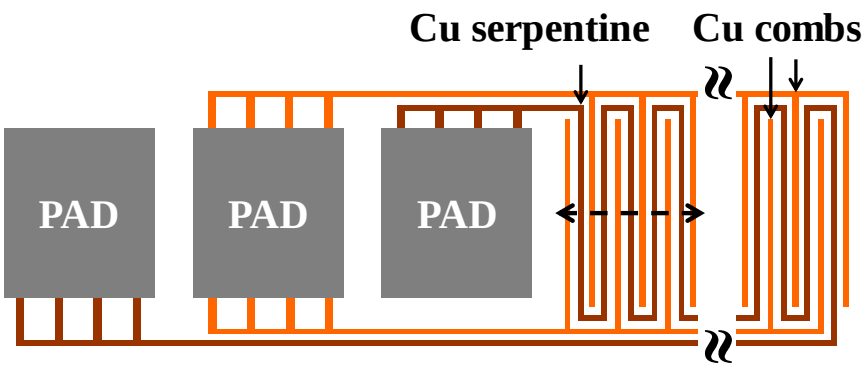
3.3.1 Experimental mask set

To conduct such studies, a complete BEOL mask set has been dedicated to electrical test structures. More specifically, a PMD stack is deposited on bare lowly resistive silicon wafers (type 1051), then contacts are etched and filled with tungsten. After this, the dual-damascene fabrication technique is employed to manufacture three metallic levels (see section 2.2) and finally, the Far BEOL is fabricated. All test structures studied in this

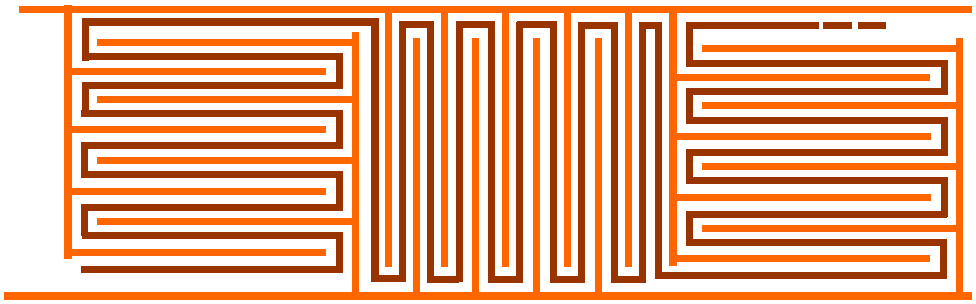
manuscript are embedded within this dedicated mask set. From design to manufacturing, the conception of this mask set followed the process of an actual chip mask set. Unless specified, electrical results presented in this work are obtained on the last copper level, referred as top-metal level. In fact, the three copper levels behave in the same manner with respect to moisture penetration however, in the case of moisture contamination from the top, the top metal level should be the first impacted.

3.3.2 Elementary test structure

Test structures must remain as similar as possible to ensure only one parameter varies from one structure to another, allowing direct comparisons between them. That is why, most of the structures that will be detailed in the following are based on a very common BEOL test structure often referred as interwoven serpentine/comb (figure 3.3.a). In order to diminish the variability effect on metallic lines patterning, the serpentine/comb interlacing is divided in two types of blocs, one where the combs are perpendicular to the pad alignment direction, and the other where they are parallel to the pad alignment direction, hence called horizontal and vertical blocs respectively (figure 3.3.b).



(a) Illustration of the elementary electrical test structure.



(b) Illustration of alternated horizontal and vertical blocs.

Figure 3.3: Schematic top view of the elementary structures.

3.3.3 Surface variations

Based on the principle shown in figure 3.3, the number of blocs is varied in order to obtain several similar structures with only one variable parameter: the interwoven Comb-Serpentine-Comb (C/S/C) metallic lines length. Table 3.1 summarises the structures

having different C/S/C lengths, spanning over two decades, from 3.7 cm for the smallest to 384.4 cm for the longest.

Test structure name	Number of blocs	Serpentine length (cm)
SU & SUBP	4	3.7
S04 & S04BP	7	11.9
S & SBP	15	28.4
S2 & S2BP	50	40.3
S3b & S3BP2	81	80.2
S3 & S3BP	100	86.1
S4 & S4BP	181	160.3
S5 & S5BP	424	384.4

Table 3.1: Metal C/S/C structure length variations summary. S stands for surface.

3.3.4 Line space variations

In order to estimate the interconnect reliability dependence on several parameters such as applied electrical field or oxide/copper ratio for instance, structures with various line-to-line spacings and widths have been designed. Table 3.2 summarises the structures designed and their respective line-to-line spacings and copper line widths.

Test structure name	Line spacing (nm)	Line width (nm)
SPC2BP	105	134
SPC3BP	120	134
SPC4BP	126	134
SPC5BP	140	134
SPC6BP	165	134
W1BP	126	120
W2BP	126	262
W3BP	126	402

Table 3.2: Top metal level line space and width variations summary table.

3.3.5 Seal-ring

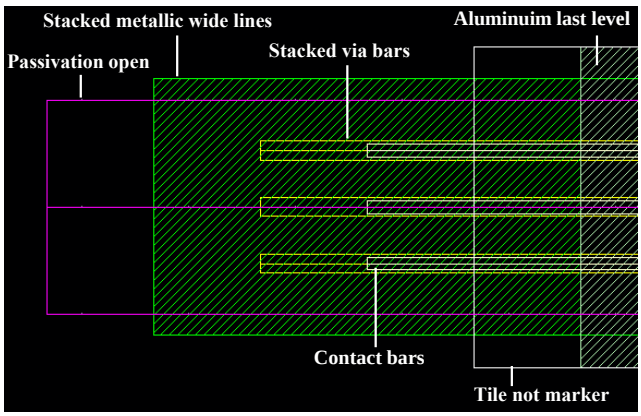
3.3.5.1 Role in conventional chips

In order to understand the role of the chip seal-ring, it is helpful to recall that once the wafer fabrication is over, they have to be cut to obtain chips. This wafer-dicing step can be very traumatising for chips as it may involve an important amount of mechanical stress due to sawing, charging, contamination in the case of plasma-based dicing, thermal heating and dilatation if laser singulation is used. Moreover, these techniques can be combined, hence chips must be protected from contamination, but also from delamination and mechanical stress-induced cracks diffusion from the chips edges at the same time.

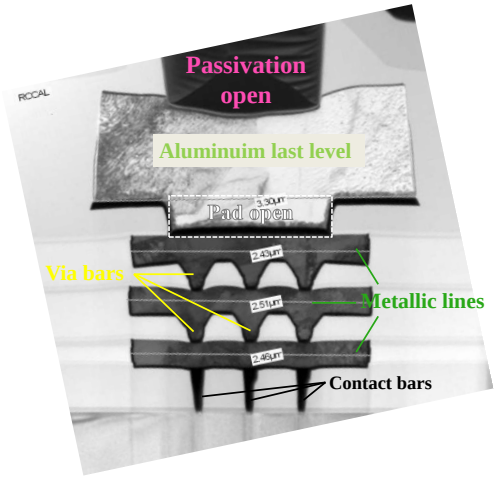
Consequently, the seal-ring serves several purposes, protecting the chip chemically and mechanically.

3.3.5.2 Adaptation to reduced size test structures

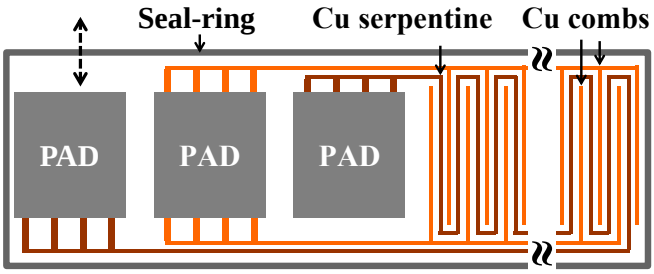
This protection is also required for elementary electrical structures, however, as they are characterised at wafer level, wafer dicing will not be performed. In consequence, the mechanical protection offered by the seal-ring is not crucial. Which turns out to be particularly convenient as tightness to external pollutants can be achieved with narrow seal-rings, which does not offer case of cracks and mechanical protection. Hence, this allows to design a narrower seal-ring in elementary test structures, which is required to ensure that these test structures can be placed in dicing streets between chips. For our study, a seal-ring has been especially designed in order to ensure tightness to external pollutants, especially moisture, preventing lateral pollutants diffusion. Because it intends to be as similar as possible to an actual chip seal-ring, it has been designed according to the DRM rules. Therefore, it consists in a stack of wide metallic passes connected by three via, or contact, placed side by side (figure 3.4).



(a) Description of the seal-ring CAD layout.



(b) Perpendicular cross-section of a test structure seal-ring.



(c) Example of use of seal-ring in test structures. The dashed arrow corresponds to the cross-section in figure (b).

Figure 3.4: Electrical test structure compatible seal-ring.

This seal-ring CAD (figure 3.4.a) is the result of a detailed comparison with seal-ring of actual chips C2M and simulation by OPC algorithms. Indeed, as explained in section 3.2.2.1, chips and test structures are not subjected to the same C2M algorithms, hence differences have been compensated by adjusting the seal-ring CAD in order to obtain the same silicon footprint than an actual chip.

3.4 Process control and optimisation

It is clear that process control is required throughout the fabrication process in order to guarantee every step meets production targets, hence expected functionality of chips and test structures within acceptable variability boundaries. To ensure such targets are met, several methods are jointly used. Inline process control, which consists in extensive measurement after every critical fabrication step and production recipe qualification and optimisation. These aspects have been extensively studied and are crucial in the semiconductor industry, hence we do not aim to provide exhaustive detail here but a slight overview of what is needed to produce high quality electrical test structures.

3.4.1 Inline process control

Inline process control is a general term to designate measurements performed on unfinished wafers, to ensure one or several fabrication steps have been satisfactory realised before continuing the fabrication. Different types of measures are carried out depending on the fabrication step to be assessed.

3.4.1.1 Thickness

A critical step for the BEOL is the CVD (or PECVD) deposition of dielectrics as described in section 2.2. Indeed, variability in deposited thickness would lead to level-to-level capacitance and leakage current variations, which is neither acceptable in our case, nor in actual chips fabrication. Consequently, after material deposition, for instance after SiOC:H low-κ dielectric, thickness is measured by ellipsometry and must be within acceptance margins around the target to continue on its route to the next fabrication step.

3.4.1.2 Critical Dimensions

Similarly, after insolation and etch steps, the actual line-to-line spacing and line width are measured by inline SEM, also referred as CD-SEM because they are exclusively used for Critical Dimension (CD) measurements, in order to detect eventual defects or off-target variability. Once more, this type of process control is needed for the fabrication of our test structures and even more important for actual chips. In the same manner than for thickness measurements, if it does not meet the targets, the wafer will not continue on its route. Depending on the step considered, the problem can be solved by a reprocessing. In particular, if CD of the insulated photoresist resin is off-target after the photo-lithographic step, all the photoresist resin can be removed before a reprocess.

3.4.2 Process optimisation

To make sure test structures used throughout the following studies have the wanted line-to-line spacing, copper line thickness and width, robust and perfectly tight seal-ring, control TEM cross-sections are performed. This section will mention most significant developments that have been required to provide as-expected test structures.

3.4.2.1 Structure line width and spacing

Line width and spacing are important parameters to check as they have a direct impact on the electrical properties of the test structure, such as Time-to-Breakdown (T_{BD}) and line-to-line leakage current for instance. To this extent, several cross sections have been performed on several locations of the structure and in several sites on a wafer to evaluate the field-to-field variability (see section 2.4.1). Figure 3.5 is an example TEM cross section in the C/S/C structure on which the line spacing, width and thickness are measured.

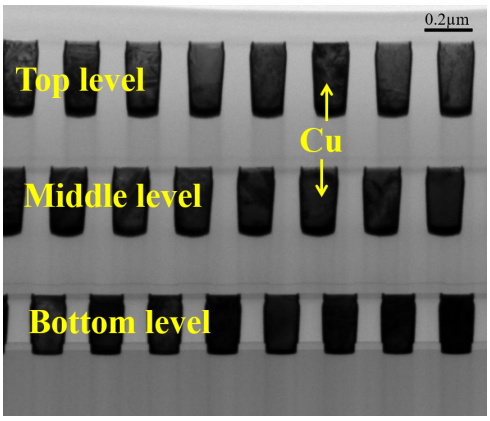


Figure 3.5: Cross section perpendicular to the copper lines of the C/S/C structure.

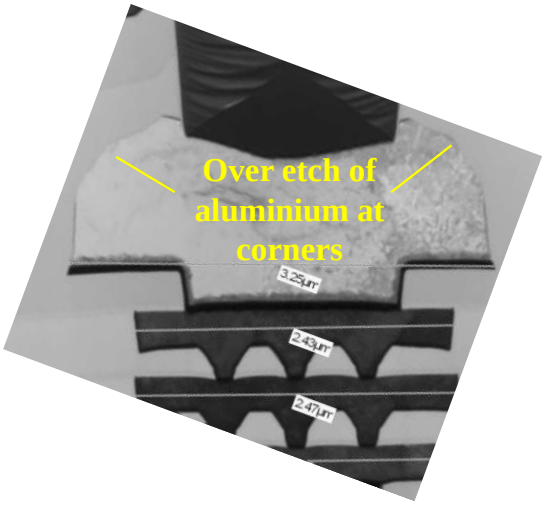
The following table 3.3 summarises the results of those inspections. It underlines that the bottom dimension (space and width) are very close to the expected target, however top dimensions are different. Unfortunately, this discrepancy is inherent to the via and line etch which is realised in two steps (see section 2.2). The second step is aggressive to allow repeatable via opening though SiCN copper capping of the line underneath.

Measure type	Center	Mid-radius	Edge	Target (nm)
Line-top space (nm)	100	110	92	134
Line-bottom space (nm)	120	131	134	134
Line-top width (nm)	144	148	154	126
Line-bottom width (nm)	128	119	116	126
Line thickness (nm)	319	344	291	330

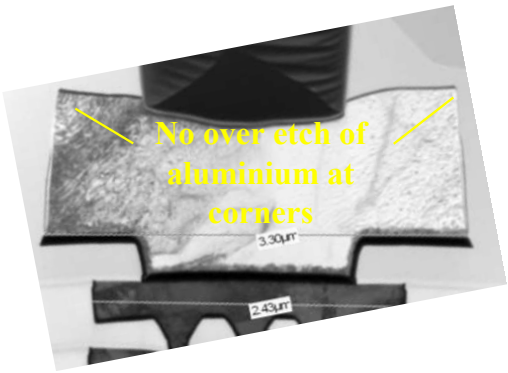
Table 3.3: Top metal level line space and width variations summary table.

3.4.2.2 Aluminium deposition and etch process step

As described in section 2.3.3, a good control of the aluminium etch is crucial in preventing moisture diffusion paths. That is why, at the end of the fabrication process, the quality of the aluminium in pads and in the seal-ring has been checked. This allowed to optimise the chemistry used as the first trials have clearly shown that the aluminium etch chemistry was too aggressive for the quantity of aluminium to be etched on the wafer surface (figure 3.6.a). Consequently, lower the etching gas concentration proved to produce better aluminium aspect in our case, as shown in figure3.6.b.



(a) Perpendicular cross-section of a seal-ring, showing aluminium over etch.

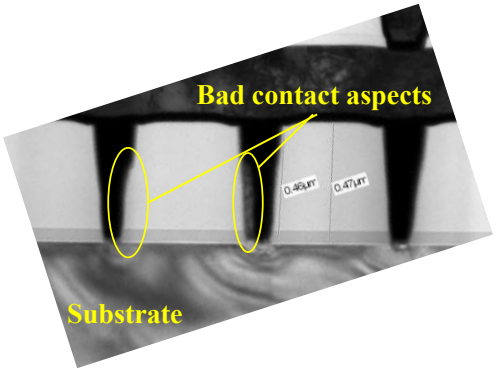


(b) Perpendicular cross-section of a test structure seal-ring after aluminium etching correction.

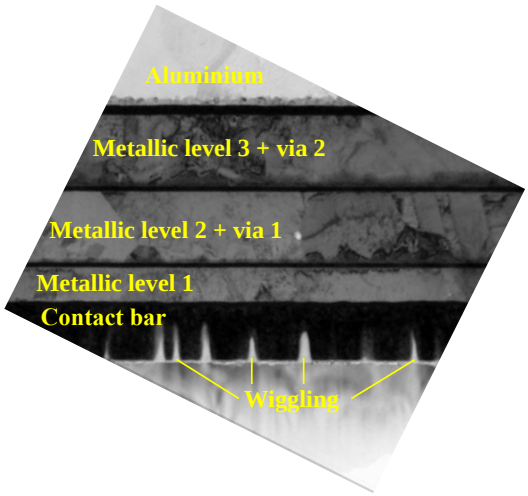
Figure 3.6: Cross-sections before (3.6.a) and after (3.6.b) aluminium etching correction.

3.4.2.3 Seal-ring bars profile improvement

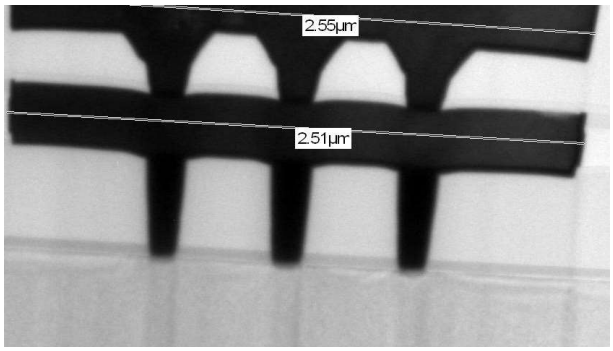
In the same manner, longitudinal and perpendicular cross-sections have been realised in the seal-ring in order to assess its manufacturing process regularity as it will constitute an important element for our studies. Figure 3.7 presents an example of a process improvement that has been necessary at the contact level because of dangerous irregularities observed with the standard recipe. Indeed, as it can be seen on figure 3.7.a, the contact shape is rather unusual. The narrowing at the bottom is problematic as it means the contact bar is likely to let a space between the bottom of the contact and the substrate, considering the length of contact bar required to constitute the seal-ring (3.7.b). Therefore, the etching chemistry has been adjusted to improve the regularity of the contact bar on the wafer surface and increase the contact CD at the bottom which is not critical for our test structures because their purpose is not to connect a FEOL device such as a transistor for instance. To be more precise, the etching of the first copper line and contact is performed in two sub steps, (described in section 2.2.3), the second step, is responsible for the deeper part etch and contact opening. That is why the oxygen flow of the second step has been increased to produce a more aggressive etch, hence a contact bar with a slightly larger CD. In turn, this reduced the effect of photoresist resin wiggling in contact bars constituting the seal-ring at the contact definition process step (figure 3.7.c).



(a) Bad contact aspect before recipe modification.



(b) Contact bar wiggling in seal-ring longitudinal section before recipe modification.



(c) Good contact aspect after recipe optimisation.

Figure 3.7: Contact level cross-section in the same direction than the seal-ring before 3.7.a, 3.7.b and after 3.7.c the contact etch recipe shape regularity improvement.

Once structures have been designed, and the manufacturing process assessed and previously mentioned process improvements carried out, it has been necessary to confirm that the produced seal-ring is perfectly tight to moisture and other pollutants. Indeed, this is crucial to provide a solid basis to our studies as they greatly depend on the seal-ring efficiency. This is done in section 3.5.

3.5 Test structures and multi-probing influence

Prior to any study, it is required to ensure that the electrical test methodology that we will need for moisture study is reliable enough to allow repeatable measurements over time. One of the main requirements is that our automated test hardware equipment (an Electroglas 4090μm) does not induce a degradation of the structures this study will rely on.

3.5.1 Context

In many applications such as automotive and medical, chips must be highly reliable and thus, pass challenging quality assessments including Wafer-Level Reliability evaluation, exhaustive Parametric Test and extended Electrical Wafer Sort. To fulfil such demanding requirements, a large number of test structures – placed in wafer dicing streets – are needed. Hence, prior to our study, it is necessary to assess the pads reliability and efficiency to keep moisture out of our electrical test structures despite an extensive number of probings. Furthermore, the smaller the die, the higher the wafer area dedicated to dicing streets. Indeed, figure 3.8 plots the percentage of wafer area dedicated to dicing streets as a function of die area. Percentages are calculated assuming a square die and same street width on X and Y. When the die is not a square, the percentage of wafer area dedicated to dicing streets might be slightly different. Therefore, a way to reduce the dicing streets area is to reduce the street width. To this extent, structures with narrower pads are mandatory but, probing equipment having a limited precision, hitting small pads in reduced street width might provoke non-previously existing reliability issues in test structures.

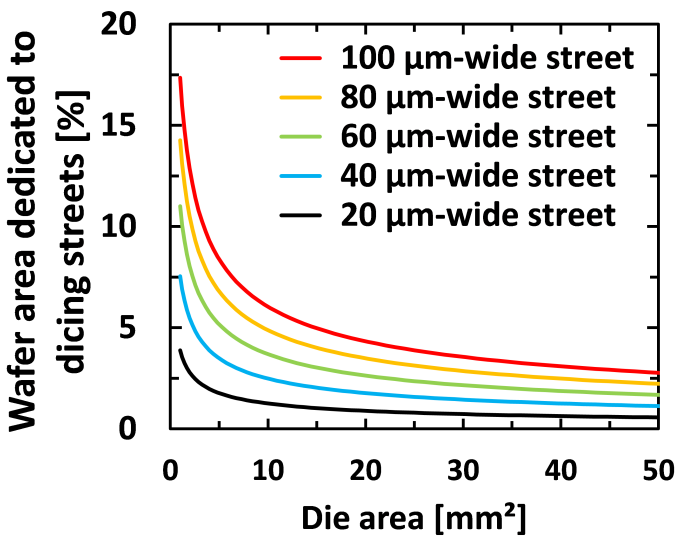


Figure 3.8: Percentage of dicing streets area as a function of the chip size for different street widths.

Consequently, it is interesting to determine at which point the pad width becomes critical in order to guaranty high quality standards. The corollary is true for our moisture-related study where very robust pads are needed to allow multiple probing without putting at risk the pad tightness.

3.5.2 Pad tightness

Hence, as suggested in section 2.5, it is crucial that pads remain tight to external pollutants while allowing electrical connectivity. However, probing equipment having a limited precision, hitting 70μm-heighten by 70μm-wide pads might provoke non-previously existing reliability issues in test structures. Consequently, test structures with pad width varying from 30 μm to 130 μm with a step of 20 μm have been designed. To remain compatible with our probing equipment, pads spacing and height are kept to 60μm and 70μm, respectively. Moreover, the serpentine length is kept to 86.1 cm and the line-bottom distance to 134 nm (see tables 3.1 and 3.3).

3.5.2.1 Pad structure

Pads are constituted of a stack of all metallisation and via levels (figure 3.9) described in section 2.3. This serves two main purposes, electrical connectivity available at every level of the interconnect and robustness and rigidity to endure the mechanical stress induced by probing.

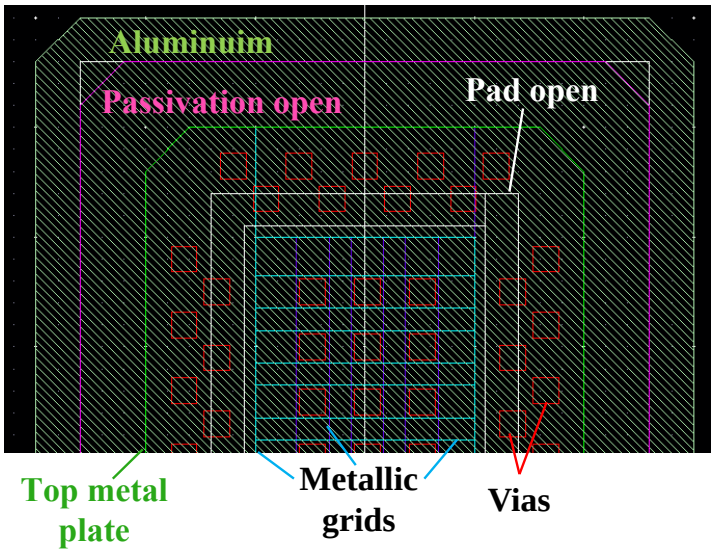
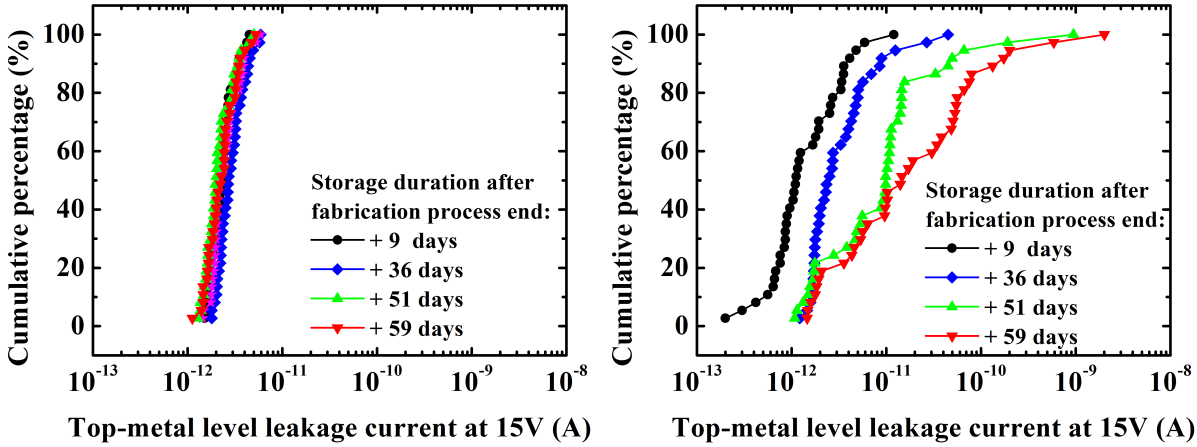


Figure 3.9: CAD pad structure.

3.5.2.2 Multi-probing and pad size

At the end of the fabrication process, leakage current of structures enclosed by seal-ring has been regularly measured during 59 days with a bias of 15 V while wafers were stored at room condition. When the pad width is between 50 and 130 μm, leakage does not evolve as time since fabrication process end increases (figure 3.10.a), which confirms the seal-ring efficiency to block moisture ingress in the structures. To the contrary, for 30μm-wide pad structures, the leakage increases dramatically right after the first measurement (figure 3.10.b).



(a) Cumulative distributions of measured leakage currents at 15V measured on structures with 70μm-wide pads.

(b) Cumulative distributions of measured leakage currents at 15V measured on structures with 30 μm-wide pads.

Figure 3.10: Cumulative distributions of measured leakage currents at 15V for test structures having different pad widths.

In order to ensure that leakage current increase observed on 30μm-wide pads structure is not the consequence of copper corrosion, serpentine resistance measurements have been carried out and no evolution was observed as shown in figure 3.11. Measurements for structures with wider pads produce similar distributions.

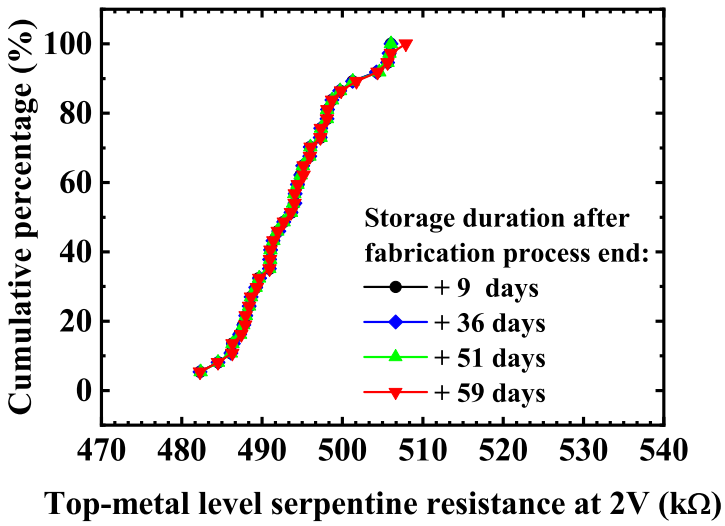


Figure 3.11: Cumulative serpentine resistance 30μm-wide pads structures.

Every structure has been observed by SEM and only 30 μm-wide pad edges are found to be widely damaged (figure 3.12). Therefore, we can assume that the observed leakage current increase is due to moisture ingress through the identified cracks.

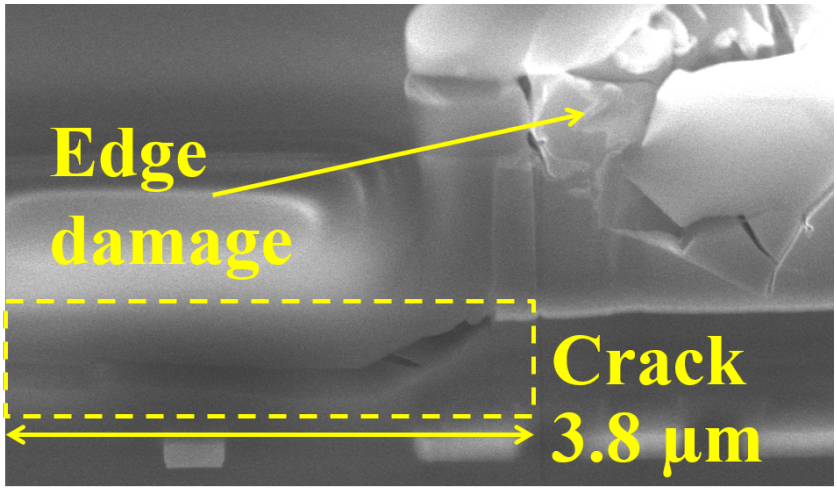


Figure 3.12: SEM inspection of 30 μm-wide pads, showing heavily damaged pads.

To confirm this assumption, a slightly misaligned probing has been performed on 50μm-wide pads just after the measurement carried out 51 days after fabrication process end. On the measurement performed only 8 days later, a leakage current increase is observed on the 50μm-wide pads structure (figure 3.13) while no increase is seen for 70, 90, 110 and 130μm-wide pads structures.

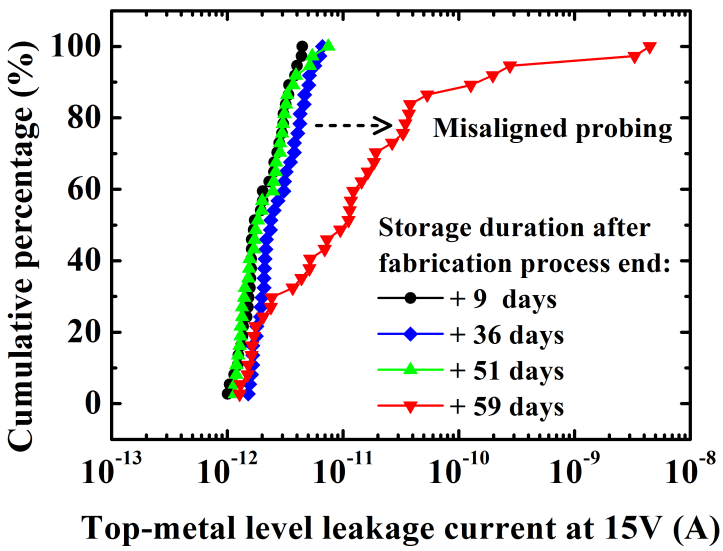


Figure 3.13: Cumulative leakage currents measured at 15V on 50μm-wide pads.

To confirm that the observed leakage current increase only 8 days after the misaligned probing (figure 3.13) is due to damages to the pad structure, such leaky structures have been observed using cross-section SEM technique (figure 3.14). These observations reveal deep cracks diving from the pads edge to BEOL layers providing a path for moisture ingress as shown in figure 3.12. Looking at this SEM image, it seems clear that the probe tip hitting close to the edge of the pad produced important damages under the passivation layer. The long crack dives down to the second copper metallic layer which makes the passivation pointless.

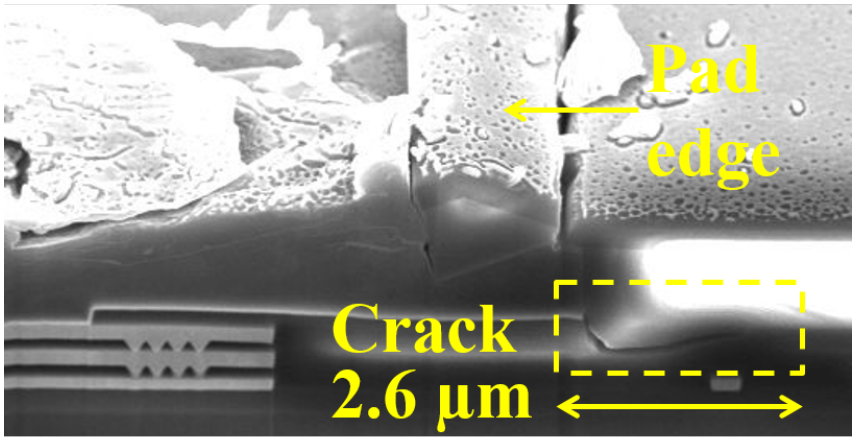


Figure 3.14: SEM image of an important crack diving under the passivation layer of a 50μm-wide pads.

This further confirms that narrow pads are not suitable for multi-probing tests as probe tips hitting close or on the pad edge provokes important cracks.

3.5.2.3 Consequences

We highlight that an important number of probe touchdowns on the same structure may have an impact on the final results of the study, which is not acceptable, if pads are narrower than 50μm. However, 70 μm-wide are also at risk if the number of required touchdowns is important, hence only pads larger than or equal to 90μm seem reliable in that case. Consequently, based on the results from this analysis, in particular figure 3.10.a, it has been chosen to use 110μm-wide pads on every structure that will be involved in the following studies with multi-probing over time. The acronym BP at the end of the structures name used in the following studies, and in table 3.1, will refer to 110μm-wide pads. This ensures our future results will not be biased by the impact of probing itself on the structures but the consequence of their own degradation. Nonetheless, it should be noted that it implies that, despite a compatible seal-ring, our electrical test structures cannot fit in dicing streets anymore, which is a considerable downside for an evident industrial reason: costs. Thus, despite of being used for this study, 110μm-wide pads are not interesting from an industrial point of view.

3.6 Conclusion

To conclude, electrical test structures have been designed taking into account C2M algorithms and OPC treatment differences between test structures and actual chips. This has been necessary in order to ensure the silicon targets and results are as similar as possible to chip BEOL. Once these steps have been successfully completed, in-line process control allowed to ensure the electrical test structures mask set presented similar morphological parameters to standard production wafers of the same technology, which is crucial in the scope of our study. Also, SEM and TEM inspection techniques allowed to spot and correct irregularities observed in the seal-ring contact level and aluminium cap

for instance. Then, it has been shown that the seal-ring provides an efficient protection against moisture ingress, a crucial point for the following of our study. Furthermore, a study of the effect of multi-probing has been carried-out. It pointed out that narrow pads can be heavily damaged by multi-probing as cracks can be formed from the pad edge extending to lower metallic levels, which leads to a dramatic ingress of moisture in the structures. This study confirmed the relevance of wide pads to prevent unwanted moisture ingress, as a result, 110μm-wide pads will be used for moisture-related studies. The work presented in this section constitutes the prerequisite necessary to the study of SiOC:H low-κ dielectric material electrical characteristics and the influence of moisture on them.

Chapter 4

Moisture and electrical characteristics of SiOC:H dielectric

"What is wanted is not the will to believe, but the will to find out, which is the exact opposite."

Bertrand Russell

4.1 Introduction

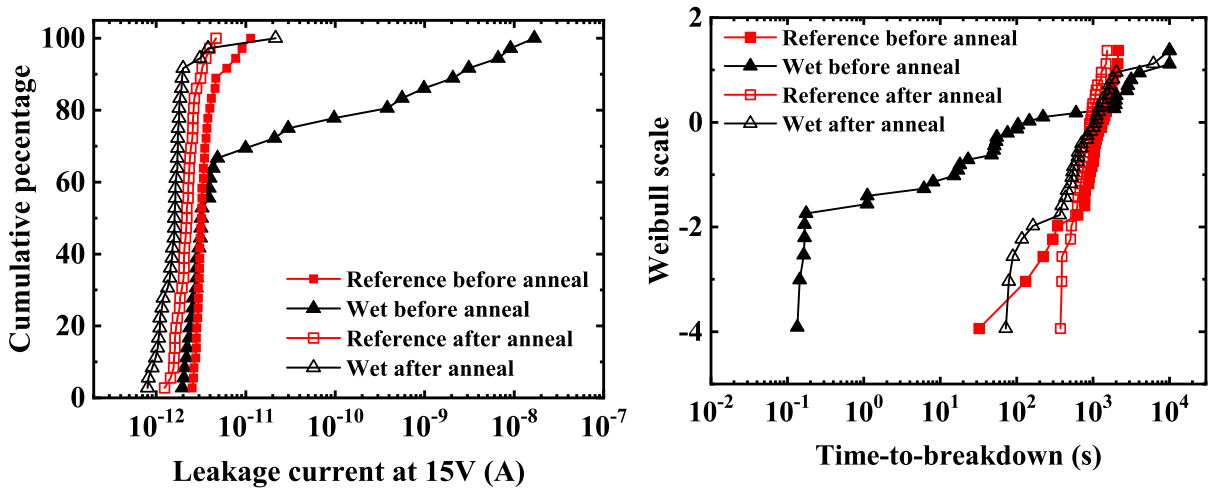
In order to gather more information on the effect of moisture on the SiOC:H low-κ dielectric, it is necessary to thoroughly study its electrical properties and their modification in presence of moisture. For that, the set of electrical test structures described in chapter 3 will be used, and the characterisation techniques presented in section 1.4.2, together with more unconventional techniques, will be employed. The aim of this analysis is to correlate the SiOC:H electrical behaviour with the chemical information gathered in chapter 2 to allow a physical understanding of the peculiar electrical behaviour of the SiOC:H low-κ dielectric in presence of moisture.

4.2 Thermal anneals and moisture ingress acceleration methodology

First of all, to conduct this study, it is necessary to have electrical test structures that are polluted by moisture. However, as seen in section 2.5.4, because of silicon nitride used in the Far BEOL (see section 2.3 for more detail), moisture is relatively slow to diffuse into the SiOC:H material. As a consequence, moisture ingress is particularly time taking which is not suitable from an industrial perspective. Hence, it is necessary to find a proper moisture ingress acceleration methodology.

4.2.1 High temperature anneal effects

In the search for such methodology, it is necessary to ensure that the wafers used to evaluate candidate methodologies are taken in the same initial state with respect to moisture pollution. Thus, prior to evaluation, a high temperature anneal is systematically performed to desorb moisture that might have previously polluted the SiOC:H dielectric material. The effects of a 72 hours-long 300∘C anneal on electrical parameters have been investigated by leakage current and time-to-breakdown measurements. As it is a destructive measurement, the time-to-breakdown is measured on identical structures, that are placed side by side in order to reduce in-field variability. Firstly, figure 4.1 underlines the fact that such anneal has no significant effect on SR3BP protected test structures, *i.e.* on structures enclosed by a seal-ring (see section 3.3.5 for more details). Thus, they are called reference structures as their electrical characteristics, such as leakage current or time-to-breakdown, are not impacted by moisture and shall serve as reference values. To the contrary, on S3BP unprotected test structures, *i.e.* without seal-ring, also called wet structures, the leakage current is recovered by the anneal in the sense that, after anneal, it is very close to the seal-ring protected structure one while it was much higher before anneal. In the same manner, the time-to-breakdown distributions of unprotected annealed and protected test structures are very close and much higher than the distribution obtained on not-annealed unprotected test structures, highlighting the recovery effect of the 72 hours 300°C anneal (figure 4.1.b).



(a) Leakage current distributions of test structures before and after a 72 hours anneal at 300°C.

(b) Time-to-breakdown Weibull distributions of test structures before and after a 72 hours anneal at 300°C.

Figure 4.1: Recovery of leakage current and time-to-breakdown by a 72 hours anneal at 300°C on moisturised test structures.

Nonetheless, a 300°C anneal for several hours presents the disadvantage to be potentially harmful for the interconnect structure, by interface degradation for instance [137]. Hence, in order to avoid this degradation, the temperature of such anneals is kept below 300∘C. In the following of our study, a 24 hours anneal at 250°C is used as a recovery anneal, even though some moisture might remain at this temperature [53]: interface integrity is of prime importance.

4.2.2 Moisture-related ageing acceleration

Thanks to the recovery offered by this high temperature anneal, we can ensure that wafers are in similar state with respect to moisture before being submitted to different climatic chambers and assess which one is the most effective to induce moisture ingress.

4.2.2.1 Methodology

As a consequence, a common procedure has been applied to the test wafers, summarised by figure 4.2. First the recovery anneal, is performed to recover leakage current and time-to-breakdown and then the test wafer is placed in a climatic chamber for 168h (one week) where temperature and relative humidity can be adjusted. This storage under controlled environment is often referred as Temperature Humidity Bias (THB) in the literature [80] and is extensively used in the industry for wafer-level and packaged chips qualification standard procedures [138], [139]. Before and after recovery anneal and climatic chamber storage, leakage current and time-to-breakdown are measured on protected and unprotected test structures. Hence, the effect of each step can be qualitatively measured by comparison of leakage current and time-to-breakdown distributions.

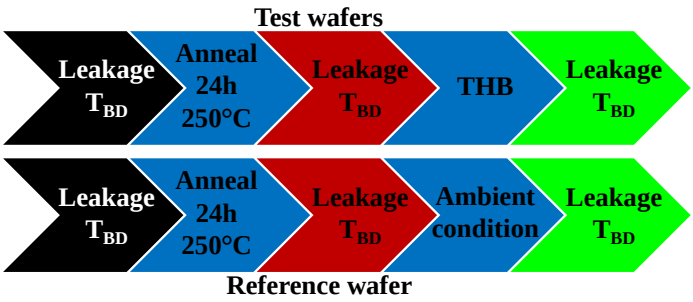
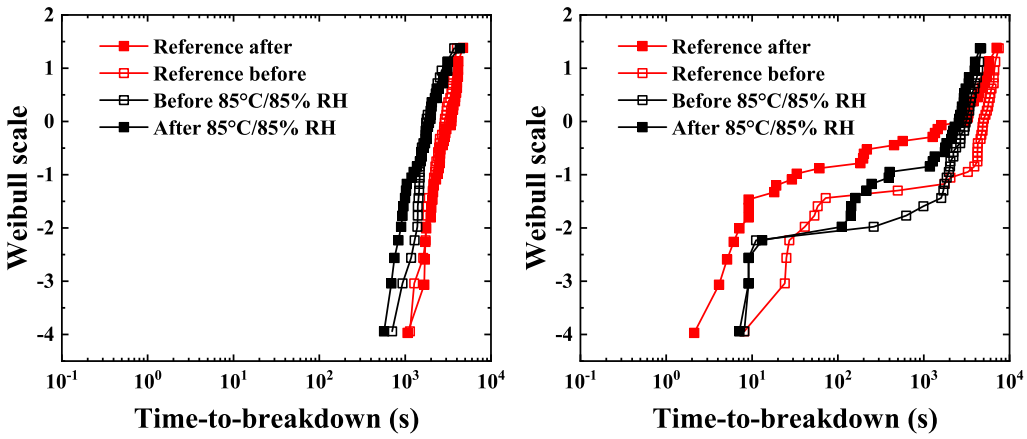


Figure 4.2: Methodology applied on test and reference wafers.

4.2.2.2 Results for different atmospheric conditions

Using the methodology represented in figure 4.2, a common climatic condition [140], [139] has been assessed and compared to storage at room condition: 85°C/85% Relative Humidity (RH), at atmospheric pressure. Figure 4.3.a presents the results for protected structures. As one can see, there is no degradation of the Weibull distribution for any of the considered wafers meaning that the seal-ring remains efficient under this climatic condition. To the contrary, figure 4.3.b exhibits important differences between Weibull distributions obtained on unprotected test structures before and after THB. Indeed, despite the fact that the higher time-to-breakdown values measured after the THB seem to be very similar to those measured before (top of the distribution), a significant decrease is observed for approximately a third of the distribution. This observation alone would suggest that the 168 hours 85°C/85% RH storage has accelerated moisture ingress. But, looking more closely to distributions of the reference wafer discredits this idea as it presents stronger distributions degradation after the same 168 hours of storage than at room conditions. Consequently, the 85°C/85% RH storage is not an appropriate moisture ingress acceleration methodology.

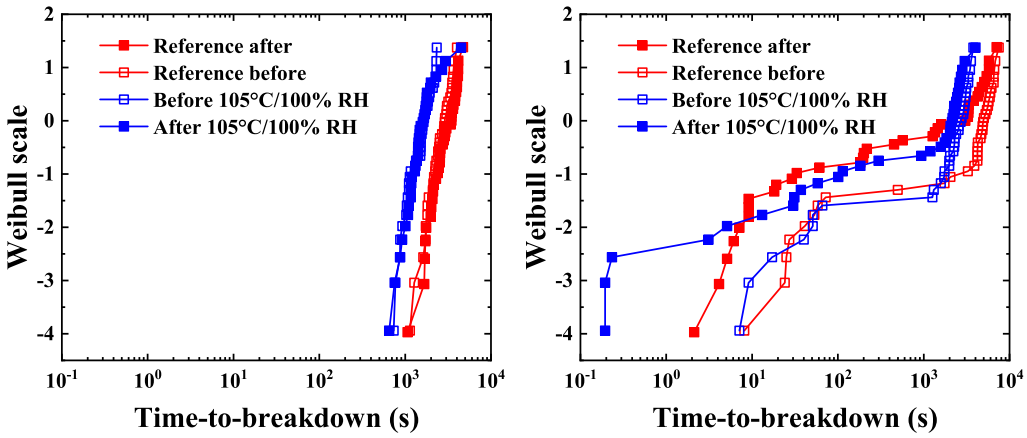


(a) Time-to-breakdown Weibull distributions of protected test structures before and after 168h of storage at controlled conditions.

(b) Time-to-breakdown Weibull distributions of unprotected test structures before and after 168h of storage at controlled conditions.

Figure 4.3: Effect of 168h of storage at 85°C/85% RH compared with room conditions.

As a result, a more aggressive climatic condition has been tested: 105°C/100% RH unsaturated under twice the atmospheric pressure (2 bars), which is also a common climatic storage condition in the industry [141]. The results of 168 hours of storage in the aforementioned conditions together with reference wafers are shown in figure 4.4. Similar reasoning than for the previous climatic condition results lead to similar conclusions: Weibull distributions after 168 hours of respective storage exhibit very similar time-to-breakdown degradations (figure 4.4.b). As a result, we conclude that 168h of storage at 105°C/100% RH unsaturated under twice the atmospheric pressure is not an efficient moisture-related ageing acceleration methodology.



(a) Time-to-breakdown Weibull distributions of protected test structures before and after 168h of storage at controlled conditions.

(b) Time-to-breakdown Weibull distributions of unprotected test structures before and after 168h of storage at controlled conditions.

Figure 4.4: Effect of 168h of storage at 105°C/100% RH and 2 atmospheric pressure compared with room conditions.

Unfortunately, none of the tested conditions, summarized in table 4.1, allowed to accelerate moisture ingress in unprotected test structures compared to room condition storage which confirms that stressful climatic biases are not suitable to accelerate moisture ingress. Such inability to accelerate moisture ingress is unexpected and additional experiments have been carried out to understand it.

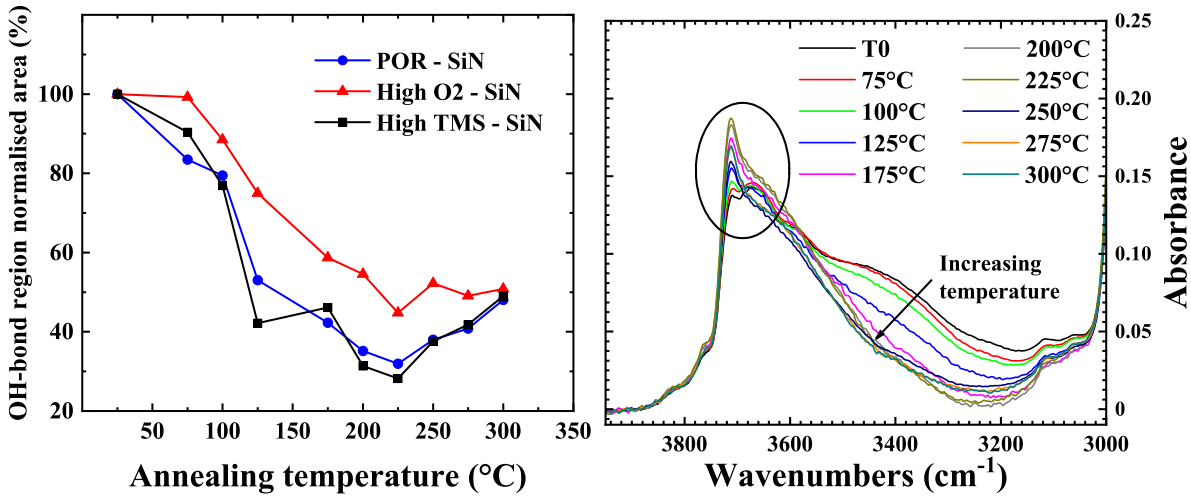
Temperature (°C)	Relative Humidity (%)	Saturated humidity
85	85	N/A
85	95	N/A
105	100	No
120	100	No

Table 4.1: Unsuccessful moisture ingress acceleration climatic storage conditions.

4.2.3 Material considerations

In order to understand the inability to accelerate moisture ingress in the BEOL, it is necessary to study the thermal sensitivity of moisturised blanket SiOC:H low-κ dielectric material. As already done in section 2.5.4.3, the MIR infra-red characterisation technique, allows to observe the evolution of the moisture content over time. Thus, the same blanket wafers *i.e.* exposed to moisture thanks to 497 days of storage under room condition, are used (see section 2.5.4) to estimate the effect of temperature on moisture contained in the SiOC:H material. One hour anneals have been performed at increasing temperatures, by steps of 25°C, from 75°C to 300°C. After each anneal, the moisture content is estimated by peak area integration similarly to the experiment in section 2.5.4.3. Figure 4.5.a presents the evolution of moisture-related peak area between two successive temperatures. In this manner we observe the effects of anneals on moisture quantity present in the material. After the first anneal, at 75°C, a decrease of the moisture content is observed, in particular for the POR SiOC:H material. As the temperature increases, the moisture content clearly decreases until reaching a minimum at 225°C. The decrease of the moisture content seen between the anneal at 75°C and the anneal at 125°C explains why the climatic storage conditions used in section 4.2.2.2 failed to accelerate moisture ingress in our test structures. The small increase observed from 225°C to 300°C is unexpected and requires a precise look at MIR spectra to be understood. Indeed, looking closely at spectra displayed in figure 4.5.b reveals a more complex effect of the anneal on the moisture present in the SiOC:H material. In this analysis, two different wavenumber ranges can be distinguished: a sharp peak at 3700 cm $^{-1}$ (circled), corresponding hydroxyl groups bonded to the SiOC network and isolated referred as free -OH bond stretching by Knop *et al.* [142], and a broader peak from 3200 cm^{-1} to 3500 cm^{-1} corresponding to hydrogen-bonded hydroxyl groups interacting with each other [142]. Before the successive anneals, the broad peak is maximal and decreases strongly until after the 1 hour-long 225°C anneal. In the meantime, the sharp peak increases and reaches its amplitude maximum at the same temperature while its width is also slightly increasing. After anneals at temperatures higher than 225°C, the sharp peak amplitude decreases while the broad peak remains stable. However, even after the 300°C anneal, the sharp peak previous increase is not fully recovered and thus, the moisture content is not completely desorbed

which indicates that some hydroxyl groups are still very strongly bonded to the material. This suggests that high temperature anneals, further than only partly desorbing moisture, might also modify the kind of moisture in the SiOC:H dielectric material. However, it is theoretically inaccurate to draw moisture content by simple peak amplitude comparison as the sharp peak is the result of a very small fraction of the moisture, with a strong vibration amplitude while the broad peak is induced by an important amount of moisture with a weak vibration amplitude. To this extent, the sharp peak analysis is interesting for material understanding purposes but the moisture inducing the broad peak is more likely to have a more significant influence on the material electrical properties and performances.



(a) -OH bonds region normalised area evolution after respective 1 hour anneals at increasing temperatures.

(b) MIR absorption spectra after respective 1 hour anneals at increasing temperatures.

Figure 4.5: Effect of increasing the anneal temperature on the moisture content and moisture-related absorption bands.

As a consequence, this MIR analysis, brings evidence to the fact that THB stress attempts in section 4.2.2.2 cannot succeed as temperatures used are too high to incorporate moisture in the SiOC:H dielectric material. Alternatively, this experiment helps understand why time-to-breakdown distributions of unprotected test structures shown in section 4.2.2.2 were not fully recovered. As a result, in the following of this work, moisture ingress is the result of waiting time at room conditions, which in turn constrains the number of experiment that can be conducted on a given period of time and preclude important statistic gathering.

4.3 SiOC:H time-to-breakdown

As suggested in section 1.5.3.4, time-to-breakdown is the main parameter to observe when assessing the SiOC:H dielectric reliability as neither leakage current nor capacitance value does correlate accurately with time-to-breakdown, hence dielectric lifetime. Therefore, it is necessary to deeply study the time-to-breakdown and its dependencies in order to spot eventual moisture-induced modifications.

4.3.1 Intrinsic SiOC:H

First of all, the unpolluted SiOC:H dielectric reliability must be assessed in order to serve as a comparison reference to evaluate the effect of moisture on the dielectric reliability, in particular on the time-to-breakdown.

4.3.1.1 Electrical field dependence

One of the main aspects to be assessed is the unpolluted SiOC:H dielectric material electrical field dependence of the time-to-breakdown. This has partly been discussed in the section 1.4.3, detailing the main models used for lifetime estimation. Reliability data is extracted from CVS Weibull distributions plots presented in figure 1.18.b of section 1.4.2. As one can note, the three models described in section 1.4.3 seem to fit accurately the data, however an analysis of the fit quality is required to determine which model fits best with our data.

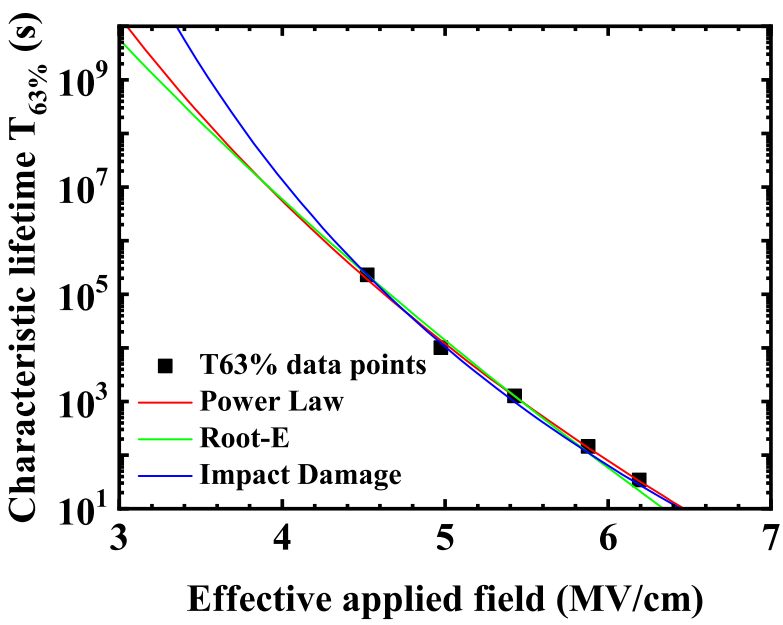


Figure 4.6: Median times-to-breakdown at different electrical fields along with the Root-E (R-E), Power Law (PL) and Impact Damage (ID) models respective trends.

Hence, these models have been fitted to experimental time-to-breakdown value at 0 in a Weibull scale $W(0)$ corresponding to $T_{63\%}$ of time-to-breakdown, using two methods: increasing the number of fitted points from higher to lower fields (backward fitting) or from lower to higher fields (forward fitting). Whatever the fitting method, R^2 analysis reveals important R^2 degradation for PL and R-E models, while the ID model is found to be the best fit across the whole range of fields without any R^2 degradation (figure 4.7). Thus, we confirm the conclusion from Muralidhar *et al.* that the ID model is the most accurate to extrapolate $T_{63\%}$ at actual product fields using high fields data [58].

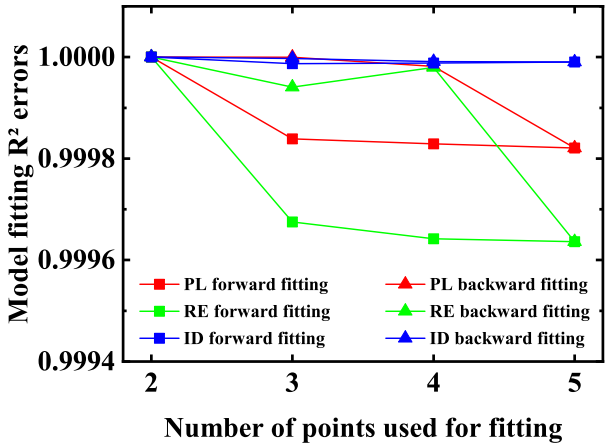


Figure 4.7: R^2 values for Root-E (R-E), Power Law (PL) and Impact Damage (ID) models with backward and forward fitting.

4.3.1.2 Serpentine length dependence

In the same manner, it is also important to evaluate the effect of the C/S/C structure length (see section 3.3 for structure details). The main yield model used for area scaling is the Poisson model, which has been extensively used for thin oxides [143], [144], [145], [146]. The so-called Poisson yield model supposes that the defect rate generation is constant over time and defects are independent from each other, which might seem to apply to interconnect reliability *a priori*, but defect clustering does occur in photolithographic field [147] where the fabrication induces non uniform defect distribution for instance [148], [149]. Indeed, previous literature have shown that very poor CVS reliability data might result in non-Poisson distributions, especially for advanced technology nodes interconnects [150], [151], [147]. This results in fact in what is called a compound Poisson model, which consists in the sum of uniform Poisson distributions [149], [152] :

$$P(k) = \int_0^\infty \frac{\lambda^k}{k!} e^{-\lambda} f(\lambda) d\lambda \tag{4.1}$$

In which the probability to have k fatal defects $P(k)$ is a function of the fatal defect density λ and $f(\lambda)$, the defect density mixing function. This defect density function can be expressed as:

$$f(\lambda) = \frac{b^a \lambda^{a-1} e^{-b\lambda}}{\Gamma(a)} \tag{4.2}$$

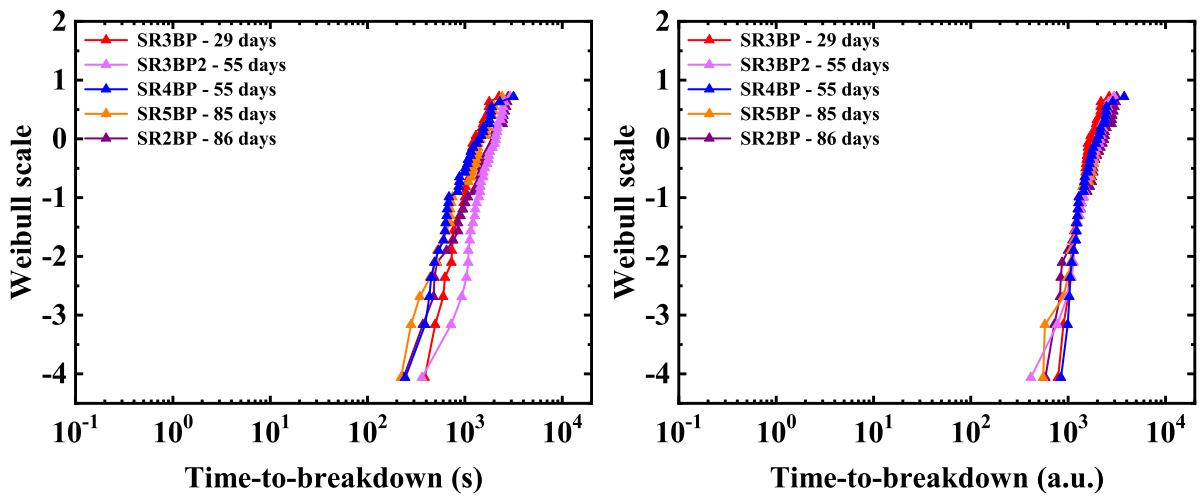
Where a, b are positive numbers and $\Gamma(a)$ is the Gamma function. Injecting equation 4.2 in equation 4.1 gives:

$$P(k) = \int_0^\infty \frac{\lambda^k}{k!} e^{-\lambda} f(\lambda) d\lambda = \frac{\Gamma(k+a) b^k}{k! \Gamma(a)(1+b)^{k+a}} \tag{4.3}$$

This expression is also known as the negative binomial distribution [149], [152]. In our case, it is considered one defect is sufficient to degrade the yield, hence k is taken to 0, which gives:

$$P(0) = \frac{1}{\left(1+\frac{1}{b}\right)^a} = \frac{1}{\left(1+\frac{A.D}{\alpha}\right)^\alpha} \tag{4.4}$$

Where $A.D = \frac{a}{b}$ and $\alpha = b$ with α known as the cluster parameter and having an important impact on the lifetime extracted by the area scaling model. In fact, as shown by Shen *et al.* and Chen *et al.*, neglecting the clustering in lifetime extrapolation leads to failure underestimation, which is not acceptable from an industrial point of view [147], [149]. However, $f(\lambda)$, the defect density mixing function, is hardly determined in practice [149], because consequence of the multiple fabrication steps, making area-scaling extrapolation very difficult to achieve. Nonetheless, one of the main Weibull distribution properties is to be invariant by lateral and vertical shifts in a Weibull scale, implying the shape parameter, β, to be area independent. This allows to determine the activated area of a Weibull distribution by measuring the required shifts to overlap the distribution with a known area, a method referred as Shift & Compare by Chen *et al.* [149]. Consequently, this aspect is to be explored as moisture might have an effect on the compliance of the studied interconnect test structures on the shape parameter invariance. Figure 4.8.a underline the fact that despite C/S/C variations from 40.3 cm to 384.4 cm, the time-to-breakdown varies only a little, in other words, their Weibull distributions are very close to each other. Shape parameters for different protected C/S/C structure lengths are, 2.2, 3.07,3.14, 2.1 and 2.1 for SR2BP, SR3BP, SR3BP2, SR4BP and SR5BP respectively. Despite the fact that there is some variation, no correlation is observed between C/S/C length and β values. Variations of β values is probably due the weak statistic used in our experiment, only 37 sites per structure. Moreover, the Shift & Compare method has been used in figure 4.8.b, in which different distributions can be superposed very closely. This confirms the aforementioned property of the Weibull shape parameter. However, due to the differences of shape parameter values and the absence of correlation between β and the C/S/C length, we cannot conclude if the area scaling of our protected test structures follows a Poisson distribution or if a compound Poisson distribution is needed.



(a) Weibull plots of time-to-breakdown for different protected C/S/C structure lengths.

(b) Superposition of Weibull plots of time-to-breakdown for different protected C/S/C structure lengths.

Figure 4.8: Weibull plots of time-to-breakdown for different C/S/C structure lengths.

4.3.2 Moisture ingress effect

As already mentioned in section 1.5.3.3, moisture ingress induces a decrease of the time-to-breakdown during CVS. This effect is confirmed by figure 4.9 when compared with protected structures (see figure 4.8.a) in which strong differences are observed between unprotected structures with different C/S/C length. However, there is no clear correlation between mean time-to-breakdown and C/S/C length. For instance, structures S2BP and S5BP have similar mean time-to-breakdown but C/S/C length varying from 40.3 cm to 384.4 cm respectively while S3BP, S3BP2 and S4BP structures have intermediate C/S/C length but higher mean time-to-breakdown. To the contrary, time-to-breakdown decrease seems to correlate with time elapsed since the end of the wafers fabrication. This is due to the fact that CVS tests are hardly performed at the same moment, on the same wafer, for every die on the wafer. Even, the test duration itself induces a bias as moisture continue to diffuse in unprotected test structures during the test. Moreover, the lack of an efficient acceleration methodology of wafer level moisture ingress prevents any saturation of moisture in the SiOC:H material to avoid the effect of the cumulative wait time between two tests. Therefore, for unprotected structures, the later the test is performed, the wider the distribution and the lower the mean time-to-breakdown, hiding the effect of the C/S/C structure length. In the light of these constraints, we cannot conclude if moisture affects the C/S/C length scaling property of the time-to-breakdown.

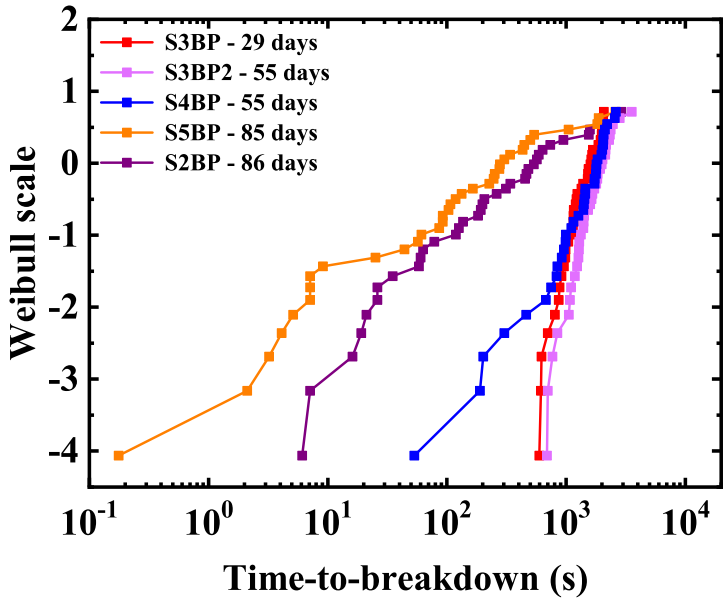


Figure 4.9: Weibull plots of time-to-breakdown for different unprotected C/S/C structure lengths after translation. Days since fab-out are indicated.

Looking at the shape of the Weibull distributions of time-to-breakdown of unprotected C/S/C structures, especially those tested the latest (85 and 86 days), it seems that a clustering model fitting would have been more appropriate. Indeed, unlike the Weibull statistical model that supposes defects are independent one from another, the clustering model brings the idea that once a defect appears, components of the population sharing common attributes, one of these might be spatial proximity for instance, are more likely to experience similar defect. Intuitively, this seems consistent with previous evidence of moisture diffusion though the SiOC:H dielectric material (see section 2.5.4) and would need to be confirmed by further dedicated studies.

4.3.3 Breakdown point localisation

Another important aspect to consider is the breakdown localisation. Indeed, breakdown is supposed to occur randomly in the structure if SiOC:H low-κ-based interconnects obey a perfect Poisson area scaling law [153]. However, as we have seen in section 4.3.1.2, it is not exactly the case, SiOC:H is very sensitive to manufacturing-induced damages [113] (see sections 2.2 and 2.2.7 for more details). Hence, it is interesting to determine the breakdown point to spot eventual localised defects or structure weaknesses which could enhance defect clustering such as line-to-line distance narrowing for instance. Alternatively, study of the breakdown point distribution in presence of moisture could provide information on the explanation of early breakdown mechanism for structures with moisture (see section 4.3.2 for more detail). The immediate solution would be to determine these breakdown points localisations by visual inspections, which is possible during engineering development steps but as it is extremely time-consuming, it is clearly not conceivable in the industry. Moreover, only a fraction of breakdowns is visible optically: when the breakdown-induced damages are tremendous. Furthermore, it is easily confused with dust particles on the wafer surface as shown by figure 4.10 where a breakdown point is visible, marked by a tiny dark spot. Also, such extrusion of the passivation might be hidden by aluminium dummy pattern atop the copper C/S/C structure.

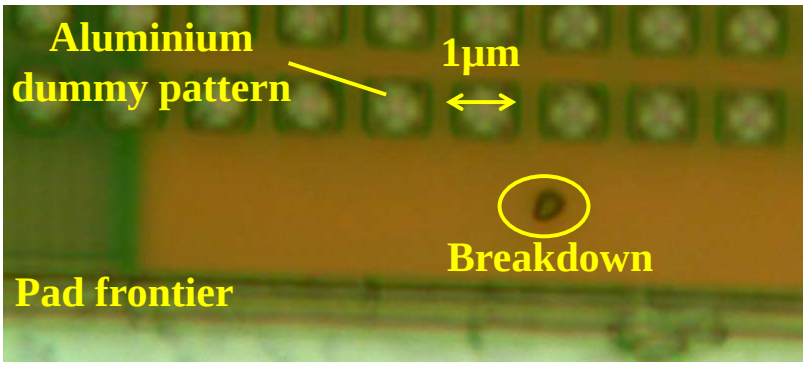


Figure 4.10: Optical inspection showing an extrusion of the upper BEOL layer, consequence of the temperature rise caused by the breakdown.

4.3.3.1 Optical Beam-Induced Resistance Change

Hence, as some breakdown point localisations cannot be verified with sufficient certainty by visual inspection, they have been searched by Optical Beam-Induced Resistance CHange (OBIRCH) (figure 4.11). This technique is also time-consuming but offers much better certainty than visual inspection as it localises the breakdown point by biasing the structure to monitor its resistance while a laser beam is scanning the wafer surface. When the laser beam hits the polarised structure area, the resistance is decreased, because of a laser-induced temperature increase while nothing happens when it hits an unbiased area. Figure 4.11 is an example where the biased area is highlighted in green.

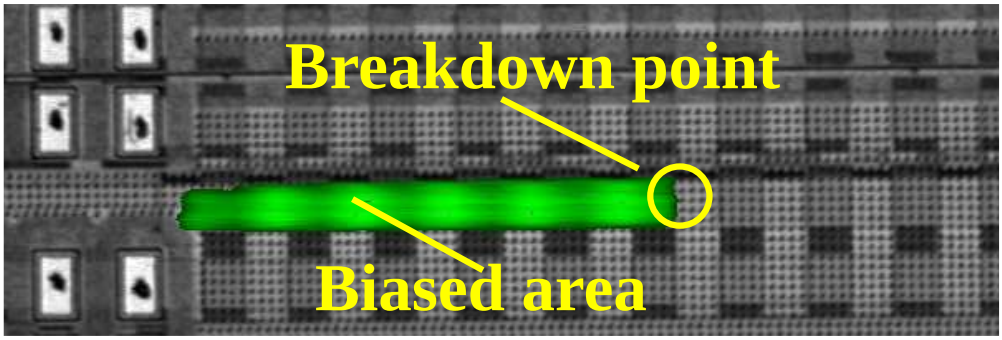


Figure 4.11: OBIRCH polarised area highlighting (green) on a S4BP test structure after dielectric breakdown.

However, this technique has limitations as the line resistance cannot be too high, otherwise the beam-induced resistance change is too small to be detected. Consequently, it might not detect breakdown points for some very long C/S/C structures.

4.3.3.2 Electrical methodology

In order to be able to localise every breakdown point on a short time-scale, we have successfully developed an automatable electrical localisation method which has been applied on reference and wet structures broken by CVS at 60 V. After the CVS test, resistances between pads 1 and 2, R_1, and between 2 and 3, R_2 are measured (figure 4.12). As the serpentine resistance, $R_{SERPENTINE}$, is measured before CVS, location of the breakdown point can be estimated by a simple ratio: $R_1/ R_{SERPENTINE}$ or $R_2/ R_{SERPENTINE}$ which are the location in percent of the total serpentine length from the top (connected to pad 3) or the bottom (connected to pad 1) of the serpentine, respectively.

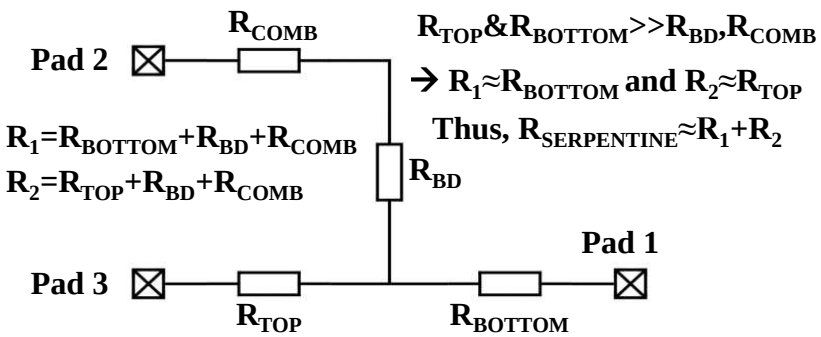


Figure 4.12: Equivalent circuit after oxide breakdown.

To validate the electrical localisations found with our method, time-consuming OBIRCH technique has been used to spot breakdown points. Table 4.2 confirms a good agreement between the electrical method and the OBIRCH technique.

Structure	Electrical localisation	OBIRCH localisation
Reference	8	9
	8	6
	14	11
	30	31
	27	28
	4	3
	8	10
Wet	4	4
	12	9
	41	40
	14	14
	26	27
	27	25
	53	53

Table 4.2: Breakdown point bloc number for both localisation methods.

With this electrical methodology, a comparative study has been conducted to spot eventual differences between wet test structures polluted by moisture (S4BP) and references which are not (SR4BP). Figure 4.13 summarises the obtained results. One can underline the fact that the breakdown point localisation as a function of the test structure length percentile is fairly constant. In other words, despite slightly more breakdown points localised in the first and last 15% of the structure length, the breakdown points location is distributed with an equal probability throughout the structure, which suggests a Poisson breakdown point distribution and further confirms the use of compound Poisson distributions detailed in section 4.3.1.2. Apart from this possible slight effect at the edges of the structures, which is consistent with metallic density changes at the edges of the structures leading to inherent fabrication variability, especially for CMP, this nearly

uniform distribution of the breakdown point localisation confirms that there is no significant detrimental CAD or fabrication-induced defects favouring the breakdown at a very specific location in the structure. As a consequence, it is experimentally valid to study breakdown mechanisms in such structures.

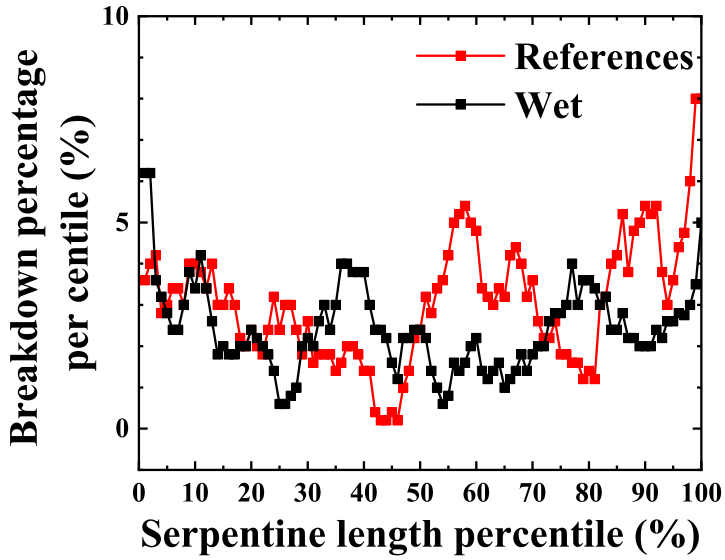


Figure 4.13: Breakdown point location percentage as a function of structure length percentile.

4.4 Breakdown mechanisms study

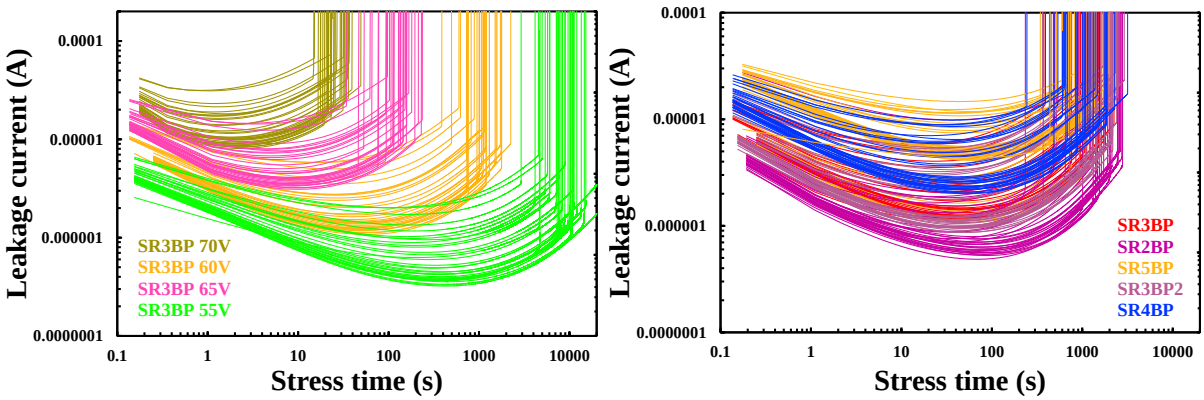
As no precise material modification information can be gathered from times-to-breakdown or other associated parameters such as leakage current or capacitance for instance (see section 4.3 for more details), neither from the breakdown localisation (section 4.3.3), it is necessary to study the behaviour of wet SiOC:H low-κ dielectric under electrical stress. In order to achieve this, usual characterisation techniques described in section 1.4.2 are employed jointly on test structures polluted and unpolluted by moisture to allow a comparative study.

4.4.1 Constant Voltage Stress (CVS)

One of the main characterisation techniques for dielectrics, CVS (see section 1.4.2.3 for more details), is used mostly to extract times-to-breakdown but discrete leakage current measurements, needed to detect the breakdown, also provide data on the evolution of the conduction during stress. Consequently, a comparative study might put in light divergences of behaviour induced by moisture under a constant electrical stress by the analysis of leakage current evolution as function of time, referred as I-t.

4.4.1.1 I-t of unpolluted SiOC:H

In order to gather information about unpolluted SiOC:H, leakage current evolution has been measured during CVS at different voltages (figure 4.14.a), and on different C/S/C structure lengths (figure 4.14.b). As one can note from figure 4.14.a, except the vertical shift of the I-t curves and breakdown times differences due to the increase of the stress voltage, two steps can be distinguished on all curves : the negative charges trapping, resulting in the leakage current decrease before increasing when entering in the degradation step in which defects are generated in the material. This observation implies that behaviours are very similar for all test voltages. Similarly, the absence of discrepancies between different C/S/C structure lengths in figure 4.14.b underlines the fact that they behave in the same manner, which sets aside significant fabrication defects.



(a) Leakage current evolution during CVS tests at different electrical fields.

(b) Leakage current evolution during 60V CVS tests performed on different C/S/C structure lengths.

Figure 4.14: Leakage current evolution during CVS tests of unpolluted test structures.

4.4.1.2 I-t of SiOC:H polluted by moisture

Similarly, leakage current evolution under CVS on moisturised test structures has been measured. Figure 4.15 underlines the fact that moisturised test structures breakdown is susceptible to occur on a very wide range of time as already seen in section 4.3. Moreover, as already mentioned in section 1.5.3.4, one cannot see a specific signature as the breakdown seems to occur without any correlation with initial leakage current (first point of the curve), leakage current or other parameters. However, it can be noted that many moisturised test structures break while the leakage current is decreasing, which is an important difference with respect to protected test structures (figure 4.14). This is particularly interesting as it suggests that moisturised test structures do not obey to the same degradation and breakdown mechanisms.

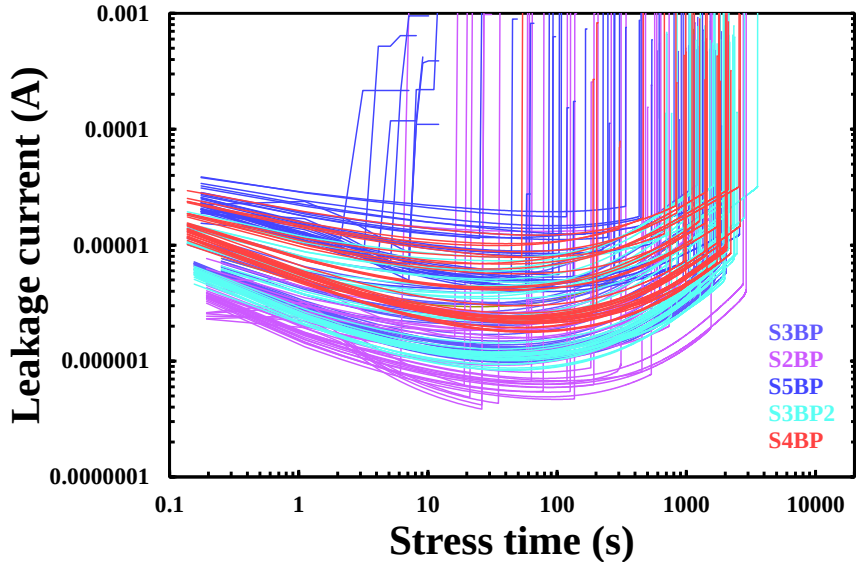


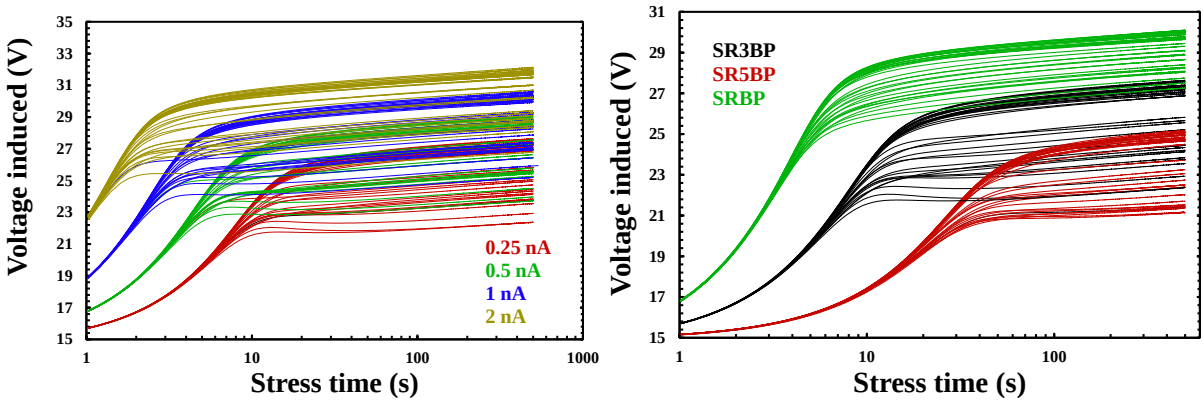
Figure 4.15: Leakage current evolution during 60 V CVS tests of moisturised test structures.

4.4.2 Constant Current Stress (CCS)

Another widely spread characterisation techniques has been employed: CCS. Despite the fact that it allows to extract time-to-breakdown similarly to CVS, it also permits to observe conduction barrier height in a more direct way. Indeed, instead of measuring the leakage current, in CCS the voltage is measured (see section 1.4.2 for more details). Because voltage can be seen as a meaningful image of electrons energy, its follow-up during CCS stress might help underline different breakdown mechanisms between unpolluted and polluted test structures.

4.4.2.1 V-t of unpolluted SiOC:H

Figure 4.16 exhibits the V-t curves measured during CCS at different currents and on test structures having different C/S/C lengths. At the beginning of V-t curves, voltages strongly increase until they reach an inflexion point after which they increase at a lower rate suggesting negative charges injection in the dielectric material resulting in barrier height raising. Then, a maximum is reached, at different times depending on the stress current, before a decrease of the applied voltage when the SiOC:H dielectric material enters the degradation phase. Figure 4.16.a highlights the fact that the evolution of voltages during CCS is very similar from one stress current to another, apart from the obvious increase of the voltage with increasing stress current, suggesting that the degradation mechanisms do not change in our range of currents. Furthermore, similar curves in figure 4.16.b indicates that all C/S/C structures lengths behave equivalently. This information suggests that the degradation mechanism leading to dielectric breakdown is not strongly dependent on the C/S/C structure length.

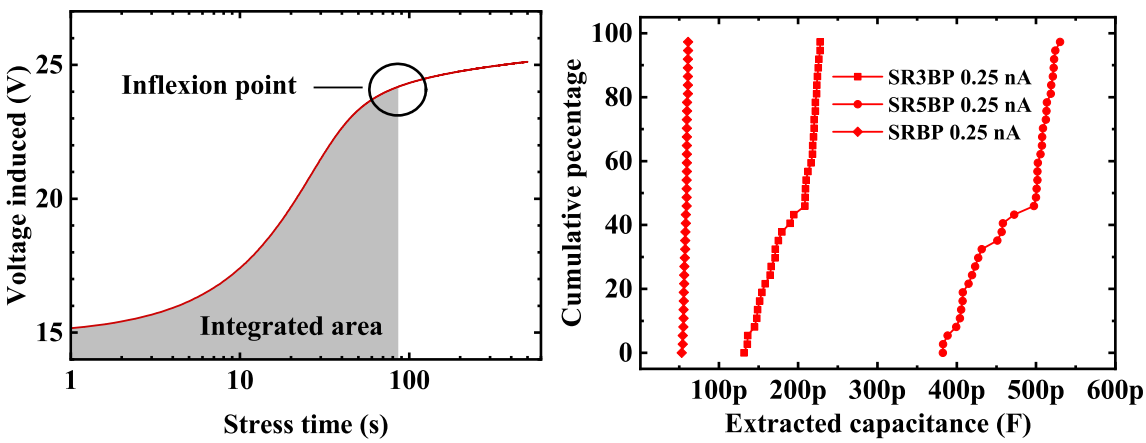


(a) Voltage evolution during CCS tests on SR3BP structures at different forced currents.

(b) Voltage evolution during 250 pA CCS tests performed on different C/S/C structure lengths.

Figure 4.16: Voltage evolution during CCS tests of unpolluted test structures.

As the steep voltage increase at the very beginning of the V-t curves is shorter for higher stress currents, it could correspond to the structure capacitance being charged at the beginning of the stress. In order to verify this hypothesis, equivalent capacitances have been extracted from integration of the area under the curves (figure 4.17.a). Figure 4.17.b allows to confirm that distributions of equivalent capacitances roughly correspond to the structure typical capacitance values measured before CCS that are 188, 65 and 550 pico-Farads for SR3BP, SRBP and SR5BP respectively. The extract relative imprecision is due to the CCS measurement step precision as well as the imprecision when extracting the inflexion point. Hence, we have confirmed that the peculiar slope change at the beginning of V-t curves is a measurement artefact and should not be considered to study SiOC:H dielectric material properties.



(a) Example of integration of CCS curve on a SR5BP test structure from figure 4.16.b

(b) Distributions of equivalent capacitances for different C/S/C structure lengths.

Figure 4.17: Equivalent capacitance integration from CCS measurements.

4.4.2.2 V-t of SiOC:H polluted by moisture

In the same manner, V-t characteristics have been measured on unprotected test structures. Figure 4.18 presents a set of CCS measurements at various stress currents. Straight away, it is clear that unprotected structures exhibit very different behaviour than protected ones (presented in figure 4.16). Indeed, apart from the fact that breakdown times are very dispersed the voltage induced by the forced current decreases, before it increases again, making the V-t curve visually wavy. This occurs at every stress current with similar amplitude between the V-t local minimum and its maximum, suggesting the appearance of such phenomenon is activated neither by the electrical field, nor the stress current.

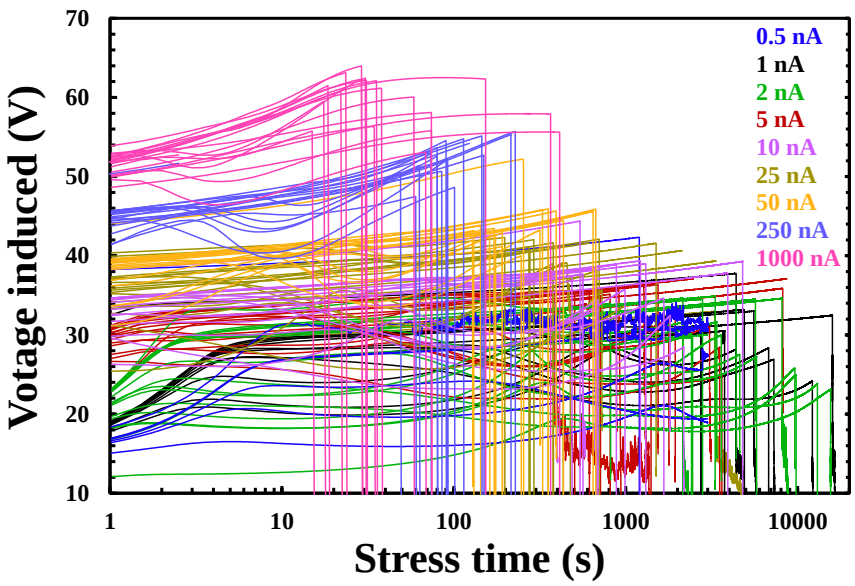


Figure 4.18: Voltage evolution during CCS tests at different currents performed on unprotected test structures.

As this peculiar V-t signature for some of the structures does not seem to be activated by the stress parameters at ambient temperature, similar experiments have been carried out on temperatures ranging from -40°C to 50°C. CCS tests at temperatures higher than 50°C have not been performed because they would probably induce a moisture desorption (see section 4.2.3 for more details). As shown in figure 4.19 the waves amplitude is notably decreased at 5°C compared with ambient temperature (27°C). This tendency is further confirmed by the waves disappearance at -40°C while their amplitude seems increased at 50°C compared to 27°C. Hence, these results undoubtedly point towards a temperature activated phenomenon whose the physical root-cause remains unclear and unpredictable as some of the structures do not present waves, even at 50°C.

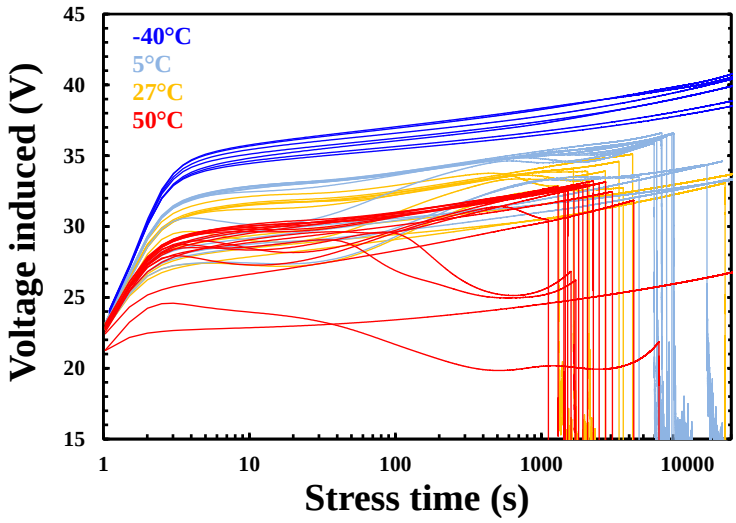


Figure 4.19: Voltage evolution during CCS tests at 2nA at different temperatures performed on unprotected test structures.

4.4.3 SiOC:H material considerations and consequences

Differences observed in sections 4.4.1, and 4.4.2 underline different breakdown mechanisms because of moisture presence in the SiOC:H dielectric material. In particular, section 4.4.2 has shown that some of the moisturised test structures exhibits peculiar behaviours during CCS tests with the appearance of what we have called waves in V-t curves. The fact that the number and the amplitude of these waves seems to be strongly dependent on temperature suggests the moisture-related breakdown underlying phenomenon also strongly depends on temperature. This could be the result of changing conduction and degradation mechanisms in moisturised test structures. This variation of the voltage could also be seen as a modulation of the barrier height, suggesting charges movement in the dielectric during stress. As a consequence, a more detailed analysis of the conduction mechanisms is required to understand such peculiar behaviours and its relation with conduction in the SiOC:H low-κ dielectric. In the same manner, the potential presence of mobile charges will be addressed in section 4.5.4.

4.5 Conduction mechanism(s)

In the scope of our study, it is particularly interesting to study conduction mechanisms though SiOC:H material as moisture affects its electrical performances (see sections 4.3 and 4.4) and thus, it is likely it also influences the conduction mechanisms.

4.5.1 Static leakage current analysis

In order to analyse the SiOC:H material conduction mechanisms, it is required to determine leakage current values under a range of electrical field. This type of information is retrieved from straightforward I-V characterisation, succinctly described in section 1.4.2.1, carried out on seal-ring protected structure. Resulting characteristics, presented in figure 4.20, show that only the first characteristic is different from the later ones (2, 3

and 4), which can be explained by charges trapping occurring in the material during the first measurement (more details in section 4.5.5) in agreement with the negative charge trapping seen during CVS measurements. Then, successive characteristics are identical, showing that the test structure electrical behaviour is stable from one measurement to another, which is necessary for a reliable conduction mechanism study as this allows the same test structure to be characterised under a wide range of conditions.

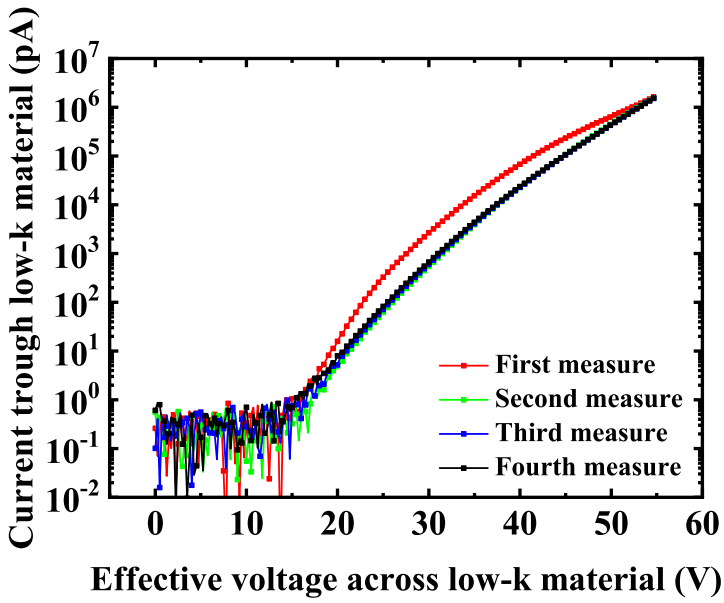


Figure 4.20: Successive I-V characteristics from a SR3BP test structure.

4.5.2 Schottky Emission and Poole-Frenkel tunnelling

It is generally accepted that, considering the relatively low electrical field across the SiOC:H dielectric material in structures, the conduction through SiOC:H dielectrics is identified to be whether Schottky thermionic Emission (SE) or Poole-Frenkel trap-assisted tunnelling (PF) [54]. Despite the fact that these conduction mechanisms have very different physical explanations, the mathematical expressions of their respective current densities are very similar. Indeed, the SE is described by:

$$J_{SE} = A^{*}.T^{2}.exp\left(q\frac{\beta_{SE}.E^{\frac{1}{2}} - \phi_{SE}}{k_B T}\right) \tag{4.5}$$

Where A^* is the Richardson constant, T the temperature, k_B the Boltzmann constant, E the electrical field, q the electronic charge, ϕ_{SE} the PF barrier height and β_{SE} a constant defined by:

$$\beta_{SE} = \left(\frac{q}{4.\pi.\epsilon_0.\epsilon_r}\right)^{\frac{1}{2}} \tag{4.6}$$

Where q is the electronic charge, and ϵ_0 and ϵ_r the free space permittivity and dielectric relative permittivity respectively. Also, it must be noted that, as its name suggests, SE is strongly dependent on temperature. While Poole-Frenkel trap-assisted tunnelling (PF)

mechanism can be expressed as:

$$J_{PF} = \sigma_0.E.exp\left(q\frac{\beta_{PF}.E^{\frac{1}{2}} - \phi_{PF}}{k_B T}\right) \tag{4.7}$$

Where T is the temperature, k_B the Boltzmann constant, E the electrical field, q the electronic charge, ϕ_{PF} the PF barrier height and β_{PF} a constant defined by:

$$\beta_{PF} = \left(\frac{q}{\pi.\epsilon_0.\epsilon_r}\right)^{\frac{1}{2}} = 2\beta_{SE} \tag{4.8}$$

Where q is the electronic charge, and ϵ_0 and ϵ_r the free space permittivity and dielectric relative permittivity respectively.

Equations 4.5, 4.7, 4.6 and 4.8 indicate that if the current is induced by SE mechanism, $\ln(J)$ should have a linear dependence on $\sqrt{E}$, while it should be $\ln(J/E)$ if the current is induced by PF mechanism. However, figure 4.21, which plots a typical example of the stabilized I-V characteristics measured and fitted on the voltage range where current is not impacted by noise *i.e.* when it is higher than 5 pA, indicates that both dependence can be assumed and thus, we cannot discriminate whether SE or PF conduction applies. Nonetheless, because I-V characteristics are very well-fitted across the full range of voltages, the conduction mechanism (whether it is SE or PF) is found to be unique. This observation remains valid on temperature ranging from 25°C to 65°C as underlined by the very good R^2 values for both SE and PF plots.

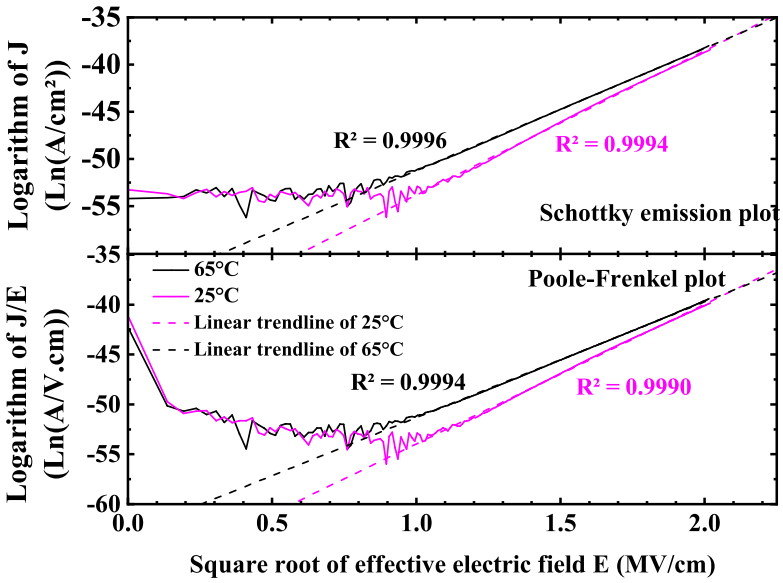


Figure 4.21: SE and PF fitting plots.

Also, equations 4.5, 4.6, 4.7 and 4.8 indicate that if the current is induced by SE mechanism, $\ln(J/T^2)$ should have an activation energy proportional to $\sqrt{E}$, while it should be $\ln(J)$ if the current is induced by PF mechanism. However, apparent activation energy extracted for SE and PF mechanisms has not a linear dependence on the square root of the effective electric field, and thus, it does not help to discriminate the underlying

conduction mechanism (figure 4.22). Nonetheless, it is worth noting that the apparent activation energy increases from 0.1 electron-Volts (eV) or less to more than 0.4 eV as the effective electric field is decreased from 2.1 Mega-Volts (MV) per centimetre to 1.4 MV per centimetre *i.e.* when the effective voltage across the low-κ dielectric decreases from 55 V to 25 V.

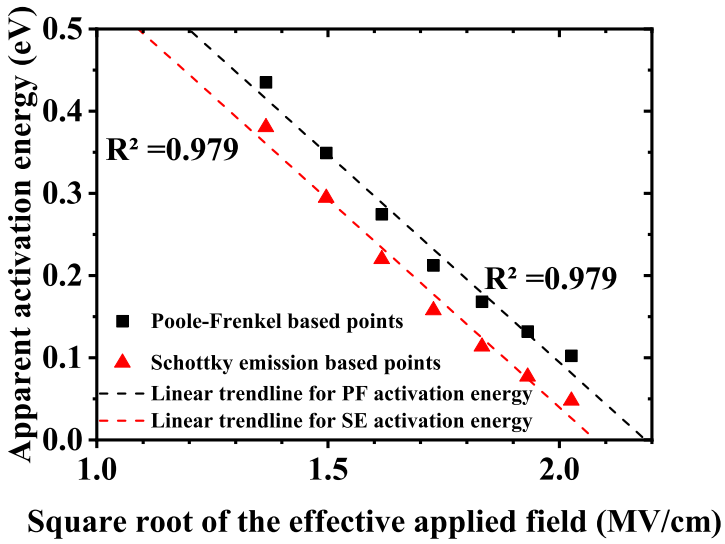


Figure 4.22: SE and PF apparent activation energies.

4.5.3 Moisture influence on conduction mechanisms

Now that conduction mechanisms in unpolluted BEOL test structures have been studied and detailed, similar characterisation procedure on test structures polluted by moisture would allow to determine if, and to what extent, conduction mechanisms change in the presence of moisture in the SiOC:H dielectric material.

4.5.3.1 Electrical analysis

Ideally, reproducing the exact same procedure on wet structures would allow to conclude precisely on the influence of moisture on the conduction mechanisms. However, as shown in figure 4.23, the electrical behaviour in presence of moisture is very different between structures having (SR3BP) or not (S3BP) a protective seal-ring (see section 3.3 for structure details). More specifically, three main aspects make the analysis more complex: firstly, there is no stabilisation in the electrical behaviour of unprotected structures as characteristics are disordered and cross each other which hints for complex and changing conduction mechanisms. Secondly, the occurrence of a hump on the first measure between 20V and 30V, not present on protected structures, points to other types of conduction such as ionic that are hardly pointed by conventional I-V characterisation. Finally, the premature breakdown, despite the fact that previous I-V characterisations were especially limited to a maximum of 35V given the degradation of time-to-breakdown noted in section 4.3, does not allow to realise an important number of I-V characterisations on the same unprotected structure.

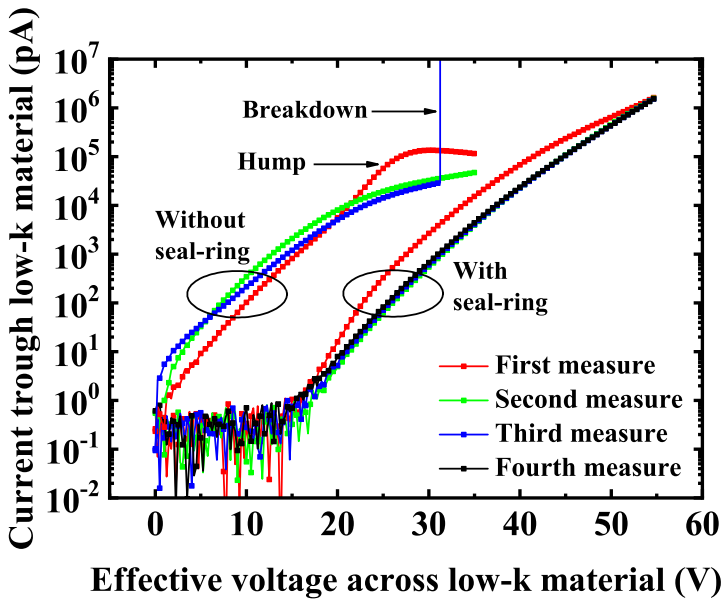


Figure 4.23: Successive I-V characteristics from S3BP and SR3BP test structures (characteristics from SR3BP structures are taken from figure 4.20).

4.5.3.2 Emission Microscopy

Considering the striking changes in conduction mechanisms due to the presence of moisture, it is necessary to ensure that the leakage current is not the consequence of defects in the structure. In order to localise where electrons cross the SiOC:H dielectric material, EMission MIcroscopy (EMMI) is used.

4.5.3.2.1 Working principle

As its name suggests, EMMI is based on detection of light emission from the electrical circuit while it is biased [154]. An EMMI analysis is performed on structures electrically biased and observed with high sensitivity cameras [154]. The choice of the camera, hence the detection spectrum, depends on the hunted phenomenon as shown in figure 4.24. In our study, we aim at detecting photo-electrons originating from atoms constituting the SiOC:H material crossed by the electron flow. Obviously, the EMMI technique is limited by the leakage current levels flowing in the SiOC:H material, thus, by the detection threshold of the camera used.

4.5.3.2.2 Leakage current localisation

EMMI technique has been applied despite the fact that leakage current and hence, electron flow densities in our case are quite low, in the order of fA/μm of serpentine length for a moisturised structure. Firstly, as shown by figure 4.25, it is clear that the current flow through the SiOC:H dielectric material is observable with this technique. To the best of our knowledge, it is the first time that such current flow through SiOC:H dielectric material is reported. Moreover, the quantity of signal depends on the bias voltage, which is consistent with electrical measurement. Indeed, the stronger the voltage, the stronger the current, which thus generates more photo-electrons. Furthermore, this result shows that the moisture-induced leakage current is not located to a specific point in the structure.

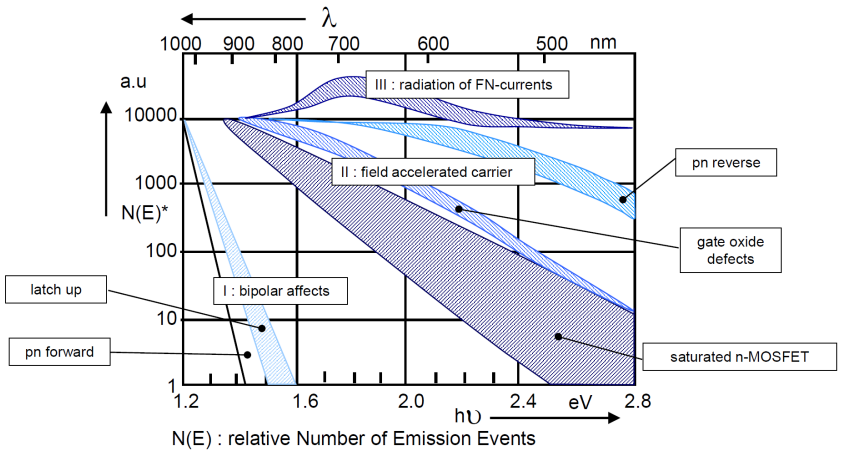


Figure 4.24: Emission sources spectra [155].

Photons are emitted by the whole structure, hence the leakage current increases on the whole structure. This suggests a global material degradation due to a global moisture diffusion and thus, other characterisation techniques should be employed to understand the peculiar I-V characteristics obtained in section 4.5.3.1.

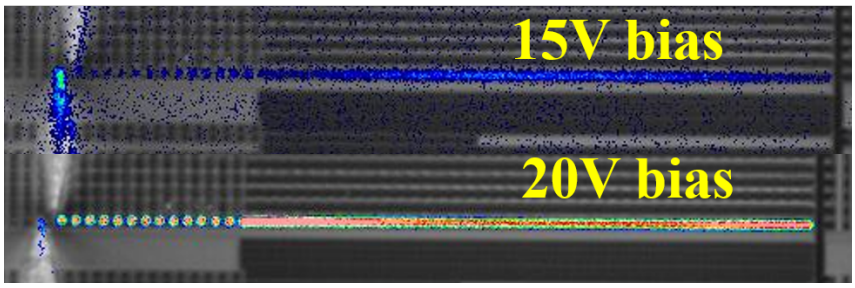


Figure 4.25: Front side EMMI image of a S3BP structure without seal-ring. Indicated bias are applied on the serpentine while the combs are kept to a 0V potential.

4.5.4 Triangular Voltage Sweep (TVS)

The Triangular Voltage Sweep (TVS) technique is a relatively confidential characterisation method, mainly used to detect and study mobile charges in dielectrics [87]. It is equivalent to quasi-static capacitance measurement but offers the advantage to consider both capacitance and conduction mechanisms. As moisture might induce mobile charges in the SiOC:H dielectric material, this technique must be employed to explore this hypothesis.

4.5.4.1 Working principle

TVS, as its name suggests, consists in applying slow voltage analogue ramp to a capacitor during which, the current flowing through the test structure is measured on-the-fly. At every point of the obtained current curve, $I_{Measured}$, the measured current, can be expressed as the sum of the structure leakage current, $I_{Leakage}$, the mobile charges-

induced leakage current, I_{Mobile}, and the capacitor charging,$C.\frac{dV}{dt}$:

$$I_{Measured} = I_{Leakage} + I_{Mobile} + C.\frac{dV}{dt} \tag{4.9}$$

where C is the structure capacitance. In equation 4.9, $\frac{dV}{dt}$ is known as it is the slope of the applied voltage ramp speed. Further than simple comparison of successive characteristics, two different methods can be used in order to extract the mobile charges contribution, prime objective of this characterisation technique.

The first one consists in measuring the static leakage current, $I_{Leakage}$ by I-V characterisations and then subtract it and $I_{Measured}$ at 0V, accounting for the numerical value of $C.\frac{dV}{dt}$, to $I_{Measured}$, which gives:

$$I_{Mobile} = I_{Measured} - I_{Leakage} - C.\frac{dV}{dt} = I_{Measured} - I_{Leakage} - I_{Measured,0V} \tag{4.10}$$

However, this method implies to measure the static leakage current before or after the TVS tests. If it is performed before, it might induce a significant stress-induced degradation on the test structure, in particular for moisturised test structures that are vulnerable to premature failure (see section 4.3 for more details). Indeed, due to the low leakage current to be measured, I-V characterizations involve a relatively long integration time at each voltage and thus, a stress time which might induce a degradation of the moisturised SiOC:H dielectric material, resulting in an increase of the leakage current, known as SILC [72] [156]. Alternatively, measuring the static leakage current after the TVS tests means the moisturised SiOC:H dielectric material has probably been degraded before the I-V characterisation. Because of these limitations induced by I-V characterisation, a second method must be considered. In this method, given the short time of stress induced by TVS, we assume that the structure static leakage current, $I_{Leakage}$, is stable between two successive TVS tests with the same ramp speed, hence only I_{Mobile} varies. As a result, subtraction of two TVS data sets obtained at the same ramp speed and using equation 4.9 allows to eliminate the static leakage current and the quasi-static capacitance contributions. Finally, only the mobile charge contribution change between two TVS tests remains:

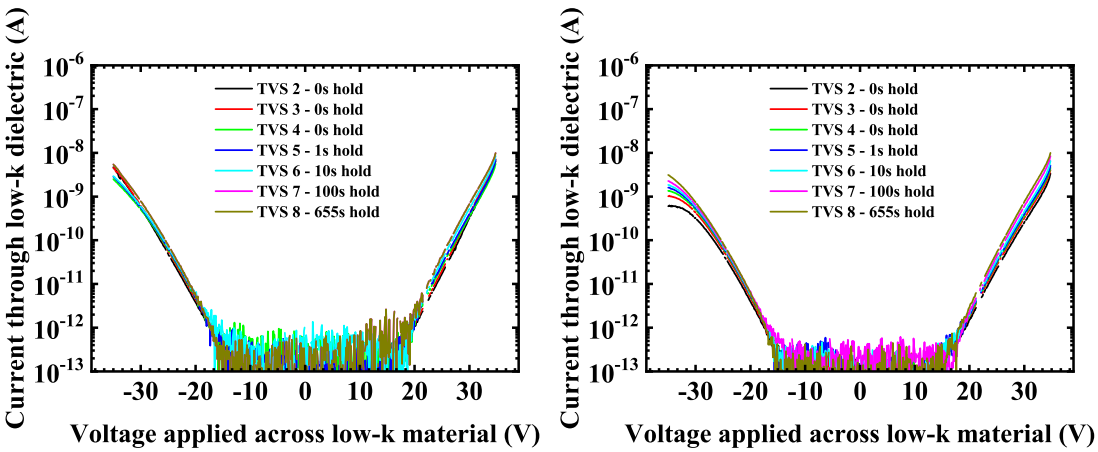
$$I_{Measured2} - I_{Measured1} = I_{Mobile2} - I_{Mobile1} = \Delta I_{Mobile} \tag{4.11}$$

where $I_{Mobile1}$ and $I_{Mobile2}$ are the mobile charges contributions for the first and the second TVS tests respectively. Equation 4.11 describes how it is possible to extract the evolution of mobile charges between successive TVS tests, without needing I-V characterisations. Therefore, in the following of our study, the second analysis methods is preferred to avoid the limitations induced bu I-V characterisations. Moreover, this method is especially interesting to compare and estimate the amount of mobile charges change depending on the hold time applied prior to the TVS test, at the starting voltage of the ramp. In order to understand the possible effect of moisture in such TVS tests, similarly to previous experiments, protected SR3BP test structures are characterised, then used in a comparative study with S3BP moisturised test structures.

4.5.4.2 TVS on unpolluted SiOC:H

TVS tests performed on SR3BP structures at 25°C underline the presence of a leakage slightly higher in the first ramp than in the second one (figure 4.26.a) which is consistent

with previous I-V characteristics (see section 4.20) where some trapping is seen. Moreover, whatever the hold time applied on the structure prior to the voltage ramp, no significant change of the leakage level is observed, meaning the conduction is stable from one characteristic to another, with a leakage current at 15V corresponding to values measured by other characterisations techniques (in the order of $10^{-12}A$) and without noticeable hump in any of the characteristics. But, as previous characterisations put into light a temperature activated mechanism (section 4.4.2), it is necessary to investigate the influence of temperature on the quasi-static response of our protected test structures. Figure 4.26.b underlines that there is no such activation in the 25°C - 60°C temperature range. As a result, no peculiar electrical conduction mechanism is observed on protected structures with the TVS characterisation technique. Because of SiOC:H material moisture desorption at temperatures as low as 75°C (see section 4.2.3 for more details), no higher temperature could be experimented.



(a) TVS characteristics of a SR3BP protected test structure after different hold times at 25°C. Ramp from 35V to -35V at 0.1V/s.

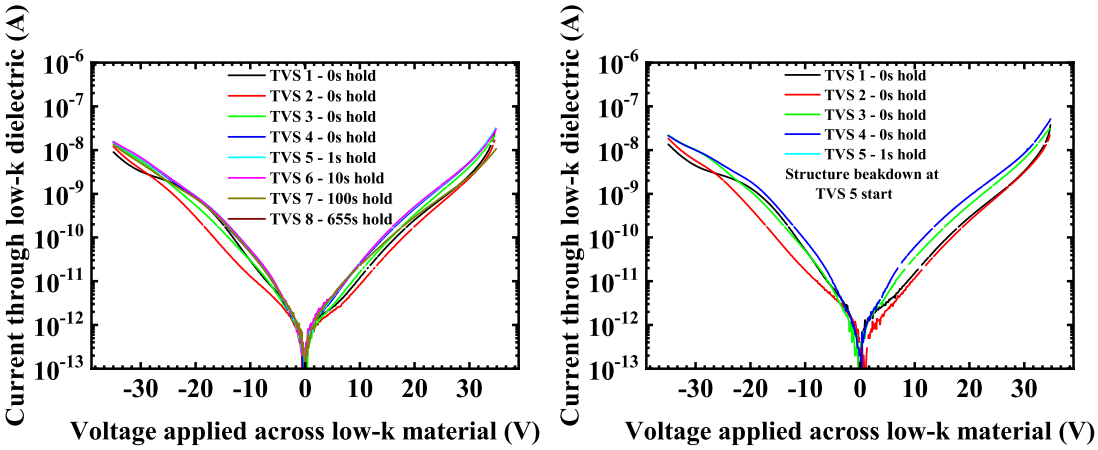
(b) TVS characteristics of a typical SR3BP protected test structure at 60°C after different hold times. Ramp from 35V to -35V at 0.1V/s.

Figure 4.26: Comparison of TVS characteristics of SR3BP structures at 25°C (a) and 60°C (b) after different hold times with a sweep speed of 0.1V/s.

4.5.4.3 TVS on moisturised SiOC:H

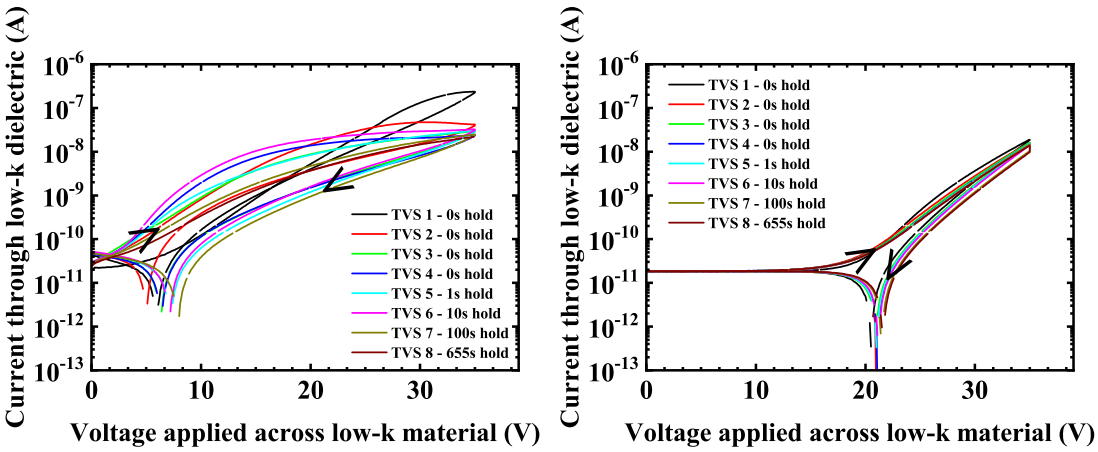
Unlike protected structures (figure4.26), significant differences can be observed between successive TVS measurements carried out at 25°C on unprotected structures. In particular a hump is observed during the first ramp of such leaky test structure, *i.e.* having a leakage current above 1nA at 15V (figure 4.27.a). Apart from the fact that early breakdown occurs on the structure at 60°C (figure 4.27.b) from which it is difficult draw conclusions from considering the very low statistic considered for this study, the presence of a hump is also clearly distinguishable in the characteristics (figure 4.27.b). Despite the whole statistic is not displayed here, the experiment suggested such humps are both more common and of higher amplitude at 60°C. Hence, it seems the occurrence of an important hump during the first characteristic is triggered, or amplified, by the increase of temperature, which is consistent with temperature-activated waves amplitude observed

in CCS tests in section 4.4.2. Furthermore, it is interesting to note that double sweeps, *i.e.* when a second ramp is applied in reverse direction to go back to initial voltage, confirms that the first characteristic is very different from the other ones. To the contrary, other characteristics look alike, having very close inflexion points and slopes, meaning the conduction is very similar between successive double sweeps, including the presence of an important bump around 15V. This bump can be attributed to moisture as it is not observed for protected test structures as shown in figure 4.28.b.



(a) (b)

Figure 4.27: TVS characteristics of S3BP structures at 25°C (a) and 60°C (b) after different hold times with a sweep speed of 0.1V/s.



(a) (b)

Figure 4.28: Double TVS sweep responses of unprotected S3BP (a) and unprotected SR3BP (b) test structures at 60°C. Ramp from 35V to -35V at 0.1V/s.

4.5.4.4 Physical interpretation

The bump observed in polluted SiOC:H structures is not the consequence of classical SE or PF conduction mechanisms because of evident electrical field dependency of these conduction phenomena (see section 4.5 for more details), but the result of the contribution

of an important number of mobile charges, to the measured leakage current. Such contribution, can be attributed to what we referred as space charges in section 1.3.2.2. The fact that figure 4.28.a clearly shows that the bump present in moisturised test structures can be reproduced similarly in positive or negative polarisation successively gives momentum to this hypothesis while no similar behaviour is observed for test structures protected from moisture. Furthermore, the width of the hump rather than a sharp peak of current is consistent with disordered moisture pollution in the SiOC:H low-κ dielectric material as shown in section 2.5.4. Such observations lead us to establish the qualitative scenario concerning free space charges movements in the SiOC:H low-κ dielectric material, during successive TVS double sweeps, presented in figure 4.29. In this scenario, we assume the free charges considered are negative, which is consistent with the SiOC:H material information, in particular the fact that moisture translates in electronegative $-$OH groups in the SiOC:H material (see section 2.19 for more details). Free charges being disorderly distributed in the SiOC:H material, they arrive gradually close to one electrode as long as the electrical field remains in the same direction. Then, when the electrical field direction changes, *i.e.* when the second TVS ramp starts, mobiles charges start to migrate to the opposite electrode. As they have been spatially grouped during the first TVS ramp, they are more likely to reach the opposite electrode in groups during the second TVS ramp. Despite such scenario might be useful to understand qualitatively the electro-chemical

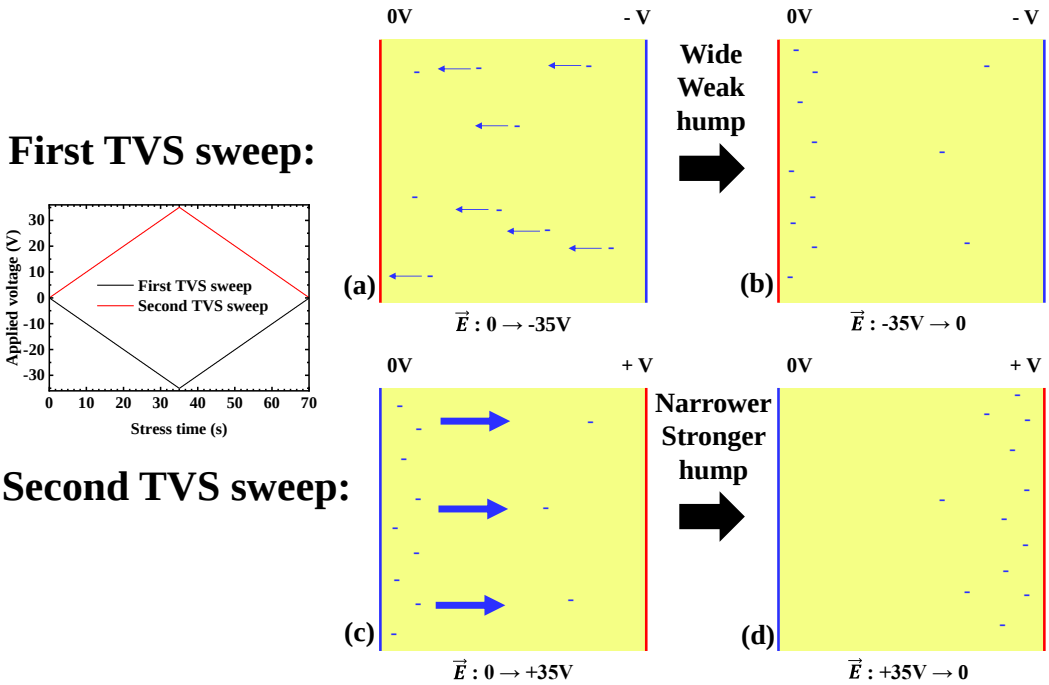


Figure 4.29: Space charges movement scenario during double TVS sweep of an unprotected S3BP test structure.

behaviour of the SiOC:H low-κ dielectric material, another important aspect is to be considered in such amorphous material: its pre-existing defects and potential interactions between moisture pollution and these defects.

4.5.5 Traps in SiOC :H dielectric

As we have seen in section 4.5.3, moisture seems to affect dramatically conduction mechanisms. Moreover, successive I-V measurements have shown that unpolluted test structures experience a charge trapping during the first measurement, resulting in lower leakage current for I-V performed afterwards, interpreted as potential barrier height rising. But this phenomenon is significantly more complex in presence of moisture because it remains difficult to distinguish charge trapping from moisturised SiOC:H material degradation. Therefore, a deeper understanding of the SiOC:H material traps is required.

4.5.5.1 As-deposited SiOC:H traps

Defect of integrated dielectrics materials are often analysed by measuring the capacitance of a test structure while an electric field is applied to it. Most of the time, the electric field is intense to induce significant defect generation in the dielectric material, which provokes a modification of the capacitance. In practice, the constant voltage stress applied on the structure is interrupted for a very short time to perform the capacitance value measurement. This method has been applied on our test structures protected against moisture (see section 3.3 for more details), unfortunately the resulting capacitance evolution over stress time, also called transient capacitance, does not vary significantly (figure 4.30). The fact that no capacitance evolution can be observed does not mean there is no significant defect generation, otherwise, dielectric breakdown would be very unlikely to occur on a reasonable time scale, however, it does not induce a measurable capacitance change to be related to the quantity of trapped charges. Similarly, no capacitance evolution over stress time is observed for moisturised test structures (figure 4.30).

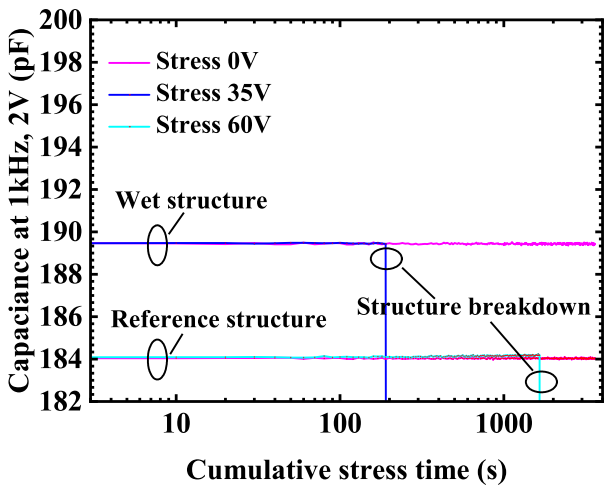


Figure 4.30: Transient capacitance of wet (S3BP) and reference (SR3BP) test structures under CVS.

In fact, the trapping phenomenon, characterised by a decrease of the current crossing a dielectric, is the consequence of electrons that recombines with the material pre-existing defects, hence called acceptor defects. The presence of these electrons in the material contributes to repels even more electrons. This can be represented energetically in a band diagram as a barrier height rising at the cathode [57]. During this process, some of the electrons gain sufficient kinetic energy to generate ionization by impacts [57], as hydrogen bonds breaking described in the ID model physical interpretation [66]. Recent studies allowed to gather information on SiOC:H dielectrics traps using the Electrically Detected Magnetic Resonance (EDMR) characterisation technique. It consists in measuring the dielectric resistance change under illumination of microwave radiation while it is placed in a magnetic field. This technique relies mainly on spin Pauli exclusion principle, which is why the sample is to be placed in a magnetic field. In fact, the magnetic field orients the electrons occupying donors and acceptors traps and only a certain frequency, called resonant frequency, of the microwave light pulse can flip the electron spin in the direction opposed to the magnetic field. Hence, this electron must move to another defect to ultimately recombine with a hole in the valence band. This produces a decrease of the material resistance at donors and acceptors traps resonant frequencies. Such resonant frequency can be determined by frequency scanning for both types of defects. As a consequence, using such technique allows to reach traps at any energy level in the material band-gap, which is particularly appropriate for SiOC:H dielectrics. Thanks to this technique, Mutch *et al.* brought evidence that, in dense unpolluted SiOC:H dielectrics, conduction is mainly assisted by carbon dangling bonds defects centres [157]. They also shown the energy range of such defect is not very broad and the defect density is 2.10^{17} defects per cubic centimetre [157]. The band gap of the SiOC:H dielectric material used in this study has been measured by XPS from the onset of energy loss spectrum of O1s orbital photoelectrons, following the procedure described in [158], [159] and [160], which shows that the POR SiOC:H has a band gap E_g of 8.0 ± 0.4 eV, similar to state-of-the-art data [157], [161]. This information results in the band diagram presented in figure 4.31. One can note that effective thickness of the MIM structure is not drawn at appropriate scale. In fact, both electrodes are 7 nanometres thick while the POR SiOC:H dielectric material is approximately 130 nanometres thick.

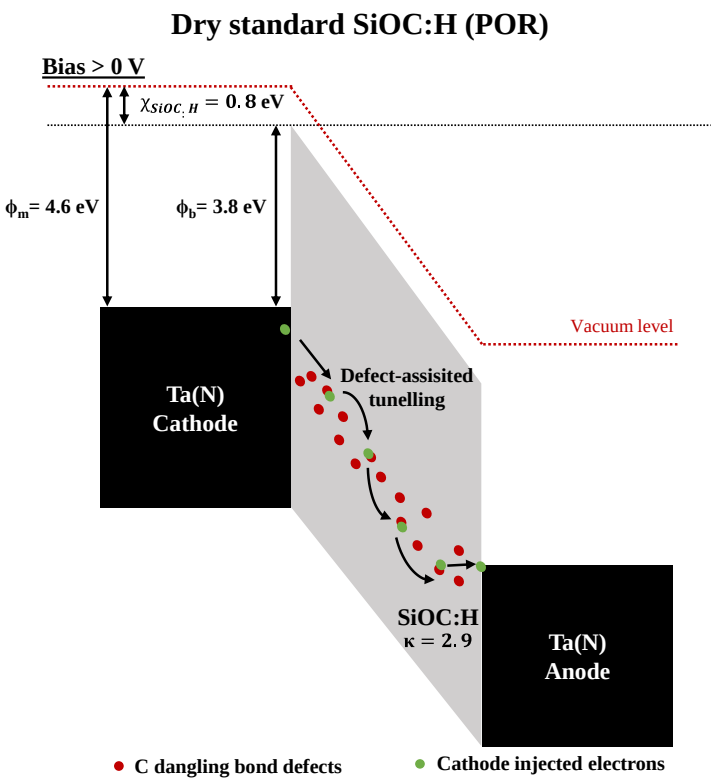


Figure 4.31: Band diagram of unpolluted integrated SiOC:H dielectric under electrical bias.

4.5.5.2 Moisture influence on traps

As said in section 4.5.5.1, carbon dangling bonds acceptor defects are present in the SiOC:H dielectric material. This information suggests these defects might be preferential recombinations locations for moisture OH groups. Brought together with the chemical structure of the material determined with FTIR and MIR spectroscopies (see section 2.5.4), especially the significant presence of $C-H_3$ groups, indicates that, in the $C-H_3$ region of the dielectric molecular structure, the oxygen of the polar OH group, which is strongly electronegative, is likely to recombine with a carbon dangling bond while the hydrogen might also establish electrostatic bonds with neighbouring hydrogen atoms. Such configuration, is in turn likely to induce non-negligible interactions between as-deposited carbon dangling bonds and OH groups from moisture, leading to significant changes in the trapping process. Furthermore, the polar OH groups around pre-existing material carbon dangling bonds defects would favour electron transport from one defect location to another. Then, this favourable configuration results in an enhanced probability for an electron to have enough energy or momentum to experience inelastic collision with a bonded hydrogen atom and to break the bond and displace the hydrogen atom far enough to prevent spontaneous bond reformation which thus, generate a defect [62]. Qualitatively, a more favourable electronic transport path results in electrons with (slightly) higher average kinetic energy. As a result, the more the moisture, the more probable the defect generation. In turn, the more defect, the more the probability of one more defect.

4.6 Conclusion

To conclude, we have shown that climatic storage at temperatures higher or equal to 85°C with very high Relative Humidity (RH) fails at accelerating moisture ingress. MIR spectra analysis allowed to provide a solid understanding of the material moisture desorption kinetic, although incomplete, suggesting significant moisture desorption at temperatures as low as 75°C, confirming the difficulty to find a moisture ingress acceleration methodology. We also pointed out the dramatic decrease of time-to-breakdown performance due to moisture ingress, supported by a methodology to systematically locate electrically breakdown points in the test structures. Peculiar electrical signatures of moisturised test structures together with material analysis undoubtedly confirm the moisture influence in the SiOC:H dielectric material. Despite the fact that test structures protected against moisture behaviour is well-known thanks to previous literature, our experiments have shown that hardly reproducible and unpredictable effects occur in the presence of moisture. For example, thermally activated waves in V-t characteristics during Constant Current Stress (CCS) tests have been identified, as well as a leakage current flowing throughout the whole structure, observed by EMission MIcroscopy (EMMI). It also suggests that moisture is electrically active and might have significant interactions with pre-existing defects in the dielectric chemical structure. Furthermore, as the Impact Damage (ID) model is gaining momentum in recent advances, it is possible that the presence of polar molecules in the dielectric favours electron transport around defect sites, in turn enhancing the defect generation probability.

General conclusion and perspectives

"People think of education as something they can finish."

Isaac Asimov

Interconnects performance, in particular in terms of reliability, is absolutely crucial for critical applications such as automotive and medicine. This need for reliability, and increasing computational power, motivated a substantial number of breakthroughs in the semiconductor industry, amongst which the introduction of SiOC:H low-κ dielectrics material in the BEOL thanks to their interesting electrical properties. The lack of understanding of moisture-related degradation mechanisms induces an inability to predict the lifetime of interconnects polluted by moisture. Advanced technology nodes, below 90 nm still extensively rely on SiOC:H low-κ and porous SiOC:H ultra low-κ dielectrics for interconnects and replacements candidates are nowhere near the corner for next decades. As a result, very high levels of understanding and mastering are required to allow Moore's law to keep going with automotive grades fail rates, from which moisture-related degradation study is the compelling extension.

In the search of a better understanding of moisture-related SiOC:H low-κ dielectrics performance degradation, a concise review of dielectric phenomena has been detailed. We have discussed to what extent SiOC:H dielectrics are challenging with respect to moisture and what are the main parameters to evaluate the dielectric quality thanks to typical electrical characterisation techniques. Physical root-causes of main reliability models, R-E, PL and ID. Recent literature shows that the latter is gaining momentum despite there is no consensus yet. However, they do not account for external pollutants influence on the dielectric reliability. Our data confirmed that moisture dramatically decreases the dielectric time-to-breakdown as well as it increases leakage current and capacitance values, despite the fact that no clear correlation can be found between these parameters.

In order to gather information on the SiOC:H dielectric material, a set of physical characterisations has been carried out: wafer level dielectric constant measurements, ellipsometric porosimetry, GISAXS, AFM and PARXPS surface analysis, EDX chemical interfaces profiles and FTIR and MIR spectroscopies chemical structure analysis. These physico-chemical characterisations gave a precise overview of the material structure at macroscopic and microscopic scales. As a result, we have shown that our SiOC:H dielectric material is non-porous and has a very uniform dielectric constant over the wafer around its typical value of 2.9. Moreover, XPS characterisations show that it is composed of 26 at. % of silicon, 41 at. % of oxygen and 33 at.% of carbon, while hydrogen is not detected, hence taken to be virtually absent. Furthermore, chemical structure analysis

revealed that it is mainly structured around Si−O−Si bonds in which some oxygen atoms are bonded to carbon atoms introduced by the TMS precursor. These carbon atoms are also bonded to several hydrogen atoms, often three, that terminate the SiOC:H molecule. Over several months, MIR monitoring of moisture-related −OH bonds region highlighted the important moisture uptake of SiOC:H material, as well as the efficiency of silicon nitride as moisture ingress barrier.

Then, to evaluate the influence of moisture on interconnect reliability, a set of electrical test structures has been designed and characterized. Thus, the so-called dual-damascene fabrication process has been described with a focus on steps that impact the SiOC:H dielectric reliability performance with respect to moisture, such as CMP and cleans. Materials and properties required to achieve successful BEOL encapsulation and Far BEOL fabrication, in particular the mechanical constraints brought by SiOC:H low-κ dielectric materials in the interconnects due to its poor mechanical properties have been detailed. All structures are based on a C/S/C elementary structure, from which line-to-line spacing is varied from 105nm to 165nm, as well as serpentine length from 3.7 cm to 384.4cm, and test pads width from 30 to 130 μm. Every structure is also designed with a robust seal-ring enclosing the whole structure, including the testing pads, in order to protect it from moisture pollution. These two versions of each structure allowed to study the effect of moisture on the structure. To ensure these test structures are similar to actual dies interconnects, we have detailed the conception steps required to transform CAD, corresponding to the user desire, into actual silicon. Firstly CAD-to-Mask (C2M) operations have translated CAD layers into physical masks, then, complex OPC has been employed in order to counterbalance optical interferences and definition constraints occurring during photo-lithography. Moreover, to obtain reliable test structures across the whole wafer, some fabrication recipe optimisations such as seal-ring contact bars profile improvement and aluminium capping etch adjustment have been optimised, with the help of inline process control.

Moreover, to base our moisture-related study on reliable and trustable results, a specific attention was paid to the probing effect through the characterisation of test structures enclosed by seal-rings with different pad widths. Indeed, as automated test equipment has a limited precision, we have shown that a slightly misaligned probing on pads smaller than 50 μm resulted in dramatic increase of the leakage current of the C/S/C structure, symptom of moisture ingress. In fact, probing on or close to the pad edge resulted in important several microns-long cracks diving from the edge of the pads down to metallisation levels, making the passivation films ineffective because of moisture diffusion paths provided by these cracks. Moreover, for an important number of successive tests on the same structures, it is not possible to ensure 70 μm-wide pad are not damaged, which, without any doubts, would ruin our moisture-related study as only one damaged pad is sufficient to allow moisture to pollute the whole structure. This also underlines that despite evident financial benefits of reducing the wafer dicing streets, this should be done with caution as large cracks might even damage the nearby chip seal-ring. Alternatively, it confirmed the fact that Far BEOL mechanical robustness is challenging, mainly because of integrated SiOC:H low-κ dielectric material poor mechanical properties, in particular for wire bonding. As a result of this observation, and given the important number of probes touchdowns required throughout our studies, the choice has been made to rely only on 110 μm-wide pads for all our electrical tests.

In the last part of this work we focused on the electrical investigation of moisture-related peculiar behaviour. Hence, several climatic storage conditions have been evaluated in order to develop an optimal moisture ingress acceleration methodology. However, no condition could unequivocally accelerate moisture ingress. As a result, a detailed SiOC:H material MIR analysis has been conducted that shown that annealing temperature as low as 75°C results in moisture desorption. Moreover, chemical analysis allowed to distinguish two main types of hydroxyl groups: bonded to the SiOC:H network and hydrogen-bonded. Then, area scaling property of the time-to-breakdown has been investigated through Poisson and compound Poisson distributions for protected structures. However, the weak statistic prevented a firm conclusion on the validity of either a standard Poisson distribution or a complex mixing function determination required for compound Poisson distribution. Furthermore, it has been confirmed that the inability to develop an appropriate moisture ingress acceleration methodology is a major sticking point for evaluating the effects of moisture on the area scaling property of the time-to-breakdown. Afterwards, a comprehensive analysis of the SiOC:H low-κ dielectric material has been conducted. It puts into light peculiar changes during CCS characterisations due to moisture soaking the SiOC:H that, surprisingly, did not appear in CVS characterisations, apart from the dramatic time-to-breakdown decrease. These waves amplitude in V-t plots measured during CCS are thermally activated, hence, so is the associated physical phenomenon. Deeper insights on electrical conduction mechanisms have been gained through standard I-V characterisations which allowed to confirm that conduction across unpolluted SiOC:H low-κ dielectric material is whether Schottky thermionic Emission (SE) or Poole-Frenkel trap-assisted tunnelling (PF). Moreover, erratic conduction through moisturised SiOC:H low-κ dielectric has been observed and because of the presence of different I-V plot inflexions, we concluded on changing conduction mechanisms. It has also been shown by EMission MIcroscopy (EMMI) that the moisture-induced leakage current flows through a preferential path but across the whole structure. As a consequence, this finding led the presented study to consider a more confidential characterisation technique: Triangular Voltage Sweep (TVS). TVS characterisations confirmed major conduction mechanisms differences between protected and unprotected test structures, result of SiOC:H low-κ dielectric material pollution by polar hydroxyl groups. Moreover, it provided evidences of mobile free space charges presence in SiOC:H low-κ dielectric material of unprotected test structures having high leakage current ($> 10^{-9}$A). This crucial information brought together with evidences of carbon dangling bonds assisting role in conduction mechanisms provided by recent state-of-the-art, give a better understanding of moisture pollution of the SiOC:H material at the molecular scale and its impact on reliability.

Indeed, various electrical characterisations and physical analysis achieved during this study pointed out the dramatic effects of moisture on the interconnect reliability because of hydroxyl groups bonding around carbon dangling bonds defects, making them closer both locally and energetically, facilitating conduction from one electrode to another. Alternatively, mobile charge contribution to conventional trap assisted tunnelling provokes peculiar electrical signatures such as bumps for instance, presumably the result of weakly bonded hydroxyl groups acting as charge carriers when strong electrical field is applied across the SiOC:H low-κ dielectric material.

Nonetheless, on an industrial point of view, it is still required to determine a reliable moisture ingress detection parameter and associated criteria in order to provide last re-

sort non-quality detection before final customer shipping. For instance, leakage current through SiOC:H low-κ dielectric material median or spread increase, time-to-breakdown median and spread decrease and capacitance increase are potential candidates. However, each of them induces important industrial constraints: leakage current cannot be used to point out faulty chips as it does not always correlate with time-to-breakdown, while the time-to-breakdown measurement is destructive, hence has a limited pertinence. Issues that do not affect capacitance evolution over time, which sadly requires months of wait time, if not years, as moisture ingress cannot be appropriately accelerated, hence additional research is required to deepen and refine information gathered in this work to achieve reliable detection of chips prone to moisture uptake. Indeed, evidences provided by this work could be reinforced by optimised experiment protocol such as leakage current measurement during TVS hold time to unravel electrical behaviour, in particular of mobile charges, prior to apply the TVS ramp. Furthermore, an extensive moisture-induced traps Electrically Detected Magnetic Resonance (EDMR) study would contribute to refine the chemical picture presented, in particular on the contribution of different hydroxyl groups to electrical conduction. Such analysis could be completed with more appropriate Metal-Insulator-Metal (MIM) or Metal-Insulator-Semiconductor (MIS) structures especially targeted to defect spectroscopy, hence with thinner SiOC:H low-κ dielectric film and lower series resistance in order to allow low frequency Capacitance-Voltage analysis (<20 Hz) for instance [162].

Ultimately, despite this work gives a better understanding of moisture-induced degradation root-causes at the chemical level and potential detection candidates, an electrochemical approach of moisture diffusion and moisture-assisted conduction phenomena in SiOC:H low-κ dielectric material is required to conclude unequivocally on the interactions between hydroxyl groups and pre-existing SiOC:H dielectric material traps and free space charges. Indeed, such study would bring a stronger theoretical basis to the empirical findings of the present work, completing a comprehensive theory-experiment correlation.

Such sharp understanding of the moisture-induced degradation process and its consequences on the interconnect could help rationalize the numerous countermeasures used to prevent moisture ingress in chips, from fabrication to in-field operation. For instance, a clear view of moisture-related underlying phenomena could offer more appropriated products qualification flows, targeting worst case conditions with respect to moisture ingress, allowing effective early detection of potential moisture-induced failures to safely enable faster time-to-market for new products. In other words, this could allow to reduce the complexity of reliable chips fabrication process, hence reducing fabrication and development costs, which are key drivers of IoT and Advanced Driver-Assistance Systems markets development for instance.

Personal publications

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