Modeling and Simulation of Alternative Channel Material MOSFETs

Tapas Dutta

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Présentée par

Tapas DUTTA

Thèse dirigée par **Georges PANANAKAKIS** et
codirigée par **Quentin RAFHAY**

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devant le jury composé de :

M. Francis CALMON
Professeur, INSA de Lyon, Président
M. Jean Luc AUTRAN
Professeur, Université Aix Marseille, Rapporteur
M. Fabien PREGALDINY
Maître de Conférences HDR, Télécom Physique Strasbourg, Rapporteur
M. Quentin RAFHAY
Maître de Conférences, Grenoble INP, Co-encadrant
M. Georges PANANAKAKIS
Professeur, Grenoble INP, Directeur de Thèse

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Tapas Dutta

Advisors: Georges Pananakakis, Quentin Rafhay

Laboratory: Institut de Microlélectronique, Electromagnétisme et Photonique - Laboratoire d'Hyperfréquence et de Caractérisation (IMEP-LAHC)

Doctoral School: Electronique, Electrotechnique, Automatique et Traitement du Signal (EEATS)

INP Grenoble

To my teachers, friends and family

Abstract

As silicon CMOS technology is approaching fundamental scaling roadblocks, alternative channel materials like Ge and III-V based devices have attracted a lot of attention and have been the subject of active research during the last 10 years. While these new materials have very promising transport properties, studies have shown that they have worse short channel performance than the Si counterparts. Hence there is a strong need to evaluate the impact of change in the channel material on the device performance in terms of the short channel effects. In this work, first some issues with conventional modeling of double gate MOSFETs are dealt with. A new analytical model of the built-in potential is proposed and shown to correct the errors due to wrong boundary conditions. The roles of quantum confinement effects, material parameters and architecture of nanoscale III-V MOSFETs on the electrostatic integrity in terms of SCEs are thoroughly examined. A modified parameter to capture the drain induced barrier lowering is used to predict the performance degradation in the post-threshold region of the MOSFETs. Impact of the source to drain tunneling on the subthreshold behavior and hence the scalability of III-V devices is also analyzed in this thesis.

Résumé

Les technologies CMOS à base de silicium approchants les limites fondamentales de la miniaturisation, de nouvelles options sont nécessaires pour continuer la feuille de route de l'industrie de semi-conducteurs. Les matériaux III-V et le germanium sont actuellement très étudiés à ces fins, pour remplacer le silicium en tant que matériau canal des transistors MOSFETs. Bien que les propriétés de transports de charges de ces matériaux soient très fortes dans les substrats massifs, les performances des composants à base de III-V présentent actuellement de fortes dégradations par rapport à ce qui pourrait être attendus. En conséquence, il est nécessaire d'évaluer théoriquement l'impact du changement de matériau de canal sur les performances de ces dispositifs. Dans ce travail, les problèmes de modélisation des effets de canaux cours des composants MOSFET à base de III-V ont d'abord été étudiés. Un nouveau modèle analytique du potentiel électrique dans le canal du MOSFET est proposé et démontré afin de corriger des erreurs dues aux mauvaises conditions limites. Les rôles des effets quantiques de confinement, des paramètres des matériaux ainsi que le rôle de l'architecture des MOSFET III-V sur les effets de canaux courts sont ensuite examinés. L'impact de l'effet tunnel dans la direction source-drain est également analysé dans la dernière partie cette thèse.

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Chapter 1

Introduction

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1.1 State of the art in transistor industry

The transistor industry has come a long way since the invention of the point-contact transistor in 1947 by John Bardeen, William Shockley and Walter Brattain at Bell Labs through today's generation of nanometric MOSFETs in multiple flavors. This growth of the transistor industry has been accompanied by miniaturization of the devices in order to increase device density on integrated circuits. During the last four decades, the trend of scaling down of the MOSFET channel length has been following the so-called Moore's law [1] that states that the transistor density on an integrated circuit doubles roughly every 18-24 months, resulting in increased functionality and performance and

reduction in production costs. In the recent past we have seen technology nodes of 45 nm going into production in 2007, 32 nm in 2009, and 22 nm process for 3-D tri-gate transistors in 2011 [2]. For sustaining the Moore's Law as device dimensions continue to shrink to physical limits, technological innovations are constantly needed.

1.1.1 Limits of scaling

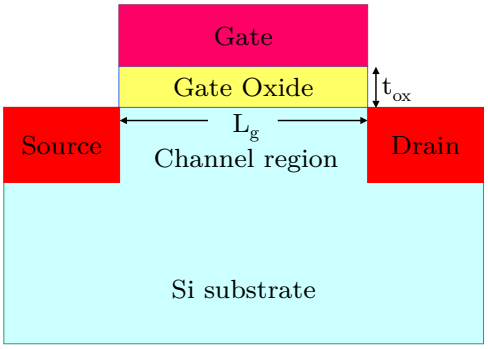

Figure 1.1: Simplified MOSFET Structure

Traditional MOSFET scaling meant a reduction in the physical dimensions: L_g, t_{ox} and the Source/Drain contacts, and also the supply voltage V_{DD} and increase in the substrate doping, N_a. The era of conventional scaling of device dimensions came to an end in the 1990s, primarily due to the inability of the SiO_2 gate oxide (1.2 nm for 90 nm technology [3]) to undergo further scaling and gate leakage becoming a critical issue. In the nanoscale regime, there exist tight trade-offs between the three main metrics that are used to qualify a field effect transistor's performance: on current (I_{on}), power consumption (P_{DD}), and Short-Channel Effects (SCEs). Figure 1.2 by Takagi et al. [4] depicts the tradeoff correspondence and the physical or device parameters that affect them. For example, power-supply voltage V_{DD}, threshold voltage V_t, and the efffective oxide thickness (EOT) affect both the I_{on} and P_{DD}, and hence there is a trade-off between these two metrics. The physical mechanisms causing the tradeoffs are shown inside the boxes.

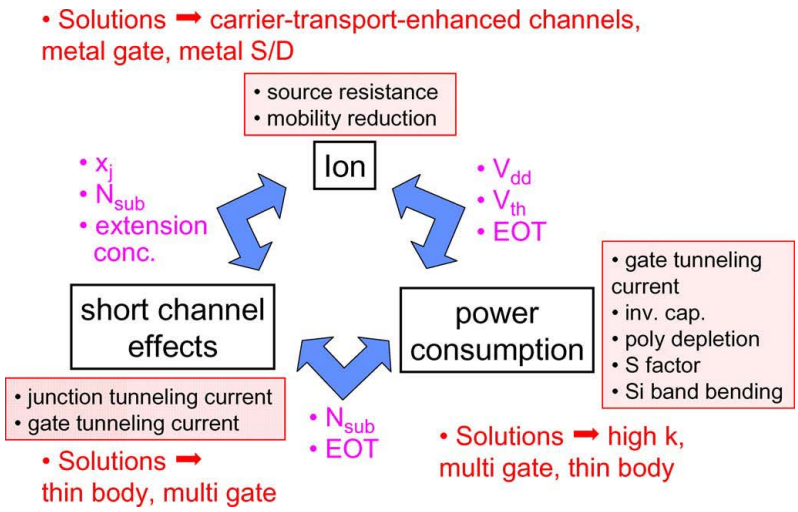

Figure 1.2: Tradeoff factors among on-current (I_{on}), power consumption (P_{DD})/leakage current(I_{off}), and SCEs under simple device scaling and possible solutions to mitigate the issues. Taken from [4]

1.1.1.1 Power Constrained Scaling

Device speed and power are two important parameters in the semiconductor device industry. The intrinsic switching delay of a MOS transistor is dependent on the gate capacitance (C_g), the supply voltage (V_{DD}) and the on-current (I_{on}) as:

$$\tau_d = C_g V_{DD} / I_{on} \tag{1.1}$$

The power consumption in a digital circuit is a sum of three components (with reference to an inverter): dynamic power (used during charging and discharging the inverter load), subthreshold leakage power and short circtuit power [5] [6]:

$$P = C_L V_{DD}^2 \alpha f + I_{leakage} V_{DD} + P_{SC} \tag{1.2}$$

where α is activity factor, C_L is load capacitance and $I_{leakage}$ is the subthreshold leakage current.

In the conventional scaling regime, with the introduction of each new technology node, the intrinsic delay was reduced and hence, the maximum intrinsic switiching speed $1/\tau_d$ improved with device scaling leading to higher clock speeds in the integrated circuits.

However, in recent years the microprocessor clock speed has saturated at around 4 GHz. This is ascribable to the enormous increase in power dissipation at high clock frequencies and hence the dissipated power density in modern CPUs is constrained to hover around 100 W cm^{-2} as shown in Figure 1.3 (taken from [5]). Beyond this limit, power dissipation in a Si MOSFET has became difficult to scale down as we have entered this regime of "Power constrained scaling" [7], and hence reduction in supply voltage is needed to stop excessive heating.

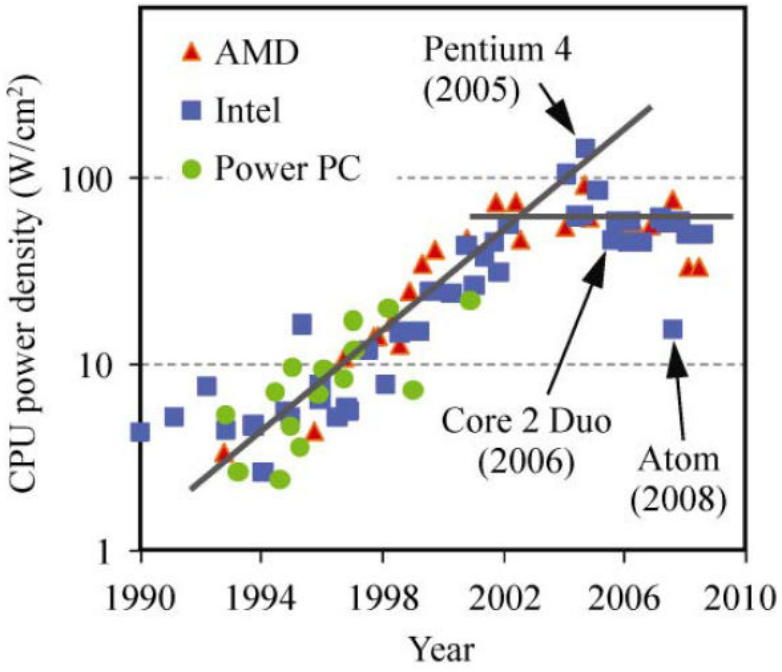

Figure 1.3: The steep increase of CPU power density in the previous generations has now somewhat saturated around 100 W cm^{-2} with the introduction of multi-core CPUs [5]

But, the supply voltage scaling has also slowed down because reduction in supply voltage causes degradation of the Si MOSFET performance as the drive current, I_{on} decreases with decrease in V_{DD}. The ITRS 2012 update [8]

has projected the gate length of Si MOSFETs to be 6 nm in 2026, with device power consumption being considered to be the limiting factor instead of speed as from circuit design perspectives speed requirement can be relaxed.

1.1.1.2 Short Channel Effects

In a long channel MOSFET, the channel potential profile is a function of the gate voltage only, and it is more or less flat along the channel direction. When the gate length is reduced and becomes comparable to the depletion-layer widths of the source and drain junctions, the applied drain voltage starts to affect the channel potential and becomes 2 dimensional (sometimes assumed to be parabolic [9]). The potential barrier is lowered due to the proximity of the source and drain and hence it becomes difficult to properly switch off the device as more carriers can diffuse from the source to the drain even at gate voltages lower than the threshold voltage, producing subthreshold current flow in the device.

Essentially seen as a source of off-state current degradation, Short Channel Effects (SCEs) are used to quantify influence of the drain bias and the loss of gate control on the device electrostatics. Figure 1.4 summarizes the modifications of the $I_d - V_g$ and $I_d - V_d$ characteristics of a MOSFET induced by short channel effects. SCEs are usually investigated in subthreshold regime and are expressed in terms of the following quantities:

- Subthreshold Slope (SS) : It is defined as the inverse slope of the $\log I_d$ Vs V_g curve.
$$SS = \frac{dV_g}{d \log I_d}$$
in mV/dec. SS increases with the shortening of the channel.

- Drain Induced Barrier Lowering (DIBL): When the drain bias is increased, the source to channel potential barrier is found to reduce in a short channel device, as shown in Figure 1.5. Conventionally it is measured as the reduction in threshold voltage per unit increase of drain

voltage.

$$DIBL = \frac{V_t(V_d = V_{DD}) - V_t(V_d = 0.05V)}{V_{DD} - 0.05V}$$

- Threshold Voltage Roll-Off: V_t roll-off is the reduction in threshold voltage as we go from long channel device to shorter channel ones.

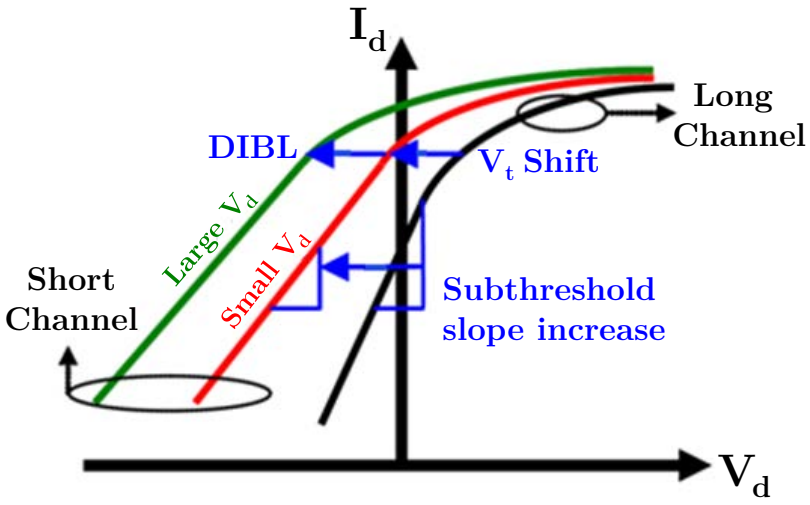

Figure 1.4: Schematic representing the impact of short channel effects on the $I_d - V_g$ characteristics of an nMOSFET

The shorter gate lengths would cause worsened short channel effects: higher subthreshold slope, higher DIBL and increased threshold voltage roll-off, leading to increased off currents in the devices. In this work, only the DIBL and the subthreshold slope will be used as figure of merit of SCEs, as they are the main causes of leakage increase.

1.1.2 Heterogeneous Scaling and Technology Boosters

The constant-field scaling as elucidated in [10], consisted of scaling the device dimensions and voltages by constant factors while moving from one technology generation to the next. In contrast to this "Happy Scaling" era of homogenous scaling (similar materials and device structures), in the early years of the last decade, the industry moved towards heterogeneous scaling where different materials and new device architectures began to be used to

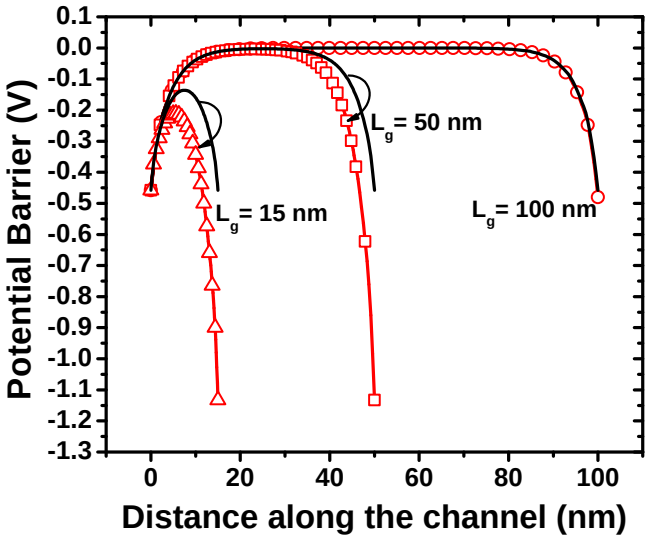

Figure 1.5: Demonstration of DIBL: While the surface potential distribution in a longer channel double gate MOSFET (100 nm gate length) does not vary with the applied drain voltage, drain induced barrier lowering is observed in the shorter channel device with 15 nm gate length. ($t_{Si} = 5$ nm, open symbols correspond to $V_d = 0.9$ V, and curves without symbols represent the $V_d = 0$ V case)

achieve the expected benefits of scaling [11]. Some of the limitations of traditional scaling have been conquered using new technological breakthroughs, sometimes called as "technology boosters". Two such boosters have been the use of Strain and High-κ Metal Gate.

In the last two decades a lot of research and eventually real application of strained Si provided a major boost to the carrier mobility in Si MOSFETs, starting with the 90 nm technology node, without the need of any radical change from the existing Si process flow. When Si is epitaxially grown on relaxed $Si_{1-x}Ge_x$, the lattice mismatch between Si and SiGe results in biaxial strain in Si layer. The amount of strain can be varied by changing the Ge content [12]. Uniaxial strain in the Si channel of MOSFETs can be induced during device processing [13], and is particularly useful for boosting hole mobility. Application of strain changes the band structure and results in altered band structure with reduced effective mass and less scattering for the electrons as well as holes leading to higher mobility, while keeping the

same channel material [14]. Both experimental and theoretical demonstrations have shown that the application of strain has the possibility to enhance on-currents by factors of around 4.5X in Si pMOSFETs and around 2X in nMOSFETs without a significant increase in leakage current [15].

An important reason for using Si in the IC industry is the reliance on the easy fabrication of the Si/SiO_2 channel/dielectric system which is stable and of very high quality compared to combinations other channel materials and their native oxides. In recent years the SiO_2 has been replaced by gate oxides with higher dielectric constants. For example, using high-κ HfO_2(κ ~20-25) or hafnium silicon oxynitride (HfSiON) to replace SiO_2 (κ = 3.9) or SiON, and metal gate electrodes to replace doped polysilicon has helped to avoid succumbing to the physical limits of conventional scaling [16]. Higher gate capacitance can be obtained compared to a SiO_2 system while suppressing the gate leakage [17]. A metal gate avoids poly depletion effects, offers lower gate resistance, lower phonon scattering and easy V_t engineering by work function tuning. A high-κ metal gate system results in much higher mobilities compared to a high-κ polysilicon gate [18]. Figure 1.6 shows how these two technology boosters helped maintain the technology improvement trend.

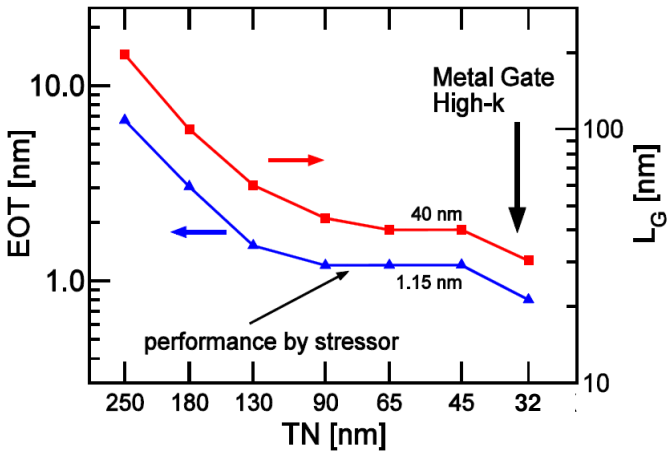

Figure 1.6: Technology Boosters: Strain and High-κ Metal Gate. (Taken from [19])

1.1.3 Possible Solutions in the Roadmap

Figure 1.7 shows the ITRS future projection about different technological innovations in different stages of growth: research required, development underway, pre-production and further continuous improvement. As already discussed, in the last decade, the following technology innovations were successfully incorporated in the existing silicon process flow: enhanced mobility and high-field transport via strain, enhanced quasi-ballistic transport (via short gate length and strain), high-κ gate dielectric, metal gate electrode, and Fully depleted SOI MOSFET.

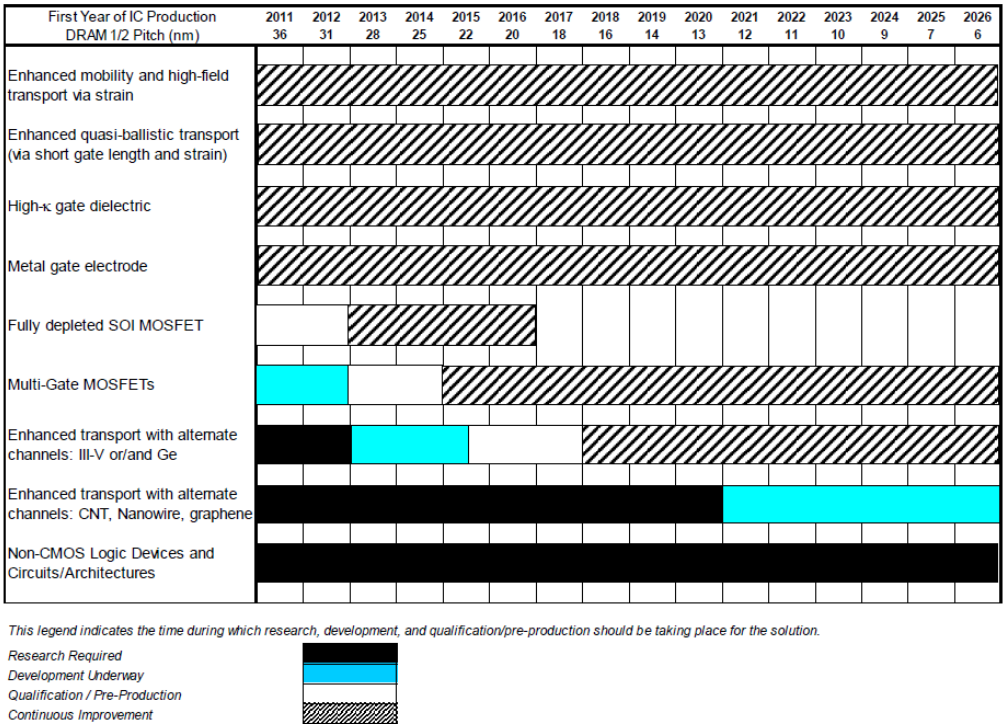

Figure 1.7: PIDS (Process Integration, Devices, and Structures) Projection, ITRS 2011 [8]

Planar Fully Depleted Silicon On Insulator (FDSOI) MOSFETs (Figure 1.8) have been well known for a long time for their advantages over the bulk counterpart: good electrostatic control enabling lower V_{DD} (for example [20]), undoped/lightly doped channel leads to reduced random dopant fluctuations

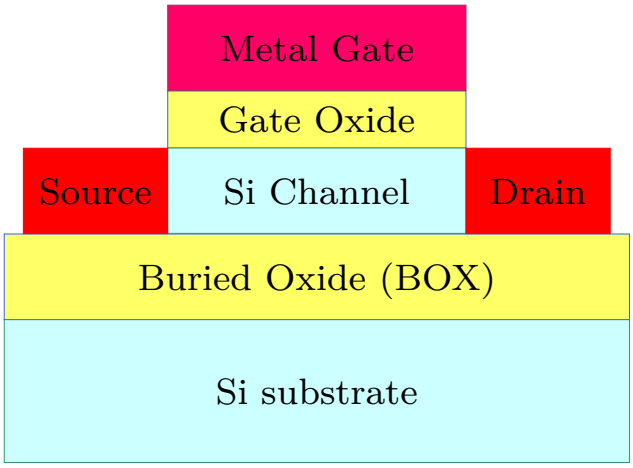

Figure 1.8: FDSOI MOSFET Structure

and hence reduced process variability, reduced source-substrate leakage due to presence of buried insulator layer, and most importantly, maintaining consistency with existing fabrication processes (e.g. the 28 nm bulk technology).

At the same technology node, Ultra Thin Body and Buried oxide (UTBB) FDSOI transistors allow to have shorter channel lengths than bulk devices. Body biasing (applying voltage to the substrate) the FDSOI device effectively makes it act like a double gate device (thanks to the very thin buried oxide layer) leading to much lower leakage and improved performance. Even in recent years the FDSOI MOSFETs have been the subject of active research [21] [22] and considered as viable alternatives to bulk CMOS, offering competition to other new technologies like FinFETs [23].

A major deviation from the planar transistors are the Multi-Gate MOSFETs, either bulk or SOI. Mulitple gates, particulalry the double and triple gate SOI FinFETs were the topic of extensive exploration in the last decade, although other possibilities: like quadruple gates, gate-all-around (GAA) MOSFETs and bulk FinFETs have also been researched [24] [25]. Figure 1.9 shows three dimensional schematics of double and triple gate FinFET devices on fabricated on SOI. These devices, due to the presence of more than one gate,

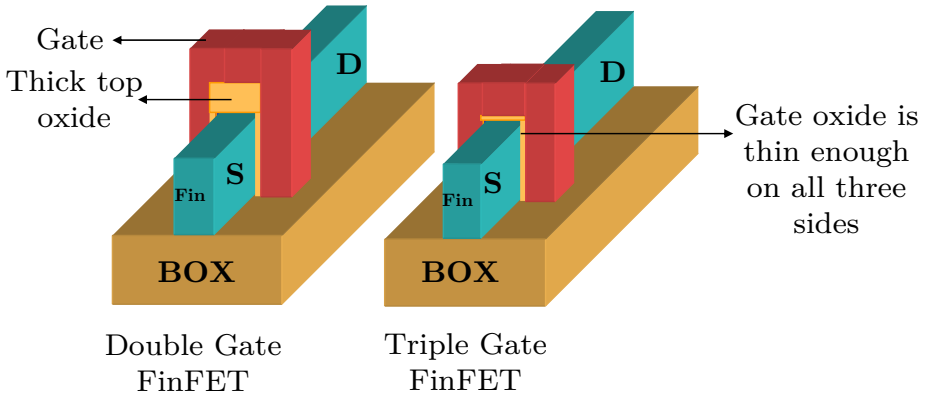

Figure 1.9: Double and Triple Gate FinFET Structures

offer higher drive currents and tighter gate control of the channel electrostatics leading to excellent short channel performance. Accordingly, the industry has already entered the production phase going with Intel's tri-gate FinFETs [2].

1.2 III-V MOSFETs

ITRS 2011 lists alternative channel materials (ACM), namely III-V and Ge based MOSFETs as currently being pursued with a goal to enter production in the next 5-10 years [8]. Indeed, of late, a lot of research has been directed towards using these high mobility materials as MOSFETs channels. For example, Figure 1.10 depicts the increase in the number of publications concerning III-V MOSFETs in the last few years, hinting at the serious consideration of these devices by the academia as well the industry.

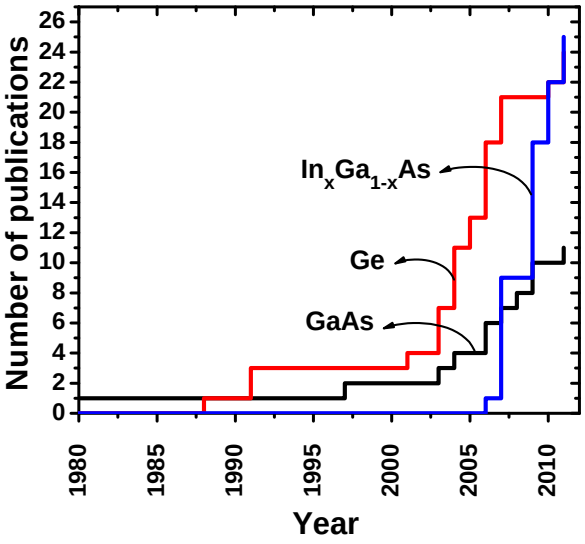

Figure 1.10: Number of publications concerned with III-V MOSFETs in IEEE TED and EDL

1.2.1 Motivation for ACM/Why III-V?

There has been, in fact a long interest in alternative channel materials for replacement of Si as channel material in transistors. The first transistor realized (point contact type) in 1947 was germanium based. As early as 1966, InAs channel transistors were proposed [26] and in 1991 Ge CMOS was demonstrated [27]. But the growth of III-V/Ge CMOS for logic remained hindered because of several technological problems (e.g. Fermi level pinning), and high mobility materials were rather mostly used for HEMT devices (which are impractical for use as logic devices due to their large gate leakages). In the last decade, they have made a comeback as some of the stumbling blocks have been dealt with (for example unpinning the Fermi level using Ga_2O_3/Gd_2O_3 as gate oxide [28, 29], achieving good quality thermally grown GeO_2 [30] etc.).

As explained in subsection 1.1.1.1 there is a need to lower V_{DD}, while maintaining, or if possible, increasing the device speed. A channel material having higher carrier mobility compared to Si can achieve this goal. In this view, III-V/Ge MOSFETs are strong candidates for high performance (HP) logic as they can offer lower power (approaching $V_{DD} = 0.5$ V) at speeds similar to, or even higher than the Si counterparts due to their inherent good transport

	HP	LOP	LSTP	III-V/Ge
Speed (I/CV)	1	0.5	0.25	1.5
Dynamic Power(CV^2)	1	0.6	1	0.6
Static Power(I_{off})	1	$5x10^{-2}$	$1x10^{-4}$	1

Table 1.1: ITRS Comparison of HP, LOP, LSTP and III-V/Ge Technologies

properties.

Comparison of HP (high performance), LOP (low operating power), LSTP (low standby power), and III-V/Ge Technologies according to ITRS 2012 report [8] is shown in Table 1.1 in terms of device speed, dynamic power and static power dissipation. III-V/Ge devices with their higher speed and lower dynamic power, are expected to outperform Si HP devices.

1.2.2 ACM Trade-offs

Table 1.2 lists some material properties of certain materials as candidates for MOSFET channel material. As can be seen, what makes germanium and III-V compound semiconductor materials attractive is their much lower effective masses and higher carrier mobilities.

Following Natori's ballistic model [31], the injection velocity of electrons in the device is related to the effective mass under non-degenerate conditions as follows [32]:

$$v_{inj} = \sqrt{2\kappa_B T/\pi m^*} \tag{1.3}$$

Hence channel materials with lighter effective masses can provide higher injection velocity, v_{inj} in ultra scaled MOSFETs. It has been demonstrated that these materials present greatly improved transport properties with respect to unstrained and even strained silicon [33].

III-V materials generally have multi-valley bandstructures: A primary Γ valley with low-effective-mass and satellite valleys (L and X) with higher effective mass for electrons. Many III-V materials, for example $In_xGa_{1-x}As$ grown lattice matched to InP or InAs grown lattice matched to AlSb have

very low effective masses in Γ valley as well as large inter-valley energy separations ($\Delta_{\Gamma-L}$, $\Delta_{\Gamma-X}$ which can be increased by increasing the In content) reducing the chances of spillover of electrons from Γ to L valley. This could lead to achieving higher mobilities at both low as well as high applied fields. Figure 1.11 shows the bandstructure of InGaAs.

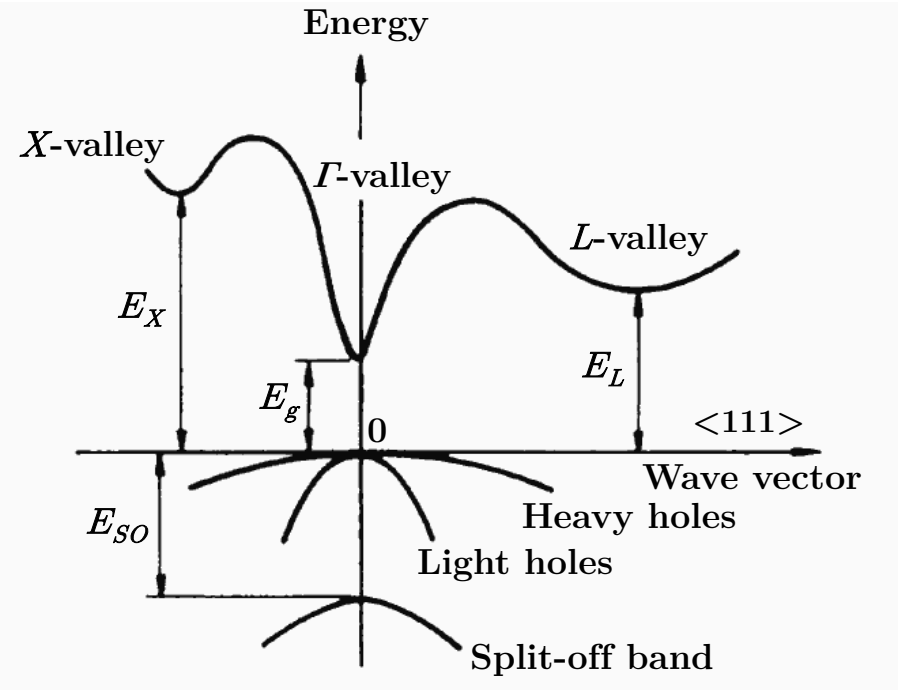

Figure 1.11: Band structure of InGaAs [34]

However, III-V materials have some issues too. The low effective masses lead to low Density of States (DOS) as

$$DOS_{2D} = \frac{2m^*}{\pi\hbar^2} n_v \tag{1.4}$$

where m^* is the DOS effective mass (for electrons in 2D, $m^* = \sqrt{m_t * m_t} = m_t$), n_v is the valley degeneracy and the factor 2 accounts for spin degeneracy. This "DOS Bottleneck" can limit the maximum I_{on} in the ballistic limit [35]. The contrast of the impact of the effective mass (m^*) on the v_{inj} and the DOS as seen from equations 1.3 and 1.4 signifies the trade-off inherent in these materials.

Material/ Property	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
m^*_{eff}	0.19	0.08	0.067	**0.041**	**0.023**	**0.014**
$\mu_n(cm^2/Vs)$	1400	3900	8500	**12,000**	**40,000**	**77,000**
$\mu_h(cm^2/Vs)$	450	1900	400	300	500	850
$E_g(eV)$	1.12	**0.66**	1.42	**0.74**	**0.354**	**0.17**
ε_r	11.7	**16.2**	12.9	**13.9**	**15.15**	**16.8**

Table 1.2: Physical properties of some Alternative Channel Materials at 300 K (Taken from [34])

In addition, the band gaps (E_g) of most of the high mobility channel materials are considerably low. Therefore the leakage currents in these devices are expected to increase exponentially. Also, the high dielectric constant of Ge and III-V materials will result in easier encroachment of the drain electric field into the channel, thereby causing more relative loss of gate control on the channel electrostatics and hence poor device characteristics.

1.2.3 Current Status of ACM Devices

Following the technological improvement and the potential performance increase of devices with Ge and III-V channels, successful fabrication of these high mobility material MOSFETs has already been achieved.

1.2.3.1 III-V MOSFET Architectures

During the course of the last few years, different architectures have been pursued by different academic and industrial groups for utilizing III-V compounds as channel materials. Some of the device structures are described below.

• Inversion Mode III-V MOSFETs (Surface Channel): It is a version of the bulk Si MOSFET with Si being replaced by III-V material, and the operating principles remain the same. Below the channel and source/drain implant layer, there exists a buffer layer followed by the substrate. Most devices demonstrated experimentally have been InGaAs based [36–39], although other

channel materials like GaAs based MOSFETs have also been fabricated [40]. Figures 1.12 and 1.13 show the schematics of such MOSFETs.

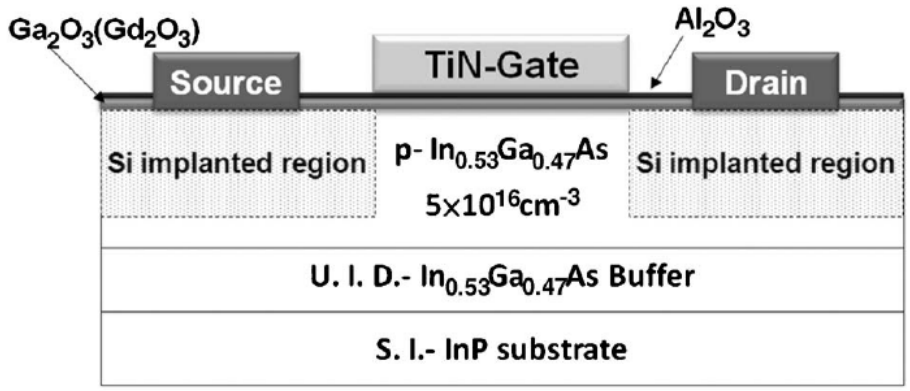

Figure 1.12: Schematic cross section of an $In_{0.53}Ga_{0.47}As$ MOSFET with TiN metal gate and Al_2O_3 /$Ga_2O_3(Gd_2O_3)$ dual-layer dielectric [36]

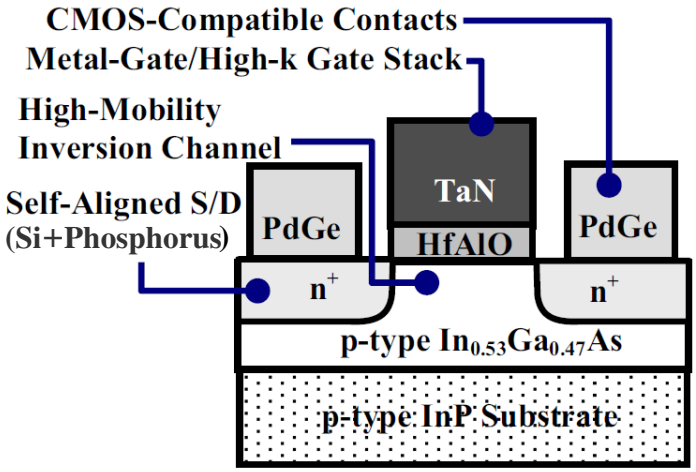

Figure 1.13: Schematic of an $In_{0.53}Ga_{0.47}As$-channel MOSFET with Gold-free ohmic contacts [41]

This architecture is well known and understood in the mainstream silicon

manufacturing community, hence it can be easily adapted to newer channel materials and it should have scalability similar to a bulk silicon MOSFET. But it has an obvious major issue: the presence of the inversion channel at the gate dielectric/III-V interface can result in a lower mobility due to interface roughness scattering. Another issue is that of the appreciably lower thermal budget of III-V layer ion implantation annealing process (higher temperatures would cause As outdiffusion resulting in degraded channel) leading to lower possible source/drain doping level and hence higher source/drain contact resistance [42], especially for thin channels.

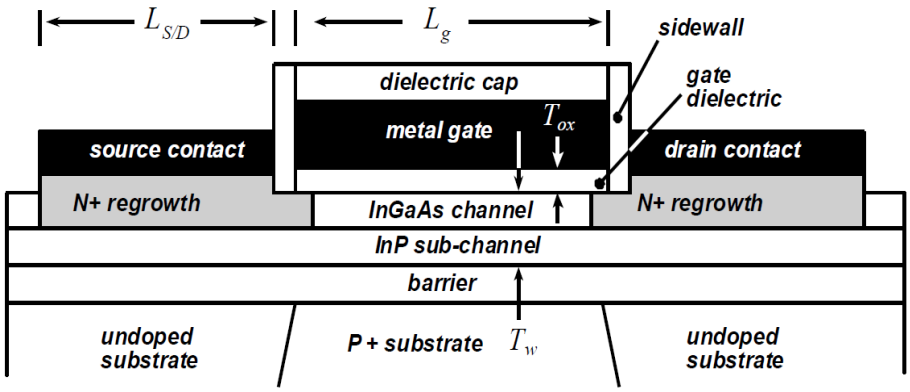

Figure 1.14: Cross-section of InP-based MOSFET with regrown extrinsic N^+ InGaAs/InAs source and drain regions. The gate stripe extends a distance W_g perpendicular to the figure. L_g is the gate length, T_{ox} the gate dielectric thickness, and T_w the thickness of the InGaAs/InP quantum well [43]

• QWFET (Quantum Well FET) with Regrown Source/Drain Architecture: The inherent problems with ion implanted S/D regions in a typical inversion mode device make it difficult to control the stoichiometry of the III-V channel, as mentioned in the previous section. To avoid this, one proposal is to keep essentially the same working principle, but have a fabrication process in which the S/D regions are formed by epitaxial growth after the patterning of the gate-stack, formation of gate dielectric sidewall spacers and etching out of the channel material in the desired S/D regions [43]. Also a high bandgap barrier layer is patterned below the channel layer for carrier con-

finement (hence the name QWFET, Quantum Well Field Effect Transistor). The cross section of a MOSFET with regrown InGaAs S/D regions is shown in Figure 1.14. However, this structure also suffers from the degradation of the channel mobility due to it being at the surface.

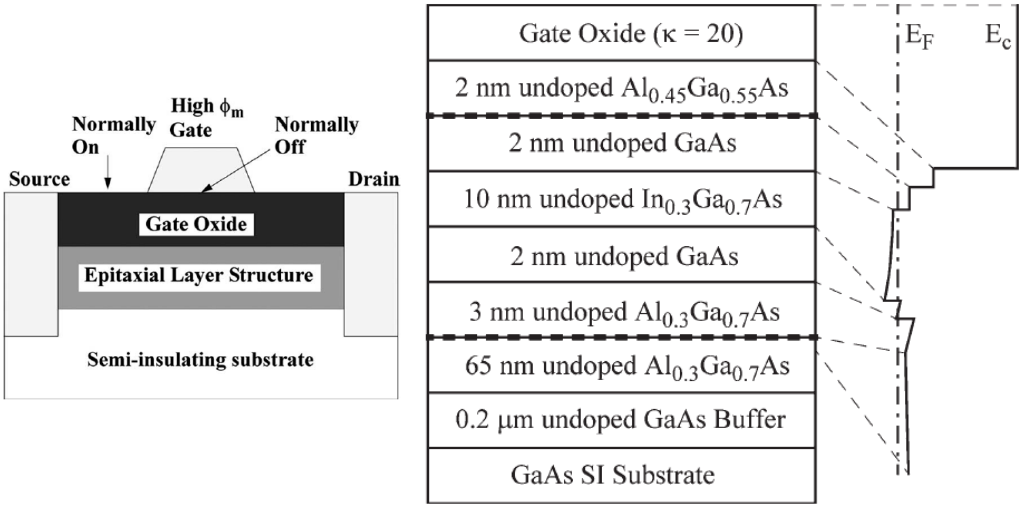

Figure 1.15: Left: Cross-sectional schematic illustration of an implant-free enhancement mode MOSFET. Ohmic-contact metal is deposited after gate-oxide removal, and the contacts are formed using conventional Ni/Ge/Au metallurgy. **Right**: Epitaxial-layer structure and energy-band diagram of an implant-free enhancement-mode MOSFET. δ-doped layers are placed at a certain distance below (bottom δ-doping) and/or above (top δ-doping) the $In_{0.3}Ga_{0.7}As$ channel layer as indicated by dashed lines. A representative energy-band diagram is shown for thermal equilibrium and under flatband conditions for t_{ox} = 18 nm and N_s = 2.4x10^{12} cm^{-2} (n_s = 2.3x10^{12}cm^{-2}). Taken from [44].

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• Flatband QWFET (Implant Free): This architecture is derived from the conventional HEMT device structure, where the high mobility, low band gap channel is buried between higher band gap materials, creating a quantum well channel. The spatial separation of the channel from the gate dielectric helps to avoid the mobility degradation due to poor quality of the gate/channel interface and Coulomb scattering. These devices are called "Flatband" QFETs because the device is in on-state under flatband condition ($\vec{E} = 0$ in the gate oxide). For an n-channel device, as the gate voltage is lowered below the threshold voltage, the channel goes into depletion. These are majority carrier devices and do not utilise the surface inversion concept of minority carrier

channel formation. An example of the layered epitaxial section is shown in Figure 1.15. While this architecture relaxes the need for a superior quality gate dielectric/channel interface, the ultimate scalability of this architecture is questionable due to the insertion of barrier layer between the gate and channel and the presence of δ-doping above the channel.

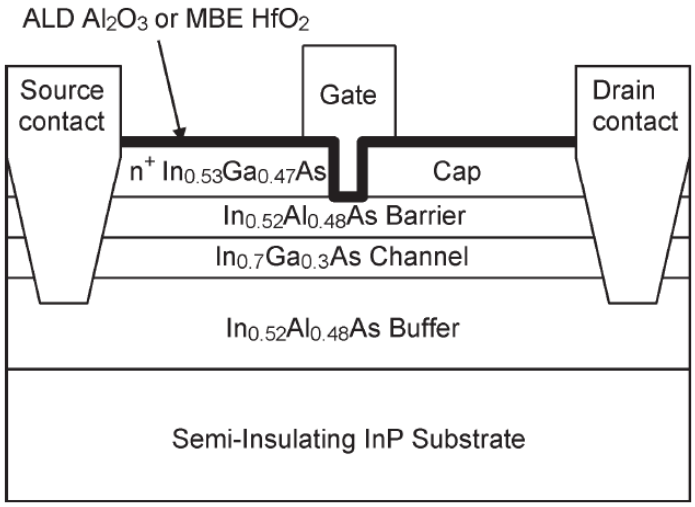

Figure 1.16: Schematic cross-sectional diagram of an enhancement-mode $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ MOSFET with 7-nm ALD Al_2O_3 (short channel device) or 10 nm MBE HfO_2 (long-channel device) [45]

• QWFET with Recessed Gate Architecture: This architecture has an undoped quantum well heterostructure layer, with gate-recess. For example the QWFET layer structure in Figure 1.16 consists of a $In_{0.52}Al_{0.48}As$ buffer layer (undoped), a thin $In_{0.7}Ga_{0.3}As$ strained quantum well (undoped), a $In_{0.52}Al_{0.48}As$ top barrier layer (undoped), and a capping layer of n^+ $In_{0.53}Ga_{0.47}As$. All these layers are grown on a semi-insulating InP substrate by molecular beam epitaxy (MBE) [45]. The n^+ cap layer is selectively etched to form a gate recess area. Being a buried channel device, it is less affected by the gate-oxide/semiconductor interface non-idealities. Also, unlike the Flatband QWFET, it does not use δ doping layer, hence the vertical scalability is better. This scheme has been used in conjunction with high-κ dielectric stack

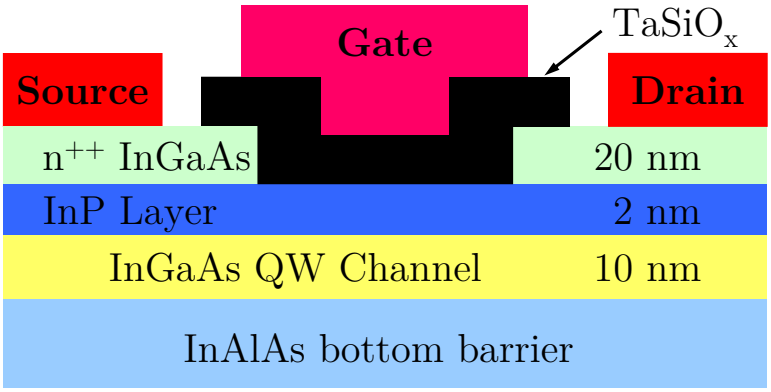

Figure 1.17: Schematic of planar, thin body, High-κ/Metal Gate $In_{0.7}Ga_{0.3}As$ MOSFET [46]

and metal gate to realize planar, tri-gate MOSFETs as well as TFETs, demonstrating excellent performance [46]. Figures 1.16 and 1.17 show examples of this kind of MOSFETs.

In this work, the considered device structure has been primarily a double gate MOSFET with a non silicon channel for the sake of modeling and understanding.

1.2.3.2 III-V and Si Heterogeneous Integration

To utilize the well established Si processing platform and for heterogeneous integration with other Si based components, one possibility worth considering is that of growing new high-mobility materials epitaxially on Si substrate. For example, [47] classifies the possibilities into the following different configurations:

- The 'More Moore' approach refers to continuing scaling and is geared towards achieving higher drive currents and has the prospects of Ge CMOS on insulator, III-V CMOS on insulator and III-V NMOS and Ge PMOS on insulator with silicon as the substrate.

- The 'More than Moore' approach is concerned with functional diver-

sification for non-digital content. It allows technology incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law", but provide additional value in different ways. Some examples are: III-V/Ge-on-insulator-on Si optical devices, ultra fast analog devices, sensors and MEMS.

- Going beyond CMOS, III-V/Ge tunnel FETs are also being pursued.

Figure 1.18 shows these options currently being researched: for both More Moore as well as More than Moore approaches.

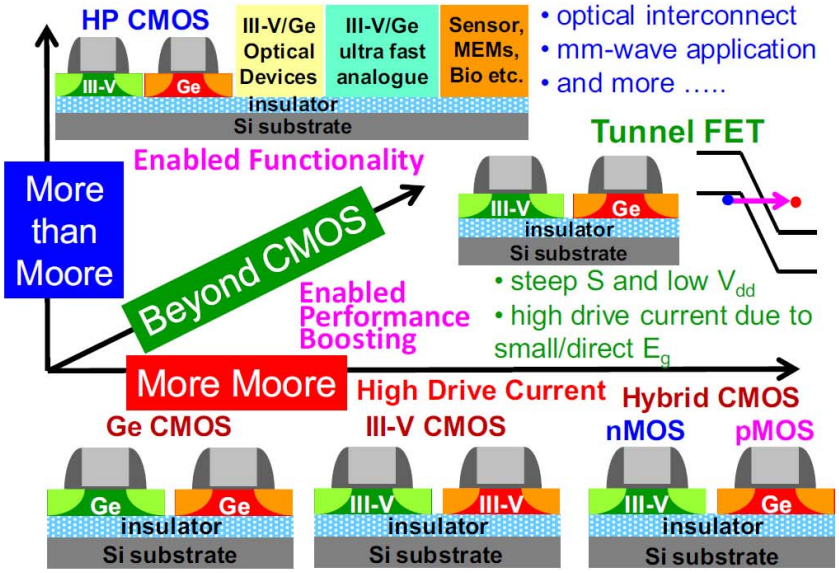

Figure 1.18: Possibilities for heterogeneous integration of ACM devices (III-V/Ge) on Si (Taken from [47])

1.3 Need to evaluate SCEs in III-V MOSFETs

III-V devices for logic applications are projected to be introduced beyond the 16 nm gate length according to PIDS 2011 predictions [8]. The short channel effects worsen and limit the device performance as we keep scaling. The impact of the extremely small separation between the source and the drain on the device performance can be analyzed through analytical modeling and

numerical simulation techniques.

Although III-V compounds offer higher mobilities, the impact of different effective masses and material parameters compared to Si needs to be investigated, so as to predict the scalability and margin of benifit compared to Si technology. The advantage of power consumption reduction possible with III-V technology against the degradation in short channel effects and increased leakage needs to be analyzed; and optimum channel lengths for introduction of III-V channels need to be determined.

1.4 Aim of the Thesis

The aim of this thesis, thus, is to examine these issues of MOSFETs with alternative channel materials from a modeling and simulation perspective. While doing so, the current technlogical limitations with regard to III-V device fabrication, stability and reliability will be ignored so as to treat a best case scenario, assuming the limitations will be overcome by the industry in the coming years, as has been done for Si technology in the past.

1.5 Organization of the Thesis

The rest of the thesis is organised as follows: The second chapter deals with modeling of the 2D channel potential in a double gate MOSFET. Then follows the main work of this thesis: the study of the role of quantum effects on SCEs in MOSFETs with alternative channel materials is described in chapter 3. The impact of source-to-drain tunneling on the scalability of III-V devices is examined in chapter 4. Finally, conclusions are drawn and some future perspectives are discussed in chapter 5.

Chapter 2

Modeling of the channel potential in a MOSFET

Contents

2.1 Introduction

The development of the transistor industry has always been accompanied by a need to develop physics based models, which can predict the behavior of

the transistors while giving insight into the underlying physical phenomena in the devices. Analytical models make it easy to understand the change in input and output characteristics as one varies different parameters of the device. It is particularly useful when one considers scaling the device: be it geometrical or V_{DD} or changing electrical parameters. Also, analytical models come in handy when we need MOSFET models for use in circuit simulators. Physically based analytical models of MOSFET channel potential are essential for rigorously capturing short channel effects [48], evaluating scaling behavior [49] and are required to evaluate subthreshold leakage [50].

The focus of this chapter is to look at some of the major techniques to model the channel potential, select an analytical model, demonstrate its efficacy for predicting the short channel effects (SCEs). We then discuss an issue with the boundary conditions in the existing models due to non inclusion of the Source/Drain regions of the MOSFET in the analysis, that results in erroneous evaluation of channel potential. The impact of the source and drain on the the potential and hence on the short channel effects (drain induced barrier lowering and subthreshold slope) will be investigated at first. A correction to the boundary conditions is proposed and incorporated into the channel potential model. The concept is then validated using numerical simulations.

2.2 Channel Potential Modeling

This section describes the analytical model of the channel potential developed by Tsormpatzoglou et al. [51] as an example of modeling the channel potential in a double gate MOSFET and the associated short channel effects.

2.2.1 Analytical Modeling

The schematic of the cross section of the device with the coordinate system used is shown in Figure 2.1

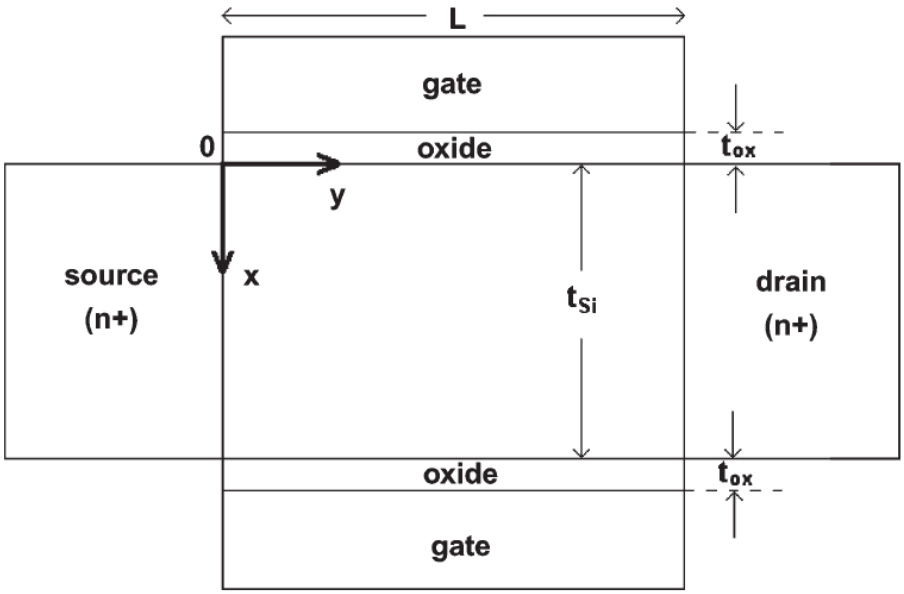

Figure 2.1: Device cross section with coordinate system

In the weak inversion region of operation, the channel potential can be described by the Poisson's equation as:

$$\frac{\partial^2 V(x,y)}{\partial x^2} + \frac{\partial^2 V(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{Si}}; \qquad 0 \leq x \leq t_{Si}, 0 \leq y \leq L \tag{2.1}$$

where N_a is the p-type doping concentration in the channel, ε_{Si} is the dielectric constant of silicon, t_{Si} is the channel thickness and L is the channel length.

For low values of drain voltage, the potential in the channel can be assumed to be a parabolic function:

$$V(x,y) = c_0(y) + c_1(y)x + c_2(y)x^2 \tag{2.2}$$

where c_1, c_2 and c_3 are functions of y alone. Since the potentials at the top and bottom channel/oxide interfaces are equal because of the symmetry of the device structure,

$$V_s(y) \equiv V(0,y) \equiv V(t_{Si},y) \tag{2.3}$$

And the boundary conditions are:

$$\left.\frac{dV(x,y)}{dx}\right|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_s(y)-V_g'}{t_{ox}} \tag{2.4a}$$

$$\left.\frac{dV(x,y)}{dx}\right|_{x=t_{Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_g'-V_s(y)}{t_{ox}} \tag{2.4b}$$

where $V_g' = V_g - V_{FB}$, V_g is the applied gate voltage, V_{FB} is the flatband voltage and ε_{ox} and t_{ox} are the dielectric constant and thickness of the gate oxide.

On solving the system of equations (2.2), (2.3) and (2.4), the coefficients c_i can be obtained as:

$$c_0 = V_s(y) \tag{2.5a}$$

$$c_1 = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_s(y)-V_g'}{t_{ox}} \tag{2.5b}$$

$$c_2 = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_g'-V_s(y)}{t_{ox}t_{Si}} \tag{2.5c}$$

Substituting coefficients from (2.5) in (2.2):

$$\frac{\partial^2 V(x,y)}{\partial x^2} = 2c_2 = 2\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_g'-V_s(y)}{t_{ox}t_{Si}} \tag{2.6a}$$

$$\frac{\partial^2 V(x,y)}{\partial y^2} = \frac{\partial^2 c_0}{\partial y^2} + x\frac{\partial^2 c_1}{\partial y^2} + x^2\frac{\partial^2 c_2}{\partial y^2} \tag{2.6b}$$

$$= \frac{\partial^2 V_s(y)}{\partial y^2} + x\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{1}{t_{ox}}\frac{\partial^2 V_s(y)}{\partial y^2} - x^2\frac{1}{t_{ox}t_{Si}}\frac{\partial^2 V_s(y)}{\partial y^2} \tag{2.6c}$$

$$= \frac{\partial^2 V_s(y)}{\partial y^2}\left[1 + \frac{x}{t_{ox}}\frac{\varepsilon_{ox}}{\varepsilon_{Si}} - \frac{x^2}{t_{ox}t_{Si}}\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\right] \tag{2.6d}$$

Using (2.6) in (2.1):

$$2\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_g'-V_s(y)}{t_{ox}t_{Si}} + \frac{\partial^2 V_s(y)}{\partial y^2}\left[1 + \frac{x}{t_{ox}}\frac{\varepsilon_{ox}}{\varepsilon_{Si}} - \frac{x^2}{t_{ox}t_{Si}}\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\right] = \frac{qN_a}{\varepsilon_S i} \tag{2.7}$$

$$\Rightarrow \frac{\partial^2 V_s(y)}{\partial y^2}\left[1+\frac{x}{t_{ox}}\frac{\varepsilon_{ox}}{\varepsilon_{Si}}-\frac{x^2}{t_{ox}t_{Si}}\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\right]-2\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_s(y)}{t_{ox}t_{Si}}=\frac{qN_a}{\varepsilon_S i}-2\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_g'}{t_{ox}t_{Si}} \tag{2.8}$$

$$\Rightarrow \frac{\partial^2 V_s(y)}{\partial y^2}\left[\varepsilon_{Si}t_{ox}t_{Si}+xt_{Si}\varepsilon_{ox}-x^2\varepsilon_{ox}\right]-2\varepsilon_{ox}V_s(y)=qN_a t_{ox}t_{Si}-2\varepsilon_{ox}V_g' \tag{2.9}$$

Thus, finally we get the following differential equation:

$$\frac{\mathrm{d}^2 V_s(y)}{\mathrm{d}y^2}-\alpha V_s(y)=\beta \tag{2.10}$$

where

$$\alpha=\frac{2\varepsilon_{ox}}{\varepsilon_{Si}t_{ox}t_{Si}+t_{Si}\varepsilon_{ox}x-\varepsilon_{ox}x^2}$$
$$\beta=\frac{qN_A t_{ox}t_{Si}-2\varepsilon_{ox}V_g'}{\varepsilon_{Si}t_{ox}t_{Si}+t_{Si}\varepsilon_{ox}x-\varepsilon_{ox}x^2}$$

The auxiliary equation is: $r^2-\alpha=0$, whose roots are: $\pm\sqrt{\alpha}$
Hence, the eneral solution is of the form:

$$V_s(y)=Ae^{\sqrt{\alpha}y}+Be^{-\sqrt{\alpha}y}$$

and the particular solution is of the form:

$$z(y)=\kappa$$

Hence we have: $z=\kappa$, $z'=0$ and $z''=0$
Using this in equation (2.10):

$$-\alpha\kappa=\beta\Rightarrow\kappa=-\beta/\alpha$$

Hence the complete solution is:

$$V_s(y)=Ae^{\sqrt{\alpha}y}+Be^{-\sqrt{\alpha}y}-\beta/\alpha$$

Since $V_s(y)$ is evaluated at $x = 0$, let

$$V_s(y) = Ae^{y/\lambda_1} + Be^{-y/\lambda_1} - \beta/\alpha \tag{2.11}$$

where

$$\lambda_1 = 1/\sqrt{\alpha}\big|_{x=0} = \sqrt{\frac{\varepsilon_{Si} t_{ox} t_{Si}}{2\varepsilon_{ox}}} \tag{2.12}$$

Let

$$A_1 = \kappa = -\beta/\alpha = V_g' - \frac{qN_a t_{Si} t_{ox}}{2\varepsilon_{ox}} \tag{2.13}$$

Now the following boundary conditions are applied for finding A and B:

$$V_s(y)\big|_{y=0} = V_{bi} \tag{2.14a}$$

$$V_s(y)\big|_{y=L} = V_{bi} + V_d \tag{2.14b}$$

where

$$V_{bi} = k_b T \ln\left(\frac{N_a N_d}{n_i^2}\right) \tag{2.15}$$

with k_b the Boltzmann constant, T the temperature, N_a the substrate doping, N_d the S/D doping, and n_i the intrinsic carrier concentration of the channel semiconductor material.

So we have:

$$V_{bi} = A + B + A_1 \Rightarrow A = V_{bi} - A_1 - B \tag{2.16a}$$

$$\begin{aligned} &V_{bi} + V_d = Ae^{L/\lambda_1} + Be^{-L/\lambda_1} + A_1 \\ &\Rightarrow (V_{bi} - A_1 - B)e^{L/\lambda_1} + Be^{L/\lambda_1} = V_{bi} + V_d - A_1 \\ &\Rightarrow B = \frac{V_{bi} + V_d - A_1 - (V_{bi} - A_1)e^{L/\lambda_1}}{e^{-L/\lambda_1} - e^{L/\lambda_1}} \end{aligned} \tag{2.16b}$$

Using (2.16) in (2.11):

$$\begin{aligned}
V_s(y) &= \left(V_{bi} - A_1 - \frac{V_{bi} + V_d - A_1 - (V_{bi} - A_1)e^{L/\lambda_1}}{e^{-L/\lambda_1} - e^{L/\lambda_1}} \right) e^{y/L} \\
&+ \left(\frac{V_{bi} + V_d - A_1 - (V_{bi} - A_1)e^{L/\lambda_1}}{e^{-L/\lambda_1} - e^{L/\lambda_1}} \right) e^{-y/\lambda_1} + A_1 \\
&= A_1 + (V_{bi} - A_1)e^{y/\lambda_1} \\
&+ \frac{V_{bi} + V_d - A_1 - (V_{bi} - A_1)e^{L/\lambda_1}}{e^{-L/\lambda_1} - e^{L/\lambda_1}} \left(e^{-y/\lambda_1} - e^{y/\lambda_1} \right) \\
&= A_1 + (V_{bi} - A_1)e^{y/\lambda_1} \\
&+ \frac{V_{bi} + V_d - A_1 - (V_{bi} - A_1)e^{2L/\lambda_1}}{e^{2L/\lambda_1} - 1} \left(e^{y/\lambda_1} - e^{-y/\lambda_1} \right)
\end{aligned}$$

Rearranging, the expression for the surface potential $V_s(y)$ is thus obtained as:

$$\begin{aligned}
V_s(y) \quad = \quad & \frac{1}{e^{\frac{2L}{\lambda_1}} - 1} \Bigg[(V_{bi} + V_d - A_1) \left(e^{\frac{L+y}{\lambda_1}} - e^{\frac{L-y}{\lambda_1}} \right) \\
& + (V_{bi} - A_1) \left(e^{\frac{2L-y}{\lambda_1}} - e^{\frac{y}{\lambda_1}} \right) \\
& + A_1 \left(e^{\frac{2L}{\lambda_1}} - 1 \right) \Bigg]
\end{aligned} \tag{2.17}$$

Here λ_1 can be recognized as the natural channel length as proposed by Yan et al. [52] and is used to characterize the short channel effects in a MOSFET.

Now for finding $V(x, y)$ from, (2.5) and (2.17) are used in (2.2):

$$V(x, y) = V_s(y) + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V_s(y) - V_g'}{t_{ox}} x + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{V_g' - V_s(y)}{t_{ox} t_{Si}} x^2 \tag{2.18}$$

Consider a point at a depth $x = t_{Si}/n (n \neq 0)$ and a given distance y along

the channel. The 2D potential $V(x,y) \equiv V_x(y)$ becomes:

$$V(x,y) = V_s(y)\left(1 + \frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{ox}n} - \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{t_{Si}}{t_{ox}n^2}\right) + V_g'\left(\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{t_{Si}}{t_{ox}n^2} - \frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{ox}n}\right) \tag{2.19}$$

$$= V_s(y)\left[1 + \frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{ox}}\left(\frac{n-1}{n^2}\right)\right] + V_g'\left[\frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{ox}}\left(\frac{1-n}{n^2}\right)\right] \tag{2.20}$$

Hence

$$V_s(y) = V(x,y)\left[1 + \frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{ox}}\left(\frac{n-1}{n^2}\right)\right]^{-1} + V_g'\left[\frac{\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{t_{Si}}{t_{ox}}\frac{n-1}{n^2}}{1 + \frac{\varepsilon_{ox}t_{Si}}{\varepsilon_{Si}t_{ox}}\frac{n-1}{n^2}}\right] \tag{2.21}$$

$$= k_1 V(x,y) + k_2 V_g' \tag{2.22}$$

$$= k_1 V_x(y) + k_2 V_g' \tag{2.23}$$

where

$$k_1 = \frac{1}{1 + \frac{\varepsilon_{ox}t_{Si}(n-1)}{\varepsilon_{Si}t_{ox}n^2}}, \qquad k_2 = \frac{1}{1 + \frac{\varepsilon_{Si}t_{ox}n^2}{\varepsilon_{ox}t_{Si}(n-1)}} \tag{2.24}$$

Now, going back to the differential equation obtained for $V_s(y)$, from equation (2.10)

$$\begin{aligned} &\tfrac{\mathrm{d}^2V_s(y)}{\mathrm{d}y^2} - \alpha V_s(y) = \beta \\ &\Rightarrow k_1\tfrac{\mathrm{d}^2V_x(y)}{\mathrm{d}y^2} - \alpha k_1 V_x(y) - \alpha k_2 V_g' = \beta \\ &\Rightarrow \tfrac{\mathrm{d}^2V_x(y)}{\mathrm{d}y^2} - \alpha V_x(y) = \frac{\beta + \alpha k_2 V_g'}{k_1} \end{aligned} \tag{2.25}$$

Let's define:

$$\alpha' = \alpha(x = t_{Si}/n) \tag{2.26}$$

$$= \frac{2\varepsilon_{ox}}{\varepsilon_{Si}t_{Si}t_{ox} + \frac{\varepsilon_{ox}{t_{Si}}^2}{n} - \frac{\varepsilon_{ox}{t_{Si}}^2}{n^2}} \tag{2.27}$$

$$\beta' = \left.\frac{\beta + \alpha k_2 V_g'}{k_1}\right|_{x=t_{Si}/n} \tag{2.28}$$

$$= \frac{\frac{qN_a t_{ox} t_{Si} - 2\varepsilon_{ox} V_g'}{\varepsilon_{Si} t_{ox} t_{Si} + \frac{t_{Si}\varepsilon_{ox} t_{Si}^2}{n} - \frac{\varepsilon_{ox} t_{Si}^2}{n^2}} + \frac{2\varepsilon_{ox} k_2 V_g'}{\varepsilon_{Si} t_{Si} t_{ox} + \frac{\varepsilon_{ox} t_{Si}^2}{n} - \frac{\varepsilon_{ox} t_{Si}^2}{n^2}}}{k_1} \tag{2.29}$$

Thus we now have the following differential equation for $V_x(y)$:

$$\frac{\mathrm{d}^2 V_x(y)}{\mathrm{d}y^2} - \alpha' V_x(y) = \beta' \tag{2.30}$$

To solve (2.30) we use the boundary conditions:

$$V_x(y)\big|_{y=0} = V_{bi}$$
$$V_x(y)\big|_{y=L} = V_{bi} + V_d$$

Since equation (2.30) is similar to equation (2.10), the solutions should be similar. We have

$$\lambda_2 = \sqrt{1/\alpha'} = \sqrt{\frac{\varepsilon_{Si} t_{ox} t_{Si} + \frac{\varepsilon_{ox} t_{Si}^2}{n} - \frac{\varepsilon_{ox} t_{Si}^2}{n^2}}{2\varepsilon_{ox}}} \tag{2.31a}$$

$$A_2 = -\frac{\beta'}{\alpha'} = \frac{2\varepsilon_{ox}(1-k_2)V_g' - qN_a t_{ox} t_{Si}}{2\varepsilon_{ox} k_1} \tag{2.31b}$$

$V_x(y)$ is obtained as:

$$\begin{aligned} V_x(y) \;=\; & \frac{1}{e^{\frac{2L}{\lambda_2}} - 1} \Bigg[(V_{bi} + V_d - A_2)\left(e^{\frac{L+y}{\lambda_2}} - e^{\frac{L-y}{\lambda_2}}\right) \\ & + (V_{bi} - A_1)\left(e^{\frac{2L-y}{\lambda_2}} - e^{\frac{y}{\lambda_2}}\right) \\ & + A_2\left(e^{\frac{2L}{\lambda_2}} - 1\right)\Bigg] \end{aligned} \tag{2.32}$$

Finally, we reexpress $V_x(y)$ as $V(x,y)$ by using (2.32) and (2.31), and switching

from (t_{Si}/n) to x:

$$\begin{aligned} V(x,y) &= \frac{1}{e^{\frac{2L}{\lambda_3}}-1}\Bigg[(V_{bi}+V_d-A_3)\left(e^{\frac{L+y}{\lambda_3}}-e^{\frac{L-y}{\lambda_3}}\right) \\ &\quad +\left(V_{bi}^S-A_3\right)\left(e^{\frac{2L-y}{\lambda_3}}-e^{\frac{y}{\lambda_3}}\right) \\ &\quad +A_3\left(e^{\frac{2L}{\lambda_3}}-1\right)\Bigg] \end{aligned} \tag{2.33}$$

where

$$A_3 = V_g' - qN_A\frac{\varepsilon_{Si}t_{ox}t_{Si}+\varepsilon_{ox}\left(t_{Si}-x\right)x}{2\varepsilon_{ox}\varepsilon_{Si}} \tag{2.34a}$$

$$\lambda_3 = \sqrt{\frac{\varepsilon_{Si}t_{ox}t_{Si}}{2\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{x}{t_{ox}}-\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{x^2}{t_{ox}t_{Si}}\right)} \tag{2.34b}$$

Here, A_3 can be shown to be the long channel surface potential and λ_3 is the scale length.

2.2.2 Concept of the extra potential in a short channel MOSFET

A short channel MOSFET's potential distribution can be seen to be incremented by an extra amount relative to the long channel case. The potential in the short channel case, $V(x,y)$ is reduced to the long channel case, $V_{long}(x) = A_3$ (which can be obtained on solving (2.1)-(2.4) under the assumption of constant potential in the direction along the channel.) Thus there is a 2D extra potential, $\Delta V(x,y) = V(x,y) - V_{long}(x)$ which is attributed to the SCEs and can be expressed as:

$$\begin{aligned} \Delta V(x,y) &= \frac{1}{e^{\frac{2L}{\lambda_3}}-1}\Bigg[(V_{bi}+V_d-A_3)\left(e^{\frac{L+y}{\lambda_3}}-e^{\frac{L-y}{\lambda_3}}\right) \\ &\quad +\left(V_{bi}-A_3\right)\left(e^{\frac{2L-y}{\lambda_3}}-e^{\frac{y}{\lambda_3}}\right)\Bigg] \end{aligned} \tag{2.35}$$

2.2.3 FlexPDE Numerical Simulation

The partial differential equation solver FlexPDE was used for carrying out the numerical simulations. FlexPDE is a "scripted finite element model builder and numerical solver" [53]. A symbolic equation analyzer expands defined parameters and equations, performs spatial differentiation, and symbolically applies integration by parts to reduce second order terms to create symbolic Galerkin equations. It then symbolically differentiates these equations to form the Jacobian coupling matrix. Its mesh generation facility generates an unstructured a triangular finite element mesh over a two-dimensional problem domain (as in this work). The finite element numerical analysis module selects the appropriate solution scheme. The adequacy of the mesh is consistently evaluated by an adaptive mesh refinement procedure and the mesh is refined whenever there is large error. The system iterates the mesh refinement and solution until a user-defined error tolerance is achieved. It has graphical output facility for plotting the output and a data export facility to write the solution data to text files. The mesh density can be user controlled. The typical structure simulated looks like the one in Figure 2.2

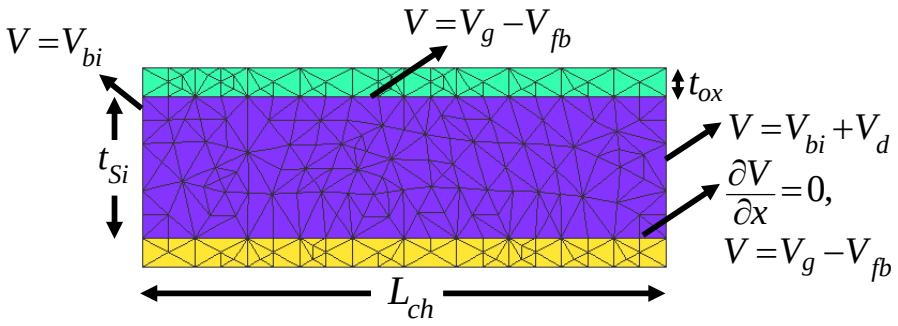

Figure 2.2: FlexPDE Simulation Structure

In this work the main equations solved in the FleXPDE simulations are:

Poisson's Equation:

$$\nabla \cdot (\nabla V) = -\frac{\rho}{\varepsilon} \tag{2.36}$$

Drift Diffusion:

$$\nabla \cdot qn\mu\nabla V_n = 0 \tag{2.37}$$

Drain Current :

$$I_d = \left| \frac{\int qn\mu dV_n}{L} \right| \tag{2.38}$$

The following Boltzmann distributions were assumed for the charge:

In the source region:

$$\rho = q\left(p_0 e^{-(V-V_{bi}-V_d)/kT} - n_0 e^{(V-V_{bi}-V_d)/kT} + N_d\right)$$

In the channel:

$$\rho = q\left(p_0 e^{-V/kT} - n_0 e^{V/kT} - N_a\right)$$

In the drain region:

$$\rho = q\left(p_0 e^{-(V-V_{bi})/kT} - n_0 e^{(V-V_{bi})/kT} + N_d\right)$$

2.2.4 Comparison: Model Vs Numerical Simulation

The analytical model for the channel potential is compared with the potential obtained from numerical simulation. They are found to be in agreement, validating the model for good L_g/t_{Si} ratios. Figure 2.3 compares the center channel potential and the surface potential for a MOSFET with 25 nm gate length, while Figure 2.4 shows the comparison of the minimum surface potential (or top of the barrier) as a function of the gate length for three different channel thicknesses.

2.3 The Question of Boundary Conditions

Recently, a detailed review and critic of these models has been published in [54], showing that, even 40 years after the first SCEs analytical models,

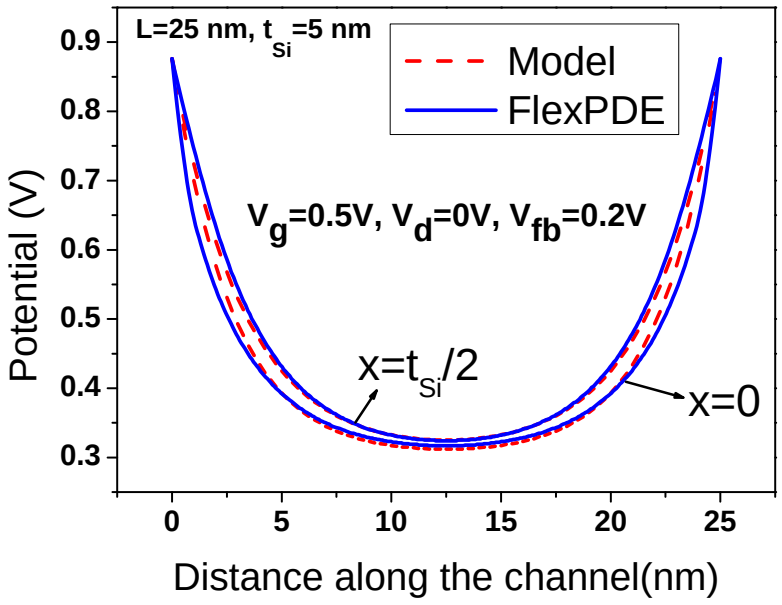

Figure 2.3: Comparison of the potential at the center and at the surface of the channel showing the agreement between numerical solution of 2D Poisson's equation and the analytical model (t_{Si}=5 nm, V_g=0.5 V, V_d=0 V, V_{fb}=0.2 V)

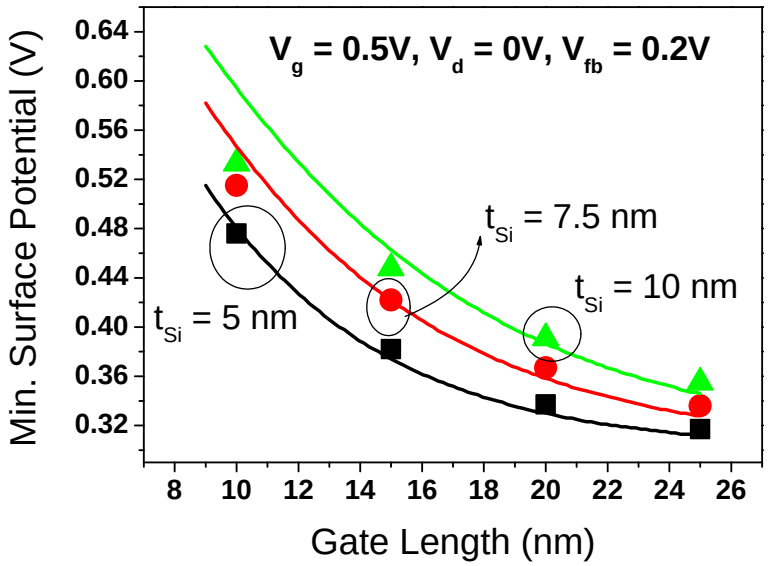

Figure 2.4: Comparison of the minimum surface potential as a function of the channel length obtained using numerical solution of 2D Poisson's equation and the analytical model for three values of channel thickness. Solid curves correspond to the model and the symbols correspond to the numerical simulations. (V_g=0.5 V, V_d=0 V, V_{fb}=0.2 V, t_{Si}=5 nm, 7.5 nm, 10 nm)

no consensus has been reached regarding the most efficient and rigorous approach. In this review however, Xie et al. have classified different types of models and in particular, the models based on polynomial description or based on the analytical solution of the 2D Poisson equation have been identified has the most suitable to reproduce SCEs, as they capture the impact of the oxide thickness [54]. All these models [48,51] use the built-in potential as boundary condition for the potential at the source/channel and drain/channel interface, thus allowing to neglect the role of source and drain on the potential, assuming source drain as very highly doped or almost metallic. Implicitly, this type of boundary condition assumes that there are no voltage drops in the source and drain and hence that the doping of the source and drain is very high.

To evaluate short channel effects, numerical simulations are at first carried out using the 2D partial differential equation solver, FlexPDE. Poisson and drift-diffusion equations are self-consistently solved in two cases: the first one includes the source/drain regions and boundary conditions for the potential are set as V_{bi} and V_{bi}+V_d respectively, at the beginning of the source and at the end of the drain, as shown in Figure 2.5. The second one does not take source and drain into account. As shown in Figure 2.5, in this case, V_{bi} and V_{bi} + V_d are applied as boundary condition for the potential, at the source and drain end of the channel respectively, as assumed by all SCE models [54]

The devices used in the study are double gate MOSFETs with gate lengths of 10, 15 and 20 nm and channel thicknesses of 3, and 5 nm with 2 nm thick gate oxides. Doping levels in the source and drain are set between 10^{24} to 10^{25} m^{-3} in the simulations.

2.3.1 Impact of the Source/Drain regions on SCEs

The DIBL and the subthreshold slope (SS) of the double gate devices simulated using the self-consistent solution of the DD and Poisson equation are shown in Figure 2.6. Cleary, excluding the source/drain region by applying V_{bi} and V_{bi} + V_d as potential boundary conditions at the edges of the channel, results in a huge overestimation of the SCEs. The DIBL and SS are found to be lesser in the case where S/D regions are included, with V_{bi} and V_{bi} + V_d

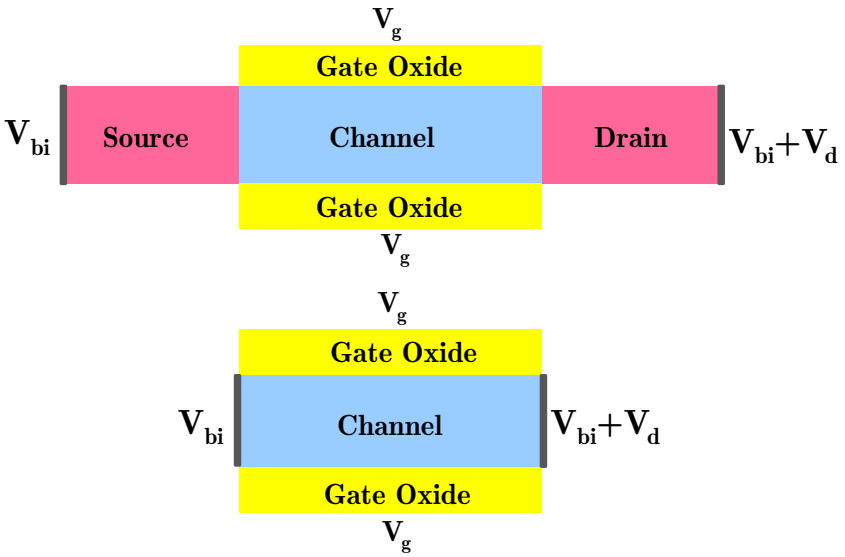

Figure 2.5: Boundary conditions applied to a MOSFET in two cases of analysis: including the S/D region and excluding the S/D region

applied on the outside edges of the source and drain.

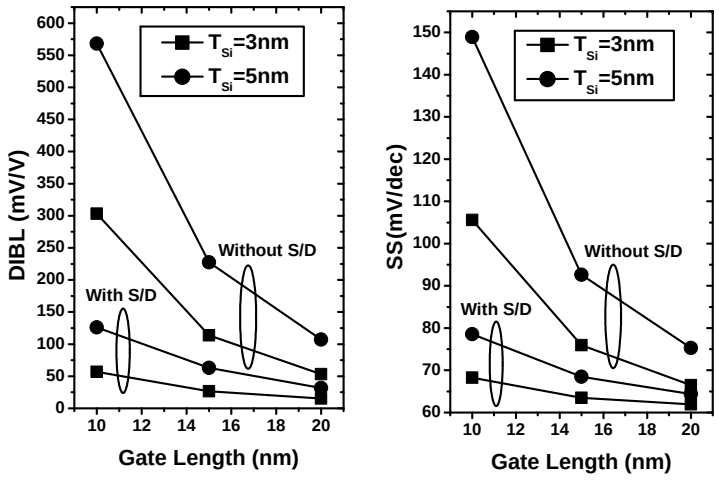

Figure 2.6: DIBL and SS as functions of channel length with or without S/D, for two channel thicknesses (DD simulations)

This result, hence indicates that the boundary conditions used in existing

analytical models of SCEs are not correct and result in overestimation of the values of the SCEs.

2.3.2 Electrostatics: Variation of the minimum of channel potential (top of the barrier)

To further understand the role of the S/D regions on the electrostatics of the device, Poisson equation has been solved in the same architectures, without the drift diffusion equation (no carrier transport), with the same boundary condition on the potential. From these electrostatic simulations, the variation of the minimum of the potential (or top of energy the barrier) has been extracted as a function of the gate and drain voltage.

Figure 2.7 shows the potential distribution at different gate voltages and the movement of the minimum of the potential, V_{min}. The value of V_{min}, obtained with the same simulated devices, has been plotted as a function of the gate voltage in Figure 2.8. The variation of V_{min} with V_g can be seen as an indirect evaluation of the subthreshold slope.

It can be seen that the slopes of the V_{min} Vs V_g plots are weaker when the S/D region are excluded than when they are included. This difference is enhanced for shorter gate lengths.

Further, as shown in Figure 2.9, ΔV_{min} is the change in the minimum channel potential as the drain voltage changes from V_d=0 V to V_d = 0.9 V.

$$\Delta V_{min} = V_{min}(V_d = 0.9V) - V_{min}(V_d = 0V) \tag{2.39}$$

Hence ΔV_{min} can be seen as an indirect estimation of the DIBL. The variation of this change in the minimum of the potential, ΔV_{min} per unit of the shift in drain voltage ($\Delta V_d = 0.9$ V) has been plotted as a function of the gate length in Figure 2.10 (the same device geometry has been used). It can be seen that it is larger when the source/drain region are neglected, and smaller when the source/drain region are included in the simulation.

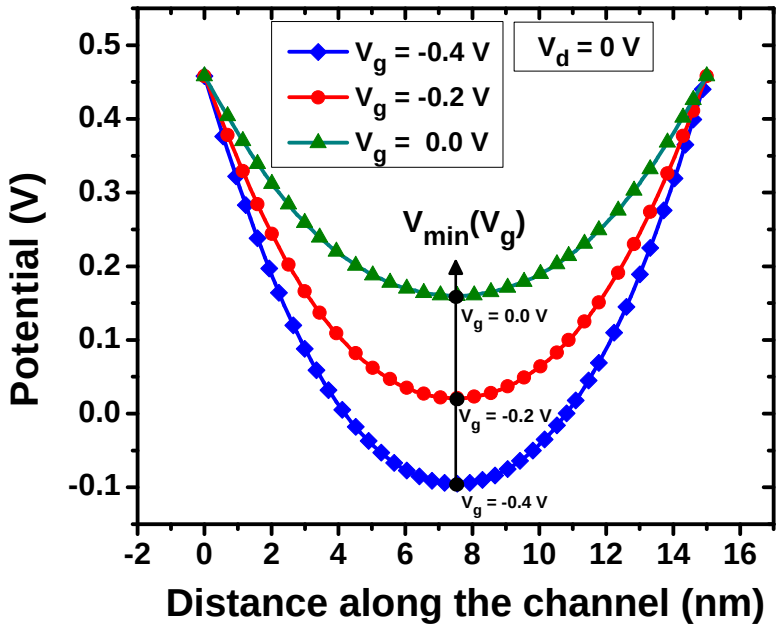

Figure 2.7: Variation of V_{min} with gate voltage, V_g at fixed drain voltage (excluding S/D).

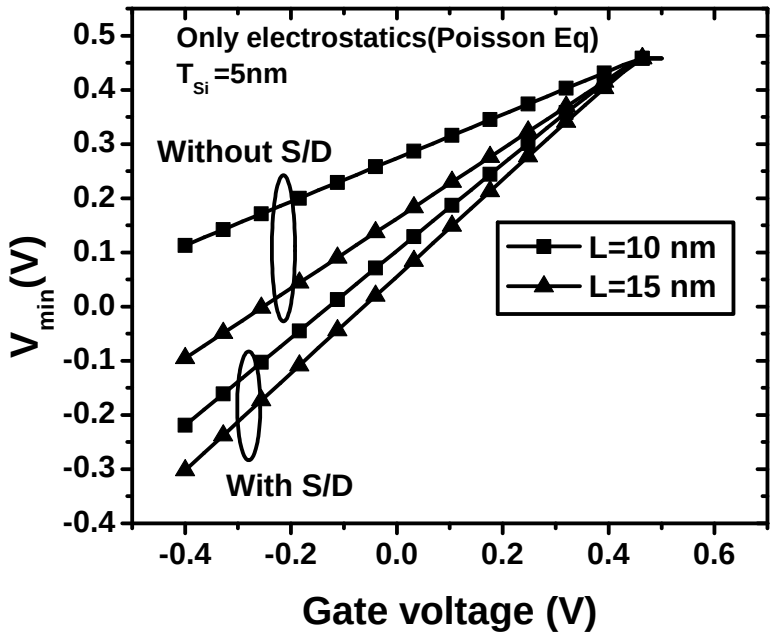

Figure 2.8: Minimum of the channel potential as a function of gate voltage (the slope being the SS equivalent) for two different channel lengths in the two cases of with/without S/D inclusion

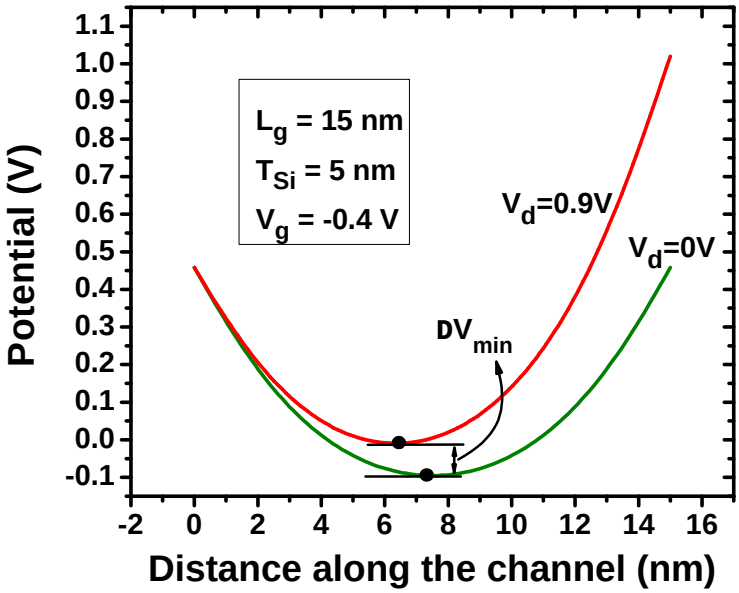

Figure 2.9: ΔV_{min} is the difference in the minimum channel potentials at V_d=0 V and V_d=0.9 V (excluding S/D)

These two results demonstrate that the overestimation of the SCEs obtained by applying V_{bi} and $V_{bi} + V_d$ as potential boundary conditions at the edges of the channel in the self-consistent solution of the DD and Poisson simulation originates from purely electrostatic effects.

2.4 Effective Built-In Potential, V_{bi}^{eff}

Two strategies are then possible to include the impact of the source/drain regions in the analytical modeling of the channel potential. Either new analytical models need to be developed, which would include the S/D in the solution of the Poisson equation. Or, the same modeling structure could be kept and new boundary conditions at the edge of the channel could be used in order to fit the simulations which include the S/D regions.

To evaluate the feasibility of the second strategy, Poisson simulations of the architecture without S/D have been carried out with arbitrarily modified

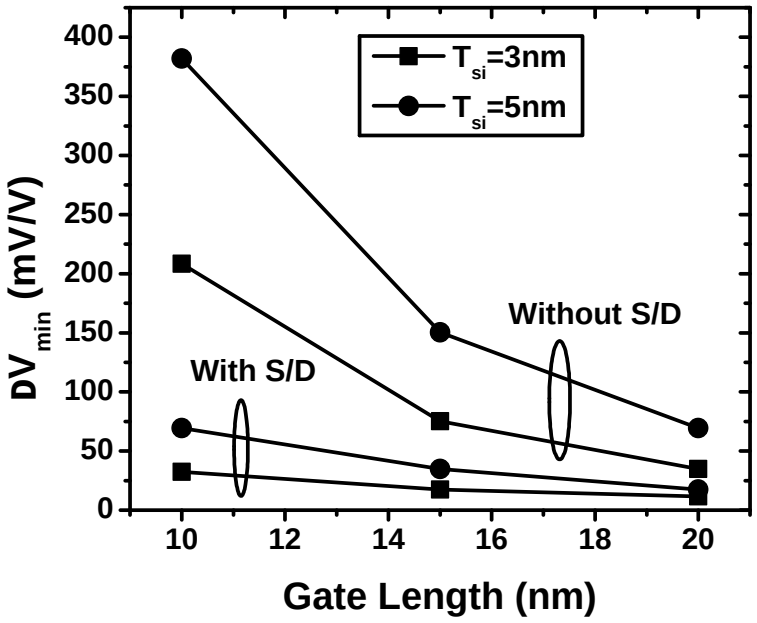

Figure 2.10: ΔV_{min} per unit of ΔV_d (DIBL equivalent) as a function of channel length, in two cases of with or without S/D inclusion, and two channel thicknesses, while solving only Poisson's equation

value of V_{bi}, in order to reproduce the channel potential of simulation obtained with the S/D region. The results of these simulations are plotted in Figure 2.11, which shows the channel potential along the S/D direction.

It can be seen that, when using two modified built-in potential values, designated here as $V_{bi}^{eff,S/D}$, the channel potential obtained neglecting the S/D matches with the potential obtained while including the S/D. This result suggests that it is possible to fit the results obtained including the S/D region, by using the right boundary conditions. Therefore, an analytical model of the effective build-in potential should be sufficient to correct the already existing analytical models of the channel potential and hence of the short channel effects.

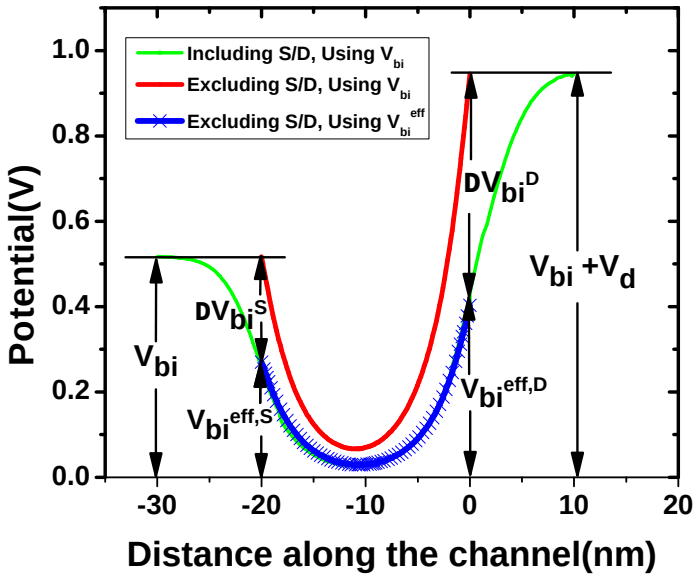

Figure 2.11: Channel potential in three cases: S/D included with V_{bi}, S/D excluded with V_{bi}, and S/D excluded with V_{bi}^{eff}, $(V_g = 0V)$

2.4.1 Analytical Modeling of V_{bi}^{eff}

To model $V_{bi}{}^{eff}$, the voltage drop ΔV_{bi} at the source/channel and channel/drain junction needs to be found, as:

$$V_{bi}^{eff,S/D} = V_{bi} - \Delta V_{bi}^{S/D} \tag{2.40}$$

The Poisson simulation carried out in section 2.3 indicates that the charge in the S/D region mainly results from depleted layers. Therefore, the field at the source/channel and channel/drain interface, but still in the S/D region, is simply given by [33]:

$$\begin{aligned} F\left(x = 0^{-}\right) &= \sqrt{\tfrac{2q}{\varepsilon_s} N_d \Delta V_{bi}^{S}} \\ F\left(x = L_g^{+}\right) &= -\sqrt{\tfrac{2q}{\varepsilon_s} N_d \Delta V_{bi}^{D}} \end{aligned} \tag{2.41}$$

where q is the elementary charge, ε_s the semiconductor dielectric constant. $\Delta V_{bi}{}^{S}$ and $\Delta V_{bi}{}^{D}$ are different voltage drops as they depend on the applied source/drain voltages as seen in Figure 2.11.

$\Delta V_{bi}{}^{S/D}$ can then be found by equating the field on each side of the junctions. This is easily accomplished by using closed form analytical model of the channel potential. In this work, the model proposed in [51] has been used to find ΔV_{bi}. This can however be also be done with other models, such like the often quoted Liu model [48].

The equation of V(x,y) given by equation (2.33) is used at first. The equation of the field can then be obtained as:

$$\begin{aligned} |F| \;=\; & \frac{1}{\left(e^{\frac{2L}{\lambda_3}}-1\right)\lambda_3}\left[\left(V_{bi}^{D}+V_D-A_3\right)\left(e^{\frac{L+y}{\lambda_3}}-e^{\frac{L-y}{\lambda_3}}\right)\right. \\ & \left.+\left(V_{bi}^{S}-A_3\right)\left(e^{\frac{2L-y}{\lambda_3}}-e^{\frac{y}{\lambda_3}}\right)\right] \end{aligned} \tag{2.42}$$

From (2.42), it is found that:

$$\begin{aligned} F\left(x=0^{+}\right) &= \frac{\left(V_{bi}^{S}-A_3\right)}{\lambda_3} \\ F\left(x=L_g^{-}\right) &= -\frac{\left(V_{bi}^{D}+V_D-A_3\right)}{\lambda_3} \end{aligned} \tag{2.43}$$

By equating (2.41) and (2.43) at $x=0$ and $x=L_g$, an expression of ΔV_{bi} is obtained as:

$$\begin{aligned} \Delta V_{bi}^{S/D} &= V_{bi}+V_{S/D}-A_3 \\ &\quad +{\lambda_3}^2\frac{q}{\varepsilon_s}N_d\left[1-\sqrt{1+\frac{2(V_{bi}+V_{S/D}-A_3)}{{\lambda_3}^2\frac{q}{\varepsilon_s}N_d}}\right] \end{aligned} \tag{2.44}$$

2.5 Impact of the Source/Drain doping

Self-consistent DD and Poisson simulations are carried out for two different source/drain doping concentrations, N_d using the same simulation framework and same template structure as in section 2.3.The DIBL and SS obtained are reported in Figure 2.12. It can be seen that higher value of the doping concentration slightly reduced the difference between the two. It means that

using the conventional boundary conditions result in more erroneous results as the source/drain doping is reduced.

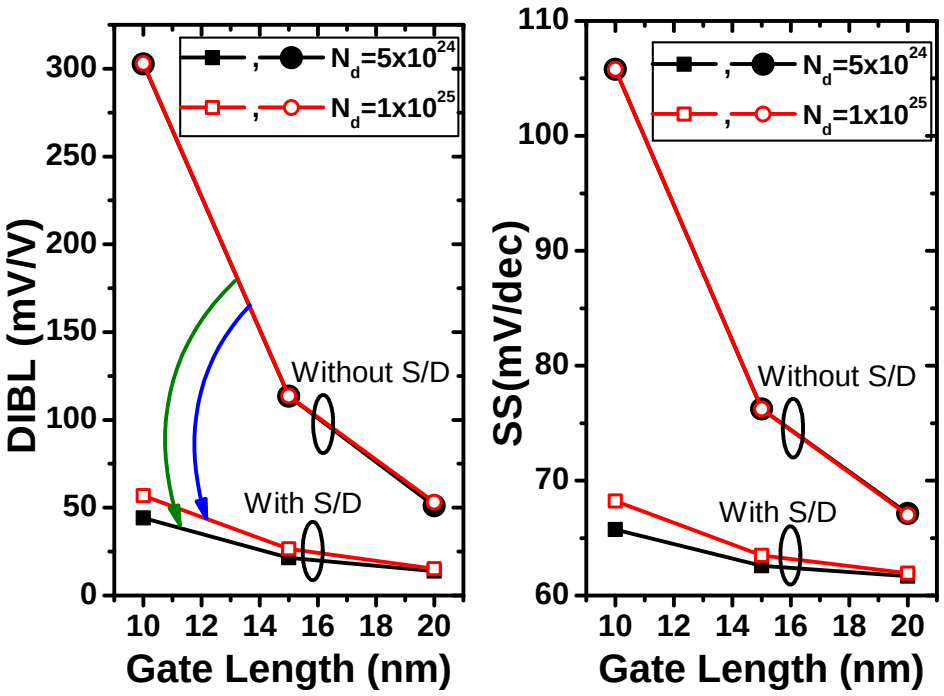

Figure 2.12: Variation of DIBL and SS with channel length with different N_d

It can be explained as an increse in the effective channel length of the MOSFETs since at conditions of low doping levels and depletion in source/drain regions, the channel-source/drain boundary shifts from the ideal case of degenerate doping in the source/drain. And the increased effective channel length leads to improved short channel effects. This can be very relevant for SCE calculations for some III-V devices where it's difficult to highly dope the source/drain regions due to limited thermal budget, as mentioned previously in section 1.2.3

Further, using the model derived in the previous section, ΔV_{bi} was calculated for different channel materials (different dielectric constants and band gaps) as a function of source/drain doping concentrations. The results are plotted in Figure 2.13.

It can be seen that the ΔV_{bi} increases with the N_d, at the same rate

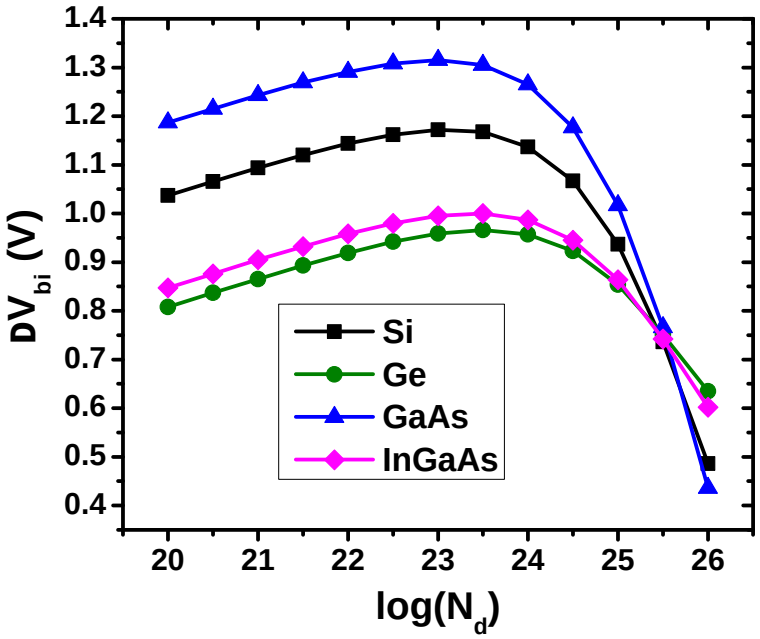

Figure 2.13: Variation of ΔV_{bi} with N_d (m^{-3}) for different channel materials

for each material till a doping concentration of around 10^{23} m^{-3} and starts to decrease afterwards, but with different slopes, the steepness of the slopes being proportional to the bandgaps of the materials. It's because the V_{bi} for each material can be represented as function of the band gaps as:

$$V_{bi}(\Delta E_g) = \frac{kT}{q} ln \left(\frac{N_a N_d}{{n_{i,Si}}^2} \right) + \Delta E_g \quad \text{where} \tag{2.45}$$

$$\Delta E_g = E_{g,sc} - E_{g,Si} \tag{2.46}$$

This, in conjunction with the doping levels, affects the V_{FB}, and hence V_g' and A_3, and finally ΔV_{bi}.

2.6 Corrected Short Channel Effects

The short channel effects of the same template structure used in section 2.3 have been recalculated using the corrected effective built-in potential, given by equations (2.40) and (2.44), for the architecture excluding the S/D region. As shown in Figure 2.14, the results obtained by neglecting the S/D region but using the built-in potential correction are now perfectly fitting the results

obtained with the architecture including the S/D.

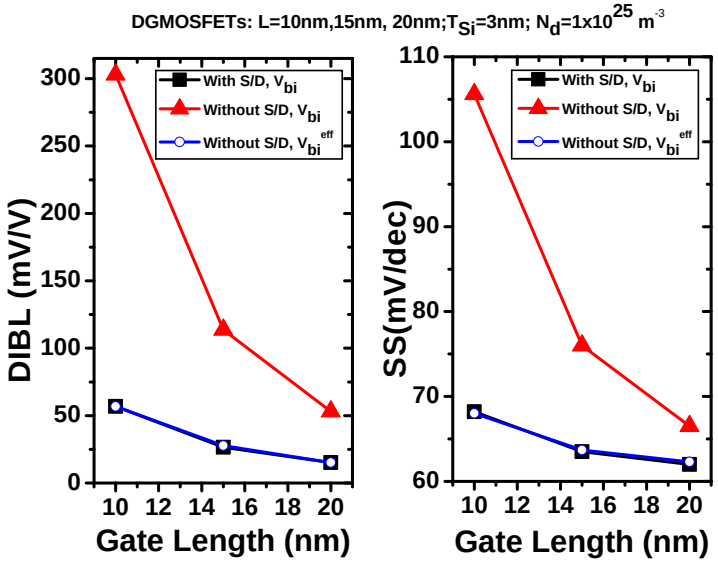

Figure 2.14: Comparison of SCEs obtained in the three cases: S/D included with V_{bi}, S/D excluded with V_{bi},, and S/D excluded with $V_{bi}{}^{eff}$

This demonstrates that the overestimation of the short channel effects, caused by neglecting the voltage drop resulting from the depletion layer in the source and drain, can be simply corrected by using the effective built-in potential formula obtained in (2.40) and (2.44). This also allows to correct most of the already proposed analytical models of the short channel effects.

2.7 Conclusion

In this chapter, the effect of the inclusion of the source/drain regions of a MOSFET on the channel potential modeling has been investigated. It has been found that in the conventional modeling approaches, the exclusion of the S/D regions leads to an overestimation of the SCEs. It is hence essential to include the S/D regions for obtaining realistic values of the potential distribution and the SCEs. This can be achieved by using an already existing model, but by replacing the built-in potential value by a modified one, proposed in

this chapter. This approach can be extended to other models and devices (e.g. TFETs)

Chapter 3

Origin of SCE increase in III-V MOSFETs

Contents

3.1 SCEs in III-V MOSFETs

The replacement of silicon as channel material by III-V semiconductors has emerged as a realistic option for the end of the roadmap of CMOS as discussed in Chapter 1. However, simulations and experimental results have

shown that III-V technologies are subject to enhanced short channel effects, including larger V_t roll-off, larger drain induced barrier lowering and subthreshold slope than the silicon devices [51, 55–57], which might compromise their use for the end of the roadmap of CMOS devices [49]. In particular, references [56] and [51] have shown by numerical simulation and analytical modeling that the subthreshold slopes of Ge and III-V MOSFET were larger than in Si, and [57] has demonstrated that $In_{0.7}Ga_{0.3}As$ Quantum Well FETs present poor scalability for the same reason.

In addition to the increased SCEs, it has been shown by the means of simulation that quantum confinement in III-V channel is enhanced [58, 59]. Indeed, due to the smaller effective masses and hence the smaller density of states (DOS) of these semiconductors, a larger degradation of the gate coupling with the channel is expected with respect to silicon channel [60]. This effect is shown to result in an increased electrical Equivalent Oxide Thickness (EOT) with respect to the physical oxide thickness, phenomenon also called dark space [58, 59, 61]. The concept of dark space has been explained in section 3.2.1

Recently published results [62, 63] have stated that the quantum effects could impact the short channel effects in the subthreshold regime. However, these results are questionable as the approach used in these works consists in comparing a classical simulator, an analytical model based on Poisson-Schrödinger fitting and quantum corrected TCAD simulation. These different codes are known to show some significant divergences and should be carried out with care, as done in [64] for different quantum confinement codes or in [65] for different codes of transport in nanoscale nMOSFET.

Moreover, SCEs have been shown to have a detrimental impact on inverter performances in the strong inversion regime. Indeed, it has been shown in [66, 67] that the SCEs in strong inversion regime, and especially the non saturation of the drain current caused by the Drain Induced Barrier Lowering (DIBL) could severely degrade the delay and propagation time of inverter and ring oscillator. Therefore, a comprehensive evaluation of the impact of SCEs in III-

Vs should not be limited to the subthreshold regime only, as carried out in [49, 51,56,57,68], but should also include strong inversion. In this regime however, the impact of quantization on the inversion charge is no longer negligible, which raises the question of role of quantum effect on the DIBL in strong inversion.

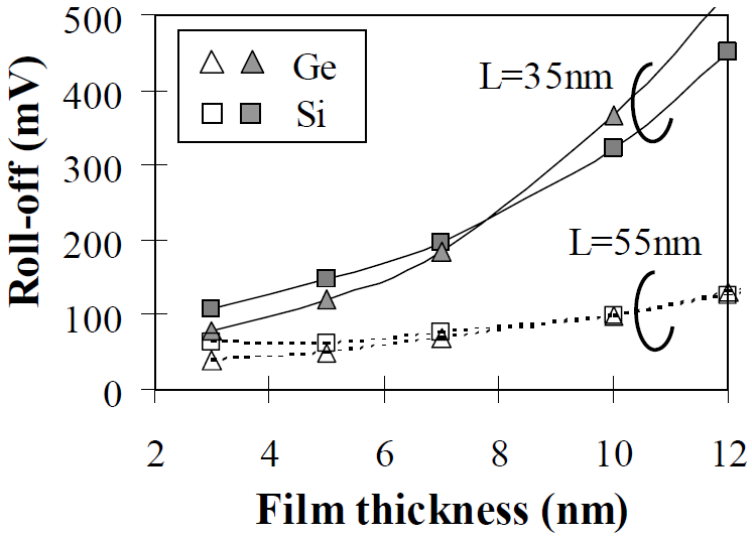

Figure 3.1: SCEs in Ge and Si as reported by Batail et al. [68]

Two questions hence still remain open:

- Do quantum effects impact the short channel effects in the subthreshold regime?

- Do quantum effects impact the DIBL in the strong inversion regime?

Therefore, SCEs in subthreshold regime will be investigated in section 3.2 of this chapter, with and without including quantum effects. Impact of material parameters is explored in section 3.3. Finally, section 3.4 will then present the role quantum effects on the DIBL in strong inversion regime.

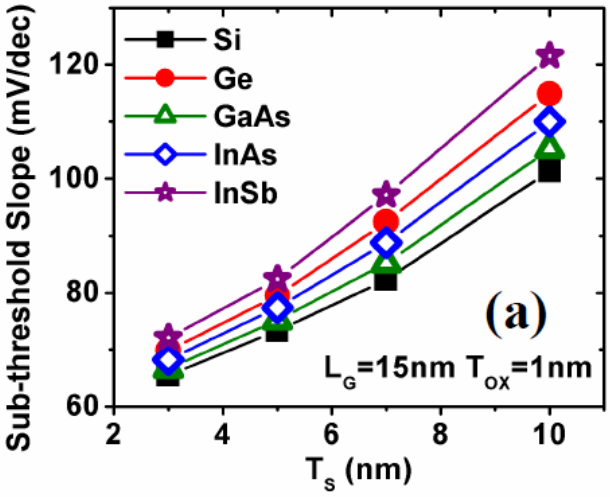

Figure 3.2: SCEs as reported by Pethe et al. [56]

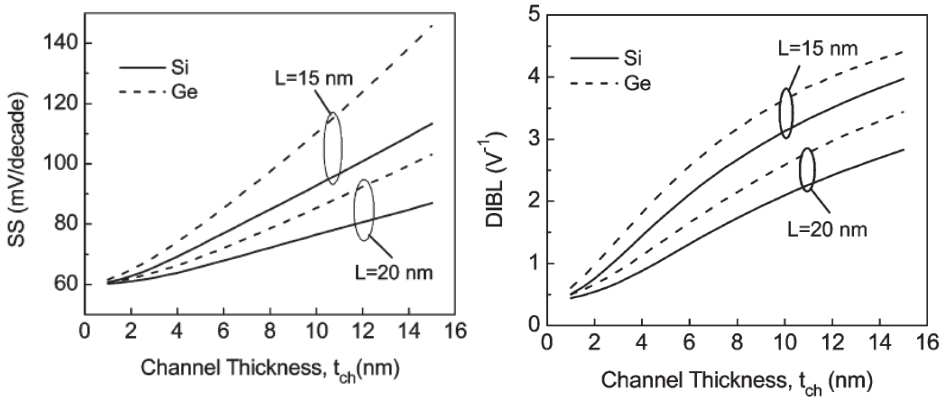

Figure 3.3: SCEs as reported by Tsormpatzoglou et al. [51]

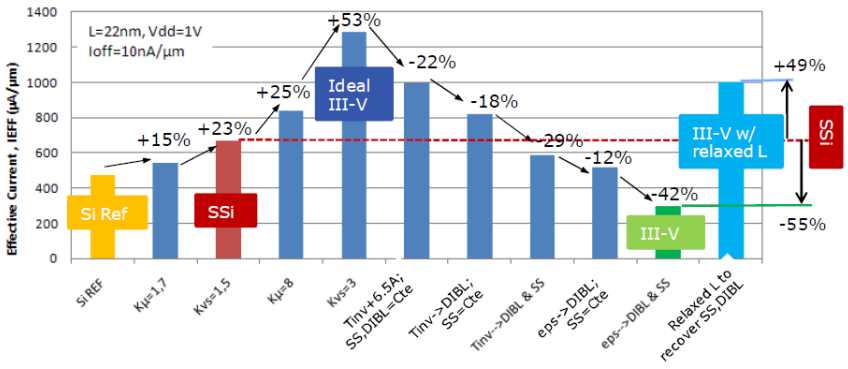

Figure 3.4: Evolution of the Effective Current, I_{eff} under impact of the following effects (all in a cumulative manner): increase in mobility 1.7X, increase in saturation velocity 1.5X (this point corresponds to strained Silicon), further increase in mobility up to 8X, further increase in saturation velocity up to 3X (this point corresponds to an ideal III-V channel), degradation in inversion density due to larger Dark Space(DS) , degradation in DIBL due to DS, degradation in SS due to DS, degradation in DIBL due to larger ε, degradation in SS due to ε (this points corresponds to a realistic III-V channel). [49]

3.2 Quantum Effects and SCEs in Subthreshold Regime

3.2.1 Concept of Dark Space

When quantum confinement in the channel is taken into account, lesser inversion charge is obtained at the same gate overdrive and this effect can be modeled as an artificial increase of the Equivalent Oxide Thickness (EOT) of the gate dielectric. This incremental EOT is called the "dark space" thickness, DS [58].

It is well known that as a result of quantization of the inversion layer in a MOSFET, electron density is found to vanish at the channel/gate oxide interface while reaching the maximum value at some distance into the semiconductor, away from the interface [69], in contrast to the classical case where the maximum electron density is expected at the interface. Figure 3.5 shows this phenomenon. There is lesser coupling of the gate voltage with the inversion charge. It is especially important in modern nanometric MOS devices where the oxide thickness is very small and is comparable to the extent of

inversion layer penetration into the channel [70].

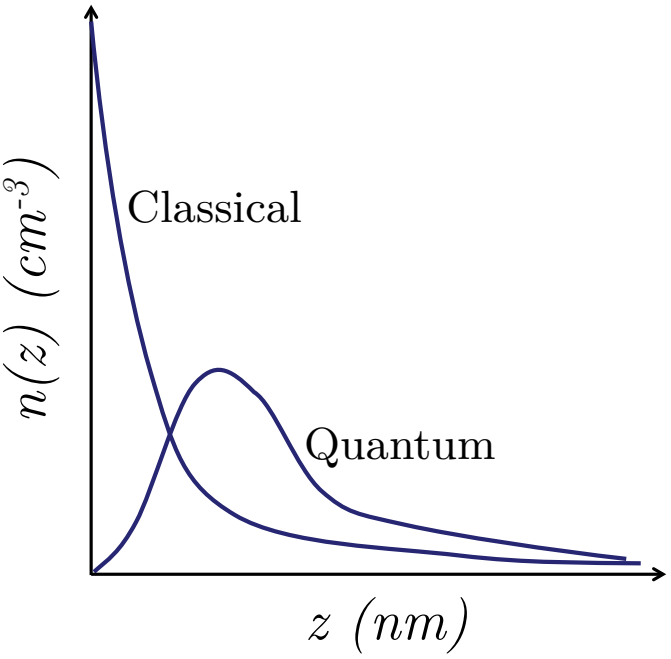

Figure 3.5: Electronic charge density obtained using classical and quantum calculations for an inversion layer

The dark space is proportional to the distance of the inversion charge centroid from the channel/gateoxide interface. The inversion charge centroid, z_{inv} can be expressed as [70] [58]:

$$z_{inv} = \frac{\int_0^\infty z\rho_{inv}(z)\,dz}{\int_0^\infty \rho_{inv}(z)\,dz} \tag{3.1}$$

On changing the effective mass of the channel material, the charge centroid shifts and hence the dark space is altered. The impact of this phenomenon on different channel materials is discussed in the next subsections.

3.2.2 Simulation Methodology

To investigate the potential effect of quantum confinement on short channel effects, several previous works have compared the results obtained using classical simulator with results obtained with an analytical model and quantum corrected TCAD simulator [62, 63]. However, as mentioned in the preceding section, this simple approach is not reliable.

Therefore, to avoid the above mentioned issue of inconsistencies across different simulators, the results presented in this section have been obtained using the same tool, i.e. the NanoMOS [71, 72] simulator suite, which self consistently solves the Poisson-Schrödinger (PS) equations, along the channel, with different transport models. Indeed, although NanoMOS being better known for its Non Equilibrium Green Function (NEGF) transport model, it also includes a Ballistic Transport Model (BTM) model and a Drift Diffusion (DD) model, which are all self consistently solved with the PS equations [71]. The NEGF model in NanoMOS is a ballistic transport model (called the Quantum Ballistic Transport Model, QBTM) which accounts for all source-drain tunneling components, and in particular the subthreshold source-to-drain tunneling, which has been shown to be significant for ultra short channel (< 15 nm) III-V nMOSFETs [50, 73]. There is another transport model (called the Classical Ballistic Transport Model, CLBTM) which, although takes into account the quantum confinement in the vertical direction, neglects the source-drain tunneling component of the drain current. The DD model available in NanoMOS differs from conventional drift diffusion model as the charge is rigorously calculated using a Poisson-Schrödinger solver. As an example, the simulation scheme for the full quantum ballistic transport calculation in NanoMOS is shown in Figure 3.6. The schematic of the device structure simulated in NanoMOS is shown in Figure 3.7.

To study the impact of quantum effect on subthreshold SCEs, NanoMOS simulations have been performed while changing the effective masses, in order to artificially modify the strength of quantization by:

- increasing the subband splitting through the decrease of the confinement effective mass,

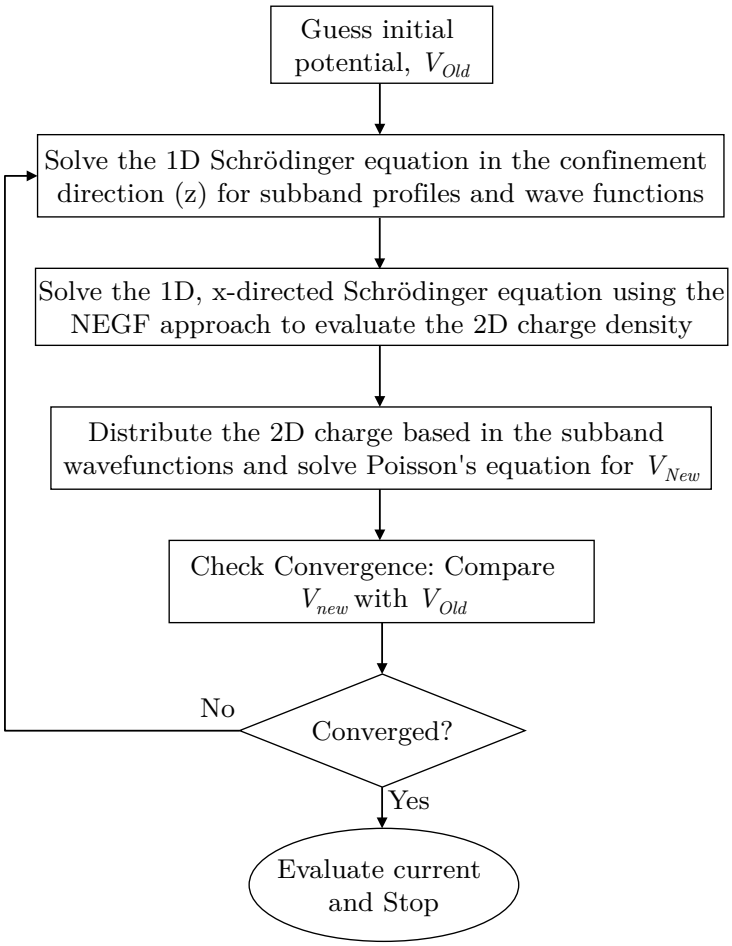

Figure 3.6: Full quantum ballistic simulation scheme in NanoMOS (Taken from [72])

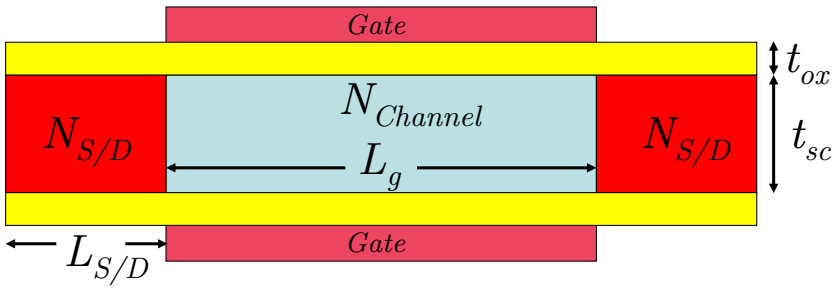

Figure 3.7: Device structure used in the NanoMOS simulations

Parameter	Value
t_{sc}	5 nm
t_{ox}	1 nm
$L_{S/D}$	10 nm
$N_{S/D}$	5x10^{19} cm^{-3}
$N_{Channel}$	10^{10} cm^{-3}
ε_{ox}	3.9

Table 3.1: Template MOSFET device parameters used in the NanoMOS simulations

- reducing the DOS in the conduction band through the decrease of the density of state effective mass [74], and
- dark space variation

These effects will therefore highlight any dependency of SCEs with quantum confinement and especially of the dark space [58, 59, 61].

3.2.3 Simulation Results

The devices considered in this section are template double gate MOSFETs with a 5 nm film thickness, 1 nm EOT and 10 nm source/drain length. The device parameters are listed in Table 3.1. To avoid any confusion with the increase of subthreshold slope due to the SCEs, source-to-drain tunneling has been ignored by using the Drift-Diffusion model for carrier transport. Three gate lengths (L_g) have been considered: 10, 15 and 20 nm and, as explained, the density of state effective mass of the channel material has been varied from $0.05m_0$ to $1m_0$. The carrier mobilites have been kept fixed as in the template MOSFET with Si channel during the simulations as it is not a factor in studying the relative subthreshold performance of the device and we are not concerned with exact values of drain currents in the simulated devices. For the same reasons, channel/gate oxide interface states are also neglected. The obtained DIBL and subthreshold slope are shown in Figure 3.8.

Contrary to [62, 63], who argued that quantization does affect the SCEs in subthreshold regime, the results obtained here with NanoMOS do not show

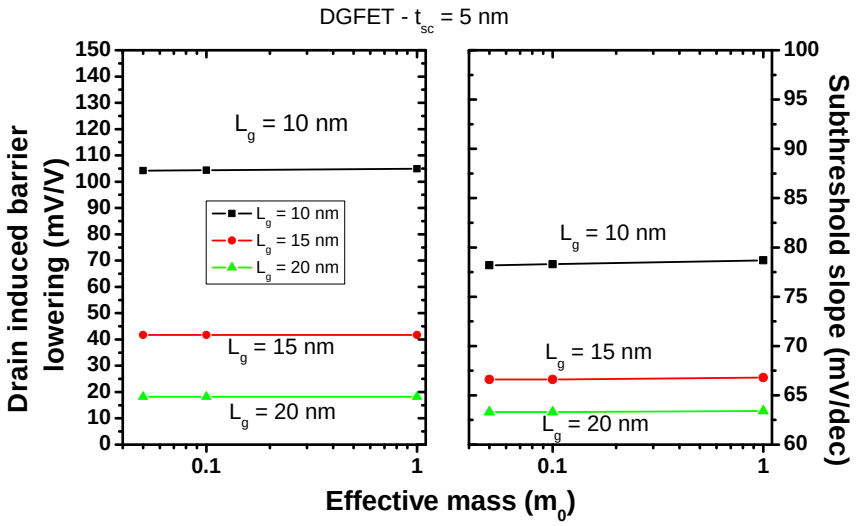

Figure 3.8: Drain induced barrier lowering and subthreshold slope as a function of the density of state effective mass, obtained with NanoMOS using the drift-diffusion model, for three different gate lengths (L_g = 10, 15 and 20 nm) of double gate MOSFET featuring a channel thickness of 5 nm and an EOT of 1 nm.

any modification of the DIBL or the subthreshold slope when the density of states effective mass is changed. These results have also been obtained when considering different values of the confinement effective mass, which mainly influence the value of the long channel threshold voltage, but do not modify the subthreshold slope or the DIBL. Therefore, neither the subband splitting induced by the reduction of the confinement effective mass, nor the increase of dark space induced by reduced DOS effective mass modifies the SCEs. In the weak inversion regime, the channel potential is hence still mostly controlled by geometry, the built-in potentials and the depletion charges.

3.3 Impact of Material Parameters

Classical simulation can therefore correctly capture the SCEs. To illustrate further the impact of the channel material parameters on the short channel effects, the double gate devices have been simulated with varying energy bandgaps and varying dielectric constants, by self-consistently computing

the Poisson and Drift-Diffusion equations using FlexPDE. These double gate devices feature a film thickness (t_{sc}) of 5 nm and an EOT of 1 nm. The same three gate lengths (10, 15 and 20 nm) have been simulated.

The DIBL and subthreshold slope have been firstly extracted for varying values of bandgap, as the channel potential profile depends on the built-in potential between the source/drain and channel *pn* junctions, and hence on E_g [75, 76]. These results are shown in Figure 3.9 and compared with the results obtained from the analytical model presented in [51]. It can be seen from Figure 3.9 that the subthreshold slope of the double gate device is independent of the bandgap value of the semiconductor. Results obtained by simulation and the model have been found to be in agreement, without fitting procedures. DIBL however seems to be a weak function of the bandgap, mostly in devices featuring large SCEs (e.g. $L_g = 10$ nm and $t_{sc} = 5$ nm). The discrepancy between the model and the simulations becomes larger for values of L_g/t_{sc} smaller than 2, which correspond to the limit of validity of the model [51].

Similar simulations have been performed for varying dielectric constants of the channel material. The DIBL and subthreshold slope obtained from these simulations are plotted in Figure 3.10, which shows, as expected that DIBL and subthreshold slope are much stronger functions of the dielectric constant [51] than of the bandgap. Both DIBL and subthreshold slope significantly increase when the dielectric constant ε_{sc} goes from $12\varepsilon_0(\sim \varepsilon_{Si})$ to $17\varepsilon_0(\sim \varepsilon_{InSb})$. These results are also in agreement with the model proposed in [51] and the simulation results. It confirms that the main cause of short channel effect increase in III-V technologies is related to their larger dielectric constants.

3.4 DIBL in Strong Inversion Regime

3.4.1 Effective current and DIBL

Conventionally, in the expression for gate delay CV/I, the current is taken to be the on-current, $I_{on} = I_D(V_g = V_d = V_{DD})$. However, the current never reaches I_{on} during the switching process, and it has been argued that

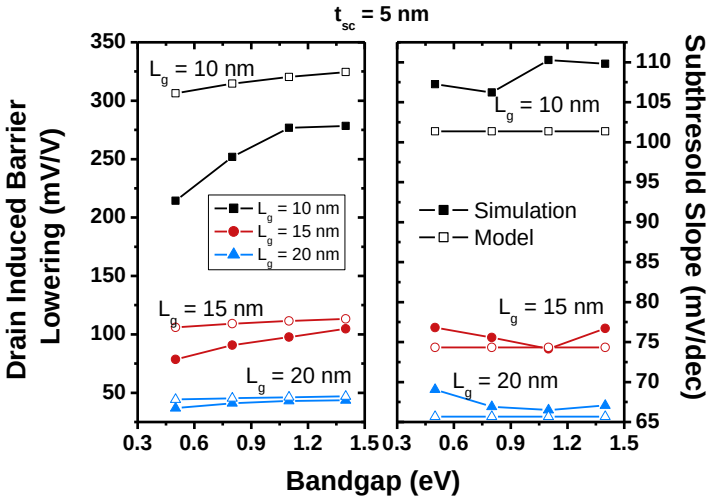

Figure 3.9: Drain induced barrier lowering (a) and subthreshold slope (b) as a function of the bandgap of the channel material, for three different gate length (L_g = 10, 15 and 20 nm) of double gate MOSFET featuring a channel thickness of 5 nm and an EOT of 1 nm. Closed symbols correspond to classical simulation results and open symbols correspond to results obtained with the model presented in [51]

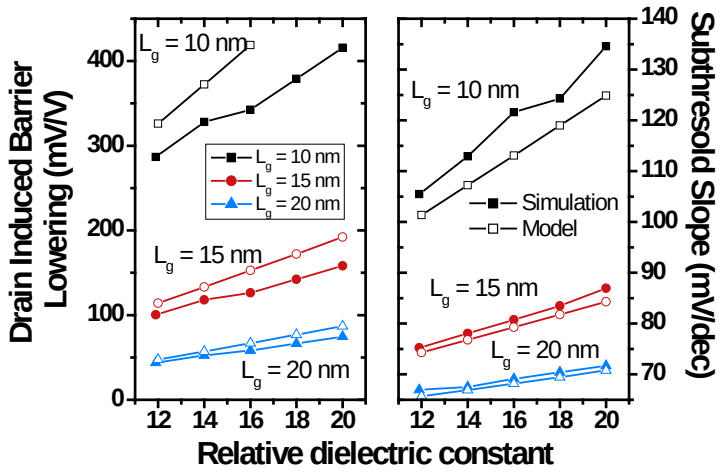

Figure 3.10: Drain induced barrier lowering (a) and subthreshold slope (b) as a function of the dielectric constant of the channel material, for three different gate length (L_g = 10, 15 and 20 nm) of double gate MOSFET featuring a channel thickness of 5 nm and an EOT of 1 nm. Closed symbols correspond to classical simulation results and open symbols correspond to results obtained with the model presented in [51].

it is necessary to take into account the linear characteristics of the device in addition to the saturation current for circuit speed calculations [77]. It has been shown [78] that using an "effective on current", I_{eff} instead of I_{on} leads to more accurate estimation of CMOS inverter delays. I_{eff} is given by:

$$I_{eff} = (I_L + I_H)/2 \text{ where} \tag{3.2}$$

$$I_L = I_d(V_g = V_{DD}/2, V_d = V_{DD}) \text{ and} \tag{3.3}$$

$$I_H = I_d(V_g = V_{DD}, V_d = V_{DD}/2) \tag{3.4}$$

Even at the same I_{on} and I_{off}, a technology with higher DIBL will result

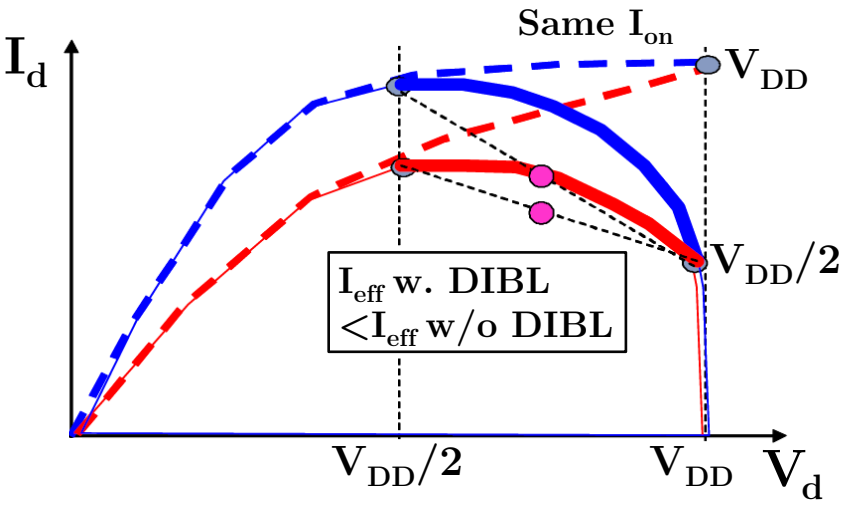

Figure 3.11: Impact of the DIBL on effective current: Technology with higher DIBL (red dotted line) will have lesser I_{eff} than that with lower DIBL (blue dotted line)
(Taken from [49])

in lesser I_{eff} [49]. Figure 3.11 explains this graphically using the switching trajectories for two devices having different DIBLs. DIBL and the switching frequency ($f = I_{eff}/CV$) can be roughly related as [49]:

$$\frac{\Delta f}{f} = \frac{\Delta I_{eff}}{I_{eff}} = -\frac{2\Delta DIBL}{V_{DD} - V_t} \tag{3.5}$$

It implies that a higher DIBL translates to lower I_{eff} and hence lower switching frequency.

3.4.2 Dark space and DIBL in strong inversion

The previous section has confirmed that the confined minority carriers could be neglected when solving the Poisson equation in subthreshold regime. However, in the inversion regime, the inversion charge has to be taken into account in the Poisson's equation, and hence quantum effects should be included. Besides, the DIBL is also known to be a function of the oxide thickness. In subthreshold condition and using the Voltage-Doping Transformation model [75, 76], the DIBL can be simply reduced to:

$$DIBL = t_{ox} \frac{\sqrt{4qN_a\varepsilon_{sc}\phi_f}}{\varepsilon_{ox}} \frac{\varepsilon_{sc}}{qN_aL_g^2} \tag{3.6}$$

where N_a is the channel doping concentration, $2\phi_f$ the surface potential at threshold, q the elementary charge, ε_{sc} and ε_{ox} the silicon and oxide dielectric constant, L_g the gate length, and t_{ox} the EOT. The DIBL may hence be impacted by the dark space, which increases the effective t_{ox} in strong inversion.

Next, subsection 3.4.3 will first present a definition and an extraction method for the DIBL in the strong inversion regime. Then, subsection subsection 3.4.4 will use this definition and extraction method to study the impact of quantization on the DIBL in strong inversion.

3.4.3 Definition and extraction method of the DIBL in strong inversion regime

Figure 3.12 shows how DIBL affects the $I_d - V_d$ curves in the saturation regime differently for a long and a short channel MOSFET. The conventional definition of DIBL is based on the threshold voltage shift induced by a drain voltage, as:

$$V_t^{DIBL}(V_d) = V_t - \lambda V_d \tag{3.7}$$

where V_d is the drain voltage, V_t the threshold voltage at low V_d, V_t^{DIBL} the shifted threshold voltage and λ, the DIBL. In the subthreshold regime, λ is extracted by calculating the gate voltage shift at a constant drain current

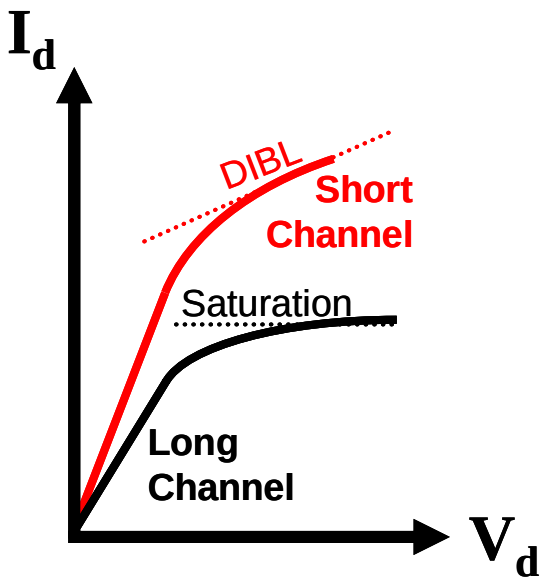

Figure 3.12: Schematic plot of the $I_d - V_d$ characteristic for a long and a short channel MOSFET, showing the impact of DIBL on the saturation regime.

of I_d-V_g curves obtained for two drain voltages. This extraction procedure is no longer relevant in strong inversion regime. One way to generalize the extraction of DIBL to all regimes is to use the approach presented in [79, 80], which extends the conventional definition of the DIBL given by equation (3.7). This extraction method is based on the parasitic increase of the drain current related to the drain voltage variation.

As shown in Figure 3.13, the increase of current δI_d resulting from the increase of drain voltage δV_d is equal to the product of the transconductance $\delta I_d/\delta V_g$ and the shift in gate voltage $\lambda \delta V_d$. Hence, λ can be defined as:

$$\lambda = \frac{\delta I_d}{\delta V_d} \Bigg/ \frac{\delta I_d}{\delta V_g} = \frac{g_d}{g_m} \tag{3.8}$$

where g_d is the conductance and g_m, the transconductance. Equation (3.8) hence enables an extraction of the DIBL, not only in subthreshold regime, but in all regimes, either from measurements or simulations results. Moreover, it is easy to show that the calculated value in subthreshold regime coincides with the value of the conventional DIBL.

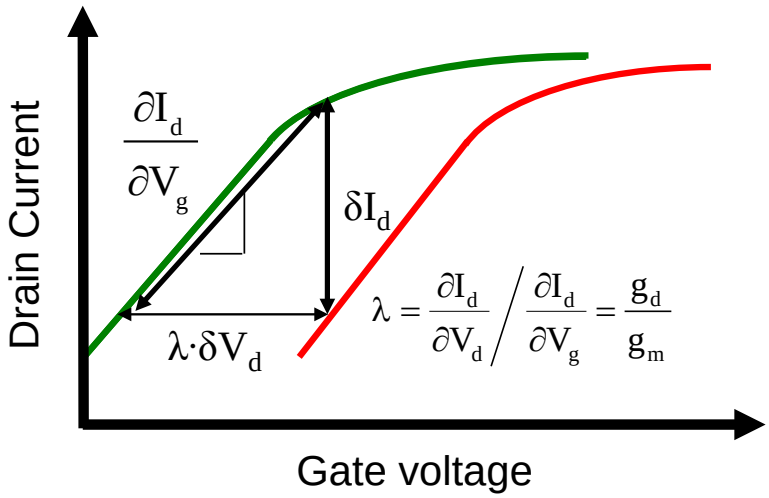

Figure 3.13: Scheme of the impact of DIBL on the subthreshold $I_d - V_g$ characteristics of an nMOSFET, illustrating the relation between the transconductance, the drain current current increased due to DIBL, and the corresponding gate voltage shift.

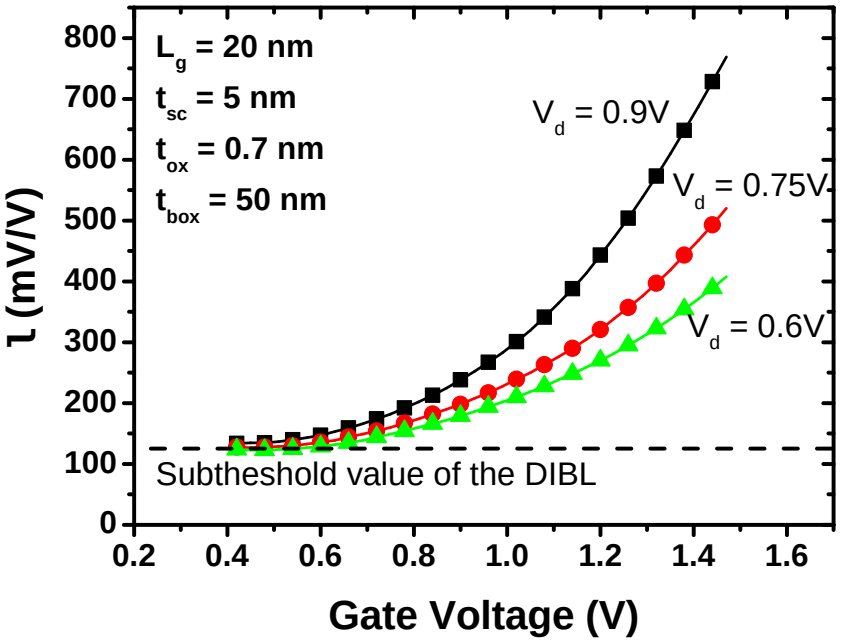

Figure 3.14: Generalized DIBL parameter λ as a function of the gate voltage, for three drain voltages (above the saturation voltage), obtained by classical drift diffusion simulation of asymmetrical double gate MOSFET featuring a gate length of 20 nm, a film thickness of 5 nm and an EOT of 0.7 nm.

Figure 3.14 shows such extraction of g_d/g_m as a function of the gate voltage, for different drain current (higher than the saturation current) obtained from simulation of a double gate MOSFET using the Drift Diffusion transport model, featuring an EOT of 0.7 nm, a 5 nm thick silicon channel and a gate length of 20 nm. It can be seen that the extracted DIBL from g_d/g_m is indeed constant in the subthreshold regime but that its value increases in the strong inversion regime. In addition, a increase of g_d/g_m for increasing value of V_d (higher than the saturation drain voltage) is also obtained from the drift diffusion simulation.

3.4.4 Impact of quantum effects and dark space on the DIBL in inversion

Equation (3.6) shows, with a simple model, that the subthreshold DIBL is a linear function of the oxide thickness. However, in strong inversion regime and in presence of quantum confinement, the equivalent oxide thickness is increased with respect to the physical oxide thickness t_{ox}, by a value called the dark space [58,59,61], which is induced by the displacement of the charge centroid away from the insulator/semiconductor interface [58] and by the reduction of the density of state due to the presence of subband level [60]. This dark space is generally in the order of 3 Å in Si, but larger in the case of III-V semiconductors, as obtained by quantum simulation in [58, 59]. Therefore, quantum effects may have an impact on DIBL in the strong inversion regime.

To clarify that point, two sets of simulation have been performed. The first set of simulations have been carried out using quantum corrected Drift Diffusion simulations in FlexPDE, while the second set have been carried out with the NanoMOS suite with the Drift Diffusion model. In the quantum corrected numerical simulations, the Hansch model [81] has been implemented as a first order quantum correction, in order to mimic the displacement of the charge centroid. Although not being able to fully capture the carrier quantum degeneracy as well as Poisson-Schrödinger calculation, the Hansch model manages to introduce an apparent additional oxide thickness in strong inversion as in the quantum case. In addition, the dark space obtained with the

Hansch model can be easily tuned, by simply changing the value of Hansch's length [81] in:

$$n_H(x) = n_0(x)\left[1 - exp\left(-\frac{x}{L_H}\right)\right]\left[1 - exp\left(-\frac{t_{Si} - x}{L_H}\right)\right] \tag{3.9}$$

where $n_H(x)$ is the corrected charge profile, $n_0(x)$ the classical profile, t_{Si} the semiconductor film thickness and L_H, the Hansch's length. On the contrary, the NanoMOS simulator rigorously accounts for quantum degeneracy, but the value of dark space can only be indirectly tuned through the variation of the density of state effective mass.

Therefore, at first, quantum corrected drift diffusion simulation of an FD-SOI MOSFET has been performed with different L_H to extract λ using equation (3.8). Figure 3.15 shows the corresponding extracted DIBL, λ as a function of the gate voltage, for three different Hansch's length (L_H = 1, 2 and 4 nm). It can be seen that in subthreshold regime, λ is unchanged, as the total charge is fixed by the geometry, the depletion charge. In strong inversion regime, on the contrary, L_H increases the value of λ, thus indicating that the DIBL is a function of the dark space, which depends, in this model, on Hansch's length.

To investigate further this effect with a more accurate treatment of quantum confinement and transport, the NanoMOS simulation suit has then been used to compute λ in double gate MOSFETs, featuring 10 nm gate length, 5 nm film thickness and 0.7 nm EOT. In this case also, the density of state effective mass has been varied to change the strength of the quantum confinement. The drift diffusion transport model coupled with Poisson-Schrödinger solution of the charge has been used with a constant mobility, in order to avoid the impact of the effective mass on carrier transport, normally included in the two other transport model [71]. Two effective masses have then been used ($0.1m_0$ and $1m_0$) to artificially emulate two different dark spaces in these devices. These different dark spaces consequently lead to the $I_d - V_g$ characteristics shown in Figure 3.16, which present a more degraded coupling in the case of the $0.1m_0$ simulation than in the case of the $1m_0$ one.

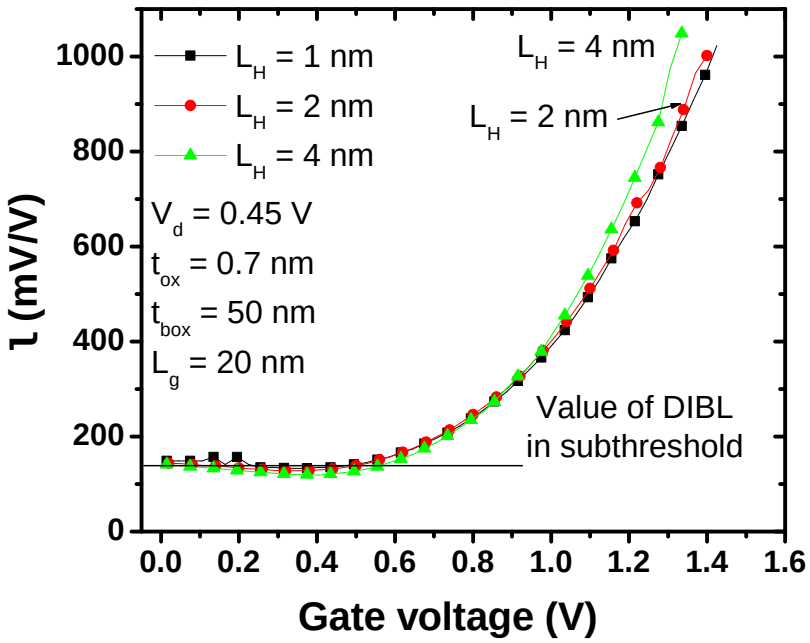

Figure 3.15: Generalized DIBL parameter λ as a function of the gate voltage, for three Hansch's lengths, obtained by quantum corrected drift diffusion simulation of FDSOI MOSFET, featuring a gate length of 20 nm, a film thickness of 10 nm and an EOT of 0.7 nm and a buried oxide thickness of 50 nm.

As no absolute extraction of the dark space is possible with the NanoMOS suite, the impact of varying dark space is evidenced by plotting the ratio of the drain current for $m_d = 0.1m_0$ to the drain current for $m_d = 1.0m_0$ ($I_{d0.1m_0}/I_{d1m_0}$). This ratio, plotted in Figure 3.17, hence corresponds to the dark space increase of $m_d = 0.1m_0$ with respect to the dark space for $m_d = 1m_0$.

The λ obtained with $m_d = 0.1m_0$ and $m_d = 1m_0$ have been calculated using the resulting $I_d(V_g, V_d)$ characteristics and equation (3.7). The same trend as in Figure 3.15 has been obtained, i.e. λ has been found to be larger for $m_d = 0.1m_0$ than for $m_d = 1m_0$, confirming that the larger dark space induced larger λ in the inversion regime.

As λ is expected to be proportional to t_{ox}, while the drain current I_d in the linear regime is inversely proportional to t_{ox}, the ratio $\lambda_{1.0m_0}/\lambda_{0.1m_0}$ as been

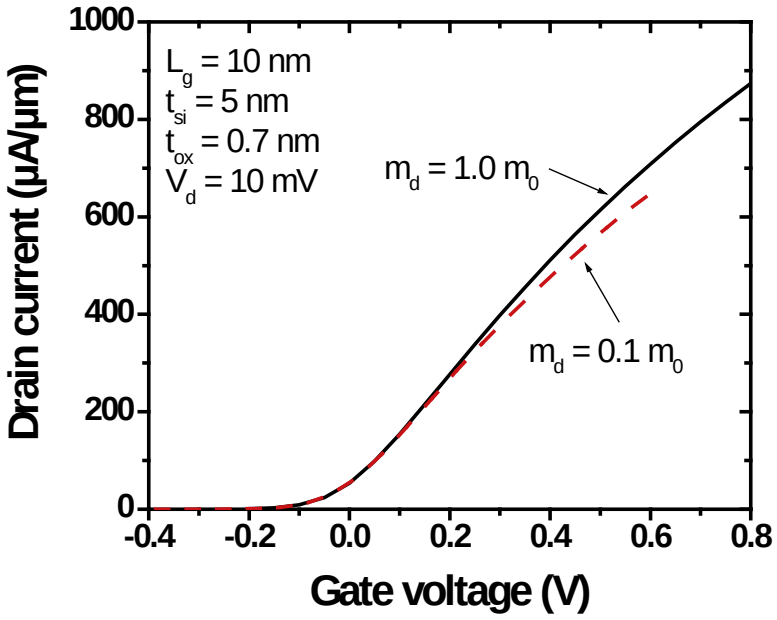

Figure 3.16: $I_d - V_g$ characteristics at $V_d = 10$ mV, obtained with NanoMOS using the Drift Diffusion transport model, for two density of state effective masses inducing two different dark spaces.

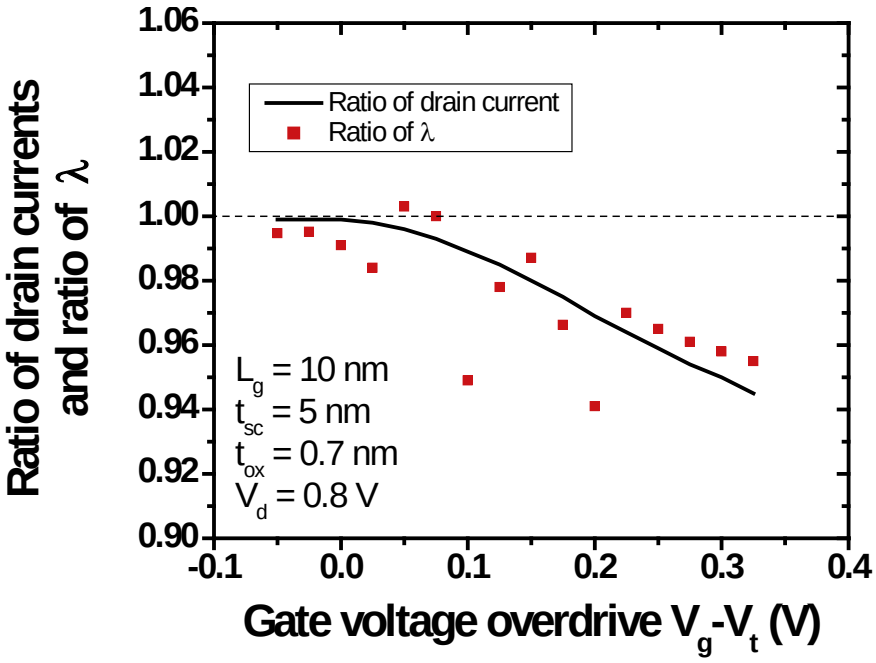

Figure 3.17: Ratio of the drain current and ratio of DIBL as a function of the gate voltage overdrive. The noise in the simulation is due to the multiple ratios and derivatives required to obtain $\lambda_{1.0m_0}/\lambda_{0.1m_0}$

plotted in Figure 3.17 and compared to the ratio $I_{d0.1m_0}/I_{d1.0m_0}$. It can be seen that $\lambda_{1.0m_0}/\lambda_{0.1m_0}$ follows the trend of $I_{d0.1m_0}/I_{d1.0m_0}$, thus confirming that λ is increased in presence of quantization in the same extent than the drain current degradation due to quantum confinement and increased dark space. This result therefore shows that a part of the DIBL in the strong inversion regime, defined by λ, is due to the presence dark space and quantum confinement and that the larger dark spaces obtained in the case of III-V MOSFETs [58, 60] may cause further enhancement of the DIBL in the strong inversion regime compared to silicon devices.

3.5 Impact of the architecture on the SCEs

The different architectures of III-V MOSFETs have been discussed in Chapter 1. The impact of different architectures on SCEs needs to be evaluated to determine their worthiness.

3.5.1 Impact of barrier layers: QWFET Vs thin films

As discussed in the introduction section, III-V heterostructure devices, also called Quantum Well FETs have attracted a lot of attention(for example [82]). All the proposed QWFET architectures include III-V barrier layers (generally InP) on top of the channel (often $In_xGa_{1-x}As$). The wide band gap barrier layers are required for carrier confinement in the lower band gap quantum well, to limit mobility degradation due to interface defects [83,84] and also for reducing junction leakage and off-state leakage currents. In this section the impact of the barrier layer above the channel is explored.

A simplified structure of such category of mulitlayered MOSFET structures is illustrated in Figure 3.18. This section examines the impact of this barrier layer on the SCEs of III-V QWFETs.

Self-consistent solution of the Poisson and Drift-Diffusion equation have hence been carried out using FlexPDE for an asymmetrical double gate device (grounded back gate), featuring a 5 nm thick $In_{0.7}Ga_{0.3}As$ channel and an InP barrier layer. At first, it has been checked that if the barrier layer is

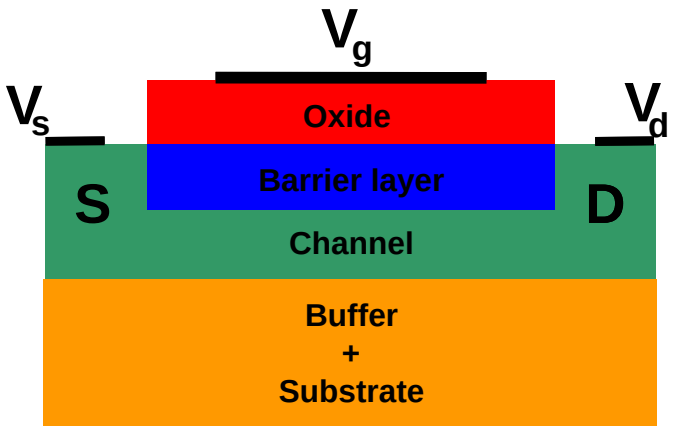

Figure 3.18: Simplified scheme of a heterostructure Quantum Well FET.

thin enough with respect to the channel thickness, no charge was transferred from the channel to the barrier under reasonable bias conditions. Hence, the barrier layer could be simply considered as an additional dielectric layer.

To illustrate the impact of this layer, the DIBL has been reported as a function of the dielectric constant of the barrier material in Figure 3.19(a), for two gate lengths (15 and 20 nm) and for two barrier thicknesses (5 and 2 nm). It can be seen that, as expected, the DIBL is increased in the presence of a barrier layer and that thinner barrier layer would lead to weaker DIBL. For larger dielectric constant and thinner barrier layer, the DIBL is reduced and the equivalent oxide thickness of the barrier stack is essentially independent of the barrier layer thickness.

However, the previous results have been obtained by applying Neumann boundary conditions to the barrier layer, as in the case of conventional dielectric layer. In fact, the potential on the left and right side of the barrier layer is set by the source and drain voltage, and the S/D boundary condition should rather be of Dirichlet type. The difference between these two types of boundary condition is reported in Figure 3.19(b), which also plots the DIBL as a function of barrier dielectric constant (T_{bar}= 2 nm).

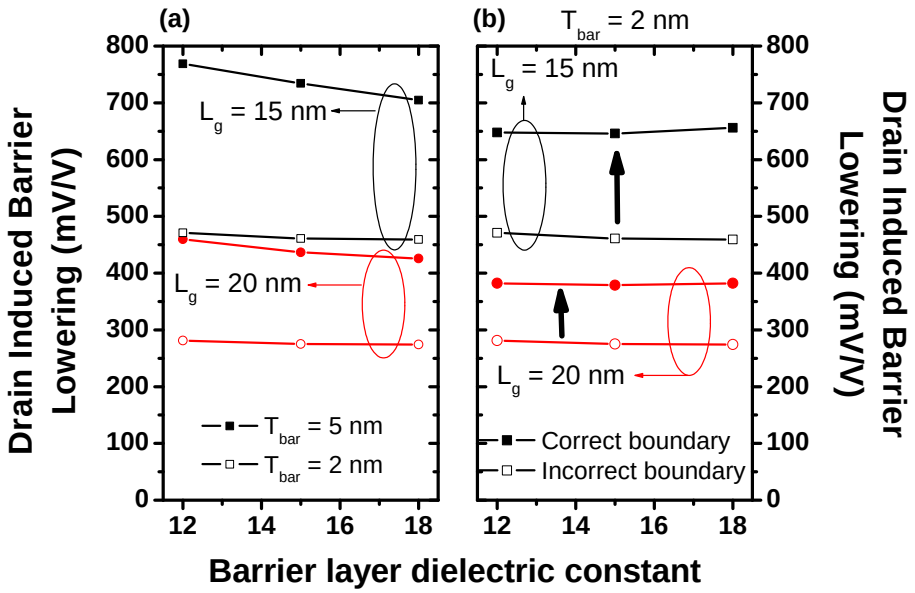

Figure 3.19: DIBL as a function of the barrier layer dielectric constant. (a) For different barrier thicknesses, using Neumann boundary condition. (b) for Dirichlet - correct (solid) boundary conditions and for Neumann - incorrect (open)

It can be seen that the DIBL is increased by when Dirichlet boundary condition are used, which means that SCEs are degraded when the barrier layer is in contact with the source and drain. In addition, an increase of barrier dielectric constant slightly increases DIBL, which shows that the drain voltage and the channel potential are in fact coupled by the barrier layer, hence acting as a fringing capacitor. Therefore, the barrier layer of the QWFET architecture not only increases DIBL by increasing the EOT, but also due to fringing capacitance.

Chapter 4

Source to Drain Tunneling and III-V MOSFETs

Contents

4.1 Leakages in Nanoscale MOSFETs

Maintaing a high I_{on}/I_{off} ratio is essential while miniaturising transistors. Different leakage mechanisms contribute to the off current in a MOSFET which can be categorized as follows

- **Source to Drain Leakage:** It consists of the off state currents along the lateral direction along the channel:
  - **Thermionic Current:** Electrons in the source side with thermal energy greater than the potential barrier can escape into drain region.
  - **Subthreshold Leakage:** It is the diffusion current in the channel due to minority carriers when the applied gate voltage is less than

the threshold voltage, $V_g < V_t$, increasing exponentially with V_g. It is enhanced by the drain induced barrier lowering effect (DIBL) as the drain voltage is increased.

- **BTBT (Band to Band Tunneling):** It is caused due to the electrons tunneling from the valence band to the conduction band (or vice versa).
- **SDT (Source to Drain Tunneling):** It is the direct tunneling of the conduction band electrons in the source to the drain through the channel potential barrier. This has been discussed in detail in the next section.
- **GIDL (Gate Induced Drain Leakage):** It occurs when the gate is biased at zero or negative voltage and drain bias, V_D is high creating a high-field $p^+ - n^+$ junction at the gate/drain overlap region and electrons can tunnel across it through mechanisms of band to band tunneling and trap assisted tunneling, leading to increased drain current and its impact can be seens as observed the upward bending of $I_d - V_g$ curves below threshold [85] [86].

Figure 4.1 shows the dominant leakage currents in the source-drain direction in a MOSFET that contribute to the net off state current.

- **Gate leakage:** It consists of leakage currents in the gate-to-channel direction.
  - **Fowler-Nordheim Tunneling:** Tunneling of electrons from the channel into the gate oxide layer through a triangular barrier
  - **Direct Tunneling:** It takes place in very thin oxide layers (when t_{ox} is less than 3-4 nm) and the electrons tunnel directly into the gate region through the forbidden energy gap of the oxide layer.
  - **Hot carrier Injection:** If the electric field at channel/gate oxide layer interface is too high, electrons can gain enough energy to cross above the potential barrier from substrate to gate insulator [87].

Figure 4.2 shows the first two types of gate tunneling mechanisms.

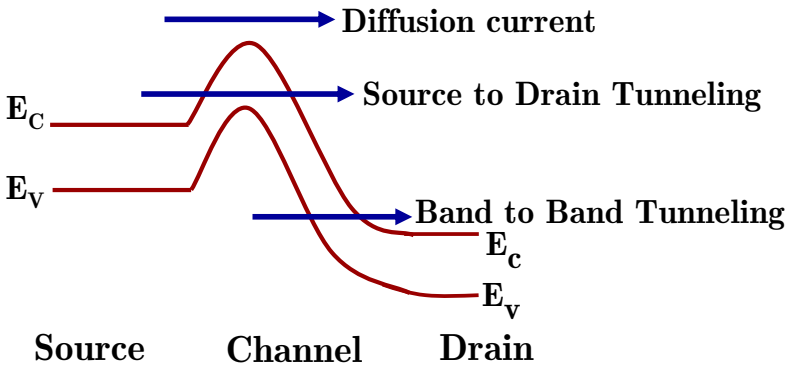

Figure 4.1: Main leakage current mechanisms in the longitudinal direction of the device: subthreshold diffusion current, SD tunneling and BTBT)

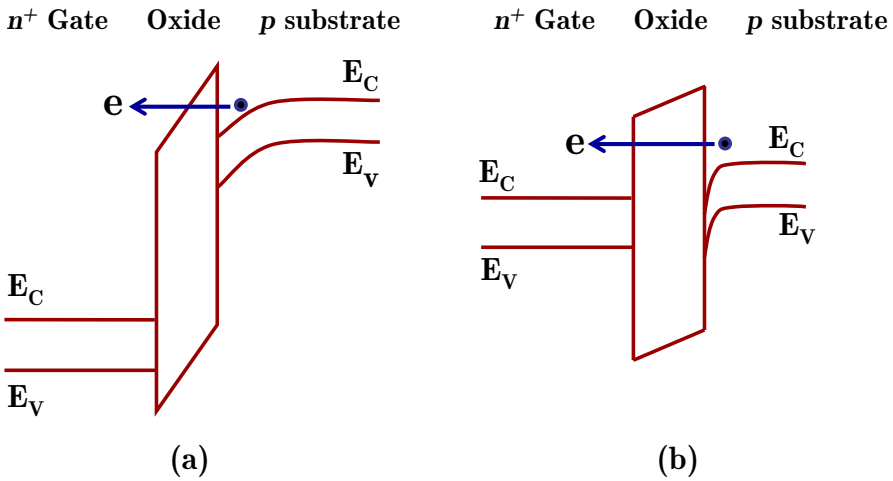

Figure 4.2: Gate Tunneling mechanisms in a MOSFET: (a) FN tunneling (b) Direct tunneling

In the previous chapters, where the goal was to focus mainly on the electrostatics and quantum confinement effects in the perpendicular direction to the channel, source-to-drain leakage currents were ignored. But since in short channel devices source drain leakage plays an important role by tunneling mechanisms, it is important to evaluate its impact on the short channel effects and explore if source-to-drain tunneling can set the scaling limit for Si and ACM devices. In this chapter the impact of the source-to-drain tunneling is studied, without taking into account any gate leakages.

4.2 Source to Drain Tunneling

As the MOSFET gate lengths get smaller with each new technology generation, due to increased proximity of the source and drain regions, quantum mechanical tunneling of carriers from source to the drain starts to play a significant role in the off state leakage and is a possible determinant of the ultimate transistor scaling limits [88] [89]. This source drain tunneling through the channel barrier can be a lot more detrimental in MOSFETs with alternative channel materials like III-V compounds as they have smaller effective masses, leading to higher off currents and poor switching characteristics.

4.2.1 The WKB approximation

The Wentzel-Kramers-Brillouin (WKB) approximation is a way to find an approximate solution to the time independent Schrödinger equation [90]. The tunneling through a barrier can be described using the tunneling probability or transparency obtained using the WKB method as given by:

$$T(E_x) = exp\left(\frac{-2}{\hbar}\int_{x_1}^{x_2}\sqrt{2m^*(E_{barrier}(x) - E_x)}\,dx\right) \tag{4.1}$$

where m^* is the effective mass of the electron, $E_{barrier}(x)$ is the channel potential energy barrier between source and drain, E_x is the electron energy with $E_{barrier}(x) > E_x$ in the tunnel region as shown in Figure 4.3. x_1 and x_2 are the classical turning points ($E_{barrier}(x) = E_x$ at $x = x_1, x_2$).

From first order perspectives, it can be readily predicted from (4.1) that a lighter effective mass corresponds to a higher value of the transparency and hence increased source-drain tunneling.

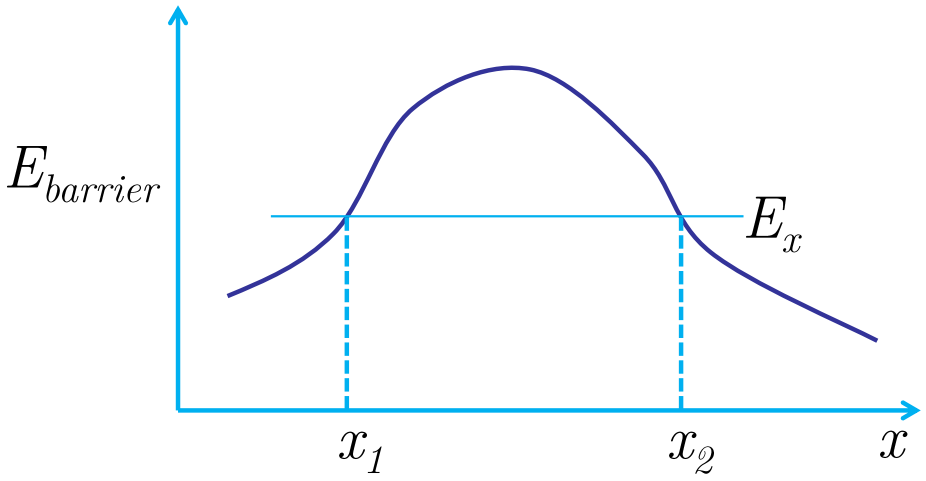

Figure 4.3: WKB Approximation

4.2.2 Effective barrier size modulation

As the gate length is reduced, the effective barrier width reduces and hence the source drain tunneling current increases. As shown in Figure 4.4 the effective barrier width is found to reduce with increased channel thicknesses. So thicker devices have increased tunneling. So this puts further constraint on the t_{sc} requirement to be made thinner, than simply worsened electrostatics.

Also, this narrowing of the channel barrier is also dependant on the applied drain bias. Higher drain voltage causes more thinning of the barrier along with its lowering (DIBL) as the conduction band is pulled down with increased drain voltage is pulled down as depicted in Figure 4.5 for an InSb device with 10 nm long gate and 2 nm thick channel. As a result the SD tunneling is expected to increase because of this two fold effect of DIBL.

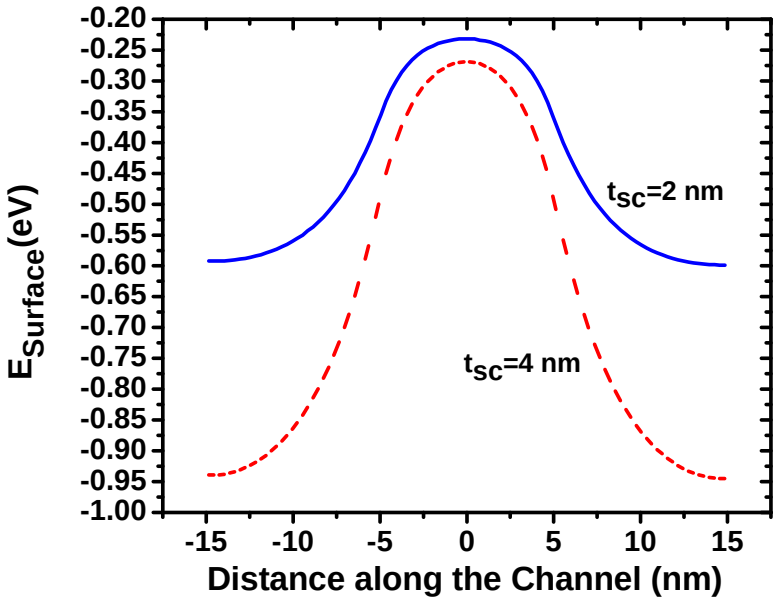

Figure 4.4: Reduction of the barrier width with increase in channel thickness. InSb channel device. L_g=10 nm, t_{sc}=2 nm, 4 nm), V_d=0.01 V

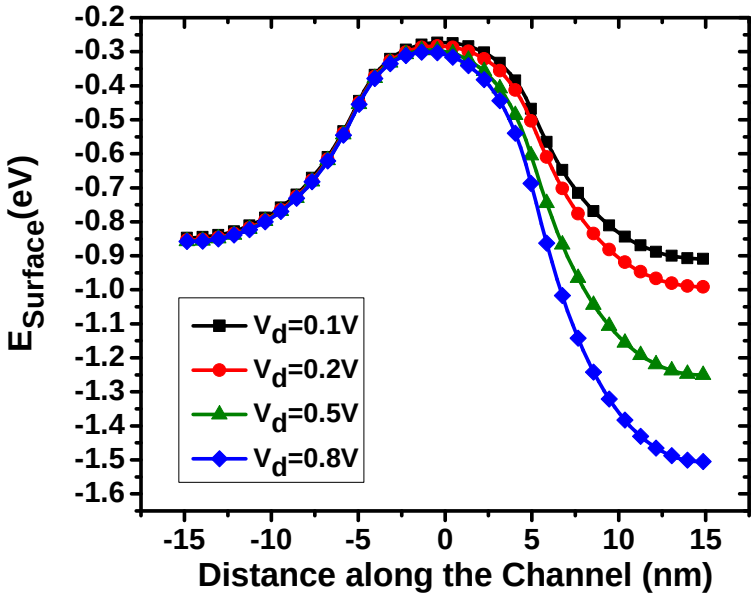

Figure 4.5: Effect of the drain voltage on the potential barrier. InSb channel device. (L_g=10 nm, t_{sc}=2 nm, 4 nm, V_d=0.1 V, 0.2 V, 0.5 V, 0.8 V)

4.3 Source Drain Tunneling and ACM

Simulations have been performed for different channel materials by varying their effective masses and dielectric constants, once including and then excluding source-to-drain quantum tunneling by using different transport models in NanoMOS, while keeping other parameters the same. In the following simulations, the devices considered are double gate MOSFETs as in the previous chapters. In [89] it was shown that S/D tunneling is negligible in devices with channel lengths greater than 10 nm for a Si device. In this study it is intended to find if the same holds true for alternative channel material MOSFETs. Ballistic transport has been assumed in the devices using the NEGF approach.

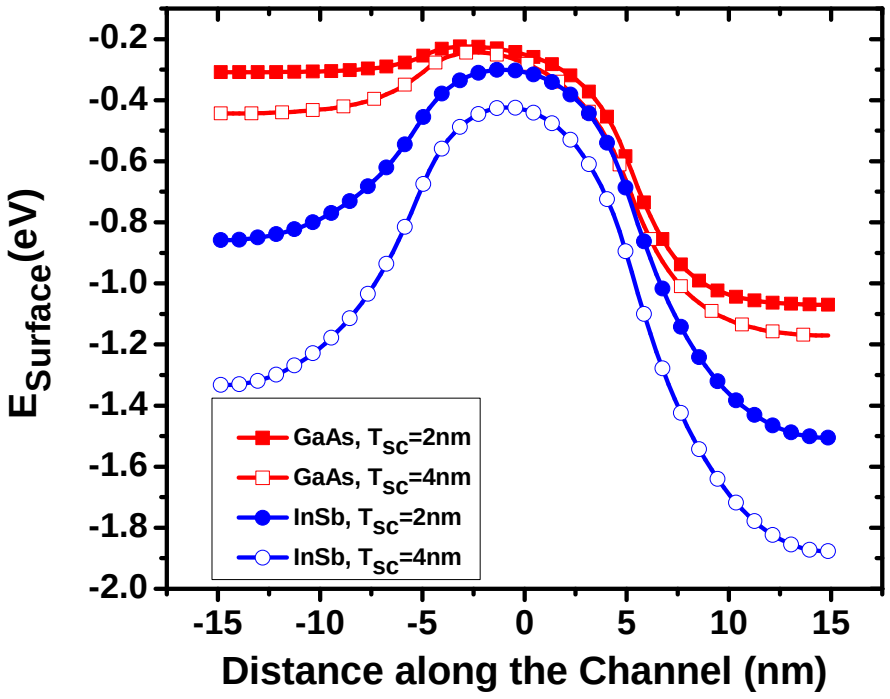

Figure 4.6: The narrowing of the potential barrier for two different materials: GaAs (red), InSb (blue) at two different channel thickness: 2 nm (closed symbols), 4 nm (open symbols)

The narrowing of the potential barrier for different materials is shown in

Figure 4.6. It is seen that the narrowing of the barrier is more for channel materials with lighter masses. Hence the SD tunneling is expected to be more in case of III-V devices.

In the simulations carried out in this section, the first ballistic transport model includes quantum confinement in the vertical direction by solving the one dimensional Schrödinger equation. And the carrier transport in each resulting subbands is then calculated using thermionic component only while ignoring any tunneling [71]. In the second ballistic transport model, the carrier transport is evaluated in each of the subbands by solving another set of one dimensional Schrödinger equation in the channel direction using the non-equilibrium Green's function (NEGF). In the latter model, the source-to-drain tunneling is accounted for.

The following channel materials were considered: Si, GaAs, InGaAs, InAs and InSb. Simulations are carried out for three channel thicknesses of 2, 3 and 4 nm and different channel lengths, ranging from 7 nm to 40 nm. The expected increased BTBT in these low bandgap devices can be compensated by using optimized architectures and the use of thin channels where quantum confinement leads to widening of the band gaps [91], and have been neglected in the following simulations for simplicity. The channel-source/drain junctions are considered abrupt as in previous chapters of this thesis.

Subthreshold slope variation in MOSFETs with different channel materials has been plotted in Figure 4.7 without considering source-to-drain tunneling, and in Figure 4.8, including source-to-drain tunneling. As already described in chapter 3, when S/D tunneling is ignored, the vertical quantum confinement alone does not alter the subthreshold slope and hence curves in Figure 4.7 are seen to huddle together. On the contrary, when S/D tunneling is taken into account, it is seen that the subthreshold slopes degrade rapidly with decreasing effective mass and increasing dielectric constant as we go from a silicon device to an InSb device.

It can also be seen that the subthreshold slopes of GaAs and InGaAs based

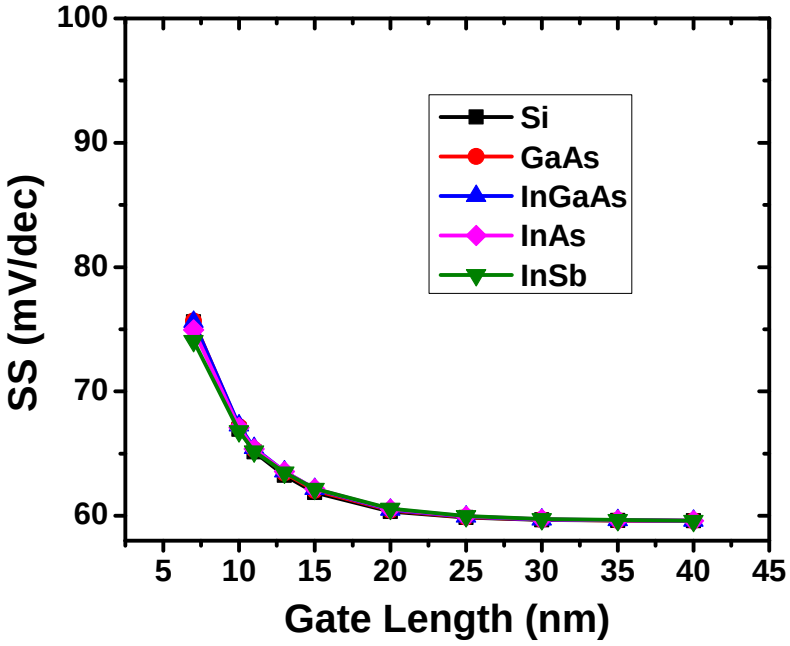

Figure 4.7: Subthreshold slope variation in MOSFETs with different channel materials, without considering source-to-drain tunneling (t_{sc} = 3 nm to ensure good electrostatics)

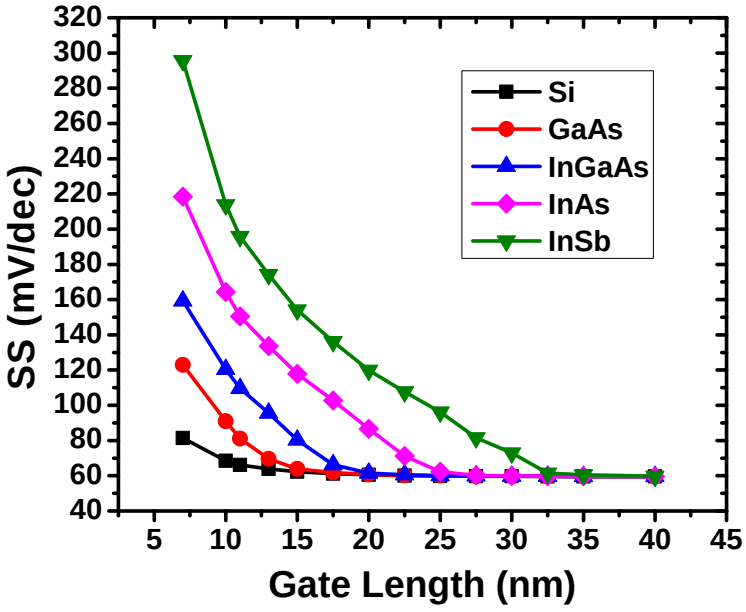

Figure 4.8: Subthreshold slope variation in MOSFETs with different channel materials, including source to drain tunneling (t_{sc} = 3 nm to ensure good electrostatics)

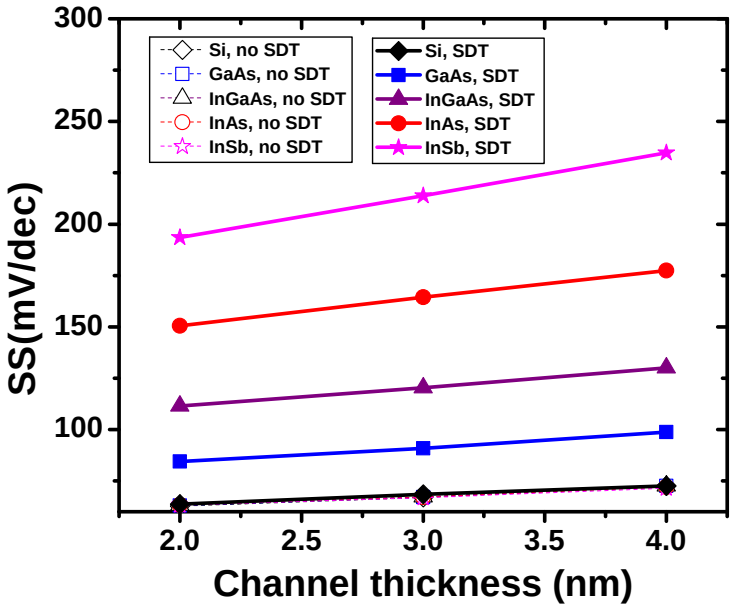

Figure 4.9: Subthreshold slope variation with channel thickness in MOSFETs with different channel materials, with and without considering source to drain tunneling (L_g = 10 nm)

MOSFETs deviate from the Si values at gate lengths around 15 and 20 nm respectively, while for other channel materials with lighter effective masses this length is well above 20 nm. So while SD tunneling is not a critical factor for Si devices for gate lengths larger than 10 nm, as has been reported in published literature, for example [89], it can cripple device operation at fairly large gate lengths if the channel material is changed to be Ge or a III-V material.

Figure 4.9 shows the variation of subthreshold slope with the channel thickness for devices with 10 nm gate lengths for the five different materials. It is seen that even with extreme geometries like t_{sc}=2 nm and L_g=10 nm which guarantee a good electrostatic control by the gate, SD tunneling is very damaging and leads to rapid degradation of the subthreshold slope in alternative channel materials.

4.4 Quantum Confinement and SDT

Confinement effective masses depend on crystal orientation as well as the thickness of the MOSFET channel. In the previous analyses, the effective masses used were that of the bulk semiconductors. However, it is known that an increase in the transport effective mass in thin semiconductor films is found compared to bulk material and this effect is observed more as channel thickness (t_{sc}) is scaled thinner and thinner. Using a tight binding approach, Liu et. al [92] have shown that in Si, although not much significant, this increase has been found to be around 10% for a 3 nm thick channel, causing m_t to rise to $0.22m_0$ from $0.19m_0$. Figure 4.10 shows the variation of the transport effective mass, m_t with the silicon channel thickness.

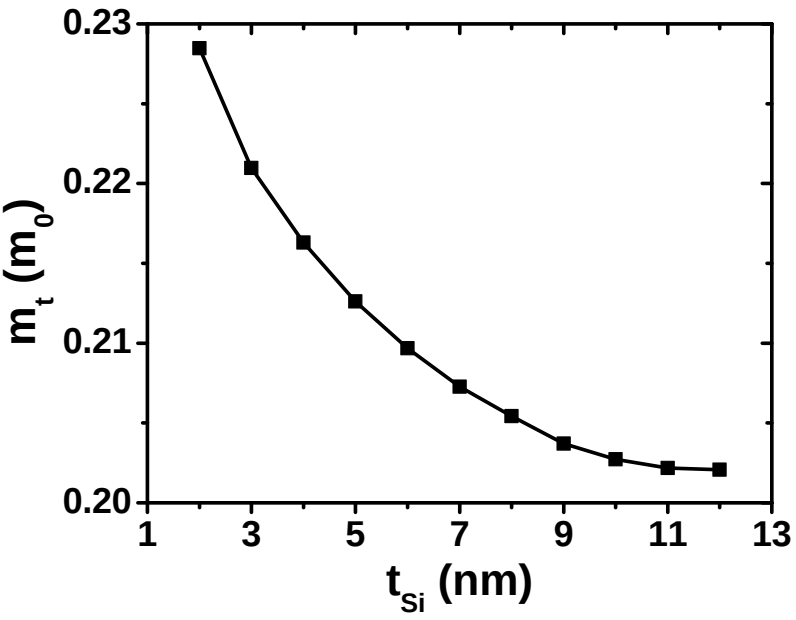

Figure 4.10: Variation of the transverse effective mass m_t with the Si body thickness [92]

In III-V materials this effect is much more pronounced due to the strong non-parabolicity of the Γ valley [73, 93–95]. For example, it has been demonstrated in [93], the effective mass model with parabolic bandstructure utilising the bulk effective mass is not valid in cases of strong quantum confinement, and full band calculations reported significant increase of the effective mass

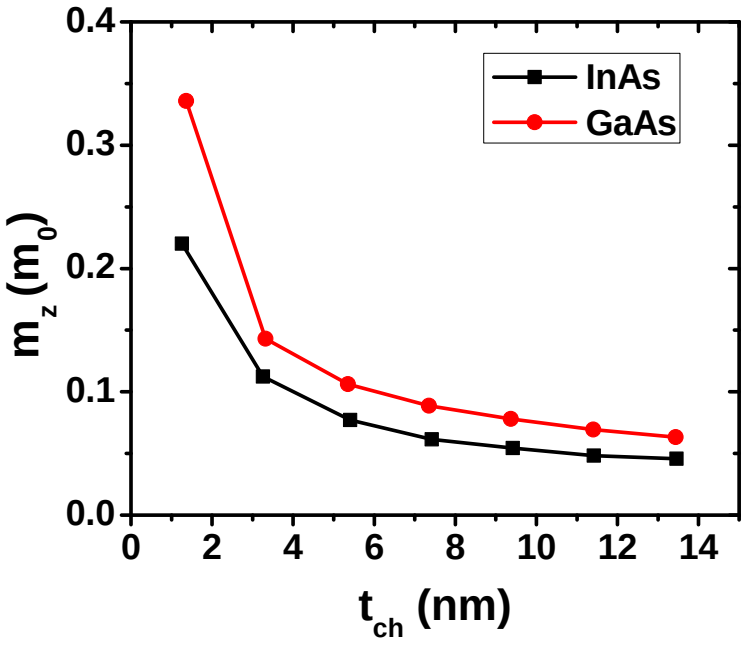

Figure 4.11: Confinement effective mass of electrons in the Γ valley as a function of the channel thickness for GaAs and InAs double gate MOSFETs [93]

with channel thickness scaling. The increase in the confinement effective mass in the Γ valley of GaAs and InAs as a function of the body thickness is plotted in Figure 4.11 (taken from [93]). Table 4.1 displays the efffective masses in bulk and in a semiconductor body with 3 nm thickness.

While increased effective masses of electrons can reduce the injection velocity and hence the on current, it can also help reduce the leakage current by reducing the tunneling transparency. Its impact on the SD tunneling leakage was hence studied to assess how this increase in the effective mass affects scalability in terms of the gate length. For this, a critical length is proposed to quantify the impact of tunneling. The *critical gate length*, L_{crit} has been defined as the gate length at which the subthreshold slope worsens by 2% due to source-to-drain tunneling.

Further simulations were carried out with the increased masses listed in Table 4.1, with GaAs and InAs devices as examples for demonstration. When

	Si	GaAs	InAs
Bulk Effective Mass, $m_{t,Bulk}$	0.2	0.067	0.023
Tight Binding Effective Mass, $m_{t,TB}$	0.22	0.17	0.12

Table 4.1: Comparison of the bulk effective mass and the effective mass taking into account the quantum confinement, calculated using a tight binding approach for Si [92], GaAs and InAs [93]. t_{sc} =3 nm

Channel Material	L_{crit} (nm)
Si	10
GaAs	15.5
InGaAs	20
InAs	26
InSb	32.5

Table 4.2: Criticial gate length (defined as the gate length at which inclusion of source to drain tunneling degrades the slope by 2%) for different channel materials

higher masses were used, the subthreshold slope improved and it was seen that the critical gate length where source-to-drain tunneling becomes a limiting factor decreased allowing comfortable scaling beyond 15 nm.

Channel Material	L_{crit} with m^*_{Bulk}	L_{crit} with m^*_{TB}	% improvement
GaAs	15.5	11	29
InAs	26	12.5	52

Table 4.3: Criticial gate lengths (in nm) calculated with bulk effective mass and effective mass obtained from Tight Binding bandstructure calculations and the percentage improvement

The comparison of the critical gate lengths obtained using bulk effective masses and the effective masses obtained from tight binding calculations available in existing literature, and the corresponding percentage decrease in the criticial length have been shown in Table 4.3. The critical gate length, L_{crit} is found to decrease by 29% for GaAs and by 52% for InAs MOSFETs, thus enabling more physical scaling of channel length than that predicted by previous calculations using bulk effective masses. Figure 4.12 shows the result graphically.

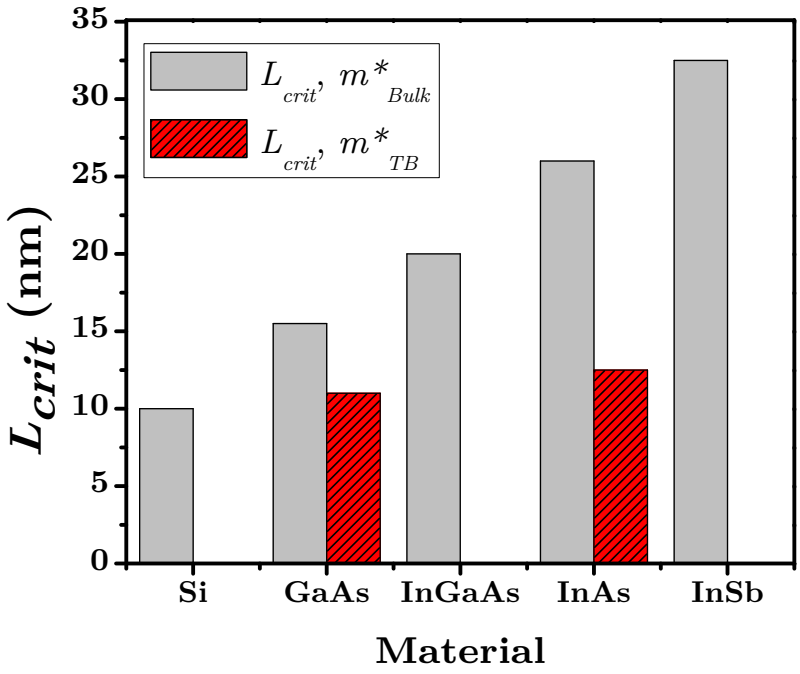

Figure 4.12: Critical gate lengths (in nm) calculated with m^*_{Bulk} and m^*_{TB}

4.5 Conclusions

The impact of source-to-drain tunneling is more severe in III-V MOSFETs than in Si devices. The channels with lower effective mass materials have worse subthreshold slopes. And this behaviour with different effective masses is displayed at longer gate lengths in III-V devices than expected in Si devices. Thus source-to-drain tunneling makes the devices with high mobility materials like III-V and Ge less scalable than a Si device, causing less aggressive shrinking of gate lengths along the roadmap beyond the 15-20 nm technology nodes. In other words, III-V devices can achieve higher on current and comparable short channel performance compared to a Si device only when the channel lengths are larger than the critical lengths.

Finally, when the increase in the effective masses with channel thickness scaling is taken into account, an improvement in the critical gate lengths is found, signalling a more optimistic scenario compared to the cases where bulk effective masses are used in the simulations.

Chapter 5

Conclusions and Future Perspectives

Contents

5.1 Conclusions

In this PhD thesis, the current state of non silicon channel MOS devices was ascertained through extensive literature survey, and then the short channel behaviour of these devices was explored via modeling and simulation. We began by providing a correction to the boundary conditions as applied in conventional potenial modeling schemes in MOSFETs. In the existing modeling approaches, the voltage drops in source and drain regions are ignored. It was found that this can lead to huge over-estimation of SCEs. To correct this, a model for an effective built-in potential was proposed, which when applied to the conventional models, is able to account for the impact of source and drain regions on the channel potential and hence the SCEs.

III-V devices display worse short channel behaviour than their silicon counterparts. The main focus of this dissertation work was on understanding the origin of the short channel effects (subthreshold slopes and drain induced barrier lowering). It was found that the quantum confinement does not have any impact on the SCEs, as long as tunneling leakages are neglected in the analysis. The detorioration in SCEs is mainly due to the worsened electrostatics of the short channel devices. Higher dielectric constants and smaller bandgaps

are accountable for the SCE degradation. The off-state characteristics of the devices are not affected by quantum effects, and hence classical simulations are able to capture them.

However, in the strong inversion regime of the device where the minority carriers are taken into account, quantum effects have to be considered. The increased dark space (due to smaller effective mass) in III-V devices results in an increase in the effective oxide thickness, which in turn increases the DIBL effect in the on-state. This was concluded using both quantum simulations with DD transport as well as DD simulations with quantum corrected charge profile using the Hansch model.

Simulations clearly showed that increased dielectric constant leads to an increase in the DIBL and the subthreshold slope, and that the DIBL is a weak function of the material's bandgap. Thus this part of the research work showed that the SCE degradation is very fundamental to III-V devices and is ascribed to their higher dielectric constants and smaller effective masses. Also, the incorporation of barrier layers in QWFET architecture was shown to cause further degradation of the SCEs.

In the final part of the thesis, the goal was to investigate the impact of the source-to-drain tunneling on the SCEs in III-V devices and predict the critical gate lengths at which its inclusion leads to significant difference compared to the case where tunneling is ignored. The impact of the increase of the effective mass due to carrier confinement in ultra thin films is also studied and it was concluded that the source-to-drain tunneling causes further degradation in the SCEs, but when the increased effective masses are used for calculations, we have more leeway and the scalability is not as bad as predicted when calculations are performed by taking the bulk effective masses instead.

Thus, to take advantage of the excellent transport properties of III-V/Ge materials, it is imperative to control the loss in terms of short channel effects. Hence device structures that offer tighter gate control, like the triple gate and gate all around/nanowire MOSFETs are good candidates for the introduction

of alternative channel materials.

5.2 Future Perspectives

Some suggested future works are as follows:

- The impact of the quantum confinement and material parameters on the threshold voltage roll-off in III-V devices can be pursued to get a more complete picture of SCE degradation.
- The on-state performace is impacted by the DIBL deterioration as demonstrated in this work. Its effect on the transistor delays can be studied to get some insights into circuit design issues that can come up with alternative channel material MOSFETs.
- The study can be repeated for III-V devices in different multi gate architectures other than the double gate: e.g. triple gate, Ω-gate, nanowire structures etc and quantify the advantages of better electrostatic control in such devices.
- While in this thesis the dielectric/channel interface imperfections were ignored, the inclusion of such non-idealities in the analysis can be done to see how much do they impact the device performance.
- Finally, comparison of the results of modeling and simulation results needs to be done with experimentally measured values.

List of Publications

Journals

- T. Dutta, Q. Rafhay, R. Clerc, J. Lacord, S. Monfray, G. Pananakakis, F. Boeuf and G. Ghibaudo, "Impact of quantum effects on the short channel effects of III-V nMOSFETs in weak and strong inversion regimes," *Solid-State Electronics*, Volume 88, pp 43-48, October 2013

International Conferences

- T. Dutta, Q. Rafhay, G. Pananakakis and G. Ghibaudo, "Modelling of the impact of source/drain regions on short channel effects in MOSFETs," in *Proceedings of the 14th International Conference on Ultimate Integration on Silicon (ULIS)*, pp.69-72, Warwick, UK, March 2013

- T. Dutta, Q. Rafhay, R. Clerc, J. Lacord, S. Monfray, G. Pananakakis, F. Boeuf and G. Ghibaudo, "Origins of the short channel effects increase in III-V nMOSFET technologies," in *Proceedings of the 13th International Conference on Ultimate Integration on Silicon (ULIS)*, pp.25-28, Grenoble, France, March 2012

Posters

- T. Dutta, Q. Rafhay, R. Clerc and G. Pananakakis, "Modeling and simulation of alternative channel material MOSFETs," presented at the *12th Dresden Microelectronics Academy*, Dresden, Germany, September 2012

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