



Development of passive circuits in nanowire-membrane technology in millimeter wave frequencies: application to functionalized interposer

Júlio Mota Pinheiro

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Microélectronique de l'USP**

dans le **École Doctorale EEATS et le PPGEE de l'EPUSP**

Development of passive circuits in nanowire-membrane technology in millimeter wave frequencies: application to functionalized interposers

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RESUMO

Este trabalho visa o desenvolvimento de circuitos passivos em banda de ondas milimétricas no interposer denominado MnM – *metallic nanowire-filled membrane*. Esse interposer está inserido no contexto onde a miniaturização dos circuitos passivos devido a elevada frequência de operação (grosso modo acima de 10 GHz até 300 GHz para ondas milimétricas) leva com que seja interessante a inserção dos circuitos passivos dentro de tecnologias integradas como CMOS, mas que devido às limitações ligadas a tecnologia não atingem uma alta qualidade, sendo por isso mais interessante em questão de performance e custo a utilização de um substrato auxiliar para a concepção de circuitos passivos que possibilite a sua integração com circuitos ativos em tecnologia integrada; substrato esse denominado de interposer. Para o desenvolvimento de um bom interposer, é necessário que apresente linhas de transmissão e vias de alta qualidade. O interposer MnM é uma membrana de alumina de baixo custo que tem pela sua fabricação naturalmente nanoporos que podem ser utilizados para o crescimento de nanofios de cobre. Para o desenvolvimento desse interposer e a apresentação de circuitos sobre ele, o processo de fabricação é aprimorado, com o enfoque no crescimento de nanofios de maneira localizada e no rendimento das fabricações. O substrato é caracterizado eletricamente para extração de perdas e da sua constante dielétrica, que verificou-se ser influenciada pelos nanoporos. Com o aprimoramento do processo de fabricação, vias de nanofios são desenvolvidas e sua performance analisadas no contexto de uma transição entre uma face e outra do substrato através de um modelo elétrico relacionado ao leiaute físico validado pelos resultados de medida. Para o modelo elétrico, uma abordagem analítica e outra matricial são propostas, com a verificação que essa via se comporta como uma via sólida com uma condutância que leva em conta o material dos nanofios e a sua densidade superficial. Verifica-se que as vias de nanofios apresentam uma performance estado-da-arte, além de suas dimensões como raio e espaçamento entre vias serem diminutas, ditadas somente pela mínima dimensão alcançada na fotolitografia. Indutâncias 3-D do tipo solenoide de duas, três, cinco e dez espiras que fazem uso dessas vias são propostas e analisadas, com a proposta de um modelo elétrico, que se relaciona ao seu leiaute físico, para ser usado por projetistas. Essas indutâncias são compactas devido ao tamanho diminuto das vias de nanofios além de apresentarem uma frequência de ressonância elevada, 98 GHz para a indutância de

duas espiras. Finalmente, um modelo distribuído novo para linhas de transmissões do tipo microfita com efeito de onda lenta, causado pelos nanofios, é proposto para gerar uma facilidade na sua concepção e simulação, já que sua simulação eletromagnética apresenta alto custo computacional. Esse mesmo modelo é também utilizado para linhas de transmissão em tecnologia PCB, que apresentam o mesmo efeito de onda lenta, mas com frequência de operação em micro-ondas. Dessa maneira, esse trabalho apresenta um avanço significativo para o interposer MnM, apresentando no final um interposer para ondas milimétricas completamente funcional.

Palavras-chave: Interposer, ondas milimétricas, nanotecnologia, interconexão 3-D, via de alta densidade, linha de onda lenta, óxido de alumina anódica (AAO).

ABSTRACT

This work aims at the development of passive circuits in millimeter-wave frequency in the interposer called MnM – metallic nanowire-filled membrane. This interposer is inserted in the context where the miniaturization of passive circuits due to the high operating frequency (roughly above 10 GHz up to 300 GHz for millimeter-waves) makes it interesting to insert passive circuits in integrated technologies such as CMOS, but that due to the limitations linked to the technology they do not present high quality, being therefore interesting in terms of performance and cost, the use of an auxiliary substrate for the design of passive circuits that allows their integration with active circuits in integrated technology; this substrate is called an interposer. For the development of a good interposer, it is necessary that it presents high quality transmission lines and vias. The MnM interposer is a low cost alumina membrane that naturally has nanopores caused by its fabrication process that can be used to grow copper nanowires. For the development of this interposer and passive circuits on it, the manufacturing process is improved, with the focus on the growth of nanowires in specific regions and on the fabrication yield. The substrate is electrically characterized for extracting its losses and its dielectric constant, which has been shown to be influenced by the nanopores. With the improvement of the manufacturing process, nanowire-vias are developed and their performance analyzed in the context of a transition between one face and another of the substrate through an electrical model related to the physical layout validated by the measurement results. For the electrical model, an analytical and a matrix approach are proposed, with the verification that the nanowire-via behaves as a solid via with a conductance that takes into account the material of the nanowires and their surface density. It is verified that the nanowire-vias have state-of-the-art performance, in addition to its small dimensions such radius and pitch between vias, dictated only by the minimum dimension achieved in photolithography. Two, three, five and ten spires solenoid-type inductions that make use of these vias are proposed and analyzed, with the proposal of an electrical model, which relates to its physical layout, to be used by designers. These inductors are compact, due to the small size of the nanowire-vias, and have a high self-resonance frequency, 98 GHz for two-spiral inductance. Finally, a new linear electric model for microstrip transmission lines with slow-wave effect caused by the nanowires is proposed, to facilitate its design and simulation, since its electromagnetic simulation

presents a high computational cost. This same model is also used for transmission lines in PCB technology, with a physical layout that creates the same slow-wave effect but with operating in microwave frequency. Thus, this work presents a significant advance for the MnM interposer, presenting a fully functional millimeter wave interposer.

Keywords: Interposer, millimeter wave, nanotechnology, 3-D interconnection, high-density via, slow-wave transmission line, anodic alumina oxide (AAO).

RESUME

Ce travail vise à développer des circuits passifs en ondes millimétriques dans l'interposeur appelé MnM - metallic nanowire-filled membrane. Cet interposeur s'inscrit dans le contexte où la miniaturisation des circuits passifs due à la haute fréquence de fonctionnement (environ supérieure à 10 GHz jusqu'à 300 GHz pour les ondes millimétriques) rend intéressante l'insertion de circuits passifs dans des technologies intégrées telles que le CMOS, mais qui en raison des limitations liées à la technologie ne présentent pas une qualité élevée, étant donc plus intéressant en termes de performance et de coût l'utilisation d'un substrat auxiliaire pour la conception de circuits passifs qui permet leur intégration avec des circuits actifs en technologie intégrée ; ce substrat est appelé interposeur. Pour le développement d'un bon interposeur, il est nécessaire qu'il présente des lignes de transmission et des vias de haute qualité. L'interposeur MnM est une membrane d'alumine à faible coût qui possède par sa fabrication des nanopores naturels pouvant être utilisés pour la croissance de nanofils de cuivre. Pour le développement de cet interposeur et la présentation des circuits passifs, le processus de fabrication est amélioré, l'accent étant mis sur la croissance des nanofils de manière localisée et sur le rendement de la fabrication. Le substrat est caractérisé électriquement pour l'extraction des pertes et sa constante diélectrique, dont on a constaté qu'elle était influencée par les nanopores. Avec l'amélioration du processus de fabrication, les voies de nanofils sont développées et leurs performances analysées dans le cadre d'une transition entre une face et une autre du substrat grâce à un modèle électrique lié à la disposition physique validée par les résultats des mesures. Pour le modèle électrique, une approche analytique et une autre matrice sont proposées, avec la vérification que cette voie se comporte comme une voie solide avec une conductance qui prend en compte le matériau des nanofils et leur densité surfacique. Il est vérifié que les voies de nanofils ont des performances de pointe, en plus de leurs dimensions telles que le rayon et l'espacement entre les voies sont faibles, dictées uniquement par la dimension minimale atteinte en photolithographie. Les inductions de type solénoïde à deux, trois, cinq et dix spires qui utilisent ces voies sont proposées et analysées, avec la proposition d'un modèle électrique, qui concerne sa disposition physique, à utiliser par les concepteurs. Ces inductances sont compactes en raison de la petite taille des voies de nanofils, et ont une fréquence de résonance élevée, 98 GHz pour les inductances à deux spires. Enfin, un nouveau

modèle électrique pour les lignes de transmission de type microruban avec un effet d'onde lente causé par les nanofils est proposé pour faciliter sa conception et sa simulation, car sa simulation électromagnétique présente un coût de calcul élevé. Ce même modèle est également utilisé pour les lignes de transmission en technologie PCB, qui présentent le même effet d'onde lente mais avec une fréquence de fonctionnement en micro-ondes. Ainsi, ce travail présente une avancée significative pour l'interposeur MnM, en présentant un interposeur d'ondes millimétriques pleinement fonctionnel.

Mots clés : Interposeur, ondes millimétriques, nanotechnologie, interconnexion 3-D, voie à haute densité, ligne à ondes lentes, oxyde d'alumine anodique (AAO).

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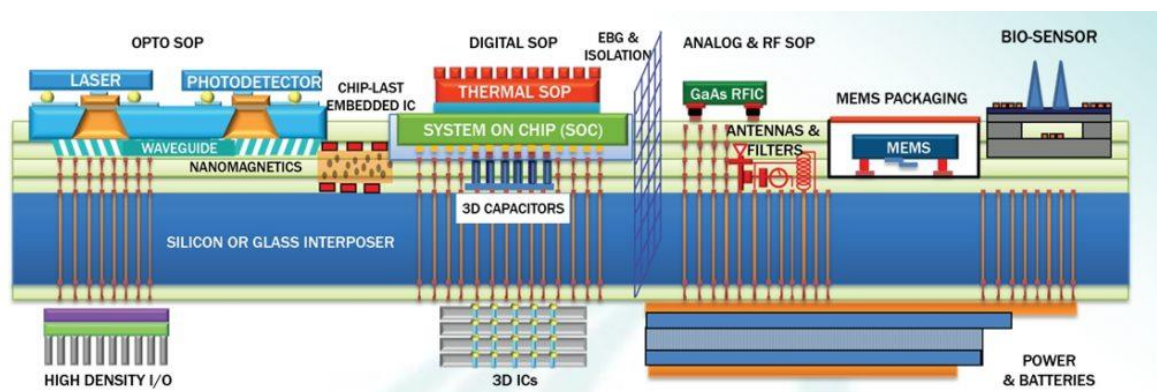
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INTRODUCTION

From a consumer market point of view, devices must have low-cost, low power consumption and small dimensions. At mm-wave frequencies, i.e. from 30 GHz to 300 GHz, with the reduced size of distributed passive devices based on transmission lines, their on-chip integration with active circuits is possible, but they still occupy a large surface area of advanced CMOS technologies necessary at mm-wave frequencies, increasing costs prohibitively. Moreover, only mm-wave passive circuits (couplers, baluns, filters, etc.) with poor quality factor can be realized in standard CMOS/BiCMOS technologies, due to the very small thickness of the back-end-of-line (BEOL). The alternative solution is to fabricate the passive devices on a low-cost interposer with good RF performance. In that case, the active circuits would be fabricated on the most appropriate technology and integrated onto the interposer.

In the last ten years, much effort has been put forth to develop platforms where CMOS chips and/or MEMS, optical links, etc., are integrated onto interposers [1], [2]. An interposer is a platform similar to a PCB, optimized for a digital and/or radio frequency (RF) role. A range of integrated circuits (ICs) in different technologies can be integrated into the interposer, with its function to provide a platform with excellent performance for signal interconnection between different ICs and circuits. This is achieved using a good dielectric substrate as the interposer that has a good redistribution layer and through-substrate-vias (TSVs). A view of the general capacities of an interposer is shown in Figure 1.

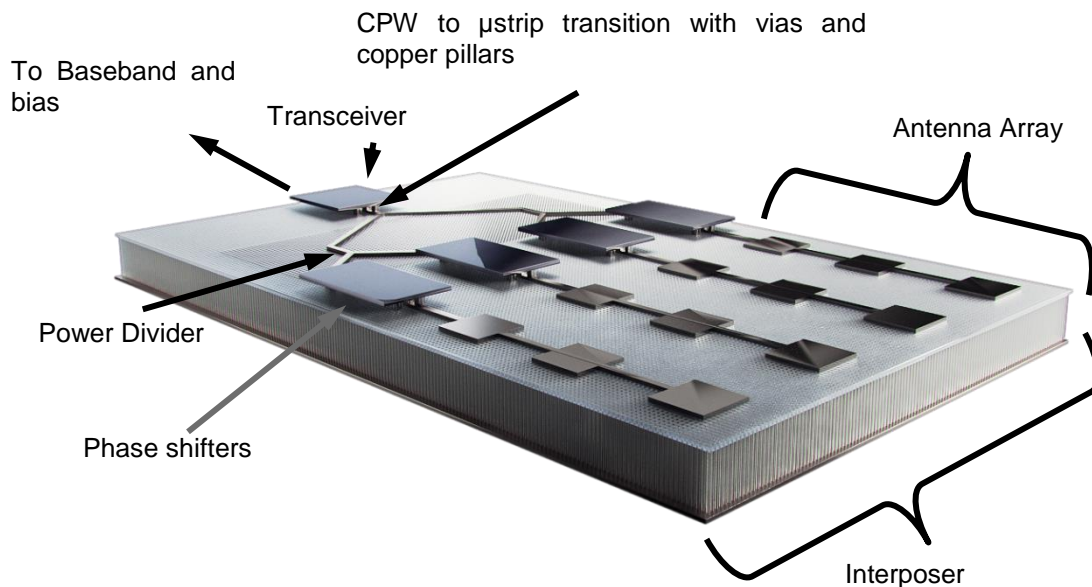
Figure 1 – Example of general applications of an interposer.



Source: Georgia Tech PRC.

A good interposer for mm-wave applications must have redistribution layers with high quality transmission lines, TSVs with good performance, among passive devices as inductors, transformers, couplers, antennas, interconnection posts, among others. In that context, the work presented in this thesis focuses on an interposer for mm-wave applications. A typical application of the mm-wave interposer that has been considered in this work is described in Figure 2, where a transmission/reception chain is shown. A baseband signal is connected to a transceiver, transferred to the interposer with interconnection posts, with TSVs connecting the baseband signal from the bottom layer to the transceiver on top, following with power dividers and phase shifters feeding an antenna array.

Figure 2 – Example of a mm-wave interposer, depicting a transmission/reception chain.



Interposers were reported in the literature using different materials such as glass [1], silicon [2], high resistivity silicon [3], liquid crystal polymer [4], among others [5]. **This work helps to develop passives devices in a new interposer substrate called metallic nanowire-filled membrane (MnM) [6].** This interposer is an anodic alumina oxide (AAO) membrane that has well-organized nanopores, where metallic copper nanowires can be grown inside, making it easier to have nanowire-via TSVs with good performance [7], [8]. The development of nanowire-vias makes it possible to have 3-D interconnections and circuits (for instance 3-D inductors). Apart from that, a wide range of transmission lines with a wide range of characteristic impedance and effective

dielectric constant can be fabricated such as standard microstrip lines [6], coplanar waveguides (CPW) [6], substrate integrated waveguides [9] and specially slow-wave microstrip lines (SMS) [10], [11]. **This work helps to develop the MnM substrate aiming on the fabrication process for passive circuits, substrate characterization, nanowire-vias, 3-D inductors and an electrical model for SMS lines.**

The interposer technology is presented in chapter 1. The fabrication process for passive devices on the MnM-platform is carefully described. Then, all the improvements to allow the fabrication of high-performance nanowire-vias are discussed. Next, the mm-wave characterization of the MnM substrate using open-ended microstrip stubs is presented. The resonant frequency of these stubs is measured and modeled to obtain the substrate dielectric constant and tangent loss. The characteristics of the substrate is then verified with the design and measurement of a filter based on short-ended microstrip stubs.

In chapter 2, nanowire-via transitions and 3-D inductors are studied at mm-waves. The nanowire-via transition uses coplanar waveguides (CPWs) to connect the top to the bottom of the MnM substrate. A simple lumped-element model is derived for the transition. State-of-the-art performance is obtained for the vias insertion loss. Next, the nanowire-via itself is mathematically modelled to help future designers. Then, based on the modeled developed for the vias, compact 3-D inductors are designed, fabricated measured and analyzed, and a lumped-element model related to the physical layout is derived for these structures.

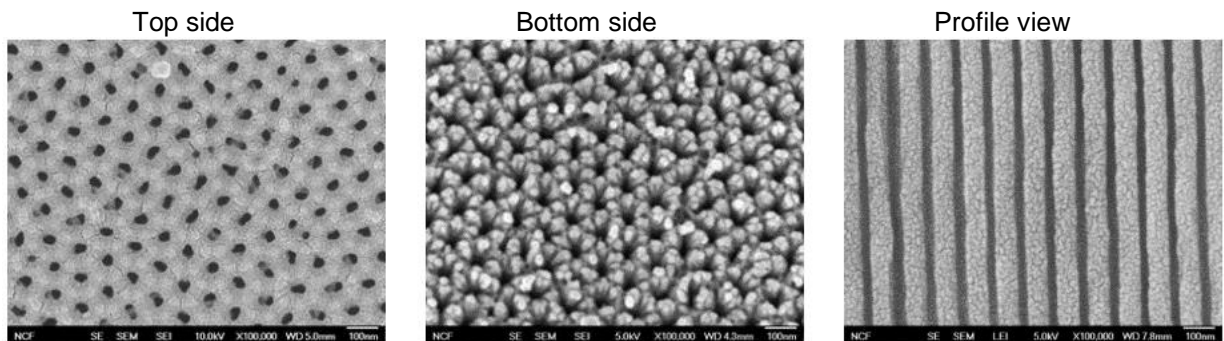
In chapter 3, a distributed model for the SMS line on the MnM substrate is presented. The model is based on a classical *RLGC* transmission line model, and because of the nanowires, a resistance, inductance and magnetic mutual coupling inductance are added. The same model is applied to a transmission line on PCB technology that have the same configuration as the SMS lines on the MnM substrate. A good agreement between measurements and the model simulations is obtained for both the MnM and the PCB technologies.

1 TECHNOLOGY DESCRIPTION AND CHARACTERIZATION

1.1 Introduction

The MnM (Metallic-nanowire-filled-Membrane) is an alumina substrate obtained through electrochemical oxidation of aluminum in specified anodization voltages, as presented in [12]. The membrane is referred on the literature as anodic alumina oxide – AAO. In the anodization process several nanopores organized with different geometric parameters (pore diameter and interpore distance) are created as shown in Figure 3. Different acids can be used in the formation process such as oxalic acid, sulfuric acid or phosphoric acid with an electric potential interval used for each solution. In this way, this technology is versatile, since the geometric parameters can be adjusted on the substrate fabrication depending on the solution used and the electrical potential, and there is not a fixed size limit for the sample.

Figure 3 – Nanopores in a membrane with 40 nm pore diameter.



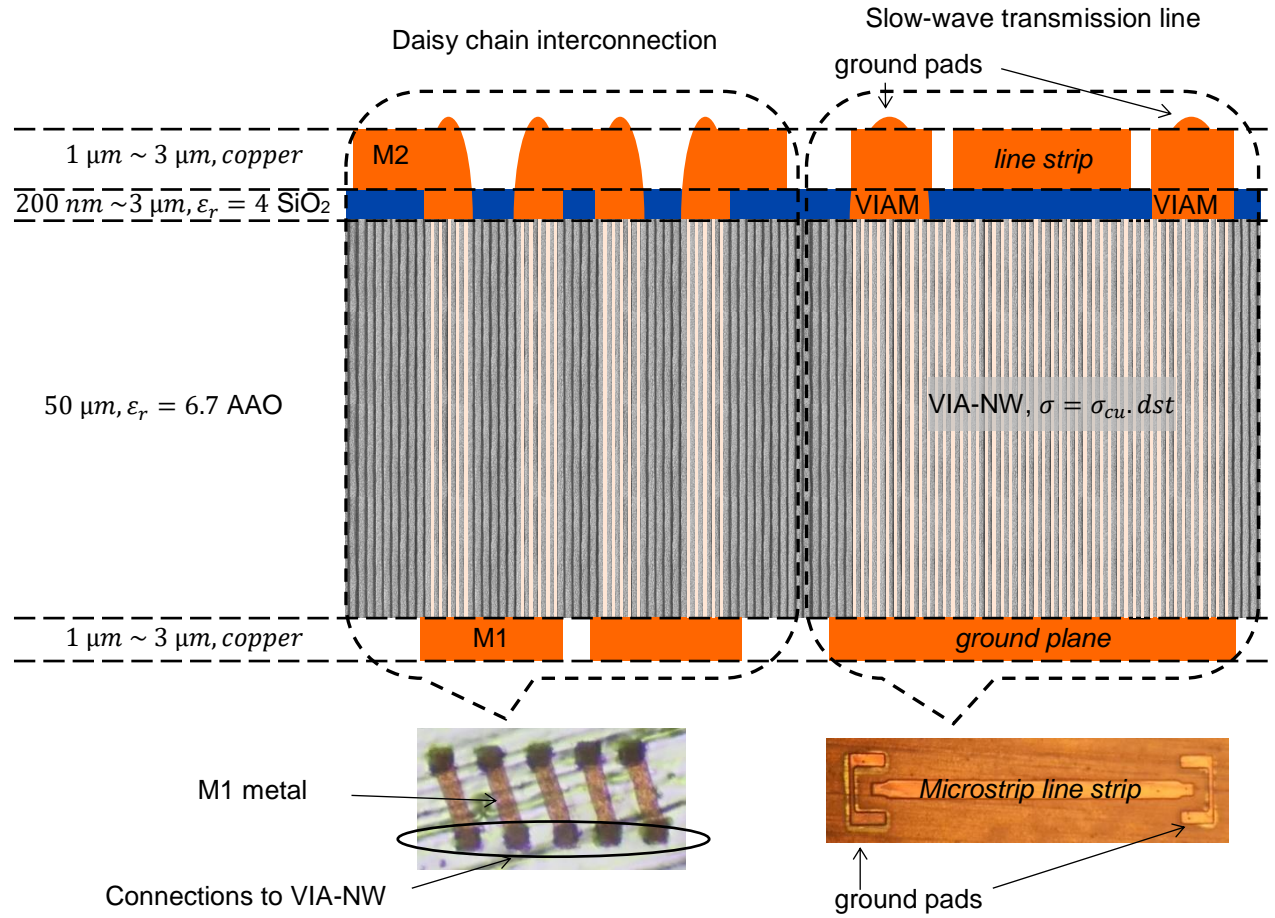
Source: InRedox – Application Note: “Are the Two Sides of Isotropic AAO Identical?”.

This membrane is used as a template for copper nanowire growth inside the pores, which is the greatest difference when comparing to other mm-wave interposers, such as low temperature co-fired ceramic (LTCC), glass, silicon, liquid crystal polymer (LCP) and others. Until the beginning of this work, the MnM substrate has been used to fabricate only slow-wave transmission lines [10], [11] as shown in the next section.

The MnM interposer technology can be seen in Figure 4 with all possible layers. From the bottom to the top of the substrate, there is a copper layer, M1, used as ground plane for microstrip lines. M1 is also the base layer for nanowire growth. Then, there is the nanoporous membrane, with air-filled or copper-filled (VIA-NW) nanopores,

having pore area density dst . On the surface, there is a dielectric oxide layer composed of silicon dioxide (SiO_2), and the top copper layer (M2). The connection of M2 with the VIA-NW is done with selective removal of the SiO_2 layer, forming a connection called VIAM. All the thicknesses and characteristics of the different layers are given in Figure 4.

Figure 4 – Technology cross section of the MnM interposer.



Based on the MnM technology illustrated in Figure 4, a family of different passive circuits can be fabricated. The left part of Figure 4 shows an example of interconnection where M1 and M2 are connected through VIAM and VIA-NW. On the right part of Figure 4 there is an example of cross-section view of a slow-wave microstrip line, where M2 is used for the signal and M1 for the ground plane. The signal strip is separated from the nanowires (VIA-NW) by the SiO_2 layer, creating the slow-wave effect that will be explained in Chapter 3. For measurement, coplanar (GSG) probes

are normally used and the VIA-NW and VIAM are to connect the ground pads to the ground plane.

The chapter is organized as follows to completely describe the technology. In section 1.2 the fabrication process of structures on top of the MnM substrate is presented, first with the process used before this work shown in section 1.2.1, followed by the optimizations performed in section 1.2.2. In section 1.3 a high frequency electrical characterization of the MnM substrate is performed, using open-ended microstrip stubs (section 1.3.1) followed by a verification with the design and measurement of a filter at mm-wave frequencies, and based on short-ended microstrip stubs (section 1.3.2). Section 1.4 presents a summary of the points presented in this chapter.




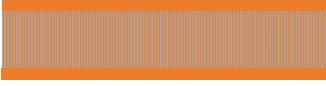
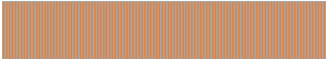
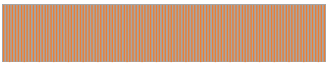
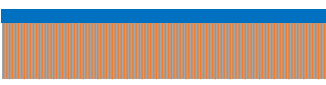
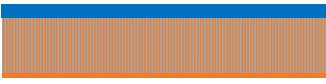
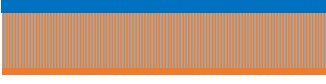
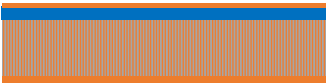

1.2 Fabrication process of circuits on the MnM Substrate

In this section, the fabrication process for circuits on the membrane is presented. First, the fabrication process used before this work is presented in section 1.2.1. This fabrication process allowed only slow-wave microstrip lines with nanowires to be fabricated all over the membrane, and only in one type of membrane (a 50- μm -thick membrane from Synkera with 55-nm pore diameter), since this combination of thickness and pore diameter was the best for nanowire growth. In section 1.2.2, it is shown how the fabrication process was modified to allow a range of different circuit with different layouts to be fabricated in a single run, and in membranes with different pore diameters.

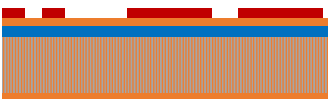
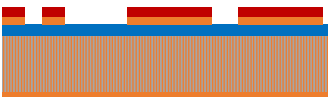
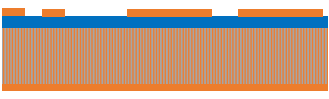
1.2.1 Former fabrication process

The fabrication process for making circuits using 50- μm -thick AAO membranes before the start of this work is described in Table 1. Using those steps, it was not possible to grow nanowires selectively on the membrane, which limited the types of circuits that were possible to fabricate.

Table 1 – Fabrication process for circuits on the MnM substrate before the start of this work.

Steps	Membrane visualization	Process/Technique	Conditions
1 Membrane cleaning		Boiling (5 minutes) for each solvent	1 – Trichloroethylene 2 – Acetone 3 – Isopropyl alcohol
2 Copper deposition on bottom of the membrane (30 nm thickness)		Sputtering	70 W; 2 mTorr; 1m30s
3 Bottom copper thickening		Electroplating	Acid copper sulfate solution from EPI and copper electrodes. 30 min with 100 mA
4 Nanowire growth through the nanopores until the formation of a copper film on the top surface		Electroplating	Same solution as last step with 60 mA ~ 100 mA (The membrane is immersed in water with developer in a vacuum chamber to lower the surface tensions and fill the nanopores with water)
5 Copper removal from the top and bottom leaving only the nanowires		Mechanical removal with a tweezer	The border of the membrane is broken to get the copper layer from top and bottom
6 Membrane cleaning		Boiling (5 minutes) for each solvent	1 – Trichloroethylene 2 – Acetone 3 – Isopropyl alcohol
7 SiO ₂ deposition on the top layer		PECVD	75 sccm – N ₂ O 30 sccm – SiH ₄ 200 W, 320 °C
8 Titanium deposition (20 nm) and copper (30 nm) on the bottom layer for the ground plane		Sputtering	Titanium: 100W 2 mTorr; 1 min Copper: 70W; 2 mTorr; 1 min 30 s
9 Bottom copper thickening		Electroplating	Same solution as step 4: 40 min 200 mA
10 Titanium deposition (20 nm) and copper (30 nm) on the bottom layer for the top surface – surface where the circuits are fabricated		Sputtering	Titanium: 100W 2 mTorr; 1 min Copper: 70W; 2 mTorr; 1 min 30 s
11 Top copper thickening		Electroplating	Same solution as step 4: 40 min 200 mA

(continues in the next page)

(continuation of Table 1)			
Steps	Membrane visualization	Process/Technique	Conditions
12 Photolithography (mask)			Thick photoresist – 3 to 4 μm
13 Top copper corrosion		Wet etching	Chromium etching solution: perchloric acid and cerium ammonium nitrate
14 Photoresist removal		Boiling (5 min)	Acetone. Afterwards cleaning with DI water

This process has been improved in order to fabricate other types of structures that need nanowires only in specific parts of the membrane such as TSVs, making a good electrical contact between the bottom and the top of the membrane; specially to make the fabrication process more reliable. The motivations for changes are listed below, and addressed in section 1.2.2.

In step 5, the copper is removed from the top and bottom of the membrane. The top copper is removed to allow the deposition of the SiO_2 layer. The bottom is removed only to prevent the mechanical deformation due to the mismatch in thermal coefficient during the SiO_2 deposition step (Table 1; step 7). The deposition is executed using the plasma-enhanced chemical vapor deposition (PECVD) technique, which requires temperatures around 320 °C. Having a membrane with copper on one side and depositing SiO_2 on the other side, leads to a considerable mechanical stress on the membrane, caused by different thermal expansion coefficients between the copper, the alumina membrane and SiO_2 . For some circuits it is important to maintain the copper layer to ensure a good electrical contact between the nanowires and the copper on one side.

Also in step 5, the top copper grown after the nanowires is removed with tweezers that is only possible since it is a contiguous layer. This removal technique is not suitable for processes with nanowires in specific regions of the membrane.

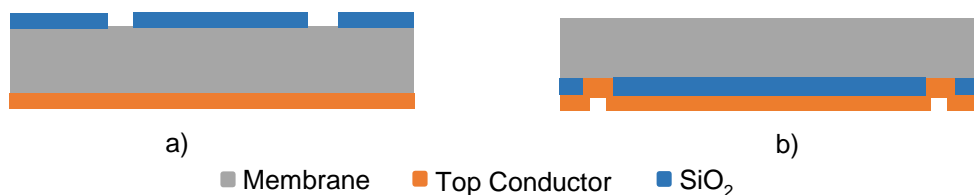
The definition of structures on the copper using a corrosion method (Table 1; steps 11-13) gives a significant difference in thickness between the border and the center of the membrane; a better thickness control is needed.

1.2.2 Fabrication Process Optimization

The first change in the fabrication process was in the SiO₂ deposition technique (Table 1; step 7) from PECVD to radiofrequency (RF) magnetron reactive sputtering. With the sputtering technique it is possible to deposit SiO₂ at lower temperatures (about 100 °C), which allows the deposition on the membrane with copper in one face with reduced mechanical stress.

The development of the selective nanowire growth was necessary for the realization of nanowire-vias (VIA-NM). With this technique, it is possible to fabricate slow-wave microstrip lines, standard microstrip lines, CPW, nanowire-vias on the same substrate and in the same fabrication run. For this selective growth, two possibilities for masking the membrane nanopores were proposed and explored. The first one consists of a SiO₂ mask on the top of the membrane, and copper on the bottom, with nanopores exposed only in selected areas, as shown in Figure 5 a). The second also uses SiO₂ as mask, with copper on top of this mask, leaving all nanopores exposed, as shown in Figure 5 b).

Figure 5 – Two masking possibilities for growing nanowires inside the membrane, in a) with the SiO₂ layer on the top and in b) with the SiO₂ layer on the bottom surface.

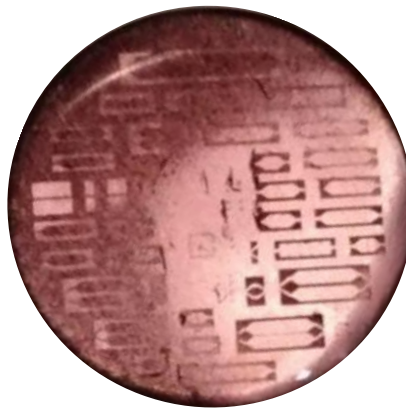


Looking at the solution proposed in Figure 5 a) the fabrication procedure would be to first deposit the SiO₂ layer on top followed by the bottom copper layer, and then etching the SiO₂. The solution proposed in Figure 5 b) is fabricated by first depositing the bottom SiO₂ layer, etching it and then depositing the copper layer below. The latter fabrication process implies that a SiO₂ wet etching solution can penetrate through the nanowires from the exposed surface, attacking the layer from both sides and diminishing the mask adherence and resolution. In the former fabrication process, all

the nanopores are covered leading to a more controlled SiO₂ etching, being it the main reason for choosing the Figure 5 a) masking solution.

Initial attempts to selectively grow nanowires were performed using only the sputtered SiO₂ as mask, as will be explained later, not being successful and often resulting in no nanowire growth or growth all over the membrane, as shown in Figure 6. Since it was suspected that the masking choice was not the only problem, further investigations were performed on all process parts involved, the SiO₂ etching procedure, the deposited SiO₂ characteristics, and the electrodeposition solution employed and its biasing.

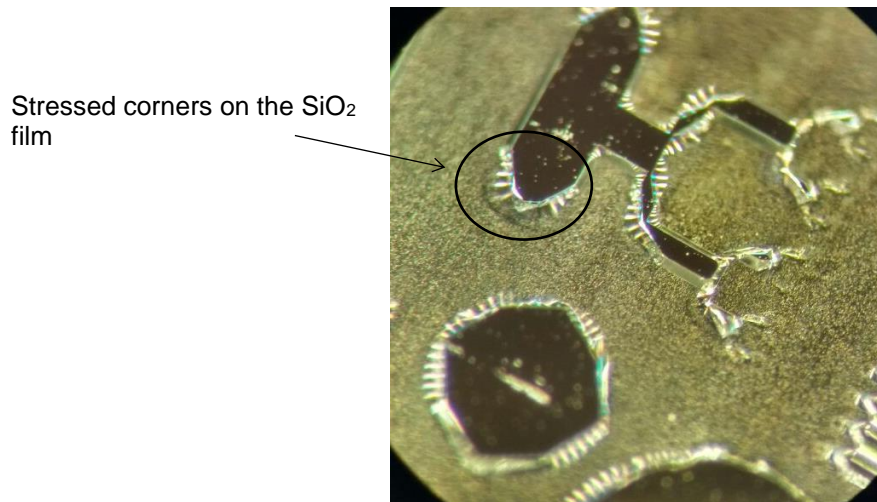
Figure 6 – Example of unsuccessful selective nanowire growth, with nanowires all over the membrane in copper color, whereas the designated regions are inside the geometric forms.



For etching the mask and exposing the nanopores, a buffered oxide etch (BOE) solution is used. A SiO₂ layer deposited on a silicon substrate on the same sputtering run is used to approximate the etching time. After several fabrication tests, it was observed that the time needed to properly expose the nanopores to have a good nanowire growth is about three to four times higher than the time for the SiO₂ on the silicon. This implies that the mask is etched an extended time after defining the exposed regions, diminishing its resolution. This might be caused by SiO₂ deposition inside the membrane nanopores. To improve the overall mask resolution, the initial 1- μ m-thick mask used in the initial fabrications was reduced to about 300 nm in thickness.

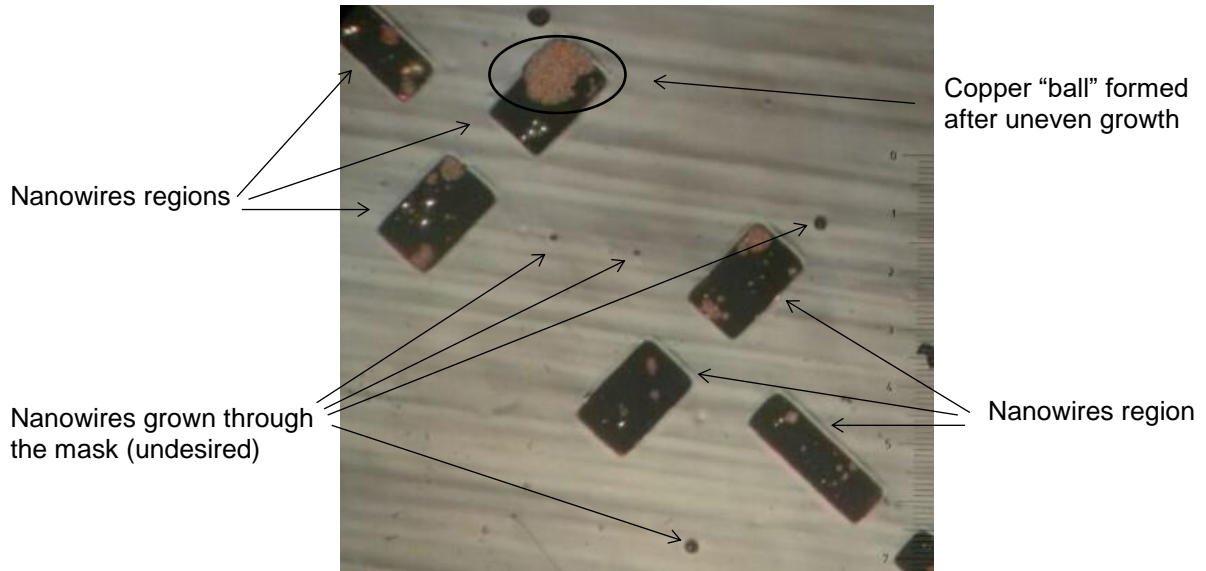
Further investigations on the SiO_2 characteristics showed that the initial recipe employed for its sputtered deposition formed an oxide with inner tensions, as shown in Figure 7. This characteristic can create cracks inside the film, making it porous and leading to nanowire growth outside designed areas. To find a more suitable deposition recipe, several depositions were done and their characteristics analyzed. As a result, the deposition gases flow ratio were changed and to further avoid thermal stress during the process, the substrate temperature is now kept low, with successive 10-minutes spaced depositions. Even with this optimized SiO_2 mask, as a preventive measure, the photoresist used for its etching is left as a second barrier for the nanowire growth mask.

Figure 7 – SiO_2 on top of a silicon substrate where a film with higher inner tensions and stressed corners is shown.



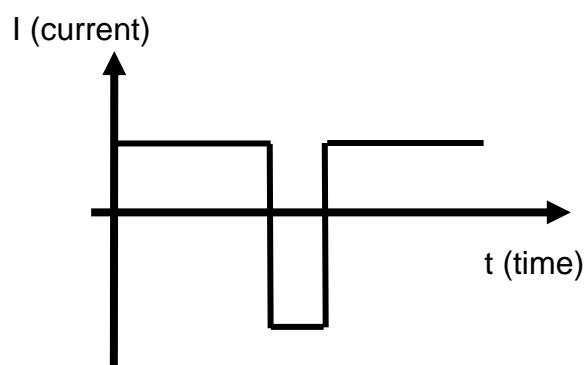
The electrodeposition solution from EPI (<https://www.epi.com/>) with DC current was used successfully for the nanowire growth in the entire membrane (Table 1; step 4). However, in the selective case, the growth was uneven and disorganized. In some areas, no nanowire growth was observed at all with either of the masking possibilities shown in Figure 5. In other areas, the growth was much faster, leading to the formation of copper “balls” and unbalanced growth between nanowire regions, as is exemplified in Figure 8.

Figure 8 – Membrane on the microscope after nanowire growth. The dark brown regions are areas stipulated for nanowire, with disorganized growth. Some regions had a faster growth than others, forming copper “balls”.



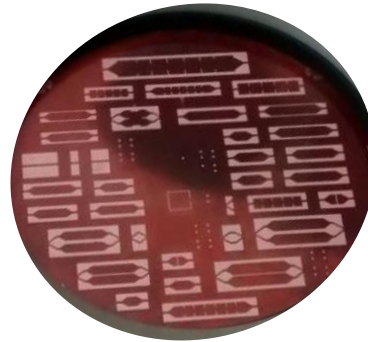
Other electrodeposition solutions for the nanowire growth were analyzed, with a solution that uses a periodic pulse reverse (PPR) biasing appearing to be the best option. The PPR bias leads to a better copper ions distribution over the sample and to a uniform copper growth. The solution “Macuspec PPR 100,” proposed by the company MacDermid was chosen.

Figure 9 – Example of periodic pulse reverse (PPR) current signal used for biasing the electrodeposition solution for nanowire growth on the membrane.



With all of these optimizations, selective copper nanowire growth was made possible. Figure 10 shows how a good nanowire growth is expected to look after the electrodeposition process, in contrast with Figure 6 before process optimization. In Figure 10, the orange regions are regions with copper grown after the growth surpassed the nanopores, the red region is a photoresist layer on top of a SiO_2 mask, serving as an additional protection layer to the mask.

Figure 10 – Nanowire growth after all optimizations. In red the photoresist additional layer on top of the SiO₂ mask, and in orange the excess copper after the nanowires growth in the delimited regions.



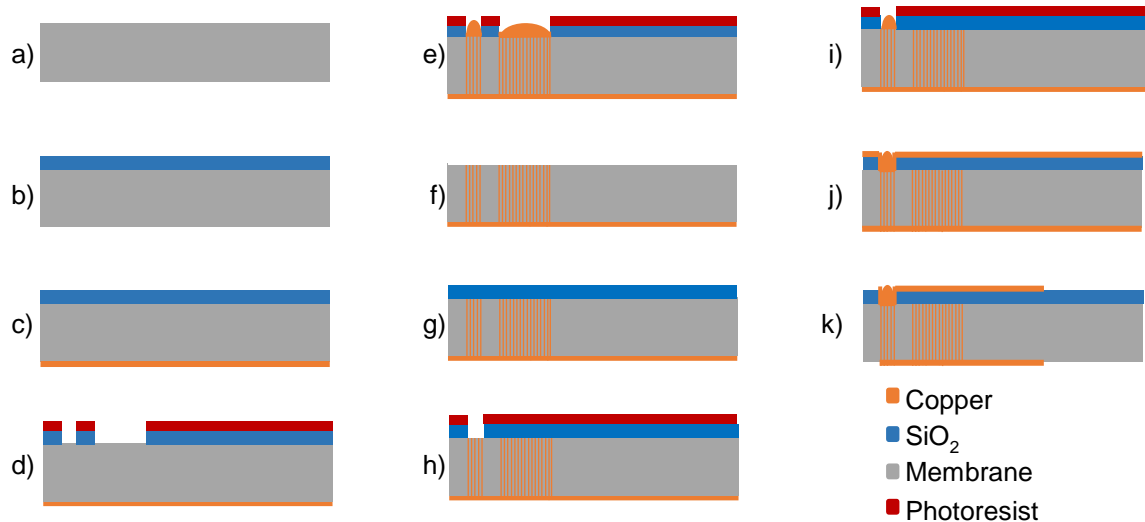
Following with the fabrication process optimization, a polishing machine (Tegramin-25 from Struers) is now employed for removing the excess copper after the nanowire growth, instead of breaking a small edge of the membrane and removing it mechanically with help of a tweezer as in the step 5 from Table 1. This technique permits to remove the natural roughness of the membrane, resulting in lower signal losses in designed circuits.

The definition of structures on the copper layer is done using a corrosion method. First, the copper was grown to the final thickness and then etched. The current density of the growth was not well controlled, leading to a thickness difference between the border and the center of the membrane. A DC and PPR electroplating solution from MacDermid were explored and a better current density control was performed, resulting in either solutions being acceptable. For convenience, the PPR solution is used as it is the same for growing nanowires. The wet etching used before was a chromium etching solution, not specific to copper, leading often to roughness on the structures edge. An etching solution specific to copper from AlfaCleaner is now employed, with a characterized typical 5 μm overetching. Masks for the structures using this corrosion method includes 5 μm more on each structure side to overcome the overetching, leading to a minimal strip width of 15 μm .

The optimizations described until now made the fabrication process more reliable. The yield of success for nanowire-vias fabrication was increased. Membranes with different pores sizes can now be used, such as 80-nm and 160-nm. Nevertheless, membranes with around 55-nm pore diameter present the best yield for nanowire

growth. Figure 11 shows the general fabrication process after all proposed optimizations. This general process is adapted to each membrane fabrication, as steps can be added or removed, as they are needed.

Figure 11 – Optimized fabrication process employed for fabricating circuits on the membrane as nanowire-vias and circuits with slow-wave transmission lines. This general process is adapted to each fabrication.



The general fabrication process can be described by the steps below.

- a) A membrane chosen in height and pore dimension, always 1-inch-diameter wafers, and cleaning 10 minutes in boiling trichloroethylene, followed by acetone and isopropyl alcohol;
- b) SiO₂ mask deposition by RF sputtering (about 330 nm): 2 mTorr, Ar 70 sccm, O₂ 30 sccm and plasma power of 150 W, with deposition rate of 16 nm/min;
- c) M1 copper deposition, first a Ti seed deposition for adherence using RF sputtering: 2 mTorr, Ar 10 sccm, 100 W, 20s is done, followed by copper seed deposition using RF Sputtering: 2 mTorr, Ar 10 sccm, 70 W, 10 minutes. The copper seed layer is then thickened using the “Macuspec PPR 100” electrodeposition solution with 25 mA DC current (about 490 mA/dm²), 20 min giving 2 μ m copper thickness;
- d) Photoresist is coated and exposed/developed. The SiO₂ mask layer is opened in a BOE (1 part HF 49% in water, 6 parts NH₄F 40% in water) solution for about 4 minutes;

- e) Nanowires (VIA-NW) are grown in the “Macuspec PPR 100” solution, using a periodic pulsed current with 20 ms positive current and 1 ms negative current. The positive current density is about 300 to 700 mA/dm² adapted to each mask used. The negative current density is about 3 to 4 times the positive current. The photoresist is left as an additional protection layer to the SiO₂ mask, for the nanowire growth;
- f) The photoresist is removed on acetone, followed by acetic acid. The membrane is then polished to remove the excess copper, and then fine polished to remove the roughness. The membrane is cleaned for 10 minutes in deionized water;
- g) SiO₂ deposition for slow-wave transmission lines as in item b). The deposition time depends on the desired thickness, usually 1 μ m, with successive 10-minutes spaced depositions to not raise the substrate temperature;
- h) Photoresist is coated and exposed/developed for masking the SiO₂. The oxide is opened using BOE, to expose the nanowire-vias region. The corrosion time depends on its thickness, and is estimated by SiO₂ deposited on the same run in silicon samples. The photoresist is left as an additional protection layer for the next step. Mask alignment is performed with alignment structures;
- i) Copper is electrodeposited to create an electrical contact between the nanowire-vias and the top copper layer (VIAM layer);
- j) The photoresist is removed and seed copper for layer M2 is deposited and thickened as in step c), for the top surface;
- k) The strips in layers M1 and M2 are defined in this step using a photoresist mask and etch using the solution “SuperEtch” from the “Alfacleaner” company for 30 s at 35°C. Over-etching is about 5 μ m. Afterwards the titanium is removed using a 20:1 water HF solution for 20 s.

1.3 Membrane characterization

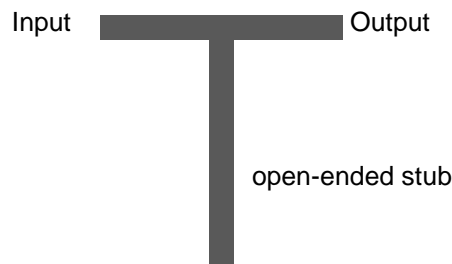
Electrical characterization of the membrane without nanowires, i.e. with the nanopores “filled” with air, is necessary to the design of passive devices on the membrane, such as microstrip lines, coplanar waveguides (CPWs), cross-overs,

among others. From the electrical characterization is extracted the relative dielectric constant ε_r and dielectric losses, represented by the loss tangent $\tan \delta$, of the substrate. First, an electrical characterization using microstrip open stubs is performed. A second characterization is done using a filter composed of microstrip lines with short-ended microstrip stubs also, as filter behavior is highly dependent on the substrate characteristics. Since the membrane presents vertical pores, it is “tough” that it has some anisotropy, i.e., the vertical ε_r is different from the horizontal one. The two characterization methods employing microstrip lines having a mainly vertical electrical field, they give us mainly the vertical ε_r .

1.3.1 Electrical characterization using open-ended stub

Quarter wavelength ($\lambda/4$) open-ended stubs in microstrip technology was first proposed in [13] for substrate electrical characterization, where the stubs form a “T” with a thru-line, as shown in Figure 12. This “T-pattern” gives a simple resonant structure. From its resonant frequency and 3-dB bandwidth, the electrical characteristics of the substrate can be extracted. In [13] equations are used to extract the relative dielectric constant ε_r of the substrate and losses represented by $\tan \delta$.

Figure 12 – “T” open-ended stubs topology used for electrical characterization.



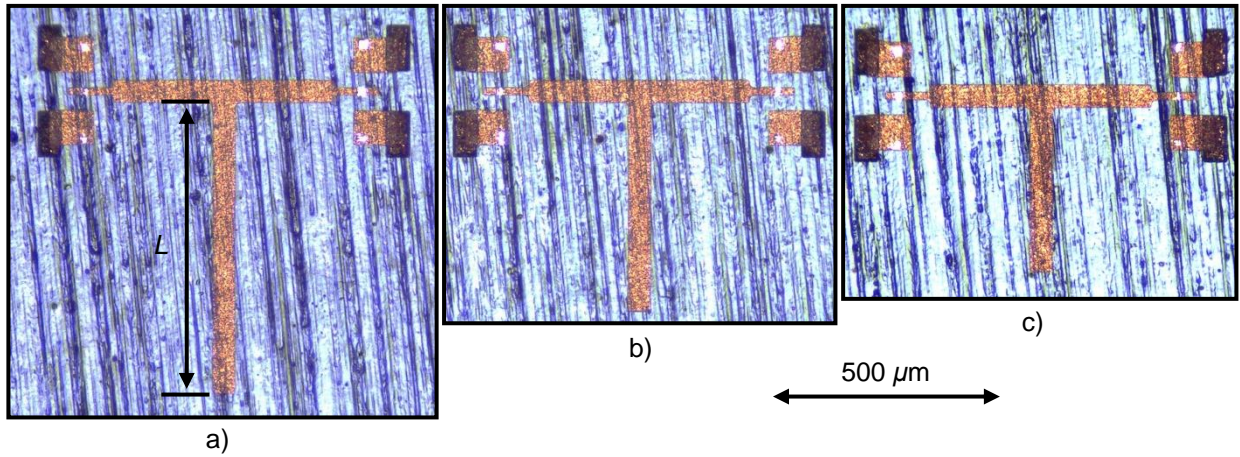
In this section, the same method is employed for the membrane characterization, and the results are compared with simulations done in the 2.5-D electromagnetic (EM) simulator from Keysight ADS/Momentum.

50- μm -thick anodic aluminum oxide (AAO) membranes from Synkera are employed in this characterization, having 55-nm pore diameter and interpore distance of 143 nm. Those have initially shown the best results for nanowires growth, and are employed for many of the circuits developed in this work. As Synkera stopped

fabricating AAO membranes, during the course of this work, the provider was changed to InRedox, with the InRedox membranes having similar electric characteristics.

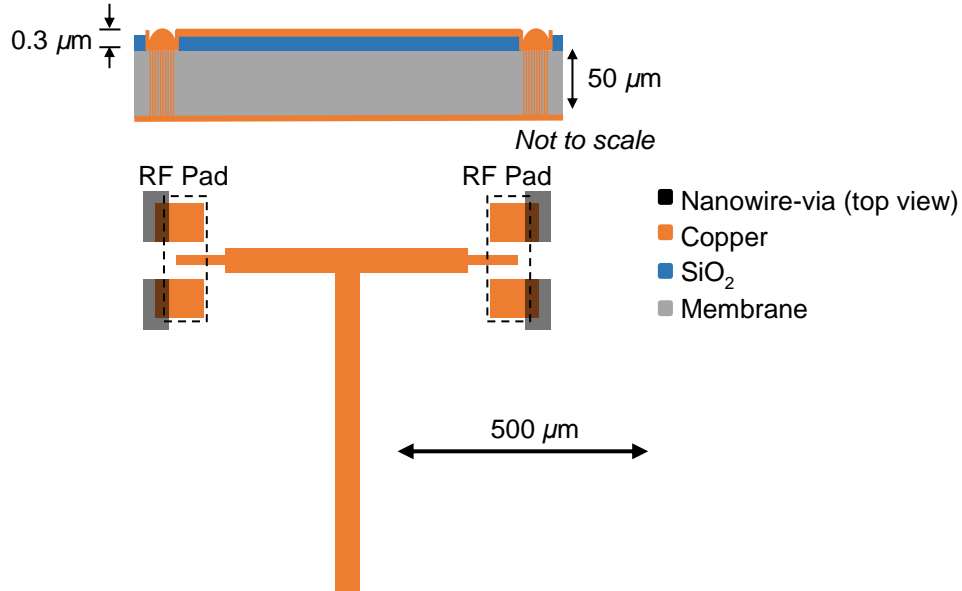
Five microstrip lines with $\lambda/4$ open stubs were fabricated, measured and analyzed. Each fabricated microstrip open-ended stub has a different length, so that the structures resonate at different frequencies. The fabricated lengths L were $640\text{ }\mu\text{m}$, $530\text{ }\mu\text{m}$, $459\text{ }\mu\text{m}$, $406\text{ }\mu\text{m}$ and $360\text{ }\mu\text{m}$, respectively. Some fabricated structures are shown in Figure 13.

Figure 13 – Microstrip lines with open stubs fabricated for electrical characterization. In a) structure with a $640\text{ }\mu\text{m}$ long stub, in b) with $459\text{ }\mu\text{m}$ and in c) $360\text{ }\mu\text{m}$. In orange the microstrip lines and in light blue the membrane. The blue color is due the SiO_2 layer.



The structures features a $0.3\text{-}\mu\text{m}$ -thick SiO_2 layer between the membrane and the top metallization, used to mask the nanopores and allow the growth of nanowires only for the resistive probe contact pads to the lower ground plane. As this layer is very thin, it does not interfere with the overall electrical characterization. The transversal section of the structures can be seen in Figure 14 a). The fabricated structures were measured with the help of a microscope and the layout reproduced in the ADS/Momentum EM simulator. In Figure 14 b), we have the layout for a structure with $640\text{ }\mu\text{m}$ long stub reproduced.

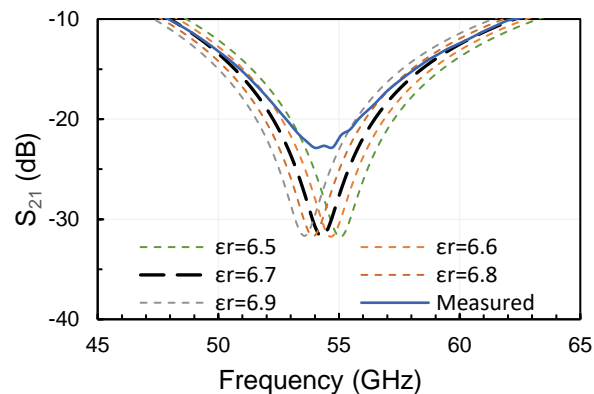
Figure 14 – In a) the transversal section of the open-ended microstrip stubs and in b) layout of microstrip line with 640 μm long stub. All structures were measured and the corresponding layout reproduced.



In the ADS/Momentum software, the membrane's parameters ϵ_r and $\tan \delta$ were set as variables, for fitting between measured and simulated S-parameters.

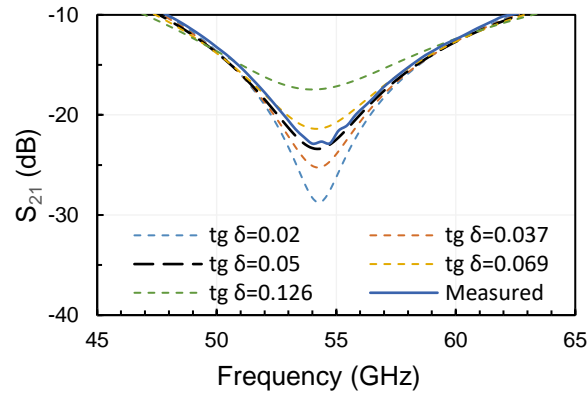
Using a co-simulation between the ADS/Schematics electrical simulator and Momentum simulator, the membrane's parameters were varied. In a first step, $\tan \delta$ was set fixed and equal to 0.01 at 60 GHz and ϵ_r was varied. In Figure 15 it is shown the measured S_{21} for the structure with 640- μm long stub that resonates at 54.4 GHz and simulations for this structure varying ϵ_r . From the same Figure 15 it can be seen that with $\epsilon_r = 6.7$ the simulated resonance frequency agrees well with the measured one.

Figure 15 – Membrane simulation ϵ_r variation and measurement with stub resonating at 54.4 GHz. Co-simulated with ADS/Momentum and ADS/Schematics. Looking at the results $\epsilon_r = 6.7$ better agrees with the measurement.



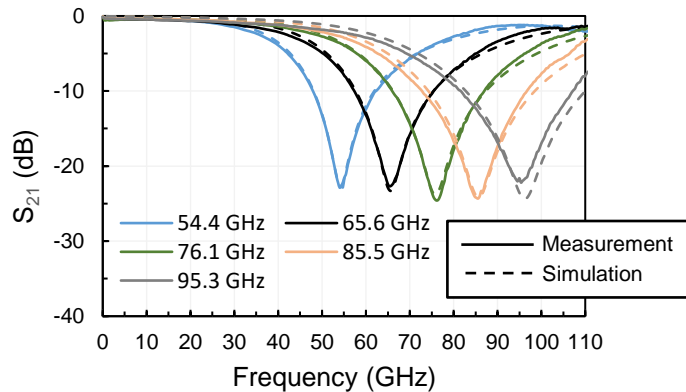
Fixing $\varepsilon_r = 6.7$, $\tan \delta$ is then varied in the same manner, with results shown in Figure 16. $\tan \delta = 0.05$ at 60 GHz leads to a good agreement between measurement and simulation results.

Figure 16 – Variation of $\tan \delta$ at 60 GHz for $\varepsilon_r = 6.7$ in comparison with the measured structure with resonance at 54.4 GHz.



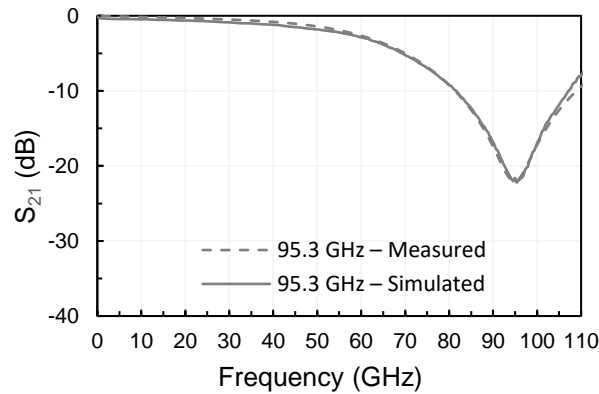
To verify that the extracted parameters $\varepsilon_r = 6.7$ and $\tan \delta = 0.05$ at 60 GHz are consistent in frequency, all other microstrip structures with open stubs were simulated using those values with Momentum. In Figure 17 it can be seen the measured and simulated S_{21} for all structures. The structures with stubs length $640 \mu\text{m}$, $530 \mu\text{m}$, $459 \mu\text{m}$, $406 \mu\text{m}$ and $360 \mu\text{m}$ resonate at 54.4 GHz, 65.6 GHz, 76.1 GHz, 85.5 GHz and 95.3 GHz respectively. Up to 85.5 GHz, the agreement between simulation and measurement results is good. At higher frequency, with the structure that resonates at 95.3 GHz, a deviation between simulation and measurement results occurs.

Figure 17 – Measured and simulated S_{21} results for all microstrip structures with open stubs using extracted parameters $\varepsilon_r = 6.7$ and $\tan \delta = 0.05$ at 60 GHz. Solid lines are measured results and dashed lines are simulated one.



For the structure that resonates at 95.3 GHz, the same procedure as before was employed to find the ε_r and $\tan \delta$. It was found that $\varepsilon_r = 7$ and $\tan \delta = 0.07$, as show in Figure 18.

Figure 18 – Measured and simulated S_{21} results for structure resonating at 95.3 GHz using extracted parameters $\varepsilon_r = 7$ and $\tan \delta = 0.07$.



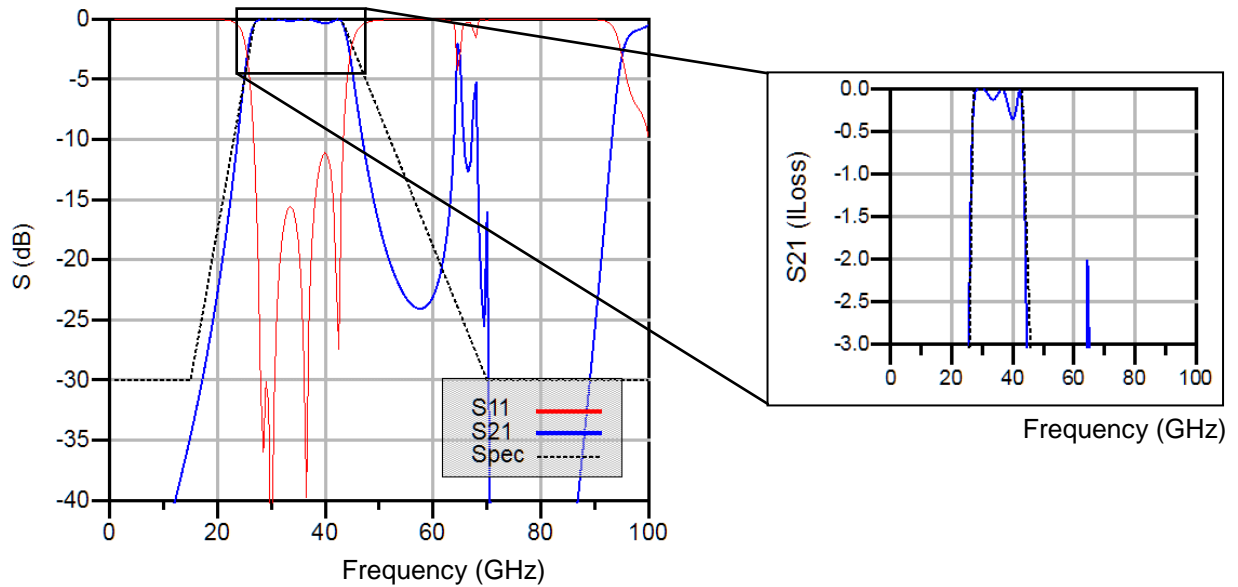
From the simulations, we can see that up to 85.5 GHz, the electrical characteristics of the porous membrane without nanowires dos not change; it is $\varepsilon_r = 6.7$ and $\tan \delta = 0.05$, whereas at 95.3 GHz this value changes to $\varepsilon_r = 7$ and $\tan \delta = 0.07$. This means that the electrical characteristics of the combination of nanopores filled with air and alumina from the membrane may change at frequencies above 80 GHz. However, only one point was measured above 80 GHz. Hence, for applications clearly beyond 100 GHz, complementary characterization in this frequency range may be necessary.

1.3.2 Electrical characterization using a filter

The filter proposed in this section was designed to be a band-pass filter in K_a band, from 27 GHz to 40 GHz, and rejection band with attenuation higher than 30 dB below 15 GHz and above 70 GHz. The filter was designed on ADS/Schematics. Initially an ideal filter was simulated with the Design Assistance tool. Afterwards, with the same specification, the *DA_SBFILTER* smart component was used to implement the filter in microstrip technology, with short-ended stubs making use of nanowire-vias. The filter was simulated using a 50- μm -thick membrane with 55-nm nanopores diameter and 143-nm spacing between pores. The dielectric constant of 7.6 for the membrane without nanowires was employed. It is slightly different from the value extracted in section 1.3.1, these works being carried out in parallel, and 7.6 being the first

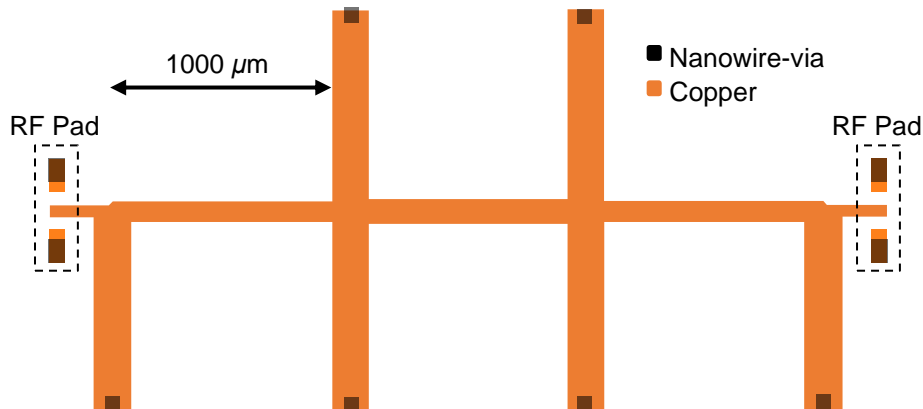
approximation used of the nanoporous membrane dielectric constant. In Figure 19 it is shown the ideal filter simulated using the Design Assistance tool. It can be seen that spurious resonances appear between 60 GHz and 70 GHz, within the rejection band. The return loss is also quite poor in the passband. This is not really an issue since the filter was designed only for characterization purposes.

Figure 19 – Simulated ideal S-parameters from the proposed K_a band pass filter and a highlight of the pass band.



The filter layout was generated using the *DA_SBFILTER* smart component. Pads were added for measurement and vias to short-circuit the stubs. The layout used for fabrication is shown in Figure 20.

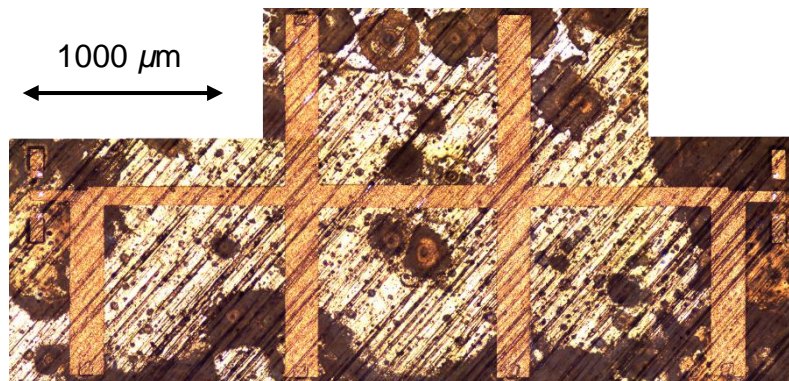
Figure 20 – Layout of the designed microstrip band-pass filter on the membrane with short-circuited stubs.



Several photos of the realized filter were taken using a microscope and the complete reconstructed photography is shown in Figure 21. The membrane surface

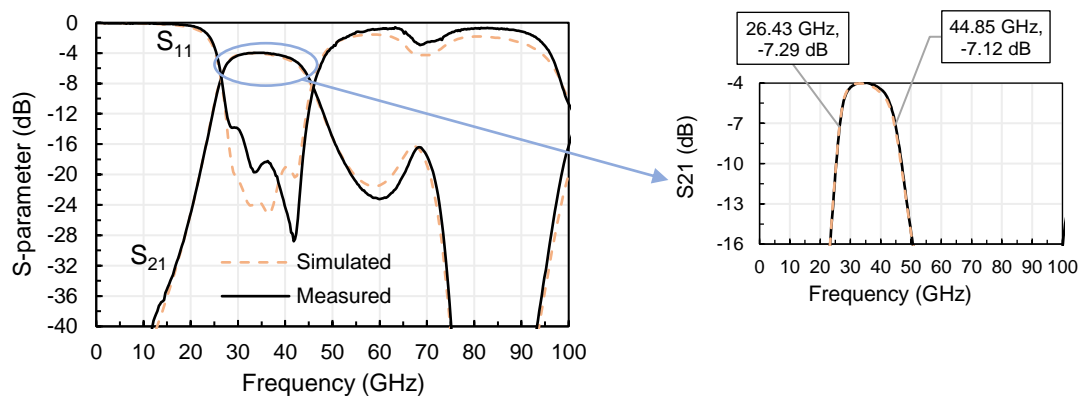
roughness can be seen as diagonal lines, and since the membrane is translucent, the bottom ground plane can also be seen. In this fabrication, some parts of the ground plane had more adhesion to the membrane than others. On the parts of the figure where the ground plane is bright there was a good adhesion between the copper and the membrane.

Figure 21 – Fabricated band-pass filter.



The filter actual physical dimensions were measured using a microscope, and the filter was simulated with the measured dimensions with ADS/Momentum. The membrane's relative dielectric constant ϵ_r and loss tangent $\tan \delta$ were varied to obtain a good agreement between simulation and measurement results. Measured and simulated S-parameters are shown in Figure 22. From the measurement results, the filter presents a 3-dB pass-band from 26.43 GHz to 44.85 GHz, slightly higher than the K_a band (27 GHz to 44 GHz). The insertion loss in the pass band is higher than 4 dB. The simulation shown in Figure 22 was carried out after fitting measurement and simulation results with $\epsilon_r = 7.1$ and $\tan \delta = 0.07$.

Figure 22 – Measured and simulated S-parameters for the microstrip band-pass filter with short-circuited stubs. Highlighted the pass-band, from 26.43 GHz to 44.85 GHz, with insertion loss higher than 4 dB.



1.3.3 Summary of membrane characterization

It was shown the electrical characterization of AAO membranes from Synkera, with 55-nm pore diameter and 143-nm interpore distance, using microstrip lines with open-ended stubs and using a microstrip filter. From the open-ended stubs, it was found that $\varepsilon_r = 6.7$ and $\tan \delta = 0.05$ extracted at 60 GHz is a good value up to at least 85.5 GHz. Above this frequency, the characteristics seem to change, and for a stub operating at 95.3 GHz the values of $\varepsilon_r = 7$ and $\tan \delta = 0.07$ were found. From the filter, the found electrical characteristics were $\varepsilon_r = 7.1$ and $\tan \delta = 0.07$. The different values found using the microstrip filter ($\varepsilon_r = 7.1$ and $\tan \delta = 0.07$) as compared to the open-ended stubs over the same frequency range ($\varepsilon_r = 6.7$ and $\tan \delta = 0.05$) can be due to process variations between the membrane's fabrication. It can also be noted that the filter fabrication process did not have the best result, having the copper metal at the bottom not properly adhering to the membrane, in this way probably leading to higher losses. The electrical values extracted from the open-ended stubs method were considered as more reliable for those reasons. As will be shown through the results presented in this work, they also agree with other fabricated passive structures on the membrane. It should also be noted that the extracted ε_r from both methods is different from pure alumina (ε_r in between 9.6 and 10), because of the influence of the air-filled nanopores.

This extraction was made using microstrip structures, so the electrical field is mainly oriented vertically in the membrane. If the electrical field is horizontal, as in coplanar waveguides (CPW), the dielectric constant may be different because of the vertical orientation of the air-filled nanopores. The dielectric loss represented by $\tan \delta$ that was found is at least two orders of magnitude higher than the expected one for pure alumina. These higher losses are probably related to the formation process of the membrane, as it might happen that not all aluminum was anodized into alumina. Another manufacturer, InRedox, explains that if the fabricated membranes have an additional thermal treatment, the dielectric losses may be decreased.

1.4 Summary

This chapter presented the MnM technology, its fabrication process and its high frequency electrical characterization.

The fabrication process was optimized during this work. With the optimization, it is now possible to have a range of different circuits with different layouts on the same membrane, especially circuits using TSVs alongside circuits using slow-wave microstrips, as will be shown in the next chapters. In addition, the fabrication process is now more reliable, with a higher yield of structures in each fabrication.

The electrical characteristics of the MnM membrane without nanowires were extracted from two methods, using open-ended microstrip stubs and a microstrip based short-ended stubs filter. With this characterization, the membrane presents a relative dielectric constant $\varepsilon_r = 6.7$ and loss tangent $\tan \delta = 0.05$, up to at least 85 GHz.

In chapter 1, now that the fabrication process optimization made its fabrication possible, nanowire-vias are explored. Transitions and a 3-D solenoid inductor employing nanowire-vias as TSVs are presented, fabricated, measured and analyzed. In chapter 3, new slow-wave transmission lines fabricated after the fabrication process optimization are analyzed and a linear model is presented.

2 VIAS ON THE MNM SUBSTRATE

2.1 Introduction

High quality through-substrate-vias (TSVs) are fundamental for an mm-wave interposer. They act as a routing structure connecting the top and bottom parts of an interposer, enabling all sorts of passive circuits and complex structures to be fabricated. A good interposer should have TSVs with high performance, to assure good signal integrity and low attenuation, and with a small footprint, to have high-density interconnections.

In the literature, TSVs in interposers appear in silicon with limited performance because of the conductivity of the silicon ($1\text{-}20\ \Omega\ \text{cm}$), achieving 0.28 dB of loss at 60 GHz for one transition [14]. Vias in high resistivity silicon (HR-Si) present better performance because of the higher resistivity of the substrate, although this solution comes with increased costs. Via transitions in glass have been demonstrated with similar performance, e.g., 0.34 dB of loss per transition at 50 GHz [15]. In Liquid Crystal Polymer (LCP) technology, a loss of 1 dB per transition at 110 GHz was achieved [4].

In the mentioned technologies, the fabrication of vias involves special processes in order to “drill” the substrate. In Si and HR-Si, deep reactive-ion etching (DRIE) process is the main technique used for via etching. For filling the via, several processes can be used, such as electroplating copper from one side to another, depositing copper, tungsten, or nickel on its side, applying conductive paste or introducing wires magnetically [3]. In addition, a barrier layer is needed between the via and the substrate (Si or HR-Si), usually a layer of silicon dioxide is used [16]. When the DRIE process cannot etch the via up to the other side due to the aspect ratio limits, a final step of substrate thinning is needed in order to open the vias. This increases the fabrication cost, complexity and fabrication time. With this fabrication process, small vias with $3\text{-}\mu\text{m}$ diameter have been reported on a $50\text{-}\mu\text{m}$ -thick substrate, using an optimized process [17].

In glass interposers, to drill the vias, several fabrication processes have been investigated, such as DRIE, photochemical etching, sandblasting, electrical discharge and laser techniques. The laser techniques produce tapered vias with different

entrance/exit diameters, such as $15/8\ \mu\text{m}$ in a $30\text{-}\mu\text{m}$ -thick substrate [18]. In LCP technology, via drilling is done mainly with excimer laser, achieving larger tapered vias with $40/20\ \mu\text{m}$ of entrance/exit diameters [19]. It can also be done by mechanically punching the substrate, achieving large vias with $50\ \mu\text{m}$ diameter [20]. The drawbacks of tapered vias formed by laser techniques are that the tapering increases via resistance and inductance, and that small diameter vias and via spacing are difficult to achieve. For filling the vias in both substrates, electroplated or deposited copper are usually employed.

Si and HR-Si modeling [21], [22] for via transitions is more complex than using good dielectrics, such as glass [23] and LCP, because it must take into account a barrier layer capacitance and the substrate loss.

Usually the reported results of transitions using TSVs in the literature show measurements at low frequencies, below 20 GHz [5], [18], [23], [24]. At higher frequencies, in the mm-waves realm, very few TSVs transitions results have been published due to the difficulty of fabrication, the large size, the high cost and the low performance. To overcome those problems a novel type of via is proposed: nanowire-vias on the MnM interposer. Using nanowires for the vias instead of opening the substrate for a “solid” via has the advantage of being low-cost, easier and simpler to fabricate still leading to reduced via dimensions, limited by the photolithography, with performance and yet, easily scalable for consumer market.

First, the performance of the nanowire-vias is accessed up to 110 GHz with CPW transmission line (Tlines) transitions. A model for a single transition is proposed and it is estimated its performance and compare to the results presented on the literature at section 2.2. Inductors using nanowire-vias, as a device on the MnM interposer using the vias capabilities, are designed, fabricated, measured and modelled at section 2.3. The chapter is concluded with a summary in section 2.4.

2.2 Nanowire-vias Transitions

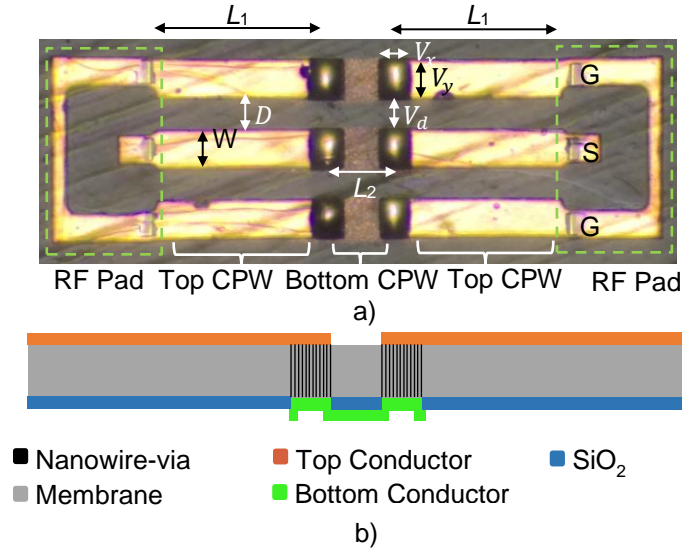
Nanowire-vias were developed on the MnM substrate as they are easier to fabricate than a solid via, with no need to drill the substrate since it is already porous

and the nanowire growth is straightforward. The nanowire-vias achieving smaller dimensions than solid vias, they open the possibility to develop high-density interconnections on the MnM substrate. This easy of fabrication reflects in this type of via being low-cost, as simple additional steps are needed.

To access the nanowire-vias performance in mm-wave frequencies, nanowire-vias transitions were designed, fabricated, measured and analyzed. Coplanar waveguides (CPW) lines were used as access lines for the vias, as it is a transmission line that is defined only in one face of the substrate that can be easily changed from one face to another, being easier than microstrips for example. Although the nanowire-vias are easy to fabricate, a full 3-D electromagnetic simulation is not straightforward, because of the high aspect ratio of each nanowire (diameter of 55 nm and length of 50 μm) and the high nanowires density in the substrate, leading to high computational cost and time. An advanced electrical model was developed, accurately predicting the via insertion and return loss. The structures are described here. Section 2.2.1 describes the fabrication process, while the measurement setup and the measurement results are described in section 2.2.2. The proposed electrical model is described in section 2.2.3, for the CPW feeding lines and the nanowire-vias. This model is then used to extract the nanowire-via transition performance, which is compared to the results presented in the literature. This section is then concluded with a summary in Section 2.2.5.

The proposed structure uses ground-signal-ground (GSG) pads for the coplanar waveguide (CPW) feeding lines, and nanowire-vias transitions, as shown in Figure 23. A transition is composed of three nanowire-vias (for G, S and G, respectively) interconnecting the top and bottom CPW feeding lines. The fabricated structure (Figure 23 a) is built on top of a 50- μm -thick anodic aluminium oxide (AAO) porous membrane with 55-nm-diameter nanopores and approximately 57 nanowires/ μm^2 . CPWs were chosen as it simplifies the measurement using GSG probes. A thin silicon dioxide (SiO_2) layer (1- μm -thick) was used as mask for the nanowires' growth. From bottom to top, the structure has four layers consisting in a bottom copper layer, a SiO_2 mask layer, the alumina membrane filled with nanowires at the vias regions and a top copper layer. The top and the bottom copper layers define the top and the bottom CPWs, respectively. The copper thickness is 1.5 μm .

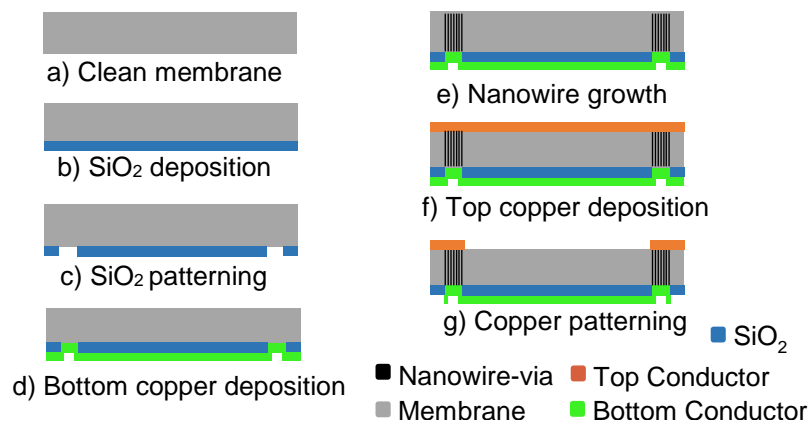
Figure 23 – Fabricated CPW structure layout for the nanowire-via characterization. a) Top view (photo) and b) Lateral view (illustration). V_x and V_y are the via dimensions and V_d is the distance between vias edge. All strips (top and bottom) are $54\text{-}\mu\text{m}$ -large (W) spaced by $36\text{ }\mu\text{m}$ (D). The access feeding Tlines have variable length L_1 , and L_2 is the bottom CPW length, respectively.



2.2.1 Fabrication Process

Several rectangular shaped vias with different dimensions, from $20\text{ }\mu\text{m}$ to $50\text{ }\mu\text{m}$, were fabricated with the same feeding Tlines. The fabrication process of the nanowire-vias is described in Figure 24. This fabrication process at the time of fabrication was not optimized as the proposed general fabrication process in Figure 11 from chapter 1.

Figure 24 – Steps of the nanowire-vias fabrication process.



The steps for the fabrication process are:

- Initially, the membrane is cleaned in boiling acetone and isopropanol, 10 min in each solution;

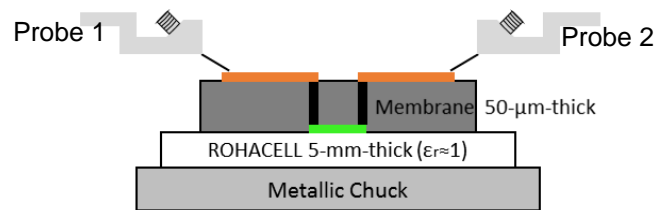
- b) A 1- μm silicon dioxide mask-layer (SiO_2) is deposited via reactive magnetron Sputtering;
- c) The SiO_2 layer is patterned by photolithography and etched by BOE (buffered oxide etch);
- d) A titanium followed by a copper seed layer is deposited by sputtering and thickened by electrodeposition in a cupric sulfate solution from EPI with $1\text{A}/\text{dm}^2$ for 12 min;
- e) Nanowires are grown by electrodeposition in the same solution;
- f) A new titanium and copper layer is deposited on the top of the membrane by sputtering, and then thickened with the same parameters as in d);
- g) The copper layers are patterned with photolithography and etched by a solution of ceric ammonium nitrate and acetic acid, forming the upper and lower CPWs

2.2.2 Characterization up to 110 GHz

The total structure (feeding Tlines + vias + bottom CPW) was characterized using GSG probes (MPI Titan probes with $100\text{-}\mu\text{m}$ -pitch) in a 300 mm semi-automatic probe station connected to an Anritsu Panorama ME7808C vector network analyzer (VNA). A line-reflect-reflect-match (LRRM) calibration was used.

To avoid shorting the bottom CPW with the metallic chuck of the probing station, a 5-mm thick ROHACELL 51 IG foam was used as a spacer between the structures and the metallic chuck, as shown in Figure 25. This foam has $\epsilon_r = 1.05$ and $\tan \delta = 0.0135$ at 26.5 GHz.

Figure 25 – Lateral schematic representation of the measurement setup using ROHACELL foam.



Five different sizes of vias were fabricated in structures with the dimensions shown in Figure 23 and different feeding Tlines lengths L_1 , as given in Table 2. The

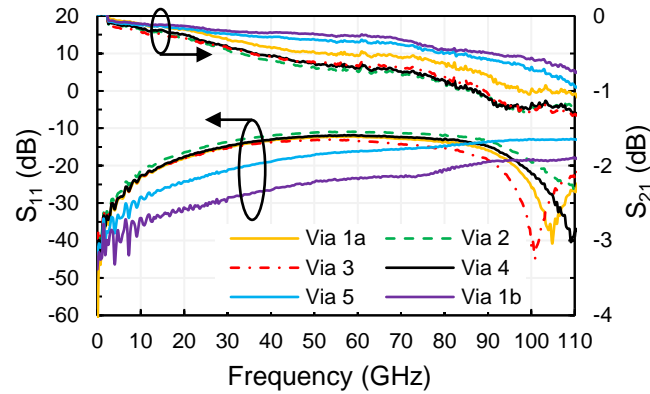
sum $V_y + V_d$ is kept constant, so the each via is centralized in the x axis of the signal and ground Tlines.

Table 2 – CPW and vias dimensions in μm .

	V_x	V_y	V_d	L_1	L_2
Via 1a	50	32	59	250	100
Via 2	45	20	71	250	100
Via 3	20	45	46	250	100
Via 4	20	30	61	250	100
Via 5	30	20	71	50	100
Via 1b	50	32	59	50	100

Figure 26 shows the measured S-parameters of the structures presented in Table 2 up to 110 GHz. Although the results are not de-embedded, a low insertion loss of the whole structure (pads + feeding Tlines + 2 via transitions) can be observed, with a worst case of 1.2 dB at 110 GHz.

Figure 26 – Measured S-parameters of the different structures with dimensions given in Table 2.

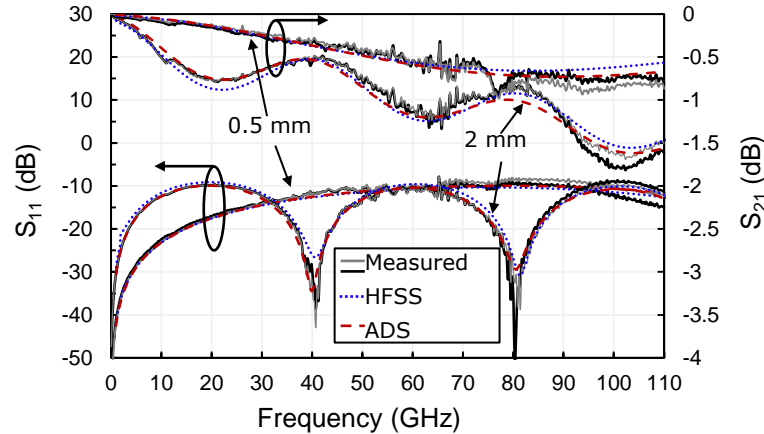


In order to verify the nanowire-via transition performance, the loss in only one transition excluding pads, feeding Tlines, and bottom Tline was assessed through a comparison between simulations and measurements. The simulations were performed combining EM simulations and an electric model for the vias. The simulations, modelling, and results are presented and discussed in the next section.

2.2.3 Electrical Model

The modelling of the whole structure was divided in two parts: CPWs and nanowire-vias. First, simple CPWs with 2 mm, 1 mm and 0.5 mm in length (two of each) with the same pads and strips dimensions (W and D) as the CPWs used in the structures with nanowire-via transitions in Figure 23 were simulated in Ansys HFSS 16 software, fabricated on the porous alumina membrane, and measured. The full 3-D EM simulation agrees well with measurements as well as the lossy transmission line model from Keysight ADS, as shown in Figure 27. In this figure, only two sets of transmission lines (2 mm and 0.5 mm) are shown for clarity. The ADS model, in agreement with HFSS, uses a transmission line with characteristic impedance of $70\ \Omega$, effective dielectric constant of 3.55, conductor loss of 45 dB/m at 60 GHz and $\tan \delta$ of 0.03. The ADS model was used to de-embed the nanowire-via structure for its simplicity and simulation speed.

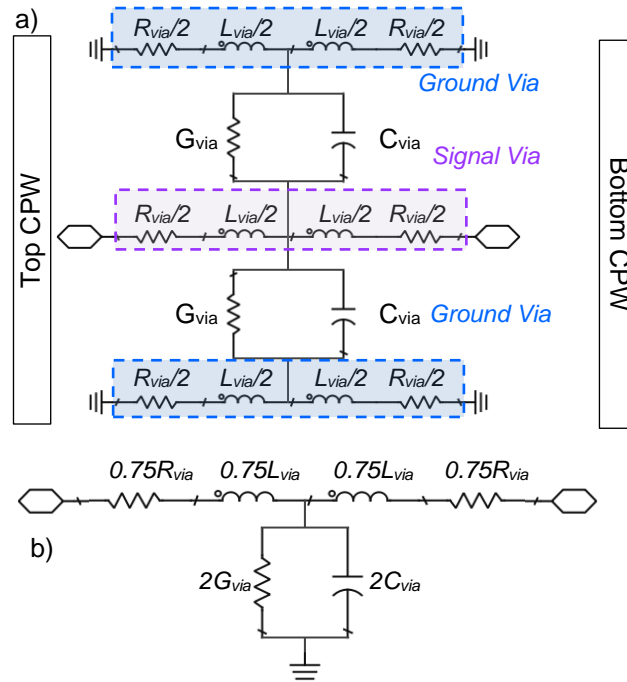
Figure 27 – Measured results of the 2-mm-long and 500- μ m-long CPWs compared to the simulated results from ADS and HFSS.



Once the CPW behavior is well modeled, the CPW feeding lines and the bottom CPWs were simulated with the lumped elements model for the vias to reconstruct the whole structure shown in Figure 23. These simulations were compared to the measurements, allowing to extract the vias loss from the model.

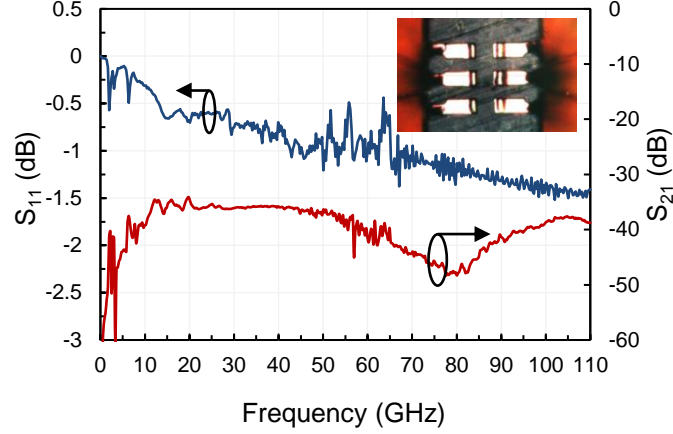
The complete electrical model for the nanowire-via transition can be seen in Figure 28 a). This model has a capacitance C_{via} and conductance G_{via} between vias, each via with a series resistance R_{via} and inductance L_{via} . This physical model was reduced to an equivalent more compact “T” model presented in Figure 28 b).

Figure 28 – a) Physical model for the transition with GSG vias, and b) Equivalent compact “T” model.



The model from Figure 28 does not take into account the direct coupling between two via transitions. This coupling was analyzed using the same structure as the one described in Figure 23, but without the bottom CPW (replaced by an open circuit). Several structures with different dimensions were measured. The measurement result of the structure with the same dimensions as Via 1b with a separation of $57\ \mu\text{m}$ between the two nanowire-via transitions (wall-to-wall distance in L2 direction in Figure 23) is given in Figure 29. The transmission parameter S_{21} shows an isolation better than 30 dB up to 110 GHz and a return loss higher than 1.5 dB, as expected from a lossy open-circuited device. Since the measurements of the whole structure with the bottom CPW, shown in Figure 26, presents a good signal transmission with low insertion loss limited to less than 1.5 dB at 110 GHz, this parasitic direct coupling between the two transitions was neglected in the model.

Figure 29 – Measurement of the direct coupling between via transition spaced of $57\ \mu\text{m}$ in a structure without the bottom CPW (replaced by an open circuit) with the same dimensions as Via 1b. The inset shows the structure during measurement.



Numeric values for the model components R_{via} , L_{via} , G_{via} , C_{via} (Figure 28) were calculated. For the inductance L_{via} , two approaches were performed to obtain its value, one analytical and the other more complete taking into account all nanowires, in a matrix approach. The comparison between the two approaches was not performed and is interesting to be done, nevertheless, the analytical approach was preferred for its simplicity.

2.2.3.1 Analytical Inductance calculation

The value of L_{via} was calculated from the inductance formula given by [25], which gives the inductance of a single via. In the case of the via on the transitions, the cross-section of the entire via was used and since the vias are not circular, an equivalent radius was found and used for eq. (1). It was necessary to modify the empirical factor proposed by [25] and presented in eq. (1) from $3/2$ to 0.3 for our case, following several magnetostatic simulations.

$$L_{via} = \frac{\mu_0}{2\pi} \left[h \cdot \ln \left(\frac{h + \sqrt{r^2 + h^2}}{r} \right) + 0.3 \left(r - \sqrt{r^2 + h^2} \right) \right] \quad (1)$$

with h the via height and r its radius.

2.2.3.2 Inductance and resistance calculation in a matrix format

To calculate the equivalent inductance and resistance of a nanowire-via in frequency, and more generally, a region with nanowires, an inductance matrix (symmetrical \mathbf{L} matrix) can be used, in conjunction with a resistance matrix (diagonal \mathbf{R} matrix). Those matrixes relate the currents and voltages of each nanowire. Using as example a region with 4 nanowires, the system can be defined as ([27], chapter 6.5):

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \left(\begin{bmatrix} R_{nw} & 0 & 0 & 0 \\ 0 & R_{nw} & 0 & 0 \\ 0 & 0 & R_{nw} & 0 \\ 0 & 0 & 0 & R_{nw} \end{bmatrix} + s \begin{bmatrix} L_{self} & M_{12} & M_{13} & M_{14} \\ M_{12} & L_{self} & M_{23} & M_{24} \\ M_{13} & M_{23} & L_{self} & M_{34} \\ M_{14} & M_{24} & M_{34} & L_{self} \end{bmatrix} \right) \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}, \text{ or}$$

$$\mathbf{V} = (\mathbf{R} + s\mathbf{L}) * \mathbf{I} = \mathbf{Z} * \mathbf{I} \quad (2)$$

where \mathbf{R} is a diagonal matrix with each nanowire DC resistance R_{nw} , \mathbf{L} is an inductance matrix, with self-inductance L_{self} and mutual M_{ij} , $i \neq j$ between each nanowire, \mathbf{V} and \mathbf{I} are column vectors with the voltage and current in each nanowire, respectively, and s is the Laplace variable (that is replaced by $j\omega$ when calculating the system for different frequencies).

In a region with N nanowires, the matrices \mathbf{L} and \mathbf{R} are square matrices with size $N \times N$. The resistance matrix \mathbf{R} is a diagonal matrix, since there are no conduction path between nanowires. The inductance matrix \mathbf{L} is a matrix with the main diagonal having the self-inductance for each nanowire and mutual inductances between nanowires i and j inside the region on the other positions. In this way the \mathbf{L} matrix is symmetric. The nanowire resistance R_{nw} , self-inductance L_{self} and mutual inductance M_{ij} can be calculated as follows [27]:

$$R_{nw} = \frac{h}{\pi * r^2 * \sigma_{copper}} \quad (3)$$

$$L_{self} = \frac{\mu_0}{2\pi} h \left[\ln \left(\frac{h}{r} + \sqrt{\left(\frac{h}{r} \right)^2 + 1} \right) - \sqrt{\left(\frac{r}{h} \right)^2 + 1} + \frac{r}{h} + \frac{1}{4} \right] \quad (4)$$

$$M_{ij} = \frac{\mu_0}{2\pi} h \left[\ln \left(\frac{h}{d_{ij}} + \sqrt{\left(\frac{h}{d_{ij}} \right)^2 + 1} \right) - \sqrt{\left(\frac{d_{ij}}{h} \right)^2 + 1} + \frac{d_{ij}}{h} \right] \quad (5)$$

where d_{ij} is the center-to-center distance between nanowires, r is the radius of each nanowire and h their height.

To solve the system in eq. (2), it is used the condition that the voltage drop is the same for all nanowires, or in a numerical approach that $\mathbf{V} = \mathbf{1}$, i.e, each $V_i = 1$, i from 1 to N and $\mathbf{1}$ is a column vector of size N where all elements are 1. Then the solved currents become:

$$\mathbf{I} = (\mathbf{R} + s\mathbf{L})^{-1}\mathbf{1} \quad (6)$$

To find the equivalent impedance Z_{eq} of the system, that gives us the equivalent resistance R_{eq} and inductance L_{eq} , one can make use of the voltage drop that is the same for all nanowires and the total current in the region $I_{total} = \mathbf{1}^t \mathbf{I}$ (the sum of the currents in each nanowire):

$$Z_{eq} = R_{eq} + j\omega L_{eq} = \frac{V}{I_{total}} = \frac{1}{\mathbf{1}^t (\mathbf{R} + j\omega \mathbf{L})^{-1} \mathbf{1}} \quad (7)$$

To solve eq. (7) in lower frequencies, first the denominator can be expanded using Taylor, becoming:

$$(k + x)^{-1} = k^{-1} - k^{-2} \cdot x + k^{-3} \cdot x^2 - k^{-4} x^3 + O(x^4) \quad (8)$$

for values of x near 0 and converging when $|x| < |k|$. When $|x| \ll |k|$ the series quickly converges, and the two first terms gives a very accurate approximation. For our case, comparing \mathbf{R} and $s\mathbf{L}$, and making the Laplace variable $s = j\omega$, we can see that $\|j\omega \cdot \mathbf{L}\| \ll \|\mathbf{R}\|$ when the frequency $\omega = 2 \cdot \pi \cdot f$ is small enough for a given matrix norm. This way, eq. (7) becomes:

$$\begin{aligned} Z_{eq} &= \frac{1}{\mathbf{1}^t (\mathbf{R} + s\mathbf{L})^{-1} \mathbf{1}} \stackrel{(k+x)^{-1}=(k^{-1}-k^{-2}x), |x| \ll |k|}{\cong} \frac{1}{\mathbf{1}^t R_{nw}^{-1} \mathbf{1} \mathbf{1} - R_{nw}^{-2} s \mathbf{1}^t \mathbf{L} \mathbf{1}} \stackrel{(k+x)^{-1}=(k^{-1}-k^{-2}x), |x| \ll |k|}{\cong} \\ &\cong \frac{R_{nw}}{N} + \frac{s \mathbf{1}^t \mathbf{L} \mathbf{1}}{N^2} \Rightarrow R_{eq} = \frac{R_{nw}}{N}; L_{eq} = \frac{\mathbf{1}^t \mathbf{L} \mathbf{1}}{N^2} \end{aligned} \quad (9)$$

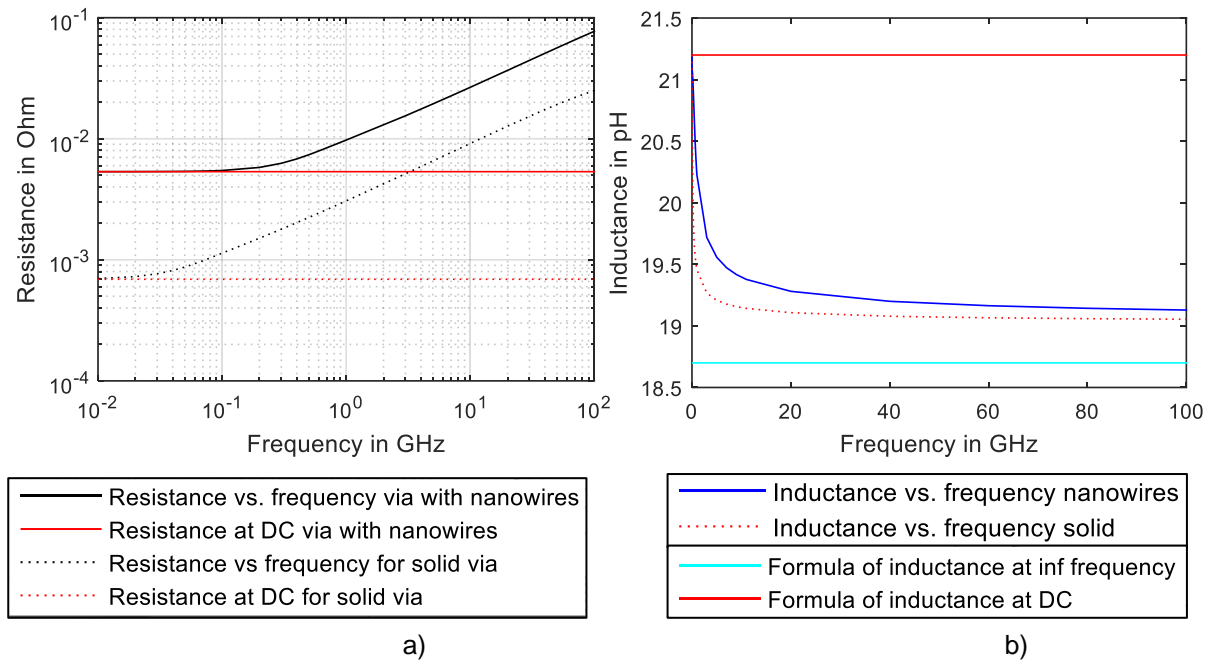
with the matrices \mathbf{R} and \mathbf{L} with size $N \times N$. The resulting L_{eq} from this approximation is the same as discretizing the formula with integrals for a solid via, with the resistance in \mathbf{R} being the resistance of each partition, where it is assumed the internal current density to be homogeneous throughout the entire cross-section of a region ([27], chapter 6.1). In the same way, the equivalent mutual inductance between two regions assuming the current distribution is homogeneous in the two regions (near DC) is calculated in the same way as in eq. (9) for L_{eq} , using a mutual matrix \mathbf{M} in place of a matrix \mathbf{L} ($M_{eq} = \frac{\mathbf{1}^t \mathbf{M} \mathbf{1}}{N^2}$), defined analogously as \mathbf{L} , with the nanowires in different regions and using the eq. (5) for calculating the mutual inductance.

At higher frequencies $\|j\omega\mathbf{L}\|$ increases and the current in the nanowire-via starts to be influenced by the skin-effect. Using this matrix approach, the calculus for the nanowire-via is the same as if we wanted to calculate the equivalent resistance and inductance of a solid via, as for the calculus of a solid via, it is partitioned in small areas that on the limit can be represented by the nanowires, since the membrane has a high nanowire density of about 95 nanowires per square micron. The main difference between both vias cases is the resistance of each partition, that changes the term \mathbf{R} in $(\mathbf{R} + s\mathbf{L})$, thus changing Z_{eq} . The notion that a via composed of parallel not sideways connected wires has skin-effect comes naturally, since the skin-effect is a magnetic phenomenon, even though at first for a nanowire-via this might not be the case, as will be shown. A comparison between a nanowire-via and a solid via is then be performed to access on how they differ.

The approach described here is applied to a circular nanowire-via with $6.42 \mu\text{m}$ in diameter. This value was chosen as we have from the center of the via to the border about 70 nanowire, being a good trade-off of a via large enough to observe the skin-effect and with the possibility to simulate with MATLAB without memory limitation. In this comparison, a copper nanowire-via is compared to a solid copper via. For the calculus, the nanowires were organized in a hexagonal honeycomb way, as they are physically on the membrane, with each nanowire having 40-nm-diameter and center-to-center nanowire distance of 107 nm (ccd). The solid circular via has an equivalent hexagonal partition, with each hexagon having an apothem of $ccd/2$ and the self-inductance for the partition considering a circular partition with radius also $ccd/2$. The

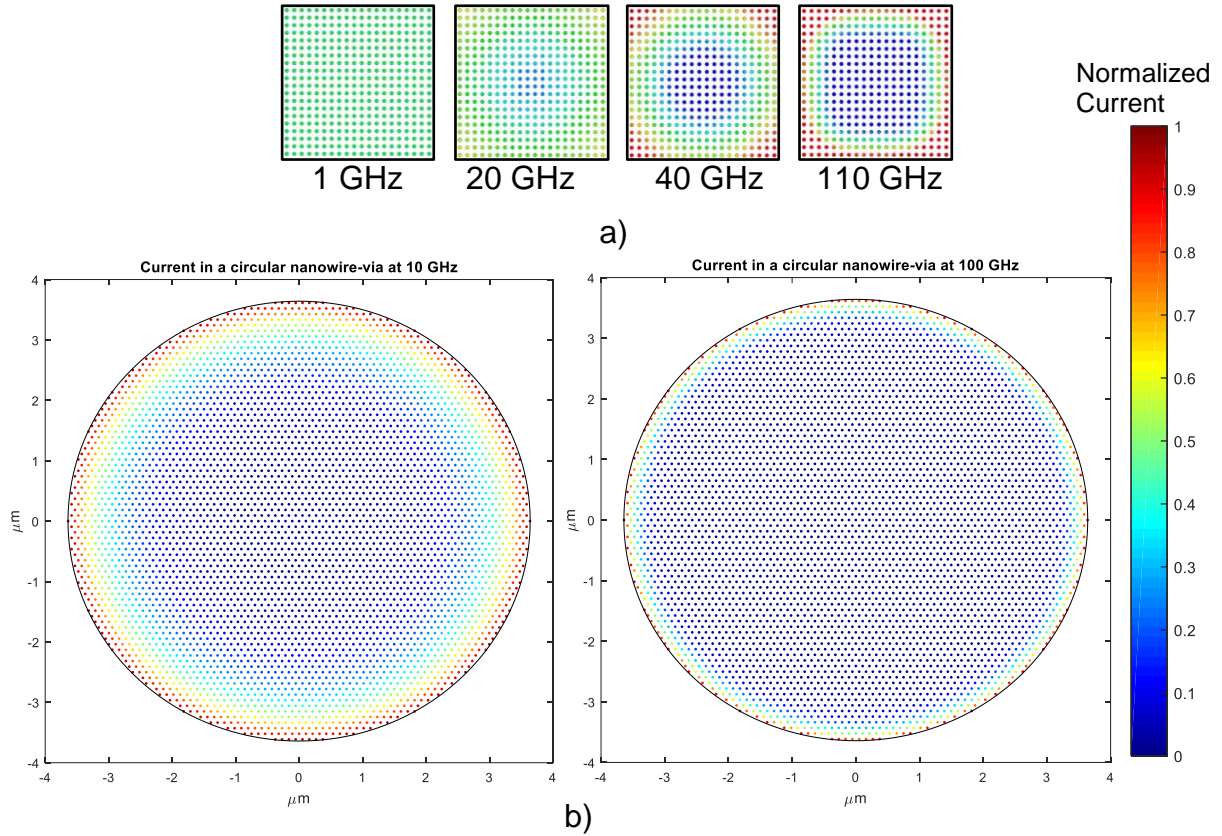
calculated resistance is shown in Figure 30 a), whereas the calculated inductance is shown in Figure 30 b), vs. frequency for the nanowire-via and solid via. At higher frequencies, where the skin-effect is observed, the resistance of the via is directly proportional to $1/\sqrt{\sigma}$. The equivalent conductance for the nanowire-via σ is thought to be proportional to the nanowires area density (dst) as $\sigma_{copper} * dst$. This can be confirmed by the results presented in Figure 30 a), where $R_{solid\ via}/R_{nanowire-via}$ gives \sqrt{dst} . In Figure 30 b), the nanowire-via presents a slightly higher inductance overall than the solid via.

Figure 30 – In a) resistance and in b) inductance of solid copper via and copper nanowire-via.



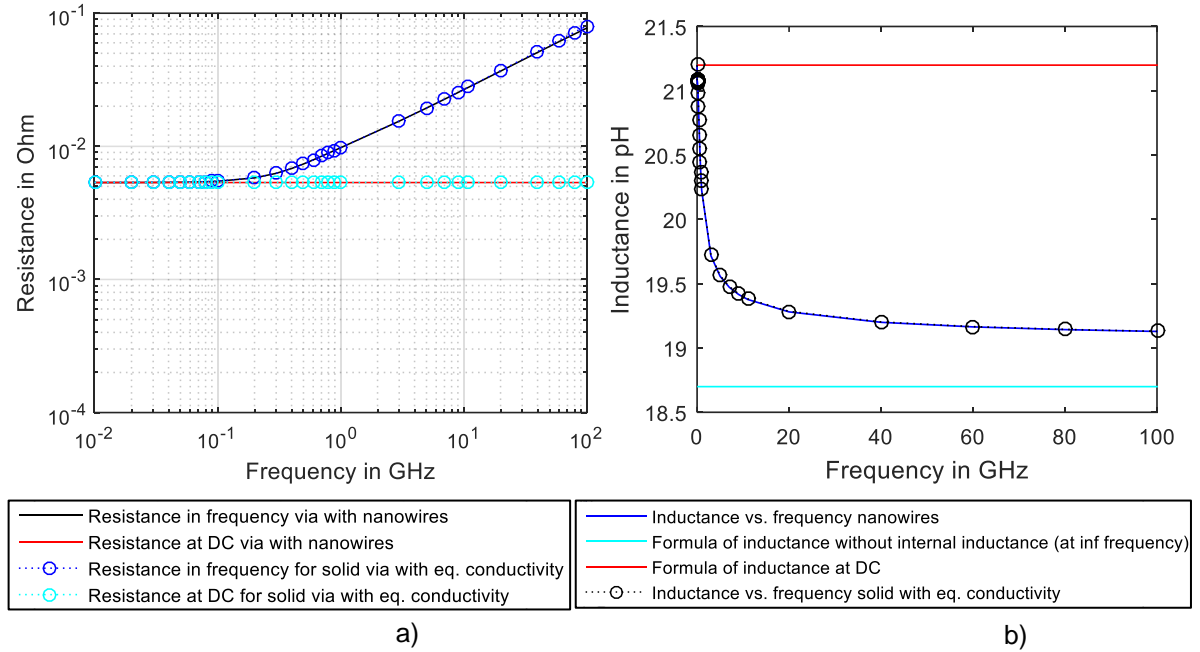
To further endorse the matrix calculus for the nanowire-via, the current in each nanowire was plotted and compared to a 2-D magnetostatic square nanowire-via simulation carried out with Ansys Maxwell. Results for the matrix approach can be seen in Figure 31 a) for Maxwell simulations and in Figure 31 b) for the matrix calculus. The skin-effect can be well observed in both cases, as at 1 GHz, the current is almost the same over all the nanowires in the nanowire-via and when the frequency increases, only peripheral nanowires conduct the current (red dots), and the current in the central nanowires vanishes (blue dots).

Figure 31 – 2-D simulation of a nanowire-via at different frequencies showing the skin effect in nanowire-vias. The dots are the cross section of each nanowire. The red and blue dots indicate high and low current densities, respectively. In a) a square nanowire-via simulated in Maxwell and in b) a circular nanowire-via in MATLAB using the matrix approach. The skin-effect is observed in both cases



The relation between $R_{solid\ via}/R_{nanowire-via}$ that gives \sqrt{dst} can be further explored to compare a nanowire-via with a solid via with a conductance of $\sigma_{copper} * dst$. Results are shown in Figure 32.

Figure 32 – In a) resistance and in b) inductance vs. frequency of a nanowire-via and a solid via with metal conductance multiplied by the nanowires density.



From Figure 32, it can be concluded that a nanowire-via has the same resistance and inductance as a solid via with the metal conductivity taking into account the nanowires density. This can also be concluded when closely analyzing the system from eq. (2). On the system, the difference in the \mathbf{L} matrix between a nanowire-via and a solid via case is only the main diagonal, i.e., the self-inductance of a nanowire or a partition for the solid via. As the value of the self-inductances is very close, this difference does not disturb the system, as can be seen in the DC value found for L_{eq} for both nanowire-via and solid via being almost the same. Thus, the main difference between the system in both cases is the \mathbf{R} matrix, where if the resistance of a solid via partition is changed to the resistance of a nanowire, it is the same as changing the metal conductivity of the solid via taking into account the relationship between both partitions areas, that is the definition of the nanowire area density on the membrane. This way we can conclude that the nanowire-via electrical characteristics is the same as a solid via with a different metal conductivity ($\sigma = \sigma_{copper} * dst$).

2.2.3.3 R_{via} , G_{via} , C_{via} calculation and model validation

The value for C_{via} was obtained by using a simple parallel plate capacitance calculation using V_x , V_d , a 50- μm -via height and ϵ_r of the membrane. The parameter R_{via} was calculated as a sum of a DC and frequency dependent component. For the DC component, since the cross section of the via is composed of nanowires, an equivalent area equal to the sum of the cross-section areas of all nanowires in the via was used. The frequency dependent component accounts for the skin effect present in the nanowire-via, which increases R_{via} value with frequency, as seen in the section previous.

The values calculated by this manner for L_{via} , R_{via} and C_{via} were used as initial values in the lumped elements model in Figure 28 b). Next, the values were adjusted to fit the measurements. The calculated values of R_{via} (DC component), L_{via} , and C_{via} remained unchanged, whereas the values of R_{via} (frequency dependent component) and G_{via} had to be adjusted to provide a good fitting to the measurements. The final values are given in Table 3.

Table 3 – Parameters for the Via Model.

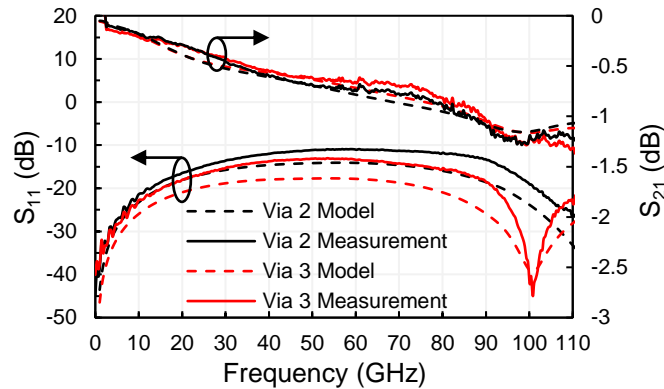
Via	Parameter	Value
All vias	G_{via} (S)	$680 * 10^{-18} f(\text{Hz})$
Via 1a	R_{via} (Ω)	$0.005 + 1.2 * 10^{-6} \sqrt{f(\text{Hz})}$
	L_{via} (pH)	13.4
	C_{via} (fF)	3.6
Via 2	R_{via} (Ω)	$0.009 + 3 * 10^{-6} \sqrt{f(\text{Hz})}$
	L_{via} (pH)	15.9
	C_{via} (fF)	2.7
Via 3	R_{via} (Ω)	$0.009 + 4 * 10^{-6} \sqrt{f(\text{Hz})}$
	L_{via} (pH)	15.9
	C_{via} (fF)	1.9
Via 4	R_{via} (Ω)	$0.013 + 3.7 * 10^{-6} \sqrt{f(\text{Hz})}$
	L_{via} (pH)	17.7
	C_{via} (fF)	1.4

The trend for the values of R_{via} is consistent with the theory, showing the structure with Via 1a as the best performing one, since it has the largest cross section. Nevertheless, all the extracted values are very small, difficult to extract and prone to

errors. This does not constitute a problem, as by using values of this magnitude it is possible to predict the via behavior and its performance correctly with little dispersion, as discussed in next section.

Figure 33 presents the simulated results of two different structures with pads, CPW feeding lines ($L_1 = 250 \mu\text{m}$), and vias as presented in Figure 23, as well as their measurements. It can be seen that the results are in good agreement, showing that the transition lumped elements model combined with the CPW 3-D EM model can predict the response of the whole structure, thus being able to predict the loss in a single via transition.

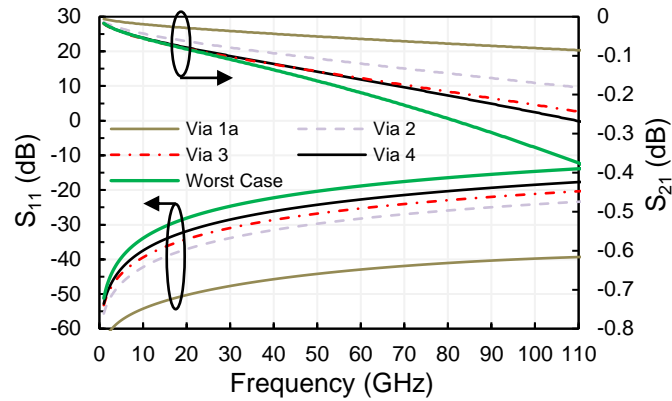
Figure 33 – Measured and modeled S-parameters of the structure with vias (Via 2 and Via 3) presented in Figure 23, with $L_1 = 250 \mu\text{m}$.



2.2.4 Comparison to the state-of-the-art

The proposed model for the nanowire-vias was used to simulate a single transition without any CPW, to verify its performance at mm-wave frequencies. The simulated results of four different via sizes are shown in Figure 34. To be more conservative when estimating the nanowire-via transition performance, a best/worst case scenario is also shown in this figure. The best case is the Via 1 performance itself and the worst case is obtained by varying in 50% the values of the worst via parameters (Via 4) given in Table 3. This shows that their exact values are not as relevant as their order of magnitude, since they still provide a high performance response when they are varied. Considering that the measurements accuracy is estimated in the order of ± 0.1 dB at 110 GHz, which is the same order of the loss in each transition, it is difficult to ensure the model accuracy.

Figure 34 – Modeled S-parameters of each single via transition.



The worst case exhibits insertion loss of 0.37 dB at 110 GHz with a return loss always better than 14 dB. Although Vias 2 and 3 are of the same size, they present different responses, with a difference of 0.05 dB in S_{21} at 110 GHz. This difference can be considered as very low and could be explained by the different orientation in the structure or more likely by the model and measurements accuracy. Finally, the mean value of the insertion loss of all vias, considering the worst-case scenario, is 0.23 dB with a min-max variation of ± 0.14 dB.

State-of-the-art results of TSVs in different technologies are provided in Table 4. It can be seen that the performance of the nanowire-vias is considerably better than the ones presented in the literature.

Table 4 – Comparison of existing via technologies for mm-wave applications.

Ref.	Substrate Material	Transmission loss of two transitions (dB)	Via size	Via length
[18]	Glass	0.07 @ 20 GHz	\varnothing 40 μm	64 μm
[15]	Glass	0.68 @ 50 GHz	\varnothing 55 μm	366 μm
[19]	LCP	0.24 @ 40 GHz	\varnothing 105 μm	51 μm
[4]	LCP	1 @ 100 GHz 2 @ 110 GHz	\varnothing 50 μm	51 μm
[26]	Si (HR)	0.06 @ 40 GHz	190 μm x 120 μm	100 μm
[3]	Si (HR)	1.06 @ 75 GHz	\varnothing 42 μm	250 μm
This work	AAO	0.46 dB @ 110 GHz	20 μm x 45 μm	50 μm
This work	AAO	0.2 dB @ 110 GHz	50 μm x 32 μm	50 μm

2.2.5 Summary

For the first time, experimental results of nanowire-vias were demonstrated up to 110 GHz. The nanowire TSVs were used as transitions to interconnect CPWs between the top and bottom layers of the substrate. The nanowire-via performance show state-of-the-art results, when compared to technologies in Si, HR-Si, glass and LCP, reported so far in the literature. A first-order approximation model was proposed for the nanowire via transition to evaluate its performance and it predicts a range of expected values. The model predicts the via response up to 110 GHz, which showed a mean insertion loss of 0.23 dB and a min-max values of ± 0.14 dB up to 110 GHz for vias with different dimensions. Moreover, this technology offers a great flexibility in the via design that cannot be obtained with other technologies.

2.3 3-D solenoid inductor

2.3.1 Introduction

One important passive device that has significant influence on a system performance is the inductor [28]. Inductors can be used in a variety of circuits as in building blocks for other passive structures as filters, diplexers/triplexers, matching networks, resonators and in conjunction with active devices as low-noise amplifiers (LNAs), voltage-controlled oscillators (VCOs), power amplifiers (PAs) and mixers.

On-chip spiral planar inductors are widely used because they are the most compatible with CMOS processes. These inductors occupy large areas and suffer from low quality factor (Q-factor) caused by their thin metallization layers, the loss from the semiconductor substrate and parasitic capacitances between conductors and between conductors and substrate. Other kinds of inductors using high resistivity silicon have been demonstrated with good quality factors [24], but they are associated with a major cost increase due to the special substrate, and still require large footprints. Selectively removing the silicon substrate [29], the above IC realization [30], or MEMS-based [31] inductors are also interesting solutions, but also lead to an important cost and complexity increase. A natural solution is to fabricate off chip the large passive devices, such as inductors, antennas, diplexers, and couplers, using a suitable substrate that

can be interconnected to the active chip using 3-D hybrid integration technologies – an interposer.

For that, through substrate vias (TSVs) are needed and they can be easier to be fabricated in an alternative substrate than in integrated technologies. By using TSVs, it becomes simpler to fabricate solenoid-type inductors with advantages such as compactness, higher Q-factor and higher self-resonance frequency than their planar spiral-type inductors counterparts [32]. Inductors have been reported using interposer technologies such as low temperature cofired ceramic (LTCC), glass, liquid crystal polymer (LCP) and high-resistivity silicon (HR-Si). Nonetheless, TSVs can increase considerably the fabrication cost and suffer from low aspect ratio, leading to large inductors exhibiting large footprints [24], [33]–[35].

Inductor modelling is a powerful design tool, as it is easier to use a lumped elements model than a simulated or measured response in circuit design and to give an insight on how to improve their performance. Complex models can provide low error and high accuracy. These complex models rely heavily on optimization to extract their parameters from S-parameters measurements.

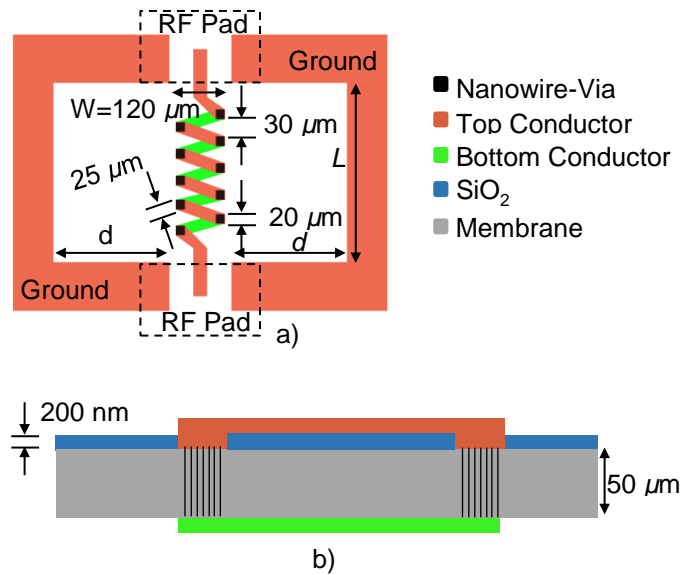
In this section, 3-D solenoid inductors using nanowire-vias realized in the MnM substrate are designed, fabricated, measured and modelled. Solenoid type inductors have been reported in the same technology as this work, but in lower frequencies up to 20 GHz and using solid TSVs, adding a step to open the substrate in the fabrication process [36]. In section 2.3.2 its topology is presented followed by the fabrication process used in section 2.3.3. In section 2.3.4 the characterization setup is described and the measured S-parameters presented. The proposed electrical model is presented in section 2.3.5, and then the inductors performance is compared to the literature in section 2.3.6. A summary the work done with the inductor is presented in section 2.3.7.

2.3.2 Design

The proposed 3-D solenoid inductor, illustrated in Figure 35, is formed by two metal layers, one at the top and the other at bottom of the 50- μm thick membrane, interconnected by nanowire-vias. The nanowire-vias provide great flexibility for the inductor design, as there are no processing constraints for their size or shape besides

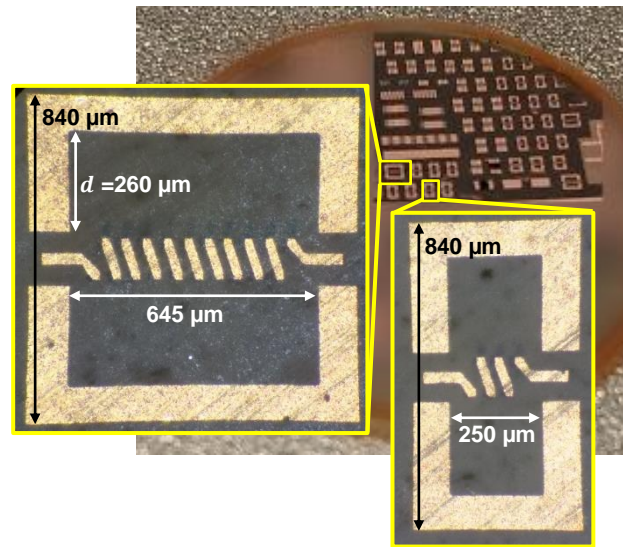
the photolithography used to realize the via. Therefore, all the dimensions provided in Figure 35 can be modified according to the designer's needs. The length of the inductor (L), its width (W), the separation between turns, the size of the vias and the width of the top and bottom strips, in this case $30\text{ }\mu\text{m}$, $20\text{ }\mu\text{m}$ and $25\text{ }\mu\text{m}$, respectively, can be adjusted accordingly. Figure 35 also shows the RF contact pads used for $50\text{-}\Omega$ characterization.

Figure 35 – Illustration of a 5-turns inductor using nanowire-vias with dimensions. In a) top view, in b) front view.



All of these dimensions change the inductor response: it is well-known that the higher the number of turns, their density and their size, the higher the inductance, and hence the lower the inductor self-resonant frequency (SRF). Several inductors with different number N of turns ($N = 2, 3, 5$ and 10 turns), same width $W = 120\text{ }\mu\text{m}$ and different lengths $L = 250\text{ }\mu\text{m}$ for $N = 2$ and 3 , $365\text{ }\mu\text{m}$ for $N = 5$, and $645\text{ }\mu\text{m}$ for $N = 10$ were simulated (in ADS Momentum, from Keysight), fabricated, and measured. Figure 36 shows the fabricated membrane with 10-turns and 3-turns 3-D inductors in detail.

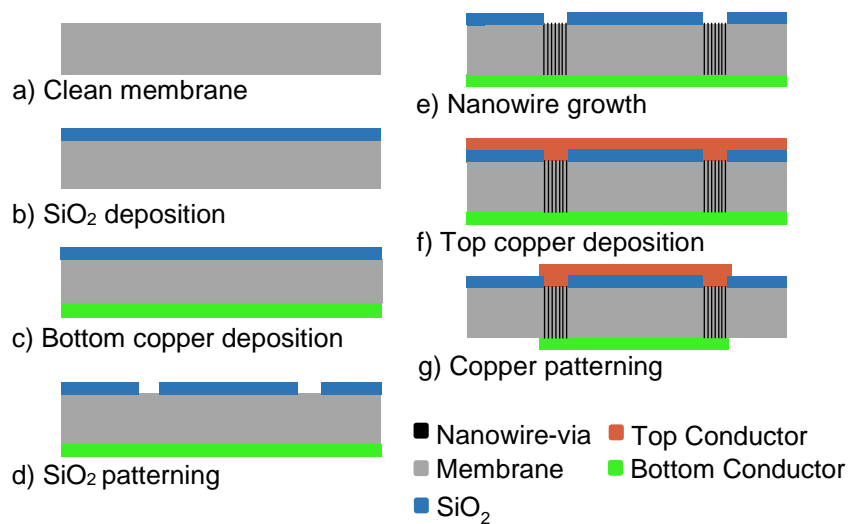
Figure 36 – The fabricated membrane with the 3-D inductors. In detail a 10-turns (left) and a 3-turns (right) inductor.



2.3.3 Fabrication process

The fabrication steps of the 3-D inductors in the porous alumina substrate are presented in Figure 37. For the process described below, AAO membranes from Synkera with 55-nm-pore diameter were used.

Figure 37 – Steps of the 3-D solenoid inductors with nanowire-vias fabrication process.



The steps for the fabrication process are:

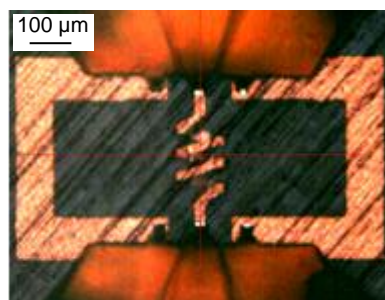
- Initially, the membrane is cleaned in acetone and isopropanol;

- b) A 300-nm silicon dioxide mask-layer (SiO_2) is deposited via reactive magnetron Sputtering;
- c) A copper seed layer is deposited by sputtering and thickened ($2\text{ }\mu\text{m}$) by electrodeposition using MacDermid Enthone's CUPROSTAR LP 1 acid plating process;
- d) The SiO_2 layer is patterned by photolithography and etched by BOE (buffered oxide etch);
- e) Nanowires are grown by electrodeposition using MacDermid Enthone's MacuSpec PPR 100 acid copper plating process;
- f) A new copper layer is deposited on the top of the membrane by sputtering and then thickened as in c);
- g) The copper layers are patterned with photolithography and etched by AlphaCleaner's Super Etch 160 forming the upper and lower strips of the inductor.

2.3.4 Characterization

The inductors were characterized up to 110 GHz using GSG probes (MPI Titan probes with $100\text{ }\mu\text{m}$ -pitch) in a 300 mm semi-automatic probe station and an Anritsu Panorama ME7808C vector network analyzer (VNA). A line-reflect-reflect-match (LRRM) calibration was employed using a Cascade impedance standard substrate (ISS). In order to prevent short-circuiting the bottom of the inductors with the metallic chuck of the probing station, a 5-mm thick ROHACELL 51 IG foam was used as spacing. This foam has $\epsilon_r = 1.05$ and $\tan\delta = 0.0135$ at 26.5 GHz. Figure 38 shows a fabricated 3-turns 3-D inductor under measurement.

Figure 38 – Picture of a fabricated 3-turns 3-D inductor under measurement.



It was chosen to fabricate the 2-turns and the 3-turns inductors with the same length. The one with 2-turns could be shorter, but if the distance between probes is less than 250 μm , the coupling between them could interfere on the device response.

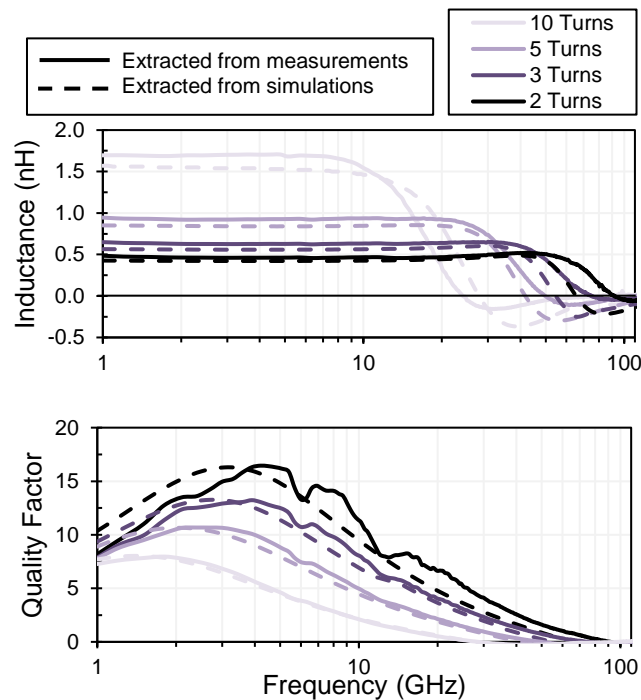
The characteristics of the inductor such as its inductance (L) and quality factor (Q) were extracted from the measured S-parameters and are presented in Figure 39. The inductance and quality factor were extracted from the Y-parameters calculated from the measured S-parameters as:

$$L = \frac{\text{Im}\{Y_{11}^{-1}\}}{2\pi f} \quad (10)$$

$$Q = -\frac{\text{Im}\{Y_{11}\}}{\text{Re}\{Y_{11}\}} \quad (11)$$

It can be seen in Figure 39 that the behavior of the inductance and quality factor are those expected for an inductor, with the SRF of each inductor at approximately 24 GHz, 50 GHz, 75 GHz and 92 GHz, respectively, where the lowest SRF refers to the longest inductor with 10 turns. The Q-factor reaches a maximum of 16 for the shortest and 8 for the longest inductor. The inductances values range from 0.5 nH to 1.7 nH.

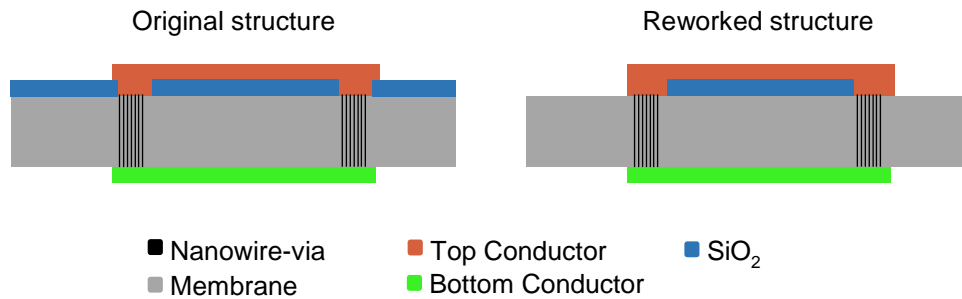
Figure 39 – Extracted inductance and Q-factor of the measured (full line) and simulated (dashed line) inductors.



The results presented in Figure 39 could be greatly improved. The fabricated inductors presented low Q -factor compared to the initial simulations. A close investigation measuring the resistivity of the SiO_2 oxide showed that there was a problem in the fabrication process. A thin layer of residual metal was left over the oxide, increasing its conductivity. Therefore, the simulations provided in Figure 39 were performed considering this thin poorly conductive layer, agreeing well with measurement results.

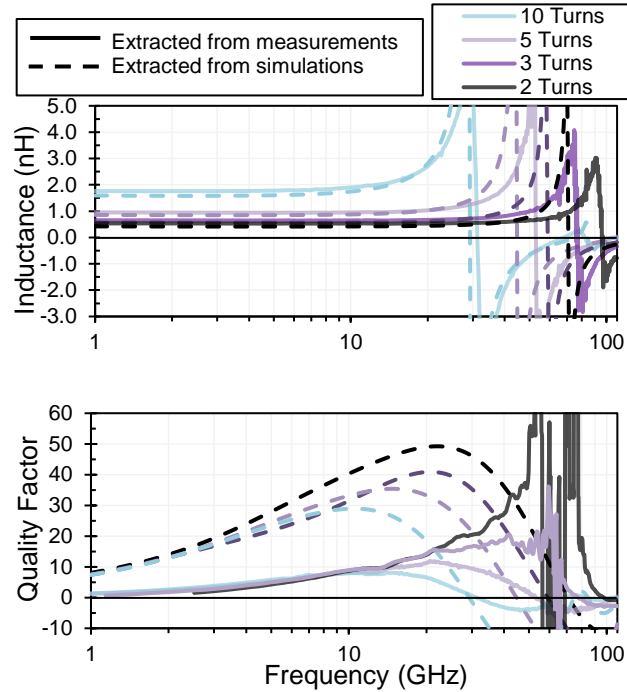
To improve the inductors response, the SiO_2 was partially removed by a BOE solution. The final structure can be seen in Figure 40, where the SiO_2 layer was removed, but remained beneath the top inductor strip due to the wet etching difficult access.

Figure 40 – Front view of the inductors before and after the SiO_2 oxide layer removed.



After this treatment, inductors were measured again, leading to much better results. The characteristics of the inductor such as its inductance (L) and quality factor (Q) were extracted from the new S-parameters and are presented in Figure 41, with ADS Momentum simulations with an air layer in place of the SiO_2 oxide. The inductances ranged from 0.5 nH to 1.7 nH, with SRF ranging from approximately 31 GHz up to 98 GHz. Experimental results show a maximum Q -factor of 35 before a noisy region for the shortest inductance with 2 turns, and 8 for the longest inductor with 10 turns.

Figure 41 – Results extracted from the measured 3-D inductors (full line) and from the ADS/Momentum simulation of the 3-D inductors (dashed line). The image features the extracted inductance and extracted quality factor.



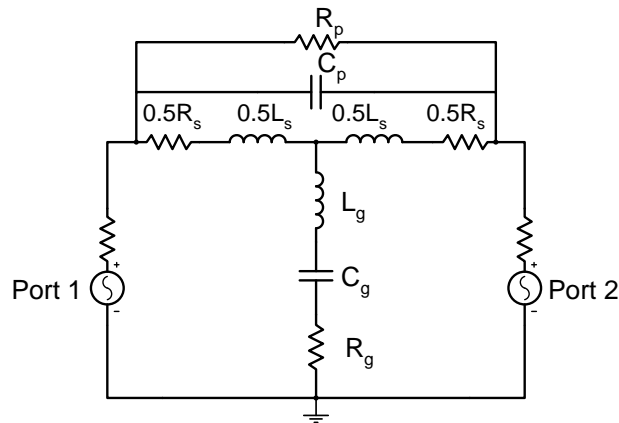
The ADS Momentum simulations exhibit a slightly lower SRF than the measurements; this can be explained by an alumina corrosion inside the nanopores caused by the SiO_2 wet etching BOE solution. The fabricated structure having less alumina, compared to a new membrane, leads to a lower capacitance between spires, and thus a higher measured SRF. The quality factor is also higher with the EM Momentum simulations, indicating that the fabricated copper might have more resistivity than a good copper; or, since the measurements are embedded, i.e., the influence of the contact probes were not removed, the contact resistance caused by the measuring probes might play a role.

2.3.5 Electrical Model

The modelling of the inductors with 3-D EM tools is time-consuming for circuits' designers, depending on the technology used, and electric models must be developed so that a technology can be efficiently used by designers. In addition, the electric model can give an insight on the parasitic elements of the inductor and help improve its performance.

In [37], both “ Π ” and “T” lumped elements models were proposed to model embedded inductors. A “T” topology, illustrated in Figure 42, was chosen to model the proposed inductors, since it is a simple circuit model based on lumped elements that can be related to the physical structure of the 3-D solenoid inductor, which is not the case for the “ Π ” topology with these inductors. The presented “T” topology is slightly different from the one proposed in [37].

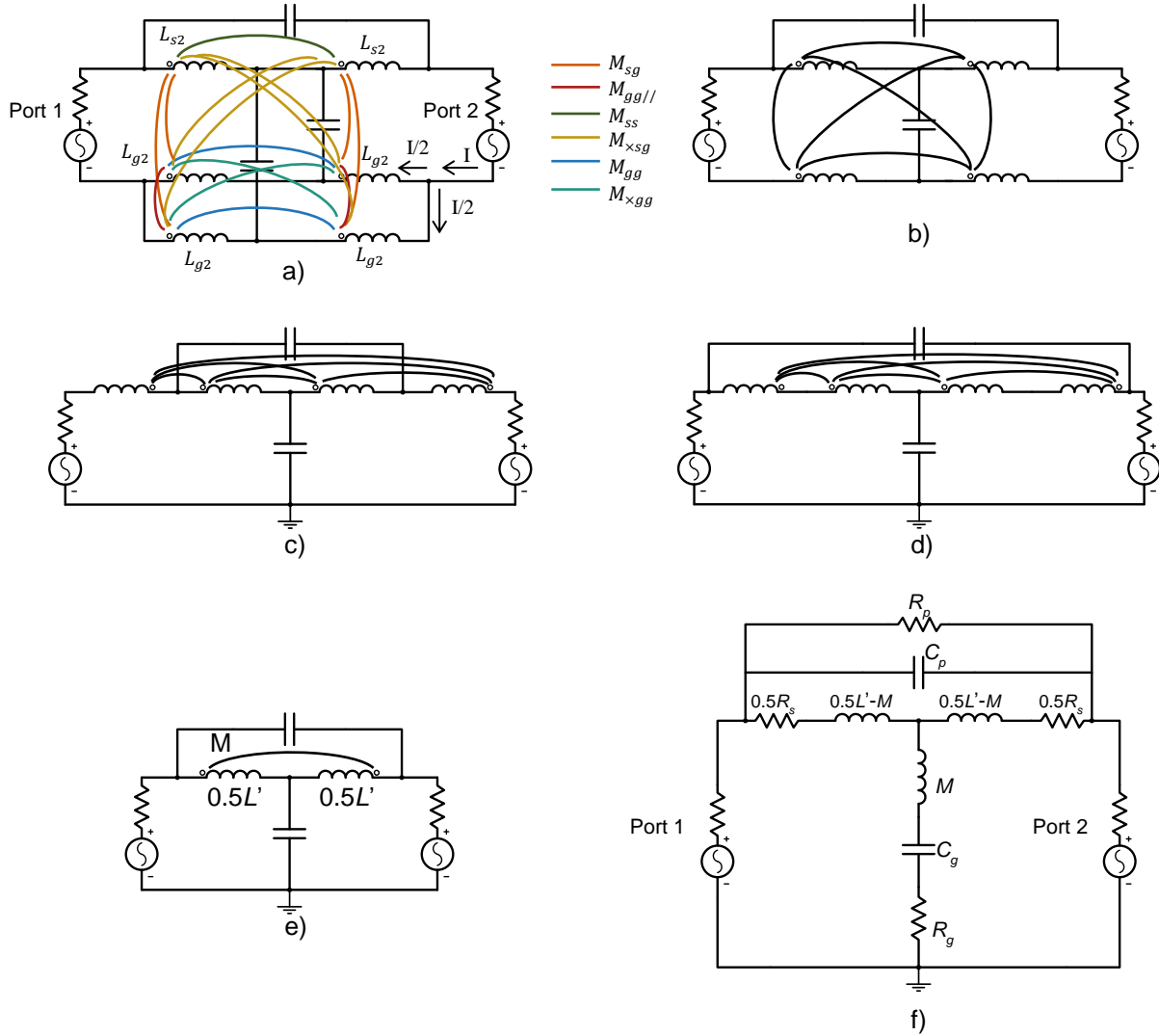
Figure 42 – “T” Model utilized for the 3-D inductors.



The “T” model, although derived directly from measurements results for solenoid inductors in [37], can also be derived when analyzing the solenoid physical structured. For that, we can start representing the solenoid structure from Figure 35 a) as in Figure 43 a), where the solenoid and two ground parts are modelled as inductances. In Figure 43 a) it is represented all mutual inductances between the half solenoid (L_{s2}) and the halves grounds (L_{g2}). The parallels halves grounds and the capacitances between the center of the solenoid and the center of the two grounds can be combined leading to Figure 43 b). Next, the ground inductance can be changed from the bottom part of the circuit to the top, i.e., it is equivalent having it in series, as at the end the loop voltage is the same, with this situation represented in Figure 43 c). The capacitance in parallel with the solenoid inductances in the circuit would only have influence at higher frequencies, and to have a compact model it is considered as encompassing the inductors from the ground plane, resulting in Figure 43 d). The model is then simplified and the four inductances are condensed as two inductances in Figure 43 e). Using a coupled inductors equivalent circuit, the final circuit in Figure 43 f) is derived; the same circuit as in Figure 42. In Figure 43 f), the losses are accounted with the addition of

resistances in series with the inductors, in parallel with the top capacitance and in series with the capacitance connected to the ground.

Figure 43 – Steps for simplifying the electrical model derived from a physical interpretation of the 3-D solenoid structure.



After all the simplification shown in Figure 43, the inductances L' and M from Figure 43 f) compared with those from Figure 43 a), can be expressed as:

$$0.5L' = L_{s2} + 0.5 * (L_{g2} + M_{gg//}) - 2 * M_{sg} \quad (12)$$

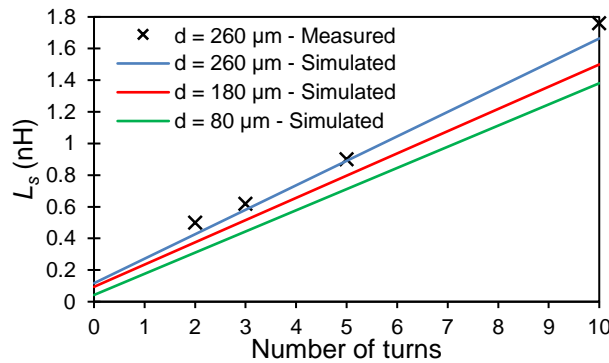
$$M = L_g = 2 * M_{xsg} - M_{ss} - 0.5 * (M_{gg} + M_{xgg}) \quad (13)$$

In this way, the series inductance L_s from Figure 42, that is the inductance that is measured by eq. (10), is related to L' and M as:

$$L_s = L' - 2 * M = 2 * L_{s2} + L_{g2} + M_{gg//} - 4 * M_{sg} - 4 * M_{\times sg} + 2 * M_{ss} + M_{gg} + M_{\times gg} \quad (14)$$

The elements from the “T” model from Figure 42 can be related to the physical layout; the resistance R_s is related to the resistance of the solenoid and return path, the inductance L_s is related to the inductance of the solenoid, ground plane and all mutual inductances shown in Figure 43 a) and in eq. (12) to (14). The resistance R_p models the resistance between the turns of the inductor, due to losses into the dielectric. The capacitance C_p corresponds to the parasitic coupling between the turns. The resistance R_g and the capacitance C_g are related to the gap between the turns and the ground plane. From [37], it is argued that L_g is related to the mutual inductance between turns, but as derived and shown in eq. (13), it also contains the influence of the mutual inductance between the solenoid and the return path (ground plane), which is not negligible. By examining simulations carried out in ADS/Momentum changing the d dimension (Figure 44) from the return path and analysing its influence in the extracted inductance L_s , we can clearly see that the ground plane influences the extracted solenoid inductance. For a solenoid design, the return path geometry needs to be taken into account.

Figure 44 – L_s extraction from measurements and simulations, versus the number of turns for different ground plane configurations.



The parameters of the model from Figure 42 were fitted to the measurements. The results are given in Figure 45 and Figure 46, showing a good agreement between electrical model and experimental result. Figure 45 show S-parameters from the measurements and from the model for the 2-turns and 10-turns inductors. For the 2-turns inductors the model can predict all measured data. For the 10-turns inductors the model cannot predict the S-parameter response beyond 70 GHz, but this frequency is more than two times the self-resonance frequency of 30 GHz of the inductor and more

than three times the frequency of 16 GHz corresponding to the maximum Q -factor for this inductor. Hence, the developed model is accurate for operation frequencies.

Figure 45 – S-parameters measured results (full line) and the model utilized for the inductors structures (dashed line).

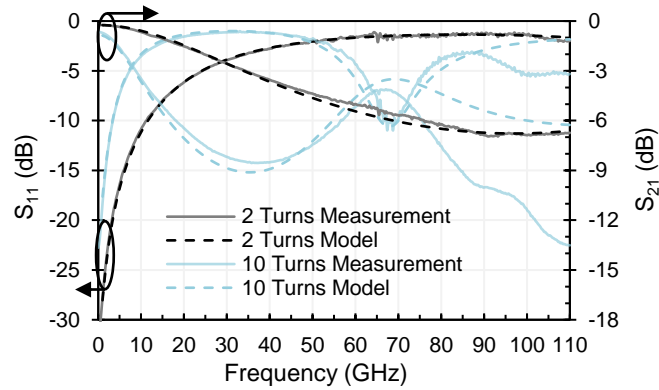
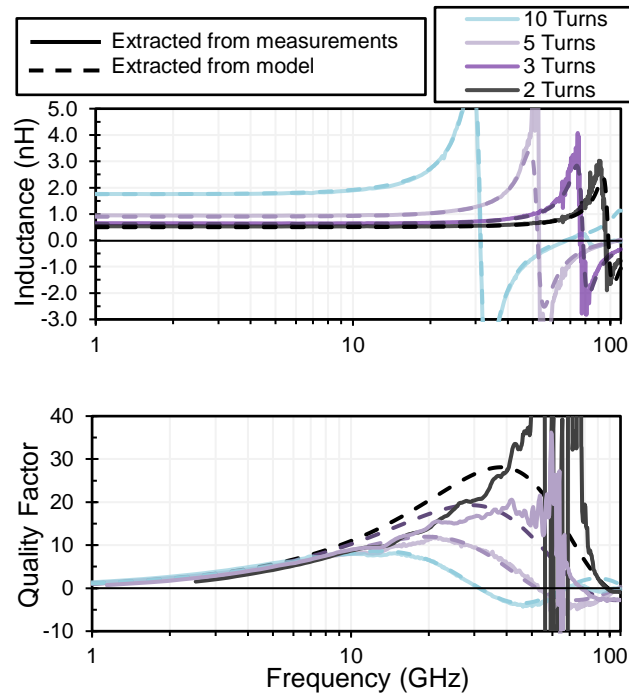


Figure 46 shows the model simulation for the inductance value and quality factor compared to the data extracted from measured S-parameters.

Figure 46 – Results extracted from the measured 3-D inductors (full line) and from the modelling of the 3-D inductors (dashed line). In a) extracted Inductance and in b) Q -factor.



The simulated and measured results from Figure 46 shows that the model agree well when predicting the equivalent inductance value over frequency. For the quality factor, it predicts well the 10 and 5-turns inductors, but there is some disagreement for the 3 and 2-turns inductors. It can be due to the fact that all resistances and

inductances in the lumped elements model do not vary in frequency, as it should because of the skin-effect.

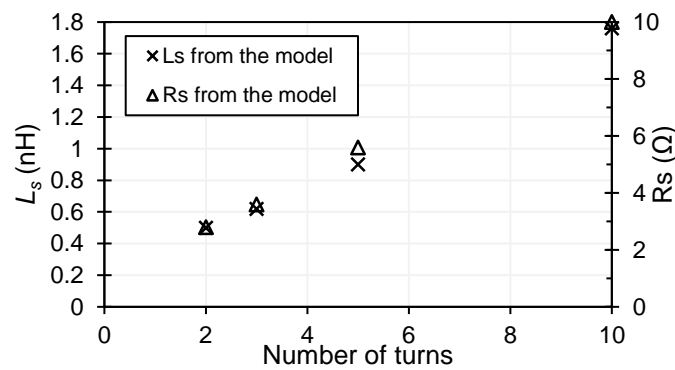
The values for the lumped elements used in the model for each 3-D inductance are given in Table 5.

Table 5 – Parameters for the inductor model.

Parameter	2 turns	3 turns	5 turns	10 turns
R_p (k Ω)	25	10	5.5	5.5
R_s (Ω)	2.8	3.6	5.6	10
R_g (Ω)	12	14	12.5	9
L_s (nH)	0.5	0.62	0.9	1.76
L_g (nH)	-0.055	-0.074	-0.12	-0.255
C_p (fF)	1.14	2.3	3.67	4.8
C_g (fF)	11.5	13.1	20.6	30.5

From Table 5, it can be seen that as the number of turns increases, the series inductance L_s , the series resistance R_s , the parallel capacitance C_p and the ground capacitance C_g increases, whereas the inductance L_g decreases with the number of turns. The two main elements of the model, L_s and R_s , increase almost linearly with the number of turns, in a similar manner as shown in Figure 47.

Figure 47 – The parameters L_s and R_s used in the model versus the number of turns for each inductor.



2.3.6 Comparison to the state-of-the-art

The results obtained for the 3-D inductor solenoid with nanowire-vias are compared to the literature in Table 2. The figure of merit (FoM) given by the ratio of the inductance and its area was used to express the trade-off between electrical

performance and footprint. The highest FoM is obtained by 3-D inductors fabricated in the BEOL of a CMOS technology [38] although their Q -factor is the lowest among the ones presented in Table 2. The technology proposed in the present work shows a good trade-off between footprint and Q -factor, comparable to that obtained with MEMS technology on glass [31]. The proposed technology also exhibits high SRF. The high SRF is due to the small overall size of the whole structure, including the nanowire-vias, and low parasitic capacitance between solenoid turns. The solenoid type inductors reported in [36], that uses the same AAO membrane, although using a thicker membrane, exhibits a lower FoM than the inductors proposed and work at lower frequencies.

Table 6 – Comparison of reported 3-D inductors in high frequency.

Ref.	Tech.	Inductor Type	L (nH)	# turns	Max Q	SRF (GHz)	Area (mm ²)	FoM (nH/mm ²)
[33]	Glass	Through substrate	4.4 / 1.8	4.5 / 1.5	75 ~ 85@3 GHz	> 3	~0.65 / ~0.5	~6.8 / ~3.6
[34]	HR Si	Through substrate	4.6 / 0.8	5 / 1	10.5@0.4 GHz / 18.8@3 GHz	5.8 / 22.4	0.349 / 0.126	13.2 / 6.3
[35]	LTCC	Through substrate	1.9	2.5	36@5.9 GHz	> 5.9	0.09	21
[38]	CMOS	Through BEOL	1.5 / 0.6	20 / 10	1.75@6.5 GHz / 4.9@11 GHz	> 20	0.013	115 / 46
[24]	HR Si	Through substrate	11.5 / 1.4	8 / 1	36# / 134#	5.91 / >10	~3.2 / ~1	~3.6 / ~1
[39]	Glass	Planar	1.4	1	55@20 GHz	> 20	~ 0.8	1.75
[31]	Glass	Over IC / solenoid	11.2 / 2.7	80 / 20	12 / 24@6 GHz	> 10	~ 4.6 / ~ 1.1	~ 2.6 / ~ 2.45
[36]	100- μ m thick AAO with solid vias	Through substrate	0.91 / 2.02	2 / 5	41 / 18 @6.9GHz	> 20 / 20	0.09 / 0.15	10 / 13.5
This work	50-μm thick AAO with nanowire- vias	Through substrate	1.7 / 0.5	10 / 2	8@16 GHz / 35@40 GHz	30 / 91	0.07 / 0.023	24 / 21

No frequency information

These results show that the nanowire-filled membrane can be a very good candidate for the development of a full low-cost and high-performance mm-wave interposer embedding 3-D inductors.

2.3.7 Summary

Novel 3-D solenoid inductors using nanowire-vias have been presented. They were fabricated on a 50- μ m thick AAO membrane. The first fabricated structures

indicated a problem in the fabrication process, which was addressed by removing the oxide mask layer. After that, the SRF of the inductors ranged from 31 GHz to 98 GHz for the 10-turns inductor and 2-turns inductor, respectively. A “T” model with lumped elements was proposed for the structures. This allows the designer to better understand the way that each parameter influences the electrical behaviour of the 3-D inductors. The fabrication used a simple low-cost technology based on 50- μm -thick AAO membranes and copper nanowires. This is a flexible technology for the designer, as the nanowire-vias size and pitch are not limited by the technology. With the presented results, a Q-factor of 35 at 40 GHz is achieved for the 2-turns inductor with a small area of 0.03 mm². The presented model is intended to help the designer use the inductor as a library, simulating faster with the lumped model than with a full 3-D EM simulation tool, and to achieve inductors with high Q-factors at a desired frequency.

2.4 Chapter summary

Vias on the MnM substrate were presented, with the use of the membrane natural nanopores to produce nanowire-vias. As shown, these vias can have a lower size and pitch as its fabrication is not dependent on drilling the substrate. Its performance as a transition were assessed using a simple lumped element model, being state-of-the-art when comparing to technologies such as Si, HR-Si, glass and LCP, with a mean insertion loss of about 0.23 dB at 110 GHz.

A 3-D solenoid inductor on the MnM substrate was also presented, as a first circuit device using the nanowire-vias, showing its flexibility as a via and the possibilities of the MnM substrate for easily creating passive devices using both substrate surfaces and without pitch limitation between vias. The 3-D inductors were conceived, fabricated, measured and modeled. Those inductors presented SRF ranging from 30 GHz to 98 GHz, for the 10-turns inductor and 2-turns inductor, respectively. The proposed “T” lumped elements electrical model can be related to the physical layout, and as such, be used to improve its performance, besides being used as a quick simulation tool.

3 SLOW-WAVE MICROSTRIP TRANSMISSION LINES

3.1 Introduction

On a good interposer, the redistribution layer must have high quality electrical paths, so that an electrical signal between different parts of the interposer does not suffer from integrity problems. For an mm-wave interposer, this means having high quality transmission lines. Traditional transmission lines (Tlines), such as microstrip and CPW, are dependent on the interposer material and metallization for achieving a good quality factor. As the Tline losses are proportional to its physical length, if the Tline electrical length can be increased for the same physical length then it would have lower losses and a higher quality factor. This is achieved using Tlines with a slow-wave effect that increases the electrical length for the same physical Tline length, achieving a higher quality factor than the traditional Tlines counterparts and diminishing the physical space used, thus enabling miniaturization and diminishing costs.

Slow-wave microstrip lines (SMS) have been demonstrated from microwave to mm-wave frequencies in different technologies, such as integrated lines on silicon [40]–[43], and PCB [44]; and different configurations, patterned ground shield transmission lines [42], [44], transmission lines loaded with distributed elements [43], using transmission lines with different characteristic impedances to create the slow-wave effect [41], among others. Such transmission lines allow reducing the size of the circuits by artificially producing high dielectric constants even if the dielectric constant of the substrate is low.

The concept of SMS lines has been also presented using blind metallic vias connected to the ground plane in two different technologies depending on the frequency range, a standard multi-layered printed circuit board (PCB) technology dedicated to RF applications [45], [46], and the substrate analyzed in this work, the metallic nanowire-filled membrane (MnM), dedicated to mm-waves [10], [11]. In both cases, the slow-wave effect is achieved by using a classical microstrip line and adding one or more layers between its dielectric layer and ground plane for placing grounded blind metallic vias/nanowires. In such a way, electric and magnetic fields are separated in the volume between the top of the vias and the ground plane. In this volume, the

electric field is almost equal to zero whereas the magnetic field is almost the same as for classical microstrip lines.

SMS lines using blind vias in PCB and MnM technologies are a good solution for the miniaturization of transmission lines as they are simple to design, fabricate, integrate and occupy less space than other slow-wave transmission lines such as slow-wave coplanar waveguide for which an equivalent electrical model was also recently proposed [47], [48]. However, until now, a comprehensive complete distributed transmission line model for these SMS lines was not reported in the literature, to the best knowledge of the author. Full 3-D electromagnetic simulation has a high computational cost for these SMS lines, being almost unapproachable to simulate since there are about 95 nanowires per square micrometer for the MnM substrate, combined with the high aspect ratio of each nanowire, generating a very dense mesh. This is less true when dealing with PCB technology; however, it is not conceivable that a designer spends too much time simply to achieve transmission lines design. Hence, to help designers use the concept of SMS lines using blind via holes, this work presents an equivalent electrical model based on a classical transmission line *RLGC* model, adding an inductance and resistance to the ground plane to model the vias/nanowires and the magnetic coupling between them. A particular effort was carried out to model the magnetic coupling between the vias, since it has a significant impact on the validity of the model.

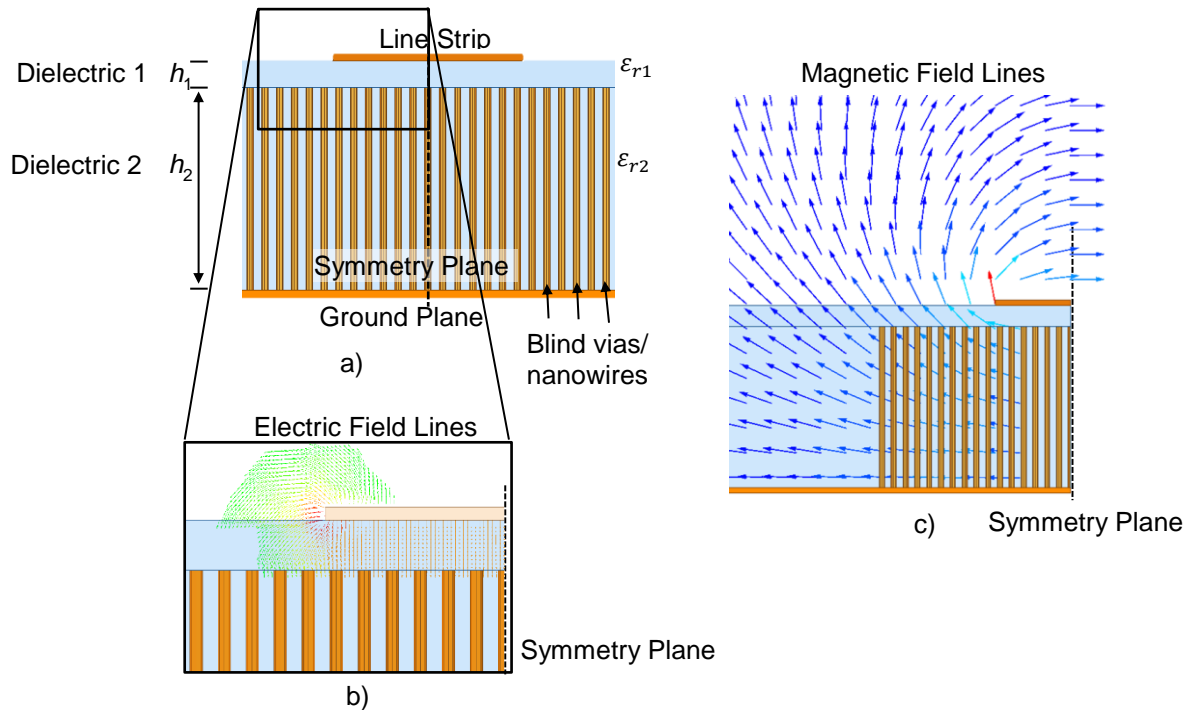
The chapter is organized as follows. First, the slow-wave effect of the SMS lines is presented in section 3.2 with its topology. After that the physics-based model of the SMS lines is proposed in section 3.3 and validated with experimental results in section 3.4. A discussion on the results is carried out in section 3.5 and this chapter is concluded in section 3.6.

3.2 Slow-wave principle

The slow-wave concept based on the use of blind via holes in microstrip lines is briefly presented here. More details were already given in [10], [11], [45], [46]. The slow-wave microstrip using blind via holes are generally composed of two main dielectric layers: the upper layer with thickness h_1 , and the bottom layer with thickness

h_2 , filled by a forest of metallic blind via holes, as shown in Figure 48 a). The patterns of the electrical and magnetic fields are shown in Figure 48 b) and c). The slow-wave effect is achieved as the electric field is confined in the upper dielectric layer whereas the magnetic field flows through the entire volume formed by h_1 and h_2 , as in classical microstrip lines. From an electrical point of view, this leads to an increased linear capacitance C while the linear inductance L is almost the same as compared to classical microstrip lines, thus diminishing the phase velocity expressed as $v_\varphi = 1/\sqrt{LC}$ and increasing the effective dielectric constant expressed as $\varepsilon_{\text{reff}} = c_0\sqrt{LC}$, with c_0 the speed of light in vacuum.

Figure 48 – In a), overview of the analyzed slow-wave microstrip line (SMS). In b) and c), visualization of the electrical and magnetic field lines, respectively, in a transversal section. Only half of the SMS line was considered, due to properties of symmetries.

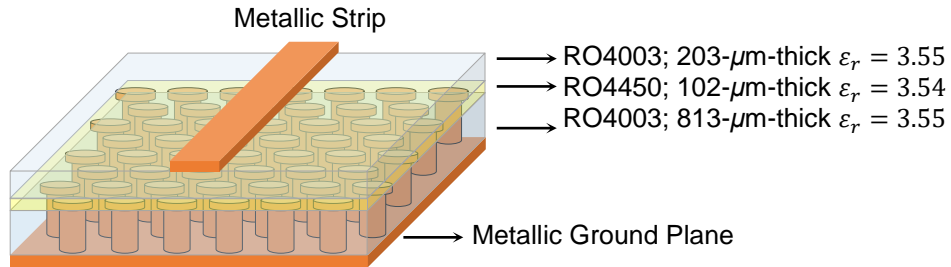


In this section, SMS lines on the two technologies analyzed, PCB and MnM, are presented in detail.

Here, two technologies are analyzed side-by-side; PCB SMS with blind vias and MnM SMS with blind nanowires, since the slow-wave effect described in Figure 48 applies to both technologies. The difference between them is the size of the structures, the blind vias, the line, that relates to the frequency band where the Tlines can operate. The bigger PCB SMS lines work in microwave frequencies, while the smaller MnM

SMS lines in mm-wave frequencies. The multi-layered PCB technology for SMS lines is presented in Figure 49.

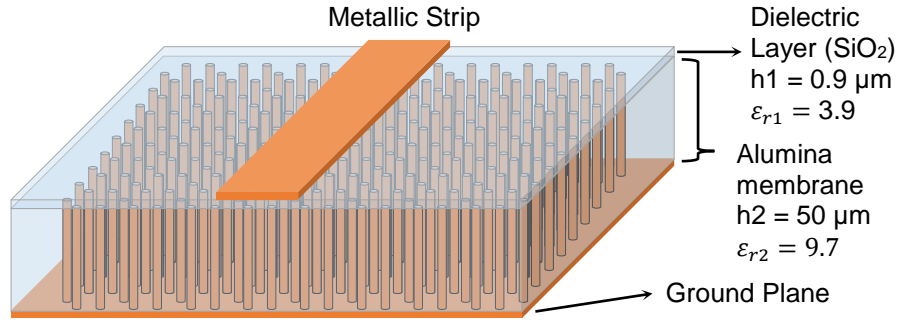
Figure 49 – Schematic of a slow-wave microstrip line in PCB technology.



The substrate is composed of a 203- μm -thick top and 813- μm -thick bottom Rogers RO4003 substrate layers, bonded using a 102- μm -thick RO4450 substrate (middle layer). Blind vias are located inside the bottom layer, and due to technology constraints, a 35- μm -thick metal pad is formed above the vias. For the calculi to be realized in the next sections, the height of the upper dielectric layer related to h_1 , shown in Figure 48 a) is considered between the bottom of the metallic strip and the top of the vias pads, thus making the height h_1 equal to 270 μm (203+102-35). In the same way, the height of the bottom dielectric layer related to h_2 is considered as the layer where the blind vias and the pads are, making h_2 equal to 848 μm (813+35). Since the relative dielectric constant of the upper and lower Rogers 4003 dielectric layers and the middle Rogers 4450 dielectric layer are very close ($\epsilon_r = 3.55$ and $\epsilon_r = 3.54$, respectively), $\epsilon_{r1} = 3.55$ was considered for the upper dielectric layer.

The higher frequency SMS line on the MnM technology is presented in Figure 50. It is made of two dielectric layers, as described in chapter 1 and also detailed in [10], [11]. The bottom layer is made of a 50- μm -thick InRedox Anodic Aluminum Oxide (AAO) membrane where blind metallic nanowires are inside the nanopores and connected to the ground plane. The top dielectric layer is a 0.9- μm -thick silicon dioxide dielectric layer over the membrane. The microstrip line is made on top of those two substrates stack, and the ground plane is made on the bottom, respectively. In practical realizations, the membrane could have a thickness between 50 μm and 100 μm , and the dielectric layer between 0.5 μm to 3 μm , depending on the slow-wave factor and characteristic impedances range that are targeted.

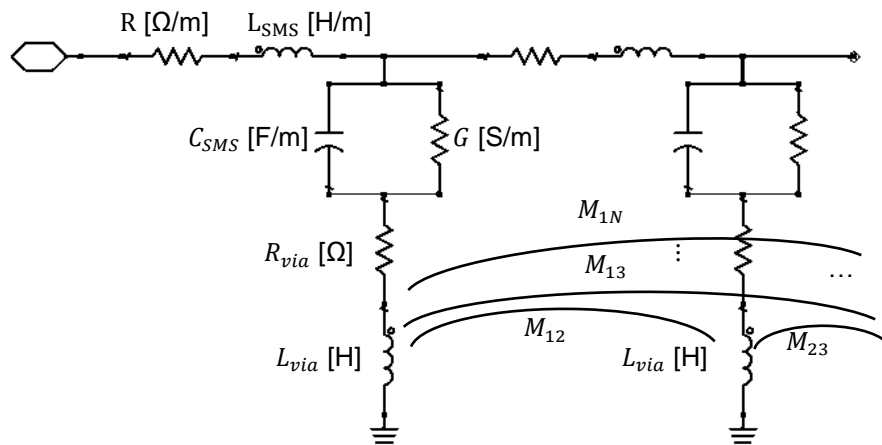
Figure 50 – Schematic of a slow-wave microstrip line in MnM technology.



3.3 Electrical model

The distributed model for the SMS lines is based on the topology of the electrical model initially proposed in [11]. The proposed model is shown in Figure 51 for two sections of a SMS line. $RL_{SMS}GC_{SMS}$ are the distributed elements of a classical microstrip line model. The inductance L_{via} and the resistance R_{via} model a group of blind nanowire or via. All the L_{via} in each section are mutually coupled between each other by a mutual inductance M_{ij} , with i and j the different sections of the model.

Figure 51 – Topology of the distributed model of the SMS lines.



It is important to note that, beyond the fact that R_{via} , L_{via} and M_{ij} were added to the classical $RLGC$ model, the calculation of the linear capacitance C_{SMS} and the linear inductance L_{SMS} of the SMS lines differs from classical microstrip lines. From the simulation in Figure 48 b), it is possible to verify that the electric field is present on the top dielectric layer with some portion that penetrates the bottom dielectric layer in

between the vias. This penetration depends on the via pitch and affects directly C_{SMS} . The linear inductance L_{SMS} is slightly affected by the metallic blind vias/nanowires, changing the way it is calculated.

The first thing to be defined for the present analysis is the area density of vias that will be considered for the C_{SMS} and L_{SMS} calculations, in each technology. For PCB technology, the via pads play an important role in the slow-wave effect because they increase the metal density from the electrical field point of view, increasing C_{SMS} . Their density dst_{pad} is expressed as:

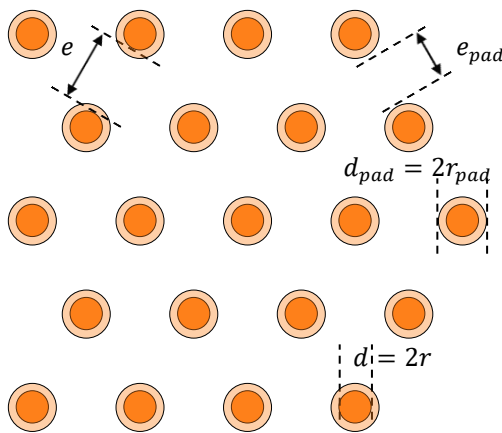
$$dst_{pad} = \frac{2\pi}{\sqrt{3}} \frac{r_{pad}^2}{(2r_{pad} + e_{pad})^2} \quad (15)$$

where r_{pad} is the radius of the pads, and e_{pad} is the pad pitch, as shown in Figure 52. The area density of vias can be defined in the same way as for eq. (15) as:

$$dst_{via} = \frac{2\pi}{\sqrt{3}} \frac{r^2}{(2r + e)^2} \quad (16)$$

where r is the radius of each via beneath the pad and e is the via pitch, as shown in Figure 52. For MnM technology, as there are no pads on top of the vias, $dst_{pad} = dst_{via}$.

Figure 52 – Schematic top view of the metallic vias organization with pads. d/d_{pad} are the vias/pads diameters, r/r_{pad} their radii, e/e_{pad} their pitches, respectively.



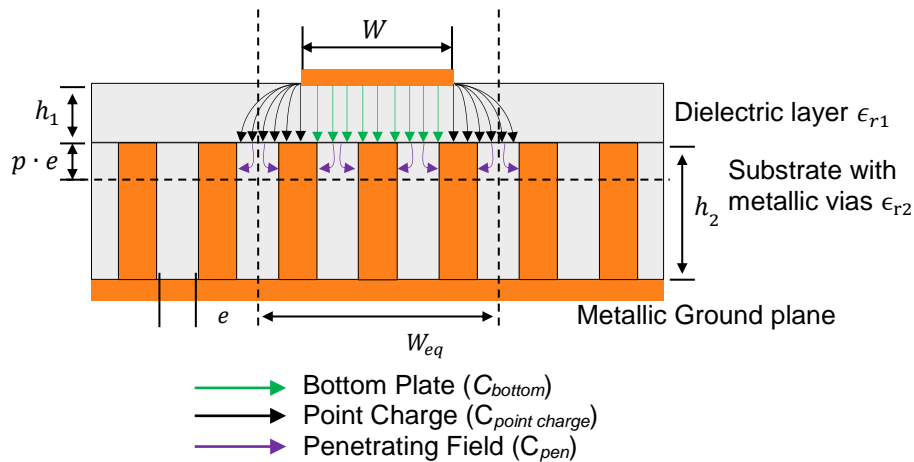
3.3.1 Linear capacitance C_{SMS}

The electrical field pattern in SMS lines with width W is shown in the transverse view in Figure 53. The upper dielectric layer of SMS lines is generally thin, in comparison to W , to increase the slow-wave effect, thus leading to a ratio $W/h_1 > 1$. Hence, the electric field lines are highly concentrated in this dielectric layer generating the most important part of the capacitance, and so the capacitance generated by the electric field that passes through the air (air fringing field) can be neglected. On the contrary, the fringing field passing through the substrate is not neglected. The electric field lines are mainly concentrated in the dielectric layer between the strip and the top of the blind metallic vias. They are separated in regions, called Bottom Plate and Point Charge Fields. Only few electric field lines penetrate between the vias, which is called Penetrating Field.

A capacitance can be associated to each region of electrical field lines, C_{Bottom} for Bottom Plate, $C_{PointCharge}$ for Point Charge and C_{Pen} for Penetrating Field, as shown in Figure 53. The sum of C_{Bottom} and two times $C_{PointCharge}$, which are in parallel, is called C :

$$C = C_{Bottom} + 2 * C_{Point Charge} \quad (17)$$

Figure 53 – Electric field lines representation for capacitance calculus for the SMS lines. The electric field lines that give the main part of the linear capacitance are included in an equivalent width W_{eq} .

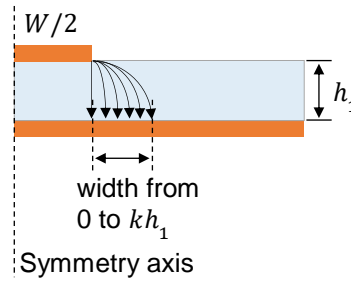


The modeling method proposed in [49] was used for the calculation of C , as follows:

The capacitance C_{Bottom} can be simply calculated as the parallel plate capacitance with width W between the strip and the top of the nanowires or via pads, separated by h_1 .

The capacitance $C_{PointCharge}$ is calculated using an elliptical path in a confined region determined by the thickness of the substrate h_1 , as shown in Figure 54 using eq. (18).

Figure 54 – Field lines considered when calculating the $C_{PointCharge}$ capacitance. The electrical field lines have an elliptical path between the bottom corner of the strip and the ground plane with ellipsis semi-major axis h_1 .



The expression of $C_{Point Charge}$ is given as [49]:

$$C_{Point Charge}(k) = \epsilon_{r1}\epsilon_0 \int \frac{width}{distance} = \epsilon_{r1}\epsilon_0 \int_0^{kh_1} \frac{dx}{h_1 * E \left[1 - \left(\frac{x}{h_1} \right)^2 \right]} \quad (18)$$

In eq. (18), k is a ratio that is discussed later. The component dx represents the width where the integral is being calculated, with integral limits from 0 to kh_1 . The distance between the width point (from 0 to h_1) to the corner of the strip is given by an ellipsoid path, with $E[1 - (x/h_1)^2]$ the complete elliptic integral of the second kind, i.e., the ellipse perimeter in one quadrant, ellipse with semi-major axis h_1 and semi-minor axis dx , $1 - (x/h_1)^2$ being the square of the eccentricity of the ellipse.

On the other hand, C can also be calculated as the capacitance of a classical microstrip line with only the upper dielectric layer and a ground plane at the top of the nanowires/vias pads, as presented in [50].

The capacitance C obtained by the calculus based on (18) considering $k = 1$, for the Point Charge, was compared to the capacitance calculated in [50] for classical microstrip lines. In [50] the characteristic impedance $Z_{microstrip}$ and effective relative

dielectric constant ϵ_{reff} for a classical microstrip line are first calculated, and $C_{microstrip}$ is derived from these two parameters, as:

$$C_{microstrip} = \frac{\sqrt{\epsilon_{reff}}}{c_0 * Z_{microstrip}} \quad (19)$$

where c_0 is the speed of light in vacuum.

It was concluded that the proposed capacitance C was higher than $C_{microstrip}$. As C_{Bottom} is easily modeled, the discrepancy should come from $C_{PointCharge}$. To correct the overestimation of $C_{PointCharge}$, C was compared with $C_{microstrip}$ and k was chosen between 0 and 1 so that C equals $C_{microstrip}$. In this sense, the capacitance C is redefined from (17) to:

$$C(k) = C_{Bottom} + 2 * C_{Point Charge}(k) \quad (20)$$

Once $C(k)$ is correctly modeled, the capacitance associated to the penetrating field lines C_{pen} was modeled using a parallel plate capacitance model with width W_{eq} . This width W_{eq} demarks the width at the top of the nanowires/via pads where the electrical field is more important (see Figure 53), and is defined as:

$$W_{eq} = W + 2 * k * h_1 \quad (21)$$

Then the expression used for C_{pen} is given by:

$$C_{Pen} = \frac{\epsilon_{r1} * \epsilon_0 * W_{eq} * (1 - dst_{pad})}{p * e} \quad (22)$$

In (22), the term $(1 - dst_{pad})$ represents an area-correcting factor, related to where there are electric field lines penetrating between the vias (see Figure 53). It is obvious that the electrical field lines penetrating between the vias are not those of a parallel plate capacitor, but the parallel plate capacitor expression can still be used considering a parallel plate length definition that takes into account the average of the length of the field lines. This equivalent length used for the parallel plate formula in (22) was defined as $p.e$. It comes from the fact that the penetration is proportional to the via pitch e , being p a penetration factor extracted from measurement results.

Once the expressions of $C(k)$ and C_{pen} have been established, the linear capacitance of the SMS line C_{SMS} can be calculated as proposed in (23).

$$C_{SMS} = dst_{pads} * C(k) + \frac{1}{\frac{1}{(1 - dst_{pads}) * C(k)} + \frac{1}{C_{pen}}} \quad (23)$$

In (23), the first term is related to the capacitance modeling the electric field lines going to the top of the metallic vias, thus the nanowires/vias pads density dst_{pads} was multiplied by the linear capacitance $C(k)$. The second term is related to the capacitance where the field lines penetrate between the vias. This term correspond to two series capacitances, the one modeling the electrical field from the strip to the top of the vias, i.e., $(1 - dst_{pads}) * C(k)$, and the one modeling the electrical field penetrating between the vias C_{pen} .

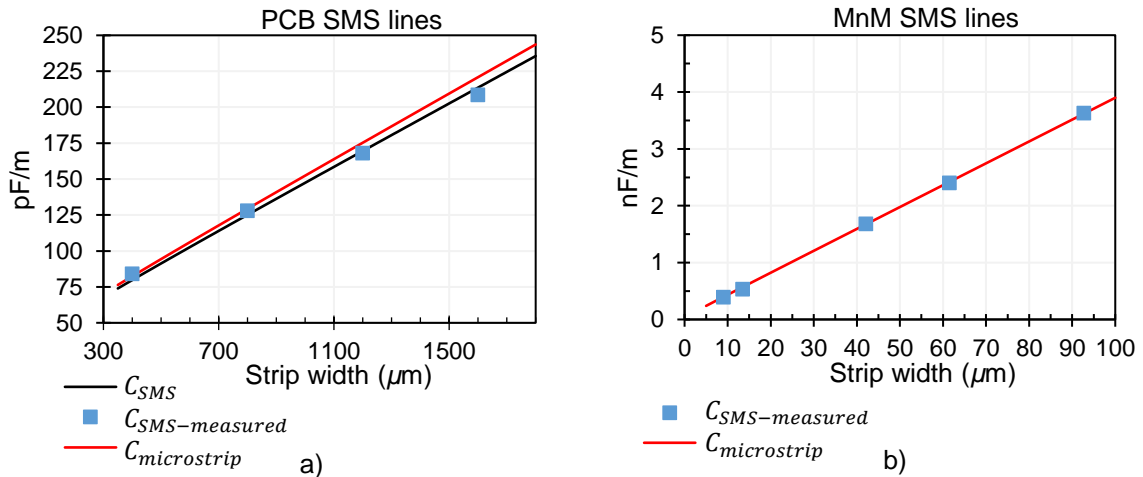
C_{SMS} from eq. (23) was compared to $C_{microstrip}$ from eq. (19) and to the capacitance extracted from measurement results. SMS lines with different widths were fabricated in both technologies, PCB and MnM, as detailed in sections 3.4.1 and 3.4.2, to validate the proposed model. The experimental capacitance $C_{SMS-measured}$ was extracted at low frequency where the capacitance is near to a quasi-static state to avoid any dispersion effect due to the vias periodicity. From measurements, $C_{SMS-measured}$ was calculated as:

$$C_{SMS-measured} = \frac{\beta}{Re\{Z\} * 2\pi f} \quad (24)$$

where f is the frequency, β is the phase constant ($\beta = Im\left\{\frac{\text{acosh } A}{\text{line length}}\right\}$), Z is the SMS line characteristic impedance calculated as $Z = \sqrt{B/C}$, and A, B, C are the elements of the ABCD matrix derived from measured S-parameters. Details concerning calibration and de-embedding are given in section 3.4.1 for PCB SMS lines and section 3.4.2 for MnM technology SMS lines, respectively. The comparison between the proposed C_{SMS} , $C_{microstrip}$, and $C_{SMS-measured}$ is shown in Figure 55. The penetration factor p was adjusted for each technology to the capacitance extracted from S-parameters measurements in lower frequencies. For PCB technology, p was fixed to 0.1. Since it was verified that MnM lines do not present significant penetrating field due

to the very high number of nanowires per area, C_{pen} can be neglected, thus meaning the capacitance is the same as a classical microstrip line having a substrate height equal to h_1 . The agreement between the three capacitances is very good, for a wide range of strip widths.

Figure 55 – Proposed linear capacitance for PCB technology a) and MnM technology b), respectively. Comparison between $C_{SMS-measured}$ extracted from measurements, $C_{microstrip}$ calculated from [50] and proposed capacitance C_{SMS} .



From Figure 55 it is possible to verify that in PCB technology, the proposed linear capacitance C_{SMS} is different from the one calculated from [50] in the way that it takes into account the penetrating electric field between pads and vias. This difference influences the characteristic impedance and phase constant β of the SMS lines, thus justifying this capacitance modelling.

3.3.2 SMS line inductance L_{SMS}

The model proposed for the linear SMS line inductance L_{SMS} considers the magnetic field lines that pass throughout the substrate with metallic vias, which are slightly different from those in a classical microstrip line. In a classical microstrip line, the magnetic field flows freely through the dielectric right below the Tline strip down to the ground plane, whereas in the SMS lines the magnetic field is slightly disturbed by the vias. The behavior of the magnetic field is also different between PCB and MnM technologies. In PCB technology, the magnetic field lines pass around the metallic vias since the diameter of the vias is larger than the skin depth at microwave frequencies, considered in practical cases. On the contrary, some magnetic field lines pass through the nanowires in the MnM technology, as their dimensions are in the nanometer scale,

much smaller than the skin depth at mm-waves. Consequently, the modeling method for each technology is described separately.

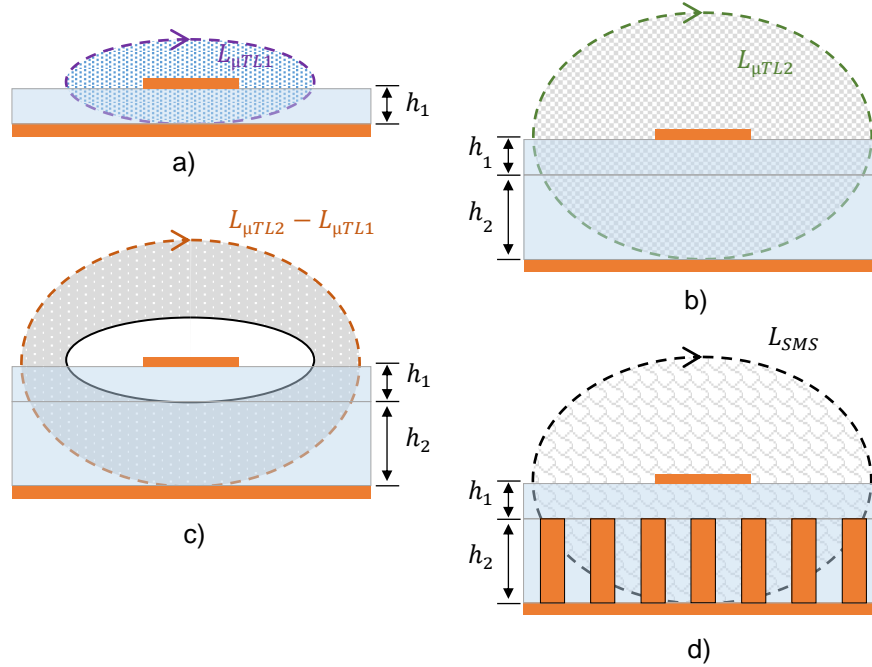
3.3.2.1 PCB technology

The proposed formula for the linear inductance is given in (25), where $L_{\mu TL1}$ is the inductance of a microstrip line with a dielectric layer thickness h_1 as shown in Figure 56 a), and $L_{\mu TL2}$ is the inductance of a microstrip line with a dielectric layer thickness $h_1 + h_2$, as shown in Figure 56 b), respectively.

$$L_{SMS} = (L_{\mu TL2} - L_{\mu TL1})(1 - dst_{vias} - \eta) + L_{\mu TL1} \quad (25)$$

The magnetic field that flows only through the part of the substrate with metallic vias is calculated by the difference $L_{\mu TL2} - L_{\mu TL1}$, as illustrated in Figure 56 c), multiplied by a weighting term $(1 - dst_{vias} - \eta)$, related to the area of the substrate without the metallic vias, where the magnetic field can pass. η represents a shape factor related to the shape of the magnetic field lines when passing around the metallic vias. This factor can be extracted either from experimental or simulated results, as will be shown below. The total inductance L_{SMS} presented in (25) is then calculated by the sum of the inductance $L_{\mu TL1}$ and the term described above.

Figure 56 – Magnetic field and corresponding inductance for a) microstrip with substrate thickness h_1 , b) microstrip with substrate thickness $h_1 + h_2$. In c) is illustrated the flux difference between a) and b), and in d) is illustrated the magnetic flux of the SMS line with metallic vias and total substrate thickness $h_1 + h_2$.



The proposed expression for the inductance L_{SMS} was compared to the inductance extracted from measurement results of the fabricated PCB SMS lines ($L_{SMS-measured}$) and to the inductance of a classical microstrip line with substrate thickness $h_1 + h_2$ ($L_{microstrip}$), respectively. $L_{microstrip}$ was calculated from [50] with thickness $h_1 + h_2$, as:

$$L_{microstrip} = Z_{microstrip} \frac{\sqrt{\epsilon_{eff}}}{c_0} \quad (26)$$

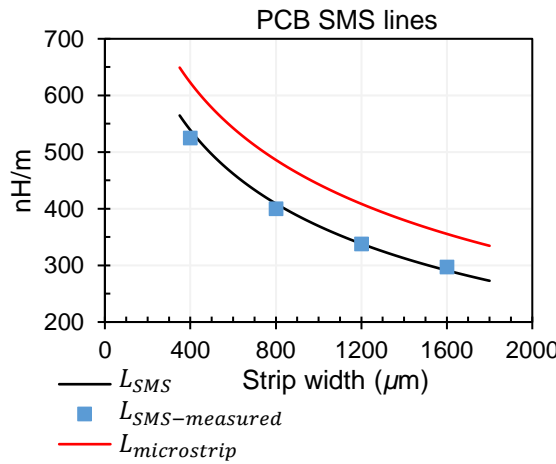
The inductance $L_{SMS-measured}$ was extracted at low frequency to avoid any dispersion issue that could come from the inductive behavior of the vias, given by:

$$L_{SMS-measured} = Re\{Z\} \frac{\beta}{2\pi f} \quad (27)$$

The comparison between L_{SMS} , $L_{microstrip}$ and $L_{SMS-measured}$ is given in Figure 57. The same shape factor η equal to 0.08 was used for the calculus of the inductance L_{SMS} of all SMS lines, so that the proposed model fits with measurement results. From Figure 57, it can be seen that the fit between the proposed expression and measurement results is very good over a wide range of strip widths. Hence, once

estimated, the shape factor η has not to be modified, regardless of the strip width (and consequently the characteristic impedance) of the SMS lines. Thus, the proposed modeling can be considered as robust. On the contrary, the inductance $L_{microstrip}$ extracted from [50] overestimates the actual inductance, thus justifying the modeling efforts carried out in this work.

Figure 57 – Comparison between the inductance of classical microstrip lines $L_{microstrip}$ (red line), the proposed inductance L_{SMS} (black line), and the inductance extracted from measurements of fabricated SMS lines in PCB technology $L_{SMS-measured}$ (blue squares).



3.3.2.2 MnM technology

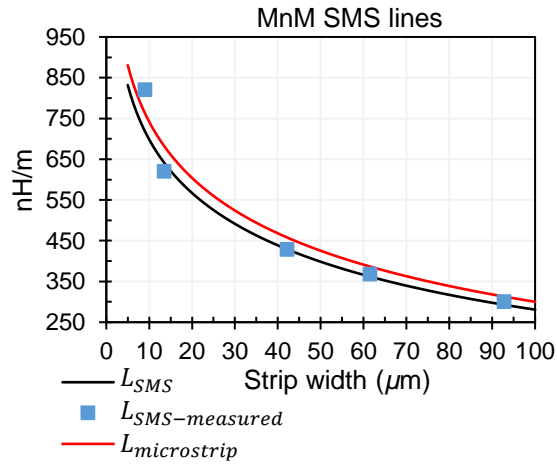
For the SMS lines on MnM technology, the linear inductance can be calculated by using a simplified version of eq. (25). As the magnetic field passes through the nanowires that exhibit a diameter smaller than the skin depth at mm-wave frequencies, the term dst_{vias} can be neglected, resulting in the expression given in eq. (28):

$$L_{SMS} = (L_{\mu TL2} - L_{\mu TL1})(1 - \eta) + L_{\mu TL1} \quad (28)$$

Even though some magnetic field passes through the nanowires, the latter still have some influence on the magnetic field, thus the factor η still needs to be used. As for PCB technology, in Figure 58 the linear inductance L_{SMS} calculated from the proposed model is compared to the inductance extracted from measurements of fabricated SMS lines, $L_{SMS-measured}$, and to the inductance of classical microstrip lines, $L_{microstrip}$ calculated from [50]. An empirical factor η equal to 0.067 was used for all SMS lines. As could be expected, the difference between the inductance derived for a classical microstrip line and that of the MnM SMS line is much smaller as compared to

the case of PCB technology, since the magnetic field is much less perturbed. However, the used of the shape factor η still leads to a better estimation of the linear inductance, thus validating again the efforts carried out in the presented study.

Figure 58 – SMS line linear inductance L_{SMS} calculated from proposed model for the metallic-nanowire-filled membrane technology (black line), compared to the inductance $L_{microstrip}$ of a classical microstrip line with substrate height $h_1 + h_2$ extracted from [50] (red line), and the inductance $L_{SMS-measured}$ extracted from measurements (blue squares).

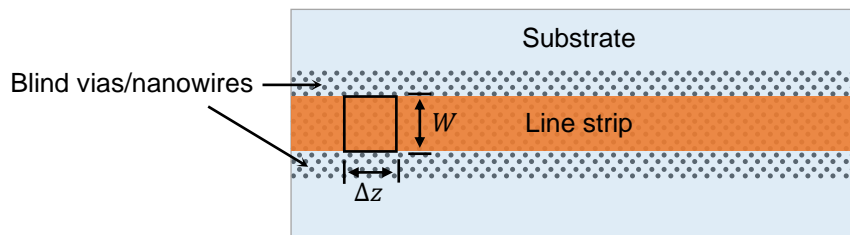


It has also to be noted that for MnM technology, since the upper SiO_2 layer is usually much smaller than the membrane height, that the shape factor η can be used for a wide range of substrate configuration using 50 μm thick membranes.

3.3.3 Metallic via inductance L_{via} and mutual M_{ij}

The expression of the inductance L_{via} of the metallic blind vias/nanowires under the line strip for a section of the model and the mutual inductance between sections M_{ij} are presented here. First, a rectangular region along the strip with size $W * \Delta z$ is defined to form a section of the model as shown in Figure 59.

Figure 59 – SMS line top view with the region with size $W * \Delta z$ for the calculi of M_{ij} .



The choice of Δz is discussed further in section 3.4. It is assumed that within this region, the current is the same in each via/nanowire. Having this region, N nanowires in the hexagonal configuration showed in Figure 52, with k and l being vias/nanowires within this region, the inductance can be calculated as proposed in eq. (9) from section 2.2.3.2 after calculation the self-inductance for each nanowire and their mutual, and building its \mathbf{L} matrix. The calculation is reproduced here in a different equivalent form as the one from eq. (9). Instead of a matrix form, a sum form is used as proposed in [27]:

$$L_{via}[H] = \frac{\sum_{k=1}^N \sum_{l=1}^N L_{M_{kl}}}{N^2} \quad (29)$$

$$L_{M_{kl}}[H] = \begin{cases} \frac{\mu_0}{2\pi} h_2 \left[\ln \left(\frac{h_2}{r} + \sqrt{\left(\frac{h_2}{r} \right)^2 + 1} \right) - \sqrt{\left(\frac{r}{h_2} \right)^2 + 1} + \frac{r}{h_2} + \frac{1}{4} \right], & \text{if } k = l \\ \frac{\mu_0}{2\pi} h_2 \left[\ln \left(\frac{h_2}{d_{kl}} + \sqrt{\left(\frac{h_2}{d_{kl}} \right)^2 + 1} \right) - \sqrt{\left(\frac{d_{kl}}{h_2} \right)^2 + 1} + \frac{d_{kl}}{h_2} \right], & \text{if } k \neq l \end{cases} \quad (30)$$

where d_{kl} is the nanowire k and nanowire l center-to-center distance and h_2 the nanowire/via height.

Then the mutual inductance between sections i and j , each one with N nanowires, is calculated in a similar manner, but with nanowires in different sections. Being m a via/nanowire in section i and n a via/nanowire in section j , the mutual inductance M_{ij} is calculated as [27]:

$$M_{ij}[H] = \frac{\sum_{m=1}^N \sum_{n=1}^N M'_{mn}}{N^2} \quad (31)$$

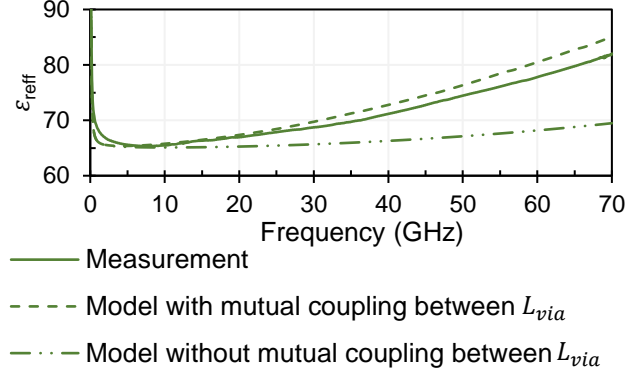
$$M'_{mn}[H] = \frac{\mu_0}{2\pi} h_2 \left[\ln \left(\frac{h_2}{d_{mn}} + \sqrt{\left(\frac{h_2}{d_{mn}} \right)^2 + 1} \right) - \sqrt{\left(\frac{d_{mn}}{h_2} \right)^2 + 1} + \frac{d_{mn}}{h_2} \right] \quad (32)$$

where d_{mn} is the nanowire m and nanowire n center-to-center distance.

The mutual couplings between sections in the model, shown in Figure 51, are necessary to better predict the behavior of the SMS lines, as shown in Figure 60. Without considering the mutual coupling between sections in the model, the model

cannot fully predict the dispersion occurring in the ϵ_{reff} extracted from measurements, whereas taking it into account, the tendency agrees better with the measured ϵ_{reff} .

Figure 60 – Comparison between the ϵ_{reff} extracted from measurements and extracted from the model with and without the mutual coupling between the inductance representing the nanowires.



3.3.4 Metallic vias resistance R_{via}

The linear via resistance R_{via} can be simply expressed by considering the number of vias of height h_2 over the equivalent width W_{eff} , defined in subsection 3.3.1, and model section length Δz , considering an equivalent conductance as $\sigma = dst_{pads} * \sigma_{copper}$ (as explained in section 2.2.3.2):

$$R_{via} [\Omega] = \frac{h_2}{\Delta z * w_{eff} * dst_{pads} * \sigma_{copper}} \quad (33)$$

3.3.5 Linear strip resistance R

The metal loss of the strip, represented in the model by the linear resistance R , is calculated from [51]:

$$R [\Omega/m] = (1 + j) \frac{R_{RF} \sqrt{f}}{1 - e^{-\frac{(1+j) R_{RF} \sqrt{f}}{R_{DC}}}} \quad (34)$$

with $R_{RF} = 0.5\sqrt{\pi\mu_0}/(W\sqrt{\sigma})$ and $R_{DC} = 1/(W * t * \sigma_{copper})$, W the strip width, t the strip thickness, σ the metal conductivity, f the frequency in Hz and μ_0 the permeability in free space.

3.3.6 Linear conductance G

The linear conductance G is classically defined as:

$$G [S/m] = \omega * C_{SW} * \tan \delta \quad (35)$$

In eq. (35), the loss tangent is related to the upper dielectric layer of the SMS line, as the electric field is confined in this layer.

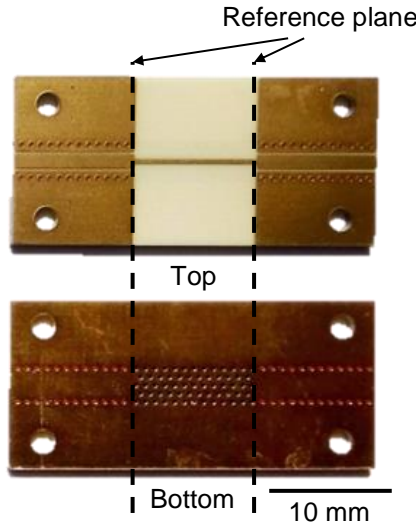
3.4 Model validation

Measurements of several SMS lines in both MnM and PCB technologies were carried out to validate the model proposed in section 3.3, through the extraction of the SMS line characteristic impedance Z_0 , attenuation constant α , and effective dielectric constant ϵ_{eff} , respectively.

The PCB SMS lines were measured with an Anritsu 3739D vector network analyzer (VNA). A thru-reflect-line (TRL) calibration was realized to place the reference planes after the feeding lines, as shown in Figure 61.

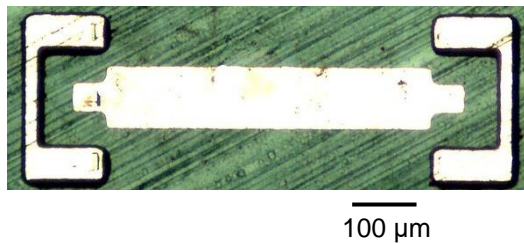
An example of fabricated PCB SMS line is given in Figure 61. It is 10-mm long and 400- μm wide, with grounded coplanar waveguide (GCPW) feeding lines. 35- μm -thick copper was used for all metals. The vias pitch is $e = 400 \mu\text{m}$ and their diameter is $d = 400 \mu\text{m}$, the pads pitch and diameter are $e_{\text{pad}} = 200 \mu\text{m}$ and $d_{\text{pad}} = 600 \mu\text{m}$, respectively, leading to a vias area density $\text{dst}_{\text{vias}} = 22.7\%$ and pads area density $\text{dst}_{\text{pads}} = 51.1 \%$. As shown in the bottom view in Figure 61, five rows of metallic vias were used for all the fabricated SMS lines in PCB technology. The rows of metallic vias were shifted to get a hexagonal configuration, with the center axis aligned with the strip center.

Figure 61 – Fabricated SMS line in PCB technology. Top and bottom views of a 10-mm long and 400- μm wide strip, with grounded CPW feeding lines.



For the MnM SMS lines, measurements were carried out with a Keysight N5227B VNA, using MPI Titan probes with 100- μm -pitch and load-reflect-reflect-line (LRRM) calibration. The MnM SMS lines were de-embedded using the two-line method proposed in [52]. In the same way, an example of fabricated MnM SMS line is given in Figure 61. It is 500- μm long, 92.75- μm wide, and 1.5- μm -thick with ground-signal-ground (GSG) pads for measurements. The ground pads are connected between each other on the metallic top layer and connected through nanowires to the bottom ground plane. The substrate employed is an AAO membrane from InRedox, with nanowire diameter $d = 40$ nm with pitch $e = 67$ nm. All metallic parts are in copper.

Figure 62 – Fabricated SMS line in MnM technology. Top view of a 500- μm long and 92.75- μm wide strip, with GSG measurement pads (with interconnected grounds).



The characteristic impedance Z_0 was obtained from measurements as [53]:

$$Z_0 = \frac{R + j\omega * L_{SMS-measured}}{\gamma_{measured}} \quad (36)$$

where $\gamma_{measured}$ is the propagation constant extracted from measured S-parameters.

Simulations were also carried out in HFSS/Ansys Electronics Desktop 2019 R2.1.

3.4.1 PCB technology results

The use of the proposed electrical model is based on three steps. First, the two factors, i.e. the penetration factor p for the linear capacitance C_{SMS} calculation and the shape factor η for the linear inductance L_{SMS} must be fixed. Then the length Δz of the elementary sections must be determined to calculate the mutual inductance between sections, and finally the elements of the electrical model can be calculated.

As discussed in sections 3.3.1 and 3.3.2, the two factors p and η can be extracted from either simulation or measurement results. Only one simulation for one strip width is necessary since the two factors do not vary over the strip width. p and η were fixed to 0.1 and 0.08, respectively. Although these values can be found by simulations, they were extracted directly from measurements.

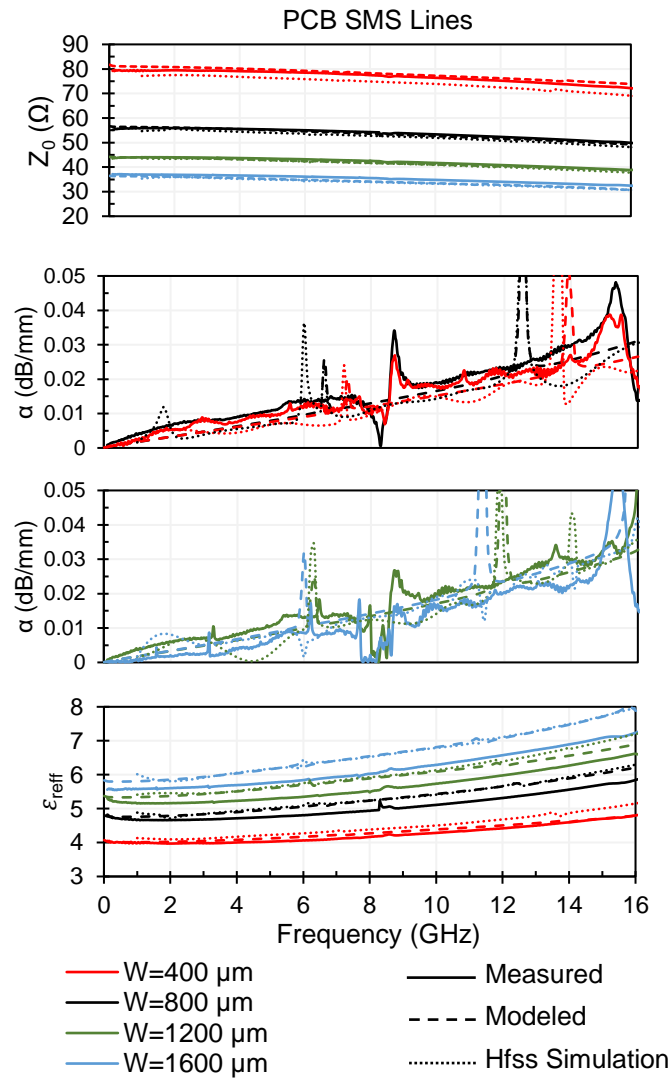
The length Δz , the length of each section of the electrical model, must be chosen much smaller than the minimum wavelength so that a steady state can be assumed inside an elementary section. In the practical examples considered in this work, the maximum operating frequency of the PCB SMS lines is around 10 GHz, before dispersion becomes significant due to the inductive behavior of the vias. $\lambda_g = 12.5$ mm at 10 GHz, by considering a maximum effective dielectric constant of 5.8 (Figure 63). To respect the condition $\frac{\Delta z}{\lambda_g} < 1/20$, which is a classical rule of thumb, Δz should be smaller than 625 μm . However, the periodicity of the blind vias is equal to 833 μm , which fixes $\Delta z = 833$ μm , so that at least one column of vias (vias in the vertical direction on Figure 61) is in the section. This leads to $\frac{\Delta z}{\lambda_g} = 1/15$, which is still acceptable. Therefore, in a 10-mm-long SMS line, there are 12 sections, each one 833- μm -long.

The inductance L_{via} for each section and the mutual inductance between sections M_{ij} were calculated depending on the width of the strip. For the SMS lines with 400- μm and 800- μm widths, only three rows of metallic vias were considered for

the metallic vias inductance L_{vias} since the farer vias catch negligible field, whereas for SMS lines with 1200- μm and 1600- μm widths all five rows were considered.

Figure 63 shows the parameters extracted from measurements, model, and HFSS simulations.

Figure 63 – Characteristic impedance Z_0 , attenuation constant α , relative effective dielectric constant ϵ_{reff} extracted from S-parameters model, simulation and measurements for the PCB technology.



The overall agreement between measurement and simulations results is very good, thus validating the proposed electrical model for SMS lines. Some peaks occur in the attenuation constant graphs. They are due to the access Tlines resonance.

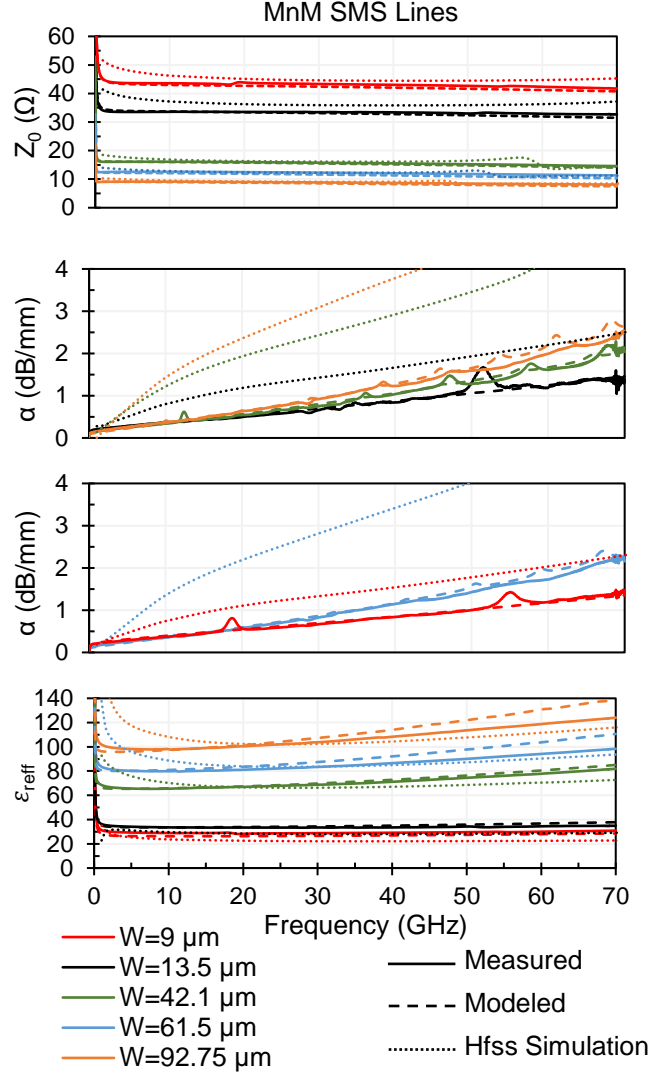
3.4.2 MnM technology results

Since for the MnM substrate used to fabricate the SMS lines would need a very high computational cost in simulating all the nanowires, simulations were carried out with the same via area density (dst_{via}) as the original membrane (about 12%) but with larger nanowires diameter and spacing.

For the MnM technology, only the shape factor for the linear inductance L_{SMS} has to be determined and for that it was used $\eta = 0.067$. 100 sections were considered to simulate 1.5-mm-long SMS lines, leading to $\Delta z = 15 \mu\text{m}$. This corresponds to the ratio $\frac{\Delta z}{\lambda_g} = 1/20$ at 100 GHz for the SMS line with the highest effective dielectric of 98 (Figure 64). Even though the measurements were carried out up to only 70 GHz, a higher frequency of 100 GHz was considered as these SMS lines can be used at higher frequencies.

Figure 64 shows the parameters extracted from measurements, model and HFSS simulations. The overall agreement between measurement and model is very good for the characteristic impedance and attenuation constant α . Concerning the relative effective dielectric constant ϵ_{reff} , the model can accurately predict its value at low frequencies up to around 20 GHz. Above 20 GHz, it slightly overestimates the dispersion. Based on these results, it can be considered that the proposed electrical model for SMS lines was validated also for the MnM technology. The HFSS simulations although made with higher nanowires diameter and spacing, could predict the characteristic impedance and relative effective dielectric constant, but overestimated the attenuation constant. This is probably due to eddy currents occurring in the “big” nanowires considered for simulations.

Figure 64 – Characteristic impedance Z_0 , attenuation constant α , relative effective dielectric constant ϵ_{reff} extracted from S-parameters model, simulation and measurements for the MnM technology.



3.5 Discussion

The agreement between the electrical model and measurement results can be considered as acceptable. The model can accurately predict the SMS lines dispersion with frequency, more visible when looking to the extracted ϵ_{reff} . Furthermore, the model overestimates the dispersion as the frequency dispersion for L_{SMS} , L_{via} and M_{ij} is not taken into account for the moment. Once taking into account the frequency dispersion for those three parameters, it is expected that its value decrease with frequency, leading to an ϵ_{reff} that increases less with frequency, agreeing better with

the measurements. As shown in Figure 60, the mutual coupling represented by M_{ij} , Figure 51, is extremely important to have an accurate prediction of ϵ_{reff} variation with frequency, being this coupling between sections of the model the main feature of the proposed electrical model.

3.6 Summary

We can conclude that the proposed electrical model can properly predict the behavior of the analyzed slow-wave microstrip lines with blind vias/nanowires. Although it does not take into account the skin effect, especially when the vias/nanowires self-inductance and mutual inductance for each elementary electrical model section are calculated, which have an influence on the result, using the values in DC leads to an acceptable agreement between simulation and measurement results. The proposed model is especially important as it can pretty well predict the dispersion of ϵ_{reff} in frequency. A next step to improve the model reliability would be to calculate L_{via} and M_{ij} versus frequency.

Finally, we have a comprehensive electrical model for the MnM SMS lines, which can be used as the redistribution layer of the MnM interposer depending on the necessities that can accurately predict the SMS line behavior and be used as a design tool.

4 CONCLUSION

From the developments presented in this work, we now have a fully functional new interposer for mm-wave frequencies. The MnM interposer has as demonstrated redistribution layer with high-performance slow-wave transmission lines and nanowire-vias. With those, passive circuits can now be designed. For achieving those goals, the fabrication process was improved, the membrane without nanowires was electrically characterized, nanowire-vias transitions were developed, the equivalent electrical conductance of a nanowire-via was derived, 3-D solenoid inductors using nanowires were analyzed and an electrical model for the slow-wave transmission lines on the substrate was proposed.

The fabrication process was improved, leading to the possibility of having more accuracy on the strip resolution, nanowires growth only in specific regions of the membrane, leading to a higher yield of success of circuits in each fabrication run.

The membrane with air-filled nanopores was characterized with two different methods, open-ended stubs and using a filter. The result is that up to 95 GHz, the membrane exhibits consistent electrical characteristics and beyond this frequency the characteristics change with the frequency and it is necessary further characterization for devices at higher frequencies.

Nanowire-vias transitions were designed, fabricated, measured and analyzed. A simple model for the transitions was employed to access its performance up to 110 GHz, with the nanowires-vias transitions exhibiting state-of-the-art performance of about 0.23 dB per transition. A single nanowire-via was further explored mathematically, and it was concluded that a via with nanowires behaves as a solid via with an electrical conductivity that takes into account the nanowires density within the membrane.

Using the nanowires, 3-D solenoid inductors were explored. The fabricated solenoid can have self-resonant frequencies as high as 91 GHz for a 2-turn inductor. A simple model based on the physical layout was derived and shown to agree well with the measurements. The formulation of the model was analyzed and concluded that for these inductors, the return path needs to be well designed as it influences the equivalent inductance of the structure.

Slow-wave microstrip transmission lines that makes use of the nanowires to achieve the slow-wave effect were modelled. The lumped element proposed linear model have the most distinctive difference that it takes into account the magnetic coupling between the nanowires. This models the dispersion that happens as the frequency increases with the transmission line characteristic.

With all of these developments, this works enables the use of the MnM substrate as an interposer, making developments for interconnections using the nanowires on the substrate, fabrication of passive circuits and a model for slow-wave lines for redistribution layer.

As future works, to enable all potentialities of this substrate as an interposer, other topics can be explored as copper posts for soldering active devices, antennas, thermal characteristics of the substrate and for the nanowire-via, substrate integrated waveguides with and without slow-wave effect among others.

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