Linearity and Efficiency of Load Modulated Power Amplifiers

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Linearity and Efficiency of Load Modulated Power Amplifiers

Linéarité et Rendement des Amplificateurs de Puissance à Modulation d'Impédance

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Στη γιαγιά Βασιλική

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Allez, CIAO!

Abstract

In modern communication standards, Power Amplifiers (PA) have to achieve high efficiencies over increasingly larger dynamic ranges and bandwidths, while maintaining stringent linearity requirements. Efficiency enhancement can be achieved by load modulated architectures such as the Doherty Power Amplifier. However, amplifiers based on this concept are typically associated with degradation in linearity. In 4G networks, digital predistortion was used to mitigate the non-linearities of load-modulated amplifiers. However, the greater bandwidths and complexity of 5G NR systems limit the applicability of DPD.

This thesis aims at addressing the inherent linearity of high efficiency power amplifiers, so that they can be operated efficiently without or with limited predistortion. It is focused on the Load Modulated Balanced Amplifier (LMBA).

The LMBA is a recent architecture, presented as an alternative to the classic Doherty PA. A new mathematical analysis of the LMBA is proposed here, focused on the load modulation trajectory. This impedance-based analysis leads to the development of a new methodology for the design of linear/efficient power amplifiers from load-pull measurements of the main transistor. Applying this methodology to a 10W GaN HEMT, we show that three different amplifiers with similar performance in single-ended configuration result in very different performance when used inside an LMBA architecture. As predicted from our theory, the amplitude (AM-AM) and phase (AM-PM) distortions of the LMBA depend on the load trajectory. Choosing it so as to minimize the phase distortion, the second harmonic termination can then be selected to maximize the efficiency. The Class J second harmonic termination is identified as the best case, resulting in -40.5dBc ACLR (Adjacent Channel Leakage Ratio) with 40.5$\%$ drain efficiency at 2.4GHz when stimulated with a 10 MHz, 8.6dB PAPR (Peak to Average Power Ratio) LTE signal.

This same methodology is then applied at a K band 1W MMIC amplifier in GaAs technology. However, at these frequencies the second harmonic termination has a very small effect on the efficiency of the power amplifier. Lacking this extra degree of freedom, the load trajectory cannot be chosen for AM-PM mitigation, and the efficiency/linearity trade-off is degraded.

Finally, the origins and effects of impedance mismatch in power amplifiers is presented. The performance of the load modulated balanced amplifier under output impedance mismatch is studied. We observed that the efficiency enhancement of the LMBA is canceled if the optimal impedance is not presented at the output. A novel double balanced LMBA is then proposed to achieve mismatch resilience in high efficiency power amplifiers.

Résumé

Les nouveaux standards de télécommunication, en particulier la cinquième génération, imposent aux amplificateurs de puissance de très hauts rendements énergétiques tout en respectant des limites très strictes en termes de linéarité. Ces hauts rendements pour des gammes de puissance étendues peuvent être atteint par des architectures d'amplificatuers à modulation de charge active, comme l'amplificateur Doherty ou Chireix. Cependant, ces derniers ont tendance à produire une grande degradation de linéarité. Dans le cadre de la 4G, la prédistorsion numérique était utilisée pour corriger ces non-linéarités. Les largeurs de bande étendues de la 5G et la complexité de certaines architectures de front-end limitent le champ d'action de ces techniques numériques.

Cette thèse vise à répondre aux problématiques liées à la linéarité des amplificateurs à modulation de charge active afin de permettre leur utilisation avec peu ou sans prédistorstion numérique. Elle se base sur une architecture récente, le Load Modulated Balanced Amplifier (LMBA). Un deuxième projet s'articule autour des performances du LMBA lorsque l'impédance présentée à la sortie de l'amplificateur est désadaptée.

Après une présentation des concepts de base des amplificateurs de puissance, l'architecture LMBA est présentée. Une nouvelle formulation mathématique en est dérivée, basée sur la trajectoire de la modulation d'impédance. Cette analyse conduit au développement d'une nouvelle méthodologie pour la conception de LMBA linéaires basée sur des mesures load-pull du transistor principal. En identifiant au préalable la trajectoire de charge qui minimise la distorsion de phase, l'impédance présentée à l'harmonique 2 peut être choisie afin de maximiser le rendement sur toute la gamme de puissance, tout en garantissant la linéarité.

En appliquant cette méthodologie à un transistor GaN de 10 W de Cree (CGH410F), on montre que trois amplificateurs avec des terminaisons harmoniques différentes conduisent à des grandes différences de performance quand utilisés dans un LMBA Une terminaison harmonique capacitive apporte le meilleur compromis rendement / linéarité. Le système final a présenté -40.5 dBc ACLR et 40.5$\%$ de rendement à 2.4 GHz stimulé avec un signal LTE de 10 MHz et 8.6 dB de PAPR.

Cette même méthodologie a été appliquée à un transistor GaAs en bande K. Cependant, à cette fréquence avec cette technologie nous avons constaté que l'harmonique 2 n'impactait que très peu les performances du transistor. Sans ce degré de liberté supplémentaire le compromis rendement/linéarité se trouve donc très limité.

Le deuxième objectif était concentré sur les origines et conséquences de la désadaptation d'impédance à des amplificateurs à modulation de charge active. Nous avons vu par simulation que l'amélioration du rendement du LMBA se trouvait très fortement dégradée lorsque l'impédaence de sortie n'était pas idéale. Une nouvelle architecture a donc été proposée, appelée le Double Balanced LMBA, qui présente une grande résilience à la désadaptation d'impédance.

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List Of Acronyms

5G NR	5G New Radio
ACPR	Adjacent Channel Power Ratio
ALM	Active Load Modulation
AM	Amplitude Modulation
CMOS	Complementary Metal-Oxide-Semiconductor
CW	Continuous Wave
DC	Direct Current
DLM	Dynamic Load Modulation
DPA	Doherty Power Amplifier
DPD	Digital Pre-Distortion
DSM	Dynamic Supply Modulation
DSP	Digital Signal Processing
EA	Envelope Amplifier
EER	Envelope Elimination and Restoration
MBB	Mobile Broadband
ET	Envelope Tracking
EVM	Error Vector Magnitude
FET	Field Effect Transistor
FM	Frequency Modulation
FOM	Figure of Merit
FPGA	Field Programmable Gated Array
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GMSK	Gaussian Minimum Shift Keying
GSM	Groupement Special Mobile
HBT	Heterojunction Bipolar Transistor

HEMT	High Electron Mobility Transistor
IMD3	Third Order Intermodulation Distortion
IoT	Internet of Things
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LINC	Linear Amplification with Non-linear Components
LLC	Low Latency Communications
LMBA	Load Modulated Balanced Amplifier
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MEMS	Micro Electro-Mechanical System
MIMO	Multiple Input Multiple Output
MMIC	Monolithic Microwave Integrated Circuit
MP	Phase Modulation
MTC	Machine Type Communication
OBO	Output Back-Off
OFDM	Orthogonal Frequency Division Multiplex
OMN	Output Matching Network
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RFFE	Radio Frequency Front End
SC-FDMA	Single Carrier Frequency Division Multiple Access
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

List Of Symbols

α	Control amplifier to main amplifier current ratio
β	Input drive level
β_0	Breakpoint drive level
γ	dynamic range
Γ	Reflection coefficient
δ	Continuous modes design parameter
η	Drain Efficiency $(\%)$
Θ_{OMN}	OMN phase shift (rad)
Θ_{Bo}	Transistor's intrinsic LM-PM (rad)
ϕ	Control amplifier to main amplifier current phase difference (rad)
ω_0	Fundamental Angular Frequency (rad/s)
a_m	Forward power wave
b_m	Reflected power wave
BW	Bandwidth (Hz)
C_{ds}	Transistor's parasitic drain-source capacitance (F)
C_{gd}	Transistor's parasitic gate-drain capacitance (F)
C_{gs}	Transistor's parasitic gate-source capacitance (F)
d_{pm}	Splitting ratio
G_P	Power Gain (dB)
G_T	Transducer Gain (dB)
g_m	Transconductance (S)
I_c	Control amplifier fundamental current (I)
i_{DS}	Time-domain drain-source current (I)
I_{DS}	DC component of the drain-source current (I)
$I_{ds,f0}$	Fundamental component of the drain-source current (A)
I_L	Output current (A)
$I_{L_{\mathrm{BO}}}$	Output current at back-off (A)
$I_{L_{\mathrm{Max}}}$	Output current at peak power (A)
I_m	Main amplifier fundamental current (A)
$I_{m1,2}$	Branch transistor's fundamental drain-source voltage (A)

I_{Max}	Maximum drain-source current (A)
K	Rollet's Factor
P_{1dB}	1 dB output power compression point (W)
P_{3dB}	3 dB output power compression point (W)
P_{in}	Input Power (W)
P_{out}	Output Power (W)
P_c	Control amplifier's output power (W)
P_{DC}	DC Power (W)
P_m	Branch amplifier's output power (W)
P_L	Output power (W)
R_{opt}	Optimal fundamental resistance (Ω)
R_{BO}	Optimal back-off fundamental resistance (Ω)
R_{Max}	Optimal peak-power fundamental resistance (Ω)
S_c	Relative transistor size Sc
V_{Br}	Breakdown voltage (V)
v_{DS}	Time-domain drain-source voltage (I)
V_{DS}	DC component of the drain-source voltage (V)
$V_{ds,f0}$	Fundamental component of the drain-source voltage (V)
v_{GS}	Time-domain gate-source voltage (I)
$V_{gs,f0}$	Fundamental component of the gate-source voltage (V)
V_K	Knee voltage (V)
V_L	Output voltage (V)
$V_{m1,2}$	Branch transistor's fundamental drain-source voltage (V)
V_{Th}	Threshold voltage (V)
V_{SAT}	Saturation voltage (V)
X_{BO}	Optimal back-off fundamental reactance (Ω)
X_{Max}	Optimal peak-power fundamental reactance (Ω)
Z_{BO}	Optimal back-off fundamental impedance (Ω)
Z_{Max}	Optimal peak-power fundamental impedance (Ω)
Z_{f0}	Fundamental impedance (Ω)
$Z_{B/J_{f0}}$	Optimal B/J continuous mode fundamental impedance (Ω)
Z_{H2}	Second harmonic impedance (Ω)
$Z_{B/J_{H2}}$	Optimal B/J continuous mode second harmonic impedance (Ω)
Z_0	Characteristic impedance ($Omega$)

Introduction

In April 1973, Marty Cooper, a Motorola engineer, was making the first phone call from a mobile terminal. He was using at the time a First Generation protocol, still analog. Today, 4.3 billion subscribers worldwide are connected to the internet using a digital cellular network. This spectacular evolution of telecommunications is based on the developments of new technologies, both hardware and software. Advanced materials such as Gallium Nitride (GaN) allow the use of higher frequencies and greater power levels. Evolved transmitter architectures and enhanced computing resources enable very high efficiencies while still respecting stringent linearity requirements. Today the world is getting ready for the fifth generation of communication standards, 5G New Radio (5G NR). It will enable a new kind of network, designed to connect virtually everyone and everything together, including machines, objects and devices. However, one of the biggest challenges of 5G will be its environmental footprint. In a global attempt to reduce the utilization of the planet's resources, the 5G NR standard aims to decrease its overall power consumption by 90% compared to 4G networks at constant data rate.

I.1 Cellular Communication Standards

The past forty years have seen the development of five generations of cellular networks, with a new standard coming approximately every ten years.

- The **First Generation** of wireless communications first appeared in 1979 in Japan, and was spread in Europe and USA by 1984. Different protocols were used, incompatible with each other. They were based on analog modulation of the voice with Frequency Division Multiple Access (FDMA), usually in the sub 500MHz bands.

- The deployment of **2G** networks started in Europe in the early 1990's, with the development of GSM technologies. GSM was a major upgrade as it used for the first time digital radio signals based on frequency shift keying GMSK modulations with Time Division Multiple Access (TDMA). The aim of 2G was to provide a secure and reliable voice communication channel, and allowed some small data oriented services.

- **3G** was launched in 2001, based on WCDMA wideband code division multiple access with amplitude and phase modulation. It is the first data-oriented cellular protocol, and allows the use of internet services such as video streaming or email exchange. Data-rates are much higher than with 2G, but still under 2 Mbps. 3G was defined by the 3d Generation Partnership Project (3GPP), a global standardization initiative that aims to harmonize the different cellular networks worldwide.

- **4G** networks are being deployed since 2010, based on the the Long Term Evolution (LTE) and later LTE-Advanced standards. On the network layer, it is an all IP packet-switching protocol. The air interface is based on Orthogonal Frequency-Division Multiple Access (OFDMA) for

Downlink and Single Carrier frequency Division Multiple Access (SC-FDMA) for uplink technology and the use of Multiple Input Multiple Output (MIMO) systems. In order to reach ultra wide bands, 4G uses Carrier Aggregation (CA), which allows the assignment of two or more frequency blocks to be allocated to one user. LTE-Advanced can theoretically reach up to 1 Gbps data-rates and handles very large data traffic volumes.

In 2018, the 3GPP presented Release 15, launching the "Phase 1" of 5G New Radio (5G NR). It has three main objectives, that are Enhanced Mobile BroadBand (**eMBB**), Ultra Reliable Low Latency Communications (**urLLC**) and Massive Machine Type Communications (**mMTC**). More than just higher data-rates, it aims for the connection of everything, everywhere. Among other evolutions, 5G NR gives access to a whole new frequency range in the millimeter waves (24GHz - 100GHz).

Table I.1: Comparison of the different generations of wireless cellular communication standards

	1G	**2G**	**3G**	**4G**	**5G**
Technology	AMPS / NMT...	GSM*	WCDMA	LTE/LTEa	5G NR
Mutliple Access	FDMA	TDMA	CDMA	OFDMA	OFDMA/BDMA
Bandwiths	30 KHz	200 KHz	3.84 MHz	20MHz	100MHz / 400MHz[1]
Bands (GHz)	0.5	0.9 / 1.8	0.9 - 2.6	0.9 - 2.6	sub-6 / 24-40
Data-rates	–	–	2Mbps	1Gbps	10Gbps

* GSM was focused in Europe. USA and Japan used alternative IS54/136, IS95 and PDC
[1] 100 MHz for the sub-6 GHz bands, 400 MHz for the milimiter-wave bands

5G NR air interface is based on Orthogonal Frequency Division Modulation (OFDM). It is particularly efficient, as it allocates dynamically very narrow time and frequency slots to each user. Figure I.1 presents an OFDM modulator. The binary data is parallelized and modulated into symbols with phase and amplitude modulations (QAM). The resulting symbols are applied to very narrowband, adjacent subcarriers, with the use of an IFFT block. 5G NR addresses various applications, from low-power IoT to 4K video streaming, that require different throughput, data-rate and latency. In order to efficiently answer these demands the waveforms can be adapted thanks to a flexible numerology. The modulation order can go from a simple BPSK to a 256 QAM. Similarly, the subcarrier spacing ranges from 15KHz to 200KHz, and the number of carriers can vary. The overall signal bandwidth can go from 3.84MHz to 100MHz in the sub-6 GHz bands and up to 400MHz in the millimeter wave bands, by allocating more or less subcarriers to each user.

The flexibility of the OFDM spectrum is illustrated on the bottom of figure I.1. Three different users are allocated a different number of subcarriers, with an empty slot between users 1 and 2. The most important property of OFDM is the orthogonality of the subcarriers : at the maximum of each individual subcarrier (top of the arrows), all the others waveforms have a value of zero.

A major drawback that comes with advanced modulations is the complexity of the resulting waveform. OFDM signals are characterized by a very high Peak power (P_{max}) to Average Power (P_{avg}) Ratio (PAPR), defined as :

$$PAPR = 10 * \log\left(\frac{P_{max}}{P_{avg}}\right) \quad (1)$$

PAPR increases with the number of subcarriers, and can reach 12 dB with a probability of 1% in some worst case scenarios (15KHz spacing with 256 QAM). Figure I.2 shows an 8.5 dB PAPR

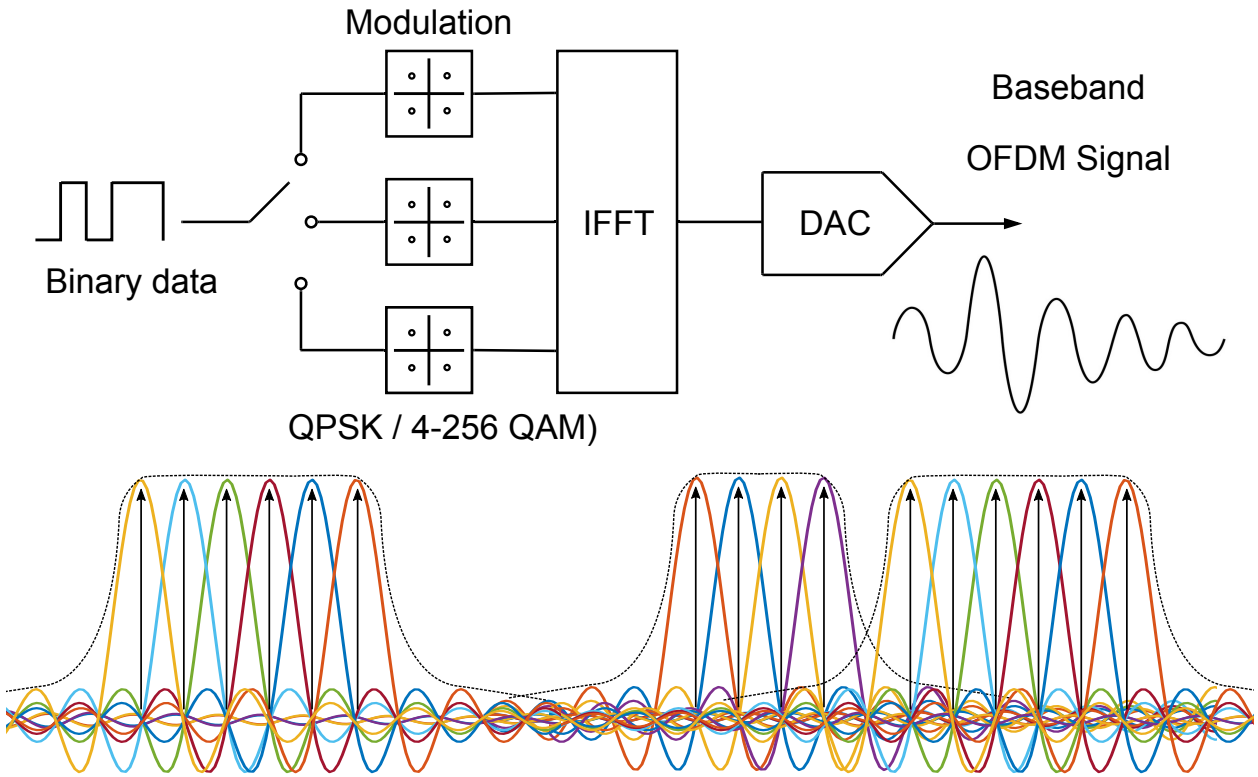


Figure I.1: OFDMA Modulator and resulting spectrum

OFDM waveform. It is becoming increasingly complicated to efficiently and accurately transmit these very high dynamic range signals. New, more advanced transmitter architectures and technologies have to be developed.

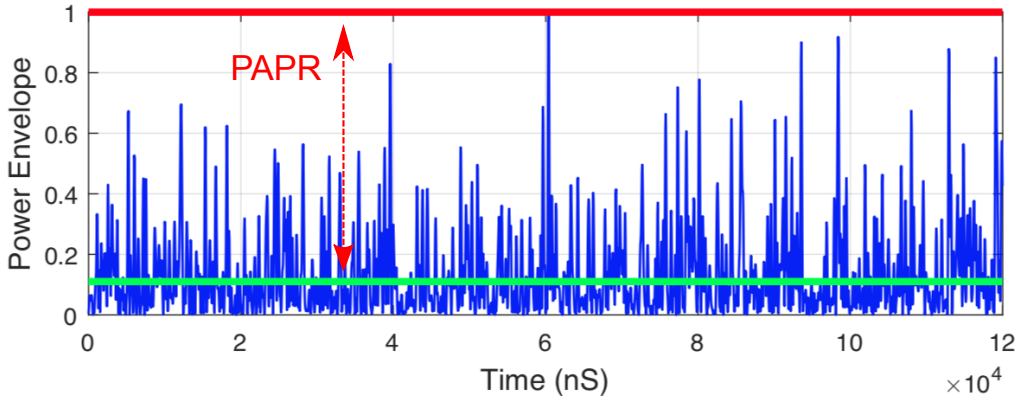


Figure I.2: 8.5dB PAPR OFDM waveform. In green the average power, in red the maximum power.

I.2 Radio-Frequency Front End Architectures

In cellular standards, communication between mobile terminals, referred to as User Equipment (UE), goes through a Base Station (BS). In 4G and 5G systems, we can distinguish two sub-protocols :

- **Uplink (UL)** : From a UE to the BS. SC-FDMA modulation can be used, a lighter version of OFDMA resulting in smaller PAPR (around 6 dB). Maximum transmit power is 23 dBm but can be smaller. They are organized in categories (from 0 to 13), depending on the hardware of the UE (number of MIMO antennas, Carrier Aggregation etc). In 5G NR OFDM can also be used when very high data-rates are needed.

- **Downlink (DL)** : From the BS to the UE. Based on OFDMA. Macro/Small/Micro/Pico/Femto cells transmit power levels going from 20dBm to over 50 dBm (several hundred watts). With 5G NR, new Active-Array BS for massive MIMO applications at millimeter-wave bands are integrated.

A radio-frequency transmitter is composed of a Modulator/Demodulator (MoDem), that creates a baseband analog signal from binary data, and the RF Front-End (RFFE). The RFFE comprises the up/down-converters and the transmit and receive paths. Figure I.3 presents a schematic diagram of an RF transmitter. The most important components in the RFFE are the Power Amplifier (PA), responsible for the emission of the signal at the required power level, the Low Noise Amplifier (LNA) that amplifies the extremely low power received signal and the various filters and switches, responsible for the organization of the frequency spectrum.

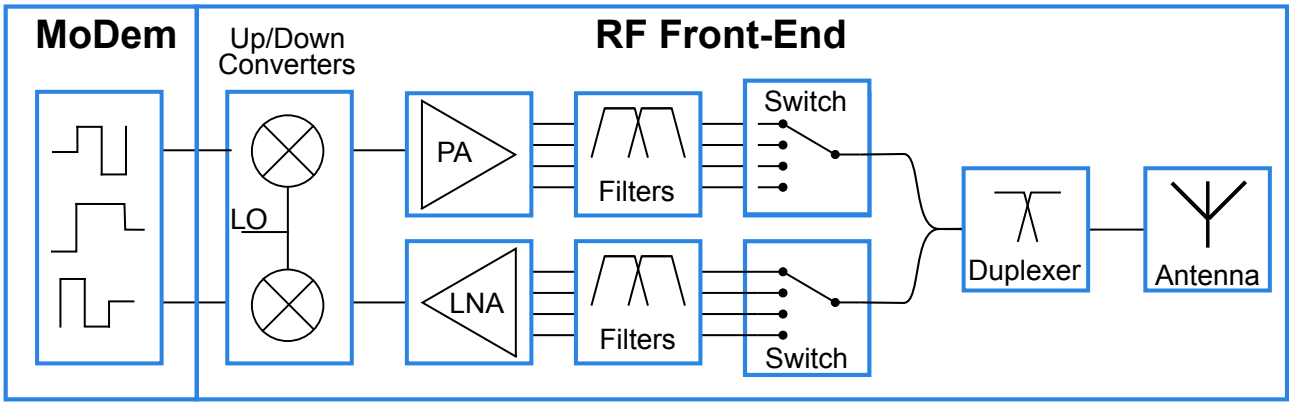


Figure I.3: Direct Conversion 5G RF transceiver

In practice, depending on the application, the front-end architecture can be more or less complex. A smartphone RFFE for example has on the same board two to three transmit paths that share the overall spectrum, and as many receive paths (LNA, duplexers, filters) as sub-bands. Base stations on the other hand usually have a distinct RFFE board for each sub-band, in order to maximize performance. Figure I.4 presents a Smart Antenna Array (SAA) base station transceiver from QORVO for millimeter-wave massive MIMO. Extensive research is done on each component comprising these systems in order to optimize performance, cost and form factor.

Within the transmitter, the Power Amplifier (PA) is the most critical component. It can represent more than 50% of the overall power consumption, and its performance determines the quality of a communication. Its function is to perform DC to RF power conversion. From a system level point of view a PA can be described with five properties :

- **Output Power** : In the sub-Watt range for mobile terminals, can reach several hundred watts for base stations.

- **Energy Efficiency** : Being the most power hungry element in the front-end, the efficiency of PAs impacts the power consumption of the whole 5G network.

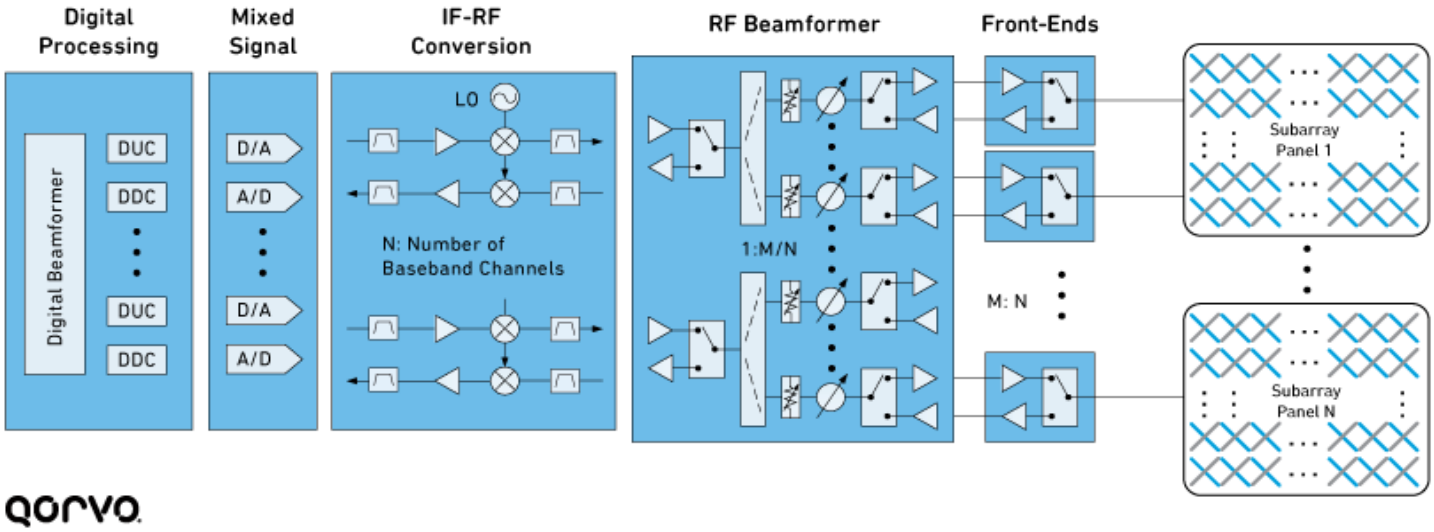


Figure I.4: Massive MIMO Transceiver

- **Gain** : The PA amplifies the very low power signal coming from the DAC and needs sufficient gain to reach the wanted output power. Usually additional drivers are needed to generate enough gain, degrading the overall efficiency.
- **Linearity** : Being a Large-Signal component, the non-linearities of a PA can strongly impact the Quality of Service (QoS) of a communication. Additionally, non-linear behaviour results in out-of-band emissions, disturbing adjacent communication channels.
- **Bandwidth** : Power Amplifiers are the main bandwidth limiting components in the front-end, as their performance tend to vary a lot with frequency. Achieving the ultra-wide bandwidths of 5G NR while keeping sufficient efficiency and linearity levels is a great challenge.

PA performance is dictated by trade-offs. Efficient operation can be achieved with different techniques, at the cost of highly degraded linearity. Similarly, higher gain usually involves multiple amplifying stages, resulting in lower efficiency. Large bandwidth can be obtained by compromising the other parameters.

Efficiency / Linearity trade-off

In order to preserve the integrity of the modulated signal and correctly transmit all power levels, the PA's average output power must be backed-off from the maximum power by the same amount as the PAPR. We call this lower power level Output Back-Of (OBO). However, efficiency is highest at maximum power, and drops very rapidly as the power decreases. This contradiction is at the heart of Power Amplifier design. Figure I.5 illustrates this trade-off. It presents the power density functions of an LTEa, WCDMA and GSM signals. The dotted line shows a class B power amplifier's drain efficiency versus OBO. 2G's GMSK (red curve) is a continuous phase frequency shift keying modulation, resulting in a constant amplitude signal. The power amplifier can be kept in saturation, where the efficiency is in theory 78%. Efficiency drops very rapidly, and reaches 35% for the 3.8dB PAPR WCDMA signal (blue curve), and goes as low as 15% with LTE (green curve) !

Taking into account all the different losses in a 5G macro base station, including, cooling and power distribution, considering 15% average efficiency for the power amplifier, the overall transmitted

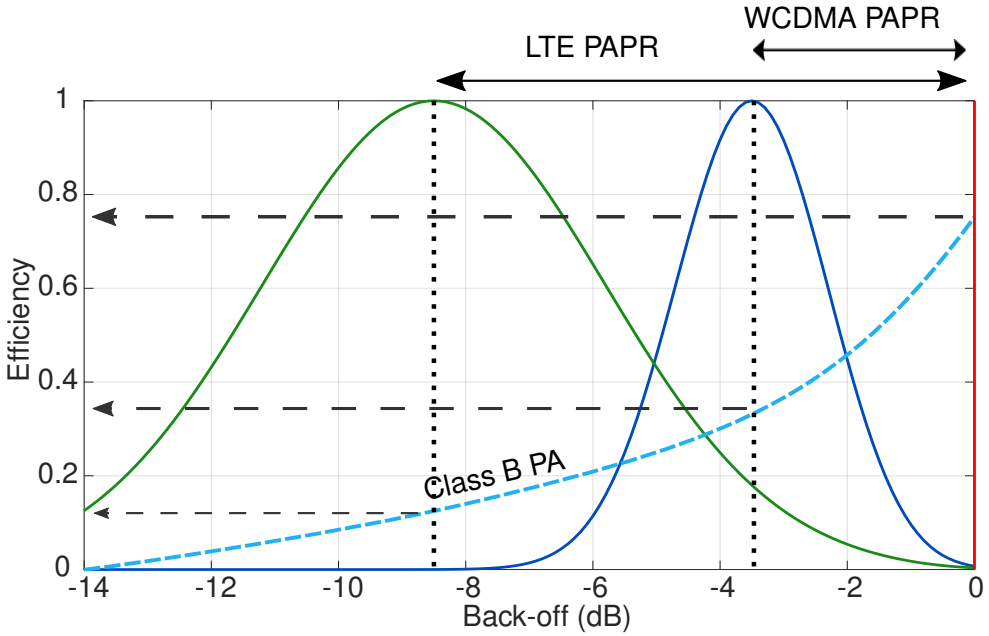


Figure I.5: Power Density Function of an LTE (green), WCDMA (dark blue) and GSM (red) signals versus OBO. In dashed blue line Class B PA efficiency versus OBO.

efficiency becomes as small as 9% ! 555 watts are necessary in order to transmit a 50 watt RF signal [1].

High Efficiency Power Amplifier Architectures

Maximum efficiency of a power amplifier is achieved when the RF swing of the output voltage reaches the supply voltage. In static systems, this occurs at maximum power. In practice, this high performance point depends on the drain voltage, output impedance and transistor technology and size. Since we cannot increase low power efficiency by dynamically changing the transistor's intrinsic characteristics, we have to take advantage of the other two degrees of freedom. We can distinguish two families of high efficiency architectures :

- **Dynamic Supply Modulation (DSM)** : Dynamically changing the drain or gate bias can keep very high efficiency for a large power range. In practice, the most common DSM technique is Envelope Tracking (ET), where a both phase and amplitude modulated RF signal is fed to the PA, and the drain bias is dynamically modulated along with the envelope variations of the input signal. [2]

- **Dynamic Load Modulation (DLM)** : For a given output current, the RF voltage swing depends on the output impedance. If DC voltage is fixed, changing this impedance can increase the RF drain voltage. DLM consists in dynamically adapting the output load termination of a power amplifier to keep a high voltage, and thus high efficiency for a large OBO. Architectures using this concept, such as the classic Doherty PA (DPA) [3] or outphasing PAs [4, 5], are typically composed of two or more transistors that interact through a non-isolating power combining network. Through asymmetric operation in amplitude and/or phase, each device controls the impedance seen by the other, thereby tracing a load trajectory that maintains efficiency while modulating the output power.

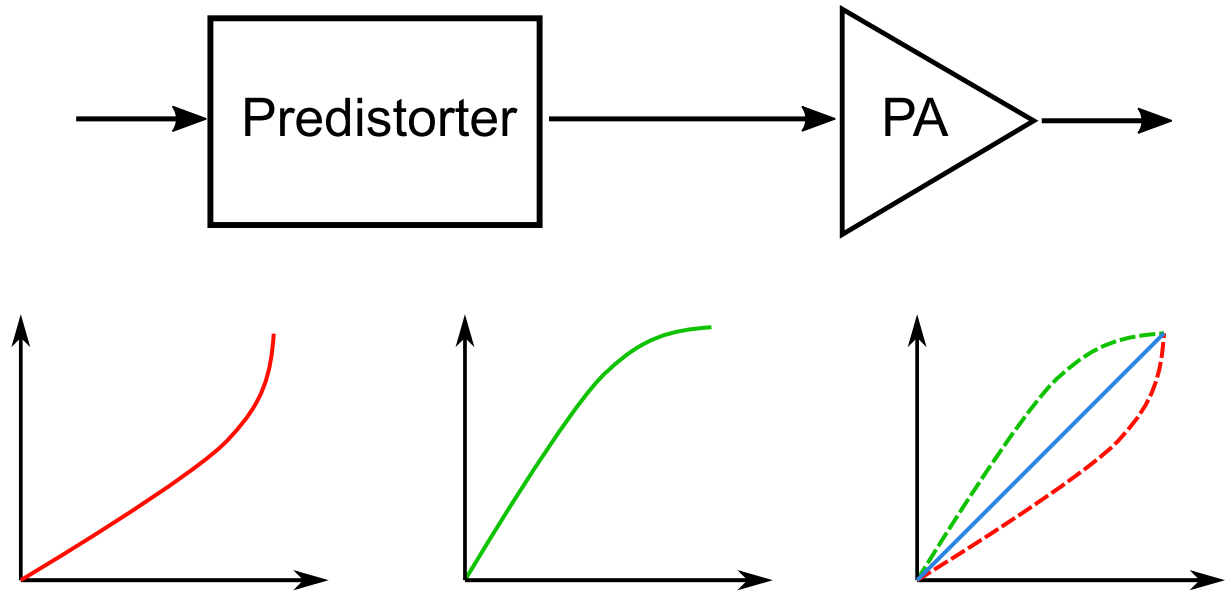


Figure I.6: Digital Predistortion : In red the predistorted signal, in green the PA characteristics, in blue the emitted signal

Linearity Considerations

Both these techniques have been widely used since 4G networks and the use of high PAPR OFDM signals. There is no doubt they will be even more popular in the next years. However, architectures based on supply or load modulation are typically associated with degradation in linearity. both the gain and phase response of a transistor are strongly dependent on the impedance and voltage presented to the drain [6]; therefore, high efficiency amplifiers are subject to strong amplitude (AMAM) and phase (AMPM) distortions [7].

5G NR imposes stringent linearity requirements in order to ensure a certain Quality of Service. Additionally, PA distortions produce InterModulation Products (IMD), that cause spectral leakage on adjacent communication channels. Adjacent Channel Leakage Ratio (ACLR) is used by designers to characterize the linearity of a transmitter.

The use of Digital Predistortion (DPD) can alleviate the linearity issues of high efficiency amplifiers. This approach, presented in figure I.6 consists in feeding a PA with a specially predistorted signal, that takes into account the transmitter's AMAM and AMPM distortions. Whereas DPD successfully mitigated nonlinearity in 4G systems, the greater bandwidths and complexity of 5G NR limit its applicability. In Massive MIMO scenarios, for example, where dozens of PAs are integrated in a limited space, the individual feedback paths needed for adaptative DPD cannot be implemented. Similarly, the DC power consumption of DPD in low-power base stations is enough to degrade the overall efficiency [8][9].

Impedance Mismatch

5G NR drastically increases the number of users by giving access to new frequency bands, both in the sub-6GHz range (FR1) and in the millimeter waves (FR2). This has a great impact in the UE RFFE, as multiple amplifiers, filters, switches etc are needed to cover the whole available spectrum, with very limited space. This very high integration results in imperfections at various points of the transmitter. Specifically, the impedance presented at the output of the PA changes within a frequency band, resulting in suboptimal performance. In base stations, power amplifiers are usually protected from such variations with an isolator. However, in Massive MIMO transceivers, where great efforts

have been made to limit the number of components, the bulky isolator has to be removed. In such an environment, crosstalk from the other array elements reflects power back to the transistor, resulting in Voltage Standing Wave Ratios (VSWR), similar to impedance mismatch.

Power amplifiers are designed to function under a 50Ω load. Impedance mismatch tends not only to degrade intrinsic performance like gain, output power or efficiency, but disrupts more complex systems such as high efficiency architectures or DPD. It becomes more and more important to find novel architectures that are VSWR resilient.

Thesis Context and Main Contributions

As we can see throughout this chapter, the power amplifier is a key component in an RF Front-End. Modern communication standards require unprecedented performance, that classic single-ended amplifiers cannot achieve. While the association of DLM and DSM with digital predistortion was sufficient to meet 4G specifications, 5G NR pushes even further the requirements in terms of bandwidth and linearity. It is therefore necessary to address the inherent distortion associated with high efficiency architectures, so that it can be operated efficiently without or with limited predistortion.

This PhD work, sponsored with a CIFRE contract between Somos Semiconductors and the ESYCOM UMR CNRS 9007 laboratory, investigates novel power amplifier architectures for future 5G communication standards. A particular interest is brought to the Load Modulated Balanced Amplifier (LMBA).

A first part of the research work was developed at SOMOS Semiconductor, a fabless CMOS PA design company located in Paris. The goal was to find novel, low complexity solutions to limit performance degradation of power amplifiers under impedance mismatch. This study led to the design of a double balanced, high efficiency load modulated balanced amplifier, presented in 2019 at the COMCAS Conference in Tel Aviv.

A second part of the work took place at Colorado University, in Boulder, USA, as part of a 1 year PhD student exchange program. It was developed under the supervision of Pr. Taylor W. Barton. it aimed at further expanding the theory of the Load Modulated Balanced Amplifier to include generalized load trajectories that can achieve in better efficiency / linearity trade-offs. A paper resulting from this study will be published during the European Microwave Week conference. An article has also been submitted for publishing at the Transactions on Microwave Theory and Techniques journal.

Thesis Outline

Chapter 1 presents the theory and mathematical formalism of the design of power amplifiers. A review of the state of the arts of transistor technologies and PA architectures is carried out.

In Chapter 2, the mechanism behind high efficiency architectures such as Dynamic Load Modulated or Supply Modulated PAs is further explored. After a brief historical review, the current state-of-the-Art technologies are examined, presenting the current limitations and the future trends.

The theory of the novel Load Modulated Balanced Amplifier is presented in chapter 3. An alternative mathematical derivation of the load modulation mechanism is proposed based on the load trajectory, and a new methodology for the design of linear and efficient LMBAs based on load pull data is presented.

Chapter 4 is focused on simulations and measurements validating the previously explored theory. The realization of a highly linear and efficient Load Modulated Balanced Amplifier is also presented. The validity of the theory is assessed for a K band MMIC LMBA in GaAs technology.

Finally, chapter 5 presents a novel, VSWR resilient high efficiency amplifier.

The conclusion summarizes the work presented in this thesis and explores future axes of research.

I.3 List of Publications

This work resulted in the following publications :

International conference publications :

- K. Vivien, G. Baudoin, O. Venard and P. Pierre-Charles-Felix, ”A Novel Double Balanced Architecture with VSWR Immunity for High Efficiency Power Amplifier,” 2019 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS), Tel-Aviv, Israel, 2019, pp. 1-5, doi: 10.1109/COMCAS44984.2019.8958381.
- K. Vivien, P. De Falco, P. Pierre-Charles-Felix, O. Venard, G. Baudoin, T. Barton, ”Load Modulated Balanced Amplifier Designed for AM-PM Linearity”, 2020 IEEE International Conference European Microwave Week (EuMW), Utrecht, Netherlands, 2020

Journal articles submitted for publication :

- K. Vivien, P. De Falco, P. Pierre-Charles-Felix, O. Venard, G. Baudoin, T. Barton, ”Linear Load Modulated Balanced Amplifier Method Based on Complex Impedance Trajectories”, Transactions on Microwave Theory and Techniques, 2020

Workshops :

- ”Towrds Highly Efficient Power Amplifiers under Impedance Mismatch”, K. Vivien, G. Baudoin, O. Venard, IEEE International Conference Radio Wireless Week (RWW), Orlando, Florida, 2019

Patents :

- H. Guegnaud, P. Pierre-Charles-Felix, V. Vinayak, ”Power Amplifier with Stepwise Envelope Trackign and Adaptative Load” WO2018162746A1, EPO

Chapter 1

RF Power Amplifiers

This chapter covers the foundations of Power Amplifier design. The various transistor technologies are presented, followed by a brief explanation of modeling techniques and the analysis tools used throughout this thesis. The different PA modes of operation are introduced together with the basics of linearization and high efficiency architectures. An overview of state-of-the-art designs tackling the various problematic associated with power amplifiers is exposed at the end of this chapter.

1.1 About Power Amplifiers

We are interested here in the fundamental concepts required to understand the design of Power Amplifiers.

A power amplifier can be considered as a DC to RF power converter, that transforms the power provided by the power supply in an oscillating energy, that adds up with the RF input signal (figure 1.1). However, part of this DC power is not converted to RF, but rather thermally dissipated by the device. We have :

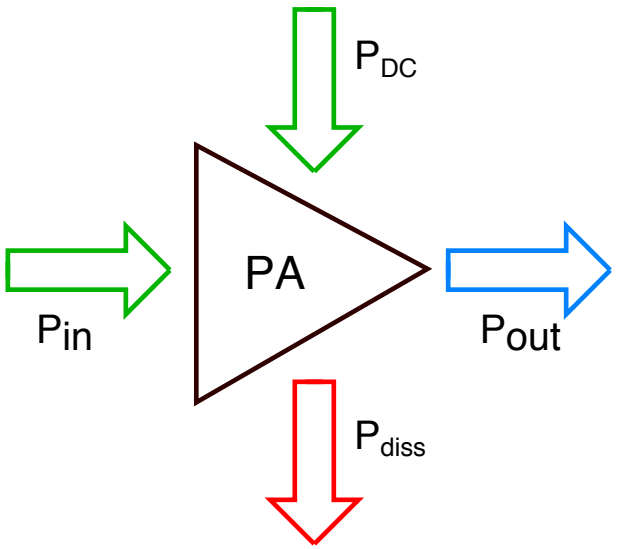


Figure 1.1: Power budget of a Power Amplifier

$$P_{in} + P_{DC} = P_{out} + P_{diss} \tag{1.1}$$

Where P_{in}, P_{DC}, P_{out} and P_{diss} are the input, DC, output and dissipated power respectively.
The Power Gain G_P of a PA is defined as the ratio of the input to the output power.

$$G_P = \frac{P_{out}}{P_{in}} \tag{1.2}$$

Here the input and output power are the actual power delivered to the input of the transistor and the power radiated by the output load.

The Transducer Gain G_T is preferred to the power gain, as it takes into account the mismatch between the PA and the generator :

$$G_T = \frac{P_{out}}{P_{gen}} \tag{1.3}$$

Where P_{gen} is the power available from the generator.
The Drain Efficiency (DE or η) is the ratio of the output power to the DC power :

$$\eta = \frac{P_{out}}{P_{DC}} \tag{1.4}$$

We can also define the Power Added Efficiency (PAE) as the ratio of the difference between the output and input power to the DC power :

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}(1 - \frac{1}{G_P})}{P_{DC}} = \eta \left(1 - \frac{1}{Gp}\right) \tag{1.5}$$

For large power gains (more than 12 dB), the PAE is very close to the drain efficiency. In commercial power amplifiers, multiple amplifying stages are usually employed in order to reach more than 20 dB of gain. The PAE is used to assess the efficiency of a component. In the research field however, where we are mostly interested in the intrinsic performance of a component and not in making a ready-to-use amplifier, PAs are usually single-stage, with a relatively low gain. Drain Efficiency becomes then the major efficiency measurement.

1.2 Practical Power Amplifier Design

Figure 1.2 presents a generic Power Amplifier. The first step in power amplifier design is the choice of the active device. This will be driven from the requirements in terms of output power, frequency, efficiency linearity and cost. The major technologies of transistors will be presented in the next section. Once the device is selected, it has to be stabilized to avoid oscillations, potentially destructive at higher levels. The stability of a single stage amplifier can be assessed with the Rollet Factor K [10], measured from its small signal S parameters :

$$K = \frac{1 - |S_{11}| - |S_{22}| + |\Delta|^2}{2|S_{21}S_{12}|} \tag{1.6}$$

Where Δ is the is the determinant of the S matrix of the 2-port network.

$$\Delta = S_{11}S_{22} - S_{21}S_{12} \tag{1.7}$$

The transistor is unconditionnaly stable if $K > 1$ and $|\Delta| < 1$. Once the transistor is stabilized the next step consists in input and output matching.

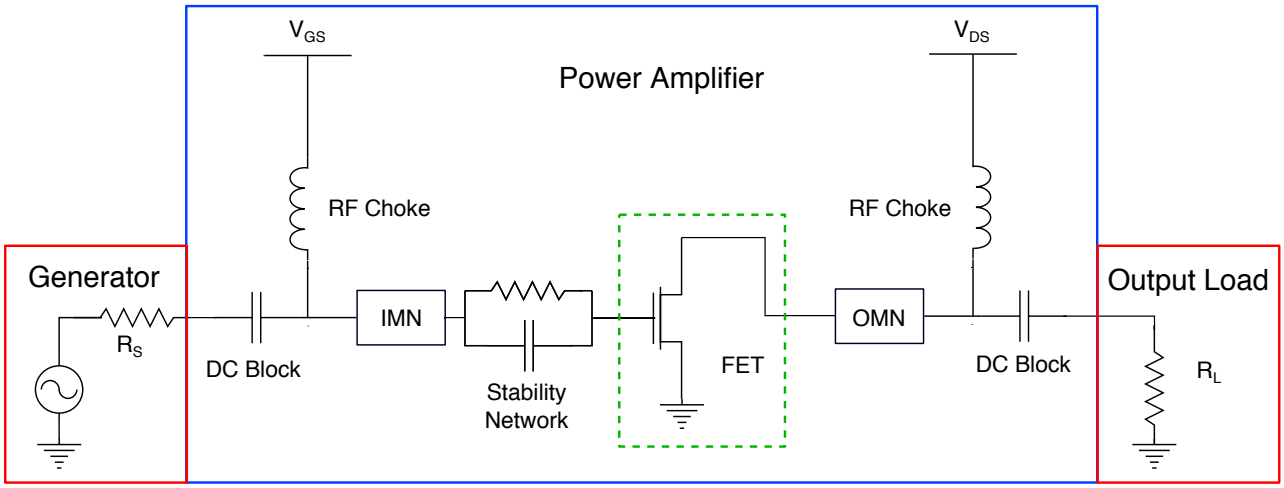


Figure 1.2: Generic Power Amplifier

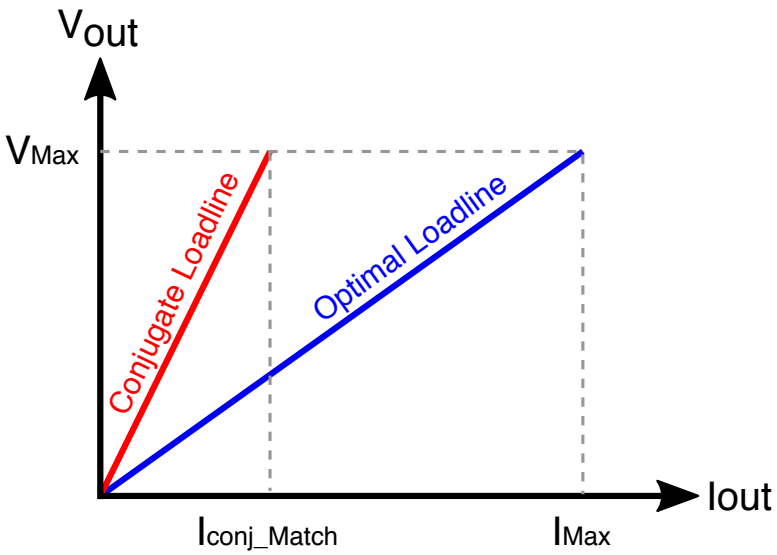


Figure 1.3: Conjugate matching versus power matching

Optimal impedance and Load Pull measurement

Impedance matching is a very important subject in high frequency circuits as it defines the power transfer between two nodes. In order to maximize this power transfer, the impedances presented at each side of an intersection need to be complex conjugates. In power amplifier design however, complex conjugate matching results in sub-optimal performance, and the transistor's physical limitations need to be taken into account [11].

For example, consider a power generator with 50Ω internal resistance and maximum current of 1A. Conjugately matching this device would result in a drain voltage swing of 50V. If this generator is based on a 10V process, the current would be limited, and the output power reduced. In order to exploit the maximum current and voltage swing, a lower value impedance has to be presented to achieve power match. Figure 1.3 illustrates the different matching techniques.

The optimal fundamental impedance is defined as the ratio of the maximum fundamental voltage

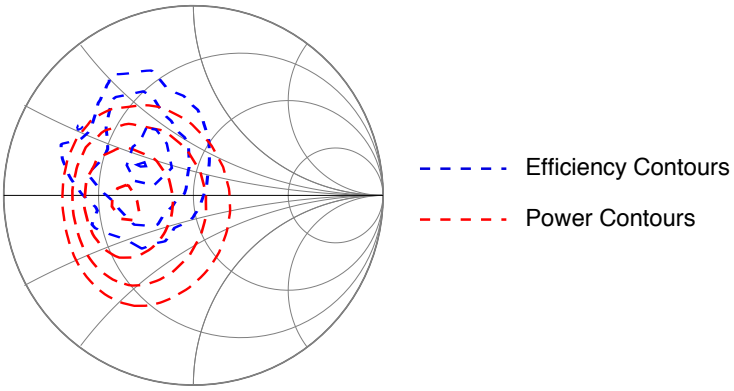


Figure 1.4: Load Pull contours on a smith chart

to the maximum fundamental current at the drain of a transistor:

$$R_{opt} = \frac{V_{ds,f0,max}}{I_{ds,f_0,max}} \tag{1.8}$$

In practice, $V_{ds,f0,max}$ and $I_{ds,f_0,max}$ are not known, and only an approximate R_{opt} can be found by calculations. In order to maximize performance, the output impedance is selected by a Load-Pull measurement.

Load-Pull measurement consists in presenting at the transistor's drain different impedances and measuring the different performance such as gain, output power and efficiency. The impedances can be synthesized with a passive or active load tuner. The results are usually displayed as contours on a Smith-Chart, like in figure 1.4. This procedure can be carried out at the fundamental and harmonic frequencies. Load-pull measurements require a complex and expensive test-bench, and are time-consuming. With the evolution of component models, computation resources and design softwares, load-pull can now also be performed in simulation. Looking at figure 1.4, it is interesting to notice that often, the maximum power and maximum efficiency impedances are not the same.

Once the optimal output impedance of the transistor is identified, the input has to be matched to the generator. This can either be a conjugate match, resulting in maximum linear gain, or a source-pull procedure can be done to optimize different parameters.

Power Amplifier architectures

Power amplifiers can be used in Single-Ended (SE) configuration or with multiple transistors. We can identify four different topologies :

- **Single Ended** : Only one transistor is used as the power structure, like in figure 1.2. It is the most simple architecture.
- **In-phase Parallel Combining** : Multiple transistors are put in parallel to increase the total output power. Wilkinson dividers and combiners are used to split and recombine the input and output signals. This architecture is widely used in IC designs in order to reach higher power levels, especially when the drain voltage is low such as in GaAs process. On the downside the extra components such as the combiners increase loss, reducing efficiency.
- **Balanced Amplifier** : Like In-phase combining, two transistors are put together, but this time they are combined with a hybrid coupler. The two amplifiers are in quadrature. This architecture is very interesting as it is very robust to impedance mismatch.

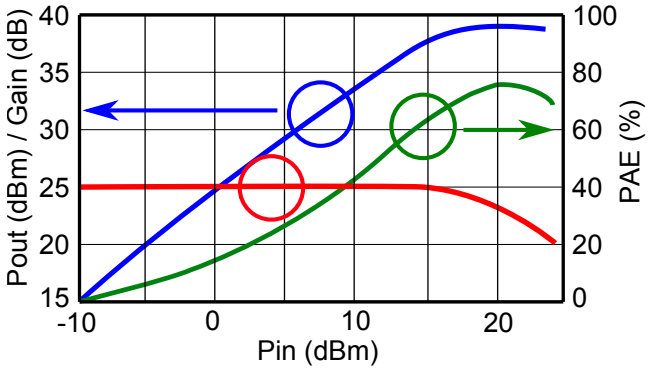


Figure 1.5: Power Amplifier characteristics : in blue the output power, in red the gain and in green the power added efficiency.

- **Differential Amplifier** : Also referred to as Push-Pull Amplifier. Two out-of-phase transistors are combined together with a balun combiner, usually a transformer. This architecture is mostly used with CMOS amplifiers, as this technology does not have a backside via. The balun combiner creates a virtual ground, drastically reducing the parasitics related to the source-to-ground access. The Push-Pull configuration also requires a four times bigger optimal impedance. In high power - low drain voltage applications this can be very interesting.

Power Amplifiers Linearity

A linear amplifier is characterized by an output varying proportionally to the input, i.e. a flat gain and phase response. Looking at figure 1.5, we can see that this is true up to approximately an input power of 15 dBm. After that, the gain (red curve) decreases, and the output power (blue curve) reaches its maximum value. We say that the amplifier is compressing. Power amplifiers are inherently non-linear systems. They can be described by a polynomial expression :

$$y(t) = \alpha x(t) + \beta x(t)^2 + \gamma x(t)^3 + ... + \kappa x^n \tag{1.9}$$

This equation is a simplified model, not including memory effects. Inside the linear region, the influence of the non-linear terms is insignificant compared to α. When the amplifier reaches compression, they become much more important, and the input-output proportionality disappears. The emitted signal is distorted, and can become unusable [11]. Under a multi-tone excitation, like an LTE modulated signal, the presence of these raised powers of x create unwanted copies of the output signal at different frequencies. At harmonic frequencies we find the second and third order distortion products. These are usually far enough and can be filtered out. InterModulation Products (IMD) on the other hand appear at combinations of the different signal frequencies, resulting in copies of the original signal very close to the actual signal band. Odd modes IMD close to the carrier cannot be eliminated after the PA, and cause interference to adjacent communication channels.

Apart from the device's intrinsic non-linearities, memory effects also degrade the emitted signal. This is a non-static behavior, that occurs with dynamic signals, as the value of the output depends not only on the present but also on the previous input or output state. We can distinguish short-term (a few micro-seconds) and long term (milliseconds to indefinite) memory effects. The main origins of memory distortion are [12]:

- Frequency memory effects : with wideband signals, the gain and phase response of the transistor and of matchng networks is not the same for each frequency component

- Bias memory effects : The rapid changes of the bias voltage due to the varying envelope of the input signal cause a lag between the DC voltage and current when the bias line is inductive.
- Temperature effects
- Technology related effects, such as trapping in GaN technologies can induce very long term memory effects
- Device degradation

In practice there are two common metrics that characterize the linearity of an amplifier : the Error-Vector Magnitude (EVM) and the Adjacent Channel Leakage Ratio (ACLR).

$$EVM = 10log_{10}\frac{\sum_{n=1}^{M}|Y(n)-X(n)|^2}{\sum_{n=1}^{M}|X(n)|^2} \tag{1.10}$$

$$ACLR = 10log_{10}\frac{P_{out,adj}}{P_{out,ref}} \tag{1.11}$$

EVM measures the error vector between the original symbol $X(n)$and the actual emitted symbol $Y(n)$. It is used to characterize the in-band distortion, and thus the error probability. In practical measurements, PA designers are rather focused on ACLR, which is widely used as a linearity assessment. $P_{out,adj}$ and $P_{out,ref}$ represent the power at the emission channel and the adjacent channel. We can measure both right and left ACLR, for the adjacent and the next (alternate) channel. ACLR characterizes the out-of band emissions, illustrated in figure 1.6.

Many different techniques have been proposed and demonstrated over the years for the reduction of amplifier non-linearities. The most straight-forward approach is to back-off the average power of the power amplifier. The output signal stays in the small-signal, linear region, at the cost of very small efficiency. The simplest linearization technique is the feedback loop. An error signal is injected from the output to the input of the power amplifier in order to cancel out the distortions. Unfortunately

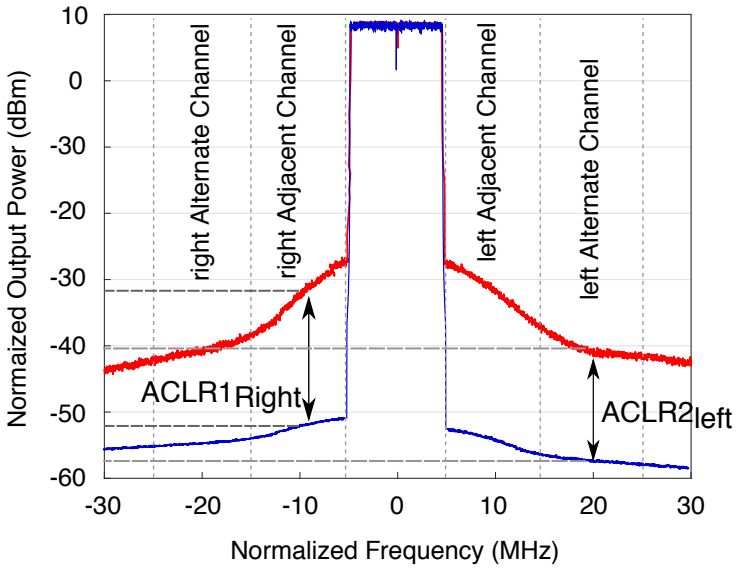


Figure 1.6: Input (in blue) and output (in red) spectrum of an LTE signal going through a PA!

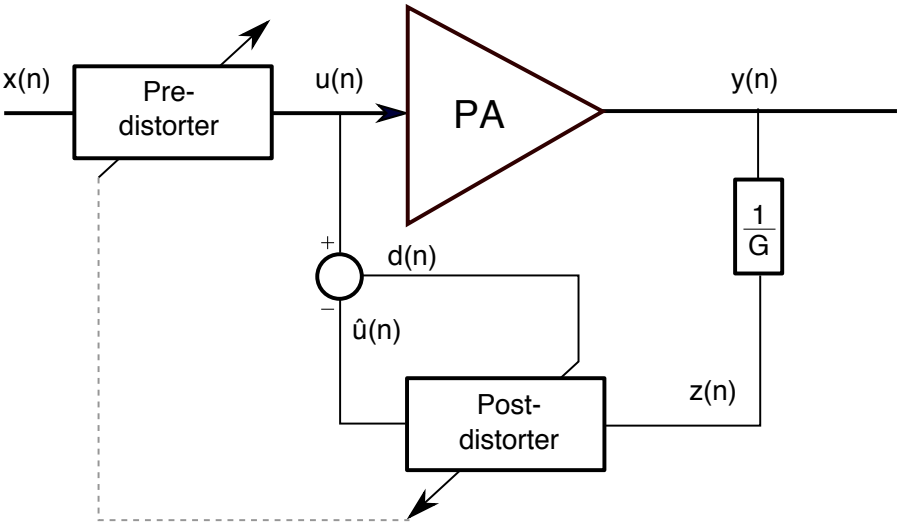


Figure 1.7: Indirect Learning Architecture for Digital PreDistortion

in high frequency circuits this technique can be very dangerous as it can create instability, especially with wider bandwidth signals [13]. Many variations have been employed, such as envelope feedback or cartesian loop. Here again bandwidth is a limitation factor, and there is a trade-off between performance and stability. An alternative technique is the feedforward loop. An error signal is still used to cancel out non-linearities but this time it is done on the output. Feedforward is an unconditionally stable architecture, but requires an extra amplifier for the error signal path. It leads to complex electronic systems, that are bulky and unefficient.

Predistortion is another linearization technique. It works by synthesizing the inverse transfer function of the power amplifier and applying it to the input signal, before the PA. The concept of predistortion can be seen on figure I.6. Analog predistorters working at RF frequencies exist, and use non-linear components such as varactors, diodes or FETs to create the inverse transfer function [14]. But with the development of very fast DSPs enabled FPGAs, Digital PreDistortion (DPD) is the most widely used linearization technique [14]). In that case the modulated signal is directly predistorted in the digital domain, before being upconverted. In order to create the inverse transfer function, DPD needs to estimate a model of the power amplifier. This model usually takes the form of a (more or less) complex polynomial with the number of coefficients and memory depth reflecting its complexity.

Indirect Learning Architecture (ILA) [15] can be used to identify the parameters of the predistorter. ILA is based on the inverse modeling approach, where a post-inverse model of the PA is identified by using the PA output signal $y(n)$ to model the PA input $u(n)$, as illustrated in figure 1.7 [16, 17]. Once the post-inverse of the PA (also known as postdistorter) has been identified, the parameters of the postdistorter are copied to an identical model that is used as the predistorter [15].

1.3 Transistor Technology

The landscape of RF applications is very diverse, including cellular communications, digital TV broadcasting, space or military applications among others. This has led over the years to the development of various technologies. The choice of the device depends mainly on the frequency and required output power levels. In satellite communications for example Travelling Wave Tubes (TWT) are used, as very high powers are needed at very high frequencies. Solid-State Power Amplifiers (SSPA) are nevertheless at the core of nearly all modern low-to-medium power RF applications, and

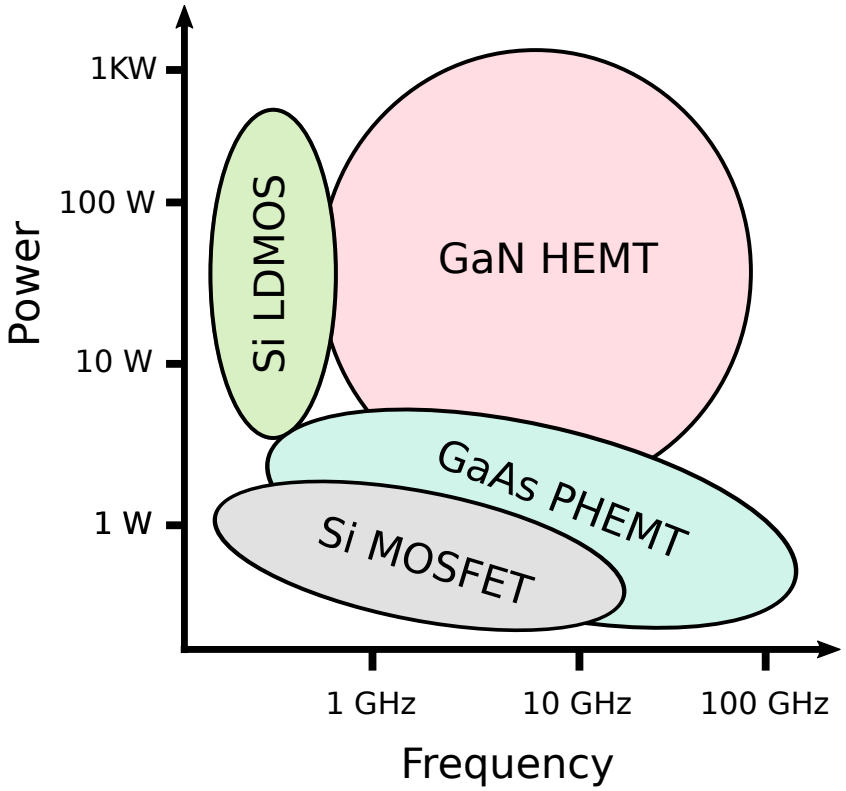


Figure 1.8: Transistors technologies and their application []

are gaining ground in the high power territory.

Table 2.1 compares the properties of the main semiconducting materials used in RF designs :

Table 1.1: Comparison of the main RF semiconductor materials

Material Property	**Silicon**	**SiC**	**GaAs**	**GaN**
Band Gap (eV)	1.12	2.86	1.42	3.39
Breakdown Field (kV/cm^2)	300	2000	400	2000
Saturation Electrical Velocity (cm/s)	9E6	2E7	1.3E7	2.3E7
Electron Mobility ($cm^2/(V.s)$)	1450	500	8500	800
Thermal Conductivity ($W/(cm.C)$)	1.45	3.5	0.46	1.3

Figure 1.8 illustrates how the different technologies are used.

Silicon Transistors

Silicon based transistors are by far the cheapest, as they benefit from the massive investments of the integrated circuits (IC) industry. In the RF field, we can distinguish three Si transistors :

- **Latteraly Diffused MOS FET (LDMOS)** : Most LTE macro base stations use LDMOS as a power device. Limited in sub 3 GHz frequencies, it can achieve several hundred watts in fairly low cost.
- **Complementary MOS FET (CMOS)** : The great majority of IC's are based on CMOS transistors. It is a very cheap technology but with relatively poor RF performance. Its low breakdown voltage constraint its use in low power applications.

- **Silicon Germanium Heterojunction Bipolar Transistor (SiGe HBT)** : SiGe present much higher performance in terms of efficiency or linearity compared to CMOS, but is limited to very low power and high frequency.

Though very cheap, Silicon transistors present relatively poor RF performance, in terms of noise, efficiency and output power. Many applications tend to use III/V materials such as Gallium Arsenide (GaAs) or Gallium Nitride (GaN).

Gallium Arsenide

Gallium Arsenide presents higher performance than Silicon in terms of breakdown voltage, electrical velocity or thermal conductivity. GaAs pseudomorphic High Electron Mobility Transistors (pHEMT) is the most widely used technology for low to medium power applications. More complex - and expensive- than CMOS, pHEMT made possible the evolution of cellular telecommunications in the past 20 years. Like CMOS transistors, GaAs presents a low breakdown voltage and is not adapted to higher power levels.

Gallium Nitride

In the past two decades, high bandgap technologies such as Gallimum Nitride (GaN) or Silicon Carbide (SiC) have made their appearance in the RF market. GaN's high breakdown voltage greatly increases the maximum output power. Combined with the thermal conductivity of SiC, GaN on SiC HEMT is a perfect candidate to achieve high power, high efficiency. The large electrical velocity also allows for high current densities, which lead to smaller transistor periphery and thus higher cutoff frequency. On the downside, GaN's low electron mobility produce a relatively high knee walkout and current collapse phenomena. This results in a slow compressive characteristic and thus non-linear operation. GaN also presents strong trapping effects, leading to short and long term memory distortions. Finally, Gallium Nitride is still a more expensive technology as the ones previously presented.

So far, there has been a distinct separation in cellular protocols between high power base stations on one hand, using LDMOS transistors, and low power, GaAs based user equipment on the other. 5GNR defines a multitude of specifications for the different applications it encompasses, and we can expect to see a very high diversity of technologies. GaN HEMT's are slowly taking over in high power high frequency applications such as base stations. While GaAs still presents the highest performance in the mid-low power ranges, CMOS technologies allow integration of the power structure and control / intelligence circuits on the same die, drastically reducing complexity of more advanced systems. CMOS seems like a great candidate for cheap millimeter-wave, low power, high component density applications such as Massive MIMO.

1.4 Transistor Modelling

Computed Assisted Design (CAD) tools are a major contributor in the evolution of wireless technologies. They make possible the design of more complex systems and give access to the components intrinsic nodes, further understanding what is going on.

The Ideal Transistor

The ideal Field Effect Transistor (FET) is shown in figure 1.9. It is a Voltage Controlled Current Source (VCCS), whose output current i_{ds} is a function of the gate-to-source v_{gs} and drain-to-source

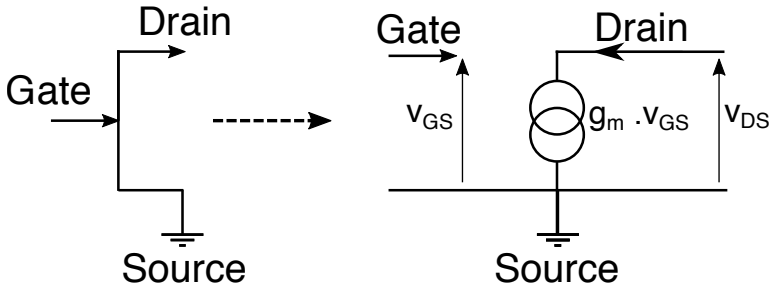


Figure 1.9: Symbol and simplified schematic of a Field Effect Transistor

v_{ds} voltages [3]. A very elementary model can be given by eq 1.12 separating the influence of v_{GS} and v_{DS} and using piece-wise linear expression: [1]:

$$i_{DS} = f(v_{DS}, v_{GS}) = f_{DS}(v_{DS}) f_{GS}(v_{GS}) \tag{1.12}$$

These two functions can be seen in figure 1.10 and are given by :

$$f_{GS}(v_{GS}) = \begin{cases} 0 & \text{if } v_{GS} < V_{Th} \\ g_m(v_{GS} - V_{Th}) & \text{if } V_{Th} < v_{GS} < V_{SAT} \\ I_{MAX} & \text{if } V_{SAT} < V_{GS} \end{cases} \tag{1.13}$$

$$f_{DS}(v_{DS}) = \begin{cases} v_{DS}/V_k & \text{if } 0 < v_{DS} < v_K \\ 1 + g_{ds}(v_{DS} - v_K)/I_{MAX} & \text{if } V_K < v_{DS} < V_{BR} \end{cases} \tag{1.14}$$

The threshold voltage V_{Th} is the minimum gate voltage required to turn-on the transistor. While v_{GS} is under V_{Th} the current i_{DS} is zero. When v_{GS} becomes bigger than V_{Th} the drain current rises, with a slope of the transconductance g_m, until it reaches the maximum current I_{MAX}, at $v_{gs} = V_{Sat}$. i_{DS} is also function of v_{DS}. While v_{DS} is smaller than the knee voltage V_K, the current rises linearly with v_{DS} up to a value determined by the gate voltage v_{GS}. This is the ohmic region, where the transistor acts like a resistor. When $v_{DS} > V_K$, the current has a much smaller dependency with v_{DS}, and varies with a slope of the output conductance g_{ds}. In this region the transistor acts like an almost ideal current source. V_{BR} represents the maximum drain voltage. $v_{DS} > V_{BR}$ can damage or break the device. Very often, for simplicity the terms V_K and g_{ds} are set to zero. The transistor then becomes a true current source, depending only on the gate voltage v_{GS}. Figure 1.11 shows the current i_{DS} as a function of v_{DS} for different values of v_{gs}. Fig. 1.11–(a) shows the normal case, while fig.1.11–(b) represents the simplified model with $V_K = g_{ds} = 0$.

The VCCS model is very basic and cannot be used in practice to design large signal power amplifiers. It is nevertheless realistic enough to be used as a start-point for the development of the theory behind the power amplifier architectures and modes of operation.

Non-Linear transistor Model

In reality a transistor is a very complex active device, made from the superposition of many layers of different materials. When using CAD tools, a much more accurate model has to be used. It takes

[1] We note for the rest of this thesis the following nomenclature : time domain signals will have lower case letter with upper case subscript (i_{DS}). DC components will have upper case letter and subscript (I_{DS}) and harmonic components will have upper case latter and lower case subscript (I_{ds})

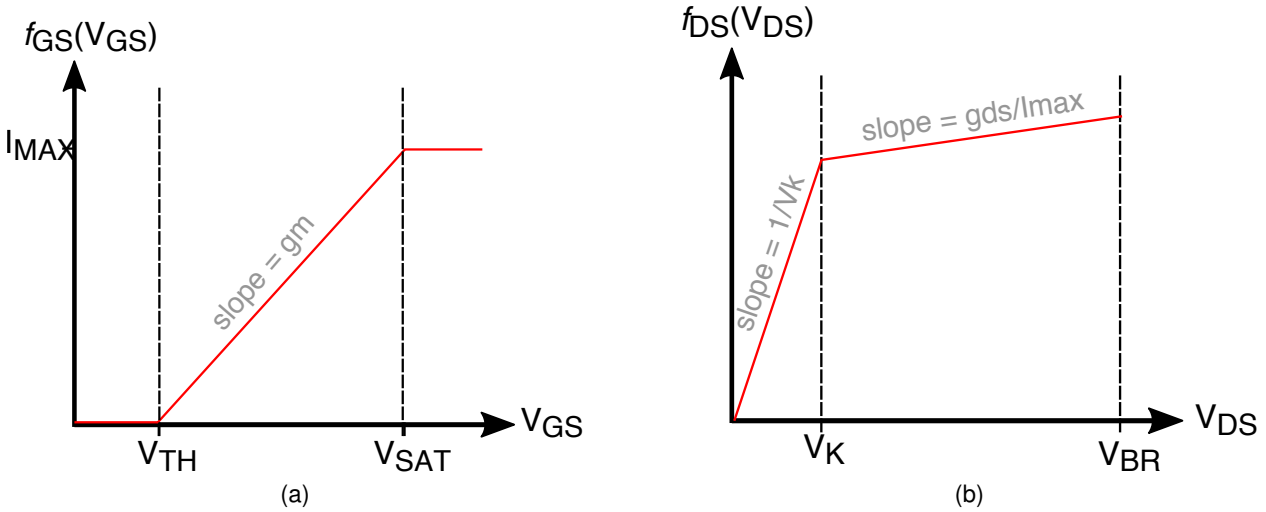


Figure 1.10: The two functions f_{GS} vs v_{GS} (on the left) and f_{DS} vs v_{DS} (on the right)

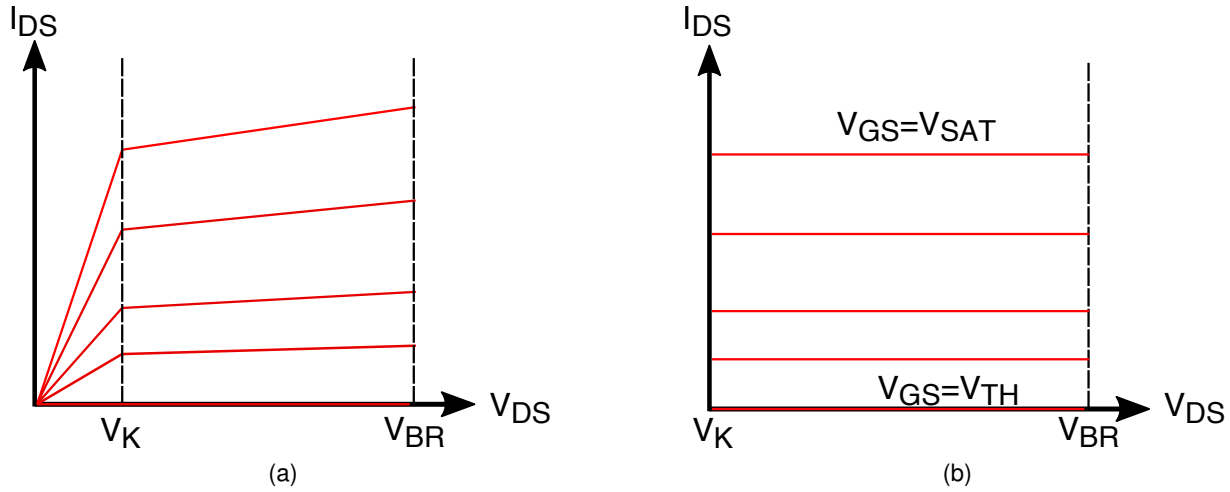


Figure 1.11: i_{DS} as a function of v_{DS}, in (a) including the knee voltage and output conductance, in (b) ideal VCCS model

into account both the physical parasitics, such as the access pads, and the various unwanted effects, such as trapping or thermal dissipation. Figure 1.12 is a schematic representing the non-linear model used by CREE for the CGH family of GaN on SiC transistors.

This is a physical driven behavioral model. The blue box represents the intrinsic transistor. We can see the voltage controlled current source, as well as the parasitic resistance and variable capacitance between the three transistor ports. These power-dependent capacitances are the main source of non-linearities in a transistor, and also limit the frequency range. The rest of the parasitics characterize either the physical access pads (here represented as lumped-component transmission lines) or the thermal effects. Most manufacturers offer their own transistor model. They usually are empirical closed-form models, based on equations rather than discrete components.

This model is particularly interesting, because it also give access to the drain current and voltage i_{DS}/v_{DS} at the intrinsic drain plane, which we will see later gives a lot of hindsight in what is actually going on with the device.

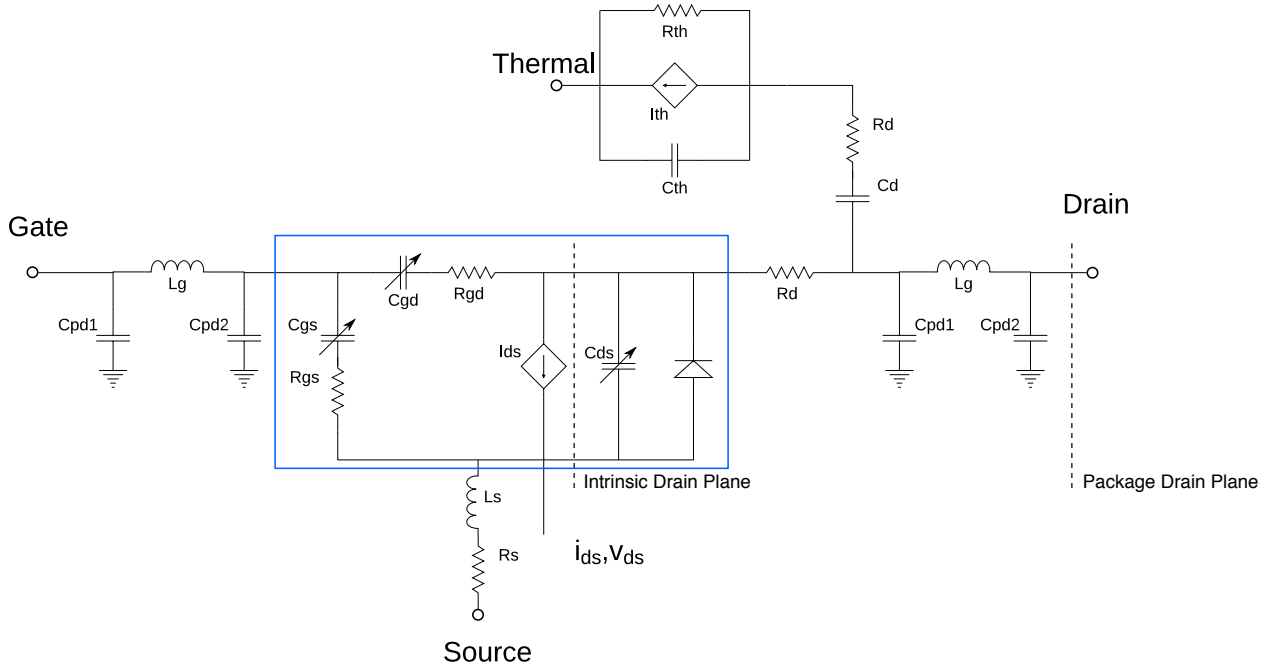


Figure 1.12: Non-Linear model of the CGH Transistors from CREE

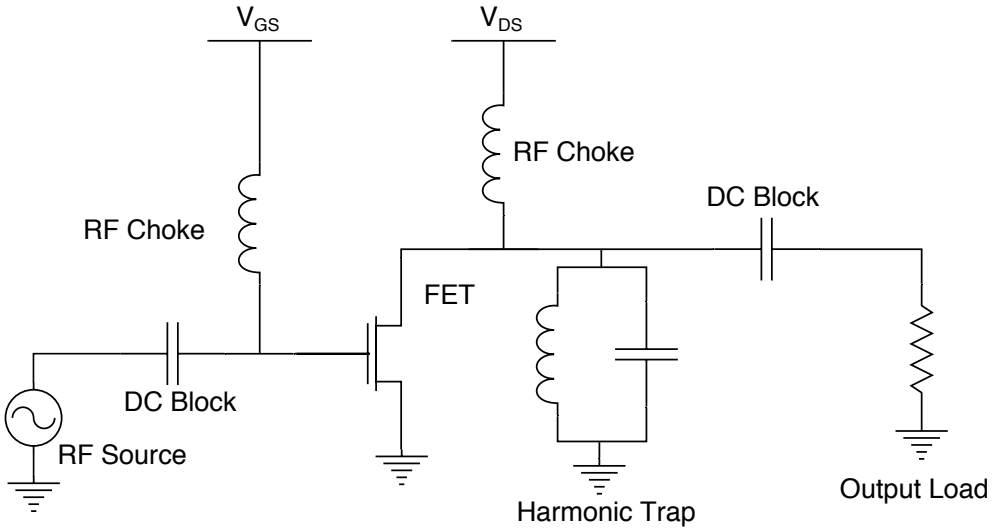


Figure 1.13: Conventional Transconductance Amplifier

1.5 Power Amplifiers Class of Operation

The conventional solid state power amplifier, also known as transconductance amplifier, is based on a Common Source (CS) configuration of a field effect transistor. The transistor's gate is chosen as the input and the drain as the output. Conventional PAs consider purely sinusoidal voltage waveforms. Figure 1.13 represents this transconductance amplifier.

The input gate voltage can be described as :

$$v_{GS} = V_{GS} + \beta V_{gs,max}\sin(\omega_0 t) \tag{1.15}$$

Where V_{GS} is the DC gate bias voltage, ω_0 the fundamental angular frequency, β the normalized

input drive level ($0 < \beta < 1$) and $V_{GS,max} = V_{SAT} - V_{GS}$ the maximum fundamental gate RF voltage swing. Depending on the value of V_{GS}, the transistor will not be conducting for the same duration of a cycle. We identify different classes of operation, with different characteristics, based on the value of the DC bias V_{GS}. They are usually identified from the conduction angle α, which represents in angular scale the relative time the transistor is conducting :

$$\sin\left(\frac{\pi - \alpha}{2}\right) = \frac{V_{Th} - V_{GS}}{V_{SAT} - V_{GS}} \tag{1.16}$$

- **Class A** : $\alpha = 2\pi$ or $V_{GS_A} = (V_{SAT} - V_{Th})/2$, the bias voltage is exactly in the middle between the threshold and saturation voltage. The RF voltage swing $V_{gs,max}$ is maximized and the transistor is always conducting. The output current is a pure sinusoid.

- **Class AB** : $\pi < \alpha < 2\pi$ or $V_{Th} < V_{GS_{AB}} < V_{GS_A}$, the bias voltage is between the threshold voltage and the class A bias. The input RF voltage swing goes under the threshold voltage, the output current can reach 0, the transistor is not always conducting.

- **Class B** : $\alpha = \pi$ or $V_{GS_B} = V_{Th}$, the bias voltage is equal to the threshold voltage. Half the time the input RF voltage is under the threshold voltage, and there is no current. The output current is a half-wave rectified sinusoid.

- **Class C** : $\alpha < \pi$ or $V_{GS_C} < V_{Th}$, the bias voltage is smaller than the threshold voltage. Most of the time the transistor is not conducting, and the output current is zeroed.

Figure 1.14 presents the output voltage and current waveforms and figure 1.15 the loadline associated with each class.

The class A and AB ($V_{GS} > V_{Th}$ or $\alpha > \pi$) time domain drain current i_{DS} can be expressed as :

$$i_{DS}(\beta, \beta_0) = \begin{cases} \frac{I_{MAX}}{1+\beta_0}(\beta \sin(\omega_0 t) + \beta_0) & \text{if } 2n\pi + \alpha_x \leq \omega_0 t \leq (2n+1)\pi - \alpha_x \\ 0 & \text{else} \end{cases} \tag{1.17}$$

where n is an integer, $\sin(\alpha_x) = -\frac{\beta_0}{\beta}$ and $\beta_0 = \frac{|V_{Th} - V_{GS}|}{V_{gs,max}}$. α_x is the angle for which v_{GS} reaches V_{Th} and β_0 the drive level for which v_{GS} first reaches V_{Th}. The conduction angle can be expressed as $\alpha = \pi - 2\alpha_x$.

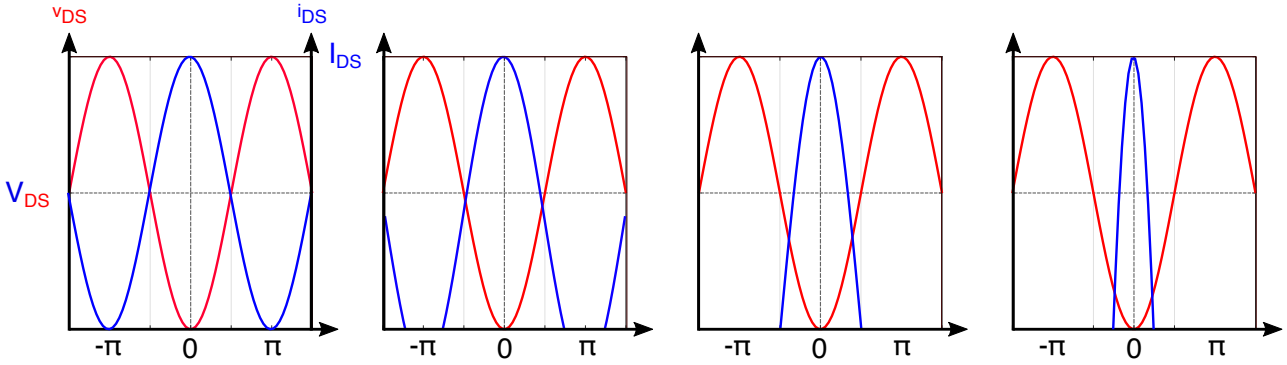


Figure 1.14: The voltage (in red) and current (in blue) waveforms at maximum drive for the different amplifier classes A-AB-B-C, from left to right.

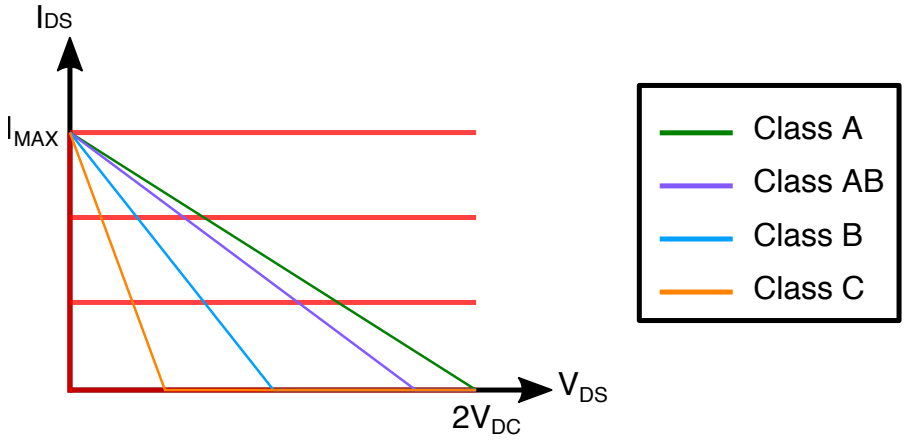


Figure 1.15: Loadline for the different classes of operation

For the Class B and C ($V_{GS} \leq V_{Th}$ or $\alpha \leq \pi$) we have :

$$i_{DS}(\beta,\beta_0) = \begin{cases} \frac{I_{MAX}}{1-\beta_0}(\beta\sin(\omega_0 t) - \beta_0) & \text{if } 2n\pi + \alpha_x \leq \omega_0 t \leq (2n+1)\pi - \alpha_x \\ 0 & \text{else} \end{cases} \tag{1.18}$$

Except for the class A, the output current is not purely sinusoidal, and thus presents harmonic components. We can study them by doing Fourier series expansion of the current i_{DS}.

For the class A/AB the DC, fundamental and harmonic components are given by :

$$I_{DS,DC}(\beta,\beta_0) = F_A Re\left\{\beta\sqrt{1-\frac{\beta_0^2}{\beta^2}} + \beta_0\pi - \beta_0\cos^{-1}\left(\frac{\beta_0}{\beta}\right)\right\}, \tag{1.19}$$

$$I_{ds,f_0}(\beta,\beta_0) = -jF_A Re\left\{\beta_0\sqrt{1-\frac{\beta_0^2}{\beta^2}} + \beta\pi - \beta\cos^{-1}\left(\frac{\beta_0}{\beta}\right)\right\}, \tag{1.20}$$

$$I_{ds,Nf_0}(\beta,\beta_0) = -F_A 2e^{-j\frac{n\pi}{2}} Re\left\{\beta\sqrt{1-\frac{\beta_0^2}{\beta^2}}\cos(N(\pi - \cos^{-1}\left(\frac{\beta_0}{\beta}\right)) + \right. \tag{1.21}$$

$$\beta_0\sin(N(\pi - \cos^{-1}(\frac{\beta_0}{\beta}))/N(N^2-1) \qquad Ha$$

with

$$F_A = \frac{I_{MAX}}{(\beta_0+1)\pi}$$

N represents the number of the harmonic. Similarly, we can express the different Fourier transform components for the class B/C cases :

(1.22) $$I_{DS,DC}(\beta,\beta_0) = F_B Re\left\{-\beta\sqrt{1-\frac{\beta_0^2}{\beta^2}}+\beta_0\cos^{-1}\left(\frac{\beta_0}{\beta}\right)\right\},$$

(1.23) $$I_{ds,f_0}(\beta,\beta_0) = -jF_B Re\left\{\beta_0\sqrt{1-\frac{\beta_0^2}{\beta^2}}-\beta\cos^{-1}\left(\frac{\beta_0}{\beta}\right)\right\},$$

(1.24) $$I_{ds,Nf_0}(\beta,\beta_0) = F_B 2e^{-j\frac{n\pi}{2}} Re\left\{\beta\sqrt{1-\frac{\beta_0^2}{\beta^2}}N\cos(N\cos^{-1}\left(\frac{\beta_0}{\beta}\right)+\right.$$
$$\left.\beta_0\sin(N\cos^{-1}\left(\frac{\beta_0}{\beta}\right)/N(N^2-1)\right.$$ $Hallbe$

with

$$F_B = \frac{I_{MAX}}{(\beta_0-1)\pi}$$

Looking back at figure 1.13, we see that the voltage across the output load is always a pure sinusoid, since the DC block and harmonic trap eliminate all the other components. In order to maximize its swing value, the drain bias voltage V_{DS} is selected as :

(1.25) $$V_{DS} = \frac{V_{BR}+V_K}{2}$$

And the fundamental voltage is

(1.26) $$v_{DS} = V_{DS} + \beta V_{ds,f0,max}\cos(\omega_0 t)$$

where $V_{ds,f0,max} = V_{DS} - V_K$. The transistor being modeled as a current source, the optimal impedance is chosen in order to maximize the RF voltage swing at maximum power, i.e. $\beta = 1$. This impedance was defined in (1.8).

Now that both the voltage and current at the transistor's drain are completely defined we can estimate the theoretical maximum output power and efficiency for different conduction angles. The drain efficiency is defined as the ratio of the fundamental RF power to the DC power :

(1.27) $$P_{ds_{f0}}(\beta) = \frac{1}{2}Re\{V_{ds,f0}(\beta)I_{ds,f0}(\beta)^*\}$$

(1.28) $$P_{DC}(\beta) = V_{DS}I_{DS}(\beta)$$

(1.29) $$\eta = \frac{P_{ds_{f0}}(\beta)}{P_{DC}(\beta)}$$

The gain can also be calculated versus the conduction angle, using (1.15)–(1.16) to estimate the input power with $V_{Th} = 0$ and $V_{Sat} = 1$:

(1.30) $$Gain = \frac{P_{ds_{f0}}(\beta)}{P_{gs_{f0}}(\beta)}$$

Finally, the Power Usage Factor (PUF) is defined as the ratio of the fundamental output power to the fundamental output power of the class A bias

(1.31) $$PUF = \frac{P_{ds_{f0}}(\beta=1)}{P_{ds_{f0,ClassA}}(\beta=1)}$$

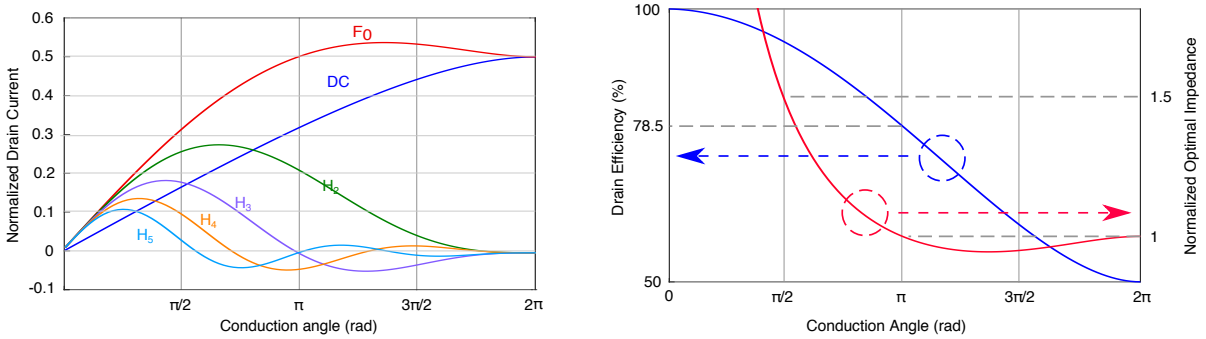


Figure 1.16: On the left the different harmonic components of Ids, on the right in red the drain efficiency and in blue the optimal impedance normalized to the class A impedance

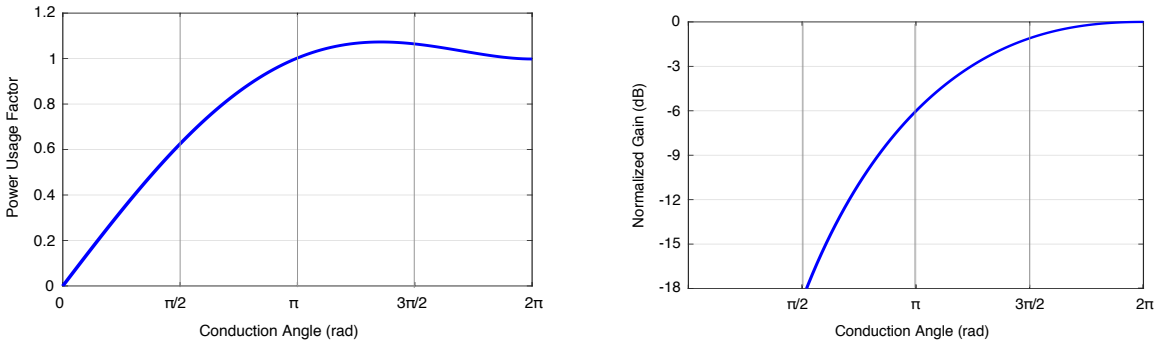


Figure 1.17: On the left the Power Usage Factor, on the right the relative gain

Figures 1.16 – 1.17 illustrate the different equations versus the conduction angle at maximum power. Figure 1.16.(a) shows the DC, fundamental and harmonic components of the drain current i_{DS}, normalized to the maximum current I_{MAX}. Figure 1.16.(b) presents in blue the theoretical drain efficiency and in red the required output impedance. 1.17.(a) shows the Power Usage Factor and 1.17.(b) the normalized gain relative to the gain of the class A. We can draw a certain number of conclusions based on these considerations :

- The drain efficiency goes from 50% for the class A amplifier up to a theoritical 100% in the deep class C. In practice a conduction angle of zero results in zero output power, illustrating that 100% efficiency cannot be achieved with that approach.
- Maximum power is attained in deep class AB ($\alpha = 5\pi/4$) and classes A and B have the same output power. Class C ($\alpha = \pi/2$) has 2 dB lower output power than classes A/B.
- The gain is maximized at class A and drastically lowers as the conduction angle changes. Classes B and C have respectively 6 and 18 dB lower gain than class A.
- Class A has no harmonic components, while class B has a very strong second harmonic. Only classes AB and C have third harmnonics, and they are in opposit sign.

In summary, Class A is presents most linear operation, as no harmonic components are present in the current waveform. On the other hand class A also has the lower efficiency. Class B reaches the same output power level with a much higher drain efficiency (78.5%), at the cost of 6 dB lower gain and second harmonic components[18]. Class C has even higher drain efficiency, but the cost

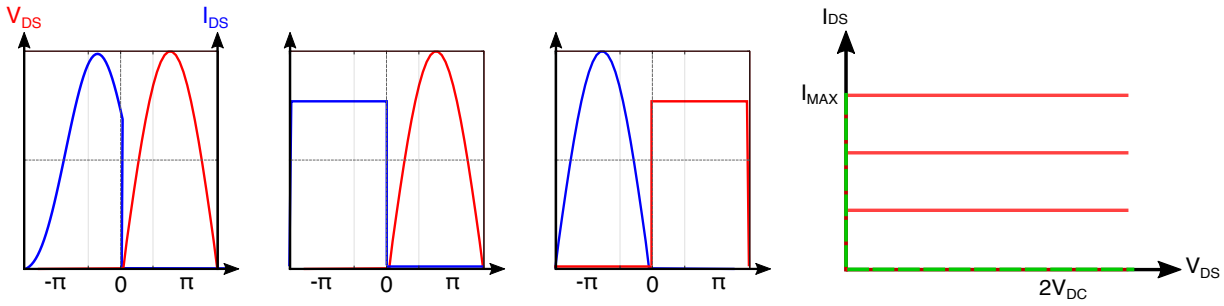


Figure 1.18: Switched Mode Power Amplifier waveforms, from left to right class E, F, F^{-1}. On the right the load line associated with SMPAs

in terms of gain and output power becomes great. The choice of the class of operation depends on the PA requirements. Most often power amplifiers are biased in class AB, in a compromise between efficiency, linearity and output power. We usually identify some sweet spots, where the different trade-offs are maximized. We note that this formulation is very idealized and based on some assumptions that we know are false, such as $V_K = 0$. The current waveform was also assumed to be half-wave rectified, with a very sharp turn-on.

Switched Mode Power Amplifiers

The drain efficiency of a power amplifier can be expanded as :

$$\eta = \frac{P_{L_{f0}}}{P_{L_{DC}}} = \frac{P_{L_{DC}} - P_{diss}}{P_{L_{DC}}} = \frac{I_{DS} * V_{DS} - \int_0^{2\pi} i_{DS}(\theta) v_{DS}(\theta) d\theta}{I_{DS} * V_{DS}} \tag{1.32}$$

We understand that power is dissipated when the voltage and current overlap, according to the factor $\int_0^{2\pi} i_{DS}(\theta) v_{DS}(\theta) d\theta$. Looking back at figure 1.14, we see that as we go from class A to class C, the current i_{DS} becomes more and more narrow, decreasing the cross-over region. Pushing this argument further, we understand that 100% drain efficiency can be achieved if the voltage and current never cross each-other. This is the concept behind Switched Mode Power Amplifiers (SMPA).We can distinguish two types of SMPAs : hard switching and soft switching architectures.

The hard-switching SMPAs include the class D and E power amplifiers. The transistor is modeled as an ideal switch, over-driving its input to reach rail to rail operation. It is assumed as an open circuit during the OFF state and as a close circuit during the ON state. The time required to transition between the two is theoretically zero. Class D is widely used in audio amplifiers. It is composed of two transistors organized in a push-pull configuration. The resulting waveforms are a square voltage and sinusoidal current. In practice the drain-source capacitance C_{DS} is a limiting factor as it greatly increases the switching time. Class-D amplifiers are very rarely used in high frequency circuits. Class E on the other hand is more common, as it uses the C_{DS} in its advantage and is composed of a single transistor. By presenting the correct harmonic impedances, ideal switching can be achieved even at very high frequencies. The almost perfect DC to RF conversion of the class E amplifier is counter-balanced by its very poor PUF.

Soft switching architectures are based on a linear transconductance amplifier biased in class B. The goal of Class F is to have a square output voltage, instead of a pure sinusoid, resulting is zero overlap of the current and voltage waveforms. To do so, an infinite number of even and odd harmonics need to be presented with an open-circuit – closed-circuit respectively, in order to shape the waveform. F^{-1} is the dual of class F, where the voltage is shaped into a half-wave rectified sinusoid and the current is squared. It is achieved by interchanging the harmonic terminations. In

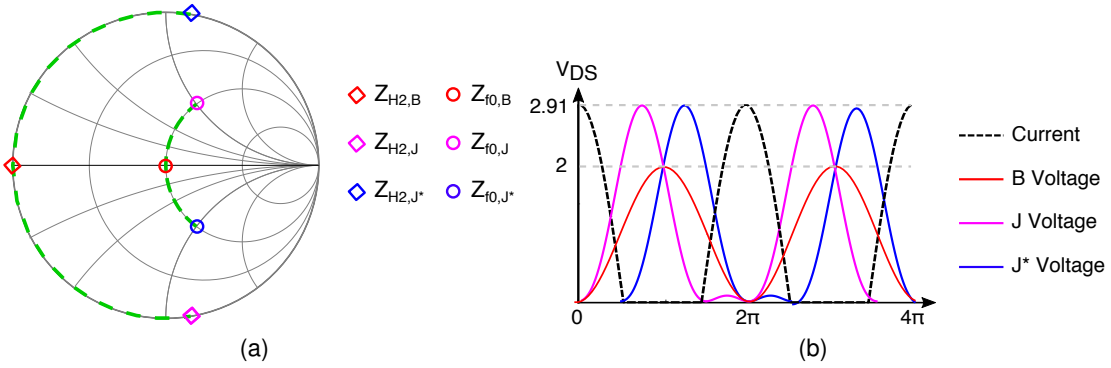


Figure 1.19: (a) Continuous Modes impedance design space. In circles and squares the fundamental and second harmonic impedances for the J/B/J* cases. (b) Voltage and current waveforms for the J/B/J* cases.

practice, the transistor's C_{DS} short-circuits most of the harmonic components. Only the second and third harmonic can be realistically manipulated. Still, Class F amplifiers have been shown to present higher efficiencies than Class B, reaching measured 81.65% drain efficiency, with similar PUF.

The different waveforms associated with the switching mode power amplifiers can be seen in figure 1.18. A drawback associated to harmonic manipulation is the overshoots that occur to the voltage and current waveforms. In the case of the class F amplifiers, the RF drain voltage is 1.57 times bigger than in conventional class B. Depending on the technology of the transistor this can be a limiting factor, as the over-voltage can damage or break the device. Specific harmonic terminations and mixed E-F modes can mitigate this voltage overshoot [19].

Harmonically tuned Power Amplifiers

Looking back at equation (1.8), we understand that in conventional transconductance power amplifiers the optimal impedance R_{opt} is purely real. This reflects the fact that the drain voltage and current waveforms v_{DS}–i_{DS} are exactly out of phase. In fact, so far only the class E amplifier assumed a complex fundamental impedance, materialized here by the C_{DS}. Along with the purely real optimal impedance, the previous classes also assumed perfect RF opens or shorts at the various harmonics. This is a difficult condition to realize in practice over a wide frequency range, and is a limiting factor in wideband designs.

Following the idea of the class E amplifier, that uses the C_{DS} to its advantage, Pr. Cripps showed in [11] that in some cases a complex fundamental impedance could be presented to a class B biased amplifier while keeping identical performance in terms of output power and efficiency. This complex impedance produces a phase shift between the voltage and current waveforms, and thus a larger overlap. In turn, this results in an efficiency degradation. However, adequate shaping of the voltage waveform, achieved by reactively terminating the second harmonic impedance, can retrieve the original efficiency. It was further shown in [20] that one could define a whole range of solutions, based on a redefinition of the drain voltage :

$$v_{DS_{B/J}}(\omega_0 t) = V_{DS}(1 - \cos(\omega_0 t))(1 - \delta \sin(\omega_0 t)) \tag{1.33}$$

Where δ is a design parameter that determines the quadrature component of v_{DS}. It ranges from -1 to 1, and actually creates a continuum of solutions that give -in theory- identical performance in

terms of output power and efficiency. $\delta = 0$ corresponds to the class B amplifier, while $\delta = 1$ or -1 are called J/J* respectively.

Equation (1.36) can be further expanded :

$$v_{DS_{B/J}}(\omega_0 t) = V_{DS}\left(1 - \cos(\omega_0 t) - \delta\sin(\omega_0 t) + \delta\frac{\sin(2\omega_0 t)}{2}\right) \tag{1.34}$$

Assuming the current to be the same half-wave rectified class B current from (1.17), we can find the required impedances at fundamental ($Z_{B/J_{f0}}$) and second harmonic frequency ($Z_{B/J_{H2}}$) for the continuous modes operation :

$$Z_{B/J_{f0}} = \frac{V_{ds_{f0}}}{I_{ds_{f0}}} = R_{opt}(1 + j\delta) \tag{1.35}$$

$$Z_{B/J_{H2}} = -j\delta\frac{3\pi}{8}R_{opt} \tag{1.36}$$

Where R_{opt} is the class B optimal impedance. Figure 1.19.(a) shows on the Smith chart the fundamental and harmonic impedances for δ equal to 0, 1 or -1. In green we can see the trajectory taken by these impedances when we sweep δ. Figure 1.19.(b) presents the voltage and current waveforms for the Class J/B/J*. This figure can help to understand how the same power and efficiency can be obtained throughout the continuum. The J and J* voltage waveforms are phase shifted compared to the class B. If the waveform was still sinusoidal (ie no harmonic component), this would result in a greater overlap with the current, and thus lower efficiency. By accordingly terminating the second harmonic, the waveform is engineered to minimize the overlap. The voltage overshoot is also important in order to retrieve the same output power.

The continuous modes concept is very interesting as it allows very wideband operation [21]. An adequate output matching network can present an impedance that goes from capacitive reactive (class J*) to purely real (class B) and then inductive reactive (class J) throughout the fundamental band, and with the correct second harmonic for each case, reaching identical power and efficiency for the whole band [20]. Multiple research also shows that harmonic tuning can find specific sweat-spots that maximize the amplifier performance [22].

The continuous modes concept can be applied to all classes of operation. We can distinguish the continuous F and F^{-1}, which lead to very wideband and highly efficient single-ended amplifiers or the even more efficient (but less linear) E-F continuums. Recently a class C continuum was derived for wide-band Doherty amplifiers [23].

1.6 Conclusion

In this chapter, the fundamental theory of RF Power Amplifier Design was presented. After looking at the main characteristics of a PA (Gain, Efficiency or linearity), some practical considerations were exposed, like the load-pull measurements or digital predistortion. A brief presentation of the different transistor technologies and the corresponding modeling techniques was then addressed. Finally the different modes of operation were mathematically derived, looking at the advantages and drawbacks of each of them.

The question of efficiency requires a more thorough study, as it was only presented at maximum power, ie when the voltage and current swings are maximized. If we take for example the class B case, we can further expand the equation (1.29) :

$$\eta(\beta) = \frac{P_{L_{f0}}(\beta)}{P_{L_{DC}}(\beta)} = R_{opt}\frac{(\beta I_{DS})^2}{4}\frac{\pi}{V_{DS}\beta I_{DS}} = \frac{\pi}{4}\frac{\beta V_{DS}\beta I_{DS}}{V_{DS}\beta I_{DS}} = \frac{\pi}{4}.\beta \tag{1.37}$$

Where β is the normalized drive level. In other words, the efficiency of the power amplifier is directly proportional to its drive level, and reaches the theoretical 78.5% only at maximum drive. At 3dB back-off ($\beta = \sqrt{2}$), the efficiency is down to 55.5% and at 9 dB ($\beta = 1/\sqrt{8}$) back-off, it is only 27.75%. Recalling what was said in the introduction, a power amplifier's average power needs to be back-off from the maximum power by the same amount as the PAPR of the modulated signal. With complex modulations such as LTE or 5GNR, the single-ended transistor presents extremely small efficiencies. More complex architectures are therefore unavoidable in order to reach the very stringent linearity and efficiency requirements of modern communication standards.

Chapter 2

Efficiency Enhanced Power Amplifier Architectures

Looking back at (1.37), the dependency of the efficiency to the drive level comes from the fact that the RF and DC voltage do not scale similarly. We understand that if one or the other came to vary differently, maximum efficiency could be kept independently of the output power level. One approach to enhance the back-off efficiency comes from dynamically changing the output impedance, such as $R_{out} = R_{opt}/\beta$, β being the normalized drive level, between 0 and 1. That way the RF voltage swing remains constant, equal to the DC drain bias, and the efficiency stays maximal. This concept is called **Load Modulation (LM)**. This variable impedance can be synthesized either with a tunable matching network or through asymmetrical operation of two or more non-isolated amplifiers. Another approach to high efficiency operation is **Supply Modulation (SM)**, which consists on dynamically changing the DC drain bias. That way V_{DS} is always adapted to be equal to the RF voltage swing $V_{ds,f0}$, keeping high efficiency independently of the output power. The most common SM architecture is Envelope Tracking amplifiers. An envelope tracker detects the input signal's amplitude and automatically adapts the drain bias voltage. The gate bias is often also tuned, but this technique is more focused on linearity enhancement.

Figure 2.1 shows the loadline associated with each approach. In very few words, high efficiency is obtained when the RF voltage swing reaches the DC drain bias voltage, independently of the RF current.

In this chapter, a review of the different high efficiency architectures is provided. The concepts and principal architectures of Supply and Load Modulation amplifiers are presented, as well as a comparison of their respective advantages and drawbacks. In the end of this chapter more advanced techniques are presented.

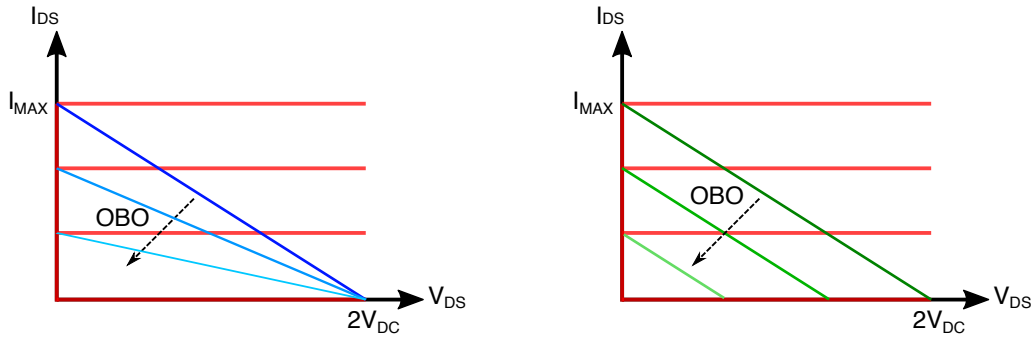


Figure 2.1: Loadline associated with High Efficiency Architectures : on the left Load Modulation, on the right Supply Modulation

2.1 Supply Modulation Architectures

Envelope Restoration

Supply Modulation relies on adapting the drain or gate bias voltage to the input signal's envelope. The first version of SM was the Envelope Elimination and Restoration (EER), proposed by Kahn in 1952 for the amplification of Single SideBand modulations (SSB) [24]. The SSB modulation is somewhat the ancestor of modern digital communications, as information is coded both on the amplitude and phase of the RF signal. EER consists on creating two separate signals : one with constant amplitude and variable phase, and another, containing only the voltage envelope. The constant amplitude RF signal is fed into a very high efficiency amplifier, for example switched-mode class E PA. The envelope can be restored at the output using a conventional voltage supply modulator, resulting in a linear amplification of the original signal.

Figure 2.2.(a) shows the concept of Envelope Elimination and Restoration. Modern approaches simplify this architecture by doing the signal separation digitally. The resulting Polar Transmitter [25], presented in figure 2.2.(b), consists of an Envelope Amplifier (EA), amplifying the baseband envelope signal and the very efficient saturated Power Amplifier. Feedback loops can also be implemented for linearity considerations. The efficiency of envelope restoration techniques depends mainly on that of the envelope amplifier, associated with the dynamic power supply. In practice, it is very difficult to have an efficient power supply that has a large enough dynamic voltage range. In particular, low powers are very difficult to implement. The required time alignment precision is another limiting factor, as small delays strongly degrade the system's linearity.

Envelope Tracking

Envelope Tracking (ET) is inspired from the previous techniques. Like with EER, the drain bias of the power amplifier is adapted to follow the envelope of the input system. The main difference here is that the power amplifier is now linear, and is fed with the original, phase and amplitude modulated signal. One of the great advantages of envelope tracking is that the modulation control voltage does not have to replicate the original envelope with great accuracy, as it is already present in the PA's output. The previous problems of EER such as zero voltage crossing are alleviated, as low power can be achieved by small input signals, even with a fixed drain bias. The time alignment is also not as important in ET systems.

The key component in envelope tracking amplifiers is the envelope amplifier. The presence of the original envelope on the PA's output gives great flexibility in the choice of the EA's architecture.

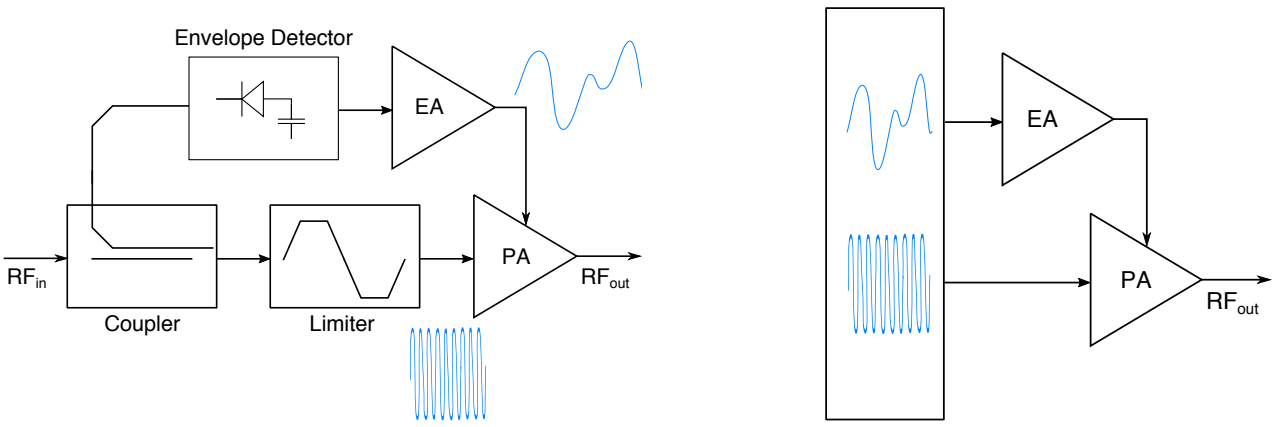


Figure 2.2: (a) Envelope Elimination and Restoration (b) Polar Transmitter

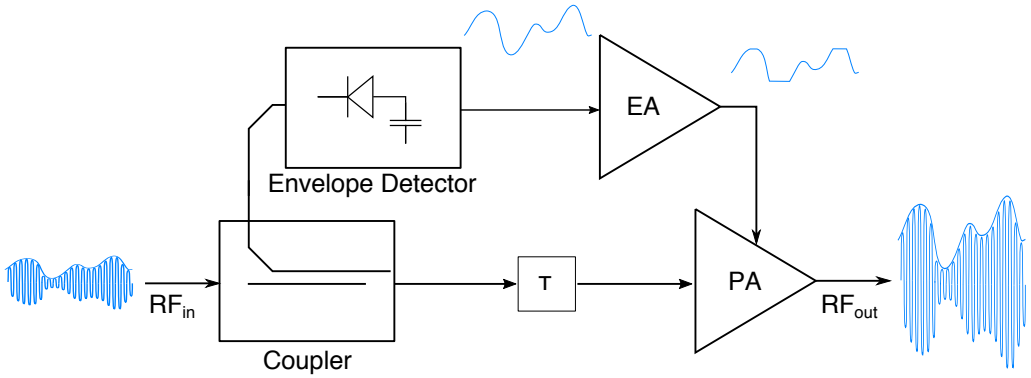


Figure 2.3: Power Amplifier with Envelope Tracking

It can be synthesized with a mix of analog and digital circuits, such as a switching power supply along with an analog regulator. In [26] a switching amplifier provided the low frequency component of the envelope with high efficiency while the linear amplifier provided the high frequency part at very high speeds, reaching 20 MHz bandwidths. Another approach is to provide discrete supply voltages, and switch between them. In [27], over 40% PAE was achieved at 6 dB back-off with a 50MHz bandwidth noise-like signal and a Discrete Supply Modulator (DSO). This is the concept behind Class G amplifiers. In handset devices, the lower complexity Average Power Tracking (APT) is used extensively. It consists on slowly adapting the drain voltage –and thus average output power– of a PA depending on the required performance, in order to adapt the overall power consumption.

Though very efficient, envelope tracking amplifiers suffer from linearity issues and present limited instantaneous bandwidths. Linear envelope amplifiers have trouble with baseband bandwidths larger than some tens of MHz. Discrete Supply modulators can work with wider bandwidth signals but degrade very strongly the overall linearity. Complex digital predistortions have to be implemented in order to keep the linearity requirements.

Today Envelope Tracking amplifiers get more and more attention for future base-station applications. In fact, extensive research is done to combine ET and load modulated amplifiers. In [2] the authors present a supply-modulated load-modulated amplifier with digital predistortion, reaching -52 dBC ACLR and 42% PAE with a 10 dB PAPR, 100 MHz signal. While complex, this architecture does not require exceptional calibration or time-alignment, and can be a good candidate for high power, wide band systems like 5G NR base stations.

2.2 Conventional Load Modulation Architectures

Load modulation can be considered as the dual of supply modulation. Instead of adapting the DC bias to the RF voltage, the RF voltage is kept constant, equal to the DC bias. Load Modulation amplifiers reach high efficiency by modulating the impedance seen at the transistor's drain, in order to achieve an RF voltage that is independent of the required output power.

We can distinguish two families of Load Modulated Amplifiers, depending on the load variation mechanism :

- **Dynamic Load Modulation (DLM)** : a reconfigurable matching network dynamically tunes the output impedance to preserve high efficiency
- **Active Load Modulation** : two or more transistors are connected with a non-isolating power combiner. Through asymmetric operation in amplitude and/or phase, each device modulates the impedance seen by the other, thereby tracing a load trajectory that maintains efficiency.

Dynamic Load Modulation

The most obvious approach to load modulation is the so-called Dynamic Load Modulation (DLM). It was first introduced in 2003 by Raab in [28]. In this paper the author presented an EER-like system, where the drain bias was fixed and the envelope was restored by dynamically tuning a MOSFET varactor on the output of a class E power amplifier. Modern DLM looks more like Envelope Tracking. The basic principle is to track the input signal's envelope and use one or multiple variable components to physically change the output load. For each input power level, the tunable matching network (TMN) will be reconfigured, in order to present the optimum impedance, reaching maximum efficiency for large power back-off. Figure 2.4 presents the basic concept of Dynamic Load Modulation. The capacitance of the reconfigurable element(s) is tuned by a high speed low power voltage amplifier. In contrast to supply modulation architectures, the overall efficiency of a DLM amplifier depends only on the power amplifier itself, as there is negligible power dissipated in the reconfigurable component. The tunable matching network can also be used to compensate for output impedance mismatch or for frequency reconfigurability. All these advantages make DLM a very promising power amplifier architecture for intelligent, reconfigurable transmitters.

The tunable matching network is a reconfigurable three port device, that transforms the output impedance to the optimal drain impedance. It is based on a reconfigurable component, usually a solid-state varactor. Extensive research is done to find optimum TMN configurations [29]. Most DLM architectures are based on two or more variable components, resulting in high complexity as separate drivers are required for each varactor. In [28] it was shown that by using a class E amplifier, a single varactor control could be achieved. Similarly, in [30] a class J amplifier was designed to require a purely reactive load modulation, making it possible again to realize the DLM with a single varactor. The resulting amplifier reached 45% PAE at 8 dB back-off at 2.09 GHz. In [31], a dual band PA based on a single element DLM is presented. It reached 61% PAE at 6 dB back-off both at 0.685 and 1.84 GHz. More recently, [32] investigated the required DLM mechanisms for wideband operation. More than 40% PAE was achieved at 6 dB back-off from 1.8 to 2.2 GHz with a single tunable element.

The variable element of DLM can also be based on switching between different states. In [33], a pulsed dynamic load modulation is presented, where an output switch changes from two different states at very high speed. The duty cycle of the switching defines the presented output impedance. The paper presents 43.3% PAE at 6 dB back-off with a 10 MHz LTE signal at 0.837 GHz. However, the linearity of the system is very poor as even after DPD measured ACLR where higher than -32.5 dBc.

More generally, linearity is the major drawback of DLM. Looking back at equation (1.37), we see that if the RF drain voltage is no longer dependent on β, the output power becomes proportional to β, while the input power is still proportional to β^2. A 6 dB increase of the input power results in a 3 dB

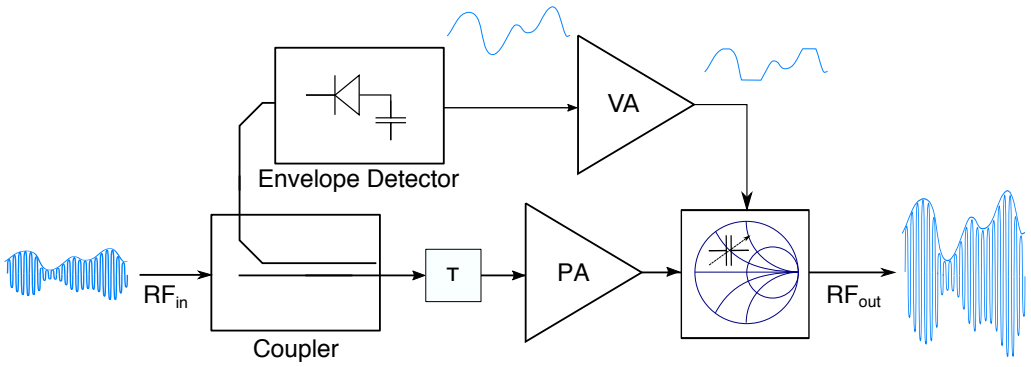


Figure 2.4: Dynamic Load Modulation

increase of the output power. The tuning speed is also a limiting factor, as varactors are bandwidth limited components. State-of-the-arts DLM amplifiers present limited linearity with only 3.4 MHz signals and digital predistortion [31]. For the moment, tunable matching networks are mainly used in a static manner, in reconfigurable power amplifiers or antenna tuners.

Active Load Modulation

As opposed to DLM, active load modulation does not require a reconfigurable component. The impedance variation is achieved here through the mutual interaction of one or more power amplifiers. The concept of Active Load Modulation (ALM) can be seen on figure 2.5. Looking at 2.5.(a), the impedance seen by the current source I_1 is equal to :

$$Z_1 = \frac{V_1}{I_1} = R_1 \tag{2.1}$$

If a second current source is injecting a current I_2 in the same resistance, the voltage V_1 will rise. Looking at figure 2.5.(b), the impedance seen by the current source I_1 has changed :

$$Z_1 = \frac{V_1}{I_1} = R_1 \frac{I_1 + I_2}{I_1} = R_1 \left(1 + \frac{I_2}{I_1}\right) \tag{2.2}$$

The impedance seen by the first current source is modulated by the current injected from the second source. Active load modulation amplifiers exploit this mechanism to achieve high efficiency over a wide dynamic range. Connecting together two or more power amplifiers with a non-isolating combiner, each device will modulate the impedance seen by the other. This is the mechanism behind the most famous high efficiency architectures : the Doherty Power Amplifier (DPA) or the Outphasing Power Amplifier (OPA), also known as Chireix Power Amplifier.

Doherty Power Amplifier

The Doherty Power Amplifier is by far the most widely used high efficiency architecture. It was invented in 1936 by William H. Doherty to achieve simultaneous high efficiency and high linearity for kilowatt radio transmitters. In its simplest form -yet still very used today-, no digital control or external component is needed to achieve high back-off efficiency. It is composed of two power amplifiers,

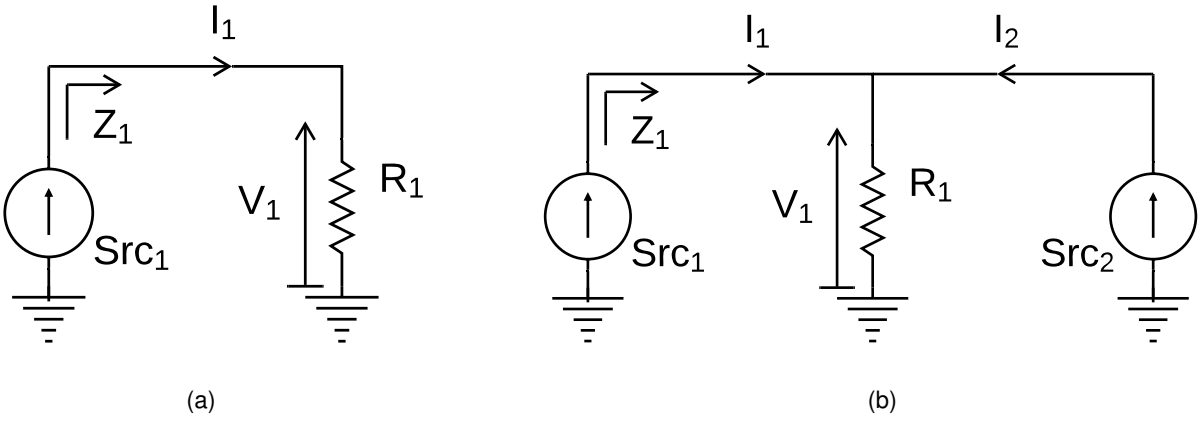


Figure 2.5: Active Load Modulation mechanism

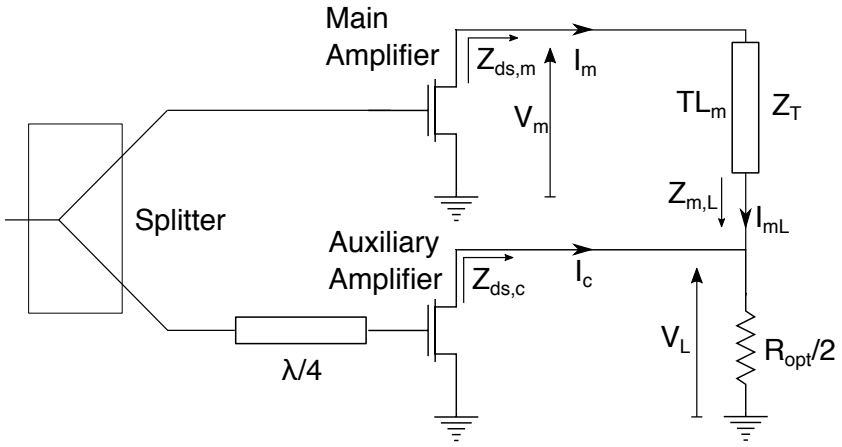


Figure 2.6: Conventional Doherty Power Amplifier

referred to as the Main and Auxiliary amplifier, connected together through a non-isolating combiner. The DPA attempts to generate two high efficiency points, one at a given back-off power P_{OBO}, and the other at maximum power. The Doherty operation can be separated in two regions :

- **Low-Power region :**$P_{out} < P_{OBO}$: In the low power region the auxilary amplifier is turned-off. The main amplifier, usually a regular class B PA, sees a certain drain impedance $Z_{ds,m} = Z_{opt}/\beta_0$. Z_{opt} is the optimal impedance at maximum power, defined in (1.8), and β_0 is referred to as the breakpoint and is related to the output back-off range (OBO). When the normalized input drive voltage β reaches β_0, the RF voltage swing reaches its maximum value, and the PA starts compressing. It has achieved maximum efficiency.

- **Doherty region** : The Auxiliary amplifier is designed to turn on and start conducting when $\beta = \beta_0$. It will inject a second current inside the combiner, and the impedance seen by both the main and auxiliary amplifier will decrease. The output power of the main amplifier will increase as the impedance decreases, while keeping very high efficiency. As β reaches 1, both the main and auxiliary amplifiers will reach maximum power, and a second efficiency peak is achieved.

Figure 2.6 presents a conventional Doherty power amplifier. W.H. Doherty derived this architecture for a 6 dB back-off [34], which can be translated into β_0 = 0.5. In the conventional DPA, the main and auxiliary amplifiers are identical, and deliver at maximum power the same current. The auxiliary amplifier is biased in class C, in order to stay off until $\beta = \beta_0$. Looking back at equation (2.2), we see that in order for the impedance at the main amplifier's drain to decrease, an impedance inverter is necessary, materialized by a quarter wave-length line. Mathematically, the impedance seen by the main ($Z_{ds,m}$) and auxiliary amplifier ($Z_{ds,c}$) and the impedance Z_{mL} seen at the output of the transmission line TL_m can be expressed as :

$$Z_{ds,m} = \frac{Z_T^2}{Z_{mL}} \tag{2.3}$$

$$Z_{ds,c} = \frac{R_{opt}}{2}\left(1 + \frac{I_{mL}}{I_c}\right) \tag{2.4}$$

$$Z_{mL} = \frac{R_{opt}}{2}\left(1 + \frac{I_c}{I_{mL}}\right) \tag{2.5}$$

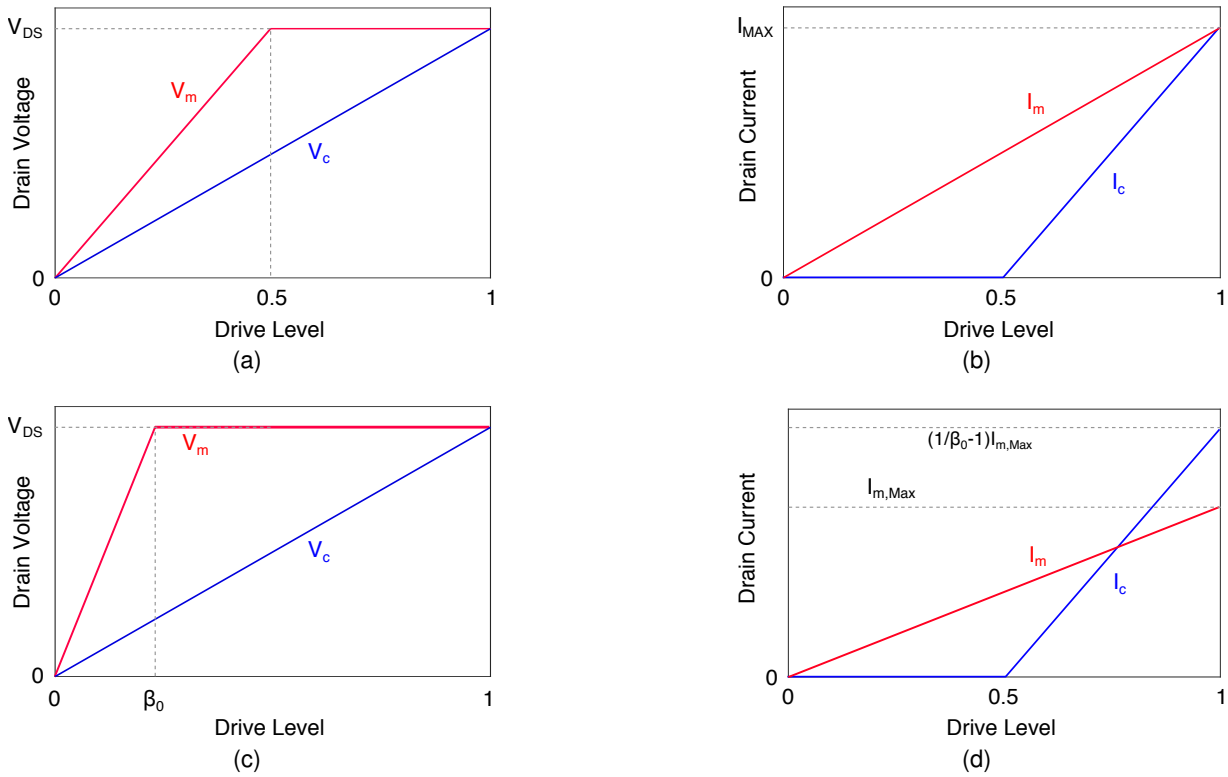


Figure 2.7: (a)Voltage and (b)current profiles for the main (red) and auxiliary (blue) transistors of a 6 dB Doherty Power Amplifier. In (c) and (d) for an arbitrary output back-off.

Where Z_T is the impedance of the transmission line TL_m and R_{opt} the optimal impedance at peak power. The subscripts m, c and mL refer to the main and auxiliary amplifiers and the output load respectively. Referring to the fundamental equations of a quarter-wave length transmission line,

$$I_{mL} = \frac{V_m}{Z_T} \tag{2.6}$$

Substituting (2.6) in (2.5) and choosing $Z_T = R_{opt}$,

$$Z_{ds,m} = R_{opt}\left(2 - \frac{I_c}{I_m}\right) \tag{2.7}$$

$$Z_{ds,c} = R_{opt}\frac{I_m}{I_c} \tag{2.8}$$

In the low power region, the auxiliary amplifier is turned off, resulting in $I_c = 0$. The impedance seen by the main amplifier is $Z_{ds,m} = 2R_{Ropt}$. At $\beta = \beta_0$, the RF power $P_{L,f0}$, DC power $P_{L,DC}$ and drain efficiency η can be computed as :

$$P_{L,f0}|_{\beta=\beta_0} = R_{ds,m}\frac{(\beta_0 I_{DS})^2}{4} = R_{opt}\frac{I_{DS}^2}{8} = \frac{V_{DS}I_{DS}}{8} \tag{2.9}$$

$$P_{L,DC}|_{\beta=\beta_0} = \frac{\beta_0 V_{DS}I_{DS}}{\pi} = \frac{V_{DS}I_{DS}}{2\pi} \tag{2.10}$$

$$\eta|_{\beta=\beta_0} = \frac{\pi}{4} \tag{2.11}$$

V_{DS} and I_{DS} refer to the DC drain voltage and maximum current. Similarly, when $\beta = 1$, $Z_{ds,m} = Z_{ds,c} = R_{opt}$, and $I_c = I_m$:

$$P_{L,f0}|_{\beta=1} = R_{ds,m}\frac{(I_{DS})^2}{4} + R_{ds,c}\frac{(I_{DS})^2}{4} = \frac{V_{DS}I_{DS}}{2} \tag{2.12}$$

$$P_{L,DC}|_{\beta=1} = \frac{2V_{DS}I_{DS}}{\pi} \tag{2.13}$$

$$\eta|_{\beta=1} = \frac{\pi}{4} \tag{2.14}$$

In theory, the drain efficiency reaches 78.5% both at back-off and maximum power. We can also see in these equations the back-off dynamic range γ :

$$\gamma = \frac{P_{L,f0}|_{\beta=1}}{P_{L_f0}|_{\beta=\beta_0}} = 4 \tag{2.15}$$

Figure 2.7 (a) and (b) shows the theoretical current and voltage profiles of the conventional DPA. We notice that while the current I_m scales linearly with β, the drain voltage V_m reaches its maximum value at the breakpoint $\beta = \beta_0$, and stays there. The efficiency of the main amplifier is thus maximum in the whole Doherty region. Figure 2.8 (a) – (e) shows the corresponding output power, drain efficiency, gain and impedances. As predicted, this form of Doherty Power Amplifier results in high efficiency at both 6 dB back-off and at maximum power. The efficiency in between these two points is reduced, because the auxiliary amplifier is not saturated. A very interesting feature of the DPA is its -theoretical- linearity. Referring back to the DLM situation, we explained that load modulation results in gain compression. We can see this effect in figure 2.8(c), where the gain of the main amplifier (red curve) decreases by 3 dB during the load modulation. In the Doherty architecture however, the auxiliary amplifier brings extra power to the system, resulting in an overall flat gain.

We note that for these simulations, the main transistor's DC and fundamental current was modeled following (1.22), while the class C was approximated to a simplified piece-wise linear current according to :

$$I_{DS,c} = I_{ds,c} = \begin{cases} 0 & \beta < \beta_0 \\ I_c\frac{\beta-\beta_0}{1-\beta_0} & \beta > \beta_0 \end{cases} \tag{2.16}$$

Modern 5GNR signals present an effective PAPR that can reach up to 12 dB in worst case scenarios. The conventional DPA has to be adapted to these complex signals. Raab [35] expanded the theory of a Doherty Power Amplifier to an arbitrary back-off range, which was first demonstrated in [36]. This architecture is called Asymmetrical DPA, as the auxiliary transistor is required to be larger than the main, in order to increase the load modulation. The breakpoint β_0 can be related to the output back-off range γ as :

$$\beta_0 = \frac{1}{\sqrt{\gamma}} \tag{2.17}$$

And the current I_c at maximum drive is now :

$$|I_c| = |I_m|\left(\frac{1}{\beta_0} - 1\right) \tag{2.18}$$

The output load impedance has to be set to

$$R_L = R_{opt}\beta_0 \tag{2.19}$$

We can calculate the impedance seen by both transistors as well as the delivered power and efficiency:

$$Z_{ds,m} = R_{opt}(\frac{1}{\beta_0} - \frac{I_c}{I_m}) \tag{2.20}$$

$$Z_{ds,c} = R_{opt}(\frac{I_m}{I_c}) \tag{2.21}$$

$$P_{L,f0}|_{\beta=\beta_0} = \frac{V_{DS}\beta_0 I_{DS}}{4} \tag{2.22}$$

$$P_{L,DC}|_{\beta=\beta_0} = \frac{V_{DS}\beta_0 I_{DS}}{\pi} \tag{2.23}$$

$$P_{L,f0}|_{\beta=1} = \frac{V_{DS}I_{DS}}{4}\frac{1}{\beta_0} \tag{2.24}$$

$$P_{L,DC}|_{\beta=1} = \frac{V_{DS}I_{DS}}{\pi}\frac{1}{\beta_0} \tag{2.25}$$

$$\eta|_{\beta=\beta_0} = \eta|_{\beta=1} = \frac{\pi}{4} \tag{2.26}$$

Figure 2.7 (c) and (d) show the resulting voltage and current waveforms and 2.9 presents the output power, efficiency gain and impedance associated with an X dB back-off DPA.

An other interesting variation of the classic DPA is the three-way Doherty, which is made of a main amplifier and two auxiliary amplifiers. By biasing each device at a different gate voltage, the first auxiliary amplifier can turn on at 9 dB back-off and the second at 6 dB back-off, resulting in three efficiency peaks. This architecture is particularly interesting for very large back-off ranges, but requires higher complexity and larger form factor.

In theory, the Doherty Power Amplifier can bring considerable efficiency improvements for high PAPR signals while keeping a linear operation. In practice, two major drawbacks are associated with this architecture :

- **Limited bandwidth** : The Doherty combiner is basically a quarter-wave length transmission line. While very simple and efficient, this component is particularly narrowband. The DPA is usually restricted to less than 10% fractional bandwidth [37]. This is in contradiction with 5GNR ultra wideband signals, even in the sub-6GHz bandwidths

- **Linearity degradation** : In most Doherty PAs, the auxiliary amplifier is biased in class C, effectively turning on at the right moment. Recalling figure 1.17, we can see that the class C amplifier presents a severe gain reduction and low power usage factor. In practice, the low gain of the class C is not enough to compensate the gain compression of the main transistor, resulting in amplitude distortion (AMAM distortion) [38, 39]. Similarly, the phase delay introduced by a transistor is dependent on the output impedance. Load Modulated amplifiers such as the DPA present strong phase distortion (AMPM distortion) due to the load variation [7]. Actual DPAs employed in base-stations are systematically implemented along with digital predistortion in order to mitigate this issue and fully exploit the high efficiency. This is a limiting factor as many case scenarios cannot apply DPD, such as mobile terminals, nano-base stations or massive MIMO systems.

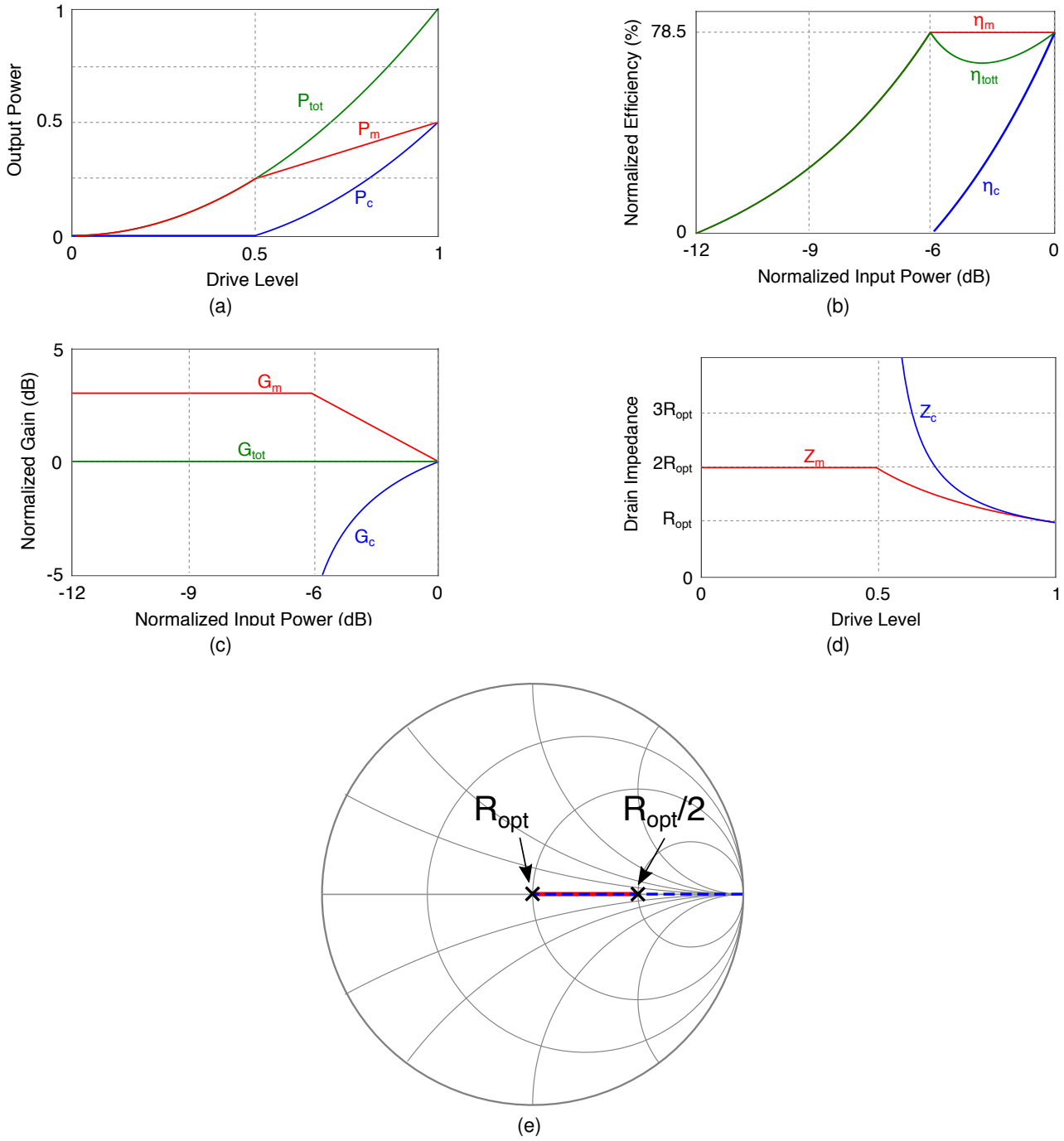


Figure 2.8: (a) Output Power, (b) Efficiency, (c) Normalized Gain, (d) Drain Impedance, (e) Load Trajectory of main (in red) and auxiliary (in blue) transistors and at the output (in green) of a 6 dB back-off Doherty Power Amplifier

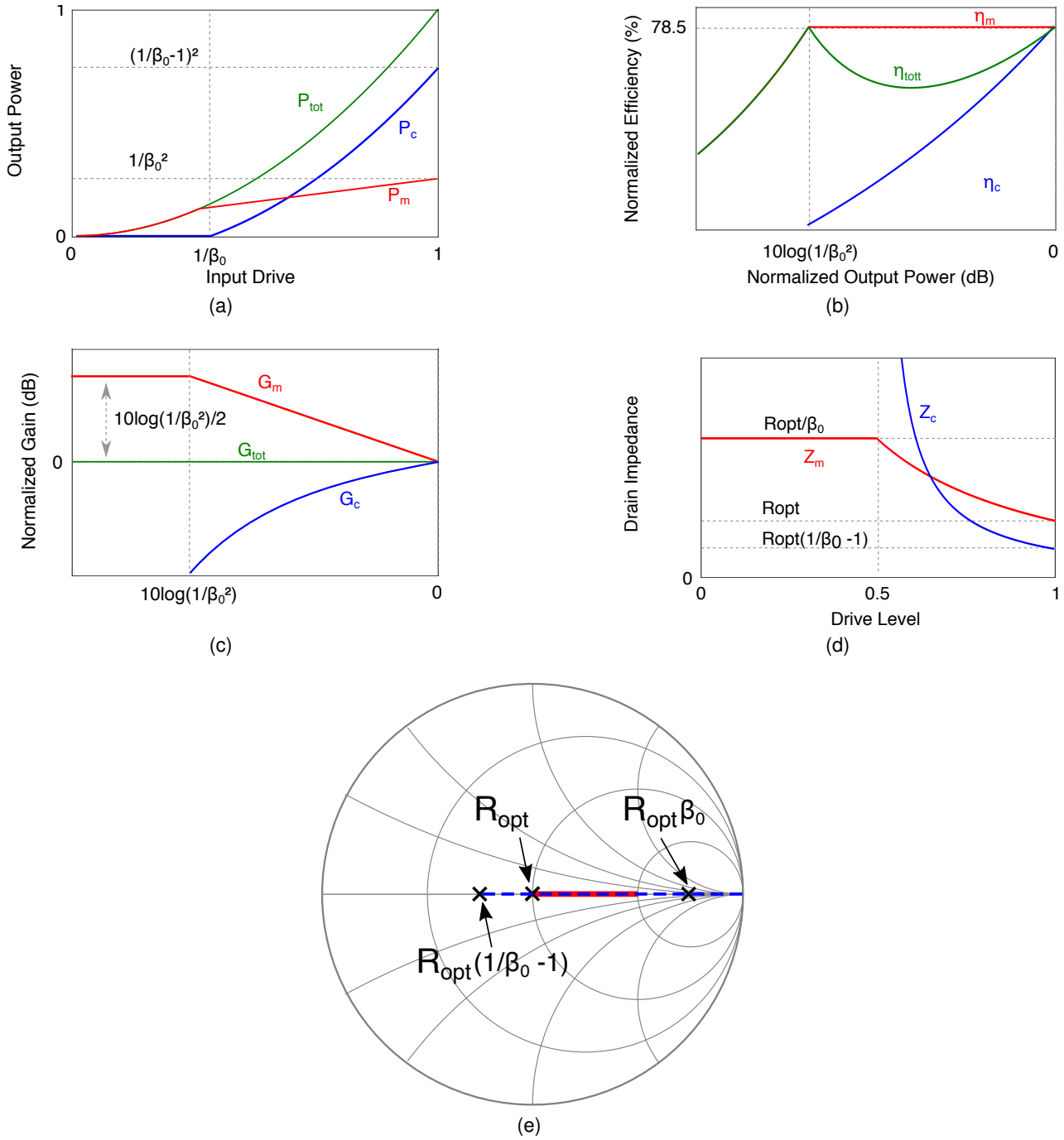


Figure 2.9: (a) Output Power, (b) Efficiency, (c) Normalized Gain, (d) Drain Impedance, (e) Load Trajectory of main (in red) and auxiliary (in blue) transistors and at the output (in green) of an X dB back-off Doherty Power Amplifier

Extensive research is done around the conventional DPA in order to resolve the aforementioned issues. Integrating the DPA in a signle chip such as in MMIC or RFIC tehcnologies is also a very big challenge for future designs **??**.

Outphasing Power Amplifier

In 1935, one year before W. H. Doherty presented his paper, Henri Chireix invented the Outphasing Power Amplifier (OPA, or Chireix) [40]. The Doherty load modulation mechanism is based on asymmetric amplitude operation between the two devices. The OPA is also based on two or more transistors connected through a non-isolating combiner, but assumes identical drain currents with variable phases. The fundamental concept of outphasing consists on translating the original amplitude and phase modulated signal into multiple phase modulated constant-envelope waveforms that are fed to separate transistors. The non-isolating combiner is designed such that the interaction of the different transistors results in a reconstruction of the original signal at the output. In the conventional Outphasing power amplifier, the transistors are modeled as ideal voltage sources. The impedance seen at their drain is modulated, following the principle presented at the beginning of this section. The output power is thus controlled by the relative phase shift (ψ) between the different paths. When ψ is zero, the PA branches' output signal add constructively, resulting in maximum power. For other angles, the power is outphased, until total cancellation occurs and zero output power is obtained at $\psi = 90°$. In practice, it is difficult to obtain very low powers only with outphasing, and input drive variation is operated to reach a large enough dynamic range. The original case is referred to as pure-mode outphasing while the latter is called mixed-mode outphasing. Having a constant envelope signal, the transistors constituing an outphasing amplifier are usually designed in class E or F, resulting in very high efficiency for -theoretically- all power levels. It is important to understand that in OPA, the output impedance and thus power of each transistor is dependent on the outphasing angle. As such, there is no dissipated power at lower drive levels.

In 1974 Cox proposed a similar architecture where the output combiner was replaced by an isolating Wilkinson combiner, resulting in the Linear Amplification with Non-Linear Components (LINC) [13]. The outphasing principle is still maintained in LINC, but there is no longer load modulation. As such the gain and phase response of all the transistors is constant, and the overall linearity depends only on the precision of the outphasing angle and the mismatch between each transistor. On the downside, the outphased power is radiated out of the system by the isolation resistor of the combiner, resulting in non-efficient operation at high outphasing angles. It is not therefore a high efficiency architecture.

The outphasing operation can be described as following : considering an input amplitude and phase modulated signal :

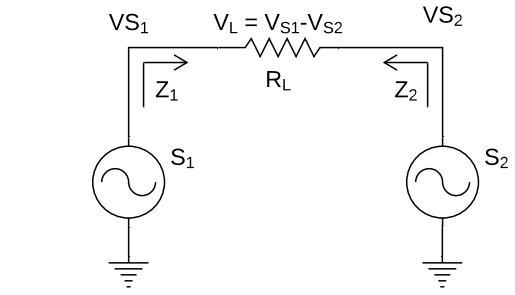
$$S_{in}(t) = A(t)\cos(\omega t + \phi(t)) \tag{2.27}$$

This signal can be separated into two constant amplitude phase modulated signals :

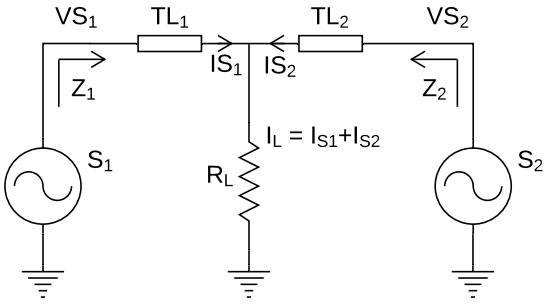
$$S_1(t) = \frac{\max(A(t))}{2}\cos(\omega t + \phi(t) + \psi(t)) \tag{2.28}$$

$$S_2(t) = \frac{\max(A(t))}{2}\cos(\omega t + \phi(t) - \psi(t)) \tag{2.29}$$

$$\psi(t) = \begin{cases} \cos^{-1}(\frac{A(t)}{\max(A(t)}) & \text{for series combining} \\ \sin^{-1}(\frac{A(t)}{\max(A(t)}) & \text{for differential combining} \end{cases} \tag{2.30}$$



(a)



(b)

Figure 2.10: Different outphasing combining : (a) Differential combining and (b) Series combining

The outphasing angle ψ will depend on the output combiner's architecture. We can distinguish series (or common-mode) combining, or differential combining. Figure 2.10 presents the two combining mechanisms. The output signal is the sum or difference of the two branch PAs outputs :

$$S_{out}(t) = \begin{cases} S_1(t) + S_2(t) & \text{for series combining} \\ S_1(t) - S_2(t) & \text{for differential combining} \end{cases} \tag{2.31}$$

In outphasing operation, the input is overdriven in order to reach rail to rail operation. Under such conditions the transistor can be modeled as a constant voltage source of magnitude V_0. The output voltage V_L can be measured for a differential combining:

$$V_{S1} = V_1 e^{j\psi_1} \tag{2.32}$$

$$V_{S2} = V_2 e^{j\psi_2} \tag{2.33}$$

$$I_L = \frac{V_L}{R_L} = \frac{V_1 e^{j\psi_1} - V_2 e^{j\psi_2}}{R_L} \tag{2.34}$$

In ideal conditions, we have $V_1 = V_2 = V_0$ and $\psi_1 = -\psi_2 = \psi$, resulting in

$$I_L = \frac{V_0}{R_L}(e^{\psi} - e^{-\psi}) = I_1 = I_2 \tag{2.35}$$

We can now calculate the admittance seen at the drain of each transistor :

$$Y_1 = \frac{I_1}{V_{S1}} = \frac{2\sin^2\psi}{R_L} + j\frac{\sin 2\psi}{R_L} \tag{2.36}$$

$$Y_2 = \frac{I_2}{V_{S2}} = \frac{2\sin^2\psi}{R_L} - j\frac{\sin 2\psi}{R_L} \tag{2.37}$$

Under series combining, we can use the quarter-wave length lines with characteristic impedance R_L to follow a similar procedure, as they transform the constant voltage $V_{S1,2}$ into a constant current $I_{S1,2}$ at the other end. We can find the output current and branch admittances :

$$Y_1 = \frac{I_1}{V_{S1}} = \frac{2\cos^2\psi}{R_L} + j\frac{\sin 2\psi}{R_L} \tag{2.38}$$

$$Y_2 = \frac{I_2}{V_{S2}} = \frac{2\cos^2\psi}{R_L} - j\frac{\sin 2\psi}{R_L} \tag{2.39}$$

$$I_L = -j\frac{V_0}{R_L}(e^{\psi} + e^{-\psi}) \tag{2.40}$$

The output power can be measured at the load as a function of the outphasing angle :

$$P_{L_{f0}}(\psi) = \begin{cases} \frac{2V_0^2\cos^2(\psi)}{R_L} & \text{for series combining} \\ \\ \frac{2V_0^2 sin^2(\psi)}{R_L} & \text{for differential combining} \end{cases} \tag{2.41}$$

The only difference between the two combining methods is the required outphasing angle, that must go from 0 to $\pi/2$ in differential combining and $\pi/2$ to 0 for series combining. Figure 2.11 presents the impedance trajectories and the equivalent parallel resistance and susceptance. Figure 2.12 shows the output power versus the outphasing angle for the two combining methods. We notice that in contrast with the Doherty PA, the outphasing load trajectory is following constant impedance circle, and thus presents a very strong reactive component. This in turn results in a phase shift between the voltage and current time-domain waveforms, and thus an important efficiency drop. In a Chireix combiner, this is addressed by adding two compensating susceptive elements of opposed value in parallel to each transistor, in order to shift the load modulation. The load trajectories are pushed together, and the reactance is zeroed for two selected outphasing angles. Figure 2.14 presents a differential combined Chireix outphasing amplifier, with the two shunt elements. The admittances seen at each branch are now

$$Y_1 = \frac{I_1}{V_{S1}} = \frac{2\cos^2(\psi)}{R_L} + j\frac{\sin(2\psi) - \sin(\psi_{comp})}{R_L} \tag{2.42}$$

$$Y_2 = \frac{I_2}{V_{S2}} = \frac{2\cos^2(\psi}{R_L} - j\frac{\sin(2\psi) - \sin(\psi_{comp})}{R_L} \tag{2.43}$$

Where $\psi_{comb} = \sin^{-1}(B_{comp}R_L)$, B_{comp} being the compensating susceptance. Efficiency will be maximized at each zero reactance point. The ratio of output power at these two outphasing angles, equivalent to the back-off dynamic range, can be found to be :

$$\Delta P_{L_{f0}} = \frac{\cos^2(\psi_{comp})}{\cos^2(\pi/2 - \psi_{comp})} \tag{2.44}$$

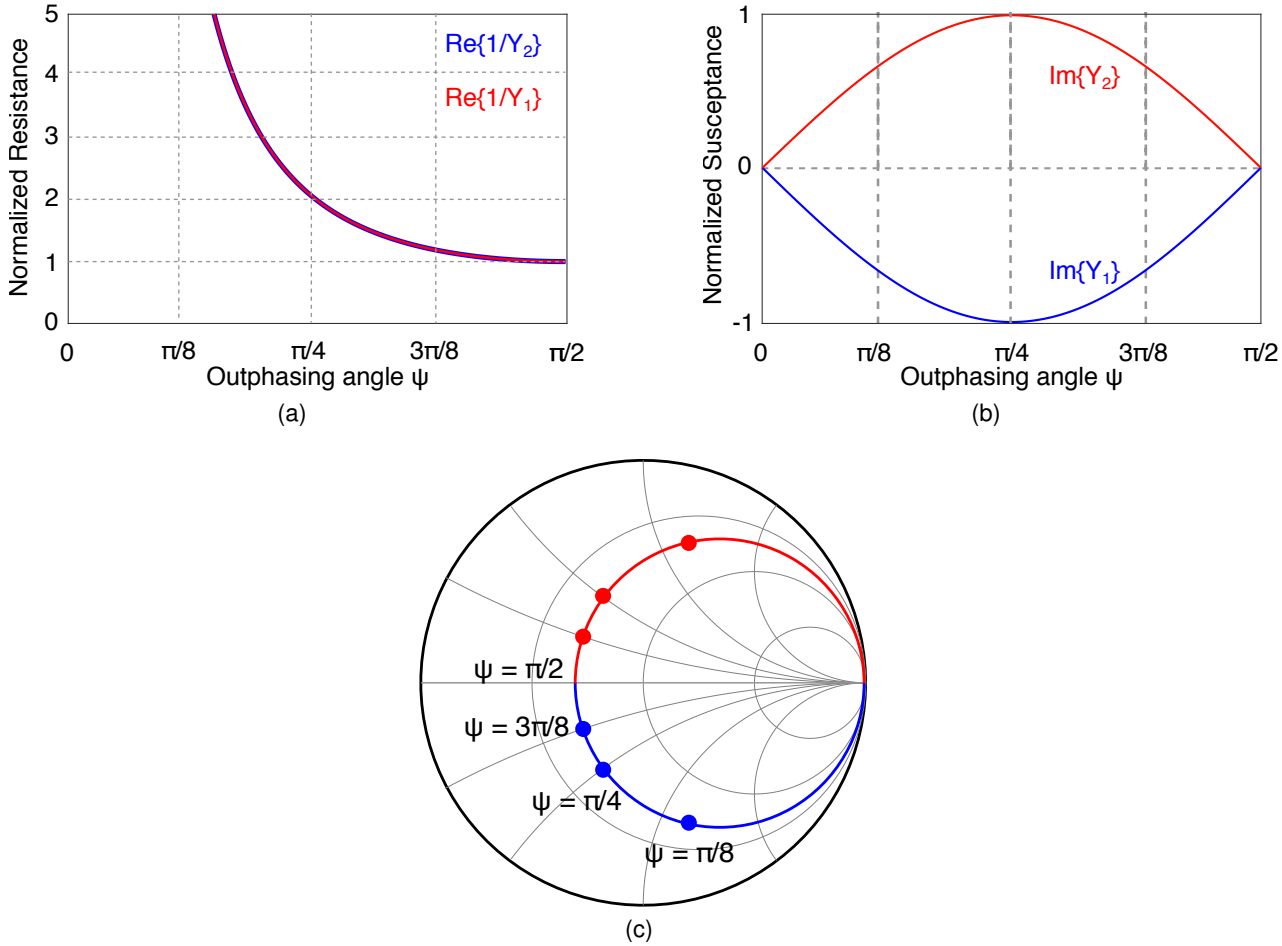


Figure 2.11: Load Trajectory of the simple Outphasing combiner. (a) The equivalent parallel resistance R_p, (b) the parallel susceptance X_p and (c) the load trajectory on the Smith chart.

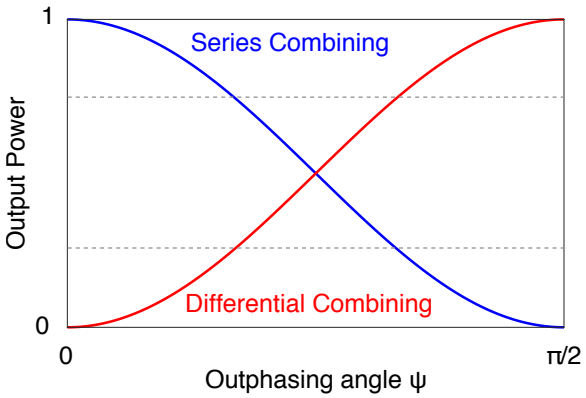


Figure 2.12: Output power versus outphasing angle

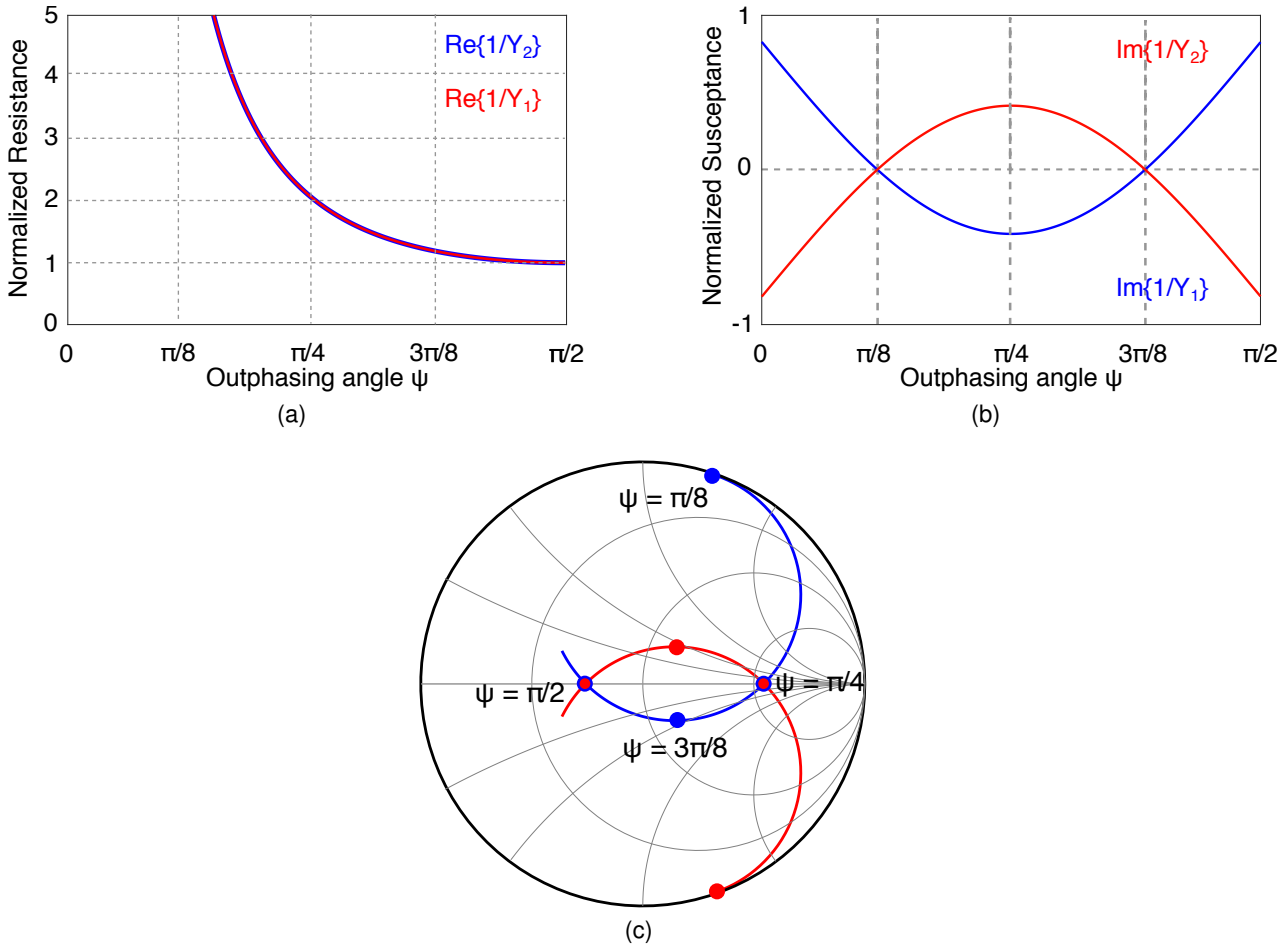


Figure 2.13: Load Trajectory of the Chireix Outphasing combiner. (a) The equivalent parallel resistance R_p, (b) the parallel susceptance X_p and (c) the load trajectory on the Smith chart.

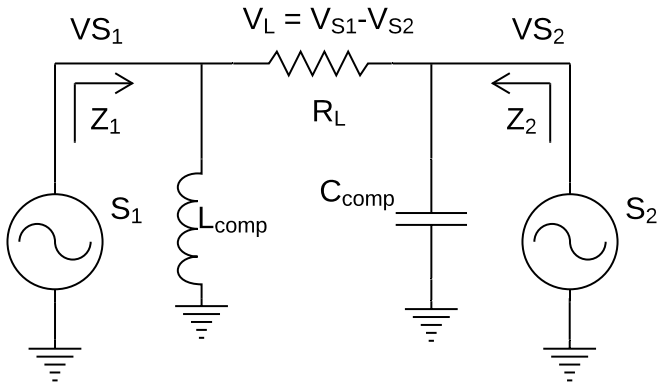


Figure 2.14: Chireix Combiner

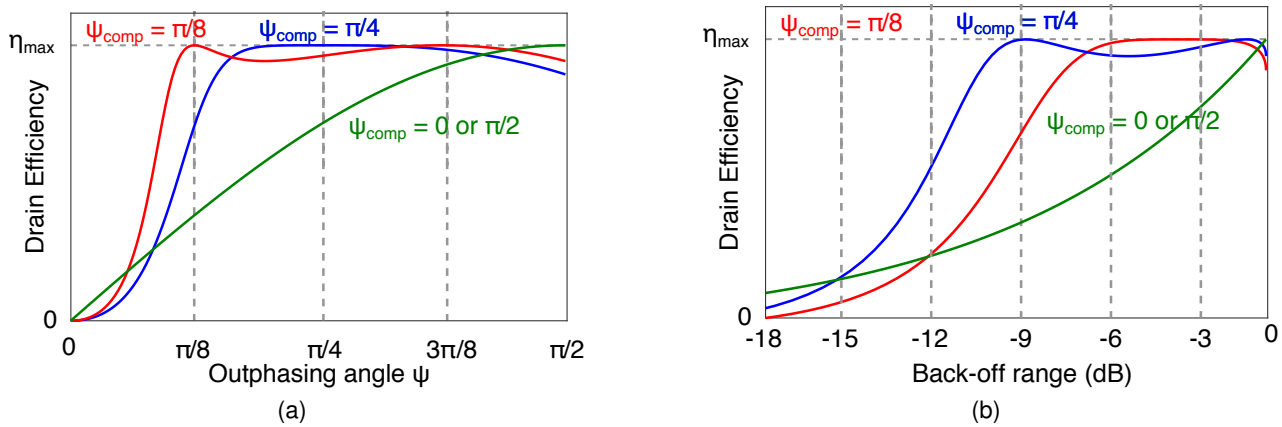


Figure 2.15: OPA theoretical drain efficiency for different compensating reactances, in (a) versus the outphasing angle and in (b) versus the resulting output power

In figure 2.13 the Chireix load trajectories and the real and imaginary parts of the corresponding admittances are presented. Theoretical calculation of the efficiency of an outphasing amplifier is complicated, but we can approximate it to the following equation :

(2.45) $$\eta_{OPA} = \eta_{PA}.\eta_{PF}$$

(2.46) $$\eta_{PF} = \frac{Re\{Y_1\} + Re\{Y_2\}}{|Y_1| + |Y_2|} = \frac{2\cos^2(\psi)}{\sqrt{4\cos^4(\psi) + (2\sin(2\psi) - 2\sin(2\psi_{comp}))^2}}$$

Where η_{PA} is the branch amplifier theoretical maximum efficiency and η_{PF} the power factor efficiency, defined as the ratio of real power to the overall output power. Figure 2.15 presents the estimated overall efficiency versus the outphasing angle (in (a)) and the real output power (in (b)).

Outphasing Power Amplifier is a very promising technique, as it can -relatively- easily achieve high efficiency at very large output power back-offs [41]. It has however some major drawbacks that still make its implementation in actual systems very challenging. Similar to the Doherty Power Amplifier, the Chireix combiner is an inherently narrowband structure, in that the compensating reactances shift the load trajectories with frequency. OPA also presents very strong non-linearities, as the drain impedance shows very strong reactive variations. Nevertheless, it is getting a lot of attention for future 5G NR transmitters.

2.3 Evolution of Load Modulated Architectures

The theory presented in the previous subsections allows great insight to the load modulation mechanism, but in practice is not applied as such, as the idealized models used to derive it are not realistic. Actual power amplifier design is driven from load-pull measurements or simulations, and these should be taken into account in high efficiency architectures.

Generalized Load Modulated Amplifier

Hallberg presented in [3] a generalization of the Doherty Power Amplifier. The generalized operation considers arbitrary main/auxiliary transistor size ratio and current phase difference. The output

combiner along with the matching networks are considered as a lossy two-port black box, defined by some boundary conditions, extracted from load-pull data. Looking at figure 2.16, the boundary conditions equate the black-box parameters to the required transistor drain impedances at $\beta = \beta_0$ and $\beta = 1$:

$$Z_{11} + Z_{12}\alpha_M = Z_m|_{\beta=1} \tag{2.47}$$

$$Z_{22} + Z_{12}/\alpha_M = Z_c|_{\beta=1} \tag{2.48}$$

$$Z_{11} + Z_{12}\alpha_{\beta_0} = Z_m|_{\beta=\beta_0} \tag{2.49}$$

$$Z_{22} + Z_{12}/\alpha_{\beta_0} = Z_c|_{\beta=\beta_0} \tag{2.50}$$

$$\alpha_M = \frac{I_c|_{\beta=1}}{I_m|_{\beta=1}} = \sqrt{\frac{Re\{Z_m|_{\beta=1}\}P_c|_{\beta=1}}{Re\{Z_c|_{\beta=1}\}P_m|_{\beta=1}}}e^{-j\theta} \tag{2.51}$$

$$\alpha_{\beta_0} = \frac{-Z_{12}}{Z_c|_{\beta=\beta_0} + Z_{22}} \tag{2.52}$$

Where the m and c subscripts refer the main and auxiliary transistor and the Z and P letters refer to the impedances found from load-pull and the corresponding output power. We note also that $Z_c|_{\beta=\beta_0}$ corresponds to the drain impedance of the auxiliary amplifier when it is turned-off. To achieve a generalized DPA, the required power from the auxiliary device is decoupled from the back-off dynamic range :

$$P_c|_{\beta=1} = xP_m|_{\beta=1} \tag{2.53}$$

$$\beta_0 = \frac{P_m|_{\beta=1}}{P_m|_{\beta=\beta_0}} \tag{2.54}$$

$$\gamma = \beta_0(1+x) \tag{2.55}$$

In order to solve the system, we need to go from a lossy two-port to a lossless three port network, where the output load is connected on the third port. This transformation can be done if and only if the following condition is valid :

$$Re\{Z_{12}\}^2 = Re\{Z_{11}\}Re\{Z_{22}\} \tag{2.56}$$

For a given back-off dynamic range and maximum output power, the devices can be selected. The impedances at back-off and maximum power for the main and auxiliary transistor can be found from load-pull, and the combiner can then be calculated from the previous equations and translated into an actual network.

The Generalized DPA formulation presents many advantages compared to the conventional architecture :

- There is no longer need for quarter-wave length transmission lines : the combiner + matching network can be a generic network design that fulfils the boundary conditions. This can potentially result in wider bandwidth.
- The relative maximum power of the main and auxiliary transistors is an extra degree of freedom. As such, new solutions can be found that present higher linearity.

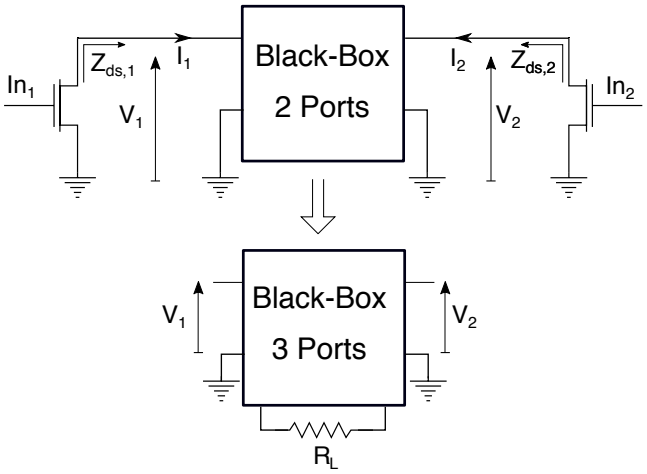


Figure 2.16: Generalized Active Load Modulation Power Amplifier

Following this concept, a Doherty amplifier was presented in [42] where this new degree of freedom was used in order to achieve a flat AMPM characteristic. The resulting amplifier achieved 41% efficiency with -40 dBc ACLR with a 10MHz 7.2 dB PAPR signal before DPD. This design is considered as a very important step towards linear high efficiency amplifiers.

A Generalized Outphasing Power Amplifier was described in [43]. A similar procedure to the generalized DPA was followed, the main difference being that the equivalent of the auxiliary transistor is not turned off at back-off, and the drain impedances are equal, i.e. $Z_m = Z_c$. Identical conclusions can be drawn in terms of linearity and bandwidth as with the DPA. In the afformention article, the authors present after linearization -41 dBc ACLR from 700 Mhz to 1 GHz, with 56% drain efficiency with a 6.7 dB PAPR single-carrier W-CDMA signal.

Dual-input Power Amplifiers

The concept of Active Load Modulation amplifiers can be expanded and described as load modulation through a non-isolating combiner with asymmetrical operation in phase and amplitude, as seen in figure 2.5. The Doherty or Outphasing power amplifiers are subcategories of this bigger family of architectures. The evolution of digital technologies and component integration has led in the recent years to the transition from plug-and-play power amplifiers to more complex transmitters. Dual-input systems are a very attractive alternative to the original single-RF input architectures, as they broaden the load modulation design space. In dual-input, the distinction between Doherty (amplitude) and Chireix (phase) load modulation is actually not that accurate, since both can be applied simultaneously.

Recently a lot of attention has been brought towards the Doherty-Outphasing continuum, based on this concept. In [44], a Doherty-Outphasing Power Amplifier (DOPA) at 2 GHz, reaching 60% drain efficiency and -47 dBc ACLR with a linearized 20MHz - 9dB PAPR LTE signal. In this paper, in the low power region the auxiliary amplifier is turned off, like in regular doherty. In the high power region, both the amplitude and phase of the auxiliary amplifier is tuned, in order to maximize performance throughout the whole dynamic range. In [45], an alternative approach is explored where three different regions are defined : a low power region, a Doherty region and an Outphasing region. The resulting amplifier presents 66% drain efficiency at 12 dB back-off, with -46 dBc ACLR with a 10MHz signal after digital predistortion.

This concept can be further expanded to also include envelope tracking. In [46], a linear dual-input Doherty power amplifier was designed, whose back-off efficiency was further enhanced with discrete level supply modulation. The resulting amplifier presented 38.7$\%$ PAE and -47 dBc ACLR

with a predistorted, 60MHz LTE-like signal with 10 dB PAPR. The same concept was applied in [47] to a dual-input Chireix Outphasing amplifier, reaching 23% PAE at 9.1 GHz with a 10MHZ, 12 dB PAPR signal. As often in outphasing amplifiers, only -31 dBc ACLR was achieved after digital predistortion.

These generalized architectures focus on a mixed-mode operation, relying on digital tools and multiple RF front ends. Their impressive performance make them very promising for very high power base stations, where the computing ressources are available.

2.4 Harmonically Tuned Load Modulated Amplifiers

The original Doherty or Outphasing power amplifiers are based on a purely real fundamental load trajectory, limited to the Class B amplifier. Generalized load modulated amplifiers expand the design space by finding the optimal fundamental and harmonic terminations through load-pull, resulting eventualy in complex fundamental and harmonic impedances. This section presents an analysis verified with simulation of harmonically tuned load modulated amplifiers.

Extended B/J continuum

In section 1.5, we saw that the optimum resistance design space could actually be expanded to include complex terminations, associated with reactive harmonic impedances. This concept can be extended to load modulation, and leads to :

$$R_L = 2\frac{V_{DS} - V_K}{\beta I_{DS}} = \frac{R_{L,opt}}{\beta} \tag{2.57}$$

$$Z_{f_0,B/J} = \frac{R_{L,opt}}{\beta} + j\delta\frac{R_{L,opt}}{\beta} = R_L(1 + j\delta) \tag{2.58}$$

$$Z_{H_2,B/J} = -j\frac{3\pi}{8}\delta\frac{R_{L,opt}}{\beta} = -j\frac{3\pi}{8}\delta R_L \tag{2.59}$$

Where $R_{L,opt}$ is the optimum class B impedance. V_{DS} and I_{DS} correspond to the DC drain voltage and current and V_K to the knee voltage. The corresponding current/voltage waveforms and load trajectories can be seen on figure 2.17.

$\delta = 0$ leads to the class B case, where the fundamental impedance is purely real and the second harmonic is shorted. With this formulation, we notice that for $\delta \neq 0$, a harmonic load modulation is required to maintain the appropriate voltage and current waveforms when the fundamental impedance is varied. This would suggest an asymmetry in the class B/J continuum, the B case being advantageous. However in [4, 48], another approach was suggested, in which the second harmonic termination is fixed, for example to the required second harmonic at peak power :

$$Z_{H_2,B/J} = Z_{H_2,B/J}|_{\beta=1} = -j\frac{3\pi}{8}\delta R_{L,opt} \tag{2.60}$$

In turn, a constant second harmonic requires a fixed reactive component, equal to that required at peak power in our example :

$$Z_{f_0,B/J} = \frac{R_{L,opt}}{\beta} + j\delta R_{L,opt} = R_L(1 + j\delta\beta) \tag{2.61}$$

This new formulation implies that in load modulated amplifiers, high efficiency can be maintained by moving inside the B/J continuum. In a very high back-off design, optimal load modulation for a

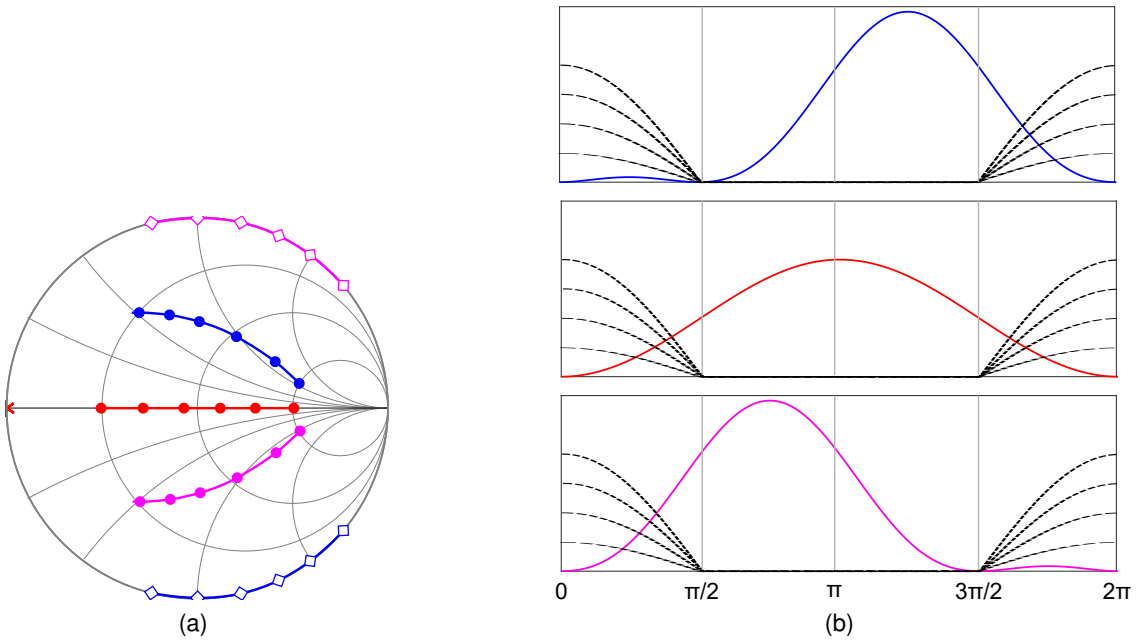


Figure 2.17: Continuous Modes theory applied to load modulation. On the right, in dotted black lines the current waveform for different drive levels. In blue, red and magenta the voltage waveform for the classes J, B and J* second harmonic terminations, for different drive levels. On the Smith chart on the right we can see the corresponding fundamental (in dots) and second harmonic (in diamonds) terminations throughout the load modulation.

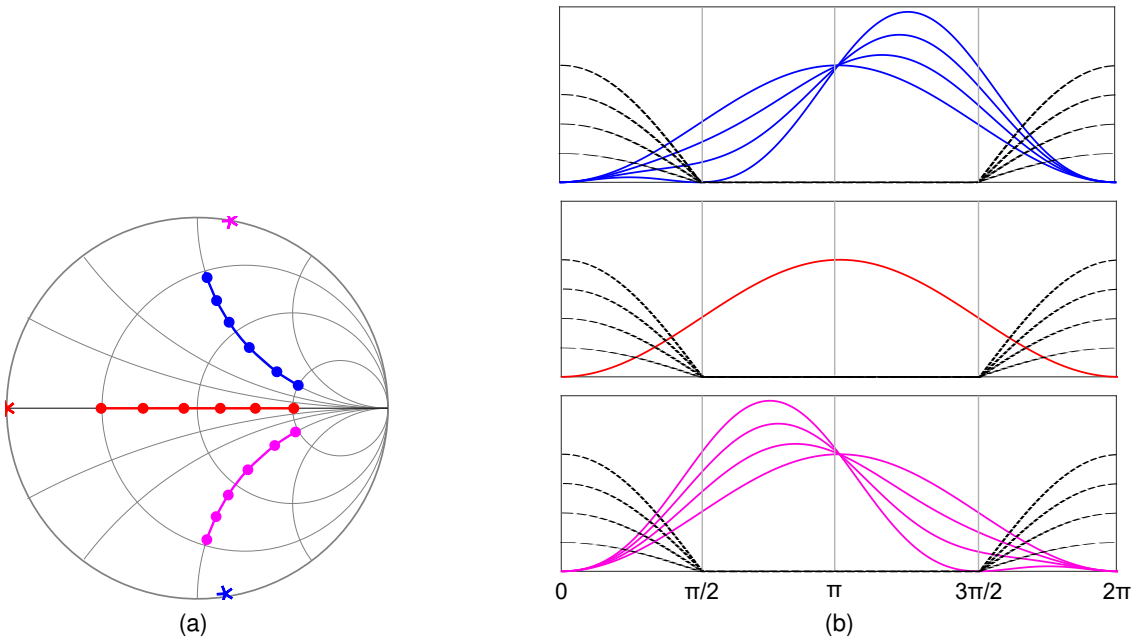


Figure 2.18: Fixed Second harmonic continuous modes load modulation. On the right, in dotted black lines the current waveform for different drive levels. In blue, red and magenta the voltage waveform for the classes J, B and J* second harmonic terminations, for different drive levels. On the Smith chart on the right we can see the corresponding fundamental (in dots) and second harmonic (in diamonds) terminations throughout the load modulation.

$\delta = 1$ second harmonic termination goes from a class B (purely real fundamental impedance) to a class J. Figures 2.17 and 2.18 present the load trajectories and resulting voltage and current waveforms for the two load modulation scenarios, with varying (2.17) and fixed (2.18) second harmonic.

Practical Harmonic Load Modulation

The analysis presented here assumed zero knee voltage and an ideal half-wave rectified current. A real RF transistor is not a perfect current source and presents a transient region characterized by the knee voltage. In practice highest efficiency will be observed when the drain voltage is allowed to go deep inside the knee region, resulting in current clipping. The fundamental voltage swing is therefore maximized and the harmonic components generated by the current clipping can be used to further engineer the voltage waveform, thus reducing the voltage/current overlap. Current clipping however results in lower output power. We notice in load-pull measurements that the maximum efficiency and maximum power contours are usually shifted.

By allowing current clipping, the harmonic components in the waveform will change depending on the PA input drive, and thus the back-off level. In turn this has a significant effect on the load trajectory. Optimal load trajectories therefore have to be found from load-pull measurements or simulations.

In order to explore the effects on the load trajectory of the second harmonic termination, load pull simulations at 2.4 GHz were performed on the CGH40010F device from Cree. It is a 10W, GaN HEMT with 28V drain supply voltage. This device was chosen because its model gives access to the current and voltage at the intrinsic drain plane. We can thus directly compare the simulated data with the theoretical waveforms. Prior to the load-pull, a first Class B optimum impedance was calculated according to equation 1.36 for the class B mode. This impedance was de-embeded to the package plane using the data from the transistor model. The device was stabilized with a parallel RC network (8Ω 4.3pF) and a shunt resistor (40Ω). With the transistor loaded with the calculated optimum impedance, the input was conjugately matched to 50 Ω. The device was biased in deep class AB, at $V_{DS} = 28V, I_{DS,q} = 20mA$. The input power was swept from 15 to 32 dBm and the reflexion coefficient spanned from 0 to 0.8 around the optimum impedance, with 144 different impedance points. Five different second harmonic terminations were chosen, in order to study their effects on the load trajectory :

- **Class B termination** : the second harmonic at the packaged plane is selected to be short-circuited at the intrinsic drain plane, resulting in class B waveforms
- **Peak power Class J/J*** : Considering the theoretical peak power of the device (41 dBm), a class J and J* impedance is selected, according to 1.36
- **Back-off power Class J/J*** : Optimal class J/J* impedance for a 6 dB back-off on the device (i.e. 35 dBm)

The resulting harmonic impedances can be found in table 2.1. A load-pull simulation was performed for each second harmonic termination. The third harmonic was set at 50Ω, as at these frequencies it is practically shunted by the transistor's C_{DS}.

The built-in load-pull tool of Advanced Design System (ADS) was used. The results of the five load-pull simulations can be seen on figure 2.19. We are mainly interested here in the gain and power added efficiency versus output power for each case. 5 load trajectories have been selected, that maximize PAE throughout the load modulation. These trajectories can be seen on the Smith charts of figure 2.20 on the left at the package plane of the device, and on the right at the de-embeded, intrinsic drain plane.

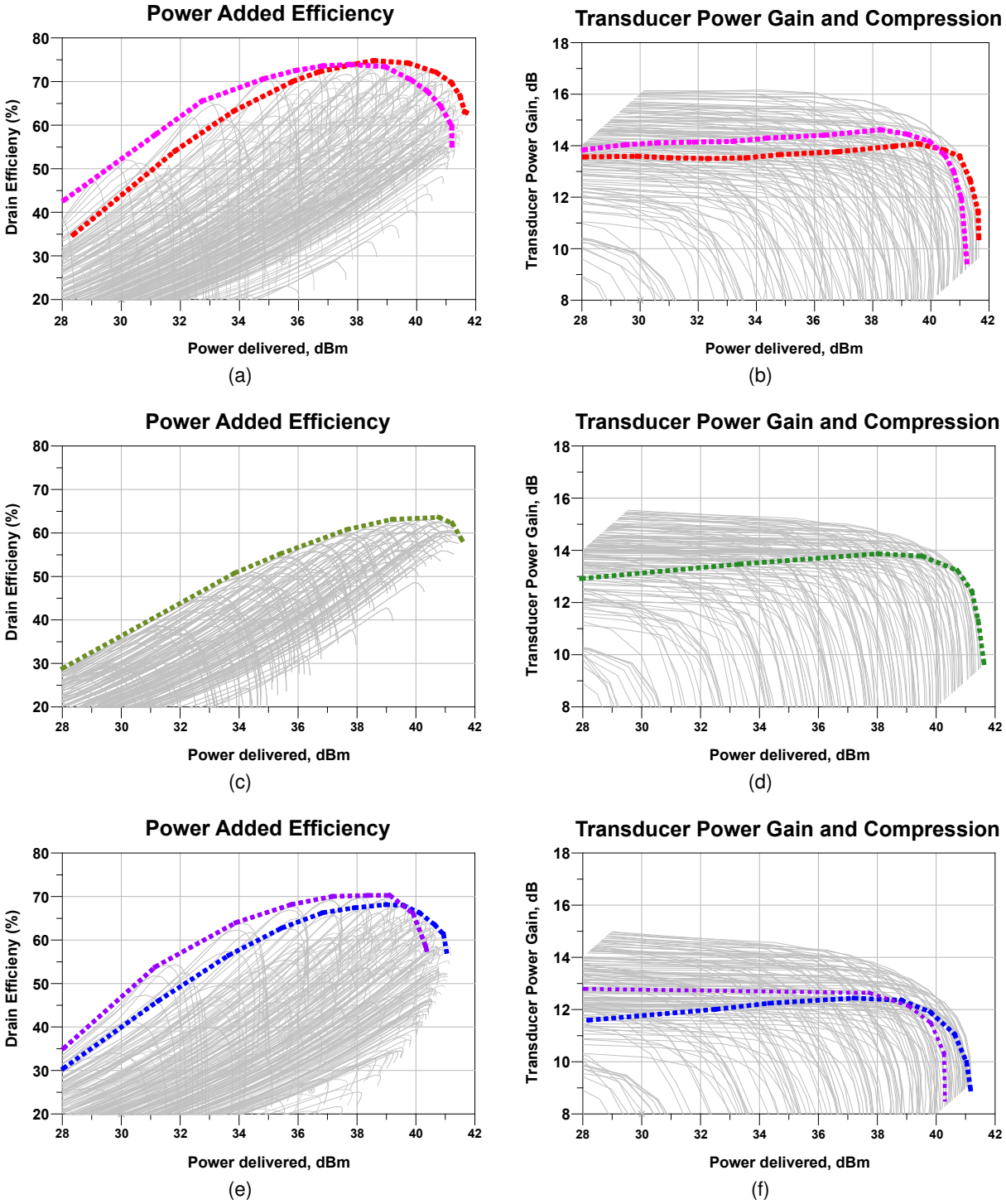
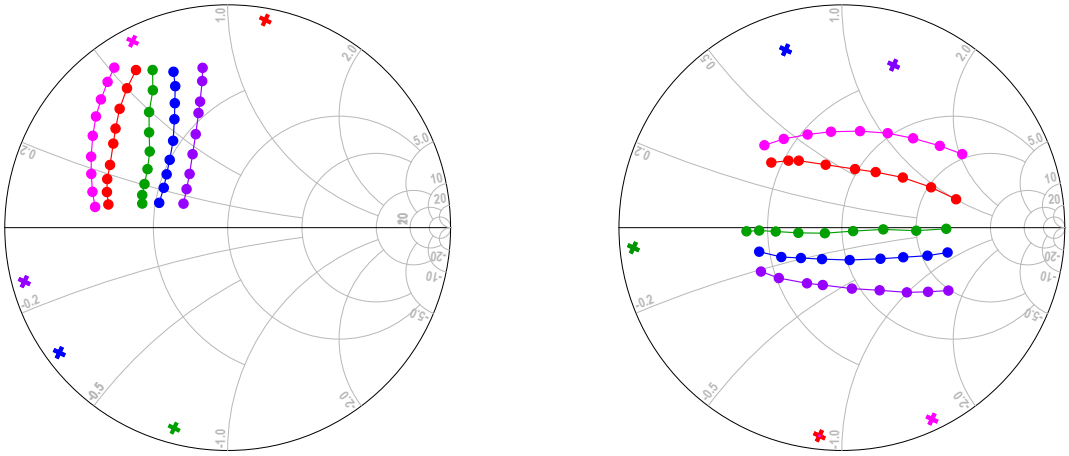


Figure 2.19: Load-pull results for the different harmonic terminations, with the PAE on the left and Gain on the right. From top to bottom, Class J, B and J* harmonic terminations. For the J and J* case, the back-off and peak power termination simulations are grouped. The dotted line show the performance of a load modulated amplifier with the corresponding second harmonic. The color code is identical as on the plotted trajectories on the Smith chart of figure 2.20



(a) (b)

Figure 2.20: In solid line with dot markers, load trajectories providing maximum drain efficiency for five different harmonic terminations, (a) at the transistor's package plane and (b) at the de-embeded intrinsic drain plane. The corresponding second harmonic terminations are marked with a cross, using the same color code.

Table 2.1: Second harmonic impedance presented for each load-pull setup.

	Class B	Class J		Class J*	
		Peak Power	Back-off Power	Peak Power	Back-off Power
Package plane	1-j37	1+j58	1+j30	1-j20	1-j7
Intrinsic plane	1.5-j2.5	2-j.47	2.2-j.80	6+j36	18+j60

As expected, the optimal load trajectories depend on the harmonic termination. In the class B case, the shorted second harmonic leads to a purely real load trajectory, while a reactive second harmonic requires a complex trajectory. The harmonic load trajectories are however rather far from what expected from the theory in figure 2.18. This deviation is most probably originated in the interaction with the knee region.

It can be noted that for the three peak power harmonic terminations (red, green and blue trajectories), similar maximum power is achieved, around 41 dBm. Efficiency at this maximum output power is also comparable, around 60%. In the class B case, the highest efficiency point is very close to the maximum power. This is not the case for the J/J* terminations, where maximum efficiency is achieved at 1.5-2 dB back-off. This can be explained in terms of harmonic components. In the J/J* configurations, the current clipping generates harmonic voltage components, shaping the waveform and achieving smaller voltage/current overlap. This effect does not take place in the class B, where all harmonics are shorted. In general, much higher efficiency is obtained at back-off when the second harmonic is reactively terminated.

As expected, the peak-power harmonic termination (red and blue) and the back-off harmonic terminations (pink and magenta) lead to slightly different output power levels. However, it seems that a more reactive impedance (pink and magenta) leads to an even grater back-off impedance. This is can be explained because the resulting second harmonic is getting closer to an open-circuit. Along with the appropriate voltage shaping, the current is going from a half-wave rectified to a squared waveform, limiting even further the overlap.

To summarize, classic load modulation assumes a purely real load trajectory. Expanding the B/J continuum, closed form solutions show that harmonically tuned load modulating trajectories can be found that achieve similar performance with a complex fundamental impedance. In practice, it is found that reactively terminated harmonic impedances result in higher back-off efficiency, as the interaction with the knee region shapes the voltage and current to a more efficient waveform.

2.5 Linearity Considerations of high efficiency architectures

While the Outphasing amplifier is known for its inherently non-linear operation, the ideal Doherty Power Amplifier is considered as a perfectly linear architecture [11]. In practice, severe amplitude (AM-AM) and phase (AM-PM) distortions are observed in the load modulated region [6].

As explained in the previous chapter, the gain of a transistor under load modulation is decreasing. This phenomenon is referred to as Load Modulation - Amplitude Modulation (LM-AM) distortion. In the theoretical Doherty PA, the compressing gain of the main transistor is compensated by the auxiliary amplifier. This is not the case in practice, as the class C biased auxiliary amplifier has lower gain than the class B. The auxiliary amplifier also presents a soft turn-on, further reducing the gain in the high efficiency region.

Similarly, the dependency of a transistor's phase response to the output impedance is not taken into account in the conventional DPA methodology. However, in [7], it was shown that the the gate-drain capacitance C_{GD} provided a feedback path between the input and output of the main power amplifier. In turn, the Miller effect produces a variation of the input gate impedance under load modulation. This non-linear impedance variation leads to very high load modulation to phase modulation distortion (LM-PM) at the drain of the transistor. In a Doherty PA, this LM-PM at the drain of the main device will result in very high AM-PM at the output of the DPA, reaching up to 30°.

We note here the following nomenclature : at the transistors drain, the amplitude or phase variations due to the change in impedance is referred to as LM-AM or LM-PM. In a load modulated amplifier such as the Doherty PA, the amplitude and phase variation at the output originates from the intrinsic LM-AM and LM-PM of the constituent transistors. However, the load modulation is implicit, and in practice these distortions occur when the amplitude of the input signal is varied. We therefore use the classic AM-AM and AM-PM nomenclature when referring to the overall architecture.

One technique to mitigate the AM-AM distortion of the DPA consists on finely tuning the bias voltages of the different devices, in order to cancel out inter-modulation products at the output [38, 49]. The ideal voltages for linearity unfortunately do not coincide with those giving maximum efficiency, resulting in a linearity-efficiency design trade-off.

In [50], AM-PM distortion of a DPA was limited by mismatching the input of the main transistor. The variation of the non-linear input impedance was thus minimized, resulting in an almost flat AM-PM. However, mismatching the input results in a smaller gain, already low in Doherty PAs.

Another approach that considers both the gain compression (AM-AM) and phase distortion (AM-PM) is based on the Generalized Doherty Power Amplifier [3], presented in the previous section. In this design, the relative transistor size and the phase difference between the main and auxiliary amplifier's current are kept as extra degrees of freedom. That way, new solutions can be found that minimize overall phase and gain distortions. In practice, the output combiner is designed in order to generate an additional, load dependent phase component, that cancels out the LM-PM of the transistors in the high efficiency region, leading to quasi flat overall AM-PM. The resulting load trajectory presents a reactive load modulation. In [42], an amplifier based on this concept reached an average PAE of 40% and -41 dBc ACLR with a 10MHz, 7.2 dB PAPR signal, without digital predistortion. This approach is very promising, as it allows for inherent linear phase operation with minimum gain or efficiency loss.

2.6 Conclusion

In this chapter, the principal Efficiency enhanced Power Amplifier architectures were presented. The concepts of Supply and Load modulation are explained and the main architectures associated with them further investigated. Compared to conventional single-ended transistors, supply and load modulation amplifiers provide a drastic increase of the back-off efficiency, making possible the use of more complex, high PAPR signals. These architectures are naturally associated with higher complexity, as more components are needed to obtain the correct high efficiency mechanisms. The two recurring issues associated with them is the relatively small instantaneous bandwidth and the inherent non-linearity.

So far, 4G base-stations have widely used conventional Doherty Power Amplifiers along with adaptive digital predistortion. However, the 5G NR standard extends the instantaneous bandwidth, reaching up to 100MHz in the sub-6GHz frequency range. As a rule of thumb, digital predistorters are required to run at at least five times the original signal bandwidth, resulting in a 500MHz sampling frequency. The DC consumption of the DPD hardware grows exponentially, making in some cases the PA's efficiency enhancement insignificant compared to the added complexity. In nano and pico base-stations, the power cost of the required DPD can outmatch the power actually consumed by the power amplifier. Similarly, in Massive MIMO or in user equipments, DPD cannot be implemented as the space and computing ressources are limited.

It is therefore important to overcome the linearity and bandwidth issues associated with these high efficiency architecture in order to alleviate or completely eliminate the digital predistortion. The next chapter presents a novel load modulated architecture that attempts to answer these new challenges.

Chapter 3

The Load Modulated Balanced Amplifier

The Load Modulated Balanced Amplifier (LMBA) is a recent architecture, first presented in [51] by Pr. Cripps. As its name suggests, it is based on the Balanced Amplifier (BA).

3.1 Load Modulated Balanced Amplifier

The Balanced Amplifier is a very famous power amplifier architecture, used extensively since the 1960. The concept of a BA is presented in figure 3.1. It consists of two identical power amplifiers connected together at their input and output by a hybrid coupler. As with any symmetrical power combining architecture, the BA allows for 3 dB more output power compared to a single-ended amplifier without changing the overall gain. An important feature of balanced amplifiers is their very high S_{11} and S_{22}, guaranteed by the isolation resistors.

In a Load Modulated Balanced Amplifier (figure 3.2), the output isolation resistor is replaced by a Control Amplifier (CA), which injects a modulating current inside the isolated port of the hybrid coupler. This current will be used to create an active load modulation of the impedance seen by the two branch transistors of the balanced amplifier. A qualitative explanation of the load modulation mechanism can be given based on the reflexion coefficient Γ seen by each amplifier. We can define

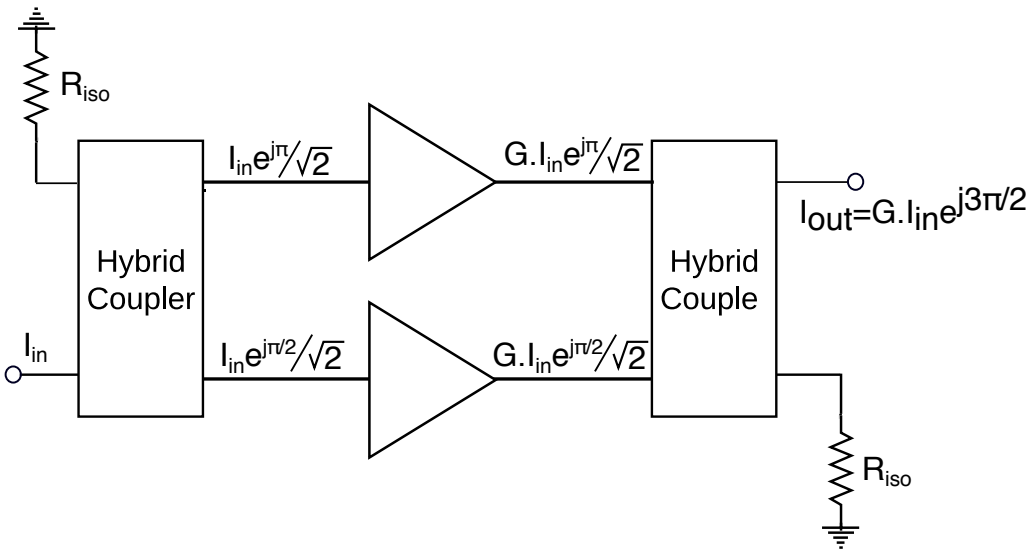


Figure 3.1: Balanced Amplifier

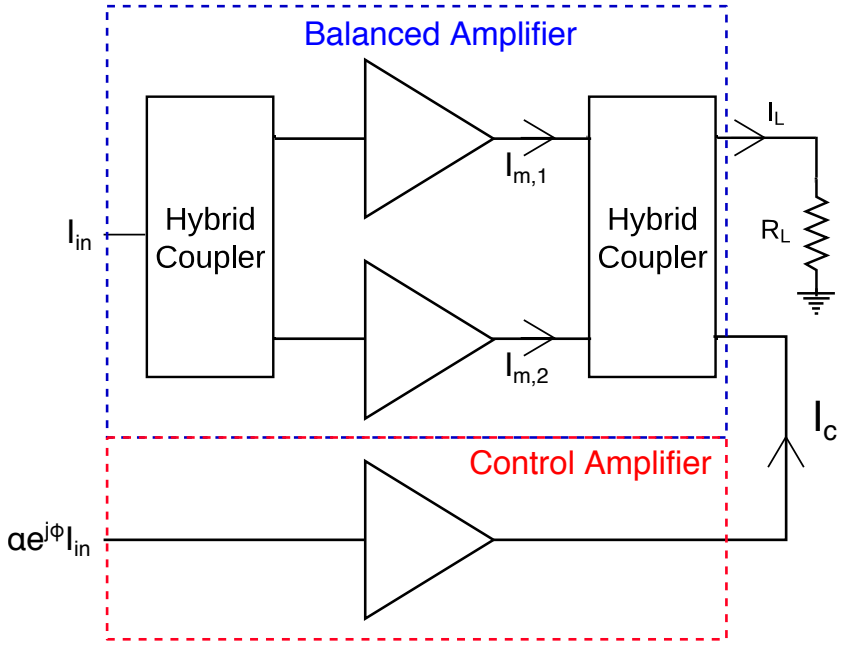


Figure 3.2: Load Modulatd Balanced Amplifier

$\Gamma_{m1,2}$ as

$$\Gamma_{m_{1,2}} = \frac{Z_{m_{1,2}} - Z_0}{Z_{m_{1,2}} + Z_0} \tag{3.1}$$

Where $Z_{m_{1,2}}$ is the impedance seen by the branch amplifiers and Z_0 the characteristic impedance of the system. The subscripts $m_{1,2}$ correspond to the branch amplifiers, denoted m_1 and m_2. The reflexion coefficient can also be defined as a power wave ratio :

$$\Gamma_{m1,2} = \frac{b_{m1,2}}{a_{m1,2}} \tag{3.2}$$

$$a_{m1,2} = \frac{V^+_{m1,2} + Z_0 I^+_{m1,2}}{\sqrt{Re\{Z_0\}}} \tag{3.3}$$

$$b_{m1,2} = \frac{V^-_{m1,2} - Z_0 I^-_{m1,2}}{\sqrt{Re\{Z_0\}}} \tag{3.4}$$

Where $V^{\pm}_{m1,2}$ and $I^{\pm}_{m1,2}$ are the corresponding forward and backward voltage and current waves.

In a Load Modulated Balanced Amplifier, the control amplifier generates a power wave inside the isolated port that is redirected towards each branch transistor's drain, effectively emulating a reflected wave. In this way, by controlling the magnitude and phase of this signal the reflexion coefficient Γ and thus the impedance $Z_{m_{1,2}}$ seen by each branch amplifier can be controlled. The load modulation is thus defined by the relative phase and magnitude of the current of the control amplifier.

Figure 3.3 presents the effects of the relative phase and amplitude of the control signal compared to the branch amplifier's signal. In figure 3.3(a) the phase of the control signal is held constant while its amplitude is varied. The magnitude of the reflexion coefficient $|\Gamma|$ will increase with respect to the ratio α of the power of the control amplifier to the branch amplifier. In figure 3.3(b) the magnitude of

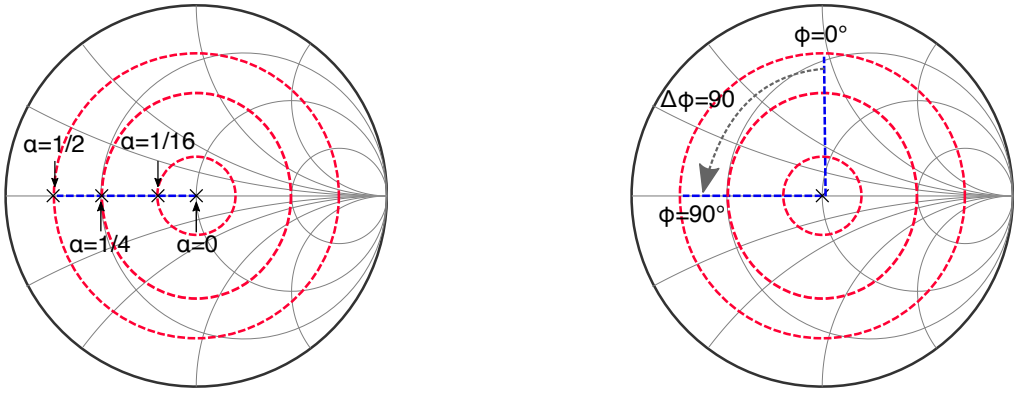


Figure 3.3: LMBA's load modulation mechanism. In (a) the relative magnitude of the control current is varied while the relative phase is held constant. In (b) the relative phase is varied while the relative magnitude is held constant.

the control signal is fixed while its phase is varied. This will result in a anti-clock-wise rotation of the reflexion coefficient in the Smith-chart.

The LMBA presents some fundamental differences compared to the previously studied load modulated architectures :

- The control amplifier, which could be compared to the auxiliary amplifier in a Doherty PA, is isolated from the balanced amplifier and therefore drives a fixed load. It is not load modulated.
- The load modulation is not dependent on the combiner. Indeed, as the control amplifier is isolated, the load modulation depends entirely on the relative amplitude and phase of the control signal.
- The hybrid coupler used as a combiner can be an ultra wideband component. If a Lange coupler is used for example, octave bandwidth can be obtained. The bandwidth is limited only by that of the individual power amplifiers comprising the LMBA.

In practice, a Load Modulated Balanced Amplifier is nothing less than an active load-pull transmitter.

In this chapter the concept and mathematical foundations of the Load Modulated Balanced Amplifier are presented, along with a bibliography of state-of-the-arts articles focused on the LMBA. In the second part of this chapter a new mathematical formulation is proposed that generalizes the LMBA operation to arbitrary load modulation trajectories. This analysis allows the prediction of the LMBA performance, and in particular the drain efficiency and AM-AM and AM-PM distortions from the performance of the branch amplifiers and the load trajectory. Finally, a design methodology inspired from this impedance based analysis is presented at the end of this chapter allowing the design of a linear/efficient LMBA from load pull data of the branch transistor.

This work is part of a PhD Student Exchange Program, and was done under the supervision of Pr. Taylor Barton in Colorado University.

State of the Arts of Load Modulated Balanced Amplifiers

The first paper published on the LMBA in 2016 presented this architecture as a reconfigurable power amplifier design [51]. The objective was to present wideband operation with high efficiency for different output power levels. The resulting amplifier reached more than 55% efficiency at 6 dB back-off

from 0.8-2GHz. To achieve such wide bandwidth, the authors chose not to implement any output matching network, only drain DC bias and second harmonic termination. The correct impedance for each frequency was synthesized through the LMBA operation. The control amplifier was not on the same board, and was fed with an additional RF port. Similarly, in [52] octave bandwidth operation was achieved, from 4.5GHz to 7 GHz with more than 60% drain efficiency at 7 dB back-off. This amplifier was designed for switched power state systems, where high efficiency over different output powers and frequencies is required. To maximize the efficiency, output matching networks were implemented in this design, resulting in slightly smaller fractional bandwidth. This two papers prove that the bandwidth of an LMBA transmitter is limited only by that of the constitutive transistors. In [53] the same concept of reconfigurable amplifier was done in MMIC technology, using Win Semiconductor's 0.25 μm GaN transistor. Power added efficiency above 35% was observed from 8 to 9 GHz for output powers ranging from 1.5W to 14.1W.

The first high-efficiency LMBA was presented in 2017 by Pr Barton in [54]. Both the balanced amplifier (BA) and the control amplifier (CA) are biased in class B, but the latter is designed to saturate early. Figure 3.4 presents conceptually the output power versus input power. In the low power region, both the balanced and the control amplifier are conducting. P_{rel}, defined as the ratio of the power of the control amplifier to a branch amplifier is held constant, and the load presented to the BA is fixed. When the CA compresses, P_{rel} increases, inducing load modulation. The resulting PA presented 41.7% back-off efficiency between 700-850 MHz. This paper also focused on the input ports architecture. So far, LMBAs were designed with two inputs, for the balanced and control amplifier respectively. In this paper, an input splitter between the balanced and the control amplifier is designed, resulting in an Single-RF Input LMBA. This concept was later applied to an octave-bandwidth amplifier. Using a phase-shifting Input Matching Network (IMN), a single-RF input amplifier was designed with 29-45% drain efficiency from 1.8 to 3.8 GHz with CW signals [55].

In 2018, a Doherty-like LMBA was presented [56]. In this architecture the balanced and control amplifiers are the equivalents of the main and auxiliary amplifier from the DPA. The control amplifier is not conducting until the breakpoint, inducing the two high-efficiency peaks. The resulting dual-input amplifier reached more than 39% drain efficiency from 1.7 to 2.5 GHz, proving once again the -relatively easily- wideband operation of the LMBA, even in Doherty-like operation. Under modulated stimulus, this amplifier presented 46%/43% PAE and -39dBc/-37dBc ACLR at 1.9 GHz and 2.1 GHz respectively. This paper also explored different input splitter functions that optimize efficiency or linearity. In [57] a single-RF input, Doherty-like amplifier is presented, along with a design methodology, following the black-box approach used previously in Doherty or Outphasing amplifiers. This

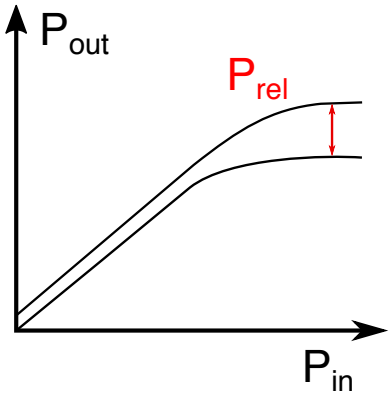


Figure 3.4: Output power of the main and the control amplifiers in the proposed High Efficiency LMBA. P_{rel}, the ratio of powers of the control amplifier to the balanced amplifier, increases in the high power region, resulting in load modulation.

paper analyses the Doherty-like operation from the LMBA's point of view, giving guidelines for the choice of the load trajectories, device relative size and biasing. The analysis of a static splitter based on the back-off range and the gain of each device is performed. The designed LMBA reached 54% and 67% drain efficiency at 6 dB back-off and maximum power, at 2.4 GHz, and 47% DE under a 10 MHz - 7.2 dB PAPR LTE modulated signal, but with only -29 dBc ACLR.

More recently, a Sequential Load Modulated Balanced Amplifier is introduced, presenting high efficiency for very large back-off ranges. In [58] 46.7% PAE is obtained at 10 dB back-off and 65% at maximum power from 3.05 to 3.55 GHz. Modulated measurements showed 43.6% PAE and -43.9 dBc ACLR with a predistorted 10 dB PAPR, 200 MHz LTE signal. Similarly, a wideband sequential LMBA was presented in [59], reaching with a 10 MHz, 9.5 dB PAPR signal 47%-58% drain efficiency from 1.6 to 2.6 GHz, but with best case linearity of -25 dBc ACLR.

These results show that the Load Modulated Balanced Amplifier is a versatile architecture, and can be adapted to many different configurations. It shows very high reconfigurability, and can be a great candidate for applications like software defined radio. The Doherty-like LMBA presents efficiency enhancement similar to its predecessor, while promising wider bandwidth. The LMBA can also achieve a linear operation with modulated signals (i.e. low ACPR) without digital predistortion, despite the gain compression observed in CW measurements. The sequential LMBA's achieved high efficiency at very high back-off ranges, at the detriment of linearity. Finally, the LMBA can be either used in dual-input or RF-input, depending on the application.

Load Modulation Mechanism

A more rigorous mathematical derivation can be done starting from the Z matrix of a hybrid coupler :

$$Z_{hybrid} = \begin{bmatrix} 0 & j & -j\sqrt{2} & 0 \\ j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & j \\ 0 & -j\sqrt{2} & j & 0 \end{bmatrix} \tag{3.5}$$

Where the ports are numbered like in figure 3.5, which represents schematically the LMBA concept. In this schematic the balanced transistors and control amplifier are represented by the current sinks I_{m1},I_{m2} and I_c respectively. The output is on port 4, which is loaded with a 50Ω resistor.

We can find the voltage at each port of the hybrid coupler based on the currents flowing in :

$$\begin{aligned} V_{m1} &= jZ_0(I_{m2} - \sqrt{2}I_c) \\ V_{m2} &= jZ_0(I_{m1} - \sqrt{2}I_L) \\ V_c &= jZ_0(I_L - \sqrt{2}I_{m1}) \\ V_L &= jZ_0(I_c - \sqrt{2}I_{m2}) \end{aligned} \tag{3.6}$$

On the output port we can write $V_L = -Z_0 I_L$. The current sources I_{m1} and I_{m2} are part of the balanced amplifier, and so their currents can be expressed as: $I_{m1} = I_m$ and $I_{m2} = -jI_m$. The previous equation can be rewritten :

$$
\begin{aligned}
V_{m1} &= Z_0 I_m \left(1 - j\sqrt{2}\frac{I_c}{I_m}\right) \\
V_{m2} &= -jZ_0 I_m \left(1 - j\sqrt{2}\frac{I_c}{I_m}\right) \\
V_c &= Z_0 I_c \\
V_L &= Z_0 I_m \left(j\frac{I_c}{I_m} - \sqrt{2}\right)
\end{aligned}
\tag{3.7}
$$

Finally, we can find the impedance seen at each port by dividing the voltage by the corresponding current, and considering $I_c = \alpha e^{-j\phi} I_m$:

$$
\begin{aligned}
Z_{m1} &= Z_0 \left(1 - j\sqrt{2}\alpha e^{-j\phi}\right) \\
Z_{m2} &= Z_0 \left(1 - j\sqrt{2}\alpha e^{-j\phi}\right) \\
Z_c &= Z_0 \\
Z_L &= Z_0
\end{aligned}
\tag{3.8}
$$

In the Load Modulated Balanced Amplifier, the impedance of the two balanced transistors can be modulated by the current of an isolated control transistor, and can take any value on the Smith-chart. This is why we consider the LMBA to be an active load-pull transmitter.

It is important to make sure that the total power injected in the system, i.e. the power of the balanced transistors and of the control amplifier is recovered at the output. The power at each port can be found as :

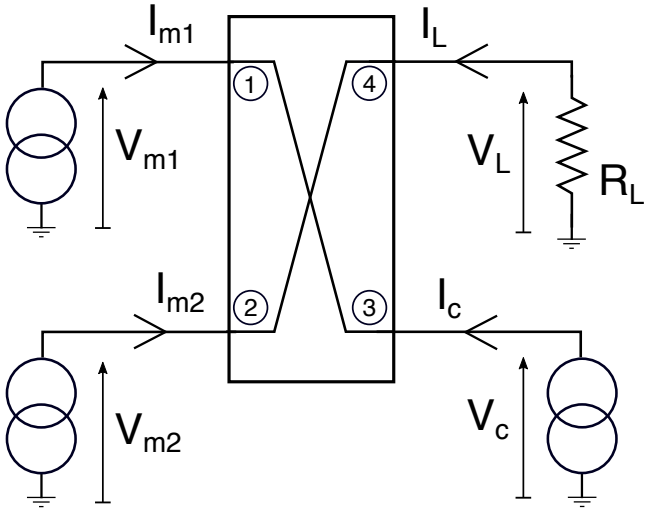


Figure 3.5: Schematic diagram of a Load Modulated Balanced Amplifier

$$\begin{aligned} P_{m1} =& \frac{I_m^2}{2} Z_0 Re\{1 - j\sqrt{2}\alpha e^{-j\phi}\} \\ P_{m2} =& \frac{I_m^2}{2} Z_0 Re\{1 - j\sqrt{2}\alpha e^{-j\phi}\} \\ P_c =& \frac{I_c^2}{2} Z_0 \\ P_L =& \frac{Z_0}{2} |I_m(j\alpha e^{-j\phi} - \sqrt{2})|^2 \end{aligned} \tag{3.9}$$

Which after rearranging becomes

$$\begin{aligned} P_{m1} =& \frac{I_m^2}{2} Z_0 (1 - \sqrt{2}\alpha \sin(\phi)) \\ P_{m2} =& \frac{I_m^2}{2} Z_0 (1 - \sqrt{2}\alpha \sin(\phi)) \\ P_c =& \frac{I_m^2}{2} \alpha^2 Z_0 \\ P_L =& I_m^2 Z_0 \left(1 - \sqrt{2}\alpha \sin(\phi) + \frac{\alpha^2}{2}\right) = P_{m1} + P_{m2} + P_c \end{aligned} \tag{3.10}$$

The power of the control signal is theoretically added to the balanced amplifier's power, regardless of their phase difference. Similar to the Outphasing amplifier, there is no power radiated in heat when the currents are in opposite phase.

We can also study the load modulation mechanism in terms of the reflexion coefficient :

$$\Gamma = \frac{Z_{m1} - Z_0}{Z_{m1} + Z_0} = -j \frac{\sqrt{2}\alpha e^{-j\phi}}{2 - j\sqrt{2}\alpha e^{j\phi}} \tag{3.11}$$

Considering the ratio of the power of the control amplifier to a branch amplifier :

$$\Delta P = \frac{P_c}{P_{m1}} = \frac{\alpha^2}{1 - \sqrt{2}\alpha \sin(\phi)} \tag{3.12}$$

We can find that :

$$|\Gamma|^2 = \frac{\Delta P}{2 + \Delta P} \tag{3.13}$$

Equation (3.13) shows what was intuitively explained at the beginning of this section. A constant ΔP ratio with a varying phase results in the Smith chart in a circle around the normalizing impedance Z_0.

Doherty-like LMBA

The previous equations explore the effects of a control signal injected in the isolated port of a balanced amplifier. We can apply them to a more concrete scenario, such as a Doherty-like operation, following the procedure presented in [57]. In this case the balanced and control amplifiers are considered as the main and auxiliary amplifiers respectively. The BA is biased in class B, and has to be

loaded with the required impedance to saturate at a predefined input voltage β_0. The CA is biased in class C, and will start conducting when $\beta > \beta_0$. In this simplified derivation the load trajectory is assumed to be purely real, leading to $\phi = \pi/2$. The branch transistors' current is defined as a half-wave rectified class B current, as described in chapter 1. The control transistor is modeled piece-wise linear, similar to the Doherty black-box calculations. The usual boundary conditions can be expressed as:

- $\beta \leq \beta_0$: the CA is turned off. The output power scales linearly with the input power. The impedance presented at the BA is equal to the characteristic impedance of the hybrid coupler, Z_0. At $\beta = \beta_0$ the BA starts compressing, reaching high efficiency. Its RF drain voltage is maximized.
- $\beta > \beta_0$: the CA turns on. The impedance seen by the BA is modulated according to (3.8), in order for the RF drain voltage to stay maximal while the current rises. When $\beta = 1$, both the balanced and control amplifier will saturate, reaching a second high efficiency peak.

The drain currents of the three transistors at the two boundaries are defined as:

$$\begin{aligned} I_{m1}\big|_{\beta=1} &= I_{max}/2 \\ I_{m2}\big|_{\beta=1} &= -jI_{max}/2 \\ I_c\big|_{\beta=1} &= \alpha I_{max}/2 \end{aligned} \tag{3.14}$$

$$\begin{aligned} I_{m1}\big|_{\beta=\beta_0} &= \beta_0 I_{max}/2 \\ I_{m2}\big|_{\beta=\beta_0} &= -j\beta_0 I_{max}/2 \\ I_c\big|_{\beta=\beta_0} &= 0 \end{aligned} \tag{3.15}$$

For high efficiency at back-off and maximum power, the branch amplifiers' RF drain voltage must be maximized, leading to

$$\beta_0 \frac{I_{max}}{2} Z_{m1}|_{\beta=\beta_0} = \beta \frac{I_{max}}{2} Z_{m1}|_{\beta=1} \tag{3.16}$$

$$\beta_0 = \frac{Z_{m1}|_{\beta=1}}{Z_{m1}|_{\beta=\beta_0}} \tag{3.17}$$

Recalling Z_{m1} from 3.8, and considering that $Z_{m1}|_{\beta=\beta_0} = Z_0$ and the phase shift $\phi = \pi/2$, the previous equation can be rewritten as

$$\beta_0 = 1 - \sqrt{2}\alpha \tag{3.18}$$

And so the required amplitude of the control PA's output current can be found as a function of the drive level

$$\alpha = \begin{cases} \frac{\beta-\beta_0}{\sqrt{2}} & \text{if } \beta \geq \beta_0 \\ 0 & \text{else} \end{cases} \tag{3.19}$$

The back-off dynamic range γ can be expressed as

$$\gamma = \frac{P_{out}|_{\beta=1}}{P_{out}|_{\beta=\beta_0}} = \left(\frac{1+\beta_0}{2\beta_0}\right)^2 \text{ or inversely } \beta_0 = \frac{1}{2\sqrt{\gamma}-1} \tag{3.20}$$

α can be expressed as a function of the back-off range :

$$\alpha = \sqrt{2}\frac{\sqrt{\gamma}-1}{2\sqrt{\gamma}-1} \tag{3.21}$$

Similarly the ratio of the power of the control amplifier to a branch amplifier :

$$\Delta P = \frac{P_c}{P_{m1}} = 2\frac{(\sqrt{\gamma}-1)^2}{2\sqrt{\gamma}-1} \tag{3.22}$$

An important aspect of the Doherty-like LMBA is the gain compression. Recalling what was said for the DLM, load modulation is accompanied by a gain compression. In the Doherty power amplifier this compression was compensated by the auxiliary amplifier, who was also load modulated. In the LMBA this is no longer the case, as the control amplifier drives a fixed load. We can estimate the gain compression :

$$G_c = \frac{P_{out}|_{\beta=1}}{P_{out}|_{\beta=\beta_0}}\frac{P_{in}|_{\beta=\beta_0}}{P_{in}|_{\beta=1}} = \frac{\gamma}{(2\sqrt{\gamma}-1)^2} \tag{3.23}$$

In other words, the Doherty-like LMBA is in theory an inherently non-linear amplifier.

Figure 3.6 compares the Doherty Power Amplifier (blue curves) to the Doherty-like LMBA (red curves). Fig. 3.6(a) presents the value of β_0 versus the output back-off, and 3.6(b) the back-off impedance normalized to the optimal maximum impedance versus the output back-off. We can see that for an identical back-off range, the back-off impedance required by the balanced amplifier of the LMBA is larger than that of the Doherty PA. A real transistor has a limited dynamic range over which high efficiency can be maintained through load modulation [60]. Thus, the higher the β_0 for a large back-off, the higher the efficiency a real transistor would present.

Fig. 3.6 (c) and (d) compare respectively the magnitude of the maximum current and maximum power ratios of the control (auxiliary) to the branch (main) amplifier. Looking at the current ratios, we can be surprised by the fact that the LMBA always requires a smaller current for the control amplifier, even for very large back-offs. This result is obtained here because in this methodology, the impedance at the drain of the control amplifier is fixed to Z_0. At maximum power the control amplifier is loaded with a much bigger impedance than the balanced amplifier, and thus requires a small current. In practice, a more interesting factor is the relative power ratio. While it is always smaller in the case of the LMBA than in the DPA, this ratio is much closer to what we could have expected. In practice, the control amplifier is probably matched with an OMN. This relative current ratio is actually observed at the drain of the branch amplifiers. Nevertheless,3.6(d) shows that for a given back-off, a smaller power is required from the control amplifier than from the auxiliary amplifier in a DPA. Furthermore, in the LMBA the control amplifier is compared to only one branch amplifier. The balanced amplifier as a whole has 3 dB more output power, further reducing the ratio of main to control power. This is one great advantage of the LMBA, in that a smaller device ratio is needed for a given back-off.

Finally, we can see in figure 3.6(e) the gain compression versus the output back-off range. As expected, while the DPA is -theoretically- perfectly linear, the LMBA presents sever compression. In

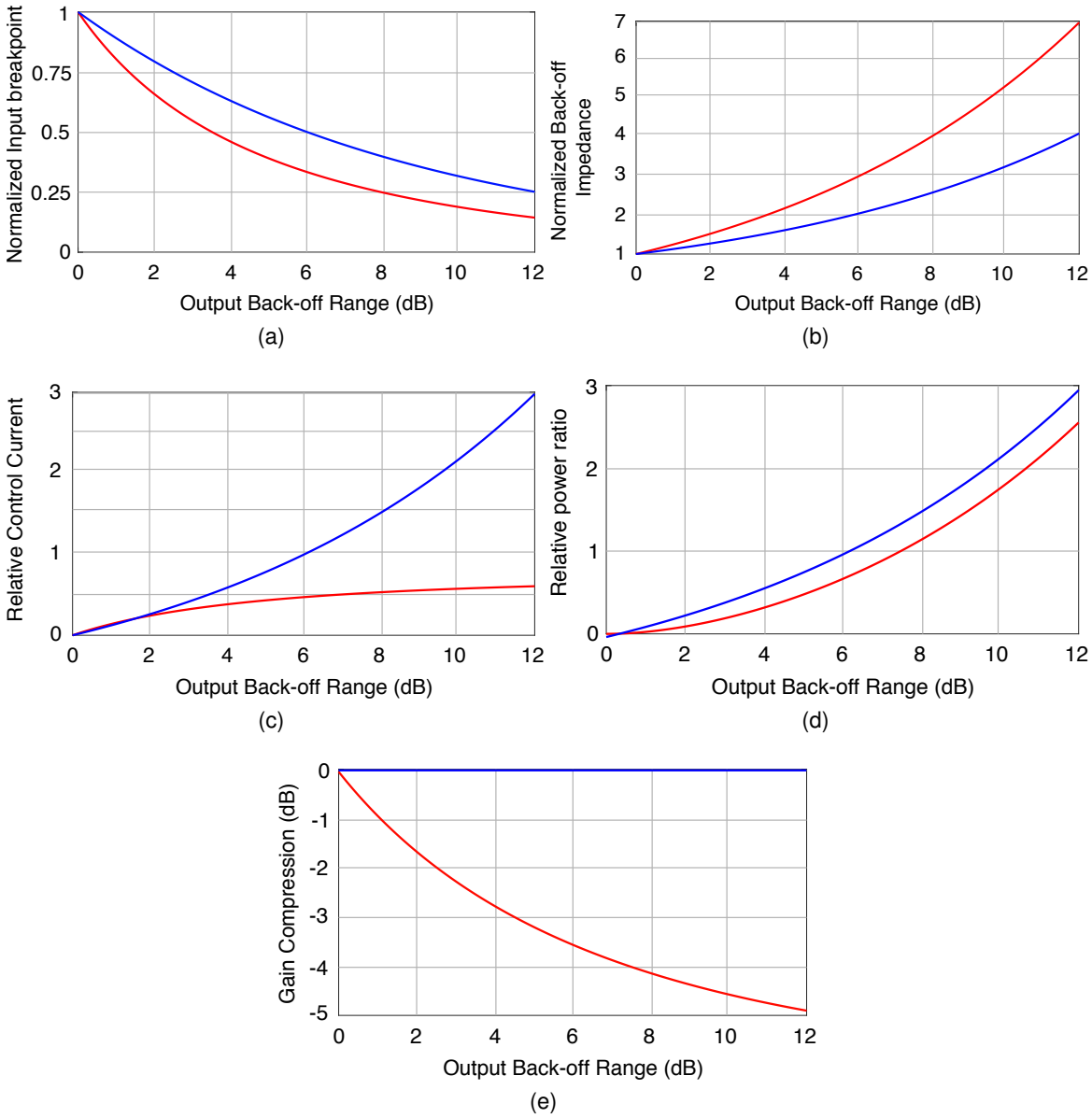


Figure 3.6: Comparison of a Doherty PA (in blue) and a Doherty-like LMBA (in red).

practice however, the DPA is found to also have a dip in the gain in the load modulation region. On the other hand, the different Doherty-like LMBA's found in the literature present a much smaller gain compression, in the order of 1-1.5 dB for 6 dB output back-off range. In [56], the authors also showed that appropriate input splitting function could attenuate even further this non-linear operation.

All in all the LMBA presents some real qualities for a high efficiency amplifier. Compared to the DPA, it should be able to reach similar efficiency enhancement, at least for a certain range of output back-off, while requiring a smaller control to main transistor size ratio. The bandwidth is limited only by that of the comprising amplifiers and octave-bandwidth operation has been shown in the literature. In dual-input mode, the LMBA can be reconfigured dynamically, as the load modulation is defined only by the relative phase and amplitude of the control transistor. This extra degree of freedom plays a role in the wide bandwidth of the architecture. At a first approach, the LMBA seems like an inherently non-linear amplifier, but some preliminary results show that linear operation could still be obtained without DPD. This is a very important issue and will be the subject of the next sections.

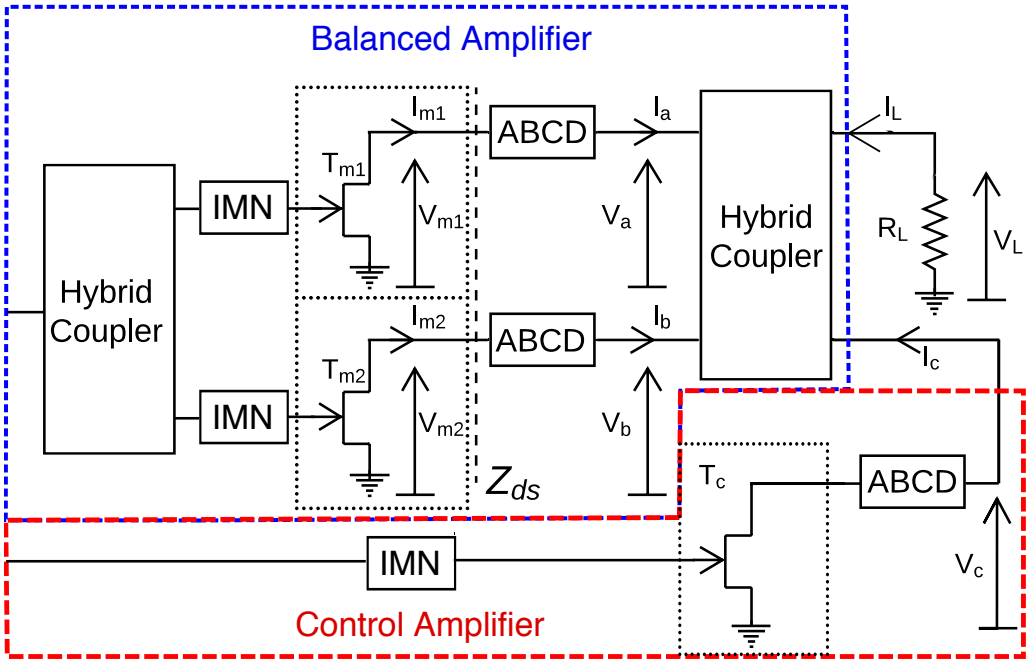


Figure 3.7: Schematic of the Generalized LMBA

3.2 Generalized LMBA Mathematical Analysis

In the previous section, the analysis was limited to a purely real load trajectory, i.e. $I_c = \alpha I_{m1}$ and $\phi = \pi/2$. This is based on the conventional Class B operation, which requires a real optimum resistance to maximize efficiency. In chapter 2, we saw that the optimum resistance design space could actually be expanded to include complex fundamental impedances associated with appropriate reactive second harmonic terminations. This broaden design space could eventually lead to solutions presenting a better trade-of between efficiency and linearity. Another approximation of the previous methodology is the absence of a matching network. The transistors' parasitics are neglected, and purely real impedances can be presented directly at the package plane. The control amplifier's drain voltage is adapted to present the required output power loaded with the same impedance Z_0 as the one required at back-off for the balanced amplifier, which also happen to be the characteristic impedance of the quadrature coupler. This is far from being realistic, as we know that transistors require complex impedances at their package plane, found usually through load-pull simulations. Furthermore, the drain voltage of the CA can only be adapted to a certain extent. In practice output matching networks (OMN) are designed to transform the output impedance Z_0 into the optimal impedance for each device.

We propose here an alternative design methodology, taking into account both the transistor's parasitics as well the requirement for an OMN. Whereas previous works have followed an analysis in terms of the back-off dynamic range parameter γ [57], here we focus on the load trajectory, based on the impedances selected at peak ($Z_{\max}$) and back-off (Z_{bo}) power levels. The subscripts bo and $\max$ describe the values of the different voltages/currents at back-off ($\beta = \beta_{\mathrm{bo}}$) and at peak power level ($\beta = 1$).

Fig. 3.7 shows a generalized schematic of the LMBA, consisting of the main balanced PA comprising the two hybrid couplers and main transistors $T_{m_1} T_{m_2}$, and the control PA comprising transistor T_c. We note here the following nomenclature: the subscripts *m1*, *m2*, *c* and *L* refer to the two branch transistors, control transistor and output port respectively. In order to perform the analysis at the intrinsic drain of the device, the ABCD parameter blocks in Fig. 3.7 representing the generalized

output matching networks (OMNs) and transistor parasitics (mainly C_{ds}) are de-embedded in the mathematical derivation. Once again, we will employ the Doherty-like LMBA approach, in which the control PA is turned on in the high-power region to generate load modulation [56, 57]. The boundary conditions are the same as in the previous section.

Combiner Operation

Based on the Z-parameter matrix of the (ideal) hybrid coupler with characteristic impedance Z_0, the voltages at the four ports of the coupler are written as:

$$\begin{aligned} V_a &= jZ_0(I_b - \sqrt{2}I_c) \\ V_b &= jZ_0(I_a - \sqrt{2}I_L) \\ V_c &= jZ_0(I_L - \sqrt{2}I_a) \\ V_L &= jZ_0(I_c - \sqrt{2}I_b) \end{aligned} \tag{3.24}$$

These expressions are de-embedded to the main transistors' intrinsic drain by replacing $\{V_a, I_a\}$ and $\{V_b, I_b\}$ with $\{V_{m1}, I_{m1}\}$ and $\{V_{m2}, I_{m2}\}$ through the ABCD matrix of the lossless OMN:

$$\begin{bmatrix} V_{m_{1,2}} \\ I_{m_{1,2}} \end{bmatrix} = \begin{bmatrix} a & jb \\ jc & d \end{bmatrix} \begin{bmatrix} V_{a,b} \\ I_{a,b} \end{bmatrix} \tag{3.25}$$

In back-off, the control amplifier is turned off according to the Doherty-like LMBA operation used here and in [57]. Therefore, there is no load modulation and the OMN must match Z_0 to the desired back-off impedance $Z_{\mathrm{bo}} = R_{\mathrm{bo}} + jX_{\mathrm{bo}}$. According to [61], the ABCD parameters can be directly calculated for a given Z_0, Z_{bo} and an arbitrary phase shift θ_{OMN}, assuming Z_0 is purely real:

$$\begin{aligned} a &= h(R_{\mathrm{bo}}\cos(\theta_{\mathrm{OMN}}) - X_{\mathrm{bo}}\sin(\theta_{\mathrm{OMN}})) \\ b &= jhZ_0(R_{\mathrm{bo}}\sin(\theta_{\mathrm{OMN}}) + X_{\mathrm{bo}}\cos(\theta_{\mathrm{OMN}})) \\ c &= jh\sin(\theta_{\mathrm{OMN}}) \\ d &= hZ_0\cos(\theta_{\mathrm{OMN}}) \\ h &= 1/\sqrt{Z_0 R_{\mathrm{bo}}} \end{aligned} \tag{3.26}$$

From the balanced amplifier operation the following relationships are known:

$$\begin{aligned} I_{m_2} &= -jI_{m_1} \\ I_L &= -\frac{V_L}{Z_0} \end{aligned} \tag{3.27}$$

Combining equations (3.24)–(3.27), the impedance presented at the main transistors' drains can be expressed as:

$$Z_{m_{1,2}} = Z_{\mathrm{bo}}\left(1 - j\sqrt{2}\frac{\sqrt{R_{\mathrm{bo}}Z_0}e^{-j\theta_{\mathrm{OMN}}}}{Z_{\mathrm{bo}}}\frac{I_c}{I_{m_1}}\right) \tag{3.28}$$

The voltages at the remaining ports of the hybrid coupler are

$$V_L = -Z_0\left(\sqrt{\frac{2R_{\mathrm{bo}}}{Z_0}}e^{-j\theta_{\mathrm{OMN}}} - j\frac{I_c}{I_{m_1}}e^{-2j\theta_{\mathrm{OMN}}}\right)I_{m_1} \tag{3.29}$$

$$V_c = I_c Z_0 \tag{3.30}$$

Equations (3.28), (3.29), and (3.30) describe the fundamental operation of the LMBA. By separately controlling the currents I_{m_1} and I_c the impedance seen by each main transistor can be changed, while the control amplifier is isolated and drives a fixed load.

Generalized Doherty-like Operation

Like in the previous section, we can apply the combiner equations to the Doherty-like currents. In order to establish current continuity between the back-off and load-modulation operating regimes as described above, at the break-point $\beta_{\rm bo}$ we can write:

$$\begin{aligned} I_{m1}|_{\beta=\beta_{\rm bo}} &= \beta_{\rm bo}\frac{I_{\max}}{2}e^{-j\Theta_{\beta_{\rm bo}}} \\ I_{m2}|_{\beta=\beta_{\rm bo}} &= -j\beta_{\rm bo}\frac{I_{\max}}{2}e^{-j\Theta_{\beta_{\rm bo}}} \\ I_{c}|_{\beta=\beta_{\rm bo}} &= 0 \end{aligned} \tag{3.31}$$

At peak drive when $\beta = 1$:

$$\begin{aligned} I_{m1}|_{\beta=1} &= \frac{I_{\max}}{2} \\ I_{m2}|_{\beta=1} &= -j\frac{I_{\max}}{2} \\ I_{c}|_{\beta=1} &= \alpha e^{-j\phi}\frac{I_{\max}}{2} \end{aligned} \tag{3.32}$$

With the phase of the current I_{m1} at maximum drive defined as the reference (zero) point, the currents I_{m1} and I_{m2} have in back-off a phase offset represented as $e^{-j\Theta_{\beta_{\rm bo}}}$. This factor, which we term the intrinsic LM-PM of the transistor, describes the phase variation of the intrinsic drain current due to the change of the operating point (both load impedance and input power) between the peak power and back-off power conditions. This effect results from the Miller effect and is dependent on the device technology. It is the source of the very high phase distortion in load modulated amplifiers, with typical values in the range of 10 to 30 degrees for GaN devices [62]. Because $\Theta_{\beta_{\rm bo}}$ depends on the nonlinear behaviors intrinsic to the device, we do not attempt to model it but will instead determine its behavior through large-signal load-pull simulation in the next section.

Requiring maximum efficiency at both back-off and maximum power results in the second boundary condition. For a generalized LMBA with complex impedances, maximum efficiency is obtained when the in-phase component of the drain voltage reaches the DC supply voltage. Equating these two voltages results in the following relationship between $\beta_{\rm bo}$ and the impedances $Z_{m_{1,2}}$ at these two power points:

$$\begin{aligned} \mathrm{Re}\left\{\frac{\mathrm{I_{max}}}{2}\beta_{\rm bo}\mathrm{Z_{m_{1,2}}}|_{\beta=\beta_0}\right\} &= \mathrm{Re}\left\{\frac{\mathrm{I_{max}}}{2}\mathrm{Z_{m_{1,2}}}|_{\beta=1}\right\} \\ \beta_{\rm bo} &= \frac{\mathrm{Re}\{\mathrm{Z_{m_{1,2}}}|_{\beta=1}\}}{\mathrm{Re}\{\mathrm{Z_{m_{1,2}}}|_{\beta=\beta_0}\}} \end{aligned} \tag{3.33}$$

Applying these boundary equations to the current I_L and the impedances seen by the main transistors yields:

$$Z_{m_{1,2}}|_{\beta=\beta_0} = Z_{\rm bo} \tag{3.34}$$

$$Z_{m_{1,2}}|_{\beta=1} = Z_{\rm bo} - j\sqrt{2}\alpha e^{-j\phi}\sqrt{R_{\rm bo}Z_0}e^{-j\theta_{\rm OMN}} \tag{3.35}$$

$$I_{L_{\rm bo}} = \frac{I_{\max}}{2}e^{-j\Theta_{\beta_{\rm bo}}}\sqrt{\frac{2R_{\rm bo}}{Z_0}}\frac{\mathrm{Re}\{\mathrm{Z_{m_{1,2}}}|_{\beta=1}\}}{\mathrm{Re}\{\mathrm{Z_{m_{1,2}}}|_{\beta=\beta_0}\}}e^{-j\theta_{\rm OMN}} \tag{3.36}$$

$$I_{L_M} = \frac{I_{\max}}{2}\left(\sqrt{\frac{2R_{\rm bo}}{Z_0}} - j\alpha e^{-j\phi}e^{-j\theta_{\rm OMN}}\right)e^{-j\theta_{\rm OMN}} \tag{3.37}$$

Finally, writing the impedance presented at maximum output power as $Z_{m_{1,2}}|_{\beta=1} = Z_{\max}$, with $Z_{\max} = R_{\max} + jX_{\max}$, the current factor $\alpha e^{-j\phi}$ can be related to $Z_{\max}$ and Z_{bo} as:

$$\alpha e^{-j\phi} = j\frac{Z_{\max} - Z_{\text{bo}}}{\sqrt{2R_{\text{bo}}Z_0}}e^{j\theta_{\text{OMN}}} \tag{3.38}$$

We can now express the load current I_L at back-off and peak power conditions based on the expected peak and back-off load impedances and the maximum current $I_{\max}$:

$$\begin{aligned} I_{L_{\text{bo}}} &= \frac{R_{\max}}{R_{\text{bo}}}\sqrt{2\frac{R_{\text{bo}}}{Z_0}}e^{-j\theta_{\text{OMN}}}\frac{I_{\max}}{2}e^{-j\Theta_{\text{bo}}} \\ I_{L_{\max}} &= \frac{Z_{\max} + Z_{\text{bo}}^*}{\sqrt{2R_{\text{bo}}Z_0}}e^{-j\theta_{\text{OMN}}}\frac{I_{\max}}{2} \end{aligned} \tag{3.39}$$

From (5.17) we can identify some key parameters of the LMBA. The output back-off and maximum power levels can be related to the maximum power of each branch transistor and the load trajectory:

$$\begin{aligned} P_{L_{\max}} &= P_{m_{max}}\frac{|Z_{\max} + Z_{\text{bo}}^*|^2}{2R_{\text{bo}}R_{\max}} \\ P_{L_{\text{bo}}} &= 2P_{m_{\max}}\frac{R_{\max}}{R_{\text{bo}}} \end{aligned} \tag{3.40}$$

Where $P_{m_{\max}}$ is the maximum power of the branch transistors $T_{m_{1,2}}$.

The dynamic range back-off range γ is written as:

$$\gamma = \frac{P_{L_{\max}}}{P_{L_{\text{bo}}}} = \left|\frac{Z_{\max} + Z_{\text{bo}}^*}{2R_{\max}}\right|^2 \tag{3.41}$$

We define the AM-AM distortion as the ratio of the gain of the LMBA at back-off and peak power. Similarly, the AM-PM distortion is described as the ratio of the phase of the output voltage V_L at the same power levels :

$$\begin{aligned} \text{AM}-\text{AM} &= \frac{P_{L_{\max}}/P_{in_{\max}}}{P_{L_{\text{bo}}}/P_{in_{\text{bo}}}} = \frac{|Z_{\max} + Z_{\text{bo}}^*|^2}{4R_{\text{bo}}R_{\max}}\frac{G_{m1_{\max}}}{G_{m1_{\text{bo}}}} \\ \text{AM}-\text{PM} &= \angle(\Delta V_L) = \angle(Z_{\max} + Z_{\text{bo}}^*) - \Theta_{\text{bo}} \end{aligned} \tag{3.42}$$

Equation (3.42) can be rewritten as:

$$\text{AM}-\text{AM} = \gamma\frac{R_{\max}}{R_{\text{bo}}}\frac{G_{m1_{\max}}}{G_{m1_{\text{bo}}}} \tag{3.43}$$

$$\text{AM}-\text{PM} = \text{atan}\left(\frac{X_{\max} - X_{\text{bo}}}{R_{\max} + R_{\text{bo}}}\right) + \Theta_{\text{bo}} \tag{3.44}$$

Here, $G_{m1_{\max}}$ and $G_{m1_{\text{bo}}}$ correspond to the gain of the main amplifiers at maximum and back-off power levels, and Θ_{bo} the previously defined load dependent current phase.

As can be seen from the derivation we propose, the AM-AM and AM-PM behaviors of the LMBA depend on both the behavior of the branch transistor ($G_{m1_{\max}}$, $G_{m1_{\text{bo}}}$, Θ_{bo}) and the selected load trajectory ($Z_{\max}$, Z_{bo}). Therefore, if the transistor's characteristics are well known, the impedance trajectory can be selected to influence the linearity in the LMBA architecture.

Control Amplifier Analysis

From (3.30), the control amplifier drives a fixed load; this is one of the main differences between the LMBA and DPA architectures. The control PA can therefore be designed independently of the main PA, and its input signal can be generated so that it provides the correct power level and phase to the balanced amplifier.

We can de-embed to the drain of T_c as in (3.25)–(3.26). The new ABCD parameters are:

$$\begin{aligned} a_c &= h_c(R_c\cos(\theta_c) - X_c\sin(\theta_c)) \\ b_c &= jh_cZ_0(R_c\sin(\theta_c) + X_c\cos(\theta_c)) \\ c_c &= jh_c\sin(\theta_c) \\ d_c &= h_cZ_0\cos(\theta_c) \\ h_c &= 1/\sqrt{Z_0R_c} \end{aligned} \tag{3.45}$$

Here, the load impedance presented to the control PA device is assumed to be some $R_c + jX_c$, with an arbitrary phase shift θ_c between the transistor and the hybrid coupler. Using (3.32), (5.17) and (3.45) we can write the control PA drain current current I_{ds_c} as:

$$I_{ds_c} = j\frac{I_{\max}}{2}\frac{Z_{\max} - Z_{\rm bo}}{\sqrt{2R_{\rm bo}R_c}}e^{j(\theta_{\rm OMN}+\theta_c)} \tag{3.46}$$

The required phase ϕ_c of this current for the correct load modulation is :

$$\phi_c = \arctan(Z_{\max} - Z_{\rm bo}) + \theta_{\rm OMN} + \theta_{\rm c} \tag{3.47}$$

The maximum power $P_{c_{\max}}$ needed from T_c to support the LMBA operation can be related to the maximum power of each main transistor:

$$P_{c_{\max}} = P_{m_{\max}}\frac{|Z_{\max} - Z_{\rm bo}|^2}{2R_{\max}R_{\rm bo}} \tag{3.48}$$

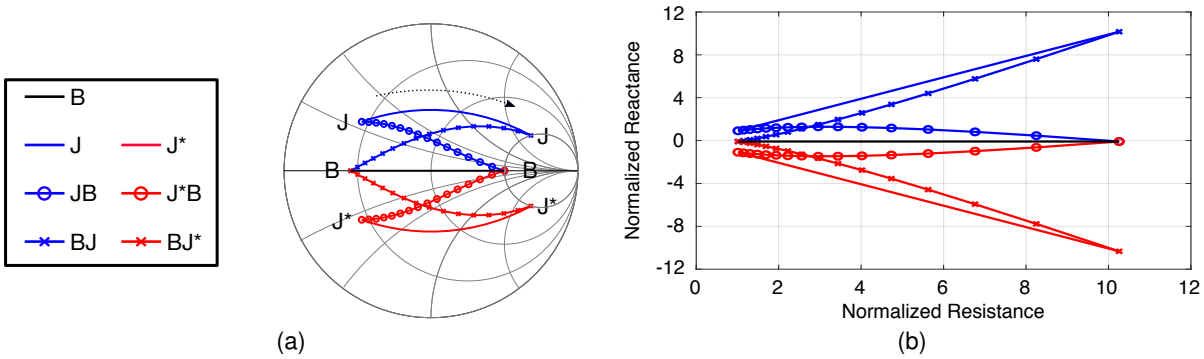
The correct phase and turn-on point can both be controlled by an appropriate input signal and gate bias.

The size of T_c, its drain voltage V_c and drain impedance Z_c can be chosen freely by the designer to achieve highest efficiency at the power level $P_{c_{\max}}$.

Impact of the load trajectory on the linearity of the LMBA

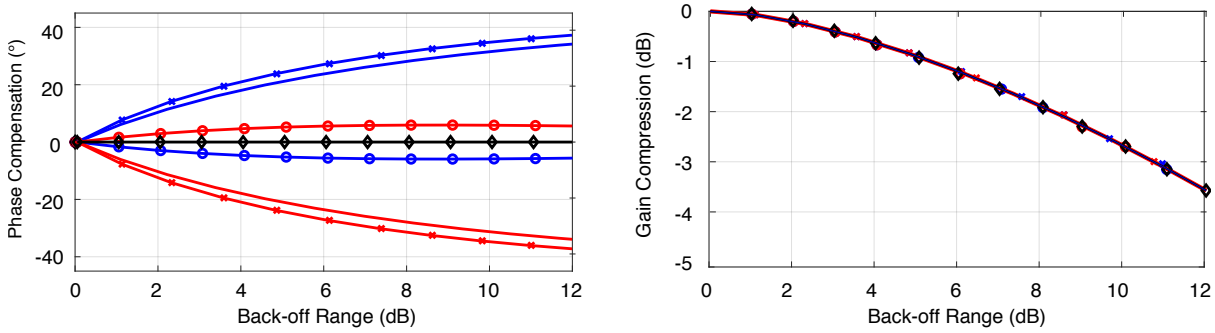
Based on the analysis in the previous subsections in terms of the load impedances presented at peak and back-off power levels, it is clear that the selected load trajectory will influence the LMBA linearity. Similarly, it is well known that load trajectory will determine the PA efficiency. Conventional load modulation assumes that a resistive load modulation is desirable [11, 63]. On the other hand, from (3.42) we observe that the AM-PM distortion for a purely real load modulation is equal to the intrinsic LM-PM ($\Theta_{\rm bo}$). This phase distortion can be substantial and depends on several factors such as device technology and operating frequency. If an appropriate reactive component to $Z_{\max}$ and/or $Z_{\rm bo}$ is introduced, it can compensate for the intrinsic LM-PM, leading to negligible net AM-PM distortion at the output of the LMBA, while also affecting efficiency.

Fig. 3.8 presents seven different load impedance trajectories, selected to explore the contributions of the load trajectory on the amplitude and phase distortion of the LMBA. Each trajectory has the same resistive component at the start (peak power) and end point (back-off power), but with different reactive components. The equations used to trace them are presented beneath. In these



(a) (b)

Figure 3.8: The seven load trajectories compared in this section: B (black), J and J* (solid blue and red), BJ and BJ* (blue and red, cross markers), and JB and J*B (blue and red, circle markers), presented in the (a) Smith chart, and (b) impedance plane.



(a) (b)

Figure 3.9: (a) Phase distortion and (b) gain compression versus γ for the different load trajectories presented in Fig. 3.8, calculated from (5.20)–(3.42).

equations, the parameter δ represents the relative value of the reactance, and takes the value of either 1 (J family of trajectories) or -1 (J* family of trajectories). $\beta_{\rm bo}$ is chosen in each case to produce 12 dB of dynamic range, according to (5.20). The drive parameter β is swept over $\beta_{\rm bo}$ to 1, producing the load modulation trajectories. We compare these modulation types which we name based on the starting and ending operating class as follows.

- **B**: (black curve) representing a purely resistive load modulation
- **J and J***: (solid blue and solid red) with a fixed reactance to resistance ratio, expressed by

$$Z(\beta) = \frac{1}{\beta}(1 + j\delta) \tag{3.49}$$

- **BJ and BJ***: (blue and red, cross markers) in which the reactance to resistance ratio varies from 0 to δ, according to

$$Z(\beta) = \frac{1}{\beta} + j\delta\frac{\beta_o - \beta}{\beta_o - 1} \tag{3.50}$$

- **JB and J*B**: (blue and red, circle markers) in which the reactance to resistance ratio varies from δ to 0, according to

$$Z(\beta) = \frac{1}{\beta} + j\delta\frac{\beta - 1}{\beta_o - 1} \tag{3.51}$$

Figs. 3.9(a) and (b) plot the AM-AM and AM-PM of the LMBA versus the back-off range, for each trajectory. They are computed according to (5.20)–(3.42), assuming $G_{m1_{\max}}/G_{m1_{\mathrm{bo}}} = 1$ and $\Theta_{\mathrm{bo}} = 0$. That way only the contribution of the load trajectory is plotted. While the naming convention used here is based on the B-J continuous modes, the analysis in this section is based only on fundamental frequency load trajectory and harmonic termination is for the moment not addressed.

We see that the AM-AM is similar for all trajectories and increases as we get into higher back-off ranges. Looking back at (5.20)–(3.42), we understand that the AM-AM is similar for all cases because they have identical resistive parts at both ends.

The AM-PM on the other hand ranges from 0 (class B case) to ± 40 degrees (BJ or BJ*) at 12 dB back-off. It is interesting to note that while the JB/J*B trajectories appear somewhat opposite to the BJ/BJ* in the Smith chart, their resulting AM-PM effects are comparatively small. This can be understood by looking at (3.42) : we see that for an identical resistive component variation, the phase distortion is defined by the absolute difference in reactance. We can therefore conclude that the preferred strategy to compensate for the intrinsic LM-PM distortion of the branch transistor is to introduce reactive loading at the back-off impedance.

3.3 Investigating the AM-PM / Efficiency compromise

From the previous section, we understand that a reactive load trajectory can be found that minimizes the AM-PM distortion of the LMBA. In the previous chapter we saw that harmonically tuned load modulated amplifiers, with appropriate reactive load trajectories could result into very high back-off efficiencies. We therefore need to find optimal second harmonic terminations and back-off and maximum fundamental impedances that will minimize the phase distortion while maximizing efficiency.

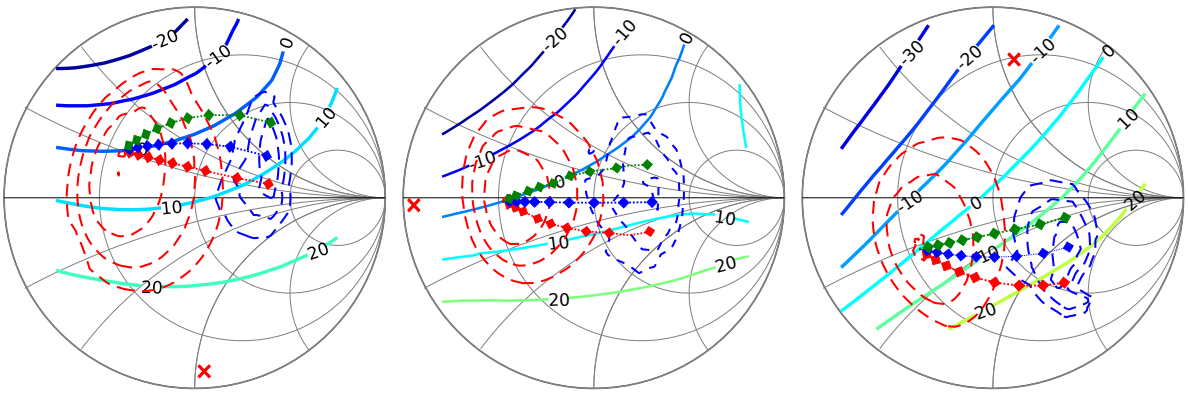
In this section an investigation of the optimal fundamental and harmonic impedances is performed on the CGH40010F device from Cree. Load pull simulations are used to identify the optimal impedances at peak and back-off power levels. Three different harmonic terminations are chosen, corresponding to class B, J and J* harmonic impedances. The load-pull procedure is as follows:

1. **Second Harmonic Termination** is selected. Three harmonic terminations are considered, that correspond to a class B, J and J* amplifier. Considering the theoretical maximum power of the device (41 dBm), the class B optimal resistance can be approximated according to (1.36). The fundamental and second harmonic impedances at the intrinsic drain plane can be calculated according to (1.36) for all three cases.

2. **Stability and Input Match.** A parallel RC network is designed to stabilize the transistor loaded with the previously found impedances. The resulting small-signal input impedance is then matched to $50\ \Omega$ with an additional input matching network (IMN). In this work, different IMNs are designed for the three example PAs.

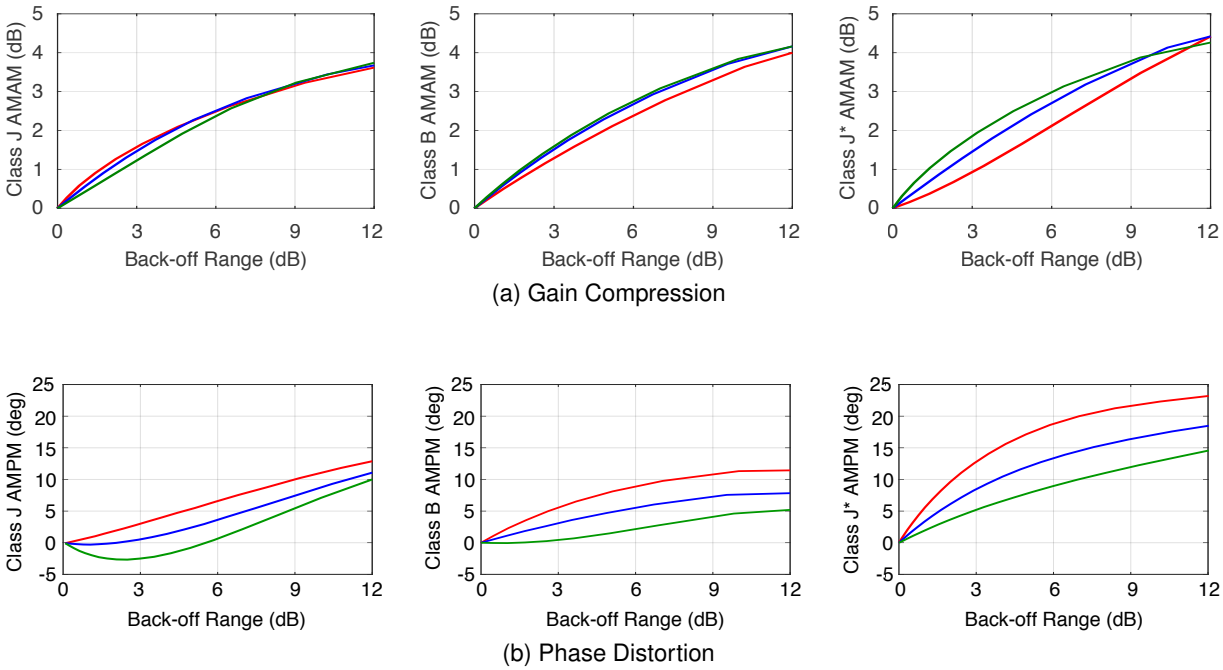
3. **Fundamental Load-Pull.** The fundamental impedance presented to the transistor's drain is swept. Here, reflection coefficient magnitudes up to 0.8 relative to the previously found Z_{opt} are simulated. An input power sweep is performed for each impedance and the gain, drain efficiency and phase distortion recorded.

Figs. 3.10 and 3.11 summarize the resulting load-pull data for class J, B and J* operation. In Fig. 3.10, the red cross marker shows the position of the second harmonic termination, reflecting the class of operation. The red dashed lines represent the power contours at a fixed 2 dB compression, the center being the impedance at maximum power for the given second harmonic. The blue dashed lines are drain efficiency contours at 37 dBm. The AM-PM contours are shown in colored curves. To generate them, the phase of the intrinsic drain current is first simulated at each load-pull impedance at low power (Pin= 15dBm). The zero phase reference point is selected to be the



(a) Class J (b) Class B (c) Class J*

Figure 3.10: Results of the load-pull measurements for the classes J/B/J*. The solid lines represent the intrinsic phase distortion contours. The dotted red and blue contours show respectively the maximum power and maximum efficiency at back-off. The red cross marks the second harmonic termination. The diamond markers represent the selected load trajectories.



(a) Gain Compression

(b) Phase Distortion

Figure 3.11: Estimated overall phase and amplitude distortion of an LMBA based on (3.42) and the load-pull data. In order to catch the distortion due to the load modulation only, the transistor is in a very linear zone, with input power of 15 dBm and 0 dB of compression.

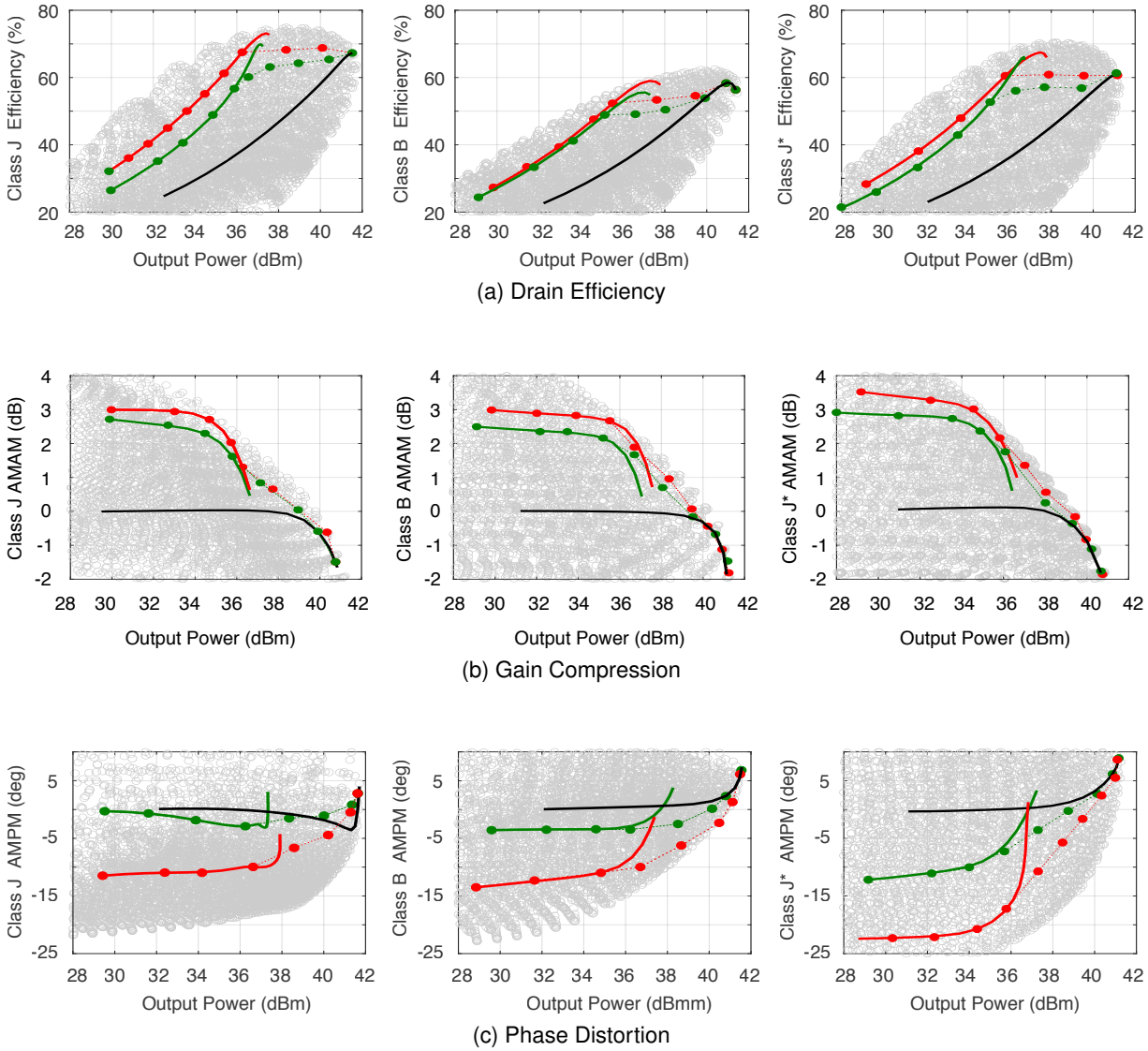


Figure 3.12: From top to bottom, simulated drain efficiency, gain compression and phase distortion for the class J/B/J*, from left to right. The gain compression and phase distortion take into account both the load-pull data and the load trajectory, according to (3.42).

peak-power impedance, i.e the intrinsic drain current phase for all other points is normalized to the value at the peak power impedance. The AM-PM distortion of the LMBA is then calculated based on equations (3.43)-(3.44), replacing Z_{Max} the peak-power impedance and Z_{BO} andΘ_{BO} by each load pull impedance and the corresponding normalized phase of the intrinsic drain current. That way, the AM-PM of the actual LMBA using this transistor under this harmonic loading is predicted from the load pull data. The effects of the second harmonic terminations on the fundamental impedance can be clearly seen, introducing the expected complex components from continuous mode theory. The AM-PM distortion also changes with the operating mode but with a weaker dependence.

Comparing the efficiency and AM-PM contours in Fig. 3.10, it is apparent that a range of back-off impedances can be selected with similar efficiency performance but with an approximately 10 degree range in AM-PM distortion. To illustrate this effect we consider three load trajectories that start from the same maximum power impedance but have reactive components at back-off.

In the blue trajectories the reactive to resistive ratios at peak power and back-off are equal, while in green/red this ratio becomes bigger/smaller in back-off. From Fig. 3.10 it can be seen that the back-off efficiencies of all three trajectories will be similar. Fig. 3.11 presents the predicted AM-PM and AM-AM of the LMBA versus the back-off power for each of these load trajectories. As in Fig. 3.10, these figures account for both the load-pull data and the load trajectory effects according to (3.42). They are taken at an input power equal to 15 dBm, and therefore only account for the load modulation, and not the transistor's intrinsic AMAM and AMPM non-linearities. The results in Fig. 3.11 show that the AM-PM distortion depends strongly on the selected load trajectory. For the B and J cases, we can find optimum impedances that minimize the phase variation, reaching only 6 degrees of distortion at 12 dB back-off. The class J* on the other hand shows greater than 15 degrees of AM-PM for all cases. In contrast, the AM-AM does not seem to depend as much on the load trajectory, with a worst-case variation of 1 dB in the J* case. Strong gain compression is expected in the LMBA architecture, as described in [57].

When input power variation is included in the simulation, the resulting performance is as seen in Fig. 3.12. Here, simulations are performed for the three different harmonic terminations at each load-pull impedance point with input power ranging from 15 to 35 dBm to generate each grey point in the "cloud."

It is worth noting that while all three PA classes reach similar maximum power levels, their drain efficiencies are not equal. The class J transistor reaches up to 75% drain efficiency, while the class B goes only up to 63% and the class J* to 70%.

The highlighted curves show the device performance over input power for three different drain impedances: the drain impedance that produces maximum output power according to Fig. 3.10 (black curve), and for the two back-off impedances corresponding to the decreased and increased reactance to resistance ratio impedances in Fig. 3.10 (red and green curves). Dashed lines represent the extrapolated performance of the load modulated amplifier, plotted by tracking the 1 dB compression point of each curve found over the load trajectory.

Two conclusions can be drawn from the load-pull data. Referring to the class J results in Fig. 3.12, we see that by sacrificing 8 percentage points of drain efficiency, the AM-PM distortion can be drastically reduced, from 12 degrees to 3 degrees. The AM-AM performance is largely unaffected by the selection of PA operating class. These results confirm what was observed in Fig. 3.11. The second conclusion is that when taking into account both the drain efficiency and the phase distortion, the class J appears superior to the other cases for our specifications.

3.4 Generalized LMBA design methodology

In the previous sections, a new mathematical formulation for a generalized LMBA was presented. Adding an Output Matching Network (OMN) between the hybrid coupler and the main and control transistors, arbitrary load modulation can be presented to the branch amplifiers. This analysis showed that the load trajectory could influence the overall AM-PM of the LMBA with an extra phase factor that either cancels or adds up with the intrinsic LM-PM of the branch transistors. Therefore, if the transistor's characteristics in terms of gain, phase distortion and efficiency are known for the back-off and peak-power impedances, the overall performance of the LMBA can be deduced, without having to design anything. The previous investigation also showed that by generalizing the LMBA operation to arbitrary complex impedances, optimal load trajectories could be found that maximize the linearity/efficiency trade-off.

Based on this research, a new methodology is proposed for the design of a Load Modulated Balanced Amplifier. It is based on load pull data of the device used as a branch PA. The methodology is as follows :

1. **Main transistor selection**. This choice is based on the required maximum power $P_{m_{\max}}$. We see from (5.19) that this power depends on the load trajectory, which is still to be determined. As an initial approximation we can consider the case where both Z_M and $Z_{\rm bo}$ are purely real. $P_{m_{\max}}$ then depends only on the overall output power and back-off range:

(3.52) $$P_{m_{\max}} = P_{L_{\max}} \frac{2\sqrt{\gamma} - 1}{2\gamma}$$

2. **Preparation for load-pull**. For the different second harmonic terminations to be considered for load-pull, the device is stabilized and the input matched to $50\ \Omega$. The harmonic impedances are determined for maximum efficiency at back-off, based on δ and $P_{\rm bo}$ according to (1.8) and (1.35)-(1.36).

3. **Load-pull and trajectory selection.** From the load-pull measurement we are interested in maximum power and drain efficiency contours, as well as AMAM and AMPM contours of the LMBA, such as those presented in figures 3.10, 3.11 and 3.12. First we select a peak-power impedance based on the desired output power / drain efficiency compromise. Then, for each load-pull impedance, the predicted back-off range, maximum power, AM-AM/AM-PM distortions and drain efficiency of the LMBA are calculated from (5.20)–(3.42). If the results are not satisfactory the second harmonic can be re-tuned and steps 2 and 3 repeated.

4. **Control transistor selection.** With the back-off and maximum impedance chosen, $P_{c_{\max}}$ can be found from (3.48). We can select a device that will give the highest efficiency for the desired output power, noting that standard PA design techniques can be used for the control PA due to its fixed load impedance.

5. **Passive network design** including the OMNs and the hybrid couplers.

This methodology can be employed for the design of a Doherty-like LMBA, and allows a straightforward choice of design trade-offs. We also notice that it can be used directly on a single-ended PA, to analyse its potential performance in a Doherty-like LMBA, without having to fabricate the whole load modulated amplifier.

3.5 Conclusion

In this chapter the Load Modulated Balanced Amplifier is presented, along with a mathematical derivation of the load modulation mechanism. A novel, Generalized Doherty-like LMBA analysis is then proposed, considering arbitrary impedances for maximum and back-off power levels. This approach suggests that the load trajectory impacts not only the output power and efficiency but also the linearity of the LMBA. An investigation of the optimal load trajectory in terms of efficiency and linearity is performed, reaching to the conclusion that a Class-J like load modulation results in high efficiency with minimal AM-PM distortion. A new design methodology is presented at the end of this chapter, inspired from the theory and the performed investigations. This methodology will be applied in the next chapter for the design of three harmonically tuned Load Modulated Balanced Amplifiers.

Chapter 4

Practical Design of a linear and efficient LMBA

The methodology presented in the previous chapter can be applied to any transistor technology and operating frequency. For the CGH40010F at 2.4GHz, it predicted that a class J harmonic termination should result in the best linearity/efficiency compromise. In this chapter we test this theory in two different scenarios.

In the first part, three LMBAs are desgined at 2.4 GHz, with 46 dBm maximum output power and 6 dB back-off. They are based on the same CGH40010F transistor as previously and have different harmonic terminations, operating in classes J, B and J* respectively. In the first section, load-pull simulation of the device is performed for each harmonic termination, in order to find the optimal back-off and peak-power impedances. Three PAs are then designed, that present in single-ended configuration the chosen back-off impedance. In section 2, the designed PAs are load pulled to find the optimal load trajectory, after fabrication. Finally, in section 3, the PAs are combined to create three harmonically tuned LMBAs. Since the control amplifier in the LMBA is isolated and drives a fixed load, it has only a small impact on the LMBA linearity. Therefore, since the control amplifier is not the main subject of research, the same PA design is used both for the branch and the control amplifiers. The three LMBAs can be compared, and the theoretical results of the previous chapter –showing the superiority of the class J both in terms of linearity and efficiency– can be assessed.

In a second part of this chapter, in section 4, the validity of the theory in a very different context is tested: a K band GaAs-based MMIC LMBA is designed in an attempt to reach a linear-efficient operation.

4.1 Design of three power amplifiers in classes J, B and J*

Selection of peak power and back-off impedances form load-pull measurements

In this section the methodology presented at the end of chapter 3 is applied to design three harmonically tuned LMBAs. The specifications are 46 dBm maximum output power and 6 dB back-off. The back-off power level is thus 40 dBm, resulting in 37 dBm per branch amplifier. The harmonic impedances for each amplifier at the package plane are chosen as $2 + j35$, $2 - j41$ and $1 - j4$. At the intrinsic drain plane, these impedances are the textbook optimal second harmonic terminations for a class J, B and J* operation respectively, considering the branch back-off power level of 37 dBm. The device is stabilized with the previously found network (4pF//8Ω and a shunt 40Ω resistor) and the input impedance is matched to 50Ω.

Figures 4.1–4.6 show the results of the load-pull simulations for the class J, B and J* second harmonic terminations respectively. We can see in 4.1,4.3 and 4.5 the drain efficiency (a), the

Table 4.1: Power levels of the branch amplifiers (subscript m), the control amplifier (subscript c) and the overall LMBA (subscript L) at back-off (subscript bo) and peak power (subscript max) and impedances selected for the three different classes of operation for the main PA.

	$P_{m_{\max}}$	$P_{m_{\mathrm{bo}}}$	$P_{c_{\max}}$	$P_{L_{\mathrm{bo}}}$	$P_{L_{\max}}$	γ	Z_{bo}	$Z_{\max}$	Z_{H2}
J	41.1	37	40.2	40	45.9	5.9	59 + j23	20 + j9	2 + j35
B	40.9	36.8	39.6	39.8	45.8	5.8	50 + j4	17 - j	2 - j41
J*	40.7	36.7	40.7	39.9	45.9	5.9	53 - j20	16 - j10	1 - j4

gain compression – or AM-AM– (b) and the phase distortion –or AM-PM– (c) versus output power. Figures 4.2, 4.4 and 4.6 present the load pull contours for each case at the de-embeded intrinsic drain plane (a) and at the package plane (b). In red we have the maximum power contours, in blue the maximum efficiency contours at 37 dBm (the branch back-off power) and in coloured lines the AM-PM normalized at the peak power impedance, taken at a gain compression of 1 dB. From these load pull results we can choose for each case the peak power and back-off power impedances, following this procedure :

- Choose peak power impedance, as a compromise between maximum power and drain efficiency.
- Choose a back-off power impedance. In our case we aim at an overall back-off power of 40 dBm (maximum power minus back-off range), resulting in 37 dBm per branch amplifier. We choose the back-off power impedance as a compromise between drain efficiency and gain compression at 37 dBm.
- Measure the resulting AM-AM, AM-PM, maximum power and back-off range of the corresponding LMBA, according to eq.b (5.19)–(3.42) with the selected impedances and considering the branch amplifiers maximum power to be 41 dBm.

In the drain efficiency, AM-AM and AM-PM plots we have highlighted in blue the curve corresponding to the back-off impedance and in red to the peak power impedance. The AM-AM and AM-PM plots are normalized by the value at low power (28 dBm) of the curve corresponding to the peak power impedance. The two chosen impedances are also shown with a green diamond on the Smith charts. We note here that both the AM-AM and AM-PM results include both the measured performance and the load trajectory effects, as in equation (3.8). The resulting characteristics of the LMBA for each harmonic termination for the chosen back-off and maximum impedance are presented in table 4.1.

These results bring the same conclusion as in the previous chapter. The class J second harmonic termination results in the best efficiency / linearity compromise. While the J* case presents high efficiency, it has a very strong AM-PM distortion in the load modulation zone. On the contrary, the class B case presents a relatively flat AM-PM, but at the cost of lower back-off efficiency.

Output Matching Network Design

Now that the different fundamental and harmonic terminations are chosen, we can design an Output Matching Network (OMN) that will transform the characteristic impedance Z_0 into the required impedances. The OMN starts by fixing Z_{H2} with an open stub and a transmission line. The rest of the OMN is a T-network that matches the fundamental impedance. The amplifier is stabilized with the previously found network and the input conjugately matched. The J,B and J* output matching

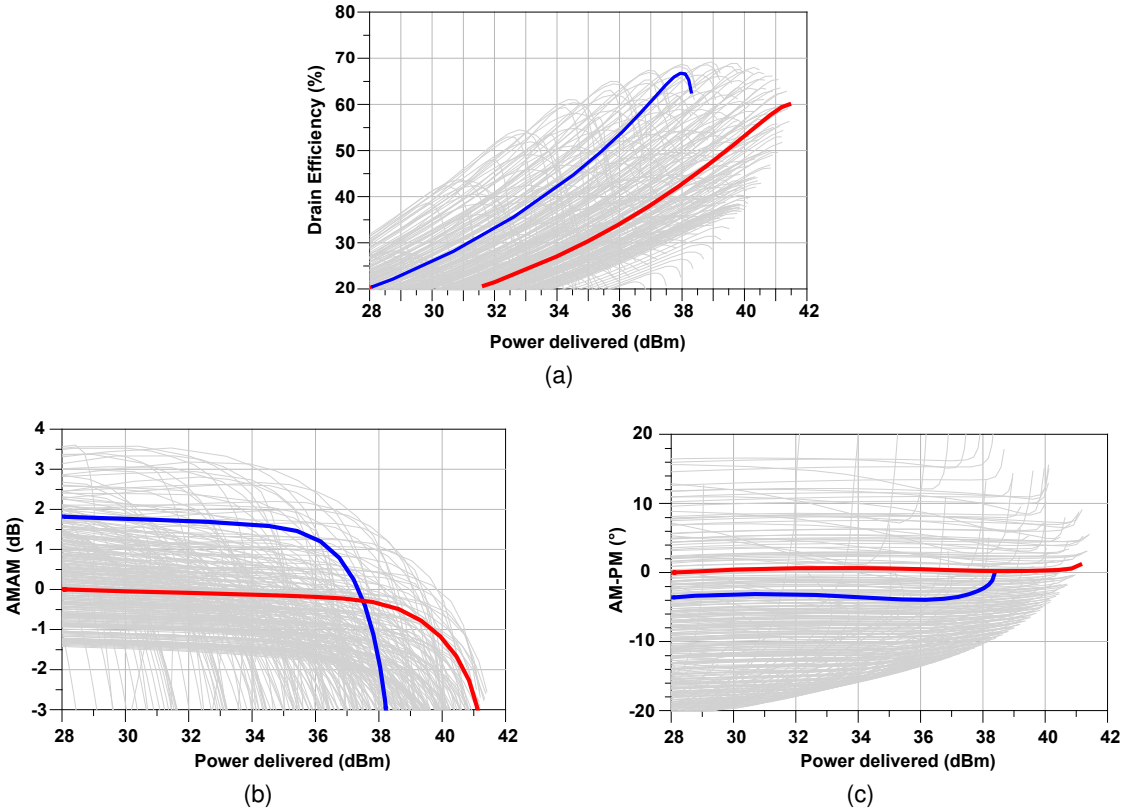


Figure 4.1: (a) Drain Efficiency, (b) AM-AM and (c) AM-PM versus output power for the class J second harmonic termination. Each grey curve corresponds to a different output impedance. The red curves correspond to the impedance resulting in maximum output power. The blue curves correspond the selected back-off impedance. AM-AM and AM-PM curves are normalized to the value at low power (28 dBm) of the red curve, corresponding to a peak-power impedance.

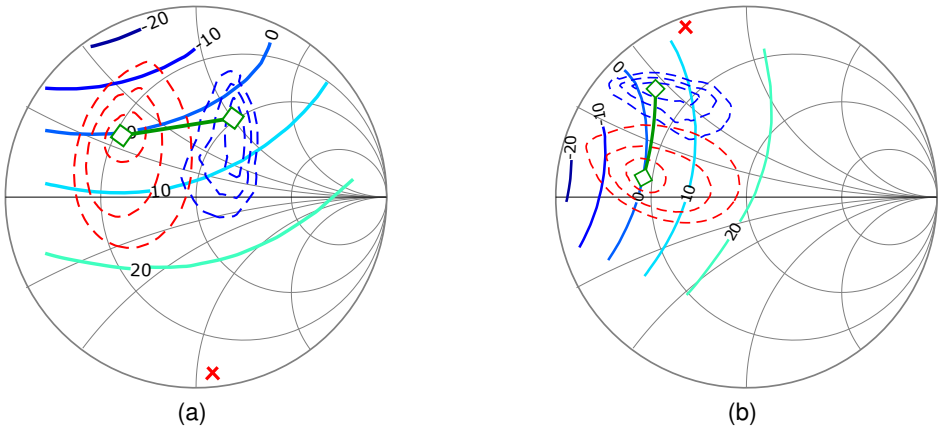


Figure 4.2: Load pull contours at the intrinsic plane (a) and package plane (b) for the class J second harmonic termination. Maximum power contours are in red, maximum efficiency contours at an output power of 37 dBm are in blue. The two diamond markers represent the impedances chosen for maximum and back-off power. The red cross represents the second harmonic impedance.

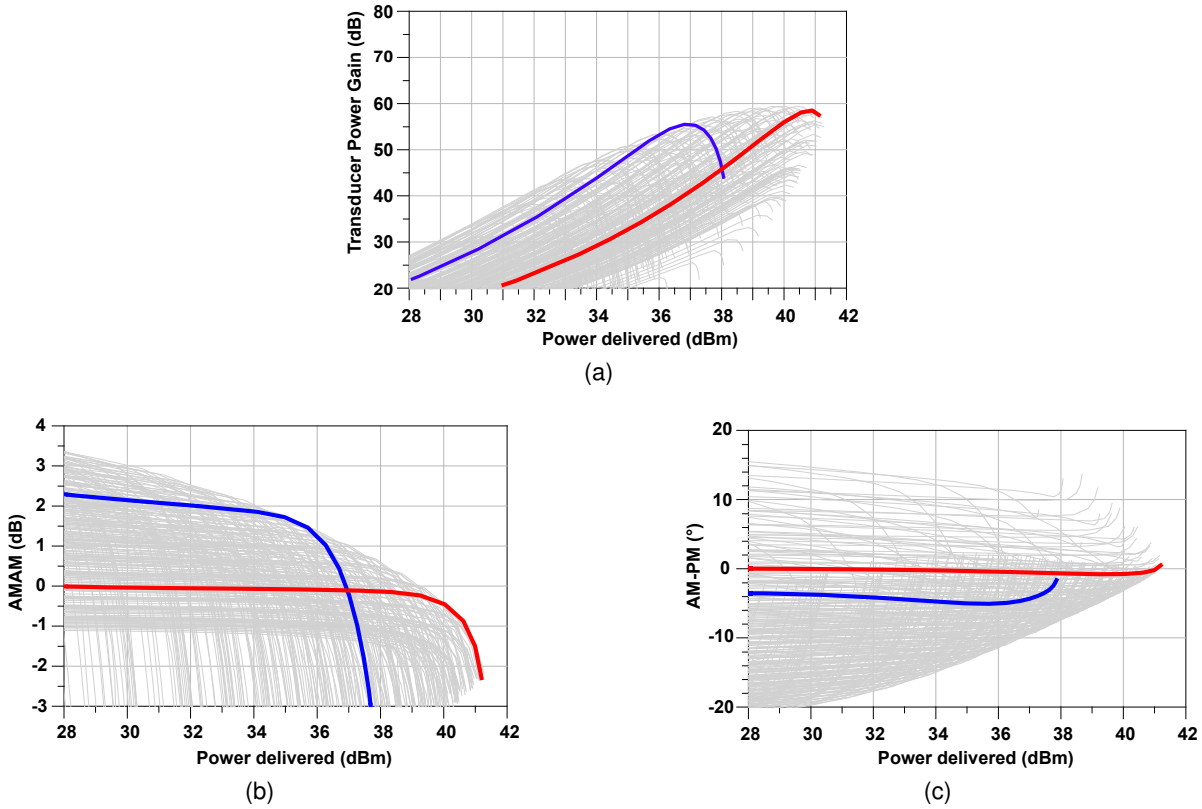


Figure 4.3: (a) Drain Efficiency, (b) AM-AM and (c) AM-PM versus output power for the class B second harmonic termination. Each grey curve corresponds to a different output impedance. The red curves correspond to the impedance resulting in maximum output power. The blue curves correspond the selected back-off impedance. AM-AM and AM-PM curves are normalized to the value at low power (28 dBm) of the red curve, corresponding to a peak-power impedance.

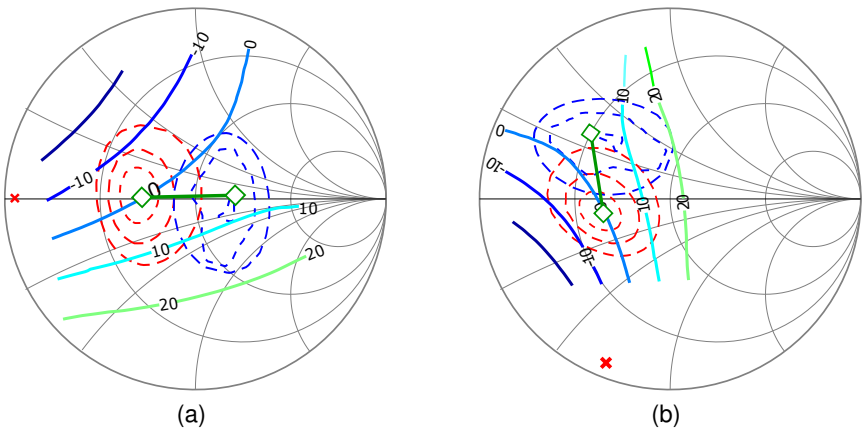


Figure 4.4: Load pull contours at the intrinsic plane (a) and package plane (b) for the class B second harmonic termination. Maximum power contours are in red, maximum efficiency contours at an output power of 37 dBm are in blue. The two diamond markers represent the impedances chosen for maximum and back-off power. The red cross represents the second harmonic impedance.

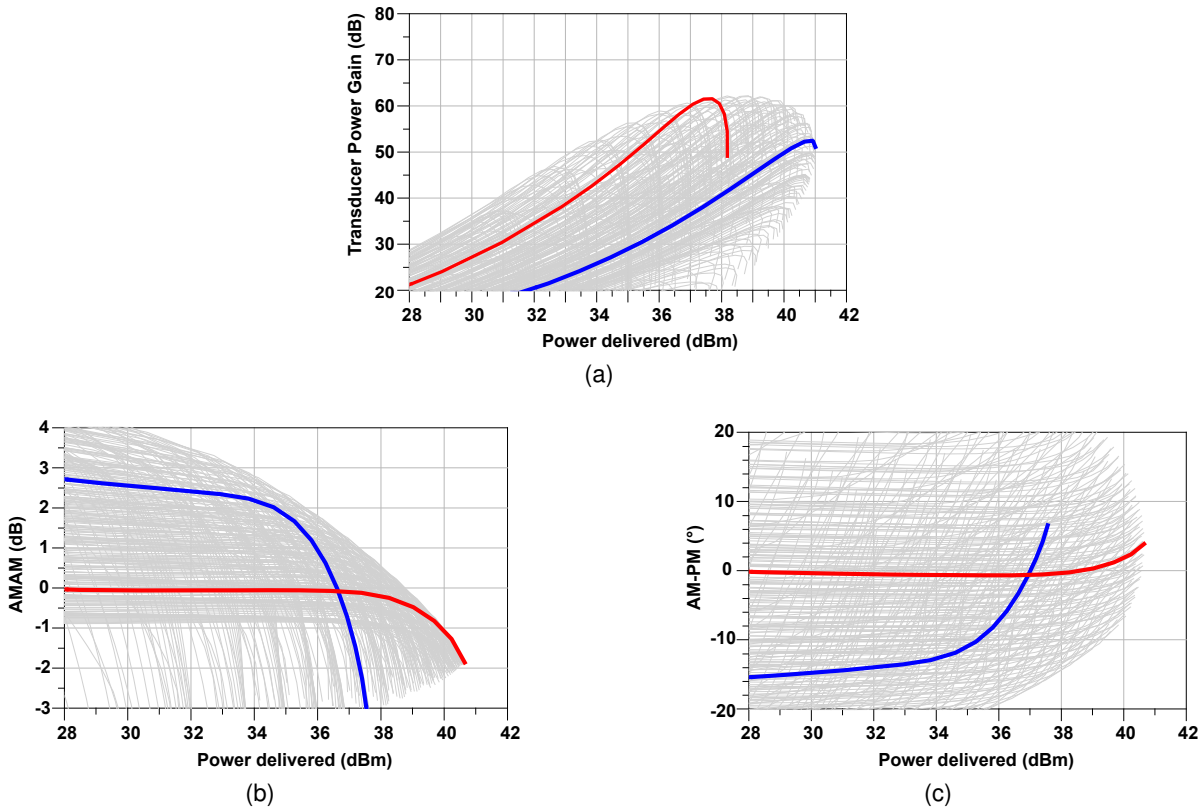


Figure 4.5: (a) Drain Efficiency, (b) AM-AM and (c) AM-PM versus output power for the class J* second harmonic termination. Each grey curve corresponds to ba different output impedance. The red curves correspond to the impedance resulting in maximum output power. The blue curves correspond the selected back-off impedance. AM-AM and AM-PM curves are normalized to the value at low power (28 dBm) of the red curve, corresponding to a peak-power impedance.

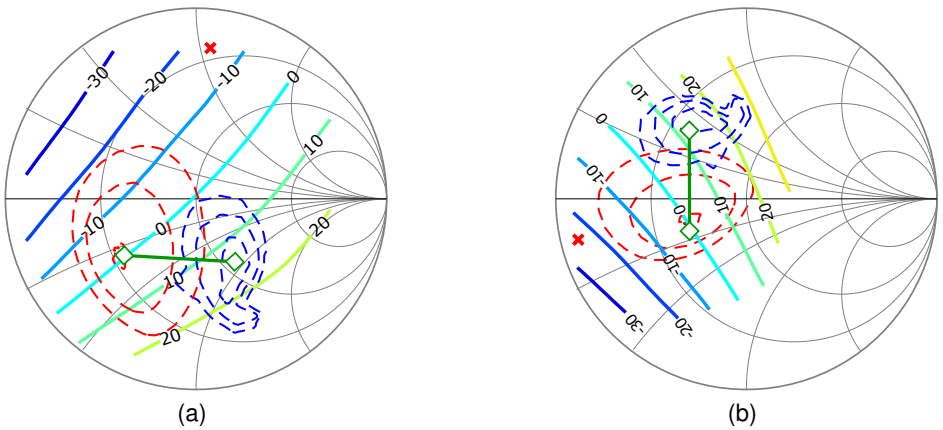


Figure 4.6: Load pull contours at the intrinsic plane (a) and package plane (b) for the class J* second harmonic termination. Maximum power contours are in red, maximum efficiency contours at an output power of 37 dBm are in blue. The two diamond markers represent the impedances chosen for maximum and back-off power. The red cross represents the second harmonic impedance.

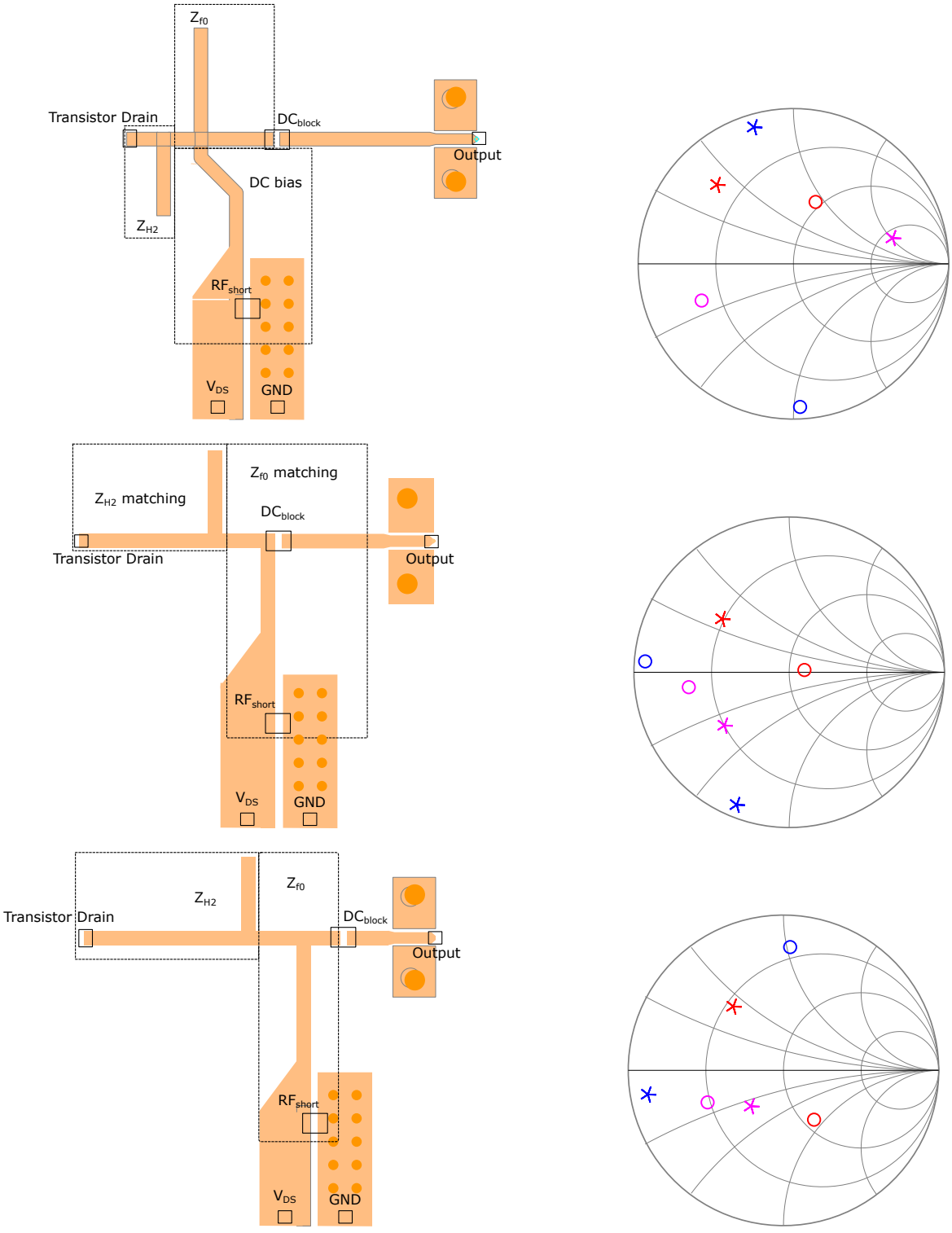


Figure 4.7: On the left, from top to bottom Output Matching Networks of the class J, B and J* PAs. On the right the resulting fundamental (in red), second harmonic (in blue) and third harmonic (in magenta) terminations at the intrinsic drain plane (with circles) and at the package plane (with stars).

networks can be seen on the left of figure 4.7, from top to bottom respectively. For the Class J, the T-network requires an open stub. The bias is thus provided through a quarter-wave length line,

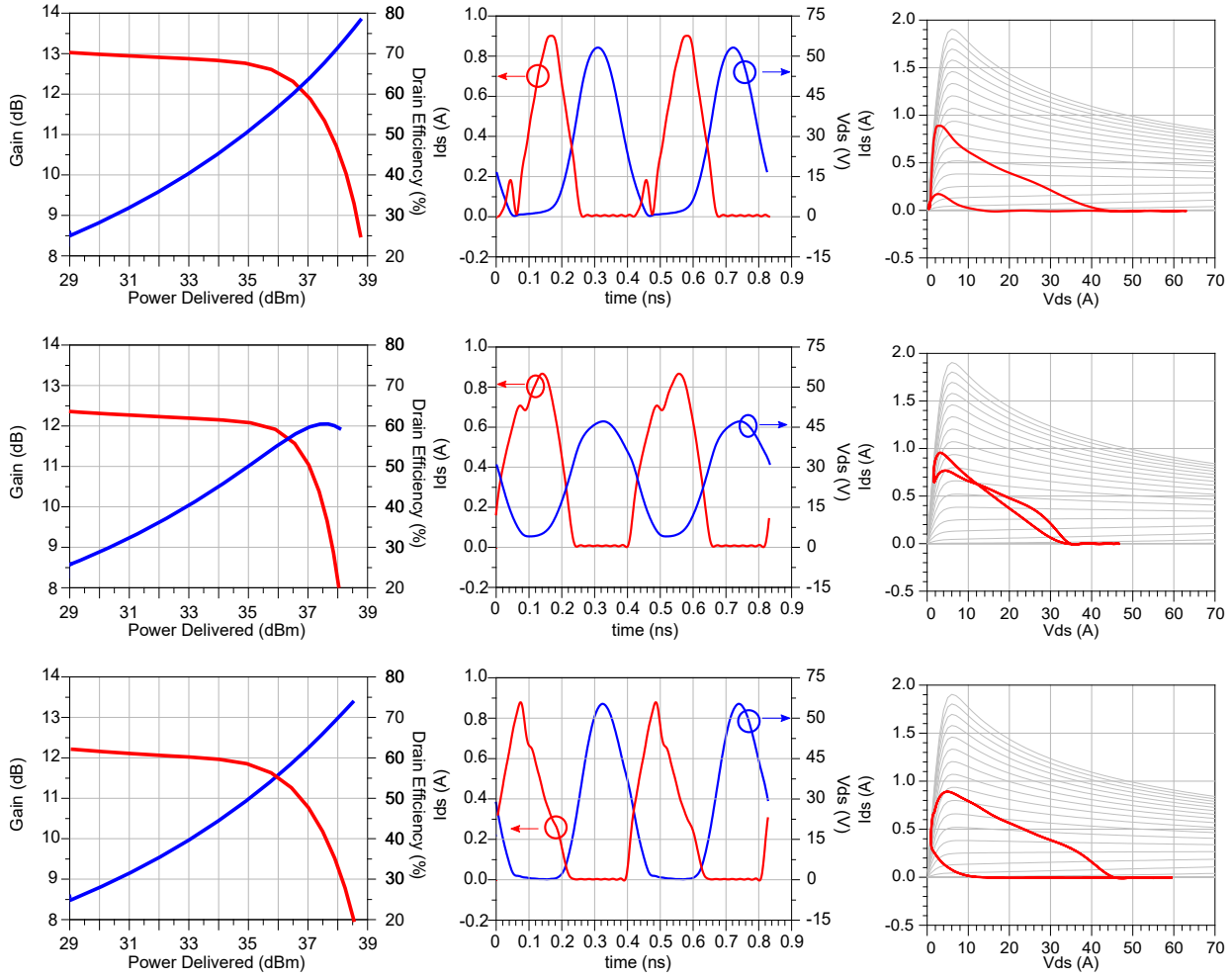


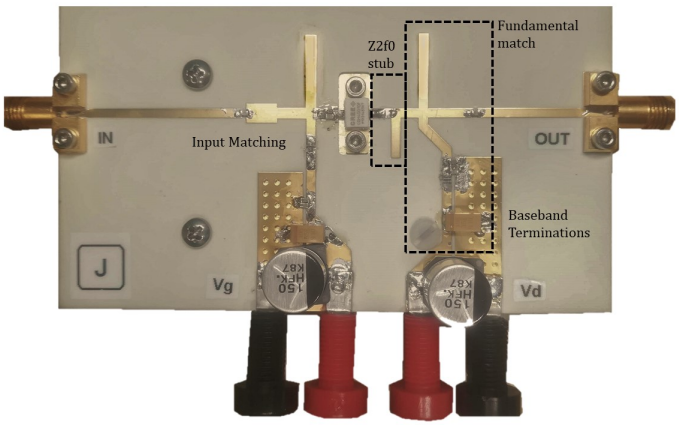
Figure 4.8: Simulated performance for the class J, B and J* amplifiers, from top to bottom. The left charts present the drain efficiency (in blue) and gain (in red) versus output power. The charts in the midle show the voltage (in blue) and current (in red) waveforms at 1dB compression. The charts on the right show the resulting load-line in red and in grey the DC drain current versus drain voltage for different gate voltages.

positioned after the matching network. For the B and J* case, a shorted stub is needed, the bias is thus included inside the matching network. On the right of figure 4.7 we can see the corresponding fundamental (in red), second (in blue) and third (in magenta) harmonic impedances presented at the intrinsic drain plane (with circles) and at the package plane (with stars). The fundamental impedance is taken at 2.4GHz.

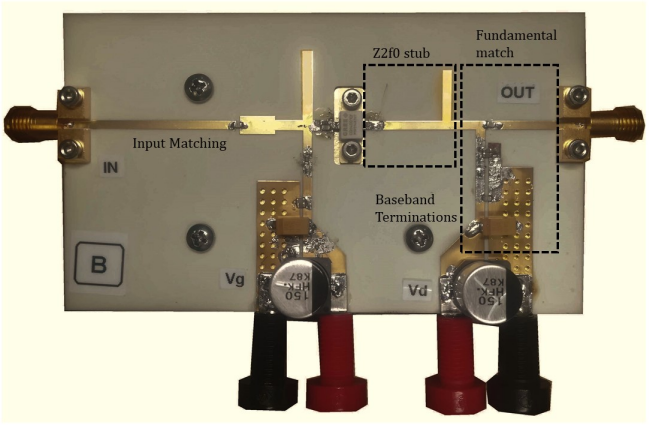
The layout of the three amplifiers were EM simulated with Keysight's Momentum electromagnetic simulator. The resulting PAs were then simulated with the Harmonic Balance engine of ADS. Gain and drain efficiency versus output power at 2.4 Ghz are presented in figure 4.8, along with the voltage/current waveforms and load line at 1 dB compression. We can clearly see the evolution of the voltage waveforms predicted from the continuous modes theory. The J/J* drain voltage peaks at a higher value than the class B, and is slightly phase shifted from the current waveform. The class B load line is –almost– a straight line, while the J/J* presents the hysteresis-like shape. As predicted, the class J presents the higher efficiency.

Measurement of the three power amplifiers' performance

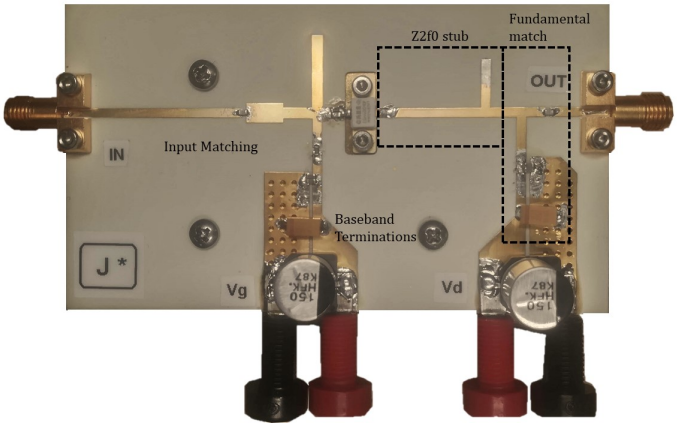
Figure 4.9 shows the three manufactured boards. 4 copies of each PA was realized by Circuits West on a 0.762mm Rogers 4350B substrate with gold plating.



(a) Class J



(b) Class B



(c) Class J*

Figure 4.9: Power Amplifier boards

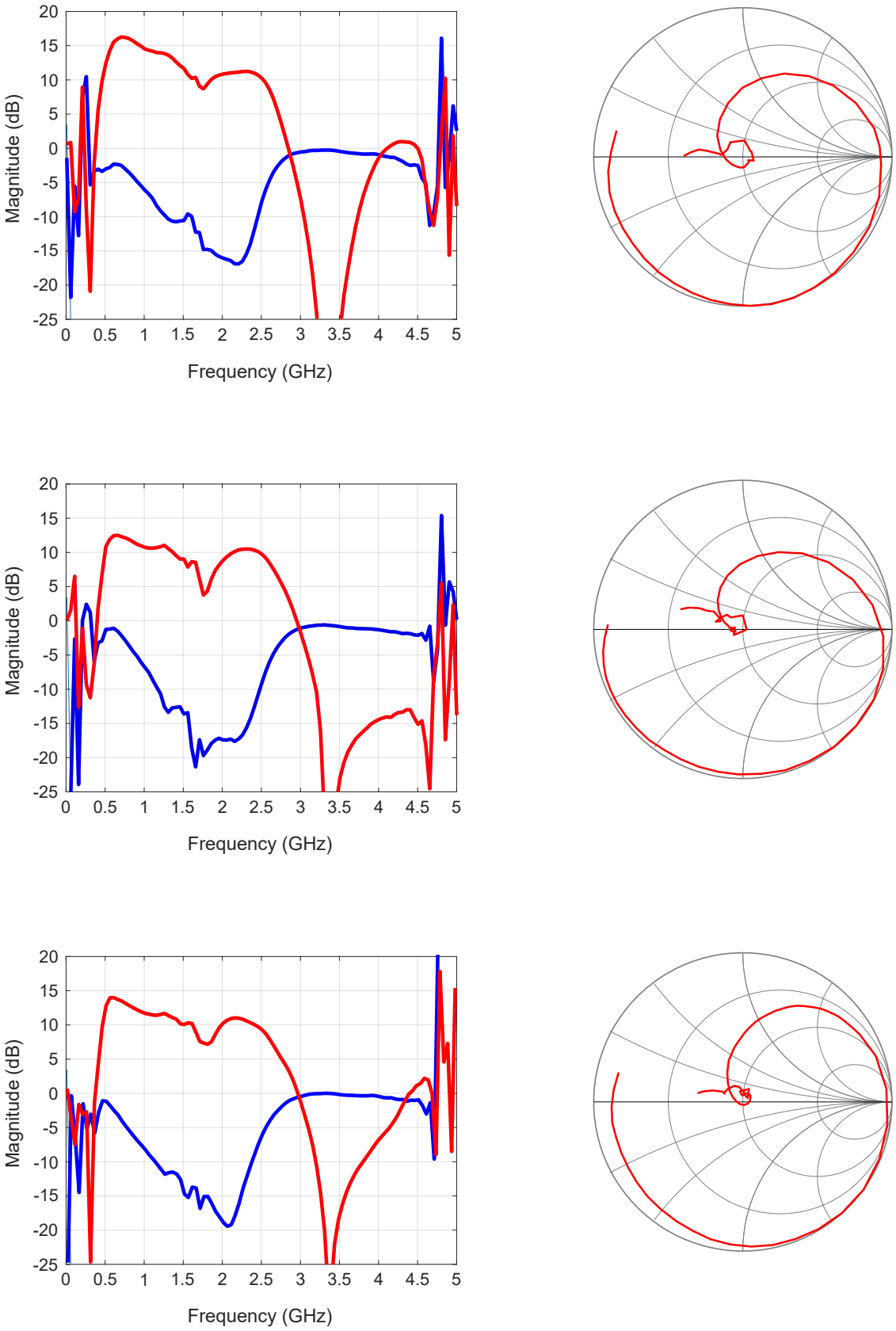


Figure 4.10: S parameters measuremets of the class J, B and J* boards, from top to bottom. On the left plots the S21 parameter is in red and the S11 in blue, and the Smith charts on the right present the S11.

On figure 4.10 we can see S Parameters measurement of each PA, made on a ZVA-40 Vector Network Analyser. For these measurements, the drain voltage was set to 28V and the quiescent current at 60 mA. We notice an S_{11} less than -10 dB and an S_{21} more than 10 dB at 2.4 GHz. We conclude that all the PAs are well matched, and present a reasonable gain. Looking at the K-factor, we see that the PA is potentially unstably around 1GHz. The stability network has to be tuned, changing the parallel capacitor from 4pF to 3.2 pF. This in turn impacts the resulting gain.

Figure 4.11 presents CW measurements of each amplifier, along with the simulated results. On

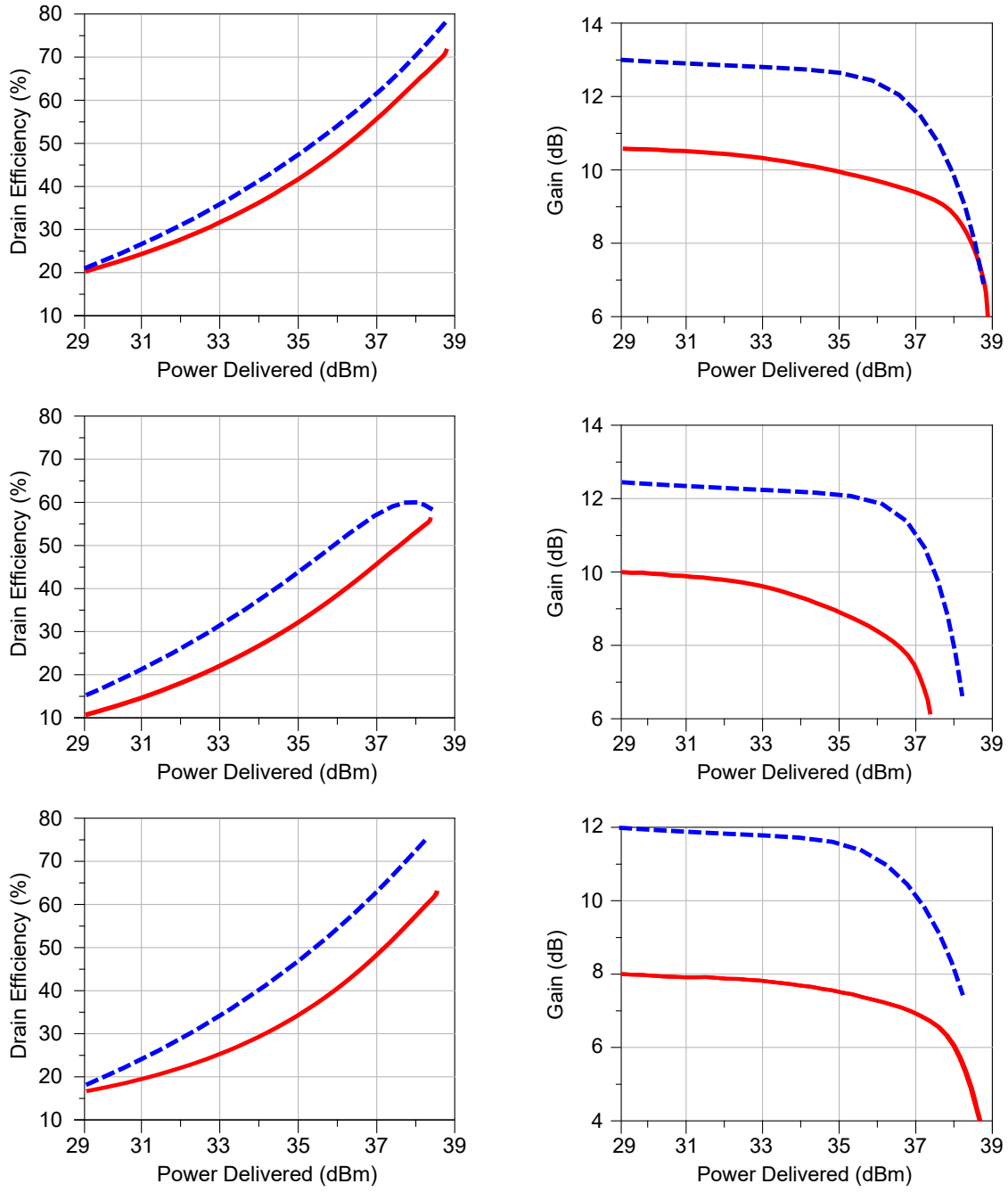


Figure 4.11: Measured and simulated results for the Class J, B and J*, from top to bottom. On the left the drain efficiency, on the right the gain. In red the measured performance, in dotted blue the simulated.

the left we can see the drain efficiency and on the right the gain. The test bench is based on a SMW-200A signal generator and an FSW40 signal analyzer, both from Rohde-Schwarz. A 40 dB gain, 40 dBm peak power driver is used at the input, and power sensors detect the input and output power level. Measured results are quite different from simulations. Both the gain and drain efficiency are substantially lower than predicted. Three different factors can explain this discrepancy :

- The lower stability capacitor decreases the overall gain. In an indirect way it also impacts the efficiency.
- The CGH40010F device model is known for overestimating the gain in simulation.
- We are using the device with a smaller drain bias voltage, for which the model is not as precise.
- OMN simulation was done only with ADS Momentum 2D simulator, and without taking into account the parasitics related to the SMD components. Starting 2GHz, it is common practice to use special Modelithics libraries that take this into account, and use HFSS 3D simulator to accurately design the matching network.

Despite the difference between simulation and measurement, the class J always has the best drain efficiency and the class B the worst. The class J* has lower drain efficiency than predicted, compared to the two other classes. We suspect that manufacturing inaccuracies are responsible for this lower performance, as even in simulation the J* design was very sensible to variations.

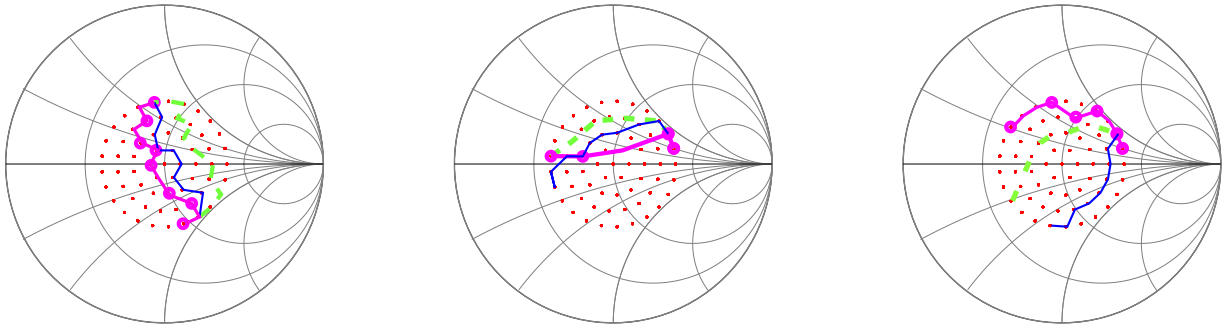
4.2 Load-pull measurement of the three Power Amplifiers

From a theoretical point of view, the LMBA operation is strictly equivalent to load-pull, as the control amplifier is isolated. In order to further investigate the impact on the LMBA operation of the second harmonic termination of the branch amplifier, all three PAs are load-pulled. One board of each amplifier was sent to Anteverta Microwave, a Maury Microwave subsidiary. By load-pulling the boards, the effects related to the fundamental impedance matching are canceled, and we can compare directly the effects of the different second harmonic terminations.

64 fundamental impedances were presented at the output, up to a reflexion coefficient of $|\Gamma| = 0.4$. The input power was also swept, from 5 dBm up to 30.5 dBm.

Figure 4.12 –4.13 presents the results of the load pull measurements. On figure 4.12 we can see in red dots the presented load-pull impedances. We have also plotted three trajectories, that result in maximum efficiency (blue trajectory), flat AM-AM (green trajectory) and flat AM-PM (magenta trajectory). Figure 4.13 presents the drain efficiency, AM-AM and AM-PM versus output power, for each input power level and output impedance. In black we present the results at 50Ω, i.e. the intrinsic performance of each board. We can also see the three previously defined trajectories on each plot. The maximum efficiency trajectory (in blue) was taken by tracking the convex hull of the drain efficiency. For the constant AM-AM and AM-PM trajectories, a gain and phase value was set as an objective, and the closest trajectory was plotted. The gain and phase objectives were chosen in a compromise between output power and efficiency.

Looking at the load trajectories of figure 4.12, we can directly see a very interesting result : in the class J and B cases, the maximum efficiency trajectory is in between the constant AM-AM and AM-PM, and all are very close. This directly shows that both cases can achieve simultaneously high efficiency along with high linearity. As predicted, this is far from being the case with the class J* : the maximum efficiency trajectory is at the opposite of the flat AM-PM, and very far from the flat AM-AM. In the class J case, both the maximum efficiency and flat AM-PM curves pass very close to the 50Ω impedance, showing that the amplifier is well matched on the output. In the class B case the curves are further away from the center of the Smith chart, but still not very far. In the J* case neither the



(a) Class J (b) Class B (c) Class J*

Figure 4.12: Optimal Load trajectories for maximum efficiency (in blue), constant AM-AM (in green) and constant AM-PM (in magenta) for each power amplifier.

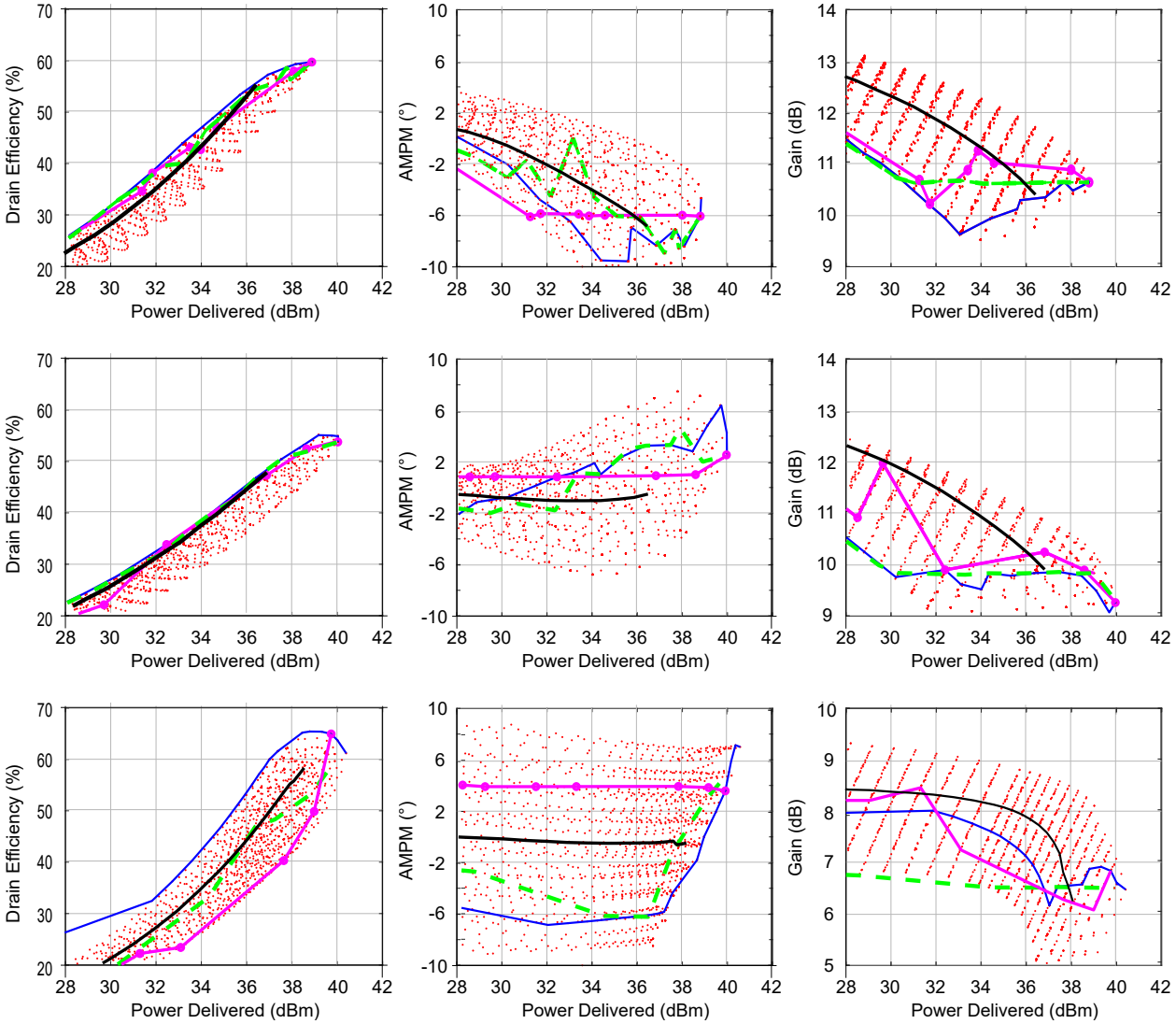


Figure 4.13: Load-pull measurements of the class J,B and J* amplifiers, from top to bottom. From left to right drain efficiency, AM-PM and gain versus output power. The black curve shows the results under 50Ω. The blue, green and magenta curves show the extrapolated results in a load modulation scenario, tracking the optimal trajectory for maximum efficiency, flat AM-AM or flat AM-PM respectively.

maximum efficiency nor the flat AM-AM or AM-PM trajectories are near the 50Ω impedance, showing that the transistor is poorly matched.

In figure 4.13 we can see from left to right the drain efficiency, AM-PM and gain versus output power. The results at 50Ω are plotted in black. The three trajectories are also highlighted in each plot. We notice that contrary to what was seen previously, the drain efficiency of the class J is relatively low, reaching only 55$\%$ at 50Ω. In the B and J* cases we are closer to what was seen in measurement and simulations. We observe the same in trend in terms of output power, as in the class J and B the maximum output power at 50Ω is less than 37 dBm, and the overall output power barely reaches 39 dBm in the class J. One explanation of these lower results comes from the input stability network. During the load-pull procedure, the parallel resistor broke and instability was observed at certain impedances. Another network was synthesized by the measurement engineer in order to properly stabilize the amplifier and improve the heat dissipation. This results in a higher low power gain but a large soft compression, i.e. the class J and B gains are constantly decreasing. Despite this, the measurement was done up to a gain compression of 4 dB. We therefore suspect that the amplifiers are not really at saturation, thus reaching lower output power and drain efficiency. This is not the case with the class J*, where the low power gain is flat and we can clearly see the compression. In this case we can be sure that the amplifier is driven into saturation, reaching maximum output power and efficiency. Another limitation of the measurement is the low reflexion coefficient, reaching a maximum Γ of 0.4.

Regardless of these issues, the results correlate what was speculated in the previous sections from simulations. In the classes J and B, quasi-constant AM-PM can be achieved while keeping very high efficiency. On the contrary, the class J* amplifier presents very strong AM-PM distortion, in the order of 14 degrees when tracking maximum efficiency.

4.3 Load Modulated Balanced Amplifier based on Harmonically Tuned Power Amplifiers

In this section we use the previous harmonically tuned power amplifiers to design three Load Modulated Balanced Amplifiers. The goal is to study the impact of the second harmonic termination of the branch amplifiers on the overall linearity and efficiency of the LMBA. Load-pull measurements from the previous section of the single-ended harmonically tuned PAs show that the class J and B amplifiers should be able to present almost constant AM-PM while keeping high efficiency, whereas the class J* has a very high AM-PM distortion. In table 4.1 we estimated the power of the control amplifier to be between 39.6 dBm and 30.7 dBm. The CGH40010F device can therefore be a very good candidate for this operation. As we have explained before, the control amplifier drives a fixed load, and conventional power amplifier design methods can be applied. Therefore, the control amplifier is identical to the branch amplifiers. The drain bias voltage is raised to 28V to deliver enough output power – around 40 dBm.

Investigation in simulation

Before making the LMBAs we investigate in simulation the load modulation operation. In order to eliminate various sources of errors such as the branch transistors non-linearities, we want the control signal to be an accurate image of the transistors drain current, i.e. $I_c = \alpha e^{j\phi} I_{m1,2}$. A first simulation is performed where the control amplifier is fed with a signal coming from the output of a branch amplifier. That way the resulting LMBA corresponds to an active load-pull system, and the load impedances presented at the drain of the branch amplifiers are not affected on the various parasitic effects such as compression. The simulation test-bench can be seen on figure 4.14. An ideal coupler with -30 dB coupling factor is used to connect the input of the control amplifier with the output of one

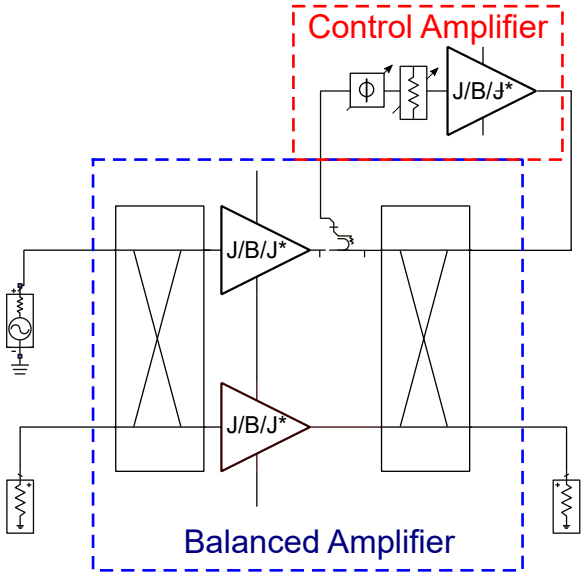


Figure 4.14: Simulation test bench of the LMBA

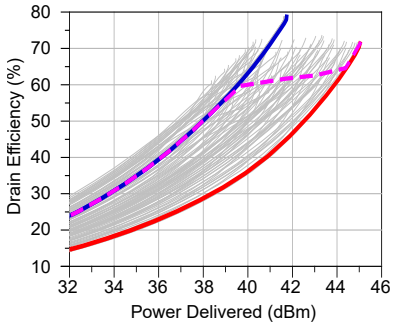
branch amplifier. The balanced amplifier is composed of two PAs connected together at the input and output with ideal hybrid couplers. A variable phase shifter and attenuator are added before the control amplifier –biased above pinch-off– in order to operate the load modulation. The phase of the control signal is varied from 0 to 360 degrees. The attenuator is set in a first step at -30 dB, in order to completely cancel the control signal, and is then varied accordingly to present a control to branch amplifier power ratio of -9dB up to 3 dB, in steps of 3 dB. This measurement is done for all three LMBAs. For simplicity, since the performance of the control amplifier affect mainly the efficiency of the LMBA, the control amplifier is always the same class as the branch amplifier.

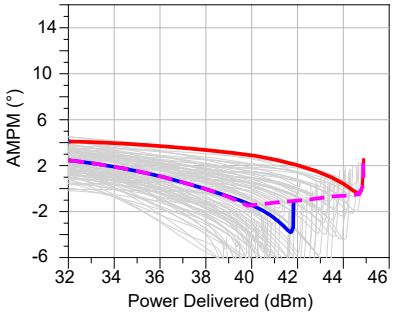
Figure 4.15 shows the simulation results. In grey we present the results for each relative power and phase. In blue the relative phase is -30 dB, resulting in practically zero control signal power. In red we have selected the curve that reaches highest efficiency. We have also plotted in magenta an extrapolated trajectory, corresponding to a Doherty-like operation. We notice that the peak-power is lower than expected, for all cases. We see that while the classes J and J* reach similar performance in terms of gain or drain efficiency, their phase response is very different. Both the classes J and B cases present in magenta an AM-PM smaller than 3°, while it is higher than 10° for the J*.

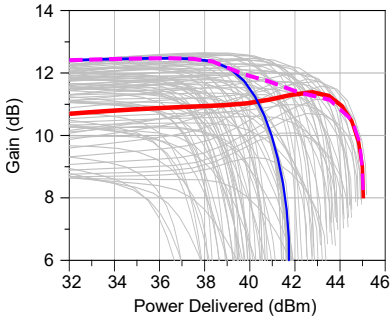
These results are in accordance with the conclusions drawn previously from the load-pull data of the single-ended amplifiers. This is a practical validation of the postulate that the performance of the Load Modulated Balanced Amplifier, in terms of both efficiency and AM-AM/AM-PM distortions, can be extrapolated directly from single-ended load-pull measurements of the branch amplifier. This is a very important aspect of the LMBA and a major advantage over other high-efficiency architectures. Indeed, the performance of a Doherty or Outphasing amplifiers cannot be accurately predicted, as they present mutual load modulation between the different constituents. In [64] a methodology to emulate a Doherty combiner and predict the Doherty characteristics from load-pull of a single-ended device is proposed, but this method requires extensive calculations, multiple steps, three different load-pull procedures and the design –in simulation– of the combiner. The LMBA on the other hand requires only one load-pull measurement, in order to select the optimal load trajectory, and all the other requirements can be calculated from the back-off and peak-power impedances.

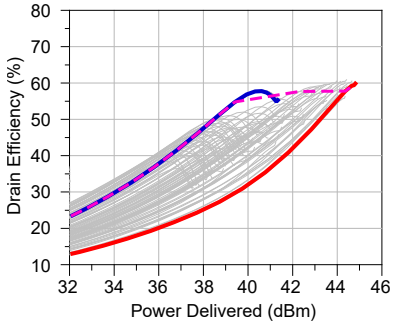
The LMBA is also simulated in pseudo-RF input, Doherty-like configuration

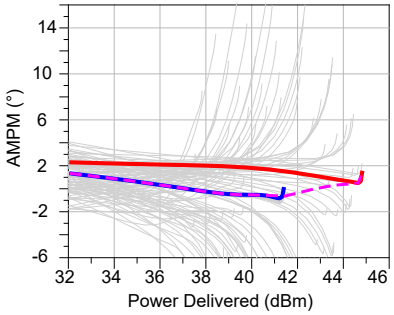
- The same signal is fed to the balanced and control amplifiers, emulating a symmetrical, static splitter. A fixed phase-offset between the two inputs is added to control the load trajectory's

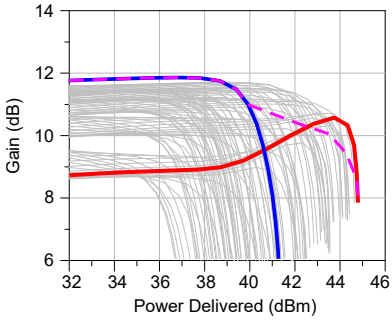

Drain Efficiency (%)
Power Delivered (dBm)

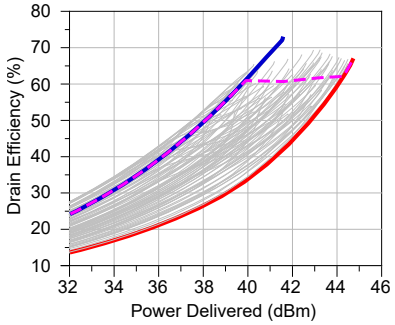

AMPM (°)
Power Delivered (dBm)

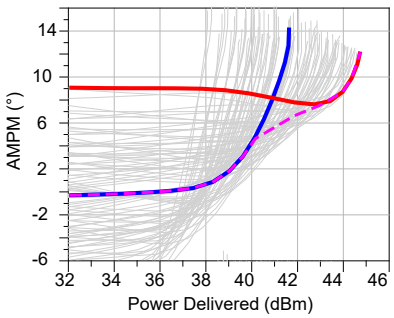

Gain (dB)
Power Delivered (dBm)


Drain Efficiency (%)
Power Delivered (dBm)


AMPM (°)
Power Delivered (dBm)


Gain (dB)
Power Delivered (dBm)


Drain Efficiency (%)
Power Delivered (dBm)


AMPM (°)
Power Delivered (dBm)

direction.

- The control amplifier is biased under the threshold voltage (class C). The gate voltage is chosen in order to turn on the transistor at the right moment.

The relative phase is chosen as a trade-off between maximum efficiency and flat AM-PM. Figure 4.16 presents the drain efficiency, gain and AM-PM for the three designs, reaching in the same conclusions as previously. On figure 4.17, we can see the resulting load trajectory for each case. This figure explains the lower output power : all three trajectories change direction when the transistors approach compression, resulting in lower peak power. This effect is due to the AM-PM distortion of all three transistors (including the control PA), which changes the relative phase relationships as the PAs compress. It was also observed in [57].

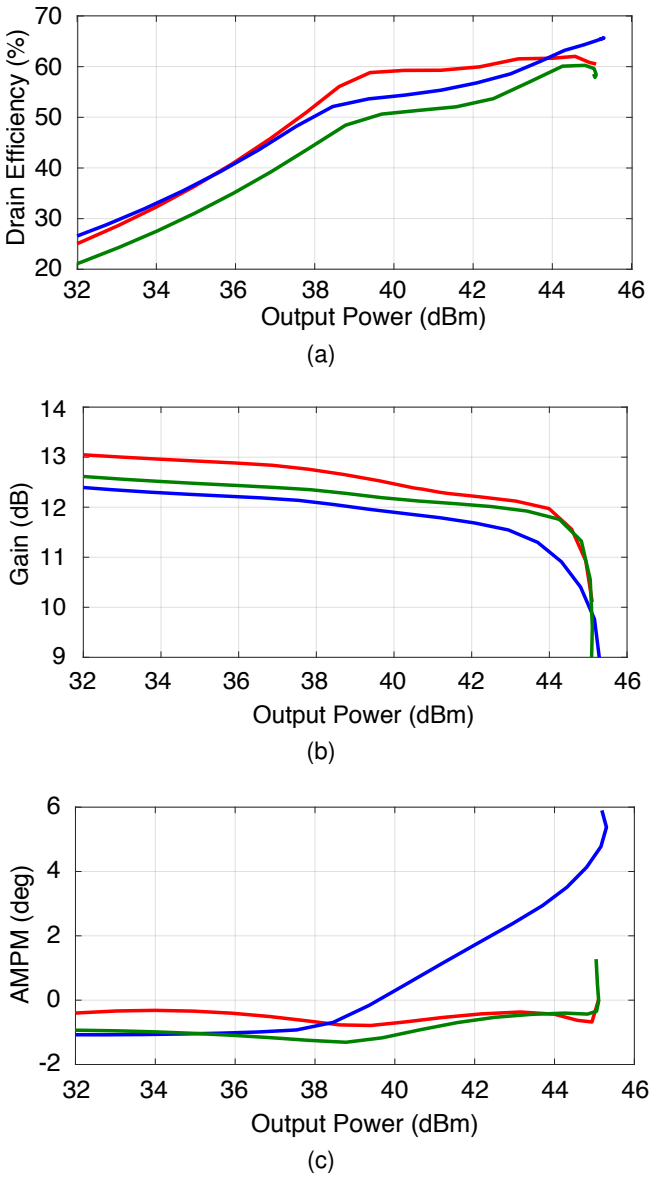


Figure 4.16: Simulated performance for the class J (in red), B (in green) and J* (in blue) LMBA. (a) – Drain Efficiency, (b) – gain and (c) – Phase distortion versus output power.

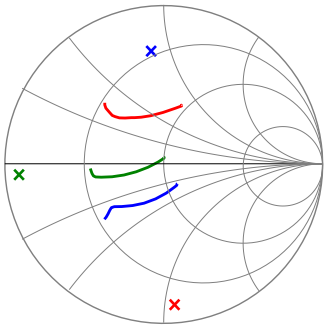


Figure 4.17: Simulated load trajectories for the class J (in red), B (in green) and J* (in blue) LMBA. Crosses represent the corresponding second harmonic termination.

CW Measurements

The experimental test setup is shown in Fig. 4.18. For CW testing, two synchronized Rhode & Schwarz SMW200A signal generators are used to generate the main and control input signals. A Rohde & Schwarz FSW40 Signal Analyzer is used to record the output. In order to measure phase distortion, the signal generators are configured in fixed phase I/Q mode, with $I = 1$ and $Q = 0$, resulting in a pure CW excitation. The I/Q data received by the signal analyzer was captured for each power level. Thus, by sweeping the input power the overall AM-AM and AM-PM characteristics are recorded.

The testing procedure has two steps. In an initial characterization, the control amplifier is turned off, and the performance of the balanced amplifier without load modulation is recorded. The drain voltage of the balanced amplifier is set at 24V, and the gate bias adapted to achieve 60 mA quiescent current for each branch amplifier. In the second step, the relative phase and amplitude of the control PA's input is swept for each main PA input power level. This produces effectively a load-pull of the balanced amplifier and we can determine the optimal impedance presented for peak output power.

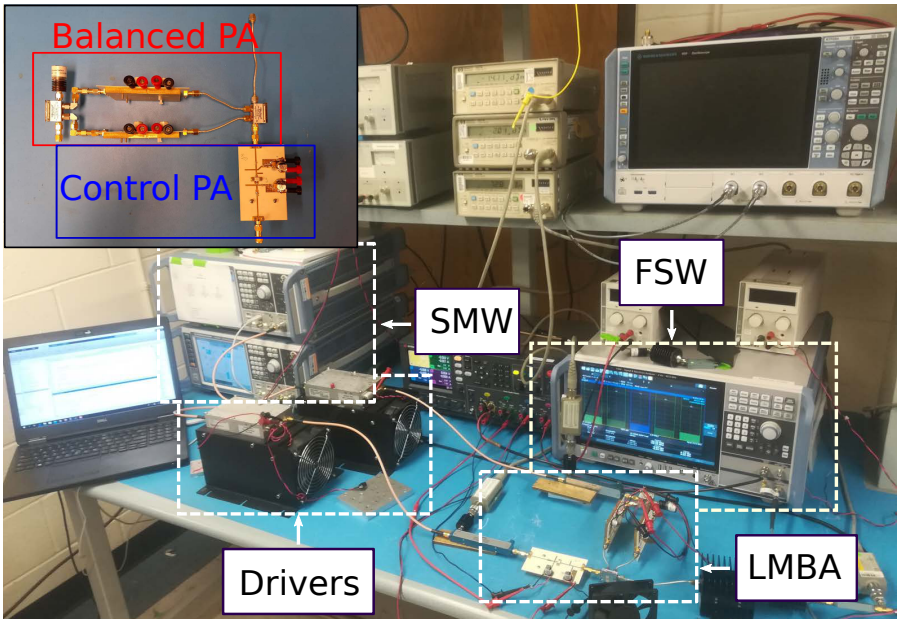


Figure 4.18: Photograph of the experimental test setup, with inset showing detail of LMBA under test.

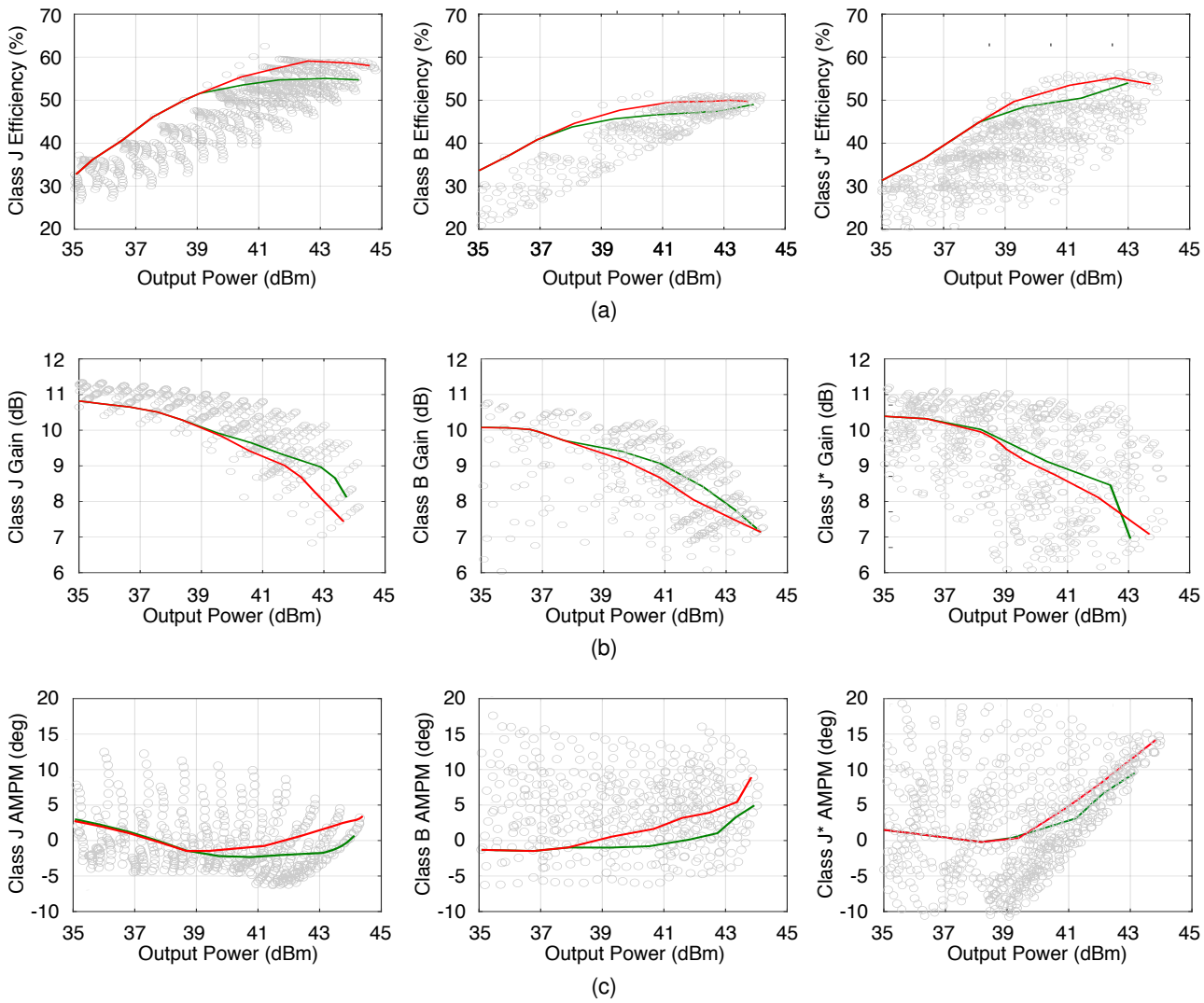


Figure 4.19: Measured performance under CW stimulus of the class J, B and J* LMBA, from left to right. (a) – drain efficiency, (b) – gain and (c) – phase distortion versus output power. The highlighted red curves present a high efficiency trajectory, the green curves present a linear-efficient trajectory.

Table 4.2: Measured results for each amplifier and load trajectory with modulated signals.

	Class J		Class B		Class J*	
Phase Offset (°)	170	190	120	140	90	110
DE (%)	40.5	44	33	36	38	40
Gain (dB)	10.6	10.3	9.8	9.6	10	9.9
ACLR (dBc)	-40.5	-33	-38.5	-31	-33	-31

During this test the control amplifier is biased in class B, with 28V drain voltage and a quiescent current of 60 mA. The result of these measurements is the cloud of points seen in Fig. 4.19.

Two trajectories are selected, corresponding to different fixed phase offsets between in the main and control PA input signals: one for maximum efficiency (in red) and the second representing a linearity-efficiency compromise. For each case the two trajectories have 20° of phase difference. As expected, the class J amplifier once again presents the best compromise, achieving higher efficiency than the other cases with a particularly flat AM-PM. Note that all measurements — efficiency, gain and output phase — include the effects and power consumption of both the balanced and control PAs.

Modulated Measurements

Modulated measurements are next performed and the two relative phase offset settings for efficiency and linear-efficient compromise are compared for each class of operation. The control PA is biased in class C, and the two input signals have the same amplitude. The testing signal is an 8.6 dB PAPR LTE signal with 10-MHz bandwidth. The two signal generators' basebands are synchronized and time-aligned with an external oscilloscope. For a flatter dynamic gain response, the gate bias of the main device is lowered, to 30 mA of quiescent current for each branch amplifier. Table 4.2 summarizes the measurement results for all cases. We note that the 0.75-dB insertion loss of the output coupler degrades the overall LMBA performance. Assuming an approximately 0.5-dB improvement with a microstrip design, we estimate the back-off and maximum efficiency would improve by 5 percentage points. The best case is identified as the class-J amplifier, with a fixed relative phase offset of 170 degrees. This configuration achieves -40.5 dBc ACLR with 40.5$\%$ drain efficiency at 35.2 dBm average output power.

Figure 4.20 presents the dynamic AM-AM (on the left) and AM-PM (on the right) characteristics for the class J, B and J* LMBA in red, green and blue respectively, for the linear-efficient phase offset found previously. Figure 4.21 shows the corresponding spectrum, with the same color code. We can compare the dynamic AM-AM/AM-PM cloud of points with the green curve of the static measurements of figure 4.19. While the AM-PM follows a similar trend in the static and dynamic measurements, the AM-AM is different. The expected 1.5 to 2 dB of gain compression from figure 4.19 is not present when using a modulated signal. This was already observed in [56] and was traced back to technological memory effects of GaN transistors, such as trapping and device heating. It is a general result, as sweat spots on the gate bias can usually be found that result in linear operation under dynamic measurements [11]. We can conclude from this measurements the great importance of the phase distortion in the linearity of a power amplifier. Indeed, while all three cases have similar AM-AM response, they present a different AM-PM, resulting in very different ACLR.

The pseudo-RF input class-J LMBA was linearized using a memory polynomial of 4th order and a memory depth of 2 samples. The resulting system achieved at 35 dBm average output power, -48 dBc ACLR with 39.8$\%$ drain efficiency, 44.8$\%$ when deembedding the coupler's losses. Figure 4.22 shows the unlinearized spectrums measured with the class-J LMBA for a phase offset of 170° (in green) and 190° (in red), and in the linearized spectrum for a phase offset of 170° (in blue).

Table 4.3 shows a comparison summary of the LMBAs presented in this work and state-of-the-art GaN PAs with similar operating frequency and power level. Compared to the other presented RF-input LMBA works, the class-J pseudo RF-input LMBA presented here demonstrates 13-15 dB better ACLR before DPD, operating with similar performance to a dual-input LMBA with reduced signal complexity.

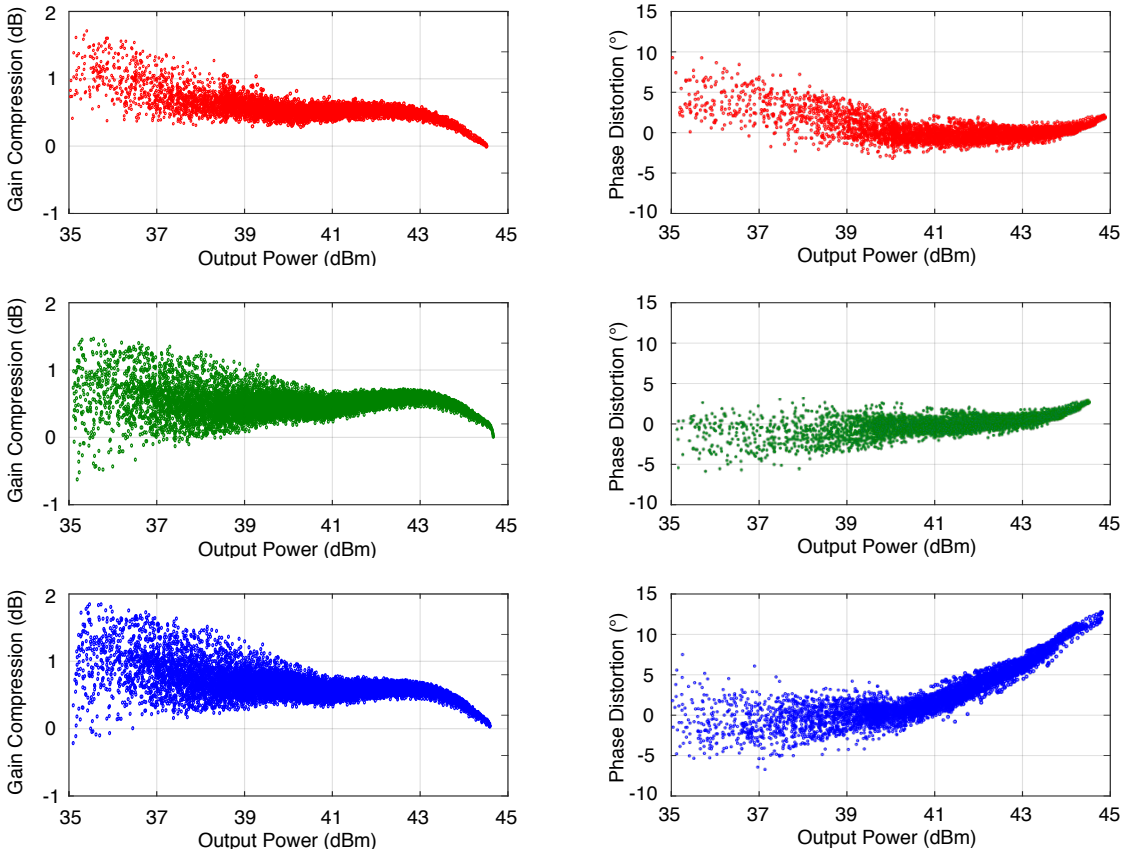
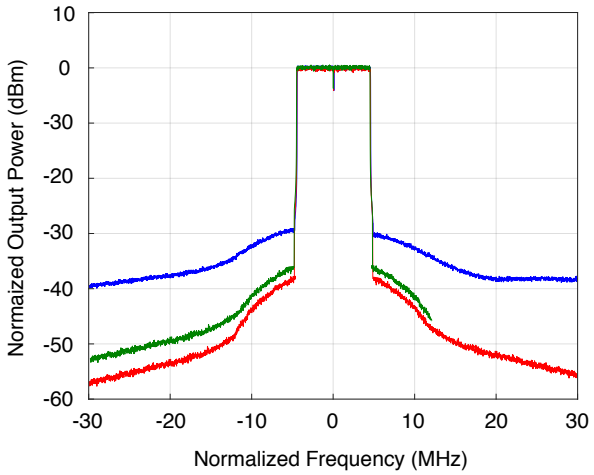


Figure 4.20: Dynamic measurements of gain compression (on the left) and Phase distortion (on the right) with a 10 MHz, 8.7 dB PAPR LTE signal for the classes J, B and J* Doherty-like LMBA, from top to bottom.



(a)

Figure 4.21: Spectrum of the class J, B and J* Doherty-like LMBA in red, green and blue respectively, with a 10 MHz, 8.7 dB PAPR LTE signal.

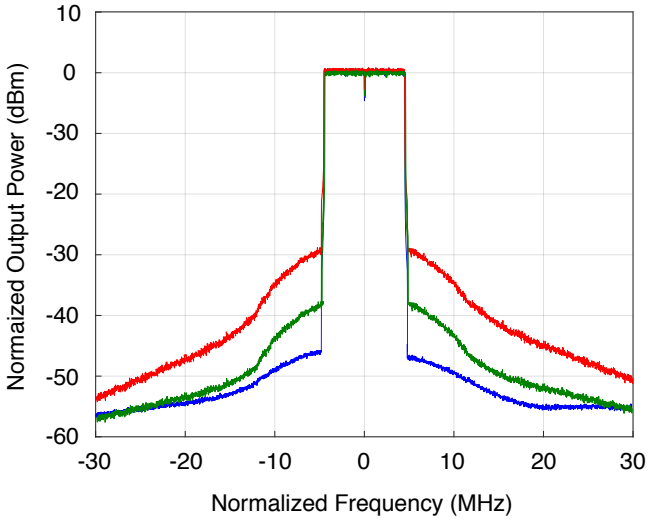


Figure 4.22: In red and blue, spectrum of the unlinearized Class J LMBA with a fixed phase offset of 190° (in red) and 170° (in green). In blue the spectrum with a 170° phase offset after applying DPD

Table 4.3: Comparison of modulated measurements to state-of-the-art GaN load-modulated power amplifiers.

Ref.	Arch.	Freq. (GHz)	BW (MHz)[1]	PAPR (dB)	Avg Pwr (dBm)	DE (%)	ACLR (dB
[42]	DPA	2.14	10	8.6	35.5	44	-40.8/-47.9
[65]	DPA	0.8	20	7.1	33	33.2	-42.5
[66]	DPA	2.3	10	7.2	35.3-33.7	45.5	-35.6
[67]	DPA	3.5	10	8.4	34.5	42.4	-37
[68]	DPA	5	40	7.4	32	42	-43.8 / -51.
[56]	LMBA	1.7-2.5	5	9	39.4-40	43-46	-39 / -53[2]
[59]	LMBA	3.05-3.55	40	9	35.5	63.2	-25 / -46.7
[55]	LMBA	1.8-3.8	3.84	9	31 - 32	17 - 26	-26 / -30
[57]	LMBA	2.4	10	7.5	38	47	-27
	Class-J LMBA	2.4	10	8.6	35.5	40.5 / 39.8[2]	-40.5 / -48
This Work	Class-B LMBA	2.4	10	8.6	35.5	33	-48.5
	Class-J* LMBA	2.4	10	8.6	35.5	38	-33

[1] Instantaneous signal bandwidth
[2] Including DPD

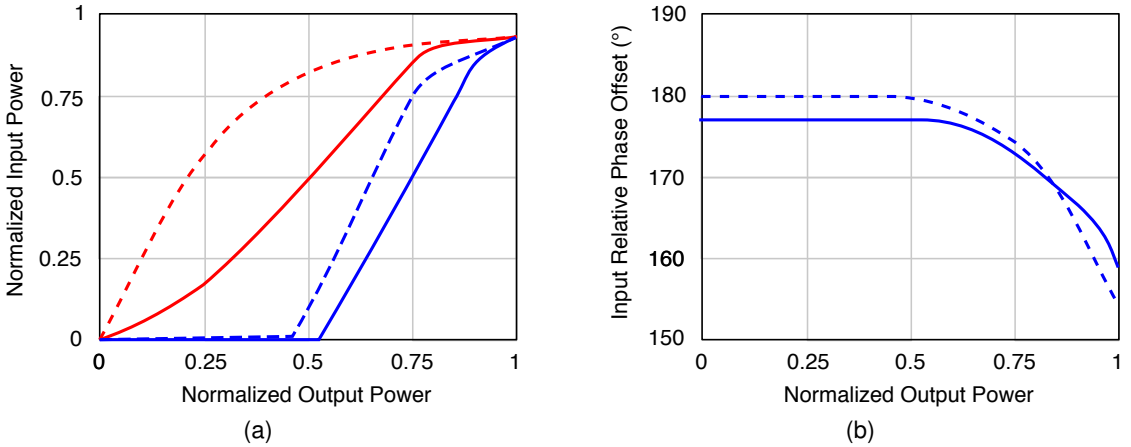


Figure 4.23: Shaping functions for the Dual-Input Class J Doherty-like LMBA. On the left the amplitude of the normalized input versus the normalized output for the balanced (in red) and control (in blue) amplifiers for a higher linearity (solid line) and higher efficiency (dotted line) shaping. On the right the input relative phase offset versus the normalized output power for a higher linearity (solid line) and higher efficiency (dotted line) shaping.

Dual-Input Investigation

The modulated measurements presented so far assumed a pseudo single RF input configuration. Exploiting the dual-input configuration of the designed LMBAs can push even further the linearity/efficiency compromise. In this case the control amplifier is biased above threshold and specific shaping functions are applied to the input signals of the balanced and control amplifiers. In our case we have three shaping functions : two amplitude functions that modify the amplitude of the inputs of the balanced and control amplifier and one phase function that modifies the phase of the input of the control amplifier. These shaping functions can be determined from the static measurements of figure 4.19, tracking either maximum efficiency, flat AM-AM or flat AM-PM versus output power, or a compromise of them. They were generated through matlab, using the convex hull function on the static data.

Two different shaping objectives were investigated, one to reach higher efficiency with the same linearity and an other to reach higher linearity for the same efficiency. Figure 4.23–a presents the amplitude shaping functions of the higher linearity (in solid line) and higher efficiency (in dotted line) for the input signal of the balanced amplifier (in red) and the control amplifier (in blue) versus the normalized output power. Figure 4.23–b shows the relative phase difference between the two inputs for the higher efficiency and higher linearity scenarios, versus the normalized output power. The shaping functions were applied to the modulated LTE signal used previously with the following procedure: the amplitude of the modulated signal is squared and normalized by its maximum amplitude, in order to transform it from an IQ voltage waveform to a normalized power waveform. The amplitude shaping functions are then applied to this signal in order to extract the balanced and control's amplifier inputs' amplitude. The phase of the balanced amplifier's input is identical to that of the original signal, while the phase of the control amplifier's input is the sum of the original phase and the phase given from the shaping function. The higher linearity shaping functions resulted in a 3.3 dB lower ACLR for the same efficiency, while the higher efficiency resulted in 3 more percentage points of DE for the same ACLR.

The concept of shaping the signals at each input of the LMBA is somewhat similar to that of Digital Predistortion. Indeed, the two inputs are predistorted in order to reach higher efficiency or higher linearity. we could in theory use the dual-input to achieve much higher linearity, in the

order of -50 dBc ACLR. The shaping functions however were deduced from static measurements. We saw previously that this approach fails to adequately catch the characteristics of the amplifier under modulated stimulation. In [69], the authors proposed an Adaptive Signal Separation algorithm (ASSA) that optimizes the static shaping functions on the go from modulated measurements, similar to adaptive DPD. More generally, digitally assisted dual-input amplifiers are a very interesting field of research, and new dual-input DPD algorithms are very promising for very high efficiency, high linearity and large bandwidth systems[70].

4.4 Design of a 28 GHz LMBA in GaAs 0.10um technology

So far in this chapter we have applied the design methodology presented previously on a GaN based power amplifier at 2.4 GHz. This technology – at this frequency– clearly favours a class J like load modulation, both in terms of efficiency and linearity. It is interesting to test the validity of these results in different scenarios, such as higher frequency or different technology.

5G NR includes whole new bands in the millimeter waves. Among others, the 28GHz band is particularly interesting for low power massive MIMO applications. These frequencies are often associated with poor efficiency, as conventional power amplifiers often present less than 20% PAE at 6 dB back-off. In order to test the theory presented above at higher frequencies and with other technologies, a dual-input Doherty-like Millimeter-wave Integrated Circuit (MMIC) 30 dBm LMBA is designed in GaAs 0.10 um technology from Win Semiconductor. The dual-input configuration was chosen in order to keep an extra degree of freedom during the measurement.

Evaluation of the device

Win Semiconductor develops a PHEMT device on a GaAs substrate with 10μm gate length. The PIH-10 technology provides a 4 V 30 dBm GaAs pseudo-morphic High Electron Mobility Transistor and incorporates thick metal layers for low loss–high quality factor passive components. The f_T is around 100 GHz, allowing the use of this transistor in the millimeter waves. The technology provides a power density of 1.4 W per millimeter. In order to design a 30 dBm LMBA, we start with a branch amplifier of 0.75 mm gate width with 10 fingers of 0.075mm width each.

Following the load-pull based methodology presented above, the design of a linear and efficient LMBA can be operated in two steps :

- The first step consists in finding the optimal load trajectory that minimizes the overall phase distortion.
- The second step is to choose the corresponding second harmonic termination that maximizes the efficiency of this load trajectory.

Harmonic tuning of power amplifiers becomes complicated as the fundamental frequency increases. At 28GHz, the second harmonic is at 56 GHz, which is rather close to the f_T. We can assess the harmonic tuning capacity of the technology from harmonic load pull measurements.

The first step of the technology assessment is the identification of the parasitic drain – source capacitor C_{ds}. In MMIC design, the output parasitics are almost negligible, and the output stage of a transistor can be directly modeled as an ideal current source with a shunt capacitor C_{ds}. The value of C_{ds} can be obtained directly from S-Parameter measurements or simulations. For this test, the input and output of the transistor was loaded with 50Ω. The transistor was biased in deep class AB, with a quiescent current of 10 mA. Figure 4.24 presents on the Smith chart the resulting S_{11} (in blue) and S_{22} (in red). At 28 Ghz $S_{2,2} = 0.7e^{-j162*\pi/180}$. The corresponding admittance can be expressed

as $Y = G_p + jC_{ds}\omega$, resulting in $C_{ds} = 0.33pF$. G_p is the output conductance of the transistor, related to the ideal current source.

Now that the C_{ds} has been estimated, we can de-embed it to continue our analysis at the intrinsic drain plane. The de-embeding can be operated on the circuit, adding two extra shunted capacitors of value $\pm C_{ds}$, as in figure 4.25. The current in-between the capacitors is the same as that on the intrinsic drain plane.

We can now do the harmonic load-pull simulation and look at the resulting impedance presented at the intrinsic drain plane. Considering a 30 dBm LMBA and 6 dB back-off, we want high efficiency from the balanced PA at 24 dBm, or 21 dBm per branch amplifier. Accounting for the various loss, we can aim for $\mathrm{P_{BO}} = 22\ \mathrm{dBm}$ back-off power. Considering a drain voltage of 4V, the corresponding class B optimal resistance can be found to be :

$$R_{opt} = \frac{V^2}{2P_{\mathrm{BO}}} \approx 50\Omega \tag{4.1}$$

The test bench is based on ADS integrated harmonic load-pull bench. The output fundamental impedance is set to $Z_L = 5 - j15$, equivalent to a 50Ω resistance in parallel with a capacitance of value $-C_{ds}$, in order to cancel out the C_{ds} and present at the intrinsic drain plane R_{opt}. The third harmonic is left at 50Ω, as it has practically no effect at these frequencies. The input impedance is conjugately matched to the transistor's gate, loaded on the drain side with Z_L, and with all the harmonics shunted. The output second harmonic is set at $Z_{H2} = 0.95e^{j\phi}$, where ϕ is swept with 15° from 0° to 345°. Figure 4.26 shows in red dots the presented second harmonic termination and in green circles the corresponding second harmonic impedance seen at the de-embeded intrinsic drain plane. It is striking to see on the Smith chart how the circle has closed around the value of C_{ds}. Even if an appropriate output impedance is chosen that cancels the C_{ds}, the resulting quality factor is too small and the second harmonic becomes strongly resistive. We conclude that at this frequency with this technology, second harmonic tuning is very limited. For practical reasons, the second harmonic will thus be left at 50Ω, in order to simplify the design of the Output Matching Network (OMN) and decrease the insertion loss.

Now that we know that the second harmonic termination has very little effect on the transistor's performance, we can do a fundamental load-pull simulation in order to look for the optimal load trajectory. The same configuration as for the harmonic load-pull is used, but this time the second harmonic is set to 50Ω and the fundamental impedance is swept around Z_L. The input power was also swept, from 5 to 17 dBm.

Figure 4.27 presents the results of the load-pull measurement on the Smith chart at the intrinsic drain plane on the left and at the physical drain access on the right. The red dotted lines represent the

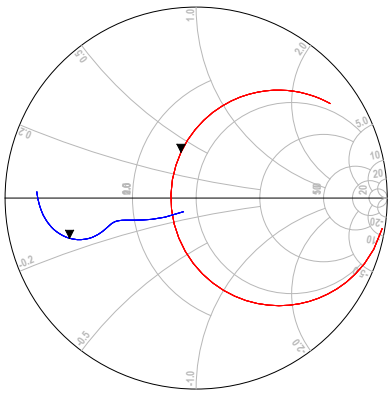


Figure 4.24: S11 (in blue) and S22 (in red) simulations of the transistor.

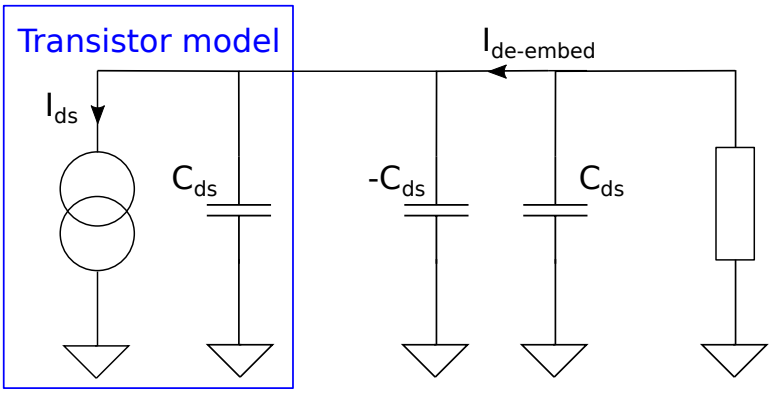


Figure 4.25: De-embeding of the transistor's C_{ds} parasitic capacitance.

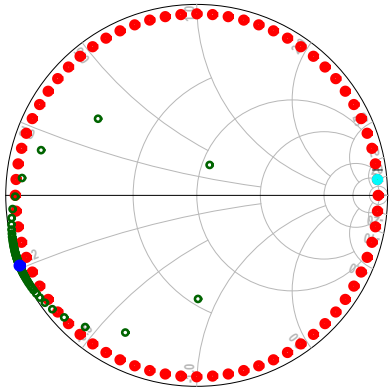
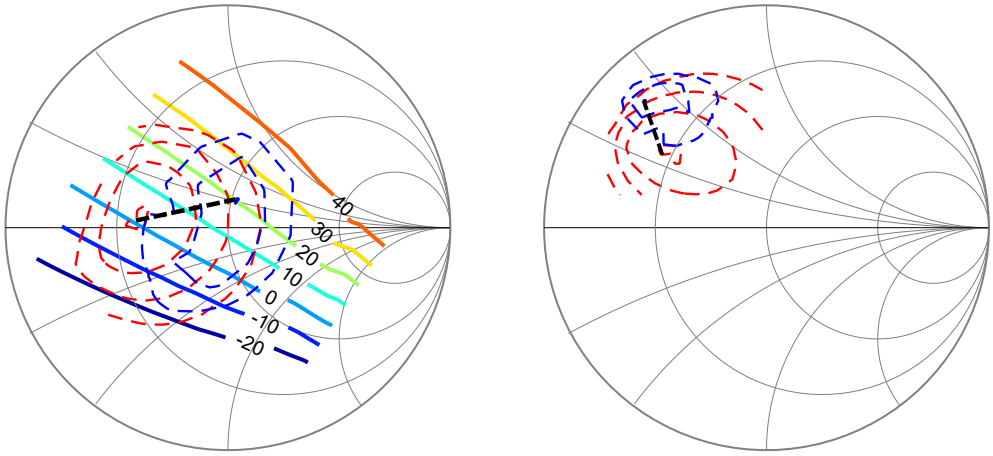


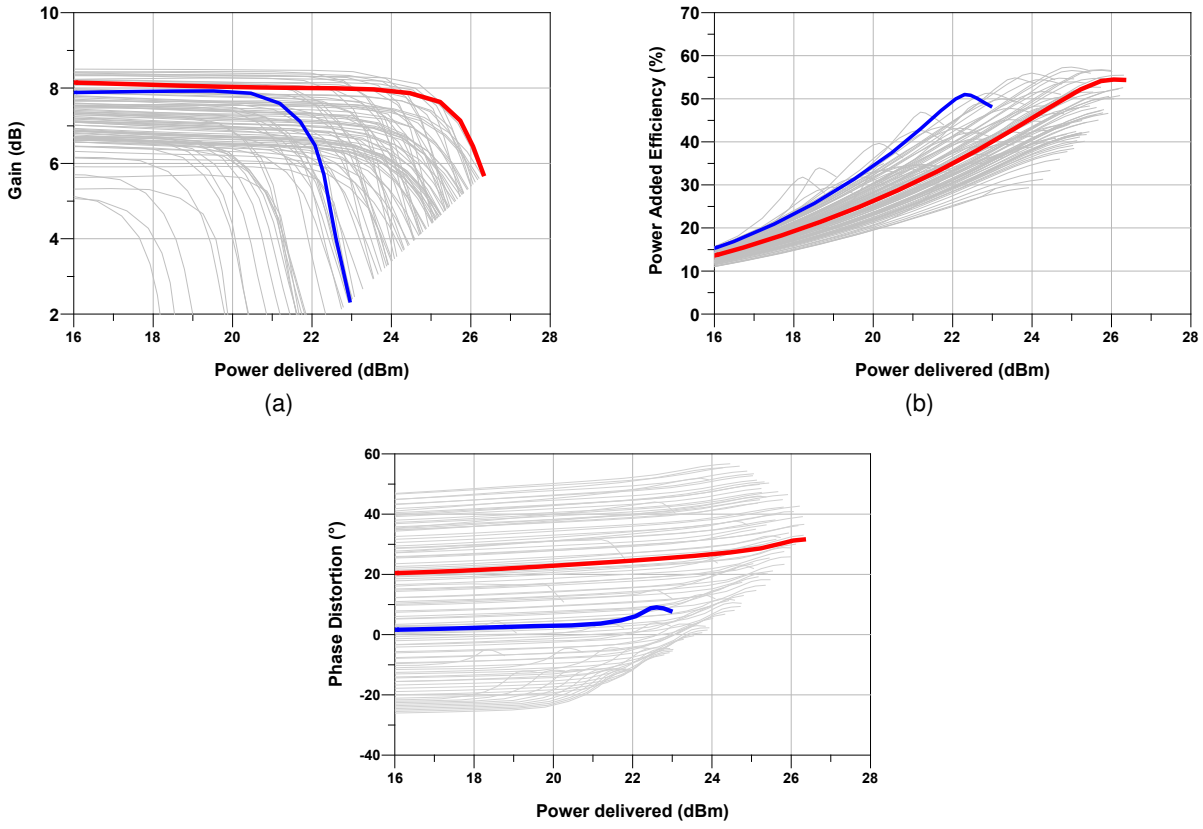
Figure 4.26: Harmonic load-pull simulation results. In red the second harmonic impedances presented at the transistor's physical drain access. In green the corresponding impedance seen at the de-embeded intrinsic drain plane. The impedance highlighted by the cyan dot at the physical drain access is transformed into the impedance highlighted by the blue dot at the de-embeded intrinsic drain plane.

maximum output power contours, the blue dotted lines the maximum PAE contours at a fixed output power of 22 dBm and the coloured lines the estimated overall AM-PM contours of the corresponding LMBA at the same fixed output power of 22 dBm. The AM-PM contours take into account both the variation of the phase of the intrinsic drain current and the load trajectory, as seen in the previous chapter. The black dotted line represents the load trajectory that maximizes efficiency throughout the load modulation. Figure 4.28 shows the results at the physical drain access versus the output power. We have highlighted in red and in blue the curves corresponding to the impedance that results in maximum output power and in maximum efficiency at 22 dBm. Looking at figure 4.27–a, we can see that following this trajectory results in 20° of phase distortion. We can see a similar trend in figure 4.28–c We understand that since we cannot use the second harmonic termination as a degree of freedom, we cannot minimize the phase distortion. The resulting LMBA will thus present high AM-PM and will not be linear. Nevertheless, we can use this data to choose our back-off and maximum impedance. Table 4.4 summarizes the LMBA parameters chosen from the load-pull data, based on the methodology presented in the previous section. The BO and M subscripts correspond to the back-off and peak power values, and P_m, P_c, and P represent the power of each branch PA, the control PA and the overall output power respectively.



(a) (b)

Figure 4.27: Fundamental load pull results, on the left at the de-embeded intrinsic drain plane and on the right at the physical drain access. In red maximum power contours, in blue maximum PAE at a fixed output power of 22 dBm and in coloured lines the estimated overall AM-PM of the corresponding LMBA at a fixed output power of 22 dBm. The black dotted line is the load trajectory that maximizes PAE.



(a) (b) (c)

Figure 4.28: Fundamental load-pull results versus output power. In a) the gain, in b) the PAE and in c) the estimated overall AM-PM of the corresponding LMBA. In red and blue the curves corresponding to the peak output power and maximum back-off efficiency respectivelly.

Table 4.4: Design specifications and simulation results for the Doherty-like LMBA.

Z_{BO}	Z_{M}	$P_{m_{\mathrm{BO}}}$	$P_{m_{\mathrm{M}}}$	P_{c}	P_{BO}	P_{M}
7+j16	10+j6.5	21 dBm	28 dBm	27 dBm	24 dBm	30.5 dBm

Realization of the Doherty-like 30 dBm LMBA at 28 GHz

While we know that we cannot use this device at this frequency to design a linear LMBA, we can still make a high back-off efficiency power amplifier. The design specifications and simulation results can be found on table 4.5. Since there was extra space on the reticle for this MMIC run, three power amplifiers were designed :

- A 24 dBm Balanced Amplifier
- A 27 dBm Single-Ended amplifier
- A 30 dBm dual-input LMBA, using the balanced amplifier as a main amplifier and the single-ended as a control amplifier.

The layout of the resulting LMBA can be seen on figure 4.29. The other two amplifiers can be found in the appendix. In order to have enough gain, every amplifier is composed of two stages, with a driver and power transistor. All the power transistors are 0.75 mm large (10x0.075mm) and the drivers are 0.45 mm large (6x0.075mm). Figure 4.30 and 4.31 presents some EM simulation results of the LMBA. The S parameters and other results of the other designs can also be found in the appendix.

The input and output hybrid couplers are based on Lange couplers, but are different. The input coupler is designed on a single metal layer, in order to pass the gate bias lines underneath. The width of the fingers is 8μm and their spacing is 4μm. The output coupler is using both metal layer, in order to decrease loss, with a metal width of 8μm and spacing of 11μm. The two couplers can be seen on figure 4.32 and 4.33. Under the layouts we can also see the amplitude (on the left) and phase (on the right) imbalance.

Table 4.5: Design specifications and simulation results for the Doherty-like LMBA.

Parameter	Design Goal	Simulation Result
Frequency (GHz)	27 - 29	27.5 - 28.5
Maximum Input Power (dBm)	$<$ 20	$<$ 16 for each input
Maximum Output Power (dBm)	30	29.5
Maximum PAE ($\%$)	40	37
6 dB Back-off PAE ($\%$)	35	32
Input Return Loass (dB)	$<$ -10	$<$ -15

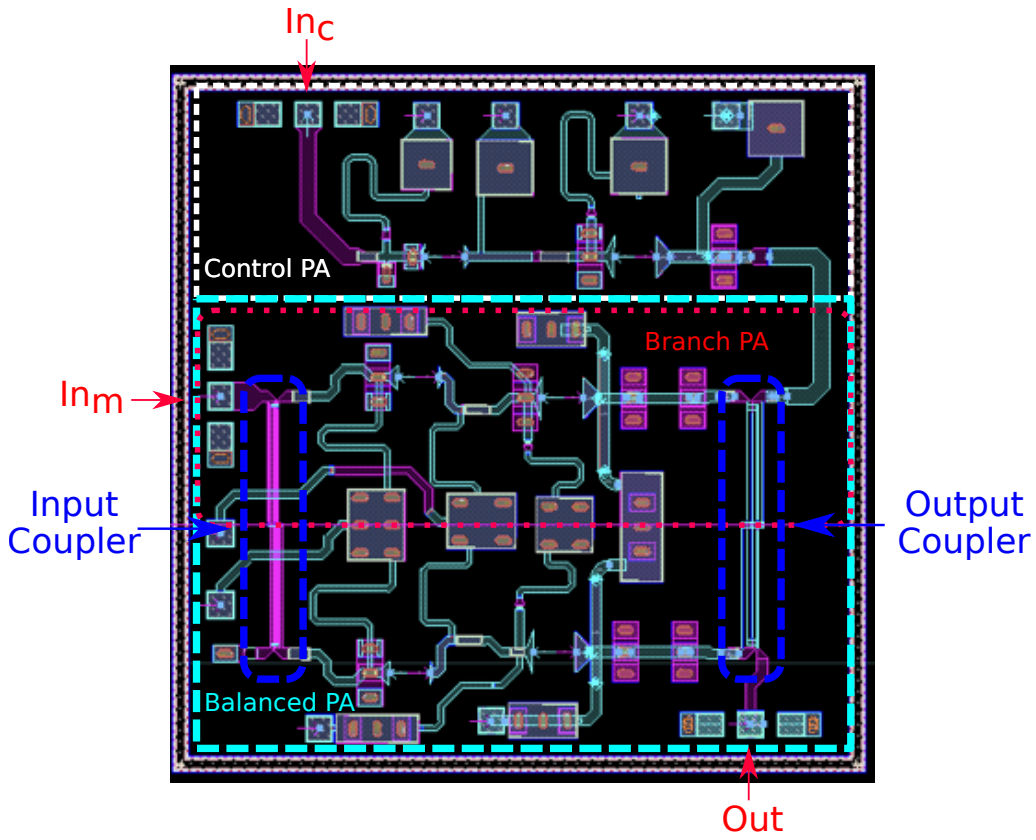
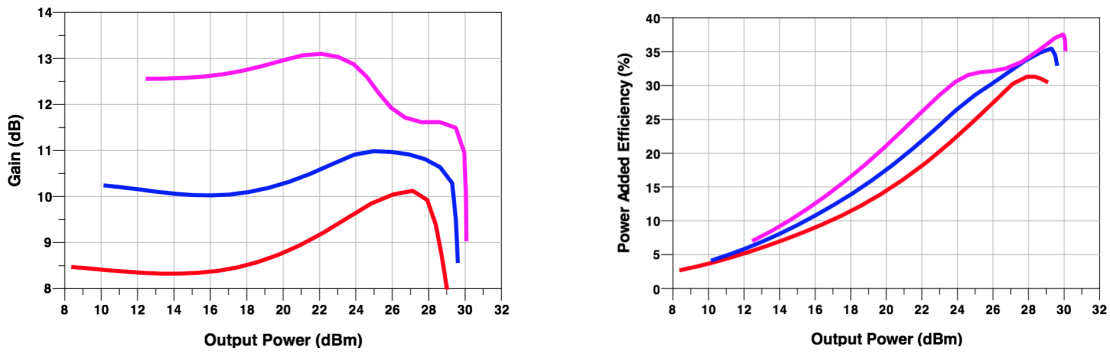


Figure 4.29: Layout of the GaAs Load Modulated Balanced Amplifier



(a) (b)

Figure 4.30: Gain (on the left) and PAE (on the right) versus Output Power of the Doherty-like LMBA at 27 GHz (in blue) 28 GHz (in pink) and 29 GHz (in red)

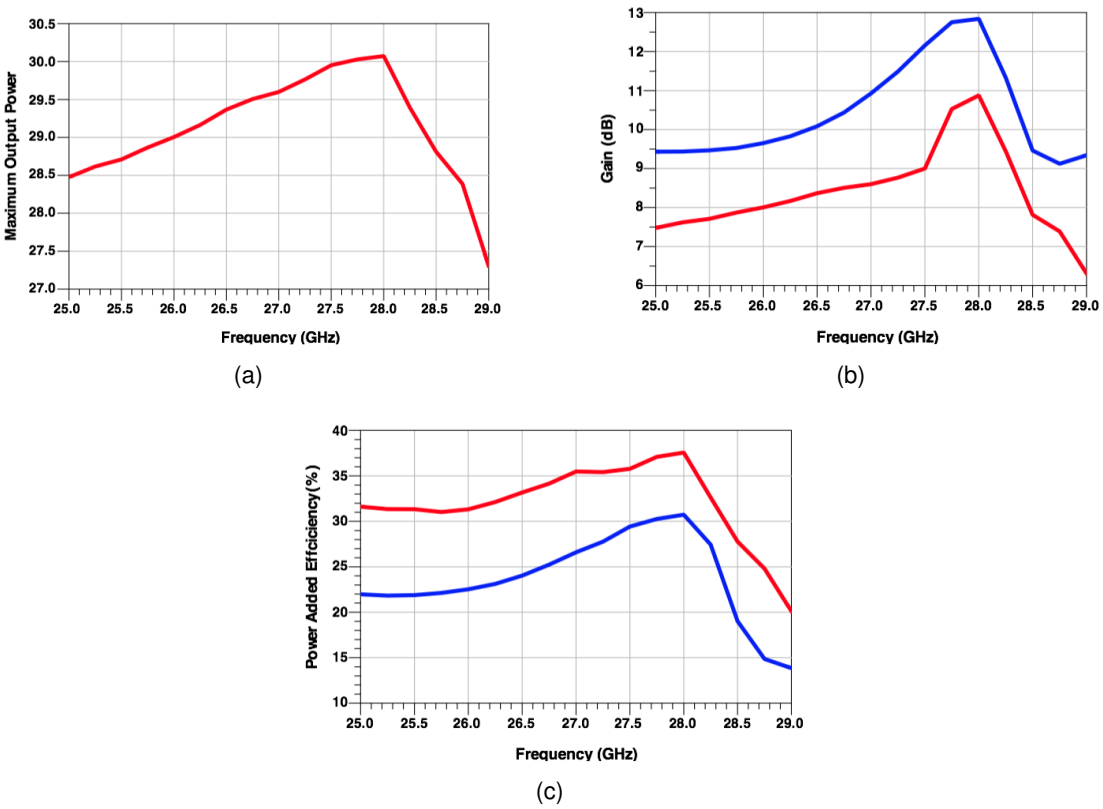


Figure 4.31: a– Maximum output power, b– Gain and c– PAE versus frequency of the Doherty-like LMBA. In red at peak power, in blue at 6 dB back-off.

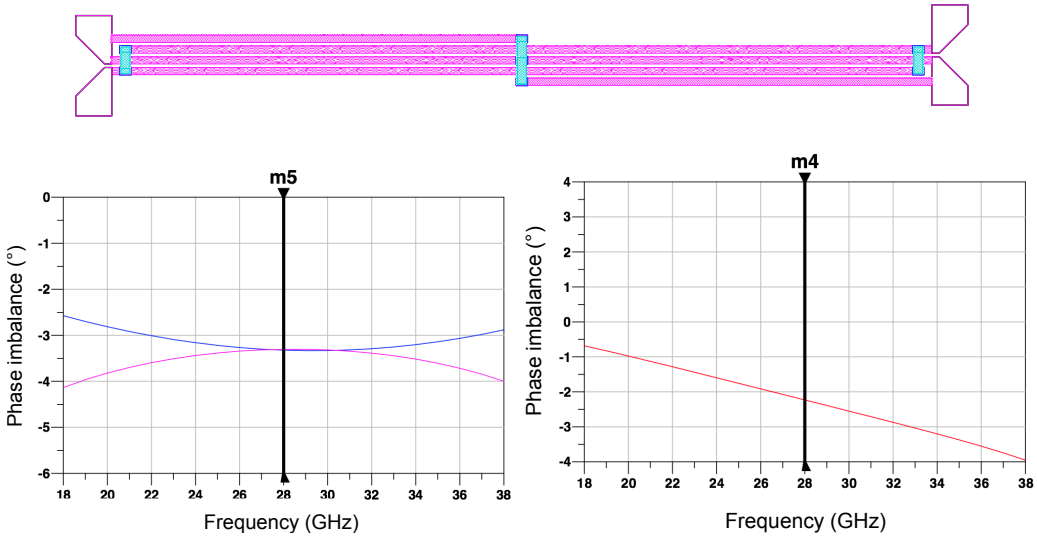


Figure 4.32: On the top layout of the input lange coupler. On the bottom EM results of the input Lange coupler. On the left amplitude imbalance, on the right phase imbalance.

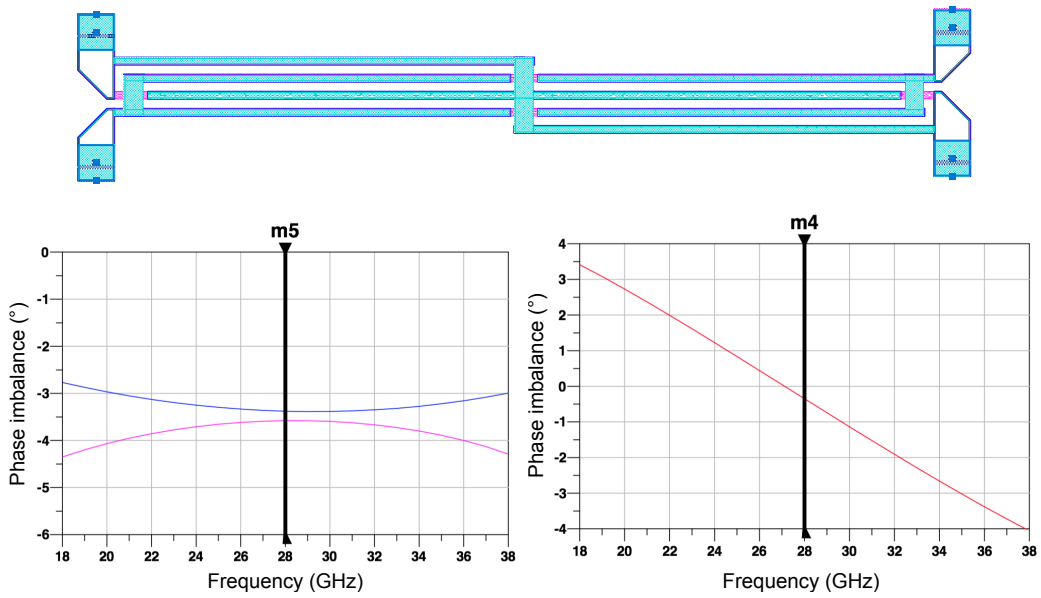


Figure 4.33: On the top layout of the output lange coupler. On the bottom EM results of the output Lange coupler. On the left amplitude imbalance, on the right phase imbalance.

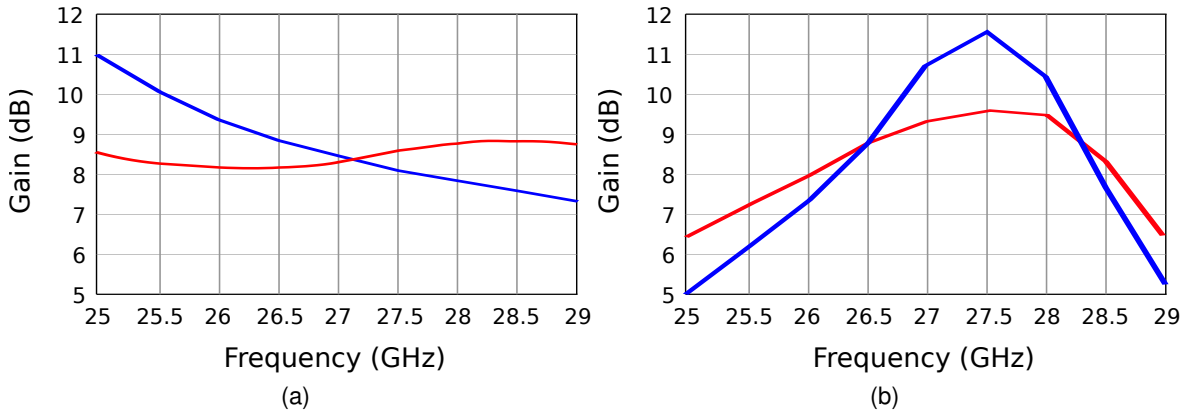


Figure 4.34: Gain of the branch amplifier

Looking at table 4.5, we see that the resulting bandwidth of the LMBA is very narrow compared to the original goal. This can be understood by looking at figure 4.34. We can see the gain of a branch amplifier without the driver stage (on the left) and with the driver stage (on the right). The impedance presented at the drain of the power stage is varied : the blue lines correspond to a peak-power impedance ($Z_L = 10 + j6.5$) and the red lines to a back-off impedance ($Z_L = 7 + j16$). We clearly see that while adding the driver results in 3 dB higher gain at the center frequency, it is much more narrow. The driver stage is very narrowband, especially with the peak-power impedance. The reason behind this is the variation of the gate impedance of the power stage during the load modulation : in order to absorb this variation, the Intermediate Matching Network (IntMN) resulted in a narrowband operation. A potential solution to this issue is to exploit the balanced architecture. Indeed, balanced PAs present very low S_{11}. Having a single-ended driver stage feeding a balanced power stage would result in higher bandwidth.

The designed amplifier is the first LMBA operating in the millimeter-wave bands. It achieved at the center frequency 30% PAE at 6 dB back-off. The bandwidth is particularly narrow for this high

Table 4.6: Comparison of the simulated performance of the GaAs Doherty-like LMBA to the state-of-the-art millimeter-wave high efficiency amplifiers.

Ref.	Tech.	Freq. (GHz)	BW (GHz)	Peak Pwr (dBm)	$\mathrm{PAE}_{\max}(\%)$	PAE @ 6BO($\%$)	Gain (d
[71]	GaN	28.5	1	35.6	22-28	17 - 23	10
[72]	GaAs	25.8	0.5	25.1	16.5	12.6	7
[73]	GaAs	31.1	2.8	26.3	35	28	14
[74]	GaAs	28.5	2.5	27.5	37-39	25-29	18-20
[75]	GaN	28	2	39	26 - 31	21 - 24	30
This work	GaAs	28	1	30	36	30	13

frequency, but a solution for a wider band design has been identified. We notice that the hybrid couplers can operate correctly from 23 GHz to 34 Ghz, and thus the limiting factor here is only the matching networks. Wideband design should be fairly easily obtained, at the cost of slightly less efficiency. Table 4.6 compares the resulting design to the state-of-the-arts millimeter-wave high efficiency amplifiers. We see that apart from the bandwidth, the simulated results are at the state-of-the-art. In particular the PAE at back-off outperforms that observed in the literature. This is very encouraging, as a solution for a wider bandwidth operation has already been identified.

4.5 Conclusion

In this chapter the impact of the class of the branch amplifier of an LMBA on the AM-AM / AM-PM distortion is studied. Three LMBAs based on class J, B and J* power amplifiers are designed and tested. The best linearity / efficiency compromised is found with the class-J LMBA, where 40.5% drain efficiency and -39.6 dBc ACLR are achieved with a 10 MHz 8.6 dB PAPR signal at 2.4 GHz. The same amplifier can achieve -48 dBc ACLR with a low processing cost digital predistortion, making it a viable option for low power base stations. The dual-input configuration shows also very promising results when higher complexity systems can be implemented.

An article will be published in the 2020 European Microwave Week conference presenting the results of the Class J LMBA and comparing an efficient and a linear-efficient load modulation. A journal paper focused on the generalized LMBA theory and the comparison of the the harmonically tuned LMBAs has also been submitted at the Transactions on Microwave Theory and Techniques, waiting for approval.

We understand from equation (3.42) that a change of reactance in the load trajectory will cancel out the AM-PM in load modulated amplifiers. The sign and magnitude of this variation depends on the profile of the phase distortion versus output impedance, which is technology dependent. Here this profile favours a class J like load modulation. This result seems to be a general case for GaN transistors, as the characteristics of this technology, such as the different parasitics' relative order of magnitude, are similar across devices. Taking into account the superior back-off performance often associated with class J second harmonic terminations, it is clearly the best option for GaN PAs. In the second part of this chapter a 30 dBm GaAs Doherty-like LMBA was designed at 28GHz. The original goal of this design was to make a linear-efficient LMBA at millimeter waves, following the methodology presented earlier. An assessment of the transistor showed that harmonic tuning has very limited effects on this technology at this frequency. We thus lack the required degree of freedom on the load trajectory to achieve linear and efficient operation.

It would be interesting to compare these results either to high frequency GaN transistors or lower

frequency GaAs pHEMTs. It is the authors' expectation that the class J load trajectory will generally bring a certain improvement regarding the phase distortion when harmonic tuning is possible.

From this work, a paper will be presented at the 2020 European Microwave Week conference in Utrecht. It is focused on the Class J LMBA, showing the design of a linear and efficient LMBA. An article presenting the generalized LMBA analysis and the resulting methodology has also been submitted for publication at the Transactions on Microwave Theory and Techniques journal.

Chapter 5

Mismatch Resilient Power Amplifier

In the previous chapters, novel architectures presenting high efficiency for large back-off power ranges were presented. The condition for these systems to operate properly is that the impedance presented at the output of the system (mainly the impedance of the antenna) is always equal to a predefined characteristic impedance Z_0, usually for telecommunication systems equal to 50Ω. When this output impedance varies, the amplifier is no longer terminated with an ideal load, resulting in sub-optimal performance. The degree of degradation depends on the importance of this impedance mismatch.

We know from microwave theory that in a transmission line, any discontinuity will produce a partial reflexion of a traveling wave. Impedance mismatch can be such a discontinuity. Considering the characteristic impedance Z_0 and the actual output impedance Z_L, the reflected wave β is found to be :

$$\beta = \alpha \frac{Z_L - Z_0}{Z_L + Z_0} \tag{5.1}$$

Where α is the forward wave. We can define a complex reflexion coefficient Γ :

$$\Gamma = \frac{\beta}{\alpha} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{5.2}$$

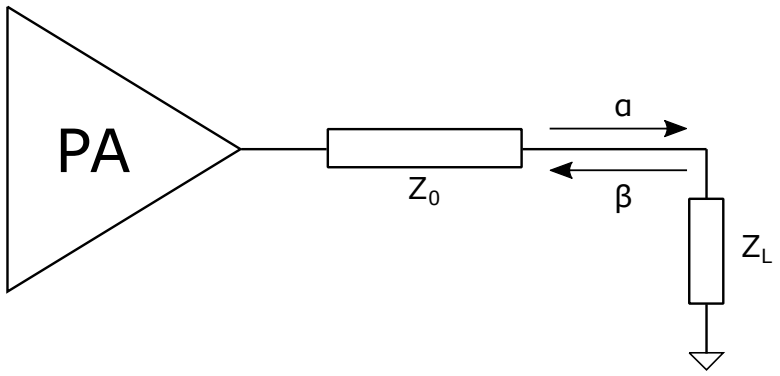


Figure 5.1: Impedance mismatch : When the output impedance Z_L is different from the predifined characteristic impedance Z_0, part of the forward wave α generated by the power amplifier will be reflected back. This reflected wave β will perturb the operation of the power amplifier and decrease its performance.

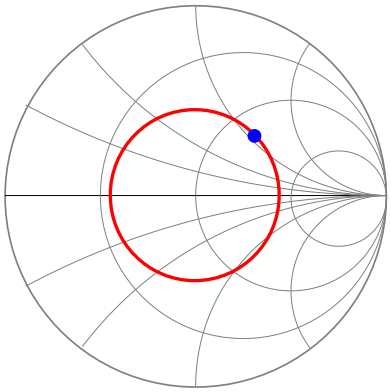


Figure 5.2: Graphic representation of impedance mismatch. The red circle represent a VSWR 2:1, equivalent to a $\Gamma = 0.33$. The blue dot corresponds to a $\Gamma = 0.33e^{j\pi/4}$, or, considering $Z_0 = 50\Omega$, an impedance $Z_L = 69.5 + j36.8\Omega$

We can also define the scalar Voltage Standing Wave Ratio (VSWR) as :

$$\mathrm{VSWR} = \frac{1 + |\Gamma|}{1 - |\Gamma|} \tag{5.3}$$

We can interpret a given impedance mismatch either as a non-optimal output load Z_L, a complex reflection coefficient Γ or a voltage standing wave ratio. We can see this graphically with a Smith Chart in figure 5.2. The red circle represents a VSWR of 2:1, or – similarly – a Γ of 0.33.The blue dot corresponds to a $\Gamma = 0.33e^{j\pi/4}$ or, considering $Z_0 = 50\Omega$, $Z_L = 69.5 + j * 36.8$.

This chapter is organised as follows : in the first section the origins and effects of impedance mismatch are explored. An overview of the main mismatch detection and cancellation methods is then presented in section 2, comparing their respective advantages and drawbacks. The Balanced Amplifier is then presented in section 3 as an alternative mismatch resilient architecture. Finally, section 4 studies the sensibility to mismatch of the Load Modulated Balanced Amplifier and presents a novel Double-balanced LMBA, that achieves high back-off efficiency under severe impedance variations.

This research was developped with SOMOS Semicondcutor, as its products, mainly CMOS PAs for handset and IoT devices are subject to great variations of output impedance. The goal of this work was to study the impact of impedance mismatch on CMOS PAs and explore solutions that retrieve the RF performance – mainly the drain efficiency.

5.1 Origins and effects of impedance mismatch on power amplifiers

In general, the RF Front-Ends of User Equipments and Base Stations are very different. Impedance mismatch has therefore different origins for each case.

Impedance Mismatch in User Equipments

U.E. Front End Modules (FEM) have to integrate in one PCB board all the different power amplifiers, filters, switches, duplexers and quadplexers necessary for all the different connection technologies provided by the UE. Figure 5.3 presents a Front-End Module (FEM) of a 2G/3G/4G cellphone based on MediaTeK Phase 5 platform (a handset RFFE manufacturer). Three linear power amplifiers – for the low (0.7–0.9 GHz), mid (1.7–2.02 GHz) and high bands (2.3–2.7 GHz)– are responsible for the 3G-4G phase and amplitude modulated signals, while a saturated power amplifier efficiently

amplifies 2G GMSK signals. The duplexers and quadplexers are responsible for Frequency Division Duplex (FDD) operation and Carrier Aggregation (CA). The Single Pole 10 Through (SP10T) switches share the –single or multiple– antenna(s) between the different paths. All these components have to be integrated in an extremely small space, and have to be cheap. We understand that in such an environment, it is very difficult to precisely control the impedance presented at the power amplifier's drain for all the frequency bands. In particular, the duplexer and quadplexer are often based on Surface Acoustic Wave (SAW) filters. Despite their very high out-of-band rejection, SAW filters are known for having a rather poor S11 throughout the operating band, resulting in impedance mismatch. In practice, 3GPP expects the power amplifier to respect the linearity requirements up to a drain VSWR of 3:1 – equivalent to a $\Gamma = 0.5$.

U.E.s are usually portable devices. As such, their environment is always changing, going from inside a pocket to the ear of a user and then sitting on a wooden or metallic table. The radiation pattern of an antenna strongly depends on the space around it. This changing environment thus impacts the emission of the output signal, often resulting in power being reflected back to the amplifier, and thus the appearance of a VSWR [76]. This second source of impedance mismatch is much more unpredictable, and can result in greater Γ. 3GPP demands for 4G power amplifiers to be able to withstand a VSWR of up to 10:1 –$|\Gamma| = 0.82$– without damage.

We therefore understand that power amplifiers in user equipments are practically never loaded with a 50Ω impedance, resulting in quasi-constant performance degradation. This issue is well known from PA designers, who have to make sure the power amplifier is fulfilling the specifications even under impedance mismatch.

Impedance Mismatch in Base Stations

Things are very different in 4G Base Stations, which have much more space for the RF Front End. On the contrary of UE Front-End Modules, base stations have a separate RFFE for each band of operation, strongly reducing the number of components after the power amplifier. Furthermore, power amplifiers are very often protected by an isolator: under impedance mismatch, the power reflected to the amplifier is redirected to an isolation resistor and radiated out of the system. The PA therefore always sees an optimal 50Ω impedance.

Things are changing with 5G NR and the new categories of base stations. In femto or pico cell base stations, the front-end has to be compact, reducing the number of components to the strict minimum. The usually bulky isolator, that does not bring any extra functionality except protection, has to be removed. As such, the non-linearities of other components such as duplexers therefore results in impedance mismatch at the transistor's drain. Things get even worse in Massive MIMO antennas, where dozens of PAs emit simultaneously in a very limited space. Eliminating the isolator produces very high crosstalk between the different amplifiers, resulting in strong VSWR at the transistor's drain. In [77], the authors showed that the efficiency of a beamsteering Massive MIMO transmitter where the element PAs are not isolated depended very strongly on the angle of the beam, because of this crosstalk.

Consequences of Impedance Mismatch in Power Amplifiers

Power amplifiers are designed to operate under a characteristic output impedance, usually 50Ω. Maximum power, efficiency and linearity are all function of the presented load impedance. A higher than optimal load will lead to a premature saturation (lower peak power), with a higher gain and eventually high efficiency. A smaller load will inversely allow for more output power –if technologically possible– at the expense of efficiency.

In order to assess the consequences of impedance mismatch, load pull measurements were perfomed on a 1W CMOS power amplifier from SOMOS Semi at 0.9 GHz. The power amplifier's

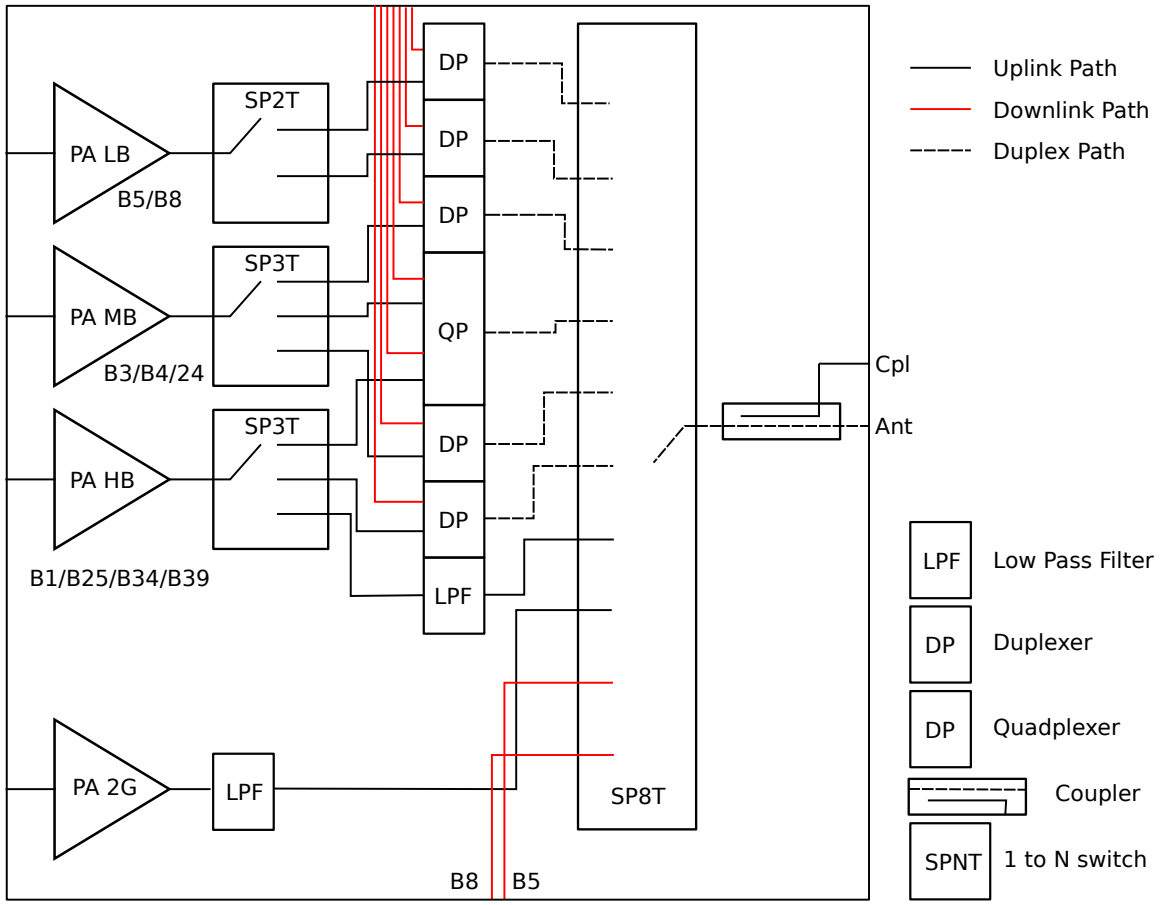


Figure 5.3: User Equipment RF Front End example. Here an LTE Cat 12 triple band 2G/3G/4G RFFE from Mediatek Phase 5 platform. Source : SOMOS Semiconductor

input and output are internally matched to 50Ω. Only the fundamental output impedance is varied, all output harmonic terminations and input terminations are left at 50Ω. For this measurement, the PA was first presented with 50Ω, and then with 12 points selected from the VSWR 3:1 circle, with 30° steps between them. The choice of this VSWR is based on the maximum expected VSWR imposed from the 3GPP for which the linearity requirements have to be fulfilled. The input power was swept from 6 to 20 dBm. Figure 5.4–a presents the drain efficiency versus output power, figure 5.4–b the gain versus output power and figure 5.4–c the ACLR versus output power, when stimulated with a 10 MHz 6 dB PAPR SC-FDMA LTE signal. Figure 5.4–d shows on the Smith chart the corresponding presented impedances. Figure 5.5 presents on the right the maximum drain efficiency and on the left the maximum output power versus the phase of the reflexion coefficient presented at the load. In dotted line we present the results under 50Ω.

We can see from these curves the dependecy of the performance of the power amplifier on the output load. The peak output power goes from approximately 29 dBm up to 32 dBm, almost 3 dB of difference. Similarly, drain efficiency ranges from 62$\%$ down to 37 $\%$. We understand that from a PA designer point of view, it is particularly challenging to realize a power amplifier that respects the stringent requirements of 5G NR under impedance mismatch.

This results concern conventional power amplifiers, mainly single-ended or power combined PAs. Impedance mismatch can also alter the operation of more complex architectures :

- In load modulated amplifiers, the reflexion coefficient presented at the different devices' drain will depend on the output couplers. In a Doherty PA for example, the main and auxiliary ampli-

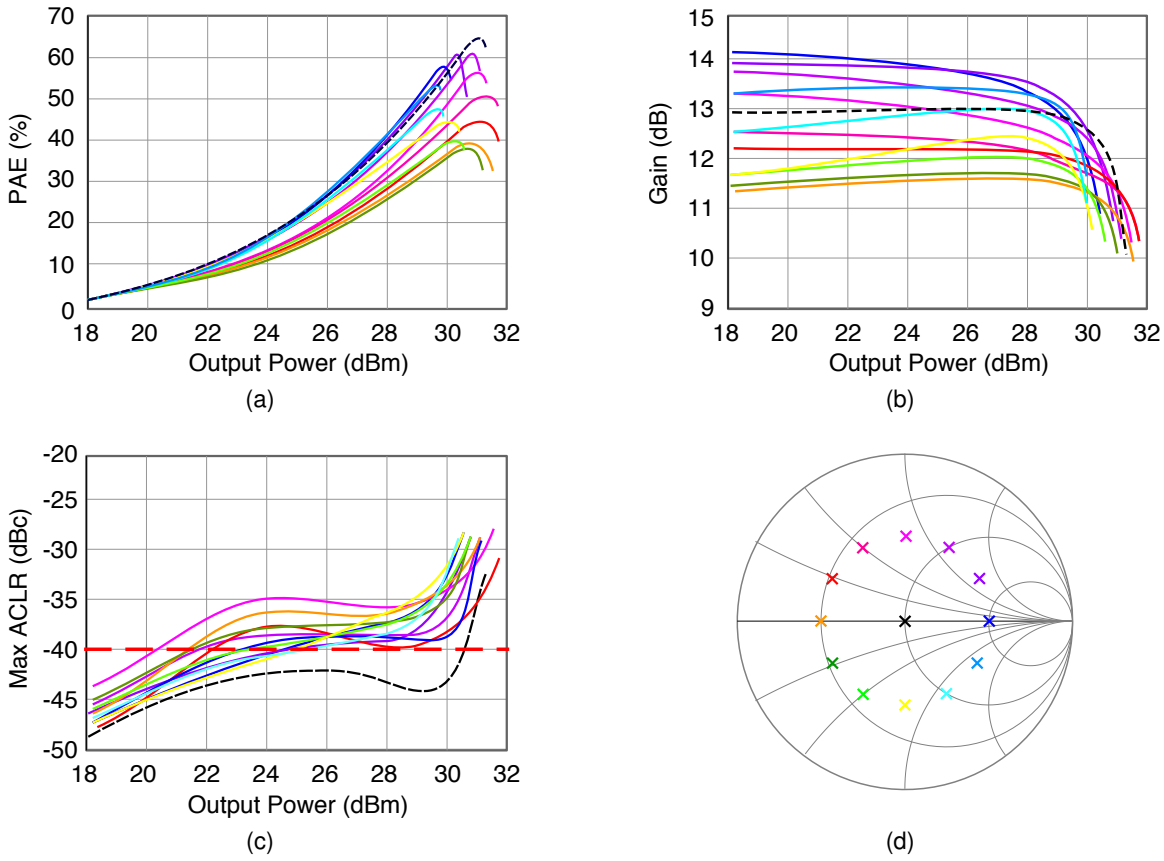


Figure 5.4: Load-pull measurements at 0.9 GHz of a 1W CMOS Power Amplifier from SOMOS Semi. In a), b) and c) PAE, Gain and maximum ACLR versus output power respectivelly, in d) the presented impedances.

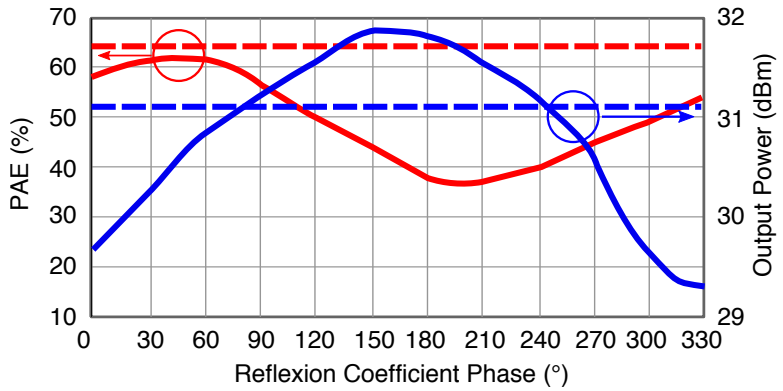


Figure 5.5: In red maximum PAE and in blue maximum output power versus the phase of Γ, for a VSWR=1:3. Dotted lines represent the values with 50Ω

fiers will see the same $|\Gamma|$, but with a different phase, depending on the combiner's phase shift. The load modulation is no longer optimal, further reducing the already poorer performance.

- Adaptive Digital Predistortion uses a directional coupler to detect the emitted signal and characterize the power amplifier. Under VSWR, the measured signal is no longer image of the PAs nonlinearities, and the predistortion algorithm can even make things worse [78]. Special algorithms must therefore take into account the impedance mismatch in order to successfully linearize the PA [79].

Another important aspect of impedance mismatch is its consequences on device reliability. As the name VSWR suggests, impedance mismatch results in the superposition of the incident and reflected voltage waves. In turn this produces voltages maximums and minimums along the transmission path. Under high mismatch, the voltage maximums look more like voltage spikes. If present at the transistor's drain, they can potentially break the device. This is especially true with small band-gap technologies such as GaAs or more importantly CMOS. In fact, the low tolerance to high voltages is one of the reasons CMOS tends to be disqualified for high power PA designs.

5.2 Performance Restoration under Impedance Mismatch

Different solutions exist to correct or cancel out the effects of impedance mismatch on power amplifiers. Considering the device reliability, the most effective solution is to simply detect the voltage overshoot and reduce the output power, either by lowering the gate bias voltage (and thus the gain), lowering the DC drain voltage or lowering the input power. These techniques aim at protecting the transistor from damage, but do not address the lower performance.

It is is much more difficult to actually correct the performance degradation due to impedance mismatch. We can distinguish two different solutions :

- **Impedance detection and correction** : the most straightforward approach consists in somehow detecting the output impedance, and tuning a Tunable Matching Network (TMN) to bring the detected impedance back to 50Ω.
- **Mismatch resilient architectures** such as the Balanced Amplifiers are passively protected from impedance mismatch. Under VSWR, performance is degraded but by a much smaller amount, and the actual degradation depends –in theory– only on the magnitude of the Γ, and no longer on its phase.

Impedance Detection

The most classic impedance detector is based on using directional couplers to detect the incident and reflected waves. Comparing their phase and amplitude difference directly gives the reflexion coefficient. Though very precise, this technique is very bulky, and adds extra loss, reducing output power and efficiency.

A more direct approach consists in using analog impedance detectors. These can either be polar [80, 81] – detecting both magnitude and phase of the output impedance– or scalar [82] –detecting only magnitude information. They are based on analog blocks such as comparators, voltage mixers and rms voltage detectors. In [83], two CMOS voltage detectors were used to measure the real part of the output admittance $1/\mathrm{R_p}$. While this is not enough to completely command an impedance tuner to retrieve nominal – 50Ω– performance, the authors showed that they could use this measurement to assess the peak power degradation, and thus the reduced linearity. Silicon technologies such as CMOS or SOI are in a clear advantage over III/V technologies, as they can integrate on chip the required complex analog circuits.

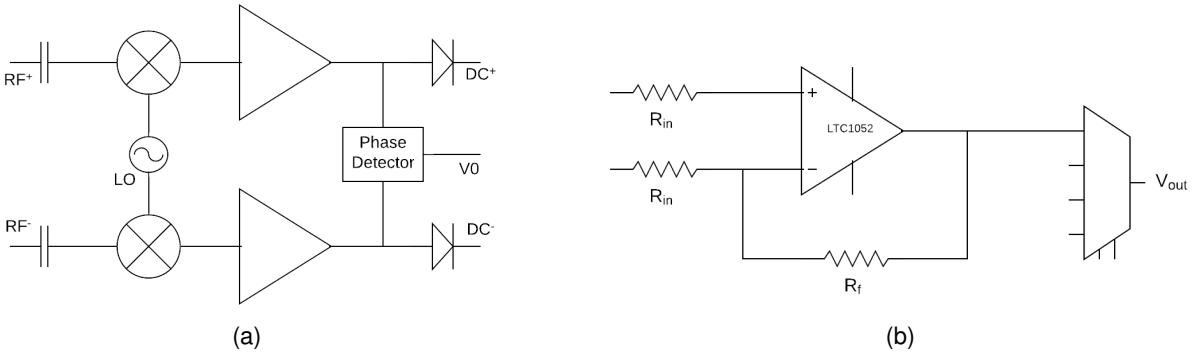


Figure 5.6: In a) a complex impedance detector, measuring the amplitude and phase difference of two different voltages (RF_+ and RF_-. In b) the –simpler– voltage rms detector used in the 6-ports reflectometry approach.

Recently, a novel impedance sensing technique based on 6-ports reflectometry was presented [84]. This approach consists in inserting a certain number of voltage detectors on a transmission line that sample the voltage standing wave at different points. This gives the ability to make *in situ* measurements of the complex load impedance without bringing any additional loss. The concept was later further generalized and impedance sensing up to a VSWR of 10:1 was obtained with 4 voltage sensors positioned directly on a pre-existing output matching network [85]. This approach is very promising, as it allows a precise complex measurement of the impedance with simple analog voltage rms detectors. A vector measurement can thus be obtained without using mixers and oscillators. This approach could be used in mixed technologies RFICs, that use for example a GaN or GaAs power amplifier but include in the same package analog and digital circuits in CMOS or SOI. Figure 5.6 compares the detector circuits for a) a classic impedance detector and b) a reflectometry based detector. We note that the latter technique requires as many operational amplifiers as detection points, usually between 4 and 6.

Impedance Tuner

Once the output impedance has been correctly measured, a tuning mechanism has to be used in order to retrieve nominal performance. This is mainly obtained with a Tunable Matching Network (TMN), similar to the one used in Dynamic Load Modulation.

We can distinguish two subcategories of TMN :

- Continuous Steps / Varactor based TMN : Generaly based on a diode or FET transistor whose capacitance depends on the DC voltage.
- Discrete Steps / Switched capacitor based : a bank of switched capacitors digitally switched on or off changes the total reactance.

Varactor based TMNs require very high tuning voltages, and are strongly non-linear. Impedance mismatch correction systems therefore use mainly switched capacitors as a tuning element. Since impedance mismatch is a slow process –it is a matter of seconds–, the small bandwidth associated with switched capacitors is not an issue. Furthermore, practically any semiconductor technology includes adequate switches and capacitors.

Different topologies can be used as a tunable matching network, but usually simple π or cascaded ladder networks are used. Depending on the complexity of the system and the algorithm, two, three or more tunable elements can be used.

A very important part of an impedance tuner is the algorithm used to correctly tune the variable components. Once again different approaches can be used. The easiest technique is the iterative algorithm that finds the optimal configuration of the TMN after a certain number of trials [82]. While simple to implement, this technique takes a non-negligeable amount of time to converge, and the state of the amplifier during the process is unknown. LUT based algorithms can also be used [83]. They are rather simple to implement but present limited performance. More complex algorithms using FGPAs or DSPs are much more robust, at the cost of very high complexity [80].

Mismatch detection and correction systems are very promising as they can completely solve the issue related to impedance mismatch. Various CMOS impedance detectors have been presented in the literature, and recently a simpler detection architecture based on reflectometry has been shown to be compatible with III/V technologies. Mismatch correction is on the other hand a very difficult task, as a robust correction algorithm requires large computational ressources. It is therefore not adapted for UE equipments or massive-MIMO systems.

Balanced Amplifier

An alternative solution to impedance mismatch is the use of mismatch resilient architectures. These systems somehow eliminate the reflected wave, thus protecting the amplifier.

The most commonly used technique is the isolator. Usually based on circulators positioned between the PA and the antenna, the reflected wave is redirected at the isolator on a third port, terminated with a 50Ω impedance. It will be radiated by the resistance as heat. The power amplifier never sees this reflected wave, and constantly operates as if terminated correctly. It's performance are independent on the output impedance. Power emitted by the antenna is still reduced, as part of it is reflected back to the isolator. The effective efficiency is therefore degraded, but linearity is maintained. This technique is massively used in 4G Base Stations. The main drawback is the isolator, a bulky and lossy component.

The Balanced Amplifier (BA) presented in chapter 3 is another mismatch resilient architecture. We can understand this feature by looking at the S matrix of the hybrid couplers, defined as :

$$Z_{hybrid} = \begin{bmatrix} 0 & j & -j\sqrt{2} & 0 \\ j & 0 & 0 & -j\sqrt{2} \\ -j\sqrt{2} & 0 & 0 & j \\ 0 & -j\sqrt{2} & j & 0 \end{bmatrix} \tag{5.4}$$

where ports 1 and 2 are the in-phase and quadrature ports, and ports 3 and 4 the isolated and output ports. Considering that the two amplifiers connected to the ports 1 and 2 generate an incident wave of magnitude A and phase difference of 90°, the incident and reflected waves at each port can be found to be :

$$a_1 = A \qquad b_1 = 0 \tag{5.5}$$

$$a_2 = Ae^{-j\frac{\pi}{2}} \qquad b_2 = 0 \tag{5.6}$$

$$a_3 = 0 \qquad b_3 = 0 \tag{5.7}$$

$$a_4 = 0 \qquad b_4 = \sqrt{2}Ae^{-j\frac{\pi}{2}} \tag{5.8}$$

Where a_n and b_n are respectively the incident and reflected waves at each port. If the impedance at the output port (port 4) is mismatched, part of the output power b_4 will be reflected back to the hybrid coupler with a reflexion coefficient Γ_L. We can write :

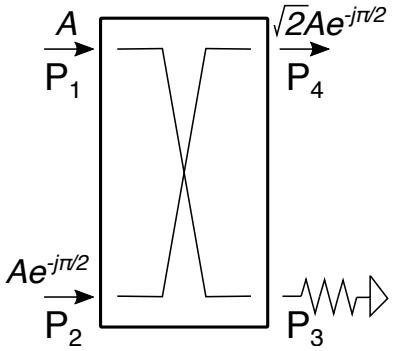


Figure 5.7: Schematic of a hybrid coupler. Ports 1 and 2 represent the in-phase and quadrature ports, and ports 3 and 4 the isolated and output ports.

(5.9) $a_1 = A$ $b_1 = -A.\Gamma_L$

(5.10) $a_2 = Ae^{-j\frac{\pi}{2}}$ $b_2 = Ae^{-j\frac{\pi}{2}}\Gamma_L$

(5.11) $a_3 = 0$ $b_3 = -\sqrt{2}A.\Gamma_L$

(5.12) $a_4 = \sqrt{2}Ae^{-j\frac{\pi}{2}}.\Gamma_L$ $b_4 = \sqrt{2}Ae^{-j\frac{\pi}{2}}$

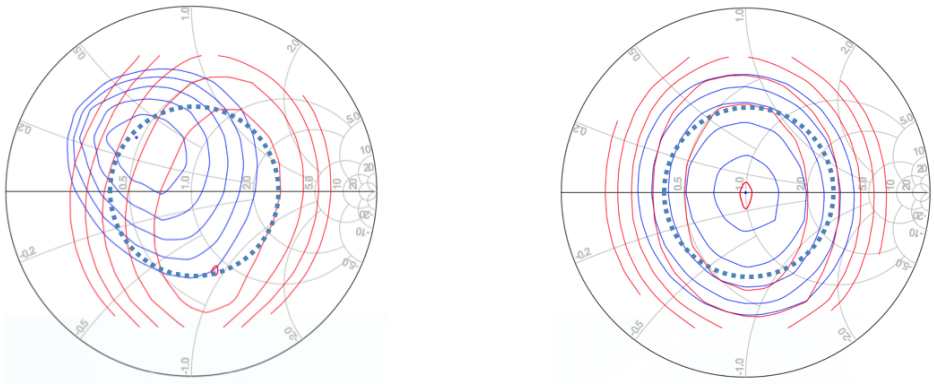
On port 2, the reflected wave b_2 is in phase with the incident wave a_2 while on port 1 they are in opposition. In other words, the branch amplifiers will actually see the same $|\Gamma_L|$, with a phase rotation of 180°. They will tend to compensate each-other. This is where the mismatch resilience comes from, as when one amplifier is loaded with a smaller impedance, the other will see a higer one. The performance degradation associated to the mismatch can therefore be mitigated.

Furthermore the reflected waves $b_{1,2}$ will end up in the isolation port. There is no trace of Γ_L on b_4 or $a_{1,2}$. This provides the balanced architecture with a very good output isolation S_{22}, and thus protects the amplifiers from a voltage standing wave. It can be noted that the same effect takes place on the input. Balanced amplifiers actually present outstanding S_{11} and S_{22} performance.

This impedance compensation can be highlighted by directly comparing load-pull measurements of two different power amplifiers. Both are made of two 27 dBm internally matched CMOS PAs from SOMOS Semi. In the first case Wilkinson combiners are used to combine in-phase the two PAs, making a parallel combined amplifier, while in the latter hybrid couplers are used, in order to make a balanced PA. The load-pull measurement was operated with a passive load tuner from Focus Microwave. The input signal was a CW stimulus at 1.85 GHz and the input power was swept from 5 dBm up to 18 dBm. A reflexion coefficient of up to 0.8 was presented to the two PAs.

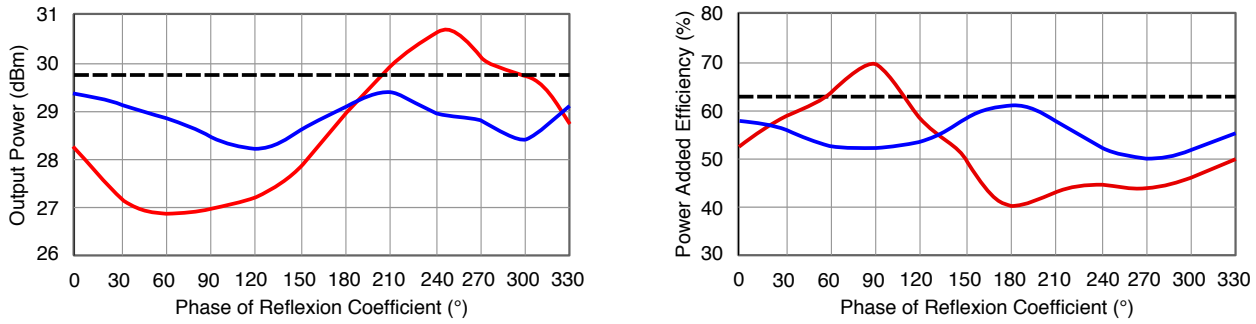
Figure 5.8 a) and b) present the load-pull measurements of the parallel combined and balanced power amplifier respectively. Red contours represent maximum output power and blue contours maximum efficiency. Efficiency steps are of 5 percent and output power steps are of 1 dBm. In figure 5.8 a) the maximum values are 69.3% and 30.7 dBm. In figure 5.8 b), the maximum values are 63% and 29.8 dBm.

The output matching networks of the 27 dBm amplifier composing the balanced and parallel combined PAs was optimized to have at zero reflexion a good compromise between linearity, efficiency and output power. Looking at figure 5.8 a), considering a $|\Gamma_L|$ of 0.33, we can see that for Γ_L phases going from 60 to 110 degrees, efficiency is higher than at Γ_L = 0, while output power is lower. For Γ_L phases going from 210° to 300°, efficiency will be close to its minimum while output power will go higher, to its maximum value. We know that in a balanced configuration, the two amplifiers will see an opposite Γ. Considering a $\Gamma_L = 0.33e^{-j\pi}$, one power amplifier will be at maximum efficiency



(a) (b)

Figure 5.8: Comparison of load-pull measurements of –a a parallel combined amplifier (with a Wilkinson combiner) and –b a balanced amplifier (with hybrid couplers). In red we have peak power contours and in blue peak PAE contours.



(a) (b)

Figure 5.9: Comparison of load-pull measurements of the parallel combined amplifier (in red) and balanced amplifier (in blue). Figure a) presents the peak output power and figure b) the peak PAE versus the phase of the reflection coefficient for a $|\Gamma| = 0.33$.

while the other at maximum power, they will compensate each-other. For the BA, (fig. 5.8 b) both efficiency and maximum power contours are centered around the Smith chart origin and are very symmetrical. We see that in a balanced amplifier, the performance degradation depends mainly on the magnitude of $|\Gamma|$, and not so much on its phase.

Figure 5.9 compares the performance of the parallel combined and the Balanced Power Amplifier versus the phase of Γ_L for a $|\Gamma_L| = 0.33$. The parallel combined configuration presents higher maximum efficiency and output power, but also smaller minimum performance. There is 3.6 dB and 29 percentage points of variation in terms maximum output power and efficiency. The balanced architecture has much less performance variations, 1.2 dB and 9 percentage points. For this application, degradation due to mismatch is more contained and mainly depends on the magnitude of Γ_L, the behavior of the amplifier can be predicted more accurately.

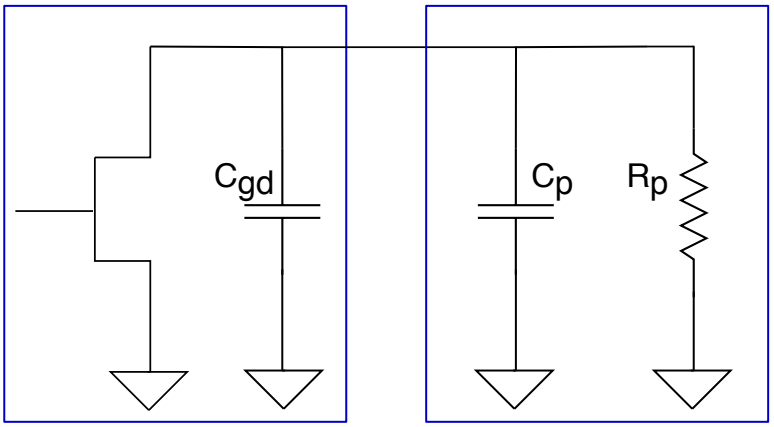


Figure 5.10: Model of transistor and output matching network in RFIC design. The C_p capacitance is the exact opposite of the C_{ds} capacitance, in order to cancel it out. The R_p resistance is therefore the load presented at the intrinsic drain plane.

5.3 Mismatch Resilient High Efficiency Power Amplifier

CMOS Load Modulated Balanced Amplifier

As presented in chapters 3 and 4, the balanced amplifier can also be used as the main amplifier in a Load Modulated Balanced Amplifier. In order to study the behavior of this architecture under VSWR, a 34 dBm CMOS doherty-like LMBA was designed. It was simulated using Advanced Design System (ADS) from Keysight. It was designed for operation over 1750 - 1950 MHz. The design was made following the methodology from [54].

The starting point was the size ratio S_c between the main and the auxiliary transistors. It was fixed to 0.5, based on the available CMOS transistors. The corresponding back-off range γ and the power division factor d_{pm} where then estimated. They can be found on table 5.1. Considering a peak output power of 34 dBm, and a resulting γ of 6.7 dB, the back-off power P_{BO} is 27 dBm, or 24 dBm per branch amplifier. For this design unmatched transistors were chosen. For the balanced amplifier, a single CMOS die with two 30 dBm transistors was used. For the control amplifier a 27 dBm device on an other die was chosen.

CMOS RFIC design methodology is different from that for discrete PAs. Since there is no package, the device parasitics – mainly due to the copper pillars that will connect the die to the substrate – are quasi-negligible. The output load is therefore represented as a parallel RC network, like in figure 5.10. The C_p capacitance is actually negative (it is an inductance in reality) and its value is the opposite of that of the transistors' drain-source capacitance C_{ds}, in order to cancel it out. The R_p is then chosen accordingly to achieve the required output power. It is, in practice, the impedance presented at the intrinsic drain plane. If the second harmonic is shorted, optimal Class B operation is then obtained, with –in theory– high efficiency for the given output power.

The first step consists in estimating the C_{ds}. This can be obtained from simple S parameters, looking at the S_{22}. An ideal negative capacitance or the corresponding shunt inductance can then be applied to the drain to cancel out the C_{ds}. An ideal $R_p = R_{opt}$ resistance can be estimated from (1.8). It is then swept in order to find its optimal value. Finally, the second harmonic termination and the C_p can be swept again to optimize the termination. This process was done on the 30 dBm device for the two different output power levels, at back-off (24 dBm) and peak power (29 dBm) and for the control amplifier at peak power (27 dBm). All transistors were supplied with 3.5V.

The resulting LMBA parameters and chosen impedances are summarized in table 5.1.

The output matching networks, the hybrid couplers as well as all the interconnections were made

Table 5.1: Design parameters of the Load Modulated Balanced Amplifier.

γ	S_c	d_{pm}	$Z_{m,BO}$	$Z_{m,M}$	$Z_{c,M}$
4.7	0.5	0.58	6.84+j9.3	7+j2.61	8.2+j7

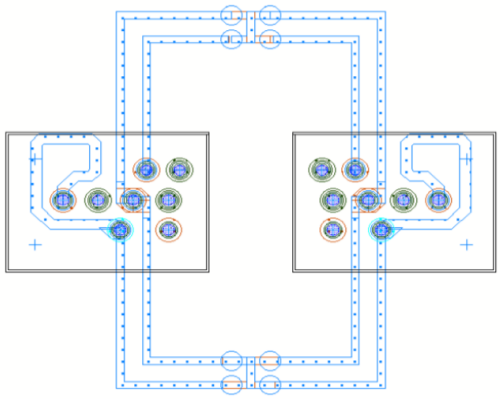


Figure 5.11: Layout of the hybrid coupler in BT technology. The square boxes represent the IPD capacitors that have to be connected with copper pillars on the substrate.

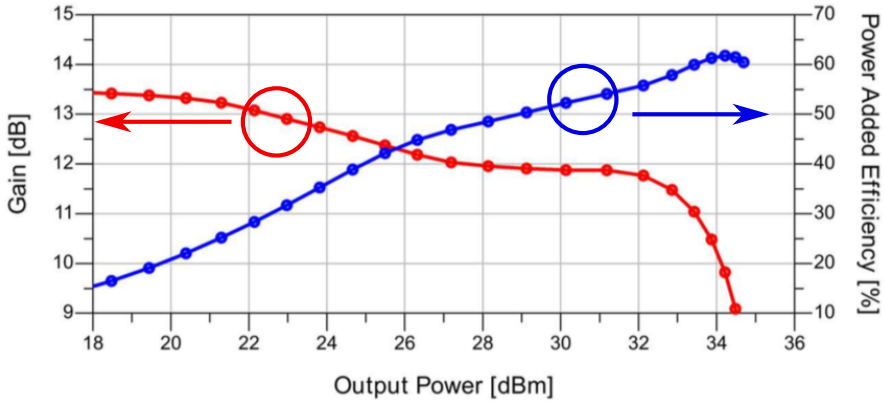


Figure 5.12: Performance of the CMOS Load Modulated Balanced Amplifier. In red the Gain versus the output power, in blue the Power Added Efficiency versus the output power

on a laminate Bismaleimide-Triazine (BT) substrate. It has 5 thick metal layers, allowing the design of complex passive circuits with a relatively high quality factor Q. The different capacitors needed were designed in an Integrated Passive Device (IPD) technology from TSMC and the CMOS power amplifiers were provided by SOMOS Semi. Both the IPD and the CMOS dies are designed to be plugged on the BT substrate with copper pillars. The BT and IPD designs have not been fabricated and electromagnetic extractions were used for all simulations. Figure 5.11 shows the output hybrid coupler's layout.

CW simulations are performed with a single-tone signal at 1.85 GHz. Figure 5.12 shows the simulated efficiency and gain versus output power. Efficiency is around 48$\%$ at 6 dB back-off and reaches up to 63$\%$ at maximum power. The gain of the power amplifier looses around 1.5 dB in the load modulated zone. These results are similar to those expected from a classic Doherty-like PA.

We are interested in exploring the effects of impedance mismatch. One difference with a classic balanced PA is the replacement of the isolation resistor by the auxiliary amplifier. This introduces a reflexion coefficient Γ_{iso} on the isolated port. Considering that the reflected wave is re-injected

from P_{iso} to the branch amplifiers we can rewrite the incident and reflected waves at each port of the output coupler:

$$a_1 = A \qquad b_1 = -A.\Gamma_L(1+\Gamma_{iso}) \tag{5.13}$$

$$a_2 = Ae^{-j\frac{\pi}{2}} \qquad b_2 = Ae^{-j\frac{\pi}{2}}\Gamma_L(1-\Gamma_{iso}) \tag{5.14}$$

$$a_3 = -\sqrt{2}A.\Gamma_L\Gamma_{iso} \qquad b_3 = -\sqrt{2}A.\Gamma_L \tag{5.15}$$

$$a_4 = \sqrt{2}Ae^{-j\frac{\pi}{2}}\Gamma_L \qquad b_4 = \sqrt{2}Ae^{-j\frac{\pi}{2}}(1-\Gamma') \tag{5.16}$$

Where $\Gamma' = \Gamma_{iso}.\Gamma_L$. In case of $\Gamma_{iso} = 0$ (perfectly matched 50Ω resistor), reflected power to the transistors' drain is symmetrical and the two amplifiers compensate each other, like in a normal balanced PA. A different value of Γ_{iso} will add a new reflection term that has different effects on each PA. It will add with the original Γ_L on one while it will be opposite to it on the other. Furthermore, this new asymmetrical reflected wave is redirected back to the antenna, producing a VSWR. Depending on the value of Γ_{iso}, and thus of the S_{22} of the auxiliary transistor, the VSWR compensation will be more or less degraded.

Another effect of mismatch is the performance degradation of the auxiliary amplifier. The power reflected from the antenna will be redirected to the auxiliary PA's drain. This amplifier will see a mix of the control signal *and* the main amplifier's signal, resulting in a different reflexion coefficient than that at the output. Its performance will be strongly degraded.

The designed LMBA was simulated with a varying output load, presenting a $\Gamma_L = 0.33$ with a phase going from 0 to 360°. The results can be seen on figure 5.13. We can see high variations in performance. Maximum PAE changes from 55% down to 36%, and maximum power goes 31dBm to 33 dBm. In figure 5.14 we can see in red and blue the impedances seen by each branch amplifier of the balanced PA at back-off (on the left) and at peak power (on the right). The black dotted line shows the presented load impedance. We see that the amplifier is not very balanced, as there is a clear mismatch between the impedances seen at each branch amplifier's drain. We can also notice that this mismatch is more important at peak power, when there is load modulation. This can be explained by the fact that the control amplifier is also exhibiting decreased performance, further mismatching the system. Our study shows that the LMBA does not inherit the mismatch tolerance of a balanced amplifier.

Double Balanced Load Modulated Balanced Amplifier

In order to retrieve VSWR immunity, the reflection coefficient at the isolated port must be set to zero. In other words, S_{22} of the auxiliary amplifier has to be extremely low. In order to achieve the best performance, power amplifiers are presented with an optimal load, which is not the conjugate of the transistors output impedance. They often have have poor S_{22}.

To solve this issue we propose an alternative architecture with a double balanced output stage. We replaced the classic single ended control amplifier by a balanced PA, which has very good S_{22}. The isolated port of the output coupler is thus loaded with a $\Gamma_{iso} \approx 0$. The auxiliary amplifier becomes "invisible" to the main PAs, who can now act like a normal balanced amplifier, while benefiting from the load modulation. The control amplifier becomes also mismatch resilient.

A schematic of the Double Balanced LMBA can be seen on figure 5.19. This architecture requires two hybrid couplers on the output. They were designed together in the same BT substrate in order to optimize size and performance. In order to keep the same transistor size, two 24 dBm transistors were used for the control amplifier. The optimal impedance was found with the same procedure as earlier. A new matching network was designed to match the control amplifiers' drain to the hybrid coupler. The overall layout of the Double Balanced LMBA can be seen on figure 5.19.

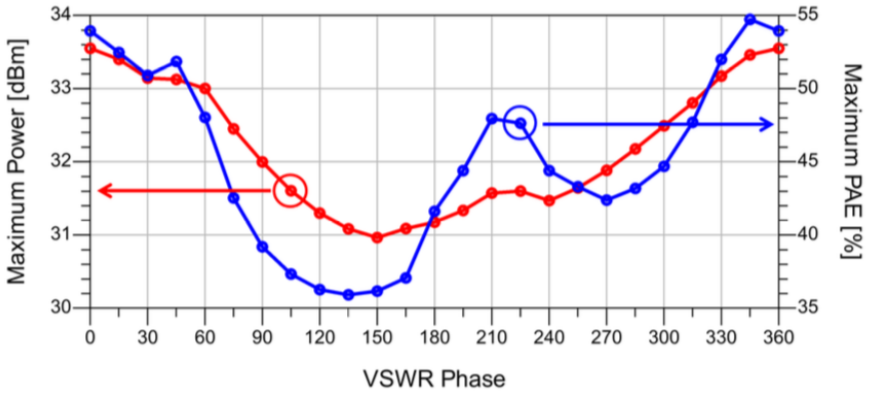


Figure 5.13: Maximum power (in red) and Power Added Efficiency (in blue) versus the phase of the reflexion coefficient Γ, for a VSWR of 3:1.

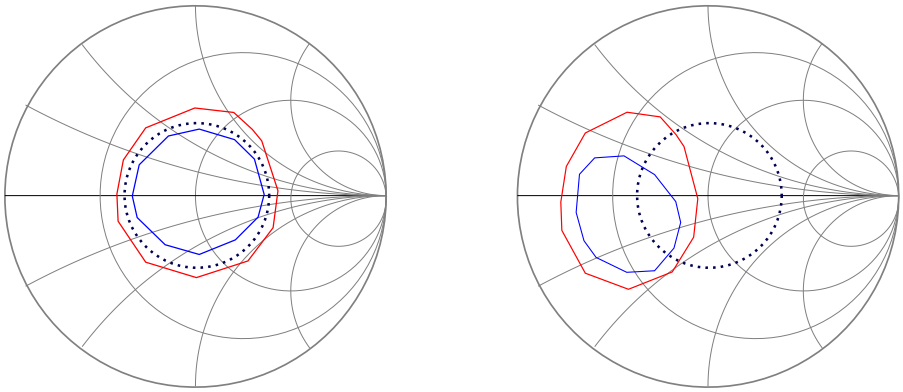


Figure 5.14: In red and blue simulated drain impedance seen by each branch PA of the balanced amplifier, in black the presented load impedance. On the left when at back-off, when the control amplifier is turned-off. On the right at peak power, under load modulation.

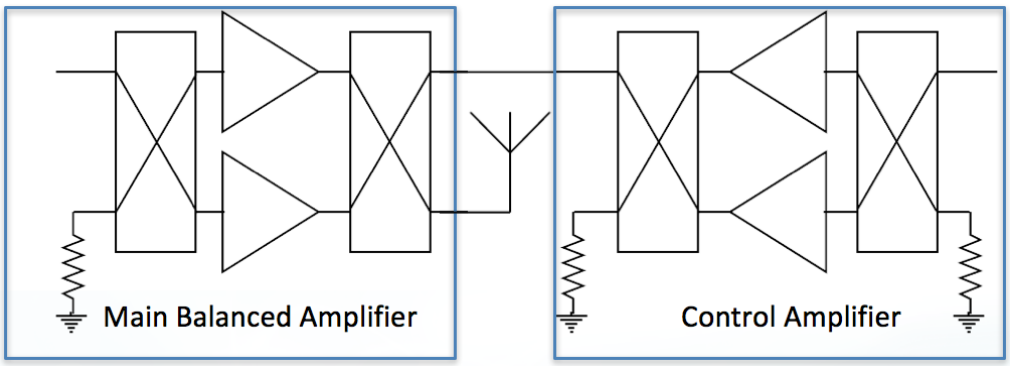


Figure 5.15: Schematic diagram of the Double Balanced Load Modulated Balanced Amplifier

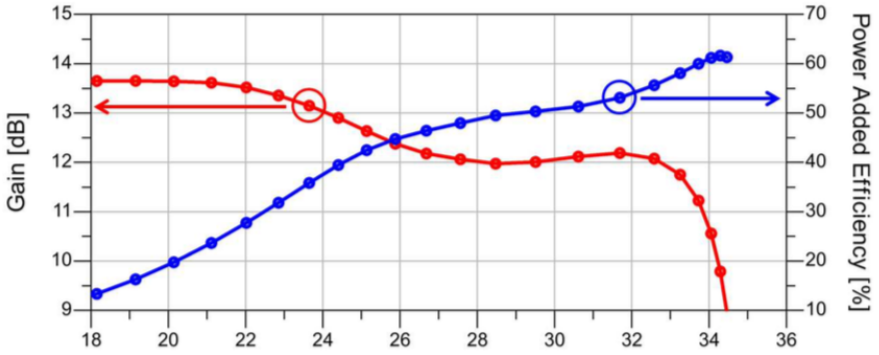


Figure 5.16: Performance of the Double Balanced Load Modulated Balanced Amplifier. In red the gain and in blue the Power Added Efficiency versus the output power.

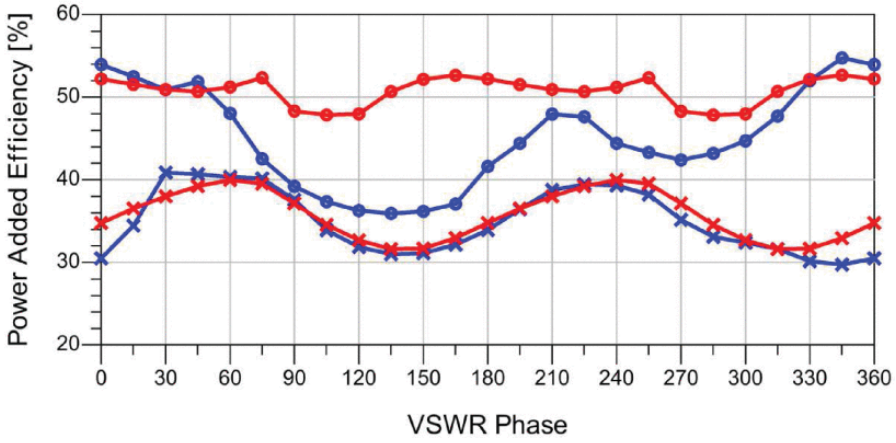
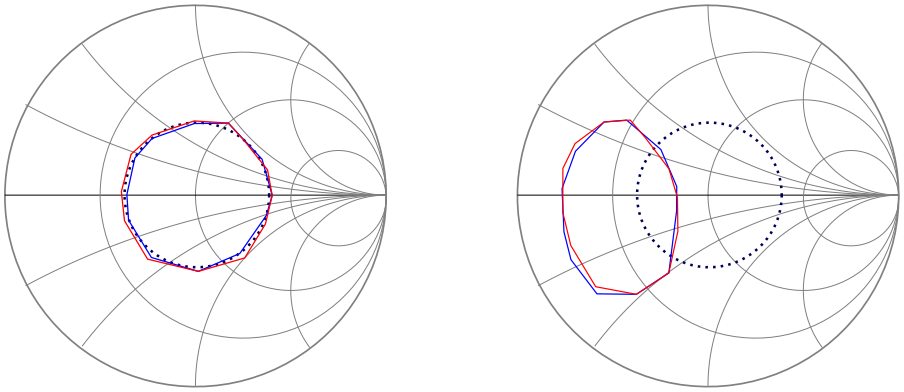


Figure 5.17: Maximum power (in red) and Power Added Efficiency (in blue) versus the phase of the reflexion coefficient Γ, for a VSWR of 3:1. With dot markers at peak power, with x markers at back-off power.

Same CW simulations were done to characterize this novel LMBA under 50 Ohms. Figure 5.16 shows Gain and PAE for one CW simulations at 1.85 GHz.

We see similar results as in figure 5.12. The next step is to test VSWR immunity. A varying load was applied with a $|\Gamma_L| = 0.33$ and a phase going from 0 to 360°. Figure 5.17 compares the efficiency of the conventional (in blue) and double balanced LMBA (in red) at peak power (in dots) and at 6 dB back-off (with crosses). As expected, the double balanced LMBA shows small variations when changing the phase of the reflexion coefficient. Performance degradation depends mainly on the magnitude of Γ_L. It is interesting to see that we observe similar PAE at PBO for both designs. In the low power region (auxiliary PA turned-off, no load modulation), the classic LMBA also exhibits some mismatch tolerance. This implies that the reflected wave coming from the isolation port predicted in (13)–(16) seems to be insignificant. Performance degradation of figure 5.13 comes mainly from the auxiliary amplifier operating under mismatch. Figure 5.18 presents the drain impedances of each branch amplifier of the balanced PA. We can see that the system is much more balanced than before, thus reaching high VSWR resilience.

Figure 5.19 presents the layout of the Double Balanced Load Modulated Balanced Amplifier in BT substrate technology. The red box presents the footprint of the main CMOS amplifier, composed of two 27 dBm CMOS transistors. The blue boxes represent the footprints of the control CMOS amplifiers. They are 24 dBm devices, with only one transistor per die. Unfortunately the substrate



(a) (b)

Figure 5.18: In red and blue simulated drain impedance seen by each branch PA of the balanced amplifier, in black the presented load impedance. On the left when at back-off, when the control amplifier is turned-off. On the right at peak power, under load modulation.

was not manufactured, and measured results of the Double-Balanced LMBA cannot be presented.

5.4 Conclusion

In this chapter, the origin and effects of impedance mismatch in power amplifiers was studied. We saw that in front-end modules where space is limited, such as user equipments or massive MIMO scenarios, the power amplifiers cannot be protected. Impedance mismatch degrades the performance of single ended PAs, but also disturbs the operation of more complex architectures such as DPD or load modulation. The most straightforward solution consists in detecting this mismatch and correcting it, using tunable matching networks. While vector impedance detectors become feasible, even with III/V semiconductor materials, the corrections algorithms required for the control of the TMN are too complex to implement in the low-power low complexity architectures where mismatch is an issue.

An alternative solution, ideal for these aforementioned scenarios, is the balanced amplifier. This architecture inherently presents mismatch resilience. While there is still performance degradation, it is mainly a function of the magnitude of the reflexion coefficient. As such, big dips in performance are avoided.

Finally, the mismatch tolerance of the Load Modulated Balanced Amplifier was studied. We showed that the LMBA does not inherit the intrinsic mismatch resilience of the balanced amplifier. A novel architecture was then proposed, based on a double balanced stage. The designed amplifier presented more than 30% back-off efficiency and 45% peak efficiency with a VSWR of 3:1. The transistors used for this project were CMOS transistors, designed by SOMOS Semi. However, the architecture should be technology agnostic, as we didn't use any assumptions or specific requirements towards the device. It should be particularly interesting in GaAs based amplifiers, which also suffer from impedance variations.

An article based on this work was published and presented in the COMCAS Conference in Tel Aviv, in November 2019 under the name "A Novel Double Balanced Architecture with VSWR Immunity for High Efficiency Power Amplifier".

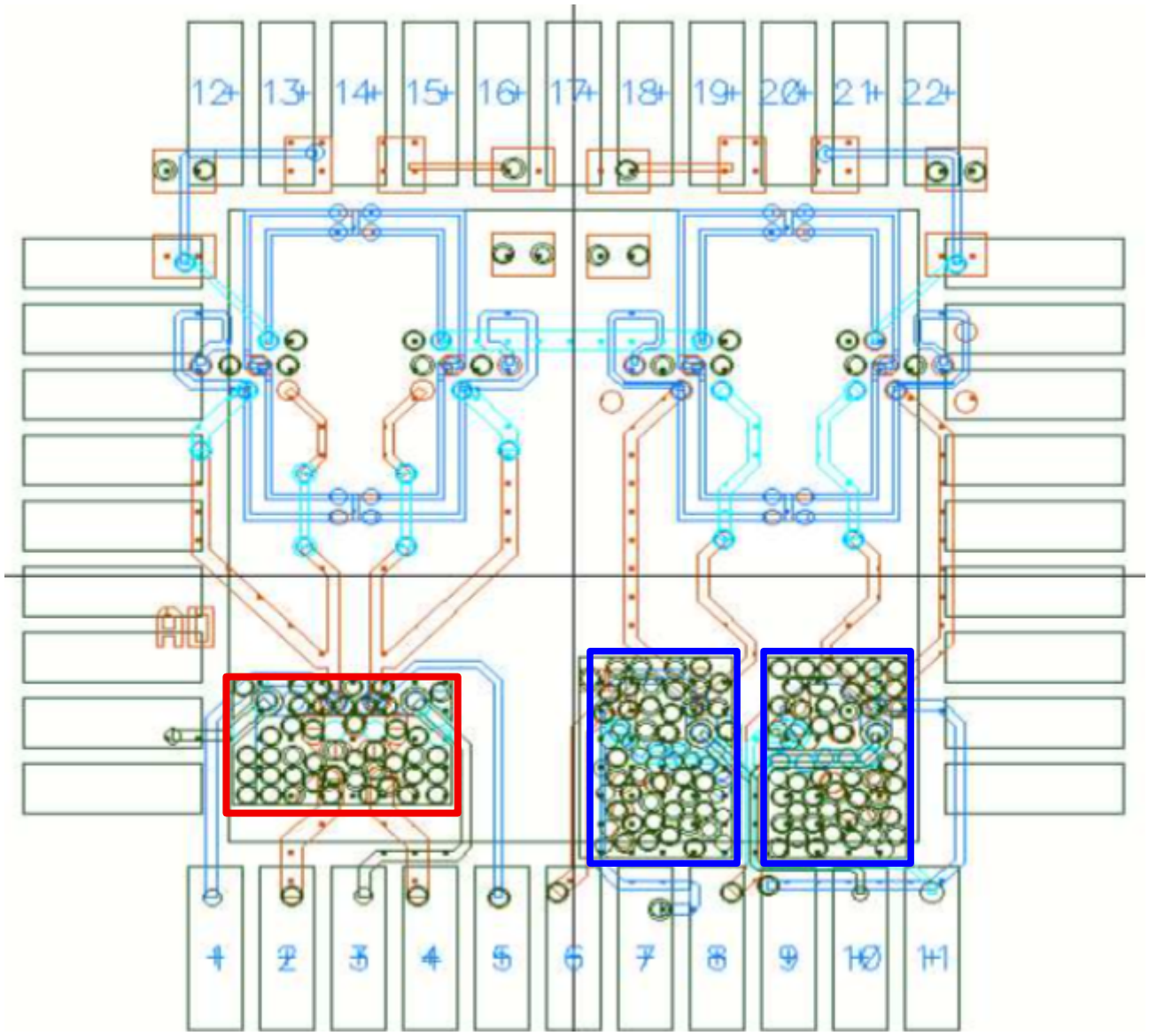


Figure 5.19: Layout of the Double Balanced Load Modulated Balanced Amplifier. We see here the layout of the substrate (in BT technology) which incorporates the OMN and the output combiners.

Conclusion and future work

Wireless communications have seen in the past forty years a spectacular evolution and deployment, and are a major contributor of this new ”digital” era. With a new generation of communication standards approximately every 10 years, the demands in terms of quality of service, power consumption and price have drastically increased. In a global attempt to reduce the extraction of the planet's ressources and the greenhouse gas emissions, the trend for higher data rates and worldwide connectivity seems to be a contradiction. Energy efficiency is therefore a sine qua non condition for 5G NR.

In a wireless transmitter, the most power hungry element has been found to be the power amplifier, whose goal is to give enough power to the emitted signal to establish a communication. Conventional power amplifiers, presented in chapter 1, can maintain high efficiency for a fixed output power for a large bandwidth. However, the efficiency drops drastically when the power is reduced. Considering the high dynamic ranges of the waveforms of 5G NR – potentially more than 10 dB of peak-to-average power ratios– the overall average efficiency of single-ended amplifiers can be less than 30$\%$.

High efficiency architectures for wide dynamic ranges were invented in the 1930's, mainly in the form of the Doherty Power Amplifier or Chireix Amplifier (or Outphasing), presented in chapter 2. Systems based on these architectures can achieve very high back-off efficiencies, reaching in some cases more than 60$\%$ efficiency at 9 dB back-off. Based on Active Load Modulation (ALM), they achieve high efficiency for different output powers by using multiple transistors connected together through a non-isolating combiner. The mutual interaction of the devices results in a modulation of the impedance seen at the output. ALM architectures have been used extensively in 4G base stations, in order to reduce the power consumption. However, in their original – and simpler – form, these systems are often associated with high signal distortion and inherently small bandwidth, making their implementation difficult in more complex systems. Digital predistortion (DPD) is often necessary in order to successfully establish a communication channel. While this is feasible in 4G high power base stations, it becomes more complex in the case of 5G NR. DPD requires digital computing typically 5 times the signal's bandwidth. In 5G NR, this can result in up to 500 MHz in the sub-6 GHz bands, or even 2GHz in the millimeter-wave bands. Considering the power required by the predistorter, the efficiency improvement associated with the DPD can become negligible. Similarly, low power base stations, massive MIMO antennas or handset devices do not have the computing ressources and complexity for predistortion. It is therefore important to further push the linearity-efficiency compromise in order to design linear and efficient PAs that require either very simple DPD or that can be used stand-alone.

A solution to the linearity issue associated with load modulated architectures is the choice of alternative load trajectories that minimize the amplitude and phase distortion of the amplifier. In chapter 1, it was shown that tuning the impedance presented at the drain of a transistor at the harmonic frequencies results in a shaping of the voltage and current waveforms. It was proven through theory and measurement that similar performance in terms of maximum output power and efficiency could be obtained independently of the second harmonic termination by appropriately choosing the

fundamental impedance. This impedance continuum forms the so called J/B/J* continuous modes of operation. In [4, 3] , it was shown that using sub-optimal load trajectories and harmonic impedance tuning could result into better compromises of efficiency and linearity.

In chapter 3, a novel active load modulation architecture was presented, the Load Modulated Balanced Amplifier (LMBA). It is a very versatile architecture, as it can be used either as a reconfigurable PA or a Doherty-like, high efficiency amplifier. One of the major perks of the LMBA is its inherently wideband combiner, based on hybrid 90° couplers. Many papers in the recent literature have presented and exploited this new architecture, showing that it can achieve similar efficiency enhancement as more classic systems such as the Doherty PA. Recently in [55], a design methodology for a high efficiency, single RF-input Doherty-like LMBA was presented. However, this design methodology considers only conventional Class B amplifiers, where the second harmonic is shunted. The resulting amplifier showed high efficiency but very poor linearity.

In a general case, variation of the fundamental drain impedance results in the compression of the gain of a transistor, and a change of the phase of the drain current. The amount of these nonlinearities is determined by the device technology, but is found –from measurement– to be almost independent of the second harmonic terminations. In high efficiency architectures, the overall nonlinearities will depend on the intrinsic amplitude and phase distortions of the device and on the actual design of the output combiner. In a second part of chapter 3, a generalized analysis of the LMBA is performed from a load trajectory point of view. We showed that in the case of the LMBA, gain compression –and thus amplitude distortion– is unavoidable, and depends mainly on the required dynamic range. However, the phase distortion is a function of the device intrinsic parasitics and the actual load modulation. As such, optimal load trajectories can be found that cancel out the intrinsic phase distortion, resulting in a quasi-flat AM-PM characteristic. Since the transistor's phase distortion is almost independent on the second harmonic termination, harmonic tuning can be operated once the flat AM-PM load trajectory is found, in order to maximize the efficiency.

Following the theory proposed in chapter 3, a novel, load-pull based design methodology is presented in chapter 4, that generalizes the approach from [55] for complex load terminations. In order to validate the theory and methodology, three load modulated balanced amplifiers are designed, whose branch PAs have different harmonic terminations. They are referred to as J, B and J* and the second harmonic is respectively capacitive, shunted and inductive, following the continuous modes theory. When measured alone, all three branch PAs show similar performance in terms of output power and drain efficiency, the class B showing approximately 10 percentage points less PAE. When using them inside the LMBA, since the second harmonic changes, the three designs have different fundamental load trajectories, in order to achieve high efficiency over a wide dynamic range. In turn, this load trajectories result in different LMBA characteristics. While all designs present relatively high efficiency (more than 50% at 6 dB back-off) they have very different phase distortions. The best case both in terms of efficiency and linearity is found to be the class J PA, and the worst –in terms of linearity– the class J*. We see therefore the importance of the branch PA, as three almost identical amplifiers result in very different LMBAs. This work resulted in the publication of a conference paper at the 2020 European Microwave Week international conference under the title "Load Modulated Balanced Amplifier designed for AM-PM linearity". A second article has also been submitted to the Transactions on Microwave Technologies and Techniques journal under the title "Linear Load Modulated Balanced Amplifier Design Method Based on Complex Impedance Trajectories".

To test the validity of this theory in a more global approach, a load modulated balanced amplifier MMIC was designed, at 28 GHz, based on a Gallium Arsenide pHEMT device. A study of the technology was performed, in order to assess the utility of harmonic tuning. It was shown that at these high frequencies, with this technology, harmonic tuning is very complicated and brings very small changes in the device's characteristic. The choice of the load trajectory is therefore very restrained,

as there is no other degree of freedom to maximize the efficiency. As a result, it appears that we are not able to design a simultaneously linear and efficient LMBA with our specifications. Nevertheless, a high efficiency Doherty-like LMBA was designed, with state-of-the-art back-off efficiency. Unfortunately the amplifier is particularly narrowband, due to some design choices that were not optimal. The MMIC LMBA, as well as two other amplifiers –a single-ended PA used as the control amplifier and a balanced PA used as the main amplifier in the LMBA– are currently under fabrication, and will be soon be tested by the Microwaves group of Colorado University – Boulder.

In the last chapter of this thesis, another challenge of power amplifier design was studied : the issue of impedance mismatch. It is a well-known fact that in handset devices, the power amplifier is never actually loaded with the appropriate 50Ω impedance, partially due to the complexity of the RF front-end, but mainly because the environment of the device is constantly changing. Usually in base stations, the PAs are protected with an isolator and do not have issues of antenna mismatch. However, systems such as nano-cell base stations or massive MIMO do not have room for the bulky isolator. Impedance mismatch deteriorates the amplifier's overall performance, and can even damage or destroy the device. In high efficiency architectures, impedance mismatch drastically decreases the back-off efficiency. The Balanced Amplifier is an inherently mismatch resilient architecture. Being the basic constituent of the LMBA, the sensibility to impedance mismatch of the LMBA was studied in chapter 5. It was shown that in the back-off region, when the control amplifier is turned off, impedance mismatch has little effect to the overall performance. However, at peak power, this resilience is no longer observed, the system is unbalanced. This sensitivity was tracked down to the control amplifier, which is a conventional, single-ended PA. In order to alleviate this issue, a novel Double-Balanced LMBA is presented, where the control amplifier is also a balanced PA. The overall size of the amplifier does not change a lot, as the transistor periphery is still the same. Using CMOS RFIC technology, the double-balanced LMBA was integrated in a 5mm x 5mm design. The resulting amplifier presented more than 30% back-off efficiency under a VSWR of 3:1. A paper presented this work in the COMCAS international conference at Tel-Aviv, in October 2019, under the title "A Novel Double Balanced Architecture with VSWR Immunity for High Efficiency Power Amplifier".

The contributions of this thesis are summarized as follows :

- A new mathematical description of the Load Modulated Balanced Amplifier in Doherty-like operation based on the loads presented at back-off and peak power.
- The proposal of a novel design methodology for the design of a Doherty-like LMBA using load-pull measurements of the branch transistor to achieve the best linearity/efficiency trade-off.
- The article "Linear Load Modulated Balanced Amplifier Method Based on Complex Impedance Trajectories" was submitted for publication at the TMTT journal
- The design of three harmonically tuned LMBAs to support the proposed methodology. Our results showed that Class J like harmonic termination of the branch amplifier results in the best linearity/efficiency trade-off for GaN devices when harmonic tuning is possible.
- The design of a K band 30 dBm dual-input MMIC LMBA in GaAs 0.15um process from Win Semiconductor.
- A novel double-balanced LMBA architecture resilient to antenna mismatch

Future Work

In the immediate future, measurement of the K band MMIC amplifiers presented at the end of chapter 4 has to be done. The three MMIC designs will be delivered to the University of Colorado Boulder

by the end of the year 2020. The measurement and analysis will be performed directly on the dies with a probe station.

The work presented in this thesis is focused on exploring novel architectures that achieve the required linearity and efficiency of 5G NR while minimizing the system complexity. So far the study was focused on narrowband systems in order to minimize the various parasitic effects related to wideband operation, such as short and long-term memory or sub-optimal impedance trajectories throughout the band. One of the great challenges of modern power amplifier designs is to maintain the high linearity and efficiency over large frequency bands in order to minimize the number of PAs in an RF Front-End. Similarly, 5G NR waveforms can achieve up to 200 MHz instantaneous bandwidths. The resulting performance is not only dependent on the RF frequency characteristics of the PA, but also on the baseband and harmonic terminations. Recently a continuous modes LMBA was designed [86]. The matching network presented fundamental and harmonic class J, B and J* impedances throughout the band, reaching more than 46% PAE at 6 dB back-off from 1.45 GHz to 2.45 GHz. It would be particularly interesting to see if linear operation can still be obtained with such wideband architectures. The linearity could also be compared at different frequency points, in order to see the evolution of the AM-PM distortion with the resulting load trajectory. A wideband linear-efficient LMBA could also be designed by synthesizing a network presenting class J like impedances throughout the band. There are strong reasons to believe that at least 50% fractional bandwidth could be achieved with such a linear-efficient class J LMBA in the sub-6 GHz bands.

As stated earlier, the results of chapter 4 are technology dependent. Non-zero second harmonic termination results in higher drain-source voltage. It is therefore challenging to design a robust Class J amplifier in CMOS or GaAs technologies. It would be interesting to see if linear and efficient load trajectories can still be found for these technologies, at frequencies where harmonic tuning is possible with the device parasitics.

French abstract – Résumé de la Thèse

Depuis le début des communications cellulaires, dans les années 80, un nouveau standard de télecommunications mobiles se déploit approximativement tous les dix ans. Chaque nouvelle génération impose son lot de contraintes aux fabricants de composants afin d'améliorer toujours plus les performances tout en diminuant les coûts et la taille des circuits.

Parmi les grands challenges que doit relever le nouveau réseau de télécommunications 5G (5G NR), le rendement énergétique est primordial. Dans un contexte mondial de limitation des émissions de gaz à effet de serre et de l'exploitation des ressources planétaires, le coût énergétique pour la transmission d'un bit de donnée doit être réduit de 90% par rapport à la précédente génération de réseaux mobiles.

Des signaux de plus en plus large bande sont exploités dans le but d'augmenter au maximum le débit, atteignant jusqu'à 400 MHz dans certains cas. Pour optimiser l'utilisation des cette bande passante, des modulations complèxes, à très haute efficacité spéctrale sont utilisées. Or, ces signaux conduisent à des grandes différences entre la puissance maximale et la puissance moyenne émise (PAPR). Afin d'émettre correctement tous les niveaux de puissances nécessaires, la puissance moyenne de l'amplificateur de puissance (PA) doit être réduite, de la même quantité que le PAPR du signal émis. On appelle ce niveau de puissance Puissance Back-Off (OBO). Or, le rendement énergétique des PA est au plus haut à la puissance maximale, et diminue très rapidement. Ainsi, en considérant un amplificateur classique, ayant un rendement maximal de 78% et un signal LTE (4G) avec un PAPR de 8.5 dB, le rendement moyen peut chuter jusqu'à 15%. Cette contradiction est au cœur du développement des amplificateurs de puissance.

Un rendement élevé pour une gamme de puissances étendue peut être atteint en changeant dynamiquement l'impédance vue au drain des transistors. Les architectures basées sur ce concept, sont en général composées de deux ou plusieurs transistors, connectés ensembles à travers un réseau combineur non-isolant. En imposant une asymétrie de phase et/ou d'amplitude, chaque transistor module l'impédance vue par l'autre, traçant une trajectoire de charge qui maintient le rendement pour toute la gamme de puissances.

Malgré leur efficacité énergétique, les architectures basées sur ce concept présentent généralement une très forte dégradation de la linéarité. Les caractéristiques du transistor telles que le gain et sa phase dépendent de l'impédance présentée à la sortie. Ainsi, les amplificateurs à modulation de charge active sont soumis à des fortes distorsions d'amplitude (AM-AM) et de phase (AM-PM).

Récemment, l'Amplificateur Équilibré à Modulation de Charge Active (Load Modulated Balanced Amplifier - LMBA) a été présenté comme une nouvelle alternative aux amplificateurs à modulation de charge active classiques comme l'amplificateur Doherty (DPA) ou Chireix (OPA). Il est composé d'un amplificateur principal, équilibré (Balanced Amplifier) et d'un amplificateur de contrôle. L'amplificateur équilibré est constitué de deux amplificateurs de branche reliés entre eux par des coupleurs hybrides en entrée et en sortie. L'amplificateur de contrôle injecte un signal dans le port isolé du coupleur de sortie, qui va venir moduler l'impédance vue au drain des transistors de branche. La figure 20 présente un schéma de principe de cette architecture. Par rapport aux autres

architectures à modulation de charge active, le LMBA présente trois avantages significatifs :

- L'amplificateur de contrôle est isolé, et voit donc toujours la même impédance de sortie. Ainsi, il peut être conçu séparément du reste du circuit, et n'influe que très peu la linéarité du LMBA.
- Le combineur de sortie du LMBA est un coupleur hybride. A l'inverse du PA DOherty, la modulation d'impédance est donc indépendante de sa structure, et est définie uniquement par les rapports de phase et d'amplitude entre le signal de contrôle et le signal des transistors de branche. Ainsi, la modulation d'impédance peut être reconfigurée après fabrication, en générant séparément ces deux signaux.
- Le coupleur hybride utilisé comme combineur est un composant large bande. Le LMBA peut donc en théorie atteindre des bandes passantes plus élevées que l'amplificateur Doherty, de façon très simplifiée.

Cette thèse a pour but d'étudier l'impact de la trajectoire des impédance sur la linéarité des amplificateurs à modulation de charge active. Cette étude est basée sur l'amplificateur LMBA, choisi ici pour sa flexibilité et ses capacités de reconfiguration de la trajectoire après fabrication. Une nouvelle analyse mathématique du fonctionnement du LMBA est proposée, qui se base sur les impédances en back-off et à puissance maximale ainsi que sur les performances du transistor de branche pour ces charges. Cette nouvelle formulation aboutit à une méthodologie de conception d'amplificateurs LMBA et de prédiction des performances à partir de mesures load-pull du transistor de branche. Cette méthodologie est ensuite utilisée pour étudier l'impact des terminaisons harmoniques des transistors de branche sur la linéarité du LMBA. Nous montrons par la théorie et la mesure qu'une impédance capacitive à l'harmonique 2 conduit à une trajectoire d'impédance qui maximise le compromis linéarité / rendement. Cette même méthodologie a aussi été appliquée à un transistor GaAs de WIN Semiconductor en bande K. Le but était de concevoir un LMBA MMIC à très haut rendement à 28 GHz. Cependant, à cette fréquence – et pour cette technologie – l'harmonique 2 a un trop faible impact sur les performances du transistor. Sans ce degré de liberté un fonctionnement linéaire et à haut rendement ne peut pas être atteint simultanément.

Enfin, un dernier objectif était articulé autour de la désadaptation d'impédance. Dans les systèmes nomades tels que les téléphones portables ou les terminaux IoT l'impédance de l'antenne varie au fil du temps, en fonction de l'environnement du système. Or, les amplificateurs de puissance sont conçus pour fonctionner sous une impédance d'antenne précise, généralement 50 Ω. Une étude traçant l'origine de cette désadaptation et ses conséquences sur les amplificateurs de puissance est conduite. La sensibilité du LMBA à la désadaptation d'antenne est ensuite évaluée. Enfin, une nouvelle architecture est proposée, le Double Balanced LMBA, qui permet de garder un haut rendement avec une grande résilience à la désadaptation.

Analyse généralisée du LMBA

L'amplificateur Doherty classique est composé de deux transistors reliés par un combineur non-isolant. On peut distinguer deux zones de fonctionnement :

- A basse puissance, l'amplificateur dit auxiliaire est éteint. Uniquement l'amplificateur principal fonctionne, qui voit une impédance de sortie Z_{bo}. Si cette impédance est bien choisie, l'amplificateur principal va saturer à la puissance back-off et atteindre un très haut rendement.
- L'amplificateur auxiliaire, polarisé en Classe C, s'allume lorsque l'amplificateur principal commence à saturer. Les deux transistors n'étant pas isolés, ils vont moduler mutuellement leur impédance de sortie. L'amplificateur principal – qui voit sa charge diminuer – pourra générer

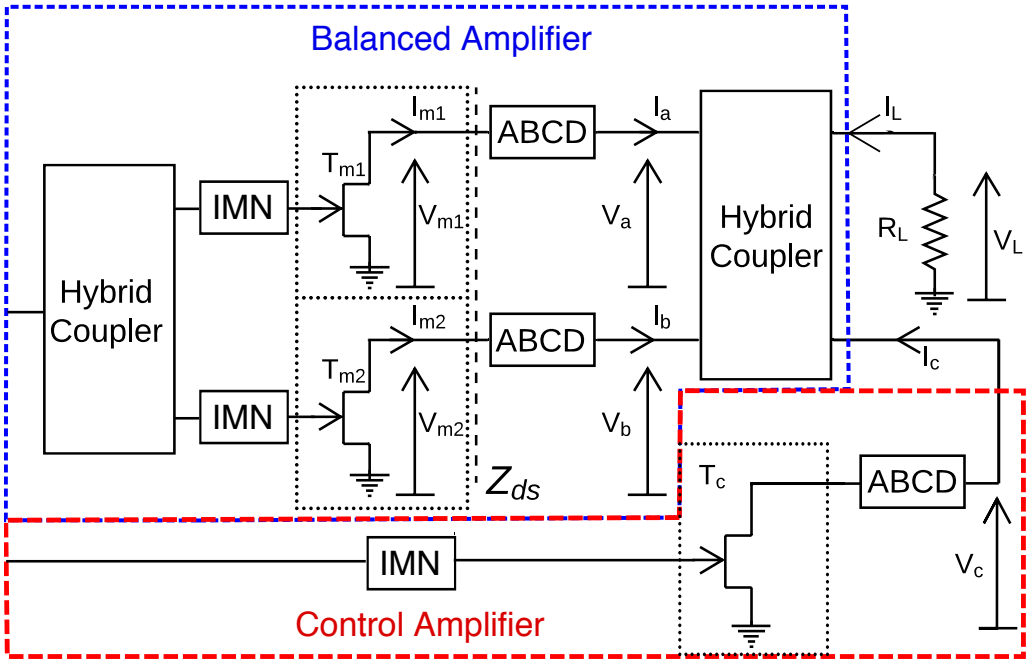


Figure 20: Schéma d'un amplificateur LMBA avec des blocks ABCD représentant les circuits d'adaptation d'impédance de sortie.

plus de puissance tout en restant saturé et gardant un haut rendement. A puissance maximale, les deux amplificateurs saturent et voient une impédance finale $Z_{\max}$. Un deuxième pic de rendement est atteint.

Avec cette technique, des rendements moyens supérieurs à 50% peuvent être atteint avec des signaux 4G. Cependant, le gain d'un transistor dépend de l'impédance au drain et varie lorsque celle-ci est modulée. De même, il a été montré dans [62] que la capacité parasite grille-drain crée une boucle de contre-réaction au sein même du transistor. Par effet Miller, l'impédance d'entrée va aussi dépendre de la charge de sortie, impactant la phase du courant de drain, et donc du signal émis. La modulation d'impédance va donc générer au sein d'un transistor des distorsions d'amplitude (LM-AM pour Load Modulation-Amplitude Modulation) et de phase (LM-PM pour Load Modulation-Phase Modulation). Naturellement, ces distorsions vont avoir un impact sur les amplificateurs à modulation de charge active, qui présentent donc des distorsions d'amplitude (AM-AM) et de phase (AM-PM) particulièrement importantes. Les auteurs de [6] ont montré que la distorsion de phase des transistors (LM-PM) était la principale source de non-linéarité dans les amplificateurs à modulation de charge active. Nous notons ici que les termes LM-AM et LM-PM sont utilisés uniquement pour les transistors qui voient leur charge varier. Au niveau des architectures à modulation d'impédance nous utilisons uniquement les termes AM-AM et AM-PM, car la modulation d'impédance se fait à l'intérieur, et l'impédance à la sortie est fixe.

Différentes techniques ont été trouvées pour améliorer la linéarité des amplificateurs Doherty, généralement au détriment du gain. Une première approche consiste à optimiser les tensions de polarisation des différents transistors [38]. Malheureusement les tensions de polarisation linéaires ne permettent pas de trouver un pic de rendement à puissance back-off. Une méthode alternative est présentée dans [42]. Les auteurs ont montré que le choix de la trajectoire de la modulation d'impédance peut influencer très fortement la linéarité. En ajoutant une partie imaginaire sur l'impédance Z_{bo}, la distorsion AM-PM du DPA pouvait être quasiment annulée.

Cette méthode est très prometteuse car elle permet de rajouter des nouveaux degrés de liberté,

et donc de trouver des solutions avec un meilleur compromis linéarité/rendement. Cependant, elle est opérée ici de façon empirique. Une optimisation complexe est effectuée entre les deux transistors et le combineur afin de trouver les bonnes impédances. Cet article ne considère pas non plus les impédances harmoniques, qui sont choisies en amont dans le seul but de maximiser le rendement.

L'amplificateur LMBA peut être utilisé pour obtenir une modulation d'impédance de type Doherty. L'amplificateur équilibré fait office d'amplificateur principal, et l'amplificateur de contrôle d'amplificateur auxiliaire. En polarisant l'amplificateur de contrôle en classe C, les mêmes zones de fonctionnement que l'amplificateur Doherty peuvent être identifiées. La différence principale entre les deux architectures est que l'amplificateur de contrôle est isolé du système et voit donc une charge fixe.

Dans [57], une ana- lyse mathématique du LMBA est présentée qui aboutit à une méthodologie pour la conception d'un amplificateur LMBA à modulation d'impédance de type Doherty. Cette analyse se restreint à une modulation d'impédance purement réelle, basée sur des amplificateurs de branche en classe B, et ne prend pas en compte la linéarité du système. Ainsi, l'amplificateur réalisé présente 47$\%$ de rendement avec un signal modulé de 10 MHz - 8.6 dB de PAPR, mais une linéarité très faible, autour de -27 dBc.

Ici nous proposons une nouvelle approche, visant à généraliser les travaux de [57]. Le but est d'exprimer le fonctionnement du LMBA pour des trajectoires d'impédance arbitraires afin d'étudier l'impact de la trajectoire de modulation sur la linéarité. Notre développement commence à partir de la figure 20. En considérant que l'impédance caractéristique des coupleurs hybrides est purement réelle, les blocs d'adaptation d'impédance (blocs ABCD) ont été insérés entre les transistors et le coupleur de sortie afin de permettre des impédances complexes au drain des transistors. Nous incluons dans ces blocs le circuit d'adaptation de sortie (OMN) mais aussi les accès de sortie des transistors ainsi que la capacité parasite C_{ds}. Nous éliminons (de-embed) ainsi les éléments parasites, et pouvons mener notre étude au drain intrinsèque du transistor, au bornes de la source de courant interne.

Notre analyse commence en posant les conditions de l'opération de type Doherty appliquées au LMBA:

- En basse puissance, l'amplificateur de contrôle est éteint. Il n'y a donc pas de modulation d'impédance, et les réseaux d'adaptation (OMN) doivent transformer l'impédance caractéristique du coupleur hybride en l'impédance idéale Z_{bo}.
- Dans la zone de modulation d'impédance, l'amplificateur de contrôle injecte un courant qui va se rediriger vers le drain des amplificateurs de branche. A la puissance maximale les deux amplificateurs de branche voient l'impédance $Z_{\max}$.
- Afin de garantir un rendement élevé à puissance back-off et maximale, la partie réelle de la tension de drain des transistors de branche doit atteindre la valeur de la tension d'alimentation.

En imposant ces conditions aux tensions et courants des différents transistors et aux réseaux d'adaptation de sortie (OMN) nous pouvons exprimer le courant I_L de sortie du LMBA à puissance back-off et maximale en fonction du courant maximal du transistor de branche, de sa distorsion de phase Θ_{bo} due à la modulation d'impédance et des impédances $Z_{\max}$ et Z_{bo}:

$$
\begin{aligned}
I_{L_{\mathrm{bo}}} &= \frac{R_{\max}}{R_{\mathrm{bo}}}\sqrt{2\frac{R_{\mathrm{bo}}}{Z_0}}e^{-j\theta_{\mathrm{OMN}}}\frac{I_{\max}}{2}e^{-j\Theta_{\mathrm{bo}}} \\
I_{L_{\max}} &= \frac{Z_{\max}+Z_{\mathrm{bo}}^{*}}{\sqrt{2R_{\mathrm{bo}}Z_0}}e^{-j\theta_{\mathrm{OMN}}}\frac{I_{\max}}{2}
\end{aligned}
\tag{5.17}
$$

Ou $I_{L_{\rm bo}}$ et $I_{L_{\rm max}}$ sont le courant de sortie à puissance back-off et maximale, Z_0, $R_{\rm max}$ et $R_{\rm bo}$ les impédances caractéristiques du coupleur et la partie réelle des impédances $Z_{\rm max}$ et $Z_{\rm bo}$, et $I_{\rm max}$ le courant maximal des transistors de branche. La puissance totale P_L du LMBA en ces deux points de puissance peut être exprimée en fonction de la puissance maximale des transistors de branche $P_{m_{\rm max}}$ et des impédances $Z_{\rm max}$ et $Z_{\rm bo}$:

$$\begin{aligned} P_{L_{\rm max}} &= P_{m_{max}} \frac{|Z_{\rm max} + Z_{\rm bo}^*|^2}{2R_{\rm bo}R_{\rm max}} \\ P_{L_{\rm bo}} &= 2P_{m_{\rm max}} \frac{R_{\rm max}}{R_{\rm bo}} \end{aligned} \tag{5.18}$$

La puissance du signal de contrôle $P_{c_{\rm max}}$ et sa phase Φ_c nécessaires pour produire cette modulation d'impédance sont alors :

$$\begin{aligned} P_{c_{\rm max}} &= P_{m_{\rm max}} \frac{|Z_{\rm max} - Z_{\rm bo}|^2}{2R_{\rm max}R_{\rm bo}} \\ \Phi_c &= \tan^{-1}\left(\frac{X_{\rm max} - X_{\rm bo}}{R_{\rm max} - R_{\rm bo}}\right) + \Theta_{OMN} + \Theta_c \end{aligned} \tag{5.19}$$

Ou Θ_c et $\Theta_{\rm OMN}$ sont les retards de phase des réseaux d'adaptation de l'amplificateur de contrôle et des amplificateurs de branche respectivement.

L'équation (2) nous donne l'étendue dynamique de la modulation de charge en fonction de la trajectoire d'impédance et de la puissance du transistor de branche :

$$\gamma = \frac{P_{L_{\rm max}}}{P_{L_{\rm bo}}} = \left|\frac{Z_{\rm max} + Z_{\rm bo}^*}{2R_{\rm max}}\right|^2 \tag{5.20}$$

Enfin, les distorsions d'amplitude et de phase du LMBA peuvent être déduites à partir de la trajectoire d'impédance et des distorsions LM-AM et LM-PM du transistor de branche pour cette trajectoire :

$$\mathrm{AM-AM} = \frac{P_{L_{\rm max}}/P_{in_{\rm max}}}{P_{L_{\rm bo}}/P_{in_{\rm bo}}} = \frac{|Z_{\rm max} + Z_{\rm bo}^*|^2}{4R_{\rm bo}R_{\rm max}} \frac{G_{m1_{\rm max}}}{G_{m1_{\rm bo}}} \tag{5.21}$$

$$\mathrm{AM-PM} = \angle(\Delta V_L) = \arctan\frac{X_{\rm max} - X_{\rm bo}}{R_{\rm max} - R_{\rm bo}} - \Theta_{\rm bo} \tag{5.22}$$

Ou $\Theta_{\rm bo}$ représente la distorsion LM-PM et $G_{m1_{\rm max}}$ et $G_{m1_{\rm bo}}$ le gain du transistor de branche pour les deux niveaux de puissance.

Nous voyons bien que la linéarité et la dynamique du LMBA dépendent du transistor de branche et de la trajectoire d'impédance. Si nous considérons le cas classique du transistor en class B, cette trajectoire devient purement réelle. Il en résulte que l'AM-PM du LMBA est égale à la distorsion de phase LM-PM intrinsèque du transistor. Celle-ci peut atteindre 30° dans certains pires cas. En ajoutant une partie réactive ou inductive à cette trajectoire, une nouvelle composante de phase vient s'ajouter à la LM-PM du transistor. Pour un transistor de branche donné, nous pouvons donc trouver des trajectoires d'impédance qui vont minimiser la distorsion AM-PM et donc maximiser la linéarité du LMBA.

Jusqu'ici notre étude a porté uniquement sur la fréquence fondamentale. Or, nous savons que les terminaisons harmoniques influent très fortement le rendement des amplificateurs de puissance.

Ainsi, pour une terminaison harmonique donnée, il y a une trajectoire d'impédance fondamentale qui va maximiser le rendement du transistor. Or, nous pouvons montrer par simulation que la distorsion LM-PM est quasi-indépendante des impédances harmoniques. Ainsi, si nous choisissons une trajectoire d'impédance qui minimise l'AM-PM, nous pouvons trouver une impédance harmonique 2 idéale qui va maximiser le rendement durant la modulation d'impédance.

Il est intéressant de noter que si le comportement du transistor de branche pour une trajectoire donnée est connu, alors la linéarité du LMBA peut être prédite. De plus, le transistor de contrôle est isolé du système et voit une impédance fixe; c'est donc un amplificateur classique, et son rendement peut être approximé. Ainsi, en effectuant des mesures load-pull du transistor de branche nous pouvons estimer le comportement global du LMBA, sans avoir à le fabriquer.

A partir de cette analyse nous proposons une nouvelle méthodologie pour la conception d'un amplificateur LMBA à modulation de charge type Doherty, à partir de mesures load-pull :

- **Choix du transistor de branche** : ce choix va dépendre principalement de la puissance et de la fréquence du système. En se référant à l'équation (2), nous voyons que pour une puissance de sortie donnée, la puissance requise du transistor de branche va dépendre de la trajectoire de modulation. Dans une première approximation nous pouvons estimer la puissance pour une trajectoire purement réelle. La puissance du transistor de branche devient alors

(5.23) $$P_{m_{max}} = P_{L_{max}} \frac{2\sqrt{\gamma} - 1}{2\gamma}$$

- **Mesures load-pull** : des mesures load-pull du transistor de branche sont effectuées. Ces mesures peuvent être faites pour plusieurs terminaisons d'harmonique 2. De ces mesures nous sommes intéressés aux contours de puissance maximale, aux contours rendement à la puissance de back-off, et aux distorsions LM-AM et LM-PM du transistor.

- **Analyse des données load-pull** : à partir de ces mesures nous pouvons identifier l'impédance optimale à puissance maximale $Z_{\max}$. Le centre des contours de puissance peut être choisi. Le gain du transistor et la phase du courant de drain pour toutes les autres impédances sont normalisées par rapport aux valeurs à l'impédance $Z_{\max}$, afin d'identifier les distortions LM-AM et LM-PM. Enfin, les distorsions AM-AM et AM-PM du LMBA peuvent être prédites en utilisant les équations (5)-(6) et en y remplaçant Z_{bo} par toutes les autres impédances et $G_{m1_{\mathrm{bo}}}$ et Θ_{bo} par les mesures LM-AM et LM-PM. L'étendue dynamique du LMBA peut être calculée de façon similaire avec l'équation (4). Ainsi, pour chaque trajectoire d'impédance, partant de toutes les impédances vers l'impédance maximale choisie, nous pouvons estimer l'étendue dynamique, les distorsions AM-AM et AM-PM et le rendement du LMBA –si une hypothèse sur le rendement du transistor de contrôle peut être émise. Ces mesures peuvent être faites pour différentes terminaisons harmoniques, afin de trouver le meilleur compromis.

- **Choix du transistor de contrôle** Une fois que les impédances de back-off et maximale sont choisies, la puissance de l'amplificateur de contrôle peut être calculée avec l'équation (3). On peut alors sélectionner un transistor afin d'obtenir le meilleur rendement.

- **Conception des circuits** : les circuit passifs comme le coupleur hybride ou les réseaux d'adaptation peuvent être conçus.

Etude de l'impact des terminaisons harmoniques à la linéarité du LMBA

Nous voulons utiliser cette méthodologie afin d'étudier différentes architectures d'amplificateurs de branche pour mesurer leur impact sur la linéarité du LMBA. Plus précisément, nous voulons voir si,

en utilisant l'impédance harmonique 2 comme degrée de liberté, un meilleur compromis rendement / linéarité peut être identifié. L'objectif de cette partie était donc de concevoir trois LMBA dont les impédances harmonique 2 sont respectivement capacitive, nulle et inductive. Ces terminaisons sont empruntées à la théorie des modes continus [87] et peuvent être définies comme :

$$Z_{opt,f0} = R_{opt}(1 + j\delta) \tag{5.24}$$

$$Z_{opt,H2} = -j\frac{3\pi}{8}\delta R_{opt} \tag{5.25}$$

$$R_{opt} = \frac{(V_{ds} - V_K)^2}{2P} \tag{5.26}$$

Ou V_{DS}, V_K et P représentent la tension d'alimentation du drain, la tension de coude du transistor et la puissance émise souhaitée. δ est le paramètre des modes continus, et peut aller de -1 à 1. Cette théorie prédit que la puissance et le rendement d'un transistor sont les mêmes quelle que soit la valeur de δ. $\delta = 0$ aboutit à un amplificateur classe B classique. On nomme classes J et J* les cas ou $\delta = 1$ ou -1.

En imposant une harmonique 2 réactive (δ non nul), on voit dans (8) que l'impédance optimale fondamentale possède une partie imaginaire. Cela permettrait donc de comparer des trajectoires d'impédance réelle, inductive ou capacitive.

La puissance de sortie maximale a été fixée à 46 dBm, avec 6 dB de back-off, à 2.4 GHz. En appliquant la méthodologie présentée plus haut, nous calculons qu'il nous faut une puissance de 15W pour chaque transistor de branche. Nous avons donc utilisé les transistors CGH40010F de Cree. Les modèles de ces composants donnent accès au drain intrinsèque du transistor, nous pouvons donc choisir directement les harmoniques et observer la trajectoire d'impédance vue de la source de courant interne, sans les parasites.

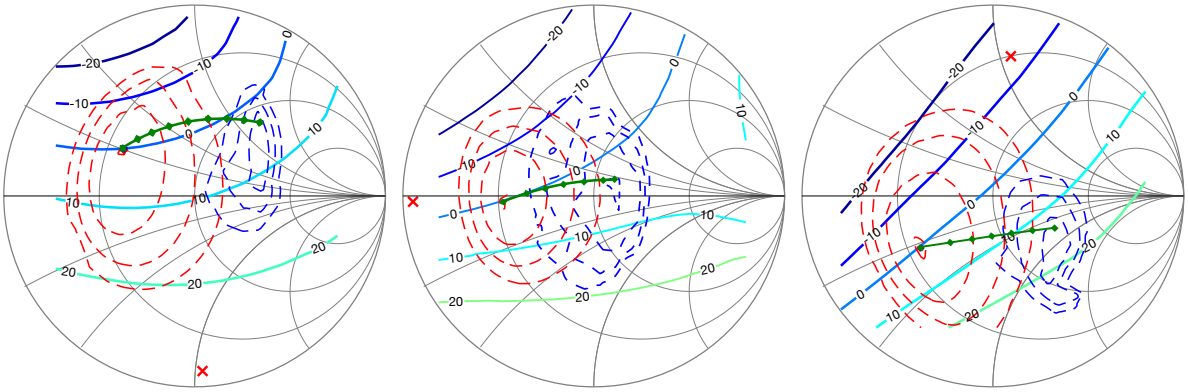
Afin de maximiser le rendement back-off, l'impédance harmonique 2 est choisie en se référant aux équations (8)-(10), en remplassant P comme la puissance de back-off. δ est choisi égal à -1, 0 et 1 respectivement, pour chaque LMBA. Les trois circuits résultants sont nommés classe J, classe B et class J* respectivement. Les impédances harmoniques résultantes sont présentées dans le tableau 2.

Trois simulations load-pull sont effectuées sur le transistor CGH40010F, avec les terminaisons harmoniques mentionnées plus haut. La figure 21 présente les résultats sur les abaques de smith.

Les traits en pointillés rouges représentent les cercles de puissance maximale, et en pointillés bleus les cercles de rendement maximal à une puissance de sortie égale à la puissance back-off. Les croix rouges montrent la position de la terminaison harmonique 2. Ces données sont analysées en suivant la troisième étape de la méthodologie. L'impédance produisant la puissance maximale est choisie comme l'impédance optimale maximale ($Z_{\max}$). Nous normalisons alors le gain et la phase du courant de drain pour toutes les autres impédances par rapport à ceux de l'impédance $Z_{\max}$. les équations (5) et (6) sont alors utilisées pour calculer les distorsions AM-AM et AM-PM du LMBA résultant. Sur la figure 21, les lignes colorées montrent les contours d'AM-PM calculées ainsi. Ces contours sont pris à une puissance de sortie faible (15 dBm), afin de limiter les effets parasite comme la compression des transistors.

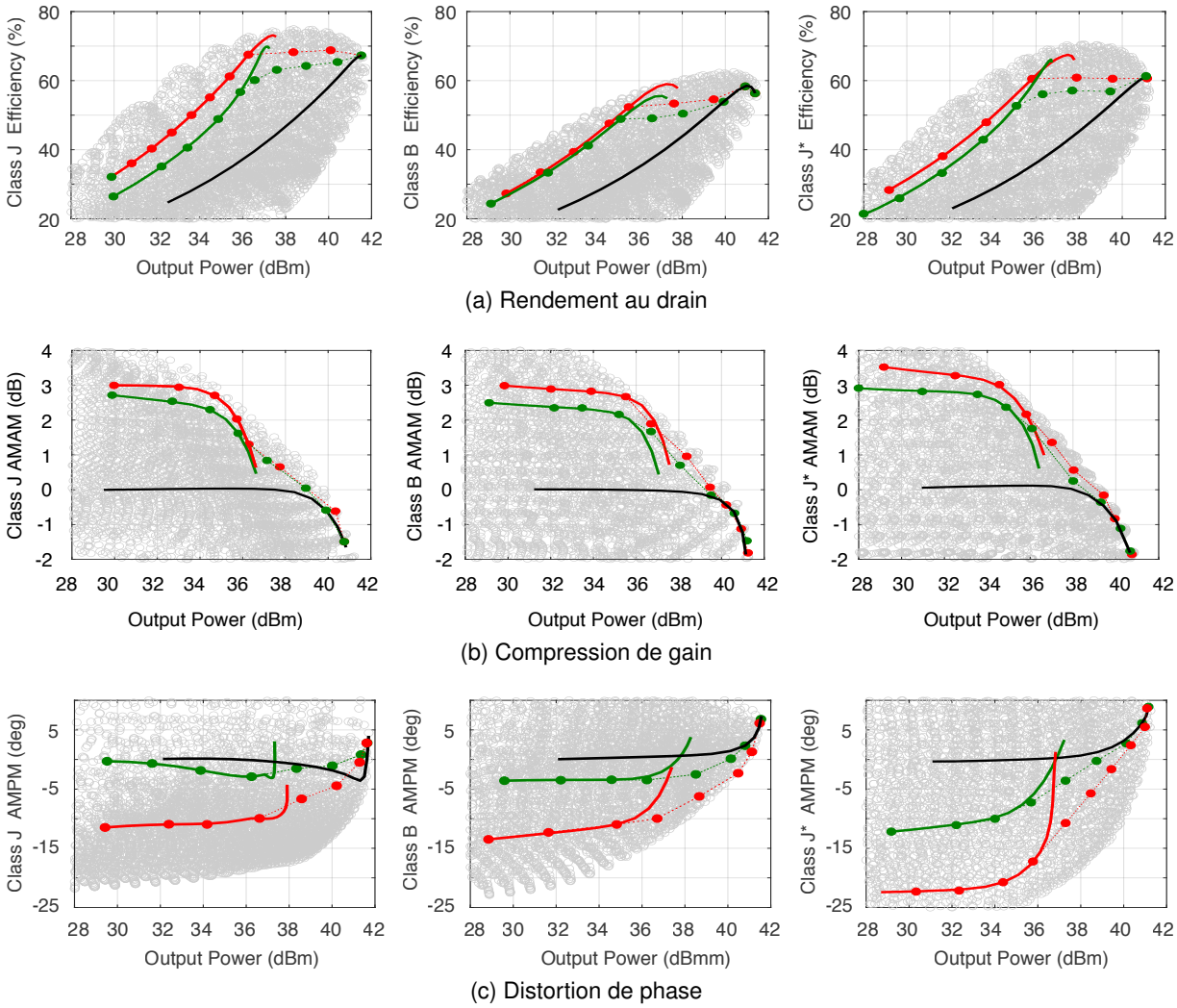
Nous pouvons voir directement les conséquences de la terminaison harmonique. En fonction de l'impédance à l'harmonique 2, le centre des cercles de puissance et de rendement ont une composante inductive, purement réelle et capacitives pour les classes J, B et J* respectivement. Cependant nous pouvons noter que les courbes AM-PM ne changent que très peu d'un cas à l'autre, illustrant la quasi-indépendance de la LM-PM à l'harmonique 2.

Une trajectoire optimale est choisie pour chaque terminaison harmonique, affichée en vert. Chaque extrémité de la trajectoire correspond aux impédances $Z_{\max}$ et Z_{bo}. Le but de ces trajectoires est de minimiser la distorsion AM-PM tout en gardant un rendement élevé en back-off.



(a) Classe J (b) Classe B (c) Classe J*

Figure 21: Simulation load-pull pour les trois terminaisons harmoniques J/B/J*. Les cercles de puissance sont en pointillés rouges, les cercles de rendement à puissance de back-off en pointillés bleus et la distorsion AM-PM en traits colorés. Les croix montrent la terminaison harmonique 2. Les diamants rouges et verts présentent les deux trajectoires d'impédance.



(a) Rendement au drain

(b) Compression de gain

(c) Distortion de phase

Figure 22: En (a) le rendement, en (b) et (c) les compressions AMAM et AMPM en fonction de la puissance de sortie, pour chaque impédance et chaque puissance de sortie. En rouge les courbes maximisant le rendement en back-off, en vert celles du compromis linéarité/rendement et en noir à l'impédance maximale. Les courbes pointillées montrent les performances extrapolées d'une modulation d'impédance.

Cette première figure nous permet déjà de comparer la linéarité de ces trois cas de figure : les trajectoires sélectionnées pour les classes J et B produisent une distorsion de phase inférieure à 5°. Pour la classe J* la trajectoire dépasse les 10° de distorsion.

La figure 22 montre les résultats des simulations en fonction de la puissane de sortie, pour chaque impédance et chaque puissance d'éntrée. Cette dernière va de 15 dBm à 35 Bm. En (a) nous avons le rendement et en (b) et en (c) les distortions AM-AM et AM-PM du LMBA. En noir et en vert nous montrons les courbe correspondant aux impédance Z_{Max} et Z_{bo}, présentées à la figure 21. En pontillé nous avons extrapolé les résultats dans une configuration de modulation d'impédance, en suivant pour chaque impédance de la trajectoire sélectionnée la valeur correspondant à une compression de 1dB.

Sur cette figure nous observons que la même puissance maximale est atteinte pour les trois différentes harmoniques 2. Cependant, le rendement change beaucoup d'un cas à l'autre. La classe J atteint jusqu'à 75$\%$ de rendement, tandis que la classe B ne dépasse pas 63$\%$ et la classe J* 70$\%$. Ceci est en accord avec [41], qui a montré que la classe J est particulièrement adaptée pour maximiser le rendement en back-off dans les amplificateurs à modulation de charge active. En regardant les courbes d'AM-AM nous observons une très faible différence entre les trois cas de figure; l'impédance harmonique ne semble pas impacter la compression du gain importante que l'on observe régulièrement dans les amplificateurs LMBA. Enfin, concernant l'AM-PM, nous voyons que l'amplificateur classe J présente la plus faible distortion. A l'inverse, l'amplificateur J* – dont la partie imaginaire de la modulation d'impédance est l'opposée de celle de la classe J – présente une distorsion AM-PM qui peut presque atteindre les 20°.

De ces simulations nous montrons que pour une distorsion AM-AM quasi-identique, l'impédance à l'harmonique 2 permet de trouver des trajectoires de modulation qui minimisent la distorsion AM-PM. En prenant en compte le rendement et les distorsions, l'amplificateur classe J se montre supérieur aux deux autres, et maximise le compromis rendement/linéarité.

Cette étude basée sur des mesures load-pull du transistor de branche prédit que l'impédance à l'harmonique 2 peut influencer fortement la distorsion AM-PM de l'amplificateur LMBA.

Fabrication et mesure des LMBA en classe J, B et J*

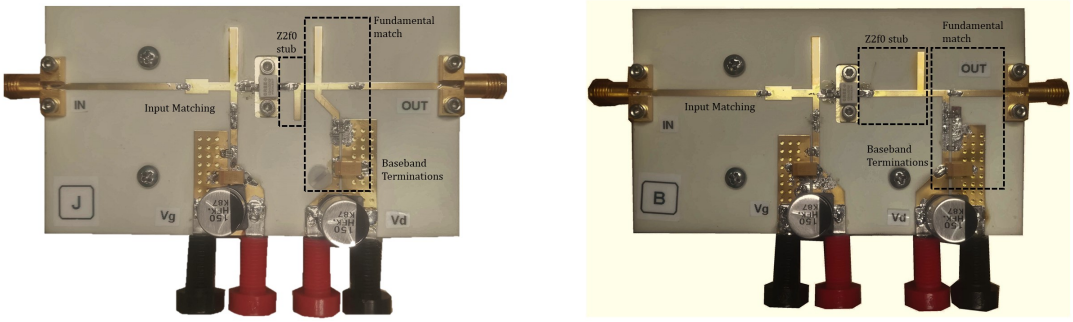
Table 2: Puissance maximale des amplificateurs de branche (indice m), de l'amplificateur de contrôle (indice c) et du LMBA (indice L) à puissance back-off (indice bo) et puissance maximale (indice max) et les impédances fondamentales et harmoniques sélectionnées pour les trois différents amplificateurs.

	$P_{m_{\max}}$	$P_{m_{\mathrm{bo}}}$	$P_{c_{\max}}$	$P_{L_{\mathrm{bo}}}$	$P_{L_{\max}}$	γ	Z_{bo}	$Z_{\max}$	Z_{H2}
J	41.1	37	40.2	40	45.9	5.9	59 + j23	20 + j9	2 + j35
B	40.9	36.8	39.6	39.8	45.8	5.8	50 + j4	17 - j	2 - j41
J*	40.7	36.7	40.7	39.9	45.9	5.9	53 - j20	16 - j10	1 - j4

Les deux dernières étapes de notre méthodologie consistent à choisir l'amplificateur de contrôle et concevoir tous les circuits passifs. En se basant sur les résultats des mesures load-pull, l'impédance back-off avec le meilleur compromis rendement/linéarité est choisie dans tous les cas. Le tableau 2 présente les impédances fondamentales et harmoniques ainsi que les puissances de sortie P_L et les puissance maximales des transistor de contrôle ($P_{c_{\max}}$) et de branche ($P_{m_{\max}}$). Vu les puissances requises, nous voyons que le même transistor CGH40010F peut être utilisé comme amplificateur de

contrôle. L'amplificateur de contrôle du LMBA sera dorénavant toujours identique aux amplificateurs de branche. Sa tension de drain est adaptée afin de produire la puissance maximale requise.

Les trois circuits résultants peuvent être vu sur les figures 23(a), (b) et (c). Trois exemplaires de chacun ont été fabriqués à chaque fois afin de former les 3 LMBAs. Des coupleurs hybrides externes ont été utilisés pour combiner les trois circuits entre eux.



(a) Classe J

(b) Classe B

(c) Classe J*

Figure 23: Les trois amplificateurs en classes J, B et J*

Des mesures avec un signal LTE de 10 MHz et 8.6 dB de PAPR sont effectuées. Deux générateurs Rohde Schwartz alignés temporellement génèrent le même signal pour l'amplificateur principal et de contrôle. L'amplificateur de contrôle est polarisé en classe C, afin qu'il puisse s'allumer au bon moment. Le signal de contrôle est déphasé par rapport au signal principal, et la phase a été choisie afin de maximiser le compromis rendement / linéarité. La figure 24 montre les mesures dynamiques des distorsions AM-AM et AM-PM des trois LMBA. Nous voyons très clairement que tandis que l'AM-AM est quasi-identique pour les trois cas, l'AM-PM change beaucoup avec l'impédance harmonique. Les LMBA classes J ou B présentent une distorsion de phase inférieure à 4°, tandis que le classe J* a plus de 10° de distorsion. A puissance moyenne de 35.5 dBm, les LMBA J,B et J* ont atteint 44, 33 et 38 % de rendement respectivement pour une ACLR de -40.5, -38.5 et -33 dBc. Le LMBA classe J est donc largement supérieur aux deux autres en terme du compromis rendement/linéarité, comme prédit plus haut par les mesures load-pull.

Notre méthodologie, qui consiste à prédire les performance d'un LMBA à partir des mesures load-pull du transistor de branche, a donc bien été validée par la mesure, vu la concordance des résultats entre les simulations load-pull et les mesures des trois LMBA fabriqués. Nous pouvons aussi conclure que dans le cas des amplificateurs de technologie GaN, lorsque l'impédance harmonique 2 peut être utilisée comme un degré de liberte, une terminaison harmonique capacitive permet d'obtenir le meilleur compromis rendement / linéarité.

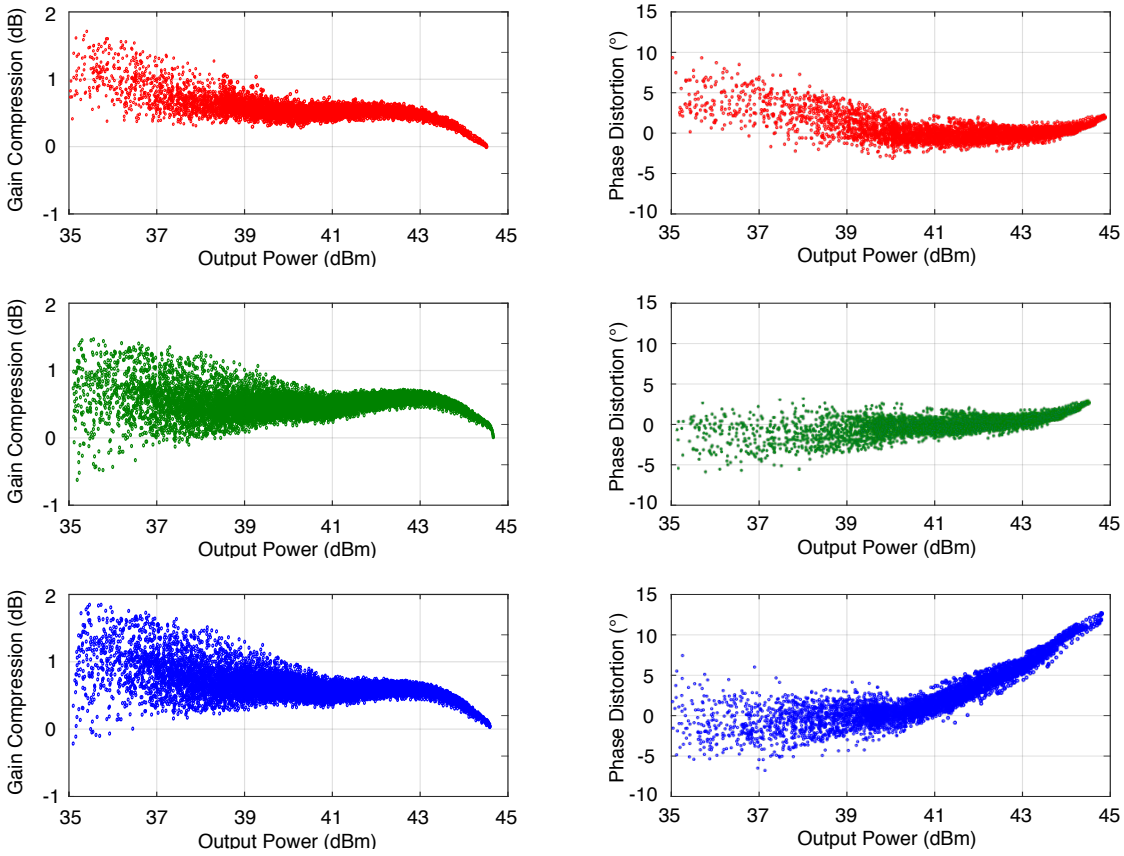


Figure 24: Measures AM-AM (à gauche) et AM-PM (à droite) pour les LMBA J, B et J* de haut en bas, avec un signal modulé de 10MHz, 8.7 dB de PAPR.

Conception d'un amplifier LMBA en bande K en technologie GaAS

Afin de tester la validité de notre méthodologie dans d'autres contextes, un MMIC LMBA en bande K est conçu en technologie GaAs 0.1um de Win Semiconductor. Le but est de fabriquer le premier MMIC LMBA aussi haut en fréquences, avec une puissance de sortie de 30 dBm et 6 dB de back-off. Une étape préliminaire de faisabilité a montré qu'à cette fréquence, l'impédance harmonique avait un impact trop faible pour être utilisée comme degré de liberté. Le choix de trajectoire de modulation d'impédance gardant un rendement élevé est donc très limité. La méthodologie présentée plus haut à donc été utilisée, mais dans le but de maximiser le rendement, et non pas la linéarité.

L'amplificateur résultant peut être vu sur la figure 25. Il comporte deux entrées RF (pour les amplificateurs principal et de contrôle). Chaque amplificateur (les deux amplificateurs de branche et celui de contrôle) comporte un étage driver et un étage de puissance. Les dimensions de la puce sont 3x3 mm. La figure 26 présente le gain et le rendement simulé de l'amplificateur à 27, 28 et 29 GHz. Nous voyons que le rendement back-off est élevé uniquement à 28 GHz : l'amplificateur fonctionne en mode Doherty sur une bande très étroite. L'origine de ce problème a été identifié dans les circuits d'adaptation inter-transistor. La modulation d'impédance des transistors principaux impact aussi leur impédance d'entrée. Les driver placés juste avant voient donc l'impédance de drain changer, et leur performance est dégradée. Une solution potentielle serait d'utiliser un seul driver, placé en amont du coupleur hybride d'entrée. Ainsi l'amplificateur équilibré présenterait toujours la même charge au drain du driver.

Les circuits sont aujourd'hui en cours de fabrication et seront testés prochainement par les

équipes de l'Université du Colorado.

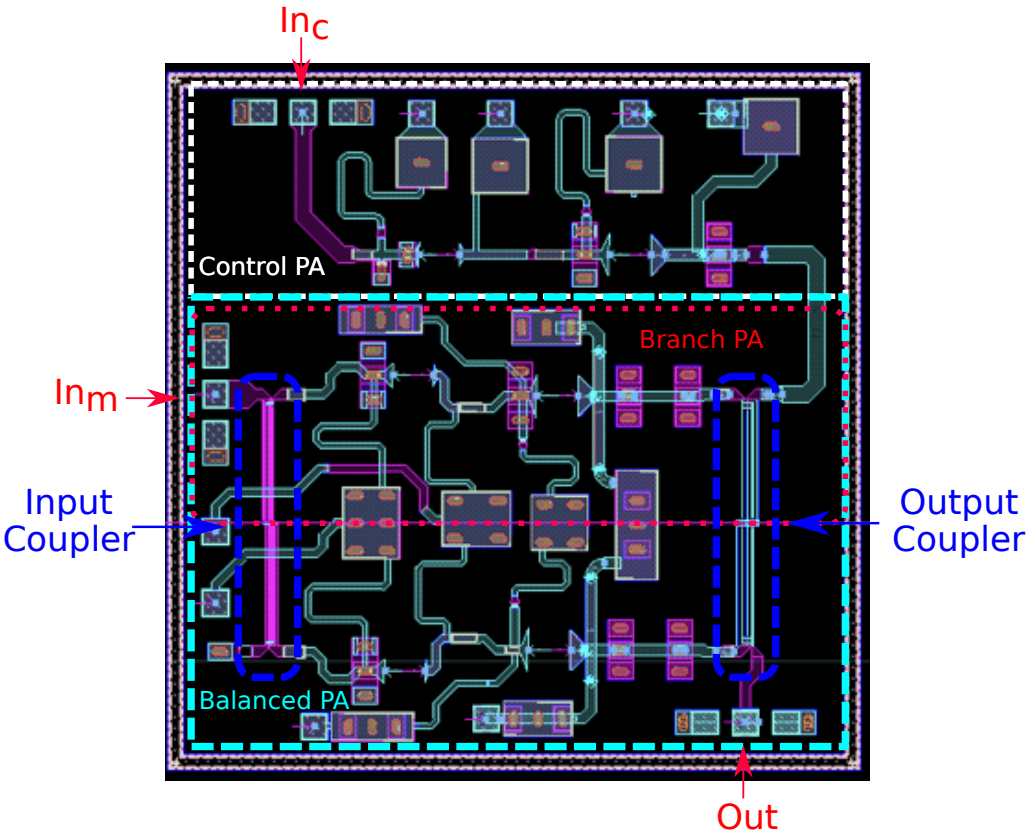
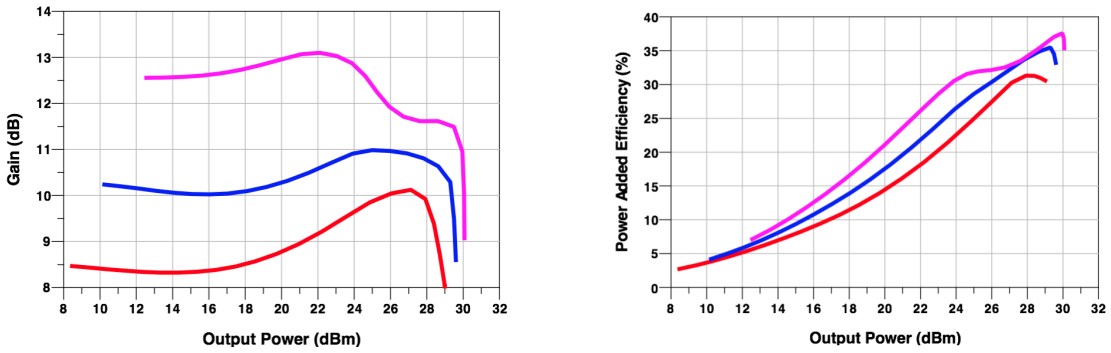


Figure 25: Layout du LMBA en technologie GaAs



(a) (b)

Figure 26: Gain (à gauche) et PAE (à droite) par rapport à la puissance de sortie du LMBA à 27 GHz (en bleu), 28 GHz (en rose) et 29 GHz (en rouge).

Amplificateurs de Puissance robustes à la désadaptation d'impédance

Les amplificateurs de puissance sont conçus pour fonctionner avec une impédance de sortie caractéristique Z_0 fixée, en général égale à 50 Ω. Mêmes dans le cas des amplificateurs à modulation de charge active, l'impédance varie à l'intérieur du système; l'amplificateur global s'attend toujours à

voir en sortie l'impédance Z_0. Or, dans plusieurs applications cette impédance peut varier de façon aléatoire. Dans les téléphones portables par exemple, l'environnement des terminaux change constamment, et donc le diagramme de rayonnement de l'antenne se voit affecté. De la puissance peut être redirigée vers l'amplificateur de puissance, qui observe ainsi un changement de l'impédance de sortie. Historiquement, dans les stations de base, les amplificateurs de puissance sont protégés de ce phénomène par des isolateurs, qui redirigent cette puissance réfléchie vers une résistance d'isolation. Cependant, dans certaines applications 5G comme le Massive MIMO, la densité de composants par surface donnée augmente considérablement, et les isolateurs doivent être supprimés. Dans cet environnement composé de multiples éléments rayonnants, de la puissance peut être réfléchie vers tous les autres amplificateurs. Ainsi, il a été observé dans [77] que le rendement d'une antenne MIMO dépendait de l'angle du rayon d'émission, à cause de ce phénomène de désadaptation.

La désadaptation d'impédance impact toutes les performances des amplificateurs de puissance. Une impédance trop élevée va avoir tendance à diminuer la puissance maximale émise. La linéarité de l'amplificateur est donc fortement dégradée. Inversement, une impédance trop faible va permettre une plus grande puissance de sortie au détriment du rendement, qui diminue très rapidement. Dans les systèmes plus complexes, comme les amplificateurs à modulation de charge active, la désadaptation en sortie impact les performances maximales mais aussi à puissance back-off. L'objectif était d'étudier l'impact de la désadaptation d'impédance sur les amplificateurs de puissance et de trouver une architecture à modulation de charge active robuste à ce phénomène.

Face à cette problématique, deux techniques différentes peuvent être mises en place. La première consiste à détecter l'impédance de sortie de l'amplificateur et agir sur le système afin de retrouver les performances nominales. Différentes approches de détection d'impédance ont été implémentées, avec différents niveaux de complexité. Récemment [85], un détecteur vectoriel d'impédance à été proposé basé sur le concept de la réflectométrie. En installant 4 détecteurs de tension RMS à différents endroits du circuit d'adaptation de sortie, l'impédance peut être mesurée avec une bonne précision. Le système de détection en soi est très simple, utilisant uniquement des amplificateurs opérationnels basiques fonctionnant à basse fréquence. Une fois l'impédance détectée, un tuner d'antenne peut être utilisé afin de transformer l'impédance observée en l'impédance caractéristique Z_0. Ces approches, de détection et correction, peuven apporter de très grandes améliorations des performances. Elles souffrent cependant de deux grands inconvénients :

- Les circuits de détection d'impédance sont basés sur des blocs analogiques relativement complexes. Ils sont donc très bien adaptés pour fonctionner sur des technologies silicium, comme le CMOS, mais leur implémentation sur des amplificateurs GaAs ou GaN est très compliquée.
- Les tuners d'impédance peuvent avoir une très grande précision sur l'impédance finale. Cependant l'algorithme qui estime la configuration idéale pour transformer l'impédance de sortie est généralement trop complexe pour être utilisé tout seul, sur des téléphones portables.

Cette approche est donc très peu utilisée en pratique. L'alternative est alors de se baser sur des architectures d'amplificateur de puissance qui sont naturellement robustes aux changements d'impédance, comme l'amplificateur équilibré (BA). Cet amplificateur est connu pour avoir un très bon S11 et S22. Lorsque l'impédance de sortie varie, une partie de la puissance émise par le transistor est réfléchie et retourne vers le coupleur hybride de sortie. Comme dans les isolateurs classiques, cette onde réfléchie se retrouve redirigée vers le port isolé du coupleur puis est rayonnée sous forme de chaleur par la résistance d'isolation.

Pour rappel, le LMBA est composé d'un amplificateur équilibré et d'un amplificateur de contrôle, branché sur le port isolé du coupleur de sortie. Nous nous sommes donc demandé si le LMBA pouvait hériter des performances de l'amplificateur équilibré sous désadaptation d'impédance. Pour cela, un amplificateur LMBA en CMOS a été conçu, en suivant la méthodologie de [57]. L'amplificateur

fonctionne à 1.85 GHz, avec une puissance maximale de 34 dBm et 6 dB de back-off. La figure 27 présente les résultats de simulation de cet amplificateur. Il atteint 48% de rendement à puissance back-off et 61% de rendement à puissance maximale. Nous avons alors fait varier l'impédance de sortie du LMBA afin de voir l'évolution de ses performances. Nous avons présenté en sortie un VSWR de 3:1, en faisant varier sa phase de 0 à 330 degrés. La figure 28 montre en rouge la puissance maximale de sortie et en bleu la PAE maximale. Nous observons une variation de 20 points de PAE et de presque 3 dB de différence de puissance de sortie. La figure 29 montre en pointillés l'impédance présentée à la sortie du LMBA, et en rouge et en bleu celle vue aux ports du coupleur hybride, avant les OMNs des amplificateurs de branche. En (a) il s'agit de l'impédance back-off (et donc non-modulée) et en (b) l'impédance à puissance maximale. On peut observer sur cette figure que l'amplificateur n'est plus très équilibré, vu la différence entre les courbes rouge et bleue. Ce déséquilibre est d'autant plus important à puissance maximale, lorsqu'il y a modulation de charge. Ceci peut être expliqué par le fait que l'amplificateur de contrôle subit lui aussi la désadaptation, et la modulation de charge ne se fait donc pas correctement.

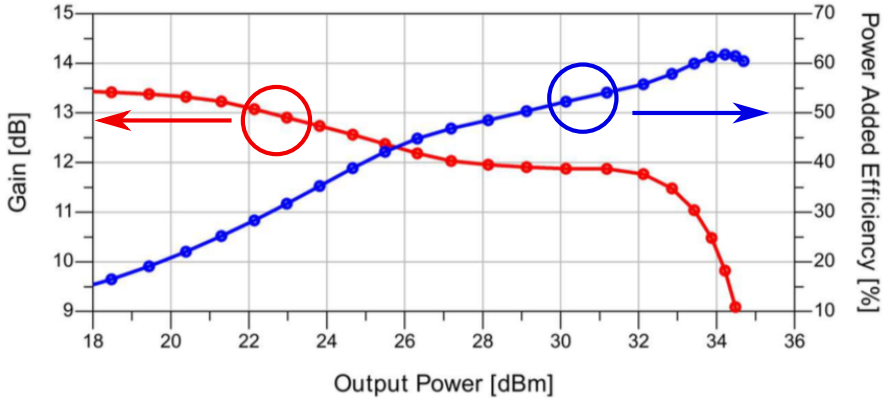


Figure 27: En rouge le gain et en bleu la PAE du LMBA CMOS

Afin de retrouver les performances nominales, le coefficient de réflexion du port isolé de l'amplificateur équilibré doit être nul. Cela revient à dire que l'amplificateur de contrôle doit avoir un S_{22} très faible. Nous proposons donc une nouvelle architecture avec un étage de sortie double balancé. On a remplacé l'amplificateur de contrôle classique par un deuxième amplificateur équilibré, qui à donc un très bon S_{22}. Ainsi, en back-off cet amplificateur devient invisible pour l'amplificateur principal.

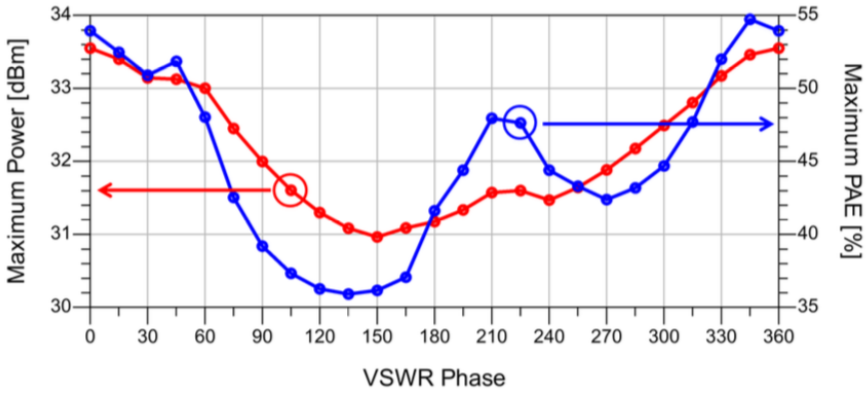


Figure 28: En rouge la puissance maximale et en bleu la PAE en fonction de la phase du coefficient de réflexion pour VSWR de 3:1

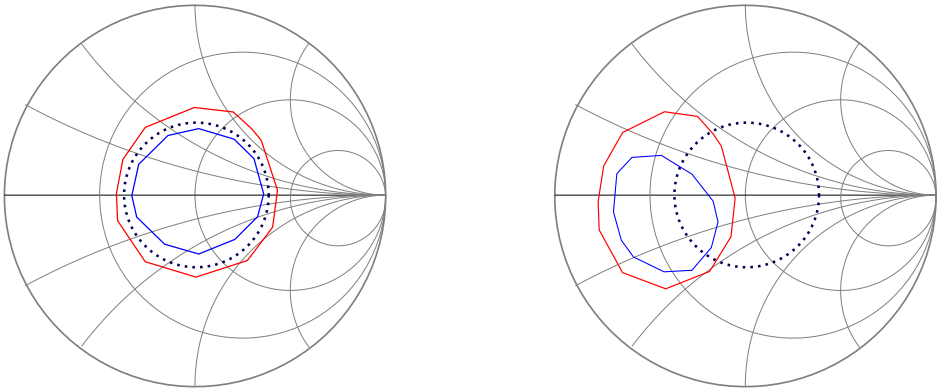


Figure 29: En rouge et bleu les impédances vue par chaque ampli-ficateur de branche et en pointillés noirs l'impédance présentée à la sortie. A gauche à la puissance back-off, quand l'amplificateur de contrôle est éteint, et à droite à puissance maximale.

A puissance maximale il acquiert une robustesse à la désadaptation, et permet donc de limiter la perte de performances. Nous notons ici que la dimension totale des transistors reste la même, car des transistors deux fois plus petits ont été utilisés dans le nouvel amplificateur de contrôle équilibré. Un schéma de principe du Double Balanced LMBA est présenté en figure 30.

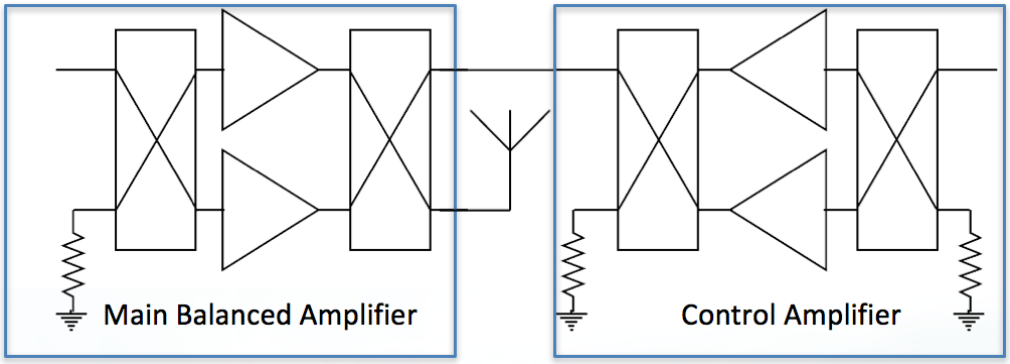


Figure 30: Schéma de principe du Double Balanced LMBA

La figures 31 montre les performances de ce nouvel amplificateur. Elles sont sensiblement identiques à celles du LMBA précédent. La figure 32 compare le rendement des deux architectures soumises à un VSWR de 3:1, avec la phase qui varie de 0 à 330 degrés. La PAE de l'architecture Double Balanced est en rouge, celle du LMBA classique en bleu. Les croix montrent les courbes à puissance back-off et les ronds à puissance maximale. Comme prévu, l'architecture Double Balanced montre une variation de PAE minime, comparée à celle du LMBA classique. Sur la figure 33 nous voyons encore une fois les impédances vues par les amplificateurs de branche en back-off à gauche et à puissance maximale à droite. Celles-ci sont parfaitement superposées, montrant que le système est de nouveau équilibré. Ainsi, l'architecture Double Balanced LMBA présente une robustesse à la désadaptation d'impédance.

La figure 34 montre le layout du Double Balanced LMBA. Il s'agit d'un circuit multi-technologies, ou tous les circuits passifs sont réalisés sur un substrat BT. Les différents transistors CMOS viennent se brancher directement sur le substrat, aux endroits indiqués par des carrés rouge (amplificateur principal) et bleu (amplificateur de contrôle).

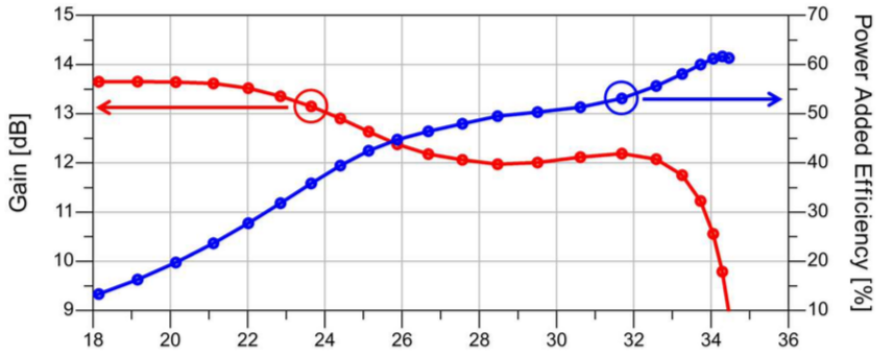


Figure 31: Performances du Double Balanced LMBA. En rouge le gain et en bleu la PAE.

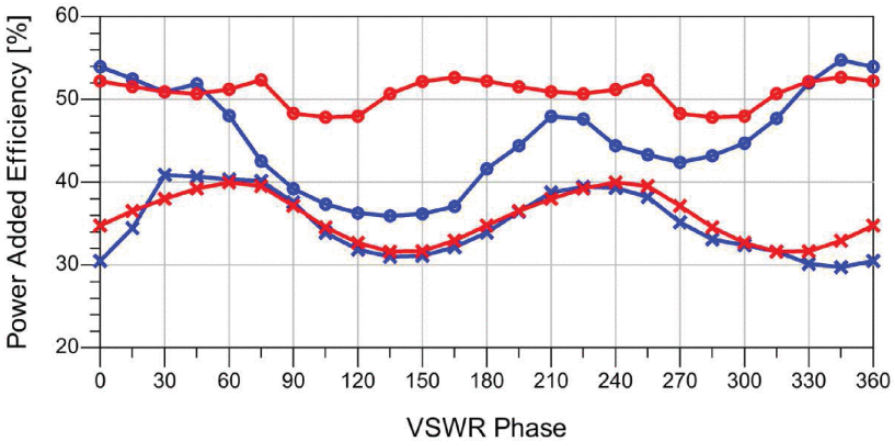


Figure 32: Le rendement du LMBA classique (en bleu) et du Double Balanced LMBA en rouge, à puissance back-off avec les marqueurs X et à puissance maximale avec les marqueurs ronds.

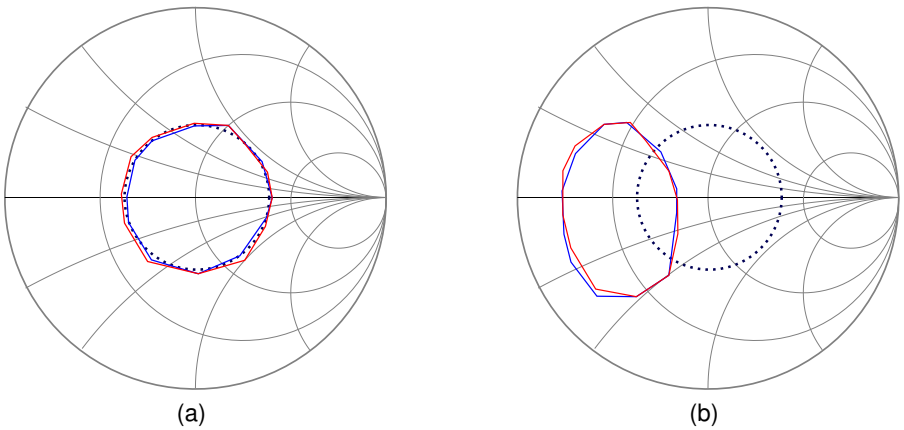


Figure 33: En rouge et bleu les impédances vue par chaque amplificateur de branche et en pointillés noirs l'impédance présentée à la sortie. A gauche à la puissance back-off, quand l'amplificateur de contrôle est éteint, et à droite à puissance maximale.

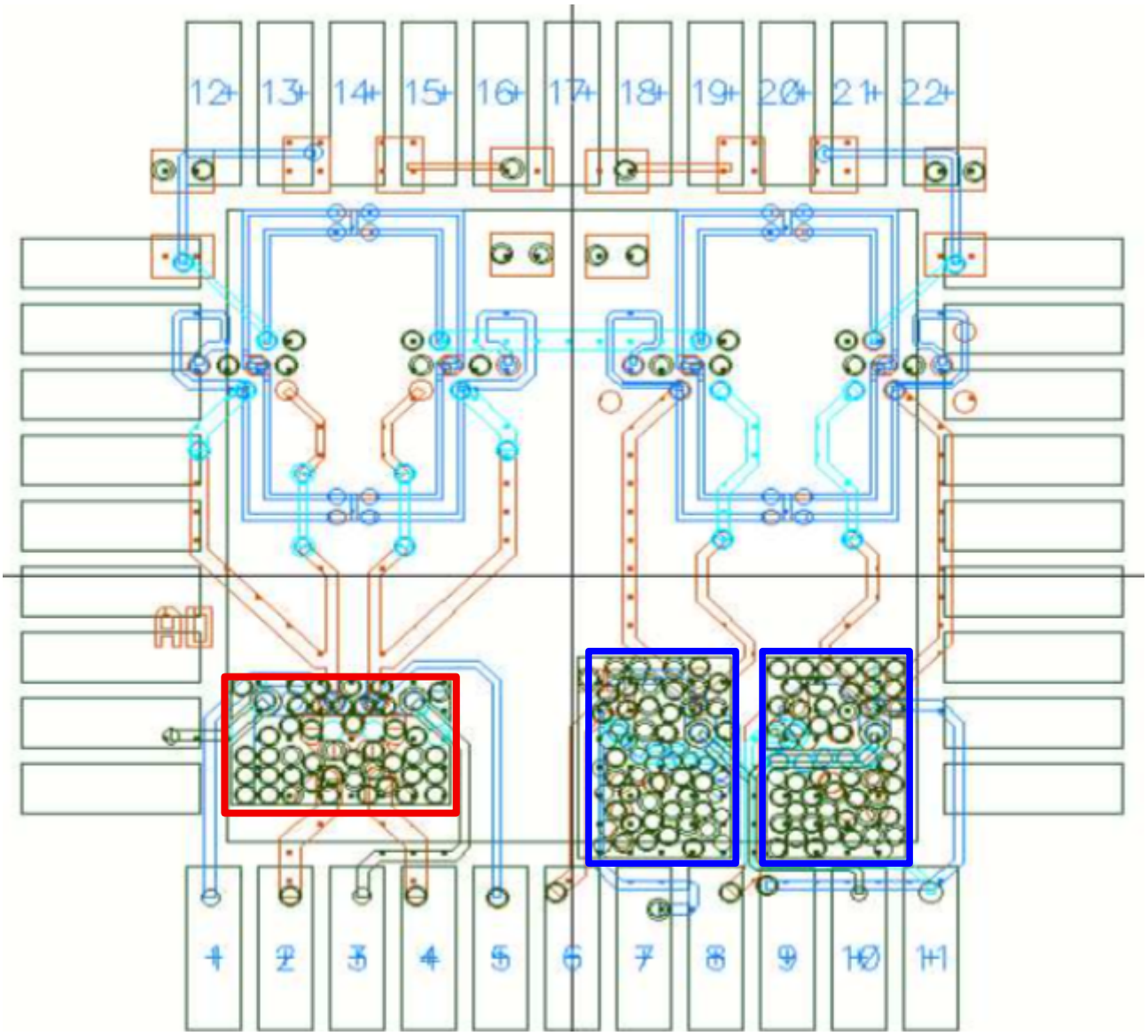


Figure 34: Layout du Double Balanced LMBA. On voit sur cette figure le substrat en technologie BT, qui contient les réseaux d'adaptation au drain des transistors et le coupleur de sortie.

Appendix A

K Band MMIC Amplifiers in Win 0.10 μm pHEMT technology

In chapter 4 we presented the layout and simulations of the MMIC Doherty-like 30 dBm K band LMBA. Here we present the layout and electromagnetic simulation results of the balanced amplifier and single-ended amplifier MMICs.

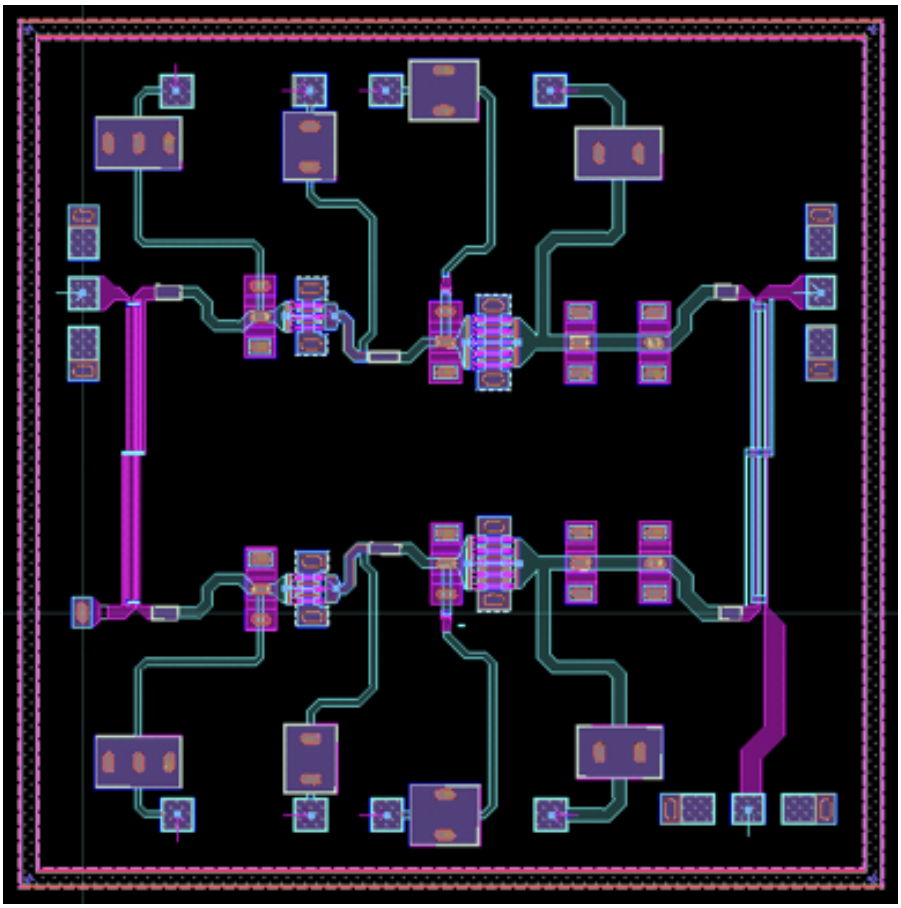


Figure 1: Layout of the GaAS K Band Balanced Amplifier

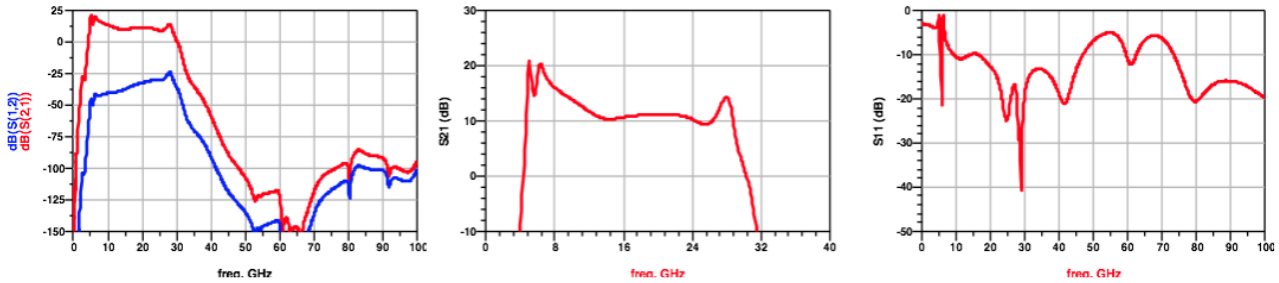


Figure 2: S Parameters extraced from the electromagnetic simulation of the K band 30 dBm Balanced Amplifier MMIC.

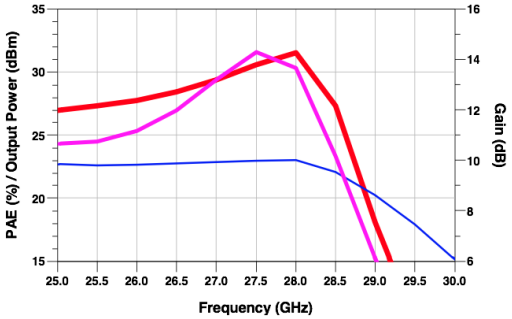


Figure 3: Electromagnetic simulation results of the K band 30 dBm Balanced Amplifier MMIC. The blue, red and pink curves correspond to the peak output power, PAE and Gain respectively.

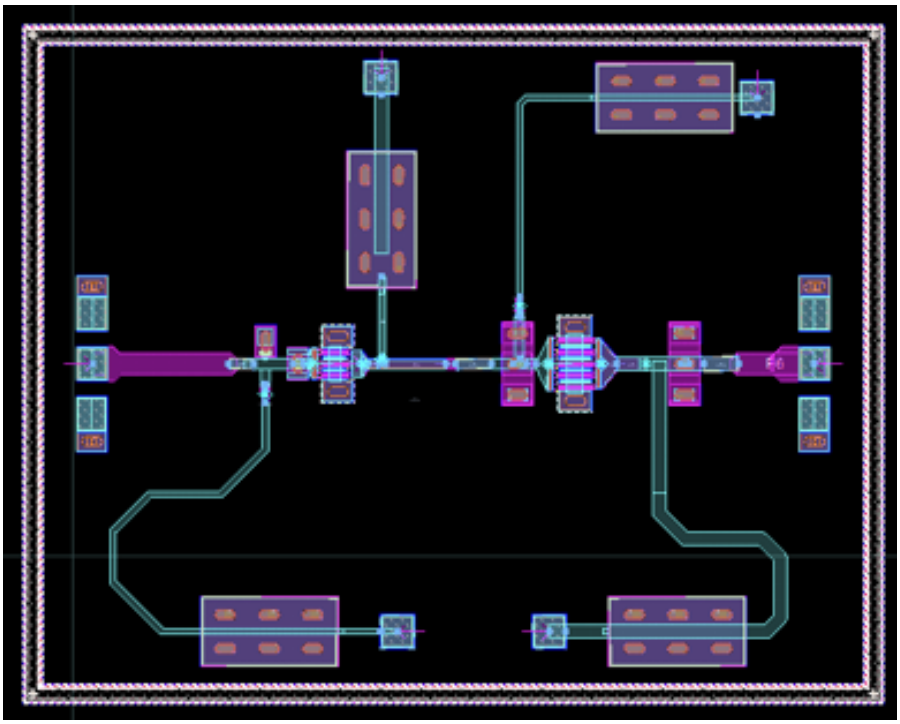
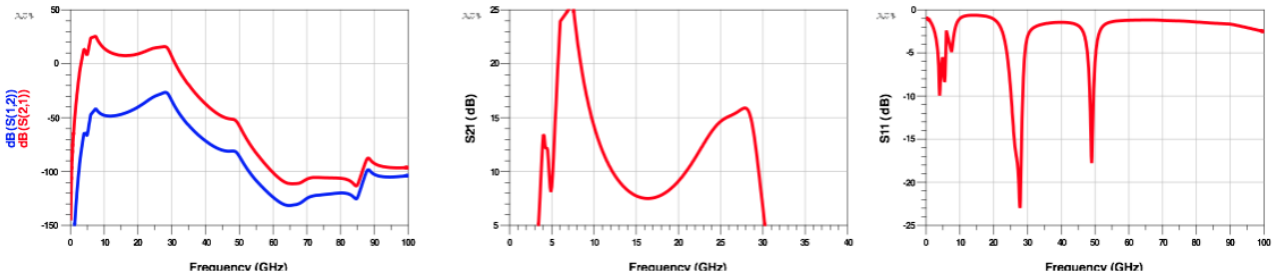
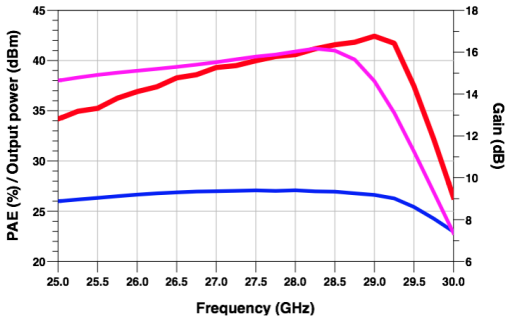


Figure 4: Layout of the GaAS K Band Single-ended Amplifier



(a)

Figure 5: S Parameters extracted from the electromagnetic simulation of the K band 30 dBm single-ended amplifier MMIC.



(a)

Figure 6: Electromagnetic simulation results of the K band 30 dBm single-ended amplifier MMIC. The blue, red and pink curves correspond to the peak output power, PAE and Gain respectively.

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