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Design of a Bidirectional on-board charger and a DC-DC converter for Low Voltage Battery in Electric Vehicles

Thèse de doctorat de l'université Paris-Saclay

École doctorale n°575 Electrical, Optical, Bio: PHYSICS AND ENGINEERING (EOBE)

Spécialité de doctorat: Génie électrique

Unité de recherche : Université Paris-Saclay, CentraleSupélec, CNRS, Laboratoire de Génie Electrique et Electronique de Paris, 91192, Gif-sur-Yvette, France.

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Thèse présentée et soutenue en visioconférence totale
le 3 décembre 2020, par

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Invité

Titre : Étude et réalisation d'un convertisseur combinant DC/DC et on-board charger pour véhicule électrique

Mots clés : chargeur embarqué, convertisseur DC-DC réversible, commutation douce, convertisseur à trois portes, transformateur planar.

Résumé : Cette thèse porte sur l'intégration du convertisseur DC-DC entre les batteries haute et basse tension (400V / 14V), avec un chargeur embarqué monophasé présent dans l'architecture du véhicule électrique. Dans cette intégration, les deux convertisseurs sont bidirectionnels et l'isolation galvanique est nécessaire entre les trois sources d'énergie. Dans une première partie de cette étude, nous sommes focalisés sur le développement d'un convertisseur DC-DC à trois ponts.

Le convertisseur DC-DC proposé est un convertisseur bidirectionnel alimenté en courant à résonance parallèle permettant de réaliser des commutations à zéro de tension sur toute la plage de puissance. Grâce à la « recopie de tension », le dimensionnement du transformateur permet la réalisation d'une

structure beaucoup plus compacte par rapport à d'autres convertisseurs à résonance. Dans la deuxième partie de ce travail, les caractéristiques du convertisseur sont étudiées afin d'optimiser la stratégie de commande et de fonctionnement. Le développement d'un transformateur planar est réalisé en respectant les normes pour les véhicules électriques et pour minimiser les inductances de fuite. L'étude de la répartition de courant dans les couches connectées en parallèle est faite de façon à éviter la présence de points chauds en haute fréquence. Le prototype et les résultats finaux sont présentés pour valider le convertisseur à 3 ponts. Après avoir analysé les résultats, quelques propositions sont faites pour améliorer les résultats dans les futurs travaux.

Title : Design of a bidirectional on-board charger and a DC-DC converter for Low Voltage Battery in Electric Vehicles

Keywords : OBC, DC-DC bidirectional converter, soft-switching, three-port converter, planar transformer.

Abstract: This dissertation focuses on the integration of two power electronic converters present in the electric vehicle (EV) architecture – the DC-DC converter interfacing the high and low voltage batteries (400V/14V) and the onboard charger (OBC). A three-port current-fed parallel resonant topology with zero voltage switching capability is developed. The converter allows bidirectional power flow between the three energy sources with high efficiency in both conversion modes, DC-DC and OBC while ensuring galvanic isolation.

A compact three-winding planar transformer is designed based on EV industry requirements, emphasizing the minimization of leakage inductances. In this design, the unequal current

sharing phenomenon between parallel-connected layers is addressed to ensure a homogeneous current distribution and eliminate the risks of thermal hotspots formation.

A 7kW experimental prototype has been constructed and tested, validating the analysis and operation of the proposed topology. Some suggestions and propositions are provided for future work aiming at efficiency improvement of the converter.

À mes parents, Francisco et Cassiana,
et à mon frère Kelvin

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Résumé en français

1- Introduction générale

L'industrie automobile des véhicules électriques est en constante évolution. L'architecture de la chaîne de traction est très similaire d'un constructeur à l'autre. Elle comporte normalement : une batterie haute tension pour alimenter l'onduleur triphasé qui pilote le moteur électrique à aimants permanents ou à rotor bobiné, une batterie basse tension pour alimenter les équipements embarqués, un convertisseur DC-DC isolé pour alimenter la batterie basse tension à partir de la batterie de propulsion. Le chargeur de la batterie haute tension peut être embarqué ou non au véhicule électrique en fonction de sa puissance, comme montre la Figure R 1-a. Lorsque le chargeur n'est pas embarqué, la charge est plus rapide, mais il est nécessaire d'avoir une station de charge dédiée est alors nécessaire. Les chargeurs embarqués présentent certains avantages, comme la possibilité d'utiliser les réseaux électriques conventionnels.

Les convertisseurs de puissance à l'intérieur du véhicule doivent être placés de manière stratégique afin de permettre leur refroidissement. Leur encombrement et leur coût doivent être réduits au minimum. Le développement d'un convertisseur unique intégrant plusieurs fonctions capables d'assurer les hautes performances de conversion requises tout en utilisant moins de composants permettrait d'envisager une réduction des coûts, une implantation facilitée à l'intérieur du véhicule et un refroidissement plus efficace. Le convertisseur devrait aussi assurer la réversibilité.

Cette thèse porte sur l'intégration du convertisseur DC-DC- entre les batteries HT et BT, et d'un chargeur embarqué en un convertisseur unique. Dans cette intégration, la première idée est de réduire le nombre de composants en partageant les structures existantes. Le principal défi sera de garder une efficacité élevée pour les deux fonctions mises en œuvre. Pour justifier le choix d'intégrer ces deux convertisseurs en particulier, malgré leur différence en courant et en puissance, nous pouvons partir des structures simplifiées proposées à la Figure R 1-b. Le chargeur peut être considéré comme l'association de deux étages de conversion: une partie AC-DC avec un correcteur de facteur de puissance (PFC) suivi d'un convertisseur DC-DC isolé similaire à celui utilisé pour la charge de la batterie BT. Ce convertisseur DC-DC peut-être un convertisseur à résonance comme le LLC, LC série, ou un convertisseur à déphasage comme le DAB (Dual-Active Bridge), un phase-shift ou un pont complet.

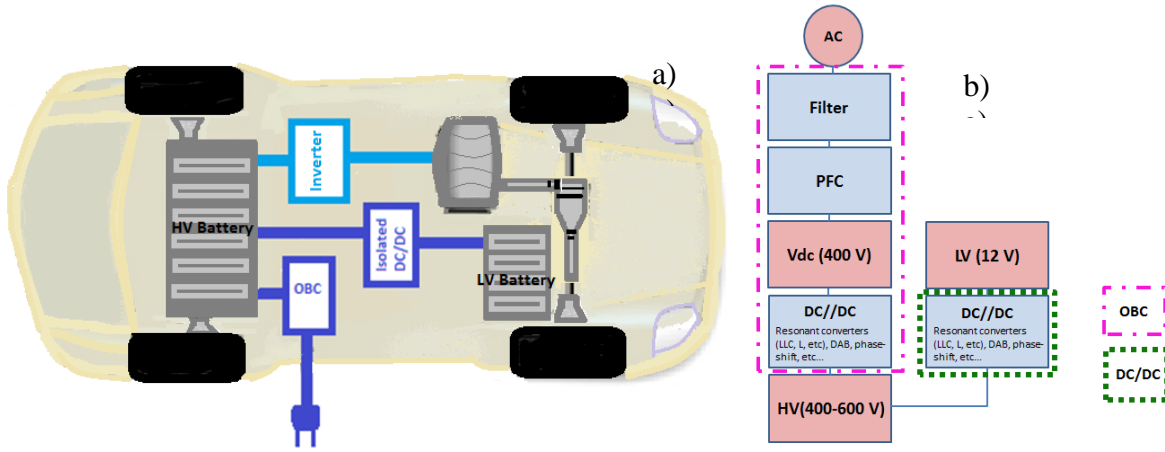


Figure R 1 : a) Architecture typique d'un véhicule électrique avec les principaux convertisseurs de puissance embarqués: l'onduleur, le chargeur OBC, et le convertisseur DC-DC b) Représentation schématique des étages de conversion entre la batterie HT, la batterie BT, le DC/DC et le réseau électrique.

Pour recharger la batterie BT, une puissance comprise entre 1 kW et 3.5 kW pourrait être sollicitée par les constructeurs. Pour la recharge de la batterie HV, la plage de puissance est définie par les normes et varie si le chargeur est connecté à un réseau monophasé ou triphasé, comme montre le Tableau R 1.

Classif.	Type	Puissance	Temps charg.	Station
Niveau 1	On-board (1Ø) 120 Vac (USA) 230 Vac (Eur)	1.4 kW (12 A) 1.9 kW (20 A)	4- 11 hours 11- 30 hours	Home or office
Niveau 2	On-board (1 or 3Ø) 240 Vac (USA) 400 Vac (Eur)	4 kW (17 A) 8 kW (32 A) 19.2 kW (80 A)	1-4 hours 2-6 hours 2-3 hours	Private or public stations
Niveau 3	Off-board (1 or 3Ø) Vac or Vdc supply	> 50 kW	< 1 hour	Dedicated

Tableau R 1: Classification des chargeurs pour les véhicules électriques. Sources:[2] and [5].

Durant cette thèse, nous nous sommes focalisés sur le développement d'un convertisseur DC-DC isolé à trois entrées/sorties pour le transfert d'énergie entre les deux batteries et la sortie du PFC. Les caractéristiques visées sont présentées par le Tableau R 2.

	Réseau AC	Batteries	HV	LV
Tension (VRMS)	85 – 265	Plage de tension	240 - 480 V	12 - 16 V
Fréquence (Hz)	50 - 60	Tension Nom.	450 V	14 V
Pmax (kW)	7 kW	P (kW) (+/-)	0 - 7 kW	0 - 3.5 kW
Imax (ARMS)	32	I _{DC} max (A)	17.5 A	250 A

Tableau R 2:Caractéristiques électriques du convertisseur combinant OBC et DC/DC.

Afin d'assurer de bonnes performances au convertisseur DC-DC à trois entrées/sorties, il est nécessaire de minimiser avant tout : les pertes par conduction du côté basse tension, les ondulations de courant, les pertes par commutations (pour permettre d'augmenter la fréquence de découpage et gagner en compacité). Les commutations à zéro de tension sont requises pour assurer un bon rendement et de meilleures caractéristiques en CEM.

Dans le Chapitre 2, le convertisseur conventionnel « Trois ponts actifs » est étudié en vue de satisfaire à notre cahier des charges.

Au chapitre 3, nous proposons un convertisseur alimenté en courant, basé sur la résonance parallèle en vue de réaliser des commutations à zéro de tension sur toute la plage de fonctionnement et dans le trois modes d'opération : OBC, DC/DC et OBC et DC/DC simultanément.

Le chapitre 4 présente le développement d'un transformateur planar à trois enroulements pour le convertisseur choisi. Comme le convertisseur permet trois modes différents d'opération, une analyse plus détaillée des pertes de puissance est également proposée. Pour cela, nous avons réalisé une étude analytique du partage de courant entre bobines parallèles et un modèle équivalent pour représenter les éléments parasites qui dépendent de la fréquence.

Le dimensionnement complet du convertisseur est présenté au chapitre 5. Ce chapitre propose aussi un modèle plus réaliste du convertisseur avec des éléments parasites affectant la résonance, et confronté aux résultats expérimentaux obtenus.

Au chapitre 6, nous considérons l'intérêt d'un convertisseur DC-DC non isolé connecté en série avec le convertisseur à résonance étudié aux chapitres précédents. Nous estimons également le rendement global pour chaque mode de fonctionnement.

2- Analyse du convertisseur à trois ponts actifs pour l'intégration de l'OBC et du DC/DC

Dans ce chapitre, nous étudions l'une des solutions possibles pour intégrer les convertisseurs OBC et LDC dans un convertisseur à trois ponts actifs. Les trois sources (le bus de tension V_{dc} du PFC, la batterie haute tension et la batterie auxiliaire basse tension) sont connectées à des ponts complets partageant le même transformateur, comme illustré à la Figure R 2-a.

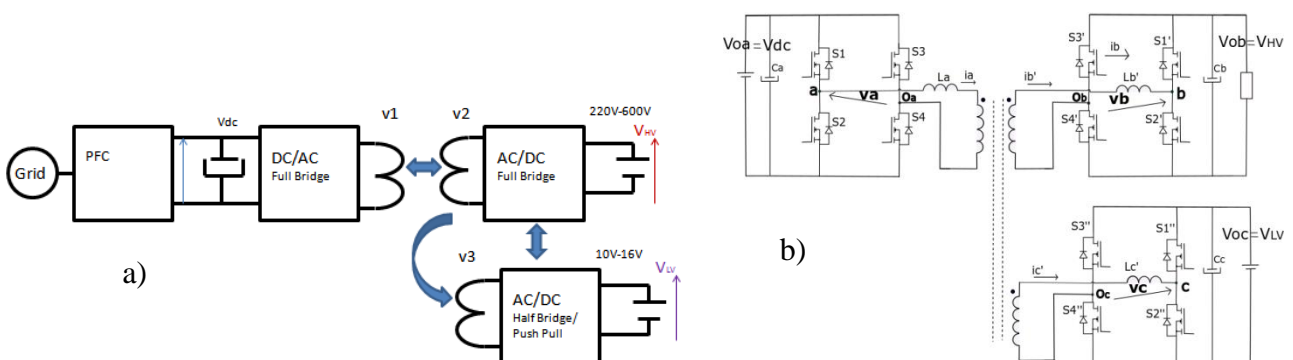


Figure R 2: a) Le convertisseur intégrant l'OBC et le DC/DC. b) Réalisation à partir de 3 ponts actifs.

Dans l'hypothèse du réglage de transfert de puissance par déphasage, ce convertisseur présente des limitations pour opérer en ZVS pour une faible valeur de charge et une large plage de variation de tension. Ces contraintes sont pourtant imposées à l'OBC et au DC-DC. Cette limitation peut être démontrée avec la représentation en circuit en π , Figure R 3, proposée en [5]. Considérons le fonctionnement illustré en Figure R 3-D. Lors de la commutation d'un transistor, celle-ci s'effectue à zéro de tension à condition que les capacités parasites puissent se charger ou se décharger grâce à un sens adéquat des courants. Par exemple, pour un transfert d'énergie de A vers B (OBC) et de B vers C (DC-DC), cela se traduit par :

$$V_{oA} > V_{oB} N_{AB} > V_{oC} (N_{BC} N_{AB}) \quad (1)$$

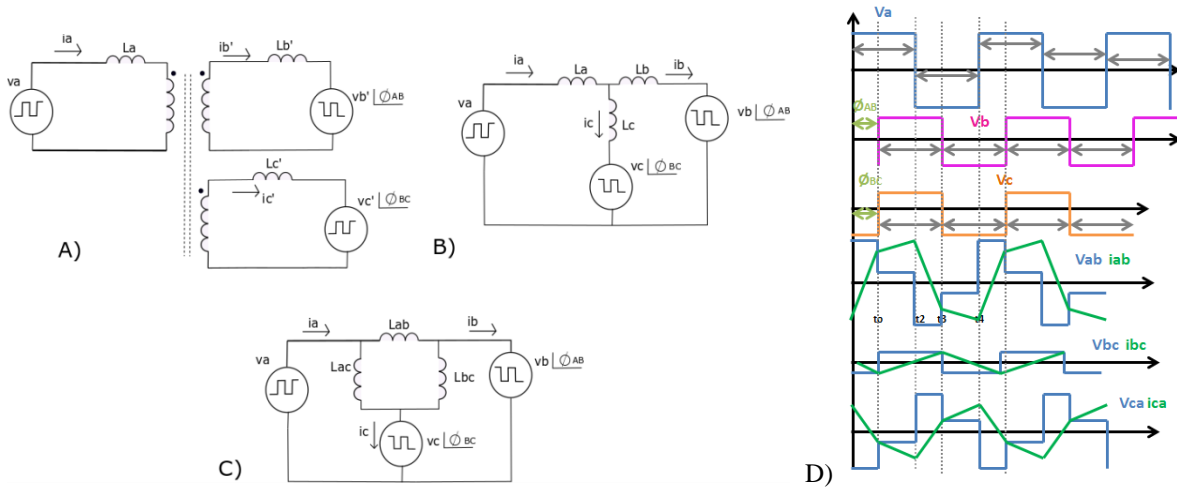


Figure R 3: a) Circuit équivalent pour les 3 ponts actifs. b) Circuit équivalent simplifié c) Circuit équivalent en π . D) Représentation des tensions et courants sur le circuit équivalent en π , pendant le transfert d'énergie du pont A vers les ponts B et C.

Les tensions imposées aux enroulements du transformateur peuvent être représentées par leurs harmoniques:

$$v_a(t) = \sum_{N=1}^{\infty} \frac{4 V_a}{N \pi} \sin(N \pi D_a) e^{i(N \omega t)}$$

$$v_b(t) = \sum_{N=1}^{\infty} \frac{4 V_b}{N \pi} \sin(N \pi D_b) e^{i(N \omega t + \phi_{AB})}$$

$$v_c(t) = \sum_{N=1}^{\infty} \frac{4 V_c}{N \pi} \sin(N \pi D_c) e^{i(N \omega t + \phi_{BC} + \phi_{AB})}$$

À partir des tensions appliquées à chaque enroulement, les courants peuvent aussi être déterminés, les puissances transférées également (Annexes 2.4.1):

$$i_{ab}(\omega t) = \begin{cases} -I_{ab0} + \frac{(V_a+V_b)}{\omega_s L_{ab}} \omega t, & 0 < \omega t < \phi_{AB} \\ I_{ab t_0} + \frac{(V_a-V_b)}{\omega_s L_{ab}} (\omega t - \phi_{AB}), & \phi_{AB} < \omega t < \pi \\ I_{ab0} - \frac{(V_a+V_b)}{\omega_s L_{ab}} (\omega t - \pi), & \pi < \omega t < \pi + \phi_{AB} \\ -I_{ab t_0} - \frac{(V_a-V_b)}{\omega_s L_{ab}} (\omega t - \pi - \phi_{AB}), & \pi + \phi_{AB} < \omega t < 2\pi \end{cases}$$

$$P_{AB} = \frac{V_a V_b}{\omega_s L_{ab}} \phi_{AB} \left(\frac{\pi - |\phi_{AB}|}{\pi} \right)$$

$$P_{BC} = \frac{V_b V_c}{\omega_s L_{bc}} \phi_{AB} \left(\frac{\pi - |\phi_{BC}|}{\pi} \right)$$

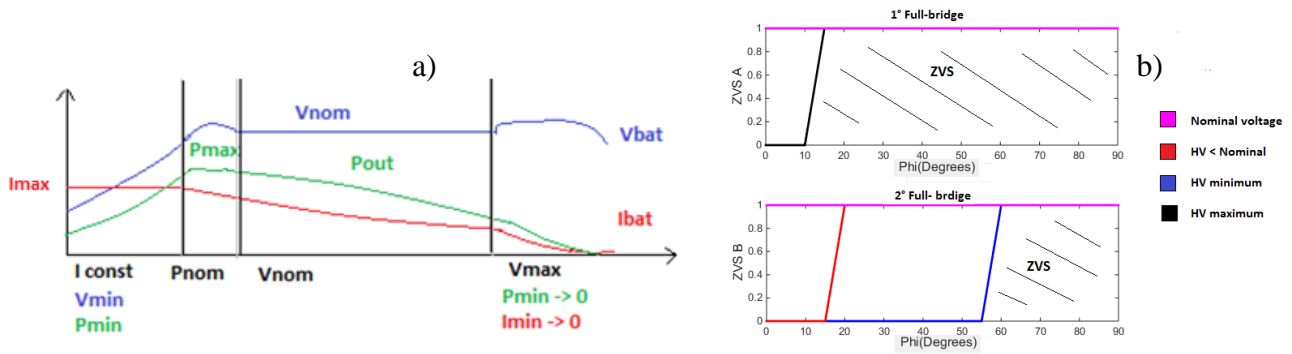
$$P_{AC} = \frac{V_a V_c}{\omega_s L_{ac}} (\phi_{AB} - \phi_{BC}) \left(\frac{\pi - |\phi_{AB} - \phi_{BC}|}{\pi} \right)$$

Pour vérifier que les limitations du convertisseur ne sont pas contradictoires avec nos exigences pour les applications OBC et LDC, nous devons aller plus avant dans la conception du convertisseur. Tout d'abord, la conception consiste à trouver l'inductance minimale pour la puissance maximale et la meilleure relation entre le gain de tension et les régions de commutation de tension nulle dans l'équation (1). Dans la Figure R 3-D, l'analyse de la commutation de tension nulle (vérifier la section 2.4.1) dans les trois ponts complets aboutit à 4 conditions:

$$\frac{(\pi - 2\phi_{AB})}{\pi} < \frac{V_{oA}}{V_{oB} N_{AB}} < \frac{\pi}{(\pi - 2\phi_{AB})} \quad (2)$$

$$\frac{(\pi - 3\phi_{BC})}{(\pi + \phi_{BC})} \leq \frac{V_{oA}}{V_{oC} N_{BC} N_{AB}} \leq \frac{(\pi - 2\phi_{BC})}{\pi} \quad (3)$$

Si nous considérons le processus de charge de la batterie se déroulant en quatre phases, comme présenté dans la Figure R 4-a, nous voyons les points à fonctionnement critique du convertisseur où le ZVS ne se produit pas, à la première et à la dernière étapes de la Figure R 4-a. Avec les conditions (2) - (3), la région ZVS peut être représentée pour chaque pont, sur la Figure R 4-b. À la tension nominale, les conditions ZVS sont présentes pour la charge de la batterie. En mode buck, correspondant à la 1^o phase de la charge de la batterie, les conditions sont dégradées dans le deuxième pont complet, connecté à la batterie HV, limitant le courant minimum. En mode boost, à faible puissance, les conditions ZVS n'existent plus dans le premier pont connecté à la tension d'entrée, V_{oa} .



Afin d'étendre la zone de commutations douces, nous pouvons aussi mettre en œuvre le réglage des rapports cycliques, comme cela a été proposé par certains auteurs en [8] - [9]. Sur la Figure R 5-a, nous illustrons la variation des rapports cycliques dans le premier et le deuxième pont (D_a et D_b) pour améliorer les conditions ZVS pendant le mode de fonctionnement OBC. La même condition en (1) est maintenue et les temps de commutation sont définis comme:

$$\left\{ \begin{array}{l} \theta_{0.5} = \pi - \pi D_a \\ \theta_0 = \emptyset_{AB} \\ \theta_1 = \emptyset_{AB} + \pi - \pi D_b \\ \theta_2 = \pi \\ \theta_3 = \pi + \emptyset_{AB} \\ \theta_{3.5} = 2\pi - \pi D_a \\ \theta_4 = \pi + \emptyset_{AB} - \pi D_b \\ \theta_5 = 2\pi \end{array} \right.$$

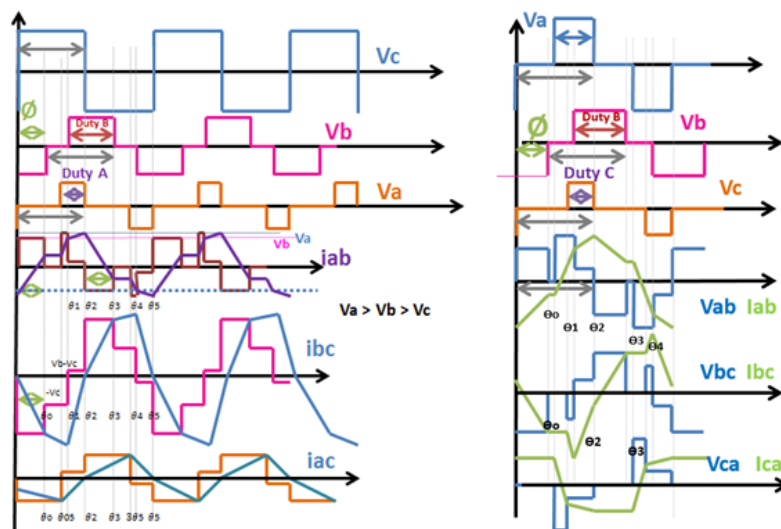


Figure R 5: a) Tensions et courants appliqués au circuit équivalent avec variation de rapport cyclique pour le premier et deuxième ponts, D_a et D_b . b) Réglage des rapports D_a , D_b et D_c .

Pour chaque transition de tension, nous pouvons écrire le courant équivalent, comme par exemple :

$$i_{ab}(\omega t) = \begin{cases} -I_{ab0} + \frac{V_b}{\omega_s L_{ab}} \omega t, & 0 < \omega t < \theta_o \\ I_{ab}(\theta_o), & \theta_o < \omega t < \theta_{0.5} \\ I_{ab}(\theta_o) + \frac{V_a}{\omega_s L_{ab}} (\omega t - \theta_{0.5}), & \theta_{0.5} < \omega t < \theta_1 \\ I_{ab}(\theta_1) + \frac{(V_a - V_b)}{\omega_s L_{ab}} (\omega t - \theta_1), & \theta_1 < \omega t < \theta_2 \\ I_{ab0} - \frac{V_b}{\omega_s L_{ab}} (\omega t - \theta_2), & \theta_2 < \omega t < \theta_3 \\ I_{ab}(\theta_3), & \theta_3 < \omega t < \theta_{3.5} \\ -I_{ab}(\theta_o) - \frac{V_a}{\omega_s L_{ab}} (\omega t - \theta_{3.5}), & \theta_{3.5} < \omega t < \theta_4 \\ -I_{ab}(\theta_1) - \frac{(V_a - V_b)}{\omega_s L_{ab}} (\omega t - \theta_4), & \theta_4 < \omega t < \theta_5 \end{cases}$$

$$I_{ab}(0) = -\frac{V_a \pi D_a}{2L_{ab}} + \frac{V_b}{2L_{ab}} (-2\phi_{AB} + \pi D_b)$$

Les expressions des courants i_{bc} et i_{ca} nous permettent de vérifier les conditions pour les commutations à zéro de tension :

$$\begin{aligned} i_a(0) < 0 \text{ et } i_a(\theta_{0.5}) < 0 \\ i_b(\theta_o) < 0 \text{ et } i_b(\theta_1) < 0 \\ i_c(0) < 0 \end{aligned}$$

Ces conditions sont valables pour le mode Boost avec faible puissance à la sortie:

$$\phi_{AB} \leq \pi D_b \leq \pi - \phi_{AB} \quad \text{or} \quad \phi_{AB} \leq \pi D_a \leq \pi - \phi_{AB}$$

$$\frac{(\pi D_b - 2\phi_{AB})}{2\pi D_a} < \frac{V_{oA}}{V_{oB} N_{AB}} < \frac{(\pi D_b - 4\phi_{AB})}{\pi D_a} \quad (4)$$

$$\frac{(2\pi D_a - \pi)}{\pi D_a} \leq \frac{V_{oA}}{V_{oC} (N_{BC} N_{AB})} < \frac{\pi}{\pi D_a} \quad (5)$$

$$\frac{N_{AB} N_{BC} V_{oC} (4\phi_{AB} - \pi)}{\pi D_b} \leq N_{AB} V_{oB} < \frac{V_{oA} (2\phi_{AB} + 3\pi D_a - 2\pi D_b)}{\pi D_b - 4\phi_{AB}} \quad (6)$$

La Figure R 6 montre la puissance de sortie et le courant RMS dans les enroulements avec le réglage du rapport cyclique du pont de sortie en mode boost. L'énergie de circulation est augmentée et permet d'obtenir une commutation douce pour les petits angles de déphasage. La Figure R 7-a montre la variation de puissance en fonction des rapports cycliques des deux ponts, D_a et D_b . Le réglage de D_a permet une amélioration dans le mode Buck du deuxième pont B, et le réglage de D_b permet une amélioration pendant le mode boost du pont A. Les conditions de ZVS pendant les transitions de tension sont présentées à Figure R 7-b. La meilleure combinaison du contrôle des différents rapports cycliques permettant d'augmenter la plage des commutations douces ou de réduire le courant de circulation.

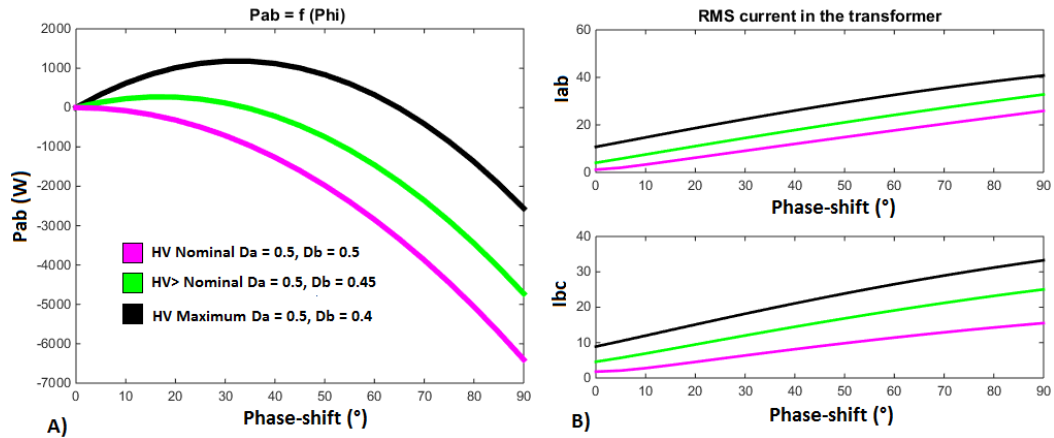


Figure R 6: a) Puissance de sortie en fonction du déphasage et rapport cyclique (Db) b) Courant RMS entre les enroulements.

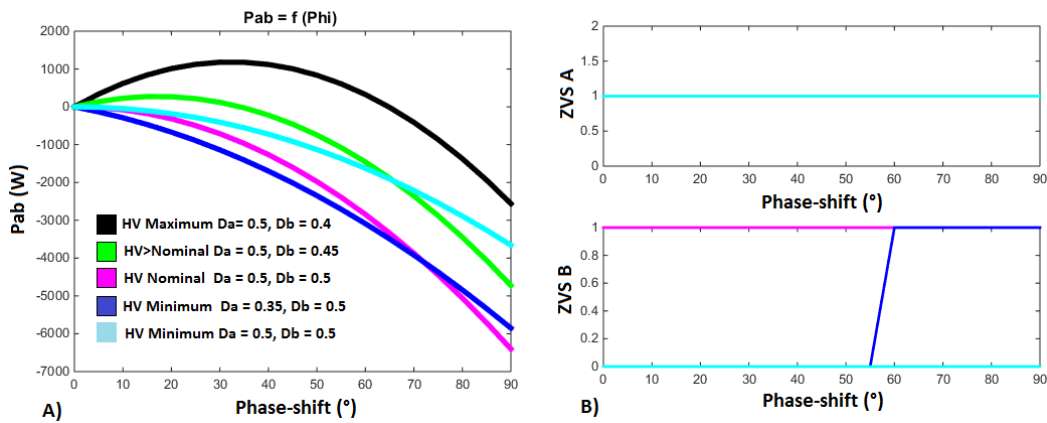


Figure R 7: a) Puissance de sortie en fonction du déphasage et rapport cyclique (Db et Da) pour améliorer les modes buck et boost b) Région avec conditions ZVS pour le ponts A et B.



Figure R 8: a) $V_{oB} = 600\text{ V}$, $V_{oA} = 450\text{ V}$ avec commutation dure sur le pont A. b) Réglage du rapport cyclique D_b pour obtenir des commutations douces sur le pont A.

Compte tenu des formes d'onde présentées dans la Figure R 5-b, les trois différents rapports cycliques, (D_a , D_b et D_c), et angles de déphasage, (ϕ_{AB} , ϕ_{BC}), sont pris en compte dans l'analyse, pour l'optimisation du fonctionnement de l'OBC. Les conditions pour le ZVS sont représentées par les équations (6), (7), (8) et (9). Ces équations sont résumées sur la Figure R 9, où les régions de commutations douces sont comparées en mode de fonctionnement boost. Sans le réglage du rapport cyclique, le pont A perd les conditions nécessaires lorsque le flux de puissance est diminué (ligne bleue). L'ajustement

du rapport cyclique sur le pont B permet une amélioration (ligne rouge). Lorsque les rapports cycliques des ponts B et C, sont réglés ensemble (D_b et D_c), les résultats sont encore améliorés.

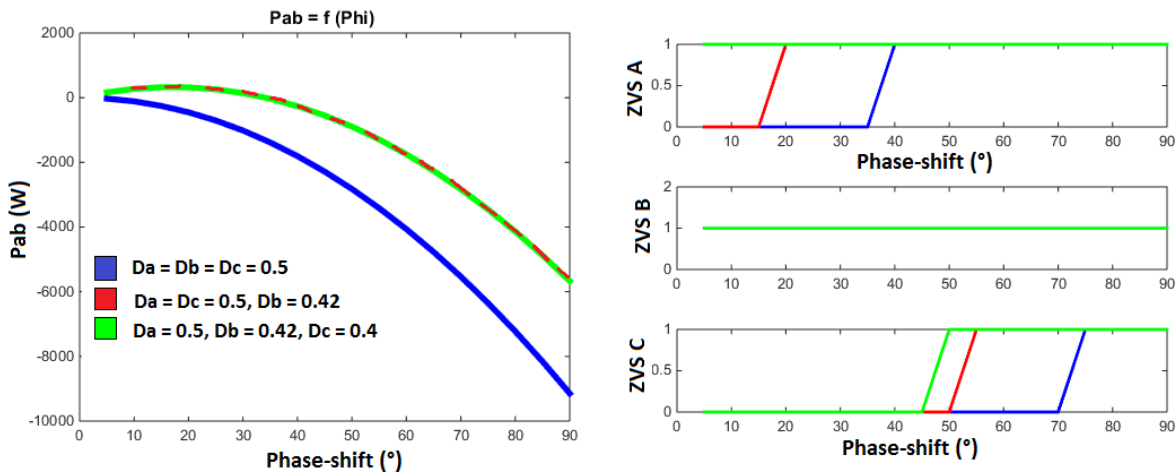


Figure R 9: a) Transfert de puissance entre le premier et le deuxième ponts b) conditions pour les commutations à zéro de tension pendant le mode Boost. Avec le réglage des rapports cycliques D_b et D_c , les communications douces peuvent être assurées dans le pont A, même à faible charge.

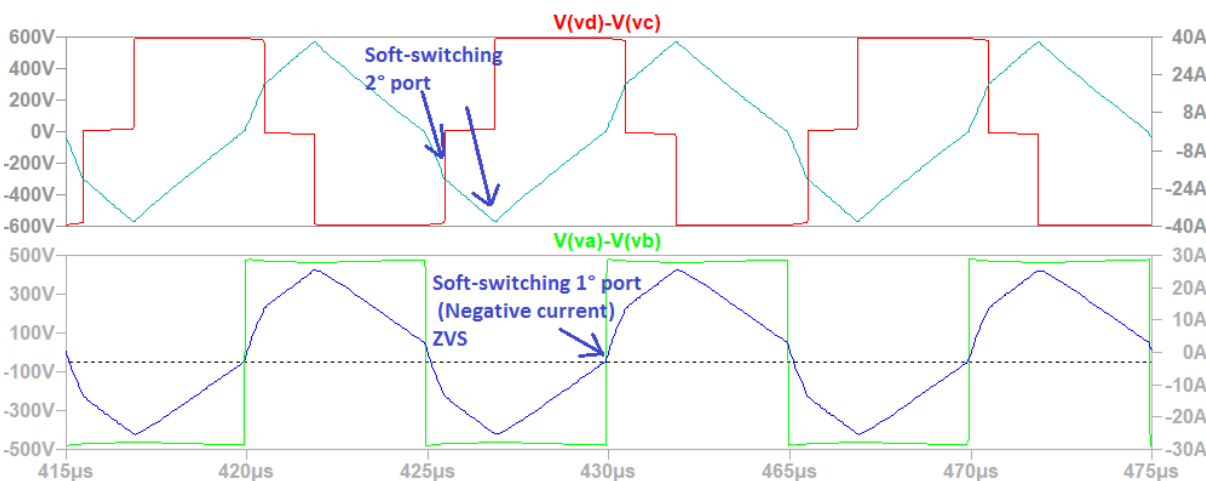


Figure R 10: Rapport cyclique modifié pour étendre la zone des commutations à zéro de tension lorsque la tension de sortie est élevée et à faible charge. $D_a = 50\%$, $D_b = 40\%$ and $D_c = 45\%$.

Le contrôle supplémentaire des rapports cycliques permet d'étendre la région de fonctionnement à commutation douces, mais il augmente le courant RMS du transformateur ou l'énergie de circulation. Nous étudions aussi l'ajout d'inductances parallèles avec le transformateur pour stocker de l'énergie utile aux commutations ZVS, comme le montre la Figure R 11. Dans ce concept, le rapport cyclique peut être maintenu constant à 50% ou être utilisé pour diminuer le courant de circulation du côté basse tension (Pont C), au lieu de fournir les conditions minimales requises pour le ZVS. Les résultats sont montrés sur la Figure R 12.

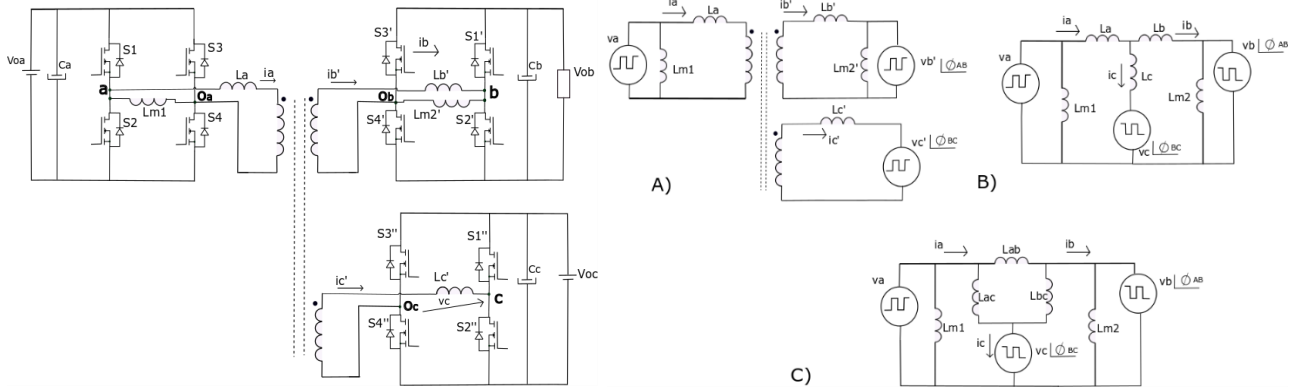


Figure R 11: a) Le convertisseur avec trois ponts actifs et l'ajout des inductances supplémentaires b) Circuit équivalent en π avec $Lm1$ et $Lm2$ pour l'analyse des conditions assurant les commutations à zéro de tension.

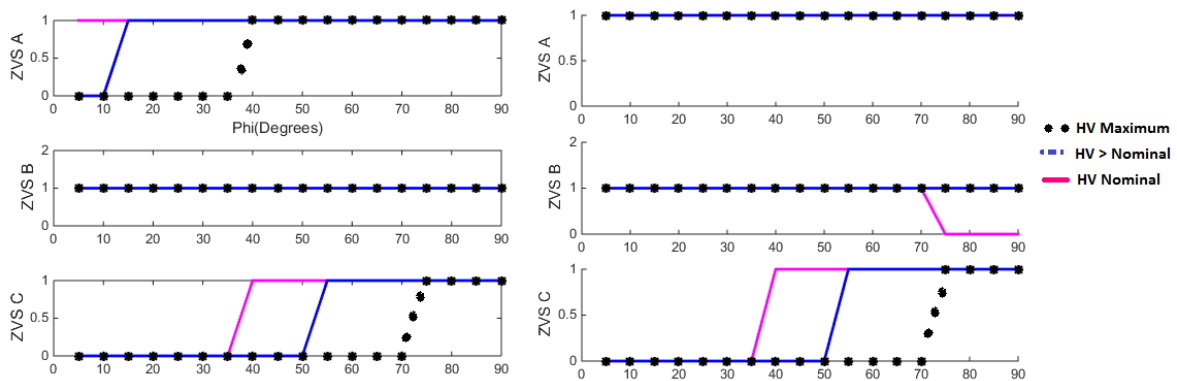


Figure R 12: Les zones avec les conditions pour le ZVS pendant le fonctionnement en mode Boost de l'OBC. a) Sans les inductances parallèles, $Lm1 = Lm2 = \infty$. b) Avec des inductances parallèles $Lm1 = Lm2 = 60 \mu H$.

La première solution, sans les inductances parallèles supplémentaires, élargit la zone de fonctionnement à commutation douce uniquement en modifiant le rapport cyclique des ponts, mais cette solution ne suffit pas pour une puissance inférieure à 1kW avec ZVS. Il permet cependant les commutations à zéro de courant, ZCS (Zero Current Switching). La solution avec des inductances parallèles étend la région de fonctionnement ZVS du convertisseur, y compris lors de la phase critique du processus de charge de la batterie, à un gain de tension élevé et une faible puissance de sortie. Néanmoins, il augmente le courant de circulation entre les ponts. Par conséquent, une attention particulière doit être prise pour comparer l'impact d'un courant RMS plus important générant des pertes de conduction plus élevées et le gain obtenu avec la réduction des pertes de puissance par commutation.

Une autre idée pour intégrer l'OBC et le LDC consiste à utiliser le convertisseur à trois ponts avec des éléments résonnants associés au contrôle de déphasage [5]. Les convertisseurs résonnants présentent quelques avantages, tels qu'une réduction des pertes par commutation, et une réduction de volume en raison de la possibilité d'augmenter la fréquence de découpage. Alternativement, nous pouvons penser à développer des convertisseurs en deux ou plusieurs étages en cascade pour atteindre les plages de variation de tension visées, et profiter de stratégies résonnantes. Il est ainsi envisageable de

développer un convertisseur à trois entrées/sorties mettant en œuvre le principe de la recopie de tension, comme présenté par les auteurs en [6] et [7] pour un convertisseur à deux ponts.

3- Le convertisseur réversible à trois entrées/sorties alimenté en courant et à résonance parallèle

Le convertisseur développé dans cette thèse est présenté sur la Figure R 13. Les trois sources de tension sont connectées en série avec des inductances que nous considérons d'abord de très forte valeur en vue de réduire l'ondulation du courant. En raison de la présence de ces inductances, l'ondulation du courant d'entrée est donc négligeable et le courant peut être considéré comme presque constant avec une petite variation autour de sa valeur moyenne. Les circuits LC connectés en parallèle aux bornes du transformateur sont utilisés dans la résonance.

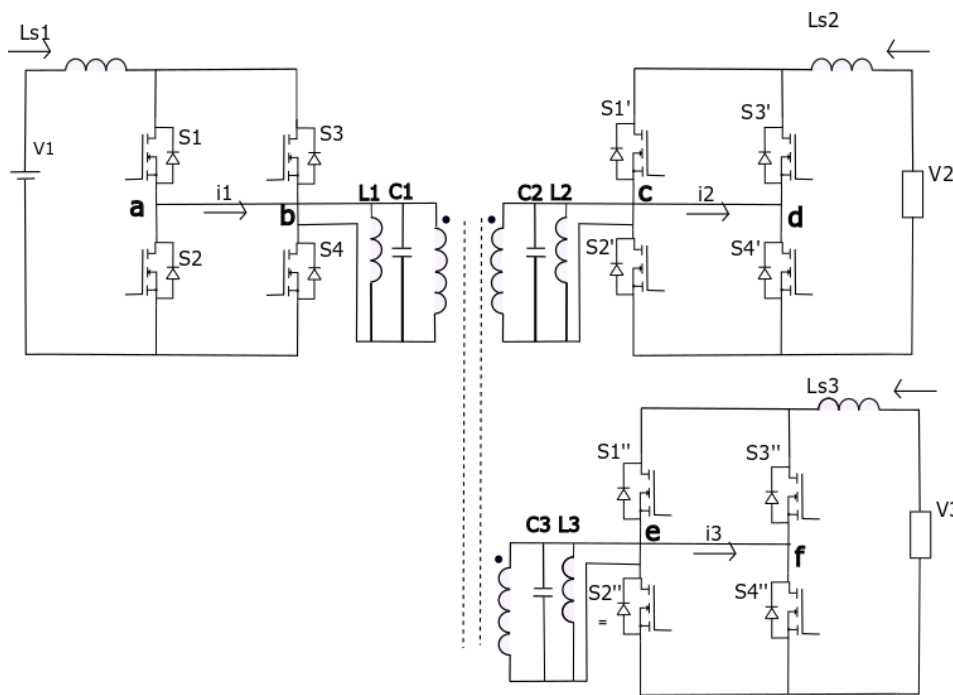


Figure R 13: Le convertisseur réversible alimenté en courant à résonance parallèle

Les transistors sont commutés alternativement par paires dans le sens diagonal comme pour un onduleur de courant dans les trois ponts. Un chevauchement est utilisé pour assurer le flux continu du courant. Lorsque les trois ponts complets sont commutés simultanément à une même fréquence, une forme d'onde rectangulaire de courant est injectée par chaque pont aux enroulements du transformateur, en parallèle avec les circuits LC.

Nous pouvons considérer la représentation sur la Figure R 14-a, où les ponts complets sont remplacés par des sources de courant carrées et le transformateur est considéré idéal, avec une inductance magnétisante infinie et une très faible énergie de fuite. Les éléments passifs sont tous transférés vers le

côté primaire du transformateur et sont représentés par une inductance et une capacité parallèle équivalente. Pour prendre en compte la présence des inductances en série, la représentation sur la Figure R 14-b peut être aussi utilisé pendant une demi-période de la période de découpage.

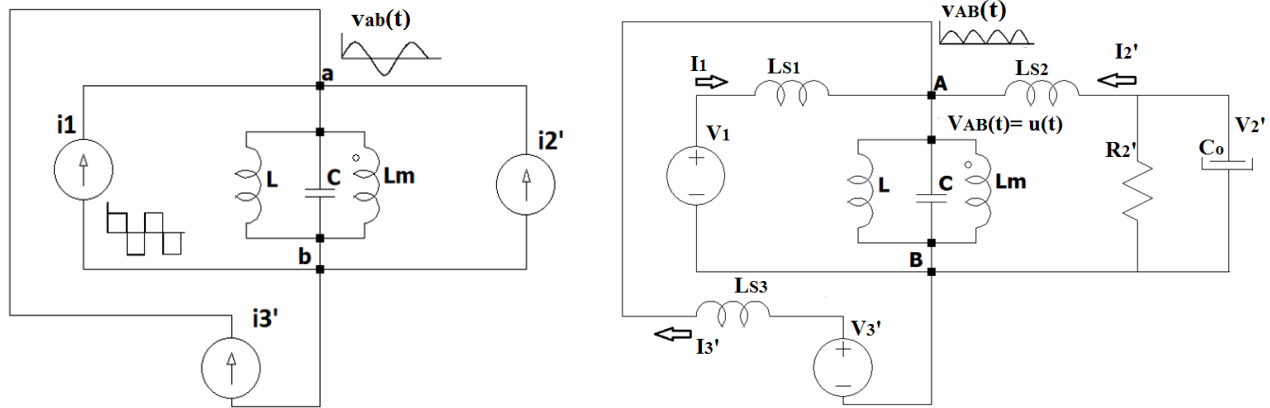


Figure R 14: a) Circuit équivalent avec inductances L_{S1} , L_{S2} et L_{S3} de fortes valeurs b) Deuxième représentation avec les inductances en série.

La somme des courants circulant dans les enroulements du transformateur est considérée comme nulle, comme on peut le voir en (1). La tension aux bornes des inductances série est calculée en fonction des trois sources de courant du côté DC :

$$V_1 = L_{S1} \frac{di_1}{dt} + u; \quad V_3' = L_{S3} \frac{di_3}{dt} + u; \quad V_2' = -L_{S2} \frac{di_2}{dt} + u \quad (7)$$

$$\frac{C L L_S}{(L_S + L)} \frac{du^2}{dt^2} + u = \left(\frac{V_1}{L_{S1}} + \frac{V_2}{L_{S2}} + \frac{V_3}{L_{S3}} \right) \frac{L L_S}{L_S + L} \quad (8)$$

La solution de l'équation différentielle dépend des conditions initiales: les transistors sont commutés lors du passage de leur tension par zéro ($u=0$), tandis que le courant dans l'inductance parallèle est alors maximal. Le condensateur équivalent est alors complètement déchargé. Les équations décrivant la tension et le courant dans la cellule résonnante parallèle sont les suivantes:

$$u(t) = I_{L_{Peak}} L W_r \sin(W_r t) + K [1 - \cos W_r t] \quad (9)$$

$$i_L(t) = -\frac{K}{L W_r} \sin(W_r t) - I_{L_{Peak}} \cos(W_r t) + \frac{K}{L} t \quad (10)$$

$$i_C(t) = C K W_r \sin(W_r t) + I_{L_{Peak}} C L W_r^2 \cos(W_r t) \quad (11)$$

La fréquence de résonance résultante du convertisseur à trois ponts dépend de la combinaison entre les éléments parallèles, mais également des inductances connectées en série avec les sources. Dans le cas où les valeurs de ces inductances en série côté DC sont très élevées par rapport à l'inductance en parallèle, la fréquence de résonance est pratiquement fixée par le circuit LC parallèle:

$$F_r = \frac{1}{2\pi} \sqrt{\frac{L+L_s}{L_s L C}} \cong \frac{1}{2\pi} \sqrt{\frac{1}{L C}} \quad (12)$$

En régime permanent, le gain entre les sources de tension et la charge est unitaire. En réalité, il sera inférieur à cause de la chute de tension aux bornes des MOSFETs et des autres éléments parasites.

Le convertisseur peut être utilisé dans des conditions ZVS lorsque la fréquence de commutation est égale ou inférieure à la fréquence de résonance. À la fréquence de résonance, l'impédance équivalente parallèle est augmentée et l'intervalle de temps correspondant à la transition est minimisé. Dans ces conditions, l'énergie de circulation est réduite et les pertes par conduction sont également minimisées. De plus, comme nous l'avons vérifié, plus faible est la fréquence de découpage, plus important est le pic de tension imposé aux transistors.

En régime permanent, la tension maximale aux bornes du transformateur correspond à la tension appliquée aux transistors de puissance. Elle peut être calculée sachant que la tension moyenne aux bornes de l'inductance côté DC est égale à zéro:

$$\frac{1}{\pi} \int_0^\pi u(t) d\omega t = V_1 \rightarrow \frac{1}{\pi} \int_0^\pi [K + (I_{L_{Peak}} L W_r) \sin W_r t - K \cos W_r t] d\omega t = V_1$$

À partir de ce résultat, nous voyons que le pic de tension dépend également du rapport entre les inductances séries côté DC (L_s) et les inductances résonnantes parallèles (L_p). Plus ce rapport est élevé, plus petit sera le pic de tension. En effet, si l'inductance côté DC est inférieure à l'inductance résonnante, la fréquence de résonance équivalente dépend également de sa valeur. D'après la Figure R 15, lorsque le rapport L_s/L_p est réduit, le pic de tension augmente:

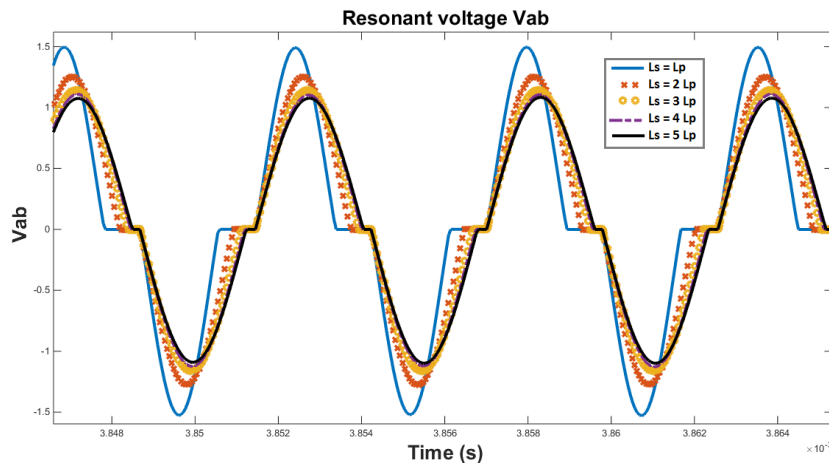


Figure R 15: Tension aux bornes du circuit résonnant pour différents ratios entre les inductances connectées en série et en parallèle.

Une des alternatives pour limiter le pic de tension sans rajouter des grosses inductances de filtrage consiste à coupler ces trois inductances. Cela est possible dans la mesure où ces inductances voient normalement les mêmes tensions. Grâce au couplage, la somme des ampères x tours moyens est théoriquement nulle (pas tout à fait en pratique car le rendement de conversion ne peut pas être égal

à un). C'est ainsi que l'encombrement global des inductances couplées peut être minimisé. Un autre avantage de cette solution est la réduction du nombre total de composants puisqu'un seul circuit magnétique est nécessaire. De plus, la réduction du pic de tension permet l'utilisation d'un MOSFET de résistance inférieure. La Figure R 16 montre que le couplage permet de minimiser cette tension, même pour de faibles valeurs d'inductance en série.

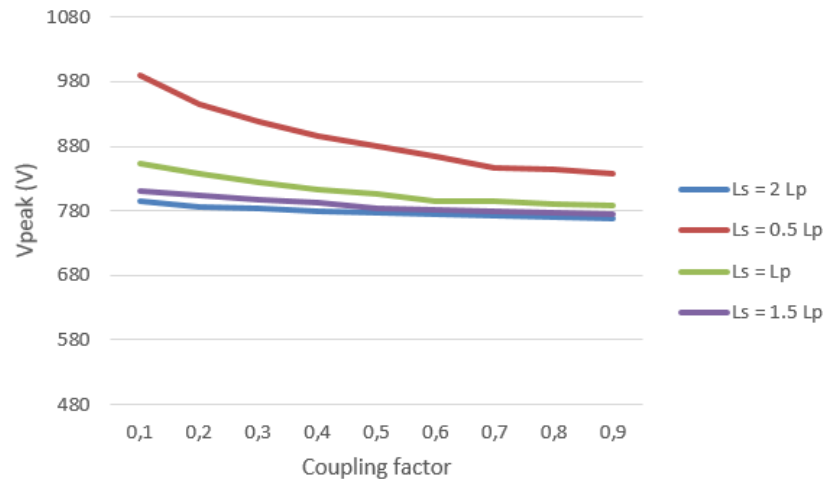


Figure R 16: Pic de tension aux bornes du circuit résonnant pour différents ratios entre les inductances en série et en parallèle, et différents facteurs de couplage entre les 3 inductances connectées en série avec les sources de tension.

Les figures suivantes illustrent le fonctionnement dans un des ponts lorsque la fréquence de découpage est inférieure, mais proche de la fréquence de résonance. Le transformateur, représenté par une inductance magnétisante infinie, est omis sur la Figure R 17, mais i_{T1} représente le courant passant du côté primaire au côté secondaire sur la Figure R 18. Considérons d'abord que les transistors de puissance S1 et S4 sont à l'état ON, pendant l'intervalle t_1 . L'inductance côté DC L_{s1} impose un courant presque constant, absorbé par le pont complet. Le courant commence à osciller entre L_1 et C_1 . À la fin de cet intervalle, C_1 , C_{s2} et C_{s3} sont complètement déchargés et les transistors S2 et S3 sont commutés à zéro de tension, pendant l'intervalle t_2 . À ce moment, le courant dans l'inductance L_1 atteint son maximum et reste constant pendant la transition. Les quatre transistors sont en conduction et le courant se répartit entre eux jusqu'à son passage par zéro.

Après, les transistors S1 et S4 sont bloqués. Pendant l'intervalle de temps t_3 , les transistors de puissance S2 et S3 sont conducteurs et le courant de résonance oscille entre L_1 et C_1 , comme dans le demi-cycle précédent. De nouveau, à l'intervalle de temps t_4 , lorsque la tension passe naturellement par zéro, les transistors S1 et S4 sont amorcés à zéro de tension. Le cycle se répète.

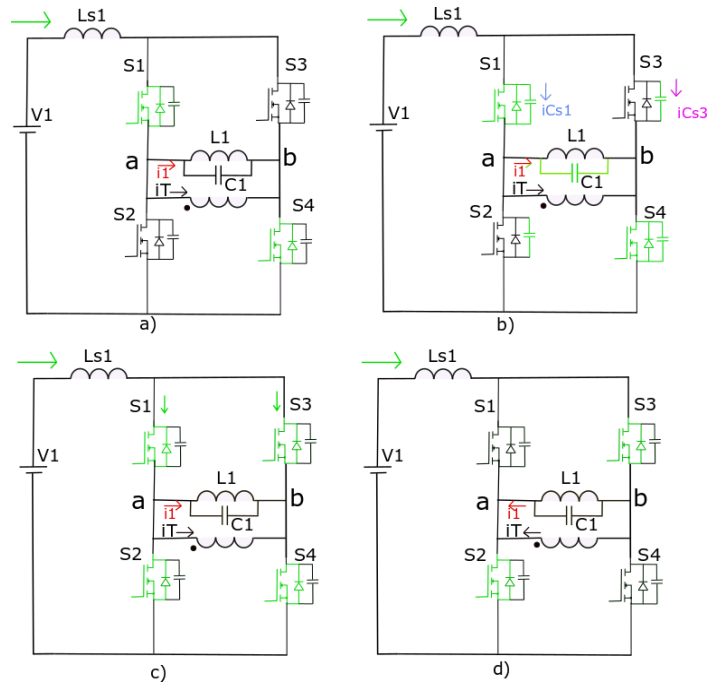


Figure R 17: Les modes de fonctionnement du convertisseur illustrés dans un seul pont. a) S1 et S4 sont ON b) Les condensateurs C_{S2} , C_{S3} et C_1 sont en cours de charge et de décharge tandis que l'énergie restante retourne à V_1 , la tension V_{ab} passe par zéro c) $V_{ab} = 0$, S2 et S3 sont amorcés à zéro de tension. D) S1 et S4 sont bloqués aussi à zéro de tension. C_{S1} , C_{S4} sont chargés progressivement tandis que V_{ab} augmente.

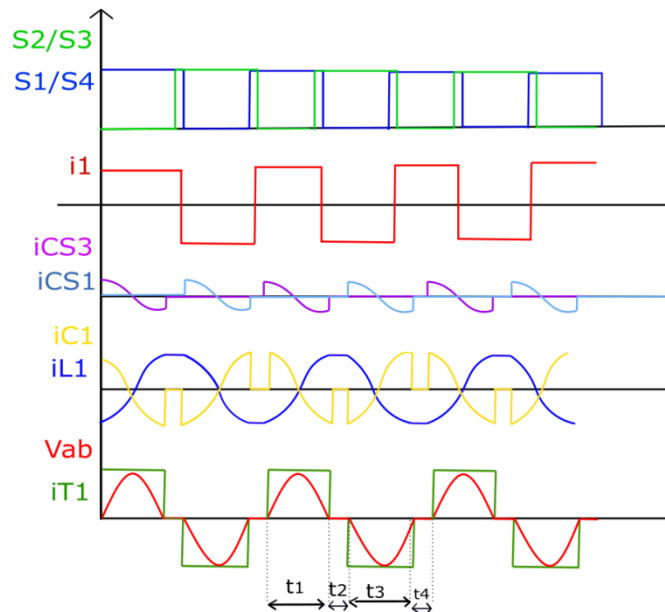


Figure R 18 : Les modes de fonctionnement du convertisseur pour un seul pont complet. Les commandes des transistors, le courant côté AC, le courant dans les capacités parasites des transistors S1 et S3, le courant de résonance dans L1 et C1, la tension du transformateur entre les bornes «a» et «b» et le courant du transformateur côté primaire $iT1$.

La stratégie de contrôle proposée pour le convertisseur bidirectionnel à trois entrées/sorties présenté dans cette thèse repose également sur la combinaison d'un signal de commutation forcée, pour éviter l'instabilité due à la variation de charge, et la détection du passage à zéro de tension permettant le ZVS. La génération du signal est présentée sur la Figure R 19. Les signaux Forced H et Forced L sont

à la même fréquence, retardés l'un de l'autre de 180° avec un petit recouvrement entre eux pour assurer la continuité du courant.

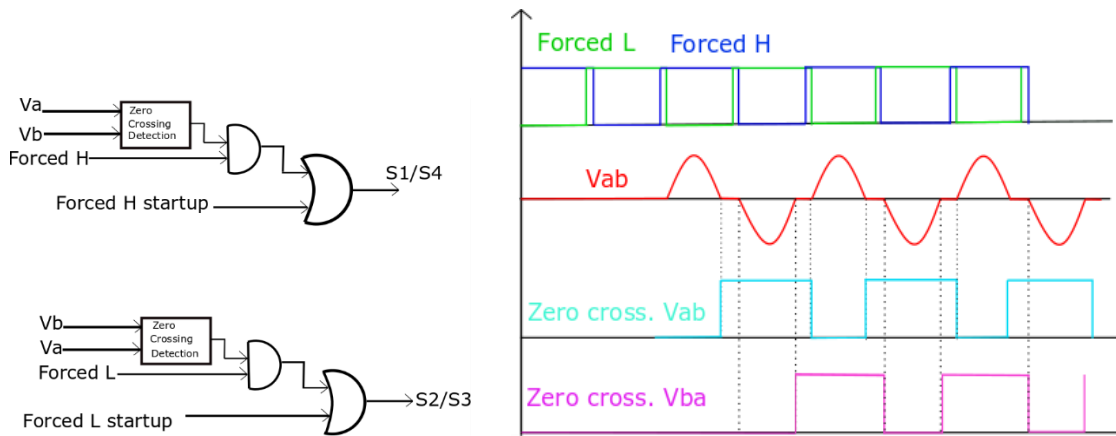


Figure R 19: La stratégie de contrôle proposée pour le convertisseur bidirectionnel à trois entrées/sorties présenté dans cette thèse repose également sur la combinaison d'un signal de commutation forcée, pour éviter l'instabilité due à la variation de charge, et la détection du passage à zéro de tension permettant le ZVS.

Pour illustrer les modes de fonctionnement du convertisseur, une application numérique est présentée ci-dessous en utilisant des inductances côté DC couplées. Cela permet de réduire le pic de tension, même en utilisant des inductances de plus faibles valeurs.

	Pont 1	Pont 2	Pont 3
Nom. Voltage (V)	480	480	20
ratio $N_1:N_2:N_3$	24	24	1
L_{s1}, L_{s2}, L_{s3}	42 μH	42 μH	73 nH
L_{p1}, L_{p2}, L_{p3}	165 μH	165 μH	290nH
C_{p1}, C_{p2}, C_{p3}	4 nF	4 nF	2.3 μF

Tableau R 3: Spécification du convertisseur utilisé dans les simulations.

La figure Figure R 20-a) et b) montre le courant au troisième et au second côté, respectivement. La Figure R 20-c) montre le courant au côté primaire du transformateur, après la cellule résonnante, et la tension de résonance V_{ab} . Des pics de courant se produisent lors de la commutation et uniquement au primaire et au secondaire en raison d'éléments parasites connectés en série avec la boucle de courant. Le convertisseur est commandé à une fréquence très proche de la fréquence de résonance. La première source de tension V_1 transfère une puissance maximale d'environ 7kW vers les deuxième et troisième côtés du convertisseur, V_2 et V_3 .

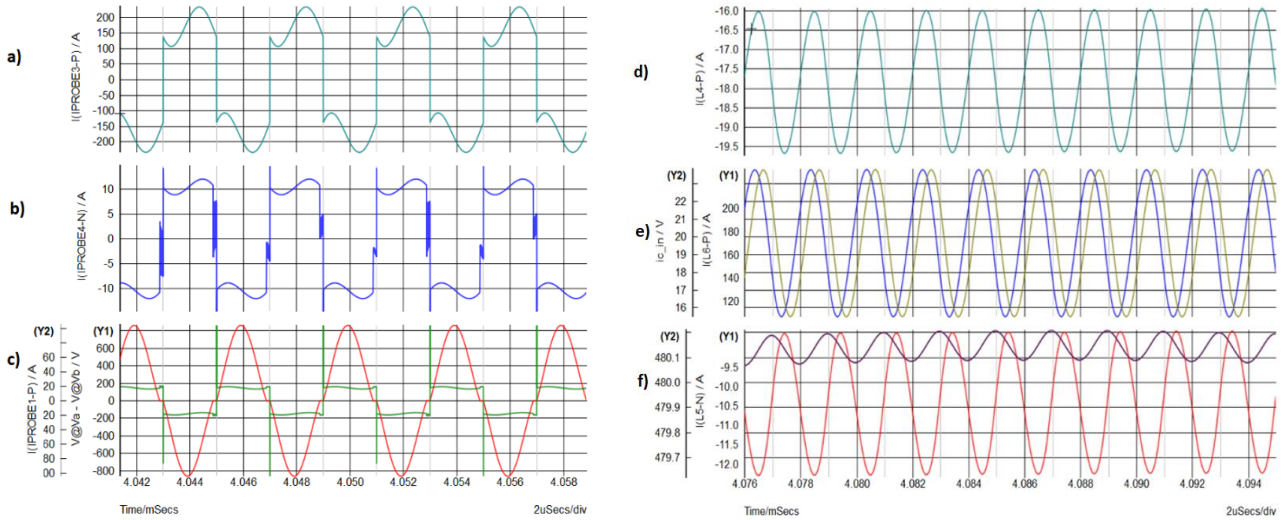


Figure R 20: Fonctionnement du convertisseur pour 7 kW vers les entrées/sorties 2 et 3 (fonctionnement simultané OBC + LDC): I- a) Courant au troisième côté, i_3 . b) Courant côté secondaire, i_2 c) Courant côté primaire du transformateur, i_{T1} et tension V_{ab} . d) courant côté DC i_{LS1} e) courant i_{LS3} et tension de sortie V_3 . f) Courant I_{LS2} et tension de sortie V_2 .

Pour assurer les conditions de commutations à zéro de tension pendant le démarrage, une stratégie a été proposée. Pour pré-charger le circuit à résonance, des commutations forcées peuvent être appliquées à une fréquence inférieure à la fréquence de résonance. Les quatre transistors d'un même pont peuvent aussi être amorcés simultanément pendant quelques instants en vue de pré-charger les inductances de filtrage. La Figure R 21 montre que la première surtension est réduite en comparaison de la Figure R 22, lorsque le temps de court-circuit imposé est plus long que le temps nécessaire donné par la formule ci-dessous:

$$t_{min} > -2RC \ln\left(\frac{V_1 L}{V_1 L + V_{Co} L_S}\right), R \text{ est une charge équivalente.}$$

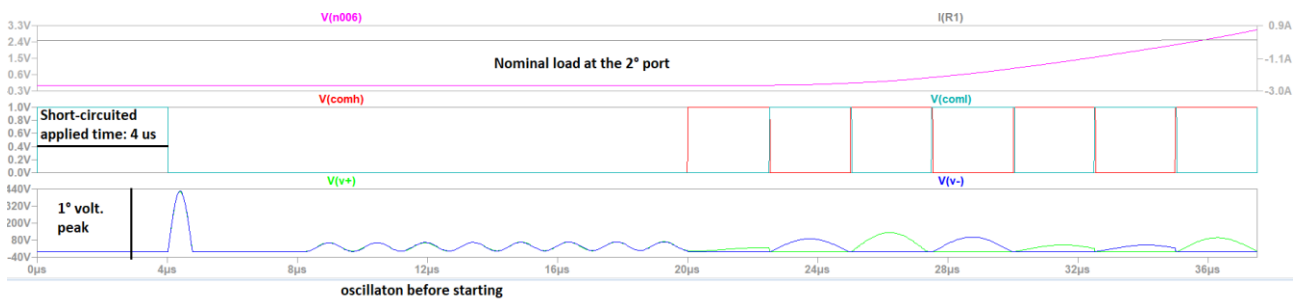


Figure R 21: Adaptation de la commande pour amorcer les quatre transistors d'un même pont pendant le démarrage avant de les faire commuter à zéro de tension. Le temps de court-circuit est suffisant pour pré-charger le circuit. L'oscillation entre C_{ds} et L_s se produit naturellement avant le fonctionnement normal du convertisseur.

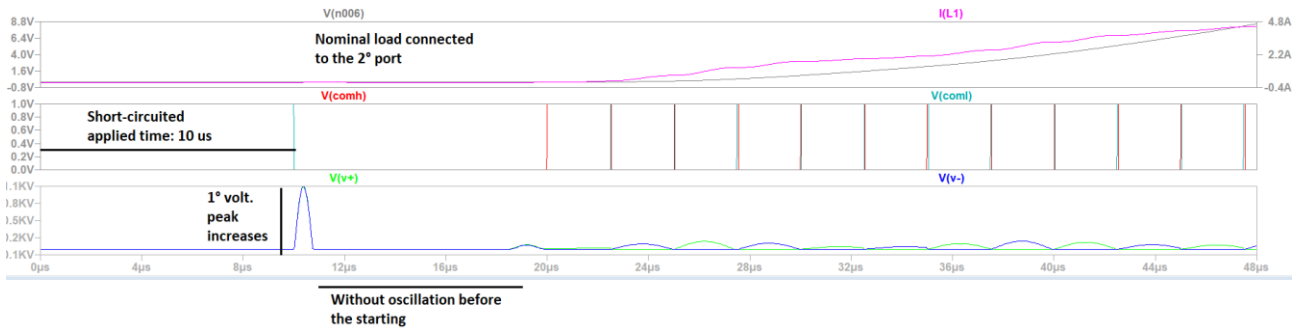


Figure R 22: Le temps de court-circuit appliqué est supérieur à celui recommandé, donc les oscillations entre C_{ds} et L_s ne se produisant pas et le convertisseur démarre lors de commutations à la fréquence de résonance en régime permanent. La surtension résultante est supérieure à la tension attendue en régime permanent.

Dans la stratégie de démarrage, il est également nécessaire de faire croître progressivement les tensions continues afin d'éviter que l'amplitude de tension au niveau du circuit à résonance soit bien supérieure à la valeur attendue pendant le régime permanent. La Figure R 23 obtenue par simulation montre cette tension lorsque le convertisseur DC-DC à trois entrées/sorties démarre alors que les courants continus ont déjà atteint leur valeur nominale. Des surtensions se produisant sur les transistors. La Figure R 24 montre l'intérêt d'augmenter progressivement les tensions continues.

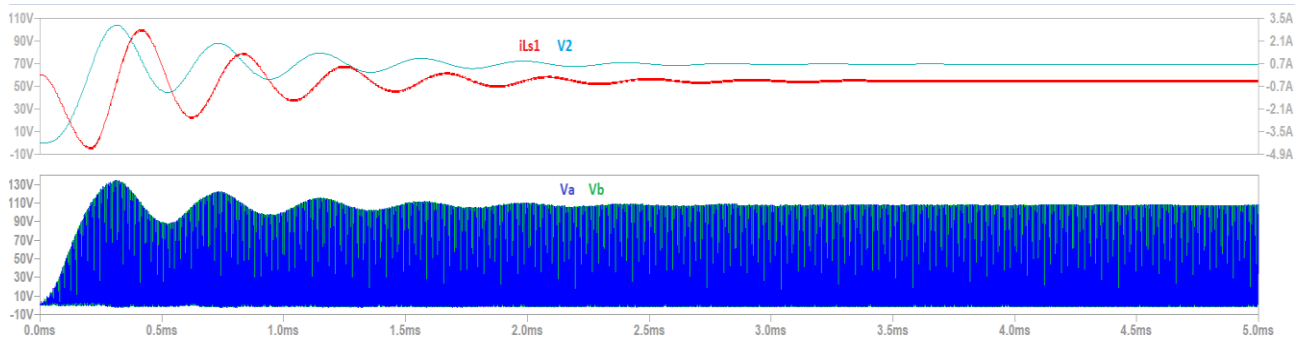


Figure R 23: Résultat de la simulation transitoire. Les tensions V_a , V_b et le courant d'entrée côté DC obtenus pour le convertisseur résonnant alimenté en courant à trois entrées/sorties.

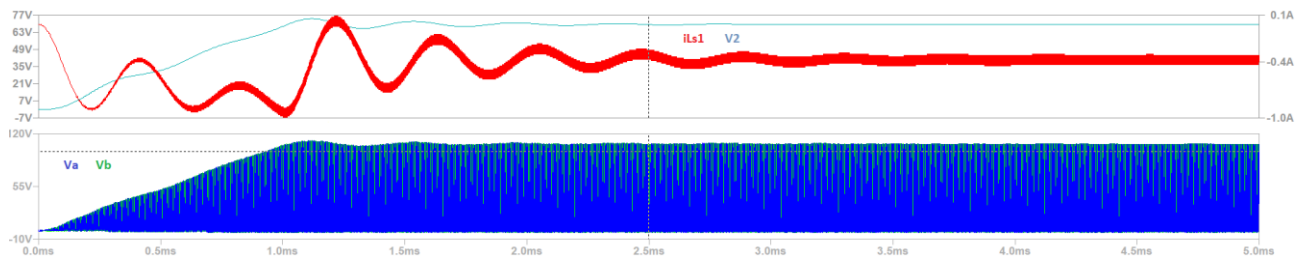


Figure R 24: Résultat de la simulation transitoire: tensions V_a , V_b et courant côté continu du convertisseur. La tension continu en entrée est augmentée de manière linéaire jusqu'à la valeur nominale pour éviter des surtensions.

Les Figure R 25 et Figure R 26 montrent les résultats expérimentaux.

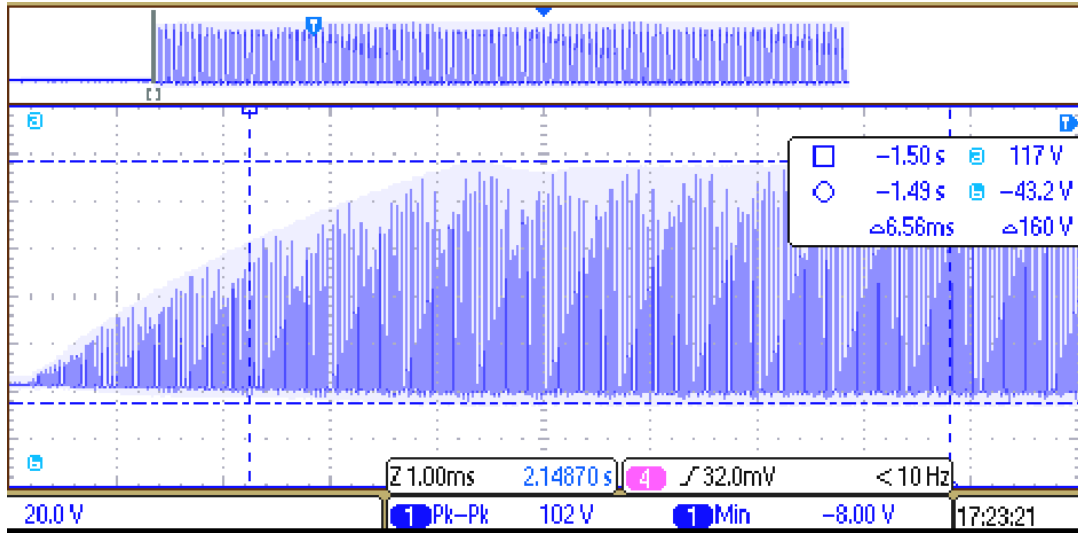


Figure R 25: Tension V_a pour le convertisseur résonnant parallèle alimenté en courant à trois entrées/sorties. La tension d'entrée V_1 est augmentée progressivement.

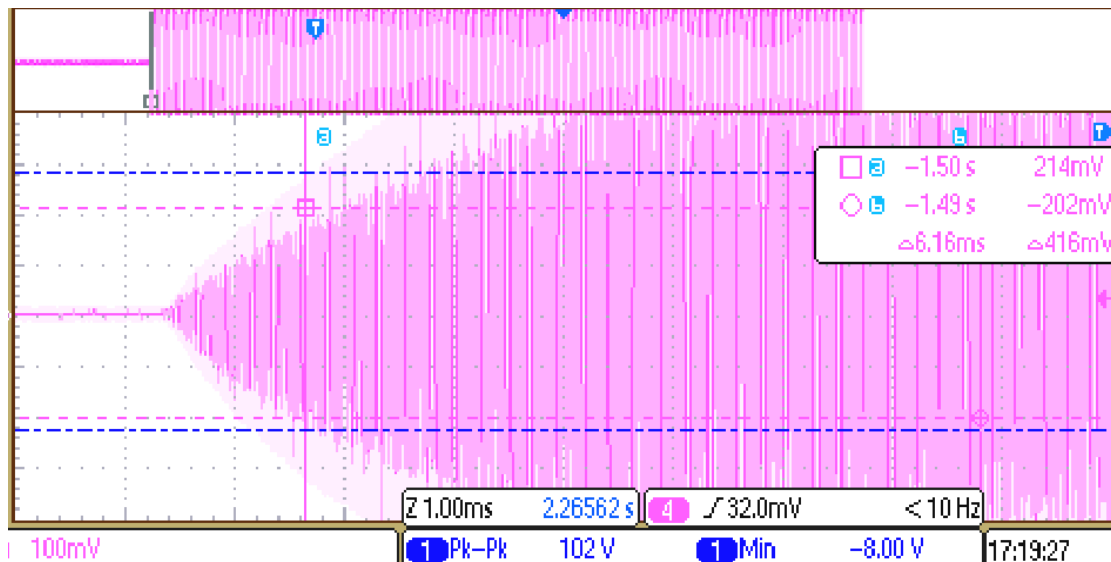


Figure R 26: Courant $i_1(t)$ dans le convertisseur résonnant parallèle alimenté en courant à trois entrées/sorties tandis que la tension d'entrée DC est augmentée progressivement. (20 mV / A).

L'étude de la méthodologie de démarrage afin d'obtenir les conditions ZVS a été réalisée pour le convertisseur résonnant parallèle bidirectionnel alimenté en courant. La méthodologie proposée permet d'éliminer d'éviter les pics de tension plus importants pendant les transitoires. Deux conditions sont nécessaires pour atteindre le ZVS lors du démarrage:

La commande du convertisseur doit réaliser un court-circuit initial pour augmenter le courant dans l'inductance côté DC, permettant ainsi l'oscillation naturelle du convertisseur avec détection de passage à zéro de tension. Une alternative consiste à imposer des commutations à fréquence fixe, inférieure à la fréquence de résonance. La charge doit consommer un faible courant pour éviter d'amortir les oscillations naturelles lors du démarrage.

4- Design du transformateur planar intégré

La technologie du transformateur planar est retenue dans ce chapitre pour réaliser un transformateur à trois enroulements, comme représenté sur la Figure R 2-a et la Figure R 13. En raison de la grande différence entre les niveaux de tension et de puissance sur les entrées/sorties, il est nécessaire de mettre en oeuvre des spires en parallèle pour supporter le courant élevé du côté basse tension. Par ailleurs, afin d'augmenter le plus possible la fréquence de découpage, le courant doit rester bien réparti entre les spires.

Dans [2], le partage de courant entre les spires en parallèle a été discuté. Il a été démontré l'importance d'une distribution équilibrée pour réduire les pertes et les hautes températures à haute fréquence. La distribution du courant peut être optimisée en utilisant des configurations entrelacées. Cependant, en raison de l'épaisseur minimale d'isolant entre les côtés bas et haute tension requise pour les applications de véhicules électriques, les configurations entrelacées associées à un nombre de tours élevé pourraient compliquer l'utilisation de la technologie planar.

Trois configurations ont été proposées pour la conception du transformateur planar à trois enroulements dans le cadre des OBC et LDC. Les trois configurations ont été retenues dans le but de réduire le coût et faciliter la réalisation du transformateur.

Afin d'estimer plus précisément les pertes en fonction de la fréquence dans les couches conductrices, une méthode analytique a été conçue et validée. Elle est présentée dans ce texte pour aider à la sélection du transformateur avec les meilleures performances, en prenant en compte le problème de distribution du courant entre les spires en parallèle. La méthode s'intègre facilement dans un script Matlab et pourrait être appliquée aux transformateurs à deux ou plusieurs enroulements, ou en présence d'un entrefer.

En ce qui concerne la détermination des pertes, lorsqu'il est nécessaire d'utiliser des couches connectées en parallèle, seulement les hypothèses de Dowell [3] ne sont pas suffisantes. Ces hypothèses impliquent en particulier que les pertes ne sont pas très bien estimées. Cela se produit parce que le courant total circulant dans chaque conducteur est considéré comme inchangé, mais en réalité ce n'est pas le cas pour les couches connectées en parallèle. Lorsque la fréquence augmente, le partage de courant entre les couches doit être identifié avant l'analyse des pertes.

La méthode de calcul des pertes utilisée dans cette thèse peut être expliquée en utilisant la structure magnétique de la Figure R 27-a. Les N couches conductrices sont empilées dans le schéma autour de la jambe centrale du noyau magnétique. Un petit entrefer est ajouté à la structure. Certaines hypothèses sont faites: les lignes du champ magnétique sont perpendiculaires à la jambe centrale du noyau magnétique; la perméabilité du noyau est infinie et l'entrefer est petit pour éviter que les lignes de champ ne s'éloignent trop. Au niveau de chaque couche conductrice, on considère un courant i_k et un flux magnétique Φ_k produit par ce courant.

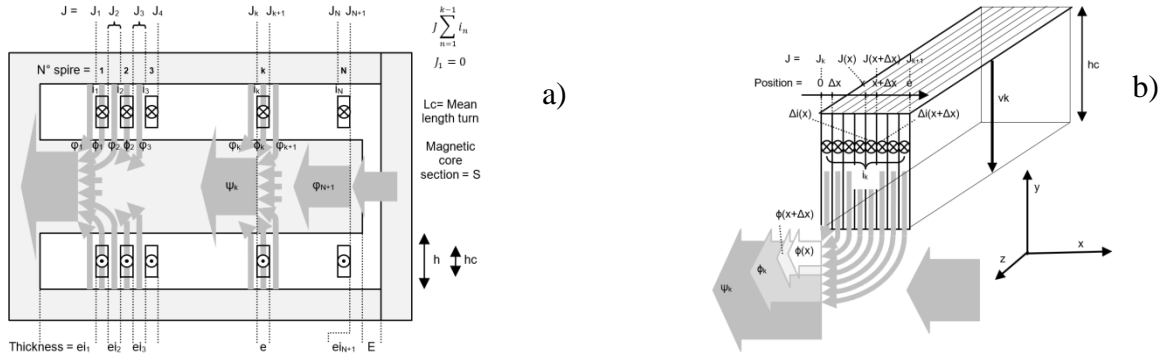


Figure R 27: a) La structure magnétique planar utilisée pour illustrer le calcul analytique des pertes
b) Un seul conducteur considéré comme l'assemblage de couches élémentaires fines.

En dehors de la région conductrice, à travers un isolant, la somme J_K des ampères-tours, J_k est calculée à partir des courants dans les conducteurs situés à gauche.

ϕ_K est le flux magnétique dans les couches d'isolation. Le flux magnétique total juste après le k-ième conducteur est représenté par ψ_k et est la contribution de toutes les couches placées sur son côté gauche.

Sur la Figure R 27-b, une seule couche est représentée sous la forme d'un assemblage de couches élémentaires infiniment minces. Dans chaque couche élémentaire circule une portion de courant $\Delta i(x)$. La chute de tension entre les portions x et $x + \Delta x$ correspond à la variation du flux magnétique, $\phi(x + \Delta x)$ et $\phi(x)$:

$$\Delta i(x + \Delta x) - \Delta i(x) = \frac{1}{r} \frac{d[\phi(x + \Delta x) - \phi(x)]}{dx} \quad (1)$$

$$J = \oint \vec{H} \cdot d\vec{y} = \oint \frac{\vec{B}}{\mu_0} \cdot d\vec{y} = \oint \frac{\Delta \phi}{\mu_0 (\Delta x \Delta L)} dy = \frac{\Delta \phi}{\mu_0 \Delta x} \oint \frac{dy}{\Delta L} \quad (2)$$

La résistance de chaque couche élémentaire de cuivre peut s'écrire:

$$\frac{1}{\Delta r} = \int \frac{\Delta x dy}{\rho \Delta L} = \frac{\Delta x}{\rho} \int \frac{dy}{\Delta L} \quad (3)$$

Avec les équations (2) et (3), on obtient le flux magnétique qui dépend de la résistance :

$$\sum \Delta \phi = J \mu_0 \sum \frac{\Delta x}{\oint \frac{dy}{\Delta L}} = J \mu_0 \sum \frac{\Delta r \Delta x^2}{\rho} = \frac{J \mu_0}{\rho} r \Delta x^2 \quad (4)$$

En supposant une forme de courant sinusoïdale, les ampères-tours, J_K peuvent ainsi s'exprimer:

$$\frac{\Delta i(x + \Delta x) - \Delta i(x)}{\Delta x^2} = \frac{\mu_0}{\rho} \frac{dJ}{dx} \rightarrow \frac{\mu_0}{\rho} j\omega J = \frac{d^2 J}{dx^2}$$

$$J = J_A e^{\alpha x} + J_B e^{-\alpha x}, \quad x_0 = \sqrt{\frac{2\rho}{\mu_0 \omega}}, \quad \alpha = \frac{1+j}{x_0} \quad (5)$$

Les coefficients J_{AK} et J_{BK} dans l'équation (5), sont déterminées par les conditions à $x = 0$ et $x = e$, J_k et J_{k+1} , respectivement, où $\alpha = (1 + j) / x_0$:

$$J_{AK} = \frac{-J_K e^{-\alpha e} + J_{K+1}}{e^{\alpha e} - e^{-\alpha e}} \quad \text{and} \quad J_{BK} = \frac{J_K e^{\alpha e} - J_{K+1}}{e^{\alpha e} - e^{-\alpha e}} \quad (6)$$

La chute de tension dans chaque partie de la couche conductrice peut maintenant être calculée:

$$v_K = j\omega \Psi_K + r \Delta x \alpha (J_{A_K} - J_{B_K}) \text{ at } x = 0 \quad (7)$$

Le flux magnétique total au centre du noyau magnétique sera la contribution du flux magnétique circulant entre les conducteurs, ϕ_k , et circulant dans les conducteurs, ψ_k :

$$\Psi_k = \sum_{n=k}^N \phi_n + \sum_{n=k+1}^{N+1} \psi_n \quad (8)$$

$$\phi_K = \frac{\mu_o \Delta L}{h_C \alpha} \frac{e^{\alpha e} + e^{-\alpha e} - 2}{e^{\alpha e} - e^{-\alpha e}} (J_K + J_{K+1}) \quad (9)$$

$$\psi_K = \frac{\mu_o \Delta L}{h_C} \int_0^{e_i} J_K dx = \frac{\mu_o \Delta L}{h_C} J_K e_{i_K}, \quad 1 \leq k \leq N \quad (10)$$

Où e_{i_k} est l'épaisseur de l'isolant.

La chute de tension dans une seule couche est la contribution des flux magnétiques ϕ_k et ψ_k , circulant dans les autres conducteurs et dans les surfaces isolantes, plus la contribution qui provient de sa propre distribution de courant, qui est aussi associée à la contribution de l'effet peau.

Il ne reste plus qu'à déterminer la solution du système avec les équations linéaires. Le système comporte $2N+1$ inconnues : N tensions v_k et au $(N+1)$ J_k . En utilisant les informations sur les connexions des enroulements et les conditions électriques des enroulements, sous forme de tension ou de courant, nous pouvons trouver la solution associée au système linéaire :

Pour les spires connectées en série, le courant total ne change pas d'une couche à l'autre. Pour les enroulements où il est nécessaire d'inclure des connexions parallèles, la chute de tension entre $x = [0: e]$ est la même pour toutes les couches. La dernière condition est que le $J_1 = 0$ à la fin de la disposition des spires. On obtient alors une matrice $(2N + 1) \times (2N + 1)$ reliant J_k et ψ_k , en utilisant l'équation (9) et l'équation (10).

$$\begin{bmatrix} \psi_1 \\ \dots \\ \psi_k \\ \dots \end{bmatrix} = \begin{bmatrix} \frac{\mu_o L_c}{\alpha h} \cdot e_{i_1} \dots + \\ \dots \\ \dots \\ \dots \end{bmatrix} \begin{bmatrix} J_1 \\ \dots \\ J_k \\ J_{k+1} \end{bmatrix}$$

Nous avons envisagé trois configurations initiales pour l'arrangement des spires dans le transformateur. Elles sont présentées à la Figure R 28. La distribution de courant et les pertes totales en fonction de la fréquence ont été obtenues pour chaque configuration par la méthode analytique. Les résultats sont présentés sur les Figure R 29, Figure R 30 et Figure R 31 pour le mode de fonctionnement OBC+DC/DC, lorsque l'enroulement primaire répartit la puissance de 7kW entre les deux enroulements secondaire et tertiaire. A côté de chaque résultat obtenu, le résultat donné par FEMM est montré pour valider la méthode analytique utilisée.

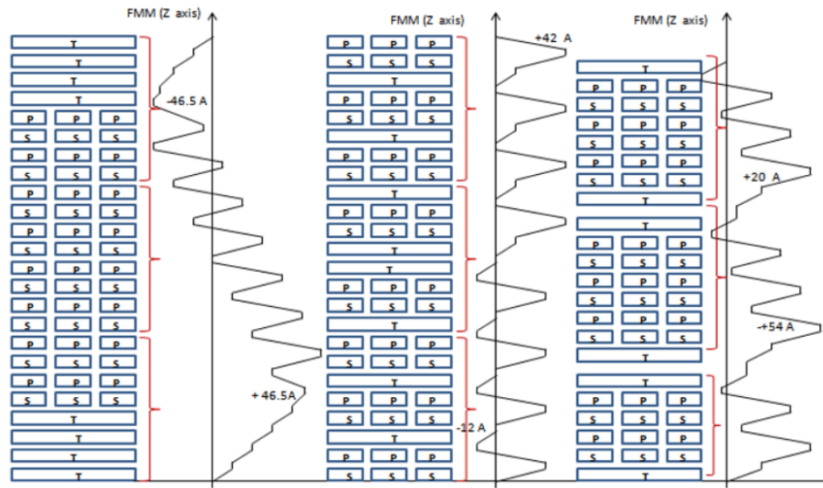


Figure R 28: Configurations de l'assemblage pour le transformateur et les ampères-tours estimés avec la supposition que le courant est bien distribué entre les couches parallèles A) Non entrelacé B) Entièrement entrelacé C) Partiellement entrelacé.

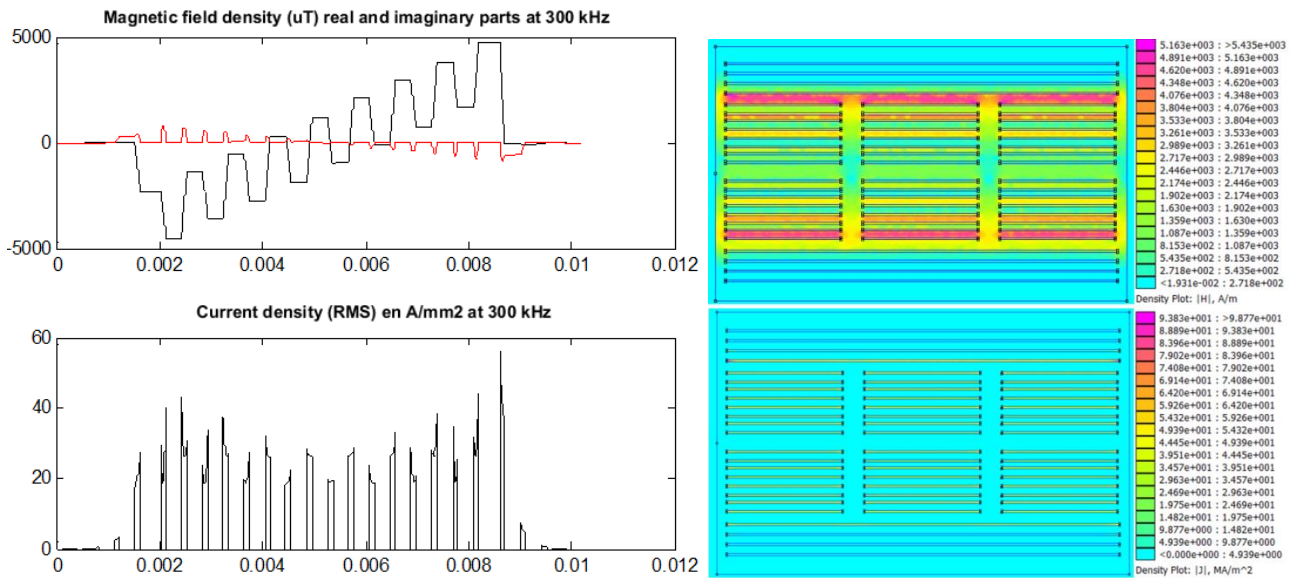


Figure R 29: Flux magnétique et densités de courant pour l'arrangement non entrelacé. a) Obtenu avec la méthode analytique b) obtenu avec FEMM

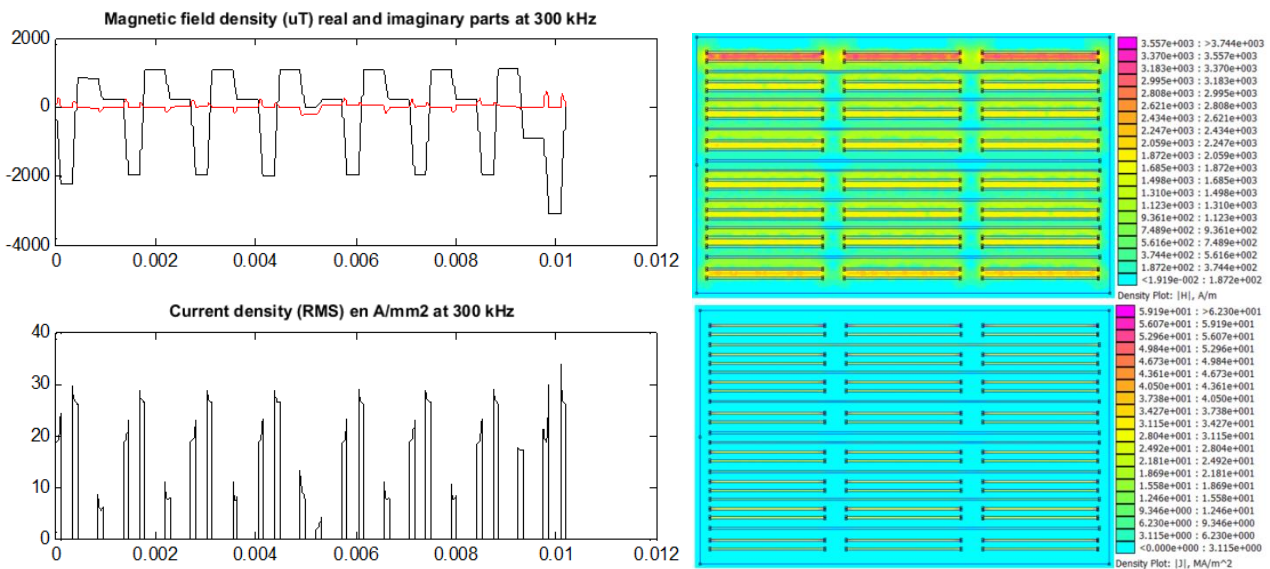


Figure R 30: Flux magnétique et densités de courant pour l'arrangement entièrement entrelacé. a) Obtenu avec la méthode analytique b) obtenu avec FEMM

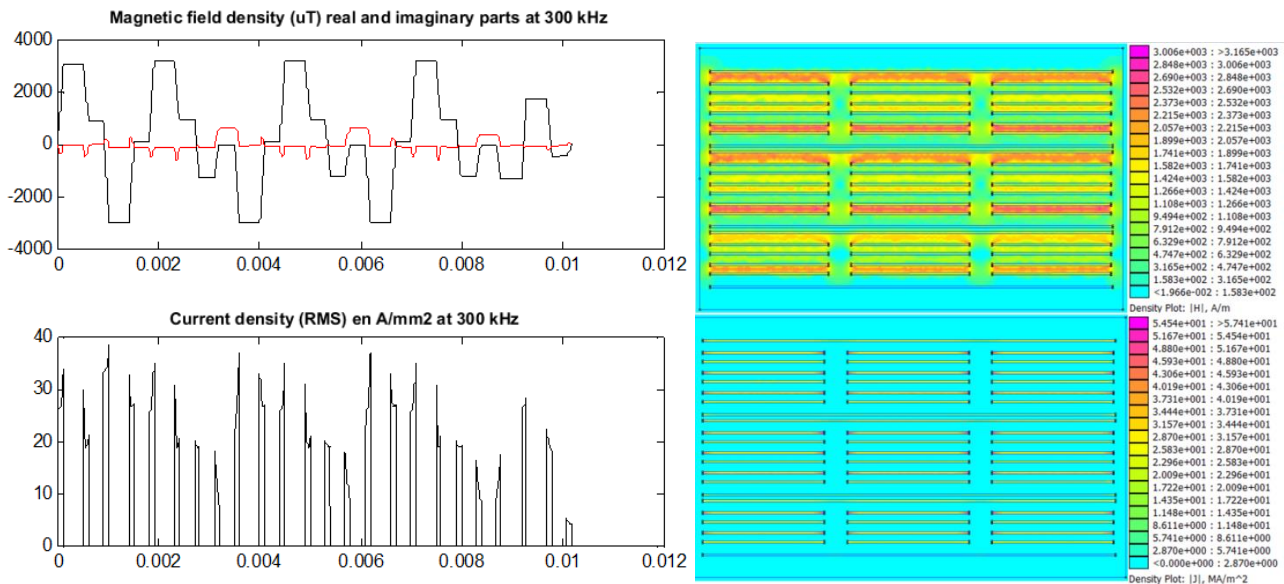


Figure R 31: Flux magnétique et densités de courant pour l'arrangement entrelacé partiellement. a) Obtenu avec la méthode analytique b) obtenu avec FEMM

On voit que le profil de champ magnétique obtenu par simulation est très similaire aux résultats obtenus avec l'approche analytique. Lorsqu'on compare les trois configurations, la seconde est la meilleure tant en ce qui concerne la répartition de courant que les pertes et les fuites magnétiques. Cette deuxième configuration a été réalisée en utilisant trois PCB de huit couches pour chacun. Le prototype est montré sur la Figure R 32.



Figure R 32: Le transformateur planar développé pour le convertisseur à trois entrées/sorties.

Après l'étude d'un modèle thermique équivalent et en considérant le refroidissement forcé par ventilateur, le Tableau R 4 renseigne sur les pertes et la température finale estimée pour les trois modes de fonctionnement: l'OBC, DC/DC (LDC) et l'OBC+DC/DC.

Mode	Pertes cuivre (W)	Pertes fer (W)	θ_c (°C)	θ_F (°C)
OBC	62.52	29.56	142.1	135.7
LDC	17.25	24.56	83.6	86.4
OBC + LDC	49.17	29.56	126.2	123.1

Tableau R 4: Estimation de la température à l'aide du modèle thermique équivalent pour les trois modes de fonctionnement du convertisseur. Les résistances thermiques sont prises en compte avec un ventilateur supplémentaire placé à 5 cm du transformateur. $\theta_{amb} = 40$ °C.

En utilisant la même méthode analytique implémentée sur Matlab, un modèle électrique équivalent a été aussi proposé en considérant l'effet de la fréquence. Pour cela, des tests en court-circuit et en circuit ouvert ont été simulés avec le script afin d'établir des matrices contenant des impédances équivalentes :

$$\left\{ \begin{array}{l} v_1 = z_{11} \cdot i_1 + z_{12} \cdot i'_2 + \dots + z_{1N} \cdot i'_N \\ v'_2 = z_{21} \cdot i_1 + z_{22} \cdot i'_2 + \dots + z_{2N} \cdot i'_N \\ \dots \\ v'_N = z_{N1} \cdot i_1 + z_{N2} \cdot i'_2 + \dots + z_{NN} \cdot i'_N \end{array} \right. \quad (12)$$

$$\left\{ \begin{array}{l} i_1 = y_{11} \cdot v_1 + y_{12} \cdot v'_2 + \dots + y_{1N} \cdot v'_N \\ i'_2 = y_{21} \cdot v_1 + y_{22} \cdot v'_2 + \dots + y_{2N} \cdot v'_N \\ \dots \\ i'_N = y_{N1} \cdot v_1 + y_{N2} \cdot v'_2 + \dots + y_{NN} \cdot v'_N \end{array} \right. \quad (13)$$

$$v'_i = \frac{v_i}{m_{1i}} \quad i'_i = m_{1i} \cdot i_i \quad z_{ij} = \frac{\alpha_{ij}}{m_{1i} \cdot m_{1j}} \quad y_{ij} = m_{1i} \cdot m_{1j} \cdot \beta_{ij} \quad (14)$$

Ces impédances équivalentes ont été modélisées comme des inductances en série avec des résistances afin de décrire les parties réelles et imaginaires du champ magnétique obtenues en fonction de la fréquence. La Figure R 33 et Figure R 34 montrent le modèle équivalent obtenu.

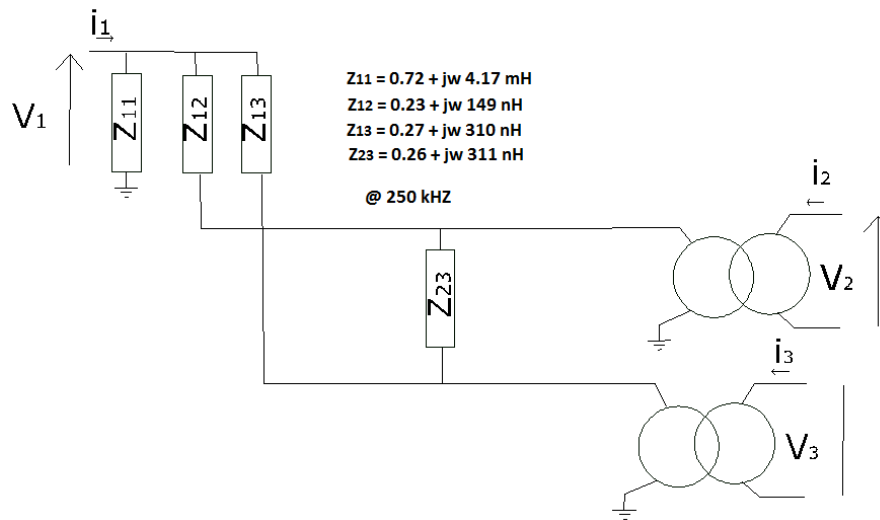


Figure R 33: Circuit équivalent du transformateur obtenu à 250 kHz.

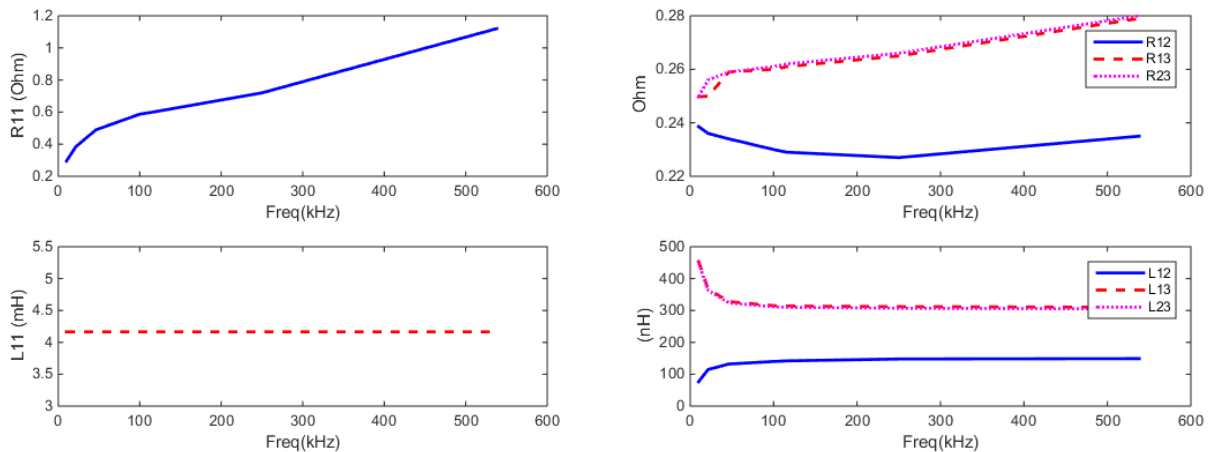


Figure R 34: Les éléments passifs du modèle équivalent obtenus en fonction de la fréquence.

Ensuite, ce modèle a été comparé avec les résultats obtenus par mesure en utilisant un analyseur d'impédance. Les résultats entre l'approche analytique et les mesures réelles sont indiquées dans le Tableau R 5.

	Résultats Matlab	Analyseur d'impédance
L10, R10	4.174 mH, 0.72 Ω	4.86 mH, 1.12 Ω
L12, R12	149 nH, 0.228 Ω	195 nH, 0.19 Ω
L13, R13	309 nH, 0.26 Ω	265 nH, 0.31 Ω
L23, R23	311 nH, 0.27 Ω	263 nH, 0.30 Ω

Tableau R 5: Les paramètres du circuit équivalent à 250 kHz.

Afin de compléter l'étude du prototype, des capacités parasites entre enroulements et propres à chaque enroulement ont aussi été modélisées, comme à la Figure R 35 et le Tableau R 6.

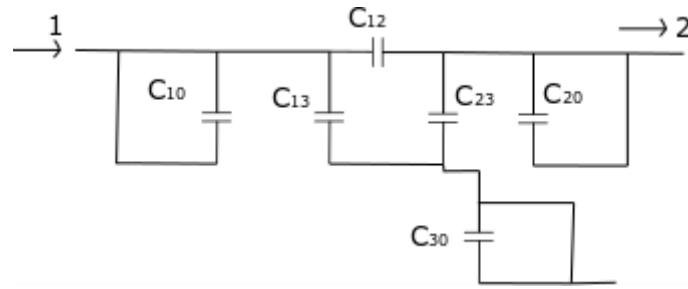


Figure R 35: Représentation des capacités parasites. $C_{30} \approx 0$

	Impedance Analyzer
C10	1.12 nF
C12	0.49 nF
C13	0.27 nF
C23	0.26 nF

Tableau R 6 : Les capacités parasites équivalentes dans le transformateur planar obtenues avec l'analyseur d'impédance et les outils de simulation.

Pour conclure, trois configurations différentes ont été proposées en visant la simplification du processus de fabrication du transformateur, la minimisation des pertes et de l'énergie de fuite. Les couches connectées en parallèle du côté de basse tension ont nécessité une analyse plus précise, et par conséquent, une méthode analytique pour déterminer la distribution du courant et les pertes. La méthode permet de mettre en évidence rapidement les inconvénients et avantages des différents assemblages de spires. Elle est donc utile pour sélectionner la configuration avec les meilleures performances pour l'application du convertisseur. La configuration donnant la meilleure répartition des courants a été réalisée et un modèle équivalent permettant d'ajouter des éléments parasites a été déterminé.

5- Design du convertisseur à résonance parallèle

Dans ce chapitre, nous présentons aussi l'influence des éléments parasites sur le fonctionnement normal du convertisseur à trois entrées/sorties et à résonance parallèle. Avec les inductances de fuite et les capacités parasites dans le transformateur obtenues au Chapitre 4, nous pouvons utiliser le modèle de la Figure R 36.

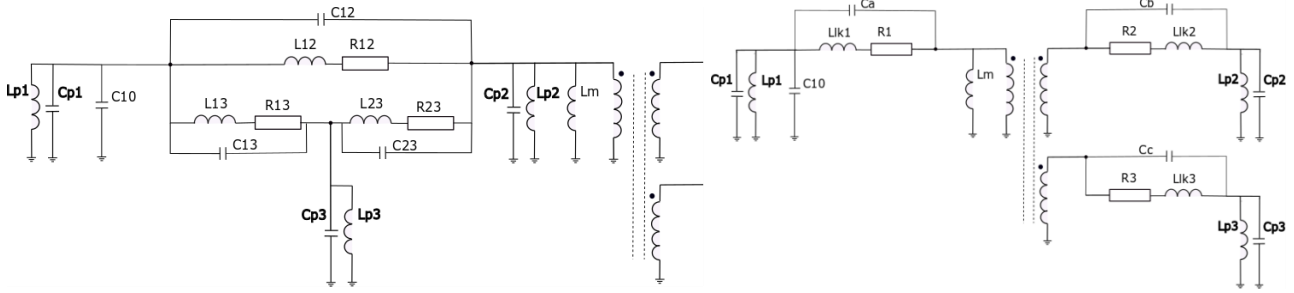


Figure R 36: Circuit équivalent du transformateur en configuration Y et Δ avec cellules résonnantes parallèles.

En utilisant les résultats des mesures avec un analyseur d'impédance et le modèle, les capacités parasites C_{10} , C_a , C_b et C_c sur la Figure R 36 peuvent être remplacées par une seule capacité comme dans la Figure R 37, C_t .

Cette représentation génère une faible erreur sur la nouvelle fréquence de résonance du convertisseur, comme nous pouvons le voir sur la Figure R 38.

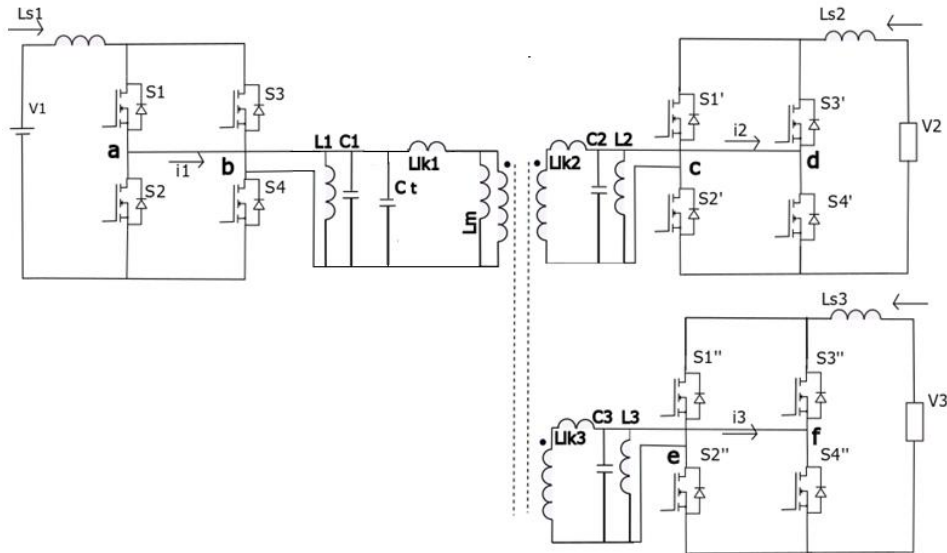


Figure R 37: Le convertisseur résonnant parallèle alimenté en courant à trois entrées/sorties avec les éléments parasites du prototype de transformateur.

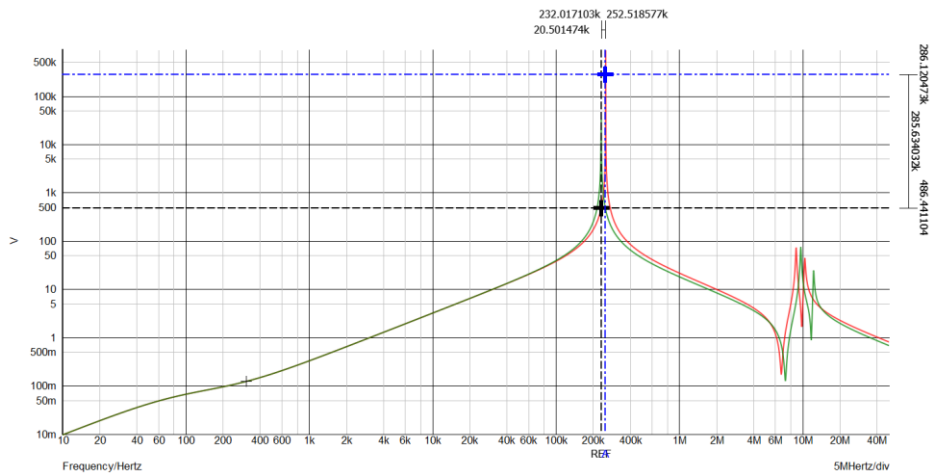


Figure R 38: Analyse d'impédance dans le but d'estimer l'effet d'une seule capacité C_t au côté primaire pour représenter les capacités parasites.

En effet, ces éléments parasites vont modifier la fréquence de résonance du convertisseur et ajouter des oscillations parasites aux fréquences ci-dessous, comme le montre la Figure R 39:

$$F_{resonant} = \frac{1}{2\pi \sqrt{(L_p)(C_p + C_t)}} \quad (15)$$

$$F_{Parasitic_1} = \frac{1}{2\pi \sqrt{(Ll k_1)(C_p + C_t)}} \quad (16)$$

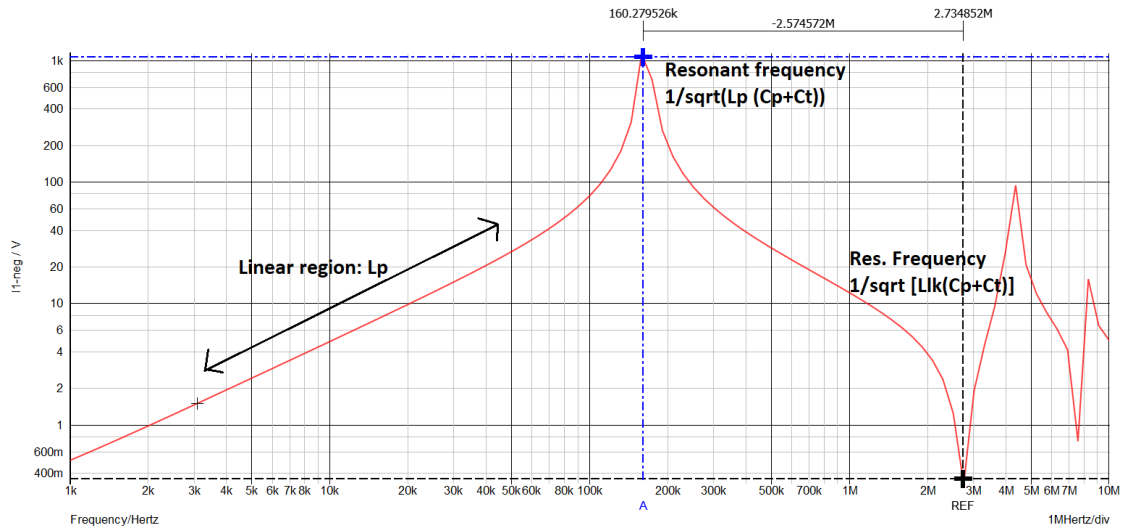


Figure R 39: Impédance du circuit équivalent dans le domaine fréquentiel.

Ces oscillations peuvent être amorties avec un circuit snubber RLC placé en parallèle avec la cellule de résonance du convertisseur aux bornes de chaque enroulement. La Figure R 40 montre les oscillations superposées aux formes d'onde du courant et tension dans les enroulements primaire et secondaire lors du fonctionnement en mode OBC. Ces oscillations peuvent être amorties, mais en augmentant les pertes.

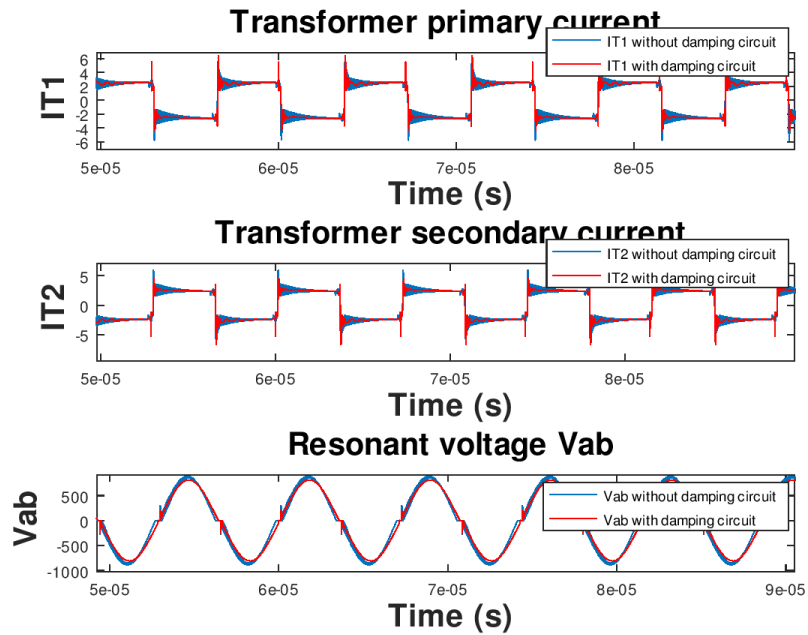


Figure R 40: Courant dans les côtés primaire et secondaire du transformateur, i_{T1} et i_{T2} , respectivement. Tension de résonance V_{ab} mesurée sur le côté primaire du transformateur. Les lignes bleues sont les données mesurées avec les oscillations parasites et la ligne rouge est le résultat obtenu avec le circuit amortisseur supplémentaire. Le circuit d'amortissement est un RLC ($R_a = 200\Omega$, $L_a = 6\mu H$ et $C_a = 1nF$. $L_{12} = 149 nH$, $L_{23} = 311nH$, $L_{13} = 310 nH$, $L_m = 4.57 mH$, $C_t = 2.53 nF$).

Le prototype complet a été réalisé avec le développement de cartes individuelles, comme le montre la Figure R 41. Des deux côtés haute tension connectées au bus DC-link à la sortie du circuit PFC et aux bornes de la batterie haute tension, des transistors SiC à 1200 V ont été utilisés. Pour la carte connectée à la batterie basse tension, des MOSFETS en Silicium ont été choisis. Pour les côtés HV nous avons utilisés un PCB à quatre couches. Pour le côté BT, le PCB comportait six couches. Des vias thermiques sont placés au-dessous de chaque transistor (TO-220) pour améliorer la dissipation thermique.

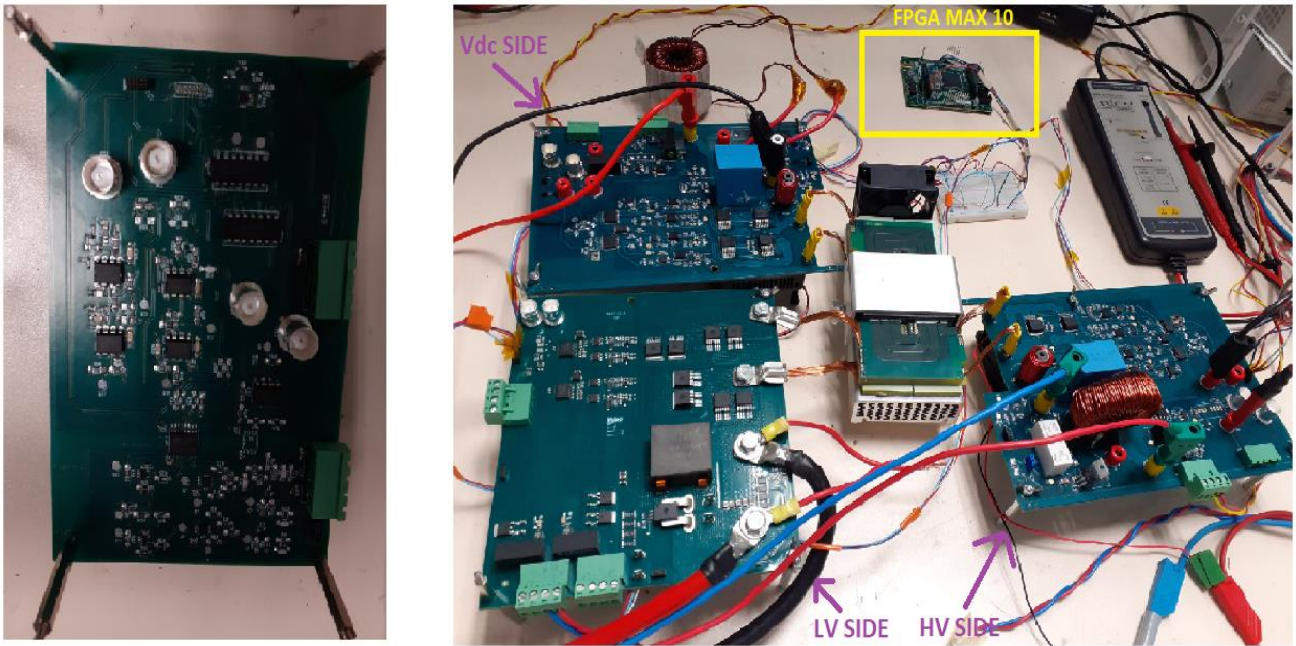


Figure R 41: Le transformateur planar et les 4 cartes conçues pour intégrer le convertisseur réversible à 3 entrées/sorties : les cartes HT, BT, Vdc et, à gauche, la carte de contrôle conçue pour la détection de passage de la tension par zéro (remplacée après par un FPGA).

Pour le refroidissement des transistors SiC et Silicium, un dissipateur avec un ventilateur ont été placés au-dessous de chaque carte électronique comme montre la Figure R 42.

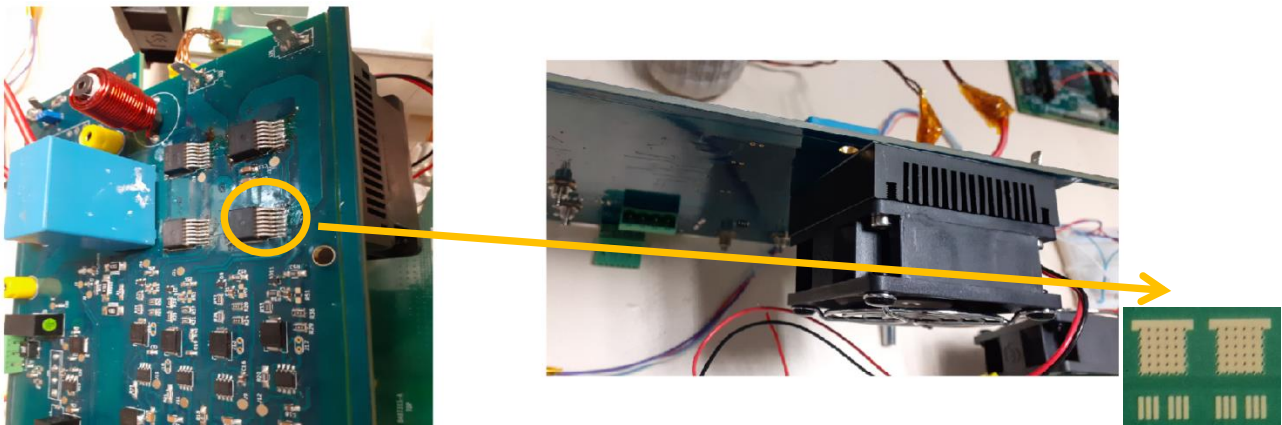


Figure R 42: Dissipateur fixé à la face inférieure du PCB pour évacuer la chaleur produite par les transistors.

Pour refroidir le transformateur, un support en aluminium a été développé, comme le montre la Figure R 43.

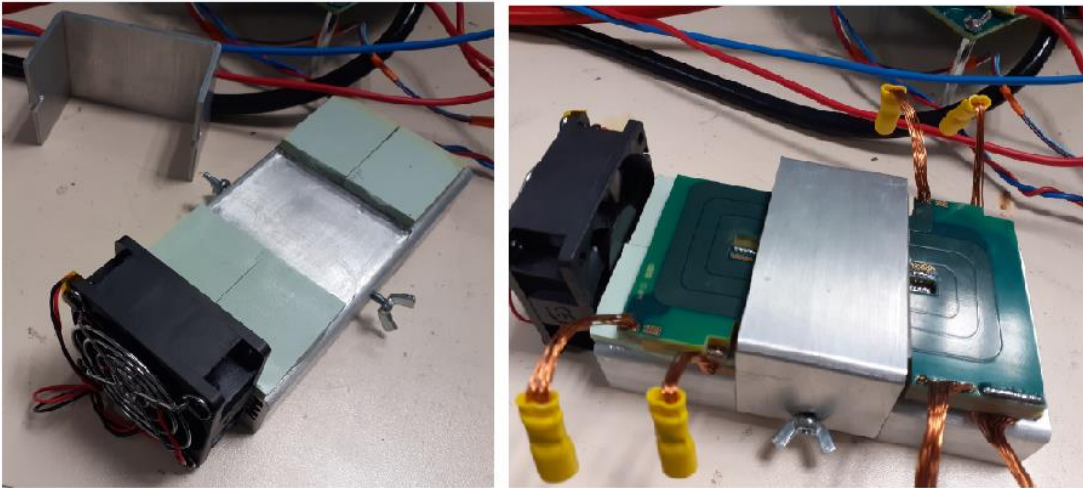


Figure R 43: Solution thermique proposée pour le transformateur.

La Figure R 44-a et b montrent la tension de résonance, le courant dans l'inductance parallèle et le courant d'entrée côté AC du convertisseur. Le courant dans l'inducteur parallèle passe par les points maximum et minimum pendant la commutation des transistors, déchargeant la capacité équivalente pour la commutation à tension nulle.

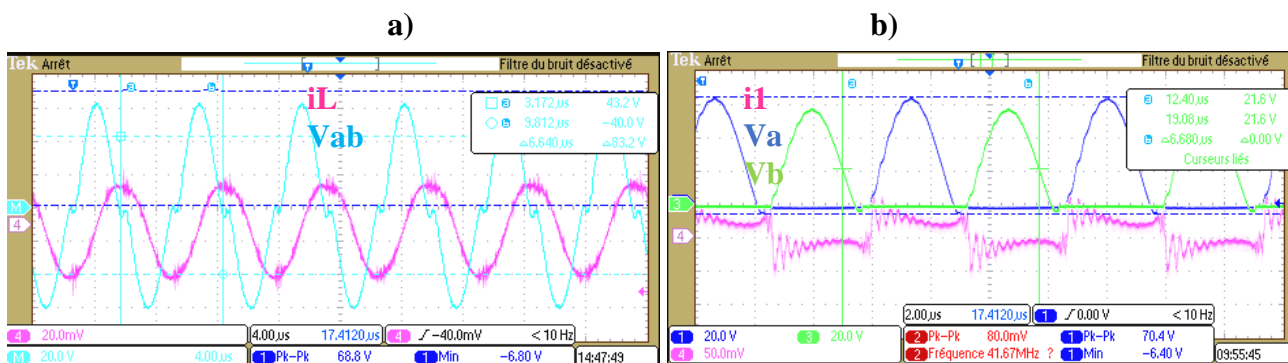


Figure R 44:a) La tension de résonance V_{ab} et le courant dans l'inductance de résonance parallèle connectée au côté primaire du convertisseur b) Tension V_a et V_b et courant du côté primaire du convertisseur pour un transfert de faible puissance.

Le convertisseur a d'abord été validé avec une charge résistive de 20 Ω connectée côté HT. Une alimentation en tension continue a été connectée directement à la première entrée/sortie du convertisseur et sa valeur a été augmentée progressivement pour éviter les dépassements de tension dans les transistors. La Figure R 45 montre la tension sur le transformateur côté Vdc et HT et le courant côté charge secondaire simulant le mode de fonctionnement OBC.

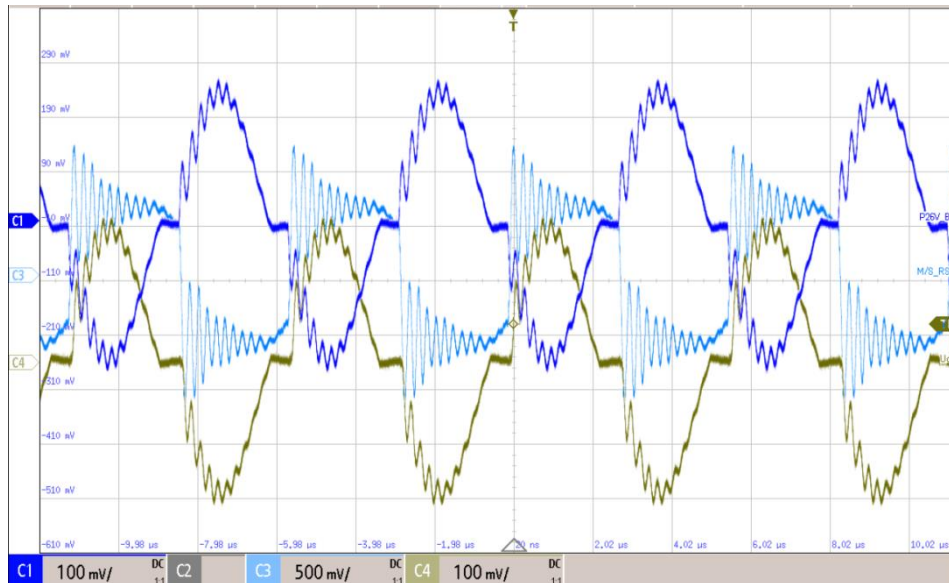


Figure R 45: Tension mesurée des deux côtés HT, ponts 1 et 2, et courant du côté secondaire du transformateur. Échelle de tension: 1/1000 et sonde de courant: 100 mV/A. Vdc = 150 V

Dans ce mode, un analyseur de puissance a été utilisé afin de mesurer le rendement de conversion pour certains points de fonctionnement. Le rendement diminue dans les faibles niveaux de puissance en raison du courant de circulation dans la cellule résonnante et les éléments passifs.

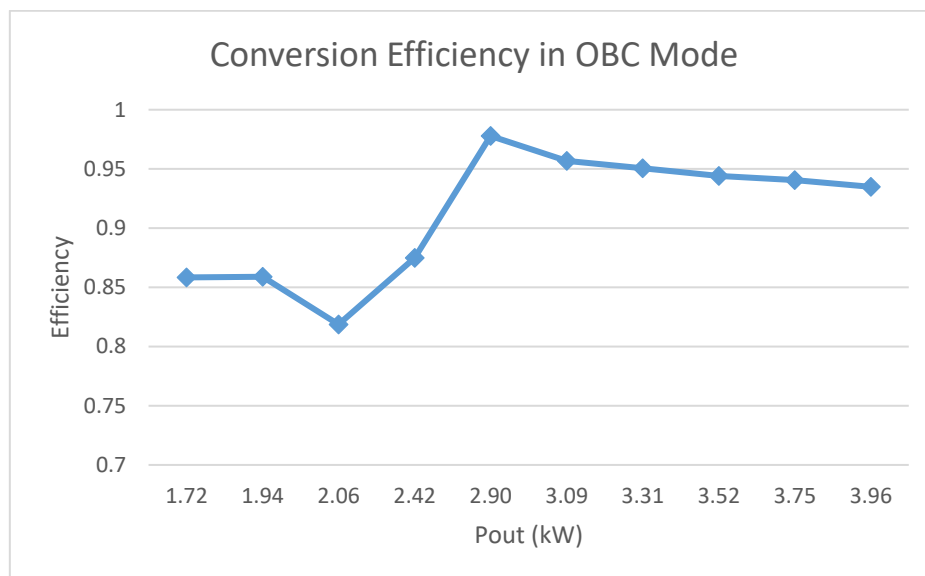


Figure R 46: Le rendement du convertisseur mesuré en mode de fonctionnement OBC ($V_{in}=240$ V).

Afin de valider le mode de fonctionnement LDC, une charge électrique dynamique a été connectée au troisième côté du convertisseur, tandis que la première entrée/sortie était en circuit ouvert. Le test a été réalisé avec une charge de courant de 150 A RMS, tandis qu'une alimentation en tension de 240 V était connectée au deuxième entrée/sortie. Les résultats sont présentés sur la Figure R 47.

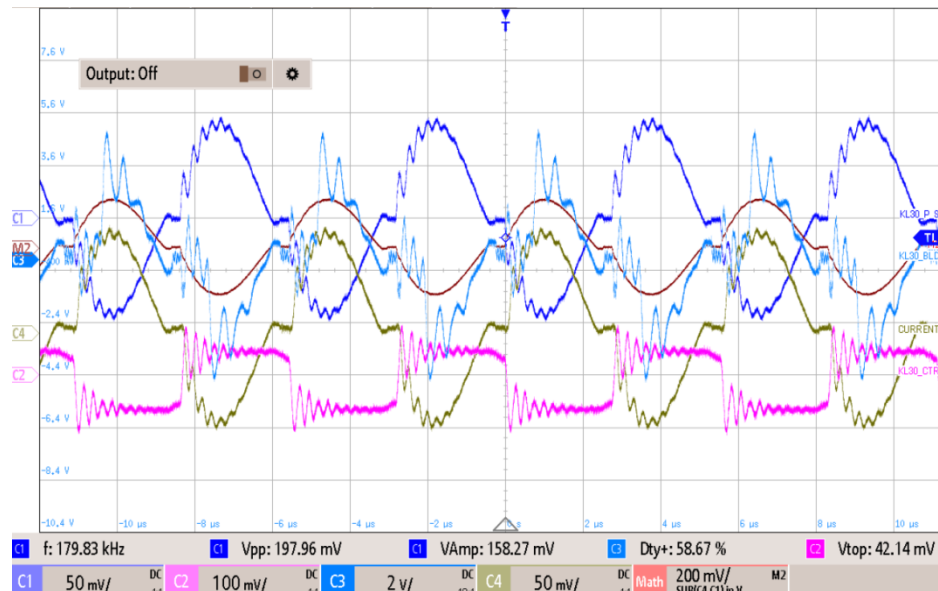


Figure R 47: Tension et courant de résonance du côté primaire et du côté secondaire du transformateur C1: Tension de résonance du côté secondaire; C2: Courant au secondaire du transformateur. C3: Courant au primaire du transformateur. C4: tension de résonance au primaire. Math: tension de résonance du troisième côté. Échelle de tension: 1/2000 et sonde de courant: 100 mV / A. $V_2 = 240$ V.

Les résultats obtenus permettant de valider les deux principaux modes de fonctionnement du convertisseur. Comme la structure est symétrique, l'OBC en mode reverse et le LDC en mode reverse se comportent comme en mode direct.

6- Le design complet des convertisseurs OBC et DC/DC

L'architecture du convertisseur OBC comporte deux étages. Le premier est dédiée au redressement et à la compensation du facteur de puissance. Le second est un convertisseur DC-DC qui permet de réguler la charge de la batterie HV et qui assure un isolement galvanique. Le convertisseur résonnant à trois entrées/sorties a des performances améliorées si la tension Vdc-link est constante, ceci permettant une conception optimale en minimisant les pertes de conduction et le volume. En raison du ZVS, les pertes de commutation sont négligeables à ce stade et la principale limitation pour augmenter la fréquence de résonance est l'augmentation de la température dans le transformateur.

Cependant, le convertisseur résonnant à trois ponts présenté dans les chapitres précédents ne régule pas la tension, et par conséquent, un étage de convertisseur DC-DC non isolé est toujours nécessaire pour assurer la variation de tension aux niveaux des batteries. Sur la Figure R 48, un demi-pont est connecté aux sorties du convertisseur résonnant à trois entrées/sorties, ce qui permet la régulation des tensions de sortie.

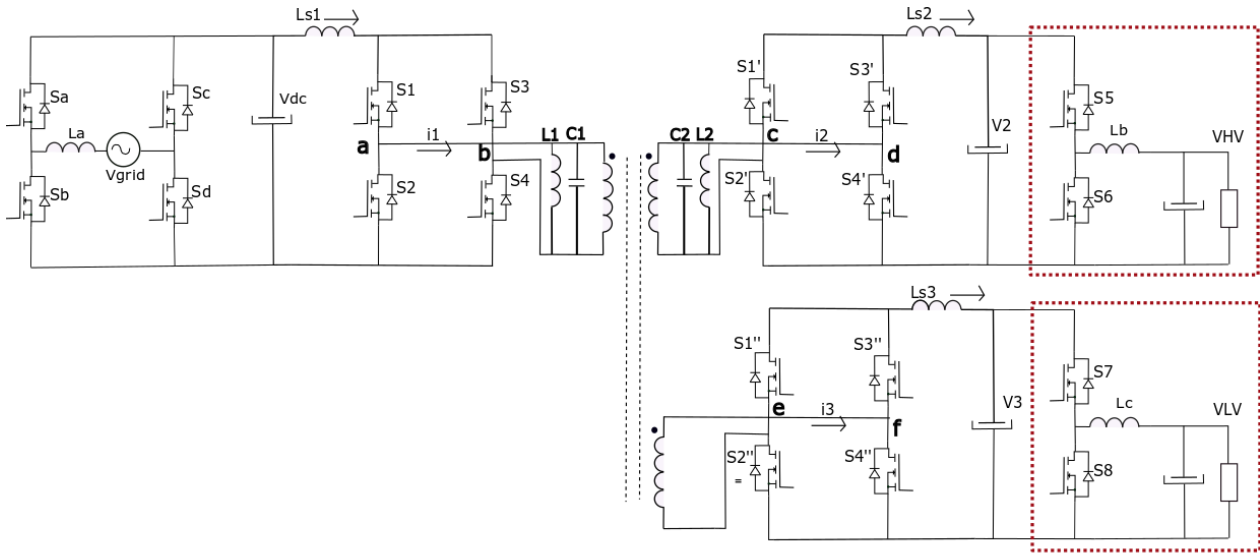


Figure R 48: L'architecture complète permettant les fonctions OBC et LDC avec réversibilité des flux d'énergie.

Cet étage DC-DC non isolé peut-être réalisé de différentes façons. Nous avons donc recherché le meilleur compromis entre les pertes de commutation et de conduction pour les côtés HV et LV. En comparant les modes de conduction continue (CCM), discontinue (DCM) et triangulaire (TCM) - [13] pour le demi-pont, nous pouvons évaluer les avantages et les inconvénients de chaque stratégie. Par exemple, en mode boost, le principal problème de fonctionnement d'un demi-pont en mode CCM est l'énergie de recouvrement reverse, comme le montre la Figure R 49. En mode DCM, ce problème n'existe plus; cependant, le transistor supérieur est bloqué deux fois pendant la même période, augmentant les pertes de blocage. Le mode TCM réduit un cycle de commutation du transistor supérieur en rendant le courant négatif. Le principal inconvénient de cette dernière solution est l'ondulation de courant augmentée, qui s'accroît à faible charge. Le contrôle de fréquence associé au mode TCM est fréquemment utilisé car il réduit l'ondulation de courant pour les faibles charges en augmentant la fréquence de commutation.

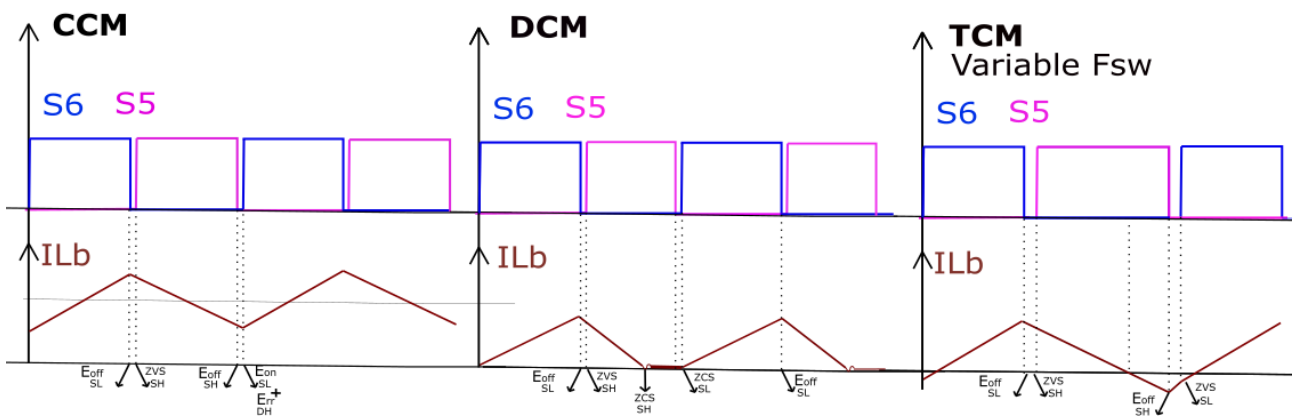


Figure R 49: Conditions de commutation en modes de conduction continue, discontinue et triangulaire.

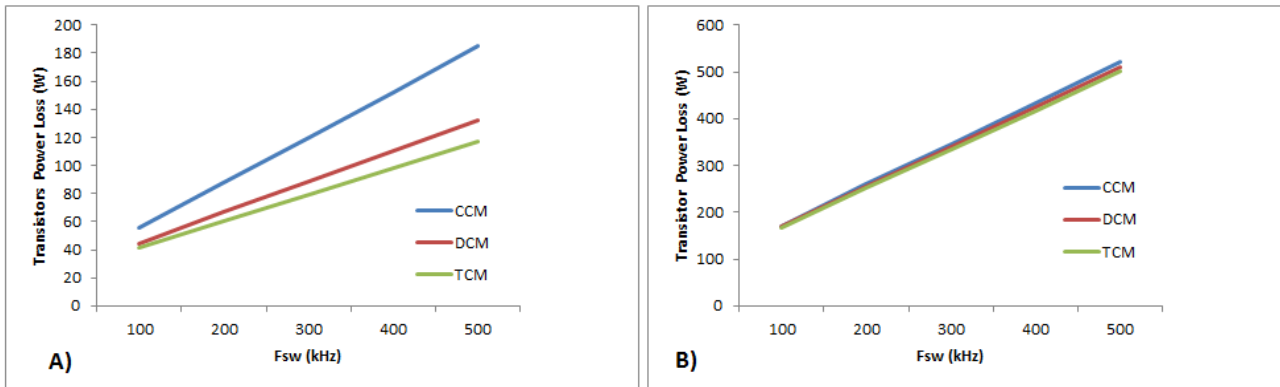


Figure R 50: Pertes estimées dans les transistors en utilisant les données des fabricants a) Côté haute tension avec 7 kW, $V_{HV} = 240-480$ V, SiC MOSFET (C3M0075120J). b) Côté basse tension avec 3.5 kW, $V_{LV} = 12-16$ V, Silicon MOSFET (2x IPB180N08).

Les pertes de conduction dans le côté BT sont très importantes, mais sur le côté haute tension, les pertes de commutation et de conduction sont également importantes. Cet impact, cependant, peut être minimisé avec l'utilisation de MOSFETS SiC. La Figure R 50 montre la différence entre les côtés HT et BT concernant l'estimation des pertes dans les transistors pour les trois modes de fonctionnement, CCM, DCM et TCM.

Côté HT, les pertes de commutation ont plus d'impact sur le rendement du convertisseur et la comparaison des modes de conduction permet de choisir le meilleur résultat. Même ainsi, dans les applications automobiles, même pour le côté BT, il est toujours important de réduire les surtensions et limiter leurs variations pour obtenir une meilleure fiabilité et robustesse accrue. Le circuit de la Figure R 51, [15] - [16], est proposé alors pour atteindre ces caractéristiques.

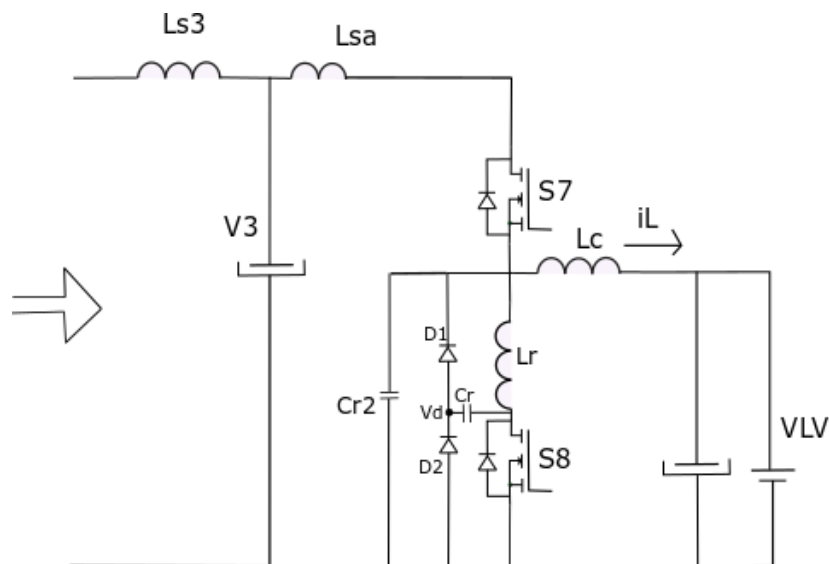


Figure R 51: DC-DC réversible non isolé connecté entre le convertisseur à trois entrées/sorties et la batterie BT incluant un circuit amortisseur LCD pour ralentir les transitions de tension et de courant.

Les formes d'onde typiques peuvent être visualisées sur la Figure R 52 pour l'application côté basse tension. La tension et le courant nominaux sont augmentés. Néanmoins, ce type de solution présente le minimum d'impact sur la conception du côté BT.

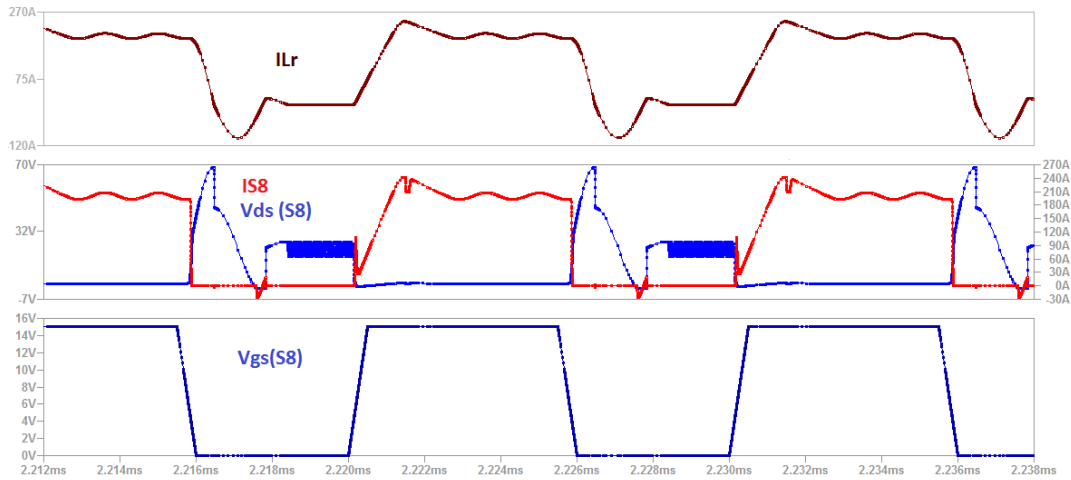


Figure R 52: Courants i_{Lr} , i_{Ds} , tensions V_{ds} , V_{gs} dans le mode Boost avec un snubber LCD.

Afin d'estimer le rendement complet de conversion pour les modes OBC et LDC, le demi-pont avec le snubber peut-être considéré au côté BT et le demi-pont en mode discontinu (DCM) pour le côté HV. Les paramètres du dimensionnement sont présentés au Tableau R 7.

Paramètres	Objectifs du côté HV	Objectifs du côté LV
Puissance	7 kW	3.5 kW
Tension moyen. En entrée	480 V _{DC} – 900 V _{AC}	20 V _{DC} – 38 V _{AC}
Tension de sortie minimale	240 V _{DC}	12 V _{DC}
Tension de sortie maximale	470 V _{DC}	16 V _{DC}
Fréquence de découpage	180 kHz	180 kHz
Ondulation de tension en sortie	< 1%	< 1%

Tableau R 7: Paramètres des convertisseurs DC-DC non-isolés pour les côtés HT et BT.

Les paramètres des convertisseurs additionnels choisis pour répondre aux objectifs du cahier de charge (voir le Tableau R 7) sont données au Tableau R 8.

Component	Valeur / Stress (HV)	Valeur / Stress (LV)
Fréquence	180 kHz	180 kHz
Puissance maximale	7 kW	3.5 kW
Inductance	9 uH	0.5 uH
Inductor max DC cur.	24 Arms	281 Arms
Inductance: Courant maximale	42 A peak	310 A peak
Inductance Volume	10.6 cm ³ (Toroid)	51.4 cm ³ (E core)
Inductance Pertes Max.	14 W	39 W
Capacité en sortie	10 uF	0.68 mF

Arrangement de condensateurs	2xUCY2H220MHD3TN	3xUBY2A221MHL+8xCKC21C104JW
Transistor Tension/Courant	16 Arms / 480 V	291 Arms/ 72 V
Transistor Reference	C3M0075120J	IPB180N08S4-02 (2 en parallèle)
Capacités de résonance C_{r1}, C_{r2}	-	1.35 μ F / 0.5 nF
Inductance de résonance L_r	-	64 nH
Clamp diodes D_1, D_2	-	32 V / 18 A

Tableau R 8: Spécification des convertisseurs DC-DC non-isolés.

En utilisant le processus de charge des batteries décrite sur la Figure R 53, le rendement de conversion est estimé sur la Figure R 54 pour les modes OBC et LDC.

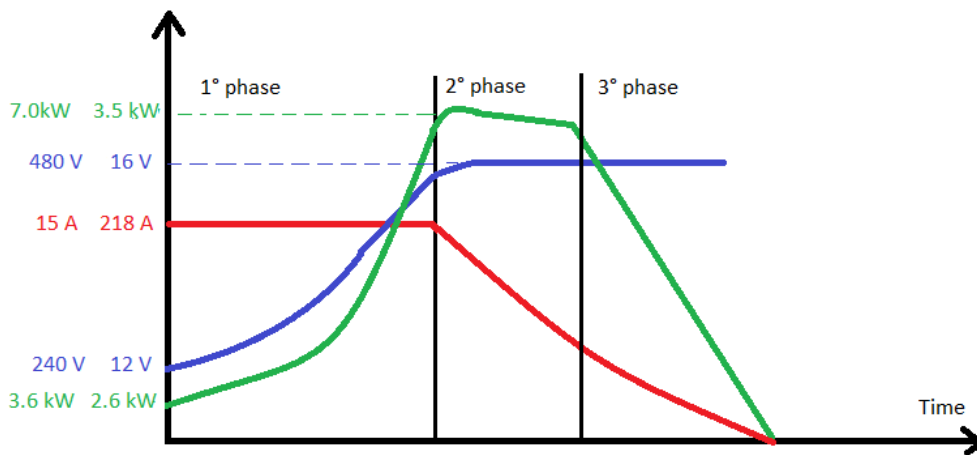


Figure R 53: étapes du processus de charge des batteries, tension, courant et puissance.

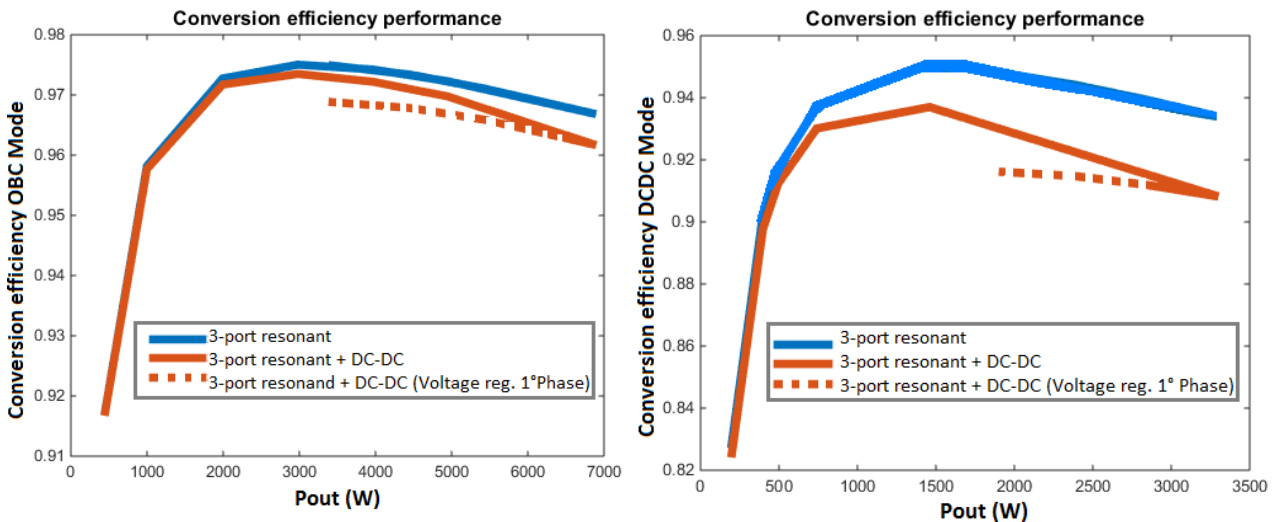


Figure R 54: Rendement estimé pour les conversions en mode OBC et LDC.

Les pertes par étage sont indiquées au Tableau R 9 et au Tableau R 10.

Bloc	Pertes	Valeur
Convertisseur résonant à 3 entrées/sorties	Dans les transistors	131.2 W
	Dans les grilles	4.5 W
	Dans le transformateur	111.12 W
	Dans les inductances filtrage	86 W
	Condensateurs de résonance	1.14 W
	Inductances de résonance	8.65 W
	Totales	342.61 W
DC-DC voltage regulation stage	Dans les transistors	26.43 W
	Dans les grilles	1.5 W
	Inductance buck/boost	14.17 W
	Dans le filtre de sortie	1.25 W
	Totales	33.35 W

Tableau R 9: Pertes par étage en mode OBC.

Bloc	Pertes	Valeur
Convertisseur résonant à 3 entrées/sorties	Dans les transistors	100.32 W
	Dans les grilles	6.5 W
	Dans le transformateur	54.42 W
	Dans le filtre de sortie	53 W
	Condensateurs de résonance	1.2 W
	Inductances de résonance	8.55 W
	Totales	224.12 W
DC-DC voltage regulation stage	Transistors	47.84 W
	Dans les grilles	1.1 W
	Inductance buck/boost	38.29 W
	Dans le filtre de sortie	28.48 W
	Totales	115.71 W

Tableau R 10: Pertes par étage en mode DC/DC (LDC).

Afin d'obtenir le rendement total pour l'OBC, un PFC réversible totem-pole est dimensionné. Pour cet étage, comme pour le demi-pont à la sortie du convertisseur à résonance, différents modes de contrôle peuvent être analysés pour trouver un compromis acceptable. En mode CCM, il n'est pas possible de faire fonctionner les transistors à zéro de tension. L'énergie de recouvrement reverse des diodes peut être élevée si des transistors en silicium sont utilisés. En mode DCM, les performances du facteur de puissance sont détériorées car le courant reste nul pendant un intervalle de temps plus long que le temps nécessaire à la transition de tension. Le mode CrCM réduit les pertes par commutation, augmente la densité de puissance et maintient un facteur de puissance moyen entre les modes CCM et DCM. Néanmoins, pour une puissance de 7 kW, le courant RMS est considérablement augmenté. Une analyse plus précise a été menée. Sur la Figure R 55, en mode CrCM, la valeur de l'inductance est réduite, permettant des commutations à quasi-zéro de tension. Il est clair que pour passer du mode CCM au CrCM, le gain obtenu pour les pertes de commutation ne doit pas être compensé par l'augmentation des pertes dans l'inductance.

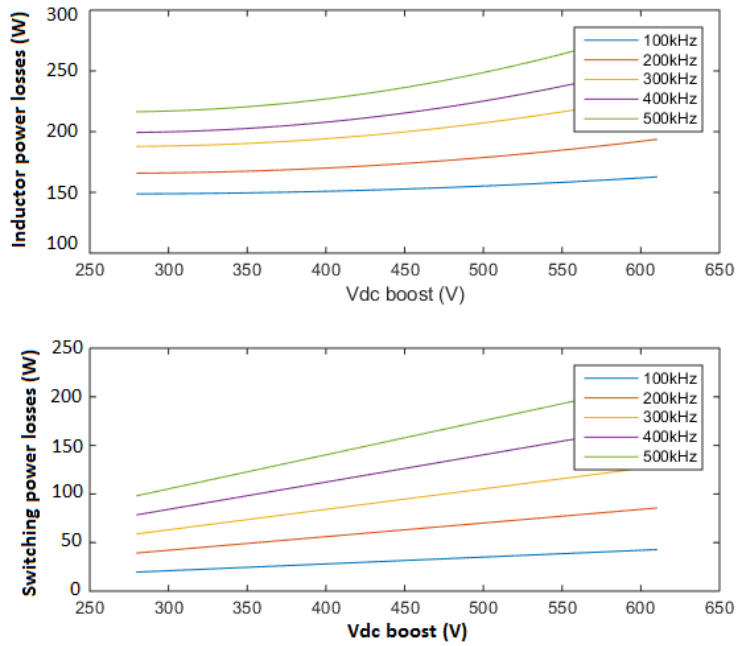


Figure R 55: Pertes de puissance dans l'inductance buck / boost et pertes de commutation dans les transistors (C3M0075120J) en fonction de la tension DC link pour différentes fréquences de commutation.

Compte tenu de la tension du convertisseur intermédiaire à résonance fixée à 480 V, les conceptions en CCM et CrCM sont comparées dans le Tableau R 11 pour le PFC totem-pole.

MODES	L_{nom} (μH)	ΔI (A)	Energie circuit magnétique (mJ)	Volume circuit magnétique (cm^3)	Pertes dans l'inductance (W)	Pertes dans les transistors (W)
CCM	100 μH	8.97	198	29.8	415	58.4
CrCM	30 μH	28.8	102	16.2	606	46.4

Tableau R 11: Comparaison de conception entre CCM et CrCM pour un PFC totem de 7 kW. La conception complète est présentée dans la section 6.5.4.

Le mode CCM présente moins de pertes. La simulation de ce circuit est présentée ci-dessous pour les modes G2V et V2G, en considérant le cas CCM. La Figure R 57 montre l'estimation des performances de conversion de l'OBC, y compris l'étage PFC commandé en mode CCM à 100 kHz.

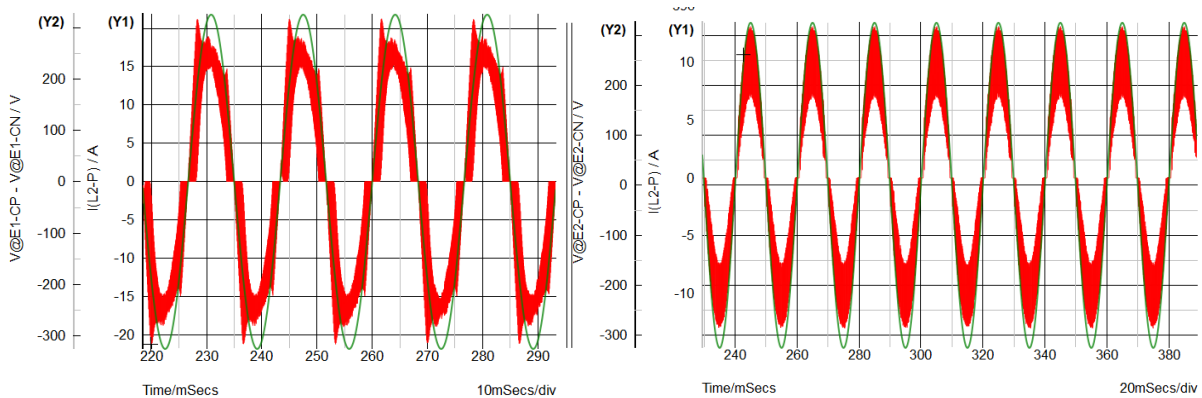


Figure R 56: Simulation de l'étage PFC : tension du réseau AA et courant dans l'inductance PFC dans les modes G2V et V2G, respectivement. $V_{dc} = 400$ V, $P = 5,0$ kW.

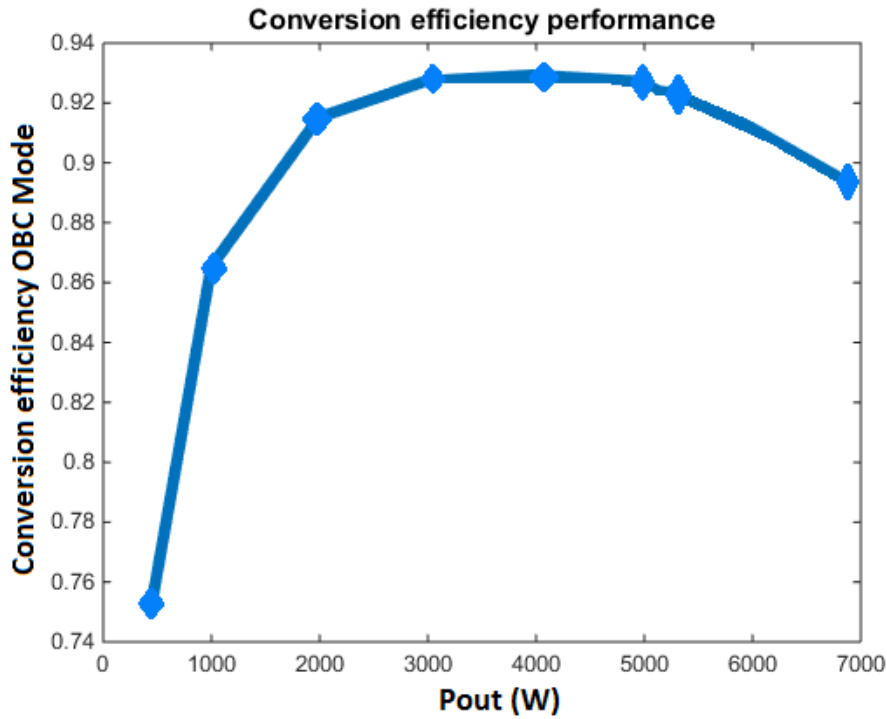


Figure R 57: Rendement global au cours du processus de charge de la batterie HV (prenant en compte les trois étages de conversion: PFC + convertisseur résonnant parallèle + étage de régulation de tension de sortie).

Finalement, comme le convertisseur DC/DC à trois ponts est commun aux modes OBC et LDC, une estimation du nombre de ses défaillances au niveau transistors et transformateur est présentée. Pour cela, nous avons considéré la méthode de fiabilité FIDES et le profil de mission illustré sur la Figure R 58.

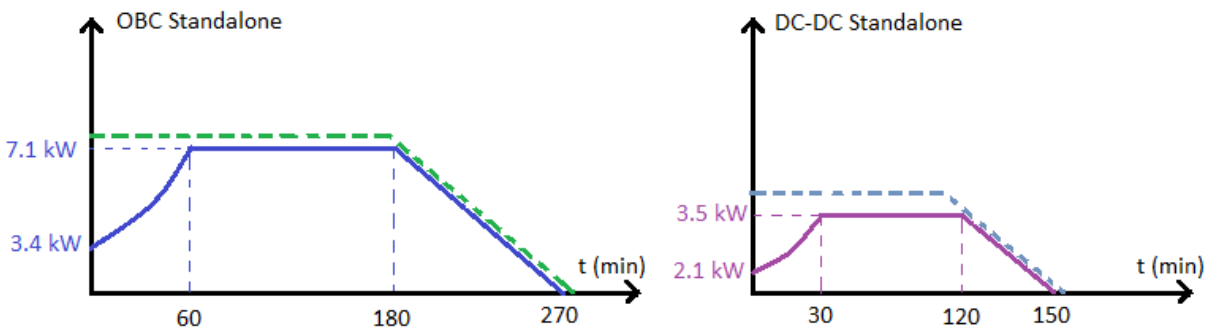


Figure R 58: Puissance de sortie utilisée dans le profil de mission pour le convertisseur parallèle à trois entrées/sorties dans les fonctions OBC et LDC.

Nous pouvons supposer que l'OBC est démarré une fois par jour et que le nombre de démarrages du convertisseur LDC est évalué en considérant le nombre de fois où le véhicule est conduit. Il est acceptable de considérer que le convertisseur LDC démarre au moins le même nombre de fois que le fonctionnement de l'onduleur de traction. Pour les niveaux de puissance discutés dans cette thèse, l'OBC fonctionne environ 3 heures par jour contre 8 heures pour le convertisseur LDC. Les taux de

défaillance obtenus avec la méthodologie FIDES sont exprimés dans un calendrier de profil annuel (8760 heures) où chaque phase décrite à la Figure R 58 doit être pondérée par sa durée 365 fois par an. Les transistors, le transformateur, les inductances de résonance et capacités films sont considérés dans cette analyse.

Pour intégrer les caractéristiques du convertisseur, le profil de mission demandé est inséré dans Simetrix, où le convertisseur est simulé pour les différentes conditions d'entrée. Le profil de puissance est codé dans l'environnement Octave pour contrôler la simulation en fonction du temps dans Simetrix et récupérer les informations après chaque cycle simulé, comme montre le la Figure R 59.

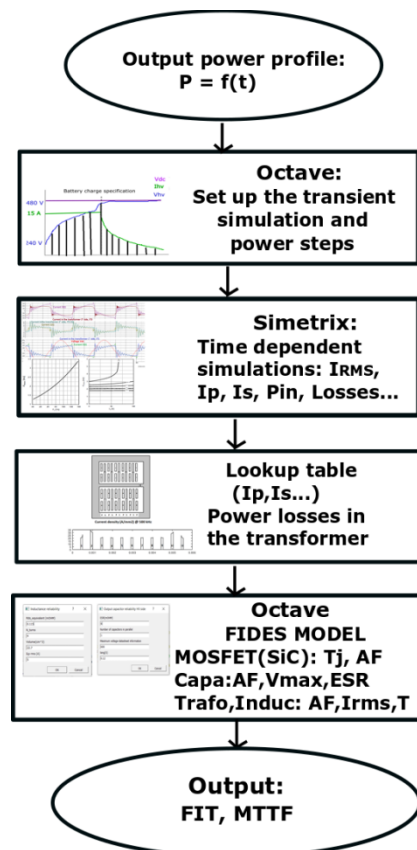


Figure R 59: Organigramme de la méthode pour intégrer le modèle de fiabilité avec des simulations transitoires temporelles.

Les résultats de la simulation, constitués des pertes et courant pour chaque transistor, et du courant dans les enroulements du transformateur primaire et secondaire, sont chargés dans Octave. Les modèles thermiques des interrupteurs de puissance et le modèle de fiabilité de tous les composants évalués sont utilisés pour déterminer le temps moyen de défaillance (MTTF) du convertisseur, comme présenté dans la Figure R 59. Le temps moyen de défaillance et les taux de défaillance dans le temps (FIT) sont présentés dans le Tableau R 12. Les transistors SiC sont utilisés dans les deux côtés haute tension, totalisant 8 transistors. Du côté basse tension, deux MOSFETS Si sont connectés en parallèle pour réaliser un switch. Il faut noter que l'étude de fiabilité n'est applicable que dans la plage pour

laquelle les composants sont qualifiés, et pour une plage de température ambiante comprise entre -55 ° C et 125 ° C.

Semiconducteurs HV	898.56
Semiconducteurs LV	367.58
Transformateur	21.38
Inductances de résonance	13.15
Inductances de lissage	18.52
Condensateurs de résonance	57.54
Condensateurs de sortie	29.90
FIT (Total)	1424.6
MTTF (années)	80.13

Tableau R 12: Taux de défaillance pour le convertisseur résonant à trois entrées/sorties.

Conclusion :

Dans le développement d'un étage DC-DC à haut rendement, la commutation douce était une condition préalable. L'architecture développée dans cette thèse, le convertisseur résonant parallèle alimenté en courant à trois entrées/sorties permet d'atteindre ces conditions. Cette architecture a été étudiée pour intégrer un chargeur embarqué de 7 kW et un convertisseur DC-DC de 3,5 kW pour charger la batterie BT auxiliaire. La cellule résonante LC en parallèle avec les enroulements du transformateur permet une commutation à tension nulle pour toutes les plages de puissance, et la structure est réversible dans tous les sens.

Le transformateur, une partie essentielle du convertisseur intégré, a été étudié au chapitre 4 et nous avons développé une structure planar. En raison de l'existence d'un courant élevé du côté basse tension et de la différence entre les batteries HT et BT, des spires connectées en parallèle sont nécessaires pour supporter le courant élevé du côté BT. Cependant, les effets indésirables à haute fréquence modifient la distribution du courant à l'intérieure des couches connectées en parallèle. Afin d'éviter une mauvaise distribution du courant, ce phénomène a été étudié en détail. La solution analytique des lois d'Ampère et de Faraday formulées à l'intérieur de chaque couche conductrice associée aux conditions de test externes a été utilisée dans une routine Matlab pour résoudre ce problème. Grâce à ce calcul rapide, il a été possible d'évaluer différentes configurations pour concevoir le transformateur à trois enroulements et de sélectionner la meilleure solution. Par rapport à une analyse par éléments finis 2D, les résultats fournis par ce calcul rapide étaient très proches.

Malgré les efforts déployés pour minimiser l'inductance de fuite, des oscillations parasites se superposent aux formes d'onde de tension sinusoïdale résonante affectant les performances du convertisseur. Mais ces oscillations peuvent être amorties comme indiqué au chapitre 5. Lors des essais, il a également été vérifié que la capacité parasite du transformateur modifiait la fréquence de résonance

du convertisseur, en diminuant sa valeur. Néanmoins, c'est une caractéristique intrinsèque de la configuration entrelacée utilisée lors de la conception du transformateur planar pour minimiser l'énergie de fuite.

Proposition d'améliorations

Malgré nos efforts pour développer un transformateur selon les normes pour véhicules électriques, certaines améliorations sont encore nécessaires. La conception du transformateur contenant trois PCB's et 24 couches se traduit par une résistance DC un peu forte et quelques difficultés lors de l'assemblage. Par conséquent, nous recommandons de réduire les rapports entre nombres des spires, comme mentionné à la fin du chapitre 4. Cette réduction peut être effectuée en divisant le transformateur en deux ou trois noyaux magnétiques plus petits et en connectant les enroulements en série du côté HT ou en parallèle du côté BT. Avec cette stratégie, les performances du transformateur et du convertisseur résonnant sont améliorées. De plus, avec une capacité parasite plus petite, la fréquence de commutation du convertisseur peut être augmentée et nous pouvons profiter de sa pleine capacité opérationnelle ZVS dans la conception d'un convertisseur plus compact.

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List of Abbreviations and symbols

OBC	On-board charger
LDC	Low voltage battery charger, isolated DC-DC converter
V2G	Vehicle to Grid
G2V	Grid to Vehicle
HV	High voltage
LV	Low voltage
PFC	Power Factor Correction
V _{dc}	DC link voltage
LLC	Isolated DC-DC series parallel resonant converter
LC	Isolated DC-DC series resonant converter
ZVS	Zero voltage switching
ZCS	Zero current switching
DAB	Dual active bridge converter
TAB	Triple active bridge converter
PSFB	Phase-shift full-bridge converter
GaN	Gallium-Nitride wide bandgap semiconductor
SiC	Silicon Carbide wide bandgap semiconductor
WBG	Wide bandgap
EMI	Electromagnetic interference
CCM	Continuous conduction mode
CrCM	Critical conduction mode
DCM	Discontinuous conduction mode
SoC	State of charge
ϕ_{AB}	Phase-shift angle between ports A and B
ϕ_{BC}	Phase-shift angle between ports B and C
N _P	Transformer primary side number of turns
N _S	Transformer secondary side number of turns
J _K	MMF - Magneto-motive force
FEM	Finite element method
FEA	Finite element analysis
\vec{B}	Magnetic flux density in Tesla
\vec{H}	Magnetic flux intensity in A/m
\vec{E}	Electric field intensity in V/m

MLT Mean length turn

TIM Thermal Interface Material

TCM Triangular conduction mode

MTTF Mean time to failure

FIT Failure rate in time

1- Introduction

1.1- Background

Nowadays, the automobile industry for electric vehicles is in continuous progress. The electric vehicle architecture with its powertrain system is very similar from one constructor to another. Generally, it can be described as in Figure 1-1: a high voltage propulsion battery (HV battery), a three-phase inverter to drive the electric motor, a low voltage battery (LV battery) historically in a lead-acid technology of 12 V to supply energy for other board equipment, an isolated DC-DC converter, and the main battery charger. The electric motor can be asynchronous with squirrel cage or synchronous, often developed with permanent magnets or wound rotor [1]. The isolated DC-DC converter charges the LV battery with the energy from the HV battery and is usually operated when the vehicle is driven. The HV battery charging occurs at higher power levels compared to the isolated DC-DC converter and thus has a standalone on-board (OBC) or off-board charger. When off-board, the charging is faster, but it requires a dedicated charging station, whereas the on-board chargers present some facilities, such as the conventional electrical grids utilization, more convenient for charging the vehicle at home, offices, or parking garages.

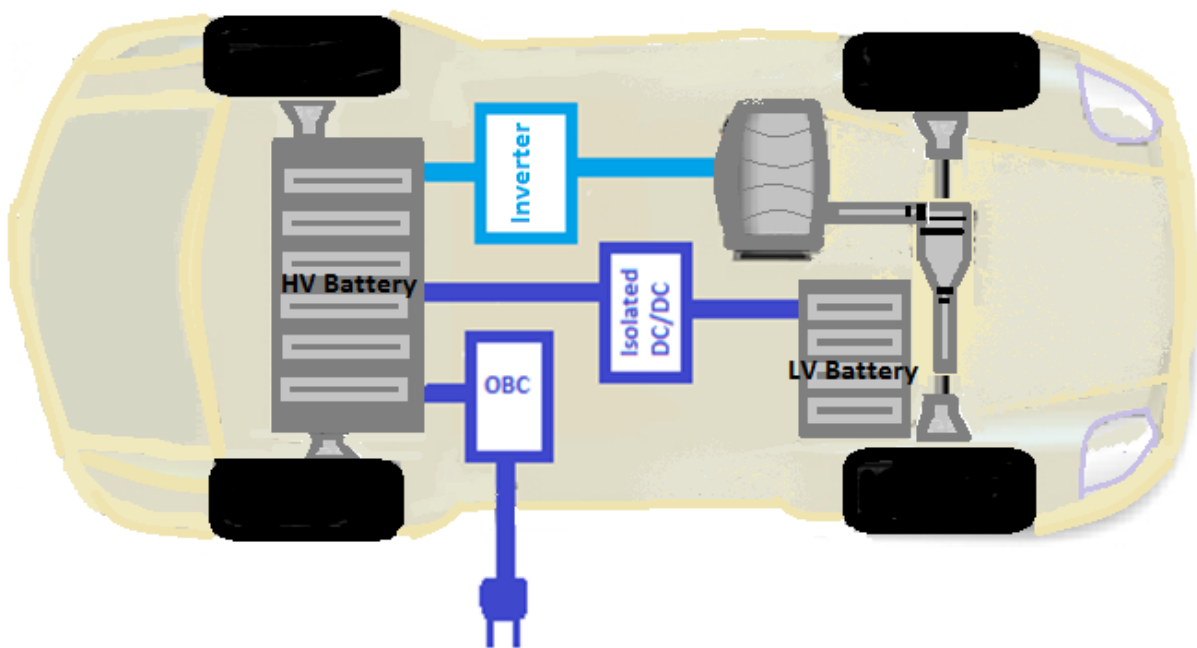


Figure 1-1: Typical architecture of an electric vehicle with the main on-board power electronic converters: Inverter, on-board charger (OBC) and isolated DC-DC converter.

Although the similarities in the powertrain architectures, each constructor determines the requirements concerning the power inverter, the DC-DC converter, the on-board charger, and the HV battery.

Therefore, each automobile supplier, such as Valeo or Valeo-Siemens, proposes its own solution to answer a request for quotation.

The DC-DC converter and the on-board charger, when compared to the inverter, are transparent for the user since they do not directly affect the vehicle driven performance. With the continuous progress in V2G applications and the demand for faster chargers, the on-board chargers are slowly becoming more important from the user point of view. Even so, these two power converters need to be strategically placed inside the vehicle and represent additional cost and volume for the constructors. The idea of developing a single product with thermal autonomy in order to replace both products represents an opportunity for this industry.

This dissertation focuses on the integration of the DC-DC converter between the HV and LV batteries, with the on-board charger. In this integration, the first idea is to reduce the number of components by sharing existing structures. The main challenge will be to keep a high efficiency for both implemented functions. Figure 1-2 shows a simplified structure of an on-board charger and DC-DC converter. As can be seen, after the Power Factor Correction stage (PFC), the converters have similar structures, and both are connected to the HV battery. The decision to share a component present in both structures must respect at least the converters standalone operations and include a third situation: the on-board charger operation when the vehicle is stationed, the DC-DC converter standalone operation when the vehicle is driven and stationed. Furthermore, bidirectional power flow capability can be demanded in both converters. If we look at the advances in the smart-grid electrical systems, the vehicle to grid (V2G) operating mode becomes a requisite in the case of the on-board charger. In the DC-DC converter case, it allows the pre-charging of the HV side, which can increase the product's value.

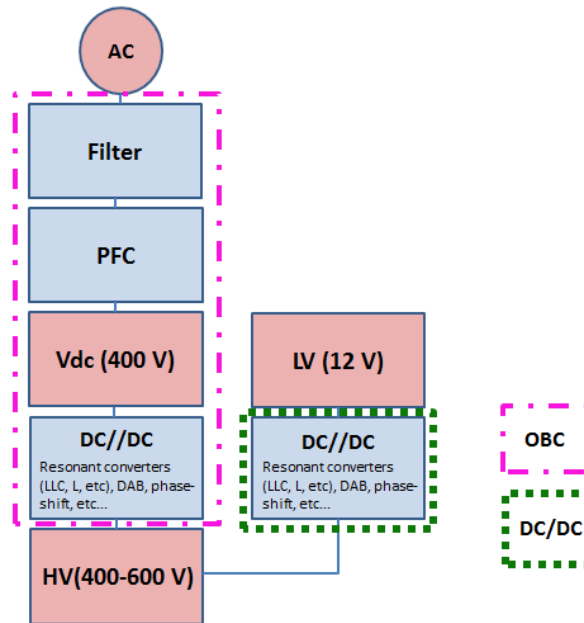


Figure 1-2: Diagram presenting the main parts of a two-stage on-board charger (OBC) and a DC-DC converter.

In order to better understand the solutions that could be adopted to develop both converters, we focus now on the characteristics of both standalone structures.

1.1.1.1- Standalone DC-DC converter

The DC-DC converter is used to manage power into the LV battery thanks to the HV battery. This LV battery is used for additional utilities, like stop, start, and diagnostic functions. For safety reasons, the DC-DC converter provides galvanic isolation between both batteries, and its power generally varies between 1.5 and 3.5 kW, depending on the constructor. For improved conversion efficiency and higher power density, soft-switched converters are widely implemented, such as phase-shift, LC series, and LLC resonant converters.

A previous thesis [3], in 2014, focused on a LLC converter development for this specific application. The converter was designed for 2.5 kW for a wide voltage range, between 220 and 410 V. Despite the difficulty in keeping a small current ripple on the LV side, the proposed solution achieved an efficiency of 95 %.

In [4], a novel converter topology, based on a current-fed buck Flyback-Forward converter, was also proposed in this application to attempt a wide voltage variation. Like the LLC resonant converter, the current-fed buck Flyback-Forward also has Zero Voltage Switching (ZVS) feature, even under light load conditions. Compared to the LLC resonant and, for the same HV/LV conversion application, the Flyback-Forward allows the current ripple reduction and thus the size of the output filter. These two prototypes are compared to a full-bridge phase-shift topology for the same unidirectional DC-DC

application in Table 1-1: Examples of DC-DC converters developed by Valeo in the last years. Sources: [3], [4].

Topology	Phase-shift	LLC resonant	Current-fed Buck Flyback-Forward
Power level	2.5 kW	2.5 kW	2 kW
VH voltage (V)	400 V	220-410 V	170-470 V
LV voltage (V)	14 V	12-16 V	9-16 V
Min. Power Density	0.61 W/cm ³	1 W/cm ³	1.43 W/cm ³
Efficiency (%)	92 %	95 %	95 %

Table 1-1: Examples of DC-DC converters developed by Valeo in the last years. Sources: [3], [4].

The power density and voltage range were gradually increased. The main difference between the DC-DC converters presented in Table 1-1: Examples of DC-DC converters developed by Valeo in the last years. Sources: [3], [4].

able1-1 and the one developed in this thesis is the bidirectional power flow. This characteristic allows the low-voltage battery utilization to pre-charge the high voltage side and support other systems when the electrical grid is not available.

1.1.2- Standalone On-board charger (OBC)

The on-board charger allows power up the propulsion battery by plugging the electrical grid. The classification between on-board and off-board considers mainly the power levels, because of the limited space available inside the vehicles to place these converters. According to the Society of Automotive Engineer, the charger types can be classified, as shown in Table 1-2, [5].

For single or three-phase charges, their architectures can also be defined as single or two-level, according to the number of conversion stages, as illustrated in Figure 1-3. In a single-stage, the rectifier, together with the isolated DC/DC converter, compensates the electrical grid's power factor. The current ripple pulsed at twice the frequency of the electrical grid is passed to the battery. Depending on the battery technology and on some automobile constructors, pulsed current, even at a small frequency around 100 Hz, is not acceptable in most cases.

Power Level	Type	Power Rate	Time	Charging's Station
Level 1	On-board (1Ø) 120 Vac (USA) 230 Vac (Eur)	1.4 kW (12 A) 1.9 kW (20 A)	4- 11 hours 11- 30 hours	Home or office
Level 2	On-board (1 or 3Ø) 240 Vac (USA) 400 Vac (Eur)	4 kW (17 A) 8 kW (32 A) 19.2 kW (80 A)	1-4 hours 2-6 hours 2-3 hours	Private or public stations
Level 3	Off-board (1 or 3Ø) Vac or Vdc supply	> 50 kW	< 1 hour	Dedicated

Table 1-2 : Electric vehicles charging types. Sources: [2] and [5]

In the two-stage architecture, the rectifier output voltage is pre-regulated, usually by a boost converter, and a bank of capacitors compensates the low-frequency current ripple. This solution decreases the current and voltage stresses on the isolated DC-DC converter, but requires electrolytic capacitors, with a limited lifetime and a small energy density. A solution to surpass these drawbacks consists of the Active filter utilization directly connected to the DC voltage link. This filter allows a significant gain in power density and lifetime, by reducing the DC link capacitor, and replacing the electrolytic by other technologies, such as ceramic capacitors. The low-frequency current ripple is usually synthesized under high-frequency switching and passed to another passive element, disassociated from the DC link, able to see a larger voltage and/or current variation, resulting in need of smaller storage capacity. The study of an active filter is outside our scope, but more details can be viewed at [6], where an active filter solution in association with a single-phase rectifier reduces the total capacitor volume.

In the second stage, the DC-DC isolated converter adapts the V_{dc} voltage link to the battery requirements, and soft-switching is essential to keep a high efficiency, as for the high/low voltage application. In [7], a high power density bidirectional on-board charger has been developed, based on the symmetrical series LC resonant converter. To achieve 12 kW/L, the author uses GaN transistors to switch at 500 kHz and under Zero-Current Switching (ZCS) conditions allowing to keep high conversion efficiency, around 95%.

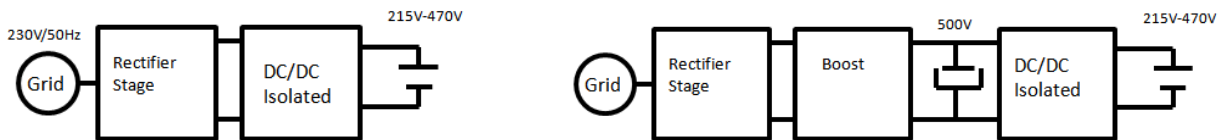


Figure 1-3: a) A single-stage charger structure. b) A two-stage charger structure.

This dissertation focuses on a single-phase, Level 2, bidirectional two-stage on-board charger with a maximum power of 7 kW.

The converter final electrical parameters, including DC-DC and OBC converters, are resumed in Table 1-3. The batteries and the electrical grid must be isolated from each other.

	AC grid	Batteries	HV	LV
Voltage (VRMS)	85 – 265	Voltage range	240 - 480 V	12 - 16 V
Frequency (Hz)	50 - 60	Nominal Volt.	450 V	14 V
Pmax (kW)	7 kW	P (kW) (+/-)	0 - 7 kW	0 - 3.5 kW
Imax (ARMS)	32	IDC max (A)	17.5 A	250 A

Table 1-3: Electrical parameters of the converter combining the OBC and DC-DC functions.

In order to attempt the V2G operating mode, a bidirectional AC/DC PFC converter must also be proposed for a single-phase, two-stage converter. We cite below the main single-phase structures allowing power factor correction and reverse power flow operation. This stage can be classified as a full-bridge rectifier and bridgeless converters. The most commonly used rectifier structure is presented in Figure 1-4-a. It consists of a diode bridge rectifier followed by a boost converter for the power factor correction. The bidirectional version of this same structure is obtained by replacing the diodes by bidirectional switches, as presented in Figure 1-4-b [27].

During the G2V operation, the diode bridge rectifies the voltage and the switch S5 is controlled in boost mode following a sinusoidal current reference in phase with the voltage. During the V2G operation mode, the converter needs to step-down the voltage, and the switch S6 is controlled, with the complement of the S5's body diode. The bridge connected to the grid is controlled in order to provide a sinusoidal current, 180° out of phase with the grid voltage, so when V_{in} is positive, S1 and S4 are turned on, and when V_{in} is negative, S2 and S3 are turned on. An overlap time during the switches transition is required for the inductor current circulation.

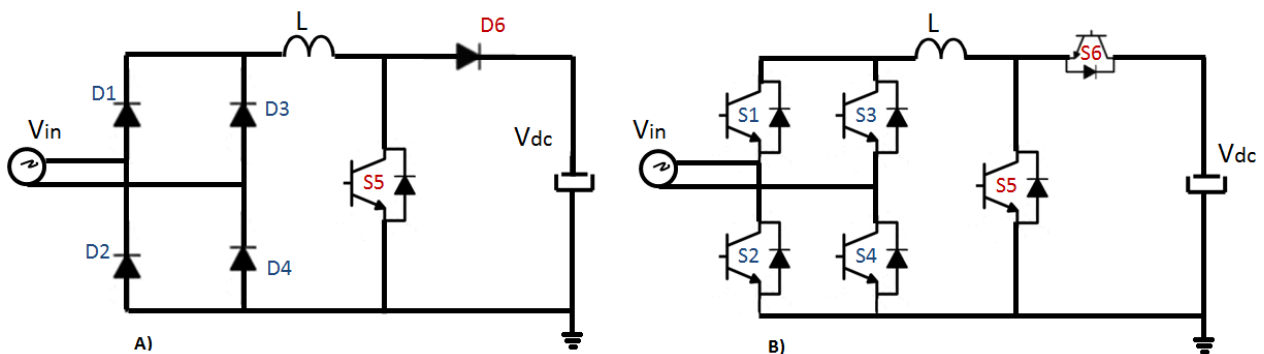


Figure 1-4: a) Conventional boost PFC converter. b) Bidirectional Boost/Buck PFC converter.

During a half-cycle of the electrical grid, at least two transistors or diodes close the current path allowing the negative of the AC source to be in contact with the DC ground reference. A bridgeless PFC converter, nevertheless, does not have a full-bridge operating at the grid frequency. Instead, the rectification and the power factor correction are made with the same switches during a half-period. An example is the Bridgeless Totem-pole converter in Figure 1-5-a. During the G2V mode, S4 is controlled as in the boost mode. The switch S2 remains ON during the positive half-cycle of the electrical grid, and S1 is ON during the negative half-cycle while the switch S4 is controlled at high-frequency in boost mode. During the V2G mode, the switches S1 and S2 alternates at the electrical grid frequency, and the switch S3 is controlled at high-frequency in buck mode. Unlike conventional bidirectional PFC, a single switch remains on during a half-cycle to close the current path, which decreases the conduction power losses. For this same reason, during an entire half-cycle, the V_{dc} link

ground is not directly connected to the electrical grid reference, which usually deteriorates the EMI aspects increasing the AC filter size. The produced frequency spectrum is similar to the bipolar modulation in single-phase inverters, with the first, second, and odd harmonics containing their sidebands. A solution to reduce the EMI could be the use of an interleaved totem-pole bridgeless converter, as in Figure 1-5-b. The addition of a second-leg delayed of 180° from the first high-frequency controlled leg allows the elimination of the second harmonic in the frequency spectrum, reducing the size and power losses in the inductance and the output current ripple.

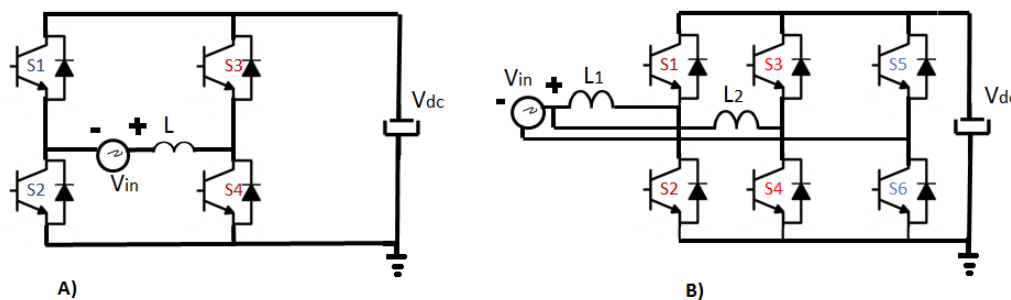


Figure 1-5: a) Bridgeless Totem-pole PFC converter. b) Bridgeless Interleaved Totem-pole PFC.

The conventional but also the bridgeless structures can be regulated on continuous (CCM), critical (CrCM), or discontinuous (DCM) conduction modes, as in the unidirectional AC-DC PFC converter [28]. As well known, the CCM presents higher switching power losses, but in some cases, it can be preferred than CrCM or DCM to reduce the power losses in the inductance depending on the maximum output power. Therefore, the control mode is a trade-off between several aspects such as, power factor, conduction losses, switching power losses, and EMI.

1.2- Discussion on existing solutions

In this section, we check the existing solutions combining OBC and DC-DC converters.

One of the solutions to include both of them into a single topology is presented in Figure 1-6, [8] and [9]. This solution is composed of a single high-frequency transformer and a mechanical switch “M” to alternate the operating modes between OBC and DC-DC converters, this last one referred by the authors as LDC.

In OBC mode, the first Front-end full-bridge converter operates as an AC-DC PFC converter, and the isolated DC-DC stage operates with phase-shift control in the primary side and synchronous rectification in the secondary side. ZVS is ensured by dead-time, even if, under light load conditions, the conversion performance decreases. The V2G operation is also present in this solution.

In the DC-DC function, the switch M is connected to position “a” to charge the auxiliary battery. Therefore, the First Front-end Full-bridge is operated as a Buck converter.

The same structure without additional elements, except by the switch M, executes both functions. The inductors in the Front-end full-bridge play three roles: the Boost PFC operation, the AC filter for the current in V2G operation mode, and the Buck inductor for charging the auxiliary battery. To perform the three functions and because of the difference on the current level, a trade-off between the features is required to adapt the inductor. The practical results show a small efficiency for the operation in DC-DC mode to charge the auxiliary battery. In this mode, the Front-end first full-bridge operates with increased current stress under hard-switching conditions.

At last, the ground reference used usually connected to the vehicle chassis is the LV battery ground, whereas, during OBC mode (G2V or V2G), the converter is floating with this architecture. One of the drawbacks is the impossibility of operating both functions together, without the charge of the HV and LV (auxiliary) batteries simultaneously.

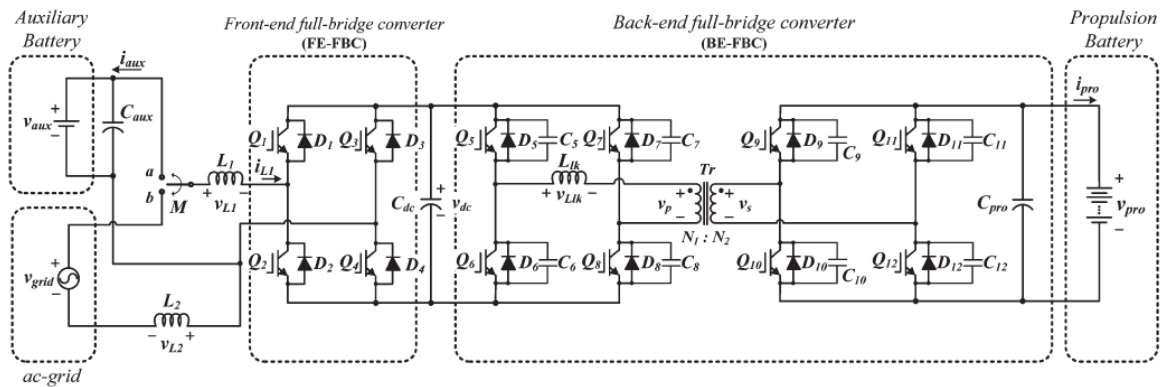


Figure 1-6: One of the proposed converters combining OBC and DC-DC converters here called LDC. - S. Kim and F. Kang [8].

In [10], a different solution is proposed. Part of the DC-DC converter used to charge the auxiliary LV battery, in Figure 1-7, is controlled as an Active filter during the charging of the HV battery in the OBC mode. The primary side of the DC-DC isolated converter is connected with passive elements, L_{aux} and C_{aux} , by changing the G switch position to compensate low-frequency oscillations (at 100 or 120 Hz), naturally present in the instantaneous input power. This solution constitutes a single-stage charger, as presented in Figure 1-3-a, where the PFC boost converter regulates the HV battery in its entire voltage range. With this feature, the charger needs to be adapted to connect the electrical grids from different countries, with voltage levels such as 85, 230 and 260 Vac, but also reach regular HV battery voltage range while keeping high conversion efficiency.

In the DC-DC mode, to charge the LV battery, a full-bridge phase-shift with a current doubler on the secondary side is used. The switch G connects the primary side to the inductance L_k , and the phase-shift control regulates the LV battery voltage with ZVS.

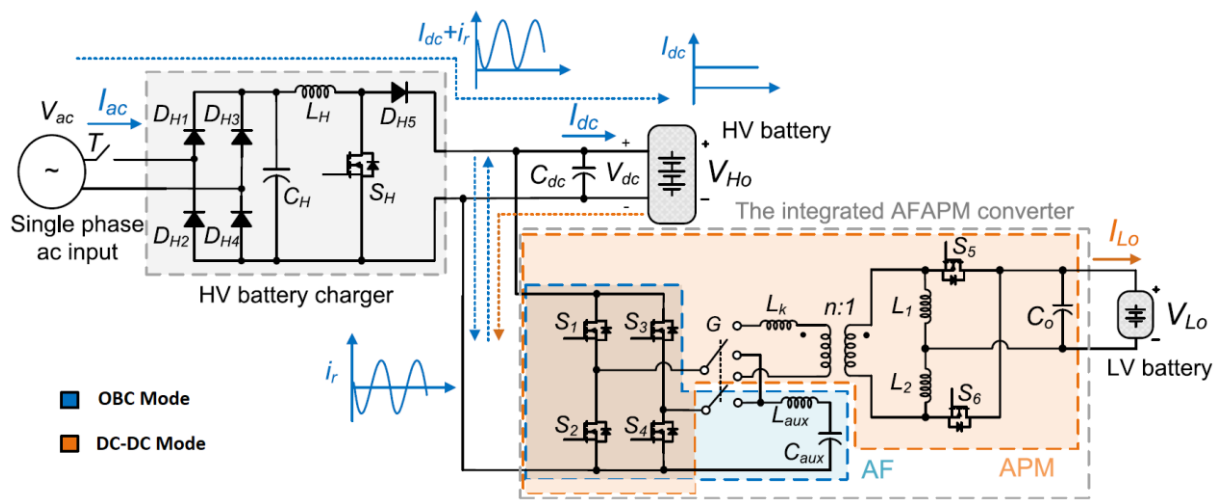


Figure 1-7: Integrated converter with OBC, DC-DC converter functions, and Active filter. - R. Hou and A. Emadi [10].

In Figure 1-8 [11], a variation of the previous solution is shown. This solution replaces the Relay G present in Figure 1-7 by operating each arm of the full-bridge primary's side as a buck converter, regulated for the compensation of the second-order low-frequency harmonic present in the OBC operating mode. The pulsating energy is mainly stored in the capacitor C_r . During the DC-DC mode, the converter is operated as a Dual Active Bridge converter (DAB), thus at light load, ZVS conditions are no longer available.

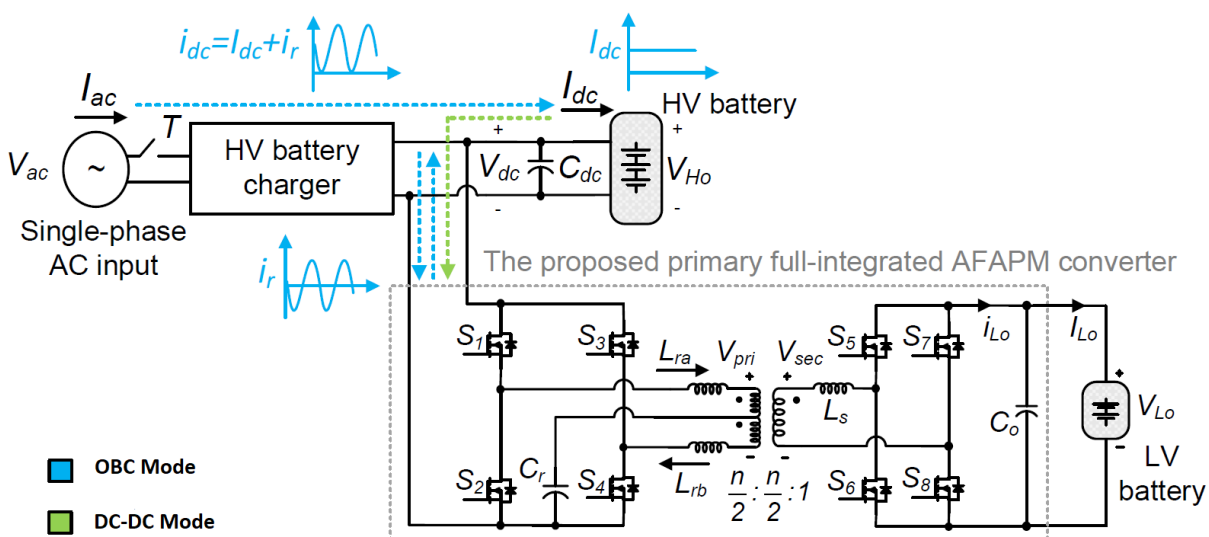


Figure 1-8: Integrated converter with OBC, DC-DC converter, and Active filter functions. - R. Hou and A. Emadi [11].

In [12], Figure 1-9, the author proposes the DAB converter utilization as an active-filter, instead of the Buck used in [11]. During the LV battery charge, the DAB converter is controlled as usual, with SPS (single-phase shift). During the OBC mode, the secondary side of the DAB is controlled by its duty cycle to assimilate the second-order component of the instantaneous input power, operating as

an Active filter. In this solution, the output capacitor C in parallel to the LV battery filters the high-frequency harmonics in the DC-DC operating mode (conventional DAB operation) and assimilates the low-frequency harmonic in the OBC operating mode.

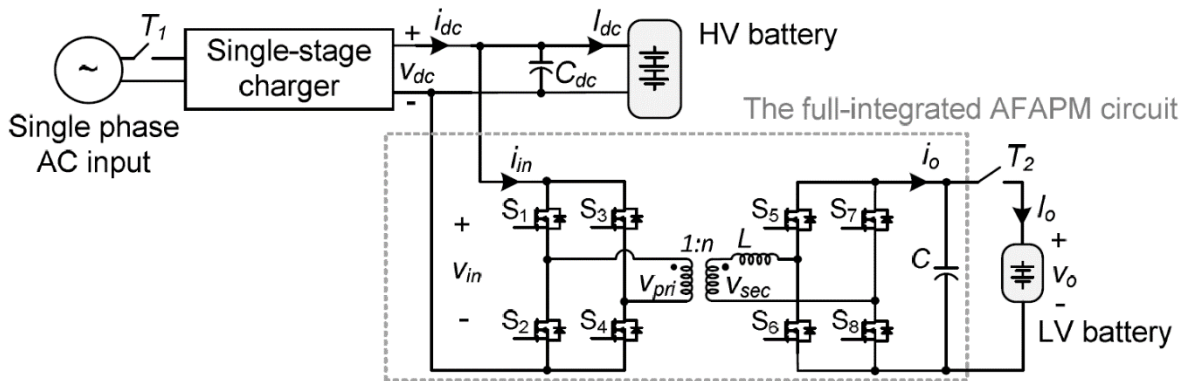


Figure 1-9: Integrated converter with OBC, DC-DC converter, and Active filter functions using DAB. - R. Hou and A. Emadi [12].

Figure 1-10 shows an alternative solution proposed in [13]. The converter charges and discharges the traction battery by configuring the switches SW1 and SW2, respectively, in close and open states. The bidirectional AC-DC stage is synchronized to the electrical grid using a PLL with active and reactive power references to regulating the power factor. The V_{dc} voltage is regulated with a buck converter to charge the traction battery, while this stage is used in boost mode in the V2G operation. It is a single-stage charger without isolation.

During the DC-DC operation to charge the auxiliary battery, switches SW1 and SW2 are respectively, in open and in closed states. The reversible DC-DC converter, in Figure 1-10, is in standby mode to apply the voltage directly from the traction battery to the DC link. The full-bridge with a center-tap transformer is controlled to charge the auxiliary battery only under constant voltage condition, by measuring its state of charge (SoC). Although this solution does not consider galvanic isolation between the electrical grid and the traction (HV) battery, its simplicity allows a cost reduction, and their use may be possible in some countries where the galvanic isolation is not mandatory.

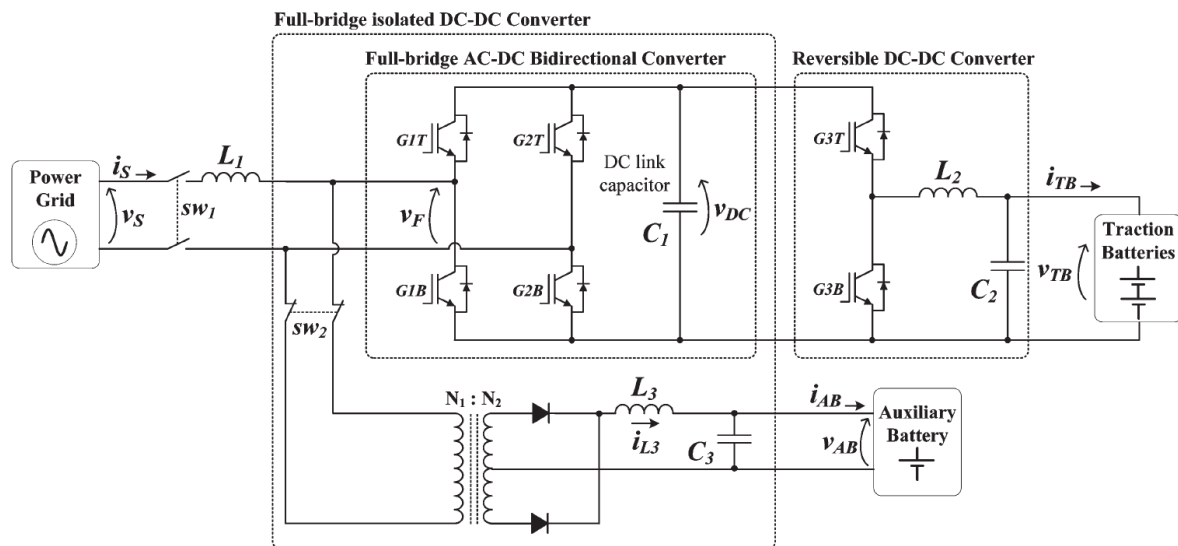


Figure 1-10: A bidirectional charger for the traction batteries and a unidirectional DC-DC converter to charge the auxiliary battery.-[13] J. G. Pinto, V. Monteiro, H. Gonçalves, and J. L. Afonso.

Figure 1-11 shows one more solution proposed in [14]. Figure 1-11-a shows the main configurations allowing the charging of the HV and LV batteries. The full-bridge phase-shift is used to charge the HV battery from the V_{dc} voltage (pre-regulated by an AC-DC PFC stage), and a half-bridge LLC resonant converter with a center-tap derivation on the secondary side to charge the LV battery. The center-tap, compared to the full-bridge, allows reducing the winding transformer current, increasing the conversion performance for the LV application. The architecture contains two independent transformers, and the detail of this integration is the use of the DC-DC LLC converter to extend the ZVS condition of the phase-shift full-bridge, as indicated in Figure 1-11-b. During the charging of the HV battery, the LLC structure is connected to the lagging leg of the phase-shift full-bridge and controlled to provide enough current to charge and discharge the MOSFET capacitances under low output conditions. The converter arrangements are modified between both modes by mechanical switches, from points Vc and Vd, to points Va and Vb, alternatively. This concept can be applied to other converters to increase the conversion efficiency and power density.

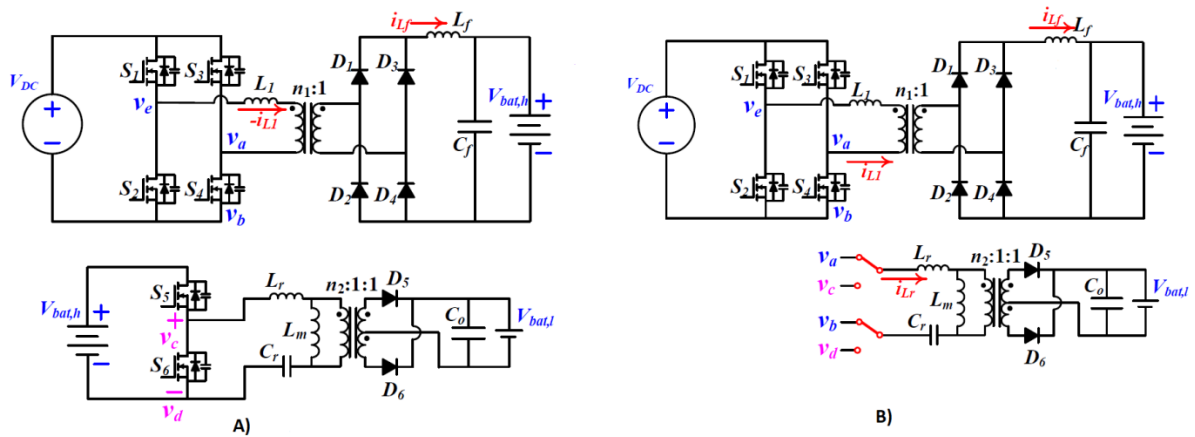


Figure 1-11: OBC Phase-shift and LLC DC-DC converter. a) Arrangement in DC-DC mode b) Arrangement in OBC mode- [14] H. Wang.

The solutions presented until now do not provide bidirectional power flow or full-isolation between the three voltage sources. However, these architectures are very useful to attempt reduced costs and improved power densities.

Figure 1-12 , [15], presents a solution where both batteries can be charged simultaneously from the electrical grid. The converter has, therefore, three operation modes: OBC, DC-DC to charge the LV battery from the HV, and OBC&DC-DC mode when the power flow coming from the electrical grid is shared between the two secondary transformer sides. The transistor placed on the center-tapped transformer winding is turned off during the OBC operating mode to block the induced voltage on this side and cancel power flow to the LV battery. When the electrical grid is disconnected, the integrated-FB (full-bridge) controls the voltage applied on the transformer, rectified on the center-tapped side, while the transistor Sa remains in ON state, allowing the LV battery charging. During the third mode, when both batteries are charged, Sa is PWM controlled in buck mode to regulate the LV voltage independently from the HV battery. In both standalone modes, the battery voltages are controlled with the duty-cycle applied in the full-bridges. ZVS occurs through the design of the series inductances as in the phase-shift full-bridge converter.

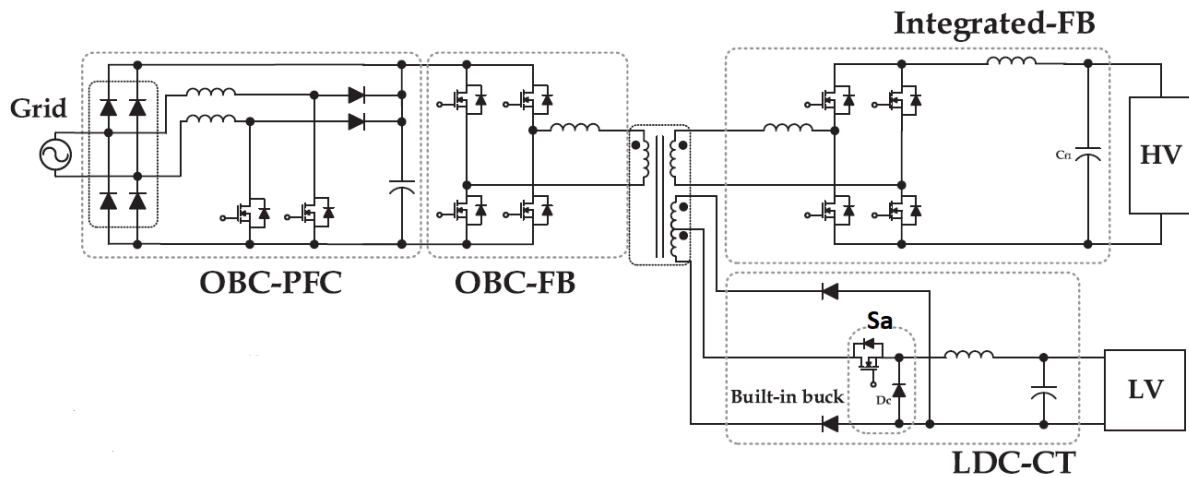


Figure 1-12: Converter combining OBC and DC-DC converter for LV battery with simultaneous operation mode. – [15] Y. Kim, C. Oh, W. Sung and B. K. Lee.

In [16], a solution using the three-phase inverter connected to the traction motor is used to charge the HV battery, and a third transformer winding allows charging the LV battery, as can be seen in Figure 1-13. The three arms from the 3-phase inverter are controlled in parallel in association with the BCONV half-bridge for power factor correction. The author uses SiC MOSFETS in the inverter. Other authors had studied the use of the inverter for charging the HV battery, as in SOFRACI, for example. The efficiency obtained, however, was impacted by the use of transistors adapted for the inverter operation, but not so much for the charging operation mode. In the solution illustrated in Figure 1-13, the use of the three arms in parallel can be applied to the low-frequency switched leg of a boost totem-pole PFC, while the high-frequency leg could be specifically designed with fast-switching transistors, increasing the conversion efficiency.

The DC-DC part of the integrated charger consists of a full-bridge connected to a three-winding transformer controlled with phase-shift control. Soft-switching is maintained, except for light load condition. The charging of the auxiliary battery occurs by controlling the Buck converter in the second transformer winding and can also occur during the vehicle's driving.

The solution contains the three main converters present in the power train and has a high potential to reduce volume and the number of components.

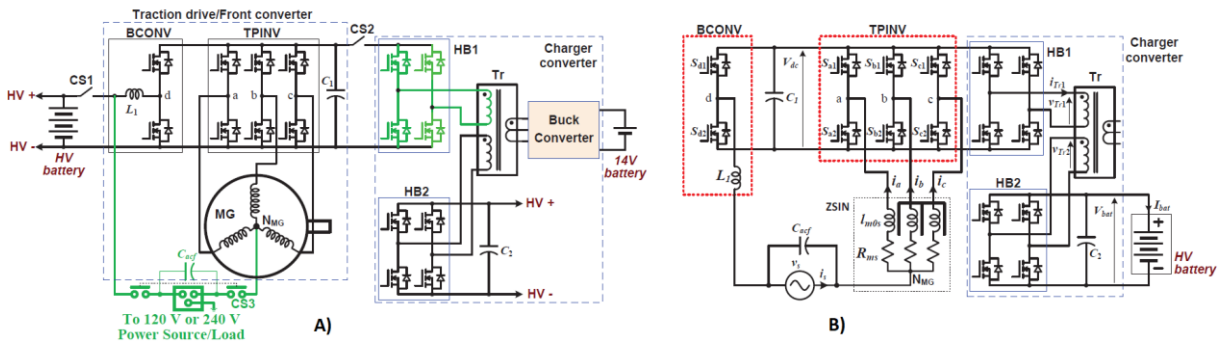


Figure 1-13: Integrated charger for HV and LV batteries, also including the 3-phase propulsion inverter. -[16] G. Su and L. Tang.

Figure 1-14 shows one more proposition, studied in [17], also allowing the simultaneous HV and LV batteries charging. The OBC structure can be classified as a single-stage because it does not have galvanic isolation. The output voltage from the diode's bridge rectifier is connected directly to the Buck-Boost PFC converter, allowing the power factor's control and the HV battery charging.

In this mode, the switch Qsel is in open-state. During the standalone DC-DC operating mode, the Qsel is closed, allowing the loop of the primary side full-bridge (transistors Q3B, Q2B, Q3C, and Q2C) with the resonant cell Cr_H and Lr_H, operating as a LLC resonant converter to charge the LV battery connected to the center-tapped side. In simultaneous mode, while the HV battery is being charged, Qsel remains open, and the half-bridge composed by transistors Q1_L and Q2_L allows part of the energy to pass to the LV battery at the same time. The capacitances connected in parallel to both transistors in this half-bridge, oscillate with the series and the new equivalent magnetizing inductance from the transformer's primary side. Therefore, the resonant converters allow better conversion efficiency in the DC-DC standalone mode, and also in the simultaneous operation mode.

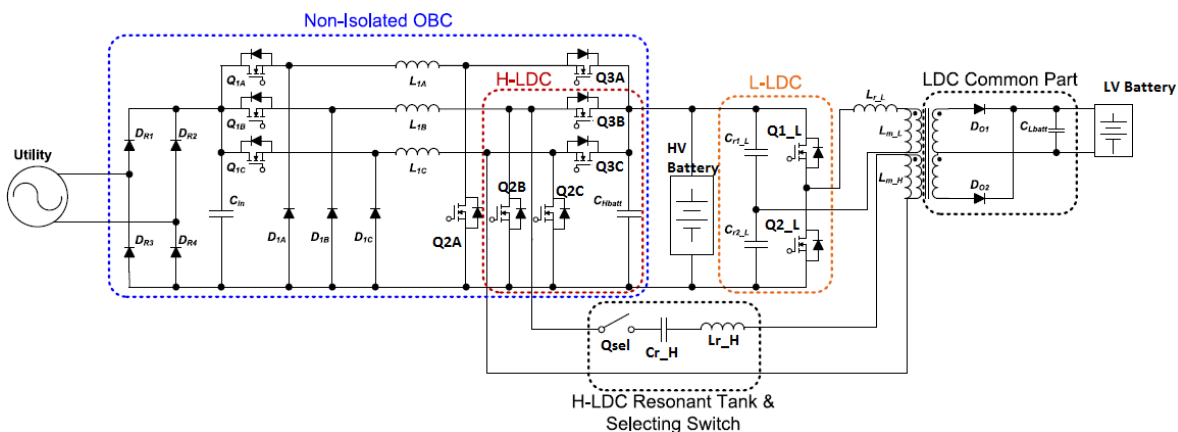


Figure 1-14: Integrated charger for HV and LV batteries, also including OBC and DC-DC simultaneous mode. [17] -D. Kim, M. Kim and B. Lee.

In order to respect the security rules for these converters in Europe, the use of three-winding transformers is very attractive. From Figure 1-2, the similarities between both isolated DC-DC converters,

used first to charge the LV battery, but also present on a 2-stage on-board charger, lead to a solution containing a three-winding transformer, as the three previous architectures. It is a requisite if at least the three operating modes are aimed: standalone OBC (G2V or V2G), standalone DC-DC converter (bidirectional), and simultaneous operation of OBC and DC-DC. Indeed, the aim of high conversion performances wherever, for standalone or simultaneous modes, justify the search for a soft-switching topology.

These two concerns are considered on the solution proposed in [18], illustrated in Figure 1-15. After the PFC stage, a three-port active bridge (TAB) is implemented. Phase-shift angles between the three ports, control the power flow direction and the three operating modes. Associated with the phase-shift, duty-cycle control extends the zero-voltage switching converter's region. However, in this solution, a wide voltage range in the HV and LV batteries is not considered.

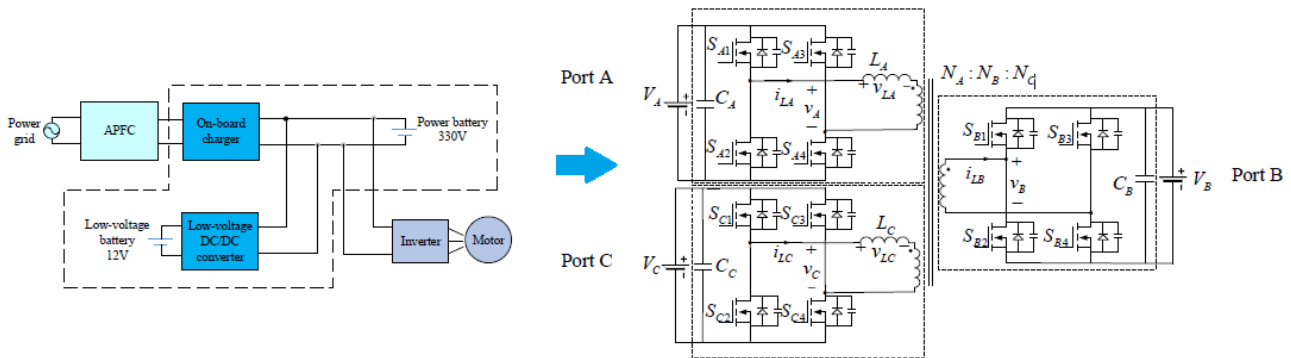


Figure 1-15: Integration of the OBC and DC-DC converters using a three-port active bridge.- [18] H. Ma, Y. Tan, L. Du, X. Han and J. Ji.

As a matter of fact, Three-port active bridges are widely exploited in fuel cells and renewable energy storage systems. The main reasons are the relatively easy bidirectional power flow control and ZVS characteristics. As an example, papers [19]-[22] propose the integration of a fuel cell, a supercapacitor, and a load using a TAB converter. The soft-switching limited range is also extended in some cases due to the duty cycle control strategies, but the studies still address a variable voltage range present in a single port only. In this thesis, we decided to develop an on-board charger in two-stages: the PFC stage to pre-regulate a V_{dc} voltage link, followed by an isolated DC-DC converter. A third winding charges the LV battery by sharing the same transformer. Based on this decision, Chapter 2 focuses on three-port converters in order to find an innovative solution that has not yet been explored. The previous solutions are listed in Table 1-4. The columns present the main features found in these existing solutions.

	DCDC Bidir	OBC Bidir	Isol (DC/DC)	Isol(DC/AC)	3 port	Soft.Swit	T control	∅ bridges(DAB)	∅ arms (PS)	Prototype
Figure 6 [8]-9]	No	Yes	Yes	Yes	No	Pseudo-ZVS	Not Fixed	Not apply	Not apply	-
Figure 7 [10]	No	Yes	Yes	Yes	No	Yes	Not Fixed	Not apply	Not apply	-
Figure 8 [11]	Yes	No	Yes	No	No	No-Low $\eta\%$	CD-AF	Not apply	Not apply	Yes
Figure 9 [12]	Yes	No	Yes	No	No	Yes	FB-AF	Not apply	Not apply	6,6 kW
Figure 10 [13]	Yes	No	Yes	No	No	No	DAB-AF	Not apply	Not apply	4 kW
Figure 11 [14]	No	Yes	Yes	No	Yes	No	Not apply	Not apply	Not apply	3,6 kW
Figure 12 [15]	No	No	Yes	Yes	Yes(PS+LLC)	Yes	Yes-FBPS+LLC	Not apply	Yes (PS)	No (Sim.)
Figure 13 [16]	No	No	Yes	Yes	Yes (FB+ CT)	No	Not apply	Not apply	Yes (1° FB)	3,3 kW
Figure 14 [17]	Yes	Yes	Yes	Yes	Yes	No	Not apply	Yes	Not apply	30 kW
Figure 15 [18]	No	No	Yes	No	No	Yes (LDC)	Yes (Boost)	Not apply	No	6,6 kW/1,9 kW

Table 1-4: Features present on the solutions integrating the OBC and DC-DC converters

1.3- Challenges in the new integrated On-board charger and DC-DC converter

The requisite for bidirectional OBC and DC-DC converters and the development of a three-port DC-DC, as illustrated in Figure 1-16, bring some challenges. In the DC-DC converter application to charge the LV battery, we see the importance of low conduction power losses. As mentioned in [3], to achieve high performances, some specific characteristics are essential, such as synchronous rectification, reduced freewheel conduction time, small current ripple, and soft-switching. Synchronous rectification is indirectly related to conduction losses in the low voltage side. This occurs because the MOSFET's body diode generally generates higher losses in comparison to the direct conduction mode. The same occurs with topologies containing an increased freewheel conduction time, generating extra losses while no power is transferred. A small current ripple also plays an important role in the output filter volume. Soft-switching over the entire battery's charging process, especially during the light load phase, impacts the converter efficiency. A comparison between DC-DC converters can also be made to this application to highlight some key points.

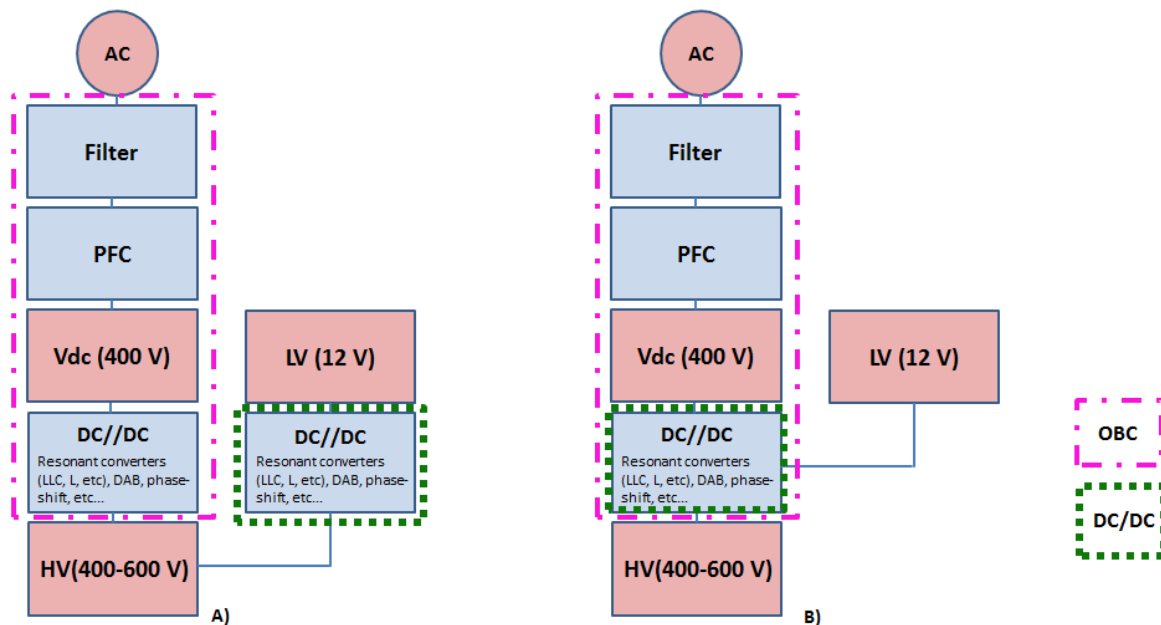


Figure 1-16: A) Diagram presenting the main parts of OBC and DC-DC converters B) Diagram presenting the OBC and DC-DC converters using a common part.

Using the data from Table 1-3, LC series resonant, LLC resonant, DAB with single phase-shift control, three-phase dual active bridge, and phase-shift converters are compared with the key points presented in Table 1-5. The first item concerns the control implementation for bidirectional power flow and if it is necessary to study a new strategy to include reverse mode. The volume is mainly related to the magnetic components present in each topology. Zero voltage switching is a key parameter for the application related with conversion efficiency and reliability. The criterion with wideband gap materials, as GaN or SiC, concerns the gain in the performance of the converter. For example, this aspect may have more impact in a converter topology without soft switching when operating under light load conditions, than in a topology operating with soft switching over the entire battery's charging process. For the first five items, the weights are considered as high, but the importance in each point can always be reevaluated according to the project target and conditions.

Criterion	Weight/Value
Bidirectional feasibility	High
Volume	High
Zero voltage switching	High
Efficiency (%)	High
Output current ripple	High
Blocking voltage	Medium
Silicon area	Medium
Synch. Rectification	Medium
Advantages in the use of GaN/SiC	Medium
Estimated cost (€)	Medium/High

Table 1-5: Some criteria to select the most appropriate isolated DC-DC converter

To verify these aspects, the design procedure is made for each one of these converters considering the DC-DC converter application (HV/LV conversion) presented in Table 1-3. The average, RMS currents, peak voltages and power losses are used to estimate the efficiency and the converter volume.

1.3.1- LLC Resonant converter

Resonant converters are widely used when the aim is to increase switching frequency and reduce the volume without increasing switching power losses. The resonance allows the transistors to switch under zero current or zero voltage conditions, eliminating part of the losses. Therefore, higher power densities can be achieved by designing the passive elements at higher frequencies.

Series resonant converters, such as the LLC, have the advantage of also presenting sinusoidal current, hence sometimes resulting in less conduction power losses compared to non-resonant converters, as the Dual-active bridge or Phase-shift converter. Figure 1-17 presents the main converter elements. The LLC series resonant converter includes an external capacitor (C_r) in series with an inductor (L_1) and the transformer magnetizing inductance (L_m). In some designs, the series inductance is partially

integrated into the transformer leakage inductance. This converter operates under variable switching frequency, and its design procedure is discussed below.

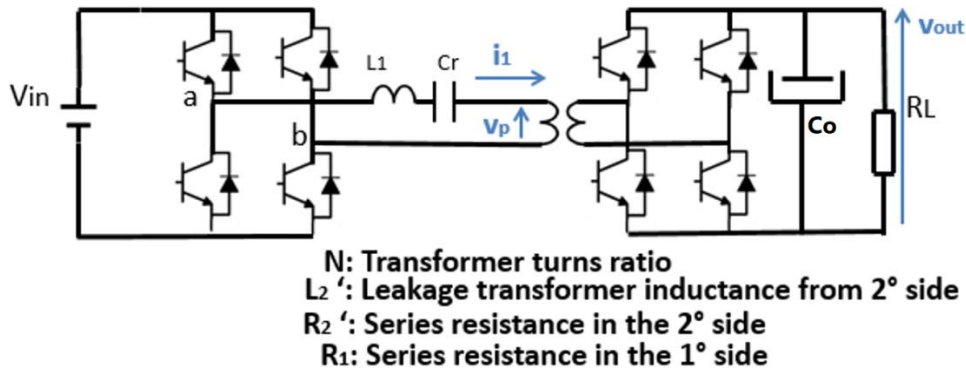


Figure 1-17: The LLC series resonant converter. The magnetizing inductance L_m is not represented, but it is an important part of the converter.

Design procedure

In the design procedure, an equivalent first harmonic model is frequently used to represent the converter, Figure 1-18. In this representation, the square voltage waveform, V_{ab} , applied in the full-bridge is only represented by the amplitude of its first harmonic, and the DC output load is represented as an AC load [3].

$$V_1 = \frac{4V_{in}}{\pi} \quad (1)$$

$$V_2 = \frac{4}{\pi} \left(\frac{V_{out}}{N} \right) \quad (2)$$

$$I_2 = \frac{\pi}{2} (I_{out} N) = \frac{\pi}{2} N \left(\frac{P_{out}}{V_{out}} \right) \quad (3)$$

$$R_{ac} = \frac{V_2}{I_2} = \frac{8 R_L}{(\pi N)^2} \quad (4)$$

The frequency can be normalized by the first resonant frequency:

$$F_o = \frac{1}{2\pi \sqrt{C_r L_1}}$$

$$\lambda = \frac{F}{F_o}$$

$$Z_o = \sqrt{\frac{L_1}{C_r}}$$

The ratio between the resonant and leakage inductors, L_1 and L_2' , depend on the transformer design, but to simplify, it can be considered one if the transformer presents symmetry between primary and secondary windings.

$$k_1 = \frac{L_2'}{L_1} = 1, \quad \text{only if the transformer is symmetrical}$$

The ratio between the magnetizing and resonant inductors, L_m and L_1 , affects the voltage gain between V_1 and V_2 and is represented by k . Higher this factor, smaller will be the output voltage range.

$$k = \frac{L_m}{L_1}$$

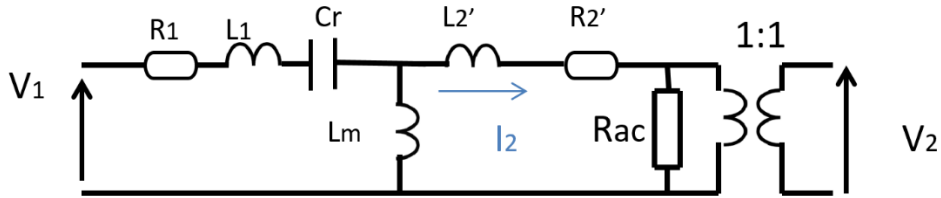


Figure 1-18: The First Harmonic equivalent circuit. L_2' and R_2' are represented in the 1° side.

A quality factor Q helps in the selection of the resonant inductance and in the voltage gain analysis. The circuit is normalized by the fundamental harmonic component of the input voltage and by the equivalent frequency, Figure 1-19.

$$Q = \frac{R_{ac}}{z_o}, \quad q_1 = \frac{R_1}{z_o}, \quad q_2 = \frac{R_2'}{z_o}$$

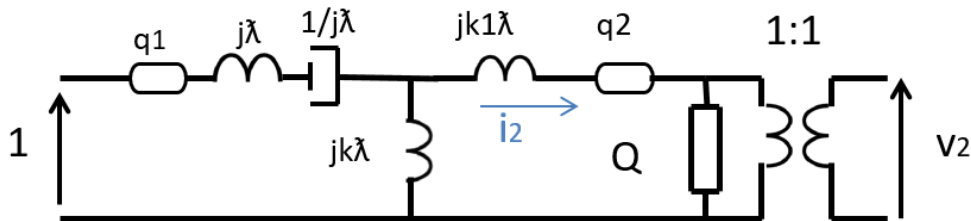


Figure 1-19: The equivalent circuit normalized by the resonant frequency.

$$v_2 = \frac{V_2}{V_1} \quad (5)$$

$$i_2 = \frac{v_2}{Q} \quad (6)$$

There is a trade-off between the ratio k to attempt the required voltage gain and the switching frequency range. To facilitate the design, the transformer is considered a symmetrical structure ($k_1=1$, $L_1=L_2'$). Typically, for an LLC resonant converter, the ratio between the inductances L_m and L_1 , k , is lower than in other topologies and only differ by a factor varying between 1.5 and 5 for the most application cases requiring large output voltage variation. However, to obtain a high power factor this factor needs to be optimized. In section 1.5.1-, two methods allow the selection of parameters k and Q . The first one consists of using the voltage gain curve to determine the minimum and maximum necessary gains from Table 1-3. The second one explores the converter capacity curve to achieve the maximum output power. In both methods, the higher as possible factor k is selected to provide the desired power with minimized circulating energy. More information is available in reference [4].

After specifying k with one of the methods, the resonant capacitor and inductor are calculated for the desired resonant frequency.

$$L_r = \frac{R_{ac} Q_{Min}}{2 \pi F_o} \quad (7)$$

$$C_r = \frac{1}{(2 \pi F_o)^2 L_r} \quad (8)$$

The transformer turn's ratio N is then calculated. For a switching frequency F_{sw} comprised between F_{min} and F_{max} , the gain G is deduced between G_{max} and G_{min} . At F_{max} (G_{min}), it is necessary to obtain the turn's ratio to reduce the maximum output voltage.

$$V_{out} = V_{in} N G_{max}$$

$$N_{p_{min}} = \frac{V_{out_{max}}}{G_{max} V_{in_{min}}} = \frac{16}{1.97 \times 220} = 0.037; N_p = 1 \quad N_s = 27$$

For an output power of 3.5 kW, the HV/LV application results in a very small k factor and a wide frequency variation range. The design can therefore, lead to increased circulating energy and power losses. In this case, the use of an auxiliary non-isolated converter connected in cascade is a solution to reduce the voltage and frequency variation ranges required by the LLC. In [4], for example, the author proposes the association with a boost converter to increase the magnetizing inductance and to reduce the frequency range. To compare the LLC with other topologies, we consider this association also. We keep for the LLC an input voltage range between 400 V and 300 V. The association leads to a higher magnetizing inductance. The results are presented in Figure 1-20 and Table 1-6.

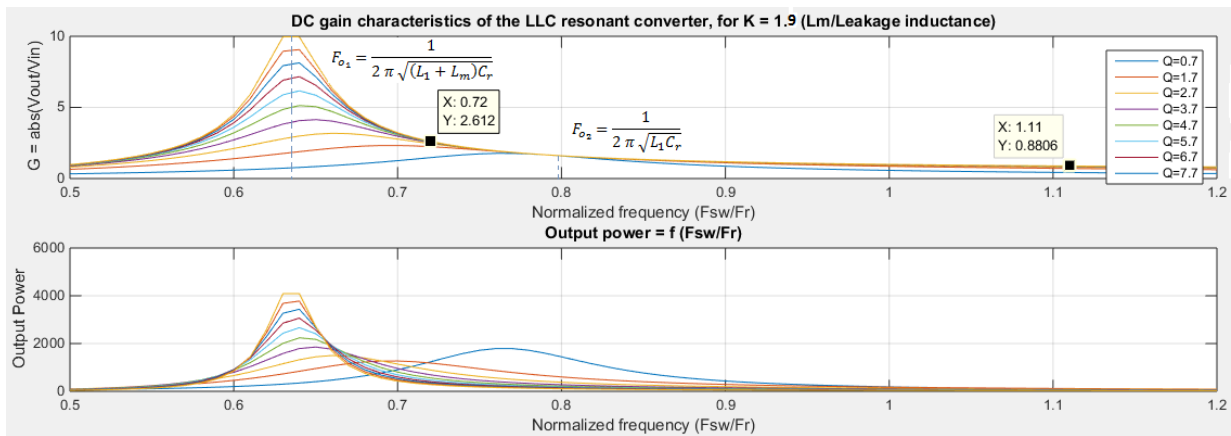


Figure 1-20: Example of a LLC converter with $k=1.9$. V_{in} : [480-300 V]; V_{out} : [10-16 V]; $P = 3.5$ kW; $L_l = 26 \mu\text{H}$; $C_r = 95 \text{ nF}$. $F_{max} = 196 \text{ kHz}$ and $F_{min} = 89 \text{ kHz}$.

Boost input	Boost output	LLC input	LLC output	L boost	ILmax boost	Ilrms boost
220-450 V	450-300 V	450-300 V	10-16 V – 14 V	15 μH	13.6 A	8.5 A

Table 1-6: Association of a non-isolated DC-DC converter with the LLC converter

In Figure 1-20, if the switching frequency is superior to the first resonant peak, the current delays the voltage and the transistors are switched at zero voltage on the primary side. The primary current is almost sinusoidal, delayed from the voltage. Its value can be estimated by considering the output current ripple remained to the first side and the current in the magnetizing inductance. These information are enough to estimate the transformer product $A_w \times A_e$, the inductors and capacitor volume and power loss. These elements are estimated as explained in the Annexes 1.5.3-.

1.3.2- LC Series Resonant converter

The schematic in Figure 1-17 can be used to represent the LC series resonant converter. The main difference between the LLC and the LC is in the transformer. The series LC resonant uses a transformer with characteristics close to the ideal, with a magnetizing inductance much larger than the series inductance, resulting in a single resonant frequency, between L_1 and C_r . This converter also reduces the switching losses and the current/voltage rate in the transformer windings. In comparison with the LLC, the series LC operates only in buck mode, and the soft-switching operation cannot be maintained under light load conditions. Despite these drawbacks, this topology allows the operation for a certain voltage range, and as it was made with the LLC converter, a pre-converter stage can be associated to it to address part of the input voltage variation.

The design procedures used for the LLC can be simplified as well as the equivalent circuit from Figure 1-19, by considering the magnetizing inductance infinite. The design procedure depends mainly on the quality factor between the equivalent AC load and the series inductor. The current in the transformer winding is considered sinusoidal:

$$i_1(t) = I_{max} \sin(\omega_r t)$$

$$I_{max} = \frac{V_1}{Z_r} = 4 \frac{V_{in}}{\pi} \sqrt{\frac{C_r}{L_1}} \quad (9)$$

$$v_{ab}(t) = v_{c_r}(t) + L_1 \frac{di_1}{dt} + v_p(t)$$

During the positive half-cycle:

$$v_{c_r}(t) = V_{in} - V_{out}N - L_1 \omega_r I_{max} \cos \omega_r t$$

$$\omega_r = \sqrt{L_1 C_r} = 2\pi F_r \quad (10)$$

The power transmitted from the primary to secondary side is calculated as:

$$P = \frac{2}{T} \int_0^\pi V_{in} I_{max} \sin(\omega_r t) dt = \frac{8 V_{in}^2 C_r}{\pi^2 \omega_r} \quad (11)$$

$$P = 4 C_r F_r V_{in} V_1 \quad (12)$$

The operating conditions are valid when the switching frequency is lower or equal to the resonant frequency.

$$F_{min} = \frac{8 V_{in}^2 C_r}{\pi^2 P_{max} 2\pi}$$

$$F_{max} = \frac{1}{2\pi\sqrt{L_r C_r}}$$

$$N = \frac{N_p}{N_s} = \frac{V_{in}}{V_{out}}$$

The dead time between the turning-off and turning-on of the transistors is necessary to ensure ZVS, to complete the charging and discharging of the transistor capacitances, C_{oss} . This time is also necessary on the LLC converter, but is less critical because of its small magnetizing inductance that helps keeping the ZVS conditions. In the series LC, this time can be estimated considering that the voltage in the resonant elements must be higher or equal to the input voltage:

$$T_{dead} = \pi \frac{\sqrt{2 L_1 C_{oss}}}{2}$$

$$L_1 = 37 \mu\text{H}$$

$$C_{oss} = 100 \text{ pF}$$

$$T_{dead} = 135 \text{ ns}$$

$$i_{L_1}(0) \frac{\sqrt{L_1}}{\sqrt{2} C_{oss}} \geq V_{in}$$

The C_{oss} capacitance depends on the transistor technology and the voltage applied, thus is not constant. As the input voltage varies, it is important to consider its evolution in the real semiconductor, as explained in [3].

1.3.3- The Dual Active Bridge (DAB)

The Dual Active Bridge is a commonly used converter for bidirectional applications. Its structure allows different variations other than the classical Single-phase Shift (SPS) control, used to reduce the current ripple, voltage stress, and expand the Zero Voltage Switching range at light load conditions.

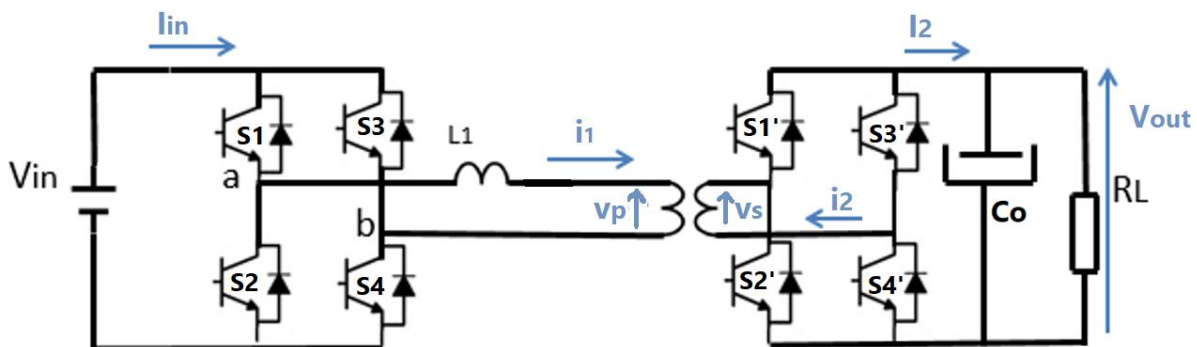


Figure 1-21: The Dual Active Bridge converter representation.

The Single-phase shift (SPS) control is obtained by shifting one bridge from another resulting in shifted square voltage waveforms with duty cycle fixed at 50%. This method is easy to implement

and shows good control dynamics, but it does not allow ZVS at light load condition and results in higher circulating current, decreasing the performance.

The Extended-phase shift (EPS) adds one more freedom degree, with an inner phase-shift angle applied between legs of a same bridge. This inner phase produces a three-level voltage waveform in one of the bridges and a two-level voltage waveform in the second (50% duty cycle). This method expands the ZVS range and decreases the current stress. More benefits can be obtained with other control strategies, such as the Dual phase-shift (DPS), and the Triple phase-shift (TPS). The comparison of the different strategies is presented in [23].

The power is controlled by the phase-shift angle between the two bridges and its transfer occurs from the leading to the lagging side, as illustrated in Figure 1-22.

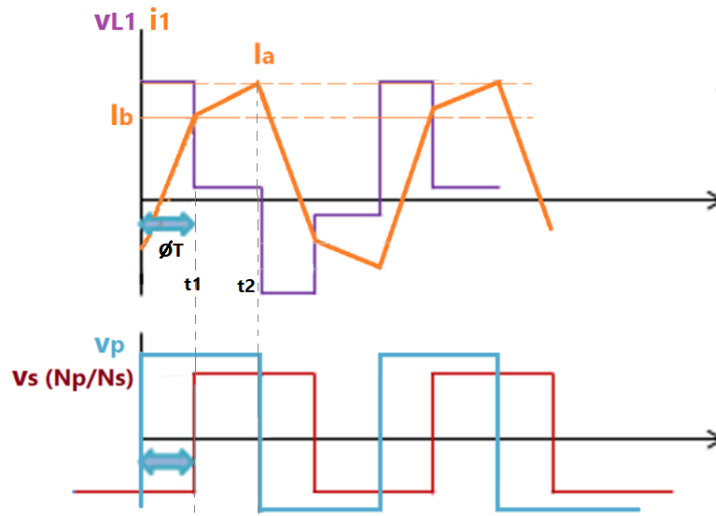


Figure 1-22: V_L and I_L typical waveforms for (SPS control)

The current in the inductance L_1 can be described as:

$$\text{for } t = [0 : t_1]; \quad i_1(t) = -I_a + \left(\frac{V_{in} + \frac{V_{out}}{N}}{L_1} \right) t \quad (12)$$

$$\text{for } t = [t_1 : t_2]; \quad i_1(t) = I_b + \left(\frac{V_{in} - \frac{V_{out}}{N}}{L_1} \right) t \quad (13)$$

$$\text{for } t = [t_2 : t_2 + t_1]; \quad i_1(t) = I_a - \left(\frac{V_{in} + \frac{V_{out}}{N}}{L_1} \right) t \quad (14)$$

$$\text{for } t = [t_2 + t_1 : 2t_2]; \quad i_1(t) = -I_b - \left(\frac{V_{in} - \frac{V_{out}}{N}}{L_1} \right) t \quad (15)$$

$$t_2 = (D T), \quad t_1 = \frac{\phi T}{2\pi} \quad (16)$$

The voltage gain depends also on the shift angle:

$$M = \frac{V_{out}}{N V_{in}} = \frac{I_{out} R_L}{N V_{in}} = \frac{(V_{in} N - V_{out}) \phi}{2\pi L_1 F_{sw} N^2 V_{in}} \left(\frac{\phi}{2\pi} - 2D \right) R_L \quad (17)$$

The current at instants t_1 and t_2 are calculated with equations (12), (13), (14) and (15):

$$I_b = \frac{(D T)}{2 L_1} \left(\frac{V_{out}}{N} - V_{in} \right) \quad (18)$$

$$I_a = \frac{(T \emptyset)}{4 \pi L_1} \left(V_{in} + \frac{V_{out}}{N} \right) + \frac{(D T)}{2 L_1} \left(V_{in} - \frac{V_{out}}{N} \right) \quad (19)$$

L_1 is the series inductance, D is the duty cycle, and \emptyset is the phase-shift between the two bridges. The output average current is:

$$I_{out} = \frac{(V_{in} N - V_{out}) \emptyset}{2 \pi L_1 F_{sw} N} \left(\frac{\emptyset}{2 \pi} - 2D \right) \quad (20)$$

The minimum conditions of soft switching are the current peaks I_a and I_b , that must be higher than zero for both power flow directions. After calculating the transformer turns ratio, the gain M is calculated again to obtain ZVS. The minimum phase-shift angle applied can be calculated as:

$$\emptyset > \frac{2 \pi D (M-1)}{(1+M)} \quad \text{and } M \geq 1$$

The maximum power transfer occurs with $\emptyset = \pi/2$:

$$I_{outMax} = \frac{3 (N V_{in} - V_{out})}{16 L_1 F_{sw} N} \quad (21)$$

Using (17) and (20), the series inductance is calculated to obtain the maximum required power:

$$L_1 \leq \frac{V_{out} (N V_{in} - V_{out}) \emptyset_{max} (\emptyset_{max} - 4 \pi D)}{4 \pi^2 F_{sw} N P_{o max}} \quad (22)$$

The RMS current in the inductor can be determined by integrating the square of the current waveform as shown in Section 1.5.3.

The maximum required voltage gain is:

$$G_{max} = \frac{V_{in_{nom}} V_{out_{min}}}{V_{in_{max}} V_{out_{nom}}} \quad \text{with ZVS}$$

Using the design requirements from Table 1-3, the voltage/current stress on the DAB topology are presented in Table 1-7 at 200 kHz.

1.3.4- The Three-phase Active Bridge (TAB)

In higher power applications and because of the current stress, the Three-phase Active Bridge is an alternative to the DAB converter. The three arms in the same bridge are delayed from each other by

120° as in the 3-phase inverter, and the command applied to the secondary side delayed of the phase-shift angle \emptyset , in order to control the voltage and output power.

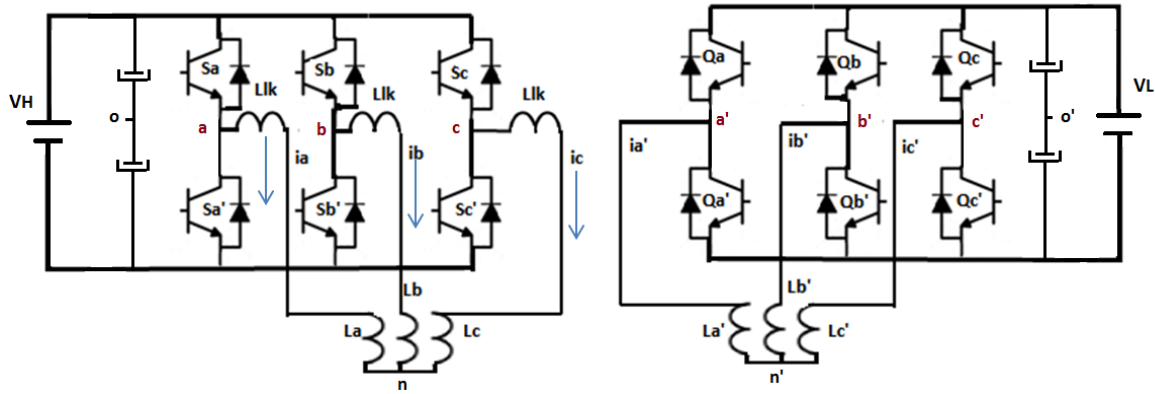


Figure 1-23: The three-phase Active Bridge

The current and voltage analysis in the transformer and transistors is quite similar to the 3-phase inverter, and we can start the analysis with a simple sinusoidal modulation principle.

The voltages V_{ao} , V_{bo} and V_{co} are square waveforms with a duty cycle of 50%, delayed of 120° from each other. On the secondary side, the voltages $V_{ao'}$, $V_{bo'}$ and $V_{co'}$ are delayed from the voltages on the primary side. The sum of the currents in the windings is zero and considering the transformer as symmetrical, the sum of the voltages is also zero:

$$V_{an} + V_{bn} + V_{cn} = 0 \quad (1)$$

$$V_{an} = V_{ao} - V_{no}$$

$$V_{bn} = V_{bo} - V_{no}$$

$$V_{cn} = V_{co} - V_{no}$$

By adding the above equations and respecting the equation (1):

$$V_{no} = \frac{V_{ao} + V_{bo} + V_{co}}{3} \quad (2)$$

The voltage over the series inductance on phase A is the difference between the voltages V_{an} and V_{an}' , and the current is determined, as demonstrated in [24]. The maximum power transfer occurs for a phase-shift of 80°, and the inductance is calculated as in the Dual Active Bridge, to obtain the maximum required power transfer:

$$L_s = \frac{2 M V_{LV}^2}{27 N F_{sw} P_{max}}$$

The current and voltage stresses are calculated for the same design requirements in Table 1-3 and presented in Table 1-7.

1.3.5- The Phase-shift converter (FBPS)

The phase-shift converter is considered with a full-bridge arrangement in primary and secondary sides. The control uses phase-shift between the arms on the same bridge, so the voltage is a three-level waveform. With the two bridges, the diode bridge in the secondary side rectifies the voltage if synchronous rectification is not implemented. During the free-wheeling phase, as presented in Figure 1-25, the four transistors on the secondary side are short-circuited to conduct the remaining transformer current. Because of the symmetry, the same control can be applied in reverse power flow to the secondary side.

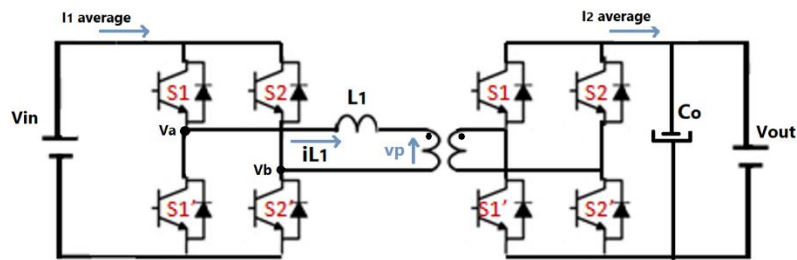


Figure 1-24: The full-bridge phase-shift converter.

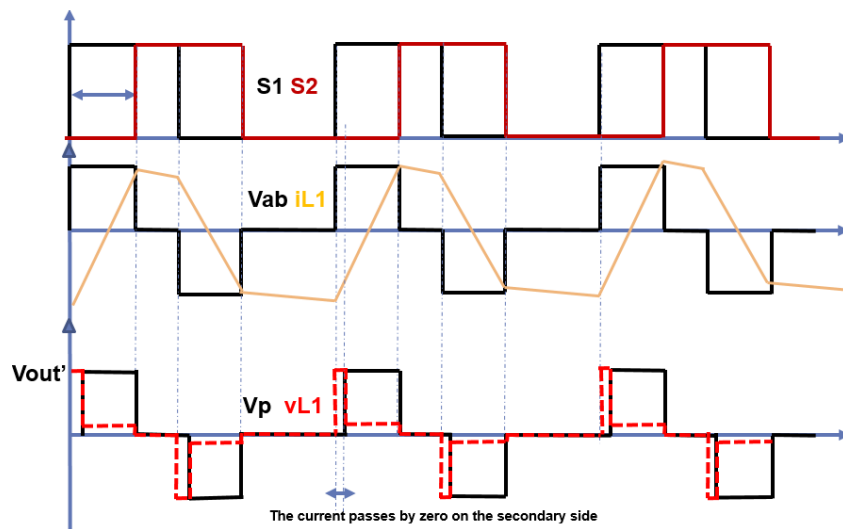


Figure 1-25: Switching signals applied to the transistors and equivalent voltage and current for nominal power condition in the FBPS converter.

The current waveform has three different slopes due to the delay time between the primary and secondary sides. Dead-time is necessary to charge and discharge the parasitic capacitances using the remaining energy on the series inductance, L_1 . The design procedure includes calculating the RMS, average current, and the maximum voltage stress in the transistors. The following table shows the results considering the operation in step-down and step-up modes.

1.3.6- A bidirectional converter with center-tapped transformer at LV side

The center-tapped transformer connected to the low voltage side provides some advantages compared to the full-bridge phase-shift converter. As the current stress is important on the low voltage side, the center-tapped transformer allows in the step-up mode, to reduce the current in the winding. In the reverse operation mode, it is similar to work with the Push-pull converter structure connected to the low voltage side.

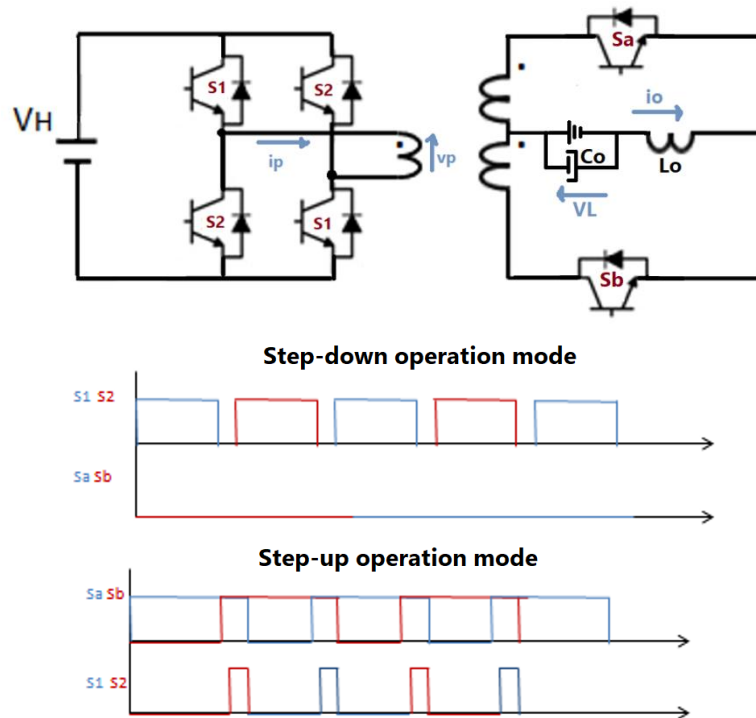


Figure 1-26: The center-tapped transformer connected to the Low Voltage Side and the switches command during the forward and the reverse modes.

The design and analysis of this bidirectional converter is presented in [25]. In boost operation mode, the transistors on the low-voltage side (Sa and Sb) need to be controlled delayed from each other 180° , and with a duty cycle superior to 50%. The transistors on the high voltage side are turned-on under ZVS, and their duty cycle is kept small to limit the current peak. These devices need to perform small conduction power loss in the reverse mode because their body diodes conduct more for an entire cycle than the transistor path.

During the buck operation mode, the gate-signals applied to the high-voltage side transistors are 180° out of phase and present additional dead time. On the low voltage side, the body diodes of transistors Sa and Sb can take over the current, operating like a high-frequency rectifier. The component's current and voltage equations are developed in [25].

The voltage and current stress for the typical DC/DC converters can be viewed in the following table.

	LLC	Series LC	DAB	3-DAB	PSFB	CT
V_{Tmax}	600 V	600 V	774 V	410 V	600 V	660 V
I_{TRMS}	12.2 A	6.8 A	6.2 A	10.8 A	8.3 A	8.3 A
I_T	4.9 A	4.0 A	4.4 A	6.5 A	7.9 A	7.9 A
V_{dmax}	25 V	16 V	34 V	56 V	42 V	42 V
I_{dRMS}	208 A	158 A	178 A	62 A	198 A	196 A
I_d	120 A	98 A	125 A	42 A	132 A	151 A
I_{pRMS}	18 A	12 A	12.5 A	9.6 A	12 A	14 A
I_{sRMS}	308 A	242 A	357 A	92 A	337 A	209 A
N	28	28	28	10	26	28
B_{max}	0.148 T	0.148 T	0.148 T	0.14 T	0.12 T	0.14 T
I_{CoRMS}	134 A	120 A	204 A	89 A	186 A	76 A
C_o	440 μ F	440 μ F	440 μ F	150 μ F	440 μ F	150 μ F

Table 1-7: Current and voltage stress in the bidirectional converters designed at 200 kHz

Figure 1-27 and Figure 1-28 show the component stress values, such as current and voltage, and the product $A_w \times A_e$ with the magnetic material volume (only the transformer and inductors) for the six isolated DC-DC converters: the resonant LLC, the series resonant LC, the Dual Active Bridge (DAB), the three-phase DAB (3-DAB), the Phase-shift converter using full-bridge (PSFB) and bidirectional converter using a center-tapped transformer on the low voltage side (CT). The output current ripple is also evaluated in the DC-DC converter LV battery application since it has an impact in the converter final volume. Figure 1-29 shows the power losses and the estimated efficiency for each topology considering the nominal operation conditions from Table 1-3 in three different switching frequencies, 100 kHz, 200 kHz and 400 kHz. The volume and power loss are estimated as explained in the section 1.5.3-Annexes.

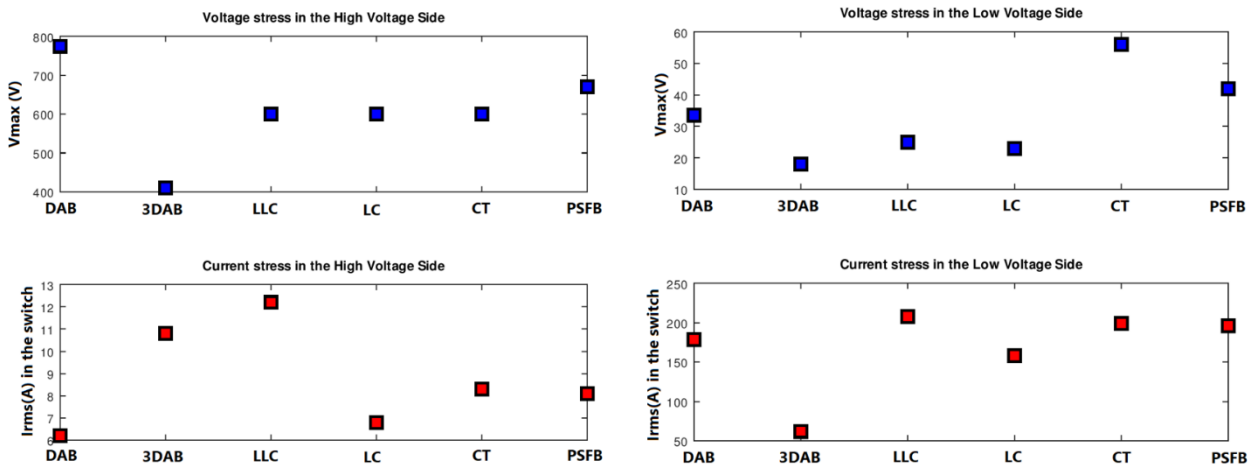


Figure 1-27: Voltage and current stresses on the LV and HV sides.

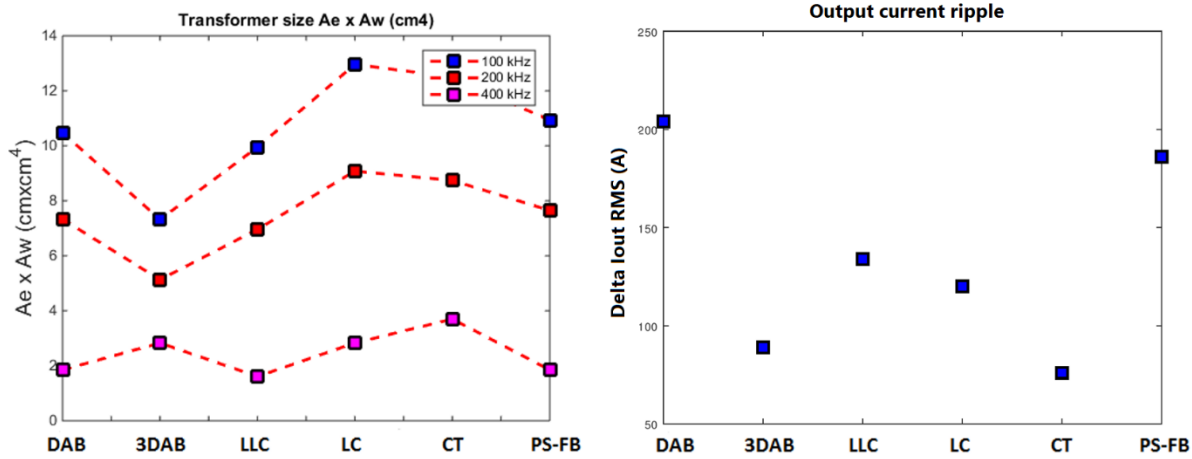


Figure 1-28: $A_e \times A_w$ (cm⁴) product for magnetic components and LV side current ripple (100 kHz).

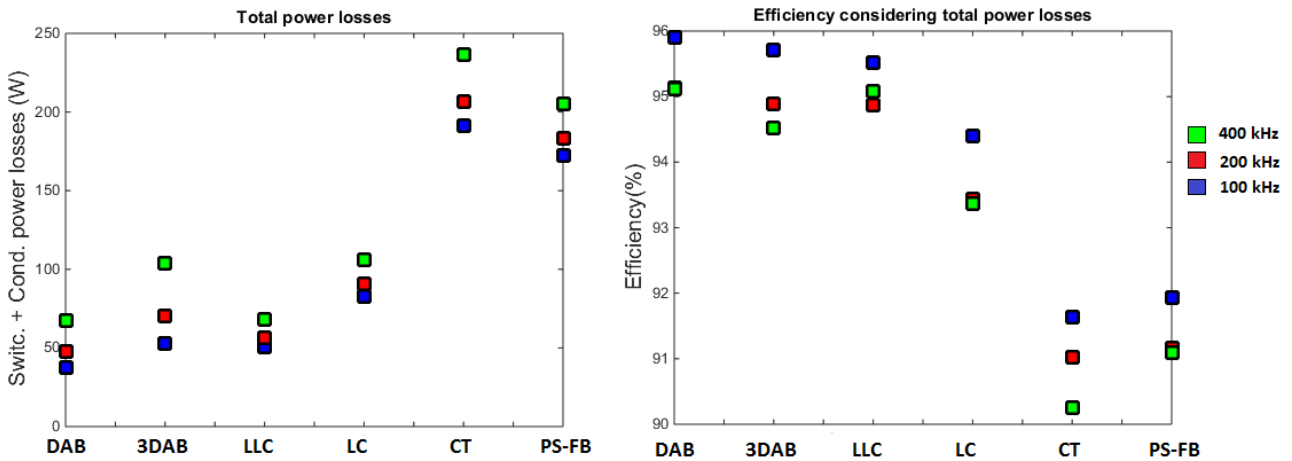


Figure 1-29: Transistors power losses and total estimated efficiency for different converters at 100, 200 and 400 kHz.

The different performances, considering the 6 converters, show the importance of reduced conduction power losses on the LV side. The 3-phase Dual Active Bridge has the lowest current stress on the low voltage side, generating reduced conduction losses, but also needs 6 switches instead of 4. Despite the increased number of switches, this topology is well suited to improve power density. Different principles present in these converters can be applied to a three-port converter to the OBC and DC-DC converter implementation, and they are better investigated in Chapter 2. To differentiate the DC-DC converter associated with the LV battery from the DC-DC isolated part present in the two-level OBC converter, the nomenclature LDC used in some of the references mentioned above, will also be adopted in the next chapters.

1.4- Dissertation outline

Chapter 2 presents the three-port active bridge converter and show their limitations to our application to achieve the voltage variation range of each battery and keep zero-voltage switching during the entire battery charging process.

Chapter 3 focuses on the study of the three-port converter proposed to integrate the OBC and DC-DC converters. It presents the operating modes, the soft-starter strategy, and the converter model. The chapter also proposes an additional coupling between the DC side inductances for the current-fed converter that can be explored in several applications.

Chapter 4 presents the development of a three-winding planar transformer. As the converter has three-different modes, a more detailed analysis concerning power losses was made. For this purpose, an analytical study of the current sharing between parallel layers at high-frequency is discussed in this chapter. An equivalent model containing parasitic elements depending on the frequency range was also developed.

The converter prototype is presented in Chapter 5. It also includes a more realistic model with parasitic elements affecting the resonance and verified by the experimental results.

Finally, Chapter 6 considers the integration of the Three-port converter with the other converter stages, as the bidirectional AC-DC PFC and a non-isolated bidirectional DC-DC converter to address the entire voltage variation range of the batteries. The total converter efficiency is therefore estimated.

1.5- Annexes

1.5.1- LLC resonant converter design

One of the design methods consists in calculating the voltage gain curve between the output voltage and the first harmonic of the input voltage in the equivalent circuit, Figure 1-19. This method includes different curves for the corresponding Q quality factor, evaluated for a wide range in order to provide the desired power.

$$V_m = \frac{1 [Z_m // (Z_2 + Q)]}{Z_1 + [Z_m // (Z_2 + Q)]} \quad (6) \text{ Voltage in the magnetizing inductance}$$

$$\text{Gain} = \frac{V_m Q}{Q + Z_2}$$

$$[Z_m // (Z_2 + Q)] = [jk\lambda // (q_2 + jk_1\lambda + Q)] = \frac{jk\lambda (q_2 + jk_1\lambda + Q)}{jk\lambda + (q_2 + jk_1\lambda + Q)}$$

$$Z_{eq} = [Z_m // (Z_2 + Q)] = \frac{jk\lambda q_2 - k k_1 \lambda^2 + jk\lambda Q}{q_2 + Q + j\lambda (k + k_1)} = \frac{j (k\lambda q_2 + k\lambda Q) - k k_1 \lambda^2}{q_2 + Q + j\lambda (k + k_1)}$$

To simplify, we neglect the series resistances in the transformer ($q_2 = q_1 = 0$). These resistances can be included in a 2° iteration procedure to ensure the converter's minimum requirements.

$$Z_{eq} = \frac{j(k\lambda Q) - k\lambda^2}{Q + j\lambda(k+1)}$$

In order to design the converter, we plot the curve gain characteristic with Matlab or other software for several factors (k) considering equals primary and secondary leakage inductances ($k_1=1$). The best design corresponds to the maximum factor (k) that gives the minimum and maximum gains, allowing the maximum output power, as shown in Figure 1-30. Smaller this ratio between the series and the magnetizing inductances, higher will be the circulating energy on the converter, increasing also its conduction power loss.

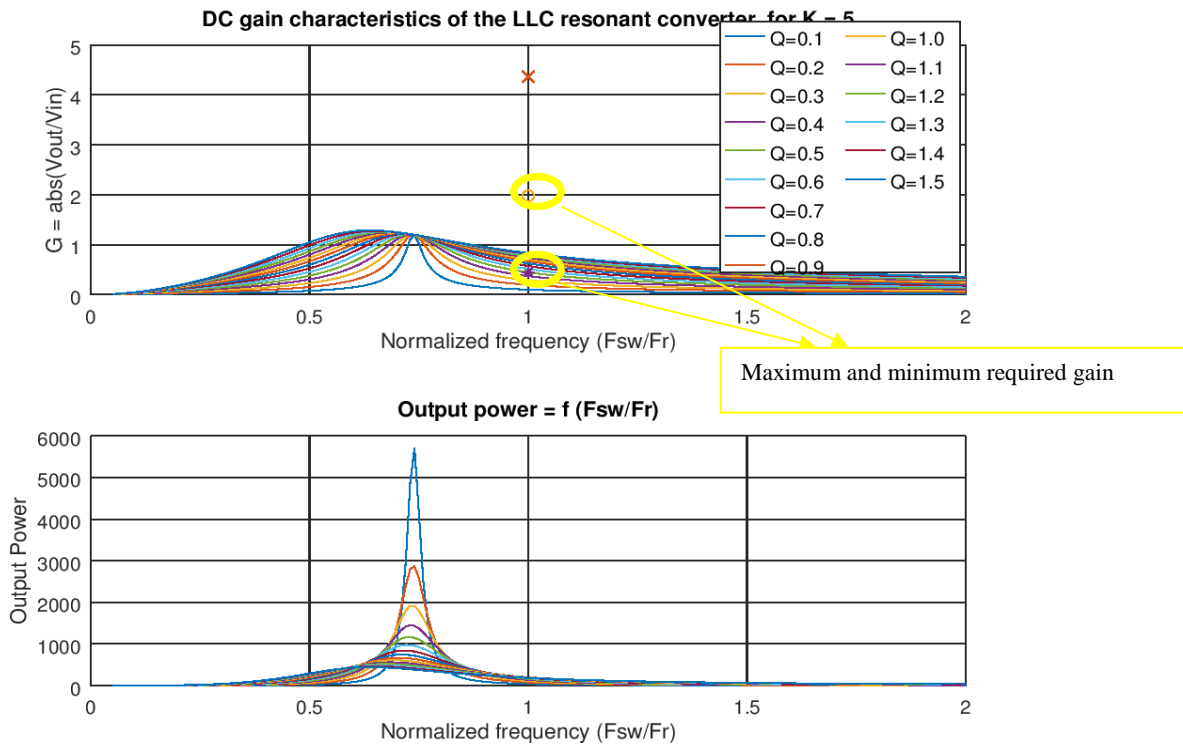


Figure 1-30: The voltage gain curve for $k = 5$ that does not achieve the maximum necessary gain.

In this example, for $k = 5$, we observe in Figure 1-30 that the maximum gain cannot be attempted. The factor k is therefore decreased and the gain checked it again until it gives the required result.

$$G_{min} = \frac{V_{out_{min}}}{N V_{in_{max}}} \quad (7)$$

$$G_{max} = \frac{V_{out_{max}}}{N V_{in_{min}}} \quad (8)$$

Method 2

The second method is taught by Professor Mohamed Charif Karimi during its lectures about soft-switched converters at Centrale Supélec, Gif Sur Yvette, in France. The method is slightly different without directly evaluating the Q factor (R_{ac}/Z_o).

It consists of checking for several frequencies and k factors, the converter capacity curve, the normalized output voltage, and the output current from the equivalent circuit in Figure 1-19. The maximum and minimum voltages are observed for each curve as well as the minimum and maximum output current. The method can also be used during an optimization process to limit the reactive energy and to minimize the conduction power losses.

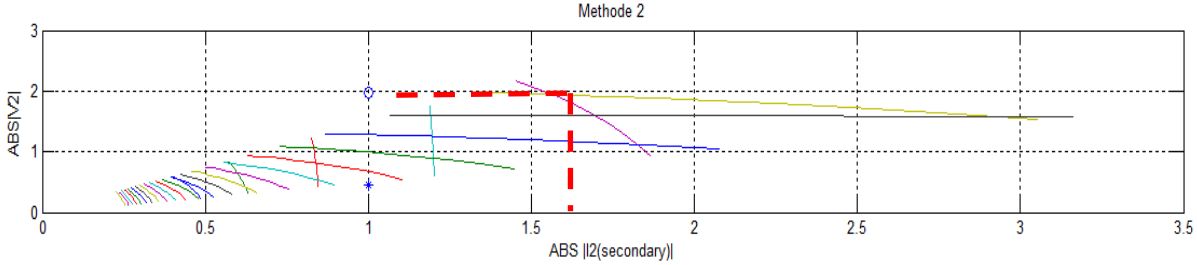


Figure 1-31: Example of the capacity curve in the LLC resonant converter for different normalized switching frequencies (F_{sw}/F_r).

Using the curve capacity, the switching frequency range can be deduced considering the load specification.

1.5.2- DAB converter

The RMS current in the inductor can be determined by integrating the square of the current waveform:

$$I_{Lrms}^2 = \frac{2}{T} \left\{ \int_0^{t_1} \left[-\frac{V_{in}(t_1+DT)}{2L_1} - \frac{V_{out}(t_1-DT)}{2L_1} + \frac{(V_{in}-V_{out})}{L_1} t \right]^2 dt + \int_{t_1}^{DT} \left[\frac{(V_{out}-V_{in})DT}{2L_1} + \left(\frac{V_{in}-V_{out}}{L_1} \right) t \right]^2 dt \right\}$$

$$I_{1average} = \frac{2}{T} \left\{ \int_0^{t_1} \left[-\frac{V_{in}(t_1+DT)}{2L_1} - \frac{V_{out}(t_1-DT)}{2L_1} + \frac{(V_{in}-V_{out})}{L_1} t \right] dt + \int_{t_1}^{DT} \left[\frac{(V_{out}-V_{in})DT}{2L_1} + \left(\frac{V_{in}-V_{out}}{L_1} \right) t \right] dt \right\}$$

The maximum required gain is:

$$G_{max} = \frac{V_{in,nom} V_{out,min}}{V_{in,max} V_{out,nom}} \quad \text{with ZVS}$$

Capacitors on secondary and primary sides should compensate the RMS current:

$$I_{cPrms} = \sqrt{I_{pRms}^2 - I_{paverage}^2}$$

$$I_{cSrms} = \sqrt{I_{sRms}^2 - I_{saverage}^2}$$

1.5.3- Volume and total power loss estimation

The total volume occupied by the converters is considered as the sum of the volume occupied by the output filter (capacitors, inductors), the volume occupied by the transformer, including the magnetizing inductance in the case of the LLC resonant converter (if the inductance is not integrated in the transformer), the volume of the series inductance, the power switches and the heat sink.

The output capacitor volume for each converter depends on the RMS current, capacitance and maximum voltage. For this example, solid tantalum capacitors are selected and used in parallel to reduce the current ripple. The center-tapped structure allows the smallest output capacitance due to the presence of the inductor in the secondary side that smooth the output current.

The power losses in the capacitors are calculated with the datasheet information:

$$P_c = \Delta I_{out_{RMS}}^2 ESR_{equivalent}$$

$$\Delta T_c = I_{ripple} \frac{ESR}{S (Heat Rad_{Factor})}$$

The volume occupied by the transformer is estimated by the product between the effective magnetic core section area A_e and the winding area A_w . This product establishes the closest available magnetic core to construct the transformer and it is determined by knowing the applied voltage waveform, the RMS current in the windings, the number of turns, the peak flux density B_{max} , the current density J , and a feasible window utilization factor Fu , that normally for discrete transformer can be settled between 0.35 and 0.40.

$$A_e A_w = \frac{V_{P_{max}}}{2 F_{sw} N_P B_{max}} \left(\frac{N_P \left(\frac{I_{P_{RMS}}}{J} \right) + N_S \left(\frac{I_{S_{RMS}}}{J} \right)}{Fu} \right)$$

Ferrite core E shape from Magnetics is considered with a same magnetic material for the four converters. The inductor volume estimation is similar to that used for the transformer, but its effective magnetic core section area is directly proportional to the peak current, due to the maximum stored energy:

$$A_e A_w = \frac{L \Delta I_{L_{max}}}{N B_{max}} \left(\frac{N \left(\frac{I_{L_{RMS}}}{J} \right)}{Fu} \right)$$

The power losses are estimated in the inductor and in the transformer. The magnetic core power losses are calculated by Steinmetz equation and by using the information available on the datasheet considering the volume of the core. The winding power losses are estimated by the product between the RMS current and the equivalent resistance. In the case of the center-tapped structure, the output filter

inductance is also considered, but in this case, only the power loss due to the DC winding resistance is considered.

In the case of the power transistors, the power losses are evaluated and a heat sink is calculated to prevent that the component has its junction temperature higher than the maximum allowed temperature. The total power losses, divided between conduction and switching power losses, are evaluated in Simetrix and compared with analytical expressions considering ZVS turn-on on the primary and ZCS on the secondary sides for the resonant converters and hard-switching at light load for the Phase-shift and DAB converters. It is also considered that the converters are synchronously rectified in order to prevent the reverse conduction power losses on the low voltage side. Reverse recovery energy is also considered for the ZVS turn-on condition.

$$P_{cond} = R_{on} I_{DS_{RMS}}^2$$

$$P_{SW} = \frac{1}{2} V_{DC} I_{DS} (T_{on} + T_{off}) F_{sw} + Q_{rr} V_{SD} F_{sw}$$

The junction temperature is determined by the product between the total power losses produced by the device and its thermal resistance between case and junction R_{thJC} , added to the case temperature, T_c . If it is necessary, T_c is reduced by increasing the size of the heat sink. It's also considered individual's heat sinks for high and low voltage sides considering the ambient temperature of 40°C.

$$T_j = (P_{cond} + P_{SW})R_{thJC} + T_c \text{ (Heat sink volume)}$$

1.6- References

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2- Investigation of Three-port topologies to integrate the OBC and DC-DC converters

2.1- Introduction

In this chapter, we investigate one of the possible solutions to integrate the OBC and the LDC converters in a Three-port active-bridge. The three sources, the V_{dc} voltage bus from PFC, the high voltage battery (HV battery), and the low voltage auxiliary battery (LV battery), are connected to full-bridge structures sharing the same transformer, as illustrated in Figure 2-1.

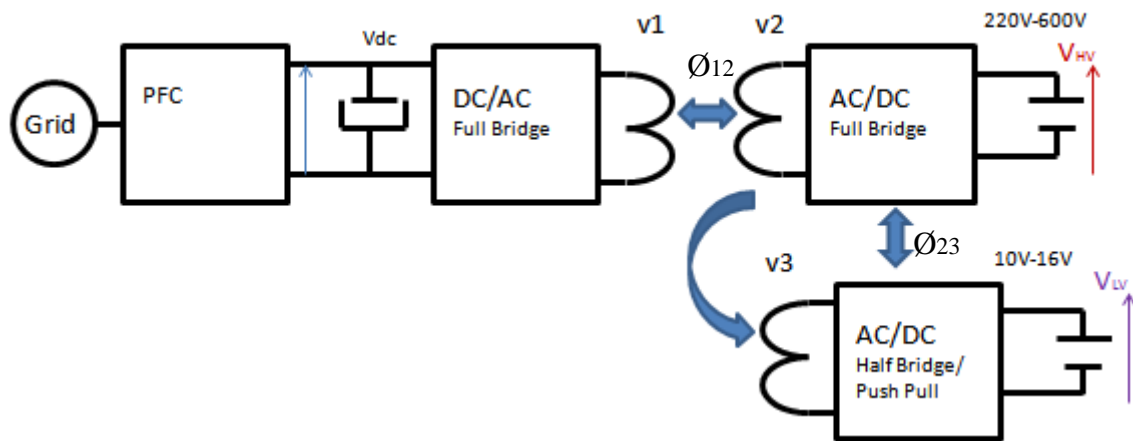


Figure 2-1: The three-port active bridge proposed to integrate the OBC and LDC converters

Three-port active converters use phase-shift between the command applied between the ports to control the power flow and regulate the output voltage, as in the Dual Active bridge converter (DAB). This converter is investigated in this section. Some of their control strategies are studied to obtain soft switching for the whole range of voltage and required power and solve a common problem that appears when the three voltage levels are magnetically coupled. The solutions discussed are based on the voltage and power levels presented in Table 2-1 and Table 2-2.

Energy source	Voltage level	Denotation
V _{dc} link voltage	450 V	V _{OA}
High Voltage Battery	240 – 600 V	V _{OB}
Low Voltage Battery	10- 16 V	V _{OC}

Table 2-1: Voltage level for the sources connected to the three ports of the converter.

Power Transfer direction	Power level
V _{OA} → V _{OB}	7.0 kW
V _{OB} → V _{OA}	7.0 kW
V _{OB} → V _{OC}	3.5 kW
V _{OC} → V _{OB}	3.5 kW

Table 2-2: Power level transfer between the ports.

2.2- The Three-port active bridge with duty-cycle control

As well known, the DAB has a limited ZVS region. For example, for low power flow and a wide range of voltages, the converter loses the Zero Voltage Switching (ZVS) capability. In this case, the phase-shift angle becomes small, and the voltage applied to the series inductance is not enough to increase the current in the right direction allowing the charge and discharge of the capacitances in parallel with the transistors. One of the solutions for this problem is the use of additional variables in the control strategy to keep the zero voltage switching characteristics during critical operation points. Many authors had studied the use of additional internal angles in the same full-bridge to achieve this objective [1]-[4].

In Figure 2-2, a three-port active bridge structure is presented. The three different voltage sources represent the three DC voltages connected to the integrated power unit: the Vdc link voltage, the HV and LV batteries, represented by V_{oA} , V_{oB} and V_{oC} , respectively. Each full-bridge produces a square voltage waveform applied to the inductance connected in series with the transformer, V_a , V_b and V_c . While the voltages are delayed from each other, the energy stored on the series inductances is different from zero allowing the power transfer between the ports, [5]. This power transfer occurs from the port in advance to the delayed port, as represented in Figure 2-3-A: three voltage sources controlled with different phase-shift angles applied to the transformer windings. If one of the ports is used as a reference, two phase-shift angles can be used to determine all the power flow modes between the three ports, ϕ_{AB} and ϕ_{BC} . A simplification in Figure 2-3-B is made by transferring the voltage sources to the transformer's primary side.

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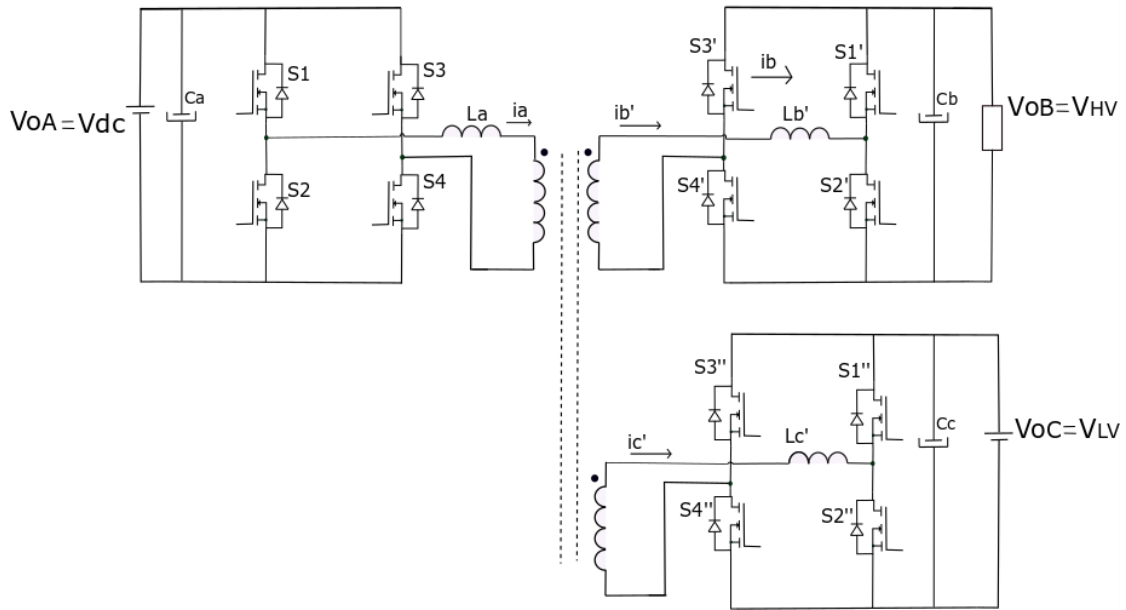


Figure 2-2: The Three-port active bridge converter.

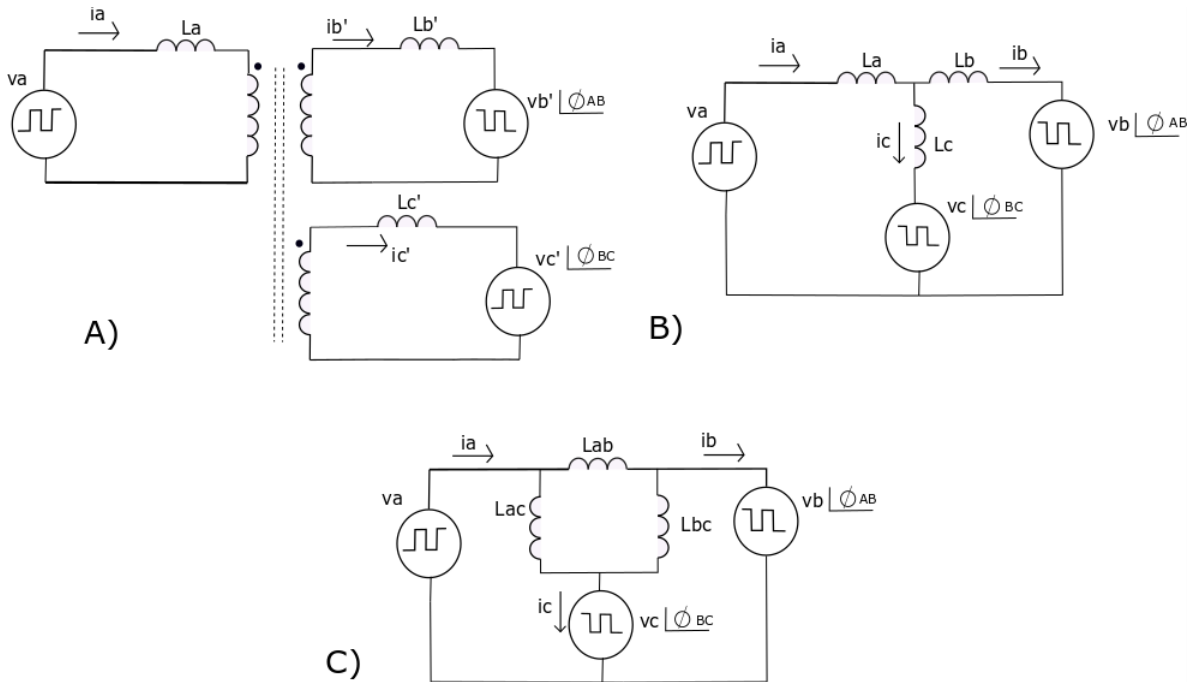


Figure 2-3: a) Equivalent circuit of the Three-port converter. b) Simplified equivalent circuit c) π equivalent circuit.

As proposed in [5], the π equivalent circuit, in Figure 2-3-C, can facilitate the circuit analysis. With this representation, we consider the magnetizing inductance much higher than the series inductances. Figure 2-4 presents the current waveforms on the three equivalent inductances for $\varnothing_{AB} = \varnothing_{BC}$, when the DC link charges the HV and LV batteries at the same time for the case where the voltages have the ratio presented in Eq. (1). The first voltage source is considered as the reference. If the current is negative during the voltage rising edges, the transistor switching occurs at zero voltage

because the current is delayed from the voltage. A similar operation occurs during the falling edges: if the current is positive, the transistor is switched under zero voltage.

$$V_{oA} > V_{oB} N_{AB} > V_{oC} (N_{BC} N_{AB}) \quad (1)$$

Therefore, if the voltage sources have a wide variation range or the RMS current between the ports becomes too small, the soft-switching conditions may no longer be attended.

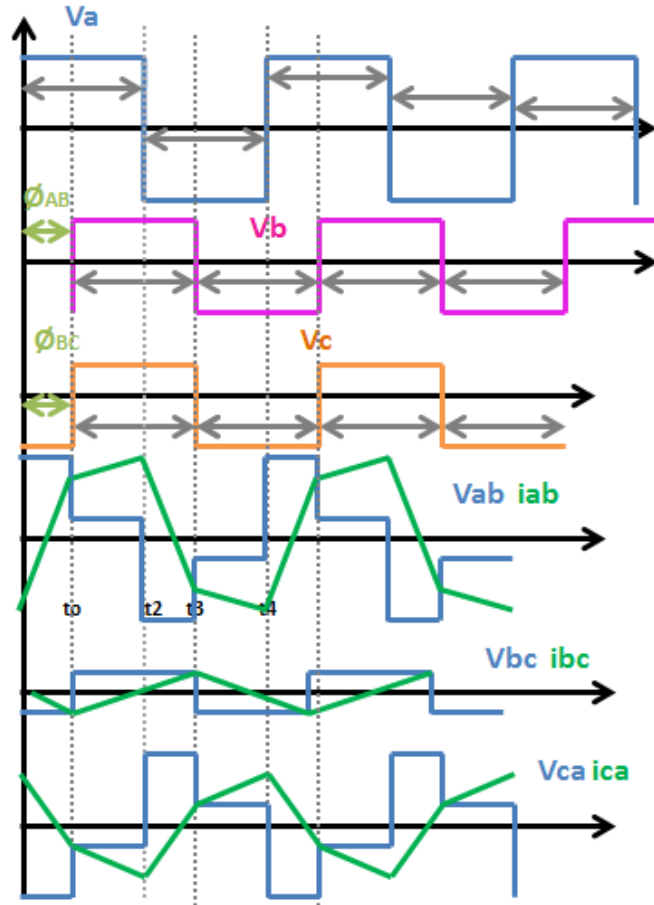


Figure 2-4: Voltage and current waveforms considering the same duty cycle (0.5) in the 3 bridges and the condition of Eq. (1).

The voltages $v_a(t)$, $v_b(t)$ and $v_c(t)$ can be represented in frequency by Fourier's decomposition, where the odd harmonics depend on the internal duty cycle of each full-bridge and phase-shift angles:

$$v_a(t) = \sum_{N=1}^{\infty} \frac{4 V_a}{N \pi} \sin(N \pi D_a) e^{i(N \omega t)}$$

$$v_b(t) = \sum_{N=1}^{\infty} \frac{4 V_b}{N \pi} \sin(N \pi D_b) e^{i(N \omega t + \phi_{AB})}$$

$$v_c(t) = \sum_{N=1}^{\infty} \frac{4 V_c}{N \pi} \sin(N \pi D_c) e^{i(N \omega t + \phi_{BC} + \phi_{AB})}$$

Where V_a , V_b , and V_c are the average values of the voltage sources V_{oA} , V_{oB} , and V_{oC} . D_a , D_b , and D_c the duty-cycles associated with the waveforms in Figure 2-4.

The currents $i_{ab}(t)$, $i_{bc}(t)$, and $i_{ca}(t)$ are defined with the voltage drop on the equivalent inductances:

$$i_{ab}(\omega t) = \begin{cases} -I_{abO} + \frac{(V_a+V_b)}{\omega_s L_{ab}} \omega t, & 0 < \omega t < \phi_{AB} \\ I_{ab t_o} + \frac{(V_a-V_b)}{\omega_s L_{ab}} (\omega t - \phi_{AB}), & \phi_{AB} < \omega t < \pi \\ I_{abO} - \frac{(V_a+V_b)}{\omega_s L_{ab}} (\omega t - \pi), & \pi < \omega t < \pi + \phi_{AB} \\ -I_{ab t_o} - \frac{(V_a-V_b)}{\omega_s L_{ab}} (\omega t - \pi - \phi_{AB}), & \pi + \phi_{AB} < \omega t < 2\pi \end{cases}$$

The power flow between the three ports is indirectly proportional to the inductances, and it can be obtained by calculating the rectified average current (in Section 2.4.1) on each inductance present in the π equivalent circuit [5]-[6]:

$$P_{AB} = \frac{V_a V_b}{\omega_s L_{ab}} \phi_{AB} \left(\frac{\pi - |\phi_{AB}|}{\pi} \right)$$

$$P_{BC} = \frac{V_b V_c}{\omega_s L_{bc}} \phi_{AB} \left(\frac{\pi - |\phi_{BC}|}{\pi} \right)$$

$$P_{AC} = \frac{V_a V_c}{\omega_s L_{ac}} (\phi_{AB} - \phi_{BC}) \left(\frac{\pi - |\phi_{AB} - \phi_{BC}|}{\pi} \right)$$

2.2.1- The zero-voltage switching conditions

To verify the converter limitations with our application requirements, for the OBC and LDC converters, let us see the typical converter design. First of all, the design consists of finding the minimum inductance for the maximum power and the best relationship between the voltage gain and the zero voltage switching conditions. According to Figure 2-4 and Figure 2-3, the analysis for zero voltage switching in the three full-bridges result in 3 conditions:

$$i_a(0) < 0$$

$$i_b(t_o) > 0$$

$$i_c(t_o) > 0$$

Using the equivalent circuit from Figure 2-3-C:

$$i_a(t) = i_{ab}(t) + i_{ac}(t)$$

$$i_b(t) = i_{ab}(t) - i_{bc}(t)$$

$$i_c(t) = i_{bc}(t) + i_{ac}(t)$$

The conditions are considered in Section 2.4.1 and allow to obtain the following results:

$$\frac{(\pi - 2\phi_{AB})}{\pi} < \frac{V_{oA}}{V_{oB} N_{AB}} < \frac{\pi}{(\pi - 2\phi_{AB})} \quad (2)$$

$$\frac{(\pi - 3\phi_{BC})}{(\pi + \phi_{BC})} \leq \frac{V_{oA}}{V_{oC} N_{BC} N_{AB}} \leq \frac{(\pi - 2\phi_{BC})}{\pi} \quad (3)$$

Following the design requirements from Table 2-1 and Table 2-2, the conditions (2) and (3) are presented in Figure 2-5:

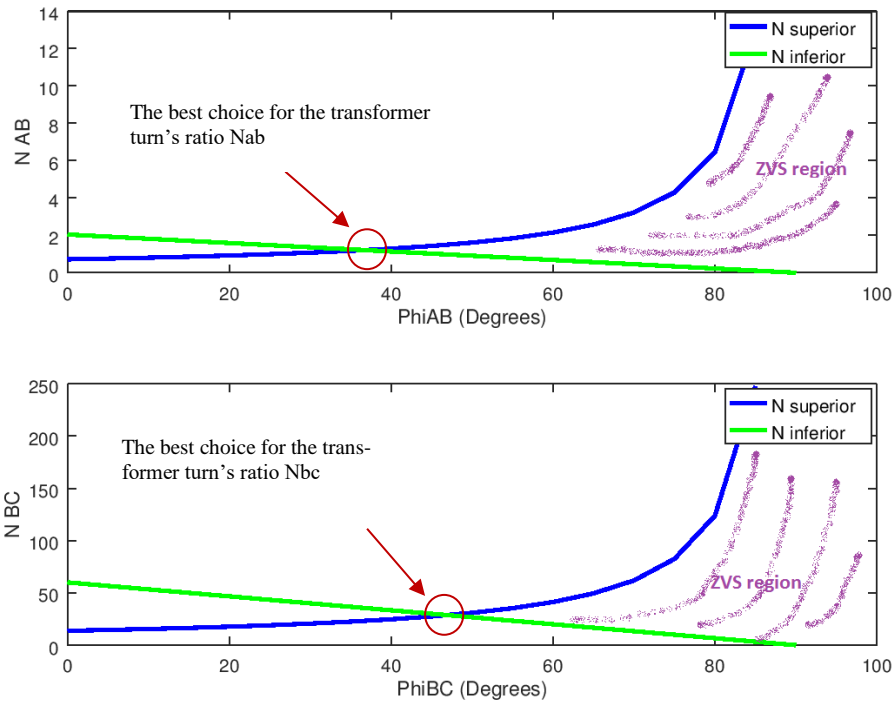


Figure 2-5: ZVS region for different voltage gains between V_a , V_b and V_c for different phase-shift angles (transferred power).

The transformer turn's ratio is designed to be close to the intersection points in Figure 2-5, representing the best choice for low power flow conditions. Out of this area, the current is no longer in the right direction allowing zero voltage switching. The power transferred between the ports is presented in Figure 2-6, and the converter design results in Table 2-3.

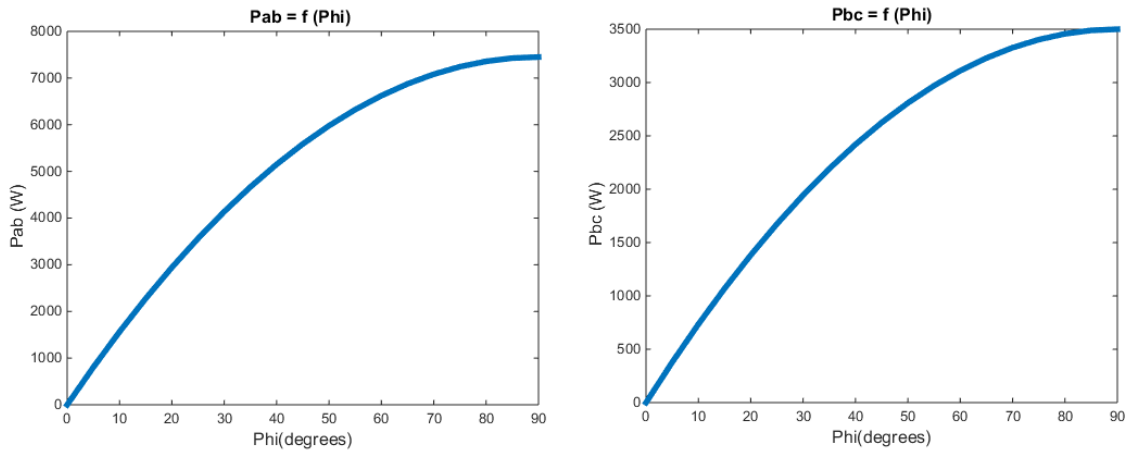


Figure 2-6: Power flow between ports A/B and B/C for different phase-shift angles.

Parameter	Symbol	Specification
1° side inductor – Port Va	La	12 μ H
2° side inductor – Port Vb	Lb	22.8 μ H
3° side inductor – Port Vc	Lc	0.065 μ H
DC side capacitance – Port Va	Ca	10 μ F
DC side capacitance – Port Vb	Cb	10 μ F
DC side capacitance – Port Vc	Cc	1.2 mF
Transformer turn's ratio OBC	Nab	1.37
Transformer turn's ratio LDC	Nbc	29

Table 2-3: The TAB parameters considering the requirements for OBC (7kW) and DC-DC (3.5kW) converters.

If we consider the battery charging process occurring into four phases, as presented in Figure 2-7, we see the converter's critical operating points where the ZVS does not occur and needs to be improved, at the first and last stages in Figure 2-7. This charging behavior is developed according to the maximum OBC's current capacity (I_{max}) and the battery SOC. The battery starts to be charged from a minimum voltage and when it achieves the nominal voltage, the charging remains for a certain time to complete the process, depending on the battery technology. With the conditions (2)-(3), the ZVS region can be represented for each bridge, in Figure 2-8. At nominal voltage, ZVS conditions are present. In buck mode, corresponding to the 1° phase of the process, the conditions are degraded in the second full-bridge, connected to the HV battery, limiting the minimum current. In boost mode, at low power, the ZVS conditions no longer exist in the first full-bridge.

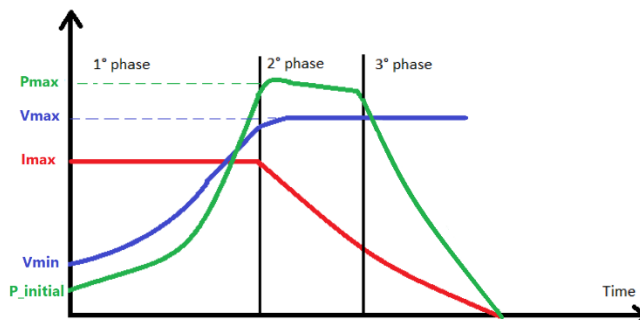


Figure 2-7: Battery charging process divided into 4 stages.

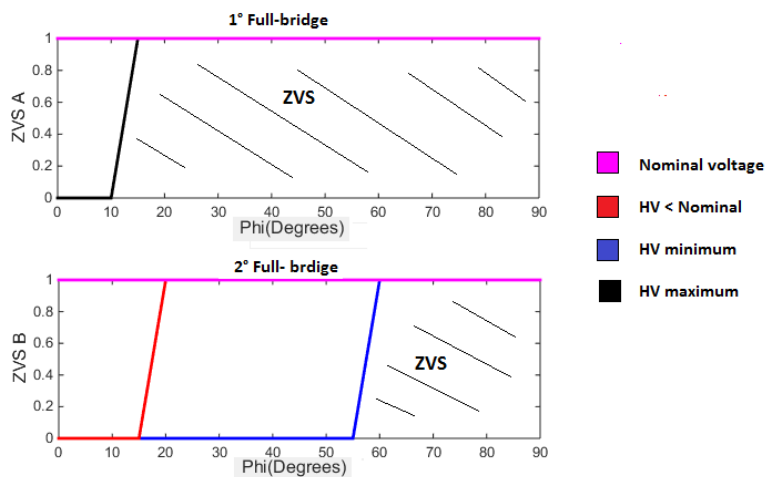


Figure 2-8: Minimum ZVS conditions on the 1° and 2° bridges of the converter during the OBC standalone mode.(1 indicates ZVS conditions, and 0 indicates hard-switching).

2.2.2- Extending the zero voltage switching regions

The use of this Three-port active bridge converter was proposed in [7] to integrate the OBC and DC-DC converters. In this reference, Zero Voltage Switching is achieved for specific design requirements by changing the duty cycle in the full-bridge associated with the voltage source requiring some variation range. The sum of the three transformer's currents contributes to obtaining better ZVS characteristics during reduced power flow exchange between the sources. However, the minimum current required by the MOSFET capacitance was disregarded, and only its direction was considered. In particular, the application conditions required in the OBC and DC-DC converters presented in Table 2-1 requires a wide voltage range for both HV and LV batteries, making the problem worse than the one studied in [7].

In order to adapt the use of a three-port active bridge for our requirements, the techniques presented in [8]-[9] are now included in the study. These techniques consist of adjusting the duty cycle of the bridges to produce an equivalent voltage in the transformer terminals matching with the input voltage and extending the soft-switching range of the converter.

As proposed in [8], the full-bridge structure associated with the voltage source that does not require a voltage variation range can be replaced by a half-bridge. This could be the case of the DC link connected to the first port in our study. However, during the battery discharging mode, it is desirable to regulate the Vdc link, according to the load connected on the AC side, whereas, it is sometimes not enough to leave the complete voltage regulation for the bidirectional PFC stage. Besides, in order to reduce the circulating current, it may be interesting to keep one more freedom degree in the analysis. There are five control variables: two external phase-shift angles, and three internal phase-shift angles (or duty cycles).

In Figure 2-9, we illustrate the duty cycles variation in the first and second full-bridges (D_a and D_b) to improve the ZVS conditions during the OBC operating mode. The same condition in (1) is maintained, and the switching times are defined as:

$$\begin{cases} \theta_{0.5} = \pi - \pi D_a \\ \theta_0 = \varnothing_{AB} \\ \theta_1 = \varnothing_{AB} + \pi - \pi D_b \\ \theta_2 = \pi \\ \theta_3 = \pi + \varnothing_{AB} \\ \theta_{3.5} = 2\pi - \pi D_a \\ \theta_4 = \pi + \varnothing_{AB} - \pi D_b \\ \theta_5 = 2\pi \end{cases}$$

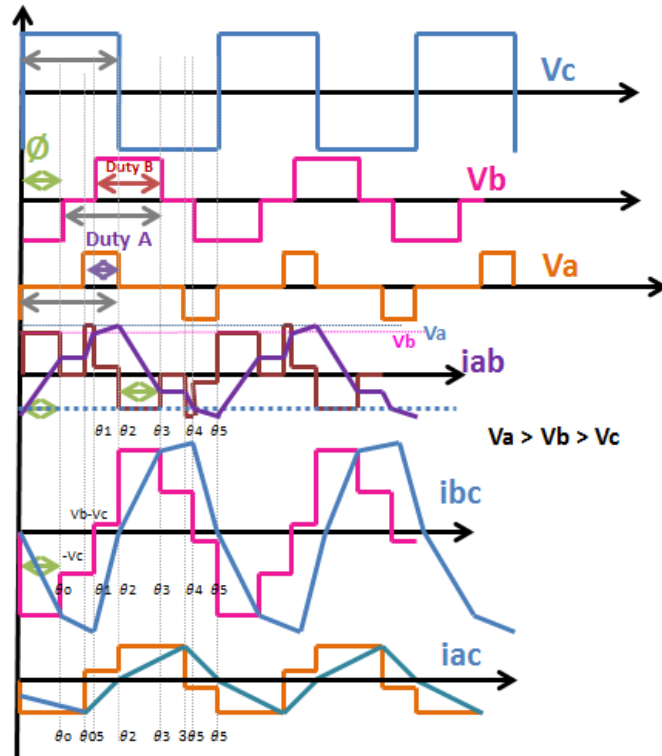


Figure 2-9: Voltage and current waveforms considering variable duty cycle for the first and second full-bridges.

The current between the voltage sources are written as:

$$i_{ab}(\omega t) = \begin{cases} -I_{ab0} + \frac{V_b}{\omega_s L_{ab}} \omega t, & 0 < \omega t < \theta_0 \\ I_{ab}(\theta_0), & \theta_0 < \omega t < \theta_{0.5} \\ I_{ab}(\theta_0) + \frac{V_a}{\omega_s L_{ab}} (\omega t - \theta_{0.5}), & \theta_{0.5} < \omega t < \theta_1 \\ I_{ab}(\theta_1) + \frac{(V_a - V_b)}{\omega_s L_{ab}} (\omega t - \theta_1), & \theta_1 < \omega t < \theta_2 \\ I_{ab0} - \frac{V_b}{\omega_s L_{ab}} (\omega t - \theta_2), & \theta_2 < \omega t < \theta_3 \\ I_{ab}(\theta_3), & \theta_3 < \omega t < \theta_{3.5} \\ -I_{ab}(\theta_0) - \frac{V_a}{\omega_s L_{ab}} (\omega t - \theta_{3.5}), & \theta_{3.5} < \omega t < \theta_4 \\ -I_{ab}(\theta_1) - \frac{(V_a - V_b)}{\omega_s L_{ab}} (\omega t - \theta_4), & \theta_4 < \omega t < \theta_5 \end{cases}$$

$$i_{bc}(\omega t) = \begin{cases} I_{bc0} - \frac{(V_b - V_c)}{\omega_s L_{bc}} \omega t, & 0 < \omega t < \theta_0 \\ I_{bc}(\theta_0) - \frac{V_c}{\omega_s L_{bc}} (\omega t - \theta_0), & \theta_0 < \omega t < \theta_1 \\ I_{bc}(\theta_1) + \frac{(V_b - V_c)}{\omega_s L_{bc}} (\omega t - \theta_1), & \theta_1 < \omega t < \theta_2 \\ I_{bc}(\theta_2) + \frac{(V_b + V_c)}{\omega_s L_{bc}} (\omega t - \theta_2), & \theta_2 < \omega t < \theta_3 \\ I_{bc}(\theta_3) + \frac{V_c}{\omega_s L_{bc}} (\omega t - \theta_3), & \theta_3 < \omega t < \theta_4 \\ I_{bc}(\theta_4) - \frac{(V_b - V_c)}{\omega_s L_{bc}} (\omega t - \theta_4), & \theta_4 < \omega t < \theta_5 \end{cases}$$

$$i_{ac}(\omega t) = \begin{cases} I_{ac0} - \frac{V_c}{\omega_s L_{ca}} \omega t, & 0 < \omega t < \theta_{0.5} \\ I_{ac}(\theta_{0.5}) + \frac{(V_a - V_c)}{\omega_s L_{ca}} (\omega t - \theta_{0.5}), & \theta_{0.5} < \omega t < \theta_2 \\ -I_{ac0} + \frac{V_c}{\omega_s L_{ca}} (\omega t - \theta_2), & \theta_2 < \omega t < \theta_{3.5} \\ -I_{ac}(\theta_{0.5}) - \frac{(V_a - V_c)}{\omega_s L_{ca}} (\omega t - \theta_{3.5}), & \theta_{3.5} < \omega t < \theta_5 \end{cases}$$

For ZVS in the full-bridges, we have the following conditions during the voltage rising and falling edges, as presented in Figure 2-9:

$$\begin{aligned} i_a(0) < 0 \text{ and } i_a(\theta_{0.5}) < 0 \\ i_b(\theta_0) > 0 \text{ and } i_b(\theta_1) > 0 \\ i_c(0) > 0 \end{aligned}$$

The conditions are valid for the boost mode under low output power conditions and are solved in Section 2.4.2 (Annexes):

$$\phi_{AB} \leq D_b \leq \pi - \phi_{AB} \quad \text{or} \quad \phi_{AB} \leq D_a \leq \pi - \phi_{AB}$$

$$\frac{(\pi D_b - 2\phi_{AB})}{2\pi D_a} < \frac{V_{oA}}{V_{oB} N_{AB}} < \frac{(\pi D_b - 4\phi_{AB})}{\pi D_a} \quad (4)$$

$$\frac{(2\pi D_a - \pi)}{\pi D_a} \leq \frac{V_{oA}}{V_{oC} (N_{BC} N_{AB})} < \frac{\pi}{\pi D_a} \quad (5)$$

$$\frac{N_{AB} N_{BC} V_{oC} (4\phi_{AB} - \pi)}{\pi D_b} \leq N_{AB} V_{oB} < \frac{V_{oA} (2\phi_{AB} + 3\pi D_a - 2\pi D_b)}{\pi D_b - 4\phi_{AB}} \quad (6)$$

Using the current definition between the ports, the RMS winding current and the average current in the voltage sources can be calculated, such as the power between the ports [10]-[11].

Figure 2-10 shows the output power and the RMS current between the ports with the adjusted duty-cycle in boost operating mode. The circulating energy is increased and helps to achieve soft-switching for small phase-shift angles.

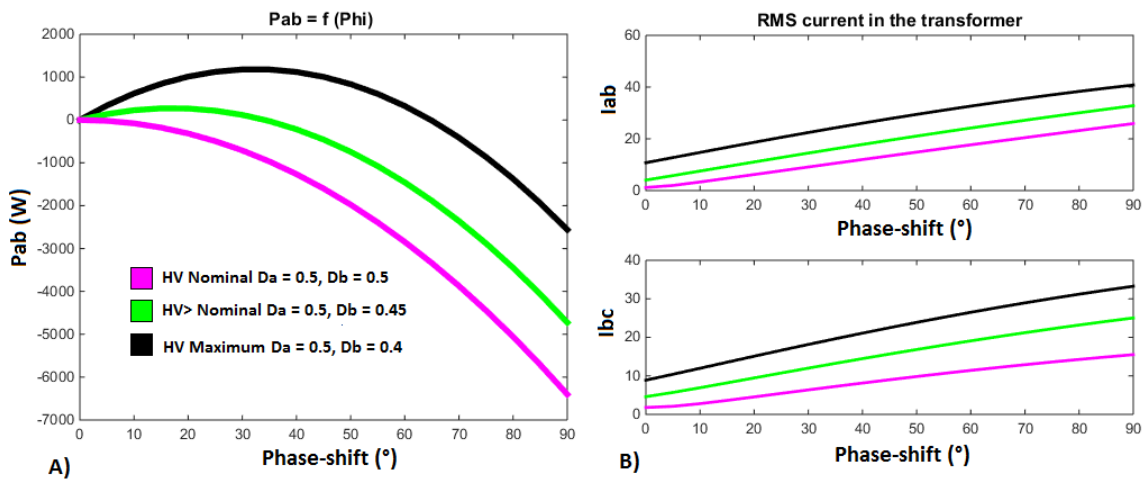


Figure 2-10: A) Output power depending on the phase-shift angle and internal duty-cycle of the output bridge (D_b) B) RMS current between the windings.

Figure 2-11 shows the power transferred, considering not only the step-up mode but also step-down. The duty-cycle of the second port (D_b) is adjusted to match the output voltage in the boost mode, while the duty cycle of the first port (D_a) is adjusted during the buck operation. During the voltage rising edges, the direction of the current is analyzed and presented in Figure 2-11-B. If the current is positive or negative according to the voltage direction to charge and discharge the capacitances, soft-switching can be obtained (1), otherwise it is classified as (0). By adjusting the first duty cycle (D_a) in buck mode, the soft-switching range of the second port (B) can be extended. During the boost mode, the duty cycle (D_b) is adjusted to benefit the first port (A).

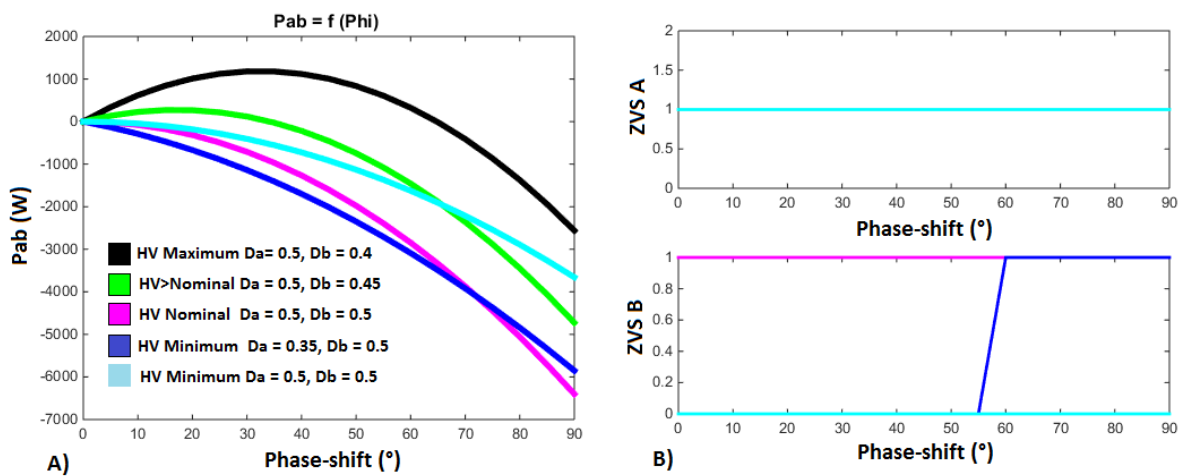


Figure 2-11: A) Output power depending on the phase-shift angle and internal duty-cycle angles (D_a , D_b) for buck and boost modes. B) Regions with extended zero-voltage switching in the first and second ports.

Therefore, the solution proposed in [5] takes benefit of the duty cycle control to extend the ZVS region during the first and last phases of the battery charging process. An example is presented in Figure 2-12. The second port connected to the HV battery requires the step-up mode, whereas the first port connected to the constant V_{dc} link voltage is under hard-switching. By adjusting the second full-bridge duty-cycle connected to the load, the equivalent current becomes negative during the voltage rising edge in the second and first sides, as represented in Figure 2-13. This is only possible because the duty cycle associated with each voltage source can be regulated to produce an equivalent RMS voltage in the transformer winding.

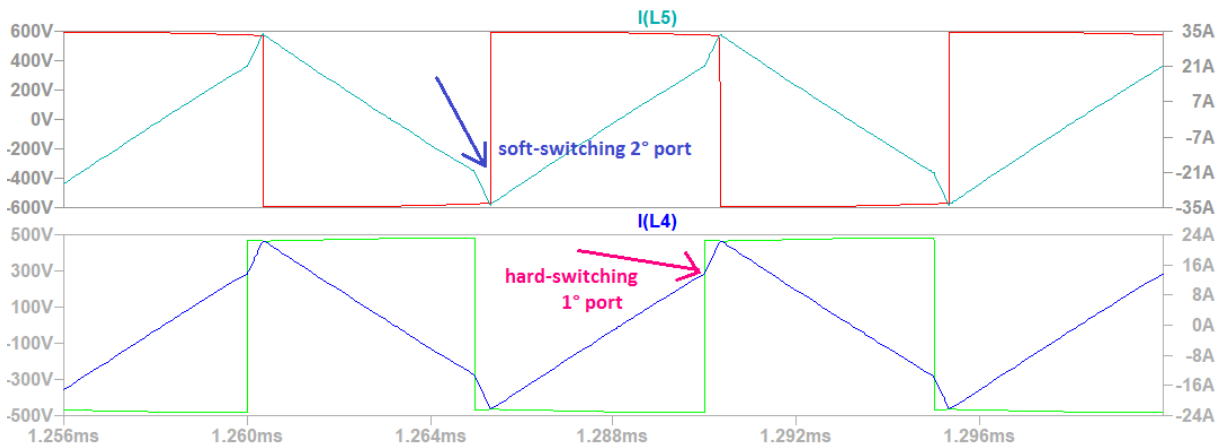


Figure 2-12: Boost mode for $V_{oB} = 600\text{ V}$ and $V_{oA} = 450\text{ V}$. Hard switching in the port connected to the lowest voltage.

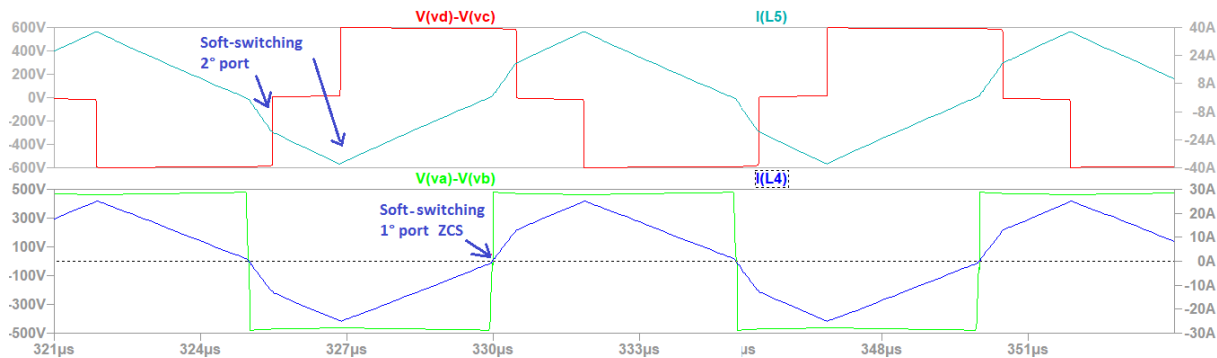


Figure 2-13: Boost mode for $V_{oB} = 600\text{ V}$ and $V_{oA} = 450\text{ V}$. Soft-switching obtained in both ports by adjusting the duty cycle of the 2° port (D_b).

A further analysis can be made to find the best combination of the duty cycle to increase the zero voltage switching range and reduce the circulating current for different situations. Considering the waveforms presented in Figure 2-14, an example is presented by using three duty-cycles, (D_a , D_b and D_c), and phase-shift angles, (ϕ_{AB} , ϕ_{BC}), to the optimization of OBC operating mode.

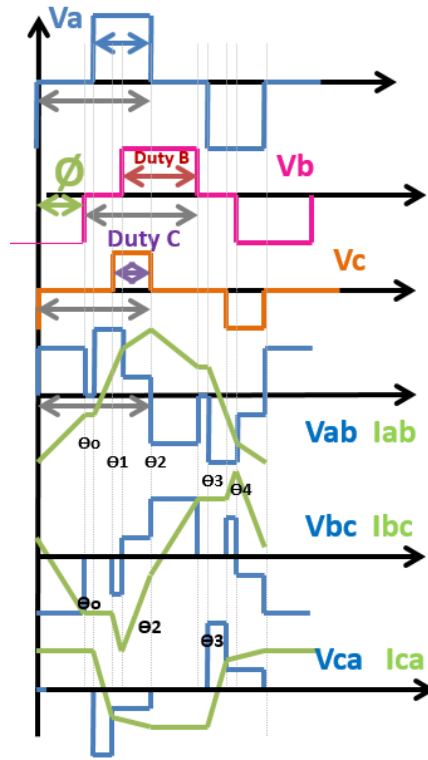


Figure 2-14: Voltage and current waveforms considering different duty cycles, $D_a \neq D_b \neq D_c$ in the three ports.

For ZVS in the full-bridges, we have the following conditions during the voltage rising and falling edges, as presented in Figure 2-14Figure 2-9:

$$\begin{aligned}
 i_a(0) < 0 \quad \text{and} \quad i_a(\theta_{0.5}) < 0 \\
 i_b(\theta_0) > 0 \quad \text{and} \quad i_b(\theta_{1.5}) > 0 \\
 i_c(\theta_1) > 0 \quad \text{and} \quad i_c(0) > 0
 \end{aligned}$$

The conditions are valid for the boost mode under low output power conditions and are solved in Section 2.4.3 (Annexes):

$$\frac{V_a}{V_b} > \frac{\pi D_b - \phi_{AB}}{\pi D_a} \quad \text{and} \quad \frac{V_a}{V_c} \leq \frac{\pi D_c}{\pi D_a - 2\pi D_c} \quad (7)$$

$$\frac{V_b}{V_a} > \frac{(2\pi D_b - \pi D_a - 4\phi_{AB})}{\pi D_a - \phi_{AB}} \quad \text{and} \quad \frac{V_b}{V_c} \geq \frac{\pi D_c}{\pi D_b - \phi_{AB}} \quad (8)$$

$$\frac{V_c}{V_a} < \frac{D_a}{D_c} \quad \text{and} \quad \frac{V_c}{V_b} \geq \frac{(\pi D_b - 3\phi_{AB})}{\pi D_c} \quad (9)$$

The current direction during the transistors switching are the minimum conditions for soft-switching, but are not enough. Their amplitude is also an important parameter to obtain the charge and discharge of the parasitic capacitances. In Figure 2-2, when S_1 is turned-off at $t=0$ and considering parasitic capacitances C_1 and C_2 associated with S_1 and S_2 , respectively, the inductance L_a needs to provide

energy to discharge C_2 and charge C_1 , and circulate through the body diode of S_2 , before its turning-on.

At $t = 0$:

$$i_{L_A}(t = 0) = I_{min}$$

$$v_{C_1}(t = 0) = 0$$

$$v_{C_2}(t = 0) = V_{oA}$$

After the turn-off delay time:

$$i_{L_A}(t = t_{dead}) = 0$$

$$v_{C_1}(t = t_{dead}) = V_{oA}$$

$$v_{C_2}(t = t_{dead}) = 0$$

$$i_{L_A} = (C_1 + C_2) \frac{dv_C}{dt}$$

$$E_{energy} = \int_0^{t_{dead}} V_{oB}' i_{L_A} dt = (C_1 + C_2) V_{oB}' \int_0^{t_{dead}} \frac{dv_C}{dt} dt = (C_1 + C_2) V_{oB}' (V_{oA}) = \frac{1}{2} L_A (I_{min}^2)$$

$$(C_1 + C_2) V_{oB} N_{AB} V_{oA} = \frac{1}{2} L_A (I_{min}^2) \Rightarrow I_{min} = \sqrt{\frac{2 (C_1 + C_2) V_{oB} N_{AB} V_{oA}}{L_A}} \quad (10)$$

The conditions (7), (8), (9), and (10) are summarized in Figure 2-15, where the soft-switching regions of the converter are compared in boost operating mode. Without the duty cycle variation, the first full-bridge (Port A) loses the soft-switching conditions as soon as the power flow is decreased (blue line). The adjust in the duty cycle associated with the port connected to the boosted voltage (D_b), allows to extend the soft conditions for smaller power flows (red line). The results are improved by adjusting the duty cycle of the third and second port together (green line, D_b , and D_c), compared to the typical control strategy.

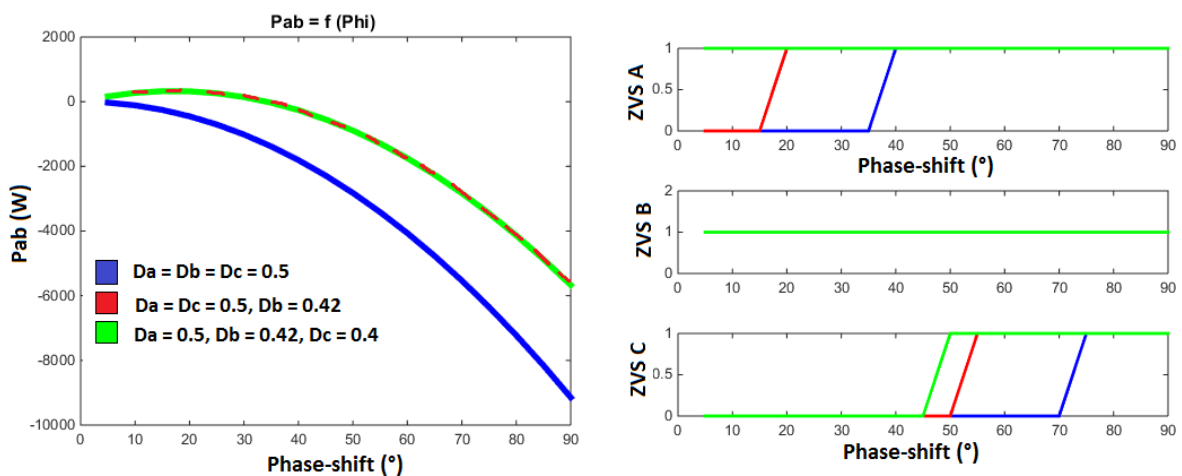


Figure 2-15: Power transfer between the first and second port and the ZVS conditions for the boost mode. By adjusting the duty cycles D_b and D_c , soft switching conditions can be attempted in the first full-bridge (Port A) at low power.

In Figure 2-16, the last stage during the OBC charging process is improved by changing the duty cycle associated with the second and the third full-bridges when the battery is almost completely charged (at low output current condition). The duty cycle is controlled at 50% for the first full-bridge, 40% in the second bridge and 45% in the third full-bridge.

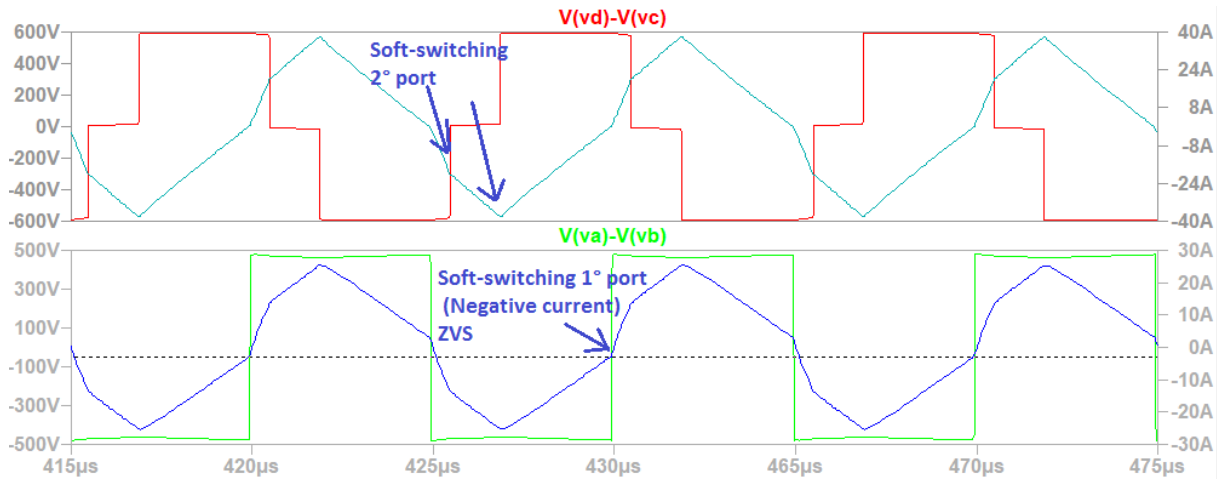


Figure 2-16: Duty cycle modified to expand the ZVS region at high output voltage and light power flow condition. $D_a = 50\%$, $D_b = 40\%$ and $D_c = 45\%$.

This duty cycle adaptation can be used to expand the converter soft switching conditions, but the RMS current is also increased due to the reactive circulating energy in OBC and LDC modes. For light power flow condition, when the duty cycle control is used to extend the ZVS region for the OBC operating mode (G2V), the current circulates in the low voltage side to compensate the energy in the other two ports. As presented in some references [10], [13], the sum of the currents during the switching instants is always zero. That is why Zero Current Switching is achieved for several operating points when the power flow decreases. The next sub-section presents a second strategy to extend the ZVS region of the converter.

2.2.3- The three-port active bridge with additional parallel inductors

The three-port converter with additional duty cycle control can extend the ZVS operation region of the converter application, but it increases the transformer's RMS current. In this section, we study the following method: add parallel inductors to obtain better performance in the OBC standalone mode. An effort is made for this specific mode because it has higher power than the LDC. Besides, the high voltage ratio between them induces circulating current in the third port side, compromising the conversion efficiency. The idea of ZVS region expansion with additional inductor is then to provide the minimum current to charge and discharge the MOSFET capacitances. In this concept, the duty cycle can be maintained constant at 50% or used to decrease the circulating current at the low voltage side,

instead of providing the minimum conditions for ZVS. The additional inductors are connected in parallel to the transformer terminals, only in the high-voltage sides, as shown in Figure 2-17.

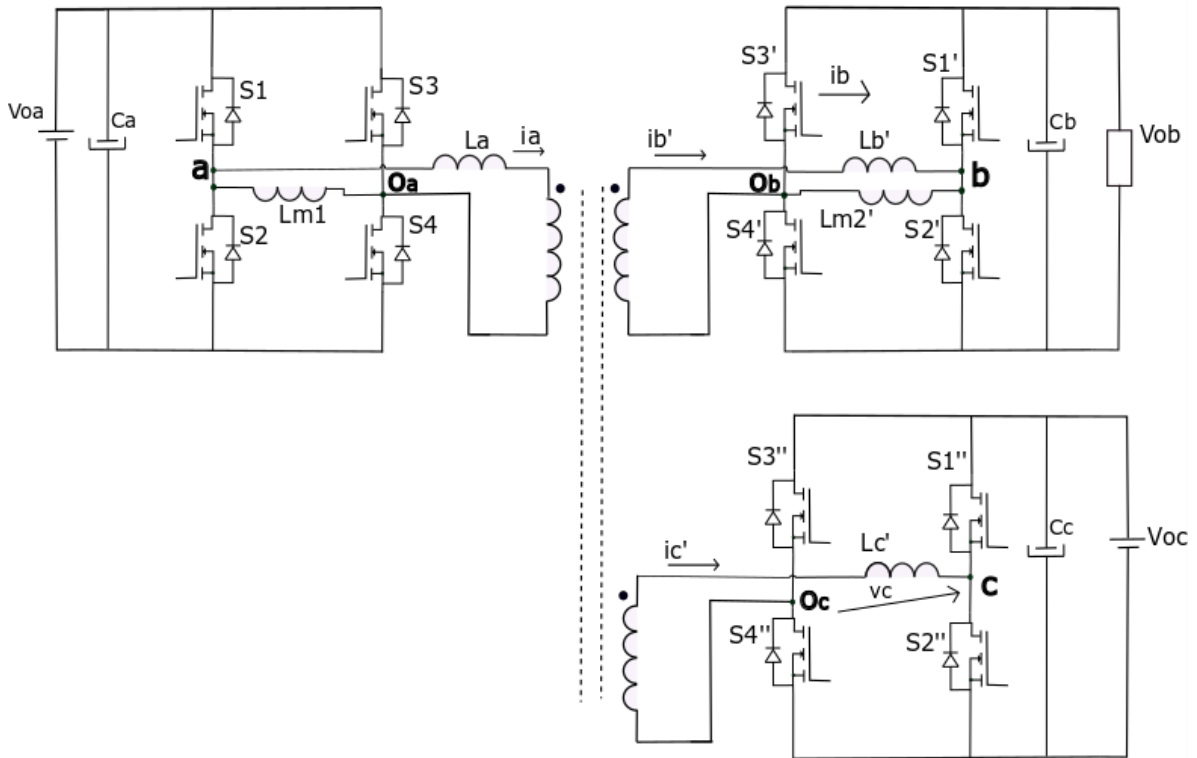


Figure 2-17: Three-port active bridge with additional inductances connected in parallel to the AC side of the V_{oA} and V_{oB} ports.

In the analysis, the current in the additional inductors are calculated and added to the main current in the transformer obtained in the previous sections:

$$i_{h_A}(t) = i_{L_{m1}}(t) + i_{L_a}(t)$$

$$i_{h_B}(t) = -i_{L_{m2}}(t) + i_{L_a}'(t)$$

i_{h_A} and i_{h_B} are the currents in each AC side connected to the first and the second voltage sources, V_a and V_b . The π equivalent circuit is presented in Figure 2-18-C.

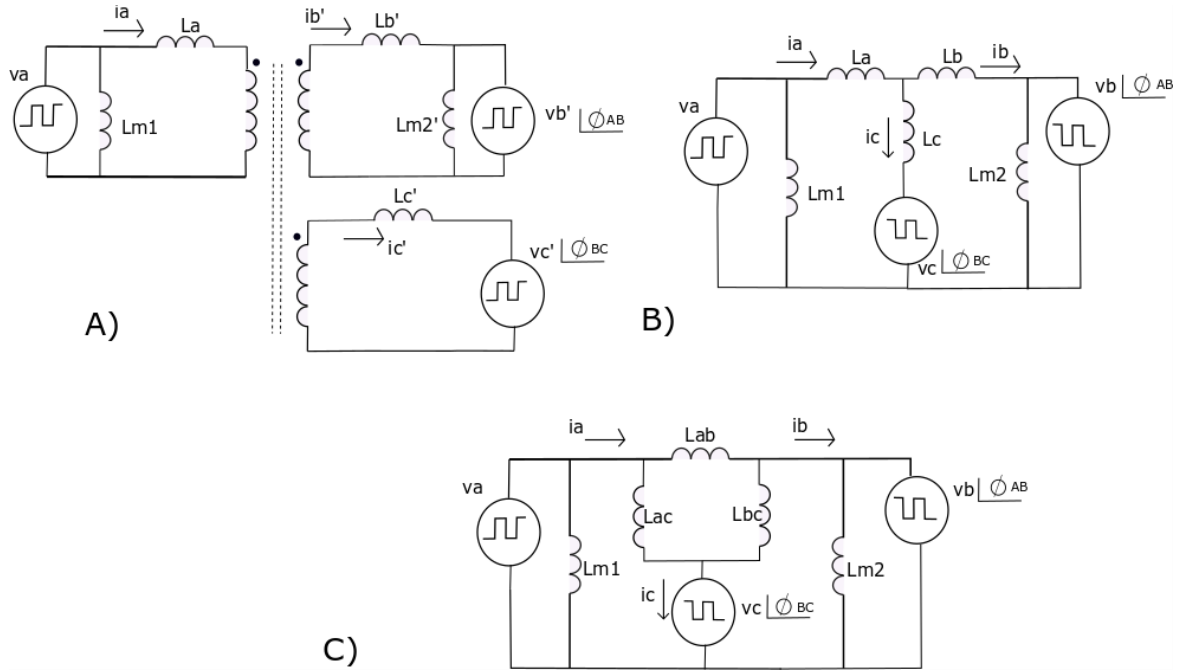


Figure 2-18: a) Equivalent circuit with L_{m1} and L_{m2} . b) Simplified equivalent circuit. c) Equivalent π circuit.

In the three-port converter, considering the capacitances C_1 and C_2 associated to the transistors S_1 and S_2 , respectively, when the transistor S_1 is turned-off at $t=0$, the current must discharge and charge the capacitances C_2 and C_1 and circulate across the body diode of the transistor S_2 , before its turning-on. At the switching time $t=0$:

$$i_{fullbridge_A}(t) = i_{L_A}(t=0) + i_{L_{m1}}(t=0) > I_{min}$$

$$i_{fullbridge_B}(t) = [i_{L_A'}(t=0)] \frac{N_A}{N_B} - i_{L_{m2}}(t=0) < -I_{min}$$

$$v_{C_1}(t=0) = 0$$

$$v_{C_2}(t=0) = V_{oA}$$

$$v_{L_{m1}}(t=0) = V_{oA}$$

After the turn-off delay time:

$$i_{L_A}(t=t_{dead}) = 0$$

$$i_{L_{m1}}(t=t_{dead}) = 0$$

$$v_{C_1}(t=t_{dead}) = V_{oA}$$

$$v_{C_2}(t=t_{dead}) = 0$$

$$v_{L_{m1}}(t=t_{dead}) = 0$$

$$i_x = i_{L_A} + i_{L_{m1}} = (C_1 + C_2) \frac{dv_C}{dt}$$

$$v_{L_a} = v_{L_{m1}} - V_{oB}'$$

$$v_{L_{m1}} = L_{m1} \frac{di_{L_{m1}}}{dt} \quad i_{L_{m1}} = \frac{v_{L_{m1}}}{L_{m1}} (t_s)$$

$$E_{energy} = \int_0^{t_s} (V_{oB}') i_x dt = (C_{eq}) (V_{oB}') \int_0^{t_s} \frac{dv_c}{dt} dt = (C_{eq}) (V_{oB}') (V_{oA}) = \frac{1}{2} (L_A + L_{m1}) (I_{min}^2)$$

$$(C_{eq}) V_{oB} N_{AB} V_{oA} = \frac{1}{2} (L_{m1} + L_A) (I_{min}^2) \Rightarrow I_{min} = \sqrt{\frac{2 (C1+C2) (V_{oB} N_{AB}) V_{oA}}{L_A + L_{m1}}} \quad (6)$$

The current in the transformer windings can be minimized because the inductors L_m now contributes with a parcel to charge and discharge the capacitances, reducing the circulating current in the LV side of the converter. When the converter step-up the output voltage, at 600V, we verify that it is no more necessary to regulate the duty cycle associated with the second bridge to obtain the ZVS, as shown in Figure 2-19.

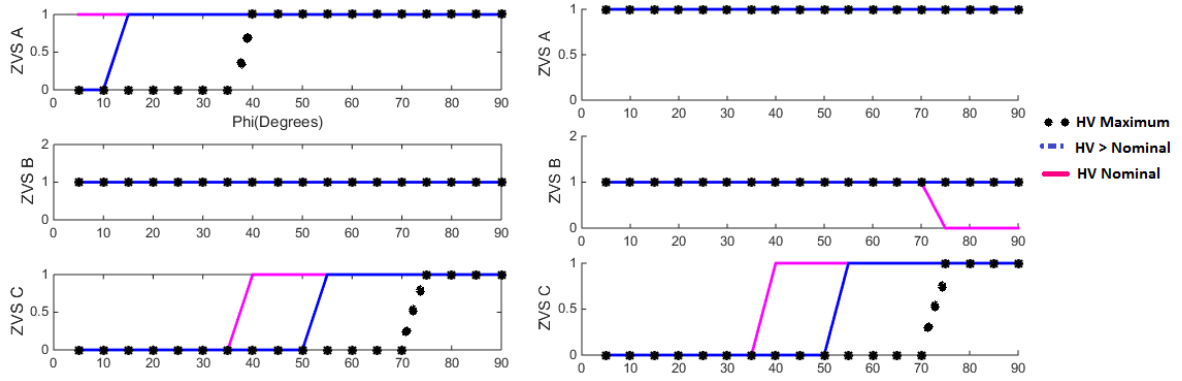


Figure 2-19: The ZVS region achieved during step-up operation of the OBC mode. a) Without the parallel inductances, $L_{m1} = L_{m2} = \infty$. b) $L_{m1} = L_{m2} = 60 \mu H$.

The next simulations show the results obtained with the additional inductors introduced in the analysis of the ZVS conditions. The same parameters from the previous simulations are used with additional inductances of $60 \mu H$. The parameters are presented in Table 2-4.

Parameter	Symbol	Specification
1° side inductor – Port V_a	L_a	12 μH
2° side inductor – Port V_b	L_b	22.8 μH
3° side inductor – Port V_c	L_c	0.065 μH
DC side capacitance – Port V_a	C_a	10 μF
DC side capacitance – Port V_b	C_b	10 μF
DC side capacitance – Port V_c	C_c	1.2 mF
Transformer turn's ratio OBC	N_{ab}	1.37
Transformer turn's ratio LDC	N_{bc}	29
Parallel inductor	L_{m1}	60 μH / 11 A_{rms} / 26 A_{peak}
Parallel inductor	L_{m2}	60 μH / 11 A_{rms} / 26 A_{peak}
MOSFETs parasitic capacitance	C_{oss}	200 pF

Table 2-4: The parameters of the Three-port active bridge used for the OBC and LDC simulation.

The step-up operation is illustrated in Figure 2-20. ZVS conditions are achieved for both ports. Nevertheless, a high current peak in the inductances is observed with an increased current ripple. This solution expands also the converter ZVS operation region, but it is necessary to pay the price of additional inductors and an increased current ripple.

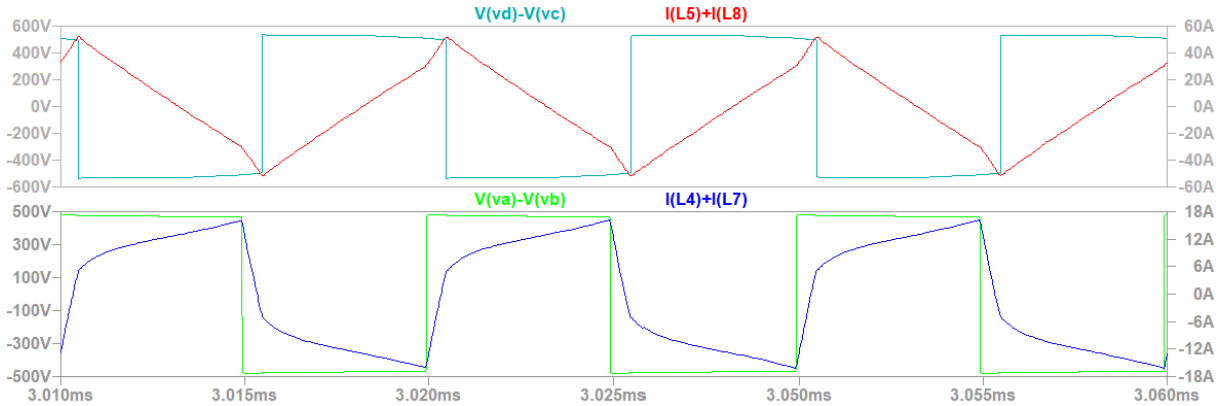


Figure 2-20: Step-up operation, high output voltage $V_{oB} = 600\text{ V}$, $V_{oA} = 450\text{ V}$.

The association of this solution with the duty-cycle control can be better investigated with an optimization routine to reduce the circulating energy and obtain the ZVS conditions. A Multi-objective optimization routine in Matlab is considered to solve problems with more than one function, containing four variables. It results in a Pareto front that contains the best solutions to minimize the functions. The three main functions are the expressions to determine the RMS currents in each port: I_{Arms} , I_{Brms} , and I_{Crms} . The variables are the duty cycle associated with the three full-bridges, and phase-shift angle: D_a , D_b , D_c , and ϕ . The constraints are the power flow directions between the ports and the current amplitude during the switching intervals to ensure ZVS:

$$i_a(0) \leq 0 ; i_a(0t5) \leq 0 \quad (\text{Theoretical ZVS of Bridge A}) \quad (1^\circ)$$

$$i_b(t_\phi) \leq 0 ; i_b(1t5) \leq 0 \quad (\text{Theoretical ZVS of Bridge B}) \quad (2^\circ)$$

$$x_{lower} \leq P_{ab} \leq x_{upper} \quad (3^\circ)$$

$$|I_{C_{DC}}| \leq \text{Minimum allowed current for OBC standalone operation} \quad (4^\circ)$$

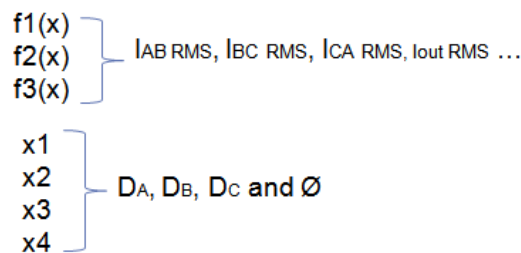


Figure 2-21: Example of multi-functions optimization applied to the Three-active bridge converter.

It is difficult to identify the best performance for both operation modes, between the OBC and the LDC, using the entire topology for multiple operating points. Generally, during the design, the priority is the nominal condition. The converter's critical operating points, during the beginning and the end of the battery charging process can be improved later with the control of the duty cycles. The solution containing parallel inductors keeps ZVS operation under light load and high voltage gain. However, especial attention should be paid to the transformer design, because of the increased circulating current.

Input Parameters							Simulation Results				
P(kW)	R _L	∅ _{AB}	∅ _{BC}	D _a	D _b	D _c	I _{aRMS}	I _{bRMS}	I _{cRMS}	V _{out} (V)	ΔI _{Cout}
0.62	600	10°	-5°	0.5	0.5	0.5	15.2	62.4	560	632	76.1
4.62	10.7	35°	17°	0.5	0.5	0.5	19.4	22.5	140	232	8.9
7.70	29.9	36°	11°	0.5	0.5	0.5	24.6	46.5	331	484	55.4

Table 2-5: Optimized parameters of the converter with additional inductors L_{m1} and $L_{m2} = 60\mu H$.

Input Parameters							Simulation Results				
P(kW)	R _L	∅ _{AB}	∅ _{BC}	D _a	D _b	D _c	I _{aRMS}	I _{bRMS}	I _{cRMS}	V _{out} (V)	ΔI _{Cout}
1.90	20	45°	25°	0.5	0.5	0.5	14.6	21.3	119.9	460	17.6
1.62	5	20°	10°	0.32	0.5	0.5	22.4	28.4	119.6	252	3.1
6.65	29	45°	20°	0.5	0.5	0.5	17.2	27.4	161.5	565	18.5
1.40	120	110°	60°	0.5	0.34	0.46	26.1	37.7	164	535	12.2

Table 2-6: Optimized parameters of the converter without the additional inductances, with only the duty cycle control.

From the observed results, during the OBC standalone operation mode, at low output voltage, 220V, the results revealed a strong influence of the duty cycle associated with the second full-bridge (D_b) on the circulating current in the low voltage side of the converter, I_{C_RMS} . When D_b is smaller than 50%, the $I_{C_{rms}}$ current tends to increase, so it is preferable to keep this duty cycle the closest as possible of 50%. The duty cycle of the first port connected to the voltage source V_{oA} (D_a) also influences the converter step-down operation during the beginning of the battery charging process. Without the additional parallel inductors, it is necessary to reduce the duty cycle D_a in the case of a low output voltage. However, this strategy increases the RMS current value in the third idled port (in the LV side that is not participating in the energy exchange). For the same conditions, the third port's duty cycle, D_c , has almost no influence on the $I_{C_{rms}}$ current during the converter step-down operation.

For a high voltage gain (the end of the battery charging process) and at light load, the duty cycle associated with the first full-bridge, D_a cannot be reduced and only assume values above 50%. Normally, the duty cycle associated with the third port, D_c , can be calculated to expand the ZVS region in the 1° solution (without the additional parallel inductors). The current in the transformer is, however, also increased.

Without the parallel inductors, the soft-switching region is extended by changing the duty cycle of the bridges, but this solution is not enough to keep ZVS with power levels under 1kW, only ZCS can be maintained. With the parallel inductors, ZVS is extended to the critical phase of the battery charging process, characterized by a high voltage gain and light load. Nevertheless, it increases the RMS current. Therefore, special care must be taken to evaluate the impact of increased RMS current in the transformer and transistor's power losses.

2.3- Conclusion

The use of the Three-active Bridge to integrate the OBC and LDC converters was investigated to integrate both converters with bidirectional power flow and Zero voltage switching. The association of phase-shift control and internal duty cycle variation proposed in the literature [10], [13] allows extending the soft-switching converter region. In [14], an integrated power unit containing the OBC and LDC converters is proposed using this topology. The solution proposed, however, does not aim at the operation of the LDC in reverse mode.

The addition of inductors connected in parallel to at least two bridges on the AC side is also investigated to provide enough current to charge and discharge the transistor capacitances and thus keep ZVS even at zero load. The solutions show the extended operation of the converter under ZVS for light power conditions, but it also results in increased circulation current and conduction power losses. In this scenario, Chapter 3 introduces a new topology to integrate the OBC and LDC converters allowing zero voltage switching in the entire power range.

2.4- Annexes

2.4.1- Current and power flow between the ports

The power flow between the three ports using the π equivalent circuit is demonstrated in [5], and the circuit proposed in Figure 2-3-c is valid if the magnetizing inductance is much higher than the series inductances used for the power transfer. Therefore:

$$L_{ab} = \frac{L_a L_b + L_b L_c + L_a L_c}{L_c} \quad L_{bc} = \frac{L_a L_b + L_b L_c + L_a L_c}{L_a} \quad L_{ac} = \frac{L_a L_b + L_b L_c + L_a L_c}{L_b}$$

$$V_a = V_{oA} \quad V_b = V_{oB} \frac{N_A}{N_B} = V_{oB} N_{AB} \quad V_c = V_{oC} \frac{N_A}{N_B} \frac{N_B}{N_C} = V_{oC} N_{AB} N_{BC}$$

$$L_b = L'_b N_{AB}^2 \quad L_c = L'_c N_{AB}^2 N_{BC}^2$$

The output and input average current value (without considering the losses), can be calculated by the integral of the respective currents $i_{ab}(t)$, $i_{bc}(t)$ and $i_{ca}(t)$:

$$i_{ab}(\omega t) = \begin{cases} -I_{ab0} + \frac{(V_a + V_b)}{\omega_s L_{ab}} \omega t, & 0 < \omega t < \phi_{AB} \\ I_{abt_0} + \frac{(V_a - V_b)}{\omega_s L_{ab}} (\omega t - \phi_{AB}), & \phi_{AB} < \omega t < \pi \\ I_{ab0} - \frac{(V_a + V_b)}{\omega_s L_{ab}} (\omega t - \pi), & \pi < \omega t < \pi + \phi_{AB} \\ -I_{abt_0} - \frac{(V_a - V_b)}{\omega_s L_{ab}} (\omega t - \pi - \phi_{AB}), & \pi + \phi_{AB} < \omega t < 2\pi \end{cases}$$

$$I_{ab} = \frac{2}{\pi} \int_0^\pi i_{ab} d\omega t = \frac{2}{\pi} \int_0^\pi i_{ab} d\omega t$$

$$I_{ab0} = \frac{-(V_a + V_b)\phi_{AB}}{2\omega_s L_{ab}} - \frac{(V_a - V_b)(\pi - \phi_{AB})}{2\omega_s L_{ab}}$$

$$I_{ab}(t_0) = \frac{(V_a + V_b)\phi_{AB}}{2\omega_s L_{ab}} - \frac{(V_a - V_b)(\pi - \phi_{AB})}{2\omega_s L_{ab}}$$

$$i_{bc}(\omega t) = \begin{cases} I_{bc0} - \frac{(V_b - V_c)}{\omega_s L_{bc}} \omega t, & 0 < \omega t < \phi_{BC} \\ I_{bct_0} + \frac{(V_b - V_c)}{\omega_s L_{bc}} (\omega t - \phi_{BC}), & \phi_{BC} < \omega t < \pi + \phi_{BC} \\ -I_{bct_0} - \frac{(V_b - V_c)}{\omega_s L_{bc}} (\omega t - \pi - \phi_{BC}), & \pi + \phi_{BC} < \omega t < 2\pi \end{cases}$$

$$I_{bc0} = -\frac{(V_b - V_c)(\pi - 2\phi_{BC})}{2\omega_s L_{bc}}$$

$$I_{bc}(t_0) = -\frac{(V_b - V_c)\phi_{BC}}{2\omega_s L_{bc}}$$

$$i_{ca}(\omega t) = \begin{cases} I_{ca0} - \frac{(V_a + V_c)}{\omega_s L_{ca}} \omega t, & 0 < \omega t < \phi_{BC} \\ I_{cat_0} + \frac{(V_c - V_a)}{\omega_s L_{ca}} (\omega t - \phi_{BC}), & \phi_{BC} < \omega t < \pi \\ -I_{ca0} + \frac{(V_a + V_c)}{\omega_s L_{ca}} (\omega t - \pi), & \pi < \omega t < \pi + \phi_{BC} \\ -I_{cat_0} - \frac{(V_c - V_a)}{\omega_s L_{ca}} (\omega t - \phi_{BC} - \pi), & \pi + \phi_{BC} < \omega t < 2\pi \end{cases}$$

$$I_{ca0} = \frac{-(V_a + V_c)\phi_{BC}}{2\omega_s L_{ca}} + \frac{(V_c - V_a)(\pi - \phi_{BC})}{2\omega_s L_{ca}}$$

$$I_{ca}(t_o) = \frac{-(V_a + V_c)\phi_{BC}}{\omega_s L_{ca}} + \frac{(V_c - V_a)(\pi - \phi_{BC})}{2\omega_s L_{ca}}$$

$$I_{ca}(t_2) = \frac{-(V_a + V_c)\phi_{BC}}{\omega_s L_{ca}} + \frac{(V_c - V_a)(\pi - \phi_{BC})}{\omega_s L_{ca}}$$

$$P_{AB} = \frac{2}{\pi} \int_0^\pi i_{ab}(V_a - V_b - \phi_{AB})^* d\omega t = \frac{V_a V_b}{\omega_s L_{ab}} \phi_{AB} \left(\frac{\pi - |\phi_{AB}|}{\pi} \right)$$

$$P_{BC} = \frac{V_b V_c}{\omega_s L_{bc}} \phi_{BC} \left(\frac{\pi - |\phi_{BC}|}{\pi} \right)$$

$$P_{AC} = \frac{V_a V_c}{\omega_s L_{ac}} (\phi_{AB} - \phi_{BC}) \left(\frac{\pi - |\phi_{AB} - \phi_{BC}|}{\pi} \right)$$

For ZVS in the three full-bridges, we have three conditions during the voltage rising and falling edges of the current waveforms, as presented in Figure 2-4 following the π equivalent circuit:

$$i_a(0) < 0$$

$$i_b(t_o) > 0$$

$$i_c(t_o) > 0$$

Using the current relationships:

$$i_a(t) = i_{ab}(t) + i_{ac}(t)$$

$$i_b(t) = i_{ab}(t) - i_{bc}(t)$$

$$i_c(t) = i_{ac}(t) + i_{bc}(t)$$

The first condition is equivalent to:

$$i_{ab}(0) < 0 \text{ and } i_{ac}(0) \leq 0$$

$$\frac{-(V_a + V_b)\phi_{AB}}{2\omega_s L_{ab}} - \frac{(V_a - V_b)(\pi - \phi_{AB})}{2\omega_s L_{ab}} < 0$$

$$\frac{V_a}{V_b} > \frac{(\pi - 2\phi_{AB})}{\pi}$$

$$\frac{(V_a + V_c)\phi_{BC}}{2\omega_s L_{ca}} - \frac{(V_c - V_a)(\pi - \phi_{BC})}{2\omega_s L_{ca}} \leq 0$$

$$\frac{V_a}{V_c} \leq \frac{(\pi - 2\phi_{BC})}{\pi}$$

The second condition is equivalent to:

$$i_{ab}(t_o) > 0 \text{ and } -i_{bc}(t_o) \geq 0$$

$$\frac{(V_a + V_b)\phi_{AB}}{2\omega_s L_{ab}} - \frac{(V_a - V_b)(\pi - \phi_{AB})}{2\omega_s L_{ab}} > 0$$

$$\frac{V_a(2\phi_{AB} - \pi)}{2\omega_s L_{ab}} > \frac{-V_b\pi}{2\omega_s L_{ab}}$$

$$\frac{V_b}{V_a} > \frac{\pi - 2\phi_{AB}}{\pi}$$

$$\frac{(V_b - V_c)\phi_{BC}}{2\omega_s L_{bc}} \geq 0$$

$$\frac{V_b}{V_c} \geq 1$$

The third condition is equivalent to:

$$i_{bc}(t_o) > 0 \text{ and } -i_{ca}(t_o) \geq 0$$

$$\frac{-(V_b - V_c)\phi_{BC}}{2\omega_s L_{bc}} > 0$$

$$V_b < V_c$$

$$\frac{(V_a + V_c)\phi_{BC}}{\omega_s L_{ca}} - \frac{(V_c - V_a)(\pi - \phi_{BC})}{2\omega_s L_{ca}} \geq 0$$

$$\frac{V_a}{V_c} \geq \frac{(\pi - 3\phi_{BC})}{(\phi_{BC} + \pi)}$$

2.4.2- Current and power flow between the ports with duty-cycle control (Da and Db)

Following the current waveforms in Figure 2-9, we can write the current in each time interval to deduce the soft-switching conditions and the average power transmitted between the ports as a function of the duty cycle in the first and second full-bridges, and phase-shift angles.

$$i_{ab}(\omega t) = \begin{cases} -I_{ab0} + \frac{V_b}{\omega_s L_{ab}} \omega t, & 0 < \omega t < \theta_0 \\ I_{ab}(\theta_0), & \theta_0 < \omega t < \theta_{0.5} \\ I_{ab}(\theta_0) + \frac{V_a}{\omega_s L_{ab}} (\omega t - \theta_{0.5}), & \theta_{0.5} < \omega t < \theta_1 \\ I_{ab}(\theta_1) + \frac{(V_a - V_b)}{\omega_s L_{ab}} (\omega t - \theta_1), & \theta_1 < \omega t < \theta_2 \\ I_{ab0} - \frac{V_b}{\omega_s L_{ab}} (\omega t - \theta_2), & \theta_2 < \omega t < \theta_3 \\ I_{ab}(\theta), & \theta_3 < \omega t < \theta_{3.5} \\ -I_{ab}(\theta_0) - \frac{V_a}{\omega_s L_{ab}} (\omega t - \theta_{3.5}), & \theta_{3.5} < \omega t < \theta_4 \\ -I_{ab}(\theta_1) - \frac{(V_a - V_b)}{\omega_s L_{ab}} (\omega t - \theta_4), & \theta_4 < \omega t < \theta_5 \end{cases}$$

$$i_{bc}(\omega t) = \begin{cases} I_{bc0} - \frac{(V_b - V_c)}{\omega_s L_{bc}} \omega t, & 0 < \omega t < \theta_0 \\ I_{bc}(\theta_0) - \frac{V_c}{\omega_s L_{bc}} (\omega t - \theta_0), & \theta_0 < \omega t < \theta_1 \\ I_{bc}(\theta_1) + \frac{(V_b - V_c)}{\omega_s L_{bc}} (\omega t - \theta_1), & \theta_1 < \omega t < \theta_2 \\ -I_{bc0} + \frac{(V_b + V_c)}{\omega_s L_{bc}} (\omega t - \theta_2), & \theta_2 < \omega t < \theta_3 \\ -I_{bc}(\theta_0) + \frac{V_c}{\omega_s L_{bc}} (\omega t - \theta_3), & \theta_3 < \omega t < \theta_4 \\ -I_{bc}(\theta_1) - \frac{(V_b - V_c)}{\omega_s L_{bc}} (\omega t - \theta_4), & \theta_4 < \omega t < \theta_5 \end{cases}$$

$$i_{ac}(\omega t) = \begin{cases} I_{ac0} - \frac{V_c}{\omega_s L_{ca}} \omega t, & 0 < \omega t < \theta_{0.5} \\ I_{ac}(\theta_{0.5}) + \frac{(V_a - V_c)}{\omega_s L_{ca}} (\omega t - \theta_{0.5}), & \theta_{0.5} < \omega t < \theta_2 \\ I_{ac}(\theta_2) + \frac{V_c}{\omega_s L_{ca}} (\omega t - \theta_2), & \theta_2 < \omega t < \theta_{3.5} \\ I_{ac}(\theta_{3.5}) - \frac{(V_a - V_c)}{\omega_s L_{ca}} (\omega t - \theta_{3.5}), & \theta_{3.5} < \omega t < \theta_5 \end{cases}$$

$$i_{ac}(\omega t) = \begin{cases} I_{ac0} - \frac{V_c}{\omega_s L_{ca}} \omega t, & 0 < \omega t < \theta_{0.5} \\ I_{ac}(\theta_{0.5}) + \frac{(V_a - V_c)}{\omega_s L_{ca}} (\omega t - \theta_{0.5}), & \theta_{0.5} < \omega t < \theta_2 \\ -I_{ac0} + \frac{V_c}{\omega_s L_{ca}} (\omega t - \theta_2), & \theta_2 < \omega t < \theta_{3.5} \\ -I_{ac}(\theta_{0.5}) - \frac{(V_a - V_c)}{\omega_s L_{ca}} (\omega t - \theta_{3.5}), & \theta_{3.5} < \omega t < \theta_5 \end{cases}$$

$$\left\{ \begin{array}{l} \theta_{0.5} = \pi - \pi D_a \\ \theta_o = \emptyset_{AB} \\ \theta_1 = \emptyset_{AB} + \pi - \pi D_b \\ \theta_2 = \pi \\ \theta_3 = \pi + \emptyset_{AB} \\ \theta_{3.5} = 2\pi - \pi D_a \\ \theta_4 = 2\pi + \emptyset_{AB} - \pi D_b \\ \theta_5 = 2\pi \end{array} \right.$$

$$I_{ab}(0) = -\frac{V_a \pi D_a}{2\omega_s L_{ab}} + \frac{V_b}{2\omega_s L_{ab}} (-2\emptyset_{AB} + \pi D_b)$$

$$I_{bc}(0) = \frac{V_b(2\emptyset_{AB} - \pi D_b)}{2\omega_s L_{bc}} + \frac{V_c}{2\omega_s L_{bc}} (2\emptyset_{AB} + \pi - 2\pi D_b)$$

$$I_{ac}(0) = \frac{V_c \pi}{2\omega_s L_{ac}} - \frac{V_a \pi D_a}{2\omega_s L_{ac}}$$

For ZVS in the three full-bridges, we have five conditions during the voltage rising and falling edges of the current waveforms, according to the equivalent circuit in Figure 2-3 and Figure 2-9:

$$i_a(0) < 0 \quad \text{and} \quad i_a(\theta_{0.5}) \leq 0$$

$$i_b(\theta_o) > 0 \quad \text{and} \quad i_b(\theta_1) \geq 0$$

$$i_c(\theta_o) > 0$$

Using the current relationships:

$$i_a(t) = i_{ab}(t) + i_{ac}(t)$$

$$i_b(t) = i_{ab}(t) - i_{bc}(t)$$

$$i_c(t) = i_{ac}(t) + i_{bc}(t)$$

The first conditions are equivalent to:

$$i_{ab}(0) < 0 \quad \text{and} \quad i_{ac}(0) \leq 0$$

$$i_{ab}(\theta_{0.5}) < 0 \quad \text{and} \quad i_{ac}(\theta_{0.5}) \leq 0$$

$$-\frac{V_a \pi D_a}{2\omega_s L_{ab}} + \frac{V_b}{2\omega_s L_{ab}} (-2\emptyset_{AB} + \pi D_b) < 0 \quad \text{and} \quad \frac{V_c \pi}{2\omega_s L_{ac}} - \frac{V_a \pi D_a}{2\omega_s L_{ac}} \leq 0$$

$$\frac{V_a}{V_b} > \frac{(-2\emptyset_{AB} + \pi D_b)}{\pi D_a} \quad \text{and} \quad \frac{\pi}{\pi D_a} \leq \frac{V_a}{V_c}$$

$$-I_{ab0} + \frac{V_b \emptyset_{AB}}{\omega_s L_{ab}} < 0 \quad \text{and} \quad I_{ac0} - \frac{V_c (\pi - \pi D_a)}{\omega_s L_{ca}} \leq 0$$

$$\frac{V_a}{V_b} < \frac{(\pi D_b - 4\phi_{AB})}{\pi D_a} \quad \text{and} \quad \frac{(-\pi + 2\pi D_a)}{\pi D_a} \leq \frac{V_a}{V_c}$$

The conditions in the second full-bridge are equivalent to:

$$i_{ab}(\theta_0) > 0 \quad \text{and} \quad -i_{bc}(\theta_0) \geq 0$$

$$i_{ab}(\theta_1) > 0 \quad \text{and} \quad -i_{bc}(\theta_1) \geq 0$$

$$-I_{ab0} + \frac{V_b \phi_{AB}}{\omega_s L_{ab}} > 0 \quad \text{and} \quad -I_{bc0} + \frac{(V_b - V_c)}{\omega_s L_{bc}} \phi_{AB} \geq 0$$

$$\frac{V_a \pi D_a}{2\omega_s L_{ab}} + \frac{V_b(4\phi_{AB} - \pi D_b)}{2\omega_s L_{ab}} > 0 \quad \text{and} \quad \frac{V_b \pi D_b}{2\omega_s L_{bc}} + \frac{V_c(-4\phi_{AB} - \pi + 2\pi D_b)}{2\omega_s L_{bc}} \geq 0$$

$$\frac{V_b}{V_a} > \frac{\pi D_a}{(\pi D_b - 4\phi_{AB})} \quad \text{and} \quad \frac{V_b}{V_c} \geq \frac{(4\phi_{AB} + \pi - 2\pi D_b)}{\pi D_b}$$

$$i_{ab}(\theta_1) = \frac{V_a(3\pi D_a + 2\phi_{AB} - 2\pi D_b)}{2\omega_s L_{ab}} + \frac{V_b(4\phi_{AB} - \pi D_b)}{2\omega_s L_{ab}} > 0$$

$$-i_{bc}(\theta_1) = \frac{V_b \pi D_b}{2\omega_s L_{bc}} + \frac{V_c(-4\phi_{AB} + \pi)}{2\omega_s L_{bc}} \geq 0$$

$$\frac{V_b}{V_a} > \frac{(3\pi D_a + 2\phi_{AB} - 2\pi D_b)}{(\pi D_b - 4\phi_{AB})} \quad \text{and} \quad \frac{V_b}{V_c} \geq \frac{(4\phi_{AB} - \pi)}{\pi D_b}$$

The condition in the third full-bridge is equivalent to:

$$i_{ac}(0) > 0 \quad \text{and} \quad i_{bc}(0) \geq 0$$

$$\frac{V_c \pi}{2\omega_s L_{ac}} - \frac{V_a \pi D_a}{2\omega_s L_{ac}} > 0 \quad \text{and} \quad \frac{V_b(2\phi_{AB} - \pi D_b)}{2\omega_s L_{bc}} + \frac{V_c}{2\omega_s L_{bc}}(2\phi_{AB} + \pi - 2\pi D_b) \geq 0$$

$$\frac{V_c}{V_a} > \frac{\pi D_a}{\pi} \quad \text{and} \quad \frac{V_c}{V_b} \geq \frac{(\pi D_b - 2\phi_{AB})}{(2\phi_{AB} + \pi - 2\pi D_b)}$$

Considering the waveforms presented in Figure 2-9, the different duty-cycles and phase-shift angles are taken into account by the 1^o harmonic component transferring the real power between the ports

$$\Phi_{ABfundamental} = -\Phi_{AB} + \frac{(D_b - D_a) \pi}{2}$$

$$\Phi_{BCfundamental} = \Phi_{AB} + \pi - \frac{(D_b + D_a) \pi}{2}$$

$$\Phi_{CAfundamental} = \frac{3 D_a \pi}{2} - \pi$$

2.4.3- Current and power flow between the ports with duty cycle control (Da, Db and Dc)

According to Figure 2-14, the current between the ports can be written as:

$$i_{ab}(\omega t) = \begin{cases} I_{ab0} + \frac{V_b}{\omega_s L_{ab}} \omega t, & 0 < \omega t < \theta_0 \\ I_{ab}(\theta_0), & \theta_0 < \omega t < \theta_{0.5} \\ I_{ab}(\theta_0) + \frac{V_a}{\omega_s L_{ab}} (\omega t - \theta_{0.5}), & \theta_{0.5} < \omega t < \theta_{1.5} \\ I_{ab}(\theta_{1.5}) + \frac{(V_a - V_b)}{\omega_s L_{ab}} (\omega t - \theta_{1.5}), & \theta_{1.5} < \omega t < \theta_2 \\ -I_{ab0} - \frac{V_b}{\omega_s L_{ab}} (\omega t - \theta_2), & \theta_2 < \omega t < \theta_{2.5} \\ -I_{ab}(\theta_0), & \theta_{2.5} < \omega t < \theta_3 \\ -I_{ab}(\theta_0) - \frac{V_a}{\omega_s L_{ab}} (\omega t - \theta_3), & \theta_3 < \omega t < \theta_4 \\ -I_{ab}(\theta_{1.5}) - \frac{(V_a - V_b)}{\omega_s L_{ab}} (\omega t - \theta_4), & \theta_4 < \omega t < \theta_{4.5} \end{cases}$$

$$I_{ab0} = \frac{V_a(-\pi D_a) + V_b(-3\Phi_{AB} + \pi D_b)}{2\omega_s L_{ab}}$$

$$i_{bc}(\omega t) = \begin{cases} I_{bc0} - \frac{V_b}{\omega_s L_{bc}} \omega t, & 0 < \omega t < \theta_0 \\ I_{bc}(\theta_0), & \theta_0 < \omega t < \theta_1 \\ I_{bc}(\theta_0) - \frac{V_c}{\omega_s L_{bc}} (\omega t - \theta_1), & \theta_1 < \omega t < \theta_{1.5} \\ I_{bc}(\theta_{1.5}) + \frac{(V_b - V_c)}{\omega_s L_{bc}} (\omega t - \theta_{1.5}), & \theta_{1.5} < \omega t < \theta_2 \\ -I_{bc0} + \frac{V_b}{\omega_s L_{bc}} (\omega t - \theta_2), & \theta_2 < \omega t < \theta_{2.5} \\ -I_{bc}(\theta_0), & \theta_{2.5} < \omega t < \theta_{3.5} \\ -I_{bc}(\theta_0) + \frac{V_c}{\omega_s L_{bc}} (\omega t - \theta_{3.5}), & \theta_{3.5} < \omega t < \theta_4 \\ -I_{bc}(\theta_{1.5}) - \frac{(V_b - V_c)}{\omega_s L_{bc}} (\omega t - \theta_4), & \theta_4 < \omega t < \theta_{4.5} \end{cases}$$

$$I_{bc_o} = \frac{V_c(\pi D_c) + V_b(3\phi_{AB} - \pi D_b)}{2\omega_s L_{bc}}$$

$$i_{ac}(\omega t) = \begin{cases} I_{ac_o}, & 0 < \omega t < \theta_{0.5} \\ I_{ac_o} - \frac{V_a}{\omega_s L_{ca}}(\omega t - \theta_{0.5}), & \theta_{0.5} < \omega t < \theta_1 \\ I_{ac}(\theta_1) + \frac{(V_c - V_a)}{\omega_s L_{ca}}(\omega t - \theta_1), & \theta_1 < \omega t < \theta_2 \\ -I_{ac_o}, & \theta_2 < \omega t < \theta_3 \\ -I_{ac_o} + \frac{V_a}{\omega_s L_{ca}}(\omega t - \theta_3), & \theta_3 < \omega t < \theta_{3.5} \\ -I_{ac}(\theta_1) - \frac{(V_c - V_a)}{\omega_s L_{ca}}(\omega t - \theta_{3.5}), & \theta_{3.5} < \omega t < \theta_{4.5} \end{cases}$$

$$I_{ac_o} = \frac{V_a(\pi D_a - 2\pi D_c) - V_c(\pi D_c)}{2\omega_s L_{ac}}$$

$$\begin{cases} \theta_{0.5} = \pi - \pi D_a \\ \theta_o = \phi_{AB} \\ \theta_1 = \pi - \pi D_c \\ \theta_{1.5} = 2\phi_{AB} + \pi - \pi D_b \\ \theta_2 = \pi \\ \theta_{2.5} = \pi + \phi_{AB} \\ \theta_3 = 2\pi - \pi D_a \\ \theta_{3.5} = 2\pi - \pi D_c \\ \theta_4 = 2\pi + 2\phi_{AB} - \pi D_b \\ \theta_{4.5} = 2\pi \end{cases}$$

For ZVS in the three full-bridges, there are six conditions during the voltage rising and falling edges, according to the equivalent circuit in Figure 2-3 and Figure 2-14:

$$\begin{aligned} i_a(0) < 0 \quad \text{and} \quad i_a(\theta_{0.5}) < 0 \\ i_b(\theta_o) > 0 \quad \text{and} \quad i_b(\theta_{1.5}) > 0 \\ i_c(\theta_1) > 0 \quad \text{and} \quad i_c(0) > 0 \end{aligned}$$

Using the current relationships:

$$\begin{aligned} i_a(t) &= i_{ab}(t) + i_{ac}(t) \\ i_b(t) &= i_{ab}(t) - i_{bc}(t) \\ i_c(t) &= i_{ac}(t) + i_{bc}(t) \end{aligned}$$

The conditions in the first full-bridge are equivalent to:

$$i_{ab}(0) < 0 \quad \text{and} \quad i_{ac}(0) \leq 0$$

$$i_{ab}(\theta_{0.5}) < 0 \text{ and } i_{ac}(\theta_{0.5}) \leq 0$$

$$\frac{V_a}{V_b} > \frac{\pi D_b - \phi_{AB}}{\pi D_a} \text{ and } \frac{V_a}{V_c} \leq \frac{\pi D_c}{\pi D_a - 2\pi D_c} \quad (76)$$

The conditions in the second full-bridge are equivalent to:

$$i_{ab}(\theta_0) > 0 \text{ and } -i_{bc}(\theta_0) \geq 0$$

$$i_{ab}(\theta_{1.5}) > 0 \text{ and } -i_{bc}(\theta_{1.5}) \geq 0$$

$$\frac{V_b}{V_a} > \frac{(2\pi D_b - \pi D_a - 4\phi_{AB})}{\pi D_a - \phi_{AB}} \text{ and } \frac{V_b}{V_c} \geq \frac{\pi D_c}{\pi D_b - \phi_{AB}} \quad (7)$$

The conditions in the third full-bridge are equivalent to:

$$i_{ac}(\theta_1) > 0 \text{ and } i_{bc}(\theta_1) \geq 0$$

$$i_{ac}(0) > 0 \text{ and } i_{bc}(0) \geq 0$$

$$\frac{V_c}{V_a} < \frac{D_a}{D_c} \text{ and } \frac{V_c}{V_b} \geq \frac{(\pi D_b - 3\phi_{AB})}{\pi D_c} \quad (8)$$

$$\phi_{AB \text{ fundamental}} = \frac{(D_a + D_b)\pi - 2\phi_{AB} - 2\pi}{2}$$

$$\phi_{BC \text{ fundamental}} = 2\phi_{AB} + \frac{(D_b - D_c)\pi}{2}$$

$$\phi_{CA \text{ fundamental}} = \frac{(3D_a - D_c)\pi}{2}$$

When the converter operates in the standalone OBC mode, the power flow must occur only between the ports V_a and V_b , thus the phase-shift between the first and the third port must be zero:

$$\phi_{CA \text{ fundamental}} = \frac{(3D_a - D_c)\pi}{2} = 0, \quad D_a = \frac{D_c}{3}$$

2.5- References

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3- The Bidirectional Three-port Current-fed Parallel resonant converter

3.1- Introduction

As introduced in Chapter 1, resonant converters present some advantages for medium-high power and frequency applications. The switching frequency can be increased to aim at high power density without increasing switching power losses. Hence, another idea to implement the OBC and LDC converters is the use of resonant elements associated with phase-shift control, such as the work developed in [1]. Alternatively, we can think in the development about converters with two or more cascaded stages to address the voltage variation range and profit from resonant strategies, such as the three-port converter with unitary voltage-gain, as presented by authors in [2] and [3]. In this case, as illustrated in Figure 3-1, the three-port bidirectional converter does not have to regulate the voltage. This function is transmitted to the converter connected in cascade with it, just before the HV and LV batteries. The advantage of this solution is the minimization of the current and voltage stresses in the transformer and the power transistors. Thus, a major part of the integrated converter can achieve a more compact design because of reduced power losses and a minimized volume occupied by the passive elements, the transformer, the power transistors and the heat cooling system. In order to propose a new topology, in this thesis, we explore the use of a three-port current-fed resonant converter, as presented in Figure 3-2.

The DC side inductors connected in series to the three voltage sources, V_1 , V_2 and V_3 , smooth the current and if the inductance is large enough, the DC side currents can be considered almost constants. Despite the representation in Figure 3-2, where an equivalent impedance represents the voltage sources V_2 and V_3 , the complete symmetry in the structure allows bidirectional power flow between the three ports. The passive elements connected in parallel to the AC side of each full-bridge are the resonant elements. The converter works as the dual of a series LC resonant converter. Under ideal conditions, the transformer has a very large magnetizing inductance and negligible leakage inductance.

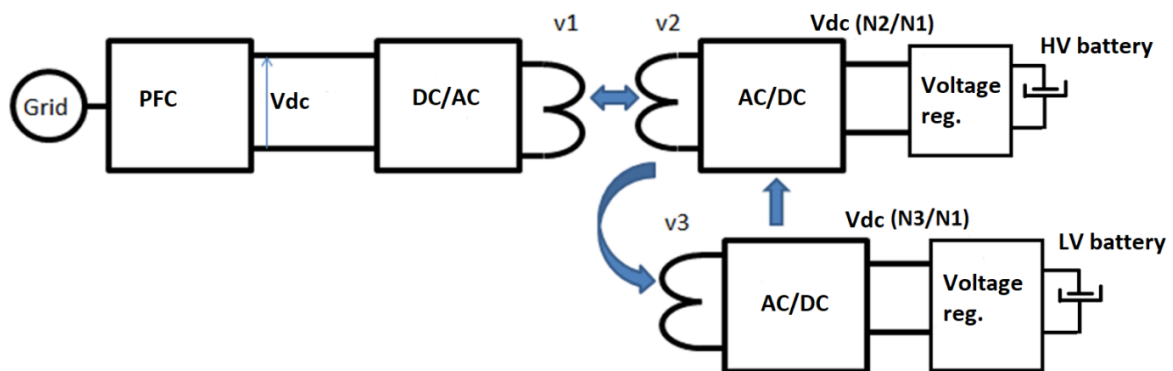


Figure 3-1: The proposition to integrate the OBC and LDC converters with 3 converter stages: A bidirectional PFC + the isolated three-port bidirectional converter + a non-isolated DC/DC converter to voltage regulation purposes.

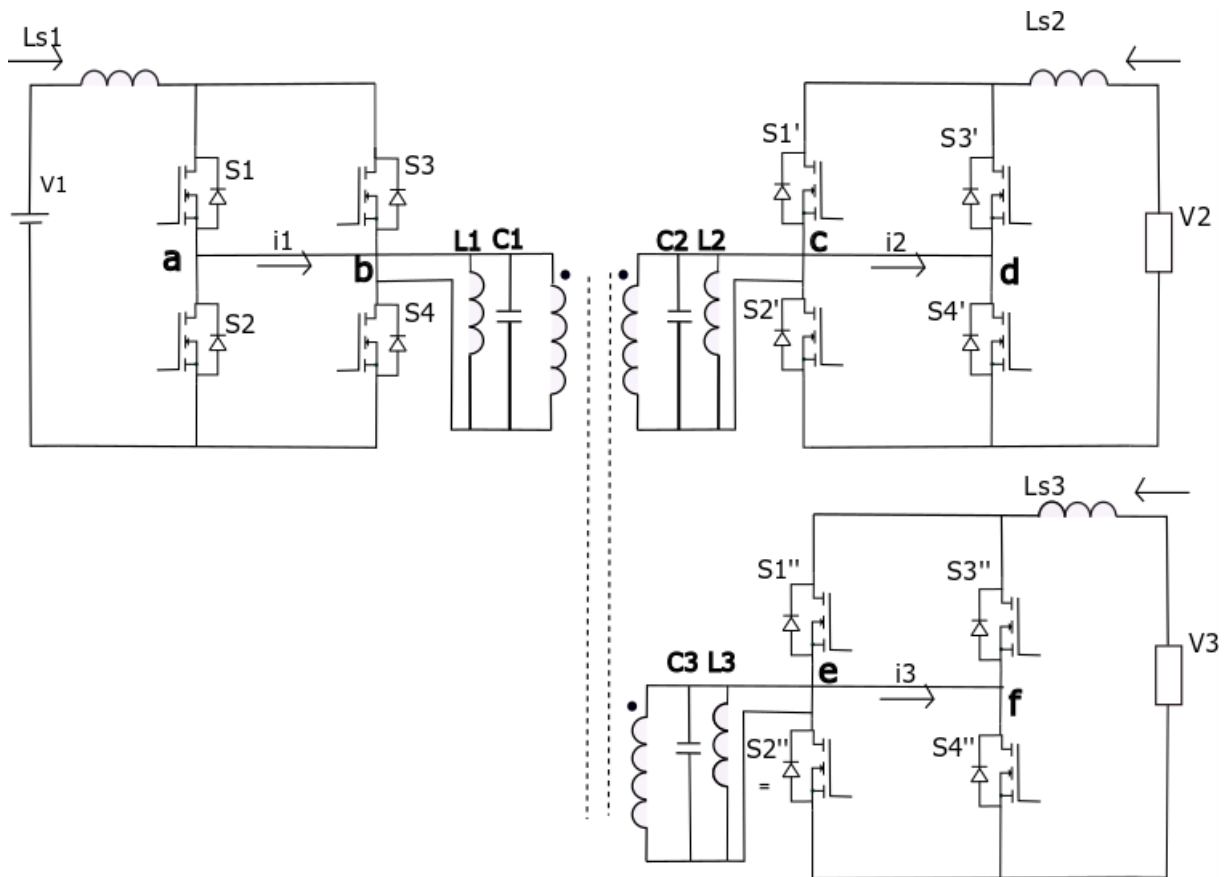


Figure 3-2: The bidirectional, Three-port current-fed parallel resonant converter.

3.2- The converter operation analysis

The converter operation consists in to command the three ports simultaneously on the same frequency. The transistors from each bridge are commuted in pairs, in the diagonal physical disposition and each full-bridge works as a current inverter. While a pair of transistors is in conduction mode, the current is injected through the transformer and the parallel circuit. The resulting current waveform on the AC side has a square waveform due to the smoothing DC side inductors, L_{S1} , L_{S2} and L_{S3} . For security reasons, to prevent open-circuit state and current discontinuity, it is recommended to keep an overlap before switching the transistors. During the overlap time, the four transistors in the same bridge are in conduction mode, before turning off the opposite transistor pair.

If the switching frequency is equal to the resonant frequency given by the equivalent parallel elements, the parallel cell connected to each AC side will operate as a band-pass filter, presenting very high impedance to the voltage harmonics, except to the fundamental frequency. The voltage first harmonic is the only component applied to the transformer. The current in the parallel inductor and the capacitor are also sinusoidal and oscillate between both components. The voltage becoming sinusoidal naturally passes at zero, thus being only necessary zero voltage crossing detection to turn on

the transistors under soft-switching conditions. During the voltage crossing, the parallel inductor handles the resonant current by discharging the parallel capacitor, but we could also think about discharging the parasitic capacitors associated with the transistors. Note that the soft-switching conditions still exist under light power operation. The current transmitted by the transformer over a half period between its different sides is the average value of the current in the DC loads. If the load is zero, the average current is zero, but the soft-switching conditions still exist because of the parallel resonant tank circuit.

To ensure symmetric currents in the transformer and to limit the impact of leakage inductance, the resonant cell may be placed in each one of the three full-bridges, justifying the existence of the pairs $L_1 C_1$, $L_2 C_2$ and $L_3 C_3$. However, nothing inhibits the existence of a single parallel inductor remained to one of the transformer sides or the integration of this element in the magnetizing inductance of the transformer if the leakage inductances are negligible.

At the resonant frequency, the first harmonic of the current and the transformer voltage are in phase and the conversion's performance achieves its maximum.

If the switching frequency is inferior to the resonant frequency, the impedance of the parallel inductor becomes slightly smaller than the parallel capacitor's impedance, thus increasing a little bit the resonant time. The converter passes to the discontinuous mode operation because the current needs extra time to achieve the zero crossing. A circulating current increases the conduction loss, but the zero-voltage switching conditions still exist under light power operation since the current first harmonic lags the voltage in the transformer. Another disadvantage in operating the converter under these conditions is that the resonant voltage peak increases since, during a half switching cycle, its average value is identical to the input voltage source. This is illustrated in Figure 3-3, where the voltage peak increases for frequencies smaller than the resonant frequency.

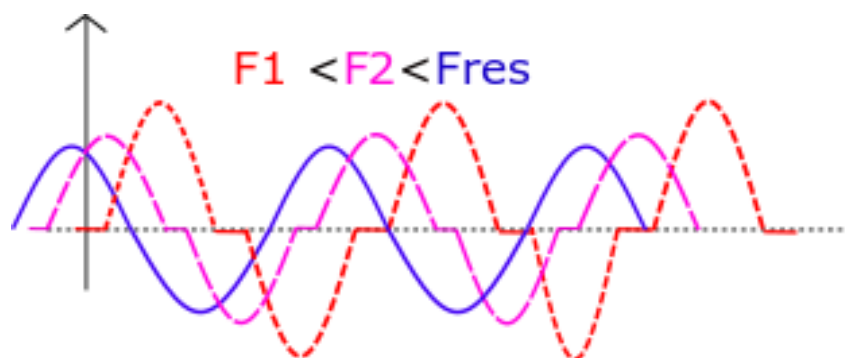


Figure 3-3: Resonant voltage in the parallel tank circuit for frequencies smaller or equal to the resonant frequency.

If the switching frequency is superior to the resonant frequency, the capacitor impedance becomes smaller. Thus, the converter's characteristic becomes predominantly capacitive, and the minimum

conditions to ensure zero-voltage switching no longer exist: the current first harmonic is no longer lagging the voltage.

Under soft-switching conditions, if we switch the three full-bridges at the same frequency and at the same time, the voltage source V_1 in Figure 3-2 imposes the voltage over the loads V_2 and V_3 . As the averaged voltage under the DC side inductors is zero, the redressed voltage at the output of each full-bridge have the same average value of the voltage source V_1 because of the converter unit gain [2], [3] and [4], except by the voltage drop over the transistors and the parasitic elements present in the circuit. Therefore, the transformer is the only element allowing the different voltage levels between the three voltage sources, V_1 , V_2 and V_3 .

In the next sub-section, we present the converter analysis in order to choose the best control strategy. Considering that the DC side inductors are large enough and that the transistor pairs of the three full-bridges are simultaneously switched, we can represent the Three-port converter in Figure 3-2 by an equivalent circuit containing three different square current sources.

The circuit in Figure 3-4 remains valid if the transformer has the characteristics close to the ideal case: a large magnetizing inductance compared to the resonant parallel inductances and very small leakage energy. The capacitors and inductors on the third and second sides are then remained to the primary side, as the current sources i_3 and i_2 . The full-bridges were replaced by three square current sources, where their signal indicates which bridge is sinking and which bridge is sourcing the power.

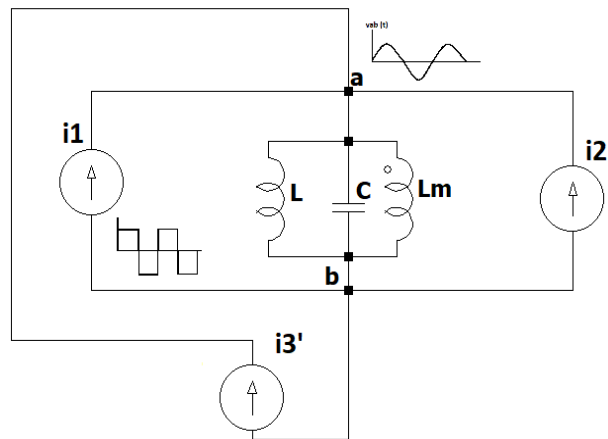


Figure 3-4: The equivalent circuit considering large input inductances, L_{S1} , L_{S2} and L_{S3} , and a large magnetizing inductance L_m . $1/L = (1/L_1 + 1/L_2 + 1/L_3)$ and $C = C_1 + C_2 + C_3$.

The first current harmonic oscillates between the parallel capacitor and the parallel inductor. This oscillation generates the sinusoidal voltage over the equivalent resonant parallel element that passes naturally by zero, allowing the zero voltage switching of the transistors. We present another equivalent circuit in Figure 3-5 to include also the role of the DC side inductors.

$$\frac{1}{L} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} \quad (1)$$

$$C = C_1 + C_2' + C_3' \quad (2)$$

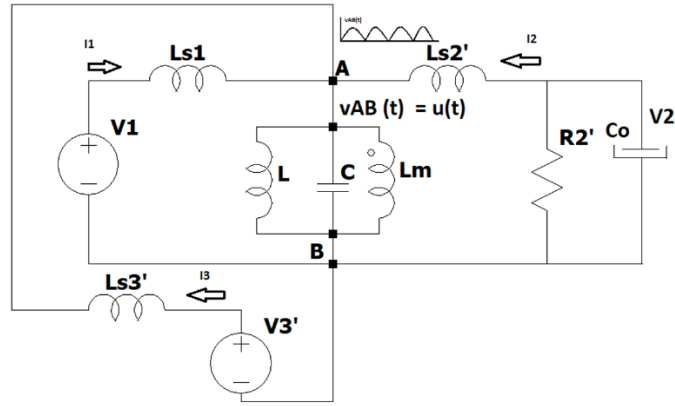


Figure 3-5: The equivalent circuit for the analysis considering the input inductors. $1/L = (1/L_1 + 1/L_2 + 1/L_3)$ and $C = C_1 + C_2 + C_3$.

In this representation, the current sources are now replaced by the series voltage power supply or the load connected in series with the DC side inductor. We replace the terminals “a” and “b” with negative and positive values by the equivalent redressed voltage between points “A” and “B”. The circuit is valid during a half-switching cycle only. An equivalent load can be also represented in any of the three ports because of the bidirectional power flow allowed by the symmetrical architecture. In the schematic of Figure 3-5, the MOSFETs are also considered to contain small on-resistance with a very small voltage drop. The total current flowing to the point “A” can be written as:

$$i_{ab} = i_1 + i_3 + i_2 = i_C + i_L + i_{Lm} \quad (3)$$

$$i_{Lm} = i_{T1} + i_{T2} + i_{T3} \cong 0 \text{ if } L_m \rightarrow \infty \quad (4)$$

The sum of the currents flowing into the transformer windings (i_{T1} , i_{T2} and i_{T3}) is considered equal to zero, as written in (4). The voltage drop on the series inductances is calculated as a function of the three current sources on the DC sides.

$$V_1 = L_{S1} \frac{di_1}{dt} + u; \quad V_3' = L_{S3} \frac{di_3}{dt} + u; \quad V_2' = L_{S2} \frac{di_2}{dt} + u \quad (5)$$

Combining the equations (3), (4) and (5), we obtain:

$$C \frac{du^2}{dt^2} + \frac{u}{L} + u \left(\frac{1}{L_{S1}} + \frac{1}{L_{S2}} + \frac{1}{L_{S3}} \right) - \left(\frac{V_1}{L_{S1}} + \frac{V_2}{L_{S2}} + \frac{V_3}{L_{S3}} \right) = 0 \quad (6)$$

The above differential equation can be simplified:

$$\frac{C L L_S}{(L_S+L)} \frac{du^2}{dt^2} + u = \left(\frac{V_1}{L_{S1}} + \frac{V_2}{L_{S2}} + \frac{V_3}{L_{S3}} \right) \frac{L L_S}{L_S+L} \quad (7)$$

$$\frac{1}{L_S} = \frac{1}{L_{S1}} + \frac{1}{L_{S2}} + \frac{1}{L_{S3}} \quad (8)$$

The general solution is:

$$u(t) = A_1 \cos(W_r t) + A_2 \sin(W_r t) + K \quad (9)$$

$$W_r = \sqrt{\frac{L+L_S}{L_S L C}} \quad (10)$$

Where K depends on the voltage sources and on the inductor values:

$$K = \left(\frac{V_1}{L_{S1}} + \frac{V_2}{L_{S2}} + \frac{V_3}{L_{S3}} \right) \frac{L L_S}{(L_S+L)}$$

The current in the equivalent parallel capacitor and in the equivalent parallel inductor are derived from the voltage in (9):

$$i_C(t) = -C A_1 W_r \sin(W_r t) + C A_2 W_r \cos(W_r t) \quad (11)$$

$$i_L(t) = \frac{A_1}{L W_r} \sin(W_r t) - \frac{A_2}{L W_r} \cos(W_r t) + \frac{K}{L} t \quad (12)$$

The solution of the differential equation depends on the initial conditions: the power transistors are switched during the zero voltage crossing, while the current still keeps its same signal just before the transition, so the current in the parallel inductor achieves its maximum value when the voltage $u(t)$ passes at zero and the equivalent capacitor is completely discharged.

$$u(0) = 0 \rightarrow A_1 = -K$$

$$i_L(0) = -I_{L_{Peak}} \rightarrow A_2 = L W_r I_{L_{Peak}}$$

$$u(t) = I_{L_{Peak}} L W_r \sin(W_r t) + K [1 - \cos W_r t] \quad (13)$$

$$i_L(t) = -\frac{K}{L W_r} \sin(W_r t) - I_{L_{Peak}} \cos(W_r t) + \frac{K}{L} t \quad (14)$$

$$i_C(t) = C K W_r \sin(W_r t) + I_{L_{Peak}} C L W_r^2 \cos(W_r t) \quad (15)$$

$$W_r = \sqrt{\frac{L+L_S}{L_S L C}} \text{ and } K = \left(\frac{V_1}{L_{S1}} + \frac{V_2}{L_{S2}} + \frac{V_3}{L_{S3}} \right) \frac{L L_S}{(L_S+L)} \quad (16)$$

Note that the resonant frequency only becomes dependent on the parallel resonant elements if the DC side equivalent inductance is much larger than the equivalent parallel inductance:

$$W_r = \sqrt{\frac{1}{LC}}, \text{ if } L_s \gg L \quad (17)$$

The DC side currents can be obtained by calculating the instantaneous voltage drop over the inductors:

$$v_{L_{S1}} = V_1 - u(t) = L_{S1} \frac{di_1}{dt} \rightarrow V_{peak} = \frac{\pi(V_1+K)}{2} \quad (18)$$

$$i_1(t) = \frac{K}{W_r L_{S1}} \sin(W_r t) + \frac{I_{L_{Peak}} L}{L_{S1}} \cos(W_r t) + \frac{(V_1-K)}{L_{S1}} t \quad (19)$$

During the steady state, the maximum voltage on the transformer terminals and therefore the voltage also applied on the power transistors during their turning-off can be calculated by using the average value over the DC side inductor equal to zero:

$$\frac{1}{\pi} \int_0^\pi u(t) d\omega t = V_1 \rightarrow \frac{1}{\pi} \int_0^\pi [K + (I_{L_{Peak}} L W_r) \sin W_r t - K \cos W_r t] d\omega t = V_1 \quad (20)$$

From this result, we see that the voltage peak over the power switches and the transformer also depends on the ratio between the DC side inductors L_s and the parallel resonant inductors L_p . Higher this ratio is, smaller will be the voltage peak. Indeed if the DC side inductor L_s has a reduced value if compared to the resonant inductor L_p , the equivalent resonant frequency is also dependent on its value as in (16), and the relation in (17) is no longer valid. In Figure 3-6, when the ratio L_s/L_p is reduced, the equivalent resonant voltage peak increases, and it is displaced to the left side.

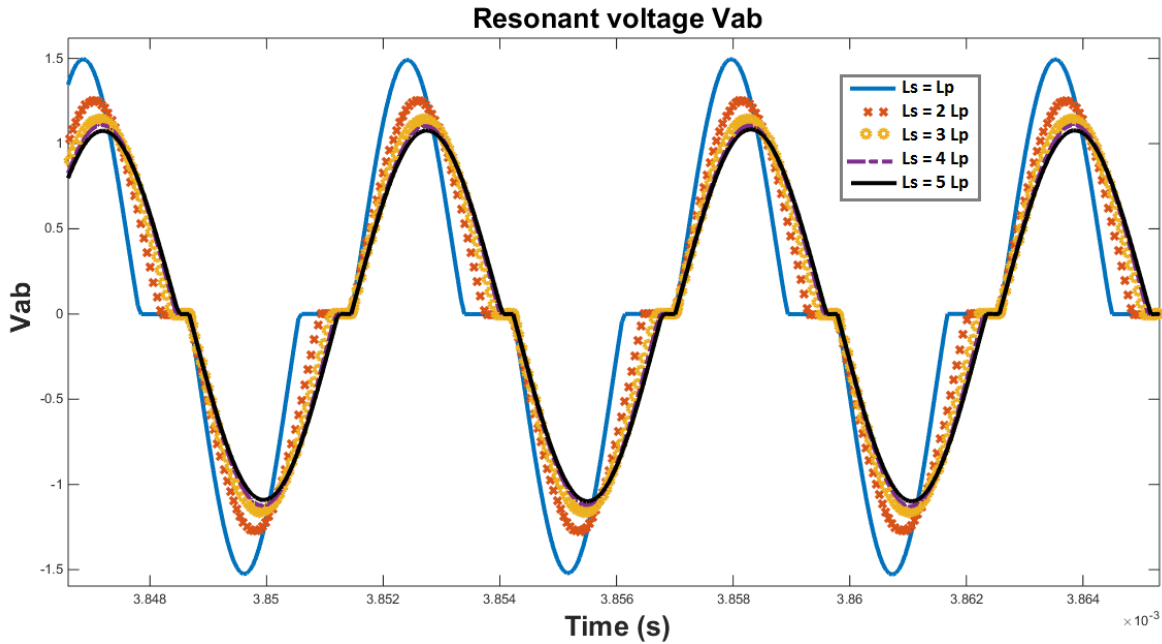


Figure 3-6: The resonant voltage for different DC side inductances L_s . The effective resonant frequency is modified by L_s when this one is not much larger than the parallel inductance L_p .

The average current on the DC side can be obtained by:

$$I_1 = \frac{2}{\pi} \int_0^\pi i_1 d \omega t = \frac{2}{\pi} \int_0^\pi \frac{K}{W_r L_{S1}} \sin(W_r t) + \frac{I_{L_{Peak}} L}{L_{S1}} \cos(W_r t) + \frac{(V_1 - K)}{L_{S1}} t d \omega t$$

$$I_1 = \frac{2}{\pi W_r L_{S1}} \left[2K + \frac{\pi^2 (V_1 - K)}{2} \right] \quad (21)$$

In the converter study, the steady-state analysis shows the converter operating at the resonant frequency. However, as explained before, when the frequency is smaller than the resonant frequency, zero-voltage switching still occurs because the current lags the voltage allowing the complete discharge of the equivalent capacitance. At the resonant frequency, the first current harmonic and the capacitor voltage are in phase; the transition time required to charge and discharge the equivalent capacitor is minimized.

The following figures illustrate a single full-bridge operation with a smaller switching frequency, but close to the resonant frequency. The transformer, represented by an infinite magnetizing inductance, is omitted in Figure 3-7, but i_{T1} represents the current passing from its primary side to the secondary in Figure 3-8. Let us consider first that the power transistors S1 and S4 are in ON state, during the interval t_1 . The DC side inductor L_{S1} establishes an almost constant current, transmitted to the load by the transformer. The circulating energy starts to oscillate between L_1 and C_1 . At the end of this interval, the voltage V_{ab} naturally crosses zero. At this moment, the current on the inductor L_1 achieves its maximum and remains constant during the transition. C_1 , C_{S2} , and C_{S3} are completely discharged and the transistors S2 and S3 can be turned-on under ZVS, during the interval t_2 . The four transistors are now conducting and the current is equally distributed between the two primary arms at the beginning until it passes by zero. After the conduction overlap time when the four transistors were in active mode, the transistors S1 and S4 are turned off. During the time interval t_3 , the power transistors S2 and S3 are conducting and the resonant current oscillates between L_1 and C_1 , such as in the positive half-cycle. Again, during the time interval t_4 , when the voltage naturally passes by zero, the transistors S1 and S4 are turned-on under ZVS also. These modes are repeated in the next period. Note that, during the overlap conduction time, the current i_{T1} is zero, meaning that there is no energy transfer between the transformer terminals. Consequently, the smaller is the switching frequency, higher will be the power losses during the transition because of the circulating energy. The regulation of the average output voltage or current is not possible by using the frequency, leading to hard-switching conditions. The best condition to operate this converter is at its resonant frequency. In the next section, we study the role of the DC side inductors in order to find a better configuration and reduce their size.

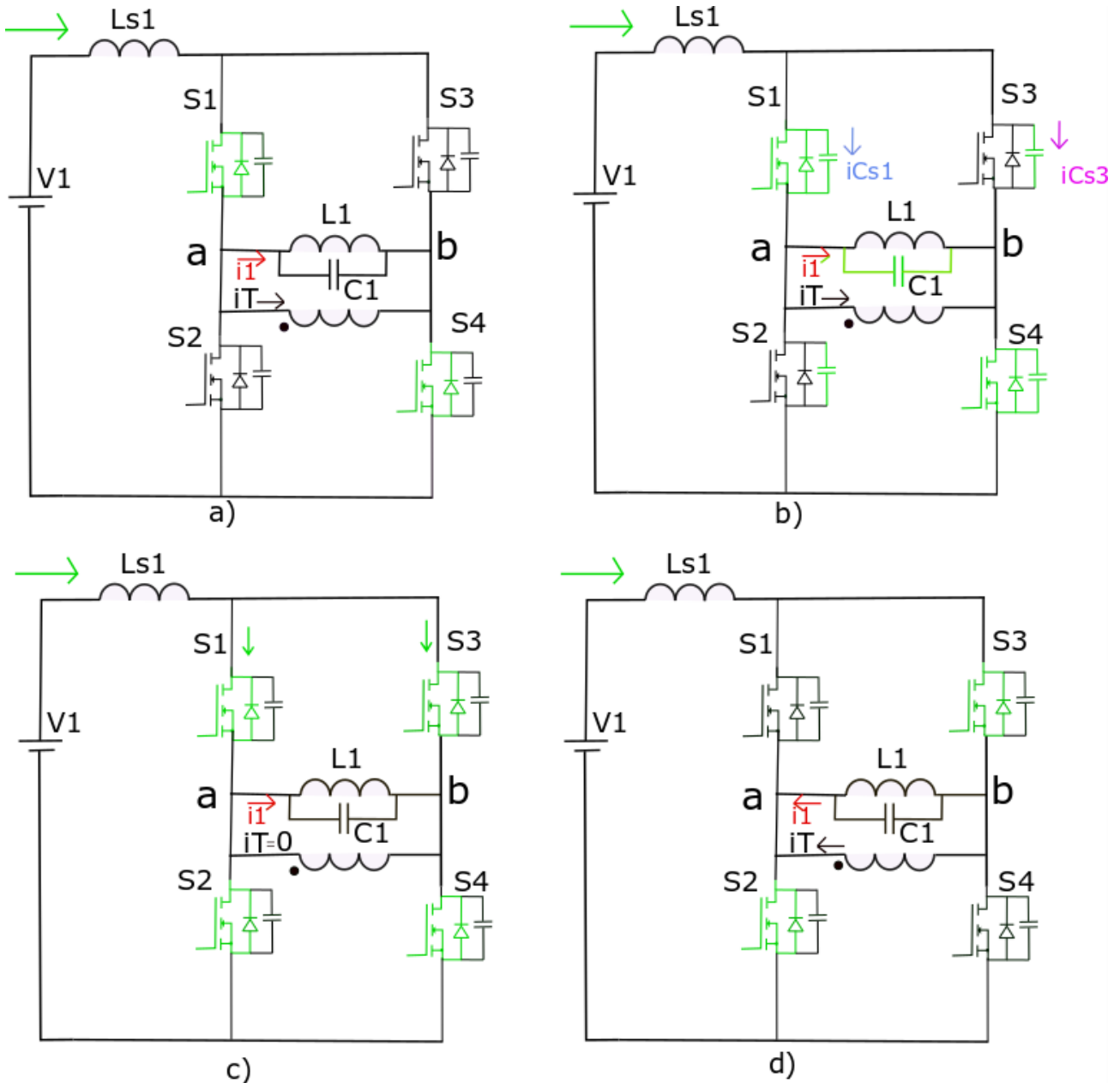


Figure 3-7: The converter operation modes illustrated during a half-cycle in a single full-bridge. a) $S1$ and $S4$ are ON and V_{ab} is on the positive half-cycle, corresponding to interval t_1 in Figure 3-8. b) The capacitors C_{S2}, C_{S3} and C_1 are being charged and discharged while the remained energy goes back to V_1 . It corresponds to the transition between intervals t_1 and t_2 in Figure 3-8. c) While $V_{ab} = 0$, $S2$ and $S3$ are turned-on under ZVS, during the time interval t_2 in Figure 3-8. d) After the overlap time, $S1$ and $S4$ are turned-off under ZVS. C_{S1}, C_{S4} are progressively charged while V_{ab} increases.

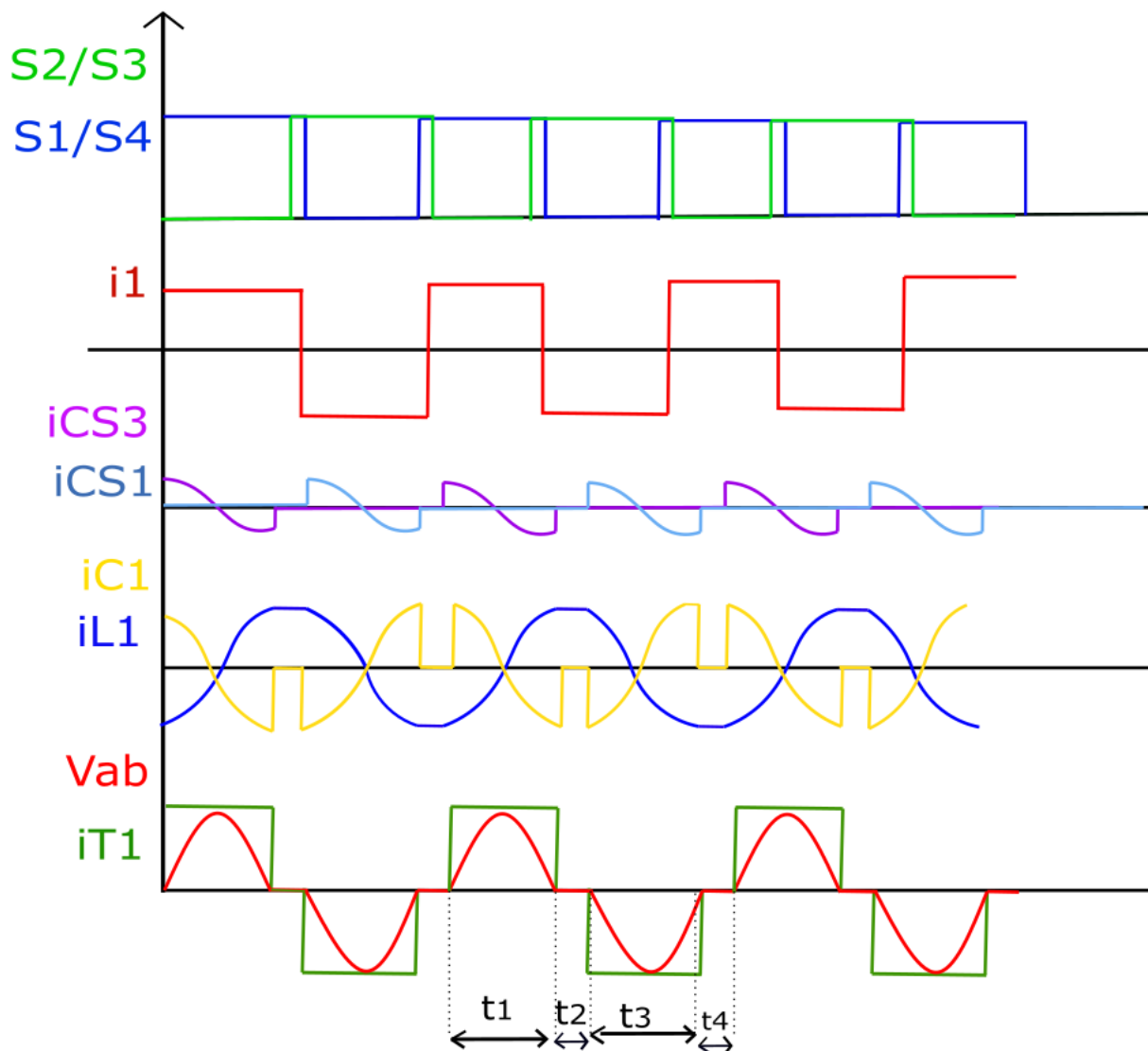


Figure 3-8: The converter operation modes for a single full-bridge. The transistors switching commands, the current in the AC side i_1 , the current in the parasitic capacitances from transistors S1 and S3 (i_{CS3} and i_{CS1}), the resonant current in L_1 and C_1 , the transformer's voltage between terminals "a" and "b" and the transformer primary current i_{T1} .

3.3- The DC side inductors

One of the three-port current-fed resonant converter characteristics is the possibility of different arrangements with the DC side inductors. The average current mainly determines the DC side inductor values in each port, and we can see from Eq. (16), (18) that it plays an important role in the resonant voltage peak. Generally, for current-fed resonant converters analysis, the DC side inductance is considered large enough to smooth and keep an almost constant current on the DC side. This was the case in the first analysis approach, where in order to simplify the equivalent circuit in Figure 3-3, we had considered square current sources in the transformer. In Figure 3-4, however, we also introduce the DC side inductors. We can see from the equations derived in the previous section that their values influence on the resonant frequency and in the resonant voltage peak.

The voltage peak is a critical parameter for the power transistors selection. It has a direct influence on the conduction power losses. The higher the nominal voltage of the transistor is, the higher will be its active resistance. Therefore, it becomes interesting to propose some solutions to minimize the resonant voltage peak. One of the solutions concern the control strategy and consists of keeping the converter operation the close as possible of the resonant frequency. Another possibility is the design of large DC side inductors to minimize this voltage. In this section, we investigate the possibility of coupling the three DC side inductors in the same magnetic core.

The use of a single magnetic core to design the three DC side inductors could bring some advantages to the configuration, especially in the case where the DC side inductances could be smaller than the parallel ones. The first and obvious advantage is the reduction of the total number of magnetic elements and their total volume. Besides, the reduction of the voltage peak without needing to increase the DC inductor values.

We consider here, three different coupling factors using the same magnetic core:

$$k_{12} = \frac{L_{S1(1-2)}}{\sqrt{L_{S1}L_{S2}}}, \quad k_{13} = \frac{L_{S1(1-3)}}{\sqrt{L_{S1}L_{S3}}}, \quad k_{23} = \frac{L_{S2(2-3)}}{\sqrt{L_{S2}L_{S3}}} \quad (22)$$

The coefficients are symmetric because of the reciprocity theorem, and the voltage drop over the DC side inductances remained to the primary side during a half-switching cycle are:

$$V_1 - u = L_{S1} \frac{di_1}{dt} + L_{S1(1-2)} \frac{di_2'}{dt} + L_{S1(1-3)} \frac{di_3'}{dt}$$

$$V_2' - u = L_{S2}' \frac{di_2'}{dt} + L_{S1(1-2)} \frac{di_1}{dt} + L_{S2(2-3)} \frac{di_3'}{dt}$$

$$V_3' - u = L_{S3}' \frac{di_3'}{dt} + L_{S1(1-3)} \frac{di_1}{dt} + L_{S2(2-3)} \frac{di_2'}{dt}$$

In the above equations, the voltage sources, the inductances on the secondary and third sides were remained to the primary side. The sum of the three above equations results in:

$$V_1 + V_2' + V_3' - 3u = \frac{di_1}{dt} (L_{S1} + L_{S1(1-2)} + L_{S1(1-3)}) + \frac{di_2'}{dt} (L_{S2}' + L_{S1(1-2)} + L_{S2(2-3)}) + \frac{di_3'}{dt} (L_{S3}' + L_{S1(1-3)} + L_{S2(2-3)}) \quad (23)$$

As the objective of this converter is to allow reverse power flow between the ports and because of the converter symmetry, it is coherent to propose the design of DC side inductors with the same self-value when remained to the same side and with the same coupling factor between the windings. Therefore, we consider the following simplification.

$$V_1 + V_2' + V_3' - 3u = \frac{di_1}{dt} L_{S_1} (1 + k_{12} + k_{13}) + \frac{di_2'}{dt} L_{S_2}' (1 + k_{12} + k_{23}) + \frac{di_3'}{dt} L_{S_3}' (1 + k_{13} + k_{23})$$

$$V_1 + V_2' + V_3' - 3u = L_{S_1} (1 + k_{12} + k_{13}) \left(\frac{di_1}{dt} + \frac{di_2'}{dt} + \frac{di_3'}{dt} \right)$$

$$V_1 + V_2' + V_3' - 3u = L_{S_1} (1 + k_{12} + k_{13}) \left(\frac{di_C}{dt} + \frac{di_L}{dt} + \frac{di_{Lm}}{dt} \right)$$

$$V_1 + V_2' + V_3' - 3u = L_{S_1} (1 + k_{12} + k_{13}) \left(C \frac{d^2u}{dt^2} + \frac{u}{L} \right), \text{ if } \frac{di_{Lm}}{dt} \cong 0 \quad (24)$$

$$\frac{C L L_{S_1} (1+k_{12}+k_{13})}{L_{S_1} (1+k_{12}+k_{13})+3L} \frac{d^2u}{dt^2} + u = \frac{(V_1+V_2'+V_3')L}{L_{S_1} (1+k_{12}+k_{13})+3L} \quad (25)$$

The same initial conditions used in the above section are still valid here. The solutions of the resonant voltage and frequency are:

$$u(t) = I_{L_{Peak}} L W_{r_2} \sin(W_{r_2} t) + K_2 [1 - \cos(W_{r_2} t)] \quad (26)$$

$$i_L(t) = -I_{L_{Peak}} \cos(W_{r_2} t) - \frac{K_2}{L W_{r_2}} \sin(W_{r_2} t) + \frac{K_2 t}{L} \quad (27)$$

$$W_{r_2} = \sqrt{\frac{3L+L_{S_1}(1+k_{12}+k_{13})}{L_{S_1}(1+k_{12}+k_{13})L C}} \quad (28)$$

$$K_2 = \frac{(V_1+V_2'+V_3')L}{[L_{S_1}(1+k_{12}+k_{13})+3L]} \quad (29)$$

The resonant frequency in (16) could be replaced by the equivalent LC parallel cell resonant frequency only if the DC side inductors were much higher than the equivalent parallel inductance. The same affirmation is confirmed in the case presented here when the three DC side inductors have a mutual coupling factor, Eq. (28). In fact, if the parallel inductance remains small compared with the DC side self-inductance, or if the mutual inductance remains much higher than the parallel inductance, then we have the same results, and the resonant frequency depends only on the parallel resonant elements. In this case, the voltage peak depends mainly on the ratio between the parallel equivalent and the DC side inductors (L/L_{S_1}). Otherwise, if the coupling factor increases, then the voltage peak depends on the ratio between the non-coupled and the parallel resonant inductances, $(L_{Self} + L_{Leak})/(L \times L_{S_1})$, thus decreasing the voltage peak.

However, if the use of the mutual coupling factors allows the design of smaller DC side inductances, then the resonant frequency depends on the mutual inductances.

When applied over one of the DC side inductances, the voltage-time balance allows us to calculate the resonant voltage peak again depending on the mutual coupling factors between the DC side inductances.

$$V_1 - u = L_{S_1} \frac{di_1}{dt} + k_{12} L_{S_2}' \frac{di_2'}{dt} + k_{13} L_{S_3}' \frac{di_3'}{dt} \quad (30)$$

$$\frac{1}{\pi} \int_0^\pi (V_1 - u) d\omega t = 0 \quad (31)$$

$$V_{peak} = \frac{\pi (V_1 + K_2)}{2} \quad (32)$$

$$V_{peak} = \frac{\pi V_1}{2} + \frac{\pi}{2} \frac{(V_1 + V_2' + V_3') L}{[L_{S_1} (1 + k_{12} + k_{13}) + 3L]} \quad (33)$$

The mutual inductance influences the resulting voltage peak. When this factor is small, the result becomes the same obtained before without the coupling proposition.

To illustrate the use of coupling inductors on the DC side, in the following figure, we present numerical values for a specific application considering a nominal voltage of 480 Vdc.

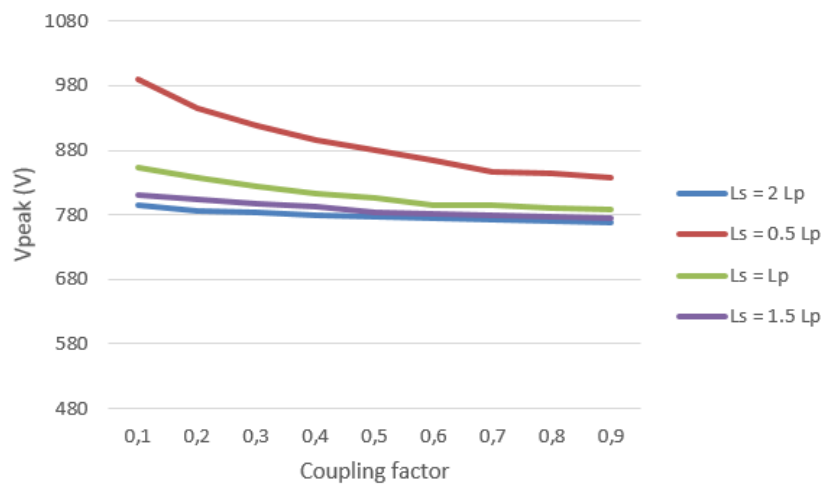


Figure 3-9: Resulting resonant voltage peak for different DC side inductance values (L_s) keeping the same parallel resonant inductance (L_p) and different coupling factors.

We notice that without the mutual coupling, the resulting voltage peak is only minimized if the DC side inductance is higher than the equivalent parallel inductance. It becomes necessary to design large inductances to smooth the current ripple and generates smaller voltage peaks.

On the other hand, by designing the three DC side inductances in the same magnetic core, the required volume becomes smaller without compromising the current ripple or the voltage peak applied to the transistors. These characteristics must be considered during the converter design.

3.4- The converter control strategy

Because of the absence of series elements connected on the AC side of the converter, by using the frequency variation is not possible to change the average output voltage neither the output current. Hence, it is interest to operate the converter as close as possible to the resonant frequency. However, because of the variation in the passive element values due to parasitic elements and aging of the electronic components during its lifetime, it is hard to know the exact value of the frequency. One of the solutions to this problem is the self-tracking of the frequency, idealized for the first time in the Mazzilli's converter [5], [6]. This strategy consists of pre-charging the converter and detecting the natural zero voltage crossing. At this moment, we switch the transistors and use the feedback of this measure to change again the transistor's state, thus leading the converter itself to find its natural resonant frequency. The main drawback of this strategy is that it can lead the converter to operate under instability conditions due, for example, to a load variation or a non-expected open-circuit condition. In [6], for a bidirectional current-fed based on a push-pull structure, a tertiary transformer winding is proposed to generate the gating signals to drive the transistors. The signal is combined with an external pulse generated by a controller to initialize the converter oscillation. The control strategy proposed for the bidirectional three-port converter presented in this thesis is likewise based on the combination of a forced switching signal, to prevent instability due to the load variation, and the detection of the voltage zero crossing allowing ZVS. The signal generation is presented in Figure 3-10. The signals Forced H and Forced L are at the same frequency, delayed from each other of 180° containing a small overlap between them to ensure the current continuity.

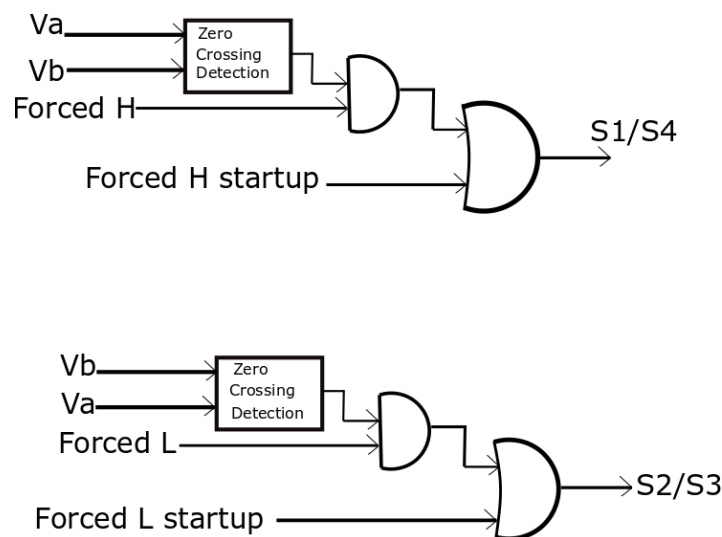


Figure 3-10: Command generation for the 3-port current-fed parallel resonant converter. Combination between a forced switching signal (Pulse H and L) and the voltage zero crossing detection (from V_{ab}).

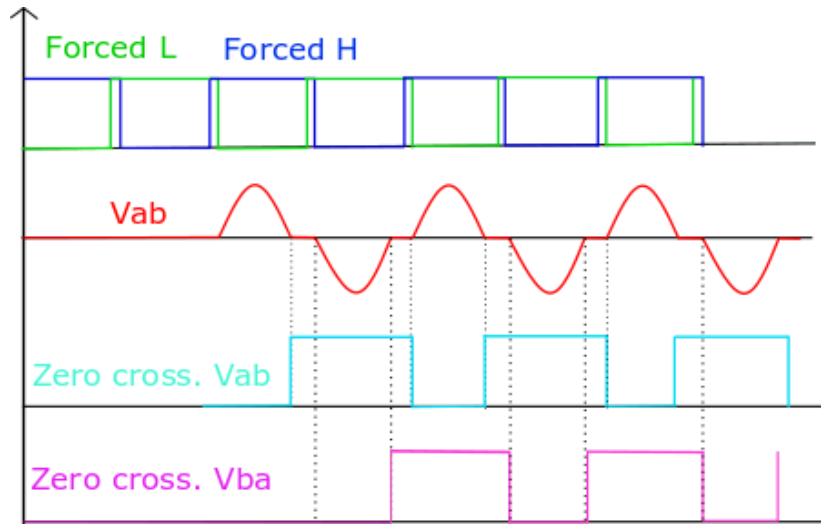


Figure 3-11: The forced switching signals at constant frequency and zero voltage crossing detection.

The signals driving the transistors S1, S2, S3, and S4 are the same used to drive the transistors in the other two ports. If the transformer characteristics are close to an ideal transformer, small leakage inductance and large magnetizing inductance, the voltage zero-crossing detection can be obtained in any one of the three transformer windings.

If the voltage in one of the ports is regulated with the use of the phase-shift strategy between the ports or between the two arms in the same port, then the soft-switching capability no more exists for at least two transistors in a single full-bridge.

To illustrate the converter operation modes, a numerical application is presented below using coupled DC side inductors. The coupling between the three DC side inductors reduces the voltage peak, even using a smaller inductance value.

	Port 1	Port 2	Port 3
Nom. Voltage (V)	480	480	20
Transformer N	24	24	1
DC side inductance	42 μ H	42 μ H	73 nH
Parallel inductance	165 μ H	165 μ H	290nH
Parallel capacitance	4 nF	4 nF	2.3 μ F

Table 3-1: Converter design specification.

In Figure 3-12-a) and b), we observe the current in the third and secondary sides of the converter, respectively. In Figure 3-12-c), the current in the transformer primary side, after the resonating cell connected to the resonant voltage V_{ab} . The current spike occurs during the switching and only on the primary and secondary sides because of parasitic elements connected in series with the current loop. The converter is controlled the close as possible of the resonant frequency, at 200 kHz, and the first voltage source V1 charges the second and third sides of the converter, V2 and V3 with a maximum power of 7 kW.

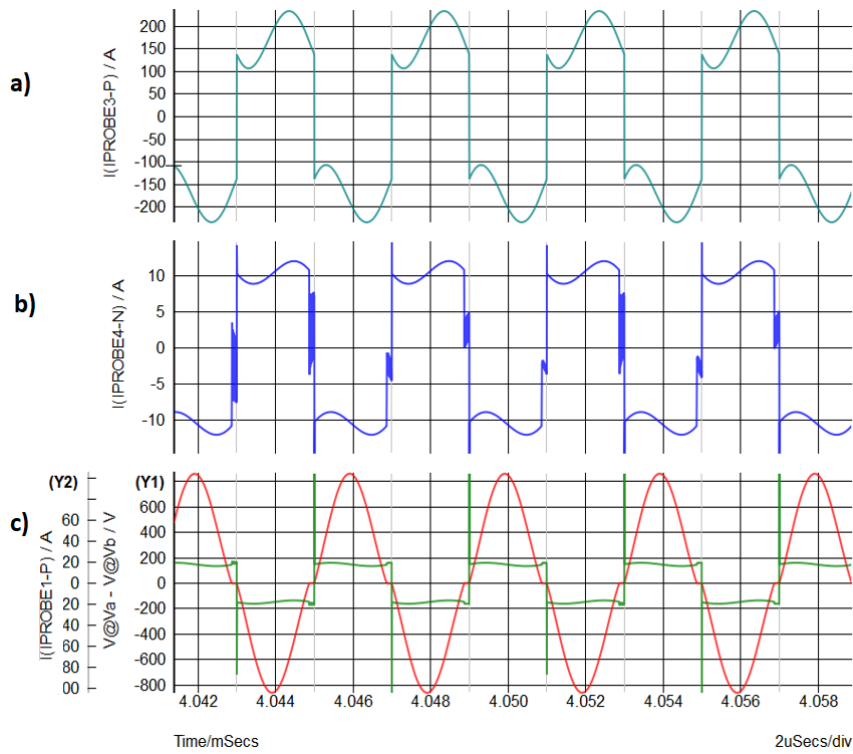


Figure 3-12: Converter operation while Port 1 supplies 7 kW for ports 2 and 3 (OBC+LDC simultaneous operation): a) Current in the third side, i_3 . b) Current in the secondary side, i_2 c) Current in the primary transformer side, i_{T1} (square waveform) and voltage V_{ab} (sinusoidal waveform).

In Figure 3-13 the current in the primary, secondary and third sides of the transformer are presented for the same operating conditions. The resonant voltage at the transformer terminals V_{ab} , V_{cd} and V_{ef} are almost identical because of the converter operation with unit voltage gain.

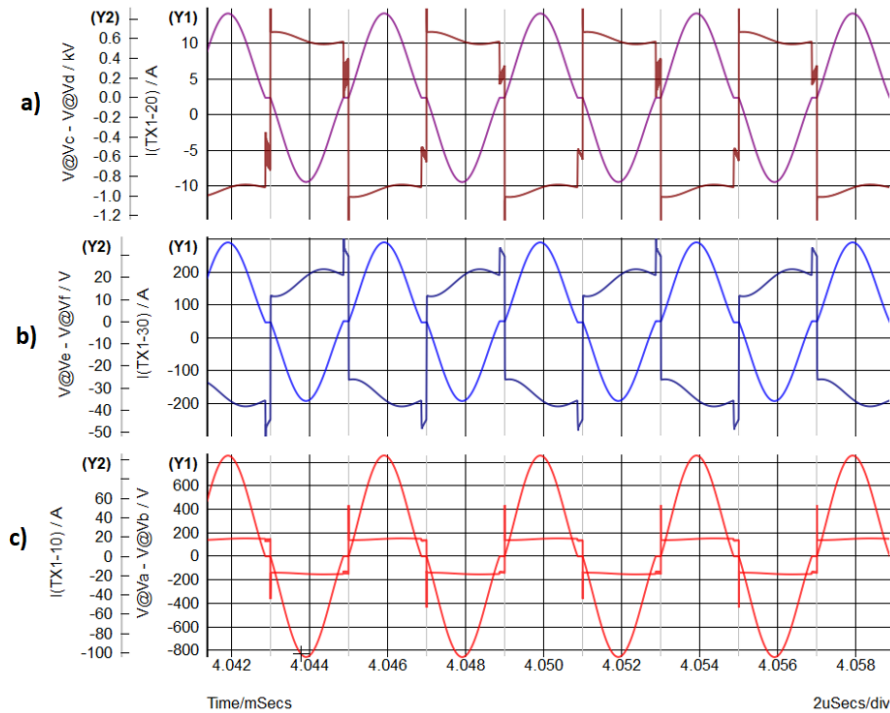


Figure 3-13: Converter operation while Port 1 supplies 7kW for ports 2 and 3 (OBC +LDC simultaneous operation): a) Current in the transformer secondary side, i_{T2} and voltage V_{cd} . b) Current in the transformer third side, i_{T3} and voltage V_{ef} . c) Current in the primary side, i_{T1} and voltage V_{ab} .

In Figure 3-14, under the same operating conditions, the input current coming from the voltage source V1 and the output current on the secondary and third ports are represented. Despite the reduced DC side inductor value, the current ripple is limited to a small range.

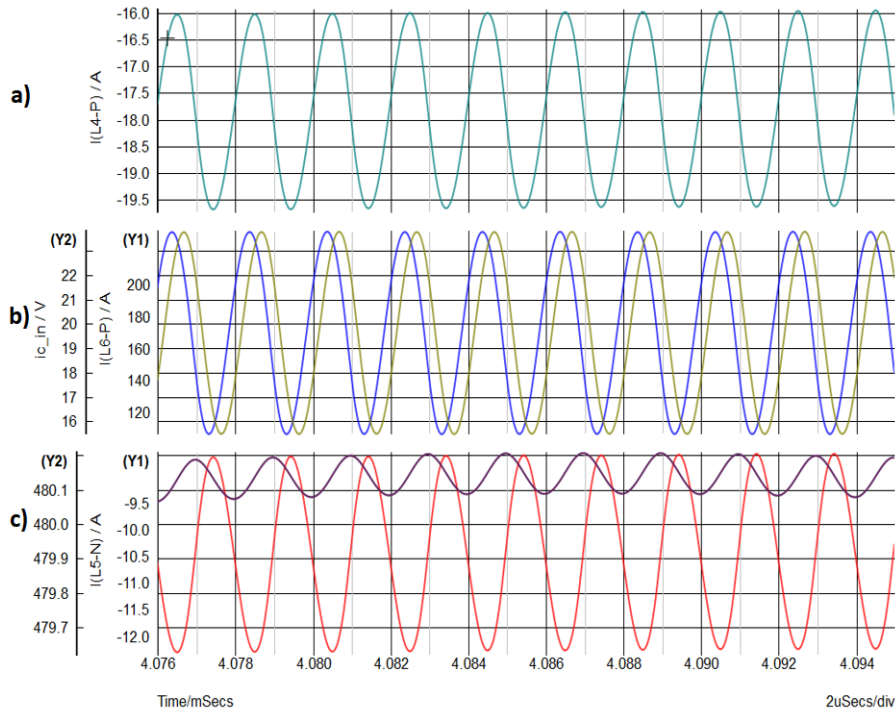


Figure 3-14: Converter operation while Port 1 supplies 7 kW for ports 2 and 3 (OBC+LDC simultaneous operation: a) DC current i_{LS1} . b) DC current i_{LS3} and output voltage V_3 . c) DC current i_{LS2} and output voltage V_2 .

Currently, the analysis had been considered during steady-state. During the converter's initialization, however, the initial conditions do not allow the immediate ZVS for this current-fed topology. These conditions are studied in the next section.

3.5- The startup of the Three-port current-fed bidirectional converter

In the present converter containing the three different voltage sources, V_1 , V_2 , and V_3 , during steady-state, ZVS exists by controlling the converter with a fixed switching frequency slightly smaller than the resonant frequency, or by using an auto self-oscillation circuit associated with the zero voltage crossing detection. However, in neither case, ZVS cannot be ensured during the transient state. In this section, the conditions for achieving ZVS during the transient state are presented for the bidirectional converter. In addition, we study a strategy without extra cost to prevent voltage overshoot during the transient state.

3.5.1- ZVS analysis during startup

In one of the control techniques, the converter operates at its natural oscillation by tracking the frequency, when the controller detects the zero voltage crossing to switch the transistors. In this solution, the converter is operated exactly at the resonant frequency and the commutation interval corresponds to the required time to charge and discharge the equivalent capacitors without adding extra conduction power losses. Another way of obtaining the ZVS, is by applying a fixed switching frequency, smaller than the resonant frequency but as close as possible of this frequency to reduce power losses. An overlap time is added to ensure the current path during the switching. In both cases, the ZVS is obtained only during steady-state, but it can lead to hard switching during the transient state.

The study in this section focuses on the transient time when no DC current has yet been established. Consequently, the resonant elements are completely discharged and no initial voltage is applied to the parallel capacitance, $v_C(0) = 0$, neither an initial current on the parallel resonant inductor, $i_L(0) = 0$. At instant $t = 0$, we consider the beginning of the three full-bridges switching in two different scenarios. The first one is presented in Figure 3-15. The voltage source V_1 is completely charged, but the voltage sources associated with V_{o2} and V_{o3} are discharged. This scenario means the converter is connected to the electrical grid, but the HV and LV sides, V_{o2} and V_{o3} , respectively, need to be pre-charged. At the instant $t = 0$, when the command is applied, the current on the DC side inductance L_{s1} starts to increase linearly. In Figure 3-15-b), we had remained the elements from the secondary and third sides to the primary side of the transformer considering an infinite magnetizing inductance.

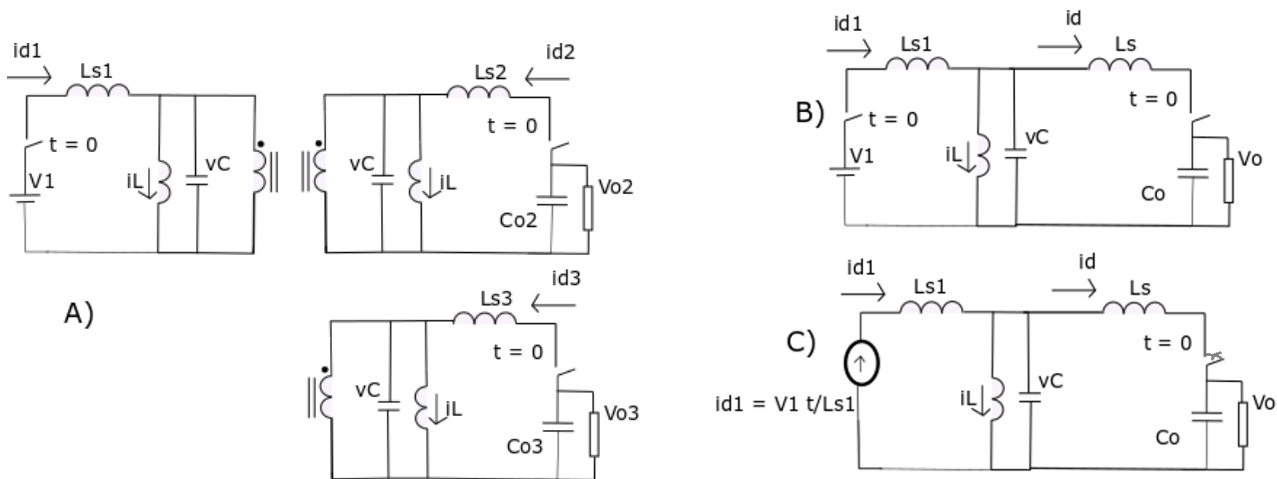


Figure 3-15: a) Equivalent circuit during the startup of the converter, when the two sources, HV and LV are completely discharged and connected to V_{o2} and V_{o3} , respectively. b) The simplified circuit with a single resonant cell and an equivalent load. c) Simplified circuit with a current-step representation.

The voltage source connected in series to the DC side inductance and the switch at $t=0$ can be replaced by a current source, as in Figure 3-15-c. The switch connected in series to the load is also closed at $t=0$. The state-space equation of the simplified circuit is:

$$\frac{d}{dt} \begin{bmatrix} i_{d_1} \\ i_d \\ i_L \\ v_C \\ v_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -1/L_{S_1} & 0 \\ 0 & 0 & 0 & 1/L_S & -1/L_S \\ 0 & 0 & 0 & 1/L & 0 \\ 1/C & -1/C & -1/C & 0 & 0 \\ 0 & 1/C_o & 0 & 0 & 1/R_o \end{bmatrix} \begin{bmatrix} i_{d_1} \\ i_d \\ i_L \\ v_C \\ v_o \end{bmatrix} + \begin{bmatrix} 1/L_{S_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_1 \quad (34)$$

$$\frac{d(i_{d_1})}{dt} = -\frac{v_C}{L_{S_1}} + \frac{V_1}{L_{S_1}}; \quad \frac{d(i_d)}{dt} = \frac{v_C}{L_S} - \frac{v_o}{L_S}; \quad \frac{d(i_L)}{dt} = \frac{v_C}{L}$$

$$\frac{d(v_C)}{dt} = \frac{i_{d_1}}{C} - \frac{i_d}{C} - \frac{i_L}{C} \quad \frac{d(v_o)}{dt} = \frac{i_d}{C_o} + \frac{v_o}{R_o}$$

The solution for the resonant voltage is derived from the equation below:

$$\frac{d^2(v_C)}{dt^2} = \frac{1}{C} \frac{d(i_{d_1})}{dt} - \frac{1}{C} \frac{d(i_d)}{dt} - \frac{1}{C} \frac{d(i_L)}{dt} \quad (35)$$

Considering the dynamic of the output and the resonant voltages, v_o and v_C , the first one can be disregarded during the increasing of the output current i_d . This assumption is justified because of the difference between the output and resonant capacitances C_o and C since the first one is larger.

The differential equation as well the solution are shown below:

$$\frac{d^2(v_C)}{dt^2} + \frac{v_C}{C} \left[\frac{L L_S + L_{S_1} L_S + L_{S_1} L}{L_{S_1} L_S L} \right] = \frac{V_1}{C L_{S_1}} \quad (36)$$

$$v_C(t) = -\frac{V_1}{C L_{S_1}} \cos(\omega_o t) + \frac{V_1}{C L_{S_1}}, \quad \omega_o = \sqrt{\frac{L L_S + L_{S_1} L_S + L_{S_1} L}{C L_{S_1} L L_S}} \quad (37)$$

The solution is given by the equivalent circuit in Figure 3-15-c) and shows that the converter starts to oscillate without any additional difficulty. The equivalent inductance gives the oscillation frequency as presented in Eq. (37).

The second scenario considers that the HV and LV sides are pre-charged from the beginning. In fact, considering additional non-isolated bidirectional DCDC converters connected in cascade with the HV and LV batteries, the pre-charge can be aimed. In this scenario, considering that the unit voltage gain concept is still valid, the three voltage sources connected in series with the DC side inductances are equivalents. Thus, the equivalent circuit can be represented by a single circuit where all the elements are on the primary side. During the initialization, we can hence consider the three full-bridges, independent from each other, as proposed in Figure 3-16. If the magnetizing inductance is large compared to the parallel resonant inductance, a parallel resistance can represent the transformer's equivalent resistance, damping the oscillations during the start-up. The resistance can also represent a damping circuit added due to the parasitic oscillations, as it will be discussed in Chapter 5.

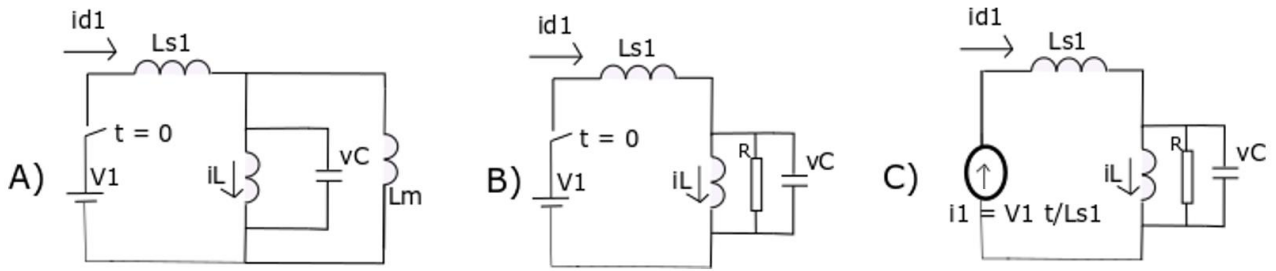


Figure 3-16: a) Equivalent circuit of a single full-bridge b) Equivalent circuit considering $L_m \rightarrow \infty$ and a parallel resistance connected in parallel to make opposition to the natural oscillation. c) Equivalent circuit represented with a current step.

The circuit is only valid during the transient of the converter operation, considering that the passive elements are initially discharged, and that the total power flow is equal to zero. In the ideal case, the resistance is infinite, and no damping factor exists. This is also important in order to obtain a sinusoidal voltage in the equivalent circuit. If the current absorbed by the load increases, the voltage between the transformer terminals is no longer sinusoidal, and no oscillation can be detected.

As it was made in the circuit from Figure 3-15, the voltage source connected in series to the switch at $t=0$, in Figure 3-16-c, can be replaced by a current source during the initial phase.

The state-space equations can be written as:

$$\frac{d}{dt} \begin{bmatrix} id_1 \\ iL \\ vC \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1/L_{s1} \\ 0 & 0 & 1/L \\ 1/C & -1/C & -1/RC \end{bmatrix} \begin{bmatrix} id_1 \\ iL \\ vC \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{s1}} \\ 0 \\ 0 \end{bmatrix} V_1 \quad (38)$$

Considering the step of a current source as represented in Figure 3-16-c, the following differential equation can be solved to describe the voltage over the capacitor:

$$LC \frac{d^2 v_C}{dt^2} + \frac{L}{R} \frac{d v_C}{dt} + \frac{v_C(L+L_{s1})}{L_{s1}} = \frac{L V_1}{L_{s1}} \quad (39)$$

The complete solution of the differential equation considering the initial voltage and the current equals to zero, $v_c=0$ $dv_c/dt=0$, is:

$$v_c(t) = - e^{\frac{-t}{2RC}} \frac{L V_1}{L_{s1} \sin(\phi)} \sin(bt + \phi) + \frac{L V_1}{L_{s1}} \quad (40)$$

$$\phi = \text{artg} \left(\sqrt{1 - \frac{4 R^2 C (L+L_{s1})}{L_{s1} L}} \right) \quad (41)$$

$$b = \frac{1}{2RC} \sqrt{1 - \frac{4 R^2 C (L+L_{s1})}{L_{s1} L}} \quad (42)$$

The voltage v_C is never negative, not even at $t = 0$, when $\sin(\phi)$ is close to one, neither under the ideal condition when the load is infinite. When $t \neq 0$ and ϕ is very small, the first parcel tends to infinite. The minimum value of $v_C(t)$ occurs at:

$$\frac{dv_C}{dt} = -\frac{1}{2RC} e^{-\frac{t_{min}}{2RC}} K \sin(b t_{min} + \phi) + e^{-\frac{t_{min}}{2RC}} K b \cos(b t_{min} + \phi) = 0$$

$$t_{min} = \frac{(\text{artg}(2RC b) - \phi)}{b} = 0, \quad v_{C_{min}} = 0 \quad (43)$$

In the equivalent load connected in parallel to the resonant inductor and capacitor, the voltage under self-detection oscillation is never negative, consequently no natural oscillation occurs and ZVS is not possible during the startup.

3.5.2- Obtaining the condition for ZVS

To obtain the self-oscillation in the converter under the second situation, the idea is to change the initial condition. In the beginning, a short-circuit time could be used to pre-charge the parallel capacitors or obtain an initial current in the DC side inductor. This condition allows an initial oscillation between the passive elements in the converter circuit. Initially, the parasitic capacitors in parallel with the transistors oscillate with the DC side inductor, as presented in Figure 3-17-b):

$$\frac{d^2 v_{C_{ds}}}{dt^2} + \frac{v_{C_{ds}}}{C_{ds} L_s} = \frac{V_1}{C_{ds} L_s} \quad (44)$$

$$v_{C_{ds}}(t) = A_1 \sin\left(\sqrt{\frac{1}{C_{ds} L_s}} t\right) + A_2 \cos\left(\sqrt{\frac{1}{C_{ds} L_s}} t\right) \quad (45)$$

The short-circuit time can be applied to initiate the natural oscillation in the converter. The same idea was applied in a single-phase current-fed inverter in [12], allowing ZVS during the converter's transient state.

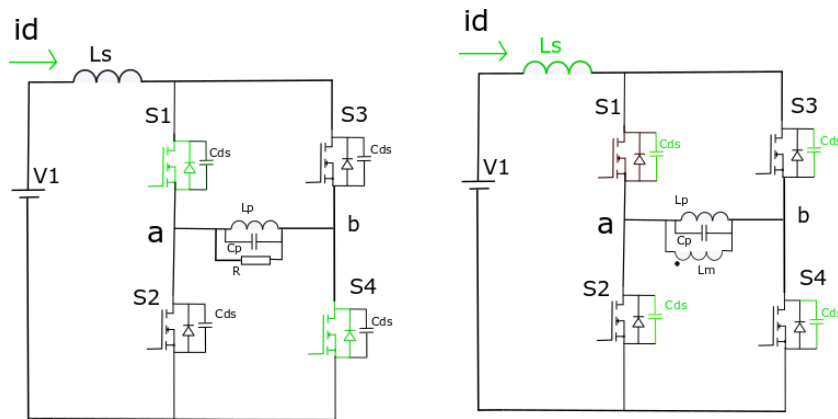


Figure 3-17: a) Equivalent circuit of a single full-bridge for the start-up analysis. b) The representation in the short-circuit interval, where the equivalent capacitor ($2x C_{ds}$) and the inductor (L_s) oscillates at the frequency $\omega_o = 1/\sqrt{2 C_{ds} L_s}$.

The goal now is to combine the forced switching signal, the short-circuit time, and the auto-oscillation detection into an OR logic port to generate the gating signals, in complement to the control proposed in Figure 3-10. After this initialization phase, the oscillation becomes close to the natural frequency calculated by the following expression:

$$F_r = \frac{1}{2\pi} \sqrt{\frac{L+(L_{stray}+L_s)}{(C_p+2C_{ds})(L_s+L_{stray})L}} \quad (46)$$

L_{Stray} represents parasitic inductances on the AC side between the transistors connected in the same leg. The solution containing the new initial condition different from zero, $v_C(t=0) = -V_{Co} \neq 0$, is used to solve the Eq. (39):

$$v_c(t) = -e^{\frac{-t}{2RC}} \frac{(V_{Co} + \frac{LV_1}{L_s})}{\sin(\phi)} \sin(bt + \phi) + \frac{LV_1}{L_s} \quad (47)$$

The voltage over the parallel capacitor can now be negative or positive, meaning that zero voltage crossing may be detected, and ZVS ensured during the converter initialization.

Now we can calculate the ideal time interval to apply the short-circuit signal based on the initial condition for the capacitor voltage, between points “a” and “b”. This time is required to the voltage pass through zero from a negative value.

$$v_c(t = t_{min}) > 0$$

$$e^{\frac{-t_{min}}{2RC}} \sin(b t_{min} + \phi) < \frac{V_1 L \sin(\phi)}{L V_1 + L_s V_{Co}}$$

We consider that the required time necessary for increasing the current is too short and that the equivalent parallel resistance to avoid damping the oscillations is large, close to infinite in the ideal case. In this case, we have:

$$t_{min} > -2RC \ln\left(\frac{V_1 L}{V_1 L + V_{Co} L_s}\right) \quad (48)$$

Two conditions can be verified to obtain the natural oscillation: the damping factor related to the equivalent load connected at the sourcing ports during the start-up; and the initial condition different from zero, obtained through the forced switching at fixed frequency or the short-circuit strategy:

$$4 R^2 C > \frac{L_s L}{(L+L_s)} \quad (1^\circ \text{ Condition})$$

$$v_C(t = 0) \neq 0 \text{ or } i(L_s) \neq 0 \quad (2^\circ \text{ Condition})$$

The second condition, when satisfied with the short-circuit strategy initiates the converter's natural oscillation but is not essential to the converter operation. The same initial condition could be obtained by applying a forced switching command to switch both transistor pairs during the first cycles of the converter controller. However, the initial forced switching frequency should be smaller than the original resonant frequency to prevent hard switching. The combination of these three signals is proposed to generate the converter control in Figure 3-18. In addition, to prevent high voltage peak stresses during transients, the DC side voltage should be increased gradually. The load connected to the output should demand a very small load current at the beginning of the converter operation respecting the 1^o condition to obtain ZVS condition.

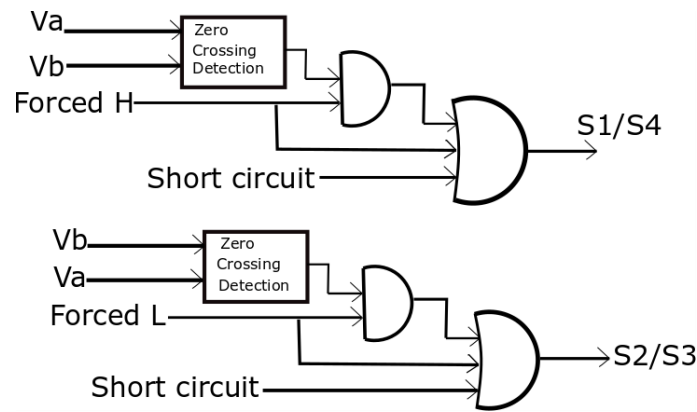


Figure 3-18: Control signals combining the short-signal time during start-up, the forced switching signal for the initial cycles and the zero voltage crossing detection.

Simulation results validate the initialization of the converter presented in Figure 3-2 with the components listed in Table 3-2. At first, the four MOSFETs are turned-on for a certain duration, before the normal switching operation. In Figure 3-19, a small short-circuit time of 4 μ s is applied for starting the converter natural oscillation. In this first simulation, the voltage V1 starts from its nominal value. Note that the initial oscillation between the MOSFET parasitic capacitances and the input inductor L_{s1} generates a high voltage peak at the beginning. In Figure 3-20, the same test is repeated, but with increased short-circuit duration, 10 μ s, charging the inductor L_{s1} with more energy and consequently generating a higher first voltage peak, which can provoke the MOSFETs breakdown.

Parameters	Value
DC side inductor (L_s), Parallel inductor (L)	314 μ H, 157 μ H
Parallel resonant capacitor (C)	4.4 nF
MOSFET capacitance (C_{ds}/C_{oss})	200 pF
Voltage source (V1)	50 V
Resonant Frequency	200 kHz

Table 3-2: Converter Design Information for each full-bridge.

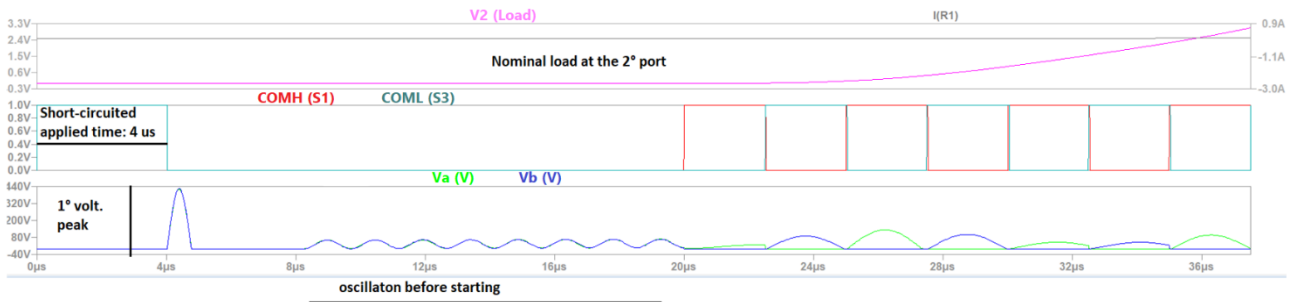


Figure 3-19: Simulation results when the short-circuit time is enough to pre-charge the circuit and the oscillation between C_{ds} and L_{s1} occurs naturally before the converter normal operation.

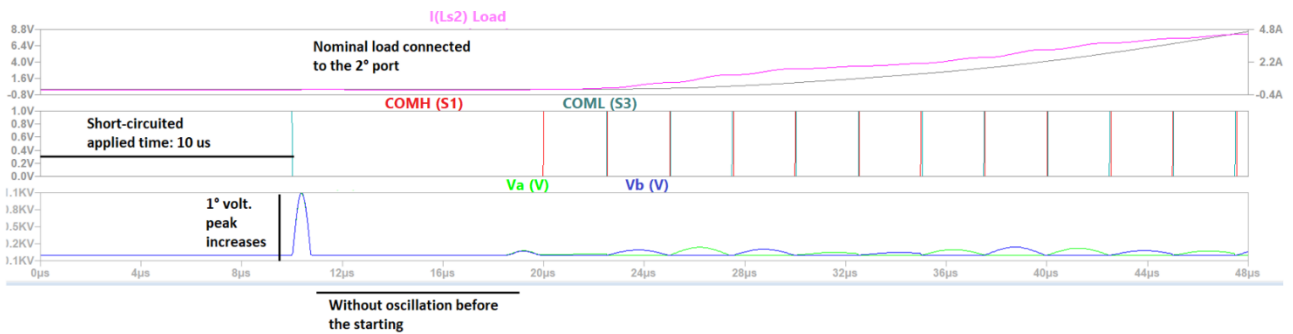


Figure 3-20: Simulation results when the short-circuit time was increased. Observe that no natural oscillation between the MOSFET capacitances and L_{s1} is observed. The short-circuit time applied is higher than the required time to pre-charge the inductor L_{s1} .

The methodology has been validated first using only a single full-bridge of the circuit presented in Figure 3-2. A resistance of 200Ω was connected in parallel with the resonating cell. The experimental verification was possible because the converter prototype was made using independent modules to connect and disconnect the ports. The results are shown in Figure 3-21. Note that the voltages V_a and V_b , are slightly dampen because of the equivalent resistance, too close to the minimum value calculated with the first condition, 150Ω .

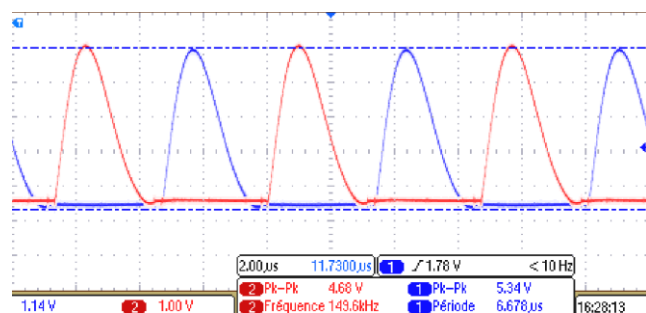
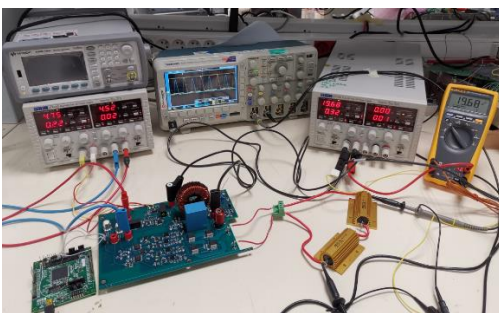


Figure 3-21: Experimental results obtained with a single full-bridge at first. Voltages V_a and V_b measured for a single full-bridge $R = 200\Omega$ (V/V : $1/20$).

Before testing the entire converter presented in Figure 3-2 at nominal conditions, we must avoid the high voltage peak applied to the transistors. In Figure 3-22 and Figure 3-23, the voltages V_a , V_b and the current on the DC side (i_{Ls1}) are compared during the transient state. In the first figure, the voltage

V1 starts at its maximum value, and in Figure 3-23, the same nominal voltage is achieved, but this time through an increasing by steps. In the first situation, the voltage peak on the transformer exceeds the value obtained during the steady-state.

The prototype design is discussed in Chapter 5, but to validate the converter's startup behavior, we present some results in this section. In Figure 3-24 and Figure 3-25, the voltage V_a and the current in the primary side of the converter, i_1 , are presented using the Three-port current-fed from Figure 3-2. In these results, the voltage V1 was increased by steps, thus eliminating higher voltage peak stresses and avoiding the MOSFETs breakdown during the transient.

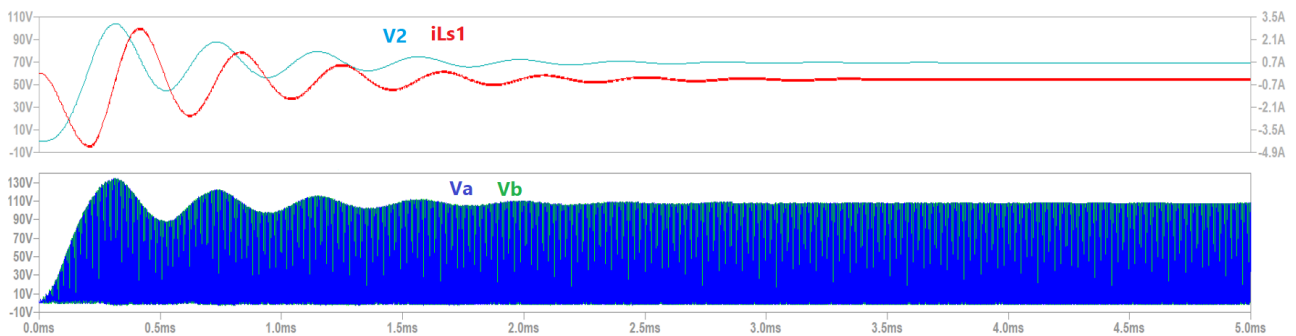


Figure 3-22: Transient simulation result. Voltages V_a , V_b and the DC side input current obtained for the Three-port Current-fed resonant converter.

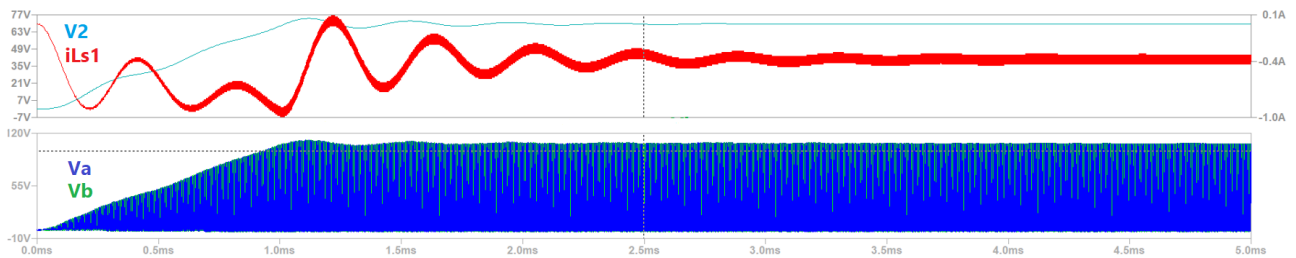


Figure 3-23: Transient simulation result: Voltages V_a , V_b and the DC current side of the Three-port Current-fed parallel resonant converter. The input DC voltage is linearly increased until the nominal voltage.

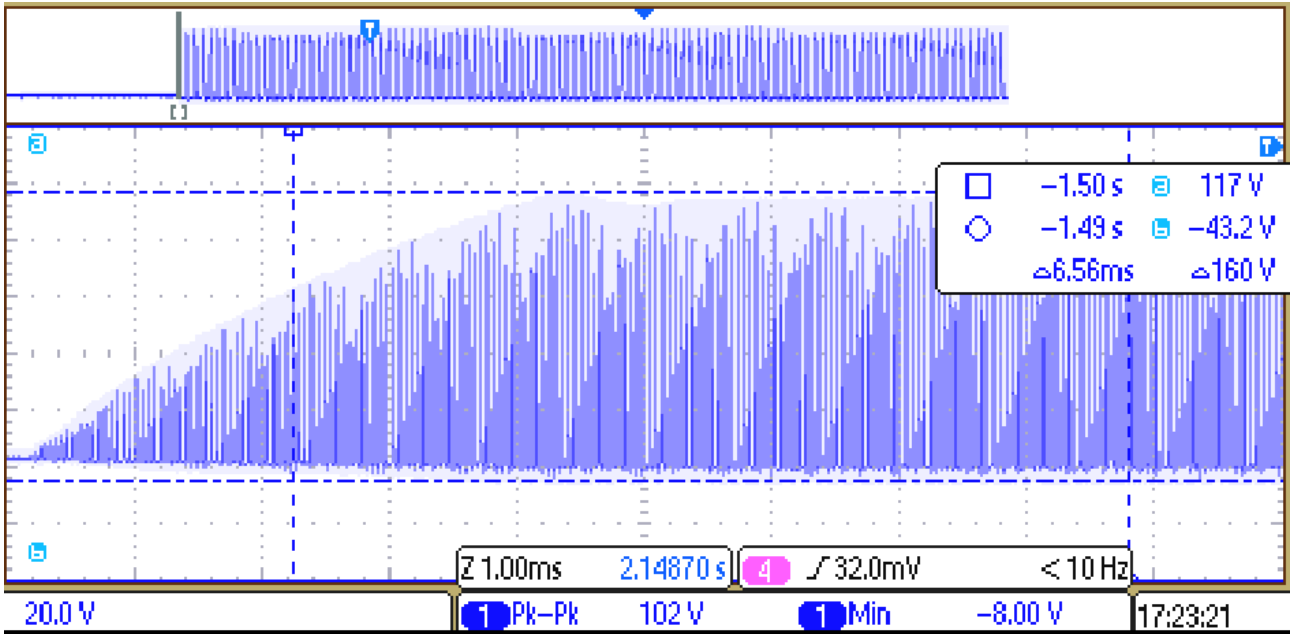


Figure 3-24: Voltage V_a for the Three-port current-fed parallel resonant converter. The input voltage V_I is increased by steps.

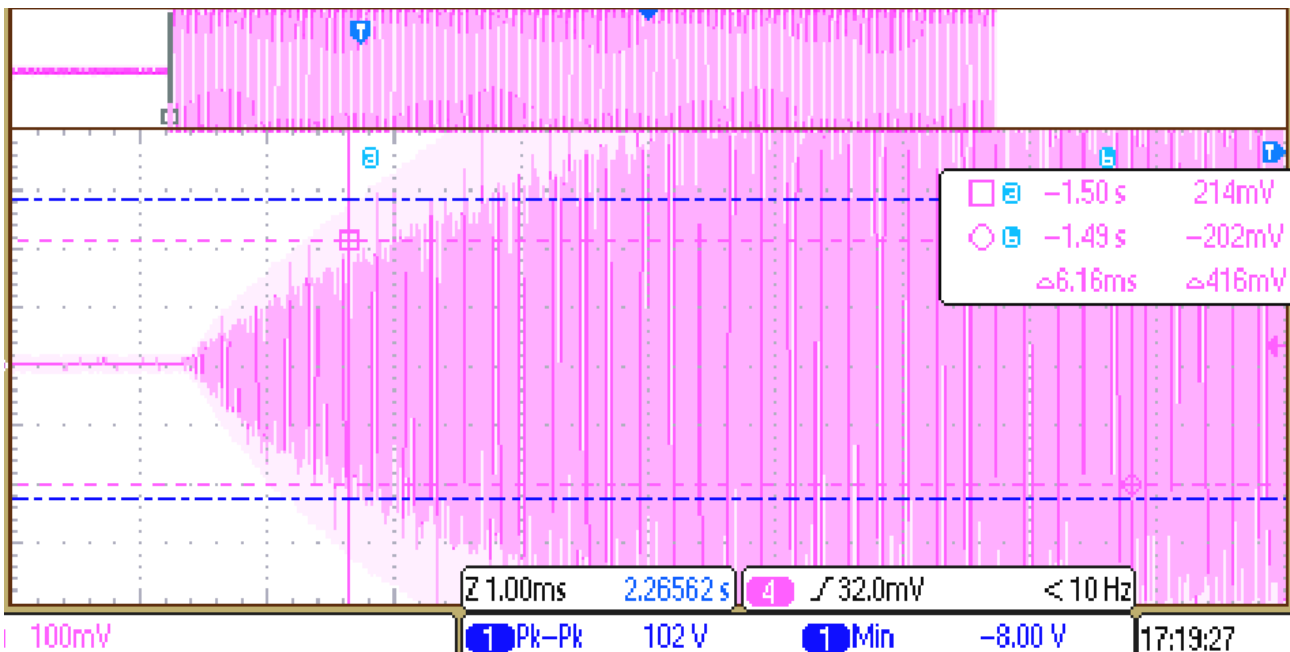


Figure 3-25: Current $i_1(t)$ in the Three-port current-fed parallel resonant converter while the DC input voltage is increased by steps. (20mV/A).

3.6- Conclusion

In this chapter, a three-port current-fed resonant converter is proposed to integrate the OBC and LDC converters. The topology presented keeps ZVS for the entire power range and permits the converter design for high switching frequency. Their operation and control strategies are also presented. Because of the current-fed arrangement with resonant elements, a start-up methodology to obtain ZVS

is proposed. The methodology without additional cost eliminates increased voltage peaks during transients. Two conditions must exist to achieve ZVS during start-up: a command used to obtain an initial condition different from zero and a small current load to avoid damping the natural oscillations. The forced switching at a fixed frequency smaller than the resonant frequency also initiates the converter operation. On the other hand, the initial conditions, when obtained with an initial short-circuit time to increase the current in the DC side inductor, allows the converter's natural oscillation with zero voltage crossing detection. This strategy is useful to track the converter resonant frequency despite the aging and the tolerance of the components. The next chapter presents the transformer development adapted for this topology.

3.7- References

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4- Design of the integrated transformer

4.1- Introduction

As discussed in the previous chapter, the transformer is an essential part of the Bidirectional Three-port resonant converter design, and its characteristics will have a significant impact on the converter's final volume and efficiency.

Considering the characteristics of the studied converter, we see that leakage inductance has a negative influence on the converter behavior generating high-frequency oscillations. These oscillations, when not damped, can affect the zero voltage crossing detection used to generate the gating signals, increase the EMI, and even contribute to higher power losses during the transistors turn on. For those reasons, the transformer should present minimal leakage inductance at the converter operating frequency range.

However, the design difficulties are increased due to the resonant converter's unit voltage gain and the high voltage level difference between the HV and the LV side. A high transformer's turn ratio minimizes the constraints in the additional DC-DC non-isolated converters. Table 4-1 shows the variation range of the three DC voltage sources where V_{dc} is the DC link voltage from the PFC stage.

	AC grid	Batteries	Vdc	HV	LV
Voltage (V_{RMS})	85- 265	Voltage range	400-500 V	240-480 V	10- 16 V
Frequency (Hz)	50- 60	Nominal Volt.	480 V	400 V	14 V
Pmax (kW)	7.2 kW	Pmax (kW)	7 kW	7 kW	3.5 kW
Imax (A_{RMS})	32	IDC max (A)	15 A	17.5 A	250 A

Table 4-1: The voltage range of the three different voltage sources presented in the integrated power unit with OBC and LDC functions.

There are two different possible implementations for the transformer. The first one is the typical transformer implemented with regular magnetic cores using Litz-wire to reduce the skin effect phenomenon, and the second is the use of a planar magnetic core, which contains a ratio height/length smaller than conventional magnetic cores. In this second technology, the conductor arrangement has a better heat dissipation because the transformer occupies a larger area with the use of copper foils or multi-layer printed PCB boards. Usually, for high-frequency applications, planar technology presents better results since the copper thickness can be reduced without any additional cost compared to Litz-wire that requires manual operations to allow better current distribution over the conductor's length. In theory, the higher the operating frequency is, the higher will be the number of operations for the Litz crossing strands, increasing the effective transformer cost. A design choice of number and diameter of strands with cost-loss tradeoff curves can be found in [1].

The turn ratio between HV and LV sides has more impact on the transformer definition, thus this number should be selected at first. The non-isolated DC-DC converter could also present a buck or a boost behavior in a single direction of power flow, but to simplify the choice of the topology, it cannot realize both operations in the same direction. It can be considered a step-down function during direct power flow and boost during the reverse mode. In this case and based on Table 4-1, the maximum and minimum turn's ratio between both windings, connected to HV and LV side, respectively, can be chosen between 24:1 and 14:1. Considering now the power level in OBC mode, twice the power level required for operation in LDC mode, a unitary voltage gain between Vdc and HV allows minimizing the current circulation present in the transformer windings due to high-frequency effects. Therefore, the turns ratio between the three sides is defined for a limited range: 14:14:1 and 24:24:1. In the first design, we have opted to design a transformer with the highest possible turn's ratio, 24:24:1.

The transformer parameters are presented in Table 4-2. Because of the planar technology advantages, such as the better heat dissipation capacity and the good reproducibility concerning mainly leakage inductance, we had opted for a planar implementation.

	N1 (Vdc)	N2 (VHV)	N3 (VLV)
N	24	24	1
Vnom (V)	480	480	20
Vpeak (V)	900	900	37.5
Vmin (V)	220	220	10
Pmax (kW)	7	7	3.5
IRMS (A)	14.5	14.5	174
Ipeak (A)	14.5	14.5	174

Table 4-2: The transformer design parameters.

For the LV side, to reduce the equivalent resistance of this winding, the use of parallel-connected windings is essential; therefore, the current sharing problem must be solved to prevent a poor design at high-frequency operation.

4.1.1- Current sharing between parallel-connected layers at high-frequency

As it is well known, at high-frequency, the copper power losses increase drastically because of two main phenomena, usually associated with the Eddy currents: the skin and proximity effects. These two effects not only increase the equivalent resistance of the transformer generating a higher power loss, but it also results in magnetic leakage energy. One of the first works taking these two phenomena into consideration was made by Dowell in 1966. His paper [2] is one of the first references in the estimation of high-frequency effects for transformers.

The first phenomenon is easily explained by considering an AC current flowing in a conductor, as illustrated in Figure 4-1. This current creates a magnetic field at the same frequency as the current source. As this magnetic field is variable, it also induces a current inside this same conductor to try canceling the magnetic field variation. Because of the induced magnetic field that appears around the source current, the current tends to distribute itself near the conductor surface resulting in a higher current density on the conductor boards. The higher the frequency of the current, the more expressive is the skin effect. An example inside a single planar conductor can be seen in Figure 4-2 for different frequencies.

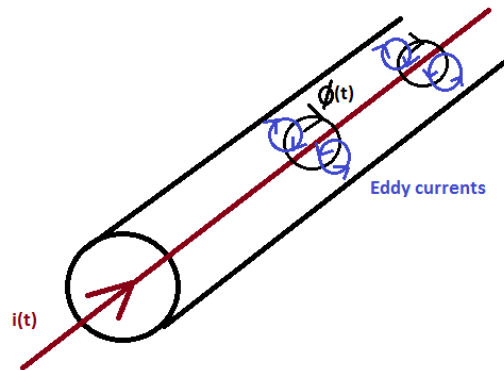


Figure 4-1: Eddy currents generated inside the conductor.

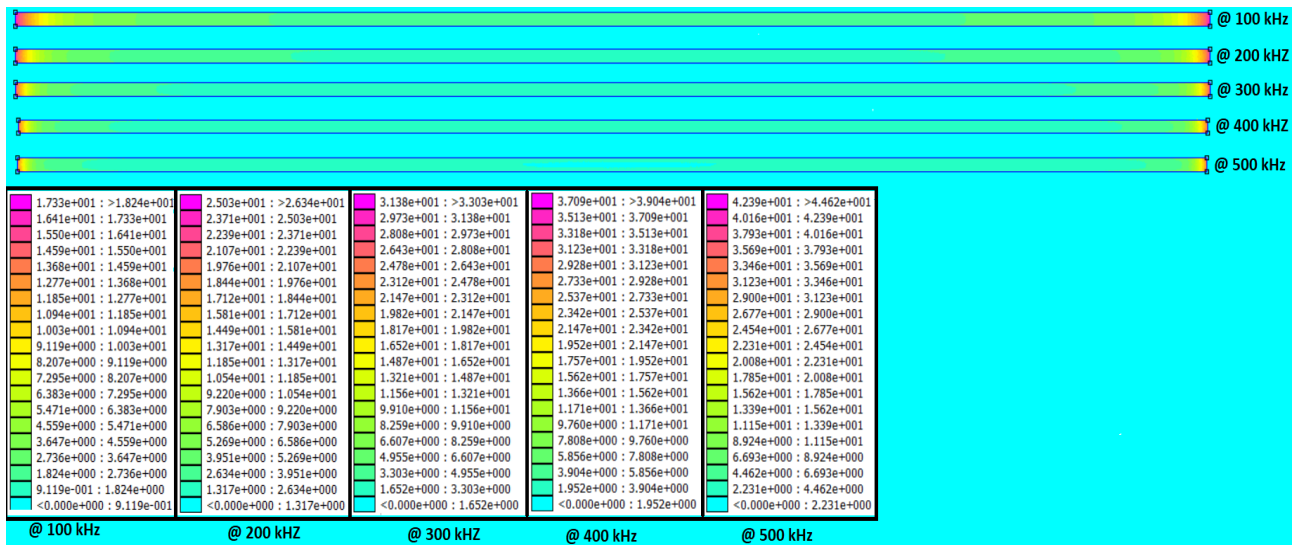


Figure 4-2: The current density inside a single planar conductor at different frequencies. Conductor height= 0.2 mm.

The proximity effect occurs in the same context, but with the magnetic field iteration between adjacent conductors. Figure 4-3 gives an example simulated with FEMM. The magnetic field created by the total current flowing inside one of the conductors interferes in its neighbor by inducing a current in the adjacent conductor to try compensating the magnetic field variation.

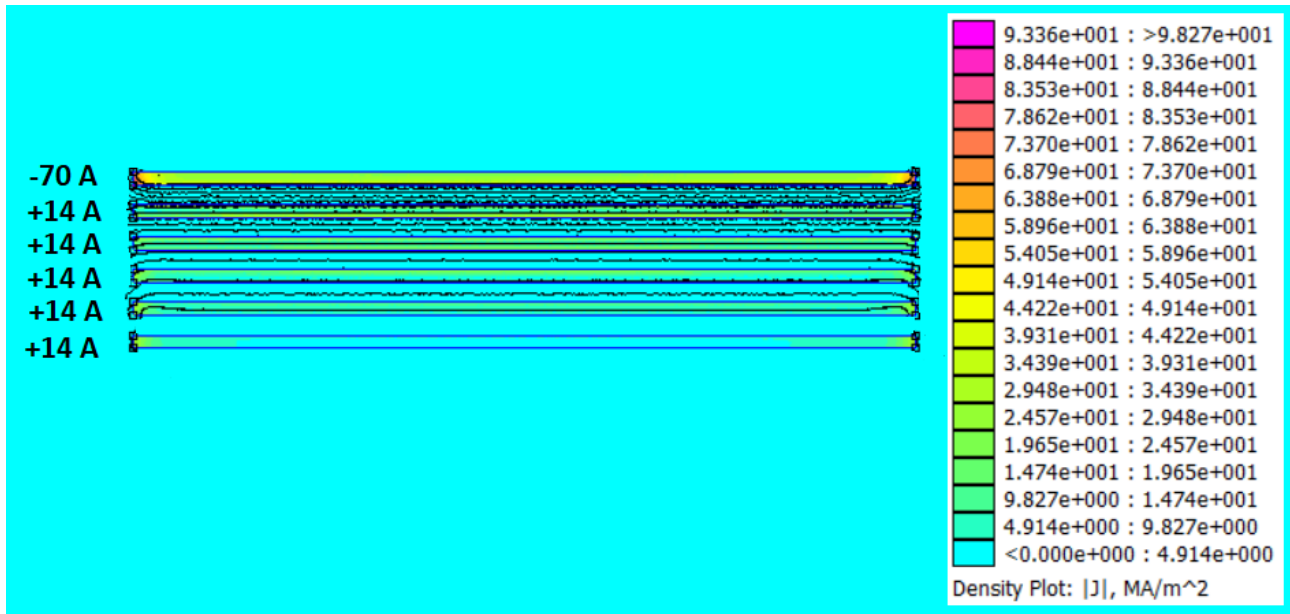


Figure 4-3: The current density inside adjacent planar conductors to illustrate the proximity effect, @ 100 kHz.

Both additional currents, from the skin and proximity effects, contribute to the increased apparent resistance in the transformer and the stored magnetic energy outside the conductors, resulting in leakage inductance.

4.1.2- Copper power losses and frequency-dependent components

In order to propose a mathematical approach to solve the problem considering the frequency dependence, the m.m.f (magneto-motive force) diagram is used to predict the magnetic field strength outside the conductor layers, as has been made by Dowell [2]. In this first approach, he has replaced circular conductors by square conductors with a mean turn length, but for planar conductors, there is no error considering this simplification. In the m.m.f diagram, the frequency alters the current distribution across each conductor, but the total current flowing inside the conductors remains constant. The magnetic field strength in the insulation layers (outside the conductors) is therefore not modified compared to a DC current, and its behavior inside the conductor layers is admitted linear. An example is presented in Figure 4-4, where a single winding is wrapped four times around the central-leg, representing an inductor.

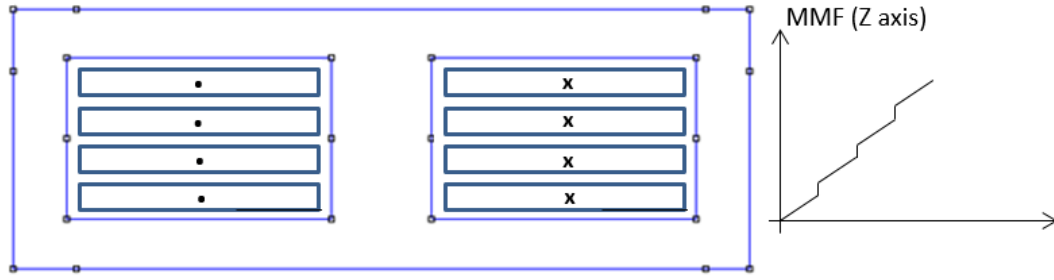


Figure 4-4: The m.m.f considering the AC resistance and leakage inductance independent from the frequency.

The frequency dependence is introduced by the skin effect in Figure 4-5. The total magnetic field strength outside the conductors remains the same presented in Figure 4-4. However, this time, the current distribution inside each conductor portion is taken into account, showing that the magnetic field inside these portions is no longer linear. The only difference is that the current is concentrated on the extremities. This phenomenon does not alter the magnetic field strength or its image, the m.m.f, outside the conductor layers.

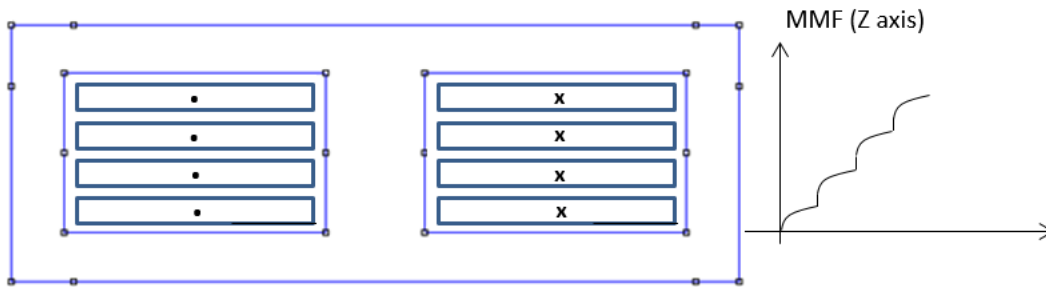


Figure 4-5: The m.m.f considering the AC resistance and leakage inductances dependent from the frequency.

In his work Dowell had considered the frequency dependence of the AC resistance and the leakage inductances by introducing some factors related to the DC values, commonly used nowadays. Later, his work had been improved, and some analytical models considering that skin and proximity effects are orthogonal had been studied in [3], giving results similar to equation (1). This model is widely used nowadays to find the relation between the AC and DC resistance in a planar transformer or an inductor.

$$R_{ac} = R_{dc} \frac{\xi}{2} \left[\frac{\sinh \xi + \sin \xi}{\cosh \xi - \cos \xi} + (2m - 1)^2 \frac{\sinh \xi - \sin \xi}{\cosh \xi + \cos \xi} \right], \quad \xi = \frac{\sqrt{\pi} d}{2 \delta} \quad (1)$$

Where δ is the skin depth, d is the conductor thickness, or equivalent diameter and m represents the m^{th} layer.

It is clear from the previous works that to minimize leakage inductance and the conductor power losses is essential to arrange all the positive and negative peaks of the m.m.f in such a way that the peaks are uniformly distributed without accentuated disequilibrium.

The problem with those approaches is that generally, when considering the existence of half-layers or when the conductor is divided into many portions to increase the current density, current is considered equally distributed between them. In one of the recent planar transformers developed in an HV-LV-DC/DC converter for electric vehicle applications [4], it had been noted that poor current distribution between the parallel-connected layers was a major problem, increasing temperature in the first prototype.

To solve this problem, and to prevent an inadequate current distribution for planar transformer design, we usually investigate current distribution with Finite Element analysis. However, due to time consuming, and the difficulties of FEM tools utilization in a pre-design stage, an innovative method is presented in the next section. This method can be quickly solved by a program routine in Matlab and allows finding an optimized solution considering plenty of propositions. The method and a first implementation are available in [5], and it was developed to analyze the transformer power losses in this thesis and also in the work presented in [4].

4.2- How to solve the current sharing problem with a more accurate analytical approach

The m.m.f diagram presenting an image of the magnetic field strength in the conductor and on the insulation portions of a planar magnetic component is not enough to determine the AC resistance and leakage inductance if the total current flowing inside a conductor divided into portions is considered unaltered. An additional step is necessary to analyze the current sharing inside parallel-connected conductors, before the determination of other parameters, as resistance and total leakage inductance. This analysis is fundamental to prevent poor current sharing inside the winding and, consequently, a poor temperature distribution in the transformer. For the applications concerned, as an HV to LV DC-DC, when one or more windings carry significant current, it is essential to propose an efficient arrangement of the conductor layers.

The magnetic structure presented in Figure 4-6 has N conductor layers distributed around the magnetic central-leg, and it also contains a small air-gap. In order to solve the problem and to limit the solution in a 2D dimension, some assumptions are necessary:

The magnetic field strength, \vec{H} , or the magnetic flux density, \vec{B} , between the conductor plates are mainly perpendicular to the central leg of the magnetic core. This assumption can be made if we consider conductor plates, with thickness much smaller than width. The magnetic core permeability is infinite compared to the other elements, and the air gap is small. This assumption is necessary since fringing paths are not modeled on this approach. Consequently, to prevent the field lines to go too far from the central leg, the air gap is considered small. Inside each conductor portion, a current $i_K(t)$ and

its respective magnetic flux $\phi_K(t)$ are considered. Outside the conductor region, the m.m.f, $J_K(t)$, is created by this same current. We represent by $\varphi_K(t)$ the magnetic flux outside the conductive regions, through the insulation layers. The total magnetic flux just after the k th conductor is represented by $\psi_K(t)$. This total magnetic flux is the contribution from all the conductor portions placed ahead, on its right side. Hence, the positions of zero m.m.f correspond to the end or the beginning of each section.

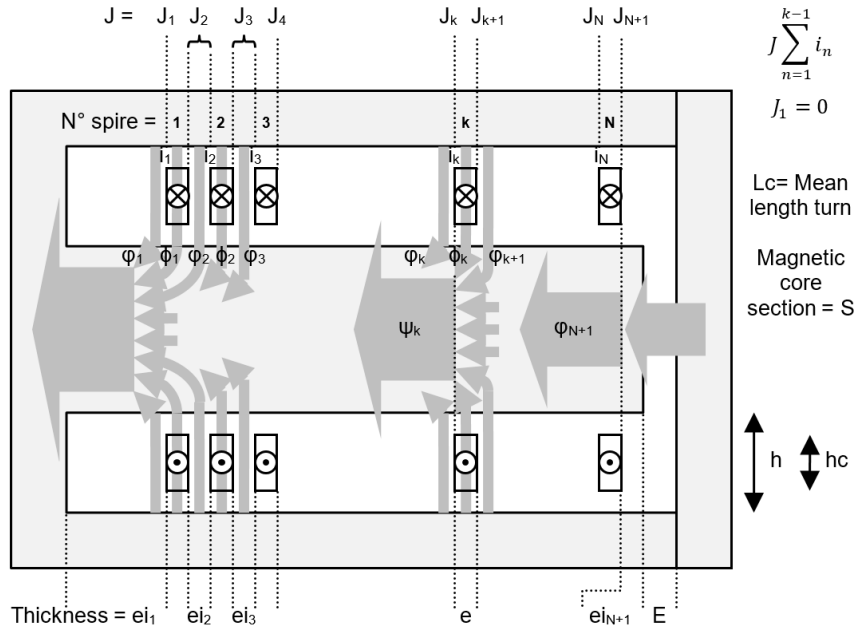


Figure 4-6: The representation of a planar magnetic structure with N conductor's layers around the magnetic central-leg.

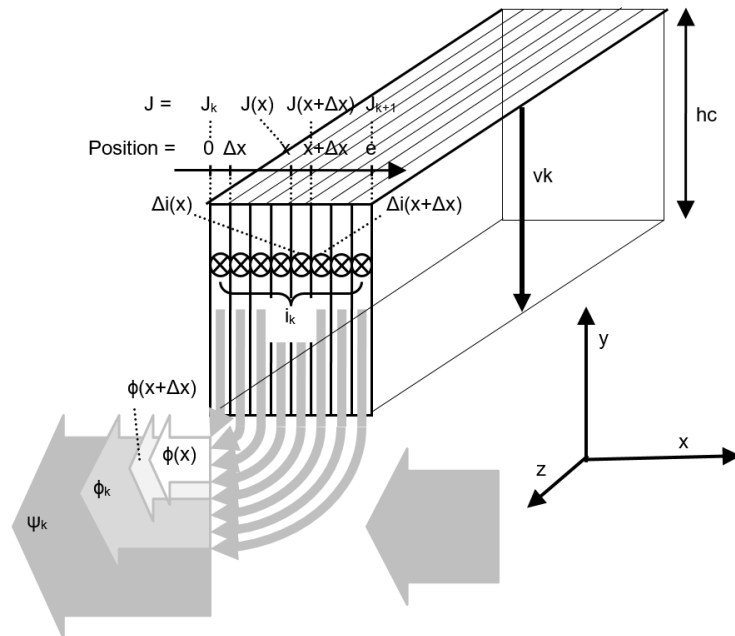


Figure 4-7: A single conductor plate divided into sub-sections.

A single conductor plate of a specific winding is represented in Figure 4-7. Inside each section of this conductor layer flows a portion of the total current depending on position and time $\Delta i(x, t)$. An

equivalent voltage drop in the x-axis reflects the magnetic flux variation inside this section of thickness Δx .

$$\Delta i(x + \Delta x) - \Delta i(x) = \frac{1}{r} \frac{d[\phi(x+\Delta x) - \phi(x)]}{dt} \quad (1)$$

The m.m.f is calculated by the Ampère's law and its variation occurs mainly in the y-axis, perpendicular to the central-leg of the magnetic core:

$$J = \oint \vec{H} \cdot \vec{dy} = \oint \frac{\vec{B}}{\mu_o} \cdot \vec{dy} = \oint \frac{\Delta \phi}{\mu_o (\Delta x \Delta L)} dy = \frac{\Delta \phi}{\mu_o \Delta x} \oint \frac{dy}{\Delta L} \quad (2)$$

$$\Delta \phi = \frac{J \mu_o \Delta x}{\oint \frac{dy}{\Delta L}} \quad (3)$$

ΔL is the conductor length over the z-axis.

The equivalent resistance of each conductor section can be calculated as:

$$\frac{1}{\Delta r} = \int \frac{\Delta x dy}{\rho \Delta L} = \frac{\Delta x}{\rho} \int \frac{dy}{\Delta L} \quad (4)$$

The total magnetic flux inside the conductor section is thus calculated by the sum of the magnetic flux portions inside the conductor.

$$\sum \Delta \phi = J \mu_o \sum \frac{\Delta x}{\oint \frac{dy}{\Delta L}} = J \mu_o \sum \frac{\Delta r \Delta x^2}{\rho} = \frac{J \mu_o}{\rho} r \Delta x^2 \quad (5)$$

And by using Faraday's law again, the current variation inside a conductor portion can be expressed by:

$$\Delta i(x + \Delta x) - \Delta i(x) = \frac{1}{r} \frac{d \sum \Delta \phi}{dt} = \frac{\mu_o \Delta x^2}{\rho} \frac{dJ}{dt} \quad (6)$$

The m.m.f can be represented by a sinusoidal current, so we can write:

$$\frac{\Delta i(x + \Delta x) - \Delta i(x)}{\Delta x^2} = \frac{\mu_o}{\rho} \frac{dJ}{dt} \rightarrow \frac{\mu_o}{\rho} j\omega J = \frac{d^2 J}{dx^2}$$

$$J = J_A e^{\alpha x} + J_B e^{-\alpha x}, \quad x_o = \sqrt{\frac{2\rho}{\mu_o \omega}}, \quad \alpha = \frac{1+j}{x_o}$$

Coefficients J_A and J_B depend on m.m.f in the extremities of the kth conductor section, between points $x = 0$ and $x = e$. Therefore:

$$J_K = J_{A_K} + J_{B_K} \quad \text{and} \quad J_{K+1} = J_{A_K} e^{\alpha e} + J_{B_K} e^{-\alpha e}$$

$$J_{A_K} = \frac{-J_K e^{-\alpha e} + J_{K+1}}{e^{\alpha e} - e^{-\alpha e}} \quad \text{and} \quad J_{B_K} = \frac{J_K e^{\alpha e} - J_{K+1}}{e^{\alpha e} - e^{-\alpha e}} \quad (7)$$

Voltage drop in each portion of the conductor section can now be calculated. For example, the kth portion is submitted to a voltage drop related to magnetic flux variation ψ_k , according to Figure 4-6:

$$v_K = j\omega \psi_K + r \Delta i(x=0)$$

$$\frac{\Delta i}{\Delta x} = \frac{\Delta J_K}{\Delta x} = \alpha (J_{A_K} - J_{B_K}) \text{ for } x=0$$

$$v_K = j\omega \psi_K + r \Delta x \alpha (J_{A_K} - J_{B_K}) \text{ at } x=0$$

Resistance r is the DC equivalent value of the winding and depends mainly on its mean length turn (MLT). In order to simplify the analysis, this resistance is represented based on ΔL , h_c and Δx . Further improvements can be made later to compensate for this value with the real DC resistance by introducing a normalization factor. Therefore, the above equation can be expressed in the 2D analysis as:

$$v_K = j\omega \psi_K + \frac{\rho \Delta L \Delta x \alpha}{h_c \Delta x} (J_{A_K} - J_{B_K}) \text{ at } x=0$$

$$v_K = j\omega \psi_K + \frac{\rho \Delta L \alpha}{h_c} (J_{A_K} - J_{B_K}) \text{ at } x=0 \quad (8)$$

The total magnetic flux passing inside the magnetic core central leg in Figure 4-6 is the contribution of the flux inside N conductor layers, ϕ_k , and passing through the insulating spaces, φ_k :

$$\psi_k = \sum_{n=k}^N \phi_n + \sum_{n=k+1}^{N+1} \varphi_n \quad (9)$$

The flux passing inside the kth conductor can be described in the same way as the flux within the core's central leg:

$$\phi_K = \iint_{B \rightarrow dS} \vec{B} = \int_0^e \frac{\mu_0 J}{h_c} (dx \Delta L)$$

$$\phi_K = \frac{\mu_0 \Delta L}{h_c} \int_0^e J dx = \frac{\mu_0 \Delta L}{h_c} \int_0^e J_A e^{\alpha x} + J_B e^{-\alpha x} dx = \frac{\mu_0 \Delta L}{h_c \alpha} \frac{e^{\alpha e} + e^{-\alpha e} - 2}{e^{\alpha e} - e^{-\alpha e}} (J_K + J_{K+1})$$

$$\phi_K = \frac{\mu_0 \Delta L}{h_c \alpha} \frac{e^{\alpha e} + e^{-\alpha e} - 2}{e^{\alpha e} - e^{-\alpha e}} (J_K + J_{K+1}) \quad (10)$$

And the magnetic flux passing through the insulating spaces:

$$\varphi_K = \frac{\mu_0 \Delta L}{h_c} \int_0^{e_i} J_K dx = \frac{\mu_0 \Delta L}{h_c} J_K e_{i_K}, \quad 1 \leq k \leq N \quad (11)$$

In equation (9), we notice the voltage drop in a single layer created by the magnetic fluxes ϕ_k and φ_k flowing in adjacent conductors and insulating spaces, combined with its internal current distribution, due to the skin effect.

The equations (7), (8) and (9) show a linear correlation between the voltage drop in a single layer and m.m.f generated by each conductor portion, upon frequency dependence. It results in N equations with $(2N+1)$ unknown variables, v_k and J_k .

Using the information about winding connections and electrical conditions, as voltage or current, we can find the solution associated to the linear system. Hence, $(N_L - 1)$ conditions are necessary to describe the layer connections for a specific winding, where N_L is the number of layers linked to this winding, associated in series or parallel. In sum, if N is the number of total layers related to N_W isolated windings in the magnetic structure, $N - N_W$ is the number of required electrical conditions to the system solution. N_W external electrical conditions exist, indicating the voltage and/or the current. In layers connected in series, the total flowing current does not change from one layer to another. In layers connected in parallel, the voltage drop between $x = [0: e]$ is the same for all layers, as indicated in Figure 4-8. The last condition indicates the m.m.f at the end of the layout arrangement, which is zero, $J_1 = 0$. A square matrix $(2N+1) \times (2N + 1)$, is then obtained relating J_k and ψ_k , using equations (7), (8), (9), (10) and (11). Now, with these conditions, it is possible to determine the current sharing between parallel-connected layers and estimate a more accurate AC resistance and leakage inductance compared to the assumptions made by Dowell and the derived analytical studies.

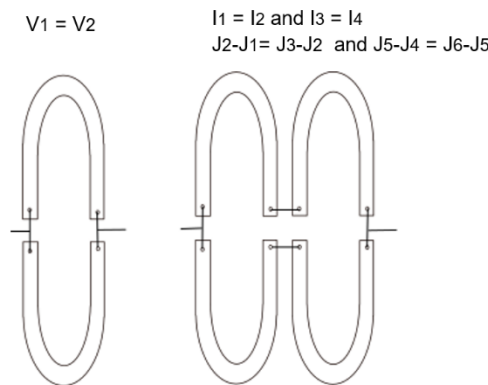


Figure 4-8: Example of parallel and series winding connection with the respective conditions.

A routine can be written in Matlab to solve this problem for different and numerous arrangements for a specific transformer design. It is necessary only to describe the winding layer's position, the connection type between them, the geometrical information about conductors sections, magnetic core, and the electrical parameters, such as voltage and current applied externally to the windings. In addition, a phase delay can also be added between voltage and current in a transformer winding. The inverse matrix only has to be calculated to give us information about current sharing inside the parallel-connected layers, power losses, and leakage inductance.

$$\begin{bmatrix} \psi_1 \\ \dots \\ \psi_k \\ \dots \end{bmatrix} = \begin{bmatrix} \frac{\mu_o L_c}{\alpha h} \cdot e i_1 \dots + \end{bmatrix} \begin{bmatrix} J_1 \\ \dots \\ J_k \\ J_{k+1} \end{bmatrix}$$

To exemplify, the current density obtained by applying the analysis proposed in this section is presented in a two-winding transformer containing series and parallel-connected layers, in Figure 4-9. In this example, the turn's ratio is 12:1 and the nominal current on the secondary side is 100 A, shared between 5 interleaved layers. Primary side has 12 series-connected turns distributed within 6 layers. Primary side has 12 series-connected turns distributed within 6 layers.

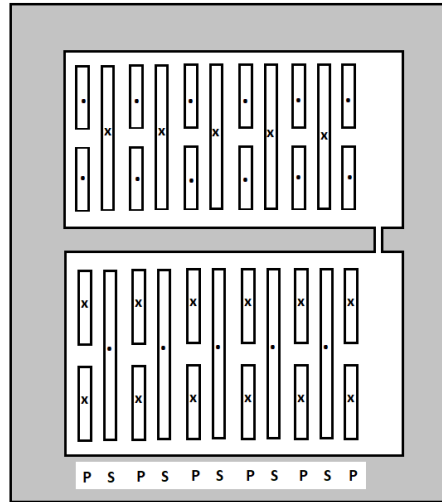


Figure 4-9: Example of series-connection in primary-side and parallel-connection in secondary-side.

The result in Figure 4-10 was obtained at 500 kHz. The method allows us to see that the current is not equally distributed between the five layers from the secondary side, and the two external layers carry a higher current density. Besides, inside each conductor section, a non-linear effect of high-frequency is also observed in the current distribution, reflected by an imaginary part of magnetic flux density.

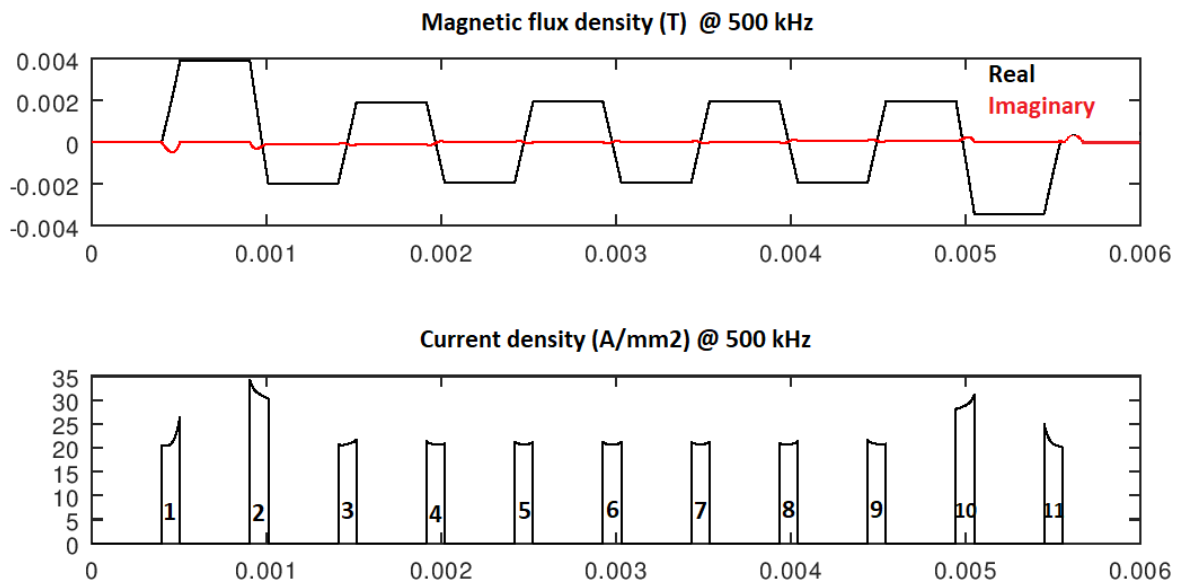


Figure 4-10: Magnetic flux and current density obtained with the analytical solution of the current sharing between parallel-connected layers.

The power losses can be directly obtained from results in Figure 4-10 by knowing about the physical properties and geometric dimensions of copper sections. Indeed, for total leakage inductance, depending on the insulating spaces between copper.

Now that we know how to predict current among parallel-connected layers, power loss, and leakage inductance, we can treat the design of our three-winding planar transformer. According to the assumptions made to solve the 2-D problem, the proposed analysis has some limitations. The winding part outside the magnetic core must be small. For the same reason, the air-gap must be carefully increased because of errors in the solution due to fringing effects.

4.3- Design of the unbalanced three-winding planar transformer for OBC and LDC

According to chapter 3, the transformer for the converter application discussed in this thesis has square current and sinusoidal voltage waveforms. Therefore, conductor power losses depend not only on switching frequency but also on current odd harmonics, taking into consideration at least the third and fifth components. Total power losses are then estimated by the sum of loss obtained for each component using the approach discussed in section 4.2.

Steinmetz approximation presents a proper result for losses in the magnetic core; thus, the coefficients given by the manufacturers are used in this estimation.

Considering now the power level application, the transformer operates under different power flow conditions, and the worst cases correspond to the maximum power in OBC, combined OBC/LDC modes, and LDC, as presented in Table 4-3. In the first mode, the electrical grid is connected, and through a Power Factor Correction (PFC) stage, the high voltage battery is charged. In the second case, the HV and LV batteries share the power coming from the electrical grid, and in the third case, the HV battery charges the LV battery while the electrical grid is idled.

Mode	N1	N2	N3
OBC	480 V / 7.0 kW	480 V / 7.0 kW	20 V / -
OBC + LDC	480 V / 7.0 kW	480 V / 5.0 kW	20 V / 2.0 kW
LDC	480 V / -	480 V / 3.5 kW	20 V / 3.5 kW

Table 4-3: Nominal power flow conditions considered for conversion efficiency equal to one.

The E planar core shape is a plausible choice for this integration since it allows higher power density. At 250 kHz, considering the magnetic material properties, the 3F36 and the 3C98 from Ferroxcube are the two pre-selected candidates presenting the best merit in the curve of power loss versus frequency. Considering different sizes of the E planar core, the closest magnetic core is selected for a maximum current density of 15 A/mm² and a window filling factor of 0.25. Compared to a traditional

transformer with a filling factor between 0.3 and 0.45, this number is smaller in the case of a planar transformer because the insulating material between conductors occupies a larger perimeter.

Because of the effective cost, we propose multi-layers PCB in the transformer integration. Consequently, standard values must be evaluated, and using equation (12), a multi-layer PCB with 105 μm copper thicknesses is the maximum thickness explored during the design allowing higher power density without also increasing skin effect.

$$\delta = \frac{1}{\sqrt{\pi F_{sw} \mu_o \sigma}} = 112 \mu\text{m}, \quad \mu_o = 4\pi \times 10^{-7}, \quad \sigma = 0.5 \times 10^8 \text{ S.m} \quad (12)$$

Another important argument is the maximum number of layers by PCB. Typically, PCBs with more than 4 layers are more expensive, but the cost can be significantly reduced depending on the total number of pieces. One strategy to limit the PCB cost is the association of multi PCBs, allowing the use of a reduced number of layers by PCB. Mechanical assembling of multi PCBs adds some constraints to the association, and to allow a robust and possible assembling under the industrial point of view, a maximum of 3 PCBs is considered, with a limit of 8 layers by PCB. The larger PCB has 105 μm of copper thickness and a maximum of 8 layers and must not have more than 3.2 mm of total thickness to reduce the complexity of the fabrication process considering mechanical aspects. Moreover, it is difficult to manipulate PCBs with higher thickness and avoid reflux of the solder flow in the vias connection.

The current balancing in the transformer operation can be improved by using interleaved configurations in the transformer, by minimization of the magnetic flux peak. However, due to the minimum insulation thickness required between low and high voltage sides, described in the standard IEC 61851-1 and illustrated in Figure 4-11, the use of interleaved configurations can increase the total PCB thickness.

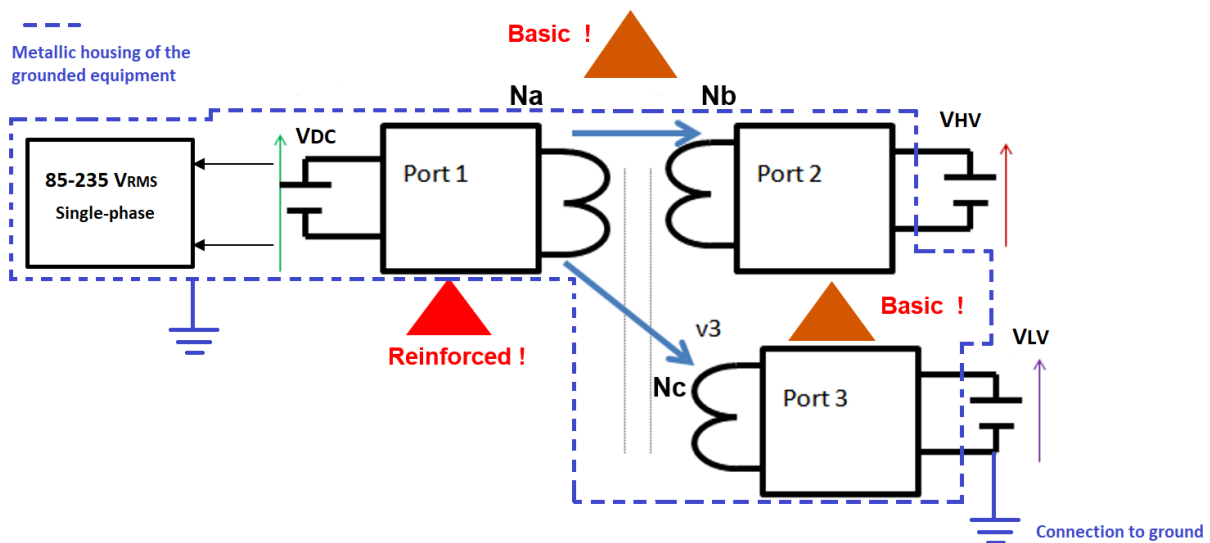


Figure 4-11: Insulation guidelines between the three different voltage sources present in the integrated OBC/LDC converter.

Three arrangements are proposed in Figure 4-12. The three configurations have the same conductor layout for both high voltage sides, consisting of three series-connected turns by layer and eight layers, required for each high voltage winding. In the low voltage side, the total current is distributed among five, six, or eight layers, depending on the resultant current density. The complete information is available in Table 4-4. The conductor layers are identified as primary, secondary, and third sides, (P), (S) and (T), respectively.

Parameters	Values
N° of layers Port 1	8 (Series) – 3 turns by layer
N° of layers Port 2	8 (Series) – 3 turns by layer
N° of layers Port 3	Between 5 and 8 (Parallel)
Copper thickness	105 μm (1, 2 and 3)
Initial core permeability	2400
Mean turn length	112.4 mm
Core section	518 mm^2
Max. N° of layers by PCB	8
Max. PCB total thickness	3.2 mm

Table 4-4: Transformer parameters used in the design.

As the highest insulation thickness is required between the layers P and T or between the layers S and T, in the first arrangement from Figure 4-12, insulation thickness is reduced since the low voltage side does not participate in the interleaving layout. Assuming a linear behavior of magnetic field inside conductive layers and also, a current equally distributed between parallel-connected layers, the magneto-motive force is represented, as indicated on the right side of each arrangement. In the first arrangement, at the low voltage side, parallel layers seem to behave as a conductor block with an increased cross-section area, not able to avoid high-frequency effects. The unbalanced magnetic field profile generates very poor current distribution on the parallel-connected layers.

In the second configuration, to improve magnetic field distribution, layers T are interleaved between layers P and S. This configuration, however, presents more constraints for the fabrication process and mechanical assembling, because of more intersections requiring reinforced insulation.

Because of the difficulties in the mechanical assembling, the third arrangement is an intermediary proposition. The layers T are set to be the external layers of each PCB to make easier the final connections. The last scheme is supposed to represent a midterm between the first and second arrangements regarding the efficiency and fabrication complexity. Note that the first configuration seems to have the least-favored performance while the last one seems to be acceptable.

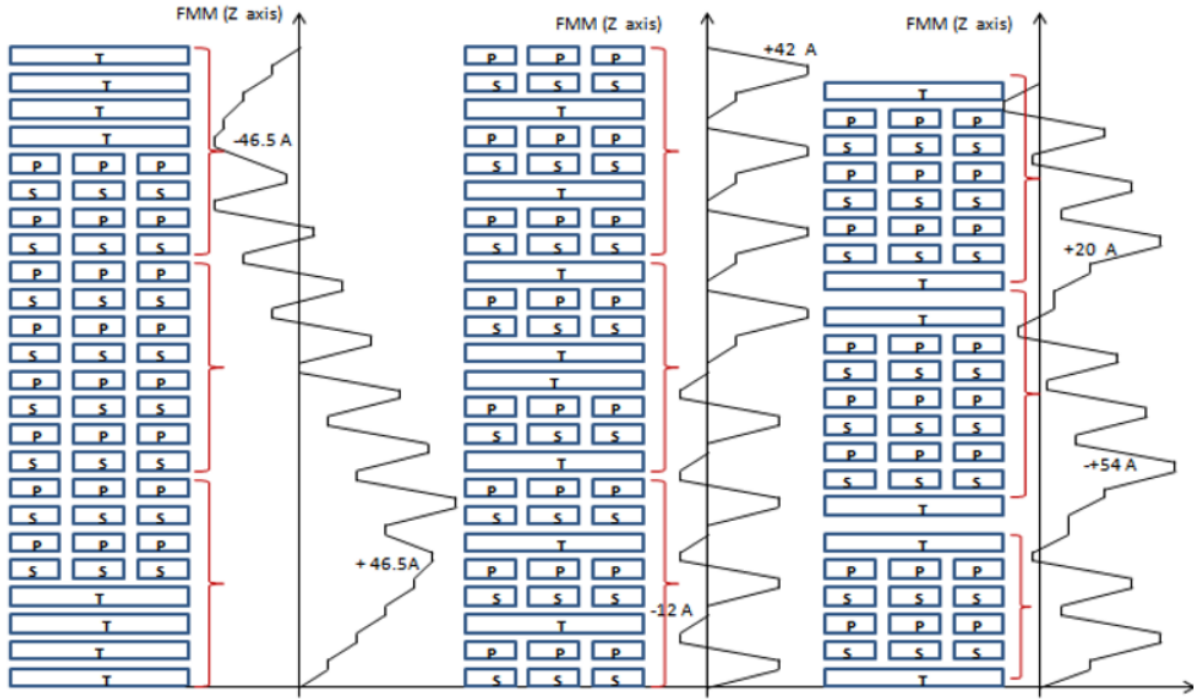


Figure 4-12: Proposed transformer arrangements and magneto-motive force estimated with approximations for equally current distribution between parallel layers and linear magnetic field strength. A) Non-interleaved B) Full-interleaved C) Partial-interleaved.

We can now use the analytical method proposed in section 4.2 for improved analysis. It is necessary to define three electrical conditions in the transformer, voltages v_k and currents J_k . We start with the simultaneous OBC and LDC operating mode. On the primary side, we indicate current and voltage, while on the secondary side, we indicate only the current, as shown in Table 4-5. The total current flowing into the first and secondary windings does not change from one layer to another; however, in the third winding, the voltage is the variable remaining constant among parallel-connected layers. Finally, 25 equations relating the voltage and the m.m.f over the conductor sections are written using a combination of equations (8), (9), (10), and (11).

Parameters	OBC + LDC mode	OBC mode	LDC mode
V1 / I1	480 V / 14 A _{RMS} (Ref)	480 V / 14 A _{RMS} (Ref)	-
V2 / I2	-10 A _{RMS} (180°)	- 14 A _{RMS} (180°)	480 V / 7.3 A _{RMS} (Ref)
V3 / I3	-	-	-175 A _{RMS} (180°)

Table 4-5: Conditions used in the analysis to calculate power loss and current distribution.

For OBC and LDC simultaneous converter operating mode and conditions presented in Table 4-5, the magnetic flux and current density in the first proposed arrangement of Figure 4-12 are presented in Figure 4-13. The magnetic field density contains real and imaginary parts, and the x-axis represents

the layer order, from bottom to top side. Note that the current in the parallel layers, T, is concentrated over the more internal layers, close to the interface with primary and secondary sides.

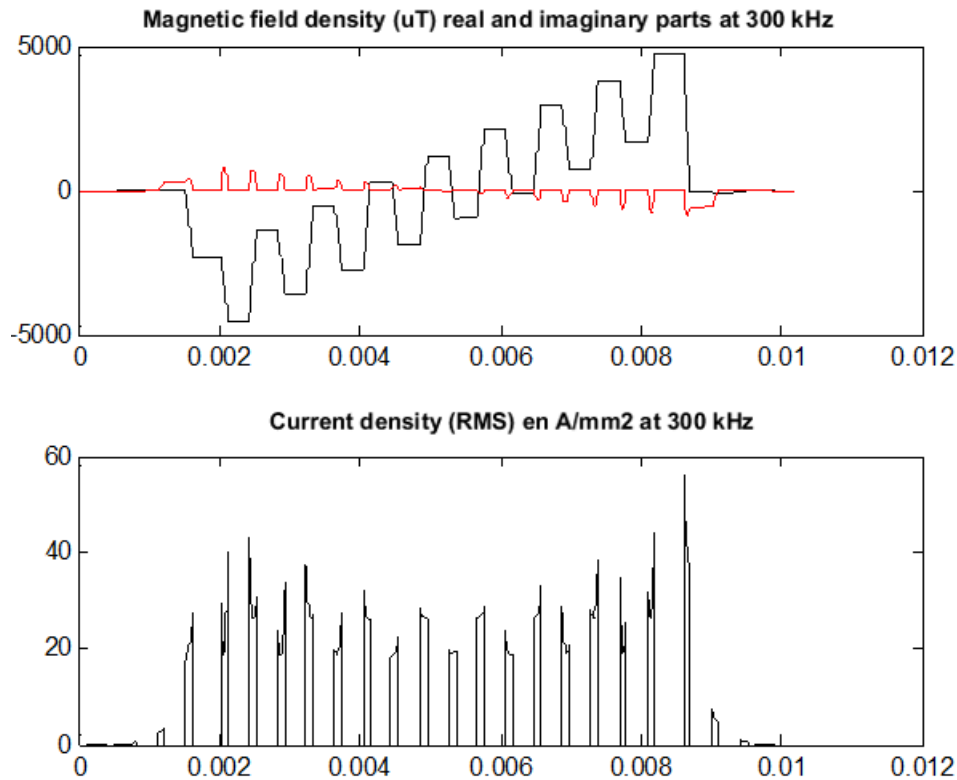


Figure 4-13: Magnetic flux density and current density for the non-interleaved arrangement.

The same conditions of OBC and LDC simultaneous operating mode are used to analyze the second and third proposed configurations indicated in Figure 4-12. The results are presented in Figure 4-14 and Figure 4-15, respectively, for the full interleaved and partial interleaved arrangements. As we can see from results, the non-interleaved, in comparison with the partial-interleaved arrangement, presents less conductive power losses. However, the magnetic field strength is more equilibrated in this last configuration presenting a smaller magnetic flux's peak and consequently reduced power loss in the magnetic core.

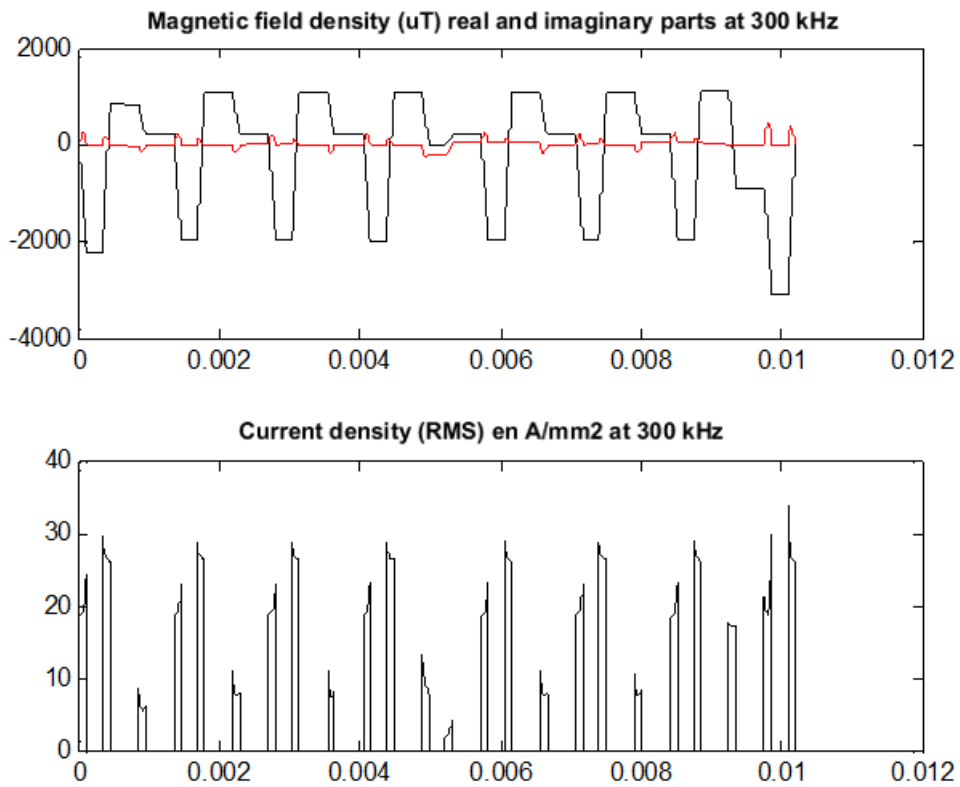


Figure 4-14: Magnetic flux density and current density for full-interleaved arrangement.

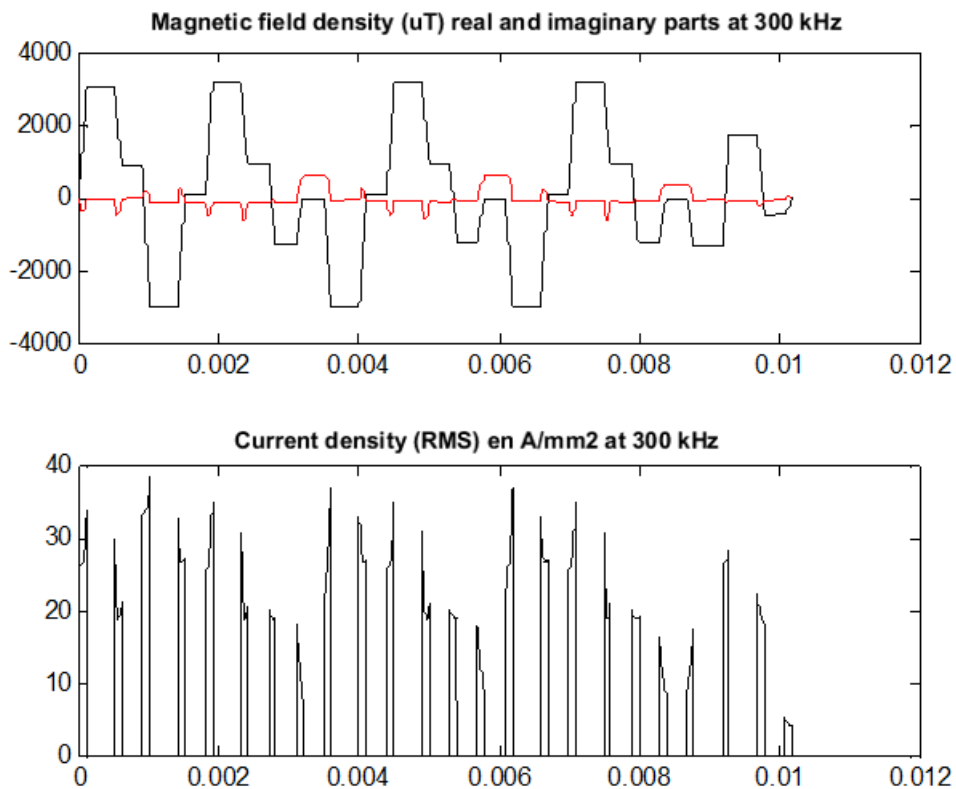


Figure 4-15: Magnetic flux and current densities for partial interleaved arrangement.

In order to validate these results, Finite Elements Analysis is now used to confirm the magnetic field intensity and current density profiles obtained with the analytical method. Since in the analytical

approach, we assume magnetic field strength as being perpendicular to the magnetic core's central-leg, a 2D-FEA analysis will be enough to verify the profile of magnetic flux and current density inside the conductor layers. The software used for this is the FEMM.

The same layout configurations described before in Figure 4-12 and the electrical conditions are indicated in the finite element analysis. We settle the distances between the conductor layers, and the frequency at 250 kHz.

Figure 4-16 shows the magnetic field strength and current density in the non-interleaved arrangement. Figure 4-17 and Figure 4-18 present results for the full interleaved and partial-interleaved arrangements, respectively. We can see that the magnetic field profile obtained with simulation is very similar to the results obtained with the analytic approach. When comparing the three configurations, the second arrangement has the best profile for current distribution and reduced power losses.

The third configuration, however, has a midterm performance. When the method for power losses calculation uses a linear magnetic field function to approximate power losses and the argument of a well-distributed current among parallel-conductors, the third configuration seems to have an acceptable performance. Nevertheless, in reality, if we consider the frequency dependency for the magnetic lines inside the conductors and that the current is not homogeneous distributed between parallel layers, the third configuration has higher power losses for LDC and simultaneous OBC&LDC operating modes, as can be seen in Figure 4-19. The results from the proposed analytical approach and FEMM confirm this obtained difference. The complete analysis considering a linear magnetic field strength and uniform current sharing among parallel conductors using Eq. (1) are available in Annexes.

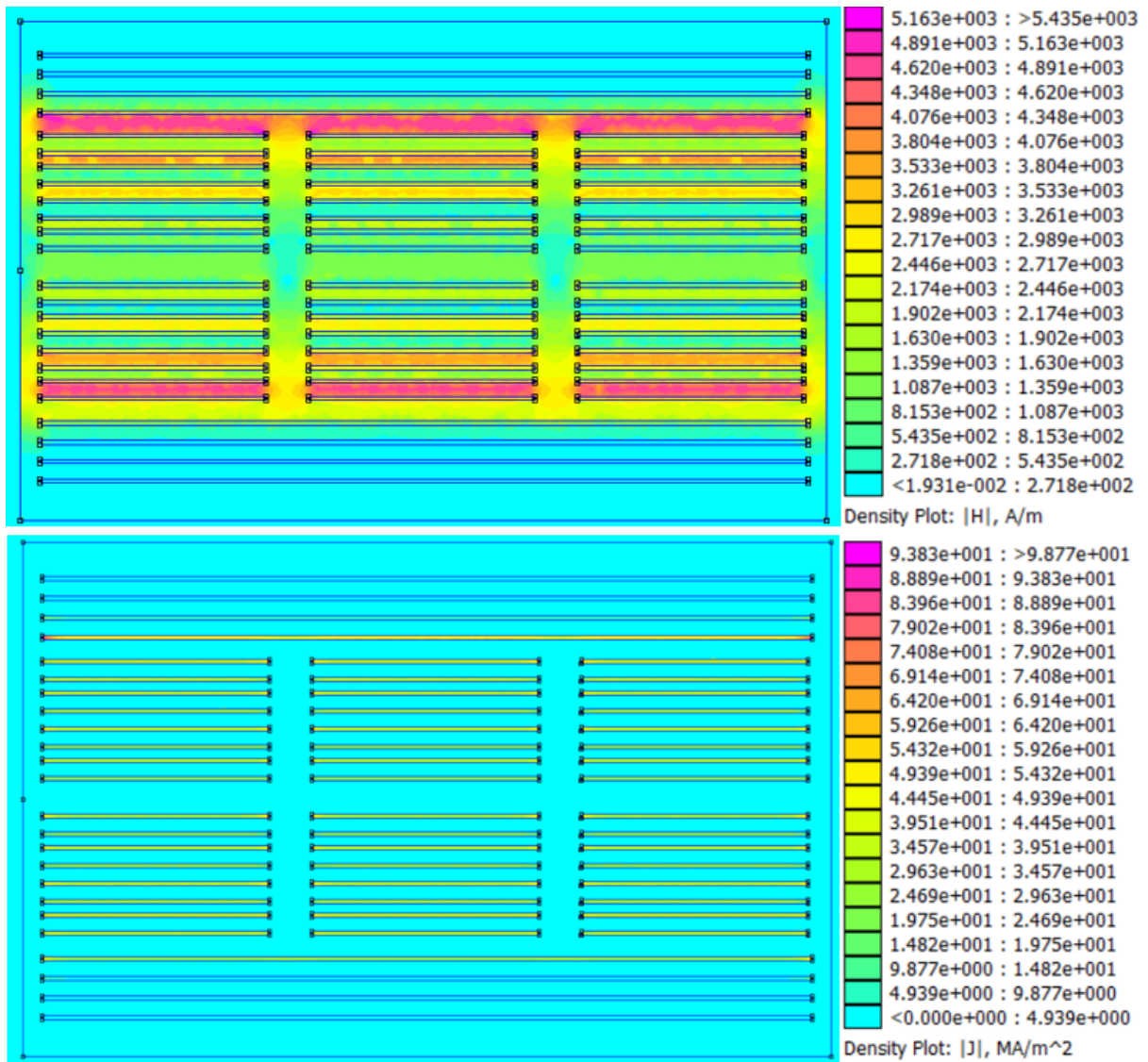


Figure 4-16: Magnetic flux strength (H/A) and current density (A/mm²) for the non-interleaved arrangement obtained in FEMM.

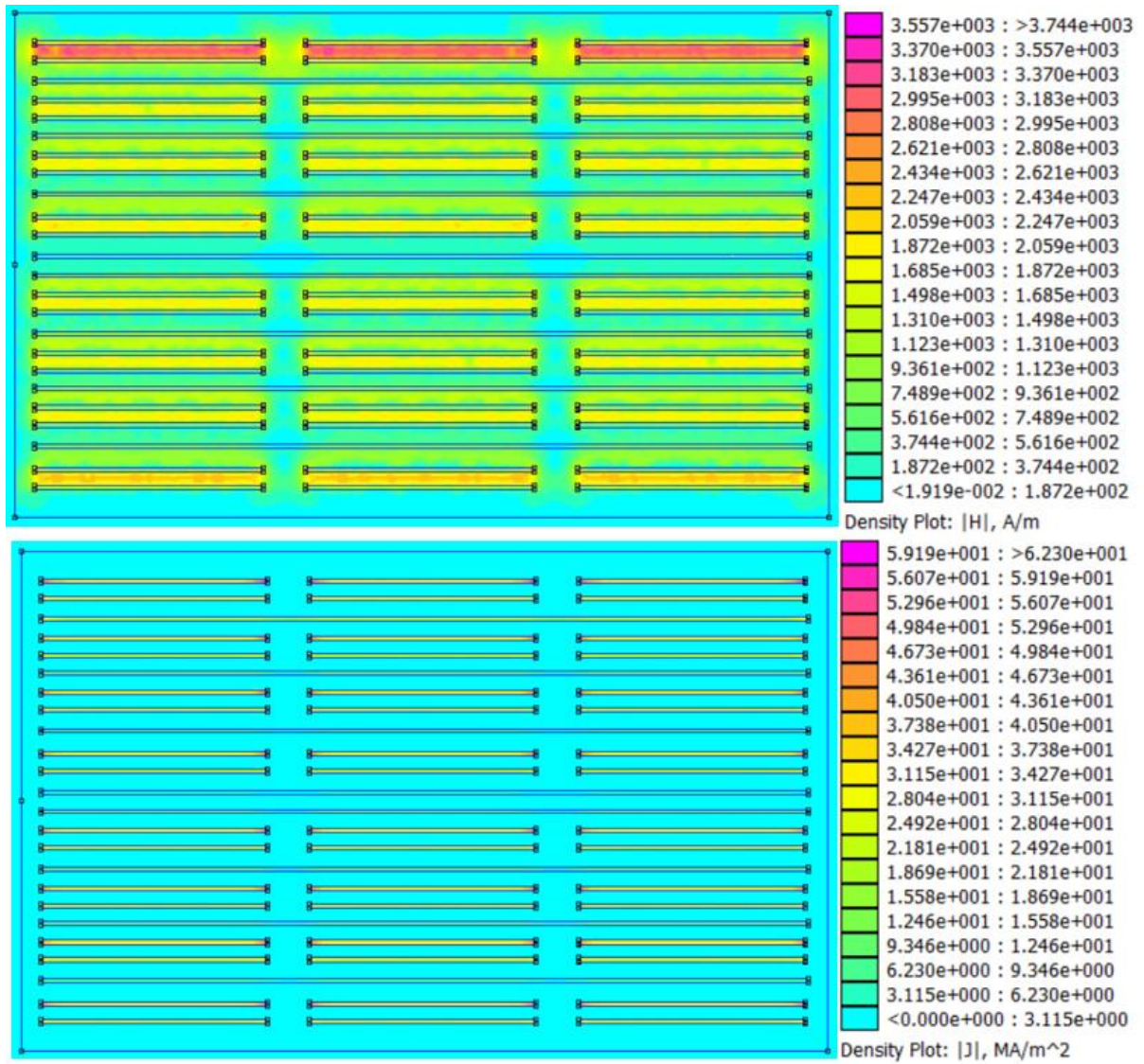


Figure 4-17: Magnetic flux strength (H/A) and current density (A/mm^2) for the full-interleaved arrangement obtained with FEA.

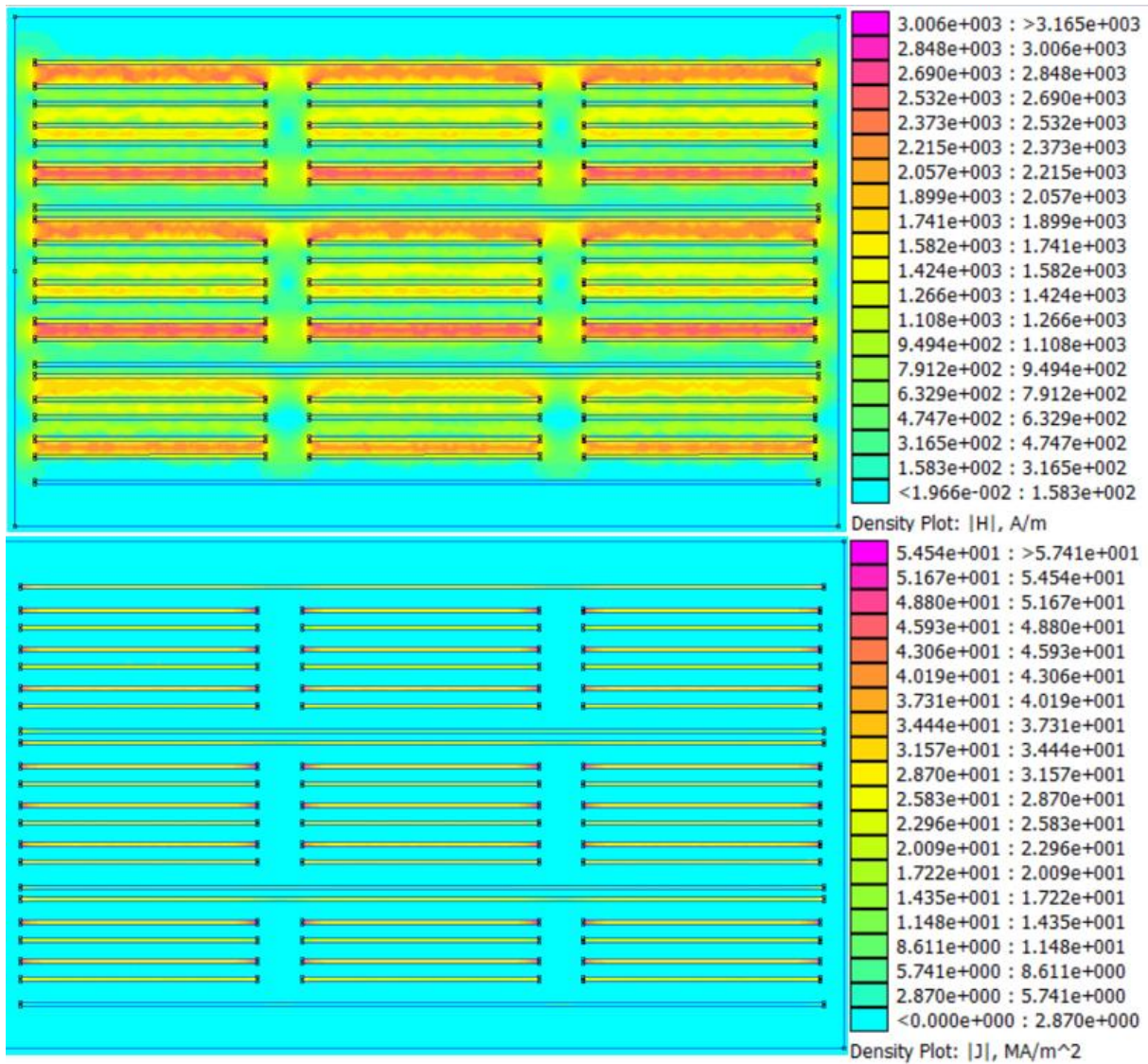


Figure 4-18: Magnetic flux strength (H/A) and current density (A/mm²) for the partial-interleaved arrangement obtained with FEA.

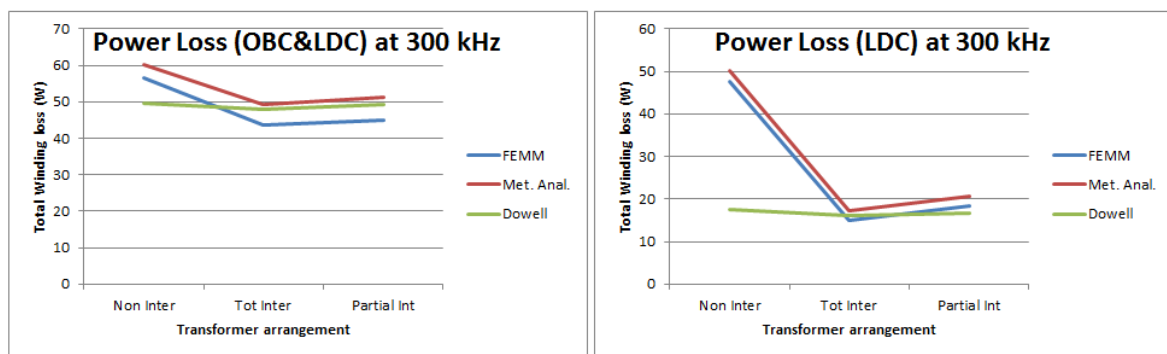


Figure 4-19: Total power loss comparison between the results obtained using the analytic method considering frequency effects and with simplification of linear magnetic flux and homogenous current sharing inside parallel-connected layers. OBC (5kW)&LDC(2kW) simultaneous mode at 300 kHz.

Both methods can be used to estimate power losses and leakage inductance when parallel-connected conductors exist. However, the proposed analytical method allows finding the solution without time

spending, as is usually required for Finite Element Analysis. It thus allows the analysis of a significant number of design propositions in an optimization routine.

Using the full-interleaved arrangement and following the conditions from Table 4-5, the analytical approach implemented in Matlab allows the magnetic flux and current density determination for the OBC and LDC standalone operating modes. The results are presented below in Figure 4-20 and Figure 4-21, respectively. During OBC mode, the high-frequency effect is minimized, thus inducing a minimal current circulation in the third winding and reduced leakage energy. During LDC mode, there is a slight disequilibrium in the flux density, concentrated on one of the extremities. This disequilibrium was also verified during OBC and LDC simultaneously operating mode and occurs because of the two parallel-connected third side layers in the middle of the arrangement. As long as this peak remains small, there is no reason for not selecting this second proposed design. The total power losses are presented in Table 4-6, according to nominal conditions for each operating mode.

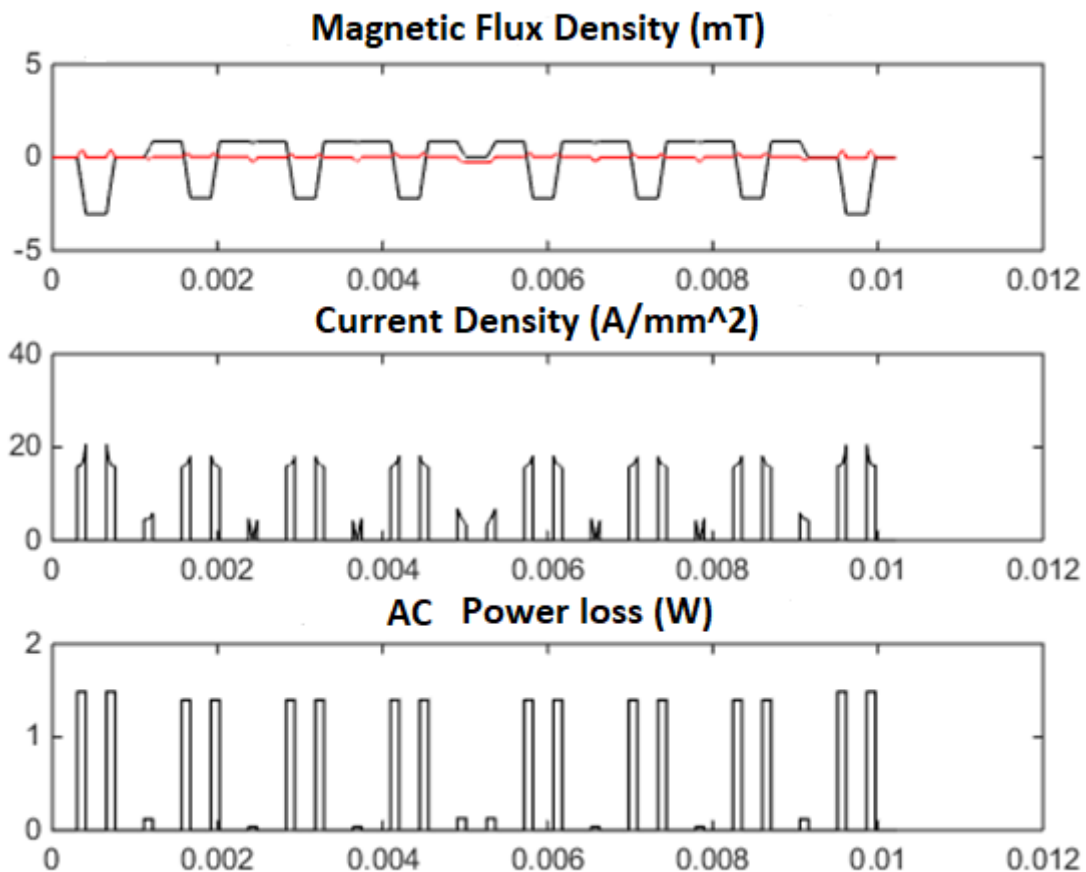


Figure 4-20: Magnetic flux, current density and power loss obtained for OBC standalone mode (6.5kW).

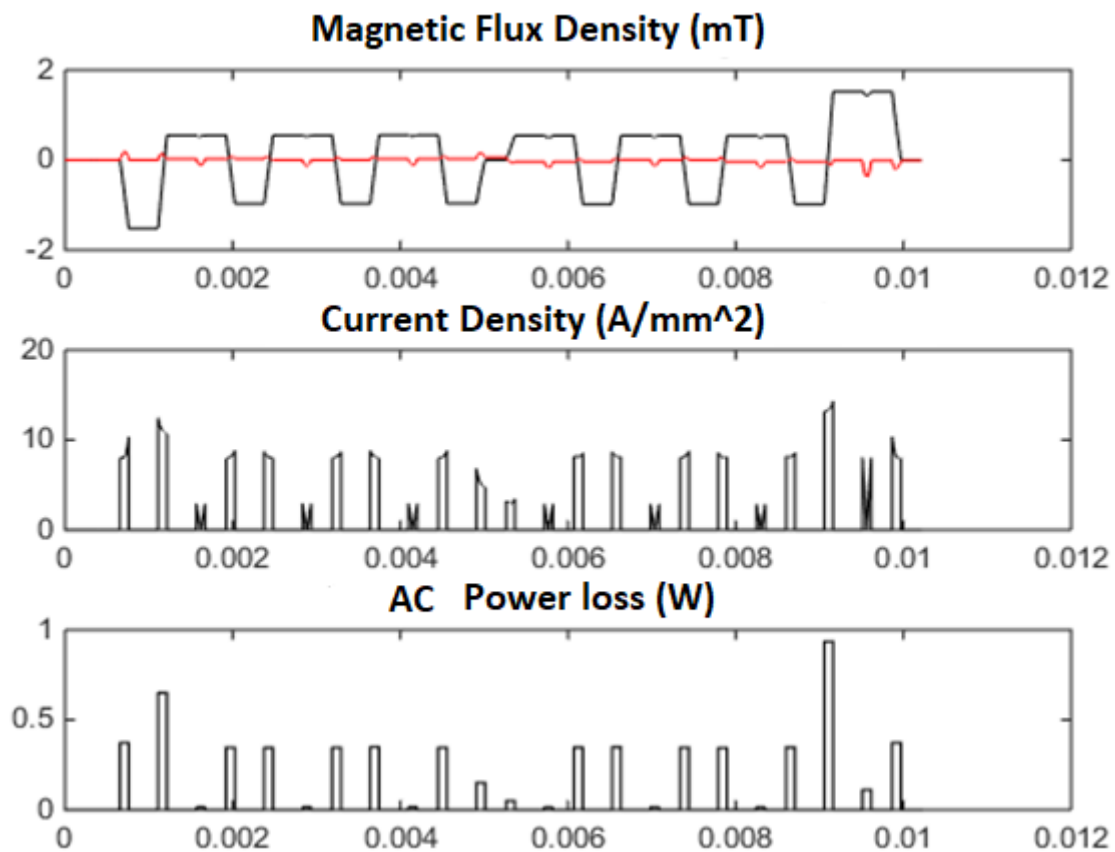


Figure 4-21: Magnetic flux, current density and power loss obtained for LDC standalone mode (3.5 kW).

Mode	Copper loss (W)	Core loss (W)	Total loss (W)
OBC	62.52	29.56	92.08
LDC	17.25	24.56	41.81
OBC + LDC	49.17	29.56	78.73

Table 4-6: Total power loss obtained in the transformer under maximum power flow conditions for each mode.

4.3.1- Transformer prototype and dielectric tests

Planar transformers are attractive because they can be integrated on the same PCB used for the other components in the main power board. The use of multilayer PCB's represents an increase in the real cost, but this cost can be significantly reduced depending on the number of units. The association of PCB's with only two or four layers is also a viable option; it allows the utilization of other insulating materials, with better thermal properties, for example, or with reduced electrical permittivity.

The transformer for the three-port current-fed converter presented in this thesis was built with an association of 3 PCB's. Each PCB separated into 8 layers with a total thickness of 3.2 mm. We suggest a maximum of 3 PCBs to limit the difficulty during the assembling process and to offer some resistance to mechanical stresses. Thinner PCB's were not possible because of the required insulating

distances between layers and the high number of turns. The PCB's stack up is not the same, but the two external PCB's are identical. The minimum insulating thickness is represented in Figure 4-22. If the total thickness does not ultra passes 3.2 mm, most of the manufacturers can respect the dielectric levels that we need.

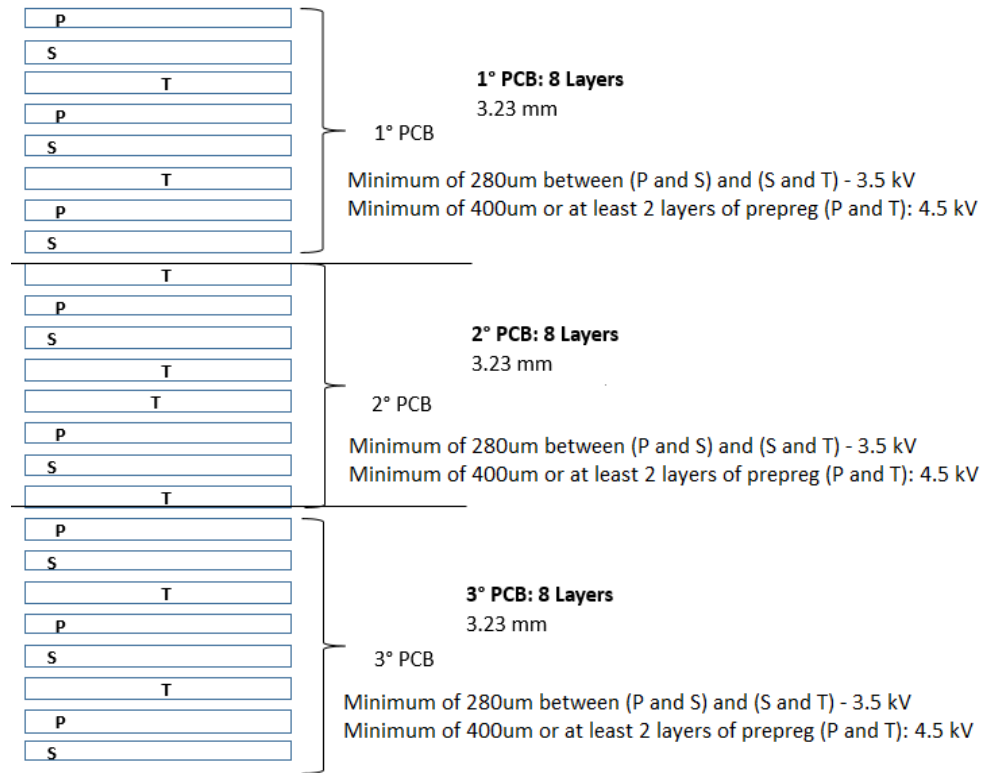


Figure 4-22: The PCB's final assembling and insulating thickness of fiberglass prepared material.

For the PCBs assembling, a dielectric material with good thermal properties is necessary. Mica is a well-known material, but in foil format, it does not support mechanical stresses and can be easily broken during manipulation because of the small foil thickness. Silicone with fiberglass is also an option or materials such as a thermal interface material containing adhesive surfaces. To connect the transformer to the main power boards, and despite the additional leakage inductance and DC resistance, extra wiring length was necessary. The final prototype is presented in Figure 4-23.



Figure 4-23: Transformer prototype.

The insulation requirements described in Figure 4-11 were tested in the prototype, Figure 4-24. The test consists of applying a sinusoidal voltage for 60 seconds with the voltage peak representing the

category. According to the standards IEC 61851-1 and IEC 60950, the integrated charger is in Category II, classified in 1500 V overvoltage. Therefore, the clearance and creepage distances, in air and along surfaces, respectively, as illustrated in Figure 4-25, must be used in the design to ensure good performance during the dielectric tests.

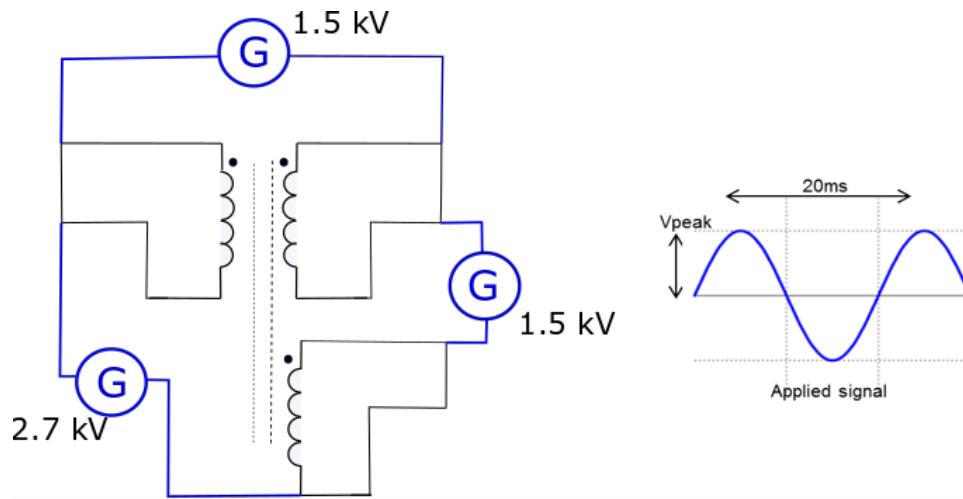


Figure 4-24: Dielectric tests between the windings to verify the insulating levels.

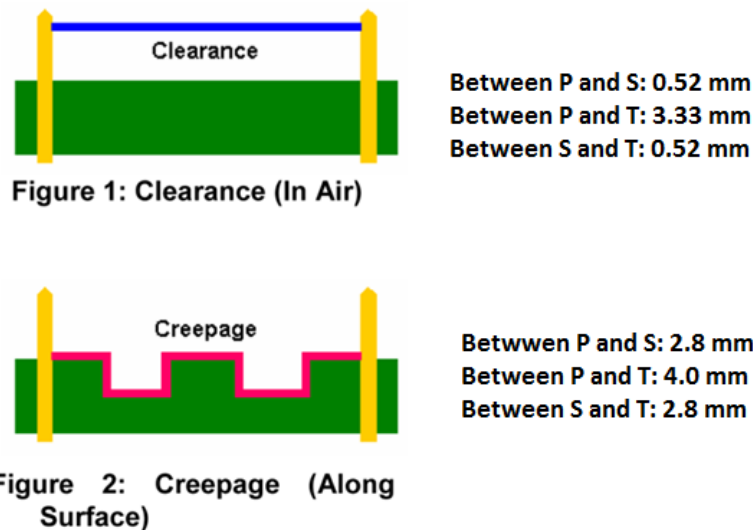


Figure 4-25: Clearance and creepage distances between conductive parts inside the transformer.

Because of the complexity in the assembling process, we had divided the tests into three phases: In the first one we validate the internal connections of each PCB; in the second phase we test the three PCB's together to verify the external dielectric layers; in the last one, we add the magnetic core. The two first phases were succeeded without failures for 2 in 3 prototypes. The last test presented a failure between phases P and T after 41 seconds, and to solve this problem, it was necessary to add an extra layer of insulating material between the PCB and the magnetic core. This solution, however, has an impact on heat dissipation.



Figure 4-26: The test bench used during the tests.

Despite the efforts to design an industrial product, the integrated planar transformer still needs to be improved in this application. The third proposed interleaved arrangement in Figure 4-12, allows keeping the distances indicated in Figure 4-25.

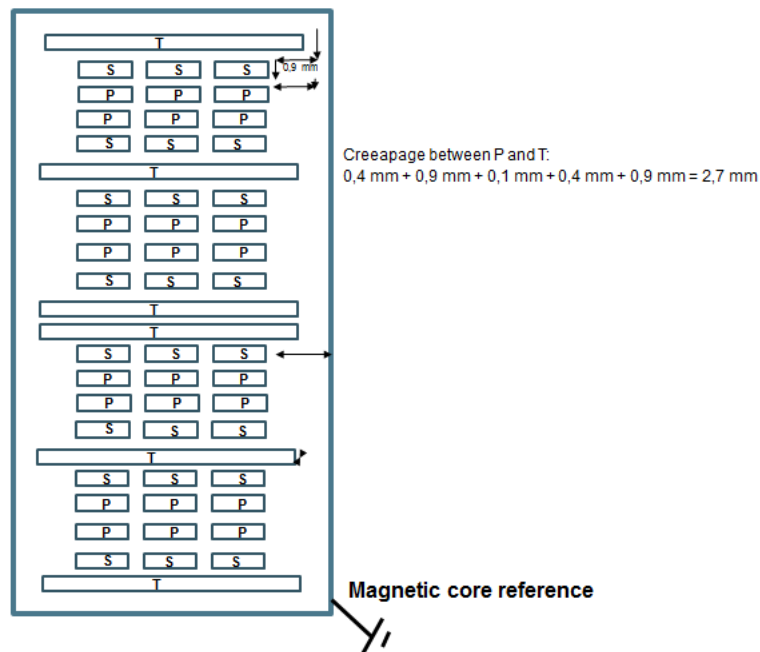


Figure 4-27: Transformer arrangement to respect the insulation requirements between the sources.

4.4- Thermal analysis

The design developed for the transformer and the study made considering high-frequency effects, allows a better current distribution among parallel-connected conductors for the two operating modes. However, this approach does not ensure uniform temperature among the PCB layers because of the prepreg thermal properties and the stack containing 24 layers; thus a thermal analysis becomes necessary to ensure heat dissipation.

Because the planar structure has a larger dissipation area, before studying a 2D simplified model among the stack up, the analysis of temperature over a single PCB layer is considered first, Figure 4-28. In FEMM software, heat flow analysis estimates the temperature elevation during the steady-state. To do so, the copper track was created with InkScape® and the .dxf file imported to the FEMM environment. The boundary conditions between air and simulated elements were settled as periodic (Dirichlet conditions) and temperature of air fixed at 42°C. Considering first that only the magnetic core is in contact with the aluminum base plate, fixed temperature in the ferrite can be used to estimate the maximum temperature difference between copper tracks and FR4. Constant heat flow is attributed to the copper track.

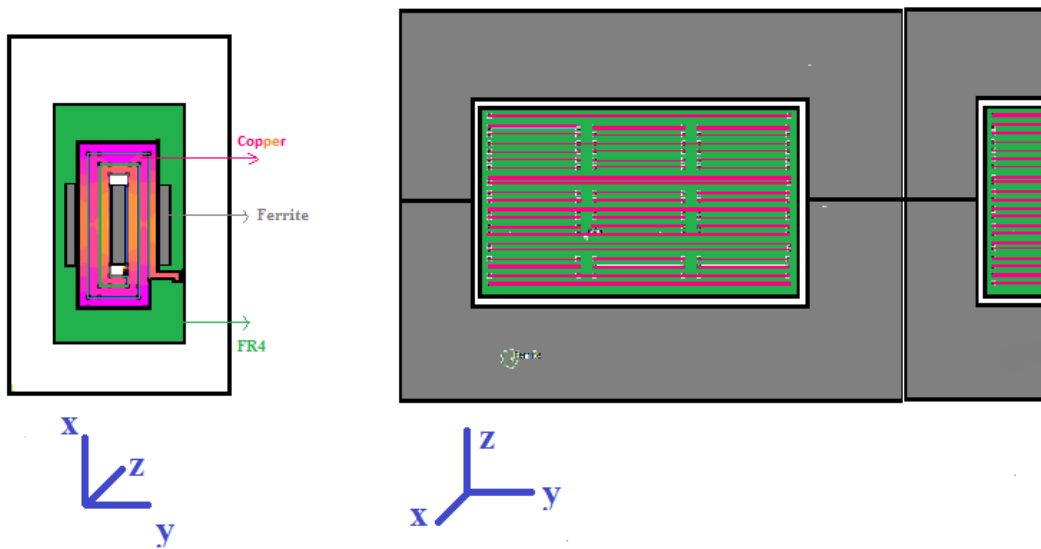


Figure 4-28: 2D simplification to study the temperature gradient in a single layer and among the stack of 24 layers.

Figure 4-29-(a) shows the results when the ferrite temperature is 50°C. The temperature difference between PCB and copper track is accentuated, close to 70°C. In Figure 4-29-(b), the ferrite temperature is fixed at 100°C, and the temperature difference between PCB and copper track is approximately 45°C. Table 4-7 contains the material thermal properties used in this simulation. Due to the different material thermal coefficients, an approximation for heat flow in the vertical direction of the transformer stack may introduce errors in the result because it cannot include all the necessary heat dissipation mechanisms.

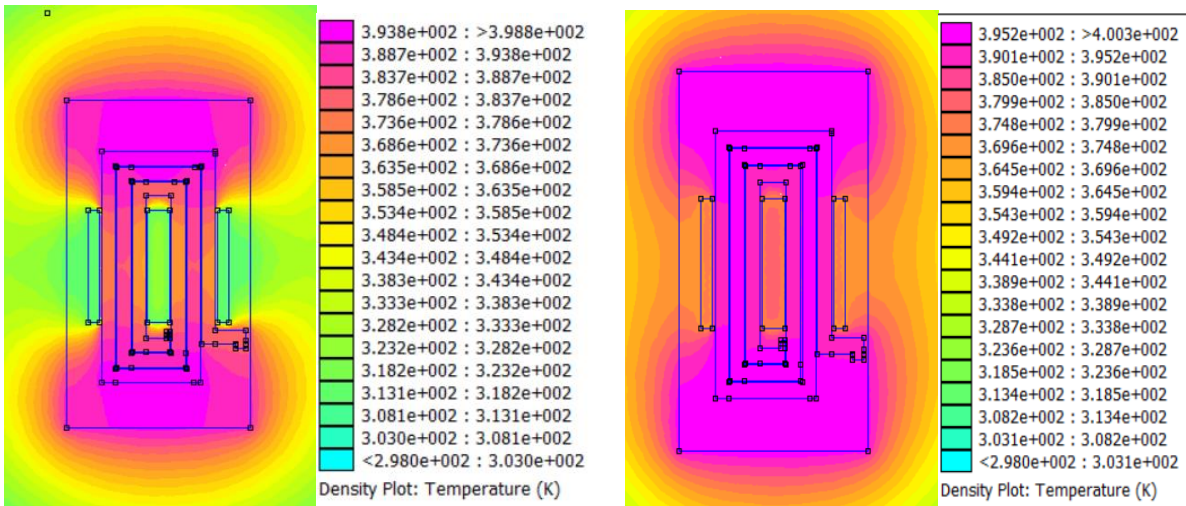


Figure 4-29: Temperature profile at steady state for Ferrite at a fixed temperature (a) 50°C b) 100°C.

	Copper winding (122mm/105 μ m)	FR4	Air	3C96
Mass density (Kg/m ³)	890	1850	1.225	4700
Thermal cond (W/mK)	390	2.25	1	4.47
Specific Heat (J/Kg K)	390	2.9	0.716	800
Heat Generation (W/m ³)	3.53 x 10 ⁶	0	0	3.76x10 ⁶

Table 4-7: Material thermal properties used in the 2D-FEM simulation.

A finite element analysis considering a 3D thermal model can be used to determine the temperature increasing in the transformer. As the power dissipated by each conductor layer was calculated previously considering the frequency influence in the current distribution among parallel conductors, the generated power loss can be applied as individual heat sources in each conductor layer. Due to the computational cost of this study and the complexity of generating the mesh between different material interfaces, we based the thermal study on an experimental approximation in the next section.

4.4.1- Empirical thermal evaluation for power loss dissipation

The thermal model used in this section estimates heat exchange with the environment and is based on empirical results presented in [5]. In the proposed analysis, conduction heat transfer is not considered, and only radiation and convection are the mechanisms responsible for the heat exchange. The tests are made considering transformer structures connected by thin electrical connections, placed on a printed circuit board and isolated from the rest of the power board to disregard the conduction heat transfer. Only magnetic cores and winding parts are evaluated.

Different structure sizes and shapes, including lengths between 1.5 cm and 15 cm (volume superior of 2 cm³), are verified in [5]. It also includes three types of magnetic material: ferrite, powder core, and ferrosilicon. The results show a uniform temperature on the winding part, allowing us to consider a single block mass exchanging heat with the environment. At first, a DC current is used to generate

power losses only on the windings. If voltage and current are measured, the electrical resistance depending on temperature can be obtained, and the gradient between the FR4 and copper can be determined:

$$R_{Winding} = R_{DC} [1 + 0.0037 (T - \theta_{amb})] \quad (13)$$

The thermal model proposed in [5] is presented in Figure 4-30. The total power loss generated by the magnetic core, and the winding, P_F and P_C , is dissipated by their surfaces. The heats transferred from the magnetic core surface to the environment, P_{EF} , and from the winding copper area to the environment, P_{EC} , are exchanged through thermal resistances R_{thF} and R_{thC} , respectively. These thermal resistances are not constant because of radiation, interfering a long time after achieving the steady-state. A thermal resistance between the magnetic core and the winding part is also used to represent the temperature difference between both parts. The power dissipated by the magnetic and conductive parts is proportional to their total surfaces in contact with air.

$$P_C + P_F = P_{EC} + P_{EF} \quad (14) \quad R_{th_{CF}} = \frac{\theta_C - \theta_F}{P_{CF}} \quad (15)$$

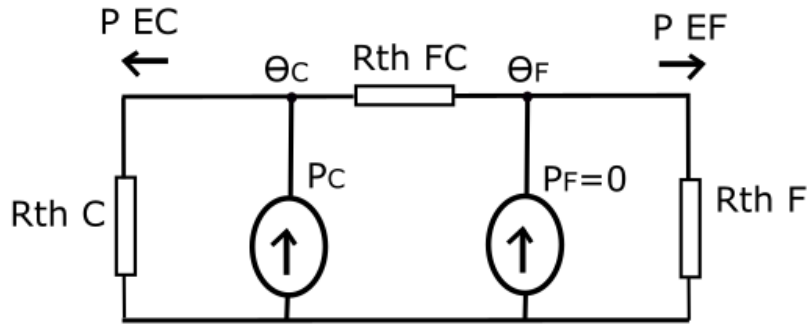


Figure 4-30: Thermal model at steady-state proposed in [5].

The idea is to use this same model developed for conventional magnetic formats for the planar structure. Therefore, a first test consists of measuring the temperature elevation in the transformer winding without the magnetic core for different DC currents to evaluate the heat-exchange capacity of the winding in the PCB. The results obtained in [5] show that the dissipated power losses, temperature variation, $\Delta\theta$, and surface area in contact with the air are related by:

$$Loss (W) = \delta Area + 20 \delta \left(1 + e^{-\frac{Area}{11}}\right) \quad Area \text{ in } (cm^2) - \text{winding area} \quad (16)$$

$$\delta = 114 \times 10^{-3} \Delta\theta + 1.5 \times 10^{-10} \Delta\theta^4 \quad \Delta\theta \text{ in } (^\circ C) \quad (17)$$

The second test consists in to verify the influence of the magnetic core in the heat dissipation mechanism. A DC current is still applied to generate the losses, and we determine the heat dissipated by the magnetic core and by the winding surface. Using expressions (14) and (15), we have:

$$P_C = P_{EC} + P_{EF} - P_F, \quad P_F = 0$$

$$Rth_{CF} = \frac{\theta_c - \theta_f}{P_{CF}} = \frac{\theta_c - \theta_f}{P_{EF} - P_F} = \frac{Area \times (\theta_c - \theta_f)}{Loss(Area, \Delta\theta) \times S_{Ferrite}}$$

$$P_{EF} = \frac{Loss(Area, \Delta\theta) \times S_{Ferrite}}{Area} \quad (18)$$

The heat transferred between the winding and magnetic core, P_{CF} , is transferred through Rth_{CF} . This resistance depends on the distance between the PCB and the magnetic core, and the thermal conductivity of the material filling this region.

Considering that, the temperatures in the PCB and magnetic core are different, $\Theta_F \neq \Theta_C$, the heat transferred between winding and magnetic core is different from zero. The total heat dissipated by the surface of the magnetic core, Rth_F , gives the temperature variation $\Delta\Theta_F$ and is precisely the same heat transferred through Rth_{CF} .

$$P_{EC} = \frac{Loss(Area, \Delta\theta) \times S_{Wind}}{Area} \quad (19)$$

$$P_C = P_{EC} + P_{CF} \quad (20) \quad P_F = P_{EF} - P_{CF} \quad (21)$$

At first, we evaluate only the PCB without the magnetic core by applying a DC current in one of the windings. The voltage drop in the winding and the temperature are measured by thermocouples at two different points on the PCB exposed area, as shown in Figure 4-31-a. During the tests, the two high voltage side windings are connected in series, and we obtain the internal winding temperature through the resistance variation while applying a DC current of 6.5 A.

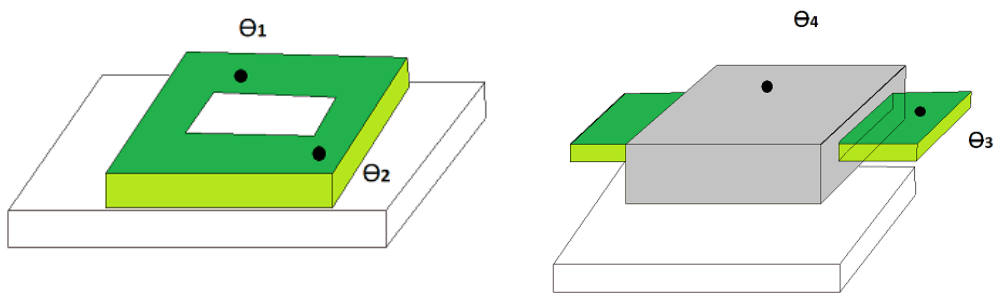


Figure 4-31: Temperature evaluation during the tests in the PCB part with and without the magnetic core. a) 1° test, PCB only. b) 2° test.

In the second test, we keep the same conditions, but now the magnetic core and PCB are evaluated together. The temperature is measured in two points, in the PCB and the magnetic core, as indicated in Figure 4-31-b. The temperature variation inside the copper winding is presented in Table 4-8.

	Point	T (°C)	ΔV (V)	$R_{dc1} + R_{dc2}$ (m Ω)	T_{max} inside the wind. (°C)	Power loss (W)
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1° Conf.	θ_1	99.3	3.42	523	99	22.1
	θ_2	96.0				
2° Conf.	θ_3	103	3.51	538	107	22.8
	θ_4	96.4				

Table 4-8: Temperature estimation inside the winding obtained with the thermal coefficients and the measured resistance. $\theta_{amb} = 22^\circ\text{C}$.

Using the empirical model, the surface areas of each element, and the common surface between the winding and magnetic core, we can estimate the maximum dissipated loss in the magnetic core and winding individual parts, as presented in Table 4-9.

$\Delta\theta_3$ (°C)	$\Delta\theta_4$ (°C)	$\Delta\theta_{1/2}$ (°C)	P (W) (From 1° test) (16) - (17)	Total area S (cm ²)	S_{Wind}/S	$S_{Ferrite}/S$	Common area (cm ²) $S_{Wind} \cap S_{Ferrite}$	P_{EC} (W)	P_{EF} (W)
81	74.4	77.3	22.6 W	218	0.61	0.39	53.23	13.79	8.81

Table 4-9: Temperature evaluation in the PCB and in the magnetic core. $\Delta\theta_x = \theta_x - \theta_{amb}$, P is the total power loss dissipated by the winding part, P_{EC} , P_{EF} are the power losses dissipated by the PCB and magnetic core, respectively. $P = P_{EC} \times S_{Wind}/S + P_{EF} \times S_{Ferrite}/S$.

The power loss dissipated by each transformer part is proportional to their areas in contact with air. As can be noted from the results, with 44% of the nominal DC current value in the transformer, the temperature achieved in the PCB is close to 100 °C. Thus, a cooling solution to evacuate power loss is necessary.

In the two first tests, the transformer was placed over a table made of wood, which is a material with low thermal conductivity. In reality, the transformer uses to be in contact with the casing of the converter made of aluminum. In order to approach the results from the real situation, the third test places the transformer over an aluminum base plate. The temperature measured is presented in Table 4-10, and the acquisition points are indicated in Figure 4-32-a. With the base plate, the heat dissipating capacity of the structure was increased, and the current to 52% of its nominal value, reaching a temperature of 100° C at the external surface, estimated at 107 °C in the copper winding.

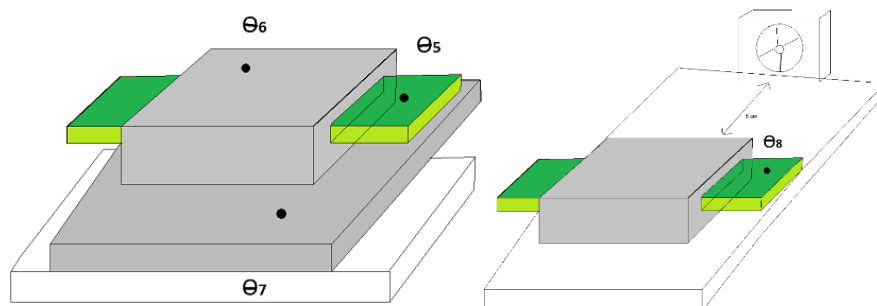


Figure 4-32: Temperature evaluation in the planar transformer. a) Placed on aluminum base plate b) cooled by a small ventilator placed 5 cm away.

	Point	T (°C)	Idc (A)	Voltage drop (V)	R _{dc1} +R _{dc2} (mΩ)	T _{max} inside the wind. (°C)	Power loss (W)
3° Conf. (Al. base plate)	θ ₅	78.6	6.5	3.3	507.7	90.0	21.4
	θ ₆	66.3					
	θ ₇	50.8					
	θ ₅	99.8	7.5	4.0	533	106.5	29.9
	θ ₆	81.9					
	θ ₇	61.2					
4° Conf. (Ventilator)	θ ₈	63.4	8.33	4.0	480	72.0	33.3
	θ ₈	85.1	10.0	5.3	530	104.6	53.0

Table 4-10: Temperature estimation inside the winding obtained with the thermal coefficients and the measured resistance.

In a fourth test configuration, to increase the transformer's heat dissipation capacity, a small ventilator is located 5 cm away from the prototype. If a forced air-cooling solution can dissipate the heat generated in the transformer, the physical implementation remains coherent with the solution proposed for the main power board. The temperature is verified in the PCB exposed area, as shown in Figure 4-32-b. Using the information obtained with experimental tests and the equivalent thermal model proposed in Figure 4-30, we estimate the thermal resistances. The obtained thermal resistances are presented in Table 4-11 for two cases, the transformer with only the PCB plus magnetic core, and with an additional ventilator.

Configuration	Total Loss (W)	P _{EC} (W)	P _{EF} (W)	R _{thC} (°C/W)	R _{thF} (°C/W)	R _{thCF} (°C/W)
Transf.	22.8	13.9	8.89	5.82	8.37	0.74
Transf. + Ventilator	53	32.3	20.7	1.95	2.41	0.63

Table 4-11: Thermal resistances obtained to describe the cooling of the prototype.

The model was obtained for measurement results while applying a DC current, but in practice, the current is a square waveform containing odd harmonics. However, if the current is well distributed between the layers, this simplification remains acceptable. The equivalent model also allows estimating the final temperature with additional power loss from the magnetic core, estimated with Steinmetz equation, $P_F \neq 0$.

Mode	Copper loss (W)	Core loss (W)	θ _C (°C)	θ _F (°C)
OBC	62.52	29.56	142.1	135.7
LDC	17.25	24.56	83.6	86.4
OBC + LDC	49.17	29.56	126.2	123.1

Table 4-12: Temperature estimation using the equivalent thermal model from Figure 4.30 for the three converter operation modes. The thermal resistances are considered with the additional fan placed 5 cm away from the transformer. $\theta_{amb} = 40\text{ }^{\circ}\text{C}$.

The results show a temperature of $142\text{ }^{\circ}\text{C}$ in the conductive parts for nominal current in the OBC operating mode. The maximum temperature reached in the PCB can be $150\text{ }^{\circ}\text{C}$.

The thermal coefficients of the PCB and ferrite found with the experimental results can now be used to formulate the boundary conditions for a simulation with finite elements using the PCB stacks, as shown in Figure 4-33, for example. In each conductor track, we apply the heat sources corresponding to the frequency-dependent calculated power loss.

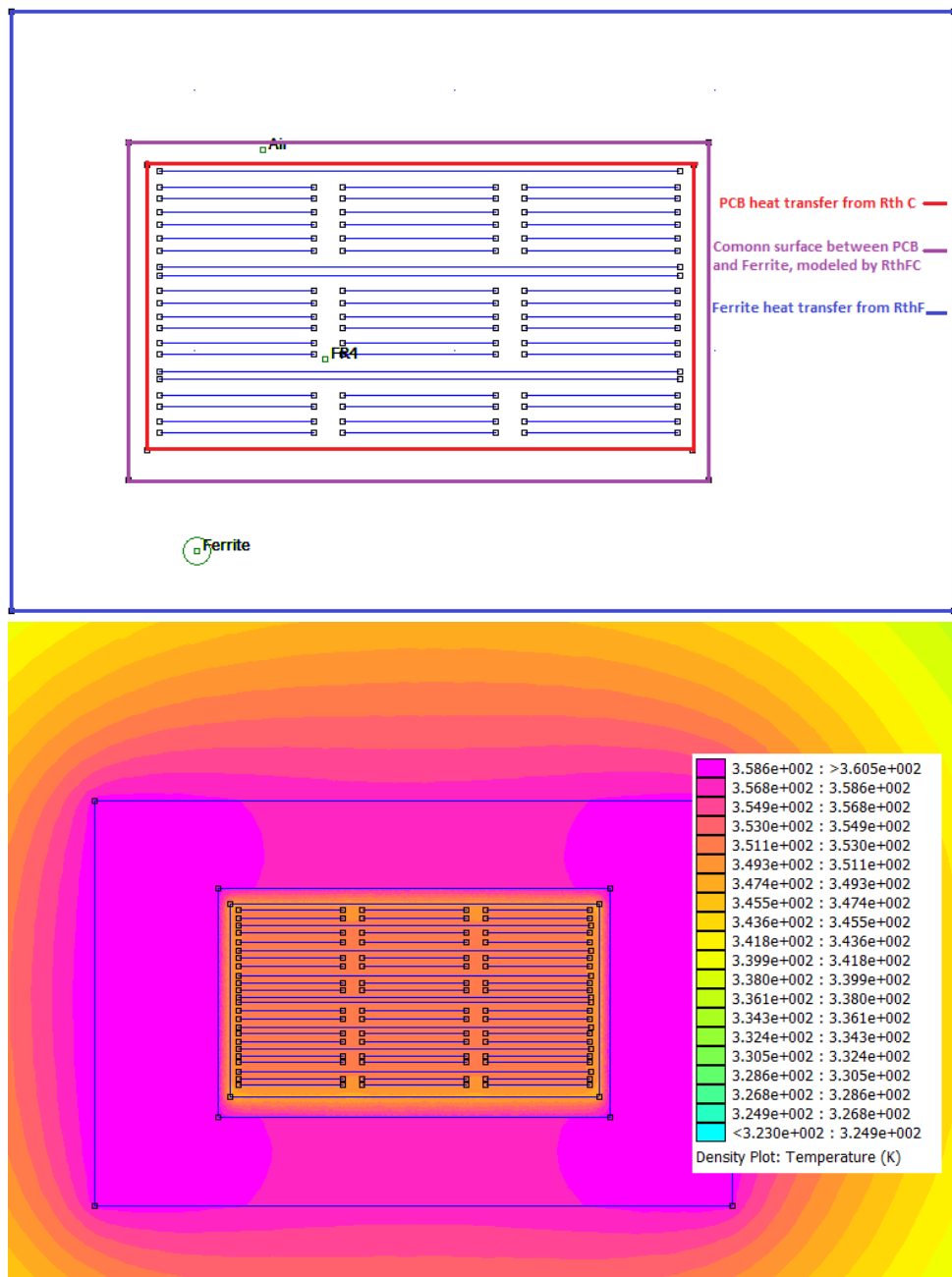


Figure 4-33: a) Boundary conditions and copper tracks containing heat sources equal to the equivalent power losses for OBC+LDC mode depending on frequency (250 kHz) b) Temperature at steady-steady.

Once a thermal model has been proposed, the next step consists in verifying temperature variation for real operating conditions, by applying an AC square current provided by the Current-fed parallel resonant converter.

The transformer was placed on an aluminum base plate, but without any cooling system, and the current was increased to 6.5A RMS value. The temperature acquisition was made by two thermocouples placed on the exposed area in the ferrite and PCB. The results are shown in Figure 4-34 and Figure 4-35 for currents of 4A_{RMS} and 6.5A_{RMS}, respectively.

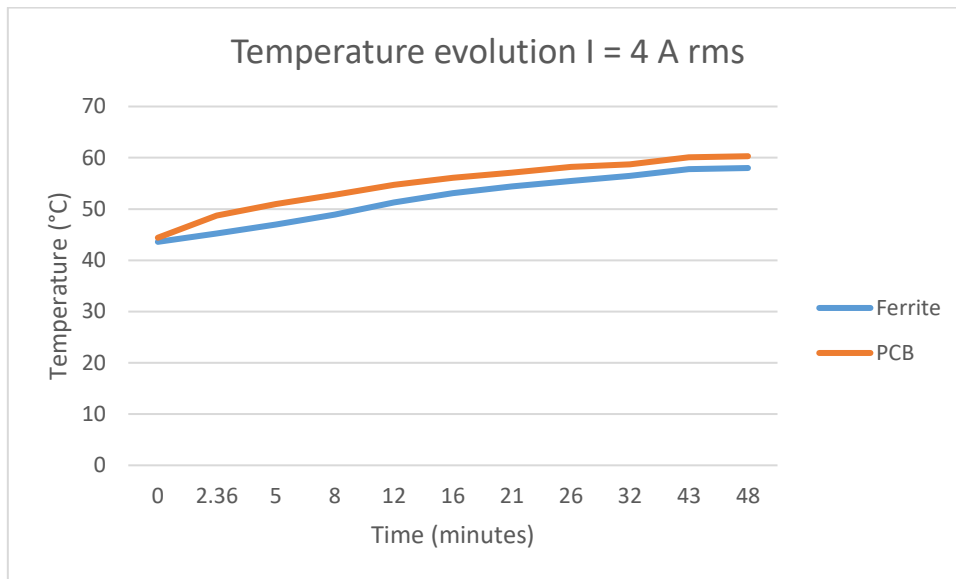


Figure 4-34: Temperature in PCB and magnetic core for square current waveform of 4 Arms. (Using high voltage sides only).

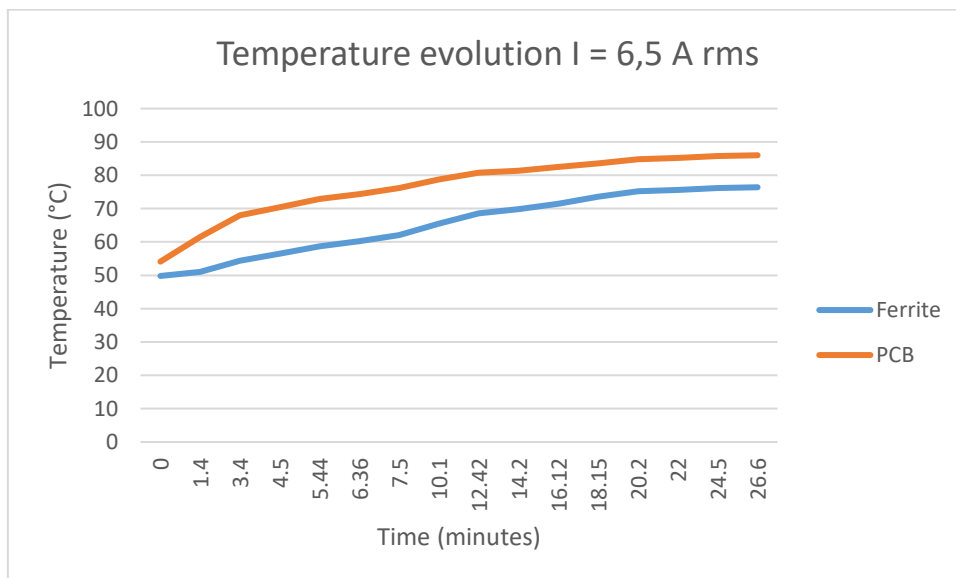


Figure 4-35: Temperature in PCB and magnetic core for square current waveform of 6.5 Arms (Using high voltage sides only).

Later, a mechanical part was fabricated not only to keep both magnetic core parts together but also to dissipate part of the generated heat. A photo is presented in Figure 4-36. An aluminum base plate with 33.8 mm^2 was extruded with the dimensions of half of the magnetic core. It allows the ferrite's surface to be in contact with the cold plate through a gap filler. The superior support is in contact with the ferrite's topside, while two screws ensure the mechanical attachment. An axial fan is placed in the vertical to flow the air through the finned part and the heat generated on the PCB.

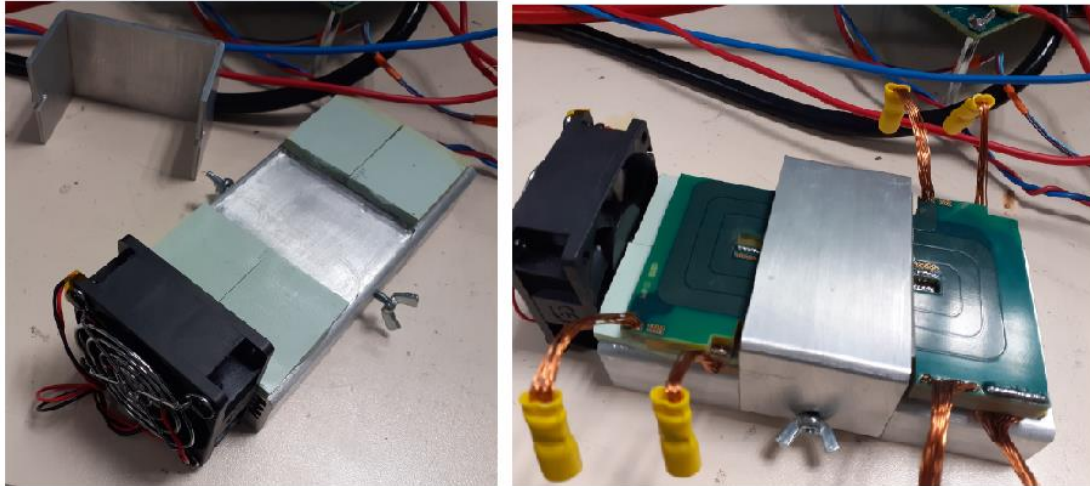


Figure 4-36: Thermal solution proposed for the transformer.

4.5- An equivalent model to include parasitic elements in the converter behavior

In this section, we discuss how to estimate an equivalent model for the three-winding planar transformer considering high-frequency effects.

The use of an equivalent network containing magnetic flux linkages and current sources between windings to represent a multi-port magnetic component is usually applied to determine an equivalent inductance matrix. In those representations, different tests under open and short-circuit conditions are necessary to estimate an inductance matrix considering the influence of individual ports by steps. Negative values can also be derived sometimes to keep a mathematical coherence, but without physical meaning. An equivalent circuit containing mutually coupled inductances for a three-winding transformer is proposed in [7] without any negative element, using information about the leakage flux path to determine leakage inductances. In [8], the same principle of mutually coupled inductances was adapted for multi-winding transformers, but the physical meaning of elements is not directly related to eddy current effects.

In the case of the planar transformer presented in this thesis, mutually coupled inductances may not be useful mainly because of the increased magnetizing inductance. However, an equivalent circuit for multi-winding transformers able to represent eddy current effects considering parallel-sharing current may be interesting.

Therefore, we start the analysis using the Ampère and Faraday laws to formulate the electromagnetic problem into a 2D representation, as has been made in section 4.3. By using equations (8), (9), (10) and (11), we can represent the voltage over a single conductor linearly dependent on the current in all other layers, taking into consideration series and parallel connections between conductor sections. The equations system is valid if the circuit operates far away from the saturation zone, justifying the Superposition's theorem application to relate voltage and current in each winding present in the transformer:

$$\left\{ \begin{array}{l} v_1 = \alpha_{11} \cdot i_1 + \alpha_{12} \cdot i_2 + \dots + \alpha_{1N} \cdot i_N \\ v_2 = \alpha_{21} \cdot i_1 + \alpha_{22} \cdot i_2 + \dots + \alpha_{2N} \cdot i_N \\ \dots \\ v_N = \alpha_{N1} \cdot i_1 + \alpha_{N2} \cdot i_2 + \dots + \alpha_{NN} \cdot i_N \end{array} \right. \quad (20)$$

$$\left\{ \begin{array}{l} i_1 = \beta_{11} \cdot v_1 + \beta_{12} \cdot v_2 + \dots + \beta_{1N} \cdot v_N \\ i_2 = \beta_{21} \cdot v_1 + \beta_{22} \cdot v_2 + \dots + \beta_{2N} \cdot v_N \\ \dots \\ i_N = \beta_{N1} \cdot v_1 + \beta_{N2} \cdot v_2 + \dots + \beta_{NN} \cdot v_N \end{array} \right. \quad (21)$$

Both systems (20) and (21) are equivalents and represent the physical behavior of a multi-winding transformer as in the conventional representation. However, the system solution is derived from equations depending on frequency, and coefficients α_{ij} and β_{ij} . These are complex coefficients considering the frequency influence, like skin and proximity effects, including also the problem of current repartition in parallel-connected conductor plates.

Remembering that these two effects were studied under a sinusoidal regime, coefficients β_{MN} and β_{NM} are the same, such as for coefficients α_{MN} and α_{NM} , because of the reciprocity principle. This affirmation can be analytically proved by taking two conductors layers in Figure 4-6 and changing the order between input and output. We verify that the expressions used to calculate the coefficients relating to voltage and current are the same. Despite skin and proximity effects, this property is maintained, and the existence of only passive and linear components allows the use of the superposition theorem.

If a single winding is supplied by a current and the others are left open, the magnetic field strength containing real and imaginary parts passing through the magnetic circuit, inside and outside conductor plates, generates at each transformer winding two orthogonal components. As the total imaginary current is zero inside a winding, the voltage drop is due to the real part, and it cannot be neglected when the frequency starts to increase.

To obtain a circuit representation that is closer to the general circuits presented in the literature, we add the transformer turn's ratio definition. As in [9], to refer voltage, current, and elements between the windings, ratios can be chosen arbitrarily. Nevertheless, to obtain a model the closest as possible to practical values, the ratios are used as the output voltage gains. We use the first winding as the reference, and remain all the elements to the primary side:

$$\left\{ \begin{array}{l} v_1 = z_{11} \cdot i_1 + z_{12} \cdot i'_2 + \dots + z_{1N} \cdot i'_N \\ v'_2 = z_{21} \cdot i_1 + z_{22} \cdot i'_2 + \dots + z_{2N} \cdot i'_N \\ \dots \\ v'_N = z_{N1} \cdot i_1 + z_{N2} \cdot i'_2 + \dots + z_{NN} \cdot i'_N \end{array} \right. \quad (22)$$

$$\left\{ \begin{array}{l} i_1 = y_{11} \cdot v_1 + y_{12} \cdot v'_2 + \dots + y_{1N} \cdot v'_N \\ i'_2 = y_{21} \cdot v_1 + y_{22} \cdot v'_2 + \dots + y_{2N} \cdot v'_N \\ \dots \\ i'_N = y_{N1} \cdot v_1 + y_{N2} \cdot v'_2 + \dots + y_{NN} \cdot v'_N \end{array} \right. \quad (23)$$

$$v'_i = \frac{v_i}{m_{1i}} \quad i'_i = m_{1i} \cdot i_i \quad z_{ij} = \frac{\alpha_{ij}}{m_{1i} \cdot m_{1j}} \quad y_{ij} = m_{1i} \cdot m_{1j} \cdot \beta_{ij} \quad (24)$$

In both systems, there are N^2 coefficients Z_{ij} or Y_{ij} to describe the transformer behavior, but due to the reciprocity principle, the elements ij are equal to elements ji ; therefore there are only N_p parameters to describe the system:

$$N_p = \frac{N(N+1)}{2}, N \text{ is the } N^\circ \text{ of windings}$$

The circuit representing the system (22) must include at least the same number N_p of impedances connected to the ports, resulting in an additional self-impedance from each winding terminal connected to the ground reference, if capacitive effects are ignored. It leads to an equivalent circuit as the one represented in Figure 4-37. A series-connected resistance and inductance represent each impedance, but it could also be the parallel association of these elements.

The tests for the transformer characterization can now be considered. We use the impedance analysis under short and open circuit cases. In the first analysis, a single winding is power supplied by a current i_1 while the other windings are under short-circuit conditions. The other currents j_i ($i \neq j$) are measured or calculated in the short-circuited windings, and the voltage drop on the first one, v_j . We repeat the test in each one of the windings to write $(N-1)$ mutual impedances. As in literature, open-circuit tests are carried out also. While a single winding is connected to a voltage source, N relations exist between the voltages measured on the opened ports. We also repeat this test for each transformer winding, resulting in N_p equations ($N_p > N$).

Negative elements may appear because of the turns ratio between windings chosen as the voltage gains. Consider, for example, a small turn's ratio chosen to represent the voltage gain between primary and secondary sides in a two-winding transformer. To obtain an equivalent voltage measured on the secondary side during the open-circuit test higher than the value applied on the primary side, if the element Z_{12} is positive, according to (22), the self-impedance Z_{22} must be negative to make this happen. From a mathematical point of view, a negative element is coherent, but is not practical in simulations, neither in the correlation with real measurements.

Under open-circuit tests, the self-impedances, Z_{ij} ($i=j$), in Figure 4-37, can be parallel-combined into a single element, resulting in the representation from Figure 4-38. This rearrangement results in positive resistances and inductances to represent a single self-impedance. However, this approximation is only valid when leakage impedances can be neglected in comparison to magnetizing elements. This condition is frequently found in planar transformers and corresponds to the case treated in this thesis. On the numerical solution implemented in Matlab, this simplification corresponds in making the other self-impedances go to infinite, except the one used as the reference. If N_p parameters are required in the circuit representation, we replace $(N-1)$ impedances by $(N-1)$ transformer voltage ratios.

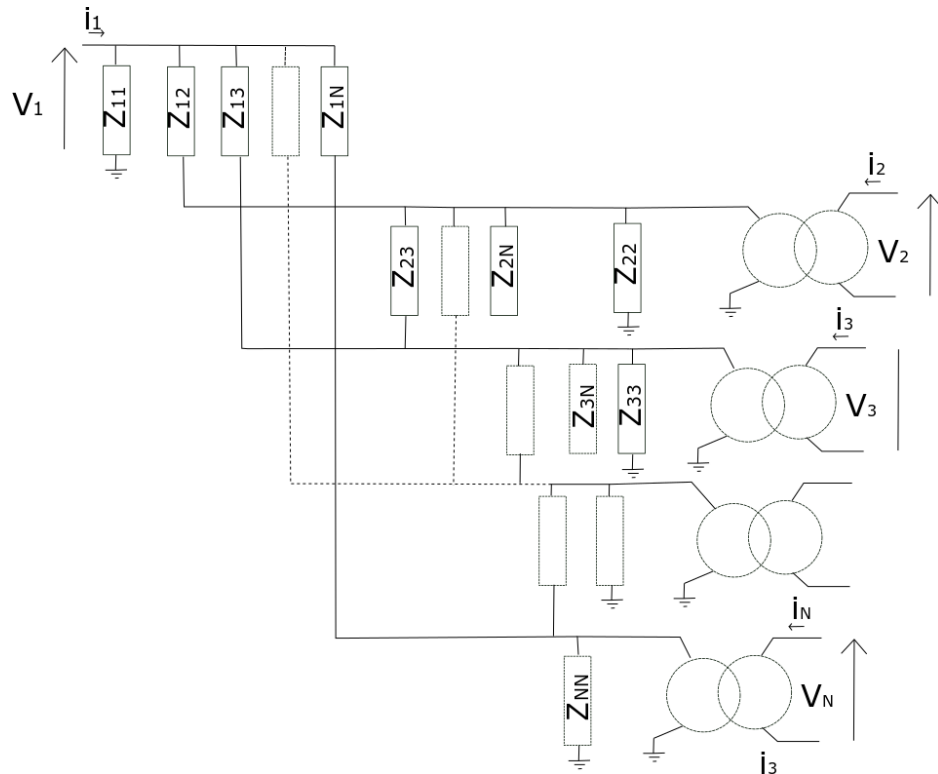


Figure 4-37: General equivalent circuit of a multi-winding transformer.

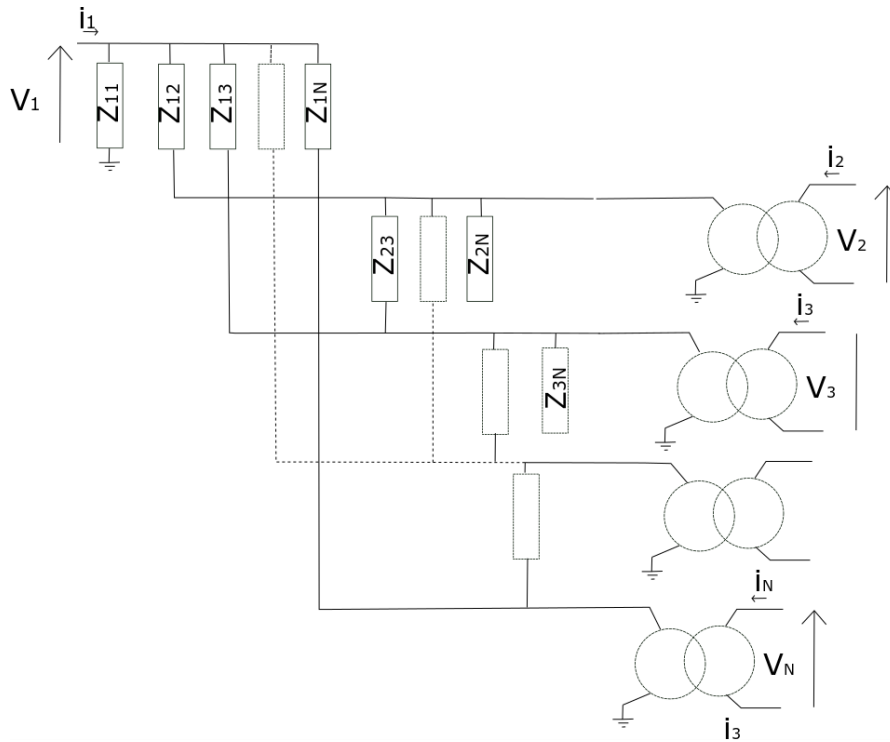


Figure 4-38: General circuit representation for a multi-winding transformer containing a single self-impedance.

The routine implemented in Matlab, in complement to the solution presented in section 4.3, determines the elements to represent the circuit in Figure 4-38 by solving the system of linear equations in (20), (21), or (22), (23), (24): resistances and inductances from leakage and magnetizing impedances, correction factors, and ratios between the ports. The last elements are real values, while the corrective factors are complex and are used to keep a single self-impedance.

4.5.1- Negative elements

The determination of models for planar transformer containing more than two windings using the description of conditions with Ampère and Faraday laws and implemented in the numerical solution may sometimes lead to negative values also for mutual inter-impedances, Z_{ij} ($i \neq j$). The correction factors introduced in the numerical solution are complex and may not have enough imaginary values to make the real part of these impedances positive. Negative values are a consequence of the short-circuit tests. While one of the windings is connected to a current source, the current induced in the short-circuited windings tends to cancel the induced magnetic flux variation, and nothing prevents the imaginary component of these induced currents from being negative, resulting therefore in impedances with opposite signals. Consider the following example: a three-winding planar transformer containing 3 series-connected turns in each winding, disposal in an interleaved arrangement in Figure 4-39.

At high-frequency, if the primary is connected to a voltage source, while the remained windings are short-circuited, the real part of the induced current in the second and third windings must result in a

negative value; still, the imaginary part can be positive or negative. By solving an example and using the considerations from section 4.3, we note that the imaginary current in the third winding is negative at 500 kHz, Figure 4-40.

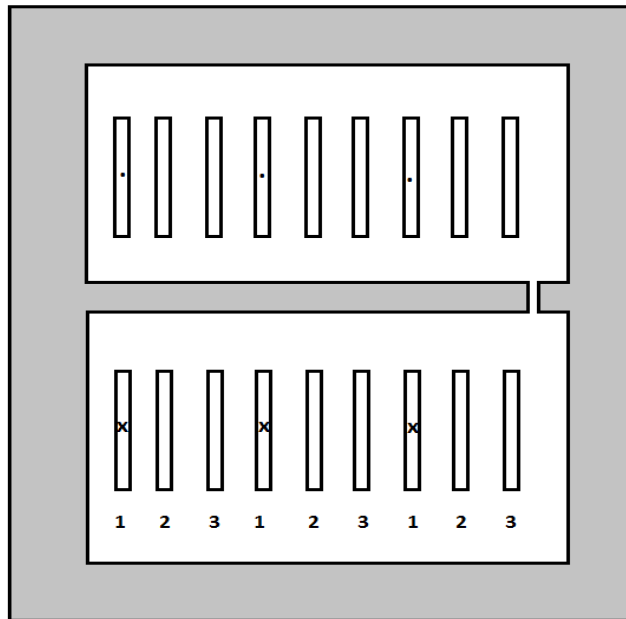


Figure 4-39: A 3-winding planar transformer used to exemplify the origin of negative impedances. 1=Primary side; 2=secondary side; 3=third side.

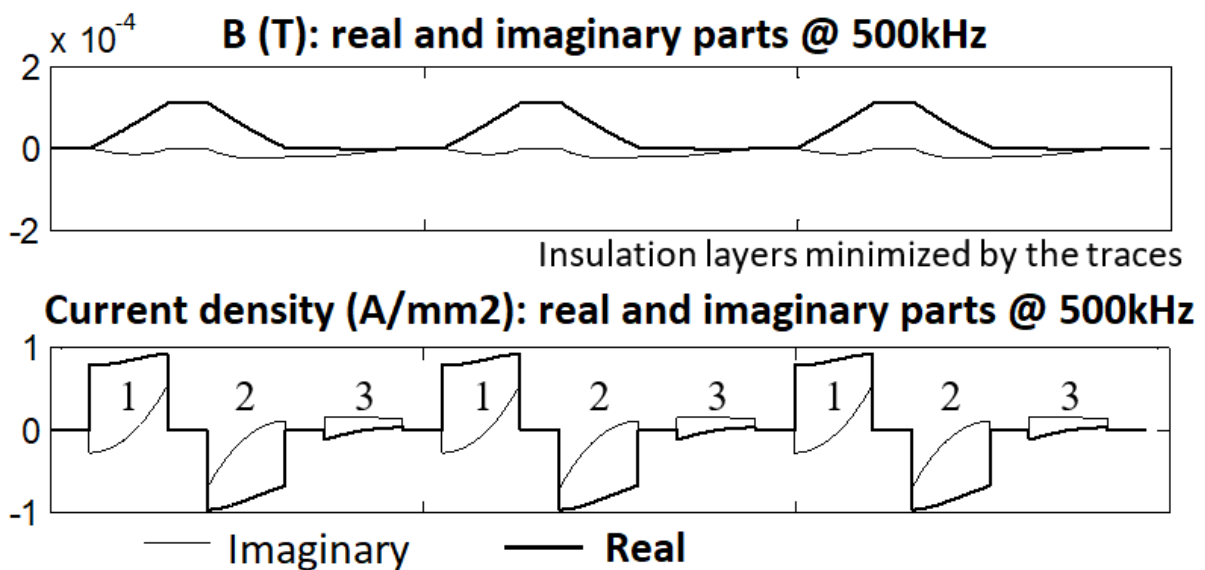


Figure 4-40: Magnetic flux and current density in each layer of a 3-winding planar transformer. 1=Primary side power supplied with a constant current; 2=secondary short-circuited side; 3=third short-circuited side. Copper thickness is considered at 105 μm and frequency at 500 kHz.

The current in the second winding contains real and imaginary parts that are negative, and its value is almost enough to make opposition to the magnetic flux variation of the first side. The negative real current on the third side helps cancel this flux variation, but, because of high-frequency effects, the real and imaginary parts have opposite signals in the third side, resulting in a negative inductance on

the impedance Z_{13} . This result is similar to the situation where the secondary and third windings behavior as a single winding, where each conductor plate has twice the section of the primary side conductor. In this situation, the magnetic flux passing through a larger conductor plate provokes the current circulation also in the reverse direction. Under low frequency, the negative element disappears when the imaginary and real parts have the same signal, and the current is equally distributed between both windings. The same example is now represented for a smaller frequency in Figure 4-41.

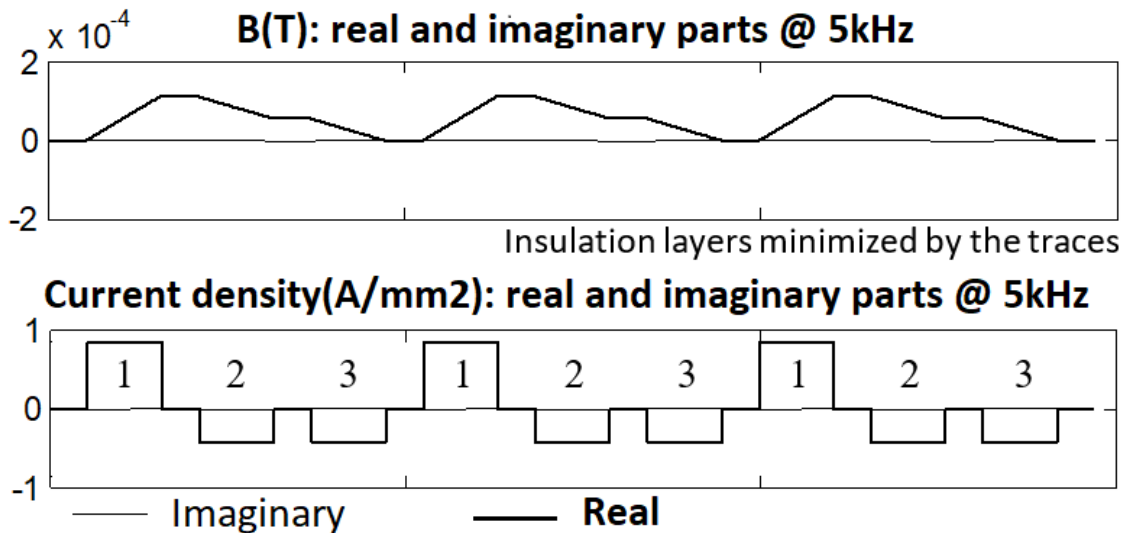


Figure 4-41: Magnetic flux and current density in each layer of a 3-winding planar transformer. 1=Primary side power supplied with a constant current; 2=secondary short-circuited side; 3=third short-circuited side. Copper thickness is considered at 105 μm and frequency at 5kHz.

The negative values are physically explained in an equivalent circuit if the operation frequency ultra-pass a determined range. This range depends on the physical characteristics of the magnetic circuit and the physical disposal of the layers. As negative values are not useful in a time-domain numerical simulator, we propose an equivalent model applied to a certain frequency range, before the negative values start to appear.

Therefore, the equivalent circuit elements can be imported into a time-dependent simulator to analyze instabilities, semiconductor commutations and include some parasitic elements in its operating frequency range. For that, a planar transformer containing more than two-windings can be represented without negative elements by the circuit in Figure 4-38 in a specific frequency range.

4.5.2- Equivalent model for the three-winding planar transformer

In this section, we determine the equivalent model for the transformer presented in the previous section. The winding arrangement is represented in Figure 4-42.

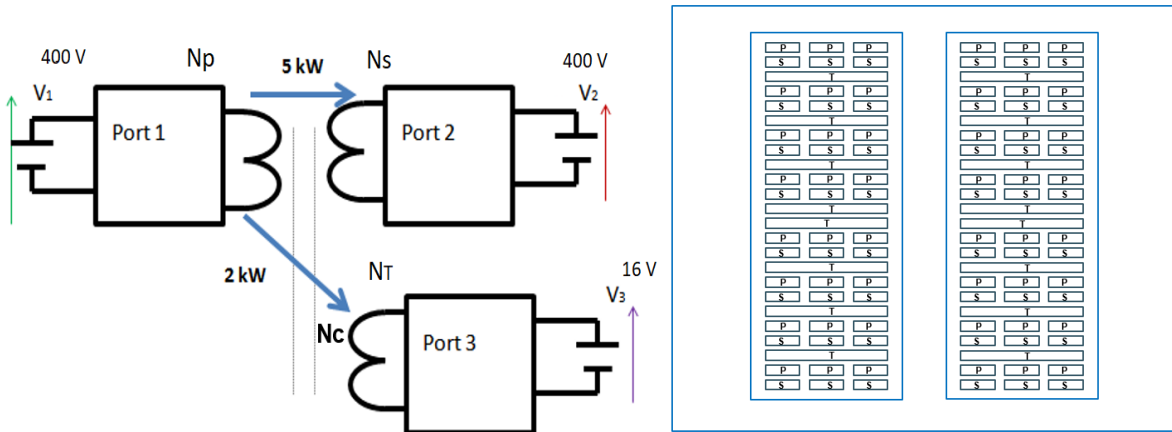


Figure 4-42: The three-winding planar transformer configuration. a) three-port converter representation b) copper layers layout placed inside the magnetic core. $N_P : N_S : N_T = 24 : 24 : 1$.

The same approach in section 4.3 is used to obtain the m.m.f, voltage, and current distribution among the transformer conductor plates. The electrical parameters are derived from short-circuit test conditions applied to each winding to determine the total current and equivalent voltage in the transformer windings. In Figure 4-43, we see the magnetic flux, current density, and power loss distributed among the PCB stacks while the primary side is connected to a voltage source at 250 kHz, and the other sides are short-circuited. Figure 4-44 presents, for the same conditions, the individual real and imaginary parts of these parameters.

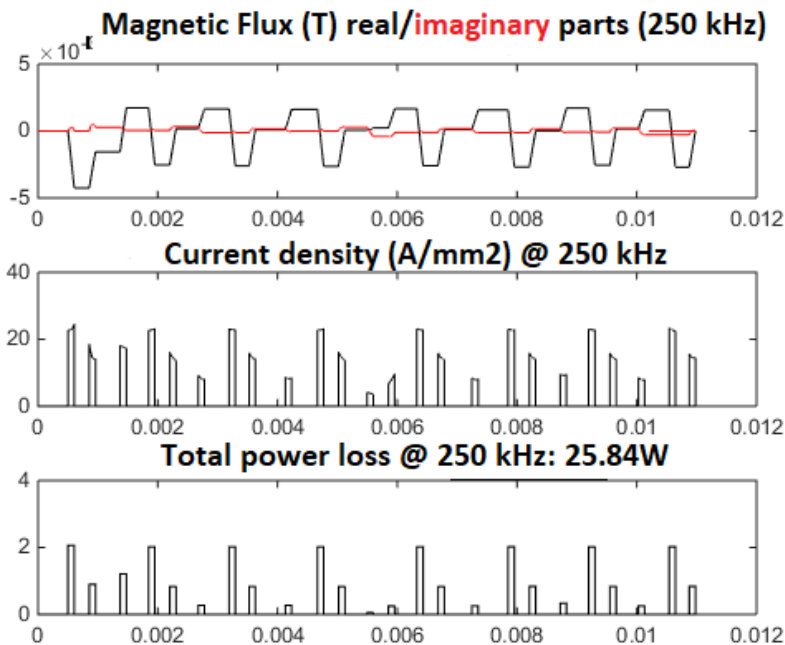


Figure 4-43: $B(T)$, $J(A/mm^2)$ and power loss for primary side supplied by a voltage source at 250 kHz, under short-circuit conditions for 2° and 3° sides. The horizontal axis represents the conductor layers in the vertical PCB stack.

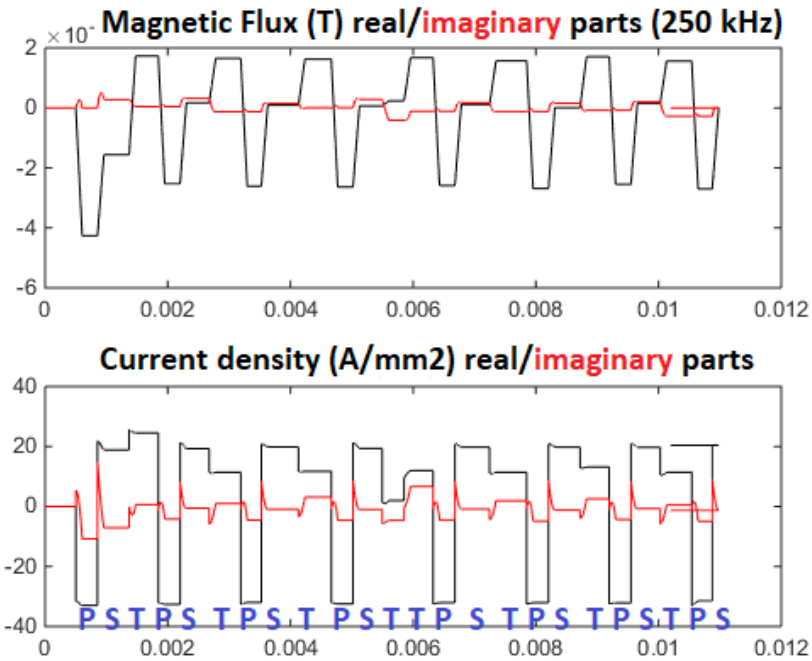


Figure 4-44: $B(T)$, $J(A/mm^2)$ real and imaginary parts for primary side supplied by a voltage source at 250 kHz, under short-circuit conditions for 2° and 3° sides. The horizontal axis represents the conductor layers in the vertical PCB stack.

Note that to compensate magnetic flux variation in the primary side, except by the first layer from the secondary side, the real and imaginary parts of the current have the same signal in the conductors S and T. If the imaginary and real parts in the other layers had the same behavior as the first layer, with opposite directions, the impedance between P and S, Z_{12} could have a negative signal in the circuit. We repeat the same test at 50 kHz and 350 kHz, Figure 4-45 and Figure 4-46, respectively. The induced currents in the second and third sides start having important imaginary values with opposite signs around 300 kHz. At high-frequency, the imaginary contribution becomes higher, and the elements from the equivalent circuit may be negatives.

circuit tests are simulated by imposing the current and or voltage on the windings. The values of the single self-impedance remained to the primary side, and the inter-winding impedances are plotted for an extended frequency range in Figure 4-48. The model in a certain frequency can be exported to time-domain simulation environments to predict parasitic oscillations in the converter.

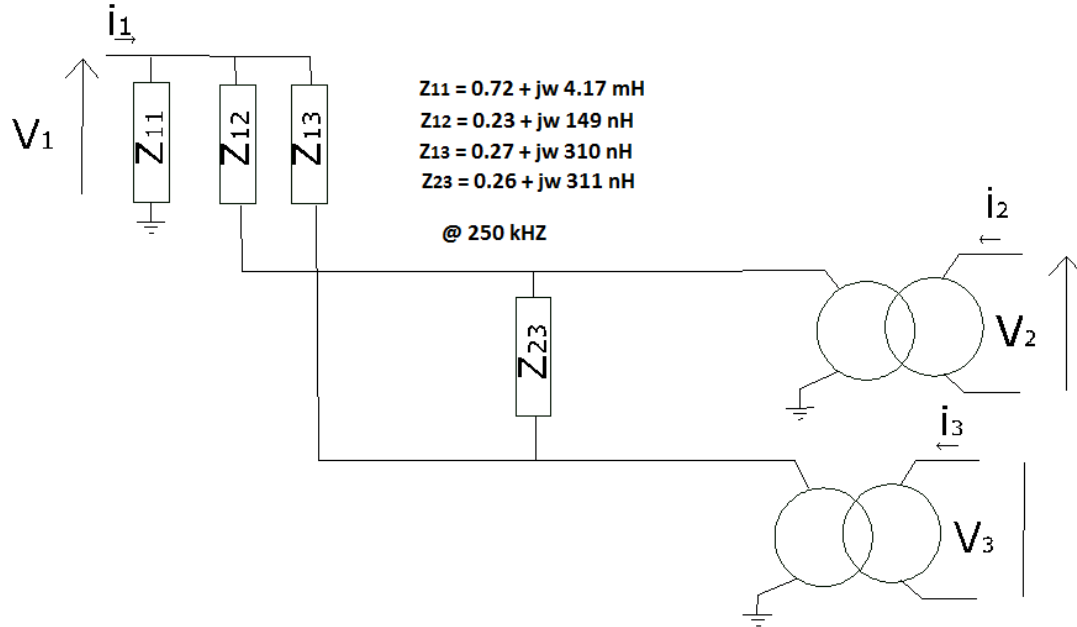


Figure 4-47: Equivalent circuit at 250 kHz.

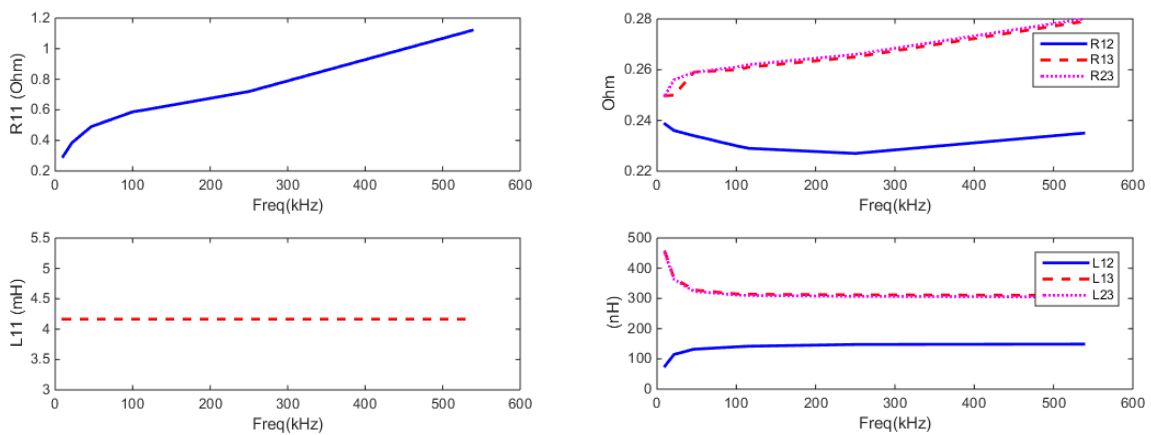


Figure 4-48 : Passive elements to represent the equivalent circuit of the three-winding transformer.

Using the same routine in Matlab, we estimate the leakage inductance between two windings. First, we evaluate the flux between two windings while the third one remains open. Figure 4-49 shows the leakage inductances between a pair of windings. The leakage energy between the first and third windings is almost the same between the second and third windings.

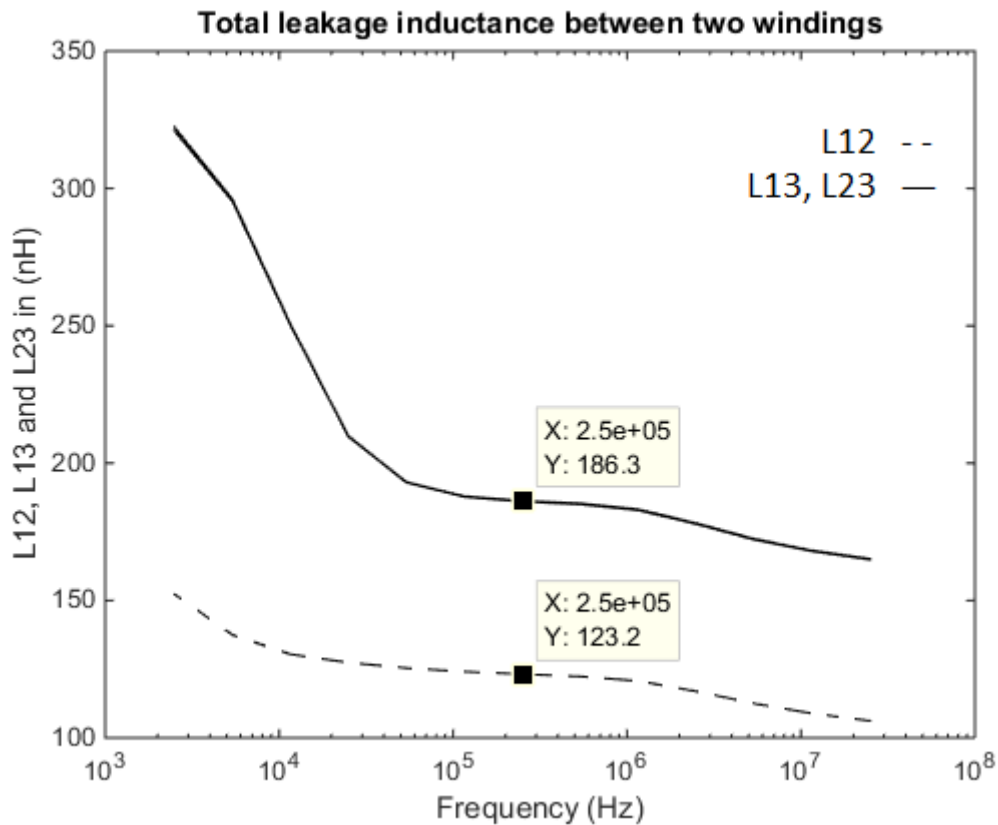


Figure 4-49: Leakage inductance between windings.

4.5.3- Experimental results

Using an impedance analyzer able to measure frequencies up to 50 MHz, we make short and open circuit tests to determine the elements in the equivalent circuit. The impedance analyzer is useful in the case of planar transformers, mainly when parasitic capacitors are not negligible, so that the transformer may present resonant peaks in a medium frequency range.

The procedure to measure the elements of the equivalent circuit consists of two main steps. The first one is the open-circuit test to determine the self-impedance and the transformer's ratio. The second step is to measure the inter-winding impedances in the short-circuit configuration: from the open winding terminals while a short-circuit is made in the other windings, as in Figure 4-50. The impedance obtained is the parallel equivalent between the self-impedance remained to the open-winding and the inter-impedances connecting this winding to the other short-circuited terminals, as written below.

$$Z_{eq1} = Z_{10} // Z_{12} // Z_{13} \quad Z_{eq2} = Z_{12} // Z_{23} \quad Z_{eq3} = Z_{13} // Z_{23} \quad (25)$$

The above equations are only valid when the self-impedance is much larger than the inter-winding impedances. Figure 4-51 and Figure 4-52 present the measurement results for open-circuit tests for high and low voltage sides, respectively. The first and second windings are symmetrical, then, only

the impedance in one of them is presented. We had not introduced parasitic capacitances in the equivalent model proposed in Figure 4-47, but, as can be seen, multi-capacitances have substantial influence in the transformer. The first resonant peak is due to the equivalent winding capacitance viewed from all the windings.

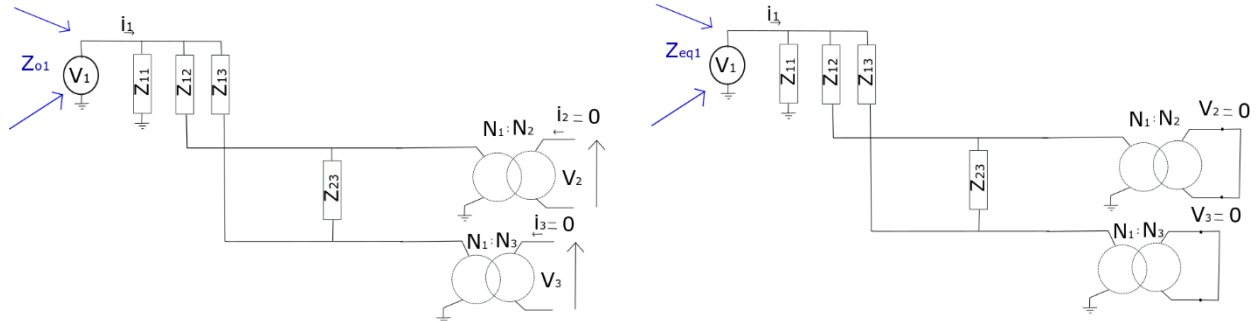


Figure 4-50: Examples of the measured impedances in the real transformer prototype using the impedance analyzer. A) Open-circuit test b) Short-circuit test.

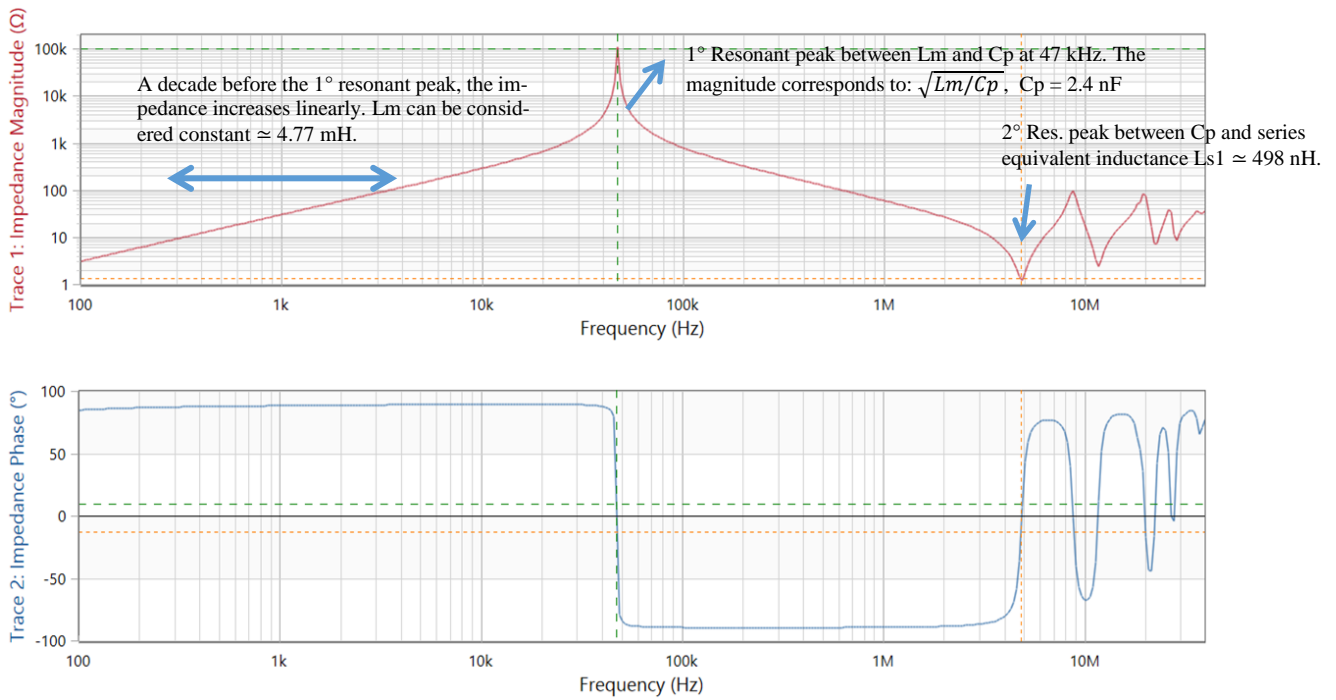


Figure 4-51: Open-circuit test using an impedance analyzer. Impedance viewed from the 1° port (one of the High voltage sides).

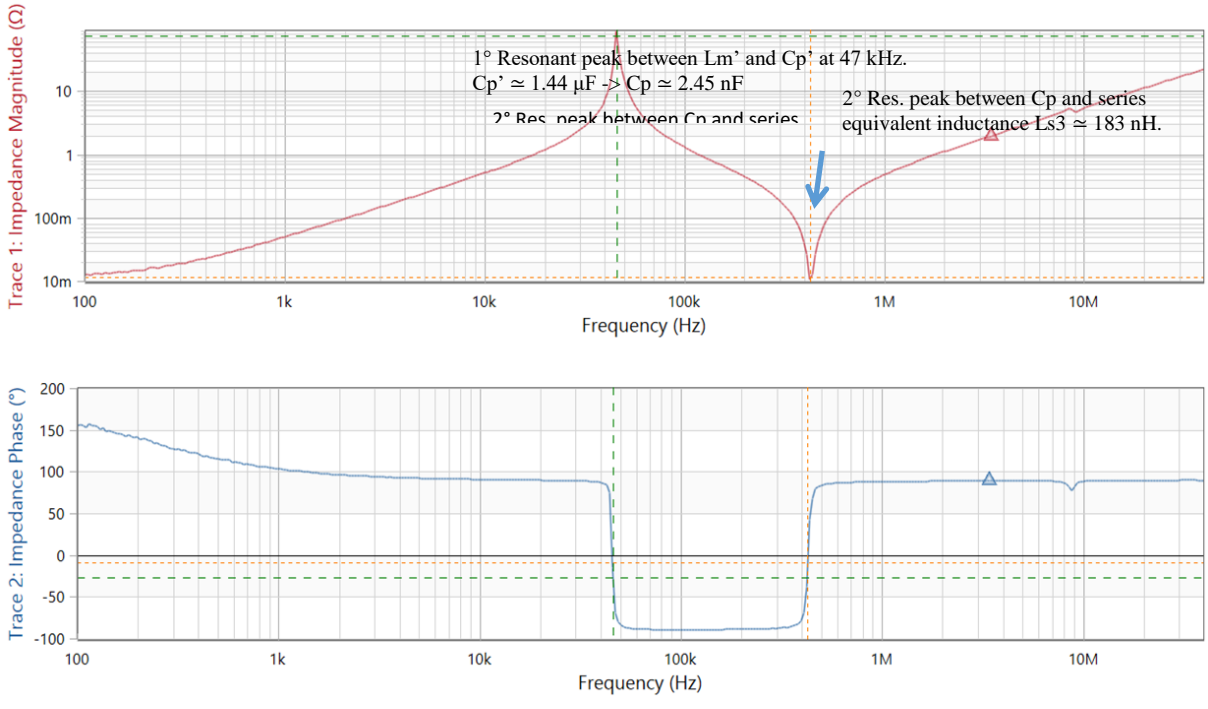


Figure 4-52: Open-circuit test using an impedance analyzer. Impedance viewed from the 3^o port (Low voltage side).

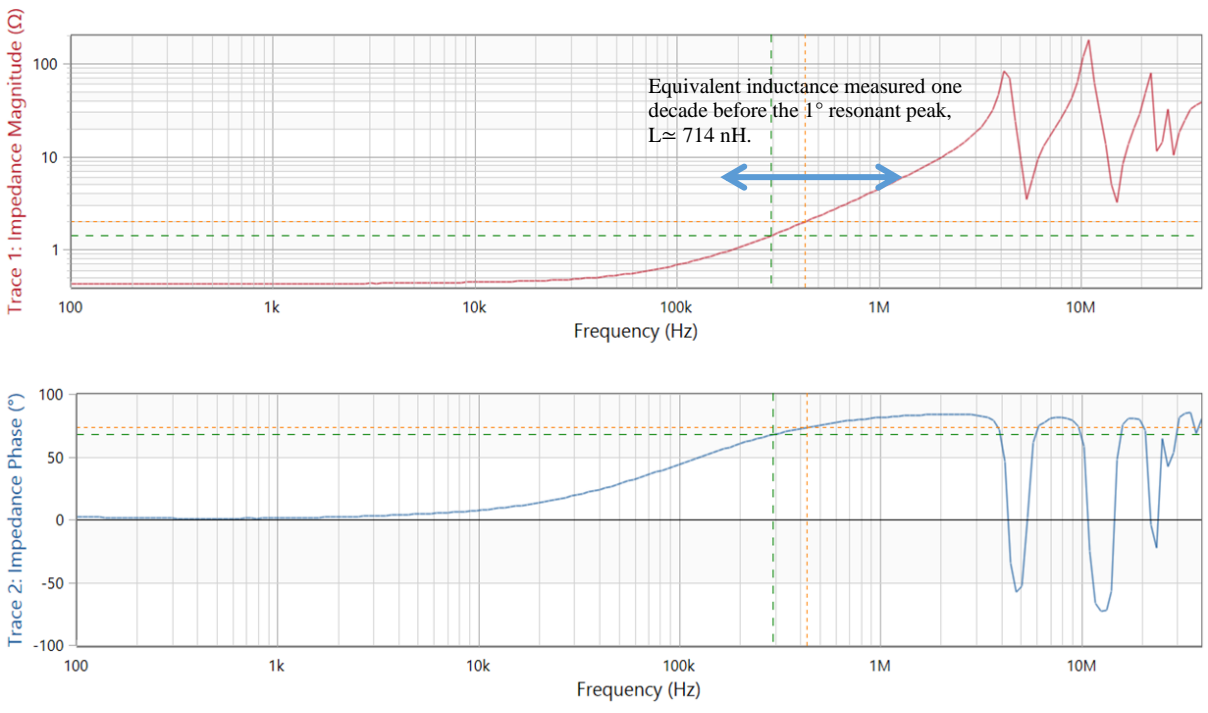


Figure 4-53: Short-circuit test using an impedance analyzer. Impedance viewed from the 1^o port (High voltage side).

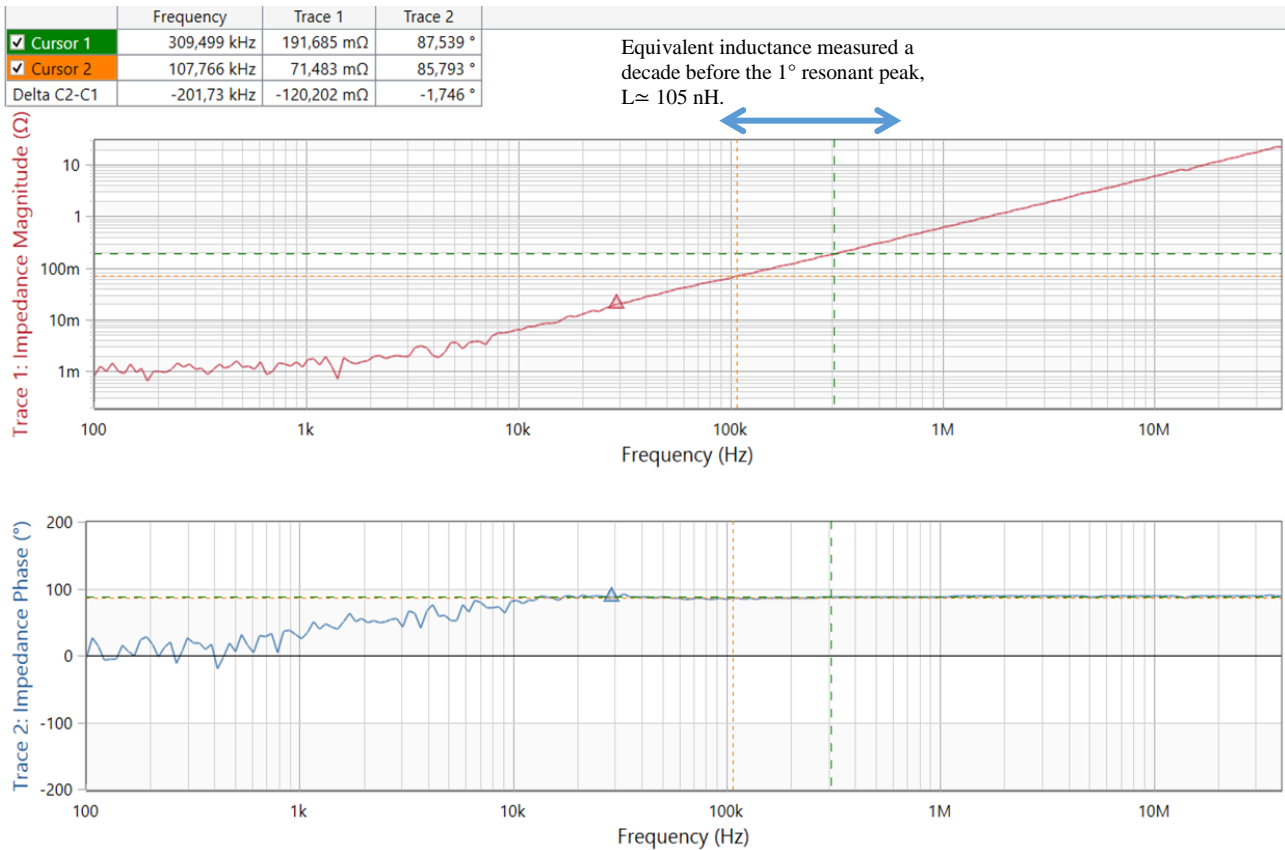


Figure 4-54: Short-circuit test using an impedance analyzer. Impedance viewed from the 3° port (Low voltage side).

Figure 4-53 and Figure 4-54 present the measurement results for short-circuit tests for high and low voltage sides, respectively. As for open-circuit tests, the impedance is the same for both high voltage sides, the impedance viewed from the second windings was omitted. The curve viewed from the third transformer winding does not present resonance in this specific frequency range. To determine the elements in the circuit from Figure 4-47, we use the inductance values during the linear region of the curves before the influence of the resonant peaks; the resistances are measured at low frequency. Table 4-13 shows the difference between the equivalent circuit parameters obtained with the impedance analyzer and the results obtained with the analytical method.

	Matlab Results	Impedance Analyzer
L10, R10	4.174 mH, 0.72 Ω	4.86 mH, 1.12 Ω
L12, R12	149 nH, 0.228 Ω	195 nH, 0.19 Ω
L13, R13	309 nH, 0.26 Ω	265 nH, 0.31 Ω
L23, R23	311 nH, 0.27 Ω	263 nH, 0.30 Ω

Table 4-13: The parameters in the equivalent circuit representing the planar transformer.

The results show coherence between the proposed model and measured values. The frequency is considered an important aspect of the equivalent circuit and negative inter-winding impedances are

physically explained. Nevertheless, we can avoid negative values and propose an equivalent model able to be used in time-depended simulations.

4.5.4- Parasitic capacitances

The approach of a network matrix relating voltage drops in each winding and total electrical charge, analogous as it was made for the equivalent circuit containing only resistances and inductances, allows the determination of a matrix of capacitances as presented in Eq. (26).

$$\left\{ \begin{array}{l} Q_1 = C_{11} \cdot v_1 + C_{12} \cdot v_2 + \dots + C_{1N} \cdot v_N \\ Q_2 = C_{21} \cdot v_1 + C_{22} \cdot v_2 + \dots + C_{2N} \cdot v_N \\ \dots \\ Q_N = C_{N1} \cdot v_1 + C_{N2} \cdot v_2 + \dots + C_{NN} \cdot v_N \end{array} \right. \quad (26)$$

Usually, the main problem with this representation is the association with the circuit in Figure 4-47 and the simultaneous solution of a magneto-static and electrostatic problem. Some authors propose an analytical calculation of stray capacitances by considering a linear voltage distribution, such as in [6] and intra and inter-winding capacitances are estimated by the common surface areas and dielectric distances between layers.

$$C_o = \frac{\epsilon_r \epsilon_o S}{\Delta h} \quad (27)$$

ϵ_r is the relative permissibility of the insulation material

S is the common surface between the winding traces

Δh is the insulation thickness

In Figure 4-55, we see the orthogonal effects of electric and magnetic field strengths if we admit the conditions used in section 4.3 and that the electric field varies linearly on the z-axis. The electrostatic energy in (28) and total charge (29) depend on the voltage distribution:

$$Energy = \frac{1}{2} \iiint_{dV} \vec{D} \vec{E} dV = \frac{\epsilon_o \epsilon_r}{2} \iiint_{0 \ 0 \ 0}^{h \ L \ F} (\Delta V^2 z^2) (dx \ dy \ dz); \quad \frac{dE}{dy} = 0; \quad \frac{dE}{dz} = Constant \quad (28)$$

$$Q_{winding} = \sum Q = \sum \iint_{dS} \vec{D} d\vec{S} = \epsilon \sum \iint_{x=0, y=0}^{F, Lc} \frac{dV}{dz} dx \ dy = \epsilon S \sum \frac{dV}{dz} \quad (29)$$

Once this result is available, the electrostatic analysis can be made. With the given voltage distribution, the software FEMM-2D simulator calculates the stored energy and the total charge in the conductors. Figure 4-57 shows the electric field strength obtained with the voltage drop information present in Figure 4-56.

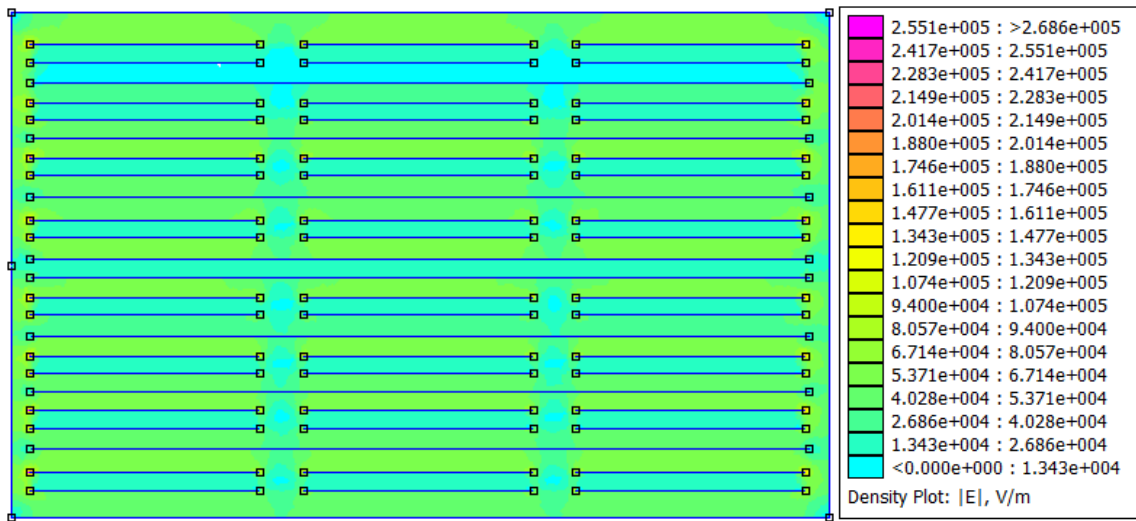


Figure 4-57: Electrostatic field strength simulated in FEMM using the voltage distribution information obtained with the previous analysis considering frequency effects.

Using the analysis for the inductances, short-circuit tests can be made to allow the simulation of capacitive effects. First, let us consider the schematic in Figure 4-58 to represent parasitic capacitances in the planar transformer. Intra-winding capacitances C_{10} , C_{20} and C_{30} due to the internal voltage distribution in a single winding; and inter-winding capacitances C_{12} , C_{13} and C_{23} due to the intersection between conductors from different windings.

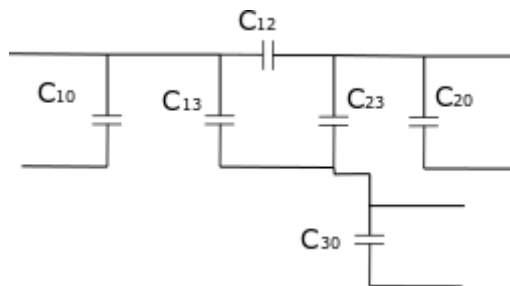


Figure 4-58: Equivalent circuit including only stray capacitances remained to primary side.

Six tests are necessary. For the specific transformer developed in section 4.4, the intra-winding capacitances C_{10} and C_{20} are almost equal, and the intra-winding capacitance C_{30} is neglected because of the parallel connection between the turns in the third winding. Therefore, only four tests are enough for the determination of these elements. The first test consists in to measure the impedance viewed from one of the ports while the others are under short-circuit conditions, Figure 4-59-a. The measured

capacitance, viewed from the primary side, is directly obtained by the first resonant peak in the equivalent curve in Figure 4-60. According to the schematic in Figure 4-58, it corresponds to the sum of C_{10} , C_{12} and C_{13} . The same test is repeated viewed from the second side, with results very similar to Figure 4-60. The impedance viewed from the third port is presented in Figure 4-61, and we note that there is no resonance, validating the affirmation of a very small capacitance C_{30} . The equations obtained are written below:

$$1^{\circ} \text{ side: } C_{10} + C_{12} + C_{13}$$

$$2^{\circ} \text{ side: } C_{20} + C_{12} + C_{23} \quad (31)$$

$$3^{\circ} \text{ side: } C_{30} + C_{13} + C_{23}$$

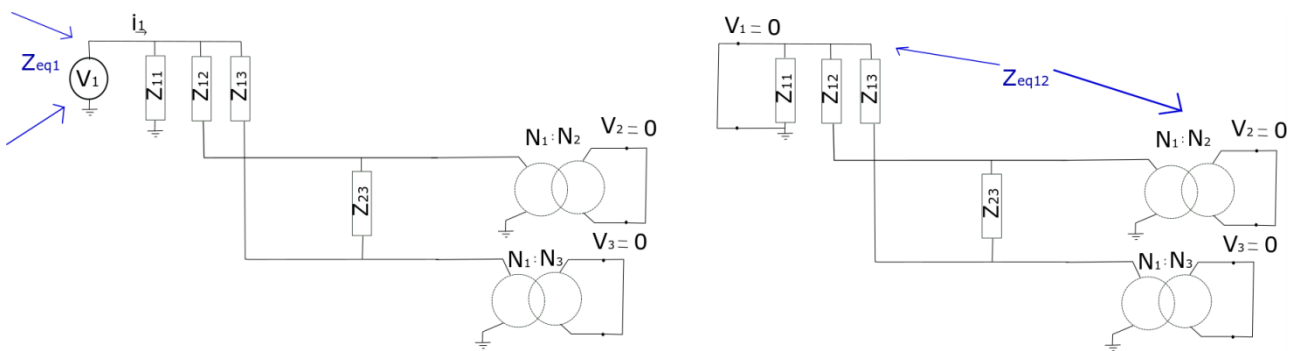


Figure 4-59: Example of the circuit configuration to obtain the parasitic capacitances a) Influence of intra-winding capacitances b) influence of inter-winding capacitances.

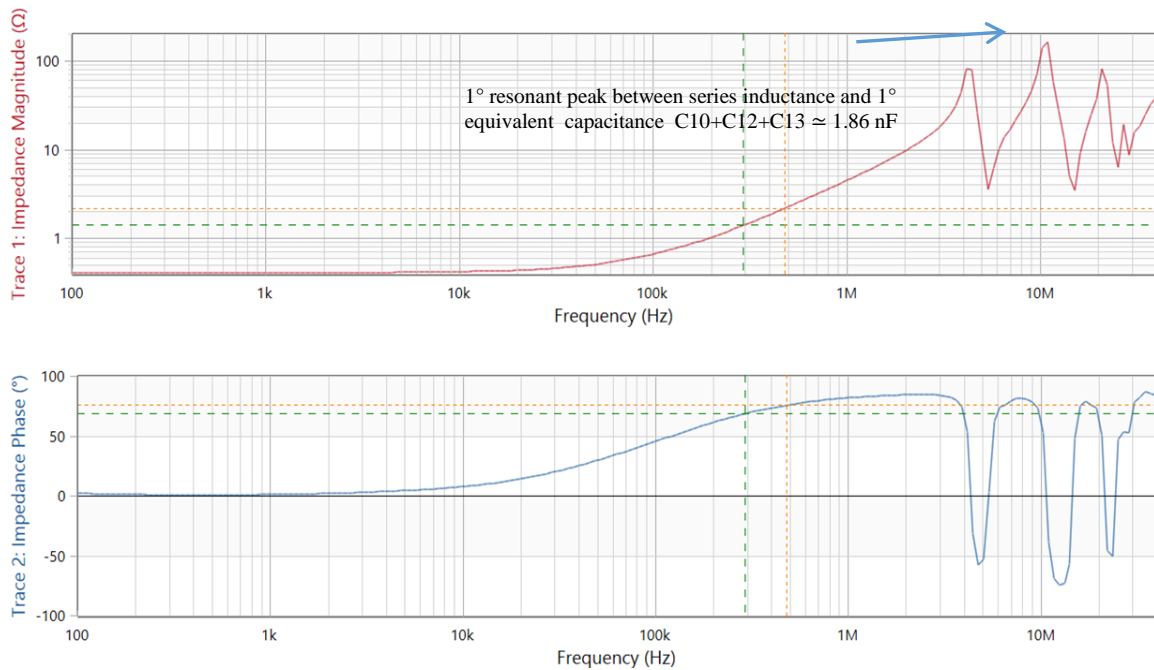


Figure 4-60: Intra-winding capacitance measured with an impedance analyzer viewed from primary side.

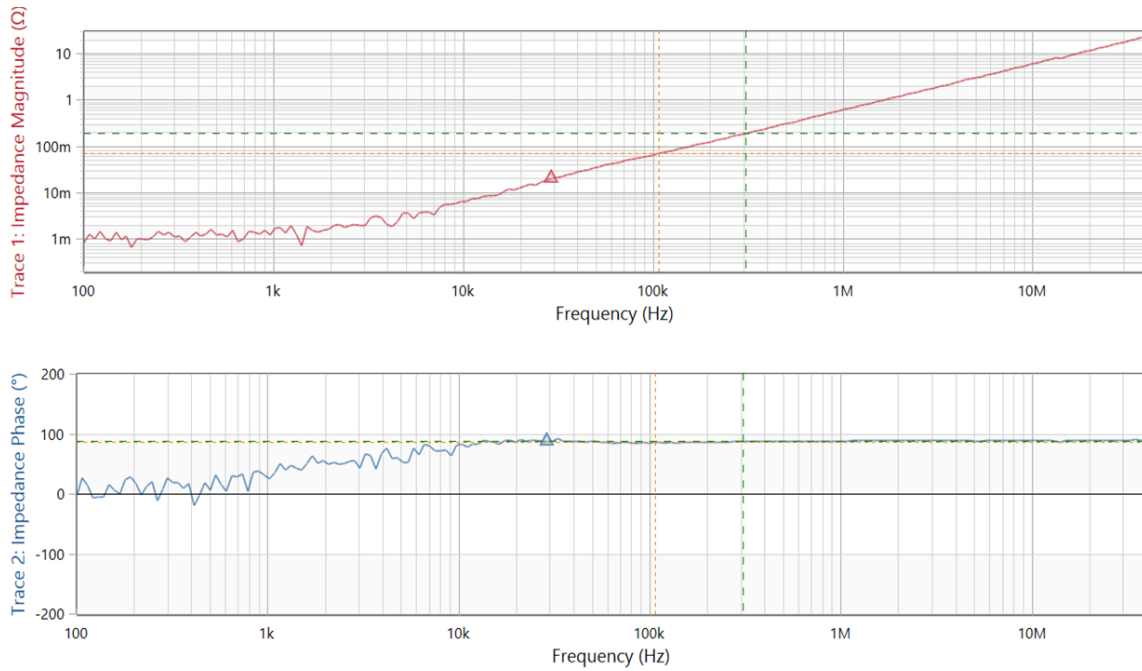


Figure 4-61: Intra-winding capacitance measured with an impedance analyzer viewed from 3° side.

The second test consists in to measure the impedance between two windings with short-circuit conditions in the three ports, as shown in Figure 4-59-a, and Figure 4-62.

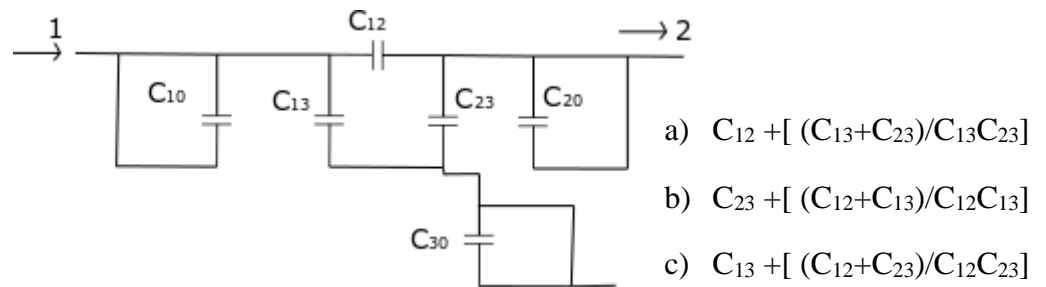


Figure 4-62: Inter-winding capacitance measurement.

$$\text{Between 1 and 2 } C_{12} + [(C_{13} + C_{23}) / (C_{13} C_{23})]$$

$$\text{Between 1 and 3 } C_{13} + [(C_{12} + C_{23}) / (C_{12} C_{23})] \quad (32)$$

$$\text{Between 2 and 3 } C_{23} + [(C_{12} + C_{13}) / (C_{12} C_{13})]$$

The tests between primary and secondary sides, and between secondary and third sides are presented in Figure 4-63 and Figure 4-64, respectively. We use the first resonant peak in association with the equivalent series inductance to determine the capacitances.

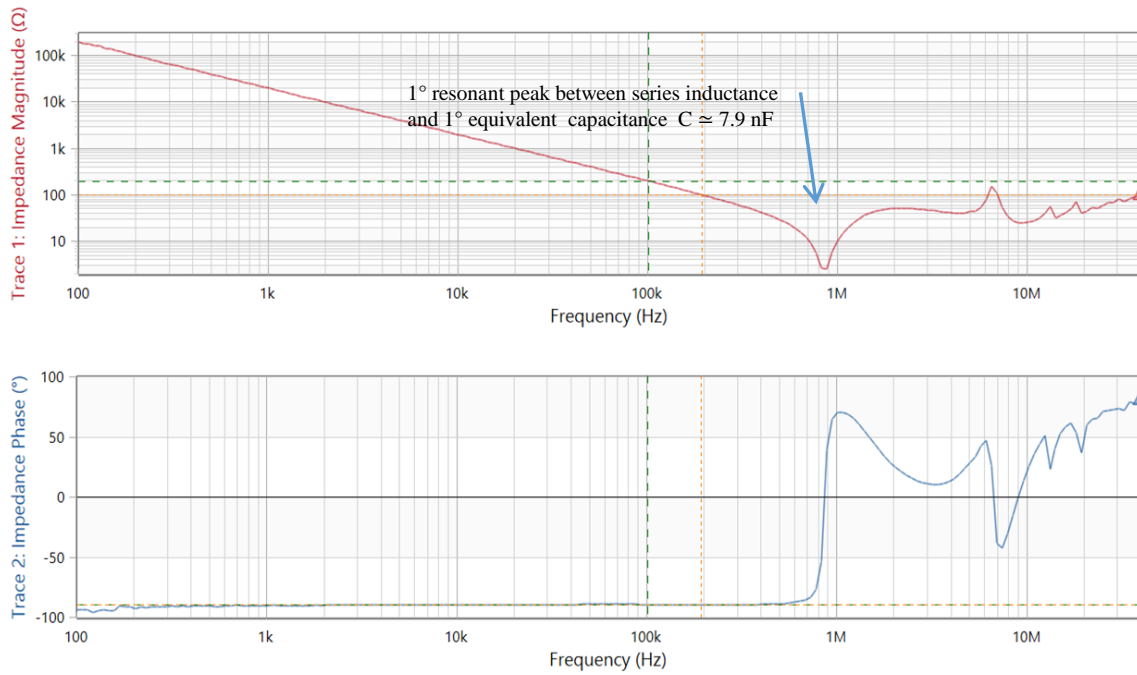


Figure 4-63: Inter-winding capacitance measured with an impedance analyzer between ports 1, 2.

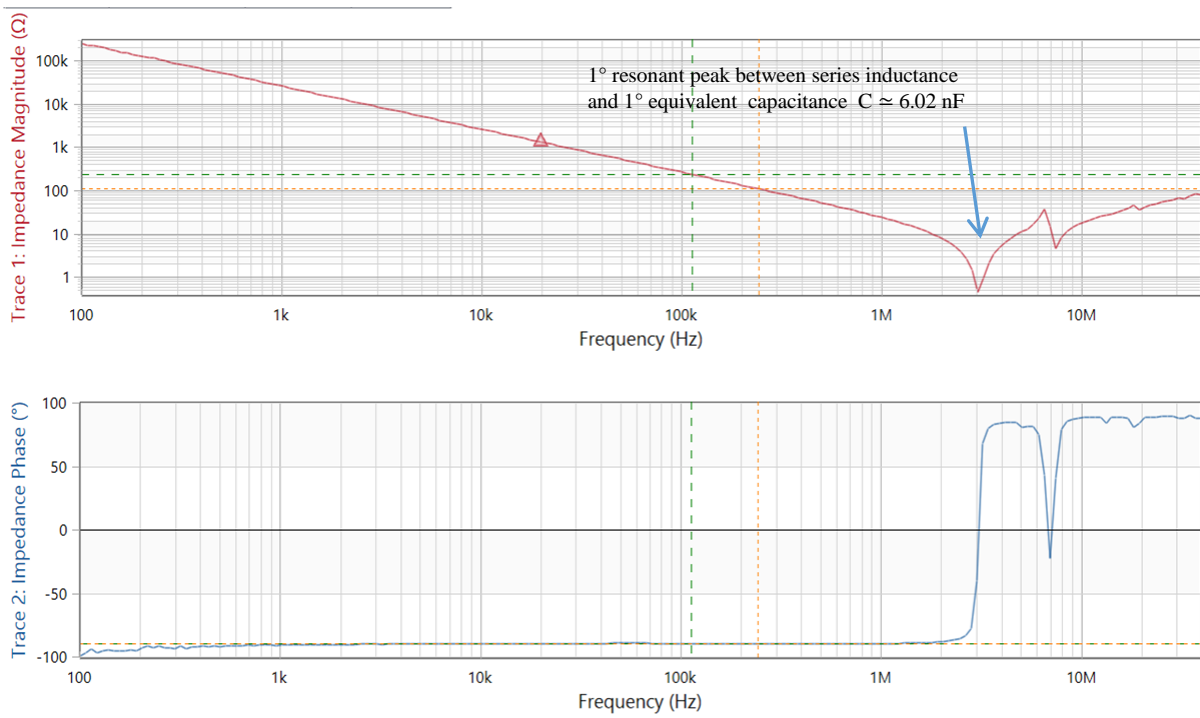


Figure 4-64: Inter-winding capacitance measured with an impedance analyzer between ports 2, 3.

Using the equations obtained with the tests described above, the individual capacitances associated with the schematic in Figure 4-58 are calculated in the second column from Table 4-14.

	Matlab /FEMM	Impedance Analyzer
C10	0.46 nF	1.12 nF
C12	0.46 nF	0.49 nF
C13	0.29 nF	0.27 nF
C23	0.17 nF	0.26 nF

Table 4-14: The equivalent stray capacitances in the planar transformer obtained with the Impedance analyzer and simulation tools.

The electrostatic analysis in FEMM also allows the determination of equivalent capacitances associated with each winding. The first simulations are made by exciting one of the ports with a small current while the other two are under short-circuit conditions, as shown in Figure 4-65, Figure 4-66 and Figure 4-67. Using the simulation tools is not possible to obtain the inter-winding capacitances directly, but the stored energy, while a single port is in short-circuit situation, allows the determination of three more equations, as shown in Figure 4-68, Figure 4-69 and Figure 4-70. The simulation conditions, the stored energy, and the total charge accumulated in the conductors are shown in Table 4-15.

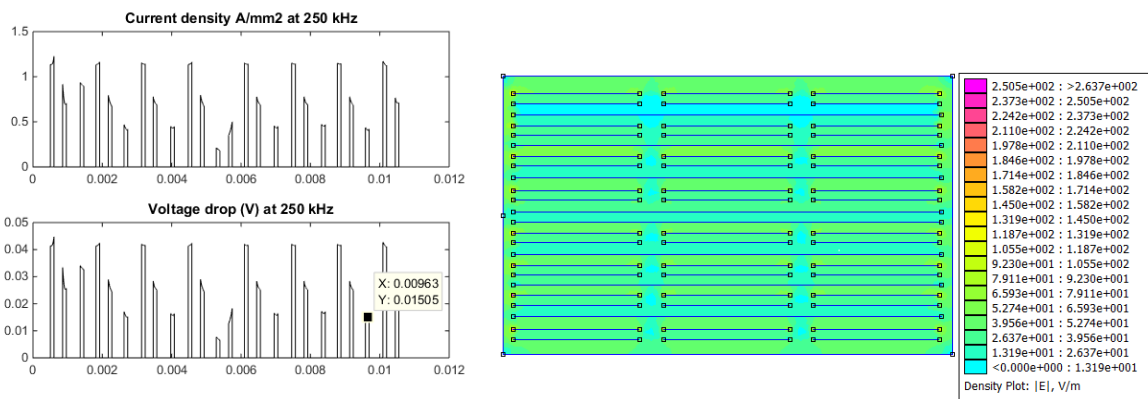


Figure 4-65: $i_1 = 1A$, short-circuit in 2° and 3° windings. a) Voltage drop considering frequency effects b) Electric field strength simulated in FEMM.

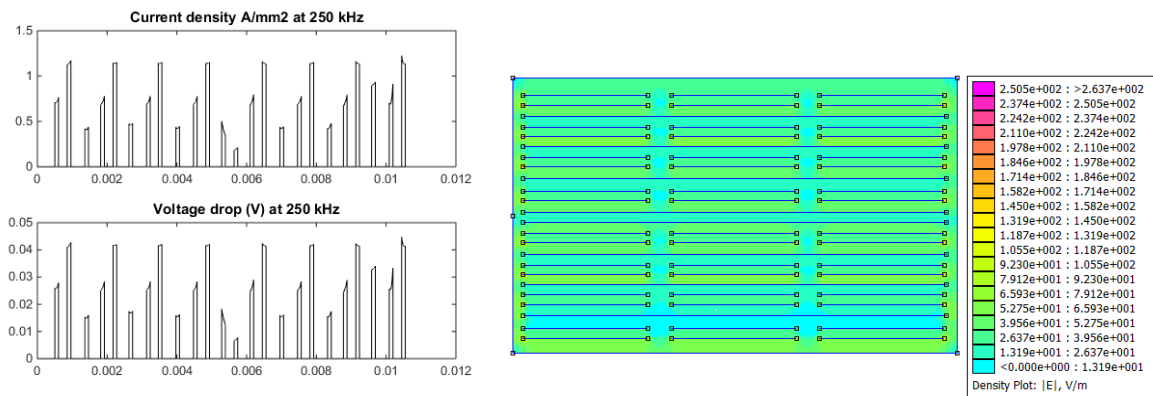


Figure 4-66: $i_2 = 1A$, short-circuit in 1° and 3° windings. a) Voltage drop considering frequency effects b) Electric field strength simulated in FEMM.

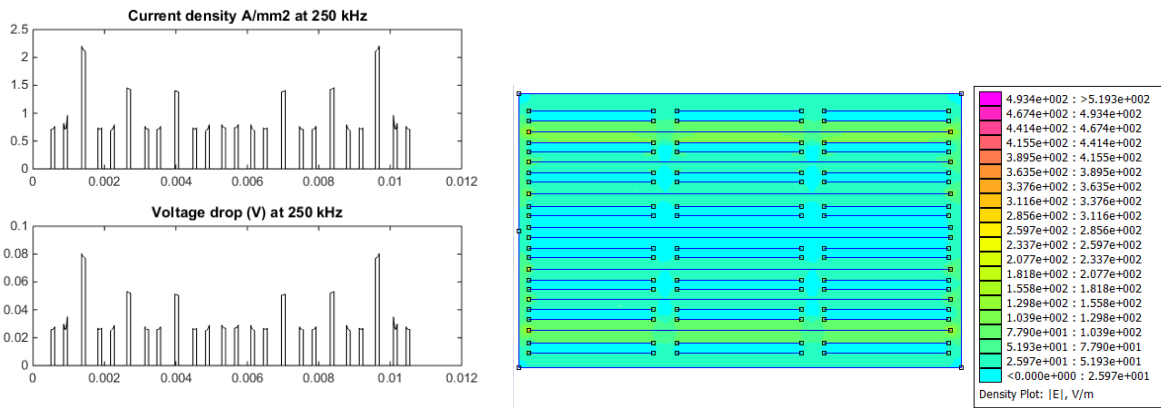


Figure 4-67: $i_3 = 10A$, short-circuit in 1° and 2° windings. a) Voltage drop considering frequency effects b) Electric field strength simulated in FEMM.

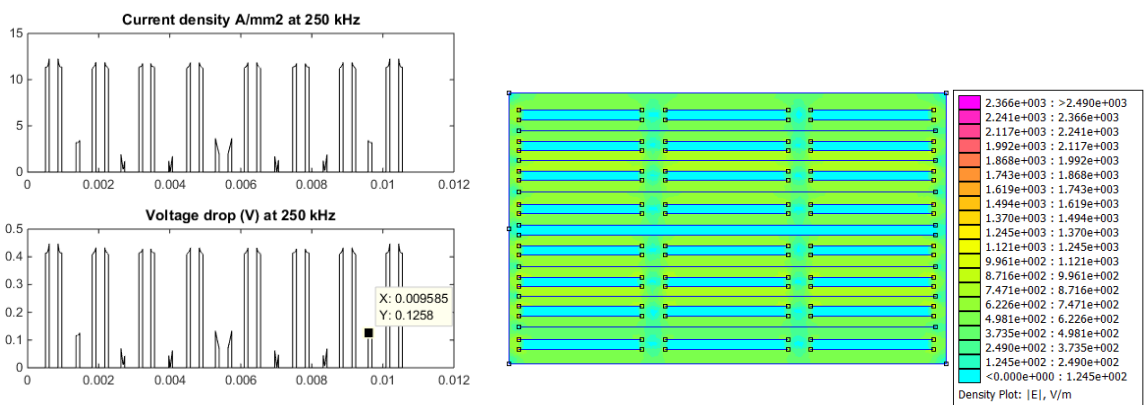


Figure 4-68: $i_1 \neq 0$, $i_2 \neq 0$ and short-circuit in the 3° winding. a) Voltage drop considering frequency effects b) Electric field strength simulated in FEMM.

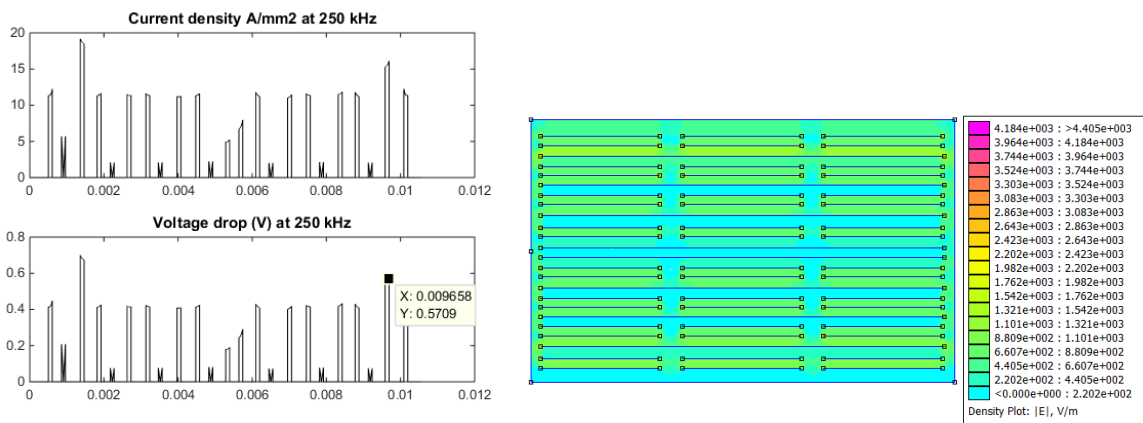


Figure 4-69: $i_1 \neq 0$, $i_3 \neq 0$ and short-circuit in the 2° winding. a) Voltage drop considering frequency effects b) Electric field strength simulated in FEMM.

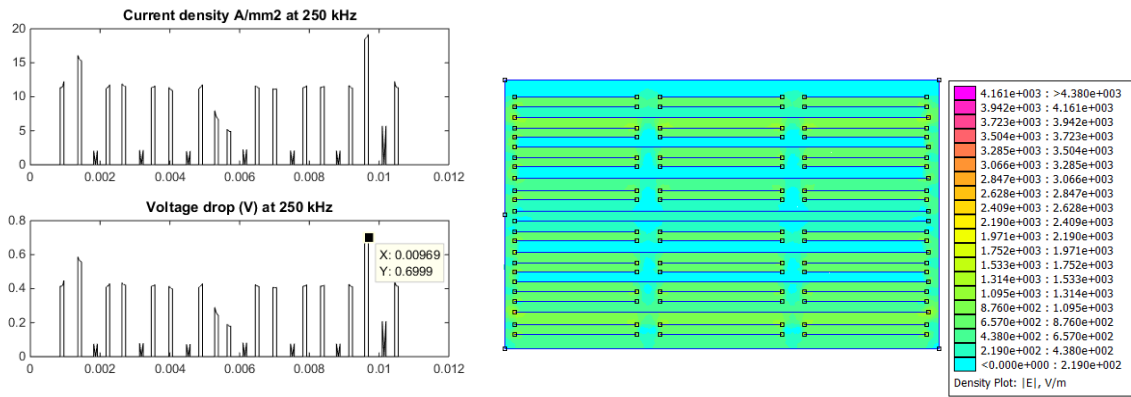


Figure 4-70: $i_2 \neq 0$, $i_3 \neq 0$ and short-circuit in the 1° winding. a) Voltage drop considering frequency effects b) Electric field strength simulated in FEMM.

In the three first tests, the voltage among the windings is not zero because there is real current components circulation inside them generating voltage drop. In the three last tests, only one of the windings is under short-circuit with imaginary current component. Therefore, the capacitance measured is not affected by this short-circuit winding.

Test conditions	Stored Energy (pJ)	Ct (nF)	$C_1 = Q_1/V_1$	$C_2 = Q_2/V_2$	$C_3 = Q_3/V_3$
Figure 4.65	0.383	0.462	0.57 nF	-0.125 nF	-0.95 nF
Figure 4.66	0.368	0.460	-0.154 nF	0.57 nF	-1.02 nF
Figure 4.67	0.652	0.022	-0.434 nF	0.473 nF	0.58 nF
Figure 4.68	74.77	0.95	0.51 nF	0.49 nF	-
Figure 4.69	98.9	0.47	0.62 nF	-	0.49 nF
Figure 4.70	111.1	0.52	-	0.63 nF	0.66 nF

Table 4-15: The stored energy and simulated capacitances in FEMM. Ct is the equivalent capacitance associated with the stored energy.

The equations describing the simulation conditions (Annexes 4.82) are used to determine the individual capacitances presented in the first column of Table 4-14. Comparing the results between the impedance analyzer and the simulation, we see a quite difference concerning intra-winding capacitance. A single equivalent capacitance of 2.53 nF can be obtained by transforming the circuit from Δ to Y, viewed from the first transformer's side, using the results from the impedance analyzer.

In the converter operation, inter-winding capacitances will affect the EMI common mode and intra-winding capacitances may alter the resonant frequency of the converter. In Chapter 5, we see the influence of parasitic elements in the converter operation.

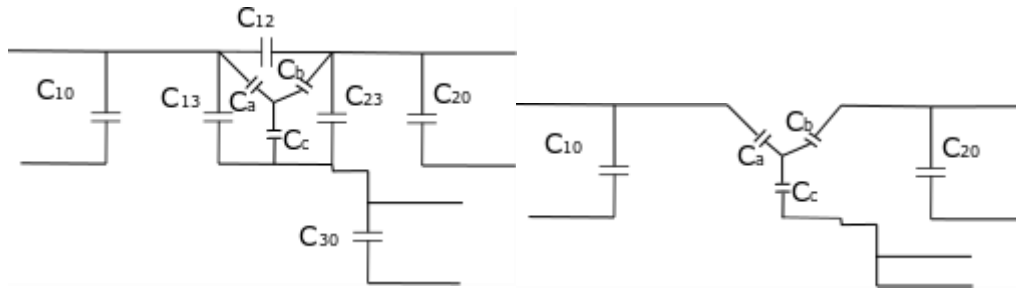


Figure 4-71: Equivalent circuit transformation to determine a single equivalent capacitance. C_{30} is neglected.

4.6- A Transformer design using copper foils

An alternative process was used to fabricate the transformer inspired by the work in [10]. The process was fully developed in the Fabrication Laboratory, La Fabrique, located at CentraleSupélec. La Fabrique has various resources, such as mechanical, electronic, and informatics, giving the users the possibility to build their prototypes. In the conception of the planar transformer, the possibility of testing different arrangements or even different insulating materials to reduce parasitic capacitances and improve thermal characteristics makes this approach worthwhile. In effect, the use of multilayer PCB implies in poor thermal dissipation in the layers located in the middle of the stack, despite the efforts to ensure a well current distribution under high-frequency effects. The use of copper foils may present some advantages over the use of PCB's because we can choose another material according to design issues. In Table 4-16, we see some candidates for constituting the insulation layers.

Mica is a great candidate to replace the FR4 because of its better thermal properties, and it can be found in a paper foil format with thicknesses of 0.1 mm, 0.2 mm. Nomex is also a paper that can be easily found and is recommended when we aim to reduce stray capacitances.

	FR4	Nomex **	Mica **	Kapton* (Polyimide film)
Thermal conductivity (W/mK)	0.29	0.139	0.35 (0.3 - 0.52)	0.12
Dielectric Strength (kV/mm)	20	33.2 (29 - 33)	25	303 (339 - 268)
Dielectric constant	4.3 - 4.7	2.6 (2.3 - 3.1)	(6.5 - 8.7)	3.5 (3.0 - 3.8)

Table 4-16: Properties of some insulating materials used in transformers.

*50% relative humidity, 1.8% water in the film, 0.25mm **50% relative humidity, 0.25mm, *** Mica content 90%, 0.2 mm.

For the conductor layers conception, we had used copper foil of 0.1 mm and a TROTEC® laser engraver to reproduce the specific design of the turns. The laser engraver reads files in SVG format, and to generate the layout of each layer in this format, we used Inkscape, indicating the electrical vias position, the distance between the turns, and their form. The setup of the laser engraving machine was adjusted by steps, such as the laser power-up, the engraving speed, and the passes number of the

laser beam. Two acrylic sheets were used to close the stack of copper and insulating layers as a sandwich. Outside clips were also developed with a 3D printer and placed only for mechanical fixation. Figure 4-72 illustrates the main steps used in this design and the final prototype. Despite the better thermal properties of mica compared with Kapton, we had only used it between layers from primary and third sides. The initial idea was to apply the mica paper to all the insulating layers, but, it turns out the material is fragile, compromising the manual assembling process.

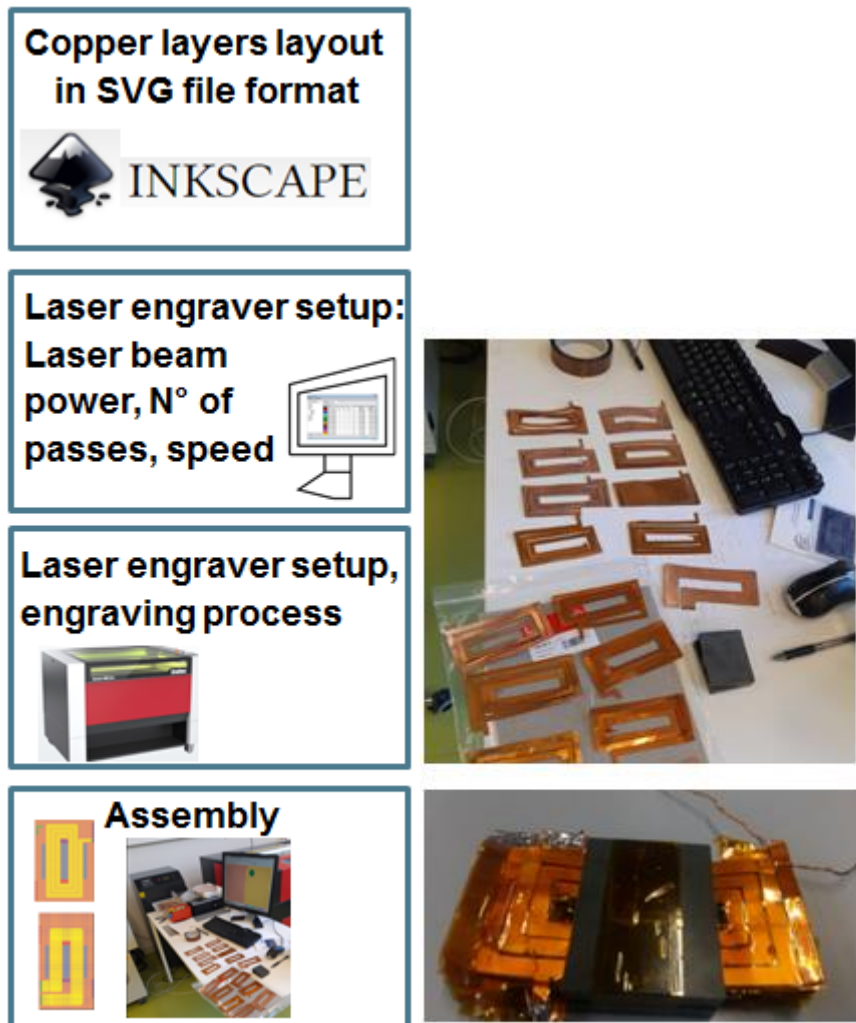


Figure 4-72: The main steps in the process to fabricate the prototype using the resources from La Fabrique.

4.7- The proposition of an improved design

With the thermal cooling solution proposed in the previous sections, we verify that for the maximum power of 7 kW, the transformer achieves higher temperatures than were expected. One of the reasons for this is the additional conductor length, necessary to connect the transformer prototype to the main power boards, once in this first version the boards were not integrated on the same PCB. The second reason is the high number of turns aimed at this project. In the total interleaved arrangement, the

connections between layers over the three different PCBs make necessary the reservation of a dedicated area only to pass the vias. Consequently, this dedicated area increases the average mean turn length of the windings, thus the equivalent DC resistances.

Now that we know the drawbacks of proposing a planar transformer with a high turn's ratio and how to determine the AC power losses accurately and leakage inductance, we propose an improvement in this design to be developed later, in future work.

In the diagram from Figure 4-73 we split the transformer into two magnetic parts. The two primary and secondary sides are series connected and the third sides are parallel connected.

Although we had opted for a single-level topology, the full-bridges could also be split into two parts, allowing to reduce the voltage peak over the transistors for both high voltage sides and the current in the low voltage side with the same transformer proposition.

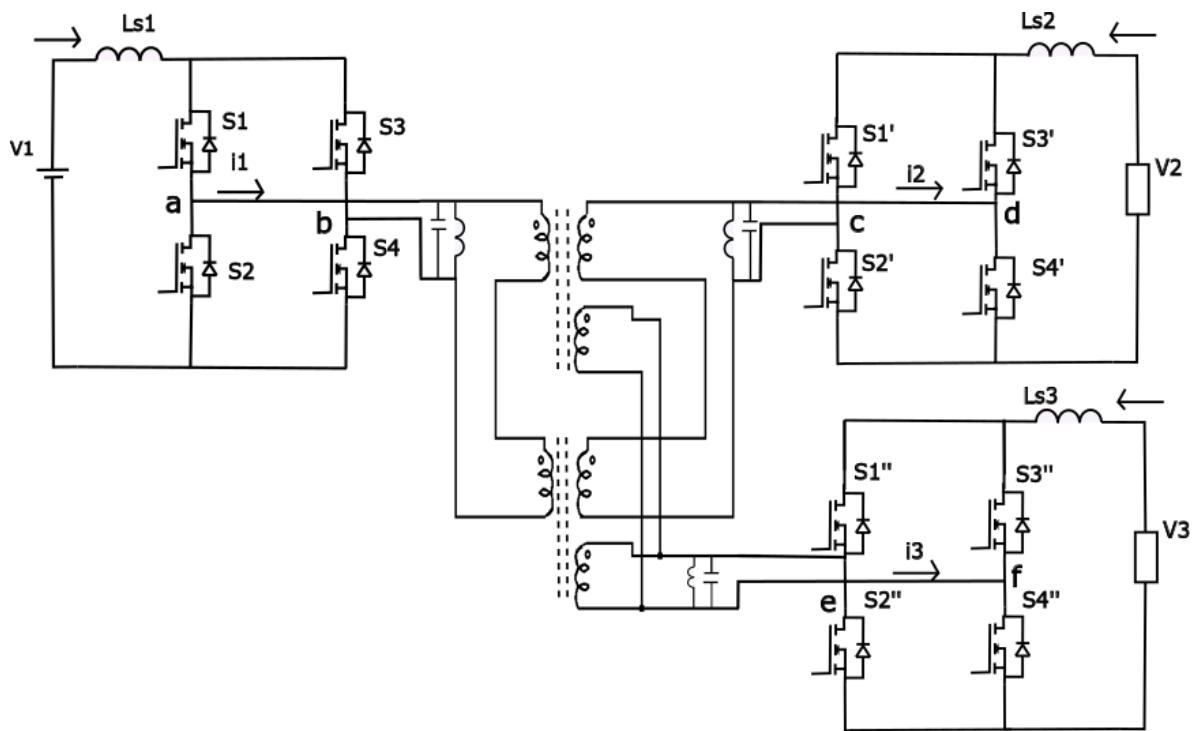


Figure 4-73: The three-winding transformer divided into two parts.

In the new proposition, we use two magnetic cores to achieve the turn's ratio of 24:24:1. In each transformer, we use two series-connected turns by layer, instead of three for both high voltage sides. Besides, instead of three PCB's, we use two PCBs with 8 layers each. One of the possible configurations is presented in Figure 4-74. The current density, power loss, and magnetic flux are shown in Figure 4-75, Figure 4-76. The power losses at 200 kHz are compared in Table 4-17 for the two designs. The winding power losses are reduced and compensate for the increase in the magnetic power losses where two magnetic cores E58 replace the single E64. The main advantage of the new configuration is the PCB temperature reduction. Other configurations can also be verified as three smaller

magnetic cores and the use of PCB with a small number of layers. The advantages include better thermal behavior and the use of PCBs containing 4 or 6 layers.

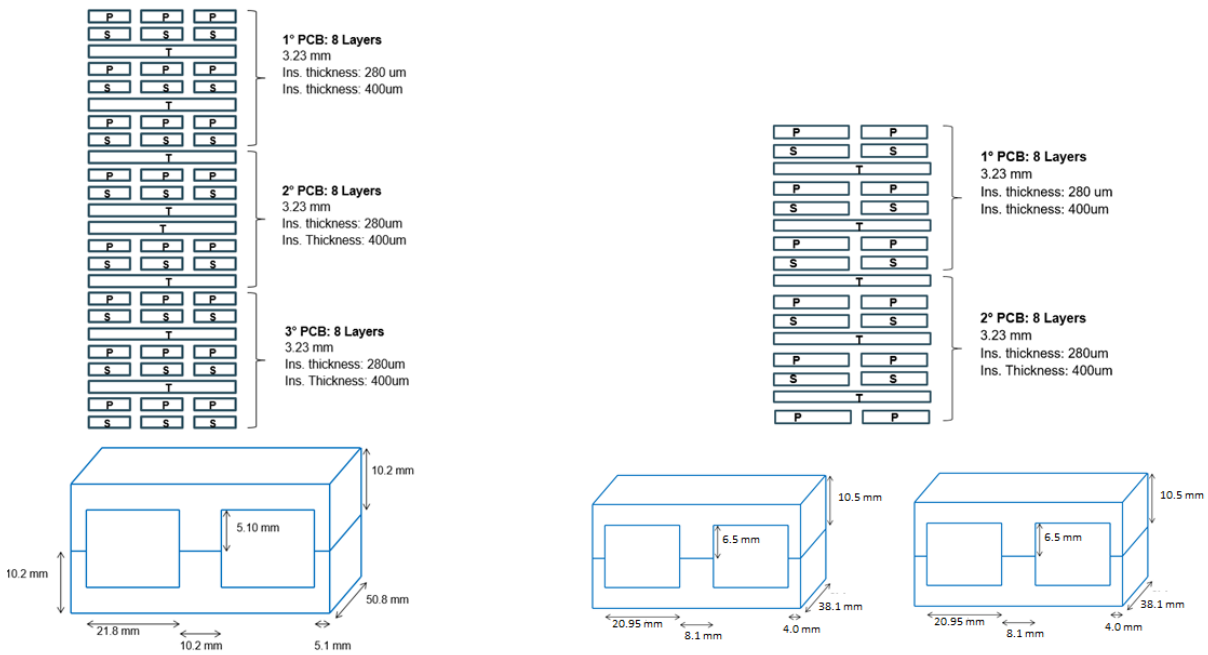


Figure 4-74: The first transformer proposition using 3 PCBs and an E64 magnetic core. b) The second proposition using 2 PCB's and 2 magnetic cores E58 for the same turns ratio.

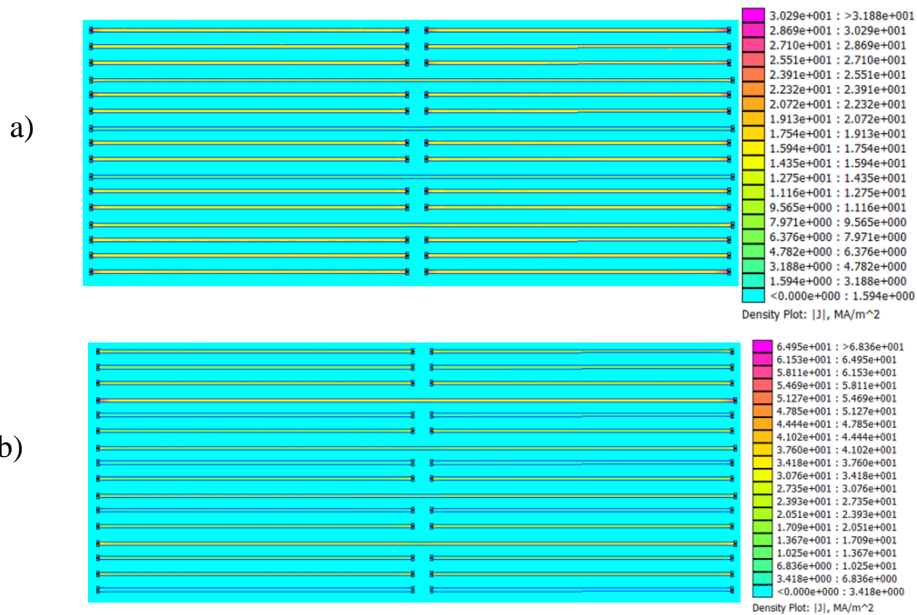


Figure 4-75: Current density from FEMM simulation results for the proposition using 2 transformers at 200 kHz a) OBC mode b) LDC mode.

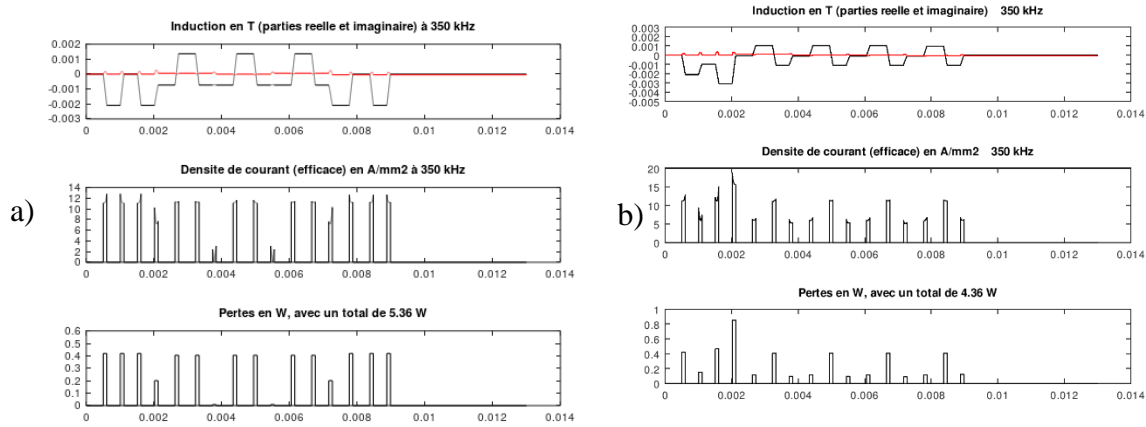


Figure 4-76: Magnetic flux, current density and power loss solved with the analytical propose method for the proposition using 2 transformers at 200 kHz a) OBC mode b) LDC mode.

	1° Design	2° Design
Magnetic power loss (W)	18.81	26.08
AC Winding power loss (W)	43.36	34.64
Total power losses (W)	64.16	63.44
N° PCBs	3	2

Table 4-17: Power losses comparison between the 1° design using a single magnetic core and the 2° design using two smaller transformers at 200 kHz for the OBC&LDC operating mode.

4.8- Conclusion

The transformer was studied as an important part of the integrated OBC and LDC converters. Three different configurations were proposed to make easier its fabrication process and minimize power loss and leakage inductance. The lossless proposed design was built in two versions, using multi-layer PCB's and copper foils. Because of the low voltage side, parallel-connected layers required a more accurate analysis, and therefore, an analytical method to determine current and power loss distribution was studied. The method allows quickly highlighting the drawbacks of the planar magnetic design and can be implemented in Matlab. The method helped in the selection of the configuration with the best performance for the converter application. The results obtained with the analytic methodology and compared with results from FEA validate the methodology. The second configuration presents a better power loss distribution and reduced leakage inductance for the transformer operating under three modes: OBC, LDC, and simultaneously OBC and LDC. However, because of the high turn ratio used in the prototype, the thermal performance needs to be improved. Besides, the use of multi-PCBs to design the product may still present some drawbacks as verified, such as the difficulty in implementing the connections between interleaved layers and the increase in the mean turn length because of the additional space to pass these connections. The use of multi-PCBs must also be full-

automatized, and the isolation between them needs to be controlled to avoid failures during the dielectric tests.

4.9- Annexes

4.9.1- Electrostatic simulation results and equivalent stray capacitances

The electrostatic simulations in FEMM while a single transformer terminal is configured in short-circuit mode, allow the determination of three equivalent equations:

$$C_{12} + \left(\frac{C_{13}(C_{30}+C_{23})}{C_{13}+C_{30}+C_{23}} \right) \quad v_1 \neq 0, v_2 \neq 0 \text{ and } v_3 = 0$$

$$C_{13} + \left(\frac{C_{12}(C_{20}+C_{23})}{C_{12}+C_{20}+C_{23}} \right) \quad v_1 \neq 0, v_3 \neq 0 \text{ and } v_2 = 0$$

$$C_{23} + \left(\frac{C_{12}(C_{10}+C_{13})}{C_{12}+C_{10}+C_{13}} \right) \quad v_2 \neq 0, v_3 \neq 0 \text{ and } v_1 = 0$$

The simulations while two ports are under short-circuit conditions gives the stored energy associated with the intra-winding capacitances in Figure 4-62.

4.10- References

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5- Design of the Bidirectional Three-port current-fed parallel resonant converter

5.1- Introduction

In this chapter, we discuss the main converter design aspects for electrical vehicle applications.

As discussed in Chapter 3, the proposed converter is operated with a unitary voltage gain to keep its zero voltage switching capability. The first full-bridge, connected to the voltage source V_1 , regulated by the PFC converter, imposes its value over the other two batteries connected in V_2 and V_3 ; thus, the only freedom degree in the design is the transformer turns ratio. In this scenario, the development of at least two additional DC-DC converters (non-isolated) is necessary to regulate the battery voltages independently, allowing the different modes: OBC, LDC, and simultaneous OBC&LDC conversions. Two solutions exist to achieve this regulation: the use of a bidirectional pre-regulating stage, or a bidirectional post-regulating stage. Each case presents advantages and limitations.

Considering a pre-regulation stage, during the HV battery charging, in the OBC mode, the voltage V_1 must be regulated according to the HV battery state of charge. In this solution, the Three-port current-fed resonant converter operates with large voltage and current variation ranges, which can significantly reduce the converter's total efficiency and add more constraints for the transformer design. The same constraints exist in the OBC reverse mode. For the LDC converter, this solution is not possible because at least one more additional stage should exist to control the LV battery voltage when the AC grid charges the HV and LV batteries simultaneously. One of the advantages in this proposition is the use of the AC/DC PFC stage to control and regulate part of the voltage range required by the HV battery. It can reduce the design constraints for the additional DC/DC converter when the batteries are being charged through the electrical grid, as illustrated in Figure 5-1-a.

The second solution consists of using two additional non-isolated DC-DC converters connected in cascade, with the HV and LV side batteries. Both structures must be bidirectional. The main advantage of this solution is to operate the Three-port current-fed resonant converter with nominal voltage for the OBC and LDC modes, increasing the efficiency of the DC/DC main converter. The disadvantage is the need for two more bidirectional converters connected in cascade with both batteries. This proposition is illustrated in Figure 5-1-b.

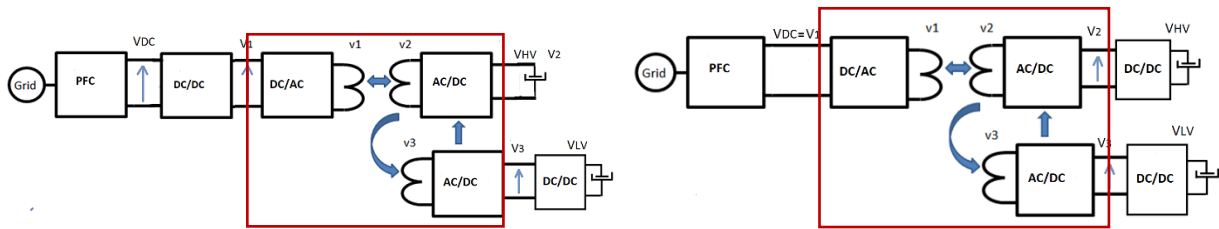


Figure 5-1: The multi-stage conversion structure. a) The voltage is partially regulated by the previous non-isolated DC/DC converter connected at the output of the V_{dc} link for the OBC operating mode. b) The additional stage is connected in cascade with the HV and LV batteries, while the Three-port converter always operates with the nominal voltage V_{DC} .

Another critical aspect of the converter design is the resonant voltage peak. As the voltage is sinusoidal, its peak is an important design parameter influencing the transistor nominal voltage and, consequently, the conduction power losses. The minimum voltage peak corresponds to the full-bridge nominal DC voltage, multiplied by a factor of $\pi/2$. Because of this characteristic, it is interesting to also consider series-connected stages to reduce the nominal voltage of the power devices, depending on the application's voltage level.

Indeed, if the transformer has a high turn ratio between the HV and LV sides, and if the LV side requires a high current level, the multi-level structure should include parallel arrangements. This solution is especially encouraged when the converter design's main objective is to achieve higher efficiencies, power density, and reliability. It allows not only the use of power transistors with smaller voltage and current values, but also the design of a smaller transformer.

However, as the application discussed in this work aimed to include two products in a single box with the same cost or with a reduced total cost, the multi-level structures become less attractive. For this converter specifically, the multi-level structures must include four switches for each bridge connected in parallel or in series to keep the current continuity and the bidirectional power flow. Plus, additional stages to accomplish the battery voltage range, increase the final cost for the integrated product. For the transformer design, on the other hand, this solution will lead to fewer constraints if two transformers replace a single one, allowing better efficiency. A 2-level structure is presented in Figure 5-2. On both high-voltage sides, two full-bridges are connected in series to allow the use of transistors with reduced voltage. On the third side, a parallel arrangement is more beneficial, allowing the use of transistors with 50% the current capacity compared to a single-level structure.

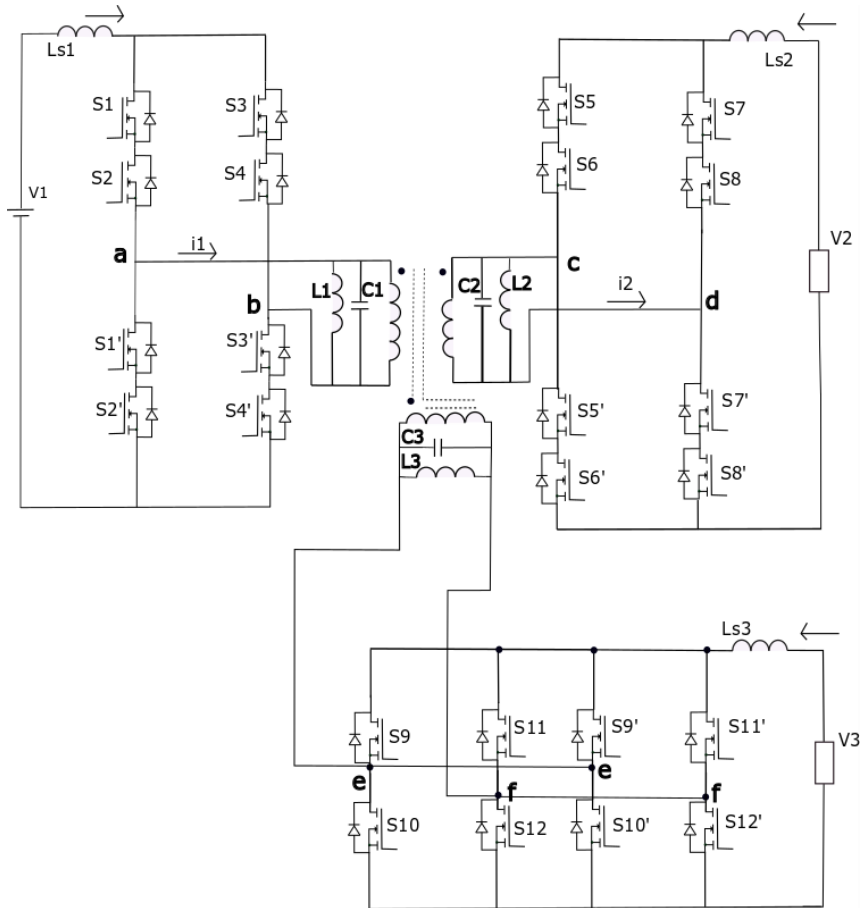


Figure 5-2: A 2-level current-fed resonant converter: Series connected for the HV sides and parallel arrangement for the LV side.

Considering the nominal requirements for the bidirectional OBC and LDC converters, we select commercial transistors of nominal voltages at 400 V, 650 V, 800 V, 900 V, and 1200 V. The next step is to select the semiconductors for our application, able to handle high voltages, medium and high currents. For medium-high switching frequencies, between 200 kHz and 500 kHz, the Insulated-Gate Bipolar Transistors are not suitable because of the increased switching times, even under soft-switching conditions. The MOSFETs, Metal Oxide Semiconductor Field Effect transistors, present a better performance at high and medium frequencies, but have limited voltage range, usually around 650 and 800 V. Nowadays, we can also cite the commercial available wide bandgap (WBG) semiconductors, the Gallium-Nitride (GaN), also called High Electron Mobility Transistor (HEMT), and the Silicon Carbide (SiC) transistors [1]. These two compound materials have higher electron mobility inducing lower conductive resistances, higher bandgap energy than Silicon, allowing the design of power transistors with increased voltage breakdown, and faster switching characteristics. Moreover, in the reverse conduction mode, both transistors present better performances than Silicon devices. The GaN transistors, for example, instead of a body diode, have a small resistance also in the reverse conduction mode; and like the SiC MOSFETs, present zero reverse recovery energy.

There are some differences between those two commercially available devices. For example, the normally-off enhancement HEMT GaN is usually driven with a low voltage between 6 and 10 V, compared to the SiC transistors that require standard voltage level, generally between 15 and 20V for low conduction resistance, with a negative value for turning-off. Sometimes the GaN transistors are commercially available in a cascode mode, also allowing the use of standard drivers. The cascode uses a Silicon MOSFET in series with the GaN transistor that is indirectly driven by the Silicon semiconductor. This configuration usually presents a slower switching behavior and sometimes does not benefit from the fast switching characteristic of the WBG material compared to directly driven GaN transistors, but allows the use of a standard driver. Both structures can be seen in Figure 5-3.

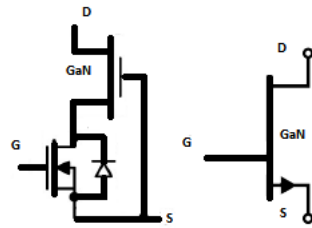


Figure 5-3: Normally-off GaN transistors a) Cascode structure where a Silicon transistor is connected in series with the GaN device allowing a standard driver between 15 and 20V b) enhancement mode direct drive GaN transistor requiring voltages between 6 and 10 V.

Despite the high voltage breakdown potential of the GaN, there are a few numbers of manufacturers offering these devices for high voltage level applications, above 650 V. One of those manufacturers is ViSiC, offering a GaN power module for 1.2kV applications. The vertical growth process to increase the voltage breakdown of the conductive layers can justify the lack of these devices on the market. This process requires an initial high investment for its production and is usually replaced by the growth of the epitaxial layer on silicon or the two-dimensional electron gas process, limiting the device's performance [1].

On the other hand, the SiC MOSFETs are commercially available for high voltage level applications, usually until 1.7 kV. Because of these characteristics, today, the tendency is to replace Silicon IGBT by Silicon Carbide devices, in some applications requiring high voltage and current, such as inverters for automobile and photovoltaic applications. In opposition, GaN devices are preferred when the frequency is high, and the voltage level is limited to approximately 400 V. In Table 5-1 and Table 5-2, we list some commercially available GaN and SiC semiconductors, as well as their voltage and current range. These data are based on some manufacturer's website information and probably will need to be updated soon.




Manufacturer		transphorm		
Part Number	GPXXXX	TPXXXXXXXX	VXXXXXX	EPCXXXXX
Voltage range	100- 650 V	650 V-1200 V	650 – 1200 V*	15- 200 V
Current range	3.5- 150 A	8- 47 A	20- 80 A	3.4- 470 A
Structure	E-mode HEMT	Cascode	Vertical/Cascode	Lateral
Package	Die & pack.	TO247/220 & pack.	Pack. & p. module	Die & pack.
Automotive	No	Yes (*No)	No	Yes

Table 5-1: Normally off GaN power transistors commercially available in nowadays (December 2019). * VisiC announced in 2016 a 1.2 kV power module at the IEEE Energy Conversion Congress and Exposition.






Manufacturer					
Part Number	SCTXXXXX	CXXXXXXXXX	SCT/SCHXXXXX	MSXXXXXX	IMXXXXX/FFXXX
Voltage range	0.65- 1.2 kV	0.9- 1.0- 1.2- 1.7 kV	0.65-1.2-1.7kV	0.7- 1.2- 1.7kV	0.65 -1.2 kV
Current range	12- 95 A	5- 196 A	3.7- 118 A	19- 115 A	4.7- 59 A
Package	HIP247-3/7 H2PAK-2	Die & TO247-3-4/7	TO247-3/4	D3PACK,TO24 7-3, p.module	P.module, TO247-3/4
Automotive	Yes	900 V (TO-247-3)	Yes	Yes	No

Table 5-2: SiC MOSFETs commercially available in nowadays (December 2019).

From the available information, we note that despite the improved performance of the GaN semiconductors, there is an evident difficulty in its fabrication process. Another point is the device validation following some standards. Note that almost all manufacturers can provide qualified SiC MOSFET, according to the automotive rules; however, we do not verify the same for GaN transistors. This can be explained by the existence of different processes for lateral or vertical growth in the fabrication process and different configurations as cascode or enhancement mode transistors, making it difficult to create a single standard procedure. The cascode structure was the first GaN transistor to answer this qualification procedure, maybe due to the similarity in terms of failure modes with the Silicon MOSFET. However, there is still a blank to link the different procedures, which might be answered with time to allow the transistor maturity.

A positive point on the commercially available devices is the different packaging offers: SiC MOSFETs in bare die, TO-247 with 3, 4, and 7 pins or integrated on a power module. It offers different thermal performances, with sometimes reduced stray inductances, such as the devices containing a Kelvin Source, allowing the connection of the Gate-source signal the closest as possible of the semiconductor bare die.

Because of the voltage level and the automotive qualification status, we gave the preference to SiC MOSFETs in the Three-port current-fed parallel resonant converter design.

In the next section, we present some guidelines and characteristics that must be followed for the converter design according to the automotive exigencies.

5.2- Design aspects considering the electrical vehicle rules

In addition to the qualification test for automotive-grade discrete semiconductors, such as the AEC-Q101, used for SiC and GaN transistors classification, the International European standard IEC 61851-1 for the technology and equipment safety information, should be considered in some design aspects of the converter. The main parameter will be the insulation requirement, a key point not only on the converter architecture requiring galvanic isolation, but also the insulation level between the AC grid, the HV, and the LV batteries.

In the equipment safety's language, the definition of basic, double, or reinforced insulations are common: It prevents the user from having access to hazardous voltages with the protection of a fixed or locked cover. The basic insulation connects the accessible conductive parts to earth, so the exposure to the voltage is limited to the overcurrent protection. The double or reinforced insulation should avoid voltage breakdown of the accessible parts.

The OBC and LDC converters are defined as Class II equipment, in which protection against Electrostatic Discharge (ESD) does not rely only on basic insulation, but also in additional safety precautions, such as double or reinforced insulation [2]. Therefore, galvanic isolation becomes necessary between the three main power sources present in the integrated OBC and LDC converters, illustrated in Chapter 4, Figure 4-11.

The basic and the reinforced insulation levels are based on the AC voltage level, between 85- 235 V RMS, for a single-phase connection. Clearance and creepage distances are also defined by the IEC 61851-1 standard and are essential in the converter design.

Note*: The standard IEC61851-1 can sometimes be replaced by the standards IEC 60664, IEC 61140, and IEC60950, depending on the country.

5.3- Converter design

The voltage range and the power consumption of each battery present in the integrated power unit OBC&LDC are available in Table 5-3.

	AC grid	Batteries	HV	LV
Voltage (V_{RMS})	85 – 265	Voltage range	240 – 480 V	10 – 16 V
Frequency (Hz)	50 – 60	Nominal Volt.	450 V	14 V
P_{max} (kW)	7.2 kW	P_{max} (kW)	7 kW	3.5 kW
I_{max} (A_{RMS})	32	I_{DC} max (A)	17.5 A	250 A

Table 5-3: Design requirements considering the batteries and the limits of the AC grid in the single-phase on-board charger.

Based on the available information to charge the HV and the LV batteries, and considering the non-regulation behavior of the Three-port parallel resonant converter, we select the nominal voltage to proceed with the design. If we check the solutions proposed in Figure 5-1, considering the voltage range of the HV battery, it is interesting to keep the additional non-isolated stages as a step-down or a step-up converter only. Given the preference for a non-isolated step-down converter, if the DC link voltage is regulated to be constant during the full battery charging process, the additional stage will need to address the entire voltage range of the battery, as illustrated at below, in Figure 5-4. Typically, for a single-phase PFC converter, the DC link voltage is regulated between 400 and 500 V. In the converter application for the integrated OBC and LDC, we select 480 V to avoid the need for a converter able of stepping-up and stepping-down the input voltage during the battery charging process.

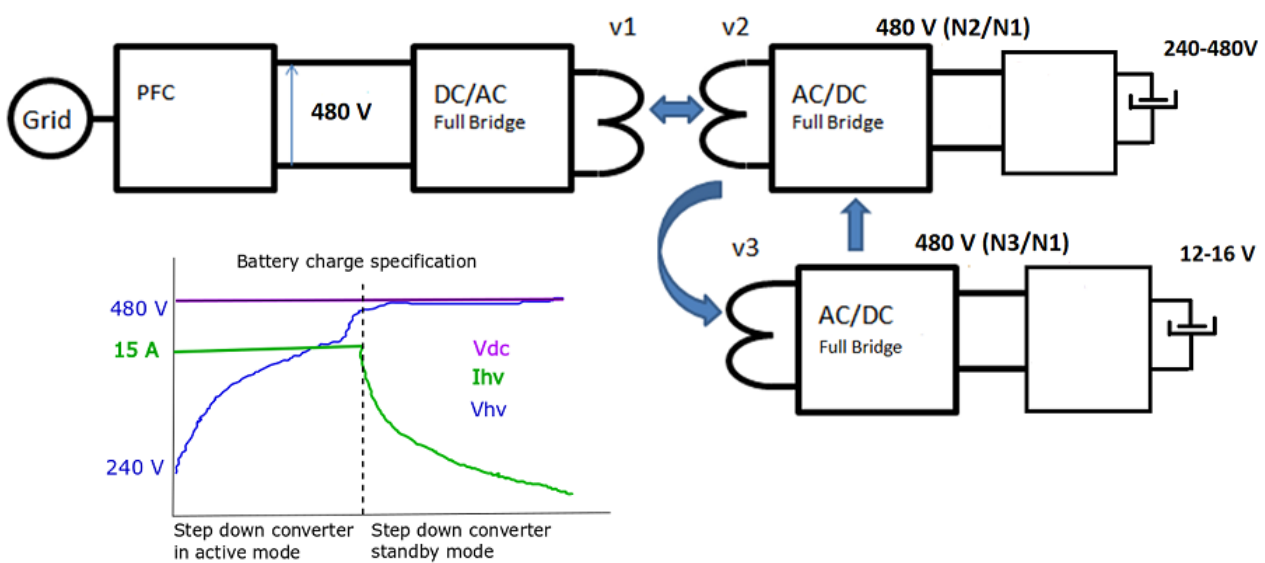


Figure 5-4: The integrated power unit containing the AC/DC converter with the Power factor regulation, followed by the Three-port current-fed converter and the additional non-isolated DC/DC converter.

In the Parallel resonant converter, the selection of appropriate semiconductors is important to increase its performance. The conduction power losses are predominant in the isolated DC-DC converter stage, and small conduction resistances (R_{dsON}) are essential to achieve optimal efficiency. For MOSFETS, R_{dsON} is proportional to V_{ds} , and that is why we must minimize the resonant voltage peak over the devices.

In particular, for our converter, with a V_{dc} voltage bus around 480 V, we can limit the voltage peak over the high side transistors to 900 V, making a SiC MOSFET of 1.2 kV the more appropriated transistor. In the low voltage side, considering the term N_3/N_1 and the high current, MOSFETS with a nominal voltage higher than 80 V may have increased R_{dsON} resistance and are hence not so convenient for the application. Using a security margin of 25% for the V_{ds} nominal voltage, 60 V and 45 V are the maximum voltage peaks allowed for 80 V and 60 V V_{ds} nominal devices, respectively. In Table 5-4, there is the resume of the possible voltage ratios in the implemented design.

Voltage ratio N_1/N_3	30 – 20
V_{DC} link (V)	480 V
V_3 (V)	16 – 24 V
V_3 peak + 25%	38 – 57 V

Table 5-4: The Vdc link voltage adapted for the OBC and LDC converters. $V_{dc} = 480$ V, 900 Vpeak on the primary side, allowing the use of 1.2 kV power transistors. For the LV side, transistors with a nominal voltage of 40 and 60 V are preferred.

Although we could use the GaN transistors and, more specifically, the EPC GaN transistors for 80V/90 A applications, we had preferred to integrate only a different device technology, the SiC for high voltage side and Si MOSFETs for low voltage side.

Taking into consideration the possibility of coupling the DC side inductors of the V_{DC} , HV and LV sides, and checking the rules for the OBC and LDC converters integration, cited in section 5.2, the clearance and creepage necessary distances to accommodate the three windings on the same magnetic core are considerable. It consequently complicates the implementation of this configuration in practice. For this reason, we opted for three single inductors.

The design procedure consists of first select the resonant frequency and the nominal voltages connected to the converter ports. Remembering that the transistors are switched during the zero voltage crossing of the resonant voltage and remembering that it does not depend on the current load, the parallel inductor needs to store enough current to charge and discharge the equivalent parallel capacitances. Therefore, during steady-state, the ZVS conditions are related to the switching frequency, depending only on the passive elements.

Using the equivalent circuit below, where one AC load is connected to one of the ports, the ZVS condition during steady-state can be considered according to the minimum current “ i_{ab} ” in Figure 5-5. This current must keep its circulation direction unaltered during the transistors switching. It must also have a minimum value to discharge the capacitances in parallel with the switches, and the additional resonant parallel capacitance, ensuring the bias of the body diode to zero voltage switching. The turning-off occurs later, to always ensure a path to the current circulation and avoid current spikes. $i_T(t)$ represents the sum of the currents in the transformer windings:

$$i_{ab}(t) = i_L(t) + i_C(t) + i_T(t) = i_L(t) + i_C(t) + [i_{T1}(t) + i_{T2}(t) + i_{T3}(t)] \quad (1)$$

$$i_{ab}(t) \cong i_L(t) + i_C(t)$$

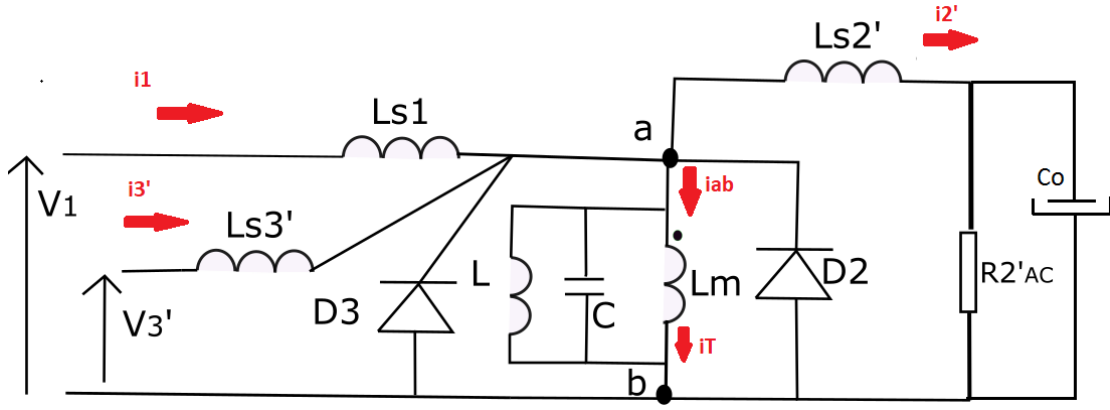


Figure 5-5: Current path before the turning-on of the switches S2 and S3.

Using the solutions for the current over the resonant inductor and over the resonant capacitor from Chapter 3, the equivalent current i_{ab} is:

$$i_{ab}(t) = K \left[\frac{C L W_r^2 - 1}{L W_r} \right] \sin(W_r t) + I_{L_{Peak}} [C L W_r^2 - 1] \cos(W_r t) + \frac{K}{L} t \quad (2)$$

$$u(t) = I_{L_{Peak}} L W_r \sin(W_r t) + K [1 - \cos W_r t]$$

The ZVS condition during steady state occurs if:

1° condition: $u(0) = 0$

2° condition: $i_{ab}(0) < 0$

$$I_{L_{Peak}} [C L W_r^2 - 1] \cos(W_r t) < 0 \rightarrow C L W_r^2 < 1 \rightarrow W_r < \frac{1}{\sqrt{C L}}$$

Hence, during steady-state, if the switching frequency is smaller than the resonant frequency, the current lags the capacitor voltage, as discussed in Chapter 3. An additional parameter may be added to choose the values of L and C, in complement to the resonant frequency. This additional parameter can be associated with a quality factor Q, depending on the load. As the switching frequency is constant, the current in the parallel inductor does not vary with the load, being important to ensure its impedance higher than the nominal equivalent load.

$$Q = \frac{R_{Load}}{Z_{Parallel}} < 1, R_{Load} = \frac{V_{in}^2}{P_{IN_{MIN}}} \quad (3)$$

Remembering the reasons why we had opted for a converter design without coupling the three DC side inductors, for simplification, we can define a ratio between the DC side and the parallel inductor values, F_L in (4). After selecting the parallel inductor using the expressions for the resonant frequency and the quality factor together (3), we start testing different values for the DC side inductor. We start with the factor F_L equal to one and then increasing it until the current ripple on the DC side, or the resonant voltage peak in (5) from Chapter 3, satisfies our requirements.

$$F_L = \frac{L_S}{L} \quad (4)$$

$$K = \left(\frac{V_1}{L_{S1}} + \frac{V_2}{L_{S2}} + \frac{V_3}{L_{S3}} \right) \frac{L L_S}{(L_S + L)} \quad V_{peak} = \frac{\pi(V_1 + K)}{2} \quad (5)$$

The current ripple on the DC side can be evaluated by using the voltage-time balance over the series inductance, depending on twice the converter switching frequency:

$$V_1 - u(t) = L_{S1} \frac{di_1(t)}{dt} \rightarrow V_1 - V_{peak} = L_{S1} \frac{\Delta I_1}{\frac{T}{4}} \rightarrow L_{S_{MIN}} = \frac{T(V_1 - V_{peak})}{4 \Delta I_1} \quad (6)$$

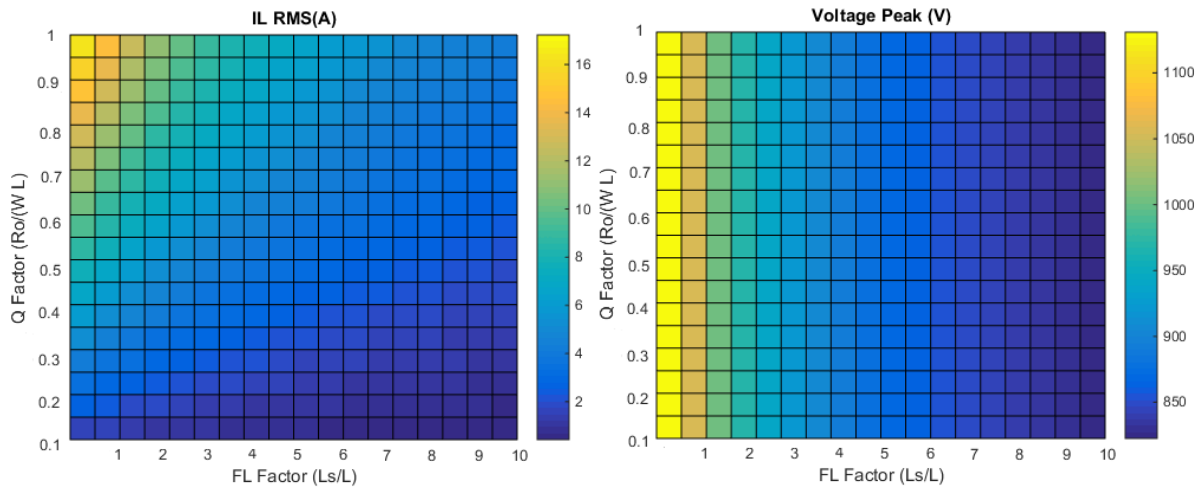


Figure 5-6: Resonant voltage peak and RMS current in the parallel resonant inductance depending on the factors Q and FL .

	Range	Nominal condition
DC link voltage (V)	450 – 500	480
High voltage side (V)	240 – 480	480
Low voltage side (V)	10 – 16	20
Output power 1° port (kW)	+7 kW/ -3.5 kW	7 kW
Output power 2° port (kW)	+3.5 kW/ -7 kW	3.5 kW
Output power 3° port (kW)	+3.5 kW / -3.5 kW	3.5 kW
Insulation voltage level (kV)	-	5.7
Resonant frequency (kHz)	-	200
Efficiency (%)	-	≥ 96

Table 5-5: Design requirements for the Three-port current-fed parallel resonant converter.

In order to simplify this design procedure, we evaluate the arguments from the previous paragraph in an optimization routine. The design consists of first to select the proper switching frequency and nominal voltage. For different Q factors and ratios F_L (4), we evaluate the resonant voltage peak to use a semiconductor device with a maximum nominal voltage of 1200 V, keeping a security margin of 25%. These steps allow having the minimum value of the passive elements. To avoid the influence of the DC side inductor on the resonating cell, we can keep the factor F_L greater than one. Taking advantage of SiC MOSFETS of 1200 V, F_L was approximated by 2. The factor Q depends on the output load, and it can be chosen close to 0.2 to attempt a reasonable performance for loads between the maximum output power until 20% of this nominal load, as shown in Figure 5-6.

$$F_r = 200 \text{ kHz}, V_{in} = 480 \text{ V}, P_{in} = 7 \text{ kW}$$

$$F_L = \frac{L_S}{L} = 2$$

$$N = \frac{V_{HighSideMAX}}{V_{LowSideMAX}} = \frac{900}{37} \cong 24 \cong \frac{V_{in}}{V_{LV_{in}}} \text{ (25 \% of margin)}$$

$$R_{Load} = \frac{V_{in}^2}{P_{IN}} = \frac{480^2}{7 \text{ kW}} = 32.9 \Omega, Q = \frac{R_{Load}}{Z_{parallel}} = 0.15$$

$$L = \frac{R_{Load}}{2\pi F_r Q} = \frac{32.9}{2\pi (200k) 0.5} = 52.4 \mu H$$

$$C = \frac{1}{L (2\pi F_r)^2} = \frac{1}{52.4\mu (2\pi 200 k)^2} = 12 \text{ nF}$$

$$L_S = \frac{L}{F_L} = 104.8 \mu H$$

$$F_r = \frac{1}{2\pi \sqrt{CL}} = 200.8 \text{ kHz}, \frac{1}{2\pi \sqrt{\frac{L_S+L}{L_S L C}}} = 246 \text{ kHz}$$

$$L_{S1} = 3 L_S = 314.4 \mu H$$

$$L_1 = 3 L = 157.2 \mu H$$

$$C_1 = \frac{C}{3} = 4 \text{ nF}$$

$$I_{1IN} = \frac{P_{outMax}}{V_{INMin}} = \frac{7.2 \text{ kW}}{460 \text{ V}} = 15.65 \text{ A}$$

$$K = \left(\frac{V_1}{L_{S1}} + \frac{V_2}{L_{S2}} + \frac{V_3}{L_{S3}} \right) \frac{L L_S}{(L_S+L)} = \left(\frac{3 \times 480}{104.8 \mu} \right) \frac{157 \mu \times 314 \mu}{(471.6 \mu H)} = 160$$

$$i_1 = I_{1IN} + i_{1AC} = I_{1IN} + I_{L_{Peak}} \sin(W_r t)$$

The current and voltage stresses in the power switches are calculate below:

$$I_{TRMS} = \sqrt{\frac{1}{T} \int_0^T [i_{1IN}]^2 dt} = \frac{I_{1IN}}{\sqrt{2}} = 11.13 \text{ A}$$

$$I_{LP\text{Peak}} = \frac{V_{DS\text{Max}}}{W_r L_1} = 4.73 \text{ A}$$

$$I_T = \frac{I_{1IN}}{2} = 7.82 \text{ A}$$

$$V_{DS\text{Max}} = \frac{\pi(V_{in+K})}{2} = 933 \text{ V}$$

At the low voltage side:

$$V_{DS\text{MaxLV}} = \frac{V_{DS\text{Max}}}{N_{13}} = \frac{933 \text{ V}}{24} = 39 \text{ V}$$

$$I_{TLV} = N_{13} I_T = 102.96 \text{ A}, \quad I_{TRMSLV} = I_{TRMS} N_{13} = 133.56 \text{ A}$$

For the DC side inductors:

$$I_{LS\text{AV}} = I_{1IN} = \sqrt{\frac{1}{T} \int_0^T [(I_{1IN} + I_{LP\text{max}} \sin(W_o t))^2] dt} = 15.65 \text{ A}$$

$$I_{LS\text{RMS}} = \sqrt{\frac{1}{T} \int_0^T [(I_{1IN} + I_{LP\text{max}} \sin(W_o t))^2] dt} = I_{1IN} + \frac{I_{LP\text{Max}}}{\sqrt{2}} = 15.65 + 3.34 = 19 \text{ A}$$

The voltage stress in the resonant capacitor is calculated as:

$$V_{\text{MaxStress}} = V_{DS\text{Max}} = \frac{\pi(V_{in+K})}{2}$$

From the maximum voltage, the current peak in the parallel resonant capacitor is:

$$I_{CP\text{max}} = C_p \frac{\Delta V_{DS\text{max}}}{\Delta t} = C_p \frac{\Delta V_{DS\text{max}}}{\left(\frac{0.25}{F_{sw\text{max}}}\right)} = 4.92 \text{ A}$$

The parasitic capacitances from the MOSFETs are in parallel with the main resonant capacitance in the equivalent schematic, and for this reason, the additional capacitances are calculated as:

$$C_{P\text{addHV}} = C_{res} - 2 \times C_{OSS} = 4.08 \text{ nF} - (2 \times 60 \text{ pF}) = 3.96 \text{ nF}$$

$$C_{P\text{addLV}} = C_{res} - 2 \times C_{OSS} = 2.35 \text{ uF} - (2 \times 2.2 \text{ nF}) = 2.35 \text{ uF}$$

Table 5-6 shows the converter design specification for the conditions presented above.

	Port 1	Port 2	Port 3
Nominal voltage (V)	480	480	20
Transf. turns ratio	24	24	1
Resonant capacitance (Cpx)	4 nF	4 nF	2.3 μF
Parallel inductor (Lpx)	157 μH	157 μH	0.27 μH
Series inductor (Lsx)	314 μH	314 μH	0.55 μH
Input cur. RMS and peak values (A)	16 A _{RMS} / 20 A	16 A _{RMS} / 20 A	188 A _{RMS} / 245 A
ILp RMS and peak values (A)	3.35 A _{RMS} / 4.7 A	3.35 A _{RMS} / 4.7 A	81 A _{RMS} / 113 A

Maximum voltage peak (V)	933 V	933 V	39 V
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Table 5-6: Design specification of the Three-port current-fed resonant converter

The Three-port current-fed parallel resonant converter is simulated for the OBC, LDC, and OBC&LDC operating modes. In Table 5-7, the converter parameters are presented for a resonant frequency of 200 kHz, with a maximum output power of 7 kW in the OBC mode and 3.5 kW in the LDC mode.

Parameters	Value
Switching frequency	180 kHz
Output power HV side	7.0 kW
Output power LV side	3.5 kW
Output power Vdc side	7.0 kW
Nominal voltage Vdc	480 V
Nominal voltage VHV	480 V
Nominal voltage VLV	20 V
Transformer turns ratio N1:N2:N3	24 : 24 :1
Resonant cell Vdc side (Lp1, Cp1)	157 μ H / 4.4 nF
Resonant cell VHV side (Lp2, Cp2)	157 μ H / 4.4 nF
Resonant cell VLV side (Lp3, Cp3)	0.27 μ H / 2.32 μ F
DC side inductor Vdc side	314 μ H
DC side inductor VHV side	314 μ H
DC side inductor VLV side	0.54 μ H

Table 5-7: The converter design specification.

The first case study is based on the simultaneous operating modes of OBC and LDC when the voltage Vdc charges both batteries connected to the HV and LV sides. The maximum power coming from the electrical grid corresponds to 7kW, shared between the batteries. The three full-bridges are controlled at the same frequency, and an overlap of 100 ns is added between the high and low voltage sides command to avoid an open-current situation.

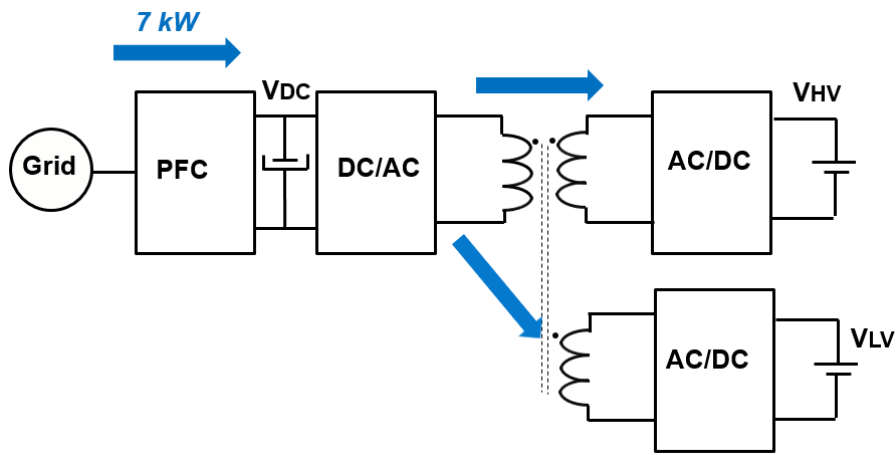


Figure 5-7: Power flow when both batteries HV and LV are being charged.

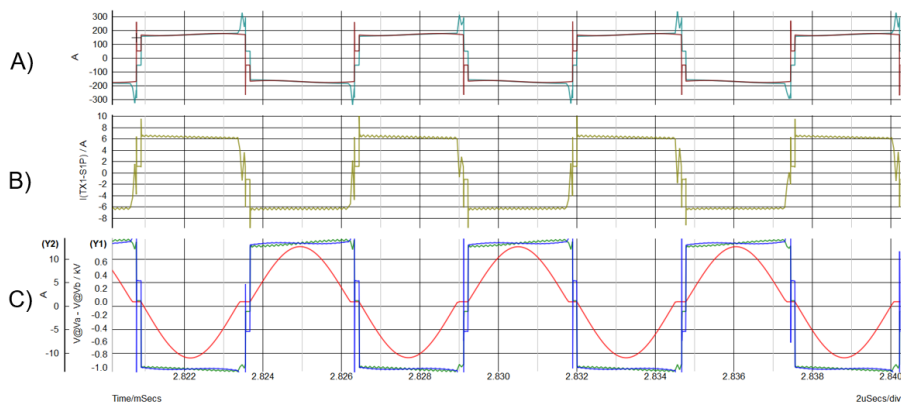


Figure 5-8: A) Current on the third side of the transformer, after and before the resonating cell. B) Current on the second side of the transformer, after and before the resonating cell. C) Sinusoidal Voltage V_{ab} and the current on the primary side of the transformer. V_{HV} power $\cong 3.72$ kW, V_{LV} power $\cong 3.24$ kW.

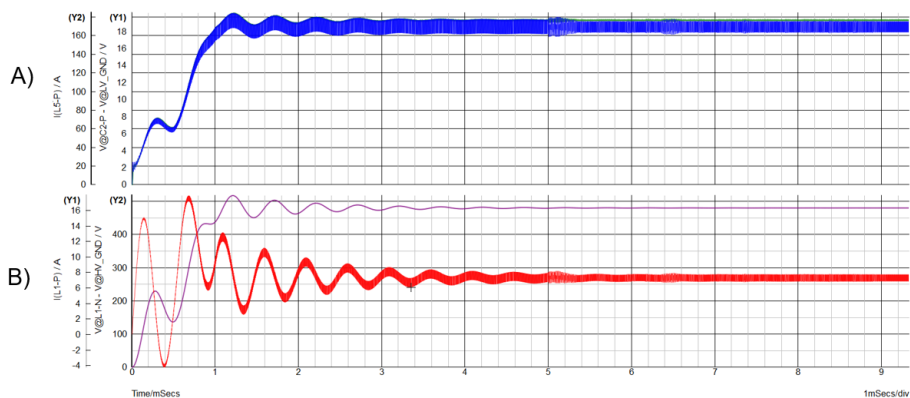


Figure 5-9: A) Voltage V_{LV} and current I_{LV} charging the LV battery. B) Voltage V_{HV} and current I_{HV} charging the HV battery. V_{HV} power $\cong 3.72$ kW, V_{LV} power $\cong 3.24$ kW.

The current spikes in the transformer windings occur during the turning-on of the transistors and the overlap time. The current is shared between the two arms in the same full-bridge before changing its signal. The other power flow situations are presented in Section 5.7.1. The simulations presented

show the converter operation with all required power flow directions. Due to the symmetry of the converter, zero voltage switching is present in all modes. In the next section, we analyze the effect of the transformer's parasitic elements on the converter behavior.

5.4- Parasitic elements affecting the converter operation

In the previous section, we had present the converter behavior for its different operational modes, but the simulation results had not yet considered enough parasitic elements. In this chapter, we study the effect of some parasitic elements that are naturally present in the converter and how to minimize their effects.

The main parasitic elements are from the transformer prototype. Despite the efforts to minimize the leakage flux, leakage inductance cannot be disregarded because of the high number of interconnections between the three PCBs and the high number of vertical electrical vias used in the prototype. Another physical explanation for the increased leakage inductance is the winding length that physically connects the transformer to the power boards. This length was relatively long because the prototypes were not integrated on the same PCB, requiring a higher conductor length to make the connection between the four boards possible.

Another element perturbing the converter behavior is the capacitance between the layers of the transformer. Unlike a non-planar magnetic component, in the planar technology, the shared area between different conductor layers increases the equivalent capacitance. Indeed, the insulation material used in the multi-layer PCB has a significant dielectric constant contributing to this phenomenon. As discussed in Chapter 4, minimize the leakage inductance had resulted in increased capacitances, and therefore their effects need to be considered.

The equivalent circuit in Figure 5-10 includes the parasitic elements in the Three-port parallel resonant converter.

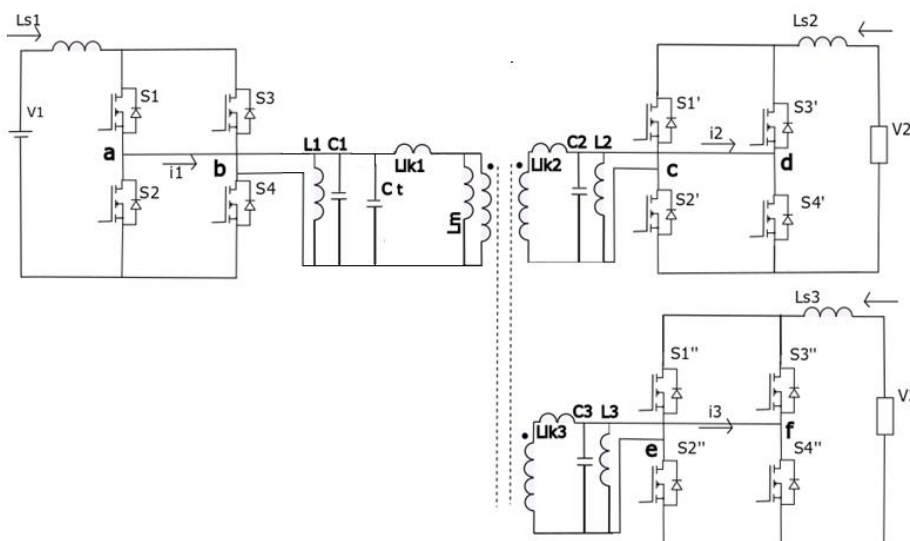


Figure 5-10: The Three-port current-fed parallel resonant converter with the parasitic elements from the transformer prototype.

To justify the circuit presented in Figure 5-10, we first consider the model proposed for the planar transformer in Chapter 4. Inter and intra-winding capacitances are associated with the resistive and inductive elements, as shown in Figure 5-11, and the converter's resonant cells are placed in parallel to each terminal. We simplify the circuit by transforming the parasitic elements from a Δ to a Y configuration, as shown in Figure 5-12. The equivalence between both circuits can be verified in Figure 5-13, with the impedance matching.

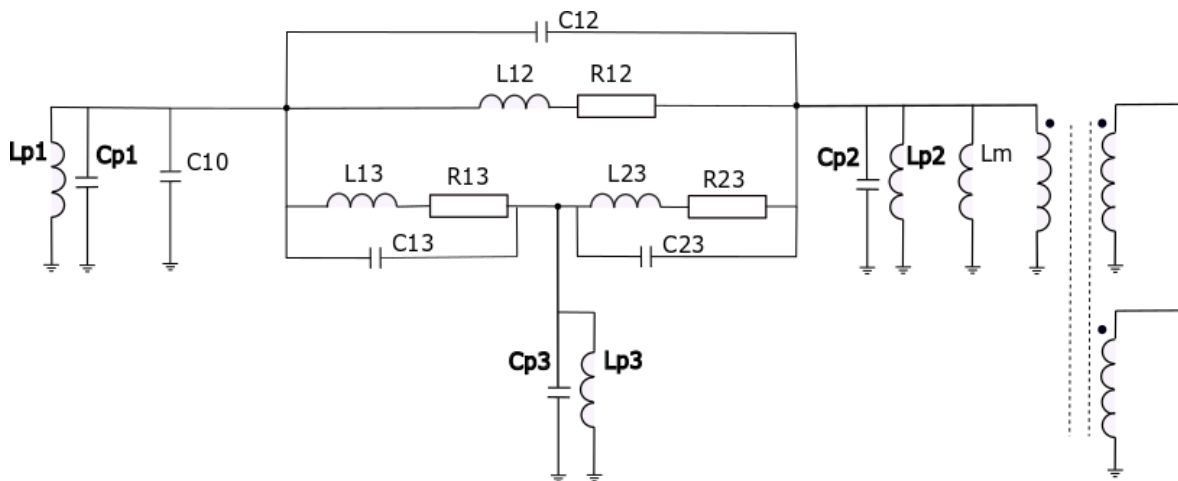


Figure 5-11: Transformer equivalent circuit obtained in Chapter 4 with parallel resonant cells.

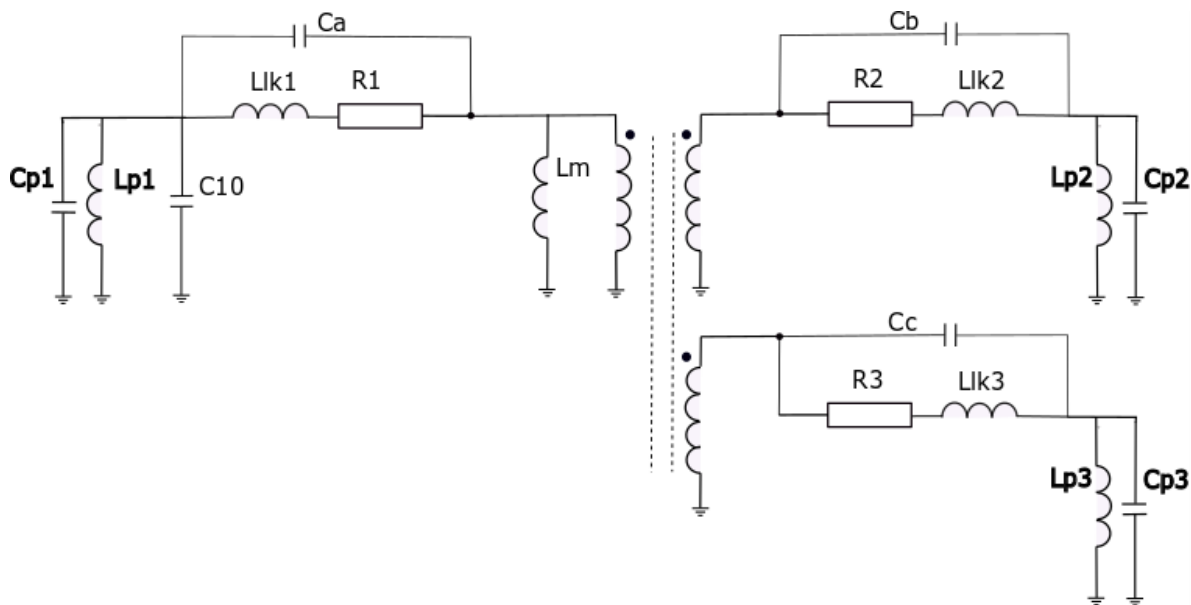


Figure 5-12: Transformer equivalent circuit in the Y configuration with parallel resonant cells.

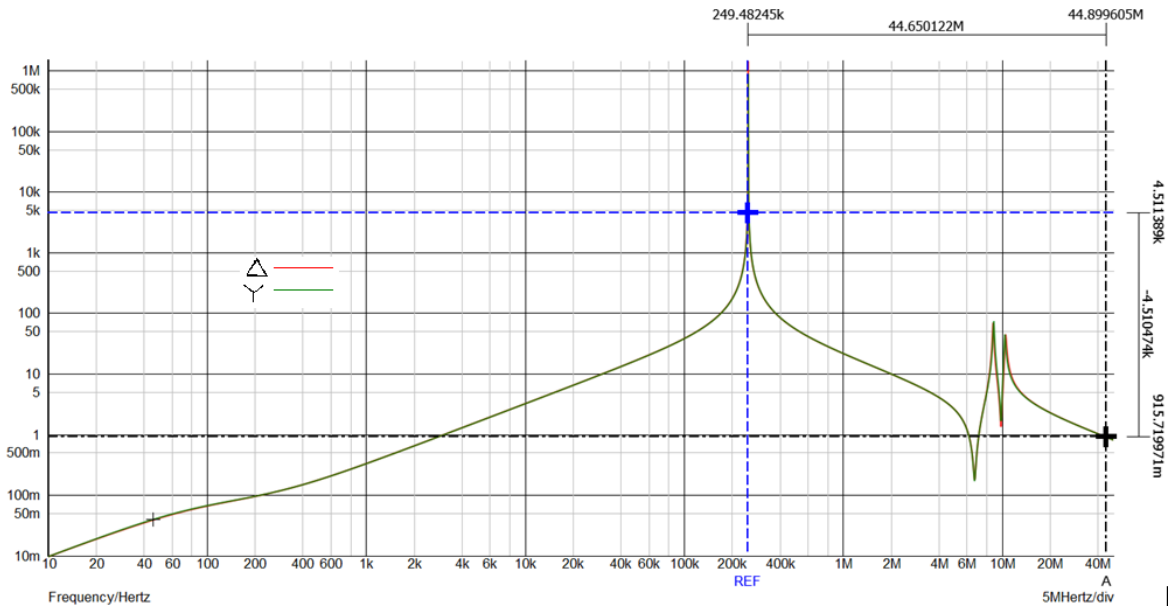


Figure 5-13: Impedance analysis comparing the Δ and Y configurations containing the parasitic capacitances.

The stray capacitances in the circuit move the converter spectrum to the left side, reducing the resonant frequencies showed in the impedance analysis. By representing inter and intra-winding capacitances by a single capacitance remained to the transformer's primary side, we simplify the equivalent circuit in the parasitic oscillations analysis. However, we may introduce an error in the result. For our transformer prototype, this error can be verified in Figure 5-14. The parasitic capacitances represented in Figure 5-12 are replaced by a single capacitance C_t , and we note a difference of approximately 20 kHz (8%) in the converter's first resonant frequency. For parasitic oscillations analysis in our application, this error is acceptable, and we proceed with the equivalent circuit in Figure 5-10.

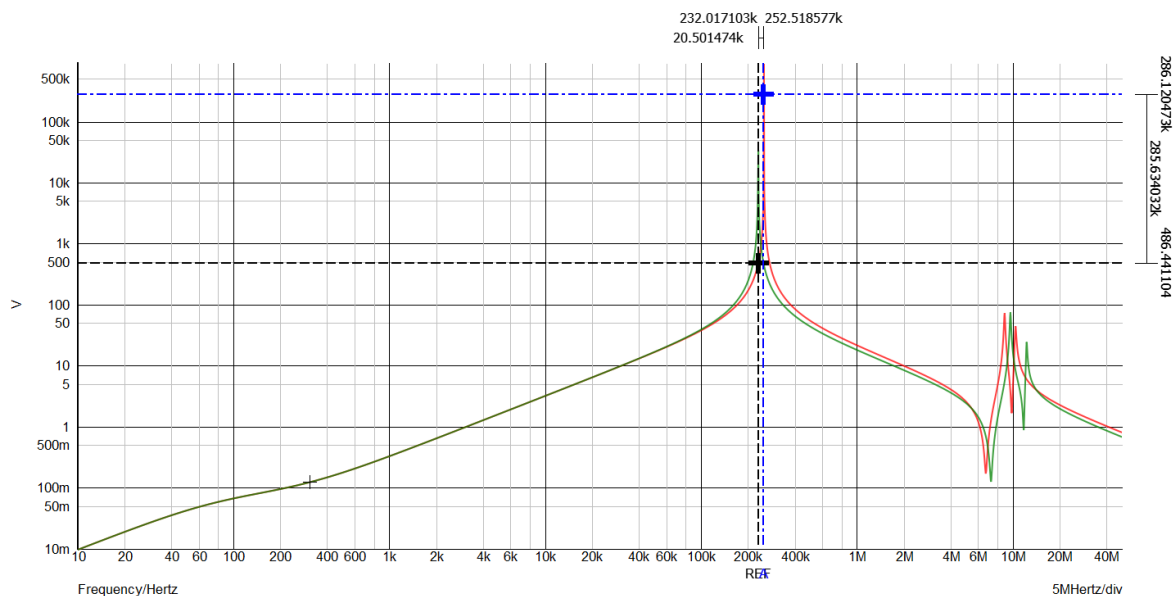


Figure 5-14: Impedance analysis comparing the effect of a single capacitance C_t remained to the primary side representing the stray capacitances, and the effects of each capacitance.

Using the parasitic elements found in Chapter 4, and described in Table 5-8, the converter behavior can be verified with time-dependent simulations.

Parameter	Value
L_{12}	149 nH
L_{13}	310 nH
L_{23}	311 nH
L_m	4.57 mH
C_t	2.53 nF

Table 5-8: Parasitic elements of the transformer in the Δ configuration, presented in Figure 5-10.

Figure 5-15 shows a high parasitic oscillation between the series leakage inductance and the parallel equivalent capacitance. The parasitic elements add oscillations to the current and voltage waveforms on the AC side, and the amplitude of these oscillations is proportional to the current load. The worst-case occurs at the beginning of the battery charging process when the voltage is minimum, and the current corresponds to the maximum power.

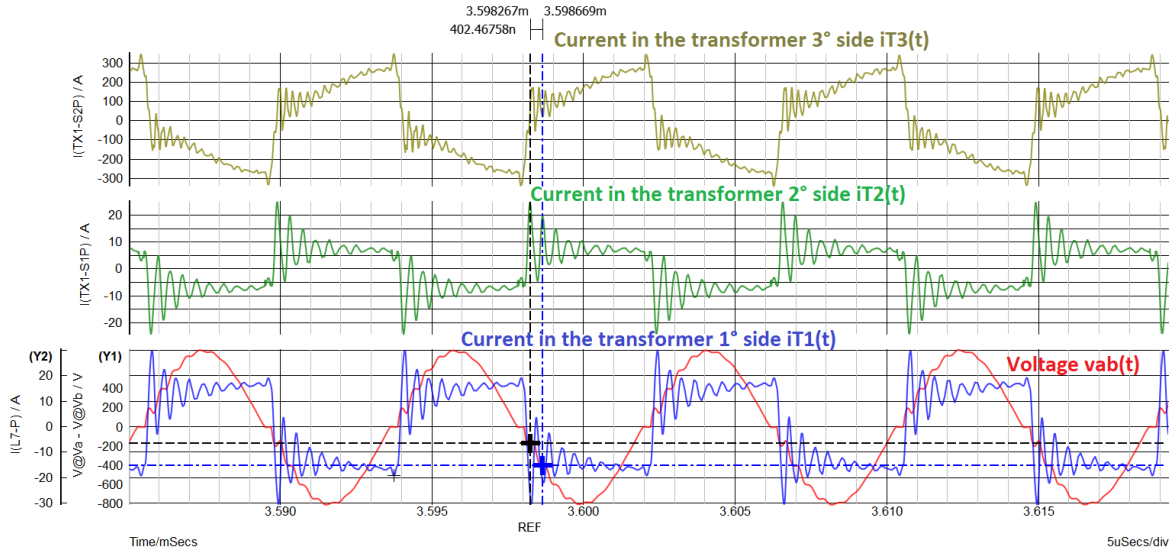


Figure 5-15: Current and voltage waveforms in the OBC&LDC operational mode.

The oscillation creates current spikes superposed to the original current and voltage waveforms. If these oscillations are not appropriately damped, it can interfere in the zero voltage crossing detection. Another effect is that the equivalent capacitor from the transformer, C_t , will also interfere with the main resonant frequency of the converter. The equivalent capacitance of the converter increases, $C_{eq} = C_t + C_1 + C_2' + C_3'$, consequently its resonant frequency decreases, where L_p is the equivalent parallel resonant inductance.

$$F_{resonant} = \frac{1}{2\pi\sqrt{(L_p)(C_p + C_t)}} \quad (7)$$

$$F_{Parasitic1} = \frac{1}{2\pi\sqrt{(l l k_1)(C_p + C_t)}} \quad (8)$$

In the frequency domain analysis, we identify only the two first frequencies, as shown in Figure 5-16.

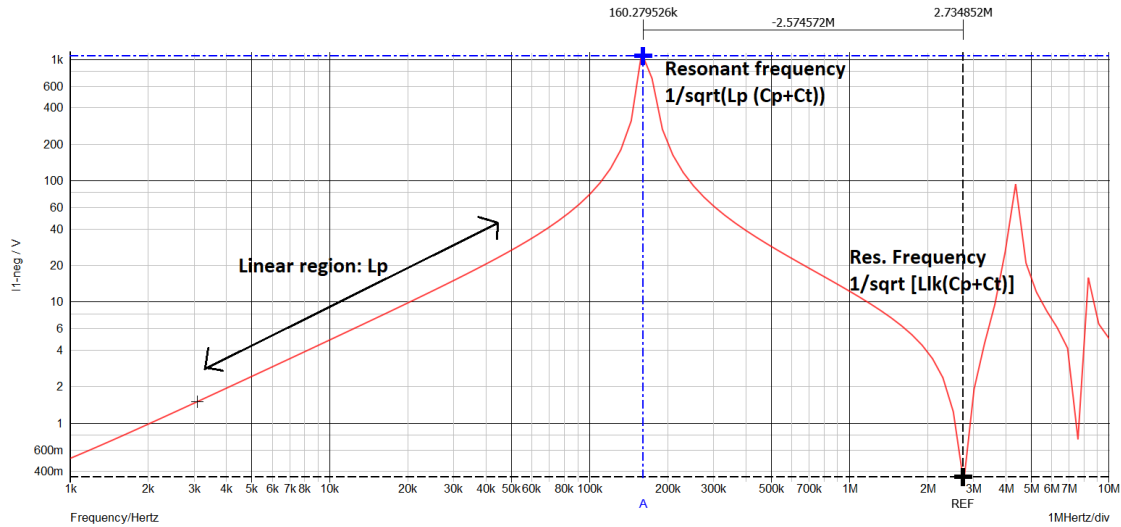


Figure 5-16: Impedance of the equivalent circuit in the frequency domain.

In Figure 5-16, in low, medium frequency, the linear region represents the parallel resonant inductance. The first resonant peak occurs for a lower frequency because of the additional parasitic capacitor from the planar transformer, C_t . Thus, $C_t + C_p$ oscillates with the equivalent parallel inductor, L_p . The second resonant peak, which is negative, occurs between the equivalent capacitance and the leakage inductance viewed from the winding, generating the parasitic oscillations.

Although the parasitic oscillations do not seem to represent a problem for the converter's switching behavior, it can generate some instability in the control strategy, and reduce the performance of the SiC transistors. Damping these oscillations require additional elements to perform a filter. We will take the OBC operating mode as an example, and Figure 5-17-A shows the equivalent circuit. From the primary side, the magnetizing inductance does not interfere in the oscillations, so we use the representation in Figure 5-17-B, with a damping circuit connected in parallel to the input.

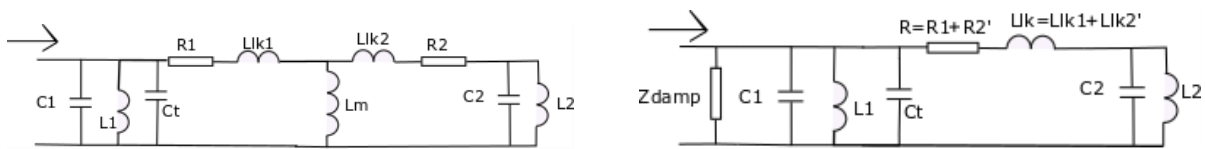


Figure 5-17: A) Equivalent circuit containing the parasitic elements from the transformer and the resonant elements in the OBC operating mode. B) Equivalent circuit with additional damping circuit viewed from the primary side.

The equivalent impedance can be evaluated by:

$$Z_1 = s L_1 // \frac{1}{s(C_1 + C_t)}; \quad Z_2 = R + s(L_{lk}) + [s L_2 // \frac{1}{s(C_2)}]$$

$$Z_1 = \frac{sL_1}{s^2 L_1 (C_1 + C_t) + 1}; \quad Z_2 = \left[\frac{(s^2 L_2 C_2 + 1)(sL_{lk} + R) + sL_2}{s^2 L_2 C_2 + 1} \right]$$

$$Z_{eq} = \frac{\left[\frac{Z_1 Z_2}{Z_1 + Z_2} \right] Z_{damp}}{\left[\frac{Z_1 Z_2}{Z_1 + Z_2} + Z_{damp} \right]}$$

An RLC circuit can be applied to damp the oscillations:

$$Z_{damp} = \frac{s^2 L_a C_a + s R_a C_a + 1}{s C_a}$$

$$Z_{eq} = \frac{s L_1 [(s^2 L_2 C_2 + 1)(s L_{lk} + R) + s L_2] [s^2 L_a C_a + s R_a C_a + 1]}{[s^2 C_a L_1 + (s^2 L_a C_a + s R_a C_a + 1)[s^2 L_1 (C_1 + C_t) + 1]] [(s^2 L_2 C_2 + 1)(s L_{lk} + R) + s L_2] + s L_1 (s^2 L_2 C_2 + 1)(s^2 L_a C_a + s R_a C_a + 1)}$$

The zeros of the above expression are the resonant frequencies and the parasitic oscillation. The equivalent series resistances present in the transformer, and in the transistors naturally damp the parasitic oscillations present in the converter, as verified in Figure 5-15. If this resistance is small, the parasitic oscillation can be approximated by a second-order term:

$$s = \frac{-R}{2L_{lk}} \pm \sqrt{\frac{R^2}{4L_{lk}^2} - \frac{L_{lk} + L_2}{L_{lk} C_2 L_2}}$$

Figure 5-18 shows the minimization of parasitic oscillations with a RLC filter.

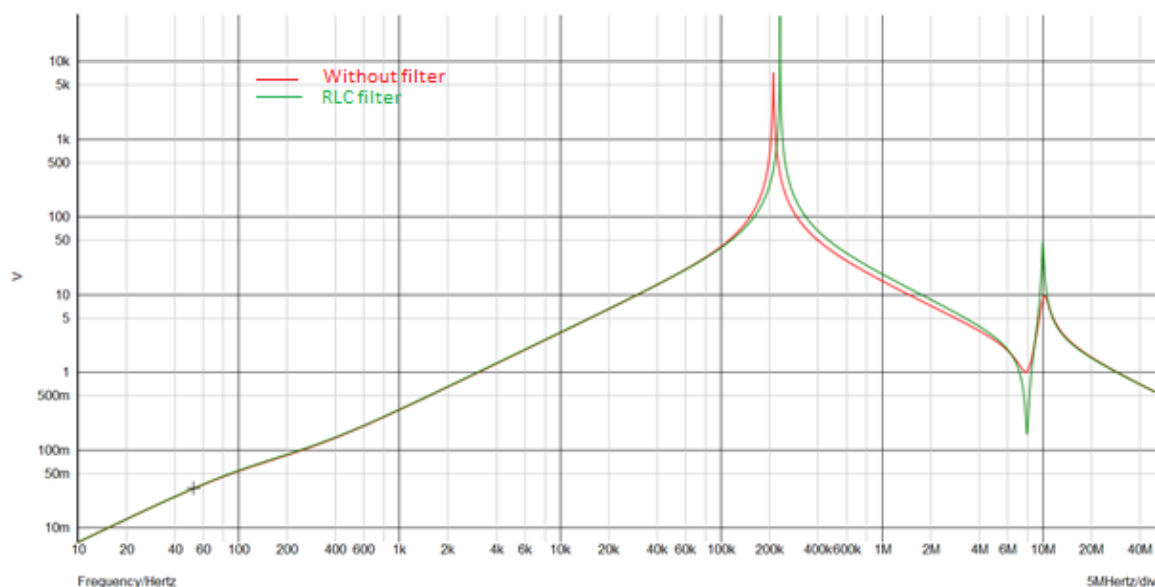


Figure 5-18: The equivalent impedance viewed from primary side with and without an RLC filter ($C_a = 1nF$, $L_a = 490nH$, $R_a = 40\Omega$).

Although increasing the capacitance C_a damp the oscillations, it is not appropriate because the resonant frequency will be reduced, leading the operational switching frequency decrease to avoid hard-switching.

In Figure 5-19, we compare the transformer currents in primary and secondary sides, as well as the resonant voltage V_{ab} , with and without damping circuit for the parasitic oscillations. The leakage inductance is 315 nH for each side and the parasitic capacitance, 2.5 nF. The additional damping circuit consists in an RLC circuit ($R_a = 10 \Omega$, $L_a = 100nH$ and $C_a = 1nF$).

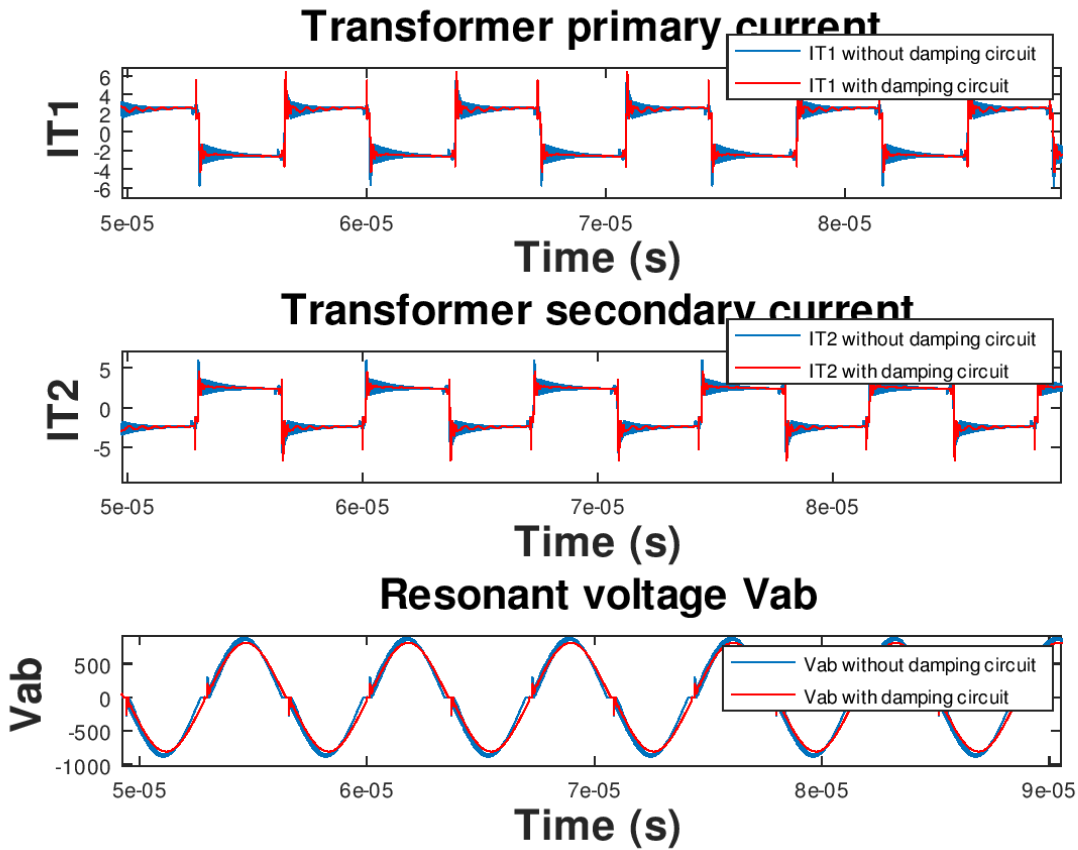


Figure 5-19: Current in the primary and in the secondary sides of the transformer, i_{T1} , and i_{T2} , respectively. Resonant voltage V_{ab} measured on the primary side of the transformer. The blue lines are the measured data with the parasitic oscillations, and the red line is the result obtained with the additional damper circuit. The damping circuit is a RLC ($R_a = 200\Omega$, $L_a = 6\mu\text{H}$ and $C_a = 1\text{nF}$)

5.4.1- Simulation of the converter with parasitic elements from the transformer

In this section, simulations of the converter are realized with the transformer parasitic elements, the spice model of the real switches integrated on the prototype, and the damping circuit. The simulation parameters are presented in Table 5-9.

Parameters	Value
Switching frequency	180 kHz
Output power HV side	7.0 kW
Output power LV side	3.5 kW
Output power Vdc side	7.0 kW
Nominal voltage Vdc	480 V
Nominal voltage VHV	480 V
Nominal voltage VLV	20 V
Transformer turns ratio N1:N2:N3	24 : 24 :1
Resonant cell Vdc side (Lp1, Cp1)	157 μH / 4.4 nF
Resonant cell VHV side (Lp2, Cp2)	157 μH / 4.4 nF
Resonant cell VLV side (Lp3, Cp3)	0.27 μH / 2.32 μF
DC side inductor Vdc side	314 μH

DC side inductor VHV side	314 μH
DC side inductor VLV side	0.54 μH

Table 5-9: Parameters of the converter used in the simulations.

In Figure 5-20, for the OBC operating mode, the leakage inductance is considered equally distributed between the transformer primary and secondary sides, and the parasitic oscillation occurs at 4.25 MHz.

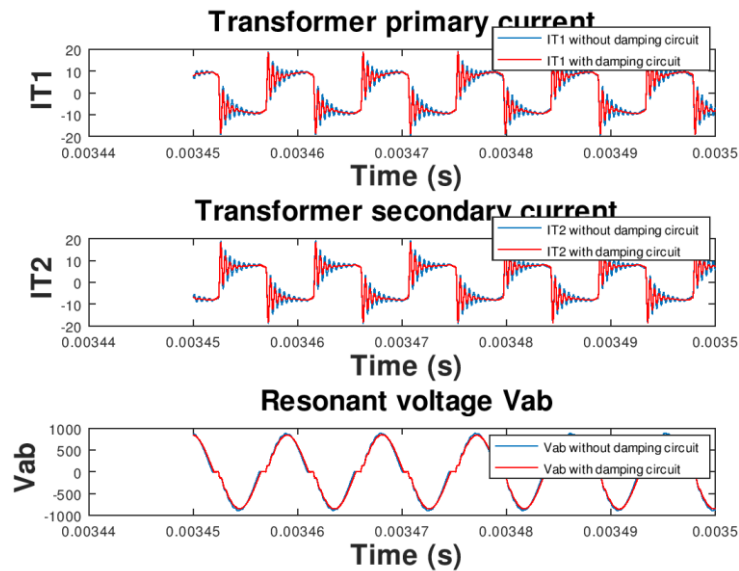


Figure 5-20: Primary and secondary currents in the transformer, as well the resonant voltage comparison: with and without a damping circuit for parasitic oscillations around 2.32 MHz ($L_a = 5\mu\text{H}$, $C_a = 1\text{nF}$ and $R_a = 70\ \Omega$) (OBC operating mode $P = 4\ \text{kW}$).

When we minimize the leakage inductance, the parallel resonant components can be omitted in the low voltage side and placed only in both high voltage sides, as in Figure 5-21.

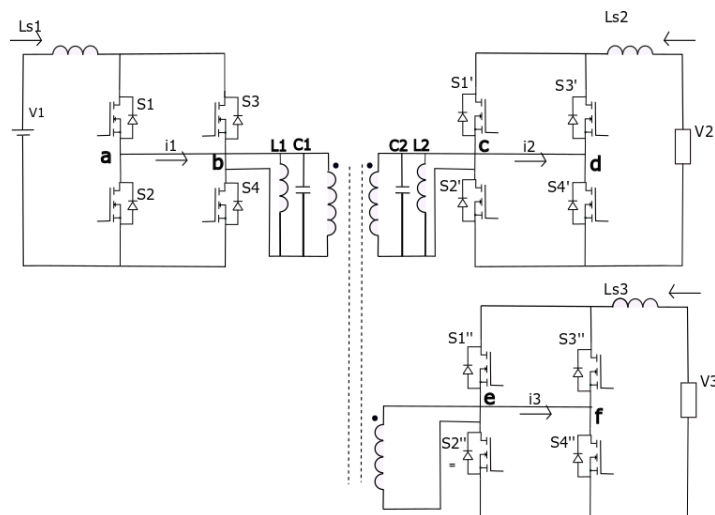


Figure 5-21: The 3-Port current-fed resonant converter without the tank circuit connected to the LV side.

Four operational modes of the integrated converter are simulated below. The tank resonant circuits are present in the first and second high side full-bridges, as in Figure 5-21. In these simulations, parasitic elements from the transformer and transistors are considered. The first case corresponds to the OBC operating mode. The second case corresponds to the charge of HV and LV batteries, while the third and fourth cases to the LDC operating mode, with positive and negative power flow, respectively.

Case A) OBC operation mode

The simulation results in Figure 5-22 present the transformer's winding currents and resonant voltage during the OBC operation mode. The voltage at the HV side is 471 V, close to the nominal Vdc link, and the output power 6.95 kW. The circulating current in the third-side, was minimized by placing the parallel resonant cells only in the high voltage sides.

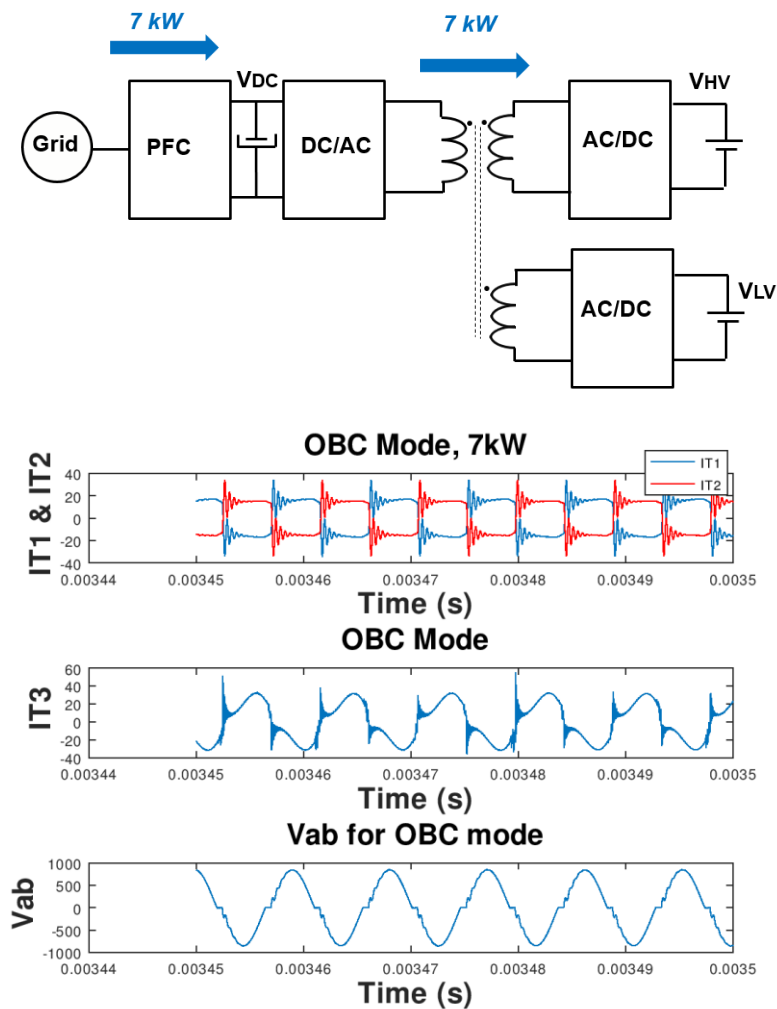


Figure 5-22: Power flow direction in the OBC operating mode. Transformer's current in primary, secondary, and third sides, i_{T1} , i_{T2} , and i_{T3} , respectively, and resonant voltage V_{ab} .

Case B) OBC&LDC operation mode

Figure 5-23 presents the transformer's winding currents and resonant voltage during the OBC and LDC simultaneous operation mode. The input power coming from the Vdc link is equally distributed

between the LV and HV ports, regulated at 19 V and 472 V. In practice, 3.5 kW remains the maximum power on the LV side.

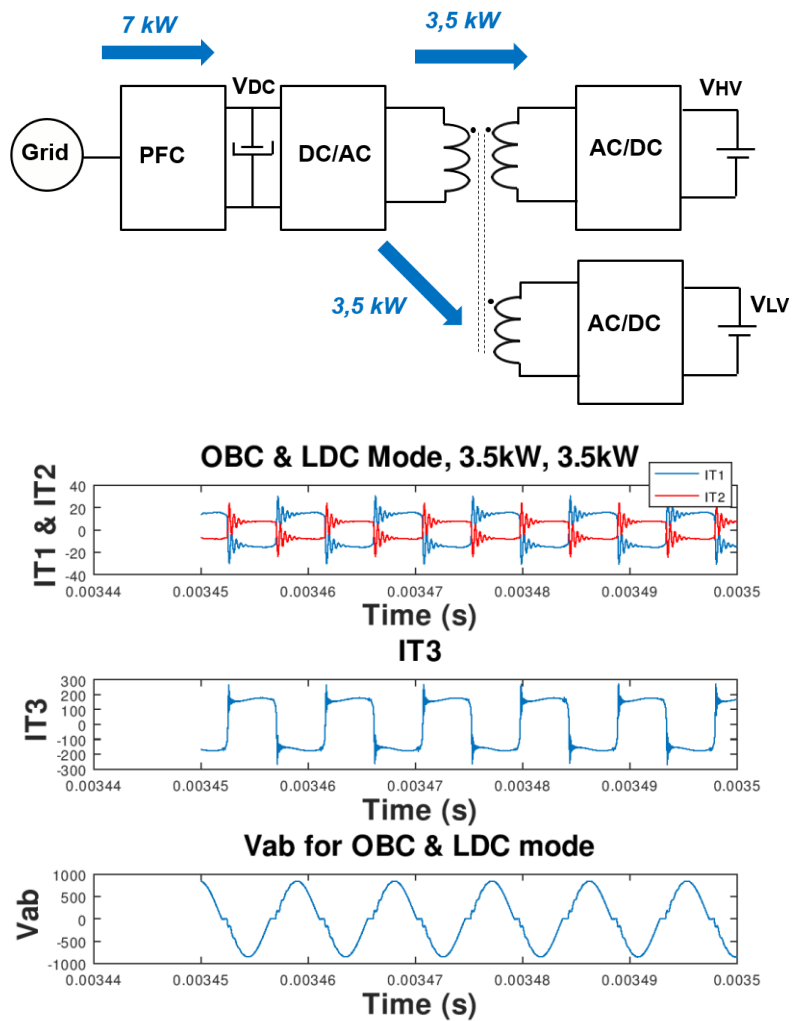
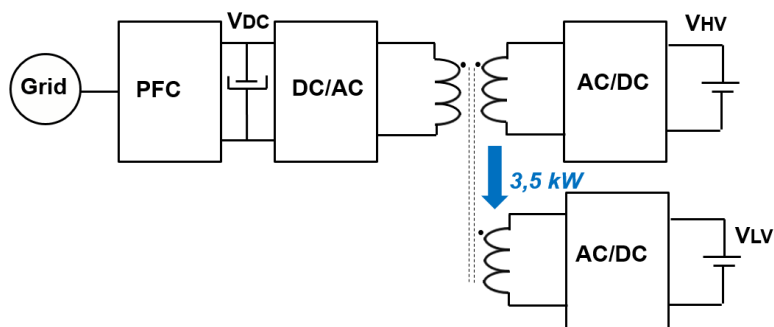


Figure 5-23: Power flow direction in the OBC+LDC operating modes. Transformer's current in primary, secondary, and third sides, i_{T1} , i_{T2} , and i_{T3} , respectively, and resonant voltage V_{ab} .

Case C) LDC operation mode

In the standalone LDC operation mode, the HV side charges the LV port. As discussed previously, in this mode, the maximum power is 3.5 kW. The current in the transformer windings, and the resonant voltage, are shown in Figure 5-24. The parasitic oscillations are decreased in this mode since the parallel resonant cell is not directly present on the LV side.



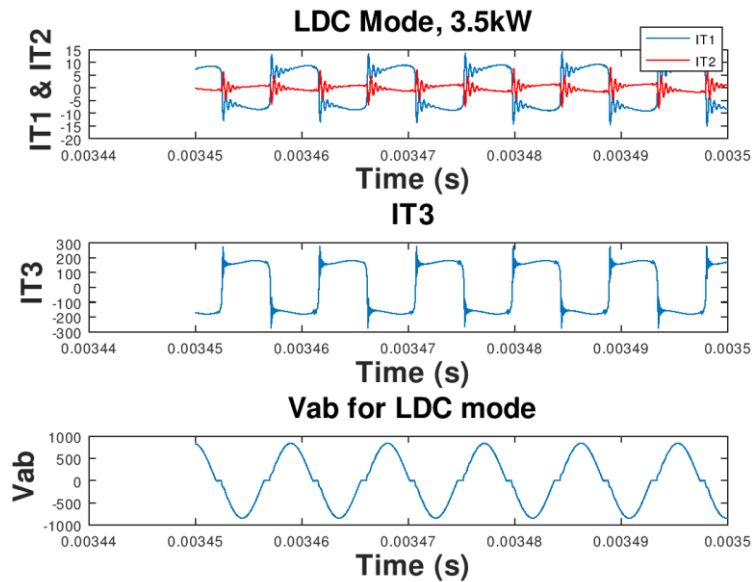
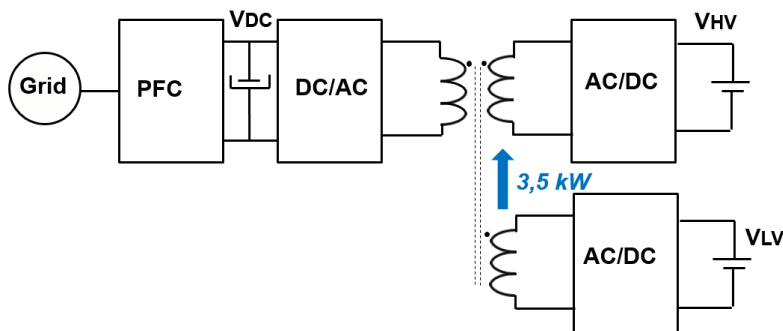


Figure 5-24: Power flow direction in the LDC mode. Transformer's current in primary, secondary, and third sides, i_{T1} , i_{T2} , and i_{T3} , respectively, and resonant voltage V_{ab} .

Case D) LDC reverse operation mode

In this operation mode, the converter can be used for two different situations. The first one is the charge of the HV side battery when the electrical grid is not present, requiring the operation close to the nominal power, 3.5 kW.

The second situation is the pre-charge of the bank capacitor associated with the HV side or the Vdc link. The capacitance present in the DC link, from the PFC stage, usually needs to be pre-charged by a diode bridge before the PFC boost control is activated. With this bidirectional converter, the bank of capacitors can be previously charged, allowing the elimination of the diode bridge. This utilization does not require a full power operation range, but the control strategy should limit the inrush current. Figure 5-25 shows the transformer currents and resonant voltage when a RC load is connected to the Vdc link. The capacitance is 1.2 mF, calculated for a single-phase totem-pole PFC converter in parallel with a resistance of 1 k Ω . The HV side's power is 3.4 kW, and the voltage is regulated at 450V.



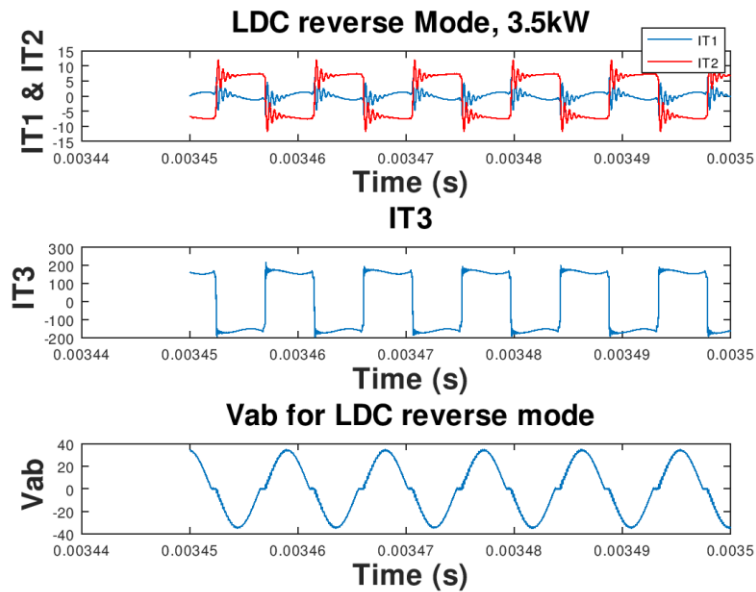


Figure 5-25: Power flow direction in the LDC reverse mode. Transformer's current in primary, secondary, and third sides, i_{T1} , i_{T2} , and i_{T3} , respectively, and resonant voltage V_{ab} .

5.5- The prototype, mechanical and thermal aspects

5.5.1- The power board

A prototype of the Three-port current-fed converter allowing the verification of the different operating modes was built. The converter was made with four independent boards: the planar transformer presented in Chapter 4 and three more boards connected to the Vdc, HV, and LV sides, as presented in Figure 5-26.

Each power board connected to the DC sources is composed of at least four blocks: the driver which receives the commands from the control board and amplifies the signals to drive the transistors; the discharging circuit proposed for protection against failure; a power supply block generating different voltage levels for the driver and signal acquisitions; plus the full-bridge containing the transistors and resonant tank circuit. The driver block also has galvanic isolation between the power and the signal sides because we use a single control board to the three power sides. Despite the additional functions, the power board side occupies a small area on the PCB. In the final product conception, the development of a single board containing all the functions would be preferable to obtain a more compact prototype. Nevertheless, to make the components manipulation easier during the first tests, the conception has been made as illustrated in Figure 5-26.

Each full-bridge also has a Hall Effect current measurement device connected in series to the DC side inductance. The LV board contains two parallel-connected transistors to constitute a single switch and share the conduction power losses. Although the transformer had been designed to be the closest as possible to the other boards, additional connection cables were unavoidable.

Considering the heat dissipation, the area delimited by the blue line in Figure 5-26 represents the more heat effective area, containing the high power components. They all can be connected through an electrically isolated thermal interface material to the same heat sink or cold plate. For automotive applications, we usually have cooling water available at 65°C, but we can also consider forced air-cooling at 85°C.

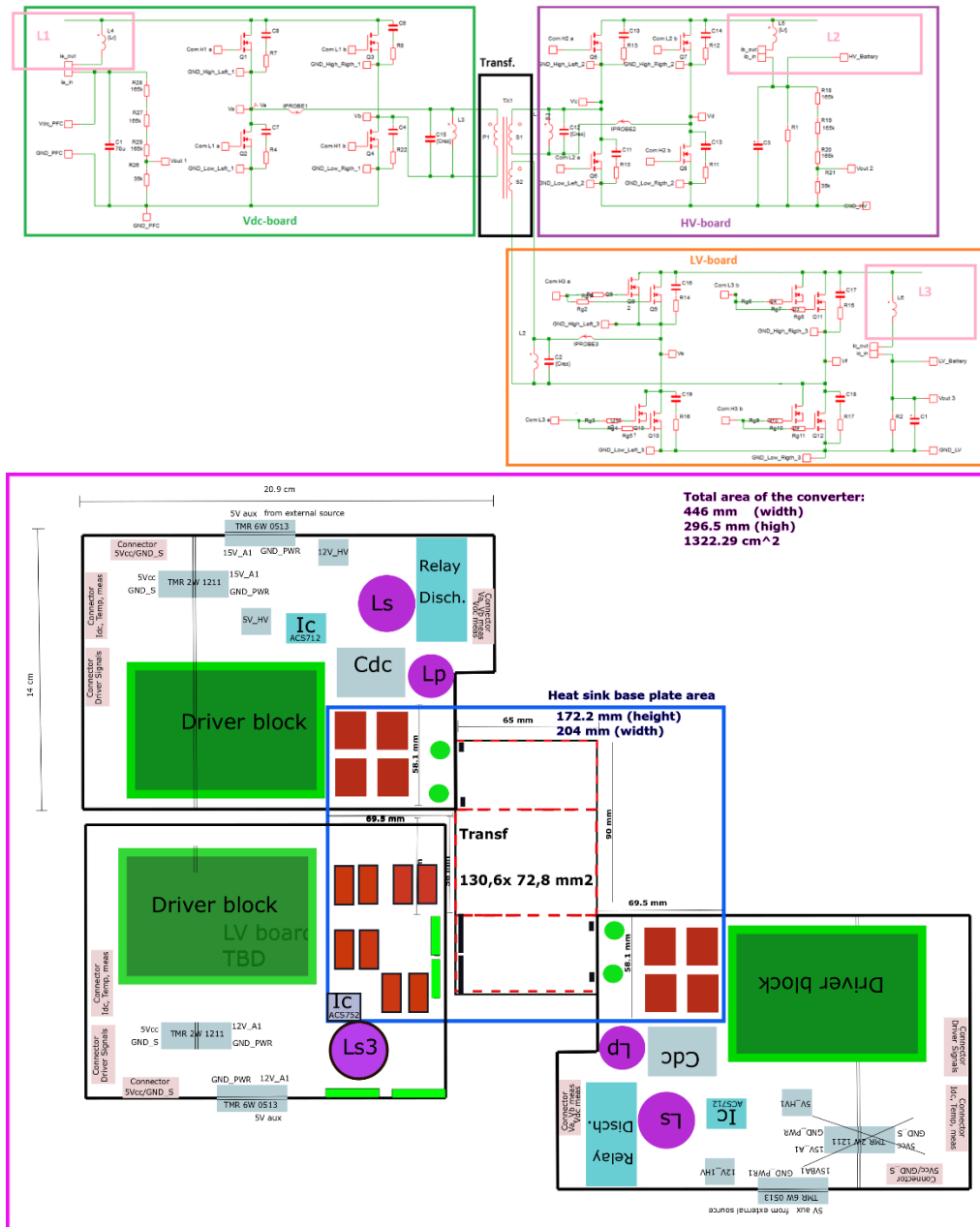


Figure 5-26: The diagram with 4 the boards designed to integrate the bidirectional 3-Port converter with: the planar transformer, the HV, LV and Vdc boards.

One additional analysis is still necessary for the conception of the cooling system, considering the total heat dissipated in each converter operational mode. Using the analysis in the previous chapters, the converter's total power losses are resumed in Table 5-10.

Mode	Semicond. Losses (W)	Transf. losses (W)	Total losses (W)
OBC	131.2	111.1	242.3
LDC	100.3	54.4	154.7
OBC+LDC	165.9	89.7	255.7

Table 5-10: Power losses estimation in the different operational modes using nominal conditions.

The next diagrams illustrate by area, the total generated heat in the OBC, LDC, and OBC+LDC modes. Notice that the maximum input power is always 7kW, distributed between the secondary and third ports connected to the HV and the LV batteries.

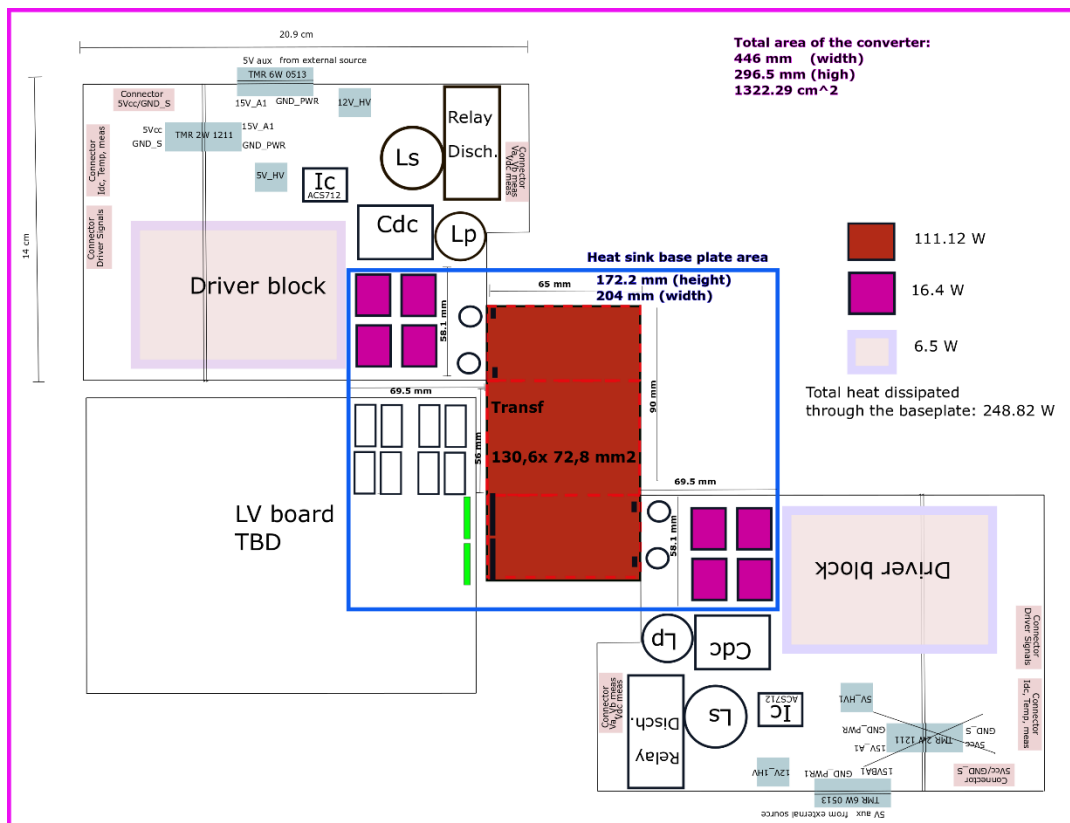


Figure 5-27: Heat dissipation in the OBC converter operational mode. $P_1=7\text{ kW}$, $P_2=-7\text{ kW}$, $P_3=0$.

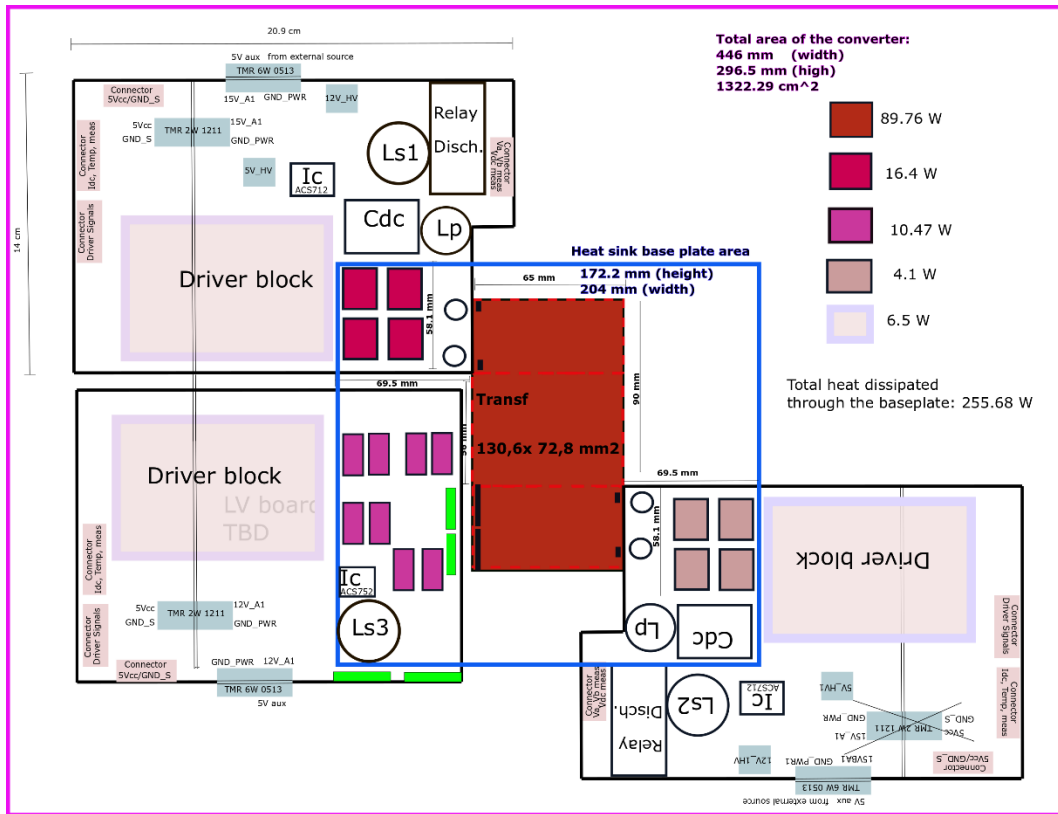


Figure 5-28: Heat dissipation in the OBC&LDC operational mode. $P_1=7kW, P_2=-3.5kW, P_3=-3.5kW$

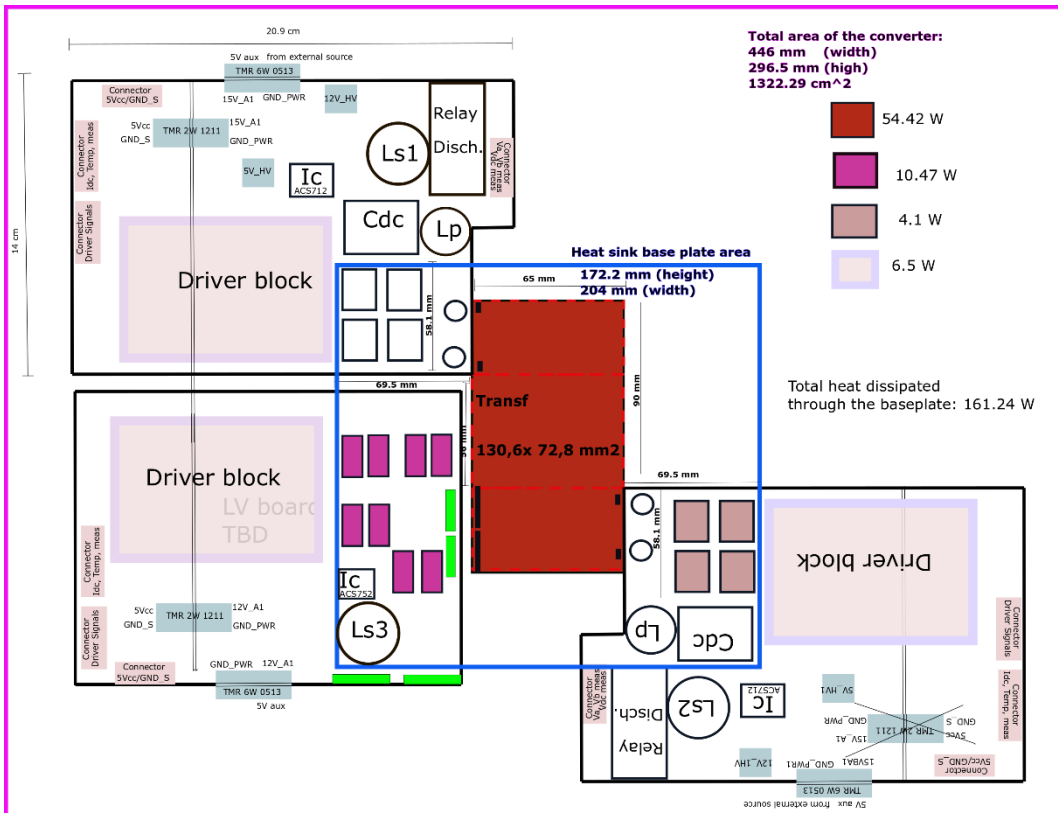


Figure 5-29: Heat dissipation in the LDC operational mode. $P_1=0 kW, P_2=3.5 kW, P_3=-3.5kW$

The worst-case for the heat sink design corresponds to the simultaneously OBC&LDC operational mode despite the more uniform heat distribution. The equivalent thermal resistance is calculated

based on the air temperature. Considering an external temperature at 65°C, the minimum static thermal resistance for a maximum temperature increase of 45°C is:

$$R_{th_{HA}} = \frac{\Delta T_{HA}}{Total\ Heat} = \frac{110-65}{255.68} = 0.176 \text{ } ^\circ\frac{C}{W} \quad (12)$$

The heat sink design will take into consideration the total area delimited by the blue line in Figure 5-27, Figure 5-28, and Figure 5-29. This area comprehends the power semiconductors, the DC side inductors, and the planar transformer.

To obtain a thermal model, we first consider the model of a single cold-plate with a thermal interface material (TIM) connected to the bottom side of the PCB board. Based on the Cauer network, it becomes possible to estimate an equivalent thermal circuit and change the heat sink model, if we would consider later, for example, a forced-air cooling system. The Cauer network in Figure 5-30 depends on the material properties, giving to the approximation a physical meaning. In the case of a PCB, every single material is assigned to a thermal capacitance and resistance, which are distributed components, but their effects can be modeled as discrete elements [8].

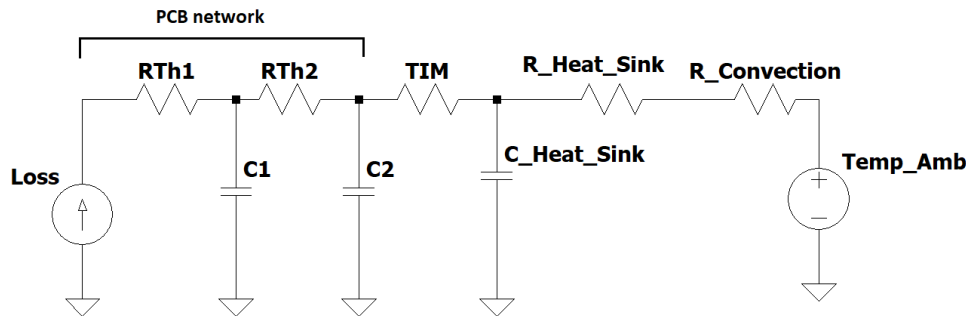


Figure 5-30: The equivalent thermal impedance representation of the PCB board, the thermal interface material, and the heatsink with the Cauer network.

The thermal resistance and capacitances in the conductive heat transfer through the heat sink are calculated as in [5]:

$$R_{Heat_{sink}} = \frac{L_{HS}}{\lambda A_{HS}} \quad \text{and} \quad C_{Heat_{sink}} = \rho C L_{HS} A_{HS} \quad (13)$$

Where λ is the material thermal conductivity, A_{HS} the surface area of the heat sink, C is the material specific-heat capacity, ρ the material density, and L_{HS} the thickness. Aluminum is the best material candidate for this application in comparison to other materials, such as copper. Indeed, it has lower thermal conductivity and is weightless and more economically competitive. Their properties are available in Table 5-11.

Properties	Aluminum	FR4 1080 – TG 150
Densit (Kg/m ³)	2700	1900
Thermal conductivity (W/m°C)	238	0.294
Specific heat capacity (J/Kg°C)	900	950

Table 5-11: Thermal properties of aluminum and FR4.

For different thicknesses, Table 5-12 shows thermal resistances and capacitances for the heat-sink, considering the area delimited by the blue line in the diagram from Figure 5-27, 351 cm².

Thickness (cm)	R _{HeatSink} (°C/W)	C _{HeatSink} (J/°C)
1	0.00119611	853.61
2	0.002392	1707.22
4	0.004784	3414.44
6	0.07176	5151.66
10	0.01196	8536.10

Table 5-12: Conductive thermal resistances and capacitances for the aluminum heat-sink.

Concerning the thermal interface material, one of the solutions is the use of the silicon or thermal materials containing fiberglass, generally used for electrical isolation purposes with good thermal performance. The material assembled on the power-board contains fiberglass with a thermal conductive coefficient of 1W/m K, and thickness of 0.15 mm. The equivalent conductive capacitance can be disregarded because of its small thickness and low specific heat capacity.

$$R_{TIM} = \frac{0.15 \times 10^{-3}}{1 \text{ W/m K } (351 \times 10^{-4})} = 4.27 \times 10^{-3} \text{ } ^\circ\text{C/W}$$

In the PCB thermal network, two configurations exist: the first one is the PCB with 4 layers for the HV boards, and the second one a PCB with 6 layers for the LV side. In Figure 5-31, we can see the stack of both proposed PCB's. The Cauer network determination associated with the stacks depends on the geometric dimensions and the material properties. A simplification can be made in order to reduce the model into a 1-D finite problem: we will not consider the spreading effects over the x and y axes of the FR4 in the PCB because of its reduced area used in the transistors assembling, also connected to the heat sink. Besides, due to the better thermal properties of the copper, the equivalent impedance of the copper layers can be disregarded. Therefore, for both PCB's, containing 4 and 6 layers, the thermal equivalent impedances are represented with 3 and 5 equivalent RC cells, respectively, as shown in Figure 5-32 and characterized by the properties of the insulation material in Table 5-13.

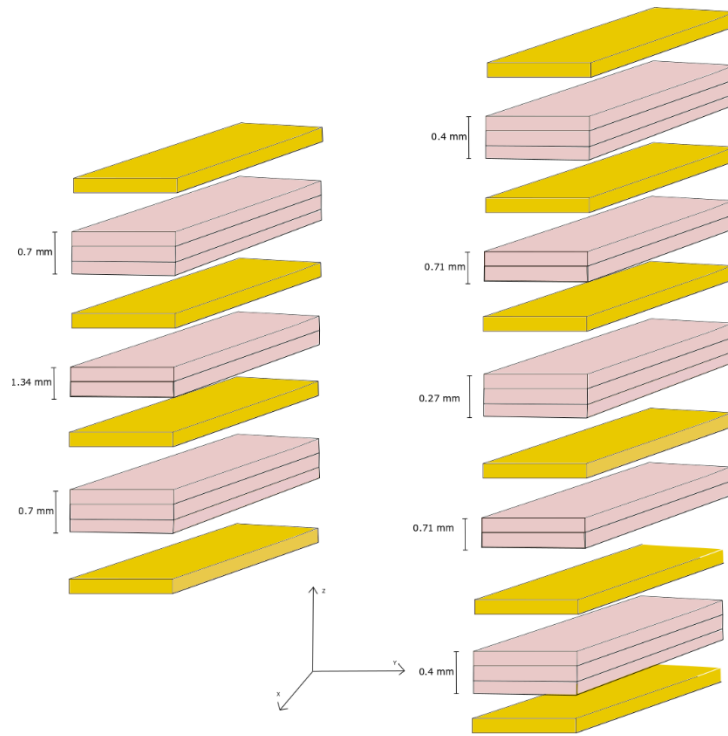


Figure 5-31: PCB stack up with 4 and 6 layers using the FR4 1080-TG 150 after pressed thickness.

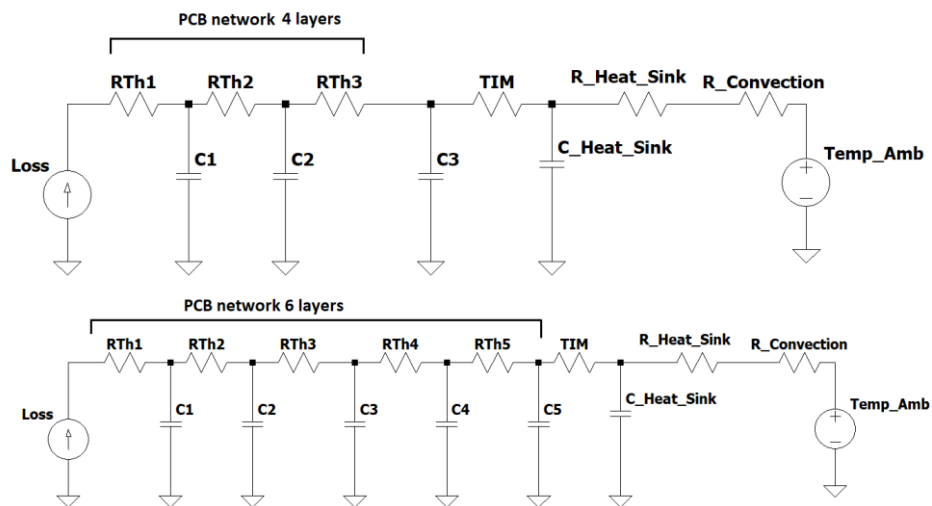


Figure 5-32: Proposed Caueer thermal model for Multilayer PCB's containing 4 and 6 layers, respectively.

N° Layer	RThx (°C/W)	Cx (J/°C)
1 / 1	0.61067 / 0.21751	4.9263 / 4.5161
2 / 2	0.9604 / 0.38609	9.4304 / 8.0161
3 / 3	0.61067 / 0.14682	4.9263 / 3.0484
- / 4	- / 0.38609	- / 8.0161
- / 5	- / 0.21751	- / 4.5161

Table 5-13 : Thermal cells to represent the Caueer model for multilayer PCB's with 4 and 6 layers.

The PCB containing 6 layers presents a better thermal characteristic compared to the PCB containing 4 layers. This result is due to the smaller total thickness of insulation layers and the increased area used to assembly the 8 transistors connected to the LV board side.

At steady-state, the thermal resistances are approximately 2 °C/W and 1 °C/W for the HV and LV board sides, respectively. Therefore, to minimize in practice the equivalent resistance of the PCB's, we added thermal vias under the semiconductor packages. The diameter of each via is 0.4 mm, and the distance between them 1.0 mm. The vias are placed under the D2Pack package of each transistor, as can be seen in Figure 5-33. The usual recommendation for the vias design is a diameter not too small (smaller than 0.2 mm) to prevent difficulty in their alignment over the PCB layers. It should neither be too large (larger than 0.6 mm), because of solder substance that could flow inside the vias during the assembling process of the board, increasing their thermal resistance. More information about thermal vias can be obtained in [9] and [10].

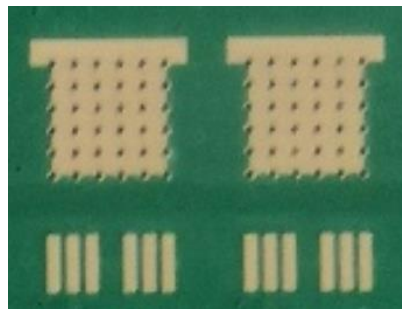


Figure 5-33: Thermal vias placed under the D2Pack transistors at the LV board.

The next step consists of determining the heat transferred by convection under natural, or air-forced cooling, or water-cooling.

A single thermal resistance represents the natural convection from the heat sink to the ambient, considering only the exchange through the bottom side, with the h_c as the convection coefficient.

$$R_{HS_{Amb}} = \frac{1}{h_c A_{HS}}$$

In [5] and in [6], we can find a typical estimation of the natural convection coefficient applied for electronic systems and automotive applications, such as 5 kW/ °C m² for a specific flow rate. One possible solution for water-cooling our prototype will be the conception of an aluminum base plate of 351 cm² with the highest thickness indicated in Table 5-12. The cooling water path can be extruded, as exemplified in Figure 5-34.

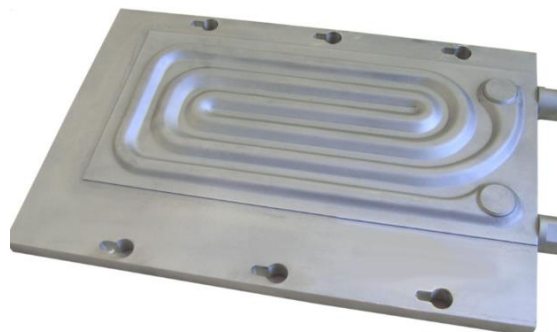


Figure 5-34: AAVID Thermalloy solution example with an aluminum base plate extruded with the water path.

Because of the big area required for the heat exchange and the need for a specific mechanical design in the base-plate with the water-cooling connecting the transformer and the PCB boards, we opted by the forced-air cooling system. The integration of the total system on the same base plate is proposed for future work.

In that manner, the transformer and the PCB boards have independent cooling systems. For the transformer, as discussed in Chapter 4, we had developed the configuration presented in Figure 5-35: the magnetic core is directly connected to the aluminum plate (the ground reference) and the last PCB bottom side as well through a gap filler. Thermal fin allows the heat dissipation at a lower resistance. The magnetic core top side is also covered by an aluminum baseplate with mechanical support at its extremities to close the two E planar cores as a sandwich. The fan is positioned vertically for heat extraction over all the 24 layers constituted in the 3 PCB's. The previous study about the current sharing between the connected layers and the total heat dissipation by layer gives us extra safety about the generated heat. The total power losses are almost equally distributed, except for the two more external layers.

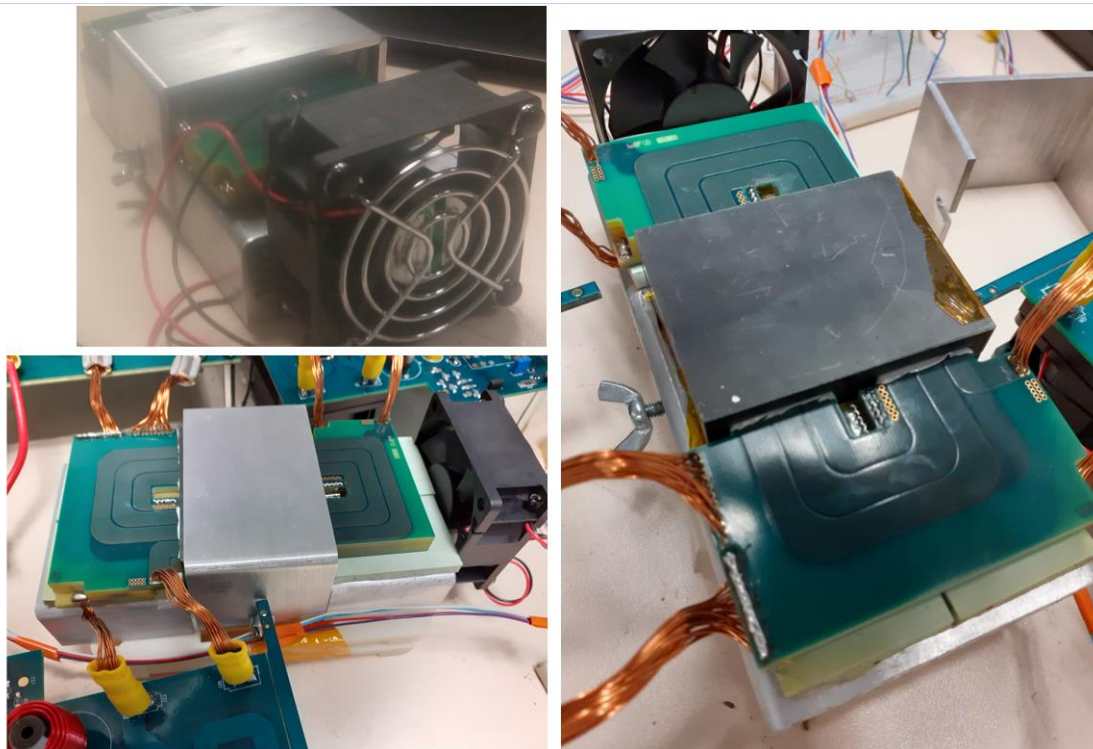


Figure 5-35: The air-forced cooling system proposed for the planar transformer.

For the three other PCB boards, we consider forced-air cooling.

5.5.2- Forced cooling convection

There are many models and optimization procedures to design a heat sink, where we should consider the forced convection cooling in finned heat sinks. However, we will stay close to the discussion presented in [11] and [12]. Figure 5-36 shows the geometry of the heat sink. The conductive thermal resistances and capacitances calculated in Table 5-13 for the base-plate are still valid for calculating the conductive heat transfer in the aluminum base plate. This last one is connected in series with the convective thermal resistance, $R_{\text{Convection}}$ associated with the finned part of the heat sink.

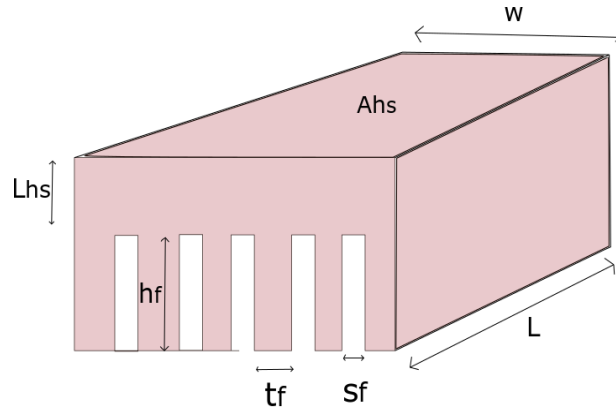


Figure 5-36: The heat sink geometry with fins for forced convection heat transfer.

To determine the average thermal transfer coefficient h_{Conv} , it is necessary to calculate the Nusselt number. It permits to characterize the transition from solid to fluid in thermal transfer between the air and the finned part of the heat sink:

$$Nu_{\sqrt{A}} = \left[\left(C_4 \frac{F_{Pr}}{\sqrt{z^*}} \right)^m + \left(\left(C_2 C_3 \left(\frac{F_{Re\sqrt{A}}}{z^*} \right)^{\frac{1}{3}} \right)^5 + \left(C_1 \frac{F_{Re\sqrt{A}}}{8\sqrt{\pi}\epsilon\gamma} \right)^5 \right)^{\frac{m}{5}} \right]^{\frac{1}{m}} \quad (14)$$

The constants are given in [11] for uniform wall temperatures:

$$C_1 = 3.24 \quad C_2 = \frac{3}{2} \quad C_3 = 0.409 \quad C_4 = 2 \quad \gamma = -\frac{3}{10} \quad m = 2.27 + 1.65 P_r^{1/3}$$

$$\epsilon = \frac{S_f}{h_f} \quad z^* = \frac{L N_{Fins} v_{air}}{P_r V'}$$

The above parameters depend on the air velocity and the flow rate, and if it is in laminar or turbulent regime. The Prandtl number, Pr , is related to the thermal conductivity and the air viscosity, while the Reynolds number tells if the flow is laminar or turbulent. Both numbers are taken into account by the Prandtl function and the Reynolds friction factor, in [4] and [11]:

$$F_{Pr} = \frac{0.564}{\left(1 + \left(1.664 Pr^{\frac{1}{6}} \right)^2 \right)^{2/9}}$$

$$F_{Re\sqrt{A}} = \sqrt{\frac{11.8336 V'}{L \eta_{Fin} v_{air}} + \left(\frac{12}{\sqrt{\epsilon}(1+\epsilon)\left(1-\frac{192}{\pi^5} \epsilon \tanh\left(\frac{\pi}{2\epsilon}\right)\right)} \right)^2}, \quad F_{Re\sqrt{A}} = f_{fr} Re\sqrt{A}$$

Where the efficiency of a single fin, found in [11] and [12] is:

$$\eta_{Fin} = \tanh h \left(h_f \sqrt{2(h_f + L_{hs}) \frac{(t_f+L)}{\lambda t_f L}} \right) \quad (15)$$

Thus, the average thermal transfer coefficient h_{Conv} , is determined according to the airflow volume, where D_h is the hydraulic diameter associated with the pressure drop in the heat sink.

$$h_{Conv} = \frac{Nu_{\sqrt{A}} \lambda_{air}}{D_h}$$

$$D_h = \frac{2 s_f h_f}{(s_f + h_f)}$$

Finally, the thermal resistance of the finned part associated with the convective heat transfer can be determined, depending on the airflow [11]-[12]:

$$R_{Convection} = \frac{1}{\rho_{air} c_{air} V' \left(\frac{-h_{Conv} A_{eff}}{1 - e^{-\rho_{air} c_{air} V'}} \right)} \quad (16)$$

Where the effective area, A_{eff} , depends on the finned area in contact with the air:

$$A_{eff} = (N_{Fins} - 1)(2 h_f \eta + s_f) L$$

$$\eta = \frac{\tanh(f)}{f}, \quad f = \sqrt{\frac{2 h_{Conv} (t_f+L)}{\lambda t_f L}} h_f$$

In order to choose the fan able to provide the airflow for achieving the desirable thermal resistance, it is necessary to represent the equivalent pressure drop in the heat sink. The fan characteristic selected for the application must intercept the equivalent curve in the thermal resistance nominal point.

The pressure drop in the heat sink is due to air acceleration, taking into account the attrition between air and the finned part surface, and it also depends on the hydraulic diameter variation considered to expand or contract air between the fan and the finned part. The Bernoulli equation gives the pressure drop that can be simplified as in (17):

$$\Delta P = \left[\left(\frac{1}{((N_{Fin}-1) h_f s_f)^2} - \frac{1}{((L_{hs}+h_f) w)^2} \right) + \left(\frac{(f_{fr} \frac{L}{D_h} + K_{se} + K_{sc})}{((N_{Fin}-1) h_f s_f)^2} \right) \right] \frac{\rho_{air} V'^2}{2} \quad (17)$$

Where the factors, K_{se} and K_{sc} , represent the variations in the hydraulic path provoking contraction and expansion, respectively.

$$K_{sc} = 0.42 \left(1 - \frac{h_f^2}{(L_{hs}+h_f)^2} \right), \quad K_{se} = \left(1 - \frac{h_f^2}{(L_{hs}+h_f)^2} \right)^2$$

Therefore, the heat sink pressure drop can be compared to the fan characteristics, based on some manufacturer's datasheets. For this choice, we are looking for curves relating to volume airflow and pressure drop in a quadratic behavior. According to the reference [11], the fan power consumption can be considered constant in a certain speed range, making it easier its selection.

With an aluminum base-plate connected to the board's bottom side, the total resistance should be smaller than $0.17\text{ }^{\circ}\text{C}/\text{W}$ (12) for a maximum temperature elevation of 35°C . Using the area delimited by the components ($204\text{ mm} \times 170\text{ mm}$), a heat sink containing 14 fins is proposed, as presented in Table 5-14. This heat sink allows dissipating the total power losses of the converter in its worst operating case.

N° of fins	14
Fin Height (mm)	87
Fin Width (mm)	6
Space between fins (mm)	9
Base plate thickness (mm)	3.5
Base plate width (mm)	204
Base plate length (mm)	170

Table 5-14: Heat sink parameters to dissipate the total power of the converter.

Using the thermal model for the forced-air cooling as proposed in the above lines, the thermal resistance is estimated with (16), as well as the pressure drop (17). Both parameters are plotted below for the heat sink parameters in Table 5-14: In Figure 5-37, the equivalent thermal resistance of the heat-sink and the fan characteristics are presented. The proposed fan measures $120\text{ mm} \times 120\text{ mm}$.

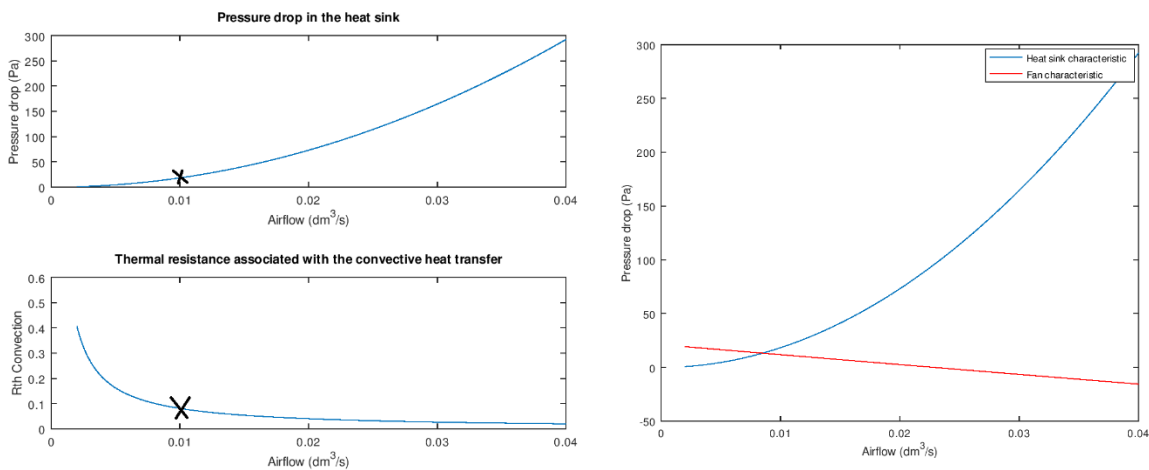


Figure 5-37: a) Pressure drop and thermal resistance for the heat-sink proposed to dissipate the total power losses. b) Intersection between the heat sink and the fan. Fan size of $120\text{ mm} \times 120\text{ mm} \times 25\text{ mm}$.

To validate the model for the air-forced cooled heat sink, the design was verified with a FEM tool proposed by AAVID [14]. The thermal resistance estimated by the software is about $0.098\text{ }^{\circ}\text{C}/\text{W}$ for the airflow rate at $0.01\text{ dm}^3/\text{s}$, presented Figure 5-38.

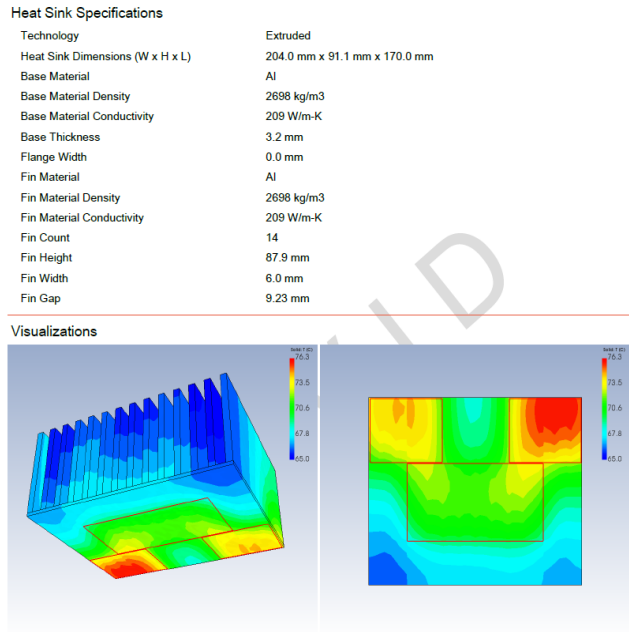


Figure 5-38: Heat sink design verification using a FEM simulation.

Because of difficulties in assembling the four boards on the same base plate, a second solution is proposed. This solution consists of using independent heat-sinks for each one of the boards. Therefore, the heat-sinks are connected to the PCB bottom side to dissipate the power losses generated by the transistors. For this, the proposed baseplate occupies the same area of the transistors. For the HV side, the base plate occupies (59 mm x 65 mm) and contains 6 fins. The fan chosen for this application measures 60 mm x 60 mm. The thermal resistance is presented in Figure 5-39, and the heat-sink details in Table 5-15.

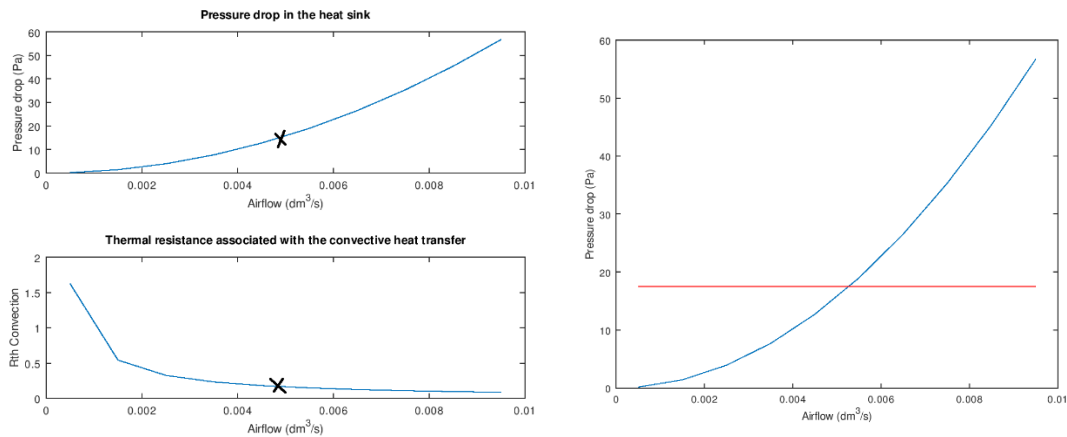


Figure 5-39: a) Pressure drop and thermal resistance for the heat sink proposed to dissipate the power losses produced in each power board. b) Intersection between the heat sink and the fan. Fan size of 60 mm x 60 mm x 10 mm.

N° of fins	6
Fin Height (mm)	20
Fin Width (mm)	3
Space between fins (mm)	9

Base plate thickness (mm)	6
Base plate width (mm)	40
Base plate length (mm)	100

Table 5-15: Heat sink parameters to dissipate the power loss of the transistors connected to the HV board.

The design above is the proposed solution for the cooling system of the integrated power converter. However, due to delays in order to develop the system and receive the components, we had replaced, for the first tests, the proposed system by a horizontal forced cooling system connected to the top side of the PCB, through a thermal interface material. The fan was connected to the bottom side of the heat sink, so the airflow passes through the finned part before being stopped by the aluminum base plate, changing its direction. Therefore, the airflow loses kinetic energy making the cooling system less effective.

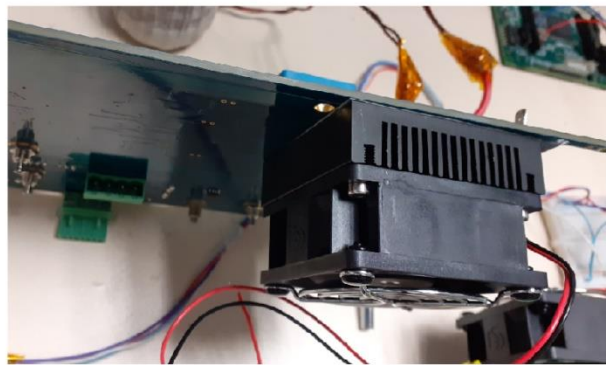
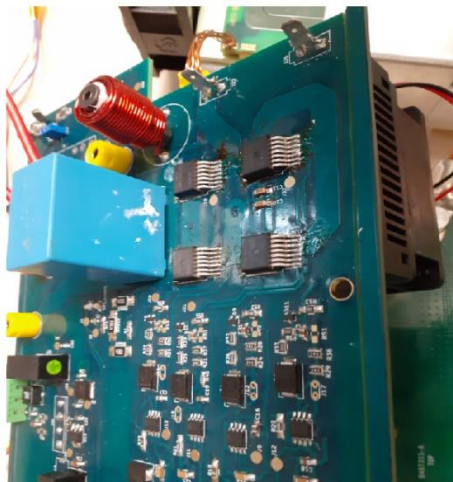


Figure 5-40: Example of the heat sink connected to the bottom side of one PCB to dissipate the heat produced by the transistors.

5.5.3- The control board

An additional board was developed to generate the commands to control the power boards. It detects the zero voltage crossing and combines the measured signals with the forced switching command at a fixed frequency to generate the control signals. A schematic of the board is presented below, Figure 5-41.

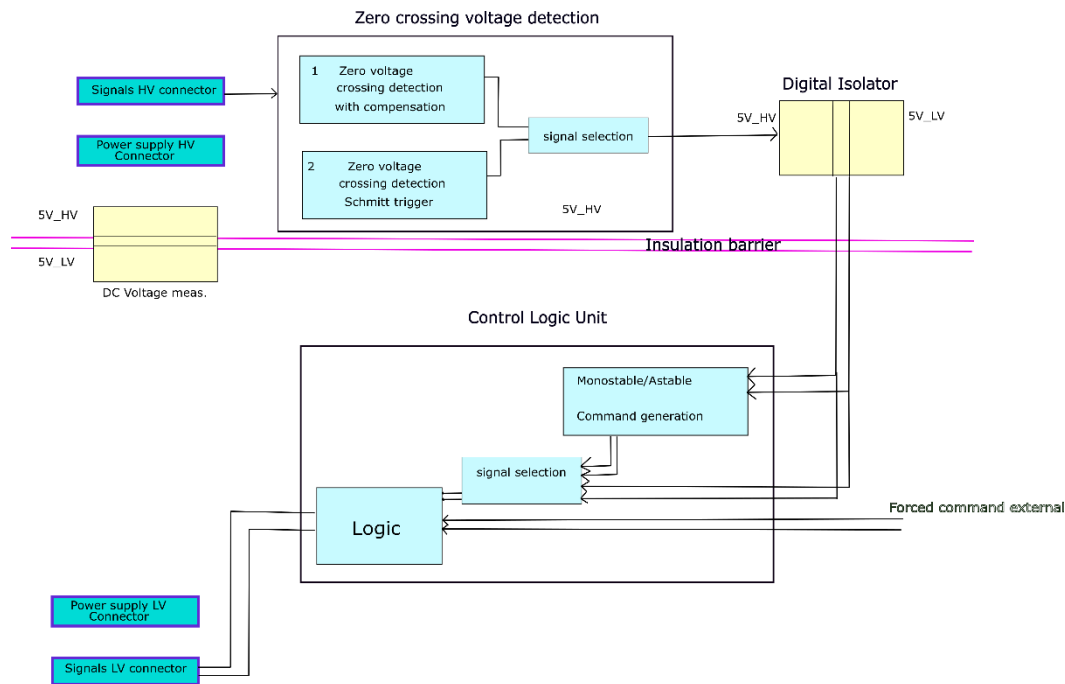


Figure 5-41: The Analog control board.

In Figure 5-41, there are the main components of the proposed control board. On the top side, the zero voltage crossing detection is generated inside the blocks “Crossing detection with compensation” and “Crossing detection with Schmitt trigger”. The first block uses a RC circuit in series with a diode to detect the zero-crossing for the DC signal in one of the arms from the bridge. Compensation in case of delays between the three boards it is possible. This strategy had been used in a series resonant converter in [15] for frequencies between 20 and 50 kHz.

The second block used for the zero voltage crossing detection receives the HF voltage measured signal from both legs of the full-bridge. A Schmitt trigger circuit generates then a pulse at every time the voltage pass by zero during its falling edge. The advantage of this circuit, composed with a hysteresis comparator, is the immunity against other high-frequency oscillations perturbing the natural oscillation. The output from these two blocks is then transmitted through a digital isolator.

The second stage, after the digital isolator, transforms the Schmitt trigger’s impulse signal into a pulse with a defined duration, using a monostable circuit in high state during a specific time. This circuit is implemented with the timer LM555 and an RC circuit connected to the discharge pin of this device. The timer comprehends an internal voltage divisor and compares a reference voltage with the external threshold and trigger pins. Both comparator outputs are applied to a flip-flop to control the output that sends a command to charge the external RC circuit. In our application, the monostable followed by the astable configurations are used, as presented in Figure 5-42. The monostable circuit creates a signal with a fixed pulse duration when the zero-crossing is detected (determined by the RC constant time). Then, the astable circuit generates the control signal at the operating frequency only during this interval.

The logic to generate the command is simple and can also be implemented in a microcontroller connected to the evaluation board. Later, during the thesis, the analog board was replaced by an FPGA MAX10 (10M08S-144-EQFP) containing an ADC block function. The DC voltage acquisition is implemented with a voltage divider and the current acquisition by using integrated Hall Effect sensors, the ACS712 for HV sides and the ACS773 for the LV side.

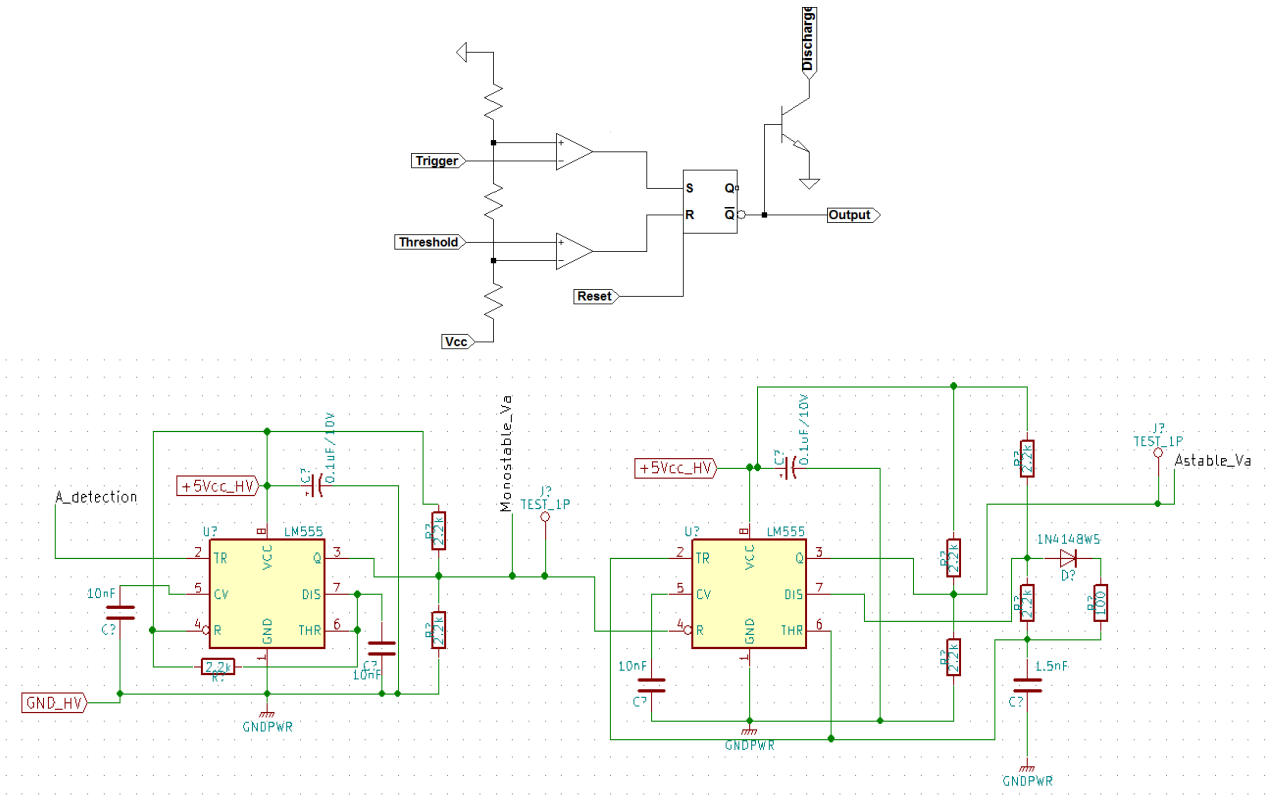


Figure 5-42: a) The LM555 diagram. b) The monostable and astable configurations implemented with the LM555 to generate the switching signals.

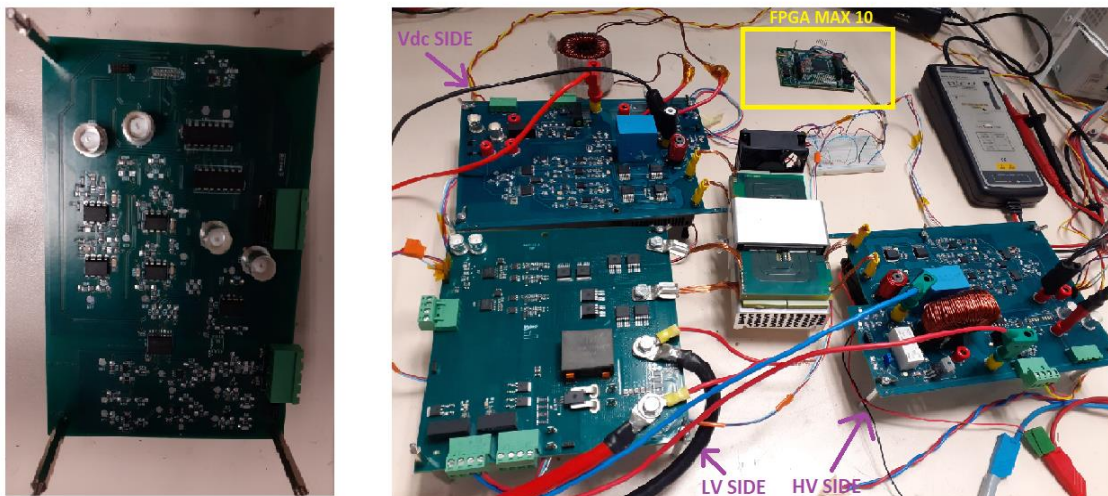


Figure 5-43: a) The 1° control board replaced later by an FPGA. b) Prototype assembly of the Three-port converter used for the experimental tests.

5.5.4- Experimental results

The converter operation was validated in a prototype of 7 kW for the different operating modes, OBC, LDC, OBC & LDC, OBC reverse mode, and LDC reverse mode.

Figure 5-44 and Figure 5-45 show the resonant voltage, the current in the parallel inductance, and the AC side input current connected to the converter's primary side. The current in the parallel inductance is passing by the maximum and minimum points during the transistors switching, discharging the equivalent capacitance for Zero-voltage switching.

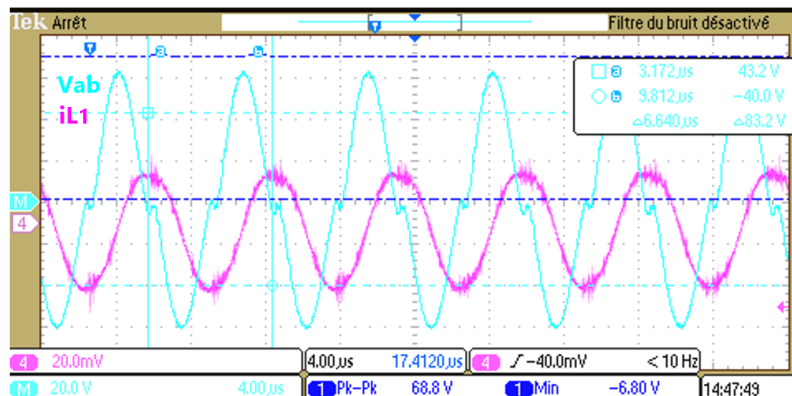


Figure 5-44: The resonant voltage V_{ab} and the current in the parallel resonant inductance connected to the primary side of the converter.

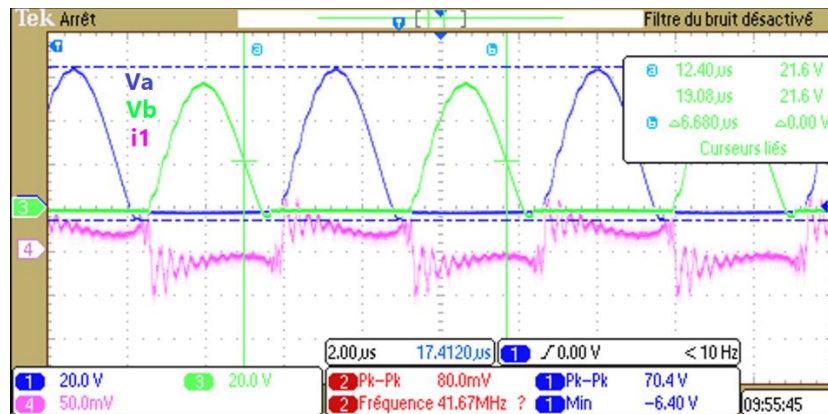


Figure 5-45: Voltage V_a and V_b and the current in the primary side of the converter for low power transfer.

The converter was first validated with a resistive load of 20Ω connected to the HV side. A DC voltage supply was connected directly to the first port of the converter, and its value was increased step by step to prevent voltage overshoots in the transistors. Figure 5-46 and Figure 5-47 show the voltage on the transformer in Vdc and HV sides and the current on the secondary load side simulating the OBC operation mode.

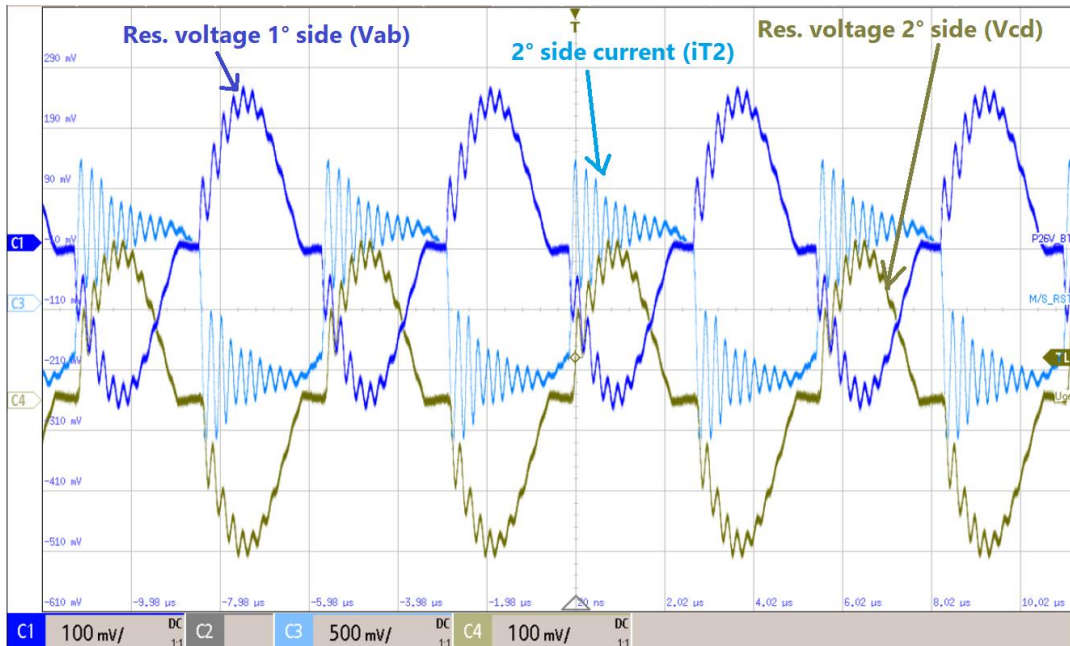


Figure 5-46: Voltage measured at both HV sides, port 1 and 2, and the current in the secondary side of the transformer. Voltage scale: 1/1000 and current probe: 100 mV/A. $V_{dc} = 150$ V.

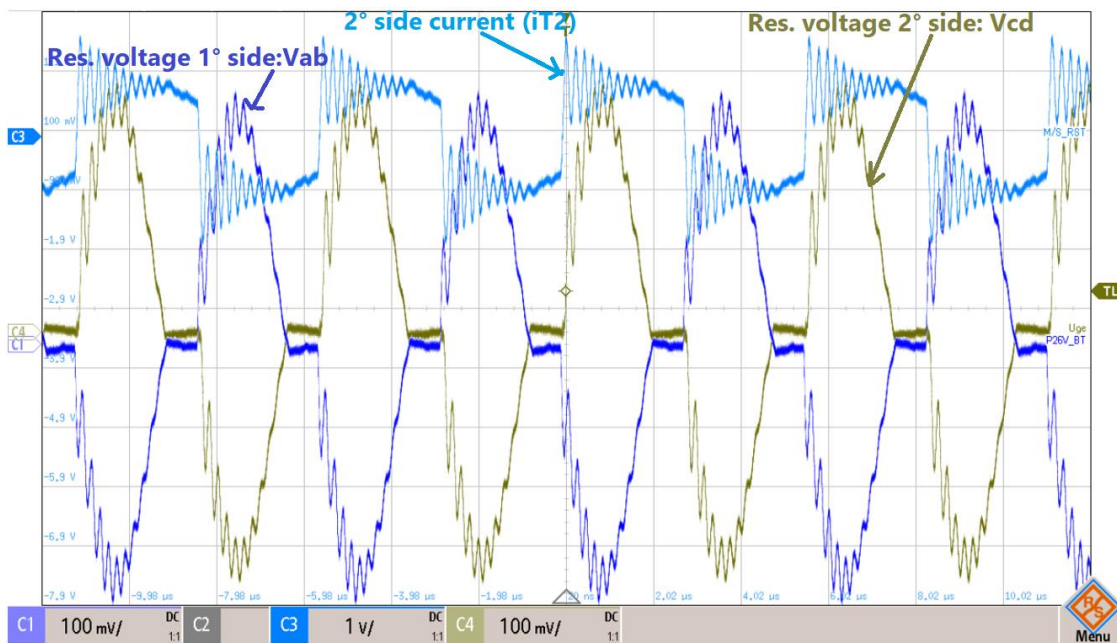


Figure 5-47: Voltage measured at both HV sides, port 1 and 2, and the current in the secondary side of the transformer. Voltage scale: 1/1000 and current probe: 100 mV/A. $V_{dc} = 250$ V.

The parasitic oscillations are significant because the nominal current is not proportional to the voltage source. Under nominal conditions, for the same current load used in this test, the voltage is close to 480 V, minimizing the effect of the parasitic oscillations.

In this mode, a power analyzer was used to measure the efficiency of some operating points. The efficiency is decreased in low power levels because of the circulating current in the resonant cell and passive elements. Besides, the transistors used in the HV sides were not the first choice and presented

higher R_{dsON} resistance compared to the previously selected transistor, increasing the conduction power losses.

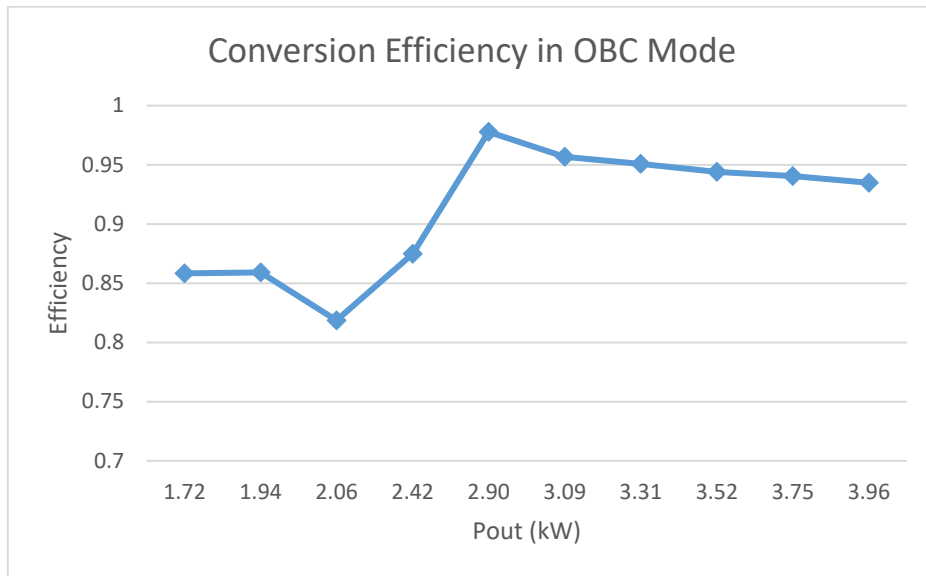


Figure 5-48: The converter measured efficiency during OBC operating mode ($V_{in} = 240$ V).

In order to validate the LDC operating mode, a dynamic electrical load was connected to the third side of the converter, while the first port was in open-circuit. The test was done with a current load of 150 A RMS, while a voltage supply of 240 V was connected to the second port. The results are presented in Figure 5-49, Figure 5-50. As verified, the current on the primary side oscillates at the same frequency and with the parasitic elements present on the V_{dc} side.

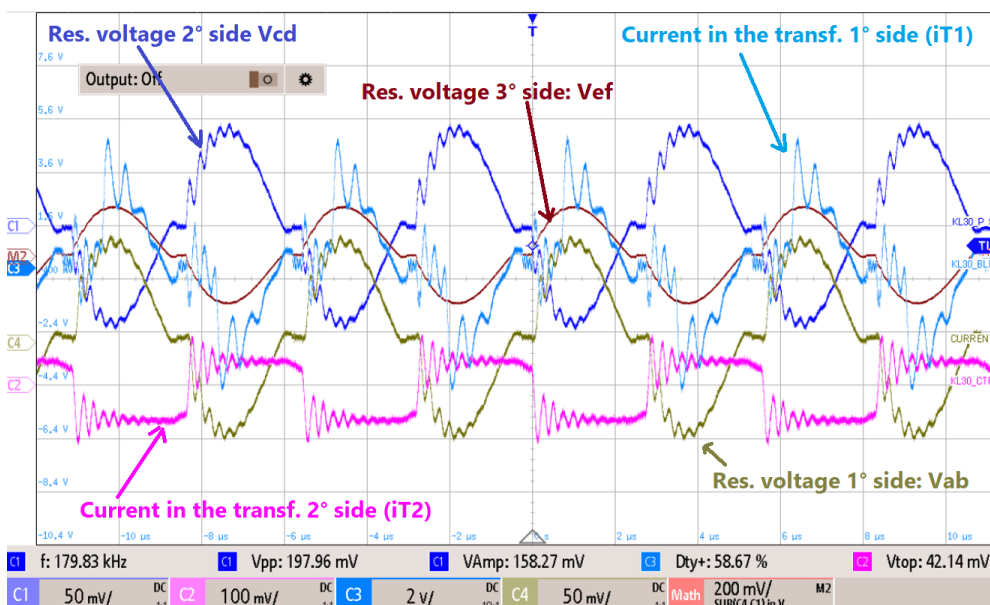


Figure 5-49: Resonant voltage and current in the first and secondary sides of the transformer C1: Resonant voltage in the secondary side; C2: Current in the transformer secondary side. C3: Current in the transformer primary side. C4: Resonant voltage in the primary side. Math: Resonant voltage in the third side. Voltage scale: 1/2000 and current probe: 100 mV/A. $V_2 = 240$ V.

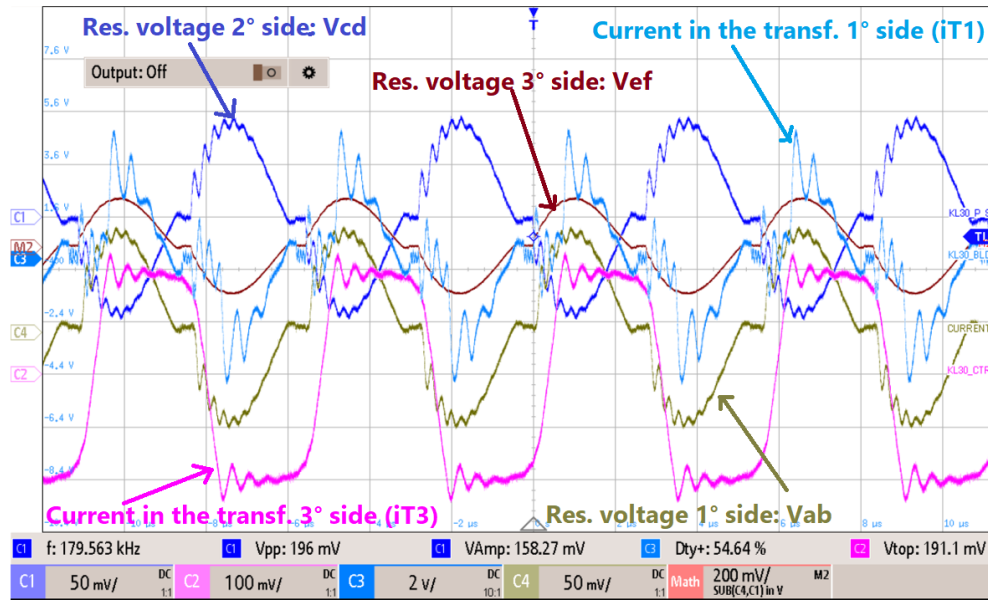


Figure 5-50: C1: Resonant voltage in the secondary side; C2: Current in the transformer third side. C3: Current in the transformer primary side. C4: Resonant voltage in the primary side. Math: Resonant voltage in the third side. Voltage scale: 1/2000 and current probe: 100 mV/A. $V_2 = 240$ V.

The results obtained allow validating the two main operating modes of the converter. As the architecture is symmetrical, the OBC and the LDC in reverse modes exhibit the same behaviors.

5.6- Conclusion

In this chapter, a prototype was developed and tested to validate the analysis and operation of the proposed Three-port current-fed parallel resonant converter. The results show the converter operation with ZVS to integrate the OBC and LDC converters. The tests also made evident the role of the parasitic elements in the converter behavior, such as the leakage inductance and the parasitic capacitances from the transformer. The parasitic oscillations are superposed to the resonant voltage waveforms affecting the converter performance. These oscillations can be damped using a snubber in parallel to the transformer and by improving the connections between the transformer and the power boards in a future design.

5.7- Annexes

5.7.1- Simulation results with different power flow directions

The second case is the converter operating on the OBC mode only, at full load, 7 kW.

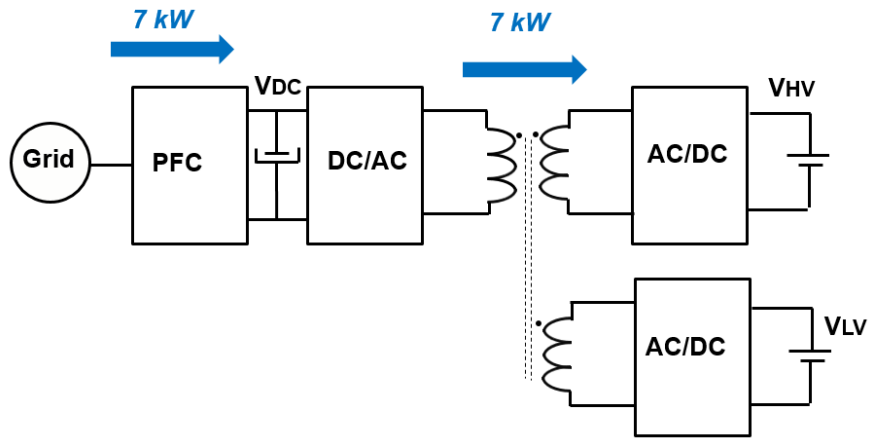


Figure 5-51: Power flow for the OBC mode only, while the HV side is charged.

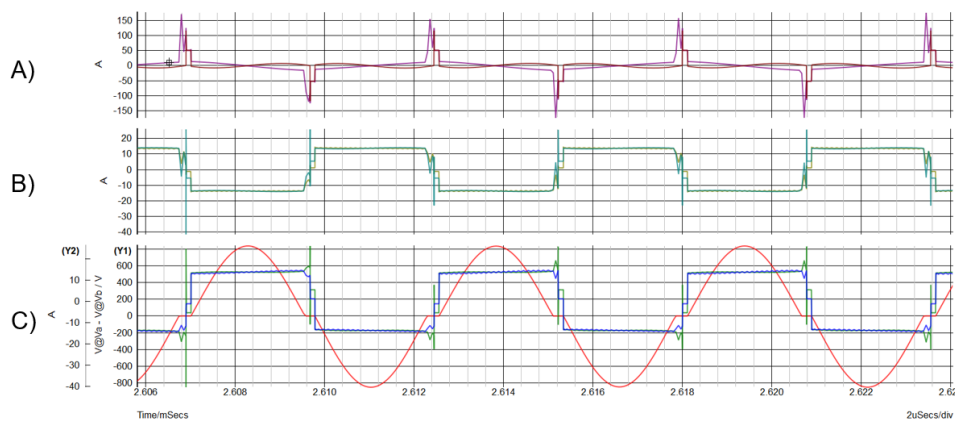


Figure 5-52: A) Current on the third side of the transformer, after and before the resonating cell. B) Current on the second side of the transformer, after and before the resonating cell. C) Sinusoidal Voltage V_{ab} and the current on the primary side of the transformer. V_{HV} power $\cong 6.48$ kW, V_{LV} power $\cong 0.1$ kW

In this mode, the third port is also controlled at the same frequency as the second and first full-bridges, inducing the current spikes in the resonant cell also placed on this third side. If the total leakage inductance is minimized, the resonant cell can be integrated only on the high voltage sides, minimizing this effect.

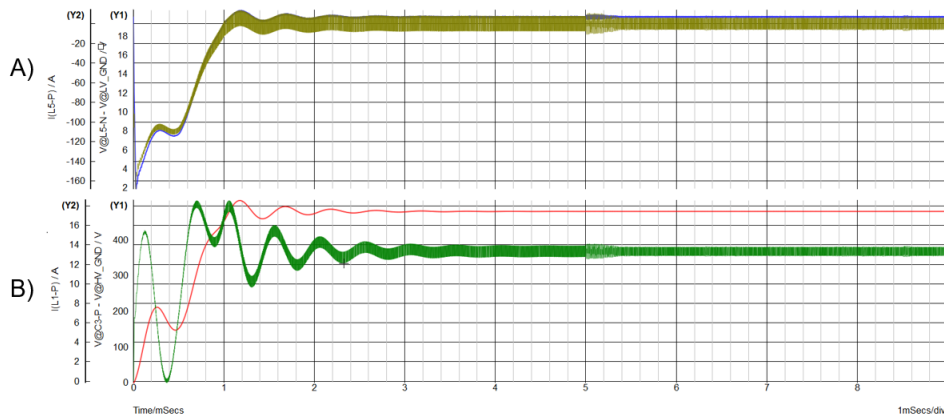


Figure 5-53: A) Voltage V_{LV} and current I_{LV} charging the LV battery. B) Voltage V_{HV} and current I_{HV} charging the HV battery. V_{HV} power $\cong 6.48$ kW, V_{LV} power $\cong 100$ W.

The third case corresponds to the OBC in reverse mode. The results presented in Figure 5-55 and Figure 5-56 are very similar to the OBC mode because of the symmetry between both high voltage sides.

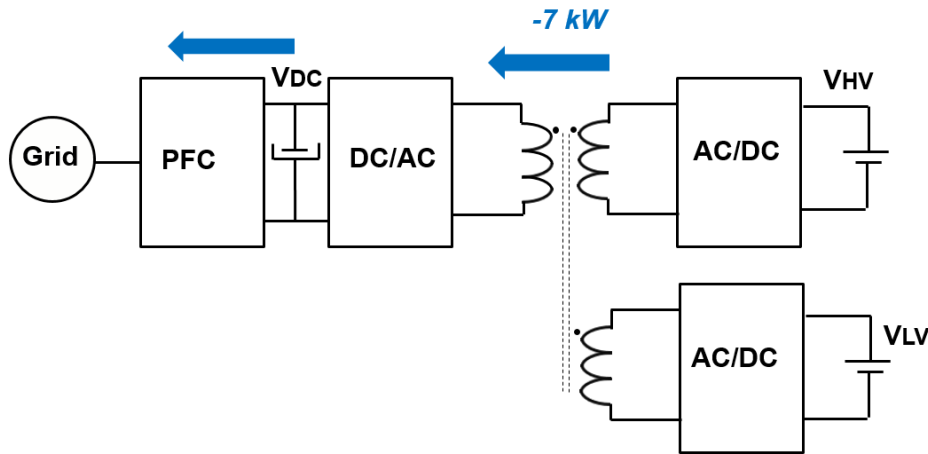


Figure 5-54: Power flow for the OBC in reverse mode, while the HV side is discharged.

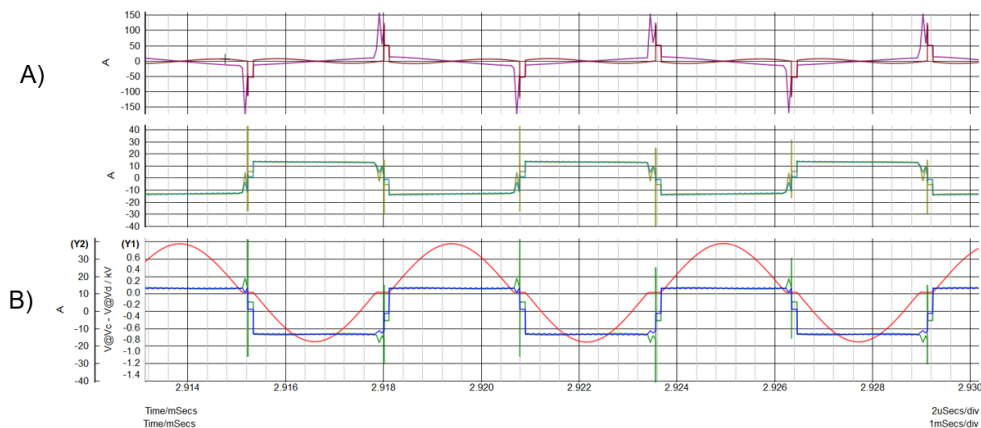


Figure 5-55: A) Current on the third side of the transformer, after and before the resonating cell. B) Current on the first side of the transformer, after and before the resonating cell. C) Sinusoidal Voltage V_{cd} and current on the secondary side of the transformer. V_{DC} power $\cong 6.48$ kW, V_{LV} power $\cong 0.1$ kW

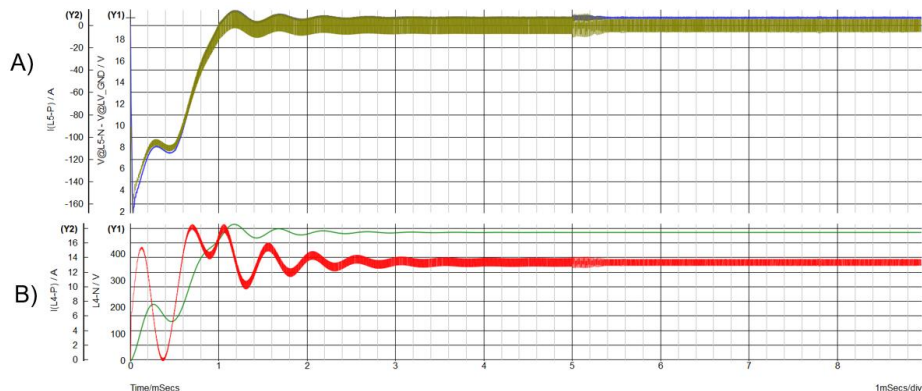


Figure 5-56: A) Voltage V_{LV} and current I_{LV} on the LV side. B) Voltage V_{DC} and current I_{DC} charging the first side. V_{DC} power $\cong 6.57$ kW, V_{LV} power $\cong 100$ W.

The fourth case is the converter operating in LDC mode when the HV charges the LV battery. The nominal power for this condition is 3.5 kW

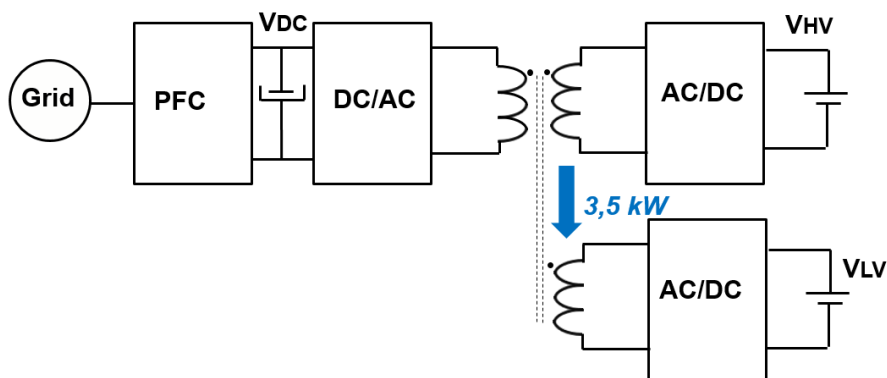


Figure 5-57: Power flow in the LDC converter operation mode.

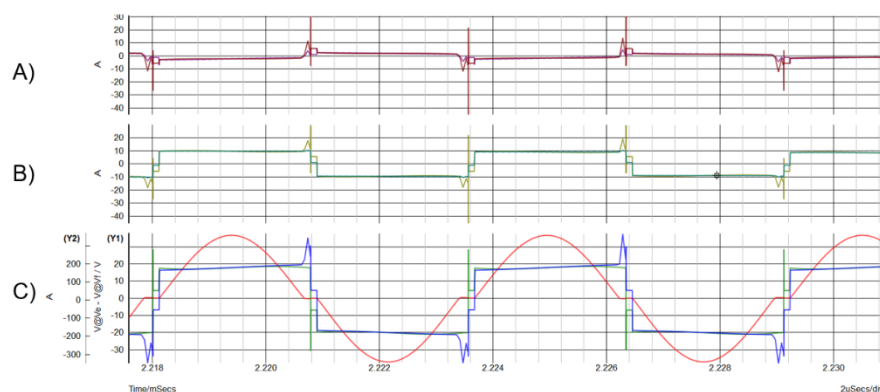


Figure 5-58: A) Current on the third side of the transformer, after and before the resonating cell. B) Current on the first side of the transformer, after and before the resonating cell. C) Sinusoidal Voltage V_{cd} and current on the secondary side of the transformer. V_{LV} power $\cong 3.26$ kW.

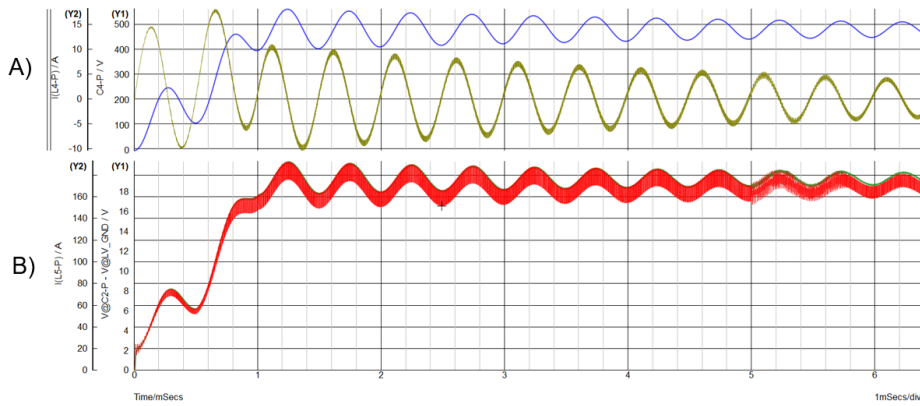


Figure 5-59: A) Voltage V_{DC} and current I_{DC} in the first port. B) Voltage V_{LV} and current I_{LV} charging the low voltage side. V_{LV} power $\cong 3.26$ kW.

The last case corresponds to the pre-charge of the HV voltage bus through the LV side. The objective is to provide a pre-charge to the HV bus, hence the power level in this direction can be much smaller than the nominal power designed for the LDC converter. The reverse direction is sometimes required for some automobile manufacturers to pre-charge the HV bus when the electrical grid is not available.

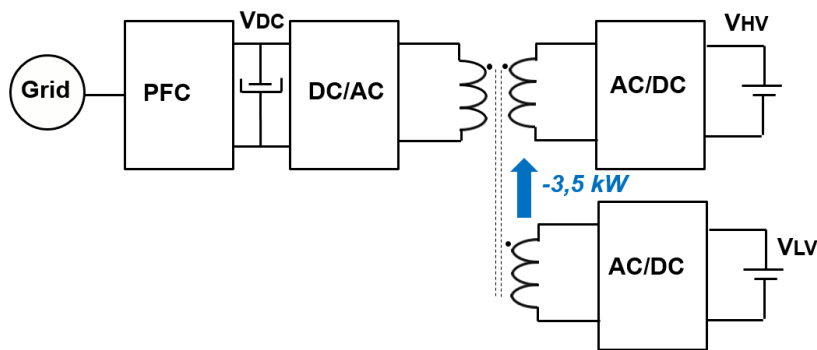


Figure 5-60: Power flow in the LDC reverse operating mode allowing the pre-charge of the HV bus.

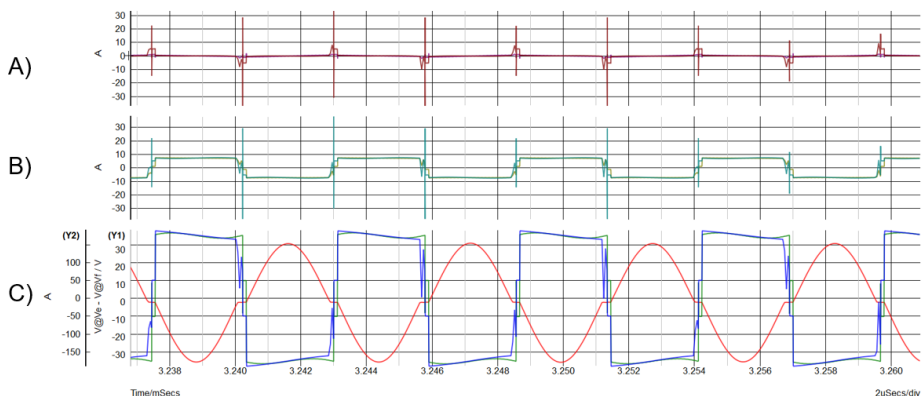


Figure 5-61: A) Current in the transformer's primary side, after and before the resonating cell. B) Current in the transformer's secondary side, after and before the resonating cell. C) Sinusoidal Voltage V_{ef} and current on the third side of the transformer. V_{LV} power $\cong -3.12$ kW

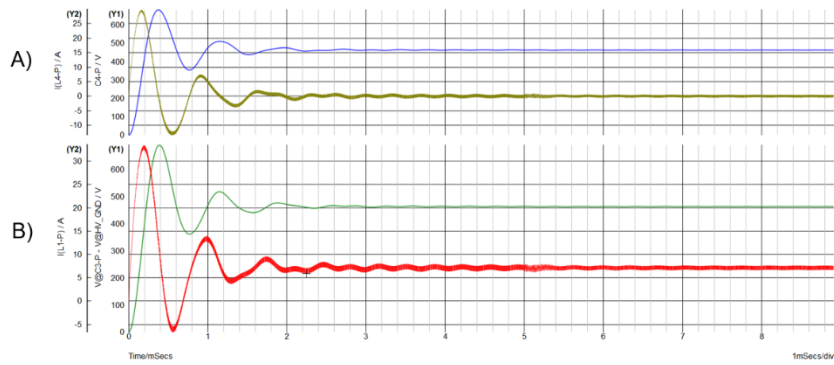


Figure 5-62: A) Voltage V_{DC} and current I_{DC} on the V_{DC} voltage bus. B) Voltage V_{HV} and current I_{HV} pre-charging the HV battery from the low voltage battery $V_{LV_power} \cong -3.12$ kW.

5.8- References

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6- The full-converter design aspects

6.1- Introduction

As presented in Chapter 1, an OBC two-stage architecture converter has the first part dedicated to rectify and compensate the converter's non-linear switching characteristic, while the DC-DC converter matches its output voltage with the HV battery providing galvanic isolation. The three-port resonant DC/DC stage has improved performance if the V_{dc} link voltage is constant, providing an optimal design by minimizing conduction power losses and volume. Because of ZVS, switching power losses are negligible in this stage and the main limitation to increase the resonant frequency is temperature increasing in the transformer.

However, the three-port converter does not regulate the voltage according to the batteries charging requirements, and therefore, a non-isolated DC-DC converter stage is still necessary to achieve the entire voltage range. In Figure 6-1, a half-bridge is connected between the Three-port resonant converter and the batteries, which allows the step-up or step-down of the voltage, depending on the power flow direction.

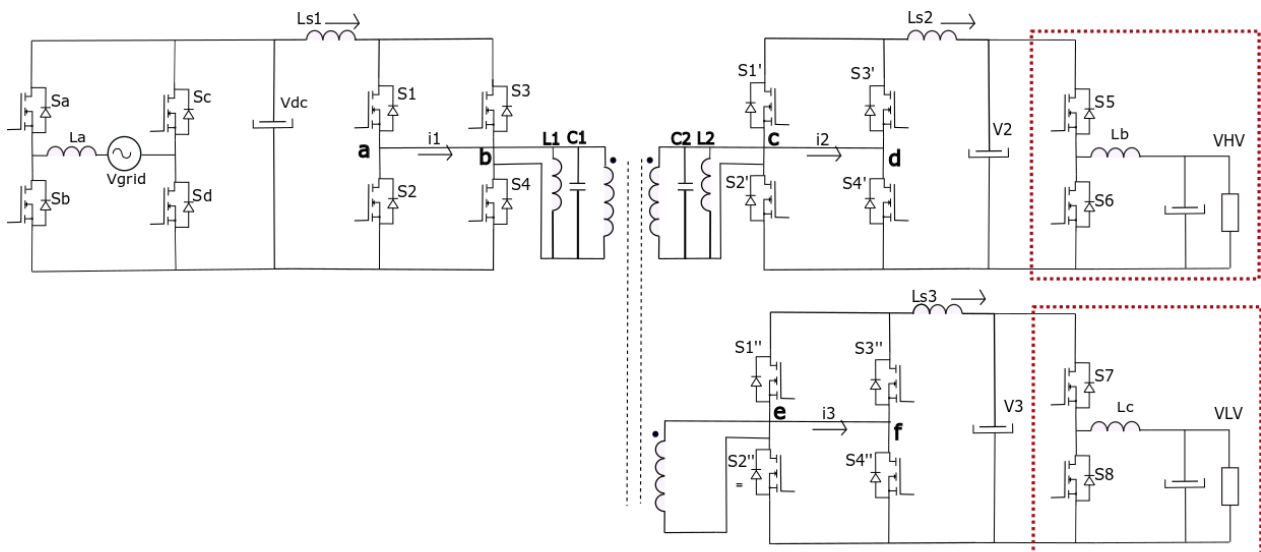


Figure 6-1: The complete architecture to include the OBC and LDC converters with bidirectional power flow.

In the PFC, the main constraints are the switching power loss at the high-frequency switched-leg and the inductor's power loss. As explained in Chapter 1, soft-switching conditions can be obtained by operating the totem-pole on discontinuous or critical modes, but the increased current ripple (for 7 kW) increases the conduction power losses. Detailed analysis must be made to select the best strategy by considering the electromagnetic emissions and the AC filter's size. On the other hand, the V_{dc}

link voltage alters the size of the capacitor bank, generally composed of electrolytic capacitors. Designers try to avoid surpassing 450 V to limit the number of series-connected capacitors for single-phase chargers at low-medium power applications.

In the non-isolated DC/DC output stage, the half-bridge is considered for a maximum input voltage of 480 VDC, the same value from the Totem pole boost PFC. The battery voltage range between 240 V and 480 V requires the step-down converter during the HV battery charging. By choosing the appropriate turn ratio in the three-winding transformer, the step-down operation can also be applied during the charging of the LV battery. For the transistors, soft-switching is required, so the next section presents some methods to reduce the switching power losses in the auxiliary converter.

6.2- Auxiliary power conversion stage for voltage regulation

In this section, we analyze the simpler converter structure to this application with the minimum possible number of components. In addition, to keep the coherence about the ZVS characteristic in the previous conversion stage, we are looking for solutions that fill this feature. Starting with the analysis of Buck converters only, some solutions for soft-switching operations are very common and can be divided into two groups: the converters with additional active devices, allowing the charge/discharge of the transistor's capacitances; and the converters with additional passive elements for resonant operation, the quasi-resonants. Some solutions are illustrated in Figure 6-2.

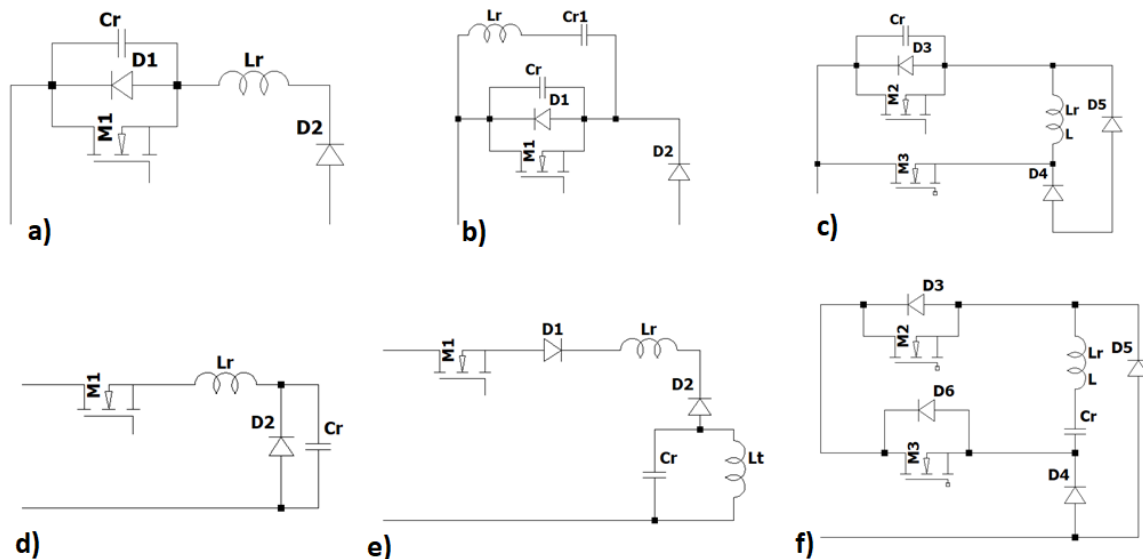


Figure 6-2: Step-down converters with soft-switching capability due to the use of additional active components and/or passive elements for resonant commutations [12].

The structures in Figure 6-2-a) and d) are the quasi-resonant solutions able to realize ZVS and ZCS, respectively, with passive elements added to the traditional Buck converter. The structures in Figure 6-2-b) and e) use additional diodes to allow a quasi-square voltage waveform with ZVS, and a quasi-square current for ZCS, both conditions obtained under fixed frequency, contrarily to the first two cases.

The structures in Figure 6-2-c) and in f) allow ZVS and ZCS, respectively, due to the use of additional active elements, a diode and a transistor in both configurations. The transistor M3 is turned-on for the discharging and charging of the energy associated with the PWM switched transistor before or after the commutation (ZVS or ZCS). In [12], these structures are compared with detailed information about limitations in frequency, duty cycles and gains.

Instead of using additional elements such as the quasi-resonant solutions, we can consider the different operating modes and try to find a balance between switching and conduction losses in the converter to find a convenient solution. Comparing the continuous (CCM), discontinuous (DCM) and triangular conduction modes (TCM)-[13] for the half-bridge connected between the Three-port converter and the batteries in Figure 6-1, we can see the advantages and drawbacks between them.

For example, in boost mode, the main problem in operating a half-bridge in CCM mode is the high reverse recovery energy, as shown in Figure 6-3. In the DCM mode, this problem does not exist anymore; however, the high-side transistor is turned-off in hard-switching in the same period, increasing the turning-off power loss. The TCM reduces one switching cycle of the high-side transistor by making the current negative. In this strategy, both transistors are turned-on under ZVS and there is no reverse recovery energy, and only power losses during turn-off in the low-side transistor need to be considered. The main drawback of this solution is the increased current ripple, which is accentuated under low power flow conditions. The frequency-control associated with the TCM is commonly used because it reduces the current ripple in low power flow by increasing the switching frequency. In [14], a hybrid control strategy associates the TCM and DCM modes. With this combination, the TCM is used during nominal and medium power operation and the DCM under low power conditions, improving the efficiency in both step-down and step-up operating modes.

Considering the application on the LV side, the conduction power losses are of major concern, but in the high voltage side, switching and conduction losses are equally important. This impact, however, can be minimized with the use of SiC MOSFETS. Figure 6-4 shows the difference between the HV and LV sides through an estimation of the transistor's power losses using the datasheet information and the three operation modes, CCM, DCM and TCM.

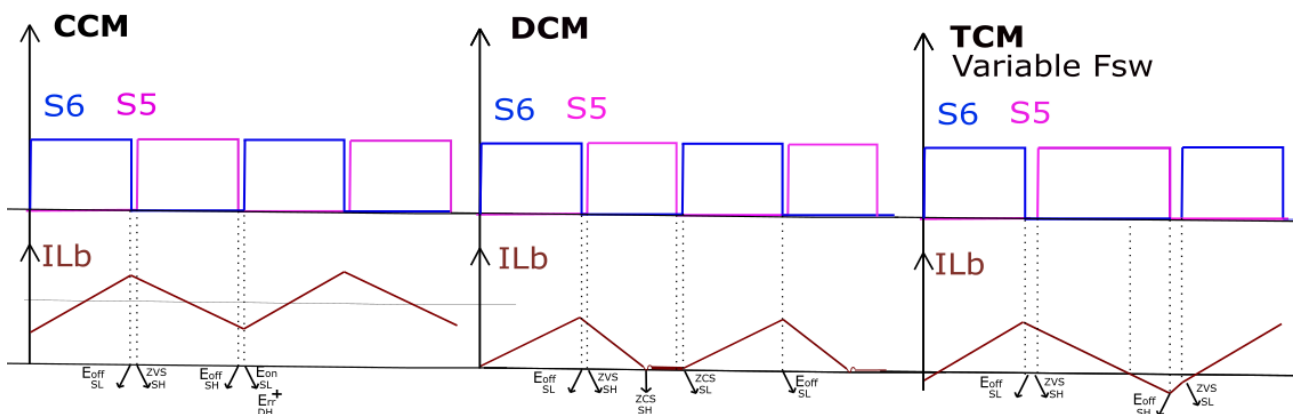


Figure 6-3: Switching conditions under continuous, discontinuous and triangular current modes.

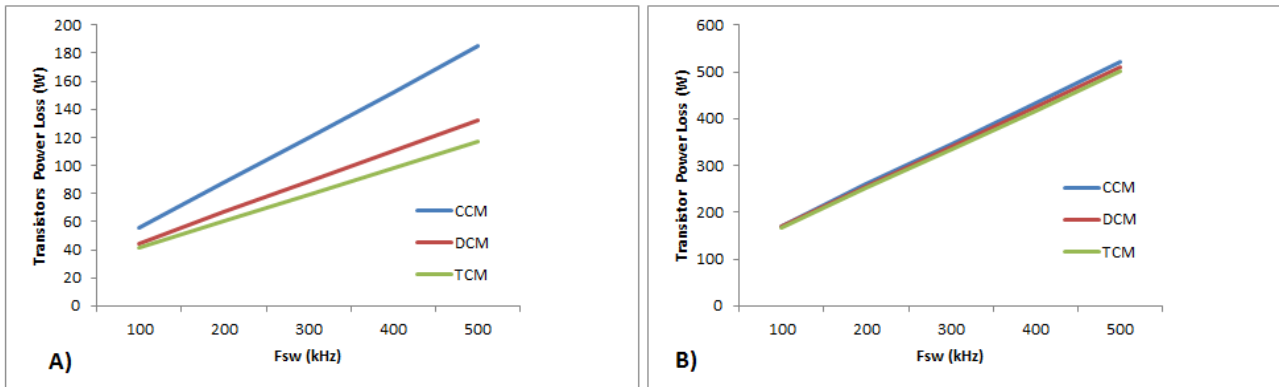


Figure 6-4: Transistor power loss estimation using the datasheet information a) High voltage side for 7 kW, $V_{HV} = 240\text{-}480\text{ V}$ with SiC MOSFET (C3M0075120J). b) Low voltage side for 3.5 kW, $V_{LV} = 12\text{-}16\text{ V}$ with Silicon MOSFET (2x IPB180N08).

On the HV side, the switching power losses have more impact on the converter efficiency and the use of these strategies allows improving its performance. Even so, in automotive applications, considering the LV side, it is still important to reduce the voltage and current spikes and stresses in the semi-conductors to achieve better reliability and robustness. Consequently, the use of additional components, such as resonant or snubber circuits to slow down the transitions on this side is an interesting solution. The circuit in Figure 6-5, [15]-[16], for example, is proposed to achieve these characteristics on the LV side.

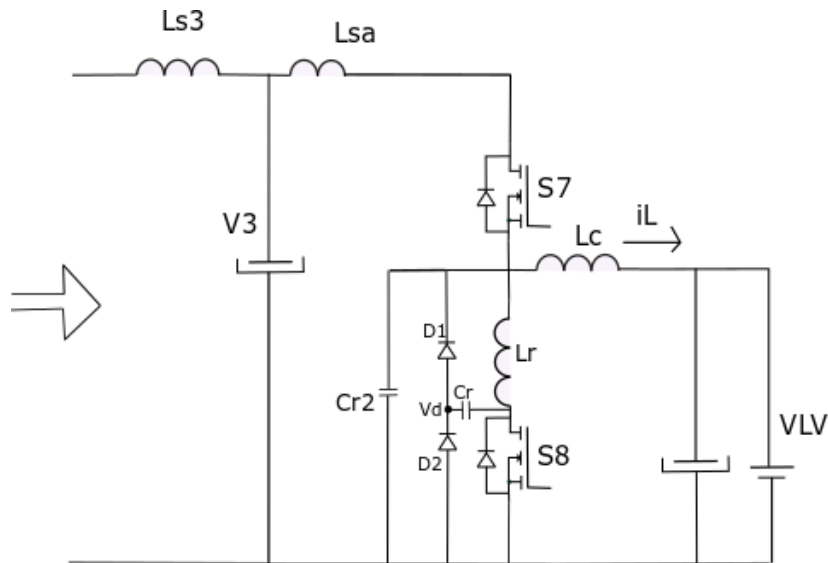


Figure 6-5: Non-isolated bidirectional stage connected between the Three-port converter and the LV side battery using a LCD snubber circuit to slow-down the voltage and current transitions.

The conduction phases in the Boost operation mode are shown in Figure 6-6. The inductor L_r will limit the current increasing on the transistor $S8$, and the capacitor C_{r2} its voltage increasing. Because of the current-fed configuration, the input current i_L is considered as almost constant.

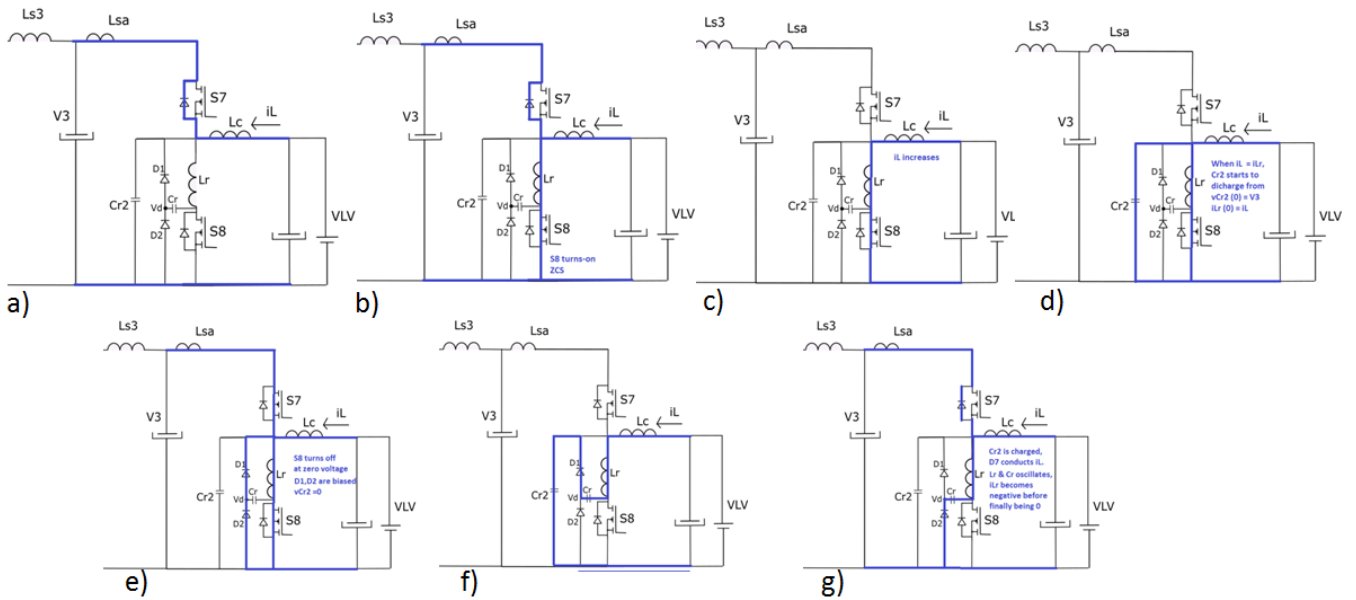


Figure 6-6: Conduction modes of the half-bridge using the LCD snubber in boost mode proposed in [15]-[16]. a) Both transistors are off and i_L decreases, but is always positive b) S8 is turned-on and its current increasing is controlled by V_{LV}/L_r c) The current is transferred to L_r . When $i_{Lr} = i_L$, the body diode from S7 is naturally blocked d) The capacitor C_{r2} is discharged from V_3 to 0 e) When $v_{Cr2} = 0$, the diodes D1 and D2 are directly biased. At the end of this phase, the transistor S8 can be turned-off at zero voltage f) C_{r2} is charged to V_{LV} while L_r and C_{r1} oscillates g) When C_{r2} is charged, the body diode D7 starts to conduct again. The current i_L is transferred to D7 and i_{Lr} decreases, until it achieves the first phase again.

The typical waveforms can be viewed in Figure 6-7 for our low voltage side application. As in most of the typical solutions using additional components, the nominal rated voltage and current are increased. Nonetheless, this kind of solution has less impact on the design of the LV side.

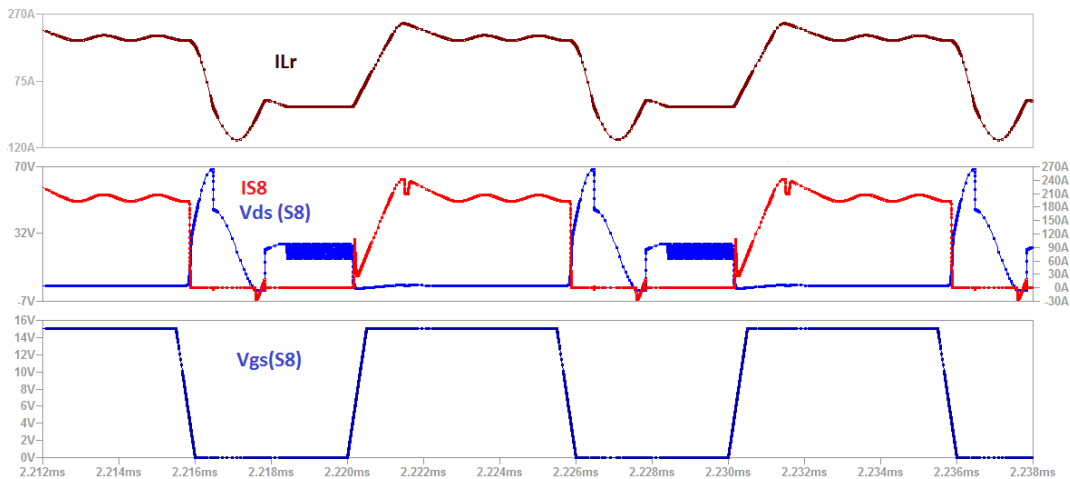


Figure 6-7: Currents i_{Lr} , i_{Ds} , voltages V_{ds} , V_{gs} in the Boost mode using the LCD snubber circuit in the half-bridge.

The quasi-resonant solution in Figure 6-2-a, applied to the bidirectional buck-boost converter represents also a good option to the LV side since it requires less additional devices in the original structure to obtain the ZVS commutations, with almost the same constraints in the voltage breakdown, as can be seen in Figure 6-8.

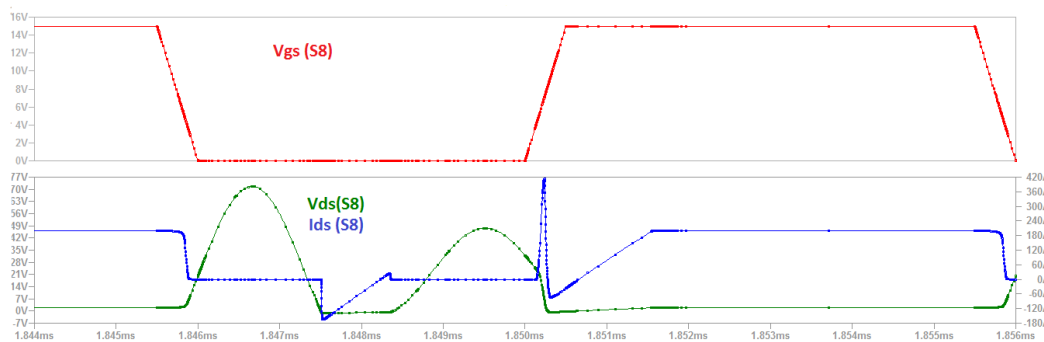


Figure 6-8: Currents i_{Lr} , i_{Ds} , voltages V_{ds} , V_{gs} in the Boost mode using the quasi-resonant circuit in the half-bridge.

6.3- Design of the output stage

The design of these stages will take into consideration some characteristics of the parallel resonant converter, such as the switching frequency and the output voltage peak. The requirements are listed below:

Parameters	Requirements HV side	Requirements LV side
Rated Power	7 kW	3.5 kW
Average Input Voltage	480 V _{DC} – 900 V _{AC}	20 V _{DC} – 38 V _{AC}
Minimum Output Voltage	240 V _{DC}	12 V _{DC}
Maximum Output Voltage	470 V _{DC}	16 V _{DC}
Operating Frequency	180 kHz	180 kHz
Output Voltage Ripple	< 1%	< 1%

Table 6-1: Requirements of the non-isolated DC-DC converter for HV and LV sides.

For the HV side, the DCM mode was preferred, and compared to TCM, has a reduced current ripple for 7 kW. Despite the increased turn-off energy and loss in the junction capacitances, the reverse recovery energy is eliminated, and the use of SiC MOSFET, the same technology used in the Three-port resonant converter, minimizes these problems.

The DC voltage transfer function:

$$M_V = \frac{V_o}{V_{in}} = D = [0.5 - 0.95]$$

The load variation occurs from 7 kW to zero while the battery is being charged. The initial battery voltage is 240 V, and the maximum current is limited by the PFC stage, controlled at 480 V, which means a maximum DC current of 15 A. The equivalent resistance range is [16, 32, 240 Ohm]. Therefore, when the battery voltage achieves the 2° phase illustrated in Figure 6-9, the voltage regulation is no longer necessary and the non-isolated DC-DC converter is in standby mode.

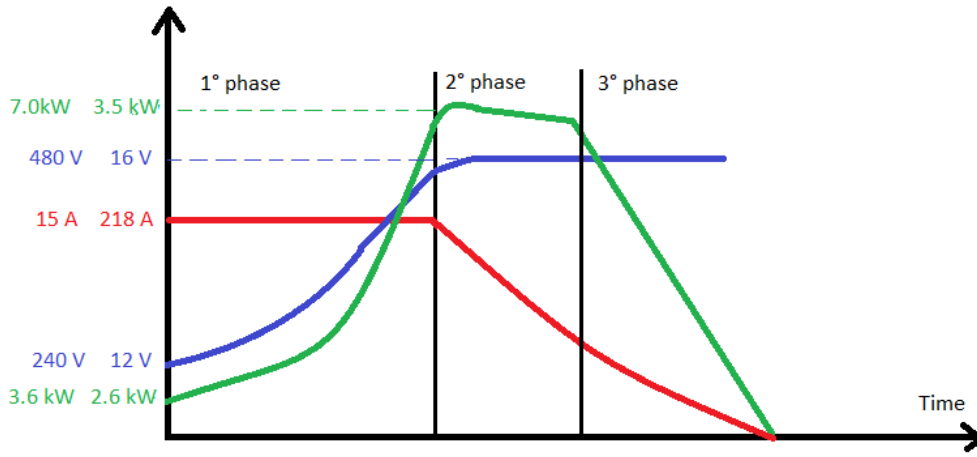


Figure 6-9: Phases during the battery charging process, voltage, current and output power.

The inductance indicates the boundaries between continuous, critical and discontinuous modes. The inductor current in discontinuous mode goes to zero at the end of the off period. Thus, the average current in the boundary between continuous and discontinuous modes [17] for constant input voltage is:

$$I_{L_{Boundary}} = \frac{1}{2} I_{L_{Peak}} = \frac{D}{2L} T (V_2 - V_{HV}) = \frac{D}{2L} T V_2 (1 - D)$$

In step-up mode, for reverse power flow, the output voltage remains constant, therefore:

$$I_{L_{Boundary}} = \frac{T V_2}{2L} D (1 - D)^2$$

At 180 kHz, the same frequency of the Three-port resonant converter, the inductance is 9 μ H. The capacitor is considered to be so large as to yield a maximum of 1 % of voltage ripple. In Figure 6-3, we consider the current waveform in DCM mode, and its ripple compensated by the output capacitor:

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{1}{2} \frac{\Delta L}{2} \frac{T}{2} \frac{1}{C} = \frac{V_{in} T D(1-D)(T_{on}+T_{off})}{8LC}$$

$$C = 10 \mu\text{F}$$

The specifications are presented in Table 6-2. The inductor full design information is indicated in the Annexes.

Component	Value / Stress (HV)	Value / Stress (LV)
Frequency	180 kHz	180 kHz
Maximum power	7 kW	3.5 kW
Inductance	9 μ H	0.5 μ H
Inductor max DC current	24 Arms	281 Arms
Inductor maximum current	42 A peak	310 peak
Inductor estimated Volume	10.6 cm ³ (Toroid)	51.4 cm ³ (E core)
Inductor Max. Power Loss	14 W	39 W
Output capacitance	10 μ F	0.68 mF
Output capac. arrangement	2xUCY2H220MHD3TN	3xUBY2A221MHL+8xCKC21C104JW
Transistor Max. cur. /volt.	16 Arms / 480 V	291 Arms/ 72 V

Transistor Reference	C3M0075120J	IPB180N08S4-02 (2 in parallel)
Resonant capacitors C_{r1}, C_{r2}	-	1.35 μ F / 0.5 nF
Resonant inductor L_r	-	64 nH
Clamp diodes D_1, D_2	-	32 V / 18 A

Table 6-2: Non-isolated DC-DC converters specification.

The LCD clamp is an interesting solution that allows soft-switching without frequency variation or high current ripple on the LV side. Despite the increased voltage and current peaks, we had opted for this solution since the conduction power losses are more accentuated on this side. The below equations allow the design of the clamp components according to the maximum current and voltage applied on the switches. These equations are derived from the analysis of the conduction modes described in Figure 6-6 and had been detailed in section 6.8.2. The design of the half-bridge is made in continuous mode. The design specification is presented in the second column of Table 6-2.

$$I_{Transistor\ Max} = I_{Lr\ Max} = I_{Ls3} + V_3 \sqrt{\frac{C_{r2}}{L_r}} \quad (1)$$

$$V_{Transistor\ Peak} = I_{Ls3} \sqrt{\frac{L_r}{C_{r1}}} + V_3 \sqrt{\frac{C_{r2}}{C_{r1}}} \quad (2)$$

$$L_r = \frac{V_3}{I_{Ls3}} t_o = \frac{V_3^2}{P_{out}} t_o \quad (3)$$

6.4- Efficiency and power loss analysis

The conversion efficiency performance needs to be estimated by considering the additional stages for voltage regulation. The conversion efficiency of the Three-port resonant part was investigated in Chapter 5, and we see how it can be improved by using transistors with smaller conduction resistances, and how the transformer performance is affected by the switching frequency.

The battery charging profiles represented in Figure 6-9 are used now to estimate the total power conversion efficiency for the different modes: OBC and DC-DC standalone operations, in Figure 6-10, and Figure 6-11, respectively. During the charging modes, the step-down DC-DC is required during the 1° phase and part of the 2° phase for the OBC. During the 3° phase, when the voltage is constant, the high-side transistor is always on. For the LDC mode, the battery requires the use of the auxiliary stage during the 3° phase also: this is because even during the phase of constant voltage, the auxiliary converter still needs to regulate the voltage on the LV battery by using a duty-cycle different from 1.

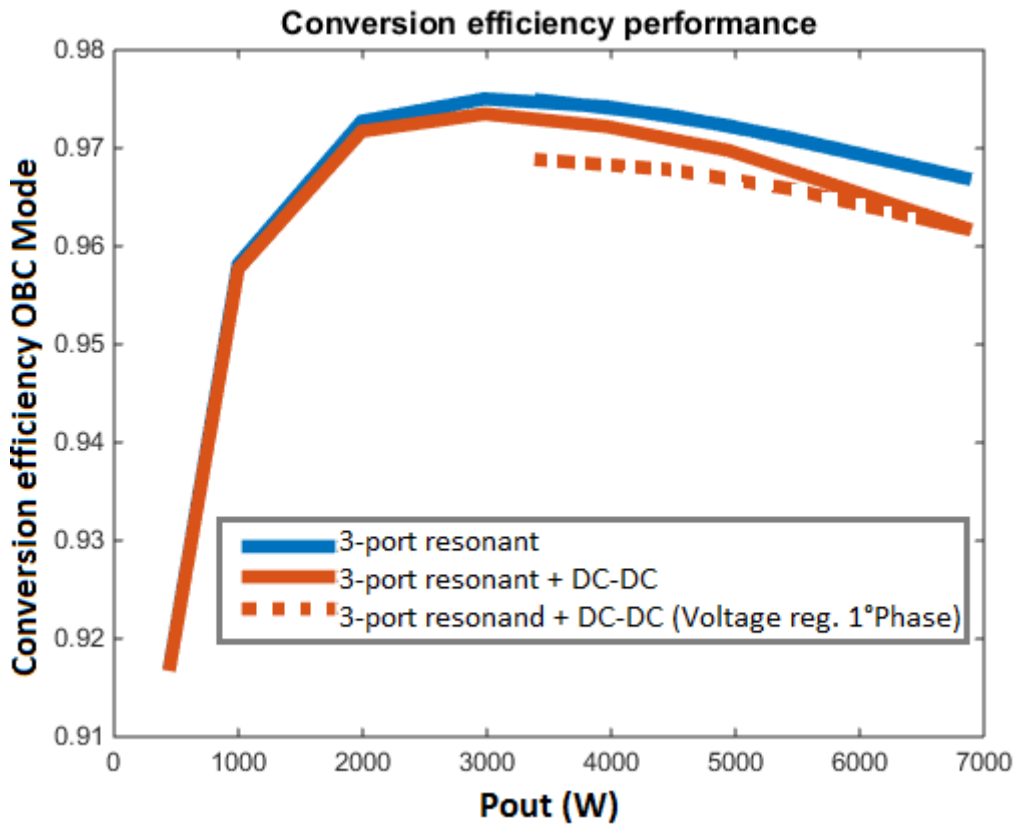


Figure 6-10: Conversion efficiency simulating the HV battery charging process.

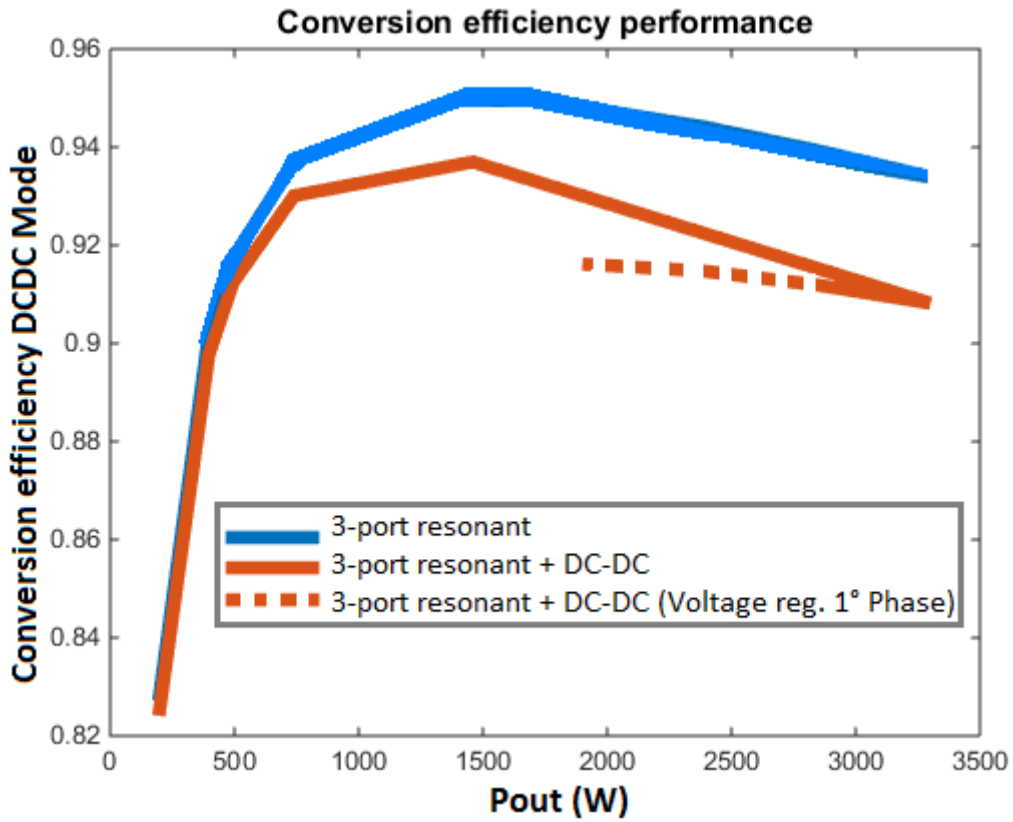


Figure 6-11: Conversion efficiency simulating the LV battery charging process.

The maximum power losses are presented in Table 6-3 and Table 6-4, respectively, for the OBC and LDC converters. The efficiency obtained for the OBC does not include the input AC-DC converter,

and therefore the values indicated in this section do not represent the entire conversion. Even so, the parallel resonant converter associated with an auxiliary converter for voltage regulation presents good performance for this particular operation mode. For the LDC converter, however, the impact of the high current present on this function limits the conversion performance, and the use of a pre-regulation stage present on the HV side instead of LV side can lead to better results. However, it will imply in a bidirectional structure able to step-down and up the voltage connected in cascade with the HV battery, also affecting the performance of the OBC.

Block	Description	Value
3-Port Resonant Converter	Transistors Power Loss	131.2 W
	Total Gate Loss	4.5 W
	Transformer Total Loss	111.12 W
	Inductor Filter	86 W
	Resonant capacitors	1.14 W
	Resonant inductors	8.65 W
	Total Power Loss	342.61 W
DC-DC voltage regulation stage	Transistors	26.43 W
	Gate Loss	1.5 W
	Buck/Boost inductor	14.17 W
	Output filter	1.25 W
	Total Power Loss	33.35 W

Table 6-3: Power loss distribution for OBC converter.

Block	Description	Value
3-Port Resonant Converter	Transistors Power Loss	100.32 W
	Total Gate Loss	6.5 W
	Transformer Total Loss	54.42 W
	Inductor Filter	53 W
	Resonant capacitors	1.2 W
	Resonant inductors	8.55 W
	Total Power Loss	224.12 W
DC-DC voltage regulation stage	Transistors	47.84 W
	Gate Loss	1.1 W
	Buck/Boost inductor	38.29 W
	Output filter	28.48 W
	Total Power Loss	115.71 W

Table 6-4: Power loss distribution for LDC converter.

6.5- The AC-DC Bidirectional Bridgeless Totem-pole PFC converter

Although the focus of this dissertation is on the Three-port current-fed parallel resonant converter, the conversion efficiency of the AC-DC stage has a significant impact on the OBC operation. In this way, we present a quick design to estimate the power losses and volume of this part. The design requirements are presented in Table 6-5.

Mode	PF	THD Current	P/ I _{RMS}	AC Voltage	Frequency
G2V	0.95	< 5% (P > 1 kW)	7 kW / 32 A	85- 265 V	45- 60 Hz
V2G	0.7 – 1.0	< 5% (P > 1 kW)	7 kW / 32 A	230 V	50 Hz

Table 6-5: Main requirements for the AC/DC converter in a single-phase configuration.

The bridgeless totem-pole converter was chosen because of its low number of devices and smaller conduction power losses compared to other structures. Controlling one of the legs in buck/boost mode, produces a frequency spectrum similar to the bipolar modulation in the single-phase inverter, where harmonics multiple of the main switching frequency appears, even the second harmonic with its sidebands, as verified in Figure 6-12.

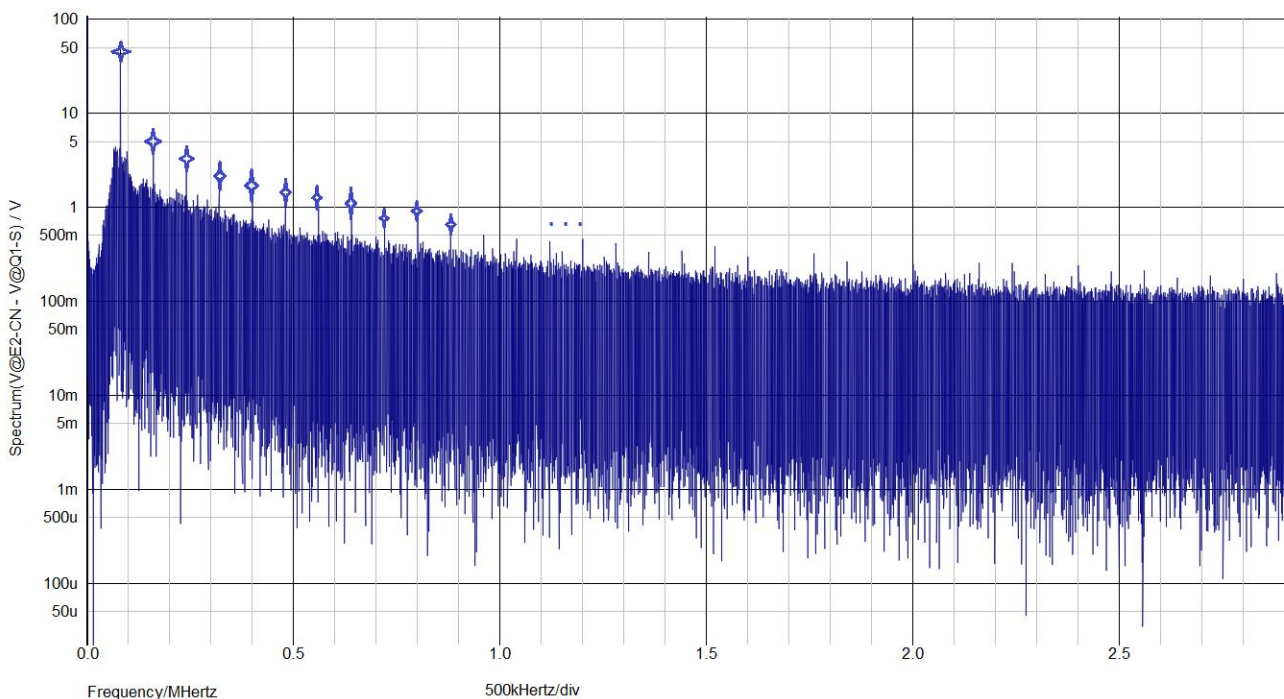


Figure 6-12: Example of a frequency spectrum of the input current from the AC grid produced with a bridgeless totem-pole PFC switched at 80 kHz. (500 kHz/div).

The converter can be operated in CCM (continuous conduction mode), CCrM (critical conduction mode), and DCM (discontinuous conduction mode) modes. In the CCM mode is not possible to operate the transistors under ZVS, and it has high reverse recovery energy from the high-frequency switched transistors. In the DCM mode, the power factor performance deteriorates because the current remains zero during a time interval longer than the time required for the voltage transition. Therefore, the CrCM mode, in general, reduces the switching power losses, increases the power density, and keeps a minimum power factor. Nevertheless, for the power application of 7 kW, the RMS current is significantly increased, and a more accurate analysis must be made.

6.5.1- Comparing the CCM and CrCM modes

In Figure 6-1, the transistors Sa and Sb are controlled in high-frequency during the boost and buck modes, respectively, for G2V and V2G modes. The second leg performed by Sc and Sd is commutated at the low-frequency line, and each transistor is ON during a half-period. These switches have higher conduction power losses, while Sa and Sb have significant switching power losses. The control schema of the voltage regulation mode in CCM is shown in Figure 6-13. The current reference is obtained from the voltage controller and is changed according to the power flow direction: its signal is positive when the converter operates with direct power flow (G2V mode) and negative with reverse power flow, V2G mode. The DC voltage viewed as a perturbation can be added at the end of the loop to make the system more robust, the feed-forward strategy.

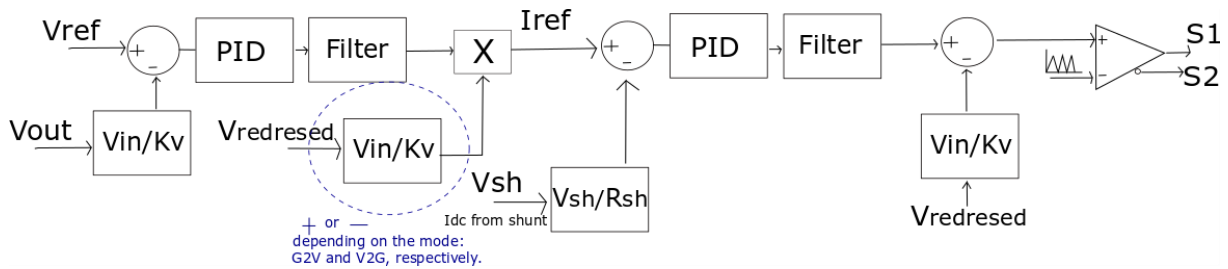


Figure 6-13: Voltage control loop for the CCM mode.

In CCM, the frequency is constant and the voltage can be written as:

$$v_{ac} = \frac{L I_{Lmax}}{T_{on}}; \quad v_{ac} - V_{dc} = \frac{L I_{Lmax}}{T_{off}}$$

The switching frequency, the minimum input AC voltage (85 Vac), and the current ripple settled around 20% define the minimum inductor value. Using the above equations, the minimum inductor value is:

$$L_{min} = \frac{V_{acmin} (V_{dc} - V_{acmin})}{F_{sw} V_{dc} \Delta I}$$

The DC-link capacitor is calculated based on the minimum Vdc voltage and the low-frequency ripple at twice the line grid frequency. The capacitance value must also handle the DC-link voltage bus during an entire half-period:

$$C_I = \frac{P_{max}/V_{DCmin}}{2(2\pi F_{grid}) V_{DCmin} \Delta V}; \quad C_{II} = \frac{P_{max} (2 \times 20ms)}{V_{dc}(V_{dcmax} - V_{dcmin})}$$

The maximum voltage in the device is the maximum DC output voltage that is the same voltage level applied in the resonant converter.

$$V_{DSmax} = V_{DCmax}$$

The MOSFET conducts the same input current:

$$I_{acmax} = I_{acmax} = I_{ac} \sqrt{2} \text{ (considering a sinusoidal current)}$$

$$I_{average} = \frac{1}{T} \int_0^{\pi} (I_{acmax} \sin \omega t) dt = \frac{I_{ac} \sqrt{2}}{\pi}$$

$$I_{rms} = \sqrt{\frac{2}{T} \int_0^{\pi} I_{acmax}^2 \sin^2(\omega t) dt} = \frac{I_{acmax}}{2\sqrt{2}}$$

Figure 6-14 presents the power losses depending on the switching frequency in the power inductor and the transistors used in the high-frequency leg.

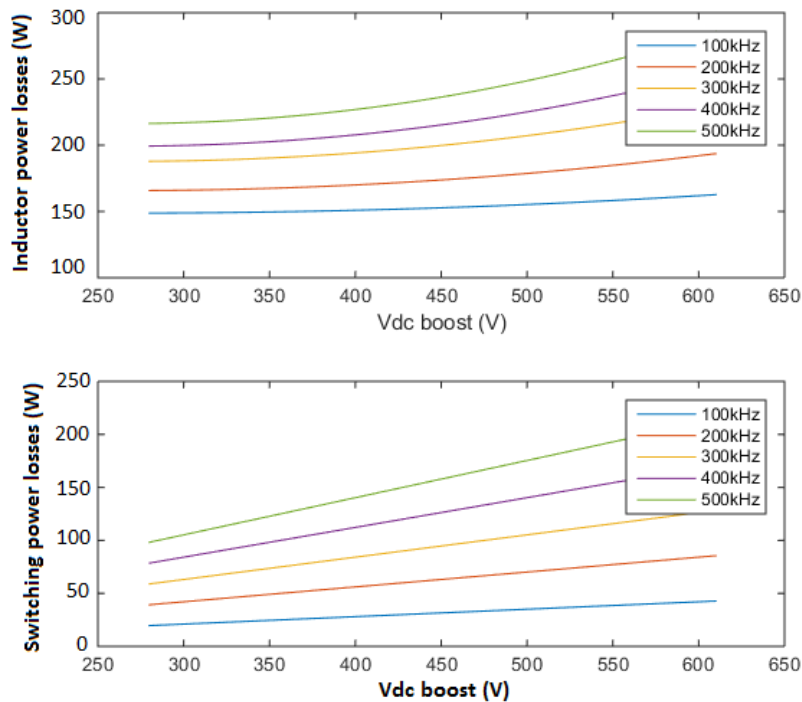


Figure 6-14: Power losses in the buck/boost inductor and switching power losses in the transistors (C3M0075120J) depending on the Vdc link voltage for different switching frequencies.

For the semiconductors selection, it is necessary to have devices with fast recovery characteristics to avoid crossover problems, such as SiC MOSFETS, like the one used in Figure 6-14. In the CrCM mode, the inductor value is reduced, allowing a quasi-zero voltage switching during the transistor turning-on. The switching frequency is minimum to complete demagnetize the inductor current:

$$L_{max} = \frac{V_{ac_{min}} (V_{dc} - V_{ac_{min}})}{F_{sw_{min}} V_{dc} (I_{peak} - 0)}$$

The switching power losses in the transistors are reduced, and the inductor value as well. However, as the current ripple is increased, the conduction power loss in the transistors and inductor increases. Considering the converter's total volume for the smallest inductance, the energy used to choose the magnetic core is not necessarily decreased since the maximum current peak is maximized (7 kW, 32 A_{RMS}, 54 A_{peak}). Besides, the EMI filter deals with a larger frequency range according to the maximum and minimum DC-link voltage. In the reverse operation mode, the frequency range is smaller than the direct mode, mainly because light power operation is not usually required. Added to that, the power factor form of the current is smaller, which is not desirable considering such a high current value application. An improved factor form can be obtained using two-interleaved legs when two inductors handle the current ripple with smaller magnetic cores and better heat dissipation. It is clear that to pass from CCM mode to the CrCM, the gain obtained in the switching power loss must not be compensated by the increased power losses in the inductor.

In the CrCM mode, the switching frequency is variable, and the on-time interval is constant. In Figure 6-15, we present the current mode control loop for the Bridgeless totem-pole.

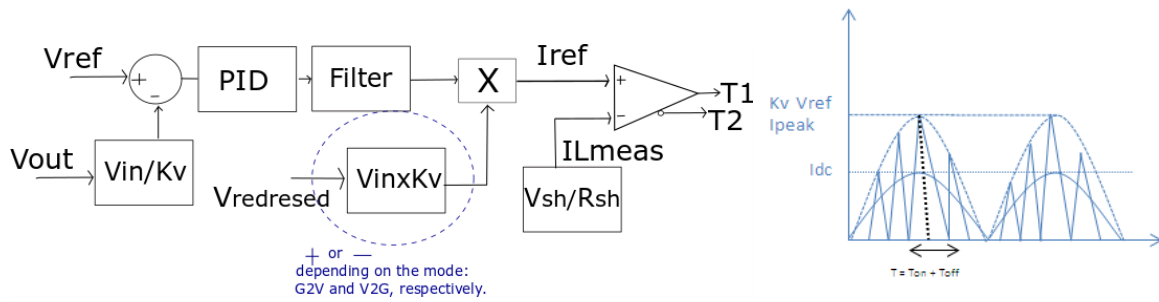


Figure 6-15: Current control loop for the CrCM mode.

K_v is a constant gain used to obtain the current reference, as can be verified in the control loop.

$$V_{ref} = k_v v_{ac} = I_{Lmax}$$

$$v_{ac} = L \frac{I_{Lmax}}{T_{on}} \Rightarrow k_v = \frac{T_{on}}{L}; \quad V_{ac} - V_o = L \frac{I_{Lmax}}{(T - T_{on})}$$

$$I_{LAverage} = \frac{I_{Lmax}}{2}; \quad I_{LAverage} = \frac{2 V_{ac}}{\pi L} T_{on}; \quad T_{on} = \frac{L I_{Lmax}}{V_{ac}}$$

$$\frac{V_o - V_{ac}}{L} = \frac{I_{Lmax}}{T_{off}}; \quad T_{off} = \frac{L I_{Lmax}}{V_o - V_{ac}} \quad V_o = V_{ac} \frac{T}{(T - k_v L)}$$

Considering the design requirements from Table 6-5 and the DC-link voltage fixed at 480 V, the designs in CCM and CrCM are compared in Table 6-6. The components selection and power loss estimation are present in section 6.8.4.

MODES	L_{nom} (μ H)	ΔI (A)	Energy for magnetic core (mJ)	Magnetic core volume (cm^3)	Loss inductor (W)	Loss transistors (W)
CCM	100 μ H	8.97	198	29.8	415	58.4
CrCM	30 μ H	28.8	102	16.2	606	46.4

Table 6-6: Design comparison between CCM and CrCM for a Bridgeless totem pole of 7kW. The complete design is shown in section 6.5.4.

The Bridgeless Totem pole in the CCM presents less power loss. The simulation of this circuit is presented below for the G2V and V2G modes, considering the CCM case. [18] contains the complete information for the control of the current and voltage loops. Figure 6-20 shows the estimation of the conversion performance of the OBC, including the PFC stage controlled in CCM mode at 100 kHz.

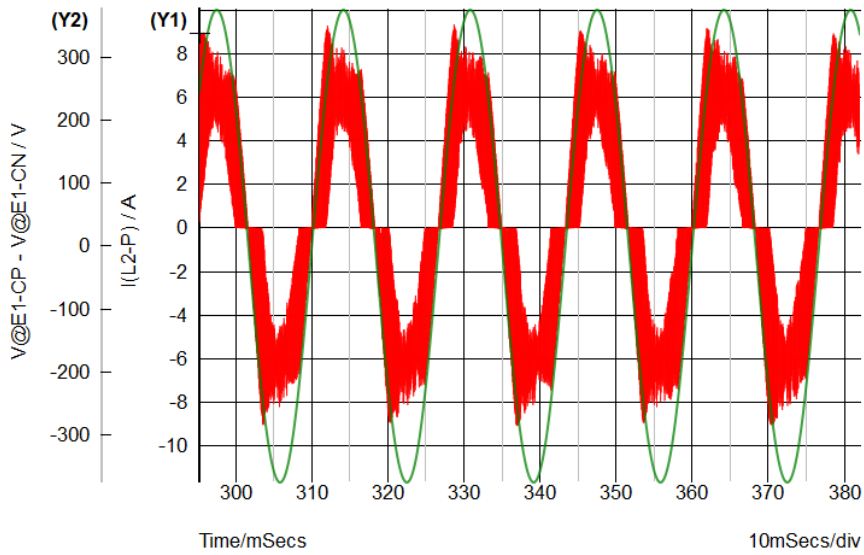


Figure 6-16: AC grid voltage and the current in the AC inductor for the G2V mode. $V_{dc} = 400V$, $P = 1.5kW$.

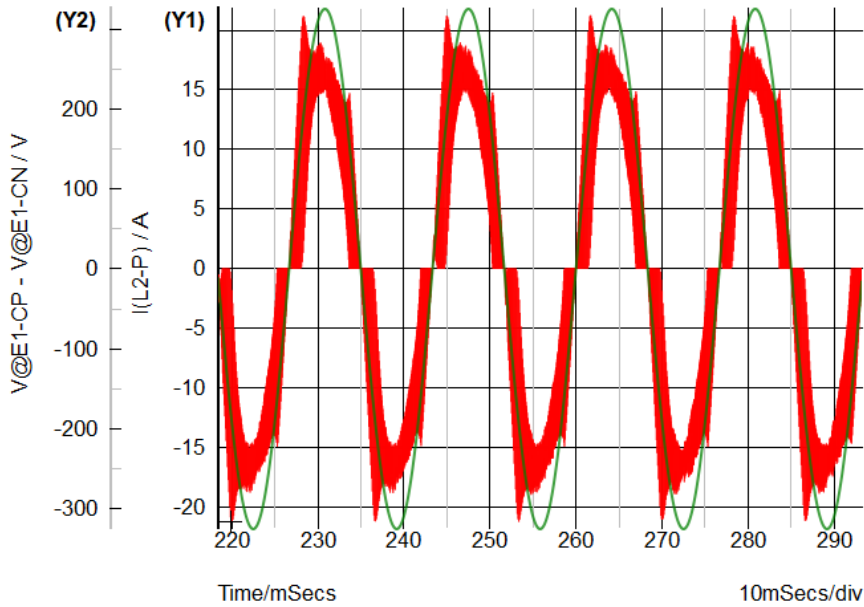


Figure 6-17: AC grid voltage and the current in the AC inductor for the G2V mode. $V_{dc} = 400V$, $P = 5.0kW$.

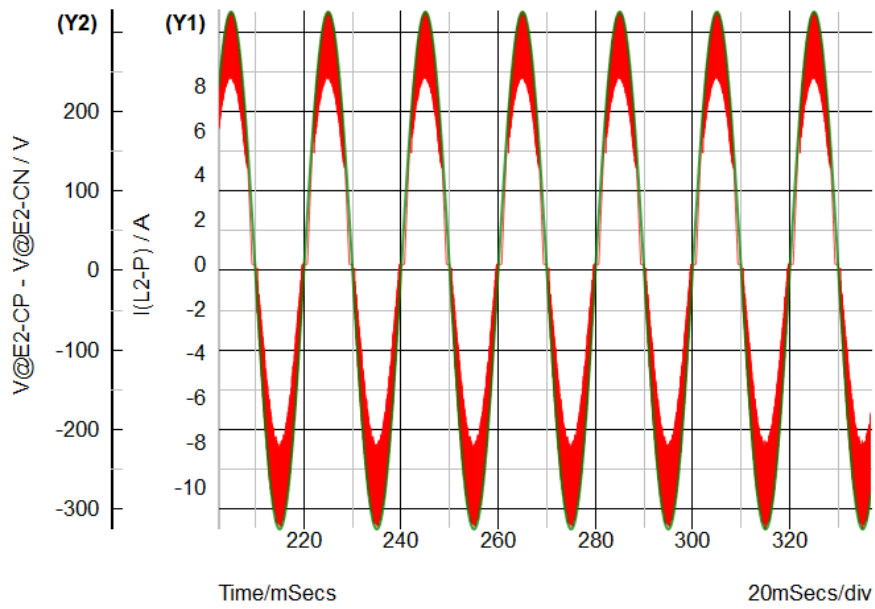


Figure 6-18: AC grid voltage and the current in the AC inductor for the V2G mode. $V_{dc} = 400V$, $P = 1.5 kW$.

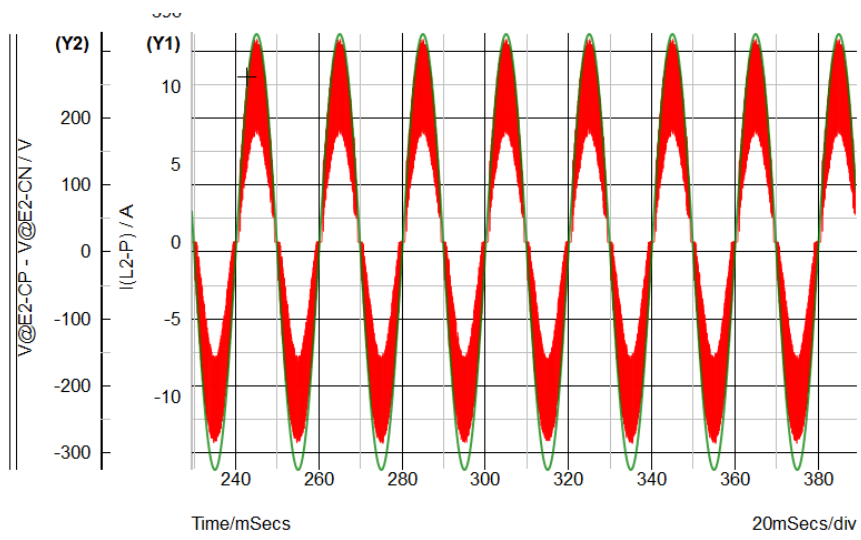


Figure 6-19: AC grid voltage and the current in the AC inductor for the V2G mode. $V_{dc} = 400V$, $P = 5.0 kW$.

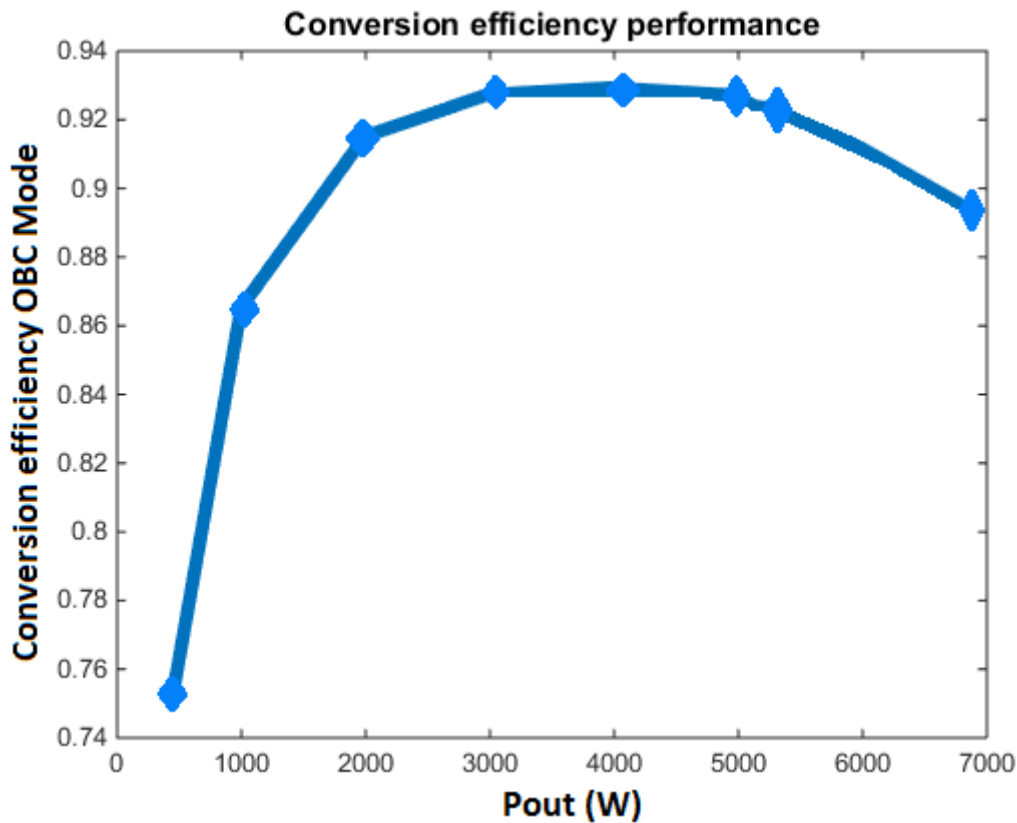


Figure 6-20: Conversion efficiency simulating the HV battery charging process, containing the three-conversion stages: PFC + Parallel resonant converter+ output voltage regulation stage.

6.6- Lifetime Prediction

The lifetime prediction and reliability study for the integrated power unit can be explored to provide additional parameters used on the onboard and DC-DC converter's design specifications, especially because some elements are shared to execute both converter functions. In the real product, however, other methods are used to estimate the converter's lifetime. Real accelerated thermals tests are applied to stress each one of the components and the entire converter to represent the product's real lifetime. Using a mission profile makes possible the estimation of a mean time to failure of the three-port converter. The approach consists of first determining the thermal stress on each power device, such as semiconductors, transformer, capacitances, inductances, taking into account the number of times each cycle is repeated in the mission profile over a year. Electrical and thermal models are needed for each component to determine the temperature increase. Time-dependent simulations are made in the converter architecture, and the results are imported into a Matlab script with the FIDES model and the method to count the cycles flow to calculate the failure rate for the mission profile. This model is not applied to electric vehicles in practice, but the acceleration factors used in the failure estimation are based on the same laws. Besides, FIDES prediction's model is an easy-to-use method of easy access and offers some facilities in order to include new device prediction models [1] in its handbook.

The methodology FIDES described in [2]-[3] is a result of a study that began in 2001 by 8 companies in France, and proposes a methodology for electronic system reliability. The methodology considers failure rates from the manufacturing, design processes, and the system's life profile, where the constraints as thermal, electrical, and mechanical overstress are also evaluated. The failure rate (λ) is a constant and is based on the useful life of the system containing the contribution of each component in the power converter, as represented in equation (1):

$$\lambda_{Converter} = \sum_i \lambda_{Component_i} \quad (1)$$

For each component, λ is the product of three factors, as represented in equation (2): the part manufacturer acceleration factor, $\pi_{PartMan}$, involving the manufacturer qualification process on the component development; the process acceleration factor, $\pi_{Process}$, that includes quality and technical control procedures during the product lifecycle; and the physical failure rate, $\lambda_{Physical}$, which includes the physical constraints during its operational useful life, as temperature, humidity and mechanical vibrations [2]-[3].

$$\lambda_{Component} = \lambda_{Physical} \pi_{Process} \pi_{PartMan} \quad (2)$$

The output power profile presented in Figure 6-21 is used to determine the failure rate of the converters. It is assumed that the OBC is started at once a day. The number of times the LDC converter is started is evaluated considering the number of times the vehicle is been driven. It is acceptable to consider that the LDC converter starts at least the same number of times the operation of the propulsion inverter is required. For the power levels discussed in this thesis, the OBC works about 3 hours by day while the LDC converter 8, between the operation of the inverter and the OBC. The failure rates obtained with FIDES methodology are expressed in a calendar of a yearly profile (8760 hours) where each phase described in Figure 6-21 must be weighted by its duration 365 times during a year.

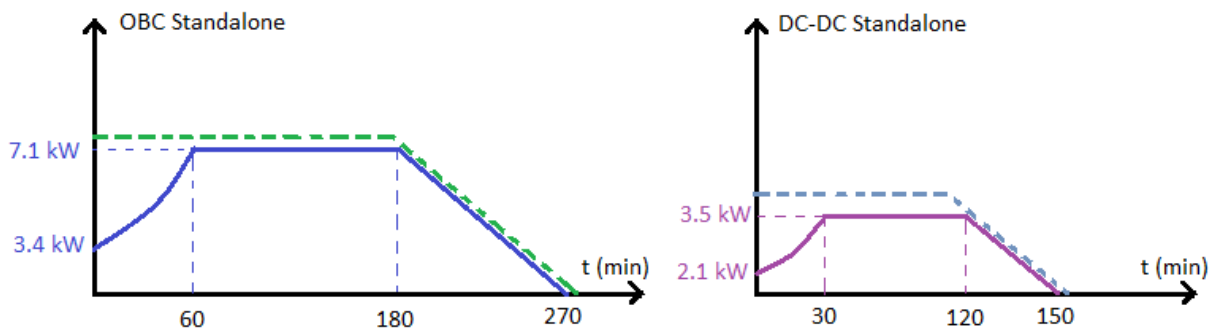


Figure 6-21: Output power used in the mission profile for the Three-port parallel converter in OBC and LDC functions.

Three groups of components are submitted to the power load profile: the magnetic components consisting of the high-frequency transformer, the resonant and DC filter inductors, the resonant capacitors and the semiconductors from high and low voltage sides.

6.6.1- Reliability of active components

The acceleration and physical factors in (2) are different for MOSFETS, IGBTs, diodes, SiC MOSFETS and GaN transistors. As mentioned in [4], these factors are well known for mature transistors, but not for the GaN and SiC transistors. According to the results available in [5], the failure mechanisms associated to the new transistors starts in the substrate and in the seed crystal, and the growth process can lead to many defects. In this same paper, a failure is defined when the process results in 20% parameters variation. The challenge is to identify the failure mechanics and how to model them. The efforts made in the development of lifetime models for SiC transistors seems to be a little more in advance compared to the GaN, but in both cases more advances are still necessary.

In FIDES, the physical failure rate for active semiconductors is defined as:

$$\lambda_{\text{Phy}} = [\sum_{\text{PhyContribution}}^N (\lambda_0 \pi_{\text{acceleration}})] \pi_{\text{induced}} \quad (3)$$

It has three contributions: the intrinsic failure rate of the components, the acceleration factor due to the thermal fatigue, and the induced factor associated to the environmental conditions impacting on mechanical stresses.

According to [6]-[7], for SiC, the main failure mechanisms related to temperature-induced and mechanical stress are bond wire and die-attach degradation. This is mainly observed for power-modules, where the use of bonding technology is the same for Si-IGBT, thus leading to the same failure mechanisms. However, because SiC uses a smaller chip area, the physical mechanisms need to be further investigated to improve their thermal model. However, despite this lack of complete information, the terms used in FIDES can be extended to include new devices. If we look at each term present in the physical failure rate (3), we can modify the necessary ones to include the SiC MOSFET used in our application.

The induced factor, π_{induced} , represents the overstress due to the physical position of the converter. It includes the weight of different environment conditions affecting the overstress and the sensitivity of the device physical properties under these conditions. It also has a policy to qualify its development phase, supervised by its manufacturer. These elements are reunited in (4).

$$\pi_{\text{induced}} = (\pi_{\text{placem.}} \pi_{\text{appl.}} \pi_{\text{rugg.}})^{0.511 \ln(C_{\text{sensitivity}})} \quad (4)$$

An audit questioner proposed in FIDES [4] (page: 50-54) is applied to evaluate the criteria for mechanical and thermal overstress for power transistors, transformer, capacitors, and inductors.

The product between the intrinsic failure rate, λ_0 , and the acceleration factor, $\pi_{\text{acceleration}}$, has the influence of five constraints: thermal constraints related to the junction temperature, casing and solder joints, and the influence of humidity and mechanical vibrations, as presented in (5):

$$\lambda_{phy} = \sum_i^{Phases} \frac{t_{annual}}{8760} (\lambda_{OTH}\pi_{TH} + \lambda_{THCasing}\pi_{THCasing} + \lambda_{THSolder}\pi_{THSolder} + \lambda_{Hum}\pi_{Hum} + \lambda_{Mech}\pi_{Mech}) \pi_{induced} \quad (5)$$

The thermal acceleration factor π_{TH} is modelled by Arrhenius equation and one of the physical tests associated with this model is the High Temperature Operating Life (HTOL), executed according to the JEDEC EIA JESD-22-A108A:

$$\pi_{TH} = e^{\frac{E_a}{k} \left(\frac{1}{T_{use}} - \frac{1}{T_{stress}} \right)} \quad (6)$$

The activation energy, E_a , is assumed as 0.7 eV for Si FETS, considered as the activation energy associated with the thermo-electrical failure mechanism; k is the Boltzmann constant, 8.617×10^{-5} eV/K. T_{use} is the reference temperature of the component and T_{stress} is the temperature achieved due to the stress. This energy for SiC MOSFETS had been estimated between 0.3 and 0.6 eV for the 2nd generation of Cree devices, the same used in our power converter. The maximum stress temperature allowed for the device is 150 °C.

The thermal acceleration factor of the case π_{THCase} and the solder joints $\pi_{THSolder}$ use the Norris-Landzberg model and represents the fatigue mechanism due to temperature variation. In FIDES, it appears with an equivalent E_a of 0.122 eV for both parts, case and solder joints considering the TO-247 package. In [4]-[5], the failure mechanisms associated with the bonding wire and die attach in SiC are considered to be very close to the ones found in Si devices, and in this text, we also consider that it has the same impact:

$$\pi_{THX} = \left(\frac{12 N_{Cyannual}}{t_{annual}} \right) \left(\frac{\min \theta_{cy}}{2} \right)^P \left(\frac{\Delta T_C}{\Delta T_o} \right)^m e^{\frac{E_a}{k} \left(\frac{1}{T_o + \Delta T_o} - \frac{1}{T_{Cm}} \right)} \quad (7)$$

$N_{Cyannual}$ and t_{annual} are the annual n° of cycles and the annual duration of the phase respectively.

Θ_{Cy} is the cycle duration in hours.

T_{Cm} , T_o , ΔT_o and ΔT_{Cy} are the maximum cycle temperature, the reference temperature, the reference thermal amplitude and the thermal amplitude of the cycle, respectively.

m is the fatigue coefficient of the material

P is the acceleration power of duration factor, 1/3 in FIDES.

The relative humidity π_{Hum} and mechanical vibrations π_{Mech} acceleration factors are based on Peck's and Basquin's models; and a same influence of those parameters is considered for the Si and SiC power devices. The complete equation can be verified in [2]-[3]. In reality, the humidity problems are reported as more accentuated with SiC [9] due to larger electric fields to which these devices are exposed. Therefore, on the exposed surfaces, the failure mechanisms can be accentuated due to corrosion and ion migration. An effort must be made by the manufacturers to ensure the performance of

these devices in those conditions. An example is presented in [9]. By submitting Si and SiC power devices under high-voltage and high-temperature environments, both devices passed the qualification at 1000 h. However, this is still one exception that is not yet ensured by all the manufacturers on the market, and further investigation is necessary to improve the correspondent acceleration factor model. In order to differentiate SiC and Si semiconductors, not only the physical part is evaluated, but also the manufacturer acceleration factor $\pi_{PartMan}$ in (2). The manufacturer acceleration factor is defined in (8). Q_{Amanuf} is the description of the manufacturer quality assurance level, Q_{Acomp} is the description of the component quality assurance level and R_{Acomp} is the risk level of the component associated with the test performed. For those three factors, the highest assurance level is equal to 3, when the assurance level obtained is higher than the reference state of art or ultra passes the expectation, and 0 in the worst case, when there is no available information or when qualification test is not performed.

$$\pi_{PartMan} = e^{1.39[1 - (\frac{Q_{Amanuf} + Q_{Acomp}R_{Acomp}}{36})\epsilon] - 0.69} \quad (8)$$

ϵ is the experience factor that the component buyer may have with his supplier, and in the studying case is considered the same for all the devices.

The thermal model used to estimate the device's junction temperature in the thermal stress factor is unidirectional and modeled with the thermal resistances to represent the heat sinks for high and low voltage sides, as presented in Chapter 5. The ambient temperature is considered at 85 °C.

6.6.2- Capacitors, transformer and inductor reliability

The failure rates of capacitors, transformer and inductor are also determined according to equation (2). For the output capacitors, the RMS current is one of the most important specifications for its reliability and it also affects the converter's efficiency resulting in a different impact for each topology. The designers usually combine technologies such as Tantalum, Aluminum and Tantalum Polymer to reduce cost and attend to the requirements of current ripple and lifetime; in some cases is necessary to investigate different combinations to find the best configuration. One of the advantages of the current-fed topology is to deal with smaller capacitances. This allows replaces aluminium capacitors by a better technology, such as ceramic or tantalum, increasing the converter mean time to failure.

The part manufacturer factor and process are determined as in the case of active components. The physical part includes mechanical, thermal and thermo-electrical acceleration factors. In the induced factor, the relative sensitivity is defined for electrical, thermal and mechanical overstress as indicated in FIDES [4]. The physical failure rate is:

$$\lambda_{phy} = \lambda_{cap} \sum_i^{Phases} \frac{t_{ann}}{8760} (\pi_{TH} + \pi_{TCy} + \pi_{Mec}) \pi_{ind} \quad (9)$$

The voltage applied ($V_{applied}$) on the capacitor, the maximum voltage specified by the supplier (V_{rated}) and the board temperature, are the factors contributing to physical stresses in these components. The thermo-electrical acceleration factor is calculated in (10):

$$\pi_{THCap} = 0.94 \left(\frac{V_{applied}}{0.4 V_{rated}} \right)^3 e^{\frac{E_a}{k} \left(\frac{1}{293} - \frac{1}{T_{board_{amb}} + 273} \right)} \quad (10)$$

The power losses and the temperature increasing are calculated with the datasheet information. For example, for electrolytic capacitors it is common to estimate the temperature increasing with the following equations:

$$P_c = \Delta I_{out_{RMS}}^2 \times ESR_{equivalent}$$

$$\Delta T_c = I_{ripple} \frac{ESR}{Surface (cm^2) \times Heat_{radiation_{Factor}} \left(\frac{W}{^\circ C cm^2} \right)}$$

For ceramic and film capacitors, the capacitance variation with temperature and humidity is usually measured to establish a mathematical relationship between them. This characteristic can vary a lot from one manufacturer to another, and for this reason, it should be obtained directly with the supplier or measured experimentally. Once this information is available, the new dissipation factor can be calculated to evaluate the losses.

In the case of transformer and inductors, the same equation (9) is used. The thermo-electrical acceleration factors are very similar:

$$\pi_{THTrafo} = 0.15 e^{\frac{E_a}{k} \left(\frac{1}{293} - \frac{1}{T_{board_{amb}} + \Delta T + 273} \right)} \quad (11)$$

$$\pi_{THInduc} = 0.09 e^{\frac{E_a}{k} \left(\frac{1}{293} - \frac{1}{T_{board_{amb}} + \Delta T + 273} \right)} \quad (12)$$

To evaluate the temperature in the transformer, we use the thermal model obtained in Chapter 4. The power analysis also made in this chapter, allows an accurate estimation of power losses for the different operating points. Therefore, a lookup table containing the power losses for different operating points has previously been calculated with the method proposed in Chapter 4 and included in the lifetime analysis.

The variation of temperature in the DC and AC side inductors due to the winding power losses are evaluated with an equivalent thermal resistance estimated considering the nominal power losses and the maximum allowed temperature. The empirical result in [10] associates this thermal resistance with the volume of the magnetic core. It is also assumed that the core loss corresponds to half of the total inductor loss, which is acceptable:

$$P_{Inductor} = \left[\left(\frac{\Delta T_{max}}{\sqrt{V_{core} (cm^3)}} \right) 24 \right] \quad (13)$$

The acceleration factors associated with humidity and mechanical vibrations are determined using the coefficients and values indicated in FIDES. Sometimes a more precise analysis is recommended because the heat flow exchanged and the impact of mechanical stress in a specific component may not be performed as expected due to its physical placement on the board.

6.6.3- Integration of the reliability model

To integrate the converter characteristics, the demanded power profile is inserted in Simetrix, where the converter is simulated for the different input conditions. The power profile is coded in Octave environment to control the time-dependent simulation in Simetrix and recover the information after each simulated cycle. In Simetrix, the power switches are modeled by a switch containing the information from the manufacturer. The Spice models available on their websites could also be used, but the simulation takes more time to achieve the steady-state.

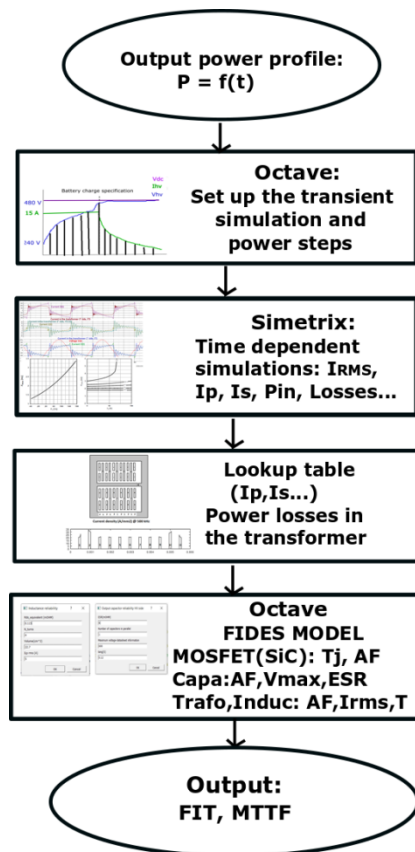


Figure 6-22: Flowchart of the method to integrate the reliability model with time transient simulations.

The simulation results, consisting of current and power losses in each power transistor, and the current in the primary and secondary transformer windings, are loaded in Octave. The thermal equivalent model of the power switches and the reliability model for all the evaluated components are used to determine the Mean Time to failure (MTTF) of the converter, as presented in Figure 6-22. The total stress is derived from the counted cycles over a year, as presented in [11], the rain flow count method.

After obtaining each component's failure rate, the total failure rate per unit of time is estimated by equation (1). The equivalent Mean Time to failure in years is obtained by considering the FIT of the converter, the number of failures in 10^9 device hours.

$$MTTF_{years} = \frac{10^9}{\lambda_{converter}} \frac{1}{8760 \text{ hours}} \quad (14)$$

The transistor's junction temperatures are presented in Figure 6-23 for an ambient temperature of 85°C .

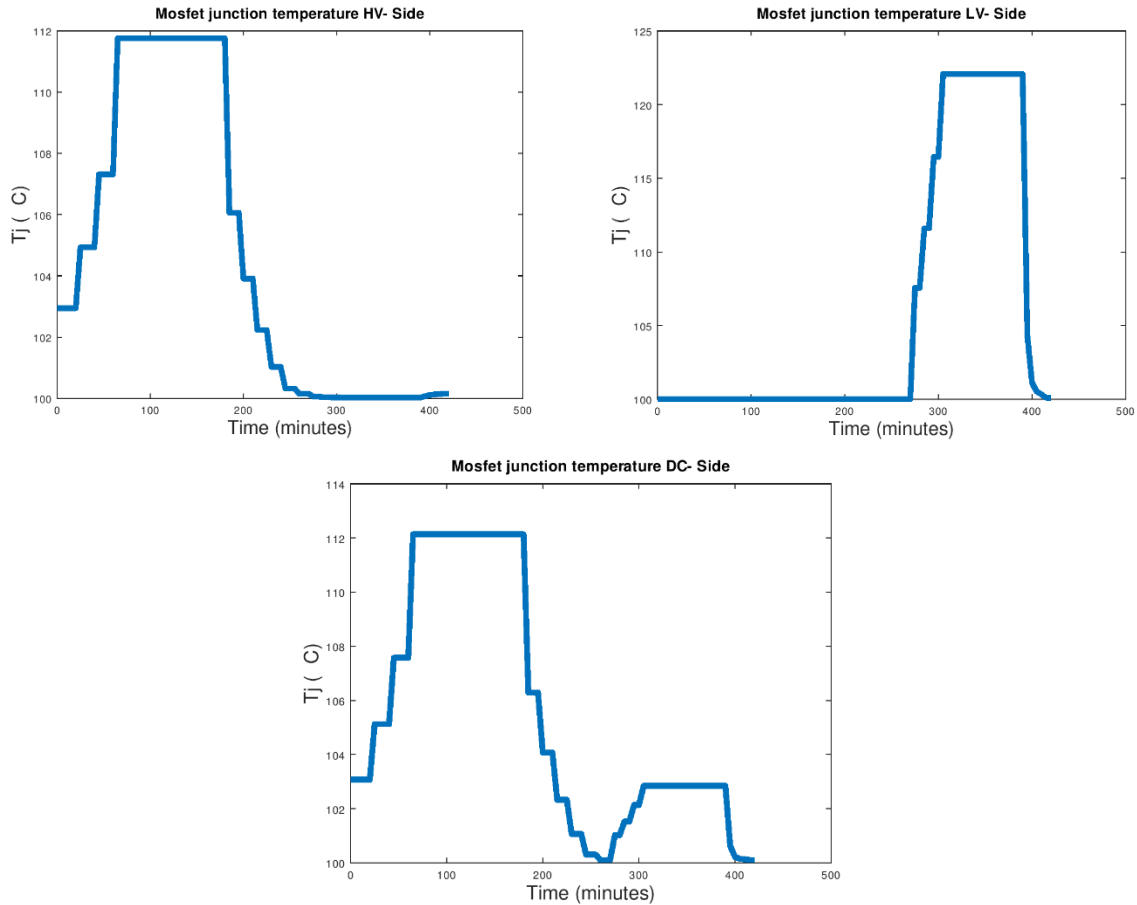


Figure 6-23: Junction temperature in the power transistors of the full-bridges connected to the HV side battery, LV side battery and Vdc link voltage.

The mean time to failure and the failure rates in time (FIT) are presented in Table 6-7. The SiC transistors are used in both high voltage sides, totalizing 8 transistors. In the low voltage side, two Si MOSFETS are connected in parallel to perform a switch. It is necessary to remark that the reliability study is only applicable in the range for which the components are qualified, and for an ambient temperature range between -55°C and 125°C .

HV semiconductors	898.56
LV semiconductors	367.58
Transformer	21.38
Resonant inductors	13.15
DC side inductors	18.52

Resonant capacitors	57.54
Output capacitors	29.90
FIT (Total)	1424.6
MTTF (years)	80.13

Table 6-7: Failure rate of the power converter.

The mean time to failure obtained is increased compared to the expected, generally between 20 and 40 years for electric vehicle applications. This is verified because the estimation does not contain the AC-DC PFC part and neither the AC input filters, resulting in a smaller number of failures. These results are only an estimation for the Three-port converter and do not include the entire charger. The approach, however, allows considering the impact on the components shared for more than one function as the transformer and the resonant elements to proceed with the product guidelines.

6.7- Conclusion

This chapter aims at the perspectives of the converter proposed for the automobile industry application. It complements the work proposed in Chapters 3, 4 and 5 to demonstrate and answer the questions about performance and size to develop the entire OBC and LDC converter by proposing some complements to work with the new topology.

7- Conclusion

The objective of this research was to develop an integrated converter with combined OBC and DC-DC functionalities required in electric vehicles. The possibility of sharing some components already present in one or both converters was one of the main targets. This feature, associated with the need for full-isolation between the sources, bidirectional power flow, independent functions, and simultaneous operation, led the research to the development of a three-port bridge converter. The focus of the thesis has therefore been on the development of the DC-DC part. In the development of a high-efficient DC-DC stage, soft switching is a requisite, and the investigation of the three-port active bridge in Chapter 2 shows how to obtain this characteristic in the entire power and voltage ranges of our application.

As an improvement from state-of-the-art solutions, we propose the three-port current-fed parallel resonant converter. This architecture was studied to integrate an on-board charger of 7 kW and a DC-DC converter of 3.5 kW to charge the auxiliary LV battery. The LC resonant cell in parallel with the transformer windings allows zero-voltage switching for low and nominal output power, while the current-fed configuration replaces filter capacitors by using inductors to smoothen the current. The structure is bidirectional in both converter functions, and it is similar to a current inverter.

The transformer, an essential part of the integrated power unit, had been studied in Chapter 4. We decide to develop a planar transformer and minimize power losses and leakage inductance to avoid interfering with the ideal converter operation. Due to a high current present on the low voltage side, and the difference between HV and LV batteries, parallel-layers are needed to support the high current on the LV side. However, high-frequency effects modify the current distribution inside parallel-connected layers, and to avoid poor current distribution, this phenomenon was investigated in detail. The analytical solution of the formulated Ampère and Faraday laws inside each conductor layer associated with the external test conditions was used in a Matlab routine to solve this problem. The program has been elaborated to study this phenomenon in a DC-DC auxiliary converter, but it was improved to solve the problem of this thesis and adapted for generalized multi-winding planar transformers. With this fast calculation method, it was possible to evaluate different arrangements to design the three-winding transformer and select the best one considering the drawbacks of the assembly process and insulation norms for electric vehicles. Compared to a 2D finite element analysis, the results provided by this fast calculation were very close. Short circuit and open circuit tests were also implemented in the routine considering frequency effects to generate an equivalent model that can be exported to simulation environments and be correlated with real measurements using an impedance analyzer.

Despite the efforts in minimizing leakage inductance, parasitic oscillations are superposed to the resonant sinusoidal voltage waveforms affecting the converter's performance. However, these oscillations can be damped, as indicated in Chapter 5. During the tests, it was also verified that the parasitic capacitance from the transformer modifies the converter's resonant frequency, decreasing its value. Nevertheless, this is an intrinsic characteristic of the interleaved arrangement used during the planar transformer design to minimize leakage inductance and AC winding power loss.

All these effects from the parasitic elements can be minimized by improving the transformer design and the prototype containing the transformer and power board parts integrated on the same board, as proposed at the end of Chapter 5.

The work developed allowed the validation of a bidirectional converter topology with ZVS full capability. This converter topology can be applied to many applications even outside the automobile domain. The integration between three power sources can be extended to four or more power sources, such as renewable energy sources and other storage elements as supercapacitors. The bidirectional power flow can be controlled using an additional non-isolated DC-DC stage, enabling the voltage or current regulation. The association of series cascaded stages also provides a solution to high voltage applications. Because of the soft-switching and current features, the proposed bidirectional converter is an alternative solution aiming at high power densities benefiting from high switching frequency capability.

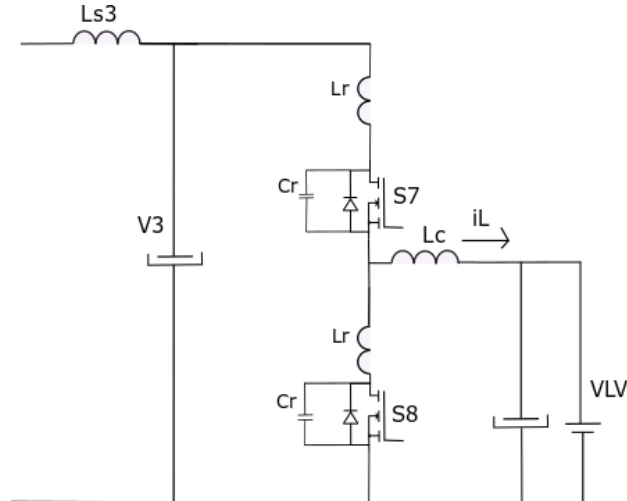
Future Work

Although the efforts we had made to develop a transformer according to the electrical standard, some improvements are still necessary. The design of the planar transformer containing three PCBs and 24 layers resulted in additional winding DC resistance, leakage inductance, and some difficulties in its assembling. Therefore, we recommend reducing its ratio of turns, as mentioned at the end of Chapter 4. This reduction can be made by splitting the transformer into two or three smaller magnetic cores and connecting the winding in series in the HV sides or parallel in the LV side. With this strategy, the performances of the transformer and the resonant converter are improved. Furthermore, with a smaller parasitic capacitance, the converter switching frequency can be increased, and we can take advantage of its full ZVS operational capability in the conception of a more compact converter.

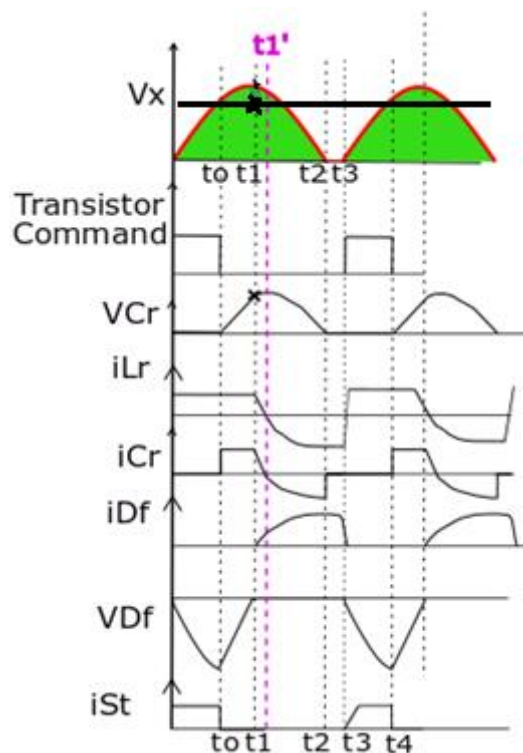
7.1- Annexes

7.1.1- Design of the Buck-boost converter for CCM mode using the quasi-resonant LC circuit

The quasi-resonant circuit is applied in the charging of the LV battery. Due to the inductor filter (L_{s3}) present at the output of the resonant converter, the current is considered as constant in this analysis. The operation intervals of the converter are described in this section.



Compared to the LCD snubber, the structure not only requires the use of fewer additional components to have ZVS commutations, but sometimes it is also possible to use the elements already present in the converter, such as the Cds capacitor of the MOSFET and parasitic inductances.



Some considerations are made in this analysis: the inductor filter L_{s3} is able to keep the output current almost constant and the duty cycle is always smaller than 0.5.

$$Z_o = \sqrt{\frac{L_r}{C_r}}, \quad \omega_o = \frac{1}{\sqrt{L_r C_r}}$$

Interval to-t1:

Before the instant to, the constant current flows in the transistor and the voltage drop on the resonant inductor and over the resonant capacitor is zero. The voltage on the diode is the equivalent input voltage V_X . The transistor is turned-off at $t=t_0$ and the current is entirely transmitted to the capacitor C_r . The capacitor voltage starts to increase while the voltage over the diode V_{Df} decreases; and the current in the resonant inductor remains constant until the capacitor voltage is equal to the input voltage V_X ($t=t_1$). At this instant, the voltage V_{Df} achieves zero.

$$i_{Lr}(t) = i_{Cr}(t) = C_r \frac{dv_{Cr}}{dt} = I_o, \quad v_{Cr} = \frac{1}{C_r} \int_0^t I_o dt + i_{Cr}(t_0) = I_o t / C_r$$

$$v_{Df} = V_X - \frac{I_o t_0}{C_r}, \quad v_{Df}(t_1) = V_X - \frac{I_o t_1}{C_r} = 0, \quad V_X(t_1) = \frac{I_o t_1}{C_r}$$

Interval t1-t2:

At the beginning of this interval, the capacitor C_r has been charged until its voltage is equal to the voltage V_X , at $t=t_1$. When this occurs, the diode D_f is forward biased and the current passes through D_f due to the stored energy in the filter. As C_r and L_r are in resonance, the current passes by zero and continues to decrease until it reaches $-I_o$.

$$v_{Df} = V_X - v_{Cr} + v_{Lr} = 0 \Rightarrow V_X - v_{Cr} + L_r \frac{di_{Lr}}{dt} = 0$$

$$\frac{dV_X}{dt} - \frac{dv_{Cr}}{dt} + L_r \frac{di_{Lr}^2}{dt^2} = 0$$

In the conventional quasi-resonant Buck converter, the first term of the above equation is zero:

$$V_X(t) = 0$$

$$-\frac{dv_{Cr}}{dt} + \frac{L_r di_{Lr}^2}{dt^2} = -\frac{i_{Cr}}{C_r} + \frac{L_r di_{Lr}^2}{dt^2} = 0, \quad -\frac{i_{Lr}}{C_r} + \frac{L_r di_{Lr}^2}{dt^2} = 0$$

The following differential equation describes the period between t_1 and t_2 :

$$\frac{i_{Lr}}{C_r} + \frac{L_r di_{Lr}^2}{dt^2} = 0$$

$$i_{Lr}(t) = I_o \cos W_o(t - t_1) - V_{peak} W_{o1} C_r \cos(W_{o1} t)$$

$$v_{Cr}(t) = \frac{I_o}{W_o C_r} \sin W_o(t - t_1) - V_{peak} \sin W_{o1} t + V_{peak} \sin(W_{o1} t_1)$$

The maximum voltage occurs at $\frac{dv_{Cr}}{dt} = 0$

$$t'_1 = \frac{\pi}{2W_o} + t_1 = \frac{T_o}{4} + \frac{V_X(t_1) C_r}{I_o}$$

The maximum voltage over the capacitor C_r at $t=t_1'$ must be higher than the input voltage V_X ($t=t_1'$).

$$\frac{I_o}{W_o C_r} + V_X(t_1) > V_{peak} \sin(W_{o1} t'_1)$$

$$\frac{I_o}{W_o C_r V_{peak}} > \sin\left(\frac{\pi T_o}{2 T_{o1}}\right) \cos W_{o1} t_1 + \cos\left(\frac{\pi T_o}{2 T_{o1}}\right) \sin W_{o1} t_1 - \sin(W_{o1} t_1)$$

If the Buck converter is switched at twice the switching frequency of the parallel resonant converter:

$$T_o = 2 \times T_{o1}.$$

$$\frac{I_o}{W_o C_r V_{peak}} > -2 \sin W_{o1} t_1$$

If the Buck is switched at the same frequency of the Current-fed parallel resonant converter: $T_o = T_{o1}$.

$$\frac{I_o}{W_o C_r V_{peak}} > \cos W_{o1} t_1 - \sin W_{o1} t_1$$

The output voltage is the average voltage over the diode Df, as shown at below:

$$0 - t_o: v_{Df}(t) = V_x(t) = V_{peak} \sin W_{o1} t$$

$$t_o - t_1: v_{Df}(t) = V_x(t) - v_{C_r}(t) = V_{peak} \sin W_{o1} t = V_{peak} \sin W_{o1} t - \frac{I_o t_1}{C_r}$$

$$t_1 - t_4: v_{Df}(t) = 0$$

$$V_{out} = \frac{V_{peak}}{\pi} [1 - \cos W_{o1} t_o - \cos W_{o1} (t_1 - t_o)] - \frac{2 I_o t_1}{C_r T_{o1}} (t_1 - t_o)$$

t_o is the ON time of the transistor

The capacitor Cr and the inductor Lr are in resonance. Considering mainly the number of additional components needed to achieve ZVS and ZCS in the switches, this solution is interesting. The additional elements in the structure are naturally present in the transistors, as the capacitor Cds and the leakage inductance of the main DC side inductance, making this solution more coherent with the purposes to reduce the number of elements. The main drawback is the frequency control.

7.1.2- Design of the Buck-boost converter for CCM mode using the LCD snubber

In the design of the circuit in Figure 6-5, we use the analysis of the conduction modes presented in Figure 6-6. Two approximations are made: the voltage drops on the transistors and diodes are disregarded, and the output inductance (Ls3) from the three-port parallel resonant converter is large enough to establish an almost constant current.

During the first phase, while both transistors are off, there are two conditions:

$$i_{L_r}(0) = 0$$

$$v_{C_{r2}}(0) = V_3$$

In the second and third phases, the low side transistor turns-on, and the current increases with the following ratio until achieves the value of I_{Ls3} :

$$\frac{di_{L_r}}{dt} = \frac{V_3}{L_r} \Rightarrow i_{L_r} = \frac{V_3}{L_r} t$$

$$i_{L_r}(t_o) = I_{Ls3} \Rightarrow t_o = L_r \frac{I_{Ls3}}{V_3}$$

This current is considered as constant and it is directly associated to the output power:

$$\eta \approx 100\% \Rightarrow I_{Ls3} = \frac{P_{out}}{V_3}$$

At the end of this phase, the diode in anti-parallel with S7 is blocked, since its current pass by zero.

At the fourth phase illustrated in Figure 6-6-d, the inductor Lr and capacitor Cr2 oscillates:

$$i_{L_r} + i_{C_{r2}} = I_{Ls3}, \quad v_{L_r} = v_{C_{r2}}$$

$$v_{C_{r2}} + L_r C_{r2} \frac{dv_{C_{r2}}^2}{dt^2} = 0$$

$$v_{C_{r2}}(t) = V_3 \cos\left(\frac{t}{\sqrt{L_r C_{r2}}}\right)$$

$$i_{C_{r2}}(t) = -V_3 \sqrt{\frac{C_{r2}}{L_r}} \sin\left(\frac{t}{\sqrt{L_r C_{r2}}}\right)$$

$$v_{C_{r2}}(0) = 0 \quad i_{L_r}(0) = I_{Ls3}$$

$$i_{L_r} = I_{Ls3} + V_3 \sqrt{\frac{C_{r2}}{L_r}} \sin\left(\frac{t}{\sqrt{L_r C_{r2}}}\right)$$

Next phase starts when the capacitor C_{r2} is completely discharged, so both diodes, D_1 and D_2 in the clamp circuit are biased:

$$i_{L_r}(t_1) = I_{Ls3} + V_3 \sqrt{\frac{C_{r2}}{L_r}}$$

$$v_{C_{r2}} = 0$$

At the end of this phase, the transistor S8 can be turned-off at zero voltage. The current path is shown in Figure 6-6-f. The resonance occurs between C_{r1} , C_{r2} and L_r .

$$I_{Ls3} = C_{r2} \frac{dv_{C_{r2}}}{dt} \Rightarrow v_{C_{r2}} = \frac{I_{Ls3}}{C_{r2}} t$$

$$v_{C_{r2}} + v_{C_{r1}} = 0$$

$$C_{r1} L_r \frac{dv_{C_{r1}}^2}{dt^2} + v_{C_{r1}} = 0$$

$$v_{C_{r1}}(0) = 0 \quad i_{L_r}(0) = I_{Ls3} + V_3 \sqrt{\frac{C_{r2}}{L_r}}$$

$$v_{C_{r1}}(t) = \left(I_{Initial} \sqrt{\frac{L_r}{C_{r1}}} + V_3 \sqrt{\frac{C_{r2}}{C_{r1}}} \right) \sin\left(\frac{t}{\sqrt{L_r C_{r1}}}\right)$$

The capacitor C_{r2} is charged while the current i_{L_r} decreases. When $i_{L_r} = 0$, and $v_{C_{r2}} = V_3$, the diode D_1 is blocked. The current i_{L_r} becomes negative since it continues to oscillate with C_{r1} , and D_2 is directly biased. The anti-parallel diode of S7 is biased and the current is gradually transferred to this diode while L_r discharges.

Using the intervals of each phase, we determine the components. Voltage and current stresses are the constraints in the clamp circuit:

$$I_{Transistor\ Max} = I_{L_r\ Max} = I_{Ls3} + V_3 \sqrt{\frac{C_{r2}}{L_r}} \quad (1)$$

$$V_{Transistor\ Peak} = I_{Ls3} \sqrt{\frac{L_r}{C_{r1}}} + V_3 \sqrt{\frac{C_{r2}}{C_{r1}}} \quad (2)$$

From the third phase:

$$L_r = \frac{V_3}{I_{Ls3}} t_o = \frac{V_3^2}{P_{out}} t_o \quad (3)$$

Equations (1), (2) and (3) allow the optimal choice of the clamp circuit components by limiting the maximum voltage and current stress in the transistors. For example, for a switching frequency of 100 kHz and a maximum voltage peak allowing the use of nominal 80-Vds MOSFETS, the following table shows the voltage and current range for different loads. The use of the duty cycle to attempt the required output voltage only results in increased voltage and current spikes during the battery charging process.

Pout (kW)	0.25	0.5	1.5	2.5	3.5
Vds peak (V)	22.76	34	55	79	96
Ids peak (A)	84	122	254	362	443

Voltage and current peak on the transistors depending on the output load. Fsw = 100 kHz, to = 0.1 T, Lr = 115 nH, Cr1 = 2.4µF, and Cr2 = 0.8 nF.

Following the design specification in Table 6-1, at 180 kHz, the maximum energy required on the DC inductor is:

$$L = 500 \text{ nH} \quad I_{L_{\max}} = 310 \text{ A} \quad I_{L_{\text{RMS}}} = 291 \text{ A}$$

$$F_{\text{sw}} = 180 \text{ kHz}$$

$$\text{Energy} = \frac{1}{2} L (I_{L_{\max}})^2 = 24 \text{ mJ}$$

$$B_{\text{sat}} = 1.2 \text{ uT} = 26 \text{ @Magnetics Kool Mu}$$

$$A_e L_e \approx \frac{2 \text{ Energy } \mu\text{uT}}{B_{\text{sat}}^2} = \frac{2 \times 24 \text{ mJ } 4\pi 10^{-7} 26}{1.2^2} = 1088 \text{ mm}^3$$

Part Selection Number from Magnetics: 00K553028E026

Core selection: Kool Mu E format core u = 26 Bsat = 1.2

$$A_w = 380 \text{ mm}^2 \quad A_e = 417 \text{ mm}^2 \quad L_e = 123 \text{ mm}$$

$$N = \sqrt{\frac{L (\text{nH})}{A_L \left(\frac{\text{nH}}{\text{T}^2}\right)}} = 2$$

$$B_{\text{max}} = \frac{L I_{L_{\max}}}{N A_e} = \left(\frac{1 \text{ uH } \times 310 \text{ A}}{3 \times 417 \text{ mm}^2}\right) = 0.25$$

$$L_{\text{initial}} = N^2 A_L = 1.1 \text{ uH}$$

$$L_{\text{bias}} = 75 \% L_{\text{initial}} = 0.70 \text{ nH}$$

The lowest wire section is calculated to reduce skin effect:

$$\delta = \sqrt{\frac{7.5 \times 10^4}{F_{\text{sw}}}} = 154 \text{ } \mu\text{m}$$

$$S_{\text{skin}} = \pi (0.15^2) = 0.075 \text{ mm}^2$$

$$J_{\text{max}} = \frac{7.5 \text{ A}}{\text{mm}^2} \quad \text{Sec} = \frac{I_{L_{\text{RMS}}}}{J_{\text{max}}} = \frac{280 \text{ Arms}}{7.5 \text{ A/mm}^2} = 37 \text{ mm}^2$$

$$R_{\text{dc}} = \rho_{\text{LitzWire}} \times N \times L_{\text{Tour}} = 0.43 \text{ m}\Omega$$

$\rho_{LitzWire}$: Litz Wire resistivity

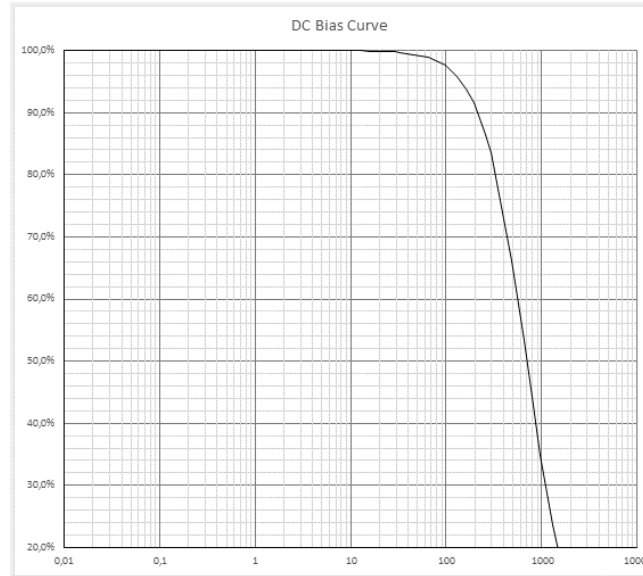
$$\varepsilon = \frac{\text{Copper thick}}{\delta} = \frac{1}{\delta} \sqrt{\frac{\text{Section}}{\pi}}$$

$$R_{ac} = \frac{\frac{R_{dc}\varepsilon}{2}[\sinh\varepsilon + \sin\varepsilon]}{(\cosh\varepsilon + \cos\varepsilon)} = 0.51 R_{dc}$$

$$P_{core} = 1800 (B_{max})^{2.02} (F_{sw})^{1.11} \left(\frac{mW}{cm^3}\right)$$

$$P_{cond} = (R_{ac} + R_{dc})I_{LRMS}^2 = 34.03 W$$

$$P_{core} = 2.09 W$$



DC bias curve of the inductor used in the DC-DC non-isolated converter for LV side.

The output filter capacitor is composed of eleven parallel capacitors: three aluminum electrolytic capacitors of 220 μF , 100V (Reference UBY2A221MHL, from Nichicon, 2.52 Arms at 125°C), and eight multi-layer ceramic capacitors of 100 nF, 650 V (Reference CKC21C104JWGACTV, 15,8 Arms at 150°C), all AEC-Q200 compliant components. The use of capacitors with higher voltage range is necessary to increase the current ripple and to prolong the useful lifetime by operating the capacitors below its rated voltage.

Parameters	Values
Inductance	1 μH
Inductor DC resistance	0.43 $\text{m}\Omega$
Max. Copper power loss	3.84 W
Max. Core power loss	34.03 W
Inductor Volume	51.400 cm^3
Output capacitance	0.66 mF / 132 Arms
Capacitor arrangement	(8x100nF/650VDC)+ (3x220uF/100VDC)
Capacitor bank volume	11 cm^3
Equivalent ESR	0.96 $\text{m}\Omega$
Power loss	16 W

7.1.3- Design of the Buck-boost bidirectional converter for DCM mode

The maximum energy required for the converter operation estimates the magnetic core volume:

$$\begin{aligned}
 L &= 9 \text{ uH} & I_{L_{\max}} &= 42 \text{ A} & I_{L_{\text{RMS}}} &= 24 \text{ A} \\
 F_{\text{sw}} &= 180 \text{ kHz} \\
 \text{Energy} &= \frac{1}{2} L (I_{L_{\max}})^2 = 20 \text{ mJ} \\
 B_{\text{sat}} &= 1.2 \text{ uT} = 19 @ \text{Magnetics Kool flux} \\
 A_e L_e &\approx \frac{2 \text{ Energy } \mu\text{T}}{B_{\text{sat}}^2} = \frac{2 \times 20 \text{ mJ } 4\pi \cdot 10^{-7} \cdot 19}{1.2^2} = 6 \text{ 628 mm}^3
 \end{aligned}$$

Part Selection Number from Magnetics: 79262

Core selection: Kool Mu Max- powder core $\mu = 19$ $B_{\text{sat}} = 1.2$

$$A_w = 455 \text{ mm}^2 \quad A_e = 210 \text{ mm}^2 \quad L_e = 60 \text{ mm}$$

$$N = \sqrt{\frac{L (\mu\text{H}) \times 10^3}{A_L \left(\frac{\mu\text{H}}{\text{T}^2}\right)}} = 21$$

$$B_{\max} = \frac{L I_{L_{\max}}}{N A_e} = \left(\frac{11 \mu\text{H} \times 42 \text{ A}}{21 \times 210 \text{ mm}^2} \right) = 0.59$$

$$L_{\text{initial}} = N^2 A_L = 11 \text{ uH}$$

$$L_{\text{bias}} = 90 \% L_{\text{initial}} = 10 \text{ uH}$$

The lowest wire section is calculated to reduce skin effect:

$$\delta = \sqrt{\frac{7.5 \times 10^4}{F_{\text{sw}}}} = 154 \text{ } \mu\text{m}$$

$$S_{\text{skin}} = \pi (0.15^2) = 0.075 \text{ mm}^2$$

$$J_{\max} = \frac{5 \text{ A}}{\text{mm}^2} \quad \text{Sec} = \frac{I_{L_{\text{RMS}}}}{J_{\max}} = \frac{24 \text{ Arms}}{5 \text{ A/mm}^2} = 4.8 \text{ mm}^2$$

$$R_{dc} = \rho_{\text{LitzWire}} \times N \times L_{\text{Tour}} = 4.06 \text{ m}\Omega$$

ρ_{LitzWire} : Litz Wire resistivity

$$\varepsilon = \frac{\text{Copper thick}}{\delta} = \frac{1}{\delta} \sqrt{\frac{\text{Section}}{\pi}}$$

$$R_{ac} = \frac{R_{dc} \varepsilon [\sinh \varepsilon + \sin \varepsilon]}{(\cosh \varepsilon + \cos \varepsilon)} = 0.61 R_{dc}$$

$$P_{\text{core}} = 566 (B_{\max})^{2.018} (F_{\text{sw}})^{1.17} \left(\frac{\text{mW}}{\text{cm}^3} \right)$$

$$P_{\text{cond}} = (R_{ac} + R_{dc}) I_{L_{\text{RMS}}}^2 = 3.84 \text{ W}$$

$$P_{core} = 9.51 \text{ W}$$

The output filter capacitor is composed of two parallel electrolytic capacitors of 22 uH, 550V. The AEC-Q200 compliant component is the UCY2H220MHD3TN from Nichicon.

Parameters	Values
Inductance	9 uH
Inductor DC resistance	4.07 mΩ
Max. Copper power loss	3.84 W
Max. Core power loss	9.51 W
Inductor Volume	10.600 cm ³
Output capacitance	10 uF
Capacitor arrangement	2x 22uF /550 VDC
Capacitor bank volume	6.13 cm ³
Equivalent ESR	5.2 mΩ
Power loss	2.29 W

7.1.4- Design of a Bridgeless totem-pole PFC (CCM and CrCM)

In the CCM, we can consider at first, the input voltage a time-dependent perturbation and the output voltage as a constant resulting in a variable current ripple. By integrating the voltage in the inductor over an entire cycle, the minimum inductance is determined.

$$T = \frac{L I_{Lmax}}{v_{ac}} + \frac{L I_{Lmax}}{V_{dc} - V_{ac}} = \frac{L I_{Lmax} [(V_{dc} - V_{ac}) + V_{ac}]}{V_{ac} (V_{dc} - V_{ac})} = L I_{Lmax} \frac{V_{dc}}{V_{ac}(V_{dc} - V_{ac})}$$

$$\Delta I_{max} = \frac{V_{acmin} (V_{dcmax} - V_{acmin})}{F_{sw} V_{dcmax} L_{min}}$$

The minimum required inductance at 100 kHz calculated for 20% of current ripple is:

$$L_{min} = \frac{V_{ACmin} (V_{DCmax} - V_{ACmin})}{F_{sw} \Delta I_{max} V_{DCmax}} = \frac{85\sqrt{472.5 - 85\sqrt{2}}}{100 \text{ kHz} (20\% 32\sqrt{2}) 472.5 \text{ V}} = 37 \text{ uH}$$

The maximum inductor current ripple occurs when the input voltage is minimum, 85 Vac and for the maximum output voltage, 472.5V. Using an inductor of 100uH ensures the converter operation in the continuous mode.

$$\Delta I_{max} = \frac{85\sqrt{2} (472.5 - 85\sqrt{2})}{100\text{kHz} 472.5 100 \text{ uH}} = 8.94 \text{ A}$$

The maximum inductor current:

$$I_{Lmax} = 32\sqrt{2} + 8.94 = 62.9 \text{ A}$$

The minimum duty cycle will be defined for the minimum output voltage:

$$D_{\min} = 1 - \left(\frac{V_{\text{acmax}} \sqrt{2}}{V_{\text{DC}}} \right) = 1 - \left(\frac{265 \sqrt{2}}{472.5} \right) = 0.79$$

$$D_{\max} = 1 - \left(\frac{V_{\text{acmin}} \sqrt{2}}{V_{\text{DC}}} \right) = 1 - \left(\frac{85 \sqrt{2}}{472.5} \right) = 0.25$$

The boost inductor values for Dmax and Dmin are calculated when T2 is turned-on:

$$L_{\min} = \frac{V_{\text{acmin}}}{\Delta I_{\max}} (T D_{\min}) = \frac{85 \sqrt{2} (0.25)}{\Delta I_{\max} 100 \text{ kHz}} = 33.6 \text{ uH} \quad @ D_{\min} \text{ and } V_{\text{in min}}$$

$$L_{\max} = \frac{V_{\text{acmax}}}{\Delta I_{\max}} (T D_{\max}) = \frac{265 \sqrt{2} (0.79)}{\Delta I_{\max} 100 \text{ kHz}} = 331 \text{ uH} \quad @ D_{\max} \text{ and } V_{\text{in max}}$$

The inductor should be designed with an intermediary value between 34 uH and 332 uH. We are going to use 100 uH as the nominal inductance for the design of the Bridgeless Totem pole controlled at 100 kHz.

The Magnetic core estimation

The maximum energy required for the converter operation estimates the magnetic core volume:

$$L = 100 \text{ uH} \quad I_{L_{\max}} = 54 + \frac{85 \sqrt{2} (472.5 - 85 \sqrt{2})}{100 \text{ kHz } 472.5 \text{ } 100 \text{ uH}} = 62.9 \text{ A} \quad I_{L_{\text{RMS}}} = 32 \text{ A}$$

$$F_{\text{sw}} = 100 \text{ kHz}$$

$$\text{Energy} = \frac{1}{2} L (I_{L_{\max}})^2 = \frac{1}{2} 100 \text{ uH} \times (62.9)^2 = 198 \text{ mJ}$$

$$B_{\text{sat}} = 1.2 \text{ uT} = 90 @ \text{Magnetics Kflux}$$

$$A_e L_e \approx \frac{2 \text{ Energy } \mu\text{T}}{B_{\text{sat}}^2} = \frac{2 \times 198 \text{ mJ } 4\pi \times 10^{-7} \times 90}{1.2^2} = 29 \text{ 830 mm}^3$$

Using the selection part number provided by one of the Manufacturers in the market, Magnetics we have:

$$L I^2 = 0.100 \text{ mH } (62.9^2) = 395 \text{ mH.A}^2$$

Part Selection: 78777 - Core selection: X Flux- powder core $\mu=40$ $B_{\text{sat}} = 1.2$, $J=5 \text{ A/mm}^2$

$$A_L = 205 \text{ nH/T}^2$$

$$A_w = 1 \text{ 150 mm}^2 \quad A_e = 478 \text{ mm}^2 \quad L_e = 170 \text{ mm}$$

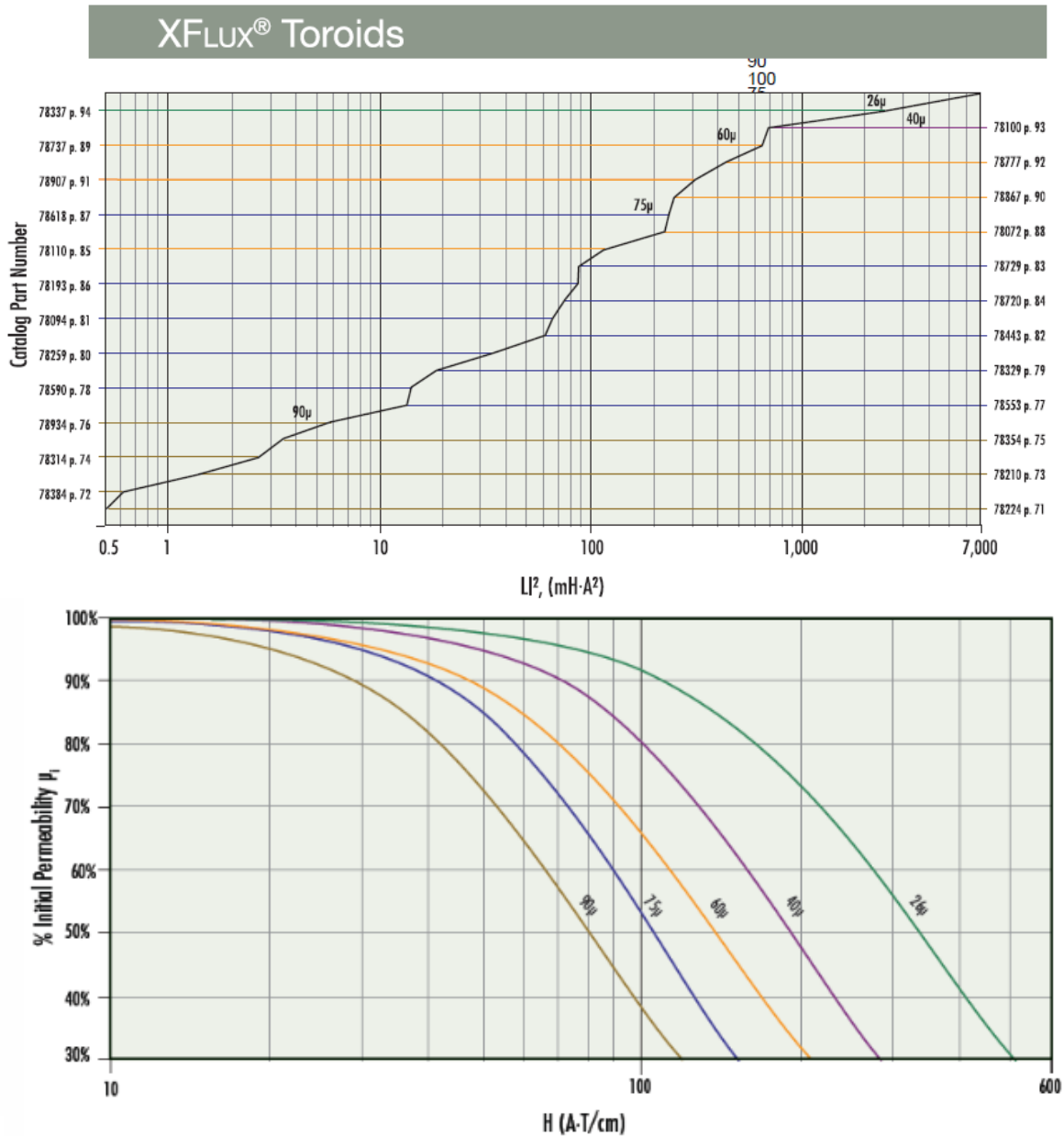
$$N = \sqrt{\frac{L (\text{uH}) \times 10^3}{A_L \left(\frac{\text{nH}}{\text{T}^2} \right)}} = 22$$

$$B_{\max} = \frac{L I_{L_{\max}}}{N A_e} = \left(\frac{100 \text{ uH} \times 62.9 \text{ A}}{22 \times 478 \text{ mm}^2} \right) = 0.59$$

$$L_{\text{initial}} = N^2 A_L = 22^2 \times 0.205 \text{ uH} = 99.2 \text{ uH}$$

$$H_{FL} = \frac{NI_{L_{max}}}{L_e} = \frac{22 \times 62.9}{0.170 \text{ m}} = \frac{8140 \text{ At}}{\text{m}} \text{ Verify in the curve for 60u material}$$

$$H_{FL} = 8140 \frac{\text{At}}{\text{m}} \times 0.01254 = 102 \text{ Oersted} = 81.4 \text{ At/cm}$$



At 142 At/cm the magnetic core has about 48 % of its initial permeability, so:

$$L_{bias} = 48\% L_{initial} = 48\% 160 \text{ uH} = 76.8 \text{ uH}$$

To obtain 160 uH for 48% of permeability, the initial non-bias inductor must be 320 uH.

$$N = \sqrt{\frac{320 \text{ (uH)} \times 10^3}{0.205 \left(\frac{\text{uH}}{\text{T}^2}\right)}} = 39$$

$$B_{max} = \frac{LI_{L_{max}}}{N A_e} = \left(\frac{320 \text{ uH} \times 54.3 \text{ A}}{39 \times 478 \text{ mm}^2} \right) = 0.93$$

$$L_{\text{initial}} = N^2 A_L = 39^2 \times 0.205 \text{ uH} = 311 \text{ uH}$$

$$H_{\text{FL}} = \frac{N I_{\text{Lmax}}}{L_e} = \frac{39 \times 54.3}{0.170 \text{ m}} = \frac{19792 \text{ At}}{\text{m}} \text{ Verify in the curve for 60u material}$$

$$H_{\text{FL}} = 19792 \frac{\text{At}}{\text{m}} \times 0.01254 = 248 \text{ Oersted} = 198 \text{ At/cm}$$

The permeability becomes 30% for the 60u material. In this situation, the 40u material remains with about 50% of its initial permeability, a better choice.

Inductor power loss estimation

The lowest wire section is calculated to reduce skin effect:

$$\delta = \sqrt{\frac{7.5 \times 10^4}{F_{\text{sw}}}} = 193 \text{ um} = 0.19 \text{ mm}$$

$$S_{\text{skin}} = \pi (0.19^2) = 0.117 \text{ mm}^2$$

$$J_{\text{max}} = \frac{5 \text{ A}}{\text{mm}^2} \text{ Sec} = \frac{I_{\text{LRMS}}}{J_{\text{max}}} = \frac{32 \text{ Arms}}{5 \text{ A/mm}^2} = 6.4 \text{ mm}^2$$

$$\text{AWG 26} \Rightarrow S = 0.16 \text{ mm}^2 \text{ Litz wire section}$$

$$N_{\text{parallel}} = \frac{6.4}{0.16} = 40 \text{ Litz wire in parallel}$$

$$R_{\text{dc}} = \rho_{\text{LitzWire}} \times N \times L_{\text{Tour}} = \rho_{\text{LitzWire}} \times N \sqrt{\pi A_e} = 0.15 \Omega$$

ρ_{LitzWire} : Litz Wire resistivity

$$\varepsilon = \frac{\text{Copper thick}}{\delta} = \frac{1}{\delta} \sqrt{\frac{\text{Section}}{\pi}} = 0.94$$

$$R_{\text{ac}} = \frac{R_{\text{dc}} \varepsilon [\sinh \varepsilon + \sin \varepsilon]}{(\cosh \varepsilon + \cos \varepsilon)} = 0.429 R_{\text{dc}}$$

$$P_{\text{core}} = 566 (B_{\text{max}})^{2.018} (F_{\text{sw}})^{1.17} \left(\frac{\text{mW}}{\text{cm}^3} \right)$$

$$P_{\text{cond}} = (R_{\text{ac}} + R_{\text{dc}}) I_{\text{LRMS}}^2 = 219 \text{ W}$$

$$P_{\text{core}} = 196 \text{ W}$$

DC bus capacitor selection

One of the design requirements is the voltage ripple, in this case required to be smaller than 5%.

$$C_{\text{dc1}} = \frac{P_{\text{max}}}{2 (2\pi 50 \text{ Hz}) V_{\text{dcmin}} (\Delta V_{\text{dc}})}$$

$$C_{\text{dc1}} = \frac{7 \text{ kW}}{2 (2\pi 50 \text{ Hz}) 480 (5\% \times 480)} = 967 \mu\text{F}$$

The second requirement is that the DC link capacitor must handle it the power during the entire period of the grid:

$$C_{dc2} = \frac{P_{\max}(20\text{ms})}{(V_{dc\max}^2 - V_{dc\min}^2)} = \frac{7 \text{ kW} \times 0 \text{ ms}}{(550^2 - 390^2)} = 930 \mu\text{F}$$

970 μF is the value that satisfies both conditions. The rms current in the DC link capacitor is calculated by subtracting the average output current from the rectified current when the input voltage is minimum, 200 Vac and the maximum input current, 32 A, $P_{in} = 2.72 \text{ kW}$ (at 85 Vac the power is limited at 2.72 kW):

$$I_{AC_{\text{rect}}}^2 = I_{\text{out}}^2 + I_{C_{\text{RMS}}}^2$$

$$I_{C_{\text{RMS}}} = \sqrt{I_{AC_{\text{rms}}}^2 - \frac{P_o^2}{V_o^2}} = \sqrt{32^2 - \frac{6400^2}{480^2}} = 29.09 \text{ A RMS}$$

A capacitor bank is proposed to attempt the requirements by associating 5 arrays in parallel of 2 capacitors connected in series to attempt the required capacitance, according to the next table:

Reference	Value	Manufacturer
ESMR401VSN391MR30S	390 μF / 400 Vdc	Chemi-con
Single array	2 capacitors in series (800Vdc) / 195 μF	
Arms (single capacitor)	2.32 Arms	85°C, 120 Hz
Combined arrays	12 arrays in parallel-28 Arms/2.3 mF	
ESR	0.050 Ω	

◆ STANDARD RATINGS

WV (V _{dc})	Cap (μF)	Case size $\phi D \times L$ (mm)	$\tan \delta$	Rated ripple current (Arms/ 85°C, 120Hz)	Part No.
400	150	22 × 25	0.15	1.30	ESMR401VSN151MP25S
	180	22 × 30	0.15	1.49	ESMR401VSN181MP30S
	220	22 × 35	0.15	1.69	ESMR401VSN221MP35S
	220	25.4 × 25	0.15	1.65	ESMR401VSN221MQ25S
	270	22 × 40	0.15	1.90	ESMR401VSN271MP40S
	270	25.4 × 30	0.15	1.88	ESMR401VSN271MQ30S
	330	22 × 45	0.15	2.15	ESMR401VSN331MP45S
	330	25.4 × 35	0.15	2.16	ESMR401VSN331MQ35S
	330	30 × 25	0.15	2.10	ESMR401VSN331MR25S
	390	22 × 50	0.15	2.40	ESMR401VSN391MP50S
	390	25.4 × 40	0.15	2.40	ESMR401VSN391MQ40S
	390	30 × 30	0.15	2.32	ESMR401VSN391MR30S
	390	35 × 25	0.15	2.05	ESMR401VSN391MA25S
	470	25.4 × 45	0.15	2.69	ESMR401VSN471MQ45S
	470	30 × 35	0.15	2.60	ESMR401VSN471MR35S
	470	35 × 30	0.15	2.28	ESMR401VSN471MA30S
	560	30 × 40	0.15	2.92	ESMR401VSN561MR40S
	560	35 × 30	0.15	2.48	ESMR401VSN561MA30S
	680	30 × 45	0.15	3.30	ESMR401VSN681MR45S
	680	35 × 35	0.15	2.79	ESMR401VSN681MA35S
820	35 × 45	0.15	3.25	ESMR401VSN821MA45S	
1 000	35 × 50	0.15	3.66	ESMR401VSN102MA50S	

Chemi-Con capacitor part selection, Ref: EMSR401VSN391MR30S.

When the charger is connected to the electrical grid, but there's no power transfer between them, the capacitor bank is charged with a leakage current that passes through the body diodes of the bridgeless totem-pole. To prevent possible damage in the SiC mosfets, sometimes it's necessary to add a parallel diode bridge with higher current capability in series with a series resistance to limit the current. This current depends on the grid connection standard. Assuming that an instantaneous power of 1 kW is admissible, the series resistance is:

$$R_{precharge} = \frac{(265 \text{ Vac } \sqrt{2})^2}{1 \text{ kW}} = 140 \Omega \quad I_{leakage} = \frac{265 \sqrt{2}}{140} = 2.67 \text{ A}$$

Power semiconductors

The maximum voltage under the semiconductors:

$$V_{\max} = V_{dc} - (-V_{ac_{\max}}) = 480 + 265\sqrt{2} = 854 \text{ V}$$

The maximum current is the same current that passes through the inductor:

$$I_{SW_{\max}} = 32 \sqrt{2} + 9 \text{ A} = 54.3 \text{ A}$$

Transistors Low Freq.

$$I_T = \frac{1}{2\pi} \int_0^\pi I_{in_{\max}} \sin(\omega t) d\omega t$$

$$I_T = \frac{I_{in}\sqrt{2}}{\pi} = 14.4 \text{ A}$$

$$I_{T_{RMS}} = \sqrt{\frac{1}{2\pi} \int_0^\pi I_{in_{\max}}^2 [\sin(\omega t)]^2 d\omega t}$$

$$I_{T_{RMS}} = \frac{I_{in_{\max}}}{2} = 22.62 \text{ A}$$

Transistors High Freq.

$$I_T = \frac{1}{2\pi} \int_0^\pi I_{in_{\max}} \sin(\omega t) d\omega t$$

$$I_T = \frac{I_{in}\sqrt{2}}{\pi} = 14.4 \text{ A}$$

$$I_{T_{RMS}} = \sqrt{\frac{1}{2\pi} \int_0^\pi I_{in_{\max}}^2 [\sin(\omega t)]^2 d\omega t}$$

$$I_{T_{RMS}} = \frac{I_{in_{\max}}}{2} = 22.62 \text{ A}$$

Conduction + switching power losses

The power losses in the transistor have the contribution of the switching frequency and the conduction power losses in the on-resistance (R_{ds}).

$$P_{\text{Total}} = P_{\text{cond}} + P_{\text{SW}} + P_{\text{Err}}$$

$$P_{\text{cond}} = [R_{DS_{\text{on}}} = f(I_{DS})] I_{T_{RMS}}^2 + V_{SD} I_F$$

The switching power losses can be estimated using datasheet information:

$$P_{\text{ON}} = E_{\text{ON}_{\text{test}}} \left(\frac{V_{\text{real}}}{V_{\text{test}}} \right) \left(\frac{I_{\text{DS}_{\text{real}}}}{I_{\text{DS}_{\text{test}}}} \right) F_{\text{sw}}$$

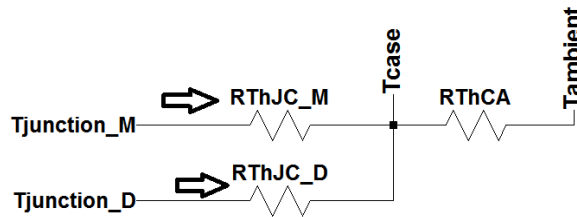
$$P_{OFF} = E_{OFF_{test}} \left(\frac{V_{real}}{V_{test}} \right) \left(\frac{I_{DS_{real}}}{I_{DS_{test}}} \right) F_{sw}, \dots$$

The $R_{DS_{ON}}$ provided in datasheet is selected according to the drain-to-source current and the maximum junction temperature of the SiC is selected.

$$R_{DS_{on}} = f(I_{DS}, T_{j_{max}})$$

$$P_{cond} = R_{DS_{on}} I_{DS}^2$$

After the power losses estimation, the junction temperature is verified considering a simplified equivalent thermal model of the SiC mosfet:



The maximum case temperature is considered at 60°C .

$$T_{j_{max}} (^{\circ}\text{C}) = T_{case} + P_{Total} R_{thjC}$$

In the bridgeless totem pole PFC we evaluate a SiC MOSFET of 1200V, 30 m Ω , 72 A to estimate the power losses (SCT3030KL).

The Bridgeless Totem pole converter design in the CrCM

In the CrCM, the current ripple depends on the voltage reference but is constant for a given output voltage. The turn-on time is always constant to increase the current until its reference value, and then the switch is turned off to decrease the current until zero. The turn-off time is variable and depends on the inductor voltage, which means that the switching frequency is variable. The average current is half of the maximum current ripple.

$$I_{L_{max}} = 2 I_{in_{Average}} = 2 \times \frac{2 \times 32 \sqrt{2}}{\pi} = 57.65 \text{ A}$$

The maximum current ripple is:

$$\Delta I_{L_{max}} = \frac{I_{L_{max}}}{2} = 28.82 \text{ A (current ripple)}$$

$$I_{L_{max}} = \Delta I_{L_{max}} + (I_{ac_{max}}) = 28.82 \text{ A} + (32 \sqrt{2}) = 74 \text{ A}$$

In the boost mode, during the OFF time:

$$V_{ac} - V_o = L \frac{I_{L_{max}}}{(T_{off})}$$

In the boost mode, during the ON time:

$$T_{on} = \frac{L I_{L_{max}}}{V_{ac}}$$

The switching frequency can be calculated:

$$F_{sw} = \frac{V_{ac} (V_{dc} - V_{ac})}{L I_{Lmax} V_{dc}}$$

The minimum inductance is calculated for the maximum desirable switching frequency, in this case, 100 kHz. The maximum switching frequency occurs at the minimum input voltage (85 Vac) because the current decreases faster: The required inductance is then determined at the minimum input voltage:

$$L_{min} = \frac{85\sqrt{2}(480 - 85\sqrt{2})}{100 \text{ kHz } 480 (74 \text{ A})} = 15 \text{ uH}$$

The minimum switching frequency will occur at the maximum input voltage:

$$T_{onmin} = \frac{L I_{Lmax}}{V_{acmin}} = \frac{40 \text{ u } 74 \text{ A}}{265 \sqrt{2}} = 7.89 \text{ us}$$

$$T_{offmin} = \frac{L I_{Lmax}}{V_{acmin} - V_o} = \frac{40 \text{ u } 74 \text{ A}}{(265\sqrt{2} - 427.5)} = 56 \text{ us}$$

$$T_{min} = 7.89 + 56 \text{ (us)} \quad F_{swmax} = \frac{1}{64.02 \text{ u}} = 15.6 \text{ kHz}$$

The Magnetic core estimation

$$I_{Lrect} = \frac{I_{Lmax}}{2}; \quad I_{Lrect} = \frac{2 V_{ac}}{\pi L} T_{on}; \quad T_{on} = \frac{L I_{Lmax}}{V_{ac}}$$

$$\frac{V_o - V_{ac}}{L} = \frac{I_{Lmax}}{T_{off}}; \quad T_{off} = \frac{L I_{Lmax}}{V_o - V_{ac}} \quad V_o = V_{ac} \frac{T}{(T - k_v L)}$$

$$L = 40 \text{ u } I_{Lmax} = 74 \text{ A} \quad I_{LRMS} = 32 \text{ A}$$

$$F_{sw} = 100 \text{ kHz} \quad \text{For the condition of 265 Vac}$$

$$L_{max} = V_{acmax} \frac{(V_{dc} - V_{acmax})}{F_{swmin} V_{dc} I_{Lmax}} = 265\sqrt{2} \frac{(450 - 265\sqrt{2})}{15 \text{ kHz } 450 \text{ V } 74 \text{ A}} = 56.5 \text{ uH}$$

$$L_{min} = V_{acmax} \frac{(V_{dc} - V_{acmax})}{F_{swmax} V_{dc} I_{Lmax}} = 265\sqrt{2} \frac{(450 - 265\sqrt{2})}{100 \text{ kHz } 450 \text{ V } 90.4 \text{ A}} = 6.93 \text{ uH}$$

$$L = 30 \text{ u } I_{Lmax} = 74 \text{ A} \quad I_{LRMS} = 32 \text{ A}$$

$$F_{sw} = 100 \text{ kHz} \quad \text{For the condition of 85 Vac}$$

$$L_{max} = V_{acmax} \frac{(V_{dc} - V_{acmax})}{F_{swmin} V_{dc} I_{Lmax}} = 85\sqrt{2} \frac{(450 - 85\sqrt{2})}{15 \text{ kHz } 450 \text{ V } 90.4 \text{ A}} = 64 \text{ uH}$$

$$L_{min} = V_{acmax} \frac{(V_{dc} - V_{acmax})}{F_{swmax} V_{dc} I_{Lmax}} = 85\sqrt{2} \frac{(450 - 85\sqrt{2})}{100 \text{ kHz } 450 \text{ V } 74 \text{ A}} = 11.9 \text{ uH}$$

$$\text{Energy} = \frac{1}{2} L (I_{Lmax})^2 = \frac{1}{2} 30 \text{ uH } x (82.8^2) = 102 \text{ mJ}$$

$$B_{sat} = 1.2 \text{ uT} = 60 \text{ @Magnetics Kflux}$$

$$A_e L_e \approx \frac{2 \text{ Energy } \mu_r}{B_{sat}^2} = \frac{2 \times 102 \text{ mJ } 4\pi \times 10^{-7} \times 90}{1.2^2} = 16 \text{ 022 mm}^3$$

Using the selection part number of Magnetics:

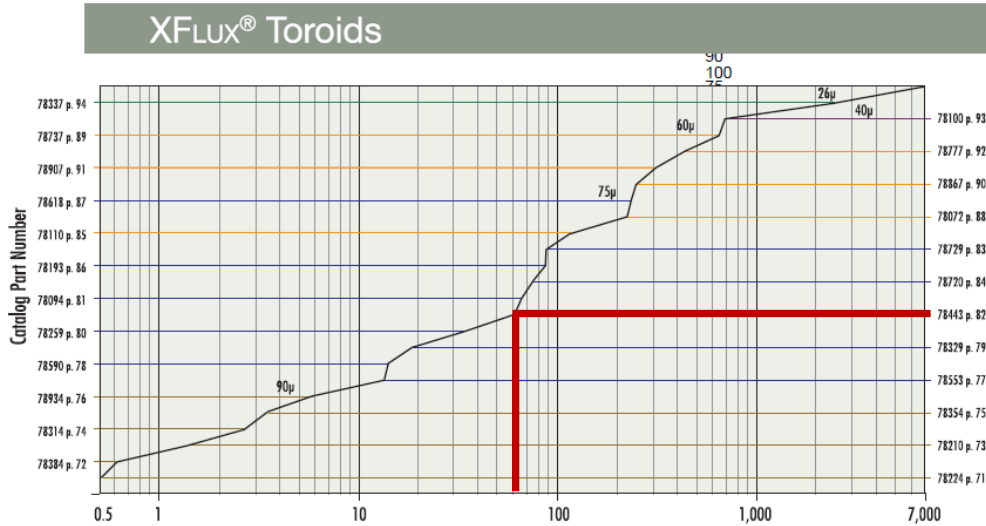
$$L I^2 = 0.011 \text{ mH } (74^2) = 60 \text{ mH} \cdot \text{A}^2$$

Part Selection: 78443 - Core selection: X Flux- powder core $\mu=75$ $B_{sat} = 1.2$

$J=5A/mm^2, A_L = 169 nH/T^2$

$A_w = 427 mm^2 \quad A_e = 199 mm^2 \quad L_e = 107 mm$

$$N = \sqrt{\frac{L(uH) \times 10^3}{A_L \left(\frac{nH}{T^2}\right)}} = 9$$



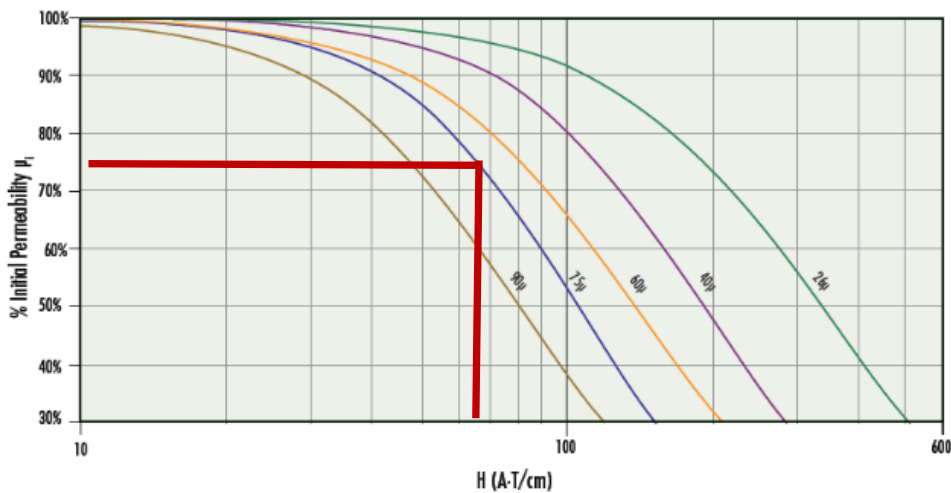
$$B_{max} = \frac{L I_{Lmax}}{N A_e} = \frac{(11 \mu H \times 74 A)}{(9 \times 199 mm^2)} = 0.42$$

$$L_{initial} = N^2 A_L = 8^2 \times 0.169 \mu H = 10.6 \mu H$$

$$H_{FL} = \frac{N I_{Lmax}}{L_e} = \frac{8 \times 74}{0.107 m} = \frac{5532 At}{m}$$

Verify in the curve for 60u material

$$H_{FL} = 5532 \frac{At}{m} \times 0.01254 = 69.4 Oersted = 55.32 At/cm$$



At 55 At/cm the magnetic core has about 75 % of its initial permeability, so:

$$L_{bias} = 75\% L_{initial} = 75\% 10.6 \mu H = 7.95 \mu H$$

To obtain 11 μH for 75% of permeability, the initial non-bias inductor must be 15 μH .

$$N = \sqrt{\frac{15 (\mu H) \times 10^3}{0.169 \left(\frac{\mu H}{T^2}\right)}} = 9.4$$

$$B_{max} = \frac{L I_{Lmax}}{N A_e} = \left(\frac{15 \mu H \times 74 A}{9 \times 199 \text{ mm}^2} \right) = 0.62$$

$$L_{initial} = N^2 A_L = 9^2 \times 0.169 \mu H = 13.69 \mu H$$

$$H_{FL} = \frac{N I_{Lmax}}{L_e} = \frac{9 \times 74}{0.107 \text{ m}} = \frac{6224 \text{ At}}{\text{m}} \text{ Verify in the curve for 75u material}$$

$$H_{FL} = 6224 \frac{\text{At}}{\text{m}} \times 0.01254 = 78 \text{ Oersted} = \mathbf{62.24 \text{ At/cm}}$$

The permeability becomes 74% for the 75u material. In this situation, the 75u material remains with about 75% of its initial permeability, a better choice.

Inductor power loss estimation

The lowest wire section is calculated to minimize the skin effect:

$$\delta = \sqrt{\frac{7.5 \times 10^4}{F_{sw}}} = 193 \mu\text{m} = 0.19 \text{ mm}$$

$$S_{skin} = \pi (0.19^2) = 0.117 \text{ mm}^2$$

$$J_{max} = \frac{5 \text{ A}}{\text{mm}^2} \text{ Sec} = \frac{I_{L_{RMS}}}{J_{max}} = \frac{32 \text{ Arms}}{5 \text{ A/mm}^2} = 6.4 \text{ mm}^2$$

$$\text{AWG 26} \Rightarrow S = 0.16 \text{ mm}^2 \text{ Litz wire section}$$

$$N_{parallel} = \frac{6.4}{0.16} = 40 \text{ Litz wire in parallel}$$

$$R_{dc} = \rho_{LitzWire} \times N \times L_{Tour} = \rho_{LitzWire} \times N \sqrt{\pi A_e} = 0.094 \Omega$$

$\rho_{LitzWire}$: Litz Wire resistivity

$$\epsilon = \frac{\text{Copper thick}}{\delta} = \frac{1}{\delta} \sqrt{\frac{\text{Section}}{\pi}} = 0.94$$

$$R_{ac} = \frac{R_{dc} \epsilon [\sinh \epsilon + \sin \epsilon]}{2 (\cosh \epsilon + \cos \epsilon)} = 0.429 R_{dc}$$

$$P_{core} = 566 (B_{max})^{2.018} (F_{sw})^{1.17} \left(\frac{\text{mW}}{\text{cm}^3} \right)$$

$$P_{cond} = (R_{ac} + R_{dc}) I_{L_{RMS}}^2 = 410 \text{ W}$$

$$P_{core} = 196 \text{ W}$$

The capacitor selection follows the same steps used in the CCM stage.

7.2- References

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