



HAL
open science

Temperature-aware ratio metric analog-to-digital readout interface for MEMS resonant sensors

Ali Mostafa

► **To cite this version:**

Ali Mostafa. Temperature-aware ratio metric analog-to-digital readout interface for MEMS resonant sensors. Micro and nanotechnologies/Microelectronics. Université Paris-Saclay, 2021. English. NNT : 2021UPAST024 . tel-03255097

HAL Id: tel-03255097

<https://theses.hal.science/tel-03255097>

Submitted on 9 Jun 2021

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Temperature-aware ratio metric analog-to-digital readout interface for MEMS resonant sensors

Thèse de doctorat de l'Université Paris-Saclay

École doctorale n° 575 EOBE Electrical, optical, bio-physics
and engineering

Spécialité de doctorat: Électronique et optoélectronique, nano-
et microtechnologies

Unité de recherche: Université Paris-Saclay, CentraleSupélec, CNRS,
Laboratoire de Génie Electrique et Electronique de Paris, 91192,
Gif-sur-Yvette, France.

Référent: : CentraleSupélec

**Thèse présentée et soutenue à Gif-sur-Yvette, le 26 mars
2021, par**

Ali MOSTAFA

Composition du jury:

Arnaud Bournel Professeur, Université Paris-Saclay	Président
Dimitri Galayko Maître de Conférences, HDR, Sorbonne Université	Rapporteur et examinateur
Franck Badets Ingénieur de Recherche, HDR, CEA LETI	Rapporteur et examinateur
Michael Kraft Professeur, KUL	Examinateur
Núria Barniol Professeur, UAB	Examinatrice
Jérôme Juillard Professeur, Centralesupelec	Directeur de thèse
Pietro Maris Ferreira Maître de Conférences, HDR, Centralesupelec	Co-encadrant de thèse

Titre: Interface de lecture ratiométrique analogique-numérique conscient en température pour les capteurs MEMS résonants

Mots clés: MEMS, résonateurs couplés, Résolution élevée, Temperature, $\Sigma\Delta$ ADC.

Résumé: La technologie MEMS a permis le développement de capteurs avec bonnes performances en termes de résolution, de sensibilité, de consommation, etc... Comme dans tout capteur, la sensibilité à la grandeur mesurée doit être maximisée, et la sensibilité aux fluctuations, telles que le dérive et le bruit, doivent être minimisées pour améliorer la résolution. L'effet de température peut-être compensé en utilisant des capteurs différentiels basés sur des résonateurs MEMS faiblement couplés. Dans tels dispositifs, les informations détectées différenciellement sont modulées à travers les signaux de sorties de deux résonateurs, et mesurées soit par la différence de phase, soit par le rapport d'amplitude entre ces signaux. Alors que le pre-

mier est généralement préféré en raison de sa nature quasi numérique, le dernier offre une résolution plus élevée, mais aussi une bonne immunité contre les fluctuations indésirables, améliorant donc le rapport signal sur bruit. Ces caractéristiques de la mesure du rapport d'amplitude motivent nos recherches pour un moyen efficace de déterminer et de convertir cette quantité du domaine analogique vers le domaine numérique. L'interface de lecture proposée est basée sur un convertisseur analogique-numérique sigma-delta ($\Sigma\Delta$ ADC), et est destinée aux applications automobiles, avec une plage de température de -40 à 125 °C. Les circuits ont été conçus sous la technologie SOI-180nm de la série XH018 des Fonderies X-FAB.

Title: Temperature-aware ratio metric analog-to-digital readout interface for MEMS resonant sensors

Keywords: MEMS, Coupled resonators, High resolution, Temperature, $\Sigma\Delta$ ADC.

Abstract: MEMS technology has allowed the development of sensors with good performance in terms of resolution, sensitivity, consumption, etc... As in every sensor, the sensitivity to the measured quantity must be maximized, and the sensitivity to every other fluctuations, such as drifts and noises, must be minimized or compensated for enhanced resolution. Recently, differential architectures based on weakly coupled MEMS resonators have been emerged as a good candidate for high thermal stability measurement. In such devices, the differentially sensed information is modulated through the resonators output signals, and measured by either extracting the phase difference

or the amplitude ratio of these signals. While the former is generally preferred because of its quasi-digital nature, the latter offers higher resolution, and higher immunity from undesired fluctuations, improving the signal to noise ratio. These features of the amplitude ratio measurement have motivated our research for an efficient way of computing and converting this quantity from the analog into the digital domain. The proposed readout interface is based on sigma-delta analog-to-digital converter ($\Sigma\Delta$ ADC), and targeted for automotive applications with a temperature range from -40 to 125 °C. The circuits are implemented using SOI-CMOS 180nm technology of XH018 series from X-FAB Silicon Foundries.

Acknowledgment

Without the help, support, and encouragement of a large number of people it would not be possible for me to write this thesis. I would like to thank the following people and organizations:

- My supervisor Prof. Jérôme Juillard, and my co-supervisor Dr. Pietro Maris Ferreira, for their guidance, trust and support. Thanks for giving me the opportunity to pursue a career as Ph.D. student.

- I want to thank Prof. Philippe Benabes, Mr. Francis Trelin and Mme. Emilie Avegnon for their assistance in chip layout designing, and for solving all computer related issues.

- I would also like to thank my dissertation committee members, Dr. Dimitri Galayko, Eng. Franck Badets, Prof. Nuria Barniol, and Prof. Michael Kraft, for their time and valuable feedback.

- Mr. J.R.R.O Martins deserve a great deal of thanks for being great colleague, and sharing his time and ideas within the past years of the Ph.D. Thanks for proofreading a chapter of this thesis and contributing with several suggestions and improvements.

- Thanks to all friends and family who have encouraged me during the years, but who I could not fit in here.

- My sweet family for always encouraging and supporting me in whatever I do.

- Last, but not least, my wonderful wife, Aya, for her love, encouragement, support, and patience.

Contents

Acknowledgment	3
Contents	i
List of Figures	vii
List of Tables	xv
Notations	xviii
Résumé long en français	1
Introduction	13
Background and motivation	13
Research Contribution	14
Organization of the thesis	17
1 MEMS resonant sensors and electronic interface	19
1.1 MEMS resonator model	19
1.2 Resonant MEMS architectures and sensing mode	22
1.2.1 Resonant sensors based on a single resonator sensors	22
1.2.1.1 Open Loop sensing mode	23

1.2.1.2	Closed Loop sensing mode	25
1.2.2	Duffing nonlinearity effect on single resonator sensors	26
1.2.3	Open loop vs. closed loop	28
1.2.4	Discussion	28
1.2.5	Resonant sensors based on weakly-coupled resonators	29
1.2.5.1	Resonant sensors based on mutually-injection-locked oscillators	31
1.2.5.2	Resonant sensors based on mode-localization oscillators	32
1.2.6	Duffing nonlinearity effect on sensors based on weakly coupled resonators	34
1.3	Global comparison	35
1.3.1	Optimum output metric in the linear oscillation regime	35
1.3.2	Optimum output metric in the nonlinear oscillation regime	37
1.3.3	Conclusion	37
1.4	Bilinear amplitude-amplitude output metric	37
1.5	Literature on the analog to digital ratiometric interface	39
1.5.1	Readout interface requirements	39
1.5.2	One step approach	39
1.5.3	Two steps approach	40
1.5.4	ADC as voltage divider	40
1.5.5	Demodulator	42
1.6	Conclusion	42
2	Ratiometric analog to digital interface based on sigma delta modulator	45
2.1	Introduction	45
2.2	Operating principle and resolution of a sigma delta converter	46
2.2.1	Operating principle	46

2.2.2	Metrics and definitions	47
2.2.3	Resolution	48
2.3	Modulator architecture selection	49
2.3.1	Domain: discrete time vs continuous	50
2.3.1.1	Coefficient sizing and trimming with frequency	51
2.3.1.2	Thermal Noise	53
2.3.1.3	Jitter	54
2.3.1.4	Switch non-idealities	54
2.3.1.5	Power consumption	55
2.3.1.6	Conclusion	55
2.3.2	Single-bit vs. multi-bit quantizer	55
2.3.3	Loop filter order	56
2.3.4	Loop topology	57
2.3.5	Conclusion	60
2.4	Modulator coefficients	60
2.4.1	Feedback-coefficient b1	61
2.4.2	Integrator-coefficients a1 and a2	62
2.4.3	Simulation results and conclusion	64
2.5	System level consideration and electrical modeling of the analog blocks	67
2.5.1	Noise	67
2.5.2	Integrator non-idealities and optimum OTA specifications	68
2.5.2.1	OTA finite DC gain	68
2.5.2.2	Limited slew-rate and gain-bandwidth of the OTA	70
2.5.2.3	Saturation	75
2.5.3	Specifications of the analog blocks	76

2.5.4	Model implementation	76
2.5.5	Simulation results	77
2.6	Conclusion	78
3	Circuit level design of the sigma delta modulator	81
3.1	Switch	82
3.2	Operational transconductance amplifier 'OTA'	84
3.2.1	OTA design comparison	84
3.2.2	g_m/I_d design considerations	87
3.2.3	Folded cascode OTA design	93
3.3	Bias circuit	95
3.4	Common mode feedback control circuit	96
3.5	Integrator	97
3.5.1	Parasitic insensitive integrator	97
3.5.2	1-bit DAC input integrator	98
3.6	Compartor	100
3.7	Feed forward coefficients	102
3.8	Non overlapping clock	102
3.9	Conclusion	103
4	Post layout simulation results	105
4.1	Introduction	105
4.2	Switch	106
4.3	Operational transconductance amplifier 'OTA'	107
4.3.1	Nominal simulation	108
4.3.2	PVT simulation	110

4.4	Capacitor bank	114
4.5	Comparator and Non overlapping clock	115
4.6	Modulator	117
4.6.1	PVT simulation	118
4.7	Conclusion	120
	Conclusion and perspectives	123
	Appendices	129
A	Parametric analysis of nonlinear duffing resonator	131
B	Noise shaping	135
C	Integrator transfer function	139
D	VerilogA	141
D.1	OTA	141
D.2	Comparator	144
D.3	Save data	146
E	Temperature aware MILO sustaining electronics	149
E.1	Introduction	149
E.2	Current to voltage temperature aware amplifier	151
E.2.1	Design consideration	151
E.2.2	Proposed transimpedance amplifier and its operating principle . . .	151
E.2.3	PVT simulation results	153
E.2.3.1	ac analysis	153

E.2.3.2	Input impedance	154
E.2.3.3	Linearity	155
E.2.4	Discussion	156
E.3	Voltage to voltage temperature aware amplifier	157
E.3.1	Operating principle	157
E.3.2	Optimization methodology	160
E.3.2.1	Input differential-pair biasing condition	161
E.3.2.2	Chanel length effect	162
E.3.2.3	Comparison of the proposed amplifier with the ordinary active load amplifier	164
E.3.3	Discussion	164
E.3.4	Complementary implementation of the proposed temperature aware amplifier	165
E.4	A 105 dB Ω temperature aware two stages transimpedance amplifier	167
E.5	Temperature aware two stage miller compensated DOTA	169
E.6	Sample and hold peak detector	171
E.7	Conclusion	173

Bibliography	175
---------------------	------------

List of Figures

1.1.1	MEMS (a) general model, (b) mechanical part model	20
1.1.2	Theoretical bode diagram of a linear MEMS resonator	22
1.2.1	General architecture of an open loop sensing mode	23
1.2.2	General architecture of a closed loop sensing mode based Self-Oscillating-Loop (SOL)	26
1.2.3	Typical nonlinear frequency responses of a Duffing resonator for different actuation forces F (shown in the color bar), considering $Q = 10^3$ and $\gamma = 10^{-2}$	27
1.2.4	Block diagram of two MEMS resonators coupled through their actuation force for a differential sensing of a stiffness mismatch ϵ	30
1.2.5	System-level view of a MILO based on a digital mixer	31
1.2.6	System-level view of a mode-localized oscillators	33
1.4.1	Comparison of, (a) $R(\epsilon)$, and (b) $B(\epsilon)$, for two simulated MILO architectures with $\theta = \pi/4$ and $\theta = \pi/2$, (c) measured MILO architecture with $\theta = \pi/4$	38
1.5.1	A simplified diagram of the possible implementation of the ratio metric analog to digital interface.	41
1.5.2	Resolution versus conversion rate of different types of ADCs	41
1.5.3	System-level view of the MILO, including the demodulator and the ratio-metric analog to digital interface.	43
2.2.1	Block diagram of a $\Sigma\Delta$ -ADC	46
2.2.2	A typical SNR versus normalized input power ($\hat{V}_{in} = V_{in}/V_{ref}$) of a $\Sigma\Delta$ M	47

2.2.3	$SQNR$ versus input power for $L = 2$, $d = 1$ and $OSR = 256$	49
2.3.1	Possible implementation of a modulator architecture	50
2.3.2	General architecture of L^{th} order discrete time $\Sigma\Delta$ modulator DT- $\Sigma\Delta$ M, (a) block diagram, (b) electrical implementation of the integrator, (c) clocking scheme of the integrator.	51
2.3.3	General architecture of L^{th} order continuous time $\Sigma\Delta$ modulator CT- $\Sigma\Delta$ M, (a) block diagram, implementation of the integrator as (b) OTA-RC or (c) Gm-C components.	51
2.3.4	The simulation of a resistor with SC circuits	53
2.3.5	$SQNR$ against linear input level for a first to fifth order modulator, considering 1-bit quantizer and OSR of 256	57
2.3.6	General architecture of L^{th} order full feedforward DT- $\Sigma\Delta$ M (FF-DT- $\Sigma\Delta$ M)	57
2.3.7	Practical implementation of a “FB- 2^{nd} -1-bit-DT- $\Sigma\Delta$ M”, (a) ordinary, (b) modified	58
2.3.8	Practical implementation of a “FF- 2^{nd} -1-bit-DT- $\Sigma\Delta$ M”, (a) ordinary, (b) modified	58
2.3.9	STFs of the architectures of Fig. 2.3.8 with an arbitrary set of coefficients that satisfy (2.3.10)	60
2.4.1	Representation of the outputs signals of the sensor	61
2.4.2	Behavioral simulation to determine the coefficients a_1 and a_2 of the modulator shown in Fig. 2.3.8 for $b_1 = 0.5$, $c_0 = 0$, $c_1 = c_2 = 1$ considering an $OSR = 256$ and an input amplitude of 0.57	64
2.4.3	Simulated transfer functions (a), and output spectrum (b), of the optimized modulator ($a_1 = 0.8$, $a_2 = 0.5$, $b_1 = 0.5$, $c_0 = 0$, and $c_1 = c_2 = 1$), considering an input sinewave of 0.1 kHz and amplitude of 0.57. The oversampling-ratio is always 256	65
2.4.4	Transient simulation of the system MILO + RM- $\Sigma\Delta$ M, for two identical ($Q = 500$, $f_s = 1$ MHz). The input ϵ is applied differentially to both resonators, and stepped every $3 \cdot 10^4$ samples (normalized to $T_s = 1 \mu s$). The modulator’s output bit-stream is then averaged through the decimation filter by OSR times to 117 samples (blue line), and compared with the ideal division (red line)	65

2.4.5	$SQNR$ versus input power of the optimized modulator ($a_1 = 0.8$, $a_2 = 0.5$, $b_1 = 0.5$, $c_0 = 0$, and $c_1 = c_2 = 1$), for $OSR = 256$. The asterisks represent the values obtained from simulations and the solid line is a linear approximation of the data	66
2.5.1	Effect of the OTA finite DC-gain on the modulator transfer functions given by (2.5.6): (a) NTF^{ρ} , and (b) STF^{ρ}	69
2.5.2	Effect of the OTA finite DC gain A_0 on the resolution of RM- $\Sigma\Delta$ M; (a) loss in LSB versus A for different OSR using (2.5.8), (b) simulated versus predicted $SQNR$ for $OSR = 256$. The gain A was assumed equal in both integrators	70
2.5.3	Parasitic insensitive integrator (a), and its output response (b) during the integration phase	71
2.5.4	Comparison of integrator response between the transistor-level circuit (using typical folded-cascode OTA) and the proposed model, considering $GBW \approx 13$ MHz, $SR \approx 11$ MV/s, $\alpha \approx 0.15$, $a = 0.8$, $e = 0.3$ and $V_{I-in} = V_x^{max} = 0.72$ V	73
2.5.5	Possible solution of $f(\alpha) = 1$ for the first integrator ($V_x^{max} = 0.72$ V and $a = 0.8$), considering different LSB error and $e = 0.3$	75
2.5.6	PSD of the output signal obtained from Cadence® simulation: (a) ideal, (b) ideal with finite DC-gain $A = 60$ dB, (c) non-ideal model, and (d) noisy non-ideal model at $T = 125$ °C	78
2.6.1	Ratiometric fully differential second order feedforward modulator	80
3.1.1	(a) NMOS, PMOS, and CMOS-TG on-resistance R_{on} comparison, considering an input voltage going from 0.2 to 1.6 V, (b) output voltage of the TG with and without dummy transistors considering 1V input signal. The simulations are carried out for: $V_{DD} = 1.8V$, $L = 0.18\mu m$, $W_n = 2\mu m$ and $W_p = 6\mu m$ (the width of dummy transistors are half of the switch transistors)	83
3.1.2	Transmission gate switch, (a) ordinary, (b) with dummy transistors	84
3.2.1	OTA architectures, (a) Load-Compensated (LC), (b) Miller-Compensated (MC), (c) Current-Mirror (CM), (d) Folde-Cascode (FC), and (e) Telescopic-Cascode (TC)	85
3.2.2	β_{I_d} and β_{WL} as a function of g_m/I_d . $n_{th} \approx 1.45$ and $\phi_t \approx 26$ mV	88
3.2.3	Normalized current and transconductance sensitivity $S_{I_d}^T$ and $S_{g_m}^T$ as a function of g_m/I_d	89

3.2.4	Simulated PMOS paramteres versus gate voltage V_G under the three temperatures $-40, 27,$ and $125\text{ }^\circ\text{C}$, (a) g_m , (b) I_d , and (c) g_m/I_d biasing condition at room temperature. The size of the transistor is $W \times L = 10 \times 3\text{ }\mu\text{m}^2$, and simulated considering $V_{DS} = V_{DD}/2$	90
3.2.5	α_L versus L for the working technology	91
3.2.6	(a) curves of $S_{g_{ds}}^T$ given by (3.2.9) as a function of $g_m/I_d _{T_0}$ for $V_{DS} = 0.9\text{ V}$, and the simulated relative induced g_{ds} variation $(g_{ds}^{T=125} - g_{ds}^{T=-40})/g_{ds}^{T=-40}$ against $g_m/I_d _{T_0}$ for, (b) $V_{DS} = 0.9\text{ V}$, (c) $V_{DS} = 1.35\text{ V}$, and (d) $V_{DS} = 0.2\text{ V}$. The curves are plotted in \log_{10} scale for more visibility, considering a PMOS device with short channel length ($L = 0.18\text{ }\mu\text{m}$ black line), and long channel length ($L = 3\text{ }\mu\text{m}$ blue line) while $W = 10\text{ }\mu\text{m}$. The corresponding σ_L parameter (for $L = 0.18\text{ }\mu\text{m}$ and $L = 3\text{ }\mu\text{m}$) is $\approx 3 \cdot 10^{-3}$ and $\approx 0.1 \cdot 10^{-3}$ respectively	92
3.2.7	Enhanced folded cascode OTA	93
3.2.8	Integrator output using FC structure for, without M_{11a} and M_{11b} (black full line), with M_{11a} and M_{11b} (blue dashed line)	94
3.3.1	Bias circuit	95
3.4.1	Switched capacitor common mod feedback control CMFB	96
3.4.2	Output common mode voltage V_{oc} of the first (black full line) and the second (blue dashed line) OTA respectively using the CMFB shown in Fig. 3.4.1, with the capacitance values listed in Table 3.4	96
3.5.1	Parasitic-Insensitive integrator	97
3.5.2	Clocking diagram	98
3.5.3	1-bit DAC integrator, (a) fully differential, and (b) single to differential	99
3.5.4	Integrator output for a differential input voltage of $2 \cdot V_x^{max} = 1.44\text{ V}$ and $a = 0.8$, fully differential structure (black full line), and single to differential structure (blue dashed line)	100
3.6.1	Double-tail comparator	101
3.6.2	Feedforward circuit	102
3.8.1	Non-overlapping clock tree	103
4.2.1	Layout of the TG switch including dummy transistors having an area of $18 \times 20\text{ }\mu\text{m}^2$	106

4.2.2	PVT analysis for 6-points temperature from -40 to 125 °C, 51-points Monte Carlo simulation for $\pm 3\sigma$ process mismatch variation at $V_{DD} = 1.8 \pm 10\%$: Typical performance is illustrated in black full line for the mean value ($\bar{\mu}$) and $V_{DD} = 1.8$ V, extreme-case conditions are in blue dashed line ($\bar{\mu} + 3\sigma, V_{DD} = 1.62$ V), and in red dotted line ($\bar{\mu} - 3\sigma, V_{DD} = 1.98$ V)	107
4.3.1	(a) layout of the OTA1 having an area of $220 \times 80 \mu m^2$, and (b) layout of the biasing circuit, it has an area of $35 \times 20 \mu m^2$. Transistors labeled M_D in the layouts are dummy devices. The layout of the OTA2 is not shown, it is only a scaled version of OTA2 and has an area of $135 \times 80 \mu m^2$	108
4.3.2	Nominal frequency response (Gain and Phase) of the OTA1 black full line, and OTA2 blue dashed line	109
4.3.3	Step response of the OTAs using unity feedback configuration	109
4.3.4	PVT frequency analysis of the amplifiers	110
4.3.5	PVT transient analysis of the amplifiers	111
4.3.6	Linearity of the OTA1 considering nominal, best and worst case conditions	113
4.3.7	Histogram of the integrator output, considering a modulator input of $2 \cdot V_x^{max}$, (a) first integrator, and (b) second integrator	113
4.4.1	Half part capacitor-bank of the modulator having an area of $380 \times 110 \mu m^2$. The capacitors are implemented using single Metal Insulator Metal (MIM) device having a 106.8 fF for $10 \times 10 \mu m^2$ area. All no-outlined capacitors are dummy devices	114
4.4.2	Histograms of the sampling, the integrating and the feedforward capacitors, and the corresponding coefficients a_1 , a_2 , and c_1/c_2 considering 501-points Monte Carlo simulation for $T = 27$ °C and $V_{DD} = 1.8$ V	115
4.5.1	(a) Layout of the double-tail comparator having an area of $60 \times 15 \mu m^2$, and (b) layout of the non-overlapping clock using 'nel' and 'pel' transistors, it has an area of $26 \times 55 \mu m^2$	116
4.5.2	Non-overlapping clock phases at room temperature and $V_{DD} = 1.8$ V	117
4.6.1	Layout of the modulator having an area of $530 \times 450 \mu m^2$	117
4.6.2	Ratiometric behavior of the modulator, (a) typical, (b) worst power, and (c) worst speed, considering transient simulation with DC inputs signals and 1MHz sampling frequency. The input signals V_x and V_y have an amplitude of $V_{ref} + \delta V_x$ and $V_{ref} - \delta V_y$ ($V_{ref} = 0.46$ V and $\delta V_y = \delta V_x$), δV_x is changed from 0 to 0.3 V and stepped by 0.01 V every 256 us ($OSR \cdot T_s$)	118

4.6.3	PSD of the bitstream obtained from transient simulation (Hann-windowed NFFT of 7630 points), for $T = 125$ °C, $V_{DD} = 1.8$ V, 1MHz sampling, and considering a near DC input signal having an amplitude of $0.57 \cdot 2V_{ref}$	119
4.7.1	The final, (a) tape out, (b) layout, and (c) schematic of the circuit	126
4.7.2	Die photograph of the chip	127
B.1	Linearized model of the modulator depicted in Fig. 2.2.1. All voltages are normalized to V_{ref}	135
B.2	Output response of a first order $\Sigma\Delta$ M: (a) output bit stream for an input frequency of 2 kHz, (b) power spectrum for an input frequency of 1 Hz. The input normalized signal amplitude is fixed to 0.8. The sampling frequency is fixed to 1 MHz	136
B.3	Noise shaping of low-pass (LP) loop filter.	137
C.1	Single ended parasitic insensitive integrator during the integrating phase	139
C.2	System level view of the integrator shown in Fig. C.1	140
E.1	System-level view of MILO sustaining electronics and readout interface	149
E.1	Transistor level of the proposed TIA	152
E.2	Nominal frequency response (Gain and Phase) of the TIA for I_1 going from 10 to 35 μA . $C_{p-MEMS} = 10$ pF and $C_{TIA-load} = 0.1$ pF	153
E.3	PVT simulation results of the TIA, (a) gain, and (b) phase, considering 8-points temperature going from -40 to 125 °C, and 3 points supply voltage $V_{DD} = 1.8 \pm 10\%$ $I_1 = 80$ μA . $C_{p-MEMS} = 10$ pF and $C_{TIA-load} = 0.1$ pF	154
E.4	(a) Nominal frequency response of the TIA Z_{in} for different values of R_0 , and (b) noise floor of the input referred current for $R_0 = 50$ k Ω . The simulation is carried out for $I_1 = 80$ μA , $C_{p-MEMS} = 10$ pF and $C_{p-load} = 0.1$ pF	155
E.5	TIA nominal output voltage at 1 MHz frequency, (a) time domain for $i_x(t)$ (differential) of 10 μA , and (b) peak value V_x for I_x (differential) going from 50 nA to 20 μA , considering nominal (black dashed line), best case conditions (blue dotted line) and worst case conditions (red full line). $R_0 = 50$ k Ω , $I_1 = 80\mu A$, $C_{p-MEMS} = 10$ pF and $C_{TIA-load} = 0.1$ pF	156

E.1	Common source amplifier with diode-connected-load (DOTA), (a) ordinary, (b) modified DOTA with ideal current source, (c) DOTA fully differential implementation of (b) with MOS current sources	158
E.2	Normalized temperature-dependent factor $\alpha_G^{(N,P)}$ obtained from simulation for: NMOS (full-line) and PMOS (dotted-line)	159
E.3	Relative temperature-induced gain variation ξ_G against the input common mode voltage for different device dimension factor η . Circuit of Fig. E.1(c) with $I_1 = 25\mu A$ and $L = 2\mu m$	161
E.4	Relative temperature-induced gain variation ξ_G against transistor's channel length L , for different device dimension factor η . Circuit of Fig. E.1(c) with $I_1 = 25\mu A$ and $V_{cm} = 1.2V$	162
E.5	Simulated and approximated gain at room temperature $27^\circ C$ (left), simulated relative error $\chi_{L\eta}$ and temperature-induced gain variation ξ_G (right) in %. $V_{cm} = 1.2V$, $I_1 = 25\mu A$ and $L = 4L_{min}$	163
E.6	Schematic of, (b) ordinary single ended with active load amplifier (AOTA), (b) complementary implementation of the DOTA shown in Fig.E.1(c)	163
E.7	Normalized gain ($G(T)/G(T_0)$) of the DOTA (blue full line right) and the AOTA (black dashed line left), considering nominal simulation with typical process model and $V_{DD} = 1.8 V$	164
E.8	Nominal frequency response (Gain and Phase) of the complementary DOTA considering $I_1 = 25 \mu A$, $\eta = 0.04$, $V_{cm} = 0.9V$, $L = 4L_{min}$ and $C_{DOTA-load} = 0.1 pF$	166
E.9	DOTA output voltage $v_{out}(t)$, (a) time domain for $v_{in}(t)$ (differential) of $0.15V$ at $1 MHz$, and (b) peak values V_{out} for $v_{in}(t)$ (differential) going from $100 mV$ to $600 mV$ at $1 MHz$, considering $T = 27^\circ C$ in black line, $T = 125^\circ C$ in red line and $T = -40^\circ C$ in blue line. $V_{DD} = 1.8V$, $I_1 = 25 \mu A$ and $C_{DOTA-load} = 0.1 pF$	167
E.1	Frequency response of the enhanced gain TIA (EGTIA), (a) loop gain, and (c) loop phase at three the temperatures -40 , 27 , and $125^\circ C$. $C_{p-MEMS} = 10 pF$ $C_{EGTIA-load} = 0.1 pF$. The values at $1 MHz$ are given, in (b) for the gain, and in (d) for the phase	168
E.2	EGTIA output voltage $v_x(t)$ for $i_x(t)$ (differential) of $1\mu A$ at $1 MHz$ and $T = 125^\circ C$	169
E.1	Proposed two stages DOTA	169

E.2	Nominal frequency response (Gain and Phase) of the cascaded two stages complementary DOTA before compensation	170
E.3	Frequency response of of the cascaded two stages complementary DOTA after compensation, (a) loop gain, (b) DC-gain, (c) loop phase, and (d) phase margin, considering $C_c = 1$ pF, $R_c = 2$ k Ω and $C_L = 1$ pF.	171
E.1	Proposed peak demodulator circuit, (a) sample and hold, and (b) clock generation	172
E.2	Sample and hold non-overlapped phases of Φ_{SH} and $\overline{\Phi_{SH}}$ obtained from the circuit shown in Fig. E.1(b) (without filtering) for $C_{Delay} = 30$ fF.	172
E.3	Input/Output of the sample and hold peak-detector circuit shown in Fig. E.1 using C_{SH} of 5, 10 and 20 pF, for $C_{Delay} = 30$ fF	173

List of Tables

1.1	The parametric sensitivities and FOMs obtained close to $\epsilon = 0$, for all architectures in the linear and nonlinear oscillation regimes.	36
1.2	Readout interface requirements	39
2.1	CT versus DT modulators	56
2.2	OTAs' requirements	76
2.3	Parameter values used in the simulation	77
3.1	Switch transistor dimensions	84
3.2	Transistor dimensions, of (a) OTA1, and (b) OTA2	94
3.3	Transistor dimensions of the bias circuit	95
3.4	CMFB capacitance values	97
3.5	Integrating and sampling capacitance values	98
3.6	Transistor dimensions of the double-tail comparator	101
4.1	Requirement, nominal, best and worst case parameter values of the OTAs	114
4.2	Specifications comparison of the proposed RM- $\Sigma\Delta$ M and the architecture developed in by Fekri et al.	120
E.1	TIA requirement	151
E.2	TIA specifications for $C_{p-MEMS} = 10$ pF and $C_{p-load} = 0.1$ pF	156

E.3 Complementary DOTA specifications, considering $I_1 = 25 \mu A$, $\eta = 0.04$,
 $V_{cm} = 0.9V$, $L = 4L_{min}$ and $C_{DOTA-load} = 0.1 \text{ pF}$ 167

Notations

MEMS	Micro-Electro- Mechanical-System
SOI	Silicon-On-Insulator
MIM	Metal-Insulator-Metal
WCRs	Weakly-Coupled-Resonators
DAC	Digital-to-Analog-Converter
ADC	Analog-to-Digital-Converter
$\Sigma\Delta$	Sigma-Delta-Modulator
UICM	Unified Current Control Model
MILOs	Mutually-Injection-Locked-Oscillators
MOLOs	Mode- Localization-Oscillators
FM	Frequency-Modulated
AM	Amplitude-Modulated
PM	Phase-difference-Modulated
RM	Amplitude-ratio-Modulated
RM-WCRs	Amplitude-ratio-Modulated based on Weakly-Coupled-Resonators
RM-ADC	Ratiometric Analog-to-Digital-Converter
VCO	Voltage-Controlled-Oscillator
OL	Open-Loop
CL	Closed-Loop
PLL	Phase-Locked-Loop
TIA	Transimpedance Amplifier
OTA	Operational Transconductance Amplifier
VD	Voltage-Divider
AAF	Anti-Aliasing-Filter
DT	Discrete-Time
CT	Continuous-Time
SC	Switched-Capacitor
MC	Miller-Compensated
LC	Load-Compensated
FC	Folded-Cascode
TC	Telescopic-Cascode
TG	Transmission-Gate switch
ST	Steady-state
PVT	Process-Voltage-Temperature

$ENOB$	Effective-Number-Of-Bits
FOM	Figure-Of-Merit
SR	Slew-Rate
GBW	Gain-Bandwidth-Product
PM	Phase-Margin
STF	Signal-Transfer-Function
NTF	Noise-Transfer-Function
$SQNR$	Signal-to-Quantization-Noise-Ratio
SNR	Signal-to-Noise-Ratio
SNR_{PK}	Signal-to-Noise-Ratio Peak value
LSB	ADC Least-Significant-Bit
LSB_Q	Quantizer-Least-Significant-Bit
OSR	Oversampling-ratio
MSA	Maximum-Stable-Amplitude
DR	Dynamic-Range
LR	Locking-Range
$dBFS$	Decibel Full-Scale
$PSD_Q(f)$	Power-Spectral-Density of the oversampled quantization noise
$PSD_{th,in-\Sigma\Delta}(f)$	Power-spectral-density of the thermal noise at the input of the modulator
$\frac{v_q^2}{2}$	In-band quantization noise power
$\frac{v_{th,out-\Sigma\Delta}^2}{2}$	In-band thermal noise power at the output of the modulator
K_B	Boltzmann's constant
ρ	Leakage factor of the DT-integrator
m	Proof mass
k	Spring stiffness
κ	Relative coupling strength
D	Damper coefficient
Q	Quality factor
ζ	Damping ratio
γ	Duffing nonlinear coefficient
ω_0	Natural pulsation of the resonator
ω_r	Resonant pulsation of the resonator
$\Delta\omega$	3dB bandwidth of the resonator (in radian)
BW	3dB bandwidth of the resonator (in Hertz)
Ω_0	Normalized natural pulsation
Ω_r	Normalized resonant pulsation
$x_L(t)$	Position of the mass with respect to its equilibrium position
$x(t)$	Normalized position of the mass with respect to its equilibrium position
$f_{spring}(t)$	Spring restoring force
$f_{damp}(t)$	Damping force
$f_{act}(t)$	Actuation force
$n_{mec}(t)$	Thermomechanical stochastic force
$f(t)$	Normalized actuation force
F	Normalized peak value of the actuation force
F_{sin}	Sinus component of the normalized actuation force
F_{cos}	Cosine component of the normalized actuation force
$n(t)$	Normalized thermomechanical force
N_{sin}	Sinus component of the normalized thermomechanical force
N_{cos}	Cosine component of the normalized thermomechanical force

θ_0	Natural phase shift of the resonator
θ_r	Resonant phase shift of the resonator
ϵ	Normalized variation of the spring stiffness
X	Normalized amplitude motion peak value
X_0	Normalized amplitude motion peak value at the resonant frequency
X_c	Normalized critical amplitude
δX	Small variation of the normalized amplitude motion peak value
$\delta\theta$	Small variation of the resonator phase shift
$\delta\Omega$	Small variation of the normalized pulsation
ϕ	Phase-difference of two coupled resonators
R	Amplitude-ratio of two coupled resonators
B	Bilinear amplitude-ratio of two coupled resonators
f_s	Sampling frequency
f_c	3dB Cut-off frequency of the analog circuit
f_T	Unity gain bandwidth frequency of the amplifier
T_{charge}	Charge phase of the dual-slope ADC
T_s	Sampling time
τ_{int}	Time constant in the closed loop DT-integrator
t_{slew}	Integrator output slewing time
Φ	Integrator Clock phase
Φ_d	Integrator delayed clock phase
$H_{mec}(s)$	Resonator's mechanical transfer function
$H_{int}(s)$	Closed-loop transfer function during the integrating phase
A	DC-gain of the amplifier
A_{int}	Closed-loop DC-gain during the integrating phase
G_f	Voltage-to-actuation force transducer
$G_{x,y}$	Displacement-to voltage transducer
V_{DD}	Higher supply voltage
τ_{int}	Time constant in the closed loop DT-integrator
t_{slew}	Integrator output slewing time
Φ	Integrator Clock phase
Φ_d	Integrator delayed clock phase
$H_{mec}(s)$	Resonator's mechanical transfer function
$H_{int}(s)$	Closed-loop transfer function during the integrating phase
A	DC-gain of the amplifier
A_{int}	Closed-loop DC-gain during the integrating phase
τ_{int}	Time constant in the closed loop DT-integrator
t_{slew}	Integrator output slewing time
Φ	Integrator Clock phase
Φ_d	Integrator delayed clock phase
$H_{mec}(s)$	Resonator's mechanical transfer function
$H_{int}(s)$	Closed-loop transfer function during the integrating phase

A	DC-gain of the amplifier
A_{int}	Closed-loop DC-gain during the integrating phase
G_f	Voltage-to-actuation force transducer
$G_{x,y}$	Displacement-to voltage transducer
V_{DD}	Higher supply voltage
V_{SS}	Lower supply voltage
V_0	Resonator steady state output voltage at the natural pulsation
V_{I-os}	Voltage output swing of the integrator
V_{cm}	Common mode voltage
V_{G-os}	Voltage output swing of the MEMS sensing amplifier
V_{ov}	Overdrive voltage
V_{OL}	Voltage-Overload-Level
V_{ref}	ADC Reference-Voltage
V_{DAC}	DAC Maximum voltage value
V_{Q-FS}	Quantizer-Full-Scale-Voltage
V_{drop}	Drop voltage due to charge redistribution effect in the integrator
V_{th}	Threshold voltage
$v_{x,y}(t)$	Sensing voltage
$\delta V_{x,y}$	Small variation of the sensing voltage peak value
$v_{I-in}(t)$	Integrator input voltage
$v_{I-out}(t)$	Integrator output voltage
ϕ_t	Thermal voltage
I_d	Drain-source forward current in MOS transistor
I_{SR}	Current during output slewing time
I_S	Specific current
i_d	Forward normalized current
$i_x(t)$	Sensing current
C_{ox}	Gate oxide capacitance per unit area
$C_{a,b}$	CMFB capacitors
C_{load}	Equivalent load capacitance in the closed loop integrator
C_p	Output parasitic capacitance in the closed loop integrator
C_s	Sampling capacitance
C_i	Integrating capacitance
C_f	Feedforward capacitance
R_{on}	On-resistance of the switch
R_{mean}	On-resistance mean value of the switch
g_m	Transconductance
a	Integrator loop coefficient
c	Feed forward coefficient
b	Feedback coefficient
α_{Vth}	Temperature coefficient of the threshold voltage
α_μ	Temperature dependence power coefficient for the mobility
μ	Carrier mobility
$\bar{\mu}$	Gaussian distribution mean value
σ	Gaussian distribution standard deviation
σ_t	Clock jitter standard deviation
n_a	Noise factor of the integrator
n_f	Noise factor of the amplifier
n_{th}	Subthreshold slope factor

Résumé long en français

Introduction et motivation

La technologie MEMS a permis l'émergence de capteurs résonants (inertiels, de masse, de température, de pression...), avec un facteur de qualité élevé ($Q > 500$), une taille microscopique et à basse consommation. Comme dans tout capteur, la sensibilité à la grandeur mesurée doit être maximisée (S_{mesure}), et la sensibilité aux fluctuations, telles que le dérive et le bruit (S_{bruit}), doivent être minimisées pour améliorer la résolution. Plusieurs approches existent dans la littérature pour supprimer ou compenser l'effet de dérive. Ils comprennent la compensation numérique avec des microprocesseurs et des capteurs de température, ou des architectures de capteurs différentiels. Ces dernières années, les architectures différentielles basées sur des résonateurs faiblement couplés (WCR) tels que les oscillateurs à injection verrouillée mutuellement (MILO) (voir la figure 1(a)) sont devenues un bon candidat pour la mesure avec une stabilité thermique élevée. Ils visent l'amplification de la variation différentielle de masse ou de raideur (k) de deux résonateurs tout en étant fortement insensible aux variations thermiques affectant également les deux résonateurs.

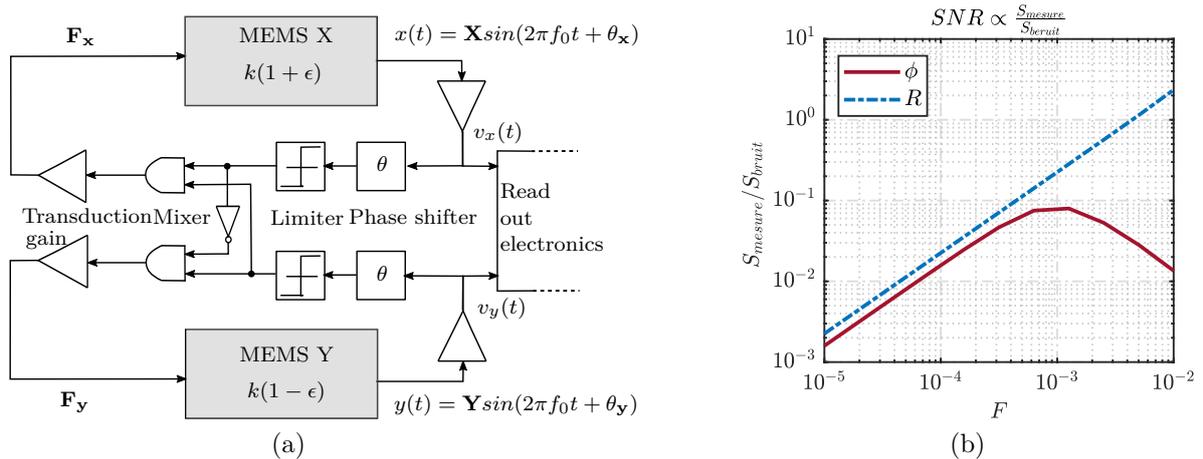


Figure 1 : Vue au niveau système des oscillateurs à injection verrouillée mutuellement (MILO) (a), performance de la mesure de différence de phase ϕ et le rapport d'amplitude R du MILO en fonction de force d'excitation F (b)

Une vue au niveau système du capteur WCR à base de MILO est représentée sur la figure 1(a). Les deux résonateurs (MEMS-X et MEMS-Y) sont placés dans une seule boucle oscillante, à l'intérieur de laquelle leurs signaux d'excitation sont issus d'un mélange entre les deux signaux de sortie. Pour certaines conditions de θ du mélangeur, l'oscillation démarre et les deux résonateurs se synchronisent et oscillent à la même fréquence (f_0). Les informations détectées différenciellement sont donc mesurées soit par la différence de phase ($\phi = \theta_x - \theta_y$), soit par le rapport d'amplitude ($R = X/Y$) entre les signaux de sortie des résonateurs. La mesure de différence de phase ϕ est généralement préféré en raison de sa nature quasi numérique. Cependant, il est récemment démontré que sous une force d'excitation élevée (F), R peut offrir un rapport signal sur bruit ($SNR \propto S_{mesure}/S_{bruit}$) plus grand que ϕ comme le montre la figure 1(b). En effet, quand la force d'excitation (F) est faible, $SNR(R)$ et $SNR(\phi)$ disposent tous les deux le même comportement avec F . Quand F devient grande la performance de $SNR(R)$ continue à augmenter linéairement avec F , alors que la performance du $SNR(\phi)$ diminue avec F . L'origine de cette dégradation c'est l'effet de non-linéarité cubique ou non-linéarité de duffing dans le résonateur.

Ces caractéristiques de la mesure du rapport d'amplitude R motivent nos recherches pour un moyen efficace de déterminer et de convertir cette quantité du domaine analogique vers le domaine numérique. Toutefois, l'interface de lecture souhaitée doit être conçue avec une stabilité thermique élevée pour préserver la capacité de rejet de dérive de la détection différentielle. Il est destinée aux applications automobiles, avec une plage de température allant de -40 jusqu'à 125 °C, pour cela les circuits ont été conçus sous la technologie SOI-180nm de la série XH018 pouvant supporter une température allant jusqu'à 175 °C.

Interface de lecture ratiométrique

L'approche la plus courante pour déterminer la quantité $R = X/Y \equiv V_x/V_y$ consiste à numériser les signaux de mouvement (à une fréquence d'échantillonnage bien supérieure à la fréquence d'oscillation) en utilisant deux convertisseurs analogique numérique (CAN), puis effectuer la démodulation et la division dans le domaine numérique. Cela nécessite deux CANs à haute résolution et à haute fréquence d'échantillonnage (f_s). Toutefois, il faut que les caractéristiques de deux CANs soient parfaitement identiques, ce qui ne peut pas être assuré tenu compte de la variation de température qui peut s'élever jusqu'à 125 °C. La deuxième approche consiste à démoduler et diviser les signaux dans le domaine analogique, puis numériser le rapport de tension par un CAN avec une fréquence d'échantillonnage f_s relativement faible. Les circuits généralement utilisés pour implémenter le diviseur de tension dans le domaine analogique sont les log-anti-log-circuits basés sur des diodes. Cependant, les caractéristiques de la diode sont très dépendants de température, et donc cette solution n'est pas préférable pour notre l'application. La troisième approche consiste à utiliser un seul CAN qui effectue en une seule étape la division et la conversion analogique numérique. En effet, le rapport des tensions des signaux d'amplitude démodulés V_x et V_y peut être effectué en injectant l'un de ces deux signaux, par exemple V_x , à l'entrée du CAN, et utilisant l'autre signal, c'est-à-dire V_y , comme une tension de réf-

rence (V_{ref}) du CAN. Comme la sortie du CAN est la valeur numérique du signal d'entrée relatif à la tension de référence, la réponse du CAN est donc équivalente à la quantité $R = V_x/V_y = V_{in}/V_{ref}$. Le grand avantage de cette solution par rapport à la première solution est qu'un CAN est omis, et par rapport à la deuxième solution est que le besoin du diviseur de tension est relaxé. En outre, le traitement des signaux à basses fréquences (dans une bande de 2 kHz) élimine le besoin d'un CAN à échantillonnage élevé, minimisant ainsi la consommation d'énergie. Cette approche est initialement proposée par Fekri et al. (2014) pour des capteurs à courants de Foucault, mais elle n'était pas optimisée aux variations de température, mais aussi fonctionne sous une seule fréquence d'échantillonnage. Le circuit de lecture développé dans ces travaux est basé sur cette approche mais adapté aux capteurs WCRs, optimisé contre les variations de température de -40 jusqu'à 125 °C, et peut fonctionner avec une fréquence échantillonnage inférieure ou égale à 1 MHz. Il est à noter que pour assurer la stabilité du CAN, la tension de référence (c'est-à-dire V_y) doit toujours être supérieure à la tension d'entrée (c'est-à-dire V_x). Autrement dit, il faut que la quantité $|R| = |V_x/V_y|$ soit toujours inférieure ou égale à 1. Cependant, en considérant la détection différentielle du MILO, la tension V_y peut être inférieure à la tension V_x . Pour cette raison, une sortie ratiométrique alternative à R ayant les mêmes propriétés (SNR), mais assurant la stabilité du CAN a été proposée. Cette métrique est donnée par :

$$B = \frac{V_x - V_y}{V_x + V_y} = \frac{V_{in}}{V_{ref}}$$

Considérant l'architecture de MILO, le métrique B est toujours borné à ± 0.57 . Dans ces travaux nous nous intéressons à la partie étude, conception et implémentation du CAN quantifiant la quantité B . La partie électronique du MILO ainsi que les blocs réalisant la démodulation des signaux ne sont pas détaillés.

Architecture du CAN sélectionnée

L'interface de lecture proposée est basée sur les convertisseurs analogique-numérique de type sigma-delta ($\Sigma\Delta$ CANs). Ces CANs combinent le concept de suréchantillonnage et la technique de mise en forme du bruit pour atteindre une résolution élevée avec une complexité et une consommation d'énergie relativement faibles. Le suréchantillonnage consiste à échantillonner le signal (à numériser) avec un facteur OSR fois plus vite que sa bande passante ($BW < f_0/2Q = 2$ kHz), l'erreur de quantification est distribuée sur une plage spectrale plus grande, diminuant alors sa puissance dans la largeur de bande du signal BW . La mise en forme du bruit est de donner une forme au bruit de quantification consistant à diminuer sa puissance dans la bande du signal BW et l'augmenter hors bande. La capacité de mise en forme du bruit est déterminée par le nombre des intégrateurs utilisés dans le modulateur $\Sigma\Delta$. Par exemple, dans un modulateur de premier ordre ou ayant un seul intégrateur, la capacité de mise en forme de bruit est de 20 dB/ décade. L'ordre de modulateur est généralement défini pour une fréquence d'échantillonnage donnée, et une résolution requise. Dans ces travaux la résolution ou le nombre de bits effectif ($ENOB$)

ciblé est d'environ 16 bits, donc pour un taux de suréchantillonnage OSR de 256 (ou une fréquence échantillonnage $f_s=1$ MHz), un modulateur de second ordre a été sélectionné. De plus, la nature du modulateur sélectionné est à temps discret où le gain d'intégrateur est implémenté par le rapport de deux capacités. Il est donc plus robuste aux variations de température et de mismatch que le modulateur à temps continu. Une vue au niveau système de l'interface proposée est représentée sur la figure 2(a).

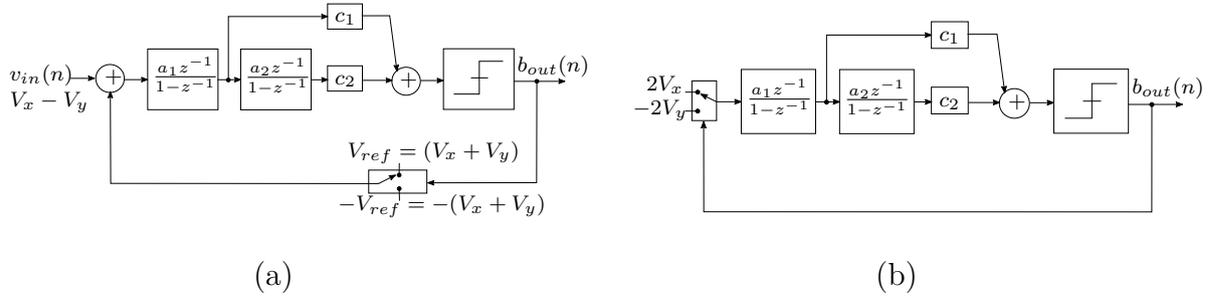


Figure 2 : système du modulateur $\Sigma\Delta$, conventionnel (a), modifié (b)

Il est à noter que le modulateur proposé (figure 2(a)) peut être aussi simplifier en enlevant l'additionneur à son entrée. En effet, quand la sortie est 0 logique, le signal à l'entrée de l'intégrateur vaut $2V_x$, et quand la sortie est 1 logique, ce dernier vaut $2V_y$. Donc en éliminant l'additionneur d'entrée, les signaux issus du MILO peuvent directement être injecter à l'entrée du modulateur comme le montre la figure 2(b). Ce qui reste à déterminer dans cette architecture sont les coefficients c_1, c_2, a_1 et a_2 . Ces paramètres définissent la plage de dynamique, et en partie la résolution du modulateur.

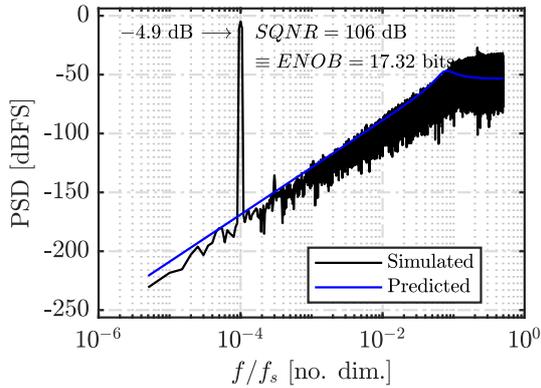


Figure 3 : PSD du modulateur pour $c_1 = c_2 = 1, a_1 = 0.8$ et $a_2 = 0.5$

L'objectif est donc d'atteindre le maximum signal sur bruit de quantification ($SQNR$) pour une dynamique de $0.57 \equiv -4.9$ dB. Pour cela l'architecture présentée sur la figure 2 a été simulée sur MATLAB en utilisant $\Sigma\Delta$ toolbox développé par Schreier. La combinaison optimale des coefficients trouvée est $c_1 = c_2 = 1, a_1 = 0.8$ et $a_2 = 0.5$. La densité spectrale de sortie du modulateur correspondante (PSD) est représentée sur la figure 3. Comme on peut le voir une résolution d'autour 17.32 bits est obtenue en tenant compte juste du bruit de quantification.

Autrement dit, une résolution de 16 bits après l'implémentation électrique du modulateur peut être obtenue en réservant 1.32 bits ou 7.9 dB de marge pour le bruit électrique et les non-idéalités des bloques analogiques (Principalement les amplificateurs). L'implémentation au niveau électrique du modulateur est donnée sur la figure 4.

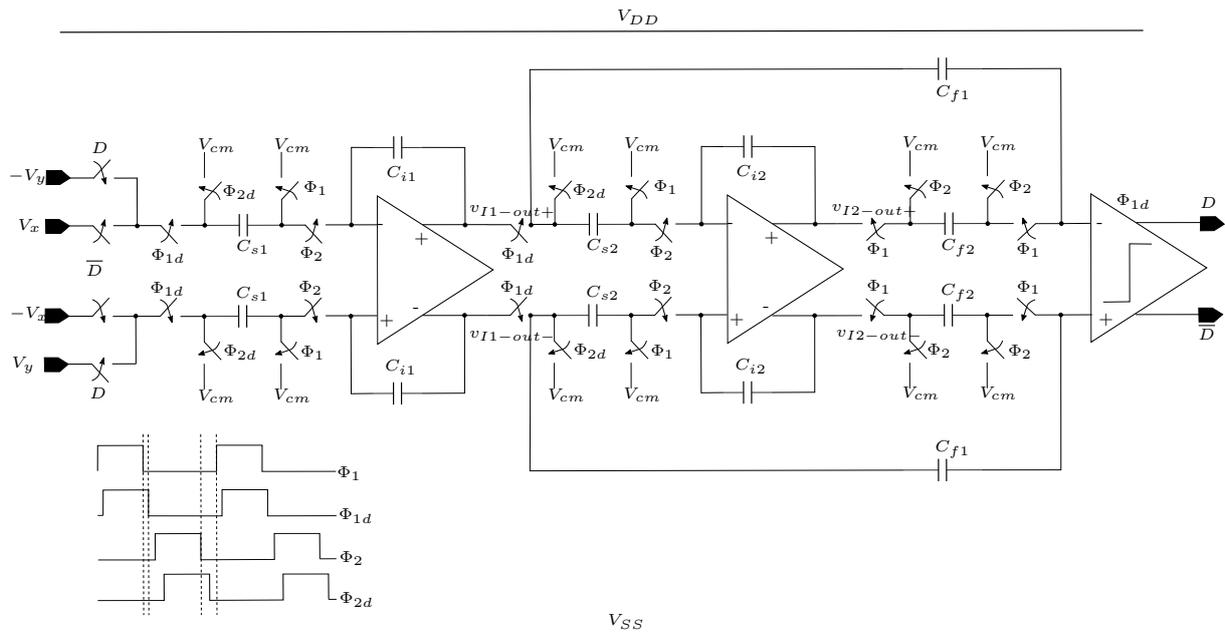


Figure 4 : Implementation électrique du modulateur

Spécifications des blocs analogiques

Les non-idéalités d'amplificateur telles que le gain DC fini (A), la limitation du slew-rate (SR) et du produit gain-bande passante (GBW) sont les causes du transfert incomplet de la charge dans un intégrateur à capacités commutés (voir figure 5). De plus, le bruit électronique du réseau de commutation (kT/C) est la cause majeure de la dégradation du $SQNR$ dans le modulateur $\Sigma\Delta$. Cependant, les trois premières non-idéalités peuvent être spécifiées en considérant la préservation de la réponse idéale du circuit. Par contre, les sources de bruit ne peuvent pas être évitées ou compensées. Donc seule une petite fraction de 0.5 dB est spécifiée pour les non-idéalités des amplificateurs.

Le gain de l'amplificateur est généralement défini selon l'ordre du modulateur et le facteur de suréchantillonnage OSR . Donc si seulement 0.2 dB parmi 0.5 dB est réservé pour cet effet, pour un modulateur d'ordre 2, A doit être $> 3 \cdot OSR \equiv 58$ dB. Par ailleurs, les spécifications SR et GBW dépendent de la nature de l'amplificateur, les valeurs des capacités constituant l'intégrateur et la fréquence d'échantillonnage. Un modèle de reproduction précise de la réponse d'un intégrateur pendant sa phase d'intégration a été donc élaboré. Il permet de s'assurer du bon fonctionnement du modulateur sans sur-dimensionner l'amplificateur, afin de réduire sa consommation au maximum. De plus, et selon la nature de l'amplificateur utilisé, le modèle proposé lie les spécifications SR et GBW de haut-niveau au paramètre g_m/I_d du transistor de bas-niveau. Ce qui permet

ainsi d'optimiser le choix de SR et de GBW pour une condition de polarisation g_m/I_d prédéfinie du transistor. Dans ces travaux, l'amplificateur de type folded-cascode a été choisi, dans ce cas on a $GBW/SR = g_m/I_d$. La figure 5 montre la réponse d'un intégrateur analogique durant sa phase d'intégration.

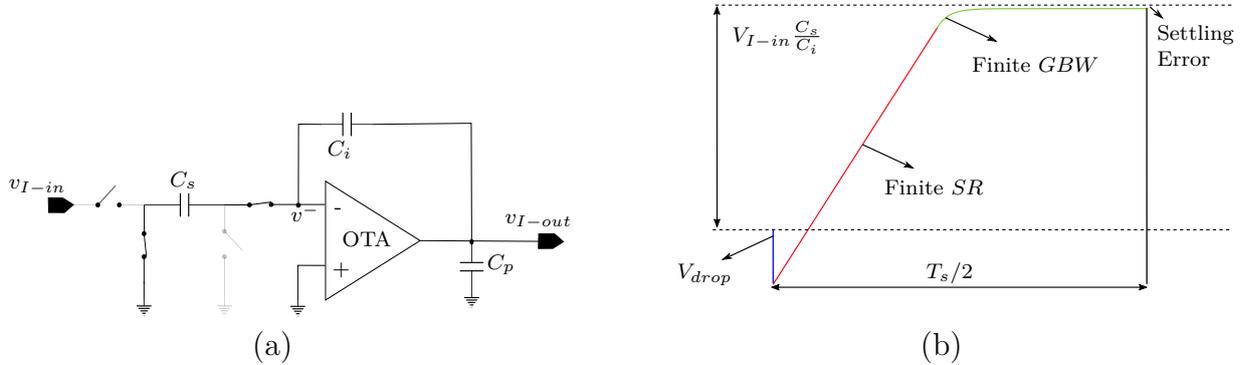


Figure 5 : Intégrateur (a), et sa réponse de sortie (b) durant la phase d'intégration

L'évolution temporelle de la tension de sortie ($V_{I-out} = a \cdot V_{I-in}$) pendant la phase d'intégration peut être divisée en trois parties. Au moment du démarrage, une baisse potentielle (V_{drop}) se produit en raison de l'effet de redistribution de charge (représentée par la ligne bleue sur la figure 5(b)). Ensuite, l'amplificateur commence à agir pour charger la capacité C_i selon les spécifications SR et GBW . Pendant le temps αT_s (représentée par la ligne rouge), la réponse est linéaire avec une pente de SR . Ensuite la tension de sortie suit une évolution exponentielle (représentée par la ligne verte) avec une constante de temps définie par la valeur du GBW . Comme pour l'effet de gain fini A , si 0.2 dB de perte du $SQNR$ ou une erreur de $\xi = 1\%LSB$ est fixée à cause de ces deux effets, le modèle proposé liant le SR et le GBW avec α et g_m/I_d est donné par les expressions suivantes :

$$SR = \frac{V_{I-out} + V_{drop} - \frac{1+a}{g_m/I_d}}{\alpha T_s/2}, GBW = \frac{1+a}{(1-\alpha)T_s/2} \cdot \ln \left(\frac{1}{\xi} \cdot \frac{1+a}{V_{I-out}} \right),$$

$$GBW/SR = g_m/I_d \text{ et } V_{drop} = C_i \frac{V_{I-out}}{C_s + C_p \left(1 + \frac{C_s}{C_i}\right)}.$$

La tension de sortie maximale V_{I-out}^{max} est fixée par la dynamique de sortie de l'amplificateur. Donc à partir des valeurs des capacités, la fréquence échantillonnage, et la condition de polarisation g_m/I_d , la combinaison optimale des spécifications SR et GBW peut être déterminée. Comme on le verra plus tard, pour améliorer la stabilité thermique du GBW , la condition g_m/I_d des transistors d'entrées doit être choisie autour 9. Les valeurs des capacités ainsi que les spécifications des amplificateurs pour ne pas dépasser une perte de 7.9 dB de $SQNR$ à la température $T = 125$ °C sont listés dans le tableau 1.

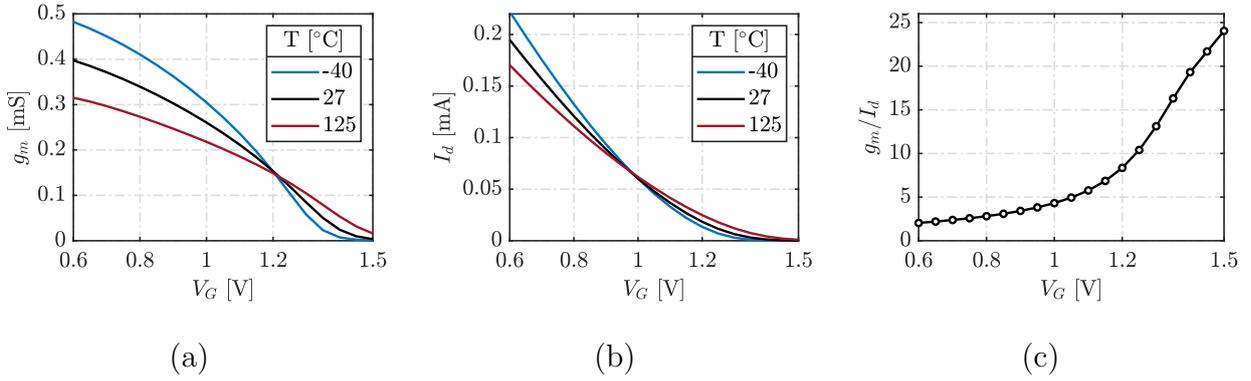


Figure 9 : Paramètres de transistor PMOS simulés en fonction de la tension de grille V_G sous les trois températures -40 , 27 , et 125°C , (a) g_m , (b) I_d , et (c) g_m/I_d

La transconductance drain-source g_{ds} ne dépend juste de la condition de polarisation, mais aussi de la longueur du canal L et de la tension drain-source V_{DS} du transistor. Donc, pour déterminer les conditions g_m/I_d aux quelles la stabilité thermique de g_{ds} est maximisée, la sensibilité de g_{ds} avec la température a été simulée pour deux valeurs de L $\{0.18\mu\text{m}, 3\mu\text{m}\}$, et sous différentes tension V_{DS} $\{0.2\text{V}, 0.9\text{V}, 1.35\text{V}\}$. Les résultats de simulation sont représentés sur la figure 10.

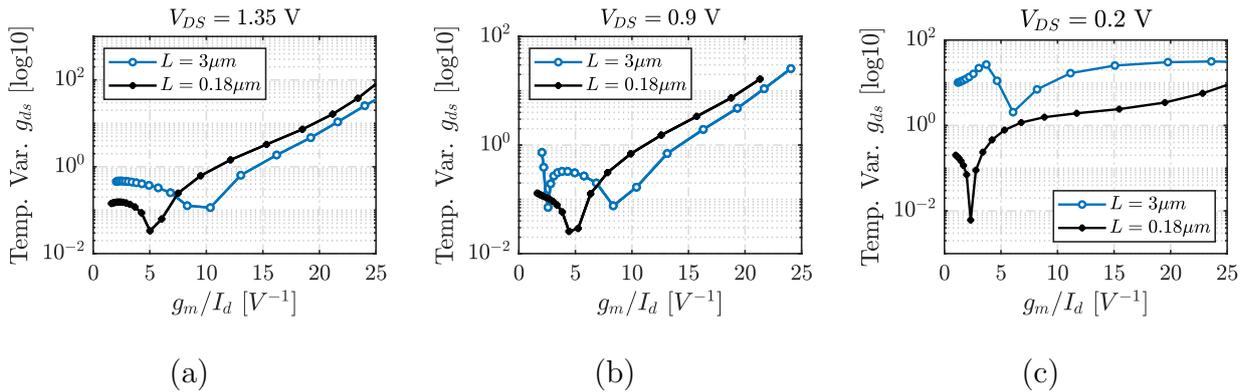


Figure 10 : La sensibilité de g_{ds} avec la température d'un transistor PMOS simulée pour deux valeurs de $L = 0.18\mu\text{m}$ (en noir) et $L = 3\mu\text{m}$ (en bleu), et sous différentes tension drain-source, $V_{DS} = 0.2\text{V}$ (a), $V_{DS} = 0.9\text{V}$ (b), et $V_{DS} = 1.35\text{V}$ (c)

Comme on peut le voir sur la figure 10, pour une tension V_{DS} inférieur à 1.35 V (qui est généralement le cas), et une longueur L plus petite que $3\mu\text{m}$, les conditions g_m/I_d sont entre $2 \sim 10$. Autrement dit, pour une condition g_m/I_d donnée (prédéfinie pour minimiser la variation du courant par exemple), une valeur de L peut donc être sélectionnée afin de minimiser la variation de g_{ds} avec la température. Le tableau 2 résume les conditions de polarisations des transistors de l'amplificateur folded-cascode présenté sur la figure 7.

Tableau 2: Conditions de polarisations des transistors

Transistor	g_m/I_d	Minimiser la Variation
M_0	6	I_d
$M_{1(2)}$	9	g_m
$M_{3(4)}$ et $M_{5(6)}$	6 ($L = 3\mu m$)	I_d et g_{ds}
$M_{7(8)}$ et $M_{9(10)}$	5 ($L = 3\mu m$)	I_d et g_{ds}

Les résultats de simulation post-extraction des paramètres GBW , A et SR en fonction de température sont présentés sur la figure 11 pour le premier amplificateur (courbes noires) et le deuxième amplificateur (courbes bleues). GBW , A et SR montrent une stabilité thermique élevée qui, de 27 à 125 °C, ne diminuent que de (1.6 MHz, 0.7 dB et 1.2 MV/s) et de (1.2 MHz, 0.3 dB et 0.2 MV/s) respectivement pour le premier et le deuxième amplificateur. Les valeurs minimales de ces paramètres sont observées à la température 125 °C, mais ils respectent toujours les valeurs spécifiées dans le tableau 1.

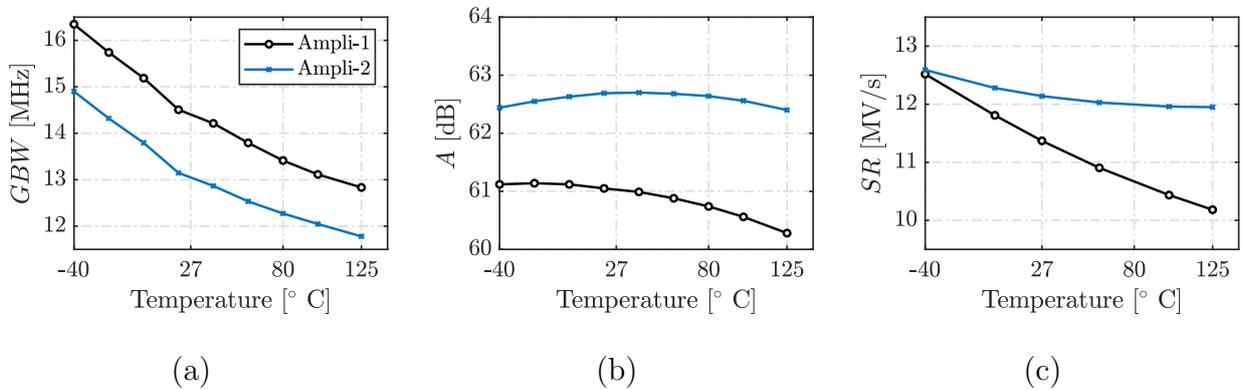


Figure 11 : Résultats de simulation post-extraction du produit gain-bande GBW (a), du gain DC A (b), et du slew-rate SR (c) en fonction de températures pour le premier amplificateur (courbes noires) et deuxième amplificateur (courbes bleues)

Implémentation du modulateur complet et résultats post-extraction

L'implémentation finale du modulateur proposé est représentée sur la figure 12. Les commutateurs et les banques des capacités sont répartis de manière à préserver une symétrie géométrique dans les deux directions. De plus, en alignant les commutateurs et les placer comme indiqué sur la figure 12 facilite la connectivité avec les signaux de commande. Le circuit de polarisation est partagé avec le premier et le deuxième amplificateur, et placé entre eux pour réduire la longueur des métaux du rail fournissant les tensions de polarisation. Le modulateur occupe une surface de $530 \times 540 \mu m^2$ et consomme de 0.8 mW sous une tension de polarisation de 1.8 V. Figure 13(a) représente les résultats de simulation

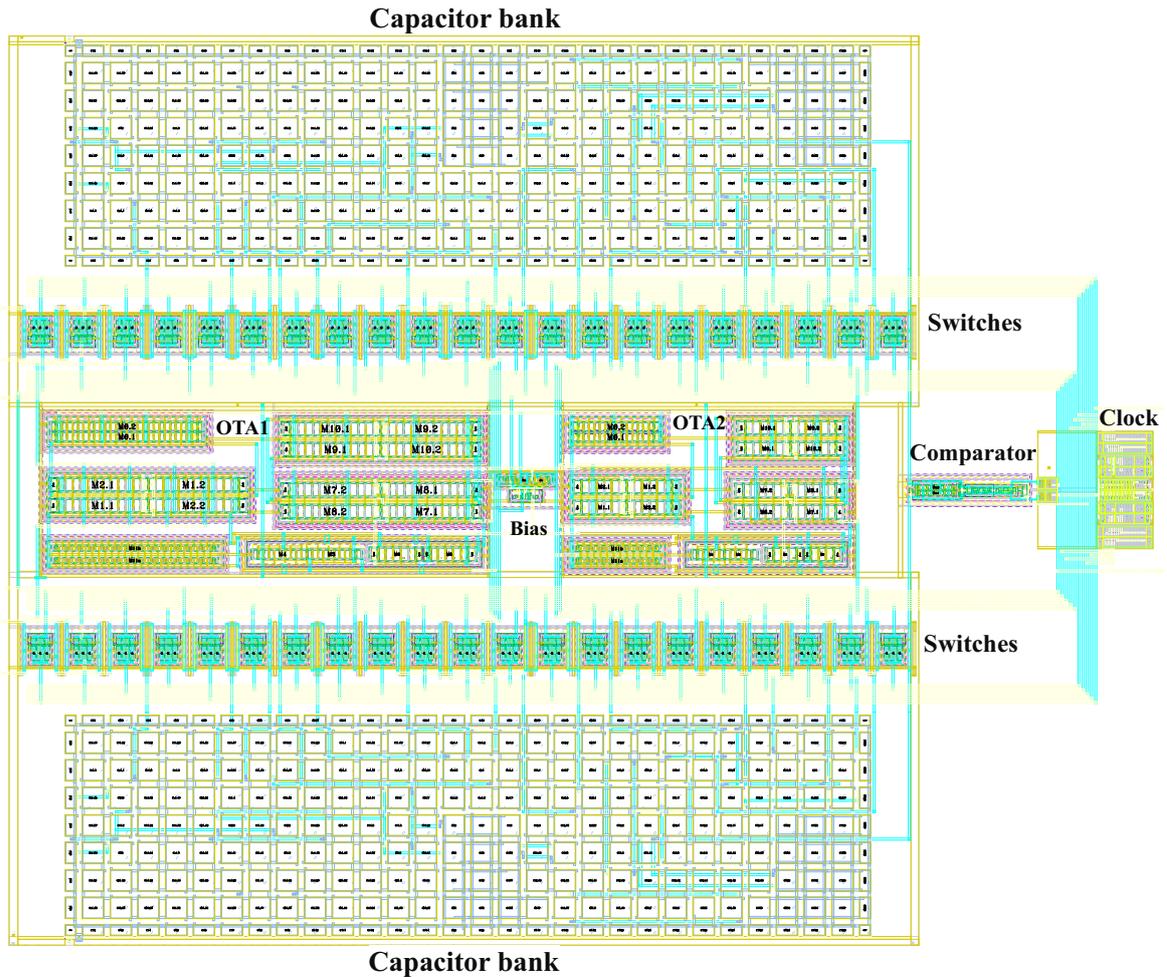
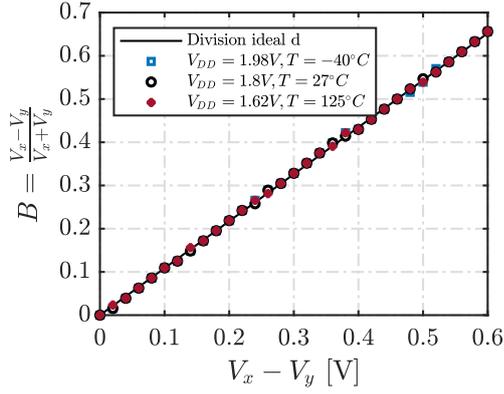
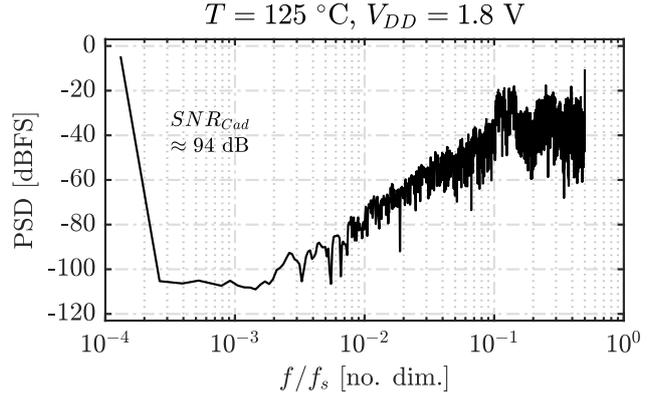


Figure 12 : Layout du modulateur ayant une surface de $530 \times 450 \mu m^2$

post-extraction de la réponse ratiométrique du modulateur sous différentes températures en tenant compte la variation standard de $\pm 10\%$ de tension d'alimentation $V_{DD} = 1.8 V$. On constate que le circuit possède une grande fiabilité aux variations de température et de tension d'alimentation, et quasiment aucune dégradation peut être constatée entre les trois courbes. Le modulateur possède aussi une bonne linéarité pour une dynamique même au-dessus de 0.57. La densité spectrale de sortie du modulateur obtenue à partir d'une simulation transitoire (NFFT 7630 points) considérant le pire cas à la température $125^\circ C$ est donnée sur la figure 13(b). Pour une fréquence d'échantillonnage $f_s = 1 MHz$, et une bande de signal $BW = 2 kHz$, la SNR obtenue est autour de 94 dB correspond à un $ENOB$ d'environ 15.34 bits. Notant que la résolution obtenue est légèrement inférieure à celle attendue de 16 bits. Cependant, des résultats plus précis du SNR peuvent être obtenus avec un nombre plus élevé de points, par contre la simulation du bruit transitoire prendra un temps de simulation très longs. Le tableau 3 résume et compare les spécifications du modulateur ratiométrique proposé avec l'architecture développée par Fekri et al.



(a)



(b)

Figure 13 : Résultats post-extraction de la sortie ratiométrique du modulateur sous différentes températures $\{-40, 27, \text{ et } 125\text{ }^\circ\text{C}\}$, et différentes tensions d'alimentation $\{V_{DD} = 1.8\text{V} \pm 10\%\}$ (a), et la densité spectrale PSD à la température $125\text{ }^\circ\text{C}$ (b)

Tableau 3 : Performance et comparaison

	Ce travail	Fekri, 2014
Technologie	SOI-XH018 ($0.18\ \mu\text{m}$)	Si/Ge BiCMOS ($0.35\ \mu\text{m}$)
Domaine	Temps discret	Temps continu
Température	$-40 \leq T[^\circ\text{C}] \leq 125$	$T = 27\text{ }^\circ\text{C}$
Horloge	$f_s \leq 1\text{ MHz}$	$f_s = 1\text{ MHz}$
Bande du signal	$BW \leq 2\text{ kHz}$	$BW \leq 1\text{ kHz}$
Nombre de bits effectif	$ENOB \approx 15.34\text{ bits}$	$ENOB \approx 15\text{ bits}$
Dynamique de sortie	$DR < 0.6$	$DR < 0.7$
Tension de référence	$V_{ref} = 0.46\text{ V}$	$V_{ref} = 0.45\text{ V}$
Consommation	$P_{rms} \approx 0.8\text{ mW}$	$P_{rms} \approx 2.8\text{ mW}$
Surface	$530 \times 450\ \mu\text{m}^2$	—
$FOM = 20 \log \left(\frac{2^{ENOB} \times BW[\text{kHz}]}{P_{rms}[\text{mW}]} \right)$	98 dB	81 dB

Conclusion et perspectives

En conclusion, ce travail a souligné les avantages des capteurs à base de MILOs notamment pour la mesure de rapport d'amplitudes. Pour quantifier et convertir cette quantité du domaine analogique vers le domaine numérique, une interface de lecture à base de modulateur sigma delta a été adapté. Un travail complet a été mené, depuis la modélisation mathématique, conception électrique, jusqu'à la réalisation du dessin des masques d'intégration. L'interface proposée et optimisé aux variations de température sur une gamme allant du -40 jusqu'à $125\text{ }^\circ\text{C}$, tout en conservant une résolution élevée de 15 à 16 bits. Le dessin final ainsi que la photographie microscopique de la puce fabriquée sont représentées sur la figure 14. A coté du modulateur la puce comprend principalement un

amplificateur autonome qui sera testé séparément pour évaluer ses performances vis-à-vis de température. En raison du manque de temps, la configuration expérimentale et la mesure de la puce n'ont pas été accomplies. Le point suivant de ces travaux sera divisé en deux phase. Dans la première phase, le modulateur sera testé séparément du MILO, et ses performances seront évaluées sur une gamme de température allant jusqu'à 125 °C. Dans ce cas, les signaux d'entrée ainsi que le signal d'horloge seront fournis par des sources de signaux hors puce. Une résolution de 15 bits ou un SNR de plus que 92 dB est théoriquement prévu à ce point. Ceci est généralement suffisant pour ignorer sa contribution du bruit devant le capteur MILO. Dans une deuxième phase, l'ensemble du circuit (MILO + modulateur) va être testé. En d'autres termes, les signaux d'entrée hors puce vont être désactivés et fournis directement par le MILO, le système sera testé sous différents états de fonctionnement (force d'excitation) et les résultats du rapport d'amplitudes tirés seront ensuite comparés avec les mesure de la différence de phase afin de mettre en évidence notre approche.

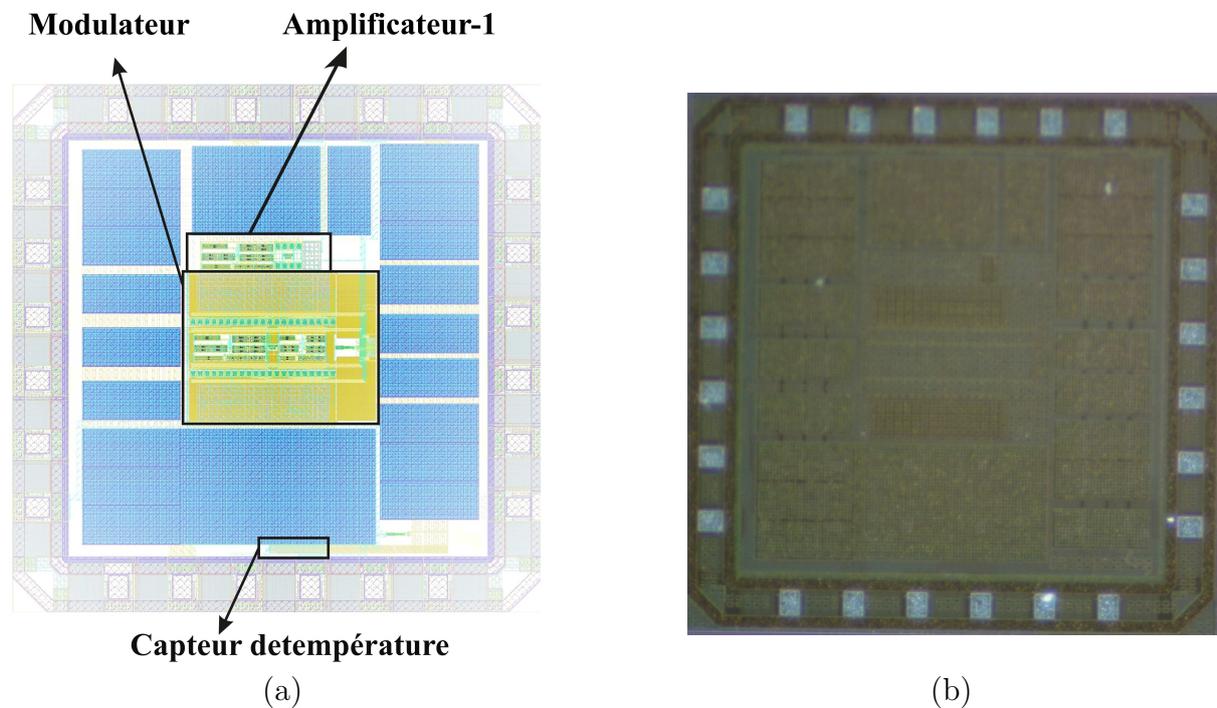


Figure 14 : Dispositif complet, (a) dessin des masques, (b) photographie microscopique de la puce

Introduction

Background and motivation

The rapid development of the microelectronics industry is the result of the advances in semiconductor manufacturing technologies. These advances have made possible the miniaturization of various sensors, and mechanical components which combined with electronics form what is known as a Micro-Electro-Mechanical-System (MEMS) or a microsystem. In a MEMS device, forces may be transduced from the electrical domain to the mechanical domain for actuation purposes, and mechanical motion may be transduced to the electrical domain for sensing purposes. In addition, the MEMS technology provides a possibility of extending the microelectronic revolution even further, to CMOS/MEMS co-integration. Its ultimate goals have been and will continue to be continuous miniaturization, expanded functionalities, lower cost, smaller size, and improved performance and reliability[1].

Microsystems can be used in vehicles, for example, as accelerometers [2] for airbag deployment, pressure sensors [3] for smart tire pressure monitoring. They can also be used as mass sensors [4] or gyroscopes to sense angular velocity or acceleration [5] for stability and vehicle safety. More than 200 sensors are expected in the new generation of smart vehicles, and they represent new investments in sensors and integrated circuits that, between 2017 and 2019, represented a 1.3 billion dollars worldwide investment with projections of growth in the next coming years [6]. However, in automotive applications, the circuit specification is strictly regulated by security and safety standards. The temperature range is arguably the most difficult environmental challenge for the sensors in the automotive industry [7]. Reliability and robustness in the device operation must be ensured for harsh environments, within the temperature range of the industrial automotive application $-40 \leq T \leq 125$ °C.

Extreme temperature conditions pose an interesting challenge for the design of integrated silicon resonant sensors. In particular, while silicon resonators are much cheaper than quartz resonators, the temperature coefficient of quartz is much lower than that of silicon [8]. In recent years, research has been actively conducted to address this material-related issue with system-level solutions, such as differential resonant sensor architectures. In particular, resonant MEMS sensors based on Weakly-Coupled-Resonators (WCRs) [9, 10, 11]. They target the amplification of difference in mass or stiffness of

two resonators, while being highly unaffected by thermal variations equally affecting both resonators. Compared to the conventional single resonator sensing architectures with Frequency-Modulated output (FM, i.e., the variation of their oscillation frequency is proportional to the quantity of interest) [3], WCRs have usually Amplitude-Ratio (between the two coupled resonators) Modulated output (RM), or Phase-difference Modulated output (PM). Thus, they are first-order independent of drift since their output metrics are intrinsically differential. As an example in [9] it has been highlighted that using PM differential measurement based on WCRs, a drift rejection ratio of higher than 100 times compared to the conventional sensing architectures can be achieved. This feature has also been emphasized using RM mode based WCRs as it was theoretically and experimentally proved in [10].

Generally, PM mode is more linear than the RM mode and is more amenable to integration because it has duty-cycle or pulse-width-modulated output [9]. However, it has been (theoretically and experimentally) highlighted that the RM mode is beneficial in terms of resolution (small detectable quantity with respect to the noise in the system, i.e. thermal noise) in some operating regime [12, 13]. This feature is not only advantageous in the nominal working conditions, but also at high temperatures where a higher thermal noise is expected. However, amplitude ratio is not a quasi-digital quantity, as opposed to phase difference, so that RM-WCRs need to overcome the bottleneck of an analog-to-digital voltage divider for successful integration. Considering the specified temperature range, a high resolution, high reliability voltage divider circuit in analog domain is not a trivial task, but remains a subject of current research.

Nevertheless, thermal stability issues in resonant sensing applications should not be envisioned from the point of view of the mechanical structure only. Recent study considering WCRs architecture has highlighted that thermal drift of the sustaining electronics that couple the two resonators is also one of the main issues limiting the performance of the sensor [14]. It may cause an error drift of several orders of magnitude beyond the resolution of the system. Thus, a high thermal stability of the MEMS sustaining electronics (hence an optimal sensor performance) must be ensured, before signals acquisition (performed by the ratiometric interface).

This manuscript presents the author's contribution to addressing the issues raised in this scientific context. It summarizes three years of research, from 2017 to 2020, at the GeePs laboratory.

Research Contribution

The present work has three areas of focus. First, it provides a general comparison of different sensor topologies, including differential architectures based on actively- and passively WCRs, such as Mutually-Injection-Locked-Oscillators (MILOs) [11] and Mode-Localization-Oscillators (MOLOs) [15]. It shows the benefits of using a ratiometric measurement over the conventional metrics schemes in terms of parametric sensitivity, and

robustness to the undesired fluctuations originating from system noise and non-idealities.

Second, and the main part of this work concentrates on the design of high-resolution (16 bits) Ratiometric Analog-to-Digital interface (RM-ADC) considering the temperature range of the industrial automotive application $-40 \leq T \leq 125$ °C, a sampling frequency of 1 MHz or lower, and a 2 kHz data rate. This interface is elaborated from system specifications and modeling, to transistor-level and layout mask drawing. Indeed, a large amount of system-level analysis on RM-WCRs is experimentally investigated and validated by our research team before concentrating on the design of the readout circuitry developed in this work. The circuit is carried out using SOI 0.18 μm of the XH018 process technology from the X-FAB Silicon Foundries [16]. This technology has an operating temperature up to 175°C, extending beyond the requirement, while providing a very low leakage current.

Third, it presents a temperature aware design of the preamplifier used in the MILO for coupling the resonators, and possible implementation of the signal-demodulator. These circuits are, however, introduced in less detail in appendix E, but still the most significant properties are provided and important aspects regarding the design are listed. Finally, the mechanical design of the MEMS element, together with the sensor packaging, is completely beyond the scope of this work.

Author's main work

- The ratiometric readout electronics presented throughout this manuscript were designed by the author and assisted by Mr. Jerome Juilliard, Pietro Maris Ferreira and Philippe Bénabès [17]. This interface is based on the sigma-delta ADC ($\Sigma\Delta$ -ADC), which is described and modeled (in chapter two), temperature aware designed (in chapter three), and verified (in chapter four) using SOI-XH018 process technology.
- Under the same technology, the author also designed temperature aware circuits for MILO sustaining electronics comprising: Transimpedance Amplifier (TIA), and Operational Transconductance Amplifier (OTA), that are partially presented in last appendix E, and will soon be published.
- Additionally, to extend the study of the ratiometric interface and the MILO sustaining electronics, the author designed a temperature aware Voltage-Controlled-Oscillator (VCO). This circuit is, however, not presented in the dissertation.

Author's participation

- The initial ideas for MILO structure as WCRs were conceived by Prof. Jerome Juilliard and Dr. Pierre Prache [9, 11]. The author is part of the subsequent system-level analysis and the related experimental results published in [12, 13, 18, 19, 20] and slightly presented in chapter one.

- The author participated with Mr. João Raposo in modeling the temperature effects in MOS transistor, and the proposed temperature aware design methodology that is partially presented in chapter three, and extensively detailed in [21].
- The author is also part with Mr. Pietro Maris Ferreira in analyzing the thermal stability for MILO architecture presented in [14].

Conference and journal papers

- J. Martins, **A. Mostafa**, J. Juillard, R. Hamani, A. Francisco, and P. M. Ferreira, “A Temperature-Aware Framework on gm/ID-Based Methodology using 180 nm SOI from -40 °C to 200 °C,” *Open Journal of Circuits and Systems (OJCAS)*, 2021.
- J. Juillard, **A. Mostafa**, P. M. Ferreira, M. Gouspy, and M. Kraft, “A highly-linear, integration-compatible output metric for amplitude-modulated resonant sensors based on weakly-coupled resonators,” *2020 SENSORS*, pp. 2–5, 2020.
- **A. Mostafa**, J. Juillard, J. R. Raposo, and P. M. Ferreira, “An Adaptative Ratio-Metric Analog-To-Digital Interface For Weakly-Coupled Resonant Sensors Based On Mutually Injection-Locked Oscillators,” *2019 Symposium on Design, Test, Integration & Packaging of MEMS and MOEMS (DTIP)*, pp. 1–4, 2019.
- J. Juillard, **A. Mostafa**, and P. M. Ferreira, “Nonlinear operation of resonant sensors based on weakly- coupled resonators : experimental investigation of an actively-coupled architecture,” 2019. [Online]. Available : <https://hal-centralesupelec.archives-ouvertes.fr/hal-01992556v2>
- P. M. Ferreira, J. R. R. O. Martins, **A. Mostafa**, and J. Juillard, “Process-Voltage-Temperature Analysis of a CMOS-MEMS Readout Architecture,” *2019 Symposium on Design, Test, Integration and Packaging of MEMS and MOEMS (DTIP)*, pp. 19–22, 2019.
- J. Juillard, **A. Mostafa**, and P. M. Ferreira, “Nonlinear operation of resonant sensors based on weakly-coupled resonators: theory and modeling,” *Transactions on Ultrasonics, Ferroelectrics, and Frequency Control (TUFFC)*, vol. 3010, no. 66, 2019.
- J. Juillard, P. M. Ferreira, and **A. Mostafa**, “Nonlinear enhancement of locking range of mutually injection-locked oscillators for resonant sensing applications,” *2018 European Frequency and Time Forum (EFTF)*, pp. 109–113, 2018.
- J. Juillard, **A. Mostafa**, and P. M. Ferreira, “Analysis of resonant sensors based on mutually injection-locked oscillators beyond the critical Duffing amplitude,” *2018 European Frequency and Time Forum (EFTF)*, pp. 114–118, 2018

Organization of the thesis

This thesis is organized into four chapters followed by a global conclusion and research perspectives:

- Chapter 1 proposes an original system-level review of existing resonant sensor architectures, both conventional and coupled, and of their performance. This highlights the benefits that can be drawn from the amplitude ratio output metric and motivates our research for an efficient way of converting this analog quantity into the digital domain. The alternative new "bilinear" amplitude-ratio-modulated metric is also discussed. Finally, an overview on the possible solutions to realize the desired RM-ADC are explained and compared with the existing architectures. Considering the specifications of the resonators, i.e., frequency range and signal bandwidth, there is an emphasis on the sigma-delta ADC interface (RM- $\Sigma\Delta$ -ADC), since it allows a high resolution (16 bits) with relatively low circuit complexity.
- Chapter 2 focuses on the architectural selection of the sigma-delta modulator used to implement the RM-ADC. It includes modulator domain, quantizer resolution, loop filter order, and loop topology. Using a system level model, the architecture is validated using MATLAB®/SIMULINK and VerilogA model using Cadence. There is an emphasis on the discrete-time second order architecture in terms of adaptability to the operating frequency and immunity from temperature variation. It also allows a significant simplification in the design considering the ratiometric functionality of the modulator. The optimum requirements of the main building blocks, i.e., OTA, are determined based on a new system level analysis using g_m/I_d methodology.
- Chapter 3 describes the transistor level design of the analog/digital circuits used in the RM- $\Sigma\Delta$ modulator. Each block is designed in transistor-level, and sizing is highlighted. A special attention is given for the OTA core of the integrator, since their imperfections directly affect the modulator performance, especially at high temperature. For this purpose, and to complete the design flow of the system-level modeling based on g_m/I_d approach, the thermal stability analysis of the main transistor parameters (g_{ds} , g_m and I_d) is also developed using the g_m/I_d methodology. The design was done using SOI 0.18 μm process technology from the X-FAB Silicon Foundries.
- Chapter 4 presents the layout of each building block designed in Chapter 3, and depicts the relevant simulations and results that validate the functionality of the analog blocks and the ratiometric operation of the proposed RM- $\Sigma\Delta$ interface. The final results of the ratiometric functionality highlight the design features of relatively high thermal stability, and robustness against process and supply variation. The results also validate the behavioral and transistor-level analyses of each building block elaborated in chapter 2 and chapter 3. The results are carried out considering Process-Voltage-Temperature (PVT) Monte Carlo or Corner simulations using Cadence Spectre® simulator. Since the transient noise simulation of the entire modulator takes too much time, the PSD of RM- $\Sigma\Delta$ output bitstream is only carried out in the worst case conditions, by considering

maximum temperature value $T = 125$ °C, minimum MEMS quality factor and higher sampling frequency. The obtained SNR under the typical process model and supply was around 94 dB corresponding to an *ENOB* of 15.34 bits at the maximum dynamic range, i.e., 0.57.

- Finally, the concluding remarks and perspectives are given in the global conclusion.

Chapter 1

MEMS resonant sensors and electronic interface

This chapter presents an analysis of open-loop and closed-loop resonant sensor architectures, considering a single resonator (« conventional » architectures) or coupled resonators. Starting from a simple MEMS resonator model, we compare these architectures and their analog or digital output metrics in terms of an original figure-of-merit. This analysis shows that amplitude-ratio measurements RM in coupled-resonator architectures, in spite of requiring analog-to-digital conversion stages, do not suffer from the usual limitations classically associated with resonant sensors. Amplitude ratio being an unbounded quantity, we propose an alternative analog output metric with the same advantages, but which is bounded and, therefore, more amenable to analog-to-digital conversion/integration. Possible state-of-the-art solutions to implement the corresponding readout interface are then compared. Finally, an approach based on $\Sigma\Delta$ ADC is highlighted as the most promising solution for ratiometric measurement.

In the manuscript, the following notation convention is used. The Z-transform of a signal is written in upper case letter, while its temporal expression is written in lower case letter. For example, the Z-transform amplitude voltage at the input of the integrator is referred to $V_{I-IN}(z)$, while its expression in the temporal domain is written $v_{I-in}(t)$. The DC component of the signal is referred with the upper case letter and lower case subscript: V_{I-in} in the example. The normalized sensitivity is referred to $S_a^b = \frac{b_0}{a_0} \frac{\partial a}{\partial b}$, where a_0 / b_0 is a specific value of a/b that is defined in the text accordingly.

1.1 MEMS resonator model

MEMS resonators are composed of a vibrating body acting as a mechanical resonator whose motion can be excited and/or sensed electrically. A general MEMS model can be decomposed into three parts as shown in Fig. 1.1.1(a). The actuation converts the input

voltage into a force (G_f), the mechanical resonator creates a mechanical displacement of the vibrating mass from the applied force (H_{mec}) and finally, the detection converts the motion into an electrical signal (G_x). For system-level analyses, the actuation and detection part can be treated as linear transduction gains, and their nonlinearity can be summed up into a nonlinear spring coefficient [22].

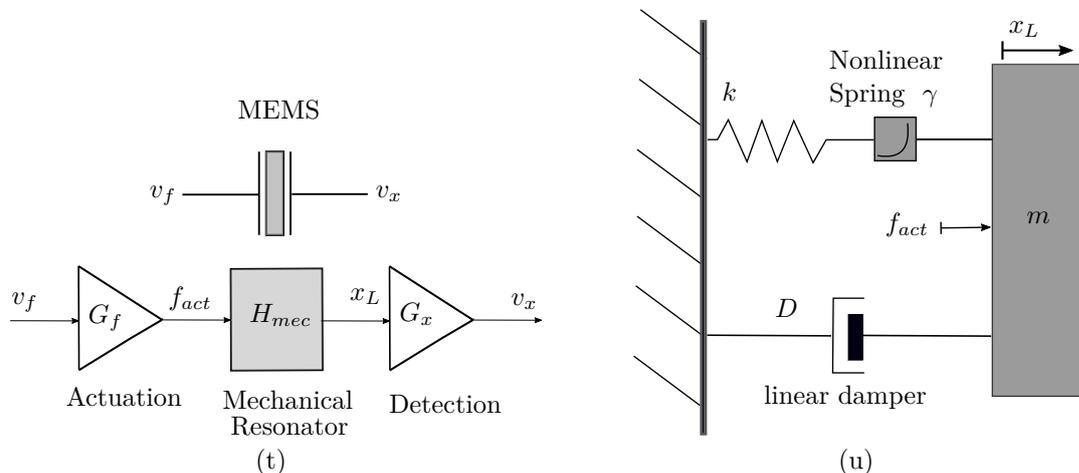


Figure 1.1.1 : MEMS (a) general model, (b) mechanical part model

The simplest MEMS model consists of a mass m , fixed to a frame by a mass-less spring of stiffness k , and damper with coefficient D . The forces acting on the mass are the restoring force f_{spring} and the damping force f_{damp} , the driving force f_{act} , generated by the actuator, and a thermomechanical stochastic force n_{mec} .

Letting x_L denote the position of the mass with respect to its equilibrium position (see Fig. 1.1.1(b) for details), τ denote time, and assuming the spring and damper are linear, we have $f_{spring} = kx_L$ and $f_{damp} = D \cdot dx_L/d\tau$. Under the assumption of linear damping, thermomechanical force n_{mec} has a white spectrum, with density $= 4kTD$. It is commonly admitted [23] that spring nonlinearity defines the ultimate performance that can be achieved with conventional resonant sensors (this will be illustrated in subsec. 1.2.1). To account for this phenomenon, we introduce a simple nonlinear spring model with a cubic restoring force (Duffing model). In this model, one may write $f_{spring} = kx_L(1 + \gamma x_L^2)$, where coefficient γ may either be positive (hardening behavior) or negative (softening behavior), depending on the dominant cause of nonlinearity [22].

Applying Newton's second law and replacing all forces by the expressions derived above, the equation governing the motion of the resonator is:

$$-D \frac{dx_L}{d\tau} - kx_L(1 + \gamma x_L^2) + f_{act}(\tau) + n_{mec}(\tau) = m \frac{d^2 x_L}{d\tau^2}. \quad (1.1.1)$$

Equation (1.1.1) can be written as,

$$\frac{d^2 x_L}{d\tau^2} + 2\zeta\omega_0 \frac{dx_L}{d\tau} + \omega_0^2 x_L (1 + \gamma x_L^2) = \frac{1}{m} (f_{act}(\tau) + n_{mec}(\tau)), \quad (1.1.2)$$

where $\omega_0 = \sqrt{\frac{k}{m}}$ is the MEMS natural pulsation and $\zeta = \frac{D}{2\omega_0 m}$ is the damping ratio of the resonator. Finally, the dimensionless equation governing the nonlinear resonator can be written as,

$$\frac{d^2 x}{dt^2} + \frac{1}{Q} \frac{dx}{dt} + x(1 + \gamma x^2) = f(t) + n(t) \quad (1.1.3)$$

where $t = \omega_0 \tau$, $x = x_L/L$, $f(t) = f_{act}(\tau)/\omega_0^2 m L$ and $n(t) = n_{mec}(\tau)/\omega_0^2 m L$ are dimensionless quantities represent respectively the normalized: time, motion amplitude, actuation, and thermomechanical force. L is a characteristic dimension of the device (typically the electrostatic gap for electrostatic resonators) and $Q = 1/2\zeta$ is the quality factor of the resonator. The resonant frequency and the quality factor can be determined with respect to the behavior of a linear noiseless resonator ($\gamma = 0, n(t) = 0$) [22]. In this case (1.1.3) can be simplified to,

$$\frac{d^2 x}{dt^2} + \frac{1}{Q} \frac{dx}{dt} + x = f(t). \quad (1.1.4)$$

The transfer function in terms of gain and phase describing the behavior of this system is then (1.1.5):

$$|H_{mec}(j\Omega)| = \frac{1}{\sqrt{\frac{\Omega^2}{Q^2} + (1 - \Omega^2)^2}} \quad (1.1.5a)$$

$$\angle H_{mec}(j\Omega) = \theta(\Omega) = \arctan \left[\frac{(1 - \Omega^2)}{\frac{\Omega}{Q}} \right] - \frac{\pi}{2} \quad (1.1.5b)$$

where Ω is the normalized pulsation ($\Omega = \omega/\omega_0$). The plots of this transfer function are depicted in Fig.1.1.2 for Q equal 20, 40 and 60 respectively.

The resonance pulsation $\Omega_r = \omega_r/\omega_0$ of the oscillator corresponds to the maximum of the gain curve, from (1.1.5a) we find,

$$\Omega_r = \sqrt{1 - \frac{1}{2Q^2}}, \quad (1.1.6)$$

which for $Q \gg 1$ yields to $\omega_r \approx \omega_0$, $\theta_r \approx \theta_0 = \frac{\pi}{2}$ and $X_r \approx X_0 = QF$ respectively. Note that, Q is also the ratio of the resonance pulsation to the half-power or 3dB bandwidth ($\Delta\omega$) around the measured peak, i.e., $Q = \frac{\omega_r}{\Delta\omega}$. In many MEMS resonant sensors, the

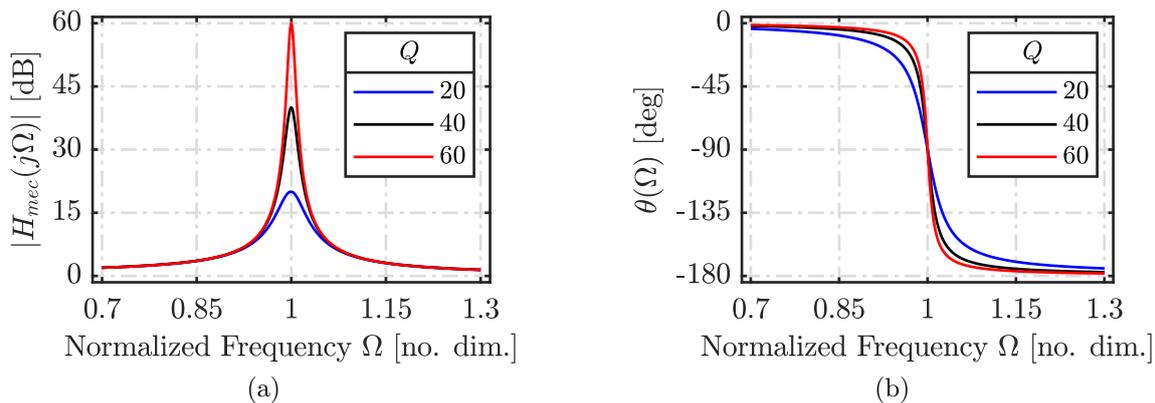


Figure 1.1.2 : Theoretical bode diagram of a linear MEMS resonator

quality factor is high ($Q > 500$), and the resonance frequency ($f_r \approx f_0$) is low (considering sensing applications), e.g., $f_0 < 1$ MHz. Hence, MEMS resonators are usually limited to narrow band applications, with a typical signal bandwidth (BW) much smaller than 2 kHz [2, 3].

1.2 Resonant MEMS architectures and sensing mode

Resonant sensors exploit the dependence of the stiffness or of the mass of the MEMS resonator to a physical quantity called the measurand. Few examples of MEMS measurands are: external acceleration or rotation [2, 5], added mass [4] and ambient pressure [3]. When the resonator is in a state of oscillation, close to its resonance frequency, stiffness or mass variations can be seen as changes of amplitude, phase or frequency of the measured output signal. Which of these output metrics is “the best” may change from one resonant sensor architecture to another. System-level analysis and performance comparison of different sensor architectures are presented in the following section, starting with architectures based on a single resonator [2, 3], then for architectures based on two weakly-coupled resonators (WCRs) [9, 15]. Each category is treated by first considering a perfectly linear resonator ($\gamma = 0$), then a nonlinear Duffing resonator ($\gamma \neq 0$).

In the rest of this document, we assume that one seeks to measure changes in the stiffness of the resonator, whose mass is supposed to be constant. A variation in stiffness will be denoted by the letter ϵ , e.g. $k \rightarrow k \times (1 + \epsilon)$

1.2.1 Resonant sensors based on a single resonator sensors

When a single resonator is used as a resonant sensor, two configurations are possible. In the Open-Loop (OL) sensing mode, the resonator is driven with a periodic signal close to its resonance frequency. Any change of ω_0 induced by the measurand can then be perceived

as a change of the phase of the resonator output signal (with respect to the drive signal) or of its amplitude. In the Closed-Loop (CL) sensing mode, the resonator is placed in an oscillator loop, imposing a specific phase between the resonator output signal and the drive signal; in this configuration, any change of ω_0 induced by the measurand can then be perceived as a change of the amplitude of the resonator output signal or of its oscillation frequency. Note that sensors with Frequency-Modulated FM or Phase-Modulated PM are "quasi-digital" because of they have duty-cycle or pulse-width-modulated outputs [8]. They can be directly interfacing with modern microcontrollers [24]. By contrast, sensors with Amplitude-Modulated AM outputs are usually "analog" and require an additional ADC for signal acquisition and post-processing. Sensors based on CL sensing mode with (quasi-digital) frequency readout are by far the most common in MEMS applications [2, 3, 24, 25, 26].

The equation governing a linear resonator subject to stiffness variation can be derived from (1.1.3) as,

$$\frac{d^2x}{dt^2} + \frac{1}{Q} \frac{dx}{dt} + x(1 + \epsilon) - f(t) = n(t). \quad (1.2.1)$$

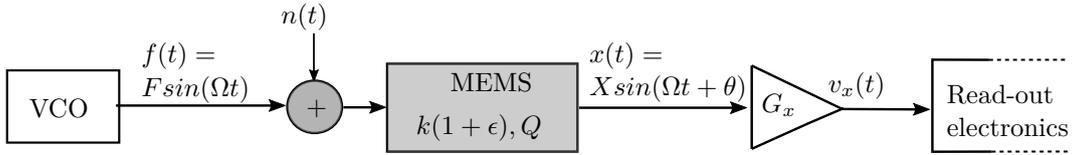


Figure 1.2.1 : General architecture of an open loop sensing mode

1.2.1.1 Open Loop sensing mode

The block diagram of OL resonant sensor architectures is shown in Fig. 1.2.1, where a Voltage-Controlled-Oscillator (VCO) is used to drive the resonator with a harmonic force $f(t) = F \sin(\Omega t)$. The $n(t)$ represents the fluctuating forces resulting from electronic equipment, i.e., VCO and thermomechanical noise. Provided, $Q \gg 1$, one may assume that the resonator response is harmonic, i.e. $x(t) = X \sin(\Omega t + \theta)$, where X is the motional amplitude and θ its phase with respect to f . In the absence of any stiffness perturbation ($\epsilon = 0$), if $\Omega_{VCO} \approx \Omega_0$ the applied signal lead the output signal by $\theta_0 \approx -\pi/2$ with amplitude of $X_0 \approx QF$. When $\epsilon \neq 0$, the transfer function of the resonator changes, leading to small variation (around the steady state value) in the phase ($\theta = \theta_0 + \delta\theta$) and in the amplitude ($X = X_0 + \delta X$) of the output signal [25]. Phase or amplitude modulation technique can then be performed to determine the quantities (δX or $\delta\theta$). In fact, by following the harmonic balance approach [27] and by projecting (1.2.1) on $\sin(\Omega t + \theta)$ and $\cos(\Omega t + \theta)$, the system state around the quasi-static limit is governed by the 2 set of equations below:

$$X(1 + \epsilon - \Omega^2) - F \cos(\theta) = N_{sin}, \quad (1.2.2a)$$

$$\Omega \frac{1}{Q} X - F \sin(\theta) = N_{cos}, \quad (1.2.2b)$$

where N_{cos} and N_{sin} are the noise components close to the carrier. The performance of this architecture (as a sensor) can then be determined by analyzing the sensitivity of its output metrics M (in the present case M may be θ or X) to mismatch ϵ , and its sensitivity to noise sources n . The sensitivity to mismatch,

$$S_M^\epsilon = \frac{1}{M_{ST}} \frac{\partial M}{\partial \epsilon} \Big|_{\epsilon=0}, \quad (1.2.3)$$

and the sensitivity to noise,

$$S_M^n = \frac{1}{M_{ST}} \frac{\partial M}{\partial n} = \frac{1}{M_{ST}} \sqrt{\left(\frac{\partial M}{\partial N_{sin}}\right)^2 + \left(\frac{\partial M}{\partial N_{cos}}\right)^2}; \quad (1.2.4)$$

where M_{ST} stands for the steady-state value of M in the noise-free, $\epsilon = 0$ case, can both be determined from (1.2.2) through straightforward differentiation. As in [13], we define the Figure-Of-Merit (FOM) of any output metric as the absolute value of the ratio of its sensitivity to mismatch over its sensitivity to noise,

$$FOM(M) = \left| \frac{S_M^\epsilon}{S_M^n} \right|. \quad (1.2.5)$$

This quantity should be maximized in order to improve sensor performance, i.e. sensitivity to ϵ and immunity from noise.

In the present architecture, the maximum sensitivity of the phase measurement can be found when working near the resonance ($\Omega_{VCO} = \Omega_0 = 1$), where $S_{\theta,max}^\epsilon \approx -\frac{1}{2} \frac{2Q}{\theta_{ST}} = \frac{2Q}{\pi}$. However, around Ω_0 , the sensitivity of the amplitude measurement is highly degraded as can be deduced from (8-b) ($S_X^\epsilon = \frac{\partial \theta}{\partial \epsilon} \cos(\theta_0) = 0$). These results can be observed from Fig. 1.1.2. At Ω_0 the slope variation of $\theta(\Omega)$ is maximal, but the slope of $X(\Omega)$ is 0. Nevertheless, S_X^ϵ can be optimized by operating at a frequency ($\Omega_{ST} \equiv \Omega_X$) relatively slightly larger or slightly smaller than Ω_0 , typically at $\Omega_X = \Omega_0(1 \pm 1/2Q)$. In this case S_X^ϵ reaches its maximum of $\mp Q/2$. However, this sensitivity is still lower than the obtained with phase measurement ($S_{\theta,max}^\epsilon \approx 4/\pi \times S_{\theta,max}^\epsilon Q$).

The sensitivity of either output metric to random fluctuations is found to be:

$$S_{\theta}^n(\Omega_0) \approx \frac{\sqrt{2}}{\pi/2} \frac{Q}{X_0}, \quad (1.2.6a)$$

$$S_X^n(\Omega_X > \Omega_0) \approx \frac{Q}{X_0}. \quad (1.2.6b)$$

Therefore the FOMs of the output metrics are as follows:

$$FOM(\theta) = \frac{X_0}{\sqrt{2}} \approx 0.71X_0, \quad (1.2.7a)$$

$$FOM(X) \approx X_0/2. \quad (1.2.7b)$$

The above expressions show that the FOMs of both metrics are almost the same and are linearly related with oscillation amplitude $X_0 = QF$. Thus, operating with a higher excitation force leads to a further performance improvement for the selected metric. It is worth recalling that X is an analog quantity while θ is quasi-digital. Thus, using the amplitude as output metric calls for additional read-out circuitry, such as demodulator, filter, and analog to digital converter ADC.

1.2.1.2 Closed Loop sensing mode

The Closed-Loop CL sensing mode consists of embedding the MEMS resonator in a loop, which sets the phase between $f(t)$ and $X(t)$ to a specific value, generally $\theta = \theta_0 = -\pi/2$. This purpose can be met by appropriate filtering of the detected signal, which is the so-called Self-Oscillating-Loop approach (SOL), as in [26]. There, the loop feedback is composed of an amplifier, a phase-shifter, a limiter, and both detection and actuation transducers (Fig. 1.2.2). Since the phase is set, the possible output metrics are X or Ω .

The performance of this system can be analyzed similarly to OL systems, as presented in the previous subsection. For $\theta = \theta_0$, the sensitivities to ϵ can be expressed as:

$$S_X^\epsilon = -\frac{1}{2}, \quad (1.2.8a)$$

$$S_\Omega^\epsilon = \frac{1}{2}; \quad (1.2.8b)$$

and the sensitivities to noise as:

$$S_X^n = \frac{X_0}{F} = Q, \quad (1.2.9a)$$

$$S_\Omega^n = \frac{1}{2X_0}. \quad (1.2.9b)$$

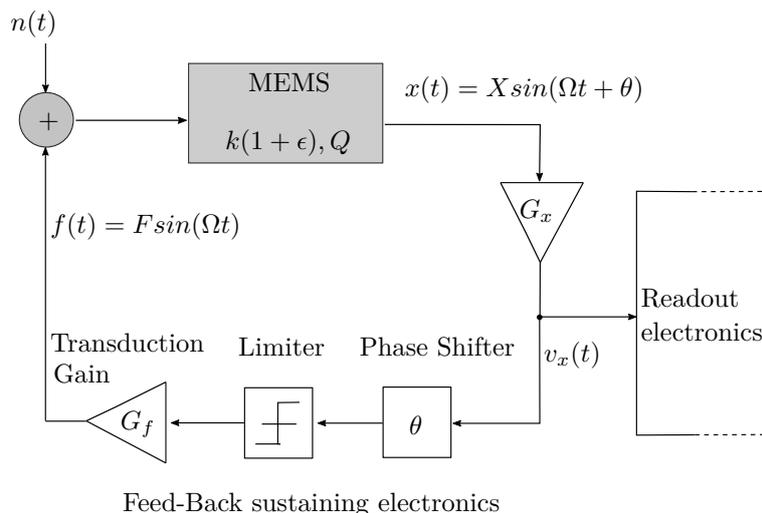


Figure 1.2.2 : General architecture of a closed loop sensing mode based Self-Oscillating-Loop (SOL)

Thus, the figures of merit become:

$$FOM(\Omega) = X_0 = QF, \quad (1.2.10a)$$

$$FOM(X) = 1/2Q. \quad (1.2.10b)$$

Hence, $FOM(X) \ll 1$, whereas $FOM(\Omega)$ can be "arbitrarily" large, depending on the magnitude of the driving force. This shows that, although X and Ω have the same sensitivity to mismatch (1.2.8), Ω is a distinctively better output metric. Moreover, Ω is a quasi-digital quantity, which can be easily digitized and analyzed. These distinctive advantages make frequency measurement the preferred output metric in CL sensing mode.

1.2.2 Duffing nonlinearity effect on single resonator sensors

According to the above results, the overall performance of an output metric can be improved by operating with a higher oscillation amplitude. However, above a given value of X known as critical (or Duffing) amplitude,

$$X_c = \frac{2}{3} \frac{1}{\sqrt{Q|\gamma|}}. \quad (1.2.11)$$

the nonlinear spring term (γx^2) appearing in (1.1.3) becomes remarkable, and the resonator response becomes nonlinear. Figure 1.2.3 shows the frequency-amplitude curves

to different actuation forces F (from $2 \cdot 10^{-4}$ to 10^{-3} shown in the color bar) of a system described with (1.1.3), for $\gamma = 10^{-2}$ and $Q = 10^3$.

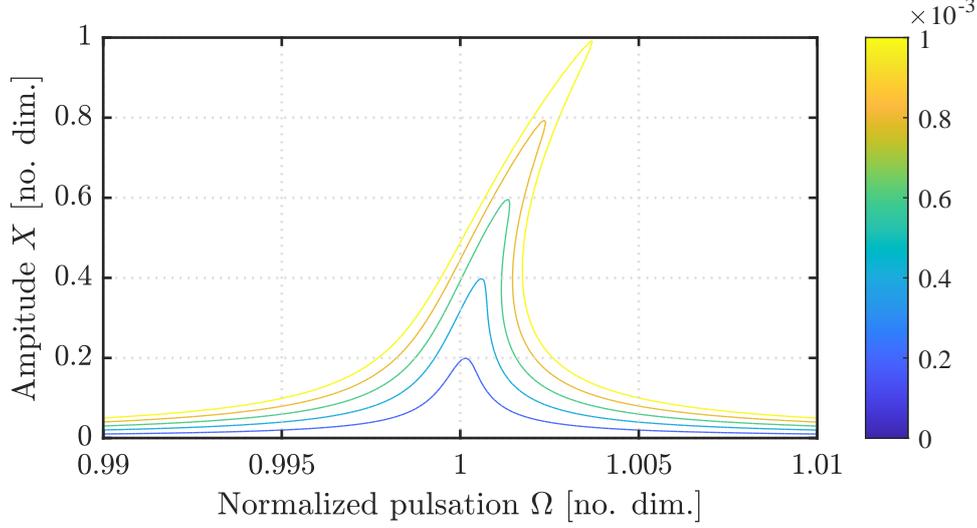


Figure 1.2.3 : Typical nonlinear frequency responses of a Duffing resonator for different actuation forces F (shown in the color bar), considering $Q = 10^3$ and $\gamma = 10^{-2}$

It can be seen that, as F increases, the curve is deformed but initially preserves its bijective character (for $\gamma > 0$, the maximum moves in the direction of $\Omega > 1$). When $F > F_c$, the frequency-amplitude response is multi-valued, meaning that, at a given frequency, the system may have several possible operating points (one to three possible amplitude steady-state solutions (Fig. 1.2.3)). In practice, the system selects based on its history one of these operating points, which gives rise to hysteresis profiles.

Based on these observations, in OL mode, a calibration step is first needed in order to define the steady-state of the system and track its resonance frequency. In addition, near the resonance, a small variation in ϵ risks of major instability due to the sudden break in the curve as shown from Fig. 1.2.3. To maintain good sensor functionality, it is important to always work in the linear regime.

However, these issues do not occur for the CL sensing mode since the system operates automatically at its resonant state [28]. Nonetheless, working with $X > X_c$ may not necessarily improve the performance of the sensor, it can be deteriorated. A further sensitivity analysis with more complex equations (including the Duffing term) is therefore performed (see appendix A). The FOM of each output metric is found as:

$$FOM(\Omega) = X_0 / \sqrt{1 + (X_0^2 / X_c^2)^2}, \quad (1.2.12a)$$

$$FOM(X) = 1/2Q. \quad (1.2.12b)$$

So that, as X_0 reaches the critical amplitude, $FOM(\Omega)$ is lowered by $\sqrt{2}$ compared

to the linear case. When $X_0 \gg X_c$, $FOM(\Omega)$ decreases with X_0 ($FOM(\Omega) \propto 1/X_0$). This dependence of the oscillation frequency to the oscillation amplitude is known as the A-f effect. The underlying result reveals that improving the frequency resolution, by operating beyond X_c , may not lead to a better Signal-to-Noise Ratio (SNR), as it has been recently shown in [29]. Note that $FOM(X)$ is the same as in the linear regime.

To conclude, nonlinearity makes open-loop sensors based on a single resonator impractical, and the A-f effect limits the use of closed-loop sensors. Thus, resonant sensors based on a single resonator should always work in the linear regime. This limitation is all the more stringent as Q is larger. However, this is not the case for WCRs, as it will be shown later in this chapter.

1.2.3 Open loop vs. closed loop

Besides the metric performance discussed in the above subsections, the limitations and imperfections of the electronic part are also a key factor for an optimum architecture. For instance, in OL sensing mode, noise and perturbations that come from the VCO are directly injected into the sensor. As a result, a variation in the driving frequency may change the system's operating point and, hence, degrading its performance. Besides, operating at a given frequency, the minimal step of frequency must be very narrow. This constraint becomes more challenging for a higher quality factor. Hence, a high precision VCO with typically higher resolution than the MEMS resonator is required. In CL, the distortions and nonlinearity in the feedback electronic can modify the noise sources' contribution, creating some frequency aliasing up-converts close to the oscillating frequency. This effect can be minimized by using a Phase-Locked-Loop (PLL) in the feedback [8]. Obviously, the PLL requires a VCO to work. However, it can be shown that near the carrier, the VCO's noise does not contribute to the MEMS oscillator's noise, unlike in the OL architectures. Thus, no need for high precision VCO. In addition, CL sensing mode does not require any frequency sweep to determine the resonance frequency, which is a major advantage in terms of sensor measurement time. According to the above analyses, it can be indicated that the ultimate performance of Ω in CL mode is slightly better than that of θ in OL mode ($FOM(\Omega) = \sqrt{2}FOM(\theta)$).

1.2.4 Discussion

Using devices modeled as single resonator sensors is sufficient for many applications. However, for high-end applications, these devices suffer from the intrinsic MEMS sensitivity to environmental conditions (temperature, humidity, pressure). The conventional solutions to this problem include temperature compensation [30, 31]. However, there is an issue with this solution: the temperature compensation electronics typically consume more power than the oscillator sustaining and readout electronics, which is less suitable for low power applications. Another solution is to compare the oscillation fre-

quency to a reference oscillator. If the reference oscillator has the same sensitivity to environmental conditions (thermal drift) as the one used for sensing, a differential measurement can be obtained. This approach has been successfully implemented in [32] and more recently in [33] for temperature compensation in accelerometers. However, parasitic couplings between the oscillators are inevitable, resulting in unwanted signal injection and frequency pulling or locking [34]. Using resonators with different natural frequencies may overcome this issue but at the cost of system complexity and additional calibration steps [35]. Alternatively, one may seek to enforce a weak coupling of the resonators, taking advantage of the parametric sensitivity of the synchronized state to perform a differential drift-free sensing. Several solutions for enforcing coupling between two (or more) resonators have been studied in the MEMS literature. Few published examples are "active" coupling through mutual-injection [9, 11, 36] or "passive" coupling through mode-localization [15, 4, 37]. The performance metrics of these architectures are given in the following subsection. We will see that, as opposed to the conventional resonant sensors based on a single-resonator, resonant sensors based on coupled resonators are not limited by the A-f effect provided amplitude-ratio, which is used as an output metric instead of frequency or phase-difference.

1.2.5 Resonant sensors based on weakly-coupled resonators

We restrict our study to closed-loop Weakly-Coupled-Resonators (WCRs) based on two resonators with nominally identical natural pulsations and quality factors. The resonators are coupled in a way that there is a force acting on one of the resonators, which depends on the state of the other resonator. Depending on the coupling mechanism and on the driving scheme, the resonators may synchronize and oscillate at the same frequency. This synchronized state can be engineered to be highly sensitive to stiffness mismatch ϵ between the resonators. In particular, the phase difference between the two synchronized resonators or the ratio of their oscillation amplitudes provides high-sensitivity measurements of ϵ , and passive immunity to environmental fluctuations. A simplified schematic of two coupled resonators is illustrated in Fig. 1.2.4.

Under the hypothesis that both resonators operate in the linear regime, the system can be described by the following set of dimensionless equations:

$$\frac{d^2x}{dt^2} + \frac{1}{Q} \frac{dx}{dt} + x(1 + \epsilon) - f_x \left(x, \frac{dx}{dt}, y, \frac{dy}{dt} \right) = n_x(t), \quad (1.2.13a)$$

$$\frac{d^2y}{dt^2} + \frac{1}{Q} \frac{dy}{dt} + y(1 - \epsilon) - f_y \left(x, \frac{dx}{dt}, y, \frac{dy}{dt} \right) = n_y(t), \quad (1.2.13b)$$

where the perturbations n_x and n_y are assumed to be independent, with equal magnitudes, and f_x and f_y are the forces used for driving the resonators and coupling them. Since

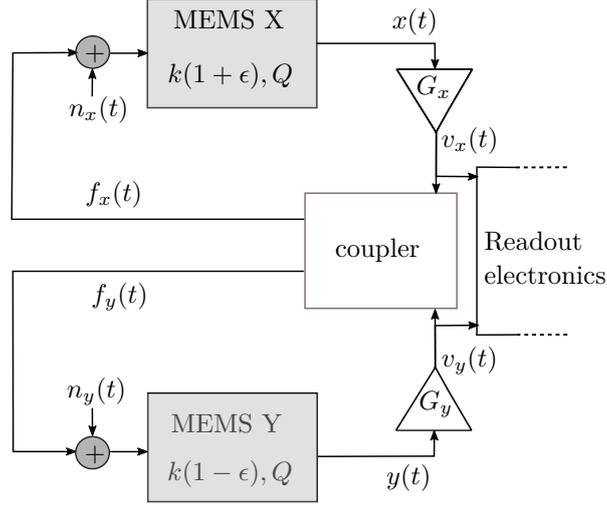


Figure 1.2.4 : Block diagram of two MEMS resonators coupled through their actuation force for a differential sensing of a stiffness mismatch ϵ

ϵ is differentially introduced in the resonators, the average resonance frequency of the system does not deviate much from Ω_0 , so that one may set $\Omega \approx \Omega_0 = 1$. The system is then governed by a set of 3 dimensionless equations governing the state of the system (amplitudes X and Y , and phase ϕ) [13]:

$$\frac{X}{2Q} - \frac{1}{2}F_{\cos x} = \frac{1}{2}N_{\cos x}, \quad (1.2.14a)$$

$$\frac{Y}{2Q} - \frac{1}{2}F_{\cos y} = \frac{1}{2}N_{\cos y}, \quad (1.2.14b)$$

$$\epsilon - \frac{1}{2} \left(\frac{F_{\sin x}}{X} - \frac{F_{\sin y}}{Y} \right) = \frac{1}{2} \left(\frac{N_{\sin x}}{X} - \frac{N_{\sin y}}{Y} \right), \quad (1.2.14c)$$

where $\phi = \theta_y - \theta_x$ is the phase difference between the driving forces f_y and f_x . Note that no particular assumption concerning the nature of the coupling is made in (1.2.14), so that, this model may be used to study WCRs indifferently with active coupling (MILOs for Mutually-Injection-Locked-Oscillators) or with passive coupling (MOLOs for Mode-Localized-Oscillators), the only difference is the expression of the driving/coupling forces $F_{\sin x, y}$ and $F_{\cos x, y}$.

In the following sub-section, the MILO architectures for which both the phase-difference $\phi = \theta_y - \theta_x$ and the amplitude-ratio $R = X/Y$ can be used as output metrics are studied. The case of closed-loop MOLO architectures, for which the amplitude ratio is the output metric of choice, is also considered. For further detailed information on these architectures, the interested reader can refer to [13].

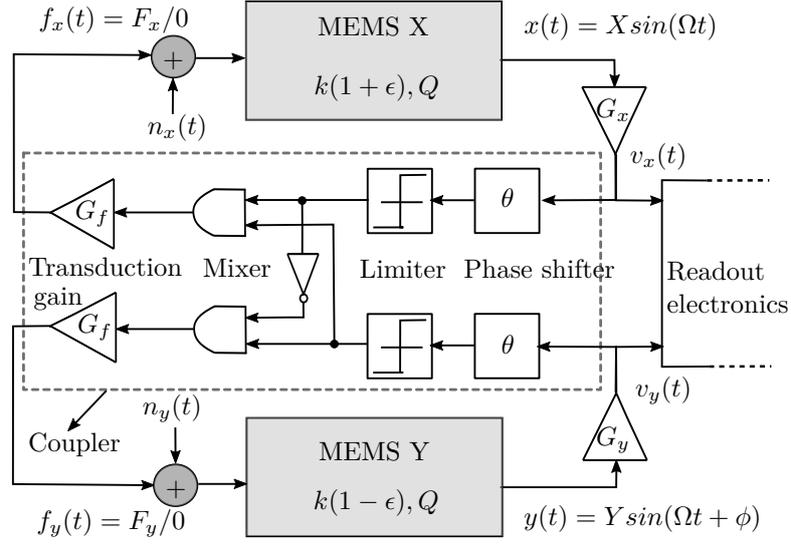


Figure 1.2.5 : System-level view of a MILO based on a digital mixer

1.2.5.1 Resonant sensors based on mutually-injection-locked oscillators

Using MILOs for resonant sensing was first proposed in [36]. In the most studied MILO architectures, the coupler consists of a nonlinear digital mixer that produces binary-valued driving forces that are independent of the motional signal amplitudes. The quadrature and in-phase components of the driving forces depend on the delay of each feedback loop θ (Fig. 1.2.5) and on the phase difference ϕ . These can be written as [13]:

$$F_{\sin x} = \frac{F}{\pi} (\cos\theta + \cos(\theta + \phi)), \quad (1.2.15a)$$

$$F_{\cos x} = \frac{F}{\pi} (\sin\theta + \sin(\theta + \phi)), \quad (1.2.15b)$$

$$F_{\sin y} = \frac{F}{\pi} (\cos\theta - \cos(\theta - \phi)), \quad (1.2.15c)$$

$$F_{\cos y} = \frac{F}{\pi} (\sin\theta - \sin(\theta - \phi)). \quad (1.2.15d)$$

When $\theta = 90^\circ$ and $\epsilon = 0$, there are two possible synchronized oscillation states, with $\phi_{ST} = \pm 90^\circ$ and $X_{ST} = Y_{ST} = X_0$. Following the same approach as in the previous subsection, the sensitivities to mismatch for R and ϕ are found as:

$$S_R^\epsilon = \pm 2Q, \quad (1.2.16a)$$

$$S_\phi^\epsilon = \mp \frac{2Q}{\pi}, \quad (1.2.16b)$$

and the sensitivities to noise as:

$$S_R^n = \sqrt{2} \frac{Q}{X_0}, \quad (1.2.17a)$$

$$S_\phi^n = \frac{2Q}{\pi X_0}, \quad (1.2.17b)$$

consequently, one may obtain:

$$FOM(R) = \sqrt{2} X_0, \quad (1.2.18a)$$

$$FOM(\phi) = X_0. \quad (1.2.18b)$$

For the aforementioned architecture, R is a better output metric than ϕ , although ϕ may be preferred because of its quasi-digital nature. A better performance of ϕ can be obtained by setting $\theta = \pi/2 \pm \pi/4$, in which case $FOM(R) = X_0$ and $FOM(\phi) = \sqrt{2}X_0$. This configuration is extensively reviewed in [20]. The best compromise in terms of sensitivity and resolution is obtained with R , when $\theta = \pi/2$, or with ϕ when $\theta = \pi/2 \pm \pi/4$. These results make sense since the coupled system is twice as dependent on ϵ as the single resonator system (ϵ appears in (1.2.13a) and in (1.2.13b)), but also has twice as many (independent) noise sources. Hence, one may expect at best a $\sqrt{2}$ improvement in the FOMs of the coupled system with respect to the single resonator system. In fact, one may formally prove that R , when $\theta = \pi/2$, or ϕ , when $\theta = \pi/2 \pm \pi/4$, are optimal in the sense that there exists no other output metric with a larger FOM for a given value of X_0 .

1.2.5.2 Resonant sensors based on mode-localization oscillators

MEMS WCRs using mode localization, originally derived in [4], are based on two electrostatically-coupled or mechanically-coupled resonators. A functional representation of a closed-loop of MOLO whose architecture is similar to the one in [15] is shown in Fig. 1.2.6. The gain κ denotes the relative coupling strength (i.e., the ratio of the coupling stiffness to the nominal stiffness k) through which the resonators are coupled. The limiter and the phase shifter ensure that the Barkhausen criterion is met in both loops, and the two resonators oscillate at Ω_0 , with the same amplitude ($X_{ST} = Y_{ST}$) provided $\epsilon = 0$. Two oscillation states are possible, being $\sin(\phi_{ST}) \approx \pm 1/Q\kappa \ll 1$ or $\cos(\phi_{ST}) \approx \pm 1$. A small variation of ϵ results in a large change of the oscillation amplitudes and a little variation in their phase difference [13]. Thus, only the amplitude ratio R is ever considered as an output metric for such sensors.

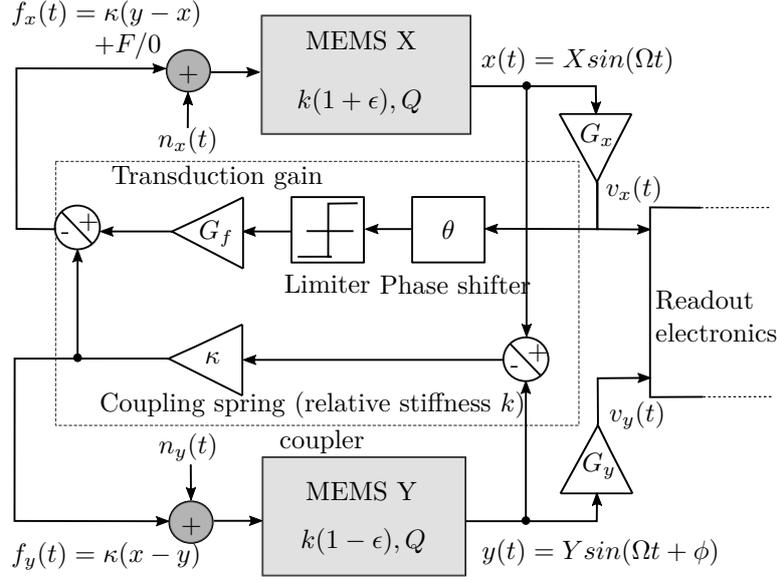


Figure 1.2.6 : System-level view of a mode-localized oscillators

For $\theta = -\theta_0 = \pi/2$, the driving and coupling terms appearing in (1.2.14) are:

$$F_{\sin x} = -\kappa X + \kappa Y \cos(\phi), \quad (1.2.19a)$$

$$F_{\cos x} = \frac{F}{\pi} - \kappa Y \sin(\phi), \quad (1.2.19b)$$

$$F_{\sin y} = -\kappa Y + \kappa X \cos(\phi), \quad (1.2.19c)$$

$$F_{\cos y} = \kappa X \sin(\phi), \quad (1.2.19d)$$

As a result, one may find from (1.2.14a) and (1.2.14b)

$$S_R^c \approx \mp \frac{1}{\kappa} \text{ (a)}, \quad S_R^n = \frac{1}{\kappa \sqrt{2} X_0} \text{ (b)} \text{ and consequently } FOM(R) = \sqrt{2} X_0 \text{ (c)} \quad (1.2.20)$$

It is notable that $FOM(R)$ is the same in the case of MOLOs and in the case of MILOs (with $\theta = \pi/2$), meaning that R is an optimal output metric in either case. To complete the parallel with MILOs, the performance of R and ϕ might still be enhanced by choosing different phase loop delay, as in MILOs. A more complete study of MOLO architectures should take this into account.

1.2.6 Duffing nonlinearity effect on sensors based on weakly coupled resonators

The performance of WCRs at large oscillating amplitudes can be studied by including the Duffing term (γ) in (1.2.13), and following the sensitivity analysis technique developed in appendix A. In the case of the MILO architecture with $\theta = \pi/2$, the sensitivities to mismatch (near $\epsilon = 0$) are found as:

$$S_R^\epsilon = -Q \left(\frac{2}{X_0^2/X_{cMILO}^2 \mp 1} \right), \quad (1.2.21a)$$

$$S_\phi^\epsilon = \mp \frac{S_R^\epsilon}{\pi}, \quad (1.2.21b)$$

and the sensitivities to noise as:

$$S_R^n = \frac{|S_R^\epsilon|}{\sqrt{2}X_0}, \quad (1.2.22a)$$

$$S_\phi^n = \frac{|S_\phi^\epsilon|}{\sqrt{2}X_0} \times \sqrt{1 + [X_0^2/X_{cMILO}^2 \mp 1]^2}. \quad (1.2.22b)$$

Consequently, one may obtain:

$$FOM(R) = \sqrt{2}X_0, \quad (1.2.23a)$$

$$FOM(\phi) = \frac{FOM(R)}{\sqrt{1 + [X_0^2/X_{cMILO}^2 \mp 1]^2}}. \quad (1.2.23b)$$

Beyond the critical amplitude $X_{cMILO} = \sqrt{(2/3)|\gamma|Q}$ (which is larger than that of a single resonator), the sensitivity to mismatch of both R and ϕ decreases as $1/X_0^2$ (1.2.21). This decrease of sensitivity is accompanied by an increase of the MILO's locking range [19]. Furthermore, as shown by (1.2.22), the sensitivity to noise of R then decreases as $1/X_0^3$, whereas the sensitivity of ϕ decreases as $1/X_0^2$. This occurs in a consequence of the nonlinear coupling term appearing in the square root on the (1.2.22b). Hence, $FOM(\phi)$ decreases linearly with the amplitude of the drive, whereas $FOM(R)$ keeps increasing. This behavior is also observed for other MILO topologies (e.g., for $\theta = \pi/2 \pm \pi/4$) and validated experimentally [12].

As far as the MOLO architecture with $\theta = \pi/2$ is concerned, in the nonlinear regime (1.2.20) becomes:

$$S_R^\epsilon \approx -\frac{1}{\kappa} \left(\frac{1}{X_0^2/X_{cMOLO}^2 \pm 1} \right) \text{ (a), } S_R^n = \frac{|S_R^\epsilon|}{\sqrt{2}X_0} \text{ (b) and } FOM(R) = \sqrt{2}X_0 \text{ (c)} \quad (1.2.24)$$

where

$$X_{cMOLO} = \sqrt{\frac{4\kappa}{3|\gamma|}} \quad (1.2.25)$$

is the critical amplitude that marks the onset of nonlinearity. The fact that this critical amplitude is different from the single resonator case and from the MILO case is one of the contributions of one of our papers [13], where theoretical properties of nonlinear WCRs are studied at length. Thus, regarding the amplitude ratio output metric, the same qualitative behavior is observed for MOLOs and MILOs, the only difference being the definition of the critical amplitude. A more complete study of nonlinear properties of WCRs can be found in [13].

1.3 Global comparison

1.3.1 Optimum output metric in the linear oscillation regime

The parametric sensitivities and FOMs obtained close to $\epsilon = 0$ are listed in Table 1.1, considering all architectures in the linear and nonlinear oscillation regimes. In the linear regime, regardless of the output metric, all sensitivities to noise decrease as $1/X_0$, while sensitivities to mismatch are independent of X_0 . Consequently, the *FOM* of any output metric increases as X_0 , with the expected $\sqrt{2}$ maximum improvement for architectures based on 2 resonators. This is hardly a surprise, but this result corrects a misconception that the ultimate resolution (i.e. the theoretical resolution of a sensor, taking into account thermomechanical noise only) WCRs may be improved by decreasing the coupling stiffness κ [37]. Arguably, the best trade-off between metric performance and readout complexity can be obtained with ϕ in MILO for $\theta = \pi/2 \pm \pi/4$, which has the best FOM and is quasi-digital. Note that sensitivity to ϵ is used as a figure-of-merit by many authors [15, 4, 25], which makes sense when measurement noise is dominant over thermomechanical noise. However, one should be careful in that case to only compare output metrics with the same readout requirements, so that measurement noise can be compared from one architecture to the next. For example, it is often read that amplitude ratio in MOLOs is $1/\kappa$ more sensitive to ϵ than conventional closed-loop frequency measurements. However, this comparison makes little sense as the readout associated with frequency measurements and amplitude measurements are very different. Indeed, they are not likely to have the same measurement noise. Furthermore, a trade-off must always be made between sensitivity and dynamic range: for example, MILOs have the best sensitivity to mismatch among amplitude or amplitude ratio-modulated architectures, but they also have the narrowest Locking-Range (*LR*) and the smallest dynamic range.

Table 1.1 : The parametric sensitivities and FOMs obtained close to $\epsilon = 0$, for all architectures in the linear and nonlinear oscillation regimes.

Sensor Topology	Single resonator			Weakly coupled resonators						
	OL			CL			MILO			MOLO
	$\Omega_{VCO} = \Omega_0$	$\Omega_{VCO} = \Omega_X$	$\Omega_{VCO} = \Omega_X$	$\theta = \frac{\pi}{2}$	$\theta = \frac{\pi}{2}$	$\theta = \frac{\pi}{2}$	$\theta = \frac{\pi}{2} \pm \frac{\pi}{4}$	$\theta = \frac{\pi}{2}$	$\theta = \frac{\pi}{2} \pm \frac{\pi}{4}$	$Q\kappa \gg 1, \theta = \frac{\pi}{2}$
Output metric	θ	X	X	Ω	ϕ	R	ϕ	R	R	R
S_M^ϵ	$\frac{2Q}{\pi}$	$\frac{Q}{2}$	$\frac{Q}{2}$	$\frac{1}{2}$	$\frac{\pm 2Q}{\pi}$	$\pm 2Q$	$\frac{\pm 4Q}{\pi}$	$\pm 2Q$	$\pm 2Q$	$\mp \frac{1}{\kappa}$
S_M^n	$\frac{2\sqrt{2}Q}{\pi X_0}$	$\frac{Q}{X_0}$	$\frac{Q}{X_0}$	$\frac{1}{2X_0}$	$\frac{2Q}{\pi X_0}$	$\frac{\sqrt{2}Q}{X_0}$	$\frac{2\sqrt{2}Q}{\pi X_0}$	$\frac{2Q}{X_0}$	$\frac{2Q}{X_0}$	$\frac{1}{\kappa\sqrt{2}X_0}$
$FOM(M)$	$\frac{X_0}{\sqrt{2}}$	$\frac{X_0}{2}$	$\frac{X_0}{2}$	X_0	X_0	$\sqrt{2}X_0$	$\sqrt{2}X_0$	X_0	X_0	$\sqrt{2}X_0$
Nonlinear										
S_M^ϵ	—	—	—	$\frac{4}{9\gamma X_0^2}$	$\frac{4}{3\pi\gamma X_0^2}$	$\frac{-4}{3\gamma X_0^2}$	$\frac{8}{3\pi\gamma X_0^2}$	$\frac{-4}{3\pi\gamma X_0^2}$	$\frac{-4}{3\pi\gamma X_0^2}$	$\frac{-4}{3\pi\gamma X_0^2}$
S_M^n	—	—	—	$\frac{1}{QX}$	$\frac{\sqrt{2}Q}{\pi X_0}$	$\frac{2\sqrt{2}}{3 \gamma X_0^3}$	$\frac{2Q}{\pi X_0}$	$\frac{4}{3 \gamma X_0^3}$	$\frac{4}{3 \gamma X_0^3}$	$\frac{2\sqrt{2}}{3 \gamma X_0^3}$
$FOM(M)$	—	—	—	$\frac{4}{9 \gamma X_0}$	$\frac{2\sqrt{2}}{3 \gamma QX_0}$	$\sqrt{2}X_0$	$\frac{4}{3 \gamma QX_0}$	X_0	X_0	$\sqrt{2}X_0$
X_c	—	—	—	$\frac{2}{3} \frac{1}{\sqrt{Q \gamma }}$	$\sqrt{\frac{2}{3} \frac{1}{Q \gamma }}$					

1.3.2 Optimum output metric in the nonlinear oscillation regime

Above X_c , the sensitivity to mismatch of all architectures decreases as $1/X_0^2$, the sensitivity to noise of R decreases as $1/X_0^3$; while that of ϕ and Ω decreases as $1/X_0$, because of the A-f effect. Consequently, the *FOM* of ϕ and Ω start decreasing with X_0 , whereas that of R keeps increasing linearly with X_0 regardless of which architecture is considered. Moreover, above the critical amplitude, the sensitivity to mismatch of R no longer depends on κ (in MOLOs) or on Q (in MILOs). Thus, sensitivity may be controlled electrically by adjusting the amplitude of the excitation force, rather than being controlled mechanically as in the linear regime. Another positive trade-off that is the decrease in the sensitivity and the increase of the sensor dynamic range, as illustrated in [19]. These interesting properties of the ratio-metric WCRs may also apply to mode-matched MEMS gyroscopes for which the amplitude variation between two resonators coupled through the Coriolis force is the metric of choice.

1.3.3 Conclusion

These results seem to open the way for interesting new paradigms of resonant sensors, whose performance is not limited by nonlinear phenomena, and motivates our research for an efficient solution of converting the amplitude ratio, an analog quantity, into the digital domain.

While R is an intrinsically differential output metric, it is also an intrinsically nonlinear function of ϵ for all WCR architectures. Thus, the sensitivity of R to ϵ is not uniform across the sensor dynamic range, and this makes impractical the use of an ADC with uniform quantization levels. In the following section, we propose an alternative ratiometric output with the same “nice” properties as R , but which has improved linearity, and is more suitable for integrated implementation.

1.4 Bilinear amplitude-atrio output metric

The Bilinear amplitude-ratio (B) was initially proposed in [38], in a different context and is expressed as:

$$B = \frac{X - Y}{X + Y} = \frac{R - 1}{R + 1}. \quad (1.4.1)$$

Like R , B is an intrinsically differential output metric. Straightforward analysis shows that, close to $\epsilon = 0$, B has the same performance (sensitivity/resolution) as R even in the large oscillation operating regime. However, several other properties make it more interesting. First of all, R may vary between 0 and infinity, whereas B is bounded between

-1 and 1. Moreover, for the most common ratio-metric WCRs architectures, B is odd, whereas R is not. Thus, the bilinear amplitude ratio is “better-behaved” than the classical amplitude ratio.

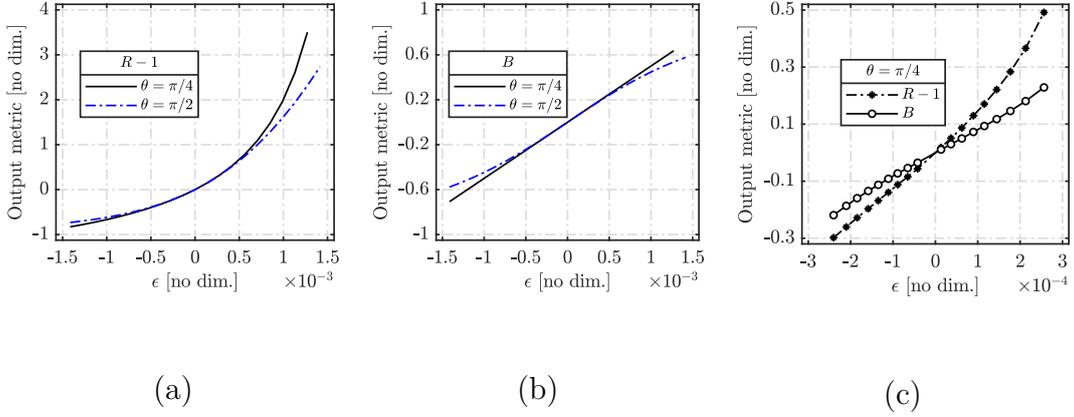


Figure 1.4.1 : Comparison of, (a) $R(\epsilon)$, and (b) $B(\epsilon)$, for two simulated MILO architectures with $\theta = \pi/4$ and $\theta = \pi/2$, (c) measured MILO architecture with $\theta = \pi/4$

To highlight these points, we plot $R(\epsilon)$ and $B(\epsilon)$ in Fig. 1.4.1(a) and Fig. 1.4.1(b) for two MILO architectures, with two identical resonators. It is apparent that B has also a much better linearity than R across the whole dynamic range. In fact, for the $\theta = \pi/4$ architecture, we have precisely,

$$B(\epsilon) = Q\epsilon, \quad (1.4.2)$$

i.e., the bilinear amplitude ratio is a perfectly linear output metric. In the case of the $\theta = \pi/2$ architecture, we have,

$$B(\epsilon) = Q\epsilon/\sqrt{1 + (Q\epsilon)^2}, \quad (1.4.3)$$

so that only second-order nonlinearity errors are present. Experimental measurements indicate that this improvement is quite robust to several non-idealities, such as those resulting from fabrication dispersions between the resonators or intrinsic resonator non-linearity [18], as shown in Fig. 1.4.1(c). The main drawback of B compared to R is the need for extra analog blocks (i.e., adder and subtractor). However, as will be shown in chapter 3, B presents interesting advantages to analog-to-digital conversion. In the following section, we review different alternatives to digitize the bilinear amplitude ratio.

1.5 Literature on the analog to digital ratiometric interface

1.5.1 Readout interface requirements

As can be seen from Fig.1.2.6 for MILO architecture, the amplifiers $G_{x,y}$ are common blocks between the sustaining electronics (detecting part) and the readout interface (acquisition part). These blocks represent the major sources of drift [14] and “intrinsic” noise in the system [9] [15]. They limit the resolution in both: the detection part and the acquisition part. However, the bilinear nature of the amplitude ratio may significantly suppress the existing temperature drift as described in [38]. Moreover, above the critical amplitude, the sensitivity to “intrinsic” noise of the amplitude ratio decreases as $1/X_0^3$ (1.2.22a), thereby the noise contribution of these stages can be highly minimized. The ultimate resolution of the sensor is then restricted by the remaining part of the readout interface [12], i.e., ADC. Consequently, this interface must have a higher Dynamic-Range (DR) than the sensor can provide. In fact, in MILO architecture, the locking-range LR for which the system remains in its locked state [19] is found $LR(B) = \left(\frac{X-Y}{X+Y}\right) |_{max} \approx \pm 0.57$, thus one may ensure $DR \geq LR$. Moreover, the desired interface must be temperature-aware designed to preserve the drift rejection capability of the differential detection. It takes $x(t)$ and $y(t)$, whose frequency may up to some MHz as inputs, and perfumes a digital representation of the quantity B as an output. According to the industrial products available for automotive application, a high-resolution sensor has from 14 to 16 bits, within a temperature range $-40 < T < 125^\circ \text{C}$ [39, 40, 41, 42]. Table 1.2 summaries the required specifications of the analog-to-digital ratiometric readout interface.

Table 1.2 : Readout interface requirements

integration-compatible	CMOS-MEMS
Resolution	≥ 16 bits
Input signal frequency	$0.1 \leq f_0[\text{MHz}] \leq 1$
Input signal bandwidth	$BW \leq 2$ kHz
Dynamic range	≥ 0.57
Temperature range	$-40 \leq T[^\circ\text{C}] \leq 125$

1.5.2 One step approach

The most common approach to determine the bilinear quantity is to digitize the motional signals (at a sampling frequency much greater than the oscillation frequency) and perform demodulation and division in the digital domain [38](Fig. 1.5.1). This approach is less

sensitive to low-frequency noise, such as flicker noise. However, this it is not very amenable to integration, as it requires two high-resolution, high sampling frequency ADCs. In addition, the two ADCs should be perfectly matched, which is not a trivial task, whether they operate at a large or a small sampling frequency.

1.5.3 Two steps approach

The two step approach consists first to perform demodulation in the analog domain. Thus, it is possible to determine B before digitizing the signals. This approach requires an adder, a subtractor, an analog Voltage-Divider (VD), and ADC to digitize the results (Fig. 1.5.1). Performing the demodulation in the analog domain considerably relaxes the constraints on the sampling frequency of the ADC(s). Here, the resolution and the complexity is strictly limited by the VD [43, 44]. In fact, the common way to implement a VD is the log-antilog network configuration [43], where the division is performed using three diode-connected transistors. However, the emitter saturation current varies significantly from one transistor to another and with temperature. An alternative method is presented in [44], where the VD is implemented by a two-quadrant multiplier using only amplifiers and resistors. A relatively high resolution can be achieved at the cost of increasing complexity and power consumption. Finally, it is possible to perform the division and the analog-to-digital conversion in a single step, as first described in [45]. In fact, the ratio of the demodulated amplitude signals can be performed by using one signal (i.e., $V_x - V_y$) as the input of an ADC, and the other signal (i.e., $V_x + V_y$) as a reference voltage. This ADC is synchronized by the oscillator output signal to minimize the leftover harmonics from the demodulation and filtering operations. The great benefit of this solution is that one ADC is omitted. Furthermore, the inherent ratio-metric conversion scheme eliminates the need for an additional VD circuit before the ADC. Besides, replacing the reference voltage with the alternative quantity $V_x + V_y$ avoids the need of external stable voltage, thus resulting in a compact circuit and a considerable reduction in power consumption. However, this approach is more sensitive to flicker noise compared to one step approach since the signals are treated at near DC frequency bandwidth. This issue can generally be mitigated using correlated double sampling or chopper stabilization techniques [46].

1.5.4 ADC as voltage divider

Considering the required resolution (16 bits) and for bandwidth (< 2 kHz), two types of ADCs are identified which could be used: dual-slope ADCs and $\Sigma\Delta$ -ADCs as depicted in Fig. 1.5.2. Dual slope ADCs operate in two phases, the charge phase during a predetermined amount of time (T_{charge}) and the discharge phase for a time lesser or equal to T_{charge} . The resolution in term of Effective-Number-Of-Bits ($ENOB$) of such devices can be expressed as [47],

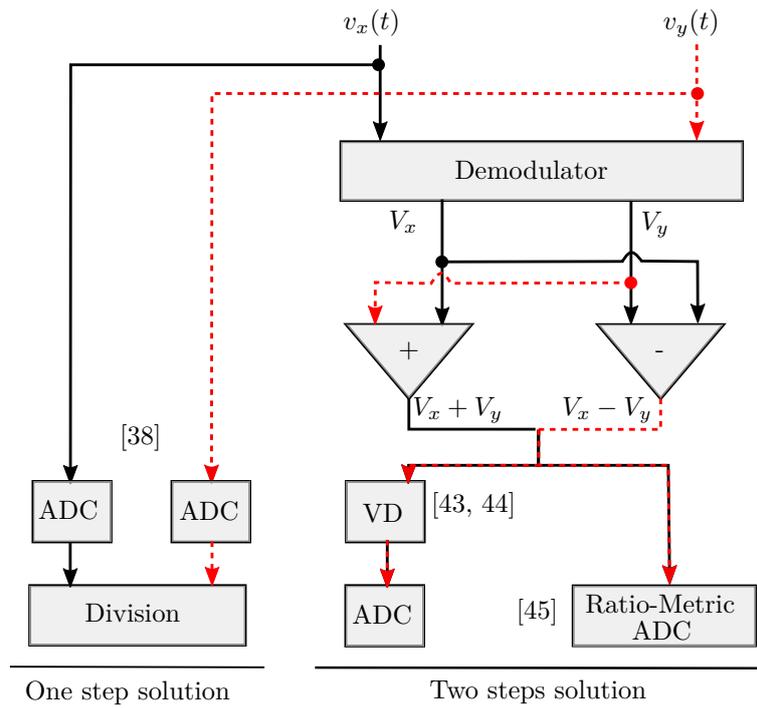


Figure 1.5.1 : A simplified diagram of the possible implementation of the ratio metric analog to digital interface.

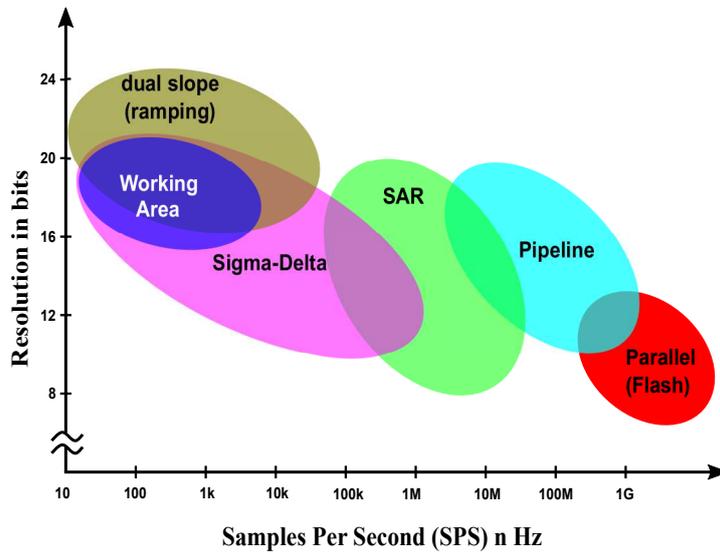


Figure 1.5.2 : Resolution versus conversion rate of different types of ADCs

$$ENOB = \log_2(f_s \cdot T_{charge}) - 1, \quad (1.5.1)$$

where f_s is the sampling frequency. The main disadvantage of this method is the slow conversion rate. For instance, a required resolution of 16 bits with a controller clock of 1 MHz results in a sampling rate of just 7.6 samples per second. This means that, the value of V_{in} should be unchanged during the charge time $T_{charge} \approx 66$ ms. In other words, the fact that the master clock is generated by the MEMS resonators, a very high quality factor is required in order to achieve a 16 bits resolution $Q > 2^{17}$. By contrast, $\Sigma\Delta$ -ADCs take advantage of oversampling and noise shaping techniques to attain high resolution with relatively low output data acquisition time [46]. As will be presented in the next chapter, with a first-order $\Sigma\Delta$ -ADC, a resolution of 16 bits can be achieved with a sampling rate of 40 times larger than that of the dual-slope ADCs, while requiring a quality factor ($Q \approx 3.10^3$). These features make $\Sigma\Delta$ -ADCs preferred for the targeted ratiometric readout.

1.5.5 Demodulator

Using synchronous demodulation technique may not be the best choice. In fact, as discussed earlier, the two MILO's outputs are not in phase. Thus, a residual error may occur when dividing the demodulated signals due to the leftover harmonics from the filtering operation. On the other hand, lowering the filter's cut-off frequency will limit the speed of the system. This last issue is a severe disadvantage when the settling time is critical. Taking samples around the voltage peaks may be an advantageous choice. Doing so leads to: (i) a higher SNR , (ii) an improved immunity to phase variation, and (iii) relaxing the constraint related to the filter. In addition, the quadrature clock to sample the sensing signal ($v_x(t)$ or $v_y(t)$) at its peak value is directly provided from the comparator output. This avoids the need of external clock generation circuit. A possible implementation of this circuit is described in appendix E. Fig. 1.5.3 presents a system-level view of the MILO, including the demodulator and the ratiometric analog to digital interface.

1.6 Conclusion

In this chapter, a generic model of MEMS resonator was given. An original system-level review of existing resonant sensor architectures, including conventional and tow weakly coupled-resonator sensors was then revised. A general figure of merit for the different output metrics used in theses architectures was defined to compare their performance in the linear and nonlinear regime. It has been highlighted that the performance of the conventional metrics such as phase and frequency of all architectures are limited by the A-f effect. In contrast, the amplitude-ratio based on WCRs keeps improved even beyond the critical amplitude. Since amplitude ratio is an unbounded quantity, we studied an al-

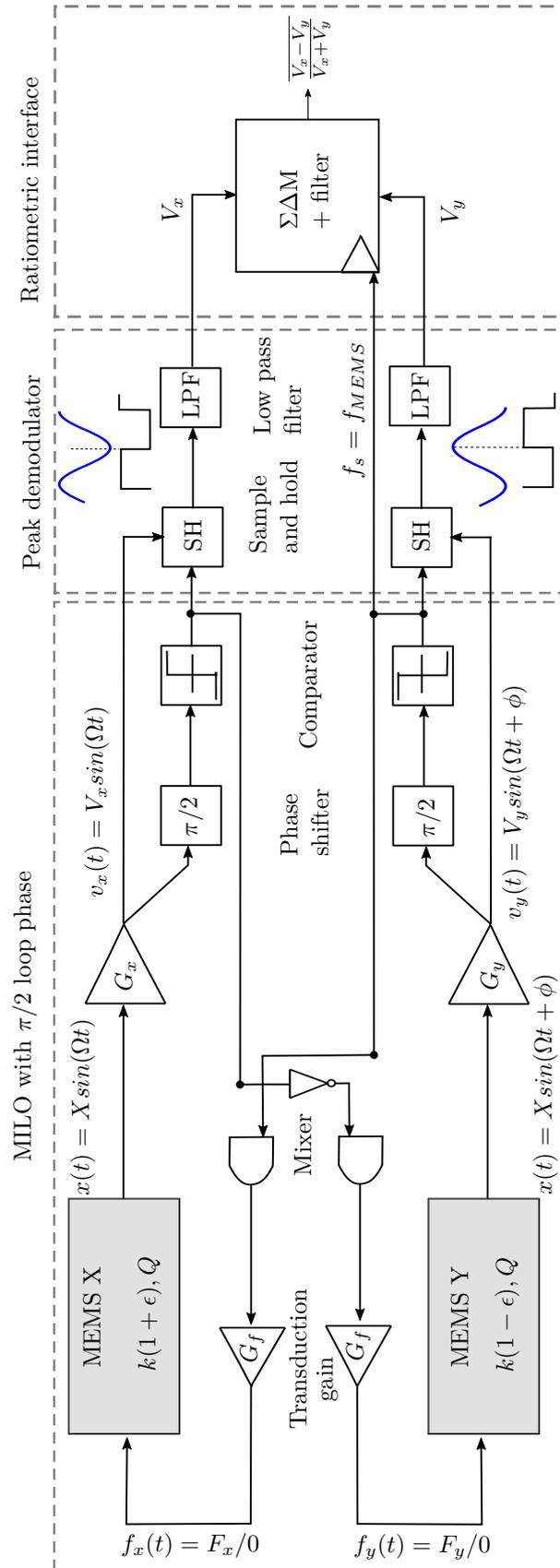


Figure 1.5.3 : System-level view of the MILO, including the demodulator and the ratio-metric analog to digital interface.

ternative analog output metric with similar advantages but being bounded and, therefore, more amenable to analog-to-digital conversion and implementation in integrated circuits. Possible state-of-the-art solutions to implement the corresponding readout interface are then discussed. Among different ADCs, the $\Sigma\Delta$ converter has been shown to be most suitable for high-resolution and moderate-speed applications.

In the following chapter, the proposed $\Sigma\Delta$ modulator design for the bilinear amplitude-ratio that is defined in sec. 1.4 will be discussed. It describes and compares in more details different modulator topologies with respect to our requirements. Afterwards, new techniques concerning the design optimization of the proposed $\Sigma\Delta$ modulator are described. Finally, ideal and noisy electrical simulation of the final modulator architecture will be presented.

Chapter 2

Ratiometric analog to digital interface based on sigma delta modulator

2.1 Introduction

In this chapter, the architectures of $\Sigma\Delta$ Modulator ($\Sigma\Delta\text{M}$) for the ratio-metric measurement are studied. Starting in the first part by introducing the useful performance metrics and describing the basic principle of sigma-delta modulation. In this section, a systematic study on the traditional single-loop single-bit topology is provided, and the plots of the output response are illustrated. The results are obtained based on behavioral simulations using MATLAB® / $\Sigma\Delta$ toolbox developed in [46]. The next section lists the large variety of the modulator architectures, including domain, quantizer resolution, loop filter order, and topology. The objective is to reduce the alternatives for implementing a ratio-metric $\Sigma\Delta\text{M}$ (RM- $\Sigma\Delta\text{M}$) by selecting the appropriate architecture from those categories. There is a stress on the one-bit feedforward topology since it allows a significant simplification in the design of ratio-metric readout of the bilinear quantity B [45]. Moreover, the specifications settled in the previous chapter specify a resolution at least 16 bits within a narrow bandwidth (< 2 kHz) at low frequencies. Therefore, the study above third-order structure or cascade topology is out of the scope of this thesis.

The third part of this chapter concentrates on exploring the optimum combination of the loop coefficients for the selected $\Sigma\Delta\text{M}$. The spot is to achieve a maximum resolution when the input signal equal to LR of the sensor while minimizing the constraints on the analog-blocks (output swing, area, and power consumption). Finally, the non-idealities of the integrator, including (finite DC gain, gain bandwidth, slew rate and output swing), which are the major sources of errors and SNR degradation, are characterized and specified to preserve a theoretical resolution of 16 bits when the absolute temperature up to 125°C . A new system-level modeling approach based on g_m/I_d methodology is proposed to estimate the optimum integrator specifications for given modulator requirements. Finally, the specifications settled by the proposed model were validated with "verilogA" using Cadence

Spectre® simulations.

2.2 Operating principle and resolution of a sigma delta converter

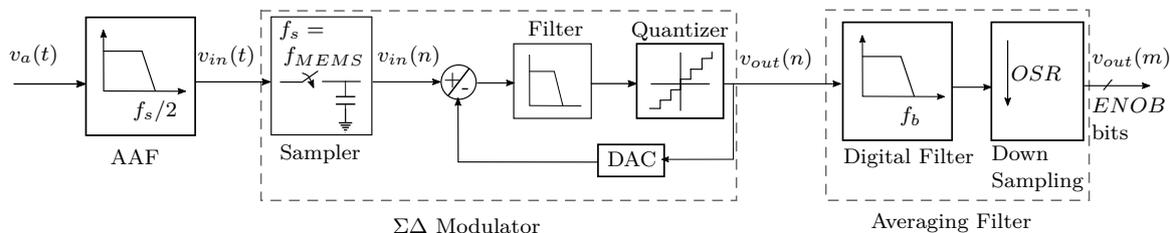


Figure 2.2.1 : Block diagram of a $\Sigma\Delta$ -ADC

2.2.1 Operating principle

The key elements of $\Sigma\Delta$ -ADCs are shown in Fig. 2.2.1. After filtering of the analog signal $v_a(t)$ through the anti-aliasing-filter (AAF), the input signal $v_{in}(t)$ is over-sampled at a rate OSR times faster than its Nyquist rate $v_{in}(n)$, and then quantized with a low resolution quantizer (1 to 4 bits). The resulting signal $v_{out}(n)$ is then converted back using digital to analog converter DAC and injected to $v_{in}(n)$, creating a closed-loop system. The loop shapes the quantization noise in a manner to force it out of the band of interest. This architecture adds a digital averaging filter (or decimator) to the process conversion to filter out noise components outside the Bandwidth ($BW = 2f_b$), and downsampling the filtered information to a slower digital code $v_{out}(m)$ (Fig. 2.2.1). In short, $\Sigma\Delta$ -ADCs take advantage of oversampling and noise shaping techniques to attain high resolution using a low-resolution quantizer. These characteristics relax the constraints on the design of the AAF and the analog blocks, making $\Sigma\Delta$ -ADCs well-suited for high-resolution low-power applications. Considering an ideal modulator with L^{th} order loop filter, the Noise-Transfer-Function (NTF) that shapes the noise out of BW , and the Signal-Transfer-Function (STF) representing the input/output gain of the modulator can be expressed by (seen appendix B for more details):

$$STF(z) = z^{-L}, \quad (2.2.1a)$$

$$NTF(z) = (1 - z^{-1})^L. \quad (2.2.1b)$$

The ideal frequency response of the STF is L delay samples, whereas that of the NTF is a L^{th} order high pass filter. Thus, the input signal is just replicated at the output with

no change, while the quantization noise is attenuated at low frequencies and amplified at high frequencies.

2.2.2 Metrics and definitions

Besides, the signal to noise (or quantization noise ($SQNR$)) ratio, and the effective number of bits $ENOB$, there are other performance indicators that characterize a $\Sigma\Delta M$ such as Voltage-Overload-Level (V_{OL}) and dynamic range DR . V_{OL} is also referred to the Maximum-Stable-Amplitude (MSA). It represents the critical amplitude of the (voltage) input signal above which the system is considered to be unstable. V_{OL} is generally determined when the SNR drops more than 3 dB below the peak SNR value ($SNR(V_{PK}) \equiv SNR_{PK}$) [48]. This amplitude is usually normalized to the reference voltage of the modulator ($\hat{V}_{OL} = V_{OL}/V_{ref}$) and specified in terms of decibel Full-Scale ($dBFS$) units (Fig. 2.2.2). Note that V_{ref} is defined as the input, whose magnitude equals the maximum magnitude of the feedback DAC (V_{DAC}) (relative to the common mode level V_{cm}) of the modulator. The dynamic range DR is defined as the maximum input amplitude for which the structure still operates correctly, to the value of the smallest detectable input amplitude signal (Fig. 2.2.2), it can be expressed as,

$$DR = SNR_{PK} - 20 \log \left(\frac{V_{OL}}{V_{PK}} \right). \quad (2.2.2)$$

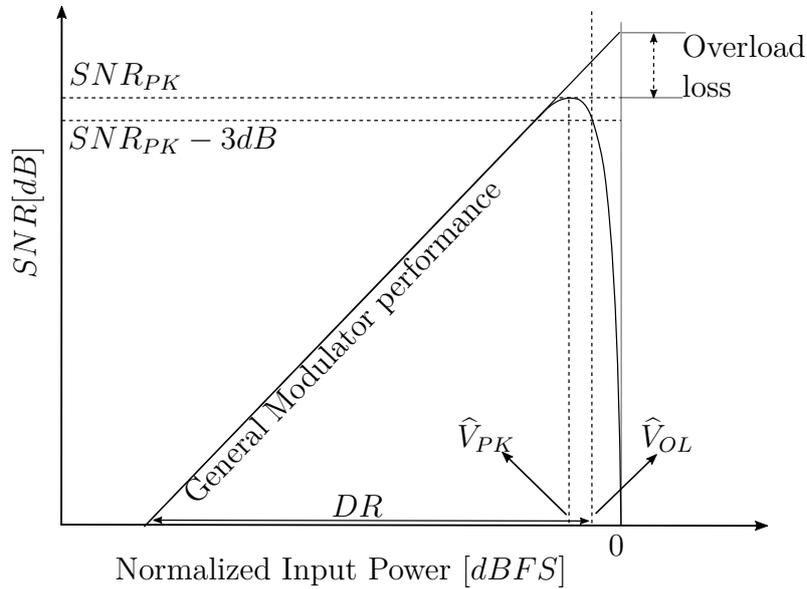


Figure 2.2.2 : A typical SNR versus normalized input power ($\hat{V}_{in} = V_{in}/V_{ref}$) of a $\Sigma\Delta M$

2.2.3 Resolution

The achievable resolution by a $\Sigma\Delta$ -ADC can be evaluated by computing the in-band noise subject to oversampling and shaping phenomena. It's recalled that the sampling clock and the signal are harmonically related since the modulator is clocked by one of the MEMS outputs signals. As a result, the quantization noise becomes correlated to the input signal. However, as mentioned in [49], the power spectral density of the oversampled quantization noise ($PSD_Q(f)$) remains accurate enough for most purposes. This quantity is expressed by,

$$PSD_Q(f) = \frac{V_{Q-FS}^2}{(2^{2d} \cdot 12) \cdot f_s/2}, \quad (2.2.3)$$

where d and V_{Q-FS} are the quantizer's full scale voltage and number of bits respectively, the remaining in-band quantization noise power ($\overline{v_q^2}$) for L^{th} order modulator (2.2.1a)) assuming ($f_b \ll f_s$), is then given by,

$$\overline{v_q^2} = \int_0^{f_b} PSD_Q(f) \times |NTF|^2 df \approx \frac{V_{Q-FS}^2}{2^{2d} \cdot 12} \cdot \frac{\pi^{2L}}{(2L+1) \cdot OSR^{2L+1}}, \quad (2.2.4)$$

where $OSR = f_s/2f_b$ is the oversampling ratio. Since the signal at the modulator output is just a delayed version of the input signal (delayed by L clock samples for an L^{th} order modulator (2.2.1a)) the general $SQNR$ expression for a L^{th} order $\Sigma\Delta M$ can be written as,

$$SQNR(dB) = 6.02d + 1.76 + 20\log(\widehat{V}_{in}) + 3.01(2L+1) \cdot \ln_2(OSR) - 10\log\left(\frac{\pi^{2L}}{2L+1}\right). \quad (2.2.5)$$

From (2.2.5), it can be noticed that the $SQNR$ is a function of three parameters: the resolution of the quantizer d , the oversampling ratio OSR and the modulator order L . Increasing these parameters to increase $SQNR$, is not without consequence at several levels, from the designer's point of view. For a required $SQNR$, it is the duty of the designer to find the set of these three parameters that optimize the overall performance and complexity of the modulator. For example, a 6dB improvement of $SQNR$ can be made for each additional bit in the quantizer. However, a larger d requires an increase in the number of bits of the feedback DAC. This makes the modulator sensitive to DAC nonlinearity error; solving this issue requires linearization techniques, such as dynamic element matching [46, 50], that increase system complexity and hence power consumption. As another example, doubling the OSR results a $(2L+1) \times 3dB$ improvement in the $SQNR$. However, OSR is restricted by the clock speed f_s and the system bandwidth $2f_b$, and hence power consumption. Finally, using a higher-order filter has a negative impact on the stability of the modulator. This may only be understood with a more complex model than the one given in appendix B, where it is assumed that the gain of

the quantizer is constant. This assumption is, in fact, valid only as long as the input of the quantizer does not exceed V_{ref} . However, for large input values and for a higher-order filter, the quantizer input is frequently higher than V_{ref} so that the effective quantizer gain decreases significantly [51]. This fact changes the pole location of the NTF leading to instability and thus to a lower MSA , as illustrated in Fig. 2.2.3. However, the first order modulator remains stable in any circumstances [46].

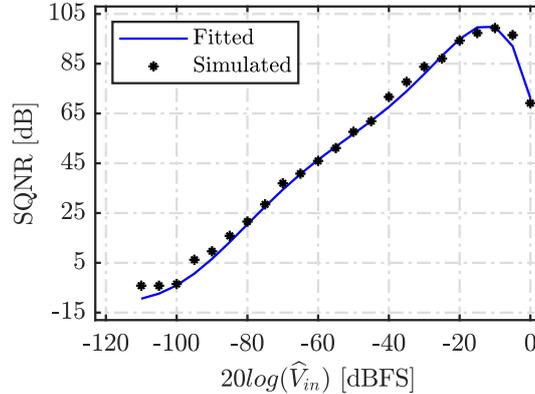


Figure 2.2.3 : $SQNR$ versus input power for $L = 2$, $d = 1$ and $OSR = 256$

2.3 Modulator architecture selection

This section focuses on the selection of the appropriate modulator for high-resolution ratio-metric measurement. Considering the requirement imposed by sensors, the targeted architecture must first adapt to the master clock of the resonators ($f_s = f_{MEMS}$), which may range from some hundred kHz to 1 MHz. Second, the locking range specified by the sensor for the bilinear quantity was approximately $LR \approx 0.57$, and thus the desired RM- $\Sigma\Delta$ M must provide a $MSA > LR$. Finally, the modulator should be temperature aware designed under the specified range from -40 to 125 °C, while maintaining a theoretical worst-case resolution of at least 16 ENOB. Yet, we have introduced the sigma-delta modulation principle, and why it's the architecture of choice when targeting a good trade-off between high resolution, low signal bandwidth, and low power consumption. However, other essential aspects practically must be considered when addressing the modulator to a specific application. Besides the loop filter order and the quantizer resolution, the modulator domain, and the loop filter topology must be considered when addressing $\Sigma\Delta$ M implementation to a specific application.. In what follows, all these aspects are investigated, and a comparative analysis is performed to figure out which is the most suitable architecture for the considered application. An illustration of the large variety of a $\Sigma\Delta$ M architectures is shown in Fig. 2.3.1.

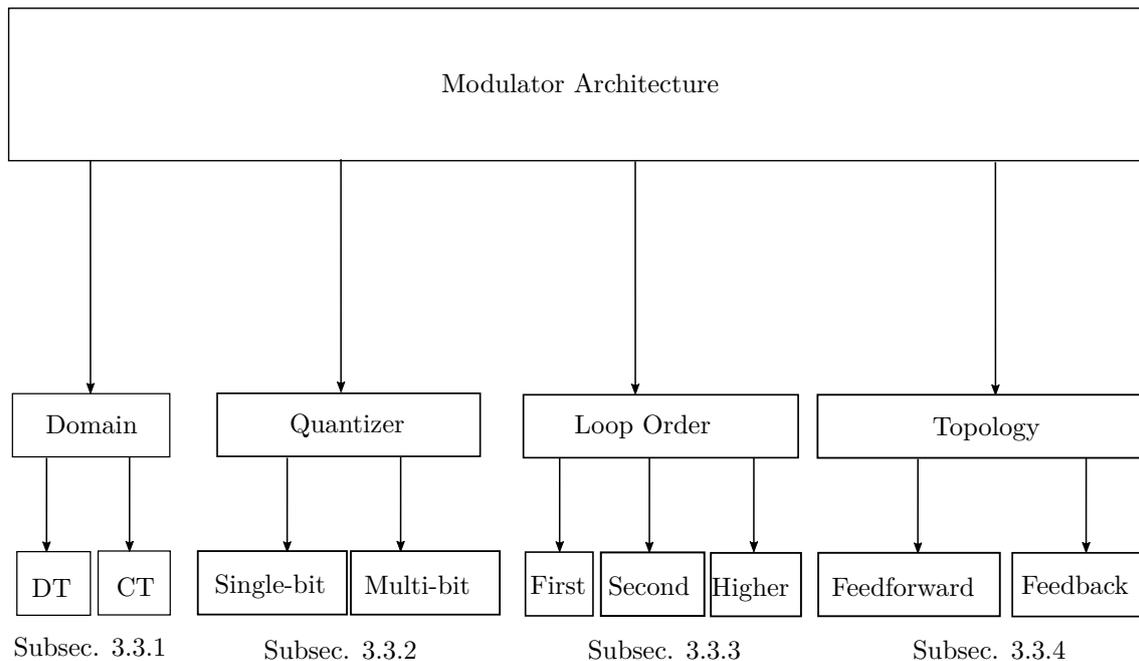


Figure 2.3.1 : Possible implementation of a modulator architecture

2.3.1 Domain: discrete time vs continuous

$\Sigma\Delta$ can be implemented using either Discrete-Time (DT) circuits or Continuous-Time (CT). The key concepts of the L^{th} order CT and DT modulator architectures are shown in Fig. 2.3.2 and Fig. 2.3.3 respectively. The main difference between them is where the sampling is done. In a DT- $\Sigma\Delta$, sampling of the input signal occurs prior to the loop filters (Fig. 2.3.2(a)), whereas for CT- $\Sigma\Delta$ sampling operation takes place just before the quantizer (Fig. 2.3.3(a)). This is a major advantage of the CT structure since all the errors generated by the non-idealities of the sampling process are shaped by the $N\text{TF}$ as for the quantization noise. Furthermore, in a DT- $\Sigma\Delta$ the loop filter is implemented by Switched-Capacitor (SC) circuits (Fig. 2.3.2(b)), whereas in a CT- $\Sigma\Delta$ by a transconductance amplifier as OTA-RC (Fig. 2.3.3(b)) or by Gm-C (Fig. 2.3.3(c)) topology.

The OTA-RC implementation is more linear than the Gm-C implementation, but it is also power consuming [52]. A trade-off to maintain a good linearity while reducing the power consumption is to perform the first stage as an OTA-RC filter and the following ones as Gm-C filters [53]. The advantages and drawbacks of DT- $\Sigma\Delta$ and CT- $\Sigma\Delta$ implementations are discussed in detail in the following subsections.

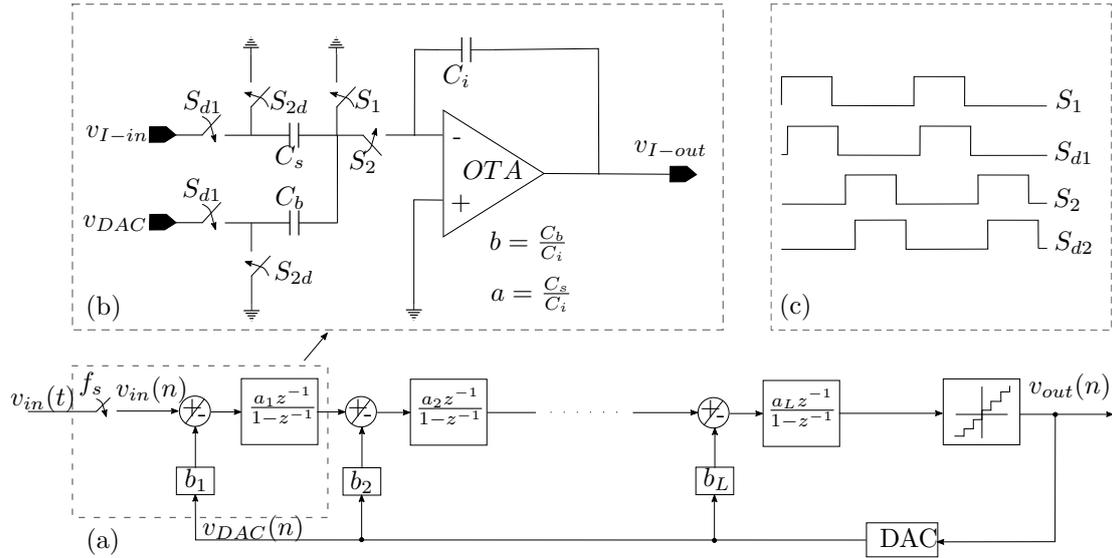


Figure 2.3.2 : General architecture of L^{th} order discrete time $\Sigma\Delta$ modulator DT- $\Sigma\Delta$ M, (a) block diagram, (b) electrical implementation of the integrator, (c) clocking scheme of the integrator.

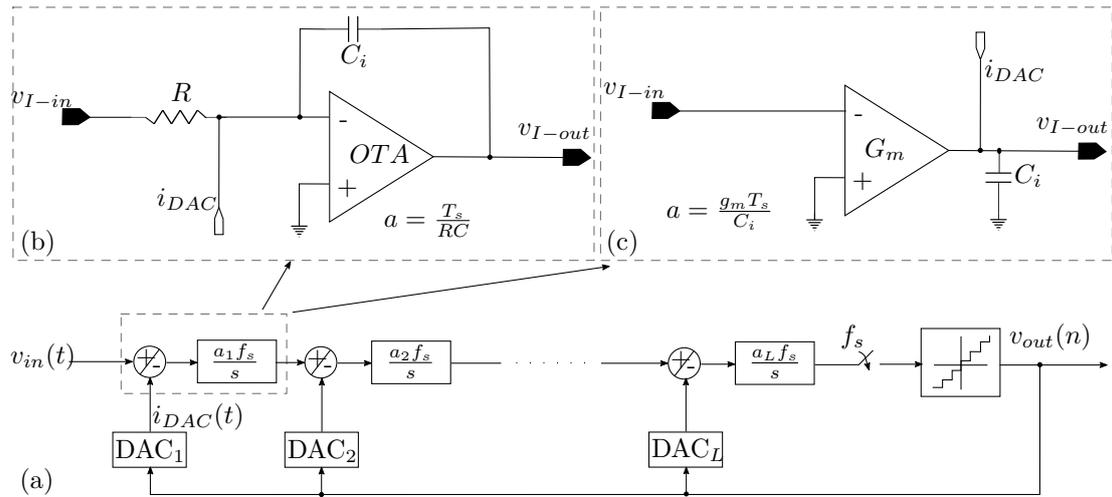


Figure 2.3.3 : General architecture of L^{th} order continuous time $\Sigma\Delta$ modulator CT- $\Sigma\Delta$ M, (a) block diagram, implementation of the integrator as (b) OTA-RC or (c) Gm-C components.

2.3.1.1 Coefficient sizing and trimming with frequency

The coefficients of the $\Sigma\Delta$ play an important role in both performance and stability. For instance, when higher-order loop filters are used, smaller loop coefficients is introduced to ensure loop stability, and preserve the noise shaping ability of the modulator. These

coefficients form a part of the loop filters and usually are co-implemented with them, as can be seen from Fig. 2.3.3(b) and Fig. 2.3.2(b). In fact, applying the total charge transfer analysis on the DT-integrator of Fig. 2.3.2(b), its output (assuming an ideal OTA) is given by

$$\begin{aligned} V_{I-OUT}(z) &= \left(\frac{C_s}{C_i} \cdot V_{I-IN}(z) - \frac{C_b}{C_i} \cdot V_{DAC}(z) \right) \times \frac{z^{-1}}{1 - z^{-1}} \\ &= (a \cdot V_{I-IN}(z) - b \cdot V_{DAC}(z)) \times \frac{z^{-1}}{1 - z^{-1}}, \end{aligned} \quad (2.3.1)$$

while for CT integrator (in the case of OTA-RC) is given by,

$$V_{I-OUT}(z) = \frac{1}{sRC_i} \cdot V_{I-IN}(z) - \frac{1}{sC_i} \cdot I_{DAC}(s) = a \cdot V_{I-IN}(z) \times \frac{1}{sT_s} - I_{DAC}(s) \times \frac{1}{sC_i}. \quad (2.3.2)$$

The coefficient a in (2.3.2) is T_s/RC_i . It can be indicated that the value of this coefficient depends linearly on the sampling time ($T_s = 1/f_s$) as opposed to those implemented by DC-integrators. This entails that the components of a CT integrator must be adjusted to allow it to operate on a different f_s . This drawback does not exist for the DT-integrators since their coefficients scale automatically with frequency. In DT-integrators resistors are emulated using a combination of switches and capacitors. Considering the switched capacitor network of Fig. 2.3.4, in which the current (i_c) charges the capacitor C_s during the half period ($0 < t < T_s/2$), assuming $v^- = 0$, one may write,

$$\overline{i_c} = \frac{1}{T_s} \int_0^{T_s/2} i_c \cdot dt = \frac{Q'(T_s/2) - Q'(0)}{T_s} = \frac{v_{I-in} \cdot C_s}{T_s} \equiv \frac{v_{I-in}}{R}, \quad (2.3.3)$$

where Q' is the accumulated charges stored in the capacitor and $\overline{i_c}$ is the average current during T_s . As can be seen from (2.3.3), the circuit actually behaves like a resistor whose value is proportional to the sampling period (T_s), and hence the resulting integrator coefficient will be adapted automatically to f_s . Another advantage of using DT-integrators is their coefficient immunity to PVT variation. In fact, due to process variation, integrated capacitors might have 10% variations, whereas resistances or transconductances values might have more than 20% variations [47]. Thus, process induced coefficient deviation of about 30% is to be expected in continuous time integrators. By contrast, implementing the coefficient as a ratio of two capacitors makes them subjected only to a 1% process mismatch variation [47]. Furthermore, resistance and transconductance values change substantially with temperature variation, whereas capacitors are intrinsically independent of the temperature variation.

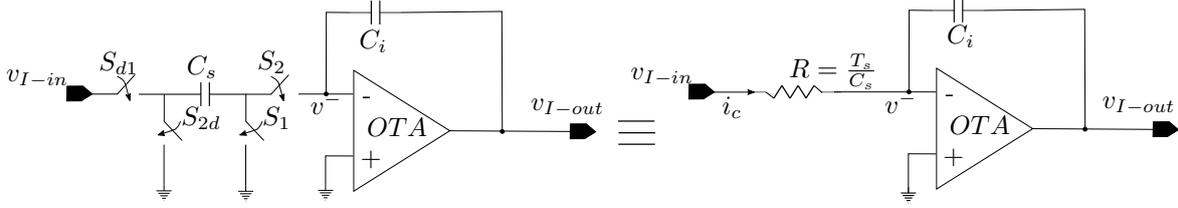


Figure 2.3.4 : The simulation of a resistor with SC circuits

2.3.1.2 Thermal Noise

Limiting the thermal noise is one of the fundamental challenges in achieving high-resolution ADCs. In fact, with technology advance, the thermal noise becomes more problematic since the supply voltages are becoming lower. Therefore, preserving the same resolution leads to an increase of the constraints on the ADC blocks. However, thanks to the noise shaping property in a $\Sigma\Delta$ M, the noise produced from the i^{th} filter is shaped by the $i^{th} - 1$ previous filters. Thus, the thermal noise is a serious concern just in the first stage [46]. If noise contribution of the OTA is neglected, the noise power spectral density at the input of the modulator ($PSD_{th,in-\Sigma\Delta}$), considering a single-ended integrator (whether CT or DT integrator) can be expressed as,

$$PSD_{th,in-\Sigma\Delta}(f) = n_a \cdot \frac{K_B T}{a C_i f_s / 2}, \quad (2.3.4)$$

where $K_B = 1.381 \cdot 10^{-23} J/K$ is the Boltzmann's constant, T is the absolute temperature of the device in degree Kelvin, a and n_a are the integrator coefficient and the noise factor. They are $(T_s/RC_i, 4)$ and $(C_s/C_i, 2)$ for CT and DT integrator respectively [48]. If it is assumed that the decimation filter cancels all out of band noise, the modulator output thermal noise power ($\overline{v_{th,out-\Sigma\Delta}^2}$) is then given by:

$$\overline{v_{th,out-\Delta\Sigma}^2} = \int_0^{f_b} PSD_{th,in-\Sigma\Delta} df = n_a \cdot \frac{K_B T}{a \cdot C_i \cdot OSR}. \quad (2.3.5)$$

Let SNR be the targeted signal to first thermal noise ratio that usually constitutes the main thermal noise contribution. The minimal value of C_i is then restricted by,

$$C_i \geq n_a \cdot \frac{K_B T}{a \cdot OSR} \cdot \frac{10^{SNR/10}}{V_{in}^2}. \quad (2.3.6)$$

The above expression shows that, for a given integrator coefficient a , the integrating capacitor C_i must be higher than a certain value in order to achieve the desired signal to thermal noise ratio. Besides, a larger C_i leads to an increase in C_s or a decrease in R by the same factor, imposing a stronger constraint in terms of gain-bandwidth (GBW) and slew-rate (SR) on the OTA, and causes an increase of the die area. This constraint is more restrictive for CT design because of its higher noise factor n_a . Moreover, R is

expected to have a positive temperature coefficient, when temperature goes up, R also increases, leading to a higher thermal noise ($4K_B T \cdot R$). This issue does not occur in DT integrator since the noise generated by the switching network does not depend on the switch on-resistance. For these reasons DT design could be more attractive for low noise applications.

2.3.1.3 Jitter

Jitter is mainly caused by the phase noise of the clock generation circuitry (the MILO in our case). It causes an added random phase modulation to the output bitstream [54]. In fact, In $\Sigma\Delta$ converter, the spectrum of the output stream is very noisy outside the signal band; a random phase modulation causes the noise outside the signal band to fold into the signal band, raising the converter noise floor and degrading its resolution. The signal to jitter noise ratio for DT- $\Sigma\Delta$ Ms (SNR_{j-DT}) can be approximated by [51],

$$SNR_{J-DT} \approx 20 \log \left(\frac{OSR^{3/2}}{2\pi f_s \sigma_t} \right), \quad (2.3.7)$$

whereas for CT- $\Sigma\Delta$ Ms (SNR_{j-CT}) by [51],

$$SNR_{J-CT} \approx 20 \log \left(\frac{OSR^{1/2}}{2\pi f_s \sigma_t} \right), \quad (2.3.8)$$

where σ_t is the clock jitter standard deviation. It can be seen by comparing (2.3.7) and (2.3.8) that the impact of jitter is significantly higher (OSR times) on CT modulators than on DT modulators. In fact, in a CT design, the sampling occurs at the quantizer rather than the input, which means the jitter affects the sum of the input plus quantization noise—a signal with considerably more power than the input alone. Jitter is one of the main concerns in CT- $\Sigma\Delta$ Ms [54]. Their implementation frequently requires the use of a highly precised clock generator [51].

2.3.1.4 Switch non-idealities

Sampling switch non-idealities such as non-linearity and charge injection is mainly attributed to the on-resistance and the associated parasitic capacitance. These produce harmonic distortion and signal deformation, which degrade the performance of the ADCs (linearity and resolution) [55]. Considering the DT design, the sampling of the input signal occurs prior to the first stage. This implies that any signal distortion produced at this level due to the switch non-idealities will come out at the modulator's output. Hence, there is a need to use an advanced sampling switch such as bootstrap, transmission gate, or dummy switch addition to preserve a good sampled signal quality. These techniques increase the die area, the design time, and the power consumption of the circuit. However, these constraints are relaxed in CT design since the sampling operation takes place at the input of the quantizer (last stage of the modulator). And the error at this level is shaped

by $i^{th} - 1$ previous stages.

2.3.1.5 Power consumption

Generally, the OTA is the most power consuming block in the analog part of the $\Delta\Sigma\text{M}$. Its finite GBW is one of the main limiting points on the speed of the modulator. This issue is more severe for DT- $\Sigma\Delta\text{M}$ than for CT- $\Sigma\Delta\text{M}$ counterparts. Assuming a one pole OTA, when the ratio of the unity GBW frequency (f_T) to the sampling frequency (f_T/f_s) decreases, the induced error of the OTA limited bandwidth increases linearly for CT integrator, while increases exponentially for DT integrator. This is because the input current to be integrated by C_i is a Dirac function for DT integrators, whereas it is a simple sinusoidal function for CT integrators. In practice and depending on the required resolution, CT-integrators' OTA can be designed with f_T/f_s around 2 to 3 compared to 5 for DT-integrators [46]. Thus, for the same conversion bandwidth, the CT-modulators are generally less power consuming.

2.3.1.6 Conclusion

The main benefits of CT over DT architectures are the speed and the power consumption. However, a DT implementation has been selected since it is more prone to reconfigurability and more robust to coefficient mismatch, especially against PVT variation. In fact, for a narrow band application < 2 kHz and sampling frequency < 1 MHz, the power consumption is not a limiting point in the design. Moreover, the pole locations of the CT integrators do not scale with frequency as in DT counterpart. This limits the use of CT- $\Sigma\Delta\text{M}$ in the considered application where the master clock is generated by the resonators, and may vary from one sensor to another. Finally, DT-modulators are less constrained by electronic thermal noise, and are more robust against jitter noise.

2.3.2 Single-bit vs. multi-bit quantizer

The multi-bit quantizer is generally followed by a feed-back DAC of the same resolution. As discussed earlier, the quantizer error is attenuated by the NTF , but this doesn't happen for the DAC errors that are injected into the first stage. Consequently, the accuracy of the DAC should be at least less than the least-significant-bit (LSB) to preserve a good linearity of the converter. To do so, an extra circuit is generally needed, such as trimming or dynamic matching [46, 50] that maximizes circuit complexity, hence power and area. By contrast, the single-bit modulator is intrinsically linear, and the DAC is implemented with only two reference voltages (V_{ref} or $-V_{ref}$) and the quantizer by just a comparator. Since the signal bandwidth is quite low ($BW \leq 2$ kHz), a relatively high $OSR > 256$ can be achieved for $f_s \leq 1$ MHz. The desired resolution can then be ensured using only 1-bit quantizer. Moreover, implementing the DAC with only two levels is beneficial for

Table 2.1 : CT versus DT modulators

	DT-modulator	CT-modulator
Jitter noise	☺	☹
Power consumption	☹	☺
Coefficient immunity to PVT variation	☺	☹
Adaptability with f_s	☺	☹
Thermal noise	☺	☹
Switch non-idealities	☹	☺

the desired ratio-metric functionality as it will be pointed out later in this chapter. The multi-bit quantization is therefore avoided, and the single bit was chosen for the final implementation.

2.3.3 Loop filter order

The selection of the loop filter order is also one of the main important points in the design. According to (2.2.5) increasing L improves the $SQNR$ significantly. This is, however, at the cost of degrading the MSA of the modulator, thereby reducing its available dynamic range [48]. Besides, each increase of L results in an extra integrator and its corresponding coefficients that increase chip area and power consumption. Figure 2.3.5 shows the $SQNR$ vs. input level for L ranging from 1 to 5 using 1-bit quantizer and considering an OSR of 256. Note that the simulated modulators have been optimized for a good compromise between aggressive noise shaping and stability, and only the quantization noise is considered. This is done using the function “synthesizeNTF” of the MATLAB® $\Sigma\Delta$ toolbox developed in [46].

From the plots, it can be inferred that for a required MSA of greater than 0.57, the modulator order must be at most 3. In addition, achieving a resolution of 16 bits or $SQNR$ of 98 dB, calls for a second or higher order modulator. Indeed, by including the thermal noise and always under the same conditions (OSR , 1-bit quantizer), a second or-

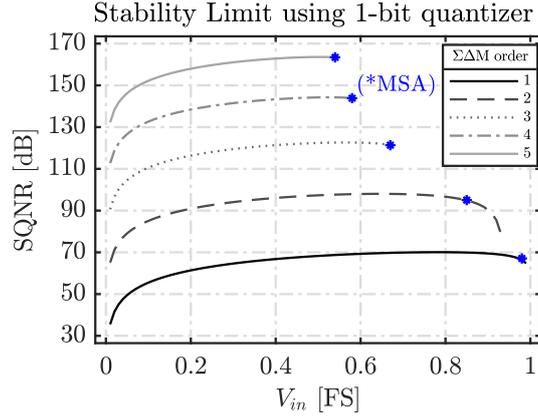


Figure 2.3.5 : $SQNR$ against linear input level for a first to fifth order modulator, considering 1-bit quantizer and OSR of 256

der modulator may not be enough. However, the modulator coefficients can be optimized to allow a higher $SQNR$ instead of a better MSA . This means that by sacrificing a portion of the available dynamic range the theoretical resolution can be enhanced, e.g., 1 to 2 bits, and hence an $ENOB \geq 16$ bits can be ensured. To conclude, the second order architecture offers a good compromise between our requirements and design complexity, and was preferred for the targeted modulator.

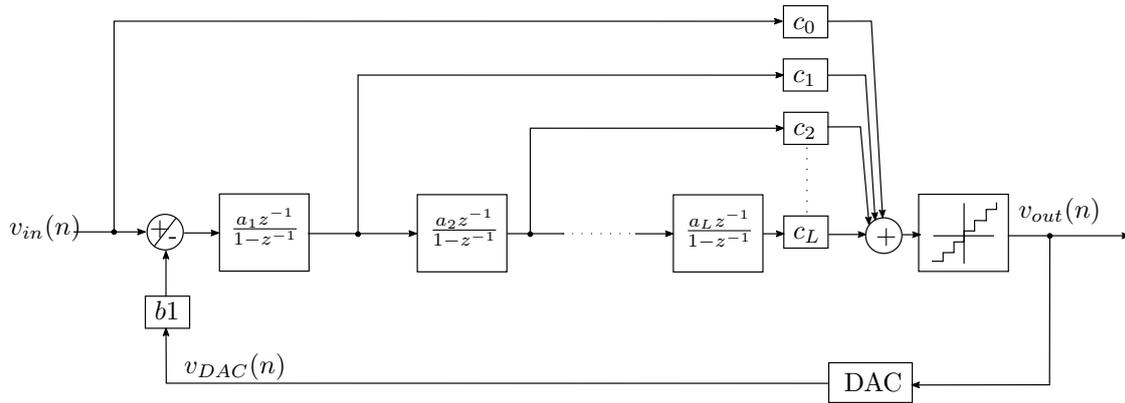


Figure 2.3.6 : General architecture of L^{th} order full feedforward DT- $\Sigma\Delta$ (FF-DT- $\Sigma\Delta$)

2.3.4 Loop topology

Single-loop $\Sigma\Delta$ can be divided into two main topologies: Distributed feedback (FB) topology (Fig. 2.3.2) and feed-forward (FF) topology (Fig. 2.3.6). The difference between them is how the loop coefficients are implemented. These coefficients are introduced to improve the stability of the modulator by creating zeros in the loop [50]. For the desired modulator functionality (ratiometric), it is reported in [17] and [45] that the FB topology

is less attractive than the FF one. This can be observed by analyzing the chosen (2^{nd} -1-bit-DT- $\Sigma\Delta$) architecture. A practical implementation of this structure employing FB compensation is depicted in Fig 2.3.7(a). In fact, the integrator input signal results from a combination between V_{in} and the feedback signal V_{ref} . The output bitstream decides whether V_{ref} or $-V_{ref}$ is added to V_{in} . Thus, the resulting signal to be integrated is $(V_{in} + V_{ref} = (V_x - V_y) + (V_x + V_y) = 2V_x)$ or $(V_{in} - V_{ref} = (V_x - V_y) - (V_x + V_y) = -2V_y)$.

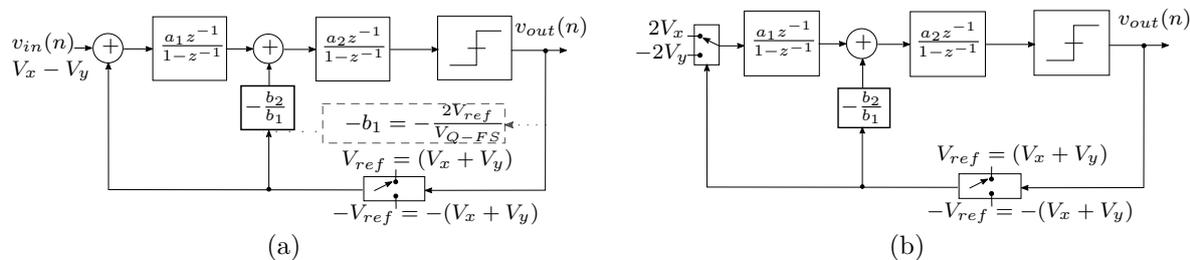


Figure 2.3.7 : Practical implementation of a “FB- 2^{nd} -1-bit-DT- $\Sigma\Delta$ M”, (a) ordinary, (b) modified

The idea is that providing the signal $2V_x$ or $-2V_y$ directly to the integrator eliminates the need for extra analog blocks such as adder and subtractor (Fig 2.3.7(b)). This technique is first described in [45]. It is worth noting that the resulting simplification can not be accomplished if the quantizer was implemented with two bits or higher. Nevertheless, the modified FB structure still does not fulfill the requirements since the signals $(V_x + V_y)$ and $-(V_x + V_y)$ should still be delivered at the second summation node (Fig 2.3.7(b)).

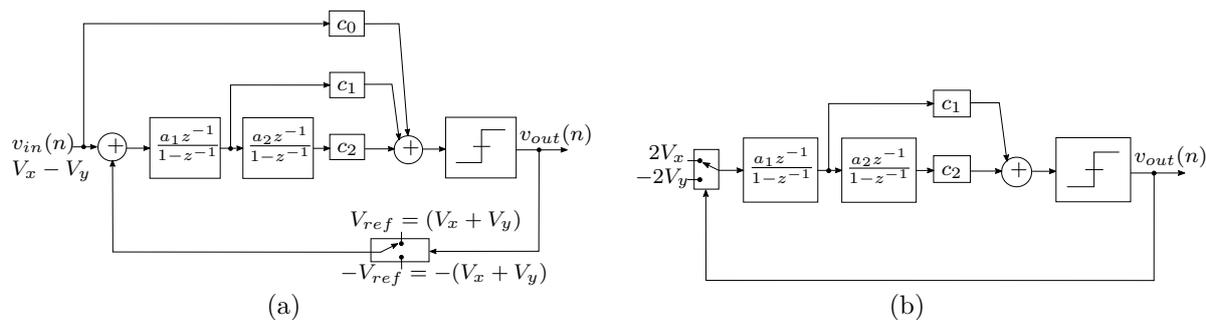


Figure 2.3.8 : Practical implementation of a “FF- 2^{nd} -1-bit-DT- $\Sigma\Delta$ M”, (a) ordinary, (b) modified

At first sight, one may stress that using FF topology does not solve the problem because of the input to quantizer feedforward path as shown in Fig. 2.3.8(a). In this instance, the

input signal ($V_x - V_y$) should be provided instead of the reference voltages. However, this branch has no influence on the stability of the modulator as opposed to that implemented in FB topology. It is usually introduced to compensate the second poles in the STF . For instance, when $c_0 = 1$ and $b_1 = 1$, the STF is equal to 1 regardless of the operating frequency. In fact, for a 2^{nd} order FF architecture, STF and NTF (assuming $g = 1$ see appendix B) can be expressed by:

$$STF(z) = \frac{z^{-2}(a_1 a_2 c_2 - a_1 c_1 + c_0) + z^{-1}(a_1 c_0 c_1 - 2c_0) + c_0}{z^{-2}(a_1 a_2 b_1 c_2 - a_1 b_1 c_1 + 1) + z^{-1}(a_1 b_1 c_1 - 2) + 1}, \quad (2.3.9a)$$

$$NTF(z) = \frac{(1 - z^{-1})^2}{z^{-2}(a_1 a_2 b_1 c_2 - a_1 b_1 c_1 + 1) + z^{-1}(a_1 b_1 c_1 - 2) + 1}, \quad (2.3.9b)$$

and the stability condition of the system by,

$$\frac{a_2 c_1}{c_2} \leq 1. \quad (2.3.10)$$

From the above expressions, it can be concluded that the input to quantizer feedforward path can be omitted since: first, the NTF does not depend on the coefficient c_0 , and second, at low frequencies (within the conversion bandwidth < 2 kHz), this branch has almost no impact on the STF ($\approx 1/b_1$), this analysis is confirmed with simulation for an arbitrary set of coefficients as shown in Fig. 2.3.9. As a result of eliminating this branch, the need of a subtractor to perform ($V_x - V_y$) is relaxed. Another advantage of the FF compensation is that it enables an inherently low-power modulator compared to the FB technique [50]. This because in the FB topology an amount of the modulator' output is fed to the output of the integrators (Fig. 2.3.2). Thus, they require high swing capabilities to avoid saturation. Indeed, the output swing requirement can be relaxed using small coefficients. However, preserving the same thermal noise, a bigger area (for C_i) is then required, and hence more power is needed to charge this capacitor. The FF topology is, therefore, the best candidate for the considered application.

The main design features of the proposed interface compared with the reference implementation [45] is that: (i) being CT it can only operate at a fixed clock frequency, (ii) it is not very robust against temperature and process variation, (iii) it has a limited Common-Mode-Rejection-Ratio ($CMRR$) due to the mismatch in the input resistors or input transconductance, which may limit the common mode input range, and creates an offset error. The final modified architecture for effectively implementing the ratiometric readout is depicted in Fig. 2.3.8(b).

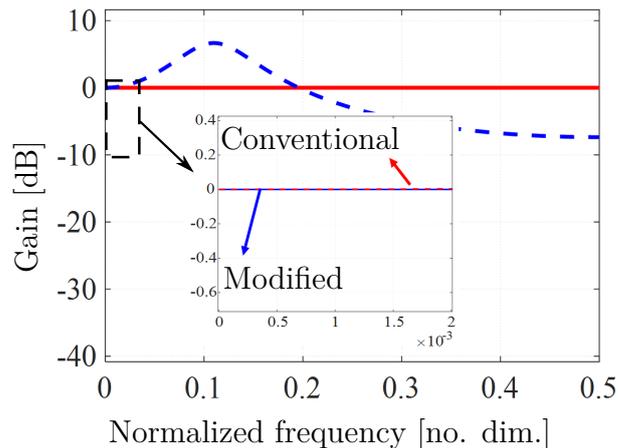


Figure 2.3.9 : STFs of the architectures of Fig. 2.3.8 with an arbitrary set of coefficients that satisfy (2.3.10)

2.3.5 Conclusion

This section has introduced the large variety of a $\Sigma\Delta$ architectures. It has performed a comparative analysis to select the appropriate design for effectively implementing the ratiometric readout. Starting by explaining the operation principle of DT and CT $\Sigma\Delta$ s, and listing their main advantages and drawbacks. The detailed comparison showed that the DT design is more adapted to the concerned application, especially in terms of adaptability and immunity to PVT variation. Next, the advantage of employing a single bit over the multi-bit quantizer when addressing narrow-band-applications was investigated. Behavioral simulations were then accomplished to obtain the optimal loop filter order that allows a resolution of greater than 16 bits and provides $MSA > LR$. Trading between the requirements and the design complexity, a second order modulator was the optimal choice. Finally, the feedback and feedforward loop topologies (compensation techniques) were presented. It was explored that combining a single quantizer with a FF topology yielding to a major simplification in the modulator design. The final selected architecture was, therefore, the FF-2nd-1-bit-DT- $\Sigma\Delta$ and henceforth is referred to RM- $\Sigma\Delta$. The optimum design space coefficients of this modulator will be discussed in the following section.

2.4 Modulator coefficients

The coefficients' choice is a crucial point in the top-down design flow. They are responsible for defining the modulator's: dynamic range, resolution, linearity, and area. The goal is to find the maximum $SQNR$, i.e. $SQNR_{PK}$, for a specific input amplitude, which is 0.57 (normalized), while preserving a good linearity and minimum area. The strategies to explore the appropriate design space starts by determining the feedback-coefficient b_1 . This coefficient is usually fixed by the technology, and it is out of the optimization step.

Second, the feedforward-coefficients c_1 and c_2 are equalized and set to 1, since in 1-bit-quantizer the relevant information at the input is the signal sign and not the amplitude. Finally, behavioral simulations for every combination of the integrator-coefficients a_1 and a_2 are performed to find the best design space solution.

2.4.1 Feedback-coefficient b_1

As mentioned in the previous section, the coefficient b_1 is defined by the voltages V_{ref} and V_{Q-FS} ($b_1 = 2V_{ref}/V_{Q-FS}$). V_{Q-FS} is specified by the supply voltages of the quantizer which is $V_{DD} - V_{SS}$, whereas V_{ref} is set by the steady-state value of the MEMS output voltage (V_0) as illustrated in Fig. 2.4.1 —noting that the coefficient b_1 has no impact on the resolution when only the quantization noise is considered. In fact, the modulator transfer functions STF and NTF have the same dependency on b_1 . Thus, the signal and the quantization noise power will be scaled by the same factor. However, when other noise sources such as switching network and amplifier are considered, the performance of the modulator will be strongly related to b_1 . If the first integrator dominates the thermal noise contribution, the SNR at the modulator's output can then be expressed as,

$$SNR = 10 \log \left(\frac{\left(\frac{V_{in}/b_1 \sqrt{2}}{v_{n,q}^2 + v_{n,th,out-\Sigma\Delta}^2} \right)^2}{\frac{\left(\frac{V_{Q-FS}}{\sqrt{2}} \cdot LR \right)^2}{v_{n,q}^2 + \frac{v_{n,th,in-\Sigma\Delta}^2}{b_1^2 OSR}}} \right), \quad (2.4.1)$$

$$(2.4.2)$$

where $\overline{v_{th,in-\Sigma\Delta}^2}$ represents the total thermal noise power at the input of the modulator. From (2.4.1), it can be indicated that improving the overall resolution requires a higher feedback coefficient, and hence a higher reference voltage ($V_{ref} \propto b_1$). It is worth noting

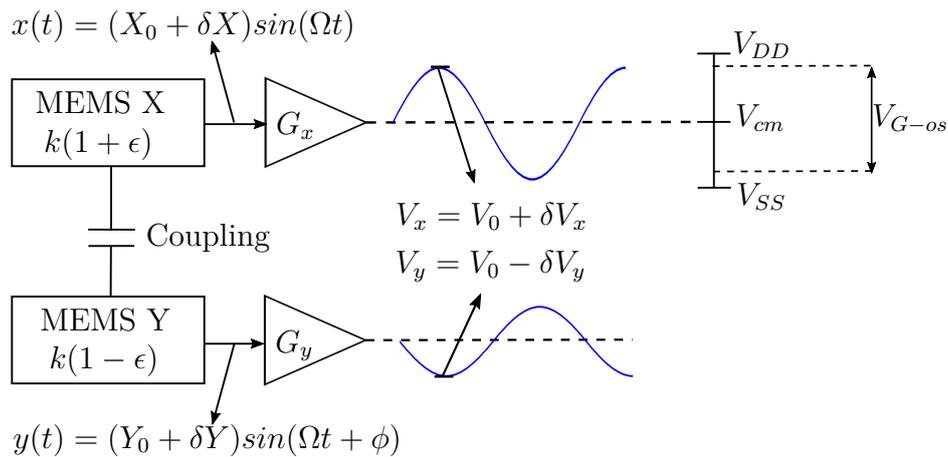


Figure 2.4.1 : Representation of the outputs signals of the sensor

that providing $2V_x$ or $-2V_y$ at the input of the modified structure shown in Fig. 2.3.8(b)

can be obtained using a fully differential input as $\{V_x, -V_x\}$ or $\{-V_y, V_y\}$ respectively. In the present analysis, the half of the fully differential implementation is used for its simplicity and intuition. The reference voltage is therefore rearranged as,

$$V_{ref}^+ = -V_{ref}^- = V_{ref} = \frac{V_x + V_y}{2} = V_0. \quad (2.4.3)$$

As mentioned above, V_{ref} value must be maximized in order to achieve a better SNR . Thus, it is recommended to design the preamplifiers G_x and G_y with a wider output swing (V_{G-os}) so that a higher reference voltage can be achieved. According to Fig. 2.4.1 and using (2.4.3), V_{ref} is related to V_{G-os} by,

$$V_{G-os} = 2V_x^{max} = 2(V_0 + \delta V_x^{max}) = 2V_{ref} \left(1 + \frac{\delta V_x^{max}}{V_0}\right). \quad (2.4.4)$$

Replacing $\delta V_x^{max}/V_0$ by its expression ($\delta V_x^{max}/V_0 = \frac{V_x - V_y}{V_x + V_y} = LR$) in (2.4.4), yields to,

$$V_{ref} = \frac{V_{G-os}}{2(1 + LR)}. \quad (2.4.5)$$

Typically, for classical topologies of amplifiers in the recent technology, the output swing using rail to rail design can reach 90% of the supply voltages [56]. However, considering PVT variations, the amplifier response may not be accurate enough when the output voltage is closer to the limits. Thus, a practical assumption is to set V_{G-os} around 80% of the supply range ($V_{G-os} \leq 0.8(V_{DD} - V_{SS})$). As a result, the maximum achievable V_{ref} is limited to 0.46 V, and consequently, we have $b_1 \leq 0.51$.

2.4.2 Integrator-coefficients a_1 and a_2

Before realizing the behavioral simulation with a different possible combination of a_1 and a_2 , some precautions must be considered. In fact, the coefficients a_1 and a_2 have a big impact on the output dynamic range of the integrators. When they are smaller, output swing requirements are smaller, if V_{I1-os} and V_{I2-os} denote the output swing of the first and the second integrator we have:

$$V_{I1-os} \geq a_1 2V_{ref}(1 + LR), \quad (2.4.6a)$$

$$V_{I2-os} \geq \nu a_2 V_{I1-os}, \quad (2.4.6b)$$

where ν is usually more than unity quantity depending on C_{i1} , C_{s2} , and the feed forward capacitance (C_{f1}), and given by,

$$\nu = \frac{C_{i1}}{C_{s2} + C_{f1}}. \quad (2.4.7)$$

The coefficient value of the first integrator is generally less than one. According to (2.3.10c) and under the assumption that $c_1 = c_2 = 1$, the coefficient a_2 must also be lower than one. These lead to a two main observations: first, from (2.4.6a) choosing $a_1 \leq 0.8$ results in V_{I1-os} requirement of lower than 65% of the supply voltages ($V_{I-os} = 0.65(V_{DD} - V_{SS})$). This simply eases the amplifier design, which in this case can be implemented using classical OTA such as folded-cascode-OTA or class A 2-stages-miller-OTA [47]. Second, from (2.4.6b), by making $\nu = 1/a_2$, the output swing requirement of the second integrator can be the same as the first integrator ($V_{I2-os} = V_{I1-os}$). Thus, they can be implemented under the same OTA topology. In addition, to avoid the converter from overloading, the quantizer input must not exceed $(V_{Q-FS}/2 + LSB_Q/2)$ for the maximum signal amplitude $V_{in} = 2V_{ref} \cdot LR$ [48], where LSB_Q is the least significant bit of the quantizer. In fact, in a single-bit quantizer $LSB_Q/2$ is equivalent to $V_{Q-FS}/2$; thus, the underlying condition (assuming $c_1 = c_2 = 1$) leads to,

$$a_1 2V_{ref}(1 + LR) \cdot (1 + a_2) \leq V_{Q-FS} \equiv a_2 \leq \frac{1}{b_1 a_1 (1 + LR)} - 1. \quad (2.4.8)$$

Additional analysis can also be applied to the loop coefficients to illustrate their impact on the total capacitance area (C_{tot}). As discussed earlier, the integrator-coefficients a_1 and a_2 are defined as the ratios of two capacitances: C_{s1}/C_{i1} and C_{s2}/C_{i2} respectively. Where, the feedforward-coefficients (c_1 and c_2) are set by the value of one capacitor $C_{f1} = C_{f2} = C_f$ [57]. Moreover, providing directly V_{DAC} as V_{ref} eliminates the need for an extra capacitor (C_b) in the first integrator, as shown in Fig. 2.3.2(b). By inspection, the total capacitance of the modulator can be written as,

$$C_{tot} = 2C_f + C_{s1} \left(\frac{a_1 + 1}{a_1} \right) + C_{s2} \left(\frac{a_2 + 1}{a_2} \right). \quad (2.4.9)$$

Generally, the values of the capacitances C_{s2} and C_f are smaller than C_{s1} , this because the equivalent noises generated from the switching network of the second and the third stage are shaped respectively by first and second-order high-pass transfer functions. If they are smaller by a factor of $h > 2$, the expression of C_{tot} can be rewritten as,

$$C_{tot} = C_{s1} \left(\frac{a_1 + 1}{a_1} + \frac{1}{h} \cdot \frac{3a_2 + 1}{a_2} \right) = C_{s1} \cdot \lambda, \quad (2.4.10)$$

where λ represents the effect of the coefficient values on the total capacitance area used in the circuit. It is worth noting that this factor is not very accurate because of the

capacitor mismatch in integrated circuits. However, it is still sufficient at this design stage to illustrate the trade-off of the coefficient sizing. For instance, minimizing a_1 and a_2 is beneficial in term of output swing requirement (2.4.6), but leads to a larger area and higher power consumption. In Fig. 2.4.2(b), the modulator of Fig. 2.3.8 is simulated considering an $OSR = 256$ and an input amplitude of 0.57, for a_1 and a_2 go from 0.1 to 0.9 with steps of 0.05. The remaining coefficients are fixed as follow $b_1 = 0.5$, $c_0 = 0$ and $c_1 = c_2 = 1$.

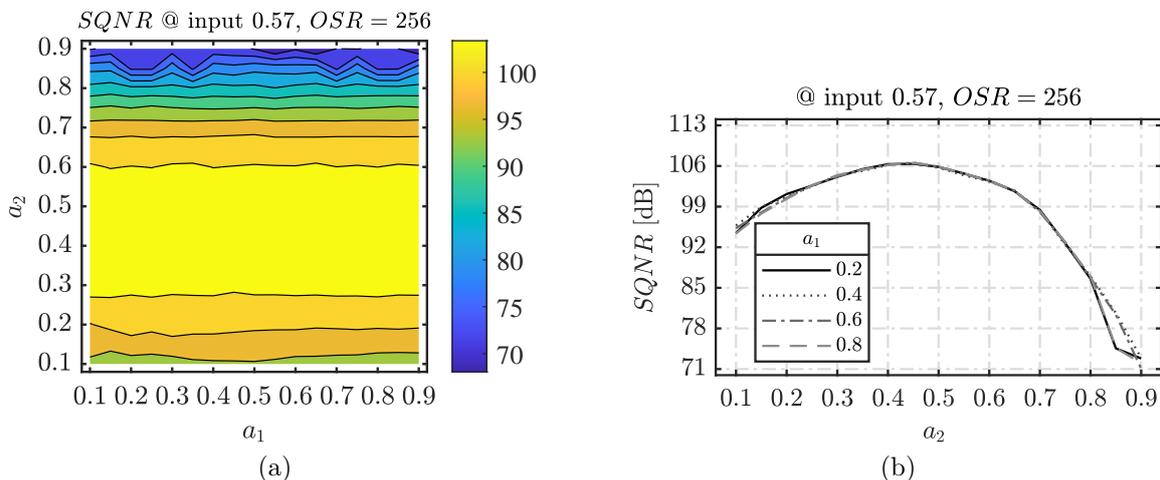


Figure 2.4.2 : Behavioral simulation to determine the coefficients a_1 and a_2 of the modulator shown in Fig. 2.3.8 for $b_1 = 0.5$, $c_0 = 0$, $c_1 = c_2 = 1$ considering an $OSR = 256$ and an input amplitude of 0.57

It can be noticed from Fig. 2.4.2(a) that the $SQNR$ changes very slowly considering a_1 , whereas it changes significantly with respect to a_2 . As an advantage, a_1 can be maximized without degrading the resolution of the modulator. Moreover, the $SQNR$ peak values are located for $0.4 < a_2 < 0.5$, where a theoretical $SQNR$ around 106 dB or $ENOB$ of 17.31 bits is achieved regardless of the a_1 values (see Fig. 2.4.2(b)). According to these results, the values of a_1 and a_2 that represent a solution for minimum area (2.4.10), maximum $SQNR$ (Fig. 2.4.2(b)), moderate output swing requirement (2.4.6), and satisfying (2.4.8) are 0.8 and 0.5 respectively.

2.4.3 Simulation results and conclusion

The bode plots of STF and NTF are depicted in Fig. 2.4.3(a). The STF plot indicates a constant gain of 6 dB (equivalent to $2 = 1/b_1$) over the band of interest (10^{-3} normalized by $f_s = 1$ MHz), this validates the assumption made in the previous section (sec.2.4) to eliminate the coefficient c_0 . The NTF has a second-order high-pass filter characteristic. It exhibits a noise shaping capacity of 5 dB more than the optimized one proposed by the automatic tools (NTF_{auto}), as shown in Fig. 2.4.3(a). This fact explains the increase of the optimized $SQNR$ presented in Fig 2.4.3(b) by approximately the same amount.

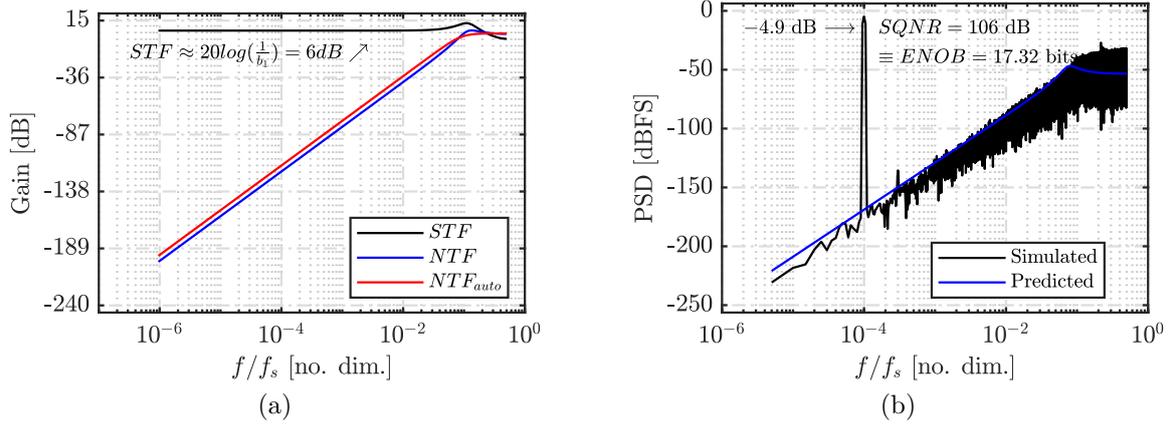


Figure 2.4.3 : Simulated transfer functions (a), and output spectrum (b), of the optimized modulator ($a_1 = 0.8$, $a_2 = 0.5$, $b_1 = 0.5$, $c_0 = 0$, and $c_1 = c_2 = 1$), considering an input sinewave of 0.1 kHz and amplitude of 0.57. The oversampling-ratio is always 256

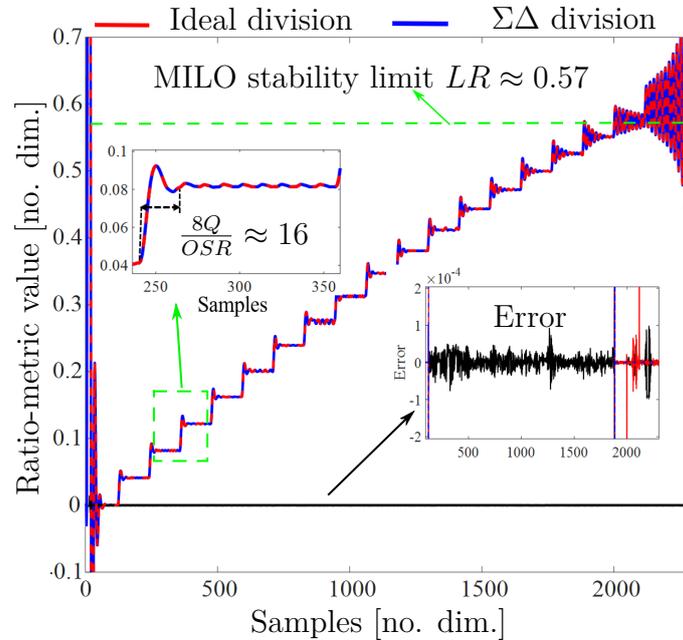


Figure 2.4.4 : Transient simulation of the system MILO + RM- $\Sigma\Delta$ M, for two identical ($Q = 500$, $f_s = 1 \text{ MHz}$). The input ϵ is applied differentially to both resonators, and stepped every $3 \cdot 10^4$ samples (normalized to $T_s = 1 \mu\text{s}$). The modulator's output bit-stream is then averaged through the decimation filter by OSR times to 117 samples (blue line), and compared with the ideal division (red line)

In Fig. 2.4.4 the system (MILO+ RM- $\Sigma\Delta$ M) is simulated with Simulink for two identical ($Q = 500$, $f_s = 1 \text{ MHz}$), linear resonators, along the system locking range. The input ϵ is applied differentially to both resonators, and stepped every $3 \cdot 10^4$ samples (normal-

ized to $T_s = 1 \mu\text{s}$) which is 7.5 times the resonators' 98% settling time ($t_r/T_s \approx 8Q$). The MILO outputs signals are then demodulated (peak sampling demodulation) and injected to RM- $\Sigma\Delta\text{M}$. The modulator output bitstream is then averaged through the decimation filter by OSR times to 117 samples. It can be indicated that the ideal and the RM- $\Sigma\Delta\text{M}$ response are perfectly matched. The residual error is limited to the "quantization white noise"; it is plotted in Fig. 2.4.5(a) as a function of the input power. As expected, the $SQNR$ attains its maximum of 106 dB for input amplitudes near $-4.9\text{dB} \approx 0.57$, while achieving a theoretical DR (2.2.2) of 103.6 dB (Fig. 2.4.5(b)).

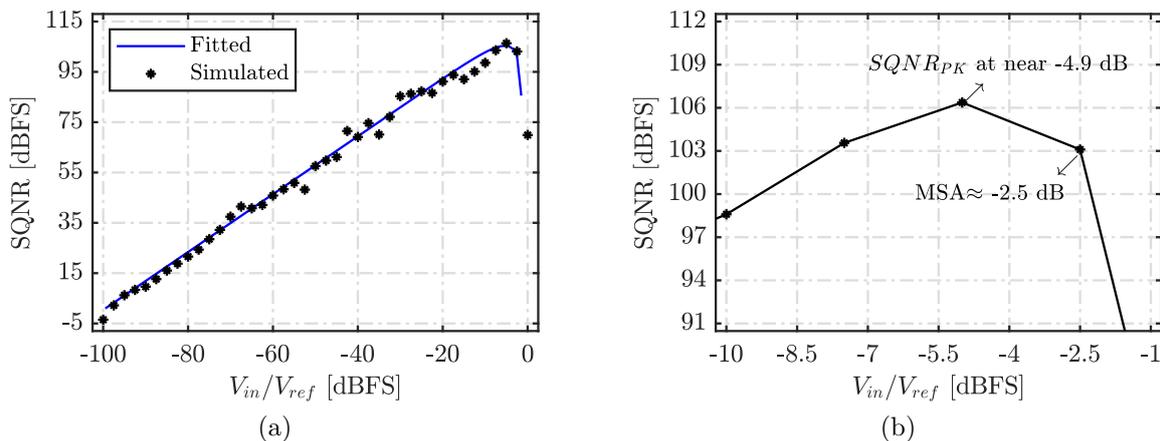


Figure 2.4.5 : $SQNR$ versus input power of the optimized modulator ($a_1 = 0.8$, $a_2 = 0.5$, $b_1 = 0.5$, $c_0 = 0$, and $c_1 = c_2 = 1$), for $OSR = 256$. The asterisks represent the values obtained from simulations and the solid line is a linear approximation of the data

Recalling that the required resolution of the modulator must be at least 16 bits when all noise sources are considered. This yields to a minimum SNR of approximately 98.08 dB that must be ensured within the temperature range. From this value, it can be observed that the quantization noise is equivalent to 16% of the total $SQNR$ loss allowable by the system ($100 \cdot 10^{(SNR-SQNR)/10}$). This implies that when the temperature reaches 125 °C, other noise sources such as $K_B T/C$ (resistance of the switches in the on-state), and circuit non-idealities (switch and OTA imperfections), must not surpass the remaining 84%. It is important to note that the non-idealities can be specified considering the preservation of the ideal response of the modulator. On the other hand, the noise sources are inherent in the DT-integrator and cannot be avoided. Hence, only 0.5 dB of $SQNR$ degradation is reserved for the circuit non-idealities, while the rest is allocated for the electronic noise.

The underlying discussion assumes that the effect of the clock jitter noise is neglected with respect to other noise sources. In fact, the jitter noise in DT modulator is $20 \log(OSR)$ times lower than the CT design. Moreover, as highlighted in Chap. 1 driving the resonators into the nonlinear regime also helps decrease the phase noise sensitivity, thus, the jitter value σ_t (2.3.7). However, the jitter noise of a MEMS based oscillator working in the nonlinear regime is not extensively studied in the literature. Considering a MEMS based oscillator working in the linear regime, the quantity $f_{MEMS} \times \sigma_t$ is around $(2.5 \sim 3) \cdot 10^{-4}$ [58]. As a result of the worst case conditions for $OSR = 256$, $f_s = 1\text{MHz}$,

and $f_{MEMS} \times \sigma_t \leq 3 \cdot 10^{-4}$, one may have $SNR_{j-DT} \geq 126$ dB, or 0.15% of the total noise.

2.5 System level consideration and electrical modeling of the analog blocks

2.5.1 Noise

As it mentioned above, the maximum $SQNR$ loss due to circuit non-idealities and to thermal noise must not surpasses 7.9 dB. If 0.5 dB is allocated to the non-idealities loss, the noise contribution of the integrators at the output of the modulator can be expressed as,

$$\overline{v_{th,out-\Sigma\Delta}^2} = \left(10^{\frac{20\log(LR)-(SQNR-7.9)}{10}} - 10^{\frac{20\log(LR)-(SQNR-0.5)}{10}} \right) \cdot V_{Q-FS}^2 \approx 133\mu V^2. \quad (2.5.1)$$

Since the noise generated from the second switched network is attenuated by the noise shaping transfer function, only the noise of the first integrator will be considered. Therefore, the equivalent referred thermal noise power at the input of the first integrator ($\overline{v_{th,in-I1}^2}$) can be written as,

$$\overline{v_{th,in-I1}^2} = \overline{v_{th,in-\Sigma\Delta}^2} = b_1^2 \cdot OSR \cdot \overline{v_{th,out-\Sigma\Delta}^2}. \quad (2.5.2)$$

A relationship between $\overline{v_{th,in-I1}^2}$ and C_{s1} can now be found by determining the total noise generated from the integrator. According to [59] the noise during the sampling phase (Φ_1) and the integrating phase (Φ_2) for a differential integrator, considering a noisy amplifier with a noise factor n_f a can be expressed by:

$$\overline{v_{th,in-I1}^2}|_{\Phi_1} = 2 \frac{K_B T}{C_{s1}}, \quad (2.5.3a)$$

$$\overline{v_{th,in-I1}^2}|_{\Phi_2} = 2 \frac{K_B T}{C_{s1}} \cdot \frac{x + \frac{2}{3}n_f}{1 + x}, \quad (2.5.3b)$$

where $x = 2R_{on}(\text{switch}) \cdot g_m(\text{pair differential})$ and n_f is defined as in [59], which is $\propto \frac{g_m(\text{active load})}{g_m(\text{pair differential})}$ of the OTA. For higher GBW and lower equivalent thermal noise, the transconductance of the input pair differential transistors is generally made larger than the active load transistors, except for some specific OTA architecture, such as current mirror amplifier [47]. As a result, $n_f \approx 1 + \frac{g_m(\text{active load})}{g_m(\text{pair differential})} \leq 2$ for an OTA having one branch load transistor, including miller compensated and telescopic cascode amplifiers,

while $n_f \approx 1 + 2 \cdot \frac{g_m(\text{active load})}{g_m(\text{pair differential})} \leq 3$ for an OTA having two branch load transistors, such as folded cascode amplifier. Considering $n_f \approx 3$ for worst case, under this condition the maximum noise power generated from the integrator (2.5.3) is when $x \rightarrow 0$. The value of the sampling capacitor the first differential integrator is therefore conditioned by,

$$C_{s1} \geq 2 \left(1 + \frac{2}{3} n_f \right) \cdot \frac{K_B T}{v_{n,th,in-I1}^2}, \quad (2.5.4)$$

and must be $C_{s1} \geq 3.8$ pF at $T = 125$ °C for $n_f \approx 3$. It is important here to note that, for $n_f = 3$, the total input referred noise of the integrator is 3/2 times larger than the noise obtained when only the switched capacitor network is considered ($4K_B T/C$). Thus, what was generally assumed to be the total noise is actually the least possible noise (for $x \rightarrow \infty$) which is not necessarily the case for a low on-resistance of the switch. This analysis is made considering a noiseless input voltage. In fact, the real input voltage is resulting from taking the peak value of the MILO output signals (see Fig. 1.5.3 for more details). Thus, any slow fluctuation of these signals will appear as a low-frequency noise, i.g., flicker noise, in the input voltage, and may degrade the resolution of the system. This issue can generally be mitigated using correlated double sampling, or chopper stabilization techniques, in the first integrator [46]. In this work, the resolution of the ratiometric interface is studied considering an ideal input voltage. However, this effect must be envisioned when implementing the entire readout interface (Amplifier, peak detector Modulator, filter.. see Fig. 1.5.3).

2.5.2 Integrator non-idealities and optimum OTA specifications

Once the architecture is selected, the next design step is to define the specifications of the modulator sub-blocks, to ensure that overall modulator performances are not degraded when designed at transistor-level. Amplifier non-idealities, including OTA finite DC-gain (A), finite GBW , limited Slew-Rate (SR), and output swing are the primary contributing sources of SNR degradation. They cause signal distortion and incomplete charge transfer in the DT-integrators. These imperfections must be modeled and inserted in high-level simulations with a relative high degree of accuracy. In this section, high level analysis and modeling of integrator non-idealities is presented. In the first part, the error caused by finite DC-gain A is modeled, and the gain specification for given modulator requirements is identified. Then, the effect of GBW and SR on the settling behavior is analyzed. Finally, the minimum output swing requirements of the integrators are specified.

2.5.2.1 OTA finite DC gain

The finite DC-gain A of the OTAs has two impacts on the modulator: a gain reduction of the STF , leading to a lower output signal power, and a pole shifting in the NTF , leading to a lower noise shaping capability. These two effects can be modeled as a magnitude and a phase leakage on the integrator ideal transfer function [57] as follow,

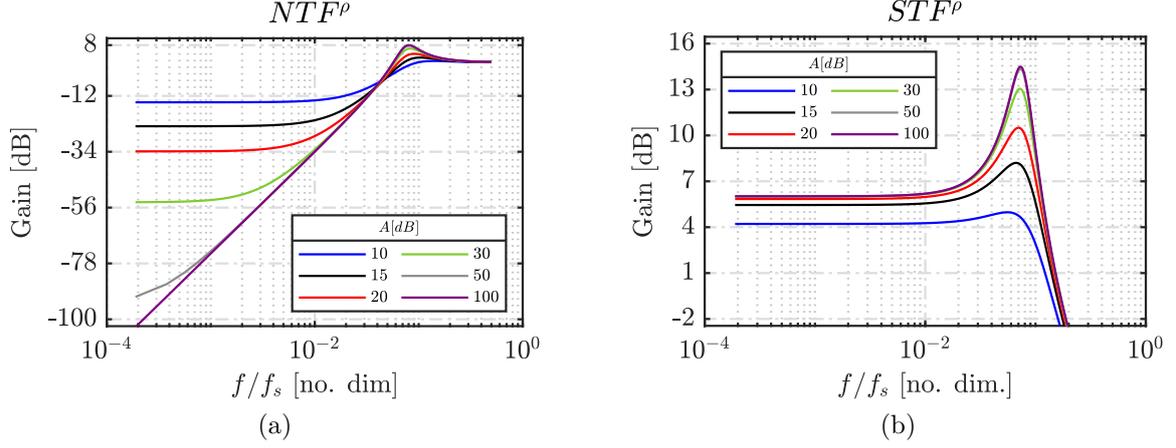


Figure 2.5.1 : Effect of the OTA finite DC-gain on the modulator transfer functions given by (2.5.6): (a) NTF^ρ , and (b) STF^ρ

$$H_i(z) = a_i \rho_i \frac{z^{-1}}{1 - \rho_i z^{-1}}, \quad (2.5.5)$$

where i denotes the integrator number and ρ is less-than-unity quantity ($\rho_i = 1 - a_i/A$) and represents the gain degradation and the filter leakage of the integrator. Using (2.3.9) the perturbed noise and signal transfer function (STF^ρ, NTF^ρ) due to finite A_0 can be written as:

$$STF^\rho(z) = \frac{a_1 \rho z^{-1} [1 + (a_2 - 1) \rho z^{-1}]}{a_1 b_1 \rho z^{-1} [1 + (a_2 - 1) \rho z^{-1}] + (1 - \rho z^{-1})^2}, \quad (2.5.6a)$$

$$NTF^\rho(z) = \frac{(1 - \rho z^{-1})^2}{a_1 b_1 \rho z^{-1} [1 + (a_2 - 1) \rho z^{-1}] + (1 - \rho z^{-1})^2}, \quad (2.5.6b)$$

where ρ is the mean value of ρ_1 and ρ_2 . The evolution of these transfer functions against finite DC-gain are depicted in Fig. 2.5.1 for A going from 10 dB to 100 dB. As expected and indicated from the plots, decreasing A leads to a gain degradation in both STF (lower gain) and NTF (higher gain) responses. The former is due to the term $(1 - \rho z^{-1})^2$ that in the conversion bandwidth becomes higher than zero leading to $STF^\rho < 1/b_1$ (Fig. 2.5.1(b)). And the later is caused by the shift of the pole placement to high frequencies that increases the NTF gain as shown in Fig. 2.5.1(a). The system resolution in term of LSB including finite A can now be expressed as,

$$LSB^\rho = 2^{\frac{1.76 - (SQNR - sqnr_{loss}^\rho)}{6.02}}, \quad (2.5.7)$$

where $sqnr_{loss}^\rho$ is a positive quantity representing the $SQNR$ loss and is expressed by,

$$\begin{aligned}
 sqnr_{loss}^p &= 20 \log \left(\frac{\langle NTF^p \rangle}{\langle NTF \rangle} \times \frac{\langle STF \rangle}{\langle STF^p \rangle} \right) \\
 &\approx 20 \log \left(\left[1 + 3 \left(\frac{OSR(1-1/\rho)}{\pi} \right)^2 \right] \times \left[1 + \frac{(1-1/\rho)^2}{a_1 a_2 b_1} \right] \right).
 \end{aligned} \tag{2.5.8}$$

It can be indicated from the above expression that the finite A entails a resolution dependency with OSR . Thus, for a required resolution and under given OSR , the appropriate A can be specified. Figure 2.5.2(a) shows the normalized least significant bit (LSB^p/LSB) for A ranges from 10 dB to 70 dB, and OSR of 64, 128, 256, and 512 respectively. It can be noted that when A is greater or equal to OSR the resolution is reduced by approximately 10%, this is equivalent to an $SQNR$ loss of only 1 dB. It can also be observed that when A is near three times OSR , around 1% LSB loss (≈ 0.2 dB) can be achieved. These results are in good agreement with [46]. For the considered application, the worst case OSR is 256; thus if the maximum allowable $SQNR$ loss due to the finite A is fixed to 0.2 dB, the gain must be $A > 3 \cdot OSR \approx 58$ dB (Fig 2.5.2(b)). This gain can be ensured using a typical folded-cascade OTA structure [60].

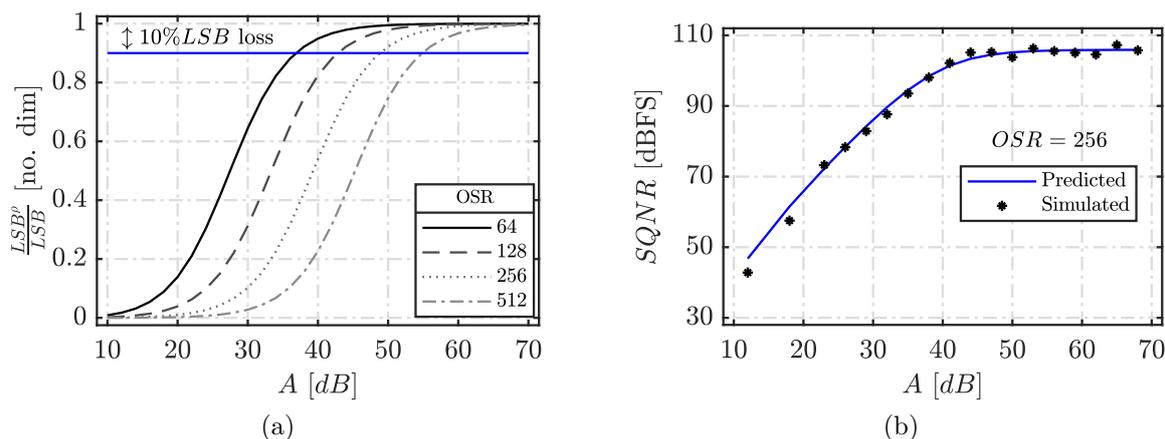


Figure 2.5.2 : Effect of the OTA finite DC gain A_0 on the resolution of RM- $\Sigma\Delta$ M; (a) loss in LSB versus A for different OSR using (2.5.8), (b) simulated versus predicted $SQNR$ for $OSR = 256$. The gain A was assumed equal in both integrators

2.5.2.2 Limited slew-rate and gain-bandwidth of the OTA

In contrast to the finite DC-gain, the effect of finite bandwidth and slew-rate of the OTA generates dynamic errors in the charge-transfer transient. This is due to the non-ideal settling behavior of the integrator and may be interpreted as a non-linear gain

[55]. Several models exist in the literature [61, 62], but they involve transistor-level parameters, which suppose a transistor-level design already existing and increase the model complexity. On the other hand, in [55, 63] a simple model of settling behavior is developed without any transistor-level parameters, which make it more attractive in the top-down design flow. This method has the advantages of reporting the settling error directly at the integrator output, avoiding the use of a complex integrator model with internal signals. However, there are issues with this technique. First, the charge distribution effect is not considered in the model. This effect, as it will be mentioned later, drives the integrator output voltage in the wrong direction, increasing the integration step, thereby affecting the settling behavior. Second, the time constant (τ_{int}) was expressed as $\tau_{int} = 1/GBW(\text{rad/s})$, where it was assumed that the GBW represents the unity-gain bandwidth of a one pole OTA when it is loaded by the integrator feedback capacitor (here denoted by C_i). However, this is the case only during the sampling phase (for a stand alone integrator), and it does not affect the settling behavior. In fact, the GBW must be determined during the integrating phase. In this time interval, the GBW is defined by the effective load capacitance (C_{load}) at the output of the integrator, which may change depending on the OTA structure (one or two stages OTA), the integrator coefficient a , and the equivalent closed-loop circuit.

These different aspects must be considered in high level model to predict the transistor-level behavior and accurately define the optimum requirements for SR and GBW . Here, a new approach based on g_m over I_d ratio (g_m/I_d) methodology is developed. It keeps the high-level advantage of the model developed in [55] while considering the charge redistribution effect and diverse possible OTA structures. Moreover, the proposed methodology addresses circuit feasibility and power consumption when determining the optimal design performance (SR and GBW). The present analysis is based on the well known Parasitic-Insensitive integrator (PI-integrator)[47]. This topology is generally preferred over others due to its immunity from charge injection error stored in the parasitic capacitors.

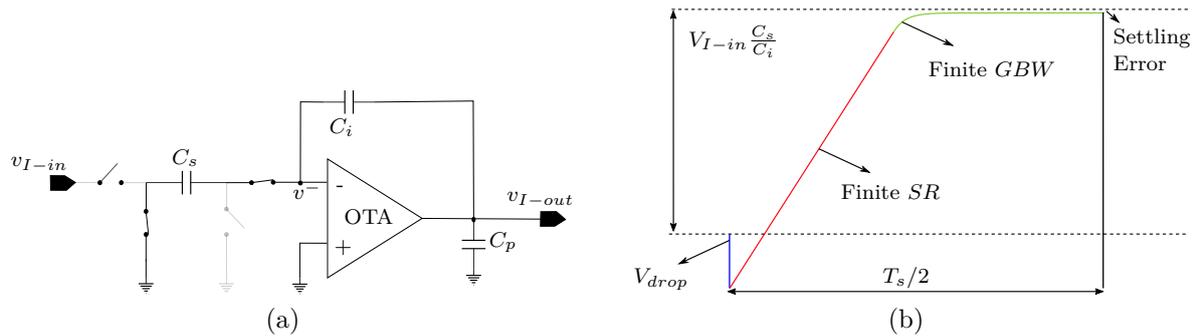


Figure 2.5.3 : Parasitic insensitive integrator (a), and its output response (b) during the integration phase

A single-ended PI-integrator during the integrating phase is presented in Fig. 2.5.3(a), where C_p is the equivalent output parasitic capacitance of the circuit. With reference to

this integrator the temporal evolution of the output voltage during the integration phase ($T_s/2 < t < T_s$) can be divided into three parts. At the starting time, a potential drop (V_{drop}) occurs due to the charge redistribution effect increasing the integration step voltage (represented by the blue line in Fig. 2.5.3(b)). Then the OTA starts acting to charge C_i according to its specifications (SR and GBW) as shown in Fig. 2.5.3(b). Firstly, the OTA is in slewing and the temporal evolution of the output voltage during the slewing time ($v_{I-out}(t \leq t_{slew})$) is linear with a slop of SR . After the slewing duration ($t_{slew} \leq t$) the output voltage follows an exponential evolution with a settling time constant inversely proportional to GBW ($\tau_{int} \propto 1/GBW$). The following equations hold assuming one pole OTA and no charges stored in C_i [55]:

$$\begin{cases} v_{I-out}(t) = -V_{drop} + SR \cdot \left(t - \frac{T_s}{2}\right) & \frac{T_s}{2} < t \leq t_{slew}, \\ v_{I-out}(t) = aV_{I-in} - (aV_{I-in} - v_{I-out}(t_{slew})) \cdot e^{-\frac{t-t_{slew}}{\tau_{int}}} & t_{slew} < t \leq T_s, \end{cases} \quad (2.5.9)$$

and,

$$t_{slew} = \frac{(1 + \alpha)}{2} T_s, \quad (2.5.10a)$$

$$V_{drop} \approx \frac{C_s}{C_s + C_p \left(1 + \frac{C_s}{C_i}\right)} \cdot V_{I-in} \equiv \frac{a}{a + e(1 + a)} \cdot V_{I-in}, \quad (2.5.10b)$$

$$SR = \left. \frac{dv_{I-out}(t)}{dt} \right|_{t=0} = \frac{I_{SR}}{C_{load}}, \quad (2.5.10c)$$

where $e = C_p/C_i$, α is the time interval allocated for the slewing duration, and I_{SR} is the SR current requirement to drive C_{load} during $\alpha \frac{T_s}{2}$. Depending on α the integrator response is partially slewing and partially exponential or completely slewing. The partial slewing response shows that the requirements on the amplifier SR and GBW evolve in an opposite way. In fact, for a higher SR , α is reduced, allowing more time for the exponential settling; this alleviate the constraint on the GBW product and visa versa. The relation between τ_{int} and GBW can be determined from the closed-loop transfer function during the integrating phase ($H_{int}(s)$), which can be written as (see appendix C),

$$H_{int}(s) = \frac{A_{int}}{1 + s \cdot \tau_{int}} \equiv \begin{cases} A_{int} = \frac{a \cdot A}{1 + a + A} \\ \tau_{int} = \frac{A/GBW}{1 + \frac{1}{1+a}A} \end{cases} \quad (2.5.11)$$

where A_{int} is the DC gain of the equivalent closed-loop circuit. Under the assumption $A \gg 1$, we retrieve $A_{int} \approx a$ and $\tau_{int} \approx (1 + a)/GBW$. Clearly, τ_{int} not only depends on the GBW as in [55], but also depends on the integrator coefficient a . One may note here that C_p does not play a role in the closed-loop transfer function. This because the driving node of the integrator is v^- and only capacitors connected to this node can perturb

the final output value [50]. C_p only acts as an extra load capacitance and increases the settling time response of the system. It worth mentioning that during the integrating phase, C_s behaves as an input current source at the node v^- . Thus, it has no impact on the effective load capacitance C_{load} seen by the amplifier. In fact, assuming a one stage OTA the equivalent output capacitance is given by,

$$C_{load} = C_i + C_p = C_i (e + 1). \quad (2.5.12)$$

From (2.5.12), it can be indicated that neglecting the parasitic capacitance ($e \approx 0$), we find $\tau_{int} = (1 + a)C_i/g_m$ instead of C_i/g_m as defined in [63]. Figure 2.5.4 compares the time response of the integrator shown in Fig. 2.5.3(a) at transistor-level (using typical folded-cascode OTA) under Cadence simulation with the presented theoretical model. The simulation is carried out considering a $GBW \approx 13$ MHz, $SR \approx 11$ MV/s, $\alpha \approx 0.15$ and $V_{I-in} = V_x^{max} = 0.72$ V. It can be indicated that the settling behavior of the presented model follows precisely the real integrator response. The only difference is the smoothed charge redistribution (lower V_{drop}) in the real case due to the switches finite on-resistance and of the parasitic capacitance at the node v^- . However, the proposed model still accurate enough to estimate the amplifier specifications. The aim is to find the optimum t_{slew} for best combination of GBW and SR that reduce the power consumption of the OTA. In fact, imposing the condition for the continuity of the derivatives of (2.5.9) in t_{slew} , and replacing τ_{int} and V_{drop} by their expressions, a first relationship between GBW , SR and t_{slew} can be obtained,

$$SR = \frac{aV_{I-in} + V_{drop} - \frac{1+a}{GBW/SR}}{t_{slew} - T_s/2}. \quad (2.5.13)$$

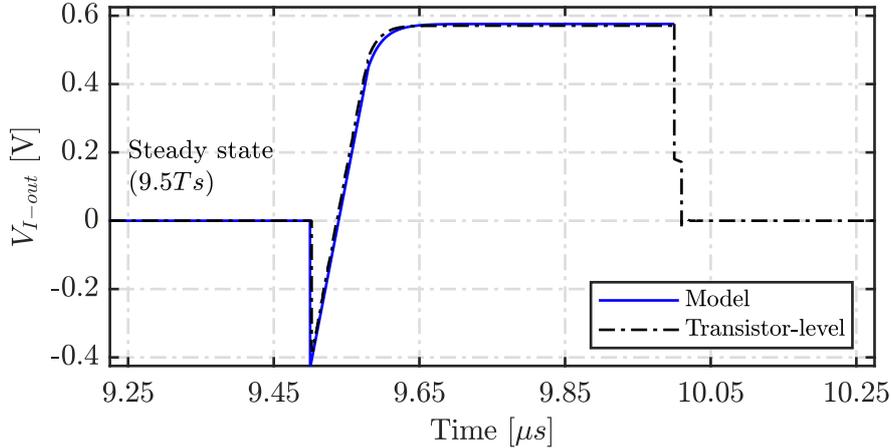


Figure 2.5.4 : Comparison of integrator response between the transistor-level circuit (using typical folded-cascode OTA) and the proposed model, considering $GBW \approx 13$ MHz, $SR \approx 11$ MV/s, $\alpha \approx 0.15$, $a = 0.8$, $e = 0.3$ and $V_{I-in} = V_x^{max} = 0.72$ V

A second relationship between these parameters can be found by imposing an output

voltage error less than $LSB/2^p$ at the end of the integrating phase. In fact, from (2.5.9) at $t = T_s$ we get,

$$GBW[\text{rad/s}] = \frac{1+a}{T_s - t_{slew}} \cdot \ln \left(\frac{2^p}{LSB} \cdot \frac{1+a}{aV_{I-in}} \cdot \frac{GBW}{SR} \right). \quad (2.5.14)$$

Depending on the OTA structure, relations between GBW , SR and g_m/I_d can be established. This relation is then inserted into (2.5.14) and (2.5.13), to find the optimum t_{slew} requirement for a given transistor operating region (g_m/I_d), resolution error ($LSB/2^p$), and sampling frequency ($1/T_s$). In practice, the driving current of the input transistors is related to the GBW (I_{GBW}) and the current through the output transistors I_{SR} set the SR requirement. There are slight differences between different amplifier structures in how GBW and SR are related for an optimum design. For instance, in single-stage fully differential (folded or telescopic cascode) OTA, the current through the input and the output branches must be kept the same for an optimal functionality ($I_{SR} \approx I_{GBW}$) [60]. On the other hand, in two stages (Miller) OTA, if it is properly compensated, the optimal operation takes place when $I_{SR} \approx (C_c + C_{load})/C_c \times I_{GBW}$ [64]. The capacitor C_c represents the compensation capacitance connected between the stages. In this work the folded-cascode OTA was preferred as it will be seen in the next chapter. In this case we have $I_{SR} = I_{GBW} = I_d$, the relation between GBW , SR and g_m/I_d is given by,

$$\frac{GBW}{SR} = \frac{g_m}{I_d}. \quad (2.5.15)$$

By dividing (2.5.14) and (2.5.13) and replacing GBW/SR by its expression (2.5.15) we find,

$$f(\alpha) = \frac{I_{GBW}}{I_{SR}} = \frac{\alpha}{1-\alpha} \cdot \frac{\ln \left(\frac{2^p}{LSB} \cdot \frac{1+a}{g_m/I_d \cdot aV_{I-in}} \right)}{\left(\frac{1+e}{a+e(1+a)} \right) g_m/I_d \cdot aV_{I-in} - 1}. \quad (2.5.16)$$

The optimum combination (or optimum t_{slew}) can be obtained by solving $f(\alpha) = 1$ for fixed design considerations (C_p , $LSB/2^p$ and g_m/I_d). In the context of DT- $\Sigma\Delta$ M, the integrators increasingly demand a trade-off between lower consumption, lower noise and good reliability to PVT variation. In fact, during the strong inversion (low g_m/I_d), it is expected to exhibit better performance in relation to parameters stability, but with higher noise [65] and higher power consumption [66]. These drawbacks can be alleviated by operating in weak inversion region (high g_m/I_d), but at the cost of reduced operation robustness in the presence of mismatch and temperature variation [66], and larger device area (aspect ratio). Thus, it is recommended to operate in moderate inversion region for a good compromise [67]. As will be shown in the next chapter, for the working technology ‘‘SOI-XH018’’ this region lies around $g_m/I_d \approx 9$.

In DT- $\Sigma\Delta$ M, C_p is mainly composed from the switched-capacitor common-mode feedback circuit (CMFB) of the OTA and from the drain-bulk capacitances of its output

transistors. The value of this capacitor is typically of the order of pF [68]. Figure 2.5.5 shows the possible solutions of the first integrator ($V_x^{max} = 0.72V, a = 0.8$) against g_m/I_d for $e = 0.3$ and considering a *LSB* error of 25%, 10%, 1% and 0.1% respectively. As expected at lower g_m/I_d values, the slewing time requirement ($\alpha T_s/2$) for a given error becomes shorter, requesting high driving current I_d . Note that, a zero α_{sol} means that the amplifier works in its normal region and is not current limited. In this case, the evolution of $v_{I-out}(t)$ is described by the second expression of (2.5.9) during the whole clock period (until $t = T_s$). Now, if the maximum allowable error at the end of the half period is fixed to 1% *LSB* (*SQNR* loss of 0.2 dB), using transistors with $g_m/I_d = 9$, the solution α_{sol} of (2.5.16) is approximately 0.21. Thus, $SR|_{\alpha=\alpha_{sol}} \approx 7.7 \text{ V}/\mu\text{s}$, $GBW|_{\alpha=\alpha_{sol}} \approx 11 \text{ MHz}$ and consequently $I_d \approx 47 \mu\text{A}$ for $C_s = 3.8 \text{ pF}$. It must be stressed that in the sampling phase C_{load} is only composed of the sampling capacitor (C_i acts as a current source) of the next integrator. This capacitance usually well smaller than the sampling capacitance of the first integrator (because of the noise requirements). Thus, if the settling error of the integration phase does not affect the modulator performance, the same applies to the settling error of the sampling phase. Moreover, this requirement is drawn only from high level model point of view. While considering a good distortion performance, e.g., process variation, and additional parasitic capacitance, e.g., input capacitance, the minimum current must be slightly larger than I_{sol} .

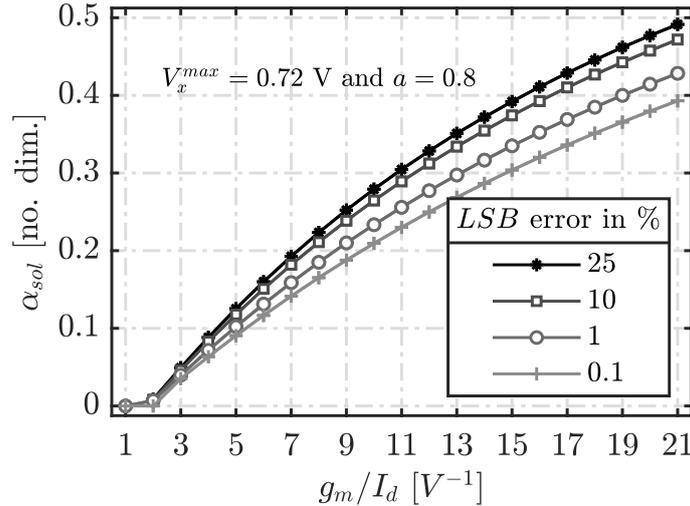


Figure 2.5.5 : Possible solution of $f(\alpha) = 1$ for the first integrator ($V_x^{max} = 0.72 \text{ V}$ and $a = 0.8$), considering different *LSB* error and $e = 0.3$

2.5.2.3 Saturation

The dynamic of signals in a $\Sigma\Delta\text{M}$ is a major concern. It is therefore important to take into account the saturation levels of the OTA that will be used. The minimum output swing of the first and second integrators can be deduced from (2.4.6), which must be higher than 1.15 V around the common mode voltage.

2.5.3 Specifications of the analog blocks

We set $C_{s2} = C_{s1}/4$, for $a_2 = 0.5$ the integrating capacitance of the second integrator is $C_{i2} = C_{s1}/2$. The OTAs used in both integrators are assumed of the same structure and implemented under the same operating point (g_m/I_d). Following the methodology developed in subsec. 2.5.2.2, the optimum GBW_2 and SR_2 are around 9 MHz and 6 V/ μ s. The biasing current of the second OTA (I_{d2}) is approximately $I_{d2} \approx I_{d1}/2.5$. According to (2.4.7), having the same output swing requirement ($V_{I1-os} \approx V_{I2-os}$), one must provide $\nu = 1/a_2$. This leads to $C_{f1} = C_{f2} \approx (a_2/a_1 - C_{s1}/C_{s2})C_{s1} = 3/8C_{s1}$. Table 2.2 summarizes the amplifiers' requirements for the first and the second integrator.

Table 2.2 : OTAs' requirements

For integrator 1	For integrator 2
$A_1 \geq 58$ dB	$A_2 \approx A_1$
$(g_m/I_d)_1 \approx 9$	$(g_m/I_d)_2 \approx 9$
$C_{s1} \geq 3.8$ pF	$C_{s2} = C_{s1}/4$
$C_{i1} = 1.25C_{s1}$	$C_{i2} = 2C_{s2}$
$I_{d1} \geq 47$ μ A	$I_{d2} \approx I_{d1}/2.5$
$GBW_1 \geq 11$ MHz	$GBW_2 \geq 9$ MHz
$SR_1 \geq 7.7$ V/ μ s	$SR_2 \geq 6$ V/ μ s
$V_{I1-os} \geq 1.15$ V	$V_{I2-os} \approx V_{I1-os}$

2.5.4 Model implementation

In order to predict the system-level behavior and help in the design procedure considering the above imperfections, two tools are generally used: Cadence/VerilogA [69, 70] and MATLAB/Simulink® [55, 63]. VerilogA is a hardware description language used for the electric modeling of analog circuits. Simulink is suitable for high-level system design, while VerilogA is preferred for integration with low-level building block implementations. Both present a good trade-off between accuracy and speed of the simulations [70], and have been widely used for $\Sigma\Delta$ non-idealities modeling [61, 69]. In this project, we decided to use VerilogA modeling language since it allows to design and model the circuit in a unified environment. Thus, it is possible to switch each building block between the ideal model, the non-ideal model, the circuit, and the physical implementation, so that the source of problems can be quickly located. The behavioral models of the amplifier and the quantizer are attached in appendix D. The description of the amplifier is based on the small signal model of single-ended structure including all imperfections (finite DC-gain and GBW , limited SR and output swing). Temperature induced variation for each parameter is also considered. For a "functional" ideal simulation, a simple amplifier model of voltage-controlled-voltage-source (vcvs) with a very high gain ($A > 100$ dB) is used. Noting that the exact model of the switch considering all non-idealities is avoided since implementing the switch with one or two transistors is easier, more accurate and hardly

preserving the same simulation time. The ideal switch model is simply designed using behavioral implementation of an “on” or “off” resistance ($R_{on} = 10\Omega$ or $R_{off} = 1G\Omega$) depending upon the control voltage. Finally, the Verilog-A description of the quantizer implement the basic function of 1-bit-ADC since the error due at this stage level can be neglected, this model is used for both ideal and non-ideal simulations. The electrical implementation of the entire RM- $\Sigma\Delta$ M schematic is then obtained by interconnecting each module using Cadence-Virtuoso® editor as depicted in Fig.2.6.1.

2.5.5 Simulation results

We performed several simulations with Cadence® on the 2nd order modulator shown in Fig. 2.6.1. Figure 2.5.6 shows the *PSD* and the corresponding *SNR* of the modulator for each case. First, in Fig 2.5.6(a), the ideal model of each component is used (ideal switch, OTA as vcvs with $A > 100$ dB and capacitor values listed in table 2.3(a)). Based on these models, the finite DC-gain effect is then evaluated for $A = 60$ dB, and the results are depicted in Fig 2.5.6(b). Next, in Fig 2.5.6(c), the vcvs are replaced by the OTA VerilogA model, including all non-idealities with the specifications summarized in table 2.3(b). Finally, in Fig 2.5.6(d), the ultimate resolution at $T = 125$ °C of noisy non-ideal modulator is evaluated by replacing the ideal switches with transmission gate switches; only the noise of the first integrator is considered. As expected, the *SNR* of the noiseless non-ideal model differs from the ideal by a value less than 1 dB (≈ 0.7 dB). Moreover, the results of the noisy non-ideal model agree with the theoretical analysis, and the main objective was achieved, which is to reach an *SNR* > 98.08 dB for $T = 125$ °C.

Table 2.3 : Parameter values used in the simulation

Capacitor	Value	Simulation values	
		For integrator 1	For integrator 2
C_{s1}	4 pF	$A_1 = 60$ dB	$A_2 = 60$ dB
C_{i1}	5 pF	$g_m/I_d = 9$	$g_m/I_d = 9$
C_{s2}	1 pF	$I_{d1} = 50 \mu\text{A}$	$I_{d2} = 20 \mu\text{A}$
C_{i2}	2 pF	$V_{I1-os} = 1.2$ V	$V_{I2-os} = 1.2$ V
C_{f1} and C_{f2}	1.5 pF		

(a)

(b)

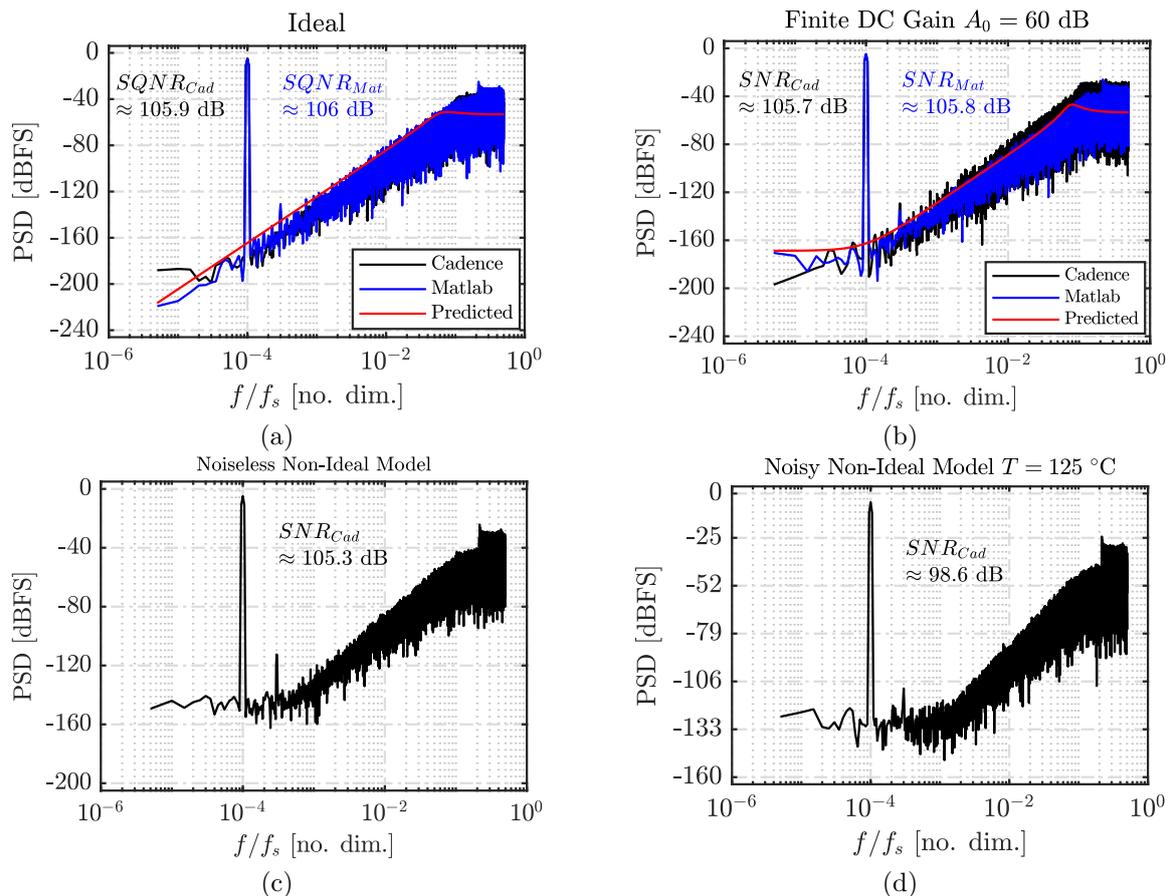


Figure 2.5.6 : PSD of the output signal obtained from Cadence® simulation: (a) ideal, (b) ideal with finite DC-gain $A = 60$ dB, (c) non-ideal model, and (d) noisy non-ideal model at $T = 125$ °C

2.6 Conclusion

Firstly, the performance metrics to characterize $\Sigma\Delta M$ are introduced in this chapter. Then the basic operation principle of the $\Sigma\Delta M$ is presented by explaining oversampling and noise-shaping concepts. Next, a comparative study including implementation domain, loop order, filtering mode, and loop topology was investigated. It has been found that, the most appropriate architecture for the application considered in this thesis can be obtained using the following structure “FF-2^{ed}-1-bit-DT- $\Sigma\Delta M$ ” which abbreviated to RM- $\Sigma\Delta M$. An optimization step of the loop coefficients was next done to meet the specifications of a theoretical resolution > 16 bits and a maximum stable amplitude larger than 0.57. Finally, the non-idealities of the integrator, which is the major source of errors in a single-bit architecture, were characterized and specified in order to not degrade the theoretical performance of more than 0.5 bit when temperature up to 125 °C. The specifications were validated using verilogA model using Cadence Spectre® simulation. The

next chapter describes the design of the analog circuits and lists the transistor dimensions. The procedure to obtain the final transistor dimensions is based on local analysis and refined using Spectre/simulations.

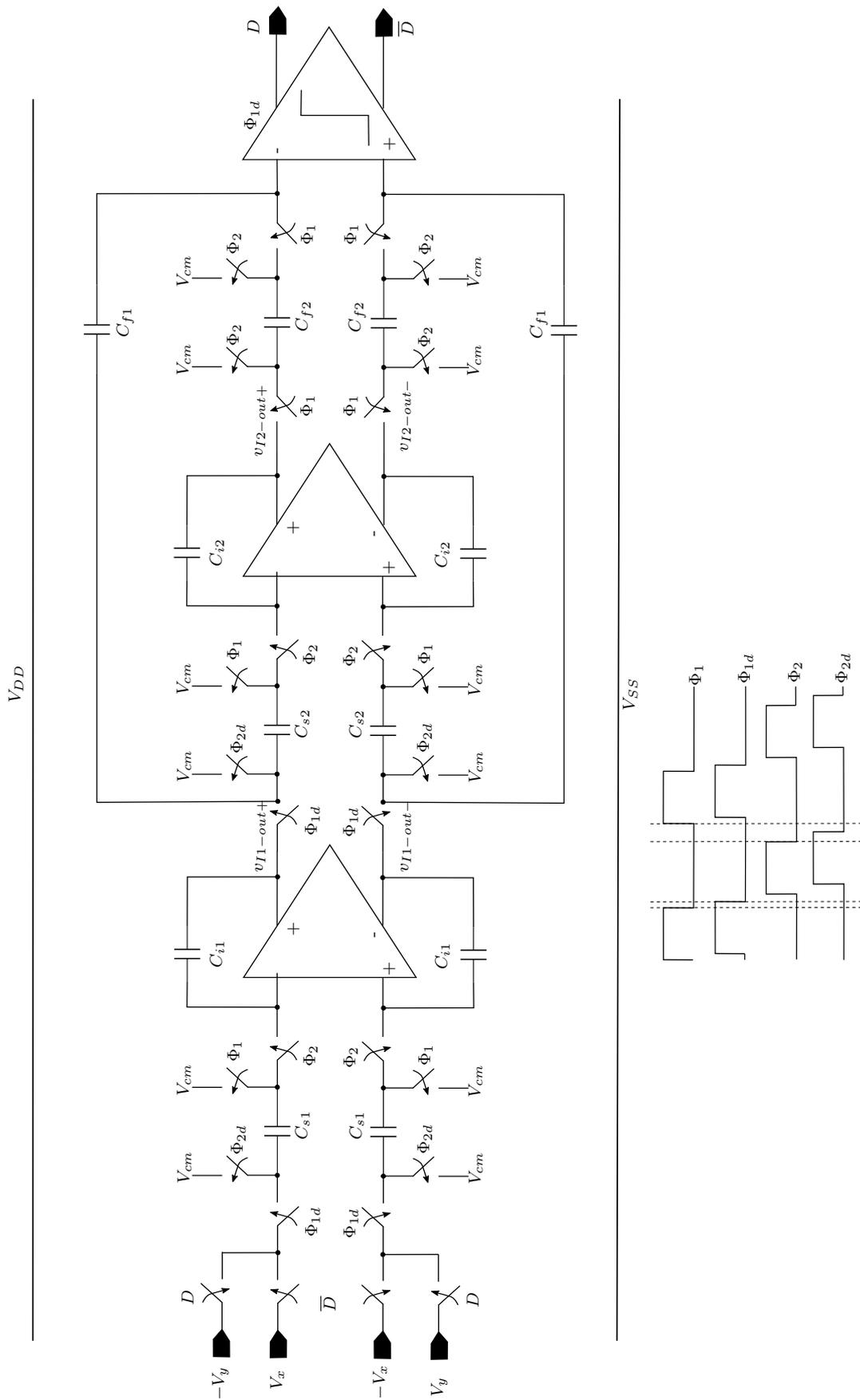


Figure 2.6.1 : Ratiometric fully differential second order feedforward modulator

Chapter 3

Circuit level design of the sigma delta modulator

This chapter describes the transistor level design of the analog circuits used in the proposed fully differential modified RM- $\Sigma\Delta$ M shown in Fig. 2.6.1. It first presents the design of the switch used in the modulator. The switch is based on transmission gate (TG) architecture to overcome the limitations of the ordinary switch design based on a single transistor. Second, it presents an overview of the most popular OTA architectures. It will be shown that considering the required specifications, the folded-cascode OTA structure is the appropriate choice. Since the amplifier is the most crucial building block in the modulator, the selected OTA must be designed to work with high thermal stability. For this purpose, an original thermal stability analysis using the g_m/I_d methodology is proposed. It highlights the optimum operating conditions of the main transistor "small-signal" parameters g_{ds} and g_m , and the quiescent current I_d . Third, the OTA biasing circuit is described. This circuit is based on wide-swing-cascode-current-mirror structure that enhances the output swing of the amplifier. The transistors constituting the biasing circuit are also designed to work under the same condition, i.e. g_m/I_d as the OTA for high thermal stability. Next, the input 1-bit-DAC integrator is discussed. Since the sensor may have a single or differential output, single to differential and fully differential integrator implementations are investigated. Both are DT designed and are, parasitic insensitive and have the same noise performance. Finally, the double tail latched comparator, and the non overlapping clock are detailed.

The design of the circuits are done using standard supply voltages of 1.8 V, and prioritizing the circuit reliability of PVT variation over the area and power consumption. The procedure to obtain the transistor dimensions is first based on transistor-level analysis of the circuit, and then refined by Spectre simulations using Cadence/Virtuoso. The post-layout simulation results and PVT analysis are, however, detailed in the next chapter.

In this work, the Silicon-On-Insulator CMOS (SOI) module of XH018 process technology from the X-FAB Silicon Foundries has been chosen. It is ideal for system-on-chip

applications in the automotive market such as control devices inside combustion engine compartments or electric engine housings with a temperature up to 175 °C, as well as embedded low-voltage applications in the communications, consumer, and industrial market [16]. Such technology is an SOI process, which uses a deep-trench buried oxide that leads to a very low junction leakage current even at high temperatures. According to foundry models, it is reported 3 pA of leakage current for measured transistors with 10 nA of drain-to-source bias current and 100 pA leakage for 80 μA bias current at 175 °C.

3.1 Switch

The requirements for switches used in SC-circuits are having a very high R_{off} resistance (to minimize charge leakage), and a relatively low R_{on} resistance (to charge the capacitance with less than half period). According to the required 16 bits resolution, one may assume that at least an error of 1% LSB (0.2 dB) due to the incomplete charge transfer in C_{s1} is tolerable. As a result, the on-resistance R_{on} of the switch is conditioned by,

$$2R_{on}C_{s1} \cdot \ln(10^2/LSB) < T_s/2 \equiv R_{on} < 3.9k\Omega. \quad (3.1.1)$$

Generally, a switch can be designed using one MOSFET (PMOS or NMOS) transistor, for which the on-resistance can be expressed as:

$$R_{on}^N \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{thn} - V_{in})}, \quad (3.1.2a)$$

$$R_{on}^P \approx \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{SS} + |V_{thp}| - V_{in})}, \quad (3.1.2b)$$

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W/L is the aspect ratio. The simulated on-resistance of PMOS and NMOS switch as a function of input voltage V_{in} are illustrated in Fig. 3.1.1(a), considering $L = 0.18\mu m$, $W_n = 2\mu m$, $W_p = 6\mu m$, and V_{in} going from 0.2 to 1.6 V. It can be indicated that R_{on} strongly depends on the input signal, yielding a greater resistance (greater time constant) for more positive (NMOS red line in Fig. 3.1.1) or negative (PMOS blue line in Fig. 3.1.1) inputs. In addition, the allowable signal range of these devices is restricted by the threshold voltage (V_{th}): greater than $V_{SS} + |V_{thp}|$ for PMOS transistor, and lower than $V_{DD} - V_{thn}$ for NMOS transistor.

Although the switch still conducts at these limits, the corresponding R_{on} becomes significantly large, leading to incomplete charge transfer to the sampling capacitor. Considering the modulator input range that was specified in (2.4.4) from 0.18 V to 1.62 V. If a NMOS switch is used, the R_{on}^N at the maximum input voltage is roughly 10 kΩ (not shown in

3.1.1(a)). This value is more than twice the required one, and may also be larger considering PVT variations (as will be seen in the next chapter). The same issue is observed using a PMOS switch, but in this case R_{on}^P is high at the minimum input voltage.

The underlining limitations can be mitigated by employing NMOS and PMOS transistors back to back, whose gates are driven with a complementary signal clock as shown in Fig. 3.1.2(a). This alternative is commonly called CMOS Transmission-Gate (TG) or bilateral switch. In fact, the on-resistance of both transistors are connected in parallel ($R_{on}^{TG} \approx R_{on}^N || R_{on}^P$). They act in a complementary way, allowing a rail-to-rail input swing around the common mode voltage, i.e. 0.9 V, and compensates the effect of the input signal variation. In other word, this combination results in a "lower", and "relatively stable" equivalent on-resistance R_{on}^{TG} , regardless of the input level as shown in Fig. 3.1.1(a). These properties make TG switch suitable for differential implementations.

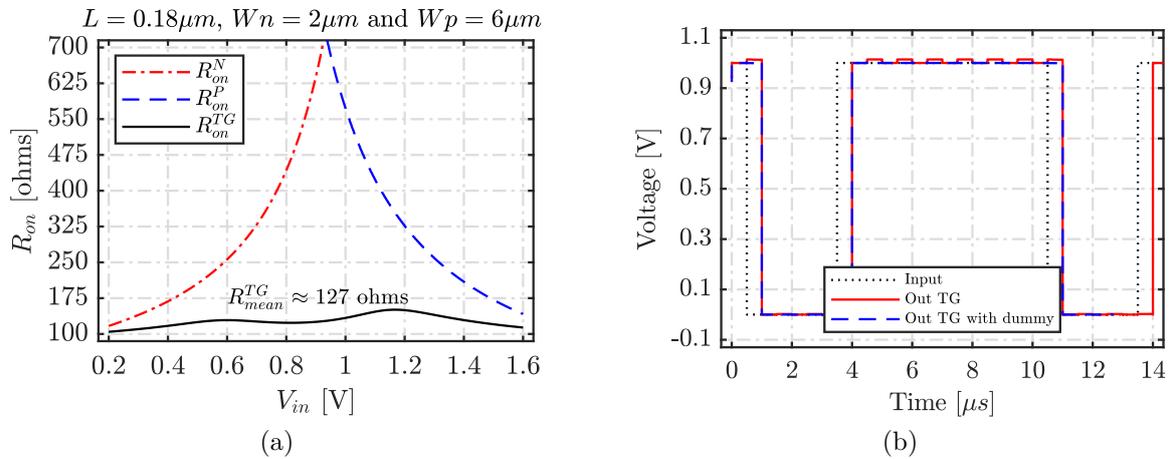


Figure 3.1.1 : (a) NMOS, PMOS, and CMOS-TG on-resistance R_{on} comparison, considering an input voltage going from 0.2 to 1.6 V, (b) output voltage of the TG with and without dummy transistors considering 1V input signal. The simulations are carried out for: $V_{DD} = 1.8V$, $L = 0.18\mu m$, $W_n = 2\mu m$ and $W_p = 6\mu m$ (the width of dummy transistors are half of the switch transistors)

In order to reduce the clock feed-through, and channel charge injection, the transistors M_1 and M_2 must have minimum dimensions [47]. The effects of these non-idealities can also be alleviated using "dummy" TG on both sides of M_1 and M_2 as schematically shown in Fig. 3.1.2(b). The advantage of this technique can be directly seen from Fig. 3.1.1(b), where no voltage error due the integration of the undesired charges in the channel is observed (red full line). The dimensions of the transistors M_a , M_b , M_c and M_c are typically half those of M_1 and M_2 . Table 3.1 lists the transistor sizes of the TG implemented in the RM- $\Sigma\Delta M$. Under these dimensions the the maximum on-resistance is $R_{max}^{TG} \approx 150\Omega$, the maximum time constant to charge C_{i1} is therefore $t_{charge} = 2R_{max}^{TG} \times C_{s1} \cdot \ln(10^2/LSB) \approx 18.8$ ns which is much lower than $T_s/2$.

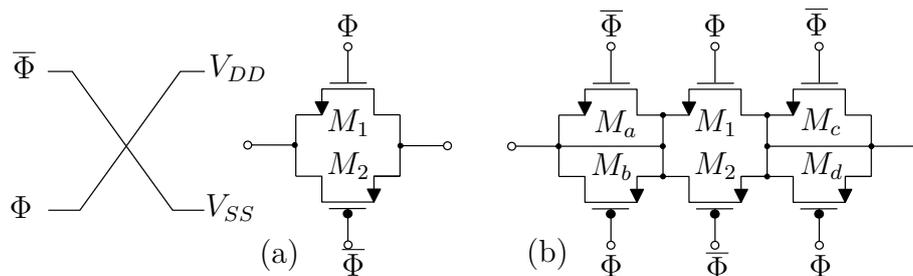


Figure 3.1.2 : Transmission gate switch, (a) ordinary, (b) with dummy transistors

Table 3.1 : Switch transistor dimensions

Device	W [μm]	L [μm]
M_a, M_c	1	0.18
M_b, M_d	3	0.18
M_1	2	0.18
M_2	6	0.18

3.2 Operational transconductance amplifier 'OTA'

In SC-circuits, the amplifiers are usually operational transconductance amplifiers OTA since the output is a current that charges a load capacitor. There are two main categories of the OTAs: single-stage structures such as Telescopic-Cascode (TC), Folded-Cascode (FC), and Current-Mirror (CM), or two-stage structures including Load-Compensated (LC), and Miller-Compensated (MC) design. Simplified fully differential implementation schematics of these OTAs (CMFB not shown) are depicted in Fig. 3.2.1. The comparison between these architectures, as well as the appropriate design choice for the considered application are discussed in the following subsection. Afterwards, the selected OTA will be temperature aware designed using g_m/I_d methodology, and optimized for maximum efficiency as in [60].

3.2.1 OTA design comparison

The two-stage OTAs consist of differential input stage producing high gain, and common source structure as output stage providing a high and flexible output voltage swing (Fig. 3.2.1(a)(b)). OTA's second stage also increases the gain that may up to some certain extent compared to single-stage OTAs. However, this addition also increases complexity including, compensation circuit to stabilize the frequency response of the OTA.

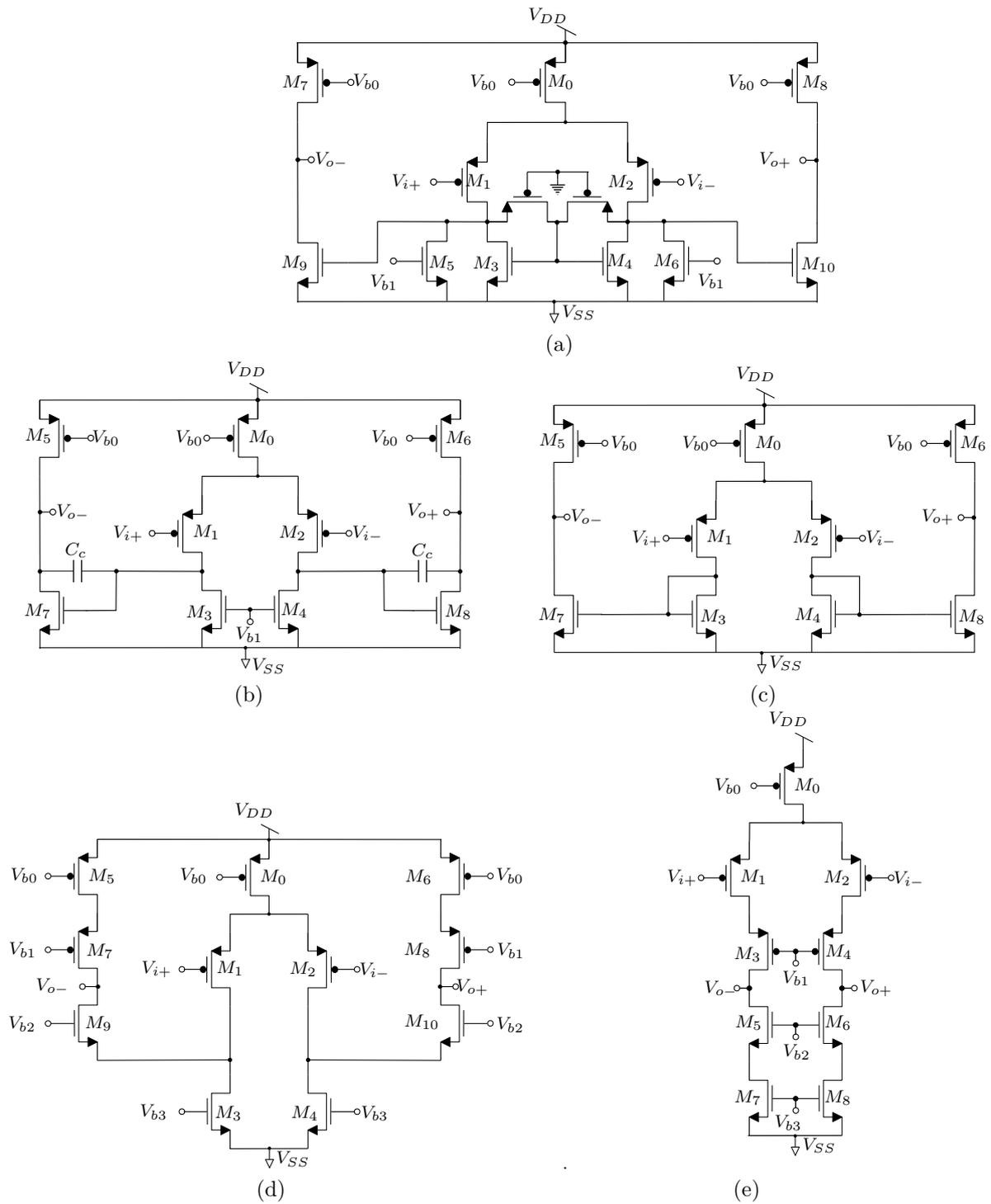


Figure 3.2.1 : OTA architectures, (a) Load-Compensated (LC), (b) Miller-Compensated (MC), (c) Current-Mirror (CM), (d) Folded-Cascode (FC), and (e) Telescopic-Cascode (TC)

MC compensation is implemented in the circuit by placing a pole splitting capacitor C_c between the stages (see Fig. 3.2.1(b)). However, this capacitor increases the effective load capacitance of the integrator, leading to a larger area, and higher current requirement in the output stage for a given SR [64]. LC-OTA structures as the one depicted in Fig. 3.2.1(a) eliminates the need of C_c [71], but at the cost of more power consumption. Moreover, the GBW in LC is function of the drain-to-source transconductance (g_{ds}) of the first stage composed by $M_{1(2)}$, $M_{3(4)}$ and $M_{5(6)}$. This fact makes it less suitable for temperature aware design perspective (it is more complicated to compensate the variation of g_{ds} compared to that of g_m).

TC-OTA compensates the drawback of two-stage OTA by stacking two transistors ($M_{5(6)}$ and $M_{7(8)}$) as shown in Fig. 3.2.1(e)) to form a cascode structure [47]. It produces higher gain and better frequency response with relatively low power consumption compared to two-stage OTA. However, stacking two transistors on the output active load transistors (M_3 and M_4) substantially reduces the output voltage swing of the amplifier. In fact, the output swing of TC-OTA is considered as the lowest one among all structures. Another disadvantage of the TC-OTA is that the common-mode voltage at the input and the output can not be set to the same value. This is a major drawback that limits the use of such OTA in a closed-loop configuration.

The FC-OTA structures (Fig. 3.2.1(d)) overcomes the difficulty in shorting the input and output, while providing a higher output swing compared to TC-OTA. The gain of the FC is slightly lower than the TC, because $M_{3(4)}$ appears in parallel with $M_{1(2)}$; thus, the output impedance is reduced. However, this can be mitigated using larger devices (L) in the output branches. FC has also reduced power efficiency due to the use of two separate bias currents compared to the bias current in TC that is shared in the same branch.

As for CM-OTA, this topology is considered as a single-stage OTA as it has one differential input pair and differential current mirror structures (see Fig. 3.2.1(c)). It is usually applied in a wide range applications as it produces high output impedance, transconductance multiplier capability, and low power consumption [47]. Meanwhile, it suffers from larger thermal noise compared to a FC-OTA because its input transistors are biased at a small portion of the total bias current and therefore have a smaller transconductance [47].

In this work, the FC-OTA topology has been preferred, since it offers the best compromise among all structures. This architecture can also adapted to our requirements (summarized in Table 2.2), DC-gain $A > 58dB$, moderate output swing $V_{I-os} = 1.15$ V, suitable for closed loop configuration, and unconditionally stable without adding a compensation capacitor. The design optimization using g_m/I_d methodology of the FC-OTA structure, including temperature variation, is presented in the following subsection.

3.2.2 g_m/I_d design considerations

The efficiency of the amplifier is strictly related to its, speed ($GBW \propto g_m$), power consumption (I_d) and total area. It is important here to note that the selected FC-OTA will be implemented with PMOS input pair devices, and only two transistors are of NMOS type (M_3 and M_4). Thus, a large amount of the following analysis is done considering a PMOS transistor. The OTA analytical analysis is based on the Unified Current Control Model (UICM) suitable for analog integrated circuit design; in this model, the drain current in the active forward region for long channel MOSFET transistor is given by [72]:

$$I_d = n_{th}\phi_t g_m \cdot \left(1 + \frac{g_m}{2\mu C_{ox}\phi_t(W/L)}\right) \equiv n_{th}\phi_t g_m \cdot \left(\frac{1 + \sqrt{1 + i_d}}{2}\right), \quad (3.2.1a)$$

$$i_d = I_d/I_S \text{ and } I_S = \frac{n_{th}}{2}\mu C_{ox}\phi_t^2 \frac{W}{L}, \quad (3.2.1b)$$

where n_{th} is the sub-threshold slope factor, and $\phi_t = K_B T/q$ is the thermal voltage; at room temperature ($T_0 = 27^\circ\text{C}$) $n_{th} \approx 1.45$ and $\phi_t \approx 26\text{mV}$. i_d is the forward normalized current, and I_S is the specific current that is technology dependent parameter. i_d is also called inversion coefficient since it indicates the inversion level of the device. i_d values of greater than 100 characterize strong inversion. The transistor operates in weak inversion with i_d up to 1. Intermediate values of i_d , from 1 to 100, indicate moderate inversion. Alternatively, one may write the current I_d and the aspect ratio W/L as a function of the transistor "strength" g_m versus g_m/I_d , in fact from (3.2.1):

$$I_d = 2n_{th}g_m\phi_t \cdot \beta_{I_d}, \quad (3.2.2a)$$

$$\frac{W}{L} = \frac{g_m}{2\mu C_{cox}\phi_t} \cdot \beta_{WL}. \quad (3.2.2b)$$

The factors β_{I_d} and β_{WL} are dimensionless quantity describing how I_d and W/L are related to g_m for a given operation region g_m/I_d . They are given as:

$$\beta_{I_d} = \frac{1}{2g_m/I_d \cdot n_{th} \cdot \phi_t}, \quad (3.2.3a)$$

$$\beta_{WL} = \frac{n_{th} \cdot \phi_t}{\left(\frac{1}{g_m/I_d} - n_{th} \cdot \phi_t\right)}. \quad (3.2.3b)$$

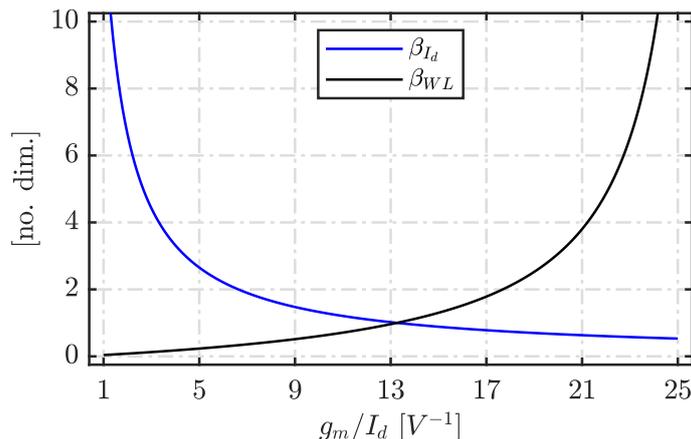


Figure 3.2.2 : β_{I_d} and β_{W_L} as a function of g_m/I_d . $n_{th} \approx 1.45$ and $\phi_t \approx 26$ mV

The expressions of β_{I_d} and β_{W_L} are valid for any inversion level: weak, moderate, or strong inversion [72]. These coefficients are plotted in Fig. 3.2.2 as a function of g_m/I_d for $n_{th} \approx 1.45$ and $\phi_t \approx 26$ mV. A trade-off between area and power consumption can be reached by an appropriate choice of g_m/I_d . It is important to note that working in weak inversion region, with g_m/I_d larger than 20, leads to a prohibitively high aspect ratio for a negligible reduction in power consumption. In strong inversion region, precisely for g_m/I_d lower than 5, a higher current can be achieved with a low aspect ratio; this is usually the case for the current biasing transistors. However, working in deep saturation region with very low g_m/I_d leads to a larger saturation voltage and hence a lower voltage swing. This trade-off must be considered in low power design. Moderate inversion region offers the best compromise between aspect ratio and power consumption for a stronger device (high g_m); thus, the amplifier pair differential are polarized to work in this region.

Let us now consider the temperature-induced variation on the current I_d and the transconductance g_m . This variation is mainly due to the threshold voltage $V_{th}(T)$ and the carrier mobility $\mu(T)$. The temperature dependence of these factors can be modeled by the following expression [67]:

$$V_{th}(T) = V_{th}(T_0) - |\alpha_{V_{th}}| \cdot (T - T_0), \quad (3.2.4a)$$

$$\mu(T) = \mu(T_0) \cdot \left(\frac{T}{T_0}\right)^{\alpha_\mu}, \quad (3.2.4b)$$

where $\alpha_{V_{th}}$ is the thermal coefficient of the threshold voltage, and α_μ is the temperature dependence power coefficient for the mobility. Assuming a temperature variation δT

around T_0 , the expression of $g_m(T)$ and $I_d(T)$ can be expressed as follow:

$$g_m(T) = g_m(T_0) + \left. \frac{\partial g_m}{\partial T} \right|_{T_0} \cdot \delta T, \quad (3.2.5a)$$

$$I_d(T) = I_d(T_0) + \left. \frac{\partial I_d}{\partial T} \right|_{T_0} \cdot \delta T. \quad (3.2.5b)$$

The temperature sensitivity $\left. \frac{\partial g_m}{\partial T} \right|_{T_0}$ and $\left. \frac{\partial I_d}{\partial T} \right|_{T_0}$ can be readily derived from (3.2.1) and (3.2.4), which in term of $g_m/I_d|_{T_0}$ can be written as [67]:

$$\frac{T_0}{g_S} \cdot \left. \frac{\partial g_m}{\partial T} \right|_{T_0} = 2(\alpha_u(2\beta_{I_d} - 1) - 1) + \frac{1}{1 - 1/\beta_{I_d}} \cdot \left(\frac{|\alpha_{V_{th}}| \cdot q}{n \cdot K_b} + 2 - \ln(4\beta_{I_d} - 2) \right) = S_{g_m}^T, \quad (3.2.6)$$

$$\begin{aligned} \frac{T_0}{I_S} \cdot \left. \frac{\partial I_d}{\partial T} \right|_{T_0} = & 8\beta_{I_d} \cdot \left(\frac{|\alpha_{V_{th}}| \cdot q}{n \cdot K_B} + 3 - 4\beta_{I_d} - \ln(4\beta_{I_d} - 1) \right) \\ & + 2(\alpha_\mu + 1) \cdot ((4\beta_{I_d} - 1)^2 - 1) = S_{I_d}^T, \end{aligned} \quad (3.2.7)$$

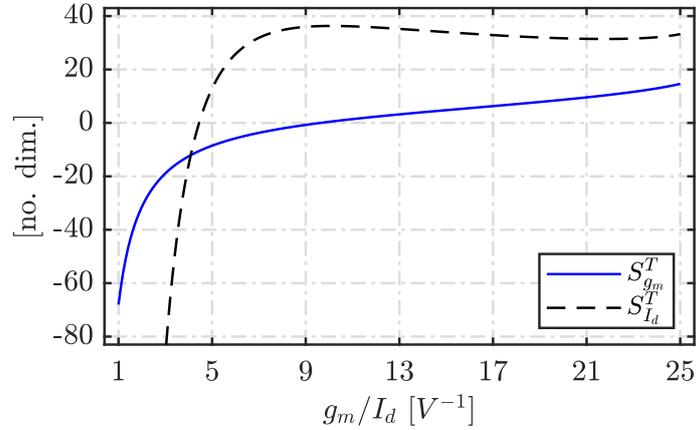


Figure 3.2.3 : Normalized current and transconductance sensitivity $S_{I_d}^T$ and $S_{g_m}^T$ as a function of g_m/I_d

where $g_S = 2I_S/n_{th}$. The coefficients $S_{g_m}^T$ and $S_{I_d}^T$ are normalized quantity represent the temperature sensitivity of g_m and I_d respectively. The threshold and mobility temperature coefficients are extracted from simulation and they are $\alpha_\mu \approx -1.35$ and $\alpha_{V_{th}} \approx -0.6$ mV/°C. $S_{g_m}^T$ and $S_{I_d}^T$ are plotted in Fig. 3.2.3 as a function of g_m/I_d . It can be indicated that the sensitivity of both I_d and g_m increase as g_m/I_d increases. The minimum $S_{I_d}^T$ can be achieved in strong inversion region for $4 \leq g_m/I_d \leq 6$, and the zero temperature

coefficient $S_{I_d}^{ZTC}$ is achieved for $g_m/I_d \approx 4.5$. While $S_{g_m}^T$ is optimum in the moderate inversion region, typically for $7 \leq g_m/I_d \leq 12$, while achieving a $S_{g_m}^{ZTC}$ for g_m/I_d close to 9.

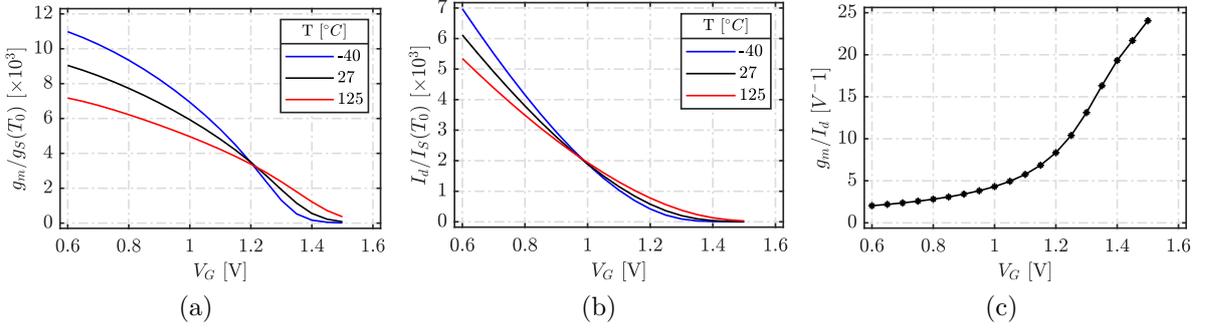


Figure 3.2.4 : Simulated PMOS parameters versus gate voltage V_G under the three temperatures -40, 27, and 125 °C, (a) g_m , (b) I_d , and (c) g_m/I_d biasing condition at room temperature. The size of the transistor is $W \times L = 10 \times 3 \mu\text{m}^2$, and simulated considering $V_{DS} = V_{DD}/2$

In order to validate the above analysis, a PMOS transistor with $W \times L = 10 \times 3 \mu\text{m}^2$ is simulated for $V_{DS} = V_{DD}/2$ versus the gate voltage V_G from 0.6 to 1.5 V. The results at the three temperatures -40, 27, and 125 °C are depicted in Fig. 3.2.4(a) for g_m/g_s , Fig. 3.2.4(b) for I_d/I_s and Fig. 3.2.4(c) for $g_m/I_d|_{T_0}$ as a function of V_G . It can be indicated that the polarity of the temperature sensitivity of g_m and I_d change around $V_G = 1.2$ V and $V_G = 0.97$ V respectively. These values correspond to $g_m/I_d|_{T_0}$ of 8.8 and 4.7 for g_m and I_d respectively. It can also be indicated that in strong inversion region, the drift induced change on g_m and I_d is more important than in weak inversion and showing a negative variation. Although the UICM model may not be very accurate in deep strong inversion level under temperature variation, the simulation results are in a good agreement with the proposed g_m/I_d model of $S_{g_m}^T$ and $S_{I_d}^T$, expressed by (3.2.6), (3.2.7), and illustrated in Fig. 3.2.3.

The drain source transconductance g_{ds} is also a critical parameter that defines the DC-gain of the amplifier. The modeling of g_{ds} needs to be handled with little more attention since, in opposition to the g_m and I_d parameters, this parameter is very sensitive to channel length effects. The significant short channel effects controlling the drain to source transconductance are, drain induced barrier lowering, velocity saturation, and channel length modulation.

The drain induced barrier lowering is a 2D effect that includes the decreases in the carriers barrier when the drain voltage V_D increases and L decreases, i.e., reduction of the PN barrier between source and gate. This entails a reduction in the threshold voltage $V_{th}(V_{DS})$, usually modeled as a linear relationship between the classic threshold voltage V_{th0} and V_{DS} : $V_{th}(V_{DS}) = V_{th0} - \sigma_L V_{DS}$, where σ_L is $\propto 1/L^m$ can be directly extracted from simulation as in [21]. Second, with the decrease of channel lengths, the electric fields are hugely increased, giving carriers more energy and increasing the probability of

scattering events. The increase of scattering limits the maximum electric field on the channel to a value E_{sat} . This saturation makes the transition between the linear and saturated regimes occur earlier than the classical limit. The corresponding saturation voltage V_{sat} is usually considered constant ($V_{sat} \approx L \cdot E_{sat}$) [73]. However, V_{sat} is also depends on V_{GS} , in [74] V_{sat} is defined as $2I_d/g_m$. Thus in order to account for both effects V_{sat} will be expressed as in [75]. Finally, when the drain to source voltage exceeds V_{sat} , the pinch-off region starts to grow towards the source, making the effective channel length decrease with the increase of V_{DS} . Thus, by accounting for all these effects, g_{ds} can be expressed by [21],

$$g_{ds} = I_d \left(\frac{\frac{g_m}{I_d} L \cdot E_{sat} + 2}{\alpha_L (V_0 + V_{DS}) \left(\frac{g_m}{I_d} L \cdot E_{sat} + 2 \right) - 2L \cdot E_{sat}} + \sigma_L \frac{g_m}{I_d} \right) \quad (3.2.8)$$

where $V_0 \approx 0.433$ V is a constant model parameter [21] and α_L is the channel length modulation factor, modeled in [76] and plotted in Fig.3.2.5 as a function of L considering the working technology [21].

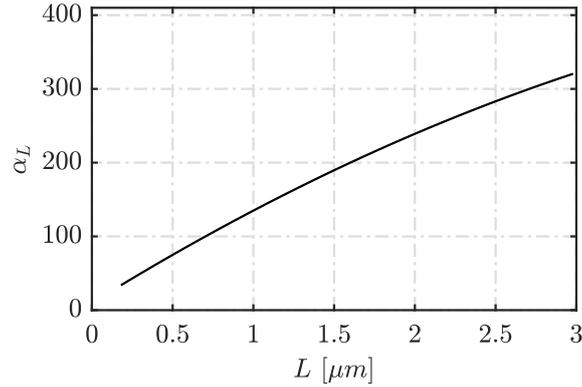


Figure 3.2.5 : α_L versus L for the working technology

Following the same approach made in deriving (3.2.5a), the temperature normalized sensitivity of g_{ds} ($S_{g_{ds}}^T$) can be readily derived from (3.2.8). By inspection we found,

$$\begin{aligned} \frac{T_0}{g_{DS}} \cdot \frac{\partial g_{ds}}{\partial T} \Big|_{T_0} = & \frac{\frac{g_m}{I_d} + \frac{2}{L \cdot E_{sat}}}{\left(\frac{g_m}{I_d} + \frac{2}{L \cdot E_{sat}} - \frac{2}{\alpha_L (V_0 + V_{DS})} \right)^2} \left[\left(1 - \frac{2}{\alpha_L (V_0 + V_{DS}) \left(\frac{g_m}{I_d} + \frac{2}{L \cdot E_{sat}} \right)} \right) \right. \\ & \left. \left(\frac{g_S}{I_d} S_{g_m}^T + \frac{2}{L \cdot E_{sat}} \frac{I_S}{I_d} S_{I_d}^T \right) - \left(\frac{g_S}{I_d} S_{g_m}^T - \frac{g_m}{I_d} \frac{I_S}{I_d} S_{I_d}^T \right) \right] + \\ & \sigma_L \cdot \alpha_L (V_0 + V_{DS}) \frac{g_S}{I_d} S_{g_m}^T = S_{g_{ds}}^T \end{aligned} \quad (3.2.9)$$

where $g_{DS} = \frac{I_d}{\alpha_L (V_0 + V_{DS})}$, I_S , $S_{g_m}^T$ and $S_{I_d}^T$ are given in (3.2.1(b)), (3.2.6) and (3.2.7) respec-

tively. At $V_{DS} = V_{DD}/2$, the sensitivity $S_{g_{ds}}^T$ is evaluated against $g_m/I_d|_{T_0}$, considering a short channel length ($L = 0.18\mu m$), and a long channel length ($L = 3\mu m$) PMOS device with $W = 10\mu m$. The corresponding σ_L parameter is $\approx 3 \cdot 10^{-3}$ and $\approx 0.1 \cdot 10^{-3}$ respectively [21], and α_L can be determined from 3.2.5. The $S_{g_{ds}}^T$ is plotted in Fig. 3.2.6(a), and compared with the simulated relative induced g_{ds} variation $(g_{ds}^{T=125} - g_{ds}^{T=-40})/g_{ds}^{T=-40}$ given in Fig. 3.2.6(b), the curves are plotted in \log_{10} scale for more visibility. It can be indicated that, the region where g_{ds} possesses a minimum temperature variation for any $0.18 \leq L[\mu m] \leq 3$ is lies between strong and moderate inversion level, typically in the range $3 \leq g_m/I_d \leq 10$. These results are also obtained for different, $V_{DS} = 1.35\text{ V}$ as shown in Fig. 3.2.6(c) and $V_{DS} = 0.2\text{ V}$ as shown Fig. 3.2.6(d). For NMOS device the minimum g_{ds} sensitivity is observed at slightly lower g_m/I_d conditions. It is important to note that the short channel low temperature sensitivity point comes in contrast with usual analog design practices that tends to maximize L to reduce second-order effects.

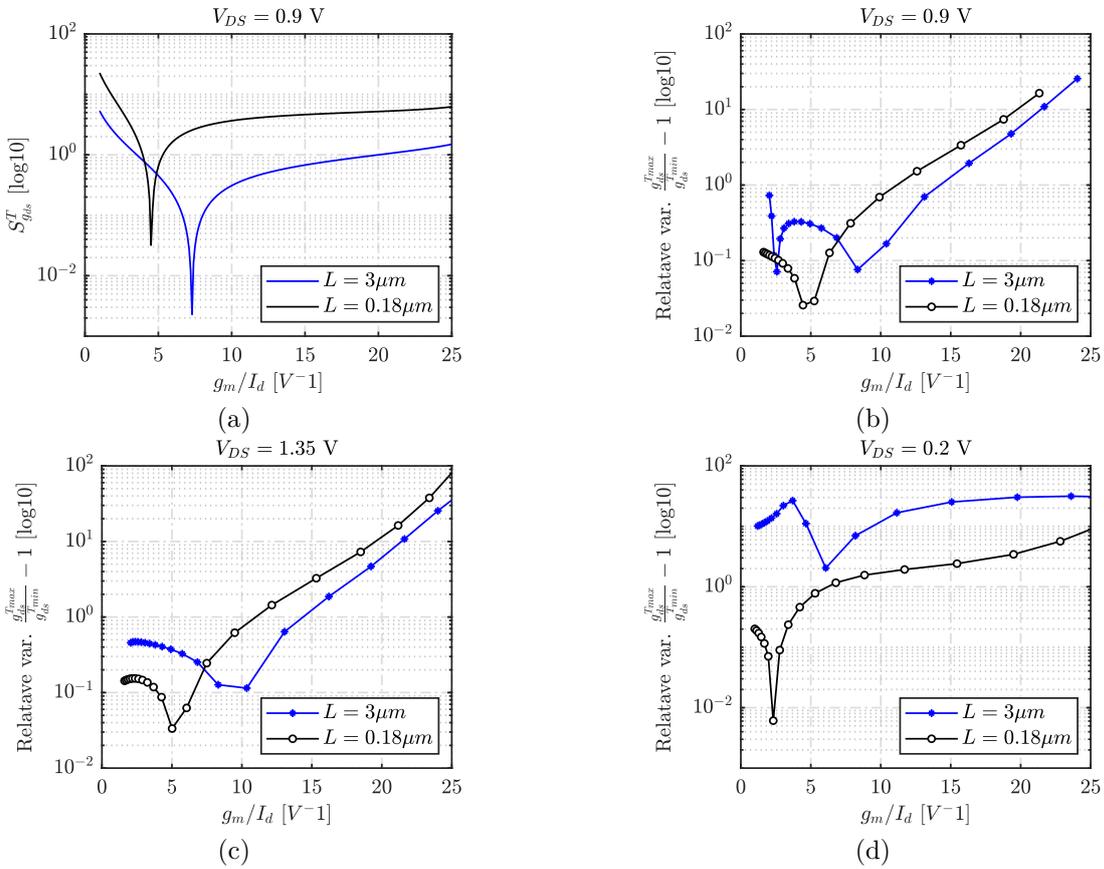


Figure 3.2.6 : (a) curves of $S_{g_{ds}}^T$ given by (3.2.9) as a function of $g_m/I_d|_{T_0}$ for $V_{DS} = 0.9\text{ V}$, and the simulated relative induced g_{ds} variation $(g_{ds}^{T=125} - g_{ds}^{T=-40})/g_{ds}^{T=-40}$ against $g_m/I_d|_{T_0}$ for, (b) $V_{DS} = 0.9\text{ V}$, (c) $V_{DS} = 1.35\text{ V}$, and (d) $V_{DS} = 0.2\text{ V}$. The curves are plotted in \log_{10} scale for more visibility, considering a PMOS device with short channel length ($L = 0.18\mu m$ black line), and long channel length ($L = 3\mu m$ blue line) while $W = 10\mu m$. The corresponding σ_L parameter (for $L = 0.18\mu m$ and $L = 3\mu m$) is $\approx 3 \cdot 10^{-3}$ and $\approx 0.1 \cdot 10^{-3}$ respectively

$(g_m/I_d)_{5(6)} \approx 5$. A relatively long channel length ($L \approx 3\mu m$) is used for M_0 , $M_{5(6)}$, $M_{7(8)}$ and $M_{9(10)}$ to minimize flicker noise and to achieve a DC-gain of 60 dB. Under this channel length value, the amplifier gain also has a higher thermal stability since the V_{DS} across these transistors is in the range of $0.2 \leq V_{DS}[V] \leq 0.9$ (see Fig. 3.2.6(b)(d)).

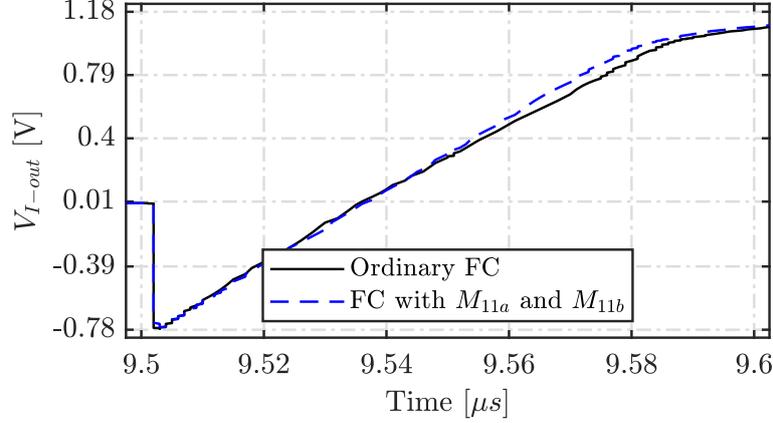


Figure 3.2.8 : Integrator output using FC structure for, without M_{11a} and M_{11b} (black full line), with M_{11a} and M_{11b} (blue dashed line)

Once g_m/I_d for each transistor is selected, one may use (3.2.3) to estimate the aspect ratio of the device. Note that the inclusion of two extra transistors M_{11a} and M_{11b} as shown in Fig. 3.2.7 minimizes the transient voltage changes during slew-rate limiting [47]. In fact, during the times of slew-rate limiting, these transistors prevent the drain voltages of M_3 and M_4 from having large transients where they change from their small-signal voltages to voltages very close to V_{I-os} . The added transistors allow the OTA to recover more quickly following a slew-rate condition. This is illustrated in Fig. 3.2.8. The second OTA is only a scaled version of the first OTA, the biasing current is roughly half of the first OTA ($I_{da2} \approx 30\mu A$ and $I_{db2} \approx 27\mu A$), and so for the aspect ratio of the devices. Table lists the transistor dimensions of the first (a) and the second (b) OTA, it includes the multiplier (M) and the finger number (ng). PVT post-layout simulation results that validate the transistor-sizing- g_m/I_d -based-approach will be detailed in the next chapter.

Table 3.2 : Transistor dimensions, of (a) OTA1, and (b) OTA2

Device	$W [\mu m]$	$L [\mu m]$	M	ng	Device	$W [\mu m]$	$L [\mu m]$	M	ng
M_0	4	2	2	36	M_0	4	2	2	18
$M_{1(2)}$	6	3	2	24	$M_{1(2)}$	6	3	2	12
$M_{3(4)}$	4	2	2	9	$M_{3(4)}$	4	2	2	5
$M_{5(6)}$	6	3	2	5	$M_{5(6)}$	6	3	2	3
$M_{7(8)}$	6	3	2	24	$M_{7(8)}$	6	3	2	12
$M_{9(10)}$	6	3	2	24	$M_{9(10)}$	6	3	2	12
$M_{11(a,b)}$	2	1	2	48	$M_{11(a,b)}$	2	1	2	24

(a) OTA1

(b) OTA2

3.4 Common mode feedback control circuit

The common mode feedback circuit CMFB is depicted in Fig. 3.4.1.

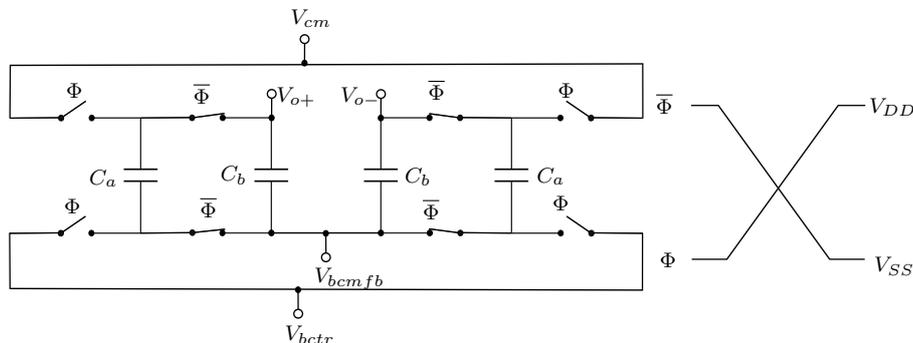


Figure 3.4.1 : Switched capacitor common mod feedback control CMFB

This circuitry is added to determine the output common-mode voltage (V_{oc}) of the amplifier and to control it to be equal to $V_{cm} = 0.9$ V. In fact, during the phase $\bar{\Phi}$, the capacitor denoted C_b generate the average of the output voltages V_{oc} with respect to the control voltage V_{bctr} , and the capacitor labeled C_a is charged to $V_{cm} - V_{bcm,fb}$. In phase Φ the capacitors C_a and C_b are connected in parallel, causing the control voltage V_{bctr} to be shifted by a fraction of $\delta V = V_{oc} - V_{cm}$. V_{bctr} then adjust the transistors $M_{3(4)}$ accordingly to maintain $V_{oc} = V_{cm}$.

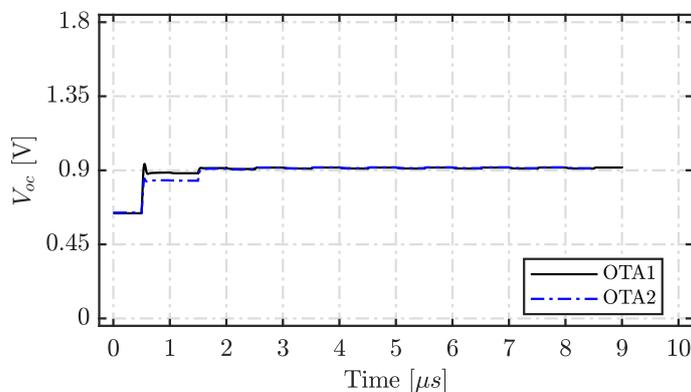


Figure 3.4.2 : Output common mode voltage V_{oc} of the first (black full line) and the second (blue dashed line) OTA respectively using the CMFB shown in Fig. 3.4.1, with the capacitance values listed in Table 3.4

The slew rate and unity-gain frequency of the CMFB control loop should be comparable to that of the differential loop to avoid output signal distortion. Using larger capacitance values (compared to C_i) may overload the amplifier during the integrating phase. Reducing the capacitors too much causes an offset error due to the residual charge injection of the switches. The values of $C_{a(b)}$ are determined by simulation and listed in table 3.4. The

dimensions of the unit capacitor (C_u) are $10 \times 10 \mu\text{m}^2$, and its capacitance is $C_u = 106.8$ fF.

Table 3.4 : CMFB capacitance values

C_a	$8C_u$	854.4 fF
C_b	C_u	106.8 fF

3.5 Integrator

3.5.1 Parasitic insensitive integrator

The single version implementation of the integrator used in this work including the parasitic capacitances is depicted in Fig. 3.5.1.

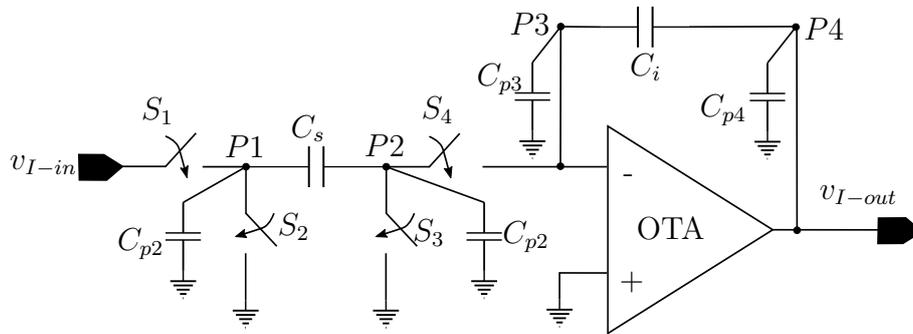


Figure 3.5.1 : Parasitic-Insensitive integrator

In this topology, the parasitic capacitances shown at the nodes P_1 and P_2 represents the top and the bottom plate capacitances of C_s , C_i , as well as the capacitances associated with the switches. The effect of the parasitic capacitances C_{p2} and C_{p3} on the transfer function is small, since C_{p3} is always connected to the virtual ground of the OTA, and C_{p2} is either connected to ground through the switch S_1 or to the OTA virtual ground through the switch S_2 . Thus both C_{p2} and C_{p3} are always remains discharged. In addition, the capacitance C_{p4} is connected to the amplifier output; it may affect the speed of the OTA but not the final settling voltage. Hence, it also does not affect the operation of the circuit. Finally, the parasitic capacitance at the node P_1 is charged to V_{I-in} during the sampling phase, and then discharged to ground during the integrating phase. This means that, C_{p1} does not affect the charge stored and delivered by C_s .

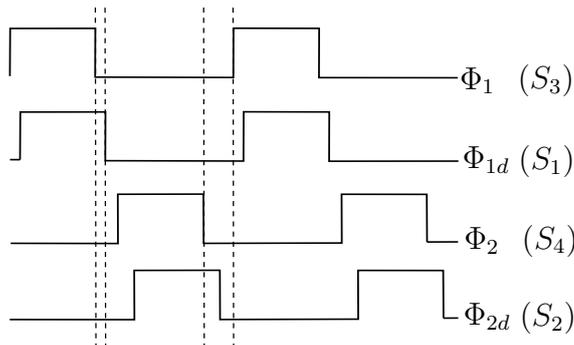


Figure 3.5.2 : Clocking diagram

The above analysis assumes that the switch clocking signals are completely overlapped as in the clocking diagram illustrated in Fig. 3.5.2. Also, the clock signals of the switches S_1 and S_2 can be made delayed with respect to S_3 and S_4 , respectively. This technique is called bottom-plate sampling; it is introduced to make the charge injection caused by S_1 and S_2 independent of the input signal [77]. The fully differential implementation also helps to reduce both charge injection and clock feed-through errors. The sampling and integrating capacitance values are specified in Chap. 2, and are given in Table 3.5 for the first and the second integrator respectively.

Table 3.5 : Integrating and sampling capacitance values

Integrator 1				Integrator 2			
C_s	$38C_u$	4.06 pF	$a_1 = 0.809$	C_s	$10C_u$	1.06 pF	$a_2 = 0.5$
C_i	$47C_u$	5.02 pF		C_i	$20C_u$	2.14 pF	

3.5.2 1-bit DAC input integrator

The fully differential structure of the input integrator, including the 1-bit DAC is depicted in Fig. 3.5.3(a). When the modulator output is digital 1, e.g $D = V_{DD}$, the negative input signal is selected $V_{in} = -2V_y$ (a negative V_{ref} is applied) ensuring a negative feed-back system. In the case when the sensor has a single ended output for each MEMS resonator, the integrator shown in Fig. 3.5.3(b) can instead be used.

This architecture is obtained by adding two switches to the integrator illustrated in Fig. 3.5.3(a). In fact, during clock phase Φ_1 , the switches S_{11} , S_1 , and S_3 are closed to sample the positive input voltage denoted v_{I-in+} across C_s^+ . Switches S_7 , S_6 , and S_{14} are also closed to discharge the second sampling capacitance C_s^- , and to short the negative input terminal v_{I-in-} to analog ground. During the clock Φ_2 , the switches S_{12} , S_5 , and S_6 are closed to apply a sample voltage to input positive terminal of the amplifier through v_{I-in-} and C_s^- . At this phase v_{I-in+} is grounded, and the positive input terminal of the amplifier is connected to C_s^+ . Thus, v_{I-in+} and v_{I-in-} are available at the inputs of the amplifier, and integrated across C_i^+ and C_i^- simultaneously. This operation assumes that

the sampling frequency is much higher than the input signal frequency, i.e., v_{I-in} does not change during both phases.

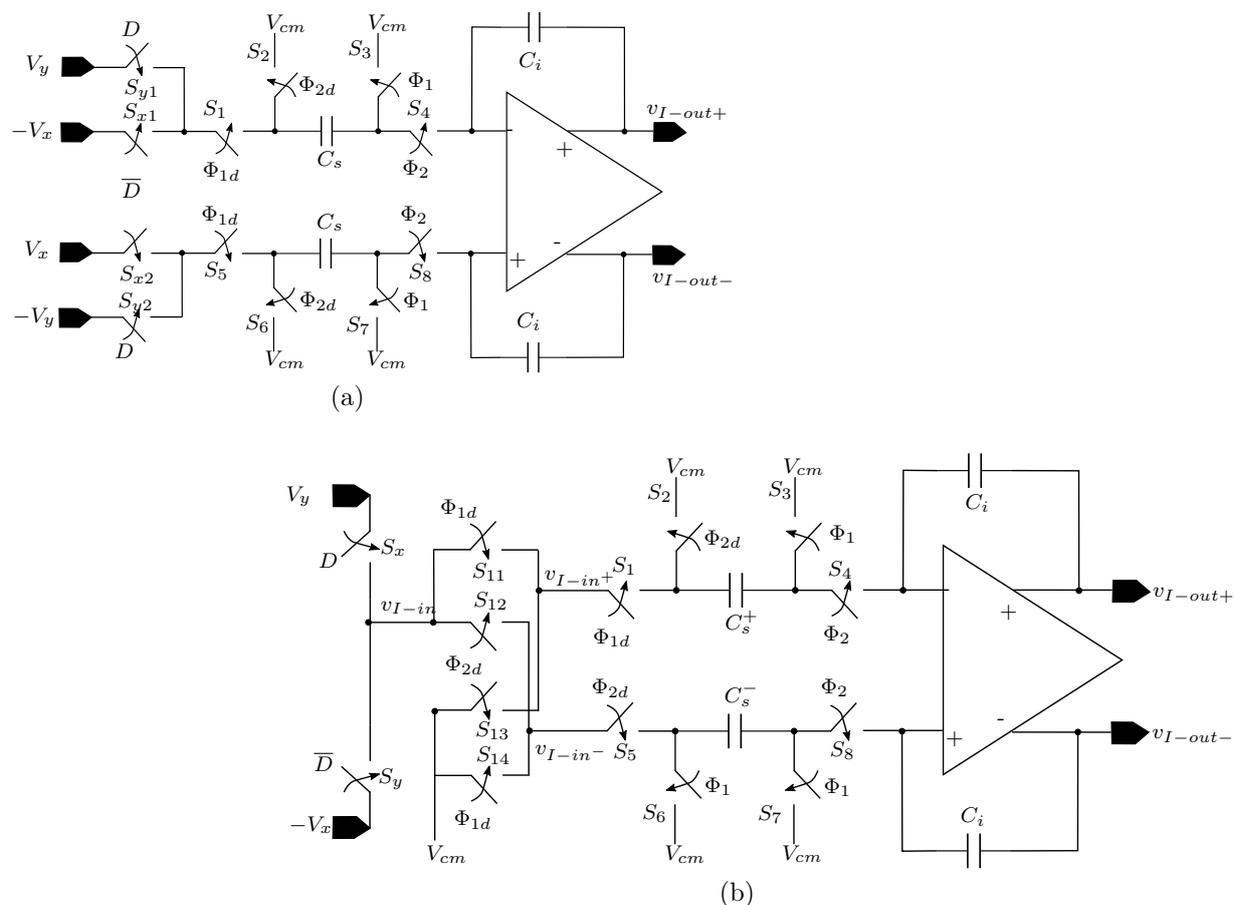


Figure 3.5.3 : 1-bit DAC integrator, (a) fully differential, and (b) single to differential

Figure 3.5.4 compares the output response of the fully differential with the single to differential integrator, considering a differential input signal, i.e. $2 \cdot V_x^{max} = 1.44$ V, and integrating coefficient $a = 0.8$. It can be indicated that both responses are exactly fitted except for the presence of a slightly lower V_{drop} in the case of the single to differential structure. This difference can be explained by the fact of extra switches in the design.

It worth mentioning that the bottom half circuit of the single to differential integrator is also parasitic insensitive and has the same properties of the circuit shown in Fig. 3.5.1. It is also important to note that both architectures have the same input referred noise voltage since the noise in SC network is independent of the on-resistance, and hence the number of the switches in the circuit. As a conclusion of RM- $\Sigma\Delta$ being DT designed, it's easier to implement the input integrator either, with a single input, or a differential input, while preserving the fully differential functionality of the RM- $\Sigma\Delta$. This also a major benefit of using a DT design. In this work, the modulator was designed with the differential input 1-bit DAC integrator.

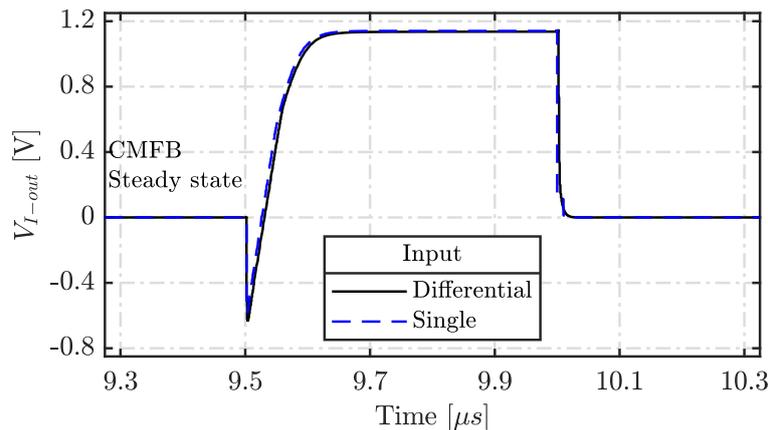


Figure 3.5.4 : Integrator output for a differential input voltage of $2 \cdot V_x^{max} = 1.44$ V and $a = 0.8$, fully differential structure (black full line), and single to differential structure (blue dashed line)

3.6 Comparator

The comparator topology implemented in this work is the double-tail comparator that was first proposed by Schinkel and al. in [78]. The working principle of this comparator is divided into three phases: precharge, decision, and regeneration. A schematic illustration of this comparator is presented in Fig. 3.6.1.

In the precharge phase, when $CLK = 0$, the transistors M_3 and M_4 charge the nodes v_p and v_m to V_{DD} respectively. These nodes force the transistors M_5 and M_6 to turn on. As soon as M_{01} begins to conduct, M_1 and M_2 start to discharge v_p and v_m respectively. Considering $V_{i+} - V_{i-} > 0$, the node v_p discharge faster than v_m , turning the transistor M_5 off, and the inverter composed by M_8 and M_{10} turns on; and the comparator latches in its regenerative phase.

This architecture was introduced because of their improved performance, especially in kick-back noise [78]. In addition, the circuit is purely dynamic and consumes power only at the rising edge of the clock. It worth mentioning that the delay time of this comparator is in order of magnitude of nanosecond [79], which is very small compared to the minimum clock period T_s . Hence, its effect can be ignored. Also, the offset error can be neglected since the $\Sigma\Delta$ modulator suppresses the non-idealities of the comparator, as discussed in Chap. 2. For further detailed information and PVT simulation results on the double-tail comparator non-idealities, the interested reader can refer to [79], provided by our research team.

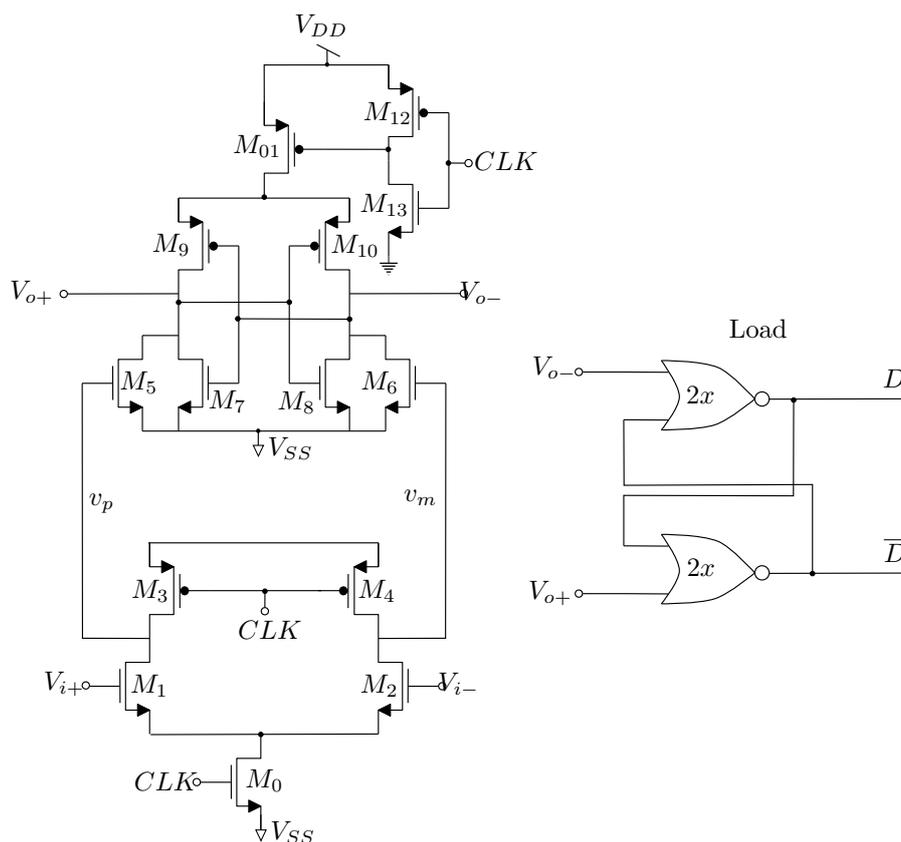


Figure 3.6.1 : Double-tail comparator

Note that the circuit has a purely digital behavior with the exception of transistors M_1 and M_2 that amplify the input signal. Hence, the devices that operate as a switch have minimum dimensions. The preamplifier usually does not have a gain much greater than 10; otherwise its time constant is too large, and its speed is limited. Thus, a minimum length and a low aspect ratio can be set for the active load $M_{3(4)}$ and the input differential pair $M_{1(2)}$ respectively. $M_{1(2)}$ must, however, have a larger length ($L = 1.44 \mu m$) to avoid mismatch effects in the decision operation. The complete transistor dimensions are listed in Table 3.6.

Table 3.6 : Transistor dimensions of the double-tail comparator

Device	$W [\mu m]$	$L [\mu m]$	M	ng
M_0	1.1	0.18	1	1
M_{01}	1.14	0.18	1	1
$M_{1(2)}$	1.8	1.44	2	4
$M_{3(4)}$	1.1	0.18	1	1
$M_{5(6)}$	0.72	0.18	1	1
$M_{7(8)}$	0.36	0.18	2	4
$M_{9(10)}$	0.36	0.18	2	4
$M_{11(12)}$	0.72	0.18	1	1

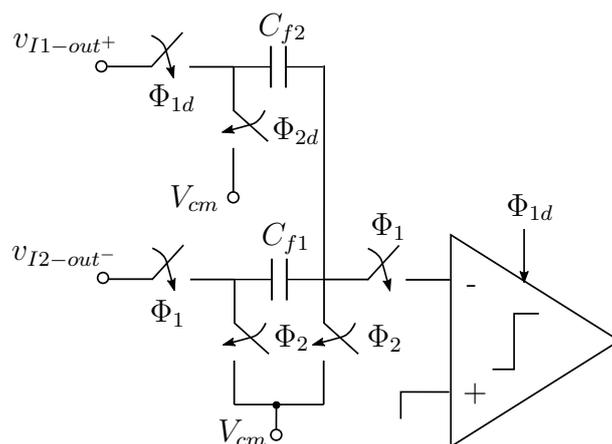


Figure 3.6.2 : Feedforward circuit

3.7 Feed forward coefficients

The adder and the feedforward coefficients are implemented as shown in Fig. 3.6.2. The resulting voltage that is applied to the comparator can be expressed as,

$$v_{comp-in-} = \frac{v_{I1-out+}C_{f1} + v_{I2-out+}C_{f2}}{C_{f1} + C_{f2}}. \quad (3.7.1)$$

Therefore, the output voltage is the sum of the inputs weighted by the feed-forward coefficients but attenuated by a constant value that is the sum of all the coefficients. Since the modulator is a single bit architecture, the only relevant information is in the sign and hence the attenuation does not affect the modulator operation. Considering $C_{f1} = C_{f2}$, yielding to $v_{comp-in-} = \frac{v_{I1-out+} + v_{I2-out+}}{2}$. The capacitances C_{f1} and C_{f2} are chosen to meet the requirement of ν that specified around 2 (Chap. 2, eq. 2). Considering the capacitor value of C_{i1} and C_{s2} given in table 3.5, for $C_{f1} = 12C_u \approx 1.28$ pF one may have $\nu \approx 2.13$.

3.8 Non overlapping clock

The non-overlapping clock signals can be generated using a simple circuit of logic gates, as shown in Fig. 3.8.1. As the switches are transmission gates, each phase needs a complementary signal ($\overline{\Phi_1}$, $\overline{\Phi_2}$, $\overline{\Phi_{1d}}$ and $\overline{\Phi_{2d}}$) for proper operation. The delay cell composed by NMOS and PMOS has the same dimensions as the transistors of the inverter to emulate the same delay. A $20\times$ buffer cell is used for Φ_1 and Φ_2 to drive 8 switches in the

integrators, 4 switches in the feedforward circuit, 8 switches in the CMFBs (OTA1 and OTA2), 4 switches in the CMFB of a stand alone for test amplifier (as will be shown in the global conclusion), and the pin of the I/O ring. A $4\times$ buffer cell is used for Φ_{1d} to drive 4 switches and the comparator, while $2\times$ buffer is selected for Φ_{2d} since it only drives 4 switches.

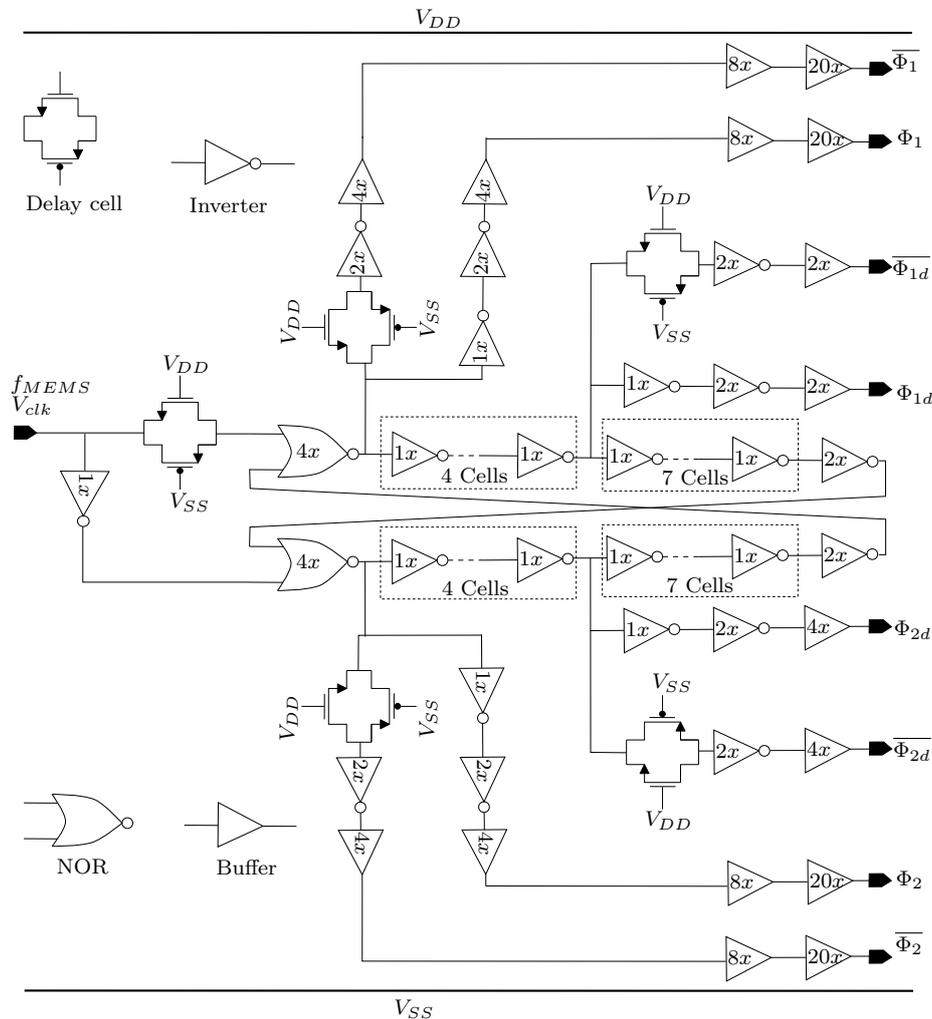


Figure 3.8.1 : Non-overlapping clock tree

3.9 Conclusion

The transistor-level design of the analog circuits used in the RM- $\Sigma\Delta$ M are discussed. The design was done using the SOI module of XH018 process technology, and prioritizing the circuit reliability against PVT variation over the area and power consumption. First, the

design of the switch is presented, and the limitations of the ordinary switch design based on a single transistor are discussed. The switch is based on the well known transmission gate structure providing a relatively stable and low on-resistance of $< 150\Omega$ considering wide input voltage range from 0.2 to 1.6 V. This value of the on-resistance is sufficiently low ensuring a negligible SNR degradation due to the incomplete charge transfer in the largest sampling capacitance C_{s1} .

Second, an overview of the OTA architectures is investigated. Considering the required specifications, the folded-cascode OTA structure is proffered. For effectively implementing the OTA with high thermal stability considering the automotive application, a new g_m/I_d methodology analysis is established. The proposed approach is based on the UICM model which encompass weak to strong inversion, with relatively simple and accurate equations. Primary, the temperature variation of the quiescent current I_d and the transconductance g_m were analyzed. The impact of second-order effects, such as gate length, and drain-source voltage, are then included to study the thermal stability of the drain-source transconductance g_{ds} that define the amplifier DC-gain. The proposed g_m/I_d based temperature sensitivity model of I_d , g_m and g_{ds} is compared and validated with simulation results using Cadence Spectre simulator. Afterword, the optimal operating point (g_m/I_d) of each transistor is selected, and the overall performance of OTA1 and OTA2 including CMFB and biasing circuit is optimized by simulation to mach the requirements settled in Chap. 2. The biasing circuit is implemented using a wide-swing-cascode-current-mirror structure that enhances the output swing of the amplifier.

Third, the single to differential and the fully differential implementation of the input 1-bit-DAC integrator are discussed, both implementations are parasitic insensitive and have the same noise performance. Thus, for a sensor having only one output, the single to differential 1-bit-DAC integrator could be used to perform a differential modulator, while preserving the same performance of the fully differential integrator. In this project, the sensor is considered with differential output; hence the fully differential of the input 1-bit-DAC integrator is used in the final modulator implementation.

Fourth, the double tail latched comparator used in the modulator is presented, and its working principle is discussed. This dynamic comparator is ideal for DT applications since it has a purely digital behavior, and consumes power only at the rising edge of the clock. Next, the feedforward circuit is presented, and the choice of the capacitance value of $C_{f1} = C_{f2}$ is discussed. Finally, the non-overlapping clock tree as well as the buffer choice for each signals ($\overline{\Phi_1}$, $\overline{\Phi_2}$, $\overline{\Phi_{1d}}$ and $\overline{\Phi_{2d}}$) are demonstrated.

In Chap. 4 the final layout of each block designed in this chapter will be presented, and the drawing technique used to minimize process and temperature variation effect will be highlighted. The final layout assembly of the modulator and the final tape-out will also be presented and discussed. The next chapter will also depict the relevant simulations and results that validate the functionality of each block designed in this chapter using four types of simulations: Nominal, PVT, Corner, or Monte-Carlo.

Chapter 4

Post layout simulation results

4.1 Introduction

This chapter presents the post-layout simulation results of each building block developed in Chap. 3. The functionality of these blocks as well as the ratiometric operation of the modulator are analyzed considering nominal, PVT Monte Carlo, or Corner simulations, using Cadence Spectre® simulator. PVT analysis is carried out for process mismatch of 3σ Gaussian distribution provided by XH018 design kit, standard supply variation $V_{DD} \pm 10\%$, and under the temperature range of the industrial automotive application $-40 \leq T \leq 125$ °C.

The switch, the OTA and its biasing circuit, the modulator coefficients, the comparator, the non-overlapping clock, and the entire modulator are presented and analyzed. The functionality of the switch, the OTA and its biasing circuit are analyzed and validated considering nominal, and PVT Monte Carlo simulations. Worst, nominal, and best case characteristics of these circuits are summarized and compared with the required specifications settled in Chap. 2. As will be shown throughout this chapter, the amplifiers possess a high reliability against temperature variation, in agreement with the g_m/I_d -based transistor sizing analyses proposed in Chap. 3. Next, the modulators coefficients implemented using capacitors are only evaluated against process and mismatch effects since the capacitors have a very low temperature, and supply dependency. As will be seen from the statistical results, the coefficients have a relative error of lower than 0.05%, confirming the DT implementation feature discussed in Chap. 2. As highlighted in Chap. 3, and according to [79], the comparator used in this work has a negligible impact on the modulator performance even when PVT variations are considered. Thus, this circuit is not analyzed in the following discussions. Also, the non-overlapping clock signals are only evaluated in the nominal case. The reason is that the inherent behavior of this circuit ensures that the delays are always present even when experiencing PVT variations. Finally, and after validating the performance of each building block, the ratiometric operation of the RM- $\Sigma\Delta$ M is analyzed with PVT Corner simulations comprising typical, worst speed,

and worst power. Since transient noise simulation of the entire RM- $\Sigma\Delta$ M circuit takes to much time, the PSD is only carried out in the worst case conditions, by considering maximum temperature value of the industrial automotive application $T = 125\text{ }^\circ\text{C}$, and minimum OSR (maximum signal bandwidth, and sampling frequency).

4.2 Switch

Figure 4.2.1 illustrates the layout of the switch having an area $18\times 20\ \mu\text{m}^2$. Process-Voltage-Temperature PVT analysis is carried out using transient simulation to extract the on-resistance mean value R_{men}^{TG} . Process variation is analyzed using 51-points Monte Carlo simulation for process mismatch 3σ Gaussian distribution with mean value denoted ($\bar{\mu}$). Temperature variation is analyzed for 6-points from -40 to $125\text{ }^\circ\text{C}$. Voltage variation is analyzed at $V_{DD} = 1.8 \pm 10\%$ (i.e. 3-points). The results are depicted in Fig. 4.2.2 for typical performance at $\bar{\mu}$ and $V_{DD} = 1.8\text{ V}$ (black full line), best-case conditions at $\bar{\mu} + 3\sigma$ and $V_{DD} = 1.62\text{V}$ (blue dashed line), and worst-case conditions at $\bar{\mu} - 3\sigma$ and $V_{DD} = 1.98\text{ V}$ (red dotted line). As can be observed, considering PVT variation the switch on-resistance is changing from $110\ \Omega$ to $150\ \Omega$, corresponding to a variation of more than 36%. This increase may not be tolerable using a simple one-transistor switch, especially when working with high voltage swing, as discussed in the previous chapter. However, using TG switch, a 36% variation or even more (after fabrication) remains negligible, since the time constant to charge the largest capacitance in the circuit still very low with respect to $T_s/2$. TG architecture is used to implement all switches in the modulator.

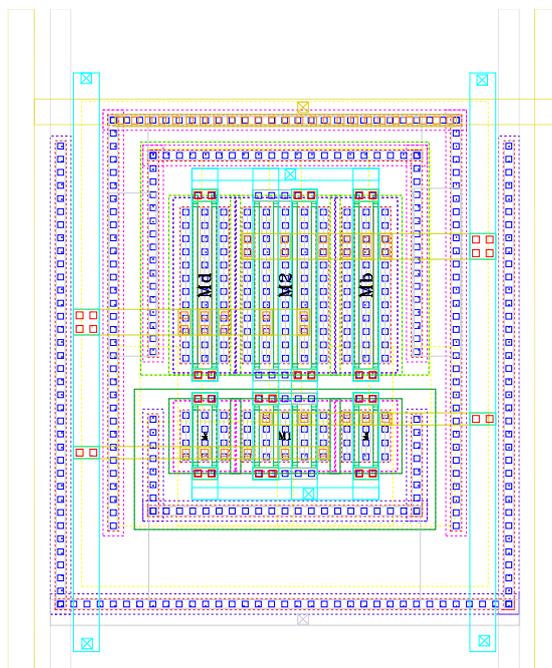


Figure 4.2.1 : Layout of the TG switch including dummy transistors having an area of $18\times 20\ \mu\text{m}^2$

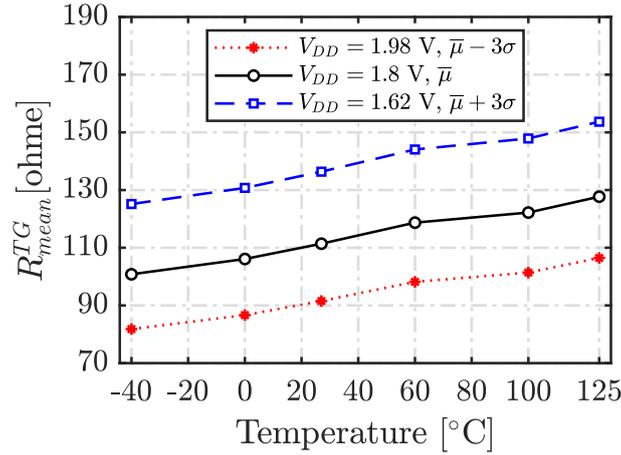
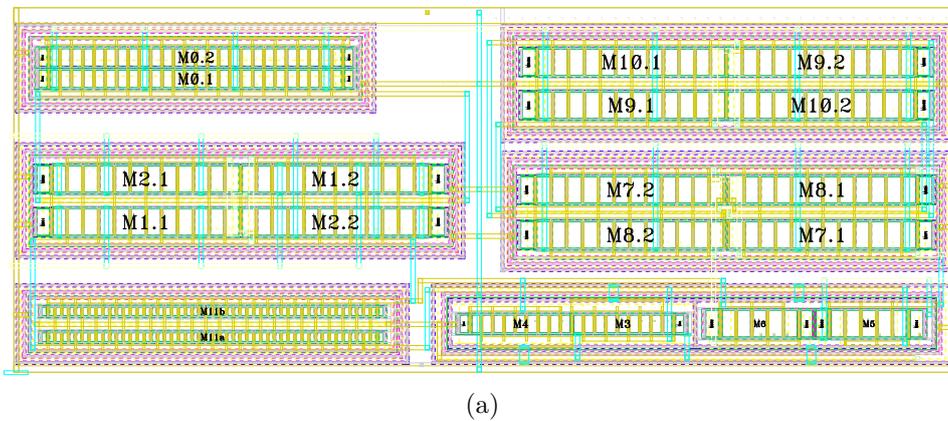


Figure 4.2.2 : PVT analysis for 6-points temperature from -40 to 125 °C, 51-points Monte Carlo simulation for $\pm 3\sigma$ process mismatch variation at $V_{DD} = 1.8 \pm 10\%$: Typical performance is illustrated in black full line for the mean value ($\bar{\mu}$) and $V_{DD} = 1.8$ V, extreme-case conditions are in blue dashed line ($\bar{\mu} + 3\sigma, V_{DD} = 1.62$ V), and in red dotted line ($\bar{\mu} - 3\sigma, V_{DD} = 1.98$ V)

4.3 Operational transconductance amplifier 'OTA'

The layout of the OTA1 and its biasing circuit are given in Fig. 4.3.1, they occupy an area of $220 \times 80 \mu m^2$ and of $35 \times 20 \mu m^2$ respectively. In these layouts, all transistors labeled M_D stand for dummy devices. These dummy transistors ensure that the etching and diffusion processes occur equally over all segments of the transistor, minimizing length roughness surface variability. Common-centroid technique is used to draw the input differential pair $M_{1(2)}$ and the active load transistors of the output branch $M_{7(8)}$ and $M_{9(10)}$ (Fig. 4.3.1(a)). This technique helps improve the matching between two transistors, and makes them immune from the effect of first-order cross-chip gradients, e.g., temperature. The multi-fingered gates also helps reduce series resistance in gate and save space. The same techniques are used for the OTA2, its layout (not presented here) is only a scaled version of OTA1 and has an area of $135 \times 80 \mu m^2$.



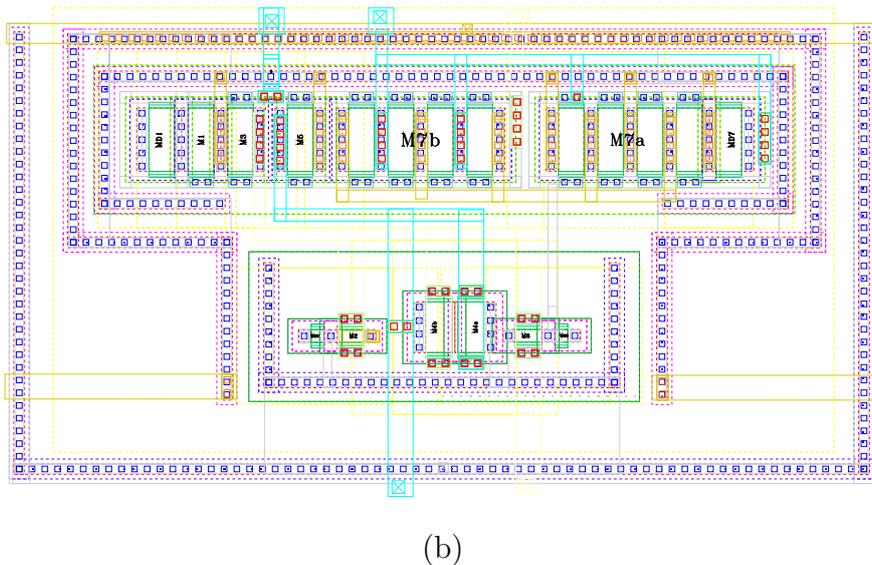


Figure 4.3.1 : (a) layout of the OTA1 having an area of $220 \times 80 \mu\text{m}^2$, and (b) layout of the biasing circuit, it has an area of $35 \times 20 \mu\text{m}^2$. Transistors labeled M_D in the layouts are dummy devices. The layout of the OTA2 is not shown, it is only a scaled version of OTA2 and has an area of $135 \times 80 \mu\text{m}^2$

4.3.1 Nominal simulation

Figure 4.3.2 shows the bode diagrams of the first OTA (full black line) and the second OTA (dashed blue line). The frequency responses are carried out in the nominal circuit conditions, i.e., $V_{DD} = 1.8 \text{ V}$ and $T = 27^\circ\text{C}$, using "stb-analysis" from Spectre simulator. It can be observed from Fig. 4.3.2 that both OTAs meet the requirement of greater than 58 dB. The gains $A_{1(2)}$ are roughly 59.5 dB and 62.6 dB respectively. It is important to note that the OTAs can be assumed of 1 pole structure, in which the unity gain frequency f_T can be approximated to GBW ,

$$GBW_{1(2)} = \frac{g_{m1(2)}}{C_{Load1(2)}} = \frac{g_m / I_d \cdot I_{da1(2)}}{C_{i1(2)} + C_a + C_b + C_{p1(2)}}. \quad (4.3.1)$$

In (4.3.1) $C_{a(b)}$ are the capacitors of the CMFB circuit, $C_{p1} \approx 0.2 \text{ pF}$ and $C_{p2} \approx 0.1 \text{ pF}$ are the parasitic capacitances at the output of the OTA1(2). Accordingly, $GBW_1 \approx 14.6 \text{ MHz}$ and $GBW_2 \approx 13.4 \text{ MHz}$; these values are a little larger than the unity gain frequencies obtained from the simulated bode responses ($f_{T1} \approx 14.57 \text{ MHz}$ and $f_{T2} \approx 13.2 \text{ MHz}$). Therefore, the circuits can still be assumed as one-pole system. As a result, the GBW requirements settled from the integrator model proposed in Chap.2, can be readily compared with f_T . At these frequencies, the OTAs possess stability phase margin $PM_{1(2)}$ of 82° and 83° respectively (Fig. 4.3.2).

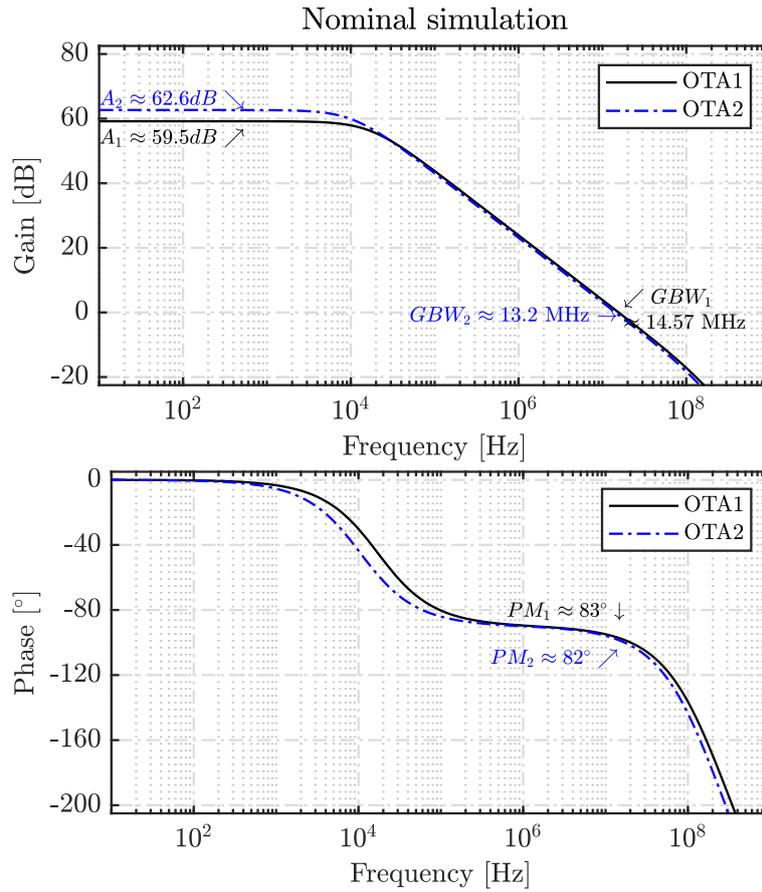


Figure 4.3.2 : Nominal frequency response (Gain and Phase) of the OTA1 black full line, and OTA2 blue dashed line

Circuit stability can also be observed from the OTAs step response illustrated in Fig. 4.3.3, where no oscillations are presented in the output settling (blue dashed line). From these responses, the differential slew rate values are approximately 22 and 25 MV/s for OTA1 and OTA2 respectively.

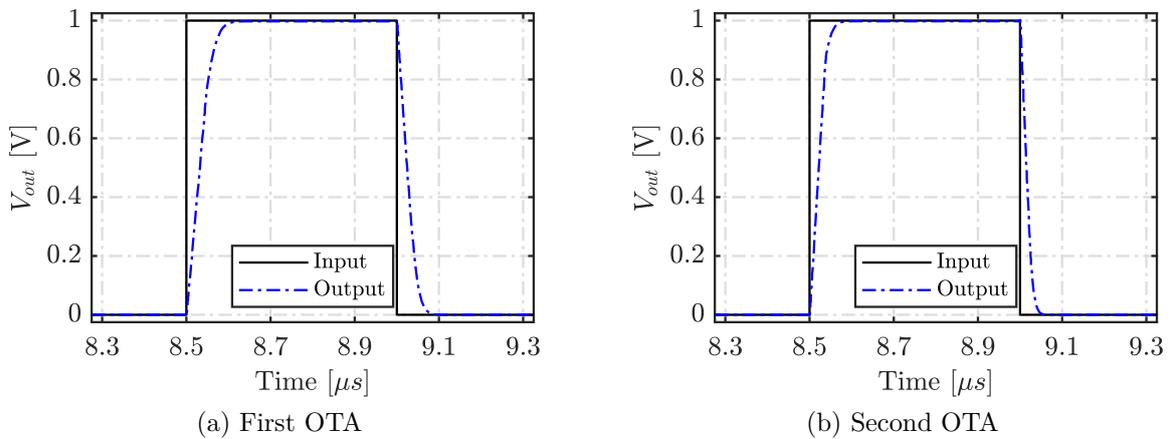


Figure 4.3.3 : Step response of the OTAs using unity feedback configuration

4.3.2 PVT simulation

PVT analysis is performed on OTA1 and OTA2 using 51-points Monte Carlo simulation for 3σ process mismatch, considering 9-temperature-points from -40 to 125 °C, and voltage variation of $V_{DD} = 1.8 \pm 10\%$.

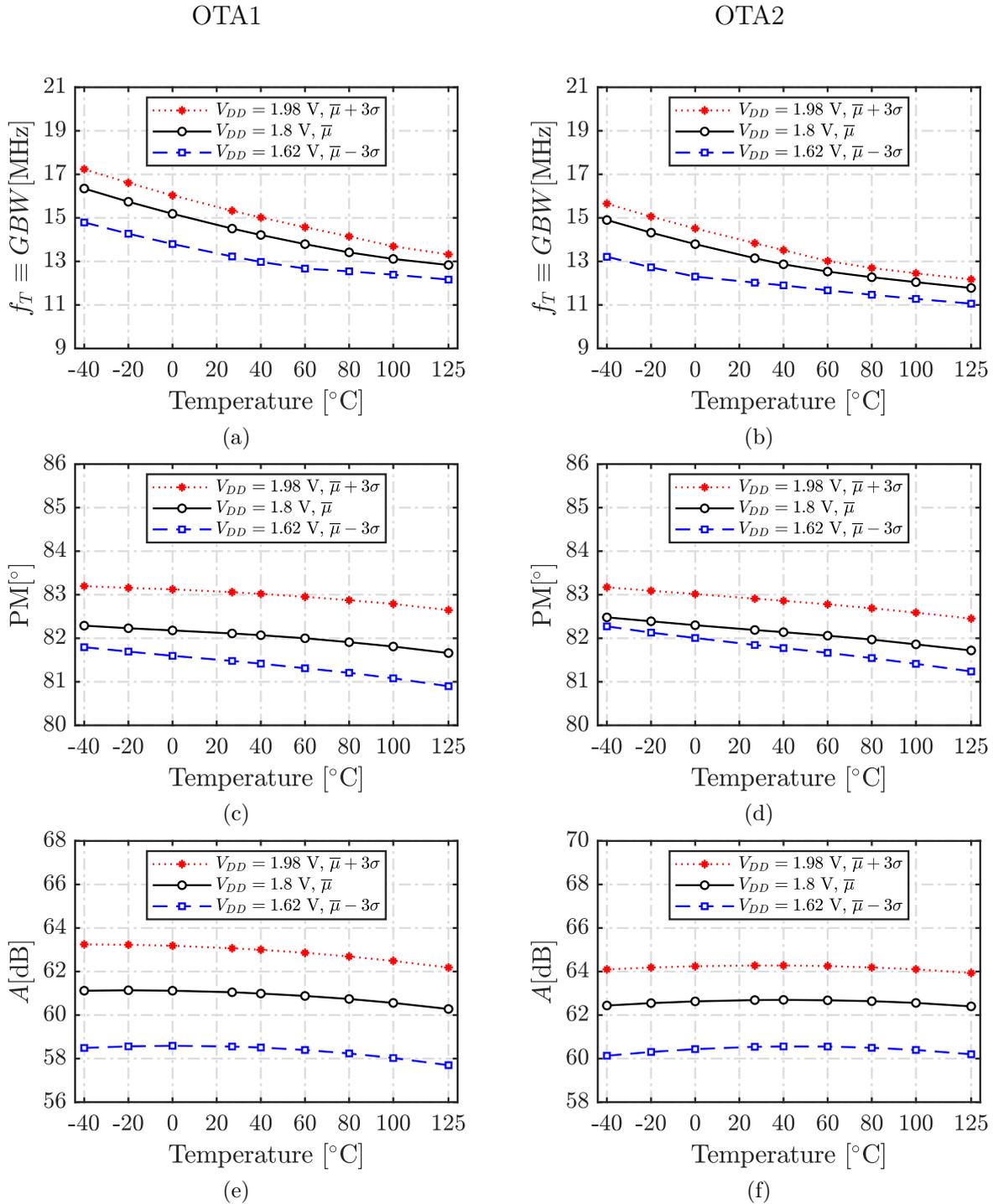


Figure 4.3.4 : PVT frequency analysis of the amplifiers

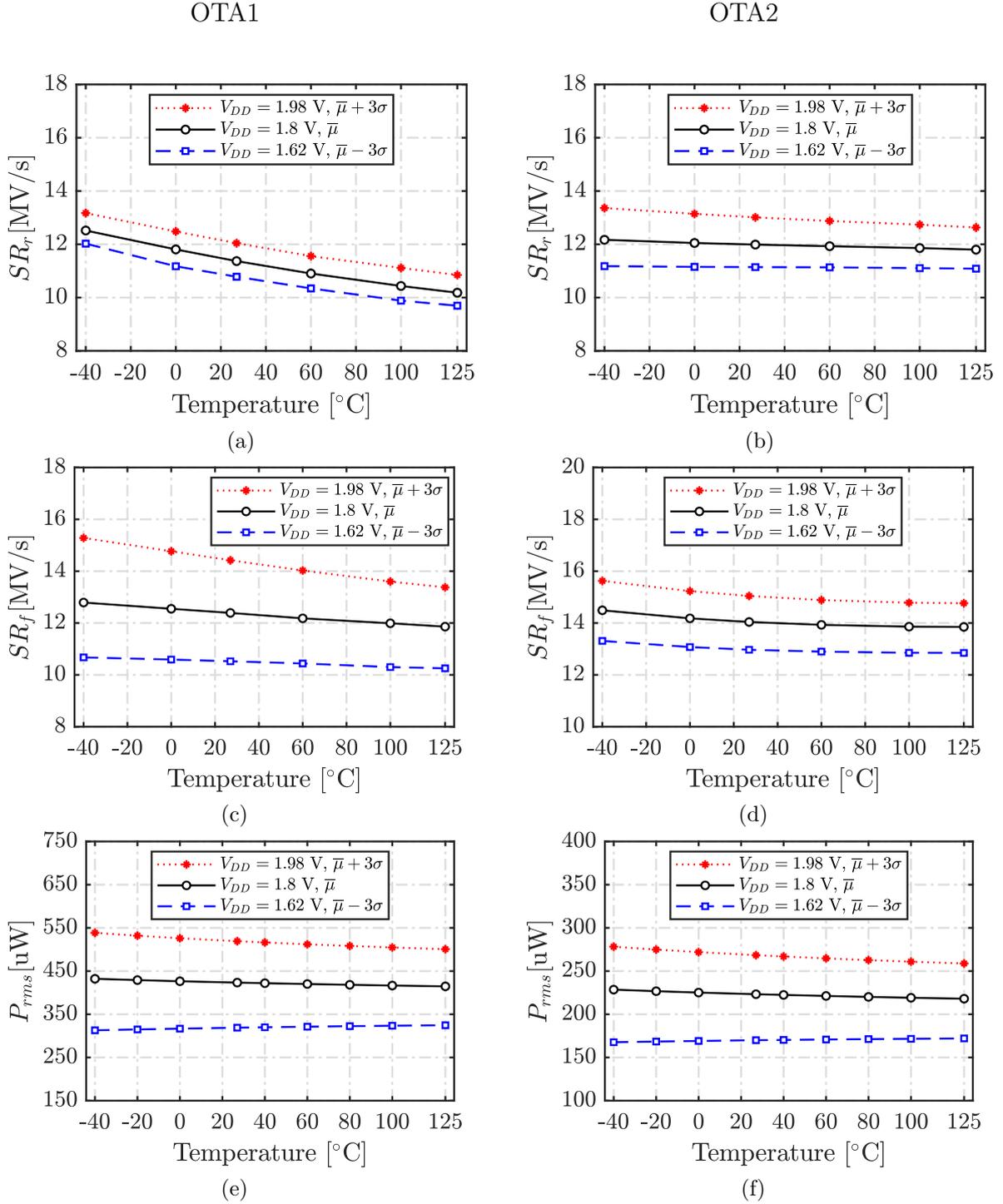


Figure 4.3.5 : PVT transient analysis of the amplifiers

The results of GBW , PM , and A are depicted in Fig. 4.3.4; typical performance is illustrated in black ($\bar{\mu}$, 1.8 V), and extreme-case conditions are in blue ($\bar{\mu} - 3\sigma$, 1.62V), and in red ($\bar{\mu} + 3\sigma$, 1.98 V). It can be indicated that considering typical performance (black curves), the temperature induced GBW variation from 27 to 125 $^{\circ}$ C of OTA1 and

OTA2 are only 1.6 MHz and 1.2 MHz respectively (Fig. 4.3.4(a)(b)). These variations correspond to less than 11.2% and 9.2% drift-induced deviation from the value at room temperature ($GBW_1 \approx 14.4$ MHz and $GBW_2 \approx 13$ MHz). Also, the amplifiers' DC-gain $A_{1(2)}$ exhibit a high thermal stability, where almost no change is noticed for OTA2, and only 1 dB is observed for OTA1 over the temperature range (Fig. 4.3.4(e)(f)).

Thermal stability of the GBW and the gain A are also preserved in the extreme circuit conditions (blue and red lines). The worst case performance of the OTAs is observed at $V_{DD} = 1.62$ V and $T = 125$ °C. In these conditions the amplifiers' characteristics reach their minimum: $GBW_1 \approx 12.2$ MHz and $GBW_2 \approx 11$ MHz, $A_1 \approx 58$ dB and $A_2 \approx 60$ dB. In addition, the amplifiers show a good stability margin with $PM_{1(2)} > 80^\circ$ for all corner's analysis as highlighted in Fig. 4.3.4(c)(d).

PVT analysis of the positive slew rate (SR_{rise}), the negative slew rate (SR_{fall}) and the power consumption (P_{rms}) are given in Fig. 4.3.5. It can be observed that SR_{rise} is slightly lower than SR_{fall} since NMOS devices are usually faster than PMOS devices. Thus, the minimum slew rate is limited by SR_{rise} and they are ≈ 9 MV/s and ≈ 11 MV/s for OTA1 and OTA2 respectively (Fig. 4.3.5(a)(b)). It can be noticed that the SR and the GBW are higher than the minimum required values to ensure a complete charge transfer under 1% LSB settling error.

It must be stressed that considering the typical simulation given in black curves, the simulated SR values are larger than the expected ($SR_1 = I_{d1}/C_{Load1} \approx 9.2$ MV/s, $SR_1 = I_{d2}/C_{Load2} \approx 8.3$ MV/s). This because the simulated values are carried out in the steady state OTA conditions, and only a small charge fraction is absorbed by the capacitors C_a and C_b to maintain $V_{oc} = V_{cm}$. Hence, the CMFB capacitors do not load the amplifier, at least in the steady state operation. However, the V_{oc} may brutally change due for example to supply voltage drop, in this case C_a and C_b sneaking more current, leading to a lower SR . This effect was implicitly considered in the model presented in Chap.2 (sec.2.5.2.2) by including C_a and C_b in the total load capacitance.

Figure 4.3.5(e)(f) show a small decreasing power consumption with temperature for all corners. This is hardly an advantageous behavior. In fact, it means that the global performance of the OTAs is hardly preserved for any circuit operating conditions. Without the biasing circuit, the OTA1 and OTA2 consume $430 \mu W$ and $220 \mu W$ respectively.

Finally, the linearity of the amplifier (or the integrator) is evaluated against temperature and supply variation, and the results (only for OTA1, the same linearity behavior is obtained for OTA2) are presented in Fig. 4.3.6. It can be indicated that for any circuit conditions, when $V_{I-in} < 1$ V, the integrator output is perfectly linear. While for $V_{I-in} > 1$ the amplifier shows a small linearity distortion, especially at lower supply voltages. At the maximum input voltage, i.e. $V_{I-in} = 2 \cdot V_x^{max} = 1.44$ V, the worst case Total-Harmonic-Distortion (THD) is roughly -43.5 dB (Fig. 4.3.6). However, as shown in Fig.4.3.7 at the maximum input voltage $2 \cdot V_x^{max}$, the integrators' maximum output swing occurrences $V_{I1-os} \approx V_{I2-os} \approx 1.15$ V are $< 5/2000$. This means that a small linearity distortion (of $THD \approx -43.5$ dB) occurs at lower voltage headroom conditions, i.e., $V_{DD} = 1.62$ V,

would only affect 0.25% of the total samples, and only when a maximum input amplitude of 1.44 V is applied to the modulator. Hence, it can be ignored. It must be point out that the output voltage of the first integrator is little bit smaller than the second integrator. In fact, according to (2.4.7), having the same output voltage for both integrators, the factor ν must be equal to 2. However, due to the capacitor matching, the actual value of ν is hardly larger than 2 ($\nu^* \approx 2.14$).

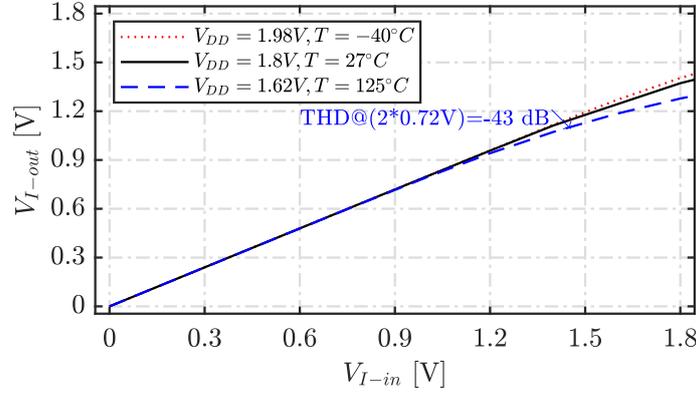


Figure 4.3.6 : Linearity of the OTA1 considering nominal, best and worst case conditions

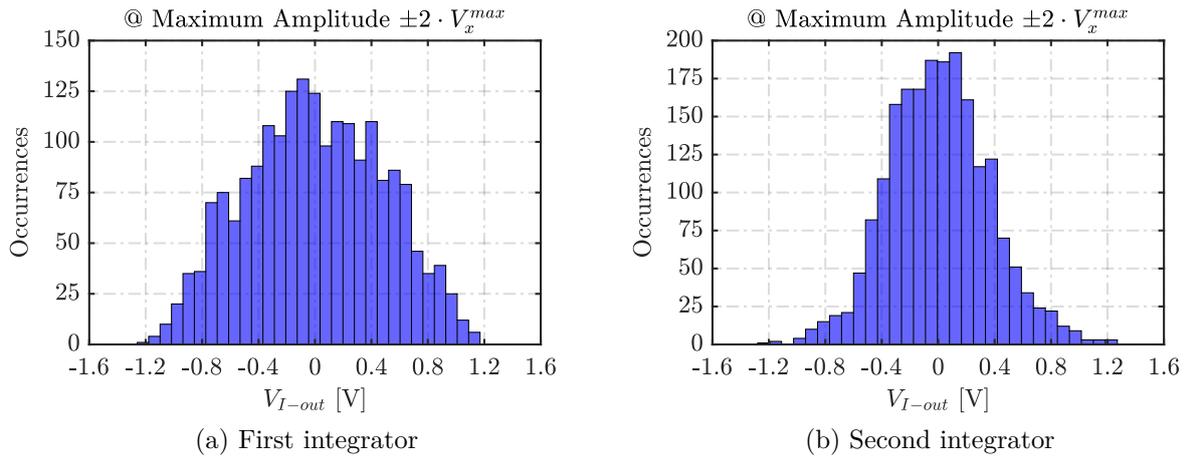


Figure 4.3.7 : Histogram of the integrator output, considering a modulator input of $2 \cdot V_x^{max}$, (a) first integrator, and (b) second integrator

Table 4.1 summarizes the maximum and minimum OTAs parameters' values considering PVT variations. As can be seen the results satisfy the requirements of the amplifiers.

Table 4.1 : Requirement, nominal, best and worst case parameter values of the OTAs

Parameter	Requirement		Nominal		Minimum		Maximum	
			1.8V, 27 °C		1.62V, $\bar{\mu} - 3\sigma$, 125 °C		1.98V, $\bar{\mu} + 3\sigma$, -40 °C	
	OTA1	OTA2	OTA1	OTA2	OTA1	OTA2	OTA1	OTA2
A [dB]	≥ 58 dB	≥ 58 dB	59.5dB	62.6 dB	58 dB	60 dB	63.2 dB	64.1 dB
GBW [MHz]	≥ 11 MHz	≥ 9 MHz	14.57 MHz	13.2 MHz	12.2 MHz	11 MHz	17 MHz	15.8 MHz
PM[°]	$\geq 70^\circ$	$\geq 70^\circ$	82°	83°	80.9°	81.2°	83.1°	83.1°
SR_r [MV/s]	≥ 7.7 MV/s	≥ 6 MV/s	10.6 MV/s	11.4 MV/s	9.8 MV/s	11 MV/s	13 MV/s	13.2 MV/s
SR_f [MV/s]			11.5 MV/s	13.8 MV/s	10.1 MV/s	13 MV/s	15.2 MV/s	15.7 MV/s
P_{rms} [μ W]	-	-	430 μ W	220 μ W	330 μ W	175 μ W	550 μ W	275 μ W

4.4 Capacitor bank

The layout of the modulator capacitors (half part) is depicted Fig. 4.4.1, they occupy including dummy capacitors an area of $380 \times 110 \mu m^2$. Common-centroid technique is also used to implement the capacitors C_{s1} with C_{i1} (dark-blue and red), C_{s2} with C_{i2} (blue and orange), C_{f1} with C_{f2} (move and black), and finally C_a with C_b (green and brown). All no-outlined capacitors in the capacitor-bank shown Fig. 4.4.1 are dummy devices.

The capacitors are implemented using single Metal Insulator Metal (MIM) device having a 106.8 fF for $10 \times 10 \mu m^2$ area. This capacitor possesses a very low voltage and temperature coefficients, their effect can be hardly neglected within the studied temperature range from -40 to 125 °C, and supply voltage variation $1.8V \pm 10\%$. Monte Carlo simulations were performed for 501-points 3σ process mismatch variation considering nominal conditions ($T = 27$ °C, $V_{DD} = 1.8$ V). The histograms of the main capacitors performing the coefficients a_1 , a_2 and c_1/c_2 are shown in Fig. 4.4.2.

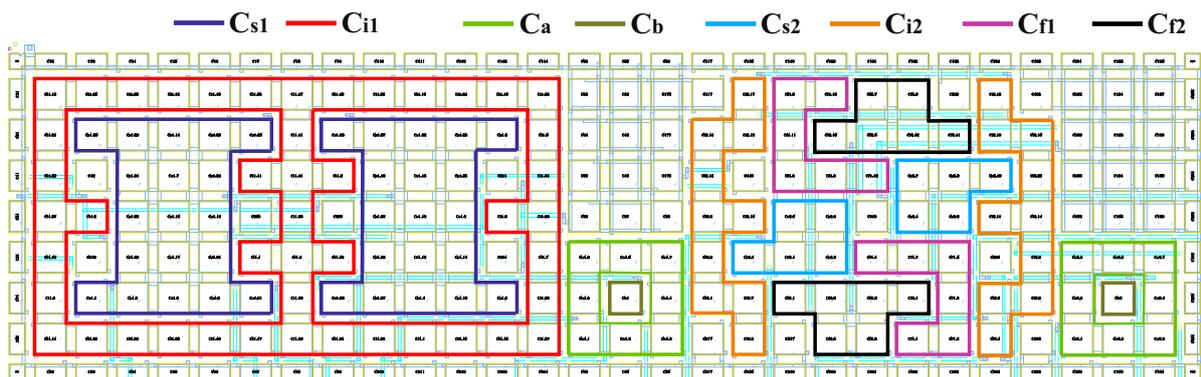


Figure 4.4.1 : Half part capacitor-bank of the modulator having an area of $380 \times 110 \mu m^2$. The capacitors are implemented using single Metal Insulator Metal (MIM) device having a 106.8 fF for $10 \times 10 \mu m^2$ area. All no-outlined capacitors are dummy devices

From the statistical results, it can be observed that a relative percentage error ($3\sigma/\bar{\mu}$) of lower than 7.5% is obtained for all capacitors (Fig. 4.4.2(a-f)). However, the coefficients a_1 , a_2 and c_1/c_2 resulting from capacitances ratio show a high immunity to process mismatch variations. Assuming a Gaussian distribution, the coefficients given in Fig. 4.4.2(g-i) achieve a relative error of lower than 0.05% considering 99.7% of the total samples ($\bar{\mu} \pm 3\sigma$). With this variation, the coefficients have almost no impact on the behavior of the modulator, i.e., SNR , as highlighted in Chap. 2 (subsec. 2.4.2).

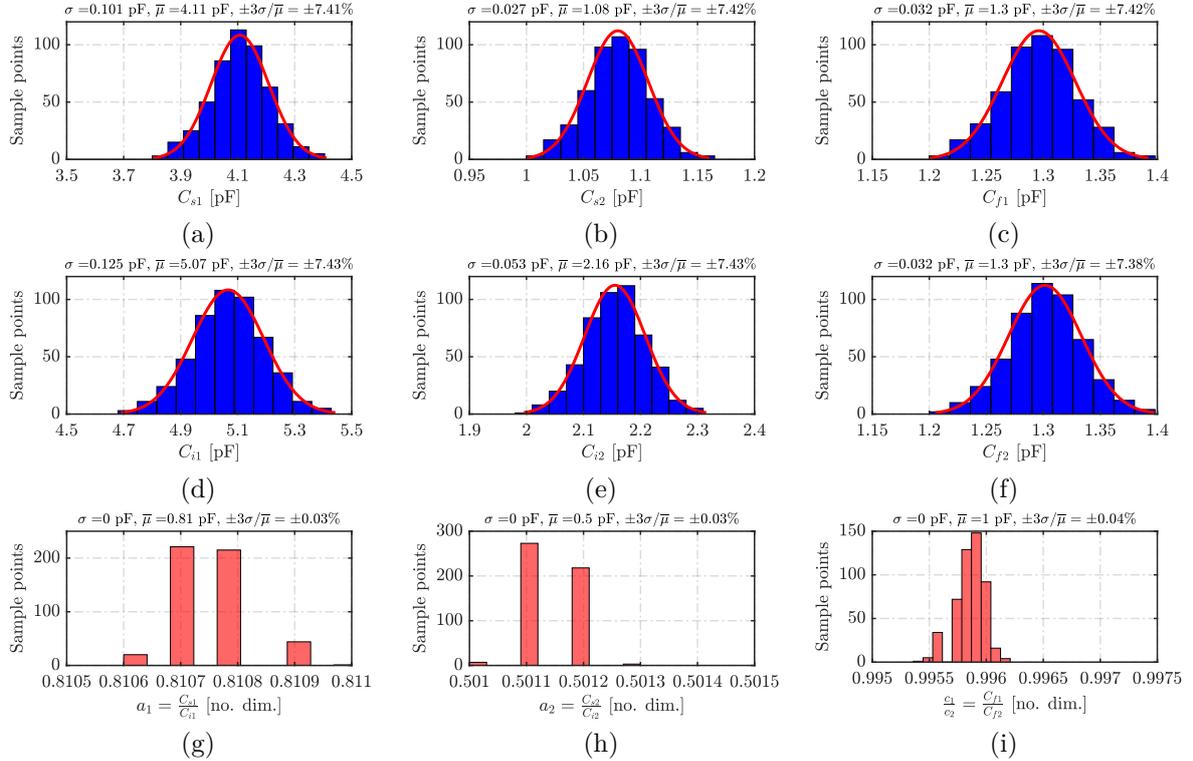


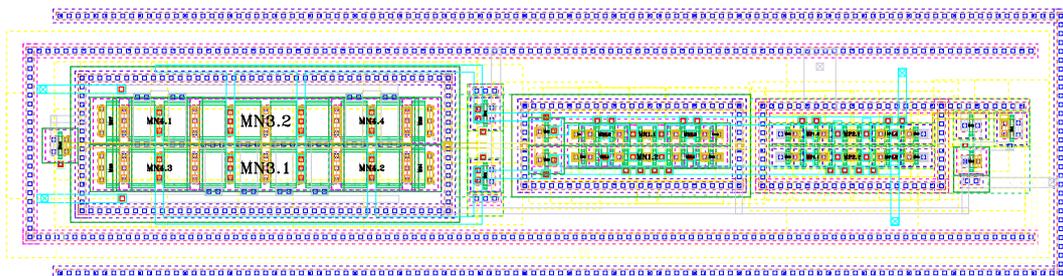
Figure 4.4.2 : Histograms of the sampling, the integrating and the feedforward capacitors, and the corresponding coefficients a_1 , a_2 , and c_1/c_2 considering 501-points Monte Carlo simulation for $T = 27^\circ\text{C}$ and $V_{DD} = 1.8\text{ V}$

4.5 Comparator and Non overlapping clock

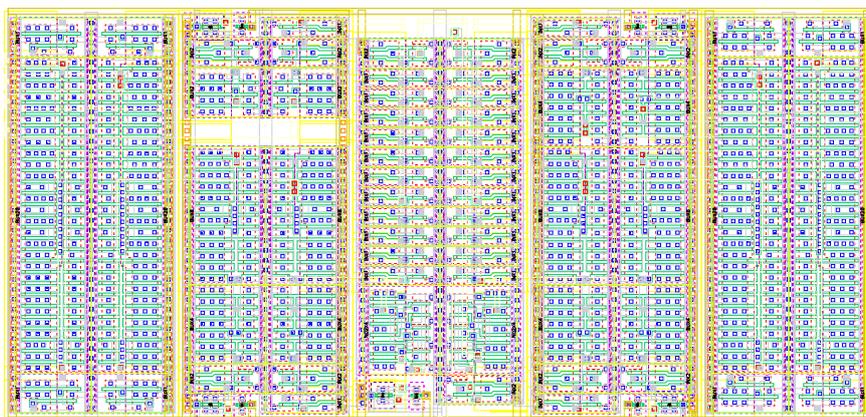
The layout of the double-tail comparator and the non-overlapping clock are given in Fig. 4.3.1, they occupy an area of $60 \times 15 \mu\text{m}^2$ and of $26 \times 55 \mu\text{m}^2$ respectively. The non-overlapping clock tree is implemented using 'nel' and 'pel' transistors, the supply voltage of this digital circuitry is separated from the supply voltage of the analog blocks of the modulator.

The post-layout time diagram of the non-overlapping clock considering nominal circuit conditions is depicted in Fig. 4.5.2. The simulation is carried out in the real operating

conditions. In fact, the clock outputs are connected to the modulator layout and are loaded by the equivalent parasitic capacitances. The dead-time is about 1 nanosecond between Φ_1 and Φ_2 , while it is about 180 picosecond between $\Phi_{1(2)}$ and $\Phi_{1(2)d}$. It is important to note that the inherent behavior of this circuit ensures that the delays are always present even when experiencing process mismatch effects, temperature and supply variations.



(a)



(b)

Figure 4.5.1 : (a) Layout of the double-tail comparator having an area of $60 \times 15 \mu m^2$, and (b) layout of the non-overlapping clock using 'nel' and 'pel' transistors, it has an area of $26 \times 55 \mu m^2$

It is worth recalling that, the delay time of the comparator is in order of magnitude of nanosecond [79], which is very small compared to the minimum clock period T_s . Hence, its effect can be ignored even when PVT variations are considered. Also, the offset error can be neglected since the $\Sigma\Delta$ modulator suppresses the non-idealities of the comparator as discussed in Chap. 2. For further detailed information and post layout PVT analysis on the comparator non-idealities, the interested reader can refer to [79], provided by our research team.

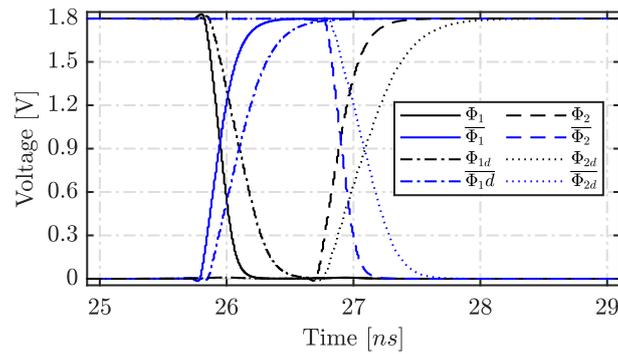


Figure 4.5.2 : Non-overlapping clock phases at room temperature and $V_{DD} = 1.8$ V

4.6 Modulator

The fully symmetrical modulator's layout is depicted in Fig. 4.6.1, the switches and the capacitor banks are distributed in a way to preserve a geometrical symmetry in both directions (as does the common centroid technique). Also, aligning the switches and place them as shown in Fig. 4.6.1, facilitate the connectivity with the non overlapping clock. The bias circuit is shared with OTA1 and OTA2, and placed between them to reduce the length of the rail metals providing the bias voltages. The modulator occupy an area of $530 \times 540 \mu m^2$.

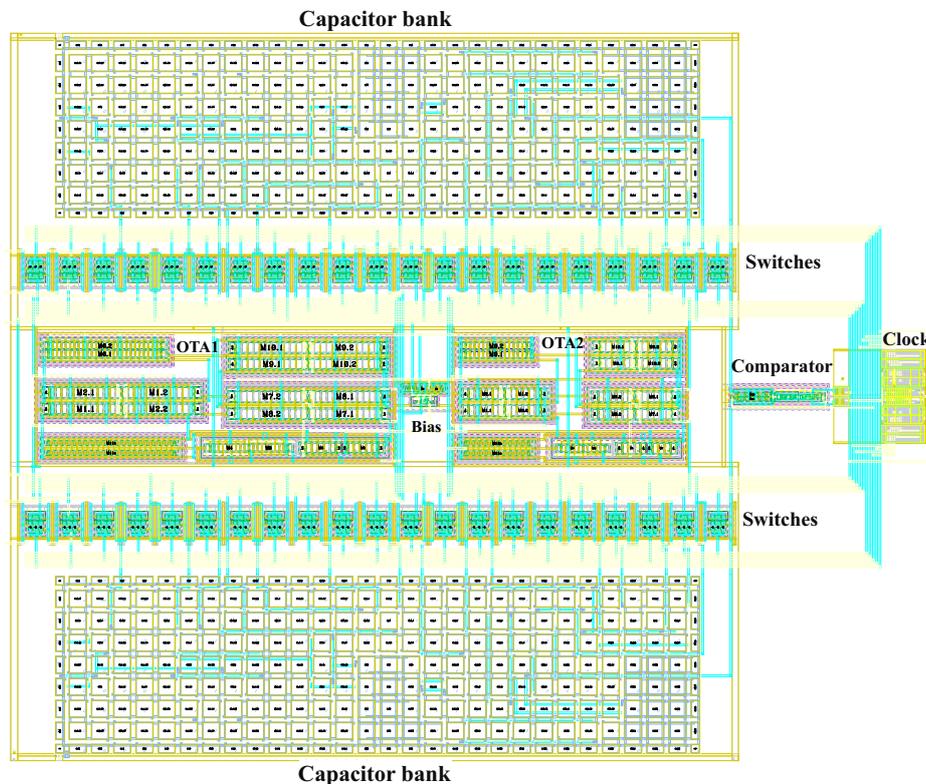


Figure 4.6.1 : Layout of the modulator having an area of $530 \times 450 \mu m^2$

4.6.1 PVT simulation

The post-layout simulation of the modulator shown in Fig. 4.6.2 is much time consuming, which makes it impractical Monte Carlo simulation. In fact, the response of the modulator was validated using nominal and limit condition simulations (as in Fig. 4.3.6). Note that the performance of the modulator depends directly on the OTA behavior, thus the modulator was simulated using the limit conditions given in Table 4.1 ($V_{DD} = 1.98$ V for $T = -40$ °C, and $V_{DD} = 1.62$ V for $T = 125$ °C). First, the ratiometric behavior of the modulator is studied considering transient simulation with DC inputs signals and 1MHz sampling frequency. The input signals V_x and V_y have an amplitude of $V_{ref} + \delta V_x$ and $V_{ref} - \delta V_y$ ($V_{ref} = 0.46$ V), for simplicity δV_y is chosen equal to δV_x , this quantity is changed from 0 to 0.3 V (slightly larger than $0.57 \cdot V_{ref} = 0.263$ V) and stepped by 0.01 V after averaging the output value every 256 μ s ($OSR \cdot T_s$). Finally the RM values are extracted by taking the differential output average value normalized to the reference voltage of the quantizer (comparator) V_{DD} , i.e. $RM = \frac{\langle D \rangle - \langle \bar{D} \rangle}{V_{DD}} \equiv \frac{\delta V_x + \delta V_y}{2 \cdot V_{ref}}$.

The results considering nominal, worst, and best case circuit conditions are depicted in Fig. 4.6.2 for (a) typical, (b) worst power, and (c) worst speed transistor model. It can be observed that first, the circuit possess high reliability to PVT variations, and almost no degradation can be noticed between the three corners. However, for certain input signals, the input may not be properly encoded by the modulator. That is, there is a range of input for which the modulator may produce the same average output value. This range is known as a dead zone. In a first-order $\Sigma\Delta$ M, dead zones occur for every limit cycle. Since the limit cycles exist with any rational input, this can be rephrased as stating that dead zones exist in the neighborhood of every rational input. Similar phenomena exist in second-order $\Sigma\Delta$ M. Limit cycle prevention is traditionally achieved by adding a dithering sequence just prior to quantization [46], or more advanced by detecting and removing technique as described in [80]. However, this issue is not investigated in this work, but still a very important point that should be envisioned to optimize the modulator response.

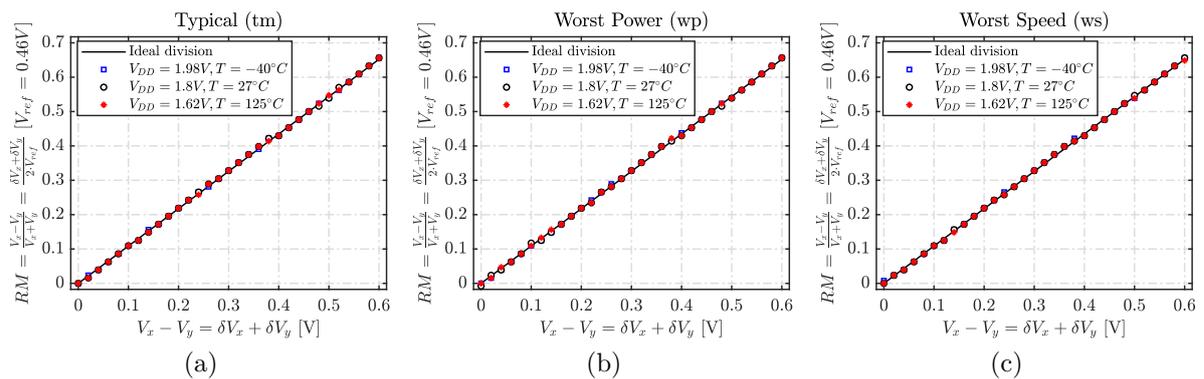


Figure 4.6.2 : Ratiometric behavior of the modulator, (a) typical, (b) worst power, and (c) worst speed, considering transient simulation with DC inputs signals and 1MHz sampling frequency. The input signals V_x and V_y have an amplitude of $V_{ref} + \delta V_x$ and $V_{ref} - \delta V_y$ ($V_{ref} = 0.46$ V and $\delta V_y = \delta V_x$), δV_x is changed from 0 to 0.3 V and stepped by 0.01 V every 256 μ s ($OSR \cdot T_s$)

The PSD of the modulator bitstream at $T = 125\text{ }^\circ\text{C}$ and $V_{DD} = 1.8\text{ V}$ obtained from transient simulation (Hann-windowed NFFT of 7630 points) is depicted in Fig. 4.6.3. The output bitstream is carried out considering near DC input signal having an amplitude of $0.57 \cdot 2V_{ref}$, and 1MHz sampling frequency. It can be indicated that the SNR is roughly 94 dB with a corresponding $ENOB$ of 15.34 bits.

Noting that the obtained resolution is slightly lower than the expected of 16 bits. However, more accurate results of the SNR may be achieved with a higher number of NFFT points, but the transient noise simulation will take very long times. Moreover, the actual resolution was evaluated considering the worst case conditions of $T = 125^\circ$ and signal bandwidth of $f_{MEMS}/Q = 2\text{ kHz}$. Thus, a higher resolution can still be achieved for a higher resonator quality factor $Q > 500$ and lower resonant frequency $f_{MEMS} < 1\text{ MHz}$. In other words, as the RM- $\Sigma\Delta$ is clocked by the resonator frequency $f_s = f_{MEMS}$, the oversampling ratio $OSR \equiv f_s/BW \propto Q$. However, this proportionality is valid as long as the error due to the amplifier finite DC-gain still negligible with respect to LSB as discussed in Chap. 2. Therefore, for a very high Q (narrow bandwidth), the maximum achievable resolution will be restricted and may be degraded for a given DC-gain of the amplifier.

It worth mentioning that the main limitation of the RM- $\Sigma\Delta$ is that the reference voltage V_{ref} is involved into the sensing output signals, this limits its maximum achievable value, which is calculated around 0.46 V. In fact, a typical value of V_{ref} in a $\Sigma\Delta$, considering 1.8 V supply voltage, could be at least $2 \times$ larger than the actual one; meaning that at least 3 dB improvement in the SNR could be gained with a higher V_{ref} . Meanwhile, with a higher V_{ref} the OTAs specifications, as well as the optimum coefficient values must be restudied following the same methodology presented in Chap. 2. Table 4.2 summarizes and compares the specifications of the proposed RM- $\Sigma\Delta$ with the architecture developed in [45].

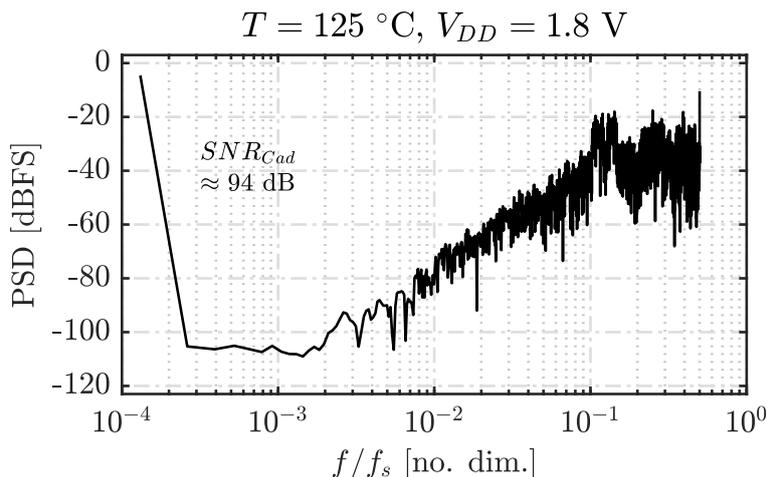


Figure 4.6.3 : PSD of the bitstream obtained from transient simulation (Hann-windowed NFFT of 7630 points), for $T = 125\text{ }^\circ\text{C}$, $V_{DD} = 1.8\text{ V}$, 1MHz sampling, and considering a near DC input signal having an amplitude of $0.57 \cdot 2V_{ref}$

Table 4.2 : Specifications comparison of the proposed RM- $\Sigma\Delta$ M and the architecture developed in by Fekri et al.

	This work	Fekri et al. [45]
Technology	SOI-XH018 (0.18 μm)	Si/Ge BiCMOS (0.35 μm)
Domain	DT	CT
Temperature range	$-40 \leq T[^\circ C] \leq 125$	$T = 27^\circ C$
Sample rate	$f_s \leq 1$ MHz	$f_s = 1$ MHz
Data rate	$BW \leq 2$ kHz	$BW \leq 1$ kHz
Effective number of bits	$ENOB \approx 15.34$ bits	$ENOB \approx 15$ bits
Dynamic range	$DR \leq 0.6$	$DR < 0.7$
Reference voltage	$V_{ref} = 0.46$ V	$V_{ref} = 0.45$ V
Supply voltage	$V_{DD} - V_{SS} = 1.8$ V	$V_{DD} - V_{SS} = 3.3$ V
Power consumption @1.8 V	$P_{rms} \approx 0.8$ mW	$P_{rms} \approx 2.8$ mW
Total area	$530 \times 450 \mu m^2$	—
$FOM = 20 \log \left(\frac{2^{ENOB} \times BW[kHz]}{P_{rms}[mW]} \right)$	98 dB	81 dB

4.7 Conclusion

In this chapter, the layout of the analog and digital blocks of the proposed RM- $\Sigma\Delta$ M are presented. The switch is first analyzed, and the on-resistance average value is evaluated against PVT variations. It exhibits a worst case on-resistance of lower than 150 Ω , ensuring a complete charge transfer within $T_s/2$. PVT simulation results of OTA1 and OTA2, including the basing circuit are then detailed. They show a high DC-gain, and GBW thermal stability that from 27 to 125 $^\circ C$ decrease only by (0.7 dB, 1.6 MHz) and (0.3 dB, 1.2 MHz) for OTA1 and OTA2 respectively. These results validate the temperature aware g_m/I_d -based sizing approach proposed in the previous chapter. The worst case values of these parameters are observed at $\bar{\mu} - 3\sigma$, $V_{DD} = 1.62$ V and $T = 125^\circ C$: they are (58 dB, 12.2 MHz) and (60 dB, 11 MHz) which always respect the requirement. In addition, the amplifiers show a good stability margin with $PM > 80^\circ$ under any PVT conditions. They consume without the biasing circuit around 430 μW and 220 μW from 1.8 V supply. The modulator coefficients are then experienced against process and mismatch effects. From the statistical results, it was observed that the coefficients achieve a relative error of lower than 0.05% considering 99.7% of the total samples ($\bar{\mu} \pm 3\sigma$). With this variation the coefficients have almost no impact on the performance of the modulator.

A fully symmetrical assembly of the full layout design was then performed to help improve the RM- $\Sigma\Delta$ M immunity from the effect of first-order cross-chip gradients, such as temperature and mismatch. The RM- $\Sigma\Delta$ M is then evaluated using PVT Corner simulations comprising typical, worst speed and worst power. The final results of the ratiometric functionality highlight the design features of relatively high thermal stability, and robustness against process and supply variation. Since the transient noise simulation of the entire

modulator takes too much time, the PSD of RM- $\Sigma\Delta$ M output bitstream is only carried out at the maximum temperature value $T = 125\text{ }^\circ\text{C}$, and worst case OSR condition ($Q = 500$, $f_{MEMS} = 1\text{MHz}$), considering typical process model and supply. The obtained SNR was around 94 dB corresponding to an $ENOB$ of 15.34 bits at the maximum dynamic range, i.e., 0.57. Since the $OSR \propto Q$, a 16 bits resolution can readily be achieved with $Q > 500$, which is typically the case considering the modern MEMS resonator. The RM- $\Sigma\Delta$ M interface has an area of $530 \times 450\ \mu\text{m}^2$ using SOI-180 nm technology and consumes 0.8 mW from 1.8 V at room temperature.

Conclusion and perspectives

Manuscript Conclusions

Our research team focuses on developing new high-performance sensing architectures based on coupled MEMS resonators, from mechanical to acquisition. As in every sensor, the sensitivity to the measured must be maximized, and the sensitivity to every other fluctuations, such as drifts and noises, must be compensated for enhanced resolution.

Several approaches exist in literature to either suppress or compensate for the drift effect. They include controlling the resonator temperature by ovenizing it, digital compensation with microprocessors and temperature sensors, or differential sensor architectures. In recent years, differential architectures based on weakly-coupled-resonators WCRs such as, mutually-injection-locked-oscillators MILOs have emerged as a good candidate for high thermal stability measurement. They target the amplification of difference in mass or stiffness of two resonators while highly unaffected by thermal variations equally affecting both resonators. However, noise sources are inherent in the system, and a more sophisticated solution must be carried out in order to minimize their effects.

For this purpose, a bilinear amplitude-ratio metric measurement B based on WCRs has been proposed. Being B unaffected by the resonators' A-f effect, it is possible to work under a higher resonator driving force so that a higher signal to noise ratio can be achieved. These interesting properties of the bilinear output metric are validated theoretically for any WCRs architectures and experimentally by considering MILOs architectures.

Moreover, this thesis provides a high resolution and temperature aware amplitude ratio readout interface for the bilinear output metric B . This interface is targeted for automotive applications with a temperature up 125 °C and 16 bits resolution. The ratiometric interface possesses good robustness against process, mismatch, and supply variations. It is adapted to any WCRs having a locking range up to 0.57 and a frequency of 1 MHz or lower. The circuit implementations are made using SOI-180nm technology of XH018 series from X-FAB Silicon Foundries. It has an operating temperature up to 175 °C, extending beyond the requirement while providing a very low leakage current.

Review of work and novelty proposed in this thesis

- An original system-level review of existing resonant sensor architectures, including conventional and tow weakly coupled resonator sensors was proposed. A general figure of merit for the different output metrics used in theses architectures was defined to compare their performance, in the linear and the nonlinear regimes. It have been highlighted that the performance, i.e., resolution, of the conventional metrics such as phase and frequency of all architectures are limited by the A-f effect, whereas the amplitude-ratio keeps improved even beyond the critical amplitude [13, 19]. Since the amplitude ratio is an unbounded quantity, we studied the bilinear amplitude-ratio output metric with similar advantages, i.e., sensitivity and resolution, but being bounded and, therefore, more amenable to analog-to-digital conversion and implementation in integrated circuits [18]. Possible state-of-the-art solutions to implement the corresponding temperature aware readout interface with a 16 bits resolution are then discussed.

- Among different existing solutions, the readout interface based on $\Sigma\Delta$ converter has shown to be most suitable for high-resolution and moderate-speed applications (< 1 MHz). A comparative study, including implementation domain, loop order, quantizer resolution, and loop topology was then investigated. It has been found that the most appropriate architecture for the application considered in this thesis can be obtained using discrete-time feedforward second order modulator [17]. An optimization step of the loop coefficients was next done to meet the specifications of a theoretical resolution of > 16 bits and a maximum stable amplitude of larger than the sensor's locking range, i.e., 0.57. Finally, the non-idealities of the integrator, which is the major source of errors in the modulator, were characterized and specified in order to not degrade the theoretical performance when temperature up to 125 °C. The specifications were determined based on a new system-level analysis using g_m/I_d methodology and then validated with verilogA model using Cadence Spectre® simulation.

- The transistor-level design of the analog circuits used to implement the ratiometric interface, including switch, 1-bit DAC integrator, amplifier, comparator, and non-overlapping clock were then detailed. The design was done using SOI-180nm process technology from the X-FAB Silicon Foundries, and prioritizing the circuit reliability against Process-Voltage-Temperature variation over the area and power consumption. The switch is based on the transmission gate architecture that overcomes the ordinary switch design limitations. It shows a low, and relatively stable on-resistance along a wide swing input level even in the presence of PVT variations. Since the sensor may has a single or differential output, single to differential, and fully differential 1-bit DAC integrator implementations are investigated. Both are DT designed and are, parasitic insensitive, and have the same noise performance. A special attention is given for the OTA core of the integrator since their imperfections directly affect the modulator performance, especially at high temperature. For this purpose, and to complete the system level modeling flow based on g_m/I_d approach, the thermal stability analysis of the main transistor parameters ($A \propto g_{ds}$, $GBW \propto g_m$ and $SR \propto I_d$) is also developed using the g_m/I_d methodology. Finally, from the proposed temperature analysis and from the simulation, the optimum

operating condition, i.e. g_m/I_d , of g_{ds} , g_m , I_d was used to design the OTA and its biasing circuit.

- A fully symmetrical assembly of the final layout design was then performed to help improve the circuit immunity from the effect of first-order cross-chip gradients, such as temperature and mismatch. The RM- $\Sigma\Delta$ M is then evaluated using PVT Corner simulations comprising typical, worst speed, and worst power. The final results of the ratiometric functionality highlight the design features of relatively high thermal stability, and robustness against process and supply variation, for an output dynamic range slightly higher than 0.57. Since the transient noise simulation of the entire modulator takes too much time, the PSD of RM- $\Sigma\Delta$ M output bitstream is only carried out in the worst case conditions, by considering maximum temperature value $T = 125^\circ\text{C}$, minimum MEMS quality factor ($Q = 500$) and higher sampling frequency ($f_{MEMS} = 1\text{ MHz}$). The obtained SNR under typical process model and supply was around 94 dB with a corresponding $ENOB$ of 15.34 bits, at the maximum dynamic range, i.e. 0.57. The RM- $\Sigma\Delta$ M interface has an area of $530 \times 450\ \mu\text{m}^2$ and consumes 0.8 mW from 1.8 V at room temperature.

Research Perspectives

The final tape out of this work is depicted in Fig. 4.7.1(b), it comprises the RM- $\Sigma\Delta$ M, a stand-alone amplifier, a stand-alone comparator, and temperature sensor. The I/O ring has 24 input/output pins attributed to the signals as defined in Fig. 4.7.1(c), the size of the bondpad opening is $1520 \times 1520\ \mu\text{m}^2$.

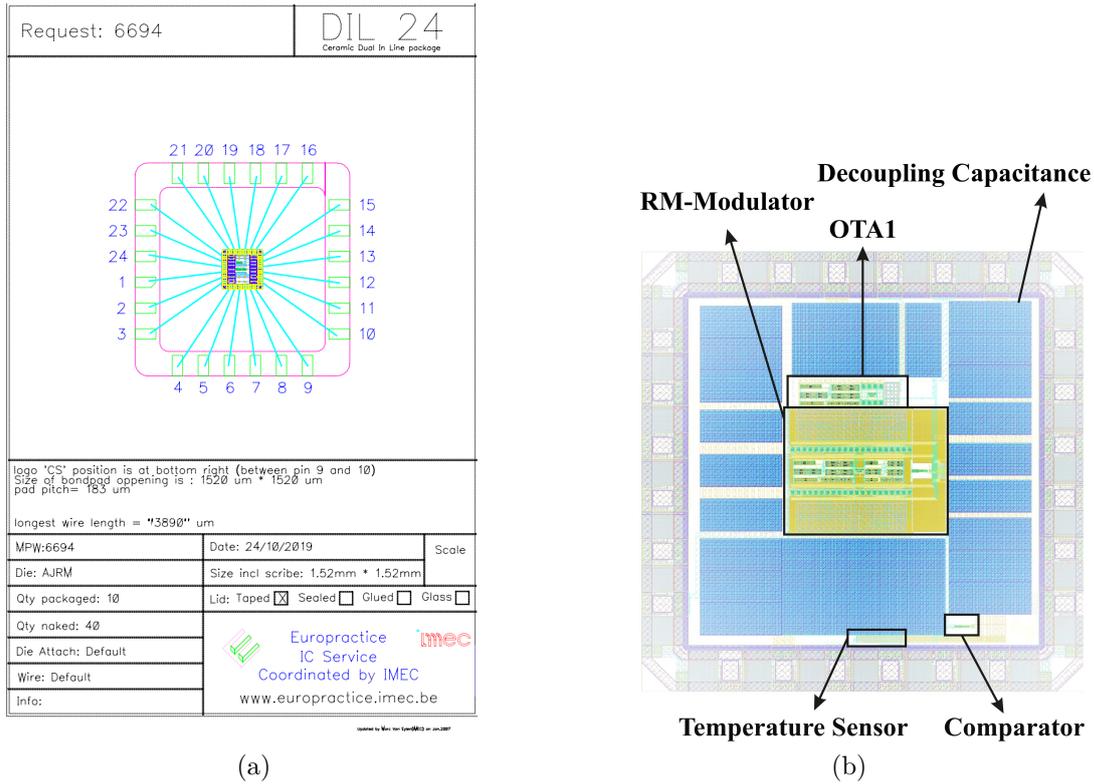


Figure 4.7.1 : The final, (a) tape out, (b) layout, and (c) schematic of the circuit

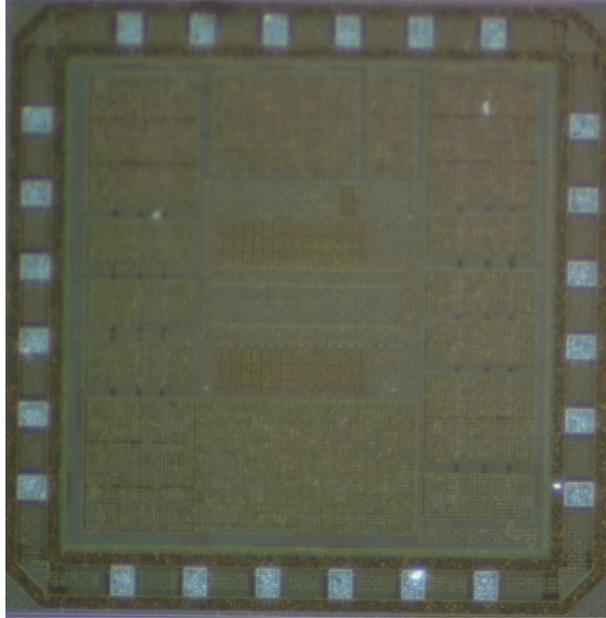


Figure 4.7.2 : Die photograph of the chip

The stand-alone amplifier is a copy of the OTA1 so that its performance can be separately extracted. The stand-alone comparator is added to validate its performance with the results presented in [79], that provided by our research team. The temperature sensor is a simple ring oscillator structure that senses the temperature of the chip and provide a frequency change at its output. Decoupling capacitors are added in the empty spaces to prevent density issue, and to decouple the analog supply voltage from the digital one.

The die photograph of the chip is depicted in Fig. 4.7.2. Due to the lack of time the experimental setup and measurement of the proposed RM- $\Sigma\Delta$ M have not been accomplished. The next points of this work will be divided as follow. First of all, the fabricated chip will be measured to verify the performance of the RM- $\Sigma\Delta$ M in term of resolution and robustness against temperature and supply variation. In this case, the RM- $\Sigma\Delta$ M will be tested separately from MILO, the input signals as well as the clock signal will be provided by off-chip signal sources. A resolution of 15 to 16 bits or a SNR of more than 92 dB is theoretically expected at this point.

In a second phase, the entire circuit (MILO + RM- $\Sigma\Delta$ M) will be tested. In this phase the RM- $\Sigma\Delta$ M will be clocked by the resonator frequency, and the MILO output signal will be demodulated and applied to the RM- $\Sigma\Delta$ M. The system will then be tested under different MILO operating states (linear and nonlinear); and the results of the amplitude ratio measured at the output of RM- $\Sigma\Delta$ M will be compared to the conventional measurements (amplitude-difference and phase-difference) to investigate our approach. Moreover, the effect of the resonator clock jitter on the modulator performance will be treated. Subsequently, the fabricated stand-alone OTA will be tested. First the performance of the OTA will be determined under different temperature conditions, and compared with the results obtained from post layout simulation. The OTA will then be tested in a feedback

configuration with external capacitors to validate the integrator model developed in Chap. 2.

Many circuit level improvement can be performed to enhance the resolution and the accuracy of the modulator response. For instance, the correlated double sampling technique (CDS), and the chopper stabilization technique (CHS) can be performed in the first integrator to further minimize the low frequency noise and increase the SNR. Besides, by providing a technique for increasing the reference voltage, i.g., from 0.46 to 1 V, can also improve the resolution of the modulator. Finally, limit cycle prevention techniques, such as adding a dithering, or detecting and removing approach, can also be implemented to eliminate the dead zone issue.

Considering the proposed MILO sustaining electronics given in appendix E; to complete the design flow, the layout of the proposed enhanced gain transimpedance amplifier EGTIA should be realized to verify that the parasitic capacitors, mismatch and process do not affect its performance. Subsequently, the layout of the MILO architecture including EGTIA must be realized and compared to the architecture presented in [14]. It worth mentioning that to make the MILO fully symmetrical, a delay buffer stage can be added to the mixer to compensate the delay effect in the inverter [14].

Appendices

Appendix A

Parametric analysis of nonlinear duffing resonator

The dimensionless equation governing a single duffing resonator subject to stiffness variation can be expressed as,

$$\frac{d^2x}{dt^2} + \frac{1}{Q} \frac{dx}{dt} + x(1 + \epsilon + \gamma x^2) - f(t) = n(t). \quad (\text{A.0.1})$$

This equation can be studied by averaging or harmonic balance techniques, one may assume that:

$$x(t) = X \sin(\Omega t + \theta), \quad (\text{A.0.2a})$$

$$f(t) = F \sin(\Omega t). \quad (\text{A.0.2b})$$

Replacing (A.0.2) in (A.0.1) and projecting (A.0.1) on $\sin(\Omega t + \theta)$ and $\cos(\Omega t + \theta)$, the system state "s" around the quasi-static limit (very close to the carrier) is then governed by the 2 set of equations bellow:

$$g_1(s) \equiv X(1 + \epsilon + \frac{3}{4}\gamma X^2 - \Omega) - F \cos(\theta) = N_{\sin}, \quad (\text{A.0.3a})$$

$$g_2(s) \equiv \frac{\Omega}{Q} X - F \sin(\theta) = N_{\cos}. \quad (\text{A.0.3b})$$

Considering closed loop sensing mode, θ is constant and given by the steady state value, i.e. $\theta_{ST} = \pi/2$, and the system state $s = [X, \Omega]^T$. This state is observed via an

output metric $M(s)$ whose sensitivity to the quantity of interest and to thermomechanical fluctuations are interested in, to determine the performance of a sensor. Letting $X = X_{ST} + \delta X$ and $\Omega = \Omega_{ST} + \delta\Omega$, and studying the resulting linearized system, the fluctuation of any output metric to the thermomechanical noise n , ($\epsilon = 0$) can be expressed by,

$$\delta M|_{\epsilon=0} = \frac{\partial M}{\partial s} \times J_s^{-1} \times [N_{sin}, N_{cos}]^T, \quad (\text{A.0.4})$$

and to the quantity of interest ϵ , ($n = 0$) by,

$$\delta M|_{n=0} = \frac{\partial M}{\partial s} \times J_s^{-1} \times J_\epsilon \times \epsilon; \quad (\text{A.0.5})$$

where J_s and J_ϵ are the jacobian matrices of $g(s)$ with respect to s and ϵ respectively. The sensitivity to epsilon S_ϵ^M and to noise S_n^M of a metric M can be derived from (A.0.5) and (A.0.4) respectively:

$$S_\epsilon^M = \frac{\partial M}{\partial s} \times J_s^{-1} \times -J_p, \quad (\text{A.0.6a})$$

$$S_n^M = \left| \frac{\partial M}{\partial s} \times J_s^{-1} \right|, \quad (\text{A.0.6b})$$

Applying this analysis on the system described by (A.0.3) with the state $s = [X, \Omega]^T$, J_s and J_ϵ are found as:

$$J_s = \begin{bmatrix} 1 + \frac{9}{4}\gamma X_{ST}^2 - \Omega_{ST}^2 & -2\Omega_{ST} X_{ST} \\ \Omega_{ST}/Q & X_{ST}/Q \end{bmatrix} \quad (\text{A.0.7a})$$

$$J_\epsilon = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \quad (\text{A.0.7b})$$

This analysis can be directly projected to the weakly (actively or passively) coupled resonator sensors with the state $s = [X, Y, \phi]^T$. This system is governed by the following 3 set of equations:

$$g_1^x(s) \equiv \frac{X}{2Q} - \frac{1}{2}F_{\cos x} = \frac{1}{2}N_{\cos x}, \quad (\text{A.0.8a})$$

$$g_2^y(s) \equiv \frac{Y}{2Q} - \frac{1}{2}F_{\cos y} = \frac{1}{2}N_{\cos y}, \quad (\text{A.0.8b})$$

$$g_3^\phi(s) \equiv \left(\epsilon + \frac{3}{8}\gamma X^2 - \frac{3}{8}\gamma Y^2 \right) - \frac{1}{2} \left(\frac{F_{\sin x}}{X} - \frac{F_{\sin y}}{Y} \right) = \frac{1}{2} \left(\frac{N_{\sin x}}{X} - \frac{N_{\sin y}}{Y} \right). \quad (\text{A.0.8c})$$

In this case the jacobian matrices J_s and J_ϵ are of $g(s)$ are as follow:

$$J_s = \begin{bmatrix} \frac{1}{2Q} & 0 & -\frac{1}{2} \frac{\partial F_{\cos x}}{\partial \phi} \\ 0 & \frac{1}{2Q} & -\frac{1}{2} \frac{\partial F_{\cos y}}{\partial \phi} \\ \frac{3}{4}\gamma X_{ST} + \frac{F_{\sin x}}{2X_{ST}^2} & -\frac{3}{4}\gamma Y_{ST} - \frac{F_{\sin x}}{2Y_{ST}^2} & -\frac{1}{2} \left(\frac{\partial F_{\sin x}}{\partial \phi} \frac{1}{X_{ST}} - \frac{\partial F_{\sin y}}{\partial \phi} \frac{1}{Y_{ST}} \right) \end{bmatrix} \quad (\text{A.0.9a})$$

$$J_\epsilon = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}, \quad (\text{A.0.9b})$$

Appendix B

Noise shaping

To understand the noise shaping operation, a first order modulator is analyzed considering the simplified linear model shown in Fig. B.1. In this model, the loop filter is defined by transfer function $H(z)$ and the quantizer is replaced by a gain g (usually < 1) [46] plus a quantization error (V_Q). All voltages are normalized to V_{ref} and the quantizer full scale voltage (V_{Q-FS}) is assumed equal to $2V_{ref}$ so that $\hat{V}_{OUT}(z) = \pm 1$.

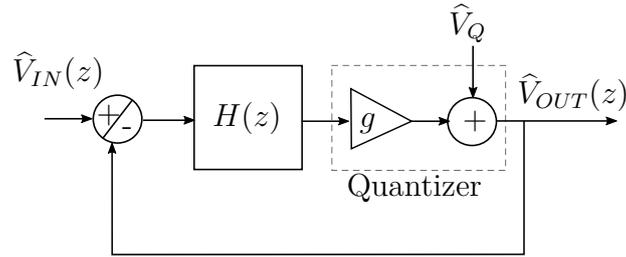


Figure B.1 : Linearized model of the modulator depicted in Fig. 2.2.1. All voltages are normalized to V_{ref}

Assuming that the loop filter is a discrete time (DT) forward-Euler integrator with constant coefficient a , the modulator output in the Z -domain can be determined by:

$$H(z) = a \frac{z^{-1}}{1 - z^{-1}}, \quad (\text{B.0.1a})$$

$$\hat{V}_{OUT}(z) = gH(z) \times (\hat{V}_{IN}(z) - \hat{V}_{OUT}(z)) + \hat{V}_Q(z), \quad (\text{B.0.1b})$$

leading to,

$$\begin{aligned} \hat{V}_{OUT}(z) &= \left(\frac{agz^{-1}}{1+(ag-1)z^{-1}} \right) \times \hat{V}_{IN}(z) + \left(\frac{(1-z^{-1})}{1+(ag-1)z^{-1}} \right) \times \hat{V}_Q(z), \\ &\equiv STF(z) \times \hat{V}_{IN}(z) + NTF(z) \times \hat{V}_Q(z), \end{aligned} \quad (\text{B.0.2})$$

where STF and NTF stand for “signal transfer function” and “noise transfer function” respectively. In order to optimize the overall performance of the modulator, the term $(ag - 1)$ in the denominator of both NTF and STF should be minimized. In ideal case modulator ($ag = 1$), STF and NTF are expressed by:

$$STF(z) = z^{-1} \quad (\text{B.0.3a})$$

$$NTF(z) = (1 - z^{-1}) \quad (\text{B.0.3b})$$

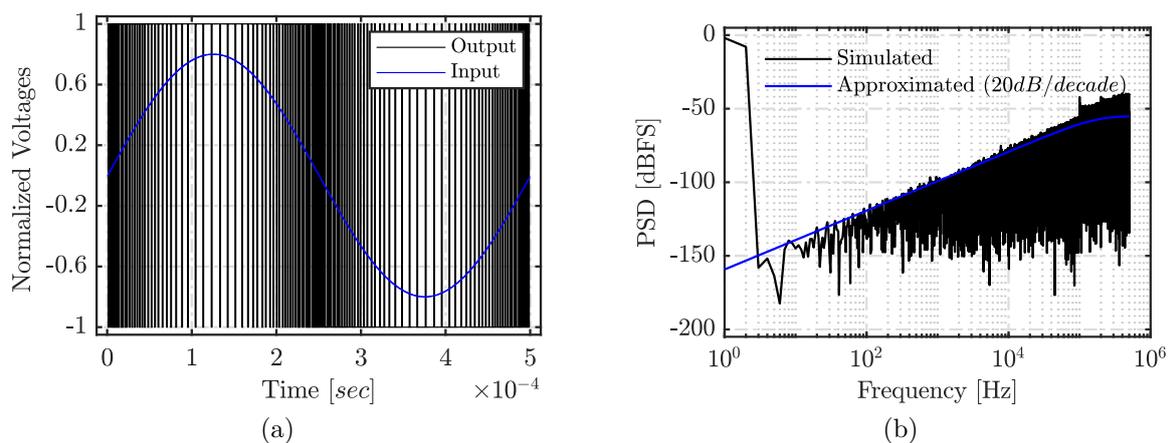


Figure B.2 : Output response of a first order $\Sigma\Delta\text{M}$: (a) output bit stream for an input frequency of 2 kHz, (b) power spectrum for an input frequency of 1 Hz. The input normalized signal amplitude is fixed to 0.8. The sampling frequency is fixed to 1 MHz

The ideal frequency response of the STF is a unit delay, whereas that of the NTF is a first order high pass filter. Thus, the input signal is just replicated at the output with no change, while the quantization noise is attenuated at low frequencies and amplified at high frequencies. The output responses of a first-order $\Sigma\Delta\text{M}$ simulated with MATLAB® $\Sigma\Delta$ toolbox [46] are depicted in Fig. B.2. Fig. B.2(a) shows the output encoded bit-stream for an input sine-wave with frequency 2 kHz and amplitude of 0.8. It can be seen that as the input amplitude decreases, the number of output high states decreases with respect to the number of low states. For instance, when the signal reaches its maximum, most of the output state is 1, whereas when the signal is near its minimum, the output is mainly -1. As a result, the average of the output bitstream follows the average of the input amplitude. Fig. B.2(b) shows the output power spectral density (PSD) for an input sine-wave with frequency 1 Hz and amplitude of 0.8. It can be observed that the quantization noise is pushed to the high frequencies with a slope of 20dB/decade, in agreement with the linearized model given in Fig. B.1. This noise shaping process can be improved by increasing the order (L) of the loop filter $H(z)$. The ideal STF and NTF

for a L^{th} order modulator are given by:

$$STF(z) = z^{-L} \quad (\text{B.0.4a})$$

$$NTF(z) = (1 - z^{-1})^L \quad (\text{B.0.4b})$$

Figure B.3 shows the shape of $NTF(z)$ from the first to the fifth-order. It can be observed that when the modulator order increases, the in-band noise decreases, and the out-of-band noise increases. This increase of out-of-band noise can be eliminated by using a higher-order decimation filter, typically with the same or higher order of the loop filter.

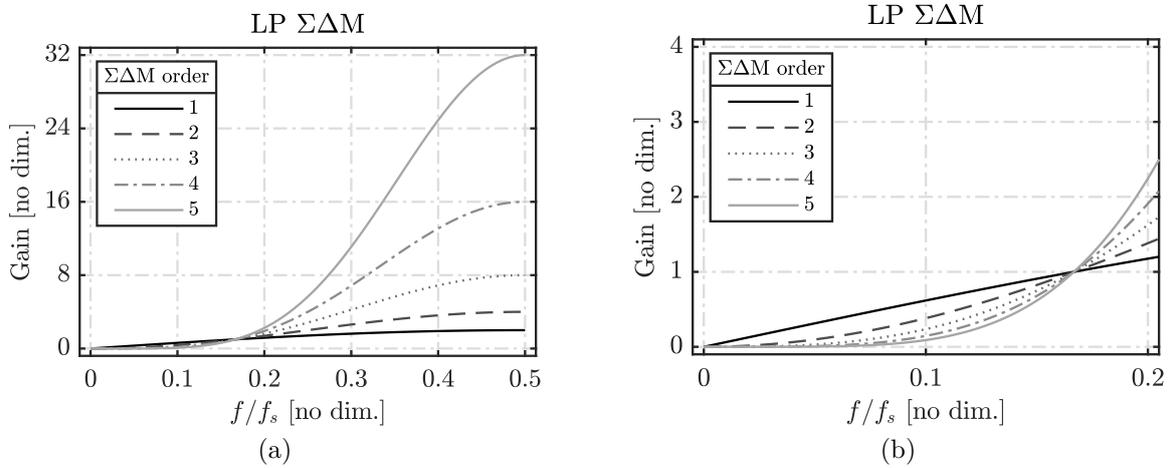


Figure B.3 : Noise shaping of low-pass (LP) loop filter.

Appendix C

Integrator transfer function

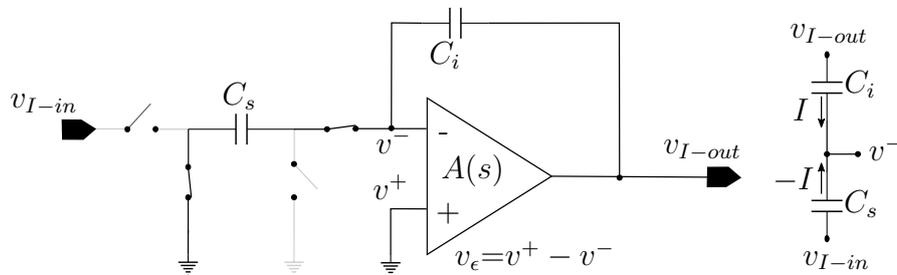


Figure C.1 : Single ended parasitic insensitive integrator during the integrating phase

During the integrating phase of the circuit shown in Fig. C.1, the potential at the negative terminal of the amplifier (v^-) is determined as follow,

$$v^- + v_{I-int} = \frac{C_i}{C_i + C_s} \cdot (v_{I-out} + v_{I-in}) \equiv v^- = \frac{1}{1+a} \cdot (v_{I-out} - a \cdot v_{I-in}), \quad (\text{C.0.1})$$

where $a = C_s/C_i$ is the integrator coefficient. From (C.0.1), the circuit given in Fig. C.1 can be schematically represented as shown in Fig. C.2.

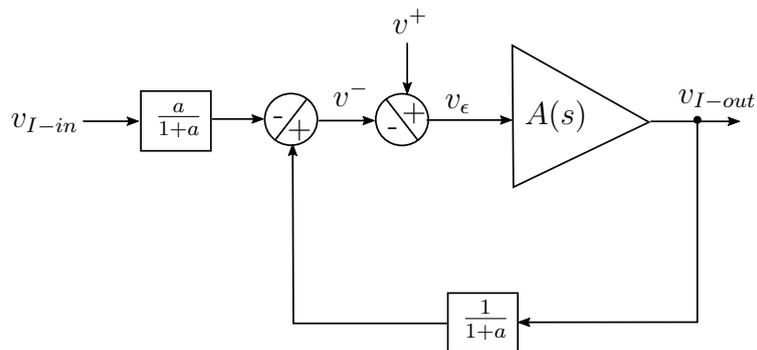


Figure C.2 : System level view of the integrator shown in Fig. C.1

The closed loop transfer function ($H(s)$) of this system assuming $v^+ = 0$ can be expressed by,

$$H(s) = \frac{a}{1+a} \cdot \frac{A(s)}{1 + \frac{1}{1+a} \cdot A(s)} \quad (\text{C.0.2})$$

If the amplifier is assumed of one pole structure, i.e. $A(s) = \frac{A}{1+s\tau}$, (C.0.2) can be rewritten as,

$$H(s) = \frac{a}{1+a} \cdot \frac{A}{1 + \frac{1}{1+a} \cdot A + s \cdot \tau} = \frac{\frac{a \cdot A}{1+a+A}}{1 + s \cdot \frac{\tau}{1 + \frac{A}{1+a}}} \equiv \frac{A_{int}}{1 + s \cdot \tau_{int}} \quad (\text{C.0.3})$$

where A_{int} and τ_{int} are the equivalent gain and time constant of the closed loop integrator. Since τ represents the cut-off frequency of the amplifier, it can be expressed in term of GBW as $\tau = A/GBW$, and accordingly $\tau_{int} = \frac{A/GBW}{1 + \frac{A}{1+a}}$.

Appendix D

VerilogA

D.1 OTA

```
// VerilogA for 2019_Ali_ADC, OTA veriloga
#include "discipline.h" include "constants.h"
// VerilogA for libCron, opamp, veriloga
#define PI 3.14159265
//-----
//- operational amplifier
// vin_p,vin_n: differential input voltage [V,A]
// vout: output voltage [V,A]
// vref: reference voltage [V,A]
// vsply_p: positive supply voltage [V,A]
// vsply_n: negative supply voltage [V,A]
//
// INSTANCE parameters
// gain = gain []
// freq_unitygain = unity gain frequency [Hz]
```

```
// rin = input resistance [Ohms]
// vin_offset = input offset voltage referred to negative [V]
// ibias = input current [A]
// iin_max = maximum current [A]
// slew_rate = slew rate [A/F]
// rout = output resistance [Ohms]
// vsoft = soft output limiting value [V]
//
module opamp_single(vout, vref, vin_p, vin_n, vsupply_p, vsupply_n);
input vref, vsupply_p, vsupply_n;
inout vout, vin_p, vin_n;
electrical vout, vref, vin_p, vin_n, vsupply_p, vsupply_n;
parameter real gain = xx;
parameter real freq_unitygain =xx;
parameter real rin = xx;
parameter real vin_offset = 0.0;
parameter real ibias = 0.0;
parameter real iin_max = xx;
parameter real slew_rate = xx;
parameter real rout = xx;
parameter real vsoft = xx;
real c1, gm_nom, r1, vmax_in, vin_val, ugf;
electrical cout;
// function to retrieve the GBW from the temperature
analog function real gbw;
```

```

input freq_unitygain;

real freq_unitygain, ans;

begin

//ans = -0.0956*pow($temperature-300, 4) + 17.042*pow($temperature-300, 3) - 3095.1*pow($tempe
300, 2) + 254250*($temperature-300) + 500e6; // TC Ibias 4500 ppm

//ans = -0.04*pow($temperature, 4) + 3.0107*pow($temperature, 3) - 544.76*pow($temperature,
2) - 117933*$temperature + 500e6; // TC Ibias 3500 ppm

gbw = ans * (freq_unitygain / 508e6);

end

endfunction

// function to retrieve the DC Gain from the temperature

analog function

real gdc, gain, ans;

input gain;

begin

ans = 0.012*pow($temperature-300, 2) -13.6*($temperature-300) + 2151.5; // TC Ibias
4500 ppm or 3500 ppm gdc = ans * (gain/1798.87);

end

endfunction

analog begin

@ ( initial_step or initial_step("dc") ) begin

ugf = gbw(freq_unitygain);

c1 = iin_max/(slew_rate);

gm_nom = 2 * 'PI * gbw(freq_unitygain) * c1;

r1 = gdc(gain)/gm_nom; vmax_in = iin_max/gm_nom;

end

vin_val = V(vin_p,vin_n) + vin_offset;

```

```
//  
// Input stage.  
I(vin_p, vin_n) <+ (V(vin_p, vin_n) + vin_offset)/ rin;  
I(vref, vin_p) <+ ibias; I(vref, vin_n) <+ ibias;  
//  
// GM stage with slewing  
I(vref, cout) <+ V(vref, cout)/100e6;  
if (vin_val > vmax_in) I(vref, cout) <+ iin_max;  
else if (vin_val < -vmax_in) I(vref, cout) <+ -iin_max;  
else I(vref, cout) <+ gm_nom*vin_val ;  
//  
// Dominant Pole.  
I(cout, vref) <+ ddt(c1*V(cout, vref));  
I(cout, vref) <+ V(cout, vref)/r1;  
//  
// Soft Output Limiting.  
if (V(vout) > (V(vsupply_p) - vsoft)) I(cout, vref) <+ gm_nom*(V(vout, vsupply_p)+vsoft);  
else if (V(vout) < (V(vsupply_n) + vsoft)) I(cout, vref) <+ gm_nom*(V(vout, vsupply_n)-  
vsoft);  
end  
endmodule
```

D.2 Comparator

```
// VerilogA for 2019_Ali_ADC, Comparator, veriloga  
‘include "disciplines.vams"
```

```

module quantizer_1bit (in_p, in_n,out_p,out_n, clk);
// input output out_p,out_n; voltage out_p,out_n;
input in_p, in_n, clk;
voltage in_p, in_n, clk;
// output
parameter real vh = 1.8;
// voltage of highest level
parameter real vl = 0;
// voltage of lowest level
parameter real vref=0.9 ;
// reference voltage
parameter real vth =0.005;
// threshold voltage of clock parameter
real td = 0 from [0:inf);
// output delay parameter
real tt = 0 from [0:inf);
// output transition time
real in;quantized;
analog begin
@(initial_step) begin
in=0; quantized=vl;
end
@(cross(V(clk) - vth, +1) ) begin
in=V(in_p)-V(in_n);
if(in>0) quantized=vh; else quantized=vl;

```

```
end
V(out) <+ transition( quantized, td, tt );
end
endmodule
```

D.3 Save data

```
// VerilogA for 2019_Ali_ADC, save, veriloga
`include "constants.vams" `include "disciplines.vams"
module save_S ( in_p, D, clock);
input D, in_p, clock;
electrical D, in_p, clock;
integer file ,r;
parameter print=0;
analog begin @(initial_step) begin
file=$fopen("./data.csv","w");
end
@(cross(V(clock)-1.1 , +1) ) begin
if((V(D)==0 || V(D)==1.8)) begin
$display(file,"%f",V(in_p));
$display(file,"%f",V(D));
$fflush(file);
if (print!=0) $display("valeur numerique:%f",V(D));
end
end
end
end
```

endmodule

Appendix E

Temperature aware MILO sustaining electronics

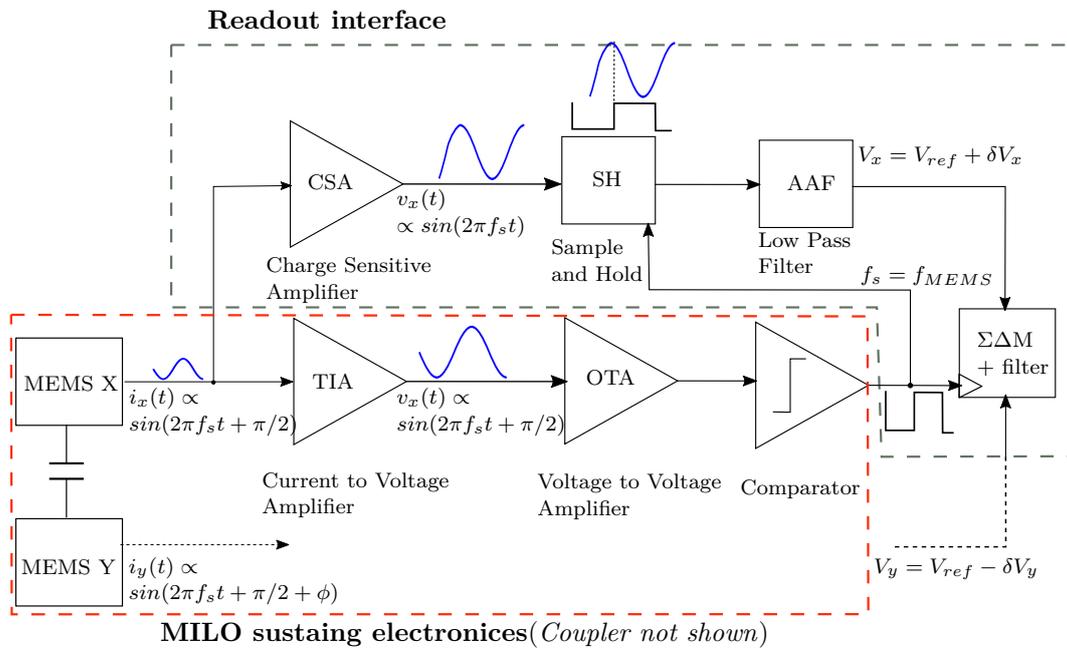


Figure E.1 : System-level view of MILO sustaining electronics and readout interface

E.1 Introduction

Thermal stability issues in resonant sensing applications should not be envisioned from the point of view of the mechanical structure only. Recent study considering the MILO architecture has highlighted that the thermal drift of the sustaining electronics is also one of the main issues limiting the performance of the sensor [14]. It may cause an error drift

of several order of magnitude beyond the resolution of the system. In fact, The main building blocks constituting the MILO loop and are responsible for its accuracy, are the preamplifier and the phase shifter, e.g. low-pass filter. The former must ensure a very accurate gain and linearity, and the later should provide the required phase shift for a given MILO operating point, e.g. $\pi/2$ in this work and $\pi/4$ in [14]. In the $\pi/4$ MILO architecture studied in [14], it has been shown that, using a preamplifier and a phase shifter based on the conventional Miller OTA structure, leading to a loop phase error of 8° when temperature up to 125°C . This variability entails a change in the MILO operating point, and hence degrading its performance. Considering the MILO architecture used for the ratiometric measurement shown in Fig. 1.5.3, the preamplifier and the $\pi/2$ phase shifter can be implemented with a single block using a current to voltage transimpedance amplifier (TIA). In fact, the sensing current delivered from the MEMS is an image of the motion velocity x' having a $\pi/2$ phase lead with respect to the amplitude motion x (assuming a sinusoidal signal). Thus, converting this current to a voltage with 0° phase shift meet the requirement of the MILO sustaining electronics as shown in Fig. E.1.

In the first part of this chapter, a temperature aware transimpedance amplifier is proposed and analysed. It deals with a signal frequency up to 1 MHz, while preserving a high thermal drift stability within the specified temperature range ($-40 \leq T[^\circ\text{C}] \leq 125$). The proposed circuit consists of two stages, the former is a current to voltage preamplifier having a conversion gain (I/V) of $80 \text{ dB}\Omega$, and the later is a post-amplification stage that enhance the gain of the first stage with a voltage to voltage gain (V/V) of 25 dB. The proposed I/V and V/V gain stages posses "separately" temperature coefficient ($TC = \frac{Gain^{max} - Gain^{min}}{\Delta T \cdot Gain^{nom}} \cdot 10^6$) of $92 \text{ ppm}/^\circ\text{C}$ and $66 \text{ ppm}/^\circ\text{C}$ respectively, and a TC of $268 \text{ ppm}/^\circ\text{C}$ when they are connected together. The circuit shows, a phase error of only 1° at the maximum operating frequency 1 MHz, an average input referred noise current of $3.75 \text{ pA}/\sqrt{\text{Hz}}$, and dissipates $445 \mu\text{W}$ form 1.8 V supply.

The second branch of the system shown in Fig.E.1, is the first part of the readout electronic performing the ratiometric acquisition. In fact, the Charge-Sensitive-Amplifier (CSA) integrates the sensing current and deliver a voltage proportional to the amplitude motion x . Thanks to the integration process, this voltage has a $-\pi/2$ phase shift with respect to the signal presenting in the MILO loop (proportional to the velocity). Thus, the demodulation phase can easily be performed using a sample and hold peak detector circuit that takes the comparator output as an input clock. In the second part of this chapter, a temperature aware amplifier that can be used in CSA stage is presented, and a possible implementation of he sample and hold peak detector circuit is developed. Due to the lack of time, the results presented in this chapter are based on transistor level simulations.

E.2 Current to voltage temperature aware amplifier

E.2.1 Design consideration

As discussed earlier the sensing current delivered from the MEMS is an image of the motion velocity x' having a $\pi/2$ phase lead with respect to the amplitude motion x . Thus, a Transimpedance-Amplifier (TIA) can be used to convert this current to a voltage with 0° phase shift. Meanwhile, the TIA must operate within the frequency range (specified in Chap. 2) from hundred kHz to 1 MHz, and supporting the parasitic capacitance resulting from the electrical contacts to the MEMS device (C_{p-MEMS}). This capacitance is in orders of magnitude of some pF, i.e. $C_{p-MEMS} < 10$ pF. Depending on the MEMS geometry, i.e. sensing capacitance (C_{sens}), and the operating condition, i.e. bias voltage (V_{bias}); the sensing current ($i_x(t) = V_{bias} \cdot \frac{\partial C_{sens}}{\partial t}$) is in order of magnitude of hundred nA to μA , thus a transimpedance gain of $80 \text{ dB}\Omega$ resulting in a voltage of the order of mV. A moderate gain around $80 \text{ dB}\Omega$ also relax the constraint related to the required bandwidth (-3 dB cut-off frequency f_c), which must be well larger than the highest input signal frequency 1 MHz (i.e. 10 times), to ensure a 0° phase shift at this point. Other Voltage to Voltage (V/V) gain stage can be post-interfaced with the TIA to enhance the gain if needed. This stage load the TIA by the gate to source parasitic capacitances (e.g. $C_{TIA-load} < 100$ fF) of its input transistors. The requirement of the TIA are listed in Table E.1.

Table E.1 : TIA requirement

I/V gain	$> 80 \text{ dB}$
Input signal frequency	$100 \text{ kHz} \leq f_s \leq 1 \text{ MHz}$
Phase-shift	0°
Bandwidth	$f_c > 10 \times 1 \text{ MHz}$
Temperature range	$-40 \leq T \leq 125 \text{ }^\circ\text{C}$
Low noise	some pA/\sqrt{Hz}
Input signal bandwidth	$BW \leq 2 \text{ kHz}$
C_{p-MEMS}	$\leq 10 \text{ pF}$
$C_{TIA-load}$	$\leq 0.1 \text{ pF}$

E.2.2 Proposed transimpedance amplifier and its operating principle

The proposed fully differential TIA that is temperature and supply voltage aware designed is depicted in Fig.E.1. It is a modified version of the regulated cascode common gate structure [81]. The idea behind making this architecture temperature and supply

insensitive is inspired from the bandgap voltage reference circuit [47]. In fact, the sensing current $i_x(t)$ goes through the common gate transistor M_1 and converted to a voltage by mean of the diode-connected load transistors M_{3a} and M_{3b} ($v_x(t) = i_x(t)/g_{m3}$). Since the bias current (I_1) is fixed all time by the current source transistor M_{0a} , and the potential at the output node is controlled by the CMFB circuit via the transistor M_{3b} to be $V_{cm} = 0.9V$, the resulting load impedance $R_{load} = 1/g_{m3}$ is also fixed all time and slightly change with PVT variations. Moreover, the common source amplifier constituted with M_2 and R_0 act as a local feedback loop with the input transistor M_1 , as a result, the input impedance ($R_{in} = 1/g_{m1}$) is divided by the loop gain ($g_{m2} \cdot R_0$). The main purpose of this configuration is to lower the input impedance by mean of the feedback feature rather than using a higher current I_1 or a larger device $(W/L)_1$. By having a low input impedance, the TIA isolates the MEMS parasitic capacitance, preventing it from achieving a higher bandwidth. This branch usually consume less power than the main branch, e.g. $I_2 = I_1/8$ in this work. It worth mentioning that a single to differential structure may be obtained by cross-coupling the input transistors M_1 and M_{01} as in [82]

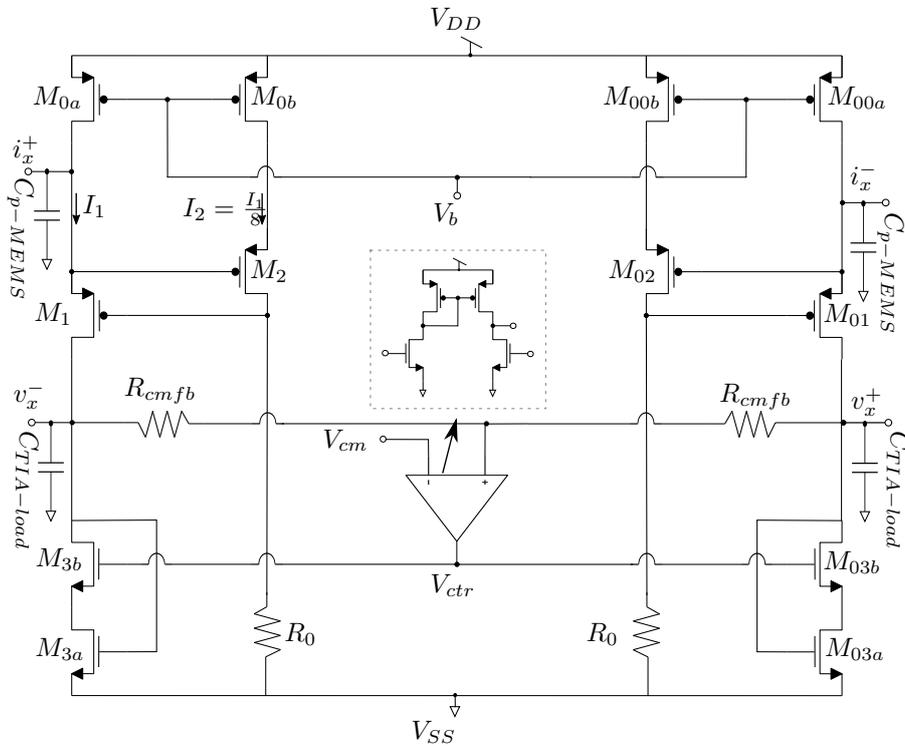


Figure E.1 : Transistor level of the proposed TIA

E.2.3 PVT simulation results

E.2.3.1 ac analysis

Figure E.2 shows the nominal bode diagram (Gain and Phase) of the proposed TIA for I_1 going from 10 to 100 μA , $C_{p-MEMS} = 10$ pF and $C_{p-load} = 0.1$ pF. It can be indicated that for $I_1 \geq 40$ μA the bandwidth f_c of the TIA is roughly 10 MHz, this value still not sufficient to ensure a near zero phase shift at 1 MHz. Thus a higher I_1 of 80 μA is selected, it provides an absolute phase shift of lower than 3° in the worst case condition ($C_{p-MEMS} = 10$ pF), and an I/V conversion gain of ≈ 80 dB Ω . Note that, when C_{p-MEMS} is low the bias current can be tuned (bias voltage V_b of M_{0a}) to trade between the gain the bandwidth of the TIA.

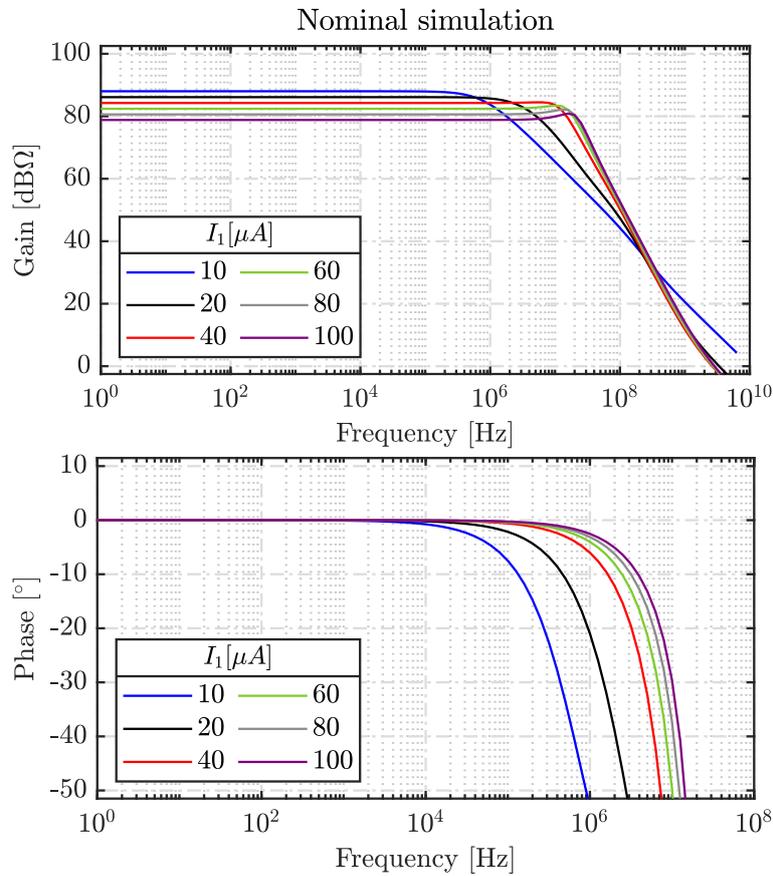


Figure E.2 : Nominal frequency response (Gain and Phase) of the TIA for I_1 going from 10 to 35 μA . $C_{p-MEMS} = 10$ pF and $C_{TIA-load} = 0.1$ pF

PVT simulation is analyzed for the TIA's gain and phase-shift at 1 MHz frequency, considering 8-points temperature going from -40 to 125 $^\circ C$, and 3 points supply voltage $V_{DD} = 1.8 \pm 10\%$ (Monte Carlo simulation is not carried out since the layout of the circuit is not yet realized). The results for $I_1 = 80 \mu A$, $C_{p-MEMS} = 10$ pF and $C_{p-load} = 0.1$ pF

are depicted in Fig. E.3. It can be clearly seen that the proposed TIA is highly immune to temperature and supply variations. The gain poses a maximum variation of less than 0.1 dBΩ within the temperature range and under any supply voltage conditions. For $V_{DD} = 1.8$ V, the gain Temperature-Coefficient of the circuit ($TC = \frac{Gain^{max} - Gain^{min}}{\Delta T \cdot Gain^{nom}} \cdot 10^6$) is approximately 92 ppm/°C. The highest and the lowest gain are 80.27 dB for ($V_{DD} = 1.62, T = -40^\circ C$) and 80.05 for ($V_{DD} = 1.98, T = 32^\circ C$) respectively. However, the TIA phase shift drops slightly for $V_{DD} = 1.62$ V compared with higher supply voltages (due to a drop in f_c not presented here), the maximum phase shift is observed at $T = 125^\circ C$ and it is approximately -6.2° . For $V_{DD} \geq 1.8$ V, the phase shift has only 1° variation within the temperature range.

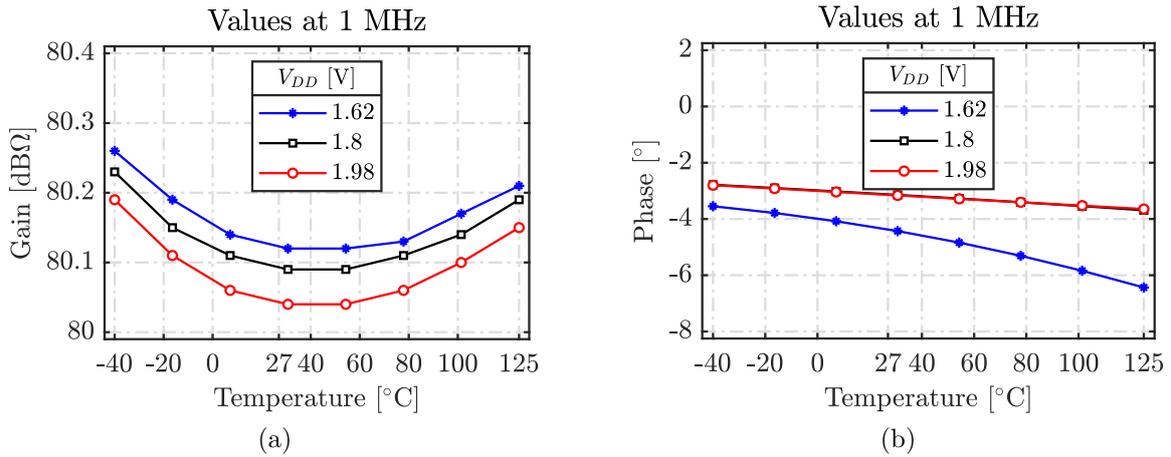


Figure E.3 : PVT simulation results of the TIA, (a) gain, and (b) phase, considering 8-points temperature going from -40 to $125^\circ C$, and 3 points supply voltage $V_{DD} = 1.8 \pm 10\%$ $I_1 = 80 \mu A$. $C_{p-MEMS} = 10$ pF and $C_{TIA-load} = 0.1$ pF

E.2.3.2 Input impedance

An other interesting property of the proposed structure is that the input/output impedance are decoupled so that they can be tuned separately for an optimal operation (for a given C_{p-MEMS}). In fact, the input impedance is expressed by,

$$Z_{in} = Z_{C_{p-MEMS}} || R_{in} \equiv \frac{1}{j\omega C_{p-MEMS}} || \frac{1/g_{m1}}{1 + g_{m2} \cdot R_0}. \quad (E.2.1)$$

From (E.2.1) the three dependant parameters of Z_{in} (g_{m1} , g_{m2} and R_0) are independent of the transimpedance gain as opposed to the ordinary resistive feedback TIA. Depending on C_{p-MEMS} , R_0 can be increased to make the Z_{in} cut-off frequency well larger than the maximum operating frequency (1 MHz). This ensure that the total sensing current power is delivered to the TIA with zero phase rotation. However, increasing R_0 leads to an increase in the input referred noise current, since R_{in} will be lowered accordingly. Figure E.4(a) shows the frequency response of the Z_{in} for different value of R_0 considering a

C_{p-MEMS} of 10 pF. It can be indicated that for $R_0 \leq 25k\Omega$ the cut-off frequency of Z_{in} exceed the maximum operating frequency 1 MHz, meaning that at least half of i_{sens} is lost and goes to ground through C_{p-MEMS} . Thus, a resistance of larger than 40 k Ω was selected for R_0 , it actually set to 50 k Ω . At this value the average input referred noise current (noise floor) within the frequency bandwidth (100 kHz $< f_s < 1$ MHz) is shown in Fig. E.4(b), considering voltage and temperature variation. It can be indicated that the nominal noise floor of the input referred current noise is hardly 3.75 pA/ \sqrt{Hz} , while the maximum value is observed at 125°C and $V_{DD} = 1.98$ V and it is 3.9 pA/ \sqrt{Hz} .

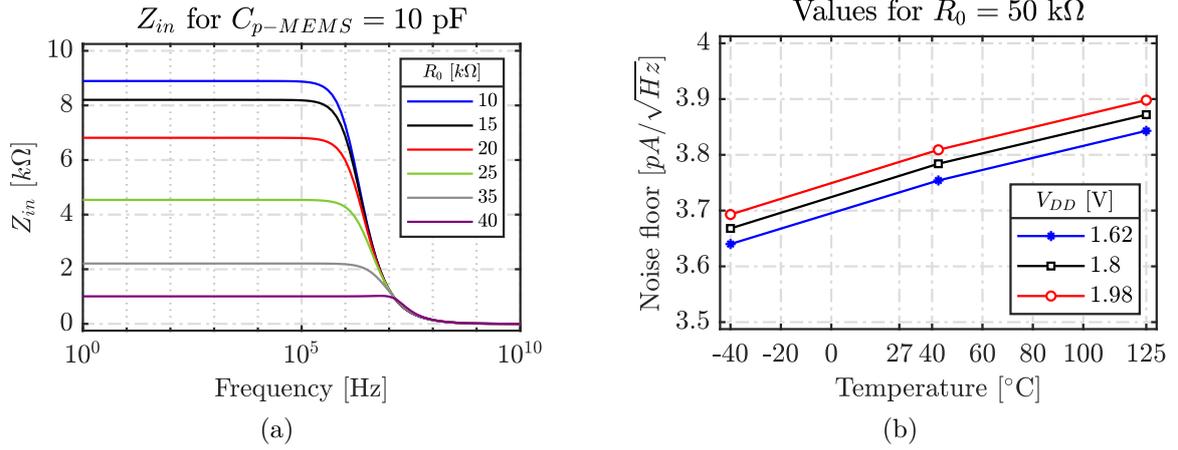


Figure E.4 : (a) Nominal frequency response of the TIA Z_{in} for different values of R_0 , and (b) noise floor of the input referred current for $R_0 = 50$ k Ω . The simulation is carried out for $I_1 = 80$ μ A, $C_{p-MEMS} = 10$ pF and $C_{p-load} = 0.1$ pF

E.2.3.3 Linearity

In Fig. E.5 the output swing of the proposed TIA is analysed for $i_x(t)$ (differential) going from 50 nA to 20 μ A and 1 MHz frequency, considering nominal condition (in black dashed line), $V_{DD} = 1.98$, $T = 125^\circ C$ (in red full line) and $V_{DD} = 1.62$, $T = -40^\circ C$ (in blue dotted line). Since the TIA gain does not deviate much from its nominal value when temperature changes (see Fig. E.3), the $v_x(t)$ peak values V_x observed in the black dashed and the blue dotted lines are almost the same and having a THD of -42.5 dB for $I_x = 20\mu A$. However, due to the lower voltage headroom at $V_{DD} = 1.62V$ (red full line), the TIA linearity is slightly degraded especially for $I_x > 10$ μ A. In this operating conditions the THD is approximately -30 dB at 1 MHz and $I_x = 20\mu A$. The specifications of the proposed TIA are summarized in Table E.2.

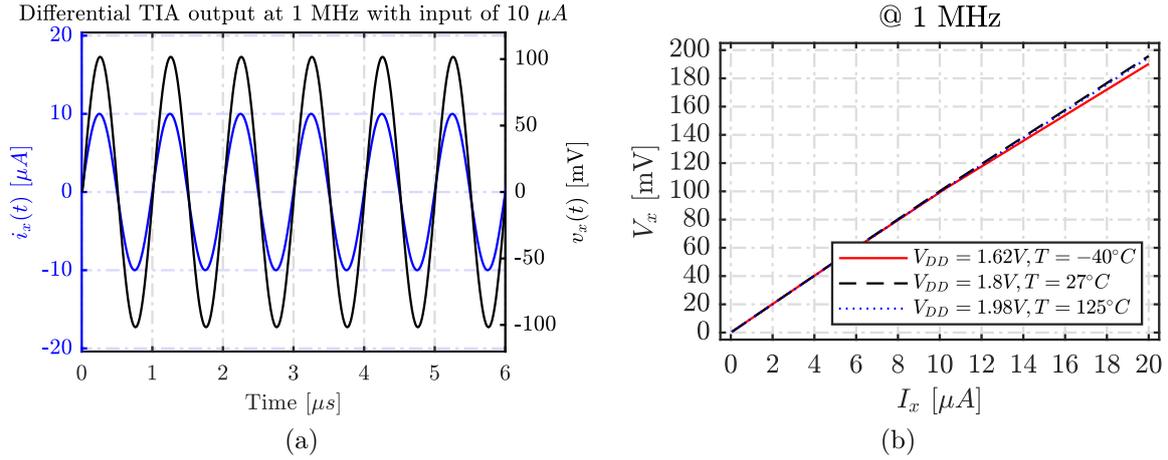


Figure E.5 : TIA nominal output voltage at 1 MHz frequency, (a) time domain for $i_x(t)$ (differential) of $10 \mu A$, and (b) peak value V_x for I_x (differential) going from $50 nA$ to $20 \mu A$, considering nominal (black dashed line), best case conditions (blue dotted line) and worst case conditions (red full line). $R_0 = 50 k\Omega$, $I_1 = 80 \mu A$, $C_{p-MEMS} = 10 pF$ and $C_{TIA-load} = 0.1 pF$

Table E.2 : TIA specifications for $C_{p-MEMS} = 10 pF$ and $C_{p-load} = 0.1 pF$

Specs	Nominal values	Worst values
I/V gain	$\approx 80.1 dB\Omega$	$\approx 80.04 dB\Omega$
TC Gain	$92 ppm/^{\circ}C$	$99.4 ppm/^{\circ}C$
Input signal frequency	$100 kHz < f_s < 1 MHz$	
Phase-shift @ 1 MHz	$\approx -2.5^{\circ}$	$\approx -6.2^{\circ}$
Bandwidth f_c	$20 MHz$	$10 MHz$
Average noise	$3.75 pA/\sqrt{Hz}$	$3.9 pA/\sqrt{Hz}$
THD @1 MHz and $20 \mu A$	$-42.5 dB$	$-30 dB$
Power consumption	$343 \mu W$	$389 \mu W$

E.2.4 Discussion

The proposed TIA design features of relatively low power consumption, high linearity, and high immunity to temperature and supply variation, are at the cost of a moderate conversion I/V gain. This gain is defined by the output voltage value V_{cm} and the biasing current I_1 . The former (V_{cm}) is usually set at the mid-range of the supply voltages, i.e. $V_{cm} = 0.9 V$ (for improved linearity), while the later (I_1) is determined according to the required bandwidth. However, for a given MEMS structure, and depending on the dynamic range of I_x , one may need an I/V conversion gain higher than $80 dB\Omega$. Thus,

a post-amplification V/V stage can be interfaced with the proposed TIA to enhance the gain. Indeed, this stage must also be temperature aware designed and having a near zero phase shift at 1 MHz. Thus, a drift-free V/V gain stage is proposed to mitigate, in some cases, the gain limitation of the TIA. This stage is presented and analysed in the following section.

E.3 Voltage to voltage temperature aware amplifier

The proposed circuit is based on well known Diode-connected-load OTA (DOTA), as the one illustrated in Fig. E.1(c) [83]. This structure is widely used in the analog controlled gain amplifier (VGA) [84]. This application mainly focus on the VGA bandwidth, linearity, and gain adjustment accuracy with respect to process and supply variations. They usually use the DOTA as a unit cell stage with relatively low gain, typically $< 5dB$. However, considering the present application, this architecture must be designed with relatively larger gain (> 20 dB) and high thermal stability. In this section, the operating principle of the DOTA is first analyzed. Then, the optimization methodology to achieve a high gain and low drift effect are discussed. Gain reliability is evaluated considering transistor's secondary effect (including: channel-length modulation, mobility and bulk effect), sizes and biasing condition. Next, the performance of the optimized diode connected load amplifier is compared (based on simulation results) with the ordinary active load amplifier, to highlight the efficiency of the proposed gain stage against the reference architecture. Finally, design bottleneck and trade-off are identified and discussed.

E.3.1 Operating principle

Neglecting short channel length effects and body effect, the g_m of an NMOS transistor in strong inversion region, is classically given by:

$$g_m(T) \approx \sqrt{2\mu_n(T)C_{ox} \frac{W}{L} I_d(T)}. \quad (\text{E.3.1})$$

A fixed voltage gain amplifier can be performed using the circuit illustrated in Fig. 1(a). It consists of a common source stage with diode-connected load amplifier (DOTA). The small signal gain magnitude of this stage can be expressed in function of the device dimension factor ($\eta = (W/L)_2/(W/L)_1 < 1$) as,

$$G_\eta(T) = \frac{g_{m_1}(T)}{g_{m_2}(T)} = \sqrt{\frac{2\mu_{n_1}(T)C_{ox}(\frac{W}{L})_1 I_1(T)}{2\mu_{n_2}(T)C_{ox}(\frac{W}{L})_2 I_1(T)}} \approx \sqrt{\frac{1}{\eta}}, \quad (\text{E.3.2})$$

which in first approximation ($\mu_{n_1} \approx \mu_{n_2}$) is independent temperature variations, since the remaining terms depend only on a geometric relationship. Indeed, the diode-connected

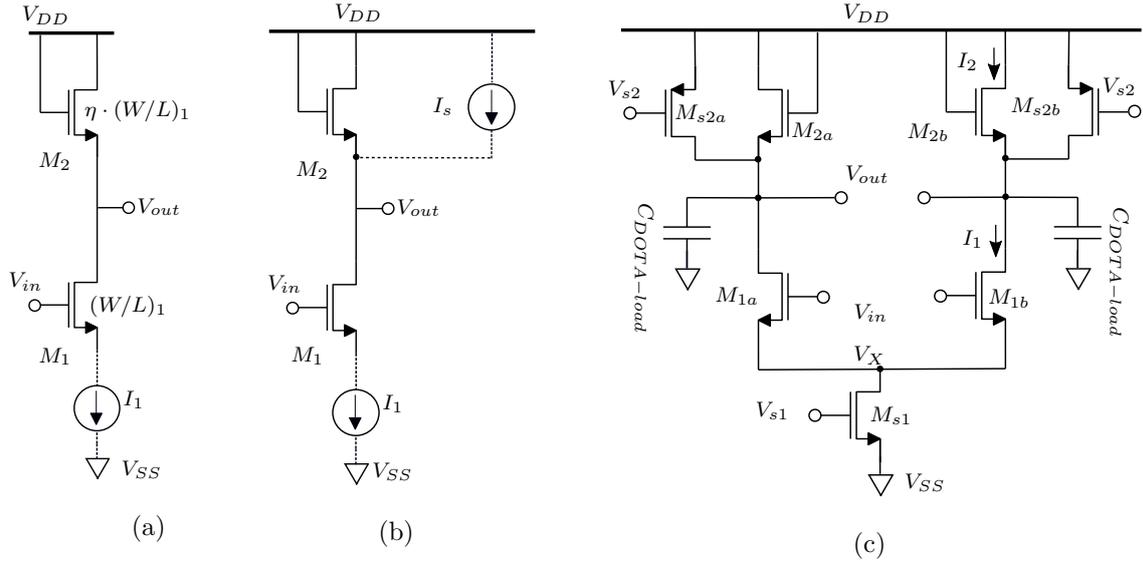


Figure E.1 : Common source amplifier with diode-connected-load (DOTA), (a) ordinary, (b) modified DOTA with ideal current source, (c) DOTA fully differential implementation of (b) with MOS current sources

load can be implemented with a PMOS device as well. For a good choice, one seeks to analyze their gain drift considering transistors' secondary effects, including mobility and body effect. The small signal gain magnitude for both configurations can be rewritten as:

$$G_{\eta}^{(N,P)}(T) = G_{\eta} \cdot \alpha_G^{(N,P)}(T), \quad (\text{E.3.3})$$

where $\alpha_G^{(N,P)}$ represents the temperature-dependent mismatch between the input transistor and PMOS or NMOS load transistor. It is given by:

$$\alpha_G^N(T) = \sqrt{\frac{\mu_{n1}(T)}{\mu_{n2}(T)}} \cdot \frac{1}{1 + \frac{g_{mb2}(T)}{g_{m2}(T)}}, \quad (\text{E.3.4a})$$

$$\alpha_G^P(T) = \sqrt{\frac{\mu_{n1}(T)}{\delta \mu_{p2}(T)}}, \quad (\text{E.3.4b})$$

where $\delta = (\mu_n/\mu_p)|_{T_0}$, for simplicity, both α_G^N and α_G^P have been directly compared and analyzed based on simulation, and the results are given in Fig. E.2. It can be indicated that using PMOS load to eliminate the body effect is not an optimal choice when temperature variation is considered. It results in a gain loss of more than 15% at the maximum absolute temperature $T = 125$ °C. Thus, it is recommended to implement both the input and the load transistors with the same type. Note that to achieve a high

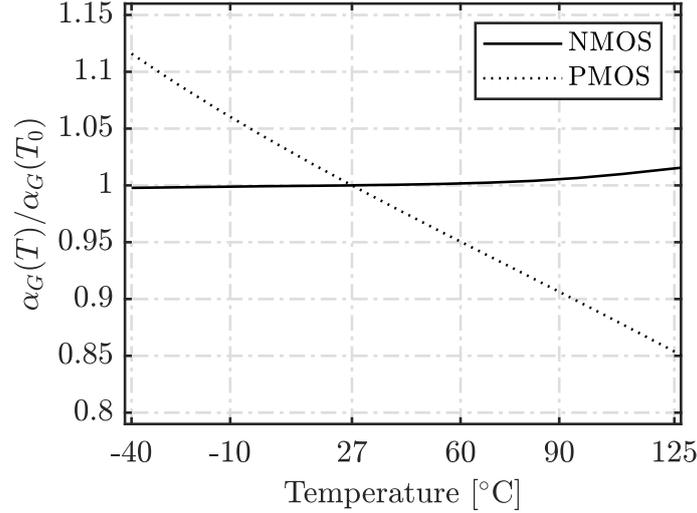


Figure E.2 : Normalized temperature-dependent factor $\alpha_G^{(N,P)}$ obtained from simulation for: NMOS (full-line) and PMOS (dotted-line)

gain, the aspect ratio (W/L) of the M_2 must decrease, thereby increasing its over-drive voltage ($V_{ov} = V_{GS} - V_{th}$) and lowering the bias voltage of the input transistor (V_{cm}). To alleviate this constraint, a fraction of I_1 can be provided by the current source (I_s) as shown in Fig. E.1(b). The idea is to lower g_{m_2} of the load device by reducing its current rather than its aspect ratio. Neglecting α_G^N , the absolute gain for the circuit shown in Fig. E.1(b) can be expressed by,

$$G_\eta \approx \sqrt{\frac{I_1}{I_2} \cdot \frac{1}{\eta}}. \quad (\text{E.3.5})$$

Thus, for a gain of 10, the aspect ratio of M_1 need to be only 10 times that of the M_2 , instead of 100 compared with the circuit of Fig. E.1(a). In fact, For a given overdrive voltage, if the $(W/L)_2$ decreases by a factor of 10, then I_2 must decrease proportionally, and g_{m_2} will be ideally lowered by the same factor. In addition, being the current ratio $I_2/I_1 = \eta$, imply that the transistor M_1 and M_2 operate under the same condition (g_m/I_d) for negligible temperature coefficient.

Figure E.1(c) shows the fully differential implementation of the single stage DOTA shown in Fig. E.1(b) with current-source transistors denoted by M_{s1} and $M_{s2(a,b)}$. M_{s1} is the current source providing the current bias condition. Note that, to relax the output swing upper limit of the DOTA, M_{s2} must be a PMOS device. For fair analysis, the channel length effects was also included considering a finite g_{ds} in following discussions. In fact, the DC-gain in conventional OTAs is directly set by the transconductance g_{ds} , while in the present architecture the gain should ideally be independent of g_{ds} , and its effect must be suppressed for optimum operation. The overall differential voltage gain of the DOTA (Fig. E.1(c)) is expressed by,

$$G_{apx}(T) = \frac{G_\eta(T)}{1 + \frac{G_\eta(T)}{g_{m1}(T)} \{g_{ds1} + g_{ds2} + g_{ds2}\}(T)} = \frac{G_\eta(T)}{1 + \chi_{L\eta}(T)}, \quad (\text{E.3.6})$$

where G_η is the enhanced gain introduced in (E.3.5), and $\chi_{L\eta}$ is a non-ideality factor considering finite g_{ds} . It can be indicated that the overall gain drift can be minimized by lowering $\chi_{L\eta}$ using long-channel devices and a higher η (i.e. $G_\eta \propto 1/\eta$). However, these will imply in larger parasitic capacitance and lower DC-gain. To minimize temperature induced current source variation, the transistors M_{s1} and $M_{s2(a,b)}$ are biased to work in strong inversion region with g_m/I_d around $4 \sim 5$ (as discussed in Chap. 3).

The current variation generated by the input pair transistors $M_{1(a,b)}$ must be claimed by the load transistors $M_{2(a,b)}$ without affecting the gain G_η . This can be ensured by making both, the input pair and the output load devices operate under the same biasing condition, regardless of whether the transistors possess a ZTC current or not. Since the active load devices $M_{2(a,b)}$ always operate in saturation region, $M_{1(a,b)}$ must also operate in this region.

Note that, the biasing condition of the diode connected transistors $M_{2(a,b)}$ is directly set by the output common mode voltage V_{oc} of the DOTA. In turn, V_{oc} depends on the input gate voltage V_{cm} , since under given current source and aspect ratio of $M_{1(a,b)}$, any increase in V_{cm} will be followed by a decrease in V_{oc} to maintain (V_{GS1}) . The condition of the input common mode voltage can then be written as $V_{cm} = (V_{DD} + V_X)/2$. In addition, ensuring that the transistors M_{s1} and M_{s2} operate in strong inversion region, yielding to $V_{ovs1} < V_X < V_{DD} - 2|V_{ovs2}|$. As a result, for an accurate $G_\eta(T)$ within the temperature range, V_{cm} must theoretically respect this inequality,

$$\frac{V_{DD} + V_{ovs1}}{2} < V_{cm} < V_{DD} - |V_{ovs2}|. \quad (\text{E.3.7})$$

By carefully selecting the size and the biasing of the devices, the overall performance of the DOTA can be optimized. The optimization procedure is discussed and validated with simulation results the following section.

E.3.2 Optimization methodology

Firstly, a selection of an appropriate V_{cm} is made considering voltage dynamic range and G_η accuracy. Secondly, the L is chosen to minimize area, and $\chi_{L\eta}$ error drift. Finally, given the required gain and accuracy, η can be selected. For design simplicity, the transistor channel length L is chosen to be the same for all transistors except for $M_{2(a,b)}$ which fixed to $8 \mu m$ to achieve $\eta \geq 0.03$. Note that, the circuit is only optimized with respect to temperature variation. Thus, only nominal simulation are presented ($V_{DD} = 1.8V$, and typical process model). The temperature-induced drift error on the gain is expressed here as $\xi_G = (G(T_{max}) - G(T_0))/G(T_0)$, where ξ_G is a value that indicates how much the gain

will change for the maximum temperature increase ($T_{max} = 125^\circ\text{C}$) relative to its nominal value at room temperature ($T_0 = 27^\circ\text{C}$).

E.3.2.1 Input differential-pair biasing condition

The circuit was first studied using long channel devices ($L = 2\mu\text{m}$) so that the error drift induced by $\chi_{L\eta}$ is highly minimized, hence $\xi_G \approx \xi_{G\eta}$. The biasing current I_1 is fixed to $25\mu\text{A}$. Aspect-ratio of the M_{s1} and $M_{s2(a,b)}$ have been obtained by imposing the same $g_m/I_d \approx 4 \sim 5$ for high current thermal stability.

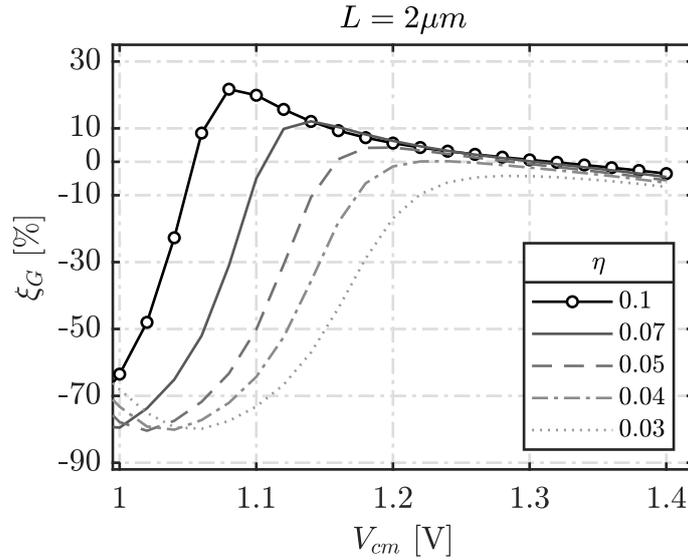


Figure E.3 : Relative temperature-induced gain variation ξ_G against the input common mode voltage for different device dimension factor η . Circuit of Fig. E.1(c) with $I_1 = 25\mu\text{A}$ and $L = 2\mu\text{m}$

The DOTA is simulated for V_{cm} varying from 1 to 1.4 V, and analyzed for different η ratio. The simulated temperature-induced gain variation ξ_G is shown in Fig. E.3. It can be observed that, for $1.2\text{V} \leq V_{cm} \leq 1.4\text{V}$ the ξ_G do not exceed $\pm 5\%$ when $\eta \geq 0.04$, and it's relatively stable along η range (small variations due to $\chi_{L\eta}$). This behavioral was expected since these values of V_{cm} fall within the range of (E.3.7). For instance, setting V_{cm} at 1.2V leads to $V_{DS_{s1}} \approx V_{DS_{s2}} \approx 0.6\text{V}$. Under these voltages we can assume that M_{s1} and $M_{s2(a,b)}$ stay in the saturation region and the overall gain drift still less than 3% within the temperature range. Also at this biasing condition the output common mode (V_{oc}) is roughly equal to V_{cm} (with little variation when temperature changes). This feature make possible the use of the DOTA with feed back configuration, or cascading 2 DOTA stages in a way that the output of the first stage being the input bias of the second stage. It worth mentioning that, a low value of V_{cm} (respectively V_X), would drive the transistor M_{s1} out from saturation region, making ξ_G more dependent on I_s as can be observed in Fig. E.3. Lower V_{cm} also leads to a decrease in I_s , and hence in the gain $\propto \frac{I_s/2}{I_2}$.

E.3.2.2 Chanel length effect

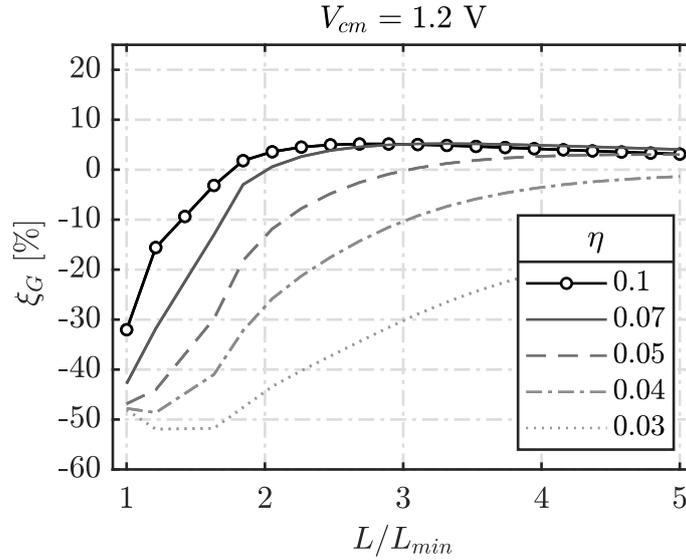


Figure E.4 : Relative temperature-induced gain variation ξ_G against transistor's channel length L , for different device dimension factor η . Circuit of Fig. E.1(c) with $I_1 = 25\mu A$ and $V_{cm} = 1.2V$

According to the temperature analysis of g_{ds} detailed in Chap. 3, for $g_m/I_d < 10$, g_{ds} has a negative TC. Thus by considering a short channel device, and neglecting the variation of G_η (i.e. 3%) and g_{m2} (since g_{m2} is very small), ξ_G ensues in a negative TC. This analysis is confirmed with simulation for different channel length from L_{min} to $5L_{min}$, the results are depicted in Fig. E.4. It can be indicated that when η and L are small, the gain shows a negative variation up to 50%. By increasing these parameters, the effect of $\chi_{L\eta}$ becomes negligible, and the total variation is limited by G_η (3%). For $L \geq 4L_{min}$ the maximum variation is bounded to $\pm 4\%$ for any $\eta > 0.04$. Assuming, $\eta \ll 1$ and $L_2 \gg L_{min}$ the non-ideality factor (for simplicity the channel length modulation effect is only considered) can be simplified to

$$\chi_{L\eta}(T) \approx \left(\frac{\lambda_n L_{min} + \lambda_p L_{min}}{L} \cdot \frac{G_\eta}{g_{m1}/I_1} \right) (T), \quad (E.3.8)$$

where $\lambda_{n,p}$ is the channel-length modulation coefficient of M_1 and M_{2s} . At room temperature, $\lambda_n L_{min}$ and $\lambda_p L_{min}$ are: $\approx 0.0054 \mu m/V$ and $\approx 0.023 \mu m/V$ respectively. Figure E.5 illustrates the simulated gain (G in blue dotted line) and the approximated gain (G_{apx} in blue full line) at room temperature using (E.3.5) and (E.3.8), for $V_{cm} = 1.2V$ and $L = 4L_{min}$. It should be pointed out that $\chi_{L\eta}$ is also represent the relative error between G_η and G_{apx} . Since G_{apx} evinces a good fitting with G at room temperature ($G_{apx}(T_0) \approx G(T_0)$), $\chi_{L\eta}$ can be extracted from simulation as,

$$\chi_{L\eta}(T_0) = 1 - \frac{G_{apx}(T_0)}{G_\eta} \approx 1 - \frac{G}{G_\eta}(T_0) \quad (E.3.9)$$

In Fig. E.5, $\chi_{L\eta}$ is plotted (in black dotted line) together with the simulated ξ_G (in black full line), as a function of the device dimensions factor η . It can be indicated that, when $\chi_{L\eta}$ decreases the gain becomes less sensitive to the temperature, until they turn into a stable region ($\eta > 0.05$). This behavior confirms that, when η is low, the temperature effect arises essentially from $\chi_{L\eta}$. Setting η at 0.05 offers a good trade-off between G (≈ 25 dB) and ξ_G (< 3).

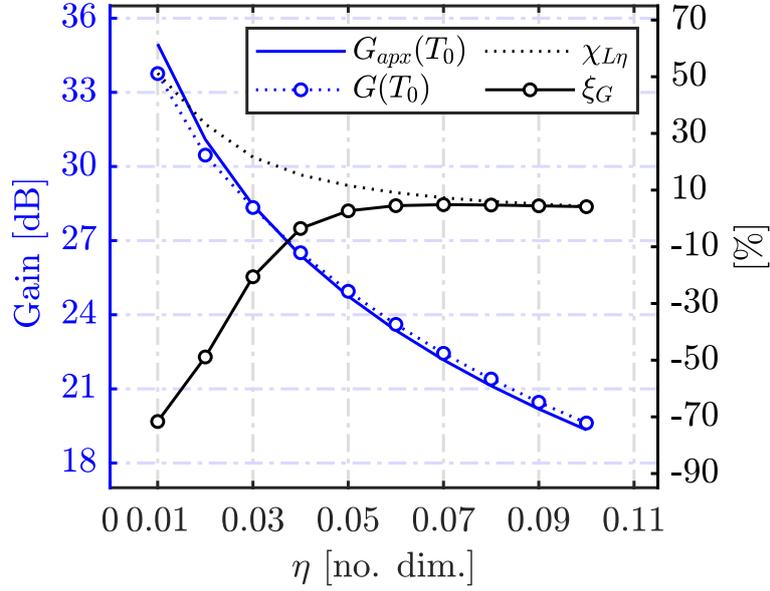


Figure E.5 : Simulated and approximated gain at room temperature 27 °C (left), simulated relative error $\chi_{L\eta}$ and temperature-induced gain variation ξ_G (right) in %. $V_{cm} = 1.2V$, $I_1 = 25\mu A$ and $L = 4L_{min}$

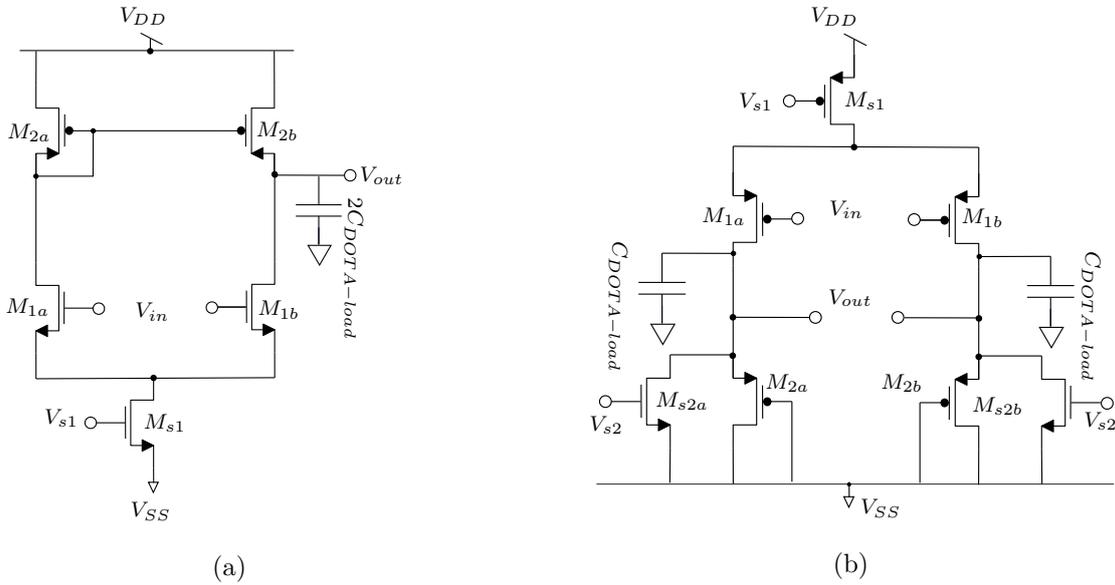


Figure E.6 : Schematic of, (a) ordinary single ended with active load amplifier (AOTA), (b) complementary implementation of the DOTA shown in Fig.E.1(c)

E.3.2.3 Comparison of the proposed amplifier with the ordinary active load amplifier

To demonstrate the gain reliability of the DOTA, a classical Active-load OTA (AOTA) is implemented (single ended) under the same technology as shown in Fig.E.6(a). $M_{2(a,b)}$ and $M_{s2(a,b)}$ are replaced by 2 PMOS-transistors having an aspect ration of δ times the transistors $M_{1(a,b)}$ and biased via V_{s2} . Fig. E.7 compares the gain reliability of the DOTA (in blue full line) against the AOTA (in black dotted line), considering typical process model and $V_{DD} = 1.8V$. The gain is normalized to the value at room temperature $G(T_0)$. For a temperature variation from -40 to 125 °C, the optimized linear gain of the proposed circuit presents a variation below 1%, while the gain of the reference design varies of 30%. Thus the proposed technique shows a $30\times$ improvement in-terms of the maximum percentage deviation as compared to the conventional scheme for the same set of conditions. The gain temperature coefficient ($TC = \frac{Gain^{max}-Gain^{min}}{\Delta T \cdot Gain^{nom}} \cdot 10^6$) of the DOTA is ≈ 60 ppm/°C, while it is around 1663 ppm/°C for the AOTA. For fair comparison, it worth point out that the AOTA could also be temperature aware designed by considering a near ZTC for g_{m1} and $g_{ds1(2)}$, as discussed in Chap. 3. However, as mentioned in [21], in such amplifier, the biasing conditions, and the choice of L for drift-free gain, leading to a very low gain (i.e. < 10 dB), compared to the proposed architecture (> 25 dB).

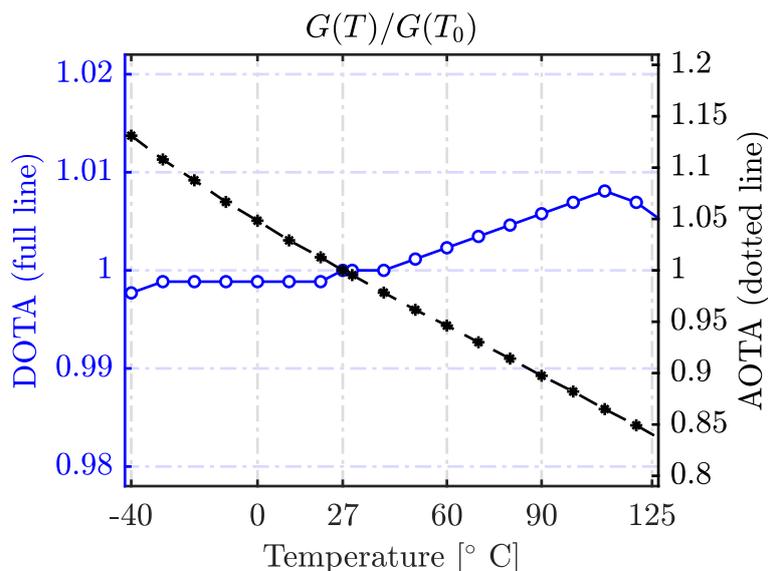


Figure E.7 : Normalized gain ($G(T)/G(T_0)$) of the DOTA (blue full line right) and the AOTA (black dashed line left), considering nominal simulation with typical process model and $V_{DD} = 1.8$ V

E.3.3 Discussion

It worth mentioning that the proposed DOTA posses -3 dB cut-off frequency of 11 MHz when loaded by a capacitance ($C_{DOTA-load}$) of 0.1 pF, and 5° phase shift at 1 MHz. It is

also important to note that the diode-connected load can be considered as a passive load, i.e. resistance. So that, it's easy to define the output common mode level as opposed to the conventional AOTA structure. This relax the need of an additional common mode feedback circuit CMFB in the design. The main limitation of the proposed structure is that it can not be used as a single ended structure, and with the input pair devices being operating in saturation region leads to a relatively higher input noise. Nevertheless, if the DOTA is used as a post-amplification stage the noise at this level can be neglected compared with the pre-amplification stage, i.e. the TIA. However, the V_{cm} of the TIA is specified at 0.9 V, which is different from the input biasing voltage of the DOTA $V_{cm} = 1.2$ V. As a solution, the DOTA can be decoupled from the output of the TIA using decoupling capacitor, and biased separately under the appropriate voltage value ($V_{cm} = 1.2$ V). Forcing the V_{cm} of the TIA to be 1.2 V, or using a level shifter stage can also overcome this issue. However, it has been found that by implementing the DOTA with PMOS devices instead of NMOS devices (complementary implementation) as shown in Fig.E.6(b), the circuit can properly operate with V_{cm} near 0.9 V. This structure is detailed in the following section.

E.3.4 Complementary implementation of the proposed temperature aware amplifier

The proposed "drift-free" diode-connected-load amplifier DOTA, can be as well implemented using PMOS devices (see Fig.E.6(b)). For a given design considerations (I_1 , G and ξ_G), the same optimization methodology can be applied to determine the appropriate design space (η , V_{cm} and L).

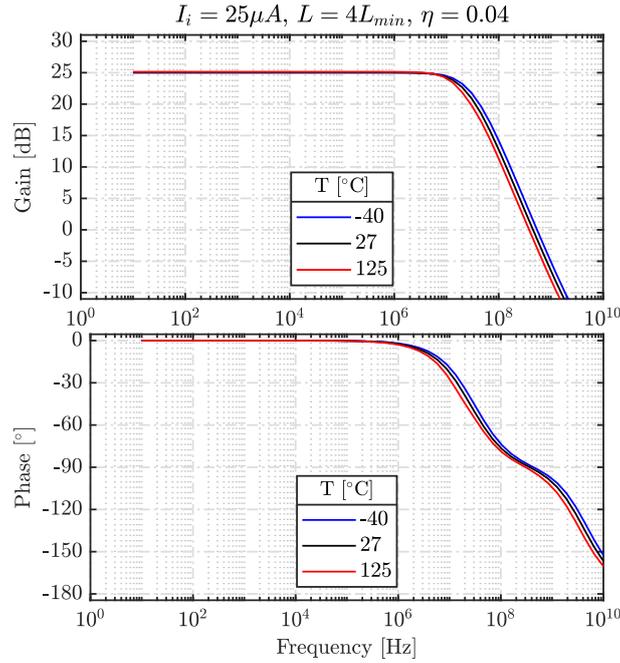


Figure E.8 : Nominal frequency response (Gain and Phase) of the complementary DOTA considering $I_1 = 25 \mu A$, $\eta = 0.04$, $V_{cm} = 0.9V$, $L = 4L_{min}$ and $C_{DOTA-load} = 0.1 \text{ pF}$

From simulation results it has been found that, for a $I_1 = 25 \mu A$, $G > 25 \text{ dB}$ and $\xi_G < 1\%$ the optimum design space values are $\eta \approx 0.04$, $V_{cm} = 0.9V$ and $L = 4L_{min}$ respectively. The bode diagrams of the complementary DOTA at -40 , 27 and $125 \text{ }^\circ\text{C}$ are given in Fig. E.8. The circuit possesses a TC gain of $66 \text{ ppm}/^\circ\text{C}$, and an absolute phase shift of less than 4.5° at 1 MHz . At room temperature the bandwidth of the circuit is roughly 17 MHz .

In Fig. E.9(b) the output swing of the proposed TIA is analysed for V_{in} (differential) going from 100 mV to 600 mV at 1 MHz frequency, considering three temperature, $T = 27^\circ\text{C}$ in (black dashed line), $T = 125^\circ\text{C}$ (in red full line) and $T = -40^\circ\text{C}$ (in blue dotted line). The results are carried out using the DOTA in a unity feed back configuration (not shown), and using typical process model with $V_{DD} = 1.8V$. As can be seen from Fig. E.9(b), there is almost no linearity distortion between 27 and $-40 \text{ }^\circ\text{C}$, with a THD (at 1 MHz and at input signal of 0.6 V) of -51 dB and -67 dB respectively. However, at $125 \text{ }^\circ\text{C}$, a small linearity distortion can be noticed (dotted blue line), the THD at this temperature drops to -48 dB from -51 dB at room temperature. It worth mentioning that the output voltage is slightly lower than the input voltage (the gain must be 1 in a unity feedback configuration), this is due to the finite gain of the DOTA that causes an attenuation of ($1/G \approx 0.057$). The specifications of the proposed complementary DOTA are listed in Table. E.3 at the three studied temperature values: -40 , 27 , and $125 \text{ }^\circ\text{C}$.

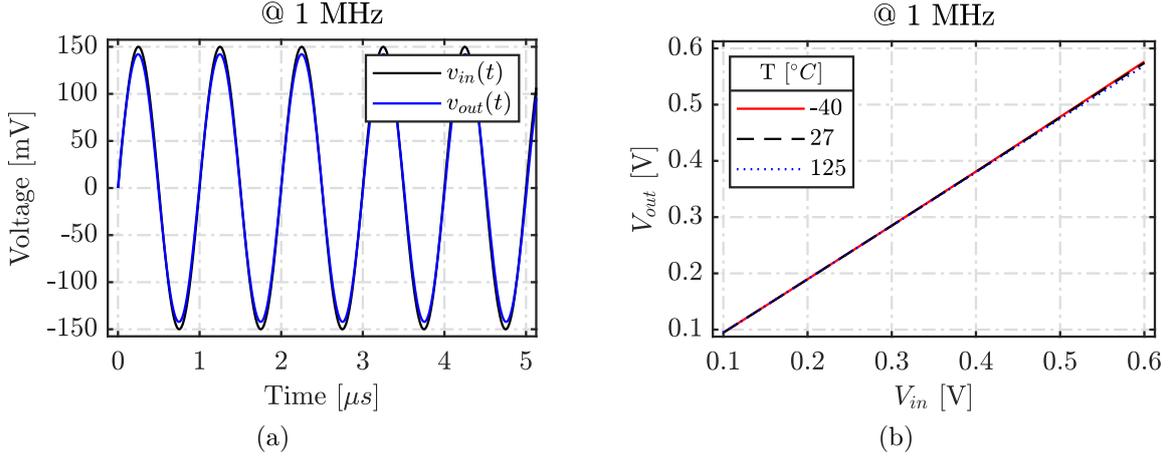


Figure E.9 : DOTA output voltage $v_{out}(t)$, (a) time domain for $v_{in}(t)$ (differential) of 0.15V at 1 MHz, and (b) peak values V_{out} for $v_{in}(t)$ (differential) going from 100 mV to 600 mV at 1 MHz, considering $T = 27^\circ\text{C}$ in black line, $T = 125^\circ\text{C}$ in red line and $T = -40^\circ\text{C}$ in blue line. $V_{DD} = 1.8\text{V}$, $I_1 = 25\ \mu\text{A}$ and $C_{DOTA-load} = 0.1\ \text{pF}$

Table E.3 : Complementary DOTA specifications, considering $I_1 = 25\ \mu\text{A}$, $\eta = 0.04$, $V_{cm} = 0.9\text{V}$, $L = 4L_{min}$ and $C_{DOTA-load} = 0.1\ \text{pF}$

Specs	$T = 27^\circ\text{C}$	$T = -40^\circ\text{C}$	$T = 125^\circ\text{C}$
V/V gain	25.03 dB	25.01 dB	25.11 dB
TC Gain	$\approx 66\ \text{ppm}/^\circ\text{C}$		
Phase-shift @ 1 MHz	$\approx -3.5^\circ$	$\approx -3^\circ$	$\approx -4.2^\circ$
Bandwidth	17 MHz	20 MHz	14 MHz
Average noise	$18\ \text{nV}/\sqrt{\text{Hz}}$	$14.9\ \text{nV}/\sqrt{\text{Hz}}$	$21.8\ \text{nV}/\sqrt{\text{Hz}}$
THD @1 MHz and 0.6V	-51 dB	-67 dB	-48 dB
Power consumption	$100.4\ \mu\text{W}$	$102.2\ \mu\text{W}$	$98.5\ \mu\text{W}$

E.4 A 105 dBΩ temperature aware two stages transimpedance amplifier

As shown in the previous section the complementary implementation of the DOTA can be used as a post-amplification stage following the proposed TIA. The Enhanced-Gain TIA (EGTIA) issued from cascading these two stages results in a gain of $\approx 80 + 25 = 105\ \text{dB}\Omega$. The EGTIA is then connected to the comparator of the MILO loop, the small parasitic capacitance at the input of this comparator is assumed of $C_{EGTIA-load} = C_{p-Comp} = 0.1$

pF. Under the same design parameters of the TIA and the DOTA, the EGTIA is simulated at the three temperatures: -40 , 27 , 125 °C. The corresponding frequency responses are depicted in Fig.E.1. From -40 to 125 °C, it can be observed that the gain change only of 0.4 dB (Fig.E.1(c)), the corresponding temperature coefficient is $TC \approx 268$ ppm/°C. Also, at the maximum operating frequency 1 MHz the absolute phase shift deviates by only 2° within the temperature range, with a maximum value of 8.1° at 125 °C (Fig.E.1(d)). This slight phase shift of 8.1° can be noticed from the transient response of the EGTIA shown in Fig. E.2. The circuit shows an average input noise of 3.87 pA/ \sqrt{Hz} and dissipates $445\mu W$ from 1.8 V supply. The remaining building blocks constituting the MILO loop including the comparator and the digital mixer have a small effect on the performance of the system. They can be implemented using hardly the same topologies as in [9]. A possible implementation of the CSA, and the peak detector demodulator (see Fig.E.1 for details) are discussed in the following sections.

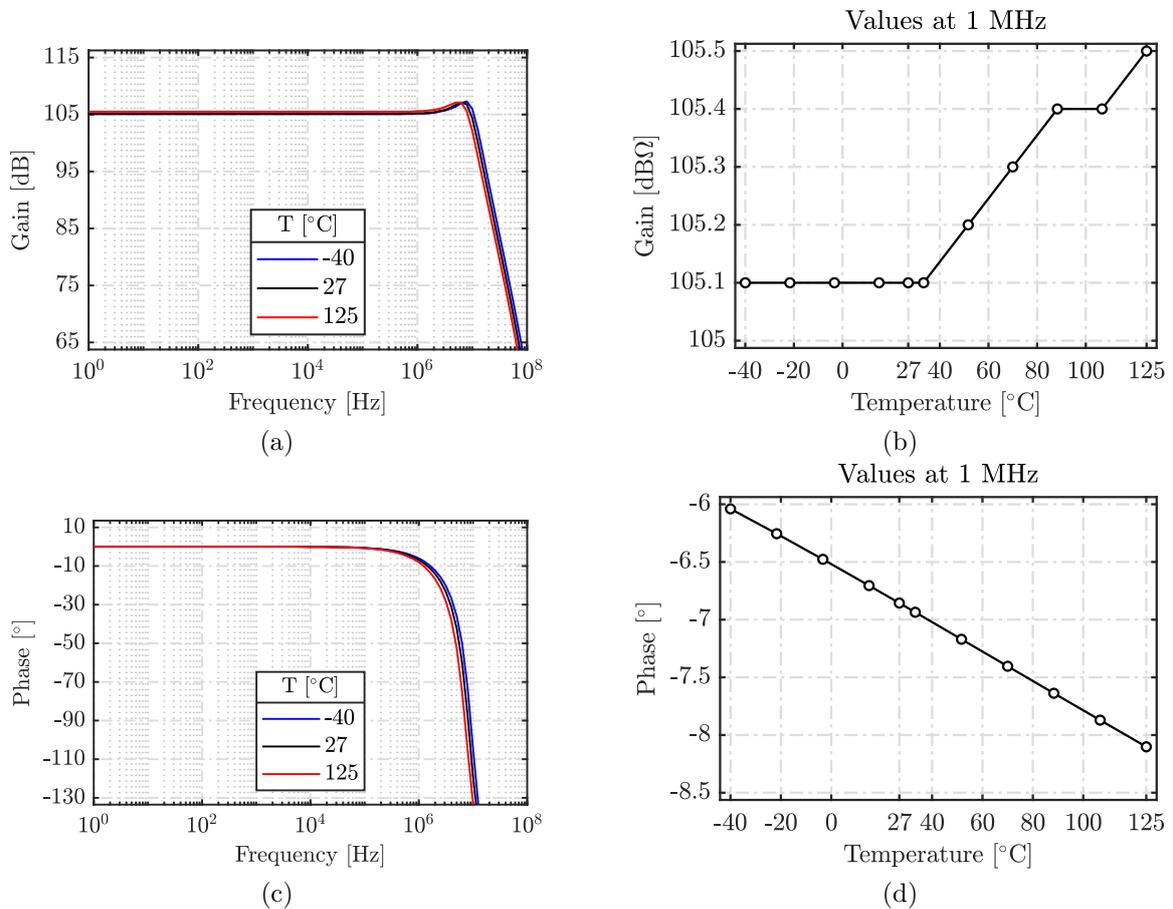


Figure E.1 : Frequency response of the enhanced gain TIA (EGTIA), (a) loop gain, and (c) loop phase at three the temperatures -40 , 27 , and 125 °C. $C_{p-MEMS} = 10$ pF $C_{EGTIA-load} = 0.1$ pF. The values at 1 MHz are given, in (b) for the gain, and in (d) for the phase

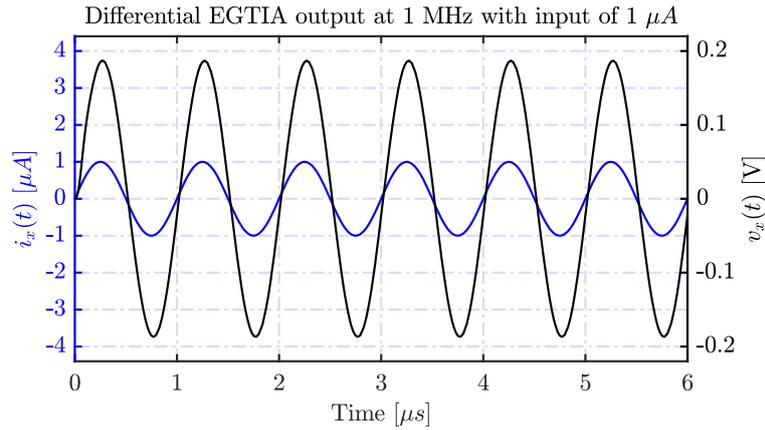


Figure E.2 : EGTIA output voltage $v_x(t)$ for $i_x(t)$ (differential) of $1\mu A$ at 1 MHz and $T = 125^\circ C$.

E.5 Temperature aware two stage miller compensated DOTA

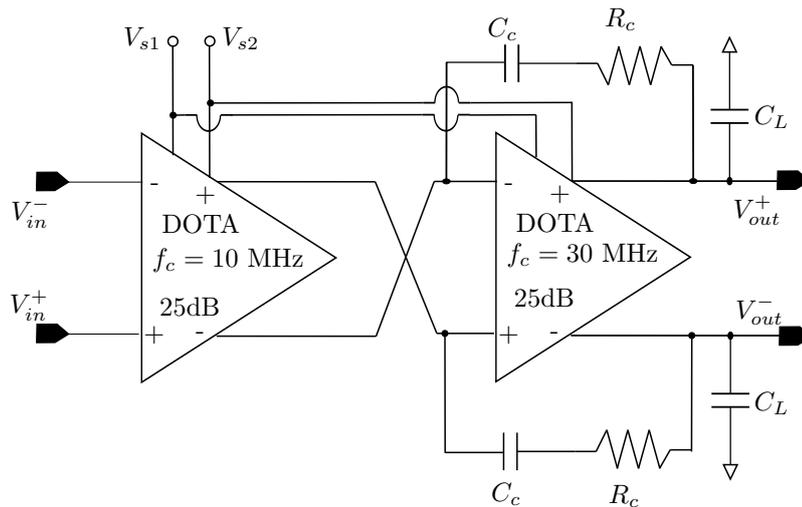


Figure E.1 : Proposed two stages DOTA

The proposed complementary DOTA operates with an input/output common mode voltage of $0.9 V$. Thus, it is possible to use the DOTA in a closed loop configuration for a given application, i.e. charge sensitive amplifier (CSA). However, the DOTA developed in this work poses a gain of 25 dB, this gain still relatively low considering a closed loop configuration. So that, the gain was increased by cascading 2 stages DOTA ($2 \times \text{DOTA}$), it ensues in a gain of ≈ 50 dB leading to a negligible closed loop error $\propto 1/G_2 \equiv 0.01\%$. In addition, the diode-connected load can be considered as a passive load. This relax the need of an additional common mode feedback circuit. However, the $2 \times \text{DOTA}$ amplifier has a double-poles that locate at the same frequency, hence the circuit is more likely

to be unstable considering closed loop utilization as shown in Fig.E.2. Thus, Miller-compensated technique is used to increasing the phase margin of the circuit by inserting a $R_c C_c$ branch between the stages as shown in Fig. E.1. This leads a shift of the pole placement of the first stage to a lower value and the pole of the second stage to a higher value. Moreover, the first DOTA is designed with a lower bandwidth ($f_{c1} \approx 10MHz$) than the second DOTA ($f_{c2} \approx 30MHz$) to help separating the two poles.

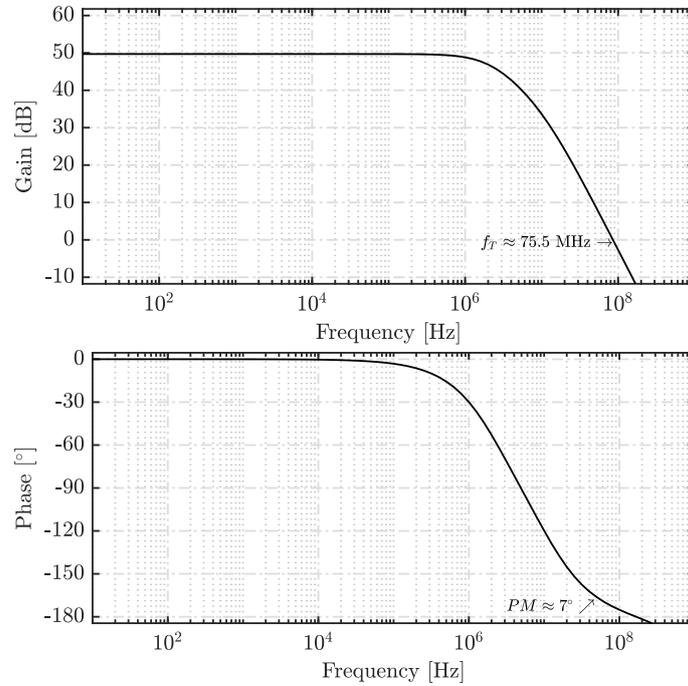


Figure E.2 : Nominal frequency response (Gain and Phase) of the cascaded two stages complementary DOTA before compensation

A phase margin larger than 60° is usually required considering transistor level design, so that a 25% degradation due to the fabrication process still tolerable ($PM > 45^\circ$). Assuming that the circuit is used in the charge amplifier CSA, the feedback charge capacitance (C_f) is usually well smaller than C_{p-MEMS} , typically in order of magnitude of $C_{p-MEMS}/10$, i.e. <1 pF. This capacitance will load the amplifier when studying its stability in open loop configuration, thus $C_L = C_f < 1$ pF. The value of R_c and C_c that demonstrate a proper compensation with a $PM > 60^\circ$ are found to be 2 k Ω and 1 pF respectively. The bode diagrams of the compensated $2 \times$ DOTA are illustrated in Fig. E.3, at the three different temperatures $-40, 27, 125^\circ C$, with $C_L = 1$ pF. As can be seen from (Fig. E.3(d)) the circuit has a $PM > 67^\circ$ over the temperature range, and a gain drift of lower than 0.6 dB with respect to the gain value at room temperature. The circuit consumes 355 μW from 1.8 V supply voltage.

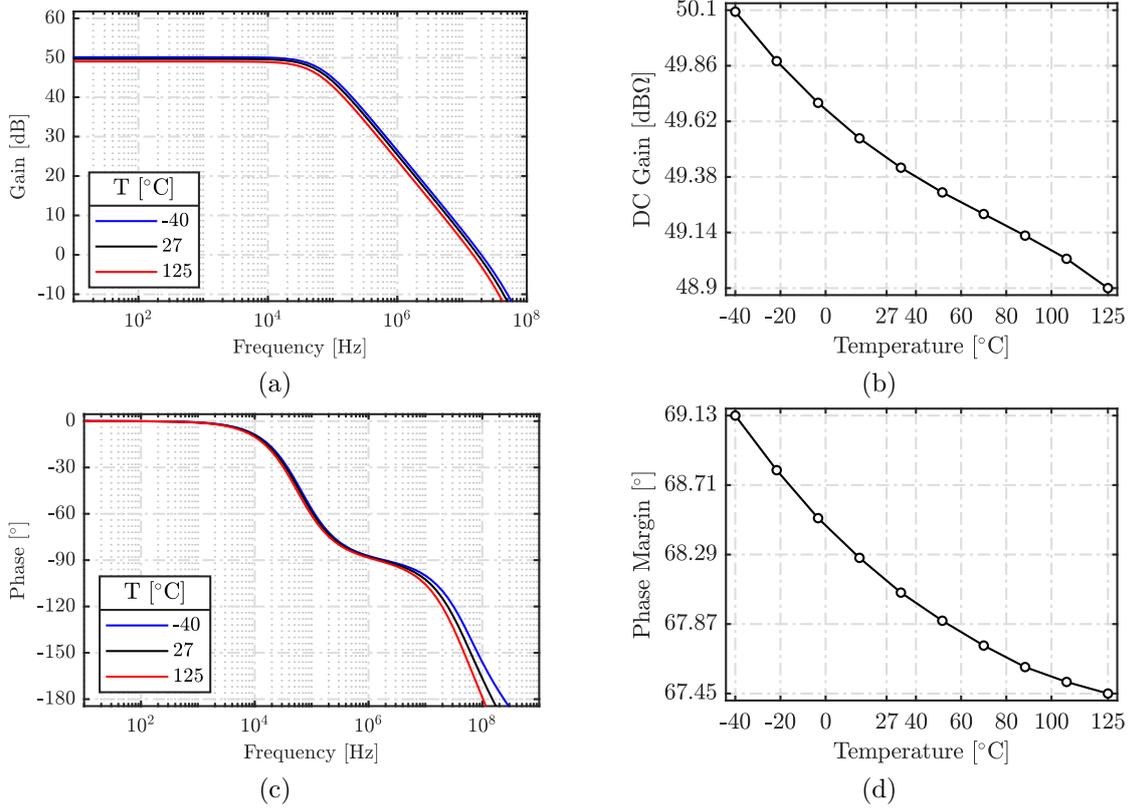


Figure E.3 : Frequency response of the cascaded two stages complementary DOTA after compensation, (a) loop gain, (b) DC-gain, (c) loop phase, and (d) phase margin, considering $C_c = 1$ pF, $R_c = 2$ kΩ and $C_L = 1$ pF.

E.6 Sample and hold peak detector

The demodulator peak-detector can be implemented using parasitic insensitive sample and hold circuit as shown in Fig. E.1(a). The charge phase Φ_{SH} has a narrow time delay $\sim T_s/10^3$ s, during which the voltage across the sample and hold capacitor (C_{SH}) tracks the peak value of the sensing voltage ($V_{ref} + \delta V$, see Fig. E.1 for details). Next, during the hold phase $\overline{\Phi_{SH}}$, the voltage across C_{SH} is buffered, filtered, and then delivered to the RM- $\Sigma\Delta$ M. In fact, the clock phase Φ_{SH} can be generated using logic gates and delay capacitors (C_{Delay}) as shown in Fig.E.1(b). For a maximum sampling duration of the order of ns ($T_s/10^3$), C_{Delay} of 30 fF is used. The resulting time diagram of Φ_{SH} and $\overline{\Phi_{SH}}$ are depicted in Fig.E.2, at $V_{DD}/2$ the sampling time (blue dashed curve) is approximately $t_{SH} \approx 1.8$ ns (the circuit is loaded by the equivalent parasitic capacitance of the TG switches).

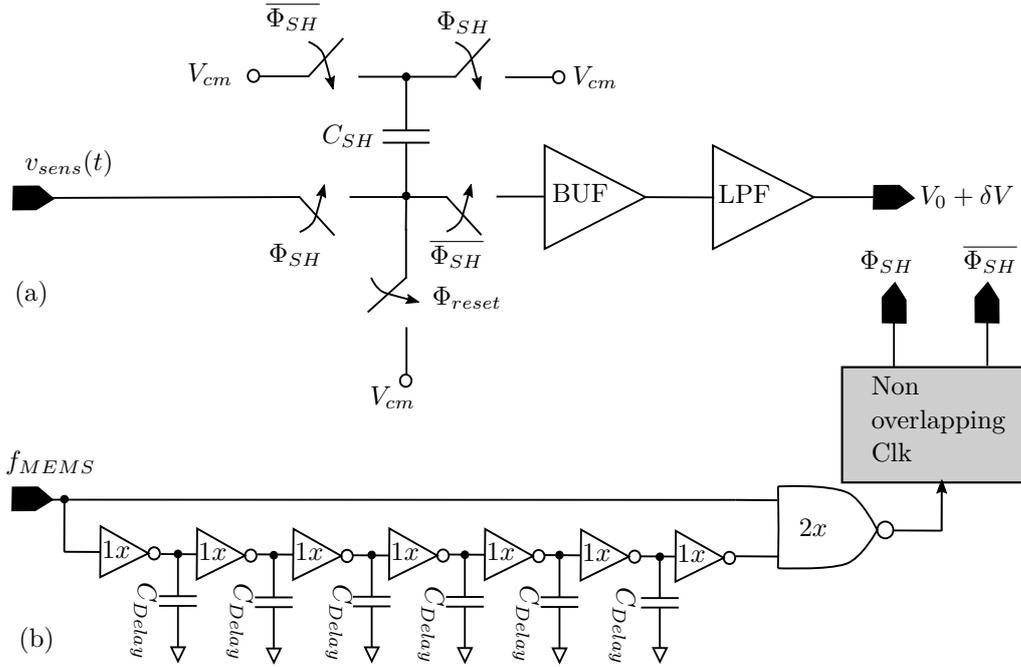


Figure E.1 : Proposed peak demodulator circuit, (a) sample and hold, and (b) clock generation

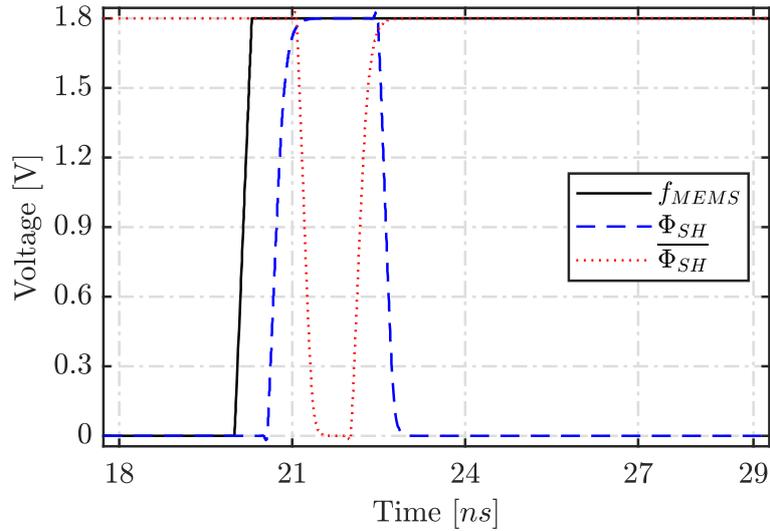


Figure E.2 : Sample and hold non-overlapped phases of Φ_{SH} and $\overline{\Phi_{SH}}$ obtained from the circuit shown in Fig. E.1(b) (without filtering) for $C_{Delay} = 30$ fF.

The sampling time constant $\tau_{SH} = 2R_{on}^{TG} \cdot C_{SH}$ must be for instance $\tau_{SH} < t_{SH}/5$, to ensure a 98% charge transfer, this leads to a $C_{SH} < 1.48$ pF considering $R_{on}^{TG} = 122\Omega$. However, this capacitance is smaller than the input capacitance of the RM- $\Sigma\Delta M$ ($C_{s1} = 4$ pF), meaning that the noise generated from the sample and hold network will be higher. Nevertheless, the value of v_{sens} change according to the MILO settling time ($\propto Q$). This relax the constraint related to C_{SH} since the peak value of v_{sens} can be tracked within

Q periods. As a result, C_{SH} can be set to any value that meets the requirements of the system. Figure E.3 represents the evolution of the demodulated signal (peak value) using C_{SH} of 5, 10 and 20 pF. It can be indicated that the peak value of v_{sens} can be fully tracked roughly after 8 periods considering a large C_{SH} of 20 pF, within this time ($8 \cdot T_s$), it can be practically assumed that v_{sens} does not change. However, these results are carried out using an ideal voltage buffer (BUF), and further analysis including noise and temperature effect of the real buffer implementation must be considered.

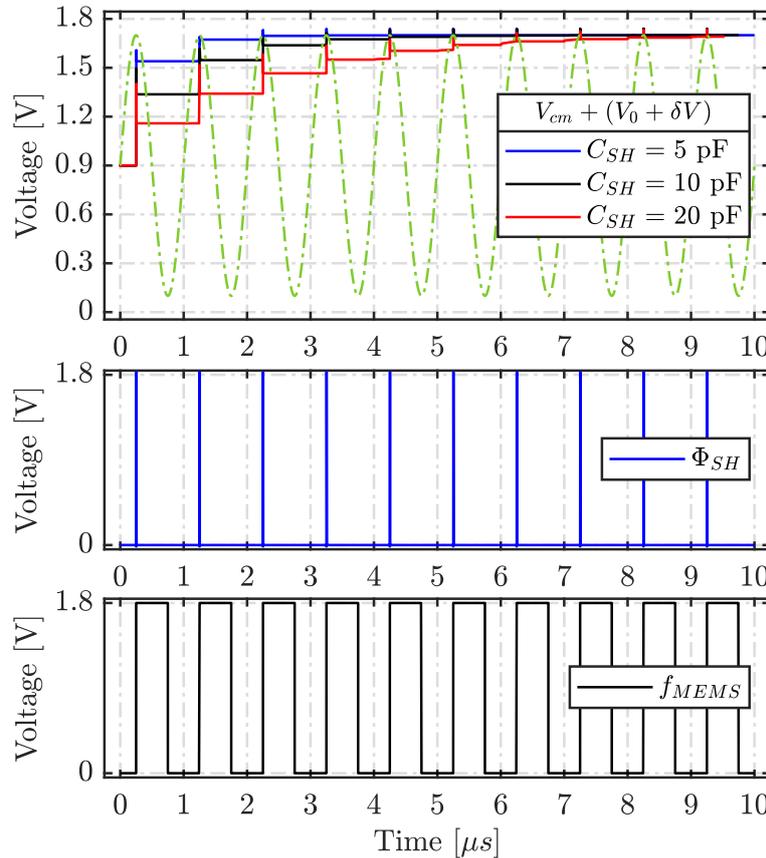


Figure E.3 : Input/Output of the sample and hold peak-detector circuit shown in Fig. E.1 using C_{SH} of 5, 10 and 20 pF, for $C_{Delay} = 30$ fF

E.7 Conclusion

In this chapter, the MILO sustaining electronics as well as the readout interface for the ratimetric measurement are discussed. The design of a temperature aware transimpedance amplifier is proposed and analysed. It deals with a signal frequency up to 1 MHz, while preserving a high thermal drift stability within the specified temperature range ($-40 < T < 125$ °C). The proposed circuit consists of two stages, the former is a current to voltage preamplifier based on the regulated cascode common gate TIA, having a conversion gain

of $80 \text{ dB}\Omega$, and the later is a post-amplification stage implemented using the diode-connected load OTA having a gain of 25 dB. The proposed TIA and DOTA gain stages posses "separately" a temperature coefficient ($TC = \frac{Gain^{max} - Gain^{min}}{\Delta T \cdot Gain^{nom}} \cdot 10^6$) of 92 ppm/°C and 66 ppm/°C respectively, and a TC of 268 ppm/°C when they are connected together. The circuit shows, a phase error of only 1° at the maximum operating frequency 1 MHz, an average input refereed noise current of $3.85 \text{ pA}/\sqrt{\text{Hz}}$, a bandwidth of 11 MHz, and dissipates $445 \text{ }\mu\text{W}$ form 1.8 V supply. Afterwards, a 50 dB gain amplifier with 0.6 dB drift error is proposed to be used in the charge amplifier of the readout interface. Finally, a possible implementation of the demodulator peak detector is described. This blocks are analyzed on a less detailed level than the TIA, but still the most significant properties are provided and important aspects regarding the design are listed.

Bibliography

- [1] C. Korvink, *Advanced Micro & Nanosystems*, 2005, vol. 2.
- [2] Y. Yin, Z. Fang, F. Han, B. Yan, J. Dong, and Q. Wu, “Design and test of a micromachined resonant accelerometer with high scale factor and low noise,” *Sensors and Actuators, A: Physical*, vol. 268, pp. 52–60, 2017. [Online]. Available: <http://dx.doi.org/10.1016/j.sna.2017.10.043>
- [3] X. Du, L. Wang, A. Li, L. Wang, and D. Sun, “High Accuracy resonant pressure sensor with balanced-mass DETF resonator and twinborn diaphragms,” *Journal of Microelectromechanical Systems*, vol. 26, no. 1, pp. 235–245, 2017.
- [4] S. Matthew, R. Arvind, Q. Alexander, and R. Reifenberger, “Ultrasensitive mass sensing using mode localization in coupled microcantilevers,” *Applied Physics Letters*, vol. 254102, no. May 2006, 2006.
- [5] A. Norouz Pour Shirazi, “Advanced interface systems for readout, control, and self-calibration of MEMS resonant gyroscopes,” Ph.D. dissertation, 2016. [Online]. Available: <https://smartech.gatech.edu/handle/1853/54936>
- [6] D. Coffin, S. Oliver, and J. Verwey, “Building Vehicle Autonomy : Sensors , Semiconductors , Software and U . S . Competitiveness,” 2019.
- [7] R. W. Johnson, J. L. Evans, P. Jacobsen, J. R. R. Thompson, and M. Christopher, “The Changing Automotive Environment : High-Temperature Electronics,” *IEEE Transactions on electronics packaging manufacturing*, vol. 27, no. 3, pp. 164–176, 2004.
- [8] G. ARNDT, “System architecture and circuit design for micro and nanoresonators-based mass sensing arrays,” 2011.
- [9] P. Prache, J. Juillard, P. M. Ferreira, N. Barniol, and M. Riverola, “Design and characterization of a monolithic CMOS-MEMS mutually injection-locked oscillator for differential resonant sensing,” *Sensors and Actuators, A: Physical*, vol. 269, pp. 160–170, 2018. [Online]. Available: <http://dx.doi.org/10.1016/j.sna.2017.11.025>
- [10] P. Thiruvengatanathan, J. Yan, J. E. Lee, and A. A. Seshia, “Enhancing parametric

- sensitivity using mode localization in electrically coupled mems resonators,” *Journal of Microelectromechanical Systems*, vol. 18, no. 5, pp. 2350–2353, 2009.
- [11] J. Juillard, P. Prache, and N. Barniol, “Analysis of mutually injection-locked oscillators for differential resonant sensing,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 7, pp. 1055–1066, 2016.
- [12] J. Juillard, A. Mostafa, and P. M. Ferreira, “Nonlinear operation of resonant sensors based on weakly- coupled resonators: experimental investigation of an actively-coupled architecture,” 2019. [Online]. Available: <https://hal-centralesupelec.archives-ouvertes.fr/hal-01992556v2>
- [13] —, “Nonlinear operation of resonant sensors based on weakly - coupled resonators : theory and modeling,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control (TUFFC)*, vol. 66, no. 12, 2019.
- [14] P. M. Ferreira, J. R. R. O. Martins, A. Mostafa, and J. Juillard, “Process-Voltage-Temperature Analysis of a CMOS-MEMS Readout Architecture,” *2019 Symposium on Design, Test, Integration and Packaging of MEMS and MOEMS, DTIP 2019*, pp. 19–22, 2019.
- [15] M. Pandit, S. Member, C. Zhao, G. Sobreviela, A. Mustafazade, and S. Du, “Closed-loop Characterization of Noise and Stability in a Mode-localized Resonant MEMS Sensor,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. PP, no. October, p. 1, 2018.
- [16] “XFAB Mixed-Signal Foundry Experts,” 2020. [Online]. Available: <https://www.xfab.com/technology/cmos/018-um-xh018/>
- [17] A. Mostafa, J. Juillard, J. R. Raposo, and P. M. Ferreira, “An Adaptative Ratio-Metric Analog-To-Digital Interface For Weakly-Coupled Resonant Sensors Based On Mutually Injection-Locked Oscillators,” *2019 Symposium on Design, Test, Integration & Packaging of MEMS and MOEMS (DTIP)*, no. Vd, pp. 1–4, 2019.
- [18] J. Juillard, A. Mostafa, P. M. Ferreira, M. Gouspy, and M. Kraft, “A highly-linear , integration-compatible output metric for amplitude-modulated resonant sensors based on weakly-coupled resonators,” *2020 SENSORS*, vol. 1, no. 0, pp. 2–5, 2020.
- [19] J. Juillard, P. M. Ferreira, and A. Mostafa, “Nonlinear enhancement of locking range of mutually injection-locked oscillators for resonant sensing applications,” *2018 European Frequency and Time Forum (EFTF)*, pp. 109–113, 2018.
- [20] J. Juillard, A. Mostafa, and P. M. Ferreira, “Analysis of resonant sensors based on mutually injection-locked oscillators beyond the critical Duffing amplitude,” *2018 European Frequency and Time Forum (EFTF)*, no. 1, pp. 114–118, 2018.
- [21] J. Martins, A. Mostafa, J. Juillard, R. Hamani, A. Francisco, and P. M. Ferreira, “A

- Temperature-Aware Framework on gm/ID-Based Methodology using 180 nm SOI from -40 °C to 200 °C,” *IEEE Open Journal of Circuits and Systems*, vol. 2, no. December 2020, pp. 1–1, 2021.
- [22] A. Brenes, “Modélisation des phénomènes non-linéaires dans un capteur MEMS résonant pour l’optimisation de ses performances et de sa fiabilité To cite this version : HAL Id : tel-01394374 L’U NIVERSITE P ARIS -S ACLAY,” 2016.
- [23] A. N. Cleland and M. L. Roukes, “Noise processes in nanomechanical resonators,” *Journal of Applied Physics*, vol. 92, no. 5, pp. 2758–2769, 2002.
- [24] Z. Fang, Y. Yin, X. He, F. Han, and Y. Liu, “Temperature-drift characterization of a micromachined resonant accelerometer with a low-noise frequency readout,” *Sensors and Actuators, A: Physical*, vol. 300, p. 111665, 2019. [Online]. Available: <https://doi.org/10.1016/j.sna.2019.111665>
- [25] S. Wang, X. Wei, Y. Weng, Y. Zhao, and Z. Jiang, “A Novel Single-Axis MEMS Tilt Sensor with a High Sensitivity in the Measurement Range,” *Sensors 2018*, vol. 18, no. 346, 2018. [Online]. Available: TiltSensor2018
- [26] C. Zhao, M. Pandit, G. Sobreviela, and P. Steinmann, “A Resonant MEMS Accelerometer With 56ng Bias Stability and 98ng/Hz^{0.5} Noise Floor,” *Journal of microelectromechanical systems*, vol. 28, no. 3, pp. 2019–2021, 2019.
- [27] A. Gelb and E. V. Velde, *Multiple-input describing functions and nonlinear system design*, 1968.
- [28] H. K. Lee, R. Melamud, S. Chandorkar, J. Salvia, S. Yoneoka, and T. W. Kenny, “Stable Operation of MEMS Oscillators Far Above the Critical Vibration Amplitude in the Nonlinear Regime,” *Journal of microelectromechanical systems*, vol. 20, no. 6, pp. 1228–1230, 2011.
- [29] X. Zou, A. A. Seshia, and S. Member, “Non-Linear Frequency Noise Modulation in a Resonant MEMS Accelerometer,” *IEEE Sensors Journal*, vol. 17, no. 13, pp. 4122–4127, 2017.
- [30] I. P. Prikhodko, A. A. Trusov, and A. M. Shkel, “Compensation of drifts in high-Q MEMS gyroscopes using temperature self-sensing,” *Sensors & Actuators: A. Physical*, vol. 201, pp. 517–524, 2013. [Online]. Available: <http://dx.doi.org/10.1016/j.sna.2012.12.024>
- [31] J. C. Salvia, R. Melamud, S. A. Chandorkar, S. F. Lord, and T. W. Kenny, “Real-time temperature compensation of mems oscillators using an integrated micro-oven and a phase-locked loop,” *Journal of Microelectromechanical Systems*, vol. 19, no. 1, pp. 192–201, 2010.
- [32] R. G. Azevedo, W. Huang, O. M. O. Reilly, and A. P. Pisano, “Physical Dual-mode

- temperature compensation for a comb-driven MEMS resonant strain gauge,” *Sensors and Actuators A* ;, vol. 144, pp. 374–380, 2008.
- [33] D. D. Shin, C. H. Ahn, Y. Chen, D. L. Christensen, I. B. Flader, and T. W. Kenny, “Environmentally robust differential resonant accelerometer in a wafer-scale encapsulation process invensense incorporated , San Jose , California , USA,” *MEMS 2017*, pp. 17–20, 2017.
- [34] J. R. Vig, “Temperature-Insensitive Dual-Mode Resonant Sensors — A Review,” *IEEE Sensors journal*, vol. 1, no. 1, pp. 62–68, 2001.
- [35] Y. Chen, D. D. Shin, I. B. Flader, and T. W. Kenny, “Tri-mode operation of highly doped silicon resonators for temperature compensated timing references,” pp. 1158–1161, 2017.
- [36] J. Juillard, A. Bonnoit, N. Barniol, A. Uranga, and G. Vidal-álvarez, “A novel architecture for differential resonant sensing,” *Procedia Engineering*, vol. 87, pp. 1573–1576, 2014. [Online]. Available: <http://dx.doi.org/10.1016/j.proeng.2014.11.601>
- [37] P. Thiruvenkatanathan, J. Woodhouse, J. Yan, and A. Seshia, “Limits to mode-localized sensing using micro- and nanomechanical resonator arrays,” *Journal of Applied Physics*, vol. 104903, no. October 2010, 2011.
- [38] M. R. Nabavi and S. Nihtianov, “A novel interface for eddy current displacement sensors,” *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 5, pp. 1623–1632, 2009.
- [39] STMicroelectronics, “AIS328DQ,” pp. 1–45, 2020. [Online]. Available: <https://www.st.com/resource/en/datasheet/ais328dq.pdf>
- [40] T. invenSense, “High Performance 6-Axis MotionTracking Device,” pp. 1–51, 2016. [Online]. Available: <https://invensense.tdk.com/wp-content/uploads/2017/11/DS-000196-IAM-20680-v1.1-Typ.pdf>
- [41] STMicroelectronics, “AIS1200PS MEMS acceleration sensor ;,” 2015. [Online]. Available: <https://www.st.com/resource/en/datasheet/ais1200ps.pdf>
- [42] Murata, “Sca830-D07 1-Axis Inclinator With Digital Spi Interface,” pp. 1–5. [Online]. Available: https://www.murata.com/-/media/webrenewal/products/sensor/pdf/datasheet/datasheet{__}sca830-d07.ashx?la=en-gb{&}cvid=20190118045358805600
- [43] J. G. GRAEME, *Graeme - Applications of Operational Amplifiers 3rd generation techniques 1973.pdf*, 1973.
- [44] K. C. Selvam and S. Latha, “A Novel Voltage Divider Circuit,” *ETASR - Engineering*,

- Technology & Applied Science Research*, vol. 2, no. 5, pp. 278–280, 2012.
- [45] A. Fekri, M. Nabavi, N. Radelji, Z.-y. Chang, M. Pertijs, and S. Nihtianov, “An Eddy-Current Displacement-to-Digital Converter Based on a Ratio-Metric Delta-Sigma ADC,” pp. 403–406, 2014.
- [46] R. Schreier, “Understanding Delta-Sigma Data Converters,” 2005.
- [47] T. C. Carusone, D. A. Johns, and K. W. Martin, *Analog Integrated Circuit Design*, 2nd ed. John Wiley & Sons, Inc, 2012.
- [48] ALEX C and DAKESIAN S, *Continuous-Time Sigma-Delta A/D Conversion*, 2006, vol. 3, no. 3.
- [49] W. Kester, “Analog devices: Taking the Mystery out of the Infamous Formula, "SNR = 6.02N + 1.76dB," and Why You Should Care,” 2009.
- [50] A. Baltolu, “Etude et conception analogique d’architectures d’acquisition acoustique très faible consommation pour applications mobiles,” 2019.
- [51] C. Jabbour, “Conversion analogique numérique Sigma Delta reconfigurable à entrelacement temporel,” 2011.
- [52] G. Vemulapalli, P. K. Hanumolu, Y.-j. Kook, and U.-k. Moon, “A 0.8-V Accurately Tuned Linear Continuous-Time Filter,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1972–1977, 2005.
- [53] K. Philips, P. A. C. M. Nuijten, R. Roovers, F. Munoz, and M. Tejero, “Increased Immunity to Wide-Band Interferers • 2004 IEEE International Solid-State Circuits Conference,” *IEEE International Solid-State Circuits Conference*, vol. 37, no. 3, pp. 271–278, 2004.
- [54] J. A. Cherry and W. M. Snelgrove, “Clock Jitter and Quantizer Metastability in Continuous-Time Delta – Sigma Modulators,” *IEEE Transactions on circuits and systems—II: analog and digital signal processing*, vol. 46, no. 6, pp. 661–676, 1999.
- [55] A. Dendouga, N.-e. Bouguechal, S. Kouda, and S. Barra, “Modeling of a Second Order Non-Ideal Sigma- Delta Modulator,” *International Journal of Electronics and Communication Engineering*, vol. 4, no. 8, pp. 327–332, 2010.
- [56] M. R. Valero, N. Medrano, S. Celma, and B. Calvo, “A high-performance 1.2 V-99 μ w rail-to-rail CMOS class AB amplifier,” *Microelectronics Journal*, vol. 46, no. 1, pp. 96–102, 2015. [Online]. Available: <http://dx.doi.org/10.1016/j.mejo.2014.10.011>
- [57] J. V. D. I. C. Marin, “Integrated Circuit Design of Sigma-Delta Modulator for Electric Energy Measurement Applications,” pp. 1–100, 2013. [Online]. Available: <http://pee.ufrj.br/teses/textocompleto/2013100701.pdf>

- [58] Geyer-Electronic, “Comparison of a Crystal Oscillator to a MEMS Oscillator Crystal vs MEMS.” [Online]. Available: <https://www.geyer-electronic.de>
- [59] R. Schreier and T. Caldwell, “Design-Oriented Estimation of Thermal Noise in Switched-Capacitor Circuits.” [Online]. Available: <http://individual.utoronto.ca/schreier/lectures/10-2.pdf>
- [60] H. Omran, “Optimum split ratio for folded cascode OTA bias current: A qualitative and quantitative study,” *Proceedings of the International Conference on Microelectronics, ICM*, vol. 2019-Decem, no. 1cl, pp. 223–226, 2019.
- [61] S. George, J. Manuel, and F. Fernández, “Behavioral Modeling Methods for Switched-,” *IEEE Transactions on circuits and systems—I: regular papers*, vol. 54, no. 6, pp. 1236–1244, 2007.
- [62] R. Rio, E. Medeiro, and B. Pe, “Reliable analysis of settling errors in sc integrators - application to the design of high-speed,” *IEEE International Symposium on Circuits and Systems*, pp. 28–31, 2000.
- [63] P. Malcovati, S. Brigati, and F. Francesconi, “Behavioral Modeling of Switched-Capacitor Sigma – Delta Modulators,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 50, no. 3, pp. 352–364, 2003.
- [64] A. P. Perez, Y. B. Nithin Kumar, E. Bonizzoni, and F. Maloberti, “Slew-rate and gain enhancement in two stage operational amplifiers,” *Proceedings - IEEE International Symposium on Circuits and Systems*, pp. 2485–2488, 2009.
- [65] J. Ou, P. M. Ferreira, and A. T. Noise, “Folded-Cascode Operational Amplifier,” *IEEE Transactions on circuits and systems—II: express briefs*, vol. 61, no. 10, pp. 783–787, 2014.
- [66] M. Akbari, O. Hashemipour, and F. Moradi, “Input Offset Estimation of CMOS Integrated Circuits in Weak Inversion,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 9, pp. 1812–1816, 2018.
- [67] P. Toledo, H. Klimach, D. Cordova, S. Bampi, and E. Fabris, “Low temperature sensitivity CMOS transconductor based on GZTC MOSFET condition,” *Journal of Integrated Circuits and Systems*, vol. 11, no. 1, pp. 27–37, 2016.
- [68] O. Choksi and L. R. Carley, “Analysis of Switched-Capacitor Common-Mode Feedback Circuit,” *IEEE Transactions on circuits and systems—II: analog and digital signal processing*, vol. 50, no. 12, pp. 906–917, 2003.
- [69] A. Zhang and G. Shi, “A fast symbolic SNR computation method and its Verilog-A implementation for Sigma-Delta modulator design optimization,” *Integration, the VLSI Journal*, vol. 60, no. 61176129, pp. 190–203, 2018. [Online]. Available: <https://doi.org/10.1016/j.vlsi.2017.09.007>

- [70] G. Zheng, S. P. Mohanty, and E. Kougianos, "Design and Modeling of a Continuous-Time Delta-Sigma Modulator for Biopotential Signal Acquisition : Simulink Vs Verilog-AMS Perspective." [Online]. Available: <http://individual.utoronto.ca/schreier/lectures/10-2.pdf>
- [71] A. F. Yeknami, *Low-Power Delta-Sigma Modulators for Medical Applications*, 2011, no. 1563.
- [72] C. Galup-Montoro, M. C. Schneider, A. I. Cunha, F. R. De Sousa, H. Klimach, and O. F. Siebel, "The Advanced Compact MOSFET (ACM) Model for Circuit Analysis and Design," *Proceedings of the IEEE 2007 Custom Integrated Circuits Conference, CICC 2007*, no. Cicc, pp. 519–526, 2007.
- [73] Y. Tsvividis and C. Mcandrew, "Operation and Modeling of the MOS Transistor by Yannis Tsvividis, Colin McAndrew. 3rd ed." 2011.
- [74] P. G. A. Jespers and B. Murmann, *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*. Cambridge University Press, 2017.
- [75] C. E. L. Etricos, "Circuitos Eléctricos, métodos de análise introdução à Síntese," 2019.
- [76] C. Huang, Y. Wu, S. Cong, Y. Yu, C. Zhao, H. Liu, H. Tang, Y. Xue, and K. Kang, "An Improved Surface Potential-Based High-Order Channel Length Modulation Model," in *IEEE Asia-Pacific Microwave Conference (APMC)*, no. 2006. IEEE, 2019, pp. 2019–2021.
- [77] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, 3rd ed., 2010.
- [78] D. Schinkel, E. Mensink, E. Klumperink, and E. V. Tuijl, "A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," in *IEEE International Solid-State Circuits Conference*, 2007, pp. 314–316.
- [79] A. V. Fonseca, L. Cron, F. A. Barúqui, C. F. Soares, P. Benabes, and P. M. Ferreira, "A temperature-aware analysis of SAR ADCs for smart vehicle applications," *Journal of Integrated Circuits and Systems*, vol. 13, no. 1, pp. 1–6, 2018.
- [80] J. Reiss, Q. Mary, M. B. Sandler, and Q. Mary, "A Mechanism For The Detection And Removal Of Limit Cycles In The Operation Of Sigma Delta Modulators," *IEEE Transactions on Circuits and Systems I: Regular Paper*, no. May 2014, 2008.
- [81] A. R. Chowdhury, N. Wary, and P. Mandal, "A Regulated-Cascode Based Current-Integrating TIA RX with 1-tap Speculative Adaptive DFE," *Midwest Symposium on Circuits and Systems*, vol. 2019-Augus, pp. 790–793, 2019.
- [82] D. Chen, K. S. Yeo, X. Shi, M. A. Do, C. C. Boon, and W. M. Lim, "Cross-coupled current conveyor based CMOS transimpedance amplifier for broadband data transmission," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*,

vol. 21, no. 8, pp. 1516–1525, 2013.

[83] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2001.

[84] H. Liu, X. Zhu, C. C. Boon, and X. He, “Cell-based variable-gain amplifiers with accurate dB-linear characteristic in 0.18 μm CMOS technology,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 2, pp. 586–596, 2015.