



**HAL**  
open science

# Ultra-Low Power Frequency Synthesizer For Internet-of-Things applications In 28nm FD-SOI technology

David Gaidioz

► **To cite this version:**

David Gaidioz. Ultra-Low Power Frequency Synthesizer For Internet-of-Things applications In 28nm FD-SOI technology. Electronics. Université de Bordeaux, 2021. English. NNT : 2021BORD0135 . tel-03336167

**HAL Id: tel-03336167**

**<https://theses.hal.science/tel-03336167>**

Submitted on 7 Sep 2021

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

THÈSE PRÉSENTÉE  
POUR OBTENIR LE GRADE DE

**DOCTEUR DE**

**L'UNIVERSITÉ DE BORDEAUX**

ECOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGÉNIEUR  
SPECIALITÉ ÉLECTRONIQUE

Par David GAIDIOZ

**Ultra-Low Power Frequency Synthesizer  
For Internet-of-Things applications  
In 28nm FD-SOI technology**

Sous la direction de : Yann DEVAL & Andreia CATHELIN

Préparée à STMICROELECTRONICS et au Laboratoire IMS.

Soutenue le 30 mars 2021

Membres du jury :

M. KERHERVE, Eric	Professeur	Bordeaux INP	Président
M. ABIDI, Asad	Professeur	University of California	Rapporteur
M. KAISER, Andreas	Directeur de recherche	Université de Lille	Rapporteur
M. BAKKALOGLU, Bertan	Professeur,	Arizona State University	Examineur
Mme. WANG, Alice	Dr. Design Senior Expert	Everactive, California	Examineur
Mme. DELTIMPLE, Nathalie	Maitre de conférences, HDR	Bordeaux INP	Examineur
M. RIVET Francois	Maitre de conférences, HDR	Bordeaux INP	Invité
M. DEVAL, Yann	Professeur	Bordeaux INP	Directeur
Mme. CATHELIN, Andreia	Dr. HDR, Design Senior Expert	STMicroelectronics	Co-Directeur



# Acknowledgements

Before starting this manuscript, I would like to acknowledge all the people that had an important impact on my thesis.

In the first place, I would like to thank Asad Abidi and Andreas Kaiser who have accepted to handle the review of this thesis. Thank you for your time and your interesting discussions related to my thesis' work.

I would also like to thank all members of the jury, Alice Wang, Bertan Bakkaloglu, Nathalie Deltimple, and François Rivet who accepted to be part of my defense's jury. An additional special thanks to Eric Kerherve who accepted to be the president of my jury.

It is time for me to switch in French to continue these acknowledgements. Je souhaite remercier sincèrement mes directeurs de thèse Yann Deval et Andreaia Cathelin pour leur patience, leur soutien et surtout leur confiance tout au long de ces années de thèse. Vos précieux conseils me suivront longtemps dans cette nouvelle vie professionnelle post-thèse qui commence.

Cette thèse s'est déroulée au sein du laboratoire commun ST-IMS entre le laboratoire IMS de Bordeaux et STMicroelectronics Crolles. Je souhaite dans un premier temps remercier tous les membres du laboratoire IMS et tout particulièrement François pour m'avoir recueilli au sein de son équipe Circuits and Systems (CAS) ainsi que mes anciens collègues Herve et Nathalie pour leurs discussions et leur bonne humeur tout au long de ces années de thèse. Un merci tout particulier à Magali pour son aide et son temps lors de nos sessions de mesures qui ont pu finaliser tout le travail fourni dans cette thèse.

Je tiens aussi à remercier tous mes collègues actuels de STMicroelectronics, tout spécialement Philippe et Frederic pour leur conseils techniques et leur temps lors des nombreuses questions que j'ai pu poser durant cette thèse.

Enfin, des remerciements particuliers pour tous mes camarades de Bordeaux et Crolles, pour ces petits moments de la vie quotidienne qui magnifient ces années de thèse. Pour n'en citer que quelques-uns, merci à Yann, Manuel, Romane, Hugo, Guillaume, Raphaël, Thibaut, Samuel, Andres, Denis et surtout merci à l'élite de la cuvette grenobloise : Antoine, Robin et Sebastien.

Je n'oublie évidemment pas les plus importants. Je souhaite sincèrement remercier mes parents et ma moitié Constance, qui ont vécu avec la même intensité que moi ces années de thèse.

*"Victoriae mundis et mundis lacrima. Bon, ça ne veut absolument rien dire, mais je trouve que c'est assez dans le ton."*  
A. Astier



# Table of contents

Table of contents .....	- 5 -
List of Figures .....	- 8 -
List of Tables.....	- 8 -
Chapter 1: General Introduction.....	- 13 -
Chapter 2: Trends and Challenges of Internet of Things Frequency Synthesizer .....	- 15 -
2.1 Frequency synthesizer trends for Internet-of-Things application.....	- 15 -
2.2 Frequency synthesizer state-of-the-art at the beginning of this work.....	- 17 -
2.3 Review of bandwidth versus channel spacing trade-offs in PLLs.....	- 19 -
2.4 Conclusion: Motivation of this thesis.....	- 21 -
Chapter 3: Proposed Dual-loop Integer-N PLL: Caliper PLL Architecture.....	- 23 -
3.1 Introduction .....	- 23 -
3.2 Caliper PLL architecture .....	- 24 -
3.3 Laplace Model of Caliper PLL architecture.....	- 27 -
3.3.1 Caliper PLL phase-domain model.....	- 27 -
3.3.2 Open Loop parameter sizing .....	- 28 -
3.3.3 Caliper PLL frequencies sizing .....	- 32 -
3.3.4 Stability verification of the system.....	- 33 -
3.4 Noise analysis.....	- 35 -
3.4.1 Noise sources and metrics .....	- 35 -
3.4.2 Phase noise domain model .....	- 40 -
3.5 Behavioral proof of concept.....	- 46 -
3.6 Conclusion.....	- 50 -
Chapter 4: Ring Voltage Controlled Oscillators study in the context of FD-SOI technology .....	- 53 -
4.2 Ring versus LC oscillators comparison.....	- 54 -
4.3 Tuning strategy of a ring-oscillator .....	- 55 -
4.4 RO study under the scope of the ISF theory.....	- 58 -
4.5 Pseudo-differential RVCO architecture .....	- 60 -
4.6 RVCO and PRVCO implementation and measurements .....	- 63 -
4.7 Conclusion.....	- 67 -

Chapter 5: Design Implementation of Caliper PLL Architecture.....	- 69 -
5.1 Introduction .....	- 69 -
5.2 Ring Voltage Controlled Oscillators .....	- 70 -
5.3 Mixer .....	- 71 -
5.3.1 Digital Down-conversion Frequency Mixer (DFM) .....	- 71 -
5.3.2 DFM implementation and measurements .....	- 77 -
5.3.3 DFM implementation inside the Caliper PLL .....	- 79 -
5.3.4 Conclusion.....	- 80 -
5.4 Charge Pump .....	- 80 -
5.4.1 Charge pump challenge .....	- 80 -
5.4.2 Proposed Bootstrapped current source .....	- 82 -
5.4.3 Biasing circuit: $V_T$ dependent voltage reference .....	- 85 -
5.4.4 Charge pump simulation and conclusion.....	- 87 -
5.5 Others Caliper PLL building blocks.....	- 88 -
5.5.1 Phase Frequency Detector (PFD) .....	- 88 -
5.5.2 PFD and Charge Pump Association .....	- 89 -
5.5.3 Digital frequency divider.....	- 89 -
5.5.4 Transimpedance low-pass filter.....	- 91 -
5.6 Physical PLL implementation and design for test .....	- 92 -
5.6.1 Top-level strategy .....	- 92 -
5.6.2 Ring oscillators.....	- 93 -
5.6.3 Digital mixer.....	- 94 -
5.6.4 Charge Pump .....	- 95 -
5.6.5 Phase Frequency Detector .....	- 97 -
5.6.6 Digital frequency divider.....	- 98 -
5.6.7 Transimpedance low-pass filter.....	- 99 -
5.7 Global PLL simulation .....	- 101 -
5.8 Conclusion.....	- 105 -
Chapter 6: Measurement Results of Caliper PLL Architecture.....	- 107 -
6.1 Introduction .....	- 107 -
6.2 Measurements set-up.....	- 107 -
6.3 Measurement results of the Caliper PLL architecture .....	- 109 -
6.4 Caliper PLL performance comparison with the state-of-the-art.....	- 115 -

6.5	Conclusion.....	- 120 -
Chapter 7: Conclusion and Perspectives .....		- 123 -
7.1	General conclusion .....	- 123 -
7.2	Perspectives .....	- 126 -
Appendix A: Open-loop phase margin and open-loop transfer function .....		- 129 -
A.1	Third order PLL open-loop phase margin computation .....	- 129 -
A.2	Expression of the Caliper PLL open-loop transfer function.....	- 132 -
Appendix B: Noise transfer function and phase noise contribution .....		- 135 -
B.1	Secondary loop filter noise transfer function computation .....	- 135 -
B.2	Secondary loop filter noise contribution .....	- 136 -
Appendix C: Detailed computation of Impulse Sensitivity Function.....		- 137 -
Appendix D: Digital down-conversion frequency mixer .....		- 141 -
Bibliography.....		- 143 -

# List of Figures

Figure 2.1: Internet-of-Things domains of application.	15
Figure 2.2: Block diagrams of a Transceiver (a) and PLL architecture (b).	15
Figure 2.3: Block diagram for conventional integer-N (a) and fractional-N PLL (b).	19
Figure 2.4: Phase noise profile of integer-N PLL and fractional-N PLL for narrow PLL bandwidth (a and c) and wide PLL bandwidth (b and d).	20
Figure 2.5: Proposed frequency synthesizer to fulfill Internet-of-Things application.	21
Figure 3.1: Detailed block diagram of the proposed Caliper PLL architecture	24
Figure 3.2: Caliper PLL Laplace model.	27
Figure 3.3 Representation of ripple effect due to the PFD pulse (a), and (b) Laplace representation of the second order transconductance filter topology.	28
Figure 3.4 Open-loop pulsation scalabing	29
Figure 3.5: Loop-filter capacitance ratio versus open-loop phase margin.	31
Figure 3.6: Bode plot of the primary loop open-loop transfer function.	33
Figure 3.7: Bode plot of the secondary loop open-loop transfer function	33
Figure 3.8: Bode plot of the Caliper synthesizer open-loop transfer function.	34
Figure 3.9: Bode plot of the Caliper synthesizer closed-loop transfer function.	34
Figure 3.10. Power spectrum representation of an ideal oscillator (a) and (b) real oscillator.	37
Figure 3.11 Oscillator Phase Noise representation in log scale.	37
Figure 3.12 Reference spurs representation (a) and (b) Adjacent channel interference.	38
Figure 3.13 Phase jitter representation in time domain (a) and (b) Phase noise with area representation.	39
Figure 3.14 Caliper PLL phase domain model.	40
Figure 3.15 Phase noise representations of reference noise (a) and (b) primary loop oscillator noise.	42
Figure 3.16 Simulated phase noise model of the Caliper PLL representing the four main contributions (noise from the dividers, both oscillators and the reference).	44
Figure 3.17 Total phase noise model of the Caliper PLL representing each noise contribution.	45
Figure 3.18 Simulink model of the Caliper PLL Architecture.	46
Figure 3.19 Simulated output frequency for a 2.42 GHz output frequency.	47
Figure 3.20 Simulated oscillator control voltage representation.	48
Figure 3.21 Perturbation representation of the reference frequency.	49
Figure 3.22 Simulated oscillator control voltages impacted by the perturbation.	50
Figure 4.1: Ring-oscillator architecture with N delay cells.	55
Figure 4.2: Ring-oscillator architecture with N = 3 delay cells.	55
Figure 4.3: Representation of a delay cell composed of a single-ended CMOS inverter.	56
Figure 4.4: Tuning strategies of a delay cell composed of a single-ended CMOS inverter.	56
Figure 4.5: FD-SOI MOS transistors technology: (a) LVT MOS cross section and (b) $V_T$ variation due to voltage body-biasing.	57
Figure 4.6: Peak injection representation and its effect on phase at zero crossing.	58
Figure 4.7: waveform and ISF representation of a typical ring oscillator.	58
Figure 4.8: Detailed waveform and ISF representation of a typical ring oscillator.	59
Figure 4.9: Pseudo-differential ring-oscillator architecture.	60

Figure 4.10: Pseudo-differential ring-oscillator architecture.	61
Figure 4.11: Pseudo-differential ring-oscillator architecture.	62
Figure 4.12: Layout of the pseudo-differential ring-oscillator and the regular ring oscillator architecture.	64
Figure 4.13: Chip photography (a) with (b) RVCOs localization and core area, (PRVCO up and inverter-based RVCO down).	64
Figure 4.14: Pseudo-Differential ring VCO measured and simulated Frequency range (a) versus body-biasing tuning under 1 V local supply and (b) measured coarse tuning range versus supply voltage under body-biasing configurations.	65
Figure 4.15: Inverter-based ring VCO measured and simulated Frequency range (a) versus body-biasing tuning under 1 V local supply and (b) measured coarse tuning range versus supply voltage under body-biasing configurations.	65
Figure 4.16: Measured and simulated phase noise for the PRVCO and the inverted-based RVCO architectures.	66
Figure 5.1: Caliper PLL architecture highlighting its innovative building blocks.	69
Figure 5.2: $N = 13$ Single-ended CMOS inverter-based Ring Oscillator topology.	70
Figure 5.3: Simulated RVCO <sub>1</sub> frequency tuning range versus body-biasing tuning (a) and (b) simulated RVCO <sub>1</sub> phase noise performance at 1 MHz offset frequency versus body-biasing tuning.	71
Figure 5.4: Classical mixer representation with digital input signals.	72
Figure 5.5: Proposed difference frequency mixer (DFM) circuit.	72
Figure 5.6: Simulated transient waveforms of the mixer input and output signals.	74
Figure 5.7: Simulated internal signals $S_1$ and $S_{QQ}$ waveforms and the mixer output signal.	75
Figure 5.8: Simulated divided-by-2 mixer output frequency under $f_1$ frequency variation.	76
Figure 5.9: Layout of the DFM prototype.	77
Figure 5.10: Measured DFM output spectrum for $f_1 = 1.496$ GHz and $f_2 = 546$ MHz.	78
Figure 5.11: Schematic representation of the digital mixer.	79
Figure 5.12: Transient simulation of the RVCOs and mixer (a) and (b) associated simulated performances.	79
Figure 5.13: General representation of a charge pump principle.	80
Figure 5.14: Current drift in transistor-based current source.	81
Figure 5.15: Proposed bootstrapped charge pump architecture.	82
Figure 5.16: Comparison between classical current source and the proposed bootstrapped current source	83
Figure 5.17: Simulated $i_N$ and $i_P$ current characteristics of the proposed charge pump.	84
Figure 5.18: $V_T$ dependent voltage reference architecture (a) and (b) Stable operating points of the voltage reference.	85
Figure 5.19: Simulated $V_{BIASN}$ and $V_{BIASP}$ voltages to verify the start-up circuit behaviour with the initial condition $V_{BIASN} = V_{BIASP} = 0$ V and $V_{DD} = 1$ V (a) and (b) $V_{BIASN} = V_{BIASP} = V_{DD} = 0$ V.	86
Figure 5.20: Bootstrapped charge pump schematic with all internal signals (a) and (b) the transient simulation of the implemented charge pump.	87
Figure 5.21: Schematic diagram of the positive-edge triggered tri-states comparator phase-frequency detector.	88
Figure 5.22: Schematic diagram of the phase-frequency detector.	88
Figure 5.23: Simulated PFD/CP characteristic.	89
Figure 5.24: Schematic diagram of the binary edge-counter frequency divider.	90
Figure 5.25: Transient simulation of the frequency divider for an input frequency of $f_{IN} = 1.496$ GHz, a divider ratio of 68 given an output frequency of $f_{DIV} = 22$ MHz.	90
Figure 5.26: Transimpedance low-pass filter topology.	91

Figure 5.27: Floorplan of the Caliper PLL detailing the location of each building block, the I/O pins, and the internal signals of the proposed PLL.	92
Figure 5.28: Layout representation of the primary loop RVCO <sub>1</sub> (a) and (b) secondary loop RVCO <sub>2</sub> .	93
Figure 5.29: Layout representation of the digital mixer.	94
Figure 5.30: Layout representation of the bootstrapped charge pump.	95
Figure 5.31: Transistor-level representation of the NMOS differential pair with active load (a) and (b) its layout representation.	96
Figure 5.32: Layout representation of the resistor inside the V <sub>T</sub> -dependent circuit.	96
Figure 5.33: Layout representation of the phase-frequency detector.	97
Figure 5.34: Layout representation of the digital frequency divider.	98
Figure 5.35: Layout representation of the primary loop filter.	99
Figure 5.36: Layout representation of the Caliper PLL.	101
Figure 5.37: Simulated output spectrum for a 2.420 GHz output frequency.	102
Figure 5.38: Simulated oscillator control voltages V <sub>CTRL1</sub> and V <sub>CTRL2</sub> .	103
Figure 5.39: Simulated Caliper PLL phase noise performance.	104
Figure 5.40: Layout representation of the Caliper PLL chip (a) and (b) an insert on the Caliper PLL active area.	104
Figure 6.1: Print circuit board of the Caliper PLL prototype.	107
Figure 6.2: Measurement set-up schematic (a) and (b) measurement set-up in the IMS Laboratory.	108
Figure 6.3: Phase noise comparison for a 440 MHz frequency between the Agilent E4400B signal generator (in black solid line) and the R&S SMT06 signal generator (in grey dot line).	109
Figure 6.4 Die photography of the proposed Caliper PLL with an insert on the PLL active area.	109
Figure 6.5: Measured power consumption of the Caliper PLL.	110
Figure 6.6: Measured frequency spectrum at a 2.420 GHz output frequency (Caliper PLL mode).	111
Figure 6.7: Measured frequency spectrum at a 2.420 GHz output frequency (full operation mode).	111
Figure 6.8: Measured reference spurs performance (at the offset frequency f <sub>IN1</sub> , internal frequency of the primary loop) over all the BLE channels.	112
Figure 6.9: Measured reference spurs performance at a 2.438 GHz output frequency for ten different tested chips (at the offset frequency f <sub>IN1</sub> , internal frequency of the primary loop).	113
Figure 6.10: Measured output phase noise for a 2.438 GHz output frequency.	113
Figure 6.11: Phase noise model of the proposed PLL representing the five main noise contributions (divider noises, oscillator noise and reference noise) compared with the measured output phase noise.	114
Figure 6.12: State-of-the-Art comparison: phase noise performance at 1 MHz offset frequency from the carrier versus power consumption.	116
Figure 6.13: State-of-the-Art comparison: rms jitter versus power consumption.	117
Figure 6.14: State-of-the-Art comparison: FoM jitter versus normalized area.	118
Figure 6.15: State-of-the-Art comparison: Normalized area versus power spending per frequency.	119
Figure 6.16: Compromise representation between the rms jitter, power spending per frequency and area.	119
Figure 7.1: Bootstrapped charge pump architecture (a), Simulated i <sub>N</sub> and i <sub>P</sub> current recovery through body-biasing under corner variation (b) and (c) under temperature variation for the typical corner.	126
Figure 7.2: Direct modulation representation of the 440 MHz reference frequency.	127
Figure A.1: Simple loop PLL phase domain model.	129
Figure A.2: General Laplace representation of a feedback system.	133
Figure B.1 : Caliper PLL phase domain model with the secondary loop-filter noise source.	135

Figure B.2 : Loop filter noise profile representation (a) and (b) Loop filter noise contribution.	136
Figure C.1: waveform and ISF representation of a typical ring oscillator.	137
Figure C.2: Detailed ISF representation.	138
Figure D.1: Down-converter Frequency mixer circuit	141

## List of Tables

Table 2A: Evolution of BLE Transceiver power consumptions.	15
Table 2B: Comparison with frequency synthesizer state-of-the-art around 2.4 GHz.	17
Table 2C: Comparison with State-of-the-Art frequency synthesizer around 2.4 GHz for IoT application	22
Table 3A: Caliper PLL characteristics compared with classical integer-N and fractional-N PLL architectures.	26
Table 3B: Laplace representations of open loop and closed-loop transfer functions.	28
Table 3C: Frequency shifts of the Caliper PLL architecture.	32
Table 3D: Noise phase transfer function of the Caliper PLL phase-domain model.	41
Table 3E: Caliper PLL parameters for the Simulink model.	47
Table 3F: Simulated Caliper PLL parameters from the transient simulation.	48
Table 4A: Transistor parameters of PRVCO and regular RVCO.	63
Table 4B: Performance summary and comparison with GHz-ring oscillator state-of-the-art.	66
Table 5A: Measured DFM frequency performance under input frequencies variation.	77
Table 5B: Component values of the primary loop filter and the secondary loop filter.	91
Table 5C: Variation of the primary loop filter components values.	100
Table 5D: Caliper PLL parameters for the transistor-level simulation.	103
Table 6A: Caliper PLL parameters.	110
Table 6B: Comparison with state-of-the-art Fractional-N PLL.	115
Table 6C: Reference classification of state-of-the-art Fractional-N PLL.	115



# 1 General Introduction

More than twenty billion connected devices are predicted in the coming years. Considering a world population of around eight billion people, it represents an average of three connected devices per person. This value is far from the reality due to the unequal access to these technologies. However, the Internet-of-Things (IoT) is a common reality in our day-to-day lives. Concerning a connected object, two critical parameters have to be taken into account: the power consumption has to be minimized to increase the battery-operated lifetime, and the cost of the object has to be as low as possible to ensure a successful mass deployment.

Sub-system of any transceiver, the frequency synthesis design is ruled by the same IoT challenges. Although today solutions provide a power consumption of around ten mW, Ultra Lower Power (ULP) solutions are more and more targeted. This virtuous goal brings the emergence of new innovative solutions. Realized in the frame of the common laboratory between STMicroelectronics and IMS Laboratory, this CIFRE thesis is targeting the following goals:

- Highlight the limitations of the actual frequency synthesizer architectures dedicated to IoT applications. From this study, the possible improvements are determined to address the IoT challenges.
- Propose a new frequency synthesis circuit implemented in 28nm FD-SOI technology. The specifications of this alternative solution are drawn to reach an optimum compromise in terms of power consumption, RF performances and silicon area.
- Support the ecosystem of the FD-SOI technology by using body-bias specific features. The proposed solution brings competitive advantages, only possible with the FD-SOI technology.

This manuscript is composed of seven chapters. This first one is dedicated to the general introduction with the presentation of the main goals and the outline of this thesis.

The second chapter reviews the trends and challenges of IoT frequency synthesizers. A first state-of-the-art valid at the beginning of the thesis highlights the performance of the actual IoT solutions, namely fractional-N PLL architecture. This

analysis determines in which innovative field our proposed PLL architecture takes place. Therefore, the thesis motivations are clearly exposed to propose a new IoT frequency synthesizer implemented in FD-SOI technology.

The third chapter introduces the proposed PLL architecture. Based on a dual-loop integer-N Offset-PLL topology, the proposed solution operates as a conventional fractional-N PLL without its complexity. Secondly, the theoretical study is performed with the stability study from the Laplace model, and a noise model is proposed. Then, the behavioral proof of concept of the proposed PLL is established by MATLAB Simulink model, designed for modeling dynamical systems.

The fourth chapter is focused on the study of Ring Voltage-Controlled Oscillators (RVCO) targeting the IoT application challenges presented in Chapter 2. The purpose of this chapter is to study how the FD-SOI technology can be used to achieve efficient RVCO topologies. In particular, frequency tuning method and phase noise study are discussed to lead to RVCO topology targeting IoT application.

The fifth chapter presents the design specifications of the proposed PLL architecture where innovative building blocks are introduced. ULP ring oscillator designs are presented showing a specific frequency tuning method enabled by body-biasing the transistors' back-gate. Secondly, a first fully digital Down-conversion Frequency Mixer (DFM) is proposed. The DFM does not require any extra selective passive filter, and it operates with quasi-quadrature inputs from the single-ended ring oscillators. Then, a bootstrapped charge pump architecture is presented. Based on a current control, the bootstrapped principle ensures constant operation over the PLL frequency range. Finally, the complete implementation of the proposed solution in 28nm FD-SOI is detailed. The top-level strategy and layout techniques of each PLL building block are explained to produce a robust and compact design.

The sixth chapter details the measurement results of the proposed PLL architecture. Proof of concept of the proposed solution is validated over the Bluetooth Low Energy frequency band (2.4 GHz to 2.48 GHz). Robustness to process variability is explored by performing die-to-die measurements. A comparison with an updated Ring-oscillator fractional-N PLLs state-of-the-art is provided. The proposed frequency synthesis achieves a state-of-the-art solution in FD-SOI technology, and it exhibits an industrial robustness scalable to other FD-SOI nodes.

The final chapter gives a general conclusion of this manuscript. Finally, research perspectives about our proposed solution are explored for future works.

# 2 Trends and Challenges of Internet of Things Frequency Synthesizer

## 2.1 Frequency synthesizer trends for Internet-of-Things application



Figure 2.1: Internet-of-Things domains of application.

In the following years, the market expectations predict more than 20 billion connected devices. These devices stand for the ambiguous term “Things” in “Internet-of-Things”. Based on [MOH\_19], these connected devices are composed of three elements:

- The physical product, composed of mechanical and electrical parts.
- Intelligence such as sensors or actuators coupled with embedded systems.
- A wired or wireless network to connect the product to the Internet.

For example, a “Thing” is a watch (Product) that monitors the heartbeat (Intelligence) and sends the data to the user account (Network). Some IoT domains are represented in Figure 2.1 to underline the main IoT strength: its coverage is everywhere. Most applications such as Smart Homes and Healthcare require devices powered by batteries. Representing the first challenge of IoT devices, these products have to present a low power consumption to expand the battery lifetime. The second challenge is related to the mass market of connected devices: the IoT products must have a small area to reduce the manufacturing costs.

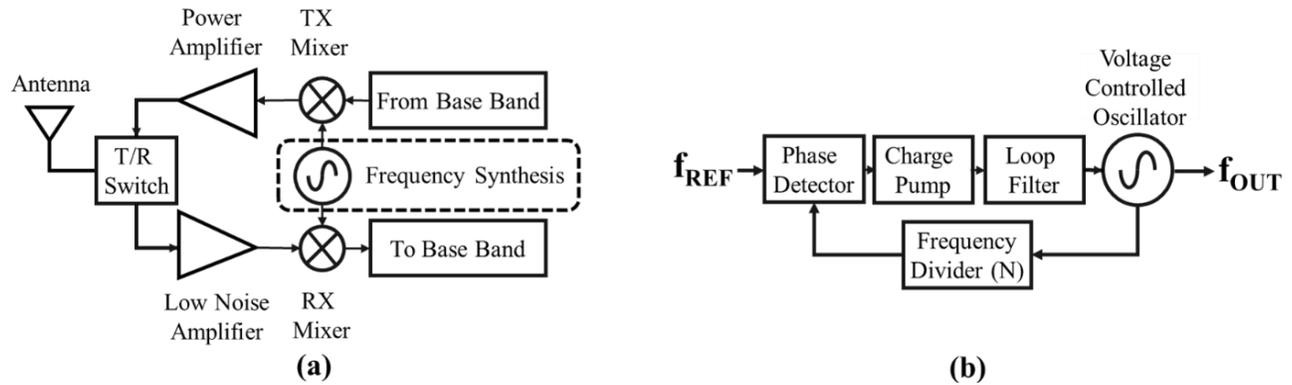


Figure 2.2: Block diagrams of a Transceiver (a) and PLL architecture (b).

In a connected device, the frequency synthesis unit is an essential element of every Radio-Frequency (RF) chain. As shown in Figure 2.2(a), a transceiver architecture using this sub-system ensures a stable frequency reference used in both transmitter (Tx) and receiver (Rx) modes. A control system is mandatory to ensure the precision and stability of a frequency synthesizer. The commonly used solution to provide a stable frequency is a Phase-Locked Loop (PLL) architecture represented in Figure 2.2(b). A PLL is a circuit synchronizing the phase of an output signal (with frequency  $f_{OUT}$ ) with a reference input signal (with frequency  $f_{REF}$ ). The phase synchronization also implies a synchronization of the two frequencies  $f_{OUT}$  and  $f_{REF}$ . The PLL architecture represented in Figure 2.2(b) gives the example with a divide-by-N frequency divider which establishes the relation  $f_{OUT} = N \cdot f_{REF}$ .

Reference	Power consumption		
	Frequency synthesis unit Pdc Freq (mW)	Rx architecture Pdc Tot(mW)	Pdc_Freq/Pdc_Tot ratio (%)
[KUO_17]	1.4	2.75	50.9
[DIN_18]	0.7	2.3	30.4
[ALG_20]	1.0	2.1	47.6
[TAM_20]	1.01	1.9	53.15

Table 2A: Evolution of BLE Transceiver power consumptions.

Among protocols dedicated to Internet-of-Things application (Wi-Fi, Zigbee, Z-wave [ALF\_15]), we are focusing on the Bluetooth Low Energy (BLE) standard [BLU\_19]. Composed of 40 channels of 2 MHz between 2.402 GHz and 2.480 GHz, the BLE standard is dedicated to short-range radio. It uses a low-power, short-range communications technology to operate for both a low-power and a longer time. Moreover, the BLE protocol shares common properties with the classic Bluetooth technology which allows manufacturers to design tiny dual-mode devices with a minimal production cost. As the BLE fits the two IoT challenges described before, this standard is a good candidate for IoT applications [DEC\_14].

The power consumptions of recent BLE transceivers are reported in Table 2A. While the total Rx power consumption is divided by 1.5 between 2017 and 2020, the frequency synthesis unit still occupies around half of the total power consumption. It highlights that power consumption is a critical parameter to be considered. Thus, the power consumption for a BLE frequency synthesizer is specified around 1 mW.

## 2.2 Frequency synthesizer state-of-the-art at the beginning of this work

	[HE_17]	[LIU_17]	[CHI_14]	[ELK_16]	[HUA_14]	[SHE_16]	[KON_16]
Oscillator Type	LC			Ring			
PLL Architecture	Fractional-N			Fractional-N		Integer-N	
Technology	40nm CMOS	40nm CMOS	40nm CMOS	65nm CMOS	40nm CMOS	14nm FinFET	45nm CMOS
Frequency Range (GHz)	1.8-2.5	1.7-2.7	2.1-2.7	2.0-5.5	N.A	0.8-4.0	2.0-3.0
Output Frequency <sup>a</sup> (GHz)	2.433	2.4	2.44	2.5	2.418	2.4	2.4
Ref Frequency (MHz)	32	32	32	50	26	19.2	22.6
Ref Spur (dBc)	-62	-66	-70	-44	-75	N.A	-65
RMS Jitter (ps)	1.98	0.72	1.71	3.6	3.29	2.99	0.97
Integ. range (Hz)	10k – 10M	10k – 100M	1k – 100M	10k – 100M	10k – 40M	100k – 600M	10k – 200M
Phase noise <sup>b</sup> (dBc/Hz)	-103	-109	-109	-91.5	-94.4	-105	-113.8
Supply voltage (V)	1	1	1	0.7	1.1	0.95	1
Power consumption (mW)	0.67	1.19	0.86	1.35	6.4	1.79	4
FOM Jitter <sup>c</sup> (dB)	-236.0	-234.6	-236.0	-227.6	-221.6	-227.9	-234.1
Area (mm <sup>2</sup> )	0.18	0.22	0.2	0.084	0.013	0.021	0.015

<sup>a</sup> All measured data is considered for the given output frequency

<sup>b</sup> Measured at 1 MHz offset frequency from the carrier.

<sup>c</sup> FOM Jitter =  $20 \log(\text{RMS Jitter}/1 \text{ s}) + 10 \log(\text{Power}/1 \text{ mW})$ .

Table 2B: Comparison with frequency synthesizer state-of-the-art around 2.4 GHz.

The purpose of this thesis is to review and analysis the IoT frequency synthesizers state of the art as of the beginning of this research work. Table 2B presents a summary of the most presentative publications at that time.

To get started, the choice of the oscillator topology is considered. Ring Oscillators (RO) take benefit of their digital nature to follow the technology node scaling to achieve small areas which is not the case for the LC oscillators. Indeed, all the reported LC-based frequency synthesizer present the highest areas among all references. Based on their compact topologies, ROs reduce the manufacturing cost and they are found more suitable for IoT applications. However, the RO phase noise performance must be considered. Indeed, RO topology presents generally more than 10 dB higher phase noise performance than the LC counterpart. Indeed, the reported LC-based PLL architectures achieve high RF performances to be considered as a possible solution for IoT frequency synthesizers.

Thus, RO-based PLL architectures have developed techniques to reach RF performance

fulfilling the IoT requirements. In particular, the oscillator phase noise behavior close to the carrier can be improved with a wideband PLL bandwidth. Both RO-based, the two integer-N PLL architectures in [SHE\_16] and [KON\_15] use this strategy to achieve performant phase noises due to a loop bandwidth around 10 MHz representing approximately a half of their respective  $f_{REF}$ . Thus, the RO phase noise performance gets close to the best reported LC-based PLL architecture in [CHI\_14] and [LIU\_17]. However, the RO phase noise performance is proportionally related to its power consumption. Consequently, by dedicating 75 % of its power budget for its free-running RO, [KON\_15] reaches the best phase noise performance among all the reported references at the cost of higher power consumption. However, a study in [CHE\_18] states that a phase noise performance of -90 dBc/Hz at 1 MHz offset from the carrier is enough with a 2 MHz PLL bandwidth to meet the BLE requirements.

The phase noise analysis highlights the trade-off between power consumption and RF performance in RO-based PLL architecture. This thesis targets a sub-mW power consumption to challenge the best-in-class LC-based PLL architectures. Thus, dealing with a limited power budget, the chosen strategy of this thesis is to study a RO-based wideband PLL bandwidth frequency synthesizer fulfilling the IoT requirements.

The last point to be considered is the choice between integer-N and fractional-N PLL architectures. Integer-N architecture shows a frequency resolution equals to the reference frequency  $f_{REF}$ . Thus, the need for a fine frequency resolution reduces both the reference frequency and the PLL bandwidth. Consequently, the reduced PLL bandwidth limits the improvement of the phase noise behavior close to the carrier. Thus, classical integer-N PLL is not a suitable option for a RO-based wideband PLL dedicated to IoT applications.

However, the frequency resolution of fractional-N PLL architecture is expressed as a portion of the reference frequency. Thus, fractional-N PLL can achieve both a fine frequency resolution and a wide PLL bandwidth [RIL\_93] [VEN\_13]. This specification makes the fractional-N PLL the commonly used solution in frequency synthesis. In particular, the reported RO-based fractional-N PLL [ELK\_16] and [HUA\_14] achieve a wide PLL bandwidth to improve the RO phase noise.

The fine frequency resolution is created by a specific system named delta-sigma modulator (DSM), this system introduces quantization noise in the PLL output phase noise. Furthermore, the quantization noise becomes dominant as the PLL bandwidth is increased. Thus, noise cancellation technique is used in [HUA\_14] to reduce the DSM quantization noise without sacrificing the PLL bandwidth. However, each technique implies additional circuitry with extra area and power consumption, thereby challenging their use in IoT applications.

Considering all these concerns, the chosen strategy for this thesis work is to study a low-power RO-based integer-N PLL architecture achieving both a wideband PLL bandwidth and a small frequency solution.

## 2.3 Review of bandwidth versus channel spacing trade-offs in PLLs

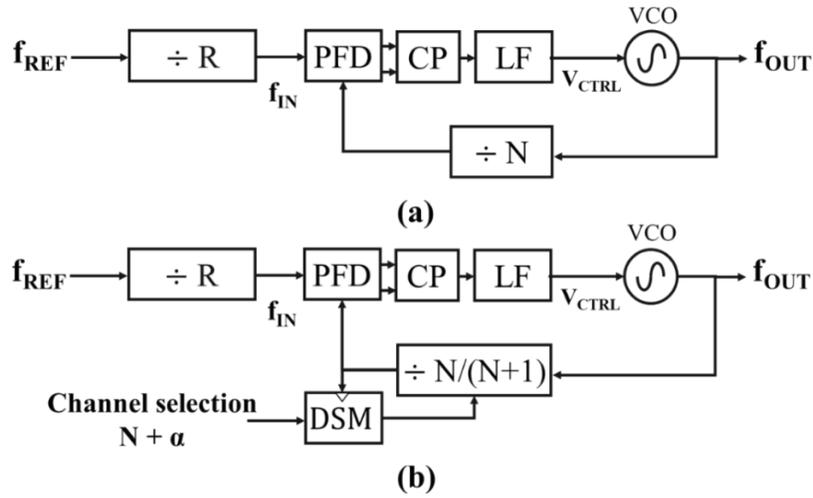


Figure 2.3: Block diagram for conventional integer-N (a) and fractional-N PLL (b).

Conventional integer-N and fractional-N PLL architectures are represented in Figure 2.3. We consider here a first out of the loop frequency division block by  $R$  such as:  $f_{IN} = f_{REF}/R$ . We suppose that each PLL architecture is a conventional charge pump PLL topology composed of a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage-controlled oscillator (VCO), and a feedback divider (by  $N$  or by  $N/(N+1)$ ).

The phase noise performances of the integer-N and fractional-N PLL architectures are compared in Figure 2.4, as we suppose a narrow bandwidth ( $f_{BW} = 200$  kHz) and a wide bandwidth ( $f_{BW} = 2$  MHz). Normally, the PLL bandwidth is chosen to be less than a tenth of the internal frequency  $f_{IN}$ , to ensure that the PLL is locked on the internal reference frequency. As illustrated in Figures 2.4(b) and 2.4(d), a wide bandwidth reduces the VCO phase noise making possible the desired use of ring-oscillators as explained previously for the IoT applications.

Integer-N PLL synthesizes output frequency  $f_{OUT}$  as an integer multiple ( $N$ ) of the internal frequency  $f_{IN}$ . Thus, the frequency resolution ( $\Delta f_{OUT}$ ) is directly correlated to the internal frequency  $f_{IN}$ , implying  $\Delta f_{OUT} = f_{IN}$ . Thus, a small frequency resolution involves a small PLL bandwidth to suppress the VCO noise. It represents the first trade-off between the PLL bandwidth and the channel spacing which is one of the major issues for using integer-N PLL architecture for narrow-channel applications.

In a fractional-N PLL, the output frequency  $f_{OUT}$  is divided by a non-integer value  $N + \alpha$ , where  $\alpha < 1$ . The output frequency resolution  $\Delta f_{OUT}$  is then achieved by varying the  $\alpha$  value to imply  $\Delta f_{OUT} = \alpha \cdot f_{IN}$ . Thus, the internal frequency and the frequency resolution are no longer constrained to be equal. A narrow channel spacing is achieved for the same internal frequency  $f_{IN}$  leading to a wider PLL bandwidth than integer-N PLL architecture. Most IoT frequency synthesizers have adopted the fractional-N architecture solving the first trade-off between the PLL bandwidth and the frequency resolution.

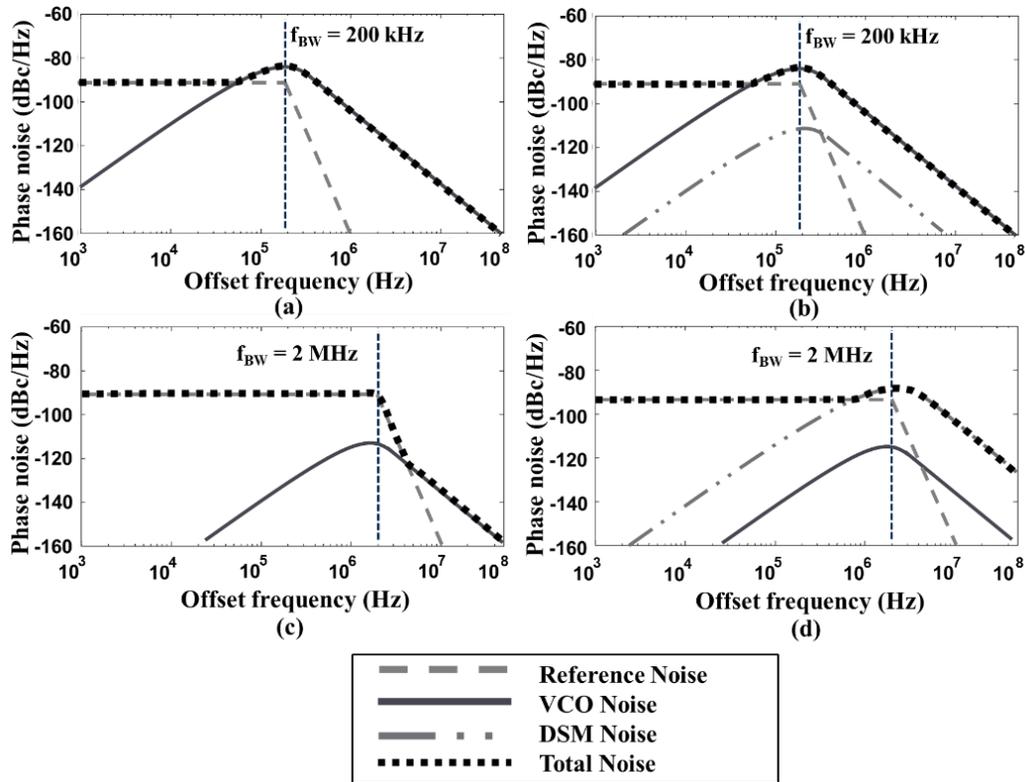


Figure 2.4: Phase noise profile of integer-N PLL and fractional-N PLL for narrow PLL bandwidth (a and c) and wide PLL bandwidth (b and d).

However, fractional-N PLLs suffer from several drawbacks caused by the fractional divider. For example, a dual modulus divider ( $N/N+1$ ) which divides 50% of the oscillator period by  $N$  and 50% of the oscillator period by  $N+1$  creates an average division ratio of  $N+1/2$ . The difference between the instantaneous divider value ( $N$  or  $N+1$ ) and the average divider value ( $N+1/2$ ) introduces quantization errors in the fractional-N PLL. The periodicity of the quantization errors creates fractional spurs hence increasing the output phase noise. A high-order delta-sigma modulator (DSM) is then used to break the periodicity of the division pattern in order to reduce the output phase noise and the fractional spurs.

The trade-off between quantization noise and PLL bandwidth is crucial for fractional-N PLL. Contrary to the VCO noise, the quantization noise is not suppressed by a wide PLL bandwidth as represented in Figure 2.4. Indeed, an expanded PLL bandwidth leads to a higher quantization noise contribution which dominates the high offset frequencies. This noise can be suppressed by a narrow PLL bandwidth wasting the benefit of the VCO noise suppression. To cope with these imperfections, recent solutions are proposing a high-order DSM combined with techniques as finite-impulse-response (FIR) [YU\_09] or Space-Time Averaging (STA) [ZHA\_20]. These solutions improve the noise performance at the cost of higher power consumption, design complexity, and Silicon area.

This review confirms the PLL specifications from the state-of-the-art analysis. The chosen strategy for this thesis work is to reach another type of compromise between PLL bandwidth, frequency resolution, and noise contribution.

## 2.4 Conclusion: Motivation of this thesis



Figure 2.5: Proposed frequency synthesizer to fulfill Internet-of-Things application.

Through this section, the main challenges of an IoT frequency synthesizer have been settled: achieving both low power consumption and a small area while fulfilling IoT protocol specifications, for example, those from Bluetooth Low Energy (BLE). Illustrated in Figure 2.5, the purpose of this thesis is to propose a frequency synthesizer that meets the IoT requirements.

The proposed frequency synthesizer is based on specific advantages of the UTBB FD-SOI technology from STMicroelectronics to acquire both low power consumption and low cost [CAT\_17]. Low power consumption is ensured using a digital paradigm. Because the 28nm FD-SOI CMOS technology provides digital circuits with a very low power consumption [CLE\_20], the frequency synthesizer is mostly based on digital building blocks. Low cost is ensured both by an industrial robustness and by reducing the silicon footprint of the synthesizer. It implies avoiding the use of an LC-oscillator since the latter occupies a large area regardless of the technological node is taking advantage of. These points yield to an inductorless VCO represented by a Ring Oscillator (RO).

However, such an oscillator is known for having a bad phase noise, especially for close-in frequencies from the carrier. Thus, it is mandatory to implement a wideband frequency synthesizer to tackle this issue. To fulfill ULP IoT applications, an integer-N PLL architecture is hence proposed with a wide PLL bandwidth to improve RO phase noise behavior close to the carrier without the complexity of fractional division.

<b>Targeted specifications for IoT frequency synthesizer</b>	
Technology	28nm FD-SOI CMOS
Oscillator type	Ring
PLL architecture	Integer-N
Power consumption (mW)	< 1 mW
PLL bandwidth	> 2 MHz
Phase noise at 1 MHz offset frequency (dBc/Hz)	< -90
FOM Jitter (dB)	< -230
Area (mm <sup>2</sup> )	< 0.03

Table 2C: Comparison with State-of-the-Art frequency synthesizer around 2.4 GHz for IoT application.

Research in the domain of frequency synthesis is moving fast. Thus, a first state-of-the-art at the beginning of the thesis has been discussed in this chapter to determine the PLL specifications of the thesis work. Therefore, these specifications are summarized in Table 2C, and they represent the thesis goals to improve the state-of-the-art of ULP IoT frequency synthesizers. The chosen strategy is to use the specific advantages of the FD-SOI technology to reach high PLL performance with an optimum compromise between the power consumption and the circuit area.

Measured performances of the proposed frequency synthesizer studied in this thesis are compared in a complete state-of-the-art that has emerged during the thesis work. Nevertheless, the recent PLL architectures presented in the novel state-of-the-art have followed the same trends presented in this chapter in terms of low power consumption and low area while achieving high RF performance.

To sum up, this thesis aims to propose an IoT frequency synthesizer that reaches another type of compromise between PLL bandwidth, frequency resolution, noise contribution, power consumption, and silicon area.

# 3 Proposed Dual-loop Integer-N PLL: Caliper PLL Architecture

## 3.1 Introduction

This chapter introduces the study of the proposed Caliper PLL architecture. Based on a dual-loop integer-N topology with a common reference frequency, the features of the proposed solution are presented. In particular, the output frequency relation and the achievable frequency resolutions are discussed. One frequency resolution is tuned using a difference frequency of the two internal loop frequencies. Due to the “Caliper effect” of the proposed architecture, the PLL shows an expanded PLL bandwidth which improves the oscillator noise behavior close to the carrier. The Caliper PLL characteristics are discussed in this section, a comparison between conventional integer-N and fractional-N PLL architectures is drawn in order to highlight the advantages of the Caliper PLL. The proposed solution operates as a conventional fractional-N without its complexity.

The second part of this chapter is focused on the stability analysis of the Caliper PLL. The study uses the Laplace representation in the phase-domain to compute the open-loop phase margin of the Caliper PLL. From this computation, the PLL stability is ensured by the sizing of the loop parameters. The multiple trade-offs involved in the stability study are discussed to achieve a wideband PLL bandwidth.

The third part of this chapter is dedicated to the noise analysis of the Caliper PLL. A phase noise model is presented. Based on the noise transfer functions, the noise computes the intrinsic noise source of each PLL building block in the output phase noise of the Caliper PLL. The total phase noise and the contributions of each PLL building block are detailed. The main noise contributors are determined, and the output phase noise computed by the model is discussed. The noise analysis determines which PLL building blocks and which loop parameters can be optimized to improve the overall PLL performance.

The final part of this chapter demonstrates in simulation the behavioral proof of concept of the Caliper PLL. Using the loop parameters computed in the stability analysis, the Caliper PLL is simulated as a dynamical system. Output frequency relation and the output frequency resolution are verified with this model. The behavioral proof of concept validates the functionality of the proposed Caliper PLL architecture.

## 3.2 Caliper PLL architecture

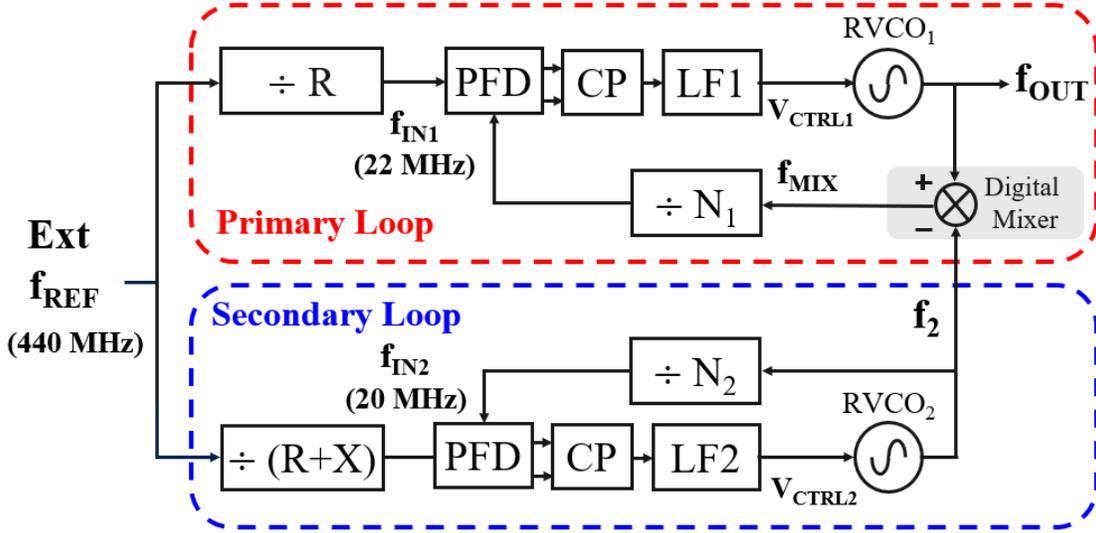


Figure 3.1: Detailed block diagram of the proposed Caliper PLL architecture.

The proposed frequency synthesizer is based on a dual loop PLL topology as illustrated in Figure 3.1. Each loop represents an integer- $N$  third-order charge pump PLL. The external common reference frequency  $f_{REF}$  is divided by two integer frequency dividers  $R$  and  $R+X$  respectively. Thus, the primary loop runs at the internal frequency  $f_{IN1} = f_{REF}/R$  to generate the output frequency  $f_{OUT}$  while the secondary loop runs at the internal frequency  $f_{IN2} = f_{REF}/(R+X)$  to produce its output frequency  $f_2$ .

The two loops are combined into an Offset PLL topology (OPLL). The output signals of frequency respectively  $f_{OUT}$  and  $f_2$  are mixed together to recover the signal  $f_{MIX}$  with a frequency of  $f_{OUT} - f_2$ . This signal  $f_{MIX}$  is then propagated in the feedback path of the primary loop. Contrary to a classical OPLL, the phenomenon of injection pulling [RAZ\_04] between the two oscillator frequencies is here avoided because the two internal frequencies  $f_{IN1}$  and  $f_{IN2}$  are already synchronized with the same reference frequency  $f_{REF}$ .

The interesting association of the OPLL topology and the dual loop architecture with a common reference frequency  $f_{REF}$  provides the output frequency  $f_{OUT}$  as a combination of the two internal frequencies  $f_{IN1}$  and  $f_{IN2}$  as:

$$f_{OUT} = f_{IN1} \cdot N_1 + f_{IN2} \cdot N_2 = f_{REF} \cdot \left( \frac{N_1}{R} + \frac{N_2}{R+X} \right) \quad (3.1)$$

where  $N_1$  and  $N_2$  are respectively the integer values of the feedback loop dividers, and  $R$  and  $R+X$  are the integer values of input dividers as represented in Figure 3.1.

Three achievable output frequency resolutions  $\Delta f_{OUT}$  may be reached with the proposed PLL topology. Focusing on only the primary loop, an increment/decrement of the divide-by- $N_1$  feedback frequency divider while keeping constant the divide-by- $N_2$  feedback frequency divider,

implies an output frequency resolution of  $\Delta f_{\text{OUT}} = f_{\text{IN1}} = f_{\text{REF}}/R$ . It represents the integer-N PLL mode with the usual channel spacing of a classical integer-N PLL.

Regarding only the secondary loop, an increment/decrement of the divide-by- $N_2$  feedback frequency divider while keeping constant the divide-by- $N_1$  feedback frequency divider, implies an output frequency resolution of  $\Delta f_{\text{OUT}} = f_{\text{IN2}} = f_{\text{REF}}/(R+X)$ . It represents here the Offset-PLL mode with the usual output channel spacing of a classical OPLL.

Concerning the overall PLL architecture, another output frequency resolution  $\Delta f_{\text{OUT}}$  is achievable. Both feedback frequency dividers ( $N_1$  and  $N_2$ ) can simultaneously be incremented and decremented while respecting the following relation:

$$\forall (N_1, N_2) \in \mathbb{N}^2, N_1 + N_2 = k \in \mathbb{N} \quad (3.2)$$

Where  $k$  is a constant integer. Hence, each increment of  $N_1$  implies a decrement of  $N_2$ . Thus, the output frequency resolution of the proposed PLL architecture is then achieved by the difference of the two internal frequencies as:

$$\Delta f_{\text{OUT}} = f_{\text{IN1}} - f_{\text{IN2}} = f_{\text{REF}} \cdot \left( \frac{X}{R \cdot (R + X)} \right) \quad (3.3)$$

Thus, the frequency resolution  $\Delta f_{\text{OUT}}$  is achieved by the proposed PLL architecture and only depends on a proper choice of the two internal loop frequencies  $f_{\text{IN1}} = f_{\text{REF}}/R$  and  $f_{\text{IN2}} = f_{\text{REF}}/(R+X)$ . Moreover, the fine frequency resolution is defined by the choice of the common reference frequency  $f_{\text{REF}}$  and the two input frequency divider values  $R$  and  $R+X$ . As the output frequency resolution  $\Delta f_{\text{OUT}}$  is tuned using a frequency difference of the two internal frequencies  $f_{\text{IN1}}$  and  $f_{\text{IN2}}$ , we propose the name of Caliper PLL for this topology.

The proposed PLL architecture overcomes the trade-off between the frequency resolution and the PLL bandwidth. Compared with an integer-N PLL with the same internal frequency  $f_{\text{IN1}}$  and the same PLL bandwidth of a tenth of  $f_{\text{IN1}}$ , the proposed PLL frequency resolution  $\Delta f_{\text{OUT}}$  is  $(R+X)/X$  times smaller. Consequently, for the same frequency resolution  $\Delta f_{\text{OUT}}$ , the proposed PLL offers a larger PLL bandwidth than classical integer-N PLL. The expanded PLL bandwidth is due to the ‘‘Caliper effect’’ of the proposed architecture, permitting to reduce the settling time of the loop and improving the VCO phase noise behavior close to the carrier.

Thus, the frequency resolution of the proposed PLL is no longer only due to the internal frequency  $f_{\text{IN}}$ . This property is also shared with the fractional-N PLL by using a Delta-Sigma Modulator (DSM). However, a high order DSM is usually used to reach high spectral purity and phase noise performance. Moreover, a high order DSM is already power and area-consuming without considering the stability issues introduced by a high-order DSM. Further techniques to improve the overall phase noise performance would increase even more the Silicon area and the power consumption of the fractional-N PLL.

The proposed Caliper PLL is hence a dual loop integer-N PLL architecture which shares the same properties as of a fractional-N PLL in terms of frequency resolution and PLL bandwidth. However, the proposed PLL achieves this fine frequency resolution only based on its architectural nature. Thus, no additional circuitry is needed to improve the overall phase noise performance and spectral purity of the system, the proposed PLL aims to target a sub-mW power consumption and a reduced Silicon area suitable for IoT applications.

	<b>Integer-N PLL</b>	<b>Fractional-N PLL</b>	<b>Caliper PLL</b>
For the same internal frequency $f_{IN}$ and same technology node			
Complexity	Single loop with integer divider	Single loop with fractional divider (DSM)	Dual loop with integer dividers
$\Delta f_{OUT}$	$\Delta f_{OUT} = f_{IN}$	$\Delta f_{OUT} < f_{IN}$	$\Delta f_{OUT} < f_{IN}$
PLL BW	$f_{BW} < f_{IN}/10$	$f_{BW} > f_{IN}/10$	$f_{BW} > f_{IN}/10$
Out-of-band phase noise	RO phase noise	DSM phase noise	RO phase noise
Spurious	Reference spurs	Reference and fractional spurs	Reference and offset spurs
Power consumption	$P_{DC} > 1mW$	$P_{DC} > 1mW$	$P_{DC} < 1mW$
Area	$< 0.03 \text{ mm}^2$	$> 0.03 \text{ mm}^2$	$< 0.03 \text{ mm}^2$

Table 3A: Caliper PLL characteristics compared with classical integer-N and fractional-N PLL architectures.

Represented in Table 3A, the proposed Caliper PLL characteristics are compared with the integer-N and fractional-N PLL architectures under the scope of IoT applications. The Caliper PLL architecture shares common properties with classical fractional-N PLL such as a narrow frequency resolution  $\Delta f_{OUT}$  and a wide PLL bandwidth. As an integer-N PLL, the out-of-band phase noise of the Caliper PLL is only composed of the ring oscillator phase noise. Contrary to fractional-N PLL where the PLL bandwidth has to be limited to reduce the DSM phase noise, the Caliper PLL fully exploits the wide PLL bandwidth without impacting the out-band phase noise performance. The wide PLL bandwidth improves the phase noise behavior close to the carrier, enabling the use of ring oscillators to target a compact frequency synthesizer.

Moreover, the phase noise and the spurs performances of a fractional-N PLL are directly linked to the power consumption of the DSM. Only based on a dual loop architecture combined into an Offset PLL topology, the proposed Caliper PLL can achieve a low power consumption compliant with IoT applications. Thus, the Caliper PLL proposes an alternative to fractional-N PLL for IoT applications.

### 3.3 Laplace Model of Caliper PLL architecture

#### 3.3.1 Caliper PLL phase-domain model

In this section, a phase-domain model of the PLL architecture is presented to determine the stability of the loop. The stability analysis is crucial especially as it is not trivial in the dual-loop topology of the Caliper PLL. Even if the phase-domain model is used to both determine the PLL parameters and ensure the PLL stability, the behavioral proof of concept is established by dynamical simulation.

Based on the small-signal approximation [HAN\_14], the linear model assumes that the PLL is locked in its steady-state and that it remains locked against weak variations of phase or frequency. Even if this model presents limitations due to its linearity, it is the most used to draw a first-order approximation of the system [BES\_07]. This mathematical model computes a phase-transfer function  $H_{CL}(p)$ , which relates the Laplace transforms  $\theta_{REF}(p)$  and  $\theta_{OUT}(p)$  of the phase signals  $\theta_{REF}(t)$  and  $\theta_{OUT}(t)$ . The Laplace representation of the Caliper PLL details the transfer function of each individual building block as illustrated in Figure 3.2. Limitations of the Laplace model are other reasons to verify the PLL stability and the PLL parameters sizing by a behavioral proof of concept which is presented at the end of this chapter.

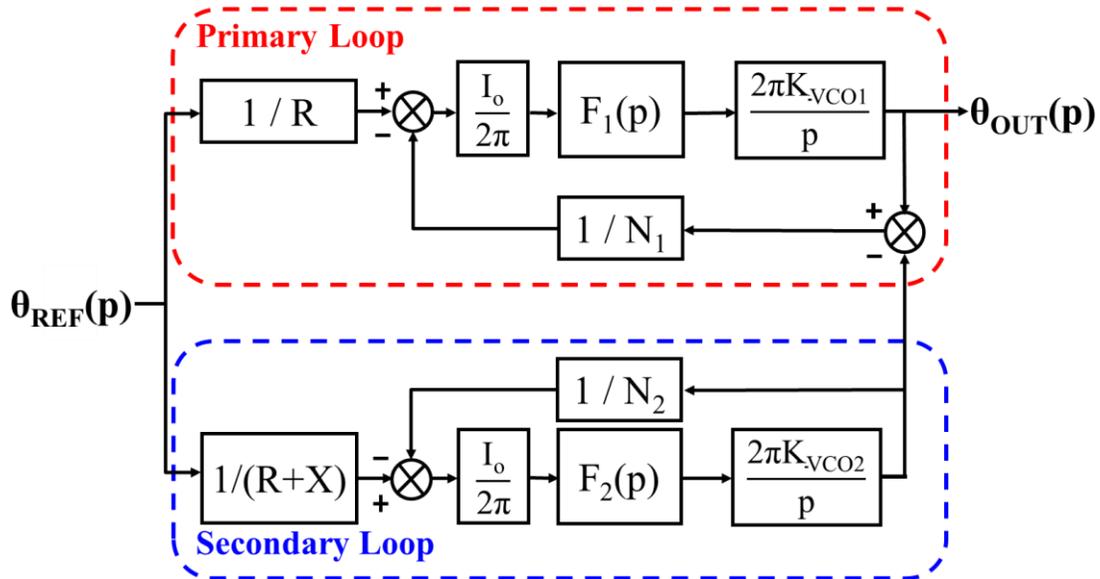


Figure 3.2: Caliper PLL Laplace model.

The combination of the phase/frequency detector and the charge pump is modeled by a gain of  $I_o/(2\pi)$ , relating the proportional current output with the input phase difference. The loop-filter is represented by its correspondent Laplace transfer-function  $F(p)$  and the oscillator by an integrator with a gain of  $2\pi K_{VCO}$ , where  $K_{VCO}$  is the oscillator gain in Hz/V. Finally, each divide-by- $N$  counter is modeled by a gain block of  $1/N$ .

Thus, the overall PLL Laplace representation can be computed. The Caliper PLL is composed of two third-order single loop PLLs in an offset-PLL topology. For clarity purpose, each single loop transfer-function is represented in Table 3B, where  $H_{OL}(p)$  and  $H_{CL}(p)$  represent respectively the open-loop and closed-loop transfer functions.

	Open-loop transfer function	Closed-loop transfer function
Primary loop	$H_{OL1}(p) = \frac{I_o}{2\pi} \cdot F_1(p) \cdot \frac{2\pi K_{VCO1}}{p} \cdot \frac{1}{N_1}$	$H_{CL1}(p) = \frac{N_1}{R} \cdot \frac{H_{OL1}(p)}{1 + H_{OL1}(p)}$
Secondary loop	$H_{OL2}(p) = \frac{I_o}{2\pi} \cdot F_2(p) \cdot \frac{2\pi K_{VCO2}}{p} \cdot \frac{1}{N_2}$	$H_{CL2}(p) = \frac{N_2}{R+X} \cdot \frac{H_{OL2}(p)}{1 + H_{OL2}(p)}$
Caliper loop	$H_{OL}(p) = H_{OL1}(p) + H_{OL2}(p) + H_{OL1}(p) \cdot H_{OL2}(p)$	$H_{CL}(p) = H_{CL1}(p) \cdot \left( 1 + \left( \frac{R}{N_1} \right) \cdot H_{CL2}(p) \right)$

Table 3B: Laplace representations of open loop and closed-loop transfer functions.

Based on the expression of the overall PLL closed-loop function, the proposed PLL is a sixth-order PLL. An expression for the open-loop transfer function is needed to define the system parameters and therefore, fulfill the phase margin requirement of the overall system. In Appendix A, the derivation of an analytical expression of the overall open-loop transfer function carries significant difficulties. Hence, the chosen strategy is to consider each single loop independently to express the phase margin and the loop parameters. Using the superposition theorem, the phase margin of the overall system is checked on the Bode representation of the closed-loop transfer function.

### 3.3.2 Open Loop parameter sizing

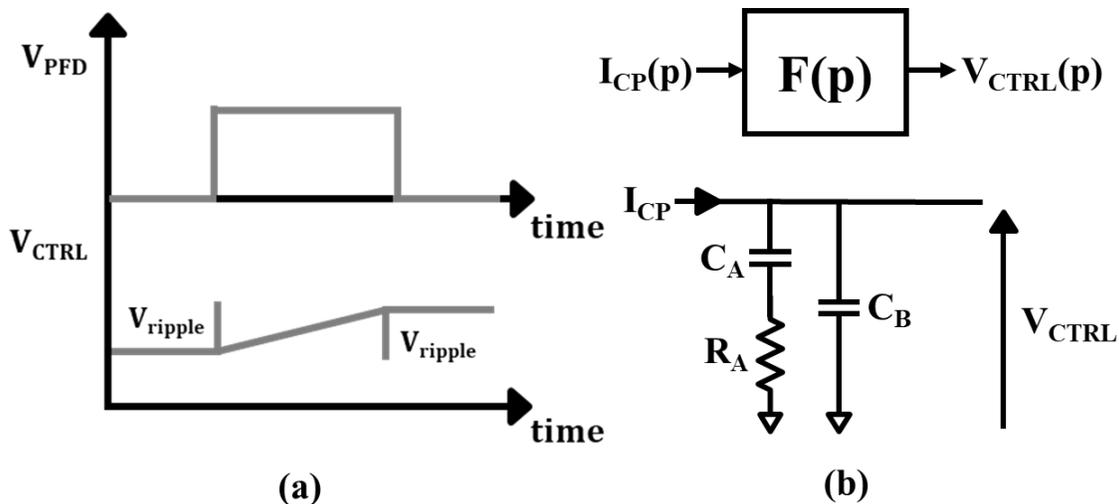


Figure 3.3 Representation of ripple effect due to the PFD pulse (a), and (b) Laplace representation of the second order transconductance filter topology.

The filter is a determinant building block, since it gives the average voltage value according to the output charge pump activity which is proportional to the phase error  $\theta_e$  and it filters out the

remaining terms of internal harmonics. These high-frequency signals are unwanted, so they are suppressed by a low-pass filter topology. The chosen filter is a second-order transconductance topology presented in Figure 3.3(b). At its first branch, the filter is composed of a resistor  $R_A$  with a capacitor  $C_A$  in series. As represented in Figure 3.3(a), the charge pump current source and the capacitor  $C_A$  form an integrator in the loop and the resistor causes a positive voltage ripple of value  $I_{CP} \cdot R_A$  at the start of each PFD pulse. At the end of the pulse, a negative ripple of equal value occurs. This ripple modulates the VCO frequency and introduces excessive jitter to the output. Hence, a small capacitor  $C_B$  is added in parallel with the  $R_A$  and  $C_A$  branch to suppress the ripple. However, adding this capacitor generates a pole, which increases the order of the system to three. Therefore, the phase degradation due to this pole must be accounted for sizing a proper choice of the other loop parameters. Furthermore, the loop filter component values ( $R_A$ ,  $C_A$ , and  $C_B$ ) should be small enough to allow the integration of the two loop filters within the PLL circuit. Thus, this constraint is taken into consideration during the PLL stability analysis.

The loop stability is determined by the open-loop phase margin criterion. The computation of the open-loop phase margin becomes an issue at higher order PLLs. It is another motivation to consider each third-order single-loop PLL independently. The open-loop phase margin also sets over architectural parameters of the loop such as the natural frequency  $\omega_n$  and the damping factor  $\xi$ . Finally, the Caliper PLL targets a wide PLL bandwidth to improve VCO behavior close to the carrier. Thus, the trade-off between bandwidth and stability is also considered during the PLL stability study.

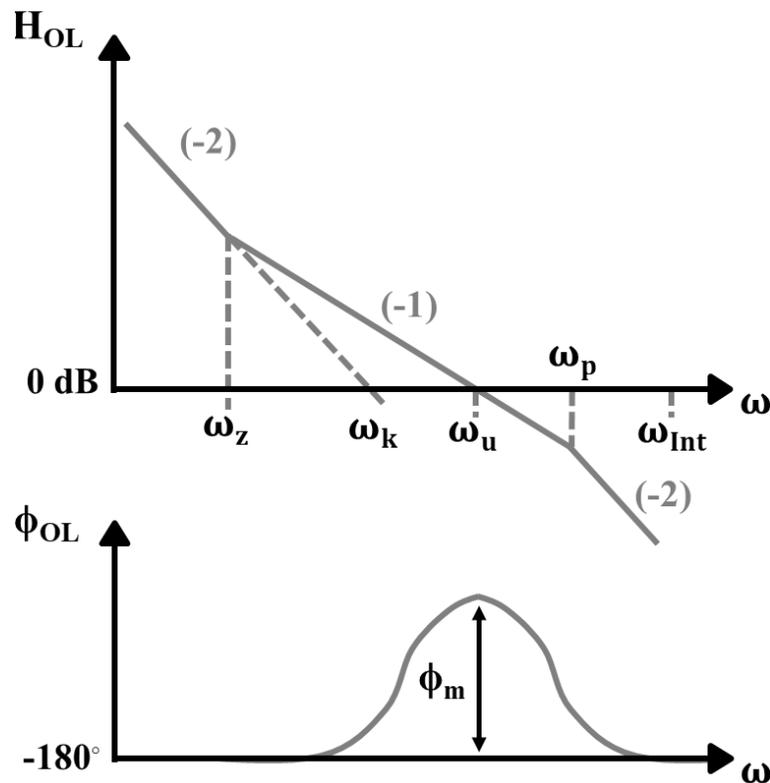


Figure 3.4 Open-loop pulsation scalabing

The transfer function of the filter is expressed as:

$$F(p) = \frac{1}{p} \frac{p + \omega_z}{C_B(p + \omega_p)} \quad (3.4)$$

with  $\omega_z = \frac{1}{R_A C_A}$ ;  $\omega_p = \frac{1}{R_A} \left( \frac{1}{C_A} + \frac{1}{C_B} \right)$  the zero and the pole of the filter respectively.

Thus, the open-loop transfer function of third-order single loop PLL represented in Figure 3.4 is also written as:

$$H_{OL}(p) = \left( \frac{\omega_k}{p} \right)^2 \cdot \frac{1 + \frac{p}{\omega_z}}{1 + \frac{p}{\omega_p}} \quad (3.5)$$

where the third pulsation  $\omega_k$  is here expressed as  $\omega_k = \sqrt{\frac{K_{VCO} I_o}{N(C_A + C_B)}}$

Considering the unity-gain pulsation  $\omega_u$  when  $|H_{OL}(p)|=1$ , the phase margin is expressed as:

$$\phi_m = \arg (H_{OL}(j\omega_u)) \quad (3.6)$$

The optimal value is set at 45 degrees. However, to guarantee a good trade-off between stability and settling time, the phase margin  $\phi_m$  is between the range of 30 to 60 degrees. Considering this maximum value of  $\phi_m$ , computation on the phase margin is proceeded. As detailed in Appendix A, a logarithmic relation between  $\omega_z$  and  $\omega_p$  pulsation is given as:

$$\omega_u = \sqrt{\omega_z \cdot \omega_p} = \omega_z \cdot k = \frac{\omega_p}{k} \quad (3.7)$$

The k-parameter can also be expressed by the  $C_A$  over  $C_B$  ratio and by the phase margin as:

$$k = \sqrt{1 + \frac{C_A}{C_B}} = \sqrt{\frac{1 + \sin(\phi_m)}{1 - \sin(\phi_m)}} \quad (3.8)$$

Thus, the pulsation  $\omega_p$  is chosen according to the internal loop pulsation  $\omega_{int}$ . To ensure a linear approximation of the model, a first approximation of  $\omega_p = \omega_{int}/4$ , allows to scale a bandwidth around a tenth of the internal frequency. The targeted phase margin allows to fix the other pulsation  $\omega_z$  and the relation between the two capacitances  $C_A$  and  $C_B$ . This last pulsation  $\omega_k$  represents the trade-off between the stability sizing and the system parameters  $K_{VCO}$ ,  $I_o$ , and  $N$ .

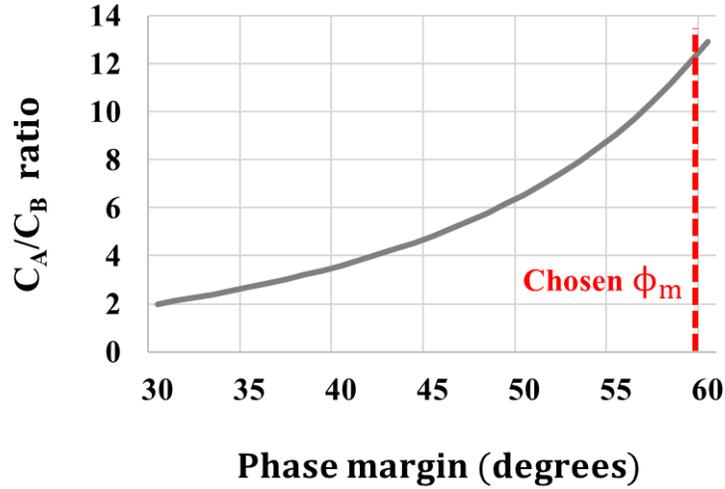


Figure 3.5: Loop-filter capacitance ratio versus open-loop phase margin.

The Figure 3.5 represents the capacitance ratio function of the targeted open-loop phase margin. A phase margin of 60 degrees is chosen to calculate the open-loop and closed-loop transfer functions ensuring their stability. The filter expression approximated by  $C_A \gg C_B$  gives:

$$F_A(p) = \frac{1}{p C_A} (p + \omega_z) \quad (3.9)$$

It enables to express an associated closed-loop transfer function:

$$H_{CLA}(p) = \frac{NUM(p)}{DEN(p)} \quad (3.10)$$

where the denominator expression has the canonical form:

$$DEN(p) = p^2 + 2\xi\omega_n p + \omega_n^2 \quad (3.11)$$

with:

$$\omega_n = \sqrt{\frac{K_{VCO} \cdot I_o}{N \cdot C_A}} ; \xi = \frac{\omega_n}{2 \cdot \omega_z} \quad (3.12)$$

It allows to verify the scalation of the filter components to target at least an underdamped response corresponding to a damping factor of  $0 < \xi < 1$ . The phase margin, the input frequency scalation and the damping factor calculation gives all the relations to size the parameters of the loop. The oscillator gain  $K_{VCO}$ , the output frequency  $f_{OUT}$ , the frequency divider value  $N$  and the internal frequency  $\omega_{INT}$  are determined by the communication protocol dedicated by the PLL. From the filter topology, the phase margin expression gives the relation between the capacitor values and the pole and zero expression of the filter. Finally, the damping factor expression gives another relation between the loop parameters to verify the stability of the overall system.

### 3.3.3 Caliper PLL frequencies sizing

This section is dedicated to the sizing of the frequencies involved inside the Caliper PLL: the common reference frequency  $f_{REF}$ , the two internal frequencies  $f_{IN1}$  and  $f_{IN2}$ , and the output frequency step  $\Delta f_{OUT}$ . Focusing on IoT applications, the proposed PLL architecture targets an output frequency resolution  $\Delta f_{OUT}$  of 2 MHz which suits the channel spacing of the Bluetooth Low Energy (BLE) specifications (2.4 to 2.48 GHz) [BLU\_19]. Consequently, a reference frequency of  $f_{REF} = 440$  MHz is chosen and implies input frequency divider values of  $R = 20$  and  $R+X = 22$  to generate the primary loop and secondary loop internal frequencies of respectively  $f_{IN1} = 22$  MHz and  $f_{IN2} = 20$  MHz. To summarize, the Caliper PLL targets a 2 MHz frequency resolution for an internal frequency of 22 MHz and a PLL bandwidth close to 2 MHz.

Number of BLE channels	N	N = 1 BLE channel	N = 40 (all BLE channels)	Special case: N = 11 BLE channels
PLL mode	Caliper PLL mode			Integer-N PLL mode
Output frequency step $\Delta f_{OUT}$	$N (f_{IN1} - f_{IN2})$	$f_{IN1} - f_{IN2} = 2$ MHz	$40 (f_{IN1} - f_{IN2}) = 80$ MHz	$11 (f_{IN1} - f_{IN2}) = 22$ MHz
Secondary loop internal frequency step	$N \cdot f_{IN2}$	$f_{IN2} = 20$ MHz	$40 \cdot f_{IN2} = 800$ MHz	$11 \cdot f_{IN2} = 220$ MHz

Table 3C: Frequency shifts of the Caliper PLL architecture.

The proper choice of the two internal frequencies  $f_{IN1}$  and  $f_{IN2}$  tackles an issue concerning the respective oscillator gains ( $K_{VCO}$  expressed in Hz/V) representing in Table 3C. Indeed, the Caliper PLL principle creates a small output frequency step  $\Delta f_{OUT}$  achieved by the difference of the two internal frequencies  $f_{IN1}$  and  $f_{IN2}$ . However, the secondary loop acts as a classical integer- $N$  PLL meaning that if the proposed PLL covers one BLE channel ( $\Delta f_{OUT} = 2$  MHz), the secondary loop needs to produce an internal frequency step of  $f_{IN2} = 20$  MHz as represented in Table 3B. Thus, to cover all the 40 BLE channels using the Caliper effect, the minimum oscillator gains  $K_{VCO1}$  and  $K_{VCO2}$  of the two oscillators must be theoretically set to 80 MHz/V and 800 MHz/V, respectively. Any noise on the oscillator control voltage is amplified by the oscillator gain, such a high oscillator gain makes the  $R_{VCO2}$  oscillator very sensitive to noise perturbation. However, the dual-loop architecture of the Caliper PLL allows to mitigate the  $R_{VCO2}$  oscillator gain.

Supposing that the Caliper PLL has to produce an output frequency step of  $\Delta f_{OUT} = 22$  MHz corresponding to eleven BLE channels. From the Caliper effect, this output frequency step is created by incrementing 11<sup>th</sup> times the divide-by- $N_1$  frequency divider and by decrementing 11<sup>th</sup> times the divide-by- $N_2$  frequency divider. The change of the divide-by- $N_2$  frequency divider implies a 220 MHz internal frequency step inside the secondary loop. As represented in the Table 3B, the integer- $N$  mode of the Caliper PLL achieves the same output frequency step of  $\Delta f_{OUT} = f_{IN1} = 22$  MHz without implying a frequency step inside the secondary loop. In this mode, the secondary loop  $R_{VCO2}$  is not impacted. Thus, to cover all the BLE channels, the minimum oscillator gains  $K_{VCO1}$  and  $K_{VCO2}$  must now be set to 88 MHz/V and 220 MHz/V, respectively. Thus, the suitable choice of the two internal frequencies  $f_{IN1}$  and  $f_{IN2}$  enables a lower oscillator gain  $K_{VCO2}$ , reducing the oscillator noise sensibility [BES\_07] and hence, improving the phase noise performance of the overall PLL. The flexibility of the Caliper PLL concerning the output frequency step modes, enables to reduce and frame the oscillator gain values for the stability analysis.

### 3.3.4 Stability verification of the system

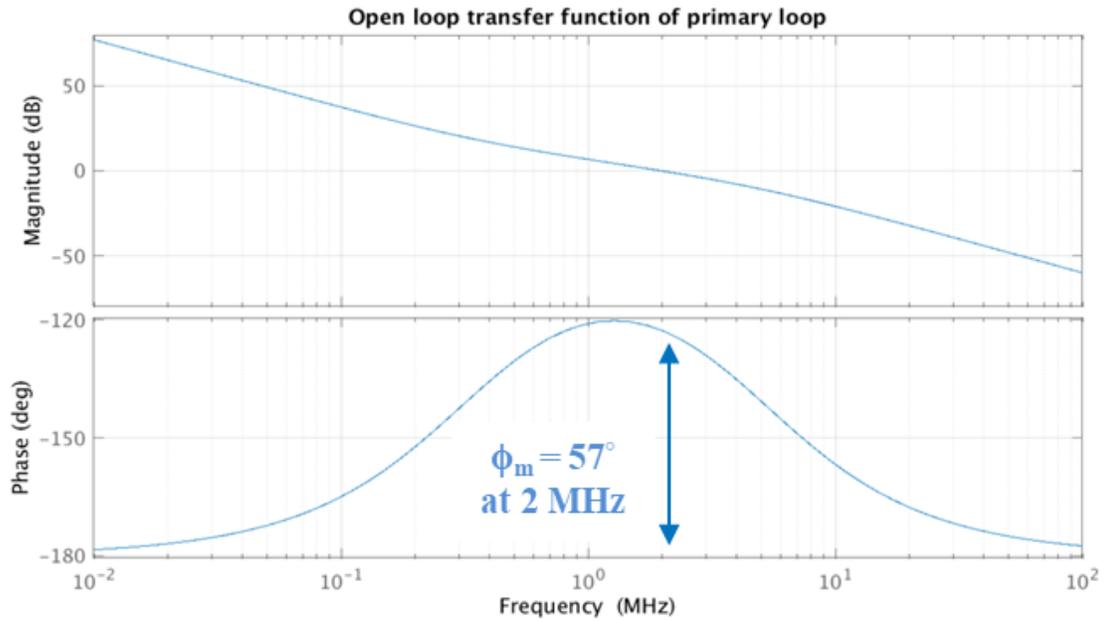


Figure 3.6: Bode plot of the primary loop open-loop transfer function.

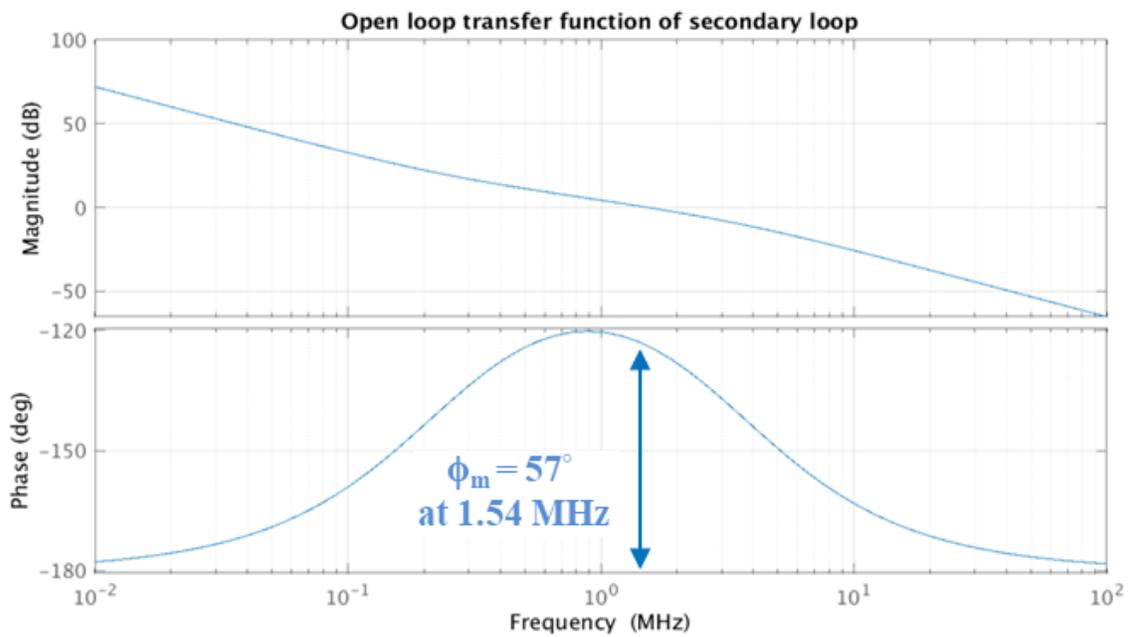


Figure 3.7: Bode plot of the secondary loop open-loop transfer function

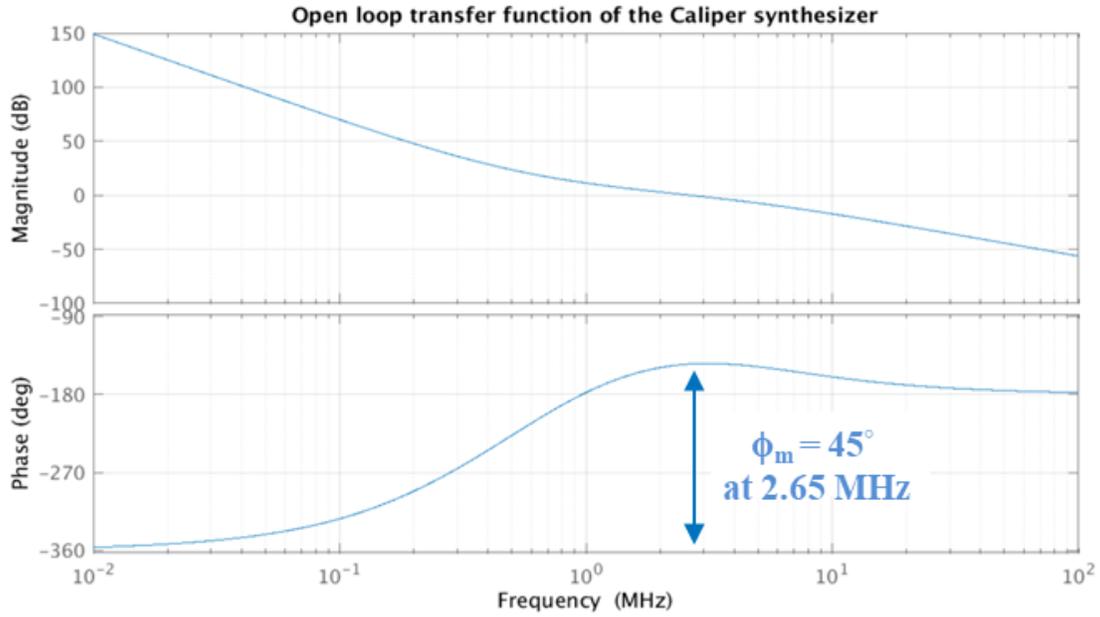


Figure 3.8: Bode plot of the Caliper synthesizer open-loop transfer function.

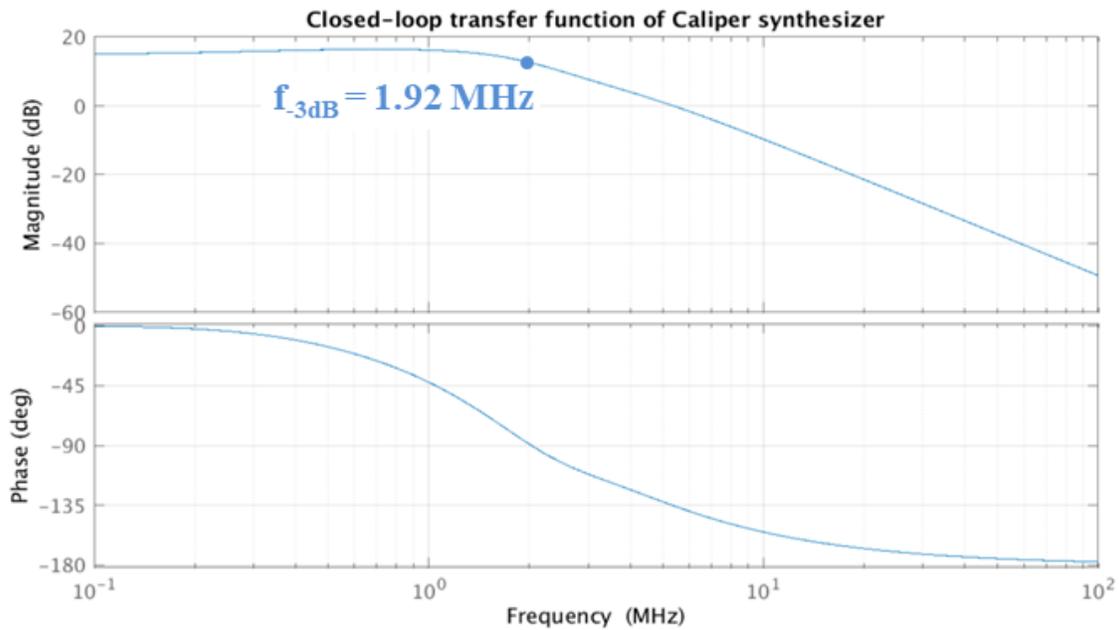


Figure 3.9: Bode plot of the Caliper synthesizer closed-loop transfer function.

Figure 3.6 and Figure 3.7 represent the open-loop Bode diagrams of the primary loop and secondary loop. Both the open-loop transfer functions show a phase margin around 57 degrees. The open-loop Bode diagram in Figure 3.8 shows a phase margin around 45 degrees to bear out the overall PLL stability. As illustrated in Figure 3.9, the closed-loop Bode diagram shows a PLL bandwidth at -3dB is around 1.92 MHz with a 3 dB overshoot.

The in-band gain is expressed as the sum of each loop gain as:

$$Gain_{inBand} = \frac{N_1}{R} + \frac{N_2}{R + X} \quad (3.13)$$

The reduction of the open-loop phase margin of the overall PLL can be explained by the non-integer behavior of the Caliper PLL. Indeed, the two single loops are presenting nearby zeroes and poles in the total closed-loop transfer function of the overall system. The non-integer behavior is another reason to verify the PLL stability with the behavioral proof of concept.

The aim of this sizing guideline is to underline the multiple trade-offs in a higher order PLL architecture. The best selection between architectural parameters as  $K_{VCO}$  or  $I_o$ , stability metrics as the phase margin  $\phi_m$  or the PLL bandwidth are also confronted by the PLL performance. Because  $K_{VCO}$  and  $I_o$  should remain constant in all channels, the  $N$  parameter is the only one to vary. Variations of these parameters ( $N_1$  and  $N_2$ ) within all the BLE channels should be verified to asset the stability of the loop. The PLL bandwidth is settled by the stability condition of the proposed PLL which is ensured by taking into consideration the stability of each integer- $N$  loop combined in an OPLL topology.

### 3.4 Noise analysis

This section is dedicated to the noise analysis of the Caliper PLL. First, the noise sources and noise metrics such as phase noise and reference spurs are presented. A noise model based on the linear phase domain model is proposed where each PLL building block is associated with its intrinsic noise source. Based on a similar approach to the Laplace phase-domain representation, each noise transfer function is computed. The noise model determines the contribution of each PLL building block in the PLL output phase noise. Thus, the noise study identifies the critical building blocks and the loop parameters to optimize the overall PLL performance.

#### 3.4.1 Noise sources and metrics

Electrical noise is created by small current or voltage fluctuations that are generated inside the devices. Noise sources are separated into two categories:

- intrinsic sources as thermal noise
- interference sources as supply noise [ARA\_10]

In the case of a frequency synthesizer, the study is focused on the noise created by the different building blocks of the system and their impact on the output specifications.

Thus, the noise analysis determines the main contributors of the system spectral purity. Their identifications and their dynamics draw the specifications of the frequency synthesizer. There are four main types of intrinsic noise.

- The **Shot noise** is usually represented by a direct-current flow present in diodes. Independent of temperature, it results from the random statistical fluctuations of the electric current when the carrier passes a junction, a gap.
- The **Thermal noise** represents a random thermal motion of the electrons inside an electrical conductor. It is unaffected by the presence of current and it is directly proportional to the temperature. Both shot noise and thermal noise are considered as white noise, their power spectral density is nearly equal throughout the frequency spectrum. Thus, these sources are indistinguishable once introduced into the circuit.
- The **Flicker noise** or 1/f noise is usually related to a direct-current flow. Thus, the flicker noise is dominant for low-offset frequencies close to the carrier until the corner frequency  $f_c$  where the white noise sources become dominant.
- The **Burst noise** occurs in semiconductors and ultra-thin gate oxide films. It consists of sudden step-like transitions between discrete voltages or current levels, as high as several hundred microvolts, at random and unpredictable times. It is possibly caused by a random trapping and release of charge carriers in defect sites in bulk semiconductor crystals.

Each source can be represented in a Thevenin or Norton version. Identifications of these sources and their impact on the system draw the output specifications of the frequency synthesizer. Thus, noise metrics are then needed to compute the noise performance of the system. The average noise power  $P_n$  is expressed as:

$$P_n = \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T n^2(t) dt \quad (3.14)$$

where  $n(t)$  represents the noise waveform, the area under the curve  $n(t)$  is computed for a long time  $T$  and is normalized by  $T$ . Instantaneous noise value is random and difficult to predict. Since the time-domain view provides limitations, the phase domain is then used. The power spectral density (PSD) of the noise  $n(t)$  is denoted by  $S_n(f)$ , it displays the average power of the noise carried in a 1-Hz bandwidth at different frequencies. The total area under  $S_n(f)$  represents the average noise power  $P_n$  as:

$$\int_0^{\infty} S_n(f) df = \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T n^2(t) dt \quad (3.15)$$

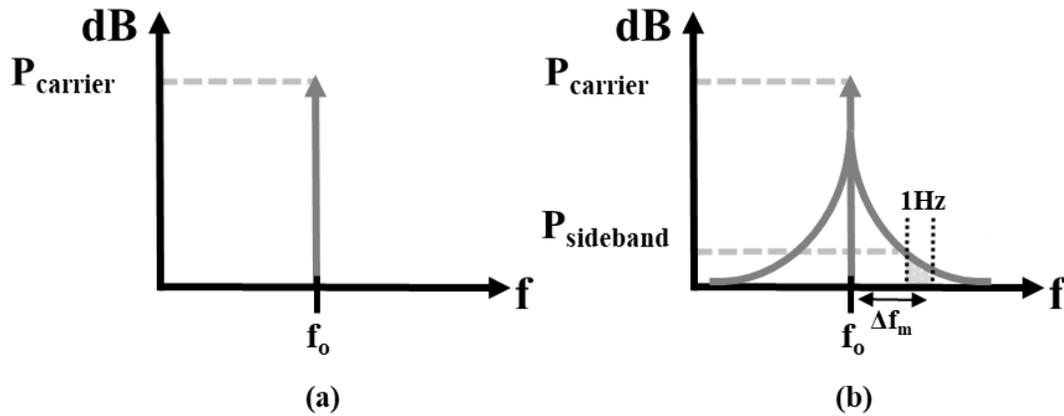


Figure 3.10. Power spectrum representation of an ideal oscillator (a) and (b) real oscillator.

The frequency synthesizer is required to generate an output signal with high spectral purity where a general expression of an oscillator is  $v(t) = A \cdot \cos(\omega t + \varphi(t))$ , with  $\varphi(t)$  representing the phase perturbation. The PLL generates the noise itself, transforming an ideal oscillator tone represented by a single tone to a noisy spectrum with skirts around the center of the carrier frequency. Represented in Figure 3.10, the real oscillator spectrum can be divided into portions of 1 Hz bandwidth at different offset frequencies  $f_m$  from the carrier  $f_0$ . The single-sideband noise spectral density  $\mathcal{L}$  in dBc/Hz is then computed as:

$$\mathcal{L}\{\Delta f\} = 10 \cdot \log \left( \frac{P_{\text{sideband}}(f_0 + \Delta f, 1\text{Hz})}{P_{\text{carrier}}} \right) \quad (3.16)$$

where  $P_{\text{sideband}}(f_0 + \Delta f, 1\text{Hz})$  represents the single-sideband power at a frequency offset of  $\Delta f$  from the carrier in a measurement bandwidth of 1Hz,  $P_{\text{carrier}}$  is the total power under the power spectrum. The advantage of  $\mathcal{L}\{\Delta f\}$  is its ease of measurement and the main disadvantage is that  $\mathcal{L}\{\Delta f\}$  shows effects of both phase and amplitude variations. Because amplitude noise can be limited,  $\mathcal{L}\{\Delta f\}$  is generally dominated by its phase noise portion [HAJ\_98].

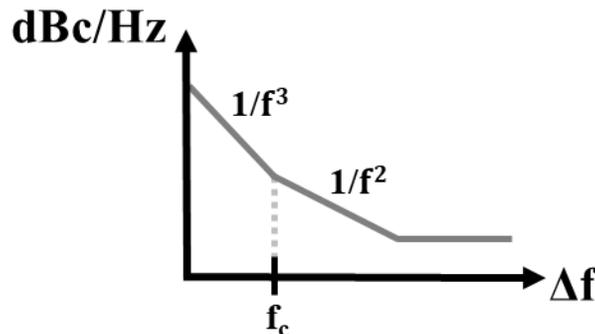


Figure 3.11 Oscillator Phase Noise representation in log scale.

Represented in Figure 3.11, the typical curve of the phase noise is separated into three regions. For low offset frequencies,  $1/f^3$  region with  $-30$  dB/decade is dominated by the Flicker noise while the  $1/f^2$  region with  $-20$  dB/decade is dominated by the white noise sources. The corner frequency  $f_c$  corresponds to the intersection between the two zones. Finally, the last region often represents the noise level of the measurement system as an external noise source. Depending on

the oscillator topology, many models are established to provide the phase noise performances. These models are semi-empirical as the Leeson-Cutler model [VAL\_08] or general models [ABI\_06] as the ISF theory [HAJ\_98]. These models highlight different approaches to explain the mechanisms of phase noise creation in oscillators. Thus, these models give design guidelines to improve the oscillator performance.

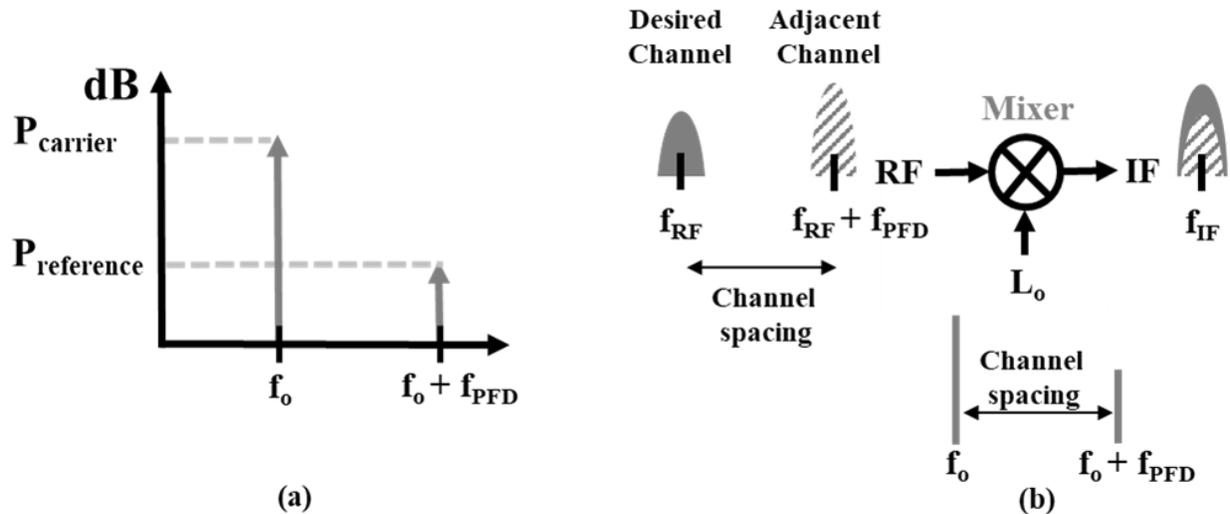


Figure 3.12 Reference spurs representation (a) and (b) Adjacent channel interference.

Another metric to measure the spectral purity of the oscillator is the reference spurs. Frequency spurs are generated by unwanted signals which are reflected as spurious frequencies on the VCO spectrum. Dual sidebands of these unwanted signals appear at the offset frequency of the carrier. The fundamental of the reference spurs is represented in Figure 3.12 at an offset frequency  $f_{\text{PFD}}$  from the carrier  $f_0$ . If the PLL architecture contains an input divide-by- $R$  divider, the frequency  $f_{\text{PFD}}$  represents  $f_{\text{ref}}/R$ , if not the frequency  $f_{\text{PFD}}$  equals the reference frequency. The main contributor of reference spurs is the PFD/CP building blocks. The Phase-Frequency Detector creates voltage pulses at the reference frequency. These pulses enable a current injection into the loop filter at the same reference frequency. However, the two pulses can enable together the current sink and the current source of the charge pump. The difference of current flow into the loop filter at the reference frequency modulates the oscillator. The frequency information is transmitted into the output spectrum by the oscillator gain  $K_{\text{VCO}}$ . Thus, the non-idealities of the PFD/CP block create a VCO frequency deviation in a locked condition. This deviation is compensated over time by the PFD/CP and generates other reference spurs.

For an example of a classical integer- $N$  PLL, the reference frequency represents the frequency resolution and it is chosen equal to the channel sizing. Thus, the output spectrum of the desired channel presents a reference spur which is in the adjacent channel as represented in Figure 3.12(b). The power of this spur catches information of the adjacent channel and brings back its information into the intermediate frequency (IF) during the down-conversion of the desired channel. This adjacent interference is important to consider because it deteriorates the conversion quality of the desired channel.

The spurs are expressed as a power ratio with its magnitude in dBc. For a simple loop with the same second-order transimpedance filter, an approximated relation of the fundamental reference power is expressed by:

$$\frac{P_{ref\ spur}}{P_{carrier}} = 20 \cdot \log \left( \frac{K_{VCO} \cdot I_{Leak}}{2\pi C_B f_{PFD}^2} \right) \quad (3.17)$$

where  $P_{ref\ spur}$  is the power of the reference spurs,  $P_{carrier}$  is the power of the carrier,  $K_{VCO}$  is the oscillator gain,  $C_B$  is the capacitor value of filter,  $I_{Leak}$  is the current leakage of the charge pump and  $f_{PFD}$  is the internal working frequency of the loop.

It is interesting to notice the design guidelines involved in this relation. Of course, the leakage current should be minimized because it is the main reason for the reference spurs creation. However, the reduction of the oscillator gain enlightens the same conclusion as the stability analysis. A reduction of this gain reduces the reference spurs power. The rise of the working frequency is coherent with the Caliper PLL architecture because this architecture presents a higher working frequency for the same frequency step than a classical integer-N PLL. However, the value of the capacitance  $C_B$  can conflict with its sizing after the stability analysis. Thus, another trade-off between stability and performance is here highlighted.

The last metric used to specify noise performance of a PLL architecture is the rms jitter. The jitter is the representation in the time domain of the phase noise as represented in Figure 3.13.a. The jitter represents a phase variation over time due to the noise involved in the system.

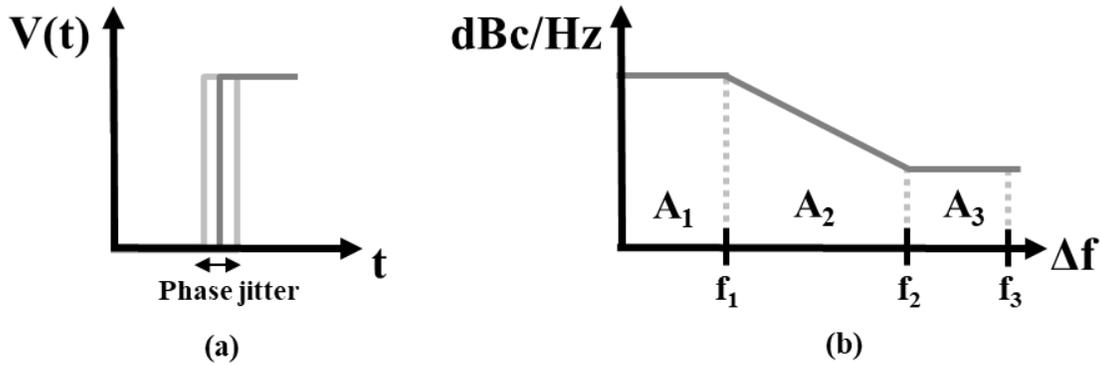


Figure 3.13 Phase jitter representation in time domain (a) and (b) Phase noise with area representation.

The rms jitter is calculated by the conversion of the phase noise. A way to compute the jitter is given by:

$$Jitter_{RMS} \approx \frac{\sqrt{2 \cdot 10^{\left(\frac{A}{10}\right)}}}{2\pi f_o} \quad (3.18)$$

where  $A$  is the Integrated Phase Noise (IPN) power, represented by the total area under the phase noise curve and  $f_o$  is the output frequency of the synthesizer.

For wide PLL bandwidth, it appears that the in-band noise level (A1 area) has an important impact on the total phase noise performance. Thus, contributions of noise within PLL bandwidth frequency are the key to improve the PLL performances.

### 3.4.2 Phase noise domain model

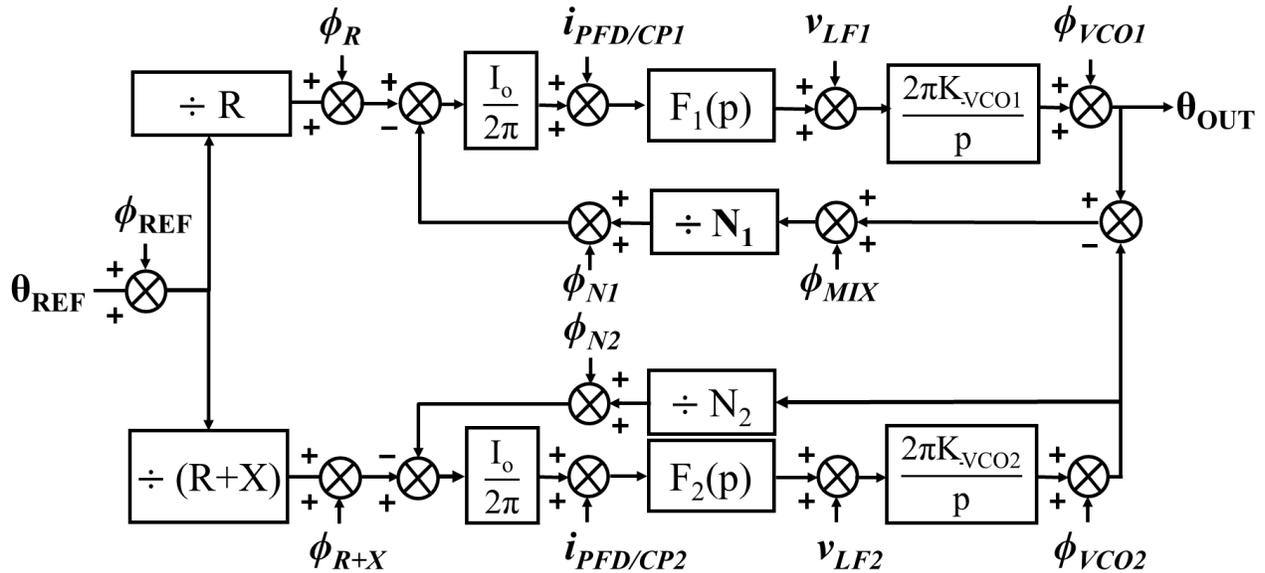


Figure 3.14 Caliper PLL phase domain model.

Linear phase domain model for the Caliper Loop PLL is based on a similar approach to the Laplace phase-domain representation. Represented in Figure 3.14, each PLL building block is associated with its phase noise source. This model considers noise created by the building block such as thermal noise, shot noise, or flicker noise. It does not consider noise as supply noise, substrate noise, or noise correlated by another block.

The noise sources are represented as phase noise sources in this representation, expected for two building blocks. The noise produced by the association PFD/CP is considered as a current noise source and the noise produced by the loop filter is considered as a voltage noise source. Each noise source is transformed into phase noise contribution by the phase noise transfer function. The noise transfer function for each noise source is represented in Table 3D.

Detailed in Appendix B, the transfer functions are separated into three groups: low-pass, band-pass, and high-pass behaviors. Within their bandwidth, the transfer functions multiply the noise source by the function gain. Because the gain is settled by the loop parameters, it is another way to design the PLL after the stability analysis. The pass-band group is composed by the secondary oscillator function because the high-pass function is filtered by the primary loop low pass behaviour. Moreover, each noise transfer function of the secondary loop is filtered through the low-pass behavior of the primary PLL Loop [PAR\_10]. Thus, it relaxes the design constraints on the secondary loop and the high-offset frequencies are only dominated by the primary loop oscillator noise.

Noise source	Noise transfer function $H_i$	In-band gain	Function type
Reference noise	$\frac{\theta_{out}}{\phi_{REF}} = H_{CL1}(p) \cdot \left(1 + \left(\frac{R}{N_1}\right) \cdot H_{CL2}(p)\right)$	$\frac{N_1}{R} + \frac{N_2}{R + X}$	Low-pass
Divider R	$\frac{\theta_{out}}{\phi_R} = R \cdot H_{CL1}(p)$	$N_1$	Low-pass
Divider R+X	$\frac{\theta_{out}}{\phi_{R+X}} = \frac{R \cdot (R + X)}{N_1} \cdot H_{CL1}(p) \cdot H_{CL2}(p)$	$N_2$	Low-pass
Divider $N_1$	$\frac{\theta_{out}}{\phi_{N1}} = R \cdot H_{CL1}(p)$	$N_1$	Low-pass
Divider $N_2$	$\frac{\theta_{out}}{\phi_{N2}} = \frac{R \cdot (R + X)}{N_1} \cdot H_{CL1}(p) \cdot H_{CL2}(p)$	$N_2$	Low-pass
Mixer	$\frac{\theta_{out}}{\phi_{Mix}} = \frac{H_{OL1}(p)}{1 + H_{OL1}(p)}$	1	Low-pass
Primary Loop Filter	$\frac{\theta_{out}}{v_{LF1}} = \frac{2\pi K_{VCO1}}{p} \cdot \frac{1}{1 + H_{OL1}(p)}$	20 dB/dec slope	Low-pass
Secondary loop filter	$\frac{\theta_{out}}{v_{LF2}} = \frac{R}{N_1} \cdot CL_1(p) \cdot \frac{2\pi K_{VCO2}}{p} \cdot \frac{1}{1 + H_{OL2}(p)}$	20 dB/dec slope	Low-pass
Primary PFD/CP	$\frac{\theta_{out}}{i_{PFD/CP1}} = \frac{2\pi R}{I_o} \cdot H_{CL1}(p)$	$\frac{2\pi N_1}{I_o}$	Low-pass
Secondary PFD/CP	$\frac{\theta_{out}}{i_{PFD/CP2}} = \frac{2\pi R (R + X)}{I_o N_1} \cdot H_{CL1}(p) \cdot H_{CL2}(p)$	$\frac{2\pi N_2}{I_o}$	Low-pass
Primary RVCO	$\frac{\theta_{out}}{\phi_{VCO1}} = \frac{1}{1 + H_{OL1}(p)}$	40 dB/dec slope	High-pass
Secondary RVCO	$\frac{\theta_{out}}{\phi_{VCO2}} = \frac{R}{N_1} \cdot H_{CL1}(p) \cdot \frac{1}{1 + H_{OL2}(p)}$	40 dB/dec slope	Band-pass

Table 3D: Noise phase transfer function of the Caliper PLL phase-domain model.

It can be noticed that the final behavior of the noise contribution (low-pass, pass-band, or high-pass) is impacted by the behavior of the noise sources. For example, the pass-band behavior of the loop filter is conjugated by the high-pass behaviour of the filter noise source to produce a final pass-band noise contribution.

The phase noise is often expressed with the single-sideband noise power to carrier ratio  $\mathcal{L}$ , which is half of the power spectral density  $S$ . The phase noise contribution of a noise source is calculated by:

$$\mathcal{L}_{out,noise_i} = |H_i|^2 \cdot \mathcal{L}_{in,noise_i} \quad (3.19)$$

where  $\mathcal{L}_{out,source}$  is the output phase noise contribution of the considered noise source,  $H_i$  is the phase noise transfer function of this noise source and  $\mathcal{L}_{i,source}$  is its single-sideband phase noise.

Thus, each block contributes to the total phase noise of the system. Noise sources represent the intrinsic noise of the PLL building blocks, they are not correlated and the total phase noise is calculated by a superposition of each output phase noise contribution as:

$$\mathcal{L}_{out,total} = \sum_i \mathcal{L}_{out,noise_i} \quad (3.20)$$

where  $\mathcal{L}_{out,noise_i}$  is the noise contribution of each noise source.

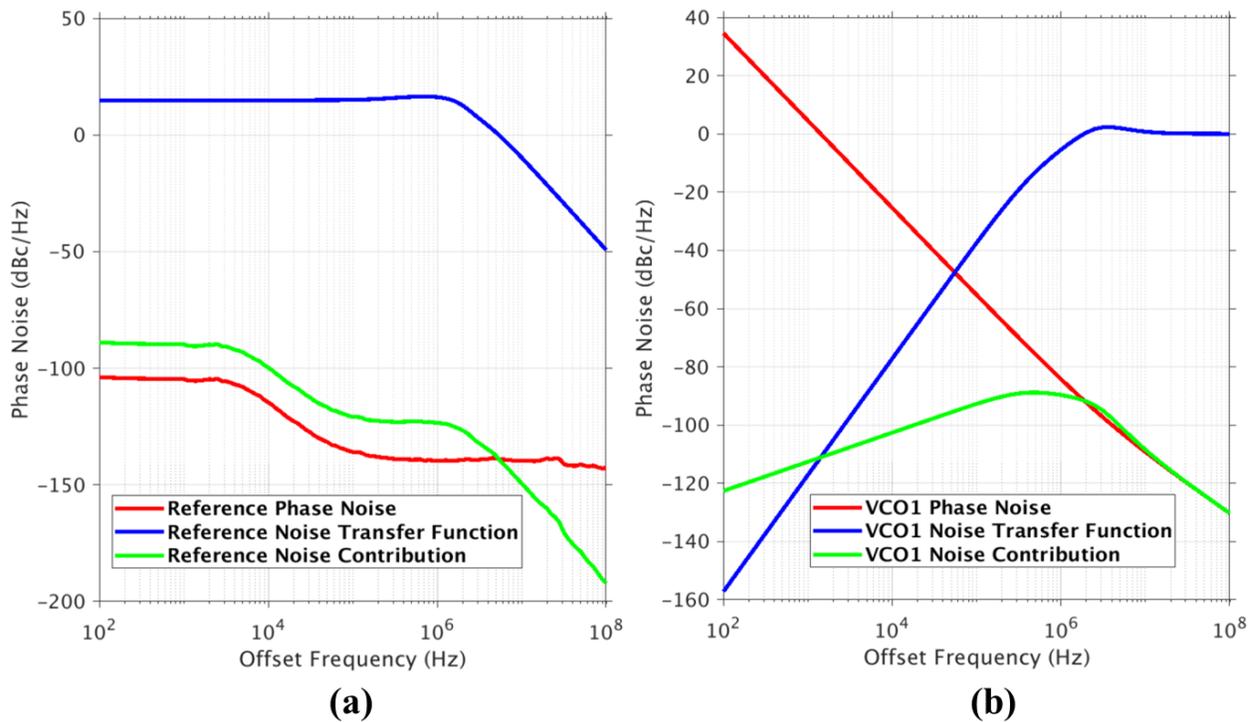


Figure 3.15 Phase noise representations of reference noise (a) and (b) primary loop oscillator noise.

Figure 3.15 represents two examples of the reference noise and the primary loop oscillator noise. Each triplet represents, the noise source in red line, the noise phase transfer function in blue line and the noise contribution in green line. It highlights how the phase noise contribution is calculated. Each triplet for each noise source is represented in Appendix B.

Intrinsic noise sources are predicted by direct measurement or by simulating the building blocks. Unless otherwise specified, the noise sources considered in this section are the simulated intrinsic noise from the implemented PLL building block of Chapter 5. Each noise source from the Caliper architecture is detailed in this section.

- Reference noise source

The reference noise source contribution of the total output phase noise coincides with the reference phase noise multiplied by the PLL loop Gain. Among different ways to predict the reference phase noise, one consists of using the Leeson's model [VAL\_08]:

$$S_{\text{ref}}(f_m) = 10 \log \left( \frac{FkT}{2A} \cdot \left( 1 + \frac{1}{f_m^2} \left( \frac{f_o}{2Q} \right)^2 \right) \cdot \left( 1 + \frac{f_f}{f_m} \right) \right) \quad (3.21)$$

where  $f_m$  is the frequency offset,  $F$  represents the noise figure of the oscillator,  $k$  is the Boltzmann's constant,  $T$  is the absolute temperature,  $A$  is the output power of the oscillator,  $Q$  is the loaded quality factor of the resonator,  $f_o$  is the carrier frequency and  $f_f$  is the flicker corner frequency.

The other way is to directly measure the phase noise performance of the source reference, crystal oscillators, or source generators. It allows to work with the real phase noise and to incorporate it inside the noise model. The reference phase noise represented in Figure 3.15(a) is evaluated using an Agilent E4400B signal source generator.

- Filter noise source

The output noise of resistive and capacitive components is computed by the thermal noise of the real part of the complex admittance of the loop filter. Modeled as a thermal noise source in parallel with the admittance  $Y$ , the single-sided power spectral density of the noise current is expressed as:

$$\mathcal{L}_{\text{filter}}(f) = 10 \log(4kT \cdot \text{Re}\{Y(f)\}) \quad (3.22)$$

where  $\text{Re}\{Y(f)\}$  is the real part of the loop filter admittance. The power spectrum density of the filter noise contribution is then calculated, the voltage noise source is subsequently filtered by the filter. Calculation of the noise contribution of the loop filter is detailed in Appendix B.

- Oscillator noise source

The intrinsic noise source of an oscillator corresponds to its free-running phase noise. Many models express the phase noise of an oscillator depending on the oscillator topology and the way to consider the noise phenomena. It can also be simulated through the RF spectrum simulator by considering an accurate prediction of the model.

- Phase detector and charge pump noise source

An ideal PFD/CP is considered for the noise study. Meaning that no DC mismatch is present between the current source and the current sink while the PLL is considered in its locked state. The dead zone corresponds to an amount of small phase error variations that are not seen by the PFD. In locked state, it is represented by a small pulse of width on control signals.

$$i_n = 10 \log \left( 2 \cdot \left( \frac{\delta_{CP}}{T_{ref}} \right) \cdot I_{n,cp}^2 \right) \quad (3.23)$$

where  $I_{n,cp}$  is the noise current of the charge pump in  $A^2/Hz$ ,  $\delta_{CP}$  is the dead zone pulse width and  $T_{ref}$  is the reference period signal. The factor 2 here considers both the current sources of the charge pump.

- Frequency divider and mixer noise

Normally the noise dividers are considered negligible for the phase noise analysis. However, the divide-by-N and the mixer proposed for the Caliper architecture are fully digital. For example, the parasitic resistance and capacitor generate their thermal noise. Their noise performance multiplied by the gain of their transfer function can have a significant impact on the total phase noise. A noise simulation of the extracted cells allows to generate the intrinsic noise of these building blocks. A thermal noise around  $-125$  dBc/Hz is then simulated, this level does not change with the divider value.

- Total phase noise of the Caliper PLL

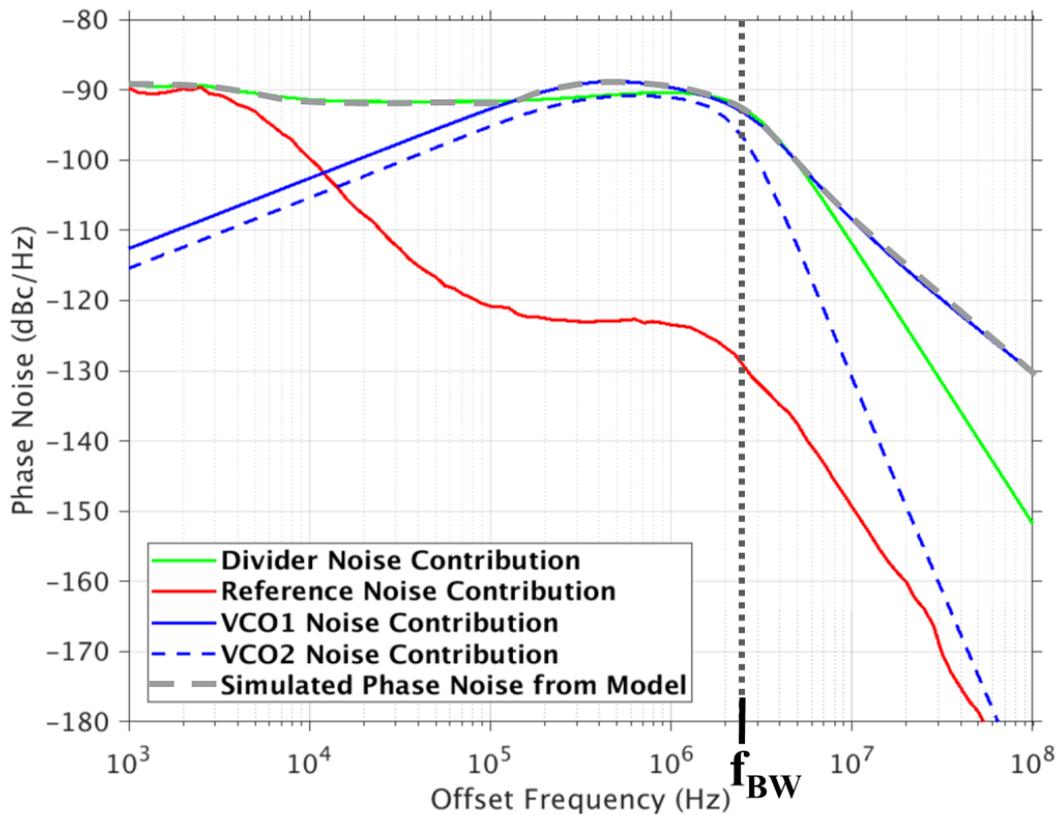


Figure 3.16 Simulated phase noise model of the Caliper PLL representing the four main contributions (noise from the dividers, both oscillators and the reference).

Figure 3.16 represents the main noise contributions and the simulated phase noise of the Caliper PLL architecture. The output phase noise is separated into two zones. The in-band phase

noise is considered for offset frequencies within PLL bandwidth, the in-band noise is here dominated by the divider noise contribution where the out-band phase noise is dominated by the oscillator phase noise from the primary loop. Generally, the main contributor within the PLL bandwidth is the reference noise. The simulated phase noise does not follow this rule. It occurs that the divider noise contributions rule the in-band noise performance in the Caliper architecture. Meaning that the noise contributions from the frequency dividers contribute strongly to the rms performance of the architecture because the rms jitter symbolizes the integrated area of the phase noise [GAO\_09]. Thus, a lower in-band noise level is expected by improving the noise performance of the four dividers.

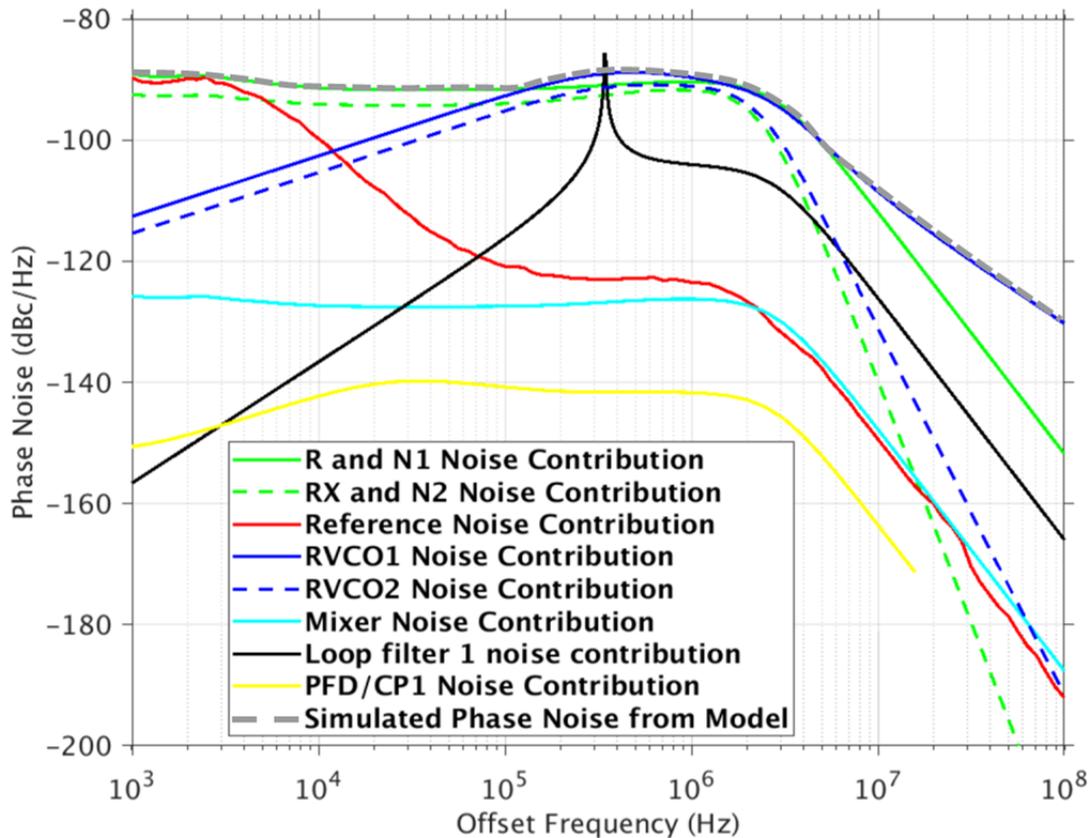


Figure 3.17 Total phase noise model of the Caliper PLL representing each noise contribution.

The phase noise model is represented in Figure 3.17, each noise contribution from the sources is compared to a measured output phase noise of the Caliper PLL architecture. As expected, the measured phase noise follows the in-band noise level within the PLL bandwidth and recovers the oscillation noise contribution for high-offset frequencies. A wide bandwidth optimizes the cleaning of the oscillator on the higher frequency range and improves the noise performance of the overall system. Moreover, the noise analysis identifies the critical building blocks and the loop parameters to optimize the overall PLL performance in terms of noise and rms jitter.

### 3.5 Behavioral proof of concept

The Laplace s-domain model treats the PLL as a continuous-time system. The sampling nature of the phase-frequency detector can add errors and thus degrade the effective phase margin. The z-domain model which is the discrete-time equivalent of the Laplace transform incorporates the discrete-time nature of the phase-frequency detector [HEI\_88]. Moreover, the linear model is valid only when the PLL is in its locked state and it does not contemplate the locking transient phenomenon, removing the linear model use if the PLL can never reach the locked state. When the PLL bandwidth is increased to be comparable to the internal reference frequency, the delay around the feedback loop can introduce excessive phase shift and thus lead to instability. Also based on linear assumptions, state-space analysis approximates the non-linear acquisition process and linear tracking of PLLs [HAN\_04].

Due to the limitations of the linear model, the proposed PLL is simulated through MATLAB Simulink, designed for modeling, simulating, and analyzing dynamical systems. Because the s-domain considers each building block as ideal, the Simulink model also allows to simulate some non-idealities of the building blocks. For example, the Simulink model can include the dead-zone of the phase-frequency detector. From the component parameters calculated in the stability analysis represented in Table 3D, the Caliper PLL is simulated through the Simulink software to establish the final behavioral proof of concept.

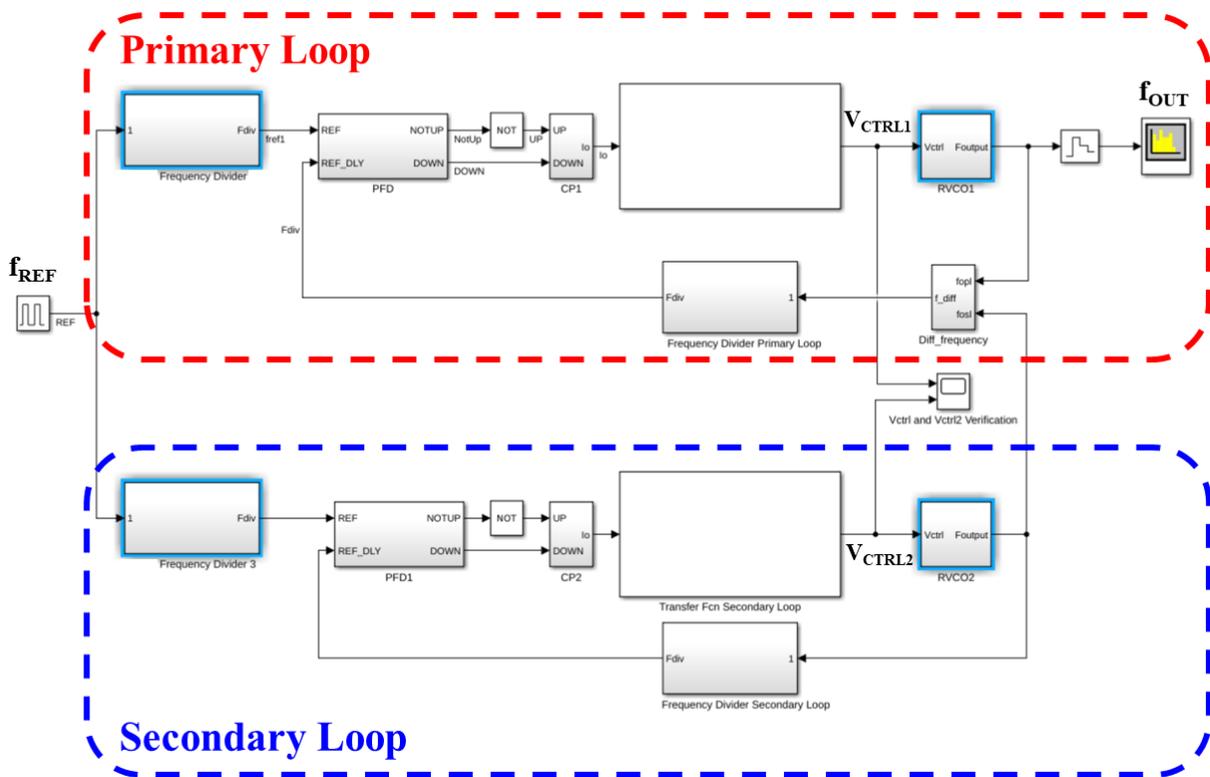


Figure 3.18 Simulink model of the Caliper PLL Architecture.

The Caliper PLL architecture in the Simulink software is represented in Figure 3.18. Each PLL block is designed using the Simulink toolboxes. For example, the charge pump uses the Simscape toolbox and the transimpedance filter is expressed by its Laplace transfer function. Represented in Table 3E, each parameter is charged into the Simulink model after the stability and noise analyses.

Symbol	Name	Values	Units
$f_{REF}$	Common reference frequency	440	MHz
$f_{IN1}$	Primary loop internal frequency	22	MHz
$f_{IN2}$	Secondary loop internal frequency	20	MHz
R	Primary loop input frequency divider	20	-
R+X	Secondary loop input frequency divider	22	-
$N_1$	Primary loop feedback frequency divider	70	-
$N_2$	Secondary loop feedback frequency divider	44	-
$I_0$	Charge pump current	10	$\mu A$
$K_{VCO1}$	Primary loop oscillator gain	245	MHz
$K_{VCO2}$	Secondary loop oscillator gain	245	MHz
$f_1$	Primary loop oscillator nominal frequency	2.28	GHz
$f_2$	Secondary loop oscillator nominal frequency	820	MHz

Table 3E: Caliper PLL parameters for the Simulink model.

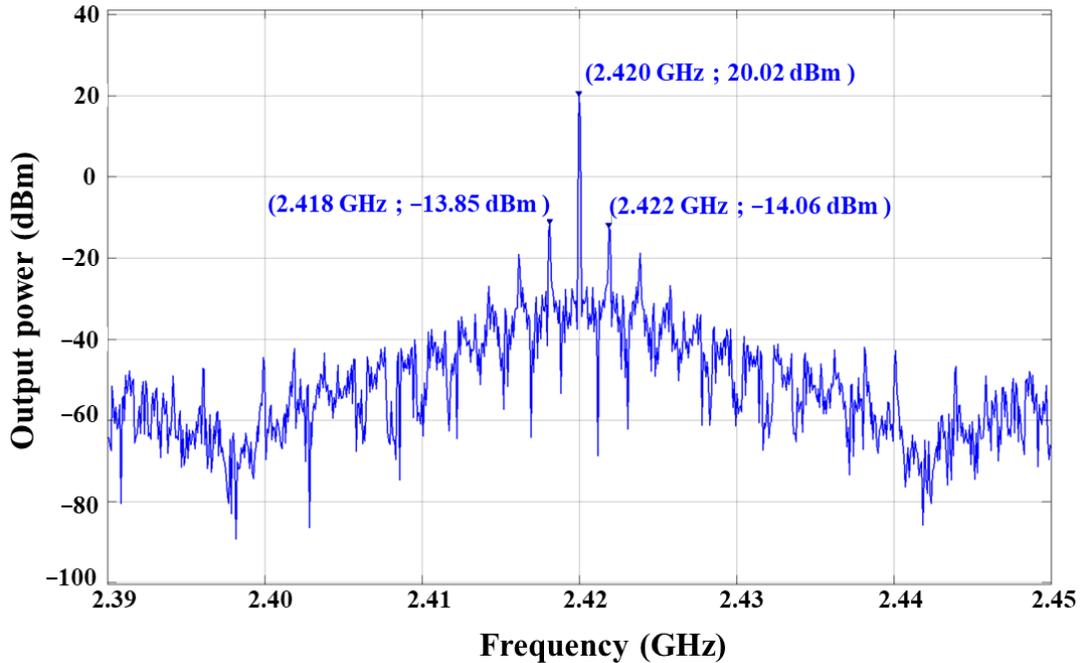


Figure 3.19 Simulated output frequency for a 2.42 GHz output frequency.

The simulated output frequency is represented in Figure 3.19. The Caliper PLL locks on the output frequency of 2.420 GHz which verifies the output frequency relation:

$$f_{OUT} = N_1 \cdot f_{IN1} + N_2 \cdot f_{IN2} \quad (3.24)$$

The spurs at 2 MHz offset frequency from the carrier is generated from the Offset-PLL topology of the proposed Caliper PLL [LEE\_05]. However, other spurs are expected at 22 MHz and 20 MHz from the carrier due to the internal frequencies  $f_{IN1}$  and  $f_{IN2}$ . Derived from the PLL topology, these specific spurs are represented in the output spectrum with an inferior power as expected. Indeed, the Simulink model is based on the architectural blocks from the Toolboxes. For example, a generic charge pump model is used for the Simulink simulation and it is not representative of the final charge pump architecture implemented in the Caliper PLL prototype. The aim of the Simulink model is to establish the behavioral proof of concept of the Caliper PLL.

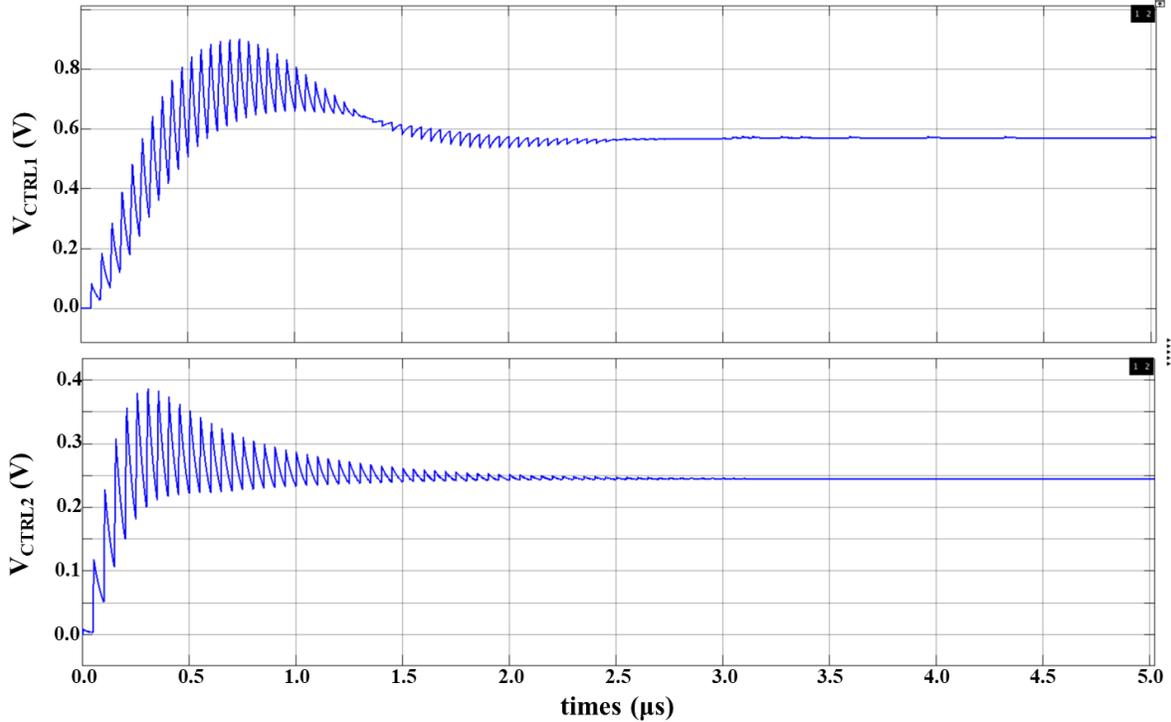


Figure 3.20 Simulated oscillator control voltage representation.

The two oscillator control voltages  $V_{CTRL1}$  and  $V_{CTRL2}$  are illustrated in Figure 3.20. The transient simulation grants the evaluation of the locking time of the PLL derived from the theoretical study. The proposed PLL achieves a simulated locking time of 3.0  $\mu\text{s}$ . The steady-state values are the control voltages that verify the output frequency relation of the oscillator:

$$f_{OUT} = f_i + K_{VCOi} \cdot V_{CTRLi} \quad (3.25)$$

Where  $f_i$  is the nominal frequency of the oscillator,  $K_{VCOi}$  is the oscillator gain and  $V_{CTRLi}$  is the oscillator control voltage.

$N_1$	$N_2$	Nominal $f_1$ (GHz)	$K_{VCO1}$ (MHz/V)	$V_{CTRL1}$ (mV)	Calculated $f_{OUT}$ (MHz)	Simulated $f_{OUT}$ (GHz)
70	44	2.28	245	571.3	2419.97	2.420
71	43			578.9	2421.83	2.422

Table 3F: Simulated Caliper PLL parameters from the transient simulation.

Table 3F gathers the simulated steady-state values of  $V_{CTRL1}$  and  $V_{CTRL2}$  for the feedback divider values of  $N_1 = 70$  and  $N_2 = 44$ . In order to verify the output frequency step of  $\Delta f_{OUT} = 2$  MHz, the same simulated values are obtained by the feedback divider values of  $N_1 = 71$  and  $N_2 = 43$ . The simulated output frequencies are in line with the calculated values which settles the proof of concept of the proposed Caliper PLL architecture.

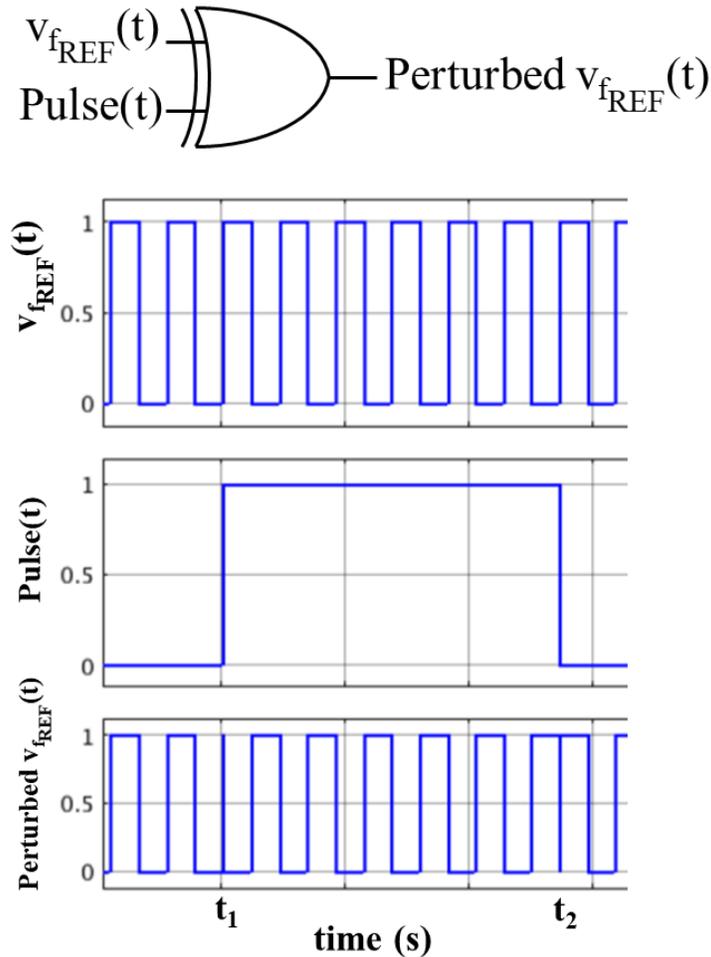


Figure 3.21 Perturbation representation of the reference frequency.

Since the Simulink model is developed to simulate dynamical systems, it could also enable to visualize the system response to an external perturbation. Represented in Figure 3.21, a perturbation is then created during the PLL locking process. A pulse injected through the XOR gate to suddenly shift the phase of the reference frequency. Thus, two perturbations occur at  $t_1 = 1.5 \mu\text{s}$  during the locking process and at  $t_2 = 5.3 \mu\text{s}$  when the PLL has recovered its locked state.

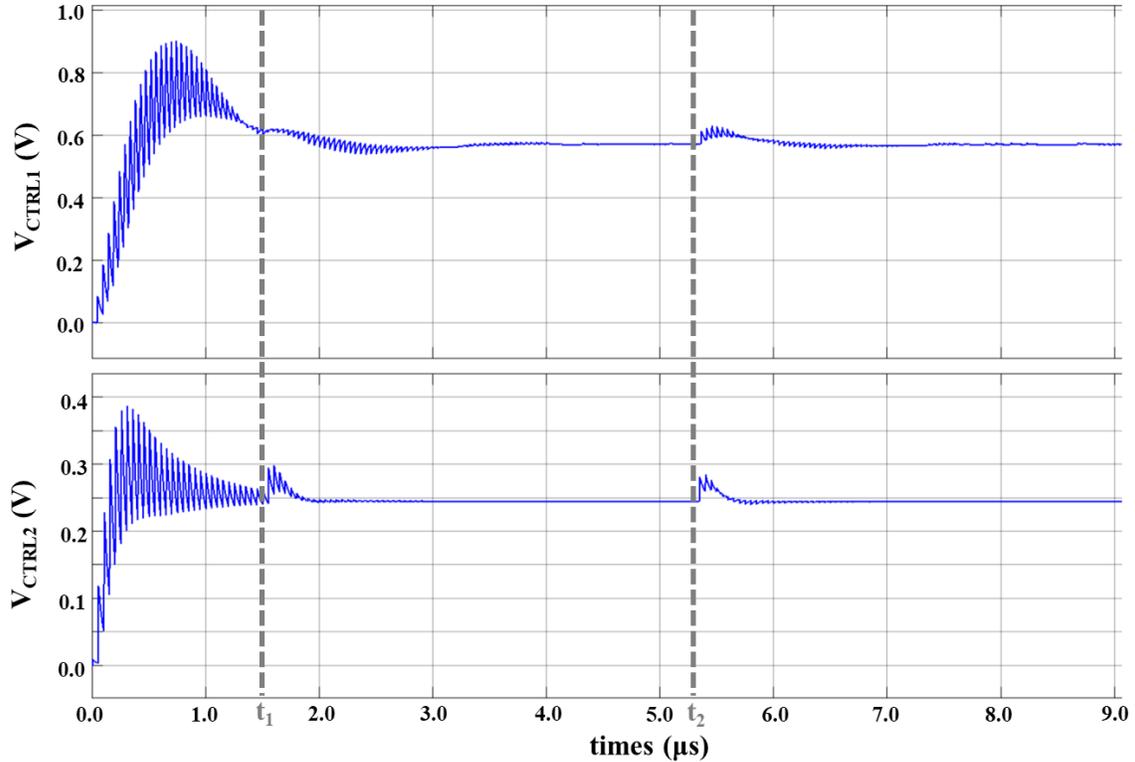


Figure 3.22 Simulated oscillator control voltages impacted by the perturbation.

The two oscillator control voltages  $V_{CTRL1}$  and  $V_{CTRL2}$  are illustrated in Figure 3.22. After the first perturbation, the system recovers the expected frequency. For the second perturbation occurring during the PLL locked state, the system recovers its locking in  $1.6 \mu\text{s}$ . This type of simulation concedes to strengthen the behavioral proof of concept of the Caliper PLL architecture.

### 3.6 Conclusion

This chapter is focused on the presentation of the Caliper PLL architecture. The proposed PLL is composed of a dual-loop topology with a common reference frequency. The main feature of the Caliper PLL is that its frequency resolution is tuned using a difference frequency of the two internal frequencies. Thus, the “Caliper effect” expands the PLL bandwidth to improve oscillator phase noise performance close to the carrier, enabling the use of ring oscillators to target a compact frequency synthesizer. Furthermore, the Caliper PLL achieves the same properties as fractional- $N$  PLL in terms of frequency resolution and PLL bandwidth. Thus, the proposed solution is an alternative to the commonly used fractional- $N$  PLL architecture for IoT applications.

Based on a Laplace model of the Caliper PLL, the stability analysis identifies all the trade-offs concerning the loop parameters. The PLL bandwidth is determined from the internal loop frequencies and the open-loop phase margin computation. The latter binds architectural parameters as the oscillator gain  $K_{VCO}$  with physical parameters as the loop-filter component values. Another trade-off concerns the integration of the two loop-filters which also limits the loop-filter component

values. The Caliper PLL deals with these multiple trade-offs to size the loop parameters and ensures the PLL stability.

The noise analysis is based on a phase domain model of the Caliper PLL. The phase noise model computes the contribution of each PLL building block in the output PLL phase noise. Thus, the loop parameters can be optimized to improve the output phase noise. As expected, the wide PLL bandwidth improves the oscillator noise close to the carrier. The noise model identifies the main contributors of the in-band phase noise. Furthermore, a crosscheck between the stability analysis and the noise analysis permits to optimize the overall PLL performance.

Due to the limitations of the Laplace model, a behavioral proof of concept is established with a Simulink model. Using the loop parameter values from the stability analysis, the dynamical Simulink model permits to verify that the proposed Caliper PLL locks on the expected output frequency. The output frequency resolution, which is the principal feature of the Caliper PLL, is then verified in simulation. Thus, the behavioral proof of concept of the proposed PLL architecture is established by the Simulink model. It validates the features of the Caliper PLL architecture as well as the loop parameters sizing from the stability analysis.



# 4 Ring Voltage Controlled Oscillators study in the context of FD-SOI technology

## 4.1 Introduction

This chapter is focused on the study of Ring Voltage-Controlled Oscillators (RVCOs) targeting the IoT application challenges highlighted in Chapter 2. The RVCO is an essential building block in any PLL architecture, thereby it is important to determine the performance of ring oscillator before the implementation of the Caliper PLL.

First, a brief comparison is drawn between the two categories of oscillators: Ring VCO and LC-VCO. The RVCO characteristics in terms of noise performance, power consumption, and area are discussed under the scope of the IoT application which permits to identify that the RVCO phase noise behavior is the main challenge to tackle. After presenting the classical RVCO frequency tuning strategies, a new tuning method approach is introduced by body-biasing the transistor back-gate. This unique tuning method is only achieved by using the specific advantages of the FD-SOI technology.

Afterwards, the RVCO phase noise performance is studied under the scope of the Impulse Sensitivity Function (ISF) theory. This theory determines the phase shift induced by a current perturbation into the oscillator. By identifying the oscillator sensitivity to phase perturbation, this theory indicates perspectives to improve the RVCO phase noise. Discussion about the ISF theory has led to the proposition of a Pseudo-differential RVCO (PRVCO) architecture which improves its immunity to phase perturbations, enhancing its phase noise performance. The PRVCO architecture is detailed and compared with a regular RVCO topology. The two ring architectures have been manufactured in 28nm FD-SOI technology. Measurement results and comparison with the state-of-the-art are provided.

Finally, performances of the two ring oscillators targeting IoT applications are discussed in the conclusion. The purpose of this chapter is to study RVCO topologies that take benefit of the FD-SOI technology to achieve efficient designs.

## 4.2 Ring versus LC oscillators comparison

Briefly, an oscillator represents a self-sustaining system that generates a periodic signal. A Voltage-Controlled Oscillator (VCO) has its oscillation frequency tuned by a control voltage. It exists two main categories of VCOs: based on an inductance-capacitance resonant tank called LC oscillators (LC-VCO) and based on delay cells called Ring oscillators (Ring-VCO or RVCO). Major differences between LC and ring VCO are specified in this section where the major trade-offs are focused on the oscillation frequency, the power consumption, and the phase noise performance.

Considering that a basic RVCO is composed of  $N$  inverter gain stages with a negative feedback. A rising edge at a node within the RVCO is propagated through  $N$  inverters stages and returns as a falling edge, forming half of the oscillation period  $T_{OSC}$  [RAZ\_19]. Thus, the RVCO maximum frequency is limited to the minimum delay achievable by the technology node. Consequently, RVCO can target frequencies about tens of GHz whereas the LC tank is preferred to reach even higher frequencies [ISS\_19].

The power consumption and the area are the two main characteristics of an oscillator targeting an IoT application. The first concern is the trade-off between the power consumption and the phase noise performance. Indeed, RVCO suffers from a poor phase noise due to a jitter accumulation between the delay cells and a poorer overall  $Q$  factor than a resonant LC tank. Moreover, jitter performance of a ring oscillator is proportionally related to its power consumption, consequently a better phase noise is reached at the cost of higher power consumption while in LC-VCO the power consumption is mainly used for biasing purposes. Thus, a comparison drawn in [ABI\_06] explicit that the RVCO burns widely much current than LC-VCO for the same phase noise at the same frequency. The ITRS oscillator Figure-of-Merit (FoM) highlights the trade-off between the oscillation frequency, the phase noise performance, and the power consumption by:

$$FoM_{OSC} = 10 \cdot \log\left(\frac{P_{DC}}{1 \text{ mW}}\right) - 20 \cdot \log\left(\frac{f_{OSC}}{\Delta f}\right) + \mathcal{L}_{\Delta f}(f_{OSC}) \quad (4.1)$$

where  $f_{OSC}$  is the oscillator frequency,  $\mathcal{L}_{\Delta f}(f_{OSC})$  is the phase noise at offset frequency  $\Delta f$  from the carrier  $f_{OSC}$ , and  $P_{DC}$  is the oscillator power consumption in mW. This FoM underlines the main guideline of an oscillator design. Considering the same oscillation frequency and the same phase noise, LC oscillators achieve lower power consumption. All these characteristics lead that the LC oscillator performs a better FoM than its RVCO counterpart. Thus, the phase noise performance of ring oscillators is the main challenge to tackle.

The second concern is the area of the oscillator because it is directly related to the manufacturing costs. The resonating tank of LC-VCOs is often based on an on-chip monolithic or planar spiral inductor along with a resonating capacitor. The capacitor is generally based on a MOS varactor to tune the oscillator frequency. Passive elements require thick metal layers which take up a large silicon area. Furthermore, the passive elements are not scalable with the process reduction contrary to the Ring-VCOs. For all these reasons, the Ring-VCOs are attractive solutions for compact oscillators. Last point of concern, the multiphase generation is native for RVCOs while

LC-VCOs require additional circuitry as I/Q dividers or polyphase filters which employ more area and power consumption in the whole system.

Concerning the IoT applications, the industrial expectations tend to expand the battery lifetime by using Ultra-Low-Power designs and aim to reduce the manufacturing cost with small area designs. Thus, RVCOs represent a good opportunity for future IoT markets, the challenge states to achieve better phase noise performance for a given power consumption.

### 4.3 Tuning strategy of a ring-oscillator

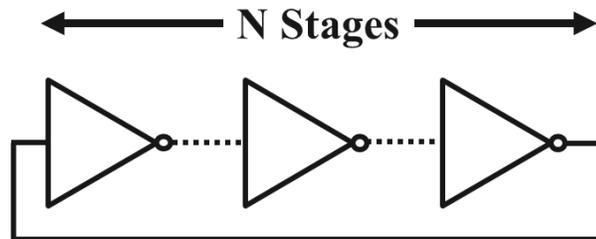


Figure 4.1: Ring-oscillator architecture with N delay cells.

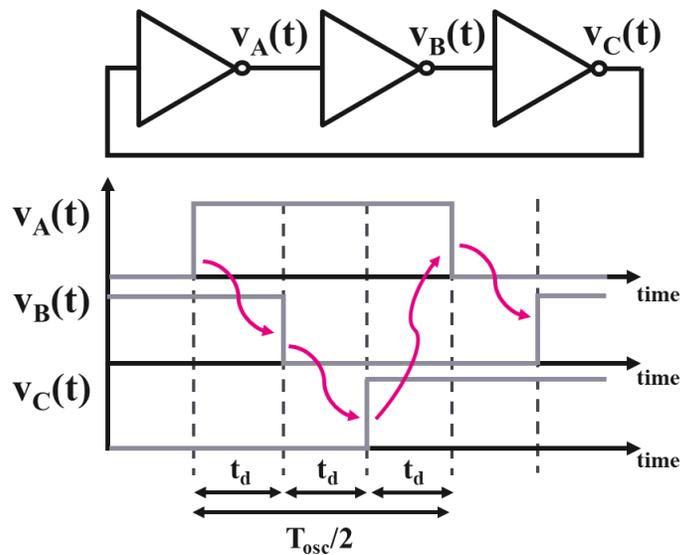


Figure 4.2: Ring-oscillator architecture with N = 3 delay cells.

Illustrated in Figure 4.1, a ring oscillator (RO) is formed by using an odd number (for single-ended RO) or an even number (for differential RO) of delay cells. Represented in Figure 4.2 for a RO with three delay stages, a rising edge of  $v_A(t)$  is inverted and propagated through  $v_B(t)$  with a propagation delay of  $t_d$ . This edge is then propagated through all the delay cells to return as a falling edge on  $v_A(t)$  after three propagation delays ( $3 \cdot t_d$ ) and thus, forming one-half of the

oscillation period  $T_{osc}$ . In addition, the relation between the number of delay cells and the propagation delay  $t_d$  satisfies the Barkhausen criterion to ensure the oscillation condition.

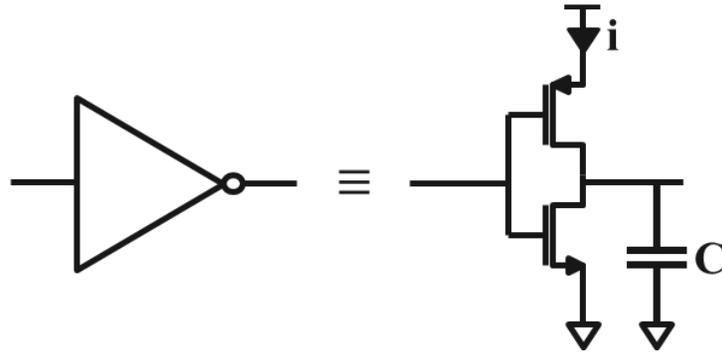


Figure 4.3: Representation of a delay cell composed of a single-ended CMOS inverter.

Illustrated in Figure 4.3, the delay cell is now considered as a simple single-ended CMOS inverter. The propagation delay  $t_d$  can be considered as the time of the linear charge or discharge of the following inverter capacitance by:

$$v(t) = \int_0^{t_d} \frac{i}{C} dt \quad (4.2)$$

Where  $i$  is the current inside the inverter,  $C$  is the parasitic capacitance of the inverter and  $t_d$  represent the propagation delay.

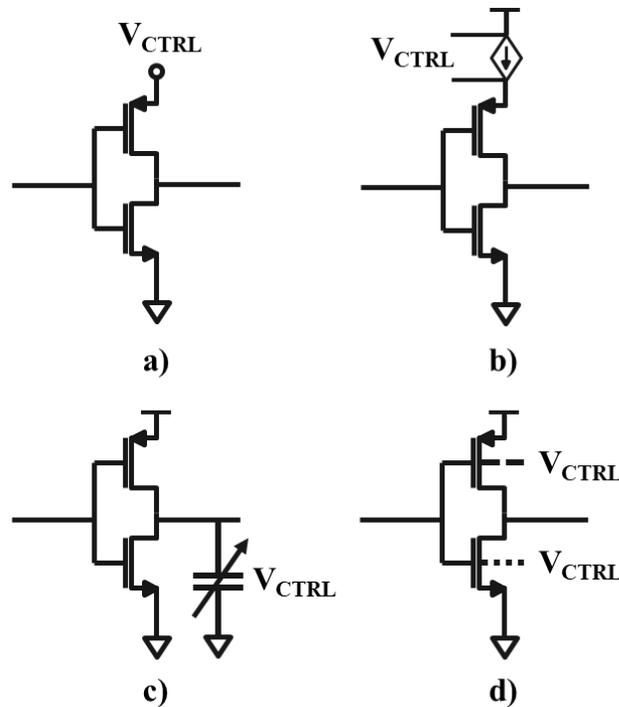


Figure 4.4: Tuning strategies of a delay cell composed of a single-ended CMOS inverter.

Hereby, the main tuning method to control the propagation delay (hence the RO frequency) is to vary the bias current inside the delay cell. Figure 4.4 illustrates some of the techniques to control the bias current of an inverter. The current can be controlled through the supply voltage as shown in Figure 4.4(a). This technique has the main disadvantage that the output signal amplitude varies according to the frequency control. Afterwards in Figure 4.4(b), another tuning technique called “Current starving” needs a voltage to current converter (V to I) to control the bias current of the delay cell. Another method consists to tune the capacitance instead of the current. In Figure 4.4(c), a varactor is added in parallel to the parasitic capacitance of the inverter. The propagation delay is here controlled by tuning the load capacitance value of the inverter without impacting the power consumption of the oscillator.

We propose another tuning method approach, only featured by using the FDSOI technology. The propagation delay is here tuned by controlling the threshold voltage  $V_T$  of the inverter. Illustrated in Figure 4.4(d), the frequency tuning method is enabled by body-biasing the transistor back-gate. Specific to the UTBB FD-SOI technology from STMicroelectronics [CAT\_17], the threshold voltage is then tuned to control the current of the inverter.

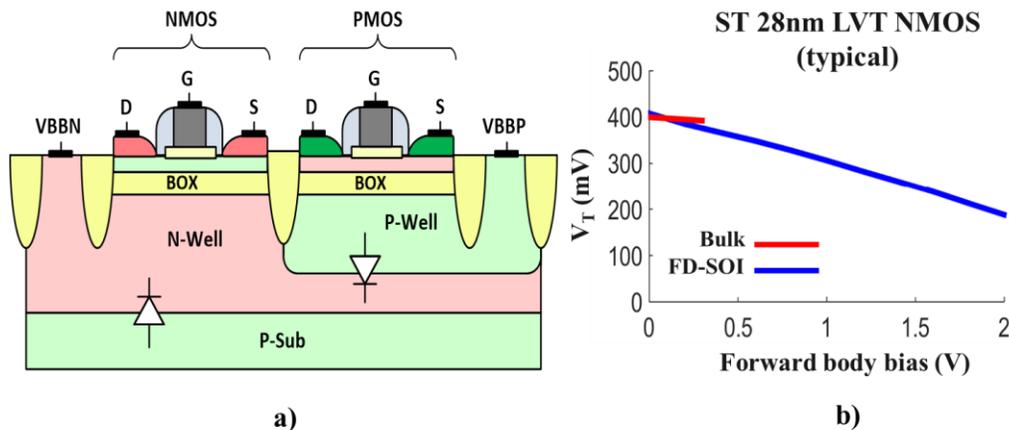


Figure 4.5: FD-SOI MOS transistors technology: (a) LVT MOS cross section and (b)  $V_T$  variation due to voltage body-biasing.

A cross-section of LVT 28nm FD-SOI CMOS transistor is shown in Fig. 4.5(a). In a typical bulk technology, the body biasing is limited by the source/drain parasitic diodes towards the substrate which only allow a limited body-biasing range of  $|0.3|$  V. Due to the channel isolation from the substrate obtained from the buried oxide layer, the source and drain diodes to the body respectively do not exist anymore, which allows a body-biasing operation over a large voltage range (0 V to  $|3|$  V respectively). A large  $V_T$  variation of hundreds of millivolts is enabled by the high body biasing factor of 85 mV/V proper to the FD-SOI technology as depicted in Fig. 4.5(b). The body biasing feature, unique of the FD-SOI technology, allows a simple access to this new frequency tuning knob. It grants a linear frequency tuning while saving power consumption and silicon area which are the two key important goals of an oscillator dedicated to IoT applications.

#### 4.4 RO study under the scope of the ISF theory

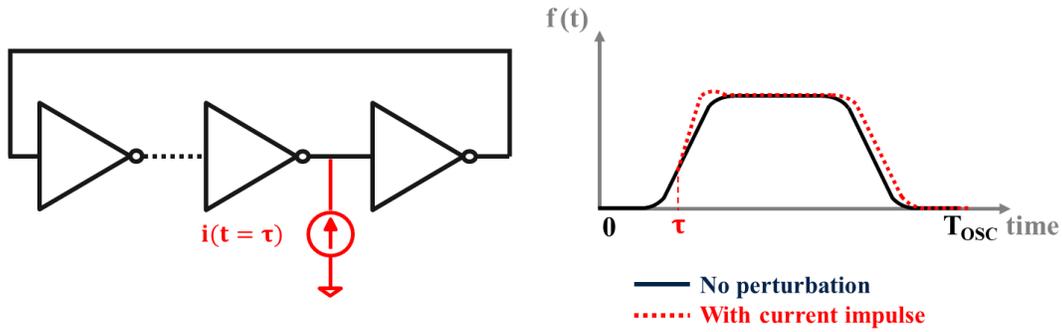


Figure 4.6: Peak injection representation and its effect on phase at zero crossing.

The Impulse Sensitivity Function (ISF) theory from Hajimiri [HAJ\_98] is an interesting tool to identify the design guidelines to optimize the oscillator phase noise performance. This theory considers the oscillator circuit as a linear time-variant (LTV) system. As represented in Figure 4.6, a current impulse is injected into one of the oscillator nodes to compute the resulting phase shift. The current impulse is injected at different points over an oscillation period and the resulting phase shift is expressed in [HAJ\_98] by:

$$\phi(t) = \int_{-\infty}^t \frac{\Gamma(\omega_o t)}{q_{max}} i(\tau) d\tau \quad (4.3)$$

where  $q_{max}$  is the maximum charge displacement across the node,  $i(\tau)$  represents the noise current injected into the node of interest and  $\Gamma(\omega_o t)$  is called the Impulse Sensitivity Function, a dimensionless,  $2-\pi$  periodic function which describes how much phase shift results from applying a unit impulse at time  $t = \tau$ .

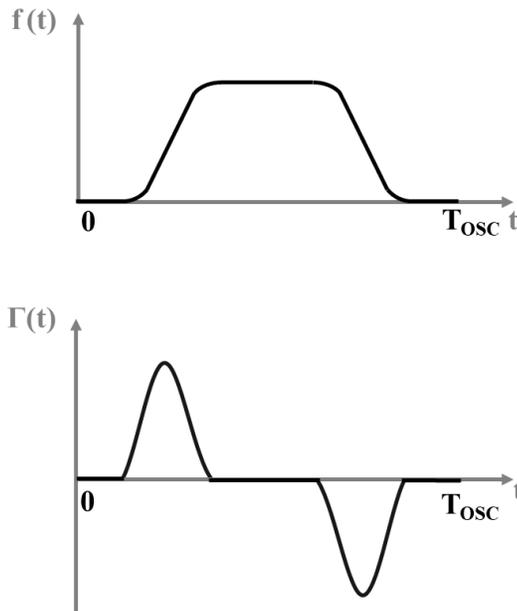


Figure 4.7: waveform and ISF representation of a typical ring oscillator.

The ISF function of a ring oscillator is represented in Figure 4.7, this representation enables to determine where the oscillator is sensitive to a phase perturbation. For instance, a ring oscillation is sensitive to phase perturbation during the transition phases. This theory also expresses the phase noise due to the white noise sources function of the ISF by:

$$\mathcal{L}\{\Delta\omega\} = 10 \log \left( \frac{\Gamma_{rms}^2 \frac{\overline{i_n^2}}{\Delta f}}{q_{max}^2 2\Delta\omega^2} \right) \quad (4.4)$$

where  $\Gamma_{rms}$  is the rms value of the ISF,  $i_n^2/\Delta f$  is the single-sideband power spectral density of the noise current source,  $q_{max}$  is the maximum charge displacement and  $\Delta\omega$  is the offset angular frequency from the carrier. From (4.4), optimum phase noise can be derived with a minimum ISF rms value. Thus, the ISF expression of a ring oscillator is calculated to determine how its phase noise can be improved.

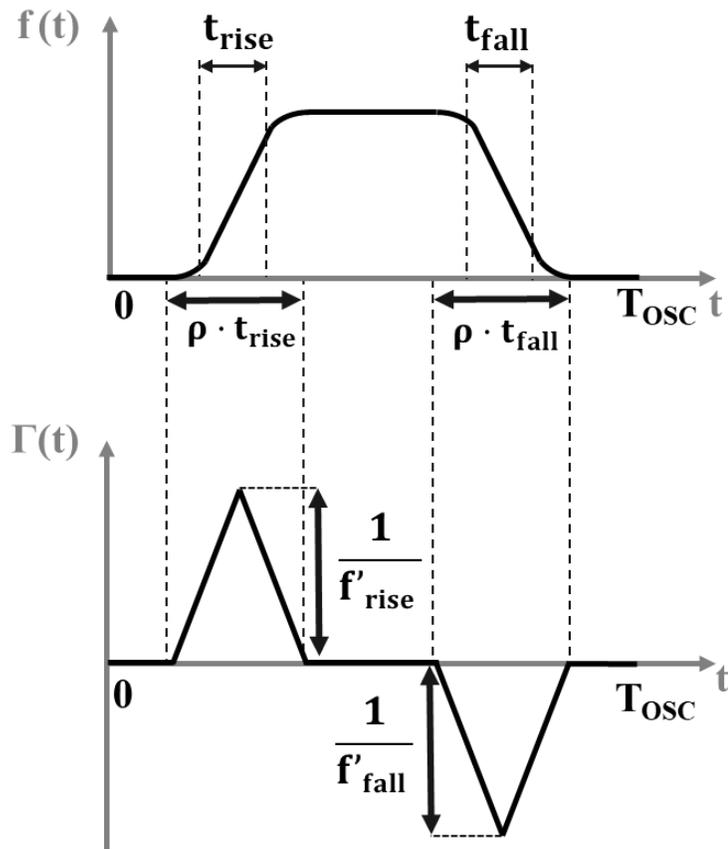


Figure 4.8: Detailed waveform and ISF representation of a typical ring oscillator.

The approximated ISF waveform of a ring oscillator is represented in Figure 4.8. The ISF waveform has two maximum values of  $1/f'_{rise}$  and  $1/f'_{fall}$  corresponding to the maximum slope during the rising and falling edge respectively. The widths of the triangles are approximated to

$\rho \cdot t_{\text{rise}}$  and  $\rho \cdot t_{\text{fall}}$  for the rising and falling edge, respectively. Adapted from the same approximations in [HAJ\_99], the rms ISF expression is given by:

$$\Gamma_{rms}^2 = \frac{4 \rho \pi^2}{3 \eta^3 M^3} \cdot \frac{1 + A^3}{(1 + A)^3} \quad (4.5)$$

where  $A$  is the ratio between the  $t_{\text{rise}}$  and  $t_{\text{fall}}$ ,  $\eta$  is a constant representing the proportional relation between the rise time and the propagation time. The constant  $\rho$  represents the portion between the rise time  $t_{\text{rise}}$  (or fall time  $t_{\text{fall}}$ ) to its total transition time. Details of this computation are given in Appendix C.

Then, the study in [HAJ\_99] highlights that the ISF function reaches a minimum for equality between the rise time and fall time values. Moreover, the ISF theory also states that the ring oscillator is sensitive to phase perturbation during its transition phase. As represented by the  $\rho$  parameter in the ISF expression, the ISF rms value is also minimized by reducing the total transition time. Therefore, another method to improve the phase noise performance of a RO is to minimize its transition times. In this way, a RO architecture is studied to verify the assumptions derived from the ISF theory.

#### 4.5 Pseudo-differential RVCO architecture

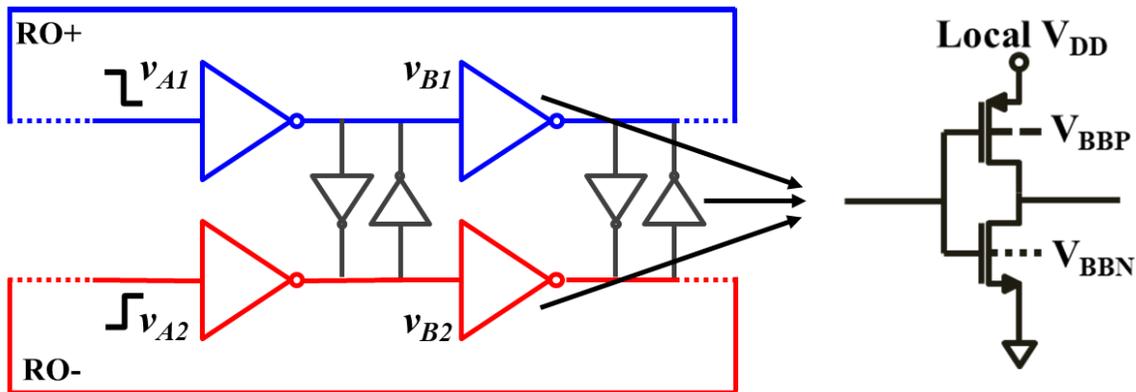


Figure 4.9: Pseudo-differential ring-oscillator architecture.

The Pseudo-differential ring-oscillator (PRVCO) is composed of  $M = 13$  identical stages regular single-ended inverter-based RVCOs in a pseudo-differential topology. As shown in Figure 4.9, each RVCO inverter is coupled from RO+ to its respective counterpart inverter RO- by two other inverters in a latch topology. The latches addition acts as a positive reaction, enforcing the two RVCOs to oscillate at the same frequency. The positive reaction shortens the transition time and imposes a phase opposition between RO+ and RO- outputs without using differential inverters. Finally, the pseudo-differential topology enables rail-to-rail output voltage swing unlike differential RVCO topology.

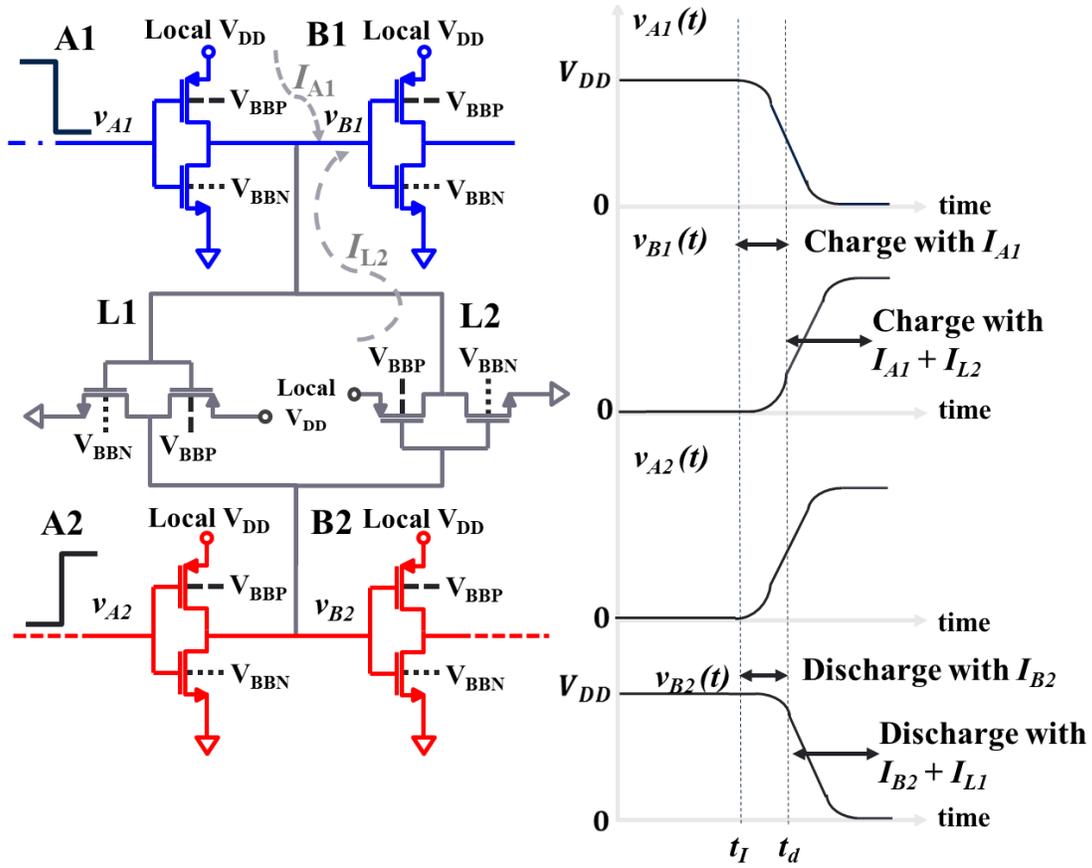


Figure 4.10: Pseudo-differential ring-oscillator architecture.

Figure 4.10 represents the transistor level view of a PRVCO. The B1 inverter input from RO+ is coupled with the B2 inverter input from RO-. Coupling is achieved by L1 and L2 inverters in a latch topology. It also illustrates the voltage transient curves of  $v_{A1}(t)$ ,  $v_{A2}(t)$ ,  $v_{B1}(t)$ , and  $v_{B2}(t)$ . From 0 to  $t_I$ , the current only flows through A1 drain until  $v_{B2}(t)$  reaches the threshold voltage of L2 Latch. After  $t_I$ , L2 Latch drives additional current which shortens the  $v_{B2}$  node charge.

From [ABI\_06], the propagation delay  $t_d$  can be integrated as:

$$\frac{V_{DD}}{2} = \int_0^{t_I} \frac{I_{inv}}{C} dt + \int_{t_I}^{t_d} \frac{I_{inv} + I_{latch}}{C} dt \quad (4.6)$$

where  $I_{inv}$  and  $I_{latch}$  are the averaged inverter and latch currents respectively, and  $C$  represents the sum of parasitic capacitances for a given node.

From (4.6), the oscillation frequency  $f_0$  of an  $M$ -stage PRVCO is expressed as:

$$f_0 = \frac{1}{M \cdot (t_{dN} + t_{dP})} = \frac{I_{inv} + I_{latch}}{M \cdot C \cdot (V_{DD} + (V_{TN} + V_{TP}) \cdot \frac{I_{latch}}{I_{inv}})} \quad (4.7)$$

where  $t_{dN}$  and  $t_{dP}$  are respectively the NMOS and PMOS propagation delays.  $V_{TN}$  is the NMOS threshold voltage,  $V_{TP}$  is the PMOS threshold voltage.

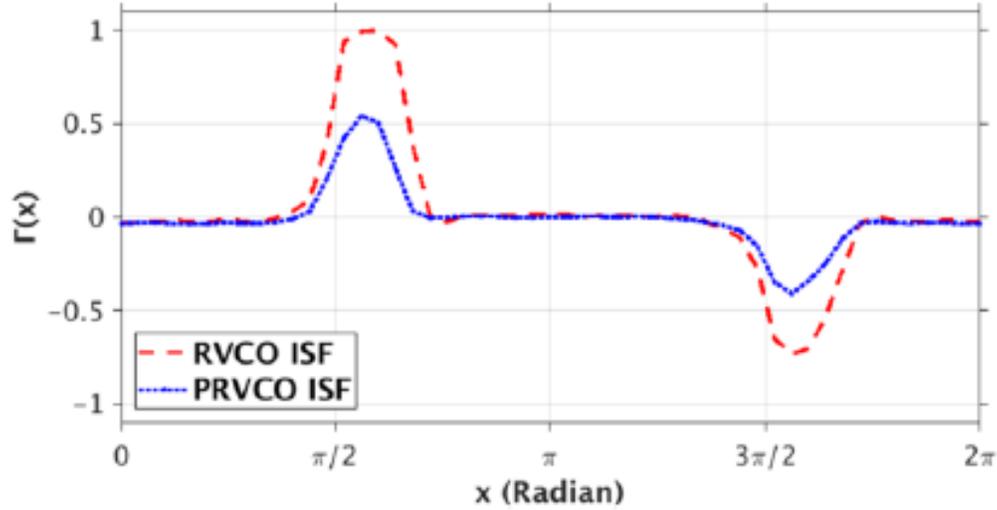


Figure 4.11: Impulse Sensitivity function comparison between the PRVCO and the inverter-based RVCO.

ISF Comparison of PRVCO and inverter-based RVCO is illustrated in Figure 4.11. As expected, the ISF waveform of the PRVCO is lower than its counterpart RVCO, indicating a reduced sensitivity to phase shift during the transition times. This confirms that the conversion of an optimized RVCO into its PRVCO counterpart is applicable to any RVCO topology to improve its immunity to phase perturbations, enhancing its phase noise performance.

A phase noise expression based on [ABI\_06] is derived to illustrate the contribution of the latch of the PRVCO architecture. The phase noise expression is based on the relationship between the jitter and the phase noise. The single-sided band of the phase noise  $\mathcal{L}(f)$  is expressed as a function of the spectral density of the period jitter by:

$$\mathcal{L}(f) = \sigma_{\tau}^2 \cdot \frac{f_0^3}{\Delta f^2} \quad (4.8)$$

Where  $f_0$  is the oscillation frequency,  $\Delta f$  is the offset frequency, and  $\sigma_{\tau}^2$  is the variance of the period jitter defined as:

$$\sigma_{\tau}^2 = M \cdot (\sigma_{t_{dN}}^2 + \sigma_{t_{dP}}^2) \quad (4.9)$$

Where  $M$  is the number of delay stages,  $\sigma_{t_{dN}}^2$  is the total period jitter contributed by the NMOS transistor and  $\sigma_{t_{dP}}^2$  is the total period jitter contributed by the PMOS.

Adapted from [ABI\_06], the PRVCO period jitter due to the white noise sources of the NMOS is:

$$\sigma_{t_{dN}}^2 = \frac{4k\gamma_N t_{dN}}{(I_{inv} + I_{latch}) \cdot (V_{DD} - V_{tN})} + \frac{kTC}{(I_{inv} + I_{latch})^2} \quad (4.10)$$

Thus, the phase noise expression for white noise source is then expressed using (4.9) and (4.10) as:

$$\mathcal{L}(f) = \left( \frac{2kT}{I_{inv} + I_{latch}} \right) \cdot \left( \frac{\gamma_N}{V_{DD} - V_{TN}} + \frac{\gamma_P}{V_{DD} - V_{TP}} + \frac{1}{V_{DD} + (V_{TN} + V_{TP}) \cdot \frac{I_{latch}}{I_{inv}}} \right) \cdot \left( \frac{f_0}{\Delta f} \right)^2 \quad (4.11)$$

where  $f_0$  is the carrier frequency and  $\Delta f$  is the offset frequency from the carrier. The latches current addition reduces the phase noise. If the latch current is null, we recover the same expression detailed in [ABI\_06]. The addition of latch improves the current and improves the phase noise performance. The two-phase noise theory confirms the expected phase noise improvement with a PRVCO topology.

Focusing on IoT applications, two PRVCO and regular RVCO architectures have been studied to evaluate their phase noise performance under the scope of two noise theories. The proposed Pseudo-differential architecture shows benefits to shorten the transition times to make it more immune to phase perturbations.

#### 4.6 RVCO and PRVCO implementation and measurements

Two structures are designed in 28nm UTBB FD-SOI technology to validate the phase noise improvement derived during the phase noise study. Regarding the PRVCO, all the transistors were designed with a length  $L = 90$  nm to achieve a good matching at RF frequencies around 2 GHz. Moreover, to ensure an optimum trade-off between phase noise and power consumption, the transistors used in ring-inverter and latch topology were designed with a width  $W = 2 \mu\text{m}$  and  $W = 500$  nm respectively for the NMOS transistors, and with widths of  $W = 4 \mu\text{m}$  and  $W = 1 \mu\text{m}$  respectively for the PMOS transistors as illustrated in Table 4A.

RO architecture	Pseudo-differential ring VCO		Regular ring VCO
	Inverter	Latch	Inverter
Length (nm)	110	100	90
NMOS width ( $\mu\text{m}$ )	0.5	2.0	2.1
PMOS width ( $\mu\text{m}$ )	1.0	4.0	4.2

Table 4A: Transistor parameters of PRVCO and regular RVCO.

The PRVCO is compared with a single-ended inverter-based RVCO composed of  $M = 13$  regular CMOS inverters. All the transistors were designed with a width of  $W = 2.1 \mu\text{m}$  for the NMOS transistors, with  $W = 4.2 \mu\text{m}$  for the PMOS transistors. To oscillate at the same frequency around 2 GHz, all the transistors were designed with a length of  $L = 110$  nm to compensate the node capacitance while achieving good matching at these RF frequencies. And so, the regular inverter-based RVCO is compared with its counterpart transformed into a PRVCO architecture. The inverted based RVCO is designed to achieve a power consumption of  $500 \mu\text{W}$  which directly asserts a total power consumption of the PRVCO around 1 mW.

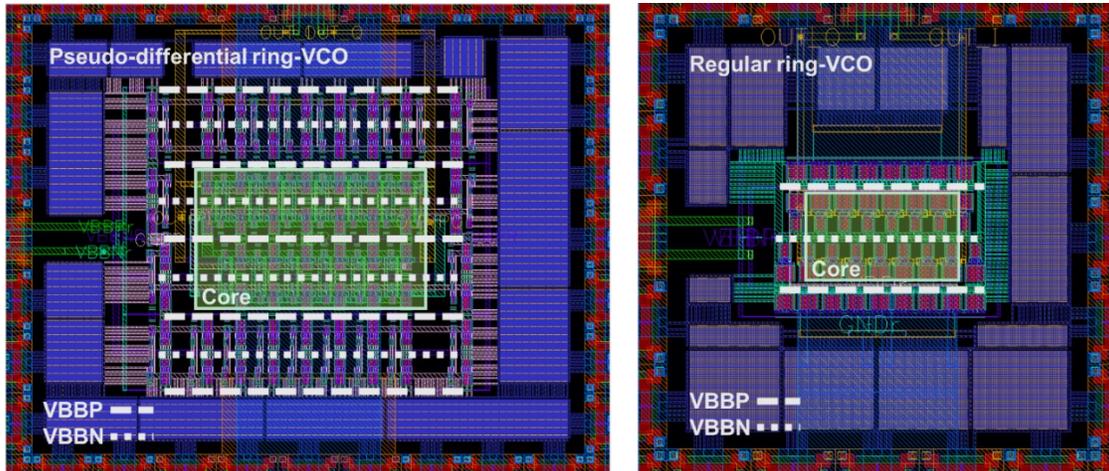


Figure 4.12: Layout of the pseudo-differential ring-oscillator and the regular ring oscillator architecture.

The Layout of the PRVCO and regular RVCO are represented in Figure 4.12. This enables to describe how the tuning strategy is realized. The same body-biasing voltage  $V_{BBN}$  is applied to all NMOS transistors. Similarly,  $V_{BBP}$  is applied to all PMOS transistors. For clarity purposes, the body-biasing voltage  $V_{BODY}$  implies  $V_{BBN} = -V_{BBP}$ . For instance,  $V_{BODY} = 1\text{ V}$  means  $V_{BBN} = -V_{BBP} = 1\text{ V}$ . By the addition of transistors all around the layout core, the common layout technique of “dummy transistors” is employed to ensure that the etching and the diffusion processes occur equally over all transistors composing the oscillator core.

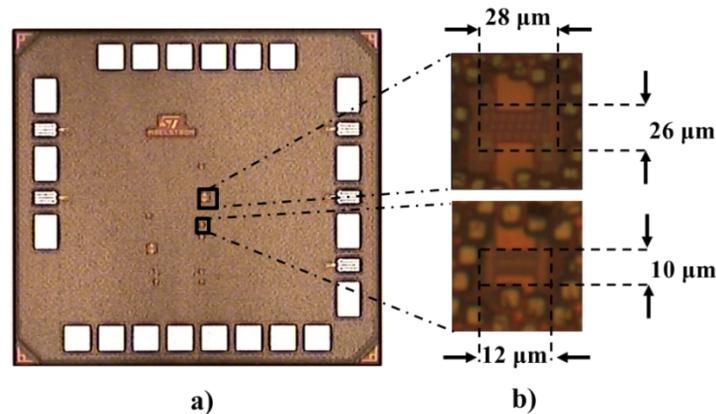


Figure 4.13: Chip photography (a) with (b) RVCOs localization and core area, (PRVCO up and inverter-based RVCO down).

The chip photomicrograph is shown in Figure 4.13. The PRVCO core area is  $28 \times 26\ \mu\text{m}^2$  while the inverter-based RVCO core area is  $12 \times 10\ \mu\text{m}^2$ . Under a 1 V typical local supply voltage, the PRVCO consumes 1.1 mW whereas the inverter-based RVCO consumes  $500\ \mu\text{W}$  at the same 1.7 GHz oscillation frequency. All the measurements are performed with a probe station, the output results are measured by a Rhode & Schwarz FSUP signal source analyzer. The low noise voltage sources from the signal source analyzer provide the supply voltage and the two body-biasing voltages  $V_{BBN}$  and  $V_{BBP}$ .

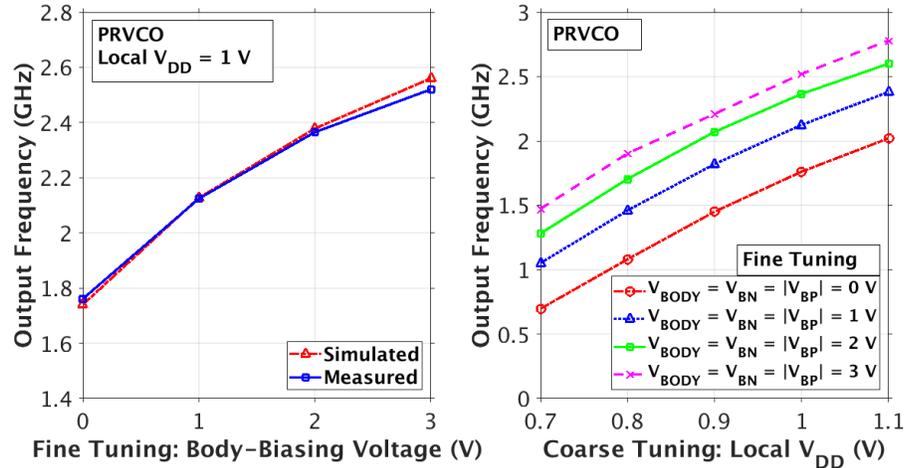


Figure 4.14: Pseudo-Differential ring VCO measured and simulated Frequency range (a) versus body-biasing tuning under 1 V local supply and (b) measured coarse tuning range versus supply voltage under body-biasing configurations.

PRVCO and inverted-based RVCO fine frequency tuning range versus body-biasing voltage are illustrated in Figure 4.14(a) and Figure 4.15(a) respectively. For the two RVCO architectures, simulation and measurement results are compared for a body-biasing between 0 V and 3 V. The PRVCO fine oscillator gain of 250 MHz/V allows a 35.4 % variation frequency under a typical 1 V local supply voltage.

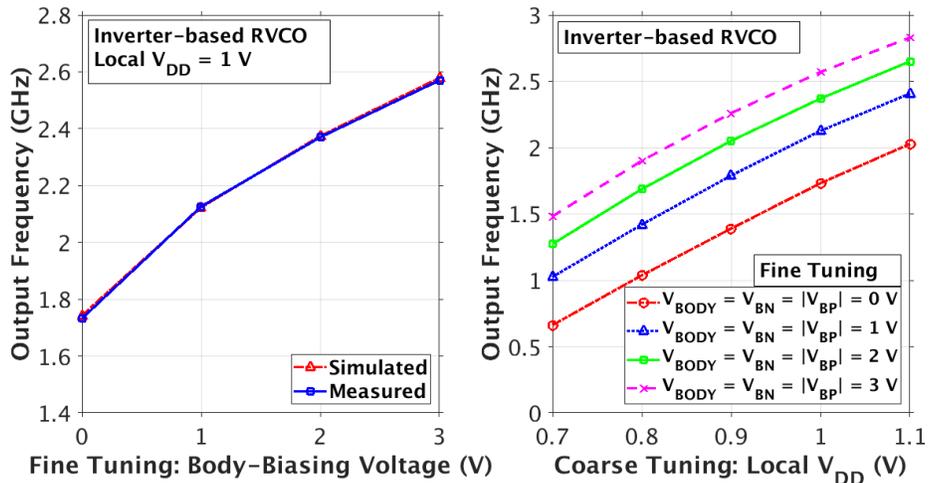


Figure 4.15: Inverter-based ring VCO measured and simulated Frequency range (a) versus body-biasing tuning under 1 V local supply and (b) measured coarse tuning range versus supply voltage under body-biasing configurations.

The PRVCO and inverter-based RVCO coarse frequency tuning range versus supply voltage are illustrated in Figure 4.14(b) and Figure 4.15(b) respectively, for different  $V_{BODY}$  values. The coarse tuning is performed by a local supply variation between 0.7 V and 1.1 V corresponding to a frequency tuning range between 0.7 GHz and 2.8 GHz. A wide Frequency Tuning Range (FTR) of 120 % is achieved for both topologies due to a robust and flexible design. High body-bias range is combined with oscillators' capability to sustain a low local VDD down to 0.7 V. Thus, a given target frequency can be obtained for different local VDD and body-biasing voltage couples. Hence, it opens a flexible and adaptive design capability.

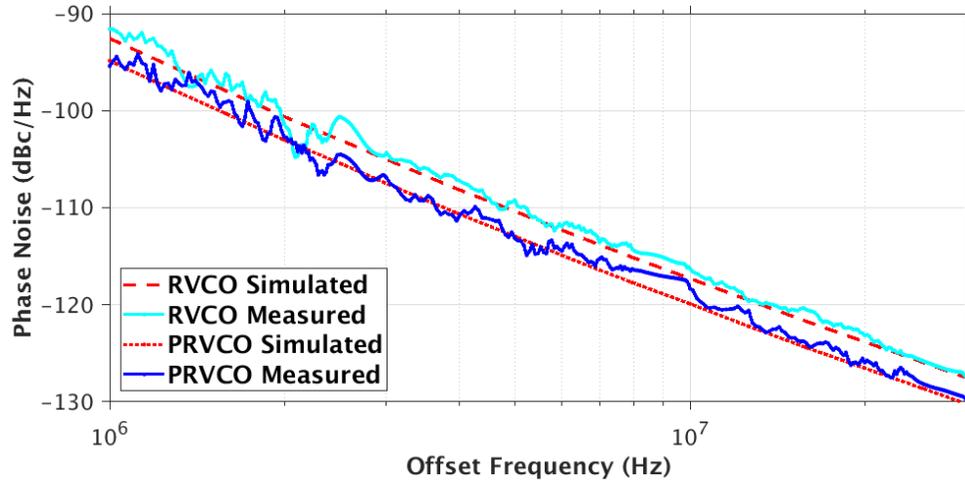


Figure 4.16: Measured and simulated phase noise for the PRVCO and the inverted-based RVCO architectures.

Figure 4.16 illustrates the phase noise under typical body biasing (local VDD = 1 V and  $V_{\text{BODY}} = 0$  V) for the two RVCO architectures. One can mention measurement results are in line with simulation results. A phase noise performance of  $-95.7$  dBc/Hz at 1 MHz offset frequency is measured for the PRVCO topology at 1.7 GHz. The PRVCO architecture achieves a 4 dB phase noise improvement compared with the inverter-based RVCO at the same oscillation frequency. This phase noise improvement validates the prediction from the architectural study. Thus, an extra phase noise improvement is expected by converting an optimized RVCO architecture into a PRVCO topology.

	This work		M. Kim et. al JSSC'16	L. Kong et. al JSSC'16	I. Sun et. al TCASSII'19	J. Yin et. al JSSC'16
Reference	[GAI 20]		[KIM 16]	[KON 16]	[SUN 19]	[YIN 16]
Topology	PRVCO	Single-ended RVCO	Current starved RVCO	Varactor RVCO	8-Phase FC-RVCO	35-Stage TI-RVCO
CMOS Technology	28nm CMOS FDSOI	28nm CMOS FDSOI	65nm CMOS	45nm CMOS	65nm CMOS	65nm CMOS
Output frequency (GHz)	1.76	1.73	1.6	2.39	3.11	3.47
Frequency range coarse (GHz)	0.7-2.78 (119.9 %)	0.7-2.83 (124.1 %)	1.2-2.0 (50 %)	2.0-3.0 (40 %)	2.68-3.56 (28.2 %)	1.7-3.47 (68.5 %)
Frequency range fine (GHz)	1.76-2.52 (35.4 %)	1.73-2.57 (38.7 %)	N.A	N.A	N.A	N.A
Supply voltage (V)	1.0	1.0	1.2	1.0	1.0	1.0
Power consumption (mW)	1.1	0.5	1.1	3.1	3.23	2.51
Phase Noise (dBc/Hz)	-95.7	-91.5	-79.1	-96.0	-95.1	-98.7
FoMosc  coarse (dBc/Hz)	160.7	159.8	142.8	158.7	159.9	165.5
FoMvco  fine (dBc/Hz)	171.6	171.6	N.A	N.A	N.A	N.A
Area ( $\mu\text{m}^2$ )	800	120	700	1000	1700	3000

Table 4B: Performance summary and comparison with GHz-ring oscillator state-of-the-art.

The PRVCO performance is summarized and compared with its single-ended counterpart and the relevant state-of-art in Table 4B. The proposed PRVCO improves the phase noise by more than a factor of two while exhibiting a State-of-the-Art FoM<sub>OSC</sub> (160.7 dBc/Hz). Moreover, the implementation of the dual coarse-fine frequency tuning method achieves a 120 % FTR and a 182.3 dBc/Hz FoM<sub>VCO</sub>. Finally, the fabricated chip respects the low consumption and the low area requirements of IoT applications.

## 4.7 Conclusion

This chapter presents the study of RVCO in FD-SOI technology. The first part is focused on an overview of RVCO characteristics. RVCO advantages such as low area or multiphase capability are confronted with the trade-off between power consumption and phase noise performance. This overview has confirmed that phase noise is the main challenge to tackle for RVCO targeting a low power consumption. Focused on the RVCO frequency tuning strategy, a new tuning method is presented. Using the body-biasing of the transistor back-gate, this unique frequency tuning method is only achieved in FD-SOI technology. Afterwards, the RVCO phase noise is studied under the scope of the ISF theory. This theory has determined that better phase noise is expected if the RVCO transition times are shortened. All the assumptions in terms of frequency tuning strategy and phase noise improvement have led to a RVCO topology proposition.

The second part of this chapter is dedicated to the study of the PRVCO topology. Composed of two ring-VCOs coupled by two other inverters in a latch topology, this architecture improves by more than a factor of two the ring-VCO phase noise performance. The PRVCO is implemented and compared to an inverter-based RVCO. The PRVCO latch positive feedback architecture gives an extra phase noise improvement by reducing the switching transition phases of a regular RVCO. Both ring-VCOs were implemented in 28nm FD-SOI CMOS technology from STMicroelectronics. Designed under a dual frequency tuning strategy, the two presented ring oscillators reach a very wide frequency tuning range. This strategy also offers two independent levers: the coarse tuning recovers the PVT variations while the fine-tuning controls the output frequency inside the PLL with a lower VCO noise sensitivity. The fine tuning is performed by the body-biasing feature which takes advantage of the FD-SOI technology integration. The Coarse-Fine tuning approach also proposes new disruptive designs, where two feedback loops are implemented in order to improve the VCO phase noise [DEV\_18].

The motivation of the RVCO study is to achieve efficient RVCO topologies in FD-SOI technology. The PRVCO topology studied in this chapter was presented at the 2020 ISCAS conference [GAI\_20], it achieves a 4dB phase noise improvement at the cost of twice the power consumption of its regular counterpart. However, both RVCO topologies promising performances for usage in low power compact IoT oscillators. In particular, the linear fine frequency tuning method which is enabled by the body-biasing feature of the FD-SOI technology, will be implemented in the Caliper PLL architecture. Given that the Caliper PLL deals with a very limited power budget which includes the two RVCOs, the chosen strategy is to implement the two loop oscillators with the single-ended RVCO topology to reach good RF performance for minimal power consumption.



# 5 Design Implementation of Caliper PLL Architecture

## 5.1 Introduction

This chapter is focused on the Caliper PLL design implementation studied in Chapter 3.

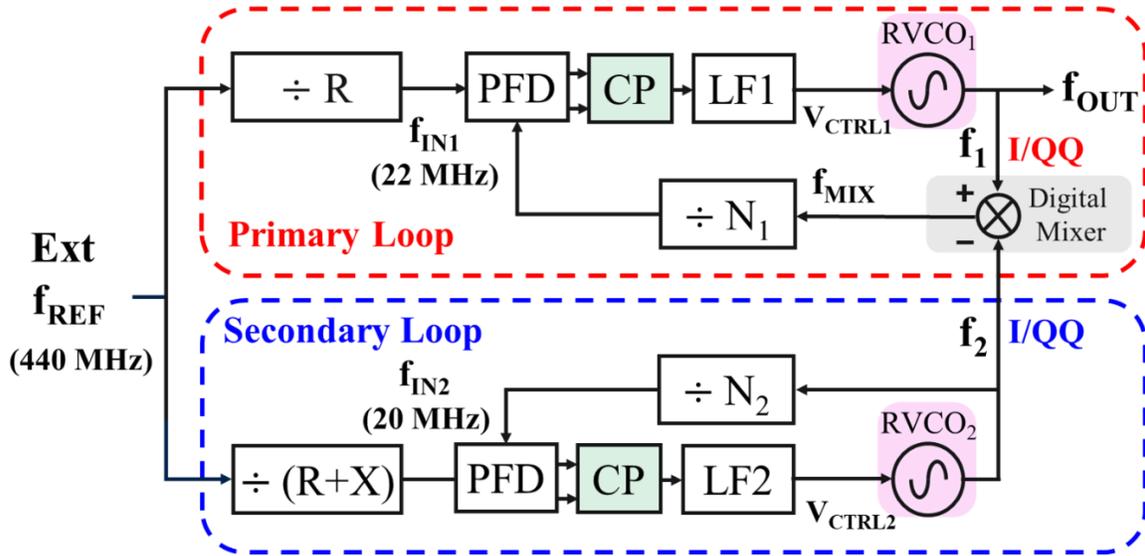


Figure 5.1: Caliper PLL architecture highlighting its innovative building blocks.

The first part of this chapter highlights designs of original blocs represented in Figure 5.1. Achieving minimal power consumption, ring oscillator design is presented using the body-biasing frequency tuning method discussed in Chapter 4. The ULP RVCOs provide quasi-quadrature inputs (I/QQ) of the digital mixer. Especially designed for the Caliper PLL, a fully digital down-frequency mixer is then proposed. The mixer does not require any passive filter to generate the  $f_{MIX}$  signal of frequency  $f_{OUT} - f_2$ . Proof of concept and measurement of the DFM are provided before its implementation inside the PLL. Then, a bootstrapped charge pump architecture is presented to ensure constant output current over the PLL frequency range. Finally, the other building blocks are introduced: The Phase-Frequency Detectors (PFD), the second-order transimpedance low-pass filters (LF1 and LF2) and the digital frequency dividers ( $R$ ,  $R+X$ ,  $N_1$ , and  $N_2$ ).

The second part of this chapter is dedicated to the physical implementation of the Caliper PLL in 28nm FD-SOI technology. Layout representation of each PLL building block is detailed, top-level layout strategy and layout techniques are discussed to provide robust and compact designs targeting industrial production. Finally, global simulations of the Caliper PLL architecture are presented to demonstrate the Caliper PLL transistor-level proof of concept.

## 5.2 Ring Voltage Controlled Oscillators

Two ring-oscillators are implemented inside the dual loop architecture of the proposed Caliper PLL. Power consumption below 1 mW is targeted for the overall PLL architecture with only half is dedicated for the ring-oscillators. Based on the conclusions of Chapter 4, the single-ended inverter-based ring oscillator topology is chosen due to its good trade-off between phase noise performance and power consumption.

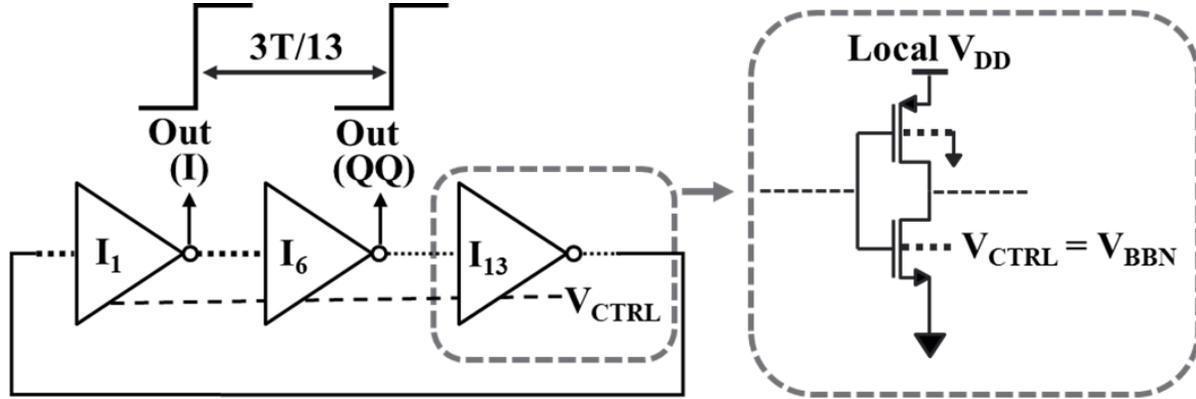


Figure 5.2:  $N = 13$  Single-ended CMOS inverter-based Ring Oscillator topology.

As illustrated in Figure 5.2, both loops of the proposed PLL contain the same single-ended inverter-based ring oscillator (RO) architecture. Each RO is composed of  $N = 13$  delay cells implemented with classic CMOS inverters. The simple RO topology achieves minimal consumption and area, but it is not able to generate quadrature signals which can be used in the mixer architecture. Here, the RO generates quasi-quadrature outputs (I and QQ) represented by a relative delay of  $3T_{osc}/13 = 0.23 \cdot T_{osc}$  where  $T_{osc}$  represents the period of oscillation. Thus, a new solution is developed to propose a mixer architecture that uses the quasi-quadrature inputs from the ROs.

The RO fine frequency tuning is controlled by body-biasing the transistors' back gate. This unique feature of the UTBB FD-SOI technology varies the transistor threshold voltage ( $V_T$ ) to control the RO frequency [CAT\_17]. The RO control voltage ( $V_{BBN}$ ) is applied in parallel to all the 13 NMOS LVT transistors. In order to simplify the physical implementation and deal only with positive voltages, the RVCO is controlled only on the NMOS transistors' body ties. Indeed, the PMOS LVT transistors' body-biasing requires a negative voltage which is complicated to handle. By only controlling the NMOS transistors, a lower frequency tuning slope, or oscillation gain  $K_{VCO}$  is expected. Verified in simulation, the frequency range is enough to cover the BLE bands between 2.4 GHz and 2.48 GHz.

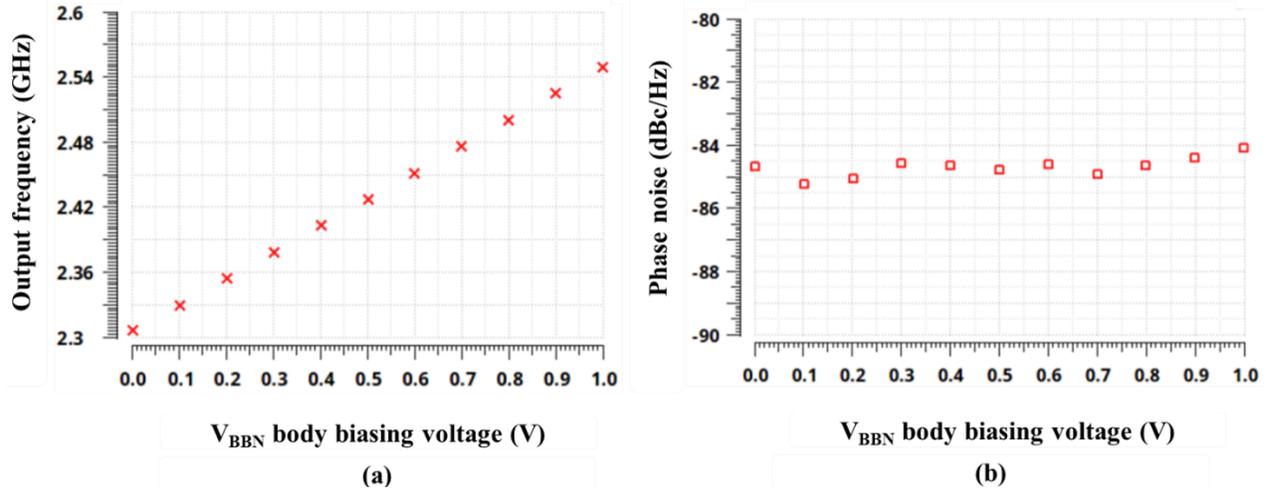


Figure 5.3: Simulated RVCO<sub>1</sub> frequency tuning range versus body-biasing tuning (a) and (b) simulated RVCO<sub>1</sub> phase noise performance at 1 MHz offset frequency versus body-biasing tuning.

The primary loop RVCO<sub>1</sub> simulated frequency tuning range versus body-biasing voltage is illustrated in Figure 5.3(a). For a V<sub>B<sub>BN</sub></sub> variation of 1 V, the output frequency varies between 2.3 GHz and 2.55 GHz, giving a linear frequency tuning slope of 250 MHz/V. Thus, the RVCO<sub>1</sub> can cover the BLE bands and it verifies that the NMOS back-gates' control is enough for the Caliper PLL application. Moreover, the RVCO<sub>1</sub> power consumption varies between 282 μA and 317 μA for the same V<sub>B<sub>BN</sub></sub> variation. Achieving a mean power consumption value of around 300 μA, the body-biasing frequency tuning method has a limited impact on the RO power consumption.

The primary loop RVCO<sub>1</sub> simulated phase noise performance at 1 MHz offset frequency versus body-biasing voltage is illustrated in Figure 5.3(b). The 300 μW RVCO<sub>1</sub> phase noise performance shows only a 1.13 dB variation around the mean value of -84.7 dBc/Hz. Thus, RVCO<sub>1</sub> achieves a robust phase noise performance among the overall PLL frequency range. Furthermore, the body biasing feature, unique to FD-SOI technology, enables this new frequency tuning knob over this very simple, compact, power-efficient, and robust RO topology.

## 5.3 Mixer

### 5.3.1. Digital Down-conversion Frequency Mixer (DFM)

A mixer is a three-port circuit that performs the function of frequency translation in wireless communication systems. An ideal mixer is a frequency multiplier that produces an output consisting of the sum and difference frequencies of the two input signals. The ideal behavior of the mixer is expressed by:

$$v_{MIX}(t) = A \cos(\omega_1 t) \cdot B \cos(\omega_2 t) = \frac{AB}{2} (\cos((\omega_1 - \omega_2)t) + \cos((\omega_1 + \omega_2)t)) \quad (4.12)$$

Usually, one of the output signals is preserved by using a selective filter. The non-idealities of the mixer create many harmonics as well as undesired mixing products of the two inputs signals. To remove the unwanted harmonics, selective filters are also placed at the input and output ports of the mixer to select only the frequency of interest. These filters are generally made by passive components such as resistors and capacitors which compose a high part of the mixer area. An upconverter mixer is used in a transmitter to shift the data signal from a low frequency to the carrier frequency for its transmission through the antenna. A down-converter mixer is used in a receiver to separate the data signal from the carrier by shifting it to a low frequency.

The proposed mixer used in the Caliper PLL architecture does not act as a classical mixer. The mixer input signals are the two signals from the RVCOs of the primary and secondary loop (of frequency  $f_1$  and  $f_2$ ). In the context of our proposed PLL architecture, the mixer provides an output signal with the difference frequency  $f_1 - f_2$  in the feedback loop of the primary loop.

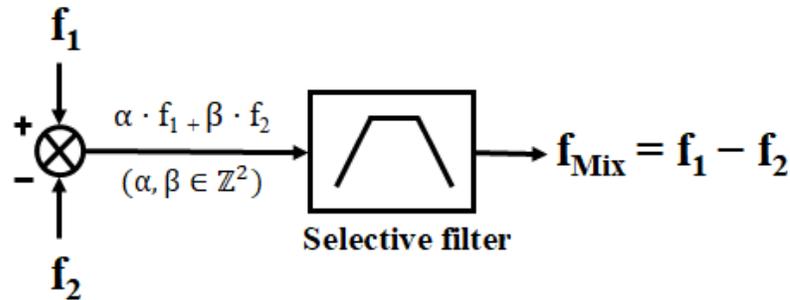


Figure 5.4: Classical mixer representation with digital input signals.

As the input signals are periodic square waves (i.e. digital signals), the mixer creates all the mixing products from the combination of the odd harmonic frequencies from the two inputs. As represented in Figure 5.4, these unwanted mixing products are commonly filtered through a selective band-pass filter which selects the desired output frequency  $f_{MIX}$ .

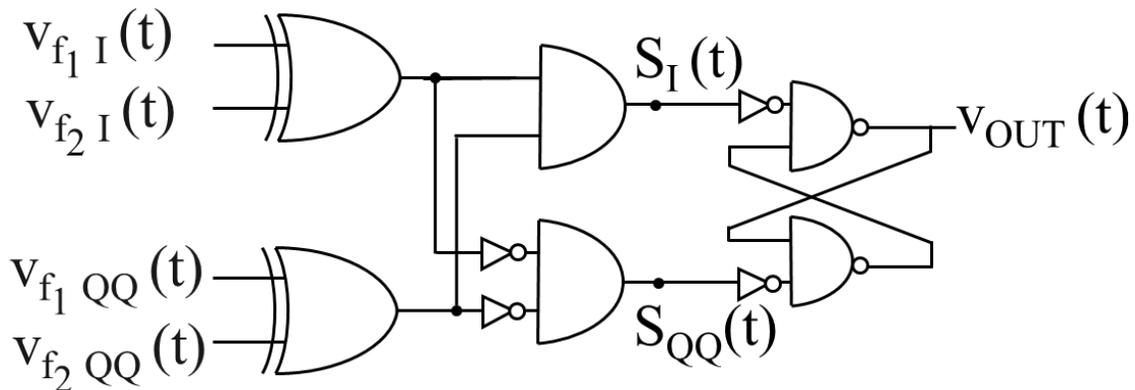


Figure 5.5: Proposed difference frequency mixer (DFM) circuit.

Based on a fully digital architecture illustrated in Figure 5.5, the proposed Down-conversion Frequency Mixer (DFM) produces the output signal  $V_{OUT}(t)$  with the wanted frequency

$f_{\text{MIX}} = f_1 - f_2$  without using any extra passive filter. The mixer area is reduced which is compliant with an IoT design guideline.

The theory of the proposed mixer normally requires quadrature inputs (I/Q) from the oscillator, produced by additional circuits based on fully differential oscillators [LI\_10] or polyphase filters [BEH\_01]. In order to reduce more the power consumption and the area of the mixer, the proposed down-converter mixer uses quasi-quadrature inputs (named I and QQ) from the ring oscillators ( $v_{f1}(t)$  and  $v_{f2}(t)$ ) with respectively  $f_1$  and  $f_2$  frequencies. For instance, the quasi-quadrature digital signals from the RVCO<sub>1</sub> can be expressed as:

$$v_{f1\ I}(t) = A \cdot \sum_{i=0}^n \frac{\cos((2i+1)\omega_1 t)}{2i+1} \quad (5.1)$$

$$v_{f1\ QQ}(t) = A \cdot \sum_{i=0}^n \frac{\cos((2i+1)\omega_1 t + \theta)}{2i+1} \quad (5.2)$$

where A is the signal amplitude,  $\theta$  represents the quasi-quadrature phase delay close to  $\pi/2$ . The quasi-quadrature inputs from the RVCO<sub>2</sub> share the same expressions with a  $\omega_2$  frequency.

To clearly explain the philosophy of the proposed mixer, we consider quadrature inputs from the oscillators ( $\theta = \pi/2$ ) with a first-order approximation ( $n = 0$ ) as:

$$v_{f1\ I}(t) = A \cos(\omega_1 t) \quad (5.3)$$

$$v_{f1\ QQ}(t) = -A \sin(\omega_1 t) \quad (5.4)$$

$$v_{f2\ I}(t) = A \cos(\omega_2 t) \quad (5.5)$$

$$v_{f2\ QQ}(t) = -A \sin(\omega_2 t) \quad (5.6)$$

The XOR gate is modeled as a multiplier, the AND gate is modeled as an adder and the NOT gate is modeled by a phase shift of  $\pi$  radians. Thus, two signals  $S_I$  and  $S_{QQ}$  are modeled by:

$$S_I(t) = A^2 \cdot [\cos(\omega_1 t) \cos(\omega_2 t) + \sin(\omega_1 t) \sin(\omega_2 t)] = A^2 \cdot [\cos((\omega_1 - \omega_2)t)] \quad (5.7)$$

Based on the same calculus, the other intermediate signal  $S_Q$  is also expressed as:

$$S_{QQ}(t) = A^2 \cdot [\cos(\omega_1 t + \pi) \cos(\omega_2 t + \pi) + \sin(\omega_1 t + \pi) \sin(\omega_2 t + \pi)] \quad (5.8)$$

which gives:

$$S_I(t) = S_{QQ}(t) = A^2 \cdot [\cos((\omega_1 - \omega_2)t)] \quad (5.9)$$

Within the first order model, the main frequency of  $S_I$  and  $S_{QQ}$  is the difference frequency  $f_1 - f_2$ . The RS latch is modeled to synchronize the two  $S_I$  and  $S_{QQ}$  signals to generate the output

signal  $f_{\text{MIX}}$  with the wanted difference frequency. In practice, the DFM works with periodic square waves as in (5.1).

The same calculus with  $n = 1$  gives the mixing products due to the odd harmonic frequencies. For instance, the expression of the signal  $S_I$  (for  $n = 1$ ) is given by:

$$S_I(t) = A^2 \cdot \left[ \cos((\omega_1 - \omega_2)t) + \frac{\cos(3(\omega_1 - \omega_2)t)}{9} + \frac{\cos((3\omega_1 - \omega_2)t)}{3} + \frac{\cos((\omega_1 - 3\omega_2)t)}{3} \right] \quad (5.10)$$

In the first order, the frequency of the  $S_I$  and  $S_Q$  is the one expected while including the other mixing products. Acting as a low pass filter the RS latch enforces the  $f_1 - f_2$  frequency component.

We are considering now quasi-quadrature input signals with a phase delay  $\theta$  close to  $\pi/2$ . Thus, the four input signals are expressed with a first-order approximation ( $n = 0$ ) by:

$$v_{f1}(t) = A \cos(\omega_1 t) \quad (5.11)$$

$$v_{f1\text{QQ}}(t) = A \cos(\omega_1 t + \theta) \quad (5.12)$$

$$v_{f2}(t) = A \cos(\omega_2 t) \quad (5.13)$$

$$v_{f2\text{QQ}}(t) = A \cos(\omega_2 t + \theta) \quad (5.14)$$

Detailed in Appendix D, the same computations than (5.8) and (5.9) give the expression for the dominant tone of the intermediate signal  $S_I(t)$  as:

$$S_{I(t)} = A^2 [\cos((\omega_1 - \omega_2)t) + \cos(\theta) \cdot \cos((\omega_1 + \omega_2)t + \theta)] \quad (5.15)$$

For a phase delay  $\theta$  close to  $\pi/2$ , the dominant  $S_I$  signal is the difference  $f_1 - f_2$  frequency. Thus, the DFM mixer can theoretically use the quasi-quadrature inputs from the two RVCOs. However, the DFM has to be verified by simulation.

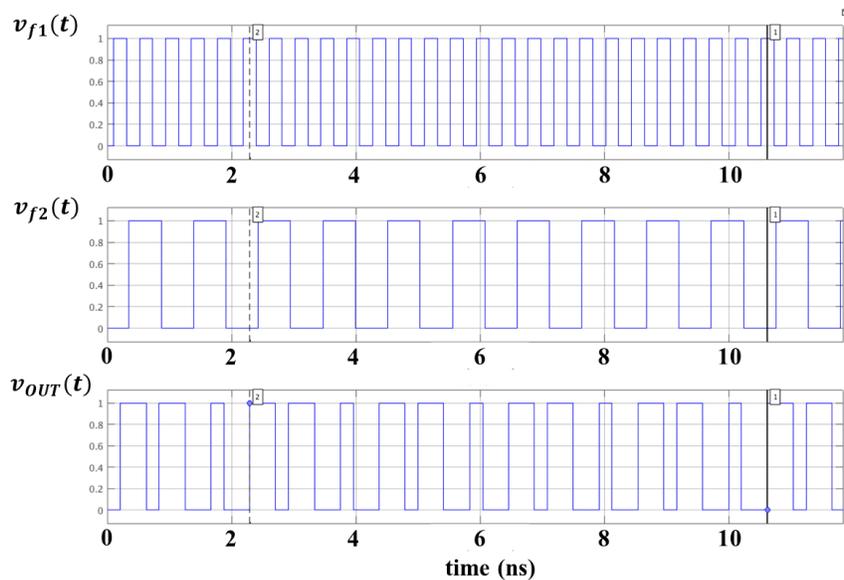


Figure 5.6: Simulated transient waveforms of the mixer input and output signals.

Based on ideal logic blocks, the DFM architecture is simulated through MATLAB Simulink software. The two inputs signals have the frequencies of  $f_1 = 2400$  MHz and  $f_2 = 960$  MHz. In Figure 5.6, the average output frequency is shown over twelve periods which gives  $f_{\text{MIX}} = 1440$  MHz. As expected, the quasi-quadrature impacts the DFM behavior. We can observe that the DFM instantaneous frequency fluctuates around the average frequency  $f_1 - f_2$ . However, this simulation is based on ideal logic building blocks. Non-idealities such as propagation delays of the logic gates have to be considered to verify the feasibility of the proposed mixer. Thus, a transistor-level simulation is mandatory to establish the architectural proof of concept.

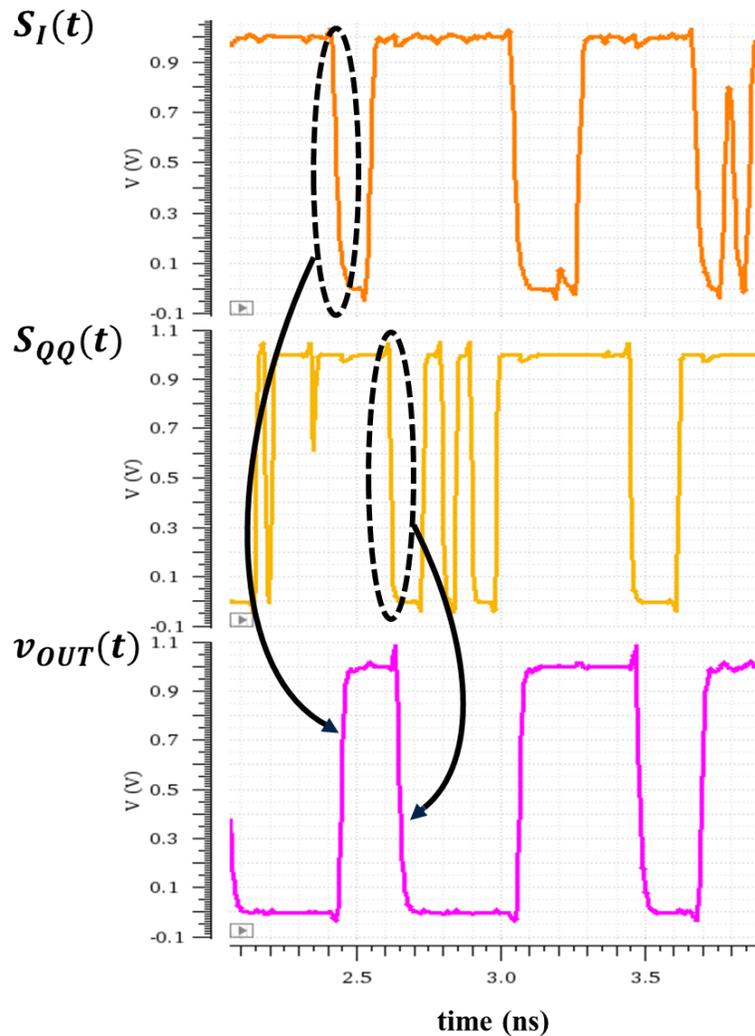


Figure 5.7: Simulated internal signals  $S_I$  and  $S_{QQ}$  waveforms and the mixer output signal.

A transistor-level simulation under Cadence Spectre software is illustrated in Figure 5.7 where the intermediate signals  $S_I$  and  $S_{QQ}$  and the output signal  $v_{\text{OUT}}$  are represented. Highlighted

in Figure 5.7, one can observe that the falling edge of signal  $S_I$  acts as a positioning signal and the next falling edge of signal  $S_{QQ}$  acts as a reset signal to shape the output signal  $v_{OUT}$ .

Due to this behavior, the duty-cycle of the  $v_{OUT}$  signal is not constant. Furthermore, the output signal of the mixer presents an instantaneous frequency that fluctuates around the average frequency  $f_1-f_2$ . The digital mixer is still compliant with the PLL requirements because the divided-by- $N1$  feedback divider is based on an edge-counter that divides the average frequency over  $N1$  periods. Thus, the frequency divider combined with the PLL loop filter acts as another selective filter to ensure the PLL locking on the  $f_1-f_2$  frequency.

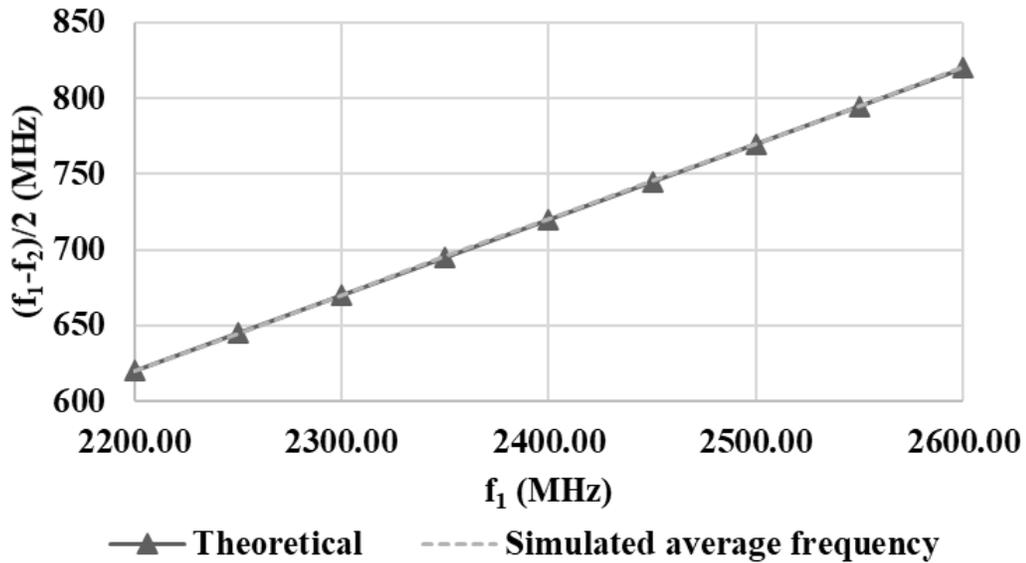


Figure 5.8: Simulated divided-by-2 mixer output frequency under  $f_1$  frequency variation.

The DFM is simulated with  $f_1 = 2.20$  GHz and  $f_2 = 960$  MHz, the output signal  $v_{OUT}$  is divided by 2 by a D-Flip-Flop to verify the precedent assumption. Moreover, the  $f_1$  frequency is tuned between 2.20 GHz and 2.60 GHz to check the DFM ability to track frequency variation. The average  $(f_1-f_2)/2$  frequency is represented in Figure 5.8. One can notice that the simulated results are in line with the theoretical results. The DFM proof of concept is then verified by architectural and transistor-level simulations. The fully digital architecture of the proposed DFM and its capability to perform with quasi-quadrature inputs reduces its impact in terms of area and power consumption once implemented inside the PLL.

### 5.3.2 DFM implementation and measurements

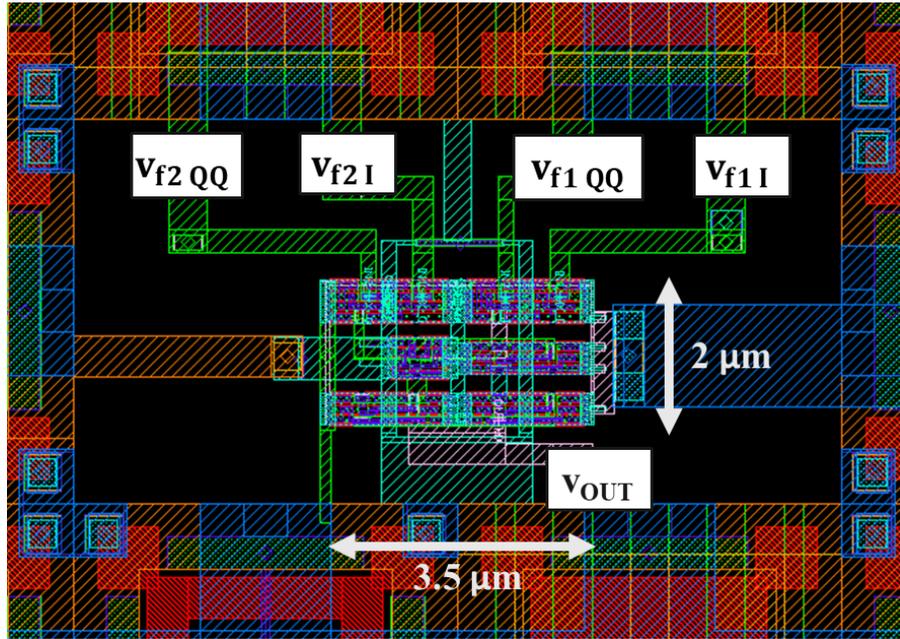


Figure 5.9: Layout of the DFM prototype.

The prototype of the digital mixer is realized by using digital standard cells dedicated to digital building blocks. As represented in Figure 5.9, the area of the proposed digital mixer is  $7 \mu\text{m}^2$ . The prototype of the digital mixer is measured under the same measurement set-up as the ring-oscillator test-structures of Chapter 4. Besides, the mixer receives the quasi-quadrature (I and QQ) inputs signals from the single-ended RO architectures presented in the previous section. Thus, the non-idealities from the input signals are considered during the measurement of the mixer performance.

VDD (V)	V <sub>BODY</sub> (V)	f <sub>MIX</sub> (MHz)	f <sub>1</sub> (MHz)	f <sub>2</sub> (MHz)	f <sub>1</sub> -f <sub>2</sub> (MHz)
1	0	950	1496	546	950
	0.5	1057	1674	619	1055
	1.0	1151	1839	687	1152
	1.5	1215	1944	729	1215
	2.0	1270	2037	769	1268
	2.5	1319	2124	806	1318
	3.0	1364	2203	840	1363

Table 5A: Measured DFM frequency performance under input frequencies variation.

The measured mixer output frequency and the input frequencies are represented in Table 5A. Inside the proposed PLL, the DFM needs to follow the dynamical frequency variations of its inputs. This property is measured by tuning the input frequencies and the measured mixer output frequency is compared to its theoretical value. Despite the non-idealities of the implemented

prototype, the measured frequency verifies the assumption that the DFM can track the input frequencies to produce the output frequency relation  $f_1 - f_2$  over the tuning range.

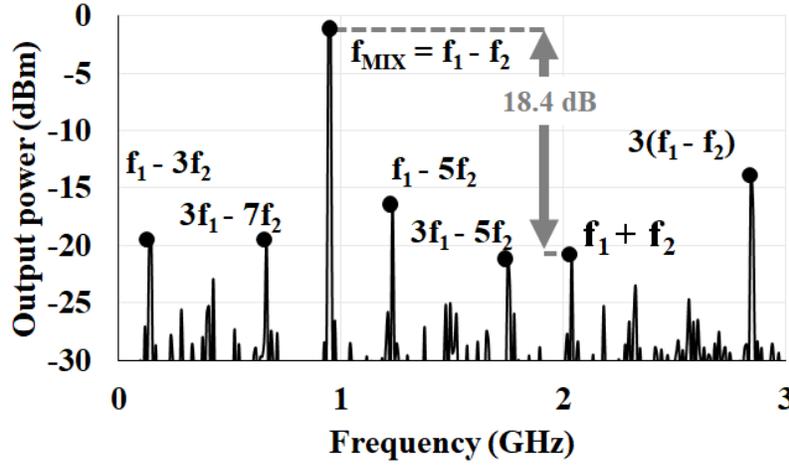


Figure 5.10: Measured DFM output spectrum for  $f_1 = 1.496$  GHz and  $f_2 = 546$  MHz.

The DFM is then measured with two quasi-quadrature inputs of  $f_1 = 1496$  MHz and  $f_2 = 546$  MHz frequencies. The output spectrum is represented in Figure 5.10 where the dominant difference frequency  $f_1 - f_2$  has the most significant amplitude to be retrieve from the other mixer products. Using the amplitudes of  $S_1(t)$  and  $S_{QQ}(t)$  signals in (5.15), the power difference between the  $f_1 - f_2$  and  $f_1 + f_2$  tones is calculated by:

$$P_{f_1 - f_2} - P_{f_1 + f_2} = 10 \log \left( \left( \frac{A^2}{A^2 \cdot \cos(\theta)} \right)^2 \right) \quad (5.16)$$

$$P_{f_1 - f_2} - P_{f_1 + f_2} = 10 \cdot \log \left( \frac{1}{\cos^2(\theta)} \right) = 18.4 \text{ dB} \quad (5.17)$$

where  $\theta = \frac{6\pi}{13}$  is the radian value of the quasi-quadrature relation. This value has been verified through measurement as highlighted in Fig. 5.10. It confirms that the first-order approximation is sufficient to validate the digital mixer operation. As input signals are square wave signals, mixing products are created between the harmonic frequencies of  $f_1$  and  $f_2$ . Represented in Fig. 5.10, the measured frequency of each tone matches the expected parasitic frequency. Exact amplitude of the other parasitic spurs should be calculated with the complete mathematical formulas taking into consideration the  $\sin(x)/x$  amplitude functions. However, these spurs are considered negligible as their amplitude is lower than the one of the third harmonic  $3(f_1 - f_2)$ . To reduce the area of the PLL, no additive band-pass filter is added. The residual mixing products around the difference frequency  $f_1 - f_2$  are directly filtered by the combination of the frequency divider and the PLL loop filter.

### 5.3.3 DFM implementation inside the Caliper PLL

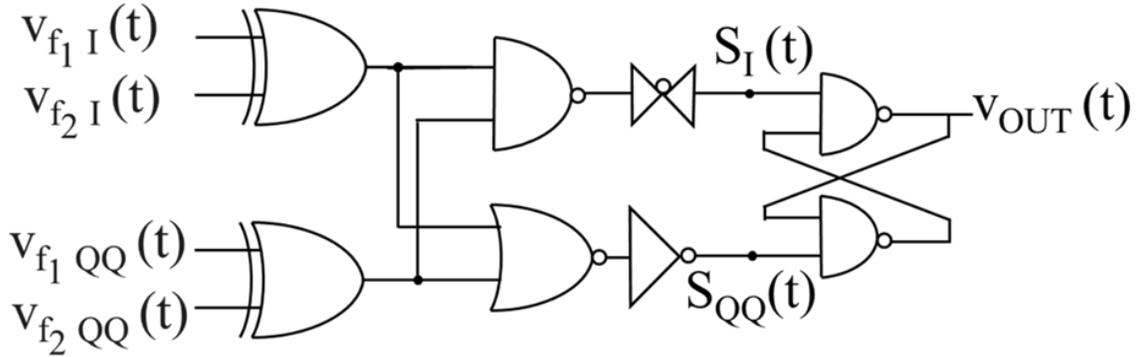


Figure 5.11: Schematic representation of the implemented digital mixer.

Illustrated in Figure 5.11, the digital mixer architecture is transformed using logic gate equivalence. For instance, the AND gate with NOT gates at its inputs is transformed into a NOR gate. A pass-gate is also added to equalize the propagation times inside the logic gates, it ensures an equivalent phase delay between the two signals  $S_I(t)$  and  $S_{QQ}(t)$  than the inputs signals  $v_{f1}(t)$  and  $v_{f2}(t)$ .

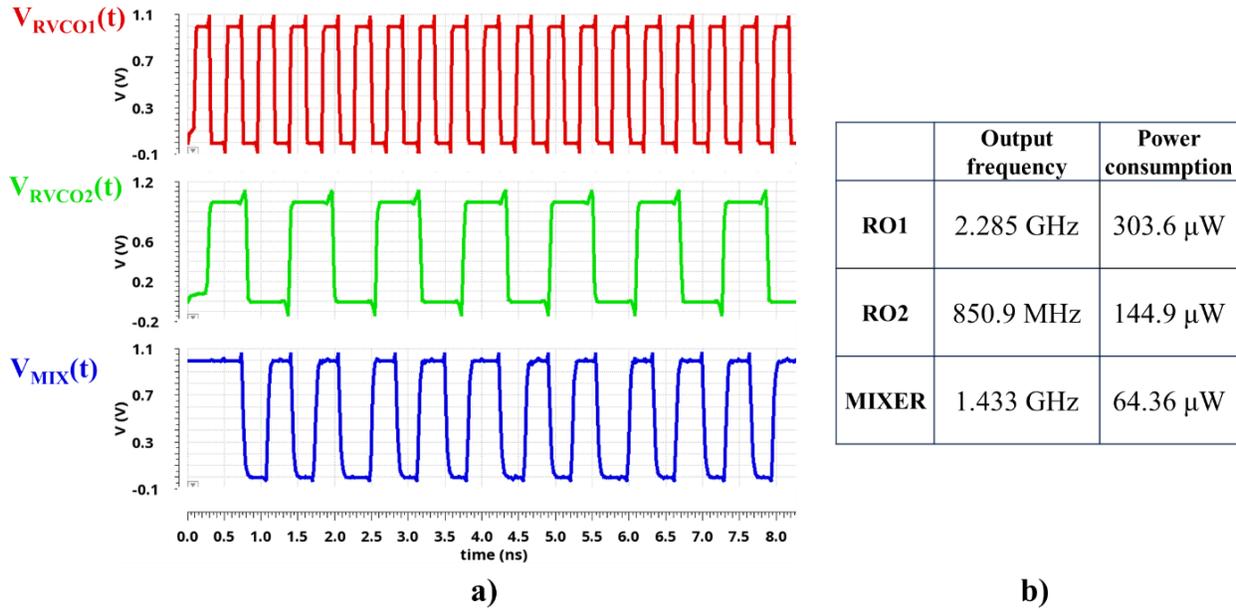


Figure 5.12: Transient simulation of the RVCOs and mixer (a) and (b) associated simulated performances.

The association of the two ring-oscillators and the digital mixer are simulated after parasitic extractions. Represented in Figure 5.12, the transient simulation enables the verification of the frequency relation between the mixer output and the two oscillators inputs under a typical 1 V supply voltage. The power consumption of the three RF parts represents half of the targeted power consumption for the total PLL architecture.

### 5.3.4 Conclusion

The proposed digital Down-conversion Frequency Mixer (DFM) generates only the difference frequency  $f_{\text{MIX}} = f_1 - f_2$  without the use of an extra filter. The study of the proposed mixer enables the use of the quasi-quadrature inputs (I and QQ) from the RVCOs. Furthermore, the DFM study determines that the frequency divider can be combined with the PLL loop filter to act as another selective bandpass filter. Thus, only the  $f_1 - f_2$  frequency can be extracted from the mixer output signal.

A prototype is implemented in 28nm FD-SOI CMOS technology from STMicroelectronics, the input signals of the mixer are generated from ring-oscillators implemented in the same test chip. The test case is the following: the ring-oscillators are providing quasi-quadrature signals (I and QQ) with a phase delay close to  $\pi/2$ . It enables to test the mixer behavior in a realistic configuration. Nevertheless, the feasibility of the mixer architecture is validated by measurement. Measurement results in terms of output frequency spectrum enable the use of the proposed digital mixer inside the Caliper PLL. In addition, its fully digital architecture, and its capability to operate with quasi-quadrature inputs reduces its impact in terms of area and power consumption once implemented inside the Caliper PLL.

## 5.4 Charge Pump

### 5.4.1 Charge pump challenge

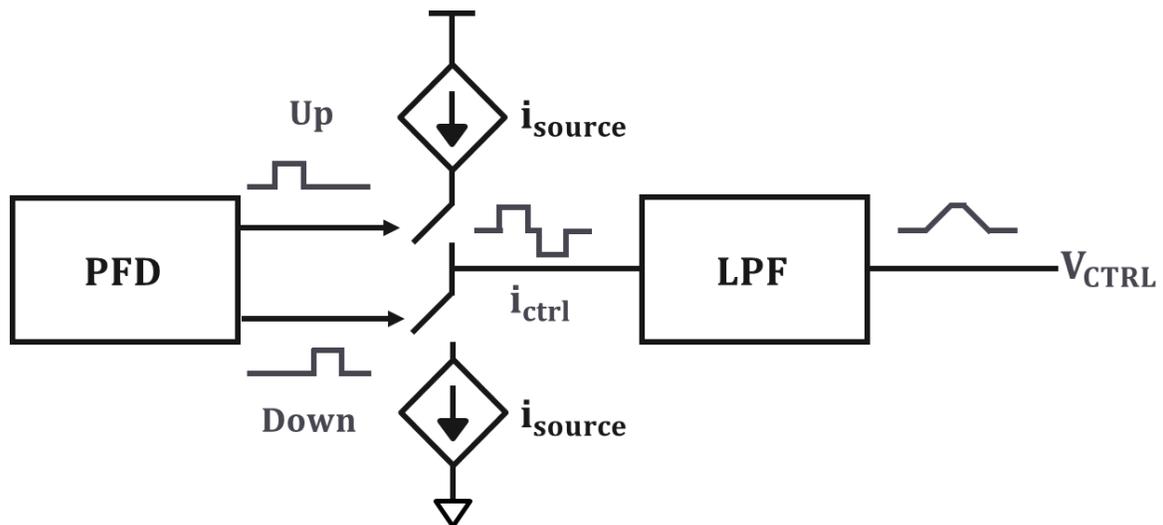


Figure 5.13: General representation of a charge pump principle.

Illustrated in Figure 5.13, the purpose of a charge pump building block is to transform the control pulses (Up and Down) from the Phase-Frequency Detector (PFD) into current pulses. These current pulses are injected into the low pass filter (LPF) and thus, transformed into the control

voltage of the oscillator ( $V_{CTRL}$ ). The ideal charge pump representation is comprised of two current sources ( $i_{source}$ ) and two switches controlled by the Up and Down signals.

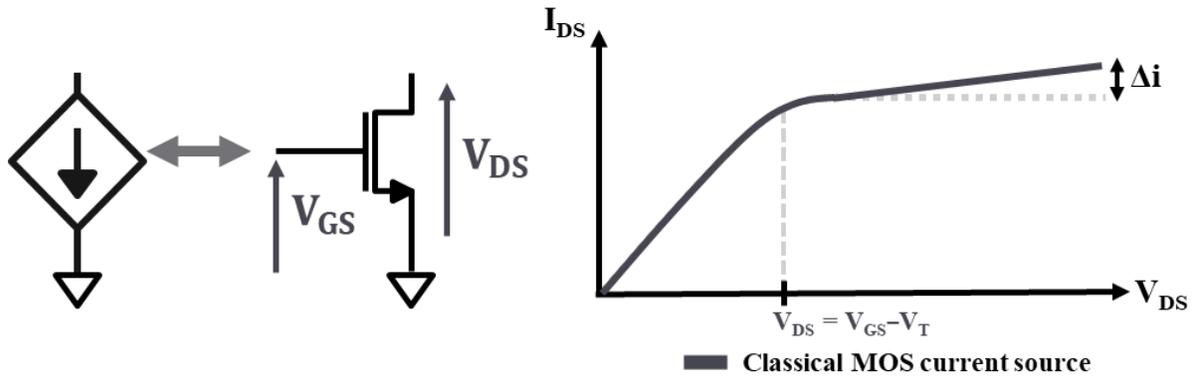


Figure 5.14: Current drift in transistor-based current source.

The main challenge of a charge pump design concerns the current source. Indeed, an ideal charge pump is composed of two equal current sources. A current source based on a MOS transistor is illustrated in Figure 5.14 where the current is set by the  $V_{GS}$  voltage of the transistor. However, the channel length modulation effect creates a current drift, degrading the current matching between the two current sources. Indeed, the  $i_{ds}$  current drifts according to the  $V_{DS}$  voltage value as represented in Figure 5.14. For instance, the  $V_{DS}$  voltage of the current source follows the  $V_{CTRL}$  voltage variation. Depending on the  $V_{CTRL}$  value, a mismatch between the two current sources causes a current leakage which is transmitted into the filter. This section proposes a charge pump architecture called bootstrapped charge pump which controls the current value over the variations of the output voltage  $V_{CTRL}$ .

### 5.4.2 Proposed Bootstrapped current source

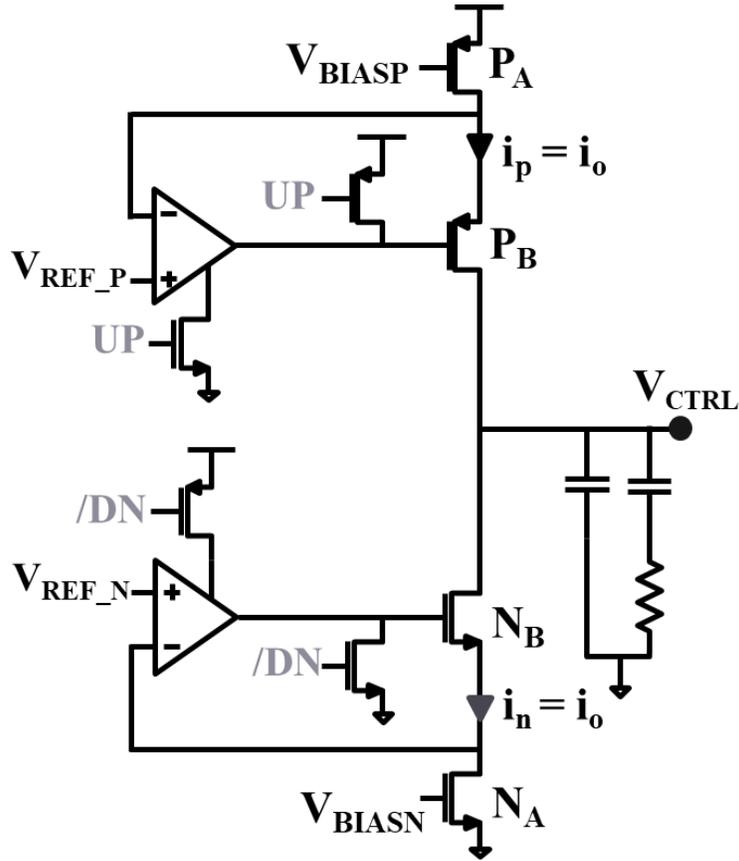


Figure 5.15: Proposed bootstrapped charge pump architecture.

The proposed CMOS bootstrapped charge pump is illustrated in Figure 5.15. The  $N_A$  and  $N_B$  NMOS transistors with the associated operational amplifier compose the NMOS bootstrapped current source. A similar structure is implemented on the PMOS side as depicted in Figure 5.15. The bootstrapped current source principle is based on a current control to compensate the variations of the output voltage  $V_{CTRL}$ .

For instance, the current  $i_N$  (respectively  $i_P$ ) is set by the transistor  $N_A$  (respectively  $P_A$ ). The voltage  $V_{DS}$  of the current source  $N_A$  (respectively  $P_A$ ) is compared with the reference voltage  $V_{REF-N}$  (respectively  $V_{REF-P}$ ). The OpAmp output voltage acts as a control loop of the  $N_B$  (respectively  $P_B$ ) transistor biasing. The  $N_B$  (respectively  $P_B$ ) transistor is then regulated to maintain the  $i_N$  (respectively  $i_P$ ) current against variations of the  $V_{CTRL}$  voltage. Thus, the proposed charge pump emulates the behavior of an ideal current source.

The minimum voltage for  $V_{CTRL}$  is then limited by the  $V_{REF-N}$  value and respectively the maximum  $V_{CTRL}$  voltage is limited by the  $V_{REF-P}$  value as:

$$V_{REF-N} < V_{CTRL} < V_{REF-P} \quad (5.18)$$

Due to the channel length modulation effect, the output resistance of the current source is finite and then creates a current shift depending on the  $V_{CTRL}$  voltage. Although, the proposed NMOS current source presents a high output resistance  $R_{OUT}$  expressed by:

$$R_{OUT} = g_{m_{NB}} \cdot r_{NB} \cdot r_{NA} \cdot (\text{Gain}_{OpAmp} + 1) + r_B + r_A \quad (5.19)$$

where  $\text{Gain}_{OpAmp}$  is the OpAmp gain,  $g_{m_{NB}}$  is the transconductance of the transistor  $N_B$ ,  $r_{NA}$  and  $r_{NB}$  are the output resistances of the transistors  $N_A$  and  $N_B$ . Thus, the regulation of the  $N_B$  transistor implies that the output resistance is also controlled to maintain a constant current in the charge pump output.

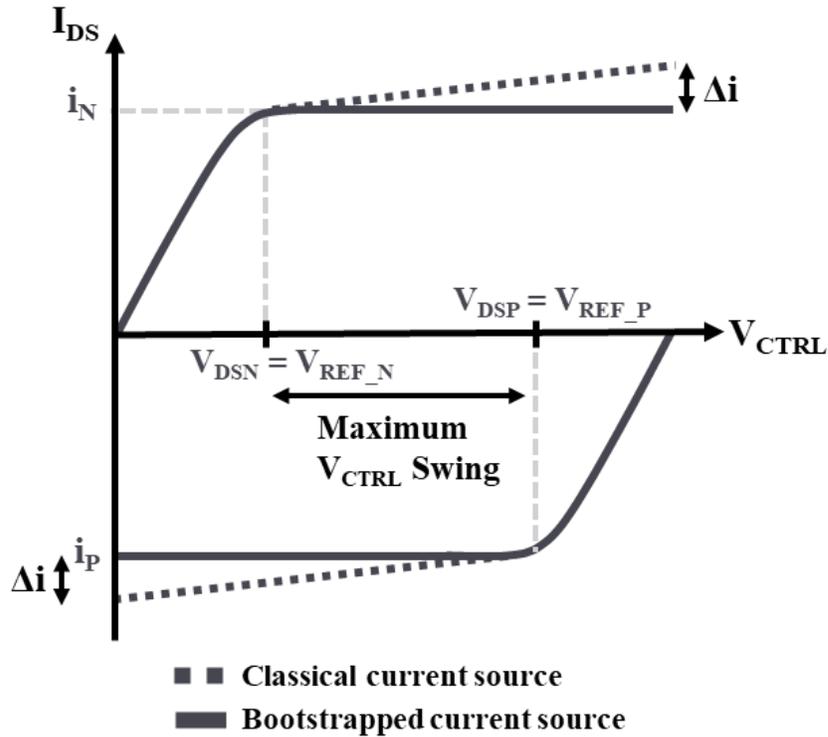


Figure 5.16: Comparison between classical current source and the proposed bootstrapped current source.

The  $V_{CTRL}$  amplitude is bounded by the two respective  $V_{DS}$  voltages of the  $N_A$  and  $P_A$  transistors. Thus, the  $N_A$  and  $P_A$  transistors are biased in linear mode to maximize the achievable amplitude swing for  $V_{CTRL}$ . It also permits to have a four-stacked transistors charge pump topology under a low supply voltage. Compared with a cascode current mirror, the proposed current source presents a higher output swing combined with a higher output resistance to reduce the channel length modulation.

Thus, the bootstrapped principle ensures a constant current independently of the  $V_{CTRL}$  voltage to reduce the channel length modulation phenomenon [RHE\_99] as illustrated in Figure 5.16. The proposed bootstrapped current source ensures a constant current throughout all the  $V_{CTRL}$  possible swings. Because the reference spur rejection capability is linked to the current difference  $|i_N - |i_P||$

[TI\_08], the bootstrapped principle maintains this difference constant over the  $V_{CTRL}$  variation to perform an expected constant reference spur performance along with the frequency tuning range.

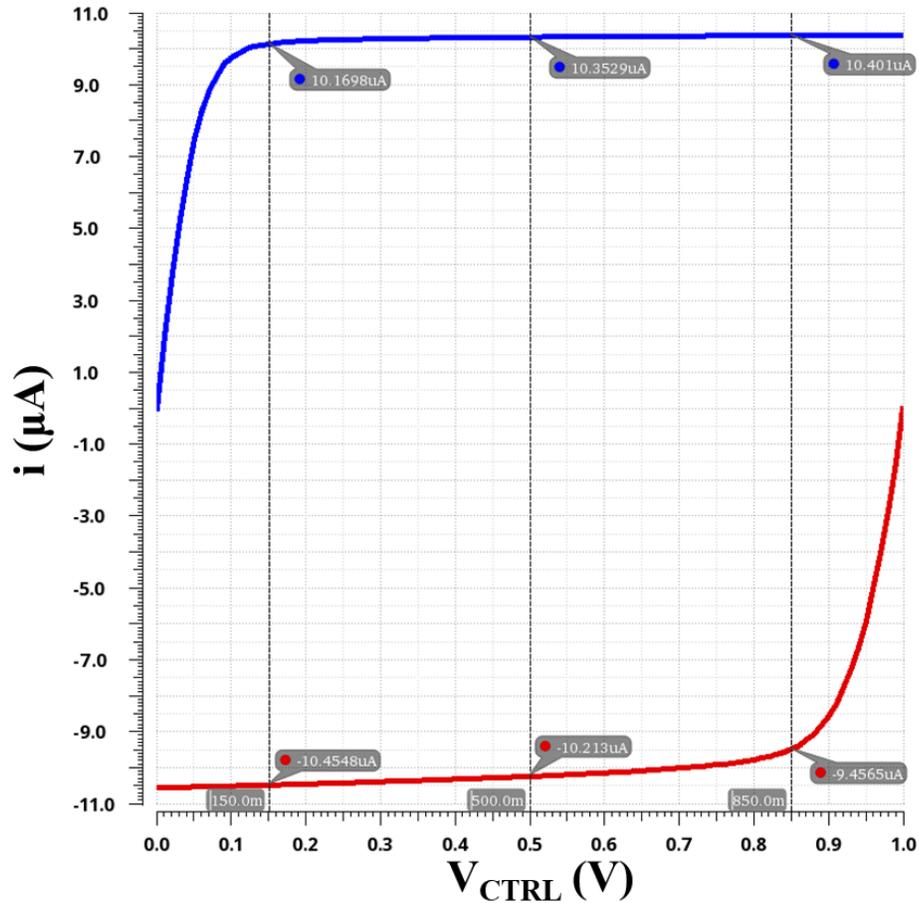


Figure 5.17: Simulated  $i_N$  and  $i_P$  current characteristics of the proposed charge pump.

The two current sources are designed to provide a  $10 \mu A$  output current as planned by the stability analysis. Figure 5.17 represents the simulated current characteristic of the proposed NMOS and PMOS bootstrapped current sources with  $V_{REFN} = 50 \text{ mV}$  and  $V_{REFP} = 950 \text{ mV}$ . The NMOS current source achieves a  $0.23 \mu A$  variation around its middle value of  $10.35 \mu A$  and the PMOS current source achieves a  $1 \mu A$  variation around its middle value of  $-10.21 \mu A$ . Based on the simulated results, the maximum expected swing achievable by the  $V_{CTRL}$  voltage is around  $900 \text{ mV}$ . The bootstrapped principle is verified by simulation and it ensures a constant current independently of the  $V_{CTRL}$  voltage variation.

### 5.4.3 Biasing circuit: $V_T$ dependent voltage reference

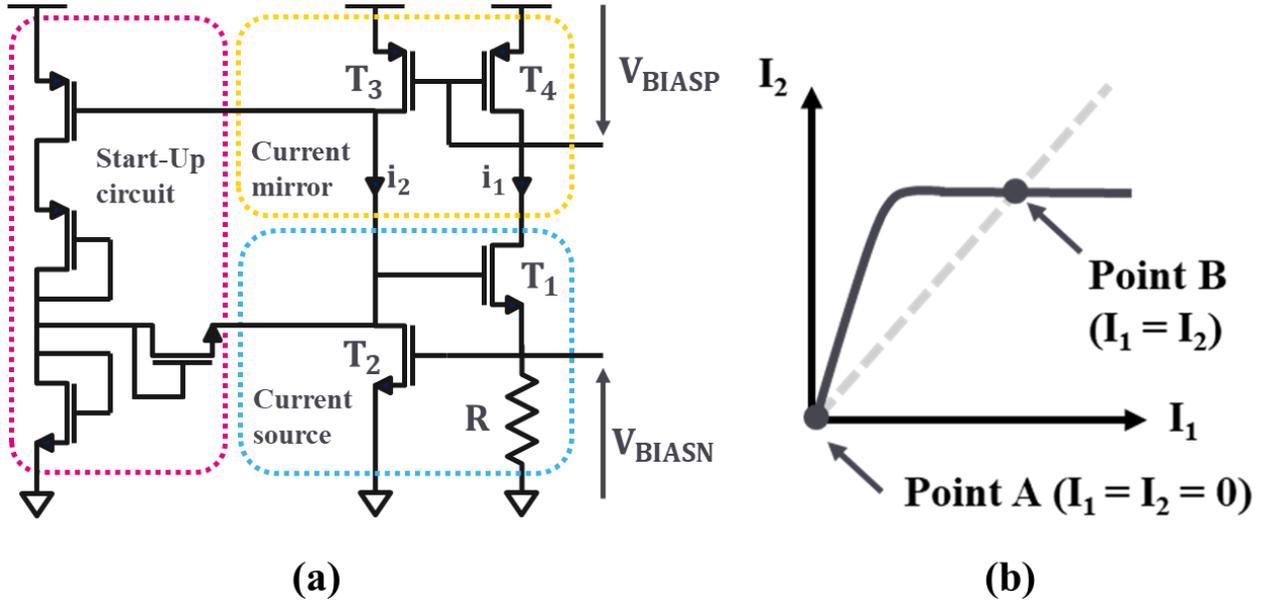


Figure 5.18:  $V_T$  dependent voltage reference architecture (a) and (b) Stable operating points of the voltage reference.

The main challenge is now to produce the bias voltages  $V_{BIASN}$  and  $V_{BIASP}$ . The two bias voltages are produced by the voltage reference circuit depicted in Figure 5.18. The  $V_T$ -dependent architecture is based on a combination of a current source (composed of  $T_1$  and  $T_2$  transistors and the  $R$  resistor) and a current mirror (composed of  $T_3$  and  $T_4$  transistors). The voltage reference is based on a positive feedback loop between the current source and the current mirror. The  $V_{GS}$  voltage of the  $T_1$  transistor is then expressed by:

$$V_{GS1} = V_{DS2} - V_{BIASN} \quad (5.20)$$

Thus, the  $i_1$  drain current is expressed by:

$$i_1 = \frac{1}{2} \cdot \mu_{N1} \cdot c_{ox1} \cdot \frac{W_1}{L_1} \cdot (V_{DS2} - V_{BIASN} - V_{T1})^2 \quad (5.21)$$

where  $\mu_{N1}$ ,  $c_{ox1}$ ,  $W_1$ , and  $L_1$  are the parameters of the  $T_1$  transistor,  $V_{DS2}$  is the  $V_{DS}$  voltage of the  $T_2$  transistor and  $V_{T1}$  is the threshold voltage of the  $T_1$  transistor. The  $V_{BIASN}$  voltage represents the  $V_{GS}$  voltage of the  $T_2$  transistor, the  $i_2$  drain current is then expressed by:

$$i_2 = \frac{1}{2} \cdot \mu_{N2} \cdot c_{ox2} \cdot \frac{W_2}{L_2} \cdot (V_{BIASN} - V_{T2})^2 \quad (5.22)$$

where  $\mu_{N2}$ ,  $c_{ox2}$ ,  $W_2$ , and  $L_2$  are the parameters of the  $T_2$  transistor and  $V_{T2}$  is the threshold voltage of the  $T_2$  transistor.

Considering (5.19) with a given  $V_{DS2}$  and  $V_{T1}$ , a decrease of the  $i_1$  current involves that the  $V_{BIASN}$  voltage increases. But if the  $V_{BIASN}$  voltage increases, it means by (5.20) that the  $i_2$  current

increases. The current equality from the matched current mirror imposes then an increase of the  $i_1$  current. Thus, any change on the  $i_1$  current creates an inverse change in the direction of the initial  $i_1$  current.

However, the positive feedback presents a major drawback represented in Figure 5.18(b). Because the two currents  $i_1$  and  $i_2$  are both defined by the current source and the current mirror, there are two achievable operating points corresponding to the current equality  $i_1 = i_2$ . The point B is the one expected at  $i_1 = i_2$  and the point A corresponds to  $i_1 = i_2 = 0$ . To avoid such a steady-state, a start-up circuit is added to the voltage reference represented in Figure 5.18(a). Composed of three diode-mounted transistors, the start-up circuit prevents the unwanted operating point A. If the circuit is on the Point A, it implies that  $V_{BIASN} = i_1 * R = 0$  and  $V_{DS2} = V_{GS1} = 0$ . The diodes force a current into  $T_2$  to increase the  $V_{GS1}$  and  $V_{DS2}$  voltages and hence increasing the  $i_1$  current. Once the circuit has reached the operating point B, the diodes do not flow current anymore and they do not influence the behavior of the voltage reference.

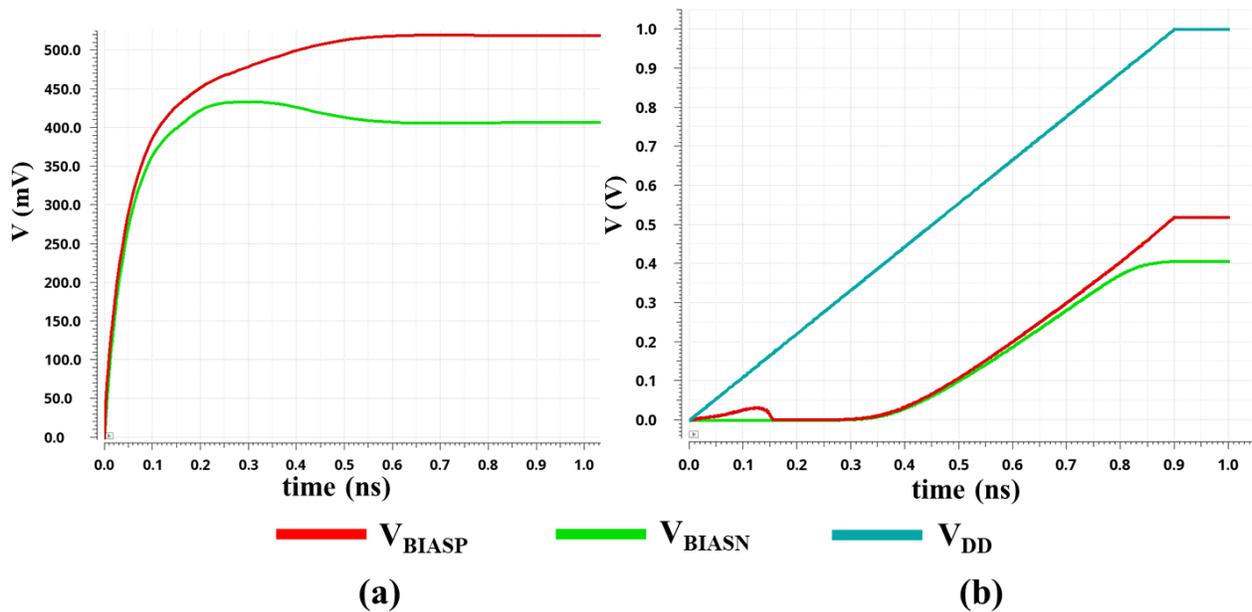


Figure 5.19: Simulated  $V_{BIASN}$  and  $V_{BIASP}$  voltages to verify the start-up circuit behaviour with the initial condition  $V_{BIASN} = V_{BIASP} = 0$  V and  $V_{DD} = 1$  V (a) and (b)  $V_{BIASN} = V_{BIASP} = V_{DD} = 0$  V.

The behavior of the  $V_T$ -dependent voltage reference with the start-up circuit is verified in simulation. Figure 5.19(a) represents the simulated transient curves of the two biasing voltages  $V_{BIASP}$  and  $V_{BIASN}$ . The initial values are forced to  $V_{BIASN} = V_{BIASP} = 0$  V to correspond on the initial operating point A. The start-up circuit recovers the biasing voltages as expected. Illustrated in Figure 5.19(b), another simulation consists to slowly raise the supply voltage  $V_{DD}$  with a ramp of 0.9 ms. This simulation allows to verify that the current created by the start-up circuit is enough to move the circuit to the operating point B. Indeed, the start-up circuit can go down when the circuit is not enough moved away from point A. In that case, the biasing voltages decrease until that the start-up circuit turns on again creating an unwanted oscillation. The behavior of the start-up circuit is then verified by simulation.

### 5.4.4 Charge pump simulation and conclusion

A particular attention was given to the study of the bootstrapped current sources and the voltage reference circuit. The latest part of this section is dedicated to the charge pump simulation of the two bootstrapped current sources. The main purpose is to keep a maximum swing for the  $V_{CTRL}$  voltage by avoiding other serial transistor addition. Thus, the four stacked transistors ( $P_A$ ,  $P_B$ ,  $N_A$ , and  $N_B$ ) enable to use a nominal 1V supply voltage.

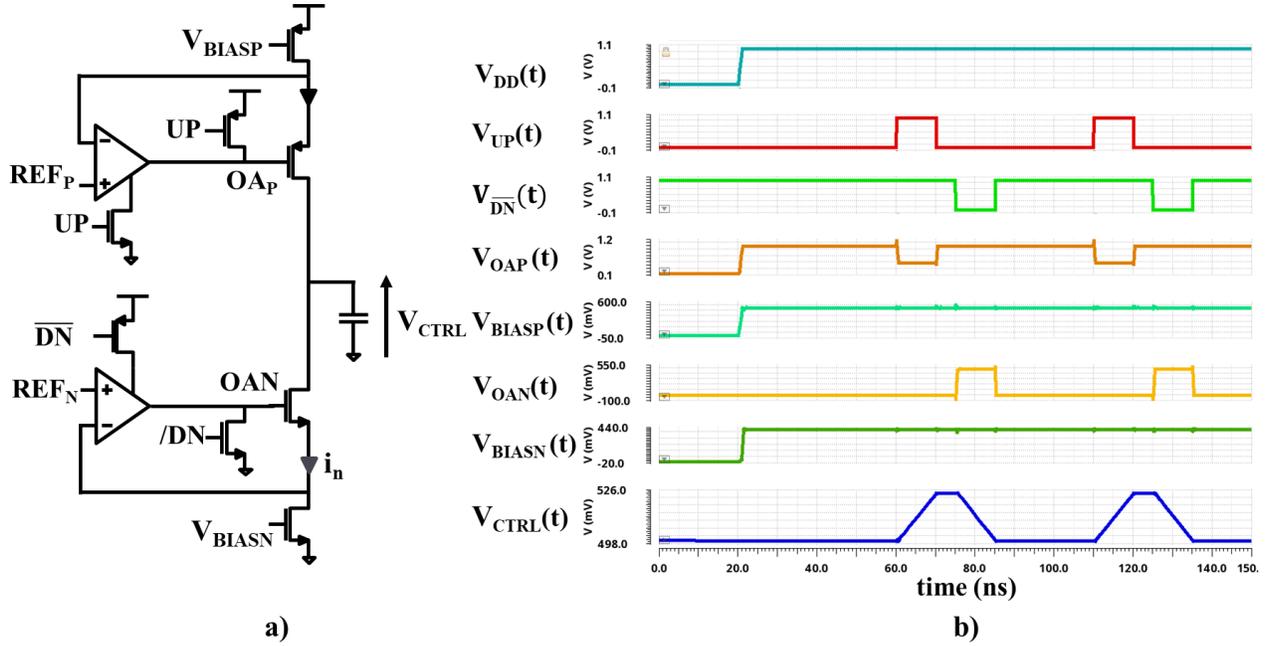


Figure 5.20: Bootstrapped charge pump schematic with all internal signals (a) and (b) the transient simulation of the implemented charge pump.

Figure 5.20(a) represents the implemented bootstrapped charge pump with its internal signals. The two  $V_{BIASN}$  and  $V_{BIASP}$  signals are generated from the  $V_T$ -dependent circuit. Emulating the phase-frequency detector output signals, the  $UP$  and  $/DN$  signals control the switches which are added into the feedback loop of the bootstrapped current sources as represented in Figure 5.20(a). The switches monitor the  $N_B$  transistor (respectively the  $P_B$  transistor) to inject current into the loop filter which is mimicked by a 4 pF capacitor.

The transient results of the parasitic-extracted simulation are represented in Figure 5.20(b). The 1V supply voltage is turned on after 10 ns to verify the start-up circuit, no input signals are generated until 60 ns to verify the biasing values of the internal signals. Finally,  $UP$  and  $/DN$  signals are generated to test the transient functioning of the charge pump. The parasitic-extracted simulation attests the functionality of the implemented charge pump architecture.

Thus, the proposed bootstrapped charge pump achieves a robust charge pump for low supply voltage operation with a constant output current flow throughout a maximized output voltage swing  $V_{CTRL}$ .

## 5.5 Others Caliper PLL building blocks

### 5.5.1 Phase Frequency Detector (PFD)

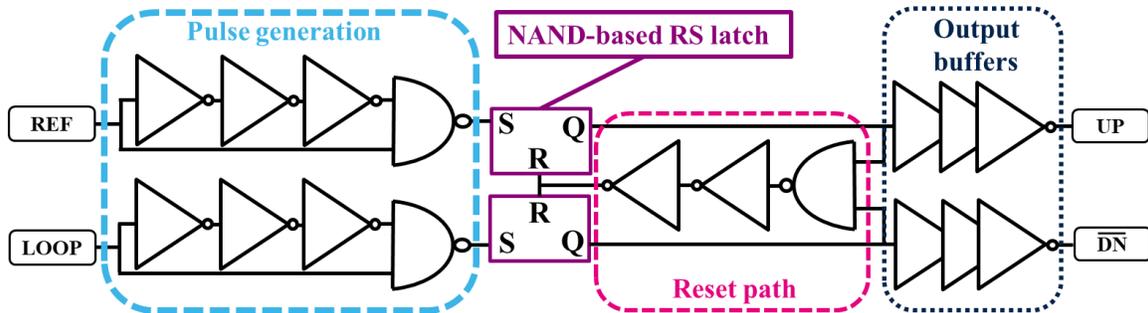


Figure 5.21: Schematic diagram of the positive-edge triggered tri-states comparator phase-frequency detector.

Illustrated in Figure 5.21, the same phase-frequency detector (PFD) architecture is implemented in both the primary and the secondary loop. The phase-frequency detector is a positive-edge triggered tri-states comparator. The rising edges of the input signals ( $V_{REF}(t)$  and  $V_{LOOP}(t)$ ) into short pulses ( $V_{REF\_pulse}(t)$  and  $V_{LOOP\_pulse}(t)$ ). These pulses trigger the RS latches and then set the output buffered signals ( $V_{UP}(t)$  and  $V_{DN}(t)$ ). The two RS latches are immediately reset after the vanishing of the last of the two pulses avoiding meta-stability issues during the reset. The time delay generated due to the time propagation of all the blocks creates a blind zone called dead zone where the PFD is not able to detect input time variation.

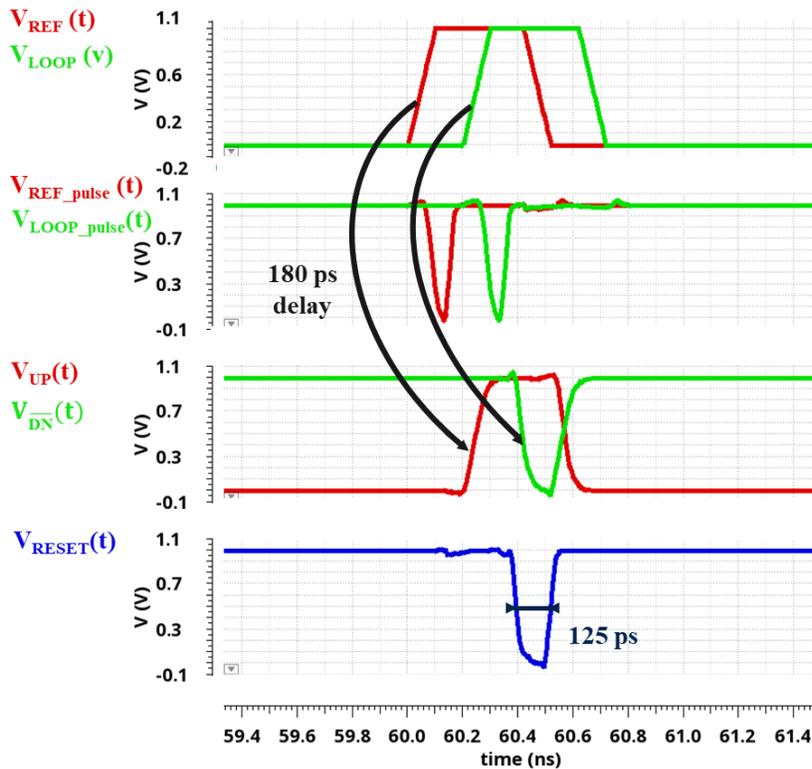


Figure 5.22: Schematic diagram of the phase-frequency detector.

The parasitic-extracted PFD is charged by the charge pump, the simulated transient diagram is represented in Figure 5.22 with the typical time delays between the internal signals for a given 1 V supply voltage and a 22 MHz reference frequency. A pure delay of 180 ps achieved between the input and output signals while the reset path is 125 ps. The functionality of the common positive-edge triggered tri-states PFD is then verified.

### 5.5.2 PFD and Charge Pump Association

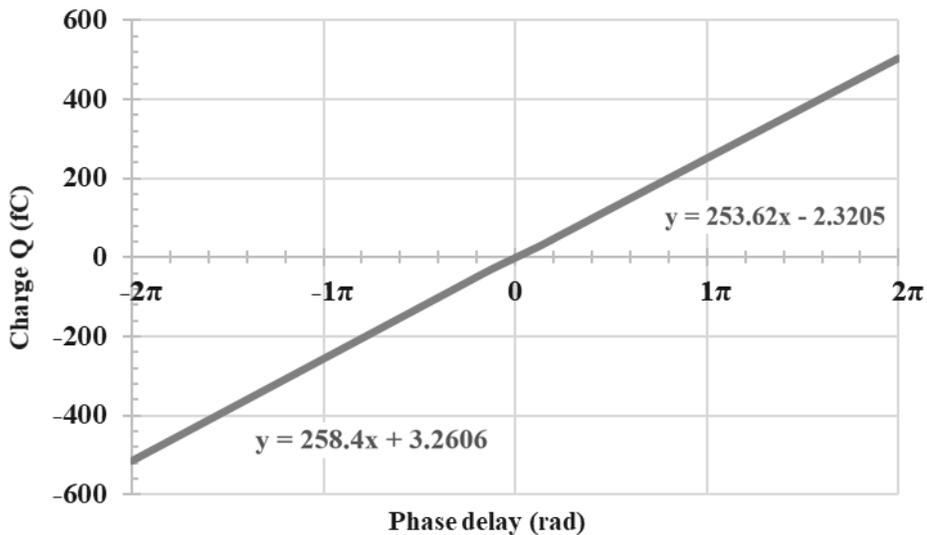


Figure 5.23: Simulated PFD/CP characteristic.

The PFD/CP characteristic is represented in Figure 5.23 by varying the delay between the two 20 MHz input signals REF and LOOP. The capacitor charge  $Q$ , corresponding to the capacitance value multiplied by the voltage drop of the capacitor ( $Q = C \cdot \Delta V$ ), is then computed. The characteristic enables to compute the value of the dead zone. The two equations of the linear trendline enable to compute the dead zone value around 170 ps which corroborates the value of the reset path and the pure delay of the PFD. The average current consumption is 17.5  $\mu\text{A}$  for the PFD/CP association. This parasitic-extracted simulation attests the functionality of the two PFD and CP blocks.

### 5.5.3 Digital frequency divider

The main concerns about the frequency dividers are how they affect the oscillator. Indeed, the input capacitance has to be considered in the oscillator drive capability which results in an oscillator output swing reduction. As the ring-oscillators are digital with rail-to-rail output, the frequency divider capacitance affects only the oscillation frequency. The Caliper PLL contains the same frequency divider architecture for the two feedback frequency dividers ( $N_1$  and  $N_2$ ) and the two input frequency dividers ( $R$  and  $R+X$ ). As explained during the study of the digital mixer, the chosen strategy is to use a digital edge-counter frequency divider. The digital approach also takes benefit from the FDSOI technology to propose a compact divider with a low power consumption for the two feedback frequency dividers and two input frequency dividers.

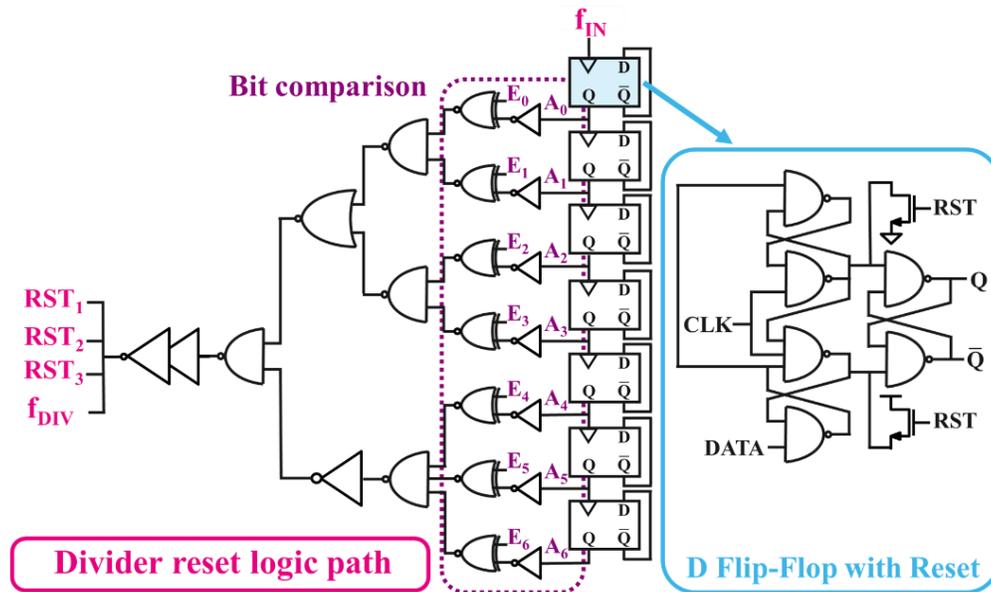


Figure 5.24: Schematic diagram of the binary edge-counter frequency divider.

Illustrated in Figure 5.24, the integer-N digital frequency divider architecture is based on a 7-bit counter represented by a series of D-flip-flop circuits. The D-flip-flop circuits divide the input frequency by two to count the number of rising edges. They generate a binary word  $A_i$  representing the current number of rising edges of the input signal  $f_{IN}$ . The  $A_i$  word is then compared to the programmable word  $E_i$  by the bit selector circuit. Once the programmed value of edges is reached, a logic path resets the counter and outputs a pulse to the phase-frequency detector (PFD). Buffered by a logic tree, the reset signal is separated into four reset pulses. Each of the three pulses resets two flip-flops when the fourth pulse both resets one flip-flop and is propagated to the PFD.

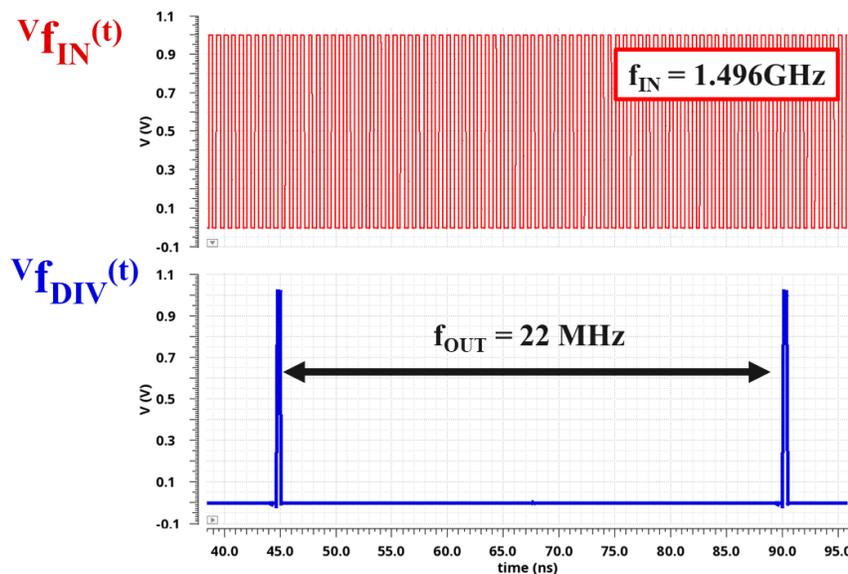


Figure 5.25: Transient simulation of the frequency divider for an input frequency of  $f_{IN} = 1.496$  GHz, a divider ratio of 68 given an output frequency of  $f_{DIV} = 22$  MHz.

Represented in Figure 5.25, the frequency divider is simulated as the primary loop feedback divider with a division value of  $N_1 = 68 = 0b1000100$ . The frequency divider receives an input frequency of  $f_{IN} = 1.496$  GHz which emulates the difference frequency  $f_{MIX}$  from the two loop frequencies  $f_1 = 2.416$  GHz and  $f_2 = 920$  MHz. The period of the output pulses is  $T = 45.4545$  ns corresponding to the expected frequency of 22 MHz. The average current consumption is around  $80 \mu\text{A}$ .

#### 5.5.4 Transimpedance low-pass filter

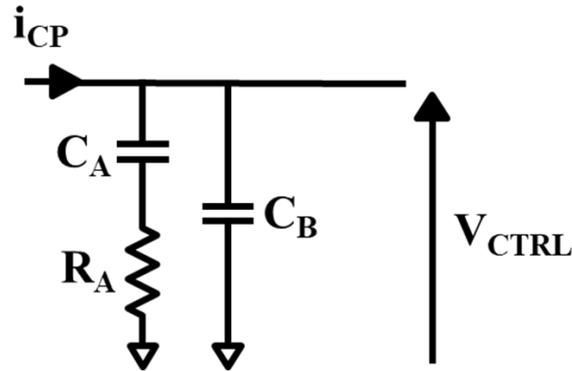


Figure 5.26: Transimpedance low-pass filter topology.

The same filter topology is implemented in both the primary and secondary loops. Represented in Figure 5.26, the transimpedance filter topology is a second-order low pass filter composed of a resistor  $R_A$  in series with a capacitor  $C_A$ . A capacitor  $C_B$  is added in parallel with the  $R_A$  and  $C_A$  network.

	$R_A$	$C_A$	$C_B$
Primary loop filter	114 k $\Omega$	4.02 pF	317 fF
Secondary loop filter	165 k $\Omega$	4.02 pF	317 fF

Table 5B: Component values of the primary loop filter and the secondary loop filter.

Given in Table 5B, the component values of the two loop filters are derived from the stability analysis. Through small enough component values, the two loop filters can be implemented which makes the Caliper PLL a fully integrated frequency synthesizer.

## 5.6 Physical PLL implementation and design for test

### 5.6.1 Top-level strategy

This section details the implementation of the Caliper PLL. It begins with the Top-level strategy representing by the floorplan of the proposed PLL. Then, layout representations of each Caliper PLL building block are discussed. Finally, the implementation and the simulation of the entire Caliper PLL are presented.

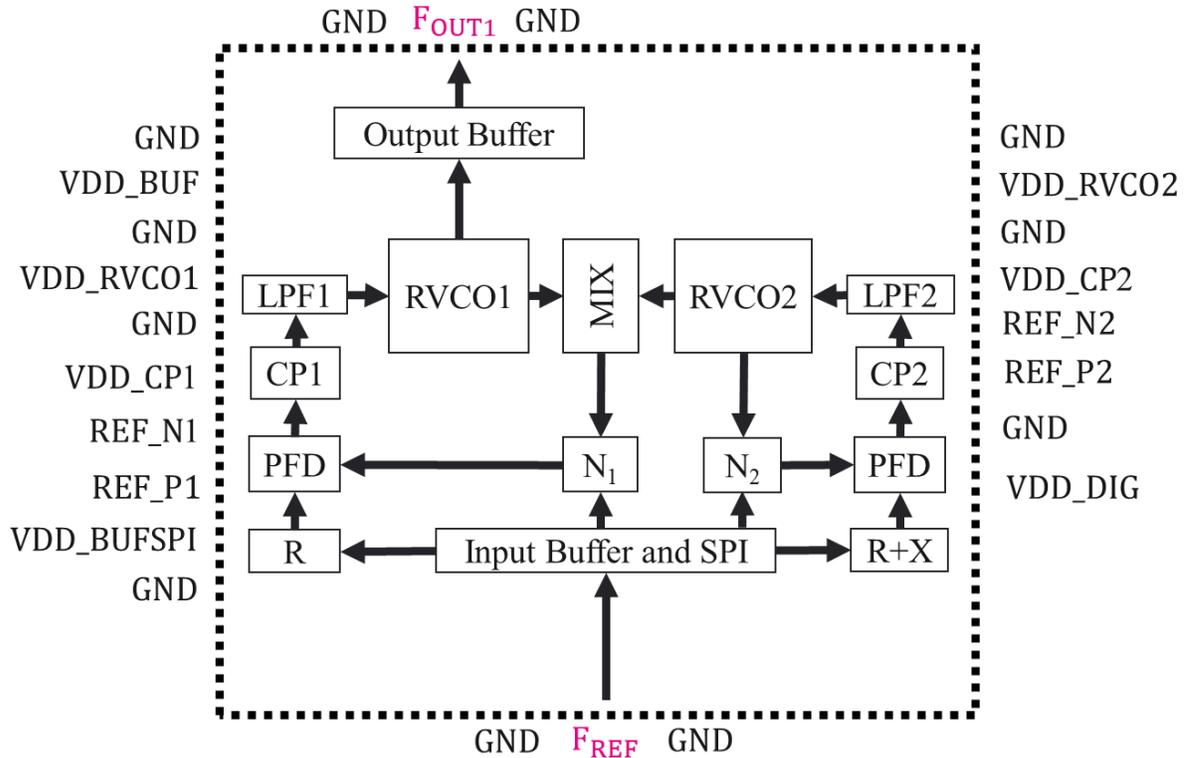


Figure 5.27: Floorplan of the Caliper PLL detailing the location of each building block, the I/O pins, and the internal signals of the proposed PLL.

Represented in Figure 5.27, the floorplan shows an overview of the PLL before laying out each building block. It identifies the number of Input/Output (I/O) pins needed for the package which marks out the area of the chip. For measurement purposes, each supply voltage is chosen to be an external output. As a protection of a sensitive signal, each supply I/O is separated between two ground pads. The strategy of a unique ground plane is chosen to minimize the presence of stray currents between two different supply areas. The stray current refers to the electricity flowing between cells and ground due to the flaws of the interconnexions. Thus, a unique ground is chosen as a voltage reference. Finally, ESD protections are provided in the guard ring to protect the chip.

The RF signals ( $f_{OUT}$  and  $f_{REF}$ ) determines the core PLL placement. The floorplan of the core anticipates the interconnexions between the internal cells. It avoids the common mistake of drawing independently the layout of each cell and making their interconnection problematic. Represented in Figure 5.27, the placement of each PLL block is anticipated with its internal interconnections. The top-level strategy is very interesting to predict the layout of each PLL building block. It also permits to consider the physical implementation of the Caliper PLL as a global system. Thus, each PLL building block layout is well thought out.

### 5.6.2 Ring oscillators

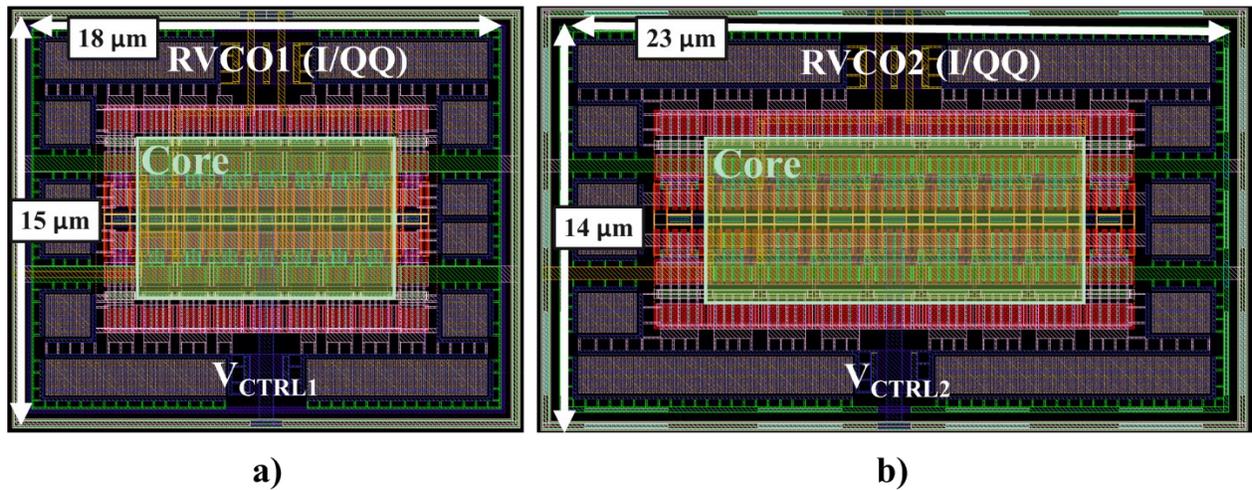


Figure 5.28: Layout representation of the primary loop RVCO<sub>1</sub> (a) and (b) secondary loop RVCO<sub>2</sub>.

The primary loop RVCO<sub>1</sub> and secondary loop RVCO<sub>2</sub> are represented in Figure 5.28(a) and Figure 5.28(b) respectively. Composed of  $N = 13$  delay stages, all the transistors were designed with a length of  $L = 85$  nm, widths of  $W = 1.2$  μm for the NMOS transistors and widths of  $W = 2.4$  μm for the PMOS transistors. Represented in Figure 5.28(b), the secondary loop oscillator RVCO<sub>2</sub> is also composed of  $N = 13$  delay stages. All the transistors were designed with a length of  $L = 180$  nm, a width of  $W = 1.0$  μm for the NMOS transistors and a width of  $W = 2.0$  μm for the PMOS transistors to target an oscillation frequency around 900 MHz. Each RVCO produces two output signals (named I and QQ) with a time delay of  $3T_{Osc}/13$  representing the quasi-quadrature inputs of the digital down-conversion frequency mixer. Because the two RVCOs share common layout considerations with the digital mixer, they are discussed in the following section.

### 5.6.3 Digital mixer

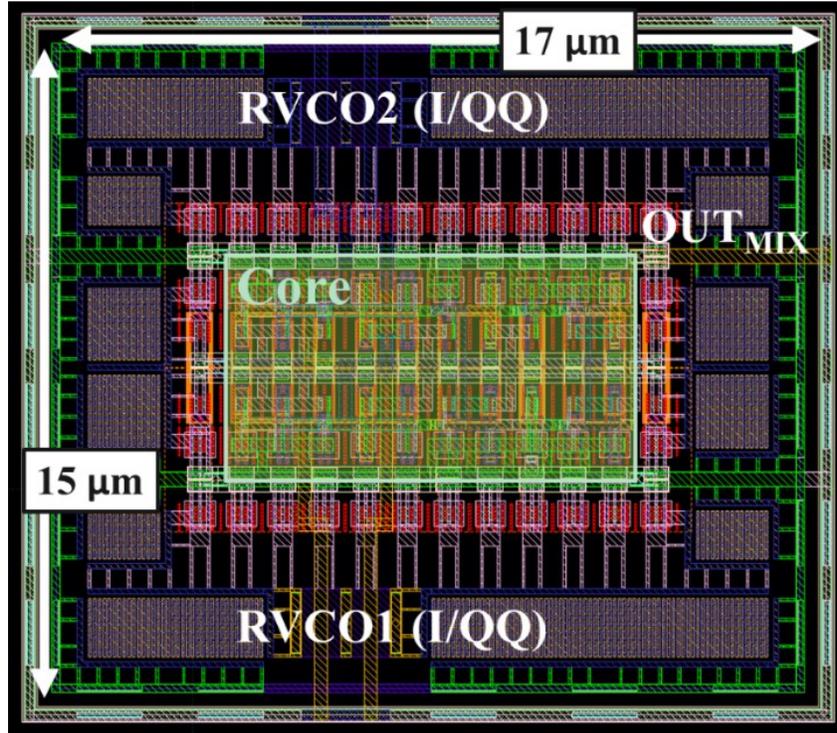


Figure 5.29: Layout representation of the digital mixer.

The layout representation of the implemented DFM is represented in Figure 5.29. All the transistors were designed with a length of  $L = 50$  nm, a width of  $W = 300$  nm for the NMOS transistors and a width of  $W = 600$  nm for the PMOS transistors to ensure a good compromise between the power consumption and the matching between all the transistors.

The two ring-oscillators and the mixer are the most sensitive parts of the PLL architecture. Two aspects are here considered. To get started, the ring oscillators are very sensitive to the voltage supply variation. Local decoupling capacitors are placed around the oscillator core to provide a stable value of the supply voltage. Secondly, the two ring oscillators and the mixer are fully digital, they spread leakage current through the substrate corresponding to the switching behavior of the logic gates. Considering two oscillators running at different frequencies, an unwanted pulling phenomenon occurs if the oscillators are physically close together. The two oscillators are then coupled, and their respective oscillation frequencies are locked to an intermediate value. Drawn across each circuit, a guard ring is routed to the ground to protect the circuit. The increased doping  $p^+$  decreases the bulk resistance of the guard ring to collect most of the carrier flowing in the silicon. Thus, the circuit is protected from external disturbance and the guard ring also avoids the internal disturbance to be spread to other circuits.

### 5.6.4 Charge Pump

The charge pump is the only analog building block of the proposed PLL architecture. The accuracy of the charge pump performance must be robust to the process variations during the manufacturing fabrication. Thus, the matching between components of the charge pump (i.e. the current mirrors or differential pairs) represents the major concern in analog design.

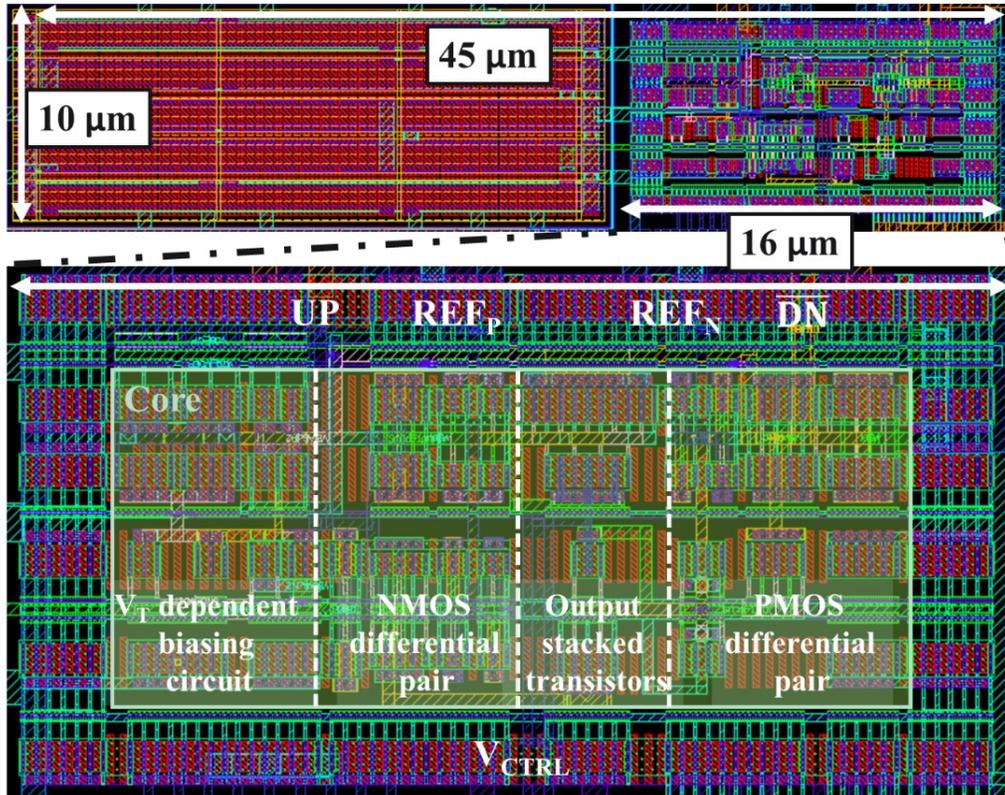


Figure 5.30: Layout representation of the bootstrapped charge pump.

The implementation of the charge pump circuit leads to the introduction of common layout techniques. The implemented charge pump architecture is represented in Figure 5.30, the bootstrapped charge pump including the NMOS and PMOS differential pairs as well as the  $V_T$  dependent circuit is depicted. All the transistors of the charge pump are designed with a gate length of  $L = 110$  nm. Dummy transistors are added to generate a regular matrix of aligned transistor gates to minimize the impact of the process variations. Thus, the layout techniques enable to implement a robust and compact design with a total area of  $450 \mu\text{m}^2$ .

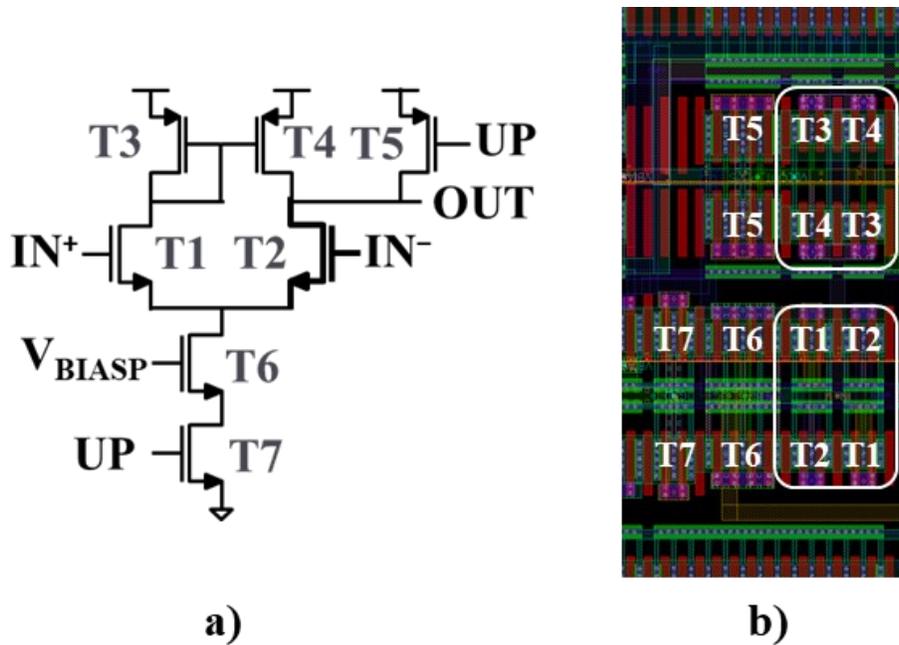


Figure 5.31: Transistor-level representation of the NMOS differential pair with active load (a) and (b) its layout representation.

The transistor-level representation and the detailed layout of the NMOS differential pair with active load are represented in Figure 5.31. The four transistors T1, T2, T3, and T4 are decomposed into basic elements of two-finger transistors. It minimizes the gate resistance and improves the device matching for the layout of the NMOS differential pair (transistors T1 and T2) and the current mirror (transistors T3 and T4). The elements are disposed as a common centroid array to make them immune from cross-chip gradients. The point of symmetry between the transistors represents the best matching performance possible.

The resistor is also a critical component because it fixes both the current inside the  $V_T$ -dependent biasing circuit and the  $V_{BIASN}$  biasing voltage. The  $V_{BIASN}$  voltage is designed around 500 mV for a current inside the  $V_T$ -dependent circuit around 10  $\mu$ A. Thus, an approximated resistance value of 50 k $\Omega$  is targeted.

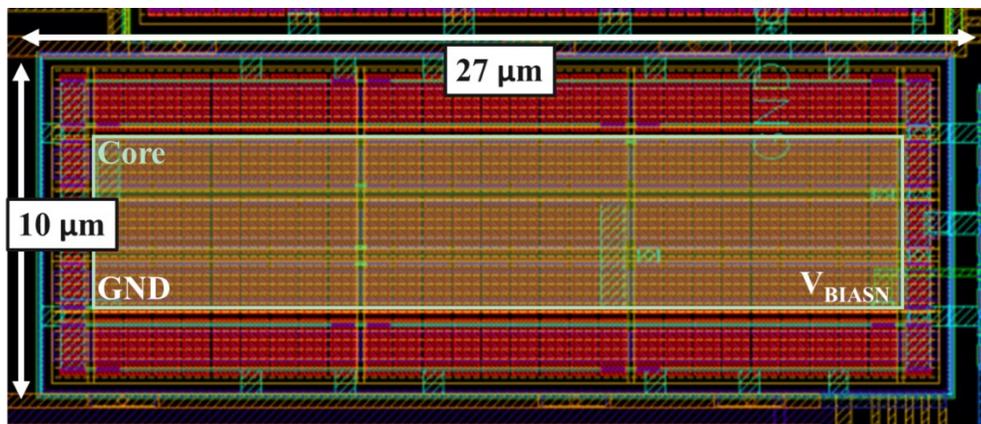


Figure 5.32: Layout representation of the resistor inside the  $V_T$ -dependent circuit.

A poly high-precision non-silicided resistor is chosen to reach a trade-off between good linearity, a high sheet resistance value, and a small process variation. The 50 k $\Omega$  resistor is sliced into nine resistances of 5.55 k $\Omega$  as represented in Figure 5.32. Each 5.55 k $\Omega$  is composed of nine series stripes. To improve the matching and then reduce the resistance variation due to the process, dummy resistors are added to ensure that each unit resistor has the same environment. All the dummy resistors are tied to the ground by the guard-ring.

### 5.6.5 Phase Frequency Detector

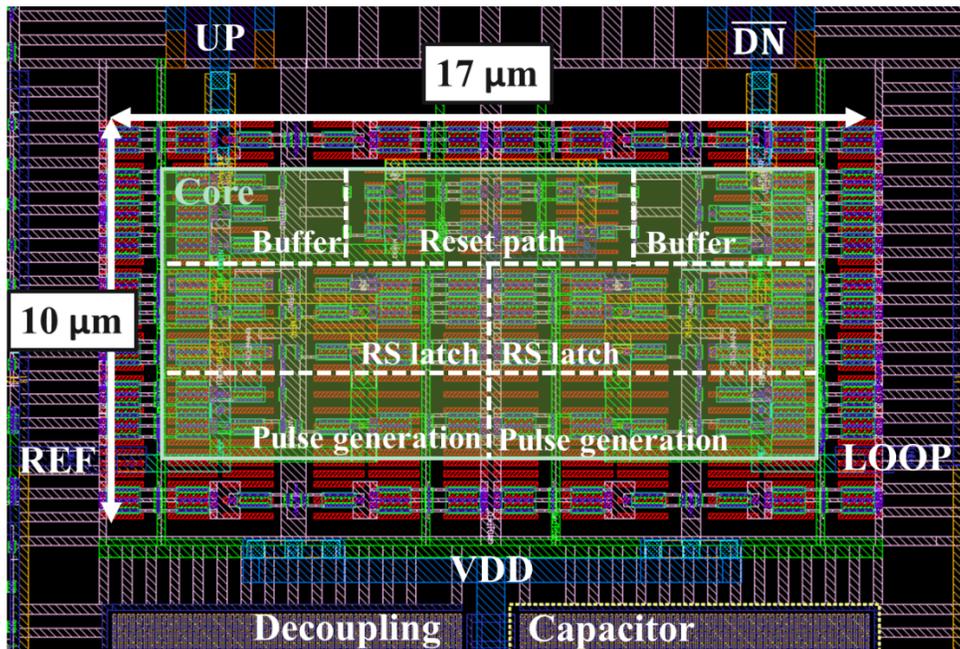


Figure 5.33: Layout representation of the phase-frequency detector.

The layout representation of the implemented PFD is represented in Figure 5.33, The pulse generation and the output buffers are designed with a transistor length of  $L = 110$  nm. The RS latches are designed with a length of  $L = 80$  nm to maximize matching and to reduce the propagation times. The reset path is also designed with a transistor length of  $L = 50$  nm to reduce the total dead zone. To generate the UP and  $\overline{DN}$  signals compatible with the proposed bootstrapped charge pump, the output buffer is composed of three inverters for the UP path and on two inverters with a pass-gate stage for the  $\overline{DN}$  path to equalize the propagation delays between the two output signals.

### 5.6.6 Digital frequency divider

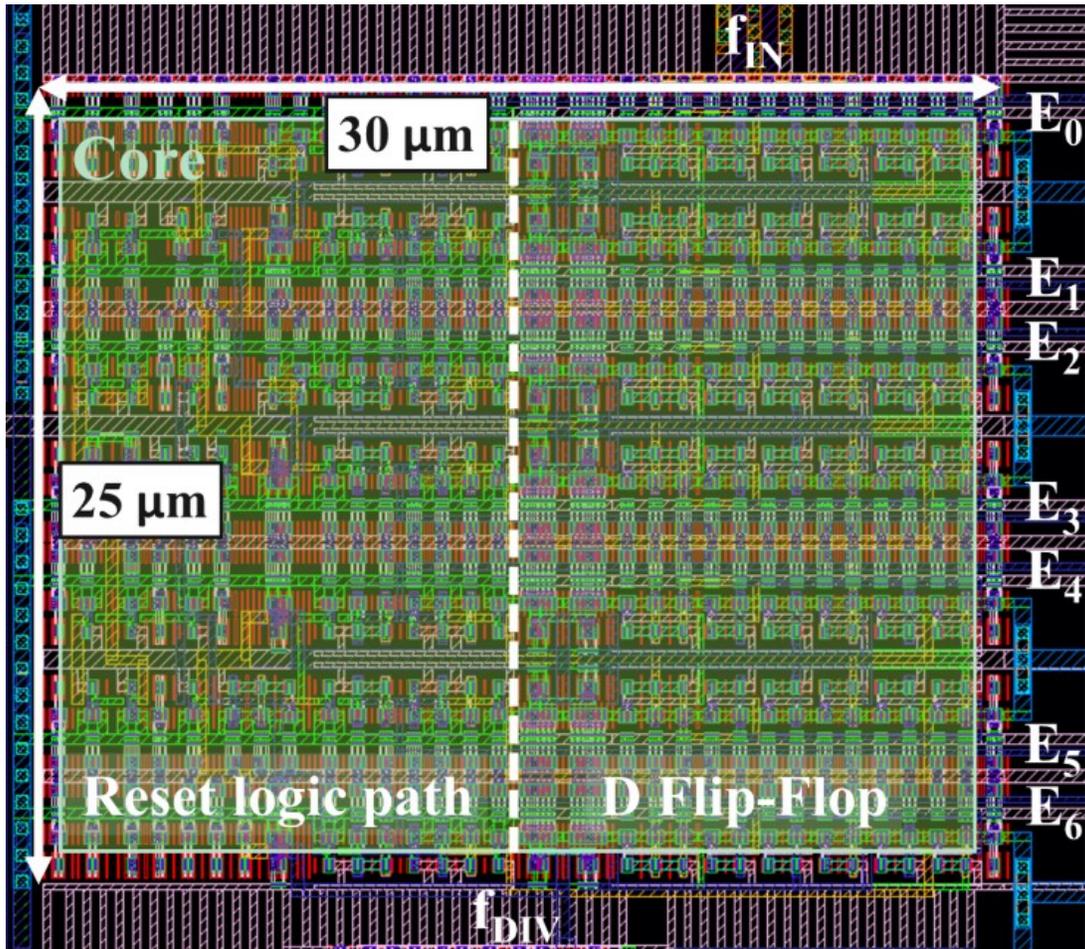


Figure 5.34: Layout representation of the digital frequency divider.

The layout representation of the frequency divider is illustrated in Figure 5.34. Due to that the first stage of D-Flip-Flop has to operate as fast as the oscillator frequency, a common transistor length of  $L = 50\text{nm}$  is chosen for every transistor of the entire divider. The compact layout reaches a compromise between power consumption and the operating frequency.

### 5.6.7 Transimpedance low-pass filter

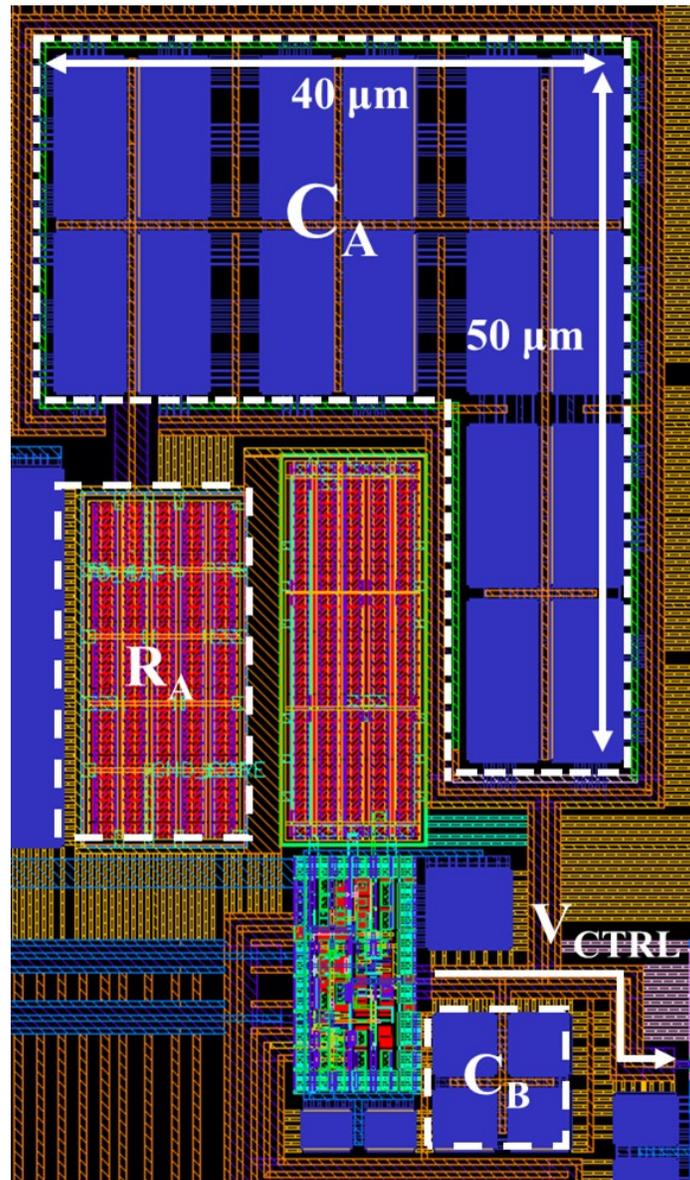


Figure 5.35: Layout representation of the primary loop filter.

The layout representation of the primary loop filter is represented in Figure 5.35. The main strategy of the filter layout is to reduce the  $V_{CTRL}$  path to minimize the access resistance. Indeed, the oscillator control voltage is a sensitive signal, any noise is directly transformed into output noise by the oscillator.

<b>Variations (%   %   %)</b>	<b>C<sub>A</sub> (pF)</b>	<b>R<sub>A</sub> (kΩ)</b>	<b>C<sub>B</sub> (fF)</b>	<b>φ<sub>m</sub></b>	<b>ξ</b>
-20   -20   -20	3.21	92	253	58.6°	0.49
0   -20   -20	4.02	92	253	61.8°	0.55
+20   -20   -20	4.82	92	253	64.1°	0.60
-20   0   0	3.21	114	317	55.1°	0.61
0   0   0	4.02	114	317	58.6°	0.69
+20   0   0	4.82	114	317	61.2°	0.75
-20   +20   +20	3.21	138	380	52.0°	0.74
0   +20   +20	4.02	138	380	55.8°	0.83
+20   +20   +20	4.82	138	380	58.6°	0.90

Table 5C: Variation of the primary loop filter components values.

Table 5C represents a variation of +/- 20 % of each component value from the primary loop filter. Only nine over twenty-seven possibilities are represented, it is enough to highlight how the filter component variations impact the behavior of the loop. As calculated during the stability analysis, the open-loop phase margin is slightly changed by the capacitance variation. However, the damping factor is directly impacted by the resistance variation. The same resistor type as the  $V_T$  dependent circuit, a poly high-precision non-silicided resistor, is chosen. Considering the trade-off between saving area and ensuring the PLL stability, only the resistance has dummy elements around its core to reduce the process variations. Capacitors are still sliced into multiple parts to be disposed in a local common centroid layout as represented in Figure 5.35. As expected, the passive elements of the filter occupy a significant part of the total PLL area. The strategy to implement the filter as the last PLL element permits to shape the filter around the existing PLL core to produce the most compact design possible.

## 5.7 Global PLL simulation

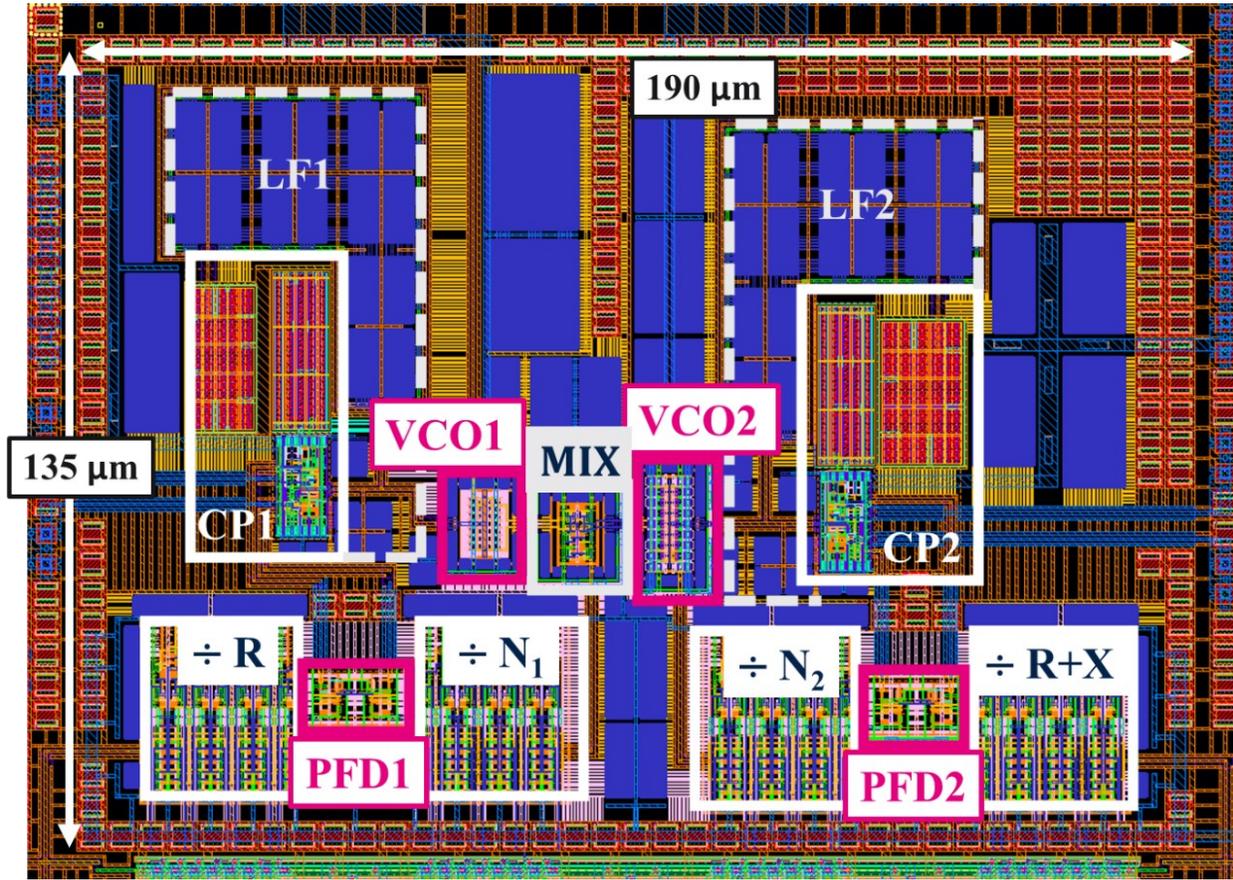


Figure 5.36: Layout representation of the Caliper PLL.

Represented in Figure 5.36, the layout representation of the complete Caliper PLL shows a core area of  $0.0256 \text{ mm}^2$  including the local decoupling capacitors. Each PLL building block is identified, one can observe that the two passive loop filters only use 17% of the total active area. Concerning the internal signals paths, each local supply voltage has extra decoupling capacitors along the path between the PLL core and the chip pads. The PLL core is centered to properly distribute both the input and output RF paths. Considering the effect of the wire bonding between the chip and the package, both the oscillator output signal path and the input signal from the reference frequency are internally buffered to manage the  $50 \Omega$  charge outside the chip.

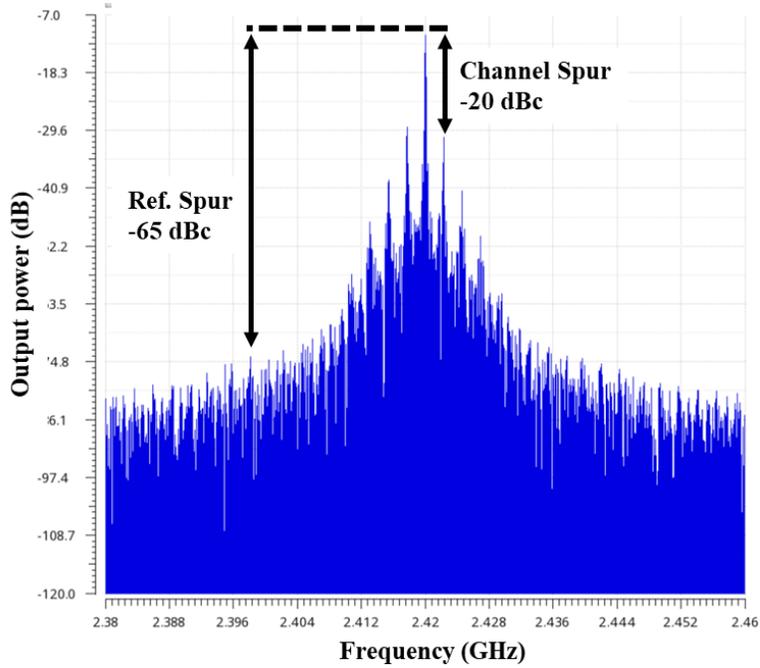


Figure 5.37: Simulated output spectrum for a 2.420 GHz output frequency.

As represented in Figure 5.37, the output spectrum shows that the Caliper PLL locks on the 2.420 GHz frequency. The spectrum is calculated using the Hamming window function from the simulated transient waveform. Concerning the sampling of the simulated signal, the number of signal periods is chosen to be a power of two to minimize the aliasing effect during the spectrum calculation. The channel spurs at 2 MHz offset frequency from the carrier are visible in the spectrum. These spurs are generated from the Offset-PLL topology of the Caliper PLL [LEE\_05]. One can notice that the spurs at 22 MHz and 20 MHz from the carrier are close to the noise floor, it is due to the ideal reference source used for the simulation.

Expressed in Chapter 3, the reference spur performance of the primary loop can be evaluated by:

$$\frac{P_{\text{ref spur}}}{P_{\text{carrier}}} = 20 \log \left( \frac{K_{\text{VCO1}} I_{\text{Leak}}}{2\pi C_B f_{\text{IN1}}^2} \right) \quad (5.23)$$

where  $P_{\text{ref spur}}$  is the power of the reference spurs,  $P_{\text{carrier}}$  is the power of the carrier,  $K_{\text{VCO1}}$  is the oscillator gain,  $C_B$  is the capacitor value of filter,  $I_{\text{Leak}}$  is the current leakage of the charge pump and  $f_{\text{IN1}}$  is the internal frequency of the primary loop.

The  $I_{\text{Leak}}$  leakage current is calculated as:

$$I_{\text{Leak}} = \frac{t_{\text{pulse}}}{T_{\text{IN1}}} \cdot |i_{\text{N}} - |i_{\text{P}}|| \quad (5.24)$$

where  $t_{\text{pulse}}$  is the pulse duration of the two signals UP and /DN from the phase-frequency detector when the PLL is locked,  $T_{\text{IN1}}$  is the period of the internal frequency of the primary loop,

$i_N$  is the current value of the NMOS current source and  $i_P$  is the current value of the PMOS current source.

Symbol	Name	Values	Units
$f_{REF}$	Common reference frequency	440	MHz
$f_{IN1}$	Primary loop internal frequency	22	MHz
$f_{IN2}$	Secondary loop internal frequency	20	MHz
R	Primary loop input frequency divider	20	-
R+X	Secondary loop input frequency divider	22	-
$N_1$	Primary loop feedback frequency divider	70	-
$N_2$	Secondary loop feedback frequency divider	44	-
$f_1$	Primary loop oscillator nominal frequency	2.285	GHz
$f_2$	Secondary loop oscillator nominal frequency	850.9	MHz
$K_{VCO1}$	Primary loop oscillator gain	250	MHz/V
$I_{Leak}$	Charge pump leakage current	38	nA
$C_B$	Primary loop filter capacitor value	317	fF
$f_{IN1}$	Primary loop internal frequency	22	MHz
$i_N$	Charge pump current of the NMOS current source	10.35	$\mu$ A
$ i_P $	Charge pump current of the PMOS current source	10.21	$\mu$ A

Table 5D: Caliper PLL parameters for the transistor-level simulation.

From the parameters of the Table 5D and (5.22), the leakage current is  $I_{Leak} = 38$  nA. Thus, the simulated reference spur is  $-41.24$  dBc at 22 MHz offset frequency from the carrier.

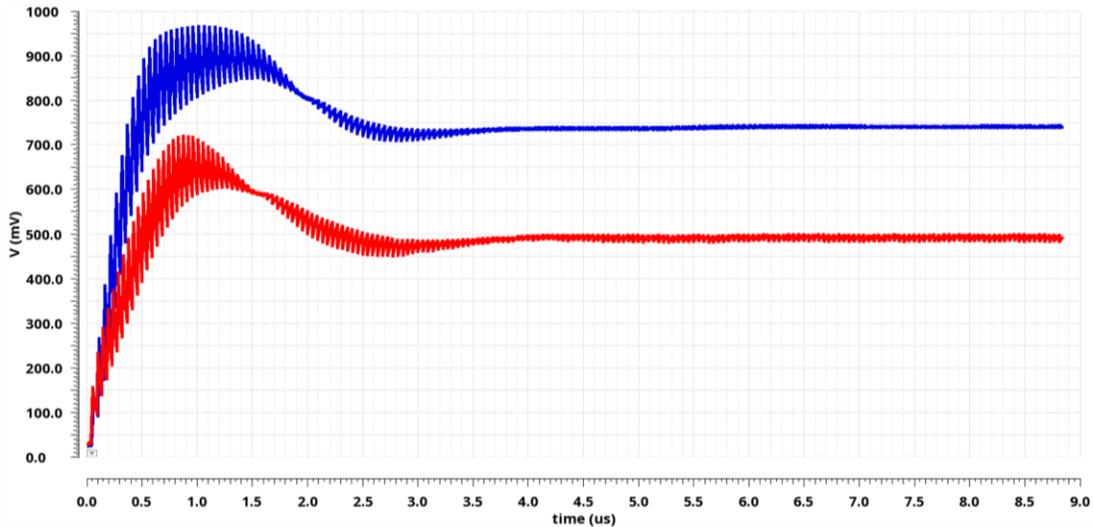


Figure 5.38: Simulated oscillator control voltages  $V_{CTRL1}$  and  $V_{CTRL2}$ .

From the values of Table 5D, the parasitic-extracted Caliper PLL is simulated to establish a transistor-level proof of concept. The Caliper PLL reaches a locked state with a locking time of  $4.0 \mu$ s. Illustrated in Figure 5.37 and Figure 5.38, the Caliper PLL locks on the 2.420 GHz output frequency which verifies the relation of:

$$f_{out} = N_1 \cdot f_{IN1} + N_2 \cdot f_{IN2} \quad (5.25)$$

Then, the stability of the Caliper PLL is verified. The Caliper PLL is simulated with different ( $N_1; N_2$ ) frequency divider values to verify the output frequency resolution of  $\Delta f_{OUT} = 2$  MHz. The proof of concept of the Caliper PLL is then verified at a transistor-level simulation.

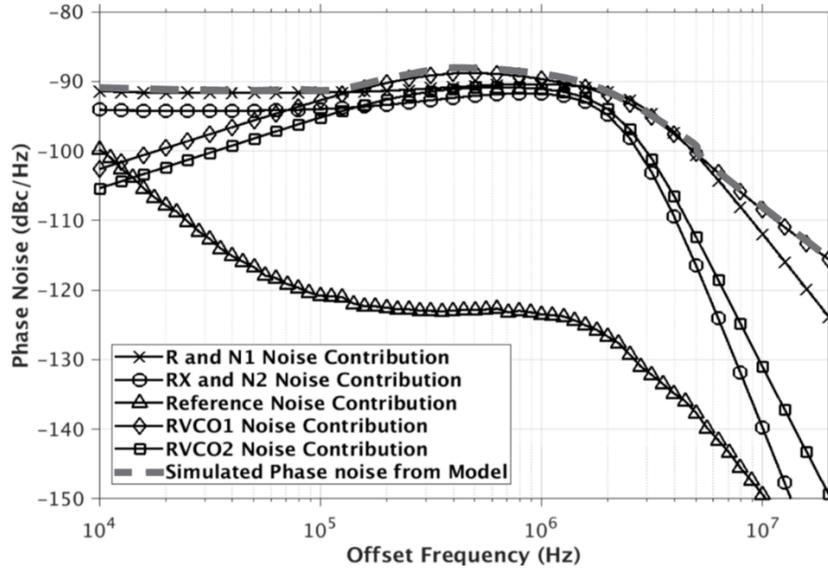


Figure 5.39: Simulated Caliper PLL phase noise performance.

Represented in Figure 5.39, the phase noise performance of the Caliper is determined from the Phase noise model established during the noise analysis of Chapter 3. Each phase contribution is calculated from the simulated phase noise of each building block. The Caliper PLL achieves a simulated PLL bandwidth of around 2 MHz. As expected, the wideband PLL bandwidth improves the RVCO phase noise close to the carrier. The in-band phase noise is dominated by the frequency divider noise contribution.

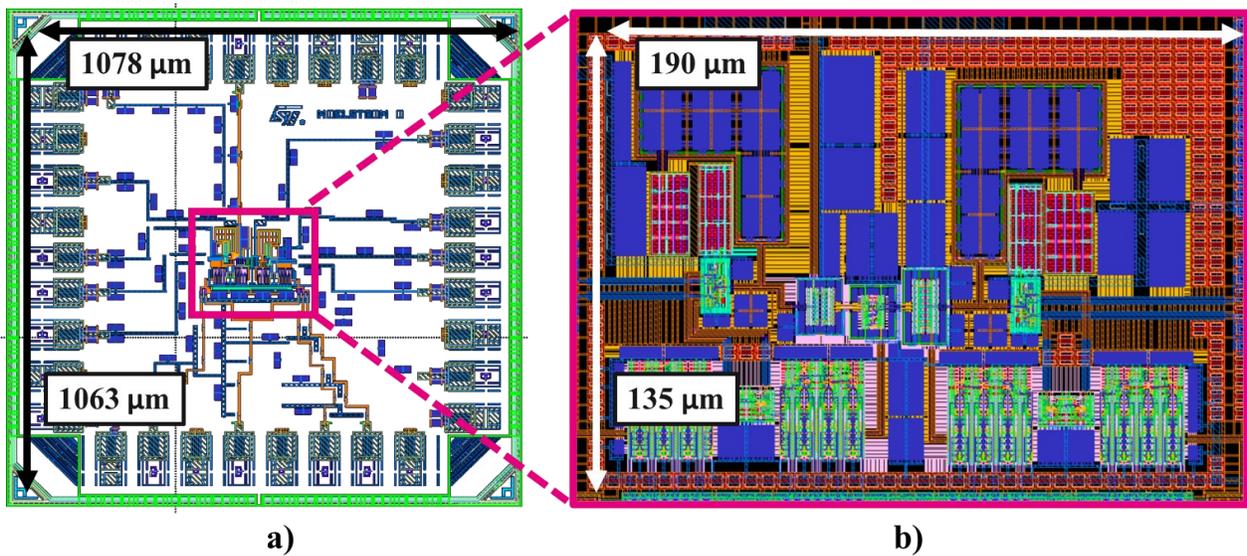


Figure 5.40: Layout representation of the Caliper PLL chip (a) and (b) an insert on the Caliper PLL active area.

Figure 5.40(a) represents the layout representation of the entire chip of the Caliper PLL architecture with an insert on the active area of the Caliper PLL in Figure 5.40(b). Additional decoupling capacitors are added between the chip pads and the core area. Moreover, input and output buffers are added to manage the  $50\ \Omega$  load of the measurement devices. The core area occupies  $0.0256\ \text{mm}^2$  for a total chip area of  $1.1459\ \text{mm}^2$ .

## 5.8 Conclusion

This chapter presents the design specifications and the chip implementation of the proposed Caliper PLL. The first part is focused on the design specification of each Caliper PLL building block. In particular, three original designs are presented in this section.

Based on the conclusion of the RVCO study in Chapter 4, a single-ended inverter-based ring oscillator topology is presented. This RVCO topology achieves good phase noise performance for minimal power consumption. The RVCO frequency tuning is enabled by the unique feature of the FD-SOI technology, the RVCO frequency is controlled by body-biasing the transistors' back gate. Furthermore, the frequency tuning control is applied on only the NMOS LVT transistors. As confirmed by the global simulations, the frequency tuning range is large enough to cover the BLE bands from 2.4 GHz to 2.48 GHz. Using only the NMOS LVT body-biasing enables to directly use the filter voltage output as RVCO control voltage without extra biasing circuit to achieve minimal power consumption. Thus, the body biasing feature, unique to FD-SOI technology, enables this new frequency tuning knob over this very simple, compact, power-efficient, and robust RO topology.

A fully digital down-conversion frequency mixer is proposed. The mixer has the particularity to generate only the difference frequency  $f_{\text{MIX}} = f_1 - f_2$  without the use of an extra filter. The study of the proposed mixer enables the use of the quasi-quadrature inputs (I and QQ) from the single-ended RVCOs. Thus, the flexibility of the mixer is a real advantage to use ultra-low power and compact RVCO topologies. A prototype is realized to verify these assumptions and the feasibility of the mixer architecture is validated by measurement. It enables the use of the proposed digital mixer inside the Caliper PLL. Furthermore, the chosen strategy is to use the combination of the frequency divider with the loop filter to act as another selective bandpass filter to extract the wanted  $f_1 - f_2$  difference frequency. The proposed digital down-conversion mixer is an original contribution that is compliant with IoT challenges in terms of ultra-low power and compact design.

Concerning the charge pump architecture, a particular attention is given to the only analog building block of the Caliper PLL. The proposed bootstrapped charge pump ensures a constant

output current throughout all the possible swings of the output voltage. The current sources are regulated by a control loop to compensate the output voltage variations. Thus, the channel length modulation phenomenon is reduced which enables the bootstrapped charge pump to provide a constant output current. A  $v_T$ -dependent voltage reference with a start-up circuit is presented to ensure a stable biasing of the current sources. Furthermore, the current sources are biased in their linear mode to maximize the achievable output swing. Thus, the proposed bootstrapped charge pump achieves a robust charge pump for low supply voltage operation with a constant output current flow throughout a maximized output voltage swing. The proposed charge pump architecture targets constant performance once implemented inside the Caliper PLL.

The others Caliper PLL building blocks are presented. Each of them shows interesting features. Concerning the digital blocks which achieve low power and compact designs, the phase-frequency detector avoids meta-stability issues during its reset and the binary edge-counter frequency divider is specified to be compliant with the digital mixer. Concerning the two loop filters, the passive elements are designed to be fully integrated inside the Caliper PLL architecture.

The second part of this chapter is dedicated to the physical implementation of the Caliper PLL architecture. The top-level strategy of a system such as a PLL architecture is very educative. Indeed, the top-level strategy identifies the position of each PLL building block and it enables to predict the interconnections with the others blocks. Thereby, the top-level layout organization determines the layout of each PLL building block in order to produce a compact PLL circuit. The physical implementation of each PLL building block is presented and the layout techniques are discussed. All the layout techniques used during the physical implementation of the Caliper PLL have one purpose: produce a robust and compact design targeting the IoT challenges of Chapter 2 while ensuring the Caliper PLL specifications detailed in Chapter 3.

Finally, Caliper PLL specifications are verified in simulation. In particular, transient simulation verifies the PLL close loop stability. Furthermore, the 2 MHz frequency resolution is confirmed. The phase noise model proposed in Chapter 3 has been successfully demonstrated here in order to determine the wideband PLL bandwidth and the main noise contributors. Finally, the transistor-level implementation of the proposed Caliper PLL architecture has been fully demonstrated.

# 6 Measurement Results of Caliper PLL Architecture

## 6.1 Introduction

This chapter is dedicated to the measurement results of this thesis work. The presented measurement set-up can perform statistical measurements to determine the circuit robustness to process variations.

Measurement performances of the Caliper PLL are discussed. Implemented in 28nm FD-SOI technology, the proposed PLL reaches a sub-mW compact solution. Caliper PLL specifications in terms of PLL stability and PLL frequency resolution are verified in measurement. Measured reference spurs performance highlights the industrial robustness of the proposed Caliper PLL architecture. In line with simulation results, measured output phase noise confirms the wideband PLL bandwidth of the Caliper PLL architecture.

Compared with the IoT fractional-N PLL architectures, the proposed frequency synthesis achieves a state-of-the-art solution in FD-SOI technology. Along these lines, the proposed PLL architecture reaches an interesting overall compromise between the RF performances, the power consumption, and the core area.

## 6.2 Measurements set-up

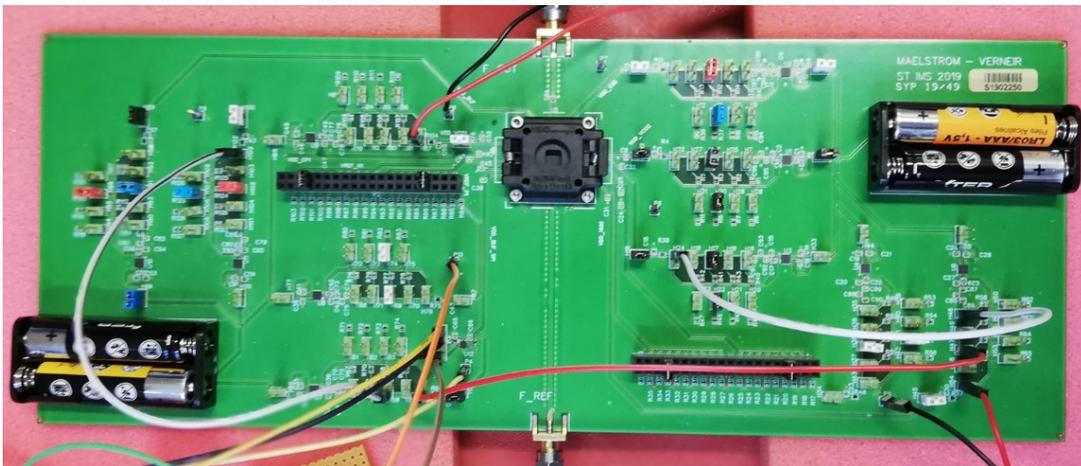


Figure 6.1: Print circuit board of the Caliper PLL prototype.

The following sections are focused on the on-chip measurements of the Caliper PLL. The prototype is implemented in 28nm FD-SOI CMOS technology from STMicroelectronics. Illustrated in Figure 6.1, a printed circuit board (PCB) is realized. The implemented chip is reported on the PCB through an integrated circuit support called “socket”. The socket is useful to test

different dies without soldering them on the circuit board. Statistical measurements are then possible to evaluate the variability of the prototype performance. The supply voltages are controlled through low-noise low drop-out regulators (LDO) powered on by external batteries. If needed, the test board also offers the possibility to use external supply voltages.

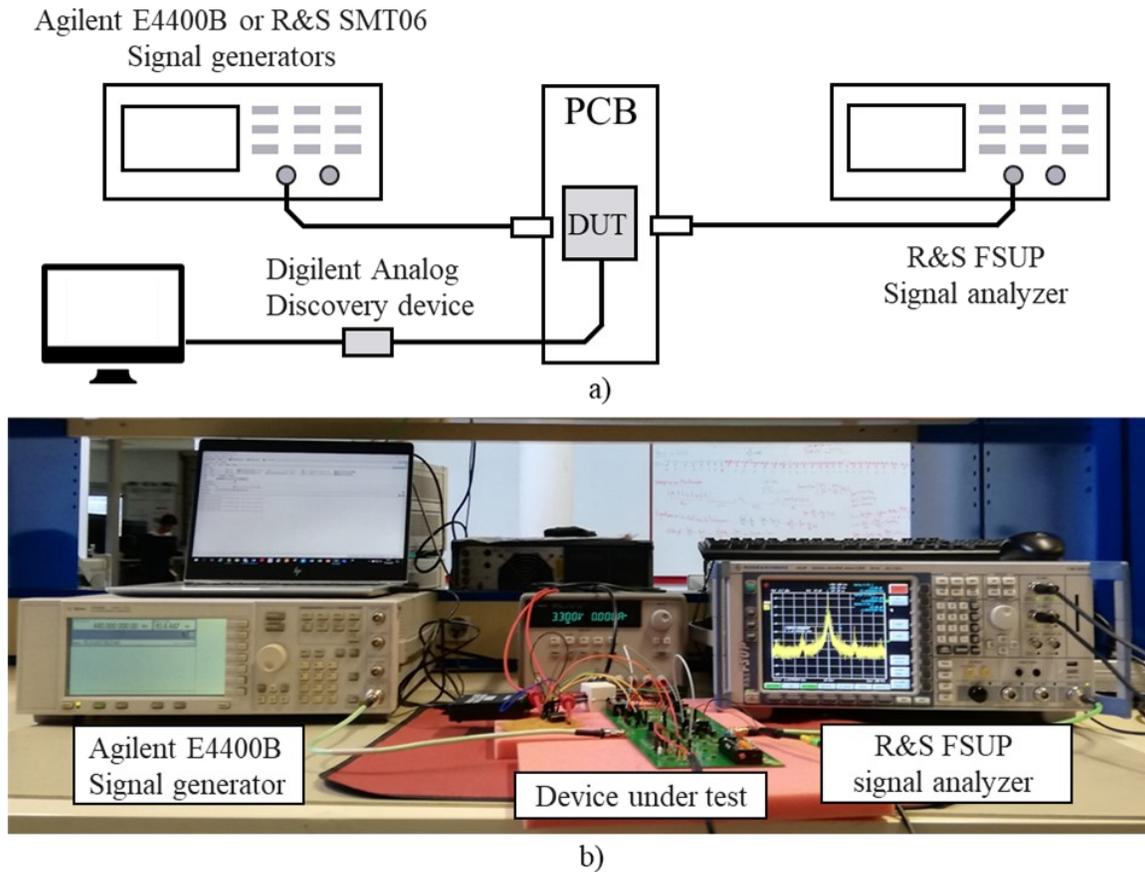


Figure 6.2: Measurement set-up schematic (a) and (b) measurement set-up in the IMS Laboratory.

The measurement set-up is illustrated in Figure 6.2(a). The external signal generator produces the 440 MHz reference signal. The reference signal is propagated to the PLL prototype located in the print circuit board. The output signal generated by the Caliper PLL is propagated to the external Rohde & Schwarz FSUP signal source analyzer. The Analog Discovery device from Digilent is used as a link between the laptop and the printed circuit board. It permits to manage the frequency dividers values and then to control the output frequency of the Caliper PLL. The PLL prototype is measured during two measurement sessions. The first session occurs at the IMS Laboratory at the University of Bordeaux. The second session takes place in STMicroelectronics, in a special room called Faraday cage. This room is used to protect the PLL prototype from external radio frequency interferences during the measurement. Only the measurement set-up of the IMS Laboratory is illustrated in Figure 6.2(b).

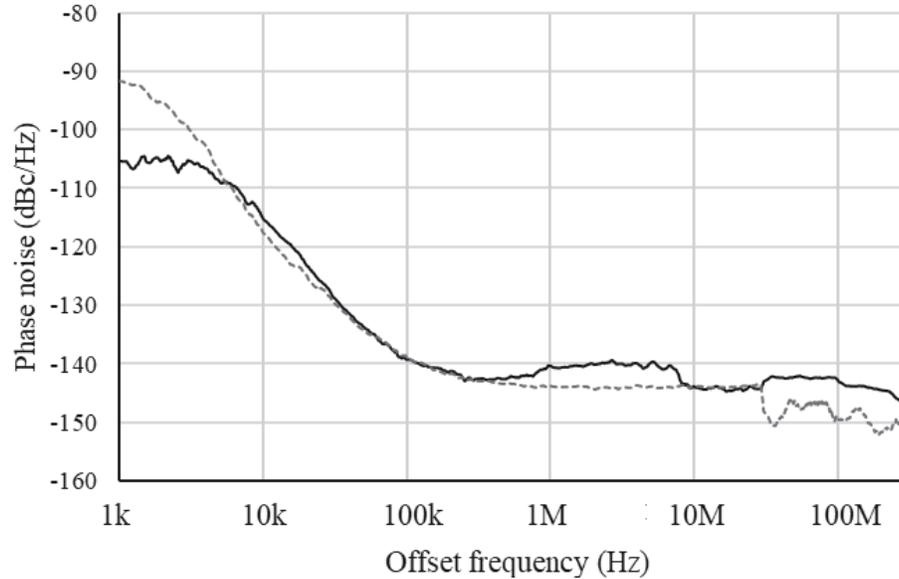


Figure 6.3: Phase noise comparison for a 440 MHz frequency between the Agilent E4400B signal generator (in black solid line) and the R&S SMT06 signal generator (in grey dot line).

The common 440 MHz reference frequency is provided by an Agilent E4400B external signal generator for the IMS laboratory set-up. Concerning the Faraday cage set-up, the reference frequency is generated by a Rohde & Schwarz SMT06 signal generator. Figure 6.3 represents the phase noise performances of the two signal generators for the same 440 MHz frequency. One can notice that the two phase noise performance is equivalent from a 10 kHz offset frequency. Thus, the phase noise contribution of the reference frequency in the output phase noise performance is considered equal in the two measurements sessions.

### 6.3 Measurement results of the Caliper PLL architecture

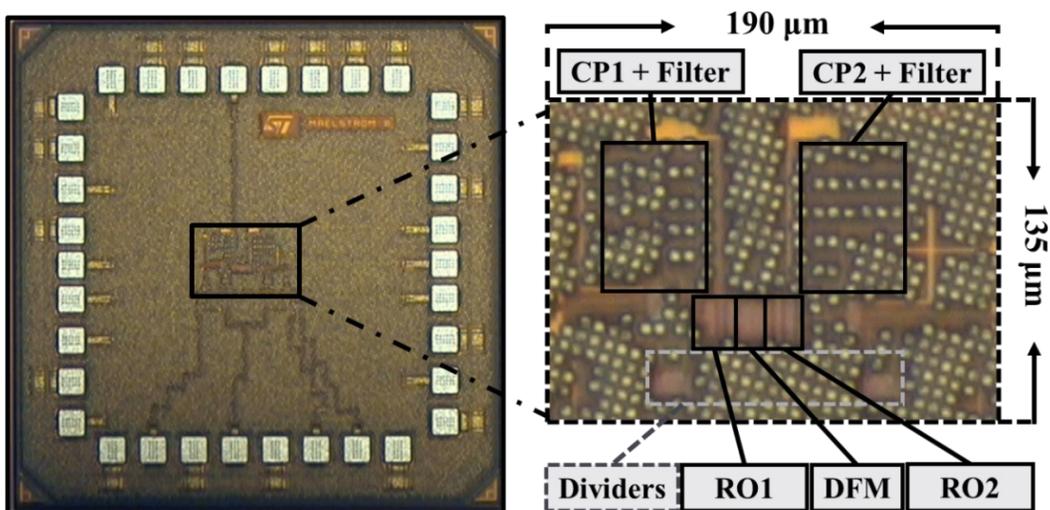


Figure 6.4 Die photography of the proposed Caliper PLL with an insert on the PLL active area.

The prototype of the Caliper PLL is fabricated in a 28nm FD-SOI CMOS process from STMicroelectronics. The die photography is shown in Figure 6.4, the active area occupies 0.0256 mm<sup>2</sup> including decoupling capacitors. Mostly composed of digital building blocks, a major part of the core is filled by the two passive loop filters (17 % of the total area).

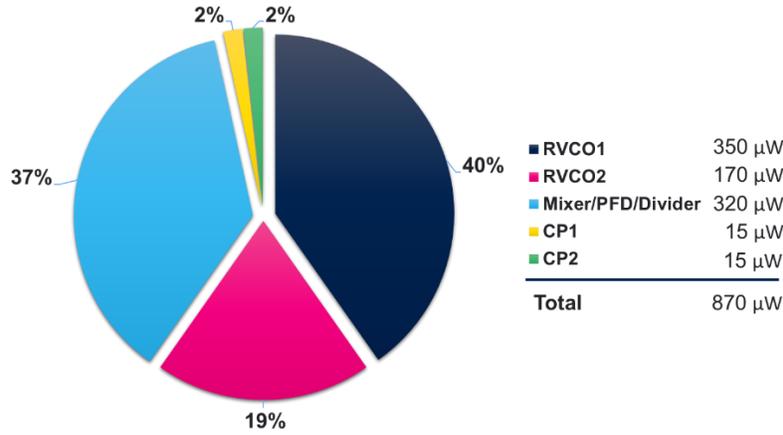


Figure 6.5: Measured power consumption of the Caliper PLL.

Illustrated in Figure 6.5, the total power consumption is measured at 870 μW under a 1V voltage supply. The two ring oscillators consume respectively 350 μW for the primary loop RVCO<sub>1</sub> and 170 μW for the secondary loop RVCO<sub>2</sub>. The power of the digital parts is 320 μW including the four frequency dividers, the down-converter frequency mixer, and the two phase-frequency detectors. Finally, each charge pump consumes 15 μW. One can notice that the two ring-oscillators are the dominant contributors of the total power consumption. However, the power consumption could be reduced further considering that the digital building blocks such as the frequency dividers represent 35 % of the total power consumption.

Symbol	Equation	Name	Values	Units
$f_{REF}$	-	Common reference frequency	440	MHz
$f_{IN1}$	$f_{REF}/R$	Primary loop internal frequency	22	MHz
$f_{IN2}$	$f_{REF}/(R+X)$	Secondary loop internal frequency	20	MHz
R	-	Primary loop input frequency divider	20	-
R+X	-	Secondary loop input frequency divider	22	-

Table 6A: Caliper PLL parameters.

For clarity purposes, Table 6A sums up the frequency parameters of the Caliper PLL. The prototype PLL locks on a frequency range from 2.28 GHz to 2.5 GHz with a common 440 MHz reference frequency. The BLE center of the band 2.420 GHz output frequency is obtained by the feedback dividers values of  $N_1 = 70$  and  $N_2 = 44$  which verifies the output frequency relation:

$$f_{OUT} = N_1 \cdot f_{IN1} + N_2 \cdot f_{IN2} \quad (6.1)$$

where  $f_{IN1}$  is the internal frequency of the primary loop and  $f_{IN2}$  is the internal frequency of the secondary loop. The measured frequency resolution of  $\Delta f = 2$  MHz is also verified in measurement which settles the final proof of concept of the Caliper PLL architecture.

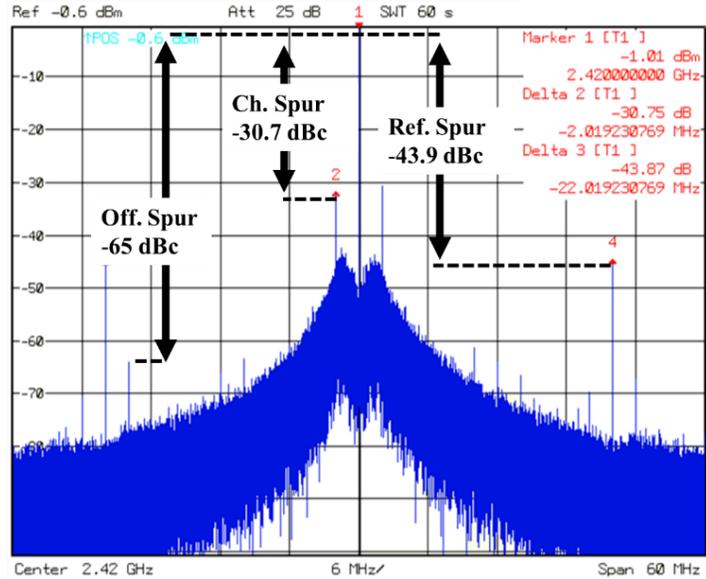


Figure 6.6: Measured frequency spectrum at a 2.420 GHz output frequency (Caliper PLL mode).

Figure 6.6 illustrates the output spectrum for a 2.420 GHz output frequency. The measured reference spur is  $-43.9$  dBc at 22 MHz offset from the carrier corresponding to the internal frequency  $f_{IN1}$  of the primary loop. Due to the Offset-PLL topology of the proposed Caliper PLL, other spurs from the combination of the two internal frequencies  $f_{IN1}$  and  $f_{IN2}$  appear in the output spectrum [LEE\_05]. Thereby, a measured spur of  $-65$  dBc at 20 MHz from the carrier corresponds to the internal frequency  $f_{IN2}$  of the secondary loop. Furthermore, a spur of  $-30.75$  dBc is measured in the adjacent channel at 2 MHz from the carrier which is compliant with the BLE needs [BLU\_19].

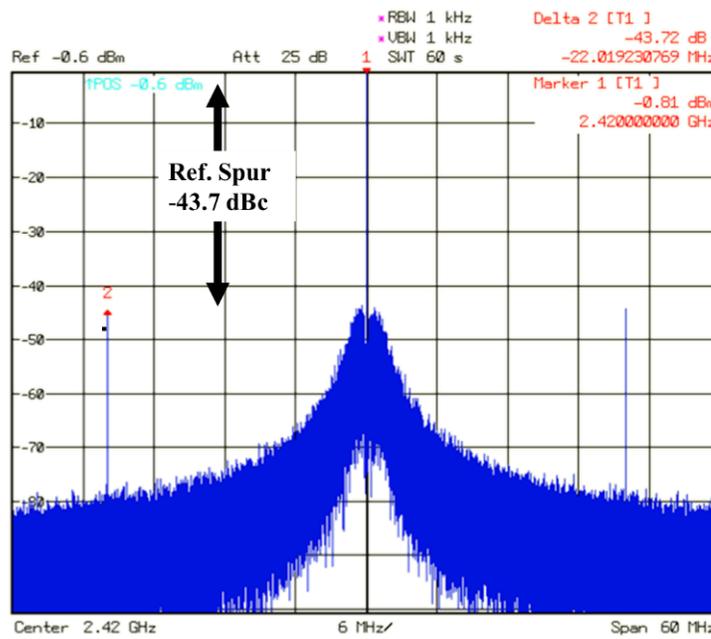


Figure 6.7: Measured frequency spectrum at a 2.420 GHz output frequency (full operation mode).

Figure 6.7 illustrates the output spectrum for the same 2.420 GHz output frequency by powering on only the primary loop with a feedback divider value of  $N_1 = 110$ . The measured reference spur is  $-43.7$  dBc at 22 MHz offset from the carrier. It confirms that the other spurs are coming from the Offset-PLL behavior of the proposed Caliper PLL.

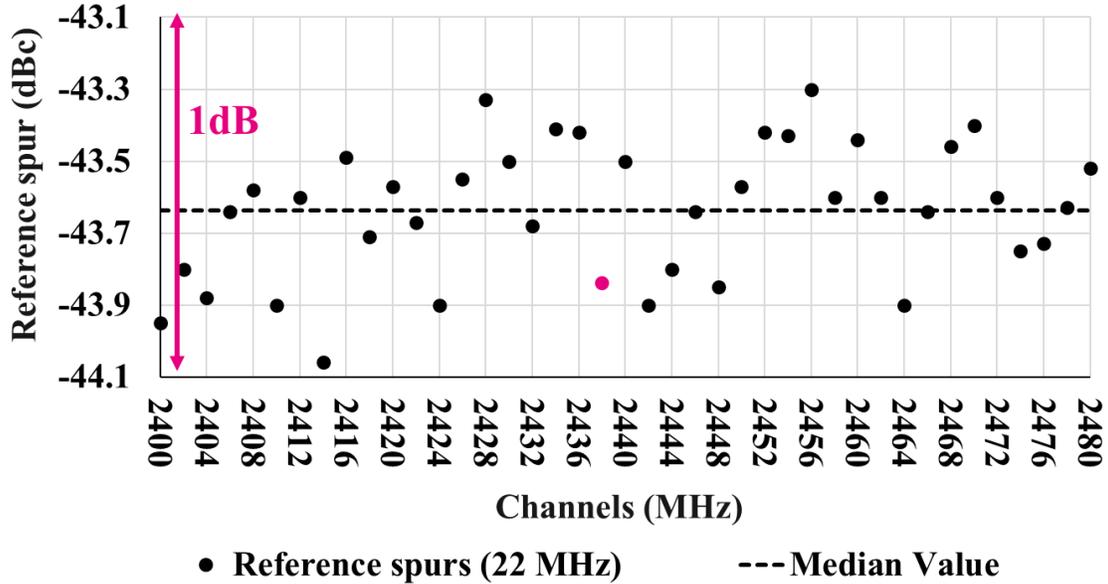


Figure 6.8: Measured reference spurs performance (at the offset frequency  $f_{IN1}$ , internal frequency of the primary loop) over all the BLE channels.

Figure 6.8 represents the measured reference spurs performance at 22 MHz offset for all BLE channels. Measured from the same chip, the reference spurs show only a 0.76 dB variation around the median value of  $-43.63$  dBc. Through the low variability, the Caliper PLL achieves a constant reference spurs performance over all the BLE channels which are in line with the BLE requirements.

In particular, the reference spurs performance is related to the charge pump architecture. Indeed, the mismatch between the current source creates a leakage current which is a contributor of the reference spurs performance. Thus, the low variability attests that the bootstrapped charge pump produces a constant performance for all BLE channels. Furthermore, it highlights the design robustness of the Caliper PLL architecture.

Around the middle of the BLE bands, the 2.438 GHz output frequency is considered to measure another type of variability. Indeed, the measurement set-up is organized to easily change the circuit on the test board. Thus, different circuits from the same wafer can be measured to determine the impacts of the manufacturing process variations on the PLL performance. The reference spurs performance is interesting to be considered for this analysis because it is sensitive to circuit variations.

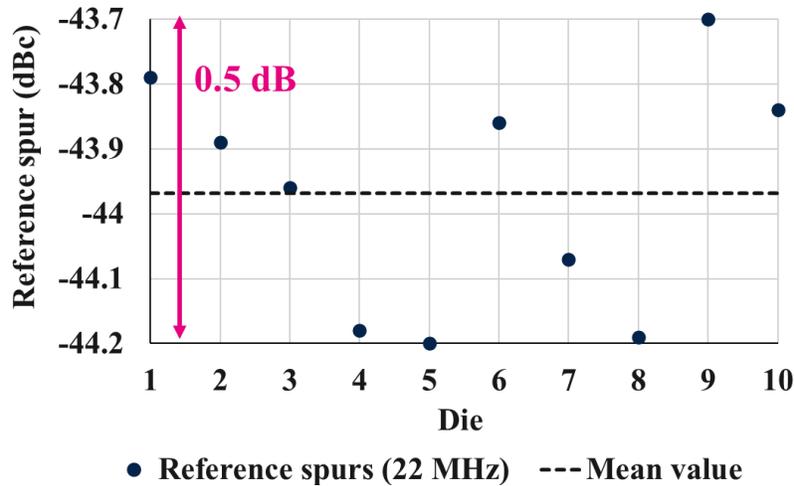


Figure 6.9: Measured reference spurs performance at a 2.438 GHz output frequency for ten different tested chips (at the offset frequency  $f_{IN1}$ , internal frequency of the primary loop).

Figure 6.9 illustrates the measured reference spurs at 22 MHz offset from the 2.438 GHz carrier for ten different random dies from the same wafer. The measured circuits show only a 0.5 dB variation around the mean value of  $-43.96$  dBc. Thus, the proposed PLL shows a reproducible and robust reference spur performance.

The low variability between different circuits indicates a robust physical implementation. The Caliper PLL shows industrial robustness to process variations by taking advantage of the layout techniques and the top-level strategy presented in Chapter 5. The 2.438 GHz output frequency is considered for the other measurements presented in this Chapter.

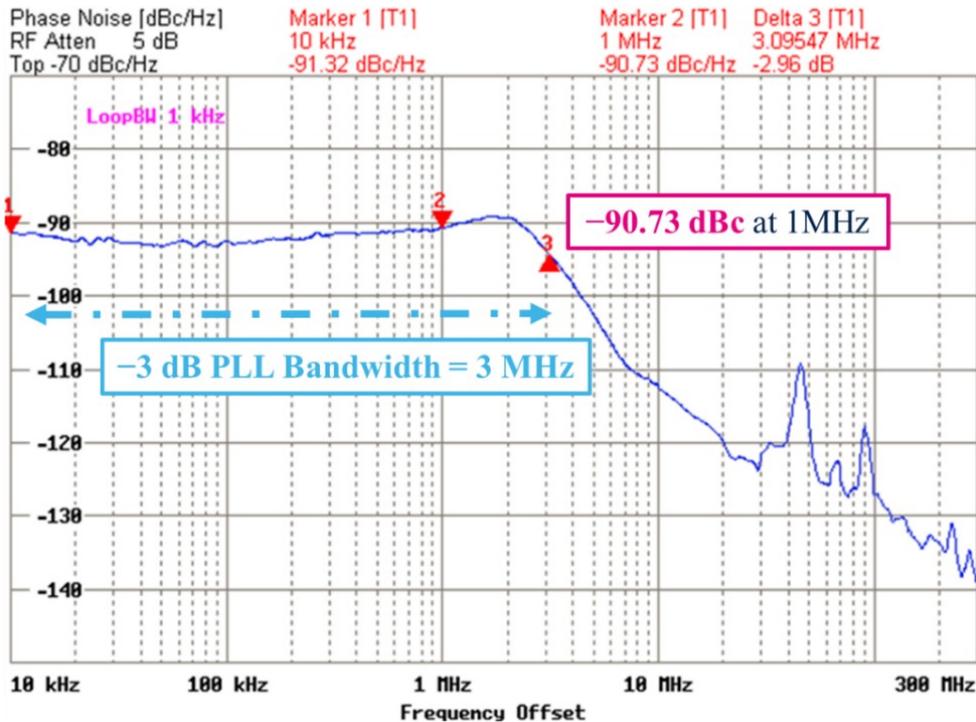


Figure 6.10: Measured output phase noise for a 2.438 GHz output frequency.

Figure 6.10 plots the measured output phase noise for a 2.438 GHz output frequency obtained by the divider values of  $N_1 = 69$  and  $N_2 = 46$ . The output phase noise measurement is very interesting because it determines the PLL bandwidth. A 3dB-bandwidth of 3 MHz is achieved. Thus, the measured PLL bandwidth is higher than the output frequency resolution of 2 MHz. It validates the “Caliper effect” of the proposed PLL architecture which creates a wideband PLL bandwidth and a smaller frequency resolution.

A measured in-band phase noise of  $-91$  dBc/Hz is achieved. Thus, the  $350 \mu\text{W}$  locked ring-oscillator achieves a  $-90.7$  dBc/Hz phase noise at 1 MHz offset from the carrier and an out-of-band phase noise of  $-112$  dBc/Hz at 10 MHz offset from the carrier. A measured 3.58 ps rms jitter is achieved by integrating the phase noise from 10 kHz to 100 MHz. The measured output phase noise is compared with the simulated phase noise from the noise model presented in Chapter 3.

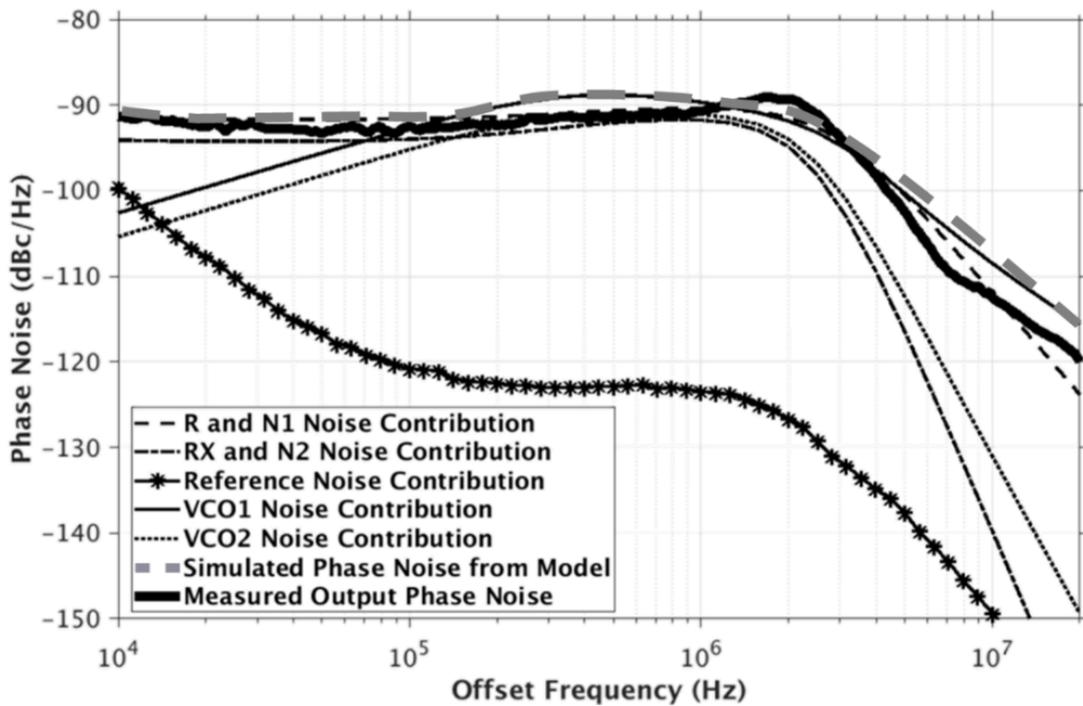


Figure 6.11: Phase noise model of the proposed PLL representing the five main noise contributions (divider noises, oscillator noise and reference noise) compared with the measured output phase noise.

Figure 6.11 illustrates the phase noise model of the proposed Caliper PLL, the model represents the main phase noise contributions with the overall simulated phase noise of the proposed PLL. It is also compared with the measured output phase noise represented in Figure 5.11. Measurement result is in line with the simulation which confirms the accuracy of the phase noise model proposed in Chapter 3. Thus, the phase noise model confirms that the internal frequency divider noise imposes the in-band noise level around  $-91$  dBc/Hz and then degrades the phase noise and jitter performances of the prototype PLL.

## 6.4 Caliper PLL performance comparison with the state-of-the-art

This section now compares the measured performances of the Caliper PLL proposed in this work with the state-of-the-art. The presented state-of-the-art gathers recent frequency synthesizers references which have emerged during the thesis work. The Caliper PLL proposes an alternative solution to fractional-N PLL for IoT applications. Thus, the state-of-the-art is composed of the best-in-class Ring-oscillator Fractional-N PLL architectures.

	This work	[ELK_16]	[KON_18]	[GON_18]	[TSA_18]	[ZHA_20]	[HE_17]
PLL Architecture	Ring Integer-N	Ring Fractional-N					LC Fractional-N
	Dual Loop	Multi-modulus divider	$\Delta\Sigma$ noise reduction	Injection-locked	Hybrid	$\Delta\Sigma$ noise reduction	Divider-less
Technology	28nm FDSOI CMOS	65nm CMOS	45nm CMOS	40nm CMOS	7nm FinFET	40nm CMOS	40nm CMOS
Frequency Range (GHz)	2.28-2.5	2.0-5.5	2.31-3.05	1.8-2.7	0.2-4.0	1.67-3.12	1.8-2.5
Output Frequency <sup>a</sup> (GHz)	2.438	2.5	2.42	2.432	3.0	2.76	2.433
Ref Frequency (MHz)	22 <sup>b</sup>	50	22.6	64	200	50	32
Ref Spur (dBc)	-44	-44	-60	-45.8	-52.3	-67.2	-62
RMS Jitter (ps)	3.58	3.6	1.5	1.6	1.05	2.26	1.98
Integ. range (Hz)	10k – 100M	10k – 100M	10k – 50M	10k – 10M	100k – 1G	1k – 100M	10k – 10M
Phase noise <sup>c</sup> (dBc/Hz)	-90.7	-91.5	-104	-108.4	-100	-100	-103
Supply voltage (V)	1	0.7	1	1	0.65	1.1	1
Power consumption (mW)	0.87	1.35	10	1.3	2.3	4.85	0.67
FOM Jitter <sup>d</sup> (dB)	-229.6	-227.6	-226.5	-234.7	-236.0	-226.1	-236.0
Area (mm <sup>2</sup> )	0.0256	0.084	0.096	0.13	0.012	0.086	0.18
Normalized Area <sup>e</sup> (10 <sup>6</sup> )	32.65	19.88	47.41	81.25	244.90	53.75	112.50
Power spending per frequency <sup>f</sup> (mW/GHz)	0.35	0.54	4.13	0.53	0.76	1.75	0.27

<sup>a</sup> All measured data is considered for the given output frequency

<sup>b</sup> Fabricated from a common reference at 440 MHz divided into a 22 MHz for the primary loop and 20 MHz for the secondary loop.

<sup>c</sup> Measured at 1 MHz offset frequency from the carrier.

<sup>d</sup> FOM Jitter = 20 log(RMS Jitter/1 s) + 10 log(Power/1 mW).

<sup>e</sup> Normalized Area = Area (mm<sup>2</sup>) / Technology node<sup>2</sup> (nm<sup>2</sup>).

<sup>f</sup> Power spending per frequency = Power consumption (mW) / Output frequency (GHz)

Table 6B: Comparison with State-of-the-Art Fractional-N PLL.

The performance of the Caliper PLL is summarized and compared with the state-of-the-art for IoT applications in Table 6B. The Caliper PLL is also compared with the best-in-class LC-oscillator Fractional-N PLL [HE\_17] which represents the virtuous goal in terms of circuit performance despite its highest area. Table 6.C details the classification used in the following figures.

Reference	This work	[ELK_16]	[KON_18]	[GON_18]	[TSA_18]	[ZHA_20]	[HE_17]
Tech. node	28nm FD-SOI	65nm CMOS	45nm CMOS	40nm CMOS	7nm FinFET	40nm CMOS	40nm CMOS
Legend							

Table 6C: Reference classification of state-of-the-art Fractional-N PLL.



Figure 6.12: State-of-the-Art comparison: phase noise performance at 1 MHz offset frequency from the carrier versus power consumption.

Figure 6.12 illustrates the phase noise performance at 1 MHz offset frequency from the carrier versus the power consumption of each reported circuit in Table 6C. The best phase noise is achieved by the injection-locked PLL architecture [GON\_18] where the noisy edges of the ring oscillator are replaced with a clean reference clock. However, a calibration loop is required to perform the injection locking technique which impacts the power consumption and the area of the overall PLL. Furthermore, the drawbacks of the injection locking technique reduce the maximal achievable PLL bandwidth. The third absolute phase noise and the best trade-off between phase noise performance and power consumption is achieved by the LC oscillator PLL [HE\_17]. All the other reported phase noises use the wideband PLL of fractional-N PLL architecture to improve the oscillator phase noise close to the carrier. A major drawback of fractional-N PLL with  $\Sigma$ - $\Delta$  noise reduction technique is represented here in [KON\_18], which achieves the second-best absolute phase noise at the cost of the highest power consumption among the reported references.

With its 2 MHz PLL bandwidth, the Caliper PLL improves the oscillator phase noise performance by achieving a  $-90.7$  dBc/Hz phase noise at 1 MHz offset frequency to the carrier. Achieving the lowest power consumption among the reported RO-based PLLs, the Caliper PLL phase noise performance meets the IoT requirements. Thus, the Caliper PLL reaches a performant trade-off between the phase noise and the power consumption. Consequently, the proposed Caliper PLL is an interesting alternative solution to fractional-N PLL architecture.

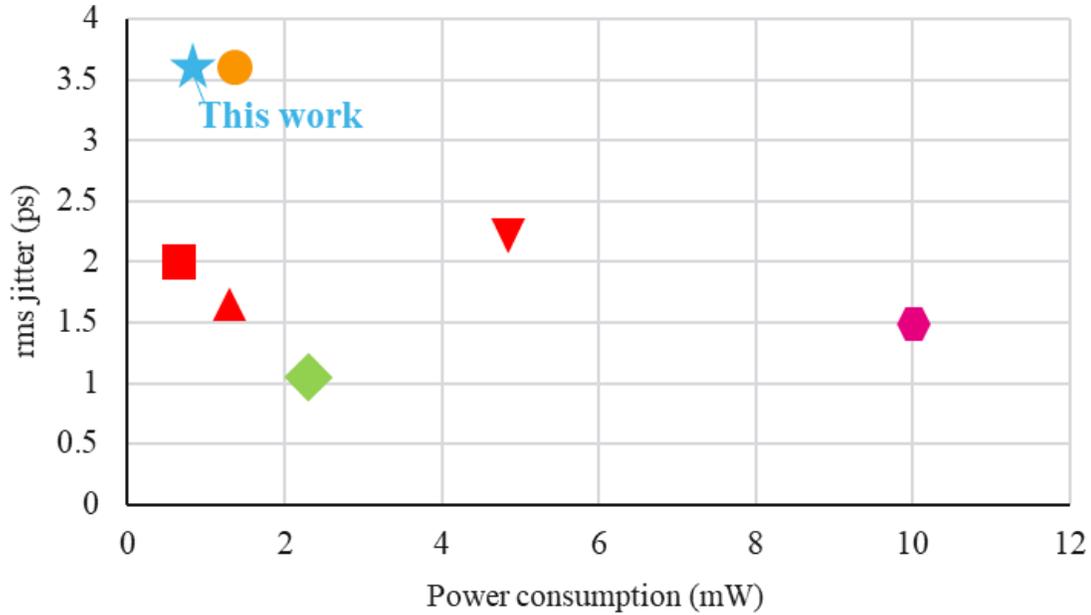


Figure 6.13: State-of-the-Art comparison: rms jitter versus power consumption.

Figure 6.13 illustrates the rms jitter versus the power consumption of each reported circuit in Table 6C. The rms jitter is calculated by the integration of the output phase noise, its unit is the second. Thus, a small rms jitter value corresponds to a better phase noise performance. Consequently, the analysis of the Figure 6.13 gives a similar conclusion than the phase noise comparison.

However, the in-band phase noise level is a major contributor of the rms jitter in wideband PLL bandwidth architecture. A high in-band noise level degrades the rms jitter performance of a PLL architecture despite a performant out-of-band phase noise. Thus, it explains why [TSA\_18] achieves a better rms jitter than [ZHA\_20] for a similar phase noise performance at 1 MHz offset from the carrier. Consequently, the Caliper PLL 3.58 ps rms jitter performance, integrated from 10 kHz to 100 MHz, is explained by its in-band noise level around  $-91$  dBc/Hz. The analysis of the rms jitter performance is very interesting to determine perspectives to improve the Caliper PLL performance.

The jitter figure-of-merit (FoM Jitter) expresses the trade-off between the rms jitter and the power consumption [GAO\_09] in:

$$\text{FoM Jitter} = 20 \log\left(\frac{\text{rms jitter}}{1\text{s}}\right) + 10 \log\left(\frac{P_{\text{DC}}}{1\text{ mW}}\right) \quad (6.1)$$

The unit of the FoM jitter is the decibel, a smaller FoM Jitter corresponds to a better frequency synthesizer design. This figure-of-merit is commonly used to compare PLL architectures.

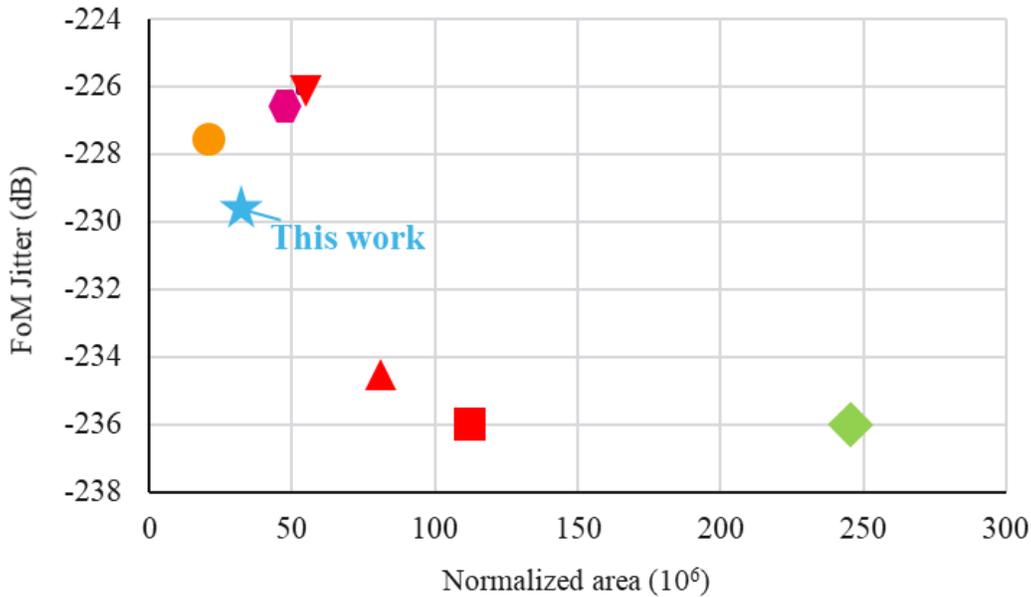


Figure 6.14: State-of-the-Art comparison: FoM jitter versus normalized area.

Figure 6.14 illustrates the FoM jitter versus the normalized area of each reported circuit in Table 6C.

A dimensionless metric named normalized area is defined as the ratio of the absolute active area in  $\text{mm}^2$  to the technology node squared in  $\text{nm}^2$ . Mostly based on digital building blocks, the Caliper PLL achieves a compact design by being integrated into the smallest CMOS planar technology node. Consequently, the proposed dual-loop architecture obtains the best absolute area among planar CMOS technologies. However, the passive devices used in the PLL loop filter are not taking benefit of the technology scalability. In particular, [TSA\_18] is the smallest technology node among all the reported references while achieving the highest normalized area. Thus, the normalized area parameter draws a fair comparison between PLL architectures over several technology nodes.

As represented in Figure 6.14, The Caliper PLL achieves the second-best normalized area after [ELK\_16] which has replaced the analog loop-filter by a digital loop-filter architecture. Thus, the proposed Caliper is a competitive IoT solution in regards to the technology node integration.

The Caliper PLL achieves a FoM Jitter of -229.6 dB in line with the State-of-the-Art Ring fractional-N PLL architectures. The best FoM jitter is achieved by [HE\_17] using the LC-oscillator at the cost of the higher normalized area among CMOS planar technology.

Thus, the Caliper PLL reaches a performant trade-off between the FoM jitter performance and the normalized area metric. Consequently, the proposed Caliper PLL is an interesting alternative solution to compact Ring fractional-N PLL architecture.

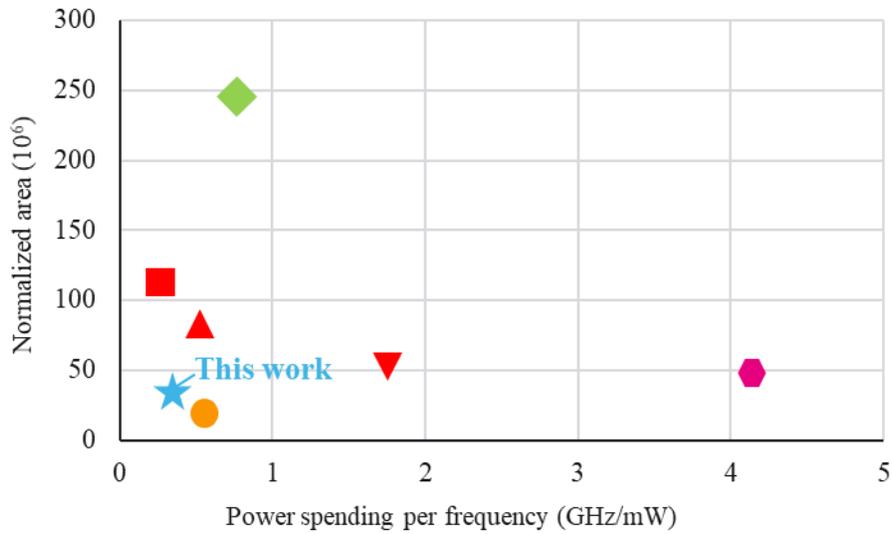


Figure 6.15: State-of-the-Art comparison: Normalized area versus power spending per frequency.

Figure 6.15 illustrates the normalized area versus the power spending per frequency of each reported circuit in Table 6C. A metric named power spending per frequency is defined as the ratio between the power consumption in mW and the output frequency in GHz. This metric represents how much the PLL circuit has to burn power to achieve the targeted output frequency. The proposed Caliper PLL achieves the best power spending per frequency among the reported RO-based PLLs. Moreover, the Caliper PLL gets close to the power spending per frequency of the LC-based PLL [HE\_17]. Thus, the Caliper PLL achieves an ultra-low power compact solution for IoT applications.

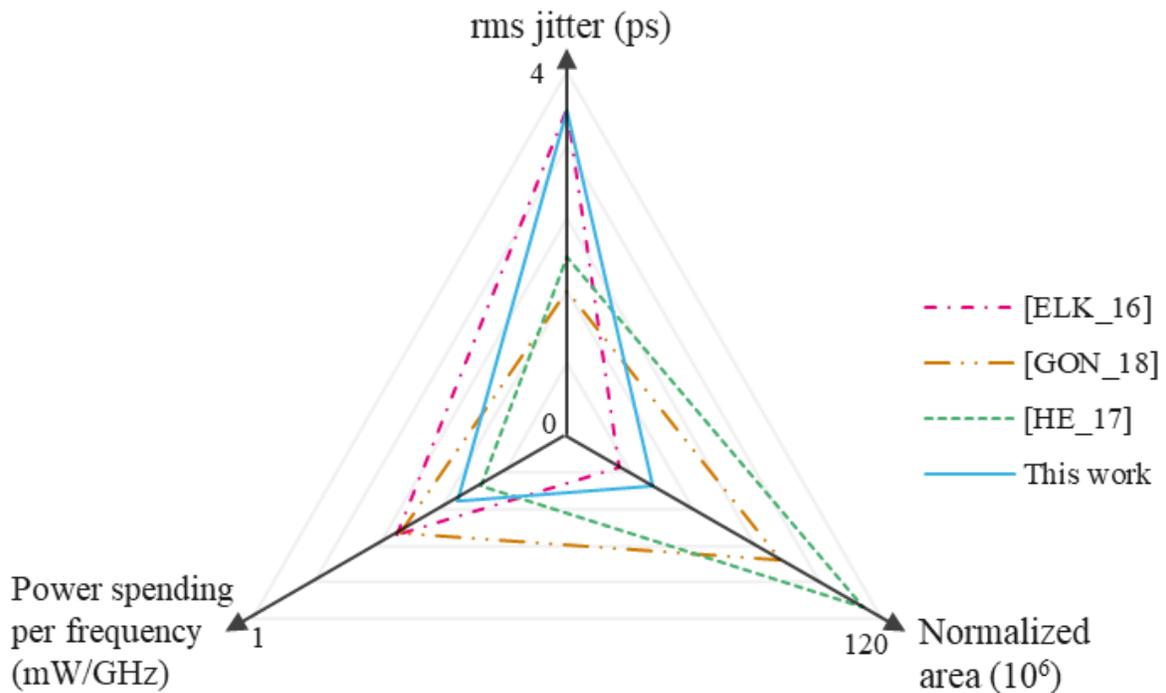


Figure 6.16: Compromise representation between the rms jitter, power spending per frequency and area.

Moreover, the Caliper PLL exhibits system-level performance in line with the best-in-class state-of-the-art while reaching a compromise between noise performance, power consumption and silicon area. Figure 6.16 illustrates this compromise where the rms jitter, the power spending per frequency, and the area are depicted for the four smallest power consumption references of Table 6C.

The proposed Caliper PLL is an original dual-loop integer-N topology to compete with the commonly used fractional-N PLL architectures for IoT applications. In order to reach the IoT challenges in terms of low power consumption and small silicon footprint, the Caliper PLL uses RO topology while dealing with a very limited power budget which impacts the RO noise performance. Thus, the proposed solution takes benefit of the FD-SOI technology combined with its architectural PLL features to achieve a performant frequency synthesizer in line with the state-of-the-art of ultra-low power ring oscillator fractional-N PLL architectures.

Considering all these concerns, we can state that the presented solution offers an interesting overall compromise. Moreover, such a solution is a good candidate for technology node straightforward portability, and it should take even more advantages from future Silicon technology nodes.

### 6.5 Conclusion

This chapter details the measurement results of the proposed Caliper PLL. The first section of this chapter details the on-chip measurements set-up. Implemented in 28nm FD-SOI CMOS technology, the chip is encapsulated in a package to be reported on a printed circuit board by a socket device. This strategy is chosen to easily perform measurements on different dies without soldering them on the test board. Thus, variability of the PLL performances is measured to determine its robustness to process variations.

The measured Caliper PLL achieves the IoT application challenges highlighted in Chapter 2. The Caliper PLL has used the advantages of the FD-SOI technology to acquire a low power consumption and a small silicon footprint. The Caliper PLL reaches a compact sub-mW solution because the PLL architecture is mostly based on digital building blocks. Even if the two ring-oscillators are the main contributors, the measured power budget shows perspectives to further reduce the power consumption. Finally, Caliper PLL specifications are verified in measurement. The 2 MHz frequency resolution is confirmed in measurement. In particular, output spectrum measurement verifies the PLL locked state. A constant reference spurs performance is measured from the same chip for all the BLE channels. Thus, the constant operation over all PLL channels validates the design specifications studied in Chapter 5. Furthermore, the reference spurs performance is measured for ten different random dies from the same wafer to evaluate the Caliper PLL robustness to process variations. Through a low variability, the Caliper PLL achieves a reproducible and robust reference spurs performance. The measured output phase noise shows a higher 3 MHz PLL bandwidth than the 2 MHz PLL frequency resolution which confirms the “Caliper effect” of the PLL architecture. Furthermore, the measured phase noise is in line with the simulation which confirms the accuracy of the phase noise model.

The measured performances of the Caliper PLL proposed in this work are compared with the complete state-of-the-art of IoT frequency synthesizer. The state-of-the-art is composed of the best-in-class ULP ring-oscillator fractional-N PLL as the Caliper PLL is considered as an alternative solution to fractional-N PLL architecture. The Caliper PLL improves the RO phase noise performance close to the carrier by its wideband PLL bandwidth without extra power consumption. Despite a rms jitter performance limited by the in-band phase noise level, the Caliper PLL achieves a FoM jitter performance in line with the state-of-the-art of RO-based fractional-N PLLs. Through the introduced normalized area metric, the Caliper PLL is a competitive solution considering the technology node scalability. Along these lines, the Caliper PLL achieves an ultra-low power compact solution for IoT applications.

Thus, the proposed frequency synthesis achieves a state-of-the-art solution in FD-SOI technology. Furthermore, the proposed Caliper PLL offers an interesting overall compromise between the RF performances, the power consumption, and the core area. Mostly based on digital blocks to reduce power consumption and area, the Caliper PLL shows an industrial robustness scalable to others FD-SOI nodes. Consequently, such a solution is a good candidate for technology node straightforward portability, and it should take even more advantages from future silicon technology nodes.



# 7 Conclusion and Perspectives

## 7.1 General conclusion

In this thesis, the challenges of Internet-of-Things (IoT) frequency synthesizer have been identified and addressed. Mass deployment is only possible with low cost connected devices showing a low power consumption and a small area. The first State-of-the-Art of fractional-N PLL solutions is provided to inspect the trends of recent IoT solutions. Main IoT requirements are then presented to determine the system-level specifications of our proposed solution. In this thesis, the new IoT frequency synthesizer takes benefit from specific advantages of the FD-SOI technology to achieve RF performance, low power consumption, and small area.

While the IoT challenges have been identified in Chapter 2, Chapter 3 presents the innovative PLL architecture which enables a narrow frequency resolution combined with a wide PLL bandwidth. Based on a dual loop integer-N Offset-PLL topology, the proposed PLL architecture operates as a conventional fractional-N PLL without its complexity. The frequency resolution is produced by the architectural nature of the proposed PLL. Thus, neither delta-sigma modulator (DSM) nor noise improvement techniques are needed. Named the “Caliper PLL”, the stability and the noise model of the proposed architecture are detailed. These studies have determined design specifications leading to the behavioral proof-of-concept.

Essential building block in any PLL architecture, Ring Voltage-Controlled Oscillators (RVCO) are studied in Chapter 4. Furthermore, the purpose of this chapter is to evaluate the capability of FD-SOI technology to provide efficient RVCO topologies. In particular, RVCOs present a new frequency tuning method based on the body-biasing of the transistor back-gate. The RVCO phase noise analysis under the scope of the ISF has led to study two RVCO topologies. The body-biasing frequency tuning method is verified by measurement results. Advantages of the FD-SOI technology were demonstrated to achieve performant low-power designs. The single-ended RVCO topology is chosen to be implemented in the Caliper PLL to reach high RF performance with minimal power consumption.

Chapter 5 is focused on the PLL circuit-level innovations which enable accurate and robust ULP operations. The two ring oscillators are implemented with simple single-ended body-bias controlled CMOS inverters, the extended frequency tuning capability is directly enabled by the FD-SOI specific feature. The proposed digital Down-conversion Frequency Mixer (DFM) does not require any extra selective passive filter. It operates with single-ended oscillators implying a

reduced power consumption. The DFM only requires quasi-quadrature inputs from the ring oscillators which further reduces the overall power consumption. A robust bootstrapped charge-pump implementation is also presented, enabling a constant operation over all PLL channels. Finally, the top-level strategy and layout techniques are presented to design a robust and compact implementation of the proposed solution.

The final chapter is dedicated to the measurement results of the proposed PLL architecture fully integrated in FD-SOI technology and its comparison with the State-of-the-Art Ring-oscillator fractional-N PLLs. The proposed solution presents an expanded PLL bandwidth which improves the ring-oscillator (RO) phase noise behavior close to the carrier. Robustness to process variability is explored by performing die-to-die measurements. The design choices enable constant reference spurs performance through the whole BLE frequency range. The presented PLL implementation exhibits system-level performances in line with the best-in-class State-of-the-Art. The proposed PLL architecture achieves the lowest power consumption among the reported RO-based PLLs and it gets close to the power consumption of LC-based PLLs. Moreover, the proposed dual-loop architecture obtains the best absolute area among planar CMOS technologies. The presented solution offers an interesting overall compromise between RF performances, power consumption and area. The proposed frequency synthesis achieves a State-of-the-Art solution in FD-SOI technology, and it exhibits an industrial robustness scalable to others FD-SOI nodes.

The thesis work presented in this manuscript carries out the full study of a PLL-based frequency synthesizer. First, the specifications of an IoT frequency synthesizer have been studied. The analysis begins with the IoT context which gives some system-level limitations. Analysis of the IoT frequency synthesizer state-of-the-art has determined the achievable solutions to handle these limitations. Thus, the commonly used PLL architecture solution to fulfill the IoT requirements in actual IoT frequency synthesizers is RO-based fractional-N PLL reaching a fine frequency resolution and a wide PLL bandwidth. Nevertheless, this solution shows a major limitation in terms of spectral purity and power consumption. This analysis is very important because it has determined the field of innovation where this thesis work takes place. Thus, the proposed Caliper PLL presented in this manuscript aims to revisit the classical integer-N PLL architecture with a wideband PLL bandwidth while achieving a small frequency resolution. Thus, the proposed solution studied in this thesis targets to be an alternative to fractional-N PLL without dealing with its complexity.

Once the PLL specifications have been determined, the proposed Caliper PLL and its properties are studied to demonstrate the proof-of-concept of the proposed architecture. The design specifications of the Caliper PLL building block are carried out by using the specific advantages of the FD-SOI technology to reach the performance targets. Indeed, it is important not to dissociate the circuit from its technology node. The system architecture and the technology node are representing both sides of a performant circuit. Furthermore, specific precautions have been taken

during the physical implementation of the Caliper PLL to produce a robust design to process variations.

Implemented in 28nm FD-SOI technology, the measured performance of the Caliper PLL meets his expectations. The Caliper PLL properties in terms of frequency resolution and PLL bandwidth are demonstrated in measurements. Furthermore, the proposed Caliper PLL reaches the IoT challenges by achieving state-of-the-art solution in FD-SOI technology. The proposed solution offers an interesting overall compromise between the RF performances, the power consumption, and the core area. Furthermore, the Caliper PLL shows an industrial robustness which is a major opportunity from a perspective of industrial production.

The original contributions presented in this manuscript are the following:

- An innovative dual-loop integer-N PLL architecture has been proposed, targeting ultra-low power compact frequency synthesizer solution for IoT applications.
- A new frequency tuning method through transistors' body-biasing has been proposed for RVCOs. This enables a wide linear range of frequency control at minimal power consumption.
- A fully digital down-conversion frequency mixer has been proposed, which generates the difference frequency without using an extra passive filter and operates with quasi-quadrature signals.
- A robust charge-pump circuit architecture has been proposed, enabling constant performances based on a control loop to compensate its output voltage variations.
- The silicon physical implementation of the proposed PLL architecture has been taped out first time right, reaching the initial targeted performances. Moreover, it demonstrates an interesting compromise between RF performances, power consumption, and area.

## 7.2 Perspectives

- Bootstrapped charge pump architecture

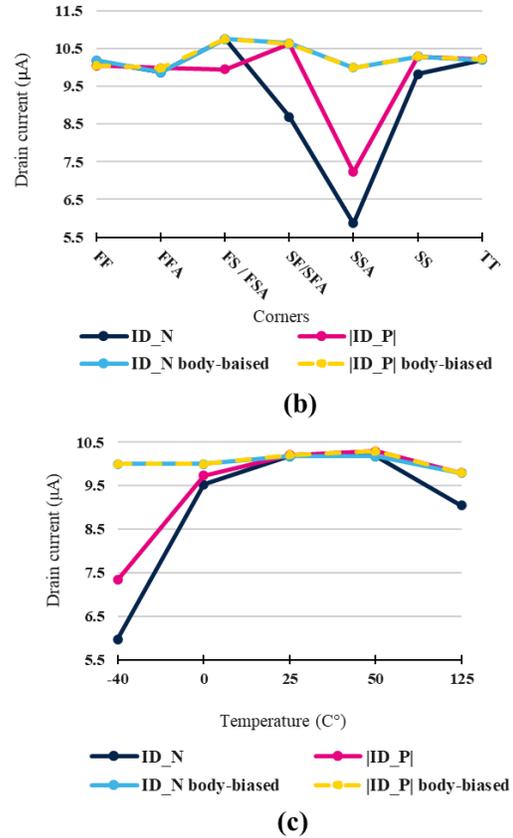
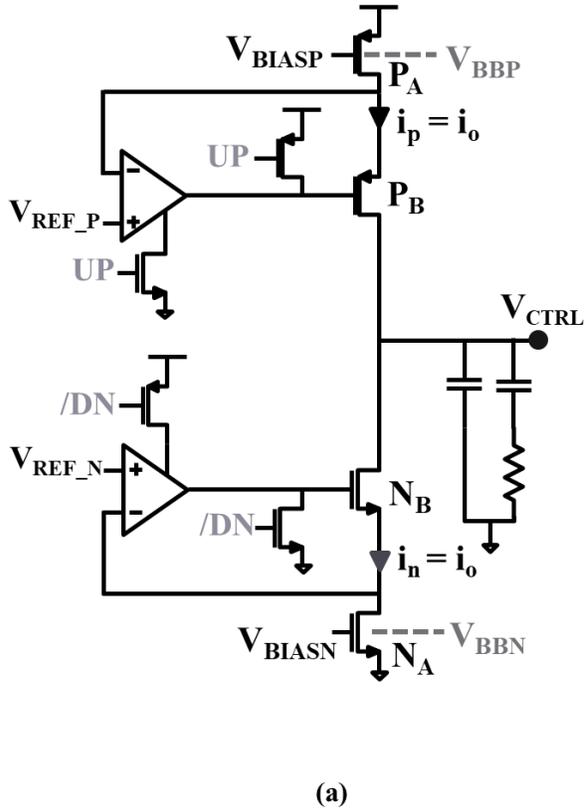


Figure 7.1: Bootstrapped charge pump architecture (a), Simulated  $i_N$  and  $i_P$  current recovery through body-biasing under corner variation (b) and (c) under temperature variation for the typical corner.

Detailed in Chapter 5, the proposed bootstrapped charge pump architecture is represented in Figure 7.1(a). Nominal values of  $i_N$  and  $|i_P|$  vary with the Process-Voltage-Temperature (PVT) variations. Represented in Figure 7.1(b),  $i_N$  and  $|i_P|$  currents are simulated under all the process corners to visualize the variations due to the industrial manufacturing process. As expected, the nominal  $i_N$  and  $|i_P|$  currents vary around the 10  $\mu\text{A}$  designed in the typical corner (TT). Figure 7.1(c) represents the  $i_N$  and  $|i_P|$  current in the typical corner (TT) with a temperature variation between  $-40^\circ\text{C}$  and  $120^\circ\text{C}$ . For each case, equality between the  $i_N$  and  $|i_P|$  current can be recovered by biasing the back-gate of the  $N_A$  and  $P_A$  transistors.

Thus, a promising perspective is to add a current control through the back-gate of  $N_A$  and  $P_A$  transistors. Moreover, the control does not impact the performance of the charge pump architecture. This current control aims to improve the reference spurs performance of the overall PLL. This another usage of the body-biasing control is very efficient to provide robust designs only achievable in FD-SOI technology.

- BLE in-context full implementation

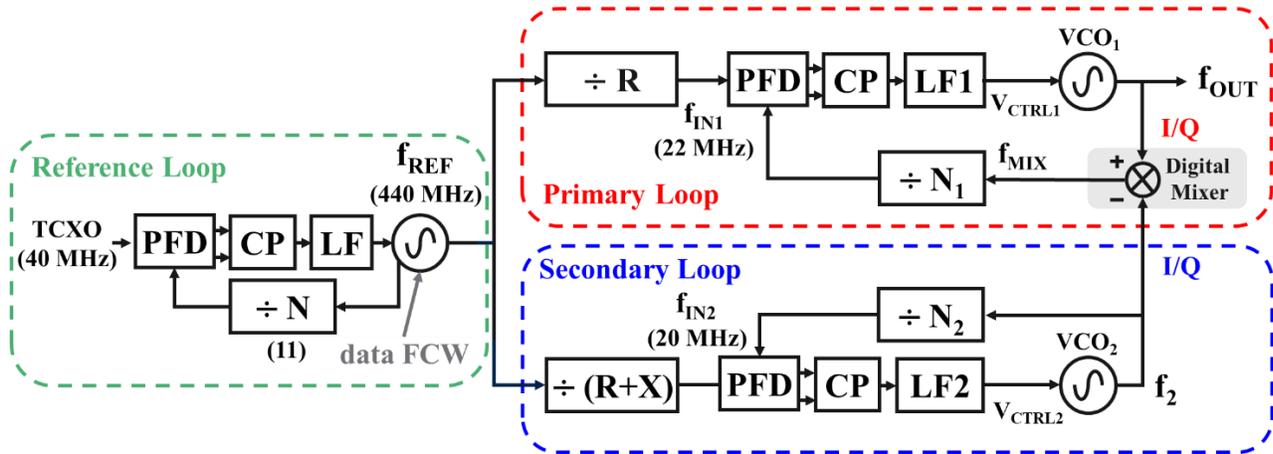


Figure 7.2: Reference loop addition to generate the 440 MHz frequency.

A possible in-context implementation is given in Figure 7.3. Actual BLE transceivers [TAM\_20] provide PLL architectures with direct Tx modulation capability. The transmitted data are transformed into Frequency Command Words (FCW) to modulate the oscillator frequency. Thus, the oscillator frequency variations are an image of the transmitted data. This specification avoids the use of a mixer on the Tx path to save power consumption (in the case of an active mixer) and area.

Instead of modulating one of the VCOs inside the Caliper PLL, an interesting perspective should be to perform this modulation on the  $f_{REF}$  reference frequency. Due to its wide PLL bandwidth, the Caliper PLL can track the  $f_{REF}$  instantaneous frequency variations while maintaining the PLL in a locked state.



# A Open-loop phase margin and open-loop transfer function

## A.1 Third order PLL open-loop phase margin computation

This appendix provides the details of the phase margin computation. Figure A.1 represents the Laplace representation of a single loop PLL.

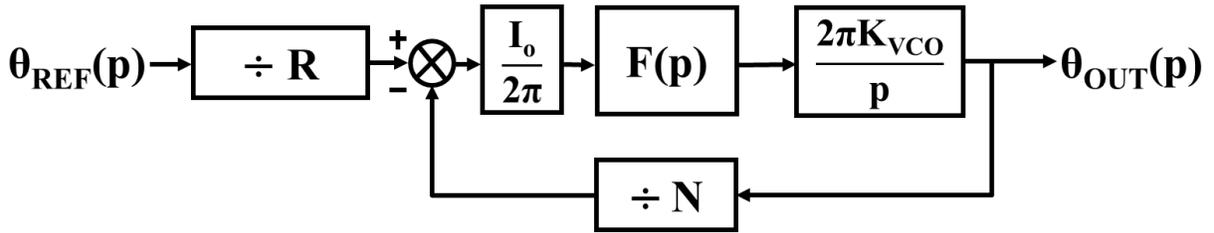


Figure A.1: Simple loop PLL phase domain model.

The closed-loop Laplace transfer function is expressed as:

$$H_{CL1}(p) = \frac{N_1}{R} \cdot \frac{H_{OL}(p)}{1 + H_{OL}(p)} \quad (\text{A. 1})$$

where  $H_{OL}(p)$  is the open-loop Laplace transfer function given as:

$$H_{OL}(p) = \frac{I_o}{2\pi} \cdot F(p) \cdot \frac{2\pi K_{VCO}}{p} \cdot \frac{1}{N} \quad (\text{A. 2})$$

Considering the filter expressed as:

$$F(p) = \frac{1}{p C_B} \frac{p + \omega_z}{p + \omega_p} \quad (\text{A. 3})$$

The open-loop transfer function is written as:

$$H_{OL}(p) = \left(\frac{\omega_k}{p}\right)^2 \cdot \frac{1 + \frac{p}{\omega_z}}{1 + \frac{p}{\omega_p}} \quad (\text{A. 4})$$

where the zero and pole pulsations are expressed as:

$$\omega_k = \sqrt{\frac{K_{VCO} I_o}{N(C_A + C_B)}}; \omega_z = \frac{1}{R_A C_A}; \omega_p = \frac{1}{R_A} \cdot \left( \frac{1}{C_A} + \frac{1}{C_B} \right) \quad (\text{A. 5})$$

For the phase margin calculation, the argument of the open-loop transfer function is needed. This calculus is detailed below:

$$\arg(H_{OL}(j\omega)) = \arg\left( \left( \frac{\omega_k}{j\omega} \right)^2 \cdot \left( \frac{1 + \frac{j\omega}{\omega_z}}{1 + \frac{j\omega}{\omega_p}} \right) \right) \quad (\text{A. 6})$$

$$\arg(H_{OL}(j\omega)) = \arg(\omega_k^2) - \arg((j\omega)^2) + \arg\left(1 + \frac{j\omega}{\omega_z}\right) - \arg\left(1 + \frac{j\omega}{\omega_p}\right) \quad (\text{A. 7})$$

$$\arg(H_{OL}(j\omega)) = 0 - 2 \cdot \arctan(\omega) + \arctan\left(\frac{\omega}{\omega_z}\right) - \arctan\left(\frac{\omega}{\omega_p}\right) \quad (\text{A. 8})$$

$$\arg(H_{OL}(j\omega)) = 0 - 2 \cdot \frac{\pi}{2} + \arctan\left(\frac{\omega}{\omega_z}\right) - \arctan\left(\frac{\omega}{\omega_p}\right) \quad (\text{A. 9})$$

Considering the unity-gain pulsation  $\omega_u$  when  $|H_{OL}(\omega_u)|=1$ , the phase margin is expressed as:

$$\phi_m = \arg(H_{OL}(j\omega_u)) + \pi \quad (\text{A. 10})$$

$$\phi_m = -\pi + \arctan\left(\frac{\omega_u}{\omega_z}\right) - \arctan\left(\frac{\omega_u}{\omega_p}\right) + \pi \quad (\text{A. 11})$$

$$\phi_m = \arctan\left(\frac{\omega_u}{\omega_z}\right) - \arctan\left(\frac{\omega_u}{\omega_p}\right) \quad (\text{A. 12})$$

The optimum value is set at 45 degrees. However, to guarantee a good trade-off between stability and settling time, the phase margin  $\phi_m$  between the range of 30 to 60 degrees. Considering this maximum value of  $\phi_m$ , computation on the phase margin is proceeded. In order to express the maximum value of the phase margin, the derivative of the phase margin expression is expressed as:

$$\frac{\partial \phi_m}{\partial \omega} = \frac{1}{\omega_z} \cdot \frac{1}{1 + \left(\frac{\omega_u}{\omega_z}\right)^2} - \frac{1}{\omega_p} \cdot \frac{1}{1 + \left(\frac{\omega_u}{\omega_p}\right)^2} = 0 \quad (\text{A. 13})$$

This relation expresses a typical relation between the pulsation as:

$$\omega_u = \sqrt{\omega_z \cdot \omega_p} \quad (\text{A. 14})$$

Considering the expression of  $\omega_z$  and  $\omega_p$ , the unity pulsation is now expressed as:

$$\omega_u = \omega_z \cdot \sqrt{1 + \frac{C_A}{C_B}} = \frac{\omega_p}{\sqrt{1 + \frac{C_A}{C_B}}} \quad (\text{A. 15})$$

Expressing the k-parameter by:

$$k = \sqrt{1 + \frac{C_A}{C_B}} \quad (\text{A. 16})$$

The maximum value of the phase margin is now written as:

$$\phi_{m_{\max}} = \arctan(k) - \arctan\left(\frac{1}{k}\right) \quad (\text{A. 17})$$

Using the trigonometric expression:

$$\tan(a - b) = \frac{\tan(a) - \tan(b)}{1 + \tan(a) \cdot \tan(b)} \quad (\text{A. 18})$$

The phase margin is written as:

$$\tan(\phi_{m_{\max}}) = \frac{1}{2} \left( \frac{k^2 - 1}{k} \right) \quad (\text{A. 19})$$

Based on the system below:

$$\tan(\theta) = \frac{\sin(\theta)}{\cos(\theta)} \quad (\text{A. 20})$$

$$\sin^2(\theta) + \cos^2(\theta) = 1 \quad (\text{A. 21})$$

Solving this system gives another expression of the phase margin as:

$$\sin(\phi_{m_{\max}}) = \frac{k^2 - 1}{k^2 + 1} \quad (\text{A. 22})$$

This relation also permits to express the k-parameter function of the phase margin as:

$$k = \sqrt{\frac{1 + \sin(\phi_{m_{\max}})}{1 - \sin(\phi_{m_{\max}})}} \quad (\text{A. 23})$$

Thus, the pulsation relation between  $\omega_z$ ,  $\omega_k$ , and  $\omega_p$  is now expressed as a function of the maximum phase margin of the system. This permits to have a first approximation on the loop-filter component parameters.

Based on the similar calculus on the phase margin, an approximate expression of the damping factor is given for a third-order PLL as:

$$\xi = \frac{1}{2} \cdot \sqrt{\frac{\frac{C_A}{C_B}}{\left(\frac{C_A \cdot C_B}{C_A + C_B}\right)}} \quad (\text{A. 24})$$

This expression is also written function of the k-parameter as:

$$\xi = \frac{\sqrt{k}}{2} \quad (\text{A. 25})$$

which enables now to have a relation between the damping factor and the targeted maximum phase margin.

## A.2 Expression of the Caliper PLL open-loop transfer function

This part details an analytical expression of the open-loop transfer function from the closed-loop transfer function. The proposed frequency synthesizer is based on a dual loop PLL topology as illustrated in Figure 3.1. Each loop represents an integer-N third-order charge pump PLL. Because the Caliper PLL is a sixth-order PLL, the chosen strategy is to consider each loop as a simple PLL to ensure separately its stability by the open-loop phase margin. The stability of the overall Caliper PLL is then ensured by using the superposition theorem.

Nevertheless, the Caliper PLL, an expression of the Caliper PLL open-loop transfer function is proposed to verify in simulation on the Bode representation the value of open-loop phase margin.

From the Caliper PLL closed-loop Laplace transfer function:

$$H_{CL}(p) = H_{CL1}(p) \cdot \left(1 + \left(\frac{R}{N_1}\right) \cdot H_{CL2}(p)\right) \quad (\text{A. 26})$$

where  $H_{CL1}(p)$  and  $H_{CL2}(p)$  represents the closed-loop transfer function of the primary loop and secondary loop, respectively.

Developed with the open-loop transfer function expression of each loop:

$$H_{CL}(p) = \frac{N_1}{R} \cdot \frac{H_{OL1}(p)}{1 + H_{OL1}(p)} \cdot \left(1 + \frac{N_2}{R+X} \cdot \frac{R}{N_1} \cdot \frac{H_{OL2}(p)}{1 + H_{OL2}(p)}\right) \quad (\text{A. 27})$$

The expression is developed by:

$$H_{CL}(p) = \frac{\frac{N_1}{R} \cdot H_{OL1}(p)}{1 + H_{OL1}(p)} \cdot \left( \frac{1 + H_{OL2}(p) + \frac{N_2}{R+X} \cdot \frac{R}{N_1} \cdot H_{OL2}(p)}{1 + H_{OL2}(p)} \right) \quad (A.28)$$

Finally, the closed-loop expression is given by:

$$H_{CL}(p) = \frac{\left( \frac{N_1}{R} \cdot H_{OL1}(p) \right) \cdot \left( 1 + H_{OL2}(p) + \frac{N_2}{R+X} \cdot \frac{R}{N_1} \cdot H_{OL2}(p) \right)}{1 + H_{OL1}(p) + H_{OL2}(p) + H_{OL1}(p) \cdot H_{OL2}(p)} \quad (A.29)$$

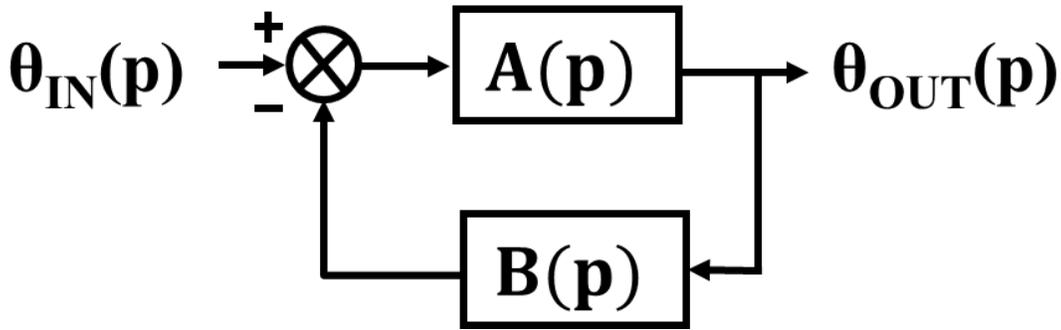


Figure A.2: General Laplace representation of a feedback system.

Figure A.2 gives a general representation of a feedback system. The close loop transfer function is then expressed as:

$$\frac{\theta_{out}}{\theta_{in}} = H_{CL}(p) = \frac{A(p)}{1 + A(p) \cdot B(p)} \quad (A.30)$$

where the open-loop transfer function is represented by  $A(p) \cdot B(p)$ .

Thus, an open-loop expression can be derived from the general expression of a feedback system, where  $A(p) \cdot B(p)$  is the open loop expression of the system. This approximated expression is used to verify the phase margin of the Caliper PLL loop:

$$A(p) \cdot B(p) = H_{OL1}(p) + H_{OL2}(p) + H_{OL1}(p) \cdot H_{OL2}(p) \quad (A.31)$$



# B Noise transfer function and phase noise contribution

## B.1 Secondary loop filter noise transfer function computation

Only the loop-filter contribution of the secondary loop is detailed in this section. Other noise transfer functions are computed based on the same methodology. Figure B.1 represents the phase noise model with the secondary loop-filter noise source.

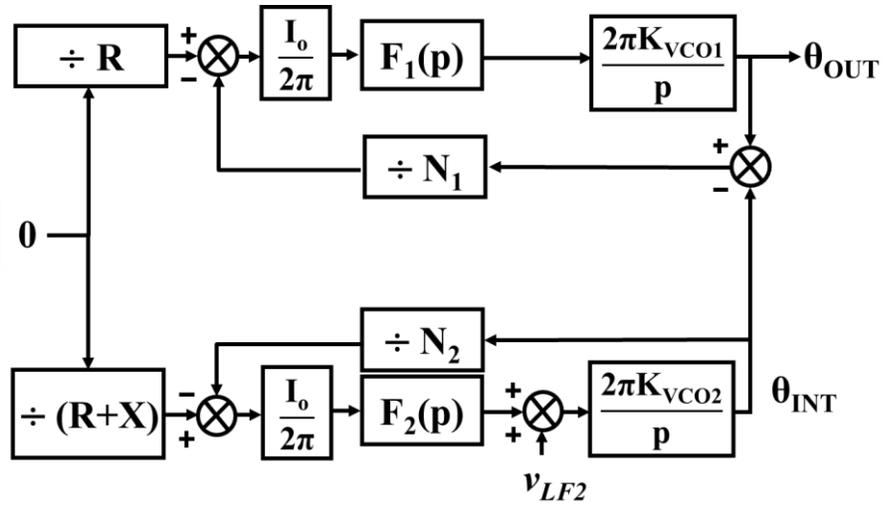


Figure B.1 : Caliper PLL phase domain model with the secondary loop-filter noise source.

Thus, the noise transfer function of the secondary loop filter noise is given by the following equations:

$$\theta_{INT} = \frac{2\pi K_{VCO2}}{p} \left( v_{LF2} + \frac{I_o}{2\pi} \cdot F_2(p) \cdot \left( \frac{0}{R+X} - \frac{\theta_{INT}}{N_2} \right) \right) \quad (B.1)$$

$$\theta_{INT} = \frac{\frac{2\pi K_{VCO2}}{p}}{1 + H_{OL2}(p)} \cdot v_{LF2} \quad (B.2)$$

where  $H_{OL2}(p)$  represents the open-loop transfer function of the secondary loop.

Thus, the total secondary loop filter noise transfer function is then expressed by:

$$H_{LPF2} = \frac{\theta_{out}}{v_{LF2}} = \frac{R}{N_1} \cdot CL_1 \cdot \frac{2\pi K_{VCO2}}{p} \cdot \frac{1}{1 + H_{OL2}} \quad (B.3)$$

The other phase transfer functions are calculated based on the same method. In particular, each primary loop phase transfer function is not influenced by the secondary loop transfer function whereas each secondary loop phase transfer function is filtered by the primary loop.

## B.2 Secondary loop filter noise contribution

The noise source of the loop filter is represented as a noise current in parallel of the real part of complex admittance of the loop filter [VAL\_08]. The single-sided power spectral density of the noise current is expressed as:

$$\mathcal{L}_{\text{filter}}(f) = 10 \log(4kT \cdot \text{Re}\{Y(f)\}) \quad (\text{B.4})$$

where  $\text{Re}\{Y(f)\}$  is the real part of the loop filter admittance.

The noise source is then filtered by the filter function, the output phase noise of the filter is then expressed as:

$$\mathcal{L}_{\text{filter out}}(f) = |F(f)|^2 \cdot \mathcal{L}_{\text{filter}}(f) \quad (\text{B.5})$$

Finally, the loop filter noise contribution is calculated as the same manner as other contributions as:

$$\mathcal{L}_{\text{filter out}}(f) = |H_{\text{LPF2}}|^2 \cdot \mathcal{L}_{\text{filter out}}(f) = |H_{\text{LPF2}}|^2 \cdot |F(f)|^2 \cdot \mathcal{L}_{\text{filter}}(f) \quad (\text{B.6})$$

where,  $|H_{\text{LPF2}}|^2$  is the amplitude of the secondary loop filter transfer function.

Thus, the total contribution of the loop filter represents a pass band behavior. Figure B.2 illustrates the intermediate stages until the computation of the loop-filter noise contribution.

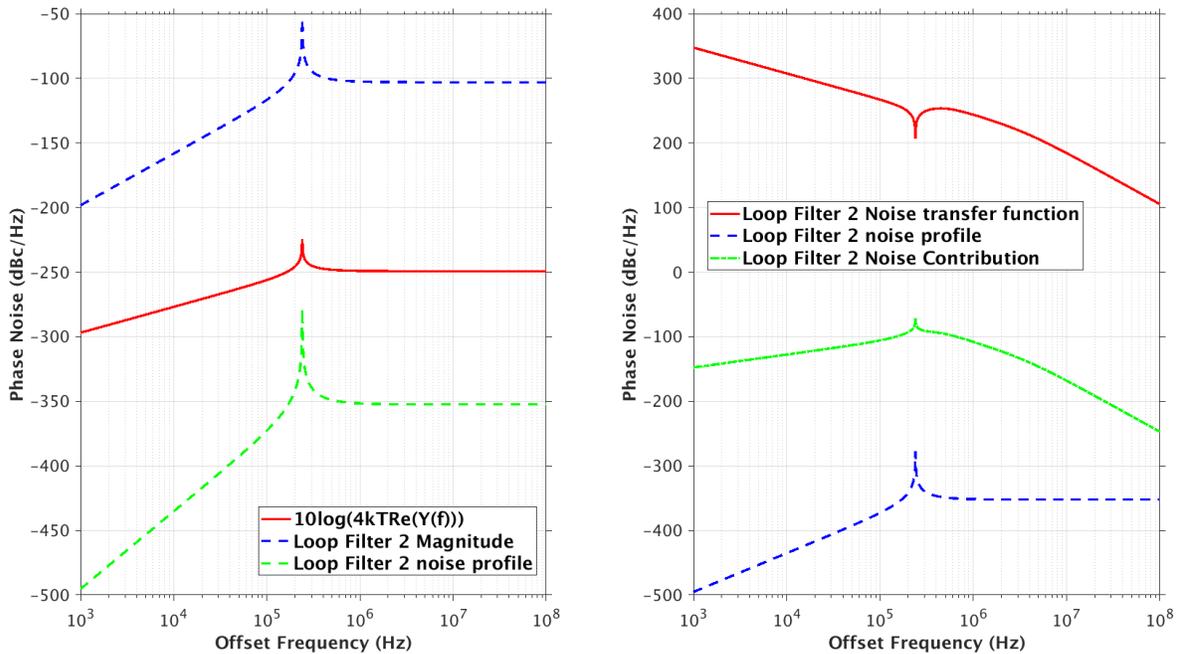


Figure B.2 : Loop filter noise profile representation (a) and (b) Loop filter noise contribution.

# C Detailed computation of Impulse Sensitivity Function

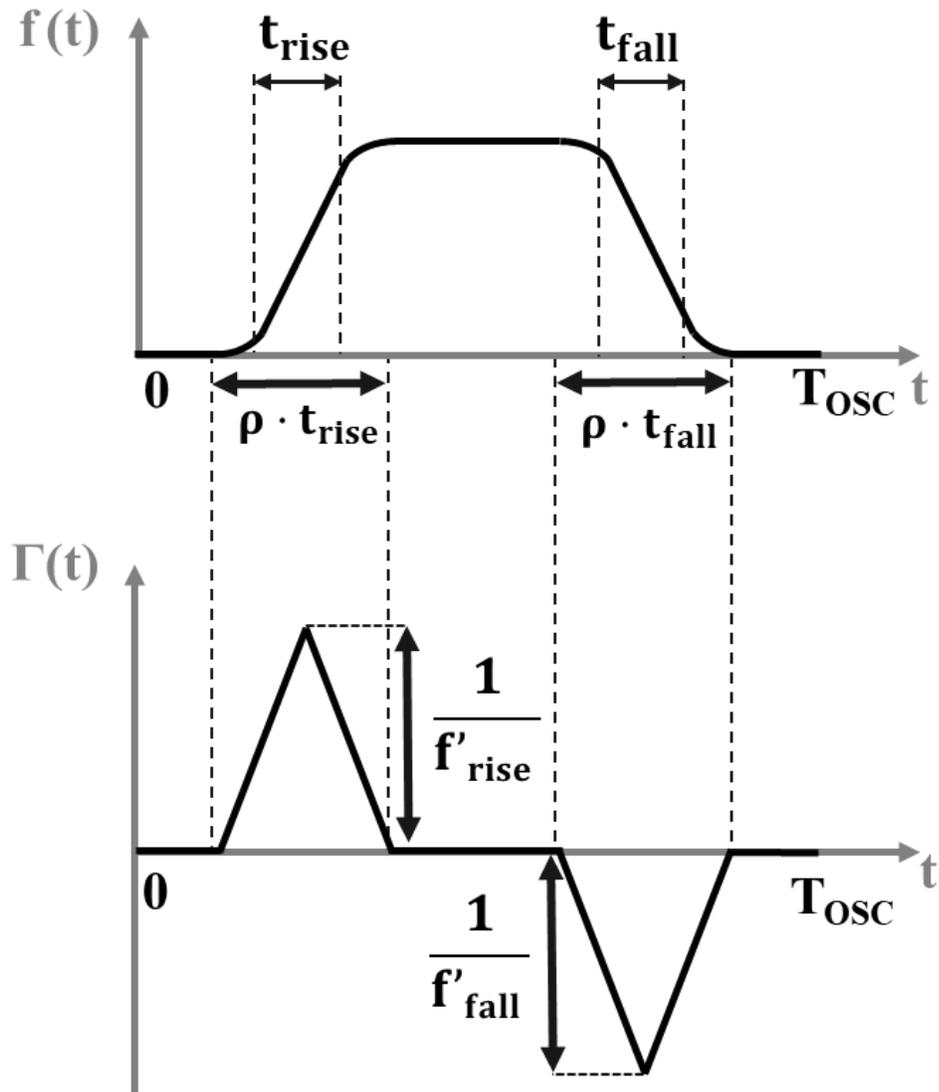


Figure C.1: waveform and ISF representation of a typical ring oscillator.

This section provides the details of the ISF calculation presented in Chapter 4. Figure C.1 represents the waveform and ISF representation of a typical ring oscillator. The approximated ISF representation is similar to [HAJ\_99], the distinction is made by the  $\rho$  constant value representing the portion of the linear part of the rise time, respectively the linear part of the fall time, to its total transition time. Contrary to the theory in [HAJ\_99], the time x-axis is used instead of the radian x-axis.

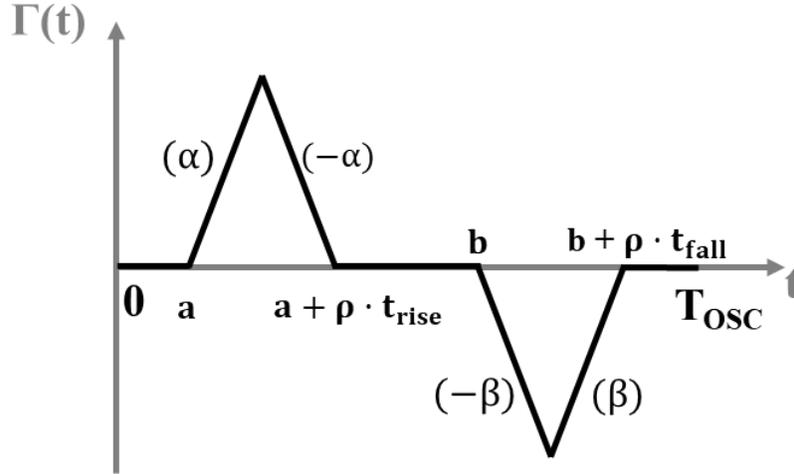


Figure C.2: Detailed ISF representation.

From the detailed representation of Figure C.2, the rms ISF value is calculated by:

$$T_{\text{OSC}} \cdot \Gamma_{\text{rms}}^2 = \int_0^{T_{\text{OSC}}} \Gamma(t)^2 dt = \int_a^{a+\rho \cdot t_{\text{rise}}} \Gamma(t)^2 dt + \int_b^{b+\rho \cdot t_{\text{fall}}} \Gamma(t)^2 dt \quad (\text{C.1})$$

Between these time intervals, the ISF function is defined by:

$$\text{for } t \in \left[ a; a + \rho \cdot \frac{t_{\text{rise}}}{2} \right] \rightarrow \Gamma(t) = \alpha(t - a) \quad (\text{C.2})$$

$$\text{for } t \in \left[ a + \rho \cdot \frac{t_{\text{rise}}}{2}; a + \rho \cdot t_{\text{rise}} \right] \rightarrow \Gamma(t) = -\alpha(t - (a + \rho \cdot t_{\text{rise}})) \quad (\text{C.3})$$

$$\text{for } t \in \left[ b; b + \rho \cdot \frac{t_{\text{fall}}}{2} \right] \rightarrow \Gamma(t) = -\beta(t - b) \quad (\text{C.4})$$

$$\text{for } t \in \left[ b + \rho \cdot \frac{t_{\text{fall}}}{2}; b + \rho \cdot t_{\text{fall}} \right] \rightarrow \Gamma(t) = -\beta(t - (b + \rho \cdot t_{\text{fall}})) \quad (\text{C.5})$$

where  $\alpha$  and  $\beta$  are the leading coefficients expressed by:

$$\alpha = \frac{2}{f'_{\text{rise}} \cdot \rho \cdot t_{\text{rise}}} \quad (\text{C.6})$$

$$\beta = \frac{2}{f'_{\text{fall}} \cdot \rho \cdot t_{\text{fall}}} \quad (\text{C.7})$$

Solving (C.1), the rms ISF value is given by:

$$\Gamma_{rms}^2 = \frac{\rho^3}{12 T_{OSC}} ((\alpha trise)^3 + (\beta tfall)^3) \quad (C.8)$$

Based on the ring oscillator period equation given in radian in [HAJ\_99]:

$$2\pi = \eta N \left( \frac{1}{f'rise} + \frac{1}{f'fall} \right) \quad (C.9)$$

with  $\eta$  is a proportionality constant representing the relationship between the propagation time  $t_d$  and the rising time  $trise$ , respectively falling time  $tfall$ . This equation is compared to the common ring oscillator period equation:

$$T_{OSC} = N(t_{dn} + t_{dp}) = \eta N (trise + tfall) \quad (C.10)$$

Derived from [HAJ\_99], the two values  $f'rise$  and  $f'fall$  are now expressed in function of  $trise$  and  $tfall$  by:

$$f'rise = \frac{T_{OSC}}{2\pi trise} \quad (C.11)$$

$$f'fall = \frac{T_{OSC}}{2\pi tfall} \quad (C.12)$$

Using (C.9), (C.11) and (C.12), the ISF rms value is expressed by:

$$\Gamma_{rms}^2 = \frac{4 \rho \pi^2}{3 T_{OSC}^3} \cdot (trise^3 + tfall^3) \quad (C.13)$$

Finally using (C.10), the ISF rms value is given by:

$$\Gamma_{rms}^2 = \frac{4 \rho \pi^2}{3 \eta^3 M^3} \cdot \frac{1 + A^3}{(1 + A)^3} \quad (C.14)$$

where A represents the ratio between the rising time  $trise$  and the falling time  $tfall$ .



# D Digital down-conversion frequency mixer

This appendix provides the details of the  $S_I(t)$  signal calculation. The Figure D.1 represents the schematic diagram of the digital mixer.

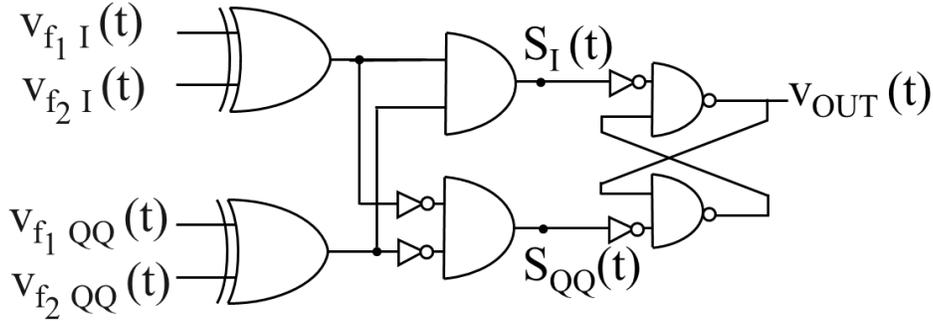


Figure D.1: Down-converter Frequency mixer circuit.

The proposed down-converter mixer uses quasi-quadrature inputs (I and QQ) from the ring oscillators ( $v_{f1}(t)$  and  $v_{f2}(t)$ ) with respectively  $f_1$  and  $f_2$  frequencies. For instance, the quasi-quadrature digital signals from the RVCO<sub>1</sub> can be expressed as:

$$v_{f1 I}(t) = A \cdot \sum_{i=0}^n \frac{\cos((2i+1)\omega_1 t)}{2i+1} \quad (D.1)$$

$$v_{f1 QQ}(t) = A \cdot \sum_{i=0}^n \frac{\cos((2i+1)\omega_1 t + \theta)}{2i+1} \quad (D.2)$$

Where  $A$  is the signal amplitude,  $\theta$  represents the phase delay between the two input signals which is close to  $\pi/4$  for quasi-quadrature. The quasi-quadrature inputs from the RVCO<sub>2</sub> share the same expressions with a  $\omega_2$  frequency.

We are considering now quasi-quadrature input signals with a phase delay  $\theta$  close to  $\pi/2$ . Thus, the four input signals are expressed with a first-order approximation ( $n = 0$ ) by:

$$v_{f1 I}(t) = A \cos(\omega_1 t) \quad (D.3)$$

$$v_{f1 QQ}(t) = A \cos(\omega_1 t + \theta) \quad (D.4)$$

$$v_{f2 I}(t) = A \cos(\omega_2 t) \quad (D.5)$$

$$v_{f2 QQ}(t) = A \cos(\omega_2 t + \theta) \quad (D.6)$$

The XOR gate is modelled as a multiplier, the AND gate is modelled as an adder and the NOT gate is modelled by a phase shift of  $\pi$  radian. Thus, the signals  $S_I$  are modelled by:

$$S_I(t) = A^2 \cdot [\cos(\omega_1 t) \cos(\omega_2 t) + \cos(\omega_1 t + \theta) \cos(\omega_2 t + \theta)] \quad (D.7)$$

The following trigonometric relations are used:

$$\cos(a + b) = \cos(a) \cos(b) - \sin(a) \sin(b) \quad (D.8)$$

$$\cos(a - b) = \cos(a) \cos(b) + \sin(a) \sin(b) \quad (D.9)$$

Form (C.8) and (C.9), we can develop :

$$\begin{aligned} \cos(\omega_1 t + \theta) \cdot \cos(\omega_2 t + \theta) &= \cos^2(\theta) \cos(\omega_1 t) \cos(\omega_2 t) \\ &- \cos(\theta) \sin(\theta) [\cos(\omega_1 t) \sin(\omega_2 t) + \sin(\omega_1 t) \cos(\omega_2 t)] + \sin^2(\theta) \sin(\omega_1 t) \sin(\omega_2 t) \end{aligned} \quad (D.10)$$

Using the relation:

$$\sin^2(\theta) = 1 - \cos^2(\theta) \quad (D.11)$$

The equation (D.7) can be written as:

$$\begin{aligned} S_I(t) &= A^2 \cdot [(1 + \cos^2(\theta)) \cdot (\cos(\omega_1 t) \cos(\omega_2 t)) + (1 - \cos^2(\theta)) \cdot (\sin(\omega_1 t) \sin(\omega_2 t)) \\ &- \cos(\theta) \sin(\theta) [\cos(\omega_1 t) \sin(\omega_2 t) + \sin(\omega_1 t) \cos(\omega_2 t)] + \sin^2(\theta) \sin(\omega_1 t) \sin(\omega_2 t)] \end{aligned} \quad (D.12)$$

which gives:

$$\begin{aligned} S_I(t) &= A^2 \cdot [(\cos(\omega_1 t) \cos(\omega_2 t)) \\ &+ \sin(\omega_1 t) \sin(\omega_2 t) + \cos^2(\theta) ((\cos(\omega_1 t) \cos(\omega_2 t)) - \sin(\omega_1 t) \sin(\omega_2 t)) \\ &- \cos(\theta) \sin(\theta) [\cos(\omega_1 t) \sin(\omega_2 t) + \sin(\omega_1 t) \cos(\omega_2 t)] + \sin^2(\theta) \sin(\omega_1 t) \sin(\omega_2 t)] \end{aligned} \quad (D.13)$$

Using (D.8) and (D.9) with:

$$\cos(a) \sin(b) + \sin(a) \cos(b) = \sin(a + b) \quad (D.14)$$

We can express the signal  $S_I(t)$  in (D.13) as:

$$S_I(t) = A^2 \cdot [\cos((\omega_1 - \omega_2)t) + \cos^2(\theta) \cos((\omega_1 + \omega_2)t) - \cos(\theta) \sin(\theta) \sin((\omega_1 + \omega_2)t)] \quad (D.15)$$

which gives:

$$S_I(t) = A^2 \cdot [\cos((\omega_1 - \omega_2)t) + \cos(\theta) [\cos(\theta) \cos((\omega_1 + \omega_2)t) - \sin(\theta) \sin((\omega_1 + \omega_2)t)] \quad (D.16)$$

Finally using (D.9), we obtain the final expression of the signal  $S_I(t)$ :

$$S_I(t) = A^2 \cdot [\cos((\omega_1 - \omega_2)t) + \cos(\theta) \cos((\omega_1 + \omega_2)t + \theta)] \quad (D.17)$$

# Bibliography

[ABI\_06]: A. A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillators," in IEEE Journal of Solid-State Circuits, vol. 41, no. 8, pp. 1803-1816, Aug. 2006.

[ALF\_15]: A. Al-Fuqaha, M. Guizani, M. Mohammadi, M. Aledhari and M. Ayyash, "Internet of Things: A Survey on Enabling Technologies, Protocols, and Applications," in IEEE Communications Surveys & Tutorials, vol. 17, no. 4, pp. 2347-2376, Fourthquarter 2015.

[ALG\_20]: A. Alghaihab, X. Chen, Y. Shi, D. S. Truesdell, B. H. Calhoun and D. D. Wentzloff, "30.7 A Crystal-Less BLE Transmitter with  $-86\text{dBm}$  Frequency-Hopping Back-Channel WRX and Over-the-Air Clock Recovery from a GFSK-Modulated BLE Packet," 2020 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 472-474.

[ARA\_10]: A. Arakali, S. Gondi and P. K. Hanumolu, "Analysis and Design Techniques for Supply-Noise Mitigation in Phase-Locked Loops," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 11, pp. 2880-2889, Nov. 2010.

[BEH\_01]: F. Behbahani, Y. Kishigami, J. Leete and A. A. Abidi, "CMOS mixers and polyphase filters for large image rejection," in IEEE Journal of Solid-State Circuits, vol. 36, no. 6, pp. 873-887, June 2001.

[BES\_07]: R.E. Best, "Phase-Locked Loops. Theory, Design and Applications", McGraw-Hill, sixth edition, New-York, USA, 2007

[BLU\_19]: SIG Bluetooth, "Core specification v5. 1," 2019.

[CAT\_17]: A. Cathelin, "Fully Depleted Silicon on Insulator Devices CMOS: The 28-nm Node Is the Perfect Technology for Analog, RF, mmW, and Mixed-Signal System-on-Chip Integration," in IEEE Solid-State Circuits Magazine, vol. 9, no. 4, pp. 18-26, Fall 2017.

[CHE\_18]: Chen et al., "A  $486\ \mu\text{W}$  All-Digital Bluetooth Low Energy Transmitter with Ring Oscillator Based ADPLL for IoT applications," 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, 2018, pp. 168-171.

[CHI\_14]: V. K. Chillara et al., "9.8 An  $860\ \mu\text{W}$  2.1-to-2.7GHz all-digital PLL-based frequency modulator with a DTC-assisted snapshot TDC for WPAN (Bluetooth Smart and ZigBee) applications," 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, 2014, pp. 172-173.

[CLE\_20]: S. Clerc, T. Di Gilio, A. Cathelin, "The Fourth Terminal, Benefits of Body-Biasing Techniques for FDSOI Circuits and Systems", Springer Nature Switzerland AG 2020, DOI 10.1007/978-3-030-39496-7.

[DEC\_14]: J. DeCuir, "Introducing Bluetooth Smart: Part 1: A look at both classic and new technologies.," in IEEE Consumer Electronics Magazine, vol. 3, no. 1, pp. 12-18, Jan. 2014.

[DIN\_18]: M. Ding et al., "A 0.8V 0.8mm<sup>2</sup> bluetooth 5/BLE digital-intensive transceiver with a 2.3mW phase-tracking RX utilizing a hybrid loop filter for interference resilience in 40nm CMOS," 2018 IEEE International Solid - State Circuits Conference - (ISSCC), San Francisco, CA, 2018, pp. 446-448.

[ELK\_16]: A. Elkholy, S. Saxena, R. K. Nandwana, A. Elshazly and P. K. Hanumolu, "A 2.0–5.5 GHz Wide Bandwidth Ring-Based Digital Fractional-N PLL With Extended Range Multi-Modulus Divider," in IEEE Journal of Solid-State Circuits, vol. 51, no. 8, pp. 1771-1784, Aug. 2016.

[DEV\_18]: Y. Deval, A. Asprilla, D. Cordova, H. Lapuyade and F. Rivet, "DLL-enhanced PLL frequency synthesizer with two feedback loops and body biasing for noise cleaning," 2018 14th IEEE Int. Conf on Solid-State and Integrated Circuit Technology (ICSICT), Qingdao, 2018, pp.1-3

[GAI\_20]: D. Gaidioz, M. De Matos, A. Cathelin and Y. Deval, "Ring VCO Phase Noise Optimization by Pseudo-Differential Architecture in 28nm FD-SOI CMOS," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain, 2020, pp. 1-4.

[GAO\_09]: X. Gao, E. A. M. Klumperink, P. F. J. Geraedts and B. Nauta, "Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 56, no. 2, pp. 117-121, Feb. 2009.

[GON\_18]: J. Gong et al., "A 1.33 mW, 1.6psrms-Integrated-Jitter, 1.8-2.7 GHz Ring-Oscillator-Based Fractional-N Injection-Locked DPLL for Internet-of-Things Applications," 2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, PA, 2018, pp. 44-47.

[HAJ\_98]: A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," in IEEE Journal of Solid-State Circuits, vol. 33, no. 2, pp. 179-194, Feb. 1998.

[HAJ\_99]: A. Hajimiri, S. Limotyrakis and T. H. Lee, "Jitter and phase noise in ring oscillators," in IEEE Journal of Solid-State Circuits, vol. 34, no. 6, pp. 790-804, June 1999.

[HAN\_04]: P. K. Hanumolu, M. Brownlee, K. Mayaram and Un-Ku Moon, "Analysis of charge-pump phase-locked loops," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 9, pp. 1665-1674, Sept. 2004.

[HAN\_14]: C. Hangmann, C. Hedayat and U. Hilleringmann, "Stability Analysis of a Charge Pump Phase-Locked Loop Using Autonomous Difference Equations," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 9, pp. 2569-2577, Sept. 2014.

[HE\_17]: Y. He et al., "24.7 A 673 $\mu$ W 1.8-to-2.5GHz dividerless fractional-N digital PLL with an inherent frequency-capture capability and a phase-dithering spur mitigation for IoT applications," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 420-42.

[HEI\_88]: J. P. Hein and J. W. Scott, "z-domain model for discrete-time PLL's," in IEEE Transactions on Circuits and Systems, vol. 35, no. 11, pp. 1393-1400, Nov. 1988.

- [HUA\_14]: Y. Huang, C. Liang, H. Huang and P. Wang, "15.3 A 2.4GHz ADPLL with digital-regulated supply-noise-insensitive and temperature-self-compensated ring DCO," 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), San Francisco, CA, 2014, pp. 270-271.
- [ISS\_19]: V. Issakov, "The State of the Art in CMOS VCOs: Mm-Wave VCOs in Advanced CMOS Technology Nodes," in IEEE Microwave Magazine, vol. 20, no. 12, pp. 59-71, Dec. 2019.
- [KIM\_16]: M. Kim, S. Choi, T. Seong and J. Choi, "A Low-Jitter and Fractional-Resolution Injection-Locked Clock Multiplier Using a DLL-Based Real-Time PVT Calibrator With Replica-Delay Cells," in IEEE Journal of Solid-State Circuits, vol. 51, no. 2, pp. 401-411, Feb. 2016.
- [KON\_16]: L. Kong and B. Razavi, "A 2.4 GHz 4 mW Integer-N Inductorless RF Synthesizer," in IEEE Journal of Solid-State Circuits, vol. 51, no. 3, pp. 626-635, March 2016.
- [KON\_18]: L. Kong and B. Razavi, "A 2.4-GHz RF Fractional- $N$  Synthesizer With  $BW = 0.25f_{REF}$ ," in IEEE Journal of Solid-State Circuits, vol. 53, no. 6, pp. 1707-1718, June 2018.
- [KUO\_17]: F. Kuo et al., "A Bluetooth Low-Energy Transceiver With 3.7-mW All-Digital Transmitter, 2.75-mW High-IF Discrete-Time Receiver, and TX/RX Switchable On-Chip Matching Network," in IEEE Journal of Solid-State Circuits, vol. 52, no. 4, pp. 1144-1162, April 2017.
- [LEE\_05]: Ching-Feng Lee and Song Tsuen Peng, "Systematic analysis of the offset-PLL output spur spectrum," in IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 9, pp. 3024-3034, Sept. 2005.
- [LI\_10]: C. Li and J. Lin, "A 1–9 GHz Linear-Wide-Tuning-Range Quadrature Ring Oscillator in 130 nm CMOS for Non-Contact Vital Sign Radar Application," in IEEE Microwave and Wireless Components Letters, vol. 20, no. 1, pp. 34-36, Jan. 2010.
- [LIU\_17]: Y. Liu et al., "An Ultra-Low Power 1.7-2.7 GHz Fractional-N Sub-Sampling Digital Frequency Synthesizer and Modulator for IoT Applications in 40 nm CMOS," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 5, pp. 1094-1105, May 2017.
- [MOH\_19]: K. S. Mohamed, "The Era of Internet of Things: Towards a Smart world", Springer Nature Switzerland DOI 10.1007/978-3-030-18133-8\_1.
- [PAR\_10]: P. Park, D. Park and S. Cho, "A Low-Noise and Low-Power Frequency Synthesizer Using Offset Phase-Locked Loop in 0.13- $\mu$ m CMOS," in IEEE Microwave and Wireless Components Letters, vol. 20, no. 1, pp. 52-54, Jan. 2010.
- [RAZ\_04]: B. Razavi, "A study of injection locking and pulling in oscillators," in IEEE Journal of Solid-State Circuits, vol. 39, no. 9, pp. 1415-1424, Sept. 2004.
- [RAZ\_19]: B. Razavi, "The Ring Oscillator [A Circuit for All Seasons]," in IEEE Solid-State Circuits Magazine, vol. 11, no. 4, pp. 10-81, Fall 2019.

[RIL\_93]: T. A. D. Riley, M. A. Copeland and T. A. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," in *IEEE Journal of Solid-State Circuits*, vol. 28, no. 5, pp. 553-559, May 1993.

[RHE\_99]: W. Rhee, "Design of high-performance CMOS charge pumps in phase-locked loops," 1999 IEEE International Symposium on Circuits and Systems (ISCAS), Orlando, FL, 1999, pp. 545-548 vol.2.

[SHE\_16]: K. J. Shen et al., "19.4 A 0.17-to-3.5mW 0.15-to-5GHz SoC PLL with 15dB built-in supply noise rejection and self-bandwidth control in 14nm CMOS," 2016 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2016, pp. 330-331.

[SUN\_19]: I. Sun, J. Yin, P. Mak and R. P. Martins, "A Comparative Study of 8-Phase Feedforward-Coupling Ring VCOs," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 4, pp. 527-531, April 2019.

[TAM\_20]: M. Tamura et al., "30.5 A 0.5V BLE Transceiver with a 1.9mW RX Achieving -96.4dBm Sensitivity and 4.1dB Adjacent Channel Rejection at 1MHz Offset in 22nm FDSOI," 2020 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 468-470.

[TI\_08]: Ching-Lung Ti, Yao-Hong Liu and Tsung-Hsien Lin, "A 2.4-GHz fractional-N PLL with a PFD/CP linearization and an improved CP circuit," 2008 IEEE International Symposium on Circuits and Systems, Seattle, WA, 2008, pp. 1728-1731.

[TSA\_18]: T. Tsai, R. Sheen, C. Chang and R. B. Staszewski, "A 0.2GHz to 4GHz Hybrid PLL (ADPLL/Charge-Pump-PLL) in 7nm FinFET CMOS Featuring 0.619pS Integrated Jitter and 0.6uS Settling Time at 2.3MW," 2018 IEEE Symposium on VLSI Circuits, Honolulu, HI, 2018, pp. 183-184.

[VAL\_08]: V. Valenta, G. Baudoin and M. Villegas, "Phase Noise Analysis of PLL Based Frequency Synthesizers for Multi-Radio Mobile Terminals," 2008 3rd International Conference on Cognitive Radio Oriented Wireless Networks and Communications (CrownCom 2008), Singapore, 2008, pp. 1-4.

[VEN\_13]: C. Venerus and I. Galton, "Delta-Sigma FDC Based Fractional-N PLLs," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1274-1285, May 2013.

[YIN\_16]: J. Yin, P. Mak, F. Maloberti and R. P. Martins, "A Time-Interleaved Ring-VCO with Reduced  $1/f^3$  Phase Noise Corner, Extended Tuning Range and Inherent Divided Output," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2979-2991, Dec. 2016

[YU\_09]: X. Yu, Y. Sun, W. Rhee and Z. Wang, "An FIR-Embedded Noise Filtering Method for  $\Delta\Sigma$  Fractional-N PLL Clock Generators," in *IEEE Journal of Solid-State Circuits*, vol. 44, no. 9, pp. 2426-2436, Sept. 2009.

[ZHA\_20]: Y. Zhang et al., "A Fractional-N PLL With Space-Time Averaging for Quantization Noise Reduction," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 3, pp. 602-614, March 2020

## **Implémentation de synthèse de fréquence très faible consommation, pour applications IoT, en technologie 28 FD-SOI**

Plus de vingt milliards d'appareils connectés sont prévus dans les années à venir, l'Internet des objets (IoT) est une réalité commune de notre vie quotidienne. Concernant un objet connecté, deux paramètres essentiels doivent être pris en compte : la consommation d'énergie doit être réduite au minimum pour augmenter la durée de vie de la batterie, et le coût de l'objet doit être aussi bas que possible pour assurer un déploiement de masse réussi.

La conception de la synthèse de fréquence est régie par les mêmes défis de l'IoT, les solutions basse consommations sont de plus en plus ciblées. Réalisée dans le cadre du laboratoire commun entre STMicroelectronics et le laboratoire IMS, cette thèse CIFRE propose un nouveau circuit de synthèse de fréquence en technologie FD-SOI. Les spécifications de cette solution alternative sont établies pour atteindre un compromis optimal en termes de consommation d'énergie, de performances RF et de surface de silicium.

**Mots clés :** Synthèse de Fréquence, Boucle à verrouillage de phase, Internet des Objets, FD-SOI technology, Oscillateurs en Anneaux.

---

## **Ultra-Low Power Frequency Synthesizer for Internet-of-Things applications in 28nm FD-SOI technology**

More than twenty billion of connected devices are predicted in the coming years, the Internet-of-Things (IoT) is a common reality of our day-to-day lives. Concerning a connected object, two critical parameters have to be taken into account: the power consumption has to be minimized to increase the battery-operate lifetime, and the cost of the object has to be as low as possible to ensure a successful mass deployment.

The frequency synthesis design is ruled by the same IoT challenges. Although today solutions provide a power consumption around ten mW, Ultra Lower Power (ULP) solutions are more and more targeted. Realized in the frame of the common laboratory between STMicroelectronics and IMS Laboratory, this CIFRE thesis Propose a new frequency synthesis circuit implemented in 28nm FD-SOI technology. The specifications of this alternative solution are drawn to reach optimum compromise in terms of power consumption, RF performances and silicon area.

**Keywords :** Frequency Synthesis, Phase Locked Loops, Internet of Things, FD-SOI technology, Ring oscillators

---

### **Unité de recherche**

[Intitulé, n° de l'unité, et adresse de l'unité de recherche]

Univ. Bordeaux, Bordeaux INP, CNRS, UMR 5218,  
Laboratoire de l'Intégration du Matériau au Système,  
351 Cours de la libération  
33405 Talence, France