Etude de durcissement de la technologie 28 nm FDSOI aux très fortes doses de radiation ionisante

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Thèse de doctorat

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ÉCOLE DOCTORALE
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Mots clés: Dose Totale Ionisante (TID), Microélectronique, Fully-depleted Silicon-On-Insulator (FDSOI), Durcissement, Régénération, Température, Compensation, Tension de grille arrière.

Résumé: Les rayonnements ionisants provoquent des dysfonctionnements dans les systèmes électroniques, de la simple erreur de calcul au dysfonctionnement total de l'appareil. À l'échelle nanométrique, les rayonnements ionisants d'énergie élevée produisent des charges susceptibles d'être piégées dans les oxydes isolants du dispositif. Ces charges piégées produisent des dégradations électriques qui se manifestent dans les dispositifs MOSFET par un décalage négatif de la tension de seuil, un affaiblissement de la pente sous-seuil et une augmentation des courants de fuite. La résilience des systèmes électroniques à ces dégradations est essentielle dans les environnements radiatifs tels que l'espace, les centrales nucléaires ou dans le cas le moins souhaité des accidents nucléaires. Ce travail vise à explorer deux axes de recherche dans le but d'étudier leur impact sur la récupération des caractéristiques électriques de dispositifs 28nm FDSOI ayant été exposés à des rayonnements ionisants. Cette thèse propose une nouvelle méthode de durcissement par régénération-compensation basée sur le dépiégeage des charges par application de cycles de recuit thermique d'une part et d'autre part sur la compensation électrique de la tension de seuil autorisée par la capacité inhérente à la technologie 28nm FDSOI d'appliquer une polarisation back-gate. Cette méthode a pu être validée par la modélisation physique des effets des rayonnements et des mécanismes de récupération, ainsi que par des expériences avec des dispositifs FDSOI. De plus, des simulations réalisées avec des cellules FDSOI basiques typiquement utilisées dans les circuits numériques ont permis de prédire leur dégradation et leur récupération, validant ainsi davantage la méthode de récupération proposée.

Title: Hardening study of 28nm FDSOI technology at very high doses of ionizing radiation

Keywords: Total Ionizing Dose (TID), Microelectronics, Fully-depleted Silicon-On-Insulator (FDSOI), Hardening, Regeneration, Compensation, Back-gate voltage.

Abstract: Ionizing radiation causes malfunction in electronic systems, from miscalculations to a total device failure. At nanometric scale, high-energy radiation produces charges liable to be trapped in the insulating oxides of the device. These trapped charges will produce electrical degradation that manifest in MOSFET devices as a negative threshold voltage shift, a subthreshold slope weakening, and an increase in leakage currents. The resilience of electronic systems to these degradation is essential in radioactive environments such as space, nuclear power plants or in the least desired case, nuclear accidents. This work seeks to explore two research approaches with the aim of studying their impact on the recovery of the electrical characteristics of 28 nm FDSOI devices after their exposure to ionizing radiation. This thesis proposes a new regeneration-compensation hardening method based on the detrapping of charges by applying thermal annealing cycles on the one hand and on the other hand the electrical compensation of the threshold voltage allowed by the inherent possibility of the 28nm FDSOI technology to apply a back-gate bias. This method could be validated through physical modeling of radiation effects and recovery mechanisms, as well as experiments with FDSOI devices. Furthermore, simulations carried out with basic FDSOI cells typically used in digital circuits enabled the prediction of their degradation and recovery, thus further validating the proposed recovery method.

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List of symbols and acronyms

Symbol	Name	Unit
V_{gf}	Front gate Voltage	V
V_{gb}	Back-gate Voltage	V
t_{ox}	Gate oxide thickness	cm
t_{box}	BOX Thickness	cm
t_{si}	Silicon thickness	cm
Ψ	Surface potential	V
Ψ_{sf}	Front surface potential	V
Ψ_{sb}	Back surface potential	V
e_0	Dielectric constant of Vacuum	F/cm^2
e_{si}	Dielectric constant of silicon	F/cm^2
e_{ox}	Dielectric constant of silicon-Oxide	F/cm^2
C_{ox}	Gate oxide capacitance	F/cm^2
C_{box}	BOX capacitance	F/cm^2
C_{si}	Silicon capacitance	F/cm^2
C_{gc}	Gate to Channel capacitance	F/cm^2
E	Electric Field	$MV.cm^{-1}$
E_{sf}	Front electric field	$MV.cm^{-1}$
E_{sb}	Back electric field	$MV.cm^{-1}$
Φ_{msf}	Front metal-semiconductor Work-function difference	eV
Φ_{msb}	Back metal-semiconductor Work-function difference	eV
V_d	Drain voltage	V
V_g	Gate voltage	V
V_s	Source voltage	V

V_{ds}	Drain-to source voltage	V
V_{th}	Threshold Voltage	V
V_{FB}	Flat-band Voltage	V
V_{bg}	Back-gate Voltage	V
V_{mg}	Mid-gap Voltage	V
I_{mg}	Mid-gap Current	A
I_{ds}	Drain-to-source Current	A
I_{on}	ON Current	A
I_{off}	OFF Current	A
n	Body Factor	mV/V
D	Dose	Gy or rad
D'	Dose rate	$Gy.h^{-1}$ or $rad.s^{-1}$
g_0	Electron-hole pairs generation	$cm^{-3}Gy^{-1}$
$f_y(E)$	Charge yield	
N_{ot}	Oxide trapped charges density	cm^{-3}
N_{otf}	Front oxide trapped charges density	cm^{-3}
N_{otb}	BOX oxide trapped charges density	cm^{-3}
D_{it}	Interface trapped charges density	$cm^{-2}eV^{-1}$
D_{itf}	Font interface trapped charges density	$cm^{-2}eV^{-1}$
D_{itb}	Back interface trapped charges density	$cm^{-2}eV^{-1}$
C_{it}	Interface trapped charge capacitance	Fcm^{-2}
C_{itf}	Font interface trapped charges capacitance	Fcm^{-2}
C_{itb}	Back interface trapped charges capacitance	Fcm^{-2}
ΔV_{ot}	Threshold voltage shift due to oxide trapped charges	V
ΔV_{it}	Threshold voltage shift due to interface trapped charges	V
E_{act}	Activation energy	eV
T	Temperature	K
q	Electron charge	C
k	Boltzmann constant	eV/K
t	Time	s
f	Frequency	s^{-1}
f_{osc}	Oscillation Frequency	s^{-1}

A	Frequency factor	s^{-1}
Ar	channel area of the transistor	cm^2
μ_n	Electron mobility	$cm^{-2}V^{-1}s^{-1}$
μ_p	Hole mobility	$cm^{-2}V^{-1}s^{-1}$
m^*	Effective mass of carriers	kg
σ_h	Holes capture cross-section	cm^2
h	Planck's constant	
Φ_{mFG}	Front gate work-function	eV
Φ_{mBG}	Back gate work-function	eV
χ_{si}	Electron affinity of silicon	
E_c	Conduction band level	
E_v	Valence band level	
E_i	Intrinsic Fermi-level	eV
E_F	Fermi-level	eV
E_{Vacuum}	Energy level of vacuum	eV
N	Number of available defect in the oxide volume	cm^{-3}
$n(D)$	number of trapped charges as function of total dose	cm^{-3}
$n(T)$	number of trapped charges to be annealed	cm^{-3}
N_{it}	Interface trapped charges density	cm^{-2}
N_{SiH}	Density of passivated bonds	cm^{-2}
N_{DH}	Density of hydrogen defects	cm^{-2}
σ_{DH}	Capture cross-section of holes reacting with DH centers	cm^2
σ_i	Capture cross-section for interface traps	cm^2
x	Depth	cm
P_{static}	Static Power	W
$P_{dynamic}$	Dynamic Power	W
P_{total}	Total Power	W

MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
TFET	Tunneling Field Effect Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
VLSI	Very-Large-Scale-Integration

BJT	Bipolar Junction Transistor
IC	Integrated Circuit
DSP	Digital Signal Processor
UTBB	Ultra Thin Body and Box
RVT	Regular Threshold Voltage
LVT	Low Threshold Voltage
RBB	Reverse Body Bias
FBB	Forward Body Bias
GO1	Gate Oxide 1
GO2	Gate Oxide 2
TID	Total Ionizing dose
SEE	Single Event Effects
SCE	Short Channel Effects
SEL	Single Event Latchup
SOS	Silicon-On-Sapphire
SOI	Silicon-On-Insulator
PDSOI	Partially-Depleted Silicon-On-Insulator
FDSOI	Fully-Depleted Silicon-On-Insulator
BOX	Buried Oxide
SS	Subtreshold Slope
ELT	Enclosed Layout Transistor
CTRW	Continuous Time Random Walk
STI	Shallow Trench Isolation
RHBD	Radiation Hardening by Design
RHBP	Radiation Hardening by Process
PSP	Surface Potential based models
PDK	Process Design Kit
EOT	Equivalent Oxide Thickness
WF	Work Function
TCAD	Technological Computer-Aided Design
SPICE	Simulation Program with Integrated Circuit Emphasis
TSC	Thermo-Stimulated-Current

W1	Wafer 1
W2	Wafer 2
NBTI	Negative Bias Temperature Instability
RO	Ring Oscillator
PLL	Phase-Locked-Loop
VLIW	Very-Long Instruction Word

Introduction

The nuclear accidents of Three Mile Island in 1979, Chernobyl in 1986 and Fukushima in 2011 have considerably boosted the market for hardened electronic devices during the past 30 years. The need to carry out interventions in harsh environments such as nuclear sites has promoted the research to develop electronic systems able to withstand high levels of ionizing radiation. Numerous studies have shown that *Total Ionizing Dose* (TID) electrically degrades semiconductor devices resulting in early aging up to a total failure of the device. Physically, a high-energy radiation, such as X- and γ-rays, creates charges liable to be trapped in the insulating oxides of a *Metal-Oxide-Semiconductor Field Effect Transistor* (MOSFET). These trapped charges alter the electrical characteristics of the transistor having as a first consequence a negative threshold voltage shift on both n- and p-type metal-oxide semiconductor (NMOS and PMOS) transistors and, an increase in the subthreshold slope producing a decrease in the operating frequency, as well as an increase in the leakage currents that impacts the consumption power of a Very-Large-Scale-Integration (VLSI) circuit.

Since the invention of the transistor in 1947, electronic devices have evolved in complex ways thanks to the advances in manufacturing processes. In 1965, Gordon E. Moore predicted with his postulate that the number of transistors in a microprocessor will double every 24 months. However, nowadays the scaling of devices is reaching its physical limits, therefore new solutions in terms of materials and structures have appeared in recent years, such as high-κ materials used in gate oxides in addition to great advances in photolithography processes. One of these structures is the Silicon-On-Insulator (SOI) technology with its two variants, Partially Depleted-Silicon-On-Insulator (PDSOI) and Fully-Depleted-Silicon-On-Insulator (FDSOI). These variants have been extensively studied for decades, but in recent years, and due to great advances and precision in manufacturing processes, they have become popular thanks to their high performance compared to Bulk-type transistors. In particular, the FDSOI technology has been considered as an ideal candidate to replace conventional Bulk-MOSFETs and continue with the downscaling.

FDSOI technology has multiple advantages over other known technologies such as high frequency performance, low power consumption, no short channel effects (SCE), an intrinsic silicon channel that reduces variability between

devices due to the manufacturing process, and the possibility of modulating its threshold voltage V_{th} by applying a body bias voltage or also called back-gate voltage V_{bg}. In addition, FDSOI transistors have the advantage of being planar, so their manufacturing process is much simpler compared to other emerging technologies such as FinFETs or nanowires. Besides, FDSOI technologies are nowadays increasingly used in space applications thanks to their architecture proved to be intrinsically resistant to single event effects (SEE) and particularly to latchup effects. However, these technologies have shown a significant sensitivity to TID effects due to radiation-induced charge trapping in the buried oxide (BOX).

An electronic system must be hardened to prevent degradation or total failure due to radiation during its mission. Many techniques can be used for that purpose, each of them presenting advantages and disadvantages that have to be taken into account. Historically, shielding was the first hardening method used to make electronic devices resistant to radiation. However, this method can be impractical or inefficient for embedded systems for which weight can be crucial. In applications that include the design of a microcircuit, radiation hardening by design (RHBD) methods have taken a great importance due to their efficiency. Radiation hardening by process (RHBP) is often used for safety demanding applications due to the hardness guaranty it provides. Nevertheless, a significant cost increase due to the important modifications of the manufacturing process is the major drawback of this method.

Hardening strategies to mitigate TID induced-effects in FDSOI devices have been explored in some recent works. They include hardening by design using 3D FDSOI transistor structure, layout techniques, and substrate biasing. This later consist to apply a body biasing that allow tuning the threshold voltage of FDSOI transistors. This technique has been widely used to increase the performance of ICs at the expense of power consumption. Recently, it has been exploited to compensate for the negative shift of threshold voltage produced by radiation effects. On the other hand, thermal annealing has demonstrated to be an effective method to improve the resistance of CMOS devices to TID. This technique consists of applying annealing cycles at high temperature in order to recover the degraded characteristics of electronic components. The higher the applied temperature, the higher the recovery. However, it is well known that high temperature cycles applied to semiconductor devices can accelerate aging and reduce their lifetime.

The technology chosen for this thesis is the 28nm FDSOI from STMicroelectronics, considering that it has shown to be promising for the design of high speed and low power integrated circuits. The goal of the thesis is to propose a new mitigation strategy based on the combined application of thermal annealing and body biasing techniques to guarantee that FDSOI devices can withstand high cumulated dose levels ($\geq$ 10 kGy) in civilian nuclear environments. We have started this work by carrying out a set of experiments on NMOS and PMOS FDSOI transistors of different sizes, including irradiation at different TID levels, annealing cycles and back gate electrostatic compensation. From the observed results, we have developed a hierarchical ensemble of modeling

approaches to describe all stages of the irradiation-regeneration process at the device level, with the goal to deduce predictable and reliable models, simple enough to extend their use at the circuit level.

This manuscript is organized as follows:

Chapter 1 presents the state of the art: the concepts related to total ionizing dose and the effects on classic and advanced MOSFET transistors as well as the main hardening methods are explained. A comparative study between different technologies is shown in order to justify the use of FDSOI transistors in this work.

Chapter 2 analyses the effect of TID on SOI structure and presents the recovery mechanisms applied sor far to this technology. A review of the principal methods, used throughout this thesis, to extract the electrical parameters of FDSOI transistors is also presented.

Chapter 3 presents a SPICE model describing TID induced degradation and thermal regeneration effect on FDSOI transistors characteristics. Results of TCAD simulations, carried out to better understand the physical impact of charge oxide trapping and interface trapping, are analyzed.

Chapter 4 explains the experimental process carried out on 28nm FDSOI transistors. The irradiation, annealing and electrical measurements are explained in detail. A complete analysis of radiation effects, back-gate voltage response and temperature effects is done to observe the influence of these phenomena separately. We extract the values of the electrical parameters affected by TID and those corresponding to annealing parameters in order to calibrate the proposed physical models.

Chapter 5 presents the new mixed strategy based on the regeneration-compensation of the TID effects in FDSOI transistors. This strategy has been applied to a 32-bit DSP designed with the studied 28nm FDSOI technology to show its efficiency. The physical models describing the effect of radiation and thermal annealing are applied to the basic cell of a digital circuit to confirm the effectiveness and predictability of the proposed models. For this purpose, the SPICE model of a CMOS inverter including all these add-ons is used to simulate with the tool ELDO the behavior of a ring oscillator built with 28nm FDSOI transistors.

Chapter 1

Radiation and their effects on electronic components

During the last decade, new materials and structures have emerged in the manufacturing of semiconductors in order to sustain the trend in scaling of transistors and improve integrated circuits (ICs) performance. Among these structures, some have proved to be resistant to harsh environments such as high temperature, space or nuclear plants. Nevertheless, the response of these structures under the most extreme conditions, such as radiation environments, should be known to guarantee their operation during the whole mission.

In this chapter, we first introduce the harmful radiation mostly present in space and nuclear environments. Then, we describe the impact of ionizing radiation on MOSFET characteristics. A focus on radiation-induced effects on silicon on insulator technology is carried out. Finally, different hardening techniques used so far to build hardened reliable circuits are presented.

1.1 Radiation environments

A radiation environment can be defined as a specific complex set of particles, having different energies, that may degrade electronic systems reliability. Radiation can be divided into two categories: ionizing radiation or non-ionizing radiation, depending on its interaction with matter. Unlike non-ionizing radiation, ionizing radiation have enough energy to break molecular bonds and remove electrons from atoms [2, 3, 4]. Ionizing radiation is characterized by their energy and their type of particle. These particles can be grouped in three categories: photons, charged particles and neutrons [5].

- Photons are zero charge and zero mass particles traveling at speed of light with an energy inversely proportional to its wavelength [6]. Highly energetic photons are quantum of electromagnetic radiations with short wavelength that are capable of significantly penetrating materials [7, 8]. There are either X or γ-rays. Generally X-rays are less energetic than γ-rays but both of them have the same type of interaction with matter that we will explain later in this chapter [6].

- Charged particles have an electrical charge that determines their interaction with matter. They include electrons, positrons, that correspond to β-rays, protons or alpha particles, and heavy ions [9]. Charged particles are produced either by the radioactive decay of a nucleus or by using particle accelerators.

- Neutrons are particles with no charge and are part of the nucleus of an atom. Neutrons are produced with nuclear fission and fusion reactions. They are classified according to their energy: thermal neutrons ($E \approx 25\ meV$), intermediate neutrons ($300\ eV < E < 1\ MeV$) and fast neutrons ($E > 1\ MeV$).

These kinds of radiation exist in different environments such as space or nuclear power plants.

In the space environment, electronic systems may be exposed to earth's radiation belts, galactic cosmic-rays or radiation produced by solar wind and flares. The main particles in this environment consist on protons, electrons and heavy ions having an energy range from few hundred keV to some GeV [10].

On other hand, in civil nuclear industry, the levels of radiation can reach the tens of kGy. And in the case of a nuclear accident, these levels can be even higher. In such environments, there are commonly γ-rays and neutrons which can be harmful for both humans and electronic systems.

(a) Nuclear plant in Tihange, Belgium. (b) Nuclear accident in Chernobyl.

Figure 1.1: Nuclear environment.

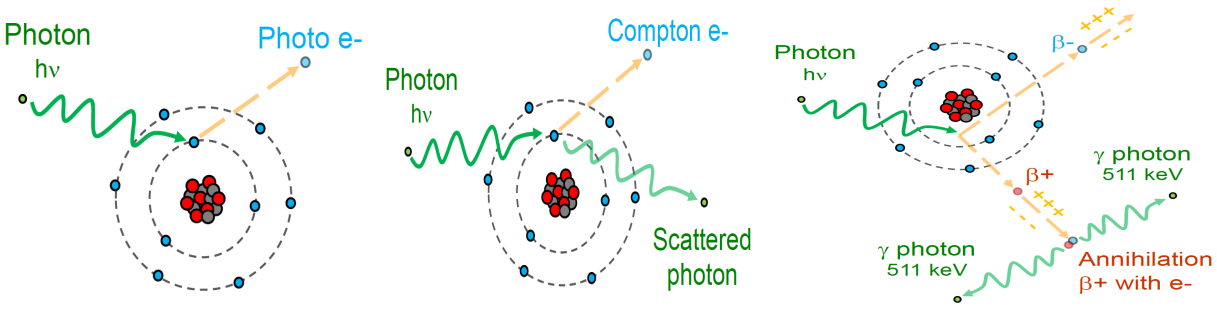
This work investigates the response of new generation semiconductor devices to ionizing radiation, particularly in civil nuclear environment where electronics are mainly exposed to high-energy γ-rays [11].

1.2 Photon-matter interactions

When photons interact with matter, different effects can occur depending on their energy. First, there is the photo-electric effect (Figure 1.2(a)) which occurs when a photon is absorbed by interacting with an electron bound to an atom. If the photon energy is greater than the binding energy of the electron, the later can be ejected from his shell and become free [12]. This effect is predominant for photons with energies between 1 and 100 keV [12].

The second effect is known as the Compton effect or the Compton scattering effect (Figure 1.2(b)). It occurs when a high-energy photon collides with a loosely-binded electron from the outer shell of an atom, giving a part of its kinetic energy to the electron which is released. However, unlike the photoelectric effect, the photon is not absorbed but proceeds on a deviated course with a lower energy [13].

Another effect of photon-matter interaction is the electron-positron pairs generation (Figure 1.2(c)). It occurs when an incident photon with energy greater than 1.022 MeV interacts in the vicinity of an atom nucleus. The energy of the photon is totally absorbed to create an electron-positron pair. The materialized positron annihilates eventually with an electron, generating a pair of 511 keV photons emitted at 180° from each other [12].



(a) Photo-electric. (b) Compton. (c) Electron-positron pairs.

Figure 1.2: Photon-matter interactions.

The total amount of energy deposited by a particle that results in the production of electron-hole pairs in materials is called total ionizing dose (TID) [14]. The unit used to quantify the absorbed dose of radiation is the Gray (Gy), which is defined as the quantity of ionizing radiation necessary to transfer an energy of one Joule to one kg of the exposed material. The quantity of energy deposited in a material during a time interval is called dose rate.

1.3 Total ionizing dose effects on MOS devices

This section aims to explain radiation-induced effects on MOS devices. First, a brief overview of conventional MOS-FET stucture is presented. Then, the physical mechanisms impacting the most senstive parts of this device during its exposure to ionizing radiation are decribed. The impact of these phenomena on the electrical characteristics of

the transistors are shown at the end if this section.

1.3.1 MOSFET structure

Today, the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is the main element in the manufacture of integrated circuits due to its high density of integrability in an integrated circuit. Its structure, displayed in Figure 1.3 is composed of a doped substrate, p- or n-type. For NMOS transistors, the substrate is p-type doped while it is n-type doped for PMOS ones. A metal gate contact induces the inversion layer in the channel at the Oxide-Semiconductor interface. An oxide layer isolates the gate from the substrate and allows its capacitive coupling. Two heavily doped regions (n- or p-type) called drain and source serve as carrier reservoirs. In addition, Complementary-MOS (CMOS) transistors include a pair of shallow-trench Isolation oxides to isolate the NMOS and PMOS structures, facilitating their manufacturing process.

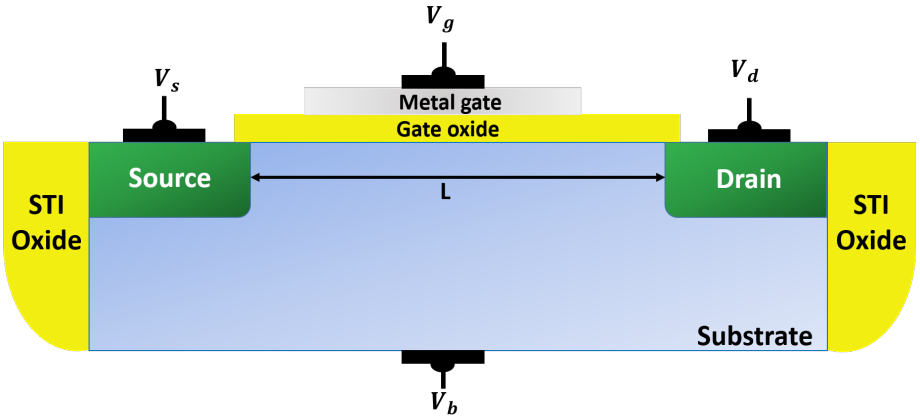


Figure 1.3: Cross-section view of a Bulk-MOSFET.

Depending on the voltage applied to the gate terminal, four operating regimes can be achieved as depicted in Figure 1.4.

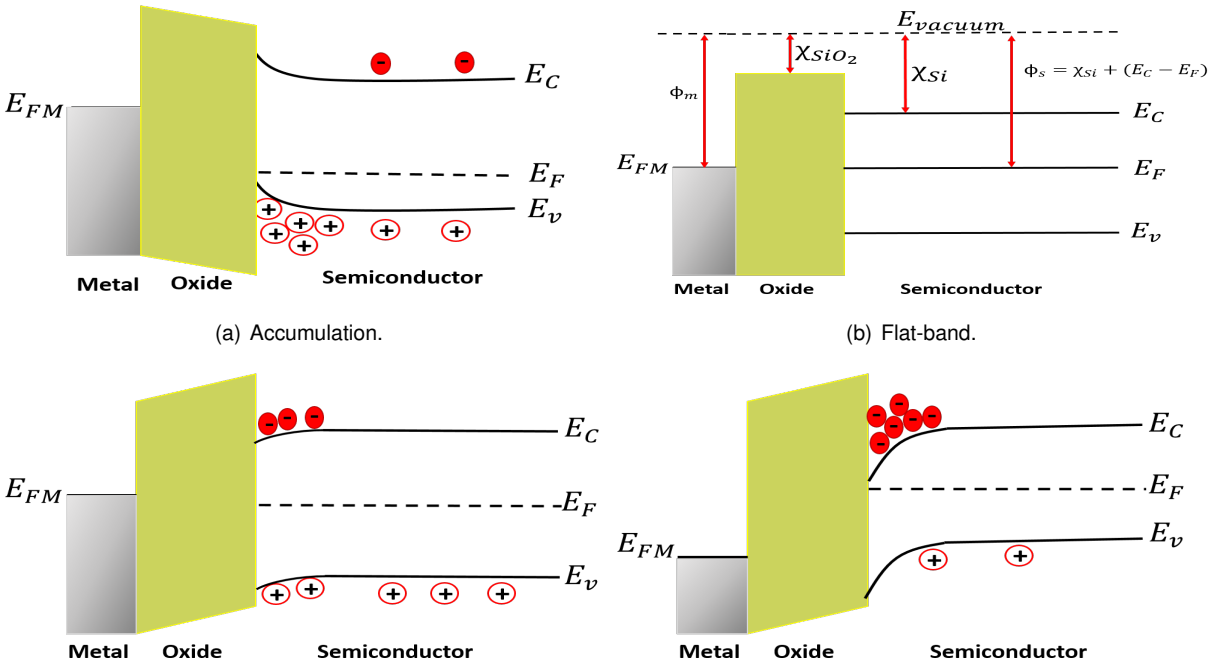
- **Accumulation:** The majority carriers of the substrate are attracted to the $Si - Oxide$ interface, i. e. the channel area. In this case the transistor is blocked because the carrier concentration prevent the passage of electrons from source to drain [15].

- **Flat-band:** This regime occurs when the applied gate voltage V_{gs} cancels the bent of bands of the semiconductor. This voltage is called Flat-band voltage V_{FB}, thus, $V_{gs} = V_{FB}$. This allows a constant concentration of majority and minority carriers in the silicon substrate.

- **Depletion:** In this regime, V_{gs} is not sufficient to attract a large number of holes under the oxide and not positive enough to attract a large number of electrons [16], so, there is neither accumulation of holes in the

valence band nor electrons in the conduction band. The channel area is deserted, hence the term depletion or desertion zone. From this voltage, the inversion channel is considered created, since, due to the increase of V_{gs}, the electron density is greater than the number of holes in the bulk. The MOSFET operated in this region is said to be in weak inversion or the subthreshold regime [16].

- **Inversion:** also called strong inversion regime, the minority carriers are accumulated at the $Si - Oxide$ interface, therefore a carrier path is created connecting the drain and source regions. The current flowing in the channel can be modulated by applying a voltage between the drain and the source.



(a) Accumulation.

(b) Flat-band.

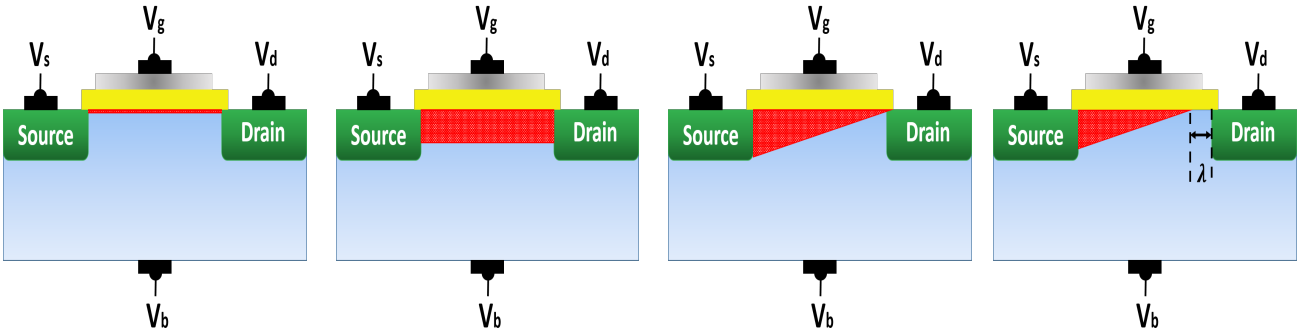
(c) Depletion.

(d) Inversion.

Figure 1.4: Operation modes of a MOS structure.

1.3.2 I-V characteristics of conventional MOSFETs

The electrical operation of the MOSFET depends directly on the induction of a carrier inversion channel at the Oxide-Semiconductor interface. This inversion channel is controlled by the voltage applied to the gate, while the intensity of the current I_{ds} flowing across the channel, drain and source is controlled by the voltage applied to drain V_{ds}. Hence, when the voltage V_{ds} increases, the MOSFET transistor can have four operating modes displayed in Figure 1.5 and 1.6. We define the threshold voltage V_{th} as the minimum gate voltage value able to establish the conduction channel in a transistor [17]:



(a) Non-conduction. (b) Linear. (c) Non-linear. (d) Saturation.

Figure 1.5: I-V Operation modes of a conventional long-channel MOS transistor.

- **Non-conduction regime or blocked mode:** The non-conduction regime implies a gate voltage $V_{gs} < V_{th}$. The applied gate voltage is not sufficient for the channel formation, as a result, the drain-source current is practically zero $I_{ds} \approx 0$. However, there is a small current that flows before reaching the threshold voltage called subthreshold current which is expressed as [18]:

$$I_{ds} \propto exp(\frac{qV_{gs}}{nKT}) \tag{1.1}$$

With n the idealty factor.

- **Linear or ohmic regime:** A gate voltage V_{gs} produces an electric field that can attract the minority carriers of the substrate to the $Si - SiO_2$ interface. As a result, a small inversion layer near the insulating oxide becomes less p-type and, their conductivity is reduced [19]. As V_{gs} increases, the area near the oxide will attract more electrons than holes and will behave like an n-type channel. For values slightly superior to threshold $V_{gs} > V_{th}$ and $V_{ds} << V_{dsat}$ the channel region has the characteristics of a resistor, then the drain current increase linearly [16].

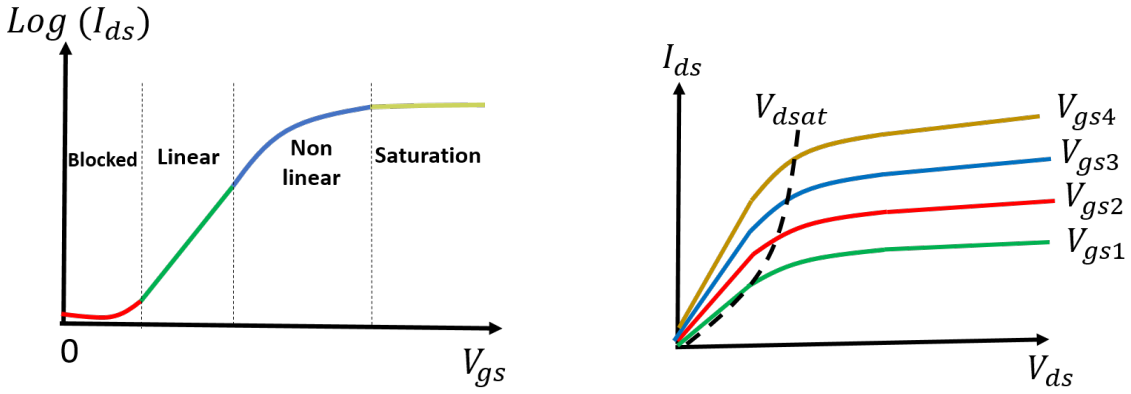
$$I_{ds} = \frac{W}{L}\mu_n C_{ox}(V_{gs} - V_{th})V_{ds} \tag{1.2}$$

- **Non-linear ohmic regime:** This regime occurs when the potential induced by the voltage applied to V_{ds} is large enough to modify the vertical electric field, causing a loss of uniformity of the density of electrons in the channel[19]. A "pich-down" or pinch occurs at the end of the channel on the drain side, therefore, the characteristic $I_d(V_{ds})$ will be non-linear as given in equation 1.3:

$$I_{ds} = \frac{\mu_n C_{ox} W}{L}((V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}) \tag{1.3}$$

- **Saturation regime:** When $V_{gs} > V_{th}$ and $V_{ds} \geq V_{dsat}$, the channel ceases to exist near the drain, i.e. the channel is "pinched-off" [17, 20]. In this case, the drain current remains constant even if V_{ds} continue to increase, the characteristic equation of this mode is given by:

$$I_{ds} = \frac{\mu_n C_{ox} W}{2L}(V_{gs} - V_{th})^2 \tag{1.4}$$



(a) Drain current as a function of V_{gs}.

(b) Drain current as a function of V_{ds}.

Figure 1.6: Electrical response of a conventional MOSFET.

1.3.3 Physical mechanisms of the TID in MOSFET devices

The physical mechanisms that take place in the creation of ionization defects in SiO_2 are illustrated in Figure 1.7. First, radiation deposit energy through generation of electron-hole pairs. A fraction of these pairs recombine and the remaining free carriers are transported in the oxide. Then, near the interface, either holes trap in defect sites or interface traps are created via H^+ reactions. These mechanisms will be described in details in the following sections.

Hole trapping

Oxide layers are the most sensitive parts of MOS devices affected by ionizing radiation. Actually, oxide traps are defects already existent in insulators that are related to oxygen vacancies in $Si - O$ bonds [1, 21]. The oxide trapped charge is typically net positive due to the capture of a hole in neutral oxygen vacancies and subsequent formation of E' centers. E' centers in amorphous SiO_2 are defects due to Si dangling bonds that occur during removal of an oxygen atom. The principal types of E' centers are: E'_δ and E'_γ (see Figure 1.8).

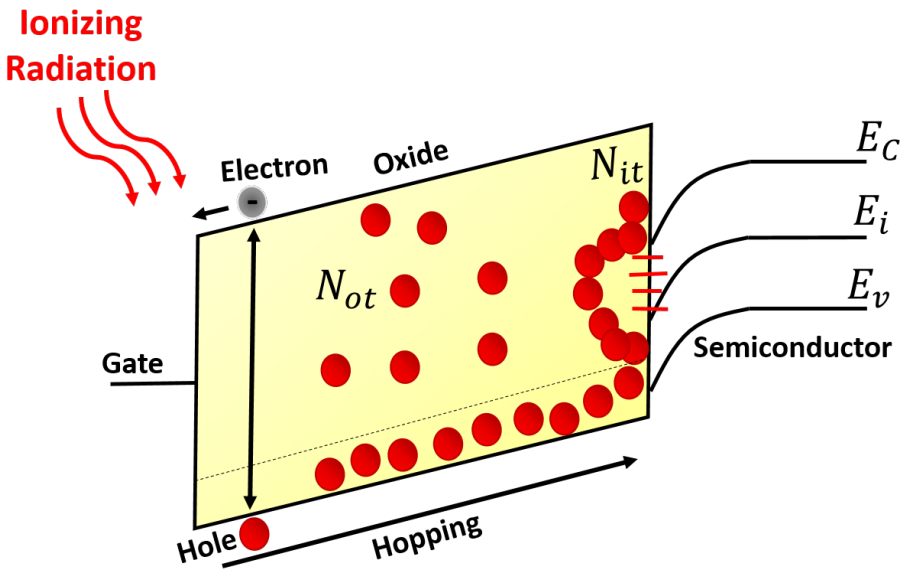
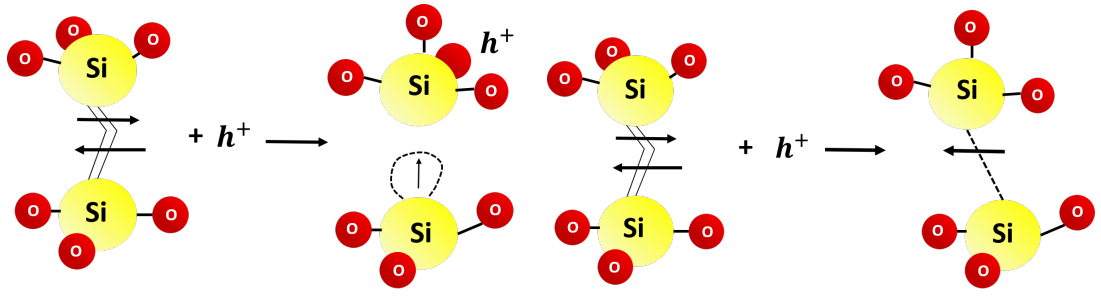


Figure 1.7: Model of radiation effects in oxides.

The E'_δ centers have an energy level between 0.5 eV and 1.0 eV above the valence band, so they are involved in the transport of holes in the oxide volume. It is considered that the E'_δ are shallow levels while the E'_γ are deeper levels[1].

Another characteristic of the E'_δ centers is their ability to exchange charges with a near semiconductor region. Indeed, both the E'_δ and the significantly deeper level hole trap center, E'_γ, can exchange charge with a semiconductor. When E' centers are located within 2.5 nm from the $SiO_2 - Si$ interface, they are called border traps [22].



(a) Schematic view of a E'_δ center.

(b) Schematic view of a E'_γ center.

Figure 1.8: Schematic view of E' centers [1].

In silicon oxides, the density value of oxygen vacancies is $10^{17}\ cm^{-3}$ and $10^{20}\ cm^{-3}$, for buried oxides and for conventional "silica glass" oxides, respectively [23].

For decades, silicon dioxide has been the insulating material used for MOSFET gate oxides, but with the continuous

scaling, its thickness has reached a physical limit. Indeed, a layer of SiO_2 thinner than 1.2 nm can be permeable to gate-to-channel tunneling that can lead to a detrimental increase in leakage current. To solve this problem, high-κ oxides have been implemented in new generations of transistors. Hafnium-based dielectrics, such as HfO_2, $HfSiON$ or ZrO_2, have shown good compatibility with silicon technology as gate oxides [24, 25]. The concept of equivalent oxide thickness (EOT) has been introduced in order to describe the high-κ dielectric with respect to SiO_2. EOT is the equivalent thickness of SiO_2 oxide giving the same capacitance for any dielectric of physical thickness t_{ox} and dielectric constant ϵ_{ox}. Then, the EOT is expressed as:

$$EOT = t_{ox} \frac{\epsilon_{SiO_2}}{\epsilon_{ox}} \tag{1.5}$$

The effects of radiation on SiO_2 gate oxides have been studied extensively [26, 27] as opposed to $High - \kappa$ dielectrics which are still a subject of study [25, 28, 29, 30].

When the device is exposed to high energy ionizing radiation (X or γ), electron-hole pairs are created. The released electrons remain in the oxide for a short period of time (few ps) due to their high mobility (20 $cm^2V^{-1}s^{-1}$) and move towards the gate. On the other hand, a fraction of the created holes recombine immediately (prompt recombination), and the remaining fraction move slowly, due to its very low mobility in oxides (in the range of 10^{-4} to 10^{-11} $cm^2V^{-1}s^{-1}$), by discrete stochastic jumps (hopping) towards the $Si - SiO_2$ interface [31, 32]. In consequence, the net charge induced by the radiation in the oxide is positive.

Interface traps creation

The build-up of interface traps is a more complex process than that of oxide charge trapping. The presence of interface traps is inherent in the manufacturing process of the device due to the incompatibility in lattice parameters between the insulating oxide (SiO_2) and the semiconductor (Si) [33, 34].

The radiation-induced interface traps, N_{it} in cm^{-2} or D_{it} in $cm^{-2}eV^{-1}$, are dominated by a family of $Si - SiO_2$ interface silicon dangling bond defects called P_b centers [33, 34]. The most important and abundant of these centers is called the Pb_0 center. A secondary contribution is provided by a closely related defect called Pb_1. Both Pb centers are silicon dangling bond defects in which the central silicon is back bonded to three other silicon atoms [34, 35].

It is well known that the formation of interface traps initiates after irradiation, either immediately (prompt generation), or slowly (delayed generation) depending on the temperature and the applied electric field [36, 37]. Several hypotheses have been formulated to explain this phenomenon, all of which coincide on the fact that the main elements responsible for the formation of interface traps are hydrogen impurities.

Lai [38, 39] has proposed a two-step model in which he describes that the holes generated in the oxide are capable of breaking the $Si-O-Si$ bonds at the interface. The second step corresponds to the formation of interface traps due to the capture of electrons.

McLean [40] proposed in his work published in 1976 a two-step model to describe the origin of interface traps. The first step corresponds to the transport of holes through the oxide towards the $Si-SiO_2$ interface. It is shown that the hole transport can be well described by a model of holes moving via polaron hopping between localized sites. The second step of the model corresponds to the radiation-induced buildup of interface traps.

This model helps to explain the difference between the rate of accumulation and creation of discrete levels at the interface. However, this model is not able to predict the quantity of interface traps generated according to the applied electric field.

The Hole-Trapping / Hydrogen-Transport (HT^2) [39, 41] model is a variation of the McLean model and explains that the discrete levels are generated by the interaction of hydrogen ions with the holes trapped at the interface. The interaction is proportional to the cross section of the trapped holes and proportional to $E^{-1/2}$. However, this model does not explain if the ions are generated throughout the oxide or only in the region close to the interface nor if there is a relationship with the manufacturing process.

The best experimental description is given by the *continuous time random walk* (CTRW) model [32, 40], in which the transport mechanism is based on discrete jumps of the holes with a random distribution of traps. The term ”Polaron” refers to the situation where the carrier interacts with the medium and creates a lattice distortion in the neighborhood. It is important to note that all the assumptions have been made on the interaction of radiation with hydrogen. However, this model fails to correctly explain the phenomenon of trap formation at the interface.

The interface trap build up is a time-dependent phenomenon. When MOS devices are exposed to ionizing radiation, interface trapped charges multiply, which is an immediate effect of the interaction between the interface and ionizing radiation commonly called ”early” component [42, 43]. The second component, called the ”delayed component”, occurs seconds to thousands of seconds after irradiation and consists of a severe increase in the number of charges trapped at the interface [44, 45]. It is presumed that this phenomenon is due to the slowness of transport of the charges trapped in the oxide towards the interface [4].

Interface traps can be classified into two categories, as shown in Figure 1.9:

- Donor: exhibits neutral behavior when it is filled with an electron and positive when it is empty.
- Acceptor: is negatively charged when filled with an electron and neutral when empty.

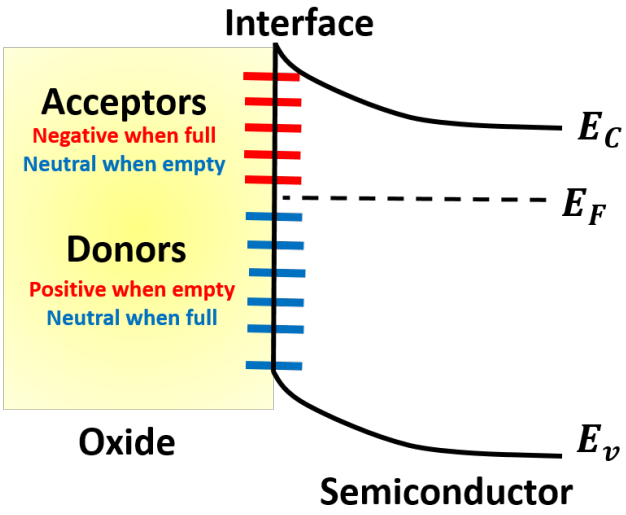


Figure 1.9: Representation of interface states.

Generally, the interface states ($eV^{-1}cm^{-2}$) are mainly donor-like in the lower half, and acceptors-like in the upper half of the silicon bandgap [4] and their density D_{it} vary between $10^9\ eV^{-1}cm^{-2} \leq Dit \leq 10^{12}\ eV^{-1}cm^{-2}$.

1.3.4 Impact on electrical characteristics

Threshold voltage shift

The main parameter affected by the radiation-induced trapped charges is the threshold voltage of the transistor. As a matter of fact, the oxide trapped charges increase the effective electric field and contribute to make easier or more difficult the inversion of the n-type or p-type channels, respectively, which consequently leads to a negative threshold voltage shift (ΔV_{th}). The interface trapped charges interact with the carriers of the channel close to the interface, which modifies the surface potential of the MOS structure according to the gate voltage, producing a variation in the subthreshold slope SS [27, 46]. These failure mechanisms are present in both NMOS and PMOS transistors. In NMOS devices, the negative ΔV_{th} makes the transistor able to turn-on with a lower gate voltage until the loss of control of the channel, i.e. when the transistor becomes conductive though no gate voltage is applied. For a PMOS transistor, the excess of oxide trapped charges also leads to a negative ΔV_{th}. In this case, it becomes more difficult to switch-on the transistor [2, 4].

The contribution to ΔV_{th} due to the oxide trapped charges is [4]:

$$\Delta V_{ot} = -\frac{1}{C_{ox}} \int_0^{t_{ox}} \Delta\rho(x) \frac{x}{t_{ox}} dx = -\frac{\Delta Q_{ot}}{C_{ox}} \tag{1.6}$$

While the contribution of the interface trapped charges to ΔV_{th} is:

$$\Delta V_{it} = -\frac{\Delta Q_{it}}{C_{ox}} \tag{1.7}$$

And then, the total ΔV_{th} is expressed as the shift caused by the oxide trapped charges and the interface trapped charges.

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} = -\frac{1}{C_{ox}}(\Delta Q_{ot} + \Delta Q_{it}) \tag{1.8}$$

Some authors prefer to express the shift of the threshold voltage as a function of the density of traps N_{ot} and N_{it}. Using the following relation, we express the densities of traps in the oxide and at the interface:

$$\Delta N_{ot} = \frac{1}{q} C_{ox} \Delta V_{ot} \tag{1.9}$$

And,

$$\Delta N_{it} = \frac{1}{q} C_{ox} \Delta V_{it} \tag{1.10}$$

Finally, the threshold voltage shift is expressed as:

$$\Delta V_{th} = V_{th0} - \frac{q}{C_{ox}}(N_{ot} - N_{it}) \tag{1.11}$$

Note that at after a certain time of irradiation, the interface trapped charges become dominant compared to the oxide trapped charges. Particularly, in an NMOS transistor, interface traps capture electrons and become negatively charged. In NMOS devices, these trapped charges compensate for the effect of the oxide charges. This phenomenon is called *rebound effect* [4, 35]. Figure 1.10 shows threshold voltage shift degradation due to oxide and interface trapping for NMOS and PMOS transistors. As we can see, the responses to TID of NMOS and PMOS devices are different: in NMOS transistors, the contributions of oxide and interface trapped charges are self-compensated while in PMOS, both contributions are additive causing a more severe degradation of V_{th}.

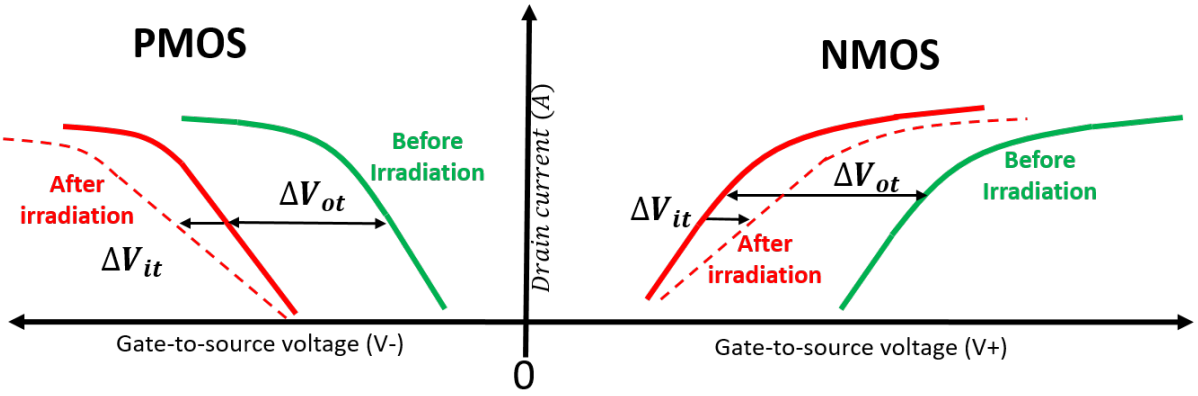


Figure 1.10: Effect of oxide and interface trapped charges on the threshold voltage of NMOS and PMOS transistors.

Leakage currents increase

The leakage current I_{off} in a MOSFET is defined as the drain current when $V_{gs} = 0$ as shown on Figure 1.11. This current is a consequence of radiation-induced charge trapping in the gate oxide and in thick lateral shallow trench isolation (STI) oxides. As a matter of fact, a MOS transistor can be viewed as a main transistor and several lateral parasitic ones. With deep subnanometric technologies, the gate oxide thickness of the main transistor has been drastically reduced and hence few charges are trapped in its volume. On the other hand, positive charges trapped in the thick lateral isolation oxides can invert the P-type region in the well/substrate of NMOSFETs creating a leakage path between source and drain or between source and well. These leakage currents lead to an increase in the static power consumption and can cause short circuits or latch-ups [47].

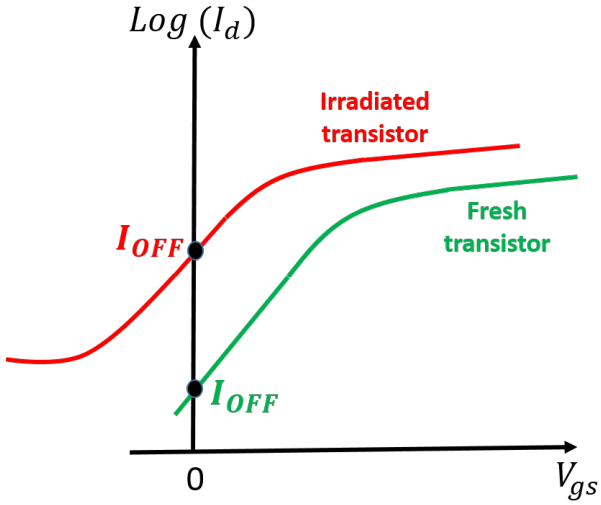


Figure 1.11: Leakage current in a NMOS transistor.

Other effects

After irradiation, it is common that MOSFETs exhibit a series of anomalies related to trapped charges [48, 49, 50]:

- Reduced mobility: the carriers mobility is degraded because of the excess of interface traps which hamper the trajectories of the moving carriers. The reduction in carrier mobility has a direct effect on the transconductance of the transistor. The carrier mobility, taking into account the effects of trapped charges, is modeled by the equation [51, 52]:

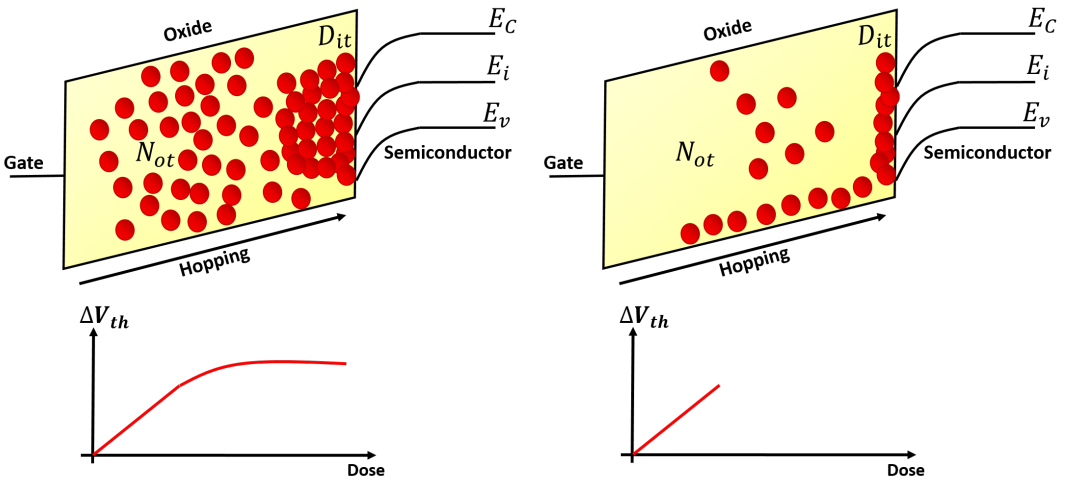
$$\mu = \frac{\mu_0}{1 + \alpha_{it}\Delta N_{it} + \alpha_{ot}\Delta N_{ot}} \tag{1.12}$$

- Reduced transconductance g_m: the gain (transconductance) of the MOS transistor is reduced due to the degradation of the mobility of carriers in the channel that interact with charges trapped in the oxide and at the interface.

- Noise increase: mainly 1/f noise. This noise is caused by the interaction between the excess of carriers trapped in the oxide and at the interface, and the carriers in the channel. This phenomenon is purely random, and is responsible for the variation in the quantity and mobility of carriers, which results in a fluctuation in the drain current [53].

1.3.5 Dose-Rate effects

It has been shown in multiple studies that radiation-induced degradation in MOSFETs is dose-rate sensitive and the distribution of charges trapped in the oxides is also dependent on the dose-rate [54, 55]. This is because N_{ot} and D_{it} have different time-constants related to the charge transport in insulating oxides. Due to that difference, N_{ot} tends to be predominant with high dose-rates where the creation of electron-hole pairs rate is very high, causing significant degradation in V_{th}. Some studies have reported that when irradiating a transistor at a high dose-rate, a saturation of charges occurs in the oxide, that is, all the available traps will be occupied. Consequently, the degradation of the threshold voltage reaches its limit [56]. However, the degradation of the subthreshold-slope continues due to the trapped charges at the $Si - SiO_2$ interface. On the other hand, D_{it} tends to be predominant at low dose-rates, degrading the speed of the device. In the work of Brown [57], it is shown that the threshold voltage dose dependence varies linearly for low levels of radiation and presents a saturation at high levels (see Figure 1.12).



(a) High dose-rate effect.

(b) Low dose-rate effect.

Figure 1.12: Effect of dose rate in oxides.

1.4 Radiation-induced effects on silicon on insulator technology

The rule of technology downscaling predicted by Moore's law has reached its limit. As a matter of fact, the reduction of the channel length and the dimensions of insulating oxides to subnanometric domain has generated new problems such as short channel effect (SCE) and increased leakage currents. So, with the aim to continue increasing the performance of electronic systems, new devices, materials and structures have emerged. In particular, silicon on insulator (SOI) and silicon on sapphire (SOS) technologies were proposed to bring new solutions to such problems. The SOS technology is not widely used anymore because it includes a sapphire layer that makes the manufacturing process more expensive [58, 59, 60].

The structure of SOI transistor resembles to that of conventional Bulk one. The most significant difference is the inclusion of a buried oxide layer (BOX) that isolates the body and the channel of the transistor[58]. The inclusion of the BOX decreases the parasitic junction capacitance, which enhances the speed of the transistor. In addition, the BOX layer eliminates the parasite NPN structure present in bulk devices [60, 61]. In this section, a brief overview of SOI transistors structures is presented. Then, the effects of radiation on this technology are introduced.

1.4.1 The SOI technology

In the SOI technology, the thickness of the silicon layer and the maximum depletion width x_{dmax} determine the physics of the device [62]. Actually, two SOI transistor structures exist: partially-depleted silicon on insulator (PDSOI) and fully-depleted silicon on insulator (FDSOI).

A partially-depleted SOI transistor has the silicon film thickness t_{si} larger than the maximum depletion width x_{dmax}, expressed as [58, 63] :

$$x_{dmax} = \sqrt{\frac{4\epsilon_{si}\Phi_F}{qNa}} \tag{1.13}$$

PDSOI transistors have a doped channel on the top of a significantly thick BOX as shown in Figure 1.13. The first integrated circuits that included PDSOI transistors had shown a huge improvement of their operating frequencies. They have been widely used for the development of high-speed microprocessors [64, 65]. However, the inclusion of a floating volume of doped silicon under the gate gives origin to some effects proper to SOI structure called floating body effects [58, 66, 67]. One of these effects is the "kink effect" which is a consequence of an accumulation of charges in the depleted zone of the channel. These charges cause a slight increase in the drain current emulating a "kink" [68] in the $I_d(V_{ds})$ characteristic of the transistor.

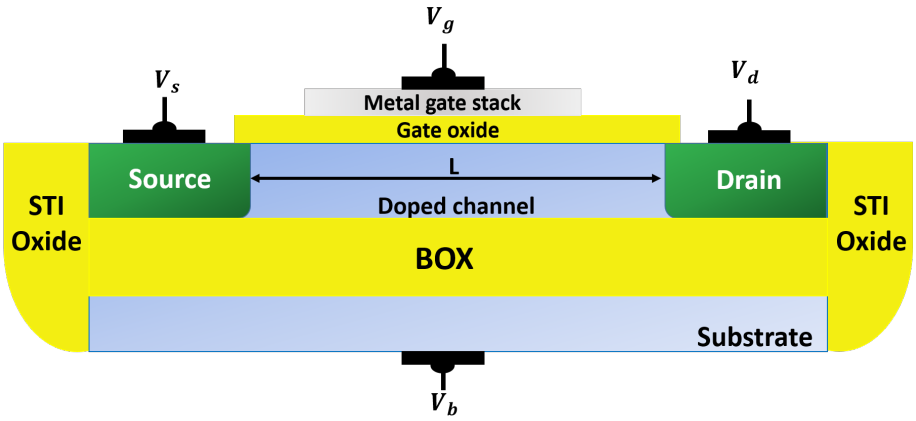


Figure 1.13: Cross section view of a PDSOI transistor.

On the other hand, FDSOI technology has emerged just after PDSOI one. FDSOI (Figure 1.14), also called ultra thin body and BOX (UTBB) SOI, is the candidate for further scaling and increasing the performance of next-generation integrated circuits. This planar structure has an extremely thin intrinsic silicon layer, which allows the depletion zone to cover the entire channel, i.e. t_{si} is lower than x_{dmax} [69]. This characteristic reduces threshold voltage fluctuation and eliminates the floating body which decreases therefore the kink effect present in PDSOIs. This technolgy presents many advantages over conventional bulk one that can be summarized as follows :

- A gate metal stack (TiN), avoiding the problem of depletion mainly found in polysilicon gates, which produces a variation in the gate oxide capacitance [70, 71].
- An intrinsic silicon layer that reduces the variability in the manufacturing process and eliminates completely the kink effect present in PDSOI transistors [72, 73].

- A subthreshold-slope close to the ideal, allowing greater switching speed.
- A High-κ dielectric gate oxide that avoids the direct tunneling of carriers from the channel through the gate oxide (gate-to-channel tunneling leakage).
- A better immunity to Short channel effects (SCE).
- The electrostatic coupling between front and back interfaces that allows a threshold voltage control [74, 75, 76].

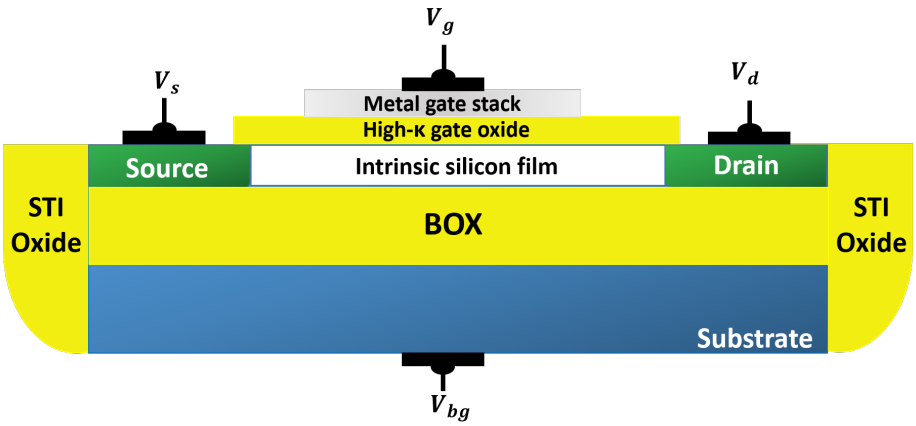


Figure 1.14: cross section view of a FDSOI transistor.

In spite of their advantages, PDSOI and FDSOI present a self-heating problem that occurs due to the BOX inclusion in the body of the transistor. This layer avoids the evacuation of heat through the substrate due to its low thermal conductivity [77, 78, 79]. Recent studies have shown that high temperatures can be reached in the region underneath the channel causing reliability issues such as noise increase, lower mobility and electromigration [77, 80, 81, 82].

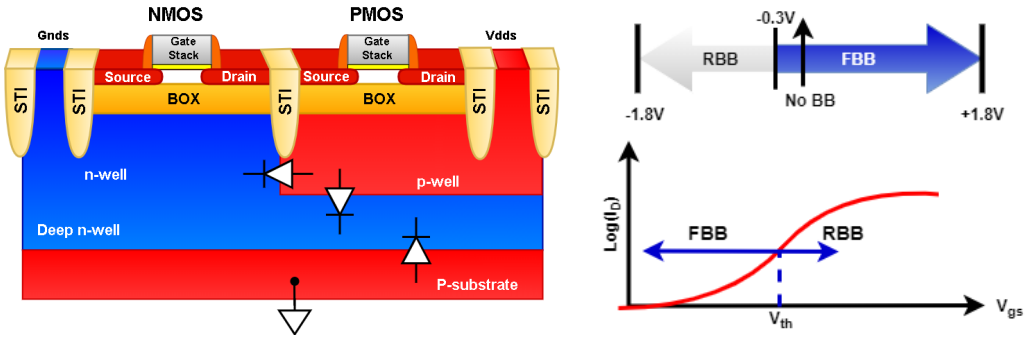
An interesting feature of FDSOI technology and that will be used in this thesis, is the body-biasing. It allows electrostatic coupling between the front and back interfaces, i.e. front and back transistors. The front transistor is composed of the gate metal stack, the front oxide and the intrinsic silicon channel while the back transistor is composed of a metal contact, the substrate, the BOX and the same intrinsic channel. This thesis focuses on 28nm FDSOI devices. In this technology, multiple threshold voltage variants of the transistors are available including low V_{th} (LVT) and regular V_{th} (RVT) devices.

- **Low Vth (LVT)**

  LVT technology, schematized on Figure 1.15 is designed on a "Flip-well" structure. So, the NMOS transistor is built on an N-type substrate and the PMOS transistor on a P-type substrate. LVT devices enhance forward

body biasing allowing the improvement of the switching speed at the expense of more leakage current consumption. This variant allows a lower nominal threshold voltage (around 0.2 V) and is generally used for high speed applications[83].

As can be observed in Figure 1.15, biasing the back-gate of FDSOI PMOS transistors positive and NMOS negative corresponds to the worst case, the reverse body bias (RBB). With this configuration, the intra-substrate “pWell-nWell” diode can turn-on with a difference of potential accross the junction, which is likely to increase the leakage currents. In this case, only a small RBB voltage is tolerated before turning-on the diode, typically limited to half of the diode direct voltage (up to -0.3 V) [74]. Biasing PMOS negative and NMOS positive corresponds to the most favorable case, the forward body bias (FBB). In this case, the ”PWell-NWell” intra-substrate junction remains reverse-biased and the range of biasing applied to the terminals is only limited by the breakdown voltage of the junction.



(a) LVT 28nm FDSOI.

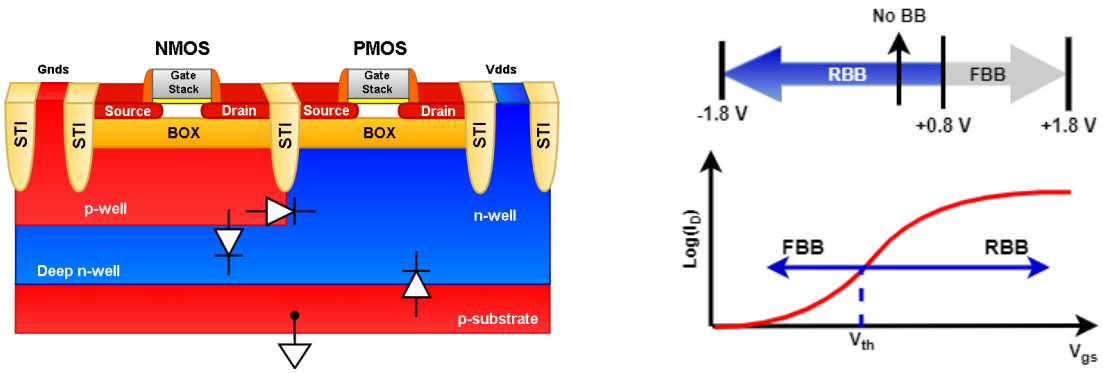
(b) Body biasing range of LVT transistors.

Figure 1.15: Cross-sectional view of an FDSOI LVT device with the back-gate voltage range.

- **Regular Vth (RVT)**

RVT NMOS and PMOS transistors are shown in Figure 1.16. They are built on a standard substrate, i.e. the NMOS transistor on a P-type substrate and the PMOS on a N-type substrate. These devices are mostly focused on RBB, enabling a reduction of the leakage current [74]. This configuration also reduces the variability of the threshold voltage V_{th} in both directions.

We also observe that the RBB voltage can be increased without any risk of leakage, while when applying a FBB, only a limited bias can be used before direct conduction of the intra-substrate junction. In the FBB configuration, the limiting value is equal to half of the sum of the supply voltage (V_{dd} = 0.9 V) and the breakdown voltage of the intra-substrate diode ($V_{diode} = 0.7\ V$): $(V_{dd} + V_{diode})/2 = 0.8\ V$ [74].



(a) RVT 28nm FDSOI.

(b) Body biasing range of RVT transistors.

Figure 1.16: Cross-sectional view of an FDSOI RVT device with the back-gate voltage range.

1.4.2 Effects of radiation on SOI transistors

When PDSOI transistors are exposed to ionizing radiation, electron-hole pairs are created in the silicon layer. The bipolar transistor formed by the source-body-drain can be easily triggered after ionization [84]. The un-recombined carriers remain in the body region and drift towards the source, rising the body potential which switch-on the parasitic bipolar transistor inherent to the SOI transistor [85, 86]. So, this makes the PDSOI technology particularly sensitive to single event latchup (SEL). In addition, the BOX layer in this technology is very thick, making it prone to trapped charges. Consequently, PDSOI devices are less resistant to TID effects than their Bulk counterpart [87].

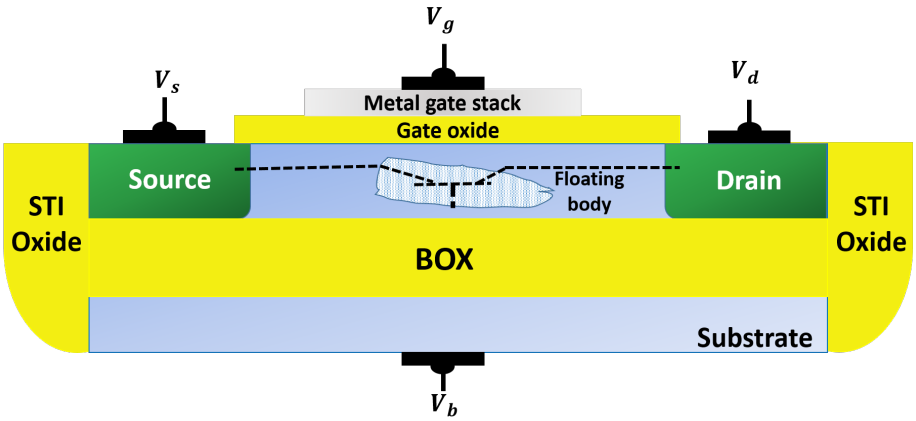


Figure 1.17: Parasitic bipolar structure in PDSOI devices.

On the other hand, FDSOI transistors have proved to be more resistant to TID effects than PDSOI ones. Numerous studies have been carried out in order to determine the resistance of FDSOI devices to radiation and the effects it produces in terms of degradation of their electrical characteristics [88, 89, 90, 91, 92, 93]. In the studies carried out by M. Gaillardin [91] [92], FDSOI transistors were irradiated at very high doses (of the order of MGy) and then tested to observe their electrical degradation. The expected electrical degradations were observed: negative ΔV_{th},

subthreshold-slope degradation and increased leakage currents I_{off}.

Radiation-induced effects on FDSOI transistors are principally due to charge trapping in the BOX. In fact, positive charge trapping in the BOX can trigger the induction of a parasitic channel on the $Si - BOX$ interface. The response to radiation of this technology differs from others due to the capacitive coupling effect between both interfaces [94], so the surface potential of the front-gate depends directly on that of back-gate. Consequently, the charges trapped in the BOX are also electrically coupled to the front surface potential [95, 96].

Multiple studies have investigated the best and worst biasing configurations for FDSOI transistors. In particular, the four bias conditions, depicted in Table 1.1 have been studied [56, 97, 98, 99]. Authors have shown that the worst biasing case is the transmission gate (TG) configuration. This can be explained by the fact that the electric field tends to separate the electron-hole pairs when they are created, preventing their prompt recombination and then increasing the charge yield [100].

Table 1.1: Different bias configurations of FDSOI transistors.

State	V_d	V_g	V_s	V_b
ON	0	V_{dd}	0	0
OFF	V_{dd}	0	0	0
TG	V_{dd}	0	V_{dd}	0
Grounded	0	0	0	0

Other studies focused on improving the radiation hardness of FDSOI transistors by thinning the BOX [97, 101, 102]. The TID tolerance was improved with a thinner BOX but not as much as expected. The BOX was thinned from 145 nm down to 11 nm while the maximum ΔV_{th} was only reduced by less than a factor of two [100, 103]. This could be explained by the fact that the coupling coefficient is enhanced with a thinner BOX and then the front transistor becomes more sensitive to the BOX trapped charges.

1.5 Radiation Hardening Techniques

Radiation hardening techniques aim to make electronic devices more resistant to ionizing radiation. These devices can therefore be used in radioactive environment such as space or nuclear power plants. Hardening techniques are chosen depending on the dose level and type of particles in order to have electronic circuits that still meet the design constraints during the whole period of the mission. Among the most known hardening techniques, we can cite:

- **Shielding**

Shielding was historically the first hardening method used in order to prevent the effects of radiation on electronic systems. This technique adds a layer of material capable of attenuating the penetration of radiation in sensitive parts. The type and size of material able to protect the electronic system depend on the nature of radiation[104]. For instance, alpha particles can be stopped just with a piece paper or some μm of copper [105] while for gamma radiation, we need at least one meter of concrete [106]. The main drawback of this technique is the weight of the shielding material which can limit its use for embedded systems.

- **Hardening methods by design**

Radiation hardening by design (RHBD) techniques are considered as a solution to implement hardened electronic systems in embedded applications such as robots or satellites. Figure 1.18 shows an example of a CMOS inverter designed using an enclosed layout transistor (ELT) technique for the NMOSFET in order to suppress leakage currents caused by charge trapping in STI oxides [107, 108]. As can be seen, $P+$ and $N+$ guard rings are generally used together with ELT to stop possible conductive paths, hence preventing inter-device leakage currents. These techniques have shown to be very effective in improving the total ionizing dose tolerance of CMOS integrated circuits. However, the main drawback of these RHBD techniques is the need of a larger silicon area on silicon wafer compared to a standard design.

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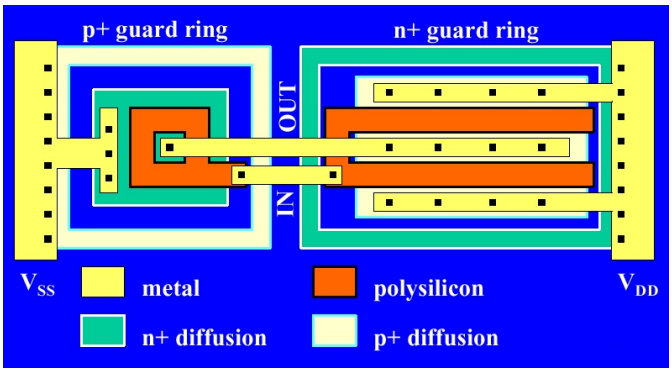


Figure 1.18: CMOS inverter designed with RHBD techniques.

- **Hardening methods by manufacturing process**

This technique of hardening implies a modification in the manufacturing process of integrated circuits. Some works have proposed the insertion of doping implants, called body-tie, with the aim of evacuating the charges trapped in the oxides of MOSFETs. In the particular case of SOI transistors, it has been possible to improve the radiation tolerance by implanting dopant ions in the BOX that create electron traps acting as recombination centers for trapped charges [109, 110].

To reduce the parasitic bipolar transistor effect in SOI transistors, the most common technique involves the use of body ties which connect the floating body region to a fixed potential [72, 85]. The excess holes created by an ion strike no longer accumulate in the floating body region because they are evacuated through the body contact [111]. This reduces considerably the parasitic bipolar transistor effects [110]. However, the ability of body ties to suppress the bipolar effect strongly depends on the relative positions of the body tie and the ion strike [72, 112].

- **Regeneration**

Trapped holes and interface traps can undergo a gradual annealing allowing the recovery of degradation induced by radiation. Several models have been proposed to explain trapped hole annealing. In these models, the combined mechanisms thermal emission and tunneling predict accuratelly the annealing process. The probability of charge detrapping depends strongly on the anneal temperature.

Annealing tests have been originally defined by standard procedures (MIL-STD-883E, Test Method 1019), in order to estimate the characteristics of radiation-induced trapped charges in the oxides of CMOS technologies and to detect a possible rebound effect. These procedures, applied after irradiation, are intended to predict the response of components during the specified mission using accelerated test conditions.

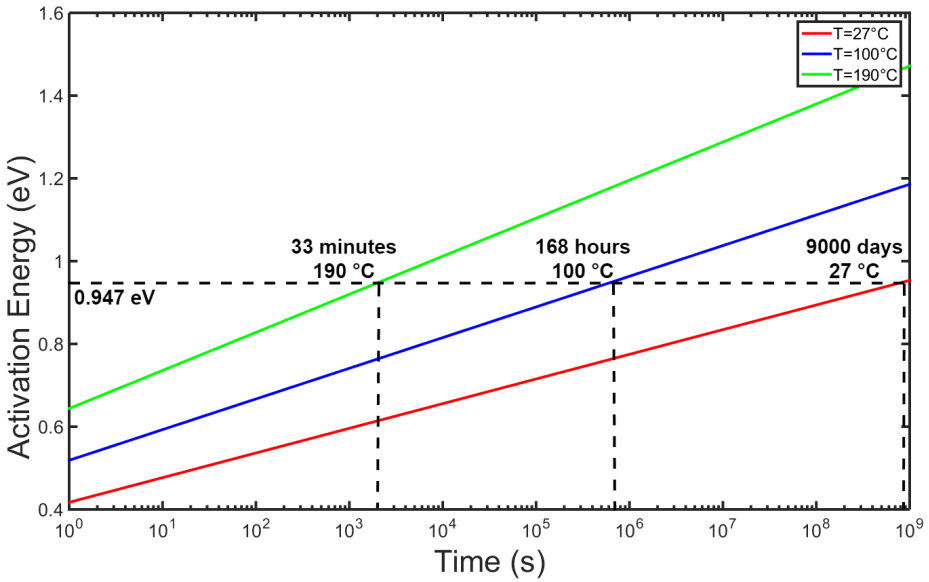


Figure 1.19: Time-temperature equivalence of annealing model.

On the other hand, several works have applied annealing to transistors during their exposure to radiation in order to recover the degradation induced by total ionizing dose and then extend their lifetime. This kind of regeneration is a thermally activated process that can be modeled by Arhenius's law [113, 114]. According to this model, the recovery of the electrical characteristics is more efficient when applying high temperatures.

Moreover, this model assumes an equivalence between time and temperature, which means that an elevated temperature annealling for a short duration can lead to the same charge detrapping as a lower temperature annealling for a longer duration. As shown by the example in Figure 1.19, a thermal annealling of 168 hours at 100 °C, as defined by the MIL-STD-883 standard, can detrap all charges in the insulating oxides having an activation energy below 0.947 eV. While at room temperature, 9000 days (around 24 years and 7 months) are required to reach this energy level.

- **Backgate bias of SOI transistors**

  In order to compensate for the V_{th} degradation produced by TID, some works have used the intrinsic property of modulating the threshold voltage of FDSOI transistors. In [92], authors proposed to calibrate back-gate voltage V_{bg} of irradiated transistors in order to cancel the threshold voltage degradation. Authors proposed a hardening strategy for nanoscaled ultra-thin BOX and body SOI technologies which is based neither on a hardening by design approach nor on a technology hardening technique. The main idea was to cancel the negative threshold voltage shift induced by TID by applying a negative back-bias to the N/P well regions. However, with this technique, the back-bias required to compensate the voltage shift induced by a high absorbed dose could be very high and, as a consequence, could cause an increase in power consumption and reliability issues.

1.6 Conclusion of the chapter

In this chapter, we introduced the effect of total ionizing dose on bulk and FDSOI transistors and we reported some hardening techniques proposed so far to decrease radiation-induced degradation on electronic devices. In this thesis we are particularly interested in FDSOI technology as it shows multiple advantages over other technologies in the design of integrated circuits. Especially, the BOX insulating layer and the intrinsic silicon layer introduce an electrostatic coupling between the front and back gates which allows the modulation of the threshold voltage in both directions. However, the addition of the BOX makes this technology more sensitive to the effects of TID. The degradation of electrical characteristics can be quite large and appropriate margins should be applied in the circuit design to have electronic systems still able to operate after receiving high dose levels. Hence, a prior knowledge of the induced-degradation on the circuit under test can help considering appropriate margins and applying an appropriate hardening technique. This can be obtained by developing accurate models of TID effects to maintain the reliability of FDSOI transistors under harsh environments such as civil nuclear or space.

Chapter 2

Theoretical study of the TID degradation and recovery mechanisms of FDSOI transistors

In this chapter we analyze the physical impact of the TID on the 28nm FDSOI technology. The effect of oxide and interface trapped charges on the electrical characteristics of FDSOI transistor is characterized through an analytical modeling. The principal methods, used throughout this thesis, to extract the electrical parameters of transistors are also described. Finally, a study about the recovery methods is carried out to observe and justify their efficiency when applied to this technology.

2.1 Physical analysis of radiation-induced effect on FDSOI transistor

As previously mentioned, electrostatic coupling between the front and back gates is a key advantage of FDSOI technology. A variation in the back surface potential Ψ_{sb} changes the front surface potential Ψ_{sf}, which modifies the front threshold voltage V_{tf}. This is why a FDSOI transistor can be seen as a double-gate MOSFET. This defines nine possible operating modes depending on the series of combinations in its gates voltages as shown in Figure 2.1.

The operating modes of a SOI structure are the same as those of bulk-devices: accumulation when $\Psi = 0$, depletion when $\Phi_F < \Psi < 2\Phi_F$ and inversion when $\Psi > 2\Phi_F$, Φ_F being the Fermi potential defined as the difference of the Fermi levels and the intrinsic level, and expressed as $\Phi_F = \frac{kT}{q} ln(\frac{N_{sub}}{ni})$ [115, 116].

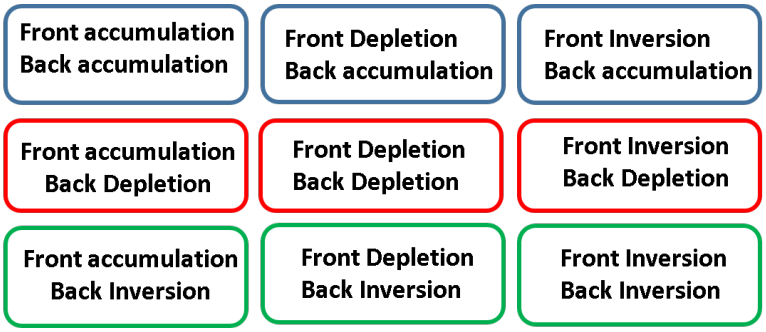


Figure 2.1: Operation modes of a FDSOI transistor.

The energy band diagram of a SOI structure is shown in Figure 2.2. It is composed of several regions which correspond to the front gate, the gate oxide, a silicon semiconductor layer, the buried oxide (BOX), and the back-gate.

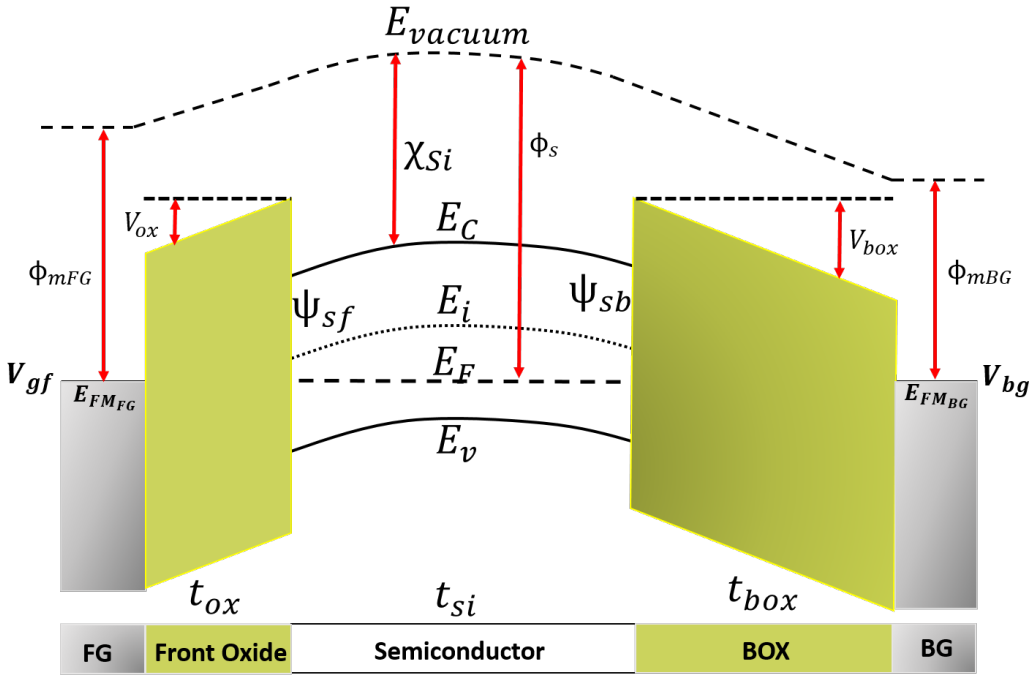


Figure 2.2: Band Diagram of a SOI structure.

The work function (WF) of a metal corresponds to the minimum energy required to extract an electron from it [117]. We define the metal-semiconductor work-function Φ_{ms} as the difference between the metal work-function of the front or back gate and the semiconductor work function [17, 118]:

$$V_{FB} = \Phi_{ms} = \Phi_m - [\chi_{si} - \frac{E_g}{2} - \Phi_F] = \Phi_m - [\chi_{si} - \frac{E_g}{2} - \frac{kT}{q} ln(\frac{N_A}{n_i})] \tag{2.1}$$

Φ_{ms}, also called Flat-band voltage V_{FB} defined as the condition where the conduction band E_c and the valence

band E_v of the body are flat at the Si–SiO_2 interface. In this condition, the surface potential as well as the electric field are equal to zero. This is achieved by applying a negative voltage to the gate [17, 118].

In equation 2.1 the quantity χ_{Si}, called electron affinity, defines the difference between the vacuum level E_0 and the bottom of conduction band of Si E_c [118]. From equation 2.1, the front and back metal-semiconductor work functions can be given by:

$$\begin{cases} \Phi_{msf} = & \Phi_{mFG} - \Phi_s \\ \Phi_{msb} = & \Phi_{mBG} - \Phi_s \end{cases} \tag{2.2}$$

The Poisson's equation is a useful approach to the calculation of electric potentials because it relates the potential to the charge density which gives rise to it. This equation has long been used in the modeling of the electric potential in MOSFET and FDSOI structures [119, 120]. For practical use, we will focus on solving this equation in a dimension expressed as:

$$\nabla \epsilon \nabla \Psi = -\rho \tag{2.3}$$

Where ρ is the charge density and ϵ the permittivity of the material. In order to analyze the impact of TID on the FDSOI MOSFET, we distinguish three regions displayed in Figure 2.3 where x represents the depth in the FDSOI structure: the gate oxide region $-t_{ox} < x < 0$, the intrinsic channel region $0 < x < t_{si}$ and the BOX region $t_{si} < x < t_{si} + t_{box}$. For this analysis, we ignore the depletion region present at the BOX-substrate interface. The calculations are inspired from the Lim-Fossum model [94].

- The region $-t_{ox} < x < 0$ corresponds to the the gate oxide region. In ideal conditions, the net charge across the oxide is zero. However, when subjected to TID, a build-up of charges are created which modifies the net charge in the oxide. So, taking into account the oxide trapped charges, Poisson's equation becomes:

$$\frac{d^2\psi}{dx^2} = \begin{cases} 0 & \text{if } N_{ot} = 0 \\ \frac{qN_{ot}t_{ox}}{\epsilon_{ox}} & \text{if } N_{ot} \geq 0 \end{cases} \tag{2.4}$$

  By integrating the expression given in equation 2.4 once and then twice, we can obtain the electric field across the oxide and the surface potential, respectively, whether or not there is oxide charge trapping:

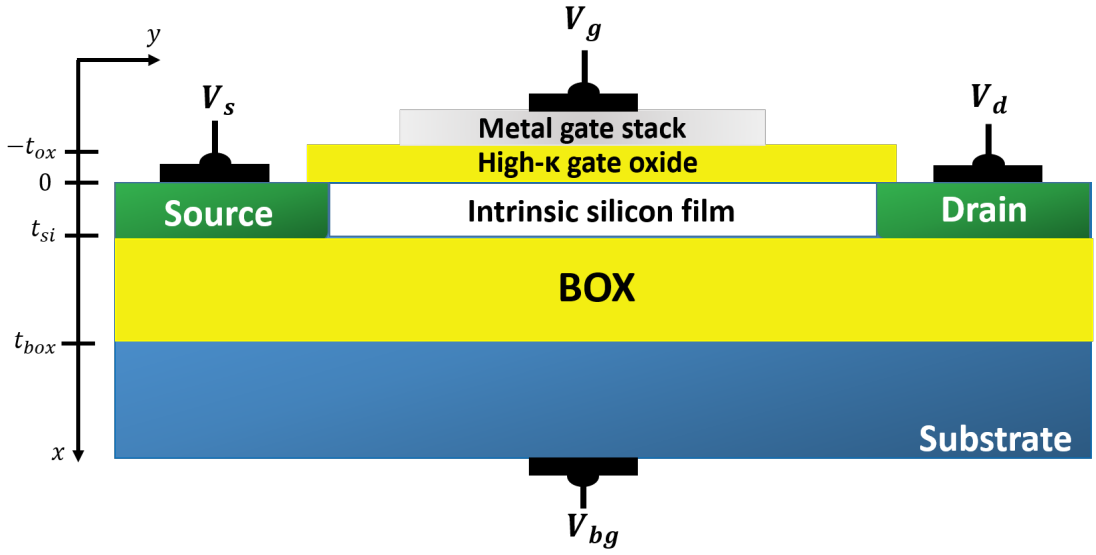


Figure 2.3: Cross section view of different regions of a FDSOI transistor.

$$E = \begin{cases} K_1 & \text{if } N_{ot} = 0 \\ \frac{qN_{ot}t_{ox}}{C_{ox}}x + C_1 & \text{if } N_{ot} \geq 0 \end{cases} \tag{2.5}$$

$$\Psi = \begin{cases} -K_1 x + D_1 & \text{if } N_{ot} = 0 \\ \frac{qN_{ot}t_{ox}}{C_{ox}}x^2 + C_2 x + C_3 & \text{if } N_{ot} \geq 0 \end{cases} \tag{2.6}$$

- The region $0 < x < t_{si}$ represents the intrinsic silicon film of the FDSOI transistor. Poisson's equation across this region is then expressed as:

$$\frac{d^2\psi}{dx^2} = \frac{qN_A}{\epsilon_{Si}} \tag{2.7}$$

By integrating once, we can find the behavior of the electric field along the channel:

$$E_{s2} = E_{s1} - \frac{qN_A t_{si}}{\epsilon_{si}} \tag{2.8}$$

And then the surface potential is given as follows:

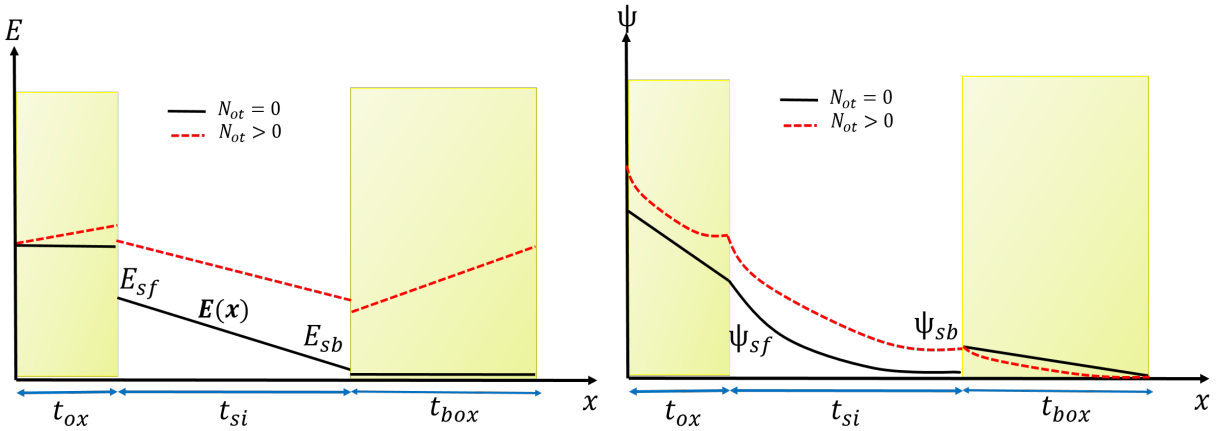
$$\Psi_{s_2} = \Psi_{s_1} - E_{s1}t_{si} - \frac{qN_A t_{si}^2}{\epsilon_{si}} \tag{2.9}$$

- The region $t_{si} < x < t_{si} + t_{box}$ corresponds to the buried oxide BOX. Like for the front oxide, without TID the net charge in the oxide is zero. However, N_{ot} plays an important role in disturbing the electric field and the surface potential in this region, where the electric field and the surface potential can be expressed as follows:

$$E = \begin{cases} K_2 & \text{if } N_{ot} = 0 \\ \frac{qN_{ot}t_{box}}{C_{box}}x + C_4 & \text{if } N_{ot} \geq 0 \end{cases} \tag{2.10}$$

$$\Psi = \begin{cases} -K_2 x + D_2 & \text{if } N_{ot} = 0 \\ \frac{qN_{ot}t_{ox}}{C_{ox}}x^2 + C_4 x + C_5 & \text{if } N_{ot} \geq 0 \end{cases} \tag{2.11}$$

With C_1, C_2, C_3, D_1, D_2, K_1 and K_2 constants.



(a) Electric Field. (b) Surface Potential.

Figure 2.4: Electric field and surface potential profile in the intrinsic channel.

The equivalent capacitive circuit displayed in the Figure 2.5 illustrates the intervention of the surface potentials and the capacitances of the SOI structure.

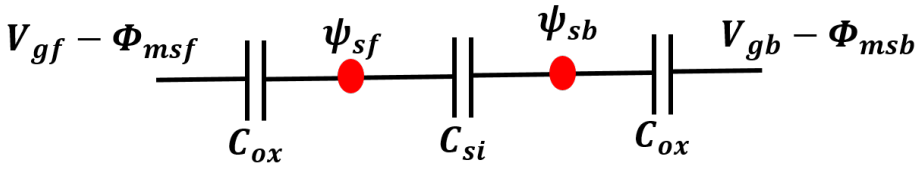


Figure 2.5: Capacitive equivalent circuit of a SOI structure.

We can analyze separately the two MOS structures, front and and back ones separately, and observe the influence of surface potentials in each. As can be inferred from Figure 2.4, for the front gate, we can write this equivalence:

$$V_{gf} - \Phi_{msf} = V_{ox} + \Psi_{sf} \tag{2.12}$$

In the same way, for the back gate we can write:

$$V_{gb} - \Phi_{msb} = V_{box} + \Psi_{sb} \tag{2.13}$$

After applying Gauss's theorem to the SOI structure, we obtain the characteristic equations 2.14 and 2.15 of the front and back gates, respectively [94, 121]. The complete analysis on how to obtain these equations is given in Appendix A.1.

$$V_{fg} - \Phi_{msf} = (1 + \frac{C_{si}}{C_{ox}})\Psi_{sf} - \frac{C_{si}}{C_{ox}}\Psi_{sb} + \frac{Q_{dep}}{2C_{ox}} \tag{2.14}$$

$$V_{gb} - \Phi_{msb} = (1 + \frac{C_{si}}{C_{box}})\Psi_{sb} - \frac{C_{si}}{C_{box}}\Psi_{sf} + \frac{Q_{dep}}{2C_{ox}} \tag{2.15}$$

Then, taking into account the contributions of the charges trapped in the volume of the oxides and at the interfaces, the front and back gate characteristic equations can be written as [122]:

$$V_{fg} - [\Phi_{msf} + \frac{Q_{otox}}{C_{ox}}] = (1 + \frac{C_{si} + C_{itf}}{C_{ox}})\Psi_{sf} - \frac{C_{si}}{C_{ox}}\Psi_{sb} + \frac{Q_{dep}}{2C_{ox}} \tag{2.16}$$

$$V_{gb} - [\Phi_{msb} + \frac{Q_{otbox}}{C_{box}}] = (1 + \frac{C_{si} + C_{itb}}{C_{box}})\Psi_{sb} - \frac{C_{si}}{C_{box}}\Psi_{sf} + \frac{Q_{dep}}{2C_{ox}} \tag{2.17}$$

Where the interface trapped charges capacitance is:

$$C_{it} = \begin{cases} C_{itf} & = qD_{itf} \\ C_{itb} & = qD_{itb} \end{cases} \tag{2.18}$$

2.2 Effect of oxide and interface trapped charges

2.2.1 Oxide trapped charges N_{ot}

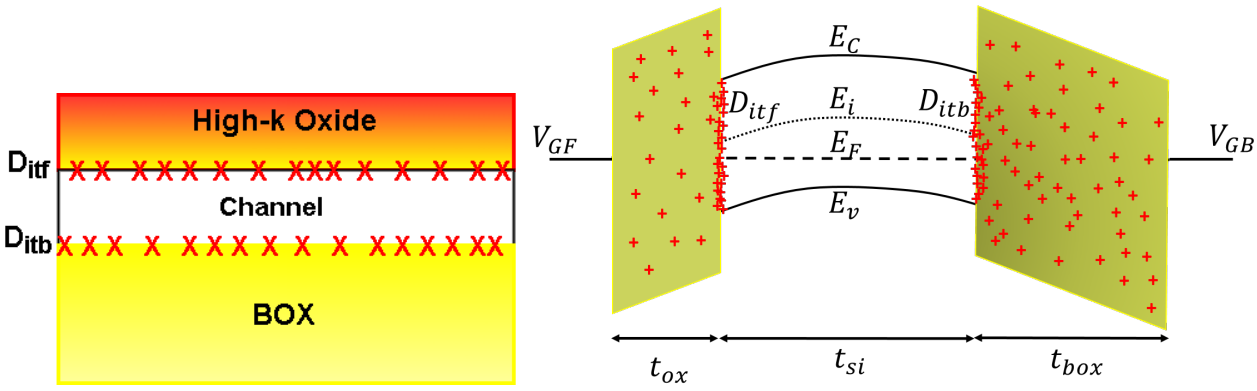
As seen previously, the charges trapped in insulating oxides (N_{ot}) disturb the electric field in MOSFET transistors. This impacts the flat-band voltage V_{FB} directly linked to the metal-semiconductor work function of the SOI structure. The shift of V_{FB} induced by oxide charge trapping can be expressed as follows:

$$\Delta V_{FB_{Not}} = \Phi_{msf} + \frac{Q_{ox,box}}{C_{ox,box}} = \Phi_{msf} + \frac{qN_{otf,b}t_{ox,box}}{C_{ox,box}} \tag{2.19}$$

Where $Q_{ox,box}$ are the charges induced by the oxide trapped charges in the gate oxide or in the BOX. $N_{otf,b}$ are the oxide trapped charges density of the front oxide or the BOX. As Φ_{msf} , $C_{ox,box}$, $t_{ox,box}$ are known physical parameters, it is necessary to determine how N_{ot} evolves with TID for having an evaluation of the flat-band voltage shift.

2.2.2 Interface trapped charges D_{it}

As previously reported, the density of charges trapped at the interfaces of the transistors has a direct impact on the subthreshold slope, leading to a degradation in the response of a transistor when switching from OFF to ON state and, in a large-scale circuit, a degradation in operating frequency. To analyze the impact of Dit on the subthreshold slope, the first hypothesis to take into account is the presence of two layers of interface trapped charges. These charges located at the front ($Si - SiO_2$) and back ($Si - BOX$) interfaces called D_{itf} and D_{itb} are responsible for modifying front and back surface potential Ψ_{sf} and Ψ_{sb}.



(a) Interface trapped charges.

(b) Band diagramm of an SOI structure including interface trapped charges.

Figure 2.6: Interface trapped charges in a FDSOI device.

Study of the impact of D_{it} on Subthreshold Slope SS

The subthreshold slope SS is a key feature that reflects the switching performance of MOSFET [121, 123, 124]. A sharper slope is essential for achieving low-power, low-voltage CMOS [125]. However, the reduction of the supply voltage of MOSFETs is limited by the floor value of the subthreshold slope, which cannot be lowered below the thermionic limit of 60 mV/decade [103]. To solve this problem, new solutions including new structures such as Tunneling Field Effect Transistors (TFETs) [126] or Ferroelectric FETs [127], and operation modes such as cryogenic operation [128, 129, 130] and negative capacitance [131] have been proposed to reduce the SS lower than the theoretical thermionic operation [132]. Despite these improvements, the exposure of MOSFET devices to ionizing radiation still produces degradation of the SS, which affects the switching speed and as a consequence the operating frequency of an IC.

The subthreshold-slope is expressed as the inverse of the ratio between the drain current and the applied gate voltage [122]:

$$SS = \frac{dV_{gs}}{d(logI_{ds})} \tag{2.20}$$

Hence, without taking into account the effect of interface trapping, the subthreshold slope can be written as:

$$SS = \frac{kT}{q} ln10(1 + \frac{Csi}{C_{ox}}) \tag{2.21}$$

If the influence of the capacitances of both interfaces is considered, we obtain the equation of the subthreshold slope with the contributions of both interfaces [122]. The complete analysis on how we get this equation is given in Appendix A.2

$$SS = \frac{kT}{q} ln10 \frac{dV_{gf}}{d\Psi_{sf}} = \frac{kT}{q} ln10[(1 + \frac{C_{si}}{C_{ox}} + \frac{C_{itf}}{C_{ox}}) - \frac{\frac{C_{si}^2}{C_{ox}C_{box}}}{(1 + \frac{C_{si}}{C_{box}} + \frac{C_{itb}}{C_{box}})}] \tag{2.22}$$

In the following chapter, a modeling of N_{ot} and D_{it} for high dose levels will be carried out to describe their impact on ΔV_{FB} and SS respectively. Furthermore, trapped charges can cause variations in the different modes of operation depending on the voltages applied to both gates, as discussed below.

2.3 Control of the threshold voltage with back-gate bias

The operation modes of a Bulk-MOSFET are well known according to its surface potential. They can also be transposed for SOI technology. As a reminder, the operating modes are:

Accumulation ($\Psi = 0$), depletion ($\Phi_F < \Psi < 2\Phi_F$) and inversion ($\Psi > 2\Phi_F$) with $\Phi_F = \frac{kT}{q} ln(\frac{N_A}{ni})$ the Fermi potential [17, 118].

2.3.1 Threshold voltage with the back-gate in accumulation mode

Increasing the back-gate voltage increases the front surface potential. We consider for our analysis, that the front channel is in inversion, then $\Psi_{sf} = 2\Phi_F$ and $Q_{inv} = \frac{1}{2}Q_{dep}$. If the back-gate is in the accumulation region then $\Psi_{sb} = 0$. Substituting these values in the equation 2.16, we obtain the threshold voltage with the back-gate in accumulation taking into account the oxide and interface trapped charges:

$$V_{Tf}^{A} = \Phi_{msf} + \frac{qN_{otf}t_{ox}}{C_{ox}} + (1 + \frac{C_{si} + C_{itf}}{C_{ox}})2\Phi_F - \frac{Q_{dep}}{2C_{ox}} \tag{2.23}$$

2.3.2 Threshold voltage with the back-gate in inversion mode

When the back gate is in inversion region that means a $\Psi_{sb} = 2\Phi_F$. Therefore, substituting this condition in the equation 2.16, the threshold voltage becomes:

$$V_{Tf}^{inv} = \Phi_{msf} + \frac{qN_{otf}t_{ox}}{C_{ox}} + (1 + \frac{C_{itf}}{C_{ox}})2\Phi_F - \frac{Q_{dep}}{2C_{ox}} \tag{2.24}$$

2.3.3 Threshold voltage with the back-gate in depletion mode:

The inversion mode of the back gate allows a drain current to flow even if $V_{gf} \leq V_{Tf}^{inv}$, being useless for practical applications. Then, the proper mode of operation is when the applied back bias is either in depletion or accumulation mode. Therefore the equation corresponding to this mode of operation is given by:

$$V_{tf}^{D} = V_{Tf}^{A} - (\frac{C_{si}C_{box}}{C_{ox}(C_{si} + C_{itb} + C_{box})}[V_{bg} - V_{bg}^{acc}]) \tag{2.25}$$

The complete derivation leading to arrive to this equation is given in Appendix A.3.

We define the Body-Factor (n) as a constant that represents the electrostatic coupling between both interfaces. It represents also the capacity of the SOI structure to modulate the threshold voltage V_{th} expressed in mV/V. The value of n corresponds to the slope of the $V_{tf}(V_{bg})$ function shown in Figure 2.7:

$$n = \frac{dV_{Tf}^{D}}{dV_{bg}} = -\frac{C_{Si}C_{box}}{C_{ox}(C_{si} + C_{itb} + C_{box})} \tag{2.26}$$

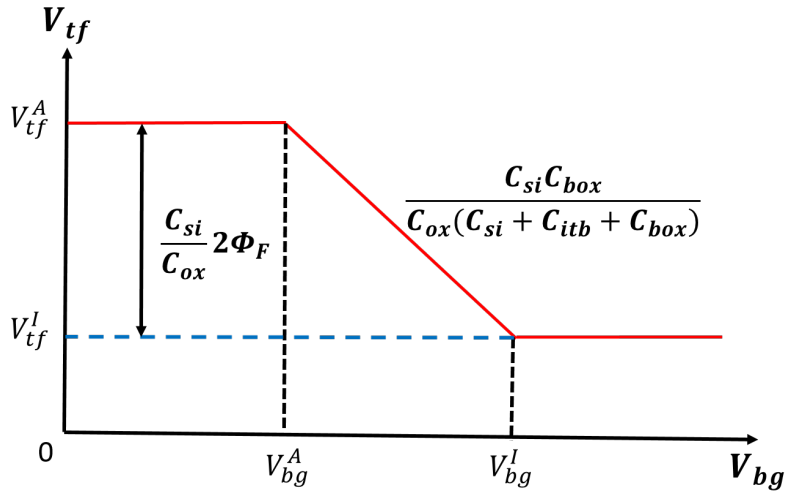


Figure 2.7: Operating modes of a SOI transistor as a function of the back-gate bias.

Hence, the variation of the front threshold voltage can be expressed as:

$$\Delta V_{tf} = [V_{Tf}^{A} - V_{Tf}^{inv}] = \frac{C_{si}}{C_{ox}} 2\Phi_F \tag{2.27}$$

2.4 Recovery mechanisms of irradiated FDSOI MOSFETs

After irradiation, the charges trapped in insulating oxides may remain trapped for a long time. The detrapping of these charges occurs naturally at room temperature, so a progressive recovery of the electrical parameters degraded by radiation is expected. However, this process is very slow and can take from few hours to years [133]. Two main recovery phenomena have been studied for years. The tunnel effect and the detrapping by annealing [134, 135].

2.4.1 Tunnel effect

The tunnel effect considered here describes the passage of an electron from silicon to the oxide followed by its recombination with a trapped hole [135]. This effect is promoted by the electric field and is independent of the temperature. The model that describes the tunnel effect is represented by a vertical front moving from the $Si - SiO_2$ interface toward the oxide, as depicted in Figure 2.8. All the carriers trapped between the silicon and the front are detrapped while those beyond the tunnel front remain trapped. The probability σ_{tunnel} of a hole tunneling out of the oxide depends exponentially on the distance from the trap level to the $Si - Si0_2$ interface, and is given by[135, 136]:

$$\sigma_{tunnel} = \alpha exp^{-\beta x} \tag{2.28}$$

Where α is the attempt to escape frequency, β is related to the tunneling barrier and x is the position in the oxide. Thus, the position of the tunneling front is determined as in [136] and is expressed as:

$$X_m(t) = \frac{1}{\beta} ln(\alpha t) \tag{2.29}$$

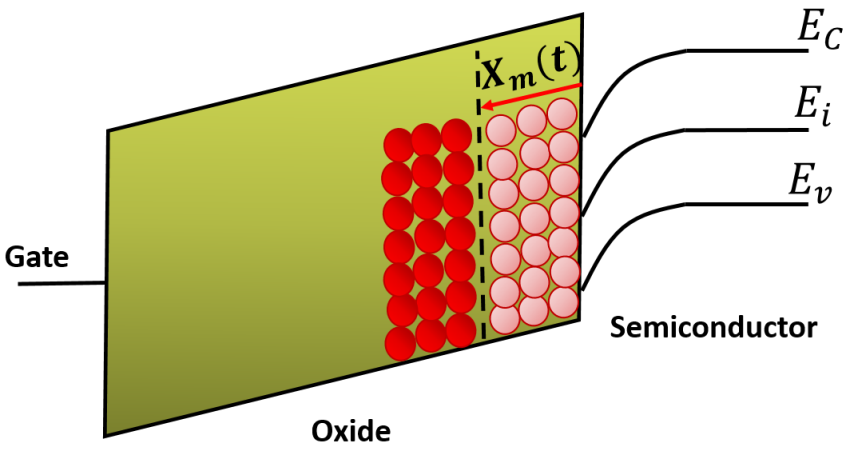


Figure 2.8: Tunnel effect model.

It was found that detrapping by tunneling is predominant at room temperature, which means a continuous but very long detrapping in steady state[136, 137]. The speed of the recovery front due to the tunnel effect was estimated in a range of 0.2 nm to 0.4 nm per decade of time [4, 136].

2.4.2 Thermal annealing

The detrapping of charges is a phenomenon that can occur slowly at room temperature and that could be accelerated by increasing the temperature [137, 138]. The higher the temperature, the higher the rate of charge detrapping and consequently the faster recovery of the degraded electrical characteristics of an irradiated transistor.

Some works [139] have proposed a detrapping model based on thermal effect by assuming that the dominant recovery mechanism is the thermal emission of charges from the valence band of the oxide. So, the recovery by thermal activation has been modeled as an horizontal front that moves from the valence band to the conduction band inside the oxide gap as shown in Figure 2.9. This model states that the charges located between the top of the valence band and the thermal front are neutralized, while those located beyond the front remain active, and therefore, the holes remain trapped [136].

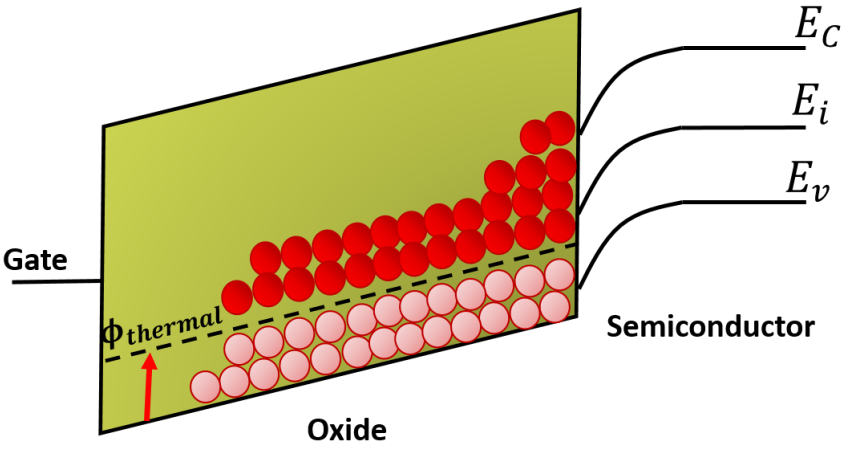


Figure 2.9: Thermal annealing model.

The position of the thermal front can be estimated assuming that the detrapping of charges is a first-order chemical reaction [113] where the probability $\sigma_{thermal}$ that a charge is detrapped follows the Arrhenius law [140].

$$\sigma_{thermal} = Aexp(-\frac{E_{act}}{kT}) \tag{2.30}$$

Where A is the frequency factor (s^{-1}), E_{act} is the activation energy (eV), k is the Boltzmann constant (eVK^{-1}) and T is the absolute temperature (K). In order to reach a specific activation energy, the annealing time and temperature must be chosen following the time-temperature equivalence as in [138]. We can rewrite Eq.2.30 to introduce the time constant $\tau = \frac{1}{\sigma_{thermal}}$ and $\Phi_{thermal}$ the position of the thermal front to reach a specific activation energy [136]:

$$\tau = \frac{1}{A}exp(\frac{\Phi_{thermal}}{kT}) \tag{2.31}$$

Using equation 2.31, we can estimate the temperature and annealing time required to reach a given activation energy level as follows [136]:

$$\Phi_{thermal} = kTln(A\tau) \tag{2.32}$$

As an example, we can see in Figure 2.10 the time-temperature equivalences necessary to reach an activation energy level E_{act} of 0.9, 0.95 0.97 and 1 eV, respectively, for a frequency factor $A = 1 \times 10^7\ s^{-1}$. In this case, the higher the activation energy level to be achieved, the higher the time-temperature compromise.

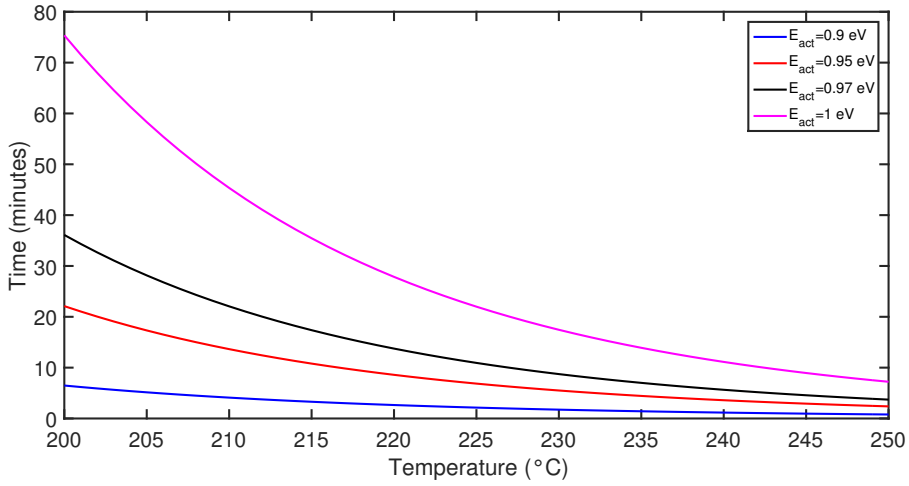
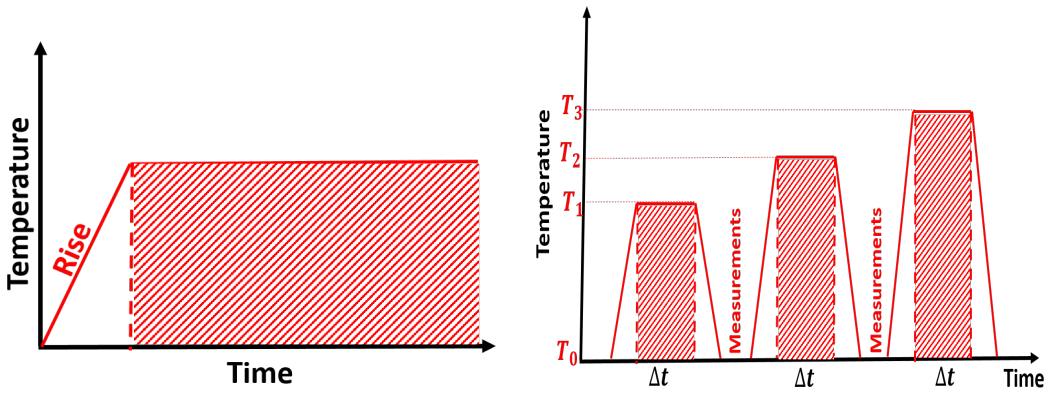


Figure 2.10: Time-Temperature equivalence for different activation energy levels

The position of the thermal front in the oxide can vary according to the method used to apply the thermal annealing. In this work, we will focus on two methods: the isothermal and the isochronal annealing shown in Figure 2.11.



(a) Isothermal.

(b) Isochronal.

Figure 2.11: Methods for the thermal annealing.

- The isothermal annealing (Figure 2.11 (a)) corresponds to a constant temperature applied over a long period of time. By applying this type of annealing we can predict the variation of the trapped charges over time with the following differential equation [113, 141]:

$$\frac{dn(t)}{dt} = -\sigma_{thermal} n(t) = -\frac{1}{\tau} n(t) \tag{2.33}$$

- The isochronal annealing (Figure 2.11 (b)) consists of a series of applied cycles of linearly rising temperatures with finite duration Δt, separated by periods of measurements at ambient temperature[113, 142]. Therefore,

the equation 2.34 models the detrapping rate followed by an isochronal annealing:

$$\frac{dn(t)}{dt} = -\sigma_{thermal} n(t) = -Aexp(-\frac{E_{act}}{kT})n(t) \tag{2.34}$$

Where the solution of this first-order differential equation is:

$$n(t) = n(0)exp[-A\int exp(-\frac{E_{act}}{kT(t')})dt'] \tag{2.35}$$

With $T = ct + T_0$, where $c = \frac{dT}{dt}$ is the slope heating rate and T_0 is the initial value of T. Hence, the trapped charges can be written as follows:

$$n(T) = n(0)exp[-\frac{A}{c}\int_{T_0}^{T} exp(-\frac{E_{act}}{kT'})dT'] \tag{2.36}$$

As explained in [141], the second derivative $\frac{d^2n(T)}{dT^2}$ presents a maximum corresponding to an inflection point of $n(T)$ at a characteristic temperature T^* that is directly related to the activation energy (see Figure 2.12). As can be find in the Appendix B, by knowing the heating slope c and the frequency factor A, we can the relation between the activation energy and the characteristic temperature as:

$$\frac{E_{act}}{kT*} = ln(\frac{AkT*^2}{cE_{act}}) \tag{2.37}$$

In this way, it is possible to extract the activation energy of a device after annealing. In an irradiated device, the charges can be trapped at different energy levels, therefore, for the same device there are different levels of activation energy which must be reached to detrap these charges.

According to the state of the art, the values proposed for the frequency factor A are quite wide, and strongly depend on the characterization method. These values ranges from: $10^7\ s^{-1}$ to $10^{14}\ s^{-1}$. The lowest values are generally obtained with I-V techniques, whereas the highest ones are obtained by using specific Thermo-Stimulated Current (TSC) techniques [113].

A model taking into account these two phenomena was proposed by McWorther in [136]. However, in this work, we make the assumption that $\sigma_{thermal} >> \sigma_{tunnel}$, that is, the contribution of the tunnel effect to the recovery of the electrical characteristics of an irradiated device is negligible compared to the contribution of the thermal one. This fact can be justified, as the technology studied in this work uses High-κ oxide above the gate oxide in order to avoid gate-to-channel tunneling. So, for our purpose, only thermal annealing will be taken into account as a regeneration mechanism.

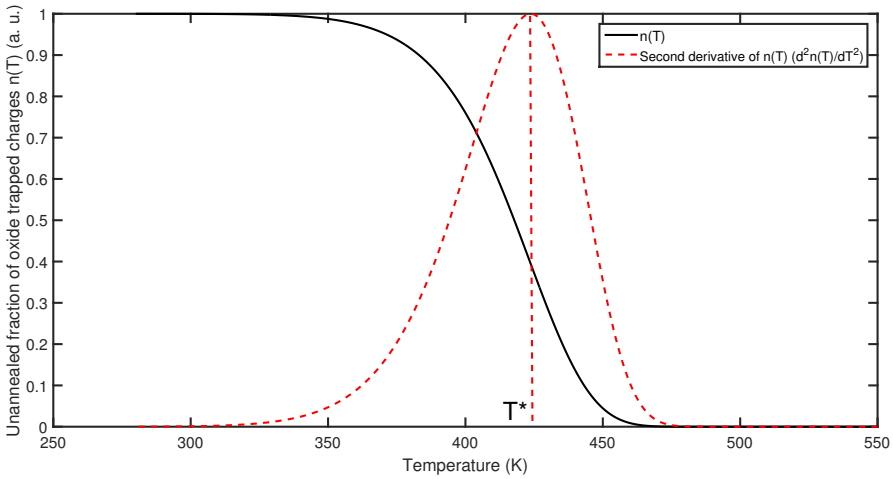
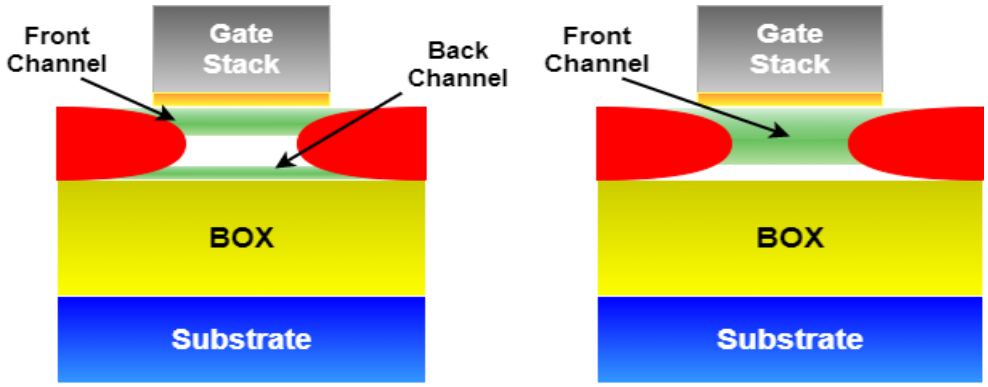


Figure 2.12: Relation between activation energy and characteristic temperature.

2.4.3 Threshold voltage compensation

As already mentioned, the coupling effect between front-gate and back-gate allows the control of the threshold voltage. Tuning the applied back-gate voltage V_{bg} modifies the front threshold voltage towards more positive or negative values [143]. This property has been used by IC designers to optimize the performance of the transistor at the expense of an increase in power consumption [83, 144]. So, depending on the applied V_{bg}, the threshold-voltage modulation can be analyzed by distinguishing two cases:



(a) Positive V_{bg}.

(b) Negative V_{bg}.

Figure 2.13: Body-biasing of a FDSOI device.

- Case 1- positive V_{bg}: When a positive V_{bg} is applied, the holes present in the intrinsic channel are repelled toward the SiO_2-Si interface. Consequently, the electrons are attracted to the $Si-BOX$ interface, forming a second conduction channel. This has an impact on the front surface potential and the direct consequence is a higher inversion charge in the main conduction channel which induces a negative shift of V_{th}. As mentioned in Chapter 1 of this thesis, this case is called Forward Body-Bias (FBB).

- Case 2- negative V_{bg}: When a negative V_{bg} is applied, the electrons of the intrinsic silicon layer are repelled towards the $Si - SiO_2$ interface of the front transistor forming a more conductive channel (Figure 2.13). The front surface potential is increased producing a positive shift of the threshold voltage. This case of biasing is called Reverse Body-Bias (FBB).

The effect on the threshold voltage in both cases can be observed in Figure 2.14.

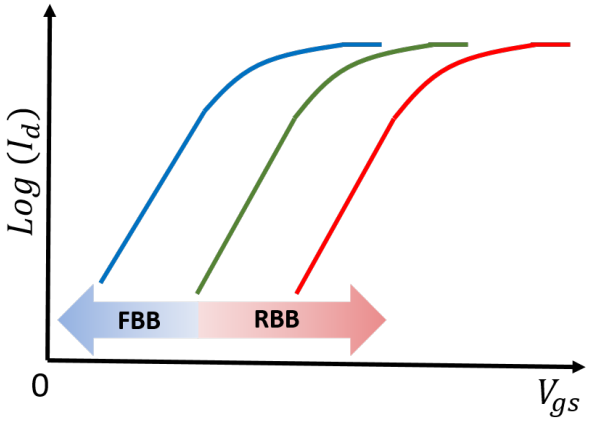


Figure 2.14: Threshold voltage modulation by apllying a V_{bg}.

Taking into account this intrinsic property of the FDSOI technology, we can deduce that a RBB can fully or partially compensate for the negative ΔV_{th} induced by the TID. Then, the use of RVT devices is advantageous for applications where FDSOI circuits are exposed to TID, due to the large range of V_{bg} allowed with RBB biasing before the conduction of the intra-substrate junction.

It must be mentioned that these effects only compensate for the negative ΔV_{th} induced by the oxide trapped charges but not for the degradation of the subthreshold-slope caused by the interface trapped charges. Also, The body factor, calculated in Section 2.3.3 varies depending on D_{it} and then, changes the compensation range of the device.

$$n = \frac{C_{si}C_{box}}{C_{ox}(C_{si} + C_{itb} + C_{box})} \tag{2.38}$$

For the 28nm FDSOI technology, n vary between 80 and 85 mV/V [144].

2.5 Electrical characterization of FDSOI MOSFETs

An important issue when working with single transistors is the extraction of electrical parameters that describe the physical behavior of the device. From the electrical measurements made on the transistors, parameters such as

threshold voltage, subthreshold slope, leakage currents, capacitance and transport parameters like carrier mobility can be determined. From these parameters, physical modeling can be carried out to get SPICE libraries able to simulate a device as close as possible to reality.

2.5.1 Threshold voltage V_{th}

The threshold voltage, is defined as the minimum gate-to-source voltage V_{gs} needed to create a conducting path between the source and drain terminals [17, 118]. There are different techniques to extract this parameter from $I_d(V_{gs})$ measurements:

Square root of I_d

One of the traditional methods to extract the threshold voltage is the square root of drain current I_d. This method consists of calculating the square root of the drain current in saturation mode to eliminate the quadratic form. From the drain current in saturation mode, and neglecting the channel length modulation parameter, we have:

$$I_{dsat} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{2.39}$$

The square root is then given as:

$$\sqrt{I_{dsat}} = \sqrt{\frac{1}{2}\mu C_{ox}\frac{W}{L}}(V_{gs} - V_{th}) \tag{2.40}$$

As can be seen in the Figure 2.15, the threshold voltage is obtained when the tangent line intercepts the V_{gs}-axis.

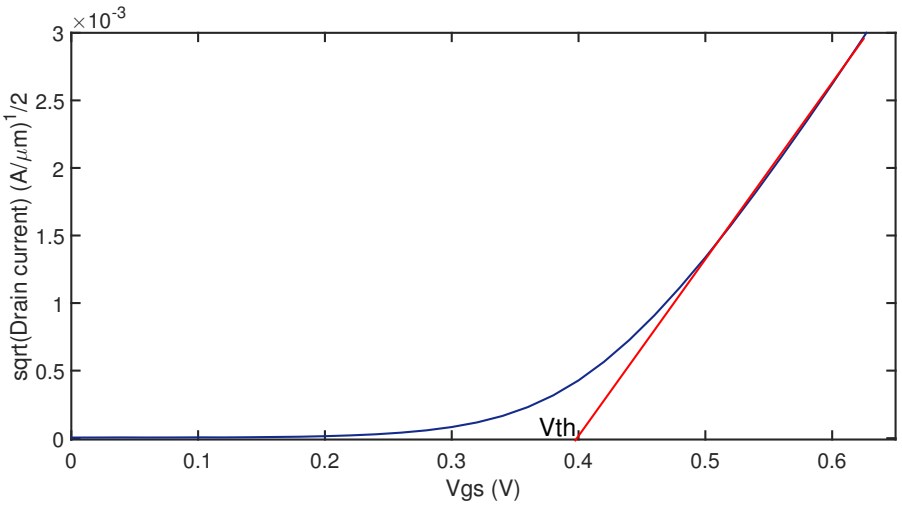


Figure 2.15: Extraction of threshold voltage by square-root of drain current method.

Maximum of derivative of transconductance $\frac{dg_m}{dV_{gs}}$

The method evaluates the transconductance derivative dg_m/dV_{gs} in order to extract the threshold voltage value. In fact, this latter corresponds to the maximum of the transconductance derivative[103] as observed in Figure 2.16. This method is not sensitive to the effects linked to the charge transport in the channel, e.g. serial resistance, mobility degradation, etc [145, 146], but is sensitive to measurement errors and noise. For this reason high quality or smooth I-V measurements are needed to avoid errors in the extraction results [147, 148].

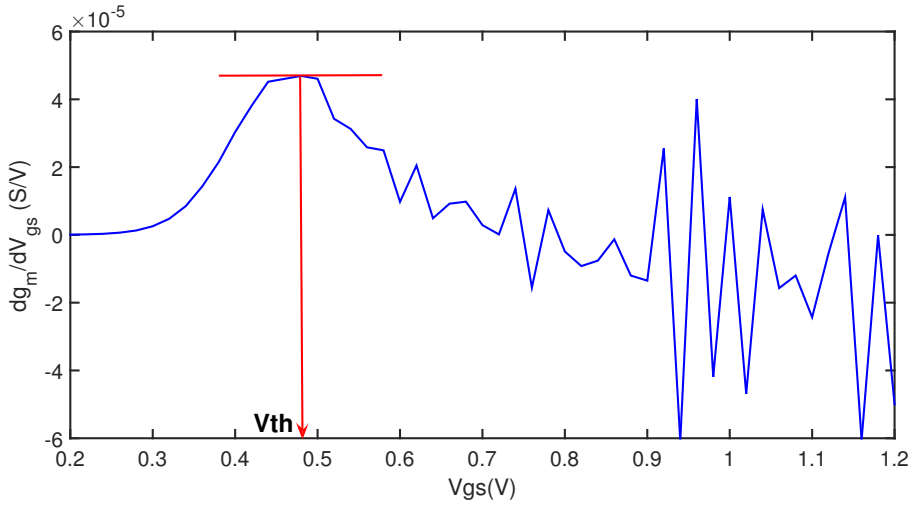


Figure 2.16: Extraction of threshold voltage by transconductance derivative method.

Constant current

A method commonly used in industries to quickly determine the threshold voltage is the constant current method. This method describes the voltage necessary to get a drain current of $10^{-7}\frac{W}{L}$ as depicted in Figure 2.17.

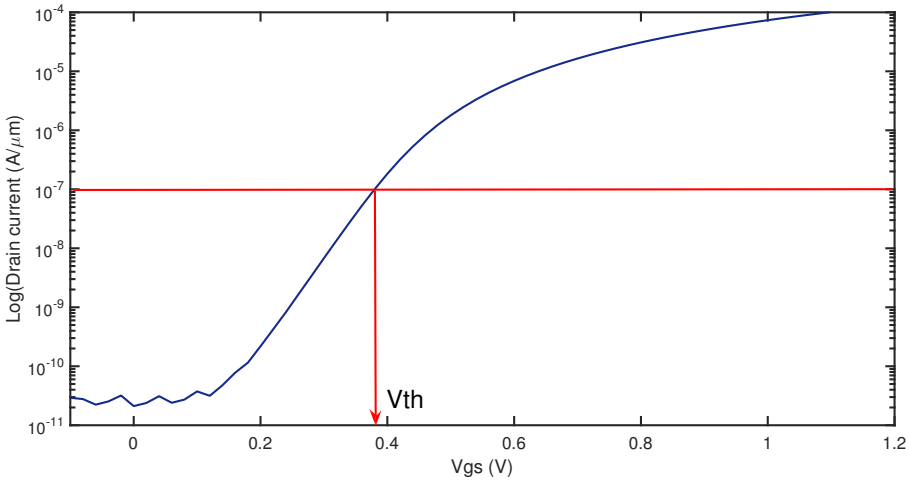


Figure 2.17: Extraction of threshold voltage by constant current method.

However, this method is not adaptable for extracting threshold voltage of FDSOI transistors as the back channel operation can not be eliminated, but it could be practical for a quick estimation of ΔV_{th} after several irradiation steps [149].

Y-function

The Y-function is a powerful tool to extract parameters related to electrical behavior and transport parameters such as mobility. This function, that was firstly introduced in [150], is defined as the ratio of the drain current in linear mode and the square root of the transconductance (Figure 2.18). Thus, the Y-function is expressed as:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\beta}(V_{gs} - V_{th}) \tag{2.41}$$

where $\beta = \frac{W}{L}\mu_0 C_{ox} V_{ds}$ represents the slope of the Y-function.

By calculating the linear fit of this function we can extract V_{th} at the interception point of the straight line and the V_{gs}-axis . The low field mobility μ_0 can be obtained from the slope β, as well as the mobility degradation coefficients θ from the $1/\sqrt{gm}(V_{gs})$[151].

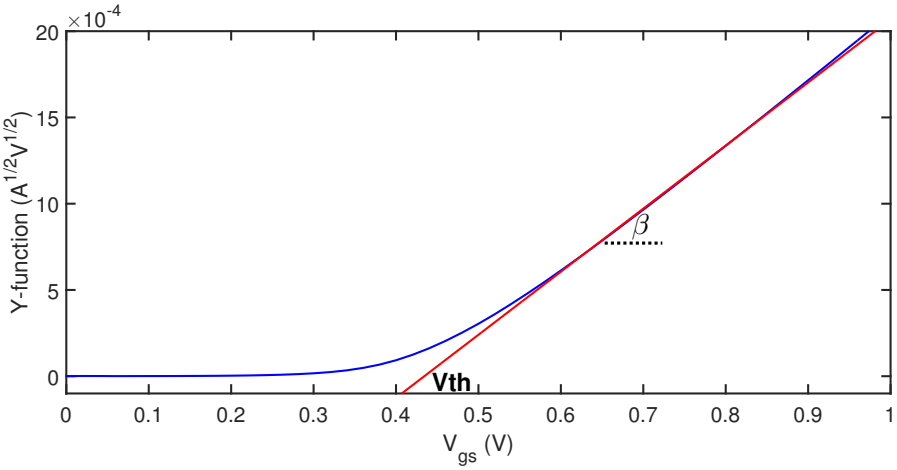


Figure 2.18: Extraction of threshold voltage by Y-function method.

Other works and authors [151] have improved this function by implementing iterative methods with the aim of finding low field mobility attenuation factors θ.

2.5.2 Extraction of trapped charges

The determination of charges trapped in oxides has been the subject of study in the last decades. Many studies have been published proposing both theoretical and experimental characterization methods in order to determine the quantity and energetic and, spatial distribution of the charges.

Charge pumping

The methods for characterizing density of charges trapped at the $Si - SiO_2$ interface commonly involve experimental structures that can be complex. A widely used experimental technique to measure charges at interfaces is the Charge Pumping (CP). The principle of this method consists of repeatedly switching the gate from inversion to accumulation, which results in an average body current [103, 152]. During the transition from inversion to accumulation, only the mobile electrons of the inversion layer are collected [153]. The recombination of the electrons trapped on the interface states with majority carriers gives rise to a current I_{CP} proportional to the average concentration of interface traps D_{it} and frequency f. Then with repetitive pulses with frequency f applied at the gate, I_{cp} is given by [154]:

$$I_{cp} = f \cdot Ar \cdot D_{it} \cdot \Delta E \tag{2.42}$$

Where A the channel area of the transistor.

The basic experimental setup for the charge pumping technique is shown in Figure 2.19 for a N-MOSFET. The gate is pulsed between accumulation and inversion while the charge pumping current is measured in the transistor body.

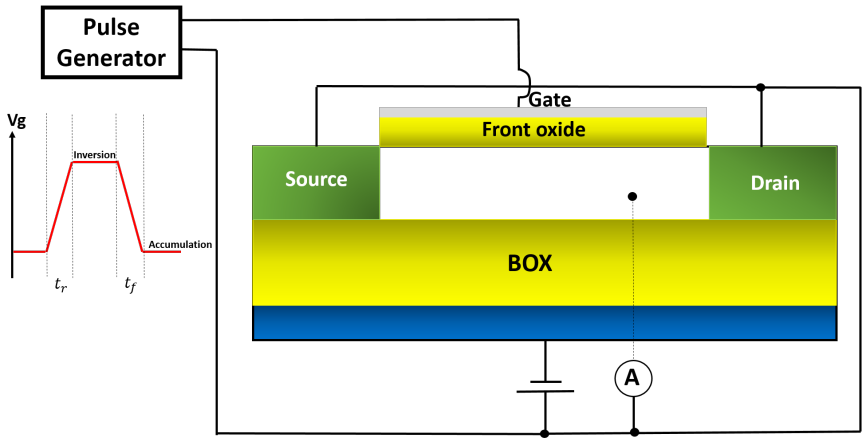


Figure 2.19: Charge pumping experimental setup for SOI devices.

C-V methods

When a MOS device is exposed to ionizing radiation, it exhibits a negative shift in its C-V response as shown in Figure 2.20. As in the case of the I-V curves, extraction of the parameters linked to the increase of charges in insulating oxides can be determined from C-V measurements.

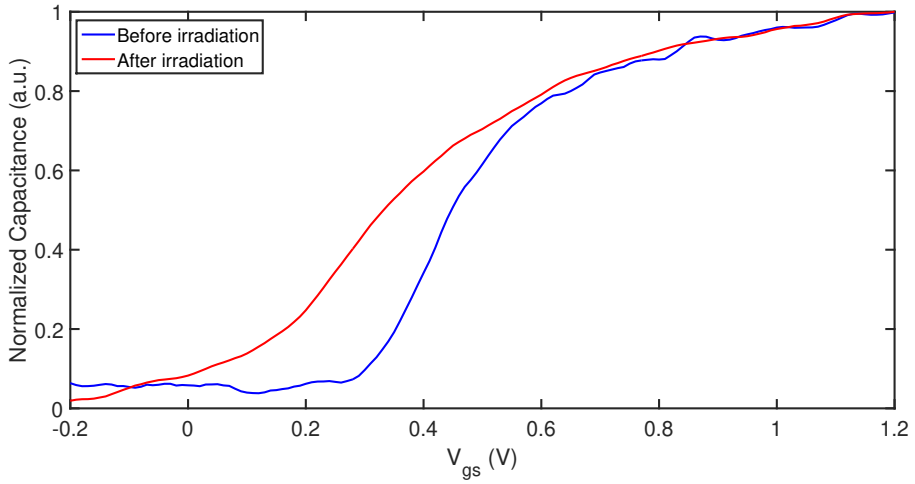


Figure 2.20: C-V measurement of a NMOS FDSOI transistor before and after irradiation.

The C-V measurements on MOSFET capacitor are commonly used for the extraction of the Equivalent Oxide Thickness (EOT) of the gate dielectric, the interface trap density (D_{it}), the fixed oxide charge density (Q_{ox}), and the doping-level [103]. A method widely used to characterize FDSOI devices is the derivative of the gate-to-channel capacitance as a function of gate voltage $C_{gc}(V_{gs})$. This technique can be employed to extract the V_{th} on both, NMOS and PMOS transistors. The V_{thn} and V_{thp}, are determined from the peak location on the curves obtained before irradiation, as shown on Figure 2.21.

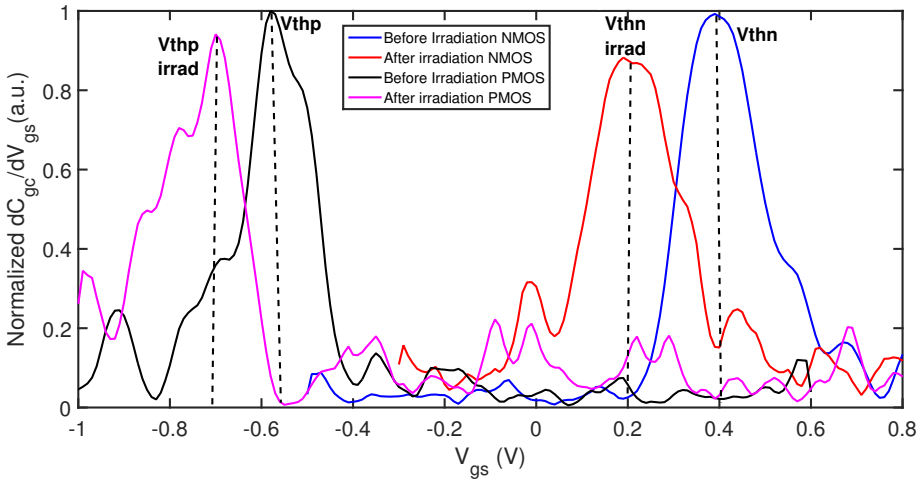


Figure 2.21: Threshold voltage extraction of NMOS and PMOS transistors.

Then, the flat-band voltage V_{FB} can be obtained by calculating the mean value between NMOS and PMOS devices as follows [155, 156]:

$$\frac{V_{tn} + V_{tp}}{2} = V_{FB} + \frac{Q_d}{C_{ox}} \tag{2.43}$$

Where $Q_d = qN_a t_{si}$ is the depletion charge across the channel.

This term is negligible for low-doped channels. As can be seen in Figure 2.21, the peak corresponding to V_{th} shifts negatively with increasing TID levels. This has a direct impact on V_{FB} that also shifts negatively. From the V_{FB} degradation, one can estimate N_{ot} for various applied TID steps as:

$$\Delta V_{FB} = \frac{Q_{ot}}{C_{ox}} = \frac{qN_{ot}t_{ox}}{C_{ox}} \tag{2.44}$$

2.5.3 Split C-V method

The split C-V method has been largely used in recent years to characterize FDSOI transistors [155, 157]. This characterization technique uses the C-V curve when it passes from accumulation to inversion at a determined frequency for several steps of front or back gate voltage. The front gate-to-channel capacitance (C_{gc}) is plotted for several values of V_{bg} as in [155] and is used to extract the parameters of the front transistor. On the other hand, the same procedure is used to obtain the gate-to-bulk capacitance C_{gb} and then to extract parameters related to the back transistor. The combination of both measurements allows the extraction of electrical and physical parameters such as substrate gate oxide, BOX, silicon thicknesses [158], the doping level, and the threshold voltage [157, 159].

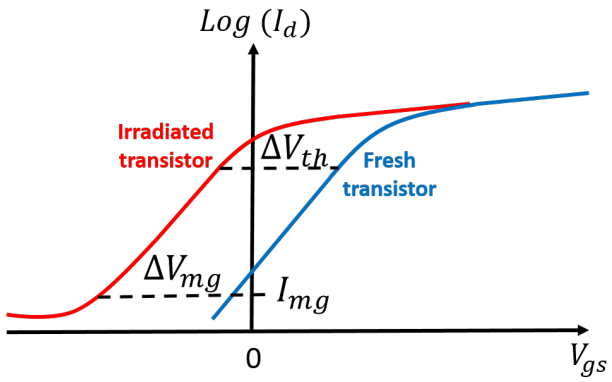


Figure 2.22: N_{ot} and N_{it} separation method.

I-V Methods

The amount of charges trapped in the oxides and interfaces can be estimated from the comparison of I-V curves at different TID levels. An important and practical reference is the one proposed by McWorther in [160] where the contributions of N_{ot} and D_{it} can be separated using I-V measurements. In this method, N_{ot} is calculated by taking into account the difference of mid-gap voltages ΔV_{mg}. The estimation of N_{it} is based on the assumption that bands are bent from mid-gap to threshold, then an increasing number of acceptor interface traps fall below the Fermi level and become negatively charged. This fact stretches out the subthreshold-current curve between

mid-gap and threshold. So, N_{it} is determined from the difference of $V_{th} - V_{mg}$ as can be observed in Figure 2.22.

For the processing of experimental data and parameter extraction, we will focus on the use of I-V curves. In particular, the extraction of V_{th} will be carried out with the Y-function. In the same way, the transport parameters such as low-field carrier mobility and degradation parameters will be extracted. In the frame of this thesis, the estimation of N_{ot} and D_{it} based on I-V measurements will be carried out as follows:

1. We extract the subthreshold-slope (SS) of each curve, before and after irradiation at low V_{ds}. A series of SS values will be obtained: $SS_0, SS_{irrad_1}, SS_{irrad_2}$,..., SS_{irrad_n} as seen in Figure 2.23.

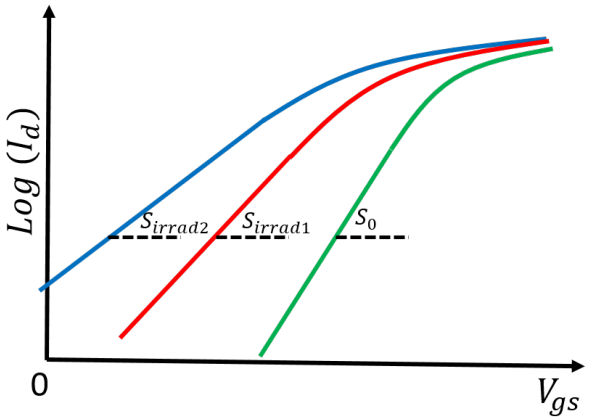


Figure 2.23: N_{ot} and N_{it}t separation method.

2. We determine the density of interface trapped charges as:

$$\Delta D_{it} = \frac{C_{ox}}{qkT(ln10)}(S_{irrad_n} - S_0) \tag{2.45}$$

3. In order to determine the contribution of the interface trapped charges to the threshold voltage shift ΔV_{it}, we assume a uniform distribution along the GAP of the silicon channel ($E_{gSi} = 1.12\ eV$). Next, we determine the density of charges per cm^2:

$$\Delta N_{it} = 1.12 D_{it} \tag{2.46}$$

4. We determine the voltage contribution of the interface trapped charges as:

$$\Delta V_{it} = q\frac{\Delta N_{it}}{C_{ox}} \tag{2.47}$$

5. As explained in Chapter 1, the total ΔV_{th} induced by the TID is due to the contributions of of charges trapped in the oxide volume and at the interface, respectively, so we can write $\Delta V_{th} = \Delta V_{ot} + \Delta V_{it}$. Knowing ΔV_{it}

and by properly extracting ΔV_{th}, we can estimate ΔV_{ot} as:

$$\Delta V_{ot} = \Delta V_{th} - \Delta V_{it} \tag{2.48}$$

It should be mentioned that N_{ot} is highly sensitive to the way V_{th} is extracted, so the extraction method must be properly chosen.

6. Finally, N_{ot} can be estimated as:

$$\Delta N_{ot} = \frac{q \Delta V_{ot} C_{ox}}{t_{ox}} \tag{2.49}$$

2.6 Conclusion of the chapter

After the studies carried out in this chapter, a correct understanding of the physical phenomena that ionizing radiation induces in the electrical parameters of MOSFETs, particularly in FDSOI ones, appears to be necessary to predict a possible failure in the device operation. Likewise, the extraction of the electrical characteristics of the tested technology is necessary to be able to quantify and consequently model these degradation. The recovery methods mentioned in this chapter have some advantages over the classical methods. The ability to regenerate a component after being subjected to radiation can extend its lifetime during a mission in radioactive environments. However, thermal annealing cycles can cause degradation when applied to electronic devices repeatedly. On the other hand, the coupling effect between the two gates of the FDSOI transistors is a great advantage that can be exploited to compensate for the negative shift of V_{th} induced by TID without degrading the reliability. The combined use of these two methods is advantageous to increase the resistance to TID of the FDSOI technology.

Chapter 3

Modeling of radiation effects and regeneration on FDSOI MOSFET devices

Physical models used by simulation tools must be accurate and capable of reproducing the behavior of electronic devices under all conditions. These models can be incorporated into compact models for their use with commercial circuit simulators, thus enabling the evaluation of a design's for predicting possible long-term failures. In this thesis, we have developed models that take into account the effect of TID on FDSOI devices and the effect of thermal annealing on the regeneration of radiation induced degradation. In this chapter, first we present simulation tools used in this thesis and that helped to validate the developed models. Then, we describe the proposed models including oxide trapping charges and interface charges modeling and their effects on threshold voltage degradation of FDSOI transistors.

3.1 Simulation tools

The great advance in computer performance has resulted in the systematic use of numerical methods to solve physical problems that seemed impossible decades ago. This fact has allowed the development of *Computer-Aided Design* (CAD) tools, such as *Technology CAD* (TCAD) or the *Simulation Program with Integrated Circuit Emphasis* (SPICE) in the electronics domain, which are of great help when simulating complex devices and circuits. These tools solve the physical equations related to the operation of the devices taking into account a series of input parameters. TCAD simulation is based on a method of finite element resolution of differential equations describing the transport of charge carriers and their interaction with the crystal lattice of semiconductors. To find a solution to the transport equations of any geometry, the area or volume must be divided into rectangular, triangular, prismatic

or pyramidal elements small enough that the solution in this local domain can be approximated by a polynomial. All the elements covering the simulated surface or volume constitute a mesh. In addition, TCAD can provide information for optimizing the IC performance [161]. SPICE simulates the electrical behavior of a circuit by taking into account compact models of components. From a netlist detailing the circuit to be simulated, and applying Ohm's and Kirchhoff's laws, SPICE creates a set of nonlinear algebraic differential equations represented in matrix form. Solving these equations is done iteratively using numerical integration methods.

As the device densities are growing exponentially, fundamental physical limits are being approached and design constraints are becoming a serious issue. The conventional way of describing, designing, modeling, and simulating nanoscale semiconductor devices is no longer valid. As a consequence, TCAD is being challenged by a number of fundamental problems such as microscopic diffusion mechanisms, quantum mechanical transport, molecular dynamics, etc [162].

On the other hand, the design of ICs implies a simulation stage that must be precise enough to be able to predict the possible cases of operation of the circuits under all conditions. This has given rise to compact models that simulate the electrical operation of transistors and provide a bridge between the manufacturing process and circuit design [163]. Like TCAD models, compact models must be able to perform simulation under different stress mechanisms with high efficiency but they must be simple enough to be incorporated in circuit simulators and sufficiently accurate and useful to circuit designers [164]. The great challenge of compact models is also to simulate other physical phenomena that can affect the performance of electronic circuits such as high temperatures, radiation in addition to complex quantum phenomena (Figure 3.1). Compact models generally include SPICE-like parameters obtained from the device's electrical behavior. Their parameters thus need to be carefully estimated and calibrated to achieve acceptable model predictivity [165].

Different compact models have emerged over the years: Surface potential-based (PSP), charge-based and threshold-voltage-based models. Threshold voltage-oriented models have been used for decades to simulate the behavior of transistors. However, in recent years, this type of compact model has been displaced by PSP models. The motivation for switching to PSP models comes from the desire to increase the physical content of the compact model and subsequently make it more suitable for modeling advanced MOS devices including low-Vdd, analog and RF applications where traditional compact models are not compatible with the circuit design [166].

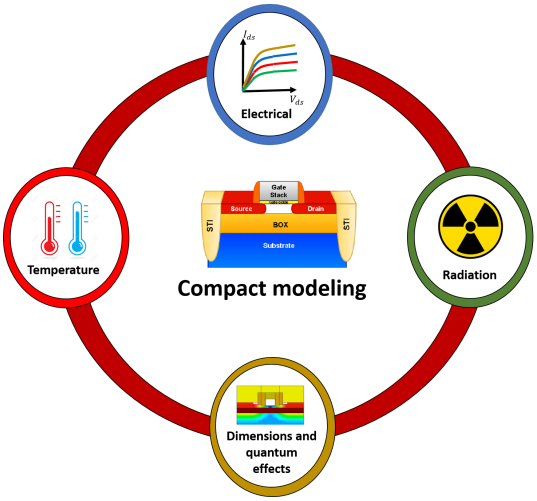
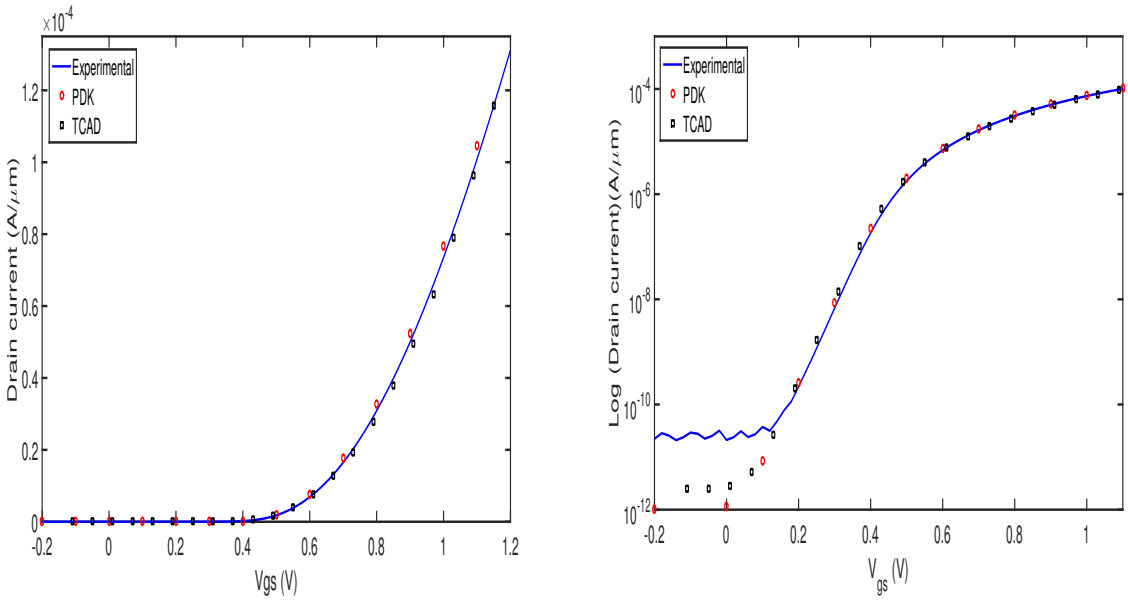


Figure 3.1: Challenges of compact modeling.

An important trend with the development of these models is the possibility to adapt them to simulate the effects of radiation on the electrical parameters of MOS devices and thus to predict degradation and a possible failure.

In this thesis, we will focus on an analysis with TCAD simulations to confirm some hypotheses corresponding to the performance degradation of FDSOI transistors subjected to ionizing radiation. Based on this, we will propose physical models that describe the behavior of charge trapping in oxides, which is the mechanism responsible for these degradation. Later, these simplified models will be implemented in a SPICE library in order to reproduce the physical phenomena linked to radiation and regeneration provided by annealing cycles.

For our study, we used the FDSOI model developed by CEA-LETI-LSM displayed in Figure 3.3 which is able to simulate the electrical characteristics of this device under different conditions, as will be shown below. We first made some simulations to verify the accuracy of the CAD tools used in this work, the I-V curves obtained from experimental measurements on a non-irradiated NMOS transistor were compared to those obtained from SPICE simulation using the 28nm FDSOI Process Design Kit (PDK) and then to the curves obtained with TCAD Synopsys sentaurus. Figure 3.2 shows a correct agreement between CAD tools, SPICE simulation and experimental results. The main characteristics of the transistor such as V_{th}, SS, I_{on} are reproducible with all simulation tools. The parameter that differs is the leakage current I_{off} (I_{ds} @ $V_{gs} = 0\ V$) which is higher for the experimental measurement, as can be observed in Figure 3.2(b). This can be caused by temperature variations, as well as the noise level that directly affects the subthreshold regime.



(a) $I_{ds}(V_{gs})$. (b) $log(I_{ds}(V_{gs}))$.

Figure 3.2: Comparison between experimental measurements, a PDK SPICE simulation and TCAD simulation.

3.2 TCAD Simulation of TID effects on FDSOI transistors

To study the electrostatic disturbances that trapped charges produce on FDSOI structure, a series of TCAD simulations were performed using the structure showed in Figure 3.3.

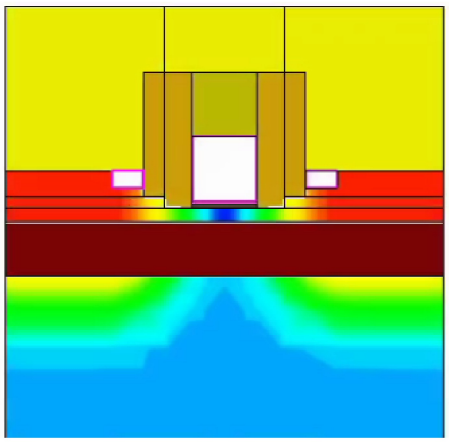


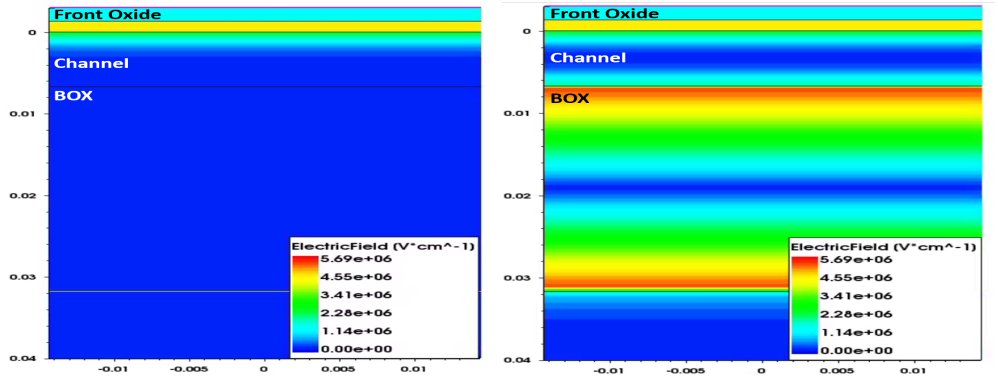
Figure 3.3: Cross-section view of a 28nm FDSOI model used in TCAD.

3.2.1 Effect of Oxide trapped charges N_{ot}

A separate analysis in the gate and BOX oxides was first carried out to observe the influence of N_{ot} on the degradation of V_{th}, the electric field (E), the electrostatic potential (Ψ) and the electron density across the channel

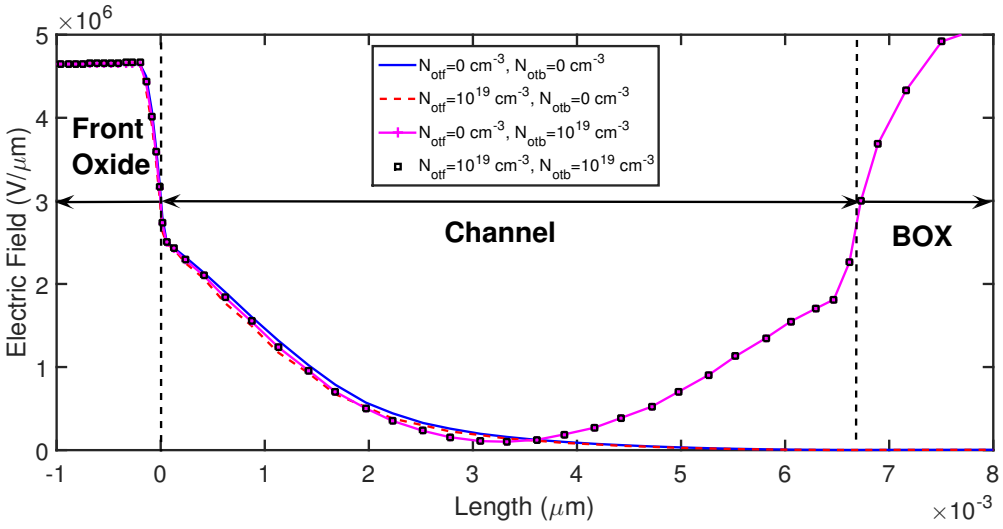
in the FDSOI structure. As previously reported in [167, 168], the number of charges trapped in the BOX produces an electric field that attracts the electrons towards the $Si - BOX$ interface inducing an inversion charge at the $Si - BOX$ interface, and thus a parasitic channel. This phenomenon modifies the back surface potential and, due to the electrostatic coupling between both interfaces, changes the threshold voltage of the transistor. For all analysis, we applied $V_g = 1\ V, V_d = 0.04\ V, V_s = V_b = 0\ V$. Likewise, all the analysis (profiles of electric field, potential and electron density) was obtained in the middle of the studied FDSOI structure ($x = 0$).

- **Effect on the electric field.** As analyzed in chapter 2 of this thesis, the inclusion of trapped charges in the oxides disturbs the behavior of the electric field in the three regions described, i.e. the front oxide, the intrinsic silicon layer where the channel is formed, and the BOX. Figure 3.4 shows the result of simulations made with four extreme cases when applying $N_{ot} = 10^{19}\ cm^{-3}$ in the oxide layers, simultaneously or separately. In (a) where no N_{ot} in the oxides are set, the electric field through the oxides remains undisturbed and follows perfectly the Poisson's equation calculated in Chapter 2. The formation of the front channel is governed by the front gate biasing and the electric field through the BOX is sensibly equal to 0. In (b) the inclusion of charges in both oxides leads to a disturbance of the electric field throughout the entire SOI structure. We observe that a parasitic channel in the $Si - BOX$ interface is induced by the electric field generated by N_{otb}. In the region corresponding to the BOX, the electric field is slightly increased. In (c) the vertical profile of electric field is plotted in the middle of the channel area, where $x = 0$ represents the the $Si - SiO_2$ interface and $x = 6.7 \times 10^{-3}\ \mu m$ correspond to the $Si - BOX$ interface. The region corresponding to the front oxide shows a small change due to the strong density of N_{ot}. A discontinuity at the $Si - SiO_2$ interface, is observed due to the change in permittivity in the materials. On the other hand, it is observed that the high concentration of N_{otb} distorts the electric field in the intrinsic silicon layer in the region above 4 nm, this fact is consistent with the formation of the parasitic channel responsible for the negative ΔV_{th} of the transistor.



(a) No N_{ot}.

(b) $N_{otf} = N_{otb} = 10^{19}\ cm^{-3}$.



(c) Electric Field across the channel.

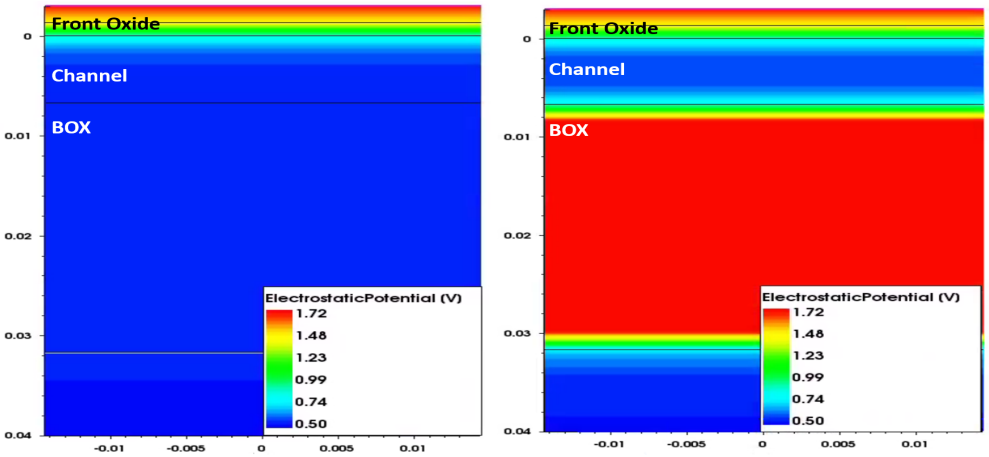
Figure 3.4: Effect of N_{ot} on the absolute value of the electric field in a 28nm FDSOI transistor.

- **Effect on the electrostatic potential.** Likewise, the electrostatic potential of the structure was analyzed under the same conditions. Figure 3.5(a) shows the structure without any trapped charge, that is, operating under ideal conditions. Figure 3.5(b) shows the device after including N_{ot} charges in both oxides. We observe that the electrostatic potential of the BOX is drastically increased. In (c) we clearly observe the relationship that exists between the electric field the electrostatic potential observed in Figure 3.4(c), and which is given by the equation:

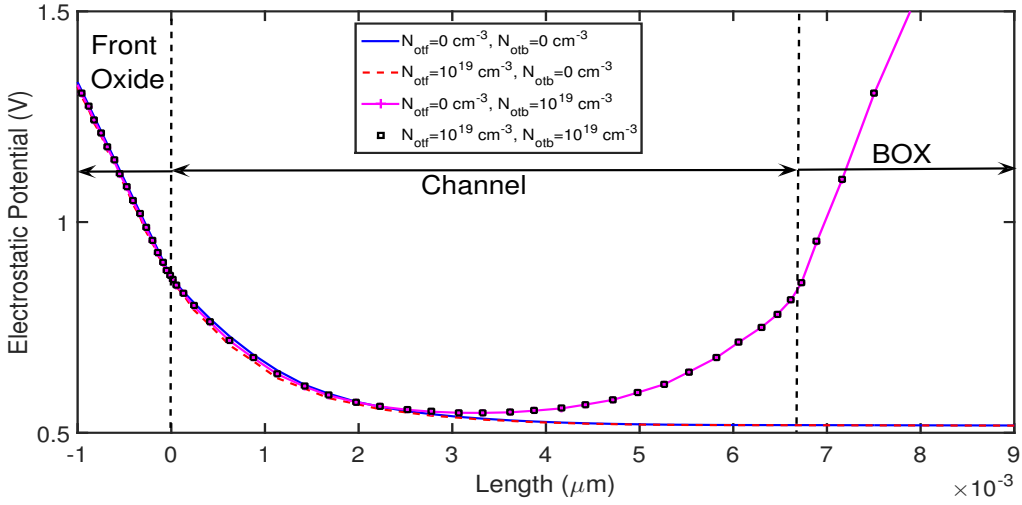
$$E = -\nabla V \tag{3.1}$$

We noticed that the increased electrostatic potential is mainly due to the contribution of charges trapped in the BOX. The contribution of N_{otf} remains negligible due to the thin oxide. Such an increase modifies the potential of the front surface which impacts the threshold voltage of the transistor. As previously mentioned, the contribution of N_{otf} is negligible due to the thin oxide thickness. Then, due to the electrostatic coupling be-

tween both interfaces, a change in the back surface potential induces a change in the front surface potential, and as a consequence a shift in the threshold voltage.



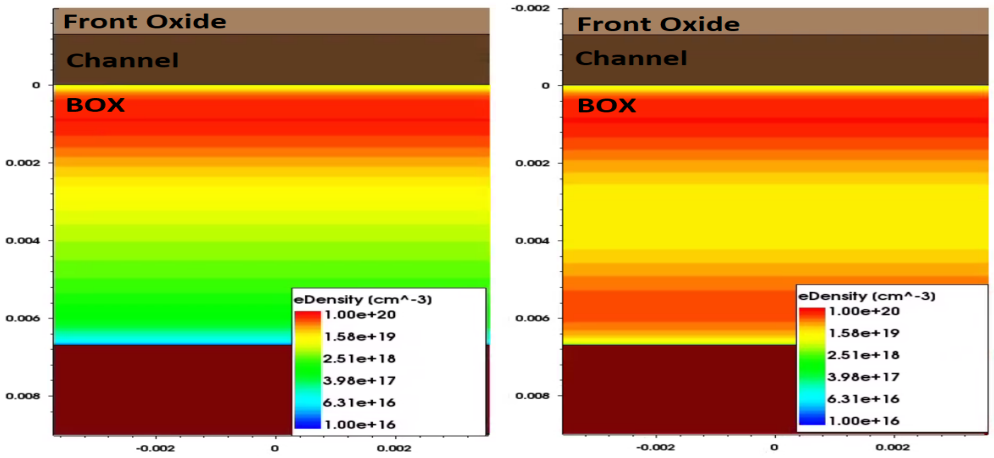
(a) No N_{ot}. (b) $N_{otf} = N_{otb} = 10^{19}\ cm^{-3}$.



(c) Electrostatic potential across FDSOI structure.

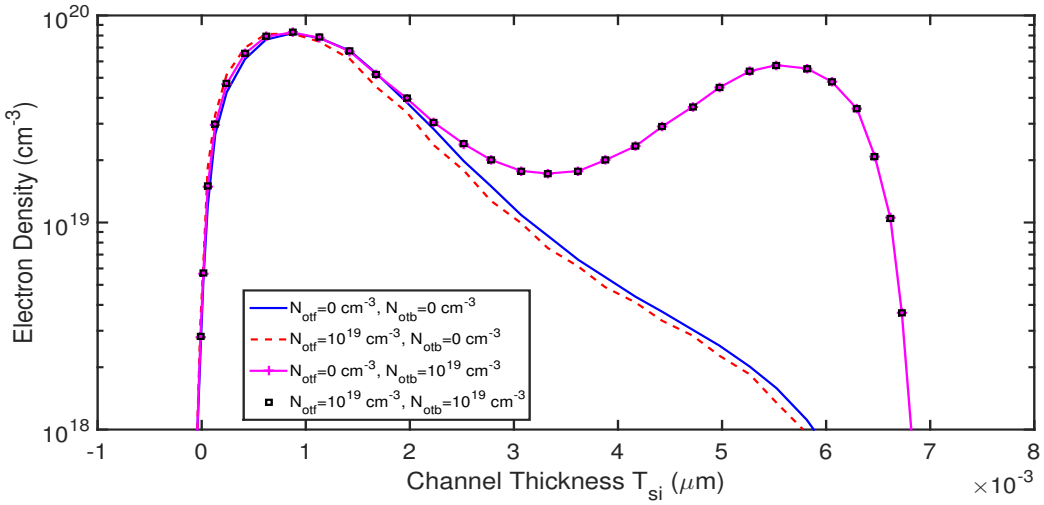
Figure 3.5: Effect of N_{ot} on the electrostatic potential in a 28nm FDSOI transistor.

- **Effect on the electron density.** Figure 3.6 shows the effect of N_{ot} on the electron density in the channel. In (a) the FDSOI transistor has not been irradiated, and so there are no charges trapped in its oxides. The front channel is induced by the voltage applied to the gate. In (b) the transistor has been irradiated and the charges trapped in the oxides disturb the electrostatic properties of the device. The high increase of N_{ot}, and especially in the BOX, induces a parasitic channel, which is clearly observed in (c) where we see that increasing N_{otb} attracts carriers to the $Si - BOX$ interface and a back-channel is formed by the electric field produced by N_{otb}.



(a) No N_{ot}.

(b) $N_{otf} = N_{otb} = 10^{19}\ cm^{-3}$.



(c) Electron density across the channel.

Figure 3.6: Effect of N_{ot} on the electron density in a 28nm FDSOI transistor.

Figure 3.7 presents the $I_d(V_{gs})$ characteristics of a NMOS transistor with different combinations of N_{otf} and N_{otb}. We can observe that the charges trapped in the gate oxide have almost no effect on the negative threshold voltage shift, then we can conclude that the N_{otb} is the main responsible for the V_{th} shift of an irradiated FDSOI transistor.

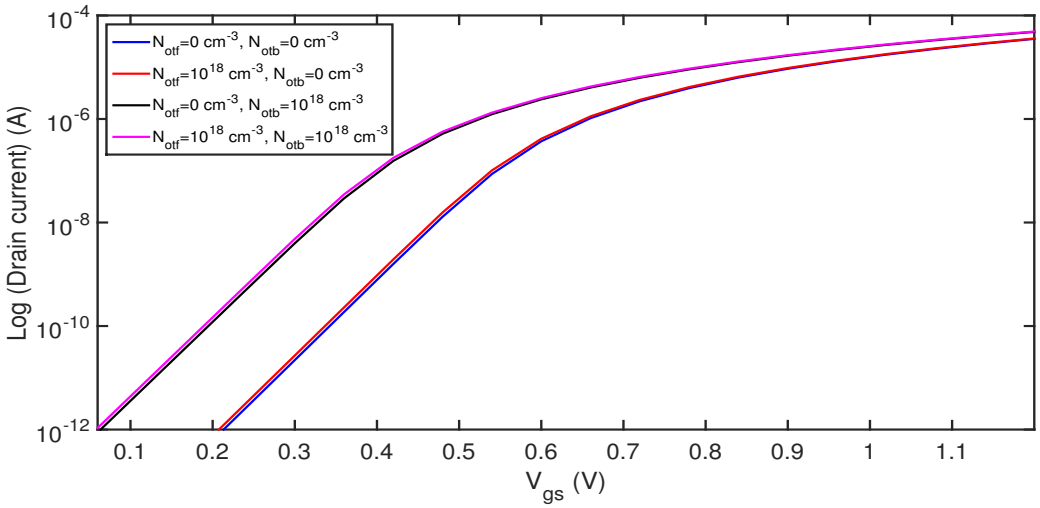


Figure 3.7: $I_d(V_{gs})$ curve of an NMOS transistor for different combinations of N_{otf} and N_{otb}.

3.2.2 Effect of interface trapped charges

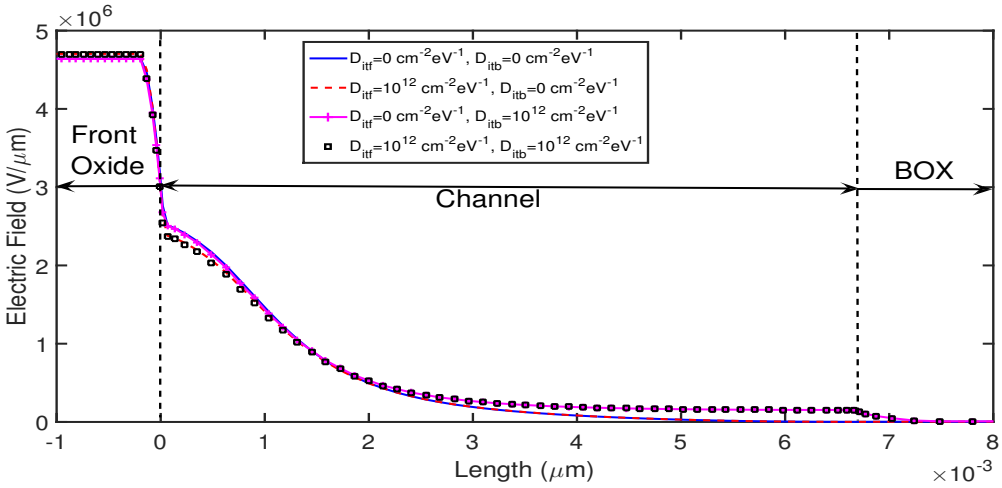
To analyze the impact of trapped charges on the $Si-SiO_2$ and $Si-BOX$ interfaces, a series of TCAD simulations was carried out. Four extreme cases were simulated summarized in Table 3.1. Those values of D_{it} correspond to severely degraded interfaces, i.e. $D_{it} = 1 \times 10^{12}\ eV^{-1}cm^{-2}$.

Table 3.1: Different analyzed D_{it} cases.

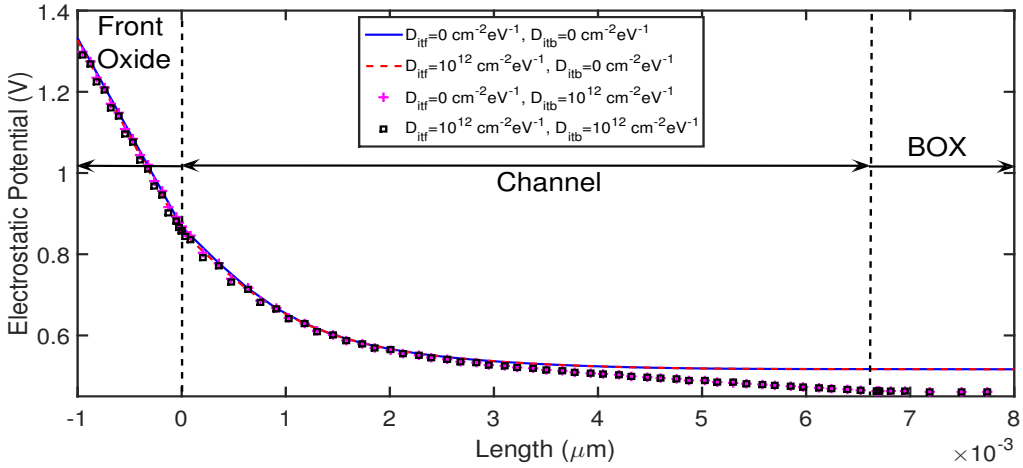
$D_{itf}(cm^{-2}eV^{-1})$	$D_{itb}(cm^{-2}eV^{-1})$
0	0
0	10^{12}
10^{12}	0
10^{12}	10^{12}

Figure 3.8 shows the effect of D_{it} (at both interfaces) on the electric field, the electrostatic potential, and the electron density in the conduction channel. We notice that a high D_{it} impacts the surface potential of the $Si-BOX$ interface which has an immediate effect on the surface potential of the $Si-SiO2$ interface. As reported in [169] the number of trapped holes becomes sufficiently large to create an electrostatic barrier near the interface that can prevent other mobile particles (holes and protons) from reaching the interface.

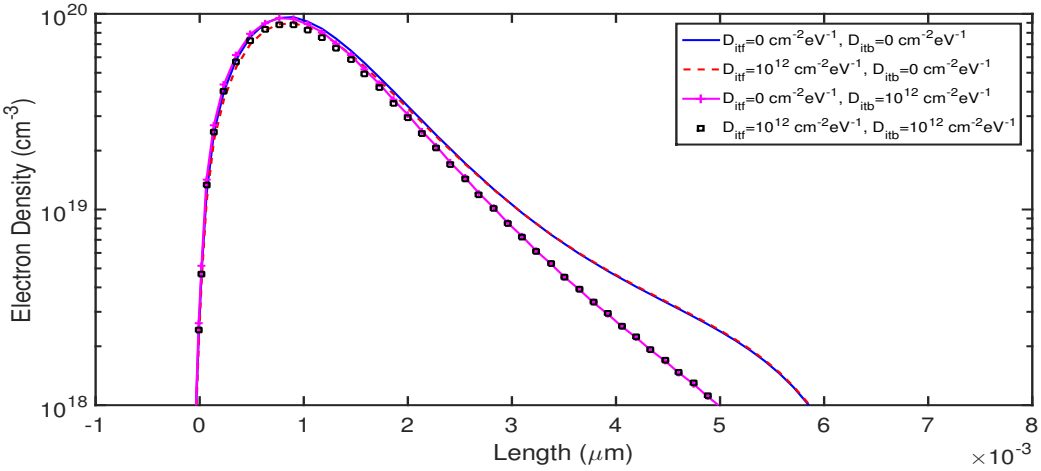
In (a) the absolute value of the electric field is constant in the region of the front oxide. At $x = 0$, the effects of different applied values of D_{it} are shown. We can see that a high D_{it} applied at an interface decreases the electric field in this area. This results from the interaction of the charges trapped at both interfaces with the electrons in the channel, producing recombination centers, leading to a slightly drop of the electrical field in the regions close to the interfaces.



(a) Electric Field.



(b) Electrostatic potential.



(c) Electron density in the channel.

Figure 3.8: Effect of interface trapped charges on a FDSOI device.

In (b) a similar behavior is observed, due to the relationship between the electric field and the potential. In particular, the electrostatic potential falls in the region close to the $Si - BOX$ interface, which is explained, as in the case of the electric field, by the interaction of the trapped charges with the carriers close to that region. As the rate of recombination is high, this produces a lower density of carriers near the interfaces, which causes the potential to fall in that region.

In (c) we can see that applying a D_{itb} decreases the electron density. This confirms the conclusions drawn from the two previous curves. The interface traps capture the channel carriers during the device operation. Therefore, there are fewer conducting carriers in the channel resulting in a deterioration of the device performance. Actually, when tuning the gate potential, a part of the voltage drop is consumed to modulate the charges trapped at the interface which reduces the number of free carriers in the channel controlled by the gate.

We apply all different cases including $D_{itf} = D_{itb}$ of $10^{13} cm^{-2} eV^{-1}$ to clearly observe the effect of D_{it} on the I-V curve of the transistor. As can be seen in Figure 3.9, these phenomena induce a progressive positive shift of the I-V curve as the level of D_{it} increases at both interfaces. This effect easily observed, as opposed to the effect of the charges trapped in the volume of the oxides.

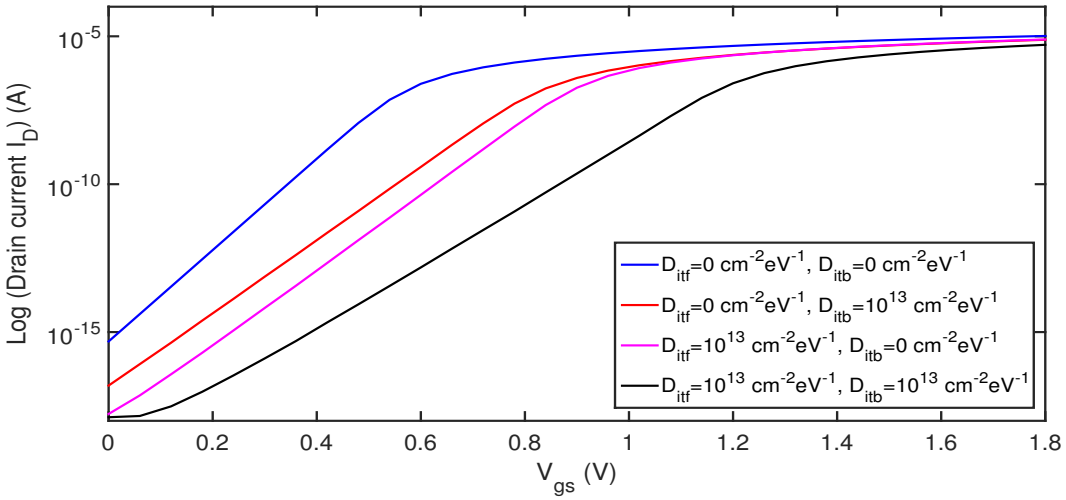


Figure 3.9: $I_d(V_{gs})$ with the only influence of D_{it}.

3.2.3 Subthreshold slope comparative

In order to demonstrate the influence of the trapped charges at each interface, we compared the values extracted from TCAD, the values calculated from the equation 3.2, and a series of values extracted experimentally in irradiated transistors. For this, we use the experimentally extracted D_{it} in a NMOS device $W = L = 1\ \mu m$ as input parameters. We consider $C_{itf} = C_{itb} = qD_{it}$.

$$SS = \frac{kT}{q} ln10 \frac{dV_{gf}}{d\Psi_{sf}} = \frac{kT}{q} ln10[(1 + \frac{C_{si}}{C_{ox}} + \frac{C_{itf}}{C_{ox}}) - \frac{\frac{C_{si}^2}{C_{ox}C_{box}}}{(1 + \frac{C_{si}}{C_{box}} + \frac{C_{itb}}{C_{box}})}] \tag{3.2}$$

Figure 3.10 shows the evolution of SS with each level of D_{it}. As a reminder, an ideal SS is $60\ mV/dec$, that is, without taking into account the interface states. In this case, the slope shows an initial value of $64\ mV/dec$, which presumes a presence of initial interface states due to the manufacturing process. The evolution of both the experimental slope and those obtained with the SS and TCAD models show similar values. This confirms that the two interfaces have a direct effect on the subthreshold slope variation, so both should be taken into account when implementing a descriptive physical degradation model.

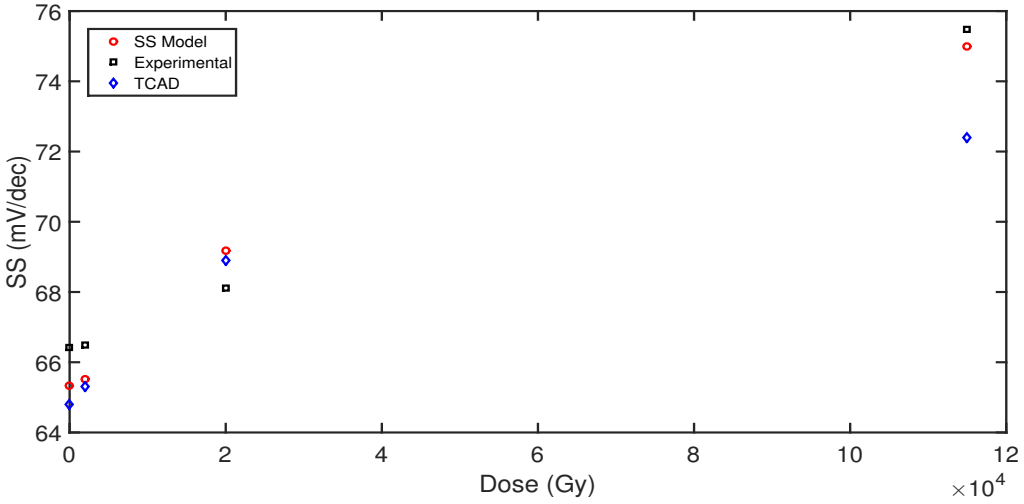


Figure 3.10: Comparison of experimental ans simulated subthreshold slope variation.

Table 3.2 shows the extracted D_{it} values, as well as the SS values.

Table 3.2: Subthreshold slope for NMOS $W = L = 1\ \mu m$.

TID	$D_{itf,b}$	SS Experimental	SS Model	SS TCAD
0	0	66,41	65,33	64,8
2 kGy	$5,14.10^{10}$	66,49	65,42	65,3
20 kGy	$1,17.10^{12}$	68,11	67,32	68,9
115 kGy	$3.29.10^{12}$	75.47	74,62	72,4

3.3 Physical Modeling of the radiation damage

Based on the conclusions arising from TCAD simulations, we propose an analytical model based on a set of physical equations able to describe of the radiation effects that affect the operation of FDSOI MOSFET devices and a model to describe the recovery of their electrical characteristics resulting from thermal annealing cycles.

The objective is to use these models with commercial SPICE simulators to reproduce and predict TID-induced degradation as well as progressive regeneration with each annealing cycle.

3.3.1 General description of oxide trapped charges N_{ot} model

In the literature, the modeling of trapped charges and its effects has been extensively investigated to describe the absorbed dose in a semiconductor device. These models are dose level or dose-rate-based, and they depend on the applications for which they are applied. For example, in [170] the oxide trapped charges model has been proposed following a trapping mechanism in a finite number of oxides defects. This allowed to predict the behavior of the degradations at high dose levels. In [171, 172, 173, 174] PSP FDSOI models taking into account radiation have been proposed, where the input parameters are the oxide and interface trapped charges (N_{ot} and D_{it} respectively). In [175, 176], the modeling of N_{ot} in the STI oxides was done to model the increase in leakage currents.

The dynamics of trapping-detraping in thick insulating oxides has been published in [177, 178, 179] for MOSFETs. The expected response for irradiated devices at high TID levels is shown in Figure 3.11. First, a quasi-linear rise of N_{ot} is observed, the slope of which represents the rate of charge trapping in the oxide. It is assumed that the oxide has a finite number of defects N. For high levels of TID, the charges created tend to occupy all the defects in the oxide leading to a saturation of trapped charges in the oxides. After the radiation process has ended, charges start to be detrapped, even at room temperature. And when applying annealing at a high temperature, the detrapping rate will grow exponentially following an Arrhenius law.

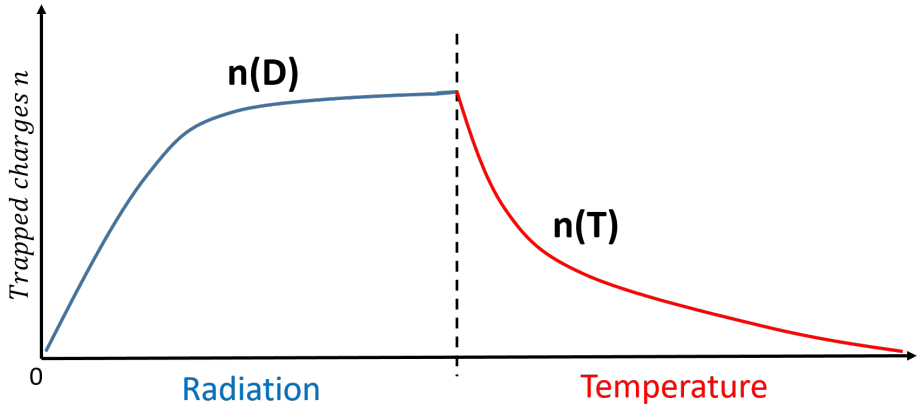


Figure 3.11: Expected response of trapped charges in MOSFET oxides during irradiation and annealing.

We have been inspired by these previous works to model the trapping-detrapping dynamics of N_{ot}, therefore, we propose a linear input-output or generation-regeneration differential equation expressed as:

$$\frac{dn(D)}{dD} = Input - Output \tag{3.3}$$

Where $n(D)$ represents the number of trapped charges as a function of the total dose. First of all, we will analyze the effects of trapped charges without taking into account the regeneration by making the following assumptions:

- A finite oxide volume.
- A finite number of available defects N.
- The oxide trapped charges saturates when $n(D) = N$.
- A negative shift of the threshold voltage is due to the holes trapped in the insulating oxides.

The model proposed by following the input-output analogy can be expressed as:

$$\frac{dn(D)}{dD} = \lambda(N - n(D)) - \sigma n(D) \qquad n(0) = 0 \tag{3.4}$$

with:

- λ the generation coefficient given by λ=$g_0 t_{ox} f_y(E) \sigma_h$.
- N the number of available traps in the oxide.
- $n(D)$ the number of trapped charges as function of total dose.
- $\sigma = Ae^{-\frac{E_{act}}{kT}}$ the Arrhenius constant.

First, we will analyze the dynamics of trapping of charges without taking into account the influence of temperature, then equation 3.4 becomes:

$$\frac{dn(D)}{dD} = \lambda(N - n(D)), \quad where \quad n(0) = 0 \quad and \quad n(\infty) = N. \tag{3.5}$$

The solution of this linear differential equation is:

$$n(D) = N(1 - exp(-\lambda D)) = N(1 - exp(-g_0 t_{ox} f_y(E) \sigma_h \ D)) \tag{3.6}$$

Brief description of the parameters

- **Electron-hole pairs generation** g_0

  The energy required to ionize a material depends directly on its bandgap E_{gap}. The number of electron-hole pairs (ehp) generated in a material per dose unit is also dependent on the material density. Hence, the electron-hole pair generation factor is expressed as the ratio of the density of the material (ρ) to the pair's creation energy (W) [48]:

  $$g_0 = \frac{\rho}{W} \tag{3.7}$$

  The values values of g_0 reported in the literature for SiO_2 vary from: $7,6.10^{14}\ cm^{-3}Gy^{-1}$ to $8,2.10^{14}\ cm^{-3}Gy^{-1}$ [48, 134, 170, 180].

- **Charge yield** $f_y(E)$

  After their creation in the insulating oxide, most of electron-hole pairs will recombine immediately. The non-recombined electrons will move towards the gate while the holes jump to the $Si - SiO_2$ interface[48]. As previously mentioned, the response of MOSFET transistors to radiation strongly depends on the biasing applied to the device. Some empirical equations have been proposed by different authors in order to determine the amount of non-recombined charges in an oxide layer [4, 178]. It is important to mention that all these functions are empirical functions and depend on the energy, type of radioactive source, and the electric field applied to the device. The recombination function is generally expressed as [181]:

  $$f_e(|E|) \approx \left(\frac{|E|}{|E| + E_0}\right) \tag{3.8}$$

  With $E_0 = 0.55\ MV/cm$ the threshold field constant [170, 179]. This value may change depending on the experimental conditions. Several values of E_0 have been proposed in [4, 182, 183, 184], ranging from $0.2\ MV/cm$ to $0.65\ MV/cm$. Other charge yield functions have been also proposed for ^{60}Co and X-rays sources [48, 178, 179, 185, 186]. Figure 3.12 shows a comparison between the charge yield functions proposed by different authors, where the variations depend on the experimental conditions in which the devices were irradiated. Therefore, the applied electric field during irradiation is a factor to be taken into account in the proposed physical model.

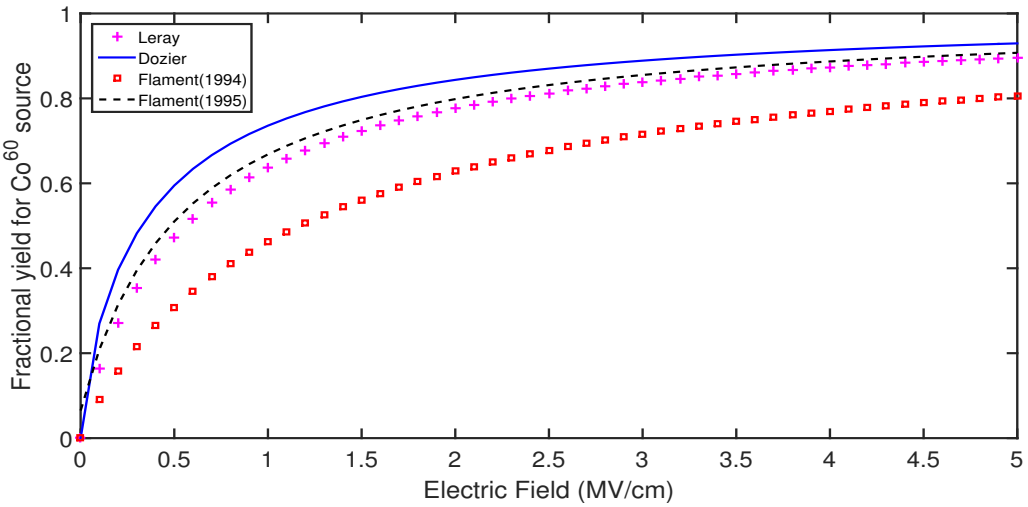


Figure 3.12: Various charge yield functions used for a ^{60}Co irradiation.

- **Capture cross-section σ_h**

  The capture cross-section σ_h expresses a critical area perpendicular to the flow of carriers where the defect can capture a carrier. The initial charge of the defect and the sign of the captured carrier determine the nature of the capture cross-section. In the case of an electron, if the defect is positively charged, it is Coulombian attractive, so its capture cross-section is large: $10^{-14}\ cm^{-2} < \sigma_h < 10^{-12}\ cm^{-2}$. On the other hand, if the defect is negatively charged, it is Coulombian repulsive and its capture section is small: $10^{-22}\ cm^{-2} < \sigma_h < 10^{-18}\ cm^{-2}$. If the defect is neutral, it can capture an electron or a hole and its capture cross-section is medium: $10^{-18}\ cm^{-2} < \sigma_h < 10^{-14}\ cm^{-2}$. In the case of SiO_2, most of these defects are neutral [187, 188].

3.3.2 Parameters used for the N_{ot} dynamics

From the TCAD simulations, we can conclude that the trapped charges in the BOX are mainly responsible for the threshold voltage shift of both NMOS and PMOS devices. As a consequence, the contribution of N_{ot} of the front oxide is negligible. Therefore, the threshold voltage shift due to the oxide trapped charges ΔV_{ot} can be expressed as:

$$\Delta V_{ot} = \Delta V_{Notf} + \Delta V_{Notb} \approx \Delta V_{Notb} \tag{3.9}$$

and then the equation 3.6 becomes:

$$n(D) = N(1 - exp(-g_0 t_{box} f_y(E)\sigma_h\ D)) \tag{3.10}$$

Table 3.3 summarizes the parameter values that we used for modeling the charge trapping in the volume of insulating oxides. The parameters described in this table were defined based on the values found in the literature [48, 69, 74]. The values N and $f_y(E)$ that are technology dependent, are fitting parameters extracted from our experimental data.

Table 3.3: Parameters used for N_{ot} model.

Parameter	Value
g_0	$8,2\ 10^{14}\ cm^{-3}\ Gy^{-1}$
t_{ox}	$1,8\ nm$ or $2,8\ nm$ (GO2)
t_{box}	$25\ nm$
σ_h	$1.10^{-13}\ cm^2$
$f_y(E)$	Fitting
N	Fitting

Figure 3.13 shows the dynamics of charge trapping in the volume of insulating oxides for high levels of TID on the experimental data of a PMOS transistor $W = 0.3\ \mu m$, $L = 0.03\ \mu m$. As described in the state of the art, for low TID levels, the growth of trapped charges is almost linear. Many models developed for low dose-rates and low levels of TID are based on linear growth approximation [48, 189]. However, when MOSFET transistors are exposed to high levels of TID, their insulating oxides are prone to saturate making these models less accurate.

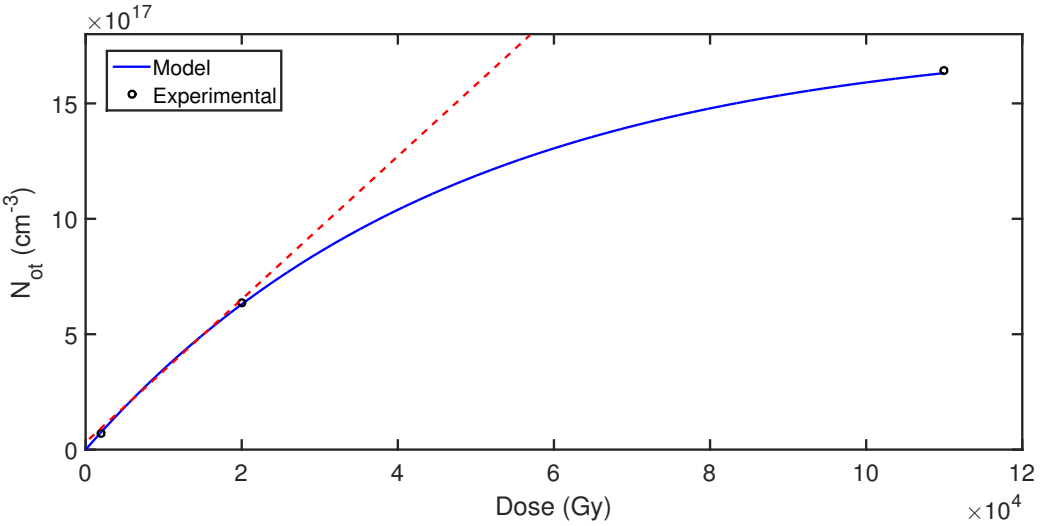


Figure 3.13: Dynamics of oxide trapped charges density N_{ot} at high levels of TID. Comparison between experimental data of a PMOS transistor $W = 0.3\ \mu m$, $L = 0.03\ \mu m$ [this work] and the model [Eq. 3.10]

3.3.3 General description of interface trapped charges D_{it} dynamics

As previously explained, charges trapping at the interfaces is a time-dependent phenomenon. Charges are trapped on the defects present at the interface such as dangling bonds inherent in the junction between the amorphous structure of SiO_2 and the crystalline structure of Silicon. Their formation is a consequence of the interaction of the

holes and hydrogen-containing defects (DH centers) leading to the release of a proton (H^+) [190]. As reported in [191] this reaction is coupled with proton transport and can be represented by the proton continuity equation expressed as [190]:

$$\frac{dn_{H^+}}{dt} = -\frac{1}{q}\left(\frac{dJ_{H^+}}{dx} - g_0 f_y N_{DH}\sigma_{DH}D'x\right) \tag{3.11}$$

By integrating the equation 3.11 we obtain the proton current density JH^+ as:

$$JH^+ = qN_{DH}\sigma_{DH}D'g_0 f_y\frac{x^2}{2} \tag{3.12}$$

where:

- N_{DH} is the density of hydrogen defects in the oxide (DH centers).
- σ_{DH} is the capture cross-section of holes reacting with DH centers.
- x is the drift length of protons.

Different physical models that describe the dynamics of trap formation and the interaction with charges have been proposed in [169, 192] for bipolar junction transistor (BJT) and [170, 181, 190] for MOS devices. All of them are based on hole-hydrogen defect reaction coupled with proton transport [192]. Hence, this model is inspired by [181, 190], under the following hypotheses:

1. A finite number of interface defects N_{SiH}.
2. A high dose rate.
3. The DH centers are uniformly distributed in the oxide.
4. We assume that the P_b centers dominate over other positively charged defects at the interface.
5. Trapping of electrons in the oxide is neglected.
6. We neglect the recombination phenomena.

Then, considering that $\Delta N_{it} = \Delta P_b$, the differential equation that describes the evolution of N_{it} is given by:

$$\frac{dN_{it}}{dD} = D\ g_0\ f_y\ (N_{SIH} - N_{it})N_{DH}\sigma_{DH}\sigma_i\frac{x^2}{2} \tag{3.13}$$

where:

- N_{SIH}: Density of passivated bonds at the interface in cm^{-2}.
- σ_i: is the capture cross-section for interface traps cm^2.

Solving this first-order differential equation, the interface trapped charges can be expressed as follows:

$$N_{it}(D) = N_{SIH}(1 - exp(-g_0 f_y N_{DH} \sigma_{DH} \sigma_i \frac{x^2}{2})D) \tag{3.14}$$

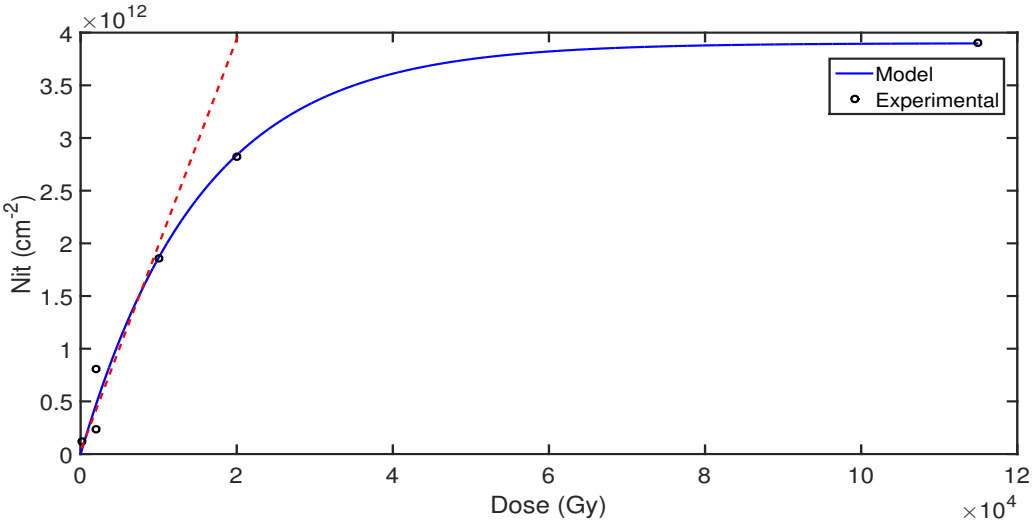


Figure 3.14: Dynamics of interface trapped charges. Comparison between experimental data of a PMOS transistor $W = 0.3\ \mu m$, $L = 0.03\ \mu m$ [this work] and the model [Eq. 3.14].

The evolution of D_{it} is shown in Figure 3.14 applied on the experimental data of a PMOS transistor $W = 0.3\ \mu m$, $L = 0.03\ \mu m$ of this work. The densities of hole trapping sites and DH centers used in the model are similar to what is reported in [190]. Table 3.4 summarizes the values of the parameters found in the literature [181, 190].

Table 3.4: Parameters used for N_{it} model.

Parameter	Value
g_0	$8,2\ 10^{14}\ cm^{-3}\ Gy^{-1}$
N_{SiH}	Fitting
N_{DH}	$1.5\ 10^{14}\ cm^{-3}$
σ_{DH}	$4\ 10^{-10}\ cm^2$
σ_i	$1.\ 10^{-13}\ cm^2$
x	$1.8\ nm$

3.4 Linear response of the N_{ot} and N_{it} models

We define a transition level of TID below which the behavior of phenomena related to TID, N_{ot} and D_{it}, can be considered linear. For the 28nm FDSOI technology, this critical level is around 10 kGy. These phenomena present an exponential behavior, therefore, for low levels of TID, the term $(1 - exp(-\alpha D))$ can be approached to αD. In this way, the proposed models corresponding to the equations 3.10 and 3.14 can be linearized, which leads to:

$$\begin{cases} N_{ot} = N g_0 t_{ox} f_y(E) \sigma_h \ D & \text{if } TID \leq 10\ kGy \\ N_{it} = N_{SiH} g_0 f_y N_{DH} \sigma_{DH} \sigma_i \frac{x^2}{2} D & \text{if } TID \leq 10\ kGy \end{cases} \tag{3.15}$$

3.5 Thermal regeneration modeling

The thermal regeneration model aims to determine and predict the regeneration rate of the electrical characteristics of FDSOI devices degraded by radiation. Our model is based on the hypothesis that the detrapping of charges is governed by the thermal front $\Phi_{thermal}$, defined in equation 2.32, which depends on the temperature of the applied cycle. Therefore, a given level of activation energy is reached by neutralizing or detrapping the charges having a lower energy. Hence, we propose a model that describes the detrapping of charges based on the following differential equation:

$$\frac{dn(T)}{dT} = -\sigma n(T) \tag{3.16}$$

where:

- σ is the Arrhenius constant.
- $n(T)$ is the number of trapped charges in the volume of the insulating oxides to be annealed.

We can solve this equation by using a separation of variables, leading to:

$$\frac{dn(T)}{n(T)} = -\sigma dT \tag{3.17}$$

To observe the influence of temperature in the equation, we express σ as a function of its temperature-dependent exponential form (Arrhenius constant).

$$\frac{dn(T)}{n(T)} = -Aexp(-\frac{E_{act}}{kT})dT \tag{3.18}$$

By integrating both sides of the equation we have:

$$\int \frac{dn(T)}{n(T)} = -\int_{T_0}^{T} Aexp(-\frac{E_{act}}{kT})dT \tag{3.19}$$

Then, the solution to this differential equation is given by:

$$n(T) = n_0 exp(-A(\int_{T_0}^{T} exp(-\frac{E_{act}}{kT})dT) \tag{3.20}$$

The general solution to the integral I in equation 3.20 is of the form $\int x^n e^{ax} dx = \frac{x^n e^{ax}}{a} - \frac{n}{a}\int x^{n-1} e^{ax} dx$. Then, in our case, the solution to this integral I is [193]:

$$I = \left[I_0 + \frac{k}{E_{act}} exp\left(-\frac{E_{act}}{kT}\right)\left[T^2 - \frac{2kT^3}{E_{act}} + \frac{6k^2T^4}{E_{act}^2} + ...\right]\right] \tag{3.21}$$

The terms subsequent to T^2 have a very small contribution to the value of the integral, therefore, considering that $T^2 >> \frac{2kT^3}{E_{act}} + \frac{6k^2T^4}{E_{act}^2} + ...$ we have an approximate solution to the integral given by:

$$I = \left[I_0 + \frac{k}{E_{act}} exp\left(-\frac{E_{act}}{kT}\right)\left[T^2\right]\right] \tag{3.22}$$

With I_0 the value of the integral at $T = T_0$. The complete development to solve this integral applied to our problem is given in Appendix B. So the detrapping dynamics for a given temperature T is given by:

$$n(T) = n_0 exp(-\left(\frac{A}{c}\right) T^2 \left(\frac{k}{E_{act}}\right) exp(-\frac{E_{act}}{kT}) + T_0^2 exp(-\frac{E_{act}}{kT_0})) \tag{3.23}$$

As was proposed in [141], for an irradiated device, the trapped charges are distributed on different energy levels, so for a multi-level model, we have:

$$n(T) = \sum_{i=1}^{n} n_{0(i-1)} exp(-\left(\frac{A}{c}\right) T_i^2 \left(\frac{k}{E_{acti}}\right) exp(\frac{-E_{acti}}{kT_i}) + T_0^2 exp(-\frac{E_{act}}{kT_0})) \tag{3.24}$$

Where T_i is the temperature of the i-th annealing cycle. This function becomes maximum when we approach an activation energy and a characteristic temperature. Therefore, the inflection point of the isochronous annealing curve corresponds to the characteristic temperature of the oxide. The inflection point are determined at the temperature for which $\frac{dn^2(T)}{dT^2} = 0$. The characteristic temperature is thus found as calculated in Appendix B, and is given as:

$$\frac{E_{act}}{kT*} = ln(\frac{akT*^2}{cE_{act}}) \tag{3.25}$$

Based on this detrapping model we propose a procedure for the extraction of activation energies as follows:

- We extract the densities of the charges trapped in the volume of the oxides as a function of each thermal annealing step.
- We plot the calculated function for the fixed values $A = 10^7\ s^{-1}$, k, the Boltzmann's constant, T the applied

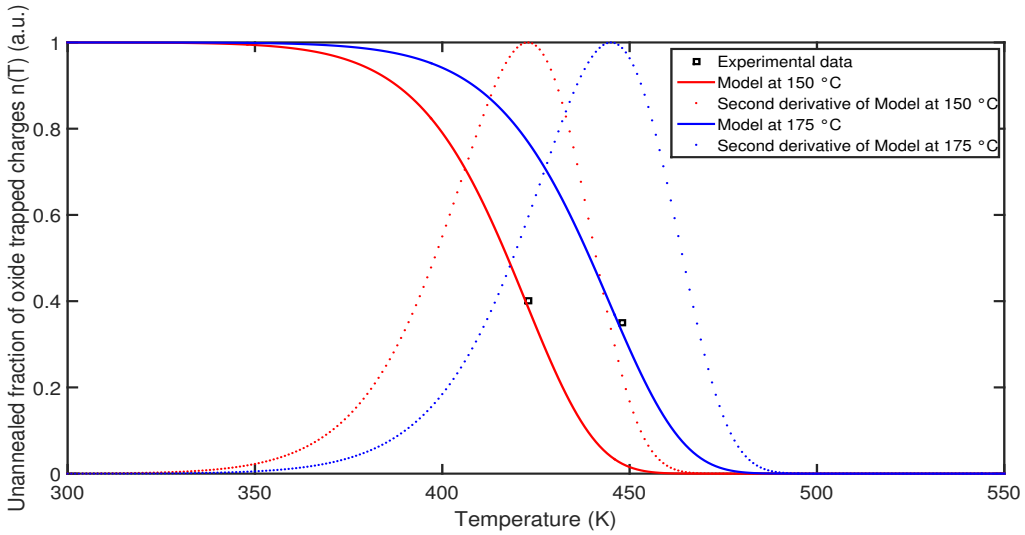


Figure 3.15: Annealing model applied to an irradiated transistor.

temperature in K, and n_{i-1} the charge density following stage $n-1$. For example, to extract the activation energy following the application of a thermal annealing step at 150 °C, we will take the density of trapped charges at 25 °C, and for annealing at 175 °C we will take the residual $n(T)$ after the annealing step at 150 °C.

- We vary the parameter E_{act} until the proposed function agrees with the experimental point. The result is a set of characteristic curves at each activation energy. Figure 3.15 shows the proposed model for extracting the activation energies after an annealing at 150 °C and 175 °C.

For practical uses, this activation energy extraction methodology will also be used to describe the regeneration of the electrical characteristics of the device that have been degraded by the charges trapped at the interfaces. In this way, equation 3.24 can be rewritten by introducing the terms N_{SiH} and N_{it}:

$$N_{it}(T) = \sum_{i=1}^{n} N_{SiH0(i-1)} exp(-\left(\frac{A}{c}\right) T_i^2 \left(\frac{k}{Ea_i}\right) exp(\frac{-Ea_i}{kT_i}) + T_0^2 exp(-\frac{E_a}{kT_0})) \tag{3.26}$$

3.5.1 Dynamic of annealing

In order to reproduce the dynamics of detrapping of charges, we use the time-temperature dependence previously explained. Starting from the fact that the detrapping phenomenon follows the Arrhenius law, we calculate the position of the thermal front which represents the expected activation energy level for a given couple of time-temperature annealing pair and a known frequency factor A. Thus, as obtained in equation 2.32, we have:

$$\Phi_{thermal} = E_{act}(eV) = kTln(A\tau) \tag{3.27}$$

To reach a level of around 1 eV, given a frequency factor $A = 10^7\ s^{-1}$, a temperature of 250 °C and a duration of 18 minutes are necessary. Figure 3.16 shows an application example using the parameters previously described. In this Figure, the activation energies extracted from the experimental data obtained in this work for 4 transistors can be observed (additional information regarding the characteristics of the transistors will be treated in chapter 4). From the time-temperature equivalence expressed in equation 3.27, we calculate the expected activation energy for a series of thermal anneals at 150 °C, 175 °C , 200 °C, and 250 °C (423 K, 448 K, 473 K, and 523 K). A similar evolution to the activation energies extracted experimentally in the devices is noticed. Thus, knowing the frequency factor and the duration of thermal annealing, one can calculate the expected activation energy for an irradiated device.

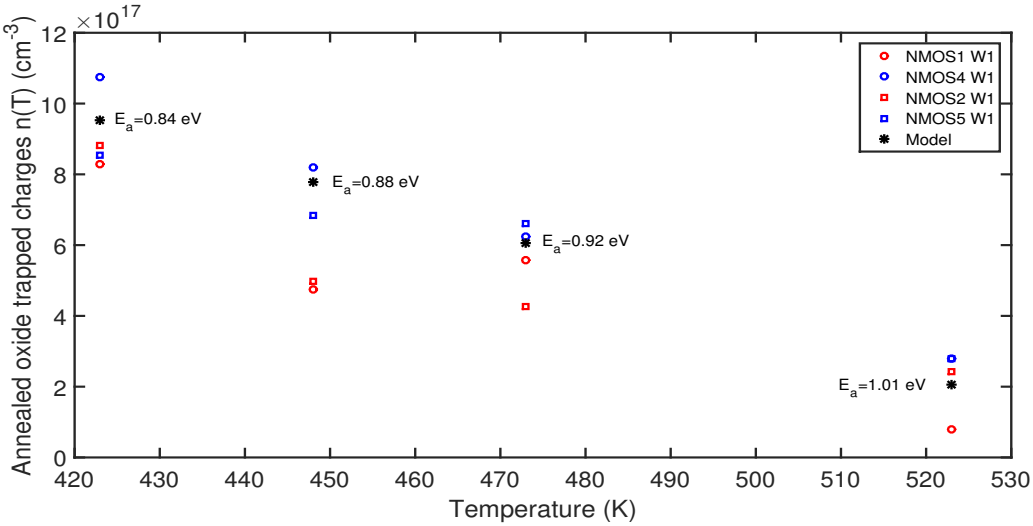


Figure 3.16: Evolution of the activation energy level with each thermal annealing cycle. Comparison between experimental data of extracted from NMOS transistors [this work] and the model [Eq. 3.27].

3.6 SPICE implementation of the physical models

As schematized in Figure 3.17 the proposed physical models were implemented using UTSOI2, a SPICE library developed by CEA-LETI [194, 195, 196]. These models were inspired from the TID model proposed in [173] where the input parameters are N_{ot} and D_{it}. In our work, the behavior of N_{ot} and D_{it} were modeled using equations 3.6 and 3.14 and implemented in order to simulate the degenerative effects of radiation in FDSOI transistors. Likewise, we have included the thermal regeneration model that describes the progressive recovery of degraded electrical characteristics described in equations 3.24 and 3.26. The electrical compensation model is intrinsic to this library, so its effectiveness was also simulated.

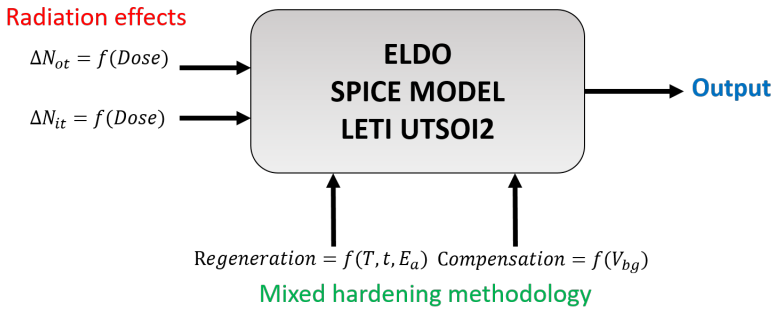
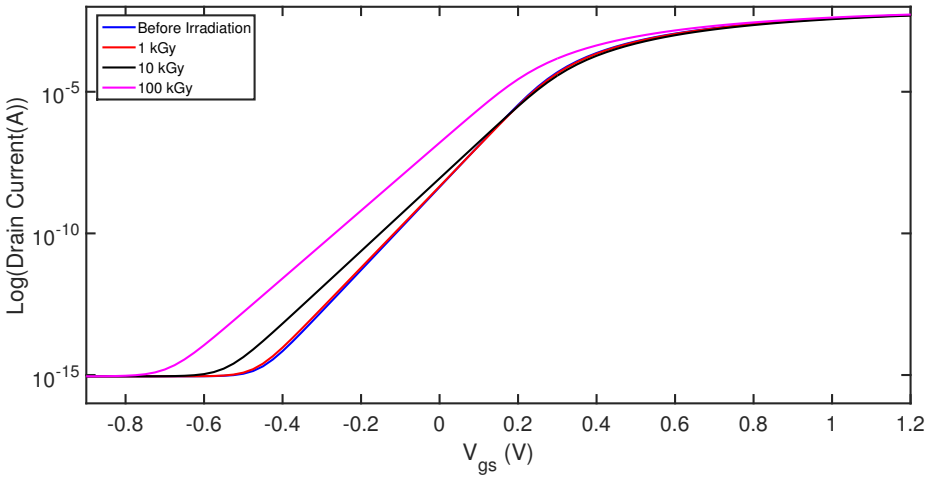


Figure 3.17: Block Diagram of UTSOI2 model including the TID effects and regeneration by annealing cycles.

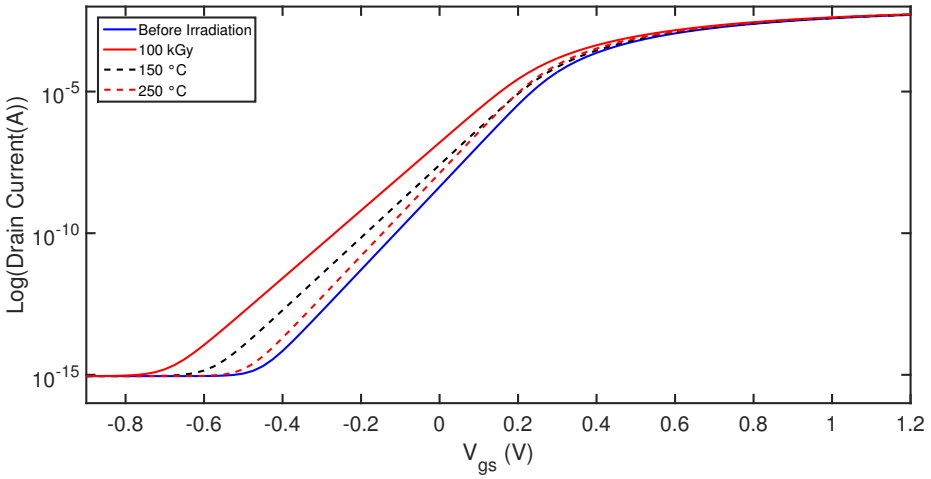
The simulation was carried out using the ELDO-SPICE simulator, but the models can be implemented in any other SPICE simulator. The input parameter, in the case of the effects of TID, is the Dose in Gy. In the case of annealing regeneration, the input parameters are the temperature, the annealing cycle and the activation energy. In the case of the electrical compensation, the input parameter is V_{bg}.

Figure 3.18 shows the simulation of each phenomenon for an NMOS transistor $W = L = 2\ \mu m$. In 3.18(a) we simulate a dose of 1 kGy, 10 kGy, and 100 kGy. The degradation of the electrical characteristics induced by radiation, such as the negative threshold voltage shift and the subthreshold slope deterioration are observed at each level of TID. The maximum degradation of V_{th} is around 180 mV at 100 kGy. In 3.18(b), the effect of thermal regeneration is observed, the progressive recovery of V_{th} and SS is noticed for two cycles applied at 150 °C and 250 °C reducing ΔV_{th} to -22 mV. In Figure 3.18(c) the electrical compensation is simulated for values of $V_{bg} = -1\ V,\ -0.5\ V,\ 0.5\ V$ and $1\ V$. This allowed us to verify that the value of the recovery coefficient $n = 80\ mV/V$ is in accordance with the values cited in the state of the art. To simulate each effect more accurately, these models should be calibrated using experimental data.

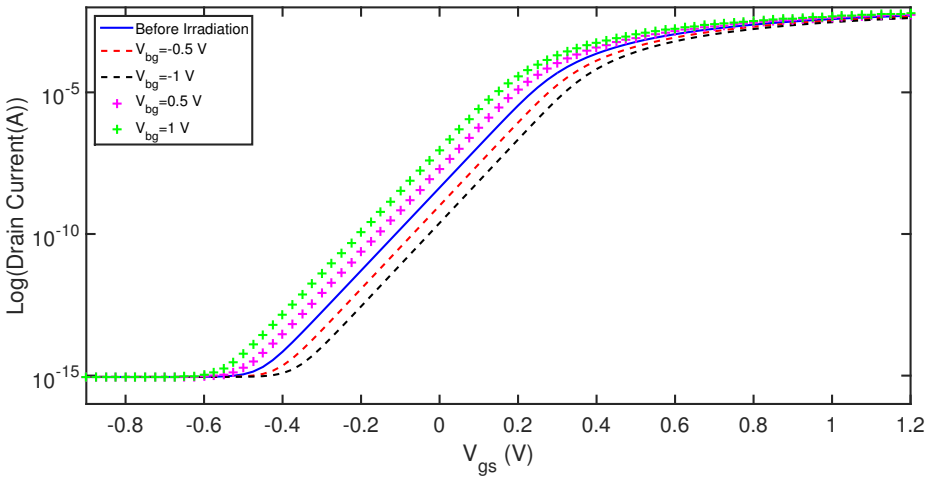
These models will be used with the objective of predicting and preventing the effects of TID in basic cells of digital circuits. For this reason, an analysis will be carried out in Chapter 5 to study the effects of radiation, electrical compensation, and thermal regeneration in the behavior of an inverter gate and a ring oscillator (RO).



(a) TID-induced degradation.



(b) Thermal annealing regeneration.



(c) Electrical compensation.

Figure 3.18: Simulation of TID-induced degradation and the recovery methods in a NMOS $W = L = 2\ \mu m$ SPICE library.

3.7 Conclusion of the chapter

This chapter showed the physical modeling, TCAD and SPICE simulations of the FDSOI technology under ionizing radiation. After a series of simulations carried out with the help of TCAD tool, we conclude that the BOX is the main responsible for the degradation of V_{th}, while the gate oxide has an almost negligible contribution in this degradation the negative shift of V_{th}. This is due to the fact that the BOX, made of SiO_2, is much thicker than the gate oxide and can thus contain a much higher amount of trapped charges.

In all the studied cases, the influence of N_{ot} and D_{it} causes a change in the electrostatic response of the SOI structure. A large concentration of N_{ot} in the BOX is responsible for establishing a parasitic conduction channel in the $Si - BOX$ interface, which results in a disturbance in the back surface potential. The coupling that exists between both interfaces produces a variation of the front threshold voltage. This was confirmed through the different simulations carried out. This allows modeling of N_{ot} taking into account the thickness of BOX.

The physical models implemented in the SPICE libraries correctly reproduce the radiation effects, as well as the thermal regeneration and the electrical compensation in the 28nm FDSOI transistors. However, these models need calibration from experimental measurements in order to more precisely simulate their electrical degradation and their recovery. This will be very useful in the following chapters to simulate the behavior of basic digital cells and to predict the degradation or total failure of more complex circuits.

Chapter 4

Experimental setup and analysis of radiation effects on irradiated FDSOI transistors

This chapter describes a series of experiments carried out with different NMOS and PMOS 28nm FDSOI transistors having different characteristics in order to observe the evolution of their main electrical parameters degradation and the contribution of the oxide and interface trapped charges densities as a function of TID levels. Afterwards, the effect of thermal annealing regeneration and electrical compensation by applying V_{bg} is investigated on irradiated devices. All these parameters are extracted from I-V curves, and particularly V_{th} which is extracted using the Y-function. As previously discussed, this technique is well adapted for new generation MOSFET devices, i.e. FDSOI transistors. The charges trapped in the oxides and at interfaces are calculated according to the procedure described in Chapter 2.

4.1 Experimental description

4.1.1 Devices

The FDSOI devices were manufactured by STMicroelectronics processed on 300mm UNIBOND SOI wafers. The intrinsic silicon thickness tsi is 7 nm, the gate EOT t_{ox} is 1.8 nm and 2.8 nm for GO1 and GO2 transistors, respectively. The buried oxide t_{box} reaches a thickness of 25 nm while the nominal gate length is 30 nm. All transistors were fabricated following the process flow scheme showed in [69]. A High-κ /Metal Gate stack (HK/MG) is used

to control Vth on the devices [69]. A metal gate stack consists of a thin metal layer, typically TiN, sandwiched between a thicker polysilicon layer above, and the high-κ gate dielectric below[125]. The channel is undoped, thus V_{th} variations due to the manufacturing process are eliminated. The n- or p-type well are implanted to have a LVT or RVT device [197].

To observe their radiation response, twenty-four 28nm FDSOI transistors with wide-long and short-narrow dimensions, different substrates (LVT and RVT), and different gate-oxide thickness (GO1 and GO2) were tested. Table 4.1 summarizes the characteristics of these transistors.

Table 4.1: Characteristics of tested MOSFETS of both wafers.

Type	Transistors	W (μm)	L (μm)
LVT	NMOS1	1	1
	NMOS2	0.21	0.03
	NMOS3 (GO2)	2	2
	PMOS1	1	1
	PMOS2	0.3	0.03
	PMOS3(GO2)	2	2
RVT	NMOS4	1	1
	NMOS5	0.21	0.03
	NMOS6	0.3	0.1
	PMOS4	1	1
	PMOS5	0.3	0.03
	PMOS6	0.3	0.1

4.1.2 Irradiation

The devices were irradiated with a ^{60}Co $bg\gamma$-ray source at the ArcNucleART facility in Grenoble, France. Two wafers with the same transistors were placed at different distances from the source, as shown in Figure 4.1(a), in order to observe the effect of the dose-rate on the devices.

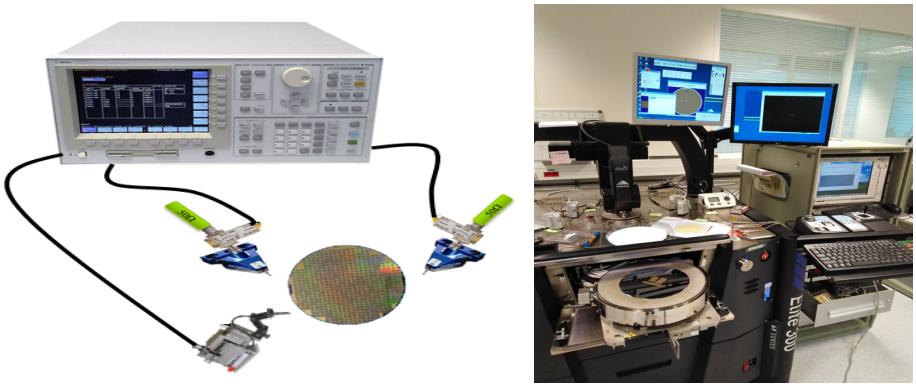
(a) Placement of both wafers. (b) $\gamma - rays$ source.

Figure 4.1: Configuration used for the irradiation of elementary FDSOI transistors.

The wafers W1 and W2 were exposed to a dose-rate of 1.3 kGy/h (36.1 rad/s) and 115 Gy/h (3.2 rad/s), respectively. The ionizing dose was deposited in three steps on both wafers. Wafer 1 (W1) with steps at 2 kGy, 20 kGy to finally reach 115 kGy (11.5 Mrad) while Wafer 2 (W2) received 200 Gy, 2 kGy up to 10 kGy (1 Mrad).

4.1.3 Electrical measurements

The measurements were carried out at the "Laboratoire de Carcatérisation et Test Électriques (LCTE)" at the CEA-LETI in Grenoble. The bias conditions applied to the transistors during their measurement are summarized in Table 4.2. It should be mentioned that the transistors used during this experiment were designed for electrical characterization of wafers, and thus were all unpackaged. This explains why we could not apply any biasing to the tested devices during the irradiation. All measures made in laboratory have been carried out with a probe test machine and a parameter analyzer (Figure 4.2).



(a) Probe test and Semiconductor parameter analyzer. (b) Electrical measurements.

Figure 4.2: Set-up used for electrical measurements.

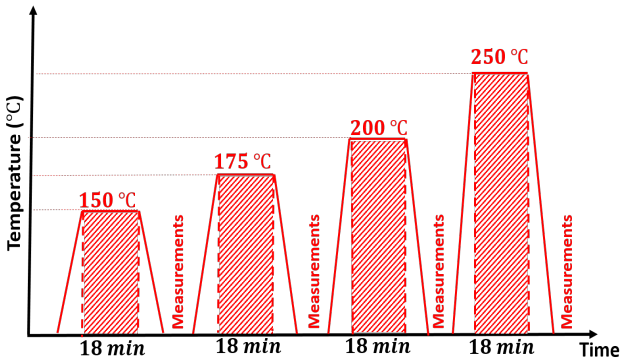
An initial electrical characterization of each device was carried out before irradiation in order to have a reference point. The curves $I_d(V_{gs})$ for different values of V_{bg}, $I_d(V_{ds})$, C (V) and G (V) were obtained using the semiconductor parameter analyzer. All I-V measurements were obtained after each irradiation step. Unlike the C(V) and G(V) measurements which were made only after the end of irradiation experiment.

Table 4.2: Electrical measurements of tested MOSFETs of both wafers.

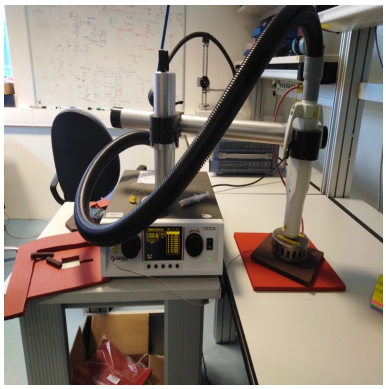
Type	Measurement	From	To	Step	Others***
NMOS	$I_{ds}(V_{gs})$	-1 V	1.2 V	20 mV	$V_{ds} = 0.04\ V\ and\ V_{ds} = 0.9\ V$
	$I_{ds}(V_{ds})$	0 V	1 V	10 mV	V_{gs}=0.2 to 1.2 V; step 200 mV
	$I_{ds}(V_{gs})$ @ V_{bg}	-1 V	1.2 V	20 mV	$V_{bg} = -1.6\ V\ to\ 1.6\ V$ step 400 mV
PMOS	$I_{ds}(V_{gs})$	1 V	-2 V	25 mV	$V_{ds} = -0.04\ V\ and\ V_{ds} = -0.9\ V$
	$I_{ds}(V_{ds})$	0 V	-1 V	10 mV	V_{gs}=0.3 to 1.5 V; step 300 mV
	$I_{ds}(V_{gs})$ @ V_{bg}	1 V	-2 V	20 mV	$V_{bg} = -1.6\ V\ to\ 1.6\ V$ step 400 mV

4.1.4 Annealing cycles

In order to observe and characterize the progressive regeneration of FDSOI transistors degraded by TID, we applied to the tested devices four isochronal thermal annealing cycles after each irradiation step (Figure 4.3 (a)). The temperatures of these cycles were 150 °C, 175 °C, 200 °C and 250 °C. The duration of each cycle was set at 18 minutes to reach an activation energy of 1 eV with the highest temperature. The electrical measurements were immediately performed at room temperature after the application of each annealing cycle. The thermal annealing process was carried out with the help of a heating machine (Figure 4.3(b)), which is capable of increasing the temperature from 25 °C to 250 °C in 65 seconds and cooling the device to room temperature in 122 seconds.



(a) Annealing cycles.



(b) Heating machine.

Figure 4.3: Annealing procedure.

4.1.5 Experimental procedure

This experiment was carried out in multiple stages described below and shown in Figure 4.4:

1. A pre-characterization including I-V and C-V measurements of all devices. This initial measurement gave us a reference point for each device.

2. Three irradiation steps were carried out at t = 1h30, t = 16h00 and t = 88h00 with electrical measurements between each step.

3. After the final irradiation step, four isochronal annealing cycles were applied with electrical measurements between each annealing cycle.

4. A set of 8 electrical measurement including the I-V measurements described in Table 4.2 were obtained.

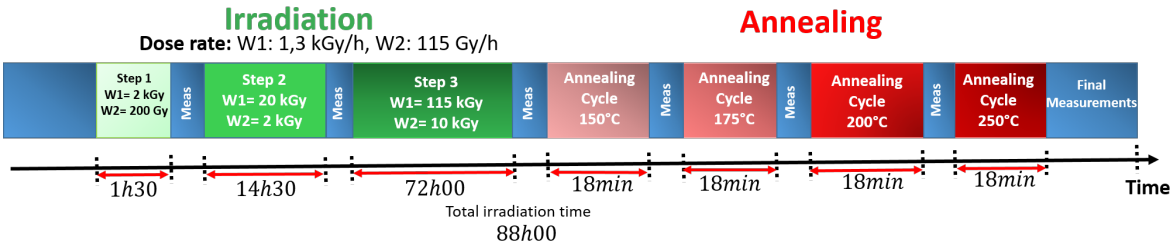


Figure 4.4: Experimental procedure timeline.

4.2 Results analysis

In this section, we analyze the experimental results obtained after irradiation, annealing regeneration and back-gate voltage compensation applied NMOS and PMOS transistors. To quantify the effects of TID on the irradiated FDSOI transistors, we have extracted some key parameters using the methods described in Chapter 2. The main parameters extracted were: the threshold voltage (V_{th}), the subthreshold slope (SS), the density of charges trapped in the oxides (N_{ot}), and the density of charges trapped at $Si - SiO_2$ interface (D_{it}).

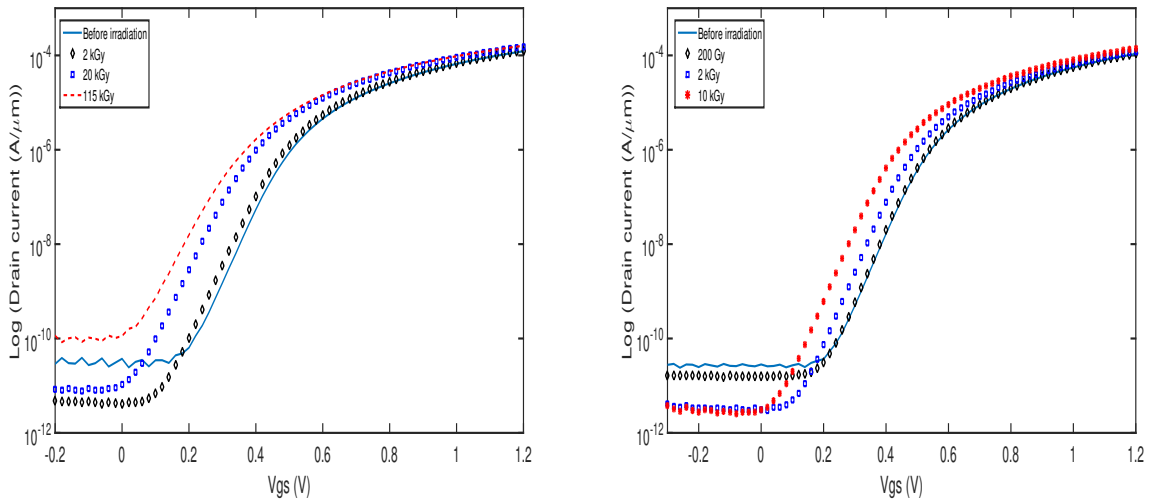
4.2.1 Radiation effects on FDSOI transistors

NMOS transistors

The FDSOI transistors exhibited typical degradation at each TID level. As expected, a negative threshold voltage shift and a degradation of the subthreshold slope were noticed. Likewise, an increase in leakage currents was observed. Figure 4.5 shows a $I_{ds}(V_{gs})$ characteristic of a long-channel NMOS transistor corresponding to W1, irradiated at 1.3 kGy/h, and the same long-channel NMOS transistor of W2 irradiated at 115 Gy/h.

Figure 4.5(a) shows the results of the NMOS transistor $W = L = 1\ \mu m$ (NMOS1) with a gate oxide thickness GO1 irradiated at different dose-rates. The exposed device NMOS1 shows a progressive negative ΔV_{th}. We noticed that the degradation of the subthreshold slope at 2 kGy is not so severe because the charges trapped at the interfaces are not significant. The leakage currents are lower than the initial curve, which can be explained by the sensitivity of the measurements to temperature changes in addition to measurement noise. The last radiation step corresponding to 115 kGy shows a severe degradation with a ΔV_{th} around 100 mV and a subthreshold slope degraded by 9 mV/dec. Likewise, the leakage current showed a significant increase mainly due to the increase in charges trapped in the STI oxides. Figure 4.5(b) shows the degradation of the NMOS transistor on W2 having the same characteristics as the one in W1. Note that as mentioned the only difference between W1 and W2 is the dose-rate where W2 is exposed to lower dose levels. The threshold voltage degradation is about 85 mV at 10 kGy which is lower than the degradation of this NMOS transistor irradiated at higher dose levels. The subthreshold

slope degradation was limited with a $\Delta SS = 4.75\ mV/dec$.

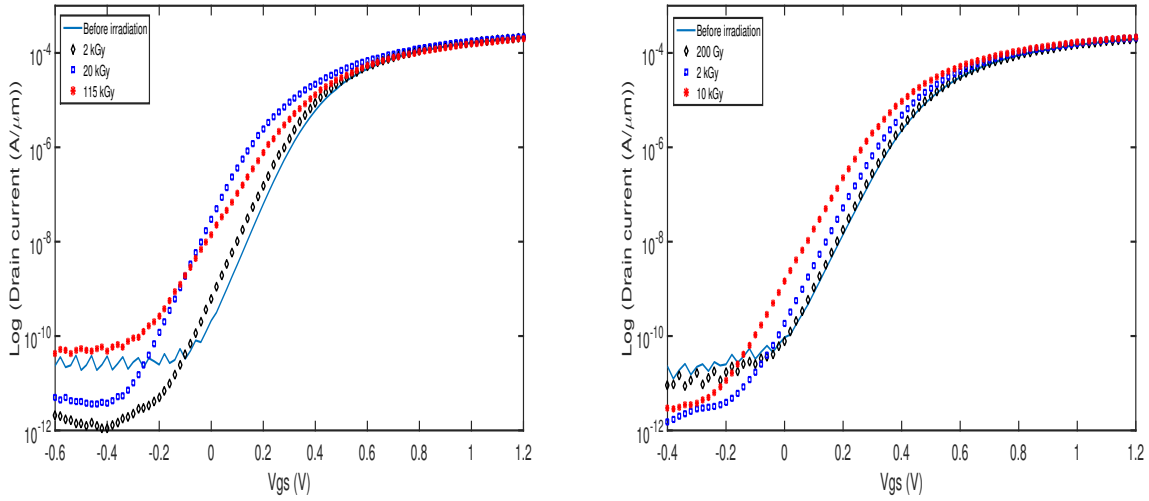


(a) NMOS1 W1.

(b) NMOS1 W2.

Figure 4.5: Radiation response of a NMOS LVT transistor $W = L = 1\ \mu m$.

Figure 4.6 shows the $I_{ds}(V_{gs})$ characteristic of a short-narrow NMOS transistor (NMOS2) with $W = 0.21\ \mu m$, $L = 0.3\ \mu m$. Due to their small dimensions compared to those with a long channel, the response of these devices is presumed to be different after a certain level of absorbed radiation. As can be viewed in Figure 4.6(a), a negative ΔV_{th} is observed up to a level of 20 kGy. The subthreshold slope degradation for the first two TID levels (2 kGy and 20 kGy) is barely noticeable with a $\Delta SS \leq 5mV/dec$ while for the third level, corresponding to 115 kGy, the $I_d(V_{gs})$ curve shows a significant degradation of the slope on the contrary to V_{th}. This can be explained by the charge saturation effect due to their small oxide volume. As a matter of fact, the charges occupy all available traps in the oxide and create new ones which produces trapped charges at deeper energy levels. The charge saturation in the oxide leads therefore to more displacement towards the interface which is the main factor of subthreshold slope degradation. It is expected a continuous degradation of the subthreshold slope if the TID continues to increase. The device on Wafer 2 exhibits a ΔSS degradation of 6.68 mV/dec and a $\Delta V_{th} = 115\ mV$ after the end of the irradiation. For all tested NMOS transistors, the maximum ΔV_{th} observed is 139 mV corresponding to NMOS2 while the mean ΔV_{th} is around 110 mV. The V_{th} degradation extracted experimentally in this work are similar to those reported in the literature for high levels of TID [91, 97, 198].



(a) NMOS2 W1.

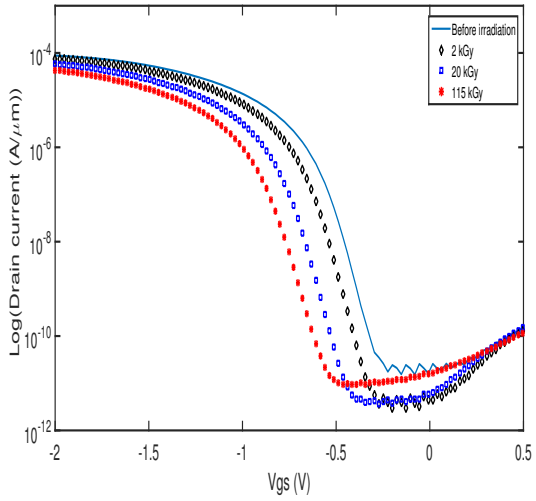
(b) NMOS2 W2.

Figure 4.6: Radiation response of a NMOS LVT transistor W=0.21 μm, L=0.03 μm.

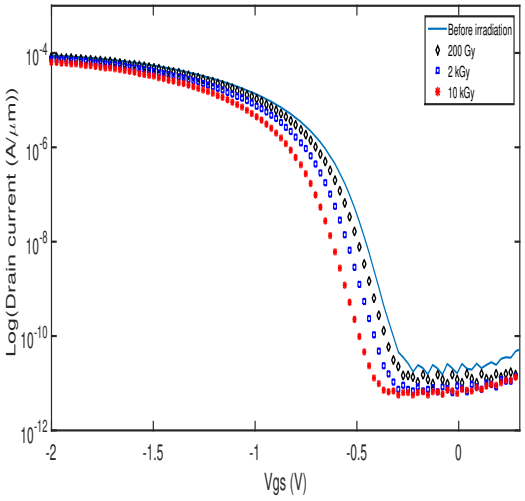
PMOS transistors

The response to TID of PMOS devices differed from NMOS ones. The analysis of experimental results showed that radiation-induced charges lead to a higher threshold voltage degradation shift for PMOS transistors. For instance, the maximum value of delta V_{th} is 358 mV and 287 mv for irradiated PMOS and NMOS transistors, respectively. However, we observed that for PMOS transistors, the SS is not severely impacted by the TID. In fact, the maximum ΔSS observed was around 15 mV/dec while for NMOS was 32 mV/dec. This phenomenon can be explained by the predominance of trapped charges in the volume of oxides created at a low dose-rate. After being trapped, these charges slowly begin to move towards the interfaces. On the other hand, the charges created by a higher dose-rate will tend to occupy both interfaces more quickly, severely degrading the SS as can be observed in the W1 devices.

Figure 4.7 shows the response of a PMOS transistor (PMOS4) $W = L = 1\ \mu m$ irradiated at different TID levels. In (a) a progressive ΔV_{th} shift with each level of TID is noticed with a maximum $\Delta V_{th} = 281\ mV$. Otherwise, SS does not show significant degradation even at the highest TID level (115 kGy) with $\Delta SS = 6.4\ mV/dec$. In (b) the V_{th} shift is significantly lower because this device was irradiated at a lower dose-rate. The maximum degradation of threshold voltage was $\Delta V_{th} = 190\ mV$ and that of subthreshold slope was $\Delta SS = 5.43\ mV/dec$. From these results, we can conclude that PMOS transistors are more sensitive to the effects of radiation than NMOS ones. In addition, unlike NMOS transistors, there is no compensating effect, i.e., rebound effect. For this reason PMOS transistors are sometimes used as dosimeters.

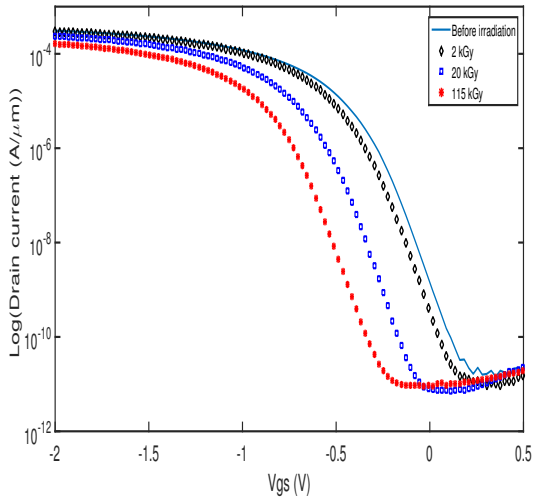


(a) PMOS4 W1.

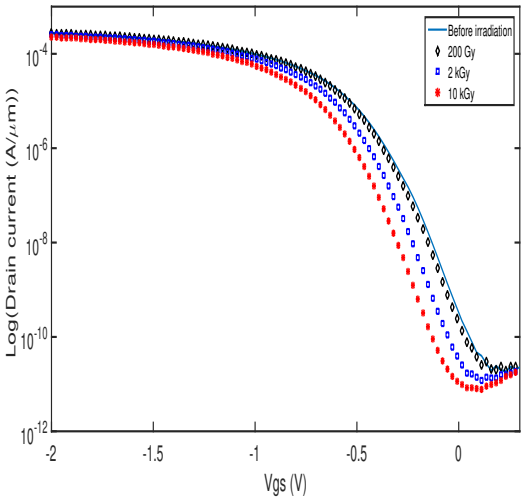


(b) PMOS4 W2.

Figure 4.7: Radiation response of a PMOS-RVT transistor $W = L = 1\ \mu m$.



(a) PMOS5 W1.



(b) PMOS5 W2.

Figure 4.8: Radiation response of a PMOS-RVT transistor W=0.3 μm, L=0.03 μm.

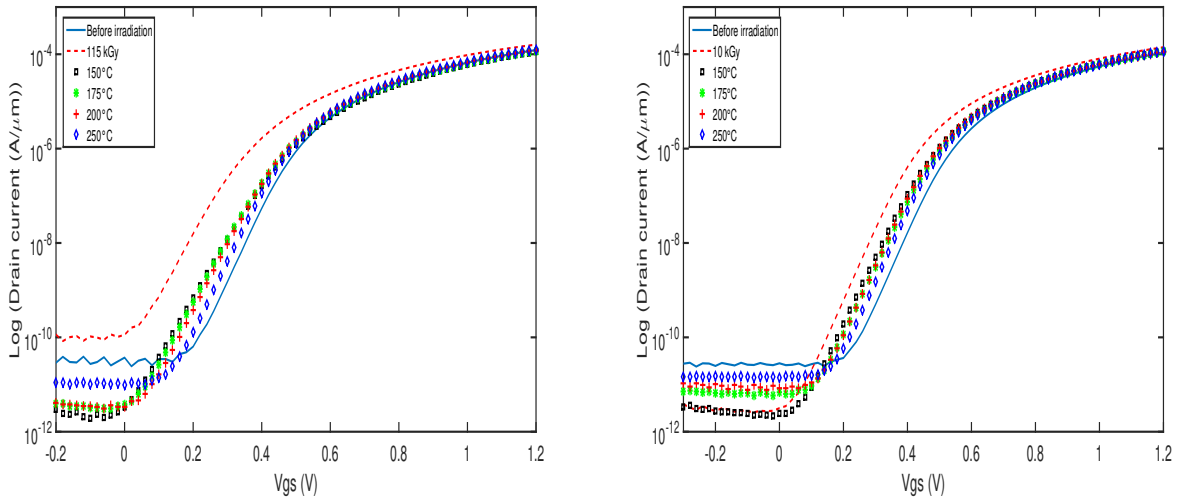
In Figure 4.8 we show the response of short short channel-narrow width transistors with W=0.3 μm, L=0.03 μm (PMOS5) after irradiation. In Figure 4.8(a) the transistor belonging to W1, irradiated at a high dose rate, shows an aggressive negative ΔV_{th} with each TID level more severe than that observed for the long channel ones. This is due to the small size of the oxides of these transistors becoming saturated with trapped charges and leading therefore to a higher threshold voltage shift. In Figure 4.8(b) the characteristic $I_{ds}(V_{gs})$ of the PMOS transistor belonging to W2 is displayed. A negative ΔV_{th} is noticed but lower than the shift observed for the same transistor in W1. This reflect the effect of the dose-rate on the threshold voltage degradation of irradiated devices. On the

other hand, the SS degradation was 12 mV/dec and 6 mV/dec for transistors on W1 and W2, respectively.

4.2.2 Annealing effect on irradiated transistors

NMOS transistors

The applied annealing cycles progressively detrap the charges in the insulating oxides, which lead to the recovery of V_{th}, SS and I_{off}. In both wafers, irradiated at different dose-rates, we can observe that a temperature of 250 °C can partially regenerate these 3 main degraded characteristics.

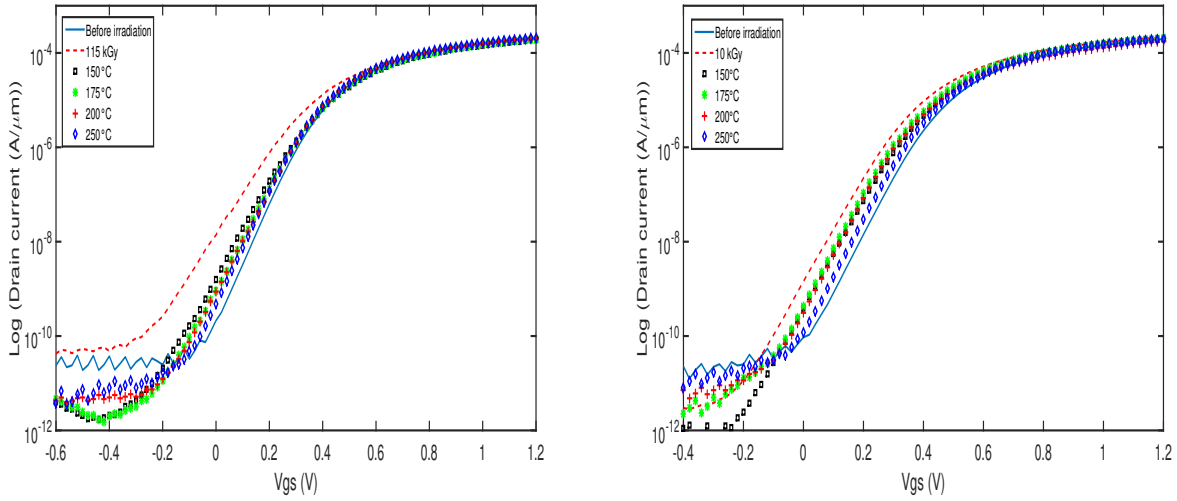


(a) NMOS4 W1.

(b) NMOS4 W2.

Figure 4.9: Regeneration of degraded electrical characteristics of a NMOS RVT transistor $W = L = 1\ \mu m$.

Figure 4.9 shows the response of the same NMOS transistors (NMOS4) $W = L = 1\ \mu m$ of W1 and W2 after irradiation and after each annealing cycle. Both devices NMOS4 of W1 and W2 exhibit progressive regeneration. However, even after applying 250 °C, a residual threshold voltage shift of 17 mV for NMOS4 W1 and of 20 mV for NMOS4 W2 remains due to the charges trapped at deeper energy levels and that were not evacuated. A higher temperature engendering higher activation energy may detrap these charges to fully regenerate the transistor. The SS was was also recovered for both transistors. Figure 4.10 shows the response of NMOS-RVT devices $W = 0.21\ \mu m$ $L = 0.03\ \mu m$ (NMOS5). After applying the 250 °C anneal, a residual ΔV_{th} of 37 mV and 34 mV was measured for the devices in W1 and W2 respectively. The SS was recovered almost totally in these devices.



(a) NMOS5 W1.

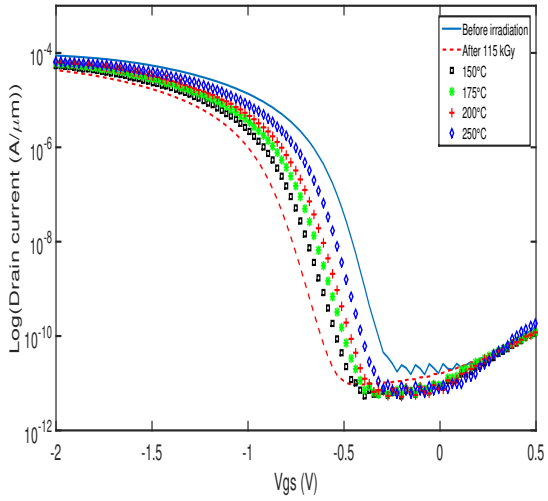
(b) NMOS5 W2.

Figure 4.10: Regeneration of the electrical characteristics of a NMOS RVT transistor $W = 0.21\ \mu m$, $L = 0.03\ \mu m$.

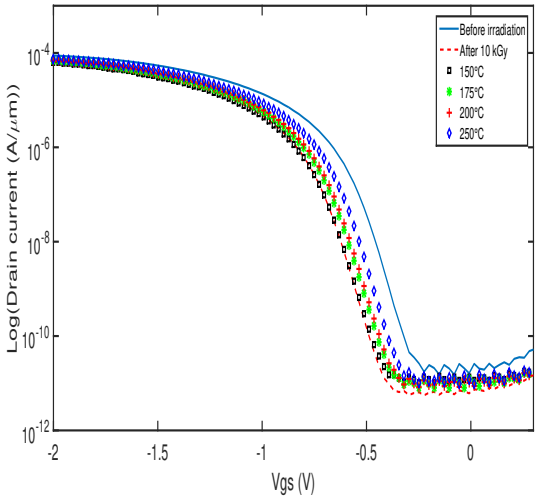
PMOS transistors

Like NMOS transistors, PMOS devices were annealed following the same experimental procedure. Figure 4.11 shows the recovery observed on irradiated PMOS4 transistors belonging to W1 and W2, after each annealing cycle. In Figure 4.11(a), the dotted line curve shows the ΔV_{th} at the end of irradiation. The subsequent curves at 150 °C, 175 °C, and 200 °C show the progressive regeneration with each cycle reaching a residual ΔV_{th} of 48 mV and a ΔSS of 2.7 mV/dec after the last annealing cycle with a temperature of 250 °C. For PMOS4 transistors of W2, that were irradiated at low dose rate, applying a temperature of 150 °C has practically no effect on the detrapping process. This can be explained by the fact that the trapped charges are located at deeper energy levels that can not be reached with such a low temperature. The cycles at 175 °C, 200 °C, and 250 °C showed great efficiency on the regeneration of both the threshold voltage and the subthreshold slope degradation.

In Figure 4.12, the thermal regeneration is shown for a short channel PMOS transistor with $W = 0.3\ \mu m$, $L = 0.03\ \mu m$. As in the previous case, the progressive recovery of the electrical characteristics is observed for the transistors belonging to W1 and W2. In both cases, a residual degradation of 28 mV and 15 mV, respectively, is measured due mainly to the charges trapped at deeper energy levels.

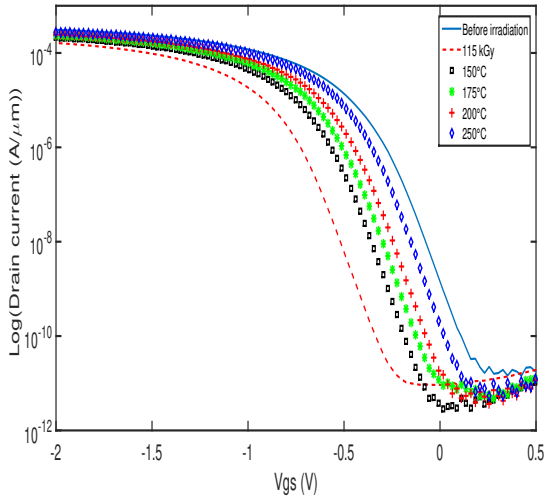


(a) PMOS4 W1.

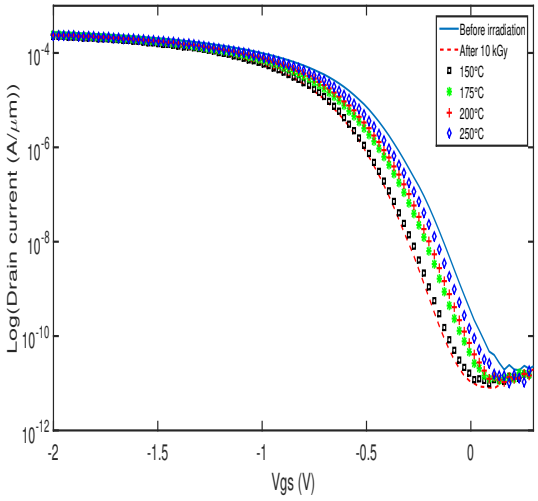


(b) PMOS4 W2.

Figure 4.11: Response of irradiated PMOS transistors with $W = L = 1\ \mu m$ to thermal regeneration.



(a) PMOS5 W1.



(b) PMOS5 W2.

Figure 4.12: Response of irradiated PMOS transistors with $W = 0.3\ \mu m$, $L = 0.03\ \mu m$ to thermal regeneration.

Table 4.3 summarizes the maximum measured degradation of V_{th} and SS as well as the residuals of these parameters after applying the last annealing cycle with a temperature of 250 °C for all irradiated devices belonging to both wafers. The values in this table confirm that in the same conditions, PMOS transistors are more sensitive to ionizing radiation than NMOS ones.

Thermal annealing is effective in regenerating the degraded electrical characteristics of both devices (NMOS and PMOS). In NMOS devices, a residue of 25 mV on average is observed after annealing at 250 °C while PMOS ones present a higher residual V_{th} due to their higher degradation. The SS degradation are almost completely

recovered after the annealing at 250 °C. For some devices, the subthreshold slope shows even an improvement with respect to the initial value. In that case, we note ΔSS_r as 0* in the table bellow. This is due to the effect of thermal annealing that evacuates the dangling bonds present at the interfaces due to the manufacturing process.

Table 4.3: Maximum degradation and recovery of all irradiated devices.

Wafer	Transistor	$\Delta V_{th_{max}}$	ΔSS_{max} (mV/dec)	ΔV_{th_r} (mV)	ΔSS_r (mV/dec)
W1	NMOS1	100	9.06	14	1
	NMOS2	139	15.73	22	2.81
	NMOS3 (GO2)	122	33	27	5.92
	NMOS4	110	12.1	17	0.22
	NMOS5	119	32.86	37	0.6
	NMOS6	109	17.25	25	2.86
	PMOS1	141	9.6	41	1.03
	PMOS2	233	5.02	28	0*
	PMOS3(GO2)	348	16.7	161	4.9
	PMOS4	281	6.41	48	2.7
	PMOS5	226	12.86	28	0*
	PMOS6	358	11.5	97	1.87
W2	NMOS1	85	4.75	27	0.77
	NMOS2	115	6.68	6	0.43
	NMOS3 (GO2)	101	15.6	18	2.57
	NMOS4	97	5.43	20	0.52
	NMOS5	98	6.36	34	0*
	NMOS6	107	1.38	28	0.48
	PMOS1	106	4.75	35	0.77
	PMOS2	208	15.7	51	2.81
	PMOS3(GO2)	287	11.8	101	0*
	PMOS4	190	5.43	56	0*
	PMOS5	210	6.26	15	0.21
	PMOS6	168	8.86	62	0*

4.2.3 Effect of Back-gate bias V_{bg}

NMOS transistors

Figure 4.13 and 4.14 show the result of applying multiple V_{bg} values on irradiated NMOS transistors. We notice that the V_{bg} technique allows the compensation of ΔV_{th} induced by radiation, but due to the high levels of TID applied to W1, the applied V_{bg} is not sufficient to fully compensate the degraded device. For W2, we were able to cancel the ΔV_{th} by applying a V_{bg} of -1.6 V to most transistors. However, and as previously mentioned, V_{bg} does not compensate for ΔSS neither for ΔI_{off}. The impact of the TID on the coefficient n was extracted. From the electrical measurements obtained, the extracted values of n for all transistors range between 76 mV/V and 81 mV/V before irradiation. This spread is due mainly to the initial presence of interface states that differs from one device to another. As exposed in Chapter 2, the body coefficient n is strongly influenced by C_{itb}, thus n variation depends on the charges trapped in the $Si-BOX$ interface. Without taking into account the contribution of interface

states, the n coefficient for a pristine device is equal to:

$$n_{fresh} = \frac{C_{si}C_{box}}{C_{ox}(C_{si} + C_{box})} \tag{4.1}$$

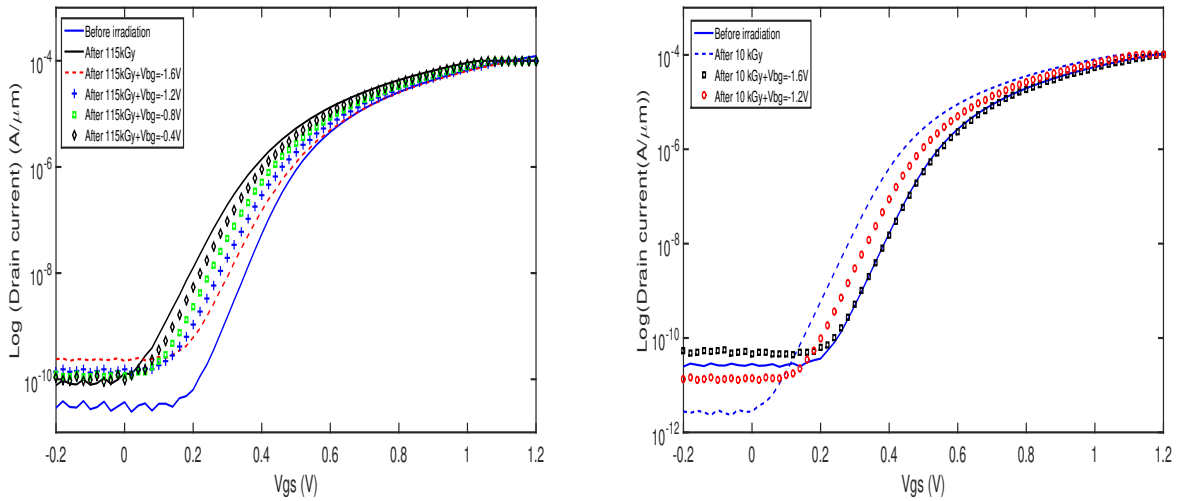
and for an irradiated device:

$$n_{irrad} = \frac{C_{si}C_{box}}{C_{ox}(C_{si} + C_{box} + C_{itb})} \tag{4.2}$$

Then, the variation of the body coefficient is expressed as:

$$\Delta n = n_{irrad} - n_{fresh} = n_{fresh}[\frac{C_{itb}}{(C_{si} + C_{box} + C_{itb})}] \tag{4.3}$$

From this expression, we can deduce that a variation of $D_{itb} = 10^{12}\ cm^{-2}eV^{-1}$ results in a $\Delta n \approx 7\ mV$. The n coefficient extracted from the devices of this experiment after 115 kGy present values between 65 mV/V and 72 mV/V. This confirms the increase of D_{itb} around $10^{12}\ cm^{-2}eV^{-1}$ for these devices.



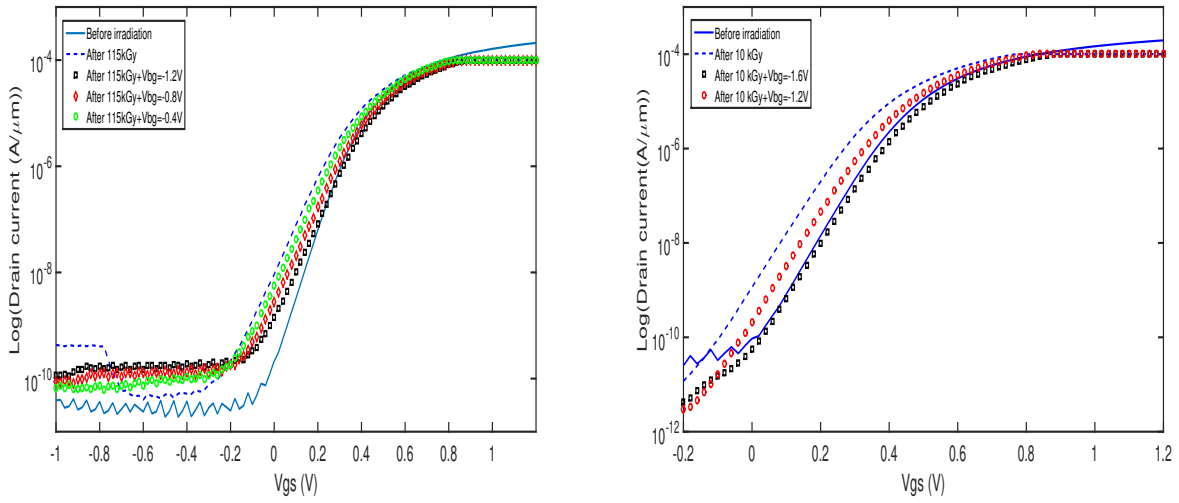
(a) NMOS4 W1.

(b) NMOS4 W2.

Figure 4.13: Back-bias response of irradiated NMOS RVT transistors with $W = L = 1\mu m$.

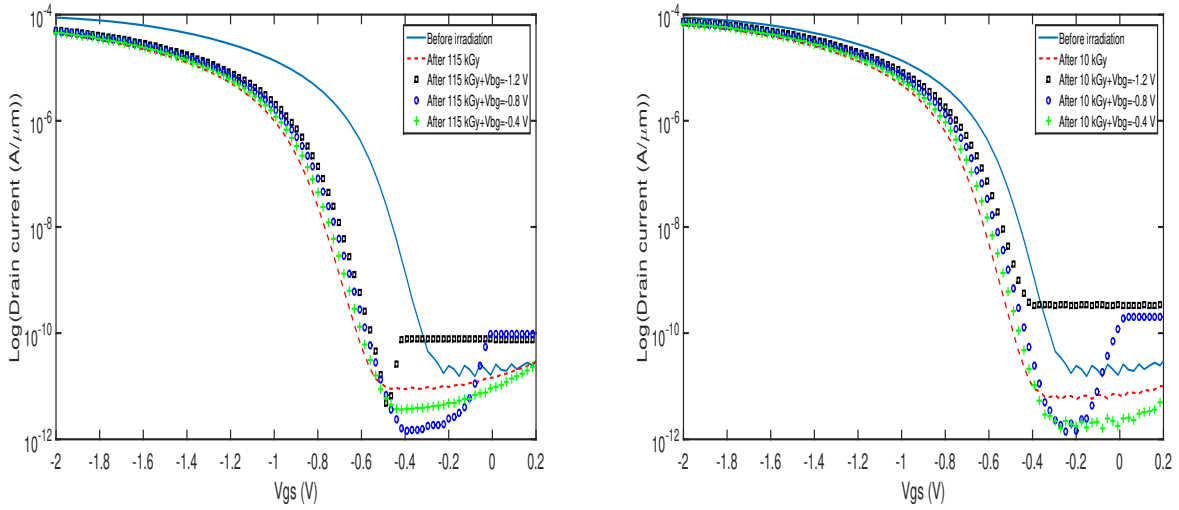
In the case of short-channel NMOS transistors, $W = 0.21\ \mu m,\ L = 0.03\ \mu m$, the applied V_{bg} was sufficient to compensate for the ΔV_{th} induced by N_{ot}, but not the one produced by D_{it}. This is observed in Figure 4.14 (a), where the ΔSS reflects the significant increase of D_{it} leading to a slower response of the device when it goes from OFF to ON state. In this case, the use of a thermal anneal is necessary to recover the SS. In the transistor of W2, depicted in Figure 4.14 (b), a V_{bg} of -1.6 V was necessary to fully compensate for the ΔV_{th}. The SS degradation was not as severe as in the W1 device, so thermal annealing was not, up to this point, necessary. In general, W2-irradiated NMOS devices exhibit low SS degradation and a ΔV_{th} that can be compensated with back-gate

technique. This fact is advantageous for applications where this level of TID is expected. On the other hand, W1 devices require a thermal anneal to recover the degradation of SS.



(a) NMOS5 W1. (b) NMOS5 W2.

Figure 4.14: Back-bias response of irradiated short channel NMOS RVT transistors $W = 0.21\ \mu m, L = 0.03\ \mu m$.



(a) PMOS4 W1. (b) PMOS4 W2.

Figure 4.15: Back-bias compensation of irradiated PMOS RVT transistors with $W = L = 1\mu m$.

PMOS transistors

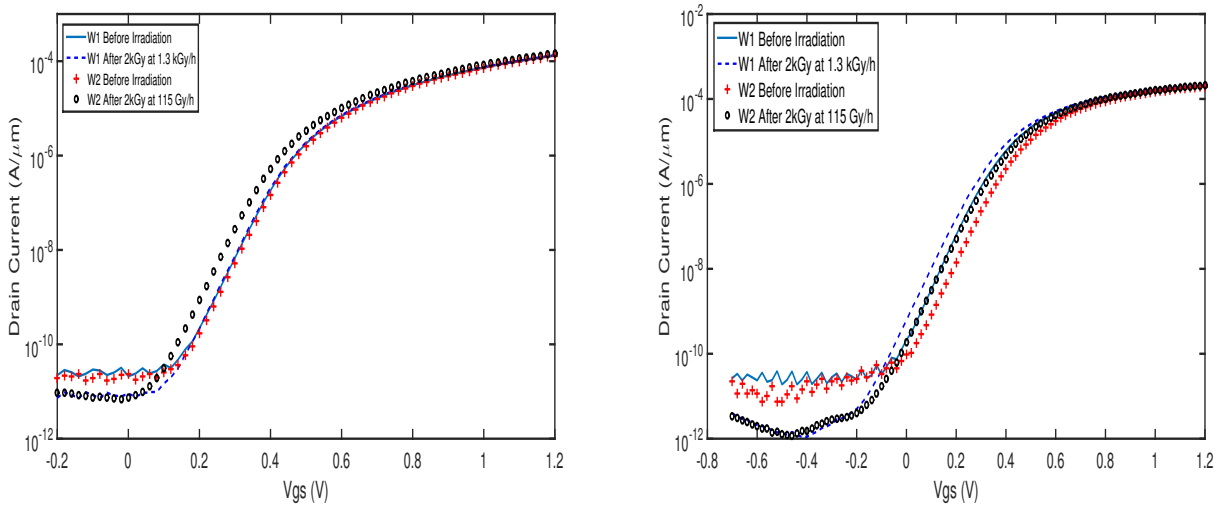
Figure 4.15 (a) and (b) shows the effect of applying V_{bg} to PMOS devices. We noticed that the applied V_{bg} is not sufficient to compensate for ΔV_{th} in both wafers, W1 and W2. Also, an increase in I_{off} is observed in the subthreshold region due to the conduction of the intra-substrate diodes resulting from the application of a V_{bg} beyond the established limit of this technology. This effect distorts the I-V characteristic of the transistors, having

as an immediate effect an increase in I_{off} and in consequence, a rise in the power consumption in an IC. Thus, to avoid this effect, the application of V_{bg} should be limited to the limits established by the physics of the component, in this case $V_{bg} \leq 1.8\ V$.

4.3 Dose-rate effects

As mentioned in the state of the art, MOSFET transistors can present different dynamics in the degradation of their electrical parameters depending on the dose-rate to which they are exposed. In order to analyze the dose-rate response of devices on both wafers, a common irradiation step was set at 2 kGy. The oxide trapped charges can present different time constants and distributions during their transport to the $Si-SiO_2$ interface when irradiated at different dose-rates. As a consequence, the magnitude of the electrical degradation can vary significantly. In most of cases, we noticed that devices irradiated at a dose rate of 115 Gy/h showed a slightly higher V_{th} degradation at a TID of 2 kGy than those irradiated at 1.3 kGy/h.

Figure 4.16(a) shows a NMOS with long channel that underwent a large degradation with $\Delta V_{th_{W1}} = -5.7\ mV$ and $\Delta V_{th_{W2}} = -56\ mV$. Figure 4.16(b) shows the dose rate effect on a short channel NMOS device. An initial variation in threshold voltage, purely due to the manufacturing process, was observed between both devices. On the other hand and as previously demonstrated, the irradiated device of W2 showed a greater degradation of threshold voltage with a $\Delta V_{th_{W1}} = -45\ mV$ and $\Delta V_{th_{W2}} = -52\ mV$.



(a) NMOS1. (b) NMOS2.

Figure 4.16: NMOS transistors irradiated up to a common point of 2 kGy at different dose rates.

Figure 4.17 summarizes the ΔV_{th} extracted from all devices at the common point at 2 kGy. Except for some special transistors, which are a minority, there is not a great difference between the ΔV_{th} in the W1 and W2 devices at

this dose level. The small difference between the two wafers can be explained by the variation of V_{th} that exists between one device and another due to process variation. This similarity in the degradations is probably due to the fact that the two wafers were irradiated at a high dose rate compared to those of experiments reported in some previous works. To really observe a dose-rate effect, devices should be exposed to a lower dose-rate.

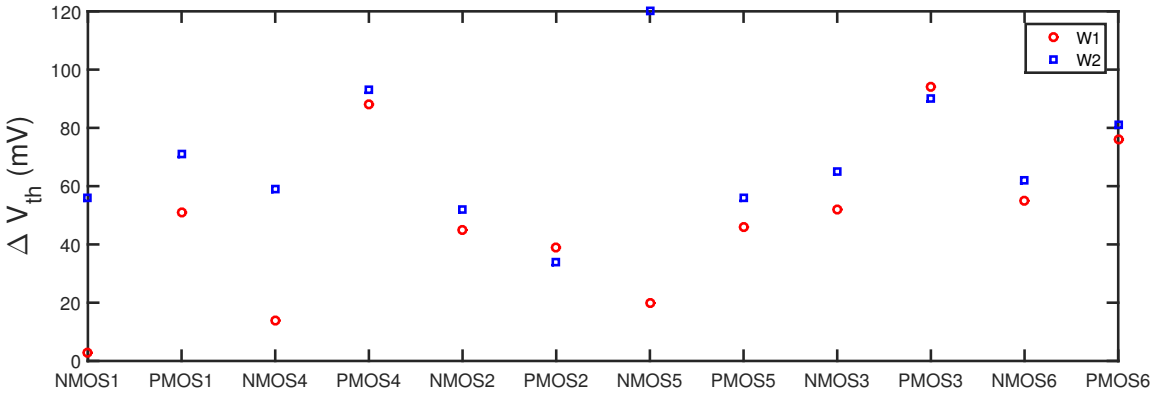
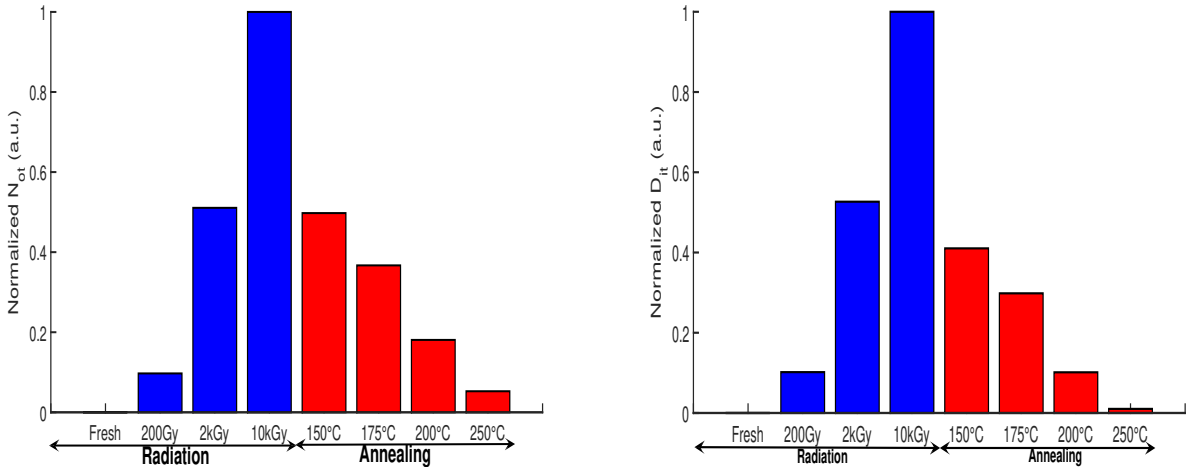


Figure 4.17: Threshold voltage shift at a common TID level of 2 kGy for all transistors.

4.4 Oxide and interface trapped charge dynamics

Following the procedure described in Chapter 2, we extracted the trapped charge densities N_{ot} and D_{it}. Figure 4.18 (a) and (b) shows the dynamics of N_{ot} and D_{it} respectively. A progressive increase of the trapped charges is noted with each irradiation step which degrades progressively the threshold voltage and SS. The application of the isochronal annealing cycles detraps the charges allowing the regeneration of the degraded electrical characteristics of the irradiated transistors. The remaining N_{ot} and D_{it} at 250 °C are responsible for the residual ΔV_{th} and ΔSS. Following the detrapping dynamics, we can estimate that an anneal around 275 °C could fully regenerate the electrical characteristics of the irradiated transistor. We observed that PMOS transistors have more residual N_{ot} and D_{it}. Hence, a higher annealing temperature (T $\geq$ 300 °C) is needed to totally recover their degraded characteristics.

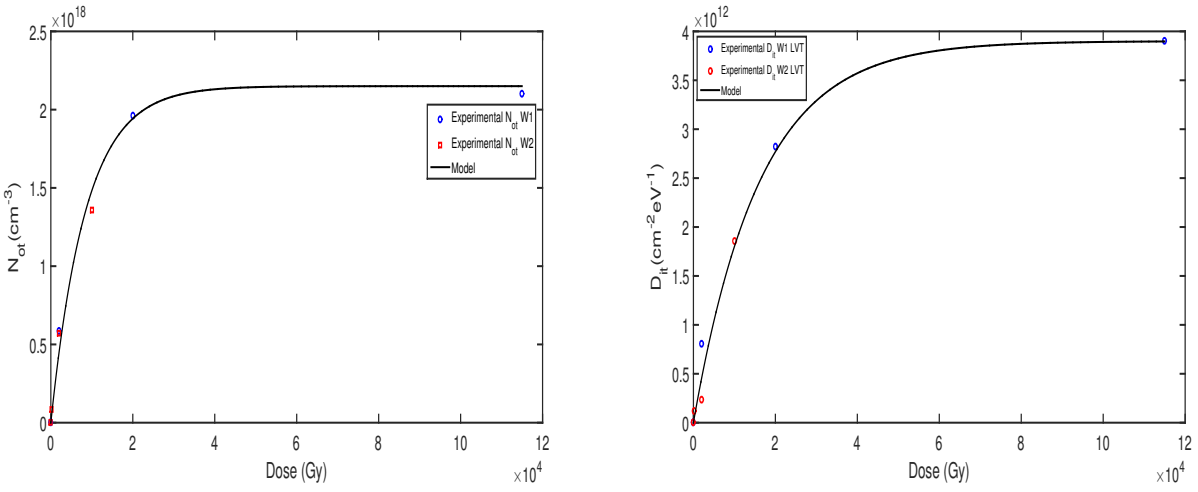
The extracted values of N_{ot} and D_{it} are within the range of those found in the state of the art. N_{ot} varies from $10^{16}\ cm^{-3}$ to $10^{18}\ cm^{-3}$ while D_{it} varies from $10^{10}\ cm^{-2}eV^{-1}$ to $10^{12}\ cm^{-2}eV^{-1}$ for both wafers. We can see here again that the annealing only partially recover the ΔV_{th}. The influence of the dose-rate on both wafers is not significant, so for the data treatment made before modeling, the transistors of both wafers are considered regardless of their irradiation conditions. This way, the model will give the the behavior of the transistors for low and high TID levels.



(a) N_{ot}. (b) D_{it}.

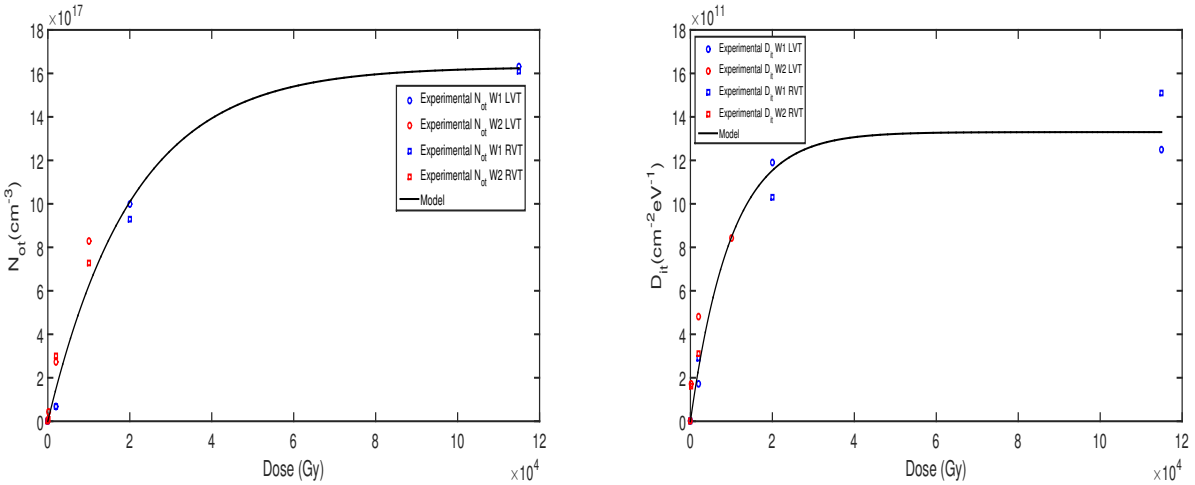
Figure 4.18: N_{ot} and D_{it} dynamics after the irradiation and annealing procedure.

Figure 4.19 and 4.20 shows N_{ot} and D_{it} extracted from the $I_d(V_{gs})$ characteristics of PMOS transistors with $W = L = 2\ \mu m$ GO2 and a PMOS $W = L = 1\ \mu m$ respectively. We see a dynamics that exponentially saturates for both N_{ot} and D_{it}, corresponding to the solution of the differential equation exposed in Chapter 3. Thus confirming the hypotheses proposed in the physical models of N_{ot} and D_{it}, where for low levels of TID (TID $\leq$ 10 kGy), a linear trapping behavior is observed. The charges generated by radiation are trapped on the defects present in the oxides volume and at the interfaces until there are no more places available. This is reflected by a slowdown in the trapping of charges on all curves. This dynamic was observed with all the irradiated NMOS and PMOS transistors.



(a) N_{ot}. (b) D_{it}.

Figure 4.19: Values of N_{ot} and D_{it} extracted for a PMOS $W = L = 2\ \mu m$ irradiated at a high dose-rate (W1).



(a) N_{ot} (b) D_{it}

Figure 4.20: Values of N_{ot} and D_{it} extracted for a PMOS $W = L = 1\ \mu m$ irradiated at a high dose-rate (W1)

Thanks to a fitting software, we were able to extract the constants related to the number of defects N, in addition to the charge yield $fy(E)$ by applying the model explained in chapter 3. The extracted values after fitting, showed in Table 4.4, agree with the values found in the state of the art for the charge yield, given without influence of the electric field, that ranges between 0.1 and 0.4 [4, 182, 183, 184]. The correlation factor R obtained after fitting shows good agreement between the extracted data and the proposed model of N_{ot}.

Table 4.4: Values for N_{ot} model extracted after fitting.

Wafer	Transistor	N	$f_y(E)$	R
NMOS	NMOS1 and NMOS4	1.63×10^{18}	0.1	0.96
	NMOS2 and NMOS5	1.03×10^{18}	0.17	0.92
	NMOS3 (GO2)	1.09×10^{18}	0.18	0.97
	NMOS6	1.55×10^{18}	0.32	0.88
PMOS	PMOS1 and PMOS4	1.38×10^{18}	0.1	0.92
	PMOS2	1.83×10^{18}	0.41	0.89
	PMOS3 (GO2)	8.83×10^{17}	0.57	0.98
	PMOS6	2.15×10^{18}	0.33	0.92

As was the case with N_{ot}, we used fitting software to extract the constants relative to the physical models proposed in chapter 3 and thus reproduce the trapping behavior. For this, we group transistors with similar characteristics. The constants found are shown in Table 4.5. The N_{SiH} values are close to those found in different works [181, 190].

Table 4.5: Extracted values for D_{it} model after fitting.

Wafer	Transistor	N_{siH}	$f_y(E)$	R
NMOS	NMOS1 and NMOS4	2.73×10^{12}	0.33	0.98
	NMOS2 and NMOS5	5.13×10^{12}	0.11	0.95
	NMOS3 (GO2)	4.27×10^{12}	0.36	0.91
	NMOS6	4.3×10^{12}	0.21	0.99
PMOS	PMOS1 and PMOS4	1.33×10^{12}	0.37	0.94
	PMOS2 and PMOS5	3.89×10^{12}	0.23	0.88
	PMOS3 (GO2)	3.65×10^{12}	0.22	0.99
	PMOS6	3.82×10^{12}	0.26	0.91

4.4.1 Activation energies

Following the procedure described in Chapter 3, the activation energies were extracted after each annealing cycle. Tables 4.5 and 4.6 show the extracted activation energy levels in the NMOS and PMOS transistors on both test wafers. In both tables, a uniformity is observed in the activation energy values with the application of each cycle, with values ranging between 0.79 and 1.1 eV for all the applied temperatures. The uniformity of the extracted values will allow us to easily make a physical model that describes the annealing process in FDSOI devices under irradiation.

Table 4.6: Activation energies of NMOS transistors.

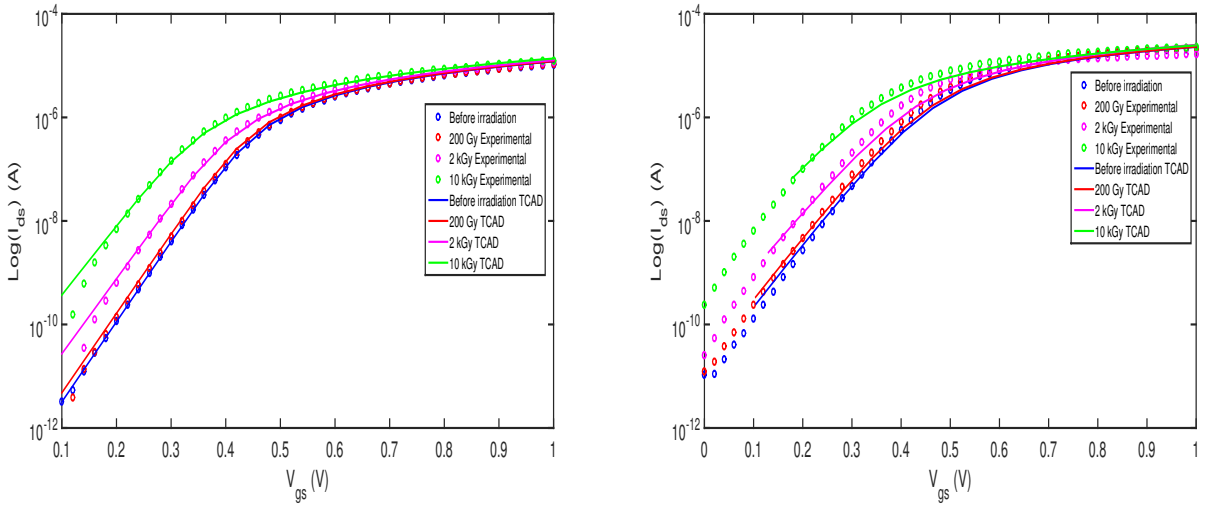
Wafer	Tr	Type	W (μ m)	L (μ m)	t_{ox}	E_a 150 °C	E_a 175 °C	E_a 200 °C	E_a 250 °C
W1	NMOS	LVT	1	1	GO1	0.795	0.85	0.91	0.945
W1	NMOS	LVT	0.21	0.03	GO1	0.794	0.852	0.963	1.004
W1	NMOS	RVT	1	1	GO1	0.806	0.875	0.925	0.982
W1	NMOS	RVT	0.21	0.03	GO1	0.822	0.91	0.984	1.1
W1	NMOS	LVT	2	2	GO2	0.798	0.922	0.965	0.995
W1	NMOS	RVT	0.21	0.1	GO1	0.803	0.865	0.93	0.96
W2	NMOS	LVT	1	1	GO1	0.837	0.872	0.958	0.985
W2	NMOS	LVT	0.21	0.03	GO1	0.839	0.846	0.928	1.04
W2	NMOS	RVT	1	1	GO1	0.849	0.871	0.956	0.99
W2	NMOS	RVT	0.21	0.03	GO1	0.8075	0.918	0.932	0.98
W2	NMOS	LVT	2	2	GO2	0.817	0.89	0.968	0.989
W2	NMOS	RVT	0.21	0.1	GO1	0.8425	0.864	0.963	0.9785

Table 4.7: Extracted activation energies of PMOS transistors.

Wafer	Tr	Type	W (μ m)	L (μ m)	t_{ox}	E_a 150 °C	E_a 175 °C	E_a 200 °C	E_a 250 °C
W1	PMOS	LVT	1	1	GO1	0.869	0.878	0.967	0.995
W1	PMOS	LVT	0.21	0.03	GO1	0.839	0.8935	0.948	1.025
W1	PMOS	RVT	1	1	GO1	0.898	0.94	0.97	1.02
W1	PMOS	RVT	0.21	0.03	GO1	0.89	0.906	0.97	1.016
W1	PMOS	LVT	2	2	GO2	0.872	0.9	0.942	1.055
W1	PMOS	RVT	0.21	0.1	GO1	0.817	0.889	0.95	1.03
W2	PMOS	LVT	1	1	GO1	0.87	0.877	0.967	0.997
W2	PMOS	LVT	0.21	0.03	GO1	0.89	0.962	0.982	1.075
W2	PMOS	RVT	1	1	GO1	0.847	0.918	1.003	1.005
W2	PMOS	RVT	0.21	0.03	GO1	0.847	0.88	0.944	1.043
W2	PMOS	LVT	2	2	GO2	0.86	0.896	0.961	1.026
W2	PMOS	RVT	0.21	0.1	GO1	0.832	0.918	0.987	0.998

4.5 TCAD validation of extracted parameters

A series of TCAD simulations were carried out taking into account the effects of N_{ot} in both oxides and D_{it} at both interfaces. We considered a uniform distribution of charge densities in the oxides and at the interfaces. Figure 4.21 shows the results of the TCAD simulation and the experimental measurements of two NMOS transistors irradiated at a maximum TID level of 10 kGy. In (a) an NMOS LVT $W = L = 1\mu m$ and in (b) a NMOS RVT transistor having $W = 0.21\ \mu m$, $L = 0.03\ \mu m$, both belonging to Wafer 2. Table 4.7 shows the TCAD simulation and the experimental measurements. Good agreement between TCAD and experience is observed at all irradiation levels, with a slight error in the subthreshold region due to sensitivity to noise and temperature of the measurements.



(a) NMOS1 W2.

(b) NMOS2 W2.

Figure 4.21: TCAD simulation and experimental measurements for different levels of TID.

Table 4.8: Comparison of experimental measurements and TCAD simulation.

Transistor	TID step	TCAD ΔV_{th}	Experimental ΔV_{th}	TCAD ΔSS	Experimental ΔSS
NMOS1	200 Gy	13	18	0.25	0.9
	2 kGy	113	110	1.95	2.2
	10 kGy	113	110	4.75	6.4
NMOS2	200 Gy	9	12	0.23	1.1
	2 kGy	48	52	2.23	2.7
	10 kGy	135	139	2.68	3.8

4.6 C-V measurements

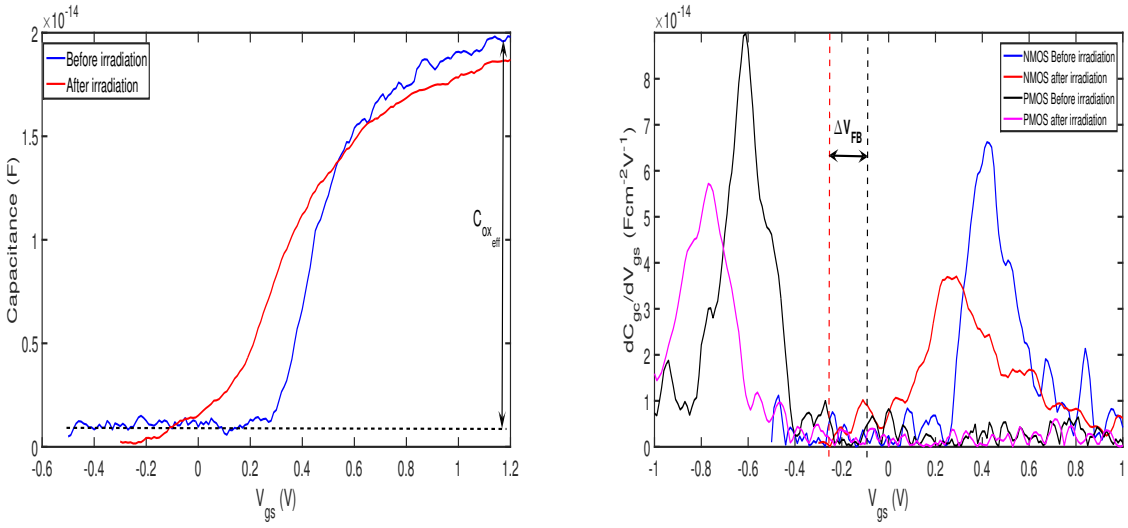
In addition to the I-V curves, a set of C-V curves was measured for each device. However, only measurements before and after irradiation were only made. On the other hand, a series of G(V) conductance measurements were carried out, but they had to be discarded due to a poor signal to noise ratio, which made it impossible to extract parameters from these curves.

From the experimental C-V measurements and using the techniques described in chapter 2, we extracted the parameters related to the equivalent oxide thickness EOT, the flat band voltage (V_{FB}), and the ΔV_{th} induced by the TID. Figure 4.22(a) shows the C-V curve of an NMOS transistor. From the extracted effective capacitance ($C_{ox_{eff}}$), we calculate EOT of the gate oxide.

$$EOT = \frac{e_{ox}}{C_{ox_{eff}}} \tag{4.4}$$

The extracted values correspond perfectly with those reported in the state of the art and by the manufacturer where GO1 varies between 1.7 nm and 1.9 nm and GO2 between 2.7 nm and 2.8 nm.

Figure 4.22 (b) shows the ΔV_{th} extracted with the technique described in chapter 2 for both NMOS and PMOS devices. The values obtained show good agreement with the values obtained with the Y-function. For NMOS devices, the values for the last irradiation step ranges between 90 mV and 120 mV for NMOS devices, and from 110 mV to 360 mV for PMOS devices on both wafers.



(a) Cgc NMOS W=L=1 μm.

(b) Derivative of C_{gc} respect to V_{gs}.

Figure 4.22: C-V measurements of a NMOS transistor before and after irradiation.

4.7 Conclusion of this chapter

In this chapter, we have described the experimental procedure and analyzed the behavior of FDSOI transistors under radiation. The effects of back gate bias and annealing applied to irradiated transistors have been investigated. We can conclude that, in all cases, a negative ΔV_{th} was noticed for both NMOS and PMOS transistors after irradiation. The PMOS transistors showed a larger degradation due to the addition of the contributions of N_{ot} and D_{it} that makes them more sensitive to the effects of radiation. We have demonstrated that thermal annealing is an effective technique to restore the electrical characteristics of FDSOI devices degraded by the TID. Nevertheless, a remaining threshold voltage degradation was observed for almost all irradiated devices, due to a residual N_{ot} and D_{it} charges located at deeper energy levels and that requires higher temperature to be detrapped. From the progressive charges detrapping as a function of the temperature, we can estimate the needed temperature for a complete regeneration could be comprised within the range of 275 °C and 300 °C. On the other hand, applying a back bias voltage has shown efficient results to compensate for threshold voltage degradation in both NMOS and PMOS types of transistors. However, there is a technological limit for V_{bg} value that has limited the compensation for some devices irradiated at a high dose level. In addition, this technique does not compensate for subthreshold slope degradation. To summarize the pros ans cons, thermal regeneration is effective when applying high temperature, but these elevated temperatures can affect the reliability of the circuits and electrical compensation is limited by the technology, and on the other hand, does not recover all radiation-induced degradation of FDSOI transistors. Both methods have advantages and limitations that must be taken into account when applying to a VLSI circuit.

Chapter 5

Total ionizing dose mitigation methodology for 28nm FDSOI devices and systems

The thermal regeneration and electrical compensation methods have been shown to be effective in reducing the impact of ionizing radiation on FDSOI devices. As was observed in the previous chapter, each method can partially regenerate or compensate for the degraded electrical characteristics of a transistor when applied individually. However, the residual degradation can be the cause of calculation errors, loss of operating frequency, as well as increased power consumption in an IC. For this reason, we propose a mixed hardening methodology based on the combination of both methods, in order to limit the damaging effects of TID on FDSOI transistors and reduce the effect of aging induced by high temperatures exposure.

We will use the models described in chapter 3, in order to simulate the degradation induced by TID in basic digital cells in addition to the proposed mixed hardening methodology to recover the performance of FDSOI circuits.

Furthermore, this mixed mitigation methodology will be experimentally tested on a DSP IC made with 28nm FDSOI technology. This will allow a study on the recovery of the operating frequency and the power consumption, two main parameters in the performance of an IC.

5.1 Mixed mitigation strategy description

The objective of the proposed method is to determine the parameters for having a mixed thermal and electrical treatment at a lower temperature. In addition, this mixed method reduces the negative impact on the device reliability due to the TID and to the high temperature. For that, we build a list containing at least one pair, formed by an annealing temperature T applied for a period Δt, and a back-gate voltage V_{bg}, to attenuate or eliminate the TID effects in a FDSOI transistor.

This characterization methodology is part of a proposed patent based on the works made in this thesis and it consists in a series of steps described as follows:

1. An electrical characterization of FDSOI transistors with different dimensions and gate oxides is made before irradiation. A set of initial curves I-V are obtained, then, from each curve, we can determine two fundamental parameters to monitor: the initial threshold voltage V_{th}, and the initial subthreshold slope SS. The tolerance parameters $V_{th_{Max}}$ and SS_{max} are chosen by the user depending on the target application. These two technological characteristics are key parameters of the performance and reliability of an integrated circuit based on MOS-type transistors. Any excessive variability in these characteristics can be fatal for the proper functioning of the circuit. Thus, the initial characteristic curve $(I_d(V_{gs})_0)$ represents a reference for normal operation of the transistor not exposed to radiation.

2. We expose each device to radiation to reach a predetermined TID level. So, the device previously characterized is degraded presenting a ΔV_{th}, ΔSS.

3. The electrical compensation is a priority, due to its low impact on the reliability of the device. Hence, we apply the electrical method V_{bg} to the transistor in order to compensate for the degradation induced by the TID. Then, we repeat step 1 to obtain a new $I_d(V_{gs})$ curve.

4. If the electrical method reaches its limit and is no longer efficient to cancel the TID-induced degradation, we apply an annealing cycle to the irradiated transistor for a specified time Δt. Once the thermal annealing cycle has finished, the electrical method is applied again for compensating the residual ΔV_{th}.

5. We repeat the steps 3) and 4) with increasing temperature steps. Thus, several iterations of the annealing steps, the electrical compensation and the measurement of the curves are carried out for a series of voltages V_{bg} at each temperature level. In other words, this step consists in applying different voltage values V_{bg} to the transistors and in measuring for each voltage value the characteristic curve $(I_d(V_{gs})_n)$ of the transistors for n varying from 1 to N for each temperature level. This makes it possible to obtain a set of curves $I_d(V_{gs})_n$ resulting from the combination of the annealing and electrical compensation.

6. The final step consists in comparing the set of curves $I_d(V_{gs})_n$ for n ranging from 1 to N with the initial characteristic curve $I_d(V_{gs})_0$ for determining the subset of curves which present less variation with respect to the initial curve. Therefore, this subset corresponds to the optimal treatment able to sufficiently heal the transistors following their exposure to radiations. A subset of optimal pairs (T, V_{bg}) is thus obtained with values composed of the applied annealing temperature and the applied back-gate voltage V_{bg} that satisfies the preset recovery criteria.

The complete process can be seen in the flow diagram displayed in Figure 5.1.

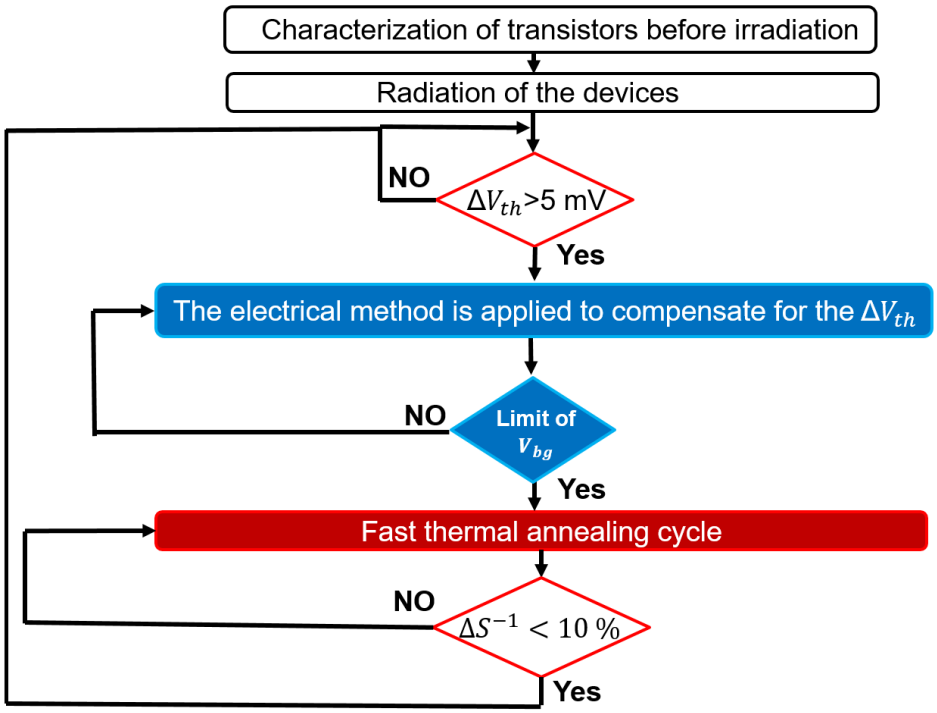


Figure 5.1: Mixed mitigation strategy flow diagram.

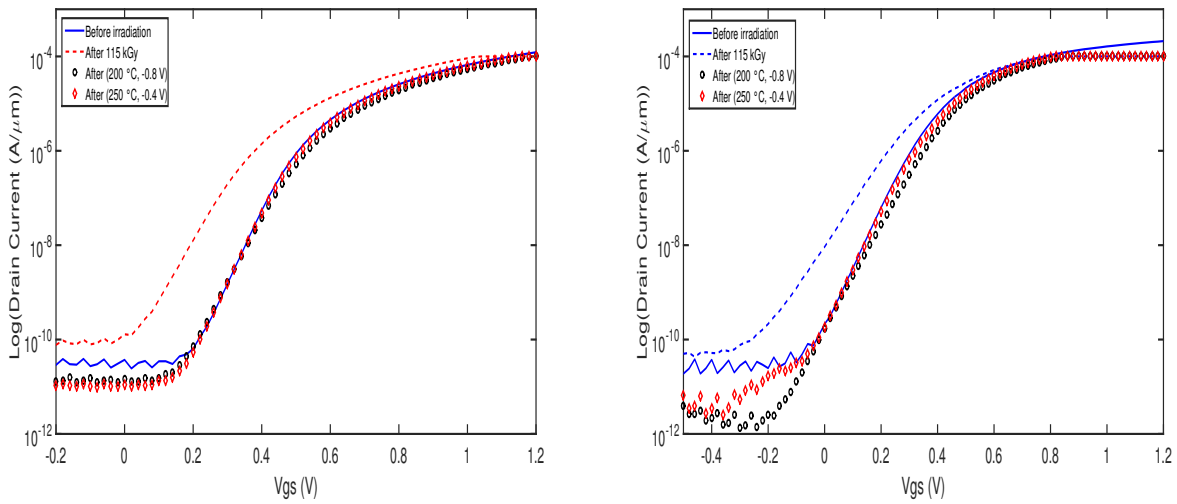
5.2 Evaluation of the mixed mitigation strategy on single FDSOI transistors

Due to their greater RBB range, RVT transistors are ideal candidates for the application of the proposed mixed mitigation methodology. As previously discussed, applying an RBB to an FDSOI transistor shifts its threshold voltage in a positive way, which allows the compensation of ionizing-induced degradation. For this reason, in this chapter, the mixed methodology will be applied only on irradiated RVT transistors belonging to W1 and W2. For our experiment, we have fixed tolerable degradation limits for the tested devices: $\Delta V_{th} \leq 5mV$ and $\Delta SS \leq 10\ \%\ (6\ mV/dec)$. We search the optimum couple (T, V_{bg}) that mitigates the effects of TID on FDSOI-RVT transistors

with the lowest possible temperature.

5.2.1 NMOS devices

Figure 5.2(a) shows the results of the mixed strategy applied to a NMOS4 W1 ($W = L = 1\mu m$) irradiated at 115 kGy. After an annealing cycle of 250 °C with a V_{bg} of -0.4 V we observe a total recovery of the threshold voltage degradation together with a remaining ΔSS of only 1.6 mV/dec. When the annealing temperature is reduced (T $\leq$ 200 °C), the RBB voltage must be enhanced from -0.4 V to -0.8 V to obtain the complete regeneration-compensation of the threshold voltage shift. With this lower temperature, the remaining ΔSS is about 5.8 mV/dec. Clearly, a trade-off between the annealing temperature and the subthreshold slope recovery has to be considered. The ΔSS may impact the operating frequency and this could not always be tolerated by the system. In this case, the annealing temperature/time should be increased.



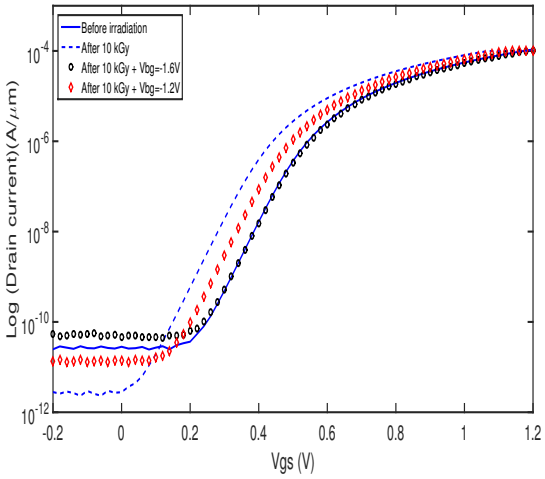
(a) NMOS4 W1 $W = L = 1\ \mu m$.

(b) NMOS5 W1 $W = 0.21\ \mu m,\ L = 0.03\ \mu m$.

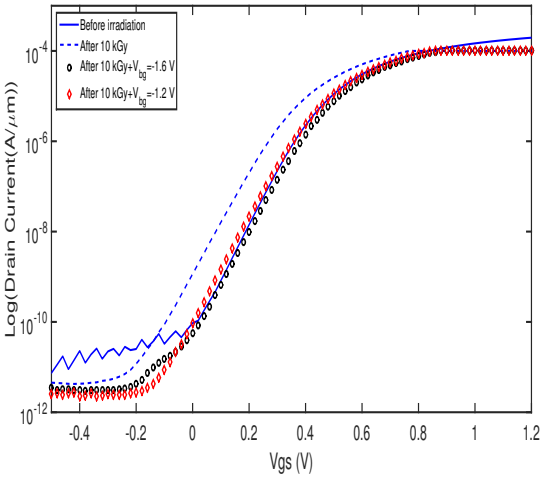
Figure 5.2: Mixed mitigation strategy of TID effects applied to NMOS RVT transistors.

Figure 5.2(b) shows the NMOS5 W1 transistor ($W = 0.21\ \mu m$, $L = 0.03\ \mu m$), in which the pairs (250 °C, -0.4 V) and (200°C, -0.8 V) satisfy the established regeneration-compensation criteria with the residual $\Delta V_{th_r} \leq 0.8\ mV$ and a $\Delta SS = 8.9\%$. The devices on W2, that were irradiated at 10 kGy, a much lower TID level than W1, present a smaller ΔV_{th}. At this dose level, the ΔV_{th} of NMOS4 and NMOS5 transistors can be recovered by only applying the electrical compensation as shown in Figure 5.3(a) and (b). We noticed in these devices that the subthreshold slope was not severely impacted by the TID, so we can recover the electrical characteristics by only using the compensation method. This can be explained by the predominance of trapped charges in the volume of oxides created at a low dose rate. After being trapped, these charges will begin to move slowly towards the interfaces. On the other hand, the charges created by a higher dose rate will have a tendency to occupy both interfaces more

quickly, which severely degrades the subtheshold slope as can be observed with W1 devices.

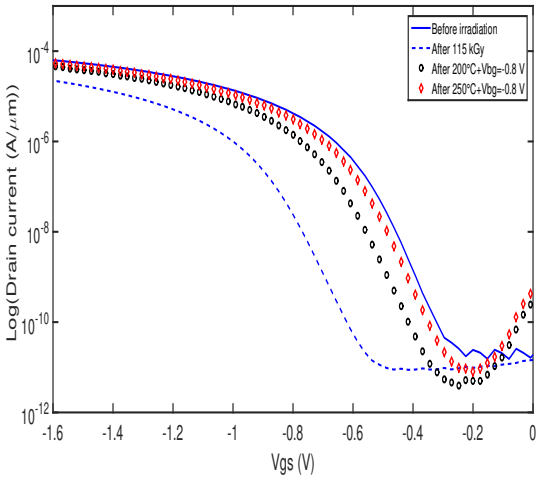


(a) NMOS4 W2 $W = L = 1\ \mu m$.

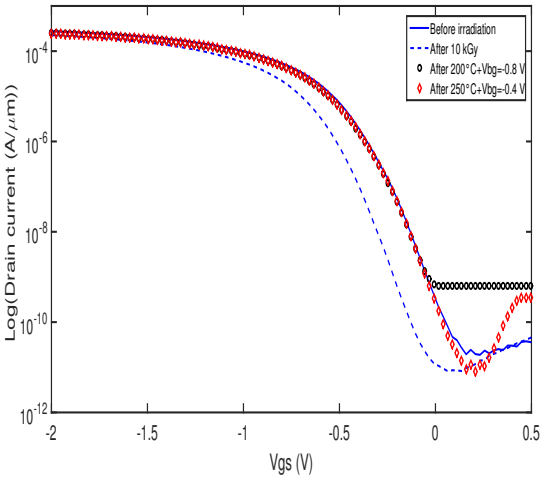


(b) NMOS5 W2 $W = 0.21\ \mu m,\ L = 0.03\ \mu m$.

Figure 5.3: Mixed mitigation strategy of TID effects applied to NMOS RVT transistors



(a) PMOS4 W1.



(b) PMOS5 W2.

Figure 5.4: Mixed mitigation strategy of TID effects applied to PMOS RVT transistors

5.2.2 PMOS devices

On both wafers W1 and W2, the PMOS transistors showed a higher ΔV_{th} than the NMOS transistors. The available RBB range is lower for PMOS transistors, compared to NMOS, then the application of a V_{bg} greater than -0.8 V puts the intra-substrate junctions into conduction. This can be seen in Figure 5.4(b), where an increase in the leakage current is observed. In (a) both recovery parameters were pushed to the limit. The pair (250 °C, -0.8 V) almost compensates-regenerates all threshold voltage degradation induced by radiation ($\Delta V_{th} = 281\ mV$). A residual

degradation ($\Delta V_{th} = 4.9\ mV$) is still observed but it satisfies the proposed recovery criteria. Due to their higher V_{th} degradation and reduced V_{bg} range compared to the NMOS transistors, PMOS transistors require a higher annealing temperature of 250 °C to reach a good recovery of their electrical parameters.

5.2.3 Optimal recovery parameters

We notice that for almost all transistors, NMOS and PMOS, we can reach the required mitigation level using an annealing temperature of 200 °C. In all devices, the leakage currents are partially or totally recovered, re-establishing their nominal power consumption. Table 5.1 summarizes the optimal (T, V_{bg}) pairs that efficiently regenerate-compensate the tested FDSOI-RVT devices and thus lower the residual degradation after applying the mixed methodology. The symbol "X" represents that only electrical compensation was sufficient to recover the electrical characteristics of the device.

Table 5.1: (T-V_{bg}) Optimum pair for mitigating TID effects on FDSOI-RVT transistors.

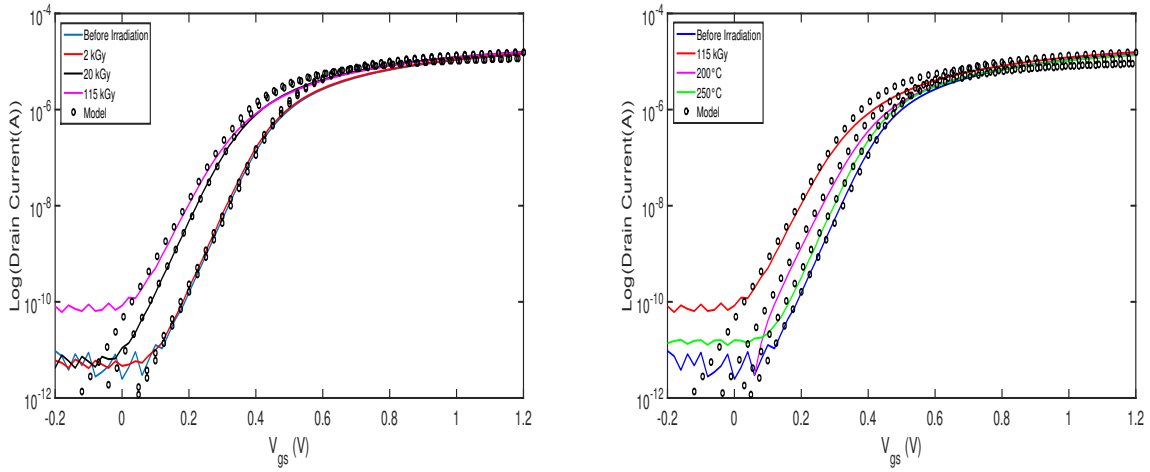
Transistors	T (°C)	V_{bg} (V)	$\Delta V_{thr}(mV)$	ΔSS_r (%)
NMOS4 W1	200	-0.8	0.6	9.8
NMOS5 W1	200	-0.8	0.8	8.9
PMOS4 W1	250	-0.8	4.9	4.8
PMOS5 W1	250	-0.8	2.3	7.6
NMOS4 W2	X	-1.6	0.3	4.2
NMOS5 W2	X	-1.6	1.6	7.7
PMOS4 W2	150	-0.4	3.5	8.1
PMOS5 W2	200	-0.4	1.3	8

5.2.4 Potential reliability issues

A thermal annealing can promote the detrapping of the radiation induced charges in the oxides. The higher the temperature, the greater the recovery of electrical characteristics. However, a high temperature can exacerbate phenomena such as negative bias temperature instability (NBTI) and electromigration [199] which induce a significant degradation and accelerated aging of the device. Other mechanical effects linked to the thermal expansion of the materials are potential issues when applying numerous thermal cycles at high temperature [200]. Therefore, prioritizing electrical compensation reduces the impact of thermal annealing cycles, safeguarding the reliability of the irradiated device. In contrast, the applied V_{bg} must not exceed the limits established by the manufacturer. The immediate effect would be the conduction of the intra-substrate junctions present in CMOS-FDSOI devices, which will result in a high increase of the power consumption in off-state as was observed in the Chapter 4.

5.3 Study of the effects of TID and thermal annealing on elementary circuits in SPICE

Figure 5.5(a) shows the simulation results of a NMOS transistor with $W = L = 1\ \mu m$ for various levels of TID. As previously described, the integration of N_{ot} affects the threshold voltage causing a negative shift. This is well reproduced with the proposed model where the greater the radiation level, the greater the ΔV_{th}. Furthermore the implementation of N_{it} model also reproduce a degradation of SS. On the other hand, the proposed detrapping model based on the thermal annealing cycles shows its effect on the same device. In Figure 5.5(b) we observe the regeneration efficiency. We plot the curve of the device before irradiation and after being irradiated at a high level of TID (blue and red lines). We apply a series of annealing cycles with temperatures between 150 °C and 250 °C where each applied temperature corresponds to a reached activation energy level. Thus, a progressive regeneration is observed as temperature increases. We can see on the graph that simulation data is consistent with experimental data.

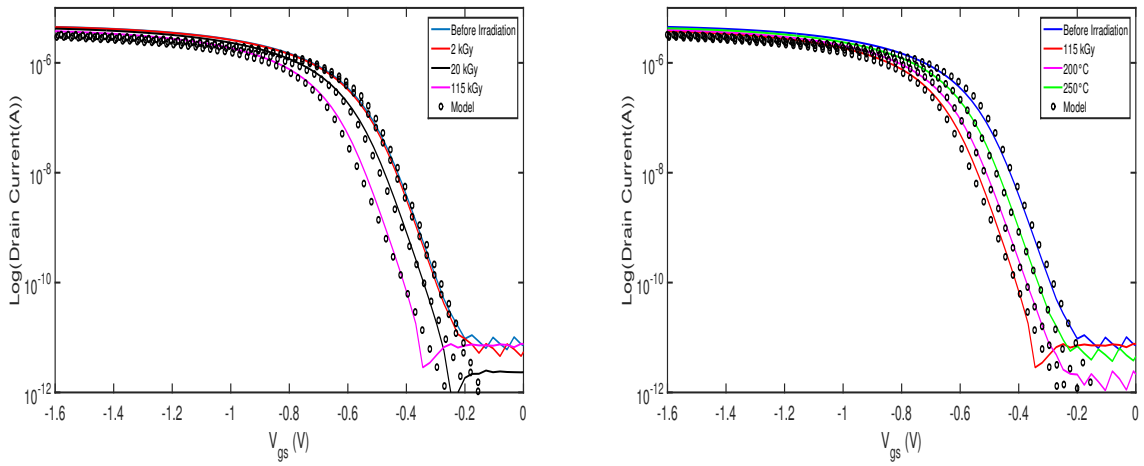


(a) Radiation response.

(b) Regeneration by applying annealing cycles.

Figure 5.5: Test of TID and thermal annealing physical models in a NMOS SPICE library.

The same series of simulations were performed on a PMOS device with $W = L = 1\ \mu m$. The same input parameters as the NMOS transistor were applied to the PMOS transistor. Figure 5.6(a) shows the progressive degradation of V_{th} and SS. As previously described, in the case of PMOS transistors, the degradation of V_{th} is more severe due to the addition of the contributions of N_{ot} and D_{it}. As expected, the progressive degradation of V_{th} was observed as well as the progressive regeneration with the application of each cycle of thermal annealing.



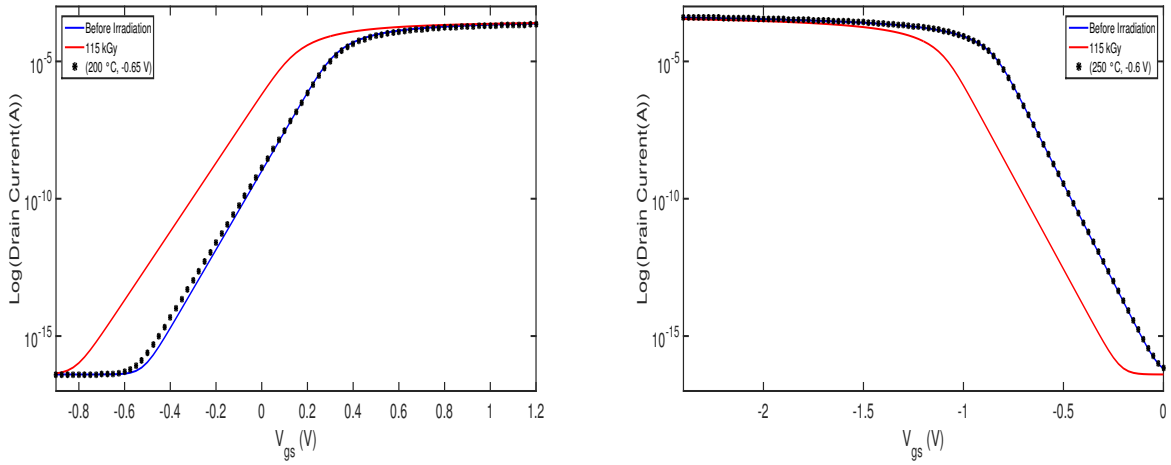
(a) Radiation response.

(b) Regeneration by annealing cycles.

Figure 5.6: Test of TID and thermal annealing physical models in a PMOS $W = L = 1\ \mu m$ SPICE library.

5.3.1 SPICE simulation of the mixed hardening methodology on elementary FDSOI transistors

Likewise, this mixed-method was implemented in SPICE following the physical models proposed in chapter 3. Figure 5.7 shows the NMOS and PMOS transistors for which the regeneration-compensation method was applied. In Figure 5.7(a), it is observed that the NMOS transistor irradiated at 115 kGy needs a pair (200 °C, -0.65 V) to satisfy the recovery criteria described in the proposed methodology.



(a) NMOS.

(b) PMOS.

Figure 5.7: Mixed mitigation methodology included in SPICE models of NMOS and PMOS FDSOI transistors

In (b) the PMOS transistor presents a greater ΔV_{th} as found with the experimental devices presented in Chapter

4. Thus, a pair (250 °C, -0.6 V) is necessary to satisfy the recovery criteria proposed in this methodology. The values of pairs (T, V_{bg}) are very close to the experimental values, which confirms the predictability of the proposed models.

5.3.2 Study of a MOSFET-FDSOI Inverter

In order to analyze the impact of the TID and the regeneration on a logic gate, we carried out the study of an inverting gate made with a NMOS transistor and a PMOS as shown in Figure 5.8. In the ideal case, applying a square logic signal at the input of this gate produces the same logic signal but inverted, that is, a logic 1 at the input produces a logic 0 at the output and vice versa. The response times of the passage from one state to the other are key parameters in the design of digital circuits and are directly linked to the responses of the transistors. The increase or decrease of these times can produce a variation in the operating frequency in addition to the power consumption in an IC. For this reason, the parameters to be monitored are the rise and fall time after applying various levels of TID, after applying the thermal annealing cycles and after applying different values of V_{bg}.

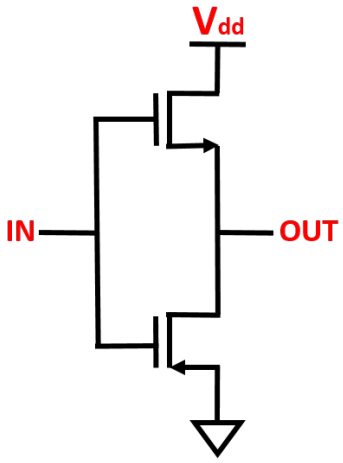
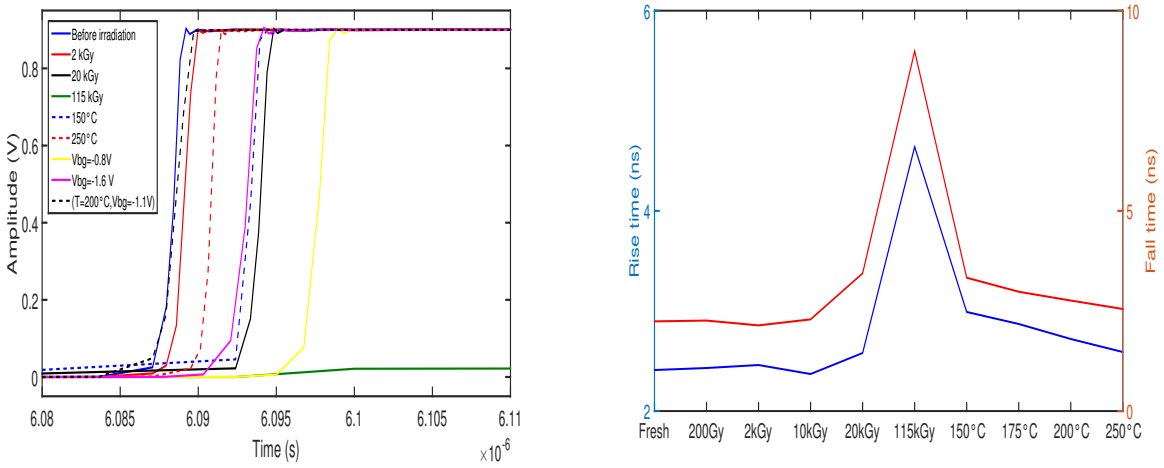


Figure 5.8: Schematic diagram of a CMOS-FDSOI Inverter.

Figure 5.9(a) shows the rise time of the gate. The application of 2 kGy of TID generates a delay in the response in addition to an increase in the rise time from 2.41 ns to 2.43 ns. At 20 kGy, the delay and rise time increase is even more significant going to a rise time of 2.58 ns. These effects are explained by the degradation of the electrical parameters of the transistors, which present a more severe ΔV_{th} and ΔSS with increasing TID levels. At the transistor level, the subthreshold slope degradation is responsible for these increases. This produces a slower response of the device in the transition from the ON to OFF state and vice versa. The delay is explained by the negative shift of V_{th} of both transistors. At a level of 115 kGy, the inverter gate is not able to change of state anymore because the electrical characteristics of both transistors show noticeable degradations.

The application of the annealing cycles produces an immediate effect in reducing the delay and the recovery of both the rising and falling times. In this case, after applying a cycle at 250 °C, the rise and fall times were almost completely recovered, which means that the subthreshold slope of both transistors was regenerated. However, at 250 °C an extra delay remains, this is because after the thermal annealing cycle, there is still a residual degradation of ΔV_{th} in the transistors, as previously shown in Figures 5.5 and 5.6. Figure 5.9(b) shows the dynamics of the rise and fall times, where it can be observed that, as expected, the higher the radiation level, the greater the delay in the response time of the gate. The observed peak represents the level at 115 kGy, where t_r is 4.64 ns, degraded around 200% with respect to its initial value, while the descent time showed a maximum degradation of 8.99 ns, around 400% degradation with respect to the initial value.



(a) Rise time.

(b) Rise and fall times after radiation and annealing.

Figure 5.9: simulation of the rise and fall time dynamics after radiation and annealing of an inverter gate.

5.3.3 Study of a Ring oscillator

The next stage is the simulation of a Ring Oscillator. These devices are composed of an odd number of inverter logic gates connected in series with positive feedback and are useful for synchronizing the computation process in digital systems and are also used to measure the effect of voltage and temperature on an IC [201]. So the desired frequency depends directly on the number of inverter stages and delay time of each inverter stage of the oscillator. The signal must go through each stage a second time to obtain the remaining phase shift, resulting in [201, 202]:

$$f_{osc} = \frac{1}{2\sum_{k=0}^{N} \tau_{d,k}} \tag{5.1}$$

With N the number of stages and τ_d the propagation delay due to the k element. In order to analyze the influence of the studied phenomena, radiation and temperature in these devices, we first develop a brief explanation of two main characteristics to take into account when designing an integrated circuit: the operating frequency and the

power consumption. There is a close link between these two characteristics. The total power consumption of an integrated circuit is the result of the contributions of the dynamic and static power consumptions. Hence:

$$P_{total} = P_{static} + P_{dynamic} \tag{5.2}$$

The dynamic power corresponds to the charging or discharging of internal capacitances as well as the short circuit current in logic gates. This short-circuit power is due to the fact that the rising and falling edges are not ideal that is, they are not instantaneous when switching from OFF to ON state as was observed in Figure 5.9. These commutations produce a simultaneous conduction of the P and N transistors of the CMOS devices, and in consequence a conduction path between the ground and the power supply [203].

The static power corresponds to power consumption when the circuit is in OFF state and there is no switching activity. It depends on the technological process of integration and represents a small part of the total power dissipated [204]. In an ideal IC, the static power should be zero, however, the subthreshold conduction through OFF transistors, leakage currents through P-N junctions, the tunneling current through gate oxide, the leakage current in the channel of the weakly blocked transistors are the main responsible for the increase of the power consumption.

Therefore, when ionizing radiation effects take place, a variation of the subthreshold slope of the transistors will produce a change in the switching response increasing the dynamic power. On the other hand, the excess of trapped charges in the oxides (mainly BOX and STI) will increase the leakage current I_{off}, then producing a potential rise in the static power of the device.

The TID-induced degradation of operating frequency has been previously studied in [205]. In this work, different RO fabricated in 28nm FDSOI were exposed to gamma radiation, leading to a decrease in their oscillation frequency. The analysis of the frequency variation is complex in these oscillators due to the different responses to the ionizing radiation of NMOS and PMOS transistors. As discussed in the case of the simulated inverter, the TID induces a delay in the response when the inverter goes from OFF to ON state. Since the frequency of oscillation of the ROs depends directly on the number of stages N and the delay τ as expressed in equation 5.1, it is expected that the frequency degradation is directly proportional to the delay produced by the TID, therefore:

$$\Delta f_{osc} = \frac{1}{2\sum_{k=0}^{N} \Delta\tau_{d,k}} \tag{5.3}$$

The operating frequency and the power consumption determine directly the performance of an IC. Consequently, an impact on the operating frequency will have an impact on the power consumption of the IC.

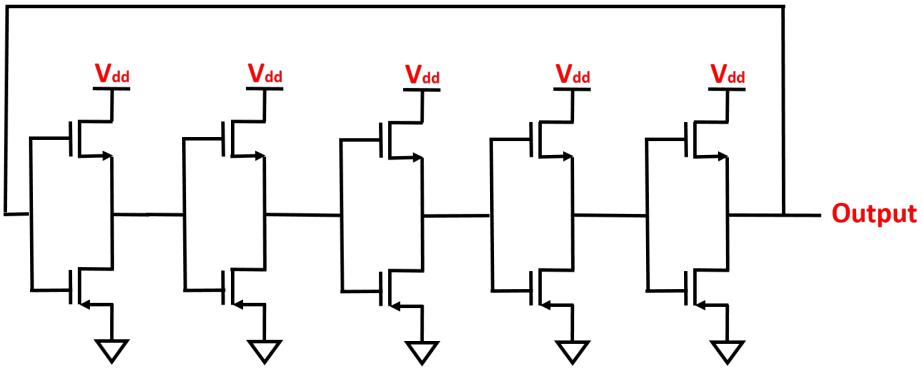
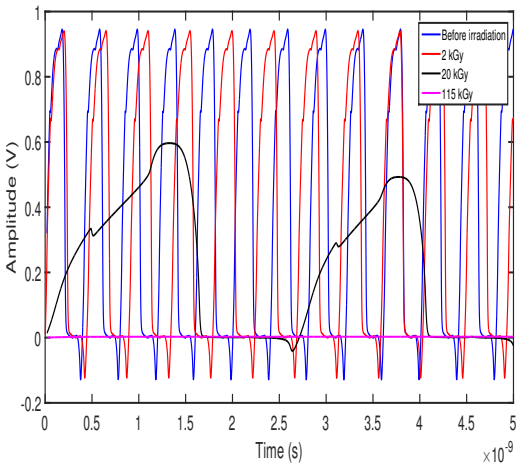
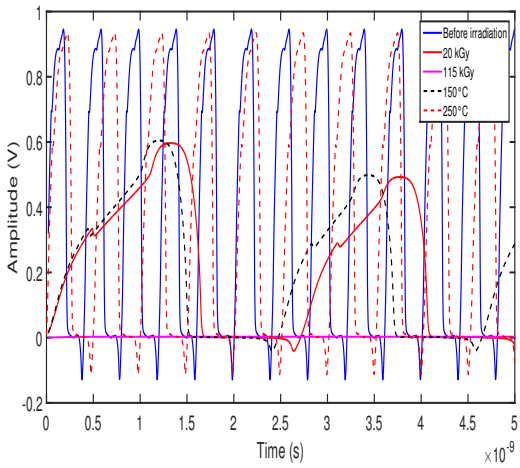


Figure 5.10: Schematic diagram of a five-stages Ring-Oscillator.

To analyze the behavior of a circuit exposed to TID, we will simulate a five-stage ring oscillator using the 28nm FDSOI transistors as shown in Figure 5.10. In this case, the parameters to be analyzed will be the oscillation frequency and the power consumption. In Figure 5.11(a) we observe the oscillation frequency of the RO. At 2 kGy, a degradation in frequency, product of the contributions of D_{it} and N_{ot} in addition to the reduction in the amplitude of oscillation, produces a reduction in the power consumption. A noticeable distortion of the signal, as well as a drastic reduction in the frequency and amplitude of the oscillation, are reported for a level of 20 kGy. The power consumption is drastically increased due to the rise of the power consumption going from 110 μW to 0.175 W. Finally, a total failure is observed at a level of 115 kGy.



(a) Oscillation frequency as function of the applied TID.



(b) Oscillation frequency as function of the applied annealing.

Figure 5.11: Oscillation frequency of the five-stages after radiation and annealing.

Figure 4.2(b) shows the progressive recovery of the oscillation frequency after application of each annealing cycle. The cycle at 250 °C almost recovers totally the oscillation frequency in addition to the amplitude of the signal. There is a residual degradation because the cycle at 250 °C is not sufficient to fully regenerate the electrical

characteristics of the transistors.

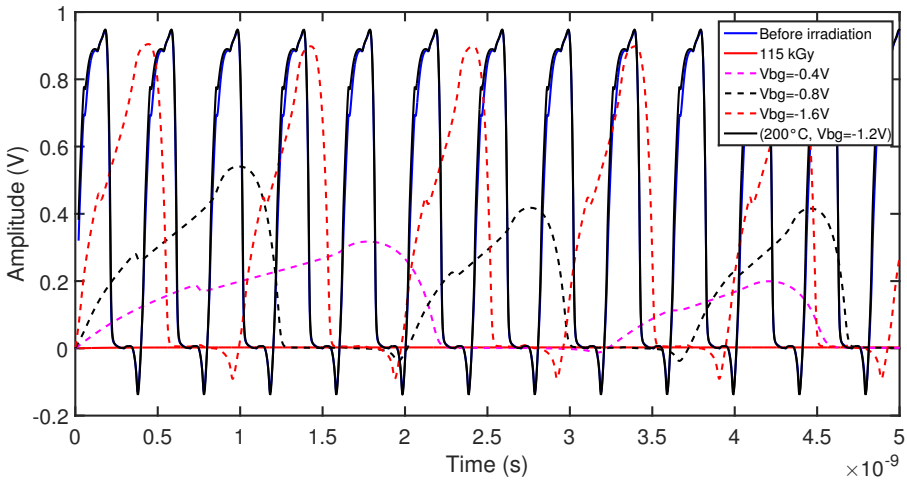


Figure 5.12: Evolution of an irradiated RO signal when applying different back-gate voltages, and when applying the mixed methodology.

Likewise, the influence of V_{bg} was simulated in the irradiated RO. Result of this simulations are displayed in Figure 5.12. First, a $V_{bg} = -0.4\ V$ partially re-establishes the operation of the RO from the total failure observed at 115 kGy, however, significant degradation of the amplitude of the oscillation signal as well as of its frequency is perceived. For a $V_{bg} = -0.8\ V$, the degradation in frequency and amplitude are still noticeable. By applying V_{bg} up to the established limit, $V_{bg} = -1.6\ V$, the amplitude of the oscillation signal is almost reestablished, nevertheless, an important frequency degradation is still observed. Furthermore, a significant distortion in the signal period is still observed. This confirms that the regeneration method is necessary to detrap the charges and reestablish the initial shape of the oscillation signal.

Table 5.2: Oscillation frequency and power consumption of the five-stages RO.

Dose and Temperature	Frequency (GHz)	Power (μW)
0 Gy	2.49	230
200 Gy	2.46	227
2000 Gy	2.23	203
10000 Gy	1.52	133
20000 Gy	1	85
115000 Gy	Fail	Fail
150 °C	1.08	88
175 °C	1.29	101
200 °C	1.52	132
250 °C	1.98	184
$V_{bg} = -0.4\ V$	0.45	6.61
$V_{bg} = -0.8\ V$	0.588	18.6
$V_{bg} = -1.6\ V$	1	86.5

From these facts, we conclude that neither regeneration nor compensation is sufficient to fully reestablish optimal oscillator performance when applied individually. One option would be to increase the annealing temperature, but this could severely damage the reliability of the component. In this way, after applying the regeneration-compensation method we managed to recover almost entirety the optimal functioning of the oscillator. For this, a couple (T = 200 °C, -1.2 V) must be applied after a level of 115 kGy of TID. Table 5.2 summarizes the oscillation frequencies and power consumption after each TID level and after each annealing cycle has been applied.

5.4 Implementation of the TID mitigation methodology

In order to implement practically the mixed methodology, we propose an electronic architecture able to reduce the effects of the TID, combining the regeneration by thermal annealing and electrical compensation. This architecture is part of the proposed patent based on the work made in this thesis. It allows the correction of the effects induced by the TID by using a combination of the two methods to extend the life-time of the FDSOI components under irradiation.

Moreover, this architecture ensures an automatic real-time electrical compensation where the applied V_{bg} value depends directly on the measurements of the TID. The thermal annealing cycle is triggered only when the applied V_{bg} reaches its limit. The proposed architecture is a control circuit designed around a feedback loop as can be seen in Figure 5.13. It includes:

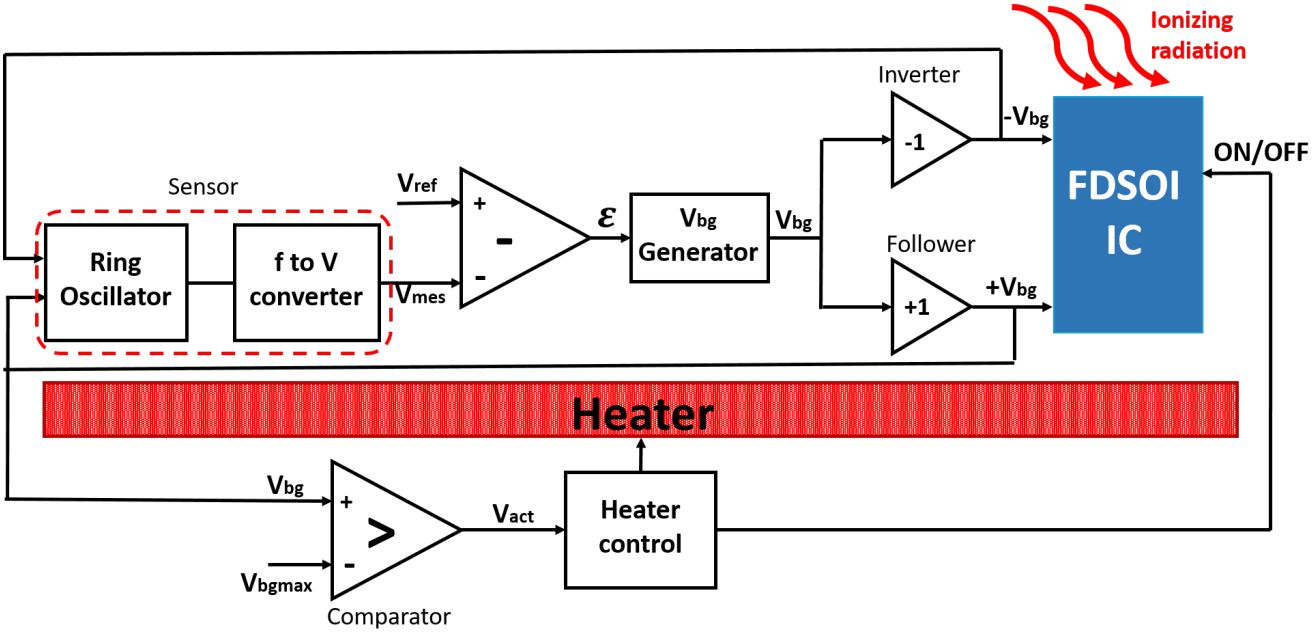


Figure 5.13: Architecture aimed to apply automatically the regeneration-compensation methodology applied to a FDSOI device.

1. A sensor block for generating a measurement signal as a function of an accumulated radiation dose resulting from the exposure of the integrated circuit to radiation. As described previously, a ring oscillator (RO) is commonly used to measure degradation in an IC. In this case, the RO circuit generates a periodic signal of frequency f_{osc}. In the absence of radiation exposure, the transistors that compose the RO circuit exhibit ideal characteristics. Under these initial conditions, the RO oscillates at an initial frequency denoted f_0.

   After radiation exposure, the NMOS and PMOS transistors in the oscillator undergo threshold voltage V_{th} and subthreshold slope SS variations. These variations translate into a shift in the RO frequency which is a function of the absorbed TID: $f_{osc} = f(Dose)$. So, this shift in frequency gives information about the absorbed dose in the protected FDSOI chip.

   Knowing that the delivered γ radiation dose is spatially uniform with respect to the whole system, and knowing that the RO is made with transistors based on the same microelectronic manufacturing technology (or same technological node) as those of the FDSOI integrated circuit IC, we can conclude that the degradation of the components in the RO is identical to those of the integrated circuit IC.

2. A frequency to voltage (f to V) converter is used to transform the frequency degradation $f_{osc} = f(Dose)$ into an electrical voltage V_{mes} variation.

3. The error detection block receives the converted signal V_{mes} and compares it with a constant reference signal V_{ref} supplied by an external voltage source. The reference voltage V_{ref} corresponds to the voltage value obtained at the output of the f to V converter before irradiation. The aim of this block is to generate an error signal ϵ which corresponds to the difference between the measurement and the reference $\epsilon = V_{ref} - V_{mes}$.

4. A V_{bg} generator for applying an absolute value of compensation voltage V_{bg} depending on the error signal $\epsilon = V_{ref} - V_{mes}$. The V_{bg} generator receives the error signal ϵ and generates a compensation voltage V_{bg} which is applied directly or inverted to the transistors of the IC in order to compensate for the effects induced by the TID. To achieve this operation, the V_{bg} generator circuit is designed to have a sufficiently high gain K (of the order of 10^3-10^4) for better precision. Then, the characteristic equation of the V_{bg} generator circuit is $V_{bg} = K.\epsilon$.

   As explained previously, it is not possible to increase the absolute value of the compensation voltage V_{bg} infinitely. Thus, the value of this voltage must be limited to a maximum value $V_{bg_{max}}$ via the addition of a voltage limiter in the V_{bg} generator circuit. The maximum value V_{bgmax} is defined according to the characteristics of the microelectronic manufacturing technology used for the realization of the system.

   The values of the compensation voltage to be applied for NMOS and PMOS type transistors may not be

identical in absolute value. However, it is possible to use a single generator circuit for both types of transistors thanks to the servo-control which provides an optimal averaged compensation. In the case where the integrated circuit IC comprises a plurality of types of transistors it is conceivable to use a plurality of V_{bg} generators each associated with a particular group of transistors.

With the help of the closed-loop servo-control, the compensation voltage V_{bg} is also applied on the transistors of the oscillator circuit to maintain the error signal ϵ at a value close to zero since the effect of the irradiation should be identical in the oscillator circuit. Thus the frequency f_{osc} of the periodic signal V_{osc} is maintained at a value close to the reference frequency f_0.

5. A follower amplifier stage is used at the output of the voltage generator to apply a positive compensation to the transistors, while voltage and an inverting amplifier stage used to apply a negative compensation voltage.

6. A comparator block activates the heating of the FDSOI circuit when the electrical compensation is no longer possible. The comparator is configured to activate the heating via the signal V_{act} to initiate an annealing cycle when the compensation voltage reaches its limit. The thermal annealing process first requires shutting down the entire integrated circuit IC but also the control circuit. The shutdown is controlled by the Heater control block following receipt of the activation signal V_{act}.

7. A heating element able to anneal the entire IC and the control circuit for a predetermined time and temperature. The heating circuit triggers an annealing cycle of the integrated circuit IC and the oscillator. The applied annealing cycles regenerate the transistors of the application circuit at a relatively low temperature ($\leq$200 °C) and for heating times of the order of a few tens of minutes, that is better than the values seen in the state of the art. For example, the heating circuit is configured to apply a temperature of 190 °C for 20 minutes.

8. After completion of the annealing cycle, the electrical treatment is restarted if the residual degradation can be compensated by V_{bg}, if not, a second annealing cycle is launched.

Both the methodology and the proposed architecture have the advantage of being able to immediately correct the effects of TID. When the device is being irradiated, the electrical method is a priority because its application does not affect the reliability of the device when it is applied within the established limits. The regeneration method by thermal annealing is only used if it is absolutely necessary, in this way, the life-time of the system can be prolonged during a mission in a radioactive environment.

5.5 Application example: 32 bit DSP 28nm FDSOI

As the mixed hardening methodology has shown great results in the recovery of the electrical characteristics degraded by TID on elementary FDSOI transistors, we prove the efficiency of the mitigation strategy when applied to a 32-bit digital signal processor (DSP) chip made with 28nm FDSOI degraded by gamma radiation.

5.5.1 Description of the devices

The device used for these experiments is a 32-bit DSP dedicated to Telecom applications [144]. It has been fabricated with STMicroelectronics 28nm FDSOI technology. The device includes the DSP and an automatic test harness as depicted in Figure 5.14. The DSP is designed with a Very Long Instruction Word (VLIW) architecture, which is well suited to Telecom applications. It is able to perform scalar and complex arithmetic operations and it embeds cordic/divide and compare/select functions. The architecture presents a pipeline depth of 10 stages in order to achieve more than 1.5 GHz at nominal voltage without using body bias. Two SRAM memories are used to feed the DSP core, one for the Program and the other for data interfaces. Each SRAM is organized in 1024 words of 32-bits.

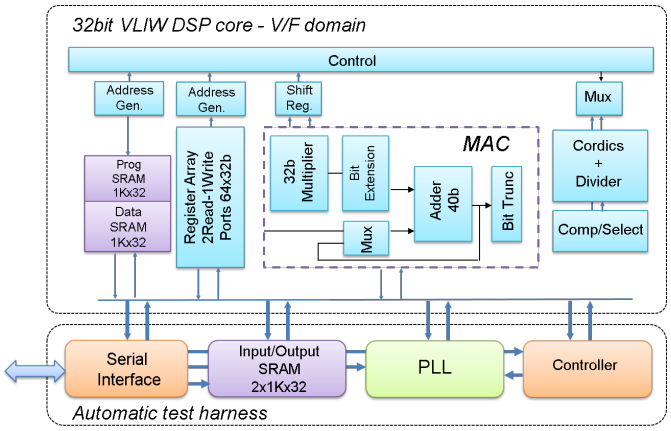


Figure 5.14: Block diagram of the 32-bit DSP FDSOI.

The automatic test harness is designed to drive the DSP core and to verify the correct result of every operation. Therefore, it is possible to detect the failure of the core and thus to measure the maximum clock frequency of the DSP as a function of the applied voltage. The harness is composed of a Phase Locked Loop (PLL) clock generator, SRAM memories a local controller and an interface. The interface is used to drive the test harness from a PC. It uses multiple commands to configure the DSP, the PLL and to read/write the SRAM memories. The PLL is used to generate the clock frequency to the DSP core. The PLL uses a dedicated different power supply pin to minimize the clock jitter, noise and to guarantee the normal operation even when the core is at low voltage. The SRAM memories on the harness contain the expected result of each DSP operation. Therefore, if the DSP computed

result differs from the expected result, an external signal is risen signaling the detection of an error.

The measurement of the circuit follow this sequence:

1. All SRAM memories are written.
2. The PLL is configured with the target frequency.
3. The voltage of the core is regulated to the target voltage.
4. The execution of the core is started.
5. The internal core results are collected.

If the current test success, another test is started with an operating frequency increased by 1 MHz. When the test fails, the results of the previous test give the maximum frequency of the circuit for the current applied voltage. A new frequency exploration is launched for each applied voltage after the PLL frequency has been initialized to its minimum frequency.

The circuit has been designed to achieve 2.6 GHz at 1.3 V when body bias is used. The test board is equipped with stabilized voltage regulators and measurement capabilities to measure the internal voltage of the circuit and the power consumption. The measurement of the power consumption is automatically triggered by the board when the test is started.

5.5.2 Experimental details

Twenty-four DSP 32-bits fabricated with 28nm FDSOI technology made by STMicroelectronics and CEA-LETI were irradiated at IRMA facility in Saclay, France, with a $^{60}Co\ \gamma - ray$ source. The devices were divided in four groups and placed at different locations in the irradiation chamber to observe the degradation of their electrical characteristics at different levels of TID. The dose was deposited in several steps to reach 128 kGy, 19.8 kGy, 12.8 kGy and 3.5 kGy in groups from 1 to 4, respectively. (see Table 5.3).

After the irradiation procedure, three isochronous thermal annealing cycles were applied to all devices for regeneration of their characteristics with temperatures of T_1 = 200 °C, T_2 = 250 °C and T_3= 300 °C and with a duration Δt of 23 minutes each. All devices were unbiased during irradiation and were measured immediately after each radiation step and after each thermal annealing cycle to evaluate the radiation effects and to observe the progressive regeneration on the degraded performances of the devices. The main measured parameters were the maximum operating frequency of the device f_{max} and the power consumption P, both available on the test bench display shown in Figure 5.15(a). This test bench is able to vary the supply voltage V_{dd} from 0.5 V to 1.3 V with a 0.05 V

step and the back-gate voltage V_{bg} between 0 to 2 V with a step of 0.5 V.

Table 5.3: Irradiation characteristics.

Devices	Dose-rate (Gy/h)	Time (h)	TID (kGy)
Group 1 (G1)	800	160	128
Group 2 (G2)	80	160	12.8
Group 3 (G3)	120	145	19.8
Group 4 (G4)	21	145	3.5

(a) Test-bench machine. (b) Test boards containing DSPs.

Figure 5.15: 32 bits DSP test material.

5.5.3 Performance degradation

After exposition of the test chips to ionizing radiation, a degradation of their performance was noticed, and in some cases, a total failure of the device. The latter was assumed when a loss of communication between the test chip and the test bench in charge of collecting the information was observed. Just before the total failure, we were able to determine the maximum TID level that this technology can tolerate. In the case of this test chip, the intrinsic resistance to ionizing radiation is around 5 kGy without applying any hardening technique. This means that a V_{bg} may eventually compensate for the performance degradation of the device only if the TID does not exceed this critical dose. Beyond a dose of 5 kGy, a thermal annealing becomes necessary.

5.5.4 Frequency (f_{max}) and power consumption (P) degradation after irradiation

As was previously discussed, there is a close link between the frequency and power consumption of an IC. A variation in frequency leads to a variation in the dynamic power consumption. During this experiment, we observed a slowdown in frequency of the device as shown in Figure 5.16 for doses below 1.4 kGy, and an increase in the frequency for higher radiation levels. The slowdown in frequency is explained by the degradation of the electrical characteristics of the transistors used in the device as was the case with the simulations of RO's previously pre-

sented. We assume that the increase in operating frequency beyond 1.4 kGy is the result of the degradation of elementary blocks in the PLL of the test chip, generating a raised frequency until a total failure.

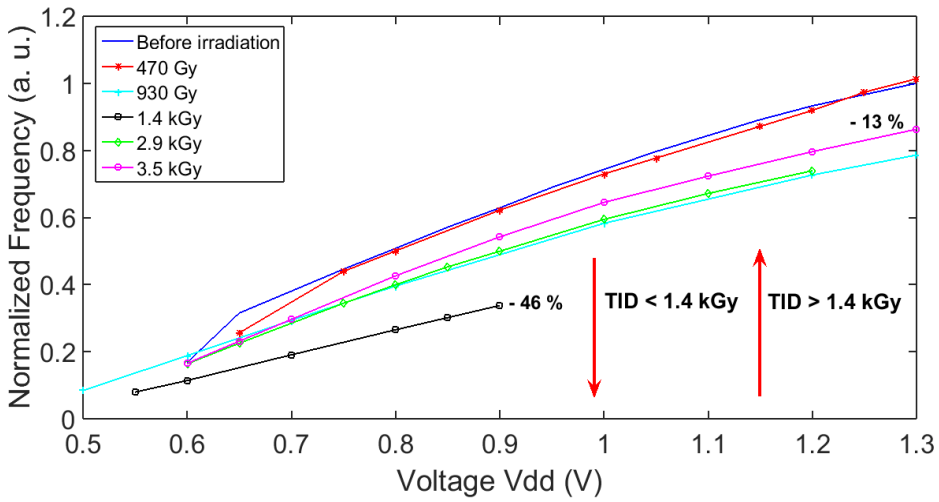


Figure 5.16: Frequency degradation at different TID levels.

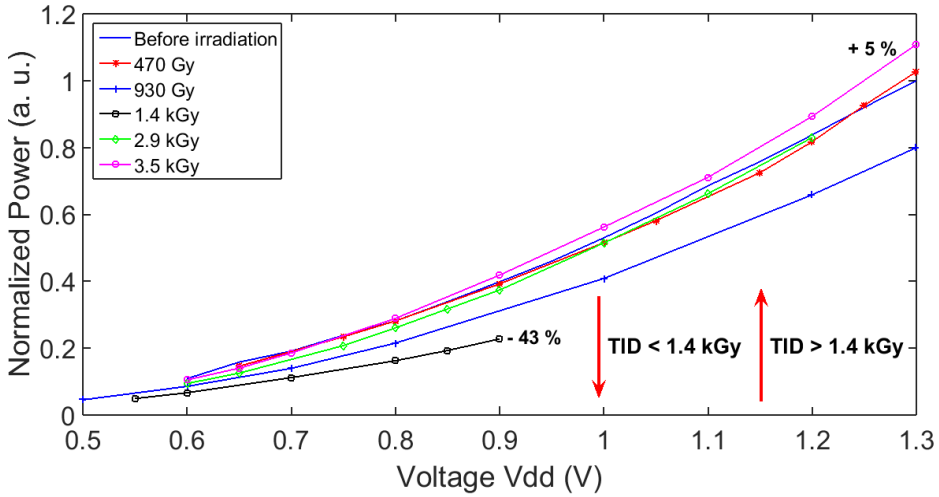


Figure 5.17: Power degradation at different TID levels.

Regarding the power consumption (Figure 5.17), we observed that for levels of TID below 1.4 kGy, the power consumed by the device tends to decrease. This is a direct consequence of the frequency behavior observed in Figure 5.16. Beyond this dose level, the power consumption of the device augments (green and pink lines) due to an increase in the leakage currents and the operating frequency. The leakage currents augment considerably with the dose due to the charges trapped in STI oxides and the degradation of V_{th}. Therefore the static power is much higher than the dynamic power after an exposure of the devices to high levels of TID. A maximum degradation of 43% is observed, together with the loss of functionality of the chip (black line).

5.5.5 Performance recovery

Figure 5.18 shows the recovery of the operating frequency when applying the proposed regeneration-compensation strategy to the test-chip. First, a total failure was noticed after the devices received 12.8 kGy. Applying a temperature of 200 °C with a back-bias of 0.5 V can partially recover the frequency degradation after the failure of the test chip. Applying a V_{bg} of 1 V and an annealing temperature of 200 °C ensures the good functioning of the test-chip. Annealing at 250 °C and 300 °C is also effective with a V_{bg} of 0.5 V, but increasing the temperature may reduce the reliability of the device.

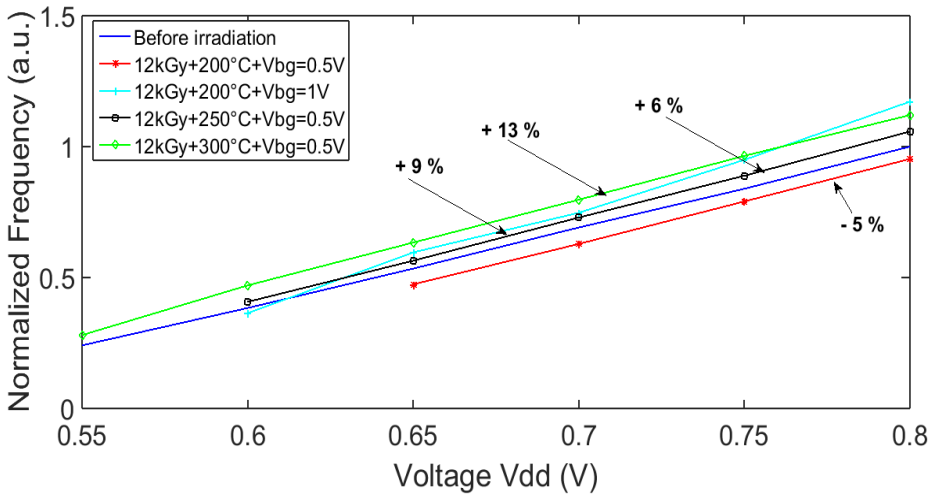


Figure 5.18: Frequency recovery after applying the T-V_{bg} method.

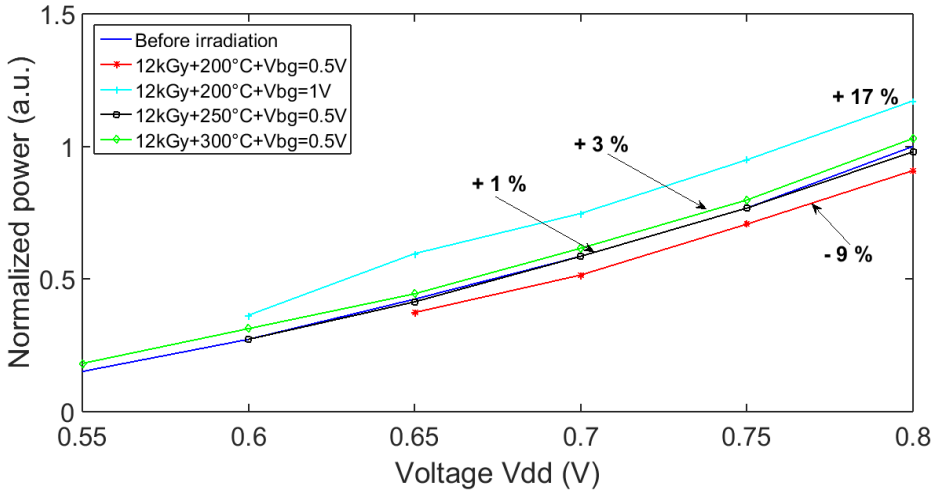


Figure 5.19: Power consumption recovery after applying the T-V_{bg} method.

Figure 5.19 shows the normalized power consumption, measured after applying the regeneration-compensation strategy. As expected, the method mitigates noticeably the effect of ionizing radiation on power consumption. This is due mainly to the annealing that enhances the evacuation of the trapped charges in the oxides and decreases,

therefore, the radiation induced leakage currents.

(T, V_{bg}) pairs for optimal recovery

Table 5.4 summarizes the pair (T-V_{bg}) necessary to regenerate-compensate for the degradation produced by the TID after each irradiation step. To minimize the effect of temperature on the reliability of the test chip, we have chosen those pairs where the temperature to be applied is the minimum value necessary to restart the test chip after the failure. In the case of test chips from Group 4 (G4), when the TID is lower than 5 kGy, an annealing temperature of 200 °C is sufficient to recover the device without applying a V_{bg}. However, an applied V_{bg} of 0.5 V has the same effect with no impact on the device reliability in order to revive the test chip. On the other hand, due to the high level of ionizing radiation reached by the devices of Group 1, a temperature above 200 °C had to be applied to revive the test chips. This is because the trapped charges in the oxides remain at deeper energy levels, so they need a higher temperature to be re-emitted.

Table 5.4: Recovery parameters.

Group/TID	Temperature (°C)	V_{bg} (V)
G1-128 kGy	250	0.5
G2-12.8 kGy	200	0.5-1
G3-19.8 kGy	200	0.5-1
G4-3.5 kGy	25	0.5

5.6 Conclusion of the chapter

We have proposed a new mixed hardening methodology that involves the combination of electrical compensation and thermal regeneration. Thus, we find the optimal match that reduces or eliminates the effects of TID on FDSOI devices. We have applied this method to elementary NMOS and PMOS FDSOI transistors and to a 32-bit DSP. Both experiments showed great effectiveness in recovering the performance of irradiated devices even at very high doses of TID. Compared with other recovery methods, which only focus on preventing the effects of radiation on devices, this method has the advantage of dynamically regenerating and correcting the electrical degradation produced by TID.

In addition, we have proposed an architecture to implement the methodology based on a control circuit including a RO as a sensor which variation in frequency can trigger the electrical method. In this way, the thermal method is only triggered when the electrical method reaches its limit. This has the great advantage of maintaining the device's reliability reducing the risk of damage caused by the repeated application of annealing cycles at very high temperatures. The combination of the two treatments offers a compromise between reliability and hardening

of the devices exposed to a prolonged irradiation and reduces the impact of the aging effects due to heating. This architecture ensures the robustness of the system when it is not always accessible, for example in a space application or in a nuclear power plant where human intervention is difficult or impossible during a mission.

The proposed physical models allowed us to carry out a series of SPICE simulations, and thus reproduce the behavior of the NMOS and PMOS transistors at different TID levels as well as the regeneration applying thermal annealing cycles. With this, we were able to observe the behavior of two fundamental blocks in digital electronics such as inverter gates and ring oscillators. As confirmed during the simulations, the TID causes delays when switching from one state to another as well as an increase in the rise and fall time in the inverter gate as a consequence of the ΔV_{th} and ΔSS of the transistors. This produces a reduction and distortion in the oscillation signal in an RO. The thermal annealing showed great efficiency in the partial recovery of the degraded electrical parameters at the transistor level, at the gate level, and at the circuit level. The V_{th} and SS, the rise, fall, and delay times of the inverting gate were partially regenerated, which was immediately reflected in a recovery in the frequency of oscillation of the RO. Based on these facts, we confirm that thermal regeneration is an effective technique, however, the temperature to be applied must be limited so as not to affect the reliability of the circuits subjected to radiation. For this, we use the electrical compensation by applying a back gate voltage in order to keep the annealing temperature as low as possible. The mixed hardening method show great effectiveness when applying to the simulated blocks, in this way, we are able to predict the degradation and recovery of elemental analog and digital circuits.

Conclusions

This study carried out on the FDSOI technology enabled us to clearly see the typical degradation induced by the TID. For all tested FDSOI transistors, we found that regarding the charges trapped in the oxide layers, the front gate oxide has a negligible influence due to its very small thickness, while the much thicker BOX is responsible for the strong threshold voltage shift. On the other hand, both interfaces $Si - SiO_2$ and $Si - BOX$, play an important role in the subthreshold slope degradation due to the presence of interface traps. During the study, we were able to integrate this behavior into a physical model for simulating the electrical degradation induced by very high doses of TID.

The proposed physical models, which were implemented in a FDSOI SPICE library, showed great efficiency to reproduce and predict the behavior of the main transistor parameters affected by the TID, i.e the threshold voltage and the subthreshold slope, as well as the regeneration provided by thermal annealing and the electrical compensation. This model was used to study the behavior of two elementary electronic circuits such as an inverter gate and a ring oscillator. In the inverter circuit, it was observed that the radiation effects induce a delay in the response in addition to affecting the rise and fall time. These effects were more noticeable in the RO, where a significant degradation in frequency and a variation in power consumption were observed during the simulations with increasing levels of TID until total failure. Furthermore, the TID-induced degradation, observed in the simulated RO (frequency and power consumption), could be confirmed experimentally in a 32-bit DSP made with 28nm FDSOI technology. However, during our experiments the elementary FDSOI transistors were irradiated without any biasing voltage applied. The fact that this configuration do not represent a worst case has been taken into account in the development of the physical models. In order to improve their efficiency, a larger series of transistors with different geometries should be irradiated under different biasing conditions. This would allow to do a statistical study for bettering the accuracy of the models. In addition, the study of the synergy between the temperature and and the applied V_{bg} during irradiation of FDSOI devices should be carried out in order to test the TID mitigation methodology proposed in this work.

With the work carried out during this thesis, we were able to propose a new mixed methodology to mitigate the effects of TID on FDSOI transistors. This mixed method was experimentally tested showing great effectiveness in recovering degraded electrical parameters. The method gave us a series of pairs (T, V_{bg}) satisfying two recovery parameters, $V_{th} \leq 5\ mV$ and $\Delta SS \leq 10\%$, from which we choose the one where the applied temperature is the lowest possible. We have simulated this mixed hardening method applied to NMOS and PMOS transistors as well as an inverter gate and a RO with the physical models implemented in the FDSOI SPICE library to observe the performance recovery. Like any hardening method, this method has advantages and drawbacks that must be taken into account. The first benefit of this methodology is the improvement of the resistance of FDSOI devices and dynamically correcting the effects due to ionizing radiation. Compared with other methods that use heat treatment, the regeneration-compensation method has the advantage of using relatively low temperatures, and only when necessary. The electrical method, using back-gate bias, allows to compensate for the negative shift of V_{th} degradation, without affecting component reliability when applied in the allowable range.

The regeneration method can be difficult to implement in embedded applications, because it requires adding heating resistors or metal heating plates in addition to circuits that limit the duration of the annealing cycle. During our annealing experiments carried out to observe the regeneration of the devices, an external heating source was used. This external source consisted of a hot air machine and an oven, so the internal temperature of the device could be slightly lower due to heat dissipation. Having a localized source of heat could improve de-trapping performance at a lower temperature, so new solutions should be explored to implement the regeneration method. Thermally insulated devices, such as SOI Devices, have been found to have a significant increase in temperature due to limited heat dissipation through the substrate. This effect, called Self-heating effect, is one of the issues to avoid when studying the scaling of a new SOI structure. However, and as it was treated in this thesis, a significant increase in temperature in an irradiated device could be beneficial to recover its electrical characteristics degraded by radiation.

Electrical compensation involves the application of V_{bg} in NMOS and PMOS transistors. However, the high density and the diversity of transistors in an IC is a factor to take into account when implementing this method. Two possible solutions can be proposed. The first is to apply a common V_{bg} which the value is determined from the degradation observed before in a series of NMOS and PMOS calibrations transistors, for this, a large number of devices with different characteristics, dimensions, oxide thickness should be characterized under different conditions. The common V_{bg} applied to all transistors is an optimum value that allows the total or partial compensation of the negative ΔV_{th} induced by the TID. The second solution involves a series of different V_{bg} generators, each compatible with a group of devices with similar characteristics. However this solution could have a significant cost on the total surface area of a silicon wafer.

Appendix A

First Appendix

A.1 Front and back-gate equations of a SOI structure

From the front and back-gate equations we have:

$$V_{gf} - \Phi_{msf} = V_{ox} + \Psi_{sf} \tag{A.1}$$

$$V_{gb} - \Phi_{msb} = V_{box} + \Psi_{sb} \tag{A.2}$$

First, we will analyze the front MOS structure. Using the Gauss theorem:

$$V_{ox} = \frac{\epsilon_s E_{sf}}{C_{ox}} \tag{A.3}$$

With E_{sf}:

$$E_{sf} = \frac{\Psi_{sf} - \Psi_{sb}}{t_{si}} \tag{A.4}$$

By replacing :

$$V_{gf} - \Phi_{msf} = \frac{\epsilon_s E_{sf}}{C_{ox}} + \Psi_{sf} \tag{A.5}$$

Developing and substituting in the equations:

$$V_{gf} - \Phi_{msf} = \frac{\epsilon_{si}}{C_{ox}}[\frac{\Psi_{sf} - \Psi_{sb}}{t_{si}} + \frac{Q_{dep}}{2\epsilon_{si}}] + \Psi_{sf} \tag{A.6}$$

$$V_{gf} - \Phi_{msf} = \frac{\epsilon_{si}}{C_{ox}}\frac{\Psi_{sf}}{t_{si}} - \frac{\epsilon_{si}}{C_{ox}}\frac{\Psi_{sb}}{t_{si}} + \frac{\epsilon_{si}}{C_{ox}}\frac{Q_{dep}}{2\epsilon_{si}} + \Psi_{sf} \tag{A.7}$$

Knowing that $C_{si} = \frac{\epsilon_{si}}{t_{si}}$:

$$V_{gf} - \Phi_{msf} = \frac{C_{si}}{C_{ox}}\Psi_{sf} - \frac{C_{si}}{C_{ox}}\Psi_{sb} + \frac{Q_{dep}}{2C_{ox}} + \Psi_{sf} \tag{A.8}$$

We regroup the terms and finally obtain the equation of the front gate voltage as a function of the front and back surface potentials.

$$V_{gf} - \Phi_{msf} = (1 + \frac{C_{si}}{C_{ox}})\Psi_{sf} - \frac{C_{si}}{C_{ox}}\Psi_{sb} + \frac{Q_{dep}}{2C_{ox}} \tag{A.9}$$

Following the same reflection, for V_{bg}, avec $V_{bg} = V_{box} + \Psi_{sb}$ et $V_{box} = \frac{\epsilon_{si}E_{sb}}{C_{box}}$ we obtain the equation relating to V_{bg}.

$$V_{bg} - \Phi_{msb} = (1 + \frac{C_{si}}{C_{box}})\Psi_{sb} - \frac{C_{si}}{C_{box}}\Psi_{sf} + \frac{Q_{dep}}{2C_{ox}} \tag{A.10}$$

A.2 Subthreshold Swing analysis

The subthreshold-swing is expressed as the inverse of the ratio between the drain current and the applied gate voltage then:

$$SS = \frac{dV_{gs}}{d(logI_{ds})} \tag{A.11}$$

We know that: $log_{10}(U) = \frac{ln(U)}{ln(10)}$, then we can write it in terms of surface potential as:

$$S^{-1} = \frac{kT}{q} ln10 \frac{dV_{gf}}{d\Psi_{sf}} \tag{A.12}$$

The front gate equation is given by:

$$V_{gf} - \Phi_{msf} = (1 + \frac{C_{si}}{C_{ox}})\Psi_{sf} - \frac{C_{si}}{C_{ox}}\Psi_{sb} + \frac{Q_s}{2C_{ox}} \tag{A.13}$$

And the back-gate equation:

$$V_{bg} - \Phi_{msb} = (1 + \frac{C_{si}}{C_{box}})\Psi_{sb} - \frac{C_{si}}{C_{box}}\Psi_{sf} + \frac{Q_s}{2C_{ox}} \tag{A.14}$$

From the equation V_{gb} we obtain the expression of Ψ_{sb} either:

$$\Psi_{sb} = \frac{V_{gb} - \Phi_{msb} + \frac{C_{sib}}{C_{box}}\Psi_{sf} + \frac{Q_s}{2C_{ox}}}{(1 + \frac{C_{sib}}{C_{box}})} \tag{A.15}$$

The contributions of interface states are expressed as $C_{sif} = C_{si} + C_{itf}$ and $C_{sib} = C_{si} + C_{itb}$

substituting in the equation V_{gf}

$$V_{gf} = \Phi_{msf} + (1 + \frac{C_{si}}{C_{ox}})\Psi_{sf} - \frac{C_{si}}{C_{ox}}[\frac{V_{gb} - \Phi_{msb} + \frac{C_{sib}}{C_{box}}\Psi_{sf} + \frac{Q_s}{2C_{ox}}}{(1 + \frac{C_{sib}}{C_{box}})}] + \frac{Q_s}{2C_{ox}} \tag{A.16}$$

The derivative $\frac{dV_{gf}}{d\Psi_f}$ is calculated:

$$\frac{dV_{gf}}{d\Psi_f} = (1 + \frac{C_{sif}}{C_{ox}}) - \frac{\frac{C_{si}^2}{C_{ox}C_{box}}}{(1 + \frac{Csib}{C_{ox}})} \tag{A.17}$$

Finally, the SS value is expressed as:

$$SS = \frac{kT}{q}ln10\frac{dV_{gf}}{d\Psi_{sf}} = \frac{kT}{q}ln10[(1 + \frac{C_{si}}{C_{ox}} + \frac{C_{itf}}{C_{ox}}) - \frac{\frac{C_{si}^2}{C_{ox}C_{box}}}{(1 + \frac{C_{si}}{C_{box}} + \frac{C_{itb}}{C_{box}})}] \tag{A.18}$$

A.3 Threshold voltage analysis

The inversion mode of the back gate allows a drain current to flow even if $V_{gf} \leq V_{Tf}^{inv}$, being useless for practical applications. Then, the proper mode of operation is when the applied back bias is either in depletion or accumulation mode. Therefore from the equation corresponding to the back-gate in accumulation mode we have:

$$V_{bg}^{acc} = \Phi_{msb} + \frac{C_{si}}{C_{ox}} 2\Phi_F - \frac{Q_{dep}}{2C_{ox}} \tag{A.19}$$

Subtracting the equation V_{bg} and V_{bg}^{acc}:

$$V_{bg} - V_{bg}^{acc} = (1 + \frac{C_{si}}{C_{ox}})\Psi_{sb} \tag{A.20}$$

Then, the back-surface potential is obtained, and expressed as:

$$\Psi_{sb} = \frac{C_{box}}{C_{si} + C_{box}}[V_{bg} - V_{bg}^{acc}] \tag{A.21}$$

In the same way, the back-gate equation is calculated in inversion mode as:

$$V_{bg}^{inv} = \Phi_{msb} + 2\Phi F - \frac{Q_{dep}}{2C_{ox}} \tag{A.22}$$

$$V_{gf} = \Phi_{msf} + (1 + \frac{C_{si}}{C_{ox}})2\Phi_F - \frac{C_{si}}{C_{ox}}\Psi_{sb} + \frac{Q_{dep}}{2C_{ox}} \tag{A.23}$$

We substitute the found value of Ψ_{sb}

$$V_{tf}^{D} = \Phi_{msf} + (1 + \frac{C_{si}}{C_{ox}})2\Phi_F - \frac{C_{si}}{C_{ox}}(\frac{C_{box}}{C_{si} + C_{box}}[V_{bg} - V_{bg}^{acc}]) + \frac{Q_{dep}}{2C_{ox}} \tag{A.24}$$

Finally, we obtain

$$V_{tf}^{D} = V_{Tf}^{A} - (\frac{C_{si}C_{box}}{C_{ox}(C_{si} + C_{itb} + C_{box})}[V_{bg} - V_{bg}^{acc}]) \tag{A.25}$$

Appendix B

Second Appendix

B.1 Thermal annealing model

From the general equation describing the detrapping rate after a thermal annealing, We have:

$$n(T) = n_0 exp(-A(\int_{T_0}^{T} exp(-\frac{E_{act}}{kT})dT) \tag{B.1}$$

Solving the integral I, and multiplying by $\frac{T^2}{T^2}$, we have:

$$I = -\int exp(-\frac{E_{act}}{kT})(\frac{T^2}{T^2})dT \tag{B.2}$$

The general solution to the integral in equation B.1 is of the form $\int x^n e^{ax} dx = \frac{x^n e^{ax}}{a} - \frac{n}{a}\int x^{n-1} e^{ax} dx$. Then, for our application. In our case, the solution to this integral I is:

$$I = \left[I_0 + \frac{k}{E_{act}} exp\left(-\frac{E_{act}}{kT}\right)\left[T^2 - \frac{2kT^3}{E_{act}} + \frac{6k^2T^4}{E_{act}^2} + ...\right]\right] \tag{B.3}$$

The terms subsequent to T^2 have a very small contribution to the value of the integral, therefore, considering that $T^2 >> \frac{2kT^3}{E_{act}} + \frac{6k^2T^4}{E_{act}^2} + ...$ we have an approximate solution to the integral given by:

$$I = \left[T_0^2 exp\left(-\frac{E_{act}}{kT_0}\right) + \frac{k}{E_{act}} exp\left(-\frac{E_{act}}{kT}\right)T^2\right] \tag{B.4}$$

Then the detrapping rate after a thermal annealing cycle is:

$$n(T) = n_0 exp(-\left(\frac{A}{c}\right) T^2 \left(\frac{k}{E_{act}}\right) exp(-\frac{E_{act}}{kT}) + T_0^2 exp(-\frac{E_{act}}{kT_0})) \tag{B.5}$$

B.2 Activation energy and characteristic temperature

From the general equation describing the detrapping rate after a thermal annealing:

$$n(T) = n_0 exp(-A(\int_{T_0}^{T} exp(-\frac{E_{act}}{kT})dT) \tag{B.6}$$

We define:

$$f(T) = -\frac{A}{c}\int_{T_0}^{T} exp(-\frac{E_{act}}{kT})dT \tag{B.7}$$

The first derivative of this equation is:

$$\frac{dn(T)}{dT} = n_0 exp(f(T))\frac{df(T)}{dT} = n(T)\frac{df(T)}{dT} \tag{B.8}$$

And the second derivative of $n(T)$:

$$\frac{dn^2(T)}{dT^2} = \frac{d^2 f(T)}{dT^2} n(T) + (\frac{df(T)}{dT})^2 n(T) \tag{B.9}$$

We calculate the first and second derivative of $f(T)$:

$$\frac{df(T)}{dT} = -\frac{A}{c} exp(-\frac{E_{act}}{kT}) \tag{B.10}$$

$$\frac{d^2 f(T)}{dT^2} = -\frac{AE_{act}}{ckT^2} exp(-\frac{E_{act}}{kT}) \tag{B.11}$$

$$-\frac{AE_{act}}{ckT^2} exp(-\frac{E_{act}}{kT}) + (\frac{A}{c})^2 exp(-\frac{2E_{act}}{kT}) = 0 \tag{B.12}$$

Finally, we find:

$$\frac{E_{act}}{kT} = ln(\frac{akT^2}{cE_{act}}) \tag{B.13}$$

Articles and patents

Scientific articles

- A New Mixed Hardening Methodology applied to a 28nm FDSOI 32-bits DSP Subjected to Gamma Radiation. A. Ureña Acuña, J. M. Armani, M. Slimani, I. Miro-Panades and P. Dollfus. Microelectronics Journal.
- A New Mixed Hardening Methodology applied to a 28nm FDSOI 32-bits DSP Subjected to Gamma Radiation. A. Ureña Acuña, J. M. Armani, M. Slimani, I. Miro-Panades and P. Dollfus. ESREF 2021.
- A Mixed Method to Mitigate the TID effects on 28nm FDSOI Transistors A. Ureña Acuña, J. M. Armani, M. Slimani, M. Cassé and P. Dollfus. RADECS 2020.
- Total Ionizing Dose Response of Commercial Off-The-Shelf Microcontrollers and Operational Amplifiers. J.M. Armani, S. Blairon, A. Urena-Acuna. RADECS 2020.
- THERMIC: a Hardened Temperature Controller for Regenerating CMOS Circuits Exposed to Ionizing Radiation. J.M. Armani, A. Urena Acuna, P. Dollfus, M. Slimani. RADECS 2020.

Patents

- Procédé de caractérisation de transistors pour l'atténuation d'effets d'irradiations sur un circuit intégré fabriqué en technologie SOI. A. Urena-Acuna, J.M. Armani, M. Slimani.
- Dispositif de correction des effets d'une dose ionisante sur un circuit intégré fabriqué en technologie SOI. A. Urena-Acuna, J.M. Armani, M. Slimani.

Résumé

Introduction

Les accidents nucléaires de Three Mile Island en 1979, de Tchernobyl en 1986 et de Fukushima en 2011 ont considérablement dynamisé le marché des appareils électroniques durcis au cours des 30 dernières années. La nécessité de réaliser des interventions dans des environnements difficiles tels que les sites nucléaires a suscité des recherches sur le développement de systèmes électroniques capables de résister à des niveaux élevés de rayonnements ionisants. De nombreuses études ont montré que les rayonnements ionisants provoquent des dysfonctionnements dans les systèmes électroniques, de la simple erreur de calcul au dysfonctionnement total de l'appareil. À l'échelle nanométrique, les rayonnements ionisants d'énergie élevée produisent des charges susceptibles d'être piégées dans les oxydes isolants du dispositif. Ces charges piégées produisent des dégradations électriques qui se manifestent dans les dispositifs MOSFET (Metal-Oxide-Semiconductor-Field-Effect Transistor) par un décalage négatif de la tension de seuil, un affaiblissement de la pente sous-seuil et une augmentation des courants de fuite. La résilience des systèmes électroniques à ces dégradations est essentielle dans les environnements radiatifs tels que l'espace, les centrales nucléaires ou dans le cas le moins souhaité des accidents nucléaires.

Ce travail vise à explorer deux axes de recherche dans le but d'étudier leur impact sur la récupération des caractéristiques électriques de dispositifs 28nm Fully-Depleted-Silicon-On-Insulator (FDSOI) ayant été exposés à des rayonnements ionisants. Cette thèse propose une nouvelle méthode de durcissement par régénération-compensation basée sur le dépiégeage des charges par application de cycles de recuit thermique d'une part et d'autre part sur la compensation électrique de la tension de seuil autorisée par la capacité inhérente à la technologie 28nm FDSOI d'appliquer une polarisation back-gate. Cette méthode a pu être validée par la modélisation physique des effets des rayonnements et des mécanismes de récupération, ainsi que par des expériences avec des dispositifs FDSOI. De plus, des simulations réalisées sur des cellules FDSOI basiques typiquement utilisées

dans les circuits numériques ont permis de prédire leur dégradation et leur récupération, renforçant ainsi la validation de la méthode de récupération proposée.

Effets radiatifs sur les dispositifs MOSFET

Lorsqu'une radiation ionisante (ex. rayons X ou γ) se présente sur un dispositif semiconducteur, des paires électron-trou sont créées sur la surface d'impact. Une fraction de ces paires se recombine et les porteurs libres restants sont transportés dans l'oxyde vers l'interface oxyde-semiconducteur. Les électrons, qui sont relativement mobiles dans l'oxyde de silicium, vont être évacués, conduits par le champ électrique induit par la tension de grille. D'autre part, les trous, du fait de leur très faible mobilité vont rester immobiles et piégés dans le volume des oxydes isolants du transistor. Ainsi, les charges piégées se déplaceront en sauts discrets (de piège en piège) jusqu'à atteindre l'interface. Les mécanismes physiques qui interviennent dans la création de défauts d'ionisation dans le SiO_2 sont illustrés dans la Figure B.1.

Nous parlons donc d'une part de la densité des charges piégées dans le volume des oxydes (N_{ot}) et d'autre part de la densité (N_{it}) de charges piégées aux interfaces entre les couches de silicium et d'oxyde isolant (couramment appelé interface $Si - SiO_2$) [180].

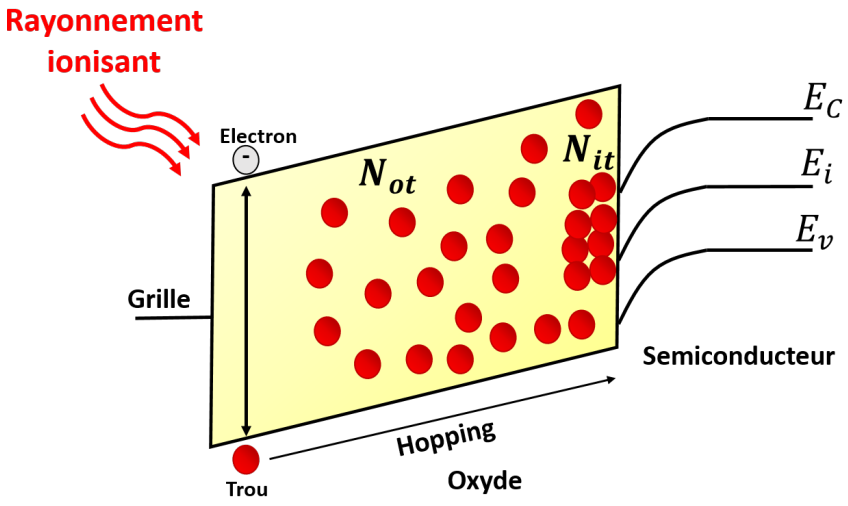


Figure B.1: Modèle des effets du rayonnement dans les oxydes.

Les charges piégées dans les oxydes produisent un comportement anormal sur les caractéristiques électriques du transistor. L'effet le plus significatif est le décalage de la tension de seuil qui deviendra de plus en plus négative

dans les deux types de transistor MOSFET, le NMOS et le PMOS. Ce décalage est dû principalement aux charges piégées dans les oxydes isolants de grille et de l'oxyde enterré "BOX". Un deuxième effet se manifeste dans la pente sous-seuil SS, qui augmente en raison de la présence de charges piégées aux interfaces $Si - SiO_2$[27, 46]. Le troisième effet électrique qui est présent lorsqu'un transistor est irradié est l'augmentation du courant de fuite I_{off} à cause des charges piégées dans les oxydes isolants STI (Shallow-Trech Isolation) situés sur les côtés du transistor et dont la fonction est de séparer les transistors NMOS et PMOS [206].

On retrouve ces défaillances à la fois dans les transistors NMOS et PMOS. Dans les dispositifs NMOS, le ΔV_{th} négatif rend le transistor capable de s'activer avec une tension de grille inférieure jusqu'à la perte de contrôle du canal, c'est-à-dire lorsque le transistor devient conducteur alors qu'aucune tension de grille n'est appliquée. Pour un transistor PMOS, l'excès de charges piégées d'oxyde conduit également à un ΔV_{th} négatif. Dans ce cas, le transistor devient plus difficile à mettre en conduction [2, 4]. La Figure B.2 montre ces effets sur les caractéristiques I-V d'un transistor avant et après avoir été soumis à un rayonnement ionisant.

Ainsi, le décalage de la tension de seuil est modélisée par le décalage provoqué par les charges piégés dans l'oxyde et les charges piégés dans l'interface.

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} \tag{B.14}$$

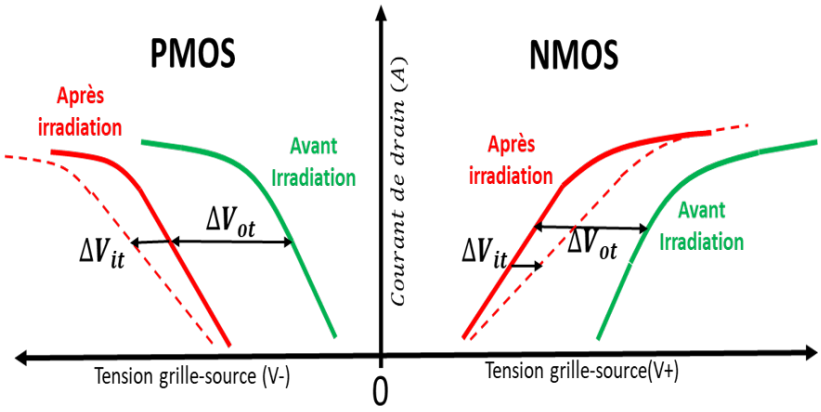


Figure B.2: Effet des charges piégées dans l'oxyde et dans l'interface sur la tension de seuil des transistors NMOS et PMOS.

Mécanismes de récupération et compensation des transistors MOSFET FDSOI irradiés

Dans le but de récupérer les caractéristiques électriques dégradées par le rayonnement, deux phénomènes de récupération seront étudiés dans ce travail, la régénération en appliquant des cycles de recuit thermique et la compensation électrique en appliquant une tension de grille arrière V_{bg}.

Recuit thermique

Le dépiegeage des charges est un phénomène qui peut se produire lentement à température ambiante et qui pourrait être accéléré en augmentant la température [137, 138]. Plus la température est élevée, plus le taux de dépiégeage de charge est élevé et par conséquent plus la récupération des caractéristiques électriques initiales d'un transistor irradié est rapide. Ainsi, la récupération par activation thermique a été modélisée comme un front horizontal qui se déplace de la bande de valence à la bande de conduction à l'intérieur de la bande interdite de l'oxyde comme le montre la Figure B.3. Ce modèle indique que les charges situées entre le haut de la bande de valence et le front thermique sont neutralisées, tandis que celles situées au-delà du front restent actives, et par conséquent, les trous restent piégés [136].

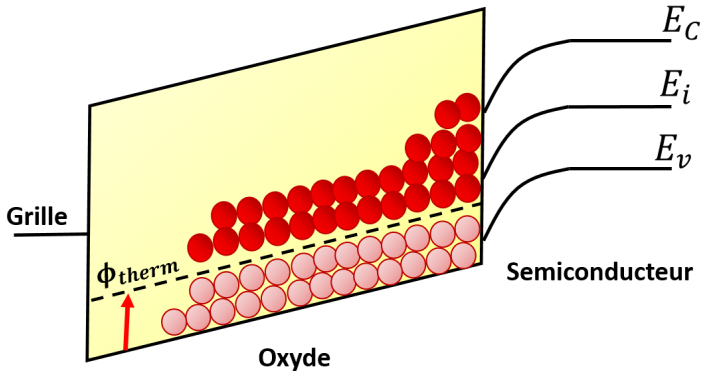


Figure B.3: Modèle de recuit thermique.

La position du front thermique peut être estimée en supposant que le depiegeage des charges est une réaction chimique du premier ordre [113] où la probabilité $\sigma_{thermique}$ qu'une charge soit détruite suit la loi d'Arrhenius [140].

$$\sigma_{thermique} = Aexp(-\frac{E_{act}}{kT}) \tag{B.15}$$

Où A est le facteur de fréquence (s^{-1}), E_{act} est l'énergie d'activation (eV), k est la constante de Boltzmann (eVK^{-1}) et T est la température absolue (K). Afin d'atteindre une énergie d'activation spécifique, le temps et la

température de recuit doivent être choisis suivant l'équivalence temps-température comme dans [138]. On peut réécrire l'équation B.15 pour introduire la constante de temps $\tau = \frac{1}{\sigma_{thermique}}$ et $\Phi_{thermique}$ la position du front thermique pour atteindre une énergie d'activation spécifique [136]:

$$\Phi_{thermique} = kTln(A\tau) \tag{B.16}$$

Compensation de tension de seuil

La compensation électrique est basée sur l'effet de couplage électrostatique entre grille avant et grille arrière qui permet le contrôle de la tension de seuil d'un transistor FDSOI. Le réglage de la tension de grille arrière V_{bg} décale la tension de seuil avant vers des valeurs plus positives ou négatives [143]. Lorsqu'un V_{bg} positif est appliqué, les électrons dans la couche de silicium sont attirés vers l'interface $Si - BOX$, formant un deuxième canal de conduction. Ceci a un impact sur le potentiel de la surface avant et la conséquence directe est une charge d'inversion plus élevée dans le canal de conduction principal qui induit un décalage négatif de V_{th}. Ce cas est appelé Forward Body-Bias (FBB). D'autre part, si un V_{bg} négatif est appliqué, les électrons de la couche de silicium intrinsèque sont repoussés vers l'interface $Si - SiO_2$ du transistor avant formant un canal plus conducteur. Le potentiel de surface avant est augmenté, produisant un décalage positif de la tension de seuil. Ce cas de polarisation s'appelle Reverse Body-Bias (RBB). L'effet sur la tension de seuil dans les deux cas peut être observé sur la Figure B.4.

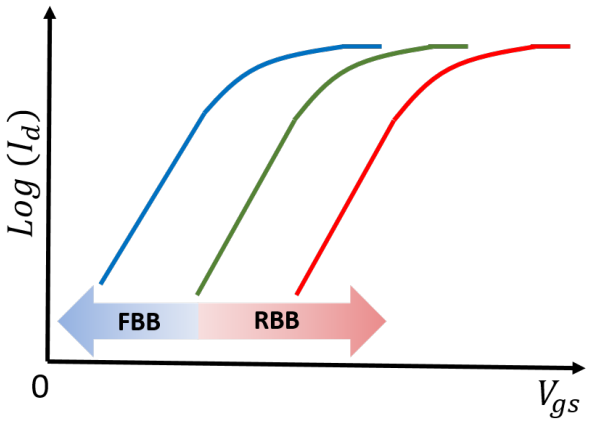


Figure B.4: Modulation de tension de seuil en appliquant un V_{bg}.

Compte tenu de cette propriété intrinsèque de la technologie FDSOI, on peut en déduire qu'un RBB peut compenser totalement ou partiellement le ΔV_{th} négatif induit par le TID. Il faut mentionner que ces effets compensent le ΔV_{th} négatif induit par les charges piégées d'oxyde mais pas la dégradation de la pente sous-seuil causée par les charges piégées d'interface. De même, la capacité de compensation dépend directement du coefficient n, qui

est directement lié aux capacités du dispositif comme décrit dans l'équation B.17:

$$n = \frac{C_{si}C_{box}}{C_{ox}(C_{si} + C_{box})} \tag{B.17}$$

Avec C_{si} la capacitance de la couche de silicium intrinsèque,C_{ox} la capacitance de l'oxyde de grille et C_{box} la capacitance de l'oxyde enterré BOX. Pour la technologie 28nm FDSOI, n varie entre 80 et 85 mV/V [144].

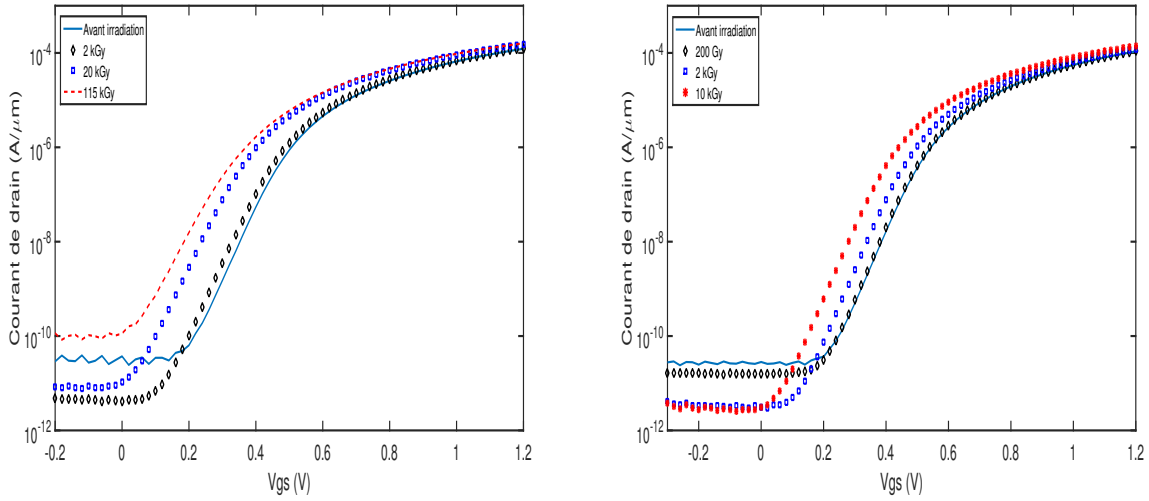
Résultats expérimentaux

Pour observer leurs réponses au rayonnement, vingt-quatre transistors FDSOI de 28 nm avec des dimensions larges-longues et courtes-étroites, différents substrats (LVT et RVT) et différentes épaisseurs d'oxyde de grille (GO1 et GO2) ont été testés. Les transistors ont été irradiés avec une source de rayons $^{60}Co\ \gamma$. Deux échantillons avec les mêmes transistors ont été placées à des distances différentes de la source afin d'observer l'effet du débit de dose sur les dispositifs. Les wafers W1 et W2 ont été exposées à un débit de dose de 1,3 kGy/h (36,1 rad/s) et 115 Gy/h (3,2 rad/s) pour finalement atteindre 115 kGy (11,5 Mrad) et 10 kGy (1 Mrad), respectivement.

Une caractérisation électrique de chaque dispositif a été réalisée avant irradiation afin d'avoir un point de référence. Les courbes $I - V$ pour différentes valeurs de V_{bg} ont été obtenues en utilisant l'analyseur de paramètres à semi-conducteurs. Afin d'observer et de caractériser la régénération progressive des transistors FDSOI dégradés par TID, nous avons appliqué aux dispositifs testés quatre cycles de recuit thermique isochrone après chaque étape d'irradiation. Les températures de ces cycles étaient de 150 °C, 175 °C, 200 °C et 250 °C. La durée de chaque cycle était fixée à 18 minutes pour atteindre une énergie d'activation de 1 eV avec la température la plus élevée. Les mesures électriques ont été immédiatement effectuées à température ambiante après l'application de chaque cycle de recuit.

Irradiation

La Figure B.5 montre une caractéristique $I_d(V_{gs})$ d'un transistor NMOS à canal long correspondant à W1, irradié à 1,3 kGy/h, et le même transistor NMOS à long canal de W2 irradié à 115 Gy/h. Après chaque palier d'irradiation appliqué, les transistors FDSOI ont présenté une dégradation typique de chaque niveau de TID: un décalage négatif de la tension de seuil, une dégradation de la pente sous-seuil et une augmentation des courants de fuite ont été observées.

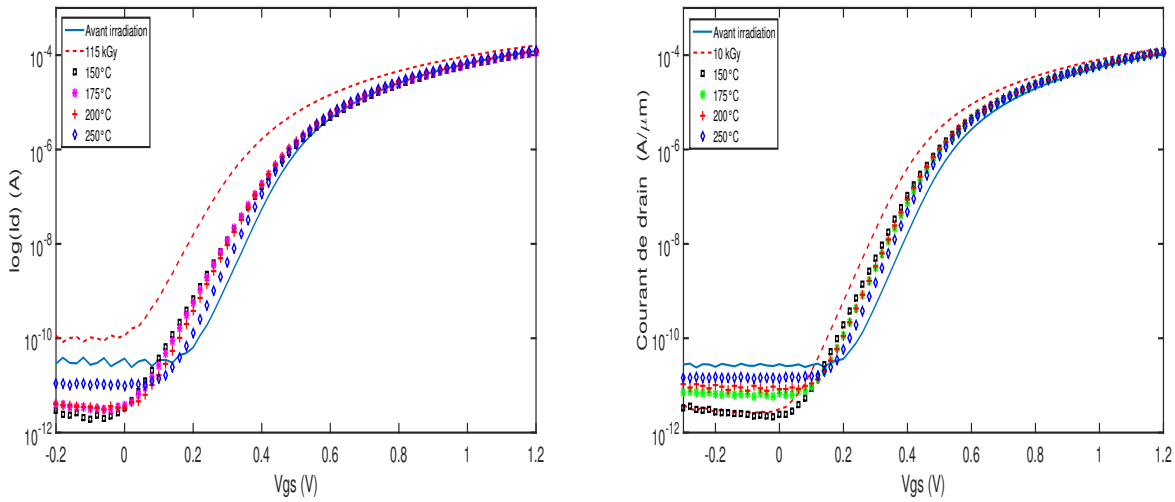


(a) NMOS W1. (b) NMOS W2.

Figure B.5: Réponse de rayonnement d'un transistor NMOS LVT $W = L = 1\ \mu m$.

Recuit thermique

La Figure B.6 montre la réponse des mêmes transistors NMOS $W = L = 1\ \mu m$ de W1 et W2 après irradiation et après chaque cycle de recuit. Les deux dispositifs NMOS de W1 et W2 présentent une régénération progressive. Cependant, même après recuit à 250 °C, un décalage de tension de seuil résiduel subsiste en raison des charges piégées à des niveaux d'énergie plus profonds et qui n'ont pas été évacuées. Une température plus élevée engendrant une énergie d'activation plus élevée peut détruire ces charges pour régénérer complètement le transistor. La pente sous-seuil a également été récupéré pour les deux transistors ainsi que les courants de fuite I_{off}.

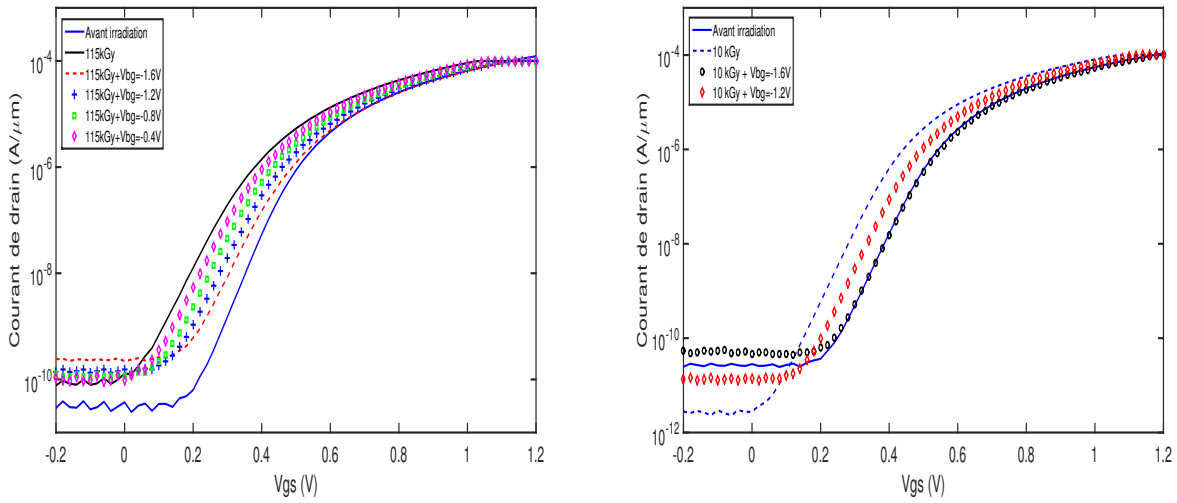


(a) NMOS W1. (b) NMOS W2.

Figure B.6: Régénération des caractéristiques électriques dégradées d'un transistor NMOS $W = L = 1\ \mu m$.

Test de la tension de grille arrière

La Figure B.7(a) et (b) montrent le résultat de l'application de plusieurs valeurs V_{bg} sur des transistors NMOS irradiés. On remarque que la modulation de V_{bg} permet la compensation de ΔV_{th} induite par le rayonnement, mais en raison des hauts niveaux de TID appliqués à W1, le V_{bg} appliqué n'est pas suffisant pour compenser entièrement la dégradation. Pour W2, nous avons pu annuler le ΔV_{th} en appliquant un V_{bg} de -1,6 V à la plupart des transistors. Cependant, et comme mentionné précédemment, V_{bg} ne compense niΔSS ni ΔI_{off}.



(a) NMOS W1.

(b) NMOS W2.

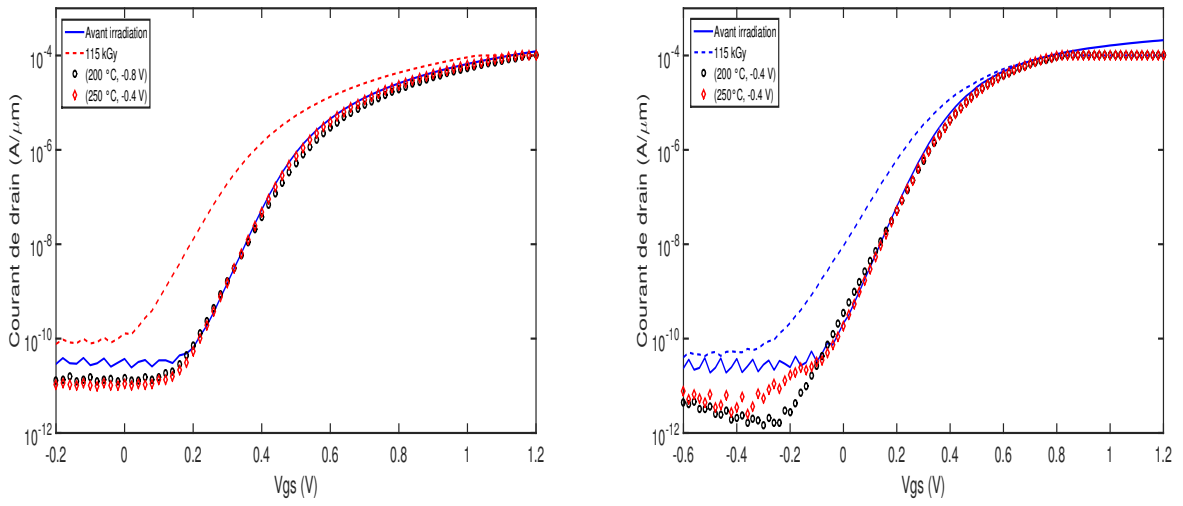
Figure B.7: Réponse de la polarisation de grille arrière des transistors NMOS $W = L = 1\ \mu m$ irradiés.

Pour résumer les avantages et les inconvénients, la régénération thermique est efficace lorsque l'on applique une haute température, mais les températures élevées peuvent affecter la fiabilité des circuits. La compensation électrique est limitée par la technologie et, en outre, elle ne corrige pas toute la dégradation induite par le rayonnement de transistors FDSOI. L'application d'une tension de polarisation arrière a montré des résultats efficaces pour compenser la dégradation de la tension de seuil dans les deux types de transistors NMOS et PMOS. Cependant, il existe une limite technologique pour la valeur V_{bg} qui a limité la compensation pour certains dispositifs irradiés à un niveau de dose élevé. De plus, cette technique ne compense pas la dégradation de la pente sous-seuil. Les deux méthodes présentent des avantages et des limites qui doivent être pris en compte lors de l'application à un circuit VLSI. Pour cette raison et afin de recouvrer les caractéristiques électriques initiales, nous proposons une méthode mixte qui utilise la régénération thermique et la compensation électrique.

Méthode mixte de régénération-compensation

L'objectif de la méthode consiste à déterminer le couple optimal (T, V_{bg}) qui atténue les effets du TID sur les transistors FDSOI avec la température la plus basse possible. Cette méthode mixte permet de réduire l'impact négatif sur la fiabilité du composant en raison d'une température élevée en utilisant prioritairement la méthode électrique. Pour cela, nous avons fixé des limites de dégradation tolérables pour les dispositifs testés: $\Delta V_{th} \leq 5\ mV$ et $\Delta SS \leq 10\ \%\ (6\ mV/dec)$.

La Figure B.8(a) montre les résultats de la stratégie mixte appliquée à un NMOS4 W1 ($W = L = 1\ \mu m$) irradié à 115 kGy. Après un cycle de recuit de 250 °C avec un V_{bg} de -0,4 V, nous observons une récupération totale de la dégradation de la tension de seuil avec un ΔSS restant de seulement 1,6 mV/dec. Lorsque la température de recuit est réduite (T $\leq$ 200 °C), la tension RBB doit être augmentée de -0,4 V à -0,8 V pour obtenir la régénération-compensation complète du décalage de tension de seuil. Avec cette température plus basse, le ΔSS restant est d'environ 5,8 mV/dec. Au vu de ces résultats, il est clair qu'un compromis entre la température de recuit et la récupération de la pente sous le seuil doit être envisagé. Le ΔSS peut avoir un impact sur la fréquence de fonctionnement et cela ne peut pas toujours être toléré par le système. Dans ce cas, la température/durée de recuit doit être augmentée.



(a) NMOS W1 $W = L = 1\ \mu m$.

(b) NMOS W1 $W = 0.21\ \mu m,\ L = 0.03\ \mu m$.

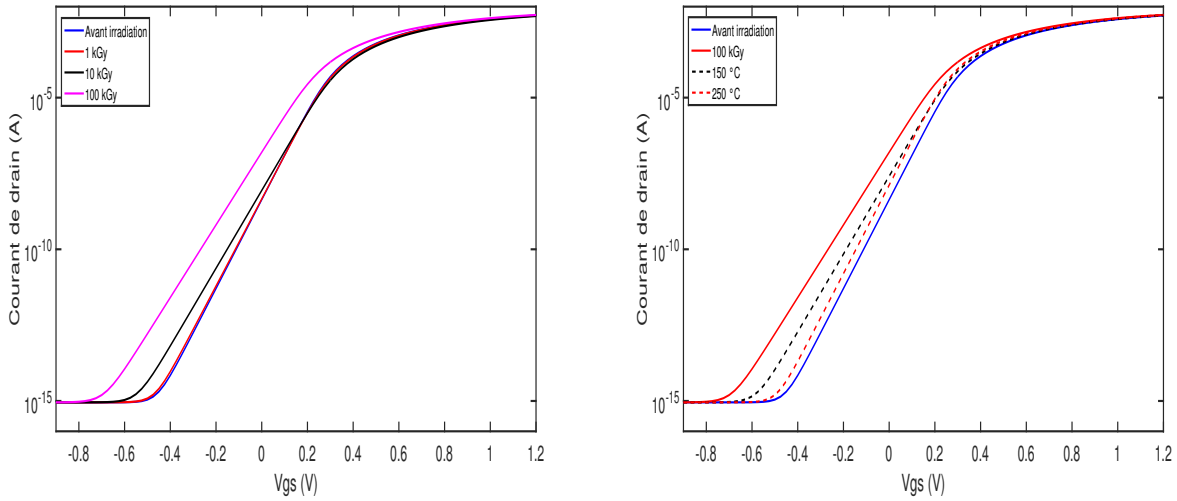
Figure B.8: Stratégie d'atténuation mixte des effets TID appliquée aux transistors NMOS.

On remarque que pour presque tous les transistors NMOS et PMOS testés, on peut atteindre le niveau d'atténuation requis en utilisant une température de recuit de 200 °C. Dans tous les dispositifs, les courants de fuite sont partiellement ou totalement récupérés, rétablissant leur consommation électrique nominale.

Modélisation des effets de dose sur les transistors FDSOI

Afin de modéliser les effets des rayonnements ionisants et les cycles de recuit thermique, une série de modèles physiques qui décrivent le comportement des charges piégées dans les oxydes, N_{ot}, dans les interfaces N_{it} et les cycles de recuit thermique qui permettent la régénération progressive des caractéristiques a été développée. Les modèles physiques proposés ont été implémentés à l'aide d'UTSOI2, une librairie SPICE développée par le CEA-LETI [194]. Ces modèles sont inspirés du modèle TID proposé dans [173] où les paramètres d'entrée sont N_{ot} et D_{it}.

Dans notre travail, le comportement de N_{ot} et D_{it} a été modélisé et implémenté afin de simuler les effets dégénératifs du rayonnement dans les transistors FDSOI. De même, nous avons inclus le modèle de régénération thermique qui décrit la récupération progressive des caractéristiques électriques dégradées (Figure B.9). Le modèle de compensation électrique étant intrinsèque à cette librairie, son efficacité a également été simulée.



(a) Dégradation induite par TID.

(b) Régénération par recuit thermique.

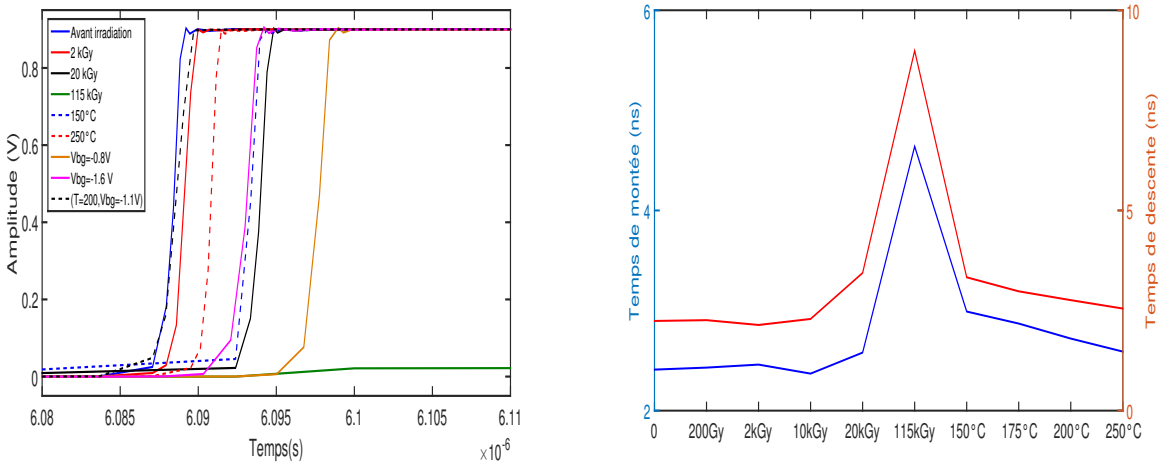
Figure B.9: Simulation de la dégradation induite par TID et des méthodes de récupération dans une librairie SPICE NMOS $W = L = 2\ \mu m$.

Étude des effets du TID et du recuit thermique sur les circuits élémentaires en SPICE

Afin d'analyser l'impact de la TID et de la régénération sur une porte logique, nous avons réalisé l'étude d'une porte inverseuse. Dans le cas idéal, l'application d'un signal logique carré en entrée de cette porte produit le même signal logique mais inversé, c'est-à-dire qu'un "1" logique en entrée produit un "0" logique en sortie et in-

versement. Les temps de réponse du passage d'un état à l'autre sont des paramètres clés dans la conception des circuits numériques et sont directement liés aux réponses des transistors. L'augmentation ou la diminution de ces temps peut produire une variation de la fréquence de fonctionnement s'ajoutant à celle de la consommation d'énergie dans un circuit intégré. Pour cette raison, les paramètres à surveiller sont les temps de montée et de descente après application de différents niveaux de TID, après application des cycles de recuit thermique et après application de différentes valeurs de V_{bg}.

La Figure B.10 montre le temps de montée de la porte. L'application de 2 kGy de TID génère un retard dans la réponse en plus d'une augmentation du temps de montée. A 20 kGy, l'augmentation du délai et du temps de montée est encore plus importante. Ces effets s'expliquent par la dégradation des paramètres électriques des transistors, qui présentent un ΔV_{th} et un ΔSS plus sévères avec des niveaux de TID croissants.



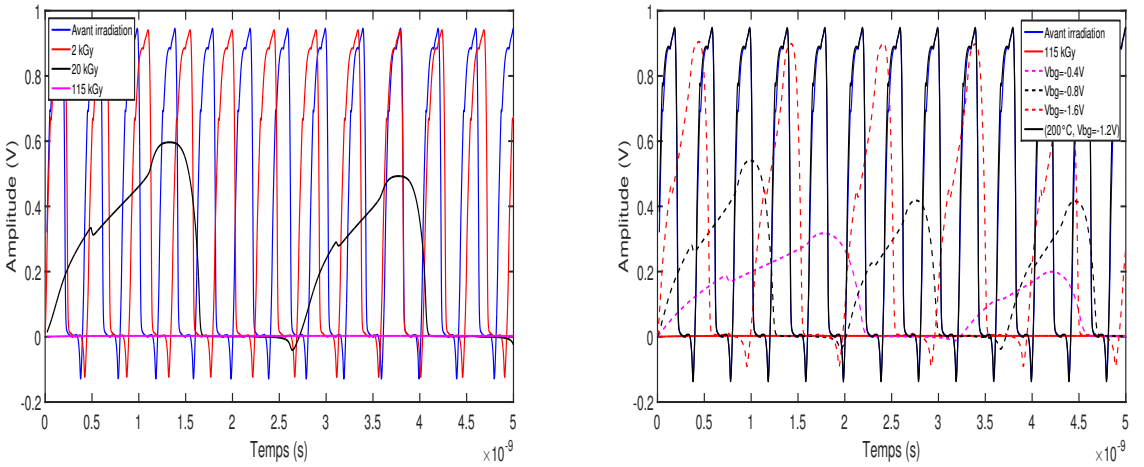
(a) Temps de montée.

(b) Temps de montée et descente après irradiation et recuit.

Figure B.10: Simulation de la dynamique des temps de montée et de descente après irradiation et recuit d'une porte inverseuse.

Pour analyser le comportement d'un circuit exposé au TID, nous allons simuler un oscillateur en anneau (RO) à cinq étages utilisant les transistors 28nm FDSOI. Ces dispositifs sont composés d'un nombre impair de portes logiques inverseuses connectées en série avec une rétroaction positive [201]. Ainsi, la fréquence souhaitée dépend directement du nombre d'étages inverseurs et du temps de retard de chaque étage inverseur de l'oscillateur. Dans ce cas, les paramètres à analyser seront la fréquence d'oscillation et la consommation électrique. Dans la Figure B.11(a) nous observons la fréquence d'oscillation du RO. A 2 kGy, une dégradation en fréquence, produit des contributions de D_{it} et N_{ot} en plus de la diminution de l'amplitude d'oscillation, produit une diminution de la consommation électrique. Une distorsion notable du signal, ainsi qu'une réduction drastique de la fréquence

et de l'amplitude de l'oscillation, sont observées pour un niveau de 20 kGy. La puissance consommée est considérablement augmentée en raison de l'augmentation des courants de fuite. Enfin, une défaillance totale est observée à un niveau de 115 kGy.



(a) Fréquence d'oscillation en fonction de la dose appliquée.

(b) Fréquence d'oscillation en fonction du recuit appliqué.

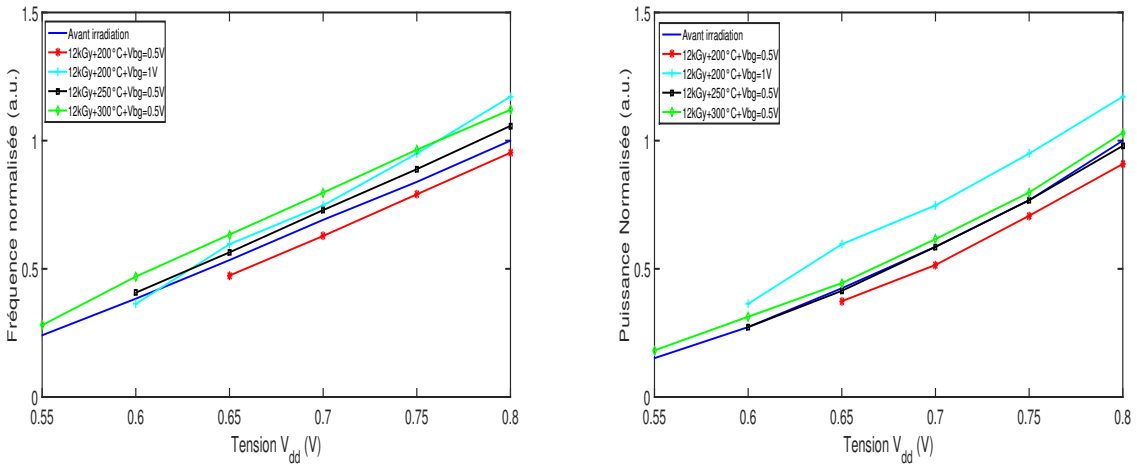
Figure B.11: Évolution d'un signal RO irradié lors de l'application des différentes tensions de grille arrière, et lors de l'application de la méthodologie mixte.

Exemple d'application sur un DSP 32-bit 28nm FDSOI

Comme la méthodologie de durcissement mixte a montré d'excellents résultats dans la récupération des caractéristiques électriques dégradées par le TID sur des transistors FDSOI élémentaires, nous prouvons l'efficacité de la stratégie d'atténuation lorsqu'elle est appliquée à une puce de processeur de signal numérique (DSP) 32 bits faite avec 28nm FDSOI dégradée par les rayonnements gamma. Pour cela, vingt-quatre DSP 32 bits fabriqués avec la technologie 28nm FDSOI de STMicroelectronics et du CEA-LETI ont été irradiés avec une source $^{60}Co\ \gamma - ray$. Les dispositifs ont été divisés en quatre groupes et placés à différents endroits dans la chambre d'irradiation pour observer la dégradation de leurs caractéristiques électriques à différents niveaux de TID. La dose a été déposée en plusieurs étapes pour atteindre 128 kGy, 19,8 kGy, 12,8 kGy et 3,5 kGy en groupes de 1 à 4, respectivement. Après la procédure d'irradiation, trois cycles de recuit thermique isochrone ont été appliqués à tous les dispositifs pour la régénération de leurs caractéristiques avec des températures de T_1 = 200 °C, T_2 = 250 °C et T_3= 300 °C et avec une durée Δt de 23 minutes chacun.

La Figure B.12(a) montre la récupération de la fréquence de fonctionnement lors de l'application de la stratégie de régénération-compensation proposée à la puce de test. Tout d'abord, une défaillance totale a été constatée après que les appareils aient reçu 12,8 kGy. L'application d'une température de 200 °C avec une polarisation arrière de

0,5 V peut partiellement guérir la dégradation de fréquence après la défaillance de la puce de test. L'application d'un V_{bg} de 1 V et d'une température de recuit de 200 °C assure le bon fonctionnement de la puce de test.



(a) Récupération de fréquence après application de la méthode T-V_{bg}.

(b) Récupération de la puissance de consommation électrique après application de la méthode T-V_{bg}.

Figure B.12: Récupération des performances du DSP FDSOI irradié

La Figure B.12(b) montre la puissance de consommation normalisée, mesurée après application de la stratégie de régénération-compensation. Comme prévu, la méthode atténue sensiblement l'effet des rayonnements ionisants sur la puissance de consommation. Ceci est dû principalement au recuit qui favorise l'évacuation des charges piégées dans les oxydes et diminue donc les courants de fuite induits par le rayonnement.

Conclusions

Grâce aux travaux menés au cours de cette thèse, nous avons pu proposer une nouvelle méthodologie mixte pour atténuer les effets du TID sur les transistors FDSOI. Cette méthode mixte a été testée expérimentalement et a montré une grande efficacité dans la récupération des paramètres électriques dégradés. La méthode nous a donné une série de couples (T, V_{bg}) satisfaisant aux deux paramètres de récupération, $V_{th} \leq 5\ mV$ et $\Delta SS \leq 10\%$, parmi lesquels nous choisissons celui où la température appliquée est la plus basse possible.

La méthode de régénération-compensation proposée dans cette thèse est prometteuse pour une application embarquée. Cela a été confirmé expérimentalement dans un DSP 32 bits réalisé avec la technologie 28nm FDSOI. L'avantage principal de cette méthode est qu'elle effectue une correction en temps réel, privilégiant la compensation électrique et utilisant la régénération que lorsque cela est nécessaire. De cette façon, la fiabilité du système est moins affectée, prolongeant sa durée de vie dans une mission dans des conditions de rayonnement élevé.

Les modèles physiques proposés, qui ont été implémentés dans une librairie FDSOI SPICE, ont montré une grande efficacité pour reproduire et prédire le comportement des principaux paramètres du transistor affectés par le TID, à savoir la tension de seuil et la pente sous-seuil, ainsi que la régénération fournie par les recuits et la compensation électrique. Ce modèle a été utilisé pour étudier le comportement de deux circuits électroniques élémentaires tels qu'une porte inverseuse et un oscillateur en anneau.

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