



Méthodologie d'évaluation d'effets des radiations dans les systèmes numériques : du niveau composant au niveau système

Israel da Costa Lopes

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IES – Institut d'Electronique et des Systèmes

Méthodologie d'évaluation d'effets des radiations dans les systèmes numériques : du niveau composant au niveau système

Présentée par Israel DA COSTA LOPES

Le 11 Décembre 2020

Sous la direction de Vincent POUGET

Devant le jury composé de

M. DUTERTRE Jean-Max	Maitre de Conférences, Ecole des Mines de Saint-Etienne	Rapporteur
M. ENTRENA Luis	Professeur, Université de Madrid	Examineur
M. LEVEUGLE Régis	Professeur, Grenoble INP, Université Grenoble Alpes	Rapporteur
M. MILLER Florent	Ingénieur, Nucléttudes	Examineur
M. POUGET Vincent	Chargé de Recherche, CNRS, IES	Directeur de thèse
M. SAIGNÉ Frédéric	Professeur, Université de Montpellier, IES	Examineur



UNIVERSITÉ
DE MONTPELLIER

To my family,

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LIST OF ACRONYMS

ACE - Architectural Correct Execution	DSP - Digital Processing Processor
ADC - Analog-to-Digital Converter	DUE - Detected Unrecoverable Errors
AEC - Automotive Electronics Council	ECC - Error Correction Code
AES - Advanced Encryption Standard	EEPROM - Electrical Erasable Programmable Read-Only Memory
AHB - Advanced High-performance Bus	EIA - Electronic Industries Alliance
AMP - Asymmetric Multiprocessing	ELF - Executable and Linkable Format
APB - Advanced Peripheral Bus	EM - Electromigration
APU - Application Processing Unit	eMMC - embedded Multimedia Card
AVF - Architecture Vulnerability Factor	EPROM - Erasable Programmable Read-Only Memory
AXI - Advanced eXtensible Interconnect	ESCC - European Space Components Coordination
AXIS - Advanced eXtensible Interface Stream	ESD - Electrostatic Discharge
BRAM - Block Random Access Memory	ESP - Emission of Solar Protons
BSP - Board Support Package	FBGA - Fine Pitch Ball Grid Array
BT - Bias Temperature instability	FF - Flip-Flop
CB - Carrier Board	FIFO - First-in-First-out
CCI - Cache-Coherent Interconnect	FIR - Finite-Impute-Response Filter
CERN - European Organization for Nuclear Research	FMECA - Failure Mode, Effects and Criticality Analysis
CLB - Configurable Logic Block	FPD - Full-Power Domain
CME - Coronal Mass Ejections	FPGA - Field Programmable Gate Array
CMOS – Complementary Metal-Oxide-Semiconductor	FSBL - First Stage Boot Loader
CoM - Computer-on-Module	FSM - Finite-State Machine
COOT - Constant On/Off Time	GCR - Galactic Cosmic Ray
COTS - Commercial-Off-The-Shelf	GEO - Geostationary orbit
CPU - Central Processing Unit	GLE - Ground Level Enhancement
CRAM - Configurable Rand Access Memory	GP - Geometry Processor
DCDC - Direct Current to Direct Current	GPIO - General Purpose Input-Output
DDR - Double Data Rate	GPU - Graphics Processing Unit
DFSR - Data Fault Status Register	HCI - Hot Carrier Injection
DMA - Direct Access Memory	HEH - High Energy Hadrons
DRAM - Dynamic Random Access Memory	

HKMG - High-k Metal Gate
HMI - Human Machine Interface
HPC - High Performance Computing
HPS - Hard Processing System
HTOL - High Temperature Operation Life
IO - Input/output
I2C - Inter-Integrated Circuit
IC - Integrated Circuit
IDDQ - Supply Voltage Quiescent Current
IDDT - Supply Voltage Transient Current
IEC - International Electrotechnical Commission
IES - Institute d'Électronique et des Systèmes
IL - Instrumentation Level
IP - Intellectual Property
IRPP - Integral Rectangular Parallel Piped
ISO - International Organization for Standardization
JEDEC - Joint Electron Device Engineering Council
JTAG - Joint Test Action Group
KVI-CART - KVI Center for Advanced Radiation Technology
LEO - Low Earth orbit
LET - Linear Energy Transfer
LHC - Large Hadron Collider
LPD - Low-power domain
LUT - Look-up Table
LUTRAM - Look-up Table Random Access Memory
MBU - Multi Bit Upset
MCU - Microcontroller Unit
MCU - Multiple Cell Upset
MDB - Mission Database
MEO - Medium Earth orbit
MIO - Multiplex Input Output

MLC - Multi Level Cell
MMCM - Mixed-Mode Clock management
MPSoC - Multi-Processor System-on-chip
NIST - National Institute of Standards and Technology
NoC - Network-on-Chip
NVM - Non-Volatile Memory
OCM - On-chip-Memory
OPAL - ONERA Proton Altitude Low
OS - Operating System
PCB - Printed Circuit Board
PCI - Peripheral Component Interconnect
PE - Processing Element
PFM - Pulse-Frequency Modulation
PID - Proportional-Integral-Derivative
PL - Programmable Logic
PLL - Phase-Locked Loop
PoP - Package-on-package
PP - Pixel Processors
PQFN - Power Quad Flat No-Lead
PS - Processing System
PSoC - Programmable System-on-chip
PSYCHIC - Prediction of Solar Particles Yields for Characterizing Integrated Circuits
PWM - Pulse-Width-Modulation
QSPI - Quad Serial Peripheral Interface
Rad-hard - Radiation-hardened
RAM - Random Access Memory
RDM - Radiation Design Margins
RHA - Radiation Hardness Assurance
RILC - Radiation Induced Leakage Current
RISC - Reduced Instruction Set Computer
RO - Ring Oscillator
ROI - Region of interest

ROM - Read-Only Memory	SO-DIMM - Small Outline Dual In-line Memory Module
RPU - Real-time Processing Unit	SOI - Silicon-on-Insulator
RTL - Register Transfer Level	SoM - System-on-Modules
SAA - South Atlantic Anomaly	SPA - Single Photon Absorption
SBC - Board Computer	SRAM - Static Random Access Memory
SBU - Single Bit-Upset	STI - Shallow Trench Insolation
SDC - Silent Data Corruption	SUT - System Under Test
SDK - Software Development Kit	TCM - Tightly Coupled Memory
SDR - Single Data Rate	TDDDB - Time Dependent Dielectric Breakdown
SDRAM - Synchronous Dynamic Random Access Memory	TEM - Transmission Electron Microscopy
SEAM - Systems Engineering and Assurance Modeling	TID - Total Ionizing Dose
SEB - Single Event Burn-Out	TTL - Transistor–Transistor Logic
SEE - Single Event Effects	UART - Universal Asynchronous Receiver Transmitter
SEFI - Single Event Functional Interrupt	UART - Universal Asynchronous Receiver-Transmitter
SEL - Single Event Latch-up	USB - Universal Serial Bus
SEP - Solar Energetic Particle	VCU - Video Control Unit
SET - Single Event Transient	VHDL - Very High Speed Integrated Circuit Hardware Description
SEU - Single Event Upset	WCA - Worst Case Analysis
SILC - Stress Induced Leakage Current	WFE - Work Function Engineering
SiP - System-in-Package	XSDB - Xilinx Software Debugger
SLC - Single Level Cell	Z7 - Zynq7000
SMU - Source and Measurement Unit	ZU+ - ZynqUltrascale+
SoC - System-on-Chip	

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RÉSUMÉ EN FRANÇAIS

Les investissements d'initiative privée dans les applications aérospatiales augmentent chaque année dans ce qu'on appelle le New Space [SVWD18]. Récemment, SpaceX est devenue la première entreprise privée à lancer des humains sur l'orbite terrestre. Dans le même temps, sur le terrain, l'intelligence artificielle nécessaire au fonctionnement des voitures autonomes [SAMS18] pousse les exigences de performance et les contraintes de puissance sur les dispositifs informatiques, conduisant la mise à l'échelle des technologies nanoélectroniques au plus près de la limite d'échelle atomique [TSMC20].

Afin de rester compétitifs et de satisfaire les exigences de leurs clients, les fabricants de systèmes doivent intégrer les dernières générations de *Commercial-Off-The-Shelf* (COTS) [BKAQ15]. Compte tenu de la complexité et du coût de la conception et de la qualification des cartes de circuits imprimés (ou PCB de l'anglais *Printed Circuit Board*) pour des composants complexes, il existe également un intérêt croissant pour l'utilisation de cartes ou de modules commerciaux à faible coût qui incluent déjà tous les circuits périphériques requis par ces composants.

Dans les domaines qui nécessitent des niveaux de fiabilité très élevés, comme les industries spatiales ou automobiles, la contrainte spécifique des environnements radiatifs doit être prise en compte. En effet, les circuits intégrés exposés aux radiations peuvent faire face à différents types de perturbations ou de pannes induites par l'interaction des particules avec leurs matériaux. Par conséquent, la fiabilité des circuits intégrés doit être caractérisée en utilisant des méthodologies d'assurance de la résistance aux radiations (RHA de l'anglais *Radiation Hardness Assurance*).

Depuis de nombreuses années, les méthodologies standard des RHA ont consisté à tester les différents composants d'un système en présence de sources de radiation ou de faisceaux de particules et d'analyser leur réponse afin de quantifier la fiabilité de chaque composant individuellement [ESA14][DOD95]. La fiabilité sous radiations au niveau système est ensuite estimée dans une approche ascendante [SCSD13]. Du point de vue des tests, cette approche classique est appelée approche au niveau composant. Elle permet de mieux comprendre le comportement des différents composants du système lorsqu'ils sont exposés à des radiations. Les résultats au niveau composant peuvent également être réutilisés pour différents systèmes et applications ou extraits de la littérature, ce qui réduit le coût de l'expérience.

Néanmoins, l'approche au niveau des composants présente plusieurs inconvénients. Le temps de faisceau de particules nécessaire pour tester chaque composant est coûteux, tout comme le développement de bancs de test spécifiques pour chaque génération de composant. L'ensemble du processus prend du temps, augmente le temps d'accès au marché (*time-to-market*) des applications industrielles et est devenu incompatible avec le rythme de renouvellement des technologies. Combinés à l'impossibilité de tester des composants complexes de manière exhaustive [JEDE06] et à la tendance à utiliser les *Systems-Off-The-Shelf* (systèmes sur étagère) comme briques élémentaires de systèmes plus grands, ces inconvénients rendent l'approche au niveau des composants de moins en moins attractive de nos jours. Idéalement, les fabricants de systèmes souhaiteraient être en mesure de qualifier un système pour un environnement radiatif en effectuant un seul test de l'ensemble du système sous radiations. Cela donne lieu à une méthodologie RHA émergente :

l'approche au niveau système [GUGU17] [SGPB18][RASB17]. Dans cette approche, comme son nom l'indique, l'ensemble du système matériel intégrant son application logicielle finale doit être caractérisé simultanément. Ainsi, le temps de faisceau et les coûts de développement du banc de test associés à de nombreuses campagnes de radiation pour différents composants seraient réduits et la réponse aux radiations au niveau système pourrait être directement obtenue. De toute évidence, les tests sous radiations et la prévision de la fiabilité ne sont pas si simples, et il existe actuellement de nombreuses limitations ou questions techniques qui nécessitent des réponses pour qu'une telle approche au niveau système soit utilisable et adoptée par l'industrie. C'est l'un des objectifs du projet européen RADSAGA, piloté par le CERN, de contribuer à la normalisation de l'approche au niveau système pour les tests sous radiations.

L'objectif de ce travail, dans le contexte du projet RADSAGA, est d'étudier la possibilité de définir une approche intermédiaire qui combinerait le concept de test au niveau système avec les connaissances et pratiques existantes des méthodologies RHA au niveau composant. Cette approche constituerait au moins une première étape, et éventuellement une passerelle vers une future méthodologie de test au niveau système. Ainsi, dans ce travail, nous étudions la définition d'une méthodologie de transition du niveau composant au niveau système pour l'évaluation des effets des radiations dans le cas particulier des systèmes numériques, et plus particulièrement dans le cas des systèmes-sur-module commerciaux (SoM de l'anglais *System-on-Module*).

Nous présentons dans un premier temps l'état de l'art des effets des radiations et d'autres problèmes de fiabilité des composants numériques, ainsi que les méthodologies actuelles de test sous radiations au niveau composant. Dans la première section, une approche ascendante est utilisée pour présenter les systèmes numériques à partir du processus de fabrication jusqu'aux solutions de systèmes numériques. Dans la deuxième section, une approche ascendante est également utilisée pour expliquer les effets des radiations sur les systèmes numériques en décrivant les différents environnements, l'interaction particule-composant et les effets des radiations au niveau transistor, composant et système. Les méthodologies classiques et émergentes pour caractériser ces effets et garantir la résistance aux radiations des systèmes numériques sont décrites. Les limites de la méthodologie de test classique au niveau composant sont signalées, telles que les exigences de préparation des échantillons. En ce qui concerne la nouvelle méthodologie de test au niveau système, les exigences sur les moyens d'irradiation pour tester différentes classes de systèmes numériques sont énumérées, telles que l'homogénéité du faisceau, la pénétration élevée et la grande taille du faisceau. Enfin, les principaux éléments constitutifs des méthodologies RHA prenant en compte les effets d'événement unique (SEE de l'anglais *Single-Event-Effects*) et la dose ionisante totale (TID de l'anglais *Total-Ionizing-Dose*) sont expliqués.

La troisième et dernière section décrit brièvement le principal mécanisme de vieillissement qui peut affecter la fiabilité des systèmes numériques et leur sensibilité aux radiations, dont l'instabilité thermique (BTI de l'anglais *Bias-Temperature-Instability*), la rupture diélectrique en fonction du temps (TDDB de l'anglais *Time-Dependent-Dielectric-Breakdown*), l'injection de porteurs chauds (HCI de l'anglais *Hot-Carrier-Injection*) et l'électromigration (EM). Ensuite, les effets possibles du vieillissement sur la sensibilité à radiation (et réciproquement), les effets dits couplés, sont brièvement présentés. Enfin, nous expliquons comment ce contexte motive le développement de nouvelles méthodologies RHA orientées vers les tests au niveau système, en particulier pour les applications à faible coût ou haut risque acceptable.

Le chapitre suivant présente le système numérique et une application spécifique que nous avons conçue comme une étude de cas pour ce travail. Une application finale destinée à être représentative de systèmes numériques aérospatiaux simples a été développée et mise en œuvre sur des SoM industriels commerciaux basés sur des SoC récents en 28nm Planar et 16 FinFET CMOS. L'ancienne technologie SoM comprend les SoC Zynq7000 (Z7) et DDR3 et les SoM les plus récents incluent les mémoires DDR4 et SoC ZynqUltrascale+ (ZU+).

Le concept d'instrumentation, dans le cadre de ce travail, est introduit, consistant à insérer des blocs de code, des blocs IP (de l'anglais *Intellectual-Property*) ou des modifications matérielles mineures pour augmenter l'observabilité du système lors des tests au niveau système. Ainsi, le code et les blocs IP d'instrumentation qui ont été ajoutés à l'application finale afin d'améliorer l'observabilité des expériences SEE et TID, sont détaillés et discutés. Des détails de mise en œuvre du banc expérimental sont également fournis, tels que les scripts Python pour le contrôle du faisceau, du banc expérimental et du système sous test (SUT de l'anglais *System-Under-Test*), ainsi que la carte mère dédiée qui a été conçue et la carte mère commerciale utilisée pour opérer les SoMs.

Le troisième chapitre présente les différentes campagnes de tests sous radiations qui ont été réalisées, au sein du consortium RADSAGA, afin d'accumuler des données pour évaluer la fiabilité de nos systèmes. Dans la première expérience, des neutrons atmosphériques ont été utilisés dans lequel un prototype de l'application finale et le logiciel de test de mémoire développé par le fabricant ont été utilisés pour effectuer une analyse de premier ordre des événements observables au niveau système et de sa corrélation avec les événements au niveau des composants. Ensuite, des expériences sous protons de 184MeV ont été menées sur des versions améliorées de l'application finale et de l'instrumentation, permettant d'observer davantage d'événements.. Afin d'obtenir des données TID sur le composant le plus complexe du système (SoC), une irradiation localisée sous rayons X a été réalisée pour comparer la dégradation des performances de la logique programmable (PL de l'anglais *Programmable-Logic*) des deux technologies étudiées. Enfin, les résultats des protons ont été mieux analysés en irradiant les ressources processeurs (PS de l'anglais *Processing-System*) et configurables (PL, programmable logic) des SoC à l'aide d'un laser impulsif à 1064 nm. Les résultats sont présentés et discutés. Ils confirment que les tests avec des protons de haute énergie devraient être la méthode à privilégier pour le test SEE des systèmes à faible coût.

Le dernier chapitre résume les leçons tirées de nos campagnes de tests au niveau système. La préparation de l'expérience comprend une bonne élaboration du plan de test, un banc expérimental fiable et une instrumentation validée. Ensuite, de bonnes pratiques lors des tests au niveau système sont proposées, telles que l'augmentation des niveaux d'irradiation, de l'exposition du système et de l'observabilité.

Par la suite, une méthodologie passerelle qui pourrait être appliquée pour l'évaluation de la sensibilité aux radiations de systèmes similaires est proposée. La méthodologie de transition commence par l'analyse du système qui consiste à identifier les composants critiques et l'utilisation des composants. Ensuite, le système est instrumenté et le plan de test est élaboré en fonction de l'utilisation des composants, des composants critiques et des exigences de la mission telles que le budget et le profil de la mission. Ensuite, des

caractérisations sous radiations sont effectuées en suivant les recommandations décrites précédemment. Une étape importante est la corrélation composant-système qui vise à obtenir des données au niveau composant à partir de données au niveau système. Enfin, les données au niveau composant et système sont utilisées pour calculer et prédire la fiabilité au niveau système. Une étude de cas d'estimation de la fiabilité a été présentée, considérant l'utilisation de nos systèmes dans une mission LEO-ISS.

En ce qui concerne l'analyse de la cause originelle des pannes au niveau système, il existe actuellement une bonne quantité de données expérimentales sous radiations disponibles dans la littérature qui peuvent aider concernant les mémoires externes telles que les composants DDR et Flash. Cela peut s'expliquer par le fait que ces composants sont relativement simples à tester de manière exhaustive sous radiations, ce qui n'est pas le cas des processeurs, FPGA, microcontrôleurs... Ainsi, l'enjeu sur les systèmes numériques est de comprendre comment et où les défauts sont générés sur ces composants complexes. Dans cette mesure, le laser impulsif et les irradiations locales sous rayons X permettent une meilleure compréhension des mécanismes de défaillance et de dégradation de ces composants. Ces techniques contribuent à valider et à améliorer les modèles de génération et de propagation des événements et, par conséquent, la qualité des prévisions de fiabilité du système.

La méthodologie de transition proposée tente de faire une utilisation optimale des données, des outils et des méthodes existants issus de l'approche classique au niveau composant. Une contribution importante de ce travail est liée à la conception et à l'insertion d'instrumentation à l'application embarquée finale afin d'améliorer considérablement l'observabilité des différents types d'événements lors des tests au niveau système. L'instrumentation doit être considérée comme un moyen d'avoir un aperçu à l'intérieur de la «boîte noire» du système. La version finale du code d'instrumentation permet cela tout en ajoutant une faible taille de code et sans impact notable sur les performances de l'application. L'exploration des capacités de contrôle et de correction intégrées aux composants a montré qu'elles représentaient également un moyen efficace d'instrumentation à faible coût. De plus, la mise en œuvre d'un logiciel flexible de test TID et vieillissement ont permis d'observer et de comparer la dégradation paramétrique des deux technologies testées sous la dose totale. De telles informations sont rares dans la littérature et revêtent une grande importance pour les concepteurs de FPGA travaillant sur des conceptions avec des critères de performance élevés pour des applications spatiales.

Plusieurs pistes ont été identifiées pour améliorer la méthodologie proposée. Développer la portabilité de l'instrumentation sur différentes architectures FPGA et processeurs permettrait de généraliser l'approche. Des outils pourraient être développés afin d'automatiser l'insertion de l'instrumentation logicielle et matérielle. Nous avons également observé la nécessité d'une norme spécifique aux radiations pour la classification et la notification des événements au niveau système observés au cours d'un test au niveau système afin de faciliter la réutilisation partielle de ces données.

La prédiction des taux de SEE au niveau système à partir des tests au niveau système est une tâche complexe et la méthodologie de transition proposée utilisant à la fois les tests au niveau système et l'analyse au niveau composant est un premier pas vers cet objectif. Afin d'étendre la méthodologie à une gamme plus

large de systèmes et d'applications, davantage d'études de cas et d'options d'instrumentation devraient être étudiées. En outre, une extension possible de la méthodologie proposée pourrait inclure la surveillance des effets couplés des radiations et du vieillissement. En effet, à ce jour, ces effets couplés sont généralement pris en compte en augmentant les marges de conception des systèmes, ce qui a des implications importantes tant au niveau économique que sur celui des performances.

1. INTRODUCTION

The private initiative investments in aerospace applications are increasing every year in what is called New Space [SVWD18]. Recently, SpaceX became the first private company to launch humans into the Earth orbit. At the same time, on the ground, the artificial intelligence required for operating autonomous cars [SAMS18] is pushing the performance requirements and the power constraints on computing devices, driving the scaling of nanoelectronics technologies close to the atomic scale limit [TSMC20].

In order to stay competitive and satisfy their customer requirements, systems manufacturers need to integrate recent generations of Commercial-Off-The-Shelf (COTS) [BKAQ15]. Considering the complexity and cost of designing and qualifying printed circuit boards (PCBs) for complex components, there is also a growing interest in using low-cost commercial boards or modules that already include all the peripheral circuitry required by those components.

In domains that require very high levels of reliability, like the space or automobile industries, the specific constraint of radiation environments has to be considered. Indeed, integrated circuits exposed to radiation can face different kinds of perturbations or failures induced by the interaction of particles with their materials. Therefore, the reliability of integrated circuits should be characterized by using Radiation Hardness Assurance (RHA) methodologies.

For many years, standard RHA methodologies have consisted in testing the different components of a system in the presence of radiation sources or particle beams and analyzing their response in order to quantify the reliability of each component individually [ESA14][DOD95]. The system-level reliability under radiation is then estimated in a bottom-up approach [SCSD13]. From a testing point of view, this classical approach is called the component-level approach. It allows a better understanding of how the different components of the system behave when exposed to radiation. The component-level results can also be reused for different systems and applications or extracted from the literature reducing the experiment cost.

Nonetheless, the component-level approach has several disadvantages. The particle beam time required for testing each component is expensive, as is the development of specific testbenches for each generation of component. The whole process is time-consuming, increasing the time-to-market for industrial applications, and has become incompatible with the pace of renewal of the technologies. Combined with the impossibility to test exhaustively complex components [JEDE06] and with the trend to use Systems-Off-The-Shelf as the elementary bricks of larger systems, those disadvantages make the component-level approach less and less attractive nowadays. Ideally, systems manufacturers would like to be able to qualify a system for a radiation environment by performing a single radiation test on the whole system. This gives rise to an emerging RHA methodology: the system-level approach [GUGU17][SGPB18][RASB17]. In this approach, as the name implies, the whole hardware system embedding its final software application should be characterized simultaneously. Thus, the beam time and testbench development costs associated to many radiation campaigns for different components would be reduced and the system-level response to radiation could be directly obtained. Obviously, radiation testing and reliability prediction are not so simple, and there are currently many technical limitations or questions that require answers for such system-level approach to be usable and adopted

by the industry. It is one of the objectives of the European RADSAGA project, driven by the CERN, to contribute to the standardization of the system-level approach for radiation testing.

The objective of this work, in the context of the RADSAGA project, is to investigate the possibility to define an intermediate approach that would combine the concept of system-level testing with the existing knowledge and practices of component-level RHA methodologies. This approach would constitute at least a first step, and possibly a gateway towards a future system-level testing methodology. Thus, in this work, we investigate the definition of a bridging methodology from component to system-level for the assessment of radiation effects in the particular case of digital systems, and more specifically in the case of commercial System-on-Modules.

In the first chapter, the state-of-the-art of the radiation effects and aging mechanisms on digital systems will be introduced. We will present the technologies and components used in digital systems as well as the radiation environments and their effects on integrated circuits. The current test and RHA methodologies will be discussed.

The second chapter will present the technical details of the system that we designed using recent technologies as a case study for this work. The hardware targets, i.e. the System-on-Modules (SoM) under test, as well as the embedded software application will be described. The instrumentation that was added to the system and that constitutes an essential element of our bridging methodology will be detailed, and its benefits and impacts discussed.

The next chapter will present the different radiation testing campaigns that were performed on our system using neutrons, protons, X-ray and laser beams. The experimental results will be synthesized and discussed.

Based on the lessons learned during those campaigns, the last chapter will summarize our guidelines and recommendations for performing system-level experiments. Then, the elements of a bridging methodology will be presented for evaluating the reliability of a system under radiation from system-level testing. The methodology will be applied to our case-study before discussing its limitations and the possible paths for improvement.

2. RADIATION AND AGING EFFECTS ON DIGITAL SYSTEMS

In this chapter, reliability mechanisms such as radiation and aging effects on digital systems will be discussed. First, technical information about components of a digital embedded system will be presented. Second, radiation levels of different environments, its interaction with system's components and effects will be described. Finally aging mechanisms that influence radiation effect sensitivity and vice versa will be presented.

2.1. DIGITAL SYSTEMS

In this section, a bottom-up approach will be used to explain the technologies of embedded digital systems starting from manufacturing process to a complete digital system platform. After describing modern CMOS technology processes, technical information of essential components for the operation of a digital system will be described. Finally, different ways of integrating those components within systems or sub-systems for aerospace and high reliability ground applications will be discussed.

2.1.1. Modern CMOS technology process

Complementary Metal-Oxide-Semiconductors (CMOS) logic provides higher performance than PMOS-only and NMOS-only logics and has been used in most of the digital Integrated Circuits (ICs) nowadays [WEHA13]. An illustration of a modern bulk planar cross-section is presented in Figure 2-1.

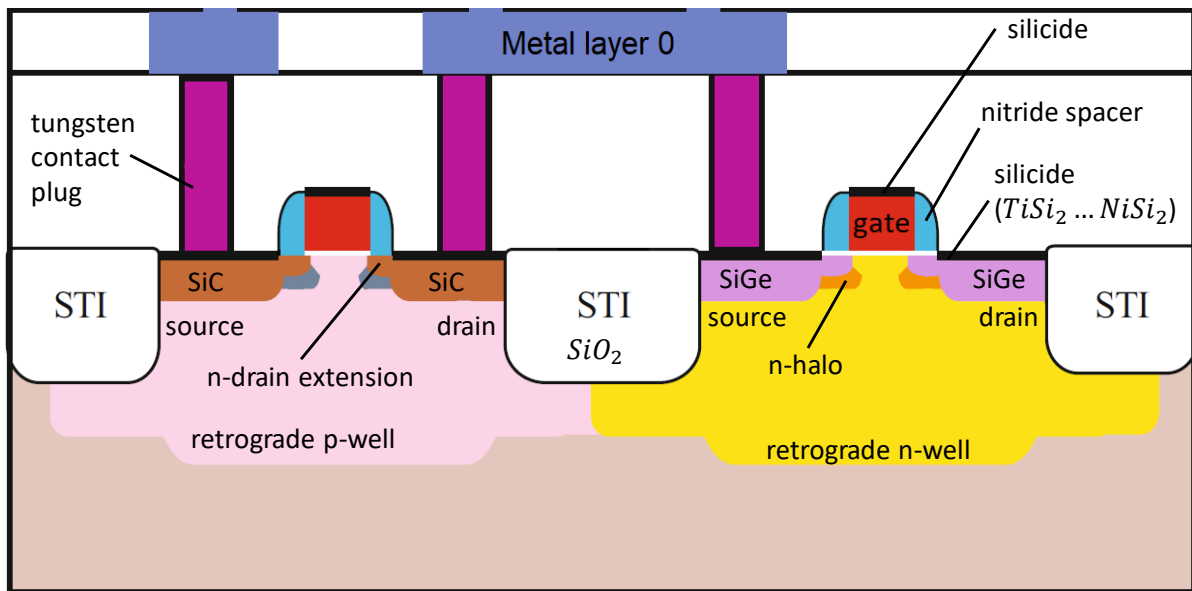


Figure 2-1. Illustration of a CMOS inverter cross-section [WEHA13].

Technology size is defined by the distance between the source and drain presented in the picture. As it can be seen, different material enhancements have been employed to improve the performance and allow further geometry scaling. As substrate, monocrystalline lightly doped silicon has been used for most digital applications. In order to isolate transistors, Shallow Trench Isolation (STI) [MAMA12] has been used having lower leakage than the previous isolation approach. For improving the performance, different materials have also been introduced such as SiC and SiGe in source and drain regions, SiGe on channels, nitride spacers [WEHA13] and silicide for the contacts [JMVE17].

For reducing gate leakage, High-k Metal Gates (HKMG) dielectric stacks has been used [MAAB07]. A Transmission Electron Microscopy (TEM) picture of a 28nm TSMC gate last technology is presented in Figure 2-2 [DIGE11].

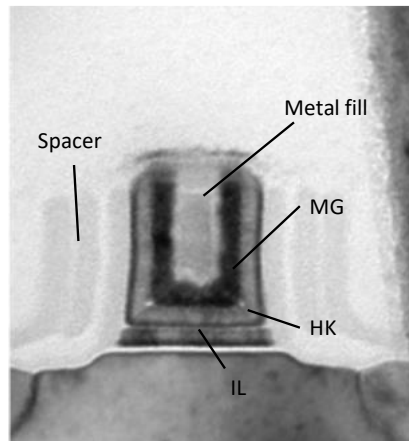


Figure 2-2. TEM picture of TSMC 28nm HKMG gate last technology [DIGE11]

Common materials used for HKMG stack are a Titanium-Nitride (TiN) as metal gate, Hafnium-Silicon-Oxygen-Nitride (HfSiON) as h-k dielectric, and Silicon-dioxide (SiO₂) as interface layer [RHRP17].

Technology nodes below 28nm also include different structures such as multi gates. It increases the drain potential screening leading to better short channel performance, lower threshold and supply voltages [BHJH15]. A 3D illustration comparing the conventional planar CMOS technology and the FinFET technology is presented in Figure 2-3 and a TEM picture of a TSMC 16nm FinFET transistor is presented in Figure 2-4 [JAME16].

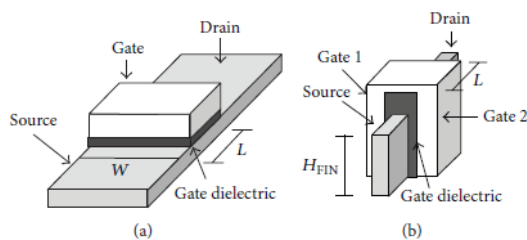


Figure 2-3. Structural comparison between (a) planar MOSFET and (b) FinFET [BHJH15].

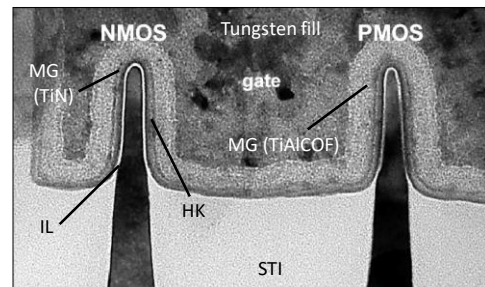


Figure 2-4. TEM images of fins and gates in TSMC 16-nm FinFET transistors [JAME16].

Comparing Figure 2-2 and Figure 2-4, it is possible to see that in the FinFET technology the HKMG stack contours the source and drain regions (not visible in two dimensions). In addition, different MG materials are used in the PMOS and NMOS transistors. Those materials compose the work function layer since Work Function Engineering (WFE) is used to control the threshold voltage and reduce short channel effects [HUHH19].

In addition to the 28nm and 16nm innovations discussed, foundries have performed further geometric scaling down to 5nm intended for high-end commercial applications such as smart phones, High Performance Computing (HPC) [TSMC20]. However, those technologies are still not mature to be applied to aerospace and high reliability ground applications as their reliability response is not as well-known as in older technologies

such as 130nm. Material and structure innovation of two modern technologies were presented. That information will be required to understand the aging and radiation reliability mechanisms that will be presented in the next sections.

2.1.2. Components of typical digital embedded systems

Currently, there is no widely accepted standard definitions of a system or a component as these concepts depend both on the considered scale and the field of application. In the context of this work, a system can be defined as an assembly or integration of sub-systems or components to deliver a functionality. Integrated Circuits (ICs) such as DCDC converters or System-on-Chips (SoCs) can be defined as systems since they integrate many elementary devices and functional blocks. In order to avoid confusion, in the following, a component will be defined as an IC and a system will be defined as an assembly of components to perform a specific functionality.

We consider a typical digital embedded system as composed of a processing core that uses memories for storing code and data, has I/O functionally and communicate with peripherals by using interconnections [NURM07]. Thus, components necessary for the operation of such embedded digital system will be discussed in this section. First, memory cell implementation details, and component integration of non-volatile and volatile memories will be described. Second, the digital SoCs, as processing cores, will be presented. Finally, DCDC converter fundamentals will be briefly synthesized.

2.1.2.1. Volatile Memory technologies

Embedded digital systems require memory ICs for storing temporary or long-term data. Memories that lose their content after a power cycle are classified as volatile memories, while memories that can keep stored data for years even after a power cycle are defined as Non-Volatile Memories (NVM). Volatile memories are usually referred as Random Access Memory (RAM) due to the possibility of accessing any address without the necessity of following a sequence. Two main RAM families are Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) [CYPR20]. SRAM can be implemented by using different circuit approaches such as Full-CMOS 6 Transistor – Memory Cell (6T-MC), poly-load Memory Cell, Thin-film Transistor PMOS Memory Cell (TFT PMOS-MC) and Loadless 4 Transistor – Memory Cell (LL4T-MC). Whereas, DRAM memories can be implemented by simply using a capacitor and one transistor as a wordline gate. Conventional 6-transistor CMOS SRAM and DRAM cell implementations are presented in Figure 2-5.

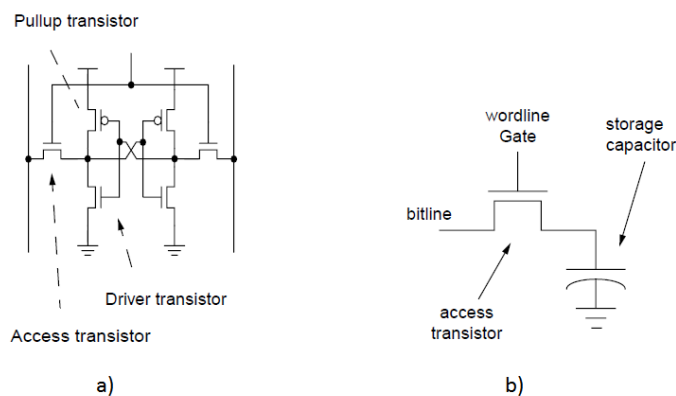


Figure 2-5. SRAM and DRAM cell implementations a) typical 6-Transistor SRAM cell implementation b) DRAM cell implementation

As it can be noted, the SRAM cell implementation requires much more transistors than the DRAM implementation, thus those memories are more expensive (about \$1-100 per megabyte) than DRAMS (about \$0.1 per megabyte) and usually have lower capacity (few megabytes) than DRAMs (few gigabytes). Those memories are commonly used as cache memories for processors as they can operate at a high speed (100 picoseconds per access) than DRAMs (10-100 nanoseconds per access). They can also be used as Configurable Random Access Memory (CRAM) for Field Programmable Gate Arrays (FPGAs) that will be described in the next section. SRAMs can keep the stored data while the power is on, while DRAM memories, which are implemented using capacitors, have to be refreshed periodically to keep the stored data. As its cell implementation is small and cheaper, DRAM memories are usually used as mass storage.

SRAM and DRAM memories can also be implemented in asynchronous or synchronous modes [JWNR08]. It means that those memories can operate following the clock cycles or the activity of their ports. When DRAM families are implemented in a synchronous way, they are called Synchronous Dynamic Random Access Memory (SDRAM). SDRAM memories can be further classified into Single Data Rate (SDR) and Double Data Rate (DDR). DDR SDRAM memories have the advantage of being able to capture the data on both rising and falling edges of the clock doubling the frequency of the DRAM [MICR01]. An illustration of a generic memory array block connected to SDR and DDR I/O Interfaces is presented in Figure 2-6.

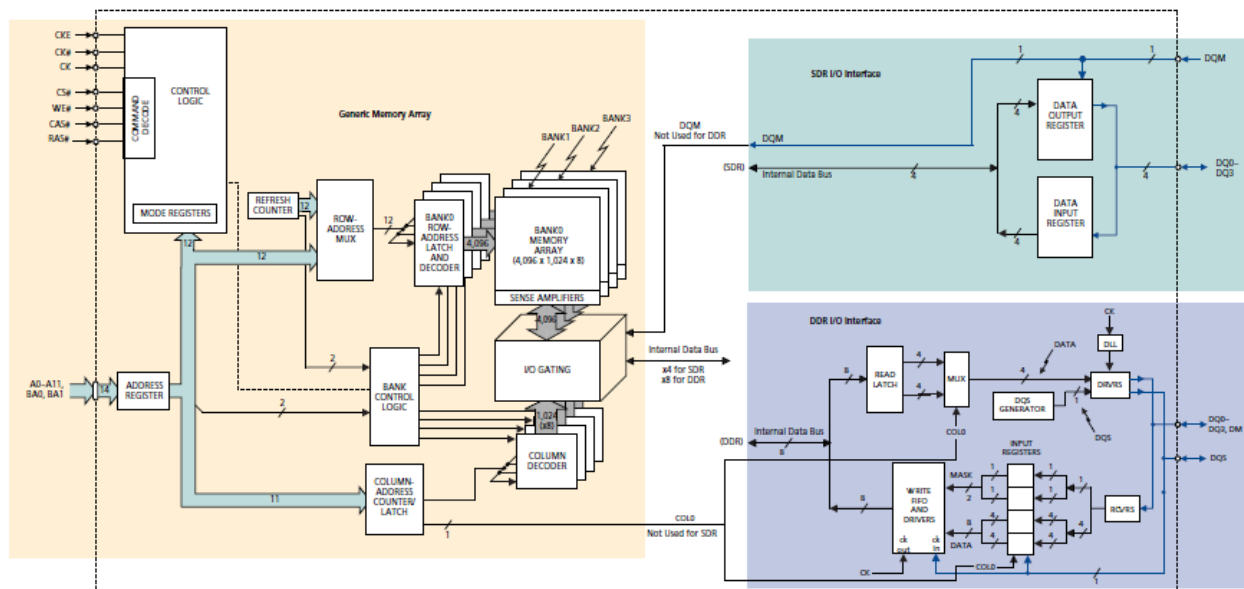


Figure 2-6. Functional block diagram of SDRAM with SDR and DDR I/O interfaces [MICR01].

As it can be seen, in SDR I/O interfaces, only registers are enough for transferring data as the information is updated in one cycle. However, in a DDR I/O memory, read latches are required to update data at different logic levels including write First-in-First-out (FIFOs), drivers etc. It is also possible to see in the figure that memory addresses are decoded to bank, row and columns addresses. Since then, different DDR SDRAM memory technologies have been produced (DDR1, DDR2, DDR3...) increasing the data rates and power efficiency [ROMO20]. The DDR technology version specification are defined by the Joint Electron Device Engineering Council (JEDEC) standards [JEDE09].

2.1.2.2. Non-Volatile Memory technologies

NVM was initially called Read-only Memory (ROM) since after storing data it was not possible to program it again. With the evolution of ROM memories, it was possible to program and erase it by different ways. When a ROM can be reprogrammed by using Ultraviolet (UV) light, it is called Erasable Programmable Read-only memory (EPROM) and when a ROM can be reprogrammed electrically in-system, it is called Electrical Erasable Programmable Read-only Memory (EEPROM). Another class of EEPROM is the Flash EEPROM, or simply Flash. EEPROMs can be reprogrammed byte-a-byte, while in Flashes the whole sector, block or page has to be reprogrammed. Flash memories have a higher capacity (dozens of gigabits) than EEPROMs that storage usually less than 1MB. Flash memories can be implemented by NOR or NAND logic gates. NAND memories have a higher capacity (64 megabits to 16 megabits) than NOR memories (1 megabit to 16 gigabits), however have a lower performance (read sequential access of 50ns) than NOR memories (read sequential access of 9ns). Thus, those kinds of memories are usually used for data storage [CYPR19]. As NOR memories operate in a high-speed they are usually used for program code storage. Flash memories can also be sub-classified into Single Level Cell (SLC) and Multi Level Cell (MLC) depending on its implementation.

A simplified block diagram of a NOR Flash memory is presented in Figure 2-7.

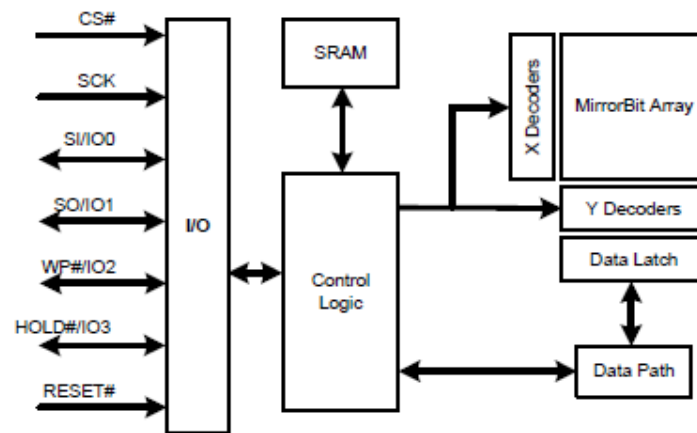


Figure 2-7. A simplified parallel NOR MirrorBit Flash block diagram [CYPR19].

The Input/output (IO) block implements a communication protocol between the memory and the host controller. It receives commands and data that is sent to the control logic whose functionality is to execute those commands and transfer data. It uses a SRAM volatile memory to store the instructions. X and Y Decoders are used for selecting a bit in the memory array that is mapped by columns and rows. Finally, data words are stored in the Data Latch that is transferred to the output by a using the Data Path block.

A Flash memory cell is stored by using a potential well to store charge data that is usually divided in bytes, pages and sectors. Pages are set of bytes and sectors and set of pages. Before writing a data, an entire Flash memory sector has to be erased and then the data can be stored page-by-page while reading operations can be done byte-by-byte.

2.1.2.3. Programmable System-on-chip technologies

The CMOS technology evolution allowed the development of highly integrated and high complexity systems. This evolution also required the development of new system architectures as Print Circuit Board (PCB) systems had high latencies to communicate between different ICs. Thus System-on-chips (SoCs) were introduced where many electronic functions are embedded in the same silicon die. As the number of processor cores on the chip increased and the bus interconnection was not enough to accomplish the inter communication speed requirements, Network-on-Chips (NoCs) appeared where telecommunication methodologies are applied to inter-processor communications on chip. Finally, the high computation power demand for High Performance Computing (HPC) motivated the embedding of many sets of processors on the same chip called Multi-Processor System-on-chip (MPSoC) [JERR04]).

The main components of a SoC or MPSoC are the Processing Elements (PE), the memories and the interconnection. SoCs can be classified into homogeneous and heterogeneous. Homogenous SoCs have only one type of PE that is instantiated several times and it is connected to distributed or shared memories by using a dedicated interconnection, whereas heterogeneous SoCs have different types of PEs such as general purpose processors, Digital Processing Processors (DSPs), hardware accelerators etc. Those different PEs use a shared interconnection medium such as a bus or NoC [HÜBN10]. A comparison between a homogenous shared memory SoC and a heterogeneous SoC is presented in Figure 2-8.

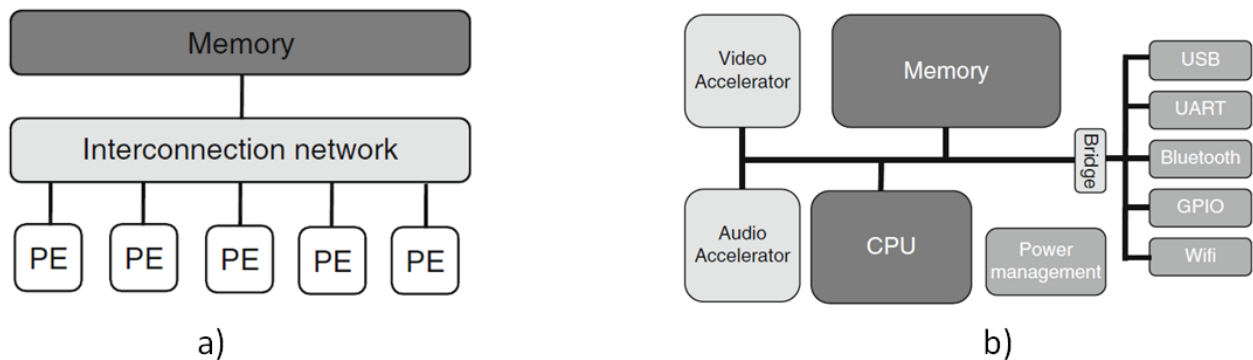


Figure 2-8. Homogenous vs Heterogeneous SoC approaches. a) Shared memory homogenous MPSoC b) Heterogeneous SoC

Different general purpose processors can be embedded in SoCs. This work will focus in Reduced Instruction Set Computer (RISC) ARM processors that are commonly used in embedded systems applications. Among different types of heterogeneous SoCs there is an interesting approach called reconfigurable or Programmable System-on-chip (PSoC) that offers high flexibility and power efficiency. Current PSoCs technologies include Processing System (PS) [XILI19] or Hard Processing System (HPS) [INTE20], Programmable Logic (PL), an extensible bus, I/O controllers and other resources.

A PS can include different types of hardware accelerators such as Video Control Unit (VCU), Graphics Processing Unit (GPU) and general purpose processors such as Real-time Processing Unit (RPU) and Application Processing Unit (APU). In addition, it also embeds different levels of cache memories and low capacity embedded memories such as On-chip-Memory (OCM), and Tightly Coupled Memory (TCM) used by a RPU. All of those memories use various optimized implementations of the SRAM memory cell.

The PL is implemented by using Field Programmable Gate Array (FPGA) technologies. FPGAs can be reconfigured by using SRAM [XILI19][INTE20] and Flash [MICR20A] memory cells, or one-time configured by antifuses [MICR20B]. FPGAs are composed by peripheral IOs and an array of Configurable Logic Blocks (CLBs) whose interconnections can be customized by routing switches [WEHA13], as illustrated in Figure 2-9.

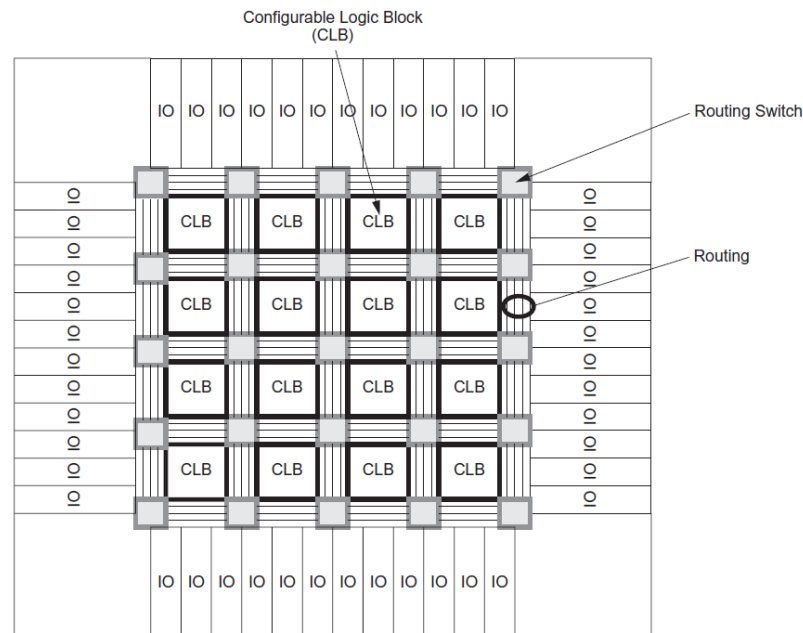


Figure 2-9. Simplified FPGA floor plan [WEHA13].

SRAM-based CLBs include Look-up Tables (LUTs) that can be used as RAM (LUTRAM) or to customize the combinatorial logic. CLBs also include multiplexers to customize the internal routing, arithmetic logics, and Flip-flops (FFs). Recent SRAM-based FPGAs also include DSP block columns, Block RAM (BRAM) columns, FIFOs, clock resources among other resources [XILI19]. Those resources are customized by loading a bitstream to a Configurable RAM (CRAM) array.

The PS communication with the PL are usually performed by using the Advanced eXtensible Interconnect (AXI) bus that supports multiple masters and slaves, high speed and bandwidth. For the communication between the PS and low speed IO peripherals such as Using the Universal Asynchronous Receiver Transmitter (UART) [FREE04] and General Purpose Input-Output (GPIO), the Advanced Peripheral Bus (APB) is used.

2.1.2.4. DCDC converters technologies for digital systems

The high integration of CMOS transistors followed by the Moore's law trend imposed a power supply voltage reduction to meet the current power consumption requirements. In addition, the gate dielectric thickness has been significantly decreased also requiring power supply voltage reduction to avoid breakdown. Thus, current CMOS components operate at very low voltages and are sensitive to small variations. Therefore, power regulation components play an essential and vital role in a digital system.

DCDC converters are power regulator devices that convert a Direct Current (DC) voltage into a higher or lower DC voltage. When they convert the input voltage to a higher voltage they are classified as step-up

converters, and when it converts to a lower voltage it is classified as step-down converters. They can be linear by using resistors, capacitive or inductive. Inductive step-down DCDC converts can be implemented in different topologies such as Buck, Bridge, and Watkins-Johnson [WENS11]. The basic operation of a switching buck DCDC converter is to use a control circuit to connect and disconnect a voltage of an inductor generating current ramps that are equivalent to the DC load current [INST12].

The control system of a DCDC converter has to be immune against load and line variations. Different control system strategies are available including Pulse-Width Modulation (PWM), Pulse-Frequency Modulation (PFM) and Constant On/Off Time (COOT). In PWM control systems of DCDC converters, the output voltage differences are corrected by changing the high level time in which the inductor is connected [WENS11]. A simplified block diagram of a current PWM Buck step-down regulator used in this work is presented in Figure 2-10 [INFI13].

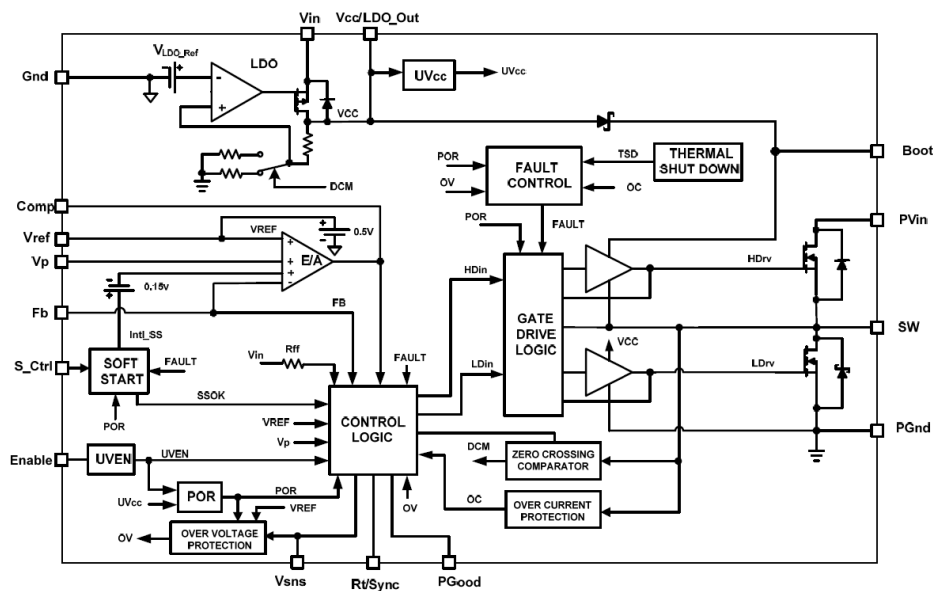


Figure 2-10. Simplified block diagram of a PWM-Buck step-down DCDC converter [INFI13].

As it can be seen in the figure, modern DCDC converters also include different protection circuits such as over voltage protection and fault control by shutting down the output when a high temperature is reached.

2.1.3. System platform solutions for aerospace and ground applications

In this section, different alternatives for integrating components to build aerospace and high reliability ground embedded systems and subsystems will be presented.

2.1.3.1. Fully commercial vs custom-designed systems

A complete aerospace, or high reliability ground application system is composed by several subsystems PCBs that embed electronic components for delivering a given functionality. As an example, a Mission Database (MDB) CubeSat contains stacked power condition, battery, digital processor, and interface PCB boards. As a payload it contains, power assembly, signal processing and transceiver PCB boards. Those different subsystems can be implemented by different ways and can embed different product grades depending on the radiation environment and the risk acceptance level [BAUM18][ROTH17].

PCB subsystems can be fully commercial when component selection and PCB assembly manufacturing is performed by the vendor or manufacturer, or custom-designed when the end-user selects the components and designs the boards. Depending on the application the end-user can even design and test their own IC components. An example of those different system or subsystem design strategies is the design of electronic systems for the accelerators at CERN. In regions where the radiation levels are not so high, fully-commercial systems can be used without testing. In areas exposed to higher radiation levels, COTS components are tested and selected before being embedded in a custom-design system. Finally, in extreme high radiation levels, custom designed systems embedding Radiation-hardened (Rad-hard) components are used [UABM17]. Fully commercial and custom-design subsystems can be implemented by using different hardware system approaches that will be presented in the next sub-subsection.

2.1.3.2. *Hardware system approaches*

Different hardware system approaches can be used to implement components or even entire digital embedded systems. An interesting approach is the System-in-Package (SiP) where different ICs are enclosed in the same miniaturized package. The ICs can be integrated in a 2-dimensional (2D) side-by-side way or in 3-dimensional (3D) vertical stacked way. SiPs can be used to integrate subsystems such as memory systems, programmable logics, power converters and transceivers [DPLU20]. Alternatively, Package-on-package (PoP), as the name implies, is the vertical stacking of different packages to build a system or sub-system. The different packages can be connected by using solder bumps and routed inside the substrate layers [CAMP11]. Stacked packages can be single-die ICs or even a SiP, as illustrated in Figure 2-11.

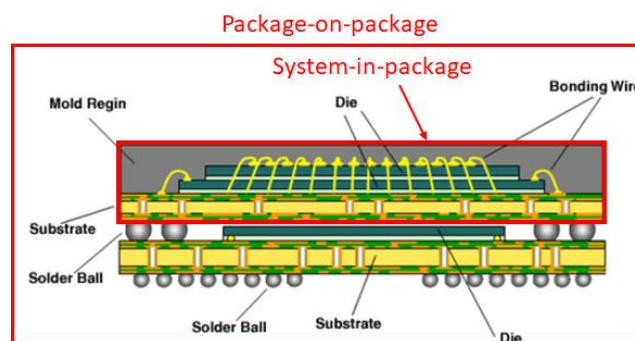


Figure 2-11. Package-on-package (PoP) hardware system. Package on the top is a SiP. [AY20]

An alternative for SiP and PoP integrated systems are the SoCs that include many functionalities in a single die, as discussed in the sub-subsection 2.1.2.3.

SiP, PoP or SoCs packages are embedded on a PCB board to build a complete computer system. However, in order to communicate with the outside analog world, additional components, not directly related to the operation of the digital system itself, have also to be embedded on the PCB board. Those additional components include external power management, Electrostatic Discharge (ESD) protection circuits, IO connectors, Human Machine Interface (HMI), IO transceiver among other components depending on the application. Two different approaches can be used to implement a whole PCB digital system or subsystem. It can be implemented by embedding all of the additional components and connectors on a single PCB board, also called Single Board Computer (SBC) or by two or more PCB boards. SBCs are not so flexible since once

the PCB is manufactured, it is very expensive to change or add embedded systems components or functionalities [AYIB18] [ABBC14].

Alternatively, a computer system can be composed by a Carrier Board (CB) to embed all the additional components and connectors, and a System-on-Module (SoM) [SOML20] or Computer-on-Module (CoM) [VERS20] board to embed the digital system components. SoMs are ready-to-use processor modules that include memories, transceivers, internal power regulators and a processing core. A processing core can be implemented by different packages such as SoC, SiP and PoP. Thus, it offers high flexibility, custom engineering and lower time to market. A picture of a CB embedding a SoM is presented in Figure 2-12.

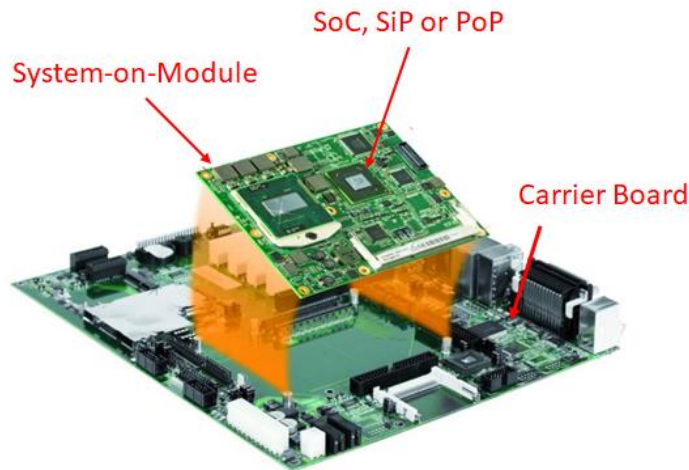


Figure 2-12. Carrier board embedding a System-on-Module that also embed SoC, SiP or PoP packages [AYIB18].

2.2. RADIATION EFFECTS

In this section the fundamentals for understanding the radiation effects in digital system will be explained. First, the radiation levels of different environments will be explained, second, practical-matter interaction physics and standard radiation measurements will be described. Finally, non-cumulative and cumulative ionizing effects on digital devices, device characterization and hardness assurance will be described. As non-ionizing cumulative effects are not a big concern for non-optics devices in this work, they will not be covered.

2.2.1. Radiation environments

The radiation environments can be divided into space, atmospheric and ground environments. The space environment will be defined in the three first sub-subsections followed by the atmospheric and ground environments.

2.2.1.1. Galactic Cosmic Rays

Galactic Cosmic rays (GCR) are originated outside of our solar system and are characterized by having decreasing fluxes with the energy that can reach up to $1.00 \text{ E}+12 \text{ GeV}$ per particle [GAIS16], as plotted Figure 2-14. The mechanisms that accelerate those particles to such high energies are not well understood yet [XAPS18].

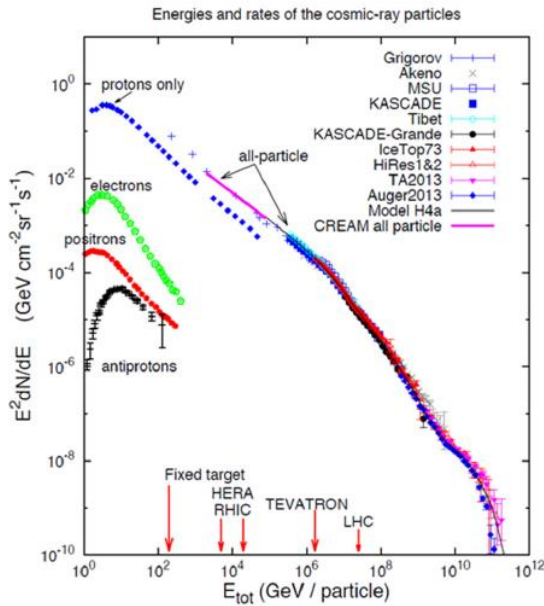


Figure 2-14. Overview of the energy spectra of various components of the cosmic radiation. Original taken from [GA16] and adapted by [SAN17].

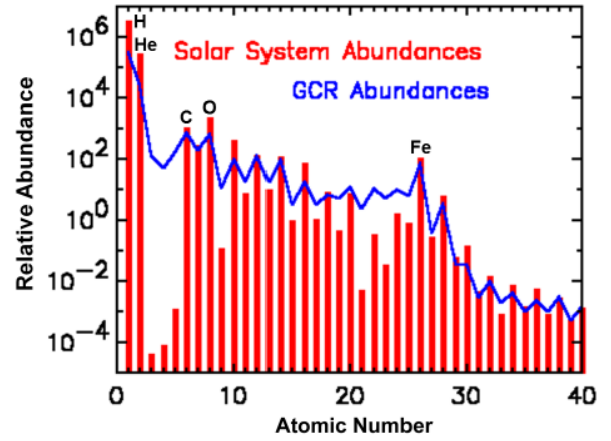


Figure 2-13. Comparison of the relative abundances of galactic cosmic rays and solar system ions [XAP18].

As we can see in Figure 2-14, about 99% of the total flux are atomic nuclei and 1% are electrons among other particles. GCR and Solar Systems relative abundances per atomic number are plotted in Figure 2-13. It is possible to see that 90% of the particles are protons, 9% alpha particles and 1% heavy ions [SANT17]. The European Space Components Coordination (ESCC) standard GCR model is the ISO 15390 [ISO04] that models the flux modulation due to both solar cycles and large scale heliospheric changes.

2.2.1.2. Solar Energetic Particles

Solar Energetic Particles (SEPs) can be originated from Coronal Mass Ejections (CME), shown in Figure 2-15 and solar winds.

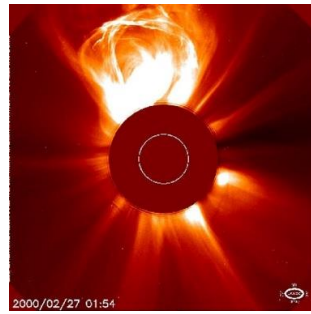


Figure 2-15. A Coronal mass ejection taken in 2000 by SOHO LASCO C2 [ZEL17a].

CMEs are large eruptions of billions of tons of plasma whose hadron composition consists of 96.4% protons, 3.5% alpha particles and about 0.1 heavier ions reaching energies up to approximately GeV/u and taking hours to days to reach the earth surface. Solar flares are burst of electromagnetism (EM) that usually accompany SEPs composed by 70% protons, 26% alpha particles and 2% heavier ions that reaches the earth surface in minutes [ARTO18]. CMEs and solar flares are Solar Particle Events (SPE) that are characterized by high fluxes during a short period of time [XAPS18].

Solar cycles have a period of about ~11 years consisting of 7 years of solar maximum and 4 years of solar minimum [XAPS18]. High solar activity decreases GCR fluxes and increase SPE probability [BART97]. The ESCC standard model for protons is the Emission of Solar Protons (ESP) [XASU00] model. The ESCC standard model for SEP heavy ions is the Prediction of Solar Particles Yields for Characterizing Integrated Circuits (PSYCHIC) [JGHC12] model that provides the yearly fluence of heavier ions normalized from alpha particle data measurements during solar maximum.

2.2.1.3. Van-Allen belt

Solar winds compress the earth magnetosphere that traps protons and electrons forming the Van-Allen belt radiation environment [XAPS18], as shown in Figure 2-16 [NASA02].

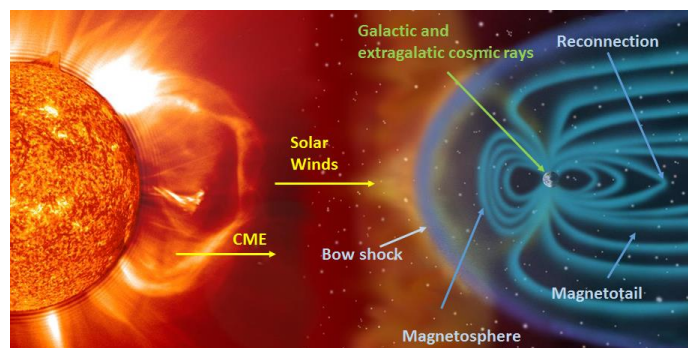


Figure 2-16. Illustration of the influence of SPE such as Solar winds and CME on the Earth's magnetosphere shape including the interactions of GCR and the Earth's atmosphere [Nasa02].

Trapped particles are mapped in (B, L) dipole coordinates, where B is the magnetic field strength and L the equatorial distance in earth radii.

The proton belt inner edge is localized at $L = 1.14$ and extends up to $L = 10$, beyond GEO altitudes. However high energy protons ($> 10\text{MeV}$ up to $\sim\text{GeV}$) have a significant flux at altitudes below $20,000\text{km}$ ($L \sim 4$ earth radii) as it can be seen in Figure 2-17. At MEO and GEO altitudes [SANT17], the magnetic field is weaker and mostly low energy protons are trapped ($< 10\text{MeV}$). On the other hand, trapped electrons have Kinect energies lower 10MeV . The electron belt can be divided into inner zone ($L = 1$ to 2) and outer zone ($L = 3$ to 10), and consequently it dominates the MEO and GEO altitudes, as it can be seen in Figure 2-18 [BOXA08].

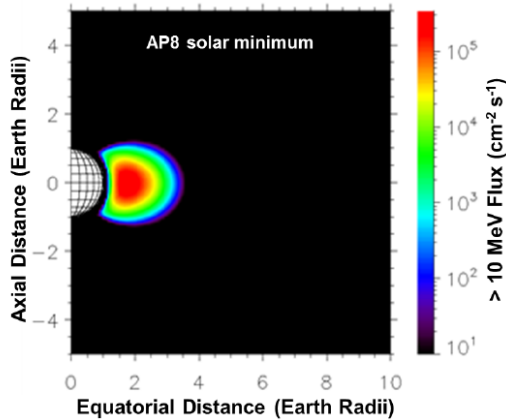


Figure 2-17. Trapped proton fluences $> 10\text{MeV}$ mapped in a dipole coordinates system [BOXA08].

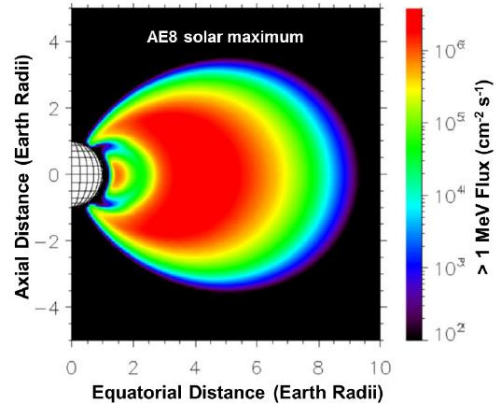


Figure 2-18. Trapped electron fluxes $> 1\text{MeV}$ according to the AE-8 model during solar maximum [BOXA08].

In general, proton populations are stable. However, CME can reconfigure the geomagnetic field increasing proton fluxes. Additionally, as the geomagnetic dipole axis is tilted (11.3°) and offset (800km) according to the earth, the lower edge of the proton belt, which have energies higher 35MeV , is localized at low altitudes of about 840km over the South America, as illustrated in Figure 2-19 [JOHG15]. This effect is called the South Atlantic Anomaly (SAA).

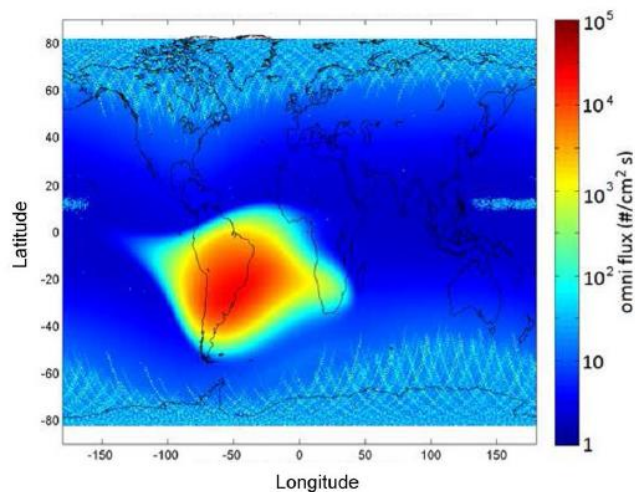


Figure 2-19. Contour plot of proton fluxes $> 35\text{MeV}$ in the SAA at an altitude of about 840km measured by the Polar Orbiting Earth Satellite (POES) from July 1998 to December 2011 [JOHG15].

The *de facto* standard global models are the AP-8 for protons [SAWY76] and AE-8 for electrons [VETT91] based on measurements from 1960-1970. Its update, AX9 model [GOHJ13] includes recent measurements from 1976 and 2016, confidence level calculations, geomagnetic variation and natural

environment variability estimation by using Montecarlo simulations. Alternately, new local models were proposed including ONERA Proton Altitude Low (OPAL) [BSLC14] for LEO missions, MEO-V2 model [SICA06], and the ONERA IGE-2006 for GEO missions [SBBF08].

2.2.1.4. Atmospheric environment

High energy GCRs ($>> \text{GeV}$) and SEPs that are not depleted away by the Earth's geomagnetic field interact with the atmosphere's atoms resulting in a complex shower of particles that undergo further interactions and decays generating secondary, tertiary particles and so on, as illustrated in Figure 2-20 [BAUM13]. The showers can be divided into electromagnetic (gamma rays, electrons and muons) and hadronic showers (protons, neutrons and pions) [SANT17]. In the upper atmosphere, protons and neutrons are the most abundant particles. However, as protons suffer losses due to coulombic interactions with atmosphere atoms, their fluxes have a higher reduction with altitude. Secondary particle fluxes depends on the altitude and latitude, as plotted in Figure 2-21 for the relative neutron fluxes [GGRZ04].

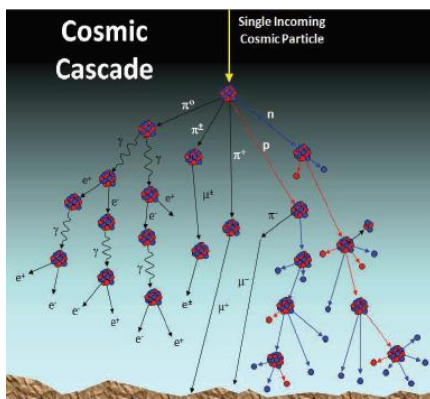


Figure 2-20. Energetic cosmic ray particle incident on the Earth's atmosphere and the resultant particle cascade [BAUM13].

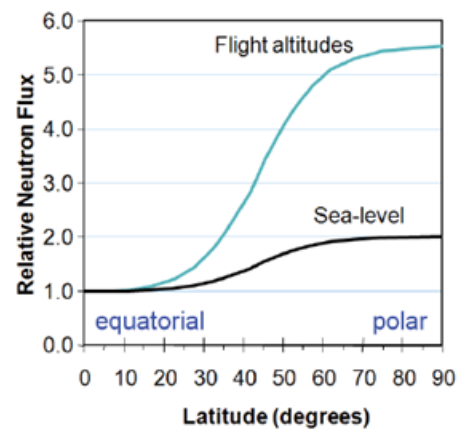


Figure 2-21. Relative neutron fluxes variation with latitude and sea-level and flight altitudes [GGRZ04].

Secondary neutrons have the highest flux at flight altitudes (9-18km) being the main concern for avionics operation [SANT17][NORM96]. At sea level, the secondary fluxes correspond to less than 1% of the primary fluxes and being composed by mostly muons, electrons and neutrons. The energy spectra of some particles at ground level is presented in Figure 2-22 [ZIEG98]. Although muons and electrons have the highest

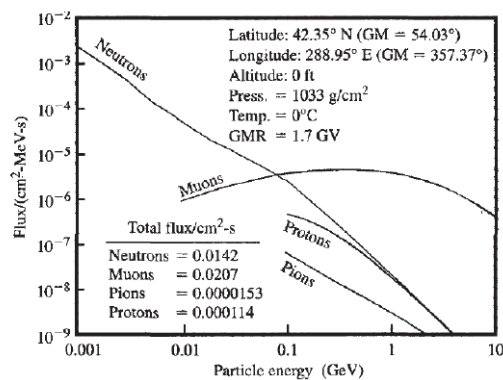


Figure 2-22. Terrestrial particle flux from cosmic sources as a function of particle energy [ZIEG98].

fluxes at sea level, they have a lower capability of generating errors (in the current digital technologies), thus high energy neutrons are also the main concern for ground application reliability.

The International Electrotechnical Commission (IEC) 62396 standard [IEC14] for radiation effects in avionics establishes the atmospheric models for calculating the neutron fluxes. A recent addition addresses the 1956 Ground Level Enhancement (GLE) event in order to calculate neutron flux enhancement ($>10\text{MeV}$) for altitudes of 12km [IEC17]. For ground level commercial applications, usually secondary fluxes are extrapolated from a standard location. The JEDEC89A standard [JEDEC06] establishes the sea-level N.Y.C high energy ($>1\text{MeV}$) neutron flux as the standard location. Neutron fluxes at different geographic positions can be calculated by using a conversion factor from the M.A Shea and D.F Smart model and the International Geomagnetic Reference Field from 1995 [SMAR95].

2.2.1.5. Radiation sources at ground level

The radiation sources at ground level that are not associated to the atmospheric environment can be divided into natural radiation and man-made radiation. The natural radiation sources or natural radionuclides are radioactive products of GCR origin, natural radioactive decay products and radiation emitted by microelectronic materials. Those natural sources of radiation include mainly alpha and beta emissions including gamma and X-ray photon emissions. The main concern of radiation emitted by microelectronic materials are alpha particles. Those alpha particles can reach 4-9MeV energies that can be enough to generate errors in microelectronics. Impurities on bulk silicon such as Uranium-238 can emit alpha particle whose flux is about $2.56 \text{ E-}06/\text{cm}^2/\text{s}$. In addition, solder bump of flipchip packages can emit alpha particles, which if not shielded by isolation layers, can also induce to errors [SANT17]. A simulation of alpha particle spectra that can be emitted by impurities in a package part is plotted in Figure 2-24.

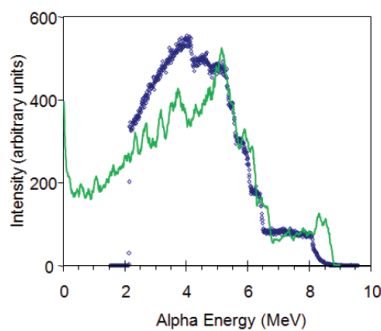


Figure 2-24. Measured alpha particle spectrum obtained from a thick foil of ^{232}Th and simulated spectrum (green) from $\text{U}^{238}/\text{Th}^{232}$ impurities in a package part [Baum13].

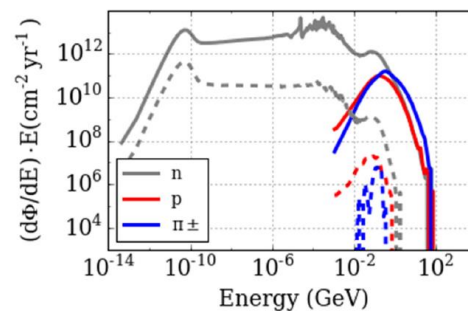


Figure 2-23. Particle energy spectra in the LHC tunnel. Solid lines correspond to the LHC tunnel and dashed lines correspond to the UI shielded location [Sant17].

The man-made radiation sources include nuclear power plants and particle accelerators used for scientific research purposes and medicine applications. Nuclear power plants are out of the scope of this work. An example of particle accelerator environment is the Large Hadron Collider (LHC) tunnel that has High Energy Hadrons (HEH) reaching energies of about 200GeV, as plotted in Figure 2-23. It also possible to see the shielding effect on the dashed lines in which thermal neutrons are less affected.

The radiation levels of different environments were presented. A summary of the radiation levels of the most important locations and events are summarized in Table 2-1.

Table 2-1. Summary of main radiation environments radiation levels including energy, flux and particle abundances

Radiation environment	Particles	Energy	Flux	Peak flux (>10MeV/u)	Integral fluence (>10MeV/u)
GCR	90% protons 9% alphas 1% heavier ions	Up to ~1E+11 GeV	1 to 10/cm2/s		
Solar CME	96.4% protons 3.5% alphas ~0.1% heavier ions	Up to ~GeV/u		Up to ~1E+06 /cm2/s	Up to ~1E+10 /cm2
Trapped protons (L = 1.14-10)	Protons	Up to ~GeV	(> 10MeV) Up to ~ E+05/cm2/s		
Trapped electrons Inner zone (L = 1-2)	Electrons	Up to 5 MeV	(> 1MeV) 1E+02-1E+06 /cm2/s		
Trapped electrons Outer zone (L = 3-10)	Electrons	Up to 10 MeV	(> 1MeV) ~3E+06 /cm2/s		
NYC at ground level	Neutrons	>10MeV	~3E-3 /cm2/s		

The composition of those particles, their energies and fluxes will define how they interact with CMOS materials and generate different radiation effects that will be explained in the next sections.

2.2.2. Particle-component interaction

This subsection is organized as follows: first sub-subsection will describe the electromagnetic and particle ionizing mechanisms, second sub-subsection will present the common methodologies to measure ionizing energy deposition, and finally, in the third sub-subsection, the mechanisms by which radiation can be accumulated in CMOS materials will be defined.

2.2.2.1. Radiation energy loss in CMOS components

The radiation present in the different radiation environments previously explained can be classified into electromagnetic and particle radiation. In the electromagnetic radiation, photons can interact with matter by three different mechanisms: photoelectric effect, Compton scattering and pair production, as illustrated in Figure 2-25. In the photoelectric effect the total energy of the photon is transferred to the electrons of the materials and the electron current will depend on the number of photons and its frequency. Whilst, in the Compton scattering mechanism, a photon collides with an electron in an inelastic way transferring part of the energy for the recoil electron and part of energy for the scattered photon that changes its frequency. Finally, in the pair production a photon induces the generation of an elementary particle and its antiparticle from a neutral boson, where photon energy is transferred to the kinetic energy of the generated particles. The dominant

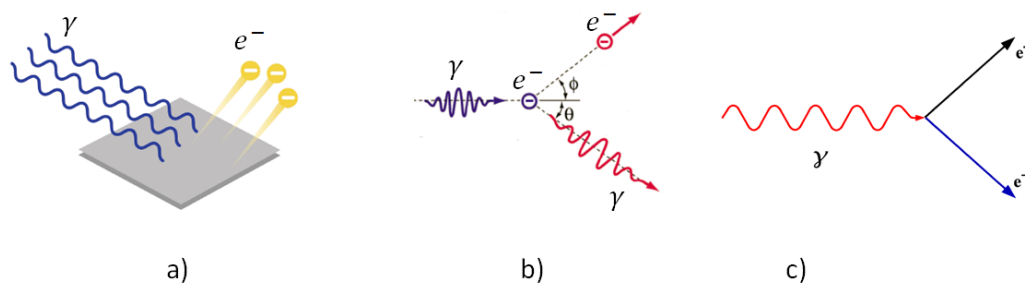


Figure 2-25. Illustration of electromagnetic-particle interactions: a) photoelectric effect, b) Compton scattering and c) pair production

electromagnetism mechanism will depend on the photon energy and the target material, as reported by [FBMC87]. For instance, when irradiating silicon with 10 KeV X-ray, the dominant mechanism is the photoelectric effect and when irradiating with 1.25MeV Co60 the dominant effect is the Compton scattering.

Particle radiation energy losses in target material can be divided into: electronic stopping power, nuclear stopping power, nuclear reactions, electromagnetic and chemical reactions. Electronic stopping is an inelastic interaction leading to excitation and ionization of both projectile and target atoms, and electron capture. Two most well-known theories are the Bohr's model from classical derivation and Beth-Bloch model from quantum mechanisms. Electronic stopping power is responsible for direct ionization where the projectile generates electron-hole pairs along its path until stopping at a given depth of the material or traversing it. An illustration of a direct ionization by a heavy-ion in a CMOS technology is presented in Figure 2-26.

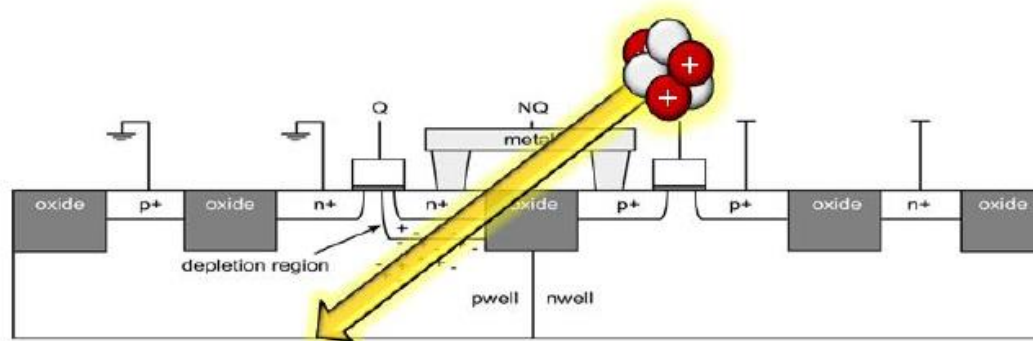


Figure 2-26. Direct ionization in a CMOS technology

The penetration depth in the material will depend on the projectile energy and type, the target material and its density. Ions heavier than protons and alpha particles mainly produce direct ionization. Heavy ions with energies commonly available in ground facilities cannot penetrate the IC package material, metal layers and substrate until reaching the sensitive regions of CMOS technologies. Thus, usually IC package delidding and substrate thinning are required for performing heavy-ion testing in digital components. In addition to that, air medium has also to have to be considered as the projectile will lose energy through it before reaching the target material. Thus, depending on the heavy-ion energy, the component under test has to be placed in a vacuum chamber.

Nuclear reactions occur when the projectile energy exceeds the coulomb barrier. In this mechanism the impinging particle reacts with the target material nucleus generating secondary particles that ionize the target material. Thus, this mechanism is called indirect ionization. It occurs mainly with protons and always with neutrons. However, it also depends on the target material. An illustration of a proton nuclear reaction in CMOS target materials is presented in Figure 2-27.

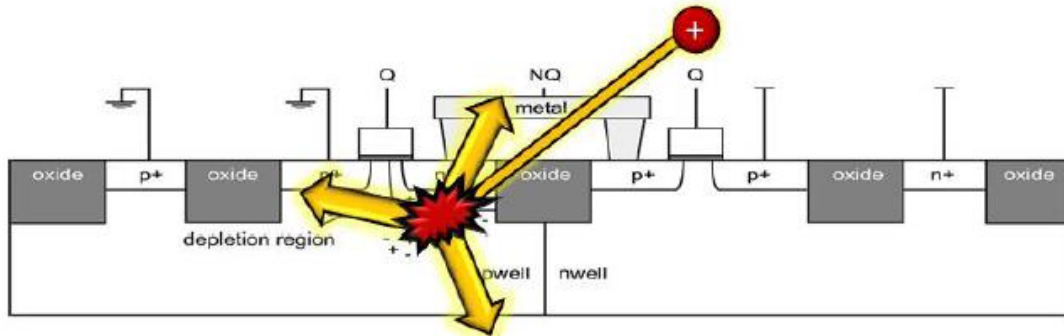


Figure 2-27. Indirect ionization in a CMOS technology

High energy protons and neutrons can easily penetrate the different package materials, substrate and metal layers reaching the sensitive area of a CMOS technology and having an influence in the component operation.

2.2.2.2. Linear Energy Transfer and projected range

When direct or indirect ionization occurs, electron-holes pair are created. A fraction of the total carriers generated can recombine. The average number of electron-hole pairs created can be calculated by the Linear Energy Transfer (LET) that represents the average deposited energy per length [ARTO18]. LET is typically estimated as energy loss per unit distance due to electronic stopping power, as stated by:

$$LET = \left. \frac{dE}{dx} \right|_{elec.} \quad 2-1$$

However, there is also a small contribution of the indirect ionization of nuclear reactions. The deposited energy by an ion track depends on its angle of incidence, as illustrated in Figure 2-28 .

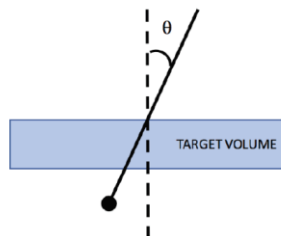


Figure 2-28. Angled incidence of ion in target for calculating effective LET

When the area of a die is much greater than its thickness and when the ion range is much greater than the target thickness divided by the cosine of the angle of incidence, the effective LET can be calculated by Equation:

$$LET_{eff} = \frac{LET}{\cos(\theta)} \quad 2-2$$

As the modern technologies have very thin die thickness and small areas this approach have to be applied with caution.

LET is commonly used to measure energy deposited by heavy-ions and the particle energy is used for protons and neutrons [JAVA19].

Ion traversing CMOS materials can be usually projected in ranges from tens to hundreds of microns. The energy deposition strength (LET) per target material depth can be represented by the Bragg curve. Bragg curves of heavy-ions for the 16.3MeV/u cocktail are plotted in Figure 2-29.

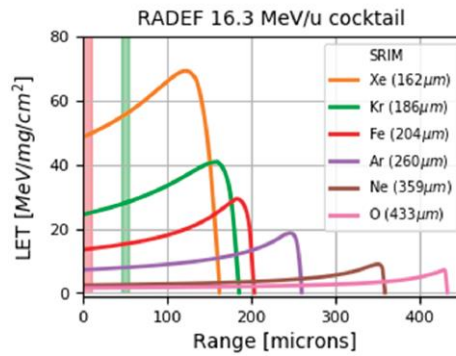


Figure 2-29. RADEF Bragg curves for the 16.3MeV/u cock tail [JAVA19]

As it can be seen the LET increases as the depth increases until reaching the maximum LET, called Bragg-peak, after that the LET abruptly decreases defining the maximum range of the particle. It also possible to note that as high is maximum LET as lower is range in silicon. Therefore, a balance has to be found between LET and range, so that Bragg peak of the LET is located in the sensitive area of the IC die. As some IC packages have thicknesses in an order of few millimeters, the common approach is remove the package (package delidding or decapsulation) and perform die thinning so that a maximum LET can be used.

2.2.2.3. Fixed and interface traps

When electron-hole pairs are generated in isolation regions, as the gate dielectric, a fraction of the total carriers escape from initial recombination. This fraction depends on the electric field in the dielectric and projectile particle and energy. Electrons have a higher mobility than holes and are easily captured by the metal gate when an NMOS transistor is biased, or can be annihilated by recombination. Holes that are not recombined can be trapped in shallow fixed traps in the dielectric.

Occupied fixed trap charges are always positive. Holes also undergo hopping movement via fixed traps until falling in deep trap sites characterized by oxygen vacancies that are few nanometers far from the SiO₂ interface. Protons can also be generated by ionization and move deep in the oxide until the SiO₂/Si interface breaking de-passivated PbH defect centers and generating interface traps. Interface traps are occupied when the transistor is in the inversion mode and have negative charges for NMOS devices and positive charges for PMOS devices [JAF15]. This process is illustrated in the Figure 2-30.

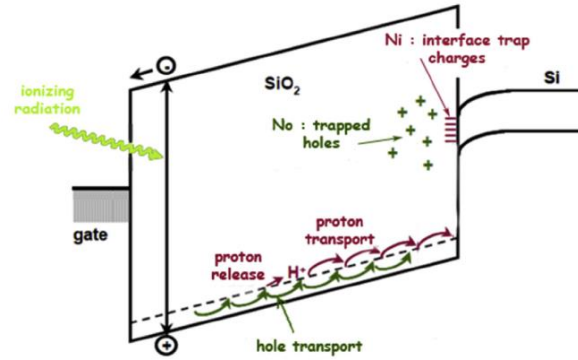


Figure 2-30 Band diagram representation of carrier transport in a NMOS structure [JAF15].

2.2.3. Single Event Effects

Localized ionizing tracks caused by heavy-ions or spread ionization tracks caused by high energy neutron interaction with the nucleus of the target material can transverse the sensitive part of an integrated circuit, as the p-n junction of a node weakly driven. When it occurs, the carriers of the ionizing track are collected by the electric field in the depletion region generating a drift current in the node. The depletion region is deformed in a funnel shape extending it deep in the semiconductor, the shape of the funnel depends on the doping of the semiconductor. The charge carriers diffuse inside the semiconductor generating a diffusion current until the carriers are diffused away from the depletion region, collected or recombined. The charge collection and diffusion occurs simultaneously and generate a pulse in the node whose time characteristics will depend on the particle characteristics and circuit parameters. This process to generate a voltage pulse in the node is illustrated in Figure 2-31 [BAUM05].

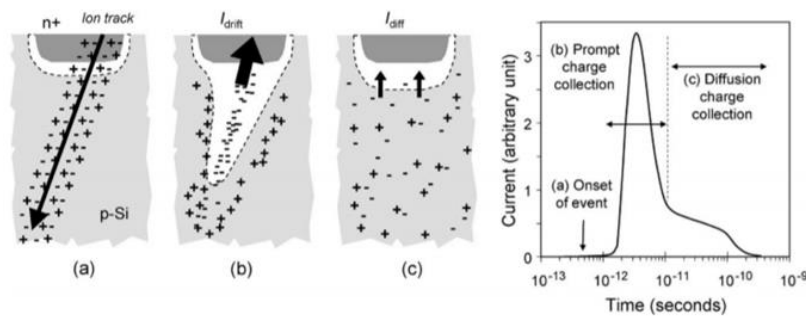


Figure 2-31. The three process of a Single Event Effect a) Electron-hole generation due to the ionizing track. b) Potential funneling due to the high electric field c) Current diffusion [BAUM05].

The collected charge has to exceed a critical charge to change the state of a memory cell in a circuit. In addition, depending on the size of the circuit, the charge can be shared with neighbor structures generating multiples effects. The critical charge depends on the operation voltage, the state of the circuit, the topology of the circuit, the doping level, and the bias of other nodes connected, then making a generic SEE model really complex to be developed [WARR12]. In the following, we focus only on SEE that concern digital devices.

2.2.3.1. Single Event Transient

Single Event Transient (SET) is characterized by a voltage or current spike in an integrated circuit node caused by a single impinging energetic particle [JEDE06]. SETs in analog devices are more critical than

in digital devices, as they change the desired voltage or current level of circuit (operational amplifiers or power regulators), whereas in digital devices, they have to be captured (stored) in a sequential cell and change its logic value to have an impact on the circuit functionality. The capturing of an SET by a memory cell depends on the bias condition, circuit architecture and time characteristics of the pulse. An example of SET effect is the heavy-ion characterization of a 65nm Flash-based FPGA [RDWJ15]. In this experiment, the authors concluded that at higher frequencies the SEU cross-section in flip-flops is higher because the probability of capturing SET is increased. They also analyzed the impact of different buffer lengths as it can be seen in Figure 2-32.

2.2.3.2. Single Event Upset

A Single Event Upset (SEU) is a soft error caused by a transient pulse generated by a single energetic particle (SET). A soft-error, in turns, is a wrong output signal from a latch or memory cell that can be corrected by applying normal functions of the device in which the latch or memory cell is contained. When a single energetic particle causes several bits of an integrated circuit to be fail at once, it is defined as a Multiple Cell Upset (MCU) and when a single energetic particle causes multiple bits of a word to fail it is defined as Multi Bit Upset (MBU) [JEDE06].

One example of SEU and MBU is the heavy-ion characterization of a 32Gb NAND Flash presented in Figure 2-33. The plot shows the Single Bit-Upset (SBU) or SEU, and different MBU cross-sections versus the heavy-ion LET [HHMM17]. As it can be seen, 6 and 7 upsets per word are seen when LET exceeds 50 MeV/mg/cm^2 .

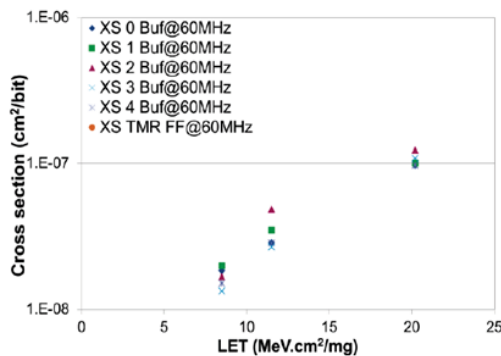


Figure 2-32. SET characterization of a FLASH-based FPGA for different Buffer lengths at 60MHz and Triple Modular Redundancy [RDWJ15].

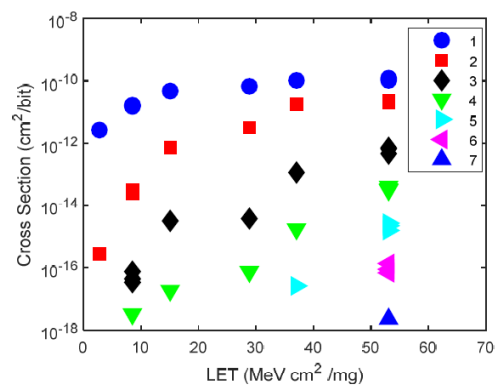


Figure 2-33. SBU and MBU cross-section of a 32Gb NAND Flash [HHMM17]

2.2.3.3. Single Event Functional Interrupt

Single Event Functional Interrupt (SEFI) is an event that makes a component to reset, lock-up or to have other malfunctioning that can be detected. When a SEFI is corrected by just repeating the operation or resetting the device, it is classified as a Soft SEFI and when the SEFI requires a device power cycle to be corrected, it is classified as a Hard SEFI. SEFIs are common in the control logic of memories or in the configuration memory of FPGAs. One example of SEFI effect is presented in a heavy-ion characterization of DDR3 memories with different capacities [WKHF18]. In this experiment they analyzed the SEFI occurrence for different operation modes: write, read/write and storage, as presented in Figure 2-34.

2.2.3.4. Single Event Latch-up

When an abnormal high current state, caused by ionizing effect of a single energetic particle, makes a device loses its functionality, it is defined as a Single Event Latch-up (SEL). SEL can cause a permanent damage or not. When a permanent damage occurs, it is not possible recover the normal functionality of the device even when a power-cycling is performed. In CMOS technologies, SEL is the result from the activation of the thyristor like junction (p-n-p-n) shorted between the supply voltage and ground caused by a single energetic particle [JEDE06]. One example of micro-SEL, characterized by a limited current increase, is presented in the heavy-ion characterization of a 28nm SoC [IRAM15]. In this experiment, the authors measured the current of the auxiliary voltage supply (VCCAUX) along the heavy-ion experiments, where it was possible to see step increments in the current that can represent sequential SELs in the SoC, as shown in Figure 2-35.

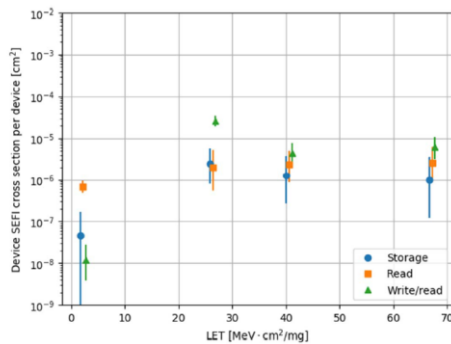


Figure 2-34. SEFI characterization of a DDR3 for different operation modes [WKHF18].

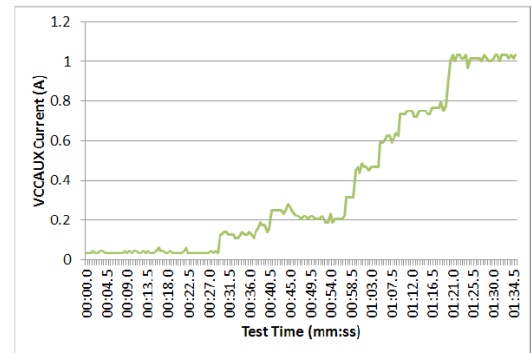


Figure 2-35. VCCAUX current versus time of a Zynq 7000 SoC showing a micro SEL characteristic: [IRAM15].

2.2.3.5. Testing Methodologies and facilities

The standard SEE test methodology consists in irradiating a component with heavy-ions at different LETs or at different proton or neutron energies, and then counting the number of events. The number of events observed versus the particle fluence defines a sensitive area of a component for a given particle energy and this area is called cross-section, as defined in: [PETE98]

$$\sigma_{SEE}[cm^2] = \frac{\text{number of SEEs}}{\text{particle fluence} \left[\frac{1}{cm^2} \right]} \quad 2-3$$

The measurement of different cross-sections allows the plotting of cross-section curves as presented in Figure 2-36 where LET_{th} is threshold LET that represents the minimum energy deposition for error generation and σ_{sat} the saturation cross-section that is related to the projected area of the sensitive volume [MANG18].

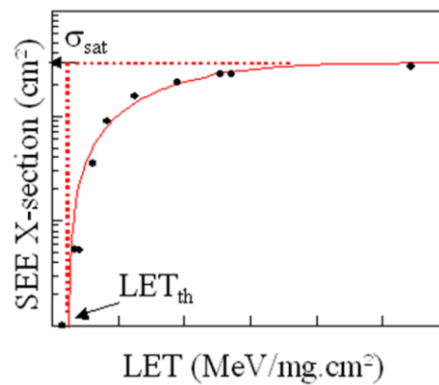


Figure 2-36. Typical cross-section curve for SEE [Mang19].

The SEE test methodologies are classically performed at component-level, however along the time emerging test methodologies such as the system-level methodology have been applied.

2.2.3.5.1. Classical SEE test approaches

The component-level SEE test methods are defined by the standards ESCC 25100 (all the parts), EIA/JESD 57, EIA/JESD 57A and EIA/JESD 89A [ESA14][JEDE06][JEDE96]. Those standards define the test procedures for heavy-ion, proton and neutron SEE characterization. The standards define the flux, fluence, particle energy, range (heavy-ions), the necessity of a vacuum chamber... For low energy (<10MeV/u), heavy-ion experiments, the standards state that the component has to be decapsulated and tested inside a vacuum chamber. For high energy heavy-ions (>10MeV/u), the experiment can be done in the air not requiring decapsulation.

An example of a facility with low energy heavy ions is the Université Catholique de Louvain (UCL) Heavy-Ion Facility (HIF) that provides energies between 9-10MeV/u using several ions from Carbon to Xenium, typical fluxes of few *particles/cm²/s* to $1.5E4 \text{ ions/cm}^2/\text{s}$ and a beam diameter of 2.5cm (10% of homogeneity) [STPL17].

Examples of high energy heavy ion facilities are the Grand Accélérateur National d'Ions Lourds (GANIL) [MODL17], Radiation Effects Facility (RADEF) [VHJK07], and Texas A&M University (TAMU)

facility [HYMA20]. The GANIL facility provides ions with energies up to 50MeV/u and fluxes from $1\text{E}+02\text{-E}+05 \text{ ions}/\text{cm}^2/\text{s}$. The RADEF facility provides energies per ion up to 22MeV/u and the maximum flux depends on ion species being able to reach up to $1\text{E}+05 \text{ ions}/\text{cm}^2/\text{s}$. Finally, the TAMU facility provides ions from helium to gold and 15.25MeV/u and 40MeV/u cocktails.

For proton energies above 20MeV and atmospheric neutrons, the experiment can be done in the air with the original package [BEZE18]. An example of proton facility for testing in air is the Lawrence Brookhaven National Laboratory (LBNL) that provides protons at discrete energies from 13.5 to 55 MeV and typical fluxes of $1\text{E}+07\text{-}1\text{E}08 \text{ p}/\text{cm}^2/\text{s}$. And an example of atmospheric neutron facility is the ChipIR facility of the Rutherford Appleton Laboratory that provides integrated neutron fluxes (Energy > 10MeV) up to $5\text{E}06 \text{ n}/\text{cm}^2/\text{s}$ depending on the device under test position [CBGC18].

An alternative radiation SEE testing methodology is the laser testing that is convenient for academic research purposes and industrial characterizations. In a laser experiment, a pulsed laser with a specific wavelength is focused in a decapsulated component by the front-side or back-side. The SEE cross-sections are plotted versus the laser pulse energy and can be correlated to heavy-ion LETs [BRWM12].

A complementary SEE characterization methodology that has been experimented by NASA for the past decade is to use high-energy (190MeV) protons for characterizing space applications for non-critical missions at system-level [GUGU17]. By using this energy, it is possible to generate more secondaries and make it possible to use mathematical gateways to extrapolate the results to heavy-ions [AMGU16]. An example of high energy protons (~190MeV) facility for system-level test is the KVI-Center for Advanced Radiation Technology (KVI-CART) that provides protons of energies up to 183MeV. The available fluxes are $5\text{E}+08 \text{ p}/\text{cm}^2/\text{s}$ for large fields, and $5\text{E}+11 \text{ p}/\text{cm}^2/\text{s}$ for small fields [GOGK09].

2.2.3.5.2. *Emerging SEE test approach*

SEE test methodologies at system-level started to be employed to reduce the cost of radiation characterization [SGPB18][GUGU17][LADB17]. System-level test consists in analyzing the radiation response of a system instead of the different functional units or components that compose it, as performed at component-level. System-level tests can be performed locally or globally. In local system-level experiments, complex components are tested, such as SoCs, and then the radiation response at system-level is analyzed, whereas, in global system-level experiments, the whole system is irradiated simultaneously.

Radiation facility requirements that allow system-level tests are large irradiation-field size and homogeneity, and high penetration depth. Homogenous large field sizes are required to simultaneously irradiate the different components in a system with the same flux. High penetration beams are required to reach the sensitive regions of the components having different package dimensions without having to perform sample preparation. In addition, high penetration beam is also required to reach components assembled on the two sides of a PCB or different PCBs of a stack. The field size and penetration requirements will depend on which

system is being considered. Therefore, different system classes have been defined in the context of the RADSAGA project, as presented in Table 2-2 [LOPE20].

Table 2-2. Definitions of system classes [LOPE20]

Class	Systems considered	Typical Volume (Length x Width x Height)
XS	SoC, SiP and PoP	2.5cm x 2.5cm x 1cm
S	Typical small-form-factor SoM	5.6cm x 5.4cm x 2.5cm
M	Typical two-sided SBC	16cm x 11cm x 5cm
L	Cubesat-like small system	10cm x 10cm x 10cm
XL	Maximum system volume	50cm x 50cm x 50cm

The volume of the different system classes will define whether the selected radiation facilities are suitable for testing them at system-level or not. For global system-level tests, a homogenous beam field area has to fit the system class area (Length x Width) and the beam penetration depth has to reach the system class depth (Height). For local system-level tests, the beam field has to be collimated to irradiate only one component/sub-system of a system class or internal resources of that component. In addition, the beam penetration depth has to be able to reach components embedded on any board of the stack and any side of the board.

Example of compliant system-level test facilities for some system classes are the ultra-high energy heavy-ions at the NASA Space Radiation Laboratory (NSRL) [BILA20], high energy protons at the KVI Center for Advanced Radiation Technology (KVI-CART), atmospheric-like neutrons at ISIS Neutron and Muon Source - ChipIR, mixed-field at the European Organization for Nuclear Research (CERN)-CHARM [MBAT15] and the Single Photon Absorption (SPA) laser facility (1064nm wavelength) at Institut d'Électronique et des Systèmes (IES) [IES20]. The parameters of the facilities and to which system classes they are compliant are summarized in Table 2-3.

Table 2-3. Overview of SEE system-level test facilities compliance for Global (G) and Local (L) tests [LOPE20].

Facilities	System class compliance										Facility parameters			
	XS		S		M		L		XL		Field size	Max. Energy (MeV)	Max. LET (Si) $\left(\frac{MeVcm^2}{mg}\right)$	Max. Range (Si) (cm)
	G	L	G	L	G	L	G	L	G	L				
NSRL heavy ions	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	60cm x 60cm	1500/u	~24.2	~222
KVI-CART protons	Y	Y	Y	Y	N	Y	N	N	N	N	13cm diam.	184	3.84E-3	~12
ChipIR neutrons	Y	Y	Y	Y	N	Y	N	Y	N	Y	11cm x 11cm	800	N/A	>10
CHARM	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	several meters	~1E+3	N/A	>50
IES Laser	N	Y	N	N	N	N	N	N	N	N	1um diam.	N/A	N/A	~0.07

SEE Radiation Hardness Assurance (RHA) activities aim to ensure that the system will meet the mission requirements until the end of the mission. The building blocks of a RHA methodology can be composed by environment definition, requirements definition, system and components evaluation, and mitigation alternatives. Environment definition can be divided into external environment to spacecraft, aircraft, or automobile, and internal environment. The definition of external environments provides the inputs for the radiation environment models previously described. The internal environment is the digital system itself, their components and the materials that will define how the particles are transported to the sensitive areas. In the requirements definition, the criticality factors of a mission should be defined in order to provide the risk acceptance levels [MCAM19].

Components and system evaluations are performed through testing, using existing data and performing data analysis. In order to perform data analysis, the SEE rate should be predicted. The ESCC standard for SEE rate prediction is to use the Integral Rectangular Parallel Piped (IRPP) method where the sensitive volume is modeled as a parallelepiped [PIBL80]. The energy spectrum from a mission environment is the input for transport calculation that returns the transmitted LET spectrum or proton energy spectrum. The cross-section curves per LET or proton energy are fitted by using Weibull or Bendel functions (protons). Finally, SEE rate is calculated by means of the convolution of the transmitted LET spectra or proton energy spectra with the fitted cross-section curve. Different tools can be used to estimate SEE rate including CREME96 based tools such as OMERE [OMER20] and Spenvis [KDME12], or directly calculated by the CREME-96 code [ADAM97].

After obtaining SEE rate, Worst Case Analysis (WCA) and Failure Mode, Effects and Criticality Analysis (FMECA) of circuit, equipment and system design are performed. If the mission requirements are not met, different mitigations strategies can be applied. Mitigations techniques can be applied at component-level such as part replacement, component-level shielding and error correction techniques, and at system-level such as latch-up protection circuitry or box level shielding. Finally, an iterative process continues where updated knowledge is used to review the parts list [MANG18].

2.2.4. Total Ionizing Dose

2.2.4.1. Parametric degradation and hard failures

Total Ionizing Dose (TID) is the accumulation of energy transferred from radiation to materials under the form of material ionization, which results in the accumulation of trapped charge in the IC dielectric materials. The gate dielectric and interface traps accumulated due to ionizing lead to threshold voltage, mobility degradation and Radiation Induced Leakage Current (RILC) [JAFB15]. TID is measured in rads or Gy and it depends on the density of the material, thus usually silicon is chosen as an approximation. Parametric degradation on digital circuits include performance and power degradation due a reduction of drive current and increase of leakage currents. Threshold voltage degradation also increase the sensitivity to intrinsic noise, as the logic voltage ranges are reduced. This signal integrity loss leads to intermittent errors in components and systems. At a certain dose, the transistors cannot switch anymore and the intermittent errors become constant errors being characterized as a hard failure. The accumulation of trapped charges due to TID on the floating gate of Flash memories can change its logic state. An example of TID-induced memory errors on a NAND Flash is presented in Figure 2-37 [NGIR10].

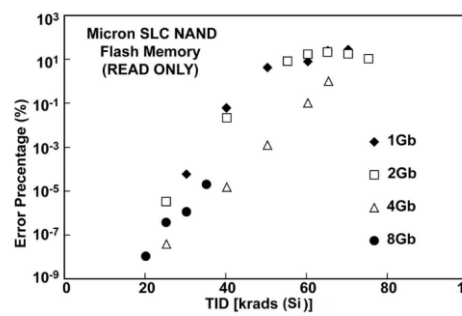


Figure 2-37. Percentage of data errors versus dose for Micron Flash Memories [NGIR10]

As the threshold voltage degradation due to TID effect is proportional to the square of the oxide thickness, devices are becoming less tolerant to threshold voltage degradation due to TID. It happens because oxide traps in thinner devices are less stable and undergo more annealing due to electron tunneling. To this extent, currently the main concern is the oxide trap generation in thicker insulators in the integrated circuit, such as STI and buried oxide of Silicon-on-Insulator (SOI). The oxide traps generation in those insulators generate Radiation Induced Leakage Current (RILC). Regarding STI, there are two kinds of leakage: Edge leakage and Inter-leakage [CLAE18].

After radiation exposition, the degradation of transistor parameters can be recovered, this process is referred to as annealing. It occurs because of the neutralization effect characterized by the electron tunneling and the thermal emission [MCWH90]. Annealing can be performed at room temperature (25°C) or can be accelerated at high temperatures ($T > 100^\circ\text{C}$). Interface traps are slightly annealed out even at high temperatures while the oxide traps are annealed out even at room temperature and can be accelerated at high temperatures. As the interface traps and oxide traps increase in different directions in NMOS devices, the annealing process initially recovers the transistor parameters, but after that, the threshold voltage is degraded again due to the interface traps, this process is called rebound effect [OLMC03].

2.2.4.2. *Testing Methodologies and facilities*

2.2.4.2.1. *Classical TID test approaches*

The conventional TID test methodology consists in irradiating a component in steps of fixed dose rates while electric parameters are measured to obtain parametric degradation versus dose. Irradiation steps are required so that parametric degradation recovery due to annealing can be measured. When it is possible, components are irradiated until a maximum dose to hard failure is achieved in order to measure component survivability.

TID experiments can have completely different results depending on the bias conditions, temperature, dose rate and the type of source. For this reason, the ESCC 22900 [ESA16], MIL-STD 883 Method 1019 [DOD04] and MIL-STD 750 Method 1019 [DOD95] standards were created to define the TID test methods. Those standards define the type of source, bias conditions, dose rate, temperature for annealing and other test parameters [BEZE18]. As the objective of TID experiments is to ionize uniformly components or systems, spread sources are commonly used, such as gamma rays or x-rays, instead of particle beams like heavy-ions or neutrons. Low energy protons can be used for doing TID experiments, however they have a lower fraction of unrecombined electron-hole pairs [ARTO18][GLZS18]. The standard type of source to perform TID experiments is Co60, because its emitted gamma-rays (1.1732MeV and 1.3325MeV) have a high ionizing power and range in comparison to X-rays and low energy protons [ARTO18][BEZE18]. An example of Co60 facility is the GAMRAY facility [TRAD20] that is based on a CEGELEC panoramic irradiator whose source activity is 400Cu (07/2016) and the dose rate is 1rad(Si)/h to 2Krad(Si)/h without shielding.

Alternatively, X-rays are a good option because it can achieve high dose rates and considerably higher fraction of unrecombined electron-pairs. In addition, low energy X-rays can well simulate proton rich space environments better than Co60 [SSPB01]. Mixed-field TID experiments can also be done in the CHARM facility at CERN, where different types of particles can irradiate the design under test such as gamma-rays, X-rays, protons... The CHARM facility can be configured by moving the shields where different positions can experimentally simulate different earth orbits or the atmospheric environment [MBAT15].

2.2.4.2.2. *Emerging TID test approach*

Regarding system-level characterization, Co60 and mixed-field radiation experiments can be done as they have high ranges. Low energy X-rays and protons have lower ranges than Co60, having a non-homogenous ionizing effect in the components of a system that have different thicknesses. This way, they are not suitable for doing system-level experiments. Examples of test facilities compliant to system-level TID tests are the Co⁶⁰ source at CERN, Office National d'Etudes et Recherches Aéronautiques (ONERA) [ONER20], Université Catholique de Louvain (UCL) [STPL17] and the (<360keV) X-ray source at IES [IES20].

The summary of the system class compliance of the cited facilities is presented in Table 2-4 [LOPE20].

Table 2-4. Overview of TID system-level test facilities compliance for Global (G) and Local (L) tests.

Facilities	System class compliance										Facility parameters			
	XS		S		M		L		XL		Field size	Max. Energy (MeV)	Dose rate (rad/h)	Max. Range (Si) (cm)
	G	L	G	L	G	L	G	L	G	L				
CERN Co60	Y	N	Y	N	Y	N	Y	N	Y	N	several meters	~2	N/A	~10
ONERA	Y	N	Y	N	Y	N	Y	N	Y	N	several meters	~2	N/A	~10
UCL Co60	Y	N	Y	N	Y	N	Y	N	Y	N	several meters	~2	36	~10
IES X-ray	N	Y	N	N	N	N	N	N	N	N	20cm x 20cm	~0.36	56K	~7.5

2.2.4.3. TID Radiation Hardness Assurance

The objective of RHA activities regarding TID is to avoid dose induced failures. Regarding external environments modeling, SEPs have an important contribution to TID effects and are stochastic in nature not allowing analytical calculations. Thus statistical average models with yearly fluences are provided with different confidence levels.

The internal environment definition is used for particle transport calculation. Transport calculation is an important step in TID as it defines the dose at the sensitive regions of a digital system. The output of a transport calculation is a dose curve that plots the dose in the sensitive region per Aluminum shielding thickness. Two different approaches can be used for transport calculation. The most precise approach is to use Monte-carlo simulations such as CREME-MC [WMRS10] for calculating the interactions of each particle for the different materials and shielding geometries. However, this approach can be very time consuming for complex spacecraft, aircraft etc. Thus, a first order analysis can be performed by using tabulated attenuation data from simple geometric shields. This approach is called sector based calculation or ray tracing. In this approach rays are traced from a target to the outside geometric model (solid sphere, sphere shell, finite slab and semi-finite slab) and then a numeric solid angles integration around the target point is performed. The total mass thickness encountered by the ray is used to determine the dose in the target position [STEP86].

TID testing data provides parametric degradation versus dose for a specific component. During the system and component evaluation, the lot-to-lot variation and uncertainties in the environment modeling imposes statistical requirements for performing TID Worst Case Analysis (WCA). Those statistical requirements include Probability of Survival (PS) and probability of degradation that are calculated by the average of the probability distribution plus a one sided tolerance limit. The mitigations approaches at system-level can be performed by replacing sensitive components or increasing shielding thickness according to the dose curve obtained in the transport calculation [MANG18].

2.2.5. Commercial-of-the-shelf vs hardened components

Commercial off-the-shelf (COTS) grade components are designed for commercial applications in which its vendor or manufacturer only specifies its performance, configuration and reliability without performing any testing after its delivery. A variant of this grade is the COTS+ components that include additional testing for making random failure rate assumptions and excluding early failing parts. An example of COTS+ components are the Automotive Electronics Council (AEC) -certified automotive parts [AUTO14]. However, manufacturing variability such as wafer-to-wafer variation and lot-to-lot increase the risk of space missions using COTS components. In addition, screening of components cannot always reduce the risk to acceptable levels [BAUM18].

Qualified components can be divided into Enhanced Intermediate Grades (EIG) and Space Grades. EIG components include Enhanced Products (EP), Qualified Manufacturers List (QML) Class Q, and Space EP grades. EIG components, as the name implies, offer a higher quality and reliability than COTS components that can be achieved by using different materials for packages and bond wires, can be characterized by radiation testing and its failure rate can be predicted by RHA methodologies. Space grade components include QLM Class V and QLM Class-V-Radiation Hardness Assurance (QLMV-RHA) grades. Space grades components offer additional reliability by performing assembly and wafer lot traceability, screening of components and burning tests [TEXA18]. An image summarizing different product grades is presented in Figure 2-38 [BAUM14].

	COTS / COTS+		Enhanced Intermediate Grades			Space grade	
	Commercial	AEC-Q100	EP	QMLQ	Space EP	QML-V	QMLV-RHA
Packaging	PLASTIC	PLASTIC	PLASTIC	CERAMIC	PLASTIC	CERAMIC	CERAMIC
Single Controlled Baseline	NO	NO	YES	YES	YES	YES	YES
Bond wires	Au or Cu	Au or Cu	Au	Al	Au	Al	Al
Pure Sn Used	YES	YES	NO	NO	NO	NO	NO
Burn-in Performed	NO	NO	NO	NO	NO	YES	YES
Radiation Tested	NO	NO	NO	NO	YES	YES	YES
Radiation Assured	NO	NO	NO	NO	YES	NO	YES
Temperature Range	-40 to 85°C	-40 to 125°C (only grade 1)	-55 to 125°C (majority)	-55 to 125°C	-55 to 125°C (majority)	-55 to 125°C	-55 to 125°C
100% 3 Temp Test	NO	NO	NO	YES	25, 125°C	YES	YES
Extra Qual/Process Monitors	NO	YES	YES	YES	YES	YES	YES
Life Test per lot	NO	NO	NO	NO	NO	YES	YES

Figure 2-38. Quality and reliability enhancements, testing and assurance of different product grades [BAUM14].

In addition to material enhancement and single controlled baselines lots, components can also be hardened during IC manufacturing by using Radiation Hardened by Design (RHBD) techniques. However, in terms of performance rad-hard components are always at least two generations behind state-of-the-art components, and future space missions will require higher computation power.

2.3. AGING MECHANISMS IN CMOS TECHNOLOGIES

Various wear-out mechanisms can lead to failures during the lifetime of a component. Those wear-out mechanisms are called aging mechanisms or aging effects. As they affect the intrinsic parameters of the circuits such as threshold voltage and leakage current, they can also change the radiation sensitivity of those components. Thus, it is important to understand those mechanisms when characterizing digital systems for long missions. The effect of aging mechanisms on the sensitivity of components to radiation effects or vice-versa is called coupled-effects. Thus, the main aging mechanisms and coupled effects that are the major concern for CMOS digital technologies will be presented.

This section is organized as follows: the first four subsections will describe the parametric degradation and test methodologies of Bias Temperature Instability, Time Dependent Dielectric Breakdown, Hot carrier Injection and Electromigration, finally coupled effects and their test methodologies will be introduced.

2.3.1. Bias Temperature Instability

2.3.1.1. Parametric degradation of CMOS gate dielectrics

Bias Temperature instability (BTI) concerns the degradation of transistor parameters due to electric field stress over the gate dielectric and high temperature stress. As a negative bias is applied to PMOS transistors and a positive bias is applied in NMOS transistor, BTI is called Negative BTI (NBTI) in PMOS transistors and Positive BTI (PBTI) and NMOS transistors [SCBA03]. NBTI is much more expressive in PMOS devices than NMOS. It is commonly associated to the dissociation of Si-H bonds and hydrogen diffusion, as illustrated in Figure 2-39 [WRKV07].

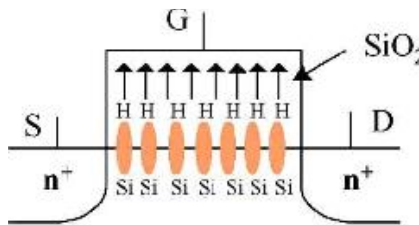


Figure 2-39. Dissociation and diffusion of hydrogen bonds [WRKV07].

Thus plenty of reaction-diffusion models have been proposed[SCBA03][ALMA05][WRKV07][CCLS03][KHHA10].

The threshold voltages and drain current degradation follow a power-law dependence. Different threshold voltage [WRKV07] and mobility degradation [KHHA10] models have been proposed.

When the voltage applied to the transistor gate is removed the transistor parameters can be recovered by means of capturing of the mobile species, and the diffusion of the mobile species back to the interface [CKRM04]. Different recovering models have been proposed in the literature[WRKV07][KCCR12][KRMK10]. According to some simulations, it was found that the NBTI degradation saturates. The NBTI degradation can be limited by the number of SiH sites or the reflection of diffusing species in a different interface, such as the nitride/polysilicon interface in a gate stack [CKRM04].

2.3.1.2. Test methodologies

At transistor level, the industry standard methodology to characterize the BTI effect is to perform on-the-fly measurements [DBHP04]. Other conventional methodology is to perform Charging Pumping (CP) measurements and apply constant stress voltage to the gate and then stop it to perform the current-voltage measurements [HINH04]. Other methodologies such as and Ultrafast Pulse (UFP) measurements can also be applied [WLCL13][YLSA05] [ZLZK10].

BTI characterization at component-level usually is performed respecting the JEDECs standards regarding the application of High Temperature Operation Life (HTOL) methodology, where a component is subjected to bias stress, temperature stress and frequency stress [JEDE05][JEDE04]. It can be performed by implementing health monitors such as flexible Ring Oscillators on FPGA or by measuring the supply voltage quiescent current (IDDQ) or the supply voltage transient current (IDDT) peak [ZHKE15A][ZHKE15B][ABKB14]. At system-level, where the only information about the degradation is the system functionality, it is extremely complex to identify which aging mechanism caused the system functionality failure [GHVG11]. One example is the characterization of the intermittent faults of a 65nm FPGA-based embedded system [ZHKE16] where the HTOL stress methodology was employed.

2.3.2. Time-Dependent-Dielectric-Breakdown

2.3.2.1. Dielectric rupture of CMOS dielectric

Time Dependent Dielectric Breakdown (TDDDB), as the name implies, is the rupture of any dielectric of an integrated circuit exposed to electric field stress. When it happens in the Front-end-of-line (FEOL) e.g. between the gate and source or drain it is called Gate TDDDB (GTDDDB), in the Back-end-of-Line (BEOL), such as parallel metal interconnections, is called BEOL TDDDB (BTDDDB), and finally it can also happen in the middle-of-line (MEOL), like between the gate and contacts, when it happens it is called MEOL TDDDB (MTDDDB), as presented in Figure 2-40 [WSLL15].

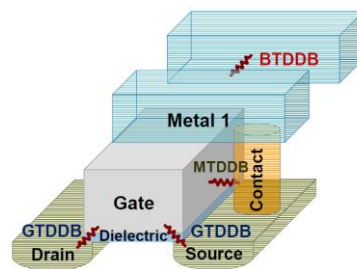


Figure 2-40. Different types of TDDDB in an integrated circuit [WSLL15].

Electric field stress generates dielectric traps that become close enough to generate a tunneling path, this way the Stress Induced Leakage Current (SILC) increases according to the density of traps until a complete path is formed, and then a dielectric breakdown occurs [NISF86]. Many electric field-dependent time-to-breakdown models were developed [PKIA02][HAOM05][CBCM06][CRL10]. At component-level, TDDDB effect may be observed by step-like current degradation.

2.3.2.2. Test methodologies

At transistor level, the conventional methodology to test the GTDDDB or MTDDDB effect is to perform stepped voltage ramp test, where a constant voltage is applied to the gate during a specific period of time and

after that, the voltage is incremented by a defined value [PKIA02][FNYY17]. For characterizing BTDD, comb-serpentine test structures are commonly designed with Metal lines to generate the parallel interconnections where the dielectric breakdown occurs [HAOM05][HAMC07][FLRP08]. At component-level, TDD can also be identified by measuring Ring Oscillator (RO) timing degradation or the IDDQ current [KPHK13][KDRM02], and following the HTOL methodologies from the JEDEC standards. However, as previously mentioned, other effects such as BTI can suppress the effect of the TDD [ZHKE15A].

At system-level, it is even more complex to discriminate TDD from other aging mechanisms. The ICs within the systems are implemented in different technologies sizes having different number of metal layers making a fault propagation analysis extremely complex [BERN15][GHVG11][ZHKE16]. An example is the aging characterization, that includes TDD, of 12nm/28nm MPSoC systems by measuring IDDQ, IDDT and health monitor timing degradations [ZHKE15B].

2.3.3. Hot Carrier Injection

2.3.3.1. Local degradation in CMOS devices

Hot Carrier Injection (HCI) is the local degradation of transistor parameters due to the electric field stress. Differently from BTI, it is more expressive in NMOS transistors than PMOS transistors. In short channel NMOS devices (technology size lower than 250nm) electrons achieve a high velocity due to high electric field close to the drain, and consequently inject carriers in the dielectric interface generating traps [RACN03]. As BTI, the HCI can be modeled by reaction-diffusion models [DFTF18][YTSI99][MMMI13], but the main differences are that the degradation effect occurs in the strong inversion mode of the transistors and the recovering of the HCI degradation is negligible, the difference between BTI and HCI is illustrated in Figure 2-41 [WRKV07].

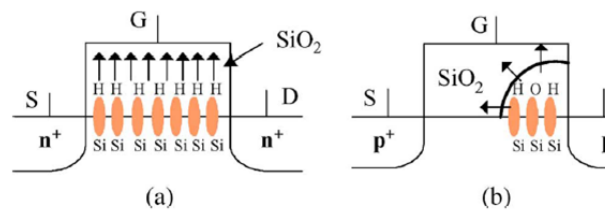


Figure 2-41. Comparison between the reaction-diffusion processes in BTI and HCI [WRKV07].

2.3.3.2. Test methodologies

At transistor level, the standard methodology to analyze the HCI effect is to perform DC stress and I-V measurements, this way it is possible to measure the drain current degradation and the threshold voltage degradation [WRKV07][ZHEN14][GLLW06]. However, the results are related to both the BTI and HCI effects, thus is not straightforward to distinguish between those distinct mechanisms during the measurements. One possible solution is to take into account the fact that the HCI recovering is negligible [WRKV07], this way after some BTI recovering, it would be possible to extract only the permanent effect of the HCI.

At component-level, different from BTI and TDD, the standard methodology to characterize the HCI mechanism is not in the HTOL methodologies defined in the JEDEC standards, because HTOL implies high temperature stress and HCI is more sensitive to low temperatures. Another difference is that TDD and BTI

are more sensitive to the voltage bias while HCI is more sensitive to the operational frequency [BERN15][ABKB14]. One possible methodology to characterize HCI degradation at component-level is by using health monitors such as flexible Ring Oscillators. An example of this methodology is the characterization of a 45nm FPGA, where Frequency Configurable Ring Oscillators were designed to be sensitive to HCI [ABKB14].

As HCI is a localized degradation at transistor level, it is pretty complex to discriminate from BTI that reproduces the same degradation. The negligible recovery of HCI could be used to discriminate it from NTBI, however components within a system have different sensitivities for the different mechanisms. Therefore, if one component has a lower NBTI recovery than the other, it could be erroneously measured as a HCI.

2.3.4. Electromigration

2.3.4.1. Parametric degradation

Electromigration (EM) is a mass transport mechanism in digital system interconnections where electrons transfer momentum to atoms. This mechanism results in the formation of voids in interconnection anodes due to metal depletion and extrusion in cathodes due to metal accumulation. At a higher level, open-circuits due to void in interconnections and shorts due to extrusion lead performance degradation and malfunctioning. An SEM cross-section image of a void formation in a cathode of a copper interconnection is presented in Figure 2-42 [ZWLM13].

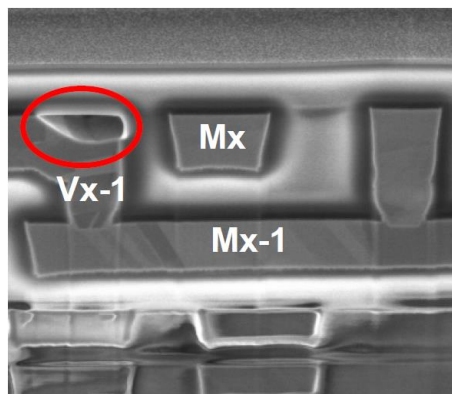


Figure 2-42. SEM cross-section image showing void formation at the cathode end [ZWLM13].

2.3.4.2. Test methodologies

The conventional EM test methodology is to design different metal lines including test line and extrusion or void monitors [ZWLM13]. Failures are measured by resistance shifts in the test metal lines after an extrusion or void formation. At component-level EM-induced failures can be discriminated from other aging mechanisms such as TDDB, NBTI and HCI by performing accelerated aging tests at low voltage and applying high frequency and high temperature stress [ABKB14][BERN15].

2.3.5. Coupled effects

2.3.5.1. Parametric degradation

Reliability fault and degradation mechanisms can have an influence in other mechanisms. Those mechanisms can be from the same type such as effects of radiation induced-degradation in radiation SEE sensitivity, or from different types such as effects of radiation-induced degradation on aging lifetime. Those

coupled effects can be positive [MPDL13A] or negative [MPDL13B] depending on the mechanism, device operation, digital structure in which it occurs and many other causes. An example of negative NBTI effect on SEE sensitivity is presented in Figure 2-43 [MPDL13B].

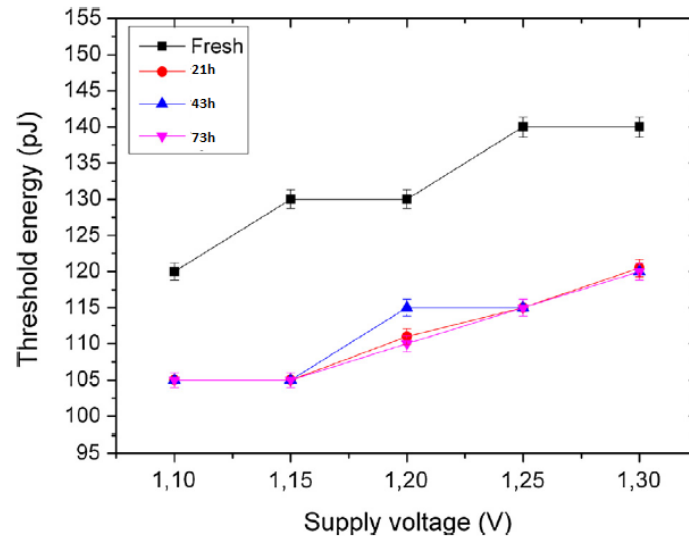


Figure 2-43. NBTI negative influence on SEE Laser energy sensitivity [MPDL13b].

2.3.5.2. Test methodologies

Currently, there is no standard test methodology for detecting coupled effects, therefore it will depend on which aging or radiation effect the tester wants to observe in the sensitivity of another radiation or aging effect. For analyzing aging effects such as NBTI on SEE sensitivity, an interesting approach is to apply NBTI stress in a device and perform laser testing on different stages of the lifetime where it is possible to observe the SEE sensitivity evolution along the time [MPLD13].

In order to observe the effect of TID in TDDB lifetime, one common approach is to irradiate devices and then subject them to ALT voltage stress test, where it is possible to see that the time-to-breakdown Weibull distributions are reduced according to the accumulated dose [SVRC02].

Considering the complexity of all the possible interactions of the different aging and radiation mechanisms, the current standard approach in the industry is to not consider such coupling, and to consider that the effects are independent. Possible coupled effects are usually covered by introducing additional safety margins in the system's reliability evaluation.

2.4. Conclusions

In the first section of this chapter, we presented the technologies and components that will be investigated in this work. The second section presented the radiation environments, particle component interaction and their effects on digital systems as well as the current component-level and emerging system-level methodologies for characterizing those effects. Finally, in the third section, the aging mechanisms, including their test methodologies, which also affect the reliability of digital systems and can influence radiation sensitivity, were briefly introduced.

In the next chapter, we will review the systems under test and the associated instrumentation that were developed to investigate those effects at the system-on-module level.

3. CASE STUDY DEVELOPMENT AND INSTRUMENTATION

In this chapter, the hardware systems and embedded software that were used and developed as case study for the RHA bridge methodology development will be presented. First, technical information of the components embedded on the systems will be explained. Second, implementation details of the applications embedded on the systems will be presented. Third, testability and data analysis issues on system-level test will be discussed. Fourth and fifth, implementation details of the software and hardware instrumentations will be described, respectively. Finally, technical details of carrier boards designed and used for the experiments will be presented.

3.1. Target System-On-Modules

Two small-form factor (56x54 mm) commercial industrial SoC-based SoM generations were used as hardware system case studies. Those SoMs can represent a simple digital embedded system or subsystem. The older generation is a Mercury ZX5 SoM based on a Xilinx7000 SoC and the newer generation is a Mercury XU5 SoM based on a Xilinx ZynqUltrascale+ SoC, both from Enclustra company. The ZX5 and XU5 SoM simplified block diagrams are illustrated in Figure 3-1.

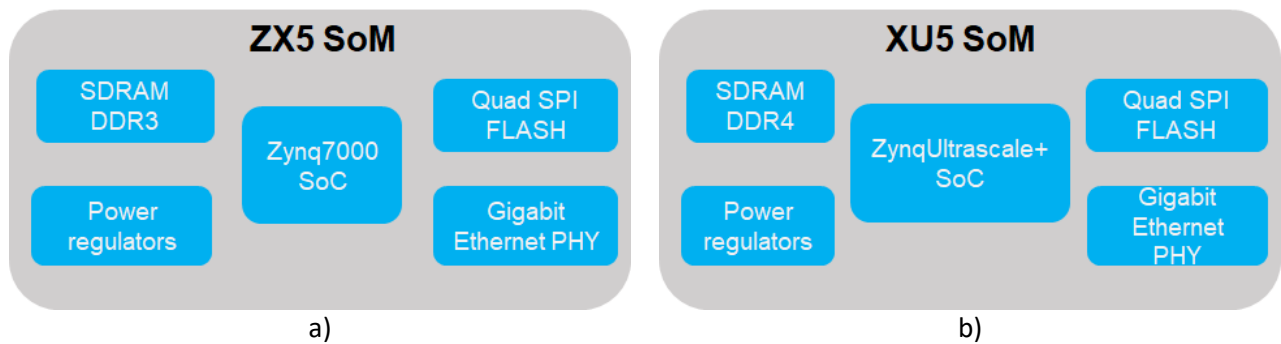


Figure 3-1. SoM generations. a) ZX5 SoM based on Zynq7000 SoC b) XU5 SoM based on Zynq Ultrascale+ SoC

In addition to the small-form factor ZX5 and XU5 SoMs, a Small Outline Dual In-line Memory Module (SO-DIMM) SoM was also used, the Mars XU3 module, which is similar to the XU5 with small differences in the components. The pictures of the different SoMs are presented in Figure 3-2.

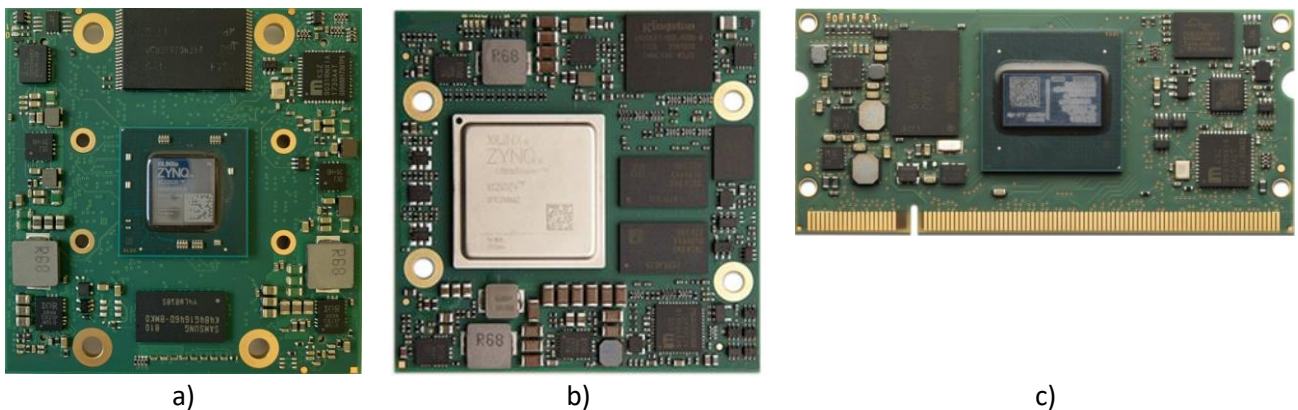


Figure 3-2. SoM pictures. a) small-factor form ZX5 SoM SoC. b) small factor form XU5 SoM SoC. c) SO-DIMM XU3 SoM

The features of each SoMs are presented in Table 3-1. Technical details of the main components of the different SoMs will be presented in the next sub-subsections.

Table 3-1. Main features of SOM generations used

Features	Mercury ZX5	Mercury XU5	Mars XU3
Dimensions	56 × 54 mm		67.6 × 30 mm
SoC	BareDie Zynq7000 SoC	Metal lid ZynqUltrascale+ SoC	BareDie ZynqUltrascale+ SoC
PS DDR	1GB DDR SDRAM	2GB DDR4 SDRAM	
PL DDR	-	512MB DDR4	-
Low capacity Flash	NAND Flash	16GB eMMC Flash	
High capacity Flash	64MB NOR Flash		

3.1.1. System-on-chips

3.1.1.1. Zynq7000 SoC resources

The ZX5 module contains the XC7Z030-1SBG485I Zynq7000 (Z7) Programmable SoC. The block diagram of the Zynq7000 SoC is presented in Figure 3-3 [XILI18A].

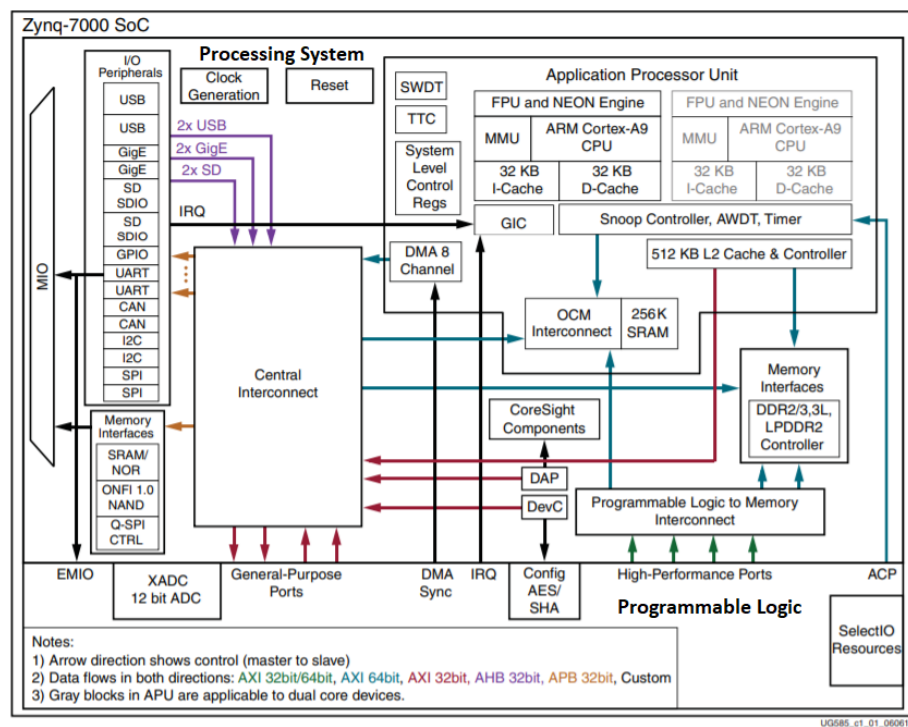


Figure 3-3. Zynq7000 SoC block diagram [Xili18]

This programmable SoC contains a Processing System (PS) and a Programmable Logic (PL) that are interconnected by using an AXI bus with 32-bit and 64-bit widths. Inside the PS, there is a Central Interconnect that intermediates the communications between the APU, Memory interfaces (e.g. DDR3 and NAND Flash) and IO peripherals by using different AMBA bus protocols (AXI, AHB and APB) depending on the speed and bandwidth requirements for the communications. The external inputs and outputs are configured by using a Multiplex Input Output (MIO). The APU contains a dual core ARM-A9 processor, 32Kb Level 1 (L1) caches, 512KB Level 2 (L2) cache, a 256KB On-chip Memory (OCM), an 8 channel Direct Access Memory (DMA) and System-level Control Registers as well as other resources.

The PL is mainly composed of CLB, BRAM and DSP resources. The CLBs are composed by 6-input LUTs, registers and cascaded adders. The BRAM blocks have a capacity of 36KB, dual port, programmable FIFO logic, and built-in Hamming error correction circuitry. The DSPs supports two's complement multiplication with 25-bit and 18-bit operators and a multiply-accumulator high-resolution of 48-bit. The clock management has global and local buffers, frequency synthesizers, phase shifting and Phase-Locked Loop (PLL) and Mixed-mode Clock management (MMCM) clock sources. The high range IO pins can be configured from 1.2V to 3.3V and the high-speed IOs can be configure from 1.2V to 1.8V.

The sizes and frequencies of the Z7 PS and PL resources are summarized in the Table 3-2 and Table 3-3, respectively.

Table 3-2. Summary of Zynq7000 PS resource sizes

PS resource	Z7030
Processor core	Dual core ARM Cortex A9
CPU maximum frequency	1GHz
OCM size	256KB
L1Cache size	32KB
L2Cache size	512KB

Table 3-3. Summary of Zynq7000 PL resources

PL resource	Z7030
Programmable Logic Cells	125K
Look-Up Tables (LUTs)	78 600
Flip-Flops	157 200
Block RAM (#36 Kb Blocks)	9.3Mb (265)
DSP Slices (18x25 MACCs)	400
MMCMs	5
PLLs	5
Maximum global buffer frequency	625MHz
Configuration bits	47 839 328

3.1.1.2. ZynqUltrascale+ SoC resources

The XU5 and XU3 models contains the XCZU2EG-1SFVC784I and XCZU3EG-2SBVA484I ZynqUltrascale+ (ZU+) Programmable SoCs, respectively. Those SoCs have exactly the same PS with different amount of PL resources. A generic ZynqUltrascale+ SoC block diagram is presented in Figure 3-4 [XILI19].

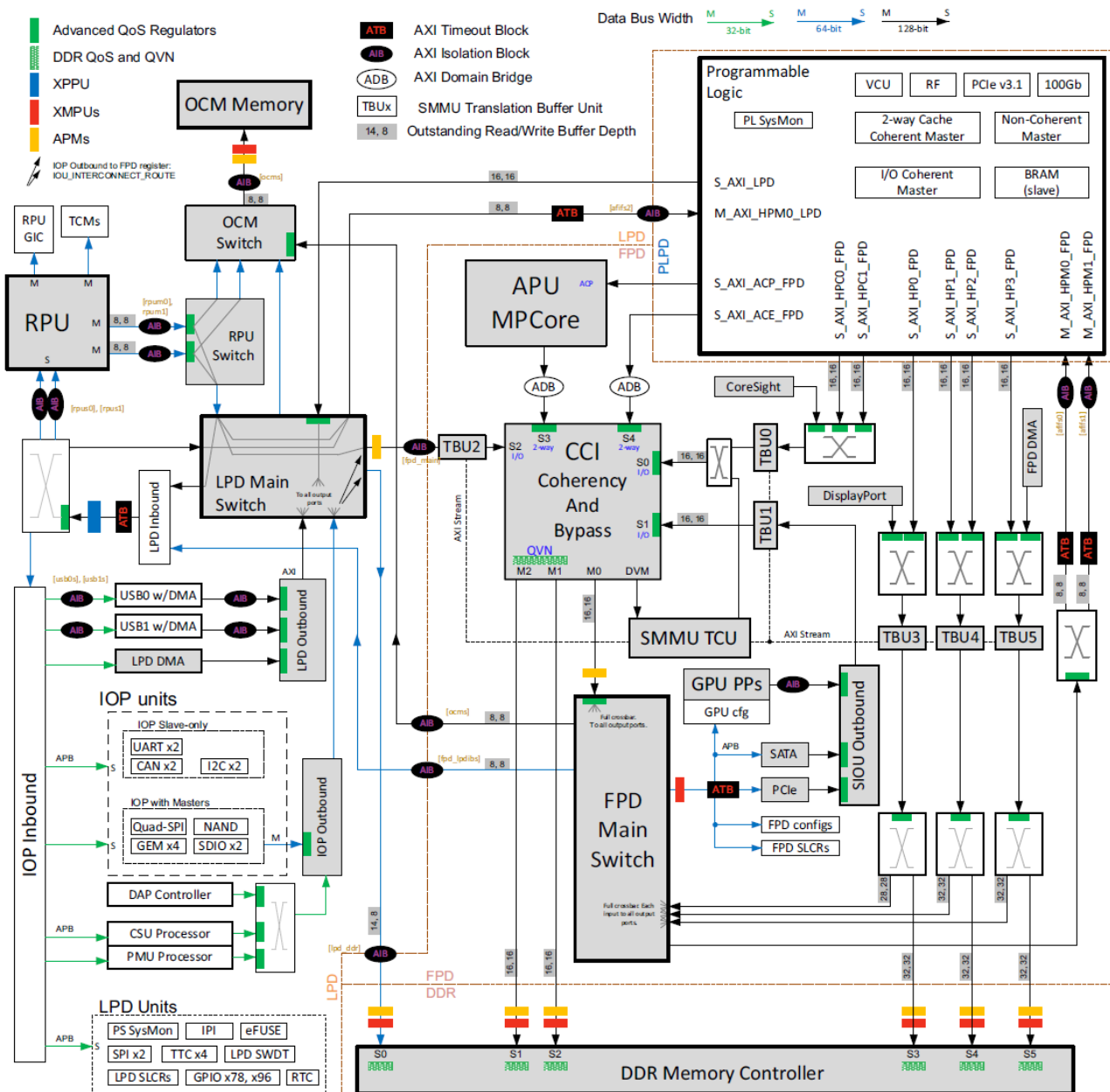


Figure 3-4. ZynqUltrascale+ SoC block diagram. [Xili19a]

This Programmable SoC has a Processing System (PS) and a Programmable Logic (PL) interconnected by Full-Power Domain (FPD) and Low-power domain (LPD) switches implemented by AXI protocols with 32 to 128 bit widths. The PS communications between APU, RPU, GPU, memory controllers, OCM and IO peripherals are intermediated by the 1MB Cache-Coherent Interconnect (CCI) cache. The APU has quad-core ARM-53 processors and 32 KB L1 caches. The RPU contains dual-core Cortex-R5 processors a 256KB TCM. Both RPU and APU can communicate to the 256KB OCM and the DDR memory controller by using different

address spaces. The GPU contains dual-core ARM Mali-400 Pixel Processors (PP) and one Geometry Processor (GP) with a shared 64KB L2 cache controller.

The ZynqUltrascale+ PL possesses mainly CLB, BRAM, Ultra RAM and DSP columns among other resources. The CLB contains 6-input LUTs, flip-flops and cascade adders. The BRAMs have 36Kb capacity and true dual-port capability and embedded FIFOs and error correction code. Whereas the Ultra RAM has 288Kb dual port capability. The DSP blocks also multiply 27 and 18-bit operands and have 48-bit multiply-accumulate resolution. Finally, the high range IOs can be configured from 1.0V to 3.3V and the high-speed IOs can be configured from 1.0V to 1.8V.

The parameters of the ZU+ PS and PL resources are summarized in the Table 3-4 and Table 3-5, respectively.

Table 3-4. Summary PS resources that are present on both ZynqUltrascale+ SoCs

PS resource	ZU2EG/ ZU3EG
RPU Processor cores	Dual-core ARM Cortex-R5
APU Processor cores	Quad-core ARM Cortex-A53
RPU maximum frequency	600MHz
APU maximum frequency	1.5GHZ
OCM size	256KB
L1Cache size	32KB
L2Cache size	1MB

Table 3-5. Summary PL resources of the two versions of the ZynqUltrascale+ SoC

PL resource	ZU2EG	ZU3EG
Programmable Logic Cells	103 320	154 350
Look-Up Tables (LUTs)	94 464	70 560
Flip-Flops	47 232	141 120
Block RAM (#36 Kb Blocks)	150 (5,3Mb)	216 (7,6 Mb)
UltraRAM (#36 Kb Blocks)	0	
DSP Slices (18x25 MACCs)	240	360
MMCMs	3	
PLLs	3	
Maximum global buffer frequency	667Hz	
Configuration bits	30 876 800	

The XC7Z030-1SBG485I Zynq7000 [XILI14] and XCZU2EG-1SFVC784I ZynqUltrascale+ [XILI20] package dimensions are illustrated in Figure 3-5 .

The portion of the configuration bits used in the implemented design are defined as essential bits and the portion of essential bits that generate an error in the application output are defined as critical bits.

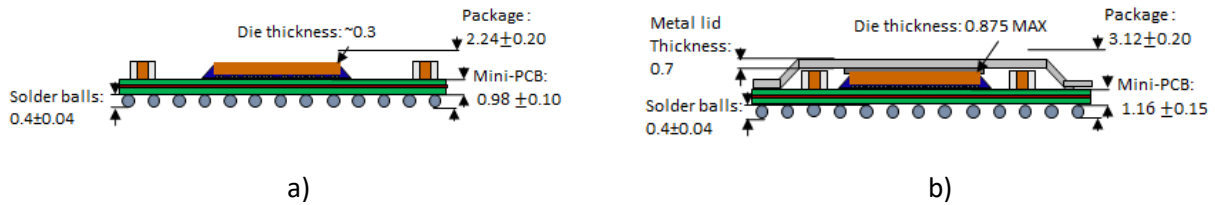


Figure 3-5. SoC package dimensions in millimeters. a) Zynq7000 bare die FBGA package b) ZynqUltrascale+ FBGA metal-lid

The XCZU3EG-2SBVA484I ZynqUltrascale+ package have the same thickness dimensions of the XCZU2EG-1SFVC784I package but without metal lid.

3.1.2. DDR SDRAM memories

The main features of the SDRAM DDRs embedded on the modules are presented in Table 3-6.

Table 3-6. DDR features of the ZX5, XU5 and XU3 SoMs

DDR Features	ZX5	XU5/XU3
DDR version	DDR3	DDR4
Manufacturer	Samsung	Micron
Part number	K4B4G1646D-BMK0	MT40A256M16GE-083E-IT-B
Supply voltage (V)	1.5 ± 0.075	1.2 ± 0.060
Density	4Gb	
Maximum transfer rate (Mb/s/pin)	2133	3200

The ZX5 module embeds one DDR3 die on the top part of the PCB board and another die on the bottom part. The XU5 module has two PS DDR4 dies on the top part, two PS DDR4 dies on the bottom part, and one PL DDR4 die on the bottom part as well. Finally, the XU3 module has one PS DDR4 die on top part and another one in the bottom part.

Both the DDR3 and DD4 chips were encapsulated in Flipchip Ball-Grid-Array (FBGA) packages. The dimensions of each package are summarized in Figure 3-6.

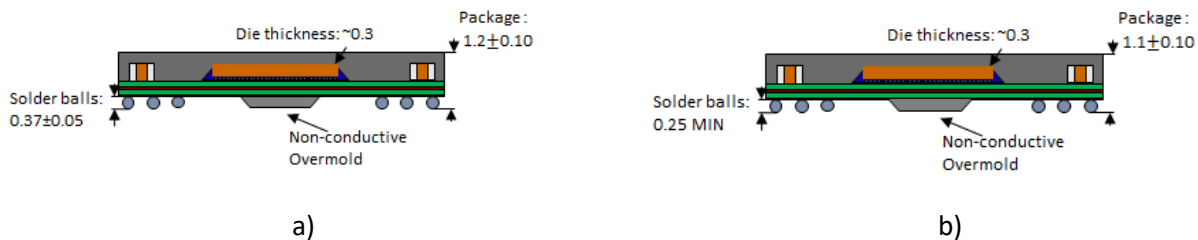


Figure 3-6. DDR package dimensions in millimeters. a) DDR3 Samsung package dimensions b) DDR4 Micron package dimensions

As it can be seen in the picture, both DDR3 and DDR4 have similar dimensions. They are covered by plastic material such as Epoxy Novolac ($C_{11}H_{19}O_6$).

3.1.3. Flash memories

Technical details of the Flash memories present on the ZX5, XU5 and XU3 modules are described in Table 3-7 .

Table 3-7. Features of Flash memories embedded on the modules

Modules	ZX5/XU5/XU3	ZX5	XU5/XU3
Flash type	NOR	NAND	eMMC
Manufacturer	Spansion	Micron	Kingston
Technology	MLC	SLC	-
Technology size	65nm	73nm	-
Part number	S25FL512S	MT29F4G08ABADAWP	EMMC16G-W525-X01U
Supply voltage (V)	3.3±0.3	3.3±0.3	-
Data retention	20 years	10 years	-
Density	512 Mb	4Gb	128Gb
Interface	QSPI		-
Page size (bytes)	512	2 112	-
Sector/Block Size (Kbytes)	128	132	-
Number of sectors/Blocks	512	2 048	-
Number of planes	-	2	-
Maximum transfer data rate (Mb/s)	80	40	-

All the modules embed a NOR low capacity Flash. The ZX5 module also embeds a high capacity NAND Flash [MICR06] and the ZynqUltrascale+ modules embed an embedded Multimedia Card (eMMC) Flash. The package dimensions of the Quad serial peripheral interface (QSPI) NOR [CYPR19] and NAND flashes are illustrated in Figure 3-7.

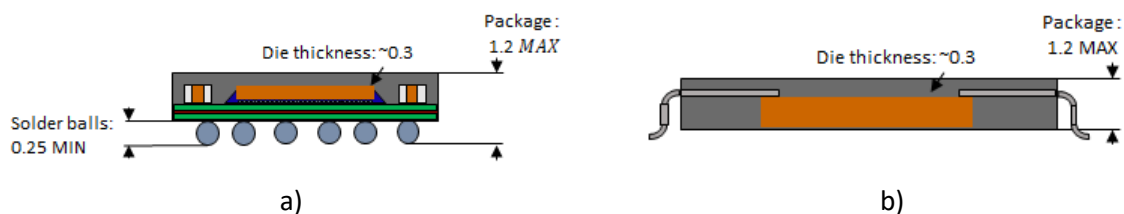


Figure 3-7. Flash package dimensions in millimeters. a) BGA QSPI NOR Flash package. b) TSOP NAND Flash package

The NOR Flash comes in a Fine Pitch Ball Grid Array (FBGA) package without overmold having maximum package thickness of 1.2mm.

3.1.4. DC-DC converters

As the input voltage of the ZX5 and XU5 modules is 12V and the components have different power supply voltage levels, different DCDC converters are embedded on the module. Thus, most of the DCDC converters are PWM buck converters. Some power regulators identified on the ZX5 and XU5 are presented in Table 3-8.

Table 3-8. DCDC converters features

Module	ZX5/XU5	XU5	
Part number	IR3899	S-1200	TPS54494
Manufacturer	IOR	Ablic	Texas Instruments
Type	PWM Buck	LDO	Dual channel PWM Buck
Technology	HEXFET	CMOS	N-MOSFET
Input range (V)	1-21	2-10	4.5-18
Output voltage (V)	3.3V	5	0.9 1.8
Output current (A)	9	0.15	3.2 2
Switching frequency (MHz)	1.2 MAX	-	0.7

The IR3899 PWM buck converter is used to convert 12V into 3.3V that is used for supplying other converters and SoM components directly such as FPGA IOs, having a rated current of 9A. The TPS5449 dual channel converter is supplied by the IR3899 converter and provides supply for low voltage components of the XU5 module such as the SoC. Both IR3899 and TPS5449 comes in Power Quad Flat No-Lead (PQFN) package as illustrated in Figure 3-8.

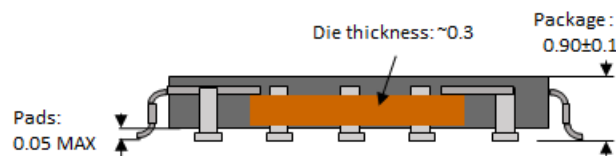


Figure 3-8. PQFN package dimensions in millimeters used on both IOR3899 and TSP54494 converters

3.2. Development tools

3.2.1. SoC FPGA design tool

All the SoC FPGA design in this work was performed by using the Xilinx Vivado Design Suite versions 2017.4, 2018.2 and 2018.3 [XILI15A]. This tool is responsible for integrating IPs for configuring the PS of the SoC such as the internal frequencies of the different processing units, the FPGA IO voltages, the peripheral (Flash) frequencies and IO pinning, the DDR parameters, among other functionalities. Regarding the PL side, this tool is used for designing, simulating, debugging, and analyzing FPGA implementations among other features. The Vivado Design flow is summarized in Figure 3-9.

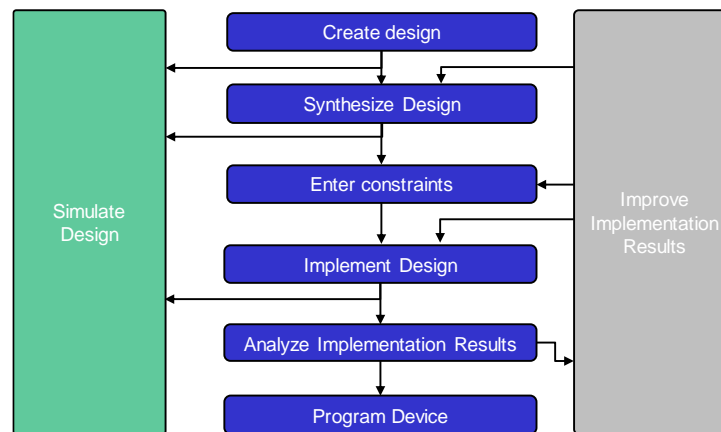


Figure 3-9. Simplified Vivado design flow

First, the design is specified by using Register Transfer Level (RTL) diagrams or block diagrams, and then the design is created by integrating Intellectual Property (IP) cores and describing the hardware design by using the Very High Speed Integrated Circuit Hardware Description (VHDL) language. After synthesizing the design, the netlist is generated containing all the required cells (CLBs, BRAMs, CLBs...) and their connections (nets). Then the user enters the constraints such as area, power and performance constraints. Thereafter, in the implementation phase, the cells are placed on the available resources and routed. Finally, the implementation results are analyzed and if they meet the specifications the bitstream is generated and the device is programmed. If the specifications are not meet, an iterative process starts by simulating the design in different phases and improving the design.

3.2.2. Software Development tools

All the software developments were performed by using the Xilinx Software Development Kit (SDK) versions 2017.4, 2018.2 and 2018.3 [XILI15B]. This software is a package that contains different tools for building software such as compilers, linkers and assemblers, and tools for debugging such as debuggers, flash writers and simulators. The SDK design flow and software stack for Xilinx SoCs are illustrated in Figure 3-10 [XILI17A]. The steps of the development flow and software stack used are outlined in red.

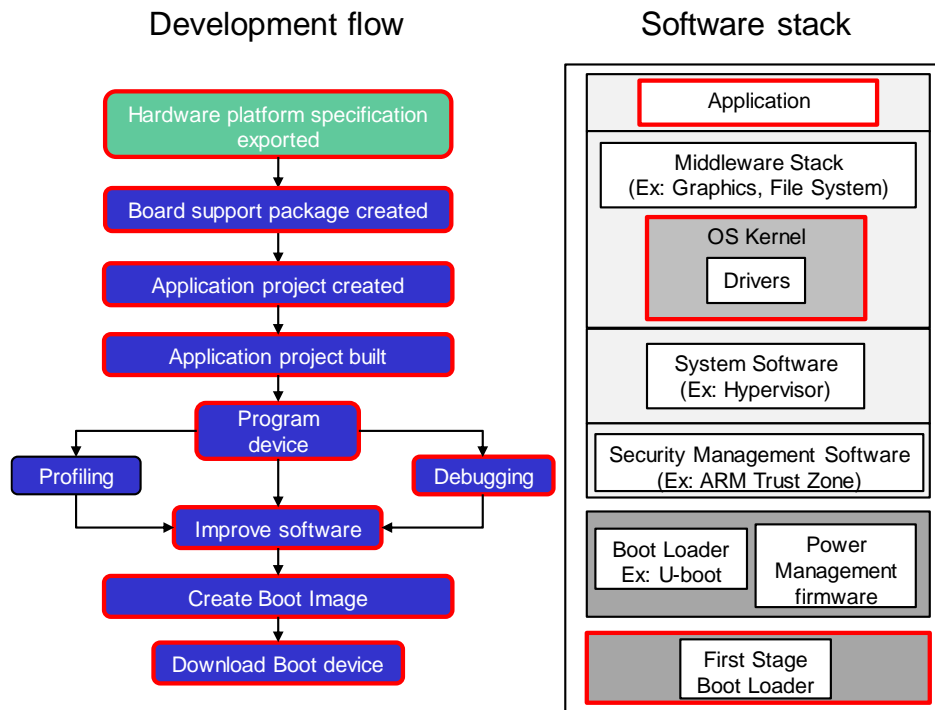


Figure 3-10. Software development flow and software stack on Xilinx SDK. Based on [XIL17A]. The development flow and software stacks used are outlined in red

In the design flow, first the hardware platform specification is exported from Vivado including the SoC device, the peripherals activated (Flash, DDR, eMMC...) and IP-cores present in the design. Then, the Board Support Package (BSP) is created for a given target hardware (APU CPU 3, RPU CPU0), Operating System (OS) such as baremetal and FreeRTOS, and programming language (C or C++). The BSP contains all the drivers for communicating the application software with hardware peripherals (Flash, DDR and IP-cores).

Afterwards, the application project is created. The software stack used for the developments is composed by an application layer implemented on either baremetal or FreeRTOS. Implementing an application in bare-metal means that the application runs directly on the target hardware instead of having an OS layer and application layer as occurs in FreeRTOS. The multi-core developments were performed using the Asymmetric Multiprocessing (AMP) software design paradigm.

After the application project be built, the FPGA is programmed with the bitstream, and Executable and Linkable Format (ELF) files are downloaded on the required cores by using the JTAG (Joint Test Action Group) protocol [TOSH91]. The functionality of the software is verified by debugging. If the specifications are meet, the First Stage Boot Loader (FSBL) application is created and compiled, and then the boot image is created including the FBSL ELF file, the FPGA bitstream and the application ELF files for each core. Finally, the Flash memory is programmed with the boot image. The FSBL code stored in the boot image is responsible for programming the FPGA, initializing the memories and loading the applications in the respective cores.

3.3. Embedded Application

In this section, the different embedded applications developed for radiation test will be presented. First, the implementations details of a control loop application intended for space and avionics will be provided. Then, RAM and Flash memory benchmarks algorithms will be presented. Finally, a benchmark developed for measuring TID and aging parametric degradation will be described.

3.3.1. SEE Space and Aviation application

SoCs are commonly used for implementing sensor processing for avionic and space applications. Thus, a scalable control loop application was designed aiming to be representative of simple digital systems operating in those environments. The control loop block diagram is presented in Figure 3-11.

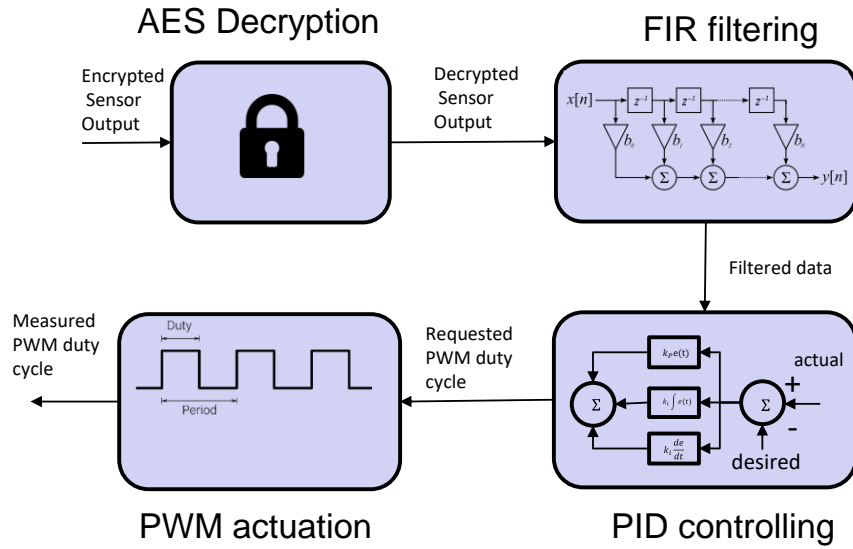


Figure 3-11. Control-loop application block diagram

The loop consists of a sequence of decryption, filtering, controlling and actuation. Encrypted sensor output is decrypted by using the Advanced Encryption Standard (AES) and a key of 16 bytes. Afterwards, decrypted data have to be filtered by using a low-pass Finite-Impute-Response Filter (FIR). Then, error values from filtered data are used to compute Proportional-Integral-Derivative (PID). The error calculation is described by:

$$e(n) = d_o - c_o(n) \quad 3-1$$

where $e(n)$ is the error in the cycle n , d_o the desired sensor output, and c_o the current sensor output in the cycle. Then, PID data is computed by:

$$PID(n) = K_p e(n) + K_i \sum_0^n e(n) + K_d (e(n) - e(n-1)) \quad 3-2$$

where $PID(n)$ is the PID data in the cycle n , K_p the proportional coefficient, K_i the integral coefficient and K_d the derivative coefficient.

Finally, the PID control data is scaled so that it is used as the requested Pulse-Width-Modulation (PWM) duty cycle. The final output is the measured PWM duty cycle. The next sub-subsection will define

how those computations and interfaces were mapped in the different ZX5, XU5, XU3 resources presented previously.

3.3.1.1. Zynq7000 implementation

A simplified block diagram of the control loop implementation in the ZX5 SoM is presented in Figure 3-12.

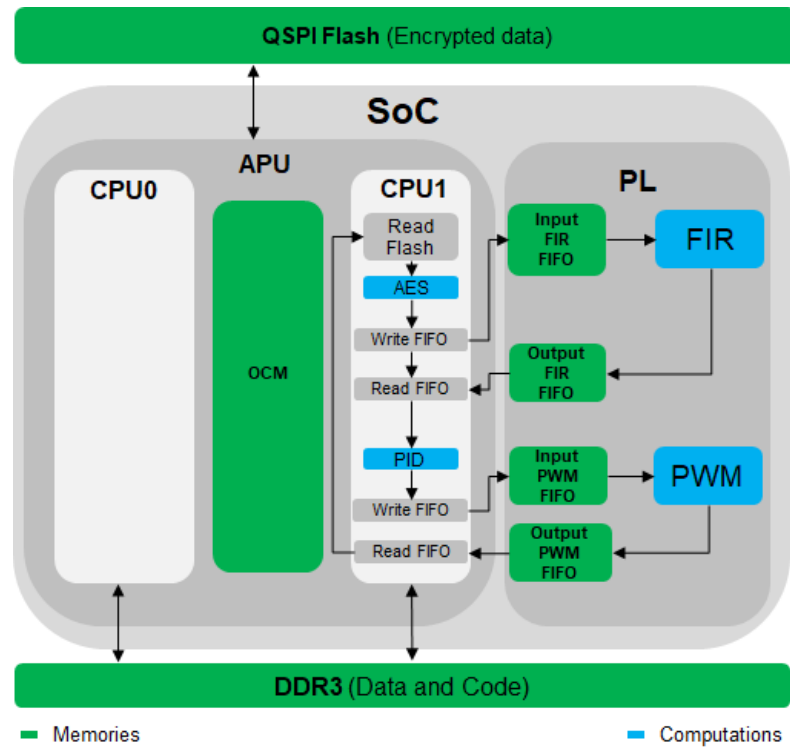


Figure 3-12. Control implementation in the ZX5 SoM

The sensor output mentioned in the previous sub-subsection was simulated by storing encrypted data on the QSPI Flash of the SoM. AES decryption key was also stored on it. It also possible to see in the figure that the different computations were mapped into software and hardware resources. The software part was implemented in baremetal with C in the CPU1 of the APU, and the hardware part was implemented with VHDL firmware and Xilinx IP-cores by using the PL resources. The algorithm begins by allocating memory data chunks of 32-bit words in the DDR3 that will be used to store encrypted data read from the Flash. Then, 16-bytes AES key and encrypted data are read byte-by-byte from the Flash by using a driver that consists in sending commands to the Quad-SPI flash controller in the PS. When encrypted data is available, AES decryption is performed by the open-source algorithm developed by [KOKK14] and validated with the National Institute of Standards and Technology (NIST) data [DWOR05]. Since decrypted data is available, it is sent to the FIR IP-Core implemented on the PL. A detailed block diagram of the PL implementation is presented in Figure 3-13.

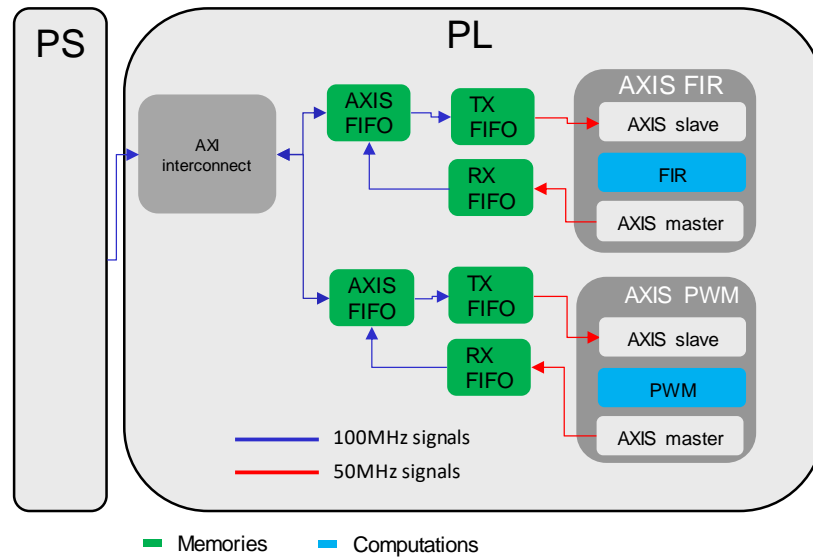


Figure 3-13. Block diagram focusing the PL

As the FIR IP-core provided by Xilinx [XILI15C] and the developed PWM IP-core have an AXI-Stream (AXIS) interface, PS data is sent to it in two phases. The AXI bus is implemented in the PL by an AXI interconnect IP core [XILI17B]. As the AXI bus is memory-mapped, an AXI-AXIS bridge IP-core with embedded FIFO was implemented in the PL [XILI15D]. However, the AXI bus operates at 100MHz and the FIR and PWM IP cores were implemented at 50MHz. The AXIS FIFO supports only one clock domain, thus independent-clock TX and RX FIFO IP cores [XILI17C] were implemented in order to communicate with the FIR and PWM IP cores. The AXI Stream FIFO is implemented with built-in FIFO resources whereas independent-clock FIFOs are implemented using BRAM resources.

In the software part, the PS communicates with the FIR and PWM IP-cores by using a driver that writes the information in the AXIS FIFO and then starts the AXI Stream communication. Then, the AXIS stream FIFO forwards the data to the TX FIFO that sends it to the FIR and PWM IP-cores. In the FIR IP-core, 21 signed coefficients are multiplied and accumulated with the input data generating an output.

Back to the software part, after reading the Output FIR FIFO, PID data is computed as described previously in Equations 3-1 and 3-2. After computing PID data, PID values are scaled to the right range for providing the requested PWM duty cycle. The PWM block (in-blue), has a configured period that is set to 16 cycles in the AXI PWM IP-core (in-gray). The PWM block clock cycle is 8 times slower than the AXIS PWM clock. The PWM block has an internal Finite-State Machine (FSM) that registers the period and duty cycle values, counts the cycles in which the PWM is high, providing the measured duty cycle to the AXI stream IP-core. Finally, PWM duty cycle is read by the CPU1 of the APU and the loop resumes.

Two control loop versions were implemented and improved. The version 1 (V1) is the beta version not including the PWM block implementations and exception abort status reporting. In this version the signals

of the PWM AXIS slave were connected on the PWM AXIS master. In the second version (V2), the PWM block was implemented, the status of exception aborts was reported and the code was optimized.

The memory footprint and loop execution time for a data chunk size of 500 words of 32 bits as well as the PL utilization of each version are presented in Table 3-9.

Table 3-9. PS and PL implementation results of the different version of the control loop application

		V1	V2
PS	Data chunk size (words)	500	
	Code size (bits)	341 388	342 676
	Loop execution time (ms)	639.68	126.35
PL	LUT	5 778	5 685
	LUTRAM	571	571
	FF	8 849	9 129
	BRAM blocks	8	8
	DSP	21	22
	AXI frequency	100MHz	
	IP cores frequency	50MHz	
	Essential bits	1 427 312	1 472 613

As one can see in Figure 3-12, the CPU0 and OCM were not used being available for the implementation of test code that will be presented in the next sections.

3.3.1.2. ZynqUltrascale+ implementation

The block diagram of the control loop implementation in the XU5 and XU3 SoMs is presented in Figure 3-14.

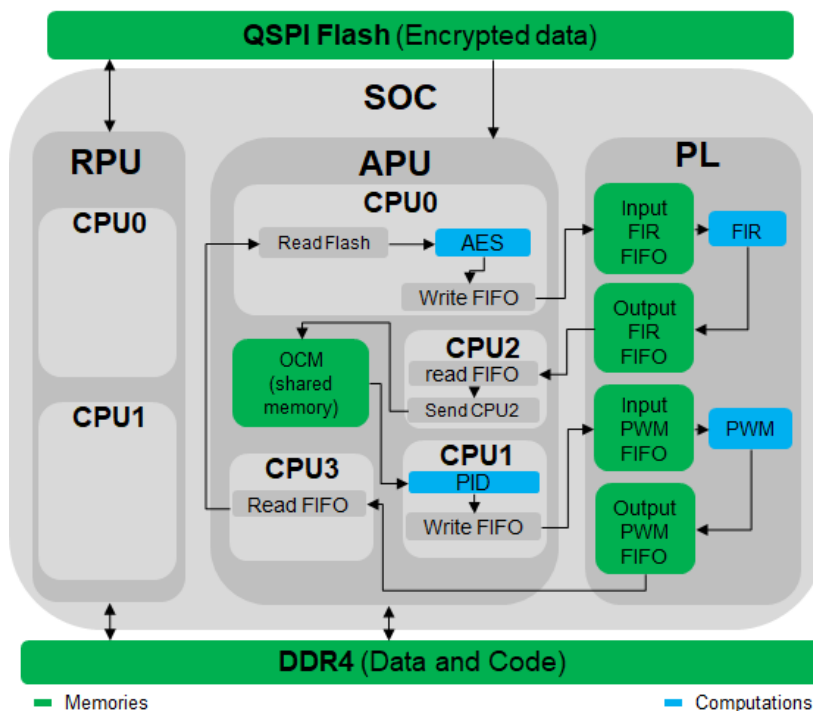


Figure 3-14. Control loop implementation in the XU3 and XU5 SoMs

As it is possible to see in the figure, the application mapping in the SoM resources was similar to the ZX5 implementation. The main difference from the ZX5 implementation was the use of the 64-bit quad cores of the APU instead of 32-bit single-core. In addition, different operations were embedded in the different CPUs. The PL implemented have the same IP-cores presented in Zynq7000 implementation, the difference is that the IP-cores were customized to 64-bit width. The same frequencies of the Zynq7000 implementation were also used.

The algorithm starts in the CPU0 of the APU that runs in FreeRTOS with C. After allocating memory in the DDR4, the encrypted data is read from the Flash by using a driver that sends commands to a Direct Memory Access (DMA) inside the Quad SPI controller. After the AES decryption, decrypted data is sent to the FIR IP-Core and then it waits until the next cycle.

Then, APU CPU1, running in baremetal, allocates memory in the DDR4 to store FIR data that will be read by the FIR Output FIFO. After reading the FIR data, the CPU1 needs to send it to the CPU2 that will compute the PID. It sends it by using a software FIFO implemented on the OCM shared memory. The CPU2, running in FreeRTOS, has a PID periodic task that checks (polling) if a new decrypted data was sent by the CPU1. That task computes the PID data and send the information to another task, named Application task, by using a FreeRTOS queue. The Application task is started first, so that the DDR4 memory is allocated for storing PID data. When the total PID data chunk is read, scaling is performed and scaled PID data is sent to PWM IP-core. Finally, in the CPU3 running in Baremetal, DDR4 memory is allocated for the PWM data that is read from the Output PWM FIFO and the loop resumes. A custom multicore synchronization library and shared memory using the OCM was implemented.

Two versions of the control loop ZU+ application was developed. In the first version (V1) or beta version, the PWM block on the PL was not implemented and the operations in the cores were performed almost sequentially. In the second version (V2), the PWM block was implemented and the code was optimized in

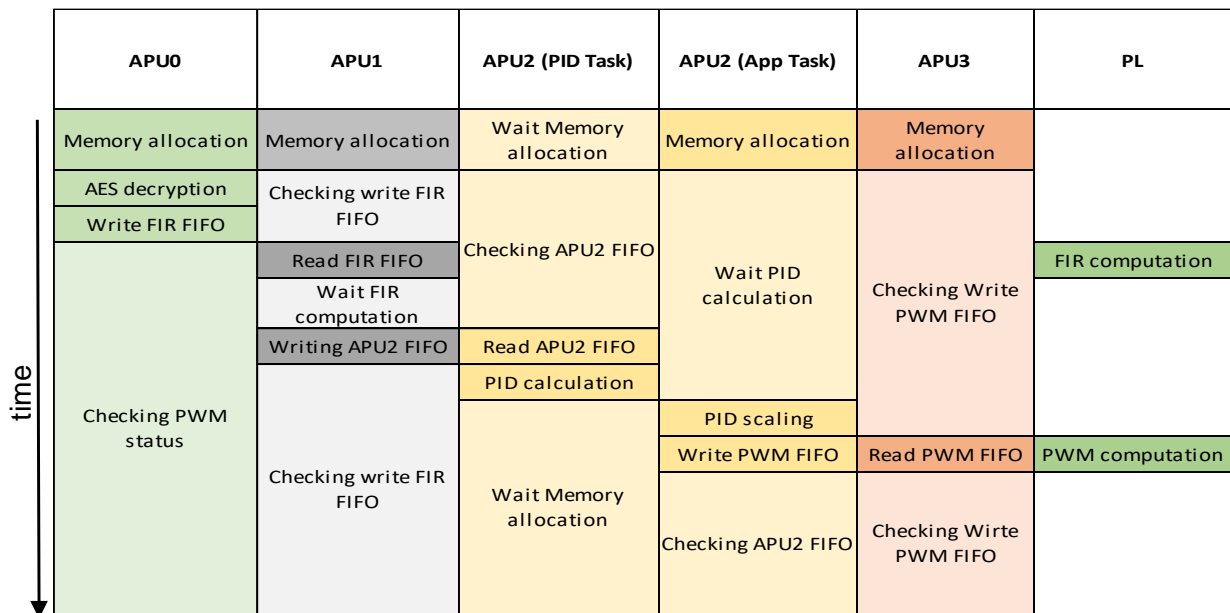


Figure 3-15. Sequence diagram of the ZU+ control loop application V2

order to make profit of the multicore parallelism. Sequence diagrams of control loop V1 and V2 are presented in Figure 3-16 and Figure 3-15, respectively.

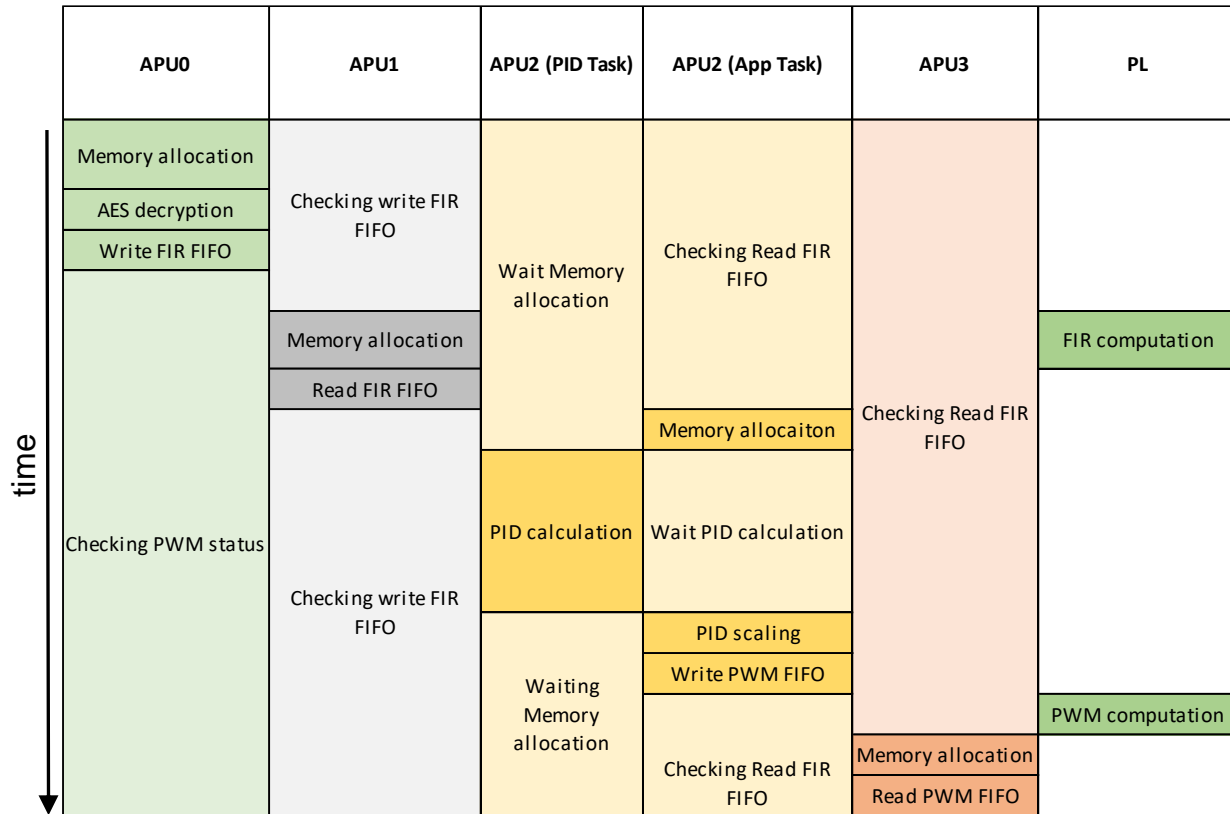


Figure 3-16. Sequence diagram of the ZU+ control loop application V1

The memory footprint and loop execution time for a data chunk size of 500 words of 64 bits as well as utilized PL resources are presented in Table 3-10.

Table 3-10. Implementation results of the different versions of the ZU+ control loop application

		V1	V2
PS	Data chunk (words)	500	
	Code size (bits)	923 400	783 016
	Loop execution time (ms)	5 059	897
PL	LUT	11 839	8 338
	LUTRAM	5 418	713
	FF	149 48	12 376
	BRAM	6	14
	DSP	87	88
	AXI frequency	100	
	IP core frequency	50	
	Essential bits	5 308 022	3 942 716

It is possible to note that the loop execution time of the ZU+ control loop V1 is about 5 seconds. This is due to the fact that the period of the PID task was set to 100ms. As this task was taking most of the processing time, this delay was removed in the second version.

3.3.2. SEE Benchmark application

3.3.2.1. RAM benchmark software

In order to test the SEE sensitivity of the RAM memories (DRAM, BRAM and OCM) of the SoMs, a generic memory test algorithm was developed. The idea of the test algorithm is to write a pattern in the memory positions, and then perform successive checking and corrections to identify the different SEE mechanisms (SET, SBU, MBU, SEFI). The benchmark application can be embedded in the same memory that is under test by defining an offset that corresponds to the amount of memory that is used by the benchmark software application.

Different memories of the SoM can be tested by changing the base address that is defined by the SoC system. Thus, in order to test a memory block, a base address is required, an offset and the test size. The generic RAM memory test algorithm flowchart is presented in Figure 3-17.

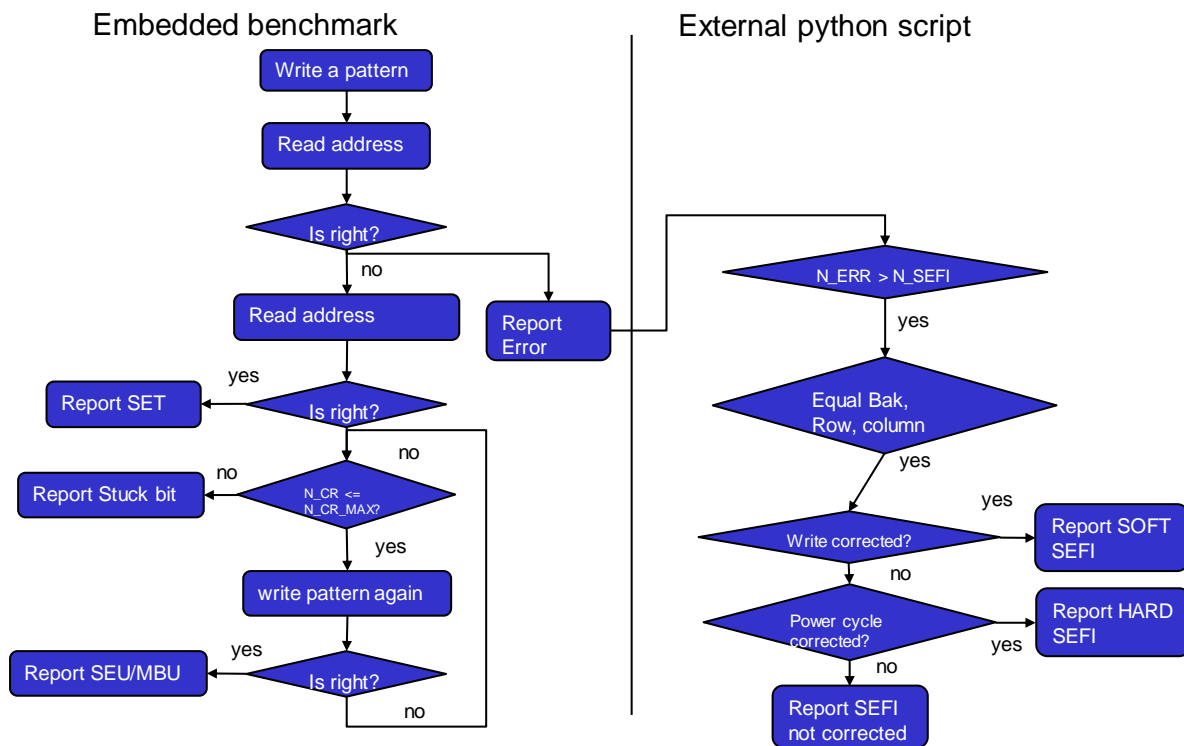


Figure 3-17. Generic RAM memory test algorithm

The left flowchart represents the steps executed in the embedded memory benchmark and the right flowchart represents an external Python script running on the host computer. As the embedded application cannot power cycle the memory it is using, an external python script is required. Details of the Python script will be explained in the following sections. The memory test algorithm was developed in FreeRTOS with the C language and the post processing of the logs was performed with a Python 3.4 script. The FreeRTOS Operating System was chosen so that the memory test algorithm runs one specific task and another periodic task informs that the application is alive. Thus, it is possible to distinguish communication problems with RAM memory, due to error in the communication circuit of memory or SEL, and timeouts on the memory test application. The test processes consist in writing pattern in a memory block, performing successive checking and corrections in each position, jumping to next position until covering all the memory test size.

The checking phase starts by comparing the value in the current address with a gold value and reporting an error, if a mismatched occurs. The address is read again, so that a SET can be identified. If the error persists, the pattern is written again to try to correct it. If the error is corrected, a SBU or MBU is reported, otherwise successive corrections and checking are applied until a maximum number of corrections. If the error is not corrected after the maximum number of attempts, a stuck-bit is reported.

SEFI on the control logic of memories are characterized by a burst of errors in many positions of the same bank, row or column [KOHL18]. As SEFIs are characterized by a burst of errors, if the number of errors exceeds a specified maximum number, other corrections are applied to confirm the SEFI or correct it in order to perform sub-classifications. If the SEFI could be corrected at run-time without requiring a memory power cycle, a Soft SEFI is reported, otherwise a Hard SEFI is reported. Finally, if a SEFI is not corrected even after a power cycle, a permanent SEFI, i.e. device destruction, is reported.

A summary of the memory footprint and loop execution time of the RAM benchmarks implemented on the Z7 and ZU+ SoMs are presented in Table 3-11.

Table 3-11. Z7 and ZU+ RAM benchmark software implementation results

Component	DDR		OCM	
SoM version	Z7	ZU+	Z7	ZU+
Code size (bits)	211 188	190 788	211 784	211 868
Loop execution time (ms)	990	1750	9.7	17.1
Test size (%)	10MB (1%)	10MB (0.5%)	100K (~40%)	100K (~40%)
Test offset	0xFFFFFFFF	0xFFFFFFFF	0x0	0x0

3.3.2.2. *FLASH benchmark software*

In order to test the SEE sensitivity of the Flash memories of the SoM, a different approach from the RAM test memory algorithm has to be used. As blocks of data are written page-by-page, and “0” values can only be written when the sector is erased, the memory positions have to be corrected sector to by sector. Thus, the generic RAM test algorithm cannot be reused and rather a flash specific one has to be developed. Thus, a Flash test algorithm was developed in FreeRTOS with C and was embedded on the DDR memories of the SoMs.

As the Flash is not used to store the code, the entire memory can be tested or a different number of sectors can be defined. The Flash memory test algorithm, as the RAM one, is implemented in an independent FreeRTOS task for the same reason informed in the former. After performing the experiments, the logs are also preprocessed in order to identify SEFIs. The memory test uses a QSPI driver, therefore it is only used for the QSPI Flash of the SoMs. The proposed Flash test algorithm flowchart is presented in Figure 3-18.

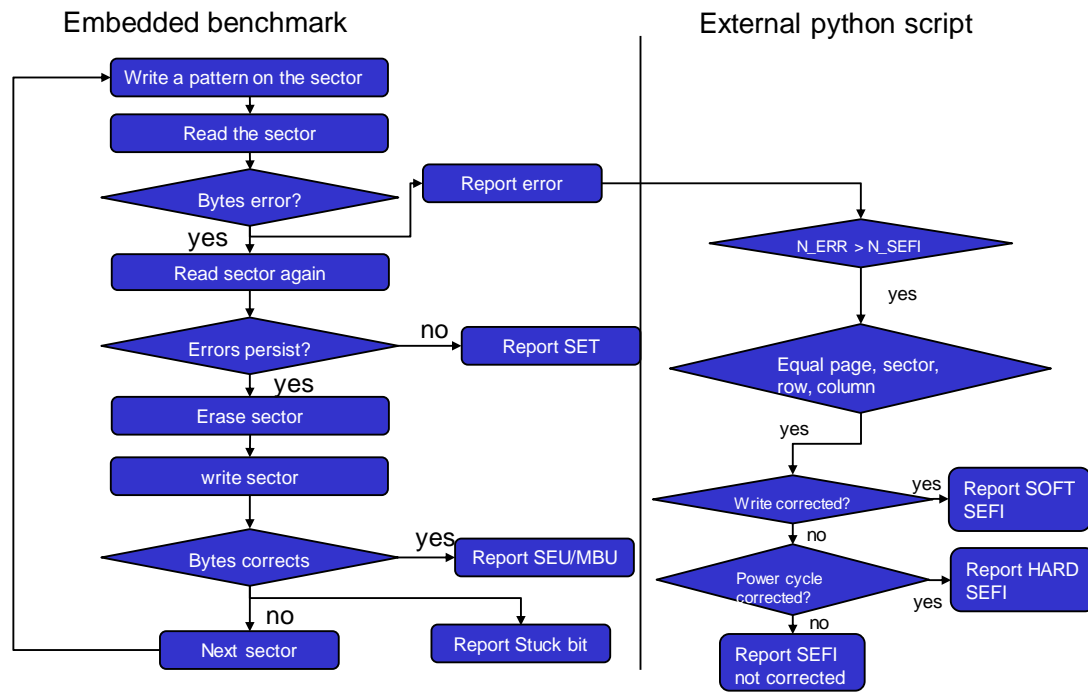


Figure 3-18. Flash memory test algorithm flowchart

The idea of the Flash memory algorithm is similar to the RAM one, it consists in writing a pattern on the pages of a sector and performing successive checking to identify the different effects. First, a pattern is written on the sector, then all the bytes are read and compared to the gold ones in order to identify mismatches. If any byte mismatch occurs, only that byte is read again. If the errors do not persist, a SET is reported, otherwise the correction phase starts. The correction phase consists in erasing the sector and writing the pattern only once. If the wrong bytes of the sector are corrected, SEU/MBU are reported, otherwise a stuck-bit is reported and the next sector is tested. As in the RAM test algorithm, a Python script is used to post-process the logs and identify the different SEFI types. The software development results of the Flash benchmark on the Z7 and ZU+ SoC are presented in Table 3-12.

Table 3-12. Z7 and ZU+ Flash benchmark software implementation results

SoM version	Z7	ZU+
Code size (bits)	874 900	278 816
Loop execution time (ms)	1 510	557
Test size (%)	128K (~0.2%)	128K (~0.2%)
Test offset	0x0	0x0

3.3.3. TID and Aging Benchmark application

As introduced in the subsection 2.2.4.2, TID experiments at system-level can be performed by using panoramic Co^{60} sources. However, one of the main challenges of that approach is to track which component within the system generated a specific parametric degradation or failure. Moreover, analog power devices fail at lower doses than highly integrated digital components, such as SoCs, which survive until doses higher than 100krad [LMSC19].

To this extent, one interesting approach to analyze parametric degradation at component-level is to perform focused TID experiments, such as using X-rays sources, on digital devices. Those components can be characterized by measuring their external electrical parameters such as power supply voltages and currents, or internal parameters such as junction temperature, propagation delay degradation and retention time for DRAM memories. As memories have already been extensively tested under TID in the literature [WKHF18], there is a great interest for the designers on the analysis of TID effects on programmable devices such as the SoCs studied in this work.

Nonetheless, identifying the source of parametric degradation on such complex devices is tricky due to the many configurable resources that are embedded on it. A common approach is to implement test structures or health monitors, which are sensitive enough to see the degradation. On FPGAs, one can take advantage of its flexibility to implement those test structures and analyze the parametric degradation at gate level. In addition, a software running on the PS of the SoC can be used as a flexible self-test controller. Thus, it is possible to monitor component-level TID degradation during a system-level test. That information has a great importance for digital designers of high-speed applications and long missions. Thus, health monitors were implemented in the PL and SoC internal system monitors and baseboard system monitors were used. A generic block diagram of the TID and aging benchmarks for the different SoMs is illustrated in Figure 3-19.

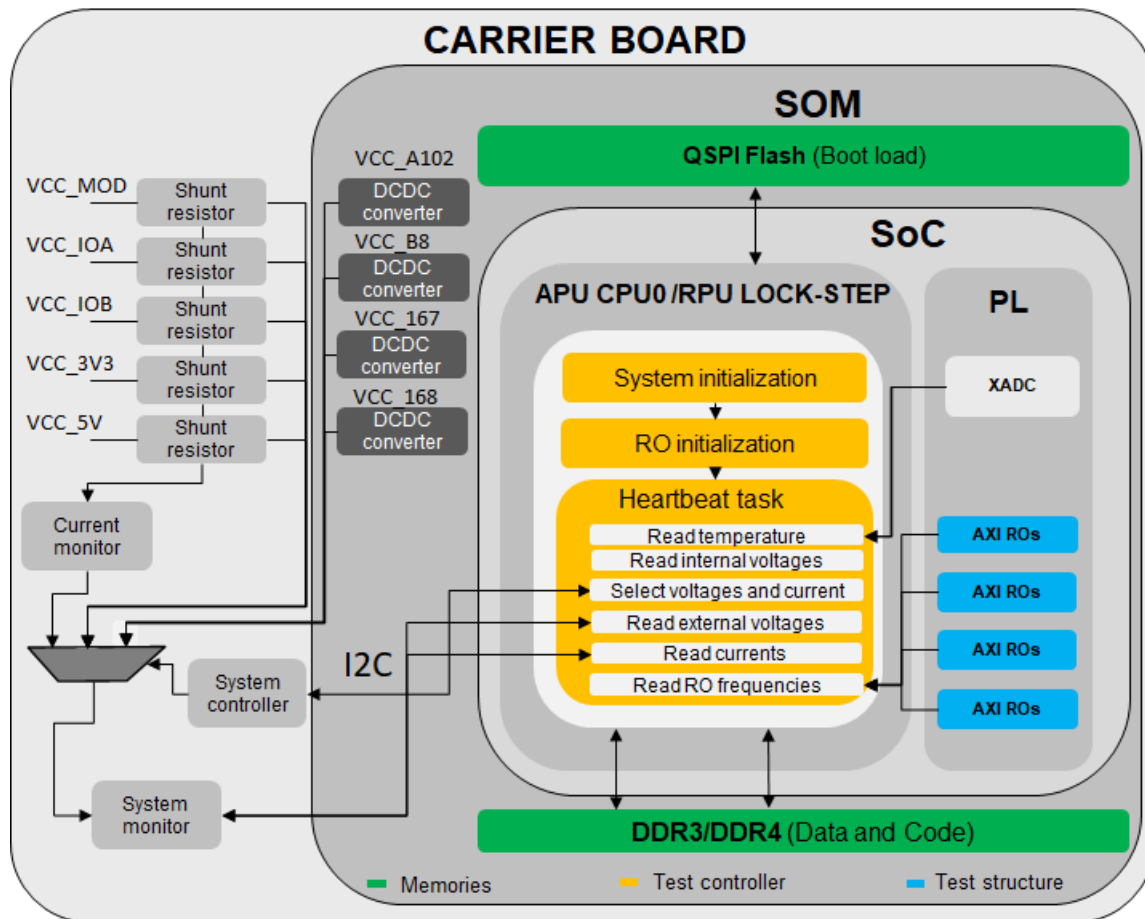


Figure 3-19. Generic block diagram of benchmark implementations on ZX5, XU3 and XU5 SoMs

The PL VHDL firmware is specific for each technology, however the PS C++ software is generic and applied to any module. For the ZynqUltrascale+ SoCs, the benchmark runs in FreeRTOS on the RPU operating at lock-step, whereas for the Zynq7000 SoC, the benchmark runs in FreeRTOS on the APU CPU0.

The health monitors consist on flexible Ring Oscillator (RO) test structures implemented on the PL. The main idea of ROs oscillators is to provide a measurement of the PL logic timing by means of the following equation:

$$1/2f = \sum_j \tau_j + \tau_{routing} \quad 3-3$$

where f is the frequency of the ring oscillator, j the index of the gate, τ_j the delay of a gate in the ring and $\tau_{routing}$ the routing delay of the feedback.

The programmable ROs are interfaced with the PS by a memory-mapped AXI slave wrapper, as illustrated in the schematic in Figure 3-20.

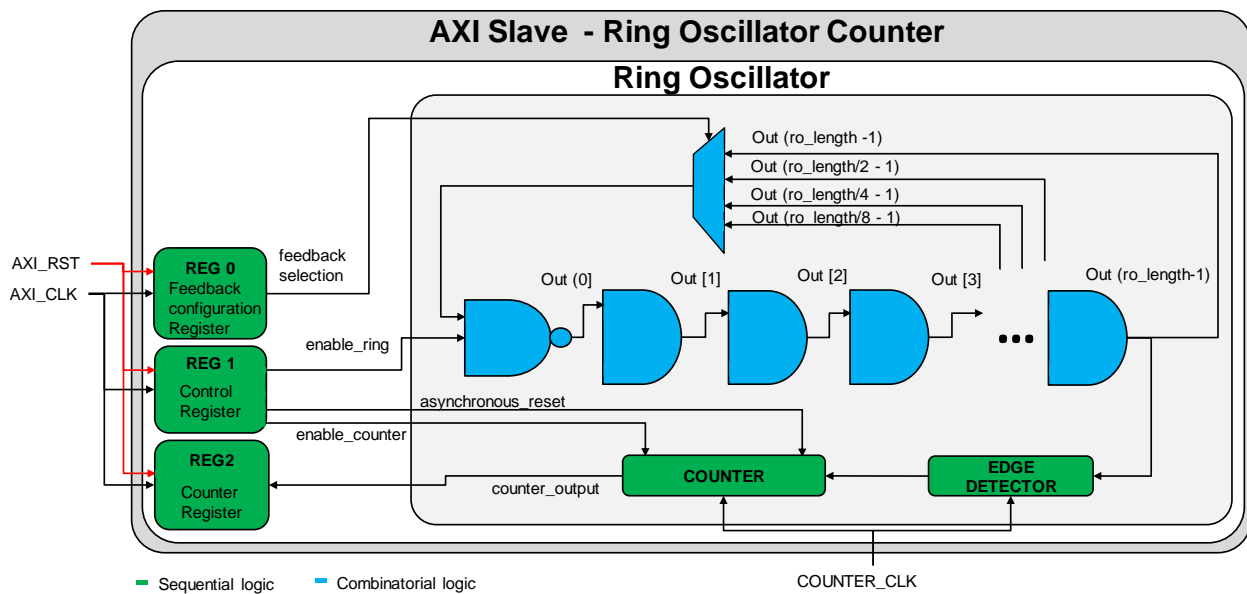


Figure 3-20. Schematic of the Ring Oscillator test structures

Three memory mapped registers are enough for controlling each RO structure. The registers are bit-mapped in order to perform different operations. The Register (REG) 1 is dedicated for controlling the test structure that consists of enabling the ring oscillators, resetting them by using a control signal, enabling the edge detector counter, and resetting the edge detector counter. The functionality of REG 0 is to select the feedback of the ring oscillator by dividing the length by 1, 2, 4 or 8. Finally, REG2 stores the edge count that when divided by the period gives the frequency of the ring oscillator. The edge counter clock is feed by an external clock source IP. This IP can be a PLL or MMCM clock source. However, the AXI registers operates at a different frequency. A block diagram showing the different clock domains of the SoC implementation is presented in Figure 3-21.

The algorithm starts with the initialization of the system and test structures and then it waits for an initialization commands sent by an Ethernet port to start the heartbeat task that will perform the measurements. The period of the heartbeat task is configured according to execution time of the different measurements. The

junction temperature and internal voltages are measures by a SoC internal system monitor localized in the PL [XILI18B][XILI17D].

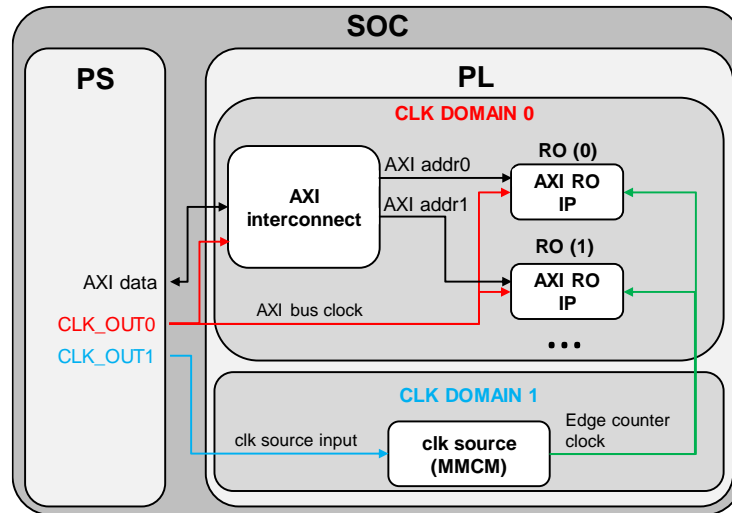


Figure 3-21. Block diagram of the clock domains of the TID/Aging benchmark implementation on SoC

The values are read by using an AXI interfaced protocol driver developed in the software. The internal voltages read by the XADC are presented in Table 3-13.

Table 3-13. SoC internal voltages measured by the XADC

<i>Voltages</i>	<i>ZX5</i>	<i>XU5</i>	<i>XU3</i>	<i>Description</i>
VCCINT	1.0	0.85	0.85	PL internal voltage
VCCAUX	1.8	1.8	1.8	PL auxiliary voltage
VCCREFP	1.25	0	0	Negative voltage reference
VCCREFN	0	0	0	Positive voltage reference
VCCBRAM	1.0	0.85	0.85	BRAM voltage
VCCPINT	1.0	0.85	0.85	PS internal voltage
VCCPAUX	1.8	0.85	0.85	PS Auxiliary voltage
VCCMEM	1.5	1.8	1.8	External DDR voltage

For measurements of external voltages and currents, a system monitor assembled on carrier board is used. This system monitor is interfaced with SoC by using an I2C (Inter-Integrated Circuit) bus [NXP14]. The different voltage and currents that can be measured are summarized in Table A-1 of the appendix.

The implementation results of the TID/Aging benchmark on the Z7 and ZU+ SoCs are presented in Table 3-14 and the parameters of two sets of ROs implemented are presented in Table 3-15.

Table 3-14. TID/aging benchmark implementation results on the Z7 and ZU+ SoCs

		Z7	ZU+
PS	Code size (bytes)	2 572 852	2 542 064
	Loop execution time (ms)	400	490
	Resource required	APU - Core 0	RPU
PL	LUT	41 743	24 477
	LUTRAM	58	256
	FF	7027	9215
	BUFG	12	8
	MMCM	4	3
	PLL	1	0
	AXI frequency (MHz)	100	50
	Edge detector frequency (MHz)	50	50

Table 3-15. Parameters of two sets of ROs implemented on the Z7 and ZU+ SoCs

	Z7		ZU+	
	GROUP 1	GROUP2	GROUP1	GROUP2
Number of ROs	16	11	13	9
RO length	3000	1024	1500	1500
RO frequency at 78C (kHz)	580	1900	2000	2000
Average gate delay (ns)	~0,5		~0,3	

A representative final application designed for SEE experiments and a benchmark for TID/Aging experiments were implemented. The proposed TID/Aging benchmark using test structures is enough for measuring the degradation at the elementary device level. However, by observing only the behavior of the final application, it is not possible to understand which components are failing in a system. Thereafter, in the next sections such testing issues, related to SEE system-level test, will be addressed.

3.4. Testability and data analysis on system-level radiation testing

In this subsection, the issues related to digital system testing will be discussed. First, testing metrics that have to be considered for both SEE and TID testing will be introduced. Then, the impact of poor testability on system-level data analysis and how to mitigate it, will be briefly discussed.

3.4.1. Testing metrics on radiation and aging testing

The functionality loss and parametric degradation of a system induced by radiation have to be measured by using different testing techniques. In order to measure functionality loss induced by SEE, functional tests have to be performed that consists in applying an input pattern and verifying if the system's output corresponds with the specified requirements. In the structural test (white-box), used when developing a system, any internal input and output are visible. However, a customer does not have access to all internal inputs and outputs of a component, thus a functional test (black-box) has to be performed. It is worth mentioning that the functional test only proves the presence of errors and not absence of errors. Therefore, the fault coverage of the system has to be defined [BUAG04].

Regarding the parametric degradation induced by TID or aging on digital systems, a parametric testing is indicated. However, as discussed earlier, the customer usually does not have access to internal degradation on components. Thus, only external measurements of electric parameters can be performed on non-programmable components such as memories and power regulator, or test structures can be designed on programmable components such as programmable SoCs. In addition, as electric parameters are degraded, it can lead to intermittent functionality loss and even permanent loss of functionality.

When performing functional or parametric tests, important metrics to be considered are controllability and observability. Controllability is a qualitative metric that indicates the easiness of forcing a value in a given node of an electronic circuit, whereas observability is a qualitative metric that indicate the easiness of observing an internal node in an electronic circuit.

The objective of radiation or aging experiments is not to force directly a value in a circuit node but observe it. Therefore, controllability is more important for performing verifications or fault injections by emulation, while high observability is extremely important for radiation and aging experiments as it defines the fault coverage of a test.

3.4.2. Impact of limited observability on root cause analysis

High observability are also important when analyzing aging and radiation results. One important data analysis is the root cause analysis that aims to identify the fault mode and source of a failure in a system. When they are identified, it is possible to apply specific hardening techniques on those resources avoiding the overheads associated to overprotection. In addition, high observability enables the understanding of fault propagation and masking on complex digital systems. Thus, it is possible to estimate more precisely the SEE rates, and TID and aging degradation probabilities.

When assembling components into a system, the observability of the inputs and outputs of the components is reduced. One way to solve that is to add instrumentation. Instrumentation, in the scope of this work, is any additional electrical circuitry, software or IP-core to increase system observability during a radiation or aging test. However, instrumentation overhead has to be considered during the tests when a self-controller is used, as it influences the results.

3.5. Software Instrumentation

In this section, the implementation details of the software instrumentations added to the control loop applications will be described.

3.5.1. Computation verification and control flow checking

The instrumentation aims to monitor data integrity of the memories used in the SoMs, the computations performed by the two different processing elements of the SoC (PS and PL) and the control flow of the application. The spare resources on the SoC were used to embed the SoM instrumentation. An illustration of the instrumentation addition on the Z7 and ZU+ SoCs are presented in Figure 3-22 and Figure 3-23, respectively.

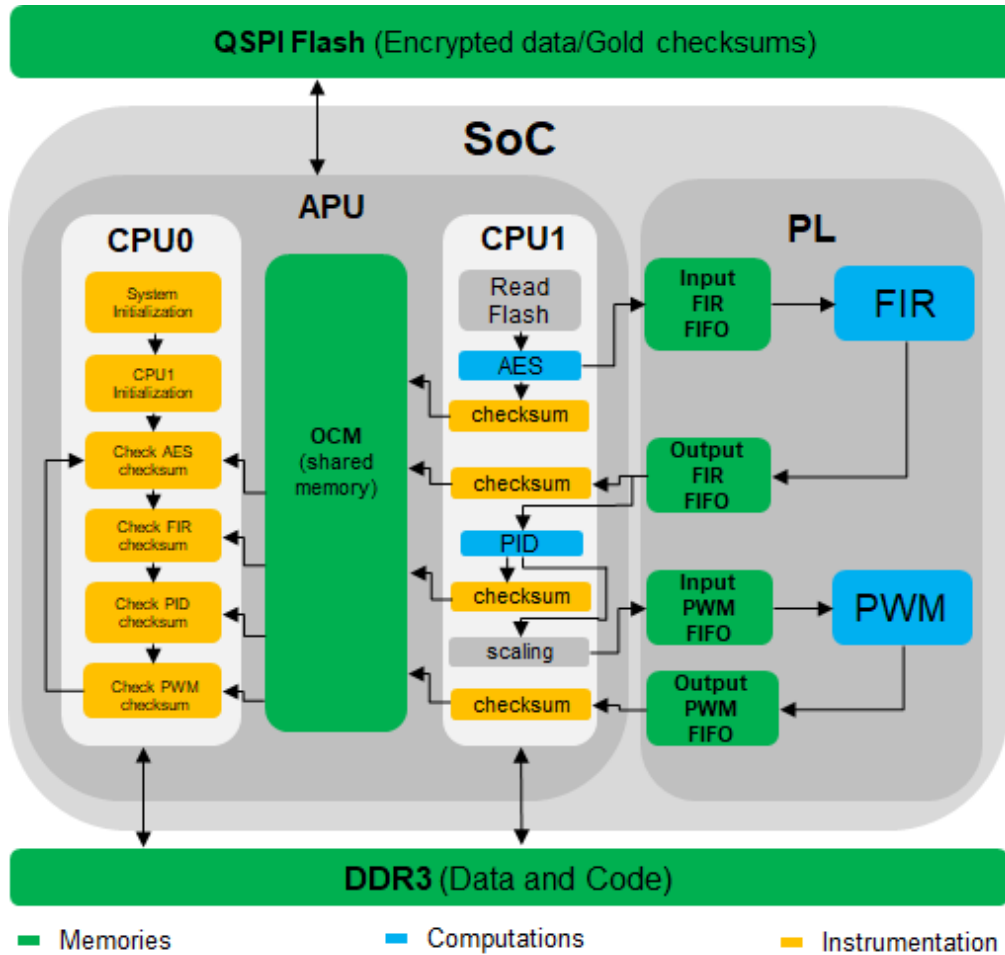


Figure 3-22. Z7 Control loop application embedding the instrumentation layer

The self-test controller was implemented in the APU core 0 for the Z7 implementation and in the RPU for the ZU+ implementation. The RPU running at lock-step was selected for the ZU+ implementation as it has a higher reliability than the APU. The objective of the self-test controller is to initialize the whole system, check computations performed in the control loop application, and receive commands by using the Ethernet protocol, so that on-the-fly test customizations can be performed. Test customization include data chunk sizes,

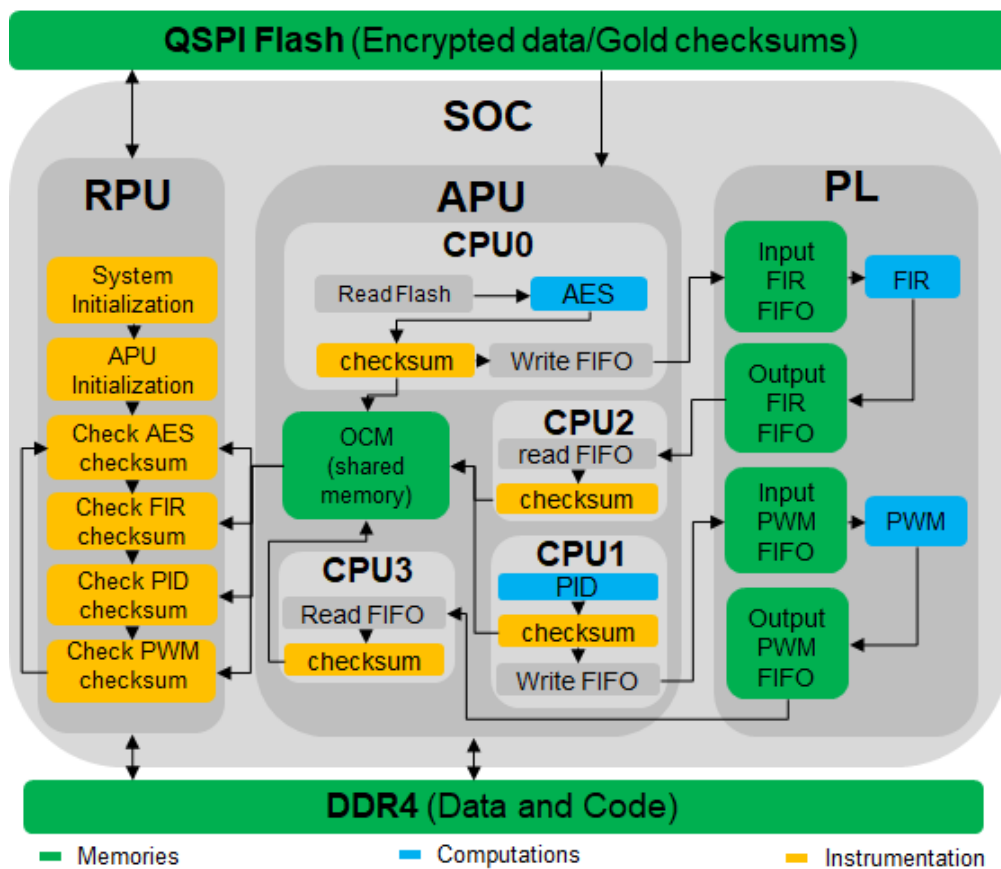


Figure 3-23. ZU+ control loop application embedding the instrumentation layer

number of test cycles and which features of the instrumentation will be added to the control loop application. The OCM was used as shared memory for both Z7 and ZU+ implementations in order to communicate the self-test controller with the cores under test. In order to share OCM data between different cores or processing units, the L2 cache was disabled on the self-test controller. The information exchanged between the self-test controller and control loop application are data to be checked, synchronization messages and commands.

3.5.1.1. Computation verification

An efficient and low-overhead computation verification is the checksum verification consisting in simply summing all the results of the data chunk computation. The sum of the computation data (AES, FIR, PID and PWM) was performed in the cores under test (APU CPU1 for Z7 and APU for ZU+) and the verification was performed in the self-test controller. After computing the checksum, 32-bit and 64-bit checksums are sent to the Z7 and ZU+ self-test controllers, respectively. Then, the self-test controller, reads the gold checksum value and compares it to the actual checksum value read from the OCM. If a checksum mismatch occurs, different corrections are performed in order to classify different events. The checksum verification and error reporting flowchart is presented in Figure 3-24.

When a checksum mismatch is identified for the first time, a checksum error is reported and then the checksums are read again. If the error persists, a persistent error is reported, the memory Error Correction Code (ECC) registers are reported and the self-test controller sends a command to the cores repeat the computation, otherwise a transient error is reported. If the error cannot be corrected, an uncorrected error is reported as well as memory ECC registers again, otherwise a corrected error is reported. In a Python script running in host

computer, the error is verified, if it is a repeated uncorrected error, the script reconfigures the SoC with the

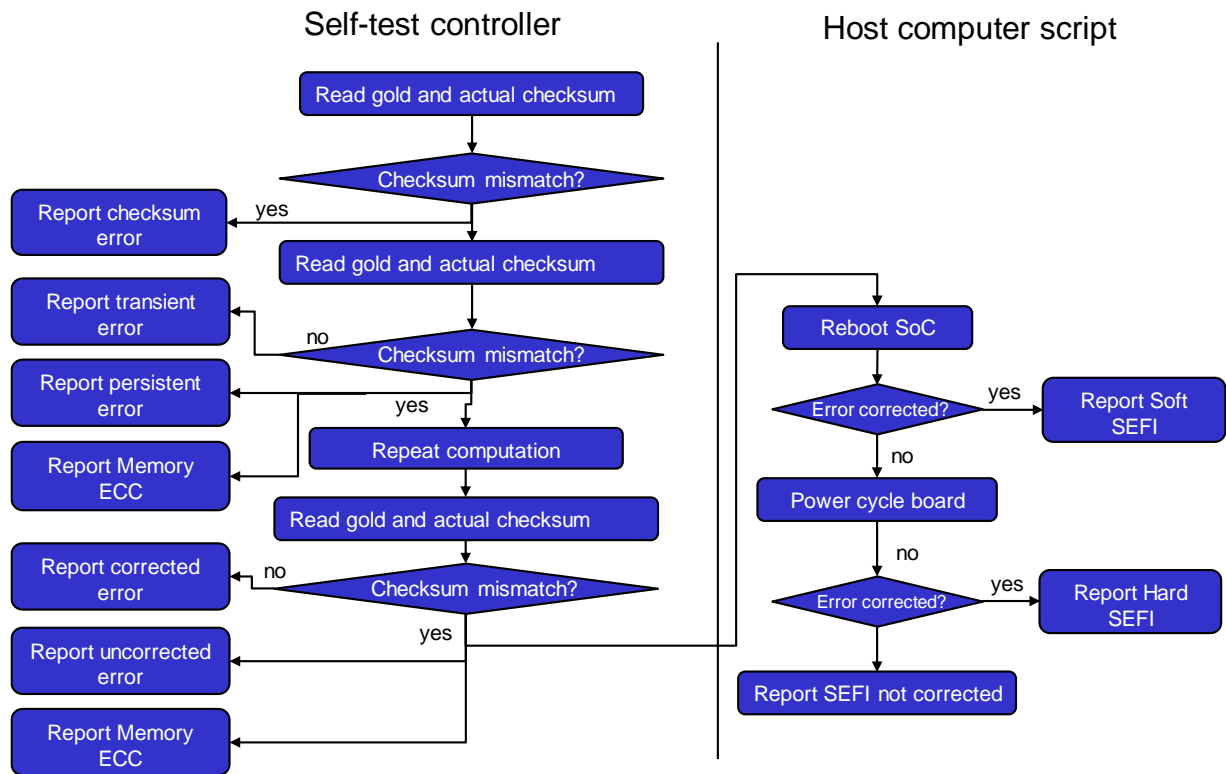


Figure 3-24. Checksum verification and correction operation performed in the self-test controller and in the host PC

code and bitstream.

If it corrects the error, a soft SEFI is reported, otherwise the board is power cycled. If a power cycle corrects the error, a hard SEFI is reported, otherwise a SEFI not corrected or permanent SEFI is reported, i.e. device destruction.

3.5.1.2. Application flow verification

The control flow verification aims to verify if the application is still executing with the right sequence. In order to verify if the control flow application is still running, watchdog counters were implemented in the control loop cores. The watchdog counters are implemented differently according to the embedded OS. In the cores embedding the FreeRTOS, for the ZU+ implementation, a periodic task increments a counter that is checked by the self-test controllers. If the counters stop increasing, a timeout is reported by the self-test controller. The watchdog counters values are verified in the self-test controller by a period task in the FreeRTOS. In the cores embedding baremetal (Z7 and ZU+ implementation), the watchdog counter is incremented between specific operations. Additionally, to the watchdog timeout verification, the current state of the system is also reported by flags. Those flags are reported when specific operations are performed. The right sequence is verified by comparing the current state with the previous state.

3.5.2. Instrumentation levels

The computation, control flow and memory integrity verification features of the software instrumentation layers were presented. The different features were divided into levels that have an associated overhead and observability. The instrumentation level (IL) has to be chosen by the tester according to the required fault coverage. The ILs are incremental, i.e. IL2 contains IL1 and IL0 and... The instrumentation code was manually added by including calls, from a developed instrumentation level library, to the application source code. The different calls are defined by their IL and the ILs are selected by using pre-processor directives (#if and #else). Thus, the code associated to one IL is only included if it is enabled.

The purpose of the IL0, is to provide minimal observability with low overhead for checking the computation of the application and its control flow. In this level, the control flow of the application is verified by detecting timeouts and reporting the current state of the application software. When the current state is not expected according to the previous state, it means the components responsible for executing (SoC) or storing the instruction (SoC, DDR) are failing. Therefore, this IL, can help on identifying errors related to the software application.

The IL1 provides an observability increase on external components (DDR and Flash) and intermediate computations (AES, FIR and PID). By correlating upsets on different memories with the error generated in the application output, it is possible to perform a more accurate component root cause analysis. Additionally, when checksums are performed on data computed at intermediate steps of the application, it is possible to observe fault masking and fault propagation between different computations.

Finally, the IL2 provides enhanced observability of SoC resources (OCM and PL FIFO). As memory upsets on PS and PL SoC resources are reported, it is possible to correlate them to checksum errors on computations performed by different resources (PS and PL), thus precision of SoC resource root cause analysis is increased. Additionally, the fault status and address of software exceptions are reported making possible to make a distinction between different resources that generate that fault (OCM, AXI bus and cache memories). Therefore, at this IL, the component root cause analysis (Flash, DDR and SoC) is extended to resources root cause analysis on the most complex component of the system (SoC).

The different verifications performed in which instrumentation level are summarized in Table 3-16.

Table 3-16. Different features of each instrumentation level

Instrumentation level (IL)	Application output checksum verification	Application flow verification	AES, FIR, PID and Checksum	DDR ECC	FLASH ECC	OCM ECC	FIFO ECC	Exception Abort status and address
0	X	X						
1	X	X	X	X	X			
2	X	X	X	X	X	X	X	X

3.5.2.1. Memory data integrity verification

In order to check the data integrity of the SoM memories built-in Error Correction Codes (ECCs) were used. The ECC mechanism consists in encoding a given block of data and attaching the coding bits to this block. The control unit of the memories encodes and decodes the content of memory addresses and writes the number of detected SEUs or MBUs on registers. The encoding process occurs when a given block of data is written in the memory, and the decoding and checking occurs when the content of this block is read. In general, hamming ECC [FIFI90], used for those memories, are able to detect and correct a single bit error and only detect double bit errors, and parity check is only capable of detecting single and double bit errors but not correcting it. The process of reporting the number of memory upsets (SEU and MBUs) was performed differently for each memory. The features of the built-in ECCs and error mechanisms of the different memories on the SoMs are presented in Table 3-17.

Table 3-17. Features of the built-in memory verification mechanisms of the Z7 and ZU+ SoMs

Memory	DDR		OCM		FIFO		Flash	
SoM	Z7	ZU+	Z7	ZU+	Z7	ZU+	Z7	ZU+
Memory verification	ECC	ECC	Detection	ECC	ECC		ECC	
Method	N/A	Hamming	Parity	N/A	Hamming		N/A	
Data block (bits)	16	64	8	64	64		128	
Coding block (bits)	10	8	1	8	8		8	
Checking type	Polling		Interruption	Polling	Interruption		Polling	

3.5.2.2. Instrumentation level implementation

The performance and code size overheads for each ILs and each Z7 implementation version (V1 and V2) are provided in Table 3-18 and Table 3-19, respectively.

Table 3-18. Code size and execution time overheads for each instrumentation level on Z7 control loop V1

IL	Code size (bits)	Code size overhead (%)	Exec. Time (ms)	Exec. time overhead (%)	Resource overhead
-	341388	-	639.68	-	-
0	343116	0.51	739.51	15.61	CORE0
1	343748	0.69	796.23	24.47	CORE0
2	349068	2.25	817.95	27.87	CORE0

Table 3-19. Code size and execution time overheads for each instrumentation level on Z7 control loop V2

IL	Code size (bits)	Code size overhead (%)	Exec. Time (ms)	Exec. time overhead (%)	Resource overhead
-	342676	0	126.35	-	-
0	348388	1.67	132.41	4.79	CORE0
1	348580	1.72	149.32	18.18	CORE0
2	349004	1.85	152.46	20.67	CORE0

The Z7 instrumentation V1 is a beta version. In this version, the exception abort handlers with status and address reporting were not implemented and the code was not optimized. In the Z7 instrumentation V2, the exception abort status and addresses are reported and the code is optimized.

The performance and code size overheads for each IL and each ZU+ implementation version (V1 and V2) are provided in Table 3-20 and Table 3-21, respectively.

Table 3-20. Code size and execution time overheads for each instrumentation level on ZU+ control loop V1

IL	Code size (bits)	Code size overhead (%)	Exec. Time (ms)	Exec. time overhead (%)	Resource overhead
-	923400	0	5059.00	-	-
0	923528	0.014	5072.00	0.26	RPU
1	924680	0.139	5250.00	3.78	RPU

The ZU+ instrumentation V1 was also a beta version for this technology. At this stage, only the checksum verifications from IL0 and IL1 were implemented. No ECC register reporting was implemented. In the ZU+ V2, the code was optimized, the ECC register were reported as well exception abort status and addresses.

Table 3-21. Code size and execution time overheads for each instrumentation level on ZU+ control loop V2

IL	Code size (bits)	Code size overhead (%)	Exec. Time (ms)	Exec. time overhead (%)	Resource overhead
-	776936	0.000	897	-	-
0	777960	0.132	907	1.11	RPU
1	778984	0.264	937	4.46	RPU
2	783528	0.848	947	5.57	RPU

3.6. Test setup

3.6.1. Generic test setup

A simplified generic experimental test setup schematic used in the different experiments is presented in Figure 3-25.

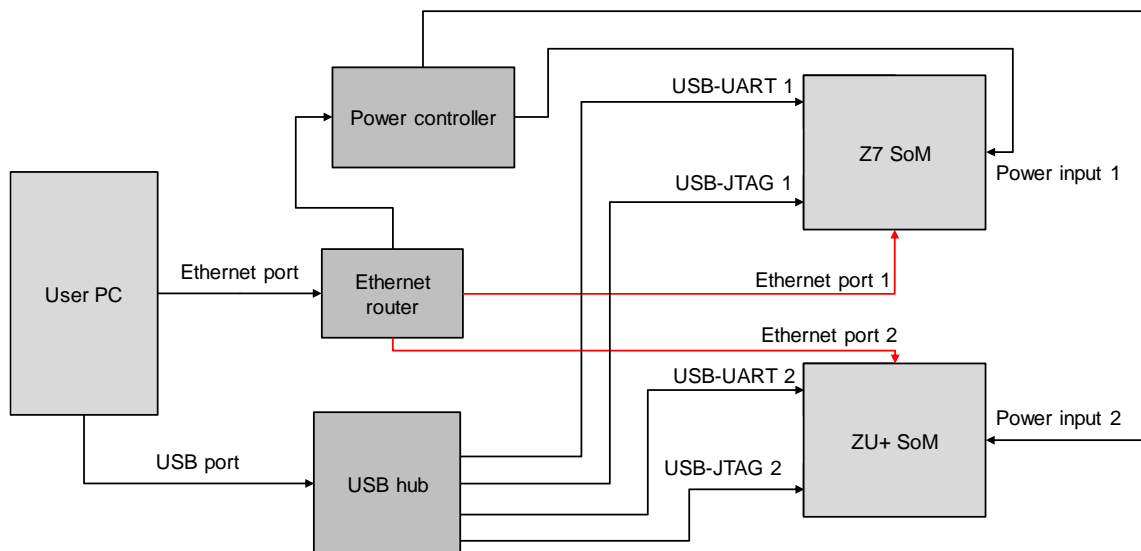


Figure 3-25. Generic test setup schematic including interfaces and protocols

As it is possible to be seen in the picture, in the experiments the Universal Asynchronous Receiver-Transmitter (UART) communication of the SoM was used for reporting the results, the JTAG for programming and debugging the SoCs and the Ethernet port [IEEE18] for performing on-line test customizations. The boards were power cycled by using Ethernet-controlled power controllers such as power switches and Source and Measurement Units (SMUs). The Ethernet and USB (Universal Serial Bus) [USB20] ports are connected to Ethernet router or switches, and USB hubs for communicating with the user PC, respectively.

3.6.2. Test script

A system-level test tool was developed in Python for managing the different communications and test procedures required for SEE and TID system-level experiments. A block diagram of the different modules implemented is illustrated in Figure 3-26.

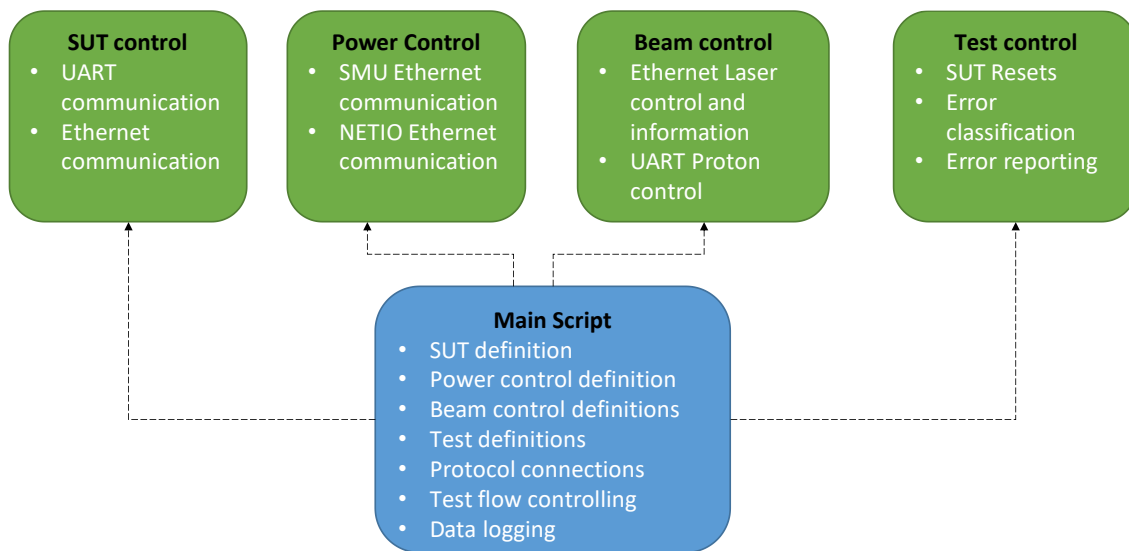


Figure 3-26. Block diagram of Python modules of a customized tool for system-level test

The different functionalities such as beam control or power control can be disabled or enabled according to the experiment. The main script defines all the addresses and ports used for the System Under Test (SUT), power equipment and beam communication. It also selects the power supply (NETIO® or Keysight® SMU) and beam (Laser or proton) to be controlled. After all the connections be performed successfully, the experiment is started. If a persistent system error occurs, the test control module opens the command line Xilinx Software Debugger (XSDB) tool and performs the software and FPGA reconfigurations. If the error is not corrected, the system is power cycled. All the SUT communications and test equipment communication are logged into a text file.

3.7. Carrier boards

Initially, a custom Carrier board (CB) was designed for a mixed-field experiment in the CHARM facility. However, due to the timing constrains and closing of the CHARM facility, the CHARM campaign was cancelled and a commercial CB was used instead. Technical details of the custom developed and the commercial CB will be presented. First, specifications and design details of the custom-designed CB will be described. Second, technical details of the case study CB will be presented.

3.7.1. Custom carrier board PCB design

A block diagram of the custom-designed CB is presented in Figure 3-27.

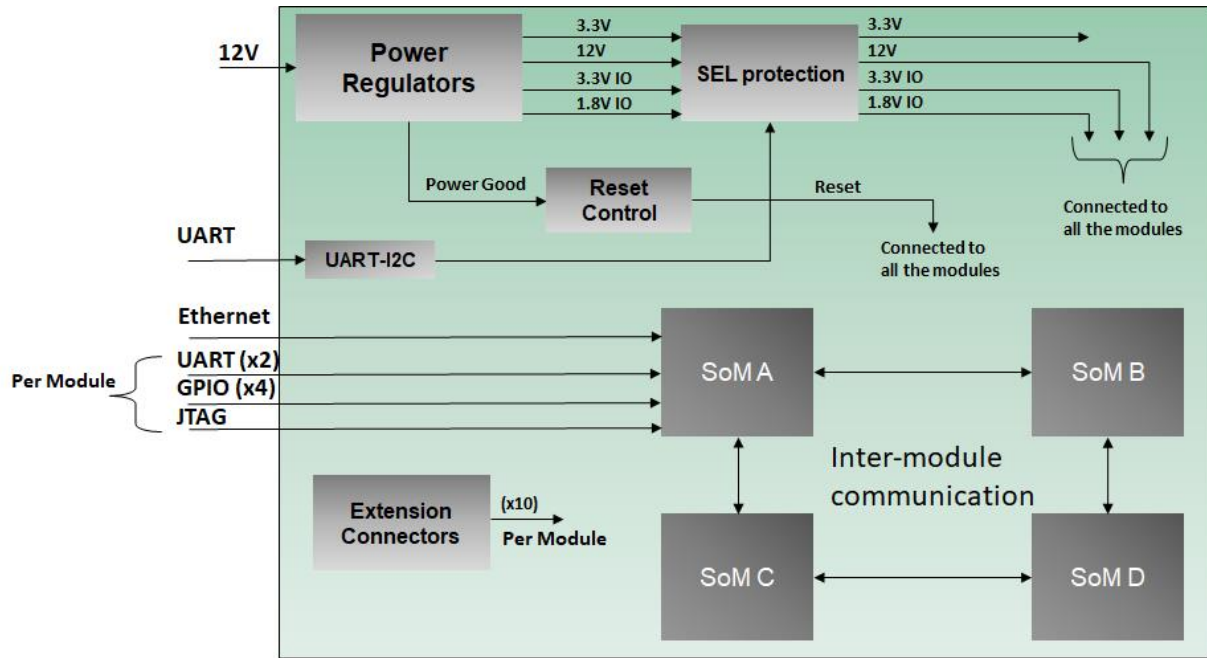


Figure 3-27. Custom-design PCB carrier board block diagram

As it can be seen in Figure 3-27, the carrier board supports four different SoMs for being tested in parallel as the mixed-field radiation environments in the facility allows the testing of systems covering a big area. In addition, it is possible to embed different applications and benchmarks in each SoM corresponding to different environments (aviation, space and ground) in order to validate the bridging methodology. The board is supplied by the 12V input that is connected to power regulators. The power regulators are assembled on daughter boards that are connected to CB (or mother board) by using connectors. It is also possible to connect three stack daughter boards providing power supply redundancy to the board as those components are critical for the experiment. All the voltages provided by the voltage regulators are connected to a SEL Latchup circuit based on current monitors and switches. SELs can be reported by using the UART protocol. The boards also support individual UART, GPIO and JTAG configuration and inter-module communication. However only one module is connected to the Ethernet connector. The PCB was designed on 8-layers, presented in the layout in Figure 3-28.

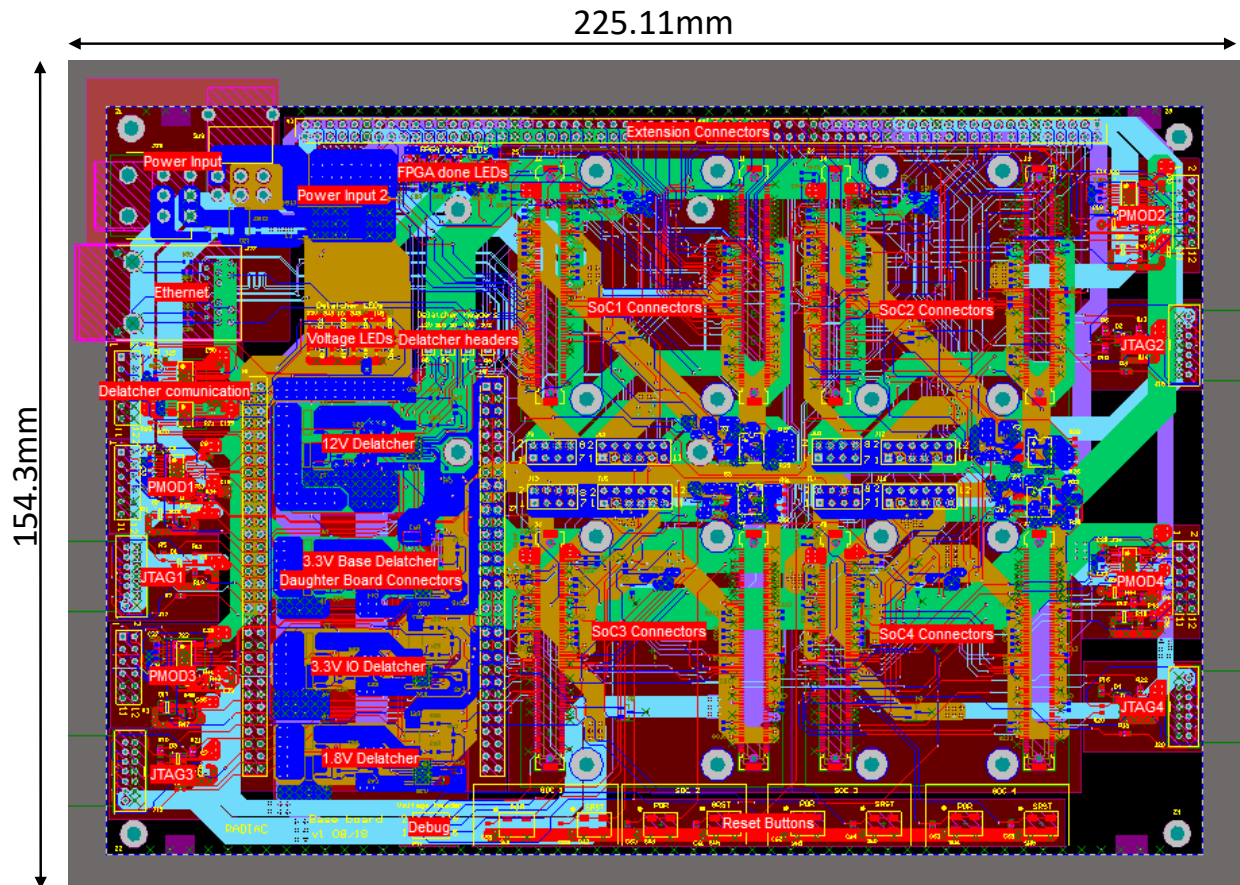


Figure 3-28. 8-layer PCB layout of the custom-designed CB

3.7.2. Commercial carrier board

A Mercury PE1-400 commercial CB was used for the experiments. A block diagram the Mercury PE1-400 is presented in Figure 3-29.

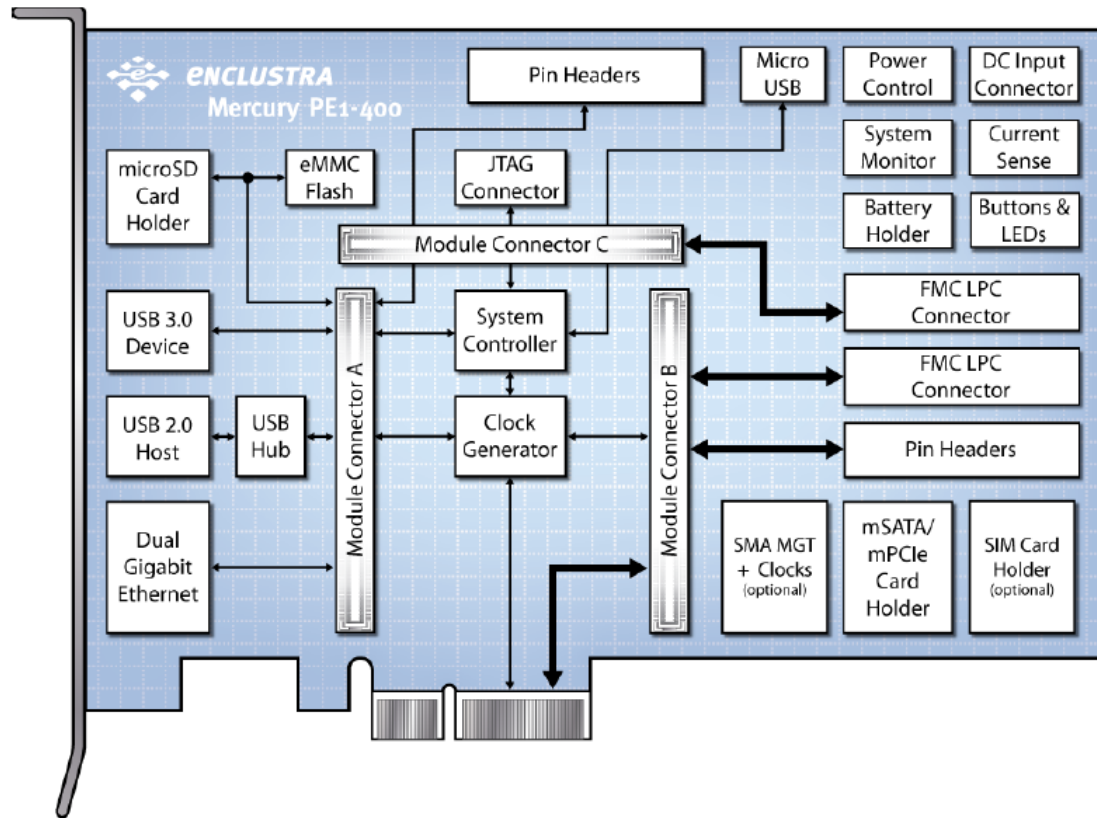


Figure 3-29. Mercury PE1+400 commercial carrier board block diagram

This board can be supplied by a 12V external supply that is filtered and connected to the SoM. Alternatively, the board can also be supplied by a Peripheral Component Interconnect (PCI) express connector or by USB. The DCDC converters on the SoM provide the lowers 2.5V and 1.8V voltages as well as a 3.3V voltage that supply most of the components in the CB. The CB also includes a step-down converted from 12V to 5V and a LDO converted from 3.3V to 1.8V. The different FPGA IO voltages for each module are selected by using jumpers and the SoC boot mode is selected by using DIP switches.

The SoM can be configured by JTAG connectors or an external SD card. It is also possible to configure the Flash on the SoM by using an I2C protocol. For the communications, the CB include a micro USB port, an USB-B 3.0 connector, and several USB-A 2.0 connectors, all of them connected the USB hub. The USB connectors can be connected to an USB-UART transceiver that is connected to the UART pins of the SoM, or connected directly to the USB 2.0 and 3.0 pins. The SoM UART can also be accessed directly by pin headers assembled on the CB. The board also include two Gigabit Ethernet connectors and PMOD connectors for the GPIO pins. The board include ESD protections to all the external connectors. The system controller manages the boot mode selection, USB hub configuration, power supply input selection among other functionalities.

3.8. Conclusions

In this chapter the development of the case study and instrumentation to be used for the proposed bridging methodology was described. First, the technical details of the target SoMs and their components were presented. Then, the development tools for developing the software and the firmware as well the development flow were introduced. Afterwards, the embedded applications for performing system-level SEE experiments and TID experiments, and their implementation results were provided. Then, the testability motivations for developing an instrumentation software layer were explained. Thereafter, the computation and flow verifications, the memory data integrity reporting, and the instrumentation levels and their overheads and benefits were presented. After, a python script for controlling the system-level experiments were described, and finally the carrier boards designed and used were presented.

4. RADIATION EXPERIMENTS

In this chapter, the SEE and TID experiments performed in order to develop and validate the bridging methodology will be presented. For each experiment radiation levels, experimental setup technical details, test methodologies and results will be presented. First component and system level neutron and proton results will be presented and discussed. Finally, component-level X-ray TID and laser experimental results will be provided and analyzed.

4.1. Experiment objectives and chronology

The main objective of the radiation experiments was to accumulate data on various kinds of component-level and system-level events, validate the ability of the instrumentation to capture events and improve the observability of the system. However, the components of the target system have different package thicknesses and a sample preparation (package delidding and thinning) would require a high budget and time. This way, highly penetrating particles were prioritized. Thus, a selection of the different collective campaigns of the RADSAGA project were targeted, which defined a strict schedule for the preparation of the test bench. Radiation test facilities available at the IES lab including laser and X-ray sources were also exploited.

The series of campaigns started with an atmospheric neutrons experiment at the ChipIR facility. In this first SEE radiation experiment, the ZU+ control-loop application and the memory benchmarks were not totally ready. Consequently, a prototype of the ZU+ application, memory benchmarks provided by the SoC manufacturer and a simple test bench were used. The objective was to perform a first-order analysis of the different components of the systems and to know how the system itself behaves when being exposed to radiation.

After the ChipIR neutrons experiment, the available ZU+ modules were destroyed, and then a beta version (V1) of the Z7 control-loop application had to be developed. This version did not include all the functionalities but was improved in comparison to the ZU+ control-loop application V1. In addition, a proper memory benchmark for radiation experiments was developed. Thus, the objective was to get the first results from a complete instrumentation version and component-level results so that they can be correlated.

Thereafter, laser SEE fault injection was conducted on the Z7 SoC PS embedding the control-loop V1 in order to better understand the proton results. The objective of this experiment was to improve resource root cause analysis by injecting faults on specific Z7 SoC PS resources and analyzing their propagation to system-level events.

In the second proton SEE experiment, both Z7 and ZU+ control-loop applications were completed (V2) and improved. Therefore, the objective was to get system-level results and component-level results on two SoM technologies.

After the last SEE protons experiments be performed, the TID radiations campaigns were started on the PL of the SoCs. The objective was to validate the ability of the TID/Aging instrumentation of measuring timing degradation and providing useful information for FPGA designers.

Finally, laser SEE fault injections were carried out on the Z7 SoC PL embedding the control-loop V1 and the ZU+ SoC PS and PL embedding the V2 in order to better understand the proton results and to increase the resource root cause analysis precision. The chronology of the different radiation experiments and which benchmarks were embedded are summarized in Table 4-1 .

Table 4-1. Chronology of the different radiation experiments and the embedded applications on different SoCs

Date	Particle	Benchmarks used	Comments/Remarks
March 2019	Atmospheric neutrons	<ul style="list-style-type: none"> • DDR3 - standard memory benchmark • DDR4 - standard memory benchmark • ZU+ -OCM standard memory benchmark • ZU+ control-loop – V1 	Testbench prototype (Z7 bench not ready)
June 2019	184MeV Protons	<ul style="list-style-type: none"> • DDR3 - developed memory benchmark • Z7 - OCM developed memory benchmark • Z7 – control-loop – V1 	Several issues with the beam line limited the total test time
July 2019	1064nm Laser	<ul style="list-style-type: none"> • Z7 – control-loop – V1 - PS 	
November 2019	184MeV Protons	<ul style="list-style-type: none"> • ZU+ - control-loop – V2 • Z7 – control-loop – V2 	Testbench hardware failures limited the total test time
January 2020	Focused X-ray	<ul style="list-style-type: none"> • Z7 - TID benchmark • ZU+ - TID benchmark 	
July 2020	1064nm Laser	<ul style="list-style-type: none"> • Z7 - control-loop – V1 - PL • ZU+ - control-loop – V2 – PS • ZU+ - control-loop – V2 - PL 	

4.2. Package test considerations on the target hardware systems

In this section, the required ranges for accessing the active layer of the different component packages will be presented. The different thicknesses used to estimate the required ranges for which one of the compounds is illustrated in Figure 4-1 and the worst case range estimation is presented in Table 4-2.

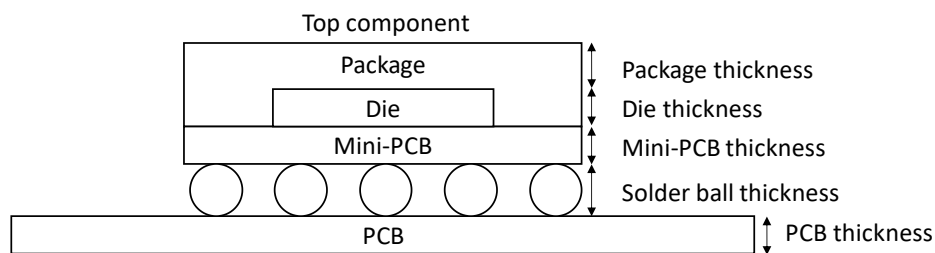


Figure 4-1. Package thicknesses considered in the range estimation

Table 4-2. Estimation of the required ranges for the different materials on the target system components

	Estimated required range (worst case)				
Component	Die substrate (Si)	Epoxy plastic package	Metal lid package (58% Fe and 42% Ni)	PCB dielectric (FR-4) and copper foils	Solder balls (63% Sn and 37% Pb)
ZX5 SoC	0.875mm	-	-	-	0.45mm
XU5 SoC		-	0.7mm	-	
XU3 SoC		-	-	-	
DDR3	0.3mm	0.5mm	-	-	0.9mm
DDR4 (top)			-	-	
DDR4 (bottom)	0.4mm		-	1.7mm	
Nor Flash	0.3mm		-	-	0.45mm
DCDC converter			-	-	0.1mm

According to SRIM simulations [ZIEG14] performed with the compounds described in Table 4-2, a proton energy higher than 50MeV is required to go through all the different materials. Regarding neutrons, according to [CARU10], thermal neutrons are enough for going through the different materials presented.

4.3. Atmospheric neutrons experiments

4.3.1. Facility parameters

As previously mentioned, the neutrons experiment was conducted in the ChipIR beam line of the ISIS spallation source located in the Rutherford Appleton Laboratory. This facility produces neutrons with energies up to 800MeV representing closely the atmosphere spectrum, as plotted in Figure 4-2.

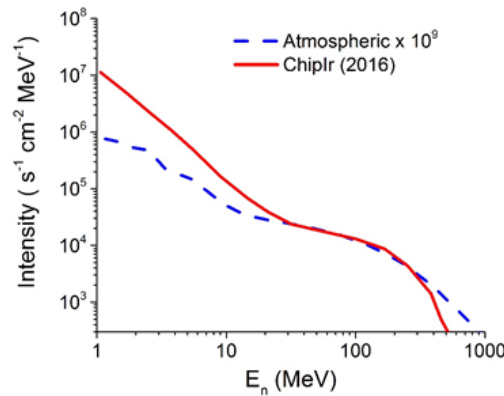


Figure 4-2. ChipIR neutron spectrum

The integral fluxes ($E_n > 10\text{MeV}$) and field sizes depend on the DUT positions. Neutrons detectors are placed on four different positions of the table. The integral flux and beam size of which position is presented in Table 4-3.

Table 4-3. Integral fluxes and beam sizes for the four positions

Position	A	B	C	D
Distance from beam output (cm)	10	110	320	440
Integral Flux ($n/cm^2.s$)	5.4E+6	4.6E+6	3.57E+6	3.1E+6
Beam size (cm^2)	7	7.9	10	11

The room layout of the ChipIR facility is presented in Figure 4-3.

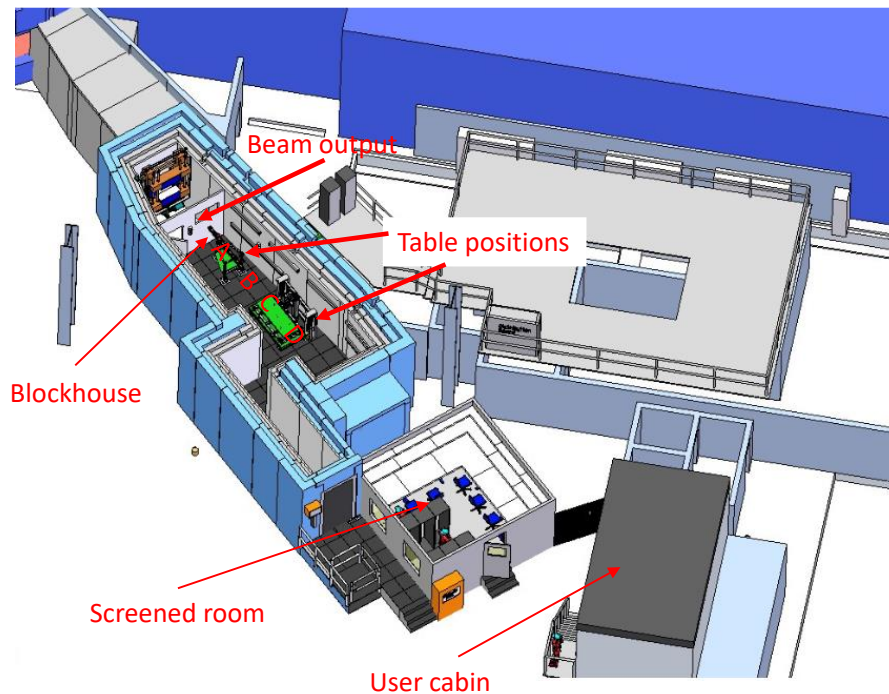


Figure 4-3. Room layout of the ChipIR facility

As it is possible to see in the picture, the Block house room (irradiation area) has two separated tables where the different positions are localized. In the Screened room (control room), the beam is controlled by the facility staff and the measurement equipment is controlled by the user. Additionally, the user can also control the experiments by the user cabin using the Ethernet protocol.

A picture of the carrier board with a SoM mounted in front of the neutron beam line is presented in Figure 4-4.

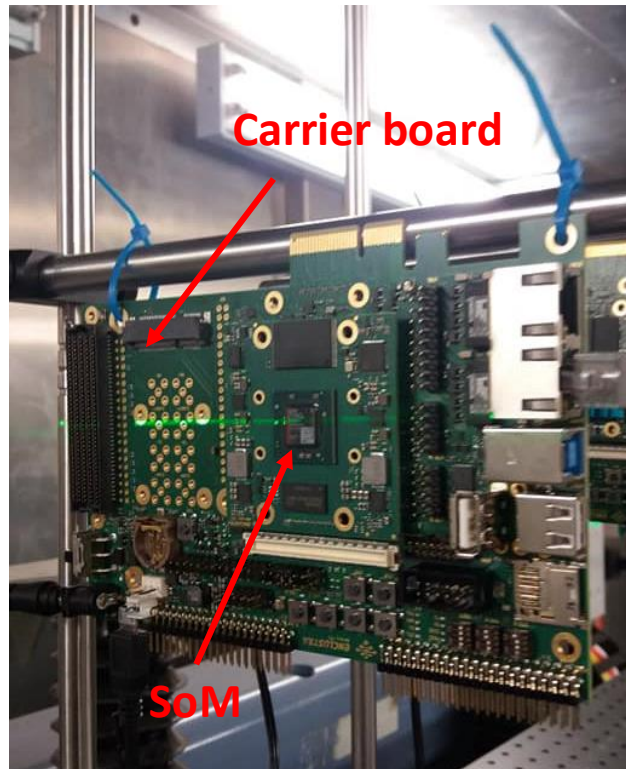


Figure 4-4. ChipIR experiment picture – Two carrier boards with SoMs mounted in front of the beam line

4.3.2. Experimental setup

Atmospheric-like neutrons up to 800MeV can penetrate dozens of centimeters of the different materials that compose the component packages and the SoM PCB. To this extent, two boards were stacked horizontally and tested simultaneously during some runs in order to save beam time. An illustration of the experimental setup for the neutrons experiments is presented in Figure 4-5.

The first Mercury PE1+ CB was placed on the C position (Figure 4-3) and the second one was placed 25cm far from the C position. The CBs were power cycled manually by using an Ethernet controlled power switch provided by the facility. The AC adapters were placed close to the boards, instead of using a power supply in the data collection area, in order to avoid voltage variations associated to long cables. The UART communication was performed by using an UART-USB converter IC embedded on the CB and then connected to an Ethernet controlled USB hub. The JTAG communication was performed by using an external JTAG-USB converter and a JTAG cable extension so that the JTAG-USB converter is not exposed to the beam, then the USB cable was connected to the same USB hub. The Ethernet cables for communicating directly with the boards (RJ-45 connectors) and the USB hub were connected to a patch panel localized about 1 meter far from the position A.

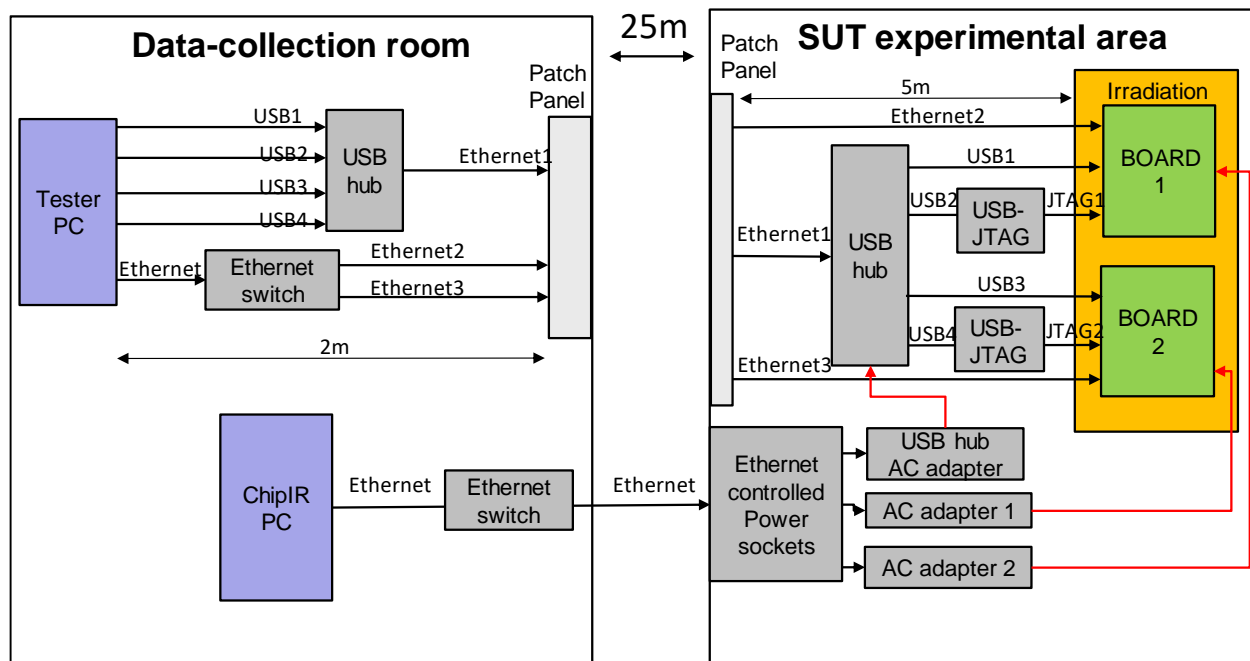


Figure 4-5. ChipIR experimental setup

In the data collection room, the user (Tester) PC was used to control the System Under Test (SUT) and the facility (ChipIR) PC was used to control the beam and power-cycle the boards. The facility also provided a beam shutter button in the data collection run, so that the beam can be quickly stopped manually without having to change the collimators to stop the beam.

4.3.3. Test methodology

The objective of this experiment was to provide system-level and component-level SEE experimental data for developing the bridging methodology. Thus, system-level experiments were conducted in the ZU+ control-loop application V1 implemented on XU5 ZU+ SoM. Component-level experiments were conducted on the ZU+ OCM, DDR and Flash memories of the ZX5 and XU5 SoMs. Some samples were subjected to non-biased high temperature stress (110C) for 53 hours in order to analyze its effect on SEE sensitivity. However, due to the time and budget constraints, it was not possible to test many samples and stress the samples for enough time (typical is 1000 hours) and in the proper conditions (biased with overvoltage). Thus, the stress performed cannot be characterized as a proper aging experiment and can be confused with lot-to-lot variations or sample-to-sample variations. The ID of the different samples is presented in Table 4-4.

Table 4-4. SUT ID for the different samples

SUT #ID	Description
ZX5 #1	Fresh (pristine)
ZX5 #2	Stressed (53H@T=100°C)
XU5 #1	Fresh (pristine)
XU5 #2	Stressed (53H@T=100°C)

A summary of the test log of the neutrons experiment is provided in Table 4-5, the detailed test log is presented in Table A-2 of the appendix.

Table 4-5. Summary of ChipIR test log

Runs #	Energy (MeV)	Average Flux	Target fluence	Minimum fluence reached	Average fluence	Maximum fluence
13	<800MeV	3.00E+06	1.00E+10	1.20E+09	1.19E+10	4.62E+10

The test process consists in loading different application on the boards by using the JTAG communications and logging the outputs by the UART communication. When no information is sent by the UART, the system-level or benchmark application is reloaded manually by using the JTAG communication. If the error persists, the entire CB is power cycled manually. Finally, if the board is not recovered after few power cycles, the board is verified by turning-off the beam and entering the irradiation room, when possible (in shared runs the board was only verified in the end of the run).

For the component-level experiments, SoC manufacturer memory benchmarks were used to test the DDR3 of the Z7 SoC, DDR4 of the ZU+ SoC, the OCM of the ZU+ SoC and the QPSI Flash of both SoCs. For the DDR and OCM experiments, the built-in ECC was not enabled in order to observe SBUs and MBUs. For the Flash experiments, the ECC correction is automatic and was not disabled. Thus, only MBUs would be possible to be observed. The parameters of the component-level memory SEE tests are presented in Table 4-6.

Table 4-6. Memory SEE test parameters

	DDR3		DDR4	OCM	Flash
Samples	ZX5#1	ZX5#2	XU5#1,XU5#2	XU5#1,XU5#2	ZX5#1, ZX5#2,XU5#1,XU5#2
Total size	1GB	1GB	2GB	256KB	64MB
Test offset	0x200000	0x200000	0x200000	0xFFFFC0000	0x0
Tested size	0.98GB	16MB	1.98GB	100KB	16MB
ECC	disabled	disabled	disabled	disabled	enabled

For the system-level experiments, a first version (beta) of the control-loop application was tested. The parameters of the control-loop system-level implementation are presented in Table 4-7.

Table 4-7. Control-loop ZU+ V1 - implementation parameters

Parameter	Value
AXI frequency	100MHz
FIR IP core frequency	50MHz
IP core FIFO size	512
AXIS-AXI4 FIFO size	512
Data chunk size	500
Instrumentation level	1

4.3.4. Results

4.3.4.1. Component-level results

The DDR memory errors were classified into SEU/MBU, SEFIs and stuck-bits. A SEU/MBU error happens when the erroneous value read from a given memory position are corrected by a writing phase. When more than one writing phases correct a memory position, it is characterized as Soft SEFI. Finally, when more than ten writing phases do not correct the value, it is characterized as a Stuck-bit. The results from two DDR3 and DDR4 samples are plotted in Figure 4-6.

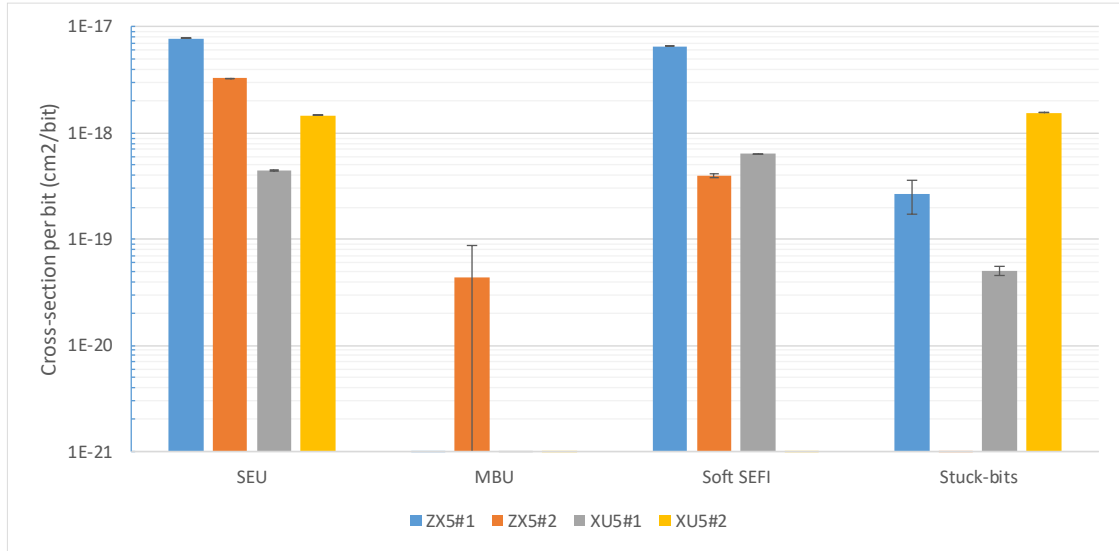


Figure 4-6. SEE cross-sections from the DDR3 and DDR4 samples

According to T-CAD simulations of the atmospheric neutrons on 65nm SRAM memories [PZLH19], the maximum LET produced by secondary ions is about 31.5 MeV/mg/cm^2 . Thus, if the neutron DDR3 results are compared to the heavy-ions results at a LET of 32.1 MeV/mg/cm^2 of the same component [GHGS12], it is possible to note that the observed SEU cross-section ($2.8\text{E-}18 \text{ cm}^2/\text{bit}$) per bit is much lower than the one observed with heavy-ions (about $1\text{E-}11 \text{ cm}^2/\text{bit}$). The same was observed for the Soft SEFIs. That difference is probably related to the low probability ($\sim 1\text{E-}09$) of generation of secondary ions at such high LET due to nuclear interaction. It can also be related to the low error capturing capability of the manufacturer benchmark used that was not initially designed for radiation experiments.

Finally, regarding the DDR4, it is possible to see that the cross-sections are higher than the ones reported by a different DDR4 manufacturer irradiated with 480MeV protons [PJBL17]. The atmospheric neutrons maximum secondary LET is higher than the maximum 480MeV proton ones that is about 15MeV MeV/mg/cm^2 [HIBL03]. Thus, this difference could be related to the neutrons secondary higher LET. Alternatively, this difference could come from the different DDR4 manufacturer or the benchmarks used to test memories. Heavy-ions results at LETs up to 15 MeV/mg/cm^2 has also been reported for another DDR4 manufacturer [GUCU17] where a higher SEU cross-section was observed ($1\text{E-}15 \text{ cm}^2$). On the other hand, a similar stuck-bit cross-section ($\sim 1\text{E-}19$) to the sample XU5#1 was observed. The lower cross-sections observed in the DDR4 experiments can also be related to the benchmark used and different manufacturer. As the same benchmark was used for both DDR3 and DDR4, it is possible to note that the DDR4 had a smaller

cross-section per bit than the DDR3 for SEUs and a higher cross-section per bit for stuck-bits. A lower SEE sensitivity is expected for DDR4 devices compared to DDR3.

During the experiments hard SEFIs on the board were also reported. Power-cycles were required to restore normal operation. Due to the low electrical instrumentation-level (absence of points of measurement), it was not possible to track which component of the board generated the hard SEFI.

In the ZynqUltrascale+ OCM experiment, no error was observed for both XU5#1 and XU5#2 samples for a fluence of $1.10\text{E}+10$ n/cm² and $1.15\text{E}+10$ n/cm², respectively. In the Flash embedded on the samples ZX5#1, ZX5#2 and XU5#1, almost no error was observed for fluences of $2.30\text{E}+09$ n/cm², $1.20\text{E}+09$ n/cm² and $6.19\text{E}+09$ n/cm², respectively. Only a MBU error was observed in the ZX5 #1 Flash. Only one application timeout was observed on the XU5 #2 Flash memory test algorithm, and 12 and 4 timeouts were observed in Fresh and Aged ZX5 Flash memory tests algorithms, respectively. As the Flash algorithm was running in a dedicated task of the FreeRTOS, the application should keep running if a SEFI occurs on Flash. Thus, the timeouts were probably generated in the SoC or DDR instead of the Flash.

4.3.4.2. System-level results

A description of the control-loop system-level event acronyms used for plotting results is presented in Table 4-8.

Table 4-8. Control-loop system-level events acronyms

Acronym	Description	IL
RPU	RPU 0 Timeout	0
PWME	PWM Checksum Error	
AESE	AES Checksum Error	1
FIRE	FIR Checksum Error	
PIDE	PID Checksum Error	

Regarding the system-level results, as explained before, a prototype of the code-instrumentation was added to the control application. This way, only checksum errors of the intermediate steps and timeouts in the RPU were observed, as it can be seen in Figure 4-7.

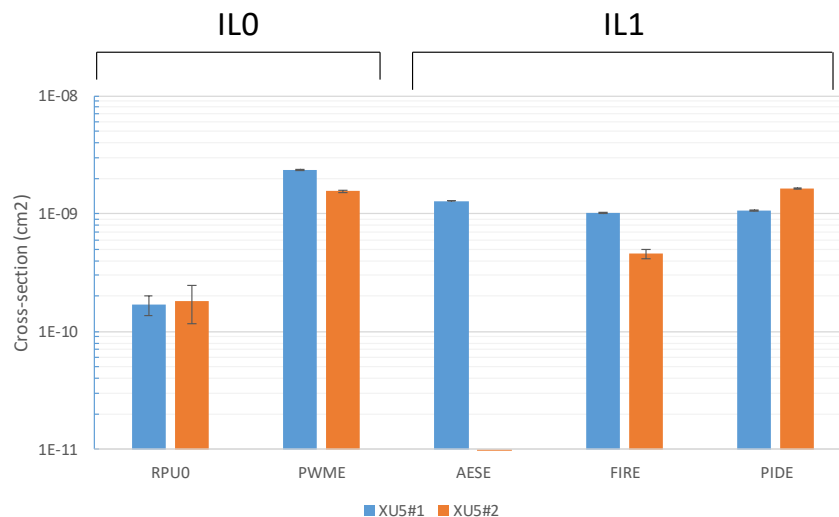


Figure 4-7. System-level events observed from two ZU+ SoM samples embedding the IL1

No synchronization error or communication between cores error was observed in the application. It is expected since the OCM was used for synchronization and no error was observed in the OCM. As only one MBU was observed on the Flash, the checksum errors were probably mostly generated by the SoC and DDR. The neutrons experiment allowed the observation of a first set of results on the control V1 and preliminary component root cause analysis by correlating system-level results with component-level results.

4.4. High energy protons experiments

4.4.1. Facility parameters

The protons experiments were performed by using the AGOR-FIRM beam line of the KVI Center of Advanced Radiation Technology (KIV-CART) facility of the University of Groningen. This beam line provides protons with energies ranging from 10 to 184MeV. The proton typical fluxes are in an order of 10^8 to 10^9 protons/cm².s and the facility delivers fluences up to 10^{13} protons/cm². For the 10cm² squared collimator used, the homogeneity is better than $\pm 10\%$.

4.4.2. Experimental setup

For the component-level and system-level experiments, the 184MeV maximum proton energy was chosen and the 10cm² collimator was used. According to SIRM simulations, those proton energies have a range of 12cm in Silicon being enough to reach the sensitive region of the component packages on the SoM. The collimator is more than enough to fully irradiate one small-form factor SoM (ZX5 and XU5), thus two ZX5 SoMs were irradiated during the Z7 experiments. For the ZU+ experiments only one XU5 SoM was irradiated at once. The Z7 beam layout, and Z7 and ZU+ experiment pictures are presented in Figure 4-8.

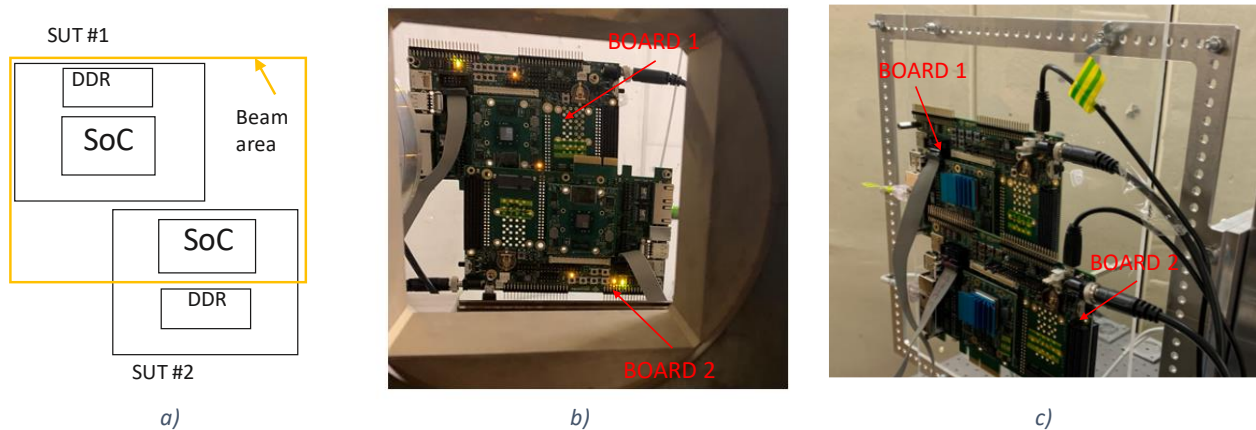


Figure 4-8. KVI-CART experiments. a) Z7 beam layout b) Z7 experiment picture c) ZU+ experiment picture (only one board was tested)

A generic experimental schematic for both Z7 and ZU+ protons experiments at KVI-CART is presented in Figure 4-9.

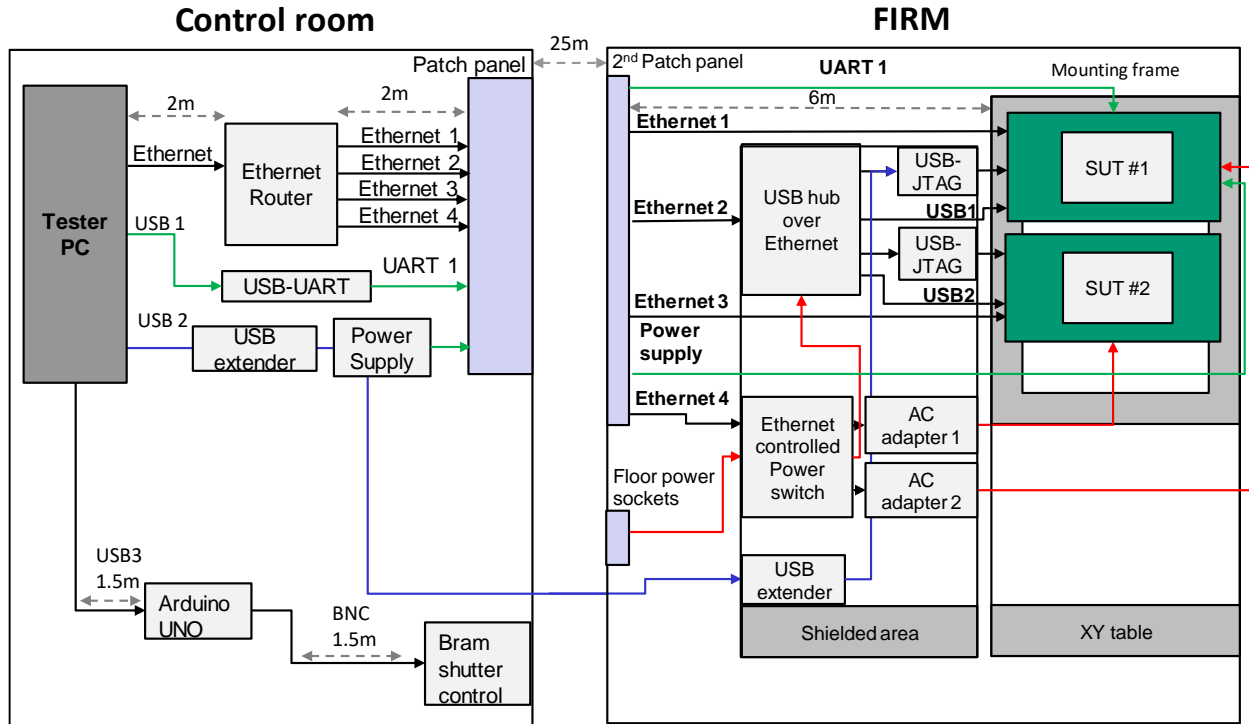


Figure 4-9. KVI-CART experiment schematic for the Z7 and ZU+ experiments

For both Z7 and ZU+ experiments, an Ethernet router was used to provide IP addresses and communicate the user PC (Tester PC) and the different experimental setup equipment in the irradiation area (FIRM) such USB hub over Ethernet and an Ethernet-controlled power switch. For the UART communications in the Z7 experiments, two USB active extensions (blue lines) were laid on the floor until the FIRM facility, then another USB A –USB micro cable was connected to the boards. Regarding the ZU+ experiment, an USB-UART cable was connected from the user PC to the patch panel and then connected to UART pins instead of the USB micro connector.

For both experiments an Ethernet controlled power switch was used to power cycle the boards, however in the middle of the ZU+ experiment, it stopped working. Thus, a power supply was connected to the patch panel BNC connectors and then directly connected to the board power supply inputs. The JTAG communication for the Z7 experiments was performed by using USB-JTAG cables connected to USB hub over Ethernet. For the ZU+ JTAG communication, a USB-JTAG cable was connected to an USB extension. And finally, for controlling the beam, a microcontroller, which was connected to the user PC by an USB port, was used to send 5V TTL signals for opening and closing the shutter.

4.4.3. Test methodology

The objective of this experiment was to obtain system-level and component-level SEE proton data for two different technologies in order to develop and validate the bridging methodology. Therefore, system-level experiments on the Z7 control-loop application and component-level experiments on the OCM and DDR3 memories were carried out in the Z7 SoM. In the Z7 system-level experiments, the DDR3 of one of the SoMs was out of the beam field so that its influence at system-level can be analyzed. Regarding the ZU+ experiments,

only one SoM running the control-loop application was characterized at a time. A summary of test logs of the KVI-CART experiments performed in June 2019 and November 2019 are presented in Table 4-9.

Table 4-9. Summary of KVI-CART experiment test logs

Date	Beam RUN #	Energy (MeV)	LET(Si) (MeV/cm2/mg)	Average Flux (p/cm2/s)	Desired fluence per run (p/cm2)	Minimum fluence reached (p/cm2)	Average fluence reached (p/cm2)	Maximum fluence reached (p/cm2)
Jun-19	7	184	3.7-3.9E-03	1-3.00E+06	1.00E+10	5.98E+08	2.77E+09	7.20E+09
Nov-19	3			3.00E+06		2.84E+09	8.08E+09	1.79E+10

Detailed test logs of the KVI-CART experiments are presented in Table A-4 and Table A-3 of the appendix.

Different from the neutrons experiments, the boards were not power cycled and reprogrammed manually and rather a Python script was used to automate this process. Thus, if no information is sent by the UART after about 15 seconds, the SoC is reconfigured to try to correct the problem. If the reconfiguration does not correct the error, a power cycle is performed by the script. Two proton campaigns were performed, therefore, the Python control script, the control-loop application and the code instrumentation were improved. In the June experiment, the beam controlling was not implemented leading to a high number of reconfigurations attempts to make the board works. This is probably due to the fact that errors in the configuration bits and in the executable application can occur during the reconfigurations when the beam is on. Thus, this feature was introduced in the November experiment. In November, the beam controlling was implemented, and the last versions of the Z7 and ZU+ control-loop applications V2 were tested.

For the June experiments, the Z7 memory test algorithm, was used to test the DDR3 and OCM memory. Both of the memories were tested simultaneously on the two different Z7 SoMs: The SoM entirely irradiated ran the DDR benchmark, and the SoM leaving the DDR3 outside of the beam was used to test the OCM. The test parameters used to test the DDR3 and the Z7 OCM are presented in Table 4-10.

Table 4-10. Z7 memory test parameters used in the KVI-CART protons experiment

	DDR3	OCM
Memory offset	0x1FFFFFF	0x0
Test size (%_	10MB (~1%)	100KB (~40%)
ECC	disabled	disabled

4.4.4. Z7 result presentation

4.4.4.1. Z7 system-level results

The extension of the control-loop system-level event acronyms observed in the higher instrumentation levels are provide in Table 4-11.

Table 4-11. Control-loop - system-level events acronyms extended

IL0		IL1		IL2	
Acronym	Description	Acronym	Description	Acronym	Description
CTRF	Control Flow Error	AESE	AES Checksum Error	FRIS	FIR Input FIFO SBU
RPU0	RPU Timeout	HAES	Hard AES SEFI	FRID	FIR Input FIFO MBU
APU0	APU Core 0 Crash	FIRE	FIR Checksum Error	FROS	FIR Output FIFO SBU
APU1	APU Core 1 Crash	HFIR	Hard FIR SEFI	FROD	FIR Output FIFO MBU
APU2	APU Core 2 Crash	PIDE	PID Checksum Error	PWIS	PWM Input FIFO SBU
APU3	APU Core 3 Crash	HPID	Hard PID SEFI	PWID	PWM Input FIFO MBU
PWME	PWM Checksum Error	DDRM	DDR MBU	PWOS	PWM Output FIFO SBU
HPWM	Hard PWM SEFI	FLAM	Flash MBU	PWOD	PWM Output FIFO MBU
				OCMS	OCM SBU
				OCMM	OCM MBU
				DAAB	Data Abort Fault
				PRAB	Prefetch Abort Fault
				UNAB	Unexpected Abort

The Z7 V1 system-level events observed in the application embedding the instrumentation level 2 are plotted in Figure 4-10.

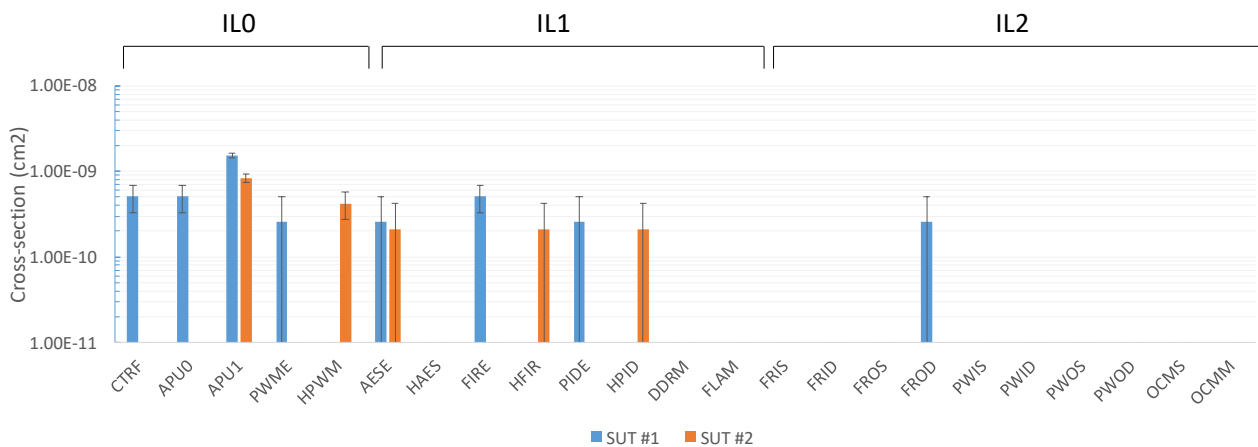


Figure 4-10. Z7 V1 system-level events when the IL2 was activated

The events were grouped by Instrumentation Levels (ILs). The SUT #1 was fully irradiated and the SUT #2 had the DDR3 out of the beam.

The application hangs (left side of Figure 4-10) were classified into application crashes (when a timeout occurs while waiting for an alive signal by the UART) and control flow errors (when the application loops in an unexpected region of the code). More application crashes and control flows were observed in the fully irradiated SUT (SUT #1) that could indicate the influence of the DDR upsets in the control flow cross-section. However, due to low number of errors, a higher fluence ($\geq 1\text{E}+10\text{ p/cm}^2$) would have to be reached to improve the statistics and confirm this conclusion.

In order to analyze SEE sensitivity impact of the IL2 and IL1 overhead, versions of the application embedding the IL1 and IL0 were tested, as it can be seen in Figure 4-11 and Figure 4-12, respectively.

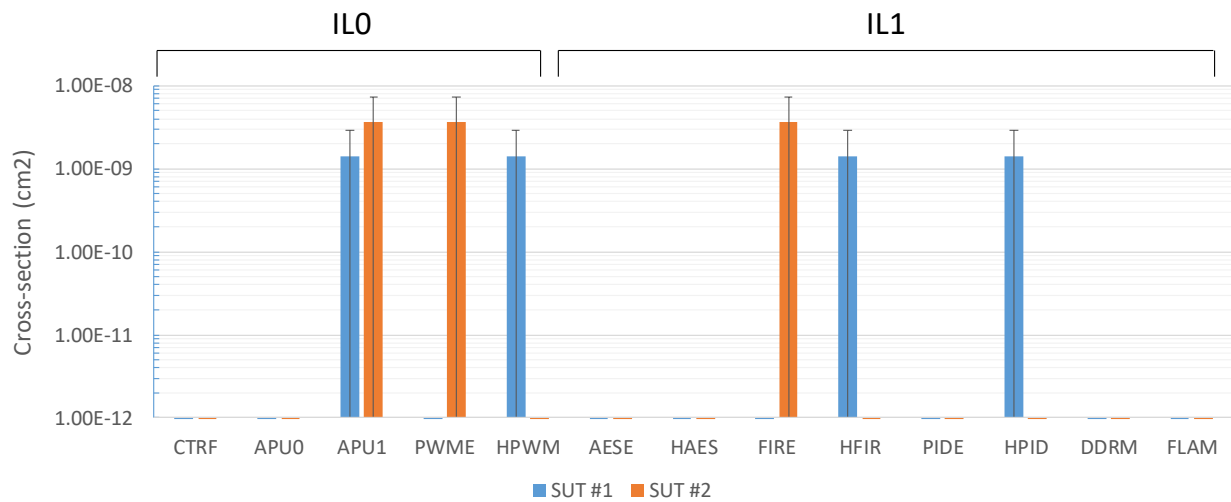


Figure 4-11. Z7 V1 system-level events when the IL1 was activated

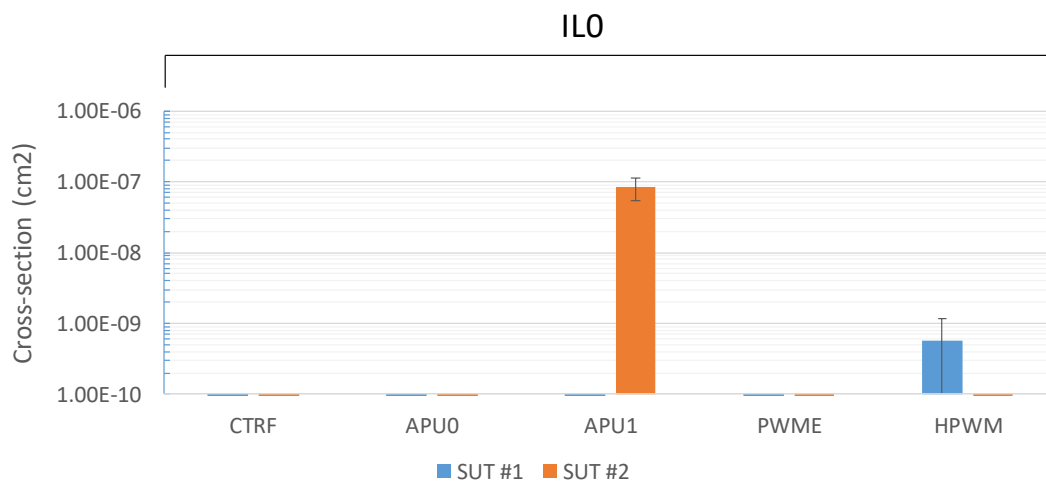


Figure 4-12. Z7 V1 system-level events when only the IL0 was activated

In general, no significant impact of the IL2 overhead was observed in the IL1 reliability. Regarding the IL1, a considerable difference was observed, however a higher error count number and fluence would be required to analyze that phenomenon.

In the November proton campaign, the Z7 control-loop V2 was irradiated where it was possible to observe additional events for a considerably smaller effective fluence ($2.07\text{E}+08$ p/cm²), as it can be seen in Figure 4-13.

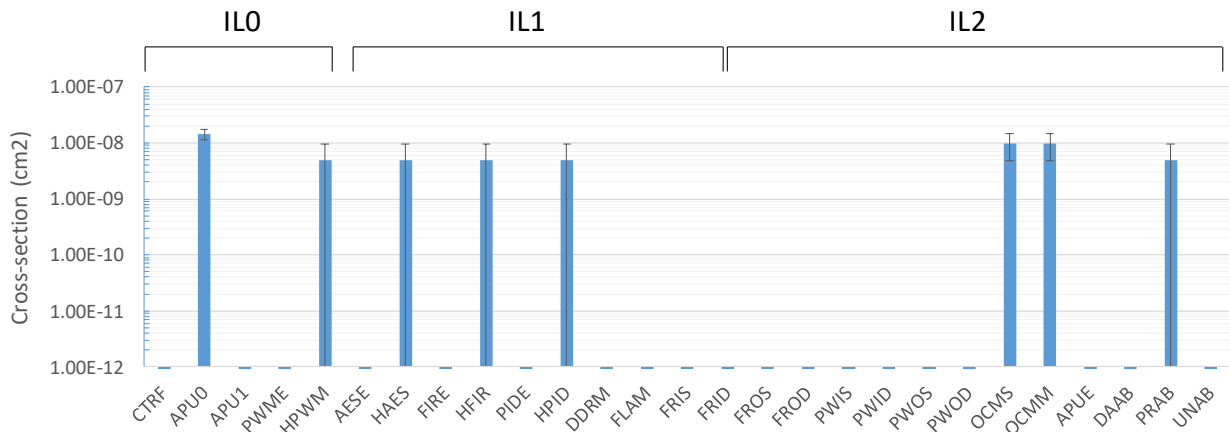


Figure 4-13. Z7 V2 system-level events when the IL2 was activated

4.4.4.2. Z7 component-level results

No events were observed on neither the DDR nor the OCM for a fluence of $4.50\text{E}+09$ and $3.78\text{E}+09$ p/cm², respectively. One possible explanation could be related to the exposure time of the DDR3 memory. As a 10MB block of memory was tested instead of the full size, the benchmark algorithm writes the block pattern and rapidly starts checking the values. Thus, the memory does not have time to accumulate observable upsets that are rather corrected in the next writing cycle. A possible solution to solve this issue would be to include a delay before the checking phase to increase the exposure time. The same applies to the OCM.

4.4.5. Z7 proton result discussion

4.4.5.1. Observability increase provided by the IL0

In the first version (V1) of the control-loop application, the application had a low error capturing capability as a small chunk size was used (500 x 32-bit words). Thus, few results with high error margins were observed making a comparison between the samples with DDR irradiated and non-irradiated, premature. In the second version (V2) of the control-loop application and instrumentation, a bigger data chunk size was used (1000 x 32-bit words) increasing the amount of data that is sent to the PL and execution time on the PS. Thus, a higher cross-section was observed even for a pretty lower fluence in the order of $1\text{E}8$ p/cm² instead of $1\text{E}9$ p/cm² reached in the V1 experiments. The IL0 features allowed essential observability regarding the proper flow of the applications and their computations.

4.4.5.2. Observability increase provided by the IL1 – V1

In the run in which the control-loop V1 embedded only the IL1 (Figure 4-11), additional computation events were observed on both SUTs. In this run, fluences reached on the SUT #1 and SUT #2 are at the same order ($1\text{E}8$ p/cm²) but the number of events observed are too low to be considered in a statistical analysis. As the computations on the control-loop are performed successively, it was possible to observe different phenomena on the SUTs. On the hard SEFI checksum observed on the SUT #1, the error happened first on the FIR computation and then was propagated to the PID computation and finally to the PWM. Whereas, on the SUT

#2, a checksum error occurred first on the FIR filter, then was masked on the PID computation and happened again on the PWM computation. That could be caused by two successive errors on the same computation loop.

4.4.5.3. Observability increase provided by the IL2 – V1

As the highest fluence was reached on the control-loop V1 application embedding the IL2 (Figure 4-10), rarer events could be observed. Thanks to that IL, a MBU on the Output FIR FIFO was observed on the SUT #1 and propagated to the PS as a Hard FIR checksum error. This observability increase helps in the root cause component analysis. Additionally, it was possible to observe two different control flow errors on the SUT #1 thanks to the IL0, where the application did not crash but was running in an undesirable region of the code. It happened on the APU core 0 and APU core 1. As this phenomenon happened only on the SUT #1, and the fluences are relatively at the same order, this could be related to upsets on the instruction code stored on the DDR.

4.4.5.4. Observability increase provided by the IL2 – V2

Finally, in the run by which the SoC embedded the IL2 (Figure 4-13), it was possible to observe additional events such as MBUs on the OCM and Prefetch aborts. Note that no memory MBUs (Flash and DDR) were detected by the control-loop V1 IL1 and control-loop V1 IL2. A low MBU cross-section is expected on the Flash due to its floating gate [BPFT17] but a high DDR MBU cross-section is expected, according to the literature, due to its lower critical charge [KOG12]. Thus, the errors were not probably detected due to the way the ECC registers were checked. In order to avoid a higher overhead, the Flash and DDR ECC registers were only checked when a checksum error occurs. Thus, it decreased the error capturing capability as few checksum errors were observed. However, the OCM MBU Parity errors trigger an interruption that is independent of the occurrence of checksum errors. Moreover, in this version of the application, a higher data chunk size was used, increasing the number of data being encoded on the OCM and being read during the execution. It increases the exposition of the OCM. The DDR controller also have a built-in mechanism to trigger interruptions. However, as that memory would trigger a high number of interruptions, the overhead of that instrumentation would have to be taken into account.

The detected Prefetch abort on the control-loop V2 IL2 also helped on identifying the application crashes that happened in the V1 (Figure 4-10), since unhandled exceptions cause application crashes. The contribution of unhandled exceptions could be the reason why the applications crashes were the most observed events on the control-loop V1 runs.

Regarding the impact of the ILs on the error capturing capability, it is possible to note that the that a higher hard PWM cross-section was observed on the control-loop V1 – IL1(Figure 4-11) than in the control-loop V1 – IL0 (Figure 4-10). However, only one event was observed in each run. Thus, a higher number of events should be observed in order to statistically analyze the instrumentation overhead impact.

4.4.6. ZU+ result presentation

4.4.6.1. ZU+ system-level results

The ZU+ V2 system-level events observed in the RUN 1 and RUN2 are plotted in Figure 4-14.

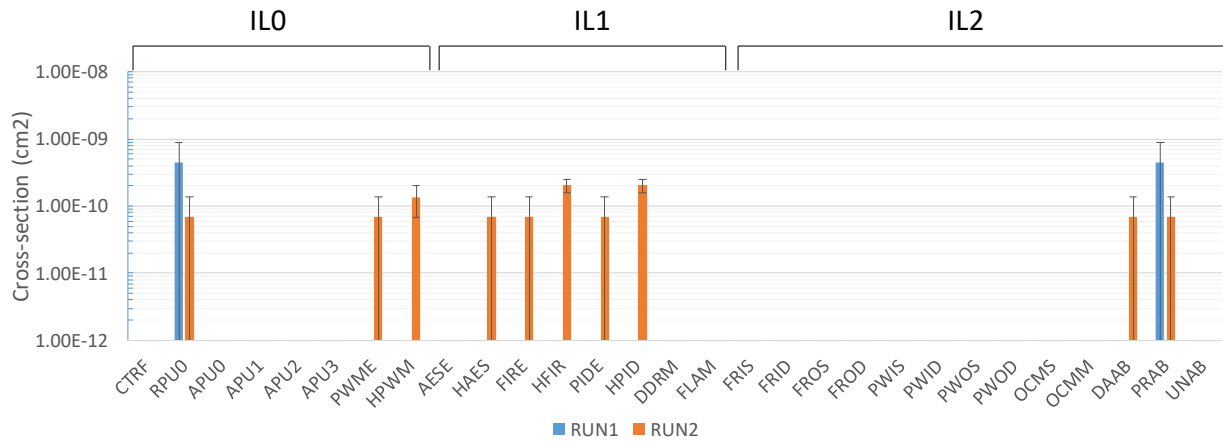


Figure 4-14. ZU+ V2 system-levels events observed when the IL2 was embedded (RUN 1 and RUN2)

As the ZU+ SoCs have two different Processing Units (RPU and APU), the application hangs were separated in the following events: RPU and APU Core 0-3 (C-3) timeouts (application crashes) and control flow errors (CTRF). In the RUN 1, no event was observed except one RPU timeout and one Prefetch Abort. Prefetch Aborts are generated when there is an issue when decoding an instruction in the processor. The module stopped sending information after 10 power cycles when a fluence of $2.84\text{E}+09 \text{ p/cm}^2$ was reached, indicating a hard failure that was confirmed posteriorly by entering the irradiation hall and checking the board.

Regarding RUN 2, an adequate fluence was reached ($1.79\text{E}+10 \text{ p/cm}^2$), however a low number of events were observed. Only one RPU timeout was observed and neither control flow error nor timeout was observed in any core of the APU. In this version of the application, abort exceptions handlers were implemented, thus instead of being reported as timeouts, application hangs were observed as Data Aborts and Prefetch Aborts. Different Hard SEFIs and checksum errors observed for the different intermediate steps (AES, PID, FIR and PWM) could represent the different sensitivity of the applications running in each core, or the influence of upsets in the PL. Regarding memory upsets (DDR4, OCM and Flash), no event was observed when the checksum mismatches occurred.

4.4.7. ZU+ proton result discussion

4.4.7.1. Observability increase provided by the IL2 – V2 sample 1

In the first run of the control-loop V2 (Figure 4-14), just a RPU application crash and Prefetch Abort were observed. Then, a hard failure, where the board was not able to power-on anymore, was observed for a relatively low fluence ($2.26\text{E}+09 \text{ p/cm}^2$) in comparison to the second run ($1.46\text{E}+10$) embedding the same application and running at the exact the same conditions. This hard failure could be related to a SEL on the DCDC converters or the ZU+ SoC, as a higher SEL cross-sections is expected for FinFET SoCs compared to planar ones [KMH18]. The difference between the fluences to a destructive failure could be related to the variability of the radiation sensitivity of the two samples (lot-to-lot variability or part-to-part variability).

4.4.7.2. Observability increase provided by the IL2 – V2 sample 2

Differently from the first run, the second sample ran for longer and events were observed with a lower cross-section. The low error count can be related to the small data chunk size used on the ZU+ experiments (500 x 64-bit words). Thanks to the IL1, it was possible to observe hard SEFI propagation from the AES computation to the PWM and from the FIR computation to the PWM. A propagation of hard FIR SEFIs to the output of the application (PWM) was observed in a higher rate than the ones starting from the FIR computation that could indicate a higher sensitivity of the resources associated to the FIR computation (PL) than the AES computation (PS). However, the errors bars are large and few events were observed. This way, a higher error count should be acquired to confirm those assumptions.

It is possible to note that neither application crashes nor control flow errors were observed on the APU cores except application crashes on the RPU. That could be related to high tolerance of the APU core or the DDR4 region used to store the code. The application crash on the RPUs could be related to a micro-SEL that was corrected by a power cycle.

No memory MBU was observed. Regarding the IL1 events (DDR4 and Flash MBUs), the absence of errors could also be related the fact that the ECC registers are only checked when a checksum error occurs, as occurred for the Z7 experiments. The absence of OCM MBUs could be related to the low data chunk size used. However, FIFO MBUs are also triggered by interruptions and are independent of the application. Thus, it could also be related to the fact the CRAM and BRAM of this technology are 50 and 2.8 times, respectively, less sensitive than the Z7 (28nm) ones, as reported in [HIE12]. One possible way of monitoring the PL of the ZU+ and Z7 experiments would be to perform bitstream readback by using the JTAG protocol. However, this operation is really time consuming (~14s for the ZU+ using Vivado in the batch mode) and its overhead should be considered when planning a digital system-level experiment on such complex SoCs.

4.5. X-ray experiments

4.5.1. Facility parameters

The X-rays experiments were performed in the IES facility. The X-ray source produces photons with energies up to 360KeV and dose rates up to 56Krad/h in a maximum field of 20 x 20 cm². The dose rates depend on the filters used, distance from the beam output, the voltage and current of the source. A measurement of the dose rates in function of the current and voltage when no filter is used is plotted in Figure 4-15.

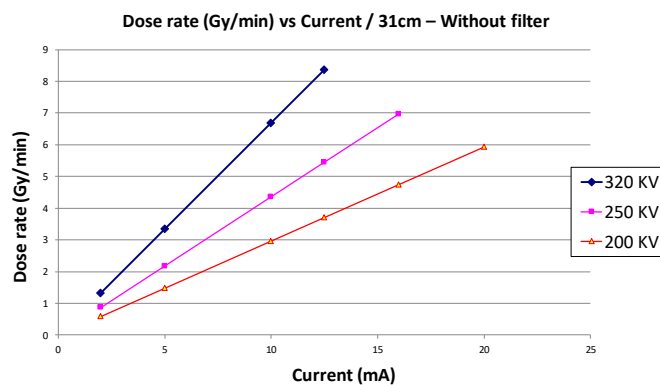


Figure 4-15. RADIAC X-ray dose rate in function of current and voltage for a distance of 31 cm from the source without filter

4.5.2. Experimental setup

As the ZU+ SoC has a 0.7mm metal lid package and the Z7 SoC is baredie, a 0.5mm Aluminum filter was used in the Z7 experiments to produce a similar dose rate and spectrum. The samples were placed 33cm far from the beam output, and a voltage of -200KV and a current 20mA were selected leading to a dose rate of 8.33 rad/s. The local irradiations were performed in the backside of the SoCs. All dose levels are given in rad (Air), i.e. not including the dose enhancement factor of X-ray in SiO₂. The experimental setup of the X-ray TID experiments is presented in Figure 4-16.

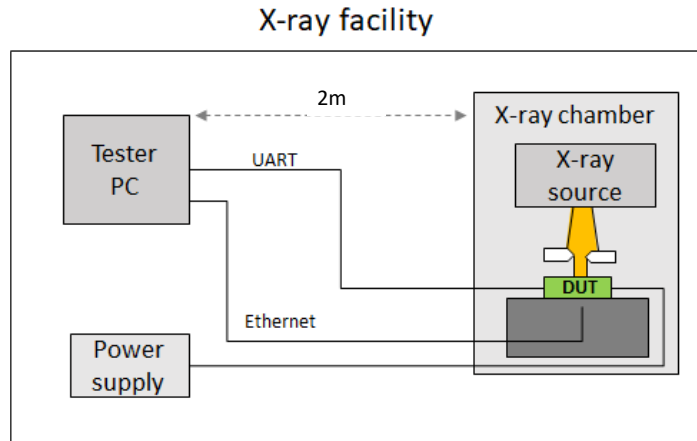


Figure 4-16. Experimental setup for the RADIAC X-ray experiment

As only one benchmark was used for the whole test campaign, JTAG reconfiguration was not required and QSPI boot mode was used instead. The Ethernet protocol was used to customize the test parameters on-the fly when required and power cycles were performed manually. In addition to the localized field size positioning, some Lead pieces were also used to shield non-DUT components of the SoM.

A picture showing the focused X-ray field position on the PL of the Z7 SoC is presented in Figure 4-17.



Figure 4-17. Picture of the Z7 board placed under the X-ray beam. The light indicates where the X-ray field will be positioned. The shielding led was not present in the picture and the Z-axis distance was increased so that the picture could be taken.

4.5.3. Test methodology

The objective of the X-ray TID experiments was to understand the timing degradation of the SoC PL configurable structures. By understanding how those structures degrade, it is possible to analyze its effect at system-level using a bottom-up approach. The timing degradations were measured by implementing Ring Oscillator (RO) test structures. This way, the timing degradations can be obtained by measuring the frequency drift of the ROs. However, the frequency drift does not only depend on the ionizing effects but also on the temperature variations and short-term BTI and HCI effects. Therefore, different groups of ROs were implemented so that only one group is irradiated and the other group suffers only the effect of the temperature and short-term aging. The floor plan of the RO test structures and the local irradiation schematic are presented in Figure 4-18.

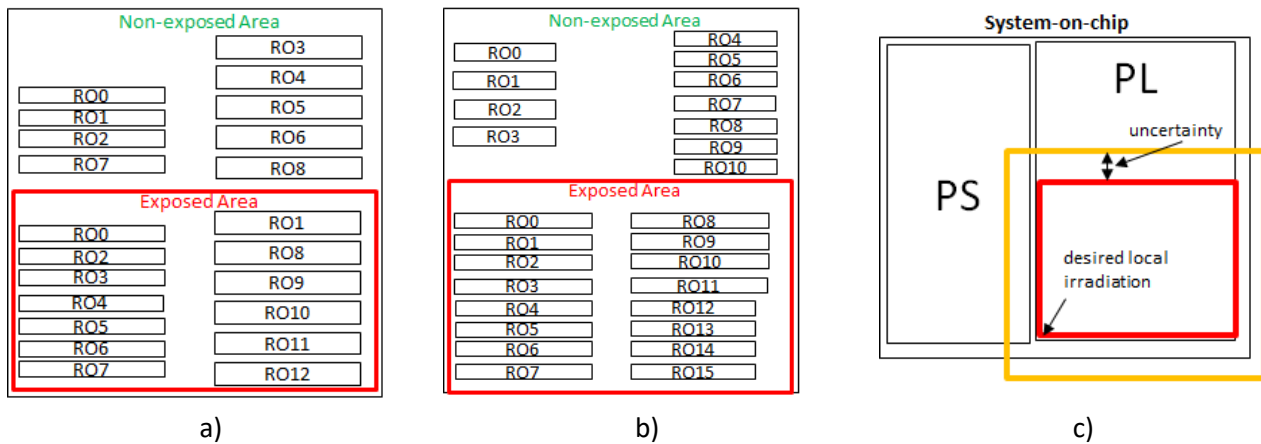


Figure 4-18. Floor plan showing two sets of rectangular RO test structures for the a) Z7 and b) ZU+ SoCs. c) Local irradiation SoC schematic (Generalized for both SoCs).

The irradiation window was defined using a beam collimator to expose only the bottom set of ROs to X-rays while leaving the top set out of the beam. In the following, those sets are designated by exposed and non-exposed, respectively. As it can be seen in Figure 4-18 c), there is an uncertainty on the irradiated area due to positioning errors and beam diffraction on the edges of the collimator.

The parameters of the implemented RO structures are summarized in Table 4-12.

Table 4-12. Structures under test

DUT	# exposed ROs	# gates per RO	Initial Frequency at 78°C (kHz)	Bus clock frequency (MHz)
Z7	16	3000	[552.7,578.1]	100
ZU+	13	1500	[1951.6,2003.0]	50

The period for monitoring the RO counters is 4 seconds, and the half of the RO frequency is defined by the rising edge counter increment divided by this measurement period. On-chip temperature measurements are performed using the embedded PL System Monitor sensor located in the non-exposed region. Before starting irradiation, a dry-run is performed, in which DUTs are supplied and operated for at least 20min until they warm-up from the room temperature to a stable operating temperature. The ROs frequencies are monitored during this warm-up phase to extract their frequency relationship with the chip temperature.

Due to the absence of heatsink on the ZU+ SoC backside, the initial stabilized temperature is relatively high, in the range of 80°C. Considering the temperature increase observed during irradiation, a fan is activated in

the vicinity of the DUTs when reaching 150krad to improve air cooling, leading to a reduction of the operating temperature by approximately 30°C and 50°C, for the Z7 and ZU+, respectively.

The irradiation campaign is a succession of 10krad steps (20min), each step followed by a 10min break, during which the DUTs are continuously supplied. Steps are spread over three days and irradiation is stopped overnight, with the DUTs being left unbiased at room temperature. Irradiation is finally stopped when a failure is first observed in the form of an interruption of the measurement reports or until the end of the available beam time.

4.5.4. Results presentation

4.5.4.1. Junction temperature and frequency drift results

Typical raw measurements of RO frequency drifts as a function of TID are presented in Figure 4-19 and Figure 4-20, respectively for the Z7 and the ZU+.

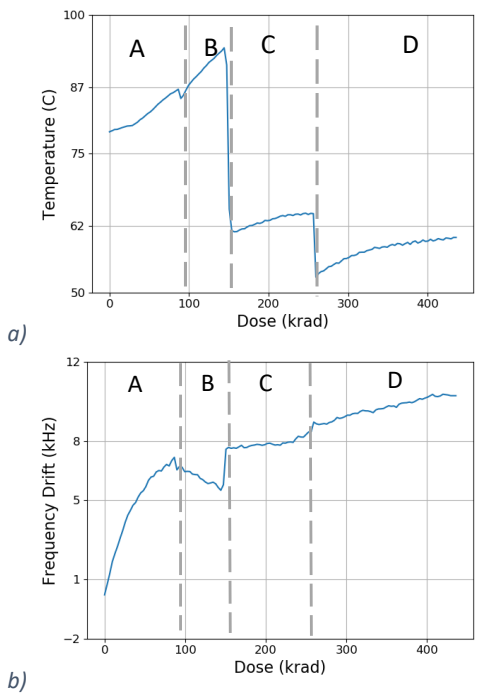


Figure 4-19. a) Z7 temperature profile during irradiation and b) Z7 typical exposed-RO frequency drift vs dose. Vertical dashed lines represent overnight breaks or fan activation at 150krad

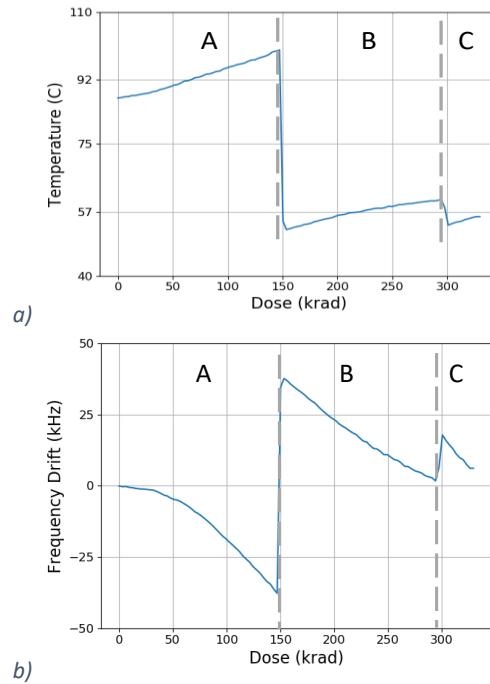


Figure 4-20. a) ZU+ temperature profile during irradiation and b) ZU+ typical exposed-RO frequency drift vs dose. Vertical dashed lines represent overnight breaks and. Air cooling activation at 150krad

First failures are observed at 340krad for the ZU+ and no failures were for the Z7 until the irradiation stops at 430krad.

4.5.4.2. TID influence on frequency and temperature

From Equation 3-3, the instantaneous frequency f of each RO can be defined as the inverse of the sum of the commutation time of each gate (τ_j) plus a propagation time ($\tau_{routing}$) corresponding to the routing delay between each gate and the feedback loop from the last gate to the first one.

Each measured frequency is, obviously, a function of temperature. We assume that the frequency drift that we measure at a given dose D and junction temperature T_j can be decomposed as the sum of two contributions given by:

$$\Delta f_{meas}(T_j, D) = \Delta f_T(T_j) + \Delta f_{TID}(T_j, D) \quad 4-1$$

The first term corresponds to the effect of temperature in the absence of radiation and is extracted by fitting the warm-up phase measurements for each RO. Indeed, an accurate modelling of the influence of temperature on the gates and routing delays would require a high level of details on the circuit's design that the author don't have access to. For the ZU+, the relationship was found to be very linear while a second order fit was required for the Z7. Table 4-13 summarizes the average temperature coefficients defined by:

$$\Delta f_{T,i}(T_j) = a_i T_j^2 + b_i T_j + c_i \quad 4-2$$

Table 4-13. Ring oscillators average temperature coefficients

DUT	a (kHz/°C ²)	b (kHz/°C)	c (kHz)
Z7	-0.0036	0.41	-11.5
ZU+	0	-1.19	0

The second term of Eq. 4-1 is due to the delays variation induced by TID measured at the current temperature T_j . It can be extracted from the temperature measurements using Eq. 4-2. As the gate thickness of the current technologies including 28nm Planar and 16nm FinFET is so thin (<2nm), the major contribution of the TID is the trap generation in the thick oxides of the device such as STI. The TID impact on the delay and temperature will depend on the technology, and the clock paths from the source to the gates that will be described in the next section.

4.5.4.3. Z7 exposed frequency drifts

The Z7 degradation patterns can be grouped into 4 groups, as plotted in Figure 4-21.a.

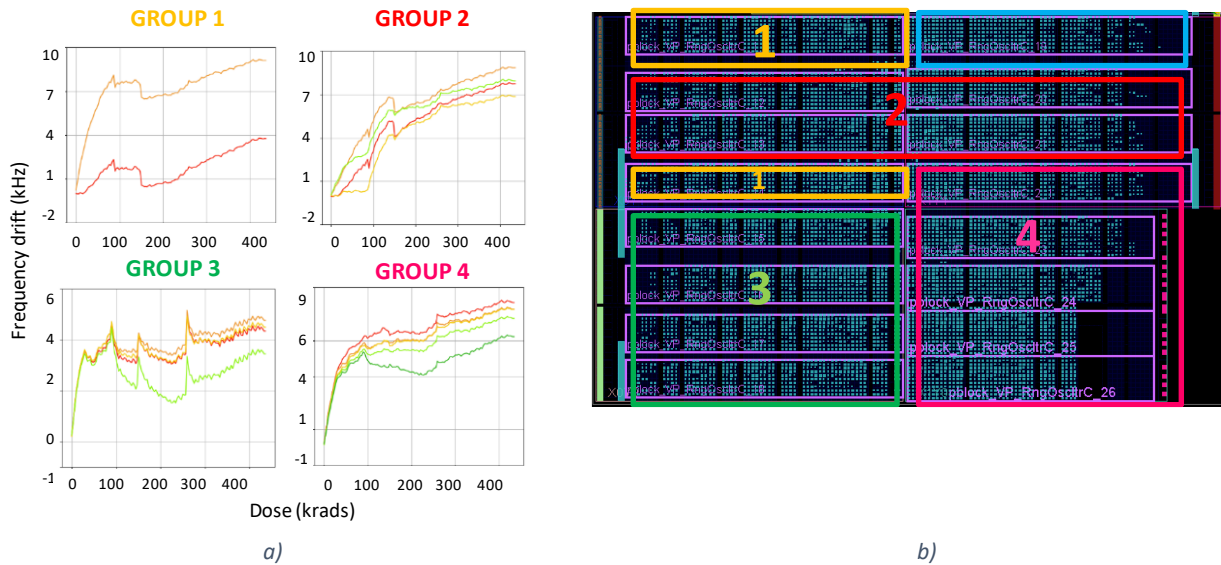


Figure 4-21. Z7 RO drifts. a) RO frequency drifts versus dose for which group b) Floor plan outlining the different groups and the RO8

The degradation patterns are associated to the place where the RO test structures were implemented on the PL, as outlined with colors associated to the groups in Figure 4-21.b. Only one RO do not belong to any group being outlined in blue.

First, the RO drifts of all the groups started to increase at different rates. Then, depending on the group, the RO drifts started to decrease, got stabilized or continued to increase. In general, the RO test structures that were placed on the bottom and top edge were less degraded by the radiation where the RO placed on the center were more degraded. It is possible to observe that the RO frequencies from the groups 3 and 4 follow a similar trend. The RO of both groups have a gradient of drifts starting from the ROs implemented on the top until the ones implemented on the bottom. However, the RO drifts from the group 3 are more sensitive to temperature variations while the RO drifts from group 4 are almost continuous.

A plot of both non-exposed and exposed Z7 RO frequency drifts is presented in Figure 4-22.

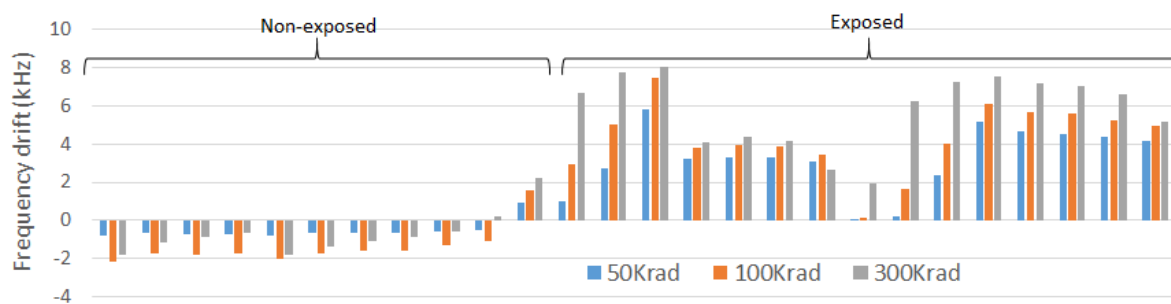


Figure 4-22. Z7 RO frequency drifts for all ROs at three dose levels

As it can be seen in the plot, the non-exposed RO frequencies decreased and then started to increase as the accumulated dose increased while the frequency of the exposed RO always increased. It was also possible to note that the last non-exposed RO that was implemented closely to the exposed region underwent positive drift. Regarding the exposed ROs, it is possible to observe two different groups with similar characteristics. Those groups correspond to ROs implemented on the left and right side of the PL. It is also possible to note, in both groups, that the degradations were higher in the test structures implemented on the center and then decrease when the RO get farther from the center.

4.5.4.4. ZU+ exposed frequency drifts

The exposed ZU+ RO frequency drifts degradations were classified into two groups. The group of RO test structures implemented on the left and right side of the PL. The TID-induced frequency drifts and the floor plan of the test structures from the two groups are presented in Figure 4-23.

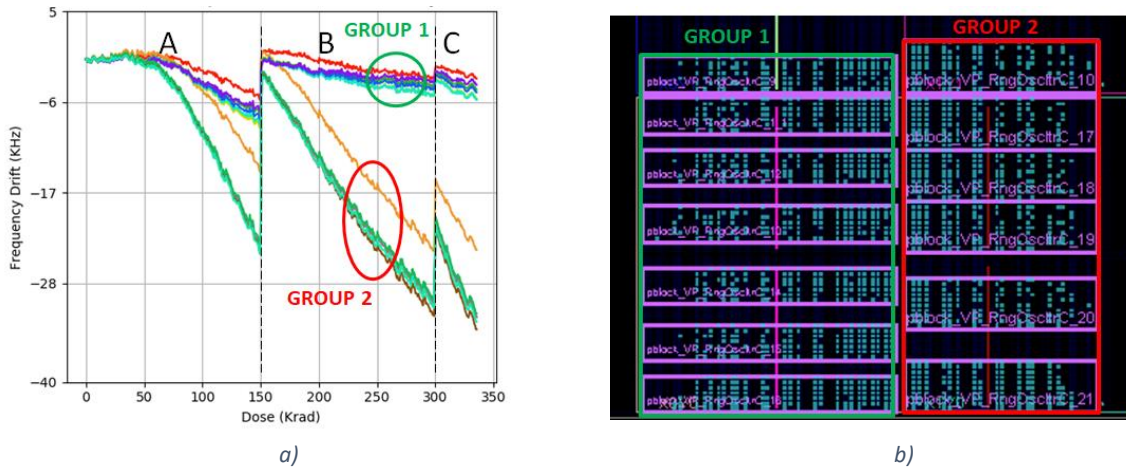


Figure 4-23. ZU+ RO drifts. a) RO frequency drifts versus dose b) Position of the RO test structures on the SoC

As it can be seen on the plot, in the first day, the RO drifts slightly increased and then started to decrease at different rates depending on the group. The RO drifts from the group 1 decreased with dose at a low rate while the ones from the group 2 strongly decreased with the dose. After the first overnight annealing (time frame B), the RO frequencies from the group 1 were almost fully recovered, then started decreasing at lower rate compared to first day. Finally, in the last day (time frame C), the RO frits from the group 1 decreased at a higher rate than the day 2.

Regarding the ROs from the group 2, it is possible to note that one of the test structures (orange curve) has a drift offset compared to the others, this test structure was implemented on the top of the group 2. The same can be observed in one test structure from the group 1 (red curve), this test structure was also implemented on the top of the group 1. Apart those peculiarities, the variance of the RO drifts within each group are pretty small in the first day. The group 2 RO frequencies were also so strongly recovered after the first overnight annealing (time frame B), and then start decreasing at approximately similar rate than the first day. However, it is possible to note that the variance within the group is increased. In the last day (time frame C), after the second overnight annealing, it is possible to note that the group 2 RO frequencies recovery is much slower than the first annealing, and then the RO drifts start to decrease at higher rate. After accumulating a dose of 340krad, the benchmark application software stopped sending the measurements by the UART. The failure was not recovered after few power cycles characterizing a hard failure.

4.5.4.5. ZU+ non-exposed vs exposed drifts

The RO drifts for both non-exposed and exposed ROs at 3 different doses are plotted in Figure 4-24.

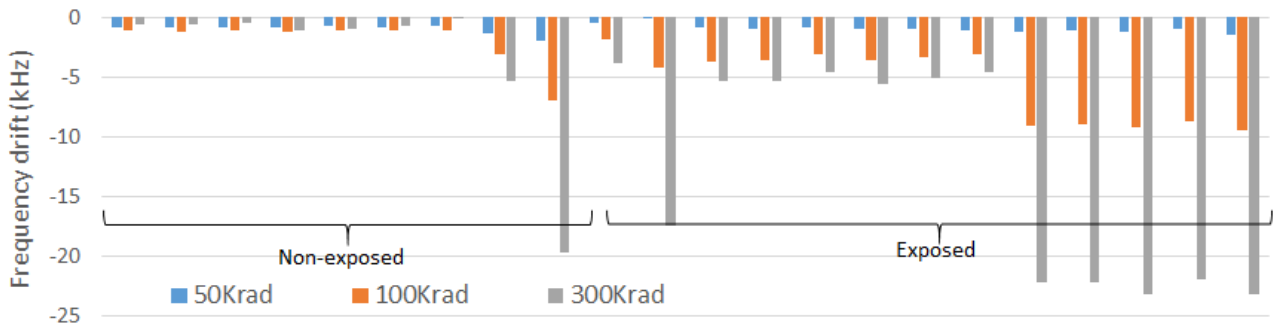


Figure 4-24. ZU+ RO frequency drifts for all ROs at three dose levels

It is possible to note in the plot that the RO frequencies were initially decreased for both non-exposed and exposed ROs, and then, after a given dose, the non-exposed RO frequencies started to increase. It is also possible to note that two non-exposed ROs close to the exposed region underwent negative drifts at rates similar to the exposed ones. Regarding the exposed RO drifts, the two groups can be separated by the magnitude of frequency drift. The exposed ROs implemented from the group 1 reached a frequency drift of about -5KHz while the exposed ROs from the group 2 reached a frequency drift lower than about -17KHz.

4.5.4.6. Z7 vs ZU+ worst case delay variation

A comparison between the worst case of the average delay variation from Z7 and ZU+ exposed ROs are plotted in Figure 4-25.

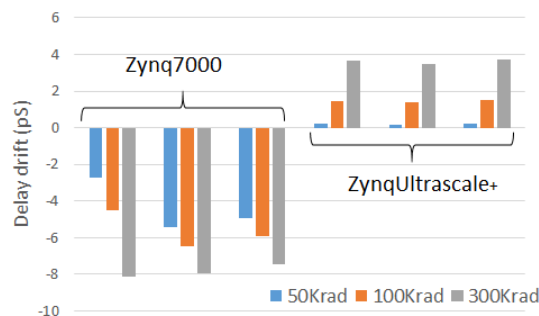


Figure 4-25. Worst cases of the average delay variation per gate at 3 TID level for Z7

It possible to note in the plot that the gate delays degraded in opposite direction for each technology and the magnitude of the delay drift of the Z7 gates was about twice the magnitude of the ZU+ ones.

4.5.5. TID results analysis

As previously presented, the frequency of the exposed Z7 ROs increased while the frequency of the ZU+ ROs decreased. However, a frequency increase due to TID is not expected. A possible explanation for that would be a degradation of the PL clock or PS clock making the impression that frequency is increasing. The difference between the two technologies could be explained by the positions where the PL clock is

generated and where the clock sources (MMCM) were placed. The clock generation and clock source positions on the two technologies are presented in Figure 4-26.

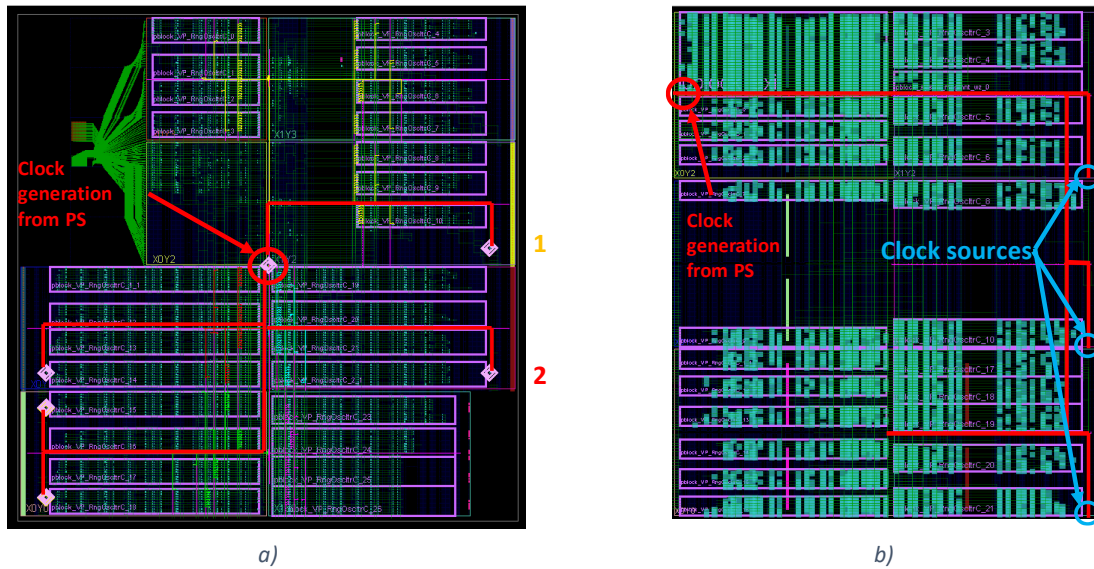


Figure 4-26. Floor plan showing the clock generation and clock source positions a) Zynq7000 SoC. b) ZynqUltrascale+ SoC

As it is possible to see in Figure 4-26.a, the Z7 PL clock is generated in the middle of the chip, while ZU+ PL clock is generated in the top left corner in the non-exposed regions. That could explain the degradation of the Z7 PL clock. Additional localized TID experiments would be required to confirm that assumption.

4.6. Laser experiments

4.6.1. Facility parameters

The Laser experiments were conducted in the Single Photon Absorption (SPA) IES facility. The facility produces laser pulses with a wavelength of 1064nm and a pulse width of 30ps focused in a spot size of 1μm by using a 100x lens. The laser pulse energy can be configured up to 50nJ depending on the required SEE event to be observed. For scanning the DUT, the motorized XY stages can move in a range of 50mm x 50mm and the motorized Z stage have a range 50mm. The spatial distribution of the charge generated by a SPA laser pulse is plotted in Figure 4-27 [POUG14].

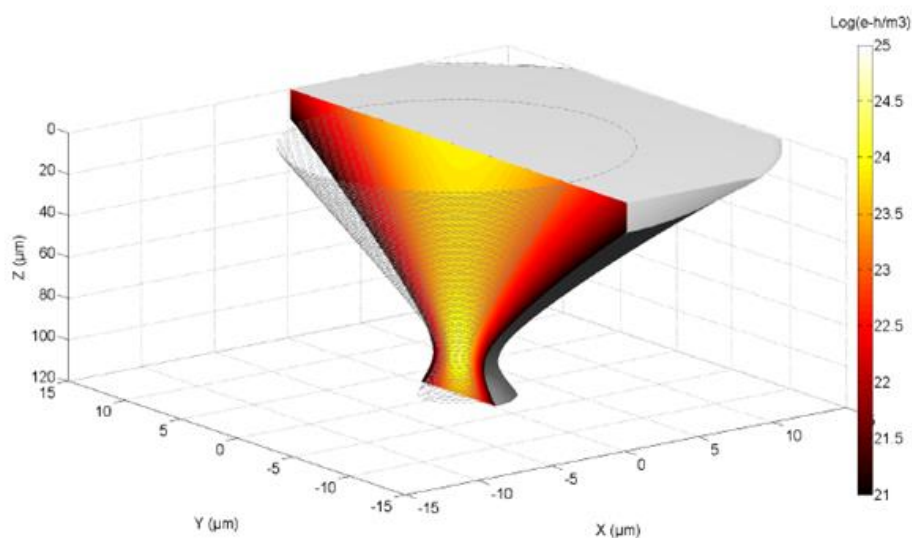


Figure 4-27. Spatial distribution of the laser induced charge through 100μm of silicon at 1064nm with a pulse energy of 1nJ [POUG14].

4.6.2. Experimental setup

Laser pulses with a wavelength of 1064nm have a penetration depth close to 1mm in Silicon. Thus sample preparation is not required for reaching the sensitive regions of the bare die SoCs present on the ZX5 and XU3 SoMs. As the DUT metal layers shield the laser pulses, the samples have to be irradiated through the backside. The packages of the bare die SoCs are flip-chip, so the modules are irradiated from the top without requiring a hole on the PCB. A schematic of the laser experimental setup is presented in Figure 4-28.

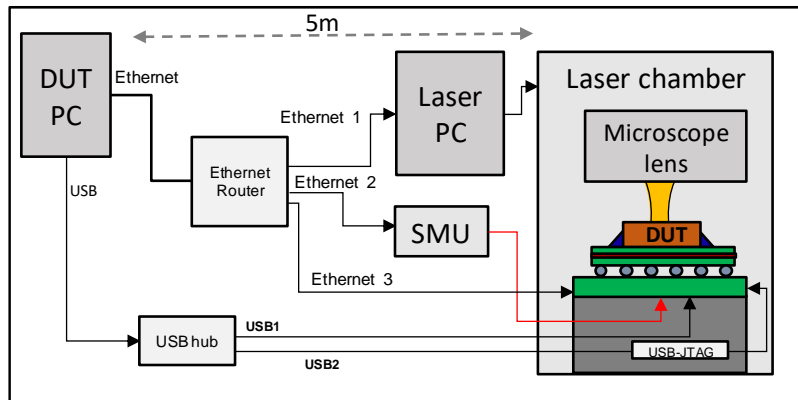


Figure 4-28. Experimental setup schematic for the RADIAC SPA laser facility

As it can be seen in the schematic, two PCs were used: one for controlling the DUT, and another one for controlling the laser source, microscope and positioning. The Ethernet port of the DUT PC is connected to an Ethernet router so that it can communicate to the Laser PC, Source Measurement Unit (SMU) and the Ethernet port of the DUT. The SMU was connected to the power input of the CB in order to power cycle it when a SEL occurs. The Ethernet connection between the DUT PC and the DUT was used for sending commands to customize the experiment on-the-fly. One USB port of the DUT PC was used for programming the SoC and reading the system output through a USB hub. The USB1 port was connected to the USB micro connector of the board and the USB2 port was connected to a USB-JTAG converter, then to the JTAG connector of the board.

A picture of the ZX5 SoM mounted on the laser test bench is presented in Figure 4-29.

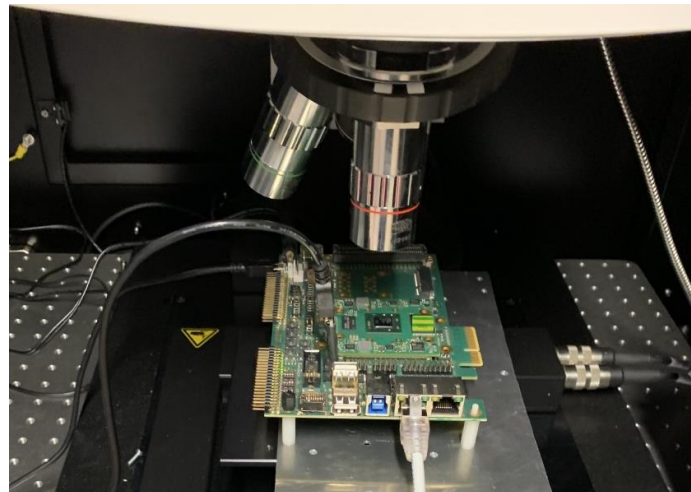


Figure 4-29. Z7 SoC mounted under the SPA laser beam

4.6.3. Test methodology

One of the objectives of the laser experiments was to better understand the proton results by injecting faults on specific resources of the system's components. In addition, the laser experiments were also used to evaluate and validate updates on the system instrumentation by verifying how the injected faults are observed.

Since the SoCs are the most complex components of the SoMs, it is worth injecting faults on specific resources of the PS and the PL. Regions of interest (ROIs) of the SoC PS are the L1 and L2 cache memories, the OCM and registers. Regarding the SoC PL, ROIs are BRAMs, CRAM and DSP used by the IP cores, and SEL sensitive regions.

The laser experiment consists in finding the threshold pulse energy required for generating one or more upsets on the ROIs and then performing automatic scans on those regions by using that energy. The threshold energies were found by manually irradiating the ROIs starting from energies of 100pJ up to 1000pJ with 50pJ steps. The triggering frequency of the laser pulses was selected to 10Hz. After finding the threshold energy, the ROIs are scanned by different scanning methods depending on the size of the ROI.

For small ROIs such as cache memories, registers, or small IP cores, the sequential scan mode was used, and for the big ROIs such as big IP cores using a lot of PL resources, the random bouncing-ball scan mode was used. An illustration of the sequential and random bouncing-ball scan modes are presented in Figure 4-30.



Figure 4-30. Laser scan modes: a) sequential b) random bouncing-ball

A summary of the Z7 and ZU+ test logs are presented in Table 4-14.

Table 4-14. Summary of Z7 and ZU+ test logs

Campaign	RUN #	Energy (pJ)	Zones	Equivalent LET(MeV/cm)	Target Pulses #/run	Minimum pulses #/run	Maximum pulses #/run
Z7 SoC	20	189-275	PS and PL	19-29	50000	20400	425142
ZU+ SoC	17	276-310	PS and PL	29-32	50000	6872	284733

The detailed test logs of the Z7 and ZU+ experiments are provided in Table A-5 and Table A-6 of the appendix.

The zones irradiated in the Z7 experiment are presented in Figure 4-31.

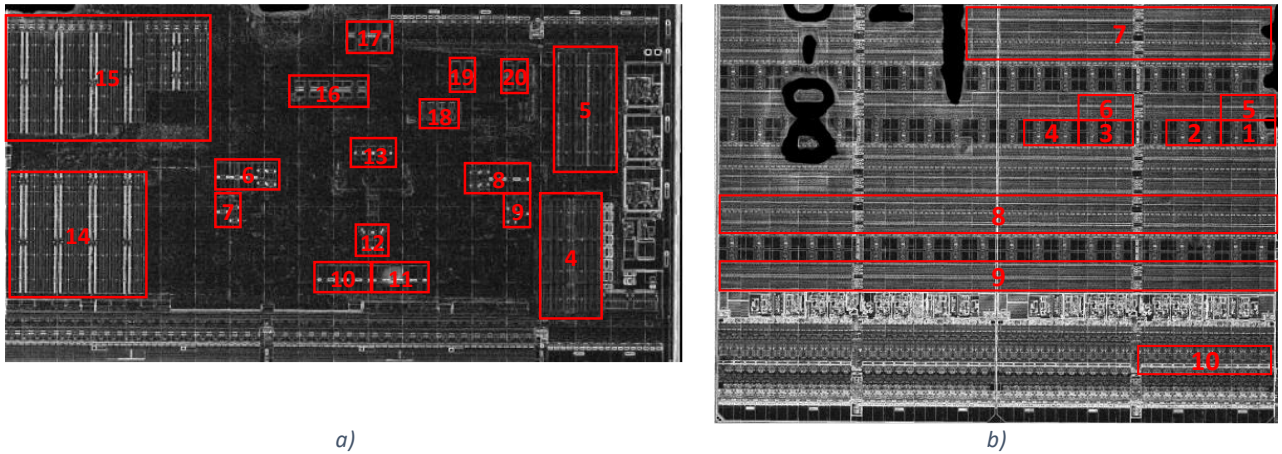


Figure 4-31. Microphotograph of the Z7 SoC a) PS and b) PL zones

As the objective of the laser experiments was to better understand the KVI-CART proton results, the control-loop software and firmware used for the protons experiments was used and slightly modified. Temperature measurement from the SoC system monitor was added to the code-instrumentation layer in order to detect SELs. Exception abort handlers were also implemented to better understand the software timeouts. Regarding the PL firmware, physical block constraints was added to concentrate the IP cores in small regions and increase the density of utilized resources. The description of the Z7 PS and PL zones are presented in Table A-7 of the appendix. All the Z7 zones were irradiated using the sequential scan mode except the big zones 7, 8 and 9.

The microphotograph of the ZU+ SoC showing the zones are presented in Figure 4-32.

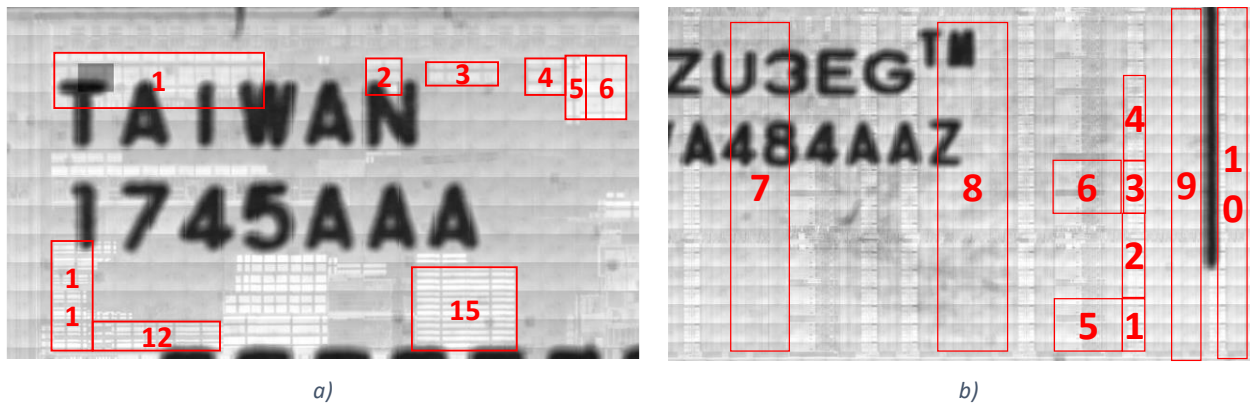


Figure 4-32. Microphotograph of the ZU+ SoC a) PS and b) PL zones

A complete definition of the ZU+ zones is provided in Table A-8 of the appendix. The same embedded application and instrumentation used in the ZU+ protons experiment was used. The physical constraints were added to limit the PL area. All the ZU+ fault injections were performed in the sequential mode except the big zones 7, 8, 9 and 10. The experiments were conducted on leadless packages without any preparation with laser engraved letters written by the manufacturer that prevented the optical access to some resources.

4.6.4. Results and discussion

4.6.4.1. Z7 correlation with proton results

A comparison of the Laser and proton Z7 results is plotted in Figure 4-33.

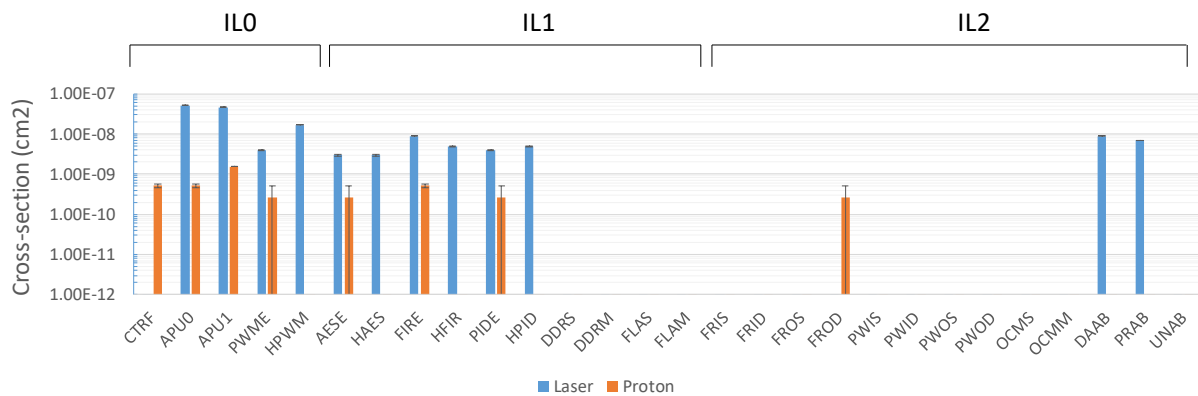


Figure 4-33. Comparison of Z7 proton and laser results.

It is possible to note in the plot that although the entire SoM was not irradiated and rather only some resources of SoC were irradiated, higher cross-sections were observed in the laser experiments than in the protons experiments. This can be related to the proton low probability ($\sim 1\text{E-}10$) of generating high LET secondaries due to nuclear interactions and the different equivalent LETs of the experiments. For a laser energy range of 189-275pJ, the equivalent LET is between 19-29 MeV/cm, while the secondaries of protons at energies around 200MeV reaches LETs up to 15 MeV/cm [HIBL03]. Thus, even higher laser cross-sections would be expected. The error counts in the proton results were considerably small leading to high error margins making a statistical analyses less precise. That difference can also indicate that the SoC is the most sensitive component on the SoM where the most sensitive resources were the FIFO BRAMs and the cache memories.

Regarding Checksum Errors, it is possible to note that a similar behavior was observed in both experiments that can indicate the fault propagation and fault masking of the application. In both experiments the FIR Checksum Error had the highest cross-section and the AES, PID and PWM Checksum Errors had a similar cross-section.

4.6.4.2. ZU+ results

A comparison of the Laser and the proton ZU+ results is plotted in Figure 4-34.

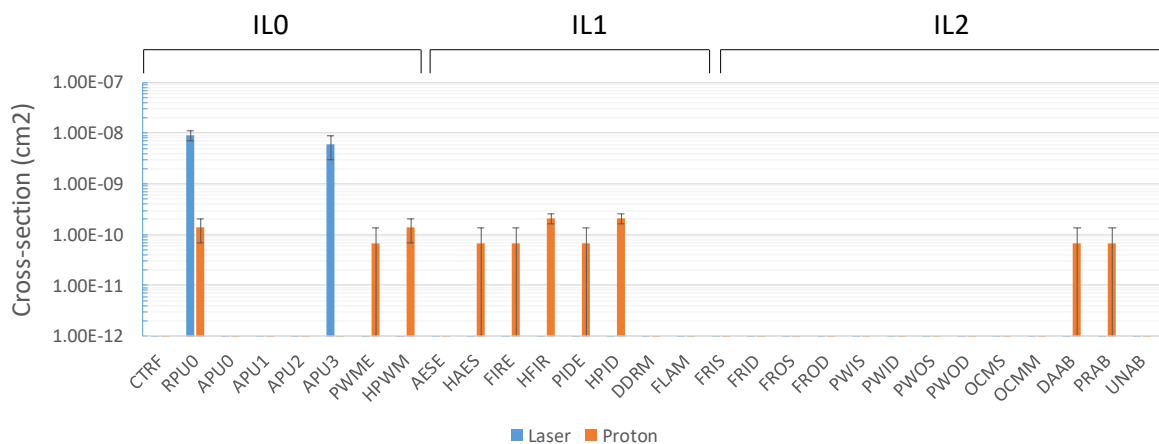


Figure 4-34. Comparison of ZU+ proton and laser results.

As for the Z7 experiments, a higher cross-section was observed in the laser experiment than in protons experiments. Similarly, the laser energy range used (276-310pJ) leads to an equivalent LET range of 29-32 MeV/cm that is higher than the maximum proton secondary LETs. In general, the ZU+ experiments had lower cross-section than the Z7 experiments that can be related to the lower ZU+ PL sensitivity [HIKB17] and the lower technology size. Regarding the laser results, not all the memories of the PS were irradiated, as performed in the Z7 experiment, due to timing constraints and the incomplete identification of the different regions of the SoC. The RPU timeouts observed when irradiating the PS can be related to some memory or registers used by RPU and the APU CPU3 Application Crash observed when irradiating the PWM FIFO BRAMs can be related to a control logic error that blocked all the PL resources until reaching the APU CPU3.

4.7. Conclusions

In this chapter, radiation experiments were carried out on the case study developed embedding the instrumentation layer. First, a prototype of the system-level application and instrumentation as well as generic memory benchmarks were initially tested with atmospheric neutrons, providing a first set of results and useful feedback on the testbench design. Then, 184MeV protons experiments on a complete version of the case study and the instrumentation were performed, including some difficulties related to the beam facility. A variety of system-level events could be observed. Successively, localized X-ray TID experiments were conducted on the Z7 and ZU+ SoC PL in order to observe timing degradation. Finally, laser fault injections were performed in order to perform resource and component root cause analysis on the SoCs.

Results on different particles at both component and system-level were obtained. This information was crucial for building and validating the proposed bridging methodology that will be discussed in the next chapter.

5. BRIDGING METHODOLOGY DISCUSSION AND PROPOSAL

The objective of this chapter is to propose a bridging RHA methodology from component to system-level and to provide some guidelines and advices to someone planning to characterize digital systems at system-level. First, some advices and tips will be provided thanks to lessons learned from the different challenges faced when characterizing the digital systems of this work. Then, the knowledge and experience obtained from the different radiation experiments will be used to propose a bridging RHA methodology. Afterwards, the proposed methodology will be applied to our case study and will be analyzed. Finally, the limitations, applicability and possible improvements of the proposed methodology will be discussed.

5.1. Guidelines and recommendations for system-level test

To perform radiation experiments on electronics is always a challenging and intensive task due to the high cost of beam times (~1000 € per hour) and technical complexity of dealing with long distance communications (up to 50m). When testing a whole digital system, the planning and execution complexity may increase. Thus, in this section, advices and recommendations will be provided supported by the different issues experienced during the system-level SEE experiments and TID experiments on complex components. The section is divided between the lessons learned when preparing a radiation experiment and executing it.

5.1.1. Experiment preparation

5.1.1.1. *Test plan definition*

A good test plan definition has an important influence on the success of a radiation campaign. A test plan has to be consistent enough so that the tester does not need to decide what should be done during the campaign but just follow the pre-defined steps. At the same time, the test plan should be flexible enough so that the tester already knows what to do when unforeseen events happen. Those unexpected events can be caused by the different situations such as:

- Beam facility problems: beam availability, beam quality...
- Early destructive failures of the SUT during the campaign
- Testbench communication issues related to the facility electromagnetic environment
- Testbench degradation during the campaign due to incomplete shielding (ex: power supplies, switches)

Therefore, those unexpected events should be anticipated so that the tester is prepared for them and can act for correcting them, mitigate them or, in the case it is not possible to correct them, decide which part of the experiment will have to be disregarded.

The elementary unit composing a test plan is commonly called a run. Defining the test plan for an irradiation campaign thus includes defining the different runs that will be executed during the campaign, either sequentially or in parallel depending on the type of facility and the test capabilities. A run definition typically includes the specific testbench parameters (sample number, frequency, benchmark used...), the required measurements and the target fluence or total dose, allowing to calculate the beam time required for the run.

To this extent, good approaches learned regarding the test preparation are:

- Defining priorities for the runs

- Having alternate test plans (A, B, C...)
- Precise estimation of the required beam time
- Calculating the accumulated dose and total fluence of samples

As an example of run prioritization for a system-level test, a run with a benchmark that exercises a memory component of an emerging technology, for which no similar results can be found in the literature, would require a higher priority than a run with a benchmark exercising a memory component of a previous generation for which results on similar parts are available. The lower priority runs would be performed only if some beam time is left.

A precise estimation of the beam time is essential for a definition of a test plan and very important due to its high cost. It should consider the mechanical mounting of the boards and communication testing. When mounting several boards in parallel, the boards usually can be moved into the beam field by using a remote-controlled table without having to enter the facility. However, this moving time and the required communication testing time should be taken into account in the estimations.

When testing FPGAs and processors, another important influence on the beam time is the reset time that can include power cycling, device configuration, and program loading. Estimating the time required for each reset should be done during the test plan preparation, using a realistic reproduction of the facility conditions, especially the cable lengths. The number of resets per run will depend on the number of SEFIs or SEL during the experiments, so it is difficult to estimate prior to the experiment. The first runs could be dedicated to estimate those numbers so that they can be used for adapting the rest of the test plan in real time during the campaign.

Once the required beam time is known, an important step is to estimate the accumulated dose of the samples along the experiment since a TID induced failure can occur. This allows estimating the number of back-up samples. A test plan with dose calculation is presented in Table 5-1.

Table 5-1. Simple test plan with dose calculation

PLAN	RUN	Proton Energy (MeV)	LET (MeV/m)	Technology	Description	Priority	Flux (n/cm ² /s)	Required fluence (n/cm ²)	Accumulated dose (rads)	Duration (s)
A	-	184	3.90E-03	A	Mechanical mounting and testing	-	3.00E+06			1800
	1				Test A	1		3.00E+10	1872	10000
					Reset time	-				900
	2				Test B	-		3.00E+10	3744	10000
					Reset Time	2				1200

5.1.1.2. Experimental setup definition

In addition to the test plan definition, the specification and test of the experimental setup is extremely important. The experimental setup should be robust in order to be able to tolerate faults and, at the same time, it should be optimized to decrease the mechanical mounting and communication test time. The major problem when defining the experimental setup is to propagate electrical signals over long distances keeping the signal integrity. The different communication protocols commonly used are:

- Long distance protocols
 - Ethernet
 - UART
- Medium distance
 - USB
- Short distance protocols
 - JTAG
 - SPI
 - I2C

Most facilities (KVI-CART, ChipIR...) have Ethernet ports and RS232 [TECH20] connectors in the patch panels. Some recent facilities include USB ports (ChipIR) and can require the use of active USB extenders. JTAG can be used for debugging and programming digital systems at lower speeds (up to Mbps) and short distances (up to few meters). JTAG has to be converted to other protocols such as USB or their voltage levels have to be raised by level shifters in order to communicate over long distances.

Power controlling equipment such as power supplies and analyzers can usually be placed in the control room and connected to the SUT over several meters by using panel connectors. For power cycling AC ports without controlling the voltage and current, power switches can be used for digital systems. It is safer to place power switches in the irradiation area to limit the length of AC adapter cables. Power switches can then be controlled by using long distance protocols such as Ethernet.

Some facilities (KVI-CART) also offer the option of beam shutter controlling and information gathering, such as flux, by using Transistor–transistor logic (TTL) signals at low frequencies (kilohertz). A simple solution to control that is to use low-cost Microcontroller Units (MCUs) connected to the user PC by USB.

Some equipment such as a USB-hub over Ethernet can help to decrease the number of cables between the control room and the irradiation area. However, it can also add complexity to the test bench setup, for example related to drivers compatibility or shielding arrangement.

During the experiments, important equipment from the experimental setup can fail such as a USB hub or power supplies. Therefore, it is also important to have back-up communication capabilities or back-up power supplies, routers, etc. Possible sources of experimental setup failures during the experiment should be reviewed and redundancy should be provided so that the experiment campaign is successful.

5.1.1.3. Benchmarks preparation

The definition of the benchmarks has also a great impact on the success of the experiment as they define the observability of events. Thus, different versions of the benchmarks should be generated such as benchmarks with different frequencies, amount of data being processed by the software and amount of configurable resources used. It is also important to have different types of benchmarks for testing the systems because application masking can occur.

5.1.1.4. *Instrumentation validation*

The instrumentation addition to the benchmarks for improving the observability will be discussed in detail in the next sections. However, it is also important to validate the instrumentation before performing the experiments. A good way of validating the test instrumentation is to perform software-based, hardware-based or laser fault injections.

Software fault injection can be designed as a part of the instrumentation itself. Some examples are the DDR4 and OCM memory controllers of ZynqUltrascale+ technology [XILI19], which provide built-in functions for injecting faults on the memory in specific positions, making possible to validate the implementation of the built-in ECC mechanisms. Regarding FPGAs, fault injection by emulation on the bitstream can be performed using partial reconfiguration. It can be customized by sending the desired frames and commands to the Internal Configuration Access Port (ICAP) of Xilinx FPGAs [LBKS18] or using the Xilinx Soft Error Mitigation (SEM) IP-core and controlling it by software [XILI18C]. Finally, a good example of fault injection for validating SEE instrumentation is the laser fault injection on SoC resources [RFKP19]. PS resources can take time to be identified, but PL resources are more easily identified by comparing it to the Vivado floor plan.

5.1.2. *Experiment execution*

Executing radiation experiments is an intensive task demanding a lot of energy and attention. To prevent human mistakes, automation of the test procedures is required. The tester should also react fast to the experiment issues along the experiment in order to not lose beam time. Several parameters of the test plan may require real-time adjustment of the test plan.

5.1.2.1. *Improving system exposition*

Improving system exposition is required when the events of interest are not or hardly observed during the experiment. This can happen when the test cycle duration of the benchmark is too short for accumulating observable events, or when a small portion of a configurable resource (FPGA) or memory is used... Of course, in some cases, the small number of events can be due to the low sensitivity of a specific technology. When a high number of events are expected (from the literature) and not observed, different versions of the benchmark should be tested. It can be performed by different alternatives:

- Increasing the amount of data being processed by the benchmark
- Increasing the resources utilization of the benchmark

However, a flexible and automated experimental setup is required for performing those modifications on the fly. Modifications of the benchmark workload can be done online by embedding a self-test controller on the spare resources of the digital systems (e.g. spare core), which can be controlled remotely by sending commands. Nevertheless, when the self-test controller is also irradiated, its cross-section should be minimized. The alternative option is to use the JTAG protocol to upload different versions of the benchmark firmware and software prepared and tested before the campaign. Although not recommended, real-time modifications of the source code of the benchmarks may be required during the experiments. In this case, a good automation of the firmware and software generation is strongly recommended.

5.1.2.2. Improving observability

The use of a flexible instrumentation layer has been proposed for improving observability. This can be implemented in two different manners. If different instrumentation levels are added to the source code with pre-processor directives in order to reduce the code overheads, the instrumentation level can be increased by loading different versions of the compiled executable. Alternately, all the instrumentation levels can be added to the source code and the tester can change it on-the-fly during the experiments by sending commands to the self-test controller. This adaptive process should typically be done during the first runs, so that the best compromise between overhead and observability is found.

5.1.2.3. Increasing radiation levels

When there is no possibility of increasing the system exposition, an alternative might be to increase the radiation levels. A flux increase takes seconds in some facilities. However, care should be taken because a higher flux can generate artefacts, like the unrealistic accumulation of events in one test cycle, and it can prevent the system to be rebooted properly. Therefore, it is also important to control the beam, when possible, in order to only open the shutter when the board is ready and executing the test benchmark.

5.1.2.4. Improving error reporting

Once the events start to be observed, actions should be taken to correct them and classify the type of event. In order to be able to react to possible trends and disturbances, a script for processing the logs and plotting the results in real-time during the experiments is highly recommended. It includes dynamic reporting of events, temperature, currents and other measurements.

When characterizing complex digital systems, it is extremely important to implement some redundancy on events reporting and report as much information as possible. Examples of that is reporting the timestamp of events in two different levels. The timestamp can be reported by the script running in the test PC and additionally by the benchmark running inside the SoC. Thus, it is also possible to detect variations and possible degradations. Another example is logging of all the operations performed by the experimental setup equipment, such as power cycles and reconfigurations in order to facilitate the post-processing of the data.

5.2. Proposed bridging methodology from component to system-level

In this section, the building blocks of the proposed bridging methodology will be presented and discussed. First, the procedures for analyzing a digital system for identifying their critical components and the components usage will be described. Then, the process of adding instrumentation to the embedded final application and elaborating the test plan will be discussed. Afterwards, the component-level and system-level test activities and data analysis will be presented. Thereafter, a methodology for estimating the system-level reliability will be proposed. Finally, a summary of the bridging methodology will be provided by combining the presented macro blocks.

5.2.1. System analysis

The first macroblock of the bridging methodology is the system analysis as illustrated in Figure 5-1.

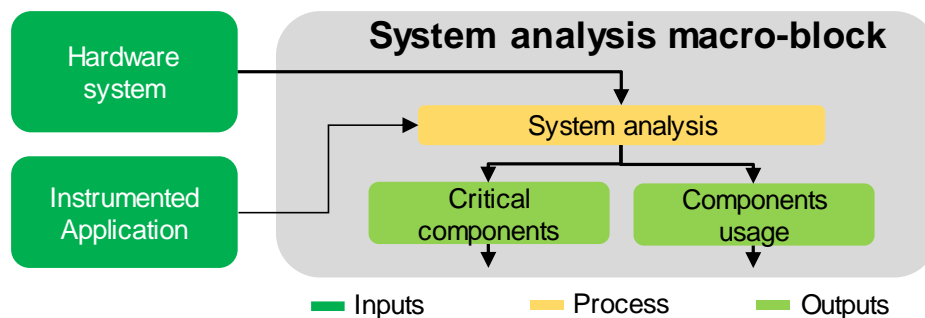


Figure 5-1. System analysis – first macro block of the bridging methodology

As it can be seen, the inputs of the systems analysis are the hardware system and the final embedded application descriptions. The hardware system includes all technical information regarding the components that compose the system and how they are interconnected. The highest level of information is the detailed system schematic, and lower levels include system block diagram, board schematics and component datasheets.

The system information will depend on the type and complexity of the target hardware system. For a Cubesat, for instance, the system block diagram would describe the different boards that compose the system such as power boards, processing boards, communication boards... Each specific board has an associated schematic. In the best case, the board manufacturer or designer provides all the connections and part numbers to the test engineer. In some cases, some important information is not provided in freely accessible schematics, due to intellectual property reasons. In such case, visual and electrical inspection of the boards may provide additional information such as components part numbers or voltage levels. Once a part number is known and the datasheet is available, technical information can be retrieved and analyzed such as electrical parameters and modes of operation, as well as technology and reliability information, when available.

Description of the embedded application includes the firmware, the software, the data and the documentation required for customizing the hardware system in order to perform the desired system functionality. The elements of this description are:

- Functional specification: defines the system as a black-box, i.e. the required inputs and the expected outputs,
- Parametric specification: defines how the system should perform, such as average power consumption and performance,
- Datasets: input vectors representative of the final application scenario,
- Firmware: source code (VHDL or Verilog), IP-cores to be integrated, FPGA bitstream, or ROM binary,
- Software: source code (C, C++...), compiled executables, or boot image.

Having access to the final embedded application and documentation is obviously a best case. In real life, the final version of an application is often not available in the early stage of a project when hardware evaluation and choices have to be made. In such case, a representative application or set of benchmarks should be defined in order to exercise the hardware in a way similar to what the final application is expected to do, as reported in [QRRA15].

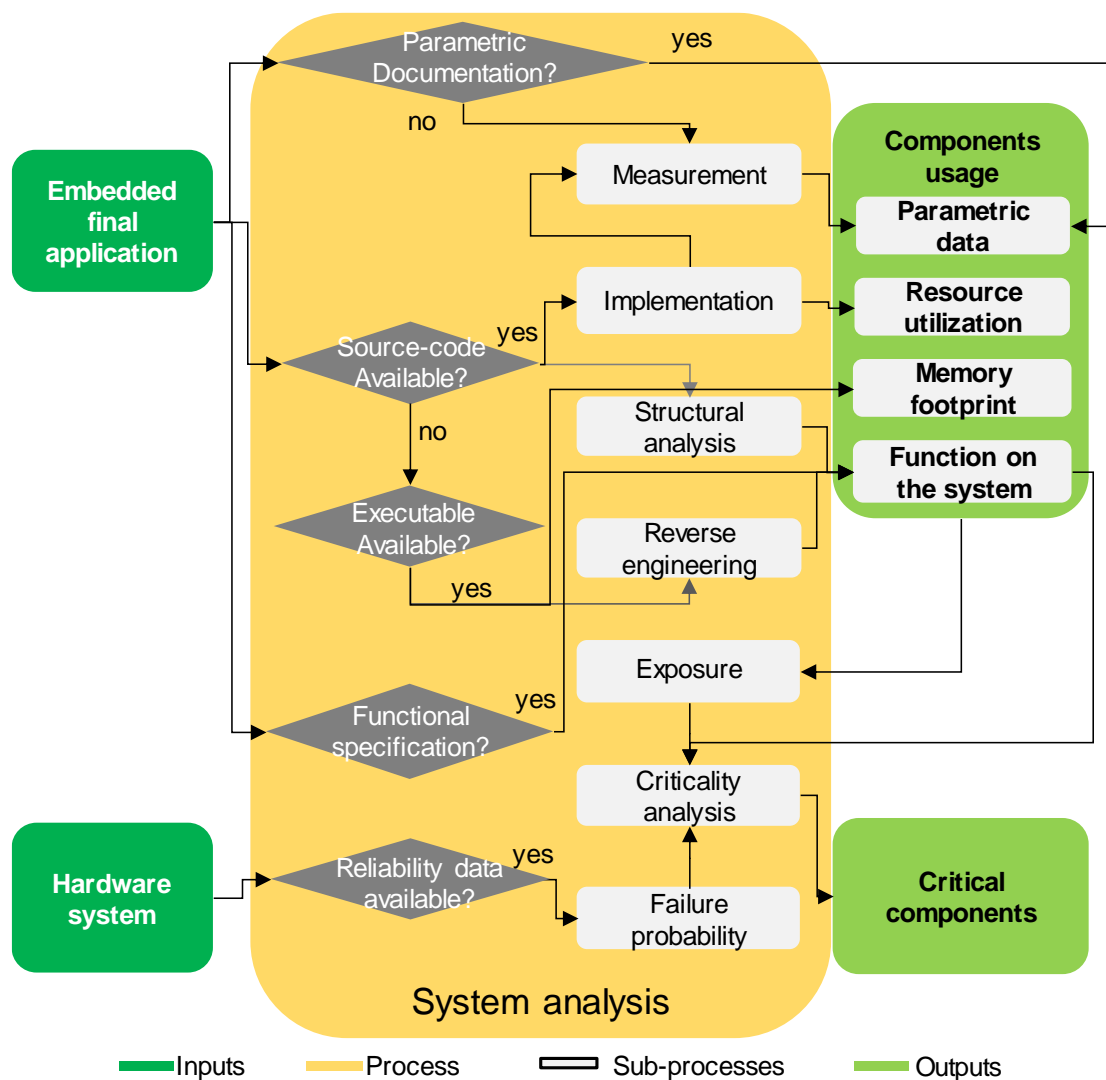


Figure 5-2. System analysis block diagram

Performing the system analysis consists in exploiting the available descriptions for identifying the critical components of the system and their usage. The critical components are the ones that have the highest impact on the system functionally or availability when they fail. The components usage stands for the result of the system customization by the embedded final application or representative benchmarks. A typical procedure for obtaining those outputs is illustrated in Figure 5-2.

5.2.1.1. Obtention of components usage

Depending on the final embedded application data provided by the designer, different activities have to be performed to extract components usage. When the source code is available, the tester can perform structural analysis to obtain the function of the different components, resources and computation units of the system. This information can also be directly obtained when a detailed functional specification of the system is provided. If only the executable files are provided, one can perform reverse engineering for obtaining the components function in the system. Memory footprint can be obtained directly from the executable files. Regarding resource utilization, they can be obtained by implementing the source code on the hardware system.

5.2.1.2. Defining critical components

The criticality of a component depends on the application and its function in the system. Power components like regulators, for instance, are essential for supplying the whole system, then they are always critical. A Flash memory that stores encryption key is a critical component until the key is loaded. Components or resources that define the computation capability or the availability of the system, such as processors or FPGAs, are also critical components. In a classical approach, components that represent a single-point of failure for the whole system should be considered as critical components, in the sense that a careful estimation of their individual behavior under radiation is required.

Evaluating the criticality of a component must be done in conjunction with evaluating the severity of the failures that it may face or induce at the system-level. Indeed, the simple corruption of non-vital data or the transient disruption of a computation cycle does not result in the same criticality as a permanent power failure of the system. Thus, an index of criticality could be defined for each component and each of its possible failure modes in order to prioritize the reliability evaluation efforts.

5.2.2. Instrumentation for testing and test plan elaboration

The second macroblock of the methodology is presented in Figure 5-3.

Additionally, to the critical components and components usage previously described, the instrumentation for testing process also takes the mission requirements as an input. Description of the mission

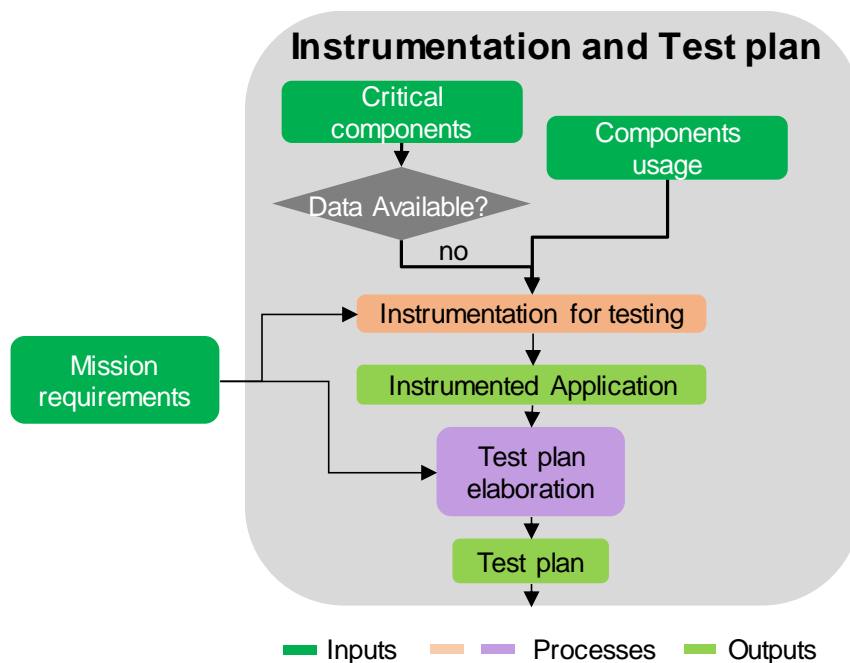


Figure 5-3. Instrumentation for testing and test plan elaboration – Second macroblock of the proposed methodology

requirements includes the mission profile and duration, the radiation environment, the test budget range, and the required fault coverage.

5.2.2.1. Adding instrumentation to the final application

The processes for adding instrumentation to the final application are presented in Figure 5-4.

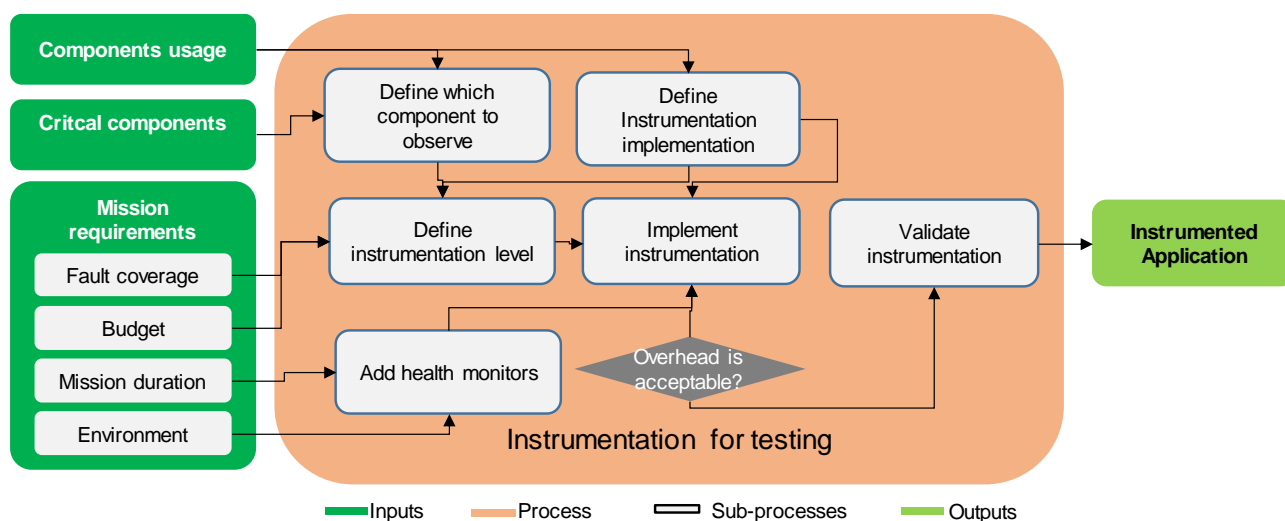


Figure 5-4. Instrumentation for testing block diagram

The first process consists in defining which components or resources should be observed. This definition depends on the critical components and the components usage. Those components can be memories that are used by the application, computations performed by the software or specific computation units, power regulators etc. Then, the instrumentation implementation should be defined according to the components usage. An efficient way of implementing instrumentation is to use spare components and resources that are not used by the final embedded application. Different levels of parallelism can be explored to implement software instrumentation. One could take advantage of multi-core parallelism and use spare cores or even

entire processing units (e.g. RPU) for implementing the instrumentation. Alternatively, if a single-core is available, one could take advantage of thread-level parallelism and implement instrumentation tasks. The operations performed by the code-instrumentation can monitor the following events:

- Computation
- Application Flow
- Data integrity
- Parametric degradation

Different algorithms can be used to check the computation performed by different component resources such as predictable range checking, checksum [NRSA90], parity bit [PRKA18] and Cyclic Redundancy Check (CRC) [ZHYU08]. However, the overhead of those algorithms should be considered when analyzing the data.

The application flow of a system can be analyzed by using watchdogs, or built-in internal debug structures such as the CoreSight technology of ARM processors [PLEG20]. Another built-in structure that can be used for improving system observability are the Data Fault Status Registers (DFSRs) of ARM co-processors [ARM16]. Those registers store important information about the sources of exceptions (e.g. memory cache errors) that can help in the resource root cause analysis.

Regarding analog measurements (e.g. temperature and voltage), some manufacturers provide internal ADC (Analog-to-digital converter) for measuring internal parameters that can be easily accessed by the application. Some carrier boards also include I2C-slave system monitors connected to the power regulators so that currents and voltage measurements can be done.

Currently, many memory components offer built-in ECC or error detection capabilities. Thus, available resources can be used to run embedded memory test benchmarks that are constantly monitoring the data integrity of the memories.

Hardware instrumentation can also be embedded to improve the observability of FPGA resources or analog parts. PL IP-cores can be developed or used for monitoring the bitstream, checking a PL computation or even checking the software application flow using the CoreSight built-in structure [PLEG20]. As those instrumentation IP-cores will also be exposed to radiation, they should be SEE-hardened or their SEE cross-section must be considered. When the estimated total dose for the mission is high, health monitors such as ring oscillators can also be implemented on configurable resources in order to monitor the parametric degradation. Custom-designed boards can also be used as hardware instrumentation for monitoring and protecting digital systems against destructive failures such as SELs. In some cases, some rudimentary patching of the PCB, like soldering a shunt resistor, may be sufficient to monitor important parameters like the supply current. This requires the full board schematic, which is rarely available for commercial digital systems. Moreover, developing a specific hardware instrumentation at board level adds complexity (i.e. time and cost) to the RHA methodology, so such decision should be taken early in the process based on an observability vs budget trade-off.

Once the components to be observed and the types of instrumentation implementations are defined, a hierarchy of instrumentation levels can be designed to achieve the fault coverage target within the budget requirements. Mission requirements shall also define if the overhead of a specific instrumentation level is acceptable.

The instrumentation can be manually added to the application by developing an instrumentation library of functions and inserting calls in the right places. This process could also be done automatically, using a customized code pre-processor and by defining the application operations that require instrumentation. When only compiled executables are available, a limited level of decompiling might be performed in order to identify the places where low-level instrumentation could be added directly at the assembly level.

Finally, the instrumentation needs to be validated. Fault injections can be performed by emulations, simulations and laser injections, as previously mentioned. The instrumentation validation will also depend on the mission budget. Once the instrumentation is validated, the instrumented final application is available for testing.

5.2.2.2. Test plan elaboration

The activities of the test plan elaboration are presented in Figure 5-5.

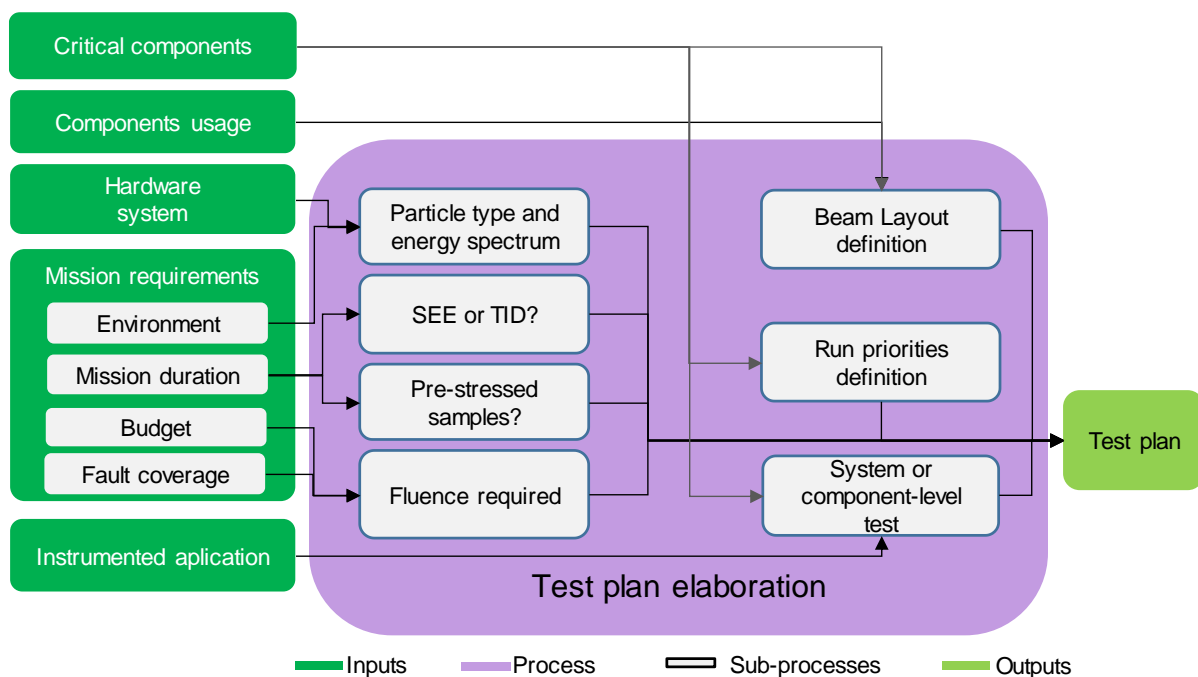


Figure 5-5. Test plan elaboration block diagram

First, the particle type and energy spectrum are defined according to the radiation environment of the mission (atmospheric neutrons, protons, Co^{60} ...) and the package thicknesses and materials of the components. Afterwards, the mission duration and dose levels will define whether TID experiments are required and if additional pre-stressed samples should be tested to identify possible synergistic or coupled effects. The requirement of pre-stressed samples also depends on the budget as aging experiments require many samples and are very time consuming.

The required fluence will depend on the required fault coverage and beam-time budget. A cost-effective system-level approach aiming for low fault coverage (worst case analysis) performed by [GUGU17] empirically proposes a fluence of $1\text{E}+10 \text{ p/cm}^2$ using only one energy (about 200MeV protons). Thereafter, the beam layout should be defined and depends on the components usage and critical components as well the particle spectrum. For instance, if a DDR3 memory is used in a digital system, the beam layout can be defined so that two digital systems are irradiated simultaneously while one of them leaves the DDR3 out of the beam. This way, the influence of such critical component at system-level can be observed. It is also important to take advantage of the beam geometry for saving beam time such as stacking digital systems horizontally in atmospheric neutrons experiments, for instance. Definition of the runs priorities should take into account the index of criticality of the components.

Finally, the criticality of some components and the test budget will define if system-level or component-level tests are required. As the radiation response of a component is obtained directly on standard component-level tests, this approach is indicated only for critical components. In low-budget missions, the component-level data can be obtained by embedding a benchmark on the target hardware and characterizing it at system-level. The complexity of choosing between system-level and component-level tests is associated to the process of finding a cost-observability-risk acceptance compromise. Thus, this process is very application dependent and difficult to generalize.

5.2.3. Radiation experiments and data analysis

The processes of the third macro-block of the bridging methodology is presented in Figure 5-6.

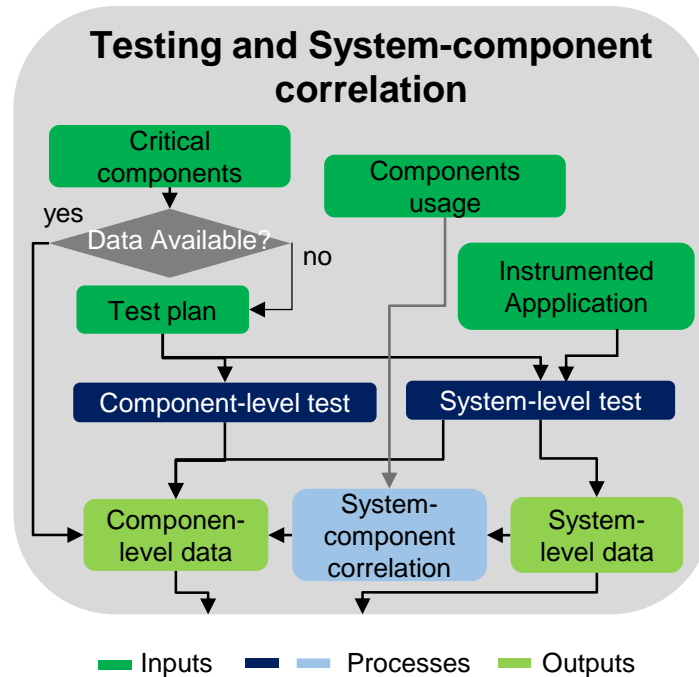


Figure 5-6. Test process and system-component correlation (data analysis) – Third bridging methodology macro block

This macro block is responsible for obtaining both component-level and system-level data required to perform system-level reliability calculation. The procedures for performing classical component-level tests were described in Chapter 2 and guidelines and recommendations for performing system-level experiments

were provided in the first section of this chapter. A well-validated remote-controlled and automated experimental setup is essential for the success of a system-level experiment as the complexity is usually increased in comparison to component-level experiments.

Thanks to the added instrumentation, it should be possible to relate a majority of the events observed during system-level tests to a root cause, i.e. the initial failing component or resource and the failure mechanism. This is the objective of the next step, which consists in correlating both component- and system-level data in order to quantify the probability of each failure mechanism for each critical component or resource.

5.2.3.1. System-component correlation

The system-component correlation sub-processes are illustrated in Figure 5-7.

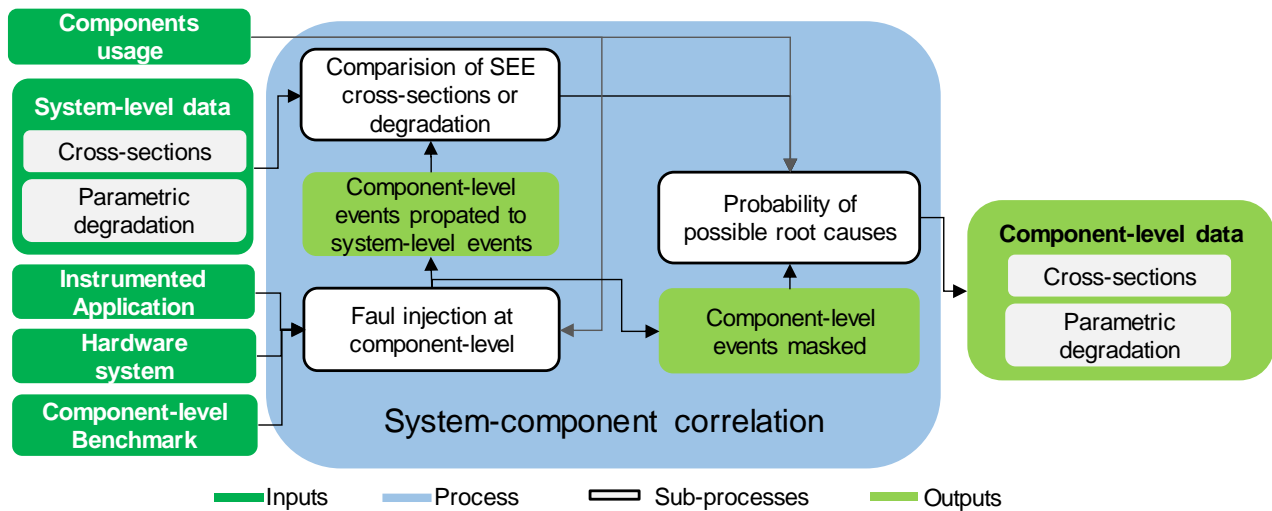


Figure 5-7. System-correlation block diagram

This correlation aims, for the most critical fault signatures observed at system-level, to identify the root cause and, when non-trivial, to understand how it propagated to a system output. We can define the root cause, or root event, as the combination of a) the component or resource initially impacted or degraded and b) the physical and electrical mechanism at the origin of the fault. As an example, an MBU affecting a code section in a memory component could be the root cause of a system hang. This system-level event to root cause correlation is required to:

- estimate the probability of occurrence of the root events in a given environment using classical component-level rate prediction methods,
- evaluate the specific masking capabilities of the system, related either to the components usage or to existing high-level hardening conditions like code or data redundancy,
- identify possible solutions to improve the reliability of the system.

At this stage, fault injection techniques can seriously help in the fault propagation analysis. Depending on the test budget and technical possibilities, it can be performed at different levels of abstraction from laser-induced fault injection at component-level to purely programmatic fault emulation at code level.

A careful structural and dynamic analysis of the application, facilitated by the availability of the source code, should allow to identify the possible fault propagation paths with their corresponding probabilities. A quantitative index representing the level of confidence on each propagation scenario can be introduced to keep track of the uncertainties during this analysis.

Regarding SEUs and MBUs in memories, the fault propagation and masking are related to the components usage of the final embedded application. The embedded application defines the frequency by which the memories are used, for instance a DDR upset in a memory cell used by the application software will not be propagated to next operations if a writing operation overrides the wrong value before a reading operation. For such analysis, a stochastic approach is commonly applied such as the Architecture Vulnerability Factor (AVF) [MWER03]. The AVF defines the probability that a memory upset will generate a system error. It can be estimated by using the cross-section per bit of a memory and then obtaining the number of system errors that were generated. The portion of memory that is effectively used (components usage) has to be considered such as the static code and data region of the application, as well as its heap and stack regions. In the AVF approach, the bits that are responsible for the normal operation of the application are classified as Architectural Correct Execution (ACE) bits. ACE bits are then sub-divided into Silent Data Corruption (SDC) when masked and Detected Unrecoverable Errors (DUE) when propagated to the output. On FPGA designs, the configuration bits that are used in the designed are defined as essential bits and the ones that can generate a system error are classified as critical bits [XILI18C]. It can be estimated by using the cross-section per bit of a memory and then obtaining the number of system errors that were generated. In software applications it can be related to DDR memory bits, cache bits and so on.

In this correlation phase, a particular effort should be put on discriminating the most critical root causes that could lead to the permanent degradation of the system, like SELs, from other events, like some SEFIs, that may lead to similar system-level signatures during a test campaign but without the long-term reliability implications. When correctly designed and implemented, the observability provided by the detailed reports of the added instrumentation should help in this effort.

Regarding TID induced degradation, since it can be considered as permanent in a first approach, its impact on digital systems is usually irreversible. Thus, it is first essential to have some analog monitoring of the phenomenon before it leads to a permanent failure. Then, the possibility to perform root cause identification will be highly dependent on how hardware isolation was implemented into the system. On a SoC like the ZU+, this analysis could benefit from the isolation of the different power domains of the chip, combined with the embedded voltage monitoring resource. A common approach to understand TID degradation propagation is to use Bayesian networks [DMBH15].

5.2.4. System-level reliability calculation

The final process of the proposed methodology consists in combining the available component-level data and obtained system-level data to perform a first order prediction of the reliability of the system, as presented in Figure 5-8.

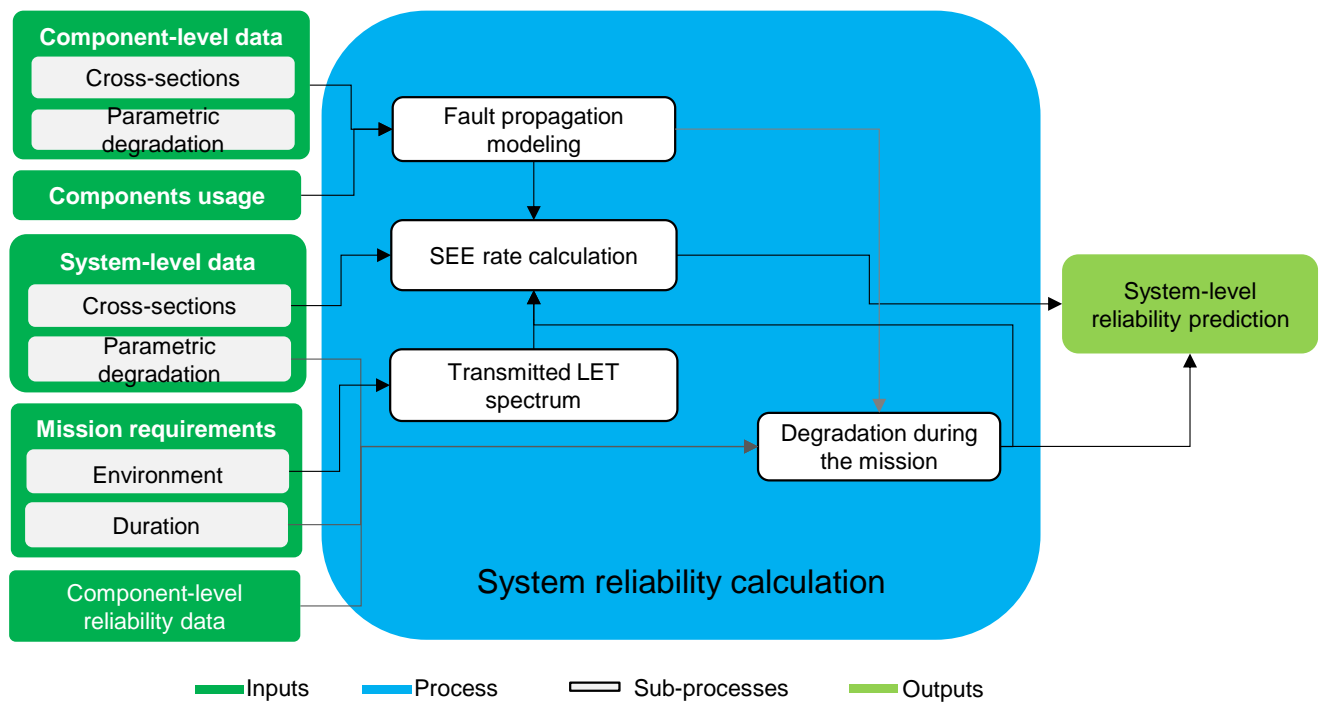


Figure 5-8. System reliability calculation block diagram.

Regarding SEE, first order system-level event rates can be calculated directly from system-level events cross-sections and the transmitted spectrum of the mission environment. When root cause analysis was not conclusive, some assumptions might be performed. Another important parameter is the threshold energy or LET that will define the fitting of the cross-section curve versus the particle energy or LET. When system-level experiments are performed with only one single particle energy (like 200MeV protons), this value should be estimated from technology information or obtained from the literature. Those assumptions can obviously lead to the accumulation of uncertainties in the SEE rate calculation. Once those parameters are known, common tools for rate calculation can be used such as OMERE [OMER20]. This process can be combined with the component-level data cross-section obtained from experiments or the literature. Components usage information can be used for modeling the fault propagation to system-level failures using tools such as the Systems Engineering and Assurance Modeling (SEAM) tool [AMSK17].

Regarding TID, the process starts by calculating the dose curve for a mission environment and duration using dose calculation tools such as OMERE. The dose calculation information can be combined with system-level parametric degradation level versus dose in order to estimate the system parametric degradation during the mission. Comparison between modeled and measured system-level parametric degradation can be used to improve the confidence level of the measurements.

5.2.5. Methodology summary

The proposed bridging methodology block diagram is summarized in Figure 5-9

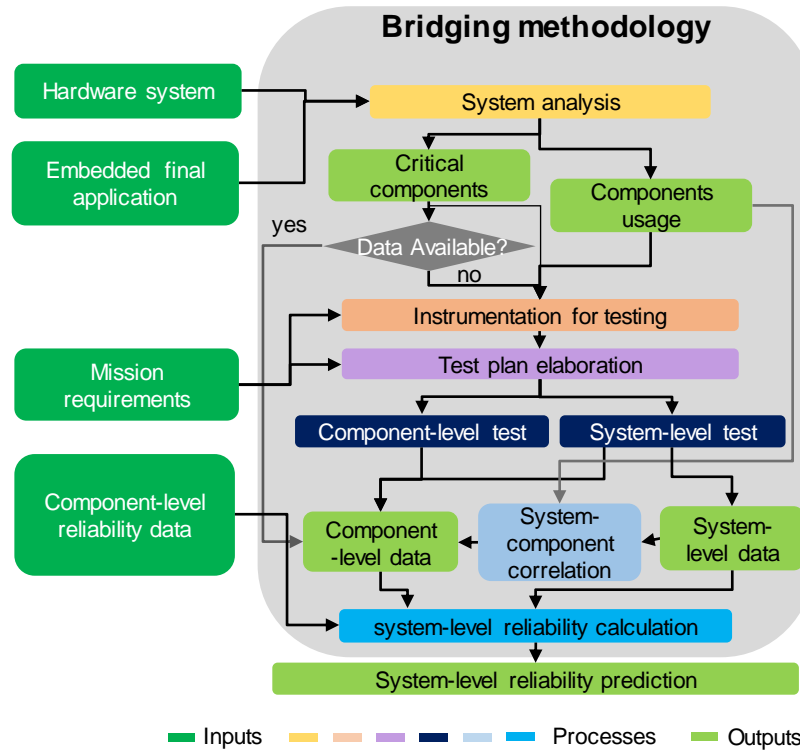


Figure 5-9. Bridging methodology block diagram

This methodology was designed for the SoMs under test in this work. As was described previously, each step or process in this methodology brings its part of assumptions, approximations and trade-offs. It should be considered as a first step in the development of a more generic and robust strategy for providing system-level reliability prediction from system-level testing and should obviously be used with much care.

5.2.6. Limitations and possible improvements of the proposed methodology

5.2.6.1. Standard error reporting for system-level

An important step towards a more generic system-level testing strategy would be the standardization of the reporting of system-level events. Indeed, in the literature, results from tests performed at system-level are most often reported using an application-specific classification of the events. This can be explained by the main motivation of the tests, which is to evaluate the impact of root events on the specific application outputs. However, this makes the results almost impossible to reuse or to transpose to a different software application on the same hardware. Another common approach is to classify the system-level events between very generic categories like critical and non-critical events, that completely loose the information that might be needed for further analysis of the system reliability.

One solution could be to introduce standard subcategories related to the impact of the events at the system-level such as the following:

- Loss of computation
- Loss of power
- Loss of data integrity

- Loss of synchronization
- Loss of performance

The applicability of such standard classification would need to be validated against a great amount of different applications.

5.2.6.2. Cross-platform library

In this work, an instrumentation library was developed targeting final applications embedded on ARM v7 and v8 micro-architectures and Xilinx SoCs. However, in order to obtain a standard error reporting, a cross-platform library being supported by most used architectures would have to be developed. It would be composed of a portable API layer, including the high-level functions and IPs that compose the different instrumentation levels, and an architecture-specific implementation layer that would make use of the particular resource, registers or primitives of each family of hardware targets.

5.2.6.3. Automated insertion of instrumentation

In this work, the instrumentation was added manually to the source-code of the final embedded application. Different alternatives can be envisioned in order to automatize this process by adding automatically code-instrumentation blocks directly in the source code or the executable binary. This could be done using a custom code preprocessor or compiler, similarly to what is done for code-level hardening. This approach would significantly decrease the time overhead associated to the instrumentation of the application.

5.3. Methodology case study discussion

We applied the proposed methodology to our case study using the results of our experimental campaigns. We considered a LEO mission on the ISS orbit and used OMERE for the environment and rate calculations. The results in terms of system-level reliability predictions for the events considered as the most critical are presented in Table 5-2.

Table 5-2. Trapped-proton error rate for a LEO ISS mission (800km/50.6°)

Intermediate rate calculations from experimental data and literature						
Data	SoM	Component	Event	SEE rate (events/day/device)		Comments
				Heavy-ion	proton	
Component-level	Z7	SoC	Soft failures	6.06E-05	3.04E-06	Some events extracted from Zynq7000, other extracted from Kynx7 and Virtex7
			Hard failures	4.74E-07	6.65E-06	
			Resettable failures	6.08E-07	3.43E-04	
		DDR	Soft failures	5.06E-11	2.85E-09	Same DDR3 part number
			Hard failures	?	?	
			Resettable failures	6.03E-06	1.12E-06	
		Flash	Soft failures	4.32E-16	0.00E+00	Same Flash part number
			Hard failures	2.41E-11	1.51E-14	
			Resettable failures	1.12E-11	3.55E-15	
		DCDC	Hard failures	?	?	
	ZU+	SoC	Soft failures	2.69E-04	2.25E-05	Extracted from a higher capacity chip from the same family
			Hard failures	5.30E-05	5.46E-03	
			Resettable failures	1.05E-04	1.05E-06	
		DDR	Soft failures	1.37E-10	3.07E-16	Extracted from a different DDR4 manufacturer
			Hard failures	?	?	
			Resettable failures	1.03E-03	4.08E-14	
		Flash	Soft failures	8.61E-16	0.00E+00	Same Flash part number
			Hard failures	2.41E-11	1.51E-14	
			Resettable failures	1.12E-11	3.55E-15	
		DCDC	Hard failures	8.38E-09	8.77E-10	Same manufacturer family
System-level	Z7	-	Soft failures	2.47E-04	1.22E-11	Low fluence, issues with the beam
			Destructive failures	-	-	
			Resettable failures	6.63E-03	0.00E+00	
	ZU+	-	Soft failures	2.63E-04	1.29E-11	Low number of errors
			Destructive failures	4.20E-04	2.07E-11	
			Resettable failures	3.32E-04	0.00E+00	
Final System-Level rate predictions						
Optimistic Total SEE rate (events/day/system)	Z7	Soft failures	2.47E-04	Soft and resettable system-level rates are higher than the sum of component-level rates. Hard failures extracted from the sum of component-level rates		
		Hard failures	7.12E-06			
		Resettable failures	6.63E-03			
	ZU+	Soft failures	2.91E-04	Soft and resettable failures rates obtained from the sum of the components rate		
		Hard failures	5.51E-03			
		Resettable failures	1.14E-03			
Conservative Total SEE rate (events/day/system)	Z7	Soft failures	4.94E-04	Non-critical - Multiplied by a margin factor of 2		
		Hard failures	2.85E-05	Critical - Multiplied by a margin factor of 4 due to lack of data		
		Resettable failures	1.99E-02	Semi-critical multiplied by a factor of 3		
	ZU+	Soft failures	5.82E-04	Non-critical multiplied by a factor of 2		
		Hard failures	1.65E-02	Critical - Multiplied by a margin factor of 4 due to lack of data		
		Resettable failures	3.41E-03	Semi-critical multiplied by a factor of 3		

The different events were classified into soft failures, hard failures, resettable failures and destructive failures. Those classifications were performed differently for the data extracted at component-level and system-level.

For the measured system-level cross-sections, soft failures are events that change the functionality of the system but not require a reset to be corrected. Resettable events, as the name implies, need soft (application re-loading and FPGA reconfiguration) or hard resets (power cycles) to be corrected. Destructive failures are the SELs or Single Event Burn-Out (SEB) that lead to the SoM destruction. During the system-level measurements, hardware instrumentation for detecting SELs was not implemented so non-destructive SEL could not be distinguished from other hard resettable failures.

For the component-level information in table 5-2, hard failures rates are calculated from SEL cross-sections from the literature.

For the final system-level rate prediction of hard failures, the worst case was considered between destructive failure measurements and the component-level hard failure rates.

Thus, the measured 184MeV proton system-level checksum errors were classified as soft failures while Soft and Hard SEFIs, and timeouts were classified into resettable failures. Finally, permanent loss of power was classified as destructive failure.

Regarding the DDR3 [KOGB12][GHGS12], DDR4 [PJBL17][GUCU17], Flash [IRNG11], Z7 SoC [CCHK19][IRAM15][YDHS18][SSGW17], ZU+ SoC [DLLT19][LKEC18], DCDC converter [AISV16] component-level data obtained from the literature, the process consisted in multiplying the cross-sections per bit, from the same or similar components, by the memory bits used (components usage) in the design and making reasonable assumptions to cover incomplete data. LET and proton energy thresholds were estimated from the literature, missing proton cross-section was obtained from heavy-ion cross-sections by using the SIMPA model [BDOU95], and heavy-ion cross-sections were obtained from neutrons and protons considering the maximum secondary ion LET [HIBL03] as the saturation LET.

A system-component correlation was performed in order to define the failures classification. By definition, component-level SEL are defined as hard failures and SEFIs were defined as resettable failures. However, the failures classification of component-level SEUs and MBUs depends on the fault tolerance of the application. As ECC was activated for Flash, DDR, OCM and FIFO BRAMs, just MBU were classified as soft failures. The DDR MBUs in the data region were classified as soft failure while DDR MBUs in the code region were classified as resettable failure as it can generate application crash, timeouts... As ECC was not implemented on the SoC PS cache memories and the FPGA CRAM, SEU on cache memories can generate soft failures and SEU in the FPGA CRAM requires a reconfiguration (resettable failure).

The total rate prediction obtained from system-level data was compared to the worst-case fault propagation of component-level data. Thus, in order to avoid underestimation, the highest rate between them was chosen and the system-level rate estimation from component-level data was used to cover unobserved

events. In the conservative estimation, common-applied Radiation Design Margins (RDM) was used depending on the criticality of the events [MFAB17].

The optimistic total rate estimation in Table 5-2 show that the event rates are relatively low. A secondary Cube-Sat mission lifetime of 0.25 years [SWAR17], considering only those events, could be validated by using this methodology since the highest rate event (Z7 resettable failure) would take 0.41 years to happen. However, if the conservative total rate would be applied, the failure risk of the mission would be high as the highest rate event (Z7 resettable failure) would take 0.13 years to happen.

Nonetheless, that approach enables only WCA. Thus, the design margin cost can be reduced through precise error rate estimation by obtaining PL critical bits and AVF out of essential and data region bits, respectively [MWER03]. Moreover, if the system availability (resettable failure rate) requirements are not met, one should know which component caused those errors. Through laser fault injection on the SoC, it was possible to identify possible PS and PL resource root causes. However, other events such as external memory (Flash and DDR) upsets were not captured by the added instrumentation.

Thus, Failure Mode Effects and Criticality Analysis (FMECA) [LIND16] rather than only WCA, should be performed, when possible, by improving the system instrumentation or performing additional laser fault injection.

5.3.1.1. Case study limitations

An important limitation of the presented case study is the lack of observability of SEL and analog parts. That could be achieved by minor hardware modifications but requiring full SoM schematic and slightly increasing the test complexity. This way, a trade-off between observability and overhead should be leveraged. Another option for SEL observation might be to use an infrared camera as performed in [BILA20].

The uncertainties added to the system reliability prediction due to the experimental result margins should also be mitigated by adding an effort to the test plan, experimental setup and instrumentation preparation. As the use of only one single proton energy around 200MeV for estimation orbit SEE rates implies assumptions and approximations on the SEE rate calculation, the experiment data should be as precise as possible to avoid error propagation.

In addition, even reaching a relatively high fluence in the ZU+ experiment ($1.79\text{E}+10$ p/cm²), low events statistics with high error bars were observed (Figure 4-14) and only proton energy cross-section saturation and estimated energy threshold were used. Those uncertainties should be considered when transposing the SEE rates to other environments.

5.4. Conclusions

In this chapter, recommendations and guidelines for performing system-level experiments were provided as well as a bridging RHA methodology proposal and case study discussion. First, lessons learned from the radiation experiments were shared in order to reduce the efforts associated to system-level test execution and preparation. Then, a bridging RHA methodology for applying the conventional component-level

RHA methods on the emerging system-level approach was provided. Finally, the methodology case study was discussed including the limitations and possible improvements.

6. CONCLUSIONS AND PROSPECTIVE

This work investigated the possibility to define a bridging RHA methodology from component-level to system-level for evaluating the reliability of digital systems under radiation.

We first presented the state of the art of radiation effects and other reliability issues on digital components and the current component-level radiation testing methodologies. We explained how this context motivates the development of new RHA methodologies oriented towards system-level testing, especially for low-cost/acceptable risk applications.

The next chapter presented the digital system and a custom application that we designed as a case study for this work. The system was developed and implemented on commercial industrial SoMs based on recent SoCs in 28nm Planar and 16 FinFET CMOS technologies. The specific code and hardware instrumentation, which was added to the system in order to improve the observability of the system in the context of a system-level testing approach, was detailed and discussed.

The third chapter presented the various radiation test campaigns that were performed, within the RADSAGA consortium, in order to accumulate data for evaluating the reliability of our system. Tests were performed using atmospheric-like neutrons, 184MeV protons, local X-rays irradiation and 1064nm pulsed laser. The results were presented and discussed. They confirmed that testing with high-energy protons should be the preferred method for screening low-cost systems for SEE.

The last chapter summarized the lessons learned from our system-level testing campaigns and proposed a bridging methodology that could be applied for radiation assessment of similar systems. A case study of reliability estimation was presented, considering our system and a LEO-ISS mission. We saw that the limitation of our hardware instrumentation regarding the lack of observability on certain destructive failures and external memories upsets could be compensated with component-level data extracted from the literature.

Regarding the root cause analysis of system-level failures, there is currently a good amount of radiation data available in the literature that can help regarding external memories such as DDR and Flash components. This can be explained by the fact that those components are relatively simple to test exhaustively under radiation, which is not the case for processors, FPGAs, microcontrollers... Thus, the challenge on digital systems is to understand how and where the faults are generated in those complex components. To this extent, pulsed laser and local X-ray irradiations enable a better understanding of the fault and degradation mechanisms on those components. This way, those techniques contribute to validate and improve the fault generation and propagation models and, as a consequence, the quality of the system reliability predictions.

The proposed bridging methodology attempts to make an optimal use of existing data, tools, and methods from the classical component-level approach. One important contribution of this work was related to the design and addition of instrumentation to the final embedded application in order to significantly improve the observability of the various kinds of events during system-level testing. Instrumentation should be seen as a way to have a peek into the system's "black box". The final version of the code-instrumentation did this while adding low code-size and performance overheads to the application. The exploration of built-in checking

and correction capabilities of the components showed that they also represent an efficient way of adding instrumentation at low cost. In addition, the flexible TID and aging benchmark implemented allowed to observe and compare the parametric degradation of the two tested technologies under total dose. Such information is rare in the literature and has a great importance for FPGA designers working on strongly time-constrained designs for space applications.

Several paths were identified to improve the proposed methodology. Developing the portability of the instrumentation on different FPGA and processor architectures would help to generalize the approach. Tools could be developed in order to automate the insertion of the software and firmware instrumentation. We also observed the need for a radiation-specific standard for the classification and reporting of system-level events observed during a system-level test in order to facilitate partial reuse of those data.

System-level SEE rate prediction from system-level testing is a complex task and the proposed bridging methodology making use of both system-level testing and component-level analysis is a starting step towards that objective. In order to extend the methodology to a broader range of systems and applications, more case studies and instrumentation options should be investigated. Additionally, a possible extension of the proposed methodology could include the monitoring of coupled aging and radiation effects. Indeed, as of today, those coupled effects are typically taken into account by adding design margins to the system, which, in turns, have significant cost implications.

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A. APPENDIX

A.1. TID benchmark details

Table A-1. Selectable external voltage and currents from the System monitor

Selection	Voltages	Currents	ZX5	XU5	XU3	Description
0	VCCMOD		12			Module supply voltage
	VCCIOA		2.5	1.8	1.8	PS and high range FPGA IO voltage
	VCCIOB		1.8			High performance FPGA IO voltage
	VCC3V3		3.3			3.3V SoM DCDC voltage
	VCC5V		5			5V SoM DCDC voltage
		IVCCMOD	-	-	-	VCCMOD current
		IVCC3V3	-	-	-	VCC3V3
1	VCCA102		0.85	1		SoM DCDC voltage on pin A102
	VCCB8		1.2	1.35		SoM DCDC voltage on pin B8
	VCCB167		0.9	1.2		SoM DCDC voltage on pin B167
	VCCB168		0.5	2.9		SoM DCDC voltage on pin B168
		IVCCIOA	-	-	-	VCCIOA current
		IVCCIOB	-	-	-	VCCIOB current
		IVCCREF	-	-	-	Reference voltage current

A.2. Neutrons experiment details

Table A-2. ChipIR complete test log

ZU+ Test log						
RUN #	SUT #ID	Energy (MeV)	Flux	Description	Desired fluence	Fluence reached
1	XU5#1	<800	3.00E+06	DDR4 test	1.00E+10	4.62E+10
	XU5#2				1.00E+10	1.97E+10
2	XU5#1			Flash test	1.00E+10	6.19E+09
	XU5#2				1.00E+10	0.00E+00
3	XU5#1			OCM test	1.00E+10	1.10E+10
	XU5#2				1.00E+10	1.15E+10
4	XU5#1			control loop - V1	1.00E+10	1.79E+10
	XU5#2			control loop - V1	1.00E+10	1.10E+10
Z7 Test log						
RUN #	SUT #ID	Energy (MeV)	Flux	Description	Desired fluence	Fluence reached
1	ZX5#1	<800	3.00E+06	DDR3 test	1.00E+10	7.07E+09
	ZX5#2				1.00E+10	2.11E+10
2	ZX5#1			Flash test	1.00E+10	2.30E+09
	ZX5#2				1.00E+10	1.20E+09
3	ZX5#1			OCM test	1.00E+10	0.00E+00
	ZX5#2				1.00E+10	0.00E+00

A.3. Protons experiment details

Table A-4. Protons experiment 1 test log

BEAM RUN #	Energy (MeV)	LET (Si) (MeV/mg/cm ²)	SUT ID	Test description	Flux (p/cm ² /s)	Beam time (s)	Fluence (p/cm ²)	Effective Fluence (p/cm ²)	Accumulated Dose(rads)
1.a	184	3.9E-03	ZX5#3	IL2 - system-level - V1 - DDR	3.00E+06	1911	5.73E+09	1.94E+09	3.67E+02
			ZX5#4	IL2 - system-level - V1 - NO DDR				3.29E+09	
1.b			ZX5#3	IL2 - system-level - V1 - DDR	1.00E+06	1220	1.22E+09	5.16E+08	7.81E+01
			ZX5#4	IL2 - system-level - V1 - NO DDR				5.14E+08	
1.c			ZX5#3	IL2 - system-level - V1 - DDR	2.00E+06	299	5.98E+08	5.96E+08	3.83E+01
			ZX5#4	IL2 - system-level - V1 - NO DDR				5.96E+08	
1.d			ZX5#3	IL2 - system-level - V1 - DDR	3.00E+06	379	1.14E+09	8.49E+08	7.28E+01
			ZX5#4	IL2 - system-level - V1 - NO DDR				3.75E+08	
2			ZX5#3	component-level - DDR	3.00E+06	2401	7.20E+09	4.50E+09	4.61E+02
			ZX5#4	component-level - OCM				3.78E+09	
3			ZX5#3	IL1 - system-level - V1 - DDR	3.00E+06	594	1.78E+09	1.05E+09	1.14E+02
			ZX5#4	IL1 - system-level - V1 - NO DDR				2.73E+08	
4			ZX5#3	IL0 - system-level - V1 - DDR	3.00E+06	580	1.74E+09	1.74E+09	1.11E+02
			ZX5#4	IL0 - system-level - V1 - NO DDR				2.40E+07	

Table A-3. Protons experiment 2 test log

BEAM RUN #	Energy [MeV]	LET (Si) (MeV/mg/cm ²)	SUT ID	Test description	Flux (p/cm ² /s)	Beam time (s)	Fluence (p/cm ²)	Effective Fluence (p/cm ²)	Accumulated Dose(rads)
1	184	3.90E-03	XU5#4	IL2 - system-level - V2	3.00E+06	948	2.84E+09	2.26E+09	4.55E+04
2			XU5#12	IL2 - system-level - V2	3.00E+06	5956	1.79E+10	1.46E+10	2.86E+05
3		3.70E-03	ZX5#5	IL2 - system-level - V2	3.00E+06	890	3.52E+09	2.07E+08	5.63E+04

A.4. Laser experiment details

Table A-5. Z7 laser test log including zones that can possibly generate errors

Z7 Laser test log						
RUN #	Energy (PJ)	Equivalent LET(MeV/mg/cm2)	Zone Irradiated	Scan mode	Pulses	Equivalent fluence (#/cm2)
1	189	19.97	L1 Data Cache	Sequential	4.25E+05	2.57E+08
2			OCM		2.39E+05	3.58E+07
3			Regs 1 and 2		6.49E+04	9.67E+07
4			L2 cache 1		4.14E+04	4.88E+06
5			L2 cache 2		4.14E+04	3.51E+06
6			Regs 3 and 4		3.64E+04	2.66E+07
7			Regs 5		2.04E+04	1.43E+07
8			Regs 6 and 7		4.75E+04	6.08E+07
9			L1 Inst Cache CPU 0		9.36E+04	7.05E+07
10			L1 Inst Cache CPU 1		3.72E+04	2.60E+07
11	275	24.04	AXIS_FIR_BRAM	Sequential	3.30E+04	3.49E+07
12			AXIS_PWM_BRAM	Sequential	3.21E+04	3.51E+07
13			AXI_1	Random	1.60E+05	1.52E+07
14			AXI_2		2.28E+05	2.32E+07
15			FIR_CLB_and_DSP		2.28E+05	2.32E+07
16			FIR_FIFO_BRAM	Sequential	3.35E+04	3.56E+07
17			FIR_FIFO_CLB		5.58E+04	5.56E+07
18			HR_IO		3.60E+04	1.57E+07
19			PWM_FIFO_BRAM		3.44E+04	3.66E+07
20			PWM_FIFO_CLB		3.78E+04	3.40E+07

Table A-6. ZU+ laser test log including zones that can possibly generate errors

ZU+ Test log						
RUN #	Energy (PJ)	Equivalent LET(MeV/cm)	Zone Irradiated	Scan mode	Pulses	Equivalent fluence (#/cm ²)
1	276	29.04	AXIS1 FIR CLB DSP1_2	Random	1.36E+04	2.45E+05
2			AXIS2		1.61E+05	8.22E+06
3			FIR AXIS BRAM	Sequential	2.74E+04	3.44E+07
4			FIR AXIS CLB		8.11E+04	1.68E+07
5			FIR CLB and DSP1	Random	2.85E+05	1.59E+07
6			FIR CLB and DSP2		8.64E+04	5.52E+06
7			FIR FIFO BRAM	Sequential	6.68E+04	5.39E+07
8			PWM AXIS BRAM		4.17E+04	5.13E+07
9			PWM AXIS CLB		1.64E+05	3.39E+07
10			PWM FIFO BRAM1		2.14E+04	1.96E+07
11			PWM FIFO BRAM2		2.05E+04	1.88E+07
12	310	32.37	Zone01	Sequential	4.98E+04	1.38E+07
13			Zone11		2.67E+04	1.65E+07
14			Zone12		7.90E+04	5.46E+06
15			Zone15.1		6.48E+04	2.11E+07
16			Zone2-4		2.80E+04	1.74E+07
17			Zone5		6.87E+03	1.74E+06

Table A-7. Zones used for laser Z7 PS fault injection

PL		PS	
Zone	Description	Zone	Description
1	FIR FIFO BRAM	4	OCM 1
2	AXIS FIR BRAM	5	OCM 2
3	PWM FIFO BRAM	6	L1 instruction cache 1 – CPU0
4	AXIS PWM BRAM	7	L1 instruction cache 2 – CPU0
5	FIR FIFO CLB	8	L1 instruction cache 1 – CPU1
6	PWM FIFO CLB	9	L1 instruction cache 2 – CPU2
7	FIR CLB DSP	10	L1 data cache – CPU0
8	AXI interconnect 1	11	L1 data cache – CPU0
9	AXI interconnect 2	12	Unidentified registers 1
10	High Range (HR) IO block	13	Unidentified registers 2
		14	L2 instruction and data cache 1
		15	L2 instruction and data cache 2
		16	Unidentified registers 3
		17	Unidentified registers 4
		18	Unidentified registers 5
		19	Unidentified registers 6
		20	Unidentified registers 7

Table A-8. Zones used for laser ZU+ fault injection

PL		PS	
Zone	Description	Zone	Description
1	FIR FIFO BRAM	1	Unidentified zone
2	AXIS FIR BRAM	2	Unidentified zone
3	PWM FIFO BRAM	3	Unidentified zone
4	AXIS PWM BRAM	4	Unidentified zone
5	FIR FIFO CLB	5	Unidentified zone
6	PWM FIFO CLB	11	Unidentified zone
7	FIR CLB DSP 1	12	Unidentified zone
8	FIR CLB DSP 2	15	Unidentified zone
9	AXI interconnect 1		
10	AXI interconnect 2		

List of Publications and Communications

Publication in an international conference:

- **Israel C. Lopes**, V. Pouget, F. Wrobel, F. Saigne, A. Touboul, and Roed, K. Røed. “Bridging RHA methodology from component to system-level applied to System-on-Modules”, accepted for oral presentation at RADECS 2020.
- **Israel. C. Lopes**, V. Pouget, K. Roed, F. Wrobel, A. Touboul, F. Saigné, J. Boch, and T. Maraine. “Comparison of TID-induced Degradation of Programmable Logic Timings in Bulk 28nm and 16nm FinFET System-on-Chips under Local X-ray Irradiation”, accepted for poster presentation at NSREC 2020.
- **Israel C. Lopes**, V. Pouget, F. Wrobel, A. Touboul, F. Saigne and K. Røed "Development and evaluation of a flexible instrumentation layer for system-level testing of radiation effects," 2020 IEEE Latin-American Test Symposium (LATS), Maceio, Brazil, 2020, pp. 1-6, doi: 10.1109/LATS49555.2020.9093681.
- Andrea Coronetti, Rubén García Alía, Jan Budroweit, Tomasz Rajkowski, **Israel C. Lopes**, Kimmo Niskanen, Daniel Söderström, Carlo Cazzaniga, Rudy Ferraro, Salvatore Danzeca1, Julien Mekki, Florent Manni, David Dangla, Alexander Koelpin, Vincent Pouget, Frédéric Saigné, Pierre Wang, Antoine Touboul, Arto Javanainen, Heikki Kettunen and Rosine Germanicus, “RHA through System-level Testing: Risk Acceptance, Facility Requirements, Test Methodology and Applications” accepted for oral presentation at NSREC 2020.
- M. Peña-Fernandez, A. Lindoso, L. Entrena, **Israel C. Lopes**, and V. Pouget. “Microprocessor Error Diagnosis by Trace Monitoring under Laser Testing”, accepted for oral presentation at RADECS 2020.
- Gennaro S. Rodrigues, Adria Barros, **Israel C. Lopes**, Vincent Pouget, Alberto Bosio, and Fernanda L. Kastensmidt. “An Approximate Error-Detection Technique for Multi-Core Real-Time Systems”, oral presentation at RADECS 2019, (in-press).

International communication:

- **Israel C. Lopes**. “Bridging methodology from component to system-level for the assessment of coupled radiation and degradation constraints in digital systems”. RADFAC 2018 (University of Montpellier, France, March 6, 2018).

TITRE : Méthodologie d'évaluation d'effets des radiations dans les systèmes numériques : du niveau composant au niveau système

RESUME

L'objectif de ce travail, réalisé dans le cadre du projet Européen RADSAGA, est de proposer une nouvelle méthodologie pour l'évaluation de la tenue aux radiations des systèmes numériques. Nous étudions la possibilité de définir une approche intermédiaire combinant le test au niveau système avec les connaissances et les méthodes connues au niveau composant. La méthodologie proposée est construite et appliquée à deux générations récentes de systèmes-sur-modules basés sur des systèmes-sur-puce en technologie 28nm et 16nm FinFET. Une instrumentation spécifique est développée et intégrée à l'application logicielle testée afin d'améliorer l'observabilité des événements durant des campagnes de test au niveau système menées avec différents types de faisceaux : neutrons atmosphériques, protons de haute énergie, impulsions laser et rayons X. Les résultats sont présentés et analysés, et les retours d'expérience sont résumés. La méthodologie passerelle proposée est alors détaillée et ses limitations et possibilités d'amélioration sont discutées.

MOTS-CLÉS: Effets des radiations, Systèmes embarqués, Systèmes-sur-puce, Méthodologie de test, Assurance de tenue aux radiations

TITLE: Bridging methodology from component to system-level for the assessment of radiation effects in digital systems

ABSTRACT

The objective of this work, in the context of the European RADSAGA project, is to propose a new methodology for radiation hardness assurance of digital systems. We investigate the possibility to define an intermediate approach that would combine the concept of system-level testing with the existing knowledge and best practices of component-level methods. Our methodology is developed and applied to two recent generations of system-on-modules based on 28-nm Planar and 16nm FinFET system-on-chips. A specific instrumentation was designed and added to the case study software and firmware application to improve the observability of the failures during system-level test campaigns performed with atmospheric-like neutrons, high-energy protons, pulsed laser and X-rays. The results are analyzed and the lessons learned from the experimental campaigns are summarized. Finally, the methodology limitations and possible improvements are reviewed.

KEY-WORDS: Radiation Effects, Embedded Systems, System-on-Chip, Testing Methodology, Radiation Harness Assurance