



Predictive tools and Radiation-Hardening-by-Design (RHBD) techniques for SET and SEU in digital circuits

Ygor Quadros de Aguiar

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Predictive tools and Radiation-Hardening-by-Design (RHBD) techniques for SET and SEU in digital circuits

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Le 8 décembre 2020

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Abstract

The reliability of electronic circuits is subject to physical damage or functional failures due to the influence of the application environment, such as the presence of atmospheric or space radiation. The particle interaction within silicon can lead to permanent or transient effects such as the Single-Event Effects (SEEs). Due to the intrinsic masking effects of combinational circuits in digital designs, Single-Event Transient (SET) effects were considered irrelevant compared to the data rupture caused by Single-Event Upset (SEU) effects. However, the importance of considering SET in Very-Large-System-Integration (VLSI) circuits increases given the reduction of the transistor dimensions and the logic data path depth in advanced technology nodes. Accordingly, the threat of SET must be carefully addressed along with the SEU characterization in electronics systems from space to ground applications. Also, to increase the reliability of the systems, radiation hardening techniques can be adopted in the process or design levels. The characterization process is usually experimental-test oriented, however, the need of adopting modeling simulations to study fundamental radiation effects and improve testing methodologies has led to an increase interest in developing SEE characterization methodologies based on simulation tools. Accordingly, this thesis provides a complete simulation chain based on a multi-physics and multi-scale approach to characterize electronics component against SEU/SET effects. Additionally, radiation-hardening-by-design (RHBD) techniques were evaluated and proposed at physical layout and circuit levels. The physical layout design influences the SEE generation mechanisms induced by a particle strike hence hardening techniques are widely used in the layout level to reduce the charge collection process. Besides analyzing

the gate sizing and transistor stacking, in this work, the transistor folding layout is proposed along with the diffusion splitting technique. The results have shown that folded designs can provide lower SET cross-section in addition to the higher threshold LET than the observed for the unfolded designs. At circuit-level, the implications of logic synthesis of cell-based designs are studied. Additionally, given the input dependence of the RHBD techniques, signal probability is proposed as an application-specific hardening approach in order to improve the hardening efficiency while reducing the design drawbacks and, very importantly, avoid misleading qualifications. For instance, a pin assignment optimization targeting SET effects can provide reduction on the overall SET rate without any area overhead. Additionally, selective TMR block insertion methodologies can be optimized based on the signal probability of the critical nodes and the majority voter architectures.

Résumé

La fiabilité des circuits électroniques est sujette à des dommages physiques ou à des défaillances fonctionnelles en raison de la présence du rayonnement atmosphérique ou spatial. L'interaction des particules dans le silicium peut entraîner des effets permanents ou transitoires tels que les effets d'événement singulier (SEE). En raison des effets de masquage intrinsèques des circuits combinatoires dans les conceptions numériques, les événements singuliers transitoires (SET) ont été considérés comme non pertinents par rapport à la rupture de données causée par les aléas logiques (SEU). Cependant, l'importance de considérer les SETs dans les circuits VLSI (Very-Large-System-Integration) augmente étant donnée la réduction des dimensions des transistors et de la profondeur du chemin de données logique dans les technologies avancées. En conséquence, la menace associée aux SET doit être soigneusement traitée en même temps que la caractérisation du SEU dans les systèmes électroniques des applications spatiales, avioniques et même pour les applications au sol. De plus, pour augmenter la fiabilité des systèmes, des techniques de durcissement peuvent être adoptées dans les niveaux de processus ou de conception. Le processus de caractérisation est généralement orienté vers les tests expérimentaux, mais la nécessité d'adopter des simulations de modélisation pour étudier les effets fondamentaux des rayonnements et améliorer les méthodologies de test a conduit à un intérêt accru pour le développement de méthodologies de caractérisation des SEEs basées sur des outils de simulation. En conséquence, cette thèse fournit une chaîne de simulation numérique complète basée sur une approche multi-physique et multi-échelle pour caractériser les composants électroniques contre les effets SEU / SET. De plus, des techniques de durcissement par design (RHBD)

ont été évaluées et proposées au niveau du layout physique et du circuit. La conception du layout physique influence les mécanismes de génération de SEE induits par une collision des particules. Par conséquent, les techniques de durcissement sont largement utilisées au niveau du layout pour réduire le processus de collecte des charges. Au-delà de l'analyse du dimensionnement et de l'empilage des transistors, ce travail propose l'utilisation du layout de transistors repliés ainsi que la technique de « diffusion splitting ». Les résultats ont indiqué que les designs repliés peuvent offrir une section efficace de SET inférieure ainsi qu'un LET seuil plus élevé que celui observé pour les designs non repliés. Au niveau des circuits, les implications de la synthèse logique des conceptions à base de cellules sont étudiées. En outre, étant donné la dépendance des techniques RHBD par rapport au signal d'entrée, la probabilité du signal est proposée comme une approche de durcissement spécifique à l'application afin d'améliorer l'efficacité du durcissement tout en réduisant les inconvénients de conception et d'éviter les qualifications trompeuses. Par exemple, une optimisation de l'affectation des broches qui vise les effets SET peut permettre de réduire le taux global de SET. De plus, les méthodologies d'insertion sélective de blocs TMR (Triple Modular Redundancy) peuvent être optimisées en fonction de la probabilité de signal des nœuds critiques et des architectures de votes majoritaires.

1

Introduction

1.1 Context and Overview

The reliability of electronic circuits is subject to physical damage or functional failures due to the influence of the environment, such as the presence of atmospheric or space radiation [1]. The energy deposition of a single energetic particle in the sensitive areas of a circuit can lead to destructive or non-destructive failures, known as Single-Event Effects (SEE). Initially, the first studies on circuit reliability under radiation effects were conducted for military or space applications. Back in 1962, the work developed in [2] was the first study to predict that cosmic radiation could become a threat for circuit design as the technology is scaled down into the nanometer world. And, only later in 1975, Binder et al. [3] were able to identify anomalies in the bit storage of flip-flop circuits within a satellite and attributed to the cosmic radiation effects.

Besides the radiation effects observed in space applications, anomalies in the circuit operation at sea level were also identified as early as 1978 [4]. However, the root of the anomalies observed in memory circuits were associated to the alpha particles emitted from the uranium and thorium naturally present in the package material surrounding the device. This paper used for the first time the term *soft errors* to associate the non-destructive radiation effects in electronics, and it is still largely adopted in the research

community. In the year after, Guenzer et al. [5] have shown that neutrons and protons can also induce upsets in memory elements when they trigger nuclear reactions within the circuit material. In this paper, the term *Single-Event Upset* (SEU) were first adopted to address the bit-flips observed in memory circuits due to the incidence of particle radiation.

Initially, most of the studies were focused in the radiation effects on memories due to the higher impact on the functionality of the systems. Only after nearly 10 years, since the first observation of upsets in satellites by Binder et al. [3], that the transient effects were observed in combinational logic circuits by May et al. [6]. Then, several works during the 90's started to look over the anomalies in the combinational part of logic circuits and it was getting more attention from the radiation effects research community [7]. It was in the work developed in [8] which reported that radiation-induced transients could propagate and upset latch gates. Though the transient effects were observed since 1984, the term *Single-Event Transient* (SET) was only first adopted in 1990, by Newberry et al. [9]. Historically, SEUs have been vastly studied in the literature while SETs were not given as much importance due to the intrinsic masking effects of combinational logic circuits [7]. There are three main masking effects inherent in digital circuits: i) electrical masking, in which the transient pulse is not able to propagate through a logic path due to electrical losses and attenuation of its amplitude; ii) logical masking, in which a SET will be masked due to the logic dependence of each digital signal; and, iii) latch-window masking or temporal masking, in which the SET pulse is masked by the latching window of a memory element, i.e. the SET does not reach the memory element on its writing mode operation. However, the transistor scaling, the reduced logic data path depth and increased operating frequencies have attenuated the electrical, logical and latch-window masking effects of logic circuits at advanced technology nodes [10–13]. Accordingly, several works started the development of radiation hardening techniques and mitigation schemes to reduce the impact of soft errors (both SEU and SET).

In this context, an Innovative Training Network (ITN) funded by the European Commission through the Marie Skłodowska-Curie Actions has been

approved in 2016 to foster the development of research on the radiation effects in electronics and to support the interaction among industry, university and laboratories. The ITN RADSAGA (RADiation and reliability challenges for electronics used in Space, Aviation, Ground and Accelerators) is composed by 31 partners from 11 European countries where 15 PhD projects [14]. The present thesis was developed in the framework of the RADSAGA Work Package 2 (Reliability and Testing).

1.2 Objectives and Contributions

The goal of this thesis is twofold: to propose a general methodology based on a simulation chain to predict the SEE susceptibility of circuits, and by using this methodology, to provide analysis of radiation-hardening-by-design (RHBD) techniques. The main investigated effect will be the Single-Event Transient (SET) in typical CMOS circuits such as standard-cell gates, adders, multipliers, etc.

The contributions of this thesis can be summarized as follows:

1. A simulation chain based on a multi-physics and multi-scale approach is proposed and used to analyze RHBD techniques.
2. We provided a deep analysis of RHBD approaches at layout-level such as Gate Sizing, Transistor Stacking and Transistor Folding;
3. By better understanding the input dependence of SET cross-section, strategies were proposed to improve the hardening efficiency of well-known RHBD techniques. For instance, we have shown that by identifying the input dependence of majority voter architectures, Triple-Modular Redundancy (TMR) insertion optimization can be improved to obtain higher fault coverage and less overhead, which is very crucial when adopting radiation hardening by design techniques;
4. We discussed how the proposed methodology can be integrated into a VLSI design methodology in order to obtain a reliability-driven synthesis, whether during the physical or the logic synthesis. Also, a pin

assignment optimization based on the signal probability is proposed to improve the circuit reliability with no overhead in area.

5. A test chip design was completely developed using a commercial 65nm bulk CMOS technology. The chip contains 18 blocks of circuits: 10 majority voter architectures, 4 circuits to study the complex-logic gate layout effects and 4 circuits to study the transistor folding layout effects. Due to limited time, experimental results were not available to be included in the thesis.

1.3 Thesis Organization

In Chapter 2, the natural radiation sources and the basic mechanisms of particle interaction with matter are described to introduce to the radiation effects analyzed in this work. Also, the well-known prediction models and the proposed prediction methodology is discussed in this chapter. Chapter 3 provides a report on well-known and state-of-the-art radiation hardening techniques. After reviewing some hardening techniques, Chapter 4 and Chapter 5 provide our analysis of some RHBD techniques. The layout-based techniques such as Gate Sizing, Transistor Stacking and Transistor Folding are explored specifically in Chapter 4. On the other hand, the circuit-level techniques are explored in Chapter 5. The proposed improvements of the radiation hardness of RHBD techniques is presented in Chapter 6. To conclude, besides providing a summary of the results obtained in this thesis and the list of publications, Chapter 7 provides a discussion on prospective future research in this subject.

2

Radiation Effects and Prediction

The evaluation of the reliability of circuits operating in harsh environments is a crucial process in order to prevent functional failures and even catastrophic events. This chapter provides the foundations to understand the dynamics of natural radiation environments and the prominent effects observed in electronic components.

2.1 Radiation Environments

In this section, space and atmospheric radiation are discussed in terms of radiation sources, particles and fluxes. For projects aiming at the near-Earth space environment, there are three main source of radiation that need to be considered as shown in Figure 2.1: the *Solar Energetic Particles* (SEPs), *Galactic Cosmic Rays* (GCRs) and geomagnetically trapped particle radiation (*Van Allen's radiation belts*). The SEPs are particles continuously released by the sun due to its activity. While the GCRs are radiation coming from outside of our Solar System and it is believed to be product from supernova explosions, the Van Allen's radiation belts are composed of both solar and galactic cosmic radiation trapped by the Earth's geomagnetic field. The Sun activity is the main radiation modulator of the space environment in

the vicinity of Earth, influencing not only on the solar particles, but also on the fluxes of GCRs and the radiation trapped by the Earth's magnetosphere. Thus, to understand the dynamics of the natural space radiation environment, it is imperative to study the solar activity, which is closely related with the number of observable sunspots in the photosphere, i.e. the sun's surface.

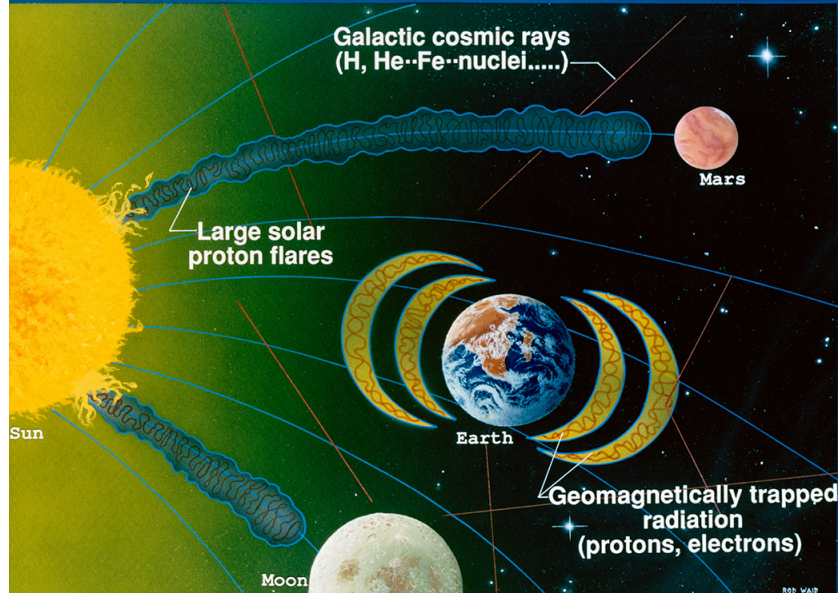


Figure 2.1: Space Radiation Environment [15].

The sun has a cyclic activity of approximately 11 years, divided into solar maximum (about 7 years) and solar minimum (about 4 years). Based on the sunspot number (also known as *Wolf number*), Figure 2.2 shows the current solar activity, cycle 24, and the predictions for the following cycle. The sun is continuously emitting low-energy particle radiation composed mostly of protons and electrons, the so-called *solar wind*. However, solar particle events, such as the Coronal Mass Ejection (CME) and solar flares, are rare events in which a massive number of high energetic particles are emitted and can reach the Earth's atmosphere in a relatively short time (few hours or days). The intensity of solar winds and the frequency of solar particle events are directly dependent on the solar activity, i.e. the number of sunspots. For instance, CMEs and solar flares are known to occur more often

during the solar maximum, especially in the declining phase [36 uznanski]. On the other hand, the GCR modulation shows an anti-correlation with the solar activity: a higher activity leads to a lower GCR flux and vice-versa [16–18]. Generally, GCRs present the lowest particle flux, however, as it is composed of high energetic particles, they are highly penetrating particles which shielding technology is not an effective solution to reduce radiation exposure. Thus, despite its low flux, GCRs are a threat for space-borne electronics and human health.

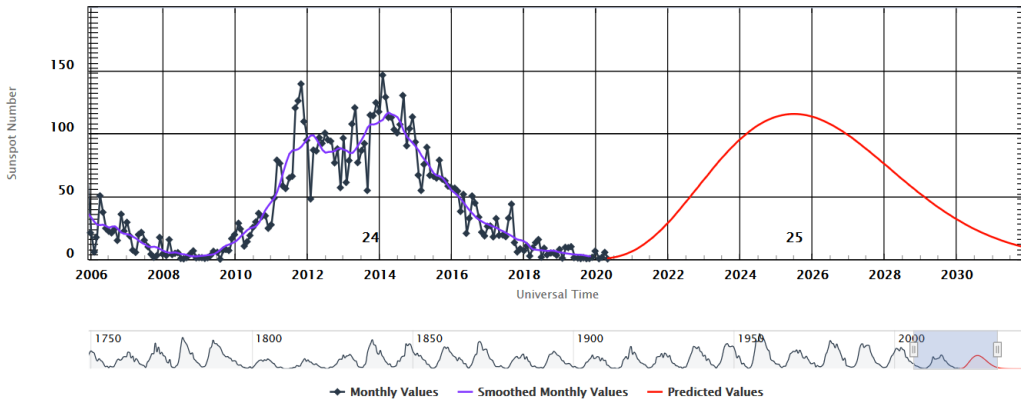


Figure 2.2: Solar Cycle Flux Progression: current solar cycle 24 and prediction of cycle 25 based on the sunspot number [19].

The trapped particle radiation in the Van Allen’s belts are clearly separated into two different belts: the outer belt consisting mainly of electrons from solar winds, and, the inner belt composed mostly of protons product of cosmic-ray interactions in the Earth’s atmosphere [20]. As can be seen in Figure 2.3, the outer belt is wider than the inner belt, and it is also the most unstable due to the weaker influence of the Earth’s magnetosphere. Similarly as the GCRs, the trapped radiation is also modulated by the solar activity: the higher the activity, the higher is the electron intensity and the lower is the proton intensity [21]. The Van Allen’s radiation belts have been always a concern for space mission designs due to its impact on the electronics reliability. Protons are able to induce a variety of effects ranging from parametric degradation due to observed dose to even singular effects. These radiation effects are further detailed in the next section. Another important

aspect to be considered in the design of components for space applications is the anomaly present in the Earth's magnetosphere. Due to a displacement and misalignment between the Earth's geomagnetic and rotational axes, energetic particles can reach low altitudes in the south of Brazil in response to a weakness in the magnetic field over South America (and, in the same way, a stronger field is observed in Northern Asia). This phenomenon is known as South Atlantic Anomaly (SAA). The SAA is a dominant contributor to the radiation damage observed in spacecraft in the low-earth orbit (LEO). This anomaly is illustrated in Figure 2.4 in which, by using the AP8 MIN model, the high proton flux is identified at altitudes as low as 500 km and below.

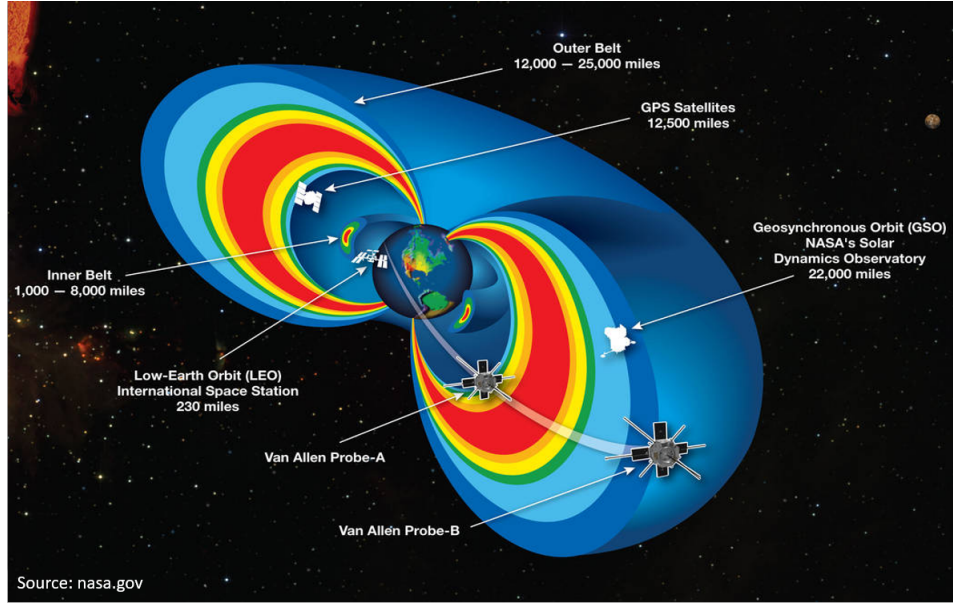


Figure 2.3: Van Allen's Radiation Belts [15]

When the cosmic radiation enters the Earth's atmosphere, they collide with the atmospheric atoms (such as nitrogen and oxygen) and produce secondary radiation. Similarly, these secondary particles can also interact with the atmospheric atoms and produce new secondary particles as shown in Figure 2.5. This phenomenon is known as *cosmic ray air shower*. Historically, the secondary neutrons have been the most expressive contributor to the radiation effects observed in the atmospheric environment. However, with the

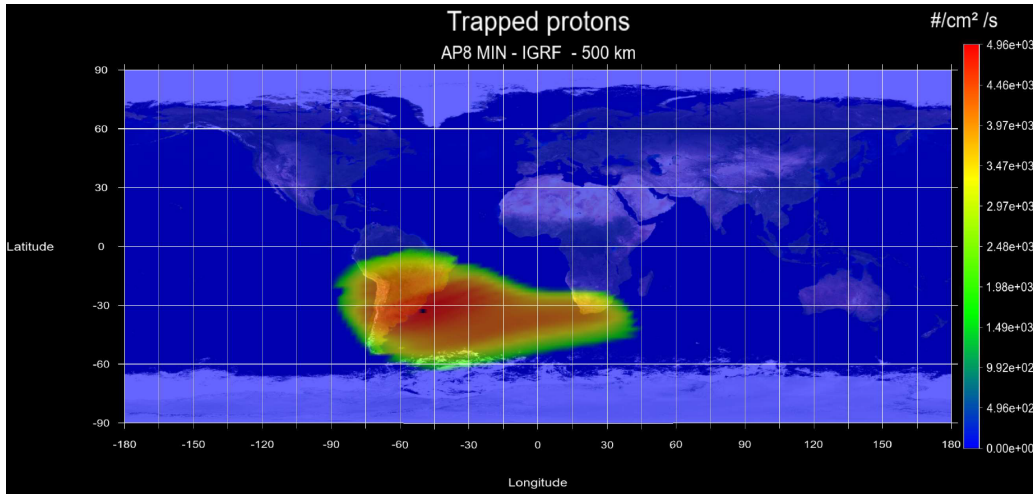


Figure 2.4: Flux intensity map for the > 10 MeV channel at 500 km altitude. Higher proton flux in the South Atlantic Anomaly (SAA) region. The graph is obtained using the AP8 model available in the OMERE software tool [22].

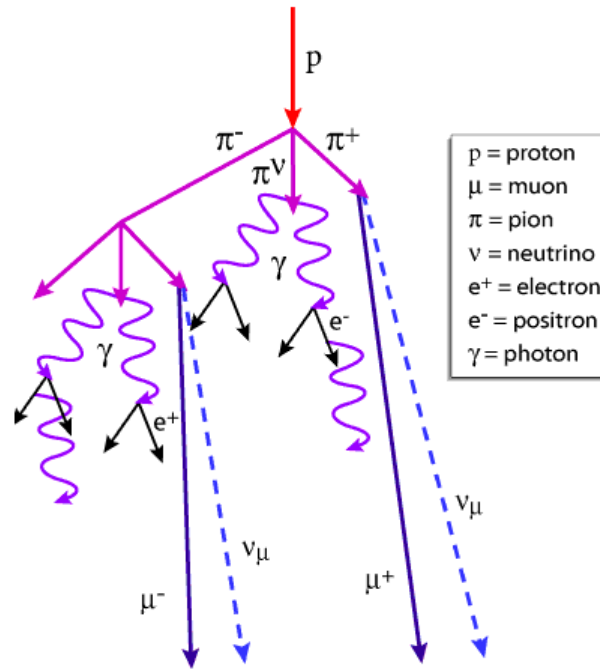


Figure 2.5: Secondary radiation induced by a proton interaction with an atmospheric atom and leading to a cosmic ray air shower [23].

technology scaling, muons have shown an increased capability of inducing radiation damage on microelectronics and, thus, they can also be considered a threat to the system reliability [24]. The neutron density increases as the altitude decreases until about 20km which the peak density is reached [25]. At ground level the density decreases to 1/500 the peak flux.

2.2 Radiation Effects

In the previous section the dynamics and the composition of the radiation environments in space and atmosphere were presented. This section provides an introduction to particle interaction physics related to the radiation effects observed in electronic components. These effects can be classified into two groups: Cumulative effects, comprising the Total Ionizing Dose (TID) and Displacement Damage (DD); and, Single-Event Effects (SEEs), a group of effects in which a single particle hit is able to disturb the correct operation of electronic devices. In this thesis, the research is focused on the study and mitigation of SEEs, more specifically the non-destructive effects, i.e. the *soft errors*. Accordingly, the following sections will be particularly directed to understand these effects.

2.2.1 Energy Deposition

Particle interactions with matter can be classified into two groups when considering SEEs: (1) interactions induced by charged particles; and, (2) induced by uncharged particles, i.e. neutrons. When a charged particle, such as protons and heavy ions, travels through the matter, it loses energy as it collides with the electrons and nuclei of the target material [26]. These collisions can lead to the generation of electron-hole pairs when sufficient energy is transferred in order to eject the electron from the valance band. This phenomenon is known as *ionization*. The main mechanism responsible for this energy transfer is the inelastic collision due to the higher probability of interaction with the atomic electrons rather than the atomic nuclei itself [26]. However, protons can also lose energy through nuclear reactions. In the

end of the interaction path, when the particle has lost most of its energy, the main energy transfer occurs due to nuclear elastic collisions, i.e. the particle collides with the nuclei and it can lead to the displacement of the lattice.

These interactions are responsible for the energy loss and the particle slowdown. The amount of energy that a particle can lose per unit length travelled corresponds to what we call the *stopping power*. There are two classifications based on the nature of the energy loss: (1) the *electronic stopping power*, for the energy loss induced by collisions with the electrons of the target material, and (2) the *nuclear stopping power*, for the energy loss due to nuclear elastic collisions. For the radiation effects concerned in this thesis, the nuclear stopping power does not provide a great contribution. Thus, only the electronic stopping power, also known as *Linear Energy Transfer* (LET) in the radiation effects community, is taken into consideration [26]. The LET measures the energy deposition induced by the ionization process and it can be described as the following equation:

$$\text{LET} = -\frac{1}{\rho} \frac{dE}{dx} \quad (2.1)$$

where ρ is the density of the target material, ΔE is the energy loss, and Δx is the ionizing path length. The LET unit is given in megaelectronvolts square centimeter per milligram ($\text{MeV.cm}^2/\text{mg}$). For electronics, the silicon density is used, $\rho_{\text{Si}} = 2.32 \text{g.cm}^{-3}$. The LET depends not only on the particle type, but also on its energy and the target material where the ionization takes place. In Figure 2.6, the variation of LET is shown as function of the ion energy in silicon. The LET of a particle increases as the energy increases until it reaches the Bragg peak, the highest LET value. Then, it decreases along with the increase in particle energy. It can be noticed that different ion species with different energies can provide the exact same LET value.

So far, only the *direct ionization* has been discussed, i.e. when the incident particle is the primary contributor to the creation of electron-hole pairs. However, high-energy protons and neutrons can experience nuclear reactions resulting in secondary particles that may be able to ionize the matter. This process is known as *indirect ionization* and it is also highly

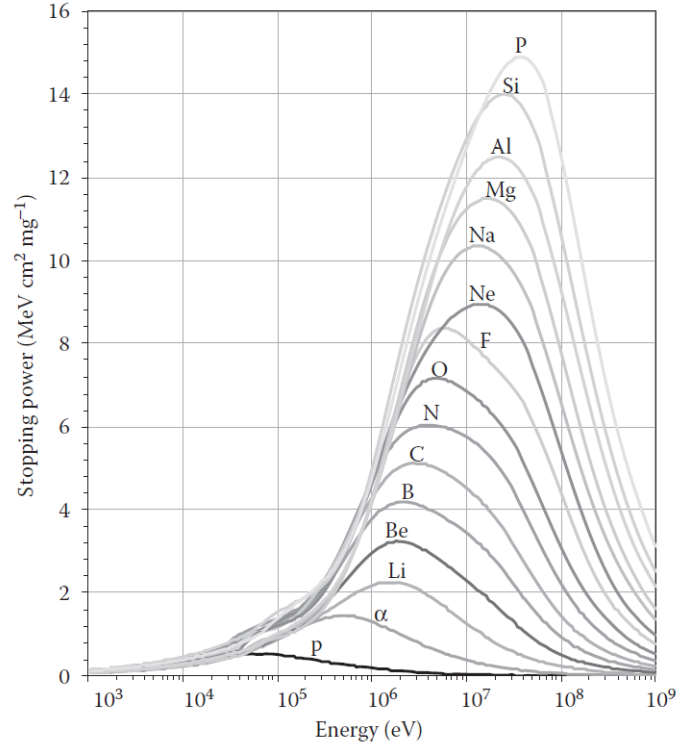


Figure 2.6: Variation of Linear Energy Transfer (LET) as function of energy for different ions in silicon [26].

important in the analysis and qualification of radiation effects on electronic components. Figure 2.7 illustrates the direct and indirect ionization of a heavy ion and a neutron, respectively. Protons interact through both direct and indirect ionization depending on its energy.

The energy deposition in the semiconductor leads to a nearly linear path of electron-hole pairs (ehp). The minimum energy required to generate a electron-hole pair can be estimate based on the band-gap energy E_g of the material using the Equation 2.2 [27]:

$$E_{ehp} = 2.73E_g + 0.55eV \quad (2.2)$$

For silicon-based devices, the silicon band-gap energy E_g is equal to 1.11 eV, therefore, the ionization energy E_{ehp} is approximately 3.6 eV/ehp. The higher the band-gap energy of the material, the higher is the energy required

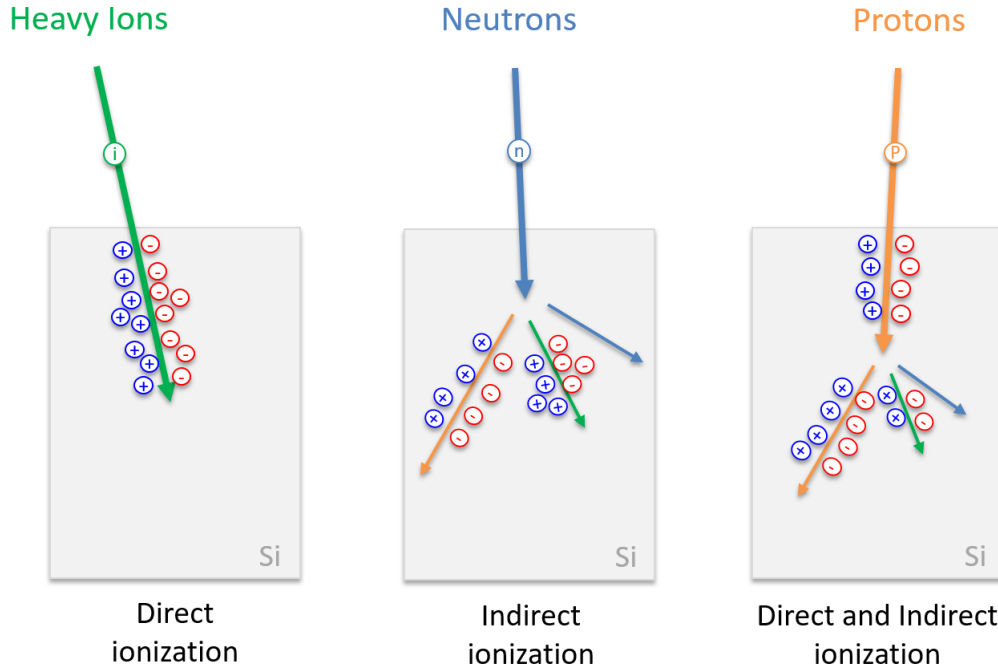


Figure 2.7: Representation of Direct Ionization and Indirect Ionization for heavy ions, neutrons and protons interaction with matter (Si stands for Silicon).

to ionize the matter. This explains why wide-bandgap electronics such as the SiC- and GaN-based devices show a better radiation performance.

2.2.2 Charge Collection

After the energy deposition, the released carriers are transported and collected by the junctions of the device. There are two main transport mechanisms to be considered in SEEs, the *drift* and the *diffusion*. Drift is a mechanism governed by the electric field present in the p-n junction of the sensitive devices. For instance, when a particle hits directly the sensitive collecting area of the circuit, the carriers will be rapidly collected due to the high electric field present in the reverse-biased p-n junctions. On the other hand, diffusion is a carrier transport mechanism governed by the carrier concentration gradients. It means that the carriers will transport from regions with high to low carrier concentration. In Figure 2.8, the ionization

process followed by carrier drift and diffusion is illustrated for a ion strike in a reverse-biased p-n junction .

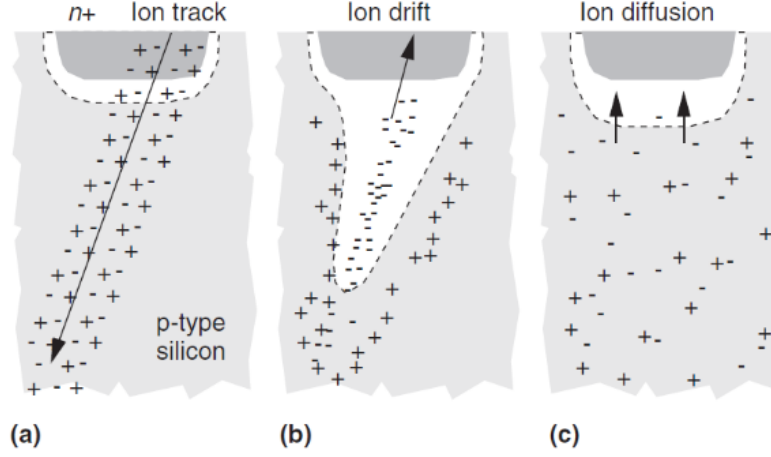


Figure 2.8: Charge collection mechanisms due to an ion strike in a p-n junction [28].

If the particle strikes in or near the p-n junction, the charge collection can be enhanced due the funneling effect in the electrical field which increases the depletion region and improve the collection efficiency (Figure 2.8 (b)). The drift and funneling effect are two very fast process due to the high electric field present in the junction. Following these processes, the remaining carriers are collected by the diffusion process or recombined. The minimum collected charge necessary to observe a SEE in a component is known as the critical charge Q_{crit} .

2.2.3 Charge Sharing and Pulse Quenching Effect

With the technology integration, transistors are placed more closely together and the critical charge is reduced. As a consequence, a single incident particle is able to induce sufficient charge collection from multiple electrodes. This phenomenon is known as charge sharing effect. The work developed by Amusan et al. [29] provides an analysis of the charge sharing effect in adjacent devices for NMOS and PMOS transistors. In Figure 2.9 (a), the outline of two adjacent NMOS devices is illustrated and two notations are given: the

active device/node, for the device that got hit by a particle and it is actively collecting the carriers; and, the passive device/node, for the device that was not hit by the particle but it is passively collecting the diffused carriers. In the Figure 2.9 (b) the collected charge is shown for the active and passive devices when PMOS and NMOS transistors are used. Clearly, it can be seen that the passive PMOS is able to collect more than a passive NMOS device. For instance, the passive PMOS collected about 40% of the charge collected by the active PMOS device, while less than 25% is collected by the passive NMOS transistor. The authors attributed this difference to the difference of the carrier diffusion coefficient of electrons and holes, and, to the bipolar amplification effect that enhances the charge collection in the PMOS devices [29][30].

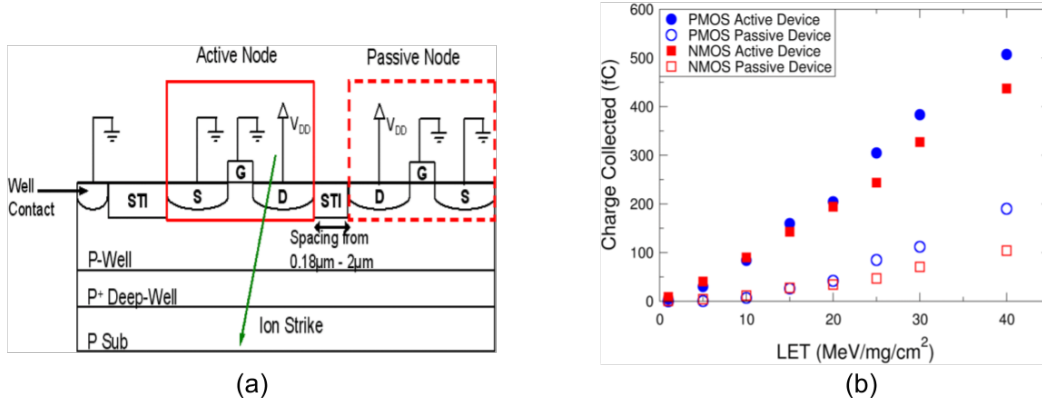


Figure 2.9: (a) outline of two NMOS adjacent devices and (b) charge collected for PMOS and NMOS as active and passive devices [29].

Though the charge sharing mechanism is responsible for the increase of SEE sensitivity due to multiple SETs or multiple SEUs, it was shown that it can also reduce the SET pulse width in combinational cells [31][32]. Due to the similar time constant for the circuit delay and the diffusion process, the radiation-induced transient is able to activate the charge collection by electrodes from following stage of circuits in such a way that the resultant transient is shortened (i.e., quenched). This phenomenon is known as Pulse Quenching Effect (PQE) and it can be better understood by analyzing the Figure 2.10. To observe the PQE, the involved circuits must have an inverting

relationship as shown in the inverter chain in Figure 2.10. The charge sharing and pulse quenching effect are two very important mechanisms necessary to understand the SEE sensitivity of state-of-the-art electronic components. Accordingly, both of them will be extensively used to discuss the results observed in this thesis.

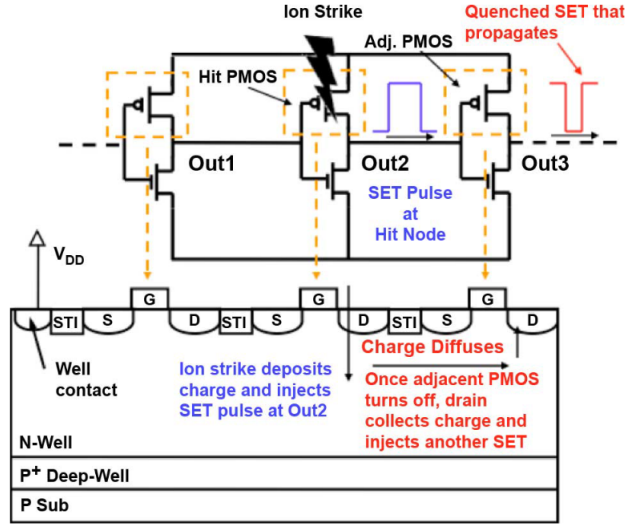


Figure 2.10: SET Pulse Quenching Effect in a inverter chain [31].

2.2.4 Masking Effects

Besides the charge sharing effects, the inherent masking effect ability of digital circuits are also fundamental when studying soft errors. They can be classified into three effects: *electrical masking*, *logical masking* and *latching-window masking* (also known as temporal masking).

Logical masking effect

Combinational circuits provide the logical masking effect when the SET event occurs in a logic gate where its output does not determine the output signal of the subsequent logic stage. For instance, a 2-input NOR gate has its output determined whenever one of its input signal is evaluated to 1, i.e. whenever one input signal is at logic 1, the output evaluates to logic

0. This phenomenon can be better understood by analyzing the block of combinational logic in Figure 2.11. A SET event occurs in the first NOR gate, in which the output signal initially was evaluated to logic 0. The SET pulse propagates to the next logic stage, which is also a NOR gate. However, this logic stage has already been evaluated to logic 0 due to the input signal provided by the NAND gate. Since the output of the second NOR gate has already been determined by the one of its inputs, the SET pulse is not able to change it, hence it is logically masked and cannot propagate to the next logic stage and reach a memory element, for instance. Although the effectiveness of this mechanism, recent technologies have shown a reduction in the logic depth of combinational circuits, thus logical masking effect has been reduced [33].

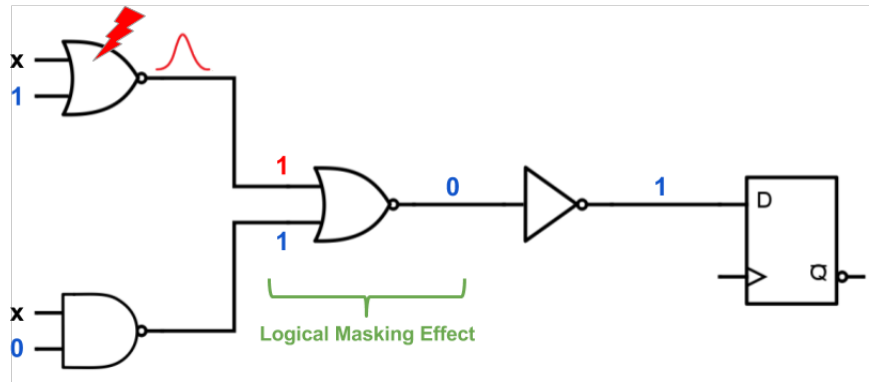


Figure 2.11: Illustration of the logical masking effect of a SET event in a 2-input NOR gate within a block of combinational circuit [34].

Electrical masking effect

The electrical masking effect is another phenomenon that can occur in a combinational circuit and prevent the propagation of a SET pulse. Due to electrical losses, a SET pulse suffers from magnitude and amplitude attenuation and it might not be able to propagate to a memory element as observed in Figure 2.12. The initial SET pulse has its waveform affected by each stage of logic, being vanished near the memory element. In this case, the propagated SET pulse did not have sufficient amplitude to upset

the memory element due to the electrical masking effect. However, it was shown that not only the transient pulse can suffer from attenuation, but it can also experience broadening effect, the so-called Propagation-Induced Pulse Broadening (PIPB) [35, 36]. The pulse width of the SET depends on the restoring current of the struck circuit and its capacitive load (fan-out). Larger capacitance can lead to increase of the critical charge, however it can lead to pulse broadening due to the longer time to restore the output voltage [37].

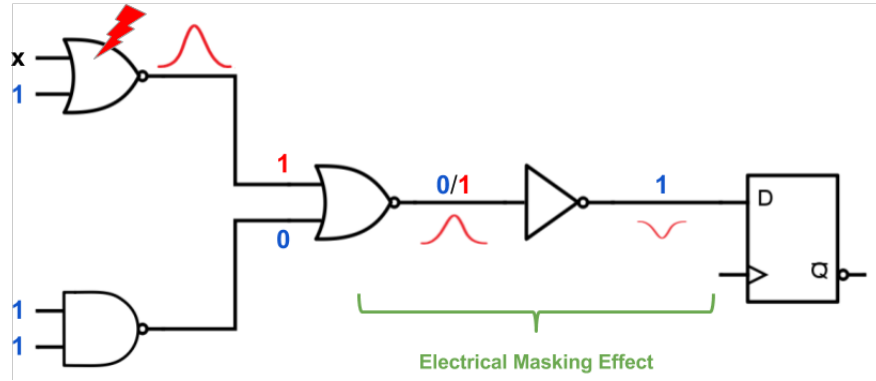


Figure 2.12: Illustration of the electrical masking effect of a SET event due to electrical losses in a logic path [34].

Latching-window masking effect

In the end, if the SET pulse has not been masked logically or electrically, it might still be masked by the latching window of a memory element. This window is composed by the setup time (T_{setup}) and the hold time (T_{hold}) around the edge of the clock signal of a flip-flop circuit. If the SET pulse does not arrive during this latching window, it will not be able to induce a bit upset, i.e. a change in the stored bit value. Figure 2.13 illustrates this phenomenon. Due to the high operating clock frequencies in advanced technologies, the latching-window effect is expected to be reduced given the short T_{setup} and T_{hold} of FF designs.

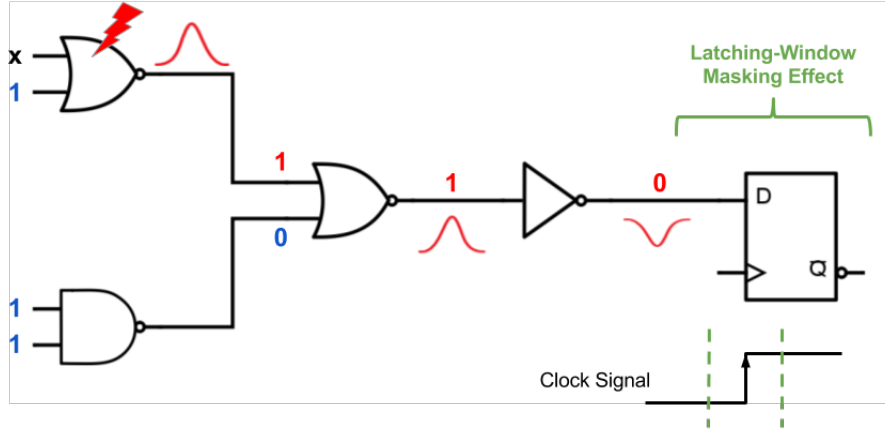


Figure 2.13: Illustration of the latching-window masking effect of a SET pulse by a flip-flop (FF) circuit [34].

2.3 Modeling and Prediction

The usage of modeling and simulation has always been present in the study of physical phenomena, especially in the field of electronics to study the behavior of MOS transistors [38, 39]. Further, with the increase of complexity of very-large-scale-integration (VLSI) system, it is increasingly necessary to use the support of simulation studies to verify and assist the development of such circuits. In this sense, Monte Carlo simulation tools have solid foundations to be used in the study of radiation effects on electronics [40]. There are many works in the literature which propose the research of radiation effects on electronics exploiting simulations and avoiding the time consuming and expensive radiation campaigns [41–48]. Mixed-mode Technology Computer-Aided Design (TCAD) simulations have been vastly used to understand the main mechanisms in SEEs on electronics. However, Monte Carlo simulation codes can have a computation time several orders of magnitude lower than TCAD simulations [40, 47]. The randomness and stochastic nature of particle interaction with the matter is a perfect fit for Monte Carlo (MC) simulations. Accordingly, a diverse number of modeling based on the MC method have been proposed to estimate and predict the radiation robustness of electronics [41–44, 47]. In contrast to deterministic models, in the MC

method, random sampling and statistical modeling are used to approximate solutions for stochastic problems, such as in particle physics.

Historically, the well-known rectangular parallelepiped (RPP) analytical model [49], also known as chord-length model, has been vastly used to analyze and predict the radiation response of electronic components [50]. In this approach, the device is assumed to have a well-defined sensitive volume (SV) in the form of a rectangular parallelepiped. The ionization track path is determined by the depth of the SV and the incidence angle, θ . It is assumed that charge collection induced by diffusion from ion striking outside the RPP is negligible and thus not considered. Also, the LET is assumed to be constant over the ionization path so that generated charge within the SV can be calculated by the product of the LET value and the ionization path length, l . In the case of a normal incidence, the ionization path length is equal to the sensitive volume depth, d . Thus, the deposited charge can be calculated using the Equation 2.3. Accordingly, if sufficient charge is deposited inside the SV, i.e. if the deposited charge Q_{dep} is superior to the critical charge Q_{crit} , a SEE is assumed to be observed in the circuit.

$$Q_{dep} [\text{pC}] = 0.01035 \cdot LET [MeV.cm^2/mg] \cdot d [\mu m] \quad (2.3)$$

Despite the popularity and its widespread use, the RPP model has turned out to be inadequate when used in advanced technology due to the complex geometry of transistors, the small sensitive volumes and the close proximity of devices. Emerging effects such as charge sharing due to multiple node collection and parasitic bipolar amplification have limited the application of the RPP approach in some cases. One possible extension to this model is the Integral Rectangular Parallelepiped (IRPP) model [51], in which not only a single SV is defined, but a collection of multiple SVs. The IRPP method is widely used to predict SEE rates in the radiation effects community and it is the standard method specified by the European Cooperation for Space Standardization (ECSS) [52]. Alternatively, the diffusion-collection model [53] has been proposed to address the limitations observed in the analytical approaches. By considering a physics-based Monte Carlo simulation,

Table 2.1: List of simulation tools dedicated to study radiation effects on electronics

Ref.	Tool	Institution	Radiation Effects
[54]	DASIE	AIRBUS	SEU
[55]	SEMM-2	IBM	SEU
[56]	MRED	Vanderbilt Univeristy and NASA/GSFC	SEU
[43]	MC-ORACLE	Université de Montpellier	SEU/SET
[57]	TIARA-G4	Aix-Marseille University and STMicroelectronics	SEU/SET
[58]	FLUKA	CERN and INFN	SEU
[42]	MUSCA-SEP3	ONERA	SEU/SET/SEL

it is possible to account for the multiple node charge collection and emerging effects observed in advanced technology nodes. This method will be further explained in the next section, as it is adopted in our prediction methodology. In Table 2.1, a non-exhaustive list of simulation tools dedicated to model and study radiation effects on electronics is presented. Further details adopted in each tool can be found in its respective reference. In this thesis, the MC-Oracle tool [43] is used to account for the energy deposition and charge collection in our SEE predictive methodology.

2.4 Proposed Prediction Methodology

To accurately assess the SEE immunity of digital circuits, it is highly recommended to adopt a multi-scale and multi-physics methodology due to the plurality of complex effects involved at silicon and circuit level [56, 42]. Different approaches taking into consideration the aspects from the particle interaction physics to the circuit layout design is explored in different codes as shown in [47]. As aforementioned, due to the technology scaling, emerging effects as parasitic bipolar amplification (PBA) and charge sharing effects need to be carefully addressed [44, 59, 60]. Therefore, layout information from the circuit design is an important determinant on the SEE prediction of electronic circuits. Accordingly, in this work a layout-based methodology

to assess the SEU/SET robustness of digital circuits using the MC-Oracle prediction tool [43] is proposed. MC-Oracle is a Monte Carlo simulation code developed to analyze the SEU/SET immunity of electronics based on the particle interaction physics within the sensitive devices. As neutrons, protons and ions can be simulated, the SEU/SET sensitivity can be calculated for different radiation environments such as space, atmosphere, ground and accelerators. The energetic particles when interacting with silicon material go through ionization process (i.e., generation of electron-hole pairs), in which parasitic charge is deposited and can be collected by the sensitive transistor junctions. Since neutrons are uncharged particles, they do not experience coulomb's interactions with orbital electrons. Consequently, neutrons cannot ionize matter directly, howsoever it is still considered as a threat for electronics in space and aviation applications due to the indirect ionization [61, 62]. Considering neutrons can experience nuclear reactions with the material target nuclei, they can induce SEE through the ionization of secondary products of nuclear reactions. Also, as it presents no electromagnetic interaction, neutrons are highly penetrating particles. In the MC-Oracle, the ionization process is modeled using tables of range and electronics stopping power pre-calculated with the Stopping and Range of Ions in Matter (SRIM) code [63]. For the nuclear reactions induced by protons or neutrons, a pre-calculated nuclear database for a given energy range is built based on the Detailed History Of Recoiling Ions induced by Nucleons (DHORIN) code [64]. The location of each nuclear reaction is determined considering the information from the nuclear database in which the mean free path of each particle, i.e. the average distance travelled between collisions, is estimated from the nuclear cross-section. Once the energy deposition is modeled by ionization and nuclear reactions, the charge transport and collection are modeled by the drift-diffusion mechanism. Accordingly, in the MC-Oracle, hundreds of thousands of particles interactions are simulated and the resulting ionizing electron-hole path is numerically divided into small fragments and the transport of the carriers is calculated [43, 65]. A simplified representation of the layout-based analysis using MC-Oracle is shown in Figure 2.14. Given a GDS (Graphical Design System) file of the circuit, the collecting

drain area of transistors can be identified and extracted to be submitted as input to the MC-Oracle calculations. In this example, the layout design of an inverter logic gate is shown in Figure 2.14 (a). The drain area of the PMOS and NMOS devices are extracted as shown in the Figure 2.14 (b). Then, considering a heavy-ion simulation, Figure 2.14 (c), the resulting ionizing track is numerically divided into small fragments in which the generated charges diffuse to the collecting drain areas. Each collecting area is divided into elementary collecting areas and the induced transient current is calculated from the integration of the collected charge along the ionizing track for each elemental section of the collecting area, Figure 2.14 (c).

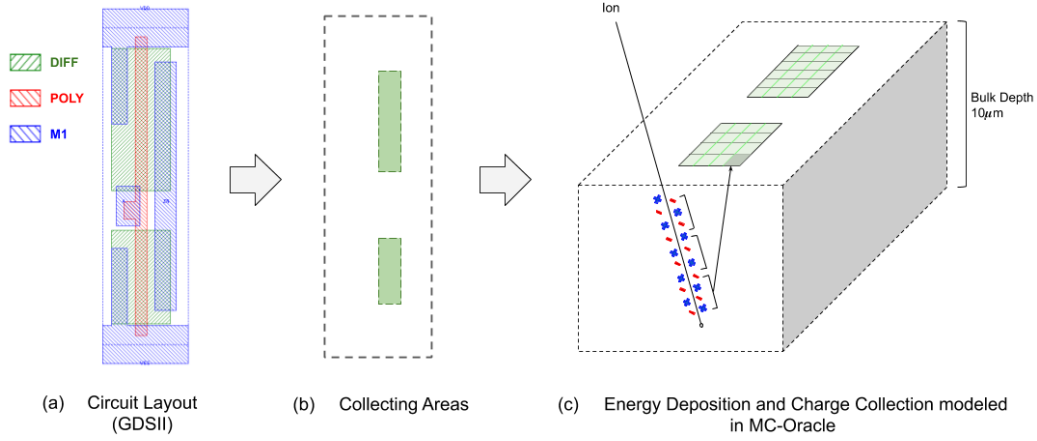


Figure 2.14: Representation of the extraction of the collecting areas from the circuit design (GDSII file) and the energy deposition and charge collection calculation in the MC-Oracle tool. Only the active diffusion (DIFF), polysilicon (POLY) and metal 1 (M1) layers are shown in the circuit layout for the sake of simplicity.

In summary, the transient current I_D of each collecting drain node is obtained following the Equation 2.4 [66]:

$$I_D(t) = q \cdot v \iiint \text{LET}(l) \frac{e^{-\frac{r^2}{4Dt}}}{(4\pi Dt)^{\frac{3}{2}}} dx dy dl \quad (2.4)$$

where q is the elementary charge, v is the carrier velocity in the junction, $\text{LET}(l)$ is the ion Linear Energy Transfer (LET) along the ion track,

r is the distance between the elemental section of the collecting area and the ion track, and D is the ambipolar diffusion coefficient. For each particle event, MC-Oracle calculates the induced transient current for each collecting area of the circuit design and stores this information in a SET current database. Therefore, multiple-node charge collection effects such as charge sharing mechanism and pulse quenching effects can be evaluated using this tool [59]. A simplified full custom design flow with the SEE characterization methodology using MC-Oracle is shown in Figure 2.15. Given the specifications concerning the system functionality and reliability (including the radiation environment), the design engineer can start the circuit design process. Once the physical verification, i.e. Design Rule Check (DRC), Layout versus Schematic (LVS) are performed, the parasitic extraction of the netlist description and GSDII file can be obtained and submitted to the SET characterization.

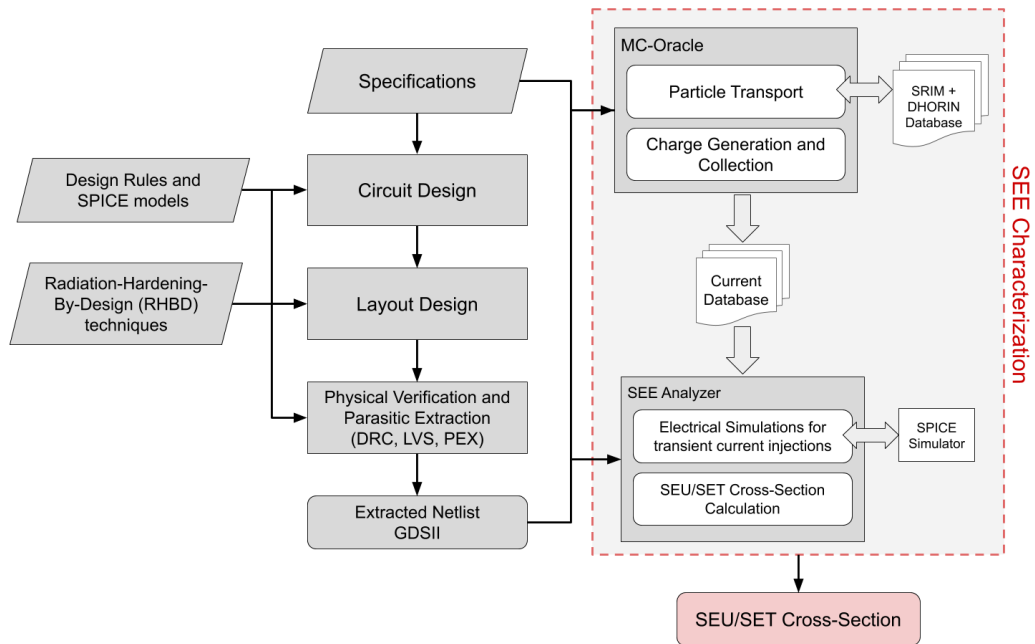


Figure 2.15: Simulation chain proposed as the SEE Prediction Methodology

The proposed SET characterization is divided into main two steps: first, aiming to build an SET current database, the MC-Oracle tool is used to perform the simulation of the particle transport and the charge collection in

the collecting areas of the circuit; second, an SET analyzer is responsible for the SPICE injection campaign using the current database provided by MC-Oracle. The main inputs to the SET characterization are: technology model, radiation environment specification, layout design (GSDII) and extracted netlist description of the circuit. For the SET cross-section and pulse width measurement, only the transient pulses with voltage peak higher than half of the supply voltage are considered, but this criterion can be easily adjusted to the needs of the user. Different hardening techniques can be adopted to prevent that critical electronics systems, such as spacecrafts and avionic control systems, fail due to the occurrence of SEEs. Accordingly, the proposed predictive SET characterization methodology allows the investigation of the hardening effectiveness of Radiation-Hardening-By-Design (RHBD) techniques at layout level and circuit level.

2.5 Conclusion

In this chapter, the fundamental concepts related to the study of radiation effects in electronics are discussed. Initially, the dynamics and composition of the space and atmospheric radiation environment are presented. The Sun is the main modulator of the radiation environment in space and Earth. For missions aiming the surrounding of the Earth, the Van Allen's radiation belts are also one of the important sources of radiation effects observed in on-board electronic systems. In addition, for low-orbit and atmospheric applications such as satellites and aviation, a high proton flux is expected in the South Atlantic Anomaly region. Depending on the nature of the incident radiation, direct and indirect ionization can be triggered within the electronic components, leading to energy deposition and charge collection by the electrodes of the critical devices. Initially, the Single-Event Transient (SET) effect showed less of a concern due to the inherent masking effect capability of combinational circuits. However, with the technology integration, the effectiveness of these effects is reduced and a higher impact of SET is observed in today's electronic technology.

After discussing the main mechanisms involved in the radiation effects

in electronics, the modeling and application of prediction methodologies are presented. Due to the increased computational power of recent technologies and the advanced particle physics models, Monte Carlo based software tools are increasingly being employed to study and predict the radiation sensitivity of circuit designs. The simulation chain used as the SEE prediction methodology was then presented. A combination of particle physics simulations issued from the MC-Oracle tool and electrical simulations from a SEE analyzer provides the valuable information for the SEE characterization of the designs studied in this thesis. Given the importance of the layout design for the consideration of SEE and, very importantly, for the application of radiation hardening techniques, the methodology adopts as input not only the circuit description in netlist format, but also the layout design information provided from the GSDII file.

3

Radiation Hardening

Due to the extensive usage of electronics systems in harsh environments, mitigation techniques against radiation effects have been vastly investigated in literature [67–70]. When components or systems are designed and validated to operate in radiation environments, they are denominated as *radiation-hardened*, or *rad-hard* for short. Radiation hardening strategies can be explored from fabrication process modifications to different circuit design implementations. A classification according to the abstraction level in the application design is proposed by the European Cooperation for Space Standardization (ECSS) [71] and shown in the Figure 3.1. The modifications in the circuit manufacturing process such as variation of doping profiles, substrate technology and the usage of different materials are examples of well-known Radiation-Hardening-by-Process (RHBP) techniques. However, besides its higher cost, RHBP are typically several generations behind the state-of-the-art CMOS technology, leading to low-grade performances. On the other hand, Radiation-Hardening-by-Design (RHBD) techniques have been shown effective in providing hardness against radiation effects with the advantages of highly-integrated technologies [70]. The RHBD techniques can be adopted from the physical layout level aiming to reduce the radiation-induced charge collection to techniques at the system level where the main goal is to mask the errors and prevent a system failure. It is important to highlight that some of the RHBD techniques discussed in this chapter can be

applied in different design levels. During the design process, the suitability of the hardening techniques is determined depending on a variety of constraints, such as the radiation environment, the acceptable error rate for the mission (availability of the system), the design time and resources.

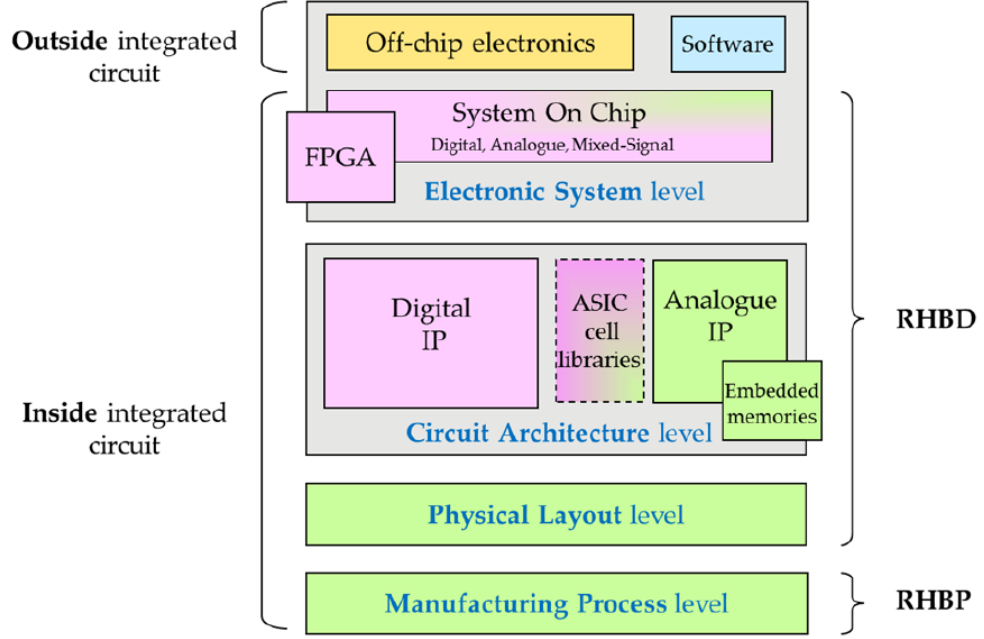


Figure 3.1: Classification of hardening techniques based on the abstraction level: from manufacturing process to system level [71].

In the last decade, the rad-hard paradigm shift from process to design level has been boosted by a growing market in the spacecraft industry known as the *New Space*. Historically, the government space agencies have played the biggest hole in this industry. However, the New Space characterizes as the commercialization of the space industry and the consequent increase of private companies developing low-cost technologies for space and providing a broader accessibility to these technologies. Consequently, a wide range of space-based applications is emerging and increasing the functionality and complexity of space systems. In order to follow this growing market, public and private actors have increased the adoption of the so-called Commercial Off The Shelf (COTS) components due to their performance, availability, cost and lead time. For instance, it is estimated that over 20% of the Electrical,

Electronic and Electro-mechanical (EEE) components in ESA satellites are COTS [72]. The COTS components are defined as any component designed for commercial purpose-only, not following any military or space standard, i.e. not radiation hardened. In this context, design mitigation techniques must be employed to ensure the functionality and performance of the system under radiation effects. In this chapter, a review on the foundations and state-of-the-art radiation hardening techniques is provided. The main goal of this thesis is to analyze and propose hardening techniques at the design level, more specifically at physical layout and circuit architecture level. Accordingly, a special attention is given to the RHBD techniques.

3.1 Radiation Hardening by Process (RHBP)

Initially, space-qualified components were majority obtained through the optimization of the manufacturing processes targeting the radiation resilience of the process technology itself, i.e. technologies issued from the so called *rad-hard foundries* [67]. These process modifications are usually kept in secret, so it is impossible to have information from the industry. However, these modifications usually relates to the application of different materials, variation of doping profiles and substrate technology. For instance, it was shown that the removal of borophosphosilicate glass (BPSG) layers, used for the planarization between metallic layers, can induce a reduction of about 8 to 10 times the SEU rate induced by neutron interactions with boron [73, 74]. However, since the adoption of the chemical mechanical polishing (CMP) in the advanced technologies, BPSG layers are no longer used in the standard manufacturing process and the main contributor to the thermal neutron SEU rate is the boron isotope ^{10}B present in the source/drain junctions of PMOS devices, p-well or tungsten plugs [75]. The natural boron (${}_5\text{B}$) is abundant in two isotopes: the boron-10 (^{10}B) in 20% and the boron-11 (^{11}B) in 80%. However, the capture cross section of the ^{10}B is three orders of magnitude higher than the ^{11}B and it is the only one able to release alpha particles that induces SEE [76, 77]. Thus, in order to reduce the impact of thermal neutrons, a boron purification process should be introduced into the

manufacturing process so the abundance of ^{10}B is reduced.

Each additional manufacturing step introduced to the conventional design process adds complexity and increases the fabrication cost. Hence, due to the high complexity of the manufacturing steps used to achieve radiation hardness, the higher costs and their usually low-volume production, these rad-hard technologies cannot follow the transistor scaling trend. In this way, the available radiation-hardened technology is normally some generations behind the state-of-the-art transistor technology [70]. One example is the Sandia's CMOS7 technology process that provides a rad-hard technology based on a 350nm Silicon-On-Insulator (SOI) design process [78], however, the first commercial 350nm technology process were adopted in mainstream applications in the early 90's. Thus, besides the higher price, building chips using rad-hard technologies also provides lower performance when compared with the highly-integrated commercial technologies. Consequently, space systems using rad-hard technology process may face challenges meeting the performance, power and area constraints expected in today's space market. This impact can be clearly observed in Figure 3.2 where the throughput (expressed in Million Instructions Per Second, MIPS) are shown for commercial and rad-hard CPUs (Central Processing Units) according to their year of introduction into the market. The throughput of a CPU is an efficiency coefficient in which the number of instructions that a CPU can execute per unit time is estimated for a given clock rate. The rad-hard CPUs providing the same throughput of the commercial CPUs are introduced into the market, in average, 8 to 10 years after the introduction of the commercial ones [67].

One alternative to rad-hard technologies is the adoption of a commercial technology process in which the transistor is built on insulating substrates, i.e. a Silicon-On-Insulator (SOI) technology [79–81]. Figure 3.3 presents a simplified 2D illustration of a NMOS device fabricated in a bulk technology and in two variants of the SOI technology. In the SOI technology, the introduction of an insulation oxide, called as buried silicon oxide (BOX) layer, separates the substrate of the device from its channel and source/drain junctions. In this manner, a reduction of the sensitive volume is obtained, leading to reduction of the charge collection process in the sensitive nodes and,

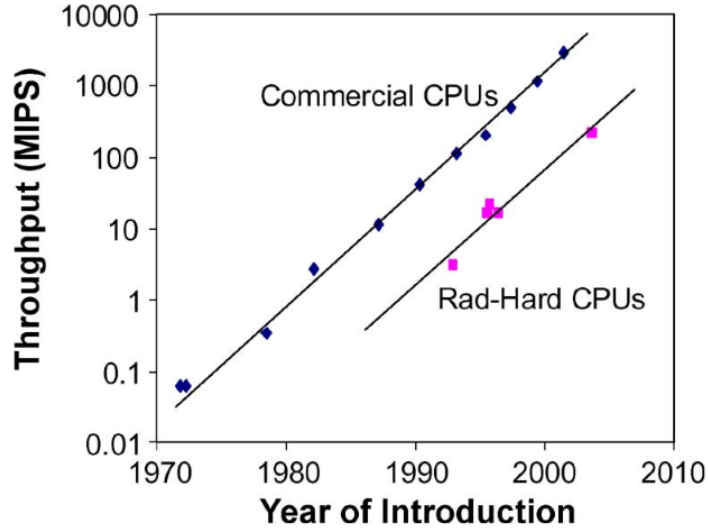


Figure 3.2: Comparing of commercial and rad-hard processors in terms of throughput (in Million Instructions Per Second, MIPS) [67].

consequently, improved radiation robustness. Additionally, the BOX layer prevents the charge sharing effect between adjacent devices due to the suppression of the carrier diffusion mechanism. And, very importantly, the SOI device structure eliminates the parasitic silicon-controlled rectifier (SCR) inherently present between transistors in bulk CMOS circuits and responsible for triggering the latch-up mechanism. Thus, SOI-based designs are intrinsically immune to single-event latch-up (SEL) effects [79]. However, despite the smaller sensitive volume and immunity to SEL, a stronger parasitic bipolar amplification (PBA) effect is observed and it might degrade the SEE hardness of the SOI-based circuits. When a particle hits the SOI device the additional carriers can recombine or drift to the pn junctions. If the majority carriers in the body are able to drift to the source junction and lower the source-to-body potential, a injection of minority carriers from the source can take place and additional carriers are collected by the drain junction, increasing the magnitude of the SEE.

Concerning the two SOI variants from Figure 3.3, the Partially-Depleted SOI (PDSOI) technology presents the closest electrical and structure characteristics to the traditional bulk technology due to the thickness of the silicon

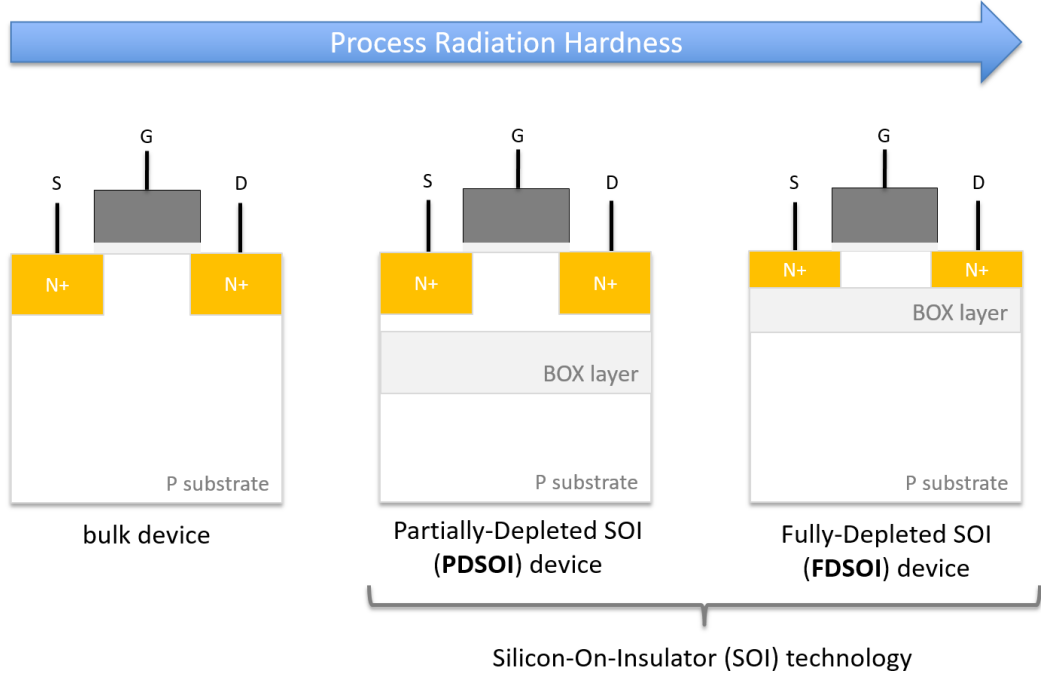


Figure 3.3: Simplified representation of a NMOS device manufactured in a bulk technology and two variants of a Silicon-On-Insulator (SOI) technology.

film layer on top of the BOX layer. The silicon film layer can be approximately of 50nm to 200nm, providing a large and partially-depleted body device and high PBA effect. On the other hand, for the Fully-Depleted SOI (FDSOI) technology, the thickness can reach from 5nm to 20nm, resulting into a fully-depleted body [82]. Due to a thinner silicon film, the FDSOI devices present a higher switching speed and better SEE hardness in response to the stronger charge inversion and low PBA effect. Although the increase in area, body ties have successfully shown to reduce the bipolar amplification, especially for PDSOI devices [81, 83, 84].

As much as RHBP techniques are quite effective in hardening electronics components against radiation effects, the industry has increasingly investing on the usage of hardening by design techniques. Specially with the introduction of the New Space market in which the space applications require short entry to the market, lower cost and more on-board processing power. In the next section, hardening techniques at layout and circuit level are discussed.

3.2 Radiation Hardening by Design (RHBD)

3.2.1 Layout-based techniques

RHBD techniques can profit from the improvements on power, performance and reduced area acquired by state-of-the-art commercially available CMOS technology process [67]. One well established RHBD layout technique used to reduce the leakage current induced by total ionizing dose effects is the adoption of edgeless transistors, also known as Enclosed Layout Transistors (ELT) [85, 86]. Figure 3.4 presents a layout comparison between the standard and the edgeless transistors. When a MOS device is under radiation ionizing dose, positive charges, i.e. holes, can get trapped within the Shallow Trench Isolation (STI) oxide next to the source and drain junctions. Depending on the density of trapped holes, a parasitic conduction path can be created in the edge of the NMOS transistors [87]. In this case, inversion in the p-substrate may occur in this parasitic channel formed in the edge between the oxide and the junctions of the transistor, leading to leakage current flow between the drain and source junctions. The enclosed transistor layout removes the connection between the junctions and the sidewall oxides, eliminating the parasitic channel and reducing the radiation-induced leakage current [86]. The parasitic leakage paths for the standard transistor layout are indicated in Figure 3.4.

The biggest drawbacks of this technique are the area overhead and the limitation on the transistor sizing [88, 86]. For instance, the minimum aspect ratio W/L that can be obtained for a edgeless transistor is of approximately 2.26. In digital design, the density and performance is the priority, thus L is kept the minimum size while W can vary depending on the constraints. However, in analog design, the W/L can be less than 1 as the L is increased to reduce leakage currents in low-power designs. Thus, ELT transistors are quite limited when targeting high performance or low-power designs. Also, due to the layout complexity and the gate geometry, SPICE models should be adapted to address the non-linearity of the channel length modulation [89]. Recently, two other layout modifications have been proposed in comparison

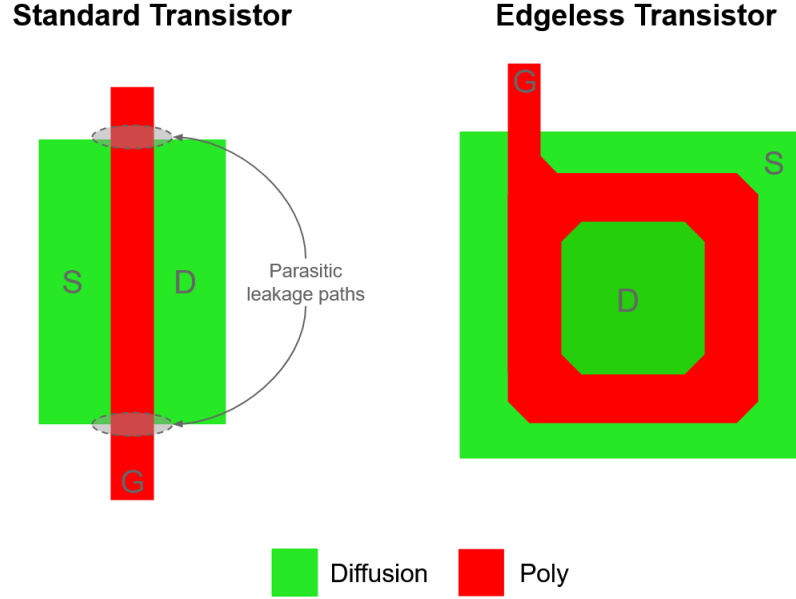


Figure 3.4: Comparison between a standard transistor layout and the edgeless transistor layout (ELT).

to the edgeless transistor: the Z-gate [90] and the I-gate transistor layout [91, 92]. Despite the promising results, more studies should be conducted to verify the applicability of these techniques and its consequent drawbacks.

The adoption of edgeless transistors is only capable of preventing leakage current paths within the transistor itself, however, when two NMOS devices are placed side-by-side a parasitic leakage path can be formed transistor-to-transistor through the STI oxide. To prevent that, p+ guard rings are used surrounding the NMOS devices, such that the p+ diffusion obstructs any possible parasitic channel between the +n diffusions. Thus, in order to eliminate the both intra-device and inter-device radiation-induced leakage paths, guard-rings have been vastly used along side the edgeless transistors [93, 94]. Figure 3.5 illustrates the structure of guard rings around the PMOS device (n+ guard ring connected to power supply voltage) and the NMOS device (p+ guard ring connected to ground supply voltage). As the guard rings provide electrical and spatial isolation, this technique has also shown to provide SEL immunity besides lowering the TID effects [86, 93]. A study was conducted to assess the hardening effectiveness of guard rings schemes

against SEL effects in a 180nm technology [94]. It was shown that both single and dual guard rings configurations (when both PMOS and NMOS devices have guard rings) are able to provide SEL immunity up to $100 \text{ MeV.cm}^2/\text{mg}$. Thus, to lower the area overhead, the single guard ring configuration should be used and prioritizing the p+ guard ring that is also able to reduce the radiation-induced leakage of the NMOS devices [94].

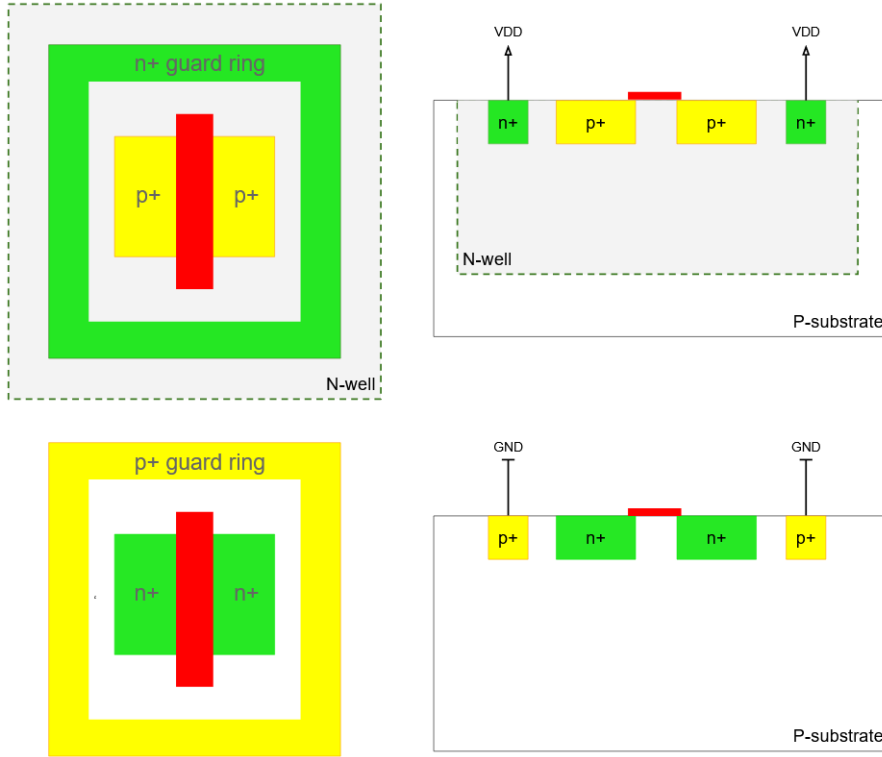


Figure 3.5: Layout and cross-sectional representation of guard rings around PMOS and NMOS transistors.

The transistor positioning within the digital CMOS layout design has also been explored to provide radiation hardness to SEE [95, 96]. In [95], the placement of NMOS transistors is evaluated in respect to the proximity to the N-well region. TCAD simulations of an inverter gate with different NMOS positioning ranging from a distance D of 200nm to 1000nm from the N-well border (shown in Figure 3.6). The results show that as closer the device is placed to the N-well region, shorter is the SET pulse width for

particle strikes at the NMOS device. This observation was attributed to: (1) the reversed-biased diode formed by the N-well and substrate interface which collects the additional carriers; and, to (2) the reinforcement of the recovery current from the PMOS devices while the *off*-state NMOS transistor is hit by the particle. Figure 3.6 illustrates this phenomenon in which the parasitic bipolar effect in the PMOS device is enhanced by the close proximity of the NMOS device. The design with the NMOS device with a distance $D = 200\text{nm}$ has nearly ten times the collected charge by the N-well in the design with $D = 1000\text{nm}$.

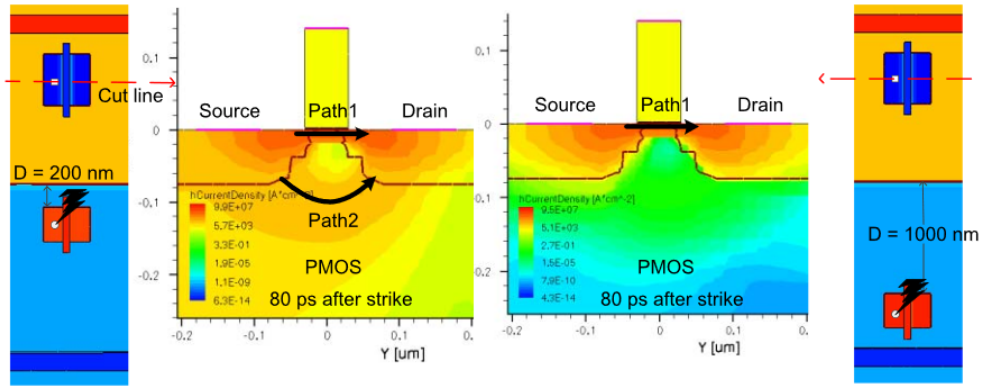


Figure 3.6: Recovery current reinforcement induced by the increased parasitic bipolar effect due to the close proximity NMOS device [95].

This collected charge is responsible for lowering the electrostatic potential in the N-well and activating the parasitic bipolar transistor. With the parasitic bipolar transistor turned *on*, additional carriers will flow from the source to the drain of the PMOS device (Path2 in the Figure 3.6), enhancing the recovery current. Although the reduction on the SET pulse width, this technique can possibly worsen the SEL resilience of the design, as shown in the TCAD simulations performed in [97]. Due to the activation of the parasitic bipolar transistor, the decrease of the Anode-to-Cathode (A-C) spacing, i.e. the distance between the PMOS and NMOS devices, has shown a decrease in the threshold LET and an increase in the saturation SEL cross-section. Therefore, the designer should have clear in mind the implications of each hardening technique and the target effects intended to mitigate. For

instance, the substrate and well taps placement has shown a stronger impact on the SEL sensitivity than the A-C spacing [97]. Thus, to counteract the negative effect of the close proximity NMOS devices, substrate and well taps placement can be used as described in [97].

Another layout technique that use the transistor placement to improve the SEE robustness is the LEAP (Layout design through Error-Aware transistor Positioning) [96]. In this layout approach, the transistors are placed horizontally in such a way that all the collecting nodes are aligned. The whole idea is to take the advantage of the charge collection by the *on* transistors to pull the output voltage back to the expected value. One example of a LEAP-based layout for an inverter gate is shown in Figure 3.7.

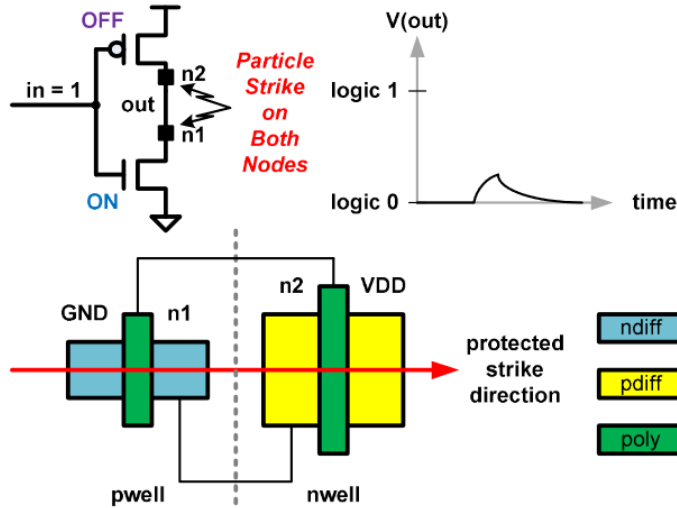


Figure 3.7: Illustration of the LEAP principle for an inverter gate. When a particle strikes both NMOS and PMOS drain nodes simultaneously, the charge collected by the *on*-state NMOS transistor reduces the overall transient pulse at the output of the gate [96].

Whenever the particle strikes horizontally, both drain regions will be collecting the additional charges [96, 68]. Due to the horizontal transistor alignment, the charge collected by the *on*-state NMOS transistor will counteract against the charge collected by the *off*-state PMOS transistor [96]. Overall, the resulting transient pulse is shortened as the *on*-state NMOS is pulling the output voltage back to the logic 0, similar principle of the recovery

current reinforcement from [95].

The transistor sizing (also known as gate sizing) is another well-known hardening technique based on the radiation-induced transient dependency on the drive strength and nodal capacitance of the circuit [98]. However, by increasing the transistor width and drain area is also increased and it can induce a greater charge collection process and increased SEE sensitivity. In the next chapter, the application of gate sizing, transistor stacking and transistor folding are investigated.

3.2.2 Circuit-based techniques

Besides the layout techniques, complete mitigation or some level of hardness against radiation effects can be achieved through circuit-based techniques. One of the most used approach is the application of the concept of redundancy, whether in hardware, software or information. The best example of redundant schemes is shown in Figure 3.8, the Triple Modular Redundancy (TMR), which is a well-known and widely used fault tolerant technique that provides robustness to SET and SEU [99]. In this approach, the critical component is triplicated in the design and all the three output signals are connected to a majority voter (MJV) circuit where the majority of the input signal determines the output signal. In other words, whenever two of the triplicates are fault-free, the correct output will be propagated. The main drawback of this technique is clearly the massive increase in area (2 duplicates + MJV circuit) and the consequent increase in power consumption. Also, despite the good fault coverage, the technique relies on the robustness of the MJV circuit, because, even if the 3 components are fault-free, whenever a particle hits the voter and deposits sufficient charge, the SET or SEU will be propagated.

This technique is largely applied in the circuit level, however, this concept has been also adopted in upper levels such as in FPGAs, System-on-Chip and software-based redundancy [100–102]. Different from the TMR implementation in hardware, when applied in the software level the biggest concern is the overhead in execution time. Several variants of the TMR schemes have

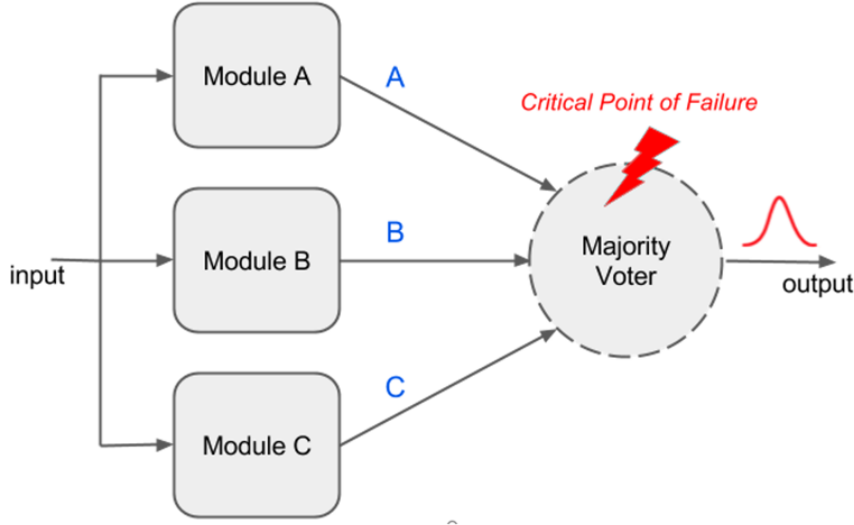
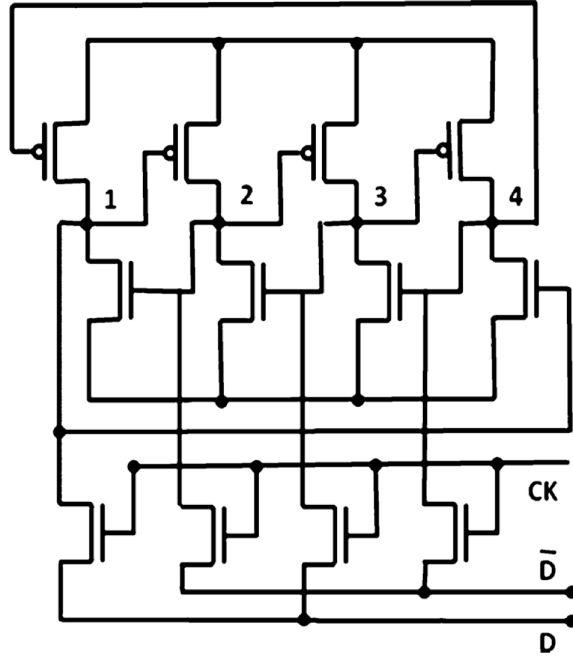


Figure 3.8: Diagram of the Triple Modular Redundancy (TMR) fault tolerance technique [45].

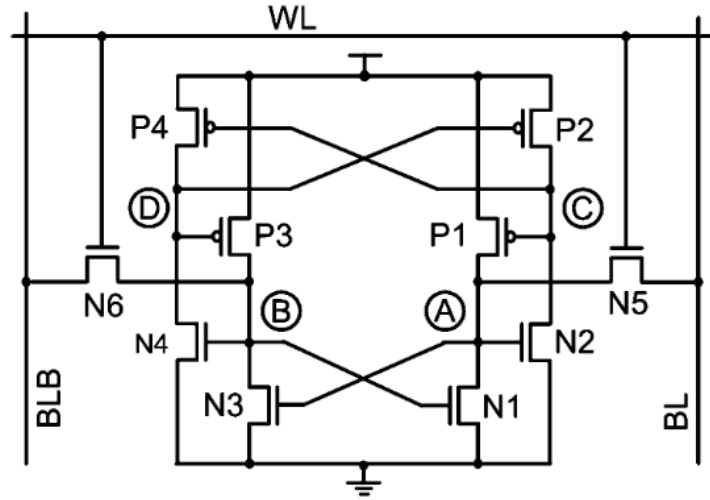
been proposed such as the Diversity TMR (DTMR) [101] in which different design implementations are used for the triplicated modules, and, the Approximate TMR (ATMR) where approximate functions are used instead of exact replicas of the main function [102]. Both variants have shown a good compromise between area/performance overhead and fault tolerance against SEE when compared to the traditional TMR scheme.

Another widely used approach in the circuit level is to harden memory cells by using redundant reinforced feedback architectures such as the Dual Interlocked Storage Cell (DICE) and Quatro circuits [103, 104]. The two circuit topologies are shown in Figure 3.9 for the design of an 1-bit SRAM cell. Instead of using a single cross-coupled inverter pair as in the standard 6T SRAM design, both circuits have a feedback mechanism sustained by interlocked structures that guarantee the correct output whenever a single sensitive node collects charge. These structures ensure that the stored bit in the memory cell is defined by more than a single pull-down/pull-up network. Although a good radiation response can be achieved, these designs have degraded read/write performance and high area overhead.

The radiation hardness of the DICE cell has been extensively validated



(a) DICE cell



(b) Q10T cell

Figure 3.9: Two circuit architectures based on reinforcement feedback: (a) Dual Interlocked Storage Cell (DICE) [68], and (b) Quatro-10T (Q10T) cell [104]

through simulations and experiments, being the main reference design for hardening technique in memory circuit designs in the literature [105–107]. The Quatro design was proposed in [104] as an alternative to the traditional DICE cell with a lower area overhead and better data stability. Some works have shown that flip-flops and SRAM designs based on the Quatro topology have a higher SEU robustness than the DICE cells [108–111]. However, with the close proximity of transistors in deeply-scaled transistor technologies, the impact of charge sharing effects have shown to be a concern for the reliability of these architectures. To address this issue, circuit-based RHBD techniques can be combined along with the layout-based techniques shown in the last section. For instance, the LEAP technique was applied in the DICE design for flip-flops in [96, 68].

The LEAP-DICE Flip-flops at 28nm bulk technology have shown a reduction of the SEU rate of approximately two orders of magnitude when compared to the traditional DICE layout design [68]. Different from the LEAP technique that aims to place specific transistors closer together so the charge sharing effect affects positively the overall SEE sensitivity, some design approaches aim to increase the nodal spacing to cope with multiple node collection of critical nodes [112, 113, 107]. With the transistor scaling, the layout design carries a stronger influence on the circuit reliability when considering radiation effects. Accordingly, more and more techniques have been adopted in the layout level to mitigate the effect of multiple node collection and parasitic bipolar amplification [114–117, 90, 92, 118].

3.3 Conclusions

With the increase of electronics systems used in radiation environments such as in space, aviation, medical applications and particle accelerators, the need to explore different hardening techniques is increasing in importance to guarantee the correctness of the applied systems. In this chapter, a review of some basic concepts and the state-of-the-art on radiation hardening techniques are briefly discussed. To increase the reliability of the system, designers can improve the radiation hardness through process modifications in

the circuit fabrication, the so-called Radiation-Hardened-by-Process (RHBP) techniques. However, with the increase search for high-performance and low-power solutions, Radiation-Hardened-By-Design (RHBD) techniques have shown to be adequate and promising when added to the benefits provided by the commercial deeply-scaled technologies. In order to cope with the charge collection mechanisms induced by a particle strike, layout-based RHBD techniques are quite effective as it directly impacts the charge collection efficiency in the sensitive nodes of the circuit. Circuit-level techniques normally uses the concept of redundancy to reinforce the logic bit in memory cells for example, or to mask the SEE occurrence through voting schemes. When a critical system is designed for a radiation environment, different parameters should be taken into consideration for the hardening technique selection. The techniques can be used together to achieve the level of hardness desired. However, area, power and performance overhead are expected, thus careful analysis should be carried out to guarantee the reliability level is achieved while respecting the design constraints. In this context, a detailed analysis of layout-based RHBD techniques is provided in the next chapter.

4

Analysis of RHBD at Layout-level

Radiation hardening techniques can be extensively used in the design level to improve the robustness of VLSI circuits used in space applications. As discussed in the previous chapter, a variety of Radiation Hardening by Design (RHBD) techniques have been developed to cope with radiation effects on electronic circuits at different levels of abstraction ranging from circuit layout to system and software design [70, 119, 120, 115, 121, 122]. In this chapter, some analysis is provided on the hardening efficiency obtained through layout design techniques, such as Gate Sizing (GS), Transistor Stacking (TS) and Transistor Folding (TF). Additionally, asymmetric designs and the Diffusion Splitting (DS) technique are explored to improve the hardening efficiency and reduce the area overhead.

4.1 Gate Sizing and Transistor Stacking

Radiation robustness can be obtained through reliability-aware logic and physical synthesis in semi-custom designs based on standard-cell methodology [123–126]. In other words, it is possible to harden a circuit by selectively using logic gates that minimize the SET generation or propagation in the most vulnerable nodes of a complex VLSI design. In [123], three selective

node hardening techniques were evaluated in the logic synthesis of different ISCAS85 benchmark circuits. It was shown that hardening techniques can be very effective when applied at standard cell based VLSI designs. During physical synthesis, hardening strategies can be explored in the cell placement to avoid charge sharing effects or to promote pulse quenching effects in electrically related combinational circuits [124–126]. Du et al. [125] demonstrated that, as feature size shrinks, cell placement has a stronger impact on the soft error vulnerability of complex VLSI due to the multi-node collection process. Accordingly, it is imperative to study selective node hardening strategies suitable to be integrated into standard cell based design methodologies. In this section, a comparative analysis is provided for the usage of gate sizing and transistor stacking when adopted in a standard-cell methodology.

4.1.1 Gate Sizing (GS)

The feature sizes of transistors, i.e. the length (L) and the width (W) of the device channel, directly influence the performance of the circuits. Transistor and gate sizing are widely used to improve delay/power trade-offs in different applications [127, 128]. A simplified representation of a transistor layout is shown in Figure 4.1. The green layer represents the diffusion area, i.e. the regions in which the p-n junctions are formed such as the source (S) and drain (D) of the transistor. The red rectangular is the polysilicon layer and it represents the gate (G) of the device. The metal 1 is shown in blue and the yellow via, the VIA0, connects the metal 1 to the diffusion layer.

The width W and length L of the transistor channel characterize the electrical behavior of the device. For instance, the drain current I_D of a transistor follows the relation shown in Equation 4.1. By changing the W/L ratio of transistors, the nodal capacitance and drive strength of the circuit are affected, leading to changes in the power consumption and propagation delay. As the length L is a process parameter determined by the transistor technology, the circuit designer can only operate on the width W of the transistor to reach the design requirements. The larger the width W , the lower the resistance. Consequently, greater is the drain current I_D , reducing

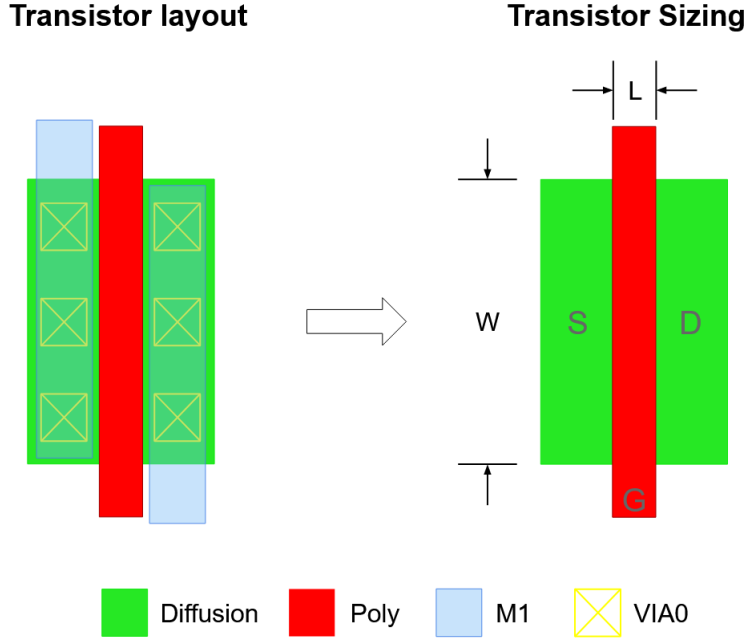


Figure 4.1: MOS transistor layout and its main feature sizing: width W and length L of the transistor channel.

the propagation delay of the circuit. However, increasing the width W also increases the capacitance, leading to an increase in power consumption.

$$I_D \propto \frac{W}{L} \quad (4.1)$$

As radiation-induced transient currents are also dependent on the drive strength and nodal capacitance of the circuit, gate sizing has also been used to improve the radiation robustness of VLSI circuits [98]. Let's analyze the radiation response of an inverter gate under different sizing scenarios. The inverter design in the Complementary MOS logic style is composed of a single PMOS transistor in the pull-up network and a single NMOS transistor in the pull-down network. The transistor schematics, truth table and the gate symbol of a CMOS inverter are presented in Figure 4.2. The channel width for the PMOS device is denoted as W_p and for the NMOS as W_n . For a input signal at low-logic value ("0", ground), the output of a inverter will be in high-logic level ("1", power supply) and vice-versa.

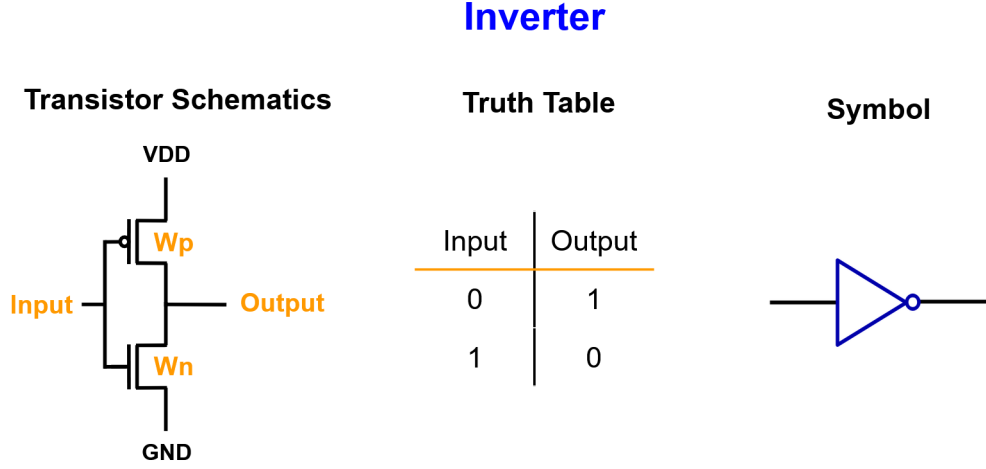


Figure 4.2: Transistor schematics of a CMOS inverter, the truth table and its symbol.

Table 4.1: Gate sizing scenarios for the SET injection at an inverter

	Wp (nm)	Wn (nm)
Scenario 1	630	415
Scenario 2	945	415
Scenario 3	630	622
Scenario 4	945	622

The four gate sizing scenarios used in this analysis are shown in Table 4.1. The scenario 1 corresponds to the minimum sizing available for an inverter gate in a standard cell library at 45nm technology, the 45nm OpenCell NanGate library [129]. In the scenario 2 to 4, the W_p and/or W_n are multiplied by 1.5. Using a SPICE circuit simulator, electrical simulations are performed with the injection of a double exponential current source with the same arbitrary SET parameters in all sizing scenario. The goal is to analyze the complex relationship between gate sizing, nodal capacitance, restoring current and the final SET pulse. The SET response for the injection campaign is shown in Figure 4.3 considering the input of the gate in low-logic level. In this polarization, the NMOS device is in *off*-state while the PMOS device is responsible for the maintenance of the output signal which is in high-logic level. As the minimum sizing is the scenario 1, its SET response is

considered as the reference for this analysis. In the scenario 2, only the W_p is increased by $1.5\times$ and the resulting SET pulse is drastically shortened. The pulse peak is not reaching half the supply voltage value, so it will possibly be electrically masked in the next gate stage. On the other hand, when only the W_n is upsized in the scenario 3, the SET pulse remains almost the same from the minimum sizing inverter at scenario 1. As the PMOS device is the one responsible for providing the restoring current, increasing the W_n does not increase the SET recovery in this case. In fact, in this analysis the same collected charge is considered for all the sizing scenarios, however, with the upsizing of the transistor, a larger collecting area is obtained leading to higher collection efficiency. Thus, if the charge collection mechanism would be considered in this analysis, the resulting SET in the scenario 3 would be expected to be larger due to the increased collection efficiency provided by the increased NMOS transistor width, W_n . In the scenario 4, both transistors are upsized and we observe a similar response of the scenario 2. This result reaffirms that, for input signal at low-logic level, the PMOS device should be upsized to reduce the radiation-induced transient pulse.

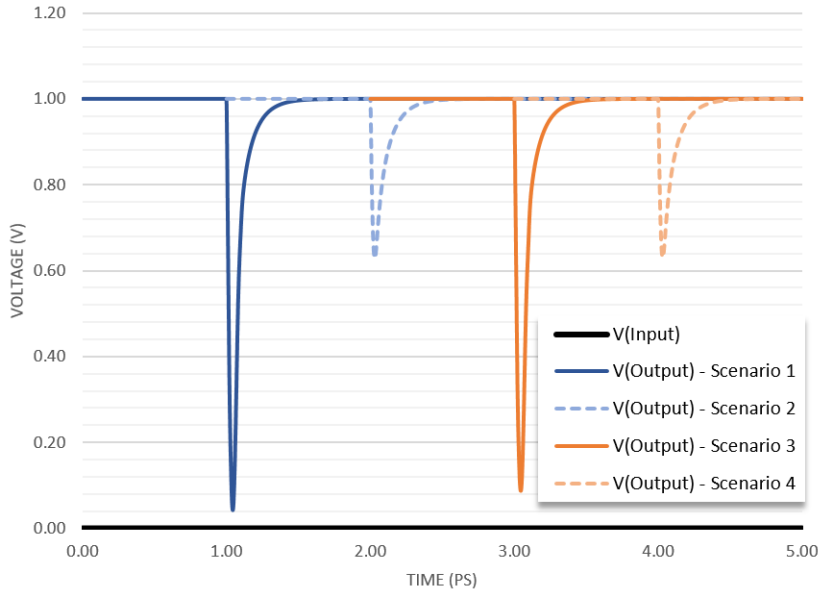


Figure 4.3: SET injection at the output of a CMOS Inverter with different sizing scenarios when the NMOS device is sensitive.

In Figure 4.4, the same analysis is done considering the PMOS device in *off*-state, i.e. input signal is in high-logic level. In this case, the SET pulse is considerably shortened only when the Wn is upsized, i.e. scenario 3 and scenario 4. Thus, in order to harden the inverter for both input cases, the scenario 4 turns out to be the best sizing in this analysis. However, besides increasing the capacitance and restoring current, upsizing transistors increases the sensitive area and it can possibly worsen the reliability of the circuit by increasing the particle incidence probability and the charge collection efficiency. In standard cell libraries, the cells are available with different drive strengths, starting from the minimum sized implementation denoted by X1, and increasing discretely to drive strength 2 (X2), drive strength 4 (X4) and so on. Due to the high regularity of circuit layout of standard cells and drive strength options, the gate sizing using standard-cell methodology is a discrete process. In [130], inverter, NAND and NOR logic gates from a 90nm RHBD cell library were characterized under heavy ion and high energy protons irradiation. Different drive strengths available in the cell library were evaluated. Results show that upsizing the cells was only efficient on reducing the SET cross-section for the inverter and NOR logic gates. In the case of the NAND2_X2 cell, the larger sensitive area dominates the SET sensitivity over the increased nodal capacitance and restoring current [130]. On the other hand, FinFET-based circuits using NAND and NOR gates have shown similar SET sensitivity in [45]. The symmetric sizing of the PMOS and NMOS transistors, provided by the strain engineering and width quantization, has led to a symmetrical collection drain area and restoring current and hence a similar soft error susceptibility for both gates. In this work, the gate sizing is evaluated using the prediction methodology described in Section 2.4. Using a multi-physics prediction methodology enables the understanding of the complex relationship between charge collection efficiency and electrical characteristics involved in layout-based radiation hardening techniques and its impact on the SEE cross-section.

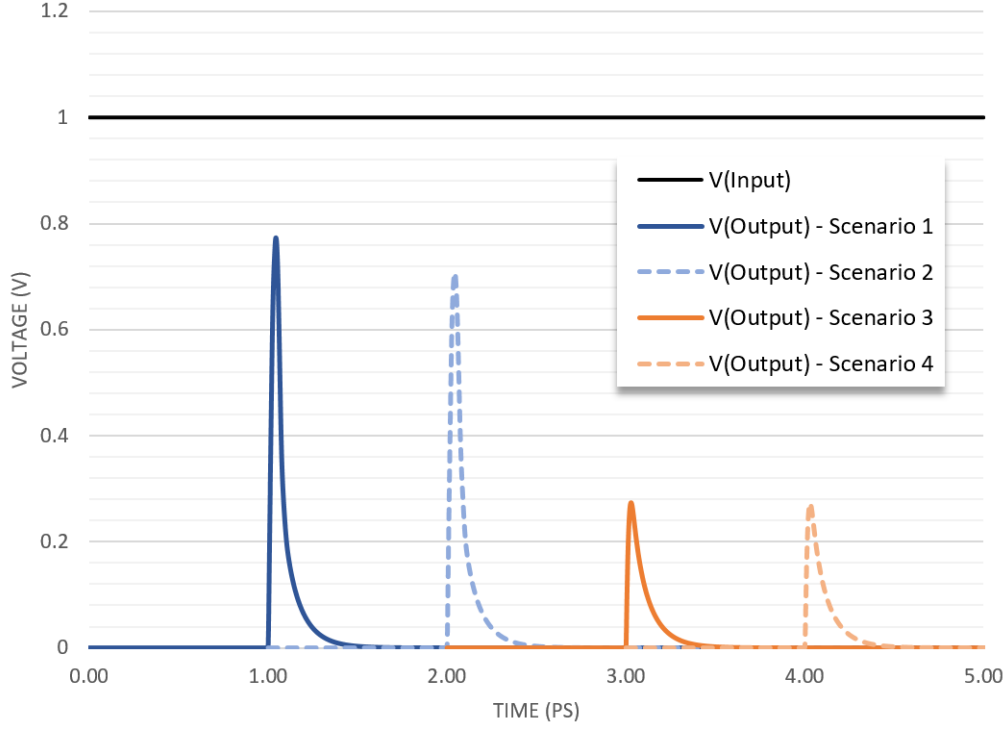


Figure 4.4: SET injection at the output of a CMOS Inverter with different sizing scenarios when the PMOS device is sensitive.

4.1.2 Transistor Stacking (TS)

Another alternative to gate sizing is to use transistor stacking (TS) to increase the nodal capacitance [123]. Stacking devices is a well-known RHBD technique used for SEU immunity in SOI designs [131, 132]. To illustrate the concept behind this hardening technique, Figure 4.5 contains the transistor schematics of an inverter and the simplified representation of the NMOS transistors at device level in a SOI technology. Instead of using two transistor as shown in Figure 4.2, the TS-based CMOS inverter adopts 4 transistors where the additional transistors are added in series to the original ones.

Due to the SOI structure, the shallow trench isolation (STI) and buried oxide (BOX) prevent charge sharing between the stacked transistors improving the overall soft error susceptibility drastically [131]. If a incident particle hits only the transistor N2 in the TS inverter, the induced SET will not be

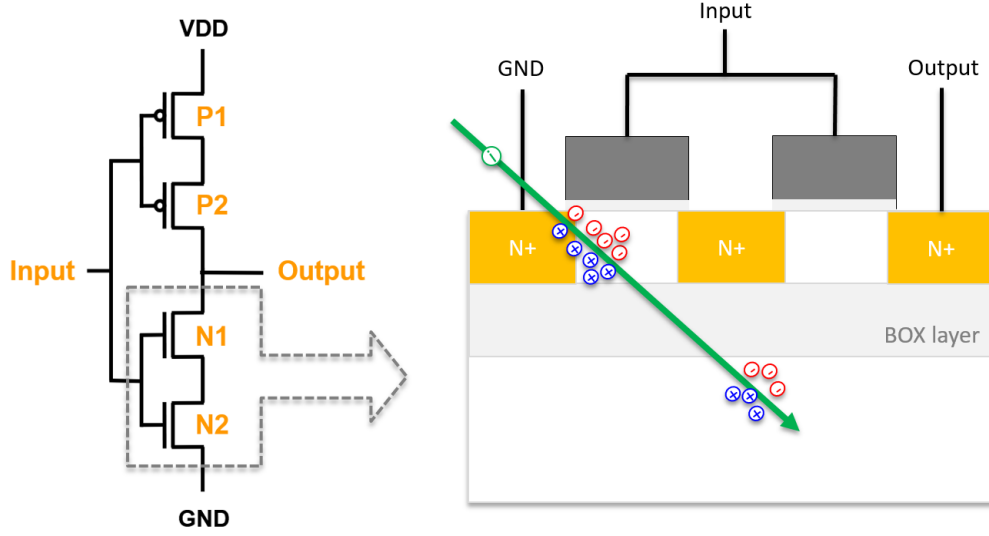


Figure 4.5: Application of transistor stacking in an inverter design based on a SOI technology and the representation of a heavy-ion ionization. The electron-hole pairs generated within the insulator are omitted due to its negligible contribution to the SEE effects.

able to propagate to the output because the transistor N1 is in *off*-state and operates as an open circuit. Accordingly, a single particle strike must deposit sufficient charge in both stacked devices, or at least in the closest one to the output, for an SEU/SET to be observed in the circuit. Recently, it was shown that by only adopting NMOS stacked devices in SOI latch designs the SEU rate can be improved in more than 80% [133]. Unlike SOI technology, bulk devices experience charge sharing effect among adjacent transistors. However, it still benefits from the increased nodal capacitance and the masking effect provided by the stacked devices. Additionally, transistor stacking enables power consumption reduction due to a lower leakage current than the observed for a same sized single transistor [134]. In [123], transistor stacking outperformed gate sizing in terms of power consumption while maintaining similar area efficiency. Although the power saving compared to gate sizing, connecting transistors in series in the stacking technique increases the effective (dis)charging resistance leading to increase in delay and consequently degradation of the circuit performance.

One of the advantages of the gate sizing and transistor stacking is that both techniques can be applied in full-custom designs or using standard-cell libraries. As discussed in the previous section, a cell library contains several logic functions implemented in different drive strengths, but also with different number of input signals. Accordingly, a 4-input NAND gate (NAND4) can be used as a 2-input NAND gate (NAND2) with stacked devices if the additional input signals are connected to the original inputs as shown in Figure 4.6. However, the TS technique is only applied in the pull-down network while in the pull-up network the additional transistor are connected in parallel, increasing the overall driving strength. Similarly, by using a 4-input NOR gate, a 2-input NOR gate with PMOS stacked devices can be obtained.

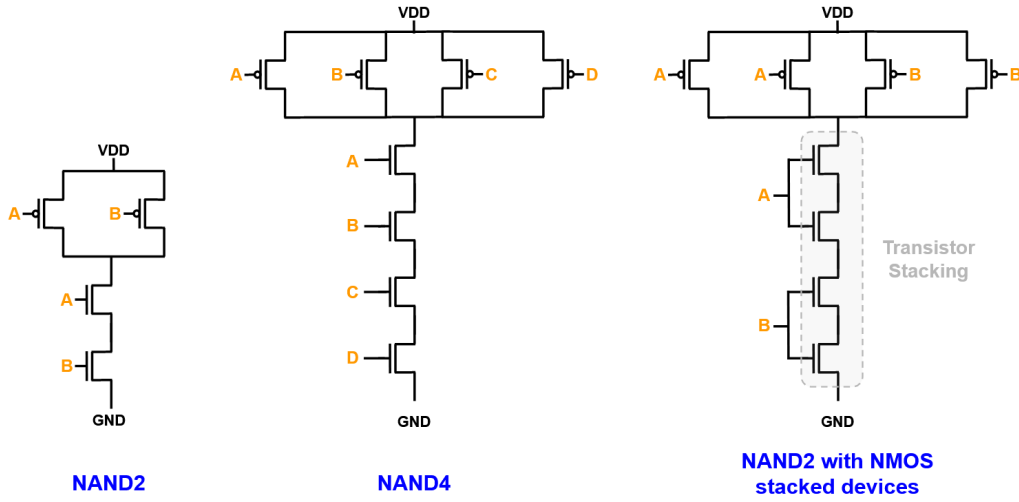


Figure 4.6: Using 4-input NAND gate to achieve stacking transistors for a 2-input NAND function with standard-cell libraries.

Taking into account the layout effects on the deposition and charge collection process, this work aims to investigate the radiation hardening efficiency of gate sizing and transistor stacking when used in cell-based methodology. Aiming at low power reliable applications, the analysis focuses on the trade-off between power consumption and radiation effects. And, more importantly, the input dependence of each technique is provided and it can be used to improve the radiation reliability of hardened standard cell libraries

while reducing its area, power and performance overhead.

4.1.3 Comparison of power and area overhead

The radiation robustness of a circuit design is influenced by a variety of physical and electrical factors. Increasing the nodal capacitance and restoring current improves the overall robustness, however layout and drain area should also be taken into consideration to evaluate the effectiveness of RHBD techniques in reducing the charge collection. Figure 4.7 presents the layout design of the NAND2_X1, NAND2_X2, NAND4_X1, NOR2_X1, NOR2_X2, and NOR4_X1. Table 4.2 presents the layout and drain area information for the NAND and NOR gates considering the minimum sized (named as the unhardened design), gate sizing and transistor stacking. It is important to notice that both NAND and NOR gates provide the same layout design area. This is also observed when considering gate sizing and transistor stacking approaches due to the cell design regularity characteristic of a standard cell library implementation. Thus, in terms of area overhead, these hardening techniques provide the same increase of 66.7% for the analysed layout design of NAND and NOR gates. However, despite the same layout design area, a different sensitive collecting area is obtained for each technique. Considering the total area of the drain junctions in the layout, i.e. the sensitive collecting area, the two techniques present an area increase. For both circuits, transistor stacking showed the greatest increase in drain area, 107.5% and 110.9% for NAND and NOR, respectively. Originally, the NOR gate presents approximately 11.6% greater drain area than the NAND gate. When applying the hardening techniques this difference reduces to 8.5% for gate sizing, and increases to 13.5% for transistor stacking.

Besides the increase in area, adopting RHBD techniques generally implies in increase in power consumption. Due to the increase in leakage current in advanced technology nodes, the static power consumption is the power metric considered in this work. Figure 4.8 presents the static power consumption for the NAND and NOR gate considering both RHBD techniques. For both standard cells, gate sizing showed the largest increase in power con-

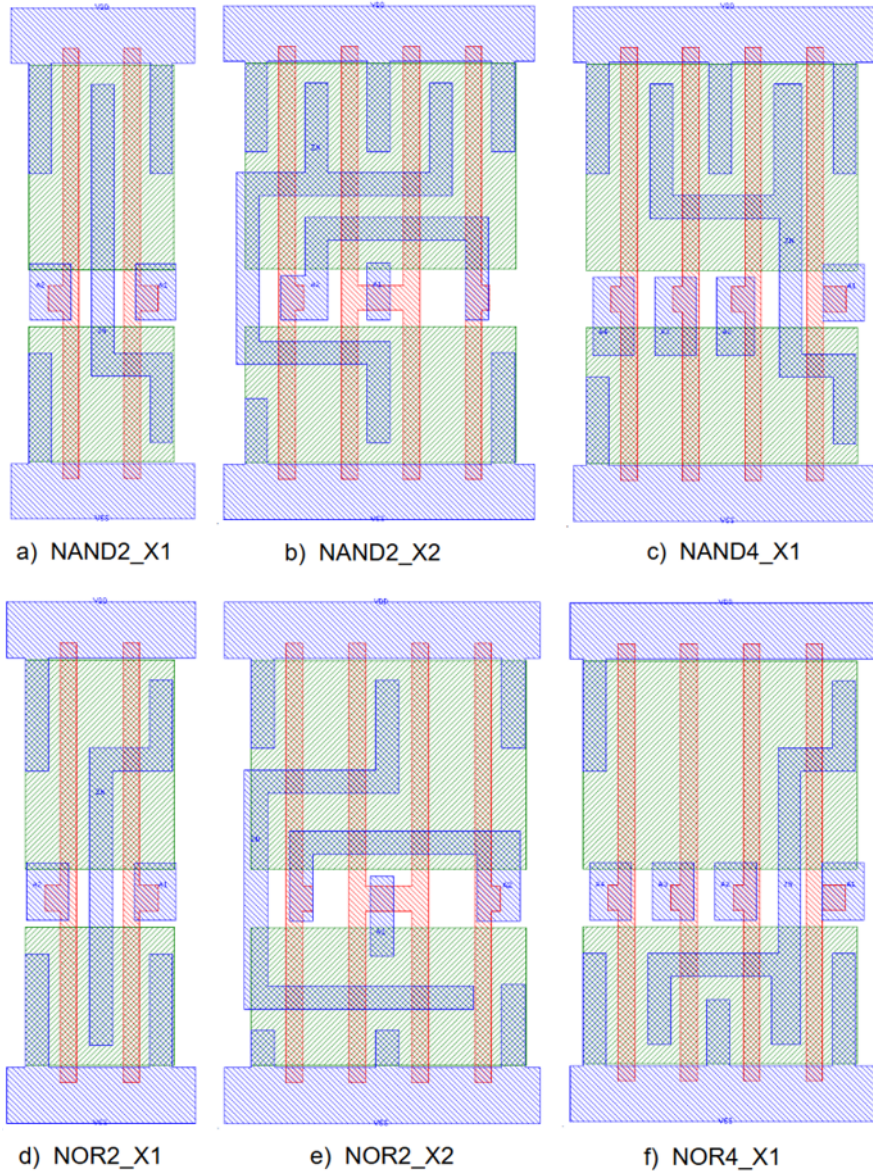


Figure 4.7: Simplified cell layout design of logic gates from the 45-nm bulk CMOS [129] containing metal1 (blue), active diffusion (green) and poly layers (red).

Table 4.2: Layout and drain area of the unhardened design, and applying gate sizing and transistor stacking techniques (Area increase is expressed in percentage)

		Unhardened (μm^2)	Gate Sizing (μm^2)	Transistor Stacking (μm^2)
Layout	NAND	0.895	1.492 (66.7%)	1.492 (66.7%)
	NOR	0.895	1.492 (66.7%)	1.492 (66.7%)
Drain	NAND	0.190	0.351 (84.6%)	0.394 (107.5%)
	NOR	0.212	0.381 (79.6%)	0.447 (110.9%)

sumption, a factor of 2. Due to the leakage current reduction provided by the transistor stacking effect, both circuits have shown lower power consumption when compared to the gate sizing technique. The NMOS transistors in the pull-down network provide higher leakage current than the PMOS transistors [134]. When adopting transistor stacking using standard cells, the stacked devices for the NAND and NOR gate are the NMOS and PMOS transistors, respectively. This explains the greater reduction observed on the static power reduction for the NAND gate, as it contains stacked NMOS devices. This also explains why the NAND gate always presents the lowest static power consumption for the three designs.

4.1.4 Impact on the SET cross-section

To analyze the hardening impact on the charge collection mechanism and on the SET cross-section, the layout information of each design from Figure 4.7 is used for the SET estimation in our methodology. Using the SET analyzer presented in Section 2.4 the SET cross-section is calculated for each design for a particle LET ranging from 2.5 to 78 $MeV.cm^2/mg$. Figure 4.9 provides the log-log representation of the SET cross-section curves for the NAND gates. The cross-section was calculated for each input signal combination and the arithmetic mean for each particle LET is shown. For 2.5 $MeV.cm^2/mg$, gate sizing provided the greatest reduction on the SET cross-section, approximately 78%, while a reduction of about 24% is expected

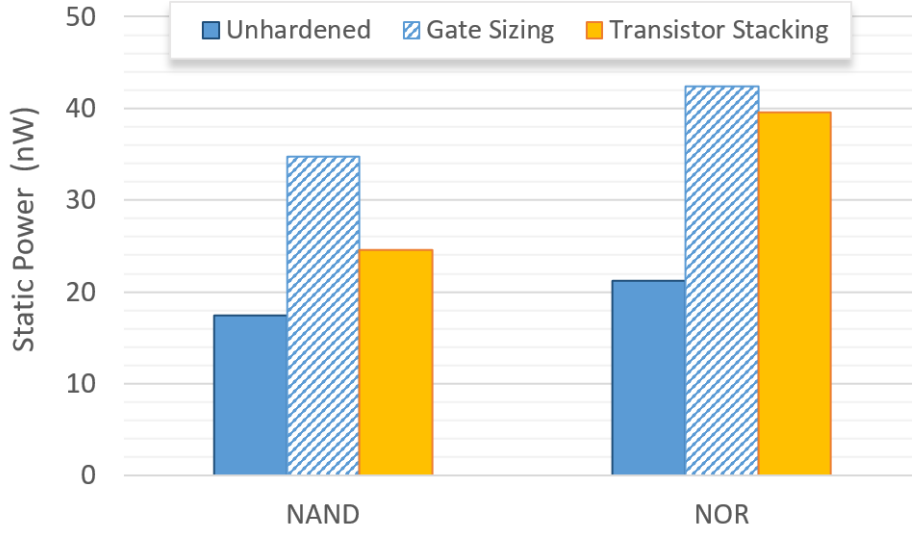


Figure 4.8: Static power consumption estimation for original, gate sizing and transistor stacking implementations of the NAND and NOR gates.

by transistor stacking approach. The radiation robustness efficiency of both techniques reduces as the particle LET increases. Due to the drain area increase shown in Table 4.2, a higher charge collection is expected. However, for $78 \text{ MeV.cm}^2/\text{mg}$, the gate sizing technique still provides a reduction on the overall SET cross-section, solely 3% of reduction. On the other hand, the transistor stacking technique increased the SET sensitivity of the circuit to about 11.7%. This increase in cross-section is related to the increase in layout area and drain regions when adopting these hardening techniques based on layout modifications. For high particle LET, the dominant effect on the circuit reliability is the charge collection efficiency enhanced by the larger transistors. A similar trend is also observed for the SET cross-section curve of the NOR gates shown in Figure 4.10. However, both techniques exhibited a higher efficiency when compared to the NAND gate. For instance, the transistor stacking provided an SET cross-section reduction of approximately 60% for the TS-based NOR gate under particles of $2.5 \text{ MeV.cm}^2/\text{mg}$, twice the reduction observed for the NAND gate. This can be explained by the reduced drain area difference between the stacked-device NAND and NOR gates and the driving capability interplay between the pull-up and pull-down

transistor networks of the two gates. To better understand these results, a closer look should be taken in respect to the input signal and the layout design of each gate.

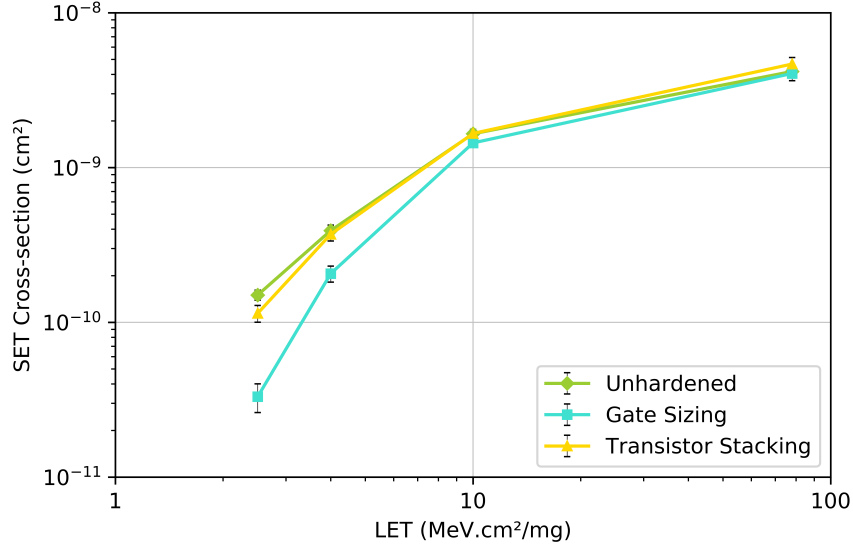


Figure 4.9: Average of the SET cross-section for each input signal the NAND logic gate: minimum sized (Original), using Gate Sizing; and Transistor Stacking.

The SET cross-section σ_{SET} for each input signal for the NAND and NOR gate under $78 \text{ MeV.cm}^2/\text{mg}$ can be seen in Figure 4.11 and Figure 4.12, respectively. The input signal combination (0, 0) is the least sensitive for the NAND gate, while for the NOR gate this is the input (1, 1). When the input signal combination (0, 0) is applied to a NAND gate, the two NMOS transistor are turned off and the two PMOS are supplying the output signal. Accordingly, a lower sensitivity is obtained for this input scenario due to the increased capacitance in the 2-series NMOS transistors and strong recovery current from the 2-parallel PMOS transistors. As the NOR gate is the complement of the NAND gate, the opposite behaviour can be observed in Figure 4.12. On the other hand, the input combination (1, 1) and (0, 0) turn out to be the most SET sensitive for the NAND and NOR gates,

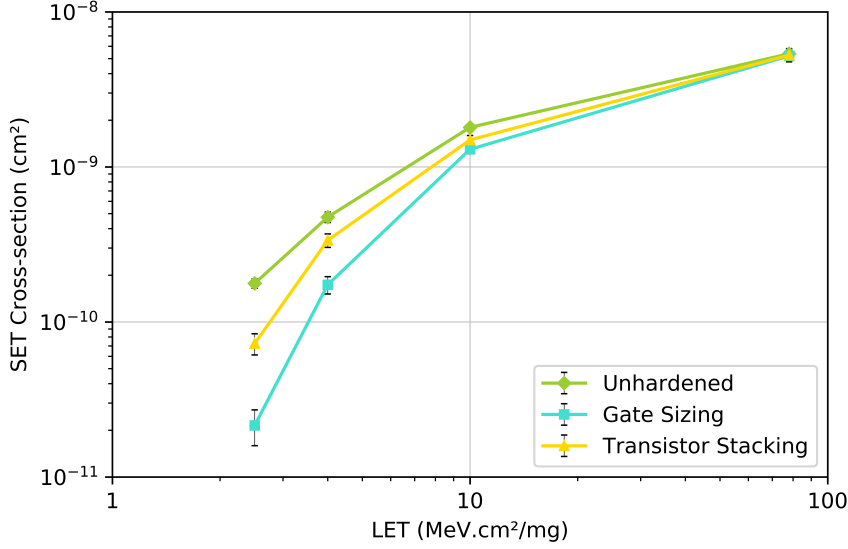


Figure 4.10: Average of the SET cross-section for each input signal the NOR logic gate: minimum sized (Original), using Gate Sizing; and Transistor Stacking.

respectively.

Notice that for the most sensitive input combination, both techniques provide a higher cross-section than the unhardened design, especially the transistor stacking. In order to explain why the TS technique worsened the reliability in some input scenarios, it is important to analyze the transistor schematics and its equivalent driving strength of each transistor network. In Figure 4.13 the transistor schematics and the equivalent driving strength of each NAND design are shown. The equivalent pull-up and pull-down driving strength of the unhardened design (NAND2_X1) are labelled as W_{peq} and W_{neq} , respectively. Based on the parallel and series associations, an estimation of the driving strength of the GS-based and TS-based designs are shown. As expected, the NAND2_X2 (GS-based design) presents $2\times$ the driving strength of the NAND_X1, for both pull-up and pull-down transistor network. However, the NAND4_X1 is logically used as a 2-input NAND gate (TS-based design), only the pull-up network has the driving strength increase

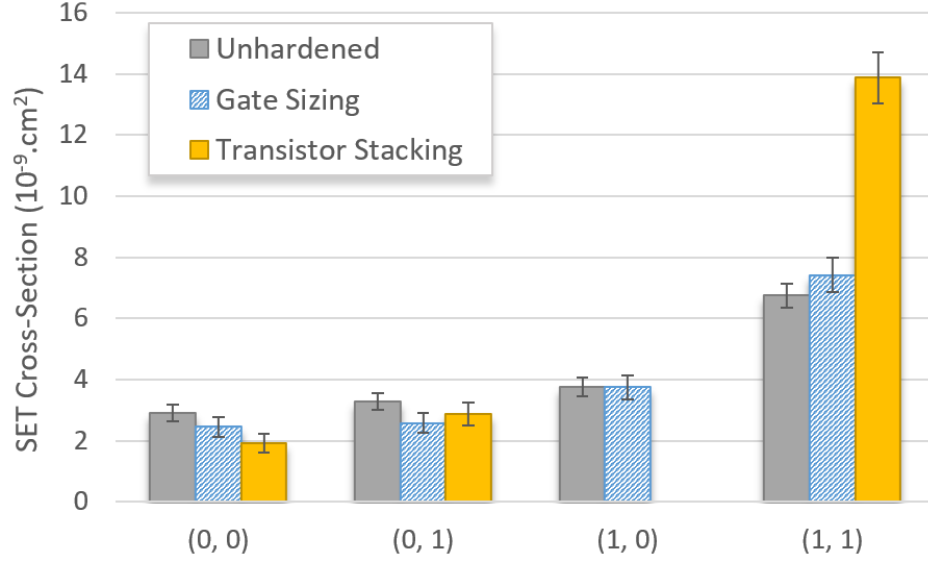


Figure 4.11: SET cross-Section for each input signal combination of the NAND gate under $78 \text{ MeV} \cdot \text{cm}^2 / \text{mg}$.

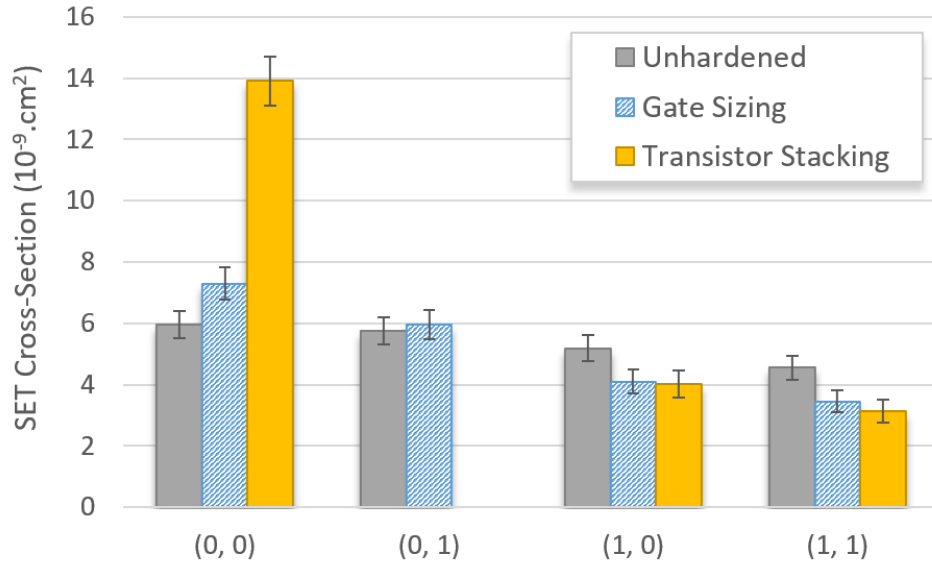


Figure 4.12: SET cross-section for each input signal combination of the NOR gate under $78 \text{ MeV} \cdot \text{cm}^2 / \text{mg}$.

while the pull-down network has its strength reduced by $1.5\times$, explaining the result observed for the input (1, 1) in Figure 4.11. Considering the worst-case input scenario, in the transistor-stacked NAND (NOR) design, all radiation sensitive transistors are PMOS (NMOS) devices. Consequently, the 4-stacked NMOS transistors in the NAND pull-down network are providing the restoring current to counteract the parasitic SET pulse from the PMOS devices.

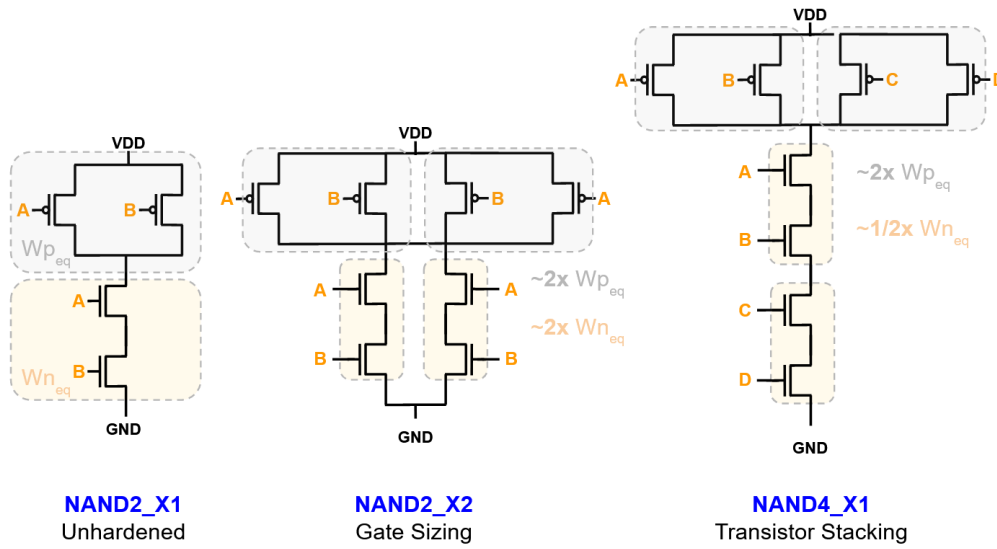


Figure 4.13: Transistor schematics and the equivalent driving strength of NAND2_X1 (unhardened), NAND2_X2 (Gate Sizing) and NAND4_X1 (Transistor Stacking).

However, transistors in series provide less current drive due to the increased effective resistance, leading to performance degradation and also larger SET pulse width and increased cross-section. Additionally, the total drain area of PMOS devices in the TS-based NAND design is twice the area of the unhardened one, inducing a higher collected charge. These can be also confirmed in Figure 4.14, which the SET pulse width measurements for each technique applied on the NAND gate are provided. The unhardened and gate sized designs present similar pulse width mean and maximum while the transistor stacking design can have a maximum SET pulse width more than $2\times$ larger than the unhardened design. As expected from the previous

results, the transistor stacking technique increases the overall pulse width mean due to the reduced drive strength of the stacked devices. The similar pulse width features between the unhardened and gate sizing design can be attributed to the balance between the increase of the recovering drain current and the collected charge in the upsized transistors.

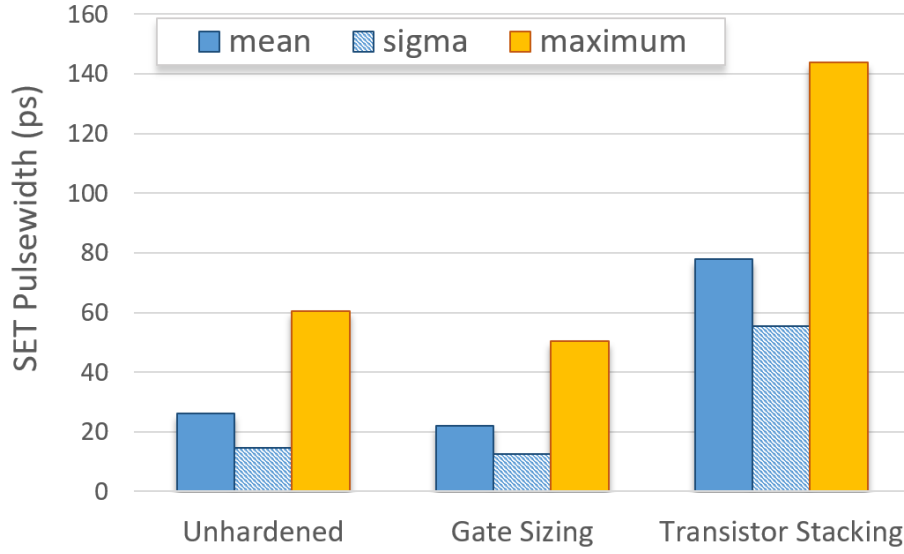


Figure 4.14: SET pulse width measurements for the NAND gate under $78 \text{ MeV.cm}^2/\text{mg}$.

Another observation from the Figure 4.11 and Figure 4.12 is that for the TS-based designs, no SET is observed for the input (1, 0) and the input (0, 1) in the NAND and NOR gates, respectively. To understand this result, we need to have a look in the transistor stacking structure of each gate. In Figure 4.15, the pull-down network of the TS-based NAND is shown, containing the 4-stacked NMOS transistors. Considering the input (1, 0), which no SET was observed in the output, the sensitive transistors are placed next to the ground supply and far from the output. In this case, whenever a particle hits the *off* transistor (red cross), the SET pulse is electrically masked by the 2-stacked transistor series before reaching the output of the gate. On the other hand, for the input (0, 1), the *off* transistors are placed just next to the output of the gate. Thus, whenever a particle deposits sufficient charge near the *off* transistor next to the output, one SET will be observed. This

same analogy can be drawn to the NOR gate where the 4-stacked PMOS transistors will mask any SET from the transistors placed next to the VDD supply. In summary, when adopting transistor stacking: (1) the transistors placed far from the output of the gate will be very likely hardened to any SET due to the electrical masking effect inherent of the stacking structure; (2) the worst-case input scenario is worsened due to the reduced driving capability of the series transistors in the stacking structure.

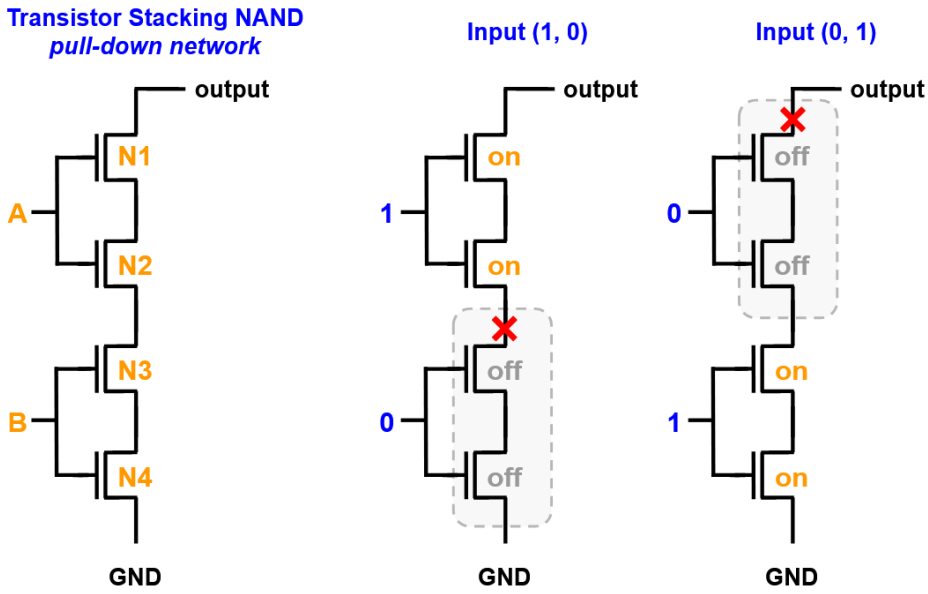


Figure 4.15: Pull-down transistor network of the TS-based NAND gate and the implications of input (1, 0) and (0, 1). Particle hits are represented by a red cross.

4.2 Transistor Folding (TF)

Transistor folding layout is widely used in digital and analog circuit design to achieve improved performance and regularity in VLSI circuits [135]. When larger transistors need to be employed, but it exceeds the fixed cell height of a given circuit design, the transistor folding layout technique is employed. The folding technique consists in connecting parallel transistors with reduced channel width to achieve a large overall width. Given a transistor

with a channel width W , the same W/L ratio, thus the same drive strength, can be achieved by connecting n transistors with channel width equals to W/n . Figure 4.16 illustrates the principle of folded transistor layouts in the case of a double-finger transistor. This layout technique divides the drain and source area into smaller partitions. Depending on the number of fingers and the connections, the drain area can be greatly reduced. For instance, instead of using the SDS connection shown for the double-finger layout, the circuit designer could have used the DSD connection and limiting the drain area reduction. Due to the reduced source and drain areas, the diffusion-to-well capacitance is also reduced.

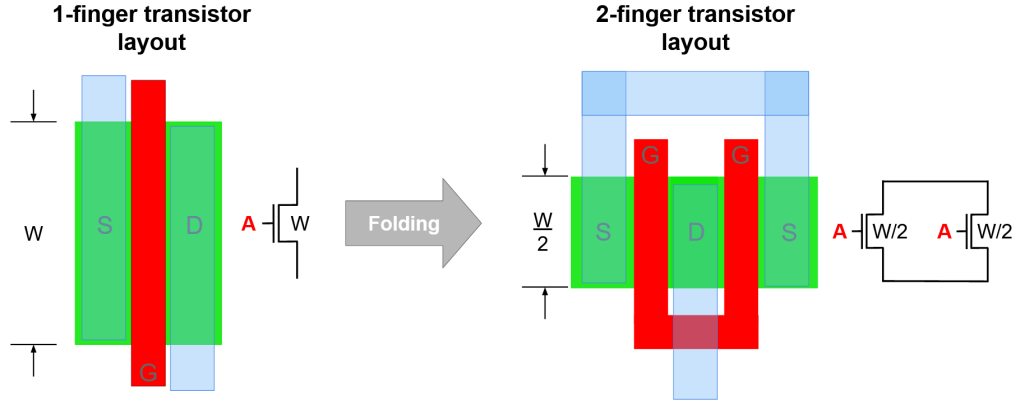


Figure 4.16: Transistor Folding Layout technique

Considering radiation effects, this technique provides a reduced collecting drain area while maintaining the same drive strength. The transistor size of the folded designs can be calculated following Equation 4.2, where W_F is the width of each folded transistor, N_F is the number of fingers, and W is the transistor width in the original design.

$$W_F = \frac{1}{N_F} \times W \quad (4.2)$$

The transistor folding technique can be adopted along with other hardening techniques such as gate sizing or dummy transistors/gates. The work in [136] was the first to propose transistor folding along with gate sizing to harden a circuit against both SEUs and SETs. A 3D mixed-mode TCAD

(Technology Computer-Aided Design) simulation was carried out to analyze the SET pulse characteristics considering alpha particle and heavy ions hit on the center of the drain junctions [136]. Different from the sizing approach, which increases the circuit drive strength at the cost of increased drain area, transistor folding is able to reduce the transistor drain area while keeping the same drive strength. The transistor sizing was able to improve the robustness only for low-energy particles while the transistor folding showed also improvement when considering high-energy particles [136][137]. In [138], different well structures and layout topologies were studied to evaluate the Propagation-Induced Pulse Broadening (PIPB) effect in inverter chains. Accordingly, a double-finger inverter chain was compared against a single-finger inverter chain. In agreement with [136], the heavy-ion results show a reduction on the overall SET pulse width, but minimum influence in the PIPB effect. Inverter chains hardened with guard rings were also evaluated using single and double-finger layout configurations with laser irradiation in [69]. Again, results showed an insignificant pulse-broadening factor for the folded inverter chain, however, a wider SET pulse width average was observed in this case [69]. The authors attributed this to the larger spacing between the drain junctions and the guard rings in the folded design, which limits the charge collection reduction provided by the guard rings. Most of the studies have provided analysis for chains of inverters, and mainly for 2-finger layout configurations. In this section, the transistor folding is applied on an inverter, NAND and NOR gates, and analyzed through layout-based predictive Monte Carlo simulations. Furthermore, the analysis of diffusion splitting along with transistor folding is provided to overcome the area overhead of multiple-finger designs.

The target circuit layouts were fully designed following a commercial Process Design Kit (PDK) in a bulk 65nm technology. Additionally, all circuits are compatible with a standard-cell library approach. Minimum width, spacing and alignment/symmetry of each layer is carefully addressed to provide compatibility among the standard cells of the target technology. The cell height is set to 13 tracks of metal pitch, i.e. $2.6\mu m$ high. To provide flexibility in cell routing, the metal 1 (M1) is primarily used for the intra-cell

connections, except for some cases in which metal 2 (M2) is used horizontally. The PMOS transistor width is $760nm$ while the NMOS transistor width is $540nm$. To analyze exclusively the impact of the folded layouts, the equivalent gate sizing was kept the same for all cases. After all circuit designs are DRC (Design Rule Check) clean, LVS (Layout Versus Schematic) checked and logic and electrical characterization is performed, the collecting drain area information can be extracted from the GDS (Graphical Design System) format file and submitted to the MC-Oracle tool [43]. All circuits were driving a fan-out 1 (FO1), i.e. an inverter was coupled to its output signal. Only the SET pulses with peak voltage higher than 0.6 V (half the supply voltage) are considered for the cross-section calculation. In addition to the double-finger designs (Figure 4.16), quadruple-finger layout configurations are also considered in this work as shown in Figure 4.17. However, one of the drawbacks of increasing the number of fingers in the folding technique, while maintaining the same gate sizing, is the increase in layout area due to the misuse of the fixed cell height. Thus, to overcome the area increase, a Diffusion Splitting (DS) layout technique is proposed and shown in Figure 4.17. Instead of using a single strip of active diffusion, a 2-row stacked diffusion transistor is used. Besides reducing the area overhead of the folding technique, DS improves the metal connection routability maintaining the same W/L ratio and the number of gate fingers. To deepen this analysis, the impact on the in-orbit SET rates for heavy ions and protons and the effect of voltage fluctuation are also presented in the following.

4.2.1 Impact on the SET cross-section

This work analyzes the applicability of the transistor folding layout technique to be used as an RHBD technique in standard-cell libraries. The layout area information for the original design (unhardened version) of the inverter, NAND and NOR gate along with the increase factor for its folded designs is shown in Table 4.3. For the three cells analyzed in this thesis, the double-finger layout configuration exhibited an area increase of approximately $1.5\times$ the original unhardened single-finger layout area. An area increase around

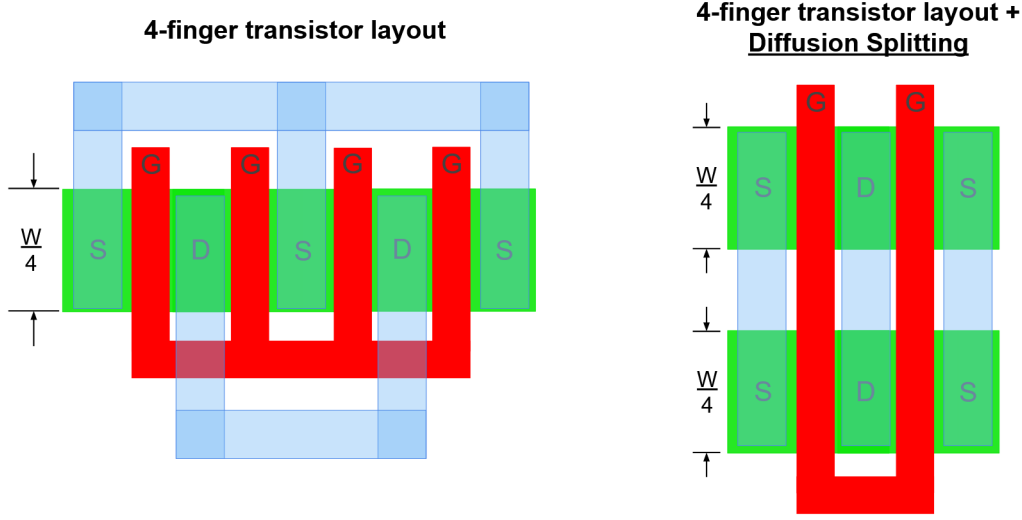


Figure 4.17: Standard quadruple-finger folded transistor layout vs. folded transistor layout with Diffusion Splitting (DS) technique in which the diffusion strip is split into 2 strips and placed vertically aligned within each other.

$2.5\times$ is expected when using quadruple-finger layout designs. However, if DS is used, the area overhead for the four-finger designs can be reduced to the same observed in the two-finger designs, that is, approximately $1.5\times$ greater than the original designs. Thus, DS provides an area reduction of 36% and 42% for the four-finger inverter and NAND/NOR cells, respectively. Once again, both NAND and NOR gates provide the same layout area in the original and folded designs due to the layout design regularity inherent of standard-cell libraries. In Figure 4.18, the simplified layout of the NAND designs containing only M1, diffusion, and poly-layers are shown. In standard-cell methodology, a fixed cell height is defined to provide regularity. Thus, as the number of fingers is increased, the cell width is increased and, consequently, the cell layout increases. As the transistor sizing is kept the same, the DS can be applied to reduce the impact on the layout area, as shown in Figure 4.18. For the sake of compactness, the layout design for the inverter and NOR gates are omitted.

The SET cross-section σ_{SET} for the inverter designs under particle LET of $78.23 \text{ MeV.cm}^2/\text{mg}$ is shown in Figure 4.19. The folded designs have

Table 4.3: Total area for each original unhardened cell layout design (μm^2) and the increase factor for its correspondent folded designs

	Original design (μm^2)	Folded designs		
		2-finger	4-finger	4-finger with DS
Inverter	1.560	$\sim 1.5x$	$\sim 2.4x$	$\sim 1.5x$
NAND2	2.444	$\sim 1.5x$	$\sim 2.6x$	$\sim 1.5x$
NOR2	2.444	$\sim 1.5x$	$\sim 2.6x$	$\sim 1.5x$

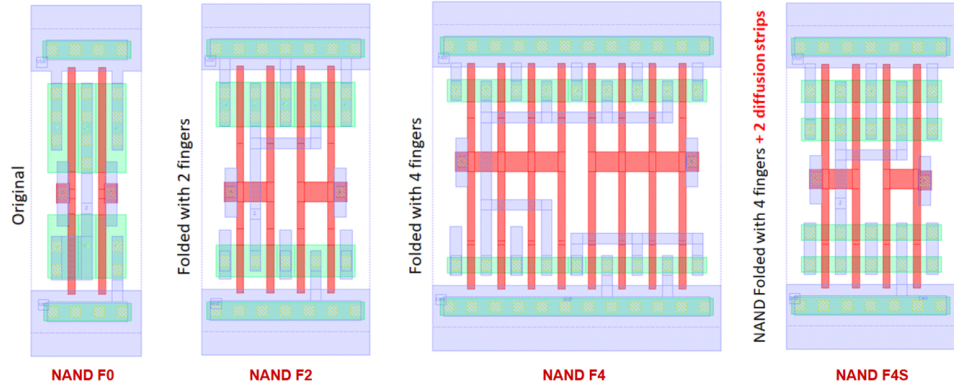


Figure 4.18: Simplified layout design of NAND F0 (no folding, unhardened), NAND F2 (2-finger design), NAND F4 (4-finger design) and NAND F4S (4-finger design with diffusion splitting). For clarity, only the metall (blue), active diffusion (green) and poly layers (red) are shown.

shown similar σ_{SET} for input 1 and input 0. Thus, using transistor folding may reduce the SET sensitivity dependence on the input signal in the inverter design at high LET. On average, the folded designs provide lower sensitivity than the unhardened design with the greatest σ_{SET} reduction for the 2-finger layout configuration, approximately 42%. The 4-finger inverter shows improvement solely for the input 1, however, despite the area reduction, DS also reduced the σ_{SET} . To analyze the folding impact for low particle LET irradiation, Figure 4.20 presents the SET cross-section for the inverter designs considering heavy ions with $LET = 5.43 \text{ MeV.cm}^2/mg$. In this case, the greatest σ_{SET} reduction is observed for the 4-finger inverter with DS, about 37%. It can be observed that, for low LET, the σ_{SET} reduces with the

increase of the number of fingers N_F , in agreement with 3D TCAD results obtained in [136]. As N_F increases, the collecting regions are reduced and sparsely distributed along the layout, then the charge sharing at low LET is limited. Thus, less folded transistors are affected by a single particle hit, leading to an improvement in the efficiency of the technique in reducing the σ_{SET} .

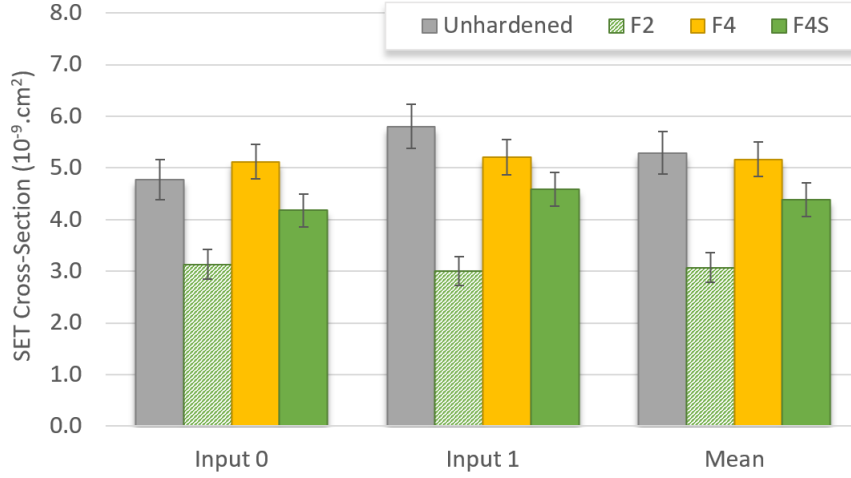


Figure 4.19: SET cross section for the inverter designs under $LET = 78.23 \text{ MeV.cm}^2/mg$ considering input 0, input 1 and the mean value.

Figure 4.21 depicts the mean SET cross-section curve for each inverter cell design considering the input 0 and input 1. Besides providing lower SET cross-section, the 4-finger designs (with and without DS) showed a higher threshold LET than the original design. For LET lower than $10 \text{ MeV.cm}^2/mg$, the 4-finger inverter with DS is preferred, while for higher LET the 2-finger design is more suitable.

Considering the NAND designs, Figure 4.22 presents the SET cross-section σ_{SET} for particle LET equals to $78.23 \text{ MeV.cm}^2/mg$. Except for the 2-finger design, the folded designs provided a higher mean σ_{SET} . At high LET, the hardening efficiency of folded transistors is limited due to the complex input dependence observed on the cross-section. The folded NAND designs show a stronger input dependence than the original unhardened version, leading to a similar or lower σ_{SET} only for inputs (0, 0) and (0, 1). The

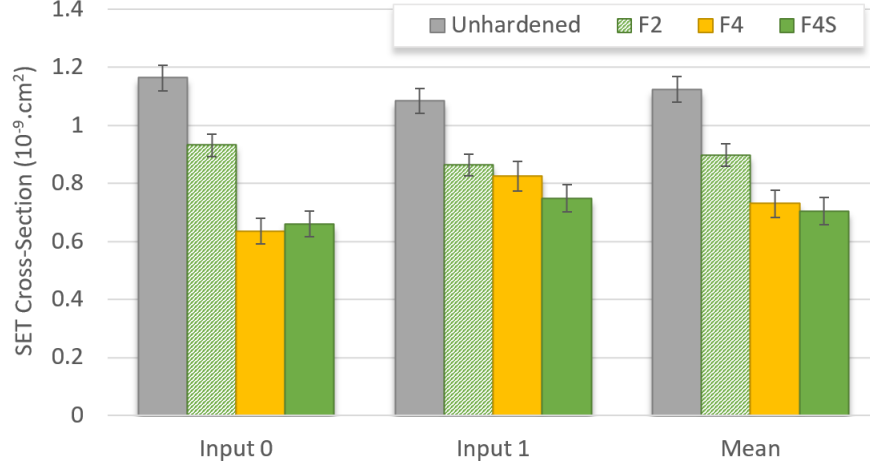


Figure 4.20: SET cross section for the inverter designs under $\text{LET} = 5.43 \text{ MeV.cm}^2/\text{mg}$ considering input 0, input 1 and the mean value.

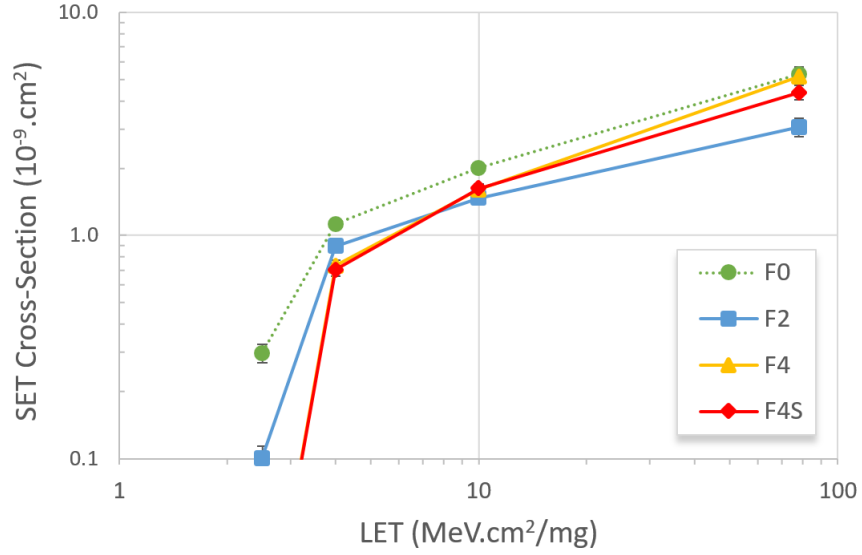


Figure 4.21: Log-Log representation of the mean SET cross section curves for the inverter designs. No event was observed in the 4-finger designs (triangle and rhombus curves) for LET lower than $5.43 \text{ MeV.cm}^2/\text{mg}$.

worst-case input scenario for NAND gates is the input (1, 1), and, in this case, transistor folding exacerbates the SET sensitivity up to approximately 62% in the 4-finger design.

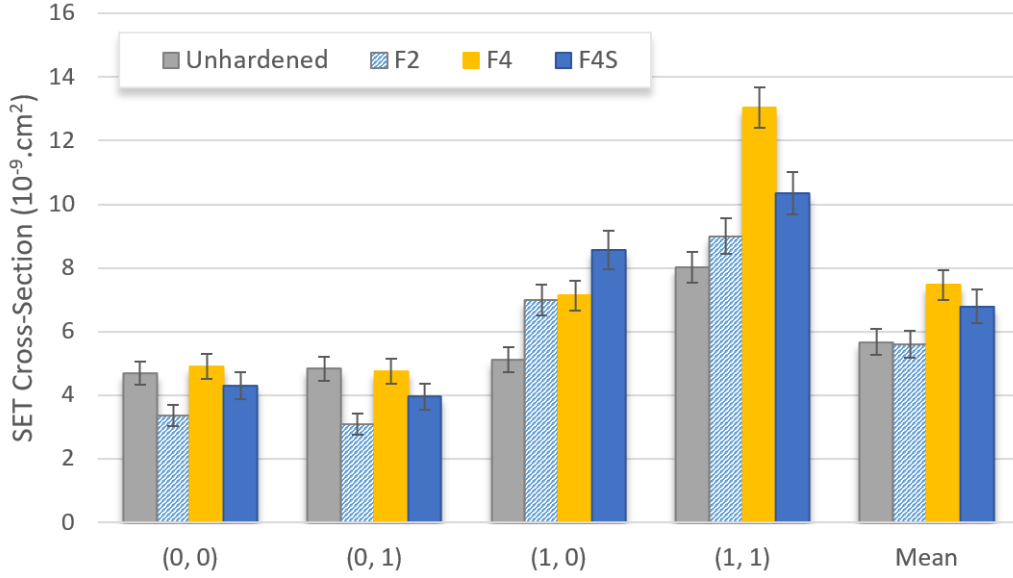


Figure 4.22: SET cross section for the NAND designs at $LET = 78.23 \text{ MeV.cm}^2/mg$ for each input signal and the mean value.

As observed for the gate sizing and transistor stacking designs in the previous section, the layout-based hardening techniques can worsen the SET robustness in the worst-case input scenario. For input (1, 1), all PMOS devices are sensitive to a particle hit, besides the lower restoring capability of NMOS devices, PMOS transistors collect more charge due to its larger drain area [139]. Similarly, in the NOR case, the input (0, 0) is the worst-case input scenario and it shows increased σ_{SET} when adopting folded transistors as shown in Figure 4.23. To reduce the increased sensitivity at the worst-case input scenarios, transistor folding can be applied only in the pull-down (or pull-up) network to balance the overall SET sensitivity. The asymmetric designs are also considered in this work and it is discussed in the following section. Despite the poor hardening performance for high particle LET, the folded designs have shown great reduction on the overall SET cross-section for low LET. Considering the NAND design under particle LET

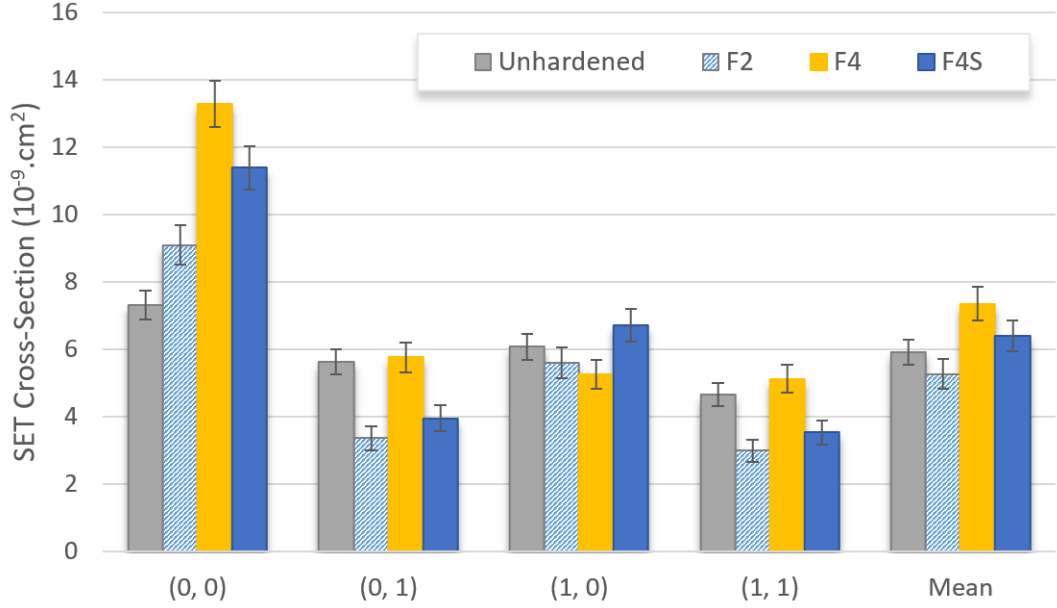


Figure 4.23: SET cross section for the NOR designs at $LET = 78.23 \text{ MeV.cm}^2/mg$ for each input signal and the mean value.

of $5.43 \text{ MeV.cm}^2/mg$ shown in Figure 4.24, the 4-finger design showed the lowest mean σ_{SET} , and similar sensitivity is obtained with DS. Thus, it is important to note that, for low LET, increasing the N_F also improves the overall SET cross-section σ_{SET} as observed for the inverter design.

However, the worst-case input scenario is still worsened by the technique, for instance, in the F2 NAND design. The full understanding of the impact on the SET cross-section can be better visualized through the curves in Figure 4.25 and Figure 4.26, for the NAND and NOR designs, respectively. As previously mentioned, for high LET, the folded designs can show the same or worse radiation robustness than the original unfolded version (F0 designs). At $10 \text{ MeV.cm}^2/mg$, the folded designs start to provide better or similar cross-section than the observed for the F0 designs. For LET lower than $10 \text{ MeV.cm}^2/mg$, the 4-finger design (F4) is preferred for both NAND and NOR. Except for the 2-finger NAND (F2), all other folded designs provided a higher threshold LET than the unfolded design. To summarize the impact of folded designs under the effects of low LET particles, Table 4.4 contains

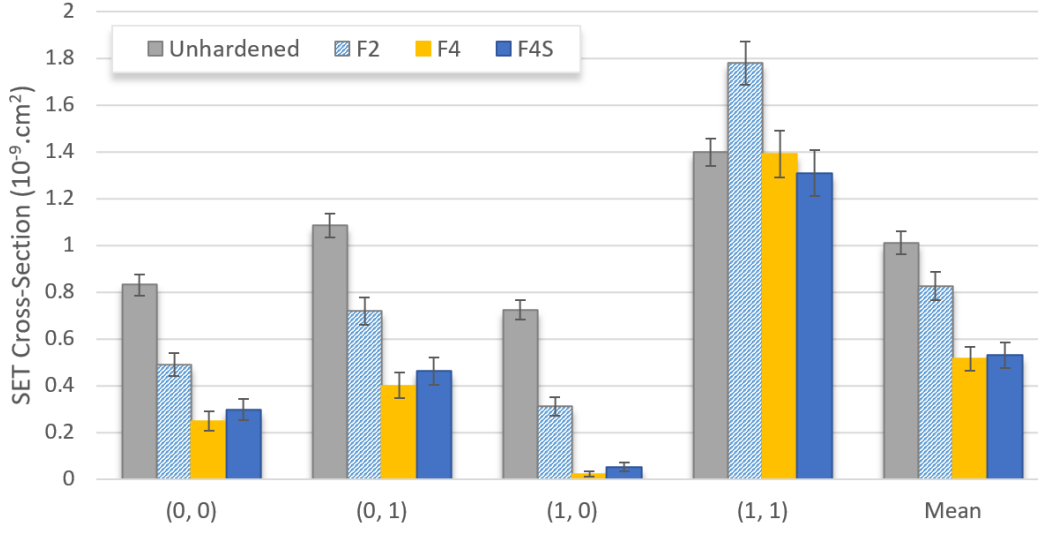


Figure 4.24: SET cross section for the NAND designs at $LET = 5.43 \text{ MeV.cm}^2/mg$ for each input signal and the mean value.

the SET cross-sections for particle LET equals to $5.43 \text{ MeV.cm}^2/mg$. For this LET, the reduction on the overall SET cross-section can range from 5% to approximately 50%. The best design option would be the 4-finger with DS for the inverter, and 4-finger design for the NAND/NOR gates.

Table 4.4: SET cross-section for each original cell layout design ($10^{-9}.cm^2$) for particle $LET = 5.43 \text{ MeV.cm}^2/mg$ and the decrease percentage for its correspondent folded designs

	Original design	Folded designs		
		2-finger	4-finger	4-finger with DS
Inverter	1.124	-20%	-35%	-37%
NAND2	1.010	-18%	-49%	-48%
NOR2	0.736	-5%	-41%	-33%

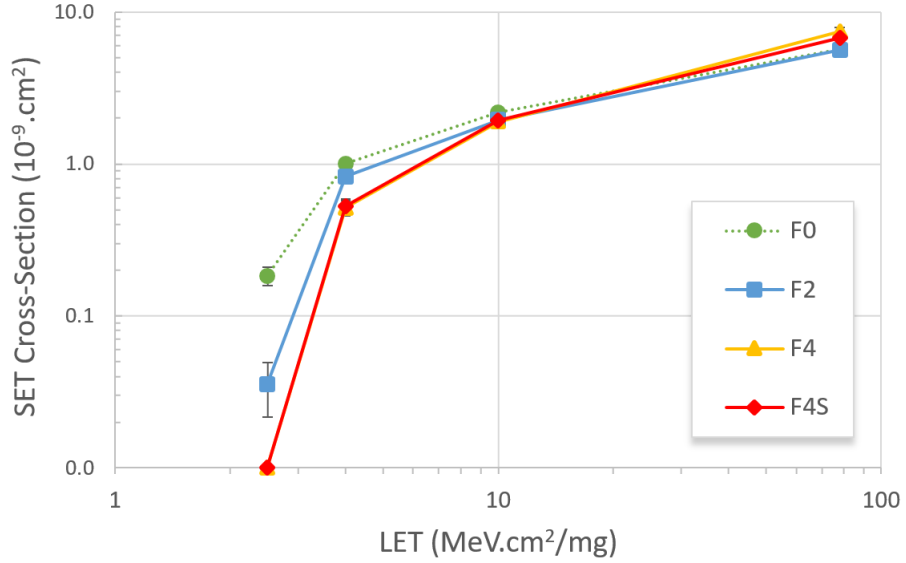


Figure 4.25: Log-log representation of the mean SET cross section curves for the NAND designs (F0: unfolded, F2: 2-finger, F4: 4-finger, F4S: 4-finger design with diffusion splitting). No event was observed in the F4 and F4S designs (triangle and rhombus curves) for LET lower than $5.43 \text{ MeV.cm}^2/\text{mg}$.

4.2.2 Asymmetric designs

As observed in the last subsection, transistor folding can induce a higher SET cross-section for the worst-case input scenario of the NAND and NOR circuits. Thus, in this section, a deep analysis is provided in order to enable a better usage of the TF technique. Figure 4.27 illustrates the transistor network of the NAND gate and its truth table. For the worst-case scenario, highlighted in red, the *off* transistors, which are sensitive to particle hits, are issued from the pull-up network, i.e. PMOS devices. So far, the folding technique has been equally applied to both pull-up and pull-down networks. To study the impact of asymmetric designs, the 2-finger design and the 4-finger design with DS are explored considering the transistor folding only in one of the networks.

The folding technique was applied only in the NMOS devices for the NAND gate, and only in the PMOS devices for the NOR gate. The SET cross-sections are shown in Figure 4.28 for each design considering only the

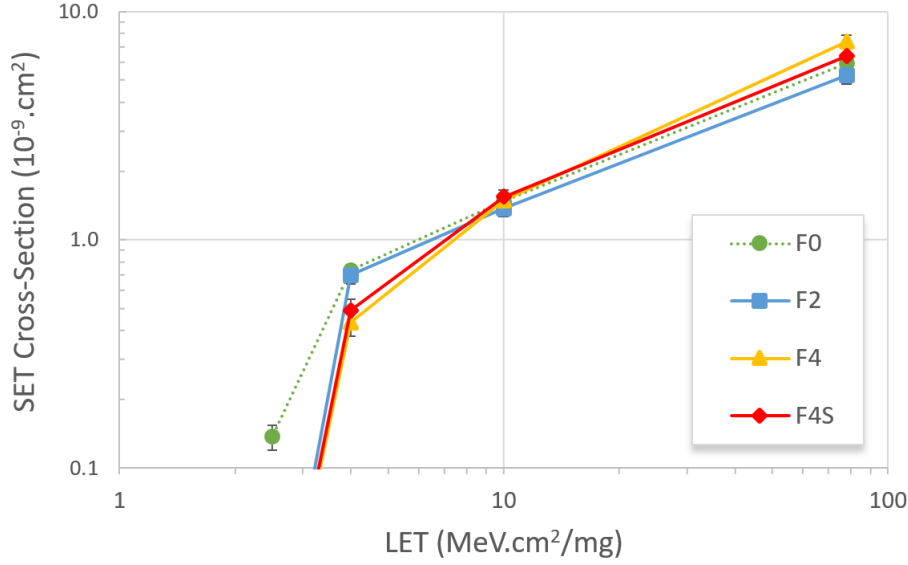


Figure 4.26: Log-log representation of the mean SET cross section curves for the NOR designs (F0: unfolded, F2: 2-finger, F4: 4-finger, F4S: 4-finger design with diffusion splitting). No event was observed in the folded designs for LET lower than $5.43 \text{ MeV.cm}^2/\text{mg}$.

worst-case input scenario, i.e. the input combination (1, 1) and (0, 0) for the NAND and NOR, respectively. The number indicates the fingers, N/P indicates when only NMOS/PMOS devices are folded, and S indicates when diffusion splitting is adopted. For instance, the F4NS circuit is the 4-finger design with only NMOS devices folded and with diffusion splitting. This nomenclature is used in the remaining of this chapter for the sake of compactness. For the $\text{LET} = 78.23 \text{ MeV.cm}^2/\text{mg}$, the asymmetric designs were able to improve the SET robustness of the circuits. The greatest reduction on the cross-section was observed for the 4-finger designs. The NAND F4NS circuit provides a reduction of 26.5% when compared to the NAND F4S circuit, while the NOR F4PS circuit has approximately 29.7% of reduction compared to the NOR F4S.

However, when adopting the asymmetric designs, not only the worst-case input SET cross-section is affected as can be seen in Figure 4.29 and Figure 4.30 in which the SET cross-section σ_{SET} for each input signal and the mean value are shown for the NOR and NAND gate, respectively. Due to

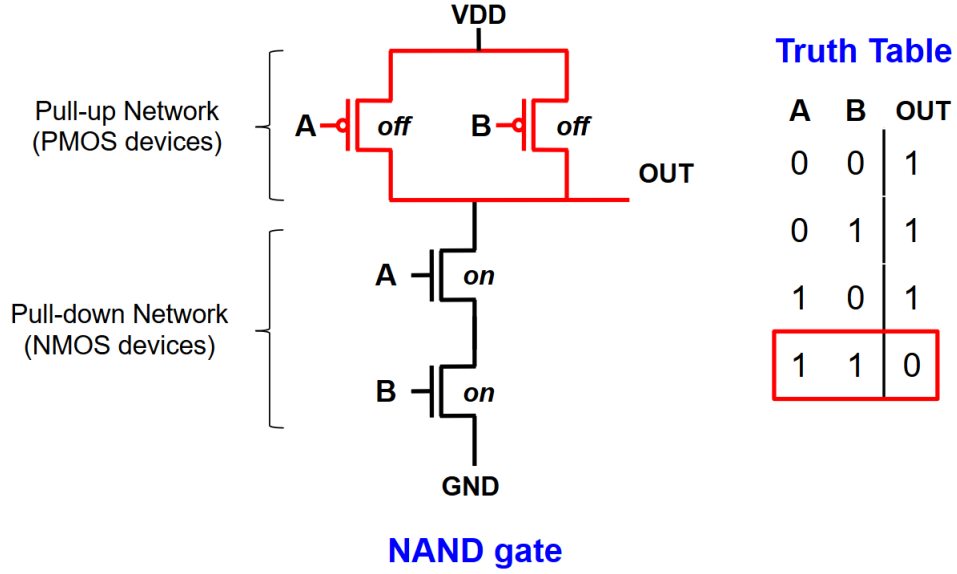


Figure 4.27: Transistor network of an NAND gate and its truth table. *On*-state and *off*-state are indicated for the transistors considering the worst-case input scenario, i.e. input (1, 1).

a small increase in the cross-section for the inputs (0, 1), (1,0) and (1, 1), the mean SET cross-section reduction for the NOR F4PS circuit is 13%, while the NOR F2P circuit provides approximately the same mean SET cross-section than the NOR F2 circuit. The same observations can be done in the results for the NAND designs in Figure 4.30. These results reaffirm the importance of considering input dependence when hardening digital logic circuits. To complete the analysis, the impact of adopting transistor folding, diffusion splitting and asymmetric designs is also evaluated under voltage variability in terms of SET cross-section values and in-orbit SET rates.

In addition to radiation effects, electronic circuits are susceptible to dynamic environmental variability, such as voltage fluctuations due to voltage drop and current derivative di/dt noise [140]. Previous works have shown that voltage variability reduces the reliability of circuits, especially when considering harsh environments under radiation effects [141, 142]. In [141], voltage variability has shown to reduce the threshold LET of different XOR topologies in FinFET and Trigate devices. Also, a reduction in the elec-

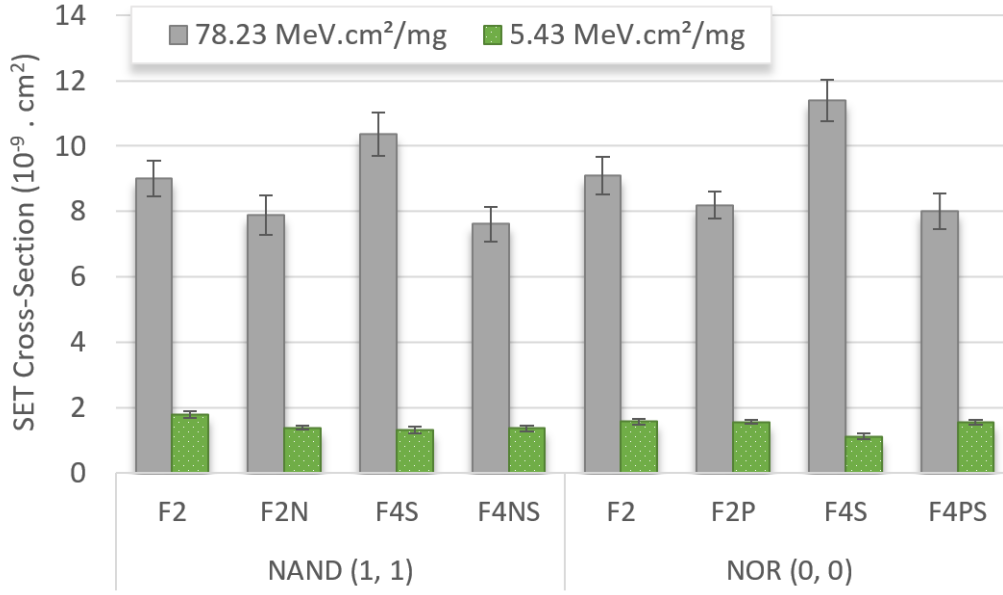


Figure 4.28: SET cross-section for symmetric and asymmetric designs of 2-finger and 4-finger with diffusion splitting of NAND and NOR gates in the worst-case input scenario, i.e. input (1, 1) and input (0, 0), respectively.

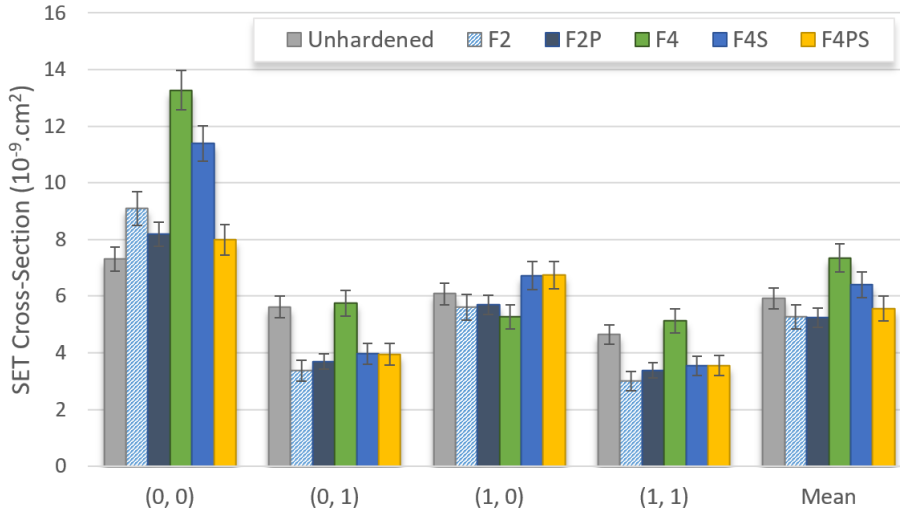


Figure 4.29: SET cross section for the NOR designs at $\text{LET} = 78.23 \text{ MeV.cm}^2/\text{mg}$ for each input signal and the mean value.

trical masking capability of the gates and increase in the SET pulse width is observed in [142]. The IR drops due to the parasitic resistance of the

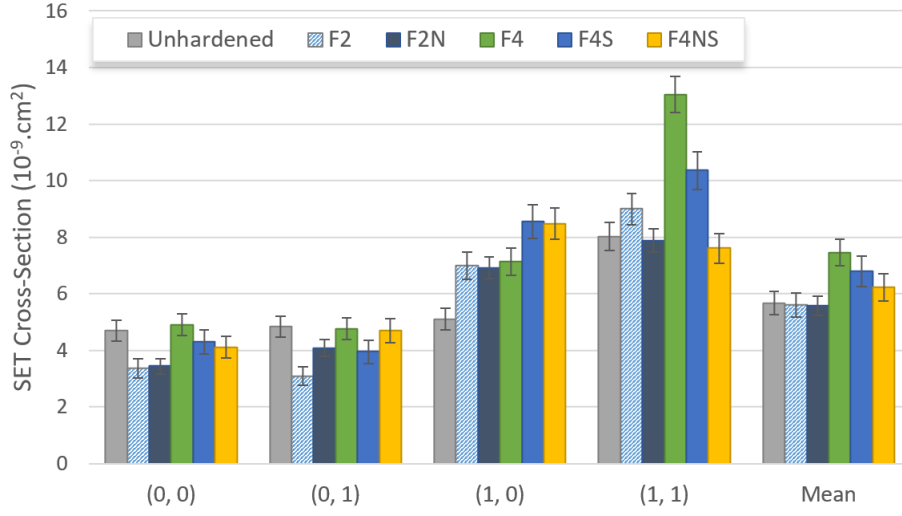


Figure 4.30: SET cross section for the NAND designs at $LET = 78.23 \text{ MeV.cm}^2/\text{mg}$ for each input signal and the mean value.

power grids can lead to $\pm 10\%$ variation on the supply voltage. Accordingly, all circuits were analyzed considering a voltage drop of -10% of the nominal supply voltage of the technology, i.e. 0.12V . The SET cross-section and the variation $\Delta\sigma_{SET}$ (in %) are shown for each circuit in Figure 4.31. As expected, a reduction on the supply voltage of the circuits reduces the driving capability and consequently reduces the recovery efficiency, leading to a higher σ_{SET} . The usage of diffusion splitting technique induces insignificant impact on the circuit robustness to voltage variability as similar SET cross sections are obtained for the F4 and F4S circuits. However, for the 3 logic gates (inverter, NAND and NOR), the F4 and F4S circuits showed the greatest σ_{SET} increase, ranging from 50% to 70% . Thus, as the number of fingers is increased, the circuit becomes more sensitive to the voltage drops. However, the asymmetric designs have shown to reduce the impact of voltage variability on the SET cross sections. Considering only the inverter designs, the F4S circuit shows the lowest σ_{SET} at nominal voltage but it is the most sensitive to voltage drops, along with the F4 circuit. On the other hand, the F2 circuit provides the lowest σ_{SET} at -10% of the supply voltage, and also the lowest variation on σ_{SET} .

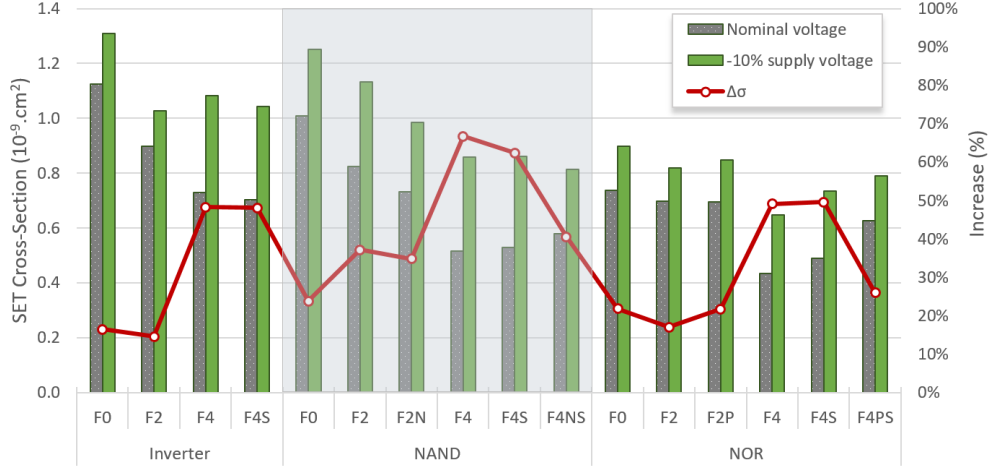


Figure 4.31: SET cross section considering a voltage drop of 10% over the nominal supply voltage and a particle LET of $5 \text{ MeV.cm}^2/\text{mg}$. The percentage increase $\Delta\sigma_{SET}$ in the cross section is also shown in red line.

For the NAND gate, the F4 circuit provides the lowest σ_{SET} at nominal voltage, but it increases up to 66% with 10% reduction on the supply voltage. In this case, the unhardened circuit is the least sensitive design to voltage variation, leading to approximately 24% of increase in the σ_{SET} . However, under voltage drop, the lowest σ_{SET} is observed for the asymmetric design F4NS circuit. Compared to the unhardened NAND circuit, when the voltage fluctuation is considered, the F4NS reduced the σ_{SET} up to 35%. For the NOR gate, similarly to the NAND gate, the F4 circuit provides the lowest σ_{SET} at nominal voltage, but high sensitivity to the voltage drops, resulting in approximately 49% increase in the σ_{SET} . However, it still provides the lowest σ_{SET} during voltage fluctuation. The diffusion splitting used in F4S increased its cross-section, but it still provides a lower σ_{SET} than the F2 circuit, with the same area overhead.

4.2.3 Impact on the in-orbit SET rate: LEO and ISS orbits

To study the impact of adopting these techniques in a radiation environment, the in-orbit SET rates were estimated for the Low-Earth Orbit

(LEO) and International Space Station (ISS) orbits. The OMERE software was used based on the SET cross-section curves calculated with the current database provided by MC-Oracle. OMERE is a tool dedicated to the analysis of space environment and radiation effects on electronics developed by TRAD and CNES [22]. The Integral Rectangular Parallelepiped (IRPP) approach is used to predict the SET rate, i.e. it is calculated by the convolution of the heavy-ion cross section data with the particle flux in the aforementioned orbits. This approach is a standard method specified by the European Cooperation for Space Standardization (ECSS) [52]. The NASA AP8MIN trapped radiation model is used for the proton fluxes under solar minimum conditions [143]. For the Galactic Cosmic Rays (GCR) fluxes, the international standard ISO 15390 model is used [144]. A fixed shielding of 1 g/cm^2 is considered. The calculated heavy-ions SET rates are shown in Figure 4.32. Firstly, it can be noticed that all folded designs exhibit lower rates than its unhardened version (F0 circuit) for both orbits. In the case of the inverter, the F4S circuit provides the lowest rate with a reduction of approximately 82% and 77% in the ISS and LEO orbit, respectively. Similarly, for the NOR gate, the F4S showed the lowest SET rate. The folded transistor and diffusion splitting provided about 66% and 55% of reduction on the SET rate for the ISS and LEO orbit, respectively.

On the other hand, the F2 circuit is expected to have a lower rate for the NAND gate. Although the cross-section calculations were performed for heavy ions, the protons are expected to dominate the SEE rates in the LEO and ISS orbits. Due to its improved accuracy when compared to analytical models, the METIS method [145–147] was used to predict the proton-induced SET cross section curves from the heavy ions data. The sum of the SET rate induced by heavy ions and protons are shown in Figure 4.33. As expected, the overall SET rate increased considerably. However, in this case, the F4 and F4S circuits are no longer the most hardened designs. The F2 circuits have shown the lowest rate for the inverter and NAND gate, for both orbits. For the NOR gate, the asymmetric design F2P provided the lowest rate, about 10% reduction for the two orbits. Except for the F2N, one can notice that whenever the asymmetric design approach is adopted, a reduction on

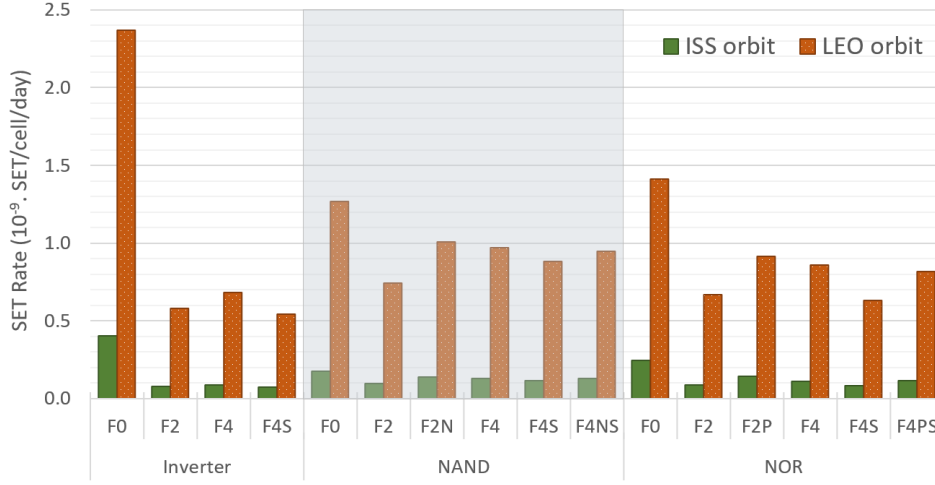


Figure 4.32: Heavy-ions SET rate estimated with OMERE [22] for each circuit and its hardened version considering the LEO (800km, 98°) and ISS (400km, 51.64°) orbit. The SET cross section average of each input signal is used.

the overall SET rate is observed.

4.2.4 Transistor Scaling and Angular Dependence

With the increasing demand of better performance and low power in critical systems, advanced technology nodes have been studied to be employed in future missions. Due to the scaling of transistors, the hardening efficiency of these techniques might be reduced as the charge sharing effects are increased in response to the close proximity of the collecting zones in the advanced technology nodes. However, in FinFET technologies, the three-dimensional structure of the transistor impacts on the charge collection process and a reduction on the charge sharing effects might be expected as shown in [148]. Further, if an SOI technology is adopted, the hardening efficiency would be highly improved due to the lack of the diffusion contribution in the charge collection [149].

Concerning the angular effect in the charge collection, folded transistors have shown a low angle dependence as investigated in [150]. As shown in Figure 4.34, only the NMOS transistors have shown an increase in the total

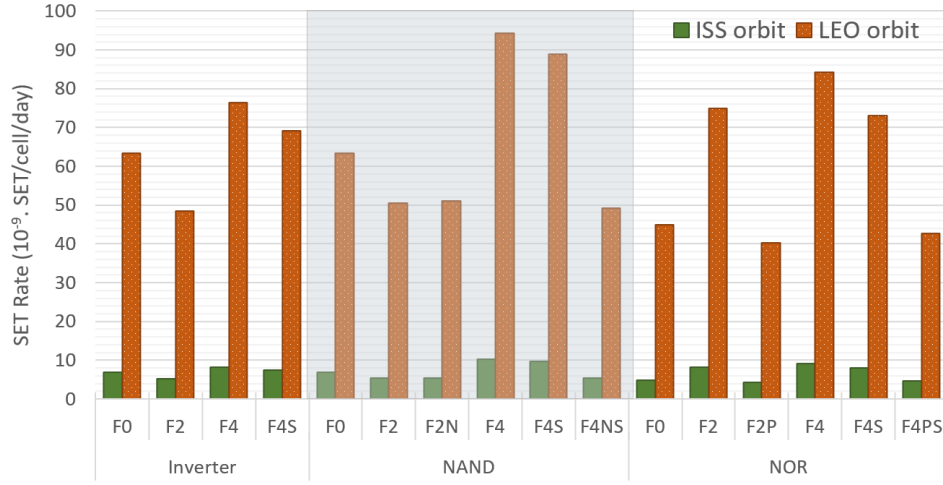


Figure 4.33: Total SET rate estimated with OMERE [22] for each circuit and its hardened version for the LEO (800km, 98°) and ISS (400km, 51.64°) orbit considering heavy ions and protons. Proton-induced SET rates are estimated with the METIS method [145]. The SET cross section average of each input signal is used.

collected charge for angled strikes. For the worst-case scenario, in which the particle strikes the center of the drain area with a tilt angle of 60°, the total collected charge of a 4-finger NMOS transistor can be 20% higher than the collected charge in original design, without transistor folding, due to charge sharing mechanisms. Thus, a very weak angle dependence can be expected in the SET cross-section of the folded designs, especially for low LET due to the reduced charge sharing between adjacent devices. Further, according to [151], deeply scaled CMOS technologies present a marginal difference on the overall charge sharing effect between normal and angled strikes.

4.3 Conclusions

Physical layout design influences the main SEE mechanisms in VLSI circuits such as charge collection and charge sharing effects. Accordingly, RHBD techniques can be adopted at layout level to improve the radiation robustness of electronic circuits. In this chapter, three RHBD techniques

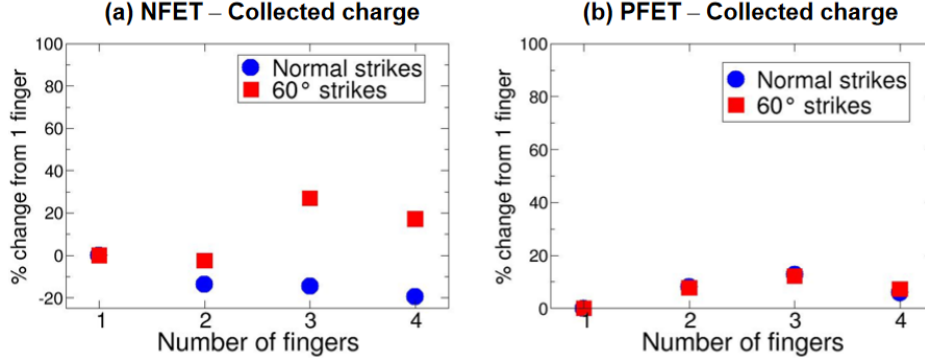


Figure 4.34: Collect Charge (CC) for normal and 60° strikes at the center of the drain area in the NFET and PFET devices for a particle LET of 40 $\text{MeV.cm}^2/\text{mg}$ [150].

exploring layout modifications were analyzed under heavy ions: gate sizing, transistor stacking and transistor folding. Firstly, the gate sizing and transistor stacking were studied based on pre-designed standard cells. The idea is to investigate how conventional standard-cell libraries can be used to maximize the reliability of VLSI systems under radiation effects. Besides the area and leakage current increase, both techniques were able to provide a reduction on the overall SET cross-section, especially for low particle LET. The NOR gate shows the greatest improvements on the SET cross-section even though transistor stacking can increase the maximum SET pulse width to $2\times$ wider than the original design. Gate sizing shows the best trade-off between area, power and reliability. However, the hardening efficiency of transistor stacking is strongly dependent on the input signal of the gate. This is a reflection to the fact that, in the stacking structure, the transistors placed far from the output of the gate will be likely unable to induce a SET pulse in the output due to the electrical masking effect. Thus, according to the application, this technique can possibly outperform gate sizing. In the next chapter, signal probability will be used in order to enhance the hardening efficiency of RHBD techniques.

After understanding the implications of adopting gate sizing and transistor stacking, the efficiency of transistor folding layout in improving the SET immunity of digital circuits is evaluated. The goal is to verify how

folded transistors can improve basic logic gates and then be applied in cell libraries. For instance, considering the cell with the minimum drive strength X1, the cell library would provide the NAND cell with different options: NAND_X1_F0 (already provided in current cell library, no folded transistor), NAND_X1_F2, NAND_X1_F4, NAND_X1_F4S and so on. The same can be applied to other logic cells with different driving strength. The results have shown that folded designs can provide lower SET cross-section in addition to the higher threshold LET than the observed for the unfolded designs. The number of fingers were also explored. At high LET, the 2-finger designs showed the best performances. However, for LET lower than $10 \text{ MeV.cm}^2/mg$, the hardening efficiency of the folded designs is expected to increase as the number of fingers is increased. Increasing the number of fingers increases greatly the final layout area. Thus, a layout technique was proposed to overcome the area overhead of multiple-finger designs. In the diffusion splitting approach, the active diffusion is split into two strips and placed vertically aligned within each other. Besides reducing the layout area, diffusion splitting may also improve the SET cross-section depending on the circuit topology, input signal and ion LET. Due to the strong input dependence of these techniques, it was also proposed to adopt asymmetric designs, i.e. applying the hardening techniques only in the PMOS or NMOS devices, depending on the worst-case input scenario of the logic gate. Voltage variability was also explored due to its impact on the reliability of deeply scaled technologies. The folded designs have shown a higher sensitivity to voltage fluctuation. However, the usage of asymmetric designs showed to reduce it. And, lastly, the in-orbit SET rates were predicted for the LEO and ISS orbits. When the SET rate is only calculated for heavy ions, all the folded designs provided lower rate than the unfolded designs. However, the protons dominate the SEE rates in the LEO and ISS orbits. When protons are taken into account, the 2-finger designs (symmetric and asymmetric) and the asymmetric 4-finger design with DS are the most hardened circuits.

5

Analysis of RHBD at Circuit-level

To complete the analysis of the RHBD techniques in different design abstraction levels, this chapter provides the assessment of circuit-level techniques. First, the charge sharing effect is evaluated considering the impact of cell placement and logic synthesis. Then, an optimization methodology is proposed to improve the overall circuit hardness through signal probability based pin swapping.

5.1 Reliability-driven Synthesis

The synthesis process in VLSI systems is a very important step when designing systems based on integrated circuits (ICs) as it defines the performance characteristics of the application. Further, besides defining the power and area characteristics of the design, it also has an important contribution to the reliability of the final synthesized circuit. Accordingly, different approaches can be incorporated into the design synthesis flow in order to improve the reliability of the circuit, for example, under radiation effects. In this context, some mitigation strategies are analyzed and proposed as a RHBD approach to be used in the logical and physical synthesis of VLSI systems.

The development of electronic circuits for space and aviation can be done using different circuit design methodologies, from field programmable gate-arrays (FPGAs) to full-custom or cell-based Application Specific Integrated Circuits (ASICs). FPGA-based designs provide fast prototyping in the cost of area and performance when compared to full-custom designs [152, 153]. However, the use of ASICs provides the best tradeoff between performance, power consumption and circuit area. One of the main design methodologies adopted in ASICs is the standard-cell methodology in which thousands of pre-designed and characterized logic gates, so called “standard-cell logic gates”, are used to design complex VLSI circuits. A Boolean function can be synthesized with a different combination of logic cells, implying a different number of transistors and layout design which directly impact the radiation robustness of the circuit. Once the highly vulnerable nodes are identified in a circuit, hardening approaches as gate sizing or hardware redundancy can be added to improve the overall reliability of the circuit [126, 154]. Recently, a considerable effort can be noticed from the research community in considering radiation hardening techniques early in the design flow of a VLSI circuit [123–125, 155–157]. The proposed predictive SET characterization methodology (discussed in the Section 2.4) can be integrated into the logic synthesis of a cell-based circuit design as proposed in Figure 5.1. From an RTL (Register Transfer Level) description, the logic synthesis is able to translate a function to a netlist description of logic gates using a given Standard-Cell library. Three main processes constitute the logic synthesis of a VLSI circuit [158]: the gate-level optimization independent of technology, i.e. the Boolean equations described in the RTL are optimized to minimize its size and the number of literals; the technology mapping, in which each logic function is transformed into a logic gate (NAND, NOR, AND, OR, etc.) from the given cell library; the gate-level optimization technology dependent, in which optimizations on the gate netlist will be performed to minimize delay in critical paths, power consumption and area usage.

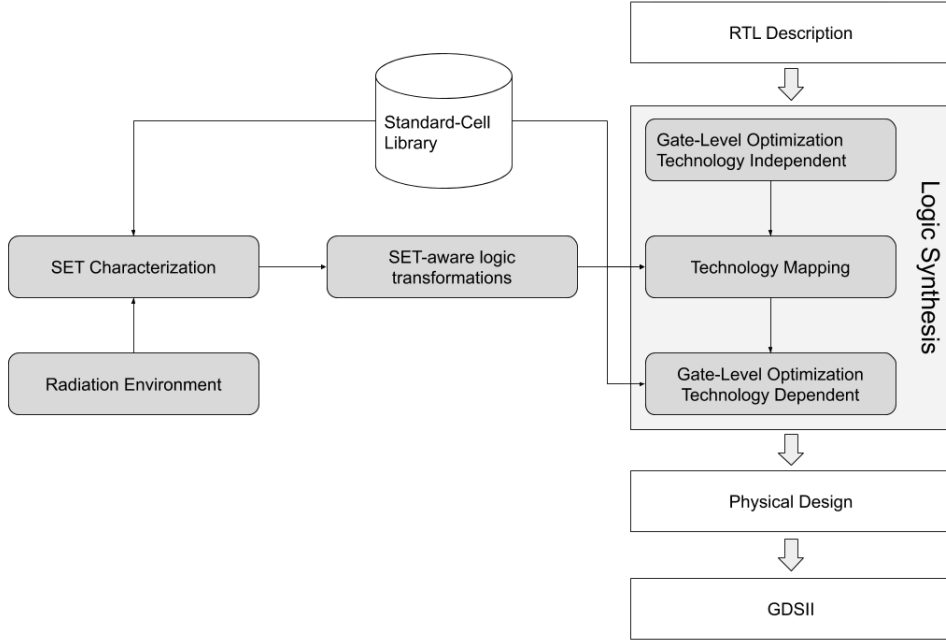


Figure 5.1: Integration of the proposed SET characterization of standard-cell libraries into the logic synthesis.

The gate netlist consists of a logic level representation of the circuit containing gate instances, from the standard-cell library, and its corresponding port connectivity. Thus, the logic synthesis has a major impact on the resulting gate netlist and therefore on the SEE immunity of the final circuit design. In the technology mapping, the technology-independent circuit is decomposed into basic primitive logic cells (INV, NAND or NOR gates). After the decomposition, a pattern matching process is performed to identify structural and functional patterns to be used in the covering process, in which the best patterns will be implemented following a cost function, i.e. delay, area and power consumption. Therefore, by assessing the SET immunity of basic logic cells and combinations of cells, it is possible to develop a reliability-driven cost function and incorporate into the technology mapping.

In the physical design process, the synthesized gate netlist provided by the logic synthesis is converted into the geometric representations of different layers used in the manufacturing process, so called circuit layout. It is also in

this step in which each logic cell layout is placed and its connections routed to minimize wirelength and improve power/performance metrics. However, the work in [126] proposed a cell placement to improve the induced SER of the circuit, instead. The placement algorithm focused on reducing the charge sharing effects. Similarly, by utilizing the SET characterization methodology on a cell library, a set of SET-aware logic transformations can be derived and adopted into the logic synthesis to improve the SET immunity of the final synthesized gate netlist. The SET cross-section of the ten mostly used standard-cell logic gates are shown in Figure 5.2 for two particle LETs. Two different drive strengths were selected for the primitive logic cells: inverter (INV), NAND and NOR gates.

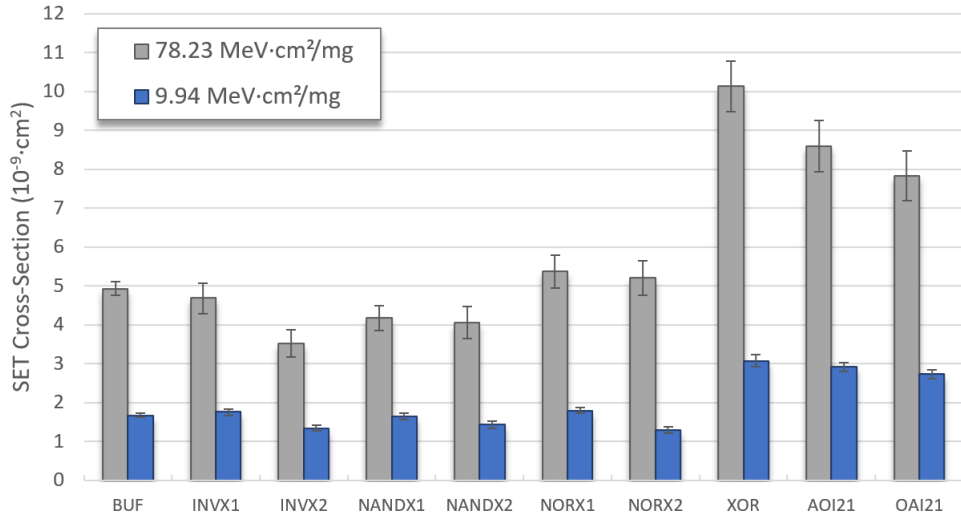


Figure 5.2: SET cross-section for eight standard-cell gates from 45nm Nan-Gate [129], for LET equals to 78.23 and 9.94 $MeV.cm^2/mg$.

As shown in the last chapter, the circuits with higher drive strength (X2) may present lower cross-section than the minimum sizing design. The And-Or-Inverter (AOI) and the Or-And-Inverter (OAI) gates implement a larger logic function, therefore, a larger layout area is used to design the circuits. Consequently, a higher SET cross-section is observed when comparing with the primitive logic cells. Based on this information, an SET-aware technology mapping could be adopted by associating a reliability cost to each logic gate.

The weight or cost of each gate can be calculated based on the radiation requirements of the mission and the SET cross-section or the estimated in-orbit SET rate. Later in this chapter, a figure-of-merit will be proposed as an example for this reliability cost function association for each standard cell, or block of circuits.

5.1.1 Multiple V_{th} cells and Voltage Scaling

One of the primary goals of logic synthesis is to minimize the delay in critical paths. This is achieved by choosing the cells with lower propagation time, and it can be done by adopting multiple threshold voltage V_{th} circuits [159]. Devices with low V_{th} provide a faster switching time and consequently speed up the circuit. However, an increase in the static power consumption is observed due to the increase in leakage currents. On the other hand, the use of high- V_{th} devices reduces the leakage currents in the cost of performance degradation. Accordingly, multiple V_{th} cells are widely used to optimize the gate netlist regarding the delay and power consumption [160]. This multiple- V_{th} assignment can also be addressed using the proposed SET characterization methodology. In Figure 5.3, the standard cells were characterized using a High-Performance (HP) process technology, i.e. low- V_{th} devices, and a Low-Power (LP) process technology, i.e. high- V_{th} devices. On overall, it is noticed an increased cross-section for the circuits based on the LP technology. This behavior is in agreement with the literature, in which it was shown that the increase on the threshold voltage leads to degradation of driving strength capability [161–163]. The NAND gates are the most sensitive to this V_{th} variation with a cross-section increase of 95% and 85% for the NAND_X1 and NAND_X2, respectively. Besides its higher cross-section, the lowest increase was obtained for the complex-logic gates AOI21 and OAI21. Another widely used technique in low-power systems is the adoption of dynamic voltage scaling [164]. However, reducing the supply voltage of the circuits increases the delay and the sensitivity to radiation effects [165, 166].

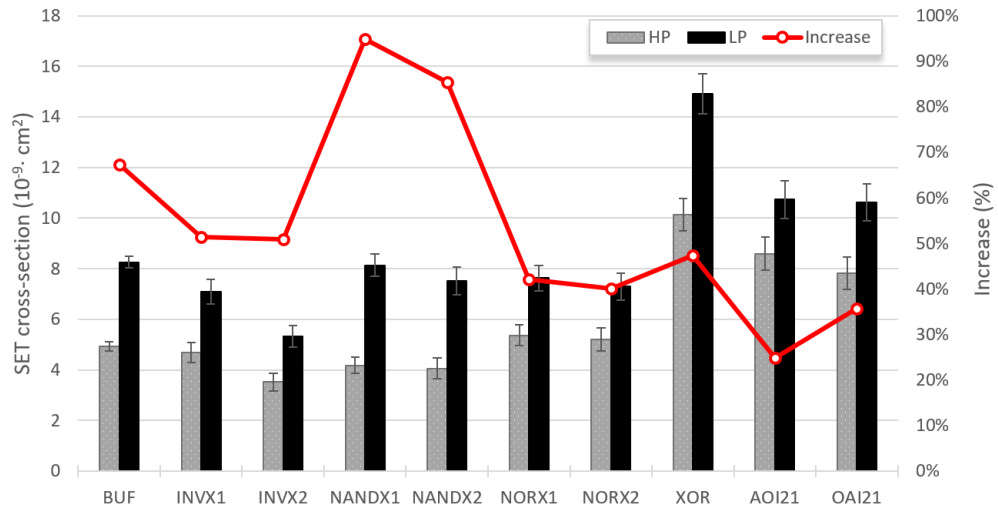


Figure 5.3: Impact of different threshold voltage devices: High-Performance (HP) vs. Low-Power (LP) devices.

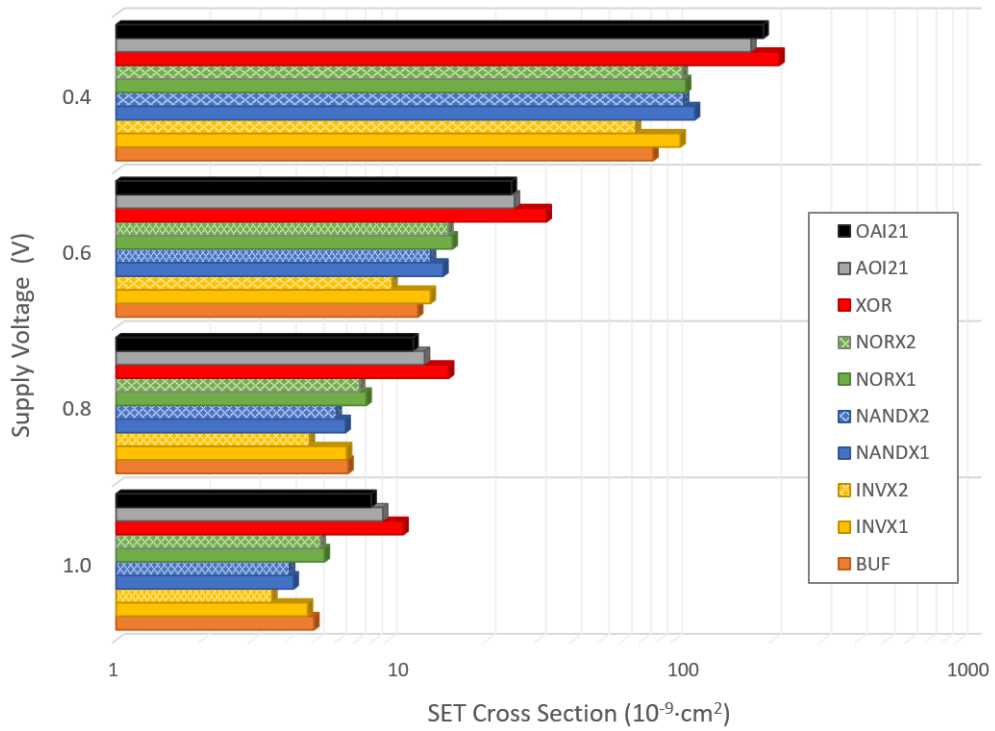


Figure 5.4: Estimation of the dynamic voltage scaling impact on the SET cross section of the standard cells.

In Figure 5.4, the SET cross-section of each gate is estimated considering the supply voltage scaling from 1 V down to 0.4 V (near-threshold regime). Reducing the supply voltage directly reduces the critical charge necessary to observed a SEE in the circuit output [165]. In nominal supply voltage scenario, the NAND gates are preferable than NOR gates as it provides lower SET cross-section. However, when considering a supply voltage scaling to 0.4 V, the NOR gates have shown a lower cross-section instead. This difference is attributed to the different drive capability impact on the transistor networks present on each gate design. Accordingly, in a system design focused on low-power design using dynamic supply voltage, logic synthesis should consider a higher usage of NOR gates instead of NAND gates.

5.1.2 Technology Mapping

Reliability-aware logic synthesis, accounting for single-event effects mitigation, consists in hardening a complex circuit by selectively using logic gates that minimize the SET generation or propagation in the most vulnerable sub-circuits of a complex VLSI design [123]. For instance, the radiation robustness of the circuit can be enhanced by choosing the best combination of standard cells that promotes the pulse quenching effect (PQE) induced by the inter-cell charge sharing in electrically related combinational circuits [151, 59]. As mentioned previously, the technology mapping is responsible for the translation of Boolean logic functions described in RTL codes to actual physical logic gates available in a cell library.

Consider the buffer gate, widely used in VLSI circuit design as a circuit amplifier, shown in Figure 5.5. In contrast to the inverter gate, a digital buffer produces an output signal of the same logic state than its input signal. Buffer insertion (also known as Repeater Insertion) is a well-known technique used in VLSI systems to optimize the circuit performance in sub-micron technology [167]. Further, with the technology scaling, the buffer insertion is increasing in importance due to the increase in the wire delays [168]. Thus, it is of utmost important to evaluate the radiation robustness of the buffer gates provided by cell libraries. From the RTL description of a

circuit, the implementation of the buffer Boolean function can be synthesized into one single buffer (BUF) gate, usually provided in the cell library, or two interconnected inverter (INV) gates. Although, the same logic function is implemented, different radiation sensitivity should be expected due to their different layout implementations provided by the standard cell design and, also, the cell placement obtained in the physical synthesis. The same difference can be expected when implementing the logic function OR and AND. To analyze which combination of gates provides the best SET robustness, the BUF, AND, and OR gates were evaluated under heavy ions and compared with INV, NAND, and NOR gate coupled with an inverter in their output.

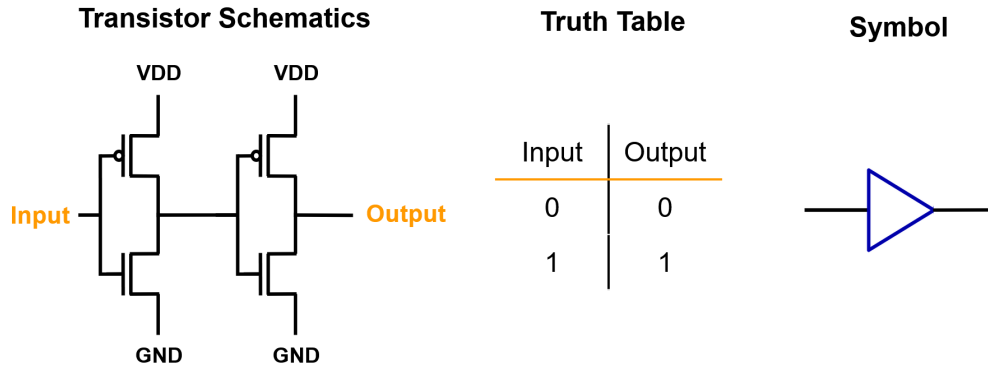


Figure 5.5: Transistor schematics, truth table and symbol of a digital CMOS buffer gate.

As shown in Figure 5.6, three cell placements for the combination of gates are evaluated to analyze the charge sharing effectiveness and its consequent pulse quenching effect. Only horizontal placements are considered in this study. It was previously shown that vertical placement, i.e. electrically connected cells placed in different cell rows, eliminates the pulse quenching effect due to the increased nodal separation and the presence of the well contacts which considerably reduces the charge sharing efficiency [169]. The cell layout of each standard cell is shown in Figure 5.7 and all cells are the minimum sized design provided by the cell library in the bulk 45nm technology, i.e. drive strength 1 (X1) cells.

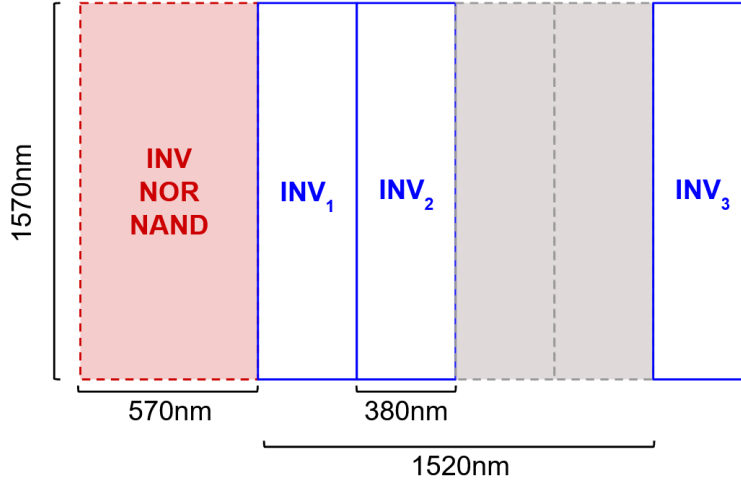


Figure 5.6: Cell placement setup used for the MC-Oracle simulations.

The SET cross-section σ_{SET} curves for the buffer and inverters are shown in Figure 5.8. Clearly, the BUF design provides a lower overall SET cross-section. In the BUF design, the two sensitive nodes are placed closer than in the INV+INV situation. In this way, a higher charge sharing effect is observed and due to the electrical relationship of these nodes (inverting stage), pulse quenching effect (PQE) takes place and reduces the overall SEE sensitivity. And, more importantly, by analyzing the layout design of the buffer gate, we can observe that the first stage inverter has a smaller transistor sizing than the second stage inverter. This can be seen in Figure 5.9. By reducing the transistor sizing of the first stage, in 50%, the SET pulse propagated to the second stage was shown to be shorter than the one propagated in the INV+INV design. Additionally, the drain collection area in the second inverter is kept the same in both designs. Thus, in the buffer gate, a shorter transient pulse is induced in the first inverter stage while keeping the same PQE effectiveness from the second stage inverter, explaining its higher robustness. The bigger difference between the designs are observed for high LET particles due to the stronger PQE impact. The BUF gate shows about 40% decrease in the σ_{SET} for a particle LET of $78.23 \text{ MeV.cm}^2/\text{mg}$. At low LET, a reduction of charge sharing between the collecting nodes is observed, leading to small difference on the SET cross-section between the designs.

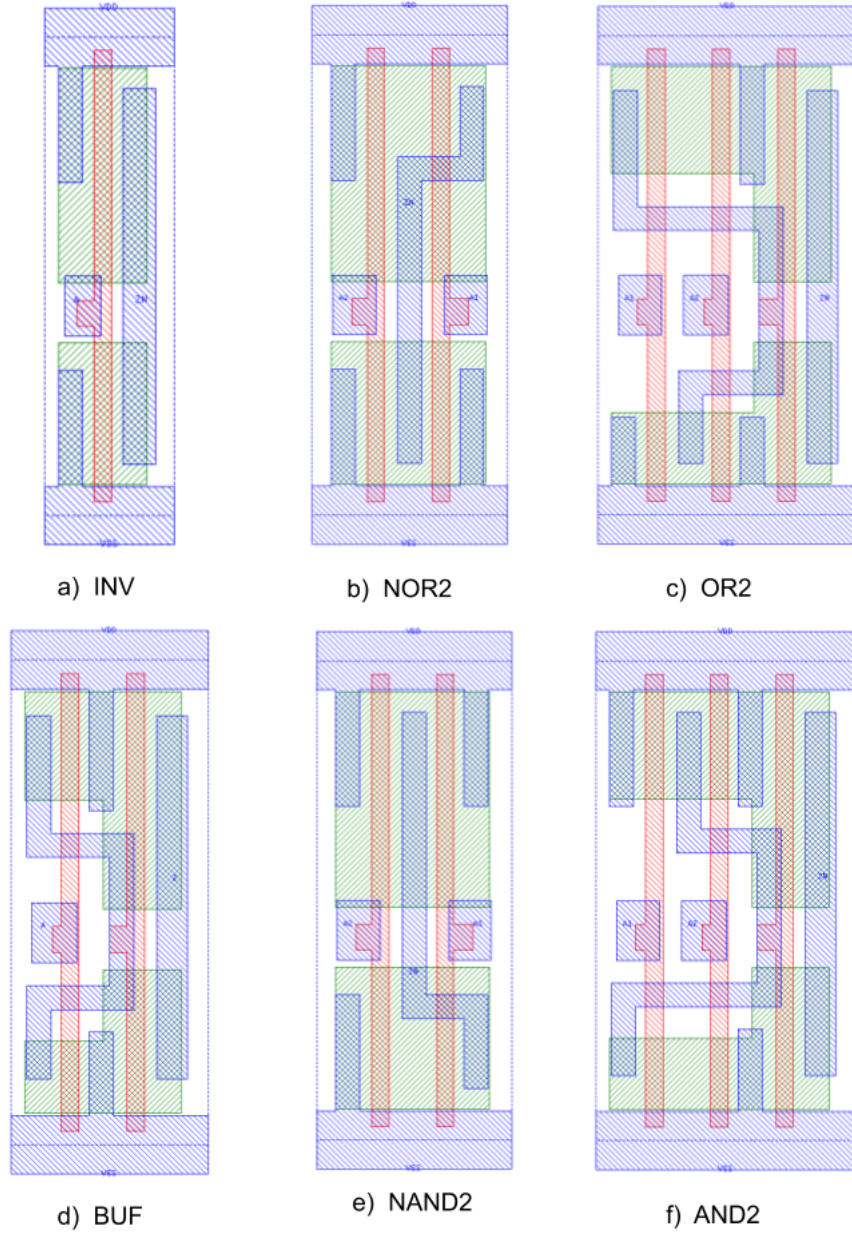


Figure 5.7: Layout design of a) INV, b) NOR2, c) OR2, d) BUF, e) NAND2 and f) AND2 in the 45 nm Open Cell Library [129]. For clarity, only the layers metal1 (blue), active diffusion (green) and poly layers (red) are shown.

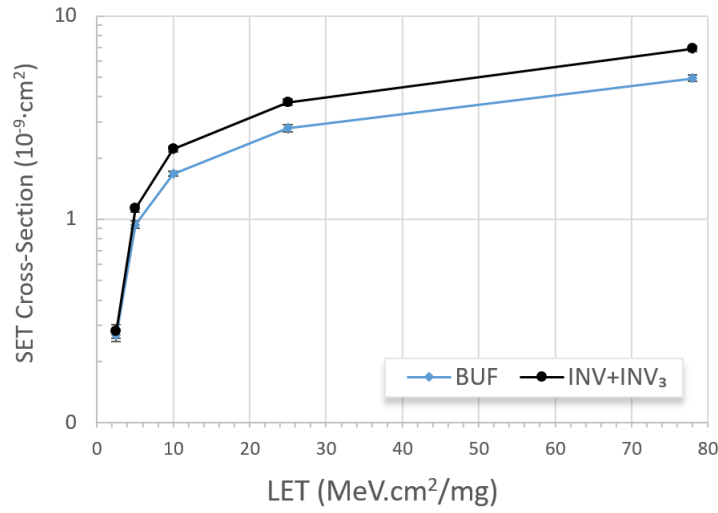


Figure 5.8: SET cross-section curve for the BUF gate and the INV+INV circuit.

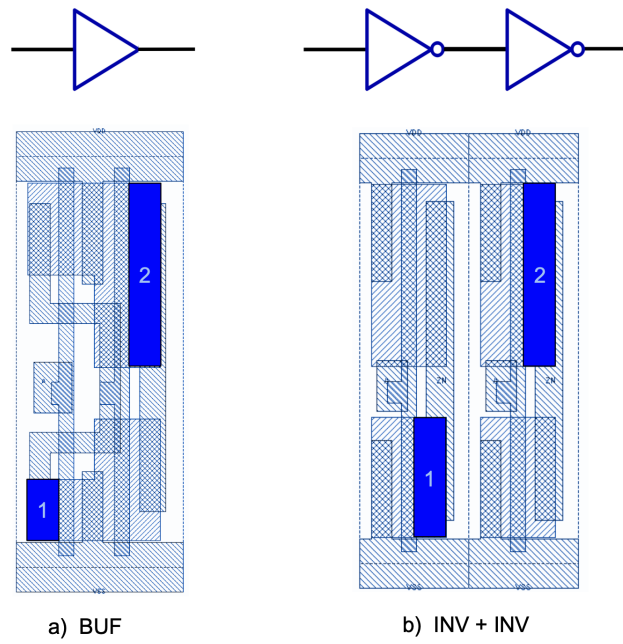


Figure 5.9: Comparison of the collecting drain area of the sensitive electrodes in the first and second stage inverters from the BUF gate and INV+INV design.

While for the best implementation of the buffer boolean function has been shown to be the BUF gate provided by the cell library, for the OR

Boolean function, the NOR+INV circuit might provide lower SET cross-section. For both OR gate and NOR+INV circuit, the input (1, 1) constitutes the worst-case scenario for the pulse quenching effect [59]. As shown in Table 5.1, the NOR+INV circuit provides lower σ_{SET} than the OR gate even with the increased distance between the NOR and INV cells. Although, the transistor sizing is reduced in the internal NOR circuit within the OR gate layout, the reduction of the restoring current and nodal capacitance overcome the benefits of the reduced drain collecting area. Unlike the inverter gate, the NOR and NAND gates present transistors in series, which degrades the recovering current of the circuit. Besides the SET cross-section, Table 5.1 also provides the layout area for the OR and AND logic implementations. Due to the regularity of layout design in a standard cell library, both logic functions present the same layout area for each implementation. As the input (1, 1) is the worst-case scenario for the reliability of the NAND gate, the NAND+INV circuits have not shown a lower σ_{SET} as observed for the NOR+INV circuits. Additionally, when the input vector is (1, 1), the NMOS device from the output inverter of the NAND gate is dominating the pulse quenching effect, different from the case of the NOR+INV schemes in which it is the PMOS device. The NMOS drain area in the inverter is approximately 35% smaller than its PMOS drain area, thus a reduction in the pulse quenching effect is expected as it directly reduces the positive effect of charge collection. Furthermore, as the output inverter is placed further from the first gate, the σ_{SET} increases in response to the reduction of pulse quenching effect.

Table 5.1: Total area for the cell layout design for the OR and AND logic implementations and the SET cross-section for a $LET = 78.23 \text{ MeV.cm}^2/\text{mg}$ and input (1, 1)

	OR logic function			AND logic function	
	Layout area (μm^2)	XS (10^{-9}cm^2)		Layout area (μm^2)	XS (10^{-9}cm^2)
OR gate	1.193	8.268	AND gate	1.193	6.984
NOR+INV ₁	1.476	4.056	NAND+INV ₁	1.476	7.098
NOR+INV ₂	1.476	4.134	NAND+INV ₂	1.476	7.254
NOR+INV ₃	1.476	4.290	NAND+INV ₃	1.476	7.332

Besides the basic primitive logic gates (INV, NAND, NOR...), standard-cell libraries also provide the so-called complex-logic gates. The usage of such standard cells, as the And-Or-Inverter (AOI) and Or-And-Inverter (OAI) cells, reduces the number of transistors in the circuit leading to denser layouts, reduced power consumption and area [170]. For example, the Boolean logic function given in Equation 5.1 can be implemented by using basic logic standard cells as the NOR and AND gates or by using the complex-gate AOI directly as illustrated in Figure 5.10.

$$Y = \neg(A1 \wedge (B1 \vee B2)) \quad (5.1)$$

For the logic synthesis of Equation 5.1, the AOI21 implementation provides 40% of reduction in the transistor count compared with the implementation using an AND gate coupled with a NOR gate. The same result can be obtained for the compliment of the Equation 5.1 when the OAI21 gate is used. Clearly, the power consumption for the complex-logic gates are also reduced, but the sensitivity to radiation is not straightforward to be predicted in advance. In [171], an optimizing synthesis methodology is proposed to reduce the transistor count of circuits. The proposed methodology is called Gate Clustering and consists in the agglutination of basic logic gates into static CMOS complex gates (SCCG) [171]. As expected, the authors confirm that the reduced number of transistor improves the power consumption and layout area. Further, the circuit performance is also improved due to the reduction of the circuit wirelength which is the main source of delay at advanced technology nodes [172, 173]. The complex logic gates AOI21 and OAI21 are compared with the radiation performance of its correspondent implementation based only on basic logic gates such as AND, OR, NAND and NOR. The simplified cell layout design of the complex gates are provided in Figure 5.11, which only the metal1, active diffusion and poly layers are shown for clarity.

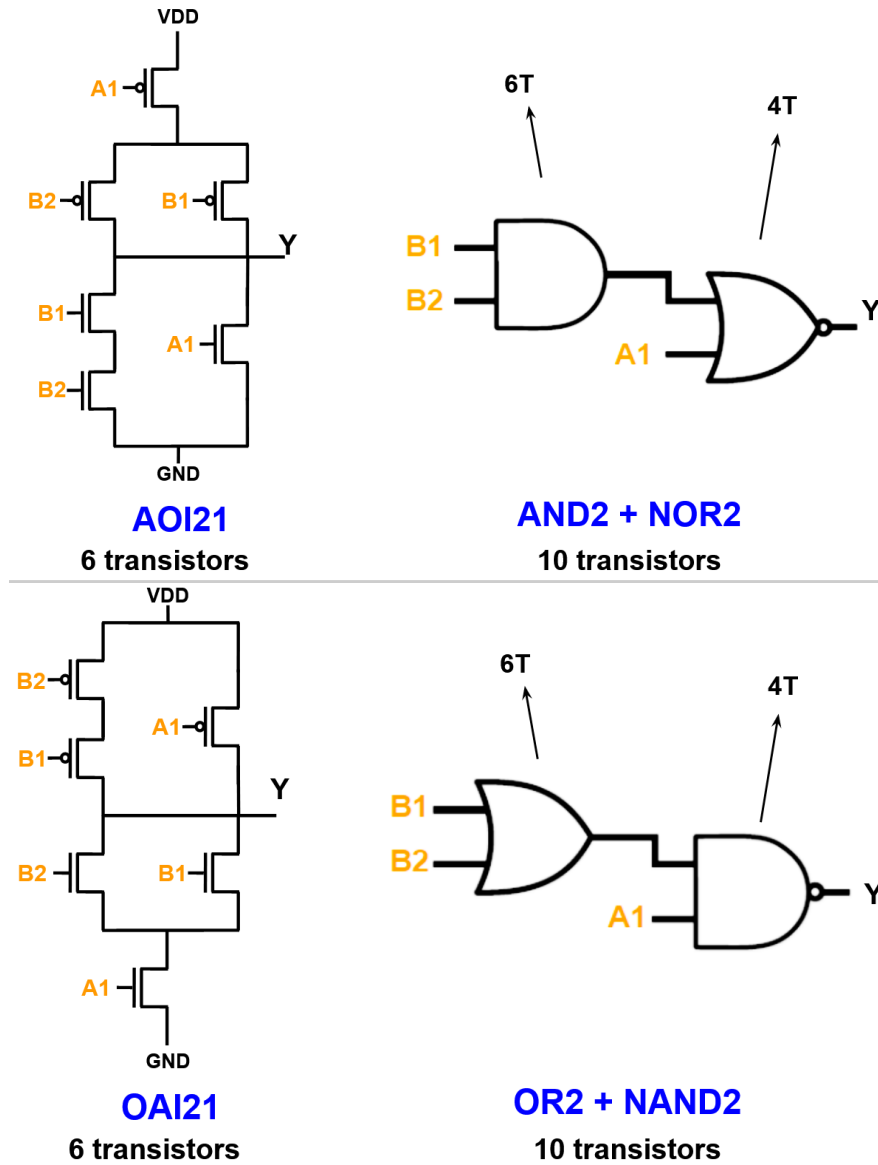


Figure 5.10: MOS transistor network of the complex logic gates AOI21 and OAI21 and its correspondent implementation with the gates: AND2, NOR2, OR2, and NAND2.

Considering the gate sizing, it is adopted the minimum cell strength available in the library for all analyzed logic cells. Therefore, the suffix X1 is suppressed in the text. The cell height is defined to $1.57\mu m$ [129] and for the implementation of the AND+NOR and OR+NAND circuits, the standard

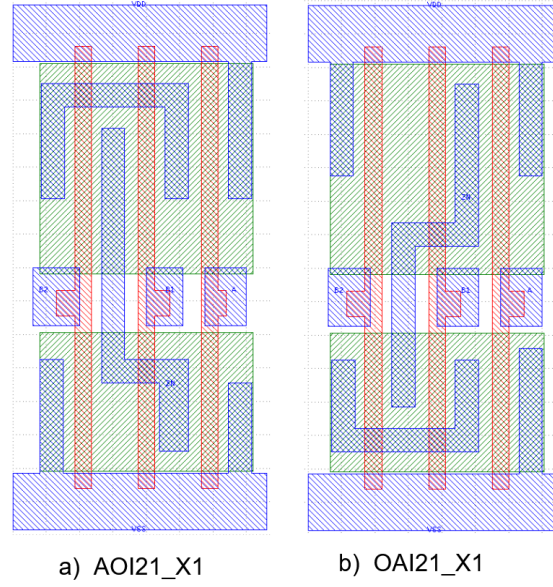


Figure 5.11: Cell layout of the complex gates: (a) AOI21 and (b) OAI21. For clarity, only the layers metal1 (blue), active diffusion (green) and poly layers (red) are shown.

cells were placed within the minimum distance. For their individual cell layout, please refer to Figure 5.7.

The complex-gate AOI21

To understand the individual behavior of the p-type and n-type devices in this study, the simulations were divided into two groups: the P-hit simulations, for which all the PMOS devices are turned *off*, i.e. input vector set to (1, 1, 1); and the N-hit simulations, for which all the NMOS devices are turned *off*, i.e. input vector set to (0, 0, 0). For instance, in the P-hit simulations, exclusively all the P-type transistors are sensitive to SET, i.e. all observed transient pulse is generated from a particle hit over the drain region of a PMOS transistor. The information of the P-hit and N-hit sensitive area can be found in Table 5.2 along with the value of the layout area and total sensitive collection area of each logic gate. The collection area refers to the area of the drain p-n junctions extracted from the layout circuit design and imported to the MC-Oracle tool for the particle simulations. Notice that the

complex-gate AOI21 provides a reduction of approximately 42% in the total layout area. However, it provides solely 14% reduction of the total sensitive area which is responsible for the charge collection during a particle interaction within the silicon. The AND+NOR implementation has the largest collection drain area while the AND gate presents the smallest one.

Table 5.2: Total area for each cell layout design, total sensitive region and P-hit and N-hit sensitive area (μm^2)

	Layout Area	Collecting Area		
		P-hit	N-hit	Total
NOR2	0.895	0.154	0.058	0.212
AND2	1.193	0.110	0.095	0.205
AOI21	1.193	0.243	0.116	0.359
AND+NOR	2.088	0.265	0.153	0.418

The SET cross-section curves considering only P-hit interactions is shown in Figure 5.12. It clearly shows that the implementation containing the basic logic cells AND+NOR provides a lower SET cross-section than the AOI21 for the entire LET range. Both circuits present the same threshold LET whereas there is a SET cross-section difference of approximately a factor of 2. The charge sharing effect and more importantly the logical masking between the AND gate and NOR gate are responsible for this reduced number of observed SET in the output of the AND+NOR implementation [174].

Any SET induced at the AND gate will be filtered by the logic of the NOR gate as observed in the truth table shown in Figure 5.13. The output of the NOR gate will remain at logic zero as long as the secondary input remains at logic one. As it will be shown further in the results, this masking effect is not observed for the N-hit configuration. By analyzing the P-hit sensitive area of the two implementations presented in Table 5.2, both the AND+NOR and AOI21 gate present approximately the same sensitive area, a difference of only 2%. However, by analyzing the structure of the combinational logic and the electrical simulation results, the SETs observed for the AND gate are logically masked by the NOR gate, thus reducing the overall drain sensitive area to the PMOS devices issued in the NOR gate [174].

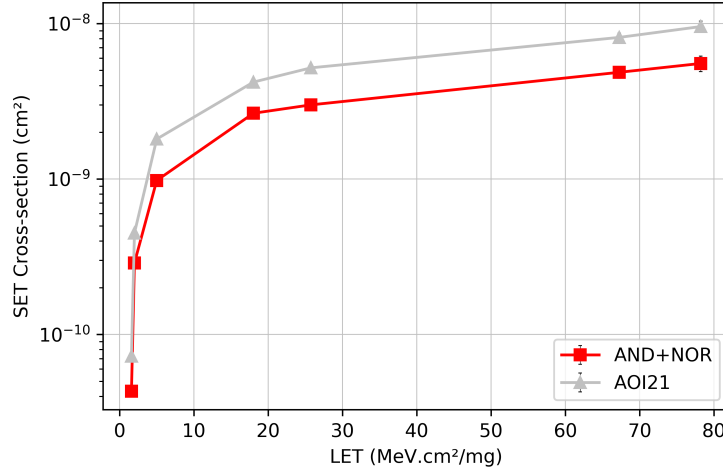


Figure 5.12: SET cross-section curve of P-hit interactions for the complex logic AOI21 gate and AND + NOR implementation.

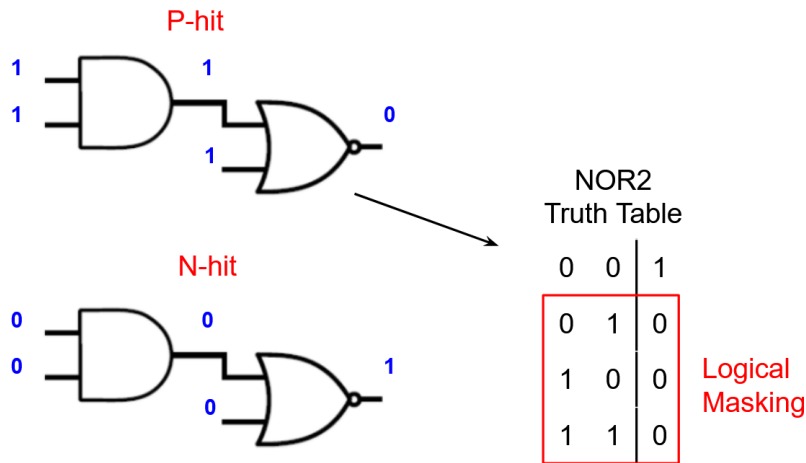


Figure 5.13: Logical masking effect for the P-hit configuration in the combinational logic circuit AND+NOR. There is no logical masking when both inputs are set to logic zero.

The Figure 5.14 presents the comparison between the SET cross-section of the AND+NOR implementation and the standalone NOR gate. It can be observed that the logical masking is effective by reducing the sensitivity of the circuit close to the sensitivity of the standalone NOR gate.

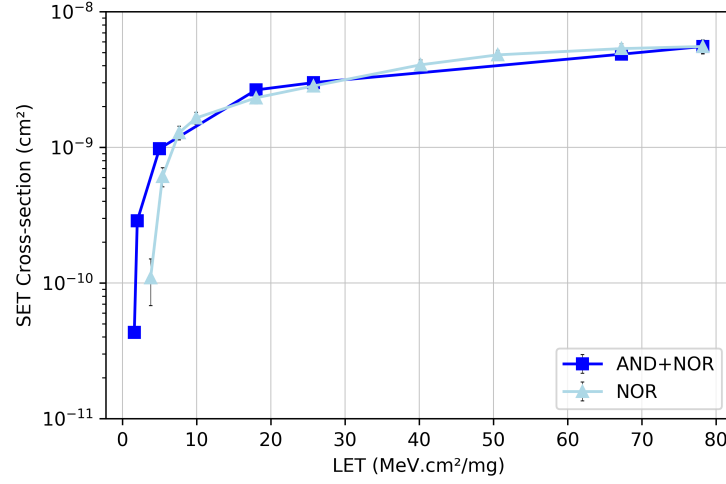


Figure 5.14: Comparison of SET cross-section curve of the AND+NOR implementation and the standalone NOR gate.

Considering only the N-hit interactions, the SET cross-sections are approximately the same for high LET ions as illustrated in the Figure 5.15. Table 5.2 indicates that both circuits present very similar N-hit sensitive area. Further, there is no contribution of logical masking effect for the input signals considered. As shown in the truth table of the NOR gate in Figure 5.13, its output is determined whenever one of its input is at logic one. Then, as originally both inputs are set to logic zero, whenever a generated SET at the AND gate propagates to the NOR gate, it will be able to propagate to its output in case of not being electrically attenuated. In this case, only the electrical masking effect takes place.

For ion LET lower than $5 \text{ MeV.cm}^2/\text{mg}$, the difference between the analyzed circuits becomes more evident as the electrical masking effect is able to filter the short transient pulses. For instance, the complex-logic AOI21 gate has approximately 24% of reduced N-hit sensitive area and it reaches about 57.3% and 83.7% reduction on the SET cross-section for $\text{LET} = 2.52 \text{ MeV.cm}^2/\text{mg}$ and $\text{LET} = 1.69 \text{ MeV.cm}^2/\text{mg}$, respectively. Moreover, the different circuit topologies provide different transistor networks with different restoring current [175, 45]. The pull-up transistor network of AOI21 gate presents two parallel PMOS transistors. Accordingly, a higher restor-

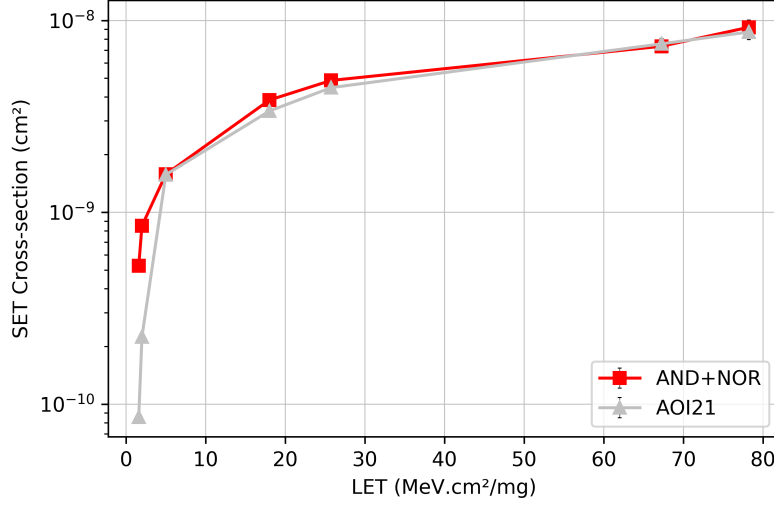


Figure 5.15: SET cross-section curve of N-hit interactions for the complex logic AOI21 agate and AND + NOR implementation.

ing current is observed in the complex-logic gate improving the radiation performance at low LET by electrically attenuating the SET pulse.

The complex-gate OAI21

Similarly, the results for the complex-gate OAI21 is divided into P-hit simulations and N-hit simulations regarding the input signal of the circuits. Table 5.3 contains the layout area, total drain collection area and the P-hit/N-hit sensitive collection areas. Due to the regularity of the Standard-Cell designs, the OAI21 provides the same reduction in layout area provided by the AOI21 implementation, approximately 43% over the OR+NAND total layout area. Despite the considerable layout area reduction, only a reduction of 17.2% in the total collection area is obtained with the complex-logic layout. The OR+NAND circuit presents the largest layout area and collection drain area while the NAND gate has the smallest areas. The SET cross-section curves for P-hit interactions is shown in Figure 5.16 for the complex-gate OAI21 and OR+NAND circuits. Both implementations presented very similar cross-section results due to the absence of the logical masking effect for the

Table 5.3: Total area for each cell layout design, total sensitive region and P-hit and N-hit sensitive area (μm^2)

	Layout Area	Collecting Area		
		P-hit	N-hit	Total
NAND2	0.895	0.088	0.102	0.190
OR2	1.193	0.143	0.073	0.216
OAI21	1.193	0.176	0.160	0.336
OR+NAND	2.088	0.232	0.175	0.406

OR+NAND under the P-hit configuration. Besides the similar SET cross-section for high LET and same threshold LET, the OR+NAND circuit shows a higher cross-section at $LET = 1.6 \text{ MeV.cm}^2/mg$, approximately a factor of 2. Similarly to what observed for the AOI21 study case, the increased difference in cross-section at low LET can be explained by the restoring current effect [174]. Due to the two parallel NMOS transistors in the pull-down network of the complex-gate, a higher restoring current counteracts against the radiation disturbance by shortening the transient pulses and reducing the SET cross-section compared to the estimated for the OR+NAND circuit.

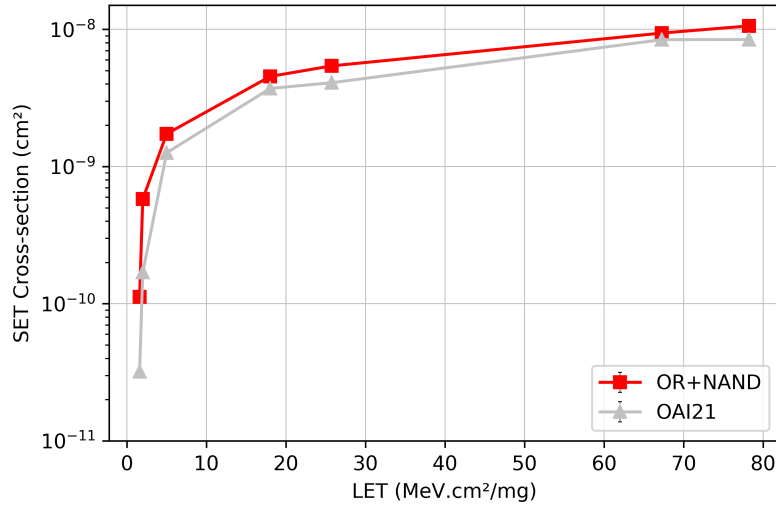


Figure 5.16: SET cross-sectional curve of P-hit interactions for the complex logic OAI21 gate and OR + NAND implementation.

Considering the N-hit simulations, the SET cross-section curves can be observed in Figure 5.17. The complex-gate OAI21 presents the highest cross-section for the complete LET range with the greatest difference under high LET. In agreement to the observed for the complex-gate AOI21, the logical masking effect is also omitted from the complex-gate OAI21 which increases the SET cross-section compared to the OR+NAND structure. Even though the latter circuit structure contains a larger N-hit collection area, as shown in Table 2, due to the logical masking the effective collection area of the circuit reduces to the N-hit sensitive area of the NAND gate. Figure 5.18 contains the gate-level schematic of OR+NAND circuit and the truth table for the NAND gate. The logical masking occurs at the NAND gate for N-hit configuration as long as one of its input signal is at logic zero. To confirm this observation, the cross-section for the OR+NAND and NAND gate are shown in Figure 5.19 considering only the N-hit interactions. Clearly, the logical masking effect is able to reduce the sensitivity of the circuit to the sensitivity of the NAND gate when the N-hit configuration is analyzed [174].

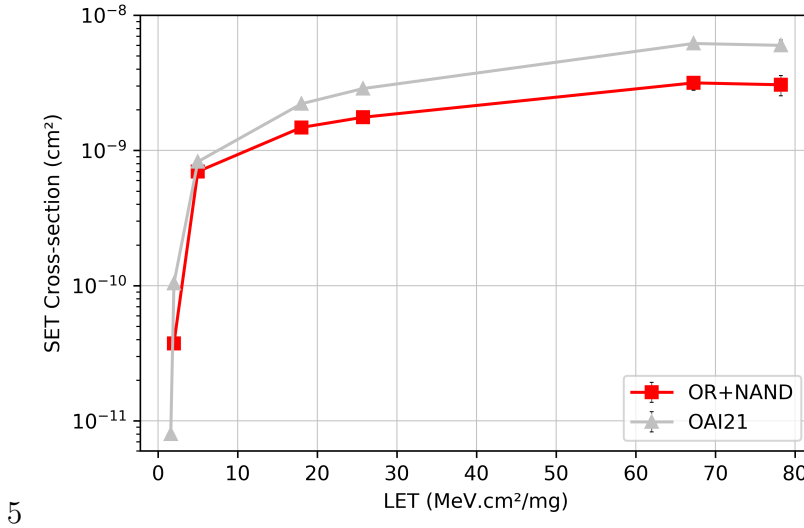


Figure 5.17: SET cross-sectional curve of N-hit interactions for the complex logic OAI21 agate and OR + NAND implementation.

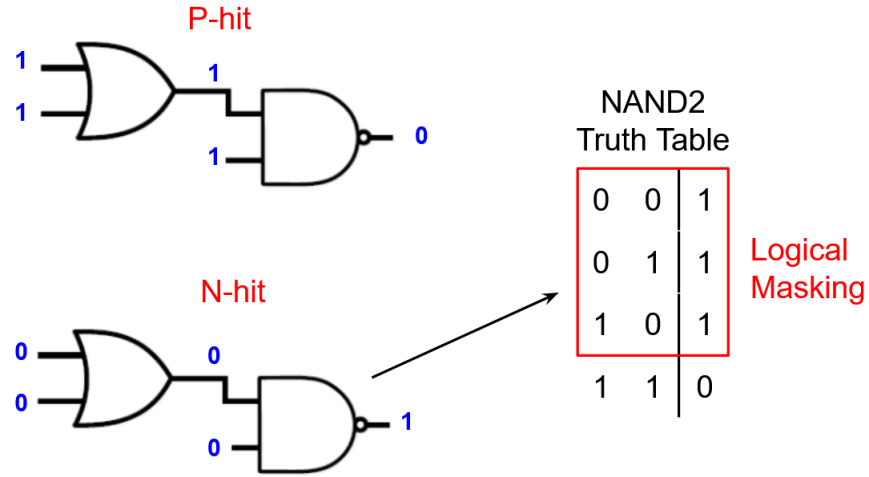


Figure 5.18: Logical masking effect for the N-hit configuration in the combinational logic circuit OR + NAND. There is no logical masking when both inputs are set to logic one.

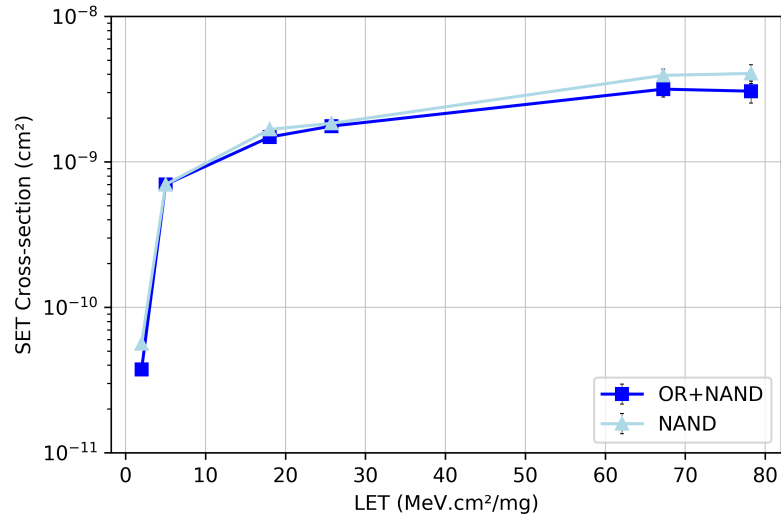


Figure 5.19: Comparison of SET cross-sectional curve of the OR + NAND implementation and the standalone NAND gate.

LET dependence

The radiation-induced cross-section can be represented in logarithmic scales as proposed in [176]. As shown in Figure 5.20 and Figure 5.21, the cross-section curve follows a power law function of the particle LET. It occurs due to the collection efficiency that depends continuously on the distance between the collection zone and the location of the deposited charge. This behavior was verified and it is in agreement with experimental data of testing campaigns in [176]. In Figure 5.20 the SET cross-section curves for the AOI21 and AND+NOR circuits are represented in logarithmic scales. Clearly, it is possible to observe the power law shape of the cross-section in function of the particle LET. However, considering the LET under $2 \text{ MeV.cm}^2/\text{mg}$ for the AOI21 and $5 \text{ MeV.cm}^2/\text{mg}$ for the AND+NOR, the cross-section curves show an abrupt decrease and fall out of the power law shape. It implies that multiple collection zones dominate the failure mechanism in different ways and the cross-section no longer follows the power law dependence [59, 176].

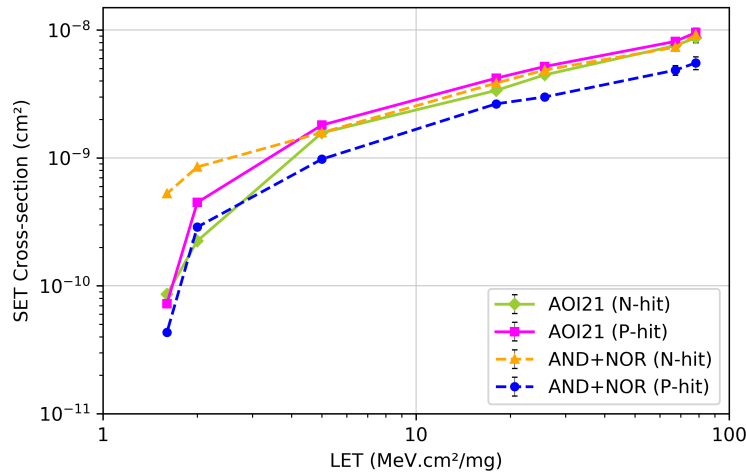


Figure 5.20: Log-log representation of SET cross-sectional curves for AOI21 and AND + NOR considering N-hit interactions and P-hit interactions.

The same points are found for the OAI21 and OR+NAND circuits in Figure 5.21. In contrast to the curves in Figure 5.20, the cross-section curves in Figure 5.21 are far more separated when comparing the N-hit interactions

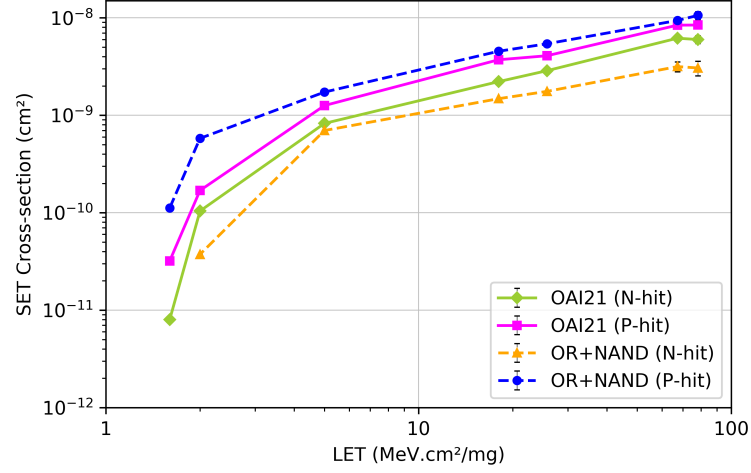


Figure 5.21: Log-log representation of SET cross-sectional curves for OAI21 and OR + NAND considering N-hit interactions and P-hit interactions.

and P-hit interactions, mainly for the OR+NAND circuit. It shows that the logic masking effect has a greater impact on the OR+NAND circuit than the AND+NOR circuit. For the complete range of LET, both SET cross-section curves for the OAI21 remained in between the cross-section curves of the OR+NAND circuit. Considering the results from the Figure 5.21, a logic synthesis optimization should prioritize the implementation using the OAI21 gate for when the P-hit interactions are the major concern while the OR+NAND circuit should be adopted for the N-hit interactions, instead. Based on these findings, the next section presents a new methodology of SET characterization based on the signal probability is proposed and discussed in detail in the next section. Additionally, a reliability-driven pin assignment is also proposed to improve the radiation hardness of standard cells.

5.2 Pin Assignment

The SET characterization of logic gates presents an input dependence due to the different interplay relation of sensitive collecting drain areas and restoring current as verified previously in this thesis. The signal switching

activity has been used to estimate power consumption in the design process of VLSI circuits for years, but it can also be used to support reliability analysis as shown in [177–179]. Until now, the SET cross-section calculation in this thesis has considered the arithmetic mean between the cross-section obtained for each input signal combination separately, i.e. the same probability to each input combination is considered. However, the proposed predictive SET characterization (Figure 2.15) can also consider the signal probability information of a given system application in order to estimate a more realistic cross-section. Moreover, by considering signal probabilities, it is possible to propose more application-efficient mitigation transformations in the circuit synthesis (Figure 5.1).

Signal switching activity in VLSI systems are widely used to estimate power consumption, and to perform timing analysis [180–182]. Considering the sensitivity to SET is directly related to the layout of the circuit and its operation mode, i.e. input signals and internal states, signal probability can also be used to improve the reliability of circuits [66]. For instance, Signal Probability based Reliability Analysis (SPRA) is an efficient tool used to analyze the reliability of VLSI circuit at gate-level [183, 184, 178]. In this context, the reliability of a gate or a circuit is defined as the confidence level that the output will be functionally correct given a fault probability. Initially, SPRA methods have been focused on physical defects due to wearout mechanisms or process variability [183]. However, due to the increase interest in reducing the impact of soft error rate, some works analyzing SET have been proposed as in [184, 178, 156, 125]. Using a SPRA algorithm, the work in [156] proposed a cell placement strategy based on the definition of bad and good pairs of logic gates referring to a measurement on how the close proximity of the standard cells would impact the circuit error rate. Similarly, [125] proposed another cell placement approach based on the signal probability and its relation to the pulse quenching effect.

In this thesis, signal probability is used to propose a reliability-driven pin assignment optimization based on the input dependence of SET sensitivity of logic gates. Based on the SET characterization of the standard cells, pin swapping, also known as rewiring, is adopted to assign the lowest signal

probability to the input pin so that the most sensitive gate input combination obtains the lowest probability of occurrence. Besides the cross-section reduction, the optimization results provide the impact on the soft error rate for single cells individually, i.e. 2-input basic logic gates and 3-input complex gates.

5.2.1 Optimization of Pin Assignment for Single-Event Transients

Pin assignment is used in the logic synthesis to improve power and performance metrics in the design of VLSI circuits by taking advantage of the functional equivalence of input pins of logic gates [158, 185, 186]. Consider the NAND gate and its truth table in Figure 5.22. A symmetric input relationship is observed when both input signal are not identical, i.e. $A \neq B$: the output signal is determined whenever one of its input is in low logic level, regardless of the input pin (a or b). The interchangeable input combinations are highlighted in Figure 5.22 (red rectangular). This symmetric input relationship is observed in all 2-input basic standard cell gates.

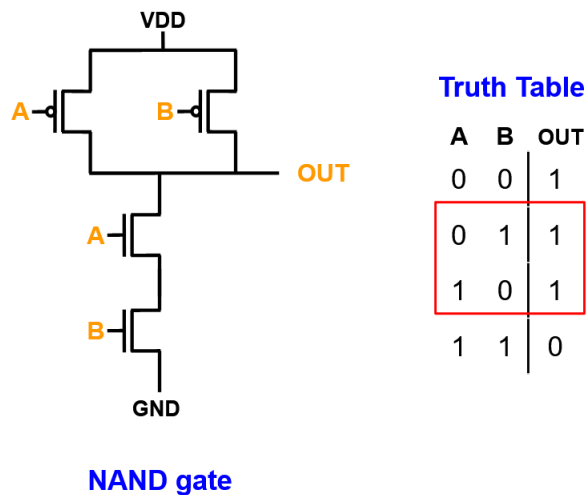


Figure 5.22: Transistor network and truth table of a 2-input NAND gate. The interchangeable input combinations are highlighted by the red rectangular.

As each input pin of a logic gate presents different electrical characteristics depending on the transistor network, power-driven logic synthesis assigns the input signal with lower switching activity to the pin with higher capacitance. Similarly, a timing-driven optimization can apply pin permutation between symmetric input pins such that the late-arriving signal is always connected to the input pin with the lowest intrinsic delay [158]. This process is known as rewiring or pin swapping [185, 186]. Considering that cross-section of logic gates is dependent on the input stimuli, a reliability-aware synthesis can be proposed based on the cell symmetric inputs and signal probabilities to improve the vulnerability of the circuit through optimal pin assignment.

A diagram illustrating the proposed SET-aware pin assignment optimization in a cell-based circuit design flow is shown in Figure 5.23. Given a circuit description in Register Transfer Level (RTL), the logic synthesis optimizes each Boolean function and maps it to logic gates available in the Standard-Cell library. As output, a gate netlist is provided, normally optimized for timing, area and/or power. With the gate netlist information and the Standard-Cell library, the SET-aware pin assignment optimization can be performed. The first step is the Input-based SET characterization, in which the symmetric input relationship of each standard cell is identified and the SET cross-section for the interchangeable input combinations calculated. For instance, the cross-section for the input combination (0, 1) and (1, 0). The methodology used to calculate the SET cross-section and in-orbit rate is explained in the next section. Based on the SET characterization results, a set of pin assignment rules is defined, i.e. there will be an input pin for each standard cell in which the net with the lowest signal probability should be connected to so the most sensitive interchangeable input combination obtains the lowest probability of occurrence. The second step, considering the switching activity of the primary inputs, the signal probability calculation can be performed for the internal net connections as illustrated in Figure 5.24. Based on the Boolean function of each gate, an equation is extracted to calculate the probability of the output signal to be at logic value 1, i.e. the gate output signal probability $P_{GATE}(output = 1)$. In this work, the Parker-McCluskey method [187] was used considering the primary inputs as

uncorrelated and with equally switching activity of 50%, i.e. signal probability equals to 0.5. Although temporal and spatial correlation is not considered in our analysis, a more complex and accurate signal probability estimation method can be easily integrated into the development flow in Figure 5.23. Applying basic probability theory, the output signal probability equations for the logic gates used in the combinational circuit in Figure 5.24 are shown in Table 5.4.

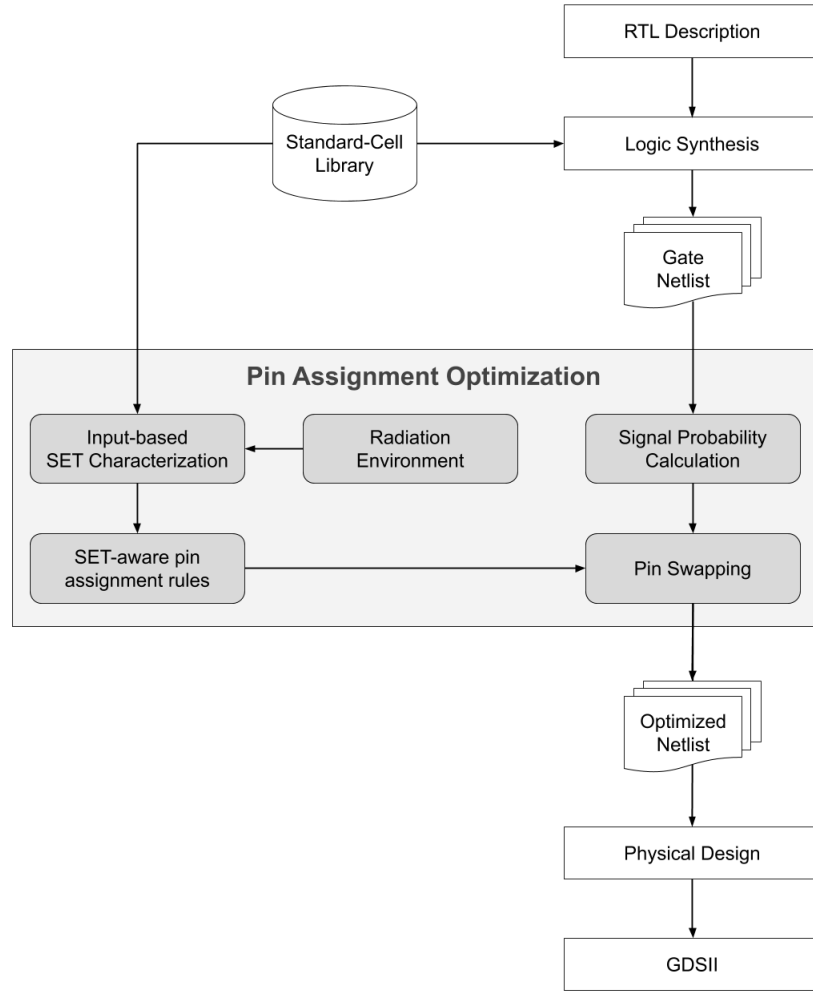


Figure 5.23: SET-aware Pin Assignment Optimization in a cell-based VLSI circuit design flow.

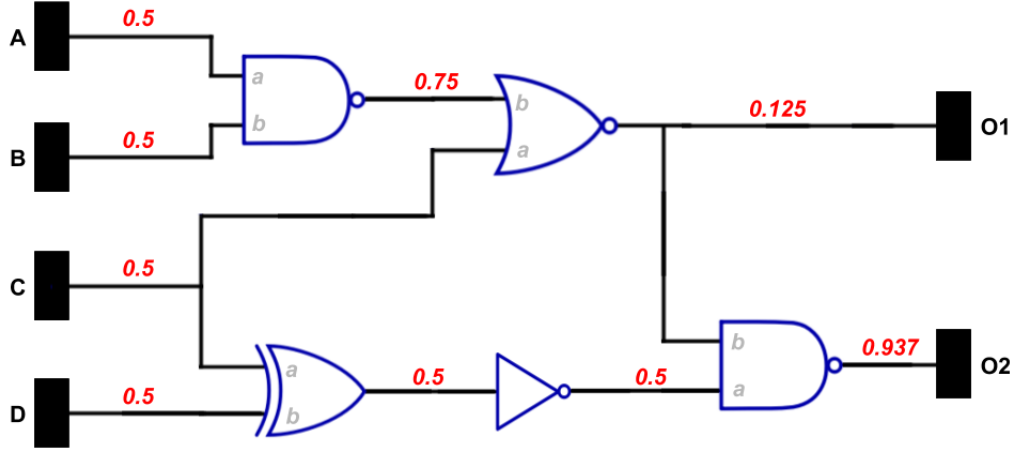


Figure 5.24: Signal probability estimation for a combinational logic circuit.

Table 5.4: Signal Probability Estimation for the INV, NAND, NOR and XOR gates

Cells	Input Signals	Output Signal Probability ¹
INV	1: a	$P_{INV} = 1 - p_A$
NAND	2: a, b	$P_{NAND} = 1 - (p_A \times p_B)$
NOR	2: a, b	$P_{NOR} = (1 - p_A) \times (1 - p_B)$
XOR	2: a, b	$P_{XOR} = p_A \times (1 - p_B) + p_B \times (1 - p_A)$

¹ Signal probability is the probability of the signal to be at logic value 1

For instance, consider the inverter gate. Given the input probability $p(a = 1) = 1$, i.e. the signal is always at logic value 1, considering its Boolean function, the probability of the output signal to be at logic value 1 is 0 ($P_{INV}(\text{output} = 1) = 0$). Thus, the signal probability equation for the inverter can be expressed by Equation 5.2:

$$P_{INV}(\text{output} = 1) = 1 - p(a = 1) \quad (5.2)$$

For clarity, the probabilities $P_{GATE}(\text{output} = 1)$, $p(a = 1)$, $p(b = 1)$ will be shortened to P_{GATE} , p_A and p_B . Following the signal probability calculation step in the Figure 5.23 is the pin swapping process. In this process, with the pin assignment rules and the signal probabilities, an optimization

algorithm can identify which pin should be swapped in order to reduce the occurrence of the interchangeable input combination with the higher SET cross-section. After the pin swapping, the standard design flow is performed with the optimized netlist.

In order to obtain important reliability information to be addressed in the optimization process, the SET characterization methodology is aligned to the identification of the input dependence [66, 188]. The sensitivity of each standard cell is extracted from the layout design in the Graphical Design System (GSDII) file. Thus, the Monte Carlo simulation tool, MC-Oracle [43], is used to obtain the SET currents. In order to consider the input signal probabilities, the Equation 6.1 is used. Given n input combinations, the overall gate SET cross-section σ_{SET} can be estimated from the input SET cross-section $\sigma_{SET}(i)$ and the input probability $p(i)$:

$$\sigma_{SET} = \sum_{i=0}^n \sigma_{SET}(i) \times p(i) \quad (5.3)$$

The input cross-section $\sigma_{SET}(i)$ is provided by the SET characterization while the input probabilities are provided by the Signal Probability Calculation in Figure 5.24. Then, this equation is used in the Pin Swapping process to evaluate when the input pins assigned from the logic synthesis should be swapped to decrease the gate SET cross-section. Similarly, this process can also adopt the soft-error rate estimation for a given mission orbit. In this work, two orbits were analysed: the Geostationary (GEO) and the International Space Station (ISS) orbits. The Integral Rectangular Parallelepiped (IRPP) method is used as specified by the European Cooperation for Space Standardization (ECSS) [52]. Additionally, a fixed shielding of 1 g/cm^2 is used and, under solar minimum, the international standard ISO 15390 [189] and NASA AP8MIN [143] flux models are used for the Galactic Cosmic Rays (GCR) and the trapped proton radiation. In this work, the standard cells are provided from the 45 nm OpenCell Library from NanGate [129].

5.2.2 Impact on the SET cross-section of standard cells

Based on the cross-section of the interchangeable input combinations, an optimized logic synthesis should prioritize the pin assignment of the lowest signal probability in such a way the most sensitive interchangeable input combination obtains the lowest probability of occurrence [188]. The input SET cross-section for NAND, NOR and XOR gates under particle Linear Energy Transfer (LET) of $5 \text{ MeV.cm}^2/\text{mg}$ is shown in Figure 5.25. It is possible to identify the most sensitive input combinations.

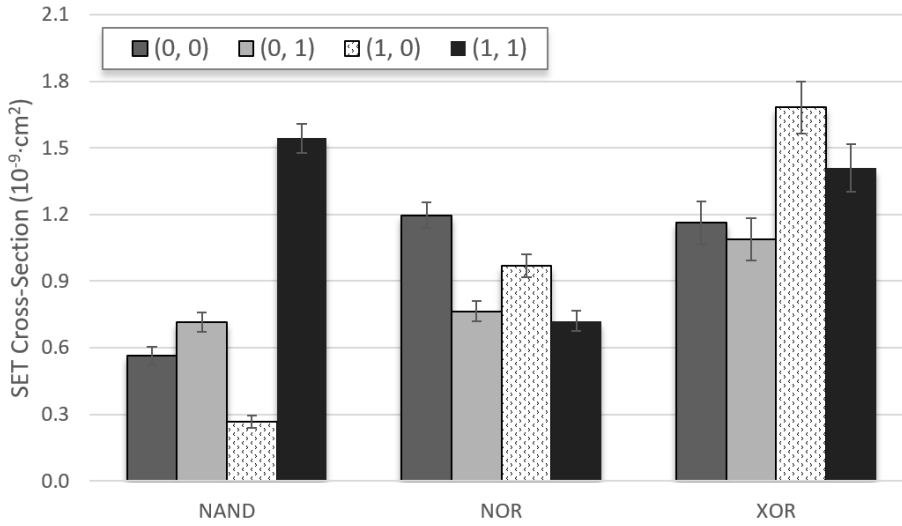


Figure 5.25: Input SET cross-section for the NAND, NOR and XOR gates under a particle with $\text{LET} = 5 \text{ MeV.cm}^2/\text{mg}$.

Considering the interchangeable input, i.e. (0, 1) and (1, 0): the NAND gate is the only cell to show the lowest cross-section for the (1, 0), while the NOR and XOR gates present the (0, 1). It implies that, considering low particle LET, the lowest signal probability should be assigned to the input B for the NAND gate, and to the input A for the NOR and XOR gates. In Figure 5.26, the gate SET cross-section is calculated for the NAND and NOR gate using the Equation 6.1 and considering 3 scenarios of input probabilities (Table 5.5 contains all the Weibull fitting parameters). Notice that, the input dependence of the SET cross-section is also dependent on the LET.

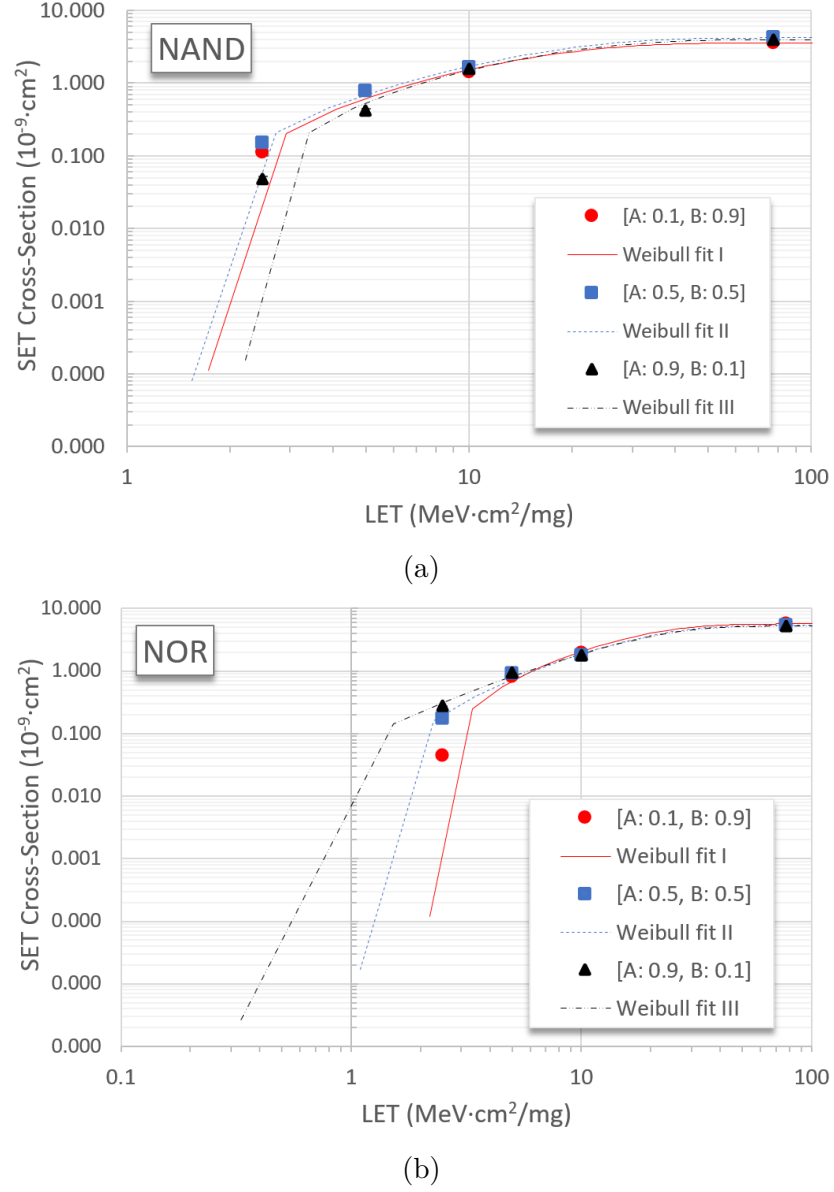


Figure 5.26: SET cross-section curves for the NAND and NOR gate in 3 input scenarios

It can be also observed in Figure 5.27, in which the input SET cross-section is shown for $78 \text{ MeV.cm}^2/\text{mg}$. Based on the SET cross-section curve, we can observe that signal probability will play an important role for low particle LET. As discussed previously, this behavior is related to the different charge collection efficiencies and the interplay relationship between pull-up

and pull-down recovery dynamics. Due to this characteristic, the in-orbit rate should be analyzed to identify the best pin assignment strategy considering the complete range of particle energy present in a given radiation environment and mission duration. This analysis is discussed later in this section.

Table 5.5: Weibull fitting parameter from the cross-section curves of Figure 5.26. Saturation cross-section and threshold LET correspond to Sat XS and LET_{TH} values, respectively.

		W	S	Sat XS (10^{-9} cm^2)	LET_{TH} ($\text{MeV.cm}^2/\text{mg}$)
NAND	I	13.74	1.16	3.57	1.73
	II	14.68	1.19	4.18	1.55
	III	14.84	1.15	3.94	2.22
NOR	I	15.03	1.22	5.68	2.19
	II	16.94	1.31	5.38	1.09
	III	17.71	1.33	5.22	0.33

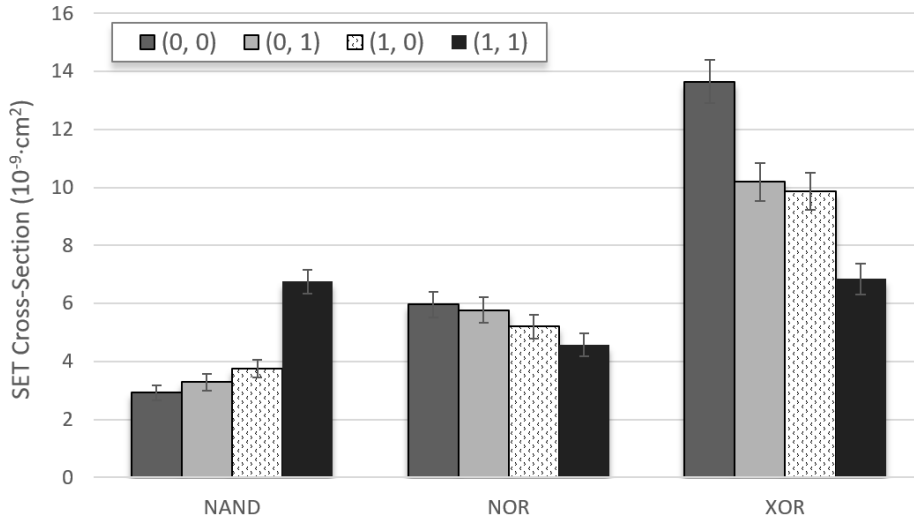


Figure 5.27: Input SET cross-section for the NAND, NOR and XOR gates under a particle with $LET = 78 \text{ MeV.cm}^2/\text{mg}$.

When adopting 3-input logic function such as AOI21 and OAI21, it is not possible to obtain a complete symmetric input relationship as observed for the 2-input gates. It is necessary to identify the interchangeable input

combinations and also what we denominate as the controllable input pin, i.e. the pin that controls the output of the function and the pin assignment cannot optimize it otherwise it will interfere within the correct logic function of the circuit. In Figure 5.28, the transistor network and truth table of the AOI21 gate is shown along with the interchangeable input combinations highlighted in red. In this case, A1 is the controllable input pin while two pairs of interchangeable input combination are possible: when A1 is in low logic level, $(0, 0, 1) \leftrightarrow (0, 1, 0)$; and, when A1 is in high logic level, $(1, 0, 1) \leftrightarrow (1, 1, 0)$. Analyzing the transistor network, it is possible to observe that the interchangeable input signal for the AOI21 are the ones from the series and parallel arrangement (B1 and B2). As the OAI21 gate is the complement of the AOI21 logic function, they present the same pairs of interchangeable input combinations.

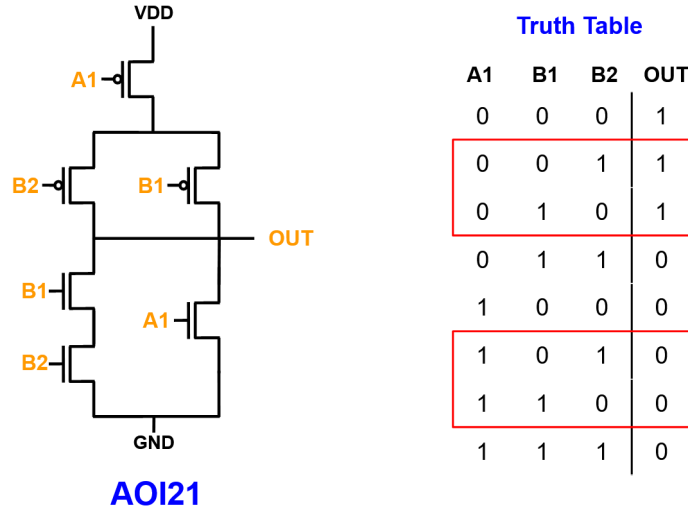


Figure 5.28: Transistor network and truth table of the AOI21 gate. The two group of symmetric input relationship are highlighted by the red rectangular.

The input dependence of SET cross-section for AOI21 and OAI21 is shown in the Figure 5.29 for a particle LET of $5 \text{ MeV.cm}^2/\text{mg}$. Interestingly, the interchangeable input combinations are the ones that provides the largest SET cross-sections. Thus, a greater impact can be expected when applying the pin assignment optimization. Among the pairs of interchangeable inputs,

the input combinations (0, 1, 0) and (1, 0, 1) provides the lowest for both circuits. If the controllable input pin A1 have a low signal probability, it means that the pair of interchangeable input combination $(0, 0, 1) \leftrightarrow (0, 1, 0)$ has a greater impact than the $(1, 0, 1) \leftrightarrow (1, 1, 0)$. As the (0, 1, 0) showed the lowest cross-section, it is recommended to assign the lowest signal probability to the input B2 so this input combination have a higher probability of occurrence then (0, 0, 1). As observed for the 2-input gates, this input dependence is dependent on the analyzed particle LET. Thus, the SET rates are analyzed for different scenarios of input probabilities in the next subsection.

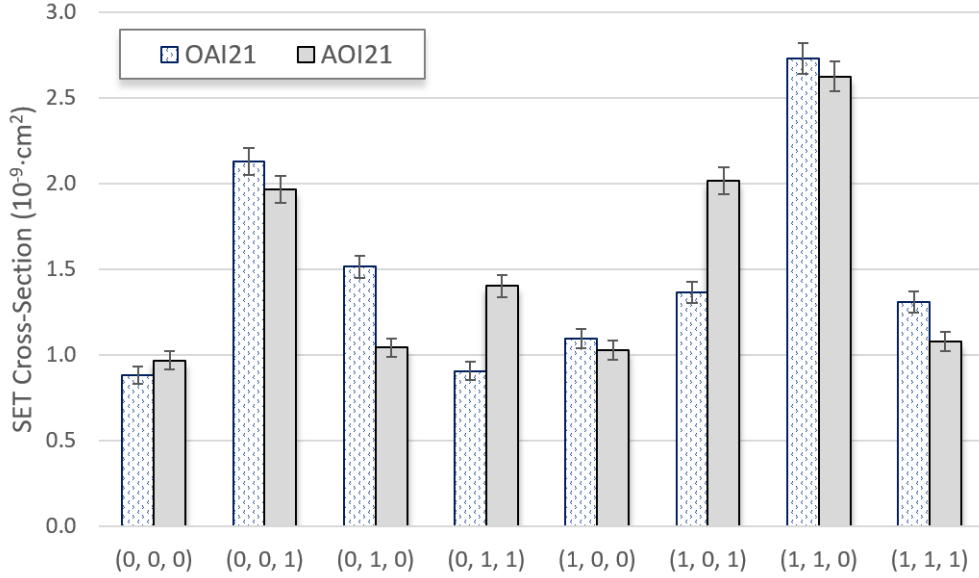


Figure 5.29: Input SET cross-section for the AOI21 and OAI21 gates under a particle with $LET = 5 \text{ MeV.cm}^2/mg$.

5.2.3 Impact on the in-orbit SET rates

After the characterization of the standard cells and the estimation of the cross-section curves using Equation 6.1 for each input scenario, the in-orbit SET rate can be calculated and it is shown in Figure 5.30 and Figure 5.31 for the 2-input and 3-input gates, respectively. Considering the 2-input

gates, the signal with the lowest probability should be assigned to the input B for the NAND gate, and to the input A for the NOR and XOR gates. This observation agrees with the cross-section obtained for low LET. As the major impact of input dependence is observed for low LET particles, it dominates the overall response in the optimization of the SET rate. The largest reduction is observed for the NAND gate operating in the GEO orbit, about 48% when the lowest signal probability is assigned to the input B.

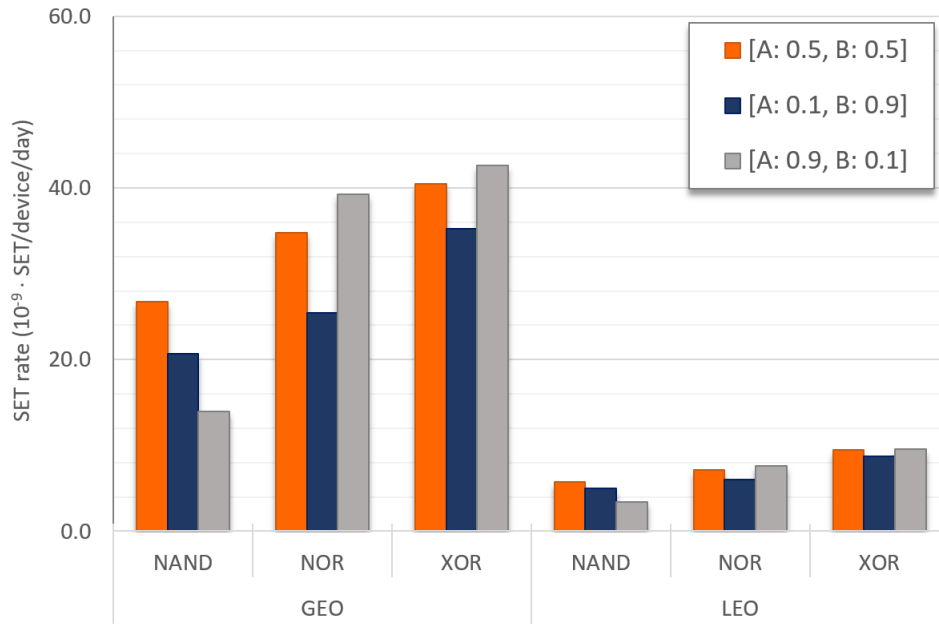


Figure 5.30: In-orbit SET rate for the NAND, NOR and XOR in the Geo-stationary orbit (GEO), 35,784 km, and International Space Station (ISS) orbit, 400 km, 51.64°.

For the 3-input gates, different conclusions can be drawn based on the signal probability of the controllable input A1: (1) if 0.1, both gates show reduced SET rate for the input scenario which B2 has the lowest signal probability; (2) if 0.5, the lowest SET rate for the AOI21 is still observed when B2 has the lowest signal probability, while for the OAI21, the reduced rate is obtained when B1 has the lowest signal probability; (3) if 0.9, both circuits show a reduced rate when B1 has the lowest signal probability. Though the higher complexity of understanding the input dependence of the 3-input

gates, they provide the greater reductions on the SET rate, reaching up to 35% of reduction.

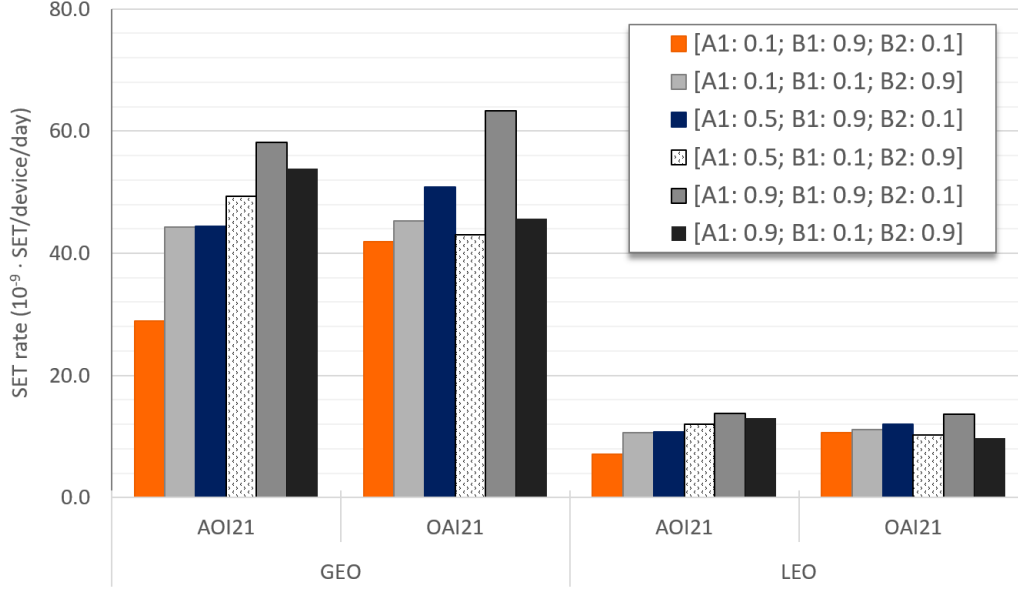


Figure 5.31: In-orbit SET rate for the AOI21 and OAI21 in the Geostationary orbit (GEO), 35,784 km, and International Space Station (ISS) orbit, 400 km, 51.64°.

5.3 Conclusions

In this chapter, the assessment of circuit-level techniques is presented. Firstly, a discussion on the importance of reliability-driven synthesis in the VLSI design flow is highlighted. The applicability of the proposed SEE prediction characterization to support synthesis algorithms targeting SEE resilience is verified. The cell-based characterization is able to provide insights on the sensitivity of logic gates considering different device technologies (high performance or low power devices) and also evaluate the impact of adopting low-power techniques as dynamic voltage scaling.

Given the input dependence of the SEE sensitivity of logic circuits, an optimization methodology is proposed to improve the overall circuit hardness through pin swapping based on the signal probability. The input dependence

is attributed to the different driving capabilities and the influence of the layout design on the SET robustness. As the influence of the layout design is LET dependent, the relationship among input signal and the gate SET cross-section is also shown to be dependent on the particle LET. The impact of adopting signal probability evaluation and pin assignment have shown the greatest cross-section reduction for low particle LET. Considering the 2-input gates, the signal with the lowest probability should be assigned to the input B for the NAND gate, and to the input A for the NOR and XOR gates. For the 3-input gates, different conclusions can be drawn based on the signal probability of the controllable input. This optimization technique provides no area overhead and can be used along with other hardening techniques. Additionally, it does not impact on the cell placement and the net routing is impacted minimally and locally.

6

Hardness improvement of RHBD techniques

Previously, the input dependency of the radiation sensitivity of digital logic circuits was verified in the results. Accordingly, a pin assignment was proposed to improve the radiation hardness of standard cells. However, the efficiency of well-know RHBD techniques such as Gate Sizing (GS) and Transistor Stacking (TS) have also shown a high input dependency. Thus, signal probability can also be used to enhance the radiation robustness of VLSI circuits by more accurately selecting the best hardened design for a given application. In this chapter, the signal probability is addressed to evaluate the hardening efficiency of the GS and TS designs. Also, hardware redundancy based on Triple Modular Redundancy (TMR) schemes can profit from the input dependency of the majority voter (MJV) architectures. The SET characterization of five different MJV architectures is provided and signal probability is proposed as an optimization strategy for the TMR block insertion process.

6.1 Gate Sizing and Transistor Stacking

As shown previously in the Chapter 4, the gate sizing and transistor stacking techniques have a strong SET cross-section dependence on the in-

put signal of the hardened circuits. Thus, with the pin assignment methodology in Chapter 5, the radiation hardening efficiency of such techniques can be enhanced depending on the input scenario of a given subcircuit. For instance, the SET cross-section for the unhardened NAND gate and the GS-based and TS-based designs is shown in Figure 6.1 for particle LET of $78.23 \text{ MeV.cm}^2/\text{mg}$. Five different input probabilities scenarios are evaluated: (1) [A: 0.5, B: 0.5], when both inputs have the same signal probability of 50% and it corresponds to the mean SET cross-section value discussed throughout this thesis so far; (2) [A: 0.1, B: 0.9], the input A has a lower signal probability than input B; (3) [A: 0.9, B: 0.1], the input A has a higher signal probability than input B; (4) [A: 0.1, B: 0.1], both input have the same signal probability of 10%; and, (5) [A: 0.9, B: 0.9], both inputs have the same signal probability of 90%. As discussed previously, these two techniques do not provide hardening for high particle LETs, when observing the mean SET cross-section value (the scenario 1). However, the TS-based NAND circuit can indeed show a reduced SET sensitivity even for a high particle LET in two particular scenarios as shown in Figure 6.1: the [A: 0.9, B: 0.1] and the [A: 0.1, B: 0.1], with a reduction of approximately 63% and 36%, respectively. Due to the hardened input (1, 0) provided by the TS-based NAND design, the overall SET cross-section can be improved whenever the input B is assigned to a low signal probability. However, if both inputs have a high signal probability as in the scenario [A: 0.9, B: 0.9], none of the hardened designs succeeded in providing lower SET sensitivity than the unhardened one. In fact, an increase of approximately 8% and 88% is expected for the GS-based and TS-based NAND gate, respectively. Thus, analyzing only the input scenario [A: 0.5, B: 0.5], i.e. the mean SET cross-section value, can be misleading and induce an increase in the SEE sensitivity of the circuit. Figure 6.2 presents the results considering a low particle LET, $3.89 \text{ MeV.cm}^2/\text{mg}$. In this situation, the GS-based design provides the best SET response for all input scenarios except for the scenario [A: 0.1, B: 0.1]. Hence, if both inputs have a low signal probability, the TS-based NAND design is able to overcome the GS-based NAND for high and low LET.

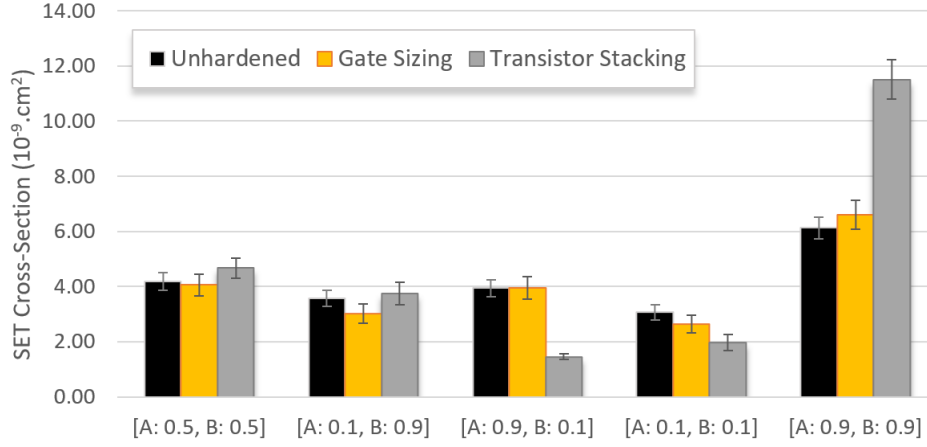


Figure 6.1: SET cross-section for the NAND gate (unhardened, gate sizing and transistor stacking versions) under particle LET of $78.23 \text{ MeV.cm}^2/\text{mg}$ considering five signal probability scenarios.

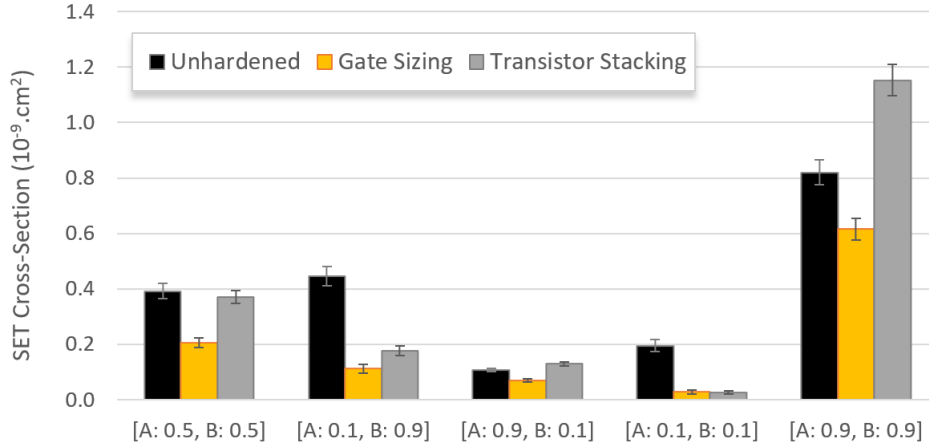


Figure 6.2: SET cross-section for the NAND gate (unhardened, gate sizing and transistor stacking versions) under particle LET of $3.89 \text{ MeV.cm}^2/\text{mg}$ considering five signal probability scenarios.

Similar conclusions can also be obtained for the NOR gate as shown in Figure 6.3 and Figure 6.4. When considering the mean SET cross-section of the designs under high particle LET, both RHBD techniques do not show any improvement on the SET robustness. However, when considering the input scenarios some designs can show better performance, as in the case of the scenario [A: 0.1, B: 0.9] and [A: 0.9, B: 0.9] in which the TS-based NOR

design overcome the gate sizing approach. A SET cross-section reduction of approximately 72% and 36% can be reached for the [A: 0.1, B: 0.9] and [A: 0.9, B: 0.9], respectively. The transistor stacking approach provides a hardened (0, 1) for the NOR design. Thus, whenever the input B has a high signal probability, the occurrence of the hardened (0, 1) is increased and a reduction on the overall SET cross-section is expected. However, if both inputs have a low signal probability as in [A: 0.1, B: 0.1], both RHBD techniques can increase the SET sensitivity of the circuit. Thus, to better quality the hardened design that best fit for a given application, the estimation of the switching activity of the internal signals can be helpful. For low LET, the gate sizing approach has also shown a better performance as observed for the NAND gate. However, for the scenario [A: 0.9, B: 0.9], the TS-based NOR still succeeds in providing the lowest SET cross-section overcoming the gate sizing design. Besides improving the radiation hardening of the techniques with input dependence, the proposed pin assignment based on the signal probability provides a more application-specific hardening analysis. In this sense, the circuit designer is able to select more efficiently the best hardened component for a specific application and avoid misleading qualifications.

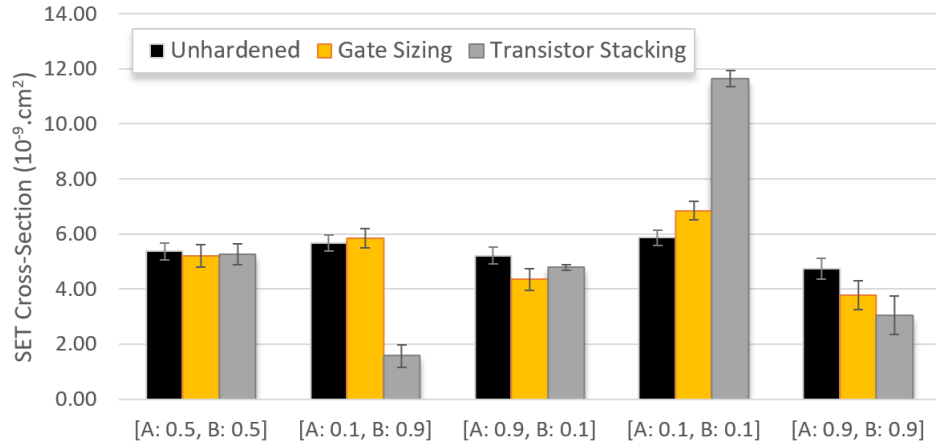


Figure 6.3: SET cross-section for the NOR gate (unhardened, gate sizing and transistor stacking versions) under particle LET of $78.23 \text{ MeV.cm}^2/\text{mg}$ considering five signal probability scenarios.

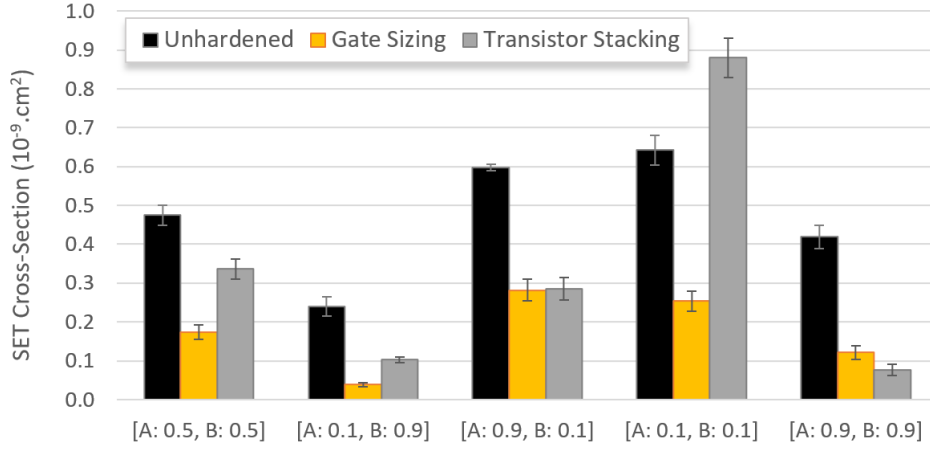


Figure 6.4: SET cross-section for the NOR gate (unhardened, gate sizing and transistor stacking versions) under particle LET of $3.89 \text{ MeV.cm}^2/\text{mg}$ considering five signal probability scenarios.

6.2 Hardware Redundancy

Fault tolerance is increasingly necessary for advanced technology circuits due to the high complexity and susceptibility to physical defects and environment disturbances as provoked by radiation interactions [100, 106, 99, 28]. Safety- and mission-critical systems, such as satellites and aircraft flight control systems, are the primary applications using fault-tolerance techniques to improve reliability. A system is assumed to be fault-tolerant when its functionality is preserved even with the presence of faults. Commonly, redundancy is the core foundation of fault tolerance techniques proposed in the literature [99]. Different from the previous hardening techniques, fault tolerance aims to mask the soft errors rather than preventing the origin of the SEE generation, i.e. the energy deposition and charge collection. There is a variety of approaches, according to the redundant part added to the system, ranging from hardware and software to information and time redundancy [100]. Hardware redundancy, also known as spatial redundancy, is widely used in space applications due to its capability of performing fault detection and/or fault correction [106]. One of the most used technique is the so-called Triple-Modular Redundancy (TMR), in which the selected critical compo-

nent or electronic circuit is triplicated and their outputs are connected to a majority voter (MJV) architecture, as explained in the Section 3.2.2. In summary, whenever two copies of the component are fault-free, the output of the majority voter will be also fault-free. However, if a fault occurs in the MJV, the technique fails to provide a correct function of the system. The applicability of TMR schemes as a Radiation-Hardening-by-Design (RHBD) approach can extend from masking the effects of Single-Event Transients (SETs) in data paths or Single-Event Upsets (SEUs) in memory elements. However, the majority voter robustness against radiation effects is crucial for the fault detection and correction efficiency of TMR strategies. Few works in the literature have provided design studies on the radiation robustness of majority voters in terms of power, delay, area and SET cross-section [190, 191, 45, 192]. The work developed in [190] provides heavy-ion experimental data and proposes a relative efficiency criterion for the majority voter selection according to the TMR strategy. Two FinFET-based majority voter circuits were evaluated under the atmospheric environment in [45]. In this case, the NAND- and NOR-based voter circuits have shown a similar soft-error rate (SER) due to the symmetric sizing of the PFET and NFET devices provided by the strain engineering and width quantization at FinFET technology [45]. The work in [192] adopts a layout-level analysis through stick diagram to evaluate the diffusion area of majority voters and to calculate a fault masking ratio. Despite the layout-based approach, charge sharing between internal nodes and, very importantly, the intra-cell charge sharing effect in the multi-level circuit implementations are not considered, which can considerably increase the voter sensitivity or reduce it through pulse quenching effect [151]. Although the good fault coverage in TMR schemes, one of the main drawbacks of adopting redundancy-based hardening techniques is the considerably high increase in area and power consumption [100, 106, 99]. Thus, it is of utmost importance to adopt optimization strategies in the TMR block insertion to selectively address the most sensitive nodes in the target design and lower the impact on the area usage and power consumption. In this work, a design exploration of MJV architectures robust to SET effects is presented considering the SET cross-section dependence on the input signals. The five architectures shown

in Figure 6.5 were designed based on a commercial 65nm bulk CMOS technology. As the folded circuits designed in Section 4.2, the MJV circuits were designed to be compatible with a standard-cell library. A fixed cell height is set to 13 tracks of the metal pitch, i.e. $2.6\mu\text{m}$ high. To provide flexibility in the cell routing, intra-cell connections are primarily done using the metal 1 (M1, blue), except for some cases in which metal 2 (M2, orange) is used horizontally.

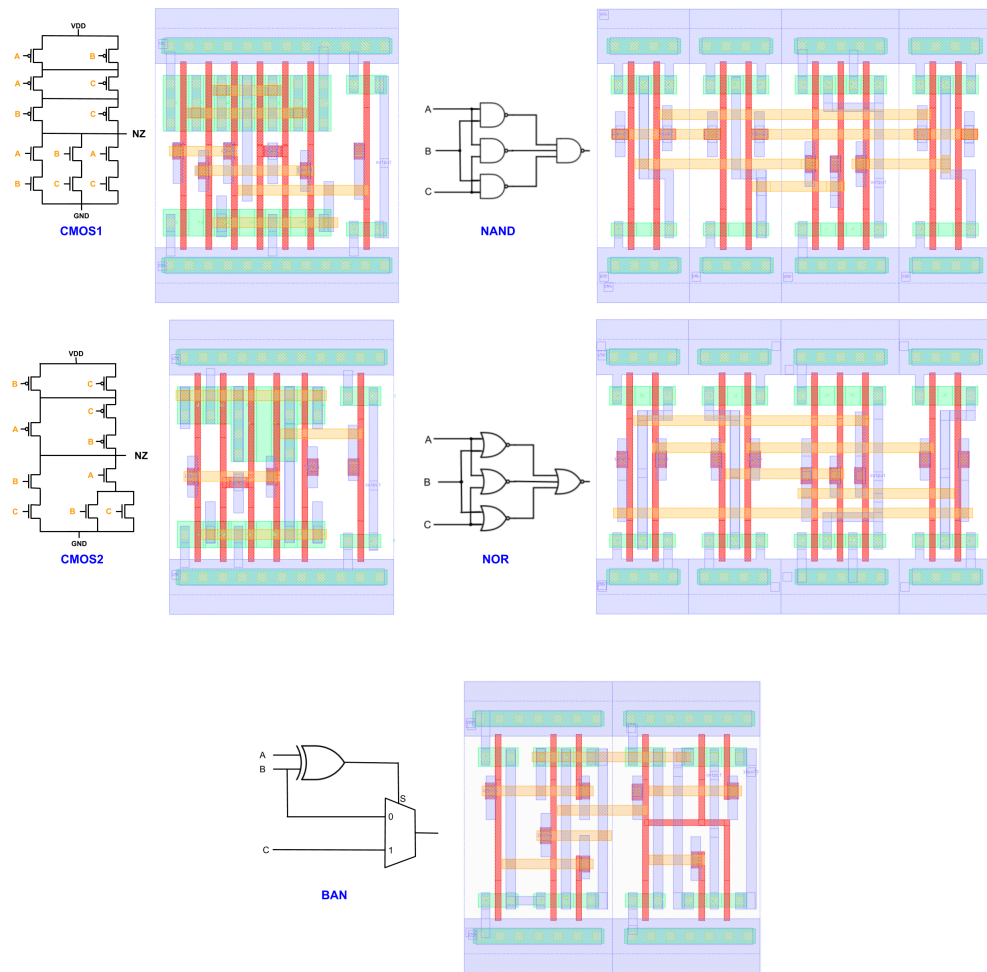


Figure 6.5: Circuit- and Layout-level implementations of the complex-gate and standard-cell-based majority voter architectures. For simplicity, only metal1 (blue), metal2 (orange), active diffusion (green) and poly (red) layers are shown.

The design of the two complex-gate majority voter followed the Euler's path graph theorem to optimize their physical layout by avoiding diffusion breaks and alleviating metal connectivity congestion [193]. For the cell-based implementations, the NAND2, NAND3, NOR2, NOR3, XOR and MUX gates were designed and characterized separately, as standard cells. To achieve a reduced layout area, both XOR and MUX circuits were designed in the PTL (Pass-Transistor Logic) style [141]. Logical Effort (LE) sizing approach was applied to all circuits to provide a driving capability comparable of the minimum-sized inverter of the cell library [194]. The transistor sizing of the minimum-sized inverter has a PMOS/NMOS ratio of 190nm/135nm. Logical Effort approach is widely used in cell library design to achieve balanced delay performance. Accordingly, to provide means of comparison between the MJV designs based on standard cells and complex CMOS implementations, only the LE sizing is adopted in this work. The Euler's path graph theorem is commonly used as a layout design optimization in which a transistor ordering is provided in such a way that diffusion breaks are avoided and metal connectivity is optimized. In Figure 6.6, the Euler's path graph theorem is applied to the CMOS 1 and CMOS2 voter.

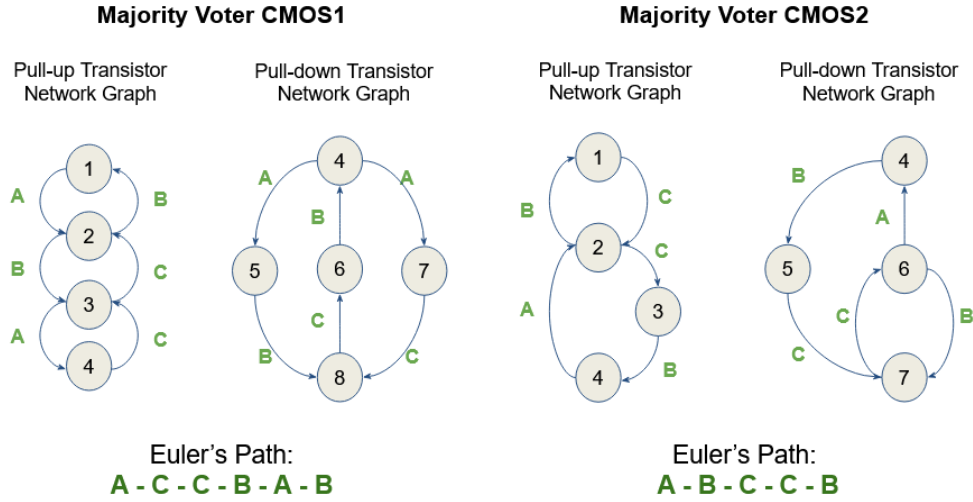


Figure 6.6: Euler's path graph theorem applied to the majority voter CMOS1 and CMOS2 layout designs.

The pull-up and pull down transistor networks, i.e. PMOS and NMOS transistors, are translated into two graphs in which the vertices corresponds to the shared source/drain junctions of the circuit and the edges are the input signal of each transistor in the network. The Euler's path, in summary, is the path that goes through all the vertices in both graphs such that each edge is traversed only once. Not all transistor networks can provide a Euler's path, however, it is also possible to obtain many path solutions for a given circuit. In the case of the CMOS2 voter represented in Figure 6.6, one possible path is the ABCCB. In this work, the path ACCBAB and ABCCB are the Euler's paths used to design the CMOS1 and CMOS2 layouts, respectively. Table 6.1 presents the number of transistors and the layout and drain area information for each voter architecture. The percentage of layout design that corresponds to the collecting drain area is also indicated. Due to the reduced number of transistor provided by the logic factoring, CMOS2 voter provides the smallest layout area. However, despite the larger number of transistors, the smallest drain collecting areas are observed for the cell-based implementations, with the smallest drain area for the NAND-based MJV. The two complex-logic implementations have about $2\times$ the drain area of the cell-based designs.

Table 6.1: Number of transistors, layout and drain area (μm^2) of the CMOS1, CMOS2, NAND-based, NOR-based and BAN majority architectures

Voters	# of Transistors	Layout Area	Drain Collecting Area
CMOS1	14	6.45	0.890 (13.8%)
CMOS2	12	5.93	0.855 (14.4%)
NAND	18	10.45	0.415 (3.9%)
NOR	18	10.45	0.455 (4.3%)
BAN	12	7.90	0.471 (5.9%)

As logical effort is adopted to provide comparable driving strength, the 3-transistor stacks used in the two complex-logic design implementations increase the drain collecting area as the transistor width is upsized. Only about 4% and 6% of the total layout of NAND/NOR and BAN voters represent the drain collecting area, respectively, while about 14% is expected for

the CMOS1 and CMOS2 implementations. Thus, adopting complex-logic based MJV architecture provides a more compact and reduced layout design. However, an increase in the drain collecting area is expected to account for the drive capability of the stacked transistors [195]. Hence, the overall SET susceptibility of the circuit is affected by an increased charge collection efficiency. In this work, the SET pulse width, cross-section and in-orbit rate is calculated for the five majority voter architectures. The maximum, mean and standard deviation of the SET pulse width distribution is shown in Figure 6.7 when considering a particle LET of $78.23 \text{ MeV.cm}^2/\text{mg}$. Considering the MJV circuits exploring standard cells, the lowest pulse widths are observed for the BAN voter while the NOR voter presents a wider distribution than the NAND voter. This observation is in agreement with the literature, as in [45] the FinFET-based NOR majority voter has also shown a wider SET distribution than the NAND implementation. Despite the great drain area in the complex-gate MJV design, the CMOS1 and CMOS2 voters show a shorter SET distribution than the NAND and NOR voters. This shorter distribution is attributed to the contribution of pulse quenching effect (PQE) inherent of inversion stages in combinational circuits [151]. As both CMOS1 and CMOS2 present an inverter gate in its output, the PQE is enhanced in these architecture and the overall SET distribution is shortened.

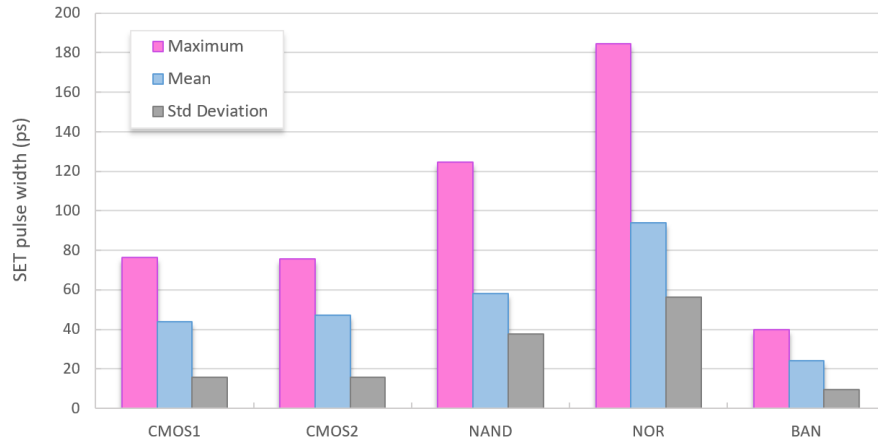


Figure 6.7: Maximum, mean and standard deviation of the SET pulse width distribution for the CMOS1, CMOS2, NAND, NOR and BAN voters under particle LET = $78.23 \text{ MeV.cm}^2/\text{mg}$.

In Figure 6.8, the SET cross-section for each circuit design is shown for two particle LET values, 78.23 and 9.94 $\text{MeV}\cdot\text{cm}^2/\text{mg}$. Although the two complex-gate implementations, CMOS1 and CMOS2, present reduced layout, they have shown the highest sensitivity for high and low LET. The reduced number of transistors of the CMOS2 implementation provided by logic factoring only induced a slight reduction of about 8% on the SET cross-section for high LET. On the other hand, an increase of about 26% is observed at low LET, when compared with the CMOS1 architecture. This can be attributed to the transistor restructuring and the consequent impact on the collecting area and the internal capacitance of the circuit [195].

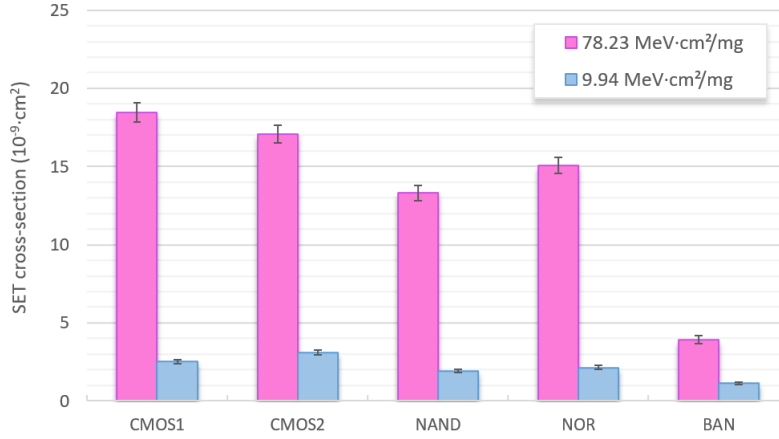


Figure 6.8: SET cross-section estimation for CMOS1, CMOS2, NAND, NOR and BAN majority voter architectures considering particle LET equals to 78.23 and 9.94 $\text{MeV}\cdot\text{cm}^2/\text{mg}$.

Further, despite the larger design area, the lowest cross-sections were obtained for the MJV architectures based on standard cells. As observed in the previous section, by using smaller transistor in the cell-based designs a reduced drain collecting area can be achieved compared to the complex-gate implementations. However, these results provide the average cross-section obtained for logic input at high and low levels. To better understand the design implications on the overall sensitivity of the circuit, the next subsection provides a discussion on the input dependence of the cross-section curve for each architecture.

The SET cross-section of the MJVs for the two possible input configuration in a fault-free TMR condition is studied: all inputs equal to 1; and, all inputs equal to 0. Considering the results for the complex-gate implementations in Figure 6.9, the CMOS2 circuit has shown a higher input dependence than the CMOS1. This is attributed to the sizing and symmetry/asymmetry of the pull-up and pull-down transistor networks. The CMOS1 architecture allows a symmetric physical layout and consequently a balanced drain collecting area distribution. On the other hand, different sizing of each branch of the transistor networks in the CMOS2 architecture provides an asymmetric physical layout and an unbalanced distribution of the collecting areas, i.e. a considerably larger collecting area is observed for the PMOS devices than for the NMOS. Furthermore, both circuits have shown a higher cross-section for the input 1 configuration due to the larger PMOS devices and lower driving capability of NMOS devices.

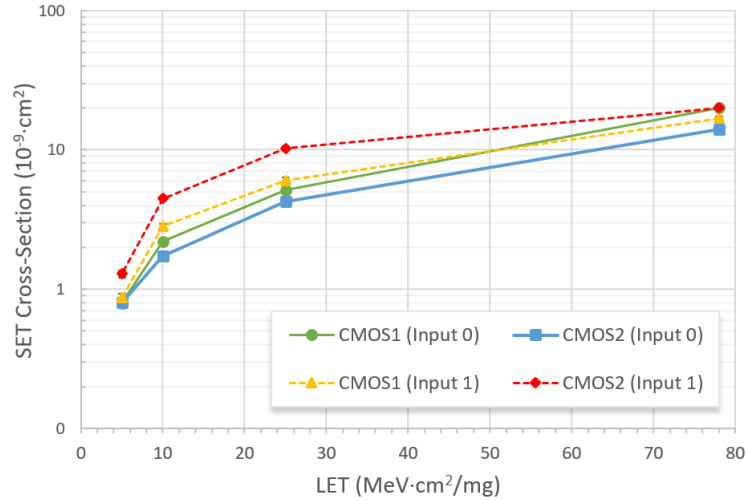


Figure 6.9: SET cross-section for the complex-gate architectures considering the two possible input configuration in a fault-free TMR scheme: all inputs in high logic level (Input 1); and, all inputs in low logic level (Input 0).

For the majority voters composed by basic logic standard-cells, we can observe two distinct behaviors, as seen in Figure 6.10: (1) a fairly low input dependence for the BAN voter; and, (2) a high input dependence for the NAND and NOR architectures. The nature of this variation is directly re-

lated to the logical masking effect capability of the MUX gate and the 3-input NAND/NOR gate in the output of the circuit, respectively. For instance, in the case of the BAN voter, when the TMR input configuration is at low logic level, i.e. all inputs equal to 0, the output of XOR gate evaluates to low logic level and the input B is selected as the output signal to the voter, as shown in Figure 6.11. If a SET occurs at the XOR gate, the MUX gate will select the input C as the output signal, which, in a fault-tree TMR scenario, would result in no SET propagation in the output of the voter. Ideally, in the TMR schemes, the majority voter is placed far from the triplicated blocks so a particle strike is not able to induce SEE in the blocks and the voter simultaneously. This logical masking effect is also observed for the input scenario where all the blocks evaluate to high logic value (input 1), also illustrated in Figure 6.11. Thus, the SEE sensitivity of the BAN voter is reduced to the radiation sensitivity of the MUX gate, for both input scenarios, explaining the low input dependence.

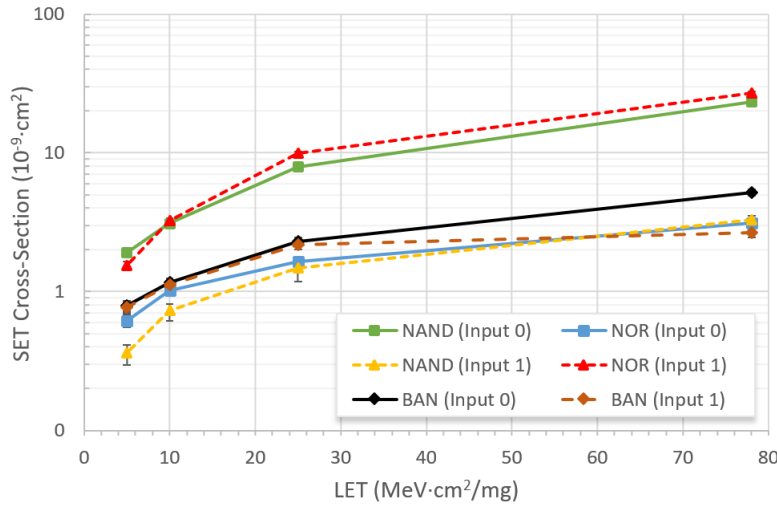


Figure 6.10: SET cross-section for the basic-logic gate architectures considering the two possible input configuration in a fault-free TMR scheme: all inputs in high logic level (Input 1); and, all inputs in low logic level (Input 0).

In the case of the NAND voter, when all inputs are at low logic value, the architecture is sensitive to the SET occurrence in any of the 2-input NAND

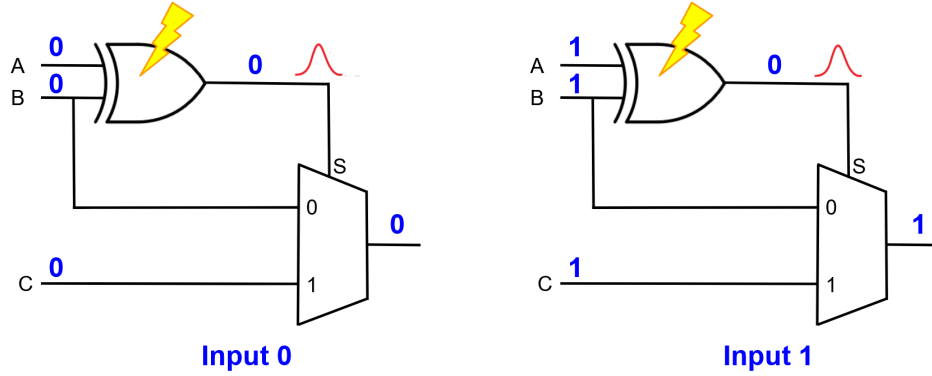


Figure 6.11: Logical masking capability within the BAN voter architecture.

gates and the 3-input gate as depicted in Figure 6.12. On the other hand, for the TMR input configuration at high logic level, i.e. all inputs equal to 1, the 3-input NAND gate is logically masking any of the SET in the 2-input NAND gates. The 3-input NAND gate will evaluate to high logic value as long as at least one of its input is at low logic value. Thus, for the input 1 scenario, the particle strike has to be able to induce a SET in the three 2-input NAND gates simultaneously so a SET is observable in the output of the MJV. The same phenomenon is observed for the NOR architecture, but the logical masking occurs when the TMR input configuration is set to low logic level [195]. Hence, depending on the output signal of the triplicated blocks in the TMR scheme, the NAND and NOR voters can provide a sensitive area only issued from the charge collection in its 3-input gate. Given the high input dependence of certain designs, the next subsection provides a signal probability analysis and discusses how it could be used to optimize the application of TMR schemes.

As aforementioned previously, the estimation of signal switching activity is widely used in circuit design to perform power and performance analysis. However, it can also be used to perform reliability analysis as shown in [177]. For instance, consider the signal probability p as the probability of the a particular net within a circuit design to be in high logic level. As shown previously, the CMOS1 and CMOS2 architectures provide higher cross-sections for the input-1 scenario (Figure 6.9). Therefore, the TMR insertion method-

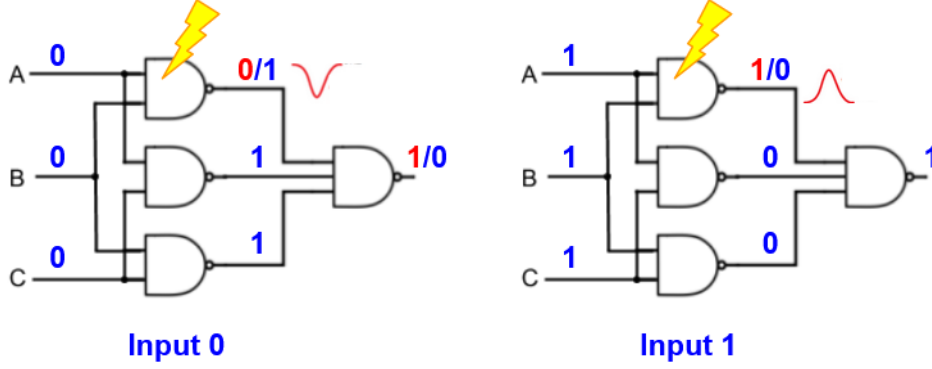


Figure 6.12: Logical masking capability within the NAND voter architecture.

ology should prioritize the insertion of these architectures in the sensitive nodes with the lowest signal probability. Considering the signal switching activity of the input signals, the gate cross-section σ_G can be calculated using the Equation 6.1, where n corresponds to the number of input combinations, σ_i is the SET cross-section for input combination i , and $p(i)$ is the input combination signal probability. However, as in a fault-free TMR condition, the 3 input signals of the voter have the same signal probability p and only 2 input combinations ($n = 2$), then Equation 6.1 can be reformulated as Equation 6.2, where σ_{MJV} is the majority-voter SET cross-section, p_{TMR} is the signal probability of the node in which the TMR will be inserted, σ_0 and σ_1 are the SET cross-section calculated for the two possible input scenarios in a fault-free TMR condition, i.e. all inputs in low logic level (input-0 scenario) and all inputs in high logic level (input-1 scenario), respectively.

$$\sigma_G = \sum_{i=1}^n \sigma_i \times p(i) \quad (6.1)$$

$$\sigma_{MJV} = p_{TMR} \times (\sigma_1 - \sigma_0) + \sigma_0 \quad (6.2)$$

Considering the Equation 6.2, the SET cross-section curves were estimated for two signal probabilities and shown in Figure 6.13 and Figure 6.14, for $p = 0.1$ and $p = 0.9$, respectively. Notice that, for $p = 0.1$, in contrast with what we observed in Figure 6.8, the NAND architecture provides the

highest cross-section curve in Figure 6.13. This is explained by the considerable high SET cross-section observed for the input-0 scenario (as shown in Figure 6.10) and the low signal probability, $p = 0.1$. On the other hand, in Figure 6.14, the NAND architecture provides the lowest cross-section along with the BAN voter.

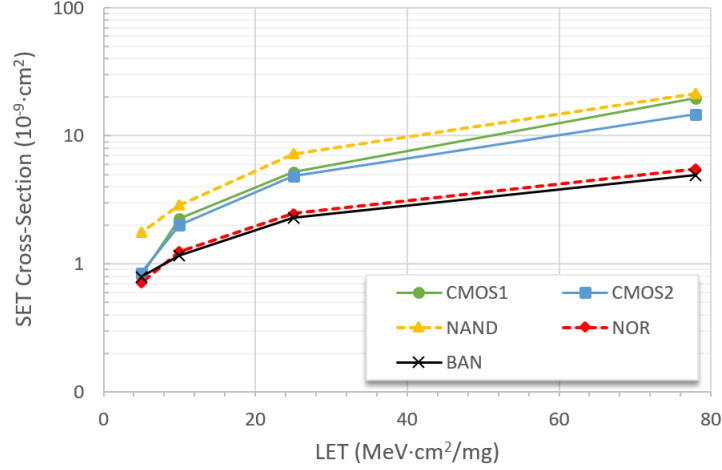


Figure 6.13: SET cross-section curves calculated for the majority voters considering a signal probability p of 0.1, i.e. higher probability of a fault-free TMR condition in the input combination (0, 0, 0).

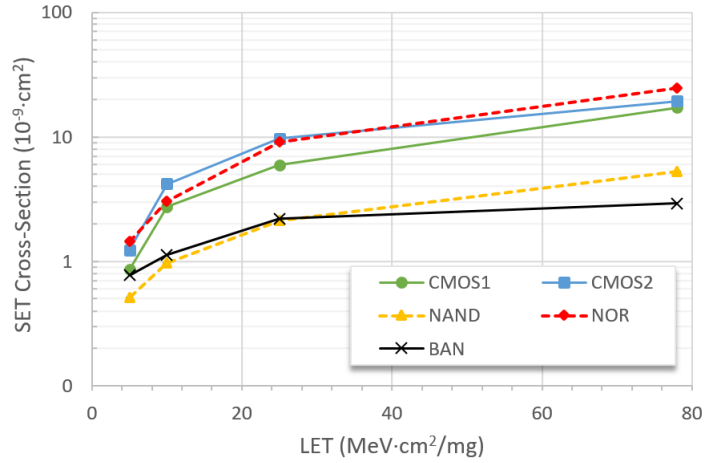


Figure 6.14: SET cross-section curves calculated for the majority voters considering a signal probability p of 0.9, i.e. higher probability of a fault-free TMR condition in the input combination (1, 1, 1).

Additionally, the NOR architecture provides the highest cross-section curves along with the CMOS1 and CMOS2 architectures. Thus, by considering the signal probability estimation to calculate the susceptibility of majority voter architectures, a more efficient and application-specific TMR insertion methodology can be obtained.

To verify the impact of a given radiation environment, Figure 6.15 presents the SET rates estimated for three signal probabilities ($p = 0.1$, $p = 0.5$ and $p = 0.9$) and two different orbits (GEO and ISS/LEO). Two distinct trends can be observed: the increase of SET rate as the signal probability is increased; the decrease of SET rate as the signal probability is increased. Different from the CMOS1, CMOS2, NOR and BAN architectures, the NAND voter is the only design that shows a decrease in the SET rate as the signal probability is increased. This is attributed to the lower SET cross-section for the input 1 configuration (Figure 6.10) due to the logical masking effect.

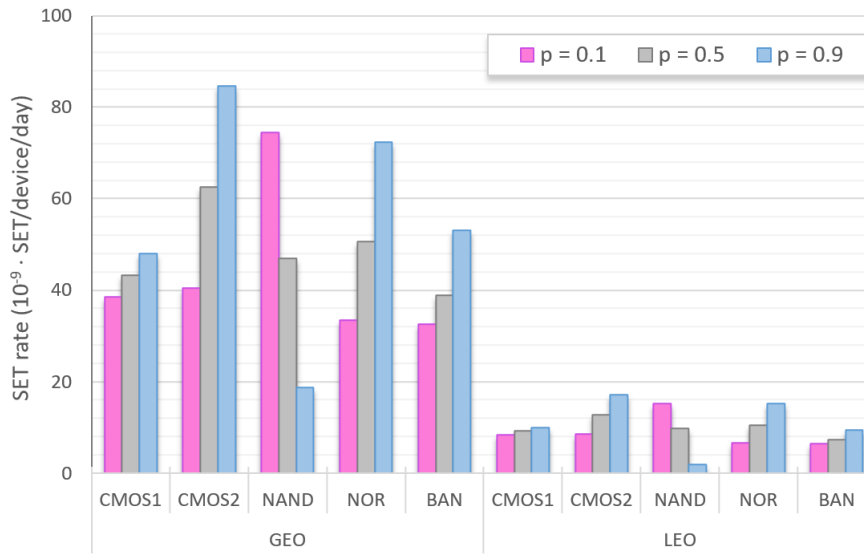


Figure 6.15: In-orbit SET rate calculated with OMERE [22] for the Geostationary orbit (GEO), 35,784 km, and for the International Space Station (ISS) orbit, 400 km, 51.64°. Three signal probability is considered: $p = 0.1$, $p = 0.5$ and $p = 0.9$.

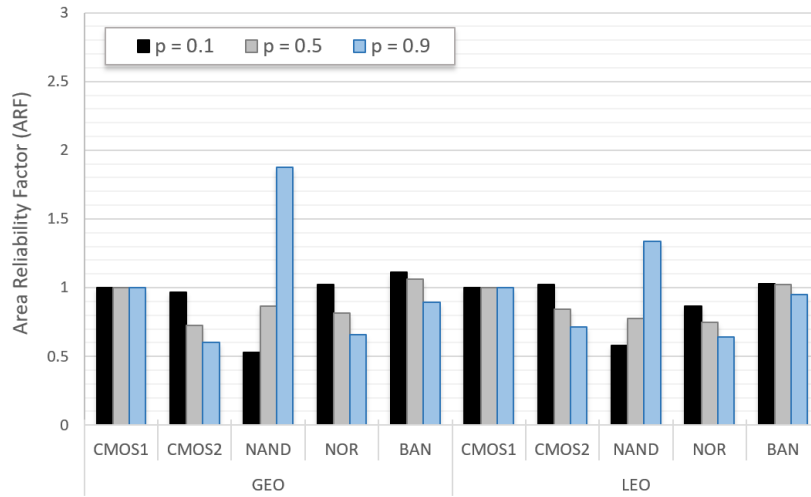
Additionally, the SET rate most sensitive to the input signal is observed for the NAND architecture while the CMOS1 is the less sensitive, a variation of approximately 300% and 25% from $p = 0.1$ to $p = 0.9$, respectively. In summary, considering the signal probability $p = 0.1$, $p = 0.5$ and $p = 0.9$, the best design for both orbits is the BAN/NOR, BAN and NAND, respectively.

Fault-tolerant designs using redundancy are often dealing with area overhead issues. To be able to assess the suitability of the majority voter regarding reliability and layout area, we have proposed the Area Reliability Factor (ARF) as described in Equation 6.3. The parameters α and β are the reliability and area coefficients, respectively. For projects with higher area constraints, a higher β can be used in the ARF calculation. The higher the ARF value, the better the circuit design. In Figure 6.16, the ARF is calculated for each majority voter considering the signal probability and for the two orbits. The results are normalized to the ARF calculated for the CMOS1 voter.

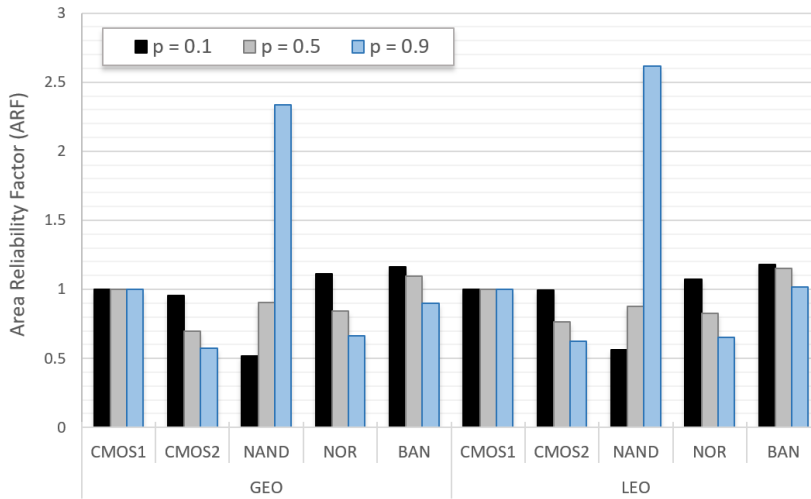
$$\text{Area Reliability Factor (ARF)} = \frac{1}{(\alpha \times \text{Rate}) + (\beta \times \text{Area})} \quad (6.3)$$

In Figure 6.16a both α and β coefficients are settled to 50%, i.e. area overhead is equally important than reliability. In this case, the BAN voter shows the highest ARF for $p = 0.1$ and $p = 0.5$, only losing to the NAND voter for the $p = 0.9$. The good SET response of the NAND voter for the input 1 scenario is so great that overcomes the area overhead of this architecture even when the area and reliability are equally important. For the GEO orbit, the NAND voter reaches almost 2 times the ARF value for the CMOS1 voter when $p = 0.9$. Although the CMOS2 voter provides the lowest layout area, its bad SET response prevented it to provide good ARF values, being inferior even to the CMOS1 voter. In Figure 6.16b, the reliability coefficient α is set to 80% while only 20% is set to the area coefficient β . In this scenario, the NAND voter can provide an ARF value over 2 times the one obtained for the CMOS1 voter in the GEO orbit, and over 2.5 times for the LEO orbit. As a higher α coefficient is used, the MJVs based on standard cells have shown

a greater ARF than what observed in Figure 6.16a. Thus, depending on the reliability and area constraints of a given system application, the ARF value based on the SEE rate calculated for the signal probability can be an efficient assessment tool to improve the radiation robustness while respecting design constraints.



(a) Reliability coefficient α and area coefficient β equal to 50%



(b) Reliability coefficient α equals to 80% and area coefficient β equals to 20%

Figure 6.16: Normalized Area Reliability Factor (ARF) for: (a) same coefficient for area and reliability, and (b) reliability coefficient (80%) is higher than area coefficient (20%)

6.3 Conclusions

Previously, the input dependency of the radiation sensitivity of digital logic circuits was verified in the results. Accordingly, a pin assignment was proposed to improve the radiation hardness of standard cells. However, the efficiency of well-know RHBD techniques such as Gate Sizing (GS) and Transistor Stacking (TS) have also shown a high input dependency. Thus, signal probability can also be used to enhance the radiation robustness of VLSI circuits by more accurately selecting the best hardened design for a given application. In this chapter, the signal probability is addressed to evaluate the hardening efficiency of the GS and TS designs. Also, hardware redundancy based on Triple Modular Redundancy (TMR) schemes can profit from the input dependency of the majority voter (MJV) architectures. The SET characterization of five different MJV architectures is provided and signal probability is proposed as an optimization strategy for the TMR block insertion process.

As shown previously, the hardening efficiency of RHBD has shown an input dependency. In this chapter, this dependence was used along the signal probability estimation in order to improve the overall radiation hardness of the circuit. Accordingly, pin assignment was used for logic circuits based on the gate sizing and transistor stacking. In this case, the improvements can reach up to 80% in the SET robustness. It was also shown that by disregarding the input signal, the hardened designs can show a higher SET cross-section than the unhardened one. Thus, besides improving the radiation hardening of the techniques, the proposed pin assignment provides a more application-specific hardening analysis. Hence, the hardening technique or circuit selection can be used more efficiently and avoid misleading qualifications.

And, to conclude, a characterization methodology based on the input dependency of the SEE is also proposed as an optimization strategy for TMR block insertion algorithms. Five distinct majority voter architectures (CMOS1, CMOS2, NAND-based, NOR-based and BAN voters) were designed and characterized under heavy ions and different input signal proba-

bilities. Despite the reduced layout design, complex-gate voter architectures have shown, on average, a higher SET cross-section than the implementations using basic logic standard-cell gates. As all architectures were designed to provide comparable driving strength, upsizing the stacked transistors in the complex-logic designs increases the charge collecting drain areas and, consequently, increases the SET cross-section of the circuit. Thus, aiming at a lower drawback in design area will compromise the reliability of the circuit. By evaluating the signal stimuli, a higher input dependence is observed for the basic-logic gate architectures (except for the BAN voter) due to the influence of logical masking effects. For instance, the 3-input gate in the output of the NAND and NOR architectures masks any SET in the 2-input gates when input scenario is high and low logic values, respectively. To overcome the logical masking effect and observe a SET in the output of the NAND and NOR architectures, the particle strike must deposit enough energy in the three replicas of the TMR schemes.

The SET rate for the CMOS1 architecture has shown to be the least dependent on the signal probability while the NAND voter showed the highest dependence. Furthermore, apart from the NAND voter, all the other design implementations have shown an increase in the SET rate as the signal probability is increased. The Area Reliability Factor (ARF) is used to verify the eligibility of the voters regarding not only the reliability but also the area constraints. The BAN voter shows the highest ARF for both $p = 0.1$ and $p = 0.5$ while the NAND voter shows the highest ARF for $p = 0.9$. Despite the larger area overhead of the NAND architecture, it succeeds in providing the highest ARF for $p = 0.9$ even when the area constraint are equally important than the reliability constraint.

Thus, it was shown that a SET assessment based on the input dependence analysis can be a useful assessment tool for optimization algorithms in the design synthesis of VLSI systems as well as for improving hardening techniques by providing an application-specific approach while fulfilling design constraints.

7

Conclusions and Outlook

7.1 Thesis Summary

Harsh environments such as in space and Earth's atmosphere present radiation particles that can interact within the components from the electronic systems. These radiation effects depend on the nature of the particle and the electronic circuit. In this thesis, we discussed the Single-Event Effects (SEEs), with a particular attention given to the Single-Event Transients (SETs). Initially, the SETs were not considered as dangerous to the circuit reliability as the data rupture caused by the Single-Event Upsets (SEUs). This was attributed particularly to the inherent ability of combination circuits in masking the radiation-induced transients, whether logically, electrically or temporally. However, in deeply-scaled technologies, the effectiveness of these masking effects is shown to be reduced and a higher impact of SET is observed in today's electronic technology. Thus, it is of utmost importance to carefully address not only the threat of SEU in memory elements, but also the SETs in combinational logic part of electronic systems. Accordingly, in this thesis, a prediction methodology based on simulation was proposed and used to assess the radiation robustness of digital designs. The methodology adopts the Monte Carlo tool, MC-Oracle and a SEE analyser developed in scripting language to perform the electrical simulations and the estimation of SET cross-section and pulse width distribution. The SET

characterization can be integrated either into a full-custom design methodology, in which the engineer can design the layout of the circuit and explore Radiation-Hardening-By-Design (RHBD) techniques and assess its hardening efficiency, or into a cell-based design flow to provide a reliability-driven synthesis.

Considering the RHBD approaches at layout-level, a deep analysis and comparison were provided for well-known techniques such as Gate Sizing (GS) and Transistor Stacking (TS). Though TS approach is widely used in Silicon-On-Insulator (SOI) technology, our analysis has shown that it can also be used in bulk technologies and provide reduction in the SET cross-section in some specific cases. However, due to the series connection of the stacked transistors, a weak restoring current is expected, leading to a wider SET pulse width distribution in the TF-based circuits. Additionally, the Transistor Folding (TF) layout technique was also investigated as a potential hardening technique. To address the drawback in layout area that the TF technique can bring in multiple-finger designs, we have proposed the Diffusion Splitting (DS) technique such that a better usage of the pre-defined tracks of logic cell layout design is achieved. For LET lower than $10 \text{ MeV.cm}^2/\text{mg}$, the hardening efficiency of the folded designs increases as the number of fingers is increased.

At circuit level, the impact of the technology mapping process in the logic synthesis was investigated. It was shown that complex-logic gates can increase the SET cross-section due to the suppression of the inherent logical masking effect of basic logic gates (NAND, NOR, INV...). Also, the intra-cell and inter-cell charge sharing mechanisms were studied in basic standard-cell gates to provide information on how to improve the logic synthesis when adopting a cell-based methodology. Given the importance of power autonomy in critical systems, the implications of adopting cell-based low-power techniques were also evaluated in terms of SET cross-section. For instance, the adoption of high-VT process devices, usually available in commercial Product Design Kits (PDKs), increases the cell SET cross-section due to the degradation in the driving strength capability compared to the regular- and low-VT process technology.

To conclude, based on the observed input dependence of the SEE sensitivity of digital circuits, two optimization techniques are proposed to increase their correspondent SEE robustness. First, a pin assignment based on the signal probability is proposed to improve the circuit reliability with no overhead in area. By identifying interchangeable signals, pin swapping can be used to reduce the SET sensitivity of a circuit. Also, by combining with the input dependence of RHBD techniques, signal probability and pin swapping can be used to improve the hardening efficiency and reduce SEE sensitivity, or even avoid misleading qualifications. And, second, a TMR block insertion optimization is proposed by identifying the input dependence of majority voter (MJV) architectures. Five MJV circuits exploiting both complex-gate layout and cell-based design were evaluated. Despite the reduced layout design, complex-gate voter architectures have shown, on average, a higher SET cross-section than the implementations using standard-cell gates. On the other hand, by evaluating the signal stimuli, a higher input dependence is observed for the standard-cell gate implementations (except for the BAN voter) due to the influence of logical masking effects in the 3-input logic gate in the output of the architecture. For instance, the 3-input gate in the output of the NAND and NOR architectures mask any SET in the 2-input gates when the input scenario is high and low logic values, respectively. Therefore, given the signal probability of a certain TMR insertion node, an optimization process can estimate which TMR architecture best provides the lower SET rate. In summary, signal probability can be used to propose a more application-specific TMR insertion optimization and consequently lower the hardening drawbacks.

7.2 Future Work

During the thesis, a test chip design was completely developed using a commercial 65nm bulk CMOS technology. The goal of the test chip was to provide experimental data to support our simulation results. Thus, as future work, the developed chip can be used to perform radiation testing in different facilities. The chip contains 18 blocks of benchmark circuits: 10

majority voter architectures, 4 circuits to study the complex-logic gate layout effects and 4 circuits to study the transistor folding layout effects. A shift register structure adopting LEAP-DICE flip-flops was designed and used as reading circuitry to the output signal of each benchmark block circuit.

Another future work would be to analyze the effectiveness of the hardening techniques studied in this thesis when applied in more advanced technology devices, such as the three-dimensional FinFET structures. Due to the fin structure, the sizing of FinFET is obtained by the number of fins, a phenomenon known as width quantization. Also, due to the strain engineering, PMOS and NMOS devices show a similar driving capability, therefore the same number of fins are used for each device type. Given the particularities of this technology, new studies should be addressed to verify the effectiveness of well-known RHBD techniques.

7.3 List of Publications

During this Ph.D. project, the results were disseminated through several publications and presentations in peer-reviewed journals and international conferences. In summary, 7 first-authored publications and 3 co-authored publications compose the total number of scientific contributions. The list of publications can be found below.

First-authored publications:

1. AGUIAR, Y.Q., WROBEL, F., AUTRAN, J-L., LEROUX, P., SAIGNÉ, F., TOUBOUL, A. D., POUGET, V., Analysis of the charge sharing effect in the SET sensitivity of bulk 45 nm standard cell layouts under heavy ions, **Microelectronics Reliability** 88-90, September 2018, pp. 920-924. DOI: 10.1016/j.microrel.2018.07.018
2. AGUIAR, Y.Q., WROBEL, F., AUTRAN, J-L., LEROUX, P., SAIGNÉ, F., TOUBOUL, A. D., POUGET, V., Impact of Complex-Logic Cell Layout on the Single-Event Transient Sensitivity, **IEEE Transactions on Nuclear Science**, 2019. DOI: 10.1109/TNS.2019.2918077

3. AGUIAR, Y.Q., WROBEL, F., GUAGLIARDO, S., AUTRAN, J-L., LEROUX, P., SAIGNÉ, F., TOUBOUL, A. D., POUGET, V., Radiation Hardening Efficiency of Gate Sizing and Transistor Stacking based on Standard Cells, **Microelectronics Reliability**, 2019. DOI: 10.1016/j.microrel.2019.113457
4. AGUIAR, Y.Q., WROBEL, F., AUTRAN, J-L., LEROUX, P., SAIGNÉ, F., POUGET, V., TOUBOUL, A. D., Mitigation and Predictive Assessment of SET Immunity of Digital Logic Circuits for Space Missions, **Aerospace**, 2020. DOI: 10.3390/aerospace7020012
5. AGUIAR, Y.Q., WROBEL, F., AUTRAN, J-L., KASTENSMIDT, F., LEROUX, P., SAIGNÉ, F., POUGET, V., TOUBOUL, A. D., Exploiting Transistor Folding Layout as RHBD Technique against Single-Event Transients, **IEEE Transactions on Nuclear Science**, 2020. DOI: 10.1109/TNS.2020.3003166
6. AGUIAR, Y. Q., WROBEL, F., AUTRAN, J-L., LEROUX, P., SAIGNÉ, F., POUGET, V., TOUBOUL, A. D., Reliability-driven pin assignment optimization to improve in-orbit soft-error rate, **Microelectronics Reliability**, 2020. DOI: 10.1016/j.microrel.2020.113885
7. AGUIAR, Y. Q., WROBEL, F., AUTRAN, J-L., LEROUX, P., SAIGNÉ, F., POUGET, V., TOUBOUL, A. D., Design Exploration of Majority Voter Architectures based on the Signal Probability for TMR Strategy Optimization in Space Applications, **Microelectronics Reliability**, 2020. DOI: 10.1016/j.microrel.2020.113877

Co-authored publications:

1. GUAGLIARDO, S., WROBEL, F., AGUIAR, Y. Q., AUTRAN, J-L., LEROUX, P., SAIGNÉ, F., TOUBOUL, A. D., POUGET, V., Single Event Latchup Cross Section Calculation from TCAD Simulations – Effect of the Doping Profiles and Anode to Cathode Spacing, Proceedings of Radiation Effects on Components and Systems (RADECS) Conference, 2019, Montpellier.

2. GUAGLIARDO, S., WROBEL, F., AGUIAR, Y. Q., AUTRAN, J-L., LEROUX, P., SAIGNÉ, F., TOUBOUL, A. D., POUGET, V., Effect of Temperature on Single Event Latchup Sensitivity, Proceedings of Design Technology of Integrated Systems in Nanoscale Era (DTIS) Conference, 2020, Marrakech.
3. SCHVITZ, R., AGUIAR, Y. Q., WROBEL, F., AUTRAN, J-L., DA ROSA Jr., L. S, BUTZEN, P. F., Comparing Analytical and Monte-Carlo-based Simulation Methods for Logic Gates SET Sensitivity Evaluation, **Microelectronics Reliability**, 2020.

Appendix A

Outil de prédictions et durcissement par design pour les SEU et SET

A.1 Introduction et Motivation

En raison des environnements de rayonnement concernés dans l'aviation et les missions spatiales, les systèmes électroniques sont sensibles aux interactions des particules et aux effets qui en découlent. Ces effets peuvent avoir un caractère cumulatif, qui dépend de la durée d'exposition dans un environnement radiatif, ou même singulier, lorsqu'une seule particule suffit à développer un effet permanent ou transitoire sur le circuit. Dans cette thèse, les effets d'événement singulier, *Single-Event Effects* (SEE), ont été au centre de l'étude, en particulier les aléas logiques, aussi connu en anglais sous le nom de *Single-Event Upset* (SEU) et les événements singuliers transitoires, ou *Single-Event Transient* (SET).

Originellement, les premières études sur la fiabilité des circuits sous l'effet des radiations ont été menées pour des applications militaires ou spatiales. En 1962, le travail développé par Wallmark et Marcus [2] a été la première étude à prédire que les rayonnements cosmiques pourraient devenir une menace pour la conception des circuits à mesure que la technologie

est réduite. Et ce n'est que plus tard, en 1975, que Binder et al. [3] a pu identifier des anomalies dans le stockage des bits des circuits de bascule à l'intérieur d'un satellite et les attribuer aux effets du rayonnement cosmique. Ces premières études se sont concentrées sur les effets des rayonnements sur les circuits de stockage, comme les mémoires SRAM. En raison des effets de masquage intrinsèques aux circuits combinatoires dans les conceptions numériques, le SET a été considéré comme non pertinent par rapport à la rupture de données causée par les SEU. Il existe trois principaux effets de masquage inhérents aux circuits numériques: i) le masquage électrique, dans lequel l'impulsion transitoire ne peut pas se propager à travers un chemin logique en raison des pertes électriques et de l'atténuation de son amplitude; ii) le masquage logique, dans lequel un SET sera masqué en raison de la dépendance logique de chaque signal numérique; et iii) le masquage de fenêtre de verrouillage ou masquage temporel, dans lequel l'impulsion SET est masquée par la fenêtre de verrouillage d'un élément de mémoire, c'est-à-dire que le SET n'atteint pas l'élément de mémoire lors de son opération de mode d'écriture. Cependant, le dimensionnement des transistors, la réduction de la profondeur du chemin logique des données et l'augmentation des fréquences de fonctionnement ont atténué les effets de masquage électrique, logique et temporel des circuits logiques aux nœuds de technologie avancée [10–13]. En conséquence, la menace associée aux SET doit être soigneusement traitée en même temps que la caractérisation du SEU dans les systèmes électroniques des applications spatiales, avioniques et même pour les applications au sol.

Dans ce contexte, plusieurs travaux ont été proposés pour développer des techniques pour augmenter la fiabilité des circuits depuis le début de la phase de conception. Ces techniques de durcissement peuvent être adoptées au niveau de processus, *Radiation-Hardening-by-Process* (RHBP), ou au niveau de conception, *Radiation-Hardening-by-Design* (RHBD). Les modifications du processus de fabrication des circuits telles que la variation des profils de dopage, la technologie des substrats et l'utilisation de différents matériaux sont des exemples de techniques RHBP bien connues. Néanmoins, au-delà de son coût plus élevé, les techniques RHBP sont généralement en retard de

plusieurs générations sur la technologie CMOS de pointe, ce qui traduit par des performances de faible qualité. D'un autre côté, les techniques RHBD se sont avérées efficaces pour fournir une dureté contre les effets des radiations avec les avantages des technologies hautement intégrées [70]. Les techniques RHBD peuvent être adoptées du niveau physique visant à réduire la collecte de charge induite par rayonnement à des techniques au niveau du système où l'objectif principal est de masquer les erreurs et d'éviter une défaillance du système.

Le processus de caractérisation des circuits sous les effets des rayonnements est généralement basé sur des tests expérimentaux. Toutefois, la nécessité d'adopter des simulations pour étudier les mécanismes fondamentaux induits par les rayonnements et aussi d'améliorer les méthodologies de test a suscité un intérêt accru pour le développement de méthodologies de caractérisation SEE basées sur des outils de simulation. En conséquence, cette thèse vise à proposer une méthodologie générale basée sur une chaîne de simulation numérique complète basée sur une approche multi-physique et multi-échelle pour prédire la susceptibilité SEE des composants électroniques et, en utilisant cette méthodologie, fournir une analyse de différentes techniques de durcissement par design (RHBD) au niveau du layout physique et du circuit.

A.2 Méthodologie de Prédiction

L'utilisation de la modélisation et de la simulation a toujours été présente dans l'étude des phénomènes physiques, notamment dans le domaine de l'électronique pour étudier le comportement des transistors MOS [38, 39]. Pour évaluer avec précision l'immunité SEE des circuits numériques, il est fortement recommandé d'adopter une méthodologie multi-échelle et multi-physique en raison de la pluralité d'effets complexes impliqués au niveau du silicium et du circuit [56, 42]. Différentes approches prenant en compte les aspects de la physique des interactions des particules à la conception de la configuration du circuit sont explorées dans différents codes, comme indiqué dans [47]. Un flux de conception personnalisé complet simplifié avec

la méthodologie de caractérisation SEE utilisant l'outil de prédiction MC-Oracle [43] est illustré dans la Figure A.1. La caractérisation SEE proposée est divisée en deux étapes principales : premièrement, visant à construire une base de données avec les courants SET, l'outil MC-Oracle est utilisé pour effectuer la simulation du transport de particules et de la collecte de charges dans les zones de collecte du circuit ; deuxièmement, un analyseur de SET est responsable de la campagne d'injection SPICE utilisant la base de données avec les courants SET fournie par MC-Oracle. Les principales entrées de la caractérisation du SET sont : le modèle technologique, la spécification de l'environnement de rayonnement, le dessin physique (le *layout* du circuit qui est décrit dans le format GDSII) et la description *netlist* du circuit (la liste de composants et ses connexions).

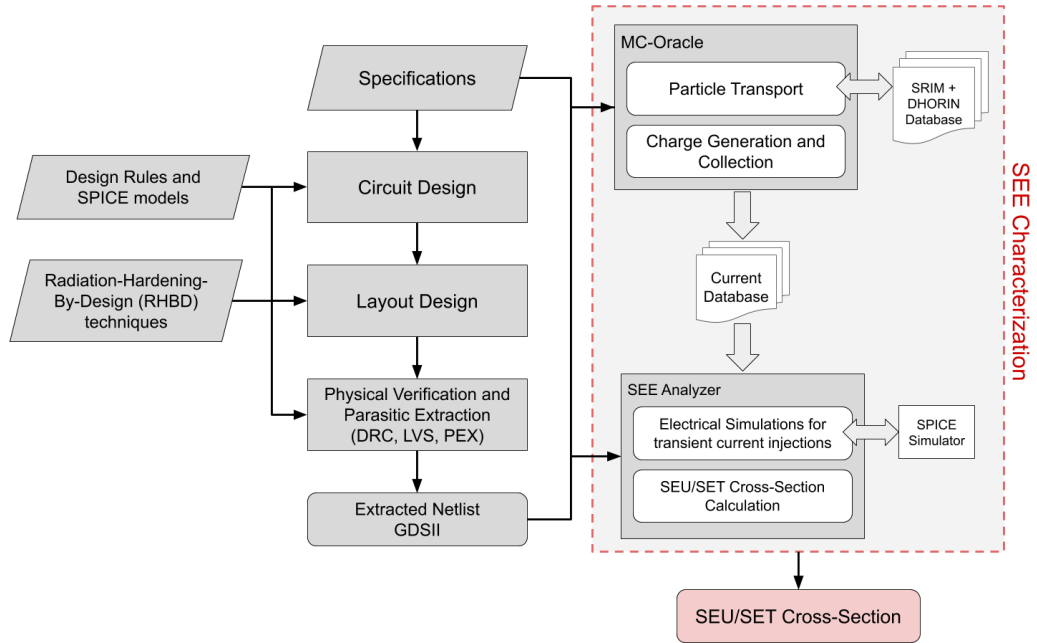


Figure A.1: Chaîne de simulation proposée comme méthodologie de prédiction de SEE

Pour la mesure de la section efficace et de la largeur d'impulsion du SET, seules les impulsions transitoires dont le pic de tension est supérieur à la moitié de la tension d'alimentation sont prises en compte, mais cela peut être facilement adapté aux besoins de l'utilisateur. Différentes tech-

niques de durcissement peuvent être adoptées pour éviter que des systèmes électroniques critiques, tels que les vaisseaux spatiaux et les systèmes de contrôle avionique, ne tombent en panne à cause de l'apparition de SEE. En conséquence, la méthodologie de caractérisation prédictive SEE proposée permet d'étudier l'efficacité des techniques de durcissement aux rayonnement au niveau de la conception physique et du circuit.

A.3 Résultats

A.3.1 Durcissement par design (RHBD) au niveau du layout physique

Dans le chapitre 4 de cette thèse, trois techniques de durcissement par design (RHBD) au niveau du layout physique ont été évaluées dans différents circuits logiques. Premièrement, le dimensionnement de grilles (*Gate Sizing*, GS) et l'empilement des transistors (*Transistor Stacking*, TS) ont été étudiés sur une bibliothèque de cellules, « *standard-cell library* ». L'idée était d'étudier comment ces bibliothèques, qui sont largement utilisées dans l'industrie des semi-conducteurs, peuvent être utilisées pour maximiser la fiabilité des systèmes électroniques sous les effets des rayonnements. Les résultats ont montré que les deux techniques sont capables de fournir une réduction sur la section efficace au SET. La Figure A.2 montre la courbe de section efficace au SET pour les différentes variantes du circuit NOR. Ce circuit a montré les plus grandes améliorations même si l'empilement de transistors peut augmenter la largeur d'impulsion SET maximale à $2\times$ plus large que la conception originale, sans aucun durcissement. Le GS montre le meilleur compromis entre la surface occupée, la puissance consommée et la fiabilité. Cependant, l'efficacité de durcissement de l'empilement de transistors dépend fortement du signal d'entrée de la grille. Ceci reflète le fait que, dans la structure d'empilement, les transistors placés loin de la sortie de la grille seront probablement incapables d'induire une impulsion SET dans la sortie en raison de l'effet de masquage électrique. Ainsi, selon l'application, le TS peut éventuellement surpasser le GS.

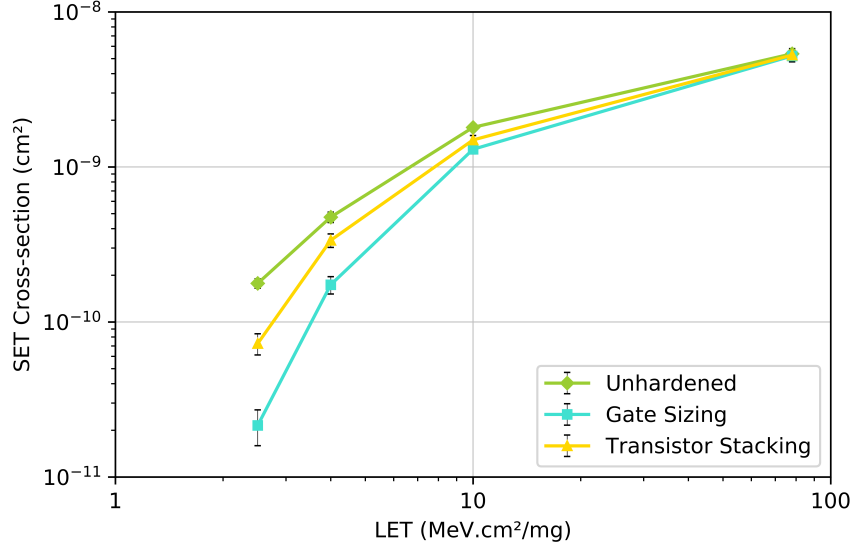


Figure A.2: Courbes de section efficace au SET pour le circuit NOR originale et en utilisant des techniques de durcissement aux rayonnements.

Après avoir compris les implications de l'adoption du GS et du TS, l'efficacité du layout de transistors repliés, autrement appelés transistors multi-doigts, pour améliorer l'immunité des circuits numériques aux SET a été évaluée. L'objectif était de vérifier comment des transistors repliés peuvent améliorer la fiabilité des portes logiques qui sont les principaux composants d'une bibliothèque de cellules. Les résultats ont indiqué que les designs repliés peuvent offrir une section efficace de SET inférieure ainsi qu'un LET seuil plus élevé que celui observé pour les designs non repliés. Dans la Figure A.3, la section efficace au SET pour des particules avec un LET de $5.43 \text{ MeV.cm}^2/\text{mg}$ est montrée, prenant en compte les différentes combinaisons possibles à l'entrée du circuit NAND. La technique de fractionnement de la diffusion, le « *diffusion splitting* » (DS), a été proposée pour réduire l'augmentation de la surface du circuit. Dans cette technique, la diffusion active du transistor est divisée en deux bandes et placées verticalement alignées l'une dans l'autre. En plus de réduire la surface occupée, la séparation de la diffusion peut également améliorer la section efficace au SET en fonction de la topologie du circuit, du signal d'entrée et du LET

de la particule. On peut vérifier ces avantages pour le circuit NAND F4S (replié quatre fois avec le fractionnement de la diffusion) dans la Figure A.3. Cependant, dans l'ensemble, le circuit NAND avec des transistors repliés deux fois (F2) s'est révélé être toujours le plus robuste. Des informations plus détaillées sur ces résultats sont disponibles dans le texte intégral de la thèse.

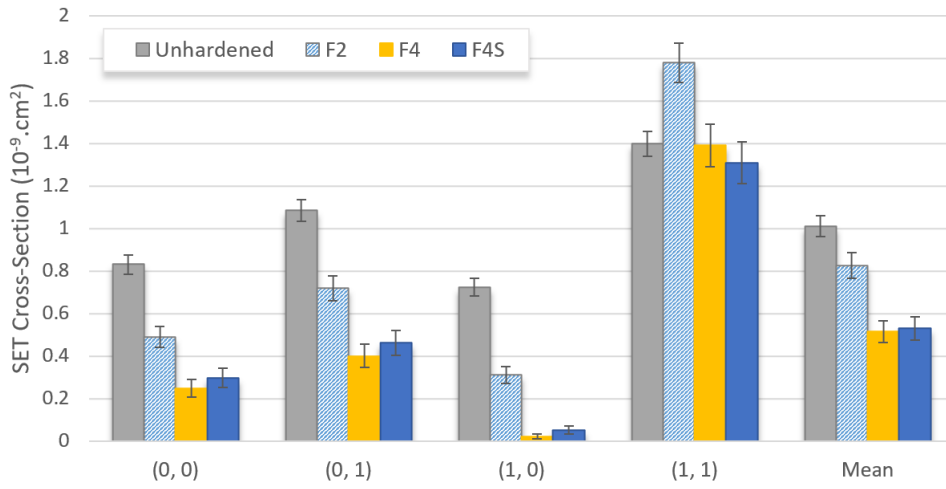


Figure A.3: Section efficace au SET du circuit NAND originale et avec transistors repliés ($LET = 5.43 \text{ MeV.cm}^2/mg$).

En raison de la forte dépendance au signal d'entrée de ces techniques, il a également été proposé d'adopter des conceptions asymétriques, c'est-à-dire d'appliquer les techniques de durcissement uniquement dans les dispositifs PMOS ou NMOS, en fonction du pire scénario d'entrée de la porte logique. Également, les taux SET ont été calculés pour les orbites LEO et ISS. Lorsque le taux SET n'est calculé que pour les ions lourds, toutes les conceptions avec des transistors repliés ont fourni un taux plus faible que les designs non repliés. Cependant, les protons dominent les taux de SEE sur les orbites LEO et ISS. Lorsque les protons sont pris en compte, les conceptions symétriques et asymétriques avec des transistors repliés deux fois (F2) et la conception asymétrique à 4 doigts (F4) avec DS sont les circuits les plus durcis.

A.3.2 Durcissement par design (RHBD) au niveau du circuit

Dans le chapitre 5, l'évaluation des techniques au niveau des circuits est présentée. Tout d'abord, une discussion sur l'importance de la synthèse axée sur la fiabilité dans le flux de conception VLSI est mise en évidence. L'applicabilité de la caractérisation de prédiction SEE proposée pour soutenir les algorithmes de synthèse ciblant la résilience aux SEE est vérifiée.

Compte tenu de la dépendance d'entrée de la sensibilité SEE des circuits logiques, une méthodologie d'optimisation est proposée pour améliorer la résilience globale du circuit grâce à un échange de broches dans les circuits logiques, en fonction de la probabilité du signal. La dépendance du signal d'entrée est attribuée aux différentes capacités de conduite des transistors et à l'influence du layout physique sur la robustesse du circuit au SET. Comme ces mécanismes sont dépendants du LET de la particule, la relation entre le signal d'entrée et la section efficace au SET est également dépendante du LET. L'impact de l'échange de broches dans les circuits logiques en fonction de la probabilité de ses signaux d'entrée est montré dans la Figure A.4.

Pour différents scénarios de probabilité de signal, le taux de SET change en conséquence. En considérant les circuits à deux entrées, le signal avec la probabilité la plus faible doit être affecté à l'entrée B pour le circuit NAND et à l'entrée A pour les circuits NOR et XOR. Pour les circuits à trois entrées, différentes conclusions peuvent être tirées en fonction de la probabilité du signal de l'entrée dominant, c'est-à-dire qui contrôle la sortie du circuit et cela ne peut pas être permuté. Cette technique d'optimisation ne fournit aucune surcharge de surface et peut être utilisée avec d'autres techniques de durcissement. De plus, cela n'a aucun impact sur le placement des cellules et le routage des connexions est affecté de manière minimale et locale dans le circuit.

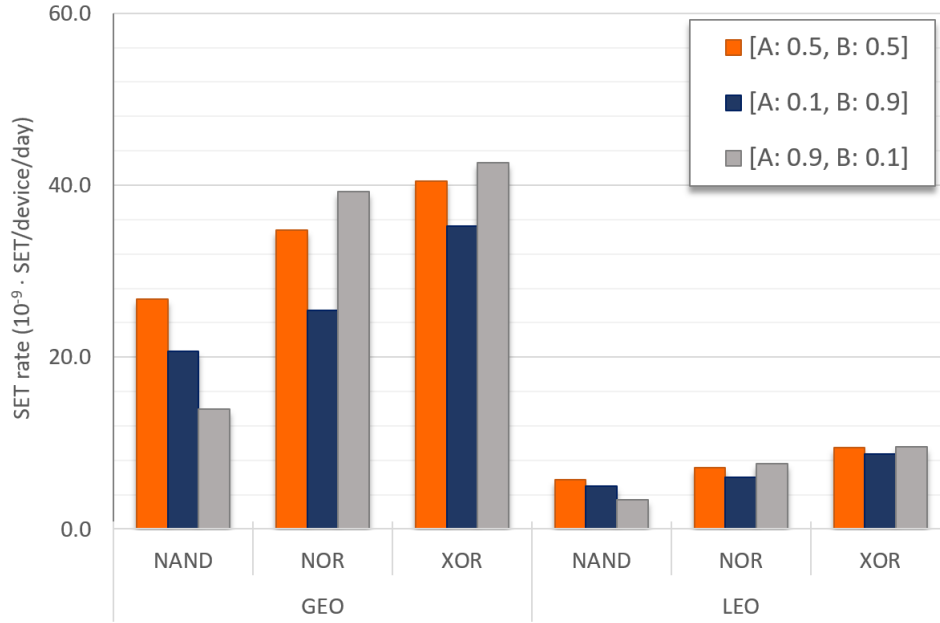


Figure A.4: Taux SET pour le circuit NAND, NOR et XOR sur l'orbite géostationnaire (GEO), à 35784 km, et l'orbite de la station spatiale internationale (ISS), 400 km, 51.64°.

A.3.3 Amélioration de l'efficacité des techniques de durcissement

Dans la première partie de cette thèse, la dépendance au signal d'entrée de la sensibilité des circuits logiques numériques au rayonnement était vérifiée dans les résultats. En conséquence, une affectation des broches a été proposée pour améliorer la fiabilité des circuits logiques basés sur des cellules standard contre les effets du rayonnement. Cependant, l'efficacité des techniques RHBD bien connues telles que le dimensionnement de grille (GS) et l'empilement de transistors (TS) ont également montré une forte dépendance d'entrée. Ainsi, la probabilité de signal peut également être utilisée pour améliorer la robustesse au rayonnement des circuits intégrés en sélectionnant plus précisément la meilleure technique de durcissement pour une application donnée.

Dans ce contexte, l'estimation de la probabilité du signal a été utilisée dans le chapitre 6 pour évaluer l'efficacité de durcissement des circuits

adoptant les techniques GS et TS. La section efficace au SET pour le circuit NAND est montrée dans la Figure A.5 pour cinq scénarios de probabilité de signal. Les résultats ont montré que les améliorations peuvent atteindre jusqu'à environ 80% de robustesse au SET. Il a également été montré qu'en ne tenant pas compte du signal d'entrée, les conceptions durcies avec une technique RHBD peuvent montrer une section efficace au SET plus élevée que celle non durcie. Ainsi, en plus d'améliorer l'efficacité des techniques de durcissement aux rayonnements, l'approche d'affectation des broches proposée basée sur la probabilité du signal fournit une analyse de durcissement plus spécifique à l'application. Par conséquent, les techniques de durcissement ou la sélection de circuits robustes peuvent être appliquées plus efficacement et éviter des qualifications trompeuses.

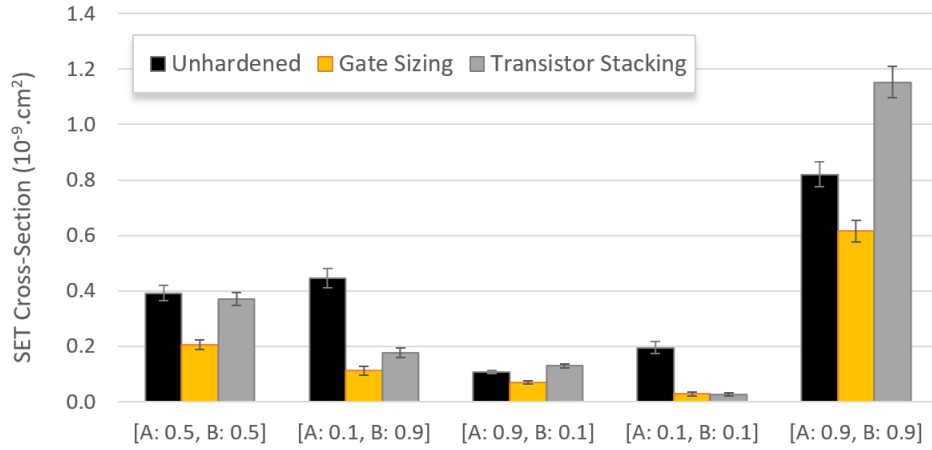


Figure A.5: Section efficace au SET pour le circuit NAND (versions non durci, dimensionnement de grille et empilement de transistors) sous particules avec LET de $3,89 \text{ MeV.cm}^2/\text{mg}$ en considérant cinq scénarios de probabilité de signal.

De plus, il a été montré que l'estimation de la probabilité du signal peut également être utilisée dans l'optimisation des techniques de redondance de hardware, telles que la triple redondance modulaire, *Triple Modular Redundancy* (TMR). Dans ce cas, une caractérisation SEE des architectures des électeurs majoritaires (MJV) peut fournir des informations sur la dépendance d'entrée du circuit. De cette manière, avec l'estimation de la proba-

bilité du signal des nœuds critiques dans un circuit intégré, une optimisation de l'insertion de l'électeur majoritaire peut être adoptée en tenant compte de la dépendance d'entrée de chaque architecture.

Dans cette thèse, cinq architectures d'électeurs majoritaires distinctes (CMOS1, CMOS2, NAND, NOR et BAN) ont été conçues et caractérisées sous des faisceaux d'ions lourds et différentes probabilités de signaux d'entrée. Malgré la surface réduite, les architectures de voteurs à porte complexe ont montré, en moyenne, une section efficace au SET plus élevée que les implémentations utilisant des cellules standard de portes logiques de base. Comme toutes les architectures ont été conçues pour fournir une capacité de conduite comparable, l'augmentation des transistors empilés dans les conceptions à logique complexe augmente les zones de drain de collecte de charge et, par conséquent, augmente la section efficace au SET du circuit. Ainsi, viser un inconvénient plus faible dans la surface de conception compromettra la fiabilité du circuit. En évaluant les stimuli de signal, une dépendance d'entrée plus élevée est observée pour les architectures de portes logiques de base (sauf pour le voteur BAN) en raison de l'influence des effets de masquage logique. Par exemple, la porte à 3 entrées dans la sortie des architectures NAND et NOR masque toutes les impulsions SET provenant des portes à 2 entrées dans le premier étage de l'architecture, lorsque le signal d'entrée est une valeur logique élevée et une valeur logique faible, respectivement. Pour surmonter l'effet de masquage logique et induire un SET dans la sortie des architectures NAND et NOR, l'incidence de la particule énergétique doit déposer suffisamment d'énergie dans les trois répliques des schémas TMR.

Pour vérifier l'impact d'un environnement de rayonnement, la figure A.6 présente les taux SET estimés pour trois probabilités de signal ($p = 0, 1, p = 0,5$ et $p = 0,9$) et deux orbites différentes (GEO et ISS / LEO). Deux tendances distinctes peuvent être observées: l'augmentation et la réduction du taux SET lorsque la probabilité du signal augmente. Différent des architectures CMOS1, CMOS2, NOR et BAN, le voteur NAND est la seule conception qui montre une diminution du taux SET lorsque la probabilité du signal augmente. Ceci est clairement attribué à la section efficace au SET inférieure pour la configuration d'entrée de valeur logique 1 en raison

de l'effet de masquage logique.

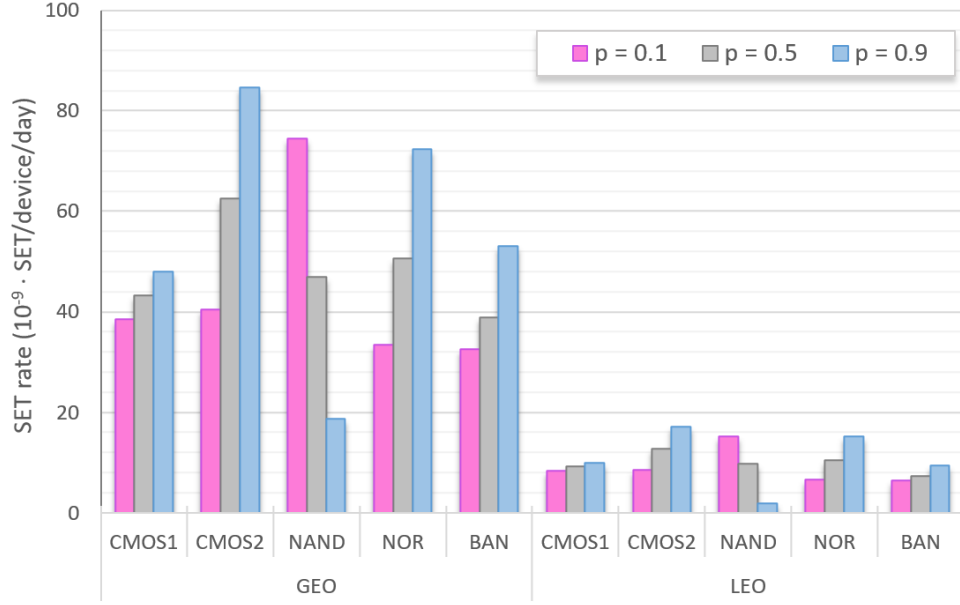


Figure A.6: Taux SET calculé pour l'orbite géostationnaire (GEO), 35784 km, et l'orbite de la station spatiale internationale (ISS), à 400 km, 51,64 °. La probabilité de trois signaux est considérée : $p = 0.1$, $p = 0.5$ et $p = 0.9$.

A.3.4 Conclusions

La fiabilité des circuits électroniques est sujette à des dommages physiques ou à des défaillances fonctionnelles en raison de la présence du rayonnement atmosphérique ou spatial. L'interaction des particules dans le silicium peut entraîner des effets permanents ou transitoires tels que les effets d'événement singulier (SEE). En raison des effets de masquage intrinsèques des circuits combinatoires dans les conceptions numériques, les événements singuliers transitoires (SET) ont été considérés comme non pertinents par rapport à la rupture de données causée par les aléas logiques (SEU). Cependant, l'importance de considérer les SETs dans les circuits VLSI (*Very-Large-System-Integration*) augmente étant donnée la réduction des dimensions des transistors et de la profondeur du chemin de données logique dans les technologies avancées. En conséquence, la menace associée aux SET doit être

soigneusement traitée en même temps que la caractérisation du SEU dans les systèmes électroniques des applications spatiales, avioniques et même pour les applications au sol. De plus, pour augmenter la fiabilité des systèmes, des techniques de durcissement peuvent être adoptées dans les niveaux de processus ou de conception. Le processus de caractérisation est généralement orienté vers les tests expérimentaux, mais la nécessité d'adopter des simulations de modélisation pour étudier les effets fondamentaux des rayonnements et améliorer les méthodologies de test a conduit à un intérêt accru pour le développement de méthodologies de caractérisation des SEEs basées sur des outils de simulation. En conséquence, cette thèse a proposé une chaîne de simulation numérique complète basée sur une approche multi-physique et multi-échelle pour caractériser les composants électroniques contre les effets SEU / SET. De plus, des techniques de durcissement par design (RHBD) ont été évaluées et proposées au niveau du layout physique et du circuit. La conception du layout physique influence les mécanismes de génération de SEE induits par une collision des particules. Par conséquent, les techniques de durcissement sont largement utilisées au niveau du layout pour réduire le processus de collecte des charges. Au-delà de l'analyse du dimensionnement et de l'empilage des transistors, ce travail a proposé l'utilisation du layout de transistors repliés ainsi que la technique de fractionnement de la diffusion, le « *diffusion splitting* » (DS). Les résultats ont indiqué que les designs repliés peuvent offrir une section efficace au SET inférieure ainsi qu'un LET seuil plus élevé que celui observé pour les designs non repliés. Au niveau des circuits, les implications de la synthèse logique des conceptions à base de cellules sont étudiées. En outre, étant donné la dépendance des techniques RHBD par rapport au signal d'entrée, la probabilité du signal est proposée comme une approche de durcissement spécifique à l'application afin d'améliorer l'efficacité du durcissement tout en réduisant les inconvénients de conception et d'éviter les qualifications trompeuses. Par exemple, une optimisation de l'affectation des broches qui vise les effets SET peut permettre de réduire le taux global de SET. De plus, les méthodologies d'insertion sélective de blocs TMR (*Triple Modular Redundancy*) peuvent être optimisées en fonction de la probabilité de signal des nœuds critiques et de la dépen-

dance d'entrée de la sensibilité des architectures des voteurs majoritaires. Enfin, cette thèse a montré que l'évaluation de la sensibilité aux SEE basée sur l'analyse de la dépendance d'entrée peut être un outil de caractérisation utile pour les algorithmes d'optimisation dans la synthèse de conception des systèmes de circuits intégrés ainsi que pour améliorer les techniques de durcissement en fournissant une approche plus spécifique à l'application tout en respectant les contraintes de conception.

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