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Coupled radiation and aging effects on wide bandgap power devices

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THÈSE POUR OBTENIR LE GRADE DE DOCTEUR DE L'UNIVERSITÉ DE MONTPELLIER

En Electronique

École doctorale I2S – Information Structures et Systèmes

IES – Institut d'Electronique et des Systèmes

Coupled Radiation and Aging Effects on Wide Bandgap Power Devices

Présentée par Kimmo NISKANEN

Le 26/11/2020

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Introduction

Electronic devices are present practically everywhere in our modern society. Nowadays, in addition to electronic devices which are present in our everyday life, such as handheld devices and household electronics, new devices are designed to be used in vast number of applications in industry, transportation and medical care. To supply necessary electrical power to the electronic systems, power electronics is required in each of the aforementioned applications.

In order to ensure and control the operation of such systems, it is necessary to assess the behaviour and reliability of electronic power devices and systems in their operation environments. Depending on the application, electronic devices face different types of stresses which must be taken into account, such as thermal, mechanical, radiative and, as a common stressor for all electronics, electrical stress.

Environments in which radiation is of concern for reliable operation of electronics include space, nuclear power plants and particle accelerators. Among those environments, atmospheric neutrons pose a threat for avionics as well as for ground level transportation applications, such as electric cars and trains.

Semiconductor power devices such as power diodes and power transistors are in the core of the power supply systems. Historically, silicon (Si) has been the dominant semiconductor material in power electronics. Due to trends of increasing efficiency and decreasing size of the electronic components and systems, Si has reached its performance limits. Therefore, there is a need for designing new materials as a replacement for Si in power electronic devices.

In recent years, the power electronics industry has been rapidly evolving thanks to wide bandgap (WBG) semiconductor materials such as silicon carbide and gallium nitride. Even though, WBG devices are starting to become more commercially available, they are still relatively recent materials in power semiconductor devices. There are still some technological barriers, which need to be overcome in order to ensure a reliable operation throughout their lifetime in harsh environments. Realized within the RADSAGA project, (RADiation and Reliability Challenges for Electronics used in Space, Aviation, Ground and Accelerators), the objective of my study is the determination of the test methodology for radiation and aging effects on commercial-off-the-shelf (COTS) WBG power devices. RADSAGA is an Innovative Training Network part of European Union's Horizon 2020 research and innovation program under the Marie-Sklodowska-Curie grant.

In this context, this thesis manuscript has five chapters. Power electronic device technologies and their applications are presented and reviewed in Chapter 1. After introducing the target applications as well as technological differences and similarities between Si- and WBG-based devices, more specific application environments with radiation are presented. In Chapter 2, the different radiation effects exhibited by electronics are described, including Total Ionizing Dose (TID), Displacement Damage (DD) and Single-Event Effects (SEE) putting more weight on SEE on WBG power devices. The end of the chapter

dedicated to aging effects on power devices.

In Chapter 3 the conducted experimental studies are presented and analysed focusing mostly on atmospheric neutron-induced single event effects on silicon carbide power metal-oxide-semiconductor field-effect transistor (MOSFET) coupled with electrical aging experiments. Finally, the impact of degraded device at system level is studied.

Chapter 1

From silicon to wide bandgap power devices

1.1 Material properties

The largest portion of the power losses in power electronics is dissipated in the semiconductor parts. Silicon material has come to its limits regarding critical electric field, operating temperature and switching frequency. In order to increase power conversion efficiency, reduce the size of the power systems and increase their robustness in harsh environments, new candidates for taking over silicon are required. Nowadays, the most attractive candidates for such task are wide bandgap (WBG) materials, such as silicon carbide (SiC) and gallium nitride (GaN), which show the best trade-off between material properties, commercial availability of the starting materials for the manufacturing processes and the maturity of their technological processes [1]. The comparison of the material properties between Si, SiC and GaN are presented in Figure 1.1.

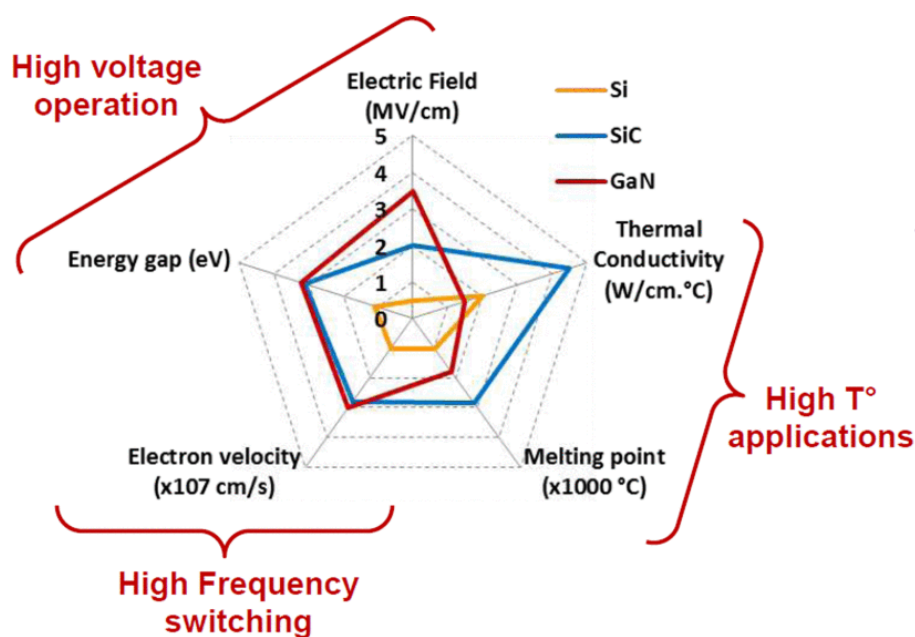


Figure 1.1: Material properties comparison between Si, SiC, and GaN [1]

From the material properties point of view, WBG power devices have several advantages over Si-based devices. High critical field allows high breakdown voltage or smaller size of the device structure for same voltage rating. High mobility allows high frequency switching and lower on-state resistance. This, in turn results in lower power consumption since the power loss in on-state is lower due to low resistance as well as due to shorter time when device is in high-resistance state between on- and off-state [1, 2].

Capability of WBG devices operating at higher temperature and higher thermal conductivity allows higher current density and therefore smaller size of the device. Due to higher thermal conductivity and higher melting point, less complex and less massive cooling systems are required when operating such devices. However, even if the critical material properties of WBG materials are superior over Si, it is not enough to fully replace Si in high power applications. Technological challenges related to packaging, interconnects and material uniformity has to be taken into account when manufacturing devices using these materials. For example, increased thermal performance of the semiconductor material allows higher operating temperature which can cause issues on the packaging and interconnects reliability [1, 3].

1.2 Semiconductor power device technologies

1.2.1 Si-based power devices

Silicon has established itself as a standard semiconductor material used in electronic components in large variety of technologies. Until today, power electronics is no exception. Over the years, technology has matured and as mentioned earlier, the limitations related to performance improvements, arise from material limitations rather than technological issues.

The most fundamental challenge in power semiconductor device design is to obtain a high breakdown voltage while having low forward voltage drop and on-resistance (R_{ON}). Obtaining a high breakdown voltage requires low doping concentration which results in high resistance of the semiconductor. Next, the most common semiconductor power diode and transistor technologies are introduced.

Diodes

The two most common power diode structures used in power applications are PN-diode (also known as PIN-diode) and Schottky barrier diode (SBD) (Figure 1.2). Compared to conventional PN-junction diode, PN-diode for power applications contains lightly doped n- drift region between the p+ region and heavily doped n+ region. Such lightly doped region is almost intrinsic and hence the name PIN-diode, where I stands for intrinsic. Such layer allows higher reverse blocking voltage compared to conventional PN-structure. However, the on-state resistance of the diode is thus increased and therefore the heat dissipation has to be correctly managed in such devices.

Instead of pn-junction, Schottky barrier diode (SBD) has a metal-semiconductor junction which results in narrower depletion region in blocking mode and lower forward voltage drop compared to conventional p-n-junction diode. Other advantages of SBD include low capacitance and fast recovery time making it suitable for high speed switching applications [4].

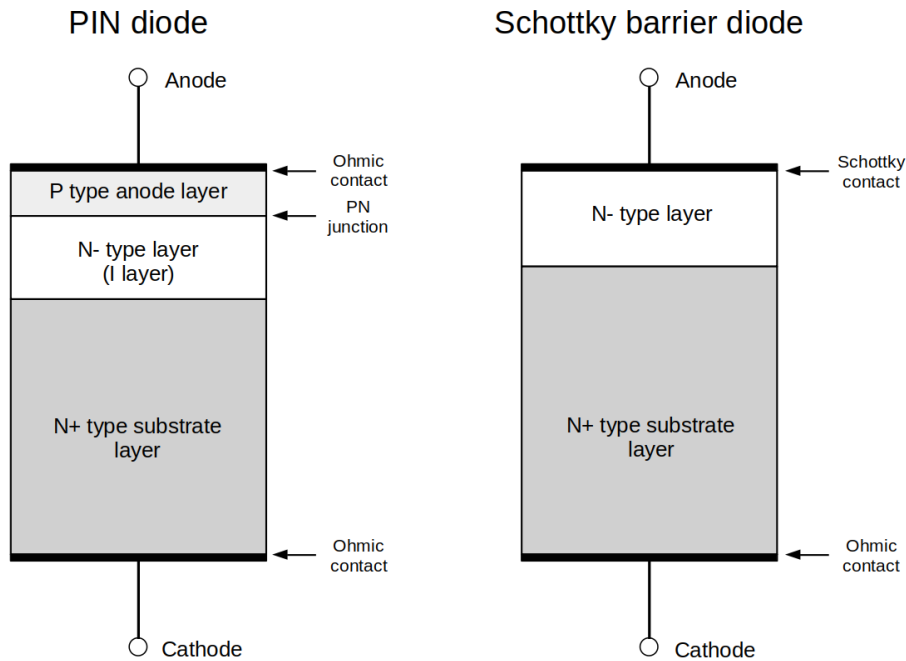


Figure 1.2: Cross section of a PIN-diode (left) and a Schottky barrier diode (right).

MOSFET

Dealing with medium or high voltage electronics, most power MOSFETs feature a multicellular vertical structure with source and drain on the opposite sides of the wafer in order to support higher current and voltage blocking capability. Current flowing between the drain and the source is controlled by modulating the surface conductivity in the p-body region under the gate, which is controlled by the gate-to-source voltage [4].

Power MOSFETs contain parasitic bipolar junction transistor (BJT) structure, where the p-body serves as base, source as emitter and drain as collector (Figure 1.3). This BJT should be kept off in order to avoid unwanted current when MOSFET is in off-state. The parasitic BJT is normally off since p-body and n+-source are shorted with source terminal. This parasitic structure plays a role in radiation sensitivity of the device which will be discussed in the next chapter. Power MOSFET structure contains also intrinsic pn-junction between body and drain, called as body diode. Such structure is useful in applications where reverse drain current is needed such as in inverter circuits. Cross-sectional layout image of vertical power DMOSFET with highlighted parasitic structures are presented in Figure 1.3. The term DMOSFET derives from “double-diffused” MOSFET in which the n+ source and p-body regions are formed by diffusion through the same mask opening during the manufacturing process [5].

Another used power MOSFET implementation is UMOSFET (also known as “trench MOSFET”). In UMOSFET, internal resistance is reduced due to the elimination of JFET region of DMOSFET. Cross-sectional image of trench MOSFET is presented in Figure 1.4.

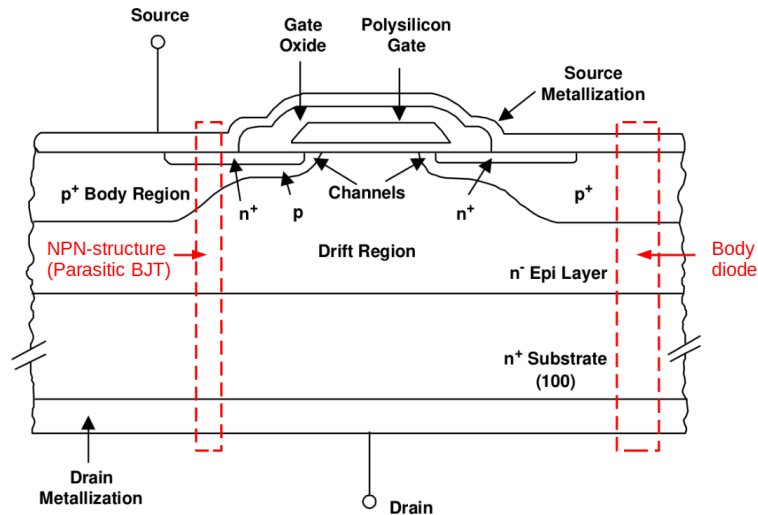


Figure 1.3: Cross-sectional layout of a planar vertical power n-channel DMOSFET with highlighted parasitic BJT and body diode structures. After [6]

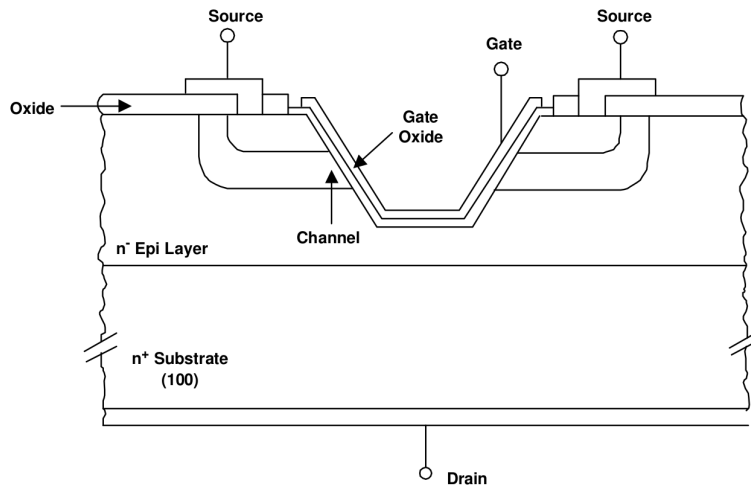


Figure 1.4: Cross-sectional layout of a vertical n-channel power trench MOSFET [6]

Super Junction MOSFET (SJ MOSFET)

As mentioned earlier, high voltage power devices voltage blocking capability is related to wide depletion layer which is obtained through low doping level in the epitaxial layer. Low doping level in the semiconductor leads to a relatively high R_{ON} . To overcome possible issues with high R_{ON} of the conventional power MOSFET, super junction power MOSFET was developed [7]. Comparison between traditional VDMOSFET and SJ MOSFET structures are presented in Figure 1.5.

Insulated Gate Bipolar Transistor (IGBT)

Insulated Gate Bipolar Transistor (IGBT) is a combination of bipolar junction transistor (BJT) and MOSFET technologies. It consists of pnpn structure and MOS gate. Advantage of IGBT is low forward voltage drop compared to MOSFET of the same size but it has higher switching times due to relatively slow decay of collector current [4]. Nowadays, with IGBT technology, it is possible to reach a blocking voltage of several kilovolts [9]. Cross-sectional layout of IGBT is presented in Figure 1.6.

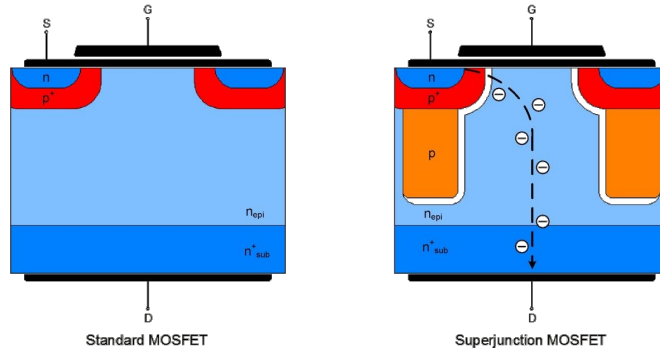


Figure 1.5: Cross section of standard MOSFET and SJMOSFET [8]

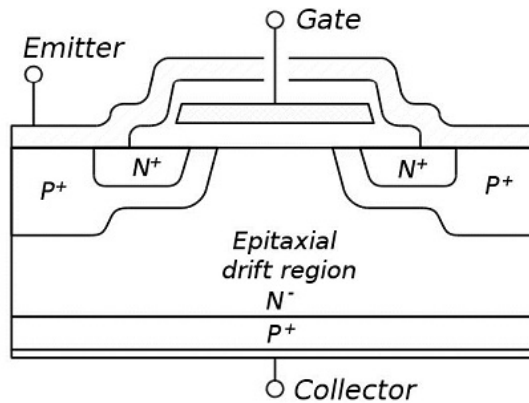


Figure 1.6: Cross-sectional layout of an insulated gate bipolar transistor (IGBT).

1.2.2 SiC-based power devices

SiC-based power devices offer superior dynamic and thermal performance over conventional Si-based power devices. Compared to Si, the critical breakdown field of SiC is 6-7 times higher and therefore, SiC devices can withstand higher electric field inside the structure compared to Si-based devices. Therefore, same blocking voltage can be achieved with thinner depletion layers. SiC-based devices also has lower on state resistance and higher thermal conductivity than their silicon counterparts resulting in higher maximum power density.

In this part, three common silicon carbide based power devices are presented: MOSFET, Metal Semiconductor Field Effect Transistor (MESFET) and Schottky Barrier Diode (SBD).

MOSFET

The geometry and the operating principle of SiC power MOSFET is very similar to its Si counterpart which structure is presented in Figure 1.3. The main difference is obviously the semiconductor material Si replaced with SiC. Due to higher critical breakdown field of SiC compared to Si, thinner epitaxial layer can be used to reach same blocking voltage capability than in Si devices. SiC MOSFETs exist in both DMOSFET and UMOSFET structures [5]. As with Si MOSFET, SiC MOSFET also contains same parasitic structures, presented in Figure 1.3.

Due to higher electric field in the device, the gate oxide layer, which in both Si and

SiC MOSFETs is silicon dioxide (SiO_2), may also be exposed to higher electric field than in Si devices. This can be a long term reliability concern for SiC MOS devices [5].

MESFET

Another SiC-based power transistor technology is MESFET which was originally developed as replacement for gallium arsenide (GaAs) microwave FETs. It has no active gate oxide between the channel and the gate terminal but the gate metal forms a Schottky contact with the n-type channel layer. MESFETs are commonly normally-on devices and applied negative gate voltage creates depletion layer under the gate reducing the channel current and if negative gate voltage is sufficient, depletion layer reaches through the channel and drain current is off [5].

SiC MESFET technology might be preferred over SiC MOSFET technology in some cases due to the poor quality of the SiC/SiO₂ interface in MOSFET. However, field dielectric might be added in order to increase the breakdown voltage of the device [10]. The n-channel MESFETs include normally-on and normally-off devices. It has a horizontal structure and the drain and the source are connected via n- or p-doped semiconductor layer. Conductivity of the channel is modulated by the thickness of the depletion region under the gate [11]. The structure of MESFET is presented in Figure 1.7.

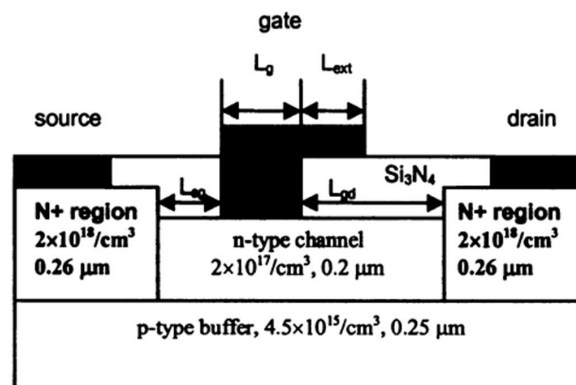


Figure 1.7: MESFET structure [11].

SBD

Due to the higher critical electric field of SiC compared to Si, thinner depletion region results in lower resistance of the drift region. Therefore, SiC SBDs offer higher breakdown voltages and faster switching speeds compared to Si SBDs. This reduces switching losses in the diode itself but also in the switching transistor within the power system. The drift region resistance does not result to significant increase in on-state voltage drop until the breakdown voltage exceeds 3 kV [12]. The structure of SiC SBD is similar to its Si counterpart structure which is presented in Figure 1.2.

1.2.3 GaN-based power devices

GaN high electron mobility transistors (HEMT) can be divided in two main categories: normally-on and normally-off devices. Intrinsically GaN HEMTs are normally-on devices

and therefore, negative bias on gate has to be applied to switch the device in the blocking state i.e. off [1]. The operation of GaN HEMT device is based on the heterojunction interface of aluminium gallium nitride (AlGaN) and GaN. Due to difference in bandgap of those two materials combined with intrinsic piezoelectric strain, electrons accumulate at the GaN/AlGaN interface forming a thin layer. Such layer of highly mobile electrons is called 2-dimensional electron gas (2DEG). Therefore, GaN HEMTs are intrinsically normally-on devices, if no further processing is done on the gate structure [13].

However, in order to guarantee a safe operation of power electronics systems, normally-off transistors are preferred. In order to achieve a normally-off device, depletion region needs to be created in intrinsic 2DEG layer under the gate. Several techniques to achieve normally-off device have been developed. Today, the most popular solutions for normally-off GaN HEMTs are cascode configuration, p-GaN gate and the recessed gate hybrid metal insulator semiconductor HEMT (MISHEMT) [14].

GaN HEMTs are often grown on the Si or SiC wafer. A thin layer of AlN is grown on the substrate wafer followed by the growth of the GaN/AlGaN heterostructure. Simplified 2D structure for GaN HEMT is presented in Figure 1.8.

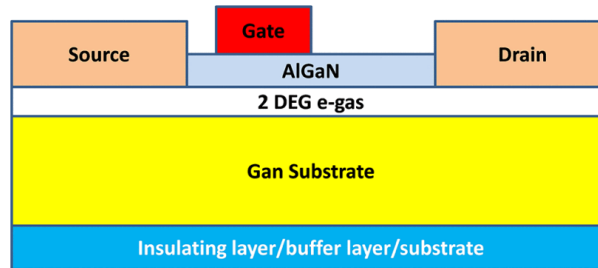


Figure 1.8: Simplified GaN HEMT 2D structure [15]. The 2DEG is formed at the interface of AlGaN and GaN layers.

Another HEMT technology, which combines metal-oxide semiconductor (MOS) structure to HEMT structure is called MOSHEMT. MOSHEMT structure is similar to conventional GaN HEMT except there is an additional oxide layer between gate contact and AlGaN barrier layer in order to suppress the gate leakage current. For example, Al_2O_3 , HfO_2 and MgCaO are used as oxide layer material [16–18].

1.3 Applications and needs

1.3.1 Application and technology

Due to the superior properties of the WBG semiconductor materials, they have gained interest in critical industrial applications, where high temperature, high power and high switching frequencies are required such as in more electric airplanes (MEA) [19], in electric vehicles (EV) and hybrid electric vehicles (HEV) [20]. Medium range of output power with high speed switching performance is the target application area for GaN devices, whereas SiC should cover more of the high power applications taking advantage of higher thermal performance of SiC [21]. Diagram of the different applications for WBG devices as a function of operating frequency and output power is presented in Figure 1.9.

Power electronics is already well implemented in different parts of the aircraft, such as in flight control, air ventilation, fuel pump etc. Due to the increasing amount of new

converter types, loads and power networks in MEA, even larger proportion of the aircraft parts needs power electronics integration [22].

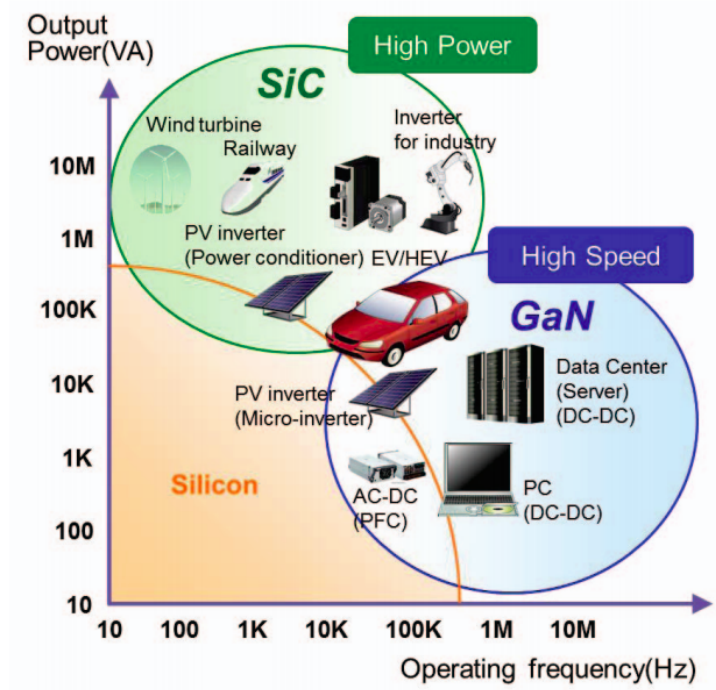


Figure 1.9: Potential applications of GaN- and SiC-based switching power transistors [21].

1.3.2 Switching power converters: from device to system

Power management of many systems is achieved by switching the current flow through the power devices between on- and off-states. In on-state, the device exhibits current flow through it and the voltage across the device consists only of the devices on-state voltage drop, which is generally some volts, depending on the technology and the current. In off-state, the voltage across the device terminals can reach thousands of volts but the current flowing through the device is only at the microampere scale. The system requirements define the used technology. MOSFET and IGBT technologies as well as Schottky power diodes are widely used in high voltage electronic systems for blocking high voltages and rectifying the current. A block presentation of power converter is presented in Figure 1.10.

There are several switching power converter topologies for different power conversion purposes. They can be classified by their input, output or conversion mode. Power converters can be used for AC-AC, AC-DC, DC-DC and DC-AC conversion. Also, they are used to step up (boost converter) or down (buck converter) the input voltage. As an example, a schematic of a simple DC-DC boost converter is illustrated in Figure 1.11.

In the core of switching power converters are power MOSFET and diode. Those are the key components of the power unit and due to their non-ideal switching behaviour, they contribute in the power consumption of the system. When a device is in on-state, it has low but not non-negligible R_{ON} . Also when the device is off, it has a small leakage current through it. On top of that, between on- and off-states, devices spend short period of time in high resistance mode dissipating power resulting in switching losses. To optimize switching process, low on-state resistance, low off-state leakage current and fast transition

from on- to off-state and back are desired. It should be kept in mind that when operating MOSFETs, a dedicated gate driver circuitry is needed in order to switch MOSFET on and off efficiently.

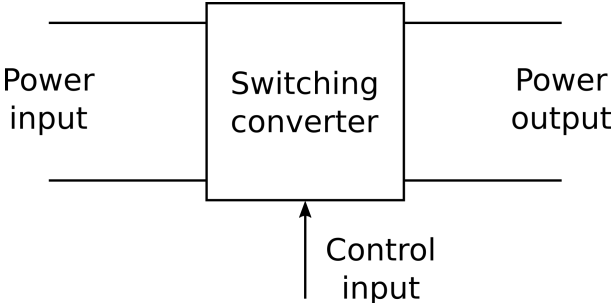


Figure 1.10: A block diagram of switching power converter [4].

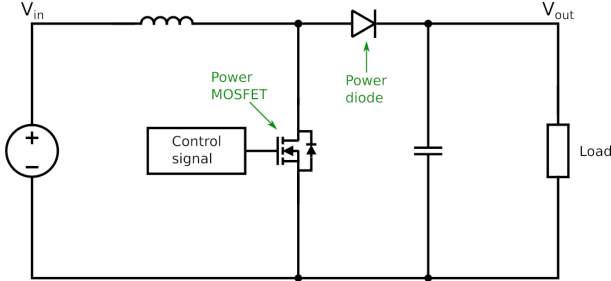


Figure 1.11: A schematic diagram of non-synchronous boost converter.

1.4 Conclusions

The wide bandgap power devices have gained interest in industry as well as in the scientific community, thanks to their superior material properties over silicon. In this chapter, we introduced the most common power device technologies based on Si, SiC and GaN materials. SiC- and GaN-based power devices are expanding the application areas of power devices in maximum power and switching speed domains.

Chapter 2

Radiation and aging effects on power devices: a state of the art

Power electronics operating in space, atmospheric and terrestrial environments are subjected to energetic radiation, which can affect the performance and reliability of the device and the system. The energetic radiation can compromise the electronics operation over time by accumulation of damage or by a single particle interaction with the device. In this chapter, such radiative environments are introduced with explanations of the radiation types as well as their origins. Then, the different radiation effects on silicon and WBG-based electronics are introduced and discussed in detail. On top of that, radiation test methodologies and facilities for power device single event effects testing are introduced. Finally, an overview of aging effects on power electronics devices is introduced.

2.1 Radiation environments

2.1.1 Space radiation environment

AC- and DC-based Power Management And Distribution (PMAD) systems are used in several space systems such in ISS and satellites for example motion control and electric propulsion purposes. Electronic power devices will then be irradiated by different irradiation types. During the post-launch manoeuvres of the electrically propelled satellites, the electronics will be subjected for several months to particles from the radiation belts. Some of the electronic systems may be switched off during the expected high radiation exposure periods but this is not always possible for the propulsion or motion control systems.

Space radiation environment consists of three main sources: galactic and extra-galactic cosmic rays (GCR), solar energetic particles (SEP) and trapped particles. Radiation environment and exposure varies depending on the mission orbit and duration. Traditionally, there are three main near-earth space mission orbits classified by the altitude:

1. Low Earth orbit (LEO) reaches 2000 km altitude from the Earth's surface. Most of the human-made objects in space are in LEO including the International Space Station (ISS)
2. Medium Earth Orbit (MEO) covers altitudes from 2000 to 35780 km. This orbit is used by Global Positioning System (GPS) satellites.
3. Geostationary orbit (GEO) is at 35 780 km altitude on which the satellite moves

around earth in 24 hours. Since the satellite is above the same spot of the Earth's surface, they can be used for telecommunication and weather monitoring.

GCRs originate from outside the solar system and consist of charged energetic particles. The majority of the GCR is made of atomic nuclei of which 87% consist of protons, 12% alpha particles and 1% consists of heavier ions [23]. The flux of GCRs is modulated by the solar activity. During the high solar activity there is attenuation in the GCR flux as illustrated in Figure 2.1.

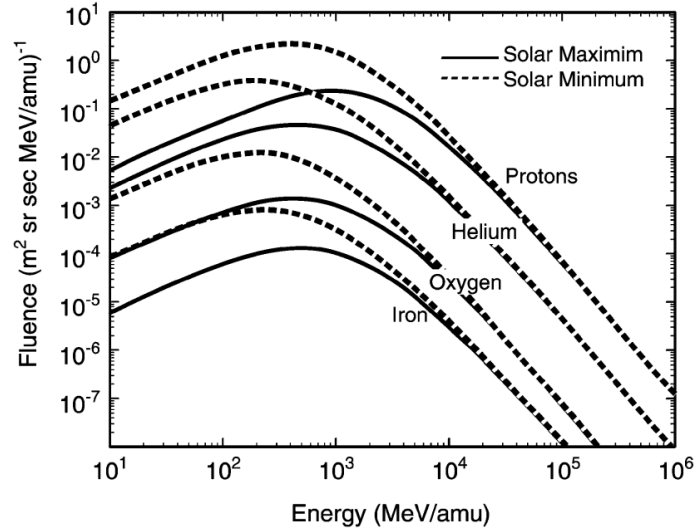


Figure 2.1: Galactic cosmic ray energy spectra for different particles during solar maximum and solar minimum [23].

The commonly used metrics for the particle interaction with material is Linear Energy Transfer (LET) which quantifies the energy deposited by the ionizing particle per unit path length in the target material [23]. LET spectra of GCR particles on GEO and interplanetary space is illustrated in Figure 2.2. Due to the Earth's magnetic field and atmosphere, LET spectrum varies depending on the altitude and geo-magnetic location.

SEPs include protons, heavier ions, electrons, neutrons, gamma rays and X-rays. Flux of SEPs vary over time and is correlated with the solar activity cycle. Solar activity maximum and minimum alternate with about 11-year cycle. Although, sometimes intense SEP events can be observed during the minimum phases. Charged SEPs are normally shielded by the Earth magnetic field and atmosphere but reach closer to the surface at high latitudes [24].

The trapped radiation belts consist mainly of protons and electrons which are trapped in gyration movement due to influence of the earth's magnetic field. Trapped particles are mostly of concern in total ionizing dose (TID) sensitive components. Such trapped particles can contribute up to 50% to the TID accumulated during the mission. However, also single event effects (SEE) have been observed to occur due to trapped protons.

Electrical propulsion used in satellites produces usually less power compared to chemical propulsion. Therefore, when travelling to the orbit, electrically propelled satellites spend longer time crossing the radiation belts resulting in tighter radiation constraint regarding both TID and SEE.

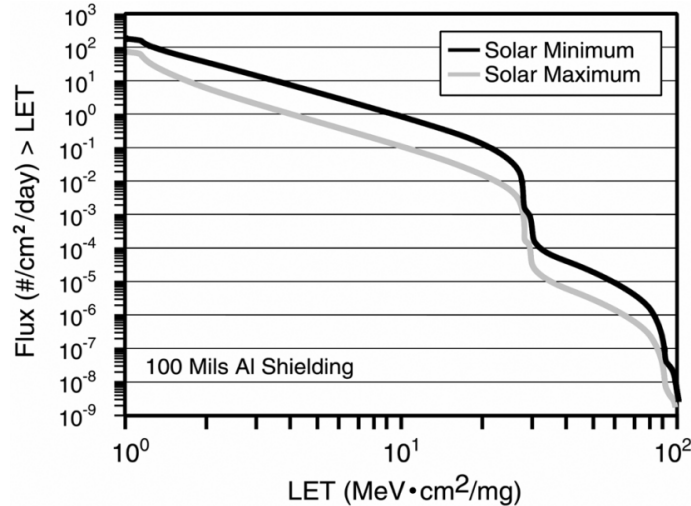


Figure 2.2: Integral linear energy transfer spectra for GCR during solar maximum and solar minimum on GEO and in interplanetary space [23].

2.1.2 Atmospheric radiation environment

In atmospheric environment, the most important radiation constraint in both avionic and ground applications are the neutrons. A neutron flux increases with the altitude but the risk for a neutron-induced failure on electronics is present also at the ground level.

The atmospheric radiation environment originates from the interaction of galactic cosmic rays (GCR) and solar energetic particles (SEP) with the atmosphere as presented in Figure 2.3. The interaction of energetic primary particles with molecules in the atmosphere results in shower of secondary, lower-energy particles, such as protons and neutrons. Regarding the SEE in the avionic altitudes, largest contribution comes from neutrons and then primary and secondary protons. It has to be noted that the particle flux is strongly dependent on the altitude. The flux at 10 km altitude is approximately 300 times higher compared to ground level. The simulated neutron and proton energy spectrums as a function of energy at various altitudes are shown in Figure 2.4.

As mentioned earlier, primary particles originate from two main sources: GCR and SEP. SEPs can result in significant enhancement in secondary particle flux at avionic altitudes. The flux can be enhanced by two orders of magnitude compared to GCR-induced neutron flux. Moreover, SEP-induced flux varies over time since the sun activity varies and it is also dependent on geographic location. In contrast to particle environment in interplanetary space, angular distribution of the particle flux is anisotropic, which adds complexity in the modelling of the environment [24]. In fact, the radiation sensitivity of the electronic components may depend on the incident angle of the particle. Therefore, it is important to assess the direction of the radiation field in the application. This will be discussed in the following sections.

Regarding the neutron energy, Griffoni *et al.* did not observe neutron induced failures on SiC MOSFET with irradiation bias voltages up to 85% of the V_{DSmax} with 50 MeV or 80 MeV neutrons [26]. Therefore, it is discussed in [27], that the higher energy part of the atmospheric neutron spectrum contributes more on the production of high energy recoils which have sufficient energy to induce device failure than the < 85 MeV neutrons.

Several instrumentations and models have been developed for studying the radiation environment at aircraft altitudes. Such methods are well summarized in RADECS2017 Short Course notes by Santin *et al.* [24]. Technical and process management issues

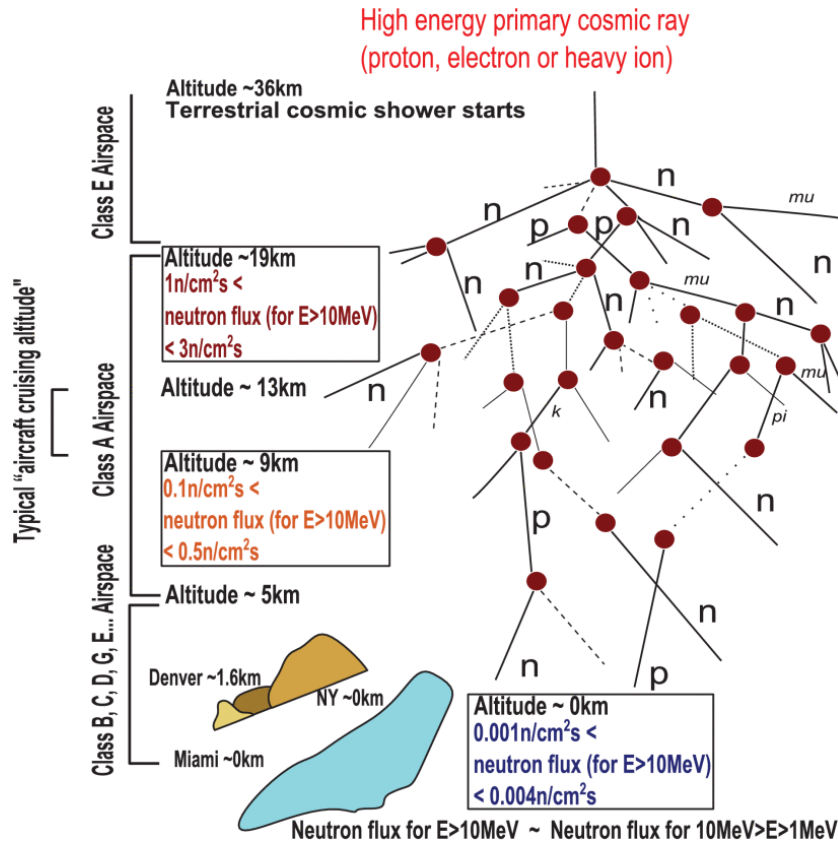


Figure 2.3: The interaction of energetic primary particles with molecules in the atmosphere results in shower of secondary, lower energy particles. Neutron flux is high at avionic altitudes but is also significant to cause SEEs at sea level [25].

due to natural radiation environment on avionic electronic systems are covered in IEC standard 62396 [28]. It should be noted that in the real aircraft environment, due to different thermalizing materials, such as fuel, water, passengers and building materials, the neutron energy spectrum and flux might be different compared to the environment outside the aircraft [24].

2.1.3 Ground level radiation environment

Regarding the electronic systems, applications in which power electronics is exposed to atmospheric radiation at the ground level include transportation, such as automotive and electric trains, renewable energy production, such as wind and solar energy as well as consumer electronics [2]. In addition, electronic systems are exposed to human-made radiation environments, such as nuclear power plants, particle accelerators and radiation treatment facilities.

The energy spectrum of ground level atmospheric neutrons differs from the one in avionic altitudes most importantly by flux. The energy distribution is similar compared to flux at avionic altitudes [24]. The direction of the flux is vertical [29]. Therefore, it is important to assess the angular orientation of the device on its radiation sensitivity. At ground level, it has to be noted that the building materials, snow and water attenuate the neutron flux as a function of their chemical composition, thickness and density [24].

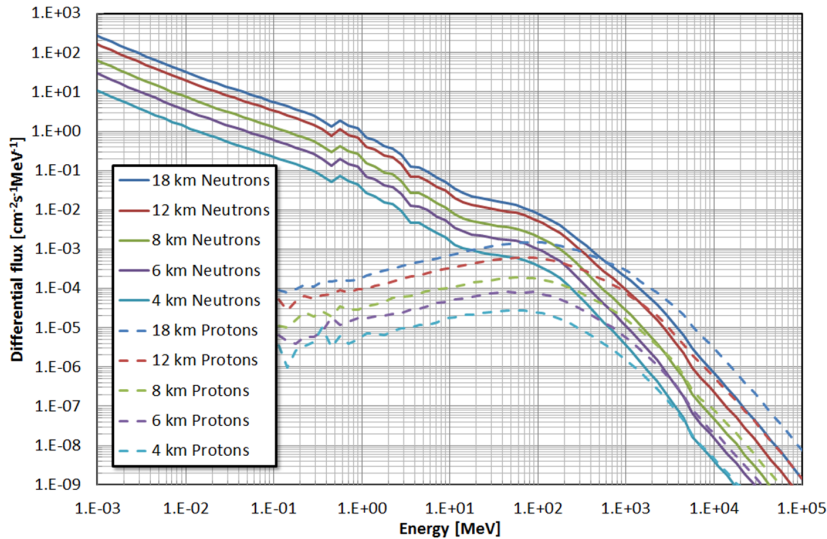


Figure 2.4: Simulated neutron and proton energy spectrum as a function of energy at various altitudes [24].

2.2 Radiation effects on electronic devices

Electronic devices are exposed to different types of radiation in their operation environments. Three main categories of radiation effects, which can affect in the reliability of the system, are single event effects (SEE), total ionizing dose (TID) and displacement damage (DD). SEE can cause a device failure by only one energetic particle whereas TID and DD are cumulative effects.

2.2.1 Total Ionizing Dose (TID)

The most sensitive materials of metal-oxide-semiconductor (MOS) system to ionizing radiation are the insulators. When exposing the oxide to ionizing radiation, electron-hole (e-h) pairs are created. Depending on the conditions, some portion of those electrons and holes eventually recombine but some portion of the electrons are separated from the holes. Due to the higher mobility of electrons [30], they are swept away due to the applied electric field. Since hole mobility is lower, they remain near their point of generation. Even though, the holes are relatively immobile compared to electrons, they do migrate through the oxide due to the electric field and the transport is sensitive to applied bias and temperature. Some fraction of those holes fall into trap states where they can persist even for years causing a threshold voltage shift of the MOS transistor. Underlying physical mechanisms of ionizing radiation on MOS system are summarized in Figure 2.5 [31].

In n-MOS devices, the oxide trapped charge results in negative threshold voltage shift and interface trapped charge results in positive threshold voltage shift and in increase of subthreshold swing (Figure 2.6) [32]. The total threshold voltage shift ΔV_T is given by the sum of the contributions of oxide trapped charge and interface trapped charge Equation (2.1)

$$\Delta V_T = \Delta V_{ot} + \Delta V_{it} \quad (2.1)$$

In order to calculate the ΔV_{it} , stretchout voltage V_{so} is defined in Equation (2.2)

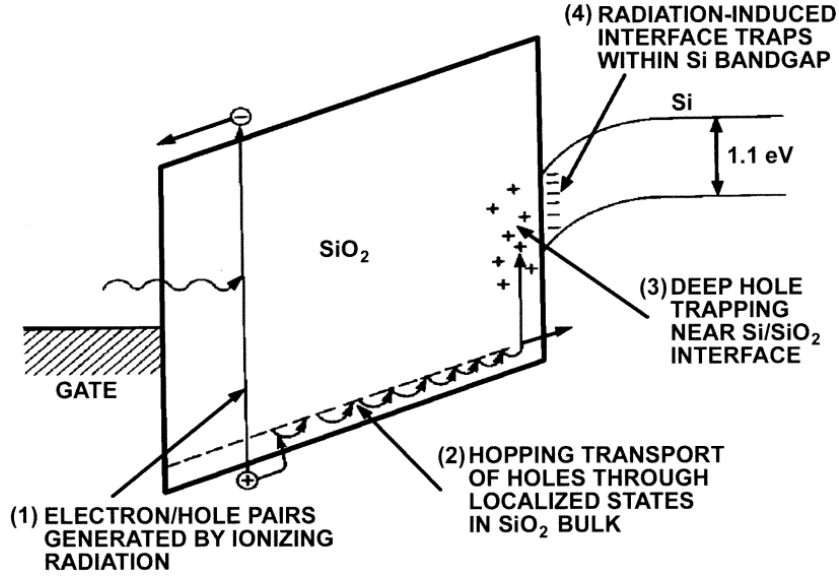


Figure 2.5: Schematic energy band diagram for MOS structure, indicating major physical processes underlying ionizing radiation response. Positive bias is applied to the gate [31].

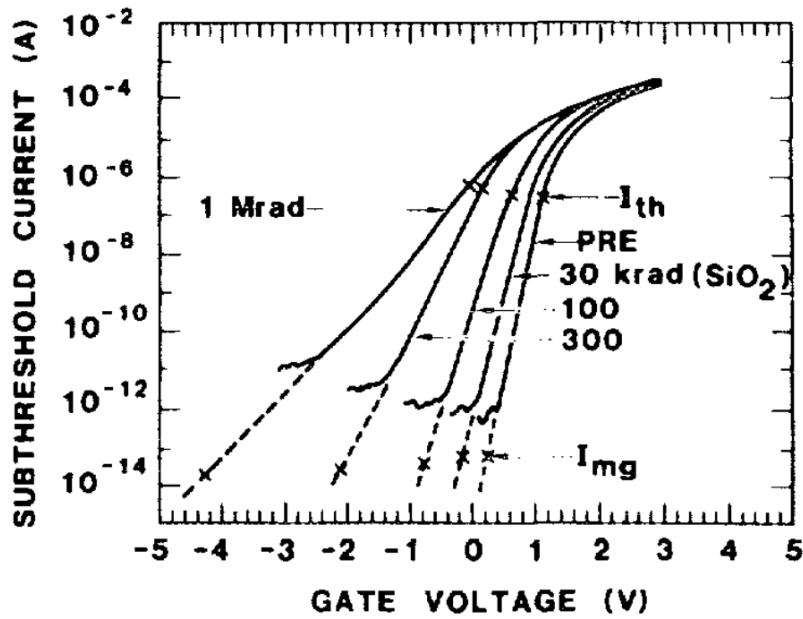


Figure 2.6: I_{DS} V_{GS} curves of the MOSFET for different ionizing doses. The change in location of the curve is related to threshold voltage shift and therefore, oxide trapped charge. The change in slope of the curve is related to interface trapped charge [32].

$$V_{so} = V_T + V_{mg}, \quad (2.2)$$

where V_{th} and V_{mg} refer to gate voltage values for respective current values in Figure 2.6. Then, the contribution of interface trapped charge and oxide trapped charge in threshold voltage shift can be calculated with Equation (2.3) and Equation (2.4)

$$\Delta V_{it} = (V_{so})_2 - (V_{so})_1 \quad (2.3)$$

$$\Delta V_{ot} = (V_{mg})_2 - (V_{mg})_1 \quad (2.4)$$

ΔV_T as a function of TID and calculated contributions from oxide and interface trapped charge are presented in Figure 2.7.

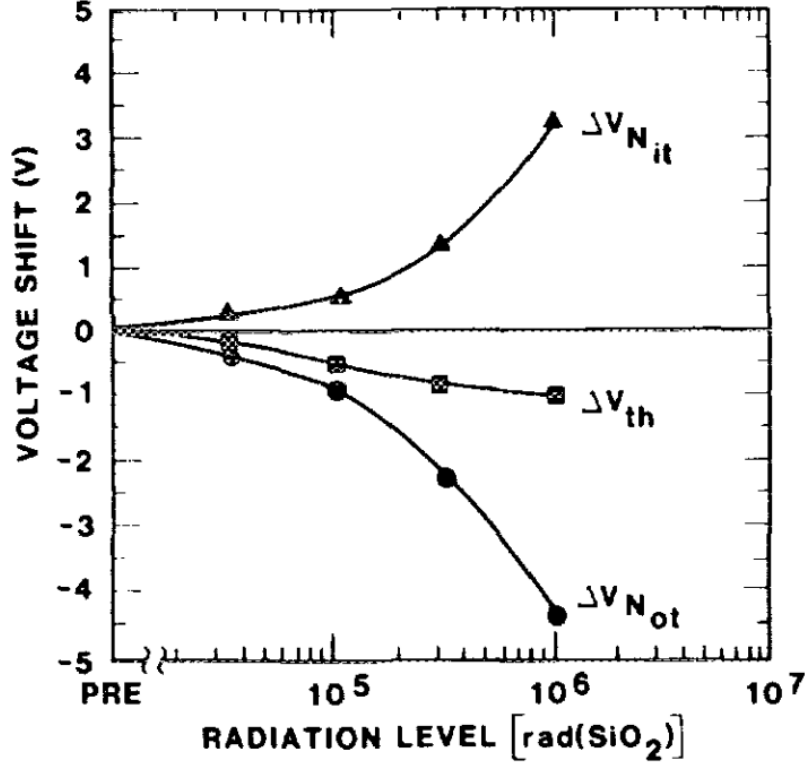


Figure 2.7: Contribution of oxide (V_{Not}) and interface (V_{Nit}) trapped charges on the threshold voltage (V_T) calculated from the curves in Figure 2.6 [32].

TID in SiC power devices

Regarding the power devices, since the fundamental structures of Si MOS and SiC MOS devices are similar, the mechanisms which lead to change in electrical parameters, are also similar. In SiC MOSFETs, the most significant TID effects are related to trapped charge in the gate oxide and at the oxide-semiconductor interface. Oxide trapped charge has an electrostatic effect causing a negative shift in threshold voltage. Since positive voltage at the gate is needed to turn nMOS device on, trapped positive charge in the oxide volume reduces the amount of positive voltage needed to turn the device on. Interface trapped charge affects the carrier mobility in the channel by trapping carriers and therefore reducing the transconductance and increasing the channel resistance. In Figure 2.8, trapped charges in a vertical MOSFET structure are drawn.

It has been observed in several studies that SiC power devices are sensitive to TID [33–42]. The effect of irradiation temperature [36, 37] and irradiation bias [38, 40, 41] on TID sensitivity of SiC MOS devices has been studied as well difference in TID sensitivity

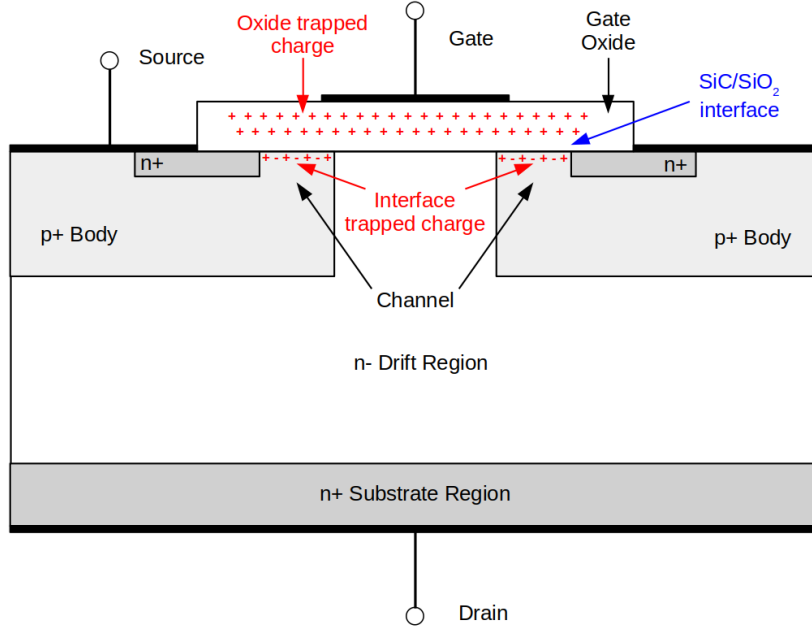


Figure 2.8: Simplified cross-section illustration of vertical SiC power MOSFET structure. Dimensions are not in scale in order to emphasize gate area trapped charge due to TID. The fundamental structure of SiC- and Si-based MOSFETs are similar. The main difference is different semiconductor material and therefore the semiconductor-oxide interface.

between n- and p-channel SiC MOSFET and MOSFETs with different gate oxidation methods [35, 37].

Ohshima et al. observed -2 V shift in V_T and increase in off-state drain leakage current of SiC MOSFETs when irradiations were performed at room temperature. Much less irradiation-induced change in such parameters were observed while irradiating devices at 150°C up to 5.8 MGy dose. However, compared to Si devices, difference in TID sensitivity due to temperature is lower [37]. Temperature dependence on TID sensitivity was also studied by Akturk et al. They did not observe significant differences in TID sensitivity between 27°C and 125°C irradiation temperatures up to 6 kGy [36].

The worst case bias condition for TID induced ΔV_T on SiC MOSFETs seems to be positive bias on the gate. The effect of TID on ΔV_T is similar between negative bias or no bias during irradiation [38, 40]. Similar gate bias dependence was observed with SiC MOS capacitors in which the stronger midgap voltage (V_{mg}) shift was observed for capacitors irradiated with positive gate bias compared to no bias or negative bias during irradiation [41].

Synergetic effect of high temperature gate bias (HTGB) and total ionizing dose on SiC MOSFETs was studied by Zhang et al. They observed stronger threshold voltage shift for γ -ray irradiated devices which were exposed to pre-irradiation HTGB compared to fresh devices. Irradiations were performed with no bias applied on the device [39]. In general, SiC MOSFETs have been found to be less sensitive to TID induced threshold voltage shift compared to Si-based devices. Figure 2.9 shows the shift in V_T for different SiC power transistor technologies compared to Si.

Since the threshold voltage shift of the transistor is commonly related to trapped charge in the dielectric part of the device, MESFETs are expected to exhibit less shift in V_T due to absence of gate oxide. However, sensitivity to ionizing radiation for MESFETs has been observed [43–46]. The shift in V_T in MESFETs is related to charge

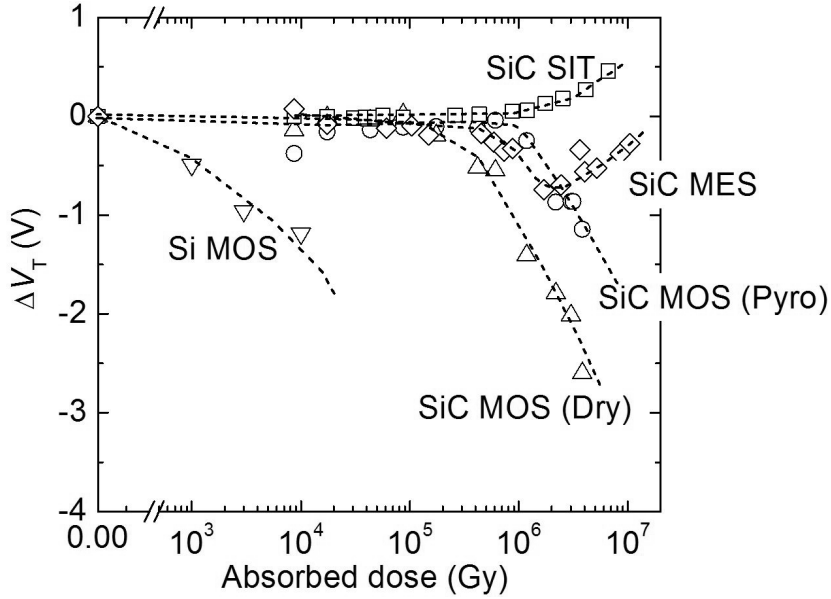


Figure 2.9: Comparison of threshold voltage shifts with TID of different technologies [11].

trapping in the semi-insulating substrate and in the buffer layer. Some contribution in ΔV_T originates from charge trapping in the insulator material of the passivation layer and semiconductor-insulator interface [44]. Also, decrease in Schottky barrier height at the gate metal-semiconductor junction and charge trapping in the n-type channel layer have been reported to contribute in V_T shift [43, 46].

TID in GaN power devices

Since the GaN HEMTs does not always have a dielectric layer under the gate like in conventional MOSFETs (except MOSHEMT and MISHEMT), it is expected that their response to ionizing radiation should be lower compared to MOSFET technologies. However, it has been shown in many studies that GaN HEMTs exhibit sensitivity to TID [16, 18, 47–53]. The most common degradation modes are threshold voltage shift and decrease in peak transconductance [16, 18, 47–49, 51]. Figure 2.10 shows a simplified cross section of GaN MOSHEMT and its charge trapping locations due to ionizing radiation.

Transconductance degradation is a result of generation of traps in the proximity of the channel where they capture charge carriers and hence decrease the mobility. Threshold voltage shift is due to the trapped charge further away from the channel layer affecting the electrostatic behaviour of the device. Jiang et al. observed threshold voltage shift and peak transconductance degradation in unpassivated GaN HEMTs under 10 keV X-ray irradiations but only threshold voltage shift in passivated devices. This is explained by the oxygen impurity traps which are present both at the surface and close to 2DEG layer in unpassivated devices whereas in passivated devices they only exist at the surface [51]. Also, gamma ray irradiation induced Schottky gate degradation has been observed for GaN HEMTs [52]. Such degradation causes increased gate leakage current in off-state and incomplete depletion of 2DEG resulting in drain-to-source leakage current.

Since introducing the oxide material in the device, we can expect to observe higher ΔV_T compared to HEMT with no oxide. It has indeed been observed in [16, 18]. In fact, for a doses up to 3 krad (in SiO_2), both MOSHEMT and HEMT exhibit the same, negative shift in V_T as a function of TID due to hole trapping in AlGaN layer. Such

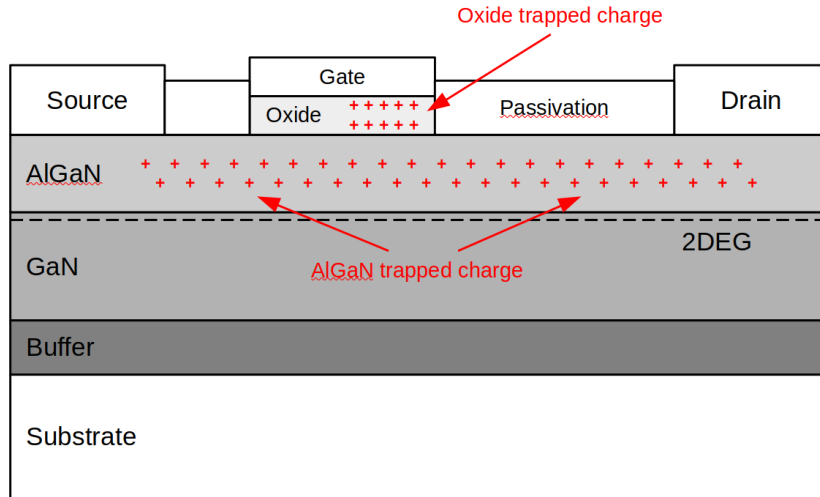


Figure 2.10: Simplified cross section representation of GaN MOSHEMT and with ionizing radiation induced trapping locations.

shift in V_T occurs at the same rate for both technologies and saturates at 3 krad dose, which corresponds to a trap density around $1 \times 10^{18} \text{ cm}^{-3}$ in AlGaN layer. However, while shift in V_T saturates for HEMT without gate dielectric, V_T for MOSHEMT continues to decrease at a slower rate due to positive charge trapping in the oxide layer (Figure 2.11) [16].

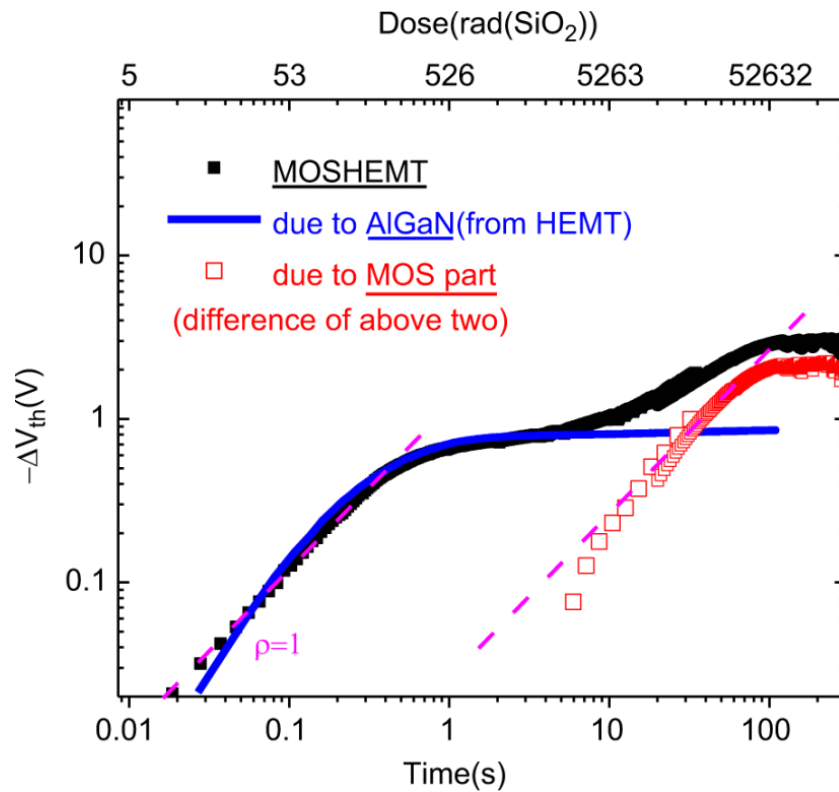


Figure 2.11: ΔV_T for HEMT and MOSHEMT as a function of TID showing similar behaviour for both devices at low doses due to trapping of positive charge in AlGaN layer and difference at higher dose values due to oxide trapping [16].

2.2.2 Displacement Damage (DD)

While TID considers the energy loss of a particle and/or electromagnetic radiation resulting e-h pair generation, displacement damage (DD) considers the nonionizing energy loss (NIEL) which results in displacement of the atom from its lattice site and phonon production. One frequently employed quantity for DD is the displacement damage dose (D_d) which is typically expressed in units of MeV/g. In simplest form, D_d is defined by the particle fluence times NIEL [54].

The simplest interpretation for DD is that the atom which is displaced, is called interstitial and the absence of atom from its lattice site is called a vacancy. Nearby vacancy and interstitial are known as a Frenkel pair. When such defects are relatively far apart in the semiconductor volume, they are known as isolated or point defects. The defects can also form larger regions of dislocation known as defect clusters, as illustrated in Figure 2.12 [54].

The DD is of a concern especially in neutron- and high-energy proton-rich environments. Such particles do not contribute as much to ionization compared to heavier charged particles. Therefore, in DD testing, protons and/or neutrons are commonly used. However, also relativistic electrons have been used [55].

The presence of defect clusters due to DD in the semiconductor lattice can cause the increase in trapping of the charge carriers, reduction of the recombination lifetime and diffusion length. As a consequence, it can be observed as decreased mobility and increased leakage current in the semiconductor devices [54]. Increase in depletion layer resistance resulting in increase in forward voltage drop has been observed for Si SBDs [56].

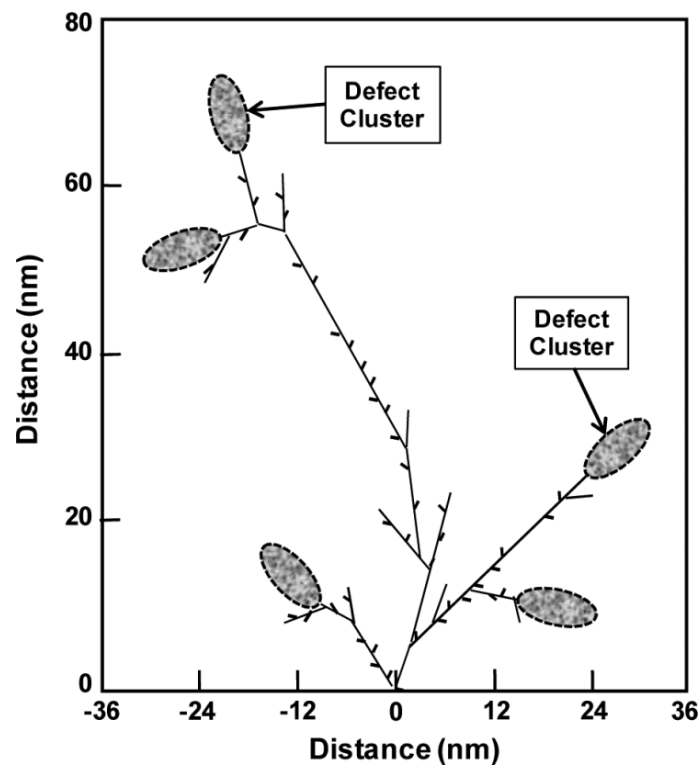


Figure 2.12: Displacement damage produced in Si by a 50 keV primary recoil atom [54].

DD in SiC power devices

Previous studies indicate that SiC devices are inherently less prone to displacement damage effects compared to their Si counterparts [57, 58]. For example, SiC Schottky barrier diodes were irradiated with 203 MeV protons and the largest change in characteristics has been observed in series resistance which increased by one order of magnitude after proton fluence of $4 \times 10^{14}/\text{cm}^2$ [57]. This effect is explained by the decrease in effective dopant density due to carrier removal by radiation induced defects. Very small changes in forward and reverse bias characteristics were observed.

In SiC JFETs, no significant changes in any of the device characteristics have been observed until $1 \times 10^{15}/\text{cm}^2$ neutron fluence whereas at higher fluence, the effect of displacement damage can be seen in decrease in transconductance and drain current [59]. However, majority of the displacement defects can be removed through high temperature annealing [60].

DD in GaN power devices

As is the case for SiC, also GaN material is relatively robust against displacement damage [55]. DD in GaN based power devices is often observed by decrease in drain current in on state and in transconductance [61–65] as well as shift in threshold voltage [66, 67]. Radiation-induced defects in GaN and/or AlGaIn layers cause carrier scattering and carrier removal from 2DEG resulting in degradation of transfer characteristics. Defect centers can be formed inside or outside the 2DEG layer. However, since the 2DEG has infinitesimal thickness, majority of the defects are formed outside the 2DEG. Defect centers outside the 2DEG scatter the carriers through Coulomb interactions affecting the mobility in the 2DEG [61].

In GaN HEMTs, it has been found that displacement energy threshold for atoms within the defect complexes is lower than for crystal atoms. Therefore, displacement due to particle-matter interaction is more likely to occur in regions with process-related, pre-existing defects and radiation induced defects [63, 66].

2.2.3 Single Event Effects (SEE)

Power MOSFETs and diodes operating in the particle-enriched radiation environments are susceptible to destructive failures which in turn affect the power system performance [68]. Single event effects (SEE) are caused by single particles interacting with the device material and creating ionization path along its track. The interacting particle may be charged, such as heavy-ion or proton, when it deposits energy due to ionization of the target material. In addition to SEE induced by charged particle, impinging particle can also interact with nucleus of the target material. This is the case especially with neutrons. Since neutron is non-charged particle, it is incapable of depositing energy by direct ionization. However, secondary particles due to neutron collision with lattice atoms of target material can ionize the material and produce electron-hole pairs along their trajectories and further induce device failure. Illustration of neutron interaction with vertical MOSFET device is presented in Figure 2.13. It has to be noted that also the charged particles can interact with the nucleus of target atoms.

In this section, SEEs in Si-based power devices are introduced and explained since their basic mechanisms are well known and agreed within the community. SEEs in WBG devices are presented and discussed in Section 2.3.

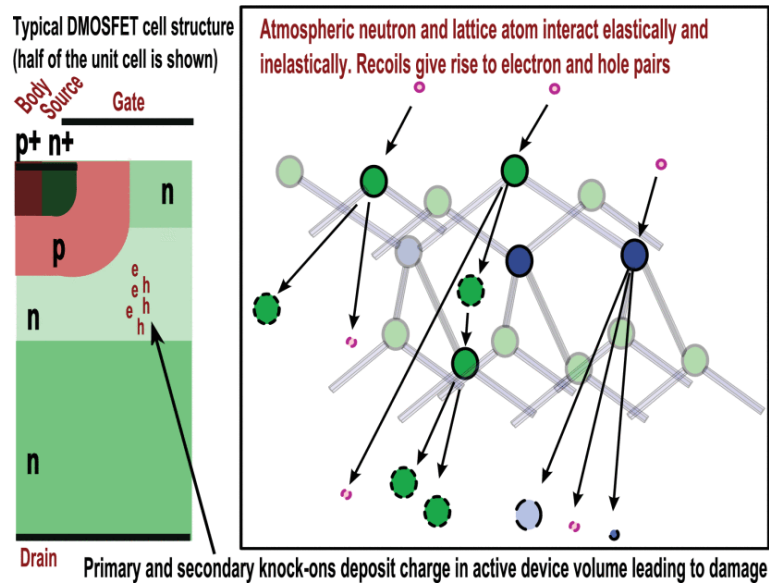


Figure 2.13: Impinging neutrons can knock atoms off their lattice sites and generated secondary recoils can further induce device failure [25].

Single event burnout (SEB)

As mentioned in previous chapter, the power MOSFET contains parasitic bipolar junction transistor (BJT) structure, where the p-body serves as base, source as emitter and drain as collector Figure 2.14. This BJT should be kept off to avoid unwanted current when the MOSFET is in off-state. The source and body of MOSFET (emitter and base of the BJT) are shorted in order to avoid the turn-on of this BJT structure. However, this parasitic BJT can be turned on due to charge generated by radiation. If the power device is in off-state blocking voltage condition, created charges separate under the electric field and cause possible destructive failure [68]. SEB mechanism in silicon (Si) power MOSFET due to heavy ion strike has been explained by the current path due to the charges generated along the ion track followed by turn-on of the parasitic npn bipolar junction transistor (BJT) [69–71]. The schematics of the parasitic BJT is presented in Figure 2.14.

The mechanism is as follows [68]:

1. e-h-pairs are generated along the ion track
2. charges separate under the electric field and current flows vertically towards the gate/epitaxial interface and further across the p-body junction to exit the device
3. due to the current flow and resistivity of the p-body region, voltage potential in this region increases and if it is high enough compared to n-source region (emitter), it results in turn-on of the BJT
4. current gain of the BJT further increases the BJT current and the process becomes self-sustaining if not interrupted by turning off the drain bias
5. resulting localized current leads to thermal runaway and device failure

SEB threshold voltage is directly related to power MOSFETs second avalanche breakdown voltage and can occur when the drain-to-source voltage (V_{DS}) exceeds the second breakdown voltage. This is explained through the IV -characteristics under quasi-stationary conditions Figure 2.15 [70]. Threshold for SEB can be raised by extending the

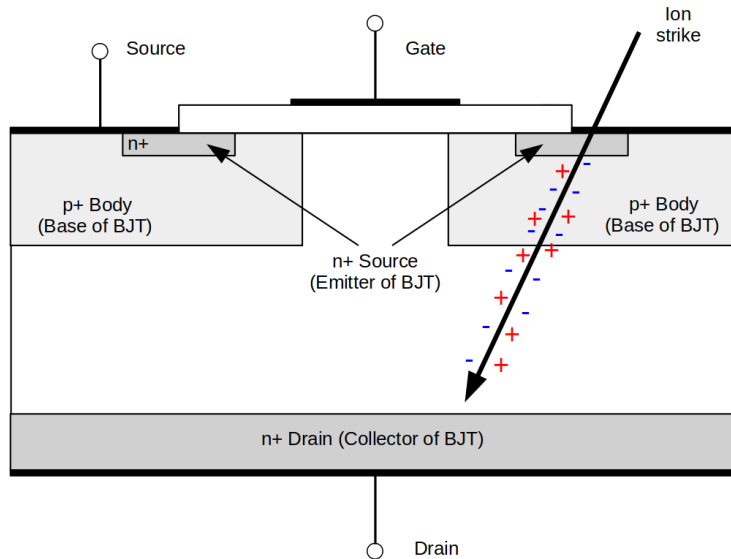


Figure 2.14: Ion-induced charge generation along the ion track and parasitic BJT structure in the vertical MOSFET.

p+-plug region at the source contact [72]. Strike location dependence to SEB sensitivity has been observed. The most sensitive location for heavy ion induces SEB is the channel area [73].

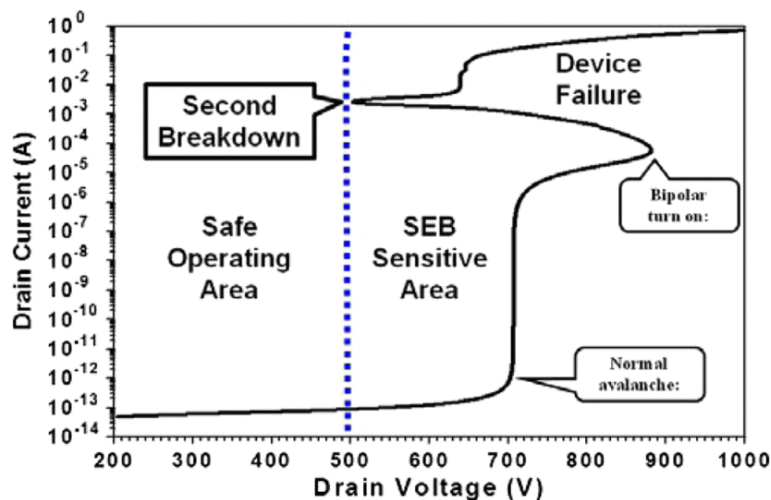


Figure 2.15: The quasi-stationary I-V curve for SEB mechanism [68]

In addition to heavy-ion induced SEB, neutron induced failure in power MOSFET was first observed in 1996 by Oberg et al. [74] followed by observation of neutron induced failures in power diodes [75]. The mechanism for neutron induced burnout in Si-based power devices is similar to the heavy ion-induced failure mechanism. Impacting neutron produces recoil ion which is able to generate charges along its track. The effect of neutron energy and type of recoils on SEB sensitivity is discussed in aforementioned studies [74, 75]. In Section 2.3, we will see that wide band gap power devices are also sensitive to single event burnout.

In Figure 2.16, we present a schematic of the evolution of the sensitive volume and

the critical charge with 10 single events, for 3 different biases for vertical power devices. The triggering of a destructive event such as a single event burnout is strongly dependent on the two parameters, the sensitive volume and the critical charge. This approach is accurate especially when dealing with power technologies having large vertical structure. In order to trigger a destructive event, a minimum amount of charge, named critical charge (Q_{crit}) has to be collected in a given sensitive volume (SV). If the collected charge (Q_{coll}) is higher than the critical charge, the destructive event occurs, where if the collected charge is lower than the critical charge, no destructive event occurs.

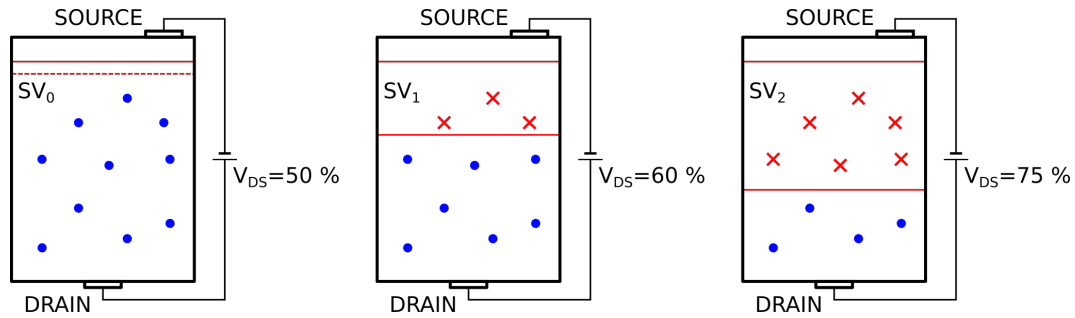


Figure 2.16: Schematic of SV with 10 single events and relative evolution of its width for 3 different drain bias voltages. Blue dots represent the non-destructive interaction ($Q_{coll} < Q_{crit}$) and red crosses represent the destructive interaction ($Q_{coll} \geq Q_{crit}$). Note that relative V_{DS} values presented here are just an example values valid for certain technology. V_{DS} value needed for destructive event is dependent on the device technology [76].

Single Event Gate Rupture (SEGR)

Single event gate rupture (SEGR) in power MOSFET can be detected as an increased gate leakage current due to formed current path through the gate dielectric. Therefore, when SEGR has occurred, the gate terminal of MOSFET cannot be used to switch transistor on and off. A device which has exhibited SEGR, may still be partly functional or completely failed [68].

SEGR occurs in Si power MOSFET due to heavy ion strike through the gate dielectric. Due to deposited charge along the ion path in the dielectric layer, conductive path is formed. If the energy stored in the gate capacitance is sufficient, temperature in the conductive path rises above the melting point of the dielectric material leading to formation of a permanent short [77]. Similar to SEB, it has been observed that the sensitivity to SEGR is dependent on the ion strike location. The most sensitive location is the neck area of the power transistor [73].

Another model for SEGR has been presented by Brews et al. Holes and electrons created by heavy ion strike in the silicon under the gate separate under electric field due to drain bias. Holes travel towards the gate dielectric and accumulate against the interface inducing image charge on the gate electrode leading to a transient increase of electric field across the gate dielectric [78]. Allenspach et al. extended the model by showing that increased amount of trapped charge is accumulated in the oxide along the ion track due to higher electric field across the dielectric [79]. Illustration of the SEGR mechanism is presented in Figure 2.17.

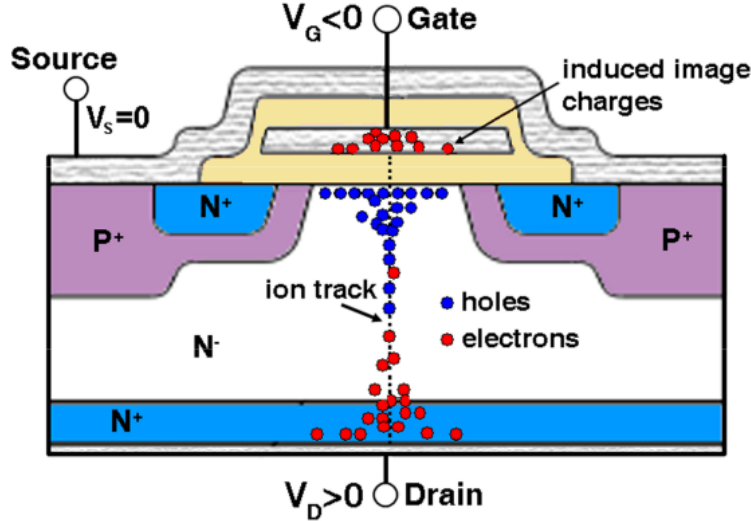


Figure 2.17: SEGR mechanism for a vertical power MOSFET[79].

Even if the SEGR is not observed during radiation test, gate dielectric weakening can occur during the radiation exposure and it can be revealed through post-irradiation electrical stress. It has been observed that the voltage bias during the heavy ion irradiation as well as ion energy plays a role in the gate oxide reliability under radiation exposure [80, 81]. In the following Section 2.3, the risk related to SEGR will be discussed for wide bandgap power devices.

Single Event Latchup (SEL)

SEL is a condition where a low resistance current path is formed through the pnpn-structure by activation of parasitic pnp- and npn-structures. SEL is mainly a concern in CMOS-structures [82]. However, pnpn structure is present also in IGBT power transistors and SEL has been observed in such technologies. When SEL occurs, current through the pnpn-structure sustains and if this current is high enough and continues for a sufficient amount of time, it can lead to a permanent short between the device terminals and therefore destruction of the device [83]. Obviously, due to their intrinsic structure, SEL is not a concern in SiC power MOSFETs or GaN power HEMTs.

2.3 SEEs on SiC and GaN power transistors: a state of the art

2.3.1 SEB mechanism in SiC devices

Several studies show that SiC power MOSFETs and diodes are susceptible to destructive single event effects due to the energetic heavy ion radiation [84–91], neutrons [25–27, 92–98] and protons [84, 99].

The SEB mechanism in SiC MOSFETs is still under debate. Based on heavy ion irradiation experiments and simulations, it has been suggested that the mechanism in SiC MOSFETs is similar to silicon-based power MOSFETs including the turn-on of the parasitic BJT [84, 85, 100], as explained in Section 2.2.3. However, some studies propose that the destructive failure can occur without activating the BJT structure [92, 94]. Those

mechanisms will be discussed further in this chapter. It is known that SEE in SiC power devices can be either destructive or non-destructive. Based on the applied drain bias voltage, single event effects on SiC power devices due to heavy ion impact can be divided in three regions (Figure 2.18) [84]:

1. non-destructive region, where no evidence of damage is observed
2. “leakage current region”, where the leakage current from drain to source permanently increases with ion fluence but damage is not catastrophic
3. SEB region, where the device exhibits destructive burnout

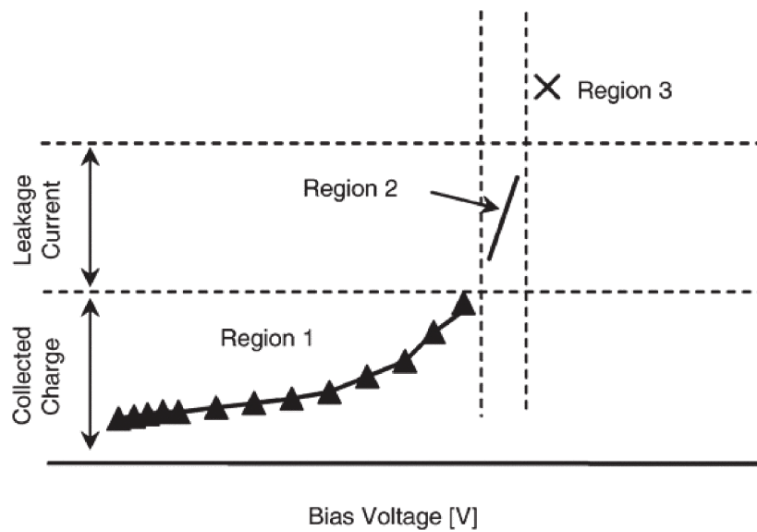


Figure 2.18: Characteristic regions for SiC power MOSFETs and diodes behavior under heavy ion irradiation [84].

Compared to its Si counterpart, the structure and operating mechanism of the SiC MOSFET are similar. The key differences between those technologies are different semiconductor materials and the thickness of the drift layer. A higher critical breakdown field of SiC allows thinner drift layer to be used in order to achieve the same voltage blocking capability than in Si devices. On top of that, higher thermal conductivity of SiC allows faster transportation of the heat away from the junction.

When comparing the SEB sensitivity of Si IGBT and SiC MOSFET with the similar ratings, it can be seen that at 75% of maximum drain voltage rating, the failure rate is approximately same for both technologies Figure 2.19. However, at the maximum rated drain voltage, Si IGBT has 10 times higher failure rate compared to SiC MOSFET [97]. A higher SEB sensitivity for Si-based power technologies has been observed also in [26, 92, 96].

Physical and technological aspects possibly related to SEB

Parasitic BJT and body diode Similar to vertical Si power MOSFETs, parasitic BJT structure exists also in SiC MOSFETs (Figure 2.20). Due to similarities in the structure and in the operating mechanism, a first evaluation could be that the SEB failure mechanism is the same as the accepted SEB mechanism in Si MOSFETs. In fact, it has

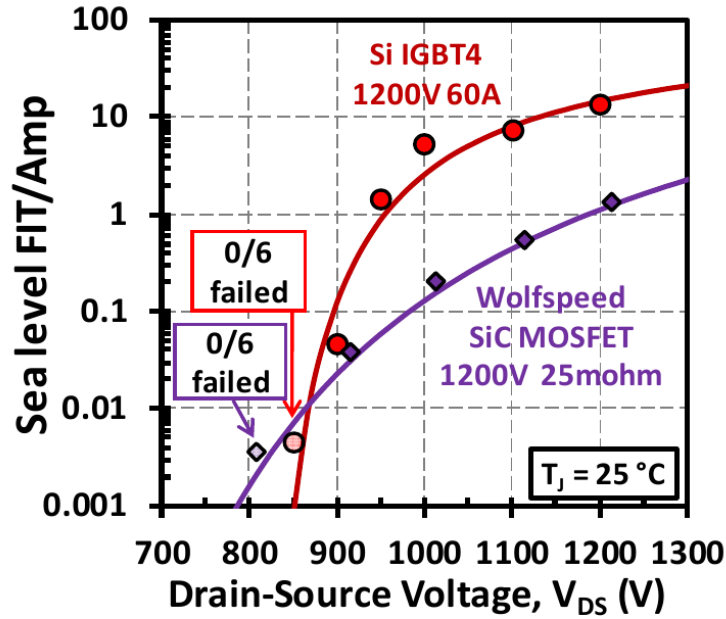


Figure 2.19: FIT/Amp versus V_{DS} for similarly rated 1200 V Wolfspeed SiC MOSFET (C2M0025120D) and 1200 V Si IGBT devices [97].

been proposed in many studies [84, 85, 100] that the SEB occurs in SiC MOSFETs due to the charge deposition followed by turn-on of the parasitic BJT, similar to mechanism which has been observed in Si MOSFETs [69–71]. The contribution of BJT on SEB will be discussed further later in this section.

As is the case with Si MOSFET, the source and the drain terminal of the SiC MOSFET are connected via pn-junction, also known as the body diode (Figure 2.20). At high drain bias voltages, the breakdown characteristics of the MOSFET are driven by the breakdown of the reverse biased body diode.

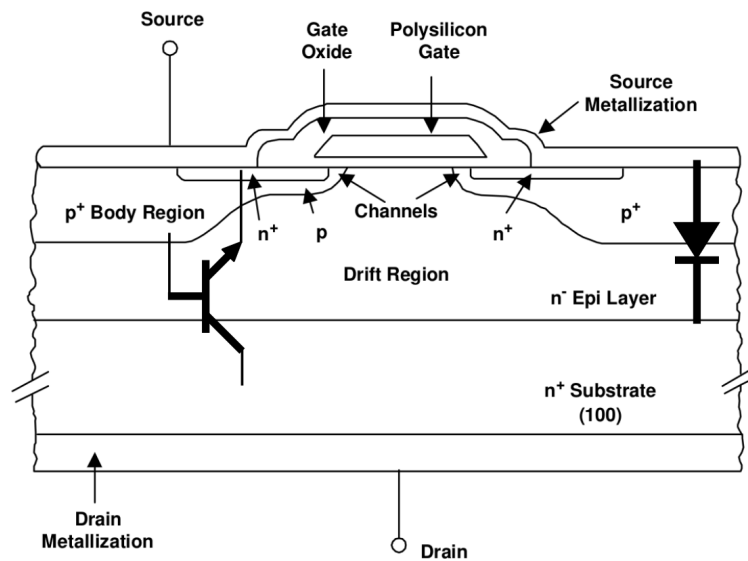


Figure 2.20: Cross-sectional view of power MOSFET with different regions and parasitic BJT and body diode structures. After [6].

Impact ionization Impact ionization is a charge multiplication process which occurs when charge traveling in the semiconductor material has enough energy to excite the electron of another atom to conduction band. If the electric field is strong enough, such charge can gain enough energy to further ionize more atoms in the material. Impact ionization rate is strongly electric field dependent and increases with increasing electric field. It has been found that impact ionization coefficient of SiC material is only marginally affected by temperature [101, 102].

Thermal runaway Thermal runaway occurs in semiconductor material, when the temperature-induced carrier concentration is high enough that the device is not able to block given voltage and the current in the device increases. This current further increases the temperature which in turn increases the current. Eventually the semiconductor material reaches its melting point causing device failure. Due to higher thermal conductivity and melting point of SiC compared to Si, SiC devices are expected to be less sensitive to thermal runaway.

Phenomena behind SEB

The contribution of parasitic BJT As mentioned in previous section, several studies suggest that the SEB mechanisms in SiC power MOSFETs is similar to mechanism in Si power MOSFETs.

In fact, Johnson et al. observed through laser testing and heavy-ion TCAD simulations that charge collection is enhanced when the laser pulse and ion track in TCAD is localized at the channel region of the MOSFET, where the parasitic BJT-structure is present. Charge collection, when laser is swept over the MOSFET structure, is location dependent but such behaviour is not observed with diode (Figure 2.21) [100].

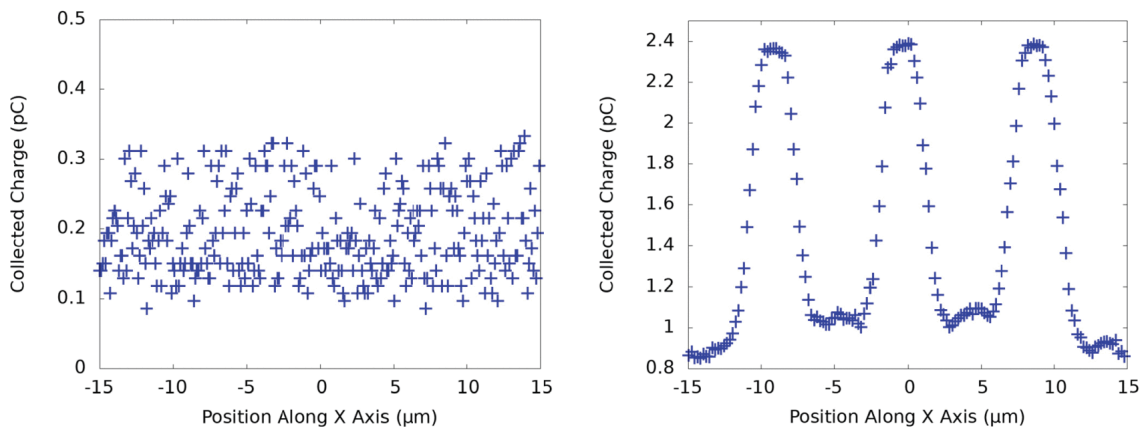


Figure 2.21: Collected charge of diode (left) and MOSFET (right) as a function of position of laser beam. Difference in collected charge response between diode and MOSFET is shown suggesting different charge amplification mechanism when sweeping the laser beam across the device structure. Devices were both biased at 50 V. Laser pulse energy was the same in both cases with wavelength of 481 nm resulting in 2.58 eV photon energy [100].

In addition, when increasing the bias, collected charge increases faster in MOSFET compared to diode (Figure 2.22) suggesting different charge amplification mechanism between these devices [100].

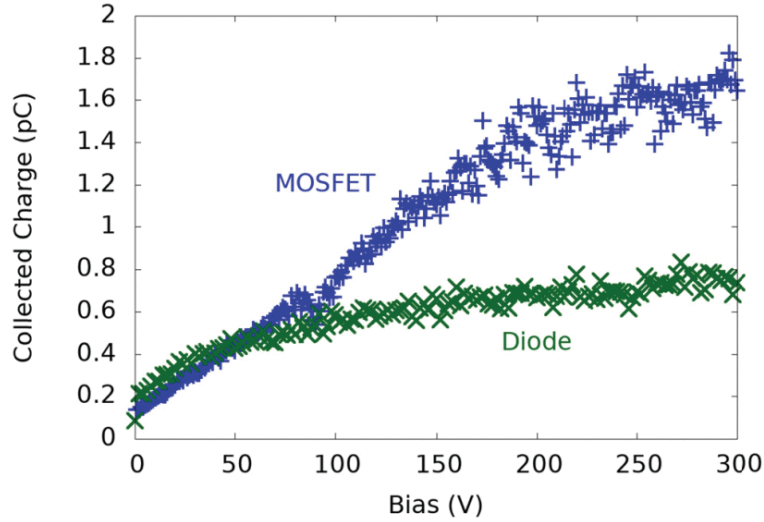


Figure 2.22: Collected charge due to laser radiation of diode and MOSFET as a function of applied bias voltage [100].

It seems that the impact ionization may play a role in the SEB triggering. In fact, based on the TCAD simulations by Witulski *et al.*, SEB mechanism was explained with combination of parasitic BJT turn-on and impact ionization. Sustaining current state was only obtained in simulations when impact ionization model was enabled [86]. Without impact ionization, a current transient induced by the impinging ion appeared and current level returned back to the pre-irradiation condition as illustrated in Figure 2.23, which also shows that applied drain bias voltage needs to be at sufficient level to induce SEB.

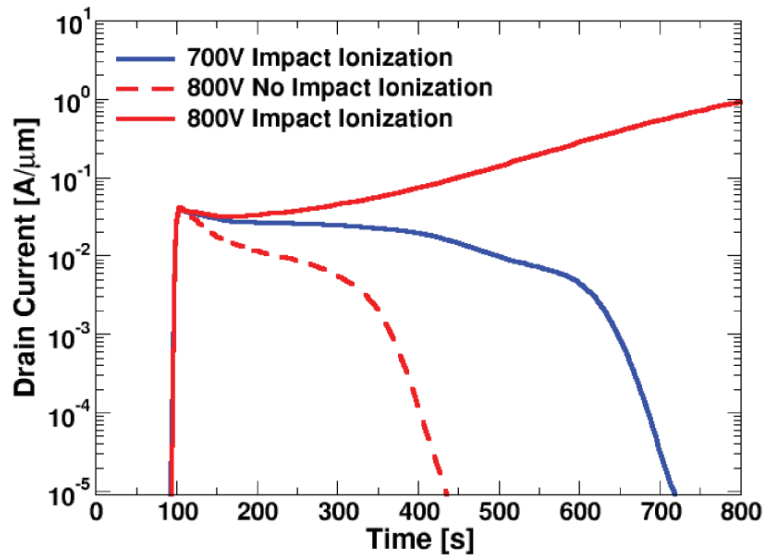


Figure 2.23: TCAD heavy-ion simulations of SiC power MOSFET with and without impact ionization. SEB occurs at 800 V when impact ionization is enabled [85].

However, if SEB in SiC occurs mainly due to the parasitic BJT turn-on, it should be expected to observe decreasing failure rate with increasing temperature. In fact, it has been observed that SiC BJT gain decreases with increasing temperature. The base current gain is observed to decrease 25% when increasing temperature from 22 °C to 122 °C as

illustrated in Figure 2.24 [103].

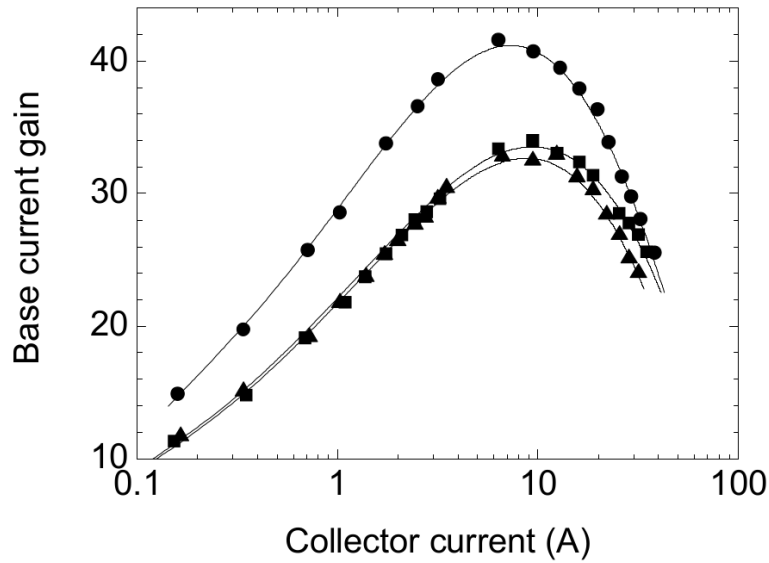


Figure 2.24: The base current gain of SiC power BJT as a function of collector current at different temperatures: 22 °C (circles), 122 °C (squares), 246 °C (triangles) [103].

Akturk et al. observed that neutron-induced failure rate of SiC MOSFETs is not dependent on the irradiation temperature [25]. They suggest that since the gain of bipolar transistor should decrease with increasing temperature, also the failure rate should decrease, which is not the case in their study. No differences in diode or MOSFET failure rate were observed between irradiation at room temperature (RT) and at 140 °C (blue triangles for RT and red circles for 140 °C in Figure 2.25).

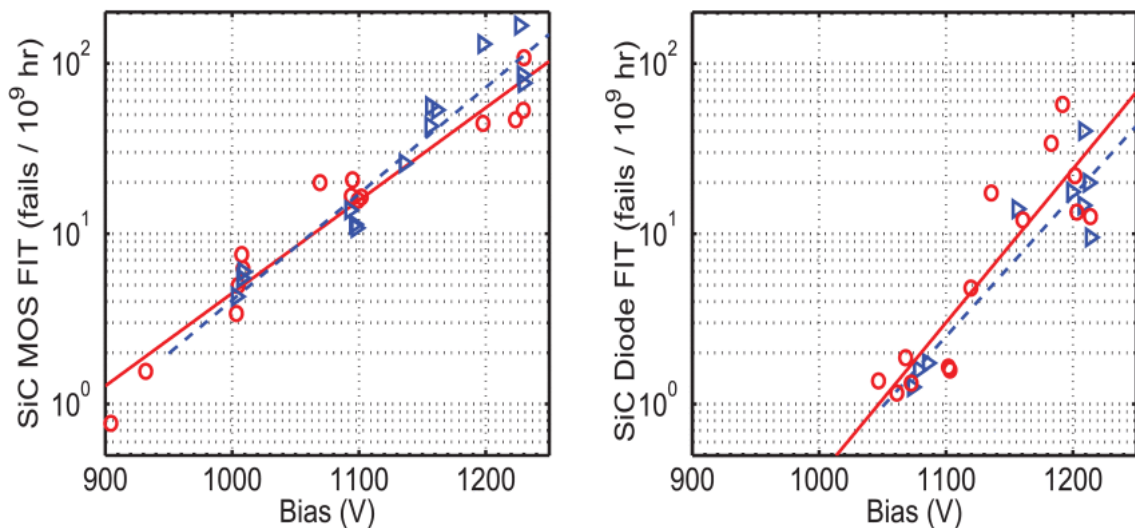


Figure 2.25: Temperature-dependent failure rates for SiC power MOSFET C2M0080120D (left) and SiC power diode C420120A (right). Blue triangles represent failure rate for irradiations at room temperature (RT) and red circles represent failure rate for irradiations at 140 °C [25].

Those results do not exclude the parasitic BJT model as a failure mechanism for SiC

MOSFETs but gives strong indicators that it might not be major contributor or at least not the only mechanism leading to failure of such devices.

The contribution of body diode As in the case of power MOSFETs, power diodes do not have parasitic pnp-structure. Therefore, it is not expected that the SEB in the diode occurs due to turn-on of parasitic BJT. Interestingly, very similar failure behaviours under neutron irradiation have been observed for both MOSFETs and diodes (Figure 2.26) [97].

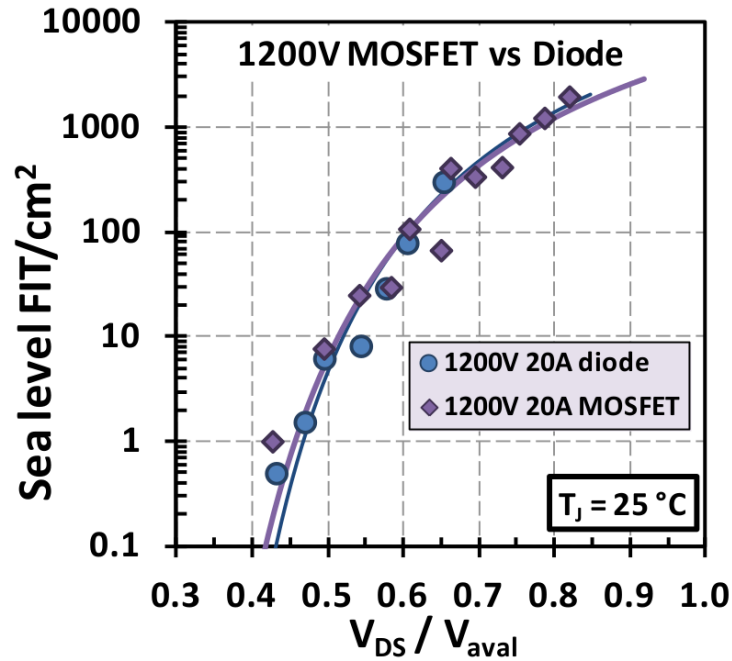


Figure 2.26: Active area normalized failure rate vs. avalanche rating normalized irradiation bias show universal behaviour between SiC MOSFET and SiC diode [97].

Similarities between failure mechanisms of MOSFETs and diodes have been observed also by Shoji et al. [94]. They observed through TCAD simulations that the SEB current and lattice temperature along the recoil track behave similarly over time in both diode and MOSFET (Figure 2.27). They also observed failure location through physical failure analysis which agree with the simulation results. Also, Asai et al. observed similar failure trend between SiC MOSFETs and SBDs Figure 2.28 [92]. No consistent differences between MOSFETs and diodes were observed. However, they observed a higher sensitivity to SEB for Si devices compared to SiC MOSFETs and diodes.

It seems that the failure rate is independent of the device type and is only dependent on the active area suggesting that SiC power MOSFETs and diodes exhibit the same failure mechanism. Due to presence of the diode structure in MOSFET and similarities in the observed failure rates between these devices, it would be justified to assume that the failure mechanism of MOSFET could be related to its body diode. Therefore, it seems that the turn-on of the parasitic BJT does not play an important role in the SiC MOSFET failure.

However, differences between MOSFET and diode behaviour have been observed as well. Johnson et al. performed two-photon laser technique supported with heavy-ion TCAD simulations and observed that above 100 V bias voltage, charge collected per laser

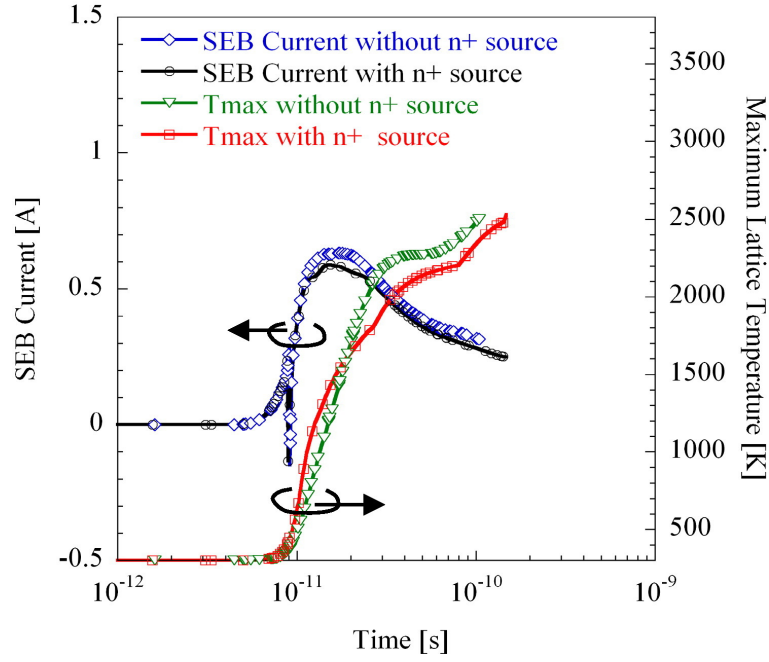


Figure 2.27: SEB currents and maximum lattice temperatures for SiC power MOSFET and diode simulated with TCAD [94].

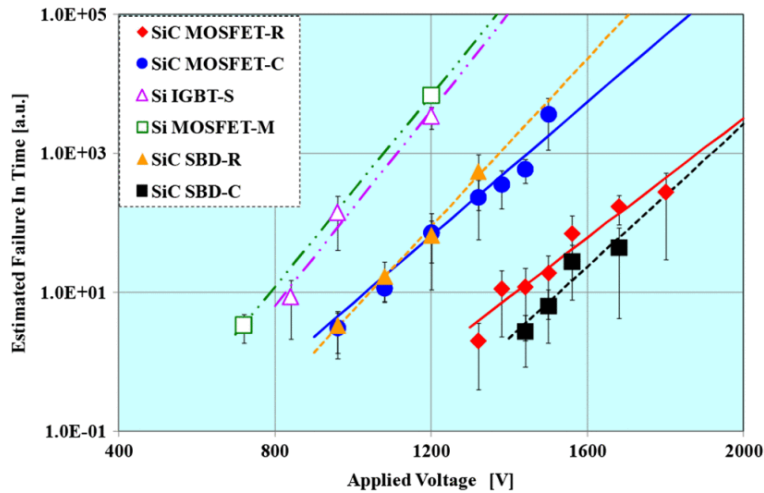


Figure 2.28: Estimated failure rates as a function of irradiation bias. Error bars represent 90 % confidence level [92].

pulse is greater for MOSFET than for diode and it increases with applied bias voltage suggesting that the charge amplification in MOSFET compared to diode originates from the parasitic BJT turn-on [100].

When comparing SiC MOSFETs with diodes, it has to be kept in mind that a vast majority of the commercial SiC diodes are based on the Schottky contact whereas the body diode in MOSFET follows the PN-diode structure. Therefore, if Schottky contact plays a role in the SEB sensitivity in a diode, the same mechanism might not be present in MOSFET body diode. Indeed, it was found by Kuboyama et al. that during heavy ion impact simulation with TCAD, the temperature at the Schottky contact exceeds the SiC melting point resulting in thermal runaway. While replacing the Schottky contact with PN-junction, the peak temperature observed at the junction 2150 K does not reach

the melting point of SiC. However, even the diode with PN-junction showed improved susceptibility to SEB, electric field at the anode contact exceeded 3 MV/cm, which is close to the critical field of SiC [104]. Therefore, while not as sensitive as Schottky contact, PN-junction of the body diode of MOSFET might still play a role in heavy ion induced SEB.

Sensitivity comparison between MOSFETs of different electrical ratings

Since the critical electric field in SiC material is higher compared to Si, same blocking voltage value of the device can be achieved with thinner drift layer, which result higher electric field value in the device structure.

Since the avalanche voltage (V_{aval}) is directly proportional to critical electric field (E_{crit}) of the material and the electric field is directly proportional to the applied voltage, the electric field over the drift layer (E_{drift}) is proportional to the avalanche rating normalized voltage and can be expressed as:

$$E_{drift} \propto \frac{V_{DS}}{V_{aval}} \quad (2.5)$$

Even though the SEB sensitivity is dependent on the absolute applied drain bias value during the irradiation exposure, it seems that the device active area and the electric field dominate the SEB failure characteristics.

Failure rate behaviour under neutron radiation spectrum has been compared (Figure 2.29) between various Wolfspeed SiC power MOSFETs with different voltage and current ratings (Figure 2.29a) and between SiC MOSFETs from different manufacturers (Figure 2.29b). It seems that the failure rate per device active area as a function of V_{DS}/V_{aval} has the same behaviour for devices with different ratings and from different manufacturers [97].

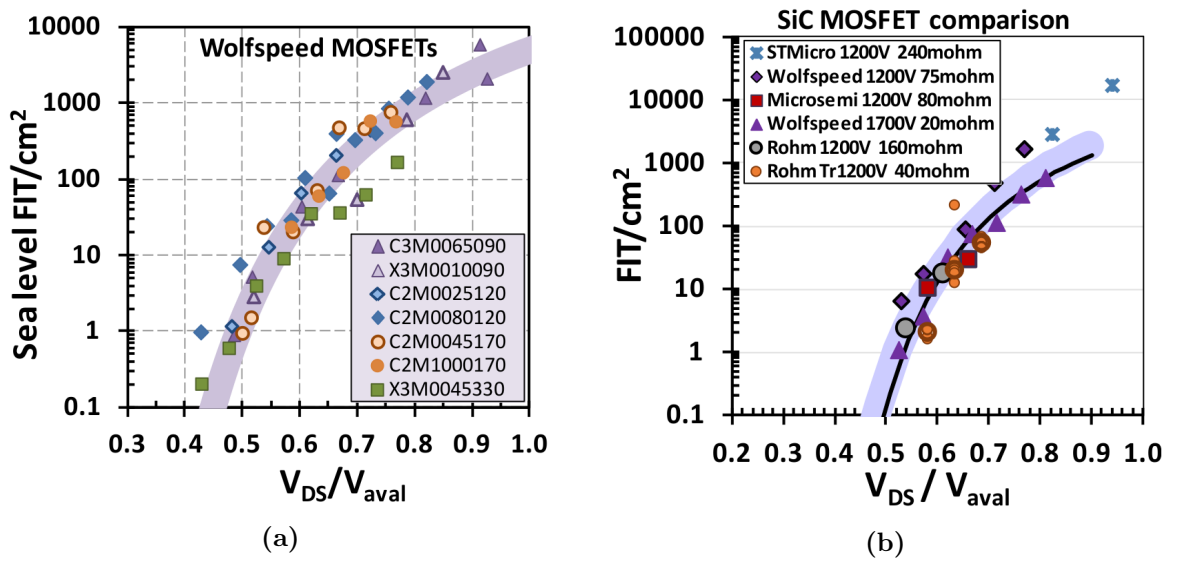


Figure 2.29: SEB failure rate per active area for Wolfspeed SiC MOSFETs as a function of normalized V_{DS} [97] for different device technologies (a) and for different manufacturers (b).

Trap assisted tunnelling (TAT) Strong bias voltage dependence of collected charge in SiC SBD during the ion strike and incomplete explanation of impact ionization model during the simulations, trap assisted tunnelling model has been suggested by Kuboyama et al. [88]. Such model is effective in SiC at high temperatures and under high electric field condition generated by heavy ion strike. Due to temperature dependence of such model, authors suggest that the high temperature at the proximity of ion strike location at Schottky barrier enhances the charge collection. Traps are generated by the ion strike along the e-h pair generation, induced current results local heating and finally carriers are generated by the TAT. More recently, this mechanism was also used by Makino et al. in order to explain anomalous charge collection in SiC SBDs [105].

Local lattice heating It has been proposed that due to the current induced by the generated charge by the ion strike, the temperature along the ion track can reach the melting point of SiC. Even though the thermal conductivity of the SiC is higher compared to Si, the charge generation and current along the ion track occurs in nanosecond scale. Therefore, in such short timescales the local heating and heat transport is only related to heat capacity and not to thermal diffusion [25]. This local heating results in thermal runaway and the degradation of integrity of the lattice structure and therefore leads to permanent failure.

Local heating phenomena is suggested also by Abbate et al. Due to the ion penetration through the device structure in SiC SBD, the temperature at the Schottky barrier exceeds the SiC melting point. It has been shown that this temperature can stay long enough to cause permanent damage to the SiC lattice [106, 107]. Simulated temperature distribution in Schottky power diode during the ion impact is illustrated in Figure 2.30 [107]. It can be seen that high temperature is localized in the ion impact position and at the metal-semiconductor interface and temperature reaches values well above the SiC melting point (3000 K).

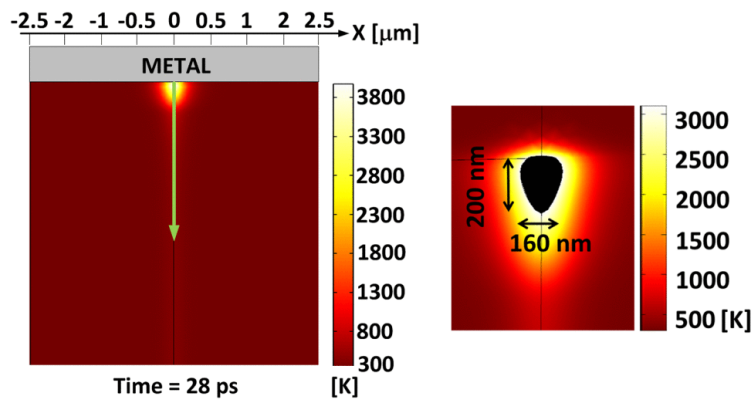


Figure 2.30: Temperature distribution in the SiC Schottky power diode during 240 MeV Br-ion strike simulated with COMSOL. $V_{DS} = 300$ V [107].

Maximum temperature of the SiC material is also dependent on the energy deposited in the material by the ion. Figure 2.31 shows the temperature during the ion strike with Br-ion energies of 60 MeV and 240 MeV which correspond to LET of approximately $27.9 \text{ MeV cm}^2/\text{mg}$ and $43.5 \text{ MeV cm}^2/\text{mg}$ in SiC at the metal-semiconductor interface respectively. Moreover, decrease in doping density results in lower maximum temperature in the lattice. This is due to lower conduction current which is limited by higher resistance

of lower doping density SiC region outside the ion impact region. It seems that especially at higher LETs, the lattice temperature is strongly dependent on the doping density [106].

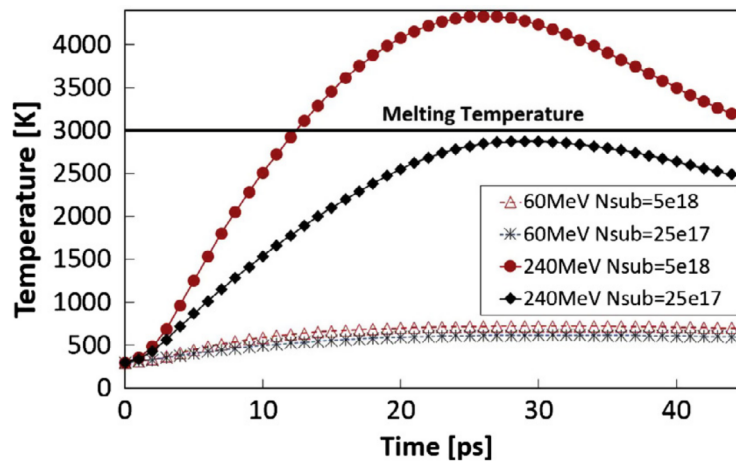


Figure 2.31: Temperature in SiC Schottky power diode during the Br-ion strike with two ion energies and two doping densities simulated with COMSOL [106].

Thermal runaway at the Schottky contact has also been simulated in [104]. Already at reverse bias voltage of 200 V (33 % of maximum rated reverse voltage), SiC Schottky diodes exhibited thermal runaway at the Schottky contact due to heavy ion impact during the simulations, which would result in device failure. When using 1.3 GeV Xe-ion, it results in LET of 62 MeV cm²/mg throughout the epitaxial layer. The thermal runaway in SiC Schottky diode is explained in 3 steps: 1) Electrons and holes generated along the ion track recombine at the Schottky contact resulting in elevated electric field due to the reduced carrier density. 2) Due to the elevated electric field, impact ionization is initiated. 3) Temperature at the Schottky contact increases resulting in thermal runaway [104].

Thermal damage after neutron irradiation has also been identified in SiC MOSFETs. Figure 2.32 shows cross-sectional SEM view of the neutron-induced SEB damage inside the SiC device. The damage in the polyimide passivation is due to expansion stress from within the device during SEB. The observed cracks in the drift layer inside the SiC lattice were formed when the maximum lattice temperature reached the sublimation temperature of SiC. Lower doping density and therefore higher resistance caused more thermal damage in the drift layer compared to n+-layer [94].

Heavy ion induced leakage current During heavy ion irradiation of SiC power MOSFET, permanent drain-to-source leakage current paths have been observed. Such SEE signature has been named single event leakage current (SEL), which has been observed in both gate and in body-diode regions of the MOSFET device [108].

Also SiC Schottky barrier diodes exhibit heavy-ion-induced leakage current increase with increasing ion fluence. Leakage current behaviour for different irradiation bias conditions as a function of ion fluence are presented in Figure 2.33.

It is suggested that the leakage paths are created by individual ions and the current is temperature dependent [89]. Leakage current increases with increasing applied bias voltage during the heavy ion exposure [89, 90, 109]. It has been observed that the normal incidence of the ion track is the worst case in terms of heavy ion induced degradation and that the degradation is significantly reduced above incident angle of 20° [109].

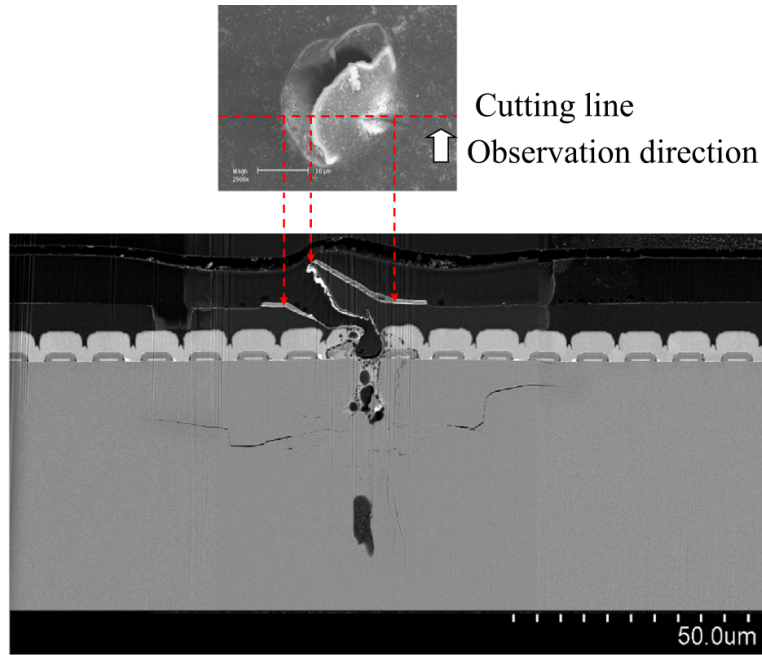


Figure 2.32: Cross-sectional scanning electron microscopy (SEM) image of neutron-induced SEB damage in 1200 V SiC power MOSFET [94].

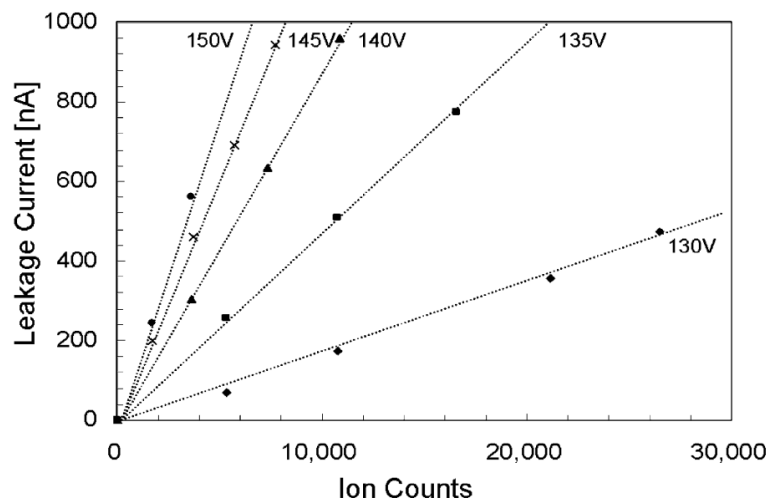


Figure 2.33: Measured leakage currents for several irradiation bias conditions for SiC SBD under Xe-ion ($LET = 73 \text{ MeV cm}^2/\text{mg}$) irradiation. Voltage values refer to irradiation bias condition and leakage current measurements were performed at 200 V bias voltage. [89].

Synergetic effect between DD and SEB As presented above, DD causes lattice defects which induce degradation in carrier mobility and noise in electronic devices. Therefore, DD is normally a source of device parameter degradation rather than a source of catastrophic failure. However, for SiC Schottky diodes, it has been observed that after sufficient amount of displacement defects under 63 MeV proton irradiation, device becomes more sensitive to SEB due to charge generation caused by single proton strike [110]. A schematic illustration of the effect is presented in Figure 2.34. The effect is similar to percolation path formation found in SiO_2 .

In addition, neutron radiation has been observed to create displacement damage in SiC material [60]. Similar actions are expected when irradiating SiC with protons. In

fact, higher defect density has been correlated with lower breakdown voltage of the SiC Schottky diodes. Defects can be either process related or stress- or radiation-induced defects.

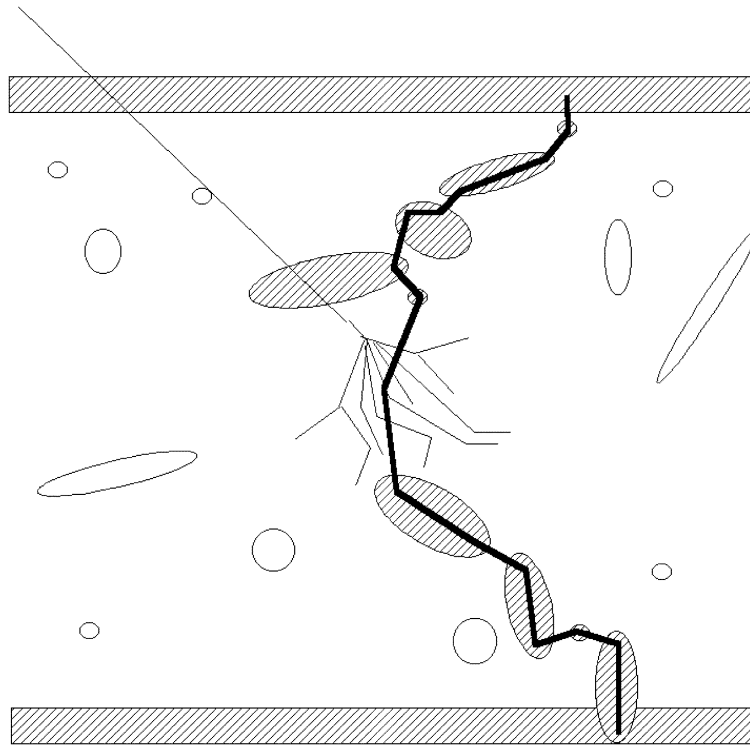


Figure 2.34: Illustration of how accumulated defects due to displacement damage and spallation reaction together can cause SEB [110].

Linear energy transfer (LET) dependence

LET defines the amount of energy lost by ionizing particle into the target material per unit of distance [111]. When dealing with particle radiation effects on electronics, unit for LET is most often expressed with $\text{MeV cm}^2/\text{mg}$. By using this unit, representation of LET is independent of the density of the target material, since it is already included in the unit. LET dependence on the SEB threshold for SiC MOSFETs under heavy ion irradiations is illustrated in Figure 2.35 for both experimental heavy-ion irradiation and TCAD simulated data. For LET values above $10 \text{ MeV cm}^2/\text{mg}$, the SEB threshold is relatively insensitive to LET. At low LET, the SEB sensitivity is highly dependent on both LET and applied bias voltage [85].

Also the TCAD simulated LET dependence is consistent with the heavy ion experiments. Figure 2.36 shows that in TCAD simulation, sustaining drain current state indicating SEB due to ion impact is achieved for LET of $20 \text{ MeV cm}^2/\text{mg}$ and above with 500 V drain bias voltage and impact ionization enabled in the simulation.

A summary of observed SEBs and their respective conditions are presented in Table 2.1. It seems that under energetic heavy-ion radiation, when LET is above $10 \text{ MeV cm}^2/\text{mg}$, SiC power devices fail around 50% of their rated V_{DSmax} or even below that regardless of the manufacturer and technology. It should be noted that most of the energetic charged particles in space environment have a LET less than $30 \text{ MeV cm}^2/\text{mg}$. Therefore, it is

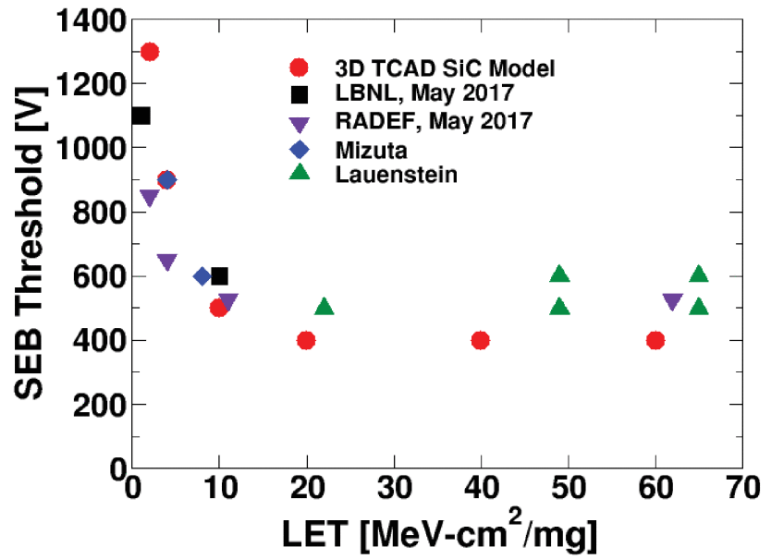


Figure 2.35: SEB Threshold of SiC MOSFETs as a function of LET of heavy-ion [86].

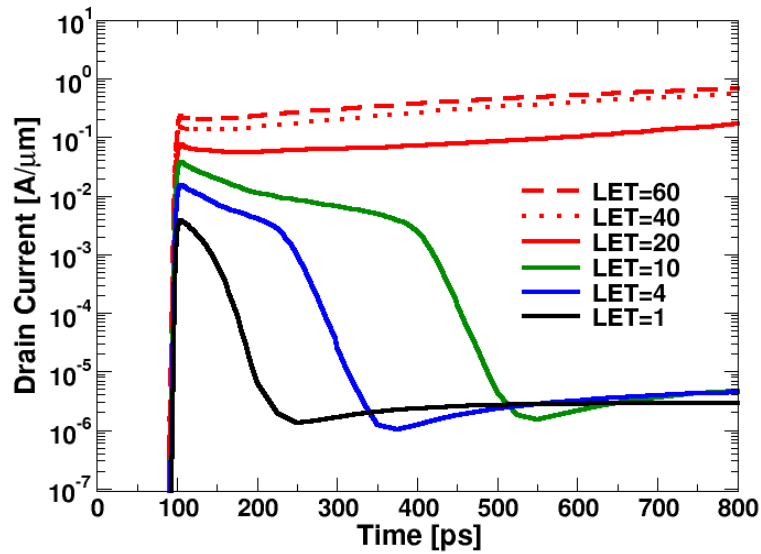


Figure 2.36: Drain current pulse for different ion LET values simulated with Synopsys Sentaurus. $V_{DS} = 500$ V during the simulation. Sustaining drain current indicating SEB due to ion impact is achieved for LET of 20 MeV cm²/mg and above [85].

evident that SiC power devices are sensitive to SEB in space environment and that even the common voltage bias derating of 50% in order to mitigate failure is not sufficient in many cases.

Table 2.1: A summary of heavy-ion-induced destructive SEB sensitivities of COTS SiC power technologies

| Part number | Technology | Ion | Energy (MeV) | LET (MeV cm ² /mg) | Failure voltage $\frac{V_{DS}}{V_{DSmax}}$ (%) | Study |
|-------------|------------|-----|--------------|-------------------------------|--|-------|
| C2M0080120D | MOSFET | Ar | 373 | 10.8 | 44 | [112] |
| CMF10120D | MOSFET | Xe | 22620 | 11.9 | 50 | [84] |
| | MOSFET | Xe | 996 | 65 | 40 | [113] |
| | MOSFET | Xe | 996 | 65 | 55 | [113] |
| | MOSFET | Xe | 996 | 65 | 45 | [113] |
| SDP06S60 | SBD | Ar | 137 | 16.7 | 53 | [88] |
| | SBD | Ag | 1110 | 49 | 42-46 | [113] |
| | SBD | Ag | 1110 | 49 | 40-42 | [113] |
| | SBD | Ag | 1110 | 49 | 38-46 | [113] |
| | PIN-diode | Ag | 1110 | 49 | 35-42 | [113] |
| | PIN-diode | Ag | 1110 | 49 | 24-30 | [113] |

2.3.2 SEGR mechanism in SiC devices

It has been stated that due to the higher critical electric field of SiC compared to Si, SiC power devices can be used in higher voltage conditions compared to Si devices of same physical dimensions. However, this applies only for the semiconductor material part of the device. When comparing SiC and Si power MOSFETs regarding their operating voltages, the higher voltage condition for SiC is considered only for V_{DS} . Actually, the gate voltage (V_{GS}) ratings between those devices are close to each other and same material type and thickness of the gate oxide are used for both device technologies. Therefore, as a first evaluation, strong differences in SEGR mechanisms are not expected. In both technologies, the SiO₂ is used as gate insulation material. However, since the crystal structure of the semiconductor material underneath the oxide layer is different, the oxide-semiconductor interface is different. It has been observed for MOS capacitors that LET of the striking ion affects the critical field required for SEGR. In Figure 2.37, the reciprocal of critical electric field of SiO₂ in MOS capacitors is presented as a function of LET of impinging ion. It seems that the slopes of the LET dependence in Figure 2.37 for SiC devices between different oxidation types and thicknesses are close to each other whereas the slope for Si devices differs. This suggests that SiC MOS capacitors are less sensitive to SEGR [114–116]. Difference in sensitivity could be explained by the differences in the oxide quality. However, critical fields for non-irradiated oxides (leftmost points in Figure 2.37, LET = 0) between SiC and Si are close to each other as well as the slopes for different oxidation processes. Therefore, the different material parameters of SiC could have an impact on inducing SEGR in SiC devices.

Considering the SEGR mechanism in Si MOS devices where the failure results from holes generated in the semiconductor layer moved towards and accumulated close to the oxide-semiconductor interface, it could be argued that the hole mobility, electron-hole creation energy and recombination rate affect the SEGR sensitivity. In fact, the hole mobility in SiC order of magnitude lower than in Si and the bandgap of SiC is higher than of Si [117]. Based on those data, it could be assumed that during the ion strike, less charges are generated, which result less holes accumulated on the oxide-semiconductor interface at the negative gate bias and/or positive drain bias. In addition, since the mobility of the holes in SiC is lower, less holes reach the interface before they are recombined in the

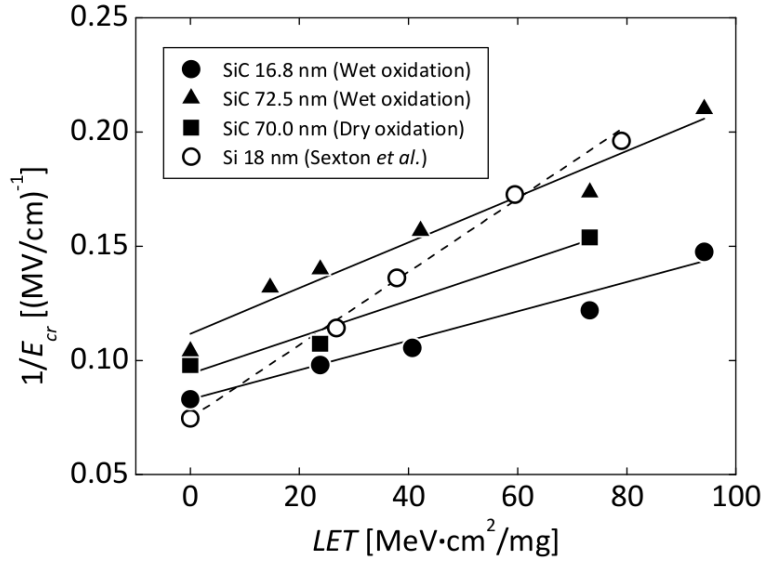


Figure 2.37: LET dependence of SEGR critical field for SiC and Si MOS capacitors [116]

semiconductor layer. Since there are less holes accumulated at the interface, the transient electric field over the oxide layer is lower and therefore could lower the probability for SEGR to occur.

2.3.3 SEB in GaN devices

Since commercial GaN power devices come in several different technologies, reported SEE sensitivities and failure mechanisms are strongly varied. In addition, several studies report radiation sensitivity tests performed on “home-made” devices. Different electrical characteristics and radiation responses between different manufacturing lots have been reported. Permanent leakage current increase has been observed in these studies even if no catastrophic failure was observed after heavy-ion exposure. Both increase in drain leakage current and sensitivity to catastrophic failures increase with increasing irradiation drain bias [15, 118–127].

GaN-based power devices have been reported to fail under heavy-ion interaction due to increased drain-to-source leakage due to accumulated positive charge under the gate leading to gate turn-on, so-called back-channel effect [15, 122, 124, 128]. Another explanation for enhanced charge collection mechanism for normally-on GaN HEMTs is associated with the bipolar effect. Electrons due to the ion strike are collected at the drain, leaving holes in the buffer region. This leads to injection of electrons from the source (emitter of the parasitic BJT) to the base of parasitic BJT. Injected electrons diffuse in the base and are collected at the drain (the collector of the BJT) [128].

Therefore, higher LET and higher angle of incidence increases the SEE sensitivity [124, 126]. Angle dependence has also been observed in [127]. In fact, it has been proposed that ions traversing in the direction between the source and drain is the worst case in terms of SEB sensitivity. It has been observed by several authors that the catastrophic SEE or strong increase in drain current occurs only with relatively high LET values. Van Vonno et al. did not observe any degradation on EPC parts at LET of 28 MeV cm²/mg at device surface when devices were biased at maximum V_{DS} . Drain leakage begins to increase with LET of 43 MeV cm²/mg and catastrophic failures were observed only at V_{DSmax} and with LET of 86 MeV cm²/mg [125]. Similar trend has been observed with Panasonic and GaN

Systems parts. With LET below $30 \text{ MeV cm}^2/\text{mg}$, devices show very little degradation even at the V_{DSmax} . With increasing LET, the V_{DS} needed for failure decreases [124, 126, 127].

Another mechanism for heavy ion induced catastrophic damage is observed when an ion traverses through the GaN layer and AlGaN buffer layer to the substrate creating a short between the drain and the substrate. Due to horizontal structure of GaN HEMTs, this type of failure is most likely to occur with normal incidence of the ion track with the device surface [127]. Schematic illustration of different failure locations are presented in Figure 2.38.

Even though, the mechanism for destructive SEE is not fully known, based on post-failure analysis of the devices, it has been observed that damage often occurs in the gate area due to the high drain current, which eventually leads to burnout [15, 126]. Typically, in GaN HEMTs, the drain side of the gate area has the highest electric field [129]. It has been proposed that an ion hit in this area may damage the gate structure such that the threshold voltage is lowered locally. Therefore the leakage current increases and produces structural changes in the AlGaN barrier of the gate area [15]. The current pulses induced by the ion strikes may cause damage to GaN power transistor. In fact, it has been observed that the drain current increases with increasing heavy ion fluence [120, 123, 125].

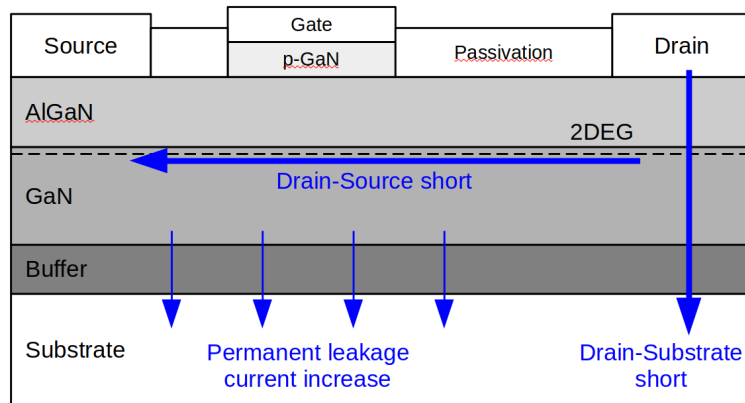


Figure 2.38: Simplified cross section representation of GaN HEMT and reported failure mechanisms due to the heavy ion irradiation.

SEEs in GaN HEMTs have also been studied through TCAD simulations [130, 131]. It has been proposed that the SEE is caused by the rupture of the dielectric passivation layer when heavy ion strikes near the field plate edge [130]. Such mechanism has also been identified experimentally [119].

Harris et. al. report no destructive failures nor significant parameter degradation on RF normally on GaN HEMTs under heavy ion irradiations. Devices were irradiated with Xe and Kr ions with several energies ranging from 391 MeV to 2530 MeV. The high SEE robustness is explained by the high leakage current of the parts compared to injected current by the heavy ion strike [132]. Similar high robustness for normally-off devices was observed by Bazzoli et al. who observed slight drain leakage current increase with observed gate damages with high LET ions [133]. Summary of heavy ion induced failure conditions for commercially available GaN HEMTs is given in Table 2.2.

Few studies on neutron-induced effects on GaN HEMTs report only parameter degradation such as decrease in transconductance and drain current and increase in gate leakage

Table 2.2: A summary of destructive SEE sensitivities of COTS GaN power HEMTs under heavy ion exposure

| Part number | Ion | Energy (MeV) | LET (MeV cm ² /mg) | Failure voltage $\frac{V_{DS}}{V_{DSmax}}$ (%) | Study | Remarks |
|--------------|-----|--------------|-------------------------------|--|-------|-------------------------------|
| PGA26E19 | Xe | 443 | 52.9 | 63 | [127] | |
| PGA26E19 | Kr | 315 | 30.6 | 77 | [127] | |
| PGA26E19BA | Ag | - | 43.6 | 54 | [124] | |
| GS66516T | Ag | - | 43.6 | 38 | [124] | |
| GS61008P-E03 | Ag | - | 43.6 | 40 | [124] | |
| EPC2014 | Xe | 3275 | 51 | - | [15] | No fail at V_{DSmax} (40 V) |
| EPC2014 | Kr | 2125 | 21 | - | [15] | No fail at V_{DSmax} (40 V) |
| EPC2001 | Xe | 3275 | 51 | 40 | [15] | |
| EPC2001 | Kr | 2125 | 21 | 100 | [15] | |
| EPC2012 | Xe | 3275 | 51 | 20 | [15] | |
| EPC2012 | Kr | 2125 | 21 | 100 | [15] | |
| EPC1007 | I | 276 | - | 90 | [123] | |
| EPC2012 | I | 276 | - | 45 | [123] | |

current [134–136] up to 1×10^{15} cm⁻² neutron fluence and modest negative shift in threshold voltage [137] after 2×10^{10} cm⁻² neutron fluence. No neutron-induced catastrophic failures on GaN HEMTs have been reported.

2.4 Testing facilities and methods used for assessing reliability of emerging power technologies under radiation

2.4.1 Principle test methodologies to assess the SEE sensitivity of power devices

Since the target applications of power devices are widespread, they are exposed to different stressors in different application environments. Therefore, reliability test standards and procedures for different application environments have been developed. Although, these are originally written for silicon technologies, they are used for testing emerging power technologies as well for example GaN technologies [15]. General aspects of SEE testing are applicable to GaN devices but the test conditions might need modifications depending on the technology under test [138]. As mentioned earlier, GaN device technologies are still widely varied and large variation in parameters means also variation in reliability data. On top of that, so far COTS GaN power devices have shown significant lot-to-lot variability, which makes the qualification process more challenging [139].

In this section, test standards and methods for reliability testing of power devices in space and atmospheric radiation environment are introduced while addressing the critical points which are still lacking within these methods.

Space environment

Common test standard for testing power devices used in space applications follows the MIL-STD 750 method 1080 [140]. It gives a description of the test procedure, instrumentation and test circuit (Figure 2.39) as well as description of the radiation environment for SEB and SEGR testing. Another testing guideline is provided by ESCC 25100 test standards [141]. It follows mainly the aforementioned MIL-STD 750 with some additional information regarding the test setup and data-analysis.

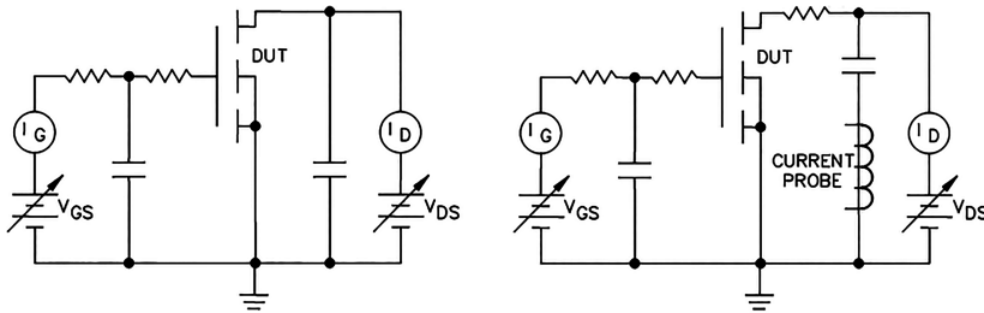


Figure 2.39: Schematics used for SEE testing of power transistors in a) destructive mode and b) non-destructive mode [140]

When investigating the radiation sensitivity of the commercial off-the-shelf (COTS) components, it has to be noted that the packaging of the component or the system can inhibit the beam to reach the active volume of the device. In the most cases, it is important to know, what is the actual radiation environment in the active volume of the component. This is especially of concern with heavy ion irradiations, since the penetration range of the ions at the most of the irradiation facilities has same order of magnitude than the dimension of the device. Also, since the thickness of power device active volume is comparable to the penetration range of the ion, variation of the amount of deposited energy along the track has to be taken into account. On top of that, it needs to be ensured that the ion penetrates the whole structure, if needed. Commonly used tool for calculating ion penetration ranges and deposited energy into the material is SRIM [142].

In order to assess the sensitivity of power devices to radiation induced failure, voltage bias condition during irradiation has to be defined. Power transistors and diodes are used to block voltages of kilovolts and deliver currents of tens of amps. During the single event testing, these devices are tested by considering the worst case bias condition in terms of SEE sensitivity. Therefore, the devices are usually tested in off-mode with applied drain bias or in a worst-case in blocking state [143]. The particle interaction does not always lead to destructive burnout during the exposure. Therefore, it is important to assess, if the radiation caused damage to the device structure by performing electrical stress after the irradiation. Standard method is to test with grounded gate ($V_{GS} = 0\text{ V}$), which means that the gate dielectric is not under electric field during the irradiation. However, it is important to perform gate voltage sweep i.e. post-irradiation gate stress (PIGS) in order to ensure functionality of the irradiated devices [140].

Methodology for SEGR radiation hardness assurance (RHA) for power MOSFETs has been developed by Ferlet-Cavrois et al. Sufficient number of devices have to be tested in order to perform meaningful statistical analysis. Probability of survival of the tested device in the radiation environment with defined confidence levels can be extracted from

the measured statistical distributions [143].

Atmospheric environment

To date, test standard for neutron-induced failures on power devices in atmospheric environment does not exist. Even though, test board described in [140] might be applicable to neutron testing, those standards introduced in previous section do not provide a standard way for extracting reliability parameters in neutron environment. Therefore, apart from the test setup, they are not adapted to neutron testing, which needs statistical approach due to stochastic nature of neutron-matter interaction. JEDEC publication JEP151 [144] describes test procedure for terrestrial neutron testing of power devices providing also information about sample selection, beam requirements and test setup. However, it still lacks information of how to calculate reliability parameters, definition of sufficient sample size and how to define failure rates, when all the devices are not failed during the irradiation testing. Failure rates can also be calculated after JEDEC standard JESD85 based on the number of failures, total number of devices and the acceleration conditions [145].

In this work, in Chapter 3, a methodology for reliability parameter and failure rate calculation for power devices under neutron environment is proposed. It is based on applying Weibull analysis on the failure data [146] followed by extraction of mean fluence to failure and failure rate in both avionic and ground level applications.

Accelerated vs. storage testing for atmospheric radiation environment

A straightforward method to determine the failure rates of power devices under terrestrial radiation is to store a number of devices under voltage bias while monitoring the number of failures over time. Such approach is suitable for measuring failure rates 1×10^4 Failure in time (FIT) and above and if large number of devices are available and storage times of several months are acceptable [147]. However, when measuring failure rates in order of 100 FIT, an artificial radiation source with increased particle flux is needed. Such approach is called accelerated testing. FIT is a unit of failure rate and 1 FIT corresponds in one device failure in 1×10^9 device hours [145] and will be presented in detail in Section 3.2.2. Energy spectrum used in such testing should be similar to terrestrial radiation environment but flux increased with appropriate acceleration factor [147, 148]. It should be noted that terrestrial radiation environment can have neutrons exceeding 1 GeV energy which are rarely attained in irradiation facilities. However, such energies in atmospheric environment are not significant regarding the destructive failure of power devices, since their flux is relatively low compared to lower energies.

2.4.2 European test facilities suitable for SEE testing of power devices

As mentioned in previous section, while testing for SEE in power devices, sufficient range of impacting particles has to be ensured either by long range particles or decapsulation of the device. Moreover, adequate LET has to be reached in order to ensure sufficient amount of generated charge inside the device volume. In the following, European test facilities which are suitable for power electronics SEE testing, are introduced.

ChipIr

ChipIr facility is located in Rutherford Appleton Laboratory, UK. It is a beamline at the ISIS spallation source with an atmospheric-like neutron spectrum with 10^9 acceleration factor compared to ground level. The beamline is dedicated for accelerated SEE testing of electronic components and systems especially for avionic and terrestrial applications. The nominal neutron flux is $5 \times 10^6 / (\text{cm}^2 \text{s})$ for neutron energies $E_n > 10 \text{ MeV}$ with a $7 \text{ cm} \times 7 \text{ cm}$ rectangular beam at the test position. In the future, the beam size is supposed to increase up to $50 \text{ cm} \times 50 \text{ cm}$. Irradiations take place in air and at room temperature [149].

GANIL

GANIL facility is located in Caen, France. There is a beamline applicable for electronic component testing which provides heavy ion beam with energies up to 60 MeV/n . With such energy it is possible to reach 1.2 mm in Si. Therefore, testing of encapsulated devices might be possible in some cases. Change of ion type during a test campaign is not possible [150].

RADEF

RADIATION Effects Facility is located in University of Jyväskylä, Finland. It is a part of the Accelerator laboratory of Department of Physics. It offers variety of heavy ions as well as low energy protons ($E_p < 55 \text{ MeV}$). Heavy ion energies of 9.3 MeV/n , 16.3 MeV/n and 22 MeV/n are available. Heavy ion and proton irradiations are performed in air or in vacuum mode. In addition, electron and X-ray beams are also available in the facility. Change of ion type during the irradiation campaign is possible [151]. Due to the modest energies of the heavy ion beam, decapsulating or thinning of the package is required in order to reach the sensitive volume of the device.

AGORFIRM

The AGOR Facility for Irradiations of Materials (AGORFIRM) is an activity of KVI CART and is situated on the University of Groningen, Netherlands. Cyclotron is used for irradiations with protons, alphas and heavy ions in air and high LET irradiations in vacuum. AGORFIRM provides protons up to 190 MeV , lighter ions (helium to oxygen) at 90 MeV/n and heavier ions from carbon to xenon at 30 MeV/n . It is also possible simulate the solar proton spectra ranging from 60 MeV to 184 MeV [152].

UCL

UCL is a cyclotron facility in Université catholique de Louvain, Belgium. They provide variety of heavy ions up to energies of 9.3 MeV/n . The beam flux is variable between a few particles $/(\text{cm s})$ and $1.5 \times 10^4 / (\text{cm s})$. The beam flux can be modified from the user station. UCL provides protons up to energy of 62 MeV [153].

CHARM

CHARM is an irradiation test facility which provides mixed radiation field. The mixed radiation field is generated through the interaction of a 24 GeV proton beam and the

target. The variety of particle radiation fields available at the facility is representative of several radiation environments allowing large acceleration factors, up to 1×10^{10} with respect to the ground level applications [154, 155].

PIF-PSI

PIF (Proton Irradiation Facility) at Paul Scherrer Institut (PSI) allows conducting experiments with realistic space proton environment as well as with mono-energetic beams up to 230 MeV. Irradiations are performed in air and the beam diameter is 9 cm [156].

Summary

The summary of different irradiation facilities and their parameters are summarized in Table 2.3.

Table 2.3: Summary of European test facilities suitable for SEE testing of power devices

| Facility | Particle type | Beam size | Max energy (MeV/n) | Remarks |
|----------------------|---|-------------------------------|------------------------------------|---|
| ChipIr [149] | Neutron | $8 \times 8 \text{ cm}^2$ | 500 | Atmospheric-like spectrum |
| GANIL [150] | Ar, Kr, Xe, Pb | $4 \times 50 \text{ cm}^2$ | 60 | Sweeping beam in air |
| RADEF [151] | Proton, O, Ne, Ar, Fe, Kr, Xe | $5 \times 5 \text{ cm}^2$ | 55 (proton), 22 (heavy ion) | In air and in vacuum testing |
| AGORFIRM (KVI) [152] | Proton, He, C, O, Ne, Ar, Kr, Xe | $3 \times 3 \text{ cm}^2$ | 190 (proton), 30-90 (heavy ion) | Possibility for solar proton spectra |
| UCL [153] | Proton, C, Ne, Al, Ar, Cr, Ni, Kr, Rh, Xe | $2.5 \times 2.5 \text{ cm}^2$ | 62 (proton), 9 (heavy ion) | |
| CHARM [154] | Mixed field | | | Irradiation chamber with different positions for different irradiation fields |
| PIF-PSI [153] | Proton | 9 cm (diameter) | 230 | |

2.5 Aging effects on power devices

Power electronics devices, such as power MOSFETs, power diodes and IGBTs are applied in variety of power electronics systems such as in switching converters and motor drivers, where high frequency switching and high voltage and current levels are required. In such applications, power devices are exposed to stress which causes device aging and eventually possible device failure. Aging of the device may cause change in device characteristics, which can result in degradation and failure power system. In some extend, these changes in characteristics can be exploited in estimation of remaining useful life (RUL) in device prognostics [157]. In this chapter, the most common aging effects on the power electronics components are introduced focusing on effects which affect the electrical parameters of the devices.

2.5.1 Aging effects on Si power devices

When switching power MOSFET between on and off-state, voltage at the gate terminal is varied between negative and positive voltages. When voltage is applied on the gate, an electric field is formed across the dielectric layer which causes degradation of the dielectric layer over time. Electric field in the oxide layer causes charge injection into the insulator layer which eventually, after sufficient amount of injected charge, can affect the device performance. Si-based power MOSFETs have been reported to suffer from shift in threshold voltage due to the electrical aging [157, 158]. Such aging leads charge trapping in the gate oxide volume which is the main contributor in V_T shift. On top of that, charge trapping may occur at the oxide-semiconductor interface affecting the carrier mobility in the channel. This can have an effect on the transconductance (g_m) and channel on-state resistance (R_{ON}) [159, 160]. In addition to the electrical effects, device operation may cause thermomechanical stress which can lead to delamination at the die attach and disconnection or breaking of the bond wires due to overheating and subsequent thermal expansion [161].

2.5.2 Aging effects on SiC power devices

SiC power MOSFETs have been reported to suffer from electrical and thermal stress resulting in instability in threshold voltage and in drain current [162–164]. Shifting of the threshold voltage of the MOSFET due to applied gate-bias stress is called threshold voltage instability. Typically, a positive gate bias results in a positive shift in V_T and a negative gate bias results in a negative shift while gate bias is applied at room temperature with electric field ranging from 2 MV/cm to 3 MV/cm [163].

Moreover, the temperature during the stress has also an effect on the device electrical characteristics. The effect of high temperature gate bias (HTGB) stress on IV -characteristics of SiC MOSFET is presented in Figure 2.40 with positive bias-temperature stress (PBTS) and negative bias-temperature stress (NBTS).

It has been proposed that the electrical stress induced shift in V_T is related to tunnelling of electrons to and from the near-interfacial oxide traps. When negative voltage is applied on the gate, electrons trapped in the near-interfacial oxide traps are pushed away from the oxide resulting in positively charged traps and negative shift in V_{th} . Under positive gate bias, electrons from semiconductor are able to tunnel into the oxide occupying traps and resulting positive shift in V_{th} [165]. Shift in V_T is also dependent on the temperature during the stress. The effect of temperature on the shift is presented in Figure 2.41.

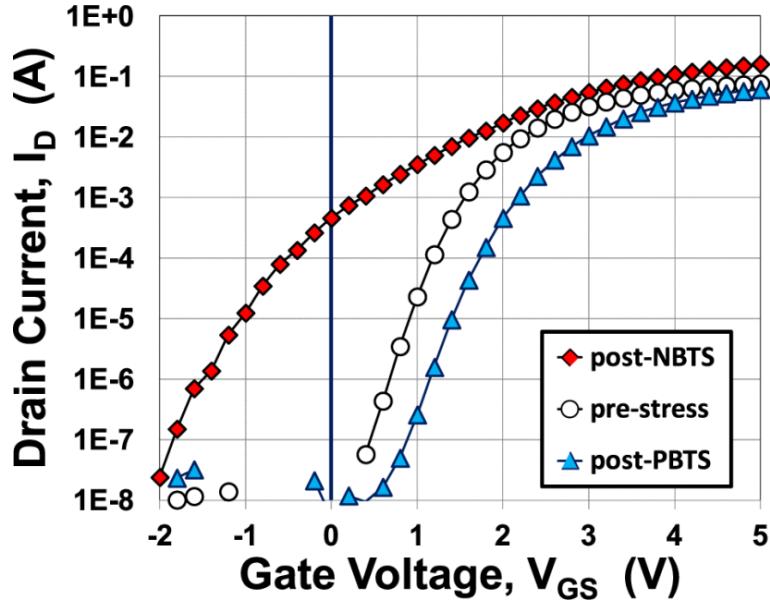


Figure 2.40: The effect of gate bias stress on the IV-characteristics under HTGB at 150 °C. NBTS: 100 h, $V_{GS} = -15$ V, 150 °C; PBTS: 600 h, $V_{GS} = 15$ V, 150 °C [163]

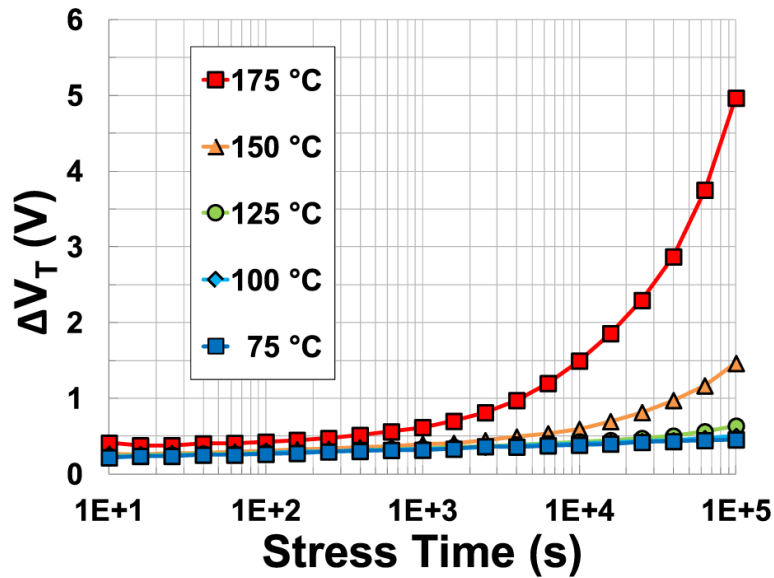


Figure 2.41: Temperature dependence of the threshold voltage shift as a function of applied stress time [163].

We can see that the ΔV_T increases not only with time but also with increasing temperature. Since the tunnelling itself is not expected to increase with temperature as much as the shift in V_T is suggesting, it is suggested that additional near-interfacial traps are activated in higher temperatures which participate in tunnelling [163]. Since the fundamental structures of the Si and SiC MOSFETs are similar, it could be expected that their aging response would be somewhat similar. Interestingly, there are some differences between those two technologies. Degradation of $I_{DS}V_{GS}$ and $I_{GS}V_{GS}$ caused by Fowler-Nordheim (FN) stress behave differently for SiC MOSFET compared to Si MOSFET. Especially, in the FN stress experiments, the gate leakage current for SiC MOSFET has been observed to increase monotonically until the oxide breakdown while for Si MOSFET the behaviour is opposite [166]. Even if no catastrophic failure occurs due to device aging, it can have an

effect on the application in which the device is implemented. When device is in off-state, negative ΔV_T can result in leakage current which results in increased power consumption in MOSFET. In case of positive ΔV_T , increased R_{ON} can result in reduction in system output efficiency [166].

2.5.3 Aging effects on GaN power devices

Normally-off GaN HEMTs are exposed to electrical stress in on- and off-state during the operation. While device is in on-state, a positive voltage is applied on the gate and charge trapping may occur in the region under gate. While device is in off-state and high drain-to-source voltage is applied, few degradation mechanisms are present [167]. Electrical stress-induced degradation mechanisms are illustrated in Figure 2.42.

When GaN HEMT is turned on by applying positive V_{GS} , it results in electric field across the p-GaN and AlGaIn layers. This electric field may result in breakdown of the buffer layer. In fact, similar to MOSFET gate oxide breakdown, time-dependent breakdown of gate layer has been observed for GaN HEMTs when applying positive voltage on the gate until breakdown occurs [167]. The mechanism for the gate breakdown has been discussed and several mechanisms have been proposed in [168–170].

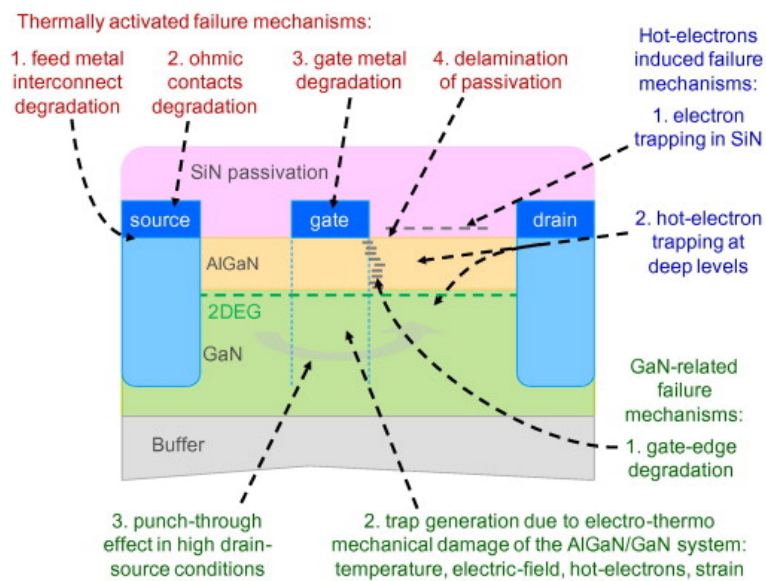


Figure 2.42: GaN HEMT degradation mechanisms [171].

2.6 Conclusions

Different radiation effects on power devices were introduced and discussed. Several mechanisms are present within the radiation-induced failure and degradation of the WBG devices. A sensitivity to destructive SEEs is still a major concern for SiC power devices in both space and atmospheric environments. On top of that, non-destructive, radiation-induced leakage currents have been observed for both GaN and SiC technologies, which can further limit the usage of such devices in harsh environments.

Radiation-induced failure mechanisms for WBG power device are still not fully known and further studies are needed in order to exploit the superior material properties of such

devices in critical applications.

A review of the radiation test methodologies show a lack of test standard for WBG power devices under atmospheric environment and a methodology for that will be proposed in the next chapter. A brief summary of European radiation test facilities was given focusing on the most important parameters regarding the radiation testing.

On top of the radiation-induced damage, it has been shown that WBG devices suffer also from the electrical stress during the device operation. Threshold voltage instability and increase in on-state resistance are of concern and they can affect the power system efficiency.

Chapter 3

Radiation and aging effects on wide bandgap power devices: The experimental study

3.1 Introduction

When operating power electronics devices in radiation environment, they are exposed to radiative stress which can cause loss of functionality of the system due to degradation or complete failure of the device. Several studies report catastrophic failures of Si-based power devices due to single event effects. More recently, sensitivity of SiC MOSFETs and GaN HEMTs to catastrophic failures have been reported. Majority of studies which reported radiation induced radiation effects on such devices, indeed focus on catastrophic effects, such as single event burnout (SEB) and single event gate rupture (SEGR).

However, as for any system, reliable operation of power electronics device is needed for full desired lifetime of the system. Therefore, on top of the sensitivity to catastrophic failures, it is important to assess if non-destructive radiation effects cause reduction in lifetime of these devices. Especially, the effect of non-destructive single-event effects on device long-term reliability have not been extensively studied.

On another point of view, during their operation lifetime, electronic devices are exposed to various stress modes. On top of the radiative stress, devices exhibit electrical stress which affect the device characteristics during its operation lifetime. Therefore, when assessing the power system lifetime, it is important to know, if radiation sensitivity of the device changes due to aging during device operation.

This work focuses, from a statistical point of view, on the impact of neutron irradiation on short and long term reliability degradation of a given SiC power MOSFET technology, especially focusing on neutron-induced SEB and long-term reliability degradation due to the non-destructive radiation effects. Long-term reliability of the irradiated devices is studied by exposing devices to electrical stress after they have been irradiated. Also, radiation sensitivities of fresh and electrically stressed devices are compared in order to find out if the electrical stress experienced by the device during its operation, has affected the radiation sensitivity. The purpose of the electrical stress is to accelerate aging process by creating defects in the device structure in an accelerated manner. On top of the experimental study, we also perform TCAD simulations in order to investigate and highlight the mechanism of both radiation and stress induced degradation.

As pointed out in Section 2.4.1, a standard methodology for reliability calculation for

neutron-induced failures in atmospheric environment does not exist to date. Therefore, a new methodology based on experimental investigations on reliability is required. For this, we propose a new methodology based on the Weibull statistics.

In addition to SEE studies, TID tests were performed for both SiC MOSFET and GaN HEMT technologies. In order to assess the effect of aging on radiation sensitivity, we performed pre-irradiation electrical stress for SiC MOSFETs. The goal is to determine the TID sensitivity and to compare the results with fresh devices.

In this chapter, the method for lifetime analysis is presented followed by test setup description. Then the different performed experimental studies are presented including statistical reliability analyses and TCAD simulations. Finally, an effect of irradiation-induced destructive failure on power system functionality is studied.

3.2 Reliability analysis: the methodologies

3.2.1 Reliability parameter extraction through Weibull analysis

The Weibull distribution is widely used in reliability and life data analysis [146]. In this study, by analysing its parameters, the Weibull distribution allows to model different failure modes and lifetime behaviour under neutron irradiation. In our case, we deploy the Weibull analysis for destructive failures. For that, experimental failure points are plotted as a function of neutron fluence. Different parameters are then extracted. Methods are presented and discussed in following sections. The general form of the Weibull cumulative distribution function (CDF) is given in Equation (3.1)

$$F(x) = 1 - e^{-\left(\frac{x-\gamma}{\eta}\right)^\beta}, \quad (3.1)$$

where x usually represents time. As described, in our study, the variable x represents particle fluence while β , η and γ are the shape, scale and location parameters respectively.

However, the most widely used distribution for life data analysis is 2-parameter Weibull distribution (Equation (3.2)), in which the location parameter γ is set to zero. The location parameter indicates the shift of the distribution location which essentially means that failures cannot occur before γ . Therefore, there should be physical or engineering reason, which states that failures will not occur before given γ and therefore justifies the location shift.

In 1-parameter version of the Weibull distribution, β is set to some defined value, which is based on historical failure data and/or knowledge of the physical mechanism of the failure. Since β is known and set, only parameter that is extracted from 1-parameter Weibull is the scale parameter, η . One parameter approach can be useful if the sample size is small and there is a reasonable assumption for β . Also one-parameter model is used if the data have no failures and therefore no β can be extracted.

In the next two sections, two different methods for extracting the parameters are presented and compared.

Linear regression model

First, we define the reliability parameters from failure data by performing linear fit in the dataset. The 2-parameter Weibull distribution is used which CDF is given in Equation (3.2).

$$F(x) = 1 - e^{-\left(\frac{x}{\eta}\right)^\beta}, \quad (3.2)$$

A change of variables is performed in order to linearize the 2-parameter Weibull-function:

$$\begin{aligned} -\ln(1 - F(x)) &= \left(\frac{x}{\eta}\right)^\beta \\ \ln(-\ln(1 - F(x))) &= \beta \ln x - \beta \ln \eta \end{aligned}$$

Since we are interested in the reached fluence when the device fails, x -variable of the distribution is therefore replaced with fluence Φ :

$$\ln(-\ln(1 - F(\Phi))) = \beta \ln \Phi - \beta \ln \eta. \quad (3.3)$$

It has to be noted that the chosen x -variable defines the unit for η . Equation (3.3) reminds us of the common line equation and β and η parameters of the Weibull function (6) can be extracted by applying (8):

$$kx + c = \beta \ln \Phi - \beta \ln \eta, \quad (3.4)$$

where k is the slope and c is the intercept of the linear fit and y -axis. In order to compare the empirical data with the distribution function, common way to obtain cumulative proportion (y -coordinate) for each failure is to apply Benard approximation Equation (3.5):

$$F = \frac{i - 0.3}{N + 0.4}, \quad (3.5)$$

where i is the running number of failure (first, second etc.) and N is the sample size. For each device failure, F is then plotted as a function of reached fluence until corresponding failure (Figure 3.1). The data is from our experimental study and the experimental details and further analysis are presented in Section 3.3. Once the data are plotted, a linear fit allows to extract the two parameters of the Weibull model which can be derived from Equation (3.4). The shape parameter, β , then defined in Equation (3.6) and the scale parameter, η in Equation (3.7):

$$\beta = \frac{k}{\ln 10} \quad (3.6)$$

$$\eta = e^{-\frac{c}{\beta}} \quad (3.7)$$

The shape parameter β of a Weibull distribution is taken as an indicator of the failure mode. In particular, if $\beta < 1$, the distribution will show a decreasing failure rate with time, which is representative of early life failures. A $\beta > 1$ value is representative of an increasing failure rate with time indicating wear-out failures. Finally, a $\beta = 1$ value is related to a constant failure rate, which is expected in the so-called useful life of the device or system. On top of that, a $\beta = 1$ value is typical of random failures, which is supposed to be the expected failure mode during stochastic neutron interaction.

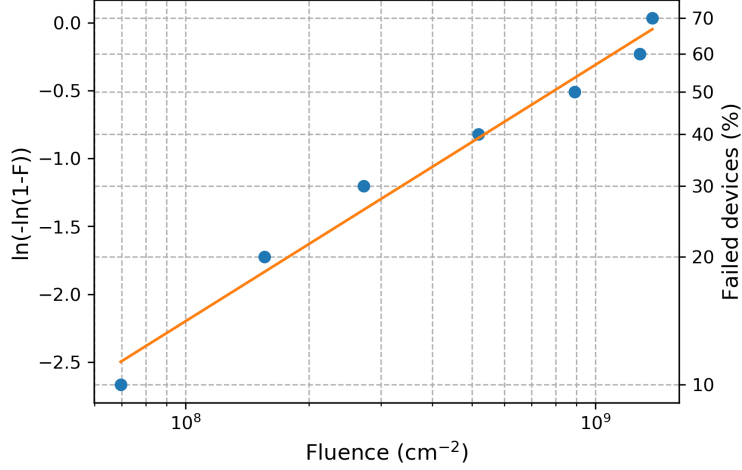


Figure 3.1: Weibull presentation of destructive failure data of SiC MOSFETs under atmospheric-like neutron spectrum. A line has been fitted to the dataset by using a least squares method. Devices were biased at $V_{DS} = 900\text{ V}$ and $V_{GS} = 0\text{ V}$. The experimental procedure of the test is described in detail in Section 3.3.

Maximum likelihood estimation (MLE)

In maximum likelihood estimation (MLE) method, the Weibull parameters are extracted by finding a maximum of the log-likelihood function Equation (3.8).

$$l = N \ln \beta - N \beta \ln \eta - \sum_{i=1}^N \left(\frac{x_i}{\eta} \right)^\beta + (\beta - 1) \sum_{i=1}^r \ln x_i, \quad (3.8)$$

where x_i is the time or fluence of given failure, N is the sample size and r is the number of failures. By taking partial derivatives $\frac{\partial l}{\partial \eta}$ and $\frac{\partial l}{\partial \beta}$ and setting both simultaneously to 0, we can extract the Weibull parameters β and η which are given in Equation (3.9) and Equation (3.10) respectively.

$$\beta = \left[\frac{\sum_{i=1}^N x_i^\beta \ln x_i}{\sum_{i=1}^N x_i^\beta} - \frac{1}{r} \sum_{i=1}^r \ln x_i \right]^{-1} \quad (3.9)$$

$$\eta = \left[\frac{\sum_{i=1}^N x_i^\beta}{r} \right]^{\frac{1}{\beta}} \quad (3.10)$$

Equation (3.9) cannot be solved analytically but the solution can be found by iterative method.

3.2.2 Failure rate and Failure in Time (FIT)

The failure rate of a given device can be expressed in Failure in Time (FIT) which is a failure rate unit defining the number of failures over a 10^9 device-hours. FIT is a standard reliability indicator extensively used in the industry and defined by the overall reliability target. The failure rate Equation (3.11) in FITs can be simply derived from the Mean Time To Failure (MTTF).

$$\lambda = \frac{10^9}{MTTF \times AF}, \quad (3.11)$$

where AF represents the accelerating factor for the particle flux and is defined as the ratio of accelerator flux and the atmospheric flux (Equation (3.12)):

$$AF = \frac{\text{Accelerator flux}}{\text{Atmospheric flux}} \quad (3.12)$$

Regardless of the method which is used to extract Weibull parameters, MTTF can be derived from the Weibull analysis by using reliability parameters β and η . In general case, MTTF can be derived after Equation (3.13).

$$MTTF = \eta \times \Gamma\left(1 + \frac{1}{\beta}\right), \quad (3.13)$$

where Γ represents the Gamma function. It should be noted that when $\beta = 1$, which is the case with purely random failures, $MTTF = \eta$. The unit of η is the same than the unit used for plotting the failures in the Weibull plot.

It should be noted that often in radiation testing, instead of time, more interesting parameter is particle fluence. Therefore, rather than using MTTF, mean fluence to failure (MFTF) is usually extracted. However, regardless of the variable, analysis is similar. The link between MFTF and MTTF is given in Equation (3.14).

$$MFTF = MTTF \times flux \quad (3.14)$$

The standard deviation σ_T for MTTF is given by:

$$\sigma_T = \eta \times \sqrt{\Gamma\left(\frac{2}{\beta} + 1\right) - \Gamma\left(\frac{1}{\beta} + 1\right)^2} \quad (3.15)$$

3.3 Experimental study

3.3.1 Devices under test (DUTs)

Studied devices in this work are commercial off the shelf (COTS) power SiC MOSFETs and GaN HEMTs. The studied SiC device is a packaged (4H-SiC die in TO-247 package with 3 pins) commercial power Vertical Double implanted MOSFET (VD-MOSFET). To date, this device is the 3rd and last generation available from the manufacturer Cree-Wolfspeed. The studied GaN HEMT (EPC2012) is a bare die device, which was surface mounted on the specifically designed printed circuit board (PCB) equipped with pins in order to connect it to the test board in similar way than the packaged SiC device. Studied devices and their electrical ratings are listed in Table 3.1.

Table 3.1: Device tested in this study

| Technology | Manufacturer | Part number | V_{DSmax} (V) | I_{DSmax} (A) | R_{DSon} (m Ω) |
|------------|--------------|-------------|-----------------|-----------------|--------------------------|
| SiC MOSFET | Cree | C3M0120090D | 900 | 23 | 120 |
| GaN HEMT | EPC | EPC2012 | 200 | 3 | 100 |

3.3.2 SEB test setup

We have designed and fabricated a dedicated test board to evaluate the irradiation effect. Two identical test boards were fabricated. In that way, it was possible to prepare a board for the next beam run while the other board was under the beam. During irradiation test, test board containing DUTs is placed under beam while drain and gate voltages are controlled. Total gate and drain currents are monitored with computer and source measurement units (SMU) in the control room. The drain voltage was applied and the total drain current was measured with a Heininger EVO HV power supply and the gate voltage was applied and current was measured with a Keysight B2902A precision SMU. The SMUs were controlled and data were collected via Ethernet and USB interfaces and scripts were developed with Python programming language. The schematic diagram of the developed irradiation test setup is presented in Figure 3.2.

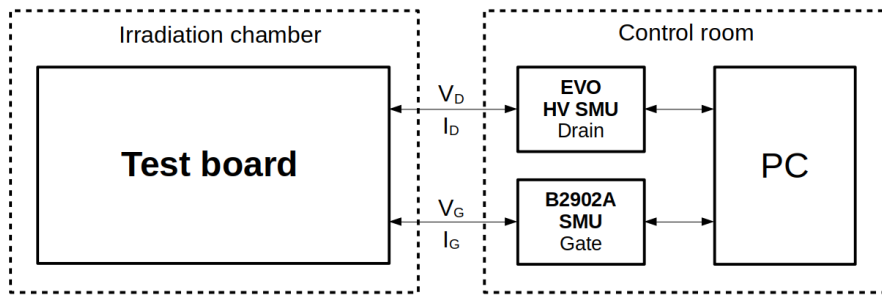


Figure 3.2: SEB test setup schematics.

The test board schematics follow the MIL-STD SEE test standard [140] and the schematics is presented in Figure 3.3 and photo of the test board with DUTs is presented in Figure 3.4. During irradiation, the destructive failures of the DUTs are identified by step increase of the total current caused by the low resistance path inside the device structure. Therefore, each DUT failure is linked to a defined time along the test. The resistor between the drain SMU and DUT limits the current drawn from the SMU to predefined value, which is typically some milliamperes preventing the SMU to reach its compliance limit in the event of DUT burnout. Capacitor placed on the drain contact of the DUT provides enough energy in order to trigger possible burnout.

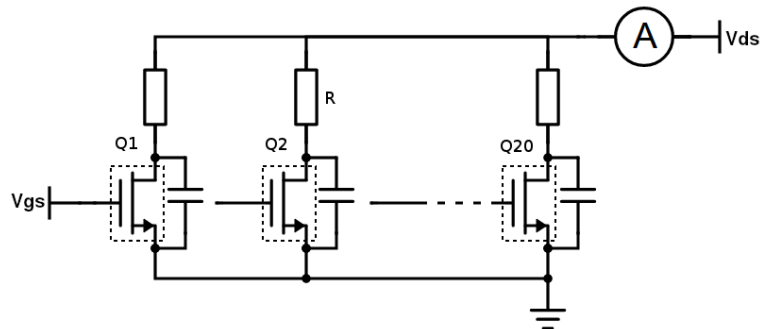


Figure 3.3: SEB test board schematics.



Figure 3.4: Photo of the test board with SiC MOSFETs placed in neutron irradiation test position.

3.3.3 Neutron radiation environment

Neutron irradiations were performed at ChipIr facility [149]. The comparison between the ChipIr and atmospheric neutron spectrum is given in Figure 3.5 and more information about the facility is also provided in Section 2.4.2.

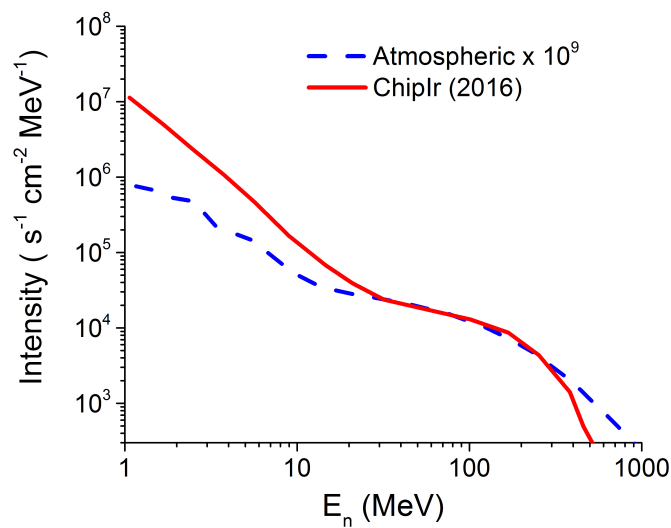


Figure 3.5: The ChipIr neutron spectrum compared to the atmospheric spectrum at ground level [149].

the semiconductor material, generated electrons and holes drift under applied electric field towards drain and source contacts respectively. The electric field across the drift layer of the MOSFET is proportional to the applied drain voltage. The electric field increases with increasing drain-to-source voltage which results higher carrier velocities in the semiconductor. Higher electric field increases impact ionization, which is one proposed contributor for SEB in SiC MOSFETs. With our method, extracted Weibull shape and scale parameters of different drain voltage configurations are presented in Table 3.2.

Table 3.2: Weibull parameters for different irradiation configurations

| V_{DS} (V) | β_{LR} | β_{MLE} | η_{LR} (cm ⁻²) | η_{MLE} (cm ⁻²) |
|--------------|--------------|---------------|---------------------------------|----------------------------------|
| 675 | 1.52 | 2.07 | 2.73×10^{10} | 2.47×10^{10} |
| 800 | 0.72 | 0.91 | 1.17×10^{10} | 7.83×10^9 |
| 900 | 0.84 | 1.04 | 1.43×10^9 | 1.24×10^9 |

Since the failures are neutron induced and therefore random in nature, the β value should be equal to 1 in each configuration. However, due to relatively low statistics, we see some differences in the β value. Since the devices were not stressed during the irradiation experiment nor their maximum electrical ratings were exceeded, we should expect $\beta = 1$ if higher number of devices were used.

After extracting the reliability parameters, failure rate in units of FIT was calculated based on the method described in Section 3.2.2. On this basis, failure rates have been calculated using Equation (3.11) and Equation (3.13). Failure rates are reported in Table 3.3 for both avionic and ground level applications.

Table 3.3: Failure rates for avionic and ground level applications in units of FIT

| V_{DS} (V) | MFTF _{LR} (cm ⁻²) | MFTF _{MLE} (cm ⁻²) | LR | | MLE | |
|--------------|--|---|-----------------------|-------------------------|-----------------------|-------------------------|
| | | | FIT _{ground} | FIT _{avionics} | FIT _{ground} | FIT _{avionics} |
| 675 | 2.46×10^{10} | 2.19×10^{10} | 0.5 | 146 | 0.6 | 165 |
| 800 | 1.44×10^{10} | 8.19×10^9 | 0.9 | 250 | 1.6 | 440 |
| 900 | 1.59×10^9 | 1.22×10^9 | 8.2 | 2260 | 10.7 | 2949 |

3.3.5 Gate bias voltage dependence on SEB sensitivity under atmospheric neutron environment

The most common method for assessing the radiation sensitivity of power MOSFET is to test with different drain bias voltage values while $V_{GS} = 0$. This is to ensure that the transistor is in off-state i.e. there is no current flowing through the channel of the transistor. However, when such devices are operating in application, such as in switching power converter, the V_{GS} is likely to vary between negative and positive values. For example, V_{GS} in switching power converter utilising SiC power MOSFET can vary from -4 V to 10 V during the switching operation [172]. Therefore, it is important to assess,

if the off-state gate voltage plays a role in the sensitivity for destructive failure while operating in radiation environment.

In this section, the effect of applied V_{GS} during irradiation on the SEB failure behaviour is studied.

Experimental details

Two different gate voltage values ($V_{GS} = 0\text{ V}$ and -4 V) for each drain voltage configuration ($V_{DS} = 675\text{ V}$, 765 V and 900 V) during irradiation were tested. It should be noted that the maximum negative static gate voltage given by the manufacturer and indicated in the datasheet is -4 V for the tested reference. 20 devices for each bias voltage configuration were used resulting in 120 devices tested in total. Test setup is described in Section 3.3.2. Devices were irradiated under atmospheric-like neutron environment at ChipIr. Details of the facility are described in Section 2.4.2.

Results

We have plotted SEB failures in a Weibull scale for all the experimental data (Figure 3.7) as described in Section 3.2.1. From the extracted Weibull parameters, the MFTF are calculated with Equation (3.13) and are presented in Figure 3.7 for different bias voltage configurations. Extracted reliability parameters are summarized in Table 3.4.

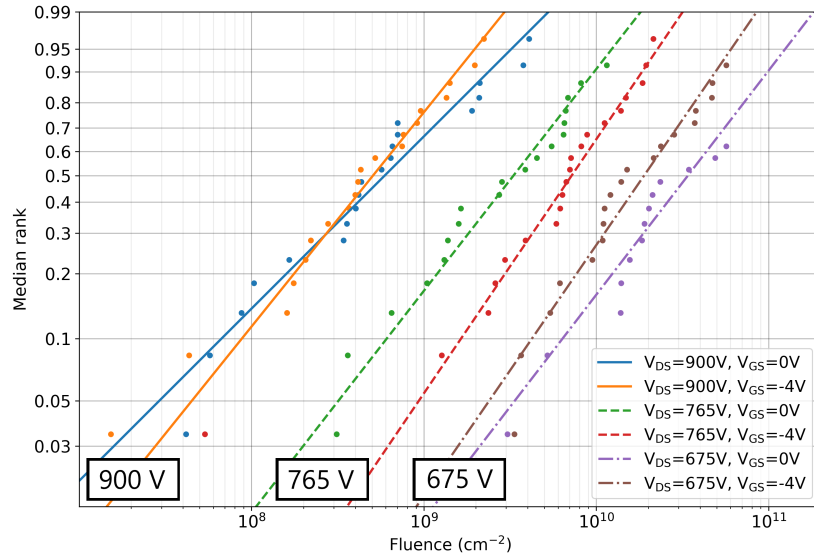


Figure 3.7: Failure data for SiC MOSFET under atmospheric neutron spectrum for different drain and gate bias configurations [173].

We can see in Table 3.4 that β values are close to 1 for each configuration. It indicates constant failure rate over time which implies random failures with time which are typical for neutron induced failures since the interaction is considered stochastic. However, for each V_{GS} value during irradiations, β values for configurations with negative gate voltages are greater compared to irradiations with $V_{GS} = 0\text{ V}$. It gives an indication of increasing failure rate over time for devices which gate was negatively biased during irradiation.

We can see in Figure 3.8 that, the MFTF decreases with increasing V_{DS} , as expected.

Table 3.4: The extracted reliability parameters for each irradiation configuration by MLE and LR methods

| V_{DS} (V) | V_{GS} (V) | β_{MLE} | β_{LR} | η_{MLE} (cm^{-2}) | η_{LR} (cm^{-2}) | $MFTF_{MLE}$ (cm^{-2}) | $MFTF_{LR}$ (cm^{-2}) |
|--------------|--------------|---------------|--------------|--------------------------------------|-------------------------------------|--------------------------------------|-------------------------------------|
| 675 | 0 | 1.12 | 1.26 | 5.19×10^{10} | 4.39×10^{10} | 4.99×10^{10} | 4.08×10^{10} |
| | -4 | 1.33 | 1.34 | 2.49×10^{10} | 2.46×10^{10} | 2.30×10^{10} | 2.26×10^{10} |
| 765 | 0 | 1.12 | 1.07 | 4.63×10^9 | 4.59×10^9 | 4.44×10^9 | 4.47×10^9 |
| | -4 | 1.27 | 0.98 | 9.58×10^9 | 9.59×10^9 | 8.88×10^9 | 9.79×10^9 |
| 900 | 0 | 0.87 | 0.92 | 9.06×10^8 | 8.75×10^8 | 9.75×10^8 | 9.11×10^8 |
| | -4 | 1.07 | 0.96 | 6.96×10^8 | 7.11×10^8 | 6.78×10^8 | 7.23×10^8 |

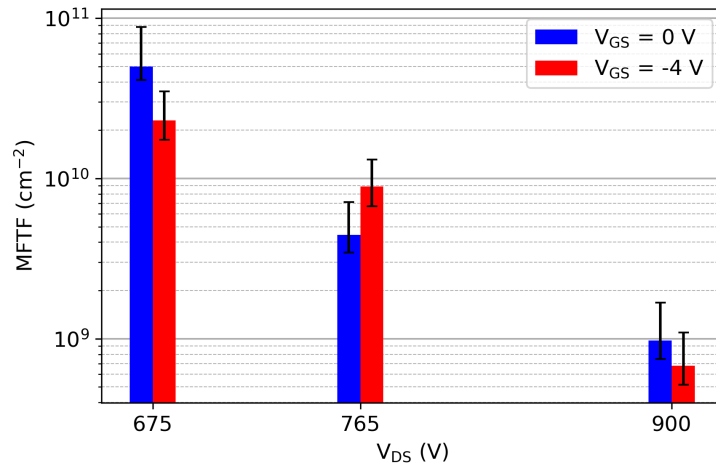


Figure 3.8: The extracted MFTF values for different irradiation bias configurations.

However, looking more closely on the MFTF for the lowest applied V_{DS} value (675 V) in Figure 3.8, it seems that MFTF is affected by the applied gate voltage. This might indicate an enhanced sensitivity to SEB when $V_{GS} = -4$ V. Since such behaviour is not observed at higher drain voltages, it is assumed that the contribution of the reverse gate bias on the risk of failure increases as the drain voltage is close to the safe operating area (SOA) limit, which for this reference has been found to be between 50 % and 75 % of the applied drain voltage [76]. Indeed, applied drain voltage results in electric field across the drift layer which is an important contributor to the SEB triggering for such devices [94], especially at maximum electrical rating.

When applying voltage on the drain of the power MOSFET with vertical structure, it will also contribute to the electric field across the gate dielectric. When applying additional negative gate bias voltage, this electric field is therefore increased and might increase the probability for a destructive failure.

3.3.6 Failure analysis of the SiC MOSFET after SEB

Furthermore, in order to increase the understanding of the radiation-induced destructive event mechanism of SiC MOSFET, a failure analysis has been performed for a (unstressed) device which exhibited SEB during neutron irradiation. The analysed device was irradi-

ated under atmospheric neutron beam up to $2 \times 10^{10}/\text{cm}^2$ neutron fluence (considering neutron energies above 10 MeV) while biased at $V_{DS} = 675 \text{ V}$ and $V_{GS} = 0 \text{ V}$.

In order to analyse the local degradation of the device several steps are required: packaging opening, localization of the defect, component cutting, polishing and observation. All steps must maintain the integrity of the device, that means that the device preparation must not induce additional defects. For that, after the opening of the resin package on the back side, the SiC die was thinned from the drain side in order to achieve a thin SiC layer which becomes optically transparent. After the failure point was located through the thin SiC material, the sample cutting line was located at the center of the observed failure location and to finish the sample preparation, the cross section of the SiC device is polished. The sample preparation and analysis took place at the Crismat Laboratory in Caen, France. The device was then analysed using a scanning electron microscopy (SEM).

Figure 3.9 represents an high-resolution image obtained during SEM analysis. The SEM image shows the SiC cross-sectioned sample after the neutron SEB event. As we can see, SEM analysis indicates the failure location inside the SiC MOSFET structure. The crack induced by the neutron irradiation is exactly located on and under the gate region. In addition, electrical characterizations in Figure 3.10 show a short circuit between the drain and the source after a SEB. During characterization, I_{DS} reaches the compliance limit of the measurement equipment already at $V_{GS} = 0 \text{ V}$, implying the loss of voltage blocking capability of the MOSFET. On top of that, low resistance current path from gate to source is observed.

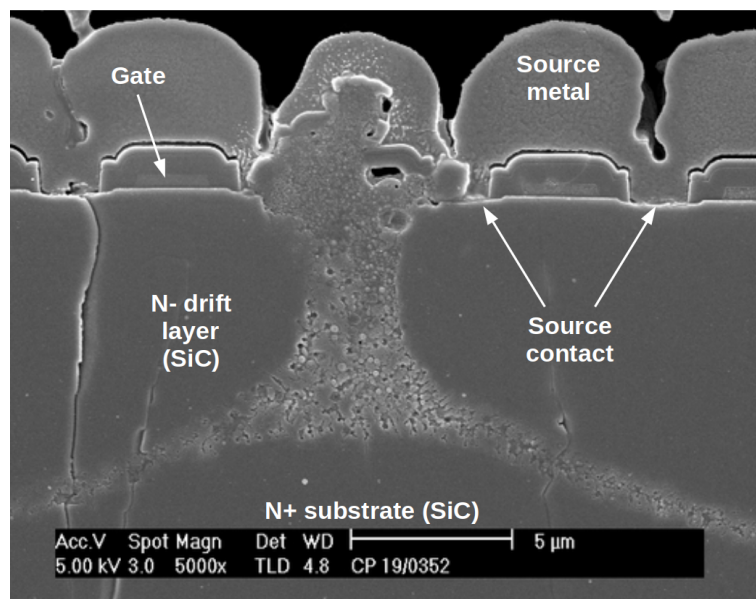


Figure 3.9: SEM image of the neutron-induced SEB in SiC MOSFET ($\times 5000$). Image of the melted area induced by the neutron irradiation located on and under the gate region.

As one can see in Figure 3.9, the cross-sectional SEM view indicates the failure location inside the SiC MOSFET structure. A melted area, located on one gate structure and inside the semiconductor lattice, is due to the high localized current caused by neutron-induced SEB and subsequent thermal expansion of the SiC material. Moreover, visually observed damage of the SEB is located close to the drift region interface with the N+ Drain doping

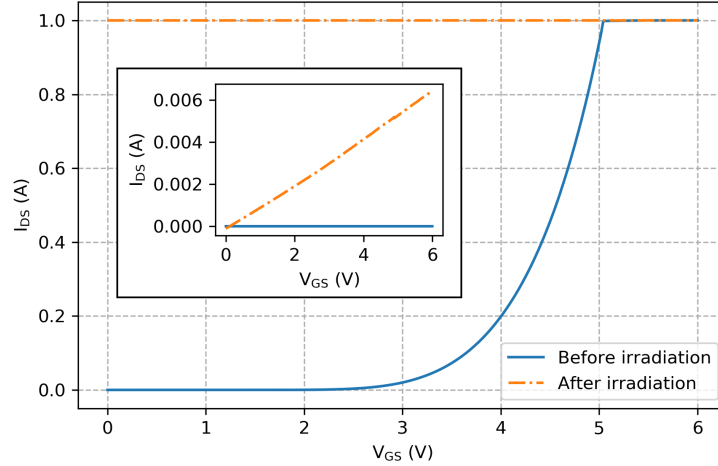


Figure 3.10: $I_{DS}V_{GS}$ -characteristics of the failed device before and after failure. $V_{DS} = 10$ V during characterization.

layer reaching to the surface of the active volume, which is supported by other studies [98]. Generated electrons and holes respectively drift towards the drain and the source contacts. If these drifting carriers gain enough energy under the influence of the electric field, impact ionization can occur and the current sustains until localized overheating of the SiC material and device breakdown.

IV-characteristics in Figure 3.10 shows SEB signature for the analysed failed device. After irradiation, high value for I_{DS} reveals a short circuit between the drain and the source. On top of that, a low resistance current path on the gate can be seen indicating also a gate failure. Though this signature alone might be linked to a SEGR, in this case and for all the observed failures, the gate failure is following the drain to source short-circuit and is clearly a side effect of the SEB.

3.3.7 Comparison of LR and MLE methods by example cases

In this section, different irradiation induced failure datasets are analysed with LR and MLE methods and Weibull parameters are compared. In all following cases, device under test (DUT) is Cree SiC MOSFET, part number C3M1020090D. Devices were irradiated with atmospheric-like neutron spectrum at ChipIr.

Effect of linearity on Weibull parameters

While the gate was grounded, the devices were biased at their maximum drain voltage. During the irradiation, 7 of 10 devices failed. In Figure 3.11, MLE and LR methods for fitting the Weibull distribution to the failure data are compared. From this analysis, Weibull parameters for LR and MLE methods are calculated and given in Table 3.5.

We can see in Figure 3.11 that the data is reasonably linear. β is higher for MLE method while η is slightly lower compared to LR method. In the case where the data is less linear (Figure 3.12, Table 3.6), we can see that the difference in β values is larger compared to linear case.

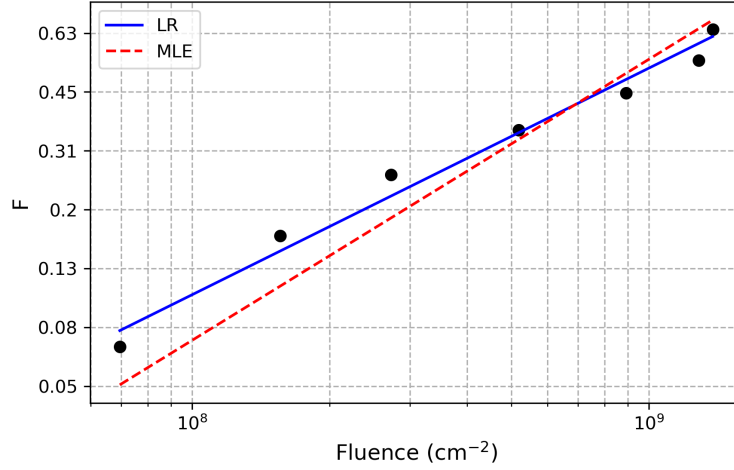


Figure 3.11: A comparison of MLE and LR fits to the failure data of destructive failures under neutron irradiation. Devices were biased at $V_{DS} = 900\text{ V}$ and $V_{GS} = 0\text{ V}$, $N = 10$.

Table 3.5: Weibull parameters for data in Figure 3.11

| Fitting method | β | η (cm^{-2}) |
|----------------|---------|-----------------------------|
| LR | 0.84 | 1.43×10^9 |
| MLE | 1.04 | 1.24×10^9 |

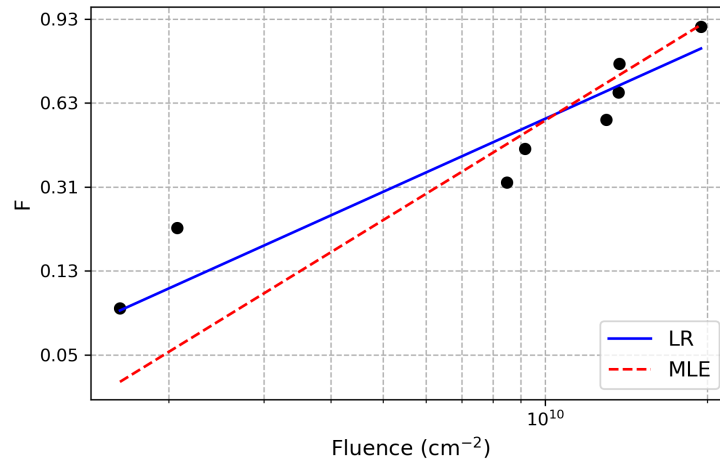


Figure 3.12: A comparison of MLE and LR fits to the failure data of destructive failures under neutron irradiation. Devices were biased at $V_{DS} = 675\text{ V}$ and $V_{GS} = 0\text{ V}$, $N = 15$.

Table 3.6: Weibull parameters for data in Figure 3.12

| Fitting method | β | η (cm^{-2}) |
|----------------|---------|-----------------------------|
| LR | 1.26 | 1.16×10^{10} |
| MLE | 1.71 | 1.13×10^{10} |

Effect of suspensions on Weibull parameters

In previous results, data is almost complete failure data meaning that the number of failures is close to the sample size. However, due to variety of reasons, usually during failure testing not all the devices fail before test is stopped. This is called censoring and sometimes more than 50% of the devices are not failed after test. In the following example, heavily censored data with 7 failures of 24 total devices is analysed. Therefore, less than 1/3 of the devices failed during the test. Such censoring is referred here as heavy censoring whereas light censoring refers to the case where more than 63% of the tested devices were failed during the test. Failure data and fits are presented in Figure 3.13 and extracted Weibull parameters in Table 3.7.

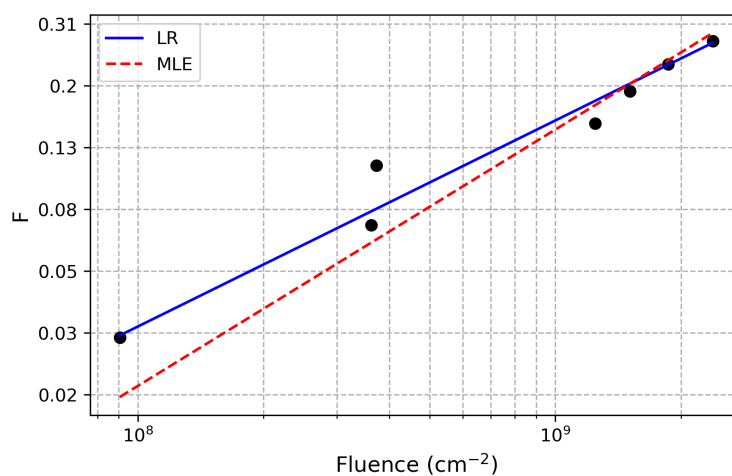


Figure 3.13: A comparison of MLE and LR fits to the failure data of destructive failures under neutron irradiation. Devices were biased at $V_{DS} = 800$ V and $V_{GS} = 0$ V, $N = 24$.

Table 3.7: Weibull parameters for data shown in Figure 3.13

| Fitting method | β | η (cm^{-2}) |
|----------------|---------|-----------------------------|
| LR | 0.72 | 1.17×10^{10} |
| MLE | 0.90 | 7.83×10^9 |

In all the previous results, MLE method gives higher value for β than LR method. Same trend has been reported previously [146]. MLE method tends to overestimate the value of β , especially when the sample size is relatively small. The effect of censoring on difference in parameters between methods are compared in Table 3.8.

Even with heavy censoring, β is not strongly affected by censoring but when the number of survived devices is high compared to number of failed devices (heavy censoring), η is strongly affected. Even if the linear regression method takes into account the sample size, it still ignores the information about the position of the censored data points after the last failure [174]. Therefore, especially when heavy censoring is involved, MLE method should give more accurate results.

Table 3.8: Comparison of MLE and LR methods in different cases

| Fitting method | $\beta_{\text{MLE}}/\beta_{\text{LR}}$ | $\eta_{\text{MLE}}/\eta_{\text{LR}}$ |
|-----------------------------|--|--------------------------------------|
| Linear, light censoring | 1.24 | 0.87 |
| Non-linear, light censoring | 1.36 | 0.97 |
| Linear, heavy censoring | 1.25 | 0.66 |

3.3.8 Coupled radiation and aging effects of SiC MOSFET

As mentioned, during its operation, device aging results in changes in device characteristics, which can originate from structural changes in the device materials. It is important to assess, if such aging affects radiation sensitivity of the device. On the other hand, in addition to catastrophic, irradiation-induced failures, it is important to study if non-destructive irradiation has an impact on long-term reliability of the device.

In this section, aging of the devices is performed in accelerated manner and the radiation sensitivity between aged and fresh devices are compared. Long-term reliability between non-irradiated and irradiated devices is studied by stressing the devices electrically until their breakdown and the magnitudes of the stress for two device categories are compared.

Accelerated aging method

Accelerated aging method in this study is constant current stress (CCS) which is applied on the gate terminal while drain and source are grounded. In CCS, a constant current of $100\ \mu\text{A}$ is applied for 100s resulting in 10 mC injected charge for all stressed devices. Schematics of the CCS circuit is presented in Figure 3.14.

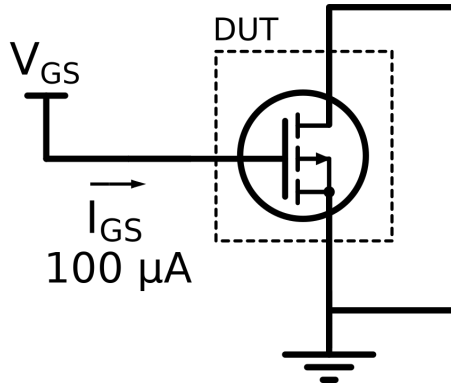


Figure 3.14: Schematics of the gate stress circuit used in CCS.

The purpose of the current stress is to create defects in the oxide layer in an accelerated manner. Chosen magnitude and duration are defined based on our empirical data from breakdown voltage (gate) and charge to breakdown measurements so that the stress level (voltage and total charge) is safely below the instantaneous breakdown point. It is important to note that this injected charge is ten times lower than the average oxide charge to breakdown, found to be at 100 mC. As a consequence, electrically stressed devices are still far from their mean charge to breakdown value. During the stress, the

gate voltage is between 37 V and 38 V, which is above the maximum rated V_{GS} but well below the instantaneous breakdown voltage which is found to be between 45 V and 50 V (part-to-part variation). Figure 3.15 represents the evolution of the V_{GS} as a function of stress time during the destructive charge-to-breakdown test.

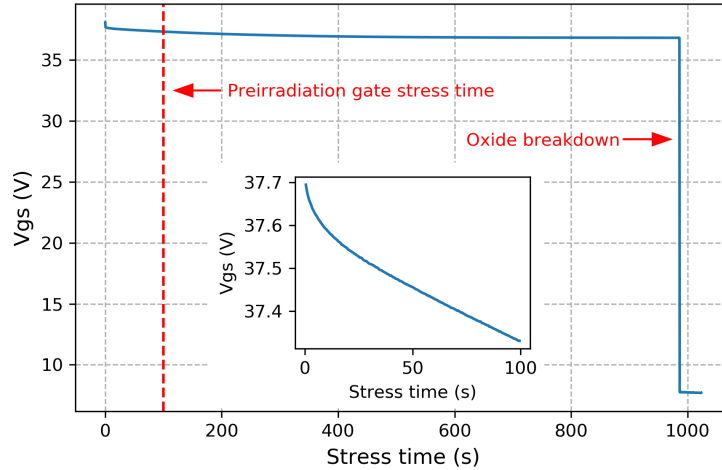


Figure 3.15: V_{GS} evolution curves during the CCS (inset graph) and charge-to-breakdown measurement for the SiC device [76]. $V_{DS} = 0$ V during stress.

The 100 s stress time is indicated in the Figure 3.15 in order to compare the magnitude of the CCS to the final breakdown of the oxide. In CCS, the current was applied on the gate for 100 s and then removed in order to avoid the oxide breakdown. In order to find the safe stressing time, some devices were exposed to 100 μ A constant current until breakdown was observed. Eventual breakdown is indicated by sharp decrease of the gate voltage indicating a low resistance path between the gate and the source. The effect of CCS on device characteristics are presented in Figure 3.16.

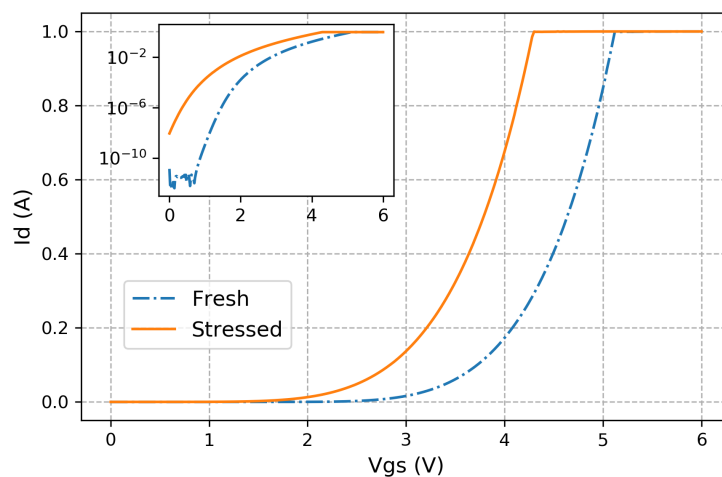


Figure 3.16: The effect of electrical gate stress on $I_{DS}V_{GS}$ characteristics in linear scale and in logarithmic scale (inset graph) for fresh and stressed. “Fresh” means before any stressing. Negative shift in V_T can be seen after electrical stress. $V_{DS} = 10$ V during characterization.

I_V -characteristics in Figure 3.16 show negative shift in threshold voltage (V_T) due to electrical stress. Similar trend has been observed in [166]. Negative shift in V_T implies positive trapped charge inside the gate oxide layer of the MOSFET. We also observe a stretchout in subthreshold region which together with negative ΔV_T increases the leakage current in off-state.

Effect of aging on SEB sensitivity

Irradiation experiment details Two sets of devices (30 devices in total) were irradiated under atmospheric neutron environment. Irradiation setup is described in Section 3.3.2 and neutron radiation environment in Section 3.3.3. 15 devices without electrical stress and 15 devices with electrical stress before irradiation were tested for SEB and results were compared. In order to avoid reaching too high fluences likely leading to displacement damage, the test was stopped at $2 \times 10^{10}/\text{cm}^2$. At this fluence, about 50 % of the devices remained un-failed whereas all others exhibited SEB.

Results Electrical characterizations for all devices were performed before electrical stressing, after electrical stressing and after neutron irradiation. In Figure 3.17, we report the I_V -characteristics for one device before and after electrically stressed and after irradiation.

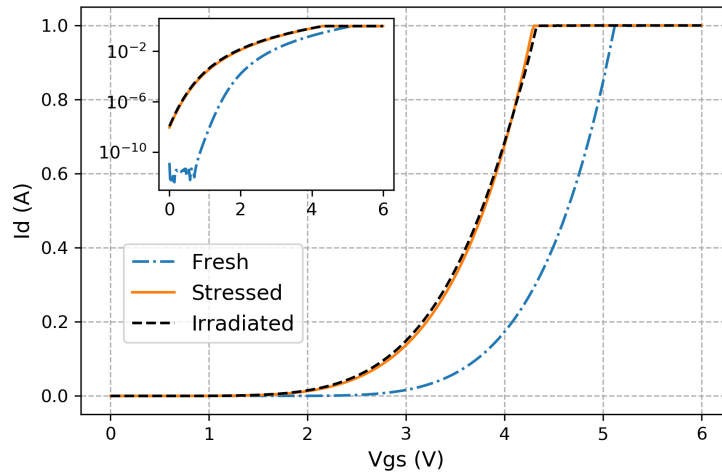


Figure 3.17: $I_{DS}V_{GS}$ -characteristic of the device in linear scale and in logarithmic scale (inset graph) for a fresh, stressed and irradiated at 50 % of V_{DSmax} . “Fresh” means before any stressing or irradiation. Then device was stressed and after that irradiated. Negative shift in V_T can be seen after electrical stress. No significant change in device characteristics after neutron irradiation is observed. $V_{DS} = 10$ V during characterization.

In order to investigate if the electrical stress affects the SEB sensitivity of the device, a Weibull analysis was performed on both stressed and fresh device failure data. Non-failed devices are taken into account as suspended values. Extracted parameters (β , η and η_{WB}) are calculated (for the 15 devices irradiated per configuration) and presented in Table 3.9.

Based on the assumption that failure rate is constant under neutron beam, also a one-parameter Weibull function, also known as Weibayes [146], was fitted to the fresh device data. A one-parameter fit can be more accurate compared to a 2-parameter model when

we have reasonable assumption for β and relatively low sample size. Therefore, β was set to 1 and η_{WB} was extracted by using Equation (3.10). This approach makes sense since we can see in Table 4.10, that the value of shape parameter β for fresh devices is close to 1, proper to random failures over time. This is expected, since neutron interaction is considered as a stochastic process.

The correlation values for linear fit (R2-values) are 0.95 for fresh devices and 0.88 for stressed devices. The result confirms that the linear fit is justified for fresh devices. However, for stressed devices the linear fit does not represent the data with sufficient precision. This low value of R2 can be explained by the concave shape in the data in Figure 3.18.

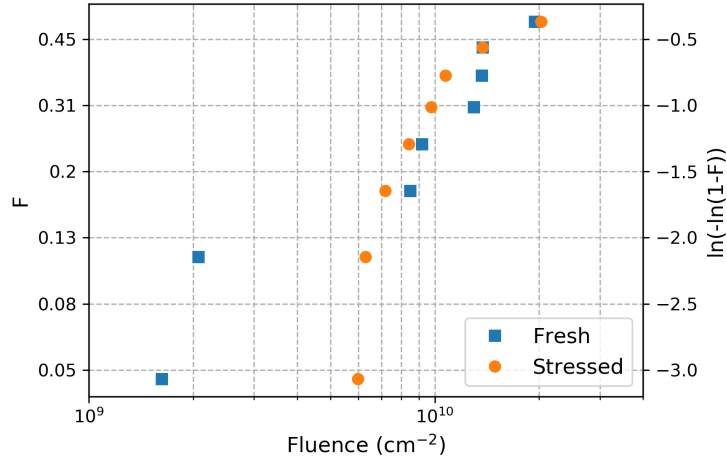


Figure 3.18: Weibull plot of neutron induced SEB. Devices were irradiated at 75% of the V_{DSmax} ($V_{DS} = 675$ V) while $V_{GS} = 0$ V. 15 devices in each configuration were irradiated [76].

Table 3.9: Reliability parameters for stressed and fresh devices

| | β_{LR} | β_{MLE} | η_{LR} (cm^{-2}) | η_{MLE} (cm^{-2}) | η_{WB} (cm^{-2}) | MFTF_{LR} (cm^{-2}) | MFTF_{MLE} (cm^{-2}) |
|----------|--------------|---------------|-------------------------------------|--------------------------------------|-------------------------------------|--|---|
| Fresh | 1.02 | 1.27 | 2.90×10^{10} | 2.45×10^{10} | 2.72×10^{10} | 2.87×10^{10} | 2.27×10^{10} |
| Stressed | 2.48 | 1.70 | 1.64×10^{10} | 2.22×10^{10} | 2.80×10^{10} | 1.46×10^{10} | 1.98×10^{10} |

The interesting point of this analysis is that in both LR and MLE methods, β is greater for stressed devices compared to fresh devices. While β is close to 1 for fresh devices, $\beta > 1$ for stressed devices. This indicates an increasing failure rate over time and therefore can, in a first approach, be related to the preliminary aging process due to the electrical stress. Note that such phenomenon has already been observed for Single Event Gate Rupture (SEGR) occurring in silicon power devices [143]. Even with such relatively low statistics, this result is an indicator of different failure mechanisms between fresh and stressed devices. In addition to difference in β , MFTF appears to be lower for electrically stressed devices.

The effect of non-destructive neutron radiation on gate reliability of SiC MOSFETs

As mentioned earlier, in order to trigger destructive event, sufficient amount of charge needs to be generated in the sensitive volume of the device. However, non-destructive events can generate charge and current transients in the device structure and might lead to device weakening and possibly a lifetime reduction during its operation.

Degradation of the gate oxide in SiC power devices due to heavy ion impact has been reported in several studies [86, 114–116, 175]. Also, it has been reported that drain-to-source breakdown voltage for SiC MOSFET can be reduced due to neutron-induced non-destructive single event effect (SEE) [76]. On top of that, it is known that gate reliability of SiC MOSFET is degraded when device is operated in short circuit conditions [176]. Therefore, it is reasonable to assume that the current transients due to non-destructive neutron interaction has an impact on the gate oxide integrity during device operation.

The goal of this section is to determine whether the irradiation weakened the devices and therefore reduced their long term reliability. Though bias configuration during irradiation was especially dedicated to assess device sensitivity to SEB and thus to favor a drain-to-source failure, post-irradiation tests have been conducted through gate oxide electrical stress.

Experimental details The irradiation test setup is described in Section 3.3.2. DUT was SiC MOSFET whose electrical ratings are presented in Table 3.1. The devices were irradiated at $V_{DS} = 800\text{ V}$, $V_{GS} = 0\text{ V}$. Devices which did not exhibit SEB during irradiations, were exposed to post irradiation electrical stress. Also, a set of fresh devices were exposed to same stress in order to compare and to reveal possible neutron-induced weakening of the devices. 17 devices in both categories were tested. Post irradiation electrical stress was applied in order to assess if the non-destructive events during irradiation impact have weakened the gate dielectric layer and therefore reduced the long-term reliability of unfailed devices. In order to compare, both non-irradiated (fresh) and unfailed irradiated devices were subjected to a Constant Voltage Stress (CVS) by using similar setup as used in accelerated aging process presented in Figure 3.14. $V_{GS} = 37.5\text{ V}$ was applied until sharp increase of the gate-to-source current, I_{GS} , was observed indicating a hard failure. This setup allowed to extract the charge to breakdown (Q_{BD}) of the oxide by integrating the current over time until the breakdown point.

Results When applying the CVS on the gate after irradiation, the defects created in the gate oxide during irradiation act as a precursor for current path and eventually a breakdown of the oxide. Figure 3.19 represents the gate current behaviour during the post-irradiation CVS for one non-irradiated and one irradiated device. We can see sharp increase in current and this point was defined as the breakdown point. All the devices show similar behaviour and the breakdown distribution will be discussed later in the section.

Current shape during the CVS in Figure 3.19 shows the increase in gate current at the beginning of the stress and before the oxide breakdown, we observe decrease in the gate current indicating electron trapping overtaking hole trapping, also observed in [177]. The higher value of overall leakage current for irradiated device in Figure 3.19 could be explained by part-to-part variability. However, on average, higher leakage currents during the CVS were observed for irradiated devices. Although, no differences in I_{GS} were found

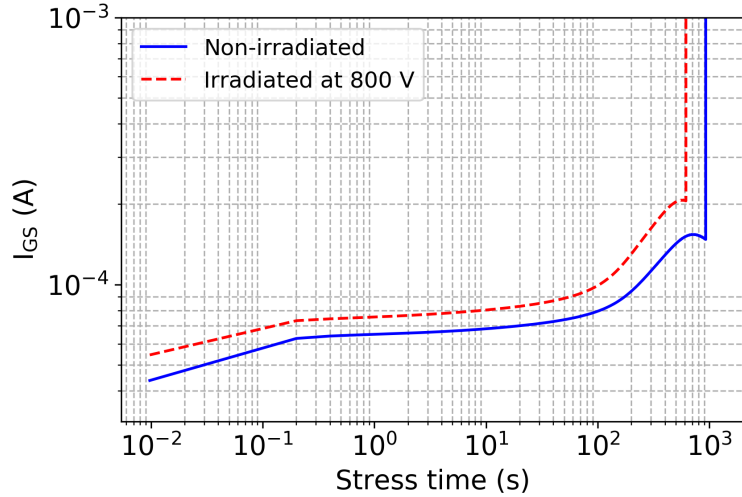


Figure 3.19: Gate current waveforms during the gate breakdown study for one non-irradiated and one irradiated device. Devices were irradiated at $V_{GS} = 0$ V and $V_{DS} = 800$ V. Devices were stressed with constant voltage stress with $V_{GS} = 37.5$ V and $V_{DS} = 0$ V.

when comparing pre- and post-irradiation characteristics at rated voltage of the survived devices. Therefore, it seems that the higher leakage current is triggered only at the higher electric field value. By integrating the gate current over time until the breakdown point, we get the amount of charge injected through the gate oxide during the CVS. These mean Q_{BD} values for fresh and irradiated devices are plotted in Figure 3.20.

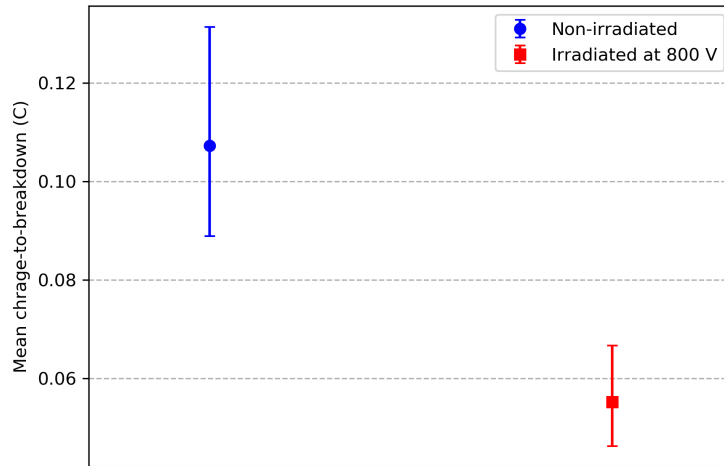


Figure 3.20: Mean charge to breakdown of gate oxide after CVS for fresh and neutron irradiated SiC MOSFETs. 17 devices were studied for both fresh and irradiated devices.

An important result is that the lower amount of injected charge needed for oxide breakdown for irradiated devices (Figure 3.20) clearly points out that neutron irradiation weakened the gate oxide.

None of the devices, which did not exhibit failure during irradiation, show single event gate rupture (SEGR) during the post-irradiation gate voltage sweep, which is a method specified in [140] for verifying oxide integrity. However, as we have seen here, if no failure is observed during the sweep, it does not imply that the gate oxide is not weakened.

Even if the gate failure was not observed during the irradiation neither during post-irradiation gate voltage sweep in the rated safe voltage region, stronger stressing through CVS reveals lower charge-to-breakdown value of gate oxide for irradiated devices. It indicates a degradation of gate integrity due to non-destructive radiation impact and therefore reduction in the reliability of the device.

It is known that the long term reliability of MOS devices is affected due to the oxide degradation [178, 179]. Current through the dielectric during irradiation generates defects which act as precursors for local current paths which can decrease the device lifetime [177]. High electric field increases the Fowler-Nordheim (F-N) tunneling through the oxide. In fact, compared to Si-based devices at same electric field E and temperature, F-N tunneling current is higher in SiC-based devices due to smaller energy barrier of the dielectric. This is due to the wider bandgap of SiC compared to Si [180].

We assume that the weakening of the oxide originates from the defect generation due to charge injection into the oxide [181] due to transient currents caused by neutron impact. Therefore, neutron irradiation contributes to the accumulation of defects in the oxide volume which further reduces the stress time needed for oxide breakdown.

TCAD simulations In order to well understand the effect of non-destructive neutron irradiation, TCAD 2D numerical simulation was performed. The software ECORCE [182] is a TCAD tool which can be used to simulate radiation effects as well as electrical aging effects on electronic components. ECORCE uses a drift-diffusion model coupled with the heat equation (i.e., thermodynamic simulation with lattice temperature) and provides a dynamic mesh generator that optimizes the mesh distribution for all modeling steps for either DC or transient analysis, and for 1D, 2D and axisymmetric geometries. For SiC material, the impact ionization model by Hatakeyama [183], mobility models as a function of parallel E-field and as a function of carrier density by Mnatsakanov et al. [184] and heat equations are used. The geometry of the TCAD device model is presented in Figure 3.21 and the parameters which were used in the simulations are listed in Table 3.10.

Table 3.10: TCAD parameters used in simulation studies

| Parameter | Value |
|--------------------------|---------------------------|
| Secondary ion type | Si |
| Ion energy | 30 MeV |
| Range in SiC | 7.14 μm |
| Angle of incidence | 0° |
| Ion track radius | 100 nm |
| Drain doping density | 10^{19} cm^{-3} |
| Epitaxial doping density | 10^{16} cm^{-3} |
| Source P-doping density | 10^{18} cm^{-3} |
| Source N-doping density | 10^{18} cm^{-3} |

In particular, the tool has been used in order to investigate both electric field distribution and current transients due to irradiation impact and eventual consequences on the long-term reliability of the device.

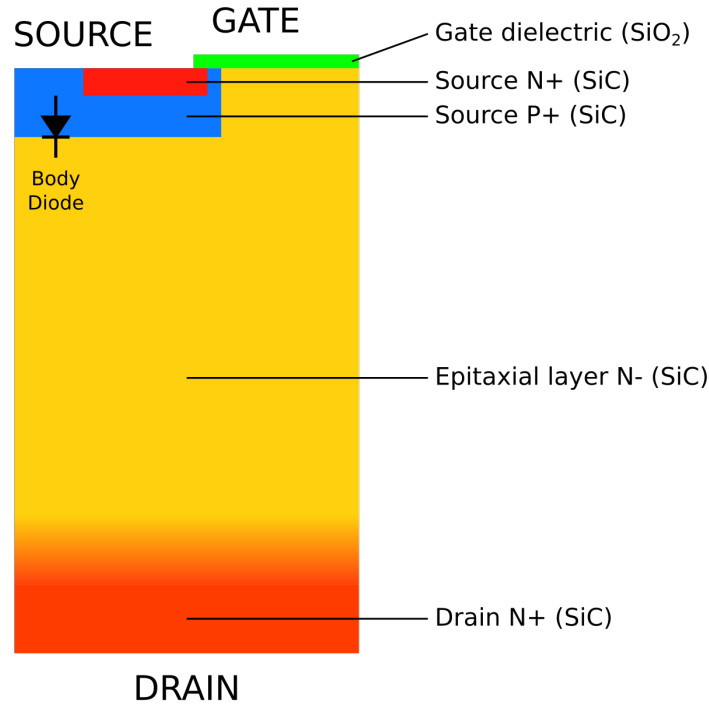


Figure 3.21: 2D-model geometry of the SiC MOSFET implemented in ECORCE.

TCAD simulation here is dedicated to rather model neutron interaction inside the semiconductor material and therefore the ionization track occurring in SiC material instead of both in oxide and in SiC. We simulate the possible weakening of the gate oxide due to the current transients induced by ionization and charge transport in the semiconductor material. Ion impact is simulated with strike point being inside the device structure instead of being at the surface of the device Figure 3.22.

In order to focus on the effect of non-destructive events, simulations of electric field in the gate oxide layer (E_{ox}) were performed in conditions in which no SEB were observed. The E_{ox} in the device structure 3 ps after the ion impact is illustrated in Figure 3.22. It can be seen that the electric field maximum in gate oxide layer is located above the ion impact point. In Figure 3.23, the simulated E_{ox} at the maximum value point indicated in Figure 3.22 and I_{DS} are plotted as a function of time while $V_{DS} = 800$ V. We can see that I_{DS} returns back to its initial value indicating that no SEB occurred.

We can see in Figure 3.23, that the E_{ox} increases almost simultaneously with I_{DS} . A high localized carrier density in SiC epitaxial layer generated by the ion strike causes reduction in electric field in the epitaxial layer along the ion track. Since electric potentials at gate and drain contacts of the device are maintained constant throughout the event, reduction in electric field in the epitaxial layer is compensated by the elevated electric field across the oxide. During the ion impact, E_{ox} in Figure 3.23 exceeds 6 MV/cm and for such devices, it has been observed that the leakage current through the oxide starts to increase when electric field in the oxide exceeds 6 MV/cm [114, 116]. It should be noted that authors in [116] found that such value applies to non-irradiated devices. In case when ion track crosses the oxide layer, the leakage current starts to increase already at lower electric field values. Therefore, generated electric field transient during ion impact induces charge injection into the oxide layer. However, the value of E_{ox} during charge collection is still well below the instantaneous breakdown field (10 MV/cm), which is in

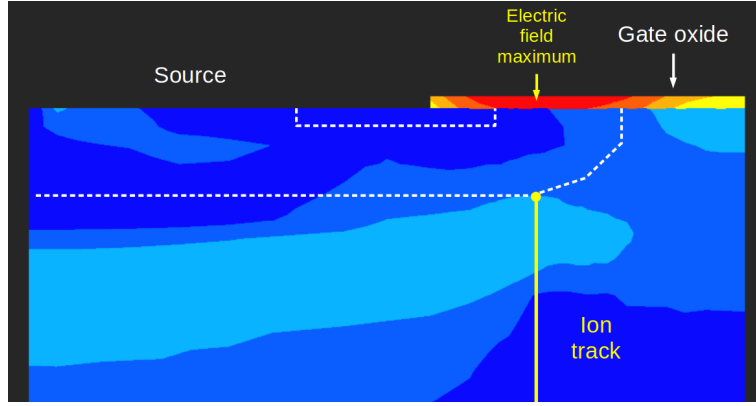


Figure 3.22: Electric field 3 ps after the ion impact simulated with ECORCE. $V_{DS} = 800$ V and $V_{GS} = 0$ V. The electric field maximum in gate oxide layer indicated by yellow arrow is located above the ion impact point.

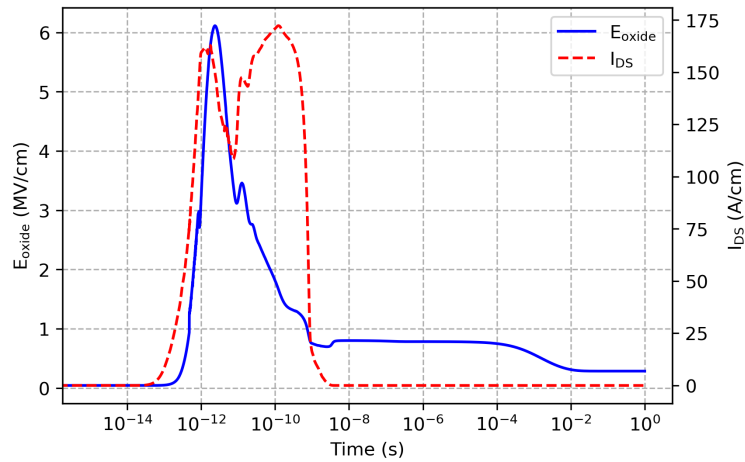


Figure 3.23: Electric field (blue solid line) and drain current (red dashed line) during the ion impact simulated with ECORCE. $V_{DS} = 800$ V and $V_{GS} = 0$ V.

agreement with the experiments since we did not observe SEGR during irradiations.

As mentioned before, these defects are very localized and can cause the breakdown of the oxide in one particular location. Due to this localized nature, we do not observe any shift in threshold voltage for the irradiated devices, which is known to be the standard indicator of oxide trapped charge in MOSFETs. This could be linked to the so-called microdose phenomena but one has to remind that on top of that, we are dealing with one or few cells impacted by a secondary ion, among hundreds of cells in the device.

Impact of non-destructive neutron radiation to drain-to-source breakdown voltage

During the SEB tests, devices which were irradiated at 50% of V_{DSmax} (450 V), did not exhibit SEB before the neutron beam was stopped at 2×10^{10} cm⁻² neutron fluence. Also, portion of the devices which were irradiated at 75% of V_{DSmax} (675 V), did not fail during irradiation. In order to determine some possible irradiation-induced long-term reliability degradation, destructive drain-to-source breakdown voltage measurements (V_{BD}) were performed after irradiation for each unfailed component.

Experimental details The irradiation test setup is described in Section 3.3.2. DUT was SiC MOSFET whose electrical characteristics are presented in Table 3.1. Schematics of the V_{BD} test circuit is presented in Figure 3.24. The goal is to observe that at which V_{DS} the device loses its blocking capability. V_{BD} were measured by increasing V_{DS} until a sharp increase in drain-to-source current (I_{DS}) was observed indicating eventually a drain-to-source breakdown. Drain bias was increased in 4 V steps in 1 s steps. V_{GS} was held at 0 V and gate current was monitored with Keysight 2902B SMU.

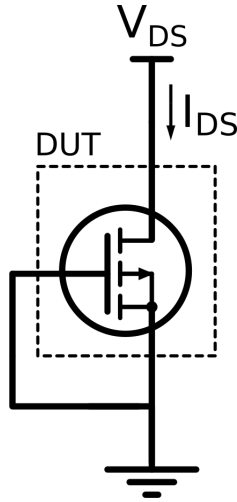


Figure 3.24: Schematics of drain-to-source breakdown voltage test circuit

Results During the destructive post-irradiation V_{BD} measurements are performed, different $I_{DS}V_{DS}$ behaviour have been observed between preliminary stressed and un-stressed devices. In particular, it appears that the electrical stress applied through preliminary constant current stress, statistically leads to a reduction of the V_{BD} . For those devices which exhibited lower V_{BD} , gradual increase in drain leakage current can be observed before the final breakdown. Figure 3.25 represents $I_{DS}V_{DS}$ behavior for two non-irradiated devices (one fresh and one stressed). We observe elevated leakage drain current levels well below the rated V_{DSmax} .

Since the pre-stressing process is related to the gate stress by creating defects in the gate oxide, one would expect to observe also elevated gate current levels during the V_{BD} sweep due to the formed conductive paths. However, no gate current increase was observed before the drain to source breakdown occurred. Thus, the gate current during the V_{BD} test for the stressed device begins to increase only after the breakdown and subsequent overheating of the device (Figure 3.25).

In Figure 3.26, the measured breakdown voltage distributions are reported for different device categories. The two V_{DS} configurations during irradiation (50 % and 75 % of V_{DSmax}) are compiled in the graphic. Non-irradiated and non-stressed devices show small variability in V_{BD} with a mean value of (1247 ± 3) V. Looking at the measured V_{BD} values for stressed (and non-irradiated) devices, a reduction can be statistically observed. Though the V_{BD} decrease is not uniform for all the stressed devices, we can note that the lowest V_{BD} value observed for stressed devices is 720 V. This is well below the V_{DSmax} and indicates a strong decrease in overall reliability of the device. On top of that, since such devices are used in switching operation mode such as in DC-DC converters, they can

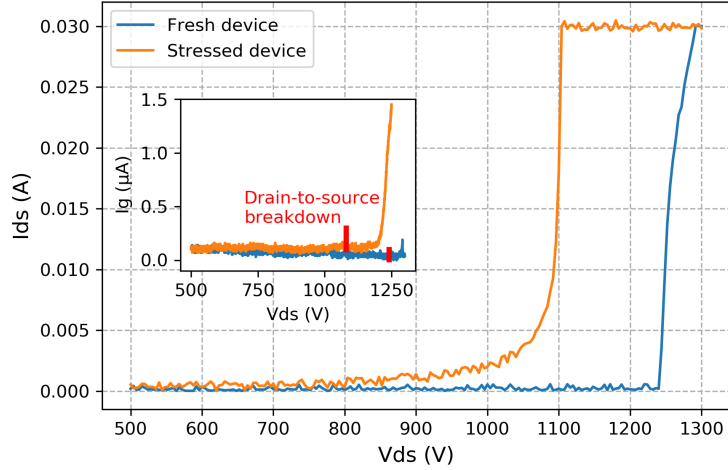


Figure 3.25: $I_{DS}V_{DS}$ -behavior of two non-irradiated devices during breakdown voltage measurement, V_{GS} being grounded. Stressed device exhibits a lower V_{BD} . For this device, the leakage current gradually increases below V_{DSmax} and reaches 2 mA at $V_{DSmax} = 900$ V. As complementary information, gate current during V_{BD} test is shown in the inset graph. The gate current increases after the drain-to-source breakdown of the device occurs, which is indicated with a red line in the inset graph [76].

exhibit current and voltage overshoots during each commutation which amplitude can exceed the expected voltage by 50% [185]. In fact, repeated applications of overvoltage have been shown to result in catastrophic failure [186].

Reducing the breakdown voltage will then intrinsically increase the sensitivity to this failure mode even though devices are subjected to a protective derating.

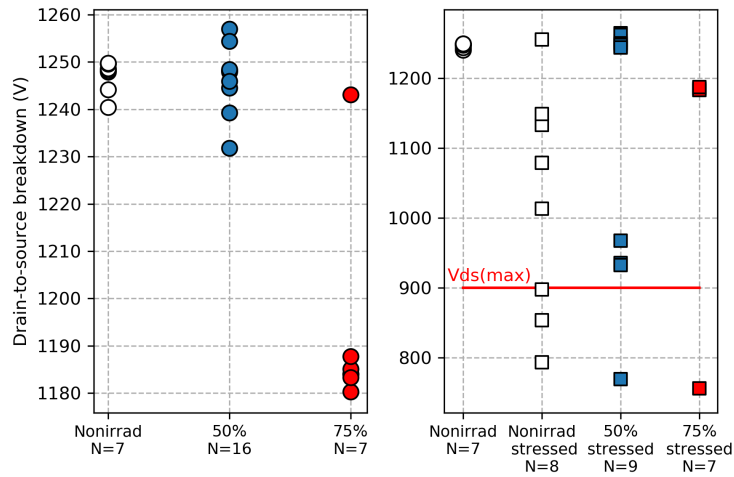


Figure 3.26: Measured V_{BD} -values for unstressed devices (left) and stressed devices (right) with different irradiation configurations. Note that 50% and 75% correspond to the percentage of applied drain bias during irradiation compared to V_{DSmax} . For each plot, V_{BD} values of fresh devices are reported as a common reference [76].

In the left graph in Figure 3.26, we can see that after irradiation in the supposed SOA (50% V_{DSmax}), a wider distribution in V_{BD} values can be observed compared to the low

variability reported for fresh devices. Surviving devices irradiated at 75 % also exhibit a slight decrease in their mean V_{BD} values. These two observations give an indicator of possible device weakening which might be due to localized electrical stresses related to current transients after neutron interaction.

We assume here that the breakdown voltage reduction is likely related to charge generation either modelled by a percolation model (electrical stress) or by very localized trapping induced by secondary ions after primary neutron interaction. However, concerning this latter case, we cannot exclude a possible action of a localized cluster of defects (displacement defects) due to either neutron interaction or secondary ion interaction creating interstitials and vacancies in a localized region. But, presented results in Figure 3.26 tend to indicate that the V_{BD} reduction is depending on the irradiation bias, consolidating the role of transient current after neutron interaction.

TCAD simulations The TCAD tool ECORCE [182] was used to simulate the effects of both pre-irradiation electrical stress and generated secondary ions after neutron interaction. In both cases, the goal is to assess the possible impact on long-term reliability of the devices. Electrical stress was simulated by creating trapped charges in the gate dielectric (oxide traps) and in the semiconductor-dielectric interface (interface traps). As a first approach, uniform spatial distribution of trapped charge was applied and 1 eV trap energy level for the interface traps was used as indicated in [187]. Neutron interaction was simulated by considering silicon ions as the secondary product of neutron collision with lattice atoms. The geometry model used for the simulations is presented in Figure 3.21 and parameters used are listed in Table 3.10. Those parameters have been found to be the best suited to fit simulation results with experimental electrical characteristics as indicated in Figure 3.27.

Electrical stress simulation Aging effects are modelled in ECORCE by creating defects both in the semiconductor and dielectric material. These defects act as traps for charge carriers, which affect the electrostatics in the device structure. Interface defects are then modelled by a thin layer of traps on the oxide-semiconductor interface and in the semiconductor side. As mentioned in the previous section, a negative shift in V_T after electrical stress was observed in the experiments. Also, as observed in the inset graph of Figure 3.17, a slight change in the subthreshold slope was observed. We used these results to extract N_{it} and N_{ot} densities generated during electrical stress using method described in [32]. Finally, change of trapped charge at the interface ($\Delta N_{it} = 8.8 \times 10^{10} \text{ cm}^{-2}$) and in the oxide ($\Delta N_{ot} = 4.6 \times 10^{16} \text{ cm}^{-3}$) have been found. The simulated $I_{DS}V_{GS}$ curves for fresh and stressed devices are compared with the experimental ones in Figure 3.27.

As one can see in Figure 3.28, for fresh devices, a simulated breakdown occurs when the V_{DS} reaches approximately 1400 V, which is a bit higher than expected from experimental results. However, when looking at stressed device behavior, a drain-to-source leakage current increase can be observed below the V_{DSmax} and the breakdown seems to occur well below V_{BD} of the fresh device and also below the V_{BD} of the real device which was found to be about 1250 V. Note that the V_{BD} values extracted from simulation are less at stake rather than the relative difference between them due to electrical stress impact. We remind that a leakage behavior was also observed in experimental results for stressed devices (Figure 3.25), supporting the simulated results.

To look more closely on the mechanism which eventually causes the increased leakage current during the breakdown, the current density in the device has been analyzed during

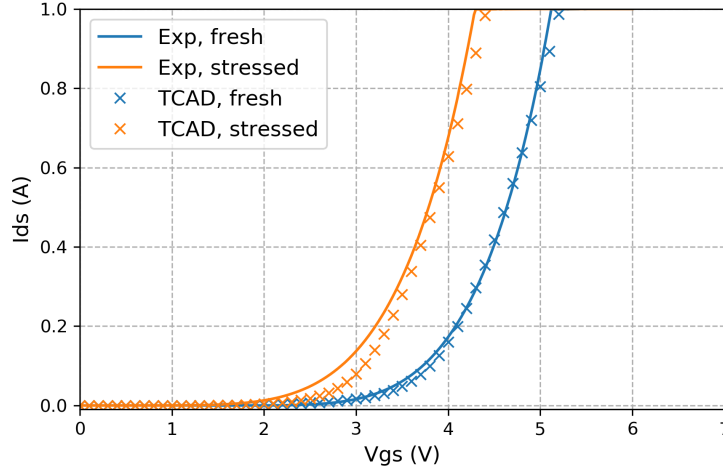


Figure 3.27: Experimental (solid line) and simulated (dashed line) $I_{DS}V_{GS}$ -characteristics before and after electrical stress for non-irradiated devices. Electrical stress effects are modeled in TCAD simulations by adding interface and oxide trapped charge. $V_{DS} = 10\text{ V}$ during the sweep.

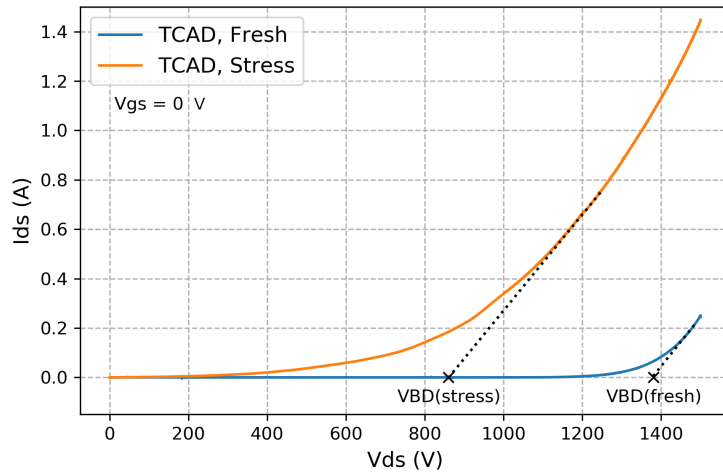


Figure 3.28: Simulated drain to source breakdown voltage measurement through $I_{DS}V_{DS}$ -characteristics for fresh and stressed device model.

the drain-to-source breakdown measurement simulation. In particular current densities have been reported in Figure 3.29 at the breakdown voltage points for fresh and stressed devices ($V_{BD(Fresh)} = 1375\text{ V}$ and $V_{BD(Stressed)} = 850\text{ V}$). As observed in Figure 3.29, on the left, in the case of the fresh device, we can see that the current flows mainly through the reverse biased body diode which goes into avalanche mode. On the right, for a simulated stressed device, an inversion channel is formed due to the injected charge in the gate area and when V_{DS} is high enough, the current flows through the channel, even when the device should be in off-state.

Heavy ion interaction simulation Since we observed lower V_{BD} value and increased leakage current with the stressed device model due to charge buildup in the oxide area, the impact of a secondary ion generated after primary neutron interaction has been simulated. To this end, a silicon recoil has been generated into the device structure, the

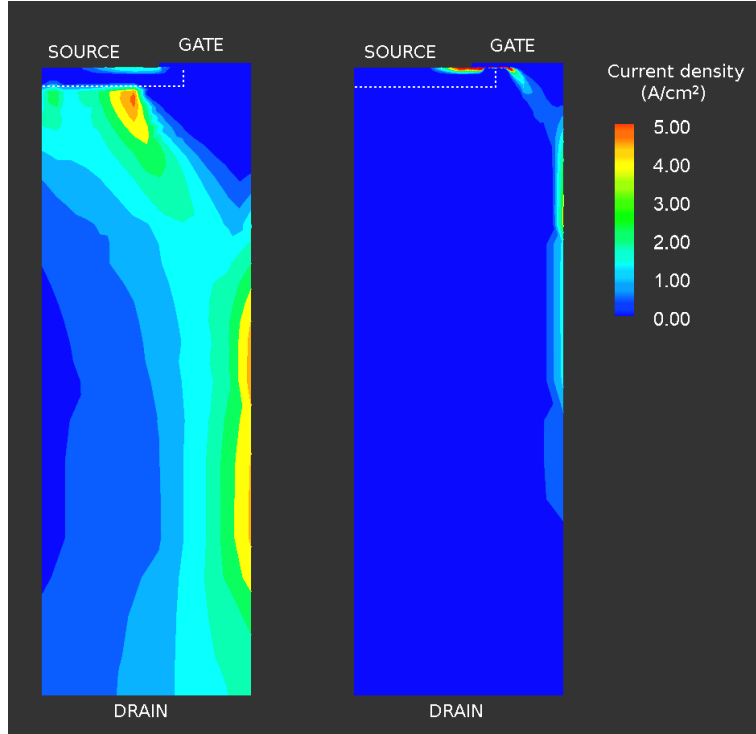
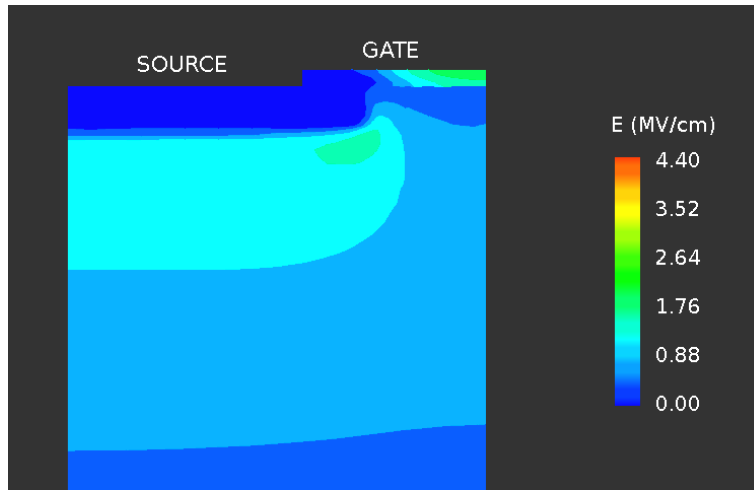


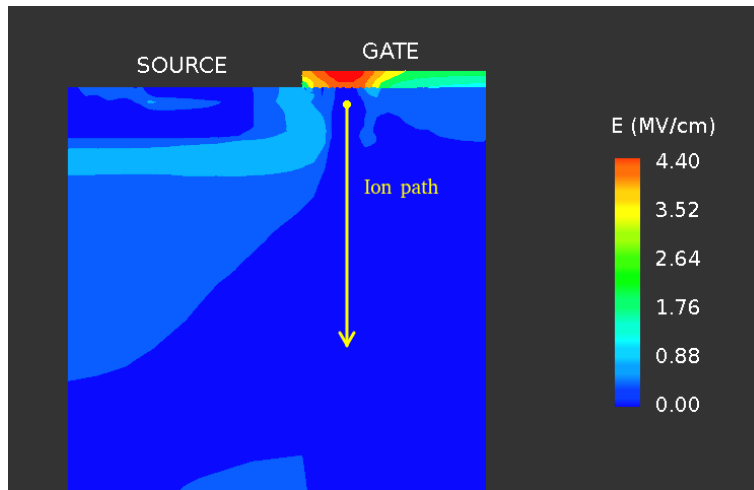
Figure 3.29: TCAD simulated current density (A/cm²) in the device for fresh (left) and stressed (right) device at their breakdown voltage, for $V_{DS} = 1375$ V (fresh) and $V_{DS} = 850$ V (stressed). Fresh device exhibits breakdown through the avalanche of the body diode whereas the electrically stressed device goes into inversion and the current flows through the channel [76].

transistor being biased at 675 V (75 % of V_{DSmax}), in order to see if non-destructive single events can cause similar effects as electrical stress and further affect the long-term reliability of the device. Electric field in the non-stressed device was simulated before, during and after the ion impact and result is presented in Figure 3.30.

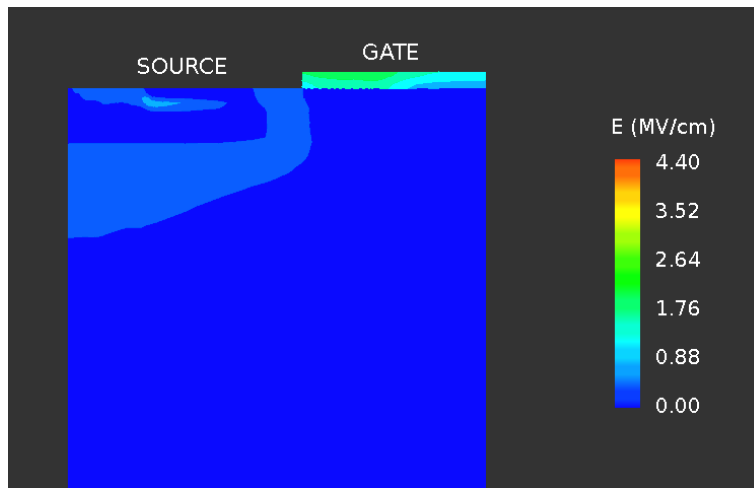
A high localized electric field region (4.4 MV/cm) can be observed in the gate oxide 1 ps after the ion impact (Figure 3.30b). Such high transient electric field leads to current through the gate dielectrics which might result in localized trapped charge buildup in the oxide [178]. Moreover, since this high localized electric field state is short in duration, it appears that 2 ps after ion impact the electric field in the oxide has recovered (Figure 3.30c). Therefore, lower total amount of trapped charge is logically expected during irradiation impact compared to pre-irradiation electrical stress. Due to such localized nature of trapped charge, no significant shift in threshold voltage is observed at the device level for irradiated devices, which is known to be the standard indicator of oxide trapped charge in MOSFETs. In order to assess the effect of localized charge buildup in more detail, current path during the electrical stress as well as transient currents through the oxide during ion impact should be defined to find out the most affected locations in the device. However, the presented results indicate that similar to pre-irradiation stressing, charge buildup in the gate area can happen even during the non-destructive single events caused by neutron interaction due to high electric field state in the oxide region during the transient. This trapped charge might then cause the V_{BD} degradation and decrease the long-term reliability of the device, as observed with electrical stressing of the device in both experimental study and TCAD modelling.



(a)



(b)



(c)

Figure 3.30: Simulated electric field at $V_{DS} = 675$ V (75% of V_{DSmax}). The electric field before the ion impact (a), 1 ps after the ion impact (b) and 2 ps after the ion impact (c), when the electric field has decreased close to its original value [76].

3.3.9 Total ionizing dose sensitivity of SiC MOSFET

The aim of this study is to assess the sensitivity of the SiC power MOSFET to TID under X-ray radiation and how the sensitivity is affected by the pre-irradiation electrical aging. Therefore, two sets of devices were irradiated and the results are compared. One set of devices is maintained without any preliminary aging whereas the other set is exposed to electrical aging.

Experimental details

DUTs and test setup Device under test is commercial C3M0120090D SiC MOSFET manufactured by Cree. Given maximum electrical ratings are $V_{DS} = 900\text{ V}$, $I_{DS} = 23\text{ A}$ and $R_{on} = 120\text{ m}\Omega$ (Table 3.1). DUTs were connected in parallel configuration on the test board. Test board schematics is presented in Figure 3.31. Total of 18 devices were irradiated of which 5 were exposed to electrical stress which is described in the next subsection.

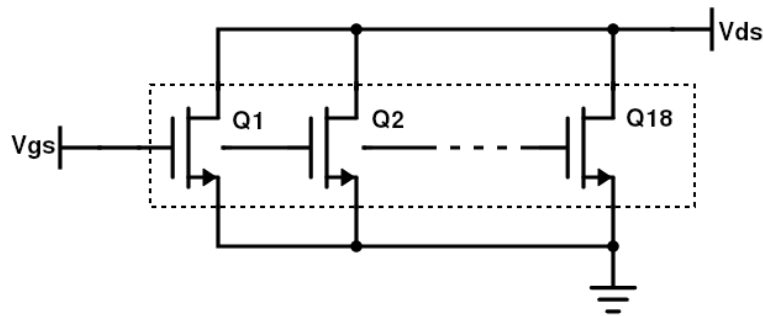


Figure 3.31: TID test board schematics. Devices were connected in parallel configuration during irradiation.

Aging method A constant current stress (CCS) has been performed on 5 devices by applying a current through the gate oxide while keeping the drain and source grounded. The $100\text{ }\mu\text{A}$ constant current was applied for 100 s resulting in a final injected charge of 10 mC . All the 5 devices have been subjected to the same stress with an identical 10 mC injected charge. This first process was intended in order to create some defects inside the active gate oxide layer. More details of the method are described in Section 3.3.8.

The electrical characterizations before aging and before and between irradiation steps included I_{DS} and I_{GS} measurements, while V_{GS} was swept from 0 V to 6 V while $V_{DS} = 100\text{ mV}$.

Radiation environment The irradiations were performed at the University of Montpellier, Institute of Electronics and Systems (IES) by using the on-site X-ray cabinet (X-RAD 320). The University of Montpellier PRESERVE platform has been funded thanks to the financial support of the Region Occitanie and the European Regional Development Fund [188]. 320 keV electron gun energy and current of 12.5 mA were used. The DUTs were subjected to X-ray radiation at room temperature (RT). During irradiation, 80% of V_{DSmax} rating (720 V) was applied at the drain and maximum negative bias ($V_{GS} = -4\text{ V}$) was applied at the gate to make sure that the transistor was in off- state, even in

case of a strong shift in V_T . Final accumulated dose of 1 Mrad was used with average dose rate of 14.75 rad/s.

Results

The IV -characteristics of the devices were investigated and effect of ionizing radiation on $I_{DS}V_{GS}$ -characteristics for one device is presented in Figure 3.32.

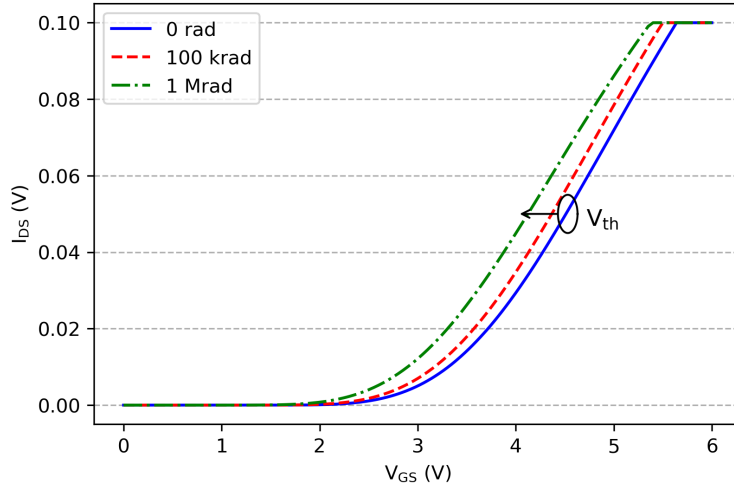


Figure 3.32: $I_{DS}V_{GS}$ -characteristics of the unstressed device after TID. We can observe a shift to the left of the $I_{DS}V_{GS}$ -curve indicating a negative shift in threshold voltage due to irradiation.

As expected, we observe that $I_{DS}V_{GS}$ -curve shifts to the left due to ionizing irradiation induced charge trapping in the oxide layer. Threshold voltages (V_T) were determined using the drain current ratio method [189]. In such method, $\frac{I_{DS}}{g_m}$, where g_m is transconductance, is plotted as a function of V_{GS} . Then, V_T is found at the intercept of the x-axis and tangent line placed at the linear part of the curve (Figure 3.33).

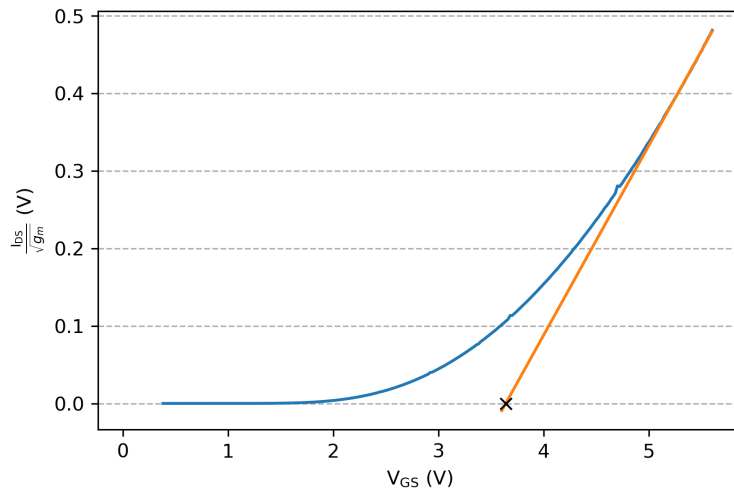


Figure 3.33: Threshold voltage extraction with drain current ratio method

As mentioned in Section 2.2.1, change in $I_{DS}V_{GS}$ -characteristics due to ionizing ra-

radiation is contributed by charge trapping in the gate oxide as well as at the oxide-semiconductor interface. Based on the previous study for silicon devices [32], contributions of interface and oxide traps on threshold voltage shift were determined based on shift in midgap voltage (V_{mg}). While the method in [32] is specifically developed for Si technology and for Si/SiO₂ interface, a recent article [40] used it to show the impact of the negative bias on the accumulation of positive charges in the gate oxide which validate this method for SiC based MOSFETs. Figure 3.34 represents the evolution of the measured threshold voltage shift as a function of TID for stressed and unstressed devices, as well as contributions of the oxide (V_{Not}) and interface traps (V_{Nit}).

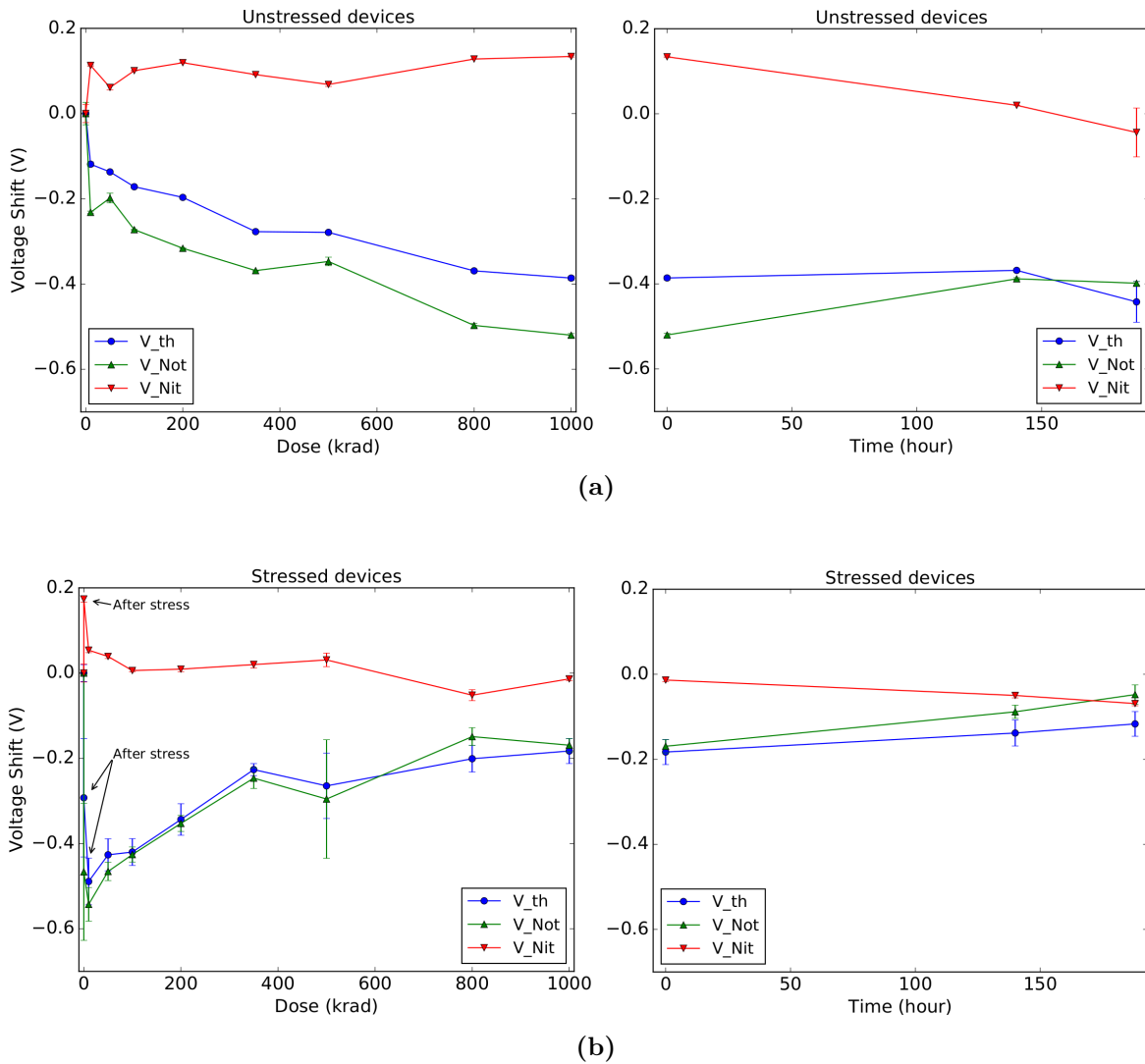


Figure 3.34: Threshold voltage shifts and contribution of oxide and interface traps on threshold voltage shift of SiC MOSFET. Left part of the figure represents the threshold voltage shift due to accumulated dose while right part shows the effect of room temperature annealing after irradiation on the threshold voltage.

We can see that unstressed devices exhibit approximately -0.4 V threshold voltage shift at 1 Mrad and the trend is monotonous and decreasing with accumulated dose. The degradation seems to be mainly driven by the oxide trapping for both stressed and

unstressed devices. Interestingly, regarding preliminary stressed devices, the behaviour of their threshold voltage is different. It can be seen in Figure 3.34 that after the first 10 krad irradiation step, the threshold voltage shifts approximately -0.5 V but after that, it starts to recover. The most significant shift occurs due to the electrical stressing. The opposite trend in threshold voltage for stressed devices suggests that defects created during the electrical aging are removed due to the energy transferred by X-ray irradiation and/or voltage applied at the gate. Since the V_{GS} was negative during irradiation and positive during aging, negative irradiation gate bias could result in removal of traps generated during the aging.

The annealing behaviour for the stressed and unstressed devices was also studied and results are presented in Figure 3.34. We can note that no significant recovery of threshold voltage was observed after 188 h of RT annealing for neither unstressed nor stressed devices. In order to study the defect-induced leakage current through the gate oxide, $I_{GS}V_{GS}$ -characteristics of the stressed devices were measured before stressing, after the electrical stress and between the irradiation steps. A typical characteristics is presented in Figure 3.35.

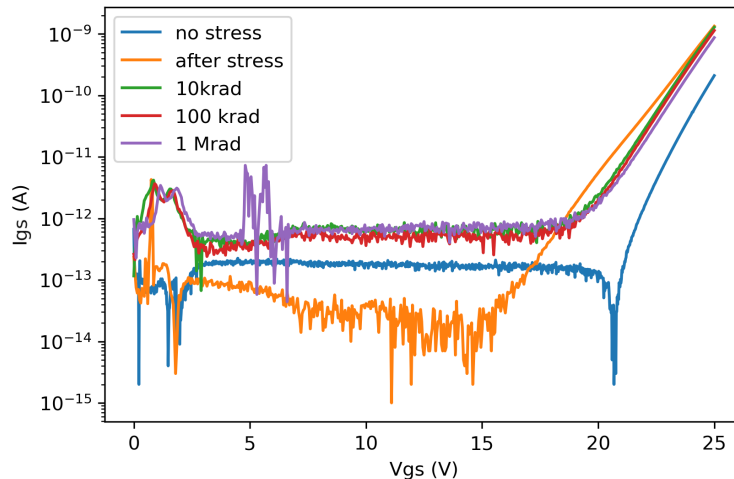


Figure 3.35: $I_{GS}V_{GS}$ -characteristics of the SiC MOSFET at different accumulated dose values.

$I_{GS}V_{GS}$ -characteristics confirm that the most significant shift in V_T occurs due to the electrical stressing. Similarly, the stressing alone has strongest effect on the $I_{GS}V_{GS}$ -characteristics. It can be seen in Figure 3.35 that the region where the leakage current starts to increase, known as Fowler-Nordheim (FN) regime, shifts left due to the stressing but moves in the opposite direction along with increasing ionising dose. Same trend was observed in V_T for stressed devices. Stress-induced shift to the left in $I_{GS}V_{GS}$ -characteristics has also been observed in [166]. Since the defects act as a precursor for the leakage current through the oxide, lower current in the FN-regime should indicate lower defect density in the oxide volume. Such behaviour supports the assumption of decreasing density of defects with increasing accumulated dose.

3.3.10 Total ionizing dose sensitivity of GaN HEMT

As already discussed in Section 2.2.1, the mechanisms for TID induced device parameter degradation in GaN HEMTs are somewhat different compared to mechanisms in Si- and

SiC-based technologies. Due to absence of active gate oxide, oxide trapped charge should not play a role in V_T shift. However, the defects in the semiconductor material and activation of the traps due to ionizing radiation cause similar effects in device parameters than in MOSFET technologies, such as shift in V_T and transconductance degradation. In this study, the effect of ionizing X-ray radiation on the threshold voltage shift of COTS GaN HEMT was studied.

Experimental details

The DUT was EPC2012 GaN HEMT manufactured by EPC. The details of the DUT is given in Table 3.1. Devices were irradiated with X-rays and the radiation environment was similar as described in Section 3.3.9 During irradiation, devices were biased at $V_{DS} = 160$ V which is 80 % of their rated maximum V_{DS} while $V_{GS} = -5$ V was applied which is the maximum safe negative gate bias given by the manufacturer. 18 devices in total were irradiated in parallel configuration.

Results

The shift in V_T as a function of accumulated dose is presented in Figure 3.36. Strongest shift occurs at 50 krad accumulated dose and after that point, the V_T starts to return towards the pre-irradiation value. The monotonous trend in V_T shift as a function of dose observed for Si and SiC devices is not observed here, which is not unexpected. The saturation of V_T shift has been reported for GaN devices earlier, as mentioned in Section 2.2.1.

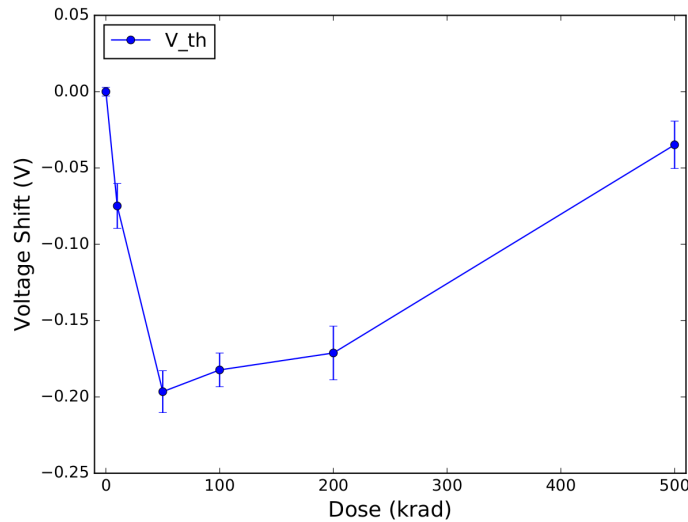


Figure 3.36: The threshold voltage behaviour of EPC2012 GaN HEMT under X-ray irradiation. 18 devices were irradiated in parallel configuration.

Ionizing radiation induced positive charge trapping in the AlGa_N and GaN layers results in threshold voltage shift. Such devices have been observed to be susceptible for electrical stress induced V_T shift. Therefore, the DC bias applied during the irradiation can also contribute to the overall shift observed during the experiment. Therefore, in the future studies, it should be mandatory to have reference devices out from the radiation

field, which are biased in similar configuration and same duration than the irradiated ones in order to differentiate between electrical stress effects and radiation effects.

3.3.11 Impact of degraded device at system level

When being used in application, power transistor is in the core of the switching power converter system, such as DC-DC-converter, where the switching functionality of the transistor allows the voltage and current conversion. Usually, when power transistor exhibits SEB, it is considered to be totally failed and therefore unable to function as a switch. Therefore, the converter is expected to fail along the failure of the transistor. In our case, we have observed SEB of SiC Power MOSFETs due to neutron irradiation. Electrical characteristics of failed device are shown on Figure 3.37. The IV-characteristics of the failed device show that even when the device is considered as failed in component testing under neutron irradiation, it can maintain some of its functionality and still has some of its blocking capability left.

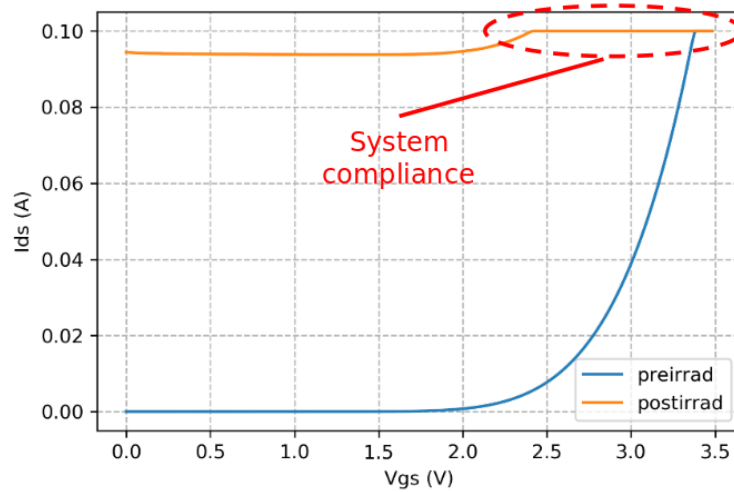


Figure 3.37: $I_{DS}V_{GS}$ -characteristics of partially failed device which was irradiated with atmospheric neutrons. $V_{DS} = 10$ V during the characterization.

In order to better understand the power system behaviour after device failure, the circuit simulation model was developed and simulated in LTspice software [190]. The schematics of the simulation model is presented in Figure 3.38. LTspice simulations were performed by using the MOSFET and diode models provided by the manufacturer [191].

To gather experimental inputs to our Spice simulations, we have also developed a boost converter (Figure 3.39) for which the evolution of system output was investigated. The converter was designed in order to have 1.25 boost ratio with 500 V of maximum output voltage ($V_{out(max)}$) with 1 A of output current (I_{out}). The converter was connected to a external 500Ω resistive load. The boost ratio and input current (I_{in}) as a function of input voltage (V_{in}) for the full operating range is presented in Figure 3.40 for both simulated and developed converter. The simulated and measured curves confirm that the developed converter is working as expected.

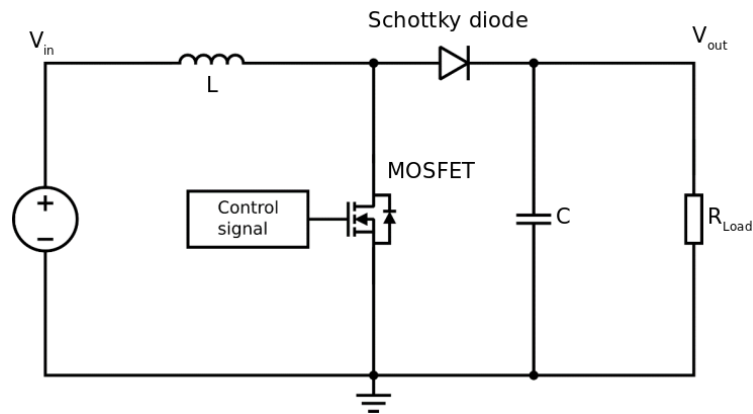


Figure 3.38: Electrical schematics of developed and simulated DC-DC-converter.

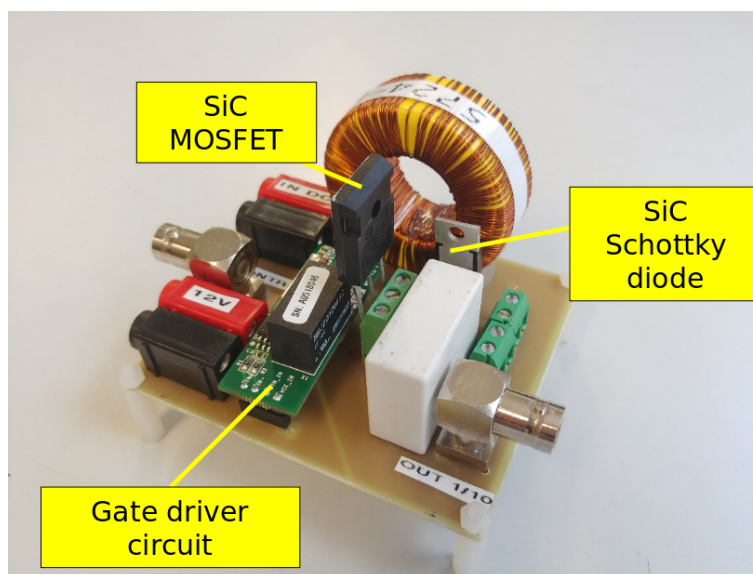


Figure 3.39: Photo of the developed DC-DC-converter unit.

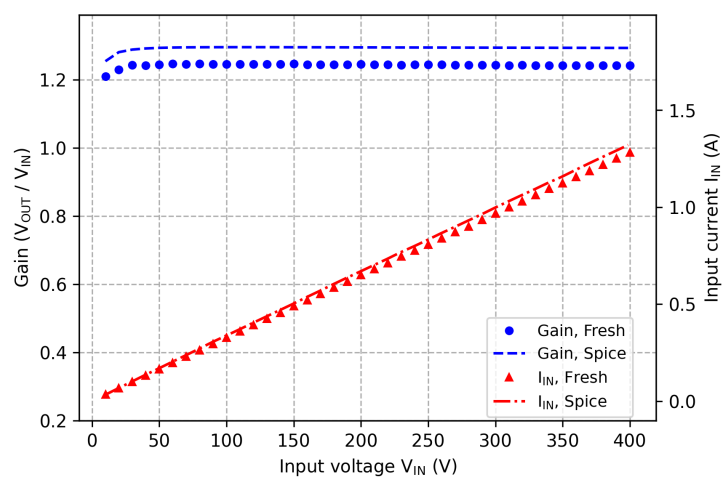


Figure 3.40: Boost ratio and input current of the DC-DC-converter as a function of input voltage.

In order to better understand the impact of failure at system level, a failed device simulation model was created by inserting a parallel resistor, as shown in Figure 3.41. The purpose of this model is to have similar $I_{DS}V_{GS}$ -behaviour than the failed device shown in Figure 3.37. This degraded model was implemented into our simulation of DC-DC boost converter circuit.

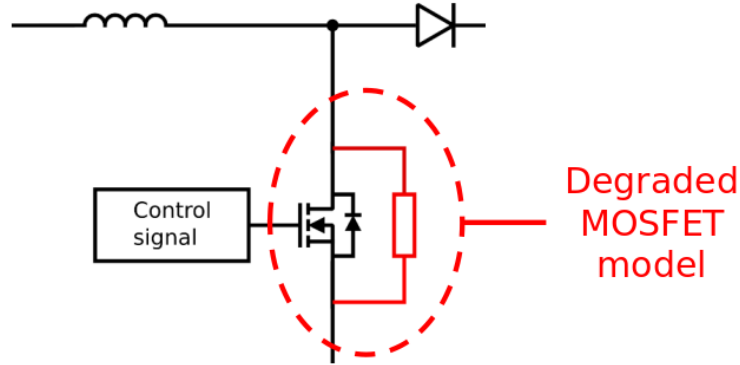


Figure 3.41: Electrical schematics of degraded device model implemented in LTspice.

Both fresh and degraded devices and simulation models were implemented into the simulated and developed converters and system responses in all cases were compared. We have compiled all the results in the Figure 3.42. Output voltage gain ($\frac{V_{out}}{V_{in}}$) and I_{in} as a function of the V_{in} are represented for fresh and degraded devices.

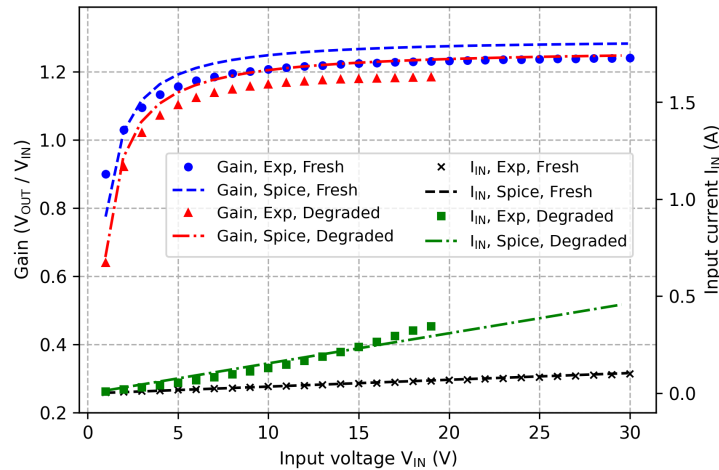


Figure 3.42: The voltage gain and input current of the DC-DC-converter as a function of input voltage V_{in} for simulated converter with fresh device model and experimental data for converter either with fresh or degraded device implemented.

We can see that the voltage gain of the system with the degraded device is slightly lower compared to the output of the system with fresh device. However, the system with the degraded device is still stepping up the voltage and working as a boost converter. This is due to the fact that despite the strong degradation observed in the $I_{DS}V_{GS}$ -characteristics (Figure 3.37), degraded device has some of its blocking capability left.

Due to this degradation and leakage current in OFF-state, we observe a higher system input current compared to the system with fresh device (Figure 3.42). After reaching 20 V input voltage, we see a sharp decrease in the gain and increase of the input current up to the compliance level of the power supply due to the loss of blocking capability of degraded device.

To finalize the study of the boost converter, the power efficiency as a function of input voltage are calculated and presented in Figure 3.43. The curves for the simulated converter with fresh device and from experimental data of the converter with either fresh or degraded device are represented. As expected, when a fresh device is implemented in the converter, the efficiency increases towards an efficiency of 97 % for 30 V. Experimental results obtained with the degraded device show the strong effect of the neutron irradiation on the power converter efficiency. In the future it would be important to identify the mechanisms at play and to estimate the parameters which influence the efficiency of the DC-DC converter especially dealing with degraded device by neutron irradiation.

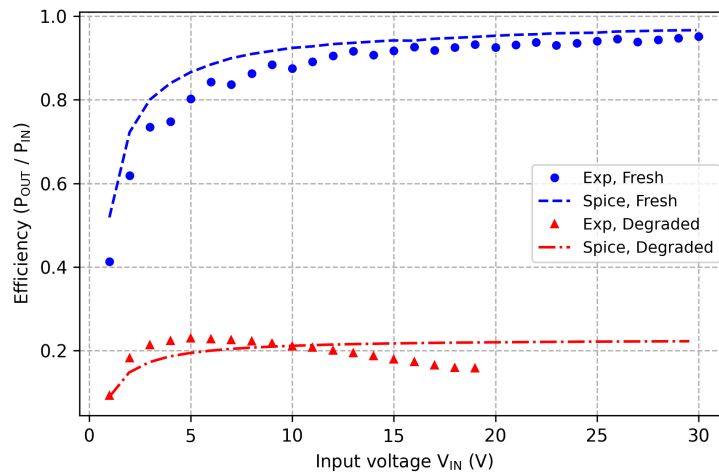


Figure 3.43: Conversion efficiency for developed and simulated converters

3.4 Conclusions

In the first part of the experimental study, Single Event Burnout sensitivity of 3rd generation (and latest available today) SiC MOSFETs under neutron irradiation was assessed. The impact of both drain and gate biases applied during irradiation were evaluated. Reliability parameters as well as the failure rates for avionic and ground applications were then extracted by proposing a novel statistical methodology. First, the SEB sensitivity of this device generation was evaluated, drawing also the sensitivity law along with applied drain voltage for this device generation. In addition, we studied if by applying additional negative gate bias voltage during irradiation testing, the probability for destructive failure would be affected.

In the second part, coupled radiation and aging effects of SiC MOSFETs under neutron irradiation were considered and studied. For this, we used two aforementioned approaches. Post-irradiation electrical stress tests revealed indicators of device weakening due to non-destructive neutron interaction. The effects of pre-irradiation electrical stress on SEB

sensitivity were studied and examined by comparing SEB sensitivities of fresh and electrically stressed devices. Moreover, TCAD simulations were performed with ECORCE software, in order to identify and address the physical mechanisms behind device failure and degradation.

On top of the SEE studies, total ionizing dose (TID) response between fresh and stressed devices were compared up to 1 Mrad accumulated dose. V_T shift and contribution of oxide and interface traps were analysed. Difference in V_T behaviour was found between fresh and stressed devices and in both cases the V_T was mainly driven by oxide trapped charge.

To complete the study, first steps were taken towards system level study by developing a simple power switching converter and implementing a failed device to see how partially failed device affects system performance. It was found that even if the device is defined as failed during the SEB testing, it can still be partly functional and the power system was not fully dysfunctional when partially failed device was implemented. However, the increased power dissipation and temperature would likely cause issues at system level.

General conclusions and perspectives

The long term-reliability of WBG power devices in radiation environment have been evaluated, studied and analysed through experimental analysis and modeling. Three interdependent lines of research were considered: 1) the degradation of the device, 2) the effect of device aging on its radiation sensitivity and 3) effect of radiation on the long term reliability of the device/system.

Based on the results obtained in this study, despite their attractive properties, WBG power devices still have some reliability issues when operating in radiation environments. On top of the sudden failures, radiation induced aging and leakage currents can compromise the functionality of the power system. Even though, WBG power devices have some similarities in their failure mechanisms compared to Si-based devices, the radiation test standards for Si-devices are not directly applicable to WBG-based devices.

Protective derating of such devices is common practice when operating in harsh environments such as in space and avionic applications. It seems that regarding the radiation induced failures 50% derating is SOA for devices tested in this study. According to results obtained during this work, devices which were irradiated at 50% of V_{DSmax} , did not exhibit destructive failure nor showed signs of parameter degradation due to neutron interaction. However, electrical stress has been observed to cause reduction in device SOA. Therefore, conducting more research in coupled aging and radiation effects would be relevant. However, especially when working with neutron-induced failures of stochastic nature, sufficient statistics is important. Therefore, future studies should be performed with higher number of devices in order to be more confident in the results found during this study.

In order to obtain more information about effects of different degradation modes on radiation sensitivity, standard stress tests for devices should be performed by applying more pre-irradiation stress modes with different magnitudes, such as high temperature bias stress with different temperature and with positive and negative biases, electrical stress with different magnitudes and dynamic mode stress (switching). On top of the standard electrical characterizations, low frequency noise measurements are needed to reveal more information about reliability degradation mechanisms. Also, due to fundamental technological differences between SiC and GaN power devices, most critical degradation mechanisms regarding their radiation sensitivity should be identified for respective technology.

Further work in the effect of degraded device on power system performance is needed. Improving the system level Spice simulation by developing degraded device model and implementing it to the simulated circuit would allow prediction of the system level effects in various types of power systems. For that purpose, more complete characterization schemes for failed and especially degraded devices need to be applied.

Publications

Journal papers:

- **K. Niskanen**, R. Coq Germanicus, A. Michez, F. Wrobel, J. Boch, F. Saigné and A. D. Touboul, "Neutron induced failure dependence on reverse gate voltage for SiC Power MOSFETs in atmospheric environment," *IEEE Transactions on Nuclear Science*, 2021 [173]
- **K. Niskanen**, A. D. Touboul, R. Coq Germanicus, A. Michez, A. Javanainen, F. Wrobel, J. Boch, V. Pouget and F. Saigné, Impact of electrical stress and neutron irradiation on reliability of silicon carbide power MOSFET, *IEEE Transactions on Nuclear Science*, vol. 67, no. 7, July 2020 [76]
- A. Coronetti, R. Garcia Alia, J. Budroweit, T. Rajkowski, I. Lopes, **K. Niskanen**, D. Söderström, C. Cazzaniga, R. Ferraro, S. Danzeca, J. Mekki, F. Manni, D. Dangla, A. Koelpin, V. Pouget, F. Saigné, P. X. Wang, A. Touboul, A. Javanainen, H. Kettunen, R. Coq Germanicus, "Radiation hardness assurance through system-level testing: risk acceptance, facility requirements, test methodology and data exploitation," *IEEE Transactions on Nuclear Science*, 2021 [192]
- Tomasz Rajkowski, Frédéric Saigné, **Kimmo Niskanen**, Jérôme Boch, Tadeo Maraine, Pierre Kohler, Patrick Dubus, Antoine Touboul, Pierre-Xiao Wang, "Comparison of the Total Ionizing Dose sensitivity of a System in Package Point of Load converter using both component and system level test approaches," *Electronics*, 2021 [193]

Conference papers:

- **K. Niskanen**, A. D. Touboul, R. Coq Germanicus, A. Michez, F. Wrobel, J. Boch, V. Pouget and F. Saigné, "Aging and gate bias effects on TID sensitivity of wide bandgap power devices," RADECS 2018 Data Workshop, Gothenburg, Sweden
- **K. Niskanen**, A. D. Touboul, R. Coq Germanicus, A. Michez, F. Wrobel, J. Boch, V. Pouget, P. Girones, S. Morand, O. Crepel, C. Weulersse, C. Binois and F. Saigné, "Silicon carbide power MOSFETs under neutron irradiation: Failure In Time demonstration and long term reliability degradation evaluation," IEEE NSREC 2019, 8th-12th July 2019, San Antonio, USA
- **K. Niskanen**, A. D. Touboul, R. Coq Germanicus, A. Michez, A. Javanainen, F. Wrobel, J. Boch, V. Pouget and F. Saigné, "Impact of electrical stress and neutron irradiation on reliability of silicon carbide power MOSFET," RADECS 2019, Montpellier, France

- **K. Niskanen**, A. D. Touboul, R. Coq Germanicus, A. Michez, F. Wrobel, J. Boch, V. Pouget and F. Saigné, "Single Event Burnout dependence on reverse gate voltage for SiC Power MOSFETs in atmospheric environment," RADECS 2020
- T. Rajkowski, F. Saigné, **K. Niskanen**, J. Boch, T. Maraine, P. Kohler, P. Dubus, A. Touboul and P. X. Wang, "Analysis of system level TID test results of a System in Package Point of Load converter," NSREC 2020
- Andrea Coronetti, R. Garcia Alia, J. Budroweit, T. Rajkowski, I. Lopes, **K. Niskanen**, D. Söderström, C. Cazzaniga, R. Ferraro, S. Danzeca, J. Mekki, F. Manni, D. Dangla, A. Koelpin, V. Pouget, F. Saigné, P. X. Wang, A. Touboul, A. Javanainen, H. Kettunen, R. Coq Germanicus, RHA through System Level Testing: Risk Acceptance, Facility Requirements, Test Methodology and Applications, NSREC2020

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TITLE: Coupled radiation and aging effects on wide bandgap power devices

ABSTRACT

Power electronic components operating in radiation environments are exposed to different types of radiation effects such as single event, dose and displacement damage effects, which affect the device functionality through device failure or degradation. On top of the radiative stress, electronic devices in operating mode are exposed to aging effects which can have an effect on the device reliability. The individual or coupled interaction of such effects may cause a failure of the device or the whole system. In order to ensure reliable operation of electronic systems, it is important to assess those effects through testing and simulations.

Recently, wide bandgap (WBG) materials such as SiC and GaN have been introduced into commercial power semiconductor device technologies as a candidate for replacing Si as a semiconductor material. However, their physical failure and degradation mechanisms are still not fully known. On top of that, since the technologies have developed, the test standards used for power devices testing in radiation environments, have not been brought up to date to be used with emerging technologies.

In this work, short- and long-term reliability of commercial off-the-shelf (COTS) WBG power technologies under radiation environment are investigated. Methodology for calculating reliability parameters and failure rates for SiC power technology in atmospheric radiation environment is proposed. Moreover, radiation sensitivity of SiC and GaN power technologies are assessed for SEE and TID supplemented by TCAD simulations.

Coupled radiation and aging effects are studied through comparing radiation sensitivity of pristine and aged devices and through post-irradiation stressing in order to address the radiation induced reliability degradation. On top of that, power system radiation induced performance degradation is studied through experiment and SPICE simulation.

TITRE: Effet des radiations sur les composants de puissance grand gap

RESUME

Les composants électroniques de puissance fonctionnant dans des environnements radiatifs sont exposés à différents effets induits par les rayonnements tels que les effets singuliers, les effets de dose ionisante et les effets de dose de déplacement, qui affectent la fonctionnalité du dispositif en provoquant une défaillance ou une dégradation de ses performances. En plus du stress radiatif, les dispositifs électroniques en fonctionnement sont exposés aux effets du vieillissement qui peuvent avoir un effet sur la fiabilité du dispositif. L'interaction individuelle ou couplée de ces effets peut provoquer une défaillance du dispositif ou du système entier. Afin d'assurer un fonctionnement fiable des systèmes électroniques, il est important d'évaluer ces effets par des tests et des simulations.

Récemment, des matériaux à large bande interdite (WBG) tels que le SiC et le GaN ont été introduits dans les technologies commerciales de dispositifs semi-conducteurs de puissance comme candidats au remplacement du Silicium comme matériau semi-conducteur. Cependant, leurs mécanismes physiques de défaillance et de dégradation ne sont pas encore totalement connus. De plus, depuis que les technologies se sont développées, les normes d'essai utilisées pour tester les dispositifs de puissance dans des environnements de rayonnement n'ont pas été mises à jour pour être utilisées avec les technologies émergentes.

Dans ce travail, la fiabilité à court et à long terme des technologies d'alimentation WBG du commerce (COTS) dans un environnement radiatif est étudiée. Une méthodologie de calcul des paramètres de fiabilité et des taux de défaillance pour la technologie de puissance SiC dans un environnement soumis à des rayonnements atmosphériques est proposée. En outre, la sensibilité aux rayonnements des technologies de puissance SiC et GaN est évaluée pour les SEE et TID, complétée par des simulations TCAD.

Les effets couplés des radiations et du vieillissement sont étudiés en comparant la sensibilité aux rayonnements de dispositifs vierges et vieillis et en appliquant un stress post-irradiation afin de traiter la dégradation de la fiabilité induite par les rayonnements. En outre, la dégradation des performances du système d'alimentation induite par les radiations est étudiée par des expériences et des simulations SPICE.