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Charge control in semiconductor quantum-dot arrays and prospects for large-scale integration

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Abstract

The second quantum revolution is underway with the promise of harnessing the full potential of quantum mechanics to develop new technologies. Among these innovations, the field of quantum information theory proposes a new paradigm to perform computation, outside of the classical computing framework based on 0/1 bit of information. Quantum computing offers a way to solve physics and computational problems that cannot be solved in reasonable time by classical computers by introducing quantum-bits (qubits) and quantum logic gates. However, quantum computers are prone to errors, requiring them to encode information from a single logical into multiple physical qubits. Thus, a universal quantum computer outperforming today's supercomputers involves the control of millions of qubits, far from the dozens of qubits in current systems. In this context, spin qubits in quantum-dot (QD) arrays are a good candidate thanks to their compatibility with standard semiconductor manufacturing.

In this thesis, we focus on the charge control of electrons inside arrays of quantum-dots. On the one hand, we demonstrate remote charge sensing in a CMOS nanowire, using an embedded single-lead quantum-dot (SLQD) electrometer. A unique electrode operates each QD, and the device is fabricated on a silicon-on-insulator 300-mm industry-standard fabrication line. We develop different detection schemes to compensate for the device's strong capacitive couplings due to its dense packing. Consequently, we control the different double quantum-dots in a 2x2 QD array and probe the Coulomb disorder inside the structure.

On the other hand, we demonstrate a scalable QD array formed by shared control gates with row/column addressing in a GaAs/AlGaAs heterostructure. Like classical integrated circuits, large-scale quantum-dot arrays must rely on shared controls to reduce the number of interconnects to $\propto \sqrt{N}$, with N the number of QDs. Here, we show the charge control of electrons in a scalable 2x2 QD array isolated from the reservoirs. We characterize the array using the constant interaction model and assess its scalability. To conclude, these two experiments path the way towards charge controls in large-scale semiconductor QD arrays.

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Introduction

At the beginning of the twentieth century, quantum mechanics transformed our understanding of physics by introducing the concept of quantification of energies, momentums, positions, etc. In fact, most *classical* physics theories can be derived from quantum mechanics. The classical physics seems to be only an approximation of our world, valid in the limits of large systems. However, some exotic phenomena exist in the quantum realm, without classical counterparts, such as quantum superpositions and entanglements.

The first quantum revolution and the Information Age.

Over the past century, quantum theories led to leaps in understanding the periodic table, chemical interactions, and semiconductor physics. This first *quantum revolution* brought many of the devices present in our daily lives like MRI imagers, lasers, and more generally semiconductor devices. Among these examples, the most emblematic is the development of the transistor. Following the first functional transistors in 1947 at Bell Labs, the transistor number in integrated circuits had followed an exponential growth given by Moore's law [Moo75].

After decades of research and engineering, billions of transistors can now be integrated into one silicon chip. Such achievements have been possible thanks to the shrinking of the industrial transistors' size from one centimeter to a few tens of nanometers [Joh16]. Moreover, the random variations from transistors to transistors are kept small enough that almost every chip produced will work [Cha09]. In particular, transistors can be combined to build logic gates with ON and OFF values, then assembled to build digital circuits. The digital nature of such circuits tends to relax the constraints on the transistors' variability, allowing to increase the circuits' size drastically. So, all this scaling potential has been harnessed to develop *classical* computing, with improvements in computing power following the same trend as Moore's law. Consequently, today we are living in an information society where information computing units (computers) play an increasingly central role [Ben86].

However, the race towards faster computers is slowing down as the density of transistors hits a plateau. The increasingly smaller dimensions of transistors give rise to new quantum phenomena, not suitable for classical logic computation. Thus, we can no longer consider a transistor as a sizable quantum device ruled by band-gap engineering, but as a collection of interacting quantum objects. Actually, the fine control of nanostructures and the manipulation of individual quantum objects spur a second quantum revolution.

A new computing paradigm brought by a second quantum revolution.

Nowadays, after more than a century of success for quantum theories, a second revolution is underway [Mac03]. First, technological innovations in miniaturization pushed first-revolution devices, such as transistors, directly into the quantum realm at the nanoscale. Then, the principles of quantum mechanics offer the promise of vastly improved performance

for quantum devices over what can be achieved within the classical framework. As a result, the second quantum revolution concerns many different technologies such as quantum sensors, spintronics, quantum materials, but also quantum information science.

Indeed, while transistors' miniaturization has driven classical computing, this has reached a limit. Quantum mechanics offers a new way of processing information, other than the conventional paradigm using classic computer logic. In particular, it introduces a new unit of information : the quantum-bit, or qubit, a bit of information exploiting the potential of quantum mechanics. A qubit is a quantum two-level system, which can be in a 0 or 1 state as a classical bit. However, the qubit can also be set in any linear superposition of the 0 and 1 states, a characteristic without classic counterparts. Such entity is written $\alpha\,|0\rangle + \beta\,|1\rangle$ with $|\alpha|^2 + |\beta|^2 = 1$. The qubit state can be seen as a unitary vector describing a so-called Bloch sphere with south and north poles corresponding to the classical state 0 and 1 [Blo46]. Moreover, multiple qubits may exhibit quantum entanglement, in which case the number of states available grows exponentially with the number of qubits. For example, a 64-qubit system represents 2^{64} states. Thus, by combining quantum superposition and entanglement, these 64 qubits can be placed in any superposition of all the 2^{64} states. In comparison, a typical 64-bit machine can only be set in one of these states at a time.

The development of quantum information systems concerns communications (e.g. quantum cryptography), but also calculations such as simulators and computers. On the one hand, a quantum simulator is designed to map a specific physics problem, either tricky to probe in the laboratory or to simulate on a classical computer, on a well-controlled experimental system. This kind of problem is particularly difficult to emulate on a traditional computer because of the exponentially increasing computational space size, as discussed previously. To illustrate, today's supercomputers can emulate up to 48 qubits in interactions [DR19]. Increasing the number of qubits to 49 requires a supercomputer twice as powerful, while the size of the quantum simulator only increases linearly. Quantum simulators are well suited to simulate quantum problems of all sizes because they obey the same laws.

On the other hand, an ensemble of qubits can function as a programmable universal quantum computer, as originally proposed by Yuri Manin and Richard Feynman in the eighties [Fey82; Man80]. Among the several models of quantum computing, the most common is the quantum circuits representation. It is a model similar to classical computing but with qubits and quantum gates instead of bits and logic gates. Single-qubit gates rotate a qubit inside the Bloch sphere and two-qubit gates entangle qubits. Other models exist but are not necessarily universal and may be limited to specific tasks only. A famous example is the D-Wave implementation of a quantum annealer for minimization problems [Har18; Kin18]. In contrast, an universal quantum computer can simulate *any* quantum problem [Llo96], with applications in materials science, chemistry, pharmaceuticals, among others [Pre18].

Such quantum computers can also solve computer science problems using dedicated quantum algorithms. Well-known protocols like Grover or Shor algorithms allow, respectively, searching in a database, and carrying out integer factorization [Gro96; Sho94]. These two examples are algorithms faster to run on a quantum computer than their non-quantum counterparts on a classical computer with similar resources. Indeed, they both benefit from

a quantum acceleration reducing the problems' complexity to polynomial time instead of non-polynomial for the classical algorithms. In other words, the time required to find an entry in an unsorted database increases linearly with the database size for a quantum computer but exponentially for a classical one. In the information age, it makes a huge difference in many computing problems, and it explains why high-performance computing companies like Atos are investigating quantum computing [ATO20]. Evidence points out that ideal quantum computers should be either as good or faster than an equivalent classical computer to solve any problem [Nie10].

Up to now, there is no such thing as a universal quantum computer powerful enough to solve any quantum problem faster than supercomputers. Efforts are being made to find a quantum system that will be somewhat the equivalent of the transistor but for quantum computing. Many approaches are explored, as we will discuss now.

The challenges of quantum computers

In 2000, David P.DiVincenzo introduced the five conditions necessary to build a quantum computer [DiV00] :

- Limited decoherence over the typical gate duration.
- A scalable system with well characterized qubits.
- The ability to initialize the system in a known state.
- A universal set of single-qubit and two-qubit gates.
- The ability to measure only a specific qubit.

In the next two decades, many platforms were studied to meet these criteria, such as trapped ions [Cir95; Hem18], photonic crystals [EB20; Ige88], superconducting electronic circuits [Aru19; Nak99], dopants [Kan00], and electron-spin trapped in semiconductor quantum-dots [Los98; Yan20]. All these different implementations somewhat fulfill the DiVincenzo criteria. One of the most advanced realizations is Google's 54-qubit superconducting quantum processor called Sycamore. Recently, a quantum algorithm designed to be hard to emulate classically was run on this device to demonstrate a quantum advantage for the first time. It took about three minutes to find the problem solution on Sycamore, whereas today's best supercomputer would require two and a half days [Aru19; Ped19]. However, Sycamore is not equivalent to an ideal 54-qubit computer.

In reality, the experimental realizations of qubits are not perfectly isolated two-level quantum systems. Each qubit interacts with its entire environment and with many degrees of freedom, especially for condensed-matter qubits. For example, the experimentalist must interact with the qubit to apply quantum gates. As a result, a realistic qubit has two decoherence channels : relaxation (decay from state $|1\rangle$ to state $|0\rangle$) and dephasing (accidental rotation along the equatorial axis on the Bloch sphere).

Decoherence has a detrimental effect on the performance of a quantum computer. Indeed, even if a quantum processor works like a digital-machine (the algorithm's solution is coded in the form of a binary word in the qubits classical states), its execution is definitely analog. Quantum gates are used to continuously change the coefficients in the system's linear superposition of states. Thus, each gate must be as precise as possible to give the correct

result, but also short compared to the coherence time to have enough time to apply the various gates in an algorithm. On Sycamore, only 20 cycles could be performed using all the qubits in the quantum processor, where a cycle consists of applying one single-qubit and one two-qubit gate on each qubit. In the short term, we can accept the error rates of current qubit implementations and benefit from a quantum advantage for specific applications only (e.g., algorithms with only a few quantum gates). In this context, Google's device paths the way towards Noisy Intermediate-Scale Quantum (NISQ) computers with 50 to 100 qubits, as described in [Pre18].

In the long run, one way to build a universal quantum computer is to create sufficient layers of redundancy by encoding the information of a single qubit over many so-called *logical qubits*. The number of *physical qubits* required to build a single error-resistant logical qubit depends on the characteristics of the physical qubits (decoherence time, connectivity, etc.) [Dev13; Jon12]. For the qubit implementations described previously, such quantum error correction protocols imply as much as 10^3 to 10^4 physical qubits per logical one [Fow12; Mar15]. So, scalability is one of the main challenges of quantum computers since millions of qubits have to be controlled to compensate for the decoherence mechanisms.

Semiconductor electron-spin qubits for large-scale quantum computers.

A potential candidate for a large-scale quantum computer is the electron-spin qubit trapped in semiconductor quantum-dots (QDs).

First, as a spin-$\frac{1}{2}$ particle, a single electron experiencing a static magnetic field is a natural two-level quantum system. It is only coupled to direct magnetic noise within the nanostructure, and indirectly coupled to charge noise via phenomena such as spin-orbit. As we will discuss, strategies aimed at considerably reducing the magnetic noise lead to coherence times of the order of the microsecond for electron-spin qubits [Blu10; Vel15]. Spin states can be manipulated via addressable microwave excitations [Kop06] or magnetic field gradients [PL08], and coupled by tuning the exchange coupling between two adjacent dots [Pet05]. In addition, spin-qubits using more than one electron have been proposed or demonstrated, such as singlet-triplet with two electrons in two dots [Mau12], exchange-only (three electrons in three dots) [Rus17], and exchange-only singlet-only (six electrons in three dots) [Sal20]. These different implementations benefit from additional features like facilitated readout, single-qubit rotations, and decoherence-free subspaces.

Second, semiconductor quantum-dots are nanoscale devices capable of trapping and controlling single charges employing electrostatic fields created with metal electrodes. They have a small footprint $\sim (100 \times 100)\,\mathrm{nm}^2$ and benefit from semiconductor nanofabrication techniques developed for integrated circuits. The electron's charge nature allows us to load and displace the qubit in a network of tunnel-coupled QDs while keeping the spin degree of freedom protected from the environment. Local electrometers probe the charges' dynamics in the different QDs. They can be located close to the QDs or directly embedded in the QD network [Elz03; Ibb20].

High-fidelity one- and two-qubit gates have been demonstrated [Sal20; Yon18], along with rapid spin readout using spin-to-charge conversion methods [Urd19; Zhe19]. However, these demonstrations were done in devices with only a few quantum-dots, up to a 3x3 QD array [Mor18]. We are far from the requirements to achieve NISQ or large-scale

quantum computing. So, the next milestones are (i) scaling-up the number of controlled quantum-dots, and (ii) developing a scalable architecture capable of hosting millions of QDs. In this thesis, we study and compare two semiconductor platforms for large-scale QD networks: silicon nanowires and GaAs/AlGaAs heterostructures.

On the one hand, silicon nanowires have the advantage of being produced on industry-standard fabrication lines. Indeed, while the advanced miniaturization of transistors gives rise to quantum effects like tunneling, dooming conventional transistors, it can be exploited to trap and manipulate single electrons. The silicon QD devices are directly integrated into transistor fabrication lines and benefit from all the technologies developed for microelectronics over the past decades. In addition, the nuclear spin noise coming from ^{29}Si nuclei in the silicon crystal can be reduced to negligible levels via isotopic purification to ^{28}Si to enhance the qubit coherence time [Vel15]. However, the electrons' effective mass in bulk silicon $m^*_{Si} = 0.26 m_\mathrm{e}$ is rather large (with m_e the electron rest mass). Therefore, the size of the electron wave function is on the order of $\sim 10\,\mathrm{nm}$, which is similar to state-of-the-art gate patterning resolution [Des12]. It limits the electrostatic control over the quantum-dots' properties and particularly on the coupling between dots. Consequently, only double quantum-dots have been demonstrated so far in foundries' silicon nanowires [Mau16; Urd19]. Moreover, the study of single nanowire devices excludes the use of proximal electrometers, and we must rely on integrated detection schemes.

On the other hand, the GaAs platform relaxes the constraints on gate patterning, thanks to an effective mass three times smaller than in silicon. Quantum-dots are patterned with multiple gate electrodes allowing fine-control of the dots' energies and tunnel-couplings with simple fabrication recipes available in laboratories' cleanrooms [Des12]. Thanks to its ease of implementation, the GaAs platform is a formidable testbed for proof of principles, such as small scale ferromagnetic simulators [Deh20] and coherent qubit shuttling over several micrometers [Jad20]. The main drawback of this platform is the inevitable presence of nuclei-spins in the crystal. So, spin-qubit operations require active manipulation methods to mitigate this magnetic noise and extend the short coherence times of a few tens of nanoseconds [Blu10]. Moreover, this quantum-dots technology is currently restricted to a single QD layer without proposals to connect multiple layers. This could be a limitation towards large-scale implementations.

Thesis outline

The experiments described in this thesis aim at the study of charge control in semiconductor quantum-dot arrays and the prospects towards large-scale integration.

In **Chapter 1**, we introduce the theoretical background for the confinement and control of electrons in semiconductor nanostructure. We detail an electrostatic model for quantum-dots and the physics of the two semiconductor plateforms. Then, we describe the charge detection methods to probe the QD devices along the thesis with either proximal or embedded local electrometers. Finally, we focus on the development of QD networks, from simple double-dots to complex two-dimensional arrays. We develop on the tuning methods to control such devices and conclude on the requirements for a large-scale QD network.

Chapter 2 describes the experimental setup. We start by the cryogenic refrigerator cooling down the devices at $\sim 70\,\mathrm{mK}$. Next, the samples' fabrication methods are presented,

including simulations of the potential landscape induced by the devices' gate electrodes. We detail the electronics with the wiring of the electrical connections, the control and acquisition apparatus, and a radiofrequency setup. To conclude, the measurement software developed in my thesis to control the experiments is presented.

In **Chapter 3**, we explore the charge detection and control of next-neighbor dots in a silicon nanowire. A single-lead quantum-dot electrometer is characterized and the energy spectrum of a single-QD is extracted. Then, we focus on the detection of multi-dots within the nanowire. Different detection schemes are elaborated to compensate for the strong capacitive couplings between the detector and the probed dots due to the device dense packing. We discuss and compare the quantum-dots homogeneity in the few- and many-electron regimes.

Finally, **Chapter 4** describes a scalable 2x2 QD array with shared control gates in a GaAs heterostructure. We start with the isolation of one to five electrons into a single quantum-dot uncoupled to the electron reservoir. We develop a numerical simulation to emulate the charge distribution inside the array as function of the gate voltages. Finally, we demonstrate the control of the charge distribution in the 2x2 QD array, isolated from the reservoir. In particular, we discuss the scalability of the array by extracting the device parameters with the numerical simulations.

CHAPTER 1

Confinement and control of electrons in semiconductor nanostructures

1.1 Introduction

Work on the manipulation of individual electrons in semiconductor nanostructures began in 1988 with the first demonstration of single-electron tunneling [Smi88]. These early quantum-dots (QDs) contained a large and uncertain number of electrons, and it took eight more years to reach the single electron occupation [Tar96]. Shortly afterward, it was proposed to use electron spin as qubits trapped in a network of electrically controlled QDs as a quantum computing unit [Los98].

In this context, we present here a brief state of the art of electron confinement and control in semiconductor QD arrays. We start by examining the basic properties of quantum-dots. A capacitive model of a single quantum-dot is developed, and its properties are described. We highlight the contributions resulting from purely electrostatic effects such as the charging energy, and quantum phenomena created by zero-dimensional confinement of electrons. Then, we describe the properties of the two semiconductor platforms employed in this thesis: a GaAs heterostructure and a silicon nanowire.

On the one hand, the GaAs platform benefits from simple electronic properties with a single conduction band valley and a small effective mass. Consequently, GaAs devices can be fabricated in research facilities with limited lithographic constraints. However, all the atoms in the crystal carry a non-zero nuclear spin, limiting electron-spin qubits' coherence time to a few nanoseconds. On the other hand, the silicon platform can eliminate nuclear spins through an isotopically purified ^{28}Si substrate, achieving milliseconds of coherence time. Furthermore, the fabrication of the silicon quantum devices is compatible with CMOS industry-standard fabrication lines, which paths the way towards large-scale integration of QD arrays. Despite these attractive properties, the silicon platform raises some challenges such as a large electron effective mass and multiple conduction band valleys, as we will discuss in the following.

Next, we explain the techniques applied to perform remote charge sensing of the quantum-dot charge dynamics. Remote electrometers have the advantage of being a non-invasive method compared to direct transport measurements in the system to probe. We detail how the unique characteristics of quantum dot contact and single-electron transistors can serve as sensitive electrometers. We continue by explaining the gate rf-reflectometry charge sensing. This technique has the benefit of reducing the number of electron reservoirs to one or zero, and several electrometers can be packed together by multiplexed measurements.

Finally, we study the formation of quantum-dot arrays, starting with a simple double quantum-dot structure. Then, linear and two-dimensional QD arrays are explored, and

their tunability is discussed. Moreover, we present the isolated regime as a solution to the device operations' complexity while increasing the number of QDs under control. In the end, the requirements for quantum computing using large-scale two-dimensional quantum-dot arrays are given.

1.2 Basics of quantum-dots

A quantum-dot is a three-dimensional confinement potential that can trap charged particles like electrons or holes. The confinement potential size is designed to be of the same order of magnitude as the Fermi wavelength of the trapped objects. Therefore, the charges cannot be considered as purely classical particles but have to be treated as quantum objects. The quantum-dots are referred to as artificial atoms since they exhibit bound and discrete electronic states similar to naturally occurring atoms or molecules.

Due to this simple definition, it exists a complete zoology of quantum-dot systems such as self-assembled quantum-dots [Kle96], single molecules trapped between electrodes [Urd11], carbon nanotubes [Dek99], and finally vertically [Kou01] or laterally [Kou97] defined quantum-dots.

In this thesis, we are interested in laterally defined quantum-dots realized either in a GaAs/AlGaAs heterostructure or a silicon nanowire. With both platforms, we apply voltages on metallic gates to electrostatically define the dot shapes and positions. In this section, we first discuss the basic properties of quantum-dots by using an electrostatic model. Then, we examine how is created the three-dimensional confinement and the specific contributions in the energy spectrum for each platform.

1.2.1 Constant interaction model

In this section, we develop a simple model for a quantum-dot embedded into an electrical circuit, as pictured in Fig. 1.1(a). We use the constant interaction model [Kou97] to describe the quantum-dot QD1 coupled via tunnel barriers to two reservoirs, source (voltage V_{S}) and drain (V_{D}), and capacitively coupled to a gate electrode (V_{G}). The tunnel-barriers are treated as leaking capacitors between two nodes and parametrized by a capacitor in parallel to a resistor, the later giving the tunnel-rate from one node to the other.

Model description

In this model, we assume that the Coulomb interactions among electrons in the dot, and between electrons in the dot and the environnement, can be parametrized by a unique capacitance C_1. This capacitance must be constant and is the sum of all the capacitances between the dot and its environnement : $C_1 = C_{\mathrm{S1}} + C_{\mathrm{D1}} + C_{\mathrm{G1}}$ with C_{S1} the source-QD1 capacitance, C_{D1} the drain-dot, and C_{G1} the gate-dot. Then, the total amount of charges in QD1, Q_1, is the sum of all the charges induces by the different nodes connected to the dot

$$Q_1 = C_{\mathrm{S1}}\left(V_1 - V_{\mathrm{S}}\right) + C_{\mathrm{D1}}\left(V_1 - V_{\mathrm{D}}\right) + C_{\mathrm{G1}}\left(V_1 - V_{\mathrm{G}}\right) \tag{1.1}$$

Using this equation, we compute the electrostatic energy of QD1 as a function of the number N of electrons in the dot as $U_{\mathrm{C}} = \frac{1}{2}C_1 V_1^2$. By introducing $Q_1 = -|e|\left(N - N_0\right)$ with $-|e|$ the electron charge and $N_0|e|$ the dot charges compensating the background

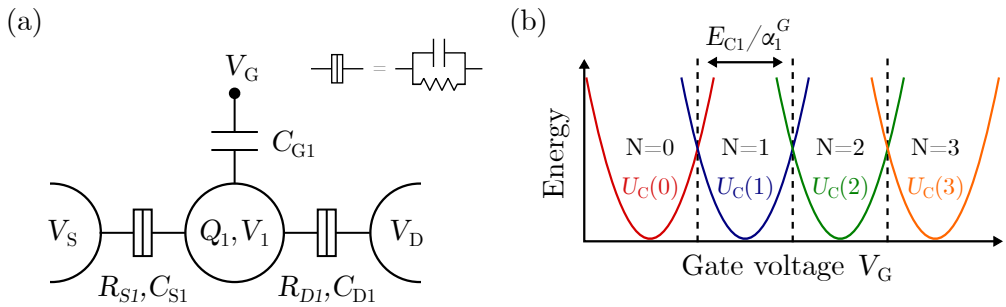

Figure 1.1: Quantum-dot in the constant interaction model. (a) Schematic of a quantum-dot embedded into an electrical circuit in the constant interaction model. The quantum-dot QD1 has a potential V_1 and contains Q_1 charges. It is capacitively coupled to a gate electrode V_G through a capacitor C_{G1}. Electrons can be exchanged with the source and drain reservoirs through tunnel barriers represented by a capacitor parallel to a resistor. **(b)** Electrostatic energy of QD1 for $N = 0 \to 1$ as a function of the gate voltage V_G. The quantum-dot ground-state occupation increases by step as the value of V_G is swept.

charges from the donors in the quantum-dots' structure, we obtain

$$U_C(N) = \frac{1}{2C_1}\left[-|e|\,(N - N_0) + C_{S1}V_S + C_{D1}V_D + C_{G1}V_G\right]^2. \tag{1.2}$$

The electrostatic potential of QD1 can be changed continuously through the different gate voltage contributions with the format $C_{i1}V_i$, for $i = \{S,D,G\}$. Consequently, the dot occupation N can be controlled by applying a gate potential as pictured in Fig. 1.1(b) where electrons are loaded into the dot from the reservoirs by increasing the gate voltage V_G. Of course, it is true only if the system stays in the ground-state during the operations.

In addition to this purely classical energy contribution, we can add the single-particle energy-level spectrum to take into account contributions like the quantum effects of the confinement potential. Considering the energy of all the occupied single-particle energy levels E_n, the total energy of the system is

$$U(N) = U_C(N) + \sum_{n=1}^{N} E_n. \tag{1.3}$$

Then, we define the electrochemical potential $\mu(N)$ of QD1 as the change of total energy between the states with N and $N-1$ electrons :

$$\begin{aligned}\mu(N) &\stackrel{\text{def}}{=} U(N) - U(N-1)\\ &= \left(N - N_0 - \frac{1}{2}\right)E_{C1} - \frac{E_{C1}}{|e|}\left(C_{S1}V_S + C_{D1}V_D + C_{G1}V_G\right) + E_N,\end{aligned} \tag{1.4}$$

where we have introduced the charging energy $E_{C1} = e^2/C_1$. This energy corresponds to the purely electrostatic energy cost of adding one electron into QD1. We remark that the electrochemical potential has a linear dependence on the gate voltages, while the energy

depends quadratically on the gate potentials. So, the electrochemical potentials of the different occupation numbers are moved altogether by preserving the level spacing when a gate voltage is swept. We use this property to discuss electron transport through the system in Sec. 1.3.1.

Finally, we define the addition energy E_{add} as the difference in electrochemical potential between two successive charge states :

$$E_{\mathrm{add}}(N) = \mu(N+1) - \mu(N) = E_{\mathrm{C1}} + (E_{N+1} - E_N)\,. \tag{1.5}$$

The addition energy is also split in two terms with on the one hand the charging energy, and on the other hand the energy spacing between two discrete quantum levels that takes into account the confinement potential and the properties of the substrate.

Gate lever-arms

In general, the second term of Eq. 1.4 is rewritten as $\alpha_1^{\mathrm{S}} V_{\mathrm{S}} + \alpha_1^{\mathrm{D}} V_{\mathrm{D}} + \alpha_1^{\mathrm{G}} V_{\mathrm{G}}$, where we have introduced the lever-arm of gate K on dot i :

$$\alpha_{\mathrm{i}}^{\mathrm{K}} = e\frac{C_{\mathrm{Ki}}}{C_{\mathrm{i}}}. \tag{1.6}$$

This so-called alpha-factor translates the effect of a gate voltage into the physical energy of a dot. As we will discuss in the following sections, the gate lever-arms vary extremely within a quantum-dot system and from one system to another. Thus, this quantity is critical to extract physical parameters of the system from experimental data, as the charging energy in Fig. 1.1(b).

However, measuring the different capacitances is challenging. It is preferred to calibrate the gate voltage effects with respect to a reference energy scale. Different energy references are available as the bias window $V_{\mathrm{S}} - V_{\mathrm{D}}$ by performing a Coulomb diamond experiment [Kou01], photon assisted tunneling with an RF excitation at a known frequency [Oos98], or a magnetic field sweep in a spin-funnel experiment [Pet05].

To conclude, we have defined a basic model to understand quantum-dots properties. In particular, the constant interaction model allows us to deal with the classic electrostatic of a charged island, with the addition of quantum contributions like the orbital spacing originating from the trapping potential. In the next sections, two different quantum-dot platforms are detailed, and we explicit each contribution to the addition energy spectrum.

1.2.2 Gallium-Arsenide heterostructure

The first platform used in this thesis is laterally defined quantum-dots in a Gallium-Arsenide heterostructure. It is an ideal testbed for quantum-dot structures and has been home to the pioneer experiments demonstrating coherent control of individual electrons [Kop06; Pet05]. The dots are defined by applying negative voltages on metallic gates on the sample surface to pattern a two-dimensional gas (2DEG) located underneath, allowing a good control over the different quantum-dot parameters.

Here, we describe how to produce the 2DEG and how quantum-dots are formed. Finally, we detail the energy spectrum of a characteristic GaAs quantum-dot by highlighting the

different contributions to the addition energy.

Two-dimensional electron gas

A heterojunction is an interface between two semiconductors with a different band-gap. By band-gap engineering, the heterostructure can be designed to satisfy various applications like solar cells [And99], lasers [Alf02], and high mobility transistors (HEMTs) [Mim02]. Here, a GaAs/AlGaAs heterostructure is combined with a silicon modulation doping to form a quantum well 110 nm below the surface, in which electrons are trapped (see Fig. 1.2(a)). The confinement along the growth axis is typically about 16 meV $\sim$ 186 K [Ste84]. So, at dilution temperature, the motion of the electrons is quantized in this direction with only the ground state occupied, and the system is considered a two-dimensional electron gas.

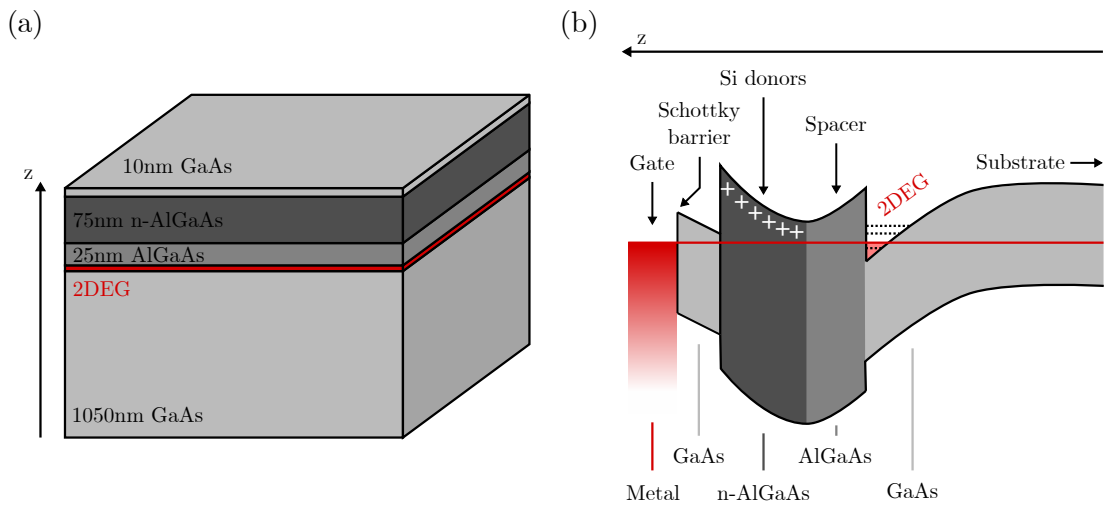

Figure 1.2: Gallium-Arsenide heterostructure and two-dimensional electron gas. **(a)** Schematic of the GaAs/AlGaAs heterostructure with the material composition and the thickness specified for each layer. **(b)** Band structure along the growth direction. The 2DEG is located 110 nm below the surface, at the GaAs/AlGaAs interface. The GaAs/AlGaAs layer is split into two parts. The first part is silicon-doped to bend the bands, create the 2DEG confinement, and provide electrons for the 2DEG. A second part acts as a spacer to spatially separate the high-mobility 2DEG from the doping layer. On top of the sample surface, an unwanted Schottky barrier is formed if a metallic gate is deposited.

The fabrication of these heterostructure relies on molecular beam epitaxy (MBE). MBE is a fundamental tool of the nanotechnologies where structures are grown epitaxially one atomic layer at a time. It results in great control over the layer composition and atomically flat interfaces. Thus, it is possible to spatially separates the doping layer (required to form the 2DEG) from the actual 2DEG, as pictured in Fig. 1.2(b). Putting these ionized impurities far from the electron gas results in better electronic properties, with less scattering and less potential irregularities. Consequently, the electron mobility of 2DEGs defined by MBE is typically three orders of magnitude greater than grown oxide interfaces like Si/SiO_2[Li13; Uma09].

The group of Andreas Wieck from the Ruhr-University (Germany) made the heterostruc-

tures used in this thesis . In the context of this collaboration, we have received 2 inch wafers split among the different projects in the group. These crystals hold a 2-dimensional electron gas 110 nm below the wafer surface with a mobility $\mu_e = 1.5 \times 10^6\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ and an electron density $n_e = 2.6 \times 10^{15}\,\mathrm{m}^{-2}$. To demonstrate the 2DEG quality, we compute the mean free path of an electron within the gas as

$$l_\mathrm{e} = v_\mathrm{F}\tau_\mathrm{e} = \sqrt{2\pi n_\mathrm{e}}\frac{\hbar\mu_\mathrm{e}}{e} \simeq 13\,\mu\mathrm{m} \tag{1.7}$$

using the parabolic band approximation, with v_F the electrons speed at the Fermi energy and τ_e the momentum relaxation time. This large mean free path means that defect-less structures can be patterned with nanofabrication techniques, as we will discuss now.

Lateral confinement

We have seen that the heterostructure gives rise to strong confinement along the growth direction and defines a high mobility two-dimensional electron gas. To perform the confinement along the two remaining dimensions, we deposit metallic gates on the heterostructure's surface. Applying a negative voltage on a gate modulates the charge density of the electron gas underneath. Thus, the gate geometry is critical to pattern the 2DEG in constrictions and quantum-dots, as pictured in Fig. 1.3. In particular, multi-dot systems can be imprinted with voltage-controlled inter-dot tunnel barriers. Moreover, the characteristic gate-dot lever-arm in this type of structure is on the order of 50 meV/V [Mar14].

Based on the 2DEG properties, we can compute the characteristic confinement potential length at which quantum-dots are formed with the Fermi wavelength :

$$\lambda_\mathrm{F} = \sqrt{\frac{2\pi}{n_\mathrm{e}}} \simeq 49\,\mathrm{nm}. \tag{1.8}$$

This is compatible with the typical resolution of electron-beam lithography, around 20 nm, mainly limited by the lift-off process. Thus, nanofabrication techniques can be used to imprint quantum-dots structures into the 2DEG.

However, the metallic gates deposited directly on top of the GaAs cap exhibit a Schottky behavior that limits the voltage range applicable without current leakage to $[-3\,\mathrm{V}, 0.1\,\mathrm{V}]$. Nevertheless, in Section 2.3.1, we develop a structure with two superimposed metallic layers. So, an insulating layer in-between the metallic patterns is required to avoid contacts and currents between each gate. We chose to benefit from this technology to prevent the formation of Schottky barriers and add an additional insulating layer between the first metallic layer and the substrate. Consequently, a wider voltage range can be applied to tune the device, from $-7\,\mathrm{V}$ to $7\,\mathrm{V}$ without any leakage current.

Energy spectrum

As discussed in Sec. 1.2.1, a quantum-dot's energy spectrum can be split between two contributions.

First, a purely electrostatic part is summarized by the charging energy E_C. To estimate this quantity, we approximate the dot as a charged disk of diameter $D = 100\,\mathrm{nm}$ and

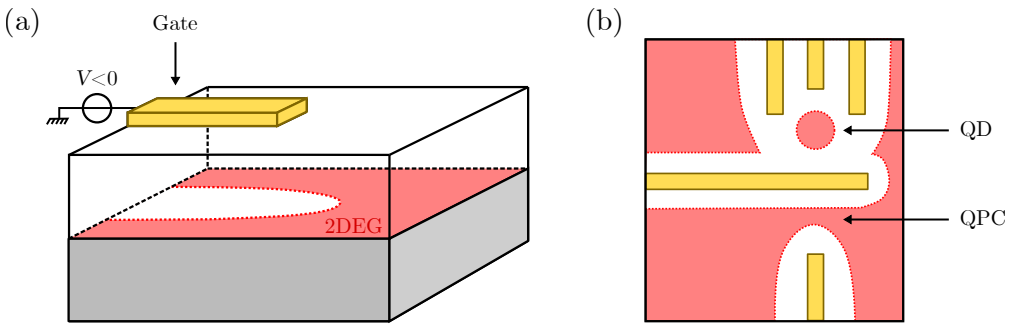

Figure 1.3: 2DEG patterns controlled by voltage gates. (a) Schematic of the electrostatic effect on the 2DEG of a metallic gate deposited on the surface of the sample. Applying a negative voltage on the gate depletes the electrons underneath. **(b)** Schematic top view of the sample. By engineering the geometry of the gates, the 2DEG can be patterned into arbitrary shapes. A quantum-point contact is formed on the lower side and a quantum-dot on the upper side.

consider only its self-capacitance :

$$C_{\text{self}} = 4\varepsilon_0\varepsilon_{\text{r}}D \simeq 46\,\text{aF}, \tag{1.9}$$

with ε_0 the vacuum permittivity and ε_r the relative permittivity of the heterostructure [Kou91]. This capacitance is an upper-bound of the total capacitance since we neglect the surrounding gates and 2DEGs existence . Nevertheless, it gives a charging energy $E_{\text{C}} = e^2/C_{\text{self}} \simeq 3.5\,\text{meV}$.

This charging energy must then be compared with the second contribution in the addition energy, which is the single-particle energy level E_{N}. Since the electrons are confined in the 2DEG within a region comparable to the Fermi wavelength, their motion is quantized into discrete orbitals and form an artificial atom. In particular, electrons are spin-$\frac{1}{2}$ particles and must respect the Pauli principle. Two electrons can occupy the same orbital only if they possess a different spin orientation. For a 2D harmonic potential of characteristic size D, the energy spacing E_{O} between two orbitals is given in [Kou97] as

$$E_n = E_{\text{O}} = \frac{\pi\hbar^2}{m^* D^2} \simeq 0.4\,\text{meV}, \tag{1.10}$$

with $m^* = 0.067m_0$ the electron effective mass in the system, and accounting for the spin degeneracy without magnetic field.

We remark that the charging energy is the dominant term in the quantum-dot addition energy E_{add}. So, the chemical potential of the quantum-dots is mostly determined by the classical Coulomb repulsion. Finally, these different energy scales are several orders of magnitude smaller than the base temperature of a dilution refrigerator $T = 70\,\text{mK} \approx 6\,\mu\text{eV}$. Consequently, we can resolve and control the electronic quantum states of GaAs quantum-dots, as we will discuss in Part 4.

1.2.3 Silicon nanowire

The second quantum-dot platform explored in this thesis relies on silicon nanowires. In the last fifty years, the development of silicon nanostructures has been tightly linked with microelectronics' exponential progress. In particular, intense efforts have been devoted to reducing the size of metal-oxide-semiconductor field-effect transistors (MOSFETs) with a yearly increase in the number of transistors per chip given by the Moore's Law [Moo75]. Moreover, it has been estimated that a total of 13 sextillion $\left(1.3 \times 10^{22}\right)$ MOSFETs have been produced worldwide between 1960 and 2018, making the transistors the most widely manufactured device in humankind history [Law18].

At the same time, silicon has been revealed as an excellent host material for quantum applications relying on charge and spin degree of freedom. For example, bulk silicon has a weak spin-orbit coupling and can be cleared of nuclear spins by ^{28}Si-isotope purification [Tyr11], which favors long coherence time for electron-spin qubits.

Thus, the prospect of combining the advanced nanofabrication technologies already available with its quantum properties make silicon a promising candidate for large scale semiconductor quantum-bit array. Furthermore, the fabrication of quantum devices on industry-standard fabrication lines permits co-integrating quantum functionalities within classical logic-circuits [Bot19; Vin18a].

In this section, we detail how a MOSFET can be used at cryogenic temperatures to host quantum-dots and highlight the host material's specificities compared to GaAs QDs.

Corner states

The devices used in this thesis are nanowire CMOS transistors, as shown in Fig. 1.4. An undoped silicon channel with a rectangular cross-section is chemically etched. The nanowire is connected at both ends with source and drain metallic contacts and is covered with gate electrodes to modulate the electron density within the channel.

Gate efficiency is optimized by adopting a so-called tri-gate geometry where the electrodes cover all but the nanowire bottom facet (see Fig. 1.4(b)) [Voi14a]. These devices differ from the traditional MOSFET in the number and the geometry of the gate electrodes. While a typical MOSFET has a single electrode wrapping the intrinsic nanowire, here we explore different gate geometries. For example, multiple gates can be added in series along the nanowire, and gates can be split in two perpendicularly to the nanowire axis to independently control each side of the nanowire electron density, as in Fig. 1.4(a). In addition, large spacers are implemented to protect the silicon nanowire from unwanted doping and have a reservoir-dot tunnel barrier opaque enough to form quantum-dots.

Nevertheless, applying electrode voltages above a so-called threshold voltage turns on the MOSFET at room temperature and a current flows between the source and drain reservoirs as expected. The current-voltage characteristics of our CMOS transistors are available in Appendix A, and will be discussed in Sec. 2.3.2.

However, the way conduction gets activated is not straightforward. In Sellier *et al.* [Sel06], the study of a similar MOSFET's conductance at cryogenic temperature shows that conduction channels start at the two upper edges of the silicon nanowire for sub-threshold voltages. This effect is due to the focusing of the gate field lines in the corners of the nanowire. These results are supported by numerical simulations, from [Voi14b], of the

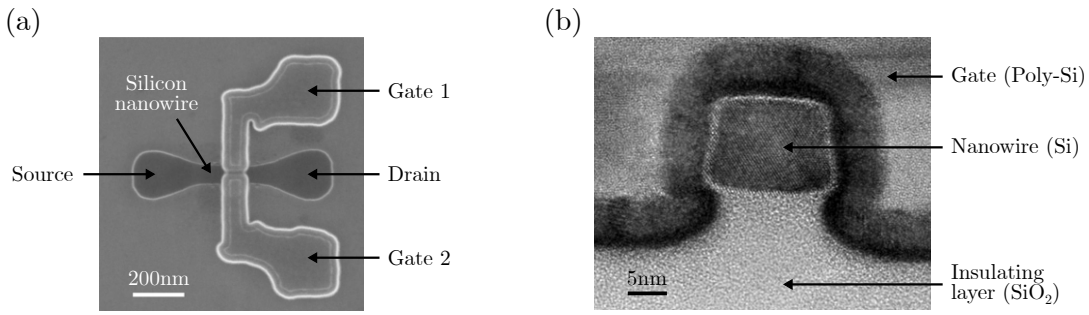

Figure 1.4: Nanowire CMOS transistor for quantum electronics.
(a) Electron-microscope top-view of a nanowire CMOS transistor. An intrinsic silicon nanowire is etched on top of a thick buried-oxide layer (BOX). Source and drain contacts act like electron reservoirs. Applying a voltage on the pair of split-gates deposited on top of the nanowire modulates the electron's density inside the nanowire. **(b)** TEM cross-view of a similar device along the electrode, perpendicular to the silicon nanowire. The intrinsic nanowire at the center of the picture is deposited on an insulating layer and is wrapped by a gate to maximize its effect.

carrier concentration inside the nanowire for gate voltages with one electron trapped into the nanowire (see Fig. 1.5(a) and (b)). The electron density indicates the formation of symmetric localized one-dimensional conduction modes parallel to the channel axis in the nanowire's corners.

Yet, this simulation deals with an ideal MOSFET and does not take into account disorder. Adding roughness at the nanowire surface and remote charges trapped into the gate dielectric break the one-dimensional mode along the nanowire and the symmetry between both edges.

Consequently, we see in Fig. 1.5(b) that $\sim 10\,\mathrm{nm}$ small quantum-dots are formed in the corners of the nanowire. We label corner-dots these potential wells along the top edges of the silicon channel. While the first electron occupies the quantum-dot with the lowest energy, the following charges will not necessarily be added to the same quantum-dot. It is expected that for a large number of electrons trapped in these corner-dots, their sizes increase, and the potential landscape is smoothed by screening. So, the different quantum-dots merge to form a unique corner-dot for each side of the nanowire.

Moreover, the random distribution of remote charges and the unique surface roughness at each edges of the nanowire break the symmetry between the corner-dots. For two neighbor corner-dots on each side of the nanowire, each edge's electron filling will be different. Thus, the split-gate geometry controls more independently each side of the silicon channel.

Finally, the reservoir-dot and the inter-dots tunnel barriers are predominantly fixed by the spacer sizes and the gate separations. However, the corner-dots' position is tunable by applying a voltage directly on the back surface of the device [Fra16], or with a global top-gate deposited above the electrodes [Ans20]. It has been reported that the inter-dot tunnel coupling between corner-dots on each side of the nanowire could be tuned over three order of magnitudes using a global top-gate [Ans20].

To summarize, the formation of quantum-dots in the silicon nanowire is given by (i) a

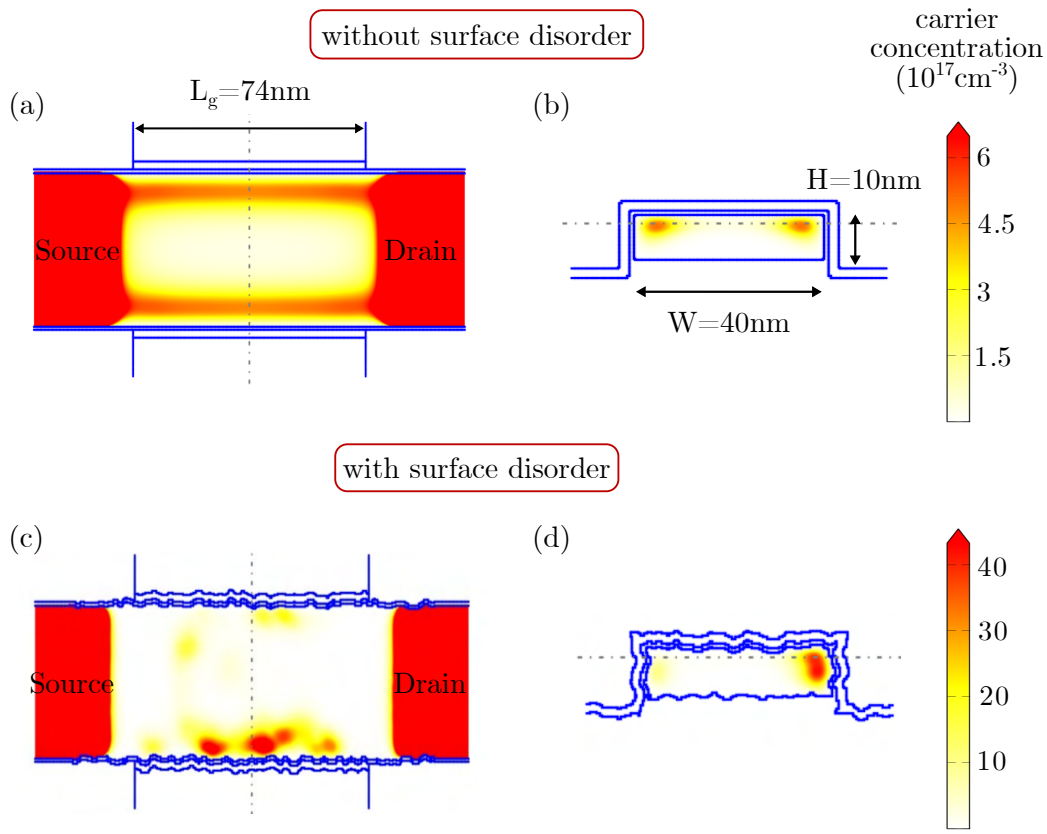

Figure 1.5: Electron density in the silicon nanowire. Simulation of the carrier concentration in a nanowire CMOS transistor from [Voi13]. The carrier concentration is computed for a temperature $T = 77\,\mathrm{K}$ and normalized so the total carrier concentration is equal to one electron in the nanowire. The top panel corresponds to a simulation without any disorder, while the bottom panel takes into account remote charge traps and surface disorder. For both panels, the left figure is a top view of the horizontal silicon nanowire, and the right one is a cross-section along the dashed axis. **(a and b)** Nondisordered case. The accumulation begins in two extended symmetric channels in the corners of the nanowire. **(c and d)** With disorder. The presence of remote charge traps and the surface roughness produce a confinement potential for the electrons in the edge states and form quantum-dots.

two-dimensional confinement rising from the accumulation of a 2DEG in the corner of the nanowire by applying a gate positive voltage and (ii) an additional localization coming from both remote positive charges and surface roughness at the nanowire/gate interface. The different tunnel barriers in the system are mostly fixed by the device geometry but can be tuned to some extent using global top or back gates.

Charging energy and orbital spacing

We can now consider the energy properties of the silicon nanowire corner-dots.

First, a consequence of the compact CMOS nanowire geometry is the direct proximity between the gate electrode and the controlled quantum-dot. Thus, these devices have large

lever-arms compare to GaAs heterostructure where the 2DEG is located 100 nm below the surface. In the case of corner dots in a split-gate geometry, typical lever-arms of 0.4 eV/V are obtained [Ans20; Bet15; Ibb20]. These important lever-arms greatly enhances the charge sensing fidelity of gate RF-reflectometry, as discussed in Sec. 1.3.2.

Concerning the corner-dots energy spectrum, it has been measured experimentally that these dots have a charging energy $E_{\mathrm{C}} \simeq$ a few tens of milli-electron-volts [Bet15; Ibb18; Voi14b], in the few-electron regime. As discussed previously, we expect the charging energy to reduce as the number of trapped electrons increases, since the strong localization induced by disorder will be progressively screened and smoothed. This significant charging energy is due to the large electron effective-mass in silicon, three times larger than in the GaAs devices. Consequently, the electronic wavefunctions are smaller and more sensitive to the crystal disorder, as discussed previously. Finally, by taking into account the small corner-dot size in Eq. 1.10, we estimate an energy spacing between two orbitals within the same quantum-dot $E_{\mathrm{O}} \simeq 1.5\,\mathrm{meV}$, as reported with spectroscopy measurements in [Voi14b]. So, the charging energy is also dominant over the orbital spacing in the dot energy spectrum for silicon QDs.

However, in addition to the orbital levels, the crystalline silicon structure gives rise to multiple conduction band valleys that must be considered to understand the corner dots' energy spectrum, as we will discuss now.

Valley physics

Crystallized silicon is a diamond lattice formed by covalent bonds. It is a well-studied semiconductor with an indirect band-gap. Indeed, electron state energies in the conduction band are minimized for a non-null value of the crystal momentum $\vec{k}$. Furthermore, this minimum is 6-fold degenerated due to the bulk silicon cubic symmetry and forms 6 different valleys. The valley-degeneracy is not a problem for regular electronic devices since it does not affect strongly their transport properties, but it is detrimental for quantum electronics due to interferences between valleys during quantum coherent manipulations. The degeneracy must be lifted, so the electrons occupy only the lowest-energy valley states, similar to the orbits.

In our silicon nanowire, the confinement in the nanowire and the interfaces reduce the crystal's symmetries and lift the 6-fold degeneracy. First, the electron effective-mass is anisotropic and consequently the stronger confinement along the z-axis moves the four $\vec{k_x}$ and $\vec{k_y}$ valleys approximately 10 meV above the two $\vec{k_z}$ valleys (see Fig. 1.6) [Bou18]. Then, the two remaining $\vec{k_z}$ valleys can be coupled by inter-valley scattering potentials [Sar11; Sar09]. Potentials that vary rapidly along the z-axis at the scale of few nanometers will lift the remaining degeneracy by forming bonding and anti-bonding combinations of the $+\vec{k_z}$ and the $-\vec{k_z}$ valley states. We call valley splitting E_{V} the energy splitting between these two states.

For our CMOS devices, the interface between the silicon nanowire and the gates' dielectric acts like an abrupt change in the potential. Characteristic values for the valley splitting range from $E_{\mathrm{V}} \simeq 10\,\mu\mathrm{eV}$ to $1\,\mathrm{meV}$ depending on the interface surfaces of the device. Nevertheless, the valley splitting can be tuned experimentally by controlling how much the quantum-dot is squeezed to the gate electrode interface. In [Ibb18], applying a negative

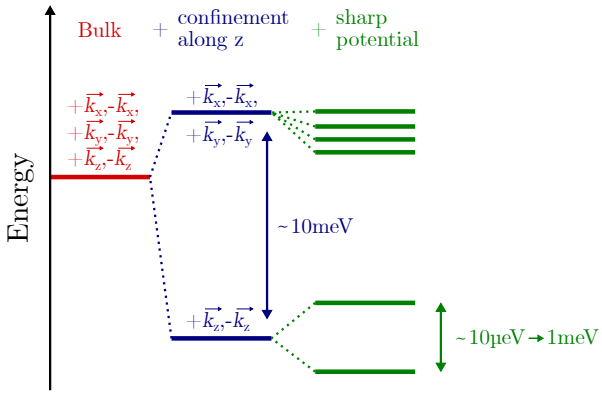

Figure 1.6: Valley splitting in silicon corner-dots. Schematic of how the 6-fold valleys degeneracy is lifted in silicon corner-dots. Starting from bulk silicon, the system symmetry is broken by the confinement potential in the corner of the nanowire. The two $\overrightarrow{k_z}$ valleys stay degenerate $\sim 10\,\mathrm{meV}$ below the four remaining valleys. The presence of a sharp potential at the nanowire-dielectric interface couples the two valleys, and gives a valley splitting which value depends on the interface details.

voltage on the back-gate continuously increases the valley splitting up to a factor two. To summarize, we have seen that silicon's 6-fold valleys degeneracy can be completely lifted inside the CMOS devices.

To understand the corner-dot's addition energy spectrum, we need to compare the valley splitting to the other contributions. Since the dot charging energy remains the dominant energy, the valley splitting must be weighed against the orbital spacing E_O.

If the orbital level spacing is much smaller than the valley splitting ($E_\mathrm{O} \ll E_\mathrm{V}$), electrons start by occupying well defined single-particle levels with increasing orbital numbers inside a unique valley. In this case, we get rid of the valley physics in the few-electron regime. Reciprocally, if $E_\mathrm{O} \gg E_\mathrm{V}$, the first electrons fill the different valleys, each time in the lowest orbit. Finally, if $E_\mathrm{O} \simeq E_\mathrm{V}$, orbits and valleys hybridize [Fri10]. Due to this mixing, it is no more appropriate to talk about defined valley or orbital quantum numbers. The new eigenstates are called valley-orbit levels, and their spacing is not necessarily regular.

For the devices studied here, the valley splitting is expected to be smaller than the orbital spacing. Nonetheless, valley splitting, then valley-orbit coupling, depends a lot on interface details. Thus, E_V is device-dependent, and it is nontrivial to predict the structure of our artificial atoms. We discuss the measured addition energy spectrum of four different devices in Part 3.

1.2.4 Conclusion

In this first section, we have discussed the basics of semiconductor quantum-dots. We have started by detailing the constant interaction model. This simple model described how we could operate quantum-dots by considering the devices as nodes capacitively coupled. We have defined the quantum-dot charging energy E_C that considers the electrostatic cost of adding an electron to a dot. Moreover, the lever-arm factors α are introduced to translate the operator voltage knobs into the system's relevant energy scales.

Then, we have presented the two semiconductor quantum-dots platform used in this thesis. The first platform is a GaAs/AlGaAs heterostructure with metallic gates at the sample surface used to locally deplete a 2DEG located 100 nm underneath. We have used two-dimensional models to predict such quantum-dots' addition energy spectrum, showing that the charge energy is dominant over the orbital spacing. The second platform relies on nanowire CMOS transistors. Corner-dots are accumulated at the top edges of the nanowire by using both the electrostatic confinement generated by the gate electrodes and the strong localization induced by remote charge traps and the nanowire/dielectric surface roughness. We have highlighted the additional contributions in the energy spectrum coming from the valley physics in the silicon nano-crystal.

In the next section, we use this knowledge to discuss how to probe quantum-dots' charge dynamics.

1.3 Remote charge sensing

In this thesis, we aim to characterize the charge distributions and dynamics inside quantum-dot arrays. This task implies to detect individual charges as small as 1.6×10^{-19} C inside semiconductor structures.

A basic approach consists of performing transport measurements through the quantum-dot device. In 1988, Smith *et al.* have performed the first realization of a single quantum-dot sensing with transport measurements, in the many-electron regime, with a GaAs heterostructure [Smi88]. However, this technique requires large coupling to the reservoirs to generate a measurable current, which is particularly difficult to sustain in the few-electron regime with laterally defined quantum-dots as the reservoir-dot coupling tends to decrease with the dot size. In consequence, it took another 12 years from the first quantum-dot sensing to detect single-electron occupation with transport measurements, by engineering the gate electrodes [Cio00; Wau95]. Transport measurements have also been used to probe double quantum-dots structures, with the additional requirement of a large tunnel-coupling between the two dots [Wie02]. Moreover, transport measurements are limited to structures in which current can flow.

For our work, we rely exclusively on so-called remote charge sensing where a local electrometer is defined close, or within the probed structures. Thus, the electrometer can be arbitrary independent from the quantum-dot tuning and detect the probed system charge dynamics even for low tunnel couplings. Compared with transport measurements, the remote charge sensing is non-invasive and will affect only marginally the probed system's charge and spin dynamics. In this section, we detail the two different techniques to probe quantum-dot arrays. First, we describe how transport measurements can be used to perform remote charge sensing. We highlight the transport features of quantum point contacts (QPC), a narrow constriction in a 2DEG. Then, we use the constant-interaction model developed in Sec. 1.2.1 to understand the transport properties of a quantum-dot and build a single-electron transistor (SET) electrometer operated in the many-electron regime. Finally, we develop a model for gate-based dispersive RF-reflectometry. This method embeds a quantum-dot electrode in an LC-resonant circuit to probe the so-called quantum capacitance between the gate and the dot. Gate reflectometry has several advantages over

transport measurements in the context of large-scale quantum-dot arrays. For example, it dramatically reduces the sensors' footprint by removing the need for one or all reservoirs in the detection protocol.

1.3.1 Transport measurements

Quantum point contact

Quantum point contacts are local constrictions of a 2DEG so that the electrons flow though a one-dimensional channel [Hou05]. If the channel width is comparable to the electron Fermi wavelength, then the confinement induces quantization of ballistic conductance.

In Figure 1.7(a), a QPC is realized in a GaAs heterostructure using two metallic gates. The IV-characteristic of the QPC shows that for $V_{\mathrm{QPC}} < -550\,\mathrm{mV}$, the channel is completely pinched, and no current flows through the system. When the gate voltage increases, the conduction jumps abruptly and stays constants until the next plateau is reached. Here, the conductance through the QPC is quantized in integer values of $2e^2/h$, the conductance quantum taking into account the electron spin degeneracy.

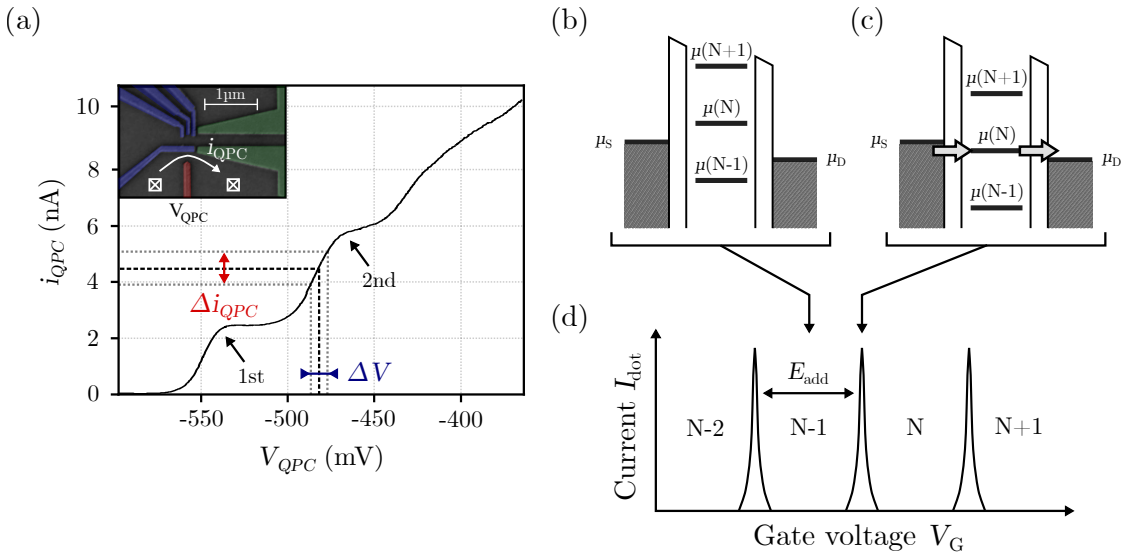

Figure 1.7: Quantum point contact and single electron transistor.
(a) Reproduced from [Ber15a]. QPC IV-characteristic measured for a bias of 30 µV. When the QPC voltage $V_{\mathrm{QPC}} < -550\,\mathrm{mV}$, the channel is completely pinched and no current i_{QPC} is measured. When the QPC voltage is increased, we observe two conductance plateaus. By polarizing the QPC at a transition, any change ΔV in the QPC electrostatic environment will produce a change of current Δi_{QPC}. (inset) SEM micrograph of the sample.
(b, c and d) Schematics of SET transport properties. (b) and (c): diagrams of the discrete electrochemical potential levels compare to the source and drain reservoirs. (b) No level falls into the bias window ($\mu_{\mathrm{S}} - \mu_{\mathrm{D}}$). Thus, the dot occupancy is fixed at $N-1$, and no transport is possible due to the Coulomb blockade. (c) The $\mu(N)$ level fits into the bias window, and the electrons tunnel one by one from source to drain at a timescale fixed by the tunnel barriers. (d) Current I_{dot} through the device as a function of the gate voltage V_{G}.

A QPC can be used to perform remote sensing by designing the electrometer close to the probed quantum-dot structures. Then, the QPC is polarized between two conduction

plateaus, where the derivative of the QPC current with respect to any voltage variation is the largest. At these spots, small changes in the electrostatic environment produce a large current response. We remark that it is preferred to work with the first conductance plateau since additional conduction channels will screen the electrostatic effect that we want to probe. Thus, the addition of a single electron into the quantum-dot can be detected. The sensitivity of the QPC electrometer depends (i) on its capacitive coupling to the quantum-dot, and (ii) to the device electronic temperature. Indeed, the Coulomb potential of the electron trapped in the quantum-dot diminishes with the distance $\propto 1/r$, so the QPC must be positioned as close as possible to the quantum-dot. In addition, the width of each step in the QPC characteristic is inversely proportional to the temperature [Wee88]. So, the electrometer sensitivity increases when the device temperature decreases.

Such detection schemes are routinely used to probe single-charge displacement inside quantum-dot systems [Elz03]. In the next section, we introduce the single-electron transistor, a more complex alternative enhancing the electrometer sensitivity furthermore.

Single electron transistor

A single-electron transistor is the most basic quantum-dot structure. It consists of a single quantum-dot connected to source and drain metallic reservoirs, and a control gate electrode as pictured in Fig. 1.1(a). Here, we explore the transport characteristics of this structure when the charging energy E_{C} is dominating the addition energy spectrum and with a device temperature $k_{\mathrm{B}}T \ll E_{\mathrm{C}}$.

For electrical transport to occur through the system, we need to align one of the available quantum levels within a bias window. The bias window is the difference in electrochemical potential between the source and the drain reservoirs and is tuned by applying a bias voltage $V_{\mathrm{SD}} = V_{\mathrm{S}} - V_{\mathrm{D}}$ so that $\mu_{\mathrm{S}} - \mu_{\mathrm{D}} = -|e|V_{\mathrm{SD}}$. To meet the transport condition $\mu_{\mathrm{S}} \geq \mu(N) \geq \mu_{\mathrm{D}}$, one can adjust the local gate electrode value V_{G} to shift the whole electrochemical ladder as pictured in Fig. 1.7(b) and (c).

To have a better understanding of the transport phenomenon, we schematize the measured current through the device when the gate voltage is swept (Fig. 1.7(d)). If none of the QD levels sit within the bias window as depicted in Fig. 1.7(a), the number of electrons inside the dot remains constant, and no current flows through the device. When the charging energy is the dominating term in the addition energy, this phenomenon is called Coulomb blockade. It has been achieved in all sort of system and only requires charge quantification [VH92].

The Coulomb blockade is lifted by changing the gate voltage so that the next QD chemical potential level is located below one of the two reservoirs. Then, one extra electron can tunnel into the dot, increasing the occupation number from $N-1$ to N. If the QD is located within the bias windows as in Fig. 1.7(c), then the extra electron will tunnel to the drain and a new one will be injected from the source and reproduce the same scheme. This sequence is called single-electron tunneling and is responsible for the Coulomb peaks in the detected current. We note that these transport measurements can be used to probe the dot energy spectrum since the distance between two peaks is given by the addition energy E_{add}.

Like for a quantum point contact, the SET can be used as a sensitive electrometer by

polarizing the gate electrode on the edge of a Coulomb peak, where the current derivative is maximized.

To conclude, the quantum point contact and the single-electron transistor can both be used as remote electrometer to probe a quantum-dots system. However, their measurement bandwidth is usually limited around 10 kHz due to the RC-constant arising from the device resistance ($\sim 10\,\mathrm{k\Omega}$) and the capacitance of the cables used to connect the device to a room-temperature electronics ($\sim 100\,\mathrm{pF}$). The bandwidth and the sensitivity can be enhanced by integrating a resonant circuit within the electrometer and probe its resonance amplitude, a circuit known as RF-QPC or RF-SET [Sch98]. The high-frequency operations of these detectors ($\gtrsim 100\,\mathrm{MHz}$) are not prone to $1/f$ noise as DC measurements. Sensitivities as small as $\sim 2 \times 10^{-4}\, e/\sqrt{\mathrm{Hz}}$ has been reported for single charge detection with a 20 MHz bandwidth [Cas07]. Nevertheless, footprints of the QPCs and the SETs are still substantial due to their own local reservoirs. In the next section, we will discuss how gate-reflectometry can integrate a charge sensor directly into the probed structure.

1.3.2 Single lead quantum-dot with RF-reflectometry

Electrometers based on transport measurements with QPCs and SETs have been used to demonstrate many milestones towards large-scale spin-qubit quantum computers [Pet05; Wat18]. When these structures are combined with RF-reflectometry, one can engineer a radio-frequency circuit to multiplex the readout of all these electrometers and greatly reduce the impact of the charge sensors wiring. It is an important requirement to build a functional quantum machine with millions of qubits and at least as many quantum-dots to probe. However, transport measurements induce a huge overhead in terms of design footprint with the necessity to add the full control of a quantum-dot, two ohmic contacts, and the corresponding control electronics. Consequently, it is difficult to envision their use as local electrometers in large-scale QD arrays.

A promising candidate to perform such operation is gate-based dispersive readout. This technique consists of probing the so-called quantum capacitance between a gate electrode and a quantum-dot. The quantum capacitance is a quantum-dot state dependant quantity related to the electric susceptibility of the dot. It is monitored by looking at changes in a radio-frequency tone applied on the electrode and reflected at the dot-electrode interface. Using this principle, single lead quantum-dot (SLQDs) electrometers have been developed to probe the charge dynamics of linear QD arrays [Ans20; Cha20b]. In this section, we detail the working principle of these SLQD electrometers in the context of Part 3. More complete explanations can be found in [Cot11] and [Miz17].

Model circuit

To understand how the quantum capacitance arises, we model our SLQD as shown in Fig. 1.8(a). The dot is capacitively coupled to its electrode via a capacitance C_{G1}, tunnel-coupled to a metallic reservoir ($R_{\mathrm{S1}}, C_{\mathrm{S1}}$) and has a charging energy $E_{\mathrm{C}} = e^2/C_1$ with $C_1 = C_{\mathrm{G1}} + C_{\mathrm{S1}}$ the dot total capacitance. The source node is used to inject charges into the dot, and its voltage is considered as grounded. The dot-gate effective capacitance C_{eff}

is defined as the variation of induced charges with respect to the apply voltage, namely

$$C_{\text{eff}} = \frac{\partial \langle Q_{\text{G1}} \rangle}{\partial V_{\text{G1}}}. \tag{1.11}$$

Here, we have introduced the gate injected charge Q_{G1} within brackets to denote a quantum expectation value. Indeed, the quantum capacitance cannot be caught by a purely classical model, and we have to consider quantum corrections.

Similarly to Sec. 1.2.1, we can compute the induced charges from the electrostatic constant interaction model as $Q_{\text{G1}} = C_{\text{G1}} (V_{\text{G1}} - V_1)$ and $V_1 = (C_{\text{G1}} V_{\text{G1}} - eN)$ with N the number of electrons inside the dot. So, we can express the number of charges induced by the gate electrode as

$$\langle Q_{\text{G1}} \rangle = \frac{C_{\text{S1}} C_{\text{G1}}}{C_1} V_{\text{G1}} + e \frac{C_{\text{G1}}}{C_1} \langle N \rangle . \tag{1.12}$$

In our classical electrostatic model, the dot occupation N depends on the dot chemical potential, as described in Fig. 1.8(b). At zero temperature, the dot population describes periodic sharp steps located at the charge degeneracy points, where a dot chemical potential is aligned with the reservoir. To obtain the quantum-dot occupation $\langle N \rangle$, we introduce the following Hamiltonian to model our quantum-dot circuit :

$$\widehat{H} = \sum_{N \in \mathbb{Z}} \left[E_{\text{C}} (N - N_{\text{G1}})^2 |N\rangle \langle N| - \frac{t_c}{2} (|N\rangle \langle N+1| + |N+1\rangle \langle N|) \right]. \tag{1.13}$$

It corresponds to the charge limit of the well studied cooper-pair box [Büt87], adjusted for single electron tunneling. The first term gives the electrostatic energy of the dot for each occupation state $|N\rangle$, with $N_{\text{G1}} = C_{\text{G1}} V_{\text{G1}}/e$ the number of charges induced by the V_{G1} gate voltage. Then, the second term is responsible for the tunneling of single electron charges into the quantum-dot from the reservoir with a characteristic tunnel coupling t_c. This Hamiltonian is associated with a discrete and periodic energy spectrum with a period given by the charging energy E_{C} as the dot energy is continuously tuned by N_{G1}.

Simplified Hamiltonian

We limit ourselves to a regime where the temperature is small compare to the tunnel coupling, and the tunnel coupling is small compare to the charging energy ($k_{\text{B}}T \ll t_c \ll E_{\text{C}}$). Thus, the interactions between charge states have to be considered only for two successive states, $|N\rangle$ and $|N+1\rangle$, close to the charge degeneracy points. When the reservoir is not aligned with a dot level, the quantum-dot can be defined by a pure charge state $|N\rangle$. Consequently, we can focus our study on a two-level system by dealing only with two charge occupancies $|0\rangle$ and $|1\rangle$ close to their charge degeneracy point. This sub-system is representative of the global Hamiltonian for any consecutive charge states.

From the simplified Hamiltonian

$$\widehat{H} = \begin{pmatrix} E_{\text{C}} (1 - 2N_{\text{G1}}) & t_c \\ t_c & -E_{\text{C}} (1 - 2N_{\text{G1}}) \end{pmatrix}, \tag{1.14}$$

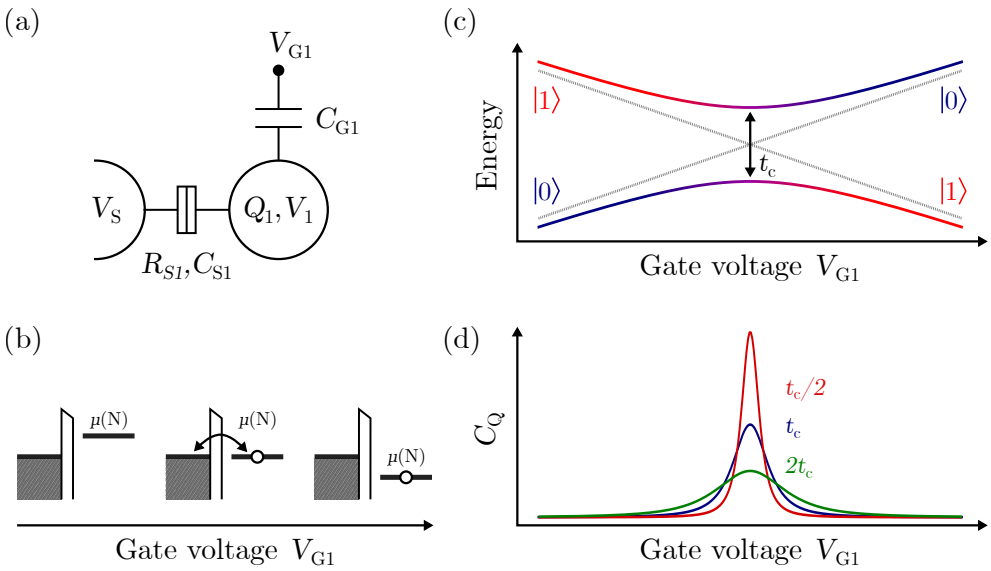

Figure 1.8: Quantum capacitance of a single-lead quantum-dot.
(a) Electrostatic model of a quantum-dot connected to a single metallic reservoir. The dot occupation is controlled by the voltage gate V_{G1} through the capacitance C_{G1}. **(b)** Schematic of the dot electrochemical potential for different gate voltage V_{G1} in the constant interaction model. Three cases are considered, from left to right : (i) the gate voltage is too small for the $\mu(N)$ level to be populated. (ii) the gate voltage bias the dot at the charge degeneracy point. An electron tunnel back and forth from the reservoir into the dot and spend, in average, the same time in the dot than in the reservoir. (iii) the gate voltage is large enough to ensure that the dot is populated 100% of the time. **(c)** Energy diagram of the two eigenstates $|+\rangle$ (lower branch) and $|-\rangle$ (upper branch) from the simplified Hamiltonian in a configuration where $t_c = E_C/100$. In dashed lines, we represent the limit with no tunnel coupling, $t_c = 0$. For low gate voltage V_{G1}, the dot is in a pure $|0\rangle$ ground-state. As V_{G1} increases, the eigenstate is described by a superposition of the two pure charge states. At the charge degeneracy point, the dot polarizability is maximized with $|+\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$. At this point, the spacing between the two branches is given by the tunnel coupling t_c. Similarly, the dot is in a pure $|1\rangle$ ground-state for large gate voltage. **(d)** Plot of the quantum capacitance with respect to the gate voltage value. The quantum capacitance is proportional to the band curvature of the $|+\rangle$ state, as plotted in (c). Its value is non-zero only close to the charge degeneracy point where it is maximized. The quantum capacitance is plotted for three different values of tunnel coupling $t_c/2, t_c, 2t_c$, with $t_c = E_C/100$. As the tunnel coupling decreases, the quantum capacitance's maximum value increases while the peak becomes narrower.

we easily compute the two eigenstates and their eigenenergies

$$\begin{aligned} |+\rangle &= \quad \cos(\theta/2)\,|0\rangle + \sin(\theta/2)\,|1\rangle \\ |-\rangle &= -\sin(\theta/2)\,|0\rangle + \cos(\theta/2)\,|1\rangle \end{aligned} \tag{1.15}$$

$$E_{\pm} = \mp\sqrt{E_{\mathrm{C}}^2\left(1-2N_{\mathrm{G1}}\right)^2 + t_c^2}, \tag{1.16}$$

where we have introduced the angle $\theta = \arctan\left[t_c/\left\{E_{\mathrm{C}}\left(1-2N_{\mathrm{G1}}\right)\right\}\right]$. We plot on Fig. 1.8(c) the energy associated with the two eigenstate branches with respect to N_{G1}, the number of charges induced by the gate voltage . For a number of induced charges far from the degeneracy point $N_{\mathrm{G1}} = 0.5$, the eigenenergies depend linearly on N_{G1}, and the associated states are comparable to the pure charge states $|0\rangle$ and $|1\rangle$. However, close to the charge degeneracy point, the two states are coupled via the tunnel-coupling t_c, and the actual quantum state is a superposition as described in Eq. 1.15. In particular, at the degeneracy point, one electron spends 50% of the time in the reservoir and 50% of the time in the dot. The spacing between the two bands at this point is directly equal to the tunnel coupling t_c.

Quantum capacitance

Now that we understand how the system energy evolves with the gate voltage $N_{\mathrm{G1}} = C_{\mathrm{G1}}V_{\mathrm{G1}}/e$, we can compute the dot occupation's expectation value near a degeneracy point. By using the derivative of the former Hamiltonian $\frac{\partial \widehat{H}}{\partial N_{\mathrm{G1}}} = 2E_{\mathrm{C}}\left(N_{\mathrm{G1}} - N\right)$ and considering only the groundstate branch $|+\rangle$, we obtain

$$\langle N\rangle = N_{\mathrm{G1}} - \frac{1}{2E_{\mathrm{C}}}\frac{\partial E_+}{\partial N_{\mathrm{G1}}}. \tag{1.17}$$

Thus, by injecting this result in the induced charges $\langle Q_{\mathrm{G1}}\rangle$ (see Eq. 1.12), we compute the dot-gate effective capacitance as

$$C_{\mathrm{eff}} = C_{\mathrm{G1}} - \frac{C_{\mathrm{G1}}^2}{e^2}\frac{\partial^2 E_+}{\partial N_{\mathrm{G1}}^2}. \tag{1.18}$$

In this equation, the first term is the constant geometrical capacitance arising from the classic electrostatic. The second term corresponds to the so-called quantum capacitance C_{Q} and depends on the dot polarization. Its amplitude is maximum when the curvature of the dot energy band is the largest. In our case, it coincides with the charge degeneracy point, due to the band opening proportional to the tunnel coupling. Using Equation 1.16, we derive the expression of the quantum capacitance in the lower branch as

$$C_{\mathrm{Q}} = \frac{C_{\mathrm{G1}}^2}{C_1}E_{\mathrm{C}}t_c^2\left[E_{\mathrm{C}}^2\left(1-2N_{\mathrm{G1}}\right)^2 + t_c^2\right]^{-\frac{3}{2}}. \tag{1.19}$$

In Figure 1.8(d), we plot the quantum capacitance for different values of the tunnel coupling. We remark that the quantum capacitance maximum value increases when the tunnel coupling decreases, but the region of N_{G1} where it is non zero becomes increasingly

small.

We add an inductor in series with the gate electrode to build an electrometer out of this single-lead quantum dot. Then, the circuit behaves as an LC resonant circuit with a resonance position that depends on the quantum-dot state through the quantum capacitance. By biasing the SLQD at a degeneracy point, any change in its electrostatic environment will slightly modify the dot alignment and consequently reduce the quantum capacitance. In T. Duty *et al.* [Dut05], the maximum phase change of a reflected wave on the resonator due to the quantum capacitance is estimated to be

$$\Delta\Phi \simeq 2Q \times C_{\mathrm{Q}}/C_{\mathrm{p}}, \tag{1.20}$$

with Q the quality factor of the LC circuit and C_{p} the total parasitic capacitance to ground. We describe the experimental setup used to probe such SLQD electrometer in Sec. 2.4.3. This expression is obtained by considering the parasitic capacitance to ground much larger than the dot capacitance C_1, as we will confirm in Sec. 3.2. Furthermore, we can compute the maximum phase change of the SLQD resonator at a charge degeneracy point

$$\Delta\Phi^{\max} \simeq 2Q \times \frac{\left(\alpha_1^{\mathrm{G1}}\right)^2}{t_{\mathrm{c}} C_{\mathrm{p}}}. \tag{1.21}$$

Thus, one way to improve the SLQD signal is to use a device with a large lever-arm α_1^{G1}. In this context, the gate-reflectometry is well suited for our silicon nanowires with large gate lever-arms compared to the GaAs devices.

Besides, we note that the radio-frequency sent to perform the dispersive readout has an additional requirement. In the present analysis, we have assumed that the quantum-dot state remains all the time in the ground-state branch $|+\rangle$, which is valid only for RF tone frequencies and amplitudes small compared to the dot tunnel coupling so that the excited branch is not populated through non-adiabatic crossing [Zen32].

In summary, we have demonstrated how to build an electrometer from a quantum-dot connected to a single lead by harvesting the possibility offered by the quantum capacitance. Sensitivities as low as $\sim 67\,\mu e/\sqrt{\mathrm{Hz}}$ have been achieved for single charge detection with an SLQD in a silicon CMOS device, outperforming the RF-SET discussed previously [Ibb20]. Also, the quantum capacitance peaks when the charge polarizability is maximum for the quantum-dot. It is not sensitive to the dot absolute occupancy number but to tunneling events only. Nevertheless, this phenomenon is quite general and goes beyond the SLQD studied here. For example, the reservoir-free dispersive readout of an electron-spin state has been shown in a double quantum-dot [Cri19]. We note that in this case, it is not an electrometer since the sensor is blind to certain charge transitions.

1.3.3 Conclusion

In this section, we have developed different charge electrometers for semiconductor quantum-dots. We have focused our study on remote charge sensing techniques where the detector back-action is limited compared to transport measurements through the quantum-dot system to probe.

First, we have considered electrometers with the use of quantum point contacts and single-electron transistors. The former is a two-dimensional constriction where the conductance is quantized with integer numbers of channels available. It features sharp steps in the QPC IV characteristic used as polarization points to increase the electrometer sensitivity. In general, SETs offer more tuning possibilities and permit to adjust for potential impurities. They rely on the Coulomb blockade to demonstrate steep peaks in the measured current. However, these two methods have a limited bandwidth due to the RC constant arising from both the device resistance and the wiring capacitance. This disadvantage is overcome by radio-frequency reflectometry with high-bandwidth, multiplexable readout. Nevertheless, the main limitation of these electrometers based on transport properties is their significant footprint using two ohmic contacts.

Consequently, we have developed the working principles of a single-lead quantum-dot probed by gate reflectometry. In addition to a classical geometrical capacitance, we have demonstrated that a quantum-dot gives rise to a state-dependent quantum capacitance. This quantum capacitance depends on the polarizability of the dot, and is maximum at the charge degeneracy points, where an electron is oscillating back and forth between the quantum-dot and the reservoir.

In the next section, we investigate the control of quantum-dot arrays, while we have focused only on single quantum-dot so far. In particular, we will highlight the charge sensing methods used in different examples from the literature.

1.4 Control of quantum-dot arrays

So far, we have considered how to build a quantum-dot in a semiconductor nanostructure and how to probe the charge dynamics of such structures using a remote electrometer.

Here, we start by looking at the properties of two quantum-dots tunnel-coupled. This system is called a double quantum-dot (DQD) and is the fundamental building block to develop QD arrays. We expand the constant interaction model developed previously to this system and show how the quantum-dots exchange electrons. Also, we summarize the automatic tuning procedures developed in the literature to get the desired occupation numbers and couplings.

Then, we go beyond the double quantum-dot and consider quantum-dot arrays. We distinguish the linear QD chains where dots are connected to only two neighbors, from the two-dimensional arrays with at least four neighbors per dot. As we will discuss, arbitrarily long linear arrays have been developed by successfully reproducing the device geometry proven in DQD experiments. Now, 2D arrays have been limited to small 2x2 QD devices, with the exception of a single 3x3 QD array. We explore the reasons and the difficulties linked to such structures.

Next, we detail the so-called isolated regime. This operation protocol consists of coupling the QD array to the electron reservoirs not all the time, as usually, but only when it is necessary. As we will describe, this simple scheme greatly simplifies the array operation by forcing the total number of electrons in the system constant during an experiment.

Finally, the development of large-scale quantum-dot arrays is considered. In particular, we demonstrate that the number of gate electrodes per quantum-dot must be reduced

to increase the number of QDs. Large scale 2D arrays are presented along the use of row/column addressing.

1.4.1 Double quantum-dot

We start by describing a structure made out of two quantum-dots in series. This system, depicted in Fig. 1.9, is built similarly to the single-dot circuit (see Fig. 1.1). We denote QD1 the left quantum-dot, and QD2 the right one. Each dot is coupled to the system gate electrodes V_{A} and V_{B} via the capacitances $(C_{1\mathrm{A}}, C_{1\mathrm{B}})$ for QD1 and $(C_{2\mathrm{A}}, C_{2\mathrm{B}})$ for QD2. QD1 is tunnel-coupled to the source reservoir, and QD2 to the drain. Finally, QD1 and QD2 are capacitively coupled, and tunnel coupled to exchange electrons so current can flow through the device.

If a single quantum-dot is an artificial atom, then this structure behaves like an artificial molecule. Here, the inter-atomic coupling is given by the tunnel coupling between the two dots. Assuming that it can be experimentally tuned, the system can be shifted from an ionic-like character with localized electrons on each dot to a covalent-like behavior where electrons are delocalized over both dots.

In the following, we start by looking at how evolves the quantum-dot occupations with respect to the gate voltages for different inter-dot tunnel coupling regimes. We will then show how such devices are tuned experimentally and explore the charge control protocols discussed in the literature.

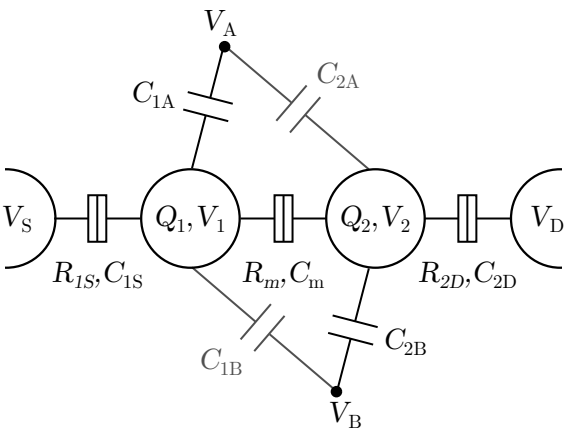

Figure 1.9: Schematic circuit of a double quantum-dot. Two quantum dots QD1, and QD2 are embedded in an electric circuit. The gate electrodes V_{A} and V_{B} tune the dots chemical potential through the capacitances C_{iK} for each dot i and gate K. Source and drain reservoirs bring electrons into the quantum-dot system and allow current measurements through the device.

Charge stability diagram

To understand how the charges occupy the two quantum-dots, we have to compute each dot's electrochemical potential in the constant interaction model. In particular, we need to take into account the cross-capacitance couplings $C_{1\mathrm{B}}$ and $C_{2\mathrm{A}}$, the inter-dot capacitance C_{Cm}, and the presence of the source and drain reservoirs. Here, we directly give the result for the electrochemical potential of QD1. The full derivation of a DQD circuit can be

found in Sec. 4.3 in the isolated regime, with no coupling to the reservoirs. We found for QD1 the chemical potential with respect to the dot occupation numbers N_1 and N_2

$$\begin{aligned}\mu_1(N_1, N_2) &\stackrel{\text{def}}{=} U(N_1, N_2) - U(N_1 - 1, N_2) \\ &= \left(N_1 - \frac{1}{2}\right) E_{\text{C1}} - \frac{E_{\text{C1}}}{|e|}\left(C_{1\text{S}}V_{\text{S}} + C_{1\text{A}}V_{\text{A}} + C_{1\text{B}}V_{\text{B}}\right) \\ &\quad + N_2 E_{\text{Cm}} + \frac{E_{\text{Cm}}}{|e|}\left(C_{2\text{D}}V_{\text{D}} + C_{2\text{B}}V_{\text{B}} + C_{2\text{A}}V_{\text{A}}\right) \ .\end{aligned} \tag{1.22}$$

The first two terms are equivalent to what we have found in the single quantum-dot expression, with the addition to the cross-capacitance couplings. Then, the last terms contain the inter-dot capacitive coupling. In this picture, the mutual charging energies E_{Cm} is the change in energy of one dot when an electron is added to the other one (see Eq. 4.5).

Now, we can figure out how the different electrochemical levels arrange themselves in our quantum-dot system. In particular, we want to determine the equilibrium electron numbers in each dot, labelled (N_1, N_2), as a function of the gate voltages V_{A}, V_{B}, and the inter-dot coupling. These charge states are summarized on so-called stability diagrams shown in Fig. 1.10. In these schematics, equilibrium occupancy number areas are delimited by solid lines. While remote charge sensors map each of these transitions up to the electrometer sensitivity, transport through the device occurs only for the specific conditions detailed below.

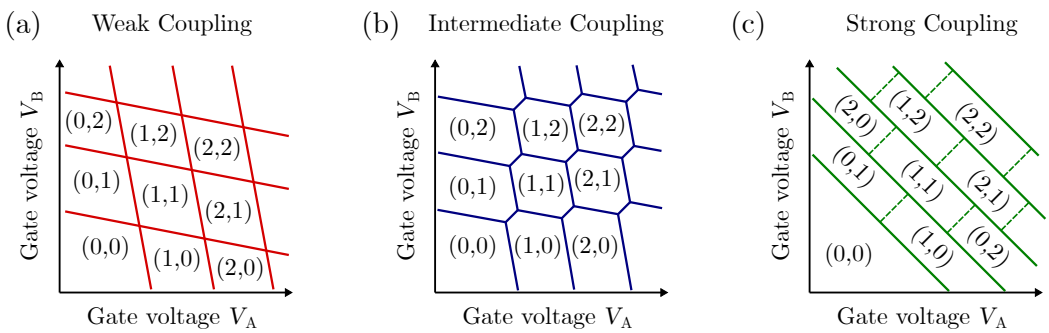

Figure 1.10: Charge stability diagrams of a double quantum-dot
Schematic stability diagram of a DQD in the **(a)** weak, **(b)** intermediate, and **(c)** strong coupling regimes (see main text).

For uncoupled double quantum-dots $C_{\text{m}} \to 0$, we plot the corresponding stability diagram in Fig. 1.10(a). We see that starting from an empty double dot (0,0) at the bottom-left of the diagram, each dot population increases as the associated gate voltage becomes more positive and that a charge degeneracy line is crossed. However, we note that the charge degeneracy lines are not purely horizontals nor verticals. This is due to the cross-capacitive coupling, which for example reduces QD1 electrochemical potential when V_{B} is increased. Electrons can be transferred from the source to the drain reservoir at each crosspoint between two degeneracy lines in this regime. Indeed, at these points, tunneling sequences like $(N, M) \to (N+1, M) \to (N+1, M+1) \to (N, M+1) \to (N, M)$ are possible within

the bias window.

When we turn on the mutual capacitance, the 4-fold degeneracy at each crosspoint is lifted, as pictured in Fig. 1.10(b). Each crosspoint is split into two so-called triple points that reveal the characteristic honeycomb lattice of two coupled quantum-dots. The distance between the triple points is set by the inter-dot capacitance C_{m}. Electronic transport is allowed only at these triple-point through typical sequence similar to $(N, M) \rightarrow (N+1, M) \rightarrow (N, M+1) \rightarrow (N, M)$ The inter-dot tunnel coupling t_c is responsible for bending the honeycomb lines near the triple points and blurred the single-particle picture.

Finally, for strongly coupled dots $C_{\mathrm{m}} \simeq C_1, C_2$, the inter-dot capacitive coupling is dominant compare to the gate couplings (Fig. 1.10(c)). Consequently, the honeycomb features disappear, and the system behaves like a single bigger dot. We can no longer distinguish the position of one electron located either in QD1 or QD2 from the charge degeneracy lines.

Tuning of double quantum-dots

Semiconductor double quantum-dots are a fundamental building block towards realizing QD arrays in the perspective of charge or spin-based quantum computing units. They exist in various platforms, including the GaAs heterostructures, and the silicon nanowires described previously. However, the tuning of a double quantum-dot is a non-trivial task in all of these platforms.

A DQD like in Figure 1.9 requires controlling each dot's occupation number, the tunnel couplings to the reservoirs, and the inter-dot tunnel coupling. The experimental knobs to accomplish this task are the gate electrode voltages available on the device. Due to the cross-capacitive couplings, each change on a gate electrode might affects all the different physical parameters. Also, device variability, induced by local charge traps and other defects, makes the gate tuning device-dependent and even susceptible to thermal cycles for the same device.

The tuning of semiconductor double quantum-dots is usually separated into two consecutive steps. The first procedure is the coarse tuning of the device, consisting of forming the quantum-dots and their depletion into the few-electron regime, as in Fig. 1.10. Current experiments still configure the device heuristically and adjust the gate voltages based on a human operator's experience and intuition. Finding the set of voltages yielding the desired confinement at the intended positions is a time-consuming iterative process. Each experiment produces results to interpret, followed by the parameter adjustments' decision. The interpretation of the results is usually the limiting factor for automated tuning algorithms, since a non-tuned device can produce complex features that cannot be fitted with the simple models developed previously.

However, machine learning algorithms have recently emerged as a "plug-and-play" technique for automated image classification [Kri12]. These algorithms are starting to be used to recognize quantum-dots states and guide the tuning process, instead of a trained operator [Kal19; Zwo20]. We detail in Fig. 1.11 the algorithm used by Zwolak *et al.* to autotune a QD system to a single or a double quantum-dot [Zwo20]. First, the raw data of a stability diagram is resized and normalized to feed into the machine learning algorithm. Then, the convolution neural network assigns a probability vector to the device's state as

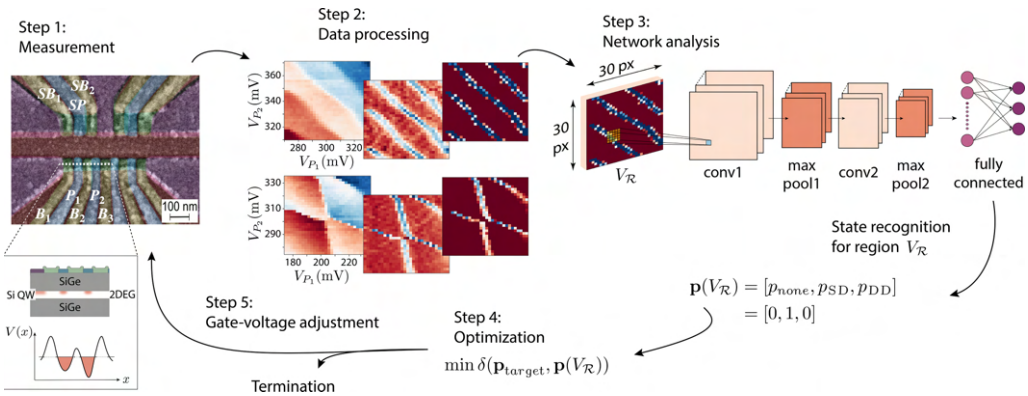

Figure 1.11: Machine learning algorithm for the coarse tuning of a double quantum-dot. Reproduced from [Zwo20]. In Step 1, a stability diagram experiment is runned on the device. The results are processed in Step 2 to remove the noise, and normalize the data sent to the machine learning algorithm in Step 3. The algorithm produces a probability vector that describes the device state as being in a single-dot, double quantum-dot, or no dot regime. Based on this result, an optimization protocol either adjusts the gate voltages and executes a new stability diagram, or terminates the tuning algorithm.

being in a single-dot, double quantum-dot, or no dot regime. Based on this vector and the desired final state, an optimization protocol either adjusts the gate voltages and starts a new experiment, or terminates the tuning procedure.

In particular, a machine learning-based algorithm has performed the coarse tuning of a quantum device "faster than human experts" [Moo20]. Nevertheless, such algorithms are still prone to errors, notably due to biased or incomplete training sets. So, the coarse tuning of a DQD remains an open debate. New propositions solve an increasing part of the tuning problem by successfully fitting the data with specific models instead of relying on machine learning state recognition [LM19].

The second tuning step consists of fine-tuning the dot parameters towards given occupation numbers and specific tunnel-coupling values, once the few-electron regime has been reached. Here, the physical models allow us to predict the system response to a voltage adjustment, and the results can be automatically fitted to extract the DQD physical parameters. Consequently, automated tuning algorithms have already been proposed several years before the coarse tuning approaches' progress [Bot18; Die18].

To conclude, we have discussed in this section the properties of semiconductor double quantum-dots. We have highlighted how the gate electrode voltages and tunnel couplings affect the dot occupancies with the appearance of honeycomb patterns in charge stability diagrams. Next, the experimental tuning of such structures has been investigated. While the most significant part of this tuning remains heuristic, automatic approaches are investigated to optimize the tuning time. In the next section, we discuss semiconductor arrays beyond the double quantum-dot that incorporate an increasing number of QDs. In this context, automatic tuning is an essential step since the tuning space grows with the array size, making human heuristic control more and more difficult.

1.4.2 Open quantum-dot arrays

In this section, we explore more complex quantum-dot structures than previously and go beyond the double-quantum dots. First, we look at linear arrays of quantum-dots and show how they benefit from the robust DQD platform. Then, we discuss the development of two-dimensional arrays.

Linear arrays

Linear arrays of quantum-dots are the natural step after the double-quantum dots discussed previously. They consist of linear chains of quantum-dots where each dot is only tunnel-coupled to its two neighbors. Linear arrays have been developed by many research groups on different platforms like GaAs heterostructures [Fuj17; Ito18; Qia20], and planar-geometries Silicon [Cha20a], or Si/SiGe [Law20; Mil19]. In the context of large-scale two-dimensional arrays, linear chains are a perfect sandbox to develop charge transfers between sub-parts of the array. As example for spin qubits, the physical transfer of electrons across the device can preserve the spin state and connect coherently remote quantum-dots [Fuj17; Qia20], while direct spin-spin coupling has a too short range [Baa17; Mal19], and indirect coupling mediated by photons has an important footprint [Sca19].

Concerning the control of such arrays, their tuning time increases linearly with the chain length. The tuning procedure's overhead due to the different cross-capacitance couplings is mitigated by the QD's small connectivity. An additional complexity of larger quantum-dot systems is the dimensionality of their charge stability diagram. Indeed, a comprehensive DQD stability diagram simply consists of a two-dimensional plot where each dot's charge is manipulated independently on the two axes. A conventional stability diagram is only a 2D cut of a higher dimensionality charge stability volume for larger linear arrays.

In Figure 1.12(a), a quadrupole QD linear array in a AsGa heterostructure is displayed (from [Fuj17]). In the QD chain, gate electrodes are designed to address either a specific tunnel coupling or the chemical potential of a dot. Each end of the array is tunnel-coupled to metallic reservoirs in order to load electrons into the structure. A remote single-electron transistor probes the charge dynamics inside the array. A stability diagram of the four-dots is plotted in Fig. 1.12(b). This diagram has been optimized to show the charge transfer of a single-electron from the array's left side, where two electrons have been loaded to the right end. It uses the two most external plungers P1 and P4 to perform the charge transfer through the points (I, A, B and C), as depicted in Fig. 1.12(b).

In this stability diagram, the different dot-to-dot and dot-to-lead transitions have different slopes and differ greatly from the honeycomb pattern of a DQD. In particular, as the dot number increases, it becomes more difficult to distinguish the transitions by their slopes due to the cross-talk. Besides, the spacing between each line varies as the addition energy spectrum is non-uniform across the array. We see that the four charge states of interest exhibit a complex geometry with the requirement to use each time the two gate electrodes in order to cross a transition.

Furthermore, this region of the charge stability volume clusters the charge states close to transitions that do not conserve the total number of electrons inside the system, which renders more complex its operation. Finally, the loading of a linear array is performed with the electron reservoirs located at each array's end. It means that each dot on the

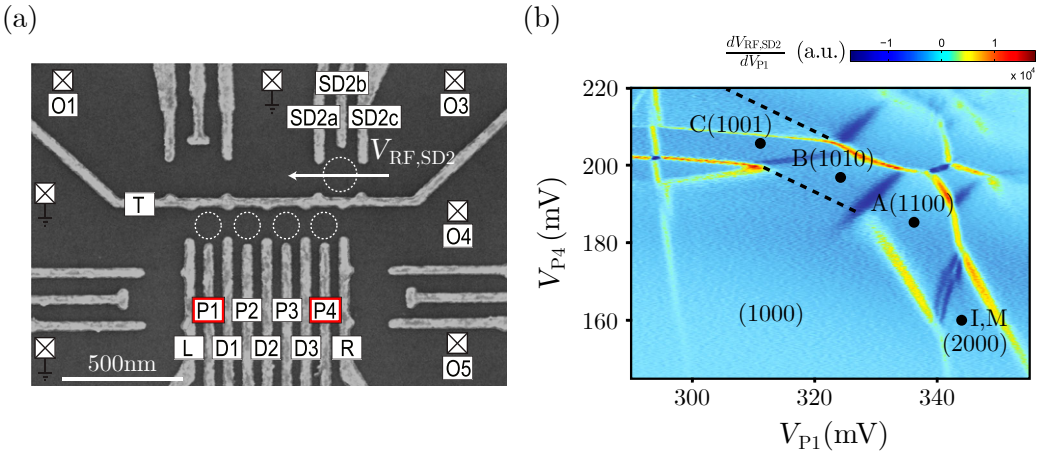

Figure 1.12: Charge stability diagram of a linear array of quantum-dots. Reproduced from [Fuj17]. **(a)** Scanning electron microscope of the linear array. Metallic gates deposited on top of a GaAs heterostructure can shape the 2DEG underneath. The dotted circles indicate the linear chain's quantum-dot positions and for the single-electron transistor used as a remote electrometer. **(b)** Charge stability diagram for the shuttling of one electron from the left side to the array to the right end. The array is initialized with two electrons in the left-most dot at the position I. A single electron is then transferred sequentially to the right end through the point A, B, and C.

chain has a different tunnel rate to the reservoirs and that the loading of dot inside the array is achieved through co-tunneling. In consequence, the stability diagrams can show latching of electron loading or missing charge transitions for failed loading, as indicated by dashed black lines in Fig. 1.12(b).

To avoid these issues and facilitate QD chains' formation, a tuning protocol has been proposed for linear arrays of quantum-dots [Vol19]. The first ingredient of this proposal relies on the use of so-called virtual gates. Virtual gates are linear combinations of multiple gate electrode voltages [Hen17; Med13; Mor18]. For example, they can be used to perform any two-dimensional cut in a charge stability volume. Here, they compensate the crosstalk and the background disorder potential.

In Figure 1.13, the stability diagram of a DQD is plotted with respect to the associated plunger gates. The device corresponds to an extended version of the device in Fig. 1.12(a) with eight QD in series. As expected, the cross-capacitive coupling between each plunger and the neighbor dots causes the charge transition lines to have a slope and depends on the whole array's voltage configuration. It means that, as previously, the global charge stability diagram of the QD chain is complex and that the voltages apply to displace one electron in a part of the array would affect the whole structure. To avoid this phenomenon, the cross-capacitive coupling of all the gates with respect to the different dots is characterized. These values are used to build a set of virtual gates with dedicated effects on either a specific dot's chemical potential or a specific tunnel coupling. The result on a DQD is depicted in Fig. 1.13(b). We recover the stability diagram of a DQD with no cross-capacitive coupling in the few-electron regime.

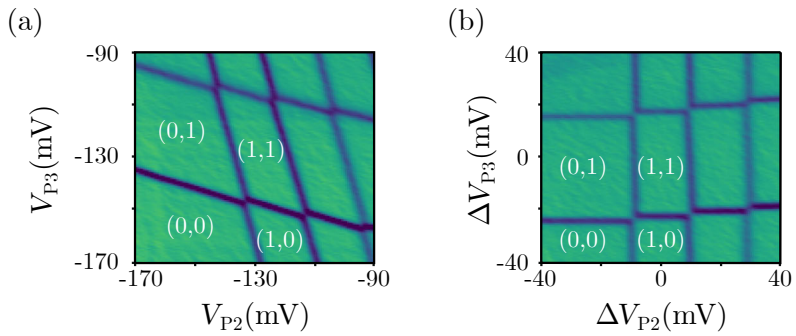

Figure 1.13: Cross-coupling compensation with virtual gates. Reproduced from [Vol19]. **(a)** Charge stability diagram of a DQD in the single electron regime. The cross-capacitive couplings between the electrodes P2 and P3 with the two quantum-dots cause the charge transitions lines to have a slope. **(b)** Same stability diagram than (a) but using the virtual gates ΔP2 and ΔP3 which compensate for the cross-capacitive couplings. The charge transition lines of the two dots are orthogonal. It greatly facilitates the tuning of the linear array since additional QD can be added without disturbing the rest of the chain.

The second ingredient of the tuning protocol for linear arrays is to add the QDs one by one, starting from a simple DQD. Each QD added to the chain is directly connected to a reservoir, and the cross-capacitances are evaluated and corrected to leave the rest of the array untouched. These techniques have been used to control an eight QDs long linear array and constitute a recipe for arbitrary long QD chain in GaAs heterostructures.

To conclude, linear arrays are well-studied QD structures with proven design. Their limited connectivity, where each QD is connected to only two neighbors, facilitates the charge control by dealing with independent DQDs, one at a time. Linear chains have been proposed to develop logical qubit with particular functionalities like the fully electronic-controllable exchange-only qubit [Rus17], and a fault-tolerant qubit using error correction [Jon18]. In the next part, we will increase the quantum-dots connectivity and investigate two-dimensional QD arrays.

Two-dimensionnal arrays

The development of linear QD arrays has relied on the complex gate structures of DQDs. Comparatively, the exploration of two-dimensional arrays has been relatively limited due to different challenges.

First, it took decades to find reliable DQD architectures with the possibility to tune both the dot occupations and their tunnel coupling in a wide enough window. These gate geometries scale well for linear chains like Fig. 1.12(a) but not towards 2D arrays. Consequently, new device structures must be explored, notably by using multiple electrode layers.

Second, the charge sensing of linear arrays is facilitated by using remote SETs along the chain. For 2D arrays, the charge sensors have to be pushed to the array's periphery and fit between the array electrodes. Otherwise, they have to rely on in-situ electrometers like gate reflectometry (see Sec. 1.3.2).

Nevertheless, small 2D arrays have been established in different platforms including

AsGa heterostructures [Muk18; Tha12], planar-geometry Si/SiGe [Law20; Rig20], and silicon nanowires [Ans20; Gil20]. The most advanced realization is a 2x2 spin qubits array in a Si/SiGe heterostructure, with independent control of each qubit and the ability to entangle all of them [Hen20]. Another 2x2 QD array has been used as a quantum simulator to study Nagaoka ferromagnetism, a ferromagnetic phase predicted in the 1960s [Deh20]. Furthermore, we remark that only charge control has been demonstrated in silicon nanowires. The lack of tunable tunnel couplings complicates the spin operations. Besides, all these structures have been limited to 2x2 arrays except for a 3x3 device that we highlight in the next section.

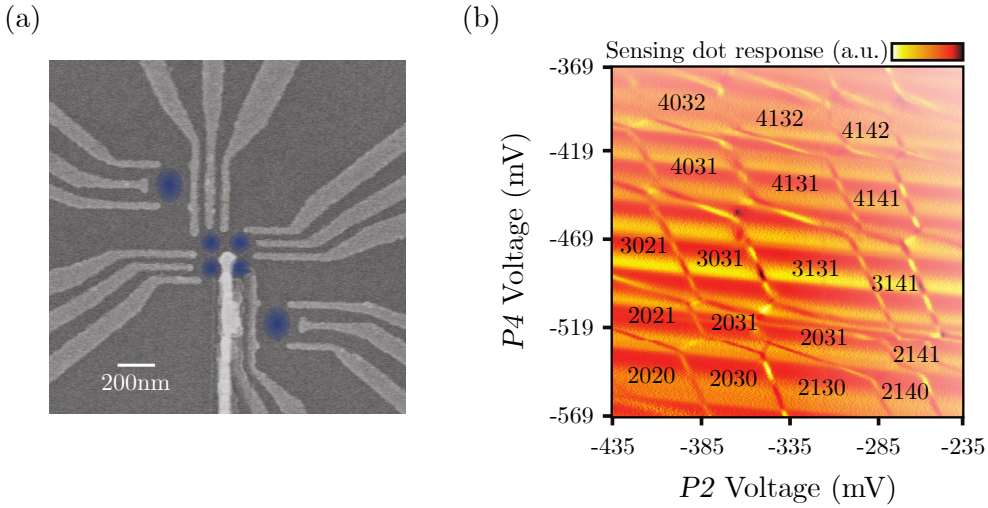

Figure 1.14: Operation of a 2x2 QD array. Reproduced from [Muk18]. **(a)** Scanning electron microscope image of the 2x2 QD array. Two metallic layers of electrode gates pattern the 2DEG located underneath the heterostructure surface. The overlaid blue circles indicate the quantum-dots position. **(b)** Charge stability diagram in the few-electron regime with respect to the plungers associated with two diagonally opposed QDs. The symmetries in the cross-capacitance couplings make it challenging to distinguish a QD charge transition by the degeneracy line's slope. Moreover, it is complicated to navigate through the charge stability volume while keeping a constant number of electrons in the system due to the couplings to the reservoirs.

To understand why, we look at a realization of a 2x2 QD array in a AsGa heterostructure from [Muk18]. If we look at the device geometry in Fig. 1.14(a), we see that the structure hosting each QD is similar to the one used in linear arrays with the addition to a single electrode, deposited after the other gates, that act as the tunnel-barrier at the intersection of all dots. In particular, local electron reservoirs are located to the side of each quantum-dot. As discussed, the SET remote charge sensors are delocalized further away due to their footprint incompatible with the array size. So, this structure benefits from the advantage of the well-proven DQD structure but it is difficult to scale-up.

We now consider the charge control of this array with the stability diagram reported in Fig. 1.14(b). This diagram corresponds to the few-electron regime and uses the plungers associated with diagonally opposed QDs. By looking at the different charge states labeled,

we see that different charge transitions have a similar slope. Indeed, the cross-capacitance couplings' symmetries imply that the two electrodes swept have a similar effect on their two neighbor dots. Besides, the coupling to the reservoirs complicates the array's operation with a fixed number of electrons within the array. It is more difficult to explore this sub-space in the charge stability volume than the linear chain since each dot is coupled to a reservoir.

To conclude, we note that the arrays explored so far have the same dot connectivity as linear chains, with two neighbors per dot. Nevertheless, the tunability, charge control, and device functionalities are enhanced with each device generation. The recent presentation of a fully programmable 2x2 hole spin-qubit in a Si/SiGe heterostructures demonstrate this high level of control [Hen20]. A bigger 2D array has been realized in our group, with a 3x3 QD device and a central dot with four neighbors. To tune this device, the isolated regime has significantly reduced the charge stability volume complexity and enhanced the array tunability, as we will discuss in the next section.

1.4.3 Isolated regime

The operation of quantum-dot arrays requires electron reservoirs to fill the different QDs with the desired occupations and reset the array by releasing the electrons. However, once these loading and unloading procedures have been carried out, the manipulations are limited to operations within the structure, relying on the inter-dot tunnel couplings. It is true even for computation based on spin-qubits, where reservoirs are only used to initiate the qubits and sometimes to read their states using spin-to-charge conversion techniques [Elz04]. Maintaining the tunnel coupling to the reservoirs during the array operations leads to charge stability diagrams challenging to interpret. In particular, this complicates the array operation because it requires carefully exploring the charge stability volumes, avoiding areas where additional electrons may be injected, or accidental unloadings occur. Moreover, it can limit the tunability of the array with for example the impossibility of reducing an inter-dot tunnel coupling without accidentally charging an excess electron.

Here, we introduce a protocol to disentangle the array's operation from the different loading/unloading sequences requiring a coupling to the reservoir. The idea is to close the reservoirs' tunnel barriers when these couplings are not desired and place the array in the so-called isolated regime. Experimentally, the concept is to push the tunnel barriers in a regime where the characteristic tunneling time is much greater than the time required to perform the experiment. Notably, it has been demonstrated that electrons can be conserved for times longer than hours in semiconductor quantum-dots [Han07].

First, this method has a considerable impact on the complexity of the charge stability diagrams. In Figure 1.15(a), we recall the stability diagram of a simple DQD. The charge states describe a characteristic honeycomb pattern. Operating this structure at a fixed number of electrons involves going through the inter-dot transitions depicted in blue and avoiding the dot-to-lead transitions in red. Next, we load $N_{\text{load}} = 1$ electron inside the DQD before going into the isolated regime. In Figure 1.15(b), we see the resulting stability diagram with a single line associated with the inter-dot transition of one electron going from one dot to the other. Thus, the gate voltages applied to control the dots' chemical potentials can be extended over a wider voltage window, which enhances the DQD tunability for this

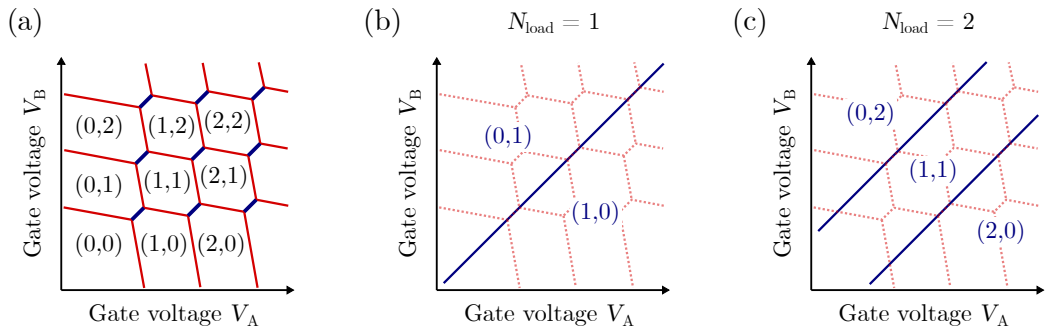

Figure 1.15: Charge stability diagrams of an isolated double quantum-dot. (a) Schematic stability diagram of a DQD in the intermediate regime coupling (similar to Fig. 1.10(b)). **(b)** Schematic stability diagram of a DQD with $N_{\text{load}} = 1$ electron loaded. Only one charge transition line remains and is associated with the inter-dot exchange of one electron from one dot to the other. The dashed red lines in the background corresponds to the open-array stability diagram, for reference. **(c)** Same than (b) with $N_{\text{load}} = 2$ electrons loaded. Only three charge states exist to map all the configurations of two electrons in two quantum-dots.

particular total number of electrons. Similarly, we show the expected stability diagram for $N_{\text{load}} = 2$ electrons loaded in the double quantum-dot (see Fig. 1.15)(c). In this case, only two inter-dot charge transition lines are visible.

We can measure the complexity of an isolated stability diagram by calculating its number of charge states k as

$$k = \binom{N_{\text{dot}} + N_{\text{load}} - 1}{N_{\text{load}}}, \tag{1.23}$$

with N_{dot} the number of coupled quantum-dots, and $\binom{i}{j}$ the binomial coefficient of i choose j. For a simple DQD, the formula simplifies as $k = N_{\text{load}} + 1$ with N_{load} charge transition lines.

To illustrate the benefits of the isolated regime, we introduce the 3x3 two-dimensional array realized in our group by Mortemousque *et al.* [Mor18]. It consists of a GaAs heterostructure with a single metallic layer defining the potential landscape of nine QDs, as pictured in Fig. 1.16(a). Here, we limit ourselves to the five QDs in the cross configuration (T, C, B, L, R) (see figure for corresponding dot labels). In Figure 1.16(b), we show the stability diagram of the isolated array with $N_{\text{load}} = 5$ electrons loaded. This configuration corresponds to a total of $k = 126$ charge states in the complete stability volume, and only 45 of them are visible in this particular stability diagram. The isolated regime made it possible to tune the device in a five electrons in five QDs regime and access only a useful sub-space of this volume, with notably one electron in each dot (indicated by the black arrow). Furthermore, the control of $N_{\text{load}} = 9$ electrons in nine dots have been demonstrated in the same structure, with a total of $k = 24310$ charge states in the charge stability volume. These states would have been difficult to explore in an open array with the presence of different total electron number areas.

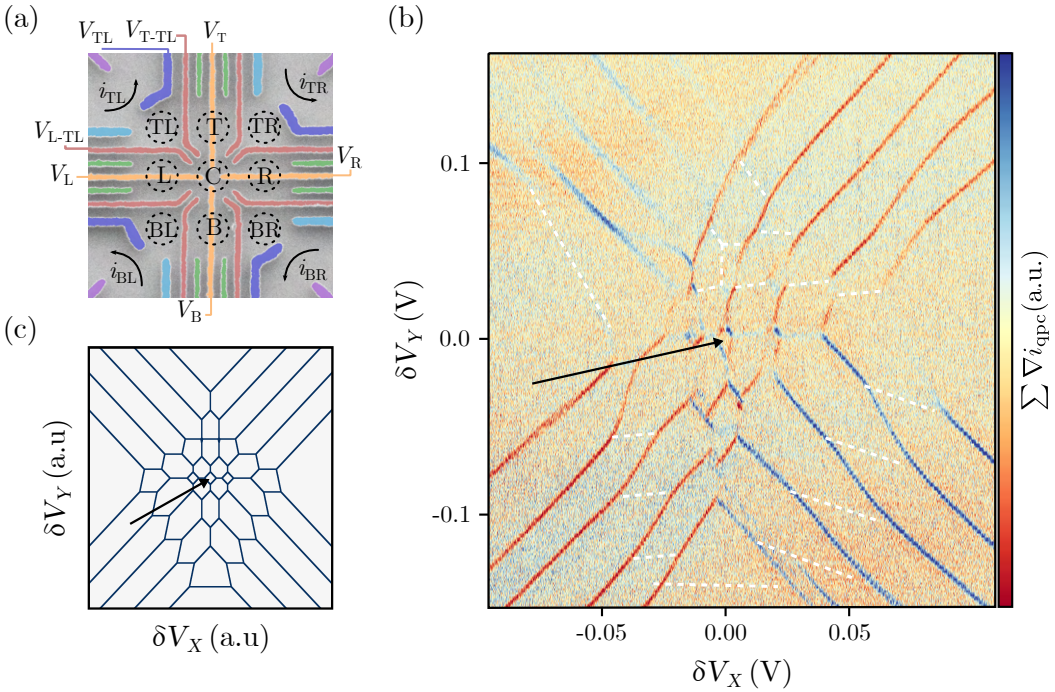

Figure 1.16: Stability diagrams of five isolated quantum-dots. Reproduced from [Mor18]. **(a)** Electron micrograph of the 3x3 QD array. A unique metallic layer defines the potential landscape of the quantum-dots indicated by dashed circles. Four QPCs sense the charge dynamics inside the array. **(b)** Isolated stability diagram with five electrons trapped in a cross-configuration within the quantum-dots (T, C, B, L, R). A linear combination of the QPCs' derivative is plotted as a function of two virtual-gates δV_X and δV_Y. The black arrow points to the one-electron-per-dot state. The electrometers are not sensitive to all charge transition. The white dashed lines are guides for the eye to replace missing lines. **(c)** Simulation of the same stability diagram using the model developed in Sec. 4.3.

To conclude, the isolated regime greatly simplifies QD arrays' charge control and permits a better tunability of the dots' parameters. It has been successfully employed to control QD systems more extensive than a DQD, like a four-QDs linear chain [Bay17] and a 3x3 two-dimensional array [Mor18]. In the latter case, the control of $N_{\text{load}} = 9$ electrons in nine dots have been demonstrated. Also, the coherent displacement of individual electron spins has been showed in three QDs in a loop configuration [Fle17]. Finally, the isolation of electrons from the reservoir improves spin-qubits' relaxation time, as reported in [Ber15b].

1.4.4 Scalability

So far, we have explored quantum-dot arrays with a limited number of dots $N \lesssim 10$. A universal quantum computing unit capable of surpassing today's supercomputers would require the control of over 64 qubits [Che18]. However, realistic qubit realizations are prone to computation errors due to the decoherence of the qubits. To avoid these errors, quantum error correction schemes have been proposed with the idea of redundantly encoding the qubit information in so-called *logical qubits*. The redundancy factor is set by the

physical qubits performances [Dev13; Jon12]. Considering state of the art qubit fidelities in semiconductor quantum dots, the overhead induced by quantum error correction implies 10^3 to 10^4 physical qubits to build a logical one [Fow12; Mar15]. Thus, it is believed that a semiconductor quantum computing unit would require at least $N \simeq 10^6$ quantum-dots to perform computation beyond the reach of the best classical supercomputers. Here, we discuss the various challenges to overcome to increase the QD arrays' size to this limit.

In the last few years, several large-scale quantum-dot array proposals have been developed by different groups [Lee20; Li18; Vel17; Vin18b]. The first step is to control each dot's chemical potential and tunnel couplings individually, while limiting the number of external controls. Indeed, current semiconductor QD arrays are defined on-chip, operated at cryogenic temperatures. So, suppose we scale the QD array discussed in the previous sections to a million quantum-dots where each QD has few gate electrodes. In that case, we obtain a quantum chip with several million terminals that need to be wire-bonded and connected to a room-temperature electronics. This scenario is unrealistic considering the space required for all these connectors and the associated thermal budget. However, a quick review of electronic developments teaches us that classical circuits have already dealt with a similar fate. In the late 1950s, as the number of components increased in electrical circuits, they have necessitated more and more soldering and inter-connections. Ultimately, integrated circuits have solved this issue by building the inter-connects directly on-chip. With the evolution of microelectronics, more and more functionality could be added to a single integrated circuit at the cost of keeping the maximum number of connections to the outside world to a few dozens. This phenomenon is known as Rent's rule and still applies to current integrated circuits such as microprocessors [Chr00]. Notably, a quantum circuit equivalent of the Rent's rule has been derived in [Fra19].

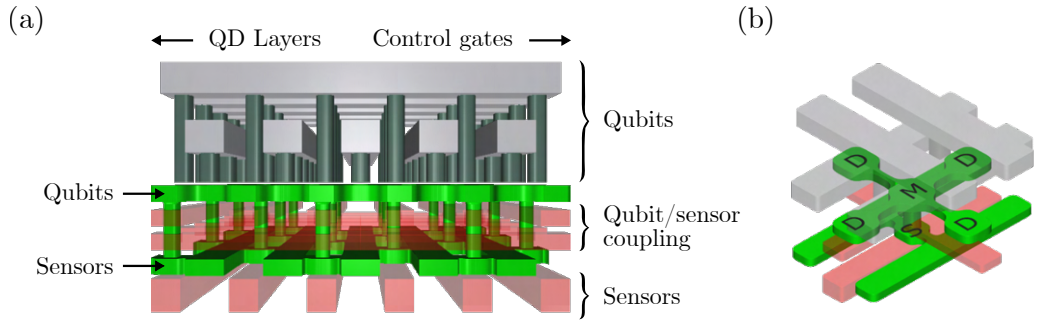

Figure 1.17: A scalable silicon QD array for quantum computing. Reproduced from [Vin18a]. **(a)** Schematic of a three-dimensional architecture for scalable QD arrays in silicon. A set of shared control gates controls a qubit layer consisting of QDs hosting electron-spin qubits. An additional active layer is designed to build local electrometers and reservoirs for the qubit array. The third control mesh turns ON the coupling between the qubits and the sensors during the initialization and the readout steps. **(b)** Schematic of the qubit unit cell. Each cell consists of four QDs in a cross configuration to apply quantum error correction protocols on *measurement* (labeled as M) and *data* (D) quantum-dots.

Consequently, the different proposals for large-scale QD arrays have in common addressing of each quantum-dot through word and bit lines, a concept borrowed directly from

conventional integrated circuits. The idea is to design control gates shared between the different quantum-dots, in a row/column manner. Thus, the number of gate electrodes only scales as $\sqrt{N}$, which is compatible with large-scale integration schemes. In Figure 1.17, we show the scalable QDs architecture proposed by Vinet *et al.* [Vin18a]. In this three-dimensional device, the top two metallic layers form a network of shared control gates. Vias connect the gates to the active layer hosting the qubits' QDs. A qubit cell consists of five QDs in a cross configuration to apply quantum error correction protocols on measurement and data quantum-dots (see Fig. 1.17(b)).

However, row/column addressing adds requirements on the quantum-dots' homogeneity across the device and on the parallel array operations. For example, in an ideal array with perfectly equal QDs, if one row is selected, then any QD along the row can be actuated by applying a voltage to its associated column. According to this principle, different operations can be carried out in parallel in this ideal array. It is good considering that corrections of errors, and more generally quantum algorithms, require operating several QDs in parallel. On the other hand, inhomogeneities between the different quantum-dots impact the parallel operations. In the worst case, only one operation can be executed at a time on the whole array. One way to attenuate these inhomogeneities could be to build local memory gates around each quantum-dot [Vel17]. These memories would save each dot's specific tuning parameters, but would complicate their unit cells.

Next, the charge readout of large arrays should benefit from gate RF-reflectometry and multiplexing. Different RF-reflectometry tones could be sent to each row, with a modulation of the column voltages applied to distinguish each dot's contribution. Otherwise, the proposal by Vinet *et al.* integrates local electrometer underneath each qubit cell. In Figure 1.17, an additional active layer is present to build SLQD sensors just beneath each qubit cell. This second layer of QDs is controlled by its own set of shared gate electrodes. A third control layer with row/column addressing tunes the coupling between the sensors and the qubits. Also, the additional levels permit to directly load electrons inside of the qubit array with these local reservoirs. Other QD array implementations must rely on charge shuttling from reservoirs located at the array's edges to fill each dot.

Finally, an additional challenge is to overcome the crosstalk between each shared electrode and its neighboring dots. We notice that the use of electrodes in a straight line, repeated for each row/column, makes the device's tuning highly symmetric. Thus, the crosstalk should be homogenous along an electrode and compensable using the neighboring lines.

To conclude, we have summarized the large scale quantum-dot array proposals from different research groups. In these structures, the critical ingredient to increase the number of controlled QD is the design of a two-dimensional array with a row/column addressing, similar to integrated circuits. It reduces the total number of gate electrodes as $\propto \sqrt{N}$, and enable dense QD packaging. However, the qubits' tolerance levels are small, so the inhomogeneity of the quantum-dots across the array must be quantified. A compromise exists between the homogeneities of the QDs and the parallelizability of operations, due to the row/column addressing. Furthermore, the charge sensing of large arrays has been discussed using multiplexed gate RF-reflectometry or the development of local SLQD remote electrometers using an additional active layer.

1.4.5 Conclusion

In this section, we have detailed the control of quantum-dot arrays.

We have started by developing a model to understand the interactions between two dots. The charge stability diagram of such systems described a characteristic honeycomb pattern as the total number of charges inside the system is increased. We have discussed tuning procedures for DQD to reach specific occupation numbers and inter-dot tunnel rates. In particular, most automated tuning relies on pattern recognition based on machine learning algorithms.

Then, we have presented linear, and two-dimensional quantum-dot arrays. Linear arrays have a limited connectivity with only two neighbors per dots. However, their gate architectures are close to the one used for DQD and permit to build long chains. An 8-QDs-long linear chain is described with its associated tuning protocol. On the other hand, two-dimensional arrays have limited size due to the difficulty of designing an efficient electrode lattice.

To simplify the array operation, we have introduced the isolated regime. Instead of having the array-leads coupling always turned on, it uses on-demand coupling to the reservoirs to fix the number of electrons in the system during an experiment. As the number of electron states in the charge stability volume increases exponentially with the number of dots, this regime is particularly helpful to focus only on a particular subspace.

Finally, we consider a quantum computing unit's specifications based on QD arrays to compete with conventional supercomputers. We show that more than $N = 1$ million of QDs would be required to outperform the latter and necessitate developing large-scale two-dimensional QD arrays. A key ingredient to increase the number of QDs is to use shared gate electrodes with a row/column addressing which reduces the number of electrode to $\propto \sqrt{N}$.

1.5 Conclusion

In this first chapter, we have discussed how to construct and control quantum-dots in semiconductor nanostructures.

We started by detailing the basics of quantum-dot systems in Sec. 1.2. By introducing the constant interaction model, we modeled quantum-dot circuits and extracted interesting quantities like the charging energy E_{C} and the lever-arm parameter α. Then, we presented the two semiconductor platforms used in this thesis. The first platform is a GaAs heterostructure with a two-dimensional electron gas located 100 nm below the surface of the sample. By applying negative voltages to the gate electrodes deposited on top of the sample, it is possible to pattern the 2DEG arbitrarily. This platform is a good testbed for prototype quantum-dot architecture, as the devices can be manufactured in a few steps within research facilities. The second system is a good candidate for large scale quantum-dots and uses industrial processes to create silicon nanowires. The devices are similar to conventional transistors and feature quantum-dots in the nanowire corners when operating at cryogenic temperatures. Additionally, the silicon lattice is a good host for electron-spin qubits with the ability to get rid of background spin nuclei, which is not possible in GaAs heterostructures.

Next, we explored how to build remote electrometers to probe charge dynamics inside QD systems in Sec. 1.3. A first approach consists of realizing transport measurements through a structure close to the probed system, as performed in Sec. 4.2.1. A quantum-point contact, a local constriction in a 2DEG, induces a quantification of ballistic conductance, and its IV-characteristic is made of sharp steps between conduction plateaus. By biasing the QPC at one of these steps, the measured current is very sensitive to any change in the electrostatic environment, including the charge dynamics within a close-by system to be probed. Similarly, single-electron transistors rely on the narrow Coulomb peaks induced by charge quantization in the dot island to construct sensitive electrometers. Then, a second approach probes the quantum capacitance between a gate electrode and a quantum-dot to perform gate-based dispersive readouts. In particular, we have detailed the operating principle of a single-lead quantum-dot embedded in an LC resonator, as it is realized to probe the charge dynamics inside a silicon nanowire in Chapter 3. This technique has the advantage of using radiofrequency circuits, and several detectors can be multiplexed together (see Sec. 2.4.3).

Finally, we have considered the control of quantum-dot arrays (see Sec. 1.4). We have introduced the basics of double quantum-dots and discussed how to tune such a system. Next, we discussed the realization of QD arrays in the literature. The architecture used to operate linear chains of up to eight QDs was presented, in addition to a tuning procedure compatible with an arbitrary long 1D chain. On the other hand, the realization of two-dimensional quantum-dot arrays has been limited to small lattices with the upper limit of a 3x3 QDs structure. It is due to the complexity of building reproducible and tunable 2D arrays. Plus, 2D arrays raise new challenges in the tuning procedure due to the dots' high connectivity. To simplify their operations, we have described the properties of the isolated regime. The idea is to cut the couplings between the array and the reservoirs when this coupling is unnecessary. The isolated regime greatly simplifies the operation of QD arrays by working with a fixed number of electrons. Ultimately, we discussed the perspective of large-scale quantum-dot arrays. We have defined the requirements of such architectures, induced in particular by a row/column addressing of QDs. Following these prerequisites, we will operate the prototype of a scalable 2D array in Chapter 4.

CHAPTER 2

Experimental setup

2.1 Introduction

As discussed in Section 1.2.1, the typical energy scale in our quantum dot systems is given by the charging energy E_C, which depends on the dot size and ranges from $\sim 1\,\text{meV}$ to $\sim 16\,\text{meV}$. Concerning the temperature, the lower-limit of the charging energy corresponds to a temperature of 10 K. Thus, the sample's electronic temperature must be kept at a much lower value if one wants to resolve single electron loading phenomena. In consequences, the first part of this chapter focuses on the dilution refrigerator used to cool down a sample at 70 mK.

Then, we discuss the two platforms employed in this thesis: a GaAs heterostructure, and a Si nanowire. In particular, we need to pattern structures on these materials at the nanoscale in order to obtain large-enough charging energies. It requires the use of advanced nano-fabrication facilities such as the Neel's Institute cleanroom or the CEA-LETI industry-standard manufacturing line. In this context, we detail how we fabricated the samples and the numerical simulations run to help design samples and facilitate their tuning.

Finally, we need to connect the sample at dilution temperature to room-temperature electronics to form and control quantum dots. To this end, the refrigerator is wired to provide signals at the sample stage without bringing in excessive noise and heat from the control electronics. Additionally, the room-temperature electronics allow DC bias, pulse sequences, and charge sensing via current measurements or a gate-reflectometry setup. Thus, we explain the wiring of the refrigerator and the associated electronics.

We conclude this chapter by introducing the measurement software developed to handle our quantum experiments.

2.2 Cryogenics

The different experiments in this thesis have been hold in a Kelvinox®MX ^{3}He/^{4}He dilution refrigerator from Oxford Instruments©. The refrigerator has a base temperature of 70 mK with a cooling power at 100 mK of the order of 100 µW. During operation, the refrigerator is inserted into a dewar filled with liquid ^{4}He at 4 K. We detail here briefly the basic principle of a dilution refrigerator.

The first proposal of a cryogenic ^{3}He/^{4}He dilution refrigerator dates back to 1951 by H. London, and its first experimental demonstration occurred 13 years later [Das65]. It relies on the mixture of the two stable isotopes of helium (^{3}He and ^{4}He) cooled below a critical temperature $T_c \sim 870\,\text{mK}$. At this temperature, the mixture undergo a phase transition

and split into two phases : a lighter ^{3}He *"pure"* phase (^{3}He concentration $> 99\%$) and an heavier *"dilute"* phase (concentration $< 10\%$). Since the enthalpy of ^{3}He is different in the two phases, we can obtain cooling by pumping the ^{3}He from the dilute phase back into the pure phase. The cooling power is generated at the phase interface and is directly proportional to the forced ^{3}He flow.

The experimental operation scheme of our dilution refrigerator is described in Fig. 2.1. It consists of a dilution unit in a vacuum flask thermally isolated from the 4 K helium bath. The unit is connected to the inlet and outlet of a pump located at room temperature. The different stages of the refrigerator are :

1. First, the ^{3}He gas from the pump exhaust is pre-cooled thanks to the 4 K liquid helium bath.
2. The ^{3}He flow is further cooled at 1.5 K by thermal contact with the *1K-pot*. It consists of a chamber, filled by the ^{4}He bath, continuously pump at a few mbar by an additional pump located at room temperature.
3. To reach the dilution temperature, the *hot* ^{3}He inlet is now cooled by the *cold* outlet, exiting the mixing chamber, by the continuous counterflow heat exchangers (efficient for temperatures $T \gtrsim 50\,\mathrm{mK}$) and step exchangers.
4. The ^{3}He inlet finally reach the mixing chamber where the dilution process takes place.
5. The dilute phase is then pumped out of the mixing chamber, and pre-cool the inlet. This cycle is completed by extracting pure ^{3}He from the dilute phase using the *still*. This chamber is kept at $\sim 800\,\mathrm{mK}$ and $\sim 1\,\mathrm{mbar}$, conditions under which only the ^{3}He evaporates.

The sample under test is thermally anchored to the mixing interface at the end of a cold finger, which embedded the electrical connections required by the experiments.

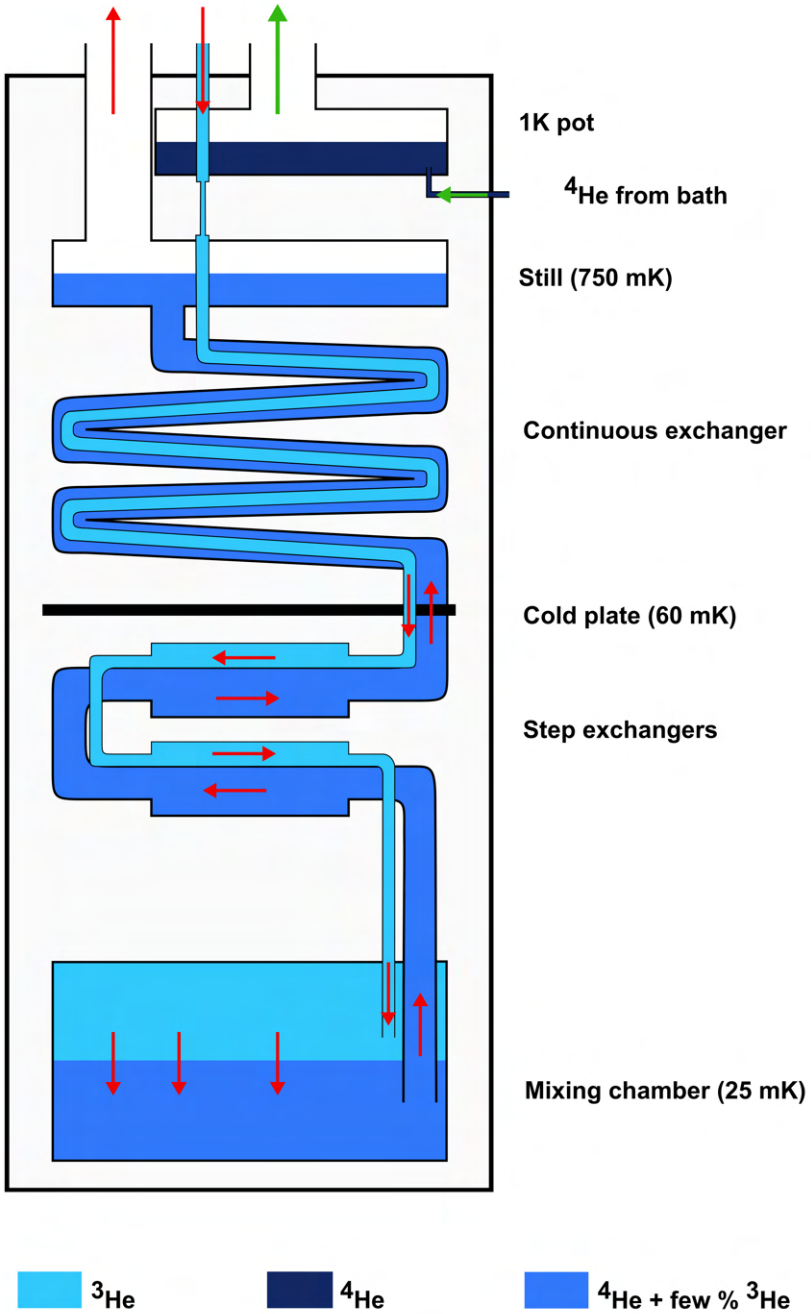

Figure 2.1: Schematic of a dilution refrigerator From [Ber15a]. A ^{3}He inlet is cooled to 4 K with a ^{4}He bath before entering the isolated refrigerator chamber. Then, the inlet is further cooled to 1.5 K by thermal anchoring to the 1 K-pot. It consists of an additional chamber that continuously pump ^{4}He from the helium bath. The dilution process occurs in the mixing chamber, at the bottom of the fridge, for temperatures below 870 mK. In order to reach these temperatures, the ^{3}He inlet is pre-cooled by the outlet through continuous and step exchangers.

2.3 Sample fabrication

As discussed in the introduction, quantum dots can be formed in a multitude of host materials. In this thesis, we explore quantum dot arrays in a silicon nanowire and a gallium-arsenide heterostructure. First, GaAs heterostructure quantum dots benefit from long expertise in fabrication from research facilities. A 2-dimensional electron gas engineered by molecular beam epitaxy can be patterned with metallic depletion gates deposited at the sample surface. However, the quantum dot layer is limited to one 2DEG, which can be a limiting factor for a large-scale architecture, along with a reduced coherence time for spin qubits due to an intrinsic nuclear spin bath. In this context, silicon appears as a better candidate for large quantum dot arrays. Indeed, thanks to the industrial processes developed with the microelectronics, we can envision silicon quantum dot in 3-dimensional architectures.

In this part, we describe how we fabricated quantum dot arrays using both platforms by means of nano-fabrication facilities. Additionally, we show numerical simulations of the electrical potential landscape close to the regime where quantum dots are formed and controlled.

2.3.1 GaAs heterostructure

The first platform used in this thesis is a GaAs/AlGaAs heterostructure with nm-wide metallic gates deposited at the surface, as discussed in Sec. 1.2.2. The group of Andreas Wieck makes the heterostructures by molecular beam epitaxy at the Ruhr-University in Germany. In the context of this collaboration, we receive 2 inch wafers that are then split among the different projects in the group. These crystals hold a 2-dimensional electron gas 90 nm below the wafer surface with a mobility $\mu_e = 1.5 \times 10^6\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and an electron density $n_e = 1.35 \times 10^{15}\,\mathrm{m^{-2}}$.

Once the wafers are received, our device fabrication has been made in the Neel Institute cleanroom facilities. The device's fine structures, depicted in Fig. 2.2(b), need the deposition of two layers of 20 to 40 nm wide metallic gates overlapping each other. The central part of the device holds a 4x4 quantum dot array with line/column addressing control gates. It consists of two sets of long metallic fingers with the vertical gates deposited on top of the horizontal ones. For each set, one gate out of two is a shared tunnel barrier control, and the other ones control the chemical potential of rows/columns. The structures surrounding the array define single-electron transistors probing the array charge dynamics, and belong to the first metallic layer.

Here, we start by detailing the fabrication process of the device. Afterward, we discuss the potential simulations used first to design the device, and then help its tuning during the experiment.

Fabrication process

The device fabrication relies extensively on the ability to imprint user-defined patterns into the substrate. In our case, the realization of resist masks with laser or electron beam lithography allows creating arbitrary patterns. For laser-lithography, we start by spin-coat a uniform layer of photosensitive resist on the sample surface. Next, we load the sample into a laser writing system that can expose patterns on the resist with a µm-resolution. The

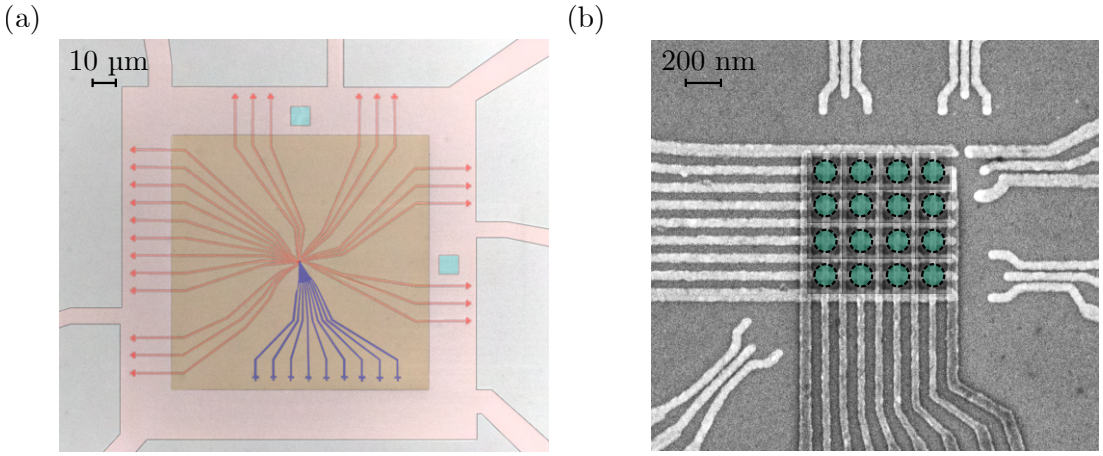

Figure 2.2: SEM pictures of the GaAs sample. (a) False color SEM picture of the device central part before the deposition of metallic connections between the fine structure and the bonding pads. The heterostructure structure surface has been etched to remove the 2DEG everywhere except where needed (light red areas). The first fine structure layer (red gates) is aligned with respect to local alignment marks (cyan). Then, a hafnium oxide patch is deposited (brown) to insulate the second metallic layer (blue gates) electrically. **(b)** SEM picture of the central part of **(a)**. Two sets of horizontal and vertical gates define a 4x4 quantum dot array (green dashed circles). One gate out of two is a tunnel barrier between rows/columns of QD, and the other one tunes the QD chemical potentials. Surrounding structures define single-electron-transistors used to sense the QD array charge dynamics.

sample is then plunged in a dedicated developer solution that will remove only the exposed resist. It results in a resist mask that mimics the desired pattern, and we can either etch the substrate or depose material through the resist trenches. In electron beam lithography, we apply the same procedure but with an electro-sensitive resist and an electron beam writer that uses electromagnetic lenses and deflectors to irradiate the sample with high energy electrons.

We present here briefly the different fabrication steps before going into the details :

1. Mesa patterning, removing the 2DEG outside of the area defined in Fig. 2.2(a).
2. Creation of ohmic contacts, allowing to measure the current flowing through the 2DEG.
3. Patterning of alignment marks for laser and electron beam lithography.
4. Deposition of a hafnium oxide insulating layer by atomic layer deposition in order to prevent the formation of Schottky barriers.
5. Definition and evaporation of the first layer of fine gate structures.
6. Covers part of the first metallic layer with a hafnium oxide patch to avoid short circuits with the second metallic layer.
7. Definition and evaporation of the second layer of fine gates.
8. Patterning of metallic connections between the fine structure and the bonding pads.

First, we get rid of the 2DEG everywhere on the wafer except where it is needed : in the central part of the device where the quantum dots are formed, and current paths from one ohmic contact to another to perform transport measurements. The mesa's patterning isolates each device on the wafer electrically and limits the amount of cross-capacitance via the 2DEG. In order to etch only outside of the mesa defined in Fig. 2.2(a), we pattern a 400 nm thick resist mask (photosensitive resist S1805) at the surface of the heterostructure via laser lithography. The surface of the sample is etched with a solution of H_2O_2/H_3PO_4 whose etching rate has been calibrated beforehand. The resist mask is removed using acetone and the sample surface is rinsed and dried.

The next step is to create ohmic contacts to connect the 2DEG 90 nm below the sample surface to bonding pads. The pads are imprinted on a resist mask with laser lithography before deposing a 300 nm stack of Ni/Ge/Au/Ni/Au. The metals are deposited in one trip inside an ultra-high vacuum chamber with the different crucibles heated by an electron beam. The metal is uniformly deposited on the resist surface and on the crystal surface inside the resist trenches. The excess metal is removed by *lift-off*, and leaves only the ohmic contacts. This step consists of removing the resist with an acetone bath so that only the metal in direct contact with the crystal stays on the sample surface. Next, the sample is annealed 1 min at 450 °C to diffuse the Germanium and Nickel into the crystal and form an alloy. Thus, we obtain ohmic contacts with low contact resistance $R_c =\sim 400\,\Omega$. It is important to perform sensitive electrical transport experiments [Iqb20].

Then, we depose a layer of 15 nm thick hafnium oxide HfO_2 with atomic-layer deposition (ALD) on all the sample surface. The hafnium oxide is a high-κ dielectric that will prevent the formation of Schottky barrier between the 2DEG and the metallic gates, allowing for positive and negative polarizations. This layer has been benchmarked for electric field up to $E \sim 4.7 \times 10^8\,\mathrm{V\,m^{-1}}$ using additional test structures. It corresponds to a difference of $\pm 7\,\mathrm{V}$ applied between the bottom and upper fine structure layers.

Next, two kinds of alignment marks are deposited in a single step, using the same laser lithography - metal deposition - liftoff cycle process. The first set of marks permits a sub-micron alignment of the different laser lithographies and to perform rough localization on the sample. A second set is deposited directly on the mesa, near the fine pattern. These additional marks are used to align the two electron-lithography layers with a precision below 10 nm. The alignment marks consist of a 20 nm thick titanium sticking layer, topped with 100 nm of gold.

A first fine structure layer made of 4 nm Ti / 11 nm Au is deposited using an electron beam lithography defined resist mask. For each electron beam lithography, we use a 70 nm thick poly(methyl methacrylate) (PMMA) resist layer. Once the liftoff is performed, we pattern a $\sim 100 \times 100\,\mu\mathrm{m}$ patch of 15 nm-thick hafnium oxide on top of the fine central part to depose the second metallic gate layers without short circuits. It does not completely recover the first electron beam layer, so we will be able to contact it to the bonding pads later on. The upper metallic gate layer is deposited using the same method than the bottom one.

Finally, we connect all the fine gates to bonding pads with a laser lithography cycle and cut the sample into smaller 3 mm × 3 mm pieces that contain one device each with a diamond-tip scriber.

Potential simulations

In order to guide the device design, we use Comsol© as a Poisson solver to compute the electric potential at the 2DEG level. In the simulation, we import the device gate geometry including the two metal layers, the hafnium oxide and the GaAs/AlGaAs heterostructure. We assume the 2DEG depleted. This hypothesis gives a good approximation of the dots' electrostatic potential far from the electron reservoirs where electron-electron interactions would smooth the barriers' potential. Such calculations do not predict the dot occupancies and their tunnel couplings for specific gate voltages. Nevertheless, they give the position of the dots qualitatively and help to tune the device by giving a rough idea of the potential landscape.

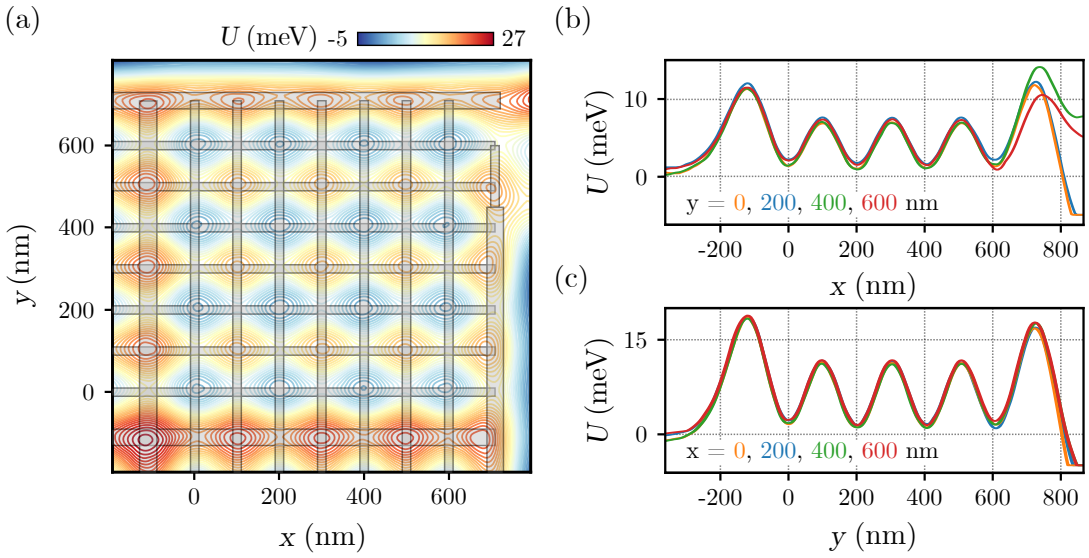

Figure 2.3: **(a)** Comsol© simulation of the electrostatic energy landscape induced by the gate electrodes. All the gate electrodes are biased at $-700\,\mathrm{mV}$, except the plungers which are grounded. We observe a minima in the landscape at the crossing of each plunger gates. **(b)** Horizontal and **(c)** vertical cuts in the electrostatic energy along the different rows/columns of quantum-dots. As expected, the potential is uniform for each QD at the center of the array, but it is not true at the array boundaries due to finite size effects. In order to align the chemical potential of each dot, the gate voltages must compensate for the differences.

In Figure 2.3, we confirm that this structure has the potential to form an array of 4x4 potential minimums that will hold quantum-dots. The array is biased with the same voltage applied on each barrier gates. We see that the outer dots, close to the array's boundaries, have a higher potential than the 4 central dots. The thicker outer gates used to isolate the array from the rest of the 2DEG explain this asymmetry. It could have been corrected by increasing the size of the dot located on the edges but we choose to preserve a uniform dot spacing. Consequently, due to the finite size of the array, the tuning of the gate voltages must compensate for the higher potential at the array boundaries.

2.3.2 Silicon nanowire

This thesis's second platform consists of silicon transistor-like nanostructures, as depicted in Fig. 2.4. An intrinsic silicon channel is connected at both ends with metallic reservoirs and accumulation gates are deposited on top of the nanowire to create and control an array of quantum dots. The devices are fabricated at the CEA-LETI on an industry-standard fabrication line.

In this part, we detail the fabrication process developed at the CEA-LETI and the potential simulations used to understand the sample dynamics.

Fabrication process

The devices are fabricated on 300 mm Silicon-On-Insulator (SOI) substrates with a buried oxide thickness of 145 nm (Fig. 2.4(b)). The top 11 nm-thick silicon layer is patterned with a electron-beam lithography - etching cycle to form the nanowire (width $W = 70$ nm to 110 nm). Next, the gate stack is made of 6 nm thermally grown SiO_2, 5 nm ALD-deposited TiN, 50 nm of Poly-Si, and topped by a bilayer hard mask 30 nm SiN and 25 nm SiO_2 (Fig. 2.4(c)). The gates are defined by multiple lithography-etch cycles, using both deep-UV and electron-beam lithography. The hard mask role is to cover the gates during the etch cycles and is removed at the end.

The resulting structure consists of 4 pairs of split gates along a silicon nanowire channel of rectangular cross-section, each overlapping opposite edges of the mesa (labeled from 1 to 8 in Fig. 2.4(e)). The gate pitch along the nanowire direction is 80 nm (gate width $W = 40$ nm, spaced by $S_{\mathrm{H}} = 40$ nm), and the split width is $S_{\mathrm{V}} = 40$ nm. The n-doped areas are defined in a self-aligned way, outside regions covered by the gates and an offset spacer. Thus, a particularly wide (35 nm) Si_3N_4 offset spacer was deposited, completely covering the inter-gate spacings (Fig. 2.4(b)), to protect the intrinsic silicon nanowire from accidental doping. The Si areas still exposed were regrown employing epitaxy, before undergoing ion implantation of n-type dopants activated by a N_2 spike anneal. These regions form the electron reservoirs, labeled S and D (source and drain) in the figures by analogy with classical MOS devices. Following these steps, the wafers are then sent to a *back-end* process that encapsulates the devices and defines bonding pads.

At room temperature, the 4 split-gate silicon devices act like field-effect transistors, and source-drain current is turned ON when we apply gate voltages above a given threshold (see Appendix A). Thus, pre-screening is achieved by discarding the devices exhibiting abnormal characteristics (e.g. voltage thresholds, saturation currents) or leaking gates directly from room temperature characterizations.

Potential simulations

In Section 1.2.3, we discussed the formation of quantum dots at dilution temperatures in the corner of the nanowire when a positive voltage is applied on a single split-gate. To understand the operation of our 4 split-gate devices, Yann-Michel Niquet (CEA-IRIG in Grenoble) developed numerical simulations to compute the carrier density in the nanowire.

The simulations rely on a self-consistent Thomas-Fermi approximation to take into account the electron-electron interactions on the carrier density. Compare to the GaAs potential landscape simulations, we are dealing with a rapidly varying accumulation

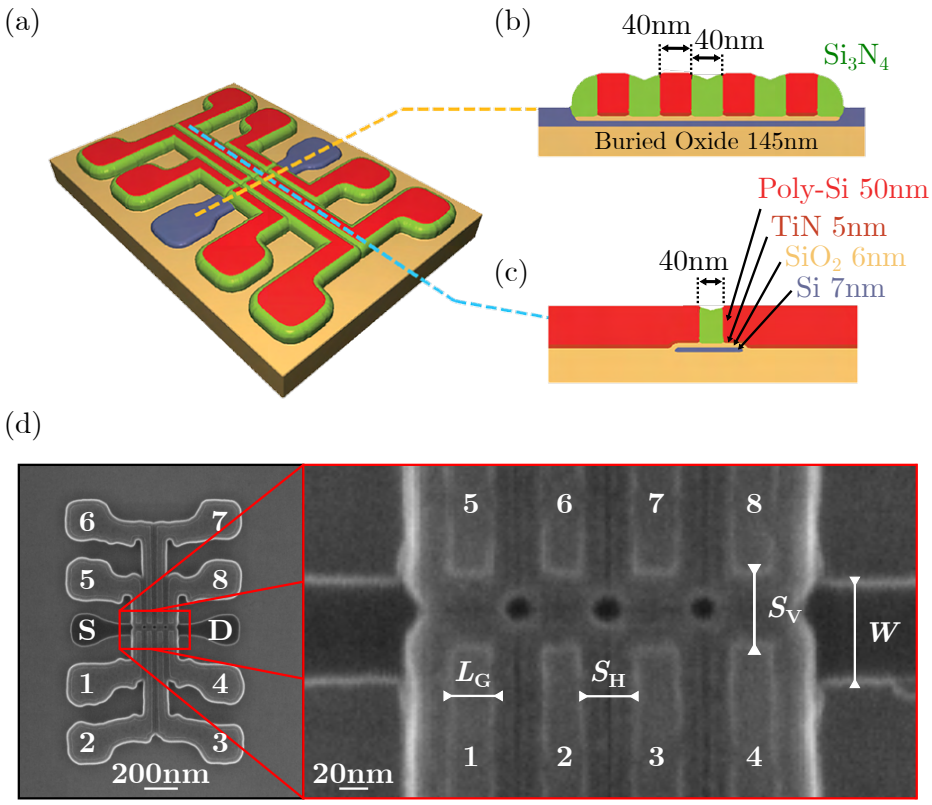

Figure 2.4: Silicon split-gate device. (a) Schematic of the 2x4 QD array silicon device. The silicon nanowire (blue) is covered with top gates (red), which are separated by spacers (green). The non-covered regions of the nanowire are highly doped to form electron reservoirs. **(b)** Cross-section along the nanowire. **(c)** Cross-section perpendicular to the nanowire, along one top gate. **(d)(Left panel)** SEM micrograph of a device similar to the one used in the present thesis. The source (S) and drain (D) contacts are labeled, as well as the quantum-dots (QD1 to QD8) and their associated electrodes (V_1 to V_8). **(Right panel)** Zoom into the central part of the device with the split-gates deposited on top of the horizontal silicon nanowire. The nanowire width is labelled W, the gate width L_G, the gate horizontal spacing S_H and vertical S_V.

potential, notably due to the limited distance between the dots and the gate electrodes. Thus, the potential landscape does not catch properly the size and shape of the dots. The source and drain contacts are assumed doped with $N_d = 10^{20}$ phosphorous per cm^3, whose ionization probabilities are calculated with an incomplete ionization model valid at low temperature [Alt06]. The density of electrons at a position r in the nanowire is given by

$$n(r) = N_c F_{1/2}[(E_c - eV(r) - \mu)/(kT)], \tag{2.1}$$

where $V(r)$ is the local potential, which includes the mean-field contribution from the ionized impurities and electrons themselves. Additionally, $F_{1/2}$ is the Fermi integral, N_c and E_c are the effective density of states and conduction band energy in bulk silicon, and μ

is the chemical potential. The calculations are run at temperature $T = 20\,\mathrm{K}$ for numerical convenience. Although the Thomas-Fermi approximation does not consider quantum effects such as confinement and tunneling, it is expected to give a fair account of the position of the dots and transport channels in the system.

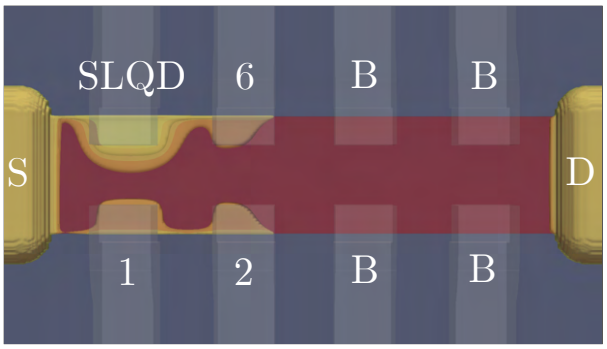

Figure 2.5: Electron density simulations. The density of electrons inside the nanowire is computed for $V_1 = 1.2\,\mathrm{V}$ and $V_1 = V_2 = V_6 = 300\,\mathrm{mV}$. The color code corresponds to 3 different iso-density of arbitrary values. The simulation is used to give an insight into the QD localizations for a given voltage configuration.

Nevertheless, we can compute the electron density inside the channel for polarization conditions similar to these studied in chapter 3. In figure 2.5, a large positive voltage ($> 1\,\mathrm{V}$) is applied on gate 5 to form a single-lead quantum dot electrometer and gate 1, 2, and 6 are biased in the few-electron regime at $\sim 300\,\mathrm{mV}$. A large dot is formed under the SLQD gate and affects the QD potential of QD1, 2 and 6. Additionally, we see that the electron density does not vanish along the nanowire for both sides. At the opposite, in the transverse direction, the dot remains fairly localized under each gate. In consequence, we expect qualitatively from this simulation that the inter-dot coupling is stronger for a double quantum dot located along the nanowire (e.g: QD1 and QD2) than in a configuration across the channel (e.g.: QD2 and QD6).

2.4 Electronics

Using the dilution refrigerator detailed previously, we can cooldown a sample at 70 mK, but we still need to detail the electronics used to control and measure such a device.

At this end, the sample under test is glued to a printed circuit board (PCB). Once the sample is wire-bonded to the board, we place the PCB at the end of the cold finger connecting all the device's pads to the refrigerator *DC wiring*. Also, the PCB embed mini-SMP connectors and surface-mounted-devices that we use to build a LC resonant circuit for gate reflectometry sensing, which is probed through a dedicated high-bandwidth *AC wiring*.

We first discuss the different refrigerator wirings installed to connect the sample to room-temperature electronics. Then, we focus on these electronics used to create and control quantum dots. Finally, we detail the whole setup performing gate reflectometry.

2.4.1 Wiring of electrical connections

The first step is to connect all the device pads to room-temperature electronics. In particular, the different samples studied in this thesis required from 10 to 40 electrical connections from room temperature down to the sample at 70 mK. These connections have different requirements in terms of bandwidth and features. Additionally, the heat brought by this wiring must be kept as low as possible. Indeed, the sample's electron temperature can significantly exceed the mixing chamber temperature due to the wiring heat and insufficient thermal contact. Thus, different wires and materials are used to satisfy both bandwidth and heat budget, depending on the line.

Here, we detail the different solutions used for the DC wiring, before discussing the large bandwidth AC wiring.

DC wiring

One way to connect a wire from room-temperature to the sample at 70 mK is to thermally anchor the wire at the different refrigerator stages that act as heat sinks, and to filter the wire's noise spectrum continuously . Indeed, the amount of heat brought by the wire's white noise is limited by its bandwidth and temperature. We discuss two implementations of this strategy: a first one consisting of limiting the wire's bandwidth, and the second one in attenuating regularly the wire's signal.

First, the ohmic contacts and some gates required only to be operated on a ms-timescale. These lines are Constantan wires, a copper-nickel alloy known for the low variation of its resistivity with temperature. We packed 30 Constantan lines altogether in a CuNi capillary with a diameter of 3 mm. The capillary is then filled with Ecosorb®, a powder containing magnetic particles, that acts as a low-pass filter. Once installed in the dilution refrigerator, the capillary is thermally anchored to the different fridge stages. It results in 30 lines from room temperature to the PCB with a DC to 10 MHz bandwidth, contained in a small capillary. Such a dense packaging implies non-negligible crosstalk between the Constanan wires that we can neglect for sub-MHz manipulation like constant voltage generation and recovering current from the mesa.

However, most of the gates have to be addressed at microsecond timescales with limited crosstalk. For example, in Sec. 4.2, we detail an electron loading pulse sequence where important crosstalk would affect the number of electrons loaded. For these lines, we installed 20 individual Thermocoax® coaxial wires. They exhibit a low-pass filter behavior with a $\sim$ 100 MHz cut-off frequency. In order to maximize both filtering and thermal resistance, we maximize the wire length in the fridge by winding the wires around Teflon tubes. At the opposite, the thermal resistance needs to be as low as possible between the mixing chamber and the PCB. This is achieved by the use of copper/stainless steel coaxial wires. The interfaces between these wires are 3.5 mm diameter mini-SMP connectors. In consequence, the important footprint and number of critical welds make this solution impracticable for all the 40 fridge lines.

AC wiring

In Section 1.3.2, we discussed the principles of gate-reflectometry charge sensing. This technique relies on the ability to probe a resonant circuit located at 70 mK whose central

frequency can range from few tens of MHz to 1 GHz. It appears that the previous DC-wiring cannot fit this bandwidth requirement without bringing excessive heat and noise directly to the sample.

To conserve a large bandwidth with reduced noise, the solution adopted here consists of using large-band attenuators to reduce the signal amplitude as we go down in temperature. Indeed, the attenuators reduce signal and noise level and thermally anchor the inner conductor efficiently . Therefore, while the signal amplitude decreases, the noise level is kept at the noise temperature of the associated stage. In our setup, attenuators located at the 4 K and 70 mK-stages interrupt high-bandwidth lines. The RF-wires are made of silver-plated stainless steel, and we use attenuators from XMA corporation® working at dilution temperatures. Thus, the attenuation levels balance the tradeoff between the noise and the maximum signal amplitude brought to the sample.

2.4.2 Control and acquisition electronics

In addition to the well isolated and filtered wiring detailed previously, we also need a room temperature control electronics and a data acquisition scheme. We detail here the apparatus used to apply arbitrary voltages, perform data acquisition, and transport measurements. The reflectometry setup to perform gate-reflectometry is investigated in the next section.

Digital-to-Analog converters

First of all, our experiments rely extensively on the generation of voltages to form and manipulate quantum dots. To this end, we use homemade 16-bit digital-to-analog converter boards (DACs) that exhibits a fast slew rate $\mathrm{SR} \simeq 2.5\,\mathrm{V\,\mu s^{-1}}$, while keeping a low noise level figure of $25\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The DAC output full voltage range is $\pm 5\,\mathrm{V}$, which results in a voltage resolution of $153\,\mu\mathrm{V}$. Each DAC board embeds 8 different outputs and we use an assembly of 4 DAC boards in this thesis. These boards are controlled by a sbRIO-9208 field-programmable gate array (FPGA) from National Instruments©. The different waveforms to apply on each DAC output are programmed in the FPGA memory before an experiment in a $\sim$ ms timescale. Up to approximately 3000 instructions can be encoded in the FPGA memory with a minimum setting time of $16\,\mu\mathrm{s}$ when a voltage order is set. Thanks to the flexibility and the low noise figure of this instrument, we can easily perform experiments where both fast (e.g. µs electron loading) and slow timescales (e.g. ms charge readout) are needed.

Acquisition board

In order to acquire the signal generated by the experiment, we use an AlazarTech© ATS460 digitizer. The card has 2 input channels sampled at 125 MHz with a 14-bit resolution. We developed a driver that benefits from the board dual-port memory to stream the data acquired to the host computer. Moreover, the acquisition can be triggered externally by the same FPGA used to control the DACs.

Transport measurements

Finally, the ability to measure the current flowing through two ohmic contacts is an essential tool to characterize our devices and to form SET detectors (see Sec. 1.3.1). This is achieved with the use of homemade IV converters with variable gain from 10^6 to $10^9\,\mathrm{V\,A^{-1}}$. For an

amplification of $10^7\,\mathrm{V\,A^{-1}}$, they have a rise time of 100 µs, which is compatible with the Constantan bandwidth.

2.4.3 Reflectometry setup

In addition to the previous voltage control and data-acquisition that rely on the DC wiring, the AC wiring allows us to build an electrometer out of a single-lead quantum dot by probing the electrode-dot quantum capacitance with the use of a resonant circuit (see Sec. 1.3.2). One advantage of this scheme is the possibility to probe many SLQDs using only one input and one output AC line wired into the dilution refrigerator. The frequency multiplexing applies as long as the resonances from the different resonant circuits / SLQDs are resolved individually. We detail here the reflectometry setup used to probe up to 2 resonant circuits $\mathrm{LC^a}$ and $\mathrm{LC^b}$ simultaneously, as shown in Fig 2.6. Since the room-temperature apparatus is identical for both SLQDs and that the refrigerator part is common, we focus on $\mathrm{LC^a}$ and highlight only the differences with $\mathrm{LC^b}$.

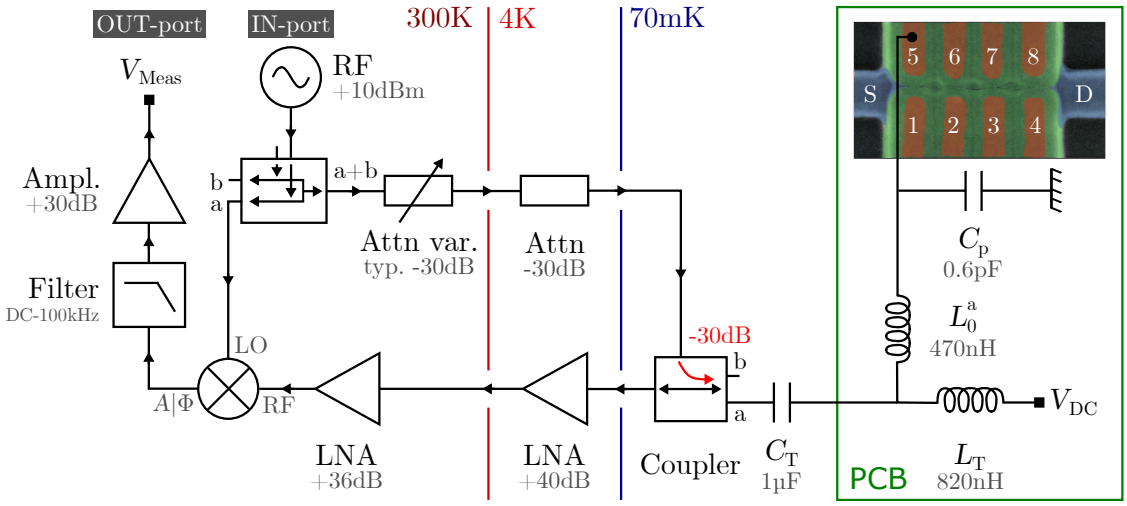

Figure 2.6: Gate RF-reflectometry setup. Diagram of the reflectometry setup to probe the resonator $\mathrm{LC^a}$ on the PCB. A RF tone is generated and sent to a homemade splitter/adder at the setup's IN-port. One half of the RF power goes to the resonator located in the dilution refrigerator at the 70 mK stage. First, it goes through a voltage-controlled attenuator at room-temperature and a fixed one at the 4 K plate, before being injected into the directional coupler. The coupler has two ports, one for each resonant circuit. The resonant circuit is connected via a bias-tee with a capacitance C_{T} for the AC port, and an inductor L_{T} for the DC port. The signal reflected at the $\mathrm{LC^a}$ resonator passes through the directional coupler and is amplified before a demodulation step by comparison with the second half of the original RF tone. The demodulator codes either the amplitude or the phase difference between these two signals, and a filter in addition to a final amplification stage makes it possible to measure the V_{Meas} voltage at the OUT-port of the setup. An additional resonant circuit $\mathrm{LC^b}$ can be probed at the same time using the multiplexed part of the circuit (splitter, fridge wiring).

First, we generate a RF tone around the circuit resonant frequency $f_0^{\mathrm{a}} \simeq 286.1\,\mathrm{MHz}$ ($f_0^{\mathrm{b}} \simeq 236.0\,\mathrm{MHz}$) using a Rhode&Schwarz© SMB100A signal generator with a 10 dBm power output. This signal is split into one reference signal going to the mixer, and the

carrier injected into the refrigerator AC input. To do so, we use a homemade splitter to sum the two carriers f_0^{a} and f_0^{b} for the AC input, and generate the two mixer reference signals. Furthermore, a voltage-controlled attenuator IDT® F2250NLGK allows tuning the summed signal power at the AC input, without affecting the mixers reference amplitude. The signal is further attenuated by 30 dB at the refrigerator 4 K-stage.

The input signal channel is then connected to the −30 dB input of a homemade directional coupler anchored at the mixing chamber. The directional coupler's output is split into two channels, one wire from the directional coupler to the PCB for each resonant circuit. A typical value of the power sent to the device is estimated to be around −100 dBm. It is worth noting that this additional splitting can be achieved on-chip directly in lithographed resonant circuits [Hor14].

The resonant circuits consist of surface-mounted inductors $L_0^{\mathrm{a}} = 470\,\mathrm{nH}$ and $L_0^{\mathrm{b}} = 820\,\mathrm{nH}$ soldered directly on the PCB and wire-bonded to a gate. It forms LC-circuits with the gate-dot capacitance $C_0 \simeq 0.02\,\mathrm{pF}$ (typical value) and the parasitic capacitance to ground $C_{\mathrm{p}} \simeq 0.6\,\mathrm{pF}$. The parasitic capacitance arises from the PCB and the bonding pads on the sample. Further developments, including the developments of on-chip inductors, are needed to reduce as much as possible the parasitic capacitance in order to maximize the SLQD phase response $\Delta\Phi \propto C_{\mathrm{Q}}/C_{\mathrm{p}}$ (Eq. 1.20). To allows DC biasing of the gate, we connect the tank circuit to a bias-T composed of a $C_{\mathrm{T}} = 1\,\mu\mathrm{F}$ capacitor (AC branch), and an inductor $L_{\mathrm{T}} = 820\,\mathrm{nH}$ (DC branch). Then, SMP connectors connect the resonant circuits to the AC wires.

Finally, the signal reflected on each resonant circuit goes back through the directional coupler. It is amplified by 30 dB with a low-noise amplifier CITLF1 from the Caltech Radiometer Group, anchored at the 4K-stage. Then, it is again amplified by 36 dB at room temperature using two MiniCircuits® ZX60-33LN-S+. Afterward, the signal is split between the two mixers AD8302 whom, with the reference signal, allows to obtain both the gain and phase difference. The phase output is filtered and amplified by an additional 18 dB homemade amplifier before digitalization.

The full reflectometry setup is resumed in Fig. 2.6. It allows us to probe the phase response of 2 resonant circuits down to 70 mK. In this context, we show in Fig. 2.7 the amplitude response of both resonant circuits before the mixers. We obtain two resonances with central frequencies $f_0^{\mathrm{a}} \simeq 286.1\,\mathrm{MHz}$ and $f_0^{\mathrm{b}} \simeq 236.0\,\mathrm{MHz}$ and quality factors $Q^{\mathrm{a}} \simeq 49$ and $Q^{\mathrm{b}} \simeq 11$. In Chapter 3, we use LC^{a} to build a SLQD detector and measure the charge occupancy of its next neighbor QDs.

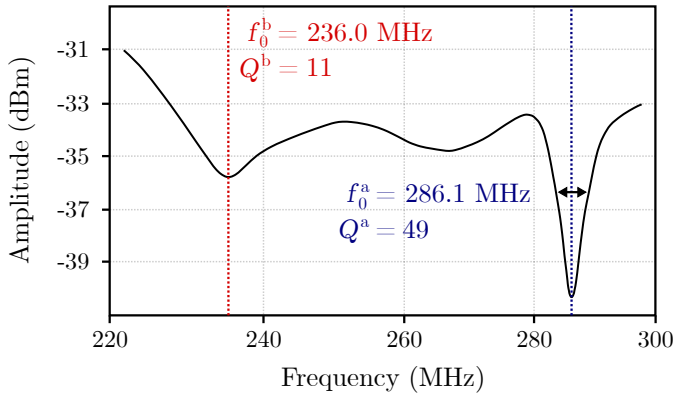

Figure 2.7: VNA response of the LC resonant circuits at 70 mK. The amplitude response of a Vector-Network-Analyser (VNA) is plotted as a function of the probe frequency. We see two peaks, each associated with a resonant circuit. For LC^a (blue dashed line), we get a center frequency $f_0^a = 286.1$ MHz and a quality factor $Q^a = 49$. For LC^b (red dashed line), we obtain a center frequency $f_0^b = 236.0$ MHz and a quality factor $Q^a = 11$.

2.5 Measurement software

The electronics described in the previous section are the hardware side of our quantum experiments. Here, we present the measurement software programming the electronics, retrieving the experimental data, and analyzing the results. The control of an experiment is summed up in three stages : (i) definition, (ii) execution, and (iii) analysis. To carry out these tasks, every laboratory relies either on homemade software or on commercial solutions. The softwares offers a high-level programming language to configure the hardware for an experiment. One of the advantages of these programming languages is their hardware agnosticism. For example, an experimentalist can use different instruments without knowing the contents of the packets sent via TCP/IP to program them. Additional features can be incorporated, such as customizable software limits on the instrument outputs to match the physical limitations of the device under test. However, the programming language limits the type of experiments possible to that built into its functionalities. In this context, measurement frameworks dedicated to quantum experiments have been developed in the last few years like Labber [Lab20] and QCoDeS [QCo20].

In this section, we first discuss the measurement software used in the group at the start of my thesis. We will focus on the specifics of this software, the experiments it enables, and our hardware's functionalities. Then, we describe the application redesign with the addition of new features such as a slow feedback loop, that I have performed with Pierre-André Mortemousque, a research engineer at CEA-LETI.

2.5.1 Software requirements

At the beginning of my thesis, the group's measurement software was an in-house suite of three different applications, as depicted in Fig. 2.8(a).

First, the experiments are defined using a graphical user interface (GUI) programmed in Python. This interface permits the user to select which instruments to be used and their configurations. The experiment consists of an N-dimensional map where any instrument

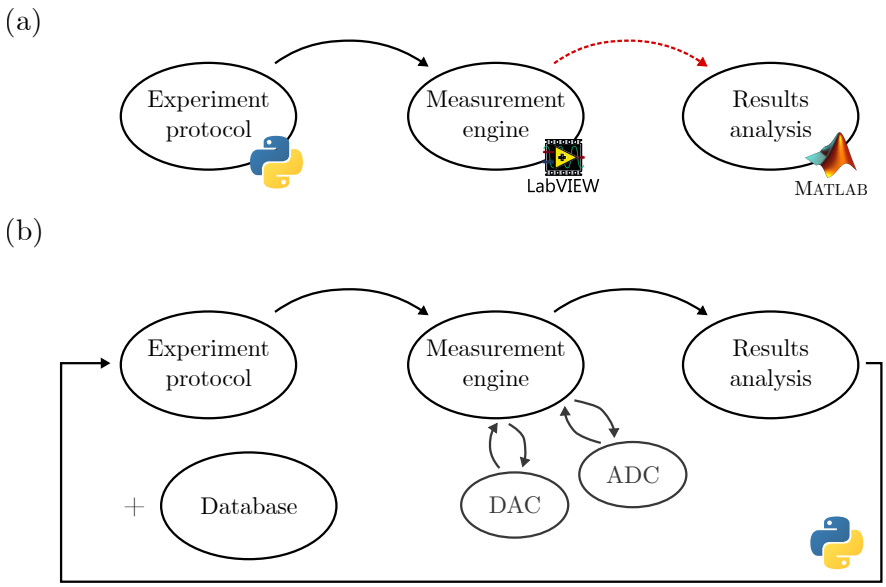

Figure 2.8: Software architecture. (a) Schematic of the previous measurement software architecture. First, an experiment is defined via a Python graphical user interface. Then, the experiment is sent to a measurement engine developed in LabVIEW. Finally, once the experiment has been completed, the user manually look at the results and perform advanced analysis with a Matlab program. **(b)** Updated schematic. The measurement software is developed with a unique programming language, Python. The different stages of an experiment are better interconnected. In particular, a feedback loop is possible from one experiment to another. Moreover, a database stores all the information about experiments: this is the starting point for long-term analysis, such as monitoring device aging.

parameter can be swept along the different axis.

Next, the recipe is sent to the measurement engine in charge of executing the experiments and communicating with the instruments. It is a complicated monolithic LabVIEW object that includes smaller components for the different hardware drivers. A batch list is present in the engine so that the user can program several experiments in advance. Now, the typical communication time between the computer hosting the measurement engine and a remote instrument is of the order of a few milliseconds. It means that we cannot refresh the voltages applied on a device at a higher rate. To overcome this problem, we need to program the compatible instruments beforehand and then trigger their executions at the start of the experiment. It is usually the case for arbitrary waveform generators such as our homemade DACs, or data acquisition systems. Instruments without internal memory are reprogrammed after each shot if necessary.

Finally, once the experiment is complete and the raw data saved, the measurement engine stops and starts the next experiment in the queue. The results are analyzed using another software, this time programmed with Matlab. The role of the analysis software is to transform the raw data into relevant quantities defined with personalized user scripts and facilitate the generation of plots. However, the analysis is not automatically triggered after the end of an experiment but is opened manually by the experimenter. Moreover,

there is no connection between the analysis and the definition of a new experiment. Each run is independent, and it is up to the user to apply feedback based on previous analysis.

2.5.2 Application overhaul

During my thesis, I worked on a complete overhaul of the measurement software, motivated by several aspects.

To begin with, the plethora of programming languages (Python, Matlab, LabVIEW) makes the entire software extremely difficult to maintain. In particular, LabVIEW applications are not compatible with compulsory version control systems as git, and laborious to integrate into a collaborative development environment. Furthermore, adding new features takes time and requires modifying each sub-part with its own language and specificities. Finally, the three sub-software are not fully interconnected with each other, and several operations are performed manually (start of analysis, feedback). Overall, the software suite relies extensively on graphical interfaces, which limit the range of capabilities and are time-consuming.

The new measurement software takes these drawbacks into account in the application's architecture, as shown on the block diagram in Fig. 2.8(b). It is wholly programmed with Python and recreates the previous applications in a unified framework with additional functionalities.

First, a new experimentation programming language has been developed. Compare to the previous one, it is a script-based language, not limited to the realization of N-dimensional maps but adapted to arbitrary schemes. It is tightly linked to a database storing all information from the experiments in their current states (defined, running, executed, analysis details). We can access information about a previous experiment such as retrieving a set of gate voltage values or any experiment results. So, this system makes it possible to have feedback from one experiment to another, with for example the automated tuning of an electrometer (see Sec. 4.2.1). It can also monitor the characteristics of a sample in the long-term by a survey of the physical parameters contained in the experiments over time.

Next, a measurement engine was developed to pre-program the instruments and handle their executions. The drivers controlling the different instruments follow simple templates developed in Python, depending on the type of instrument (actuator, acquisition, ...). Once an experiment is complete, all of its data are stored in the database, and an order is sent to the analyser.

Finally, the analyzer has the same functionalities as the previous one developed in Matlab, but is directly integrated into the application flow. The results of an analysis can be immediately injected as inputs for a new experiment. We note that the time required to perform a feedback ((i) analyse experiment A, (ii) inject values from A into a new experiment B, (iii) start B execution) is of the order of ~ 1 second. We qualify this feedback as *slow* since it is slower than our measurement bandwidth of $\sim 1\,\mathrm{kHz}$ and does not enable real-time feedback.

To summarize, we have developed a measurement software to perform the quantum experiments described in this thesis. The improvements of this application, compared to what existed at the start of my work, have been beneficial in the following chapters' experiments . In particular, the feedback loop allowed measurements that would not have

been possible with the previous application. Now, the development of the program has been performed in parallel with the experimental work. Especially, all the functionalities were not available during the silicon nanowire operation in Chapter 3. Nevertheless, developments continue with integrating new homemade instruments, new features, and an improved experiment programming language.

CHAPTER 3

Charge detection of next-neighbor dots in a silicon nanowire

3.1 Introduction

The silicon platform has been identified as a good candidate for large scale quantum computing using single electron spins in lithographically defined quantum dots. The long coherence time of electron spins in isotopically enriched silicon associated with improved control of coherent manipulation has resulted in high-fidelity single and two-qubit gates [Hua19; Wat18; Yon18; Zaj18]. Additionally, spin readout with high-fidelity in short timescale has been achieved using embedded detectors [Urd19; Wes19; Zhe19]. Following that progress, the next milestone is the coherent operation and readout of these spin qubits in nearest-neighbor tunnel-coupled 2D arrays, while preserving the same performances. Here, we use devices produced on industrial lines to improve the yield and permit large-scale control.

Towards this goal, we study here an array of 2x2 MOS quantum dots where each QD is operated with a single gate electrode. First, we demonstrate an SLQD electrometer's operation by probing with radiofrequency reflectometry a QD at one end of the array. This method allows us to get rid of a proximal charge sensor whose footprint can be similar to the qubits array itself and is compatible with a large-scale architecture [Hou16]. We use this detector to probe single QDs and record single-shot charge tunneling events to benchmark its charge sensitivity.

In a second time, we probe the charge stability and dynamics of the different double quantum dot configurations of the QD array and its Coulomb disorder. However, due to the device's tight geometry, the detector is strongly capacitively coupled to all the different gates used to control the array. In consequence, the detection range of the SLQD is limited to only a few charge transitions. We quantify this capacitive coupling and develop different schemes to probe the QD array electron occupancy from the many-electron to the few-electron regime.

3.2 Single-dot measurements

In this part, we use a single-lead quantum dot electrometer to probe the properties of the next neighbor quantum dots located along or across the nanowire. We begin by studying the electron filling of a single dot and its coupling to a reservoir. Then, we focus on a given charge transition and extract the charge sensitivity of our SLQD detector.

3.2.1 Single-lead quantum dot

In the following, we use the QD5 to form a single-lead quantum dot electrometer at the left end of the array, as discussed in section 2.4.3. However, the detector sensitivity is limited at its next-neighbor quantum dots due to the metallic gates screening. Thus, we focus on the 2x2 sub-array depicted in Fig. 3.1(a) inset, and we set the remaining gates to 0 V to decouple the array from the drain reservoir. We re-label QD5 as SLQD to distinguish it from the probed QDs (QD1, QD2, and QD6).

Detection protocol

In Figure 3.1(a), we plot the phase response of the reflectometry setup as a function of the voltage V_{SLQD} applied to the SLQD (QD1) to sweep its chemical potential. A constant phase response is observed except when a quantum capacitance's contribution occurs due to an SLQD chemical level's alignment with the source lead. We extract a peak linewidth $lw = 1.7\,\mathrm{mV}$ and a maximum phase shift on the top of the coulomb peak $\Delta\Phi \sim 1.1\,\mathrm{mrad}$. Using Eq. 1.20, we obtain a maximum quantum capacitance $C_{\mathrm{Q}} = 6.7\,\mathrm{aF}$ for the peak shown. As we will discuss in Section 3.3, there is a tradeoff between the detection range given by the SLQD linewidth and the signal strength with the peak height. Here, the peak linewidth is deliberately broadened to increase the SLQD range by applying a strong reflectometry tone power.

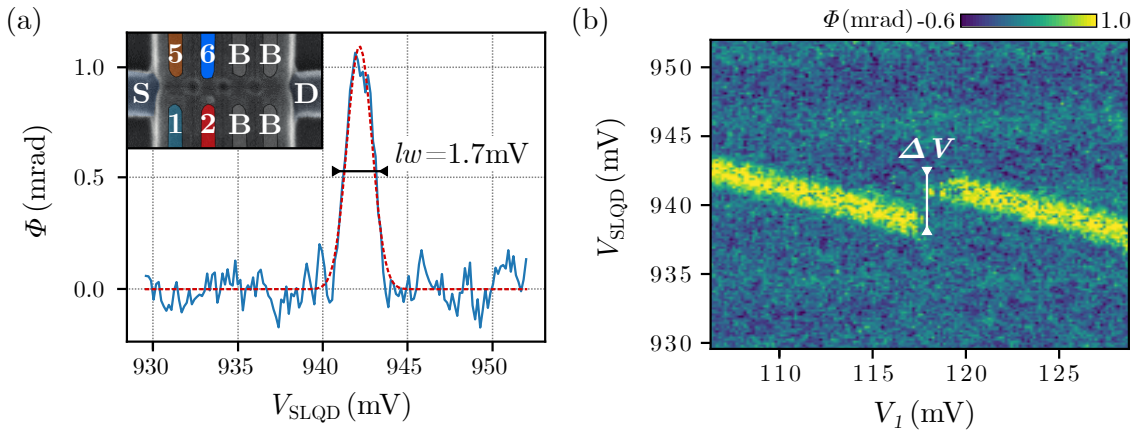

Figure 3.1: SLQD stability diagram. (a) Phase response of the reflectometry setup versus SLQD voltage V_{SLQD} (solid blue line). The phase response peaks when a SLQD energy level is aligned with the source lead. We extract the peak's linewidth $lw = 1.7\,\mathrm{mV}$ and height $\Delta\Phi \sim 1.1\,\mathrm{mrad}$ from a Gaussian fit (red dotted line). **(inset)** False color SEM micrograph of the corresponding QDs configuration. B stands for barrier gates where the voltage is set to 0 V. **(b)** The phase change of the resonant circuit is plotted as a function of V_{SLQD} and V_1. The signal line corresponds to the electrometer dot's charge degeneracy, which experiences a shift in voltage for one electron added to QD1. The voltage shift corresponds to $\Delta V = 1.9\,lw$.

The phase response of the reflectometry setup for different values of V_{SLQD} and V_1 is shown in a so-called *stability diagram* in Fig. 3.1(b). Recording the peak position for different electrostatic environments, here stepping V_1 along the x-axis, allows us to highlight two phenomena. First, there is a cross-capacitive coupling between all the metallic gates (V_{SLQD}, V_1, V_2, V_6) and all the quantum dots (SLQD, QD1, QD2, QD6). We will study

this coupling quantitatively for different detector-dot configurations in the next section. Second, for a specific value $V_1 \approx 118\,\mathrm{mV}$, the detector peak position undergo an abrupt voltage shift $\Delta V = 1.9\,lw$. Such a shift is associated with adding one charge into QD1, while its charge occupancy remains constant between two shifts.

Dot filling

Figure 3.2(a) shows an extended charge stability diagram where the filling of QD1 up to 6 electrons is observed. Several coulomb peaks from the SLQD are used to monitor the QD1 charge occupancy. As discussed in Section 1.2, increasing the number of electrons in a QD leads to higher-energy orbitals' occupation and thus to a QD wavefunction of greater extent. Consequently, the QD tunnel-coupling with its environment can change drastically with the QD occupation. This effect is visible on the bottom left of the diagram, where a fainted coulomb peak (black dashed line) is associated with a reduction of the SLQD-lead coupling leading the SLQD to leave the regime described in Sec. 1.3.2. Since we cannot control the SLQD-lead coupling independently of the SLQD chemical potential, we cannot count the absolute number of electrons inside the SLQD. However, it is not the case for the neighbor dots where we can use the SLQD peak shifts as an electrometer to count the dot occupation.

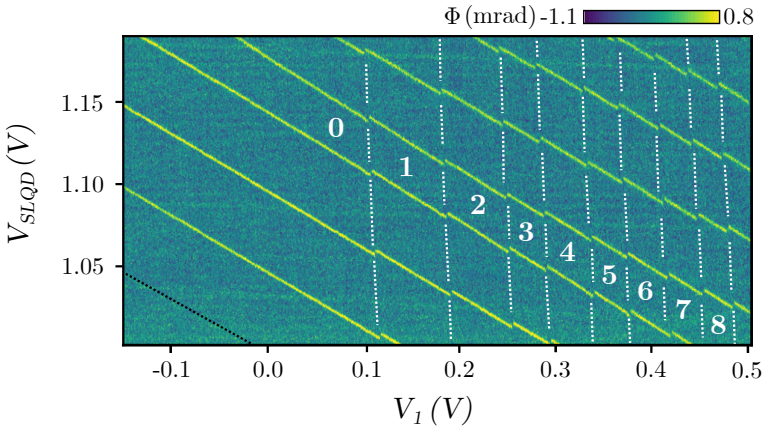

Figure 3.2: Extended stability diagram. Several SLQD peaks are used as electrometers to probe the QD1 occupation. The lack of phase shift below $V_1 \lesssim 0.1\,\mathrm{V}$, while the electrometer remains sensitive, indicates that the QD1 is empty. So, we can count the QD1 occupation (white labels) after each SLQD jump (dashed lines). It is not the case for the SLQD occupation: the detector response vanishes when we decrease the SLQD chemical potential like for the dotted black line (see main text).

From this extended stability diagram, we can extract the addition energy spectrum of QD1 introduced in Sec. 1.2.1. To do so, we measure the voltage separation ΔV_1 between two charge jumps along an SLQD peak, as depicted in Fig. 3.3(a). The addition energy of a charge state is then computed as

$$E_{\mathrm{add}} = \alpha_1^{V_1} \Delta V_1. \tag{3.1}$$

We measured the V_1-QD1 gate lever-arm $\alpha_1^{V_1} \simeq 0.3\,\mathrm{eV/V}$ via transport measurements in

the many-electron regime.

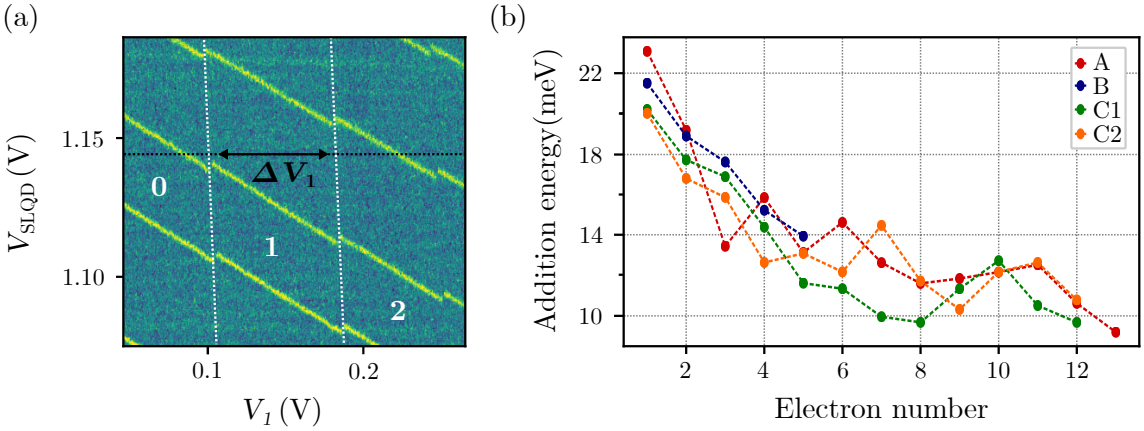

Figure 3.3: Addition energy spectrum. (a) Zoom from Fig. 3.2. In order to compute the addition energy $E_{\mathrm{add}}(N)$, we measure the voltage separation ΔV_1 between the N and the N + 1 charge transitions. **(b)** Addition energy spectrum of four different QDs across three devices (A, B and C), see Appendix B. To compute the spectrum from the transition voltage separation, we have assumed a constant lever-arm parameter $\alpha_1^{V_1}$ for each device. For all curves, we observe a decay inversely proportional to the number of electrons N due to a decrease of the charging energy. However, no reproducible peaks associated with filled shells can be distinguished in the addition energy spectrum.

We show in Fig. 3.3(b) the resulting spectrum for the current sample (device A) and 3 additional devices with similar geometries. For all devices, the addition energy $E_{\mathrm{add}}(N) = E_C + \Delta E$ is roughly inversely proportional to the number of electrons N. Indeed, it is expected that as the dot fills up, the electrons are occupying higher QD orbitals. In consequence, the dot size is increasing, and therefore the charging energy E_C decreases.

Additionally, the orbital spacing ΔE allows us to study the structure of our artificial atom. In particular, the internal spin ($\uparrow$, $\downarrow$) and valley (v_+, v_-) quantum numbers give the number of electrons per orbits (see Sec. 1.2.3). For a 2D harmonic potential with 2 valleys, we have a complete filling of orbital shells for $N = 4,12,24,...$ [Leo20; Tar96]. Thus, we expect an increase of the addition energy for the transitions following those specific occupation numbers to overcome the orbital level splitting.

However, no regular pattern appears in the addition energy spectrum of QD1 for the four devices. It supports the simulations shown in Fig. 2.5, where the first electrons are spread among few QDs pinned by surface disorder and remote charge traps. Nevertheless, we have demonstrated the electron filling of a single dot sensed by an SLQD detector. In the following, we benchmark this detection scheme by monitoring single shot tunneling events.

3.2.2 Charge sensitivity

A requirement for quantum computation using spin qubits is the ability to perform high-fidelity single-shot readout of a dot occupancy up to the single electron level [HC18]. In this part, we demonstrate this single-shot readout and measure the charge sensitivity of the SLQD detector quantitatively. First, we discuss the strategy used to lower the dot-to-lead

tunnel coupling of QD2, down to the measurement bandwidth of the SLQD. Then, we show the measurement of a single tunneling event and extract the detector's charge sensitivity.

Low tunnel coupling

In order to observe a single charge tunneling event, we need a transition (dot-to-lead, or dot-to-dot) in the measurement bandwidth of the SLQD (1 kHz). However, there are no dedicated gates to tune the tunnel couplings in our device. The strategy used here is to focus on QD2 while V_1 and V_6 are kept to 0 V. In this configuration, the QD2 wavefunction does not spread along the nanowire anymore (see Fig. 2.5 for a similar potential landscape). Thus, the tunnel coupling between QD2 and the source lead is greatly reduced.

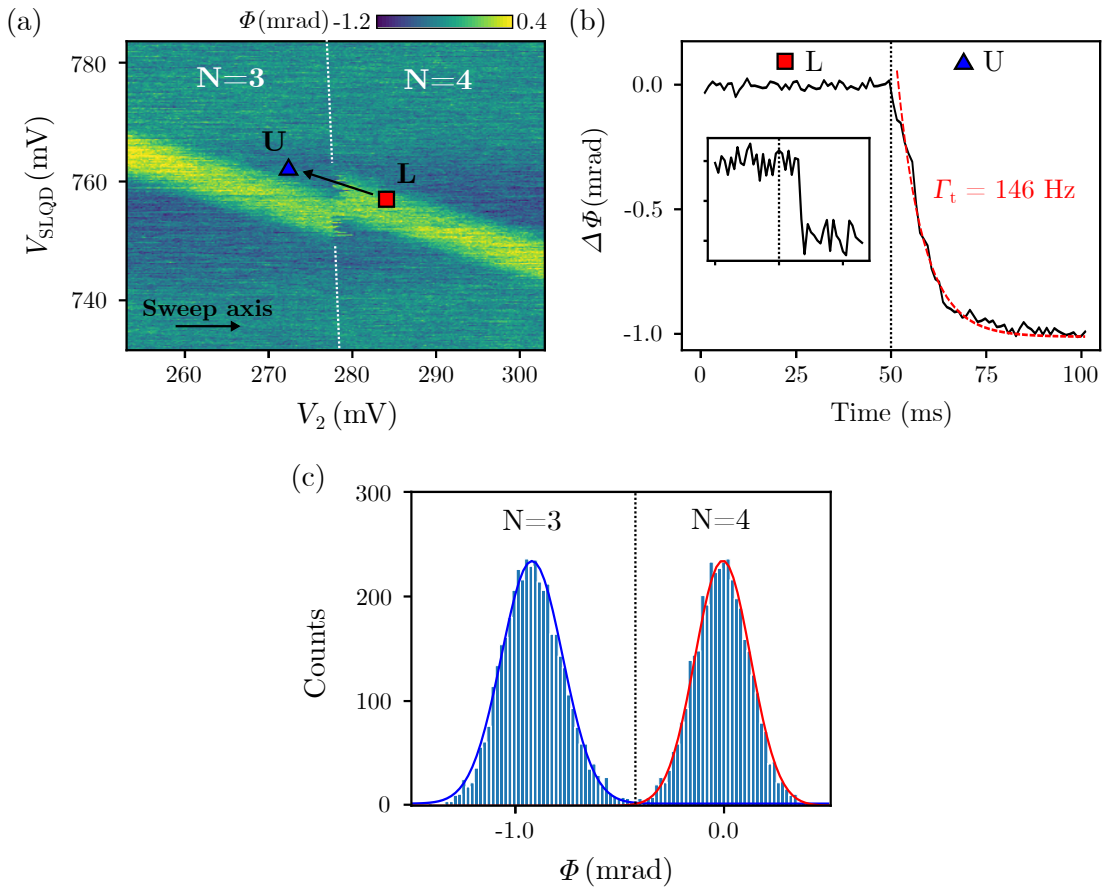

Figure 3.4: Single tunneling events. (a) Stability diagram of the stochastic QD2-to-lead transition $N = 3 \rightarrow 4$. Along the sweep axis, QD2 is brought into the $N = 4$ ground-state on a timescale faster than the QD2-to-lead tunnel rate, occasioning stochastic charge jumps. **(b)** Average of 150 time-traces of the SLQD response while the QD2 is pulsed from the loading position L (red square) to the unloading position U (blue triangle) after 50 ms. We observe a constant SLQD response at the loading and far in the unloading position. From the exponential decay, we extract a QD2-to-lead tunnel rate $\Gamma_t \simeq 146$ Hz. (insert) Single-shot time trace with a stochastic charge jump. **(c)** Histogram built from the previous time-traces. We distinguish in the SLQD phase response two peaks (gaussian fit in solid lines), each associated with a specific charge state. We measure a SNR $\simeq 6.5$ at 1 kHz.

In this regime, we increase the QD2 chemical potential at a rate of 1 kHz for each value of the detector polarization V_{SLQD} in Fig. 3.4. In particular, while the QD2 chemical potential is swept, we move from the N = 3 to the N = 4 ground-state at a speed superior than the QD2-lead tunnel-coupling. As a consequence, the delineation between those two charge states is not straight, as seen in Fig. 3.1, but exhibit stochastic charge jumps. Thus, for each shot, we visualize the time at which an additional electron enters QD2. We can now design a dedicated experiment to measure QD2-lead tunneling events in a single-shot manner.

Single-shot charge tunneling event

We set an experiment where starting with N+1 electrons (loading position L), we pulse QD2 chemical potential above the Fermi-sea (unloading position U) on a µs timescale. For every shot, we spent 50 ms per position while recording the phase response of the SLQD at 1 kHz. A single shot trace is shown in Fig. 3.4(b) insert as an example. The SLQD response remains constant up to the noise level either in the loading position or far in the unloading position. In between, the dot chemical potential is above the Fermi-sea, and the dot is still occupied. In this position, there is a fixed probability that, at each time, the last electron leaves the dot. This tunneling event happens on a time scale several orders of magnitude faster than our acquisition time. Thus, we obtain an abrupt jump on the time trace, at a random time.

If we repeat this experiment 150 times and average all the different shots, we obtain the decay shown in Fig. 3.4(b). By fitting this exponential decay in time t as $\Delta\Phi \propto \exp^{-\Gamma_t(t-t_0)}$, with t_0 the time at which the system is pulsed at the U position, we extract the dot-to-lead tunnel rate $\Gamma_t \approx 146\,\mathrm{Hz}$.

Signal-to-noise ratio

From the 150 shots, we construct an histogram of the different values of the detector (Fig. 3.4(c)). This histogram consists of two peaks each associated with a charge state (left : 3, right : 4 electrons). We fit those peaks with two gaussians of variance $\sigma_3 \approx 0.13\,\mathrm{mrad}$, $\sigma_4 \approx 0.15\,\mathrm{mrad}$ and a peak-to-peak separation $\Delta\sigma \approx 0.92\,\mathrm{mrad}$.

We define our measurement signal-to-noise ratio (SNR) as the ratio between the peak-to-peak separation and the sum of half the peak widths. Thus, for the data shown in Fig. 3.4, we obtain a SNR ≈ 6.5 for a bandwidth BW = 1 kHz. From the Gaussian fits, we compute an error rate in discriminating between the two charge states of 10^{-3}. We get rid of the bandwidth dependence by extracting the charge sensitivity $\frac{1e}{\mathrm{SNR}*\sqrt{\mathrm{BW}}} = 4.9 \times 10^{-3}\, e/\sqrt{\mathrm{Hz}}$. This value is comparable to what has been reported in literature [Col13; Zaj16] but could be improved, as we will discuss now.

On the one hand, we can reduce the noise with a better amplification chain. Indeed, the noise level, obtained from the Gaussian width, is estimated to be around $0.11\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. This value is equivalent to a noise temperature of 4.5 K, which corresponds to the noise of the cryogenic amplifier used, as already reported in a previous experiment with the same amplifier [Urd19]. Thus, the SNR could be improved by using a Josephson parametric amplifier [Sch20], decreasing the noise temperature by more than one order of magnitude.

On the other hand, we can improve the maximum phase shift given by $\Delta\Phi \simeq 2Q \times C_{\mathrm{Q}}/C_{\mathrm{p}}$

(see Sec. 1.3.2). For example, on-chip inductors are developed to improve drastically the SLQD quality factor up to $Q \simeq 1000$ [Jar19] ($Q \simeq 50$ for this experiment), and decrease the parasitic capacitance C_p.

3.3 Multi-dot measurements

In the last part, we demonstrated that the SLQD could be used to probe its next-neighbor dots, one-by-one, by realizing 2D-maps SLQD/probed dot. Here, we show different detection schemes in order to extend its detection range to multi-dot systems. First, the detector is biased at a fixed value, and we highlight the strong capacitive couplings between the dot-gates and the SLQD. It results in the detector's detuning while scanning the double-dot system and thus to a small detection window. Then, we correct the cross-capacitive coupling gate-SLQD a priori and discuss the requirement for an active feedback loop. Finally, we develop a detection scheme that overcomes the need for a feedback loop at the cost of increased experiment time. We use this method to probe a double quantum-dot on a broad voltage range, allowing us to assert the Coulomb disorder inside our device.

3.3.1 Fixed detector probe

In Figure 3.1(b), we have monitored the SLQD peak position for different values of V_1. However, we need to explore the voltage space in both V_1 and V_2 in order to probe a double-dot system like QD1-QD2. To get rid of the V_{SLQD} dependence, we bias the detector at a fixed value.

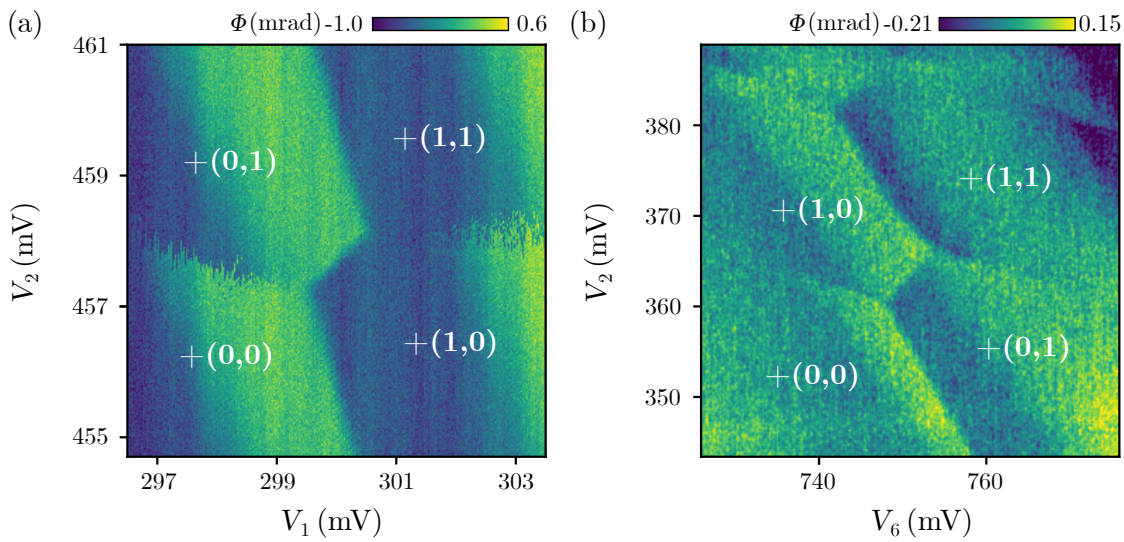

Figure 3.5: Interdot transition of the QD1-QD2 and QD2-QD6 DQD at fixed SLQD bias. (a) The detector phase response is plotted as a function of (V_1,V_2) while the SLQD bias is kept fixed. The SLQD position is tuned to have a maximal sensitivity at the inter-dot transition. In particular, the SLQD is completely turned off across the inter-dot transition due to an important SLQD-dots coupling. Additionally, the SLQD sensitivity vanishes rapidly around the inter-dot due to the cross-capacitive coupling SLQD-gates. **(b)** Same than **(a)** for the QD2-QD6 DQD and the gates (V_6, V_2).

On the Figure 3.5(a), the SLQD is biased at $V_{\mathrm{SLQD}} = 849\,\mathrm{mV}$ and the voltages V_1

and V_2 are swept over few millivolts. On this stability diagram, a QD1-QD2 inter-dot transition with a positive slope can be observed, in contrast with the QD1-lead and QD2-lead transitions of negative slopes. For clarity, we label the number of charges in each dot as (N_1, N_2), and omit a fixed charge offset estimated to be (3,1). The QD2-lead transition shows stochastic events along the fast sweep axis, similar to what has been obtained in Fig. 3.4.

However, this stability diagram is the final result of tedious manual tuning. Indeed, at fixed bias, the SLQD sensitivity quickly vanishes when we change the surrounding gate voltages by only a dozen millivolts. This behavior is also visible in Fig. 3.5(b), where a QD2-QD6 inter-dot transition is explored on a broader range. Back on Figure 3.5(a), the addition of one charge in QD1 (transition (0,0) $\rightarrow$ (0,1)) induces a voltage shift $\Delta V \simeq 3.0\,\mathrm{mV}$ on the position of the SLQD peak (see Fig. 3.1(b) for a direct observation). This shift is bigger than the SLQD linewidth $lw = 1.7\,\mathrm{mV}$. Thus, we see that the detector switch from a ON-value on the left of the transition to a OFF-value on the right. Furthermore, the cross-capacitive coupling between the applied gate voltages V_2 and V_6 with the SLQD potential slowly detune the detector. This effect is visible on the left of the transition, where the SLQD signal vanishes after $\sim 2\,\mathrm{mV}$. We note that both effects are weaker for QD2 and its associated gate V_2 due to the device geometry. In this case, the voltage shift induced by charge addition $\Delta V' \simeq 2.1\,\mathrm{mV}$ is still larger than the SLQD linewidth, but the limited V_2-SLQD coupling allows to probe more than one charge transition as it can be seen in Fig. 3.5(b).

Fixing the detector's bias allows probing the charge occupation and dynamics of a double-dot system locally. However, the cross-capacitive coupling between the next-neighbor gates (V_1, V_6) and the single-lead QD quickly detunes the detector over a few millivolts only. Additionally, the capacitive coupling between the next-neighbor dots and the SLQD completely detunes the detector when a charge is added in the probed double-dot. In consequence, this method is inefficient to explore a multi-dot system where we need to sweep dot gates over 1 V like in Fig. 3.2 .

3.3.2 Capacitive-coupling compensation

In this part, we study the different capacitive couplings quantitatively. We show that we can correct a priori the gate-SLQD cross-capacitive coupling but not the shifts induced by added charges. Finally, we set the requirements for a feedback-loop capable of correcting both gate-SLQD and dot-SLQD couplings.

A priori compensation

From the single-dot stability diagram in Fig. 3.1, we measure a lever-arm ratio $\alpha_{\mathrm{SLQD}}^{V_1}/\alpha_{\mathrm{SLQD}}^{V_{\mathrm{SLQD}}}$ $= 0.36$ between the SLQD gate and the gate V_1 on the detector dot. This lever-arm ratio corresponds to the slope of the SLQD peak between two charge jumps. It quantifies the cross-capacitance coupling between the gate V_1 and the single-lead quantum dot, normalized by the dedicated SLQD gate's effect. Taking into account the detector linewidth lw, we can directly compute the maximum detection range for which a fixed bias SLQD remains sensitive, $r_{V1}^{max} = lw/\alpha_{\mathrm{SLQD}}^{V_1} \simeq 5\,\mathrm{mV}$. This value is consistent with the limited detection range in Fig. 3.5(a).

Knowing the V_1-SLQD cross-capacitive coupling, we can set an experiment compensating the detector drift induced by V_1 on the detector during a stability diagram. With this compensation, the SLQD is insensitive to the V_1-SLQD coupling, and we record only charge jumps. The Figure 3.6 shows a stability diagram of QD1 and QD2 where the capacitive coupling due to V_1 is compensated by applying a correction on the SLQD bias : $V^c_{\text{SLQD}} = V^d_{\text{SLQD}} - \alpha^{V_1}_{\text{SLQD}} \left(V_1 - V_1^d\right)$ at each step. The default bias V^d_{SLQD} is chosen to match the best detector sensitivity at a voltage set $\left(V_1^d, V_2^d\right)$ given by the black triangle on Fig. 3.6. In this stability diagram, the SLQD response remains constant on the V_1-axis except when the QD1 occupancy changes (white dashed line). In contrast, this is not the case for the uncompensated V_2-axis where the signal vanishes due to the SLQD-V_2 coupling, like Fig. 3.5. We note that, since the detector linewidth is smaller than the detector shift induced by the addition of a single electron, it is not possible to picture more than one charge state on a compensated axis.

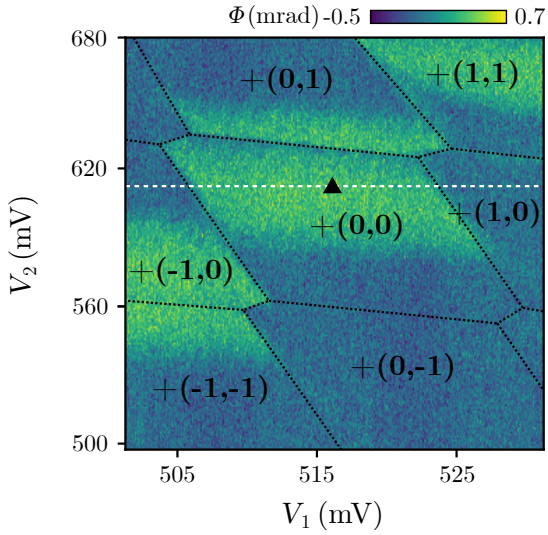

Figure 3.6: Stability diagram with a priori compensation. The detector phase is plotted in function of (V_1, V_2), while the SLQD bias position is corrected to compensate for the V_1-SLQD capacitive coupling. The initial SLQD bias is tuned at the black triangle position. The SLQD response remains constant in the +(0,0) charge state along the V_1 axis, and vanishes along the uncompensated V_2 axis. The SLQD is abruptly detuned at a charge transition allowing to access a particular charge state boundary (white dashed line).

Generalizing this method to both axes allows us to probe the boundaries of a given charge state and explore a multi-dot system by highlighting the charge configurations one by one. However, we considered so far that the lever-arm ratios are constant. For example, this is not true when a dot grows in size by increasing its electron number. Additionally, Coulomb disorder can locally drastically affect the SLQD-gates couplings by the intermediate of spurious QD transitions, as we will discuss in section 3.3.3. So, instead of building a knowledge of the cross-capacitive couplings a priori and then mapping each charge configurations individually, we look for a protocol that automatically corrects the detector drift during an experiment, and retunes the SLQD when a charge jump occurs.

Requirements for automatic feedback-loop compensation

In the last part, we have identified the need for a detection scheme to correct the bias applied on the SLQD detector in real-time, accounting for both the gate-SLQD coupling and the significant detector shifts induced by the addition of charges in the probed QDs. This apparatus is required to explore the charge configurations of a multi-dot system efficiently.

The simplest solution to adjust the SLQD bias along a gate sweep consists of using a proportional–integral–derivative (PID) feedback loop. The PID corrector takes as input the SLQD phase response Φ and its output V_{PID} is added to the SLQD DC bias as $V^{C}_{\mathrm{SLQD}} = V_{\mathrm{SLQD}} + V_{\mathrm{PID}}$. For each point of an experiment, the correction bias V_{PID} is adjusted so that the SLQD response Φ is constant. This apparatus works well to correct the SLQD detector when the signal slightly increases or decreases, like the effect of the gate-SLQD coupling. However, this simple PID corrector is not reliable for events where the SLQD is abruptly turned OFF by the addition of one charge in a probed dot.

In consequence, a FPGA-controlled feedback loop has been developed by Yang *et al.* [Yan11]. Here, the voltage correction applied to the SLQD detector is the solution of a user-defined algorithm. In [Yan11], they develop a set of equations based on the detector response to maintain the sensor sensitivity even when large charge jumps occur.

Developments are made in our group to integrate an analog-to-digital converter wired directly to the same FPGA that controlled our DACs. Once achieved, we could implement the previous solution and efficiently explore an unknown multi-dot system's charge configurations without a priori knowledge. In the mean-time, feedbacks based on our measurement software need a few seconds per loop, which is three order of magnitudes slower than the lower-bound given by the 1 kHz detector bandwidth. Consequently, in the next part, we develop a detection scheme to perform large voltage range scans without relying on a feedback-loop.

3.3.3 Full detection scheme

In the previous section, we have highlighted that the tight device geometry implies a strong capacitive coupling. We identified an FPGA based solution to maintain a high SLQD sensitivity continuously. In this part, we discuss a scheme that allows us to achieve similar results without further hardware developments. This method relies on the acquisition of the entire voltage space, including both the probed dots (e.g., V_2, V_6) and the SLQD peak (V_{SLQD}).

First, we detail the operating principle of this full detection scheme. Then, we use this technique to probe double quantum-dots in the many-electron regime and emphasize the regular honeycomb pattern. Finally, we focus on the few-electron regime and underline the Coulomb disorder present in our devices.

Detection scheme

As we have seen, the sensitivity of the detector is limited from one to few charge transitions before the signal vanishes due to the small detector linewidth and the strong capacitive coupling. Thus, a fixed sensing position can only be hold for voltage ranges $r^{max} \sim 5\,\mathrm{mV}$ while the coarse tuning of a double-dot like (QD1, QD2) implied to explore a voltage

space (V_2, V_6) as large than (500 mV × 500 mV). Since we cannot follow the SLQD peak displacements, we develop here a new scheme where we take a full trace along the SLQD axis for each value of (V_2, V_6) and then extract the peak position. In Figure 3.7(a), we show detector traces for two different gate sets $V_6 = 675$ mV and $V_6 = 800$ mV, with V_2 fixed at 460 mV.

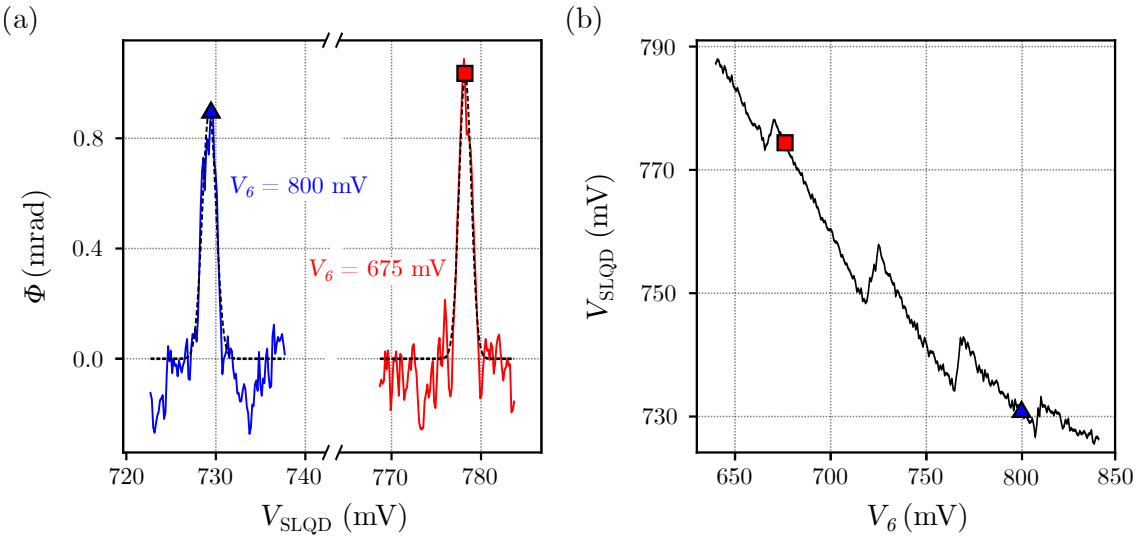

Figure 3.7: Full detection scheme. (a) An SLQD phase peak is plotted for $V_6 = 675$ mV and 800 mV and fitted as a gaussian peak (black dashed lines). Due to the capacitive couplings, the peak position is shifted by about 50 times the SLQD linewidth between these two positions. For our new detection scheme, we measure and fit the SLQD peak position for *each* QD gate set and extract the SLQD peak position. **(b)** Fitted SLQD peak position plotted against QD6 gate voltage. The peak position encodes its electrostatic environment, notably the V_6-SLQD coupling (slow drift) and the addition of electrons into QD6 (abrupt jumps).

As expected, the SLQD peak position moves on a voltage scale larger than its linewidth, and it exists no detector fixed bias V_{SLQD} that can maintain charge sensitivity for both voltage configurations. So, we fit the SLQD response with a gaussian function and extract the peak position V_{peak} for each set (V_2, V_6). In Figure 3.7(b), we plot the detector position over a range of 200 mV. We see that the detector shift encodes both the cross-capacitive coupling (slow drift) and the charge transitions (large jumps). In particular, we note that the cross-capacitive coupling is not constant over many charge transitions, as discussed previously. Finally, this detection scheme's sensitivity is constant over large voltage ranges, as long as we can measure the SLQD peak position.

Nevertheless, a drawback of this method is the time spent in taking a trace of the detector for each point of the voltage space. We minimize the experiment time by focusing only on a small voltage window around the detector peak, and we calibrate beforehand the window to follow roughly the peak shift. Thus, with a detector trace limited to 100 points acquired at 1 kHz, the acquisition time for the Fig. 3.8 and 3.9 is in the range of 2-3 hours. In return, the time spent for each set (V_2, V_6), ~ 100 ms, allows to probe charge transitions with low tunnel rate.

In conclusion, we have demonstrated a method to probe multi-dot systems using the SLQD. This scheme overcomes the large capacitive couplings SLQD-gates and SLQD-probed dots, inherent of our split-gate nanowire devices, at the cost of increased measurement time.

Many-electron regime

In Figure 3.8, we use this detection method to probe the many-electron regime of QD2 and QD6. For clarity, we removed a linear drift of the detector corresponding to the mean SLQD-gate capacitance coupling, for both gates V_2 and V_6. This extended stability diagram shows a regular honeycomb pattern, characteristic of a double quantum dots (see Sec. 1.4.1). We label each charge state (N_2, N_6) omitting a fixed charge offset estimated to $(12, 18)$. From this diagram, we can learn about the dot sizes and positions.

First, the addition energy spectrum is here almost constant and we measure a charging energy $E_c = e^2/C \simeq 6\,\text{meV}$ for both dots. We can estimate an upper bound of the dot size by considering a circular quantum dot in a 2-dimensional harmonic potential. Moreover, we only consider the circular dot self-capacitance $C = 8\varepsilon_0\varepsilon_r R$ [Kou91], with ε_0 the vacuum permittivity and ε_r the relative permittivity of intrinsic silicon. We obtain a dot radius $R \simeq 30\,\text{nm}$, whom accounting for the gate width $W = 50\,\text{nm}$, is compatible with the corner dot picture.

Furthermore, we extract the different dot-gate couplings given by

$$\frac{\alpha_{\text{SLQD}}^{V_2}}{\alpha_{\text{SLQD}}^{V_{\text{SLQD}}}} \simeq 0.2 \quad (3.2a) \quad , \qquad \frac{\alpha_{\text{SLQD}}^{V_6}}{\alpha_{\text{SLQD}}^{V_{\text{SLQD}}}} \simeq 0.5 \quad (3.2b) \quad ,$$

$$\frac{\alpha_2^{V_6}}{\alpha_2^{V_2}} \simeq 0.2 \quad (3.2c) \quad \text{, and} \qquad \frac{\alpha_6^{V_2}}{\alpha_6^{V_6}} \simeq 0.5 \quad (3.2d) \quad .$$

On one hand, equation 3.2a (respectively 3.2b) refers to the gate V_2-SLQD coupling (resp. V_6), normalized by the V_{SLQD}-SLQD lever-arm. Those lever-arm ratios are extracted from the detector peak position drift along both axis on Fig. 3.8 raw data. And as expected, the V_6 gate is more coupled to the SLQD than V_2, due to the device geometry.

On the other hand, equation 3.2c (respectively 3.2d) deals with the V_6-QD2 coupling (resp. V_2-QD6) and is obtained through the dot-to-lead transition slopes. Surprisingly, both couplings have a strong asymmetry with a much stronger effect of V_2 on QD6 than the opposite. Two phenomena explain this asymmetry. First, we are operating in a regime where $V_6 \simeq 2V_2$, plus a strong SLQD bias $V_{\text{SLQD}} \simeq 750\,\text{mV}$ while V_1 is kept at $0\,\text{V}$. Consequently, the potential landscape is asymmetric. We expect QD6 to be bigger than QD2, spread more out of the nanowire corner, and be more sensitive to its electrostatic environment. In addition, the device itself is asymmetric due to an imperfect alignment of the split-gates with respect to the nanowire. The misalignment is already visible on the room-temperature characterization of the device (see Appendix A), with an increase of the threshold voltage for the upper side of the transistor (V_5, V_6, V_7, V_8) compare to the lower side (V_1, V_2, V_3, V_4). However, we have measured for both sides similar lever-arms $\alpha_{\text{SLQD}}^{V_{\text{SLQD}}} \simeq \alpha_1^{V_1}$ in the many-electron regime, which indicates that the dots are strongly

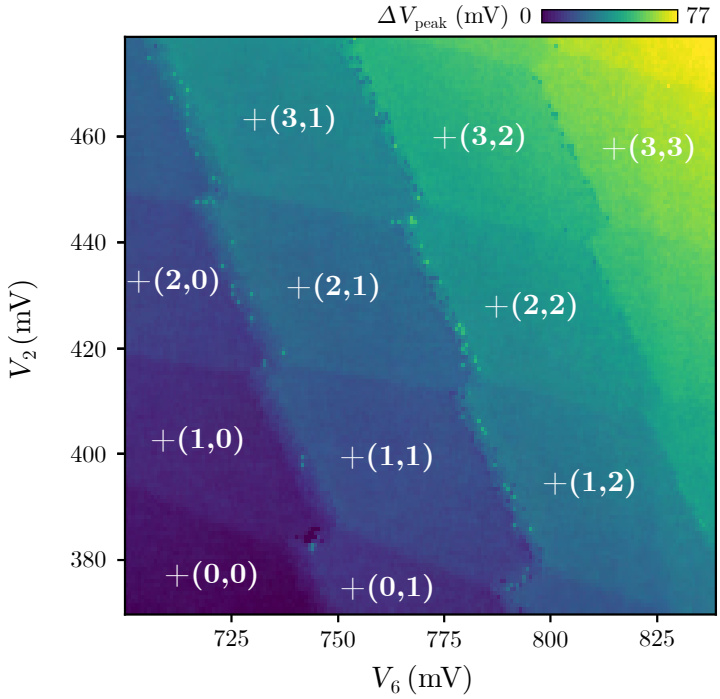

Figure 3.8: SLQD peak position in the many-electron regime. The SLQD peak position is plotted against (V_2, V_6). It describes a clear honeycomb pattern, characteristic of a DQD. We label each charge state (N_2, N_6) , omitting a fixed offset $(12, 18)$.

localized in the corners of the nanowire.

Few-electron regime

We have demonstrated that our measurement scheme can be used to explore charge transitions in the many-electron regime of the QD2-QD6 double quantum-dot. However, for the operation of a QD array, we are interested in filling each dot with a single electron. In Fig. 3.9, we have monitored the SLQD peak position while exploring the (V_2,V_6) voltage space in the few-electron regime.

First, when $V_2 > 400\,\text{mV}$, we obtain a regular honeycomb pattern, similar at Fig. 3.8. Same thing for $V_2 < 325\,\text{mV}$, where we see the inter-dot transition QD2-QD6 associated with the first electron in the double-dot system. In particular, the transition line $0 \rightarrow 1$ of QD2 is almost vertical due to a sub-Hertz QD2-lead tunnel rate.

Then, we focus on the central part of the diagram. We see that, in addition to the quasi-vertical lines associated with QD2 and the quasi-horizontal lines with QD6, there is an oblique line crossing the diagram (black line in Fig. 3.9 insert). This line corresponds to an accidental dot that we label D, which is tunnel-coupled to QD2 and QD6. Thus, the stability diagram does not picture a honeycomb pattern but a more complex structure.

In order to investigate the localization of the quantum dot D, we measure the lever-arm ratios of the different dots given by

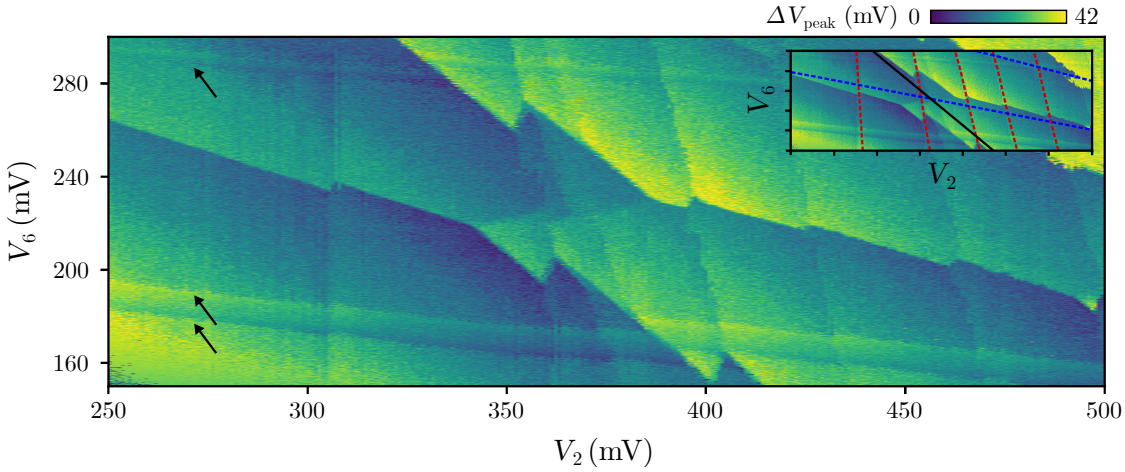

Figure 3.9: SLQD peak position in the few-electron regime. The SLQD peak position is plotted against (V_2, V_6). While a clear honeycomb pattern is visible for $V_2 < 325\,\text{mV}$ and $V_2 > 400\,\text{mV}$, the center part of the diagram despites a more complex figure with the presence of a third dot transition. Additional transitions (black arrows) are linked to spurious dots in the gate stack. **(insert)** Dot-to-lead transitions are associated to a unique color for each dot (QD2:red, QD6:blue, D:black). The left-most red (respectively lowest blue) transition corresponds to the first electron in QD2 (resp. QD6).

$$\frac{\alpha_2^{V_6}}{\alpha_2^{V_2}} \simeq 0.2 \quad (3.3a) \qquad , \frac{\alpha_6^{V_2}}{\alpha_6^{V_6}} \simeq 0.5 \quad (3.3b) \qquad , \frac{\alpha_{\text{D}}^{V_6}}{\alpha_{\text{D}}^{V_2}} \simeq 0.74 \quad (3.3c) \ .$$

The lever-arm ratios are extracted from the slope of the corresponding dot-lead transitions. For reference, we measured the lever-arm ratios for QD2 (Eq. 3.3a) and QD6 (Eq. 3.3b). We retrieve the same results than in the many-electron regime, with an asymmetry between V_2 and V_6 due to a misalignment of the gates. However, we measure a lever-arm ratio close to unity for the oblique transition, indicating that both gates have a similar effect on the quantum dot D. Thus, we infer that the dot D is not confined under a specific gate, in a nanowire's corner, but lies inside the channel, in-between the gate V_2 and V_6. This dot is attributed to unintentional doping of the channel during the formation of the source and drain reservoirs.

In addition, we highlight the triple-dot formed by QD2, QD6 and D by focusing on the central part of the diagram in Fig. 3.9. We label each dot's absolute charge occupancy and distinguish dot-to-lead transitions (solid lines) from inter-dot transitions (dashed lines). It is worth noting that among this triple-dot, the mutual capacitance of each inter-dot transition is larger than the typical values reached in the QD2-QD6 double-dot with the regular honeycomb pattern at $V_2 > 400\,\text{mV}$. This is coherent with the hypothesis of a donor trapped in-between QD2 and QD6 that leads to closer dots and larger inter-dot coupling.

Back in Fig. 3.9, we can see an additional set of lines coupled to gate V_2 (black arrows) that belong to other accidental quantum dots. Nevertheless, those dots are only capacitively coupled to QD2, QD6, and D. It has been previously reported that such defects could be

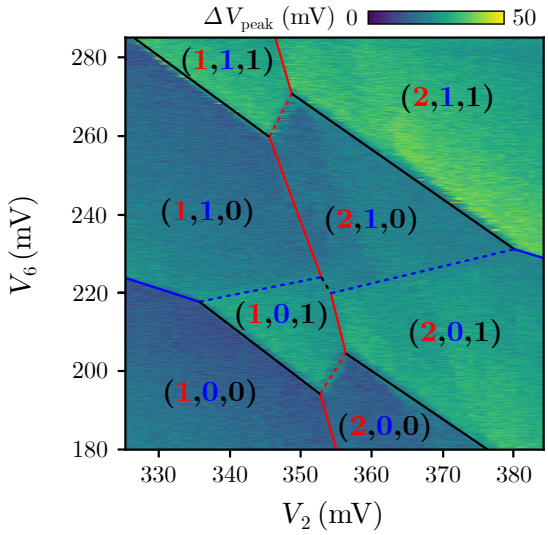

Figure 3.10: Triple-dot configuration. Zoom in the central part of Fig. 3.9. We label each charge state (N_2, N_6, N_D) and distinguish dot-to-lead (solid lines) from inter-dot transitions (dashed lines).

located in the device gate stack [Ibb18].

In conclusion, we have been able to measure a double-dot occupation up to the last electron. However, we have highlighted the presence of fixed charges, whether defects in the channel or charge trapped in the gate stack, that can be detrimental for the large-scale control of QD arrays. Indeed, the presence of static disorder modifies the electrostatic environment of the QD locally and affects the dot-to-dot variability. As discussed in section 1.4.4, a scalable architecture necessarily relies on shared control gates. It implies some requirements to match between the variability of the dot and the versatility of the architecture. Consequently, to avoid accidental dots as the dopant in the channel, different fabrication routes are currently under investigation, such as the epitaxial formation of the reservoirs.

3.4 Conclusion

This chapter has demonstrated the charge control of a 2x2 quantum dot array in a silicon nanowire. To this end, we develop and benchmark a single-lead quantum dot electrometer embedded in the array. We have highlighted the strong cross-capacitive couplings due to the tight geometry architecture. Different detection schemes are elaborated to mitigate those effects and probe double quantum-dots over large voltage ranges. These methods led us to investigate the Coulomb disorder inside the silicon device.

Following this work, several paths are under investigation. First, developing a robust silicon QD platform with low dot-to-dot variability requires an efficient way to explore each device's charge stability and dynamics. Thus, efforts are made to systematize the measurement protocols developed here and improve them, such as using feedback loops. We could then operate the array as a quantum information processor, using one side of

the nanowire as an qubit register and the other as readout sites [Fra16]. Toward this goal, a first demonstration consists of using SLQD detectors to monitor the shuttling of an electron-spin qubit from one end of the array to the other [Fuj17; Mor18]. Also, the SLQD detection allows probing electron-spin qubits isolated from the reservoirs that should benefit from improved coherence times, as demonstrated in GaAs quantum dots [Ber15b].

CHAPTER 4

Charge control of a 2x2 Gallium-Arsenide quantum-dot array

4.1 Introduction

In the previous chapter, we have operated a QD array in a silicon nanowire and probed different double quantum-dot configurations. However, it is not possible yet to tune the tunnel couplings in-between quantum-dots and with the reservoirs in our current Silicon platform. Moreover, the nanowire geometry that has been explored has limited scalability (see Sec. 1.4.4).

In this chapter, we use the Gallium-Arsenide platform as a test-bed for a scalable quantum-dot architecture. The device is pictured in Fig. 4.1(a) and was manufactured with the recipe detailed in Sec. 2.3.1. The architecture uses control gates shared between complete row and column of quantum-dots to define a 2x2 quantum-dot array. Each gate controls either a tunnel-barrier or a chemical potential along the array. Thanks to this geometry, only ten gates are required for a 2x2 QD array. For the complete 4x4 QDs device, we multiply by four the number of quantum-dots but only by approximately $\sqrt{4} = 2$ the total number of gates. Then, two challenges need to be resolved : (i) Does the device have enough tunability to control up to 4 electrons into a 2x2 QD array ? (ii) How do we tune a scalable array of quantum-dots ? Indeed, we have to demonstrate that the device architecture with shared control gates has enough versatility to control the QDs chemical potentials and inter-dot couplings. In addition to a scalable array, we have to develop a scalable tuning protocol following the increase in the size of the QD arrays.

We start by investigating how to trap electrons inside the QD array in Sec. 4.2. As discussed in Section 1.4.3, the isolated regime significantly reduces the tuning complexity by working at a fixed number of electrons. Thus, we develop a loading procedure to trap up to 5 electrons into a single QD and close its connection to the reservoir. Next, the simulations of stability diagrams in the isolated regime are detailed in Sec. 4.3. These simulations use the constant interaction model to reproduce the experimental data and characterize the device and its architecture. Finally, in Section 4.4, we explore the control of the QD array in the isolated regime by controlling first a double quantum-dot, then the complete 2x2 QD array. Through the simulations, estimates of the system parameters are extracted.

4.2 From an open system to the isolated regime

In the following, we demonstrate how to trap a fixed number of charges inside the quantum-dot array. To do this, we first use a QPC detector to sense the electron filling of a dot from the reservoir (see Section 4.2.1). Then, in Section 4.2.2, we develop the loading procedure

used to trap the electrons inside the array. Finally, we study in Section 4.2.3 different open DQDs configurations to get insight on how to tune the 2x2 QD array in the isolated regime.

4.2.1 Charge detection

Single-dot regime

In order to detect the charge dynamics inside the QD array, we use the detector controlled by the S_{R}, S_{P}, and S_{L} gates as illustrated in Fig. 4.1(a). These gates form a QPC sensor, close to the array entrance, which is biased to its position of maximum sensitivity (Fig. 4.1(b)). We monitor the current i_{QPC} flowing through the sensor to detect nearby charge events.

In Figure 4.1(c), a stability diagram of the upper-right quantum dot (QD2) is performed by sweeping the gate potential V_{B1} for different values of H_{P1}, while the rest of the array is polarized. The derivative of the sensor current along the sweep axis gives the color code. As in the case of the silicon device (Fig. 3.2), we distinguish two contributions in the sensor's response. First, the cross-capacitive coupling between the sensor and the array gates causes a slow drift of the detector response, corresponding to the gradient background on the stability diagram. Second, the sensor response experiences sharp jumps for specific voltages, forming lines. The diagonal lines are each associated with adding one electron into QD2. In contrast, the additional white dashed line coincides with a QD4 transition, as we will discuss in the next part.

If we focus on the QD2 transitions, we notice that the set of lines is evenly spaced, and the detector response remains constant as we decrease the number of electrons (lower H_{P1} values). In addition, no similar transitions are detected for $H_{\mathrm{P1}} < -100\,\mathrm{mV}$. Thus, we can count the absolute number of electrons inside QD2 starting from $N_2 = 0$ on the left of the diagram to $N_2 = 10$ on the right.

Furthermore, while the gate H_{P1} mainly affects the chemical potential of QD2, the gate V_{B1} adjusts the tunnel barrier between the dot and the reservoir due to the geometry of the device. For low negative values of V_{B1} (upper half of the diagram), there is a large coupling between QD2 and the reservoir. So, we see clear charge degeneracy lines, and the number of electrons inside QD2 is well controlled by the gate H_{P1}. Applying a negative voltage $V_{\mathrm{B1}} \simeq -750\,\mathrm{mV}$ (lower part of the diagram) reduces the tunnelling rate below the measurement time (1 ms/pt), as demonstrated by the stochastic charge jumps along the sweep direction. In section 4.2.2, we use this capability to demonstrate the isolation of an arbitrary number of charges within QD2.

Sensor tuning automation

To obtain the previous stability diagram, we have to tune the QPC at its best sensitivity. However, this position depends on the array gate voltage configuration due to the capacitive couplings. Hence, we have implemented two routines to facilitate the acquisition of stability diagrams. Using our homemade software (see Sec. 2.5), these methods automatically calibrate the QPC according to the desired stability diagrams.

The first calibration scheme consists in taking a QPC trace, similar to Fig. 4.1(b), carried out for a polarization of the array which corresponds to the middle point of the aimed stability diagram (for Fig. 4.1(c), $H_{\mathrm{P1}} = 0\,\mathrm{mV}$ and $V_{\mathrm{B1}} = -750\,\mathrm{mV}$). Next, the detector

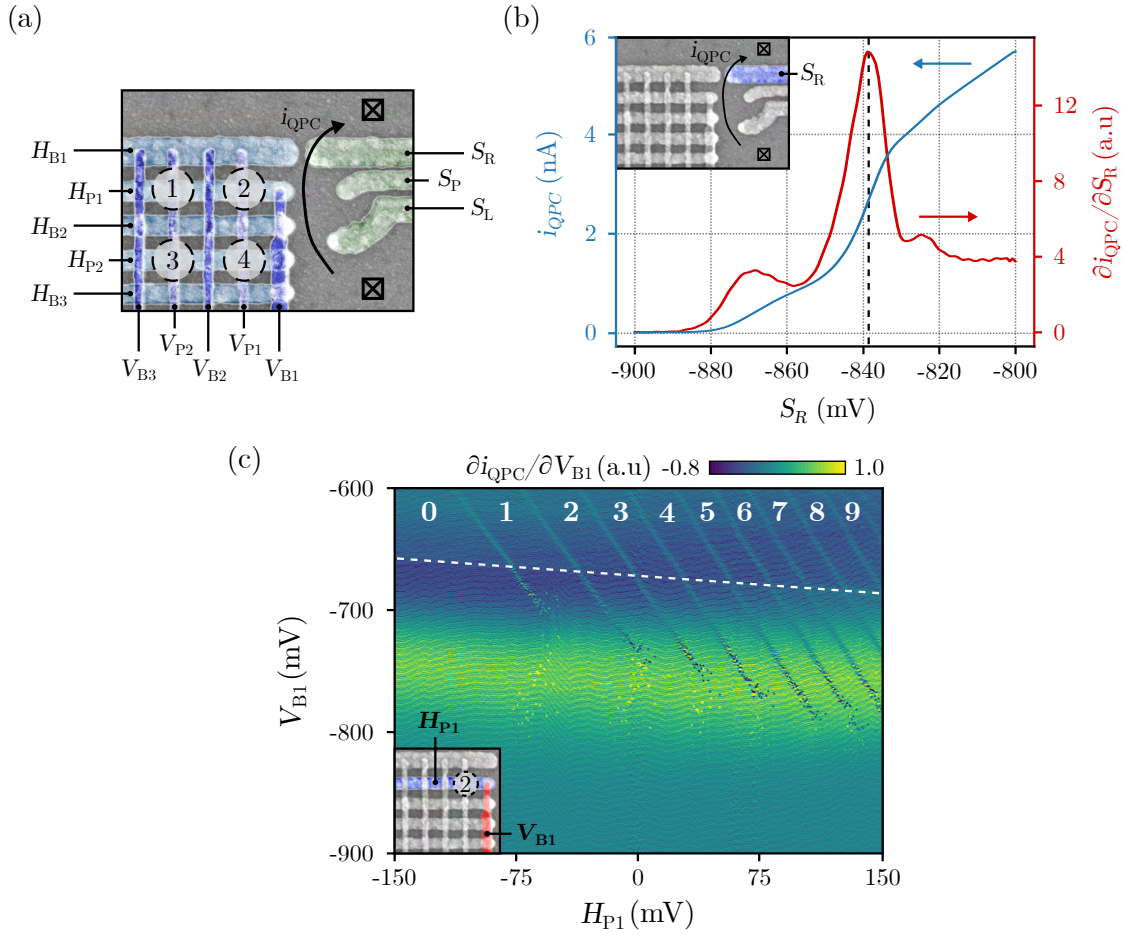

Figure 4.1: Detector tuning and single-dot stability diagram. (a) False color SEM micrograph of the device with the gate labels, the QDs configuration (QD1 → QD4), and the ohmic contacts used (black cross box). **(b)** Example of QPC characterization. The current i_{QPC} flowing through the QPC (see inset) is measured for different values of S_R (black solid line). We extract the bias that maximizes the QPC sensitivity by looking at the maximum of the current derivative (solid red line). For this particular polarization of the device, it corresponds to $S_R \approx -839\,\text{mV}$ (dashed black line). **(c)** Stability diagram of QD2 as a function of the plunger H_{P1} and the barrier to the reservoir V_{B1}. We control the occupation of QD2 from $N_2 = 0$ to 10 electrons (white labels). For $V_{B1} \lesssim -750\,\text{mV}$, the QD2-lead tunneling time is smaller than the measurement time (1 ms/pt) as demonstrated by the stochastic charge jumps along the sweep direction V_{B1}. An additional charge transition associated to QD4 is highlighted (white dashed line). Inset: device configuration.

bias is automatically extracted by finding the voltage that maximized the detector's current gradient and applied it to the stability diagram's array bias. This technique allows us to freely explore the gate voltage space without the overhead of manual detector tuning. However, inside a stability diagram, the QPC sensitivity decreases as we move from the diagram's center due to the QPC-gates capacitive coupling.

To overcome this issue, we implement a second automation routine based on a priori compensation. As for Section 3.3.2, the idea is to calibrate the detector at the edges of the stability diagram axes. Then, we guess the best QPC bias for each point of the diagram by linear interpolation and get rid of the detector-gates capacitive coupling. The main difference with the silicon device is that, here, the detector peak shifts induced by the addition of electrons are small compared to the detector peak linewidth. Thus, it is possible to observe many transitions along a compensated axis before detuning the QPC, while only one transition was observable in the silicon nanowire. For example, this automated calibration was performed along the x-axis (H_{P1}) on Figure 4.1(c). For each value of H_{P1}, the QPC bias is compensated so that the detector sensitivity remains constant. At the opposite, the uncompensated gate V_{B1} detunes the detector along the y-axis.

Finally, these methods were generalized to all the experiments to such an extent that the manual tuning of the sensor is no longer carried out. In particular, we use this automated tuning in the *loading map* experiments, which we discuss in the next section.

To conclude, we have demonstrated the control of a single-dot (QD2) chemical potential down to the single electron occupation and its tunnel-coupling to the reservoir. To achieve the charge sensing of QD2, we have used a proximal QPC as a local electrometer. We have introduced simple automatic procedures to tune the electrometer at its best sensitivity before any experiments. In the next section, we develop a pulse sequence to trap an arbitrary number of electrons in QD2 and reach the so-called isolated regime.

4.2.2 Loading procedure

In the stability diagram Fig. 4.1(c), we have seen that a negative pulse on V_{B1} turns off the QD2 tunnel coupling to the reservoir. Furthermore, applying a more negative voltage on V_{B1} also raises the QD2 potential. Thus, this pulse can bring the system into a metastable state where an arbitrary number of electrons inside QD2 is trapped above the Fermi sea level. As discussed in Sec. 1.4.3, the isolated regime where the QD array is uncoupled from the electron reservoirs is a key ingredient to facilitate the tuning of multiple quantum-dots devices. Here, we use this feature to perform the loading and isolation of up to 5 electrons in QD2. We will particularly highlight the loading of electrons inside QD2, in a metastable position, by comparing it to the emptied dot case. This demonstration is the basis of the control of the 2x2 QD array in Sec. 4.4.

Pulse sequence

To demonstrate the isolation of the electrons, we use the pulse sequence described in Fig. 4.2(a) to navigate through the stability diagram (Fig. 4.1(c)). First of all, starting from a reference point **R** with 0 electron inside QD2, we pulse gate V_{B1} down to $-900\,\mathrm{mV}$ to cut the coupling to the reservoir. Then, we pulse QD2 chemical potential to $H_{\mathrm{P1}} = 100\,\mathrm{mV}$ to reach the measurement point **M** where we take a first *reference value*. This value encodes

the sensor response for this particular gate configuration while QD2 is empty. Next, the system is pulsed back and forth to a probed point **P** within the stability diagram for a few milliseconds. On the way back, as for the first reference pulse, we first cut the coupling to the reservoir using V_{B1}, and only then we change the QD2 potential to reach the point **M** with H_{P1}. At the end of this path, a *signal value* is acquired.

In Figure 4.2(b), we show the detector response during the entire $\mathbf{R} \rightarrow \mathbf{M} \rightarrow \mathbf{P} \rightarrow \mathbf{M}$ pulse sequence. We are interested in the current difference Δi_{QPC} between the *signal* and the *reference* measurements. This quantity only describes the difference in electron occupation between the two states since the two measurements are performed for the same gate configuration (H_{P1}, V_{B1}), after different loading pulses.

Loading map

We repeat this pulse sequence so that the probed point **P** maps the stability diagram's full range. We obtain a so-called *loading map* (Fig. 4.2(c)) where, for each coordinate of **P**, we plot the value of Δi_{QPC}.

On the one hand, the upper half of the diagram shows areas whose boundaries match the charge degeneracy lines for $N_2 = 0 \rightarrow 5$ (see Fig. 4.1 (c)). Indeed, in this regime, the QD2-lead tunneling time is short compared to the time waited at the probed point **P**, so the QD2 occupation reaches equilibrium. Next, the system is pulsed back to the measurement point **M**, and a number of charges are isolated, fixed by the position of **P**.

On the other hand, in the lower part of the diagram, the QD2-lead tunnel coupling is too small to permit the loading of electrons inside QD2. So, in the isolated regime, we can manipulate a fixed number of loaded electrons independently of the reservoir. Furthermore, it facilitates the readout by freezing a charge configuration for a duration greater than the acquisition time.

We note that we have used here the $N_2 = 0$ state as a reference point **R**, but any state can be chosen. For example, selecting a reference state at $N_2 = 2$ displays the voltage range (H_{P1}, V_{B1}) that preserves this number of electrons (Fig. 4.2(d)).

To conclude, we have demonstrated the loading and isolation of up to 5 electrons inside QD2. In Section 4.4, we use this loading scheme to charge 4 electrons inside QD2 and then operate a 2x2 QD isolated array. In the next section, to facilitate the tuning of the isolated array, we take a step back and study the gate configurations that exhibit open double quantum-dots.

4.2.3 Open double quantum-dots regimes

As discussed previously, we aim to load an arbitrary number of electrons inside a single dot and close the reservoir's connection to manipulate those electrons inside an isolated 2x2 QD array. To this end, we have tuned QD2 as a *loading dot* where the dot occupation number can be selected at a location where its coupling to the reservoir is closed.

However, tuning the array from this loading position to a 2x2 QD array can be tedious for several reasons. First, we do not know so far if the three other QDs (QD1, QD3, QD4) exist, and if so their detunings and tunnel barriers with respect to QD2. Indeed, the array geometry is a regular matrix of metallic gates, but we focus here on the top-right part of the sample at the array's boundaries. There, the gate voltage configuration must compensate

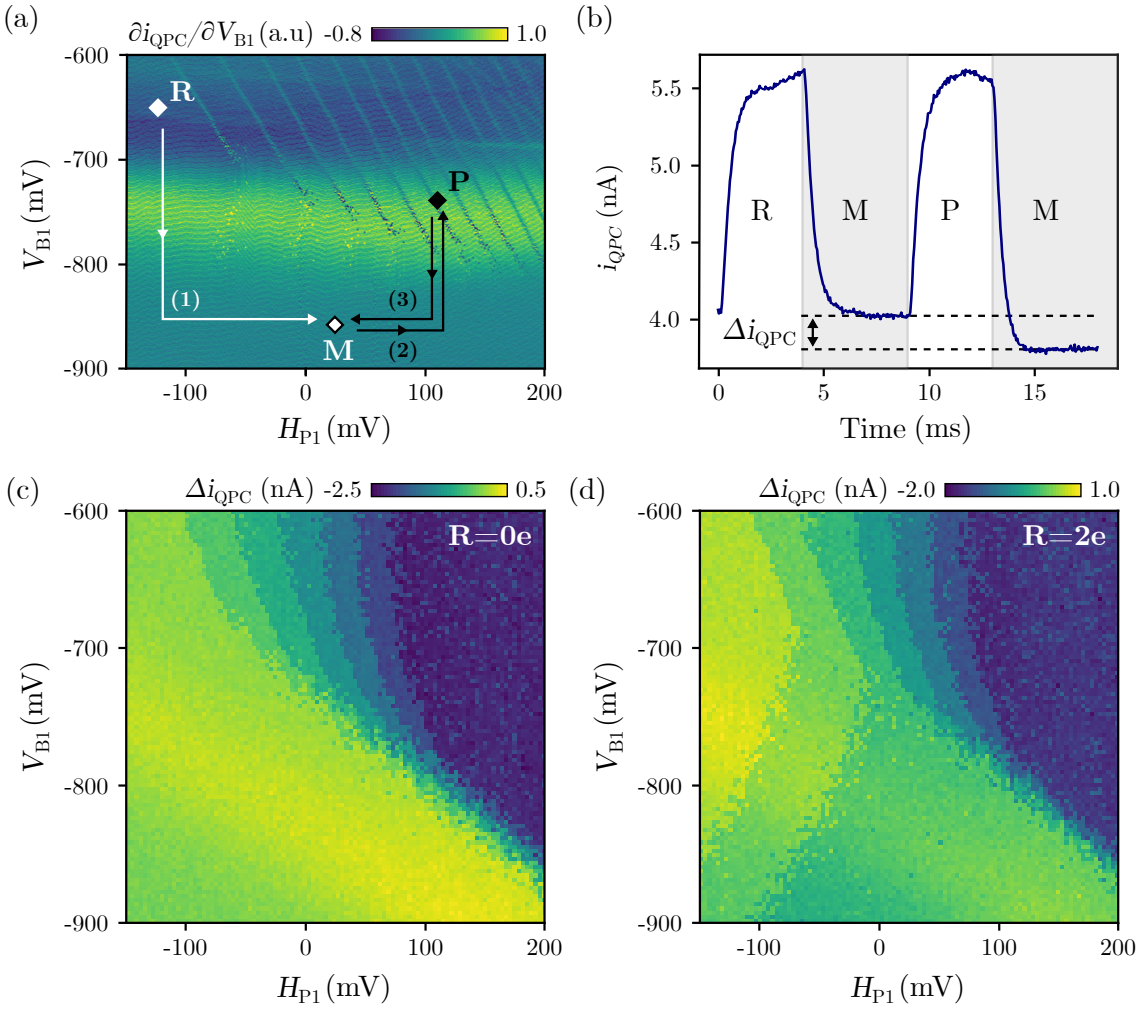

Figure 4.2: Loading scheme. (a) Loading pulse sequence. (1) The electron occupation of QD2 is set to $N_2 = 0$ at the reference point **R** by waiting 4 ms. (2) Then, the system is brought to the isolated regime, and the reference signal is recorded for 5 ms at the measurement point **M**. (3,4) This operation is repeated for all probed point **P** in the stability diagram. **(b)** Example of the detector response during the pulse sequence for a particular probed point. The difference Δi_{QPC} between the signal and reference acquisitions (respectively second and first measurements) codes the difference in QD2 occupation. The observed RC time constant is only due to the IV-converter. **(c and d)** Loading map for $N_2 = 0 \rightarrow 5$e. The value of Δi_{QPC} is plotted as a function of H_{P1} and V_{B1} for the same range as the stability diagram (a). For $V_{B1} \gtrsim 750$ mV, the QD2-lead tunneling time at the probed position **P** is short enough to allow the loading of QD2. Consequently, when the system is brought back to the measurement point, a number of charges fixed by the **P** position are isolated. The reference point **R** is set either to $N_2 = 0$e (c), or $N_2 = 2$e (d). In both cases, we do not measure any occupation number above $N_2 = 5$e. Possible explanations include loss of sensitivity of the detector and the loss of electrons when the dot is pulsed into isolation.

for the finite size of the device to achieve a symmetrical potential of 4 quantum wells. Second, we need to define a sequence of pulses to bring the device from an isolated QD2 to an isolated 2x2 QD array while preserving the number of loaded electrons. For example, if the reservoir barrier gate V_{B1} is pulsed too negatively, electrons could be pushed back to the reservoir by leaking via another part of the array.

In this section, we demonstrate the operation of two different *open* double-dots configurations, illustrated in Fig. 4.3(a) and (b) insets. From the known QD2 single-dot regime, the strategy consists of finding a polarization of the array, which allows other quantum-dots. Hence, we get an overview of how to set up the complete 2x2 QDs isolated array (see Section 4.4).

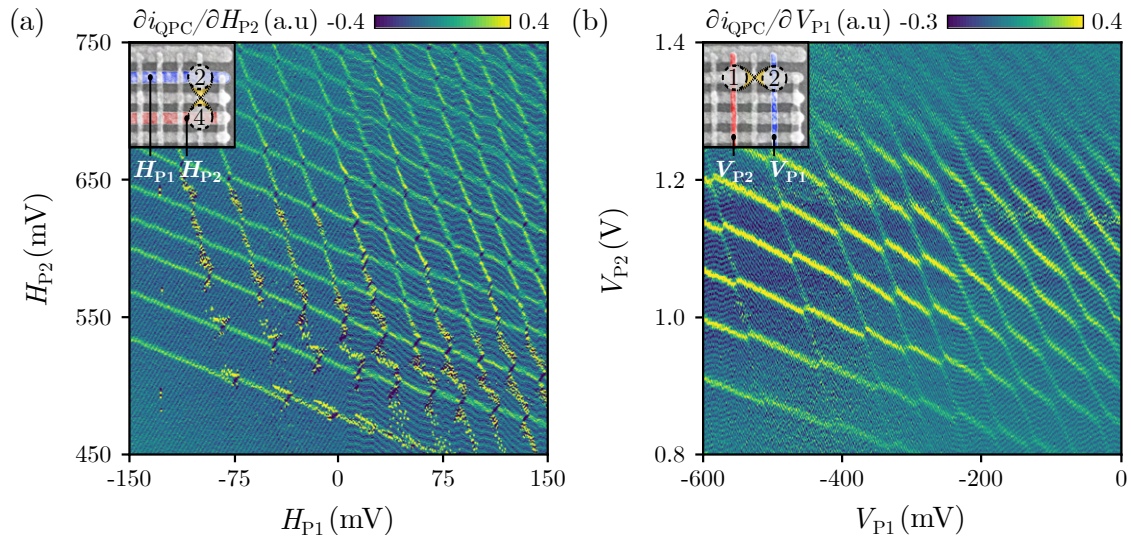

Figure 4.3: Double quantum-dots stability diagrams. (a) Stability diagram of the QD2-QD4 DQDs. Horizontal transitions (respectively vertical) are associated with QD4 (resp. QD2). A regular honeycomb pattern demonstrates that both dots exist and can exchange electrons. Stochastic charge jumps are visible for QD2 only. It indicates that the tunneling rate to the lead is stronger for QD4 than for QD2. **(b)** Stability diagram of the QD1-QD2 DQDs. Horizontal transitions (respectively vertical) are associated with QD2 (resp. QD1). While a honeycomb pattern is visible at the bottom left of the diagram, we see that for large values of V_{P1} and V_{P2} both dots merge into a bigger single dot. **Insets:** device configurations.

In Figure 4.3(a), we show a stability diagram representing a regular honeycomb pattern, characteristic of a double quantum-dots (see Sec. 1.4.1). Here, the vertical degeneracy lines are associated with the addition of electrons in QD2, while the horizontal ones are related to QD4. In the lower left part of the diagram, we see stochastic charge jumps linked to the QD2-lead transitions. It indicates that, surprisingly, the QD2-lead tunnel coupling is weaker than the QD4-lead tunnel coupling in this regime. It is due to the strong QPC polarization of S_{R}, which depletes the 2DEG nearby QD2. Therefore, in the stability diagram Fig. 4.1, QD4 has been carefully tuned to be empty to inject electrons into QD2 only in the loading procedure.

Similarly, we find a voltage configuration where the array hosts a QD1-QD2 double quantum-dots (Fig. 4.3(b)). Yet, while the QD1-QD2 stability diagram shows a honeycomb

pattern at the lower-left half, we can see in the upper-right corner that both dots merge into a bigger single-dot (see Fig. 1.10 for a similar transition). So, in this regime, the polarization of the vertical plungers V_{P1} and V_{P2} affects not only the QD1-QD2 detuning, but also the position of the dots and their coupling.

Finally, we compare the voltages applied to the different gates controlling the DQDs. First, we see that, despite featuring honeycomb patterns with similar aspect-ratios, the gate H_{P1}, H_{P2}, V_{P1} and V_{P2} are swept on completely different voltage ranges. Indeed, we have to compensate for the uneven potential landscape due to the small size of the QD array, and the asymmetric gate geometry. For example, we apply a large voltage $H_{\mathrm{B1}} = -1.3\,\mathrm{V}$ on the wide horizontal top gate H_{B1} to form the QD array, while only $V_{\mathrm{B1}} = -0.8\,\mathrm{V}$ are applied on the rightest vertical gate V_{B1} to control the electron loading of the DQDs. Second, the voltage span applied to the horizontal gates (Fig. 4.3(a)) is two times smaller than that applied on the vertical gates (Fig. 4.3(b)). This difference is explained by the fact that the vertical gates belong to a metallic layer deposited on top of the horizontal gates. So, they have a reduced gate lever-arm because of the increased distance from the 2DEG and the screening by the first metallic layer. It is not possible to give a direct comparison of horizontal versus vertical gate lever-arms since the two stability diagrams are taken for rather different potential landscapes. A thorough comparison of the different gate lever-arms is presented in Sec. 4.4.2 by biasing the array in the 2x2 QD array regime.

To summarize, we have demonstrated open array configurations which exhibit double-dot behaviors (QD1-QD2 and QD2-QD4). In Section 4.4, we use this knowledge to tune the device into a 2x2 QD array in the isolated regime.

4.2.4 Conclusion

In this first section, we have introduced a quantum-dot architecture to control a 2x2 QD array in a GaAs heterostructure.

We have demonstrated the control of QD2 in a regime where it is only coupled to the reservoir. Its occupation can be changed on a wide range $N_2 = 0 \rightarrow 10$, as its tunnel coupling to the reservoir (from sub-Hz to a few tens of GHz). The charge sensing of the array has been performed via a local electrometer sensed with transport measurements. An automatic tuning scheme is implemented to ensure the sensor sensitivity and removes manual sensor operations.

Then, we develop a procedure to set QD2 in the isolated regime by closing its coupling to the reservoir. We show that we can selectively trap between 0 and 5 charges in a meta-stable position with the electrons of QD2 located above the Fermi sea.

Finally, double quantum-dots connected to the reservoir have been demonstrated with QD2-QD4, and QD1-QD2. These experiments will be particularly useful to tune the 2x2 QD array in the isolated regime.

To prepare the operation of the isolated 2x2 QD array in Sec. 4.4, we develop in the next section a simulator for stability diagrams in the isolated regime and detail the operation scheme of the array.

4.3 Simulation of isolated stability diagrams using the constant interaction model

In the previous section, we have used the QD array to form (i) a single-dot capable of trapping electrons into the isolated regime, and (ii) different double quantum-dots open to the reservoir. The isolated regime greatly reduces the array tuning complexity and produce simpler stability diagrams than the *open* regime. We use this technique to operate a 2x2 QD array in Section 4.4. Nevertheless, we need a model to validate the measured data analysis and extract physical quantities.

In this section, we develop a simulation for stability diagrams using the constant interaction model introduced in Sec. 1.2.1 for a single-dot. First, we define a model for a double quantum-dots in the isolated regime and show how to extract meaningful properties of the system, directly from the stability diagrams. Second, we detail the simulation entries for the full 2x2 QD array.

4.3.1 Stability diagram of DQDs in the isolated regime

Here, we seek to calculate stability diagrams for a double quantum-dot and deduce interesting quantities from them. A scheme of a such DQD toy model, in the constant interaction picture, is presented in Fig. 4.4(a). We remind that the constant interaction model is a purely classical model that only considers the electrostatic interactions of the system. Here, two quantum dots, labelled 1 and 2, are capacitively coupled to two gates V_A and V_B through the capacitors $(C_\mathrm{A1}, C_\mathrm{A2})$ and $(C_\mathrm{B1}, C_\mathrm{B2})$. We consider the case where $C_\mathrm{A1} > C_\mathrm{A2}$ and $C_\mathrm{B1} < C_\mathrm{B2}$. In other words, the gate potential V_A has a stronger effect on dot 1 than dot 2 (respectively the opposite for V_B). In addition, both dots are capacitively and tunnel coupled by a mutual capacitance C_m, and a tunnel resistance R_m. We do not include any reservoirs and consider that a fixed number of electrons N_load has been loaded beforehand.

Simulation of stability diagrams

To produce artificial stability diagrams of this DQD system, like in Sec. 1.2.1, we start by defining the total charge $Q_{1(2)}$ on dot 1(2) with respect to the potential of the surrounding nodes,

$$\begin{aligned} Q_1 &= C_\mathrm{A1}\,(V_1 - V_\mathrm{A}) + C_\mathrm{B1}\,(V_1 - V_\mathrm{B}) + C_\mathrm{m}\,(V_1 - V_2) \\ Q_2 &= C_\mathrm{A2}\,(V_2 - V_\mathrm{A}) + C_\mathrm{B2}\,(V_2 - V_\mathrm{B}) + C_\mathrm{m}\,(V_2 - V_1)\,. \end{aligned} \tag{4.1}$$

We can write this system in the form $\vec{Q} = \boldsymbol{C}\vec{V}$ as

$$\begin{pmatrix} Q_1 + C_\mathrm{A1}\,V_\mathrm{A} + C_\mathrm{B1}\,V_\mathrm{B} \\ Q_2 + C_\mathrm{A2}\,V_\mathrm{A} + C_\mathrm{B2}\,V_\mathrm{B} \end{pmatrix} = \begin{pmatrix} C_1 & -C_\mathrm{m} \\ -C_\mathrm{m} & C_2 \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}, \tag{4.2}$$

with $C_1 = C_\mathrm{A1} + C_\mathrm{B1} + C_\mathrm{m}$ and $C_2 = C_\mathrm{A2} + C_\mathrm{B2} + C_\mathrm{m}$, the sum of all the capacitances attached to each dot. Knowing the charge vector $\vec{Q}$ and the capacitance matrix $\boldsymbol{C}$, we can now compute the total electrostatic energy of the double-dot $U = \frac{1}{2}\vec{Q}\boldsymbol{C}^{-1}\vec{Q}$ for a given

charge configuration (like in [Wie02]). Using $Q_{1(2)} = -N_{1(2)}|e|$, we have

$$U_{(N_1,N_2)}(V_\mathrm{A}, V_\mathrm{B}) = \frac{1}{2}N_1^2 E_{\mathrm{C1}} + \frac{1}{2}N_2^2 E_{\mathrm{C2}} + N_1 N_2 E_{\mathrm{Cm}} + f(V_\mathrm{A}, V_\mathrm{B}), \tag{4.3}$$

$$\begin{aligned} f(V_\mathrm{A}, V_\mathrm{B}) = &-\frac{1}{|e|}\Big\{C_{\mathrm{A1}} V_\mathrm{A}(N_1 E_{\mathrm{C1}} + N_2 E_{\mathrm{Cm}}) + C_{\mathrm{A2}} V_\mathrm{A}(N_1 E_{\mathrm{Cm}} + N_2 E_{\mathrm{C2}}) \\ &+ C_{\mathrm{B1}} V_\mathrm{B}(N_1 E_{\mathrm{Cm}} + N_2 E_{\mathrm{C2}}) + C_{\mathrm{B2}} V_\mathrm{B}(N_1 E_{\mathrm{C1}} + N_2 E_{\mathrm{Cm}})\Big\} \\ &+ \frac{1}{e^2}\Big\{E_{\mathrm{C1}}\left(\frac{1}{2}C_{\mathrm{A1}}^2 V_\mathrm{A}^2 + \frac{1}{2}C_{\mathrm{B1}}^2 V_\mathrm{B}^2 + C_{\mathrm{A1}} V_\mathrm{A} C_{\mathrm{B1}} V_\mathrm{B}\right) \\ &+ E_{\mathrm{C2}}\left(\frac{1}{2}C_{\mathrm{A2}}^2 V_\mathrm{A}^2 + \frac{1}{2}C_{\mathrm{B2}}^2 V_\mathrm{B}^2 + C_{\mathrm{A2}} V_\mathrm{A} C_{\mathrm{B2}} V_\mathrm{B}\right) \\ &+ E_{\mathrm{Cm}}\left(C_{\mathrm{A1}} V_\mathrm{A} C_{\mathrm{B2}} V_\mathrm{B} + C_{\mathrm{A2}} V_\mathrm{A} C_{\mathrm{B1}} V_\mathrm{B} + C_{\mathrm{A1}} C_{\mathrm{A2}} V_\mathrm{A}^2 + C_{\mathrm{B1}} C_{\mathrm{B2}} V_\mathrm{B}^2\right)\Big\}, \end{aligned} \tag{4.4}$$

and

$$E_{\mathrm{C1}} = \frac{e^2}{C_1}\left(\frac{1}{1 - \frac{C_\mathrm{m}^2}{C_1 C_2}}\right), E_{\mathrm{C2}} = \frac{e^2}{C_2}\left(\frac{1}{1 - \frac{C_\mathrm{m}^2}{C_1 C_2}}\right), \text{and } E_{\mathrm{Cm}} = \frac{e^2}{C_\mathrm{m}}\left(\frac{1}{\frac{C_1 C_2}{C_\mathrm{m}^2} - 1}\right). \tag{4.5}$$

With this definition, E_{C1} and E_{C2} are the charging energy of each dot. We remark that they correspond to the uncoupled dots' charging energy multiplied by a correction factor accounting the inter-dot coupling. In addition, E_{Cm} is the electrostatic coupling energy that corresponds to the change in energy of one dot when an electron is added to the other.

To produce a stability diagram like Fig. 4.4(b), we find, for different values of $(V_\mathrm{A}, V_\mathrm{B})$, the electron configuration with fixed total number of electrons (here $N_\mathrm{load} = 2$) which minimizes the total electrostatic energy.

Charging energies and lever-arm ratios

In the previous model, we have computed the energy of the system as a function of the charging energies E_{Ci}, the gate capacitances C_{Ki}, and the mutual capacitance C_m for each dot i and gate K. However, on a regular stability diagram experiment, we cannot directly access the energy of the system but only the charge state transitions locations. Likewise, we cannot directly measure the different capacitances of the system. A convenient way to describe the electrostatic properties of a quantum-dot is to know its charging energy and its gate lever-arms $\alpha_\mathrm{i}^\mathrm{K}$. Indeed, the lever-arms allow a direct conversion from the distances measured in a stability diagram's voltage space to an energy scale like the charging energy.

Here, we formally derive the relationships between these quantities and a stability diagram. To reduce the complexity of the system, we consider the case of uncoupled dots $C_\mathrm{m} = 0$. Indeed, we can show that the effect of the mutual capacitance on the isolated DQD is only to increase the total electrostatic energy, which does not affect the positions

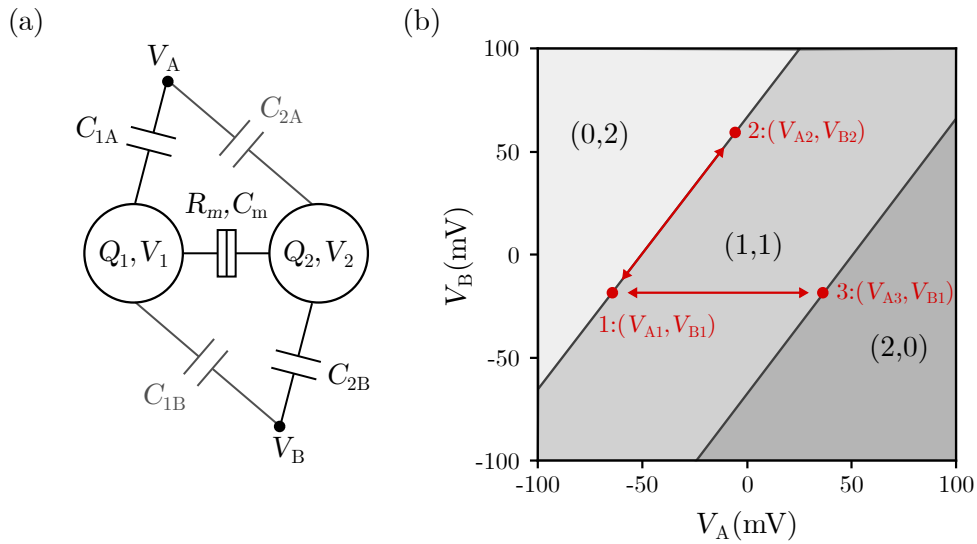

Figure 4.4: System scheme and simulated stability diagram. (a) Scheme of a double quantum-dots in the constant interaction model. Each dot (1 and 2) is coupled capacitively to gates V_A and V_B though the capacitors (C_{A1}, C_{A2}) and (C_{B1}, C_{B2}). Both dots are coupled by a mutual capacitance C_m. **(b)** Simulated stability diagram of the DQDs with $N_{load} = 2$ electrons loaded. The color codes the ground-state electron configuration labelled as (N_1, N_2). Three coordinates are highlighted and used in the main text to compute (1-2) the lever-arm ratio, and (1-3) the quantum dots charging energy.

and slopes of the charge transitions. Then, the total electrostatic energy can be simply expressed as

$$U_{(N_1,N_2)}\left(V_A,\, V_B\right) = \frac{1}{2}\sum_{i=1,2} E_{Ci}\left(-N_1 + \frac{1}{E_{Ci}}\sum_{X=A,B}\alpha_i^X V_X\right)^2. \tag{4.6}$$

First, we compute the lever-arm ratios using two points along a transition, like depicted in Fig. 4.4(b) (points 1 and 2). For each point along a charge transition, the electrostatic energy of both configurations is equal. So, for the points 1 and 2, we can write the following system

$$\begin{cases} U_{(0,2)}\left(V_{A1}, V_{B1}\right) = U_{(1,1)}\left(V_{A1}, V_{B1}\right) \\ U_{(0,2)}\left(V_{A2}, V_{B2}\right) = U_{(1,1)}\left(V_{A2}, V_{B2}\right). \end{cases} \tag{4.7}$$

The difference of the two equations gives, with $\Delta V_A = V_{A2} - V_{A1}$ and $\Delta V_B = V_{B2} - V_{B1}$,

$$\frac{\Delta V_B}{\Delta V_A} = \frac{\alpha_1^A - \alpha_2^A}{\alpha_2^B - \alpha_1^B}. \tag{4.8}$$

Thus, the slope of a charge transition gives a ratio of lever-arms. In most of our system, each plunger gate is designed to have a strong influence on only specific dots. If we consider the limit $C_{A1} \gg C_{A2}$ and $C_{B1} \ll C_{B2}$, then the slope is a direct measure of the lever-arm

ratio $\alpha_1^{\mathrm{A}}/\alpha_2^{\mathrm{B}}$.

Next, we measure the charging energies by looking at the voltage required to move electrons inside the DQD system. In Fig. 4.4(b), the points 1 and 3 correspond to the voltage cost $V_{A3} - V_{A1}$ to transfer two electrons from dot 2 to dot 1. In the same way as for Eq. 4.7, we define the system

$$\begin{cases} U_{(0,2)}\left(V_{A1}, V_{B1}\right) = U_{(1,1)}\left(V_{A1}, V_{B1}\right) \\ U_{(2,0)}\left(V_{A3}, V_{B1}\right) = U_{(1,1)}\left(V_{A3}, V_{B1}\right). \end{cases} \tag{4.9}$$

The difference of these two equations gives directly

$$V_{A3} - V_{A1} = \frac{E_{\mathrm{C1}} + E_{\mathrm{C2}}}{\alpha_1^{\mathrm{A}} - \alpha_2^{\mathrm{A}}}. \tag{4.10}$$

We remark that the voltage cost depends on the two charging energies. Indeed, in an isolated system, the total number of electrons is fixed and they can only be exchanged between the dots. In addition, we see that the stability diagram features like the transition slope and the distance between transitions are defined by ratios of either charging energies or lever-arms. For example, the diagram in Fig. 4.4(b) remains the same if we multiply by 2 the different charging energies and divide by the same amount the lever-arms. Consequently, stability diagrams can be used to extract only relative quantities and have to be paired with an energy reference scale (see Sec. 1.2.1 for possible methods).

4.3.2 Model and control protocol for the 2x2 QD array

We have developed a simulation that generalizes these calculations to any user-defined quantum-dot system. In this context, a system of m dots and n gates is parametrized by a capacitance matrix $\boldsymbol{C}$ of size $(m \times m)$ and a $(m \times n)$ lever-arm matrix $\boldsymbol{\alpha}$ of elements α_i^K. In the capacitance matrix, the off-diagonal elements C_{ij} are the opposite of the mutual capacitances between dot i and j, $C_{ij} = C_{ji} = -C_{\mathrm{m},i\leftrightarrow j}$. The diagonal elements C_{ii} correspond to the total capacitance of the dot i with respect to all the system gates and dots. They are computed using the lever-arms and mutual capacitances. In addition, a $m \times 1$ charge vector $\overrightarrow{N_0}$ takes into account the inhomogeneities in the background potential. Finally, the simulation takes as input the number of loaded electrons N_{load} and the voltages applied on each of the n gates. In the next section, we control the 2x2 QD array with the 13 gates shown in Fig. 4.1 and up to 5 loaded electrons.

Now, we have detailed in Sec. 1.4 that the control of multiple quantum-dots is complicated by the dimensionality of the charge stability volume. Here, to control the four dots' occupation in a single stability diagram experiment, we introduce a set of two virtual gates described in Fig. 4.5. We only use the plungers in pairs, $(H_{\mathrm{P1}}, H_{\mathrm{P2}})$ and $(V_{\mathrm{P1}}, V_{\mathrm{P2}})$, to tilt the voltage potential landscape of the array by applying opposite voltage offsets $(+\Delta V, -\Delta V)$. We note that if the plungers do not have a symmetrical effect on the different dots, for example $\alpha_1^{H_{\mathrm{P1}}} \neq \alpha_3^{H_{\mathrm{P2}}}$, then the tilt axis is no longer along the tunnel barrier, and asymmetries in the potential landscape are introduced. As we will see in the following, this method allows us to explore 25 of the 35 possible charge configurations of 4 electrons in 4 dots. The missing configurations are when the 4 electrons are shared in the double

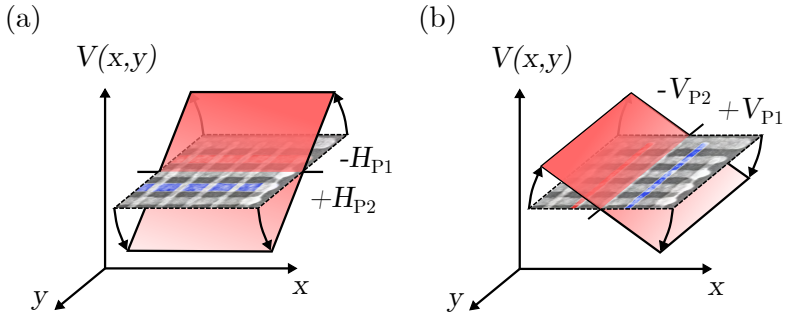

Figure 4.5: Voltage potential tilt axis. To control the 2x2 QD array occupation in a simple manner, plunger gates are associated by pair. **(a)** We apply an opposite voltage offset on H_{P1} and H_{P2} to tilt the voltage potential along H_{B2}. If the plungers do not have a symmetric effect on the different dots (e.g: $\alpha_1^{H_{P1}} \neq \alpha_3^{H_{P2}}$), then the tilt axis is no longer along H_{B2} and a global potential offset can also be added. **(b)** Similarly, V_{P1} and V_{P2} are used to tilt the voltage potential along V_{B2}.

quantum-dots along a diagonal (QD1 ↔ QD4), or (QD2 ↔ QD3) and the corresponding potential landscape cannot be defined by the combination of our two virtual gates.

4.3.3 Conclusion

In this section, we have developed a numerical model based on the constant interaction model to generate stability diagrams in the isolated regime. We have detailed the example of a double quantum-dot, and demonstrate that stability diagrams cannot extract directly charging energies and lever-arms but only ratios of these quantities. Nevertheless, we will use the ratios extracted in this simple DQD case as input parameters for the simulation of the 2x2 QD array. Indeed, we have set up the model adapted to the complete array and it contains 62 physical parameters to determine. Finally, we have defined two virtual gates to operate the array and explore its charge state volume.

4.4 Control of an isolated 2x2 quantum-dot array

In Section 4.2, we show how to trap a fixed number of electrons in QD2 within the QD array. Using this technique, we demonstrate here the control of a multi-dot system in the isolated regime. In particular, we use the model developed in the previous part to understand the experimental results and extract physical quantities along this section.

First, we load up to four electrons in the array and demonstrate the full control of a double quantum-dot by accessing the dot occupations and the inter-dot tunnel rate. Then, we move on to four electrons in the 2x2 QD array. Using the constant interaction model, we are able to reproduce and understand the intricate pattern obtained in the stability diagram. To confirm our analysis, we conclude this section by studying the isolated stability diagrams for different numbers of loaded electrons $N_{\text{load}} = 1 \rightarrow 5$.

4.4.1 Control of a double quantum-dot in the isolated regime

Here, we demonstrate the control of a double quantum-dot in the isolated regime. To form this DQD system, we introduce the dots U and B as pictured in Fig. 4.6(a) inset. Dot U

roughly corresponds to the merging of the upper dots QD1 and QD2, and dot B to QD3 and QD4. The reason is that during the sample tuning, it has been easier to start from bigger dots like dot U and B and then iteratively split them to form the 2x2 QD array developed in the next section. One possible explanation relies on the fact that, at any time, the loaded electrons must be prevented from escaping the array. In particular, the whole array gate voltage configuration must be adjusted between the loading position and the starting position of an isolated stability diagram. Thus, during these adjustments, we may unknowingly lose electrons to the reservoir. Consequently, we lower the barrier potential $V_{\mathrm{B2}} = 0\,\mathrm{V}$ to lower the chemical potential of the QD array and prevent this phenomenon.

One electron in an isolated double quantum-dot

In Figure 4.6(a), we perform a stability diagram experiment of the DQD U-B, in the isolated regime, with $N_{\mathrm{load}} = 1$ electron loaded. Along the y-axis, we sweep at the same time H_{P1} and H_{P2} in opposite directions to tilt the potential landscape, and change the detuning potential between dots U and B, as described in Fig. 4.5. For each sweep, we reset the array and re-load one electron in dot U, and then we move to an isolated position where we have further increased the barriers at the array boundaries. For ($H_{\mathrm{P1}} \simeq 0\,\mathrm{mV}, H_{\mathrm{B2}} \simeq 600\,\mathrm{mV}$), we see a transition line associated to the transfer of the loaded electron from dot U to B.

Now, the different values of the inter-dot tunnel barrier H_{B2} along the diagram x-axis have two effects on the transition. First, the transition remains almost horizontal. So, H_{B2} has a weak effect on the DQD detuning and mainly acts as an inter-dot tunnel barrier. Indeed, we see that as H_{B2} gets more positive, the inter-dot tunnel coupling increases and consequently the transition get wider and wider. At the opposite side, for $H_{\mathrm{B2}} \simeq -1.6\,\mathrm{V}$, we observe stochastic events along the sweep axis, indicating that the inter-dot tunneling time between dot U and B is reduced close to the measurement time (2ms/pt). For even more negative values $H_{\mathrm{B2}} \simeq -1.7\,\mathrm{V}$, the inter-dot transition disappears but a replica of the transition line at higher detuning is measured. It corresponds to a resonant tunneling $(1,0) \rightarrow (0,1')$, through an orbital excited state of dot B ($1'$). The excited orbital has a greater spatial extent, so the inter-dot tunneling rate is larger and electrons can tunnel faster than the measurement time. Nevertheless, we estimate that the inter-dot tunnel coupling is tunable from sub-Hz to a few tens of GHz within a 600 mV voltage range on H_{B2}.

Secondly, the transition moves not in a straight line but with a slight bending. The curvature of the charge degeneracy lines denotes a change of the gate-to-dots capacitive couplings and is a signature of dot deformations and displacements while scanning H_{B2}. This behavior cannot be grasped by the constant interaction model, where we have assumed fixed charging energies and capacitive couplings.

Finally, at the lower-right corner of Fig. 4.6(a), the voltage applied to H_{P2} is too high to keep the array isolated. For the corresponding tunnel barrier values H_{B2}, the transition is no longer visible if we reverse the sweep axis.

Four electrons in an isolated double quantum-dot

Now, we repeat the same stability diagram experiment but with $N_{\mathrm{load}} = 4$ electrons, in Fig. 4.6(b). As expected, we probe the five different charge configurations of four electrons

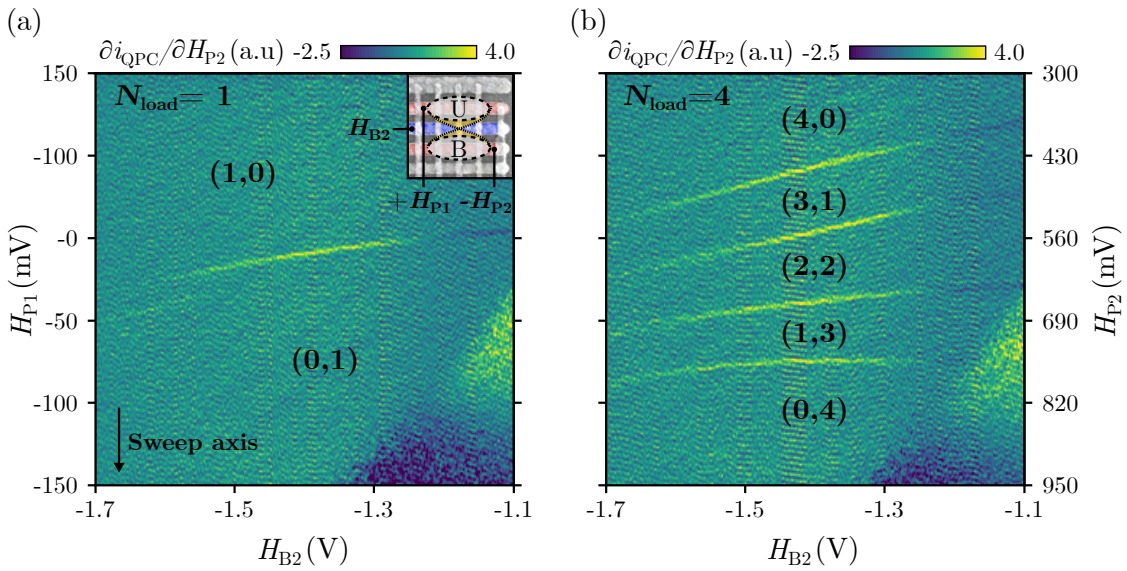

Figure 4.6: Double quantum-dot stability diagrams in the isolated regime.
(a) Isolated stability diagram of the U-B DQDs with $N_{\text{load}} = 1$ electron loaded. Along the y-axis, H_{P1} and H_{P2} are swept together to detune the DQD potential so that the dots can exchange one electron. The charge configurations are labelled as (N_U, N_B). On the x-axis, H_{B2} is used to tune the tunnel barrier between the two dots. For $H_{\text{B2}} < -1.6\,\text{V}$, the tunnel rate is reduced below the measurement time (2 ms/pt). **Inset:** device configuration.
(b) Same experiment than **(a)**, with $N_{\text{load}} = 4$.

inside a DQD along the detuning axis, and H_{B2} tunes the inter-dot tunnel barrier to the same range as before with one electron. However, we note that the (2,2) charge configuration becomes wider as H_{B2} gets more positive. It might be explained by an increase of the DQD mutual capacitance in this charge state, as the two dots get closer to each other. Anyway, the (1,0) $\rightarrow$ (0,1) charge transition is centered with respect to the (2,2) states. It shows that the positions of the dots do not depend on the number of loaded electrons.

To summarize, we have demonstrated the control of a double quantum-dot in the isolated regime. We start by loading a fixed number of electrons inside the array, using the technique developed in Section 4.2. Then, we adjust the gate voltages to form a DQD with the dot U and B, while preserving the number of electrons in the system. Through an isolated stability diagram experiment, we demonstrate the control of the electron distribution and the inter-dot tunnel coupling of the DQD. In particular, we show the possibility of closing the inter-dot tunnel coupling.

4.4.2 Control of 4 electrons in a 2x2 QD array

In the previous part, we have developed a double quantum-dot with 4 electrons trapped in the isolated regime. Likewise, we show in this section the control over the dot occupation of the 2x2 QD array. First, we perform an isolated stability diagram that exhibits the control of the array with 4 electrons. Then, we analyze experimental results with the constant

interaction model developed in Section 4.3.

Experimental results

To reach the 2x2 QD array regime, we start by iteratively applying a more negative voltage on the vertical inter-dot tunnel barrier, starting from the previous stability diagram with $V_{\mathrm{B2}} = 0\,\mathrm{V}$. Consequently, we gradually split the quantum-dots U and B until we reach a regime with 4 dots. This process is done in several steps, so that we can adjust the complete array voltage configuration.

For $V_{\mathrm{B2}} = -1.7\,\mathrm{V}$, we reach the situation where the four dots are populated and can exchange electrons, as depicted in Fig. 4.7(a). On this diagram, we tilt the voltage potential along the y-axis sweep so that electrons can be exchanged between the top (QD1, QD2) and the bottom (QD3, QD4) quantum-dots. For each sweep, we reset the array, re-load 4 electrons, and change the detuning between the left (QD1, QD3) and right (QD2, QD4) part of the array. This is achieved by applying an opposite voltage offset between V_{P1} and V_{P2}, as pictured in Fig. 4.5(b).

On this diagram, we see different kinds of charge transitions, with different slopes and line intensities. We note that we cannot access the leftmost part of the diagram at $V_{\mathrm{P2}} > 1025\,\mathrm{mV}$. For these voltage configurations, the QD array is no more isolated from the reservoir. Nevertheless, we can sort the different charge transitions by slope and line intensity.

On the one hand, the transition slope gives us information on the type of inter-dot transition concerned. Indeed, we link vertical transition lines to electron exchange between the left and the right part of the array, and respectively horizontal transitions to exchanges between the upper and lower part. However, due to the symmetries of the device, an electron jumping from QD3 to QD1 would have a transition slope similar to an electron exchanged between QD4 and QD2. This is also the case for "horizontal" jumps between QD1 and QD2, or QD3 and QD4.

On the other hand, the transition line intensity allows us to distinguish which specific inter-dot is concerned since it is related to the detector sensitivity for this particular exchange of electrons. In our case, the detector is not symmetrically coupled to each dot, thus the line intensity gives an additional information. For example, an electron exchanged between QD2 and QD4 gives a much stronger signal than between QD1 and QD3, since these two last dots are 200 nm further away from the sensor.

Using both methods, we summarize in Fig. 4.7(b) the different inter-dot transitions among the stability diagram and associate one color to each. Then, we need to deduce the charge distribution of each charge state. To do this, we start from the rightest part of the diagram where the potential is completely tilted toward the right part of the array. In this regime, the system can be summarized to a simple double quantum-dot QD2-QD4, as studied in Section 4.4.1. Consequently, we can easily identify these charge states starting from the bottom-right corner $\left(\begin{smallmatrix} 0 & 0 \\ 0 & 4 \end{smallmatrix}\right)$, where we label the dot occupations as $\left(\begin{smallmatrix} N_1 & N_2 \\ N_3 & N_4 \end{smallmatrix}\right)$. Likewise, we label the charge states consistent with a double quantum-dot QD3-QD4 in the lower part of the stability diagram. Finally, we can map the complete stability diagram by propagating the known charge states through already identified charge transitions, see Fig. 4.7(b).

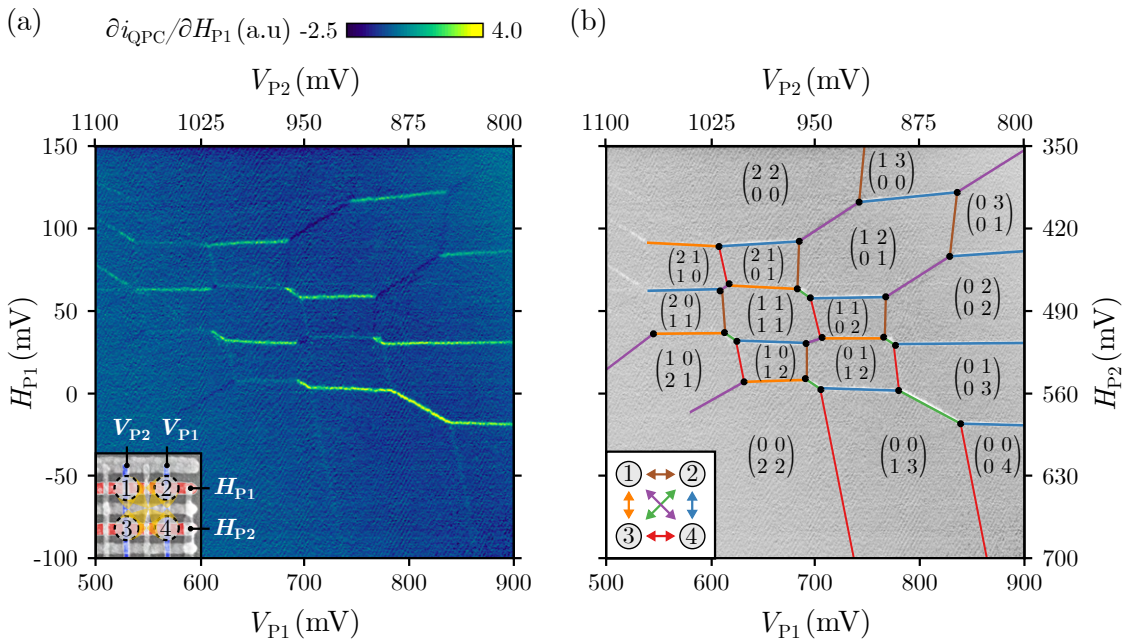

Figure 4.7: 2x2 quantum-dot array with 4 electrons in the isolated regime. **(a)** Isolated stability diagram of the 2x2 quantum-dot array with $N_{\text{load}} = 4$ electrons loaded. H_{P1}, and H_{P2} are swept along the y-axis to exchange electrons between the top (QD1, QD2) and the bottom quantum-dots (QD3, QD4). Similarly, V_{P1} and V_{P2} are stepped along the x-axis to transfer electrons from the left (QD1, QD3) to the right (QD2, QD4) part of the array. **Inset:** device configuration. **(b)** Schematic of the stability diagram (a). A color is associated with each transition based on its slope and intensity. Each color corresponds to a given inter-dot transition as depicted in figure **inset**. The charge state labels are deducted by starting from the right part of the diagram, in the limit where the array is reduced to a double quantum-dot QD2-QD4.

Among the different charge configurations, we are particularly interested in the $\left(\begin{smallmatrix}1&1\\1&1\end{smallmatrix}\right)$ state. The 1-electron in each dot state is located at the center of the whole stability diagram and is a center of symmetry for the charge transitions pattern. Now, we can discuss how the charges are re-distributed inside the array when we move away from this state. First, if we move up on the y-axis, we notice that we cannot jump directly from $\left(\begin{smallmatrix}1&1\\1&1\end{smallmatrix}\right)$ to $\left(\begin{smallmatrix}2&2\\0&0\end{smallmatrix}\right)$. Instead, only one electron jumps from QD3 to QD1 when the voltage potential is titled. Indeed, due to the mutual capacitance between QD1 and QD2, once we have added an electron to QD1, the QD2 chemical potential rises. We need to push further along the y-axis to pay for the additional mutual charging energy. In addition, the $\left(\begin{smallmatrix}2&1\\0&1\end{smallmatrix}\right)$ state is preferred due to a slight asymmetry in the tilt axis. Symmetrically, we now move down the y-axis from the 1-electron state, and the first transition corresponds to the $\left(\begin{smallmatrix}1&0\\1&2\end{smallmatrix}\right)$ state. Finally, the QD array behave similarly along the x-axis with the transitions $\left(\begin{smallmatrix}1&1\\1&1\end{smallmatrix}\right) \rightarrow \left(\begin{smallmatrix}1&1\\0&2\end{smallmatrix}\right) \rightarrow \left(\begin{smallmatrix}0&2\\0&2\end{smallmatrix}\right)$. In all of these cases, we should be able to tune the charge states surrounding the 1-electron state by adjusting the tilt of the potential landscape (as it has been demonstrated using the simulations developed in the next section).

To summarize, we have demonstrated the control of four electrons inside a 2x2 quantum-dot array. Even if we couldn't access all the possible charge configurations, we have reached the $\left(\begin{smallmatrix}1&1\\1&1\end{smallmatrix}\right)$ state. From this state, we have identified charge transitions to push selected electrons into already occupied dots. Such a protocol can be used in the context of experiments related to electron spins. Nevertheless, the use of the isolated regime and the device geometry give clear stability diagrams. We are able to catalog the different charge states thanks to specific features like horizontal, vertical, and oblique transition lines with different sensor sensitivities.

Analysis using the constant-interaction model

In this part, we push further our investigations on the isolated stability diagram with 4 electrons distributed in 4 quantum-dots using the simulation developed in Sec. 4.3 to model the 2x2 QD array.

The simulation takes as input a model of the QD array and generates a stability diagram with the same voltage ranges than Fig. 4.7, with $N_{\text{load}} = 4$. To fix the starting values for the different model parameters, we make reasonable estimations based on (i) the symmetries of the system, (ii) the constrains on the lever-arm matrix and dot charging energies obtained by using Eq. 4.8 and 4.10 on the DQD limits of the experimental stability diagram (lower and right part of the diagram). Then, we manually adjust all the model parameters iteratively to reproduce as closely as possible the measured stability diagram.

At the end of this procedure, we find a model of the 2x2 QD array that simulates a stability diagram in qualitative agreement with the experimental data, as pictured in Fig. 4.8(a). We see that the constant interaction model matches the overall shape of the stability diagram. Also, we confirm the labeling of the different charge states in Fig. 4.7(b), using the simulation outputs. Moreover, we can use the simulation to probe a larger voltage window. It results that the two tilted potentials used to explore the stability diagram can access 25 charge states out of the 35 possible ways of distributing four electrons into four dots. The 10 missing charge states correspond to the case where the array is limited to diagonal DQDs like QD1-QD4, and QD2-QD4. They fit to the configurations $\left(\begin{smallmatrix}x&0\\0&4-x\end{smallmatrix}\right)$, and $\left(\begin{smallmatrix}0&x\\4-x&0\end{smallmatrix}\right)$ with $x \in \{0;1;2;3;4\}$.

Now, we analyze the lever-arm matrix used in the QD array model and represented in Fig. 4.8(b) (the complete list of parameters can be found in Appendix C). Since we do not have an energy reference scale, we normalize each lever-arm by $\alpha_4^{H_{\text{P2}}} \simeq 53\,\text{meV/V}$, the estimation of the H_{P2} lever-arm on QD4.

On the one hand, it was necessary to assign a lever-arm about twice as strong for the horizontal gates than the vertical gates to reproduce the experimental data (as already mentioned in Sec. 4.2.3). It results from the vertical plunger potentials screening by the horizontal set of gates located in-between the vertical gates and the two-dimensional electron gas. Moreover, the vertical gates are positioned 15 nm further from the 2DEG, resulting in an additional reduction of their lever-arms. It confirms the need to apply significant positive voltages to V_{P1} and V_{P2}, made possible by the isolating layers of hafnium oxide.

On the other hand, we can compare the different plungers' effect on the dots directly below with their effects on the dots on a different row/column. For example, if we look

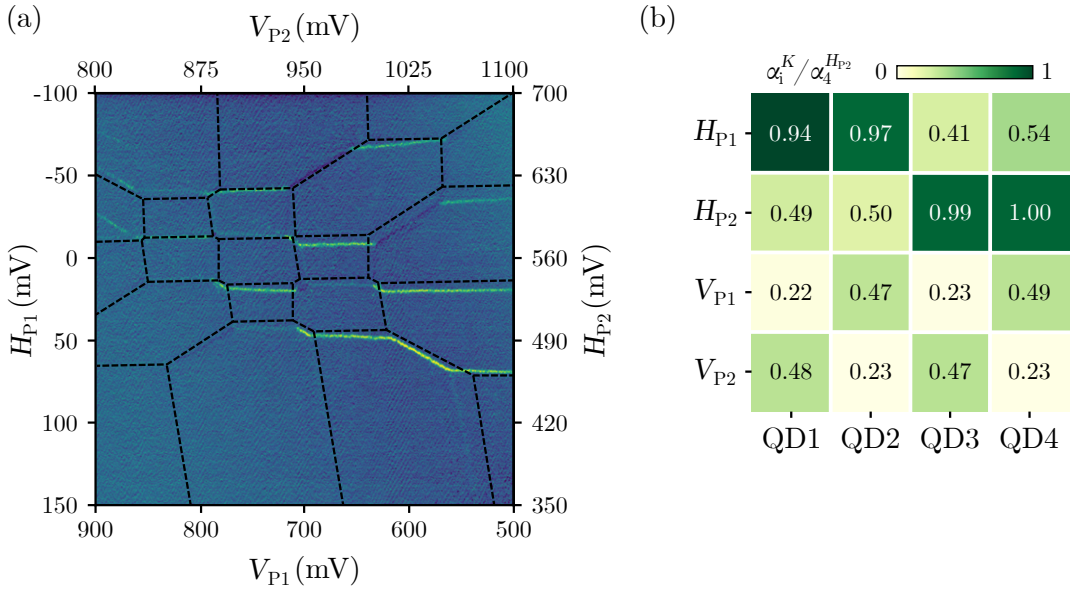

Figure 4.8: Constant interaction model of the 2x2 quantum-dot array.
(a) Simulated stability diagram of the 2x2 QD array with 4 electrons loaded (dashed black lines), superimposed on the experimental data. The constant interaction model allows reproducing the experimental data qualitatively. **(b)** Representation of the lever-arm matrix used in the simulation model. In the absence of absolute energy reference, each lever-arm is normalized by $\alpha_4^{H_{P2}}$, the H_{P2} lever-arm on QD4.

at the H_{P1} lever-arms, it has roughly a twice more significant effect on QD1 and QD2, compared to QD3 and QD4. It is also the case for the other three gates studied. We note that this discussion is only valid for the current polarization of the inter-dot tunnel barrier H_{B2}, and V_{B2}, because a decrease in their gate voltages might move the dots further apart, and therefore reduce these cross-capacitive couplings. Moreover, such crosstalk between the shared control gates and their surrounding dots is not necessarily a problem for large scale QD arrays, as discussed in Sec. 1.4.4 and in [Mor18]. Indeed, the structure's symmetries facilitate the compensation of the crosstalk, so the requirements concern more the uniformity of the crosstalk along one gate. Here, our device has shown enough tunability to explore the stability diagram.

To conclude, we have developed a model of the 2x2 QD array in the regime where we have trapped and controlled $N_{\text{load}} = 4$ electrons. We use this model to characterize the array and quantify the effects of the different plunger gates. Our structure with two layers of control gates shows that the bottom layer has a effect twice stronger than the upper one. It can be explained by screening of the upper layer by the bottom one and the increased distance of the upper layer from the 2DEG. Finally, we examined the crosstalk between a shared control gate and the neighboring dots. In our small array, this crosstalk has been homogenous enough to explore all the different charge states. In the next section, we confirm our analysis by studying the charge stability volume associated with different

loading numbers $N_{\text{load}} = 1 \rightarrow 5$.

4.4.3 Arbitrary number of electrons in a 2x2 QD array

To confirm the model of the 2x2 QD array that we have developed in the previous section, we perform the same stability diagrams than before, but for different numbers of loaded electrons in Fig. 4.9. Then, we compare the experimental data with the results of our simulations. Only the N_{load} parameter is changed in the simulation parameters, and all other quantities (lever-arms, charging energies, ...) are the same than for the diagram in Fig. 4.8.

For $N_{\text{load}} = 1$, we explore the four charge states of the stability volume with the electron in any of the four dots (see Fig. 4.9(a)). We expect the four charge states to form a unique 4-fold degenerated crosspoint, for a perfectly symmetric array. Here, we observe that this degeneracy is lifted due to the diagonal transition $\left(\begin{smallmatrix} 0 & 0 \\ 0 & 1 \end{smallmatrix}\right) \leftrightarrow \left(\begin{smallmatrix} 1 & 0 \\ 0 & 0 \end{smallmatrix}\right)$. The asymmetries in the lever-arm matrix and charging energies explain why the QD1-QD4 transition is promoted instead of QD2-QD3 for this particular cut in the stability diagram volume. This behavior was already observed in the isolated stability diagram with 4 electrons by looking for example to the $\left(\begin{smallmatrix} 0 & 2 \\ 0 & 2 \end{smallmatrix}\right)$ state. For this symmetric state ($N_1 = N_3$, and $N_2 = N_4$), it is much easier to transfer one electron from QD4 to QD1 than from QD3 to QD2. The numerical simulations agree with the experimental results and replicate the promoted diagonal transition properly. Moreover, this stability diagram gives the path to make the electron travels in the four QDs in a loop. A similar path has been used in Flentje *et al.* [Fle17] to displace coherently individual electron spins in three QDs.

In Figure 4.9(b), this particular cut of the stability diagram volume contains 9 of the 10 charge states of $N_{\text{load}} = 2$ electrons into 4 dots. The state $\left(\begin{smallmatrix} 0 & 1 \\ 1 & 0 \end{smallmatrix}\right)$ is missing here also because of the asymmetries between the DQDs QD1-QD4 and QD2-QD3. The configuration with two electrons in four dots corresponds to the scalable QD array described in [Li18], where only one in two QDs is occupied. The *sparse* occupation of the QDs has several advantages over the full array occupation (four electrons in four dots) detailed in the previous section. First, it increases the number of electrodes per QD for the same gate density. Furthermore, the crosstalk between each gate and the surrounding QDs is reduced since their distance increases. Finally, the empty sites permit new functionalities like shuttling electrons from one QD to another without interacting with another occupied QD.

Next, we investigate the stability diagram with $N_{\text{load}} = 3$ electrons loaded. Out of the 20 charge states in the stability volume, only 16 are represented in the stability diagram in Fig. 4.9(c). In Dehollain *et al.* [Deh20], Nagaoka ferromagnetism has been observed in a 2x2 QD array with 3 electrons. It requires to set resonant the four 1-electron per dot states to observe the Nagaoka ferromagnetism. However, the QD array is operated in the *open* regime, and its stability diagrams are complicated by the unwanted addition of electrons from the reservoir (see Fig. 1.14). Here, the tuning capability of the array is increased by the isolated regime.

Finally, we show the charge stability diagram of $N_{\text{load}} = 5$ electrons in an isolated 2x2 QD array. The number of states in the full stability volume grows to 56. Our cut in the stability volume contains 36 of these states, and only 22 are visible in the stability diagram in Fig. 4.9(d).

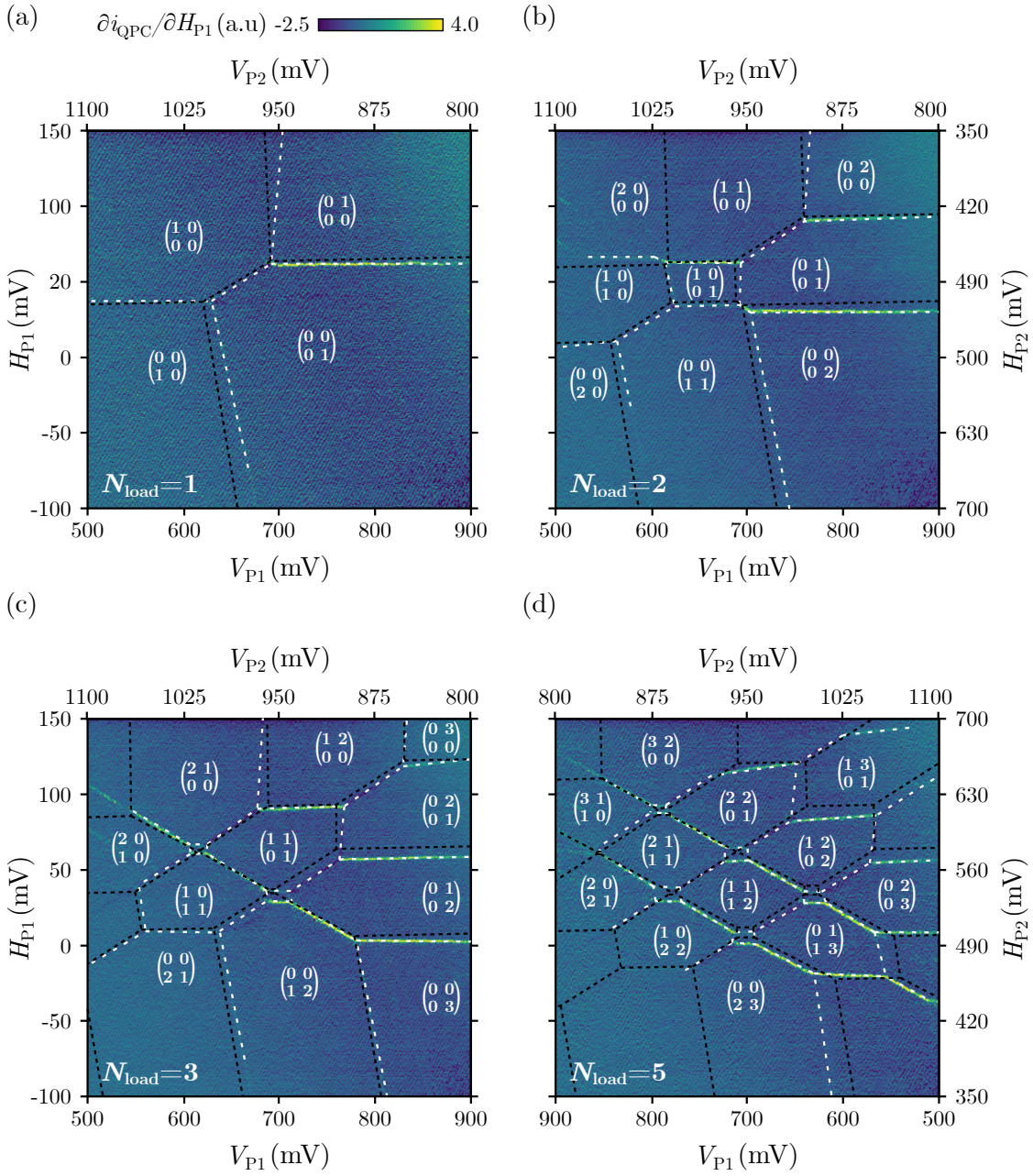

Figure 4.9: 2x2 isolated quantum-dot array with $N_{\mathrm{load}} = 1 \rightarrow 5$.
Isolated stability diagram of the 2x2 quantum-dot array with $N_{\mathrm{load}} = 1 \rightarrow 5$ electrons loaded, using the same experimental parameters than in Fig. 4.7(a). The charge transitions observed (simulated) are highlighted with white (black) dashed lines, and the different charge states are labeled. The simulated stability diagrams are all using the same model of the QD array, developed in Fig. 4.8.

To summarize, we have demonstrated that any electron number $N_{\text{load}} = 1 \rightarrow 5$ can be loaded into our isolated QD array and manipulated. The model of the 2x2 QD array developed in Sec. 4.4.2 remains valid for these different electron numbers and reproduce the observed stability diagrams correctly.

4.5 Conclusion

In this chapter, we demonstrate the charge control of a 2x2 quantum-dot array. First, we study the link between the array and the electron reservoir. A loading procedure is detailed to trap electrons inside the array and reach the isolated regime. Different double quantum-dot configurations are explored to better understand the tuning of the full QD array. Then, we develop a numerical simulation to compute stability diagrams in the isolated regime with as input a representation of the QD array in the constant interaction model. Based on limited approximations, we show how to extract some of the model parameters directly from the experimental data. Finally, multi-dot experiments are performed in the isolated regime. The control of a double-quantum dot is achieved with the tuning of the dot occupations and its inter-dot tunnel barrier. Moreover, we perform an isolated stability diagram experiment with a 2x2 QD array and 4 electrons loaded, and a model of the array is obtained by comparison with the simulations. We show that the scalable architecture of the device is capable of reaching the desired charge states. Our model's robustness is demonstrated by looking at the same stability diagrams for different numbers of loaded electrons.

Following this work, further investigations are required to take control of larger quantum-dot arrays. In particular, a new generation of devices based on the same architecture are being fabricated. These devices will benefit from experience feedback from the current thesis. They will optimize, for example, the sensitivity of the sensor and the screening of the top metallic layer (vertical gates) by the bottom one (horizontal gates). Moreover, the tuning protocols of quantum-dot arrays are still an open question, and the new devices will allow to test control paradigms on large arrays. Finally, a project in the group aims to add micro-magnets on top of an array to operate it as a spin-qubit quantum processing unit.

Conclusion and perspectives

The goal of my thesis was the development of charge control in quantum-dot arrays and the exploration of architectures compatible with large-scale integration. Indeed, quantum computers are prone to errors and require encoding information from a single *logical* quantum-bit into many *physical* qubits. Electron-spin qubits in quantum-dot arrays are a promising platform thanks to their compatibility with standard semiconductor manufacturing. So, scalable QD arrays are one of the pre-requisites for building a universal quantum computing unit, fitting millions of QDs inside a single chip, to outperform any conventional computer on specific tasks.

Towards this objective, we first demonstrated the operation of double quantum-dots in a silicon nanowire. Each QD is operated by a unique electrode, and the device is fabricated on a silicon-on-insulator 300-mm wafer using an industry-standard fabrication line. We have developed a structure-integrated electrometer by probing the quantum capacitance of a single-lead quantum-dot. The SLQD detector reduces the footprint for charge readout by requiring only one reservoir. Its charge sensitivity has been characterized to $4.9 \times 10^{-3}\, e/\sqrt{\mathrm{Hz}}$. In addition, we evaluated the energy spectrum of the QDs and showed that they are highly sensitive to the surface disorder at the interface between the electrode and the dot. Then, we developed different detection protocols to compensate for the device's strong capacitive couplings due to its dense packing. We have achieved the control of the different double quantum-dots in a 2x2 QD array and probed the Coulomb disorder inside the structure. In particular, the Coulomb disorder strongly affects the quantum-dots homogeneity in the few-electron regime but is smoothed as we increase the dot sizes.

Then, we demonstrated a scalable QD array formed by shared control gates with row/column addressing, in a GaAs/AlGaAs heterostructure. Similar to classical integrated circuits, large-scale quantum-dot arrays must drastically reduce the number of interconnects. Here, the crossbar network limits the number of electrodes for a NxN QD array to only $4N$. We have observed the loading and trapping of one to five electrons inside a single-dot. Then, a double quantum-dot was studied in the isolated mode with the control of the electrons distribution and the inter-dot tunnel coupling. In particular, we have shown the ability to reduce the inter-dot tunneling rate from the GHz to the sub-kHz regime. Finally, despite the limited number of electrodes, we have controlled the electrons' distribution in the isolated 2x2 QD array for different numbers of charge loaded. The constant interaction model was used to characterize the QD array and reproduce the isolated stability diagrams.

To conclude, further developments are needed for the control of large-scale quantum-dot arrays. On the one hand, a robust silicon platform requires low dot-to-dot variability, and a means to control the inter-dot tunnel barriers. The optimization and automation of the measurement protocols developed in this thesis make it possible to efficiently evaluate

silicon nanowire's properties at cryogenic temperature.

On the other hand, progress is required concerning the control of large arrays using the GaAs platform for proof of concept row/column addressing. An in-depth study of the dots' charging energies and couplings to electrodes is necessary to assess the QD network's homogeneity precisely. Furthermore, we could not demonstrate the tunability of tunnel-barriers in the 2x2 QD array during this thesis. Moreover, increasing the array's size would permit to confirm the scaling potential of this architecture and demonstrate parallel operations of QDs.

Besides, the *coarse tuning* of large-scale arrays remains an open problem. Here, we have manually explored the ten dimensions of the charge stability volume to find the regime with four electrons in four dots. Next, we have identified the different charge states in the final stability diagram using the transitions' slopes and the diagram's symmetries. However, this strategy cannot scale with the size of the array, as the diagram's complexity grows exponentially. Therefore, we must rely on automatic procedures. While the automatic tuning of simple DQDs is based on recognizing honeycomb patterns, this solution may not be effective for performing coarse tuning of large systems with a colossal number of charge states to identify. Consequently, new control paradigms must be developed.

Finally, the charge control inside a scalable QD array is only one facet of our quantum computer proposal. In addition, the control of electron-spin qubits in a 3x3 QD array has been shown [Mor18]. The two electrons were moved coherently across the lattice, and exchange oscillations performed in the different DQD configurations. Also, the realization of a quantum coherent link between two distant DQDs has been recently demonstrated with electron-spins transported with surface acoustic waves [Jad20]. Instead of considering a unique large QD array, such links could be used to connect multiple smaller arrays, as proposed in [Van17].

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APPENDIX A

Silicon nanowire room-temperature characterization

This appendix details the room-temperature characterization of the 4 split-gates silicon nanowire used in Chapter 3.

In Figure A.1(a), we show the current measured between the source and drain contacts while sweeping all the gates on one side at the same time. The gates from the other side are kept blocked by applying -1 V. For example, the red curve corresponds to sweeping the gate voltages (V_5,V_6,V_7,V_8) from -1 to 1 V (upper-side), while (V_1,V_2,V_3,V_4) prevent the current from flowing through the bottom-side of the device (see Figure A.1(a) inset). As expected, the split-gate device acts like a field-effect transistor at room-temperature and is turned ON when we apply a common gate voltage above a given threshold V^{th}.

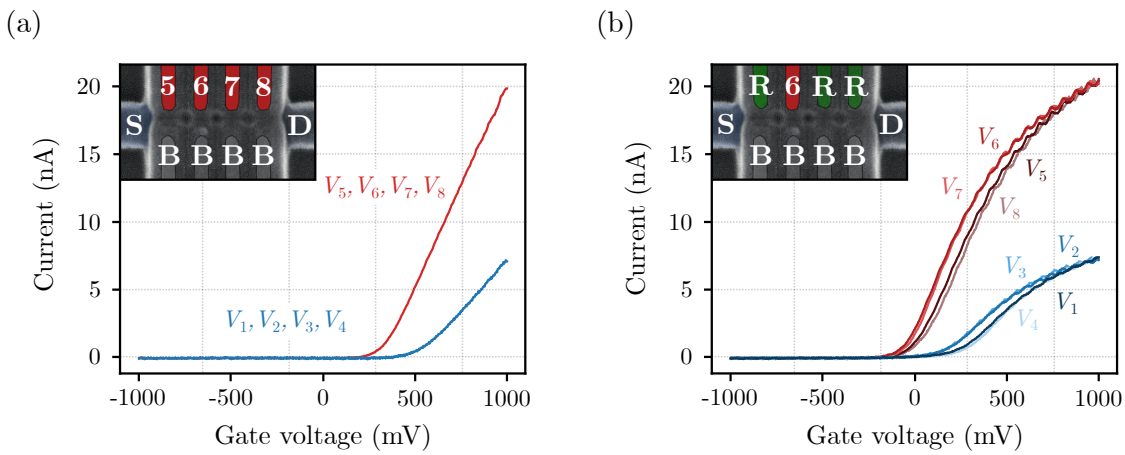

Figure A.1: Room-temperature characterization. Current measured between the source and drain reservoirs of the 4 split-gates silicon nanowire for different gate configurations at room-temperature ($T \simeq 300$ K). The source-drain bias is fixed at $V_{\mathrm{SD}} = 5$ mV. **(a)** Transport current through the nanowire as a function of the gate voltage applied simultaneously on all the gates on one side of the nanowire, while the other side is held blocked (**B**) by applying -1 V. The blue trace corresponds to the lower-side (V_5,V_6,V_7,V_8), and the red to the upper-side (V_1,V_2,V_3,V_4). **(inset)** Device configuration to measure current through the nanowire upper-side. **(b)** Current through the nanowire as a function of the voltage applied to each of the gates. To allow current to flow through the nanowire while only one gate is swept, all the other gates from the same side act like reservoirs (**R**) by applying 1 V. The other side remains blocked. **(inset)** Device configuration to characterize the gate voltage V_6.

We see that the upper-side is activated for a lower voltage $V_{\mathrm{U}}^{\mathrm{th}} = 310\,\mathrm{mV}$ compared to the lower-side $V_{\mathrm{L}}^{\mathrm{th}} = 510\,\mathrm{mV}$. Moreover, we extract the resistance value of the transistor in the linear-regime from the slope of the IV characteristics. The resistance of the lower-side $R_{\mathrm{L}} = 660\,\mathrm{M\Omega}$ is twice that of the upper-side $R_{\mathrm{U}} = 340\,\mathrm{M\Omega}$. It indicates that the lower-side gates are less effective than the upper-side in modulating the carrier density in the nanowire. This asymmetry is explained by a misalignment of the split-gates with respect to the nanowire axis during the fabrication process. It was measured on similar devices and observed using scanning electron microscopy, as depicted in Fig. A.2 where the electrodes offset $\Delta \simeq 20\,\mathrm{nm}$ is relatively large compared to the nanowire width $W = 70\,\mathrm{nm}$.

From these measurements, we expect lower lever-arms for the lower side electrodes on the silicon nanowire QDs, at cryogenic temperatures. In Chapter 3, we measure the lever-arms in different configurations and see that the misalignment of the electrodes does not affect the dot-gate lever-arm if the QD is pinned to the corner of the nanowire.

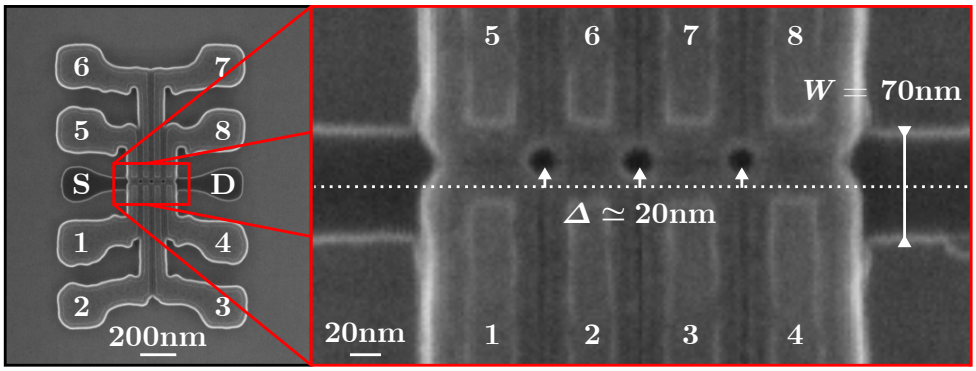

Figure A.2: Split-gates misalignment on the silicon nanowire. (left panel) SEM micrograph of a 4 split-gates device similar to the one used in Chapter 3. **(right panel)** Zoom into the central part of the device with the split-gates deposited on top of the horizontal silicon nanowire. The split-gates are misaligned by $\Delta \simeq 20\,\mathrm{nm}$ with respect to the axis of the nanowire. This offset is not-negligible compared to the nanowire width $W = 70\,\mathrm{nm}$.

Next, we check that each gate is working correctly in Fig. A.1(b). To allow current to flow through the device while a single gate is swept, we accumulate electrons under the electrodes on the same side that the gate under test. For example, the inset in Fig. A.1(b) depicts the device configuration to test the gate V_6. The gate V_6 is swept as electrons are accumulated below V_5, V_7 and V_8 by applying $1\,\mathrm{V}$. The lower-side is biased at $-1\,\mathrm{V}$ to prevent accumulation in the bottom branch. We note that the asymmetry between the lower and upper gates is reproduced in this configuration, as in Fig. A.1(a). In addition, we see that the gates on the edges have a higher threshold voltage than the gates in the middle of the device : $V_1^{\mathrm{th}}, V_4^{\mathrm{th}} > V_2^{\mathrm{th}}, V_3^{\mathrm{th}}$; and $V_5^{\mathrm{th}}, V_8^{\mathrm{th}} > V_6^{\mathrm{th}}, V_7^{\mathrm{th}}$. Indeed, due to the cross-capacitive couplings, the inner gates are assisted by two electrodes, and the edge gates only by one.

To conclude, this characterization is easy to implement at room-temperature for the pre-screening of silicon nanowire devices worthy of investigations at $70\,\mathrm{mK}$. For the device used in Chapter 3, we have measured an asymmetry between the upper and the lower gates. It is explained by an offset of the electrodes with respect to the axis of the nanowire.

APPENDIX B

Addition energy spectrum of silicon nanowires quantum-dots

Here, we show the stability diagrams used to measure the addition energy spectrum of four silicon QDs spanned in three different devices. The addition energy spectrums are summarized in Fig. 3.3. The three devices parameters are :

Device A : $W = 80\,\text{nm}$, $L_G = 40\,\text{nm}$, $S_H = 40\,\text{nm}$, $S_V = 40\,\text{nm}$.
Device B : $W = 90\,\text{nm}$, $L_G = 50\,\text{nm}$, $S_H = 50\,\text{nm}$, $S_V = 50\,\text{nm}$.
Device C : $W = 100\,\text{nm}$, $L_G = 60\,\text{nm}$, $S_H = 60\,\text{nm}$, $S_V = 60\,\text{nm}$.

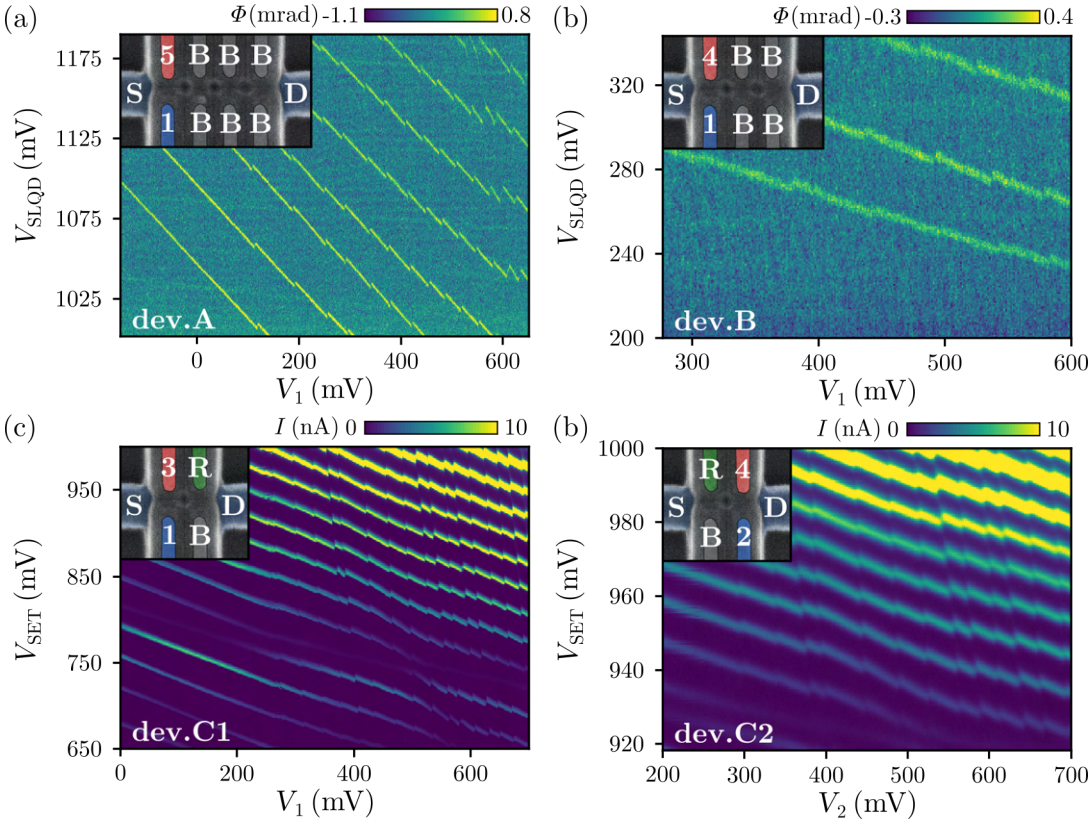

Figure B.1: Stability diagrams for addition energy spectrums. List of the stability diagrams from which the addition energy spectrum has been measured. **(a)** Device A. The QD5 is used as an SLQD to probe QD1. **(b)** Device B. The QD4 is used as an SLQD to probe QD1 **(c)** Device C. QD3 is used as a SET sensor to probe QD1. The QD4 acts like a local reservoir by applying 1 V to permit the current to flow between the source and drain contacts. **(d)** Device C. Same than (c), but QD2 is probed by QD4.

APPENDIX C

Constant interaction model of the 2x2 QD array

In this appendix, we show the parameters used in the simulations of the 2x2 QD array (see Sec. 4.4). First of all, we implement in our model only the electrodes swept in the different stability diagram experiments : H_{P1}, H_{P2}, V_{P1}, and V_{P2}. The other gates (H_{B1}, $V_{\mathrm{B1}}, ...$) were not swept in the 2x2 QD array regime, and therefore we can not evaluate their lever-arms with respect to the quantum-dots. Thus, we limit the lever-arm matrix to just four gates with four dots. In our experiments, the static gates have the effect of shifting the chemical potential of each dot. These offsets are included in the simulations within the charge vector $\overrightarrow{N_0}$, which is accounting for the background potential.

Secondly, we discard the mutual capacitance terms, namely $\forall i \neq j, C_{\mathrm{m},i\leftrightarrow j} = 0$. Indeed, we assume that the QDs are in the weak-coupling regime, which is consistent with the experimental data. So, the contributions of the mutual terms in the dot capacitance are small : $e^2/E_{\mathrm{C},i} \gg C_{\mathrm{m},i\leftrightarrow j}$, and $E_{\mathrm{C},i} \simeq e^2/C_i$. In this regime, the mutual capacitances have almost no effect on the simulated diagrams, and therefore we neglect them to simplify the model.

We summarize the parameters that best match the experimental data in Table C.1. We recall that the simulations do not give an energy reference scale, so any combination that keeps $\boldsymbol{\alpha}\overrightarrow{E_{\mathrm{C}}}$ constant produces the same stability diagram. Here, we chose to set the lever-arms of the horizontal gates (e.g. H_{P1}) on their associated dots (e.g. QD1 and QD2) to 50 meV/V, the characteristic lever-arm in such structure [Mar14]. The charging energies obtained are of the order of ~ 1 mV, and are compatible with the expected values for the device (see Sec. 1.2.2).

Table C.1: Constant interaction model parameters of the 2x2 QD array.

	α_i^{K}(meV/V)				$E_{\mathrm{C},i}$ (meV)	$N_{0,i}$
	H_{P1}	H_{P2}	V_{P1}	V_{P2}		
QD1	49.5	25.7	11.4	25.2	1.63	2.73
QD2	51.3	26.4	24.9	12.2	1.70	4.28
QD3	21.3	52.2	11.9	24.8	1.63	−4.88
QD4	28.2	52.6	25.6	12.1	1.75	−2.28

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