Design of an integrated high-voltage low-power isolated DC/DC converter for automotive applications

Etienne Foray

Etienne Foray. Design of an integrated high-voltage low-power isolated DC/DC converter for automotive applications. Electronics. Université de Lyon, 2021. English. NNT : 2021LYSEI043 . tel-03405711

HAL Id: tel-03405711
https://theses.hal.science/tel-03405711
Submitted on 27 Oct 2021

N°d'ordre NNT : **2021LYSEI043**

THESE de DOCTORAT **DE L'UNIVERSITE DE LYON**
opérée au sein de
Institut National des Sciences Appliquées de Lyon

Ecole Doctorale N° EDA160
ELECTRONIQUE, ELECTROTECHNIQUE, AUTOMATIQUE

Spécialité / discipline de doctorat :

Génie Electrique

Soutenue publiquement le 20/07/2021, par :
Etienne Foray

Design of an integrated high-voltage low-power isolated DC/DC converter for automotive applications

---

Devant le jury composé de :

Ben Dhia, Sonia	Professeur des Universités	INSA Toulouse	Présidente
Lembeye, Yves	Professeur des Universités	Grenoble INP	Rapporteur
Wicht, Bernhard	Professeur des Universités	Leibniz University	Rapporteur
Alonso, Corinne	Professeur des Universités	LAAS-CNRS	Examinatrice
Prodic, Aleksandar	Professeur des Universités	University of Toronto	Examinateur
Allard, Bruno	Professeur des Universités	INSA Lyon	Directeur de thèse
Martin, Christian	Professeur des Universités	Univ. Lyon 1 - UCBL	Encadrant

Département FEDORA – INSA Lyon - Ecoles Doctorales

SIGLE	ECOLE DOCTORALE	NOM ET COORDONNEES DU RESPONSABLE
CHIMIE	**CHIMIE DE LYON** **https://www.edchimie-lyon.fr** Sec. : Renée EL MELHEM Bât. Blaise PASCAL, 3e étage secretariat@edchimie-lyon.fr	**M. Stéphane DANIELE** C2P2-CPE LYON-UMR 5265 Bâtiment F308, BP 2077 43 Boulevard du 11 novembre 1918 69616 Villeurbanne **directeur@edchimie-lyon.fr**
E.E.A.	**ÉLECTRONIQUE, ÉLECTROTECHNIQUE, AUTOMATIQUE** **https://edeea.universite-lyon.fr** Sec. : Stéphanie CAUVIN Bâtiment Direction INSA Lyon Tél : 04.72.43.71.70 secretariat.edeea@insa-lyon.fr	**M. Philippe DELACHARTRE** INSA LYON Laboratoire CREATIS Bâtiment Blaise Pascal, 7 avenue Jean Capelle 69621 Villeurbanne CEDEX Tél : 04.72.43.88.63 **philippe.delachartre@insa-lyon.fr**
E2M2	**ÉVOLUTION, ÉCOSYSTÈME, MICROBIOLOGIE, MODÉLISATION** **http://e2m2.universite-lyon.fr** Sec. : Sylvie ROBERJOT Bât. Atrium, UCB Lyon 1 Tél : 04.72.44.83.62 secretariat.e2m2@univ-lyon1.fr	**M. Philippe NORMAND** Université Claude Bernard Lyon 1 UMR 5557 Lab. d'Ecologie Microbienne Bâtiment Mendel 43, boulevard du 11 Novembre 1918 69 622 Villeurbanne CEDEX **philippe.normand@univ-lyon1.fr**
EDISS	**INTERDISCIPLINAIRE SCIENCES-SANTÉ** **http://ediss.universite-lyon.fr** Sec. : Sylvie ROBERJOT Bât. Atrium, UCB Lyon 1 Tél : 04.72.44.83.62 secretariat.ediss@univ-lyon1.fr	**Mme Sylvie RICARD-BLUM** Institut de Chimie et Biochimie Moléculaires et Supramoléculaires (ICBMS) - UMR 5246 CNRS - Université Lyon 1 Bâtiment Raulin - 2ème étage Nord 43 Boulevard du 11 novembre 1918 69622 Villeurbanne Cedex Tél : +33(0)4 72 44 82 32 **sylvie.ricard-blum@univ-lyon1.fr**
INFOMATHS	**INFORMATIQUE ET MATHÉMATIQUES** **http://edinfomaths.universite-lyon.fr** Sec. : Renée EL MELHEM Bât. Blaise PASCAL, 3e étage Tél : 04.72.43.80.46 infomaths@univ-lyon1.fr	**M. Hamamache KHEDDOUCI** Université Claude Bernard Lyon 1 Bât. Nautibus 43, Boulevard du 11 novembre 1918 69 622 Villeurbanne Cedex France Tél : 04.72.44.83.69 **hamamache.kheddouci@univ-lyon1.fr**
Matériaux	**MATÉRIAUX DE LYON** **http://ed34.universite-lyon.fr** Sec. : Yann DE ORDENANA Tél : 04.72.18.62.44 yann.de-ordenana@ec-lyon.fr	**M. Stéphane BENAYOUN** Ecole Centrale de Lyon Laboratoire LTDS 36 avenue Guy de Collongue 69134 Ecully CEDEX Tél : 04.72.18.64.37 **stephane.benayoun@ec-lyon.fr**
MEGA	**MÉCANIQUE, ÉNERGÉTIQUE, GÉNIE CIVIL, ACOUSTIQUE** **http://edmega.universite-lyon.fr** Sec. : Stéphanie CAUVIN Tél : 04.72.43.71.70 Bâtiment Direction INSA Lyon mega@insa-lyon.fr	**M. Jocelyn BONJOUR** INSA Lyon Laboratoire CETHIL Bâtiment Sadi-Carnot 9, rue de la Physique 69621 Villeurbanne CEDEX **jocelyn.bonjour@insa-lyon.fr**
ScSo	**ScSo*** **https://edsciencessociales.universite-lyon.fr** Sec. : Mélina FAVETON INSA : J.Y. TOUSSAINT Tél : 04.78.69.77.79 melina.faveton@univ-lyon2.fr	**M. Christian MONTES** Université Lumière Lyon 2 86 Rue Pasteur 69365 Lyon CEDEX 07 **christian.montes@univ-lyon2.fr**

*ScSo : Histoire, Géographie, Aménagement, Urbanisme, Archéologie, Science politique, Sociologie, Anthropologie

Contents

List of Figures

List of Tables

Acknowledgments

First of all, many thanks to my supervisors from Ampère Laboratory, Bruno Allard and Christian Martin, for their scientific and moral support during the whole project, that went through many unexpected developments. Thank you for your numerous advice and ideas during all the PhD activity that allowed to complete it successfully.

Then, I would like to thanks the company members from the site of Milano, that made possible this PhD project in the first place. Thank you Giovanni, Maurizio, Nicola, Roberto and all the others for your trust. Thank you also to the company employees in France (Dominique and Stéphane) for your kind help. Finally, many thanks to the people from Freising site (Michael and Oliver) who supervised the project that they join partway through.

Among the other Ampère Laboratory members, I'd like to thank Pascal Bevilacqua. Thank you for your help with the fabrication of the many prototypes we created during this activity. Thank you also to administrative staff, in particular Sandrine and Michelle, for your precious help during the various steps of the PhD.

Finally, I want to thank all the lab members, especially from Vinci and Omega buildings with whom we shared coffee, lunch and many happy moments. Thank you for your encouragements and for the happy mood in the laboratory.

Thanks to my family, my friends and my girlfriend for your continuous support and the energy you brought me that allowed to bring this project to a successful end.

Finally, many thanks to the reviewers, B. Wicht, Y. Lembeye, S. Ben Dhia, C. Alonso and A.Prodic, for accepting to evaluate the PhD thesis and for their relevant comments and ideas.

Remerciements

Pour commencer, un très grand merci à mes encadrants du laboratoire Ampère, Bruno Allard et Christian Martin, pour leur soutien scientifique et moral pendant ce projet qui a connu de nombreux rebondissements ! Merci pour vos nombreux conseils et vos idées tout au long du projet qui ont permis à la thèse d'arriver jusqu'à cette fin heureuse.

Ensuite, je souhaite également remercier les personnes de l'entreprise du site de Milan qui ont rendu possible ce projet de thèse. Merci à Giovanni, Maurizio, Nicola, Roberto et les autres de m'avoir accordé votre confiance. Je veux aussi remercier les membres de l'entreprise en France (Dominique et Stéphane) pour leur aide très précieuse. Pour finir, merci aux personnes du site de Freising (Michael et Oliver) pour avoir superviser le projet qu'ils ont repris en cours de route.

Parmi les autres membres du laboratoire Ampère, je voudrais remercier en particulier Pascal Bevilacqua, pour m'avoir aider lors de la création des nombreux prototypes réalisés pendant cette thèse et pour ton précieux soutien technique. Merci également aux personnels administratifs, notamment Sandrine et Michelle pour votre aide tout au long du projet.

Enfin je tiens à remercier tous les autres membres du laboratoire, notamment des bâtiments Vinci et Oméga, avec qui nous avons partagé le repas, le café et pleins de bons moments ! Merci pour vos encouragements et pour la bonne humeur qui régnait au laboratoire.

Un grand merci à ma famille, mes amis et ma copine pour leur soutien infaillible et pour l'énergie qu'ils m'ont apportés qui m'ont permis de mener à bien ce projet de thèse.

Enfin, merci aux rapporteurs, B. Wicht et Y. Lembeye et aux examinateurs, S. Ben Dhia, C. Alonso et A. Prodic, pour avoir accepter d'évaluer mes travaux de thèse et pour leurs retours très pertinents et bienveillants.

Abstract

In the current context of energy and ecological transitions, a multiplication of high-voltage DC buses is observed in several applications, such as Electric Vehicles (EV) and photovoltaic. In parallel, there exist systems that require to be powered directly from the main supply source, like a Pyroswitch for immediate security in the automotive context. It is an actuator whose role is to physically disconnect the high-voltage battery of an EV in case of a crash and that must be powered directly from the high-voltage battery (of which voltage is close to 400 V or even 800 V nowadays) for the sake of reliability. In this perspective an isolated DC/DC converter with a high-input voltage capability and a low-power, low-voltage output is required. Strong constraints appear on the specifications of this converter, due to the automotive context, in particular regarding its size, cost and efficiency.

The approaches used today to design such a converter yield a low diversity in the proposed solutions. Most of them are based on a similar power stage architecture, that can be interesting in a low-cost perspective, but that shows some limitations in terms of performances (low maximum input voltage, low efficiency). Therefore, the design of an 800V-to-12V converter with an output power rating close to 1W cannot rely on a classical approach, especially considering the high efficiency targeted ($> 85\%$).

The approach that is proposed in this work may be based on: an on-chip integration of an increased number of components of the DC/DC converter; and/or "power modules" created when assembling several discrete components. The thesis aims at using the benefits from both approaches to create the targeted converter. In particular, the integration of the active components allows to reassess the architecture of the power stage and to increase the frequency at which it may operate, enabling a size reduction in the passive components of the converter. However, the limits from the integration technology do not allow generally to target the integration of the bulkiest devices of the converter (e.g. the transformer) thus a special attention is paid to their design.

The manuscript first presents an exploration of topologies of the power stage for the considered isolated DC/DC converter. The most interesting solutions are compared based on a few qualitative criteria and an architecture whose trade-off between size and performances seems the most suitable is identified: the multi-level flying-capacitor. The design of an integrated circuit (IC) is then described. A solution is considered to overcome the limitations of the selected integration technology (high-voltage bulk Silicon) with respect to device-to-device isolation. Then, the design methodology of a custom planar transformer suitable for high-voltage, low-power applications is introduced and several transformer designs are proposed and tested inside the complete converter. Finally, the converter is built using the various bricks created previously and the efficiency of the power stage is measured. The results of the best transformer designs are in-line with the specifications and offer a clear improvement with respect to state-of-the-art solutions, especially for the efficiency.

Résumé

Dans le contexte actuel de transitions écologique et énergétique, une multiplication des bus DC haute-tension est observée dans certaines applications telles que les véhicules électriques ou le photovoltaïque. En parallèle, certains systèmes requièrent d'être alimentés directement à partir de la source principale d'énergie : pour l'automobile, l'exemple du Pyroswitch peut être cité. Il s'agit d'un actionneur dont le rôle est de déconnecter physiquement la batterie haute-tension du véhicule électrique en cas d'accident et qui, pour des raisons de sécurité, doit être alimenté directement par la batterie principale (dont la tension aujourd'hui est proche de 400 V voire 800 V). Ainsi naît le besoin d'un convertisseur DC/DC isolé avec une forte tension d'entrée et une faible tension et puissance en sortie. De fortes contraintes liées au contexte (notamment automobile) sont placées sur le convertisseur, en termes de coût, de taille et de rendement.

Les convertisseurs actuellement disponibles sur le marché ou dans la littérature montrent une faible diversité des solutions proposées. Ils sont majoritairement basés sur une architecture similaire, qui bien qu'économique, présente de sérieuses limites en termes de performances (faible tension maximale et faible rendement). Ainsi, le design d'un convertisseur 800V-12V avec une puissance proche de 1W en sortie ne peut se satisfaire des approches utilisées classiquement, en particulier au vu du haut niveau de rendement visé (> 85%).

L'approche proposée dans cette thèse se base sur deux des principales techniques utilisées pour créer des convertisseurs de puissance : l'intégration sur puce (ou au sein d'un même package) de plus en plus d'éléments du convertisseur ; et les « modules de puissance » qui assemblent une série de composants discrets. Cette thèse propose donc d'allier les avantages de chacune de ces techniques pour créer le convertisseur voulu. En particulier, l'intégration des composants actifs permet une remise en question de l'architecture de l'étage de puissance du convertisseur ainsi qu'une augmentation significative de la fréquence de fonctionnement, qui devrait contribuer à la diminution de la taille des composants passifs. Cependant, les limites des technologies d'intégration ne permettent pas de viser l'intégration des éléments les plus volumineux du convertisseur, comme le transformateur, et une attention toute particulière est donc portée à leur dimensionnement.

Dans cette thèse, une étude de différentes topologies pour l'étage de puissance du convertisseur DC/DC isolé est d'abord menée. Elle permet d'identifier les structures les plus prometteuses en comparant un nombre limité de critères qualitatifs. Une topologie est retenue compte tenue d'un bon compromis entre performances et complexité : les convertisseurs multi-niveaux à capacités flottantes. La création d'un circuit intégré (IC) permettant l'intégration des éléments actifs de l'étage de puissance est ensuite présentée. Une solution est présentée pour contourner les limites imposées par la technologie choisie (Bulk Silicium haute-tension) en termes d'isolation entre composants. Ensuite, une méthodologie de conception d'un transformateur planaire adapté au contexte et à l'application est introduite afin de prendre en compte les principaux paramètres de dimensionnement d'un tel composant. À l'issue de cette étape, quelques transformateurs sont proposés pour être mesurés au sein du convertisseur complet. Enfin, les différentes composantes du convertisseur sont assemblées et des mesures de rendement sont réalisées sur plusieurs points de fonctionnement proches de ceux définis par l'application. Les résultats des transformateurs les plus performants sont à la hauteur des attentes et offrent une nette amélioration des performances par rapport aux solutions de l'état-de-l'art, notamment en termes de rendement.

Résumé étendu

Cette partie du manuscrit présente un résumé étendu de la thèse en français.
This portion presents an extended summary of the PhD thesis in french.

Introduction

Dans le contexte actuel de transitions écologique et énergétique, une multiplication des bus DC haute-tension est observée dans certaines applications telles que les véhicules électriques ou le photovoltaïque. En parallèle, certains systèmes requièrent d'être alimentés directement à partir de la source principale d'énergie : pour l'automobile, l'exemple du Pyroswitch peut être cité. Il s'agit d'un actionneur dont le rôle est de déconnecter physiquement la batterie haute-tension du véhicule électrique en cas d'accident et qui, pour des raisons de sécurité, doit être alimenté directement par la batterie principale (dont la tension aujourd'hui est proche de 400 V voire 800 V). Ainsi nait le besoin d'un convertisseur DC/DC isolé avec une forte tension d'entrée et une faible tension et puissance en sortie. De fortes contraintes liées au contexte (notamment automobile) sont placées sur le convertisseur, en termes de coût, de taille et de rendement.

L'approche proposée dans cette thèse se base sur deux des principales techniques utilisées pour créer des convertisseurs de puissance : l'intégration sur puce (ou au sein d'un même boitier) de plus en plus d'éléments du convertisseur ; et les « modules de puissance » qui assemblent une série de composants discrets. Cette thèse propose donc d'allier les avantages de chacune de ces techniques pour créer le convertisseur voulu. En particulier, l'intégration des composants actifs permet une remise en question de l'architecture de l'étage de puissance du convertisseur ainsi qu'une augmentation significative de la fréquence de fonctionnement, qui devrait contribuer à la diminution de la taille des composants passifs. Cependant, les limites des technologies d'intégration ne permettent pas de viser l'intégration des éléments les plus volumineux du convertisseur, comme le transformateur, et une attention toute particulière est donc portée à leur dimensionnement.

Cadre et objectifs de la thèse

Pour créer un cadre plus concret dans lequel vont s'inscrire les travaux effectués durant cette thèse, un cahier des charges présentant les principales caractéristiques souhaitées pour le convertisseur DC/DC isolé est pris en compte. Pour la tension d'entrée, deux valeurs sont retenues qui correspondent aux principaux bus de tension utilisés dans les véhicules électriques de nos jours (400 V et 800 V). Une plage de ±25% de variation de la tension d'entrée est considéré. Le reste des caractéristiques sont communes : 12 V et 1 W en sortie, une isolation galvanique entre l'entrée et la sortie du convertisseur et un rendement global supérieur ou égal à 85%.

Pour tenter d'apporter une solution satisfaisante au problème de départ, plusieurs aspects de la conception de l'étage de puissance convertisseur sont étudiés :

- Choix de la topologie de l'étage de puissance
- Conception d'un Circuit Intégré pour les composants actifs
- Conception d'un transformateur sur mesure (composant difficile à intégrer et volumineux)

Structure du manuscrit

Le Chapitre 1 se concentre sur une exploration des topologies pour l'étage de puissance. Un rapide résumé des solutions existantes est présenté et leurs faiblesses sont analysées. Une comparaison basée sur un petit nombre de critères qualitatifs de quelques structures est construite et une architecture candidate est sélectionnée.

Dans le Chapitre 2, deux versions de la topologie choisie sont présentées, leur comportement et leurs formes d'ondes sont analysés. Un premier prototype d'un convertisseur haute-tension basse-puissance est construit en utilisant des composants discrets pour valider l'analyse et souligner les potentielles difficultés rencontrées pour créer une solution avec les performances voulues.

Le Chapitre 3 est dédié à la conception d'un circuit intégré qui inclut la partie "active" de l'étage de puissance. Les objectifs du circuit intégré sont introduits et les principales limitations de la technologie d'intégration choisie sont identifiées. La solution proposée pour contourner la limite en terme d'isolation entre composants est décrite et la conception de chacun des principaux blocs internes est discutée au travers de résultats de simulation et de mesures expérimentales.

Le Chapitre 4 propose une méthodologie pour concevoir un transformateur adapté aux convertisseurs haute-tension basse-puissance. L'approche pour la conception de cet élément clé du convertisseur est tout d'abord décrite (Plan d'Expériences). Elle permet d'étudier l'influence d'un nombre restreints de paramètres de dimensionnement et, au final, de sélectionner les transformateurs les plus prometteurs.

Les résultats expérimentaux du convertisseur construit sont présentés dans le Chapitre 5. La fonctionnalité du convertisseur est validée et ses performances sont mesurées pour divers transformateurs et points de fonctionnement. Les résultats sont comparés à ceux obtenus avec les solutions existantes, pour conclure sur l'intérêt de l'approche choisie.

Au final, la conclusion générale revient sur les principales contributions de la thèse. Une brève analyse de la viabilité de la solution introduite est proposée et quelques perspectives d'amélioration sont discutées.

Chapitre 1 : Exploration de topologies

Ce chapitre présente une exploration de différentes topologies pour l'étage de puissance du convertisseur DC/DC isolé haute-tension basse-puissance visé. Un rappel des caractéristiques importantes d'un convertisseur DC/DC est d'abord effectué, puis certaines solutions existantes positionnées dans la même gamme de tension/puissance sont étudiées. Il apparait que la faiblesse de ces solutions est lié en partie à l'architecture Flyback, très souvent utilisée pour les convertisseurs basse-puissance isolés. Ainsi, une étude est menée pour identifier des topologies alternatives adaptées à l'application, en se basant sur un petit nombre de critères qualitatif. Les avantages et inconvénients de diverses structures sont discutés puis une comparaison entre-elles est effectuée. Au final, une topologie est choisie pour une première itération de la phase de conception du convertisseur.

État de l'Art

Rappels sur les convertisseurs DC/DC

Un convertisseur DC/DC est un système qui convertie une source continue d'alimentation vers un autre domaine de tension. Pour les applications visées, le convertisseur doit transformer un bus de tension DC en une source basse-tension basse-puissance pour pouvoir être directement utilisable pour un petit actionneur ou un capteur.

Un convertisseur est un assemblage de plusieurs briques qui misent ensemble forme un système complet. L'étage de puissance est une brique importante, car c'est lui qui opère la conversion de tension voulue, mais d'autres blocs sont aussi requis pour le filtrage, le contrôle ou la protection du convertisseur. Cependant, ces travaux ne se concentrent que sur l'étage de puissance c'est pourquoi le dimensionnement des autres blocs n'est pas discuté en détail dans ce manuscrit.

Parfois, une isolation est nécessaire entre l'entrée et la sortie du convertisseur DC/DC, pour éviter qu'une perturbation qui toucherait un côté du convertisseur ne se transmette de l'autre côté. Différents types d'isolations existent, l'une des plus répandue étant l'isolation galvanique, pour laquelle un transformateur est requis et c'est celle requise par l'application visée. Cette étude portera donc seulement sur les convertisseurs dits isolés, qui possèdent donc une isolation galvanique entre leur entrée et leur sortie.

Certains composants sont presque toujours présents au sein de l'étage de puissance, comme les interrupteurs de puissance, les transformateurs ou les redresseurs. La manière d'arranger ces composants pour créer l'étage de puissance est appelée la "topologie" du convertisseur. Il existe des topologies "classiques" avec des caractéristiques connues. Définir la topologie du convertisseur est une étape importante du processus de dimensionnement, car elle a une influence sur le nombre de composants requis par le convertisseur, mais également sur leur taille, leur caractéristiques électriques etc. De telle sorte que la topologie du convertisseur va en partie décider des performances de celui-ci. Les performances et les caractéristiques qui peuvent être utilisées pour décrire un convertisseur sont nombreuses, mais certaines sont communes à tous les convertisseurs et sont donc introduites ci-dessous.

- **Tensions d'entrée et de sortie**

  Les composants requis pour créer un convertisseur donné dépendent très largement des tensions d'entrée et de sortie de celui-ci. Par exemple, les interrupteurs de puissance ou les condensateurs possèdent une tension maximale à ne pas dépasser (et qui dépend de leur technologie de fabrication) qui fixe donc des limites pour la tension maximale acceptée en entrée. La tension crée en sortie du convertisseur dépend de la topologie de l'étage de puissance, qui doit donc être choisie en conséquence. Ici, la principale contrainte est liée à la tension d'entrée qui peut monter jusqu'à 1 kV, ce qui impose un fort stress aux composants.

- **Puissance**

  Les convertisseurs sont en générale conçus pour une gamme de puissance donnée, car celle-ci influence grandement le dimensionnement des composants de l'étage de puissance. En effet, les contraintes thermiques sur ces composants déterminent une limite haute de la puissance maximale que le convertisseur peut fournir. Cependant, l'application visée ici requière une puissance en sortie faible et ces contraintes thermiques ne sera donc pas centrale pour le choix des composants.

- **Rendement et pertes**

  Enfin, une des caractéristiques les plus importantes d'un convertisseur et qui permet d'évaluer ses performances est le rendement. Il est calculé en effectuant le ratio de la puissance fournie en sortie du convertisseur et de la puissance qu'il consomme. Les pertes au sein du convertisseur qui influencent le rendement sont dues à différents phénomènes et liées aux différents composants du convertisseur. Par exemple, les pertes par conduction (ou par effet Joule) et les pertes à la commutation seront notamment déterminées par les interrupteurs de puissance ainsi que par les redresseurs. Le transformateur pourra également générer des pertes par conduction mais surtout des pertes au sein du matériau magnétique (pertes fer).

Solutions existantes

Pour mieux appréhender la conception du convertisseur visé, il est intéressant de regarder ce que les solutions existantes permettent, pour essayer de comprendre comment leurs performances peuvent être améliorées. Bien que la littérature sur les convertisseurs haute-tension basse-puissance soit peu foisonnante, certains exemples peuvent être trouvés du côté des convertisseurs "off-line" (dont le but est de convertir le 230 V_{ac} redressé en une sortie $+5\ V$ ou $+12\ V$ basse-puissance). Des convertisseurs sous forme de "modules" sont également présents sur le marché.

Cependant, les performances de ces solutions ne sont pas satisfaisantes au vu du cahier des charges fixé par l'application, et ce sur plusieurs aspects. Tout d'abord, seules quelques solutions permettent de convertir une tension en entrée supérieure ou égale à 600 V, ce qui fait qu'elles ne peuvent être utilisées pour le cahier des charges centré sur la conversion 800 V vers 12 V. Ensuite, le rendement proposé par la plupart de ces solutions est en dessous de celui visé ici, bien que certains exemples se rapprochent d'un rendement de 85% (mais seulement pour des tensions inférieures à 500 V). Les faiblesses des solutions existantes peuvent être en partie expliquée par l'architecture Flyback utilisée pour l'étage de puissance dans la majorité des cas.

L'architecture Flyback possède des atouts intéressants (simplicité, faible coût, fiabilité, etc.) liés à sa structure simplifiée (seul un interrupteur, un transformateur et une diode sont requis).

Cependant, cette architecture présente de sérieuse limites qui font qu'elle n'est peut-être pas la plus adaptée dans le cas d'un convertisseur haute-tension basse-puissance. Premièrement, elle impose un fort stress en tension sur l'interrupteur de puissance (supérieur à la tension d'entrée du convertisseur) ce qui demande d'utiliser plusieurs composants en série (se pose alors le problème de répartition de la tension) ou bien un composant avec une très haute tenue en tension, souvent basé sur des matériaux "grand-gap" qui demeurent coûteux et volumineux (GaN, SiC). Ensuite, un fort stress en tension est également appliqué sur le transformateur, ce qui peut se traduire par d'importantes pertes fer au sein du matériau magnétique. Pour éviter cela, le convertisseur peut opérer à basse fréquence, mais cela risque d'augmenter la taille des composants de filtrages etc. Enfin, l'architecture Flyback pose également la question des pertes à la commutation. Si elles peuvent être réduites grâce à des modes de fonctionnement tels que le "Quasi-Résonnant", elles demeurent un des problèmes potentiel posé par cette architecture.

Exploration de topologies

Critères sélectionnés

Avant de présenter les différentes topologies étudiées, il est nécessaire de décrire les critères qui sont utilisés pour analyser et comparer les différentes structures. Ces critères sont choisis en traduisant le cahier des charges en caractéristiques clés que la topologie devra présenter pour répondre au mieux aux attentes.

- Réduction du stress en tension sur les interrupteurs de puissance

  Tout d'abord, il faut souligner qu'il existe deux types différents de stress en tension : celui qui est appliqué pendant un court instant, lors de transitions résonantes, et celui qui s'applique de manière plus "continue" durant une période de découpage. Il existe plusieurs méthodes pour réduire le premier type de stress en tension, comme les "RCD clamp" (Résistance-Condensateur-Diode) utilisées dans l'architecture Flyback. En revanche, pour le deuxième type il faut modifier la structure complète de l'étage de puissance pour le réduire, et c'est ce qui est recherché ici.

  Il est important de réduire le stress en tension sur les interrupteurs pour permettre l'utilisation de technologies d'intégration plus "classiques" (Silicium Haute-Tension). En effet, les interrupteurs qu'elles offrent ne peuvent généralement pas supporter des tensions supérieures à 700 V voire 800 V, ce qui est insuffisant au vu du cahier des charges.

  Il existe des méthodes de conception de l'étage de puissance qui permettent de réduire efficacement le stress en tension sur chaque interrupteur, en les connectant en série par exemple. Cela pose alors d'autres problèmes, en termes d'équilibrage notamment, mais qui peuvent être résolus en ajoutant des condensateurs autour des interrupteurs pour stabiliser la distribution de la tension.

- Réduction du flux magnétique dans le transformateur

  Le transformateur est un composant clé dans de nombreux convertisseurs DC/DC isolés, car il influence grandement la taille et le rendement du convertisseur global. Il génère deux types de pertes principalement : des pertes par conduction, dues aux courants qui circulent dans les enroulements du transformateur ; et des pertes fer, liées au flux qui circule dans le noyau magnétique du transformateur.

Ces dernières posent de véritables difficultés dans le cas du convertisseur haute-tension basse-puissance, car elles dépendent principalement de la tension appliquée sur les enroulements du transformateur et non du courant. Plus la tension d'excitation du transformateur est grande, plus les pertes sont élevées, ce qui pourrait être un problème au vu de la haute tension d'entrée du convertisseur. Pour permettre d'améliorer les performances du transformateur, il est vital de réduire les pertes fer et pour observer cette réduction, il est possible de surveiller la valeur maximale de la "densité du flux magnétique", notée B_{peak}, et qui s'exprime comme :

$$B_{peak} = \frac{V \cdot D}{2 \cdot A_e \cdot N \cdot f_{sw}} \tag{1}$$

Où V est l'amplitude de la tension d'excitation du transformateur ($V = V_{in}$ dans le cas du Flyback par exemple), D est le rapport cyclique (ici la forme d'onde excitation considérée est rectangulaire ce qui est souvent le cas des convertisseurs DC/DC); A_e est la section du noyau magnétique du transformateur, N le nombre de tours qui composent l'enroulement soumis à l'excitation V et enfin f_{SW} est la fréquence de l'excitation.

Plus B_{peak} est élevée, plus les pertes fer seront importantes, il faut donc réduire sa valeur en jouant sur les différents facteurs qui y jouent un rôle. La section et le nombre de tours sont liés à des considérations géométriques et dépendent donc fortement du type de noyau choisi, tandis que le rapport cyclique D est en partie déterminée par la relation entre les tensions d'entrée et de sortie du convertisseur. Du point de vue de la topologie, un des meilleurs moyens pour réduire les pertes fer sera donc de réduire la tension d'excitation du transformateur et d'augmenter sa fréquence.

- Possibilité de commutation douce

  Lors du passage de l'état bloqué à l'état passant, les interrupteurs de puissance peuvent générer des pertes liées à leurs éléments parasites intrinsèques. Ces pertes à la commutation peuvent avoir une influence négative sur le rendement du convertisseur, car elles varient avec le carrée de la tension comme le montre leur expression approchée :

$$P_{SW_{FET}} = \frac{1}{2} \cdot C_{oss} \cdot V_{DS}^2 \cdot f_{SW} \tag{2}$$

  Où C_{oss} est la capacité parasite de sortie des interrupteurs de puissance, .V_{DS} est la tension présente à leurs bornes lors de la commutation et f_{SW} est la fréquence à laquelle les interrupteurs sont pilotés.

  Pour illustrer en quoi ces pertes peuvent poser un problème, il est intéressant de faire une simple application numérique. Pour une capacité parasite de 20 pF, une fréquence de 150 kHz, les pertes sont :

$$P_{SW_{FET}} = \begin{cases} 240 \text{ mW} & \text{pour } V_{DS} = 400 \text{ V} \\ 960 \text{ mW} & \text{pour } V_{DS} = 800 \text{ V} \end{cases} \tag{3}$$

  Ces pertes très élevées pourraient largement réduire le rendement du convertisseur, puisqu'elles sont comparables à la puissance fournie en sortie du convertisseur. Il apparait donc vital de les réduire pour permettre d'atteindre les objectifs fixés pour le rendement.

Une technique largement employée pour réduire les pertes à la commutation au sein des convertisseurs DC/DC est la "commutation douce". Elle consiste simplement à retarder l'allumage d'un interrupteur de puissance, de telle manière à ce que la tension à ses bornes lors de la commutation soit nulle (d'où le nom de la technique "Zero Volt Switching" ou ZVS). Cependant, toutes les topologies de convertisseur ne permettent pas d'utiliser cette technique, c'est pourquoi le critère "Possibilité de commutation douce" est utilisé pour étudier les topologies candidates.

- Complexité de la solution

  Un des objectifs de ces travaux est de trouver une solution de petite taille et à coût réduit qui répond au cahier des charges fixé. Ainsi, une des maximes qui pourraient guider le choix de la topologie pourrait se résumer à "le plus simple sera le mieux". En effet, si augmenter la complexité d'une solution peut être utile pour améliorer ses performances, cela se traduira sans nul doute également par un coût et une empreinte plus élevée. Il va donc falloir trouver un compromis en ce qui concerne la "complexité" de l'étage de puissance, pour qu'il puisse atteindre les performances voulues tout en respectant les contraintes initiales de coût et de taille.

  Différents types de "complexité" peuvent être pris en compte, le terme demeurant assez vague. Par exemple, le nombre d'interrupteurs de puissance requis pour construire une topologie donne une idée des difficultés liées à leur intégration sur puce. Pour les composants passifs, leur nombre peut également être pris en compte, tout comme les éventuelles difficultés qui pourrait rendre leur conception plus complexe (condensateur de grande valeur, transformateur multi-enroulements etc.). La complexité peut également venir des aspects liés au contrôle du convertisseur, dans le cas où plusieurs boucles de régulation ou diverses synchronisations seraient requises par exemple.

Convertisseurs avec entrées en série

Les convertisseurs avec entrées en série (Input Series Converters ou ISC en angalis) sont un moyen d'arranger et de relier plusieurs convertisseurs "briques" identiques pour former un convertisseur "global" avec de meilleurs caractéristiques. Ces arrangements permettent de créer des convertisseurs pouvant fonctionner avec une grande tension d'entrée à partir de convertisseurs "briques" orienté vers de plus basses tensions. Les arrangements qui connectent les entrées des convertisseurs en série et leur sortie en parallèle (Input-Series Output-Parallel ou ISOP) sont un exemple de ce type de structure. Le convertisseur "brique" doit être une structure isolée, pour permettre de relier ensemble les différentes sorties tandis que les entrées sont connectées à des points de tension différents. Plusieurs variations de ces structures existent, avec une sortie commune à tous les convertisseurs par exemple (ce qui sous-entend l'utilisation d'un transformateur unique pour tous les convertisseurs « briques ») ou bien avec plusieurs sorties différentes.

Le principal avantage de ce type d'arrangement est qu'il permet de réduire la tension d'entrée de chacun des convertisseurs briques. Ainsi, le stress en tension sur les interrupteurs et le transformateur est réduit. Cela permet de construire un convertisseur acceptant une tension en entrée jusqu'à 1.8 kV en connectant trois convertisseurs de 600 V en série. Grâce à cette réduction de la tension d'entrée, l'architecture du convertisseur brique peut être simplifiée, pour réduire la complexité du convertisseur global. A noter que si le convertisseur brique peut fonctionner en commutation douce, il est fort probable que le convertisseur complet en sera également capable.

Cependant, ce type d'arrangement comporte plusieurs défauts qui diminuent son intérêt. Tout d'abord, en condition de fonctionnement réel, rien ne garantit que la tension d'entrée soit équitablement répartie sur les convertisseurs briques, ce qui pourrait causer des problèmes de surtension etc. Pour garantir cette bonne répartition, plusieurs méthodes existent (rapport cyclique commun, synchronisation des convertisseurs...) mais toutes apportent un nouveau degré de complexité au convertisseur global. Ensuite, le transformateur requis pour ce type d'arrangement pose également des problèmes. Si des solutions existent pour éviter que chaque convertisseur brique ait besoin de son propre transformateur (car leur multiplication serait contraire aux objectifs de petite taille et de faible coût), le transformateur requis dans ces structures est assez complexe, car il doit posséder au moins un enroulement pour chaque convertisseur brique. De plus, la diminution de la tension d'entrée de chaque convertisseur ne garantit pas la diminution du stress sur le transformateur, car l'aire occupée par un enroulement est également grandement réduite, l'espace total dédié aux enroulements étant divisé par le nombre de convertisseurs briques utilisés. Pour reprendre les termes du critère portant sur le flux magnétique (Eq. 1), cela revient à diviser à la fois la tension d'excitation V mais également le nombre de tours de l'enroulement N, et donc la densité du flux magnétique ne diminue pas. Cette structure de convertisseur ne garantit donc pas de réduire les pertes fer du transformateur, ce qui pourrait être un problème pour atteindre les objectifs de rendement.

Convertisseurs à capacités commutées

Les convertisseurs à capacités commutées (en anglais Switched-Capacitor ou SC) ont gagné en popularité ces dernières années car ils ouvrent la voie vers des convertisseurs DC/DC complètement intégrés. Ils tirent leurs bénéfices de leur fonctionnement basé uniquement sur des condensateurs et requièrent aucun composant magnétique (qui sont bien souvent les plus volumineux). Ces convertisseurs peuvent prendre diverses formes en fonction du ratio de conversion visé et selon les composants employés. Cependant, ils sont basés sur un principe similaire : l'étage de puissance bascule entre deux positions ce qui permet de conserver une tension stable et équilibrée entre les différents condensateurs. La tension de sortie est souvent un ratio fixe de la tension d'entrée (1/2 ou 1/3 etc.) du fait de la construction du circuit.

Une des raisons de leur popularité est qu'ils permettent d'atteindre de forte densité de puissance, grâce aux condensateurs employés qui stockent l'énergie plus efficacement que les inductances par exemple. Les condensateurs peuvent parfois être intégrés dans sur la même puce que les composants actifs, mais cela reste plus compliqué pour les convertisseurs opérant avec une tension de plus de quelques dizaines de volts ou demandant une forte puissance. Quelques exemples de circuits à capacités commutées sont toutefois présents dans la littérature, pour convertir des tensions de 230 V_{ac} redressée vers une basse tension à basse puissance, mais sans isolation. En effet, l'absence de composant magnétique ne permet pas à ces structures de proposer une isolation galvanique. Ainsi, le circuit à capacité commutées ne pourrait être utilisé seul mais nécessiterait un deuxième étage pour isoler et réguler la sortie.

L'intérêt principale des circuits à capacités commutées est qu'ils réduisent assez fortement le stress sur les interrupteurs de puissance (bien que cela dépende de l'architecture utilisée). Ainsi avec un circuit à capacités commutées de type "échelle" (où les capacités sont connectées en série), le stress en tension sur chaque interrupteur est divisé par le nombre de condensateurs connectés en série (par rapport à la tension d'entrée). Par ailleurs, si le circuit à capacités commutées est utilisé comme premier étage, la tension d'entrée du second étage, chargé d'isoler et de réguler la tension de sortie, peut être réduit. Le stress en tension des interrupteurs du deuxième étage et du transformateur est donc grandement limité.

Cependant, l'emploi des circuits à capacités commutées se traduit par un nombre important de composants actifs et passifs. En effet, pour réduire le stress en tension sur les interrupteurs, il faut ajouter des capacités en série qui ne peuvent être intégrées car ce sont des condensateurs haute-tension. Par ailleurs, le circuit pour équilibrer les capacités entre elles est composé de nombreux interrupteurs, ce qui peut rendre complexe leur intégration sur puce. Par ailleurs, en plus de tous ces composants, un deuxième étage est requis pour isoler la sortie, qui s'ajoute encore à la complexité de cette solution, car il est composé là encore de plusieurs composants etc. Enfin, si l'absence de composant inductif dans l'étage à capacités commutées interdit celui-ci d'utiliser les méthodes de commutation douce. Cet étage risque donc de générer des pertes à la commutation, qu'il s'agira de réduire le plus possible, en baissant la fréquence de commutation ou en diminuant la taille des capacités parasites.

Convertisseurs hybrides : multi-niveaux à capacités flottantes

Un autre type de topologies de convertisseur étudié est celui des topologies dites "hybrides" dans le sens où elles sont un mélange des approches classiques des convertisseurs à découpage, basés sur l'emploi d'inductance, et des approches à capacités commutées, présentées ci-dessus. Ces structures hybrides tirent parti des bénéfices des deux approches : l'aspect capacités commutées permet de réduire le stress en tension sur les interrupteurs et sur le transformateur, tandis que l'aspect inductif permet d'inclure l'isolation dans l'étage de puissance et peut permettre le fonctionnement en commutation douce. De nombreuses formes de structure hybride existent, l'une des plus connues étant les convertisseurs "multi-niveaux à capacités flottantes".

Les convertisseurs multi-niveaux à capacités flottantes (Multi-Level Flying-Capacitor ou ML-FC en anglais) sont souvent utilisés dans les convertisseurs DC/DC non-isolés afin de réduire le stress en tension sur l'inductance et donc les ondulations de courant. Leur intérêt principal au sein des convertisseurs haute-tension basse-puissance serait de réduire le stress en tension sur les interrupteurs et le transformateur, notamment grâce à la tension DC développée sur les capacités flottantes. Le transformateur étant directement connecté à l'étage de puissance, il est possible d'utiliser les techniques de commutation douce pour réduire les pertes à la commutation et donc d'augmenter la fréquence de découpage.

Cependant, une des faiblesses des architectures multi-niveaux à capacité flottante concerne la tension aux bornes de la capacité flottante. En effet, en conditions réelles, il se peut que cette tension ne soit pas celle prédite par la théorie, ce qui pourrait conduire à un stress plus grand sur les interrupteurs et le transformateur. La charge de cette capacité flottante pose également des questions pour la phase de démarrage du convertisseur, qui pourrait se révélée délicate dans certains cas.

Comparaison des différentes structures

Maintenant que les différentes structures ont été introduites, il est possible de les comparer pour identifier celle la plus adaptée à la conception d'un convertisseur haute-tension basse-puissance dans le contexte défini par l'application. Cette comparaison se base sur les critères décrits au début de l'exploration des topologies et elle est gardée la plus "juste" possible en comparant les structures avec la même réduction du stress en tension sur les interrupteurs. Pour les arrangements de convertisseurs à entrées en série, seuls deux convertisseurs brique sont utilisés. Pareil pour les étages à capacités commutées, le nombre de capacités en série est limité à deux. Pour les convertisseurs multi-niveaux, cela se traduit par l'emploi d'une seule capacité flottante qui permet de diviser par deux le stress en tension sur les interrupteurs. En opérant de la sorte, il est possible de comparer plus simplement les performances de chacune des structures par rapport aux autres critères.

En ce qui concerne la réduction du stress sur le transformateur, l'architecture qui semble permettre la plus forte réduction de la tension d'excitation est celle basée sur les convertisseurs à capacités commutées. Grâce à la réduction de tension permises par un premier étage de ce type, le deuxième étage d'une telle structure (où se trouve le transformateur) verrait sa tension en entrée divisée par deux et donc cela conduirait à réduire fortement le stress sur le transformateur. A l'inverse, les structures basés sur la mise en série d'entrée de convertisseurs "briques" ne semble pas permettre une forte réduction de ce stress en tension, du fait de la multiplication des enroulements comme souligné précédemment. Les architectures hybrides de type Multi-Niveaux à Capacité Flottante se positionnent entre les deux cas susmentionnés, car elles permettent bien de réduire le stress en tension sur le transformateur sans toutefois le faire aussi efficacement que si la tension d'entrée du convertisseur elle-même était divisée.

Les possibilités de commutation douce varient également selon les architectures. Les structures basées sur les convertisseurs multi-niveaux à capacité flottante sont tout à fait adaptées à l'implémentation de cette technique. Pour les convertisseurs à entrées en série, c'est également le cas, sous réserve que le convertisseur "brique" utilisé soit lui-même compatible avec ce mode de fonctionnement. En revanche, les étages à capacités commutées ne permettent pas, dans leur forme la plus courante, de mettre en place les techniques de commutation douce ce qui aura un impact négatif sur les pertes que cet étage risque de générer.

Pour ce qui est de la "complexité" de l'étage de puissance, les différents aspects mis en avant lors de la présentation de ce critère sont abordés.

Le nombres de composants actifs requis pour chaque structure n'est pas simple à évaluer, car il dépend notamment de l'architecture du convertisseur de base pour les arrangements convertisseurs en série ou de la topologie placée en cascade de l'étage à capacités commutées. Il est possible cependant de faire des suppositions simples sur la structure probable de ces différentes solutions et donc d'établir un classement des topologies les plus complexes. En effet, sans préciser l'architecture du deuxième étage d'un convertisseur basé en partie sur les circuits à capacités commutées, il est possible d'estimer que cette solution est celle demandant le plus grand nombre d'interrupteurs, du fait de sa structure en deux étages (d'autant plus que l'étage à capacités commutées requière déjà un nombre important d'interrupteurs). Pour ce qui est de l'association des convertisseurs en séries, si le convertisseur de base est de type Flyback, il peut ne comporter qu'un seul interrupteur mais les performances du convertisseur globales seront alors limitées. Un calcul plus réaliste serait de compteur deux interrupteurs pour chaque convertisseur brique, ce qui ouvrirait la voie à des structures plus performantes mais augmenterait le nombre total d'interrupteurs. Au final, les convertisseurs hybrides multi-niveaux à capacité flottante permettent de limiter la complexité de ce point de vue, puisque composé d'un seul étage, et si le nombre de niveaux est limité à 3, dès lors le nombre d'interrupteurs restera plus faible que ce qui est proposé par les architectures à deux niveaux.

Le nombre de composants passifs varie également selon la structure précise de chaque solution. De manière générale, les convertisseurs basés sur un étage à capacités commutées auront un plus grand nombre de condensateurs discrets, notamment pour le premier étage. Les arrangements de convertisseurs en série pourront réduire ce nombre de condensateur, mais le transformateur requis pour ce type de solution sera plus complexe, du fait que chaque convertisseur brique devra posséder son enroulement. Les architectures Multi-Niveaux à capacité flottante auront besoin de quelques condensateurs haute-tension (notamment pour la capacité flottante) mais leur impact sur la taille du convertisseur finale devrait être assez limité.

Pour finir, en ce qui concerne les complexités additionnelles liées au contrôle du convertisseur, les arrangements de convertisseurs briques doivent garantir la bonne distribution de la tension d'entrée, ce qui implique un degré de complexité supplémentaire pour synchroniser les différents convertisseurs. Les structures du type Multi-Niveaux doivent quant à elles garantir la stabilité de la tension aux bornes de la capacité flottante pour s'assurer que le stress sur les interrupteurs ne dépasse pas la tension de claquage.

Topologie retenue

En se basant sur la comparaison effectuée sur les critères retenus, une topologie est choisie. Les convertisseurs Multi-Niveaux à Capacité Flottante sont sélectionnés pour le bon compromis qu'ils offrent entre la complexité de l'étage de puissance et ses performances, en particulier le rendement. Ce choix est bien entendu lié au choix initial de la technologie d'intégration (HV bulk Silicium) auquel la notion de complexité est étroitement liée. Cette architecture est également intéressante car elle permet d'effectuer la conversion en un seul étage, ce qui limite le nombre de composants de filtrage requis. Pour rester dans une logique de bas-coût et de simplicité, la structure du Multi-Niveau est hybridée avec une architecture de type Buck isolé, qui compte un nombre réduit de composants (notamment sur le côté secondaire du transformateur).

Conclusion

Pour concevoir un convertisseur DC/DC isolé avec une grande tension d'entrée et une faible tension et puissance en sortie, quelques-unes des solutions existantes répondant à un cahier des charges similaires ont été présentées. Cependant, leurs performances ne semblent pas en accord avec les prérequis de l'application visée et l'architecture utilisée par la plupart des solutions basse-puissance (Flyback) semble expliquer au moins partiellement ces mauvais résultats.

Ainsi, une exploration des topologies pour l'étage de puissance du convertisseur a été menée, afin de trouver une architecture alternative plus en phase avec les besoins des convertisseurs haute-tension basse-puissance. Quelques critères qualitatifs ont été choisis comme retranscription des contraintes imposées par l'application et l'approche choisie et ils ont été utilisés pour étudier différentes structures de convertisseurs.

Au final, une comparaison être les architectures étudiées a été proposée et elle a montré que les structures de types hybride comme les convertisseurs Multi-Niveaux à Capacité Flottante semble offrir le meilleur compromis entre complexité et performances et ils ont donc été retenu pour concevoir une première version du convertisseur haute-tension basse-puissance visé.

Chapitre 2 : Analyse de la topologie

L'objectif de ce chapitre est de proposer une analyse détaillée du fonctionnement en régime permanent de la structure choisie du convertisseur. L'approche et les "versions" du convertisseurs choisies sont détaillées dans un premier temps. Ensuite, une analyse d'une période de découpage est proposée pour chacune des versions. Les premiers éléments qui ressortent de l'analyse sont étudiés et offrent les premières clés pour concevoir un convertisseur performant.

Approche choisie et objectifs de l'analyse

Le cahier des charges présenté durant le chapitre d'Introduction Générale se concentre sur deux valeurs de tensions d'entrée (400 V et 800 V) et pour y répondre, il est choisi d'utiliser deux variations de la structure Multi-Level Flying-Capacitor Asymmetrical Half-Bridge Flyback (ML-FC-AHBF).

L'architecture 2L-AHBF est utilisée pour répondre au cahier des charges centré sur une tension en entrée de 400 V. Elle se compose de deux interrupteurs de puissance dont le stress en tension n'est pas réduit, mais cela ne présente pas de problème étant donné que la tension maximale en entrée ne dépasse pas 500 V.

En revanche, pour le cahier des charges visant une valeur de 800 V pour la tension d'entrée, la structure utilisée est le 3L-FC-AHBF, la structure à 3-niveaux et une capacité flottante. Elle permet de diviser par deux le stress en tension appliqué sur les interrupteurs et permet donc bien de répondre au cahier des charges pour lequel la tension en entrée peut grimper jusqu'à 1 kV.

Dans les prochains paragraphes, une analyse d'une période de découpage de chacune de ces architectures est proposée, pour permettre de mieux comprendre leur fonctionnement et d'identifier certains des paramètres clés pour le design du convertisseur. L'analyse du 2L-AHBF est effectuée dans un premier temps, suivie de celle du 3L-FC-AHBF.

Analyse de la configuration 2L-AHBF

La topologie Asymmetrical Half-Bridge Flyback (AHBF ou 2L-AHBF dans ce document) peut être vue comme la version isolée de l'architecture Buck bien connue. Elle se compose de deux interrupteurs de puissance commandé de façon complémentaire, d'un transformateur et de quelques condensateurs. Un condensateur est connecté comme la sortie d'un Buck en série avec l'enroulement primaire du transformateur. Au secondaire, une diode permet de rectifier la tension obtenue en sortie du transformateur et de créer une tension stable sur le condensateur de sortie. Le schéma de l'étage de puissance qui inclut le modèle considéré pour les principaux composants apparait dans la Figure 1. Le logiciel SIMetrix Simplis est utilisé pour obtenir les formes d'ondes en simulation présentée sur la Figure 2.

Pour les interrupteurs de puissance, le modèle considéré consiste en un transistor à effet de champ de type N-MOS avec une diode de corps et une capacité de sortie connectées en parallèle entre le drain et la source du transistor. La résistance de canal du transistor n'est pas prise en compte.

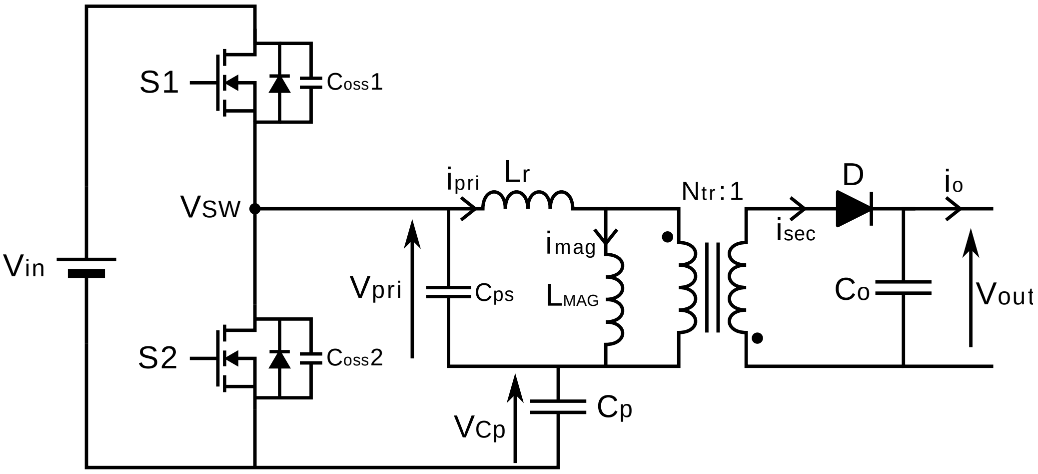


Figure 1: Modèle considéré pour la configuration 2L-AHBF

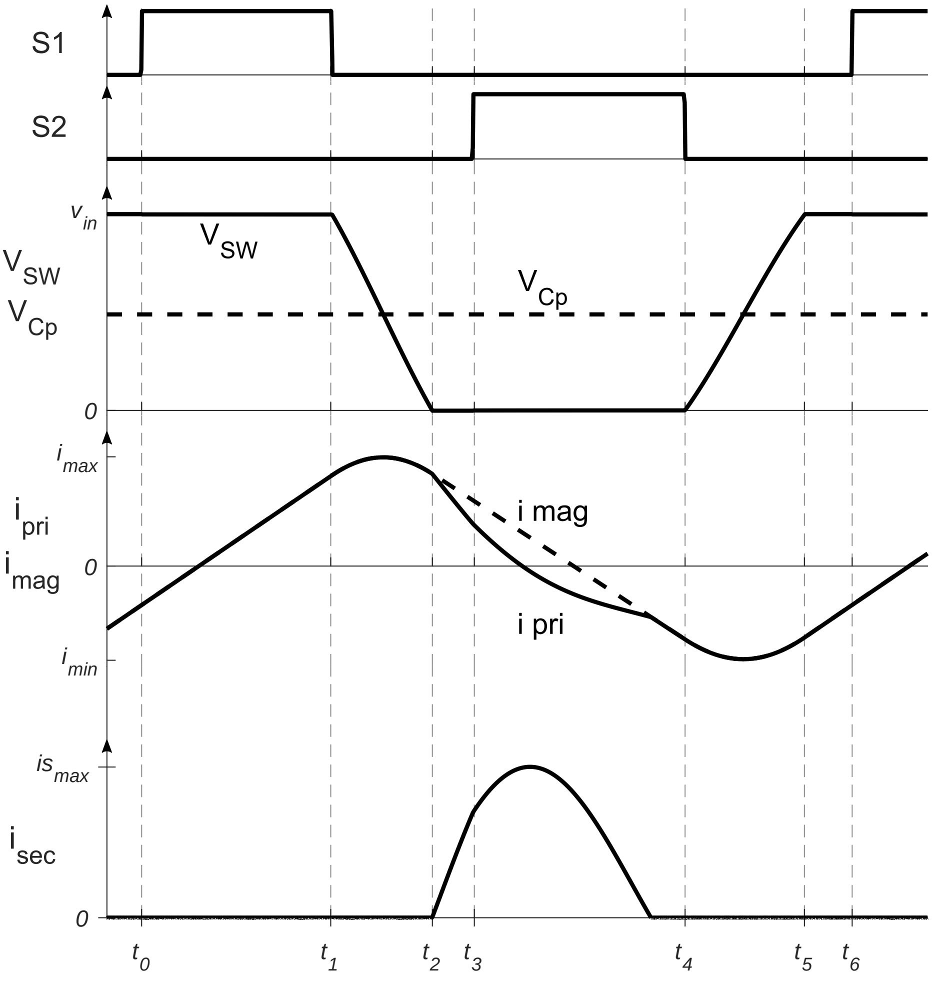


Figure 2: 2L-AHBF - Principales formes d'ondes en simulation

Pour le transformateur, le modèle est construit autour d'un transformateur idéal qui relie le primaire et le secondaire avec un rapport de transformation égale à N_{tr}. L'inductance magnétisante du transformateur est modélisée au primaire de celui-ci et est reliée en série une inductance de fuite L_r. Une capacité unique est considérée dans ce modèle comme la somme de toutes les capacités parasites du transformateur ramenées au primaire (C_{ps}). La résistance des enroulements n'est pas prise ne compte pour cette analyse.

Quelques hypothèses sont également faites pour simplifier l'analyse de la structure :

- La valeur des condensateurs au primaire C_p et en sortie C_o est assez élevée pour que la tension aux bornes de ceux-ci puisse être considérée constante.
- La valeur de l'inductance de fuite est faible devant celle de l'inductance magnétisante.

Une période de découpage de l'architecture 2L-AHBF en régime permanent peut se décomposer en six étapes.

Mode I - (t_0 - t_1)
Ce mode commence lorsque l'interrupteur S1 devient passant, ce qui force la tension au point milieu V_{SW} à V_{in}. Une tension positive s'applique sur le primaire du transformateur ($V_{pri} = V_{in} - V_{Cp}$) et le courant primaire (égal au courant magnétisant) augmente linéairement.

Mode II - (t_1 - t_2)
Lorsque S1 devient bloquant, le courant qui circule dans l'inductance magnétisante force le point milieu à chuter de V_{in} jusqu'à atteindre la masse. Lors de cette transition, les capacités parasites des composants connectées au point milieu sont (dé)chargées. En particulier, les principaux contributeurs sont les capacités de sortie des interrupteurs S1 et S2 ainsi que la capacité parasite totale du transformateur C_{ps}. Les contributions de ces capacités peuvent être ajoutées directement car elles sont toutes connectées en parallèle d'un point de vue des variations AC.

Les équations différentielles qui régissent cette transition ne sont pas explicitées ici, mais il convient de noter qu'elles font intervenir à la fois la valeur des capacités parasites, la valeur de l'inductance magnétisante ainsi que le courant magnétisant disponible au début du Mode II, qui jouent donc un rôle déterminant pour le déroulement de cette étape.

Mode III - (t_2 - t_3)
Lorsque la tension au point milieu V_{SW} devient nulle, la diode de corps du transistor S2 devient passante et un courant circule négatif alors dans le primaire du transformateur. La tension sur l'enroulement primaire est négative ($V_{pri} = -V_{Cp}$) et cela se répercute en une tension positive sur l'enroulement secondaire du transformateur, qui polarise la diode du secondaire D et un courant i_{sec} circule donc au secondaire.

La dynamique de ce courant est fortement lié à la valeur de l'inductance de fuite L_r, à la capacité parasite de la diode D ainsi qu'aux divers chutes de tension aux bornes des interrupteurs ou du transformateur. Plus la valeur de ces éléments sera grande, plus la dynamique du courant secondaire sera lente.

En ce qui concerne le courant dans le primaire, il devient légèrement différent du courant magnétisant durant cette phase de fonctionnement du fait du courant secondaire.

Mode IV - (t_3 - t_4)
Ce mode débute lorsque l'interrupteur S2 lui-même devient passant. En simulation, une légère modification de la dynamique du courant secondaire est observée : elle est liée à la chute de tension sur l'interrupteur S2 qui est différente lorsque la diode de corps conduit le courant. Or, ces chutes de tension parasites n'étant pas prise en compte pour cette analyse, le comportement du convertisseur lors du Mode IV est très similaire au Mode III décrit ci-dessus.

A noter que le courant secondaire peut s'annuler durant ce mode de fonctionnement, si la tension aux bornes du condensateur de sortie est trop élevée pour que la diode au secondaire soit correctement polarisée. Cela n'influence cependant pas les autres formes d'ondes, car la tension sur le primaire du transformateur est toujours négative et forcée par le transistor S2.

A noter que durant cette phase, le courant magnétisant diminue linéairement jusqu'à devenir négatif.

Mode V - (t_4 - t_5)
Dès que l'interrupteur S2 devient bloquant, une nouvelle transition est initiée pour la tension au point milieu V_{SW}, et celle-ci se détache de la masse pour atteindre V_{in} à la fin de la transition. Cette transition est due au courant magnétisant négatif qui (dé)charge les capacités parasites connectés au point milieu (les mêmes que durant le Mode II).

Des équations similaires peuvent être écrites pour décrire les variations du courant et de la tension au primaire du transformateur durant cette phase. Les mêmes éléments que durant le Mode II y apparaissent et jouent donc un rôle pour cette transition également.

Mode VI - (t_5 - t_6)
Ce mode débute lorsque la tension au point milieu V_{SW} dépasse V_{in} ce qui permet à la diode de corps de S1 de conduire un courant. Le comportement durant cette phase est très similaire à celui décrit pour le Mode I : une tension constante positive est forcée sur l'enroulement primaire du transformateur et le courant primaire augmente linéairement.

Lorsque l'interrupteur S1 devient passant, le convertisseur est dans les mêmes conditions qu'au début du Mode I et une nouvelle période de découpage commence.

Analyse du 2L-AHBF en régime permanent

L'analyse des formes d'ondes de la topologie 2L-AHBF donne des informations intéressantes en ce qui concerne le mécanisme de commutation douce, l'influence des composants parasites. Elle permet également d'obtenir une expression reliant les tensions d'entrée et de sortie du convertisseur.

L'analyse des phases de transitions du point milieu du convertisseur renseigne sur les possibilités de commutation douce de la topologie ainsi que sur les éléments importants liés à ces phases de transitions. En particulier, le rôle de l'inductance de fuite, qui est parfois central pour les commutations douces des convertisseurs qui fonctionnent à plus forte puissance, est ici limité. Le choix de la valeur de ce paramètre ne sera donc pas déterminant lors de la conception du transformateur. En revanche, l'inductance magnétisante est celle qui détermine le plus fortement la possibilité de commutation douce, car c'est le courant qui y circule qui permet ou non d'utiliser cette technique. La valeur de ce paramètre clé du transformateur devra être soigneusement choisie pour permettre que les transitions liées à la commutation douce des interrupteurs soient complétées.

Les phases de transitions qui permettent la commutation douce seront significativement plus longues que pour un convertisseur opérant à plus forte puissance. En effet, un des enjeux de la conception du transformateur sera de réduire l'amplitude du courant primaire. Si les valeurs crêtes de ce courant deviennent faibles, les phases de transitions pour la commutation douce seront d'autant plus longues. A tel point qu'il convient de les inclure dans l'expression de la fonction de transfert global du convertisseur décrite après.

Il est également intéressant de noter que plus la fréquence de découpage sera élevée, plus les contraintes sur la durée maximale des phases de transitions seront fortes. Ainsi, la valeur du courant primaire requis pour opérer la commutation douce augmentera à mesure que la fréquence de fonctionnement du convertisseur augmente.

En calculant de la moyenne de la tension sur l'enroulement primaire et en utilisant le fait que celle-ci est nulle en régime permanent, il est possible d'obtenir une relation qui lie la tension d'entrée du convertisseur et la tension aux bornes de C_p. Par ailleurs, l'analyse du mode de transmission de l'énergie du primaire au secondaire du transformateur permet d'écrire une relation entre V_{Cp} et V_{out}. Au final, il est possible d'écrire la relation entre la tension d'entrée et la tension de sortie :

$$V_{out} = \frac{V_{in}}{N_{tr}} \cdot \frac{L_{mag}}{L_{mag} + L_r} \cdot \frac{1}{T} \cdot (t_{on\_S1} + \frac{dt_{HS} + dt_{LS}}{2}) - V_D \tag{4}$$

Où T est la période de découpage, t_{on_S1} est le temps pendant lequel l'interrupteur S1 (ou sa diode de corps) est passant, dt_{HS} est le temps mort associé à la transition qui précède l'allumage de S1 et dt_{LS} celui qui précède l'allumage de S2. A noter que cette relation est obtenue en considérant que les transitions de la tension au point milieu V_{SW} s'effectuent de manière linéaire à un rythme constant. Cette expression révèle l'influence de la durée des transitions pour la commutation douce sur le comportement général du convertisseur.

Analyse de la configuration 3L-FC-AHBF

La topologie 3-Level Flying-Capacitor Asymmetrical Half-Bridge Flyback (3L-FC-AHBF) est la version trois-niveaux de la structure classique AHBF, qui compte quatre interrupteurs de puissance répartie en deux demi-ponts commandé avec un déphasage de 180°. Une capacité flottante est également ajoutée au circuit pour réduire le stress sur les transistors. Les autres éléments constitutifs du convertisseur sont identiques à la version 2L-AHBF, tout comme le modèle utilisé pour les interrupteurs et le transformateur. Le schéma de l'étage de puissance qui inclut le modèle considéré pour les principaux composants apparait dans la Figure 3. Le logiciel SIMetrix Simplis est utilisé pour obtenir les formes d'ondes en simulation présentée sur la Figure 4.

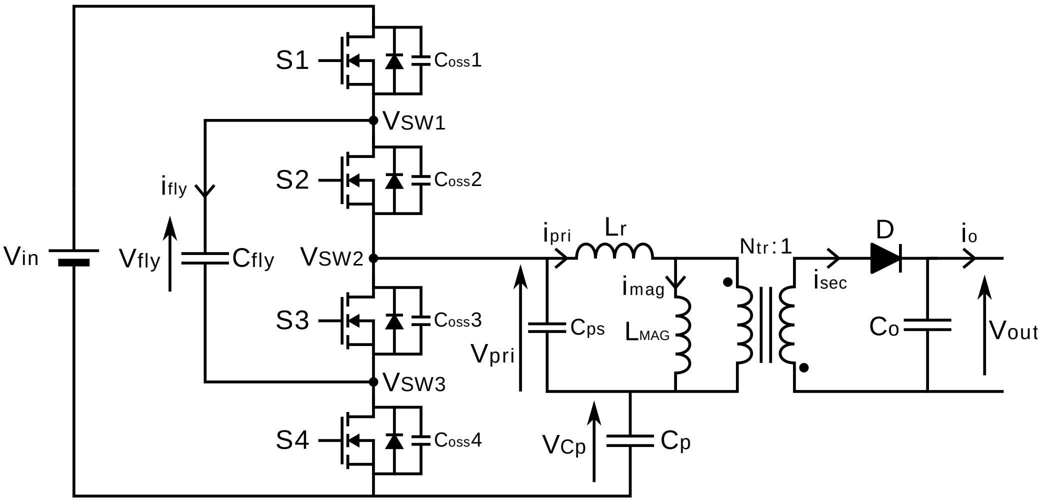


Figure 3: Modèle considéré pour la configuration 3L-FC-AHBF

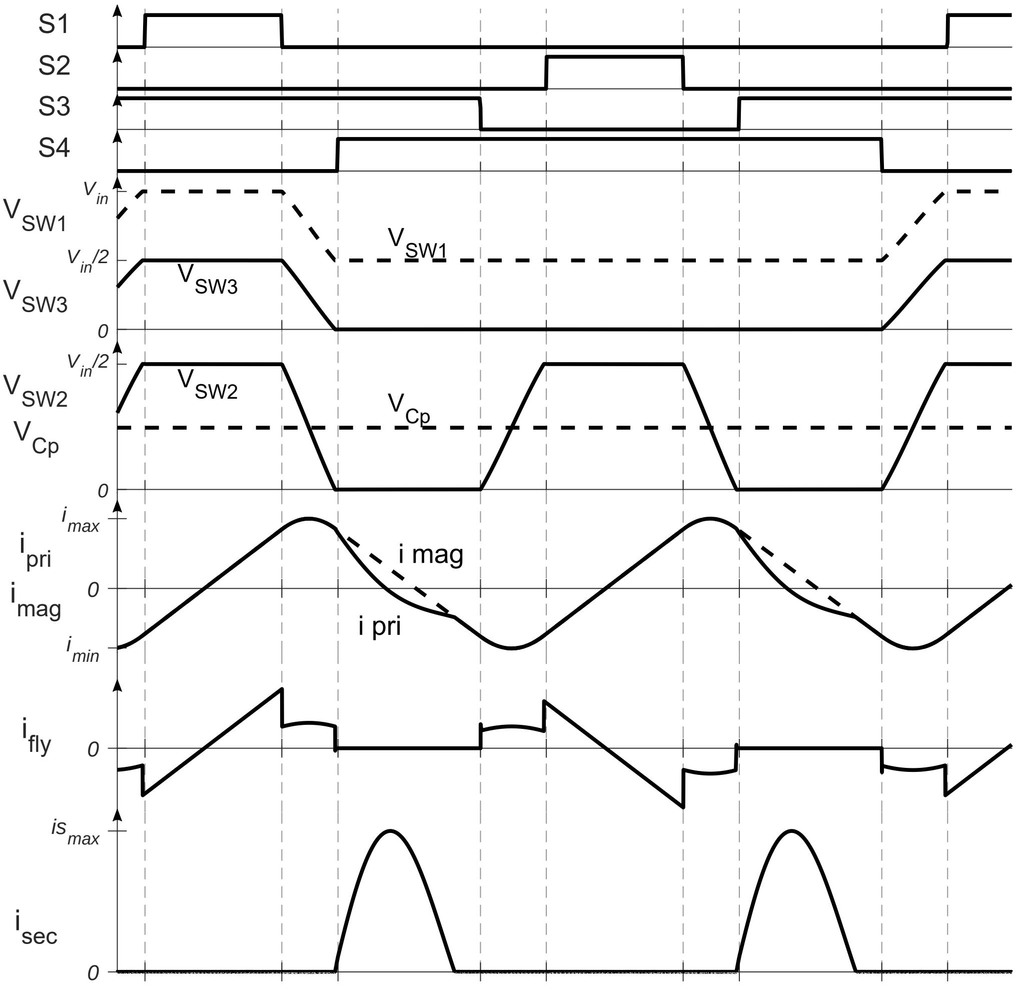


Figure 4: 3L-FC-AHBF - Principales formes d'ondes en simulation

Des hypothèses similaires à celles faites lors de l'analyse du 2L-AHBF sont posées :

- La valeur des condensateurs au primaire C_p, en sortie C_o et pour la capacité flottante est assez élevée pour que la tension aux bornes de ceux-ci puisse être considérée constante.
- La valeur de l'inductance de fuite est faible devant celle de l'inductance magnétisante.
- L'étape durant laquelle la diode de corps conduit le courant est fusionnée avec celle durant laquelle l'interrupteur de puissance est effectivement commandé à l'état passant.

Une période de découpage du 3L-FC-AHBF peut se diviser en deux demi-périodes avec un comportement et des formes d'ondes très similaires. Chacune des demi-périodes peut elle-même se décomposée en quatre étapes.

Mode I - (t_0 - t_1)
Ce mode démarre lorsque l'interrupteur S1 devient passant, l'interrupteur S3 est également passant. La tension appliquée sur le primaire du transformateur peut se calculer comme la différence de tension au point milieu (V_{SW2}) et la tension sur la capacité primaire (V_{Cp}). La tension au point milieu du pont primaire est elle-même la différence entre la tension d'entrée V_{in} et la tension sur la capacité flottante V_{fy}, qui elle-même est chargée à $V_{in}/2$. Ainsi, la tension appliquée sur l'enroulement primaire est positive ($V_{pri} = V_{in}/2 - V_{Cp}$), ce qui conduit à une augmentation linéaire du courant qui circule dans le primaire.

Le courant qui circule dans l'enroulement primaire est entièrement dû au courant magnétisant, et le courant qui circule dans la capacité flottante i_{fly} est le même qui circule dans le primaire.

Mode II - (t_1 - t_2)
Lorsque l'interrupteur S1 devient bloquant, une transition s'amorce pour les différents points flottants du pont (V_{SW1}, V_{SW2}, V_{SW3}) car le courant qui circule dans l'enroulement primaire du transformateur (dé)charge les capacités parasites connectées à ces différents points flottants.

En particulier lors de cette transition, les principales capacités parasites qui jouent un rôle sont celles liées aux interrupteurs S1 et S4 (dont la tension aux bornes varie durant cette étape) et au transformateur. Comme pour l'analyse précédente, il serait possible d'écrire les équations différentielles qui régissent cette phase de transition mais ce n'est pas détaillé ici.

A noter que durant ce mode, le courant qui circule dans la capacité flottante est lié au courant qui (dé)charge la capacité parasite de l'interrupteur S1, ce qui explique la forme de i_{fly} qui est donc une fraction du courant primaire i_{pri}.

Mode III - (t_2 - t_3)
A la fin du mode précédent, le point milieu V_{SW2} atteint le niveau de la masse, et l'interrupteur S4 peut alors devenir passant dans des conditions de commutation douce. Les deux interrupteurs du bas (S3 et S4) sont alors passants. La tension au point milieu étant nulle, une tension négative est appliquée sur le primaire du transformateur. Du fait de la connexion en inverse de l'enroulement secondaire, une tension positive se développe donc sur celui-ci, ce qui polarise la diode D au secondaire et permet à un courant de circuler de ce côté du transformateur.

Le courant qui circule dans le secondaire se soustrait au courant primaire qui devient légèrement différent du courant magnétisant, qui lui décroit linéairement du fait de la tension négative constante appliquée sur l'enroulement primaire. A noter qu'aucun ne circule dans la capacité flottante pendant cette phase, les deux interrupteurs du haut S1 et S2 étant tous deux en état "bloqué". La dynamique du courant secondaire est encore une fois largement influencée par la chute de tension sur l'inductance de fuite L_r ainsi que par la valeur de celle-ci.

Mode IV - (t_3 - t_4)
Cette étape démarre lorsque l'interrupteur S3 devient bloquant, ce qui initie une nouvelle phase de transition pour la tension au point milieu. L'interrupteur S4 reste cependant dans l'état passant, ce qui fait que la tension au points flottants V_{SW1} et V_{SW3} ne change pas. En revanche, la tension au point milieu V_{SW2} augmente du niveau de la masse jusqu'à V_{fly} grâce au courant primaire négatif.

Durant cette phase de transition, les capacités parasites des interrupteurs S2 et S3 sont (dé)chargées, ainsi que celle liée au transformateur C_{ps}. Les équations différentielles décrivant cette transition sont donc très semblables à celles précédemment évoquées.

Comme pour le Mode II, le courant qui circule dans la capacité flottante i_{fly} est lié à la décharge de la capacité parasite d'un interrupteur (ici le transistor S2).

Mode V - (t_4 - t_5)
Lorsque V_{SW2} atteint $V_{in}/2$ l'interrupteur S2 devient passant tandis que S4 reste lui dans l'état passant. Cette phase devient alors très similaire au Mode I, car la même tension est appliquée sur le transformateur (la tension sur le primaire est la même : $V_{in}/2 - V_{Cp}$) et les mêmes courants circulent.

Une des différences notables est le sens du courant qui circule dans la capacité flottante i_{fly} qui est opposé au courant primaire i_{pri} durant cette étape.

Mode VI - (t_5 - t_6)
Lors l'interrupteur S2 devient bloqué, une nouvelle phase de transition est amorcée par le courant magnétisant qui (dé)charge les mêmes capacités parasites que durant le Mode IV. La tension au point milieu chute jusqu'à atteindre le niveau de la masse.

Mode VII - (t_6 - t_7)
L'interrupteur S3 devient passant au début de cette étape, ce qui force une tension nulle au point milieu V_{SW2}, une tension négative sur le primaire du transformateur et permet donc au courant de circuler au secondaire. Cette phase est en tout point similaire au Mode III décrit plus haut, puisque les interrupteurs sont dans le même état et les tensions/courants sont également les mêmes.

Mode VIII - (t_7 - t_8)
Le passage à l'état bloqué de l'interrupteur S4 initie une nouvelle transition sur les points flottants du pont de l'étage de puissance, du fait du courant magnétisant négatif qui circule dans le primaire du transformateur. Les mêmes capacités parasites sont (dé)chargés que dans

le Mode II.

Cette étape se termine lorsque l'interrupteur S1 est commandé à l'état passant, ce qui marque le début d'une nouvelle période de découpage.

Analyse du 3L-FC-AHBF en régime permanent

Comme souligné lors de l'analyse d'une période de découpage de l'architecture 3L-F-AHBF, les mécanismes qui régissent les transitions liées à la commutation douce des différents interrupteurs sont les mêmes. Le rôle de l'inductance magnétisante est en effet central ici aussi, tandis que l'influence de l'inductance de fuite est limitée à la dynamique du courant secondaire.

De la même manière, les temps-morts implémentés entre les états passants des interrupteurs complémentaires verront leur durée fortement augmentée par rapport aux cas où les courants circulant dans le convertisseur sont élevés (lorsqu'ils opèrent à des puissances plus élevées donc).
Ainsi, leur impact sur le fonction de transfert du 3L-FC-AHBF sera également similaire à celui qu'ils ont pour le 2L-AHBF. L'expression de la relation liant la tension en entrée et en sortie du convertisseur n'est pas détaillée ici, mais ses termes sont très proches de ceux de l'expression du 2L-AHBF.

Une des particularités du 3L-FC-AHBF, et un des challenges associés à cette architecture, est la tension sur la capacité flottante. Il faut que celle-ci soit proche de sa valeur idéale pour être dans les conditions de fonctionnement qui viennent d'être décrite. Sinon, il se peut que des surtensions apparaissent sur les interrupteurs de puissance et sur le transformateur, générant des pertes et pouvant endommager certains composants.
Pour garantir que la tension de la capacité flottante est stable à $V_{in}/2$, il faut s'assurer que lorsqu'elle est proche de cette valeur idéale, les flots de charges qui entrent et sortent de la capacité flottante s'équilibrent. Pour cela, il faut que l'intégrale des courants qui circulent dans ce condensateur durant les différentes étapes d'une période de découpage soit nulle. En reprenant les différents modes de fonctionnement explicités précédemment, il apparait que les courants i_{fly} durant certains de ces modes se compensent naturellement. C'est le cas pour les modes II et VIII ou encore pour les modes IV et VI, car le courant i_{fly} qui circule durant ces étapes est toujours lié à la charge puis à la décharge d'une capacité parasite similaire. Il semble donc que seuls les modes I et V doivent être "activement" compensés, ce qui peut être fait en garantissant que ces modes ont une durée similaire et en jouant sur le déphasage entre ces deux modes. Ainsi, il apparait possible de garantir une tension sur la capacité flottante proche de sa valeur idéale sans nécessiter d'une boucle de régulation dédiée.

Résultats d'un prototype discret

Afin de confronter les résultats de cette première analyse de la topologie 3L-FC-AHBF, un prototype d'un convertisseur 500 V vers 12 V, 1 W est construit en utilisant des composants discrets.
Des transistors de type MOSFET (Metal On Semi-conductor Field Effect Transistor) sont choisis pour les quatre interrupteurs de puissance (STD1HN60K3, ST). Des gate-drivers isolés (UCC5320SC, Texas Instruments) sont utilisés pour contrôler ces transistors à partir de signaux générés par un script LabView. Les diverses tensions isolées requises pour alimenter ces

circuits sont créées grâce à des convertisseurs DC/DC isolés (MEA1D1215SC, Murata). Un transformateur existant est utilisé (DA2033-AL, Coilcraft) et une diode Schottky est choisie pour la diode du secondaire (PMEG10020ELR, Nexperia).

Les formes d'ondes des tensions et des courants de l'étage de puissance mesurées ont montré une bonne correspondance avec celles obtenues en simulation. Les mécanismes de commutation douce ont pu être implémenté pour l'ensemble des interrupteurs de puissance en utilisant les courants magnétisants, comme prévu lors de l'analyse. La tension aux bornes de la capacité flottante, bien que non mesurée directement, est évaluée et elle est très proche de sa valeur idéale $V_{in}/2$ et ce alors que le convertisseur opère en boucle ouverte, ce qui confirme qu'un contrôle précis des interrupteurs de puissance peut suffire à garantir que cette tension soit satisfaisante.

Le rendement de ce premier prototype est également évalué, en calculant le ratio de l'énergie fournie par le convertisseur sur l'énergie qu'il absorbe (l'énergie fournie aux circuits liés au contrôle de l'étage de puissance n'est pas prise en compte). Les résultats des mesures ne sont cependant pas à la hauteur de ce qui est attendu. Pour une tension d'entrée limitée à 500 V et une sortie de 12 V-1 W, le rendement se situe entre 85% et 60% selon la fréquence et la tension d'entrée. En particulier, il apparait que plus cette dernière augmente, plus le rendement chute (75% mesuré à 500 V contre 85% à 300 V). D'autre part, il est intéressant de voir l'impact positif de l'augmentation de la fréquence de découpage sur le rendement : à 400 V, un rendement de 81% est obtenu pour une fréquence de fonctionnement de 140 kHz contre seulement 74% à 100 kHz.

Ces premiers résultats confirment donc sur la difficulté de créer une solution avec un haut rendement tel que voulu ($> 85\%$), d'autant que la tension maximale n'est que la moitié de la valeur maximale visée. Cependant, ils donnent également quelques pistes sur comment améliorer les performances du convertisseur, en augmentant la fréquence de découpage notamment.

Conclusion

Ce chapitre a présenté l'analyse de l'architecture choisie pour créer un convertisseur haute-tension basse-puissance à fort rendement. En particulier, les deux versions de la topologie utilisées pour répondre aux deux cahiers des charges présentés lors de l'introduction ont été décrites. L'analyse de leur mode de fonctionnement a permis d'identifier les paramètres clés qui joueront un rôle important pour les mécanismes de commutation douce notamment. Enfin, les résultats d'un premier prototype discrets ont conforté l'analyse faite du comportement de l'architecture 3L-FC-AHBF mais ils ont également souligné les difficultés qui se posent pour atteindre les performances souhaitées pour le convertisseur final.

Chapitre 3 : Création d'un circuit intégré "brique"

Ce chapitre présente la conception d'un circuit intégré (IC) qui inclus les composants actifs requis pour créer l'étage de puissance voulu. Les objectifs que devra remplir l'IC sont décrits. Les limites de la technologie d'intégration utilisée sont présentées et une solution pour les contourner est proposée. La conception des blocs principaux inclus dans l'IC est discutée et les performances de chacun des blocs sont mesurées.

A noter que ce chapitre ne propose pas une présentation détaillée des circuits au niveau transistor des différents blocs, mais s'attarde davantage sur les fonctions qu'ils réalisent.

Motivations et objectifs

La création d'un prototype du convertisseur à la fin du Chapitre 2 a mis en exergue le nombre important de composants discrets requis autour de l'étage de puissance pour que celui-ci puisse fonctionner. Ainsi, pour réduire la taille totale du convertisseur ainsi que pour diminuer son coût, en réduisant notamment le nombre de composants discrets requis, l'intégration sur puce de la partie "active" du convertisseur est visée. La technologie d'intégration employée est un procédé Silicum standard haute-tension dit "bulk", choisi pour son faible coût.

Dans de nombreux convertisseurs de puissance, il demeure difficile d'intégrer les interrupteurs de puissance dans le même boitier que les circuits permettant de les contrôler et de les alimenter. Cependant, dans le contexte basse-puissance rencontré ici, les contraintes thermiques qui pose sur la conception des puces sont amoindries, ce qui permet d'envisager d'intégrer au sein du même boitier l'ensemble des éléments "actifs" de l'étage de puissance. L'objectif du circuit intégré sera de permettre de contrôler l'étage de puissance complet (3L-FC-AHBF) en utilisant seulement deux signaux PWMs basse-tension (par rapport à la masse). De plus, les diverses tensions requises pour alimenter les différents interrupteurs de puissance devront pouvoir être générer à partir d'une seule alimentation auxiliaire - là encore basse-tension par rapport à la masse globale de l'étage de puissance. Enfin, l'aspect "modulaire" de la structure devra également être respecté, le circuit intégré devra donc permettre de créer aussi bien la structure complète du 3L-FC-AHBF que celle simplifiée du 2L-AHBF.

Limites de la technologie et solution proposée

Comme annoncé précédemment, la technologie utilisée pour l'intégration est une technologie Silicium CMOS (Complementary Metal On Semiconductor) haute-tension sur substrat massif (ou "bulk"). Elle est plus ancienne que les technologies de type SOI (Silicon On Insulator) qui sont très utilisées aujourd'hui, mais elle reste tout de même attractive pour son faible coût de fabrication. Cependant, elle présente de nombreuses limitations, notamment en termes d'isolation. Par exemple, les procédés de types "bulk" ne permettent pas d'isoler entre eux deux interrupteurs de puissance dont la source n'est pas connectée à la même référence de tension. L'architecture visée (3L-FC-AHBF) compte quatre interrupteurs dont trois ont leur source connectée à une référence flottante, et il ne sera pas possible de placer ces quatre transistors sur le même substrat avec ce type de technologie. Par ailleurs, le substrat qui accueille les circuits construits avec cette technologie ont généralement une résistivité très élevée, ce qui pourra éventuellement créer des problèmes et générer des pertes comme discuté dans le

Chapitre 5 dédiée aux résultats expérimentaux.

Pour contourner la limite que pose la technologie choisie en termes d'isolation, chaque interrupteur de puissance devra être construit sur un substrat différent. Cela signifie que pour créer l'étage 3L-FC-AHBF il faudra utiliser quatre substrats distincts (et deux pour le 2L-AHBF), ce qui pourrait avoir un impact négatif sur le coût et la taille du convertisseur. L'empreinte du circuit intégré obtenu avec une telle approche pourrait être réduite en utilisant des techniques permettant de regrouper plusieurs puces au sein d'un même boitier (telles que le "Multi-Chip Module" ou le "System-in-Package"). L'implémentation de ces techniques demandera toutefois une étude approfondie sur la faisabilité et la viabilité d'une telle approche, mais ce n'est pas discuté ici.

Pour ne pas avoir à concevoir plusieurs circuits intégrés différents, un circuit unique est crée qui peut être instancié plusieurs fois pour permettre de créer l'étage de puissance voulu. Ce circuit intégré (IC) peut donc être vu comme une "brique" utilisée pour construire la partie active du convertisseur, c'est pourquoi il y est fait référence en tant que "IC brique" dans la suite. L'IC brique regroupe un transistor de puissance de type MOSFET ainsi les circuits requis pour le contrôler et l'alimenter. Chaque brique peut être "programmée" en changeant le signal sur une ou plusieurs de ses pins d'entrées, ce qui permet d'activer/désactiver certains de ses blocs constitutifs, la brique située en haut du pont de l'étage de puissance n'ayant pas besoin des mêmes blocs pour fonctionner que celle située en bas du pont. Les différents blocs qui composent cette IC brique sont :

- Un MOSFET de puissance haute-tension
- Le circuit de commande de la grille de l'interrupteur de puissance (gate-driver)
- Les circuits pour communiquer entre les puces (level-shifter)
- Un circuit pour transmettre la tension d'alimentation vers une référence flottante (bootstrap) ainsi que le condensateur de stockage local associé
- Les circuits permettant de programmer l'IC brique

Ces différents blocs vont permettre d'atteindre l'objectif d'intégration décrit plus haut. Le dimensionnement, le fonctionnement simplifié et les caractéristiques (simulées et/ou mesurées) de chacun des blocs fonctionnels sont discutés dans les prochains paragraphes - à l'exception des circuits permettant la "programmation" de l'IC brique, qui sont principalement composés de multiplexeurs et d'autres portes logiques.

Conception des blocs clés de l'IC brique

Interrupteur de puissance

Pour l'interrupteur de puissance, un transistor MOSFET de type N est sélectionné. Il peut supporter une tension drain-source de plusieurs centaines de volt (typiquement $\sim 600\ V$) mais le courant de drain est limité à moins d'un ampère, du fait de la construction latéral du transistor. Pour caractériser ce composant, deux aspects sont à prendre en compte : son fonctionnement en "statique" et son fonctionnement "dynamique".

Caractérisation statique

Pour la caractérisation statique de ce composant, un traceur de caractéristiques (CS5400 de Iwatsu) est utilisé. Il permet de polariser la grille du transistor et de mesurer le courant et la tension de drain pour obtenir les courbes I-V du transistor. En particulier, il permet d'observer l'influence de la tension de grille et du courant de drain sur la résistance à l'état passant du MOSFET. Cette dernière est particulièrement intéressante pour estimer les pertes par conduction que le composant générera au sein du convertisseur de puissance.

La tension de seuil à partir de laquelle un courant peut circuler dans le drain du transistor est autour de 1,2 V mais pour cette tension, une forte résistance est mesurée entre le drain et la source et le courant de saturation est bas. Plus la tension de polarisation de la grille augmente, plus la résistance à l'état passant diminue, mais au-delà d'une tension de grille-source de 3 V, la diminution observée n'est pas drastique. Pour un courant de drain de 100 mA, augmenter la tension de grille de 3 V à 7 V fait décroitre la résistance à l'état passant de seulement 5% - ce constat reste valable sur l'ensemble de la plage de variation du courant drain sur laquelle le transistor sera utilisé). De ce fait, il apparait suffisant de garantir une tension de polarisation de la grille d'au moins 3 V est suffisant pour que celui-ci se comporte de la manière attendue. Par la suite, la valeur de résistance utilisée pour calculer les pertes par conduction dans les interrupteurs de puissance sera donc la valeur moyenne mesurée de cette résistance à l'état passant qui est proche de 13 Ω.

Caractérisation dynamique

Le comportement en dynamique d'un interrupteur de puissance est fortement lié à la valeur de ses différentes capacités parasites. Deux capacités importantes sont la capacité de sortie C_{oss}, qui se mesure entre le drain et la source, et la capacité d'entrée C_{iss} qui se mesure sur la grille. Plus leur valeur est importante, plus il faudra amener de charges lors de la commutation pour permettre au transistor de changer d'état. Dans ce cas, la capacité de sortie peut-être directement mesurée aux bornes du composants, mais la capacité d'entrée ne pourra être estimer qu'en mesurant la consommation du circuit chargé de piloter la grille du MOSFET de puissance (discuté dans la prochaine Section).

Pour mesurer la capacité de sortie de l'interrupteur de puissance, un traceur de caractéristiques (B1505, Keysight) est utilisé. Pour estimer la valeur de la capacité parasite entre le drain et la source, la grille est tout d'abord reliée à la source ($V_{GS} = 0$ V). Ensuite, une tension DC de polarisation est appliquée sur le drain, car la valeur de la capacité de sortie varie fortement en fonction de la tension V_{DS}. Une composante alternative de faible amplitude et de fréquence fixe (0,1 V et 100 kHz) est ajoutée à la composante DC pour permettre d'estimer l'impédance de sortie du composant et donc la valeur de la capacité. Les résultats confirment que la capacité de sortie varie très largement avec la tension de drain-source, puisqu'elle passe de 650 pF à $V_{DS} = 0$ V à 10 pF à $V_{DS} = 500$ V. Pour une variation de tension de 0 V à 500 V la valeur moyenne de cette capacité est proche de 19 pF.

Circuit de commande de la grille

Pour pouvoir commander la grille de l'interrupteur de puissance, un circuit dédié doit être utilisé pour renforcer les signaux numériques qui ne seraient pas suffisants "forts" pour charger notamment la capacité d'entrée lié à la grille.

Pour renforcer un signal numérique et pouvoir l'utiliser pour rapidement charger/décharger la capacité de grille du MOSFET de puissance, le circuit de commande amplifie peu à peu le signal de contrôle. Ainsi, il est simplement constitué d'une chaine de porte logique de type "NON" ("inverters") de taille croissante.

Pour caractériser ce bloc, plusieurs mesures sont effectuées en ce qui concerne les différents délais et la consommation qu'il génère.

Deux types de délais différents peuvent être mesurés : ceux liés à la transmission du signal de commande au travers de ce bloc et ceux liés à la commande de la grille en elle-même. Pour le premier type, le délai varie selon le type d'information à transmettre (fermeture ou ouverture) et selon la tension d'alimentation de ce bloc. Cependant, en moyenne le délai de transmission d'un signal de fermeture est d'environ 6 ns et de 8 ns pour un signal d'ouverture (pour une tension d'alimentation de 5 V). Pour le second type, le temps de montée ou de descente de la tension de grille est mesuré. Les résultats à 5 V sont d'environ 10 ns pour la montée et 6 ns pour la descente.

Pour la consommation, le courant consommé par le bloc est mesuré pour différente fréquence de pilotage de l'interrupteur de puissance. Une augmentation linéaire du courant absorbé est observée, il est donc possible d'estimer la valeur de la capacité parasite que ce bloc doit charger/décharger à chaque cycle. Ainsi, pour piloter l'interrupteur à une fréquence de 500 kHz, un courant de 290 µA est absorbé ce qui correspond à une capacité de 100 pF. C'est donc cette valeur qui peut être utilisée pour estimer la valeur de la capacité d'entrée C_{iss} de l'interrupteur de puissance.

Level-shifters

Comme décrit dans les objectifs de l'IC brique, les quatre interrupteurs de puissance qui composent l'architecture 3L-FC-AHBF doivent pouvoir être commandés en utilisant seulement deux signaux de contrôle PWM basse-tension et référencés à la masse (et donc directement accessible seulement pour l'IC brique situé en bas du pont). Pour faire cela, il faut transmettre les signaux qui permettent de contrôler ces interrupteurs aux circuits de commande dont la référence est la source des MOSFET de puissance, et est donc flottante. Un bloc fonctionnel est donc requis au sein de chaque IC brique pour permettre de communiquer avec les autres IC brique, pour transmettre les signaux de contrôle référencés à la masse vers les autre références de tensions.

Le bloc requis pour effectuer ce changement de tension de référence est appelé "level-shifter". Dans le cas présent, le circuit "level-shifter" inclus dans l'IC brique se compose en réalité de plusieurs sous circuits. Il est notamment divisé en deux parties : une partie "basse" utilisée dans les puces en bas du pont pour envoyer les signaux de commande ; et une partie "haute" utilisée notamment dans les puces en haut du pont, qui reçoit et interprète les signaux de commandes de l'interrupteur de puissance et les transmet au circuit de commande local.

Le but de cette partie n'est pas de détaillé le fonctionnement détaillé de ce bloc mais plutôt de décrire comment il est utilisé pour atteindre l'objectif d'intégration fixé, et les performances qu'il permet d'obtenir en mesures réelles.

Un bloc "level-shifter" est utilisé pour communiquer entre deux IC brique. Si les deux IC brique appartiennent au même demi-pont (S1/S4 et S2/S3) alors ce circuit se charge de créer un temps mort pour permettre les transitions requises pour la commutation douce comme discuté lors du Chapitre 2. Pour pouvoir commander les quatre interrupteurs de puissance, deux level-shifters sont utilisés pour transmettre les signaux de commande la partie basse du pont vers les interrupteurs situés en haut du pont. Ils sont agencés de telle sorte à équilibrer les délais de transmission de signaux de contrôle, ce qui est important pour assurer que le déphasage entre les deux interrupteurs de puissance situés en haut du pont par exemple.

Une implémentation pratique de ce bloc a réalisé en plaçant deux IC briques sur un circuit imprimé (chacune étant dans un boitier à part) et en les reliant pour créer un demi-pont comme celui requis pour l'architecture 2L-AHBF. La fonctionnalité du level-shifter a été validé pour une tension d'entrée V_{in} inférieure à 40 V : il permet à partir d'un signal PWM référencé à la masse de contrôler les deux interrupteurs de puissance en garantissant un temps mort suffisant entre leur état passant respectif. En revanche, lorsque la tension d'entrée dépasse 40 V, certains défauts apparaissent sur le bloc level-shifter. Dans certains cas, le signal d'ouverture de l'interrupteur de puissance n'est pas correctement transmis/reçu sur la partie haute du demi-pont, ce qui crée des temps où les deux interrupteurs sont simultanément à l'état passant. Ce type de phénomènes peut engendrer de sérieux problèmes car il génère de forts appels de courant, qui pourrait endommager les composants et graver diminuer le rendement du convertisseur.

Du fait des contraintes de temps liées à la thèse, il n'a pas été possible de déterminer avec certitude l'origine de ce problème, ni de concevoir une nouvelle version du bloc level-shifter (ce qui aurait nécessité une nouvelle fabrication de puces). Ainsi pour l'implémentation finale du convertisseur, des composants externes devront être ajoutés pour compenser ce défaut du bloc level-shifter.

Bootstrap

Pour pouvoir contrôler les interrupteurs dont la référence est flottante, une alimentation locale est requise pour chacun d'entre eux. Pour créer ces différentes alimentations localisées, plusieurs options peuvent être envisagées. Une des options consiste à utiliser un convertisseur DC/DC isolé pour créer chacune des alimentations, mais cela risque d'augmenter fortement le coût et la taille du convertisseur au final. Une autre option consiste à créer les alimentations flottantes en partant d'une alimentation auxiliaire et en utilisant un circuit appelé "bootstrap".

Ce circuit est généralement construit autour d'une diode, qui permet de recharger la capacité de l'alimentation flottante lorsque l'interrupteur local (dont la référence est proche de celle de la diode) est passant. Lorsque l'interrupteur se bloque, la diode permet de bloquer la circulation de courant lorsque les deux références de l'alimentation flottante et de l'alimentation auxiliaire s'éloignent, ce qui permet à l'alimentation flottante de conserver une tension stable. Une capacité est donc requise pour chaque alimentation flottante, et elle est donc inclue dans l'IC brique, bien que sa valeur soit limitée à environ 5 nF (du fait des limites de la densité de capacité permise par la technologie utilisée). Dans le cas présent, la diode de bootstrap est remplacée par un transistor qui émule le rôle d'une diode, en ne laissant passant le courant que dans un seul sens.

Dans le cas de l'étage 2L-AHBF, un seul circuit de bootstrap est requis, car l'IC brique en bas du demi-pont est alimentée directement par l'alimentation auxiliaire (V_{AUX}). Le rôle du circuit bootstrap est donc de générer une tension stable dont la référence est la source de l'interrupteur situé en haut du demi-pont.

Dans le cas du 3L-FC-AHBF, la situation se complique car il faut fournir une alimentation locale aux trois interrupteurs dont la référence est flottante en utilisant seulement une alimentation auxiliaire connectée à la masse. Pour cela, chaque IC brique intègre un circuit de bootstrap qui permet de transmettre de l'énergie à l'IC brique connectée juste au-dessus. Cette connexion en cascade permet bien de créer les diverses alimentations flottantes, mais la tension de chaque alimentation diminue au fur et à mesure des circuits de bootstrap, telle que la tension d'alimentation de l'IC brique située tout en haut du pont est bien plus faible que celle de l'alimentation auxiliaire.

Les raisons qui expliquent les difficultés de générer une tension de bootstrap avec une faible chute de tension (par rapport à l'alimentation auxiliaire) sont multiples.

Tout d'abord, comme énoncé plus haut, la capacité associée à chaque alimentation globale à une valeur assez faible (du fait qu'elle est intégrée dans l'IC brique). La tension de l'alimentation flottante est donc assez sensible aux mouvements de charges qui ont lieu lors de l'ouverture/fermeture de l'interrupteur de puissance ou lors des phases de transition pour la commutation douce. Ces derniers sont d'autant plus importants que les capacités parasites qui sont connectées entre les IC briques sont grandes (leur valeur en elle-même est faible, mais elles doivent être chargées sur une grande plage de tension, ce qui au final requiert un grand nombre de charge).

Une autre raison qui peut expliquer la difficulté de réduire la chute de tension entre les alimentations flottantes est le court temps pendant lequel le circuit de bootstrap peut transmettre des charges (et donc de l'énergie) à l'IC brique flottante du dessus. Pour s'assurer qu'une tension minimale est tout de même créée sur chaque alimentation flottante, une valeur minimale pour le temps dans l'état "passant" est fixée pour les interrupteurs situés en bas du pont de l'étage de puissance (la valeur choisie est 300 ns).

En simulation, les résultats obtenus montrent que le circuit de bootstrap crée permet effectivement de générer une tension flottante suffisamment élevée pour les diverses alimentations flottantes. Dans le cas du 2L-AHBF, une tension flottante d'environ 5 V est générée à partir d'une alimentation auxiliaire de 7 V. Dans le cas du 3L-FC-AHBF, une tension de 4 V est créée sur l'IC brique tout en haut du pont si la tension de l'alimentation auxiliaire est de 7 V (mais pour cela, une capacité de bootstrap externe d'environ 50 nF est ajoutée en parallèle de celle incluses dans l'IC brique).

En revanche, des difficultés sont rencontrées lors de l'implémentation pratique de ce circuit, notamment pour mesurer la tension développée sur l'alimentation flottante. Ces difficultés sont surtout liées aux capacités parasites des sondes utilisées (sonde active TT-SI 9101) et au mauvais taux de réjection du mode commun présenté par ces sondes pour des fréquences supérieures à 1 MHz.

Conclusion

Ce chapitre a présenté la conception d'une brique de circuit intégrée utilisée pour créer l'étage de puissance voulu en contournant les limites de la technologie d'intégration visée en termes d'isolation entre composants. Le fonctionnement simplifié et les caractéristiques principales des différents blocs inclus dans l'IC brique sont décrits. Les difficultés rencontrées lors de l'implémentation pratique de certains de ces blocs ne permettent pas de les utiliser complètement dans le convertisseur final, mais les simulations montrent des résultats encourageants. Les défauts observés pourraient être résolus en effectivement une seconde itération de la phase de conception du circuit intégré ou en modifiant l'approche choisie pour la mise en boitier.

Chapitre 4 : Création d'un transformateur

Le Chapitre 4 discute la création d'un transformateur adapté aux convertisseurs haute-tension basse-puissance et aux contraintes de l'application visée. La méthodologie choisie pour la conception de ce composant clé est d'abord introduite, et les choix technologiques primaires sont présentés. Ensuite, l'influence de divers paramètres de conception est étudiée et la/les valeur(s) choisie(s) pour chaque paramètre est explicitée. Pour finir, un petit nombre de solutions est retenu pour être fabriqué et testé au sein du convertisseur haute-tension basse-puissance.

Approche sélectionnée

Pour l'optimisation du transformateur

De nombreuses approches existent pour résoudre le problème posé par l'optimisation du transformateur. Les approches analytiques tentent de modéliser le comportement du transformateur afin de prédire ses performances en se basant sur des équations. Les approches basées sur des algorithmes (géométriques ou autre) sont souvent utilisées pour permettre d'optimiser en particulier un aspect du convertisseur, en utilisant un algorithme pour parcourir un espace de solution afin de trouver les points minimum de la fonction objectif. Cependant, la précision de ces approches est limitée par la précision des modèles qu'ils utilisent, de telle sorte qu'il est difficile dans certains cas d'être certain que l'optimum donné par les précédentes techniques soit bien le meilleur design. En effet, il demeure aujourd'hui encore complexe de modéliser avec précision certains phénomènes liés au fonctionnement du transformateur, comme les pertes fer ou l'augmentation de la résistance des enroulements due aux effets de peaux et de proximité. Ainsi, il apparait raisonnable de fixer comme objectif pour la création du transformateur non pas de créer une solution qui serait la plus optimale (selon les modèles utilisés) mais de proposer plusieurs solutions qui pourraient potentiellement se révéler intéressantes lorsque utilisées au sein du convertisseur haute-tension basse-puissance.

L'approche choisie pour créer ces différentes solutions se base sur l'utilisation d'un Plan d'Expériences. L'idée directrice est de choisir un nombre limité de paramètres, considérés comme les plus importants, et d'étudier l'influence qu'ils ont sur le comportement et les performances du transformateur. Par la suite, si aucun optimum ne peut être identifié pour ce paramètre, un nombre limité de solutions différentes est retenu pour étudier l'impact de la variation de ce paramètre-là.

Pour la réalisation du transformateur

Pour permettre de restreindre l'analyse du transformateur à seulement quelques paramètres, des choix forts concernant sa conception et sa fabrication doivent être faits en amont, en se basant sur les contraintes posées par l'application et l'approche choisie pour la conception du convertisseur haute-tension basse-puissance.

Le choix de la technologie de conception du transformateur se porte sur les transformateurs dits "planaires" qui sont construits en assemblant un noyau magnétique de profil aplati autour d'un circuit imprimé où sont dessinés les enroulements. Les transformateurs planaires présentent des avantages par rapport aux transformateurs bobinés : meilleure diffusion de la chaleur, intégration avec le PCB, comportement en haute-fréquence, etc.

Dans une perspective de bas-coût comme elle est visée ici, les contraintes sur la conception du circuit imprimés où sont situées les enroulements du transformateur sont calquées sur celles généralement proposées comme étant les contraintes "standard" par les fabricants de PCB. Dans la pratique, cela se traduit par un nombre de couches du PCB limité à 4 et par une distance d'isolation/largeur de piste minimum de 100 µm.

Une vue éclatée d'un transformateur planaire similaire à ce qui est visé ici est illustrée dans la Figure 5.

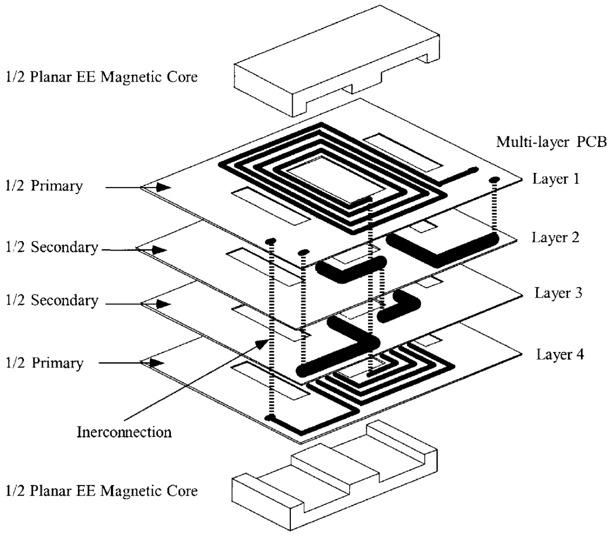


Figure 5: Vue éclatée d'un transformateur planaire

La géométrie du noyau est également décidée rapidement dans la phase de conception du transformateur. Les arrangement E+PLT sont retenus en raison de leur bon compromis entre section et volume pour le noyau ce qui devrait diminuer les pertes fer. D'autres pistes pourraient être étudiées, comme les noyaux EQ dont la partie centrale arrondie permet de réduire l'empreinte des enroulements et donc la taille complète du transformateur planaire, mais faute de temps ils ne sont pas ajoutés à la liste des noyaux utilisés.

Pour étudier l'influence de la taille du noyau sur les performances du transformateur, trois références différentes sont retenues : E18/4/10R, E22/6/16R et E32/6/20R.

Le choix du matériau du noyau magnétique est également fait assez rapidement, en se basant sur la plage de fréquence de fonctionnement prévue pour le transformateur (entre 100 kHz et 1000 kHz). Ainsi, le choix se porte sur les matériaux ferrites doux de type MnZn (Manganèse-zinc) fabriqués par Ferroxcube. Trois matériaux sont disponibles et sont retenus pour évaluer les performances obtenues avec chacun : 3F36, 3F4 et 3F46.

Création d'un modèle simplifié

Pour valider ou non certaines considérations analytiques en ce qui concerne le transformateur, un modèle simplifié permettant d'évaluer les pertes totales du convertisseur est crée. Les modèles existants étant centrés sur des problématiques qui ne sont pas toujours celles des convertisseurs haute-tension basse-puissance et les outils de simulations ne permettant généralement pas de prendre en compte l'ensemble des pertes du convertisseurs (par exemple : difficulté d'estimer les pertes fer dans les simulateurs de circuits électriques classiques), il apparaît opportun de créer un modèle sur mesure pour prendre en compte les spécificités de l'application visée.

Le modèle du convertisseur crée à l'aide de MatLab a deux buts principaux : déterminer si un étage de puissance dans des conditions données est capable d'opérer en commutation douce et évaluer les principales pertes liées aux différents composants du convertisseur.

Pour cela, il prend en entrée plusieurs caractéristiques du convertisseur (tensions d'entrée, sortie, puissance, fréquence de fonctionnement), les caractéristiques des IC brique (résistance et capacité de sortie des transistors de puissance, minimum de temps "passant") ainsi que les entrées liées à la conception du transformateur (choix du noyau, nombre de tours, inductance magnétisante).

Grâce à ces entrées, le script du modèle chargé de valider ou non le comportement en commutation douce du convertisseur calcule les variations des courants et tensions sur le primaire du transformateur sur plusieurs périodes, pour atteindre un état stable. Il est alors possible de conclure si les interrupteurs de puissance peuvent ou non opérer en commutation douce, selon la valeur de la fréquence de fonctionnement, les capacités parasites en jeu et l'inductance magnétisante du transformateur.

Ensuite, en utilisant les données d'entrée concernant le transformateur ainsi que les contraintes liées à la fabrication du PCB, les caractéristiques du transformateur sont calculées.

A partir des formes d'ondes du courant et de la tension dans l'enroulement primaire et des caractéristiques des différents composants de l'étage de puissance, il est possible d'estimer les pertes dans le convertisseur. Pour les interrupteurs, seules les pertes par conduction sont considérées. Pour le transformateur, les pertes par conduction sont calculées dans les enroulements primaire et secondaire, et les pertes fer (à l'intérieur du noyau magnétique) sont estimées à l'aide d'une formule (Steinmetz Généralisé) et des paramètres liés au matériau. Les pertes dans la diode du secondaire sont également prises en compte, en considérant une valeur fixe pour la chute de tension sur ce composant.

En sommant les différentes contributions de ces pertes, il est possible pour le modèle de calculer le rendement offert par le convertisseur tel que décrit avec les paramètres d'entrées du modèle.

Ce modèle a donc permis d'identifier les points de fonctionnement les plus intéressants pour le convertisseur et donc d'en déduire une stratégie pour concevoir le transformateur comme décrit dans les prochains paragraphes.

Paramètres de conception

Lors de la phase de conception du transformateur planaire, l'influence de différents paramètres a été étudiée pour guider les choix de dimensionnement.

Inductance magnétisante

Comme décrit lors du Chapitre 2 lors de l'étude des formes d'onde de la topologie choisie, l'inductance magnétisante du transformateur joue un rôle clé lors des transitions liées à la commutation douce des interrupteurs de puissance. Si sa valeur est trop élevée, l'ondulation du courant primaire sera trop faible pour permettre de compléter les phases de transitions et des pertes à la commutation seront donc générées (et avec elles le bruit électromagnétique associé). En revanche, si sa valeur est trop faible, l'ondulation du courant primaire risque d'augmenter sa valeur efficace et donc les pertes par conduction qu'il génère. Il s'agit donc de trouver une valeur pour l'inductance magnétisante qui permette de compléter les transitions pour la commutation douce tout en réduisant au maximum l'ondulation du courant primaire.

Il apparait que la fréquence à laquelle fonctionne le convertisseur est un des paramètres qui influe le plus sur la valeur maximale que peut prendre l'inductance magnétisante. A basse fréquence, l'inductance magnétisante pourra prendre une valeur élevée tandis qu'à haute fréquence la valeur maximale de l'inductance magnétisante sera réduite.

En utilisant le modèle du convertisseur décrit plus tôt, il est possible d'estimer la valeur maximale de l'inductance magnétisante pour un convertisseur donné opérant à une fréquence donnée. Ou, de manière analogue, il est possible pour une valeur d'inductance donnée de trouver grâce au modèle une fréquence maximale qui permet le fonctionnement en commutation douce tout en réduisant au plus la valeur efficace du courant primaire.

Rapport de transformation

Le rapport de transformation du transformateur, noté N_{tr}, peut se définir en première approximation par le rapport entre le nombre de tours qui composent l'enroulement primaire et le nombre de tours de l'enroulement secondaire.

Pour choisir la valeur la plus adaptée pour ce paramètre, il est utile d'étudier son impact sur le fonctionnement du convertisseur. Notamment, lors du Chapitre 2, ce terme apparaît clairement dans la fonction de transfert du convertisseur. Il est donc utilisé pour fixer la valeur du rapport cycle "effectif" D_{eff}. Par ailleurs, ce dernier terme peut se décomposer comme la somme du rapport cyclique "réel" d'un interrupteur et des temps-morts laissé pour les phases de transitions utiles à la commutation douce.

En considérant les contraintes existantes sur le temps passé à l'état "passant" pour les différents types d'interrupteurs de puissance (200 ns pour les interrupteurs de la partie haute du pont et 300 ns pour ceux de la partie basse), il apparait qu'une valeur donnée du rapport de transformation permet de relâcher au plus la contrainte sur la durée maximale des temps-morts, et donc d'augmenter les performances de l'étage de puissance. L'expression de la valeur optimale du rapport de transformation n'est pas décrite ici mais ses principaux résultats sont présentés.

D'après cette expression, le rapport de transformation optimal pour $V_{in} = 400\ V$, $V_{out} = 12\ V$ et les contraintes pour les temps-morts telles que décrites plus haut, est environ $N_{tr} = 15,2$ à 500 kHz. A noter que cette valeur varie légèrement avec la fréquence, du fait de l'impact sur la durée des temps morts etc, mais qu'elle reste proche de la valeur calculée.

Par ailleurs, en utilisant le modèle du convertisseur, il est possible d'estimer la valeur efficace du courant au sein du primaire du convertisseur pour différentes valeurs du rapport de transformation. Les résultats obtenus montrent que la valeur optimale du rapport de transformation qui permet de réduire au plus la valeur efficace de ce courant tout en gardant un fonctionnement en commutation douce est environ $N_{tr} = 15$.

Nombre de tours

Le nombre de tours des enroulements du transformateur est un paramètre clé qui modifie à la fois les pertes par conduction dans les enroulements et les pertes fer dans le noyau magnétique. A noter que seul le nombre de tours qui composent le primaire du transformateur est discuté ici, mais les raisonnements sont également valables pour le secondaire, dont le nombre de tours est lié à celui du primaire par le rapport de transformation choisi précédemment.

Pour ce qui est des pertes fer, la loi de Faraday indique en effet que pour une tension d'excitation donnée, si le nombre de tours qui compose l'enroulement augmente, alors l'amplitude du champ magnétique à l'intérieur du noyau diminue, et donc les pertes diminuent. Il est également important de noter que la fréquence de l'excitation de tension (qui est la fréquence de découpage du convertisseur) joue un rôle dans la détermination de ces pertes. Ainsi, il est possible de les réduire davantage en augmentant la fréquence de découpage du convertisseur. Enfin, pour les hautes-fréquences, des matériaux magnétiques existent qui permettent de réduire encore davantage les pertes fer. Pour résumer, afin de réduire au plus les pertes fer, il s'agirait pour le transformateur d'avoir des enroulements composés d'un grand nombre de tours et d'opérer à une fréquence de découpage élevée.

Cependant, concernant les pertes par conduction dans les enroulements du transformateur, il apparait que c'est le contraire qu'il faudrait faire pour les diminuer. En effet, lorsque le nombre de tours d'un enroulement augmente, la résistance de cet enroulement augmente également car il devient plus long et moins large (si une largeur finie est considérée pour la fenêtre de bobinage). Par ailleurs, l'augmentation de la fréquence des courants qui circulent au sein des enroulements impacte négativement la résistance de ceux-ci, du fait des effets de peau et de proximité. Par ailleurs, l'analyse du mode de fonctionnement en commutation douce du convertisseur a révélé que lorsque le convertisseur fonctionne a des fréquences élevées, un fort courant circule dans l'enroulement primaire du transformateur pouvant générer d'importantes pertes par conduction.

Pour limiter l'influence de la fréquence sur la résistivité des enroulements, la décision est prise de dessiner les enroulements tel que la largeur d'un enroulement soit égale à la distance entre deux enroulements consécutifs. Cela permet de réduire l'influence l'effet de proximité comme le montre les résultats de simulation à éléments finis 2D qui révèlent que l'augmentation de la résistivité des pistes pour une fréquence d'excitation à 1 MHz est de moins de 10%.

Au final, en ce qui concerne les pertes par conduction, pour les diminuer autant que possible il faudrait avoir un faible nombre de tours et une fréquence de fonctionnement basse.

Une forte contradiction apparaît donc quant au choix du nombre de tours des enroulements du transformateur. Pour augmenter les performances du convertisseur, il faudra réussir à minimiser la somme des pertes fer et des pertes joules. Il s'agira donc de trouver un équilibre entre ces deux types des pertes, en adaptant le choix du nombre de tours à la fréquence de fonctionnement du convertisseur par exemple.

Arrangement des enroulements

Comme indiqué dans le Chapitre 2, il semble important de réduire les capacités parasites liées au transformateur pour faciliter le fonctionnement du convertisseur en commutation douce, car celles-ci devront être chargées/déchargées durant chaque période de découpage. Pour cela, l'influence de l'arrangement des enroulements du transformateur sur les couches du circuit imprimé (PCB) est ici étudiée.

Deux capacités parasites différentes sont prises en compte pour cette analyse. La capacité inter-enroulement, qui se forme entre les pistes appartenant à des enroulements différents du fait des surfaces métalliques en regard. Ici, il s'agit surtout de la capacité entre le primaire et le secondaire du transformateur C_{ps}. Ensuite, la capacité de l'enroulement primaire lui-même est prise en compte, du fait de son étalement sur plusieurs couches du PCB, il peut se créer une capacité entre un bout de l'enroulement à un autre, du aux surfaces métalliques en regard également. C'est la capacité "self" du primaire $C_{p\ self}$.

En général lors de la conception d'un transformateur planaire, il est surtout question de diminuer l'influence du courant circulant dans les pistes sur une couche sur la résistivité des pistes des autres couches. Ici, les courants circulant dans les divers enroulements étant relativement réduits, il apparait plus important de réduire les capacités parasites qui se créent entre ces enroulements. Ainsi, plutôt que d'utiliser un arrangement des enroulements de type "entrelacé" ou "intercalé" - pour lequel il y a une alternance entre enroulement primaire puis secondaire sur les couches successives du PCB - un arrangement sur-mesure est considéré ici. Dans cet arrangement, l'enroulement primaire est réparti sur les deux couches supérieures du PCB tandis que l'enroulement secondaire est placé sur la couche inférieure du PCB.

Grâce à cet arrangement, la capacité inter-enroulement est fortement diminuée car la distance entre les surfaces métalliques en regard est bien plus grande que dans le cas d'un arrangement "intercalé". A noter qu'il est possible de réduire encore davantage cette capacité parasite en regroupant tout l'enroulement primaire sur la couche supérieure, ce qui augmente encore la distance inter-enroulement, mais cela limite également le nombre de tours maximum de l'enroulement primaire.

Cependant, un des dangers de cet arrangement est qu'il risque de créer une forte capacité "self" pour l'enroulement primaire, les surfaces métalliques en regards étant proches les unes des autres. Pour tenter de diminuer cette capacité, deux changements sont opérés. Tout d'abord, les pistes qui composent l'enroulement primaire sont décalées entre les deux couches, ce qui augmente la distance entre elles et diminue la capacité. Par ailleurs, cette capacité "self" est fortement dépendante de la différence de potentielle entre les surfaces en regards : si la différence de potentielle est faible, alors la capacité créée est faible aussi. Ainsi, la connexion des différentes parties de l'enroulement primaire est modifiée afin de diminuer la différence de potentielle entre les surfaces en regard.

Solutions retenues

A présent que l'influence des différents paramètres de dimensionnement du transformateur a été étudié, un petit nombre de solutions candidates est retenu pour être fabriqué puis testé au sein du convertisseur haute-tension basse-puissance.

Les solutions retenues pour le design du transformateur sont réparties en trois "famille" en fonction de leur fréquence d'utilisation lorsque utilisé dans le convertisseur.

Solutions basse fréquences ($< 400\ kHz$)

Ce type de solution va tout d'abord se caractériser par un grand nombre de tours dans l'enroulement primaire (47 tours voire 61 tours) pour tenter de diminuer les pertes fer au sein du noyau magnétique. Du fait du nombre élevée de tours requis, ce type de solution n'est pas réalisable pour le plus petit noyau magnétique choisi (E18) et requiert d'utiliser les noyaux plus imposant (E22, E32). Du fait des surfaces plus importantes, les capacités parasites pour ce type de solutions seront assez élevées, pouvant atteindre par exemple 50 pF au total pour les plus gros noyaux.

Solutions haute fréquences ($> 1000\ kHz$)

A l'inverser des solutions basse-fréquences, ce type de solutions comporte des enroulements avec un faible nombre de tours (15 tours au primaire) pour diminuer leur résistance parasite. Des noyaux de faible taille (E18, E22) sont utilisés par créer ces solutions qui sont donc potentiellement plus compactes que celles fonctionnant à basse-fréquence. Les capacités parasites liées à ces solutions sont à l'inverse très faible, pouvant atteindre moins de 10 pF pour les plus petites d'entre-elles.

Solutions moyenne fréquence

Enfin, entre les solutions haute-fréquence et les solutions basse-fréquence, une troisième famille de solutions est intercalée. Les caractéristiques en termes de nombre de tours, de fréquence d'utilisation et de capacités parasites de ces solutions se trouvent à mi-chemin entre les deux autres familles et permettent donc d'explorer une large gamme de fréquence de fonctionnement.

Conclusion

Ce Chapitre 4 a présenté la méthodologie utilisée pour concevoir un transformateur adapté aux convertisseurs haute-tension basse-puissance. La méthode retenue pour explorer l'espace des solutions possibles (Plan d'Expérience) a d'abord été introduite. Les choix technologiques de base effectués en amont de la phase de conception ainsi qu'un modèle simplifié du convertisseur, pouvant permettre d'évaluer les caractéristiques d'un grand nombre de solutions, ont été présentés. L'influence de quelques paramètres clés sur les performances du transformateur a ensuite été étudiée pour permettre leur dimensionnement. Au final, un petit nombre de solutions est proposé pour être testé au sein du convertisseur lors de l'implémentation pratique de celui-ci.

Chapitre 5 : Tests et mesures expérimentales

Le chapitre 5 présente les tests et résultats obtenus lors de l'implémentation pratique du convertisseur haute-tension basse-puissance visé. Les tests effectués ainsi que le matériel utilisé est décrit dans un premier temps. Puis, les résultats fonctionnels sont présentés pour les deux versions du convertisseur. Les résultats des performances de ces convertisseurs sont ensuite discutés et comparés avec les prédictions du modèle ainsi qu'avec les solutions existantes, pour permettre de conclure sur l'intérêt de l'approche choisie.

Tests et équipements

Afin de valider les précédentes étapes de conception du convertisseur haute-tension basse-puissance, un nouveau prototype est construit en utilisant les IC brique intégrant les composants actifs et les divers transformateurs crées. Le circuit imprimé crée pour ce prototype se divise en deux parties. Une est dédiée à l'étage de puissance et l'autre à la partie contrôle.

L'étage de puissance est principalement constitué des interrupteurs de puissance inclus dans les IC brique ainsi que du transformateur sur-mesure. Le reste des éléments qui composent l'étage de puissance sont des composants existants dont les caractéristiques sont connues : pour les condensateurs haute-tension (C_{fly}, C_p) des condensateurs céramiques (600 V, 1 µF) sont utilisés ; le condensateur de sortie est également de type céramique mais de tension plus réduite (16 V, 1 µF) ; la diode secondaire est de type Schottky (60 V, 1 A ; PMEG6010CE, Nexperia).

La partie contrôle de la carte est composée des circuits permettant de créer les signaux de commande des quatre interrupteurs de puissance. A partir de deux signaux PWM déphasés d'environ 180°, les signaux de contrôle des deux demi-ponts sont générés. En particulier, un circuit de type RC construit avec un petit condensateur et un potentiomètre permet de régler le temps mort associé à chaque interrupteur de puissance, pour permettre à celui-ci d'opérer en commutation douce. A noter que le rapport cyclique et la fréquence des divers signaux peuvent être modifiés directement sur le générateur de formes d'ondes utilisé pour créer les signaux PWM (81130A de Agilent).

Pour tester le convertisseur dans des conditions proches de son utilisation réelle, la tension en entrée est pilotée à 400 V ou 800 V à l'aide d'une alimentation de type SMU (Source Measurements Unit; 2410 de Keightley) qui permet de mesurer le courant DC fourni en entrée du convertisseur. Une charge électronique DC (BK precision 8600) est placée en sortie du convertisseur pour imposer un courant constant en sortie tout en mesurant la tension sur le condensateur de sortie. Une alimentation auxiliaire fournie l'énergie requise pour les IC brique pour fonctionner mais la puissance qu'elle délivre n'est pas prise en compte lors des calculs de rendement du convertisseur.

Résultats fonctionnels

Pour le 2L-AHBF

La configuration 2L-AHBF est mise en œuvre dans un premier temps. Seulement deux IC brique sont utilisées pour créer l'étage de puissance, qui est testé pour $V_{in} = 400\ V$, $V_{out} = 12\ V$, $P_{out} = 1\ W$ et $f_{sw} = 1\ MHz$.

Les résultats obtenus montrent que les formes d'ondes mesurées (tensions au point milieu et sur la capacité primaire C_P, courants primaire et secondaire) sont conformes à celles obtenues en simulation. En particulier, les phases de transitions requises pour la commutation douce des interrupteurs de puissance ont bien lieu. En mesurant la vitesse de transition de la tension au point milieu et les courants qui circulent dans le convertisseur durant ces phases, la valeur de la capacité parasite (dé)chargée est estimée et elle est proche de la valeur prédite par le modèle. Par ailleurs, la mesure de la tension sur la capacité primaire C_P et de la tension en sortie sont en accord avec les prédictions faites par l'expression trouvée pour la fonction de transfert principale du convertisseur.

En faisant varier la valeur de l'inductance magnétisante du transformateur (en changeant par exemple la valeur de l'entrefer), il est possible d'étudier le comportement du convertisseur 2L-AHBF sur une large gamme de fréquence. En particulier, il est possible pour chaque valeur d'inductance magnétisante de trouver la fréquence de découpage maximale qui permet de réduire au plus le courant primaire efficace tout en garantissant que l'étage de puissance opère en commutation douce. Pour des valeurs d'inductance entre 335 μH et 3.0 mH, la fréquence de découpage varie de 200 kHz jusqu'à 1000 kHz.

Les résultats obtenus pour cette fréquence maximale sont ensuite comparés avec les prédictions faites par le modèle simplifié décrit dans le Chapitre 4 qui permettait de prédire cette valeur, et la comparaison révèle que les deux valeurs sont très proches, ce qui confirme la pertinence du modèle construit ainsi que de l'estimation des capacités parasites en jeu.

Pour le 3L-FC-AHBF

Dans un deuxième temps, la configuration 3L-FC-AHBF est mise en place, en utilisant cette fois-ci quatre IC brique pour l'étage de puissance, qui est testé dans le conditions suivantes : $V_{in} = 800\ V$, $V_{out} = 12\ V$, $P_{out} = 1\ W$ et $f_{sw} = 500\ kHz$.

Les résultats des principales formes d'ondes sont également très semblables à ceux obtenus en simulation. La fonction de transfert est validée pour cette version du convertisseur en mesurant la tension sur la sortie et la capacité primaire C_P. Les phases de transitions sont également proches de celles attendues, la seule différence étant que les phases associées aux transitions d'un demi-pont (S1/S4) sont plus lentes que celles associées à l'autre demi-pont (S2/S3). Cela peut s'expliquer par la valeur légèrement différente de la capacité parasite totale connectée à chaque demi-pont, qui semble supérieure pour le demi-pont S1/S4.

La tension sur la capacité flottante C_{fly} n'est pas directement mesurée mais peut être facilement estimée en observant la tension au point milieu V_{SW2} lorsqu'un des interrupteurs du haut est passant (S1 ou S2). Il apparait que cette tension est légèrement différente lors des deux demi-périodes, ce qui indique que la tension sur la capacité flottante n'est pas exactement celle attendue (environ 387 V mesuré contre 400 V attendu). Pour parvenir à équilibrer la tension sur les interrupteurs de puissance, la tension de la capacité flottante doit être proche de sa valeur idéale. Pour cela, le déphasage entre les signaux PWM utilisés pour générer les signaux de contrôle des interrupteurs de puissance est légèrement modifié, passant de 180° à 177°. Grâce à cette modification, la tension estimée de la capacité flottante se rapproche désormais bien plus de sa valeur idéale de 400 V. Une explication pour ce déséquilibre sur la tension "naturelle" de la capacité flottante est sans doute liée à la valeur différente des capacités parasites connectées aux deux demi-ponts, qui créent de légères différences dans les formes d'ondes lors des commutations et donc un déséquilibre sur la valeur de la tension de la capacité flottante.

Enfin, comme pour la configuration précédente, il est possible de mesurer la fréquence maximale de découpage qu'il est possible d'atteindre en respectant les conditions de la commutation douce pour différentes valeurs de l'inductance magnétisante. Pour chaque valeur d'inductance magnétisante, la valeur mesurée de la fréquence maximale se révèle être proche de la valeur prédite pour cette fréquence maximale par le modèle. La différence est sans doute due aux capacités additionnelles qui perturbent l'équilibre de la tension aux bornes de la capacité flottante, mais les résultats de mesures et de prédiction restent tout de même peu éloignés, ce qui confirme encore une fois la validité l'analyse de la topologie et des mécanismes de la commutation douce.

Mesures des performances

Les mesures des performances du convertisseur sont découpées en trois étapes. Dans un premier temps, les différents transformateurs proposés à la fin du Chapitre 4 sont testés, pour identifier les solutions les plus intéressantes. Ensuite, les performances mesurées avec la configuration 2L-ABHBF sont présentées. Pour finir, les performances du convertisseur 3L-FC-AHBF sont décrites. Dans chacun des cas, seul le rendement du convertisseur est mesuré pour évaluer ses performances. D'autres paramètres pourraient être également significatifs (ondulation de la tension de sortie, bruit électromagnétique généré, etc.) mais ne peuvent être intégrés faute de temps.

Transformateurs

Parmi l'ensemble des solutions proposées pour le transformateur, trois familles de solutions ont été identifiées, selon la fréquence d'utilisation du transformateur. Dans l'ensemble, ce sont les solutions orientées vers un fonctionnement basse-fréquence qui semblent offrir le meilleur rendement pour le convertisseur : avec un noyau type E22, une solution basse-fréquence avec un grand nombre de tours permets d'atteindre l'objectif de rendement de 85% pour une charge de 1 W. A l'inverse, les solutions haute-fréquence sont limitées à un rendement inférieur à 70% dans les mêmes conditions.

En ce qui concerne l'influence de la taille du noyau, celle-ci permet bien d'améliorer le rendement, mais pour les noyaux les plus volumineux, le gain en rendement ne justifie sans doute pas la large augmentation de l'empreinte du transformateur. Les noyaux les plus compacts au contraire propose un compromis intéressant entre taille et performances, mais le rendement reste tout de même inférieur à 75% pour les meilleurs. Les solutions avec un noyau de taille moyenne (type E22) semble offrir le meilleur compromis de le cas présent.

Enfin, concernant le matériau magnétique qui compose le noyau, il apparaît que le matériau 3F46 présente des performances plus élevées que les deux autres sur l'ensemble de la gamme de fréquence. Il semble donc intéressant de privilégier l'emploi de ce matériau avec très basse pertes fer pour augmenter les performances du convertisseur.

Configuration 2L-AHBF

Le convertisseur construit en utilisant la configuration 2L-AHBF pour l'étage de puissance est testé avec les meilleurs solutions pour le transformateur, et dans des conditions nominales pour la tension d'entrée et de sortie (400 V-12 V) et pour une charge de 1 W dans un premier temps. Pour les transformateurs "basse-fréquence", le rendement du convertisseur dépasse 85% et ce qui permet donc d'atteindre l'objectif visé. En revanche, les solutions orientées vers les moyennes ou les hautes fréquences ne permettent pas d'atteindre ces objectifs, le rendement mesuré pour ces solutions étant bien plus faible que ce qui était prédit par le modèle simplifié du convertisseur. Une étude est proposée dans une prochaine section pour tenter de déterminer l'origine des pertes additionnelles qui plombent le rendement à ces fréquences.

Dans un second temps, la puissance en sortie du convertisseur est graduellement augmentée de manière à mesurer l'évolution du rendement en fonction de ce paramètre (un maximum de 4 W est placée sur la sortie pour demeurer dans une optique basse-puissance). Pour l'ensemble des transformateurs testés, augmenter la puissance en sortie permet d'améliorer significativement les performances du convertisseur : pour une solution basée sur un noyau type E18, le rendement passe de 70% à 1 W à 84% à 4 W. Il en va de même pour les différents transformateurs testés, les plus performants ayant un rendement allant jusqu'à 88% pour une charge de 3 W.

Configuration 3L-FC-AHBF

Le convertisseur construit en utilisant la configuration 3L-FC-AHBF pour l'étage de puissance est testé avec les meilleurs solutions pour le transformateur, et dans des conditions nominales pour la tension d'entrée et de sortie (800 V-12 V) et pour une charge de 1 W dans un premier temps. Pour les transformateurs "basse-fréquence", le rendement du convertisseur est proche de 85% et ce qui permet donc d'atteindre l'objectif visé. En revanche, les solutions orientées vers les moyennes ou les hautes fréquences présentent là encore un rendement plus bas que celui attendu.

Dans un second temps, la puissance en sortie du convertisseur est graduellement augmentée de manière à mesurer l'évolution du rendement en fonction de ce paramètre (un maximum de 4 W est placée sur la sortie pour demeurer dans une optique basse-puissance). Pour cette configuration, il apparait également que pour l'ensemble des transformateurs testés, augmenter la puissance en sortie permet d'améliorer significativement les performances du convertisseur : pour une solution basée sur un noyau type E18, le rendement passe cette fois-ci de 67% à 1 W à 82% à 4 W. Il en va de même pour les différents transformateurs testés, les plus performants ayant un rendement allant jusqu'à 87% pour une charge de 3 W.

Origine des pertes à moyenne et haute fréquences

Comme énoncé plus tôt, les pertes mesurées au sein du convertisseur (dans ses deux versions 2L-AHBF et 3L-FC-AHBF) sont plus bien importantes que celles prédites par le modèle lorsque la fréquence augmente au-delà de 400 kHz. Pour comprendre l'origine de ces pertes additionnelles, les performances mesurées pour deux points de fonctionnement du même convertisseur sont comparées : l'un à 400 kHz tandis que l'autre est autour de 1000 kHz. La différence en termes de pertes entre les mesures et les prédictions est d'environ 50 mW pour le premier point et de 350 mW pour le deuxième. Il semblerait donc que des pertes apparaissent à haute-fréquence qui ne sont pas prévues par le modèle.

Des mesures de températures des divers composants du convertisseur à la caméra thermique sont menées, pour tenter de déterminer la source de ces pertes. Pour les deux points de fonctionnement, une température similaire est mesurée sur le transformateur et ses enroulements, ce qui concorde avec les prédictions du modèle. En revanche, la température mesurée sur les IC brique est plus élevée pour le 2e point de fonctionnement.

En étudiant plus en détail le modèle dans le logiciel de simulation circuit utilisé des interrupteurs de puissance, il apparaît qu'une importante résistance est connectée en série avec la capacité de sortie de ceux-ci. La présence de cette résistance a par ailleurs été confirmée par des mesures d'impédances des interrupteurs (avec un modèle C_S, R_S contrairement aux mesures faites durant le Chapitre 3 faites avec un modèle C_p, R_p) qui ont révélé que cette résistance peut avoir une valeur de plus de 150 Ω. Cette résistance pourrait générer d'importantes pertes durant les transitions liées à la commutation douce des interrupteurs de puissance, durant lesquelles les capacités de sortie des interrupteurs sont chargées/déchargées.

Bien que le manque de temps n'ai pas permis d'effectuer des tests supplémentaires sur l'origine de ces pertes, il semblerait que les interrupteurs de puissance soient, en partie au moins, responsable des pertes additionnelles observées lorsque le convertisseur opère à haute ou à moyenne fréquence. Mais d'autres phénomènes pourraient également en partie expliqué ces pertes, notamment dans le substrat des IC brique dont la résistivité est élevée.

Comparaison avec les solutions existantes

Pour comparer les performances obtenues avec le convertisseur construit avec celles des solutions existantes, les solutions ayant le meilleur compromis taille-rendement sont retenues. Chaque version du convertisseur (2L-AHBF et 3L-FC-AHBF) est comparé aux solutions existantes sur une plage de tension-puissance similaire.

Convertisseurs 400 V-12 V

La comparaison des meilleurs convertisseurs 400 V-12 V proposés dans cette thèse avec les solutions existantes révèlent que la solution basée sur un noyau E22 permet d'améliorer le rendement du convertisseur bien qu'elle augmente l'empreinte occupée par le transformateur. La solution basée sur le noyau E18 permet de réduire cette empreinte mais les performances sont plus basses, bien qu'elles restent au niveau des meilleurs solutions existantes (84%). Par ailleurs, les fréquences de fonctionnement plus élevée des solutions proposées pourraient permettre de réduire la taille d'autres composants passifs, comme ceux utilisés pour le filtrage en entrée par exemple. Le transformateur planaire enfin devrait permettre de réduire la hauteur du module du convertisseur et donc de réduire son volume.

Convertisseurs 800 V-12 V

Pour les convertisseurs 800 V-12 V proposés, le rendement est significativement meilleur que celui-ci des solutions existantes. Les solutions utilisant les noyaux E18 et E22 permettent d'obtenir un rendement supérieur à 82% et 87% respectivement contre moins de 70% pour les solutions existantes. La taille du transformateur est assez grande, mais encore une fois cela est à mettre en perspective avec les bénéfices que la solution proposée pourrait apporter sur la taille des autres composants passifs et pour la hauteur (et donc le volume) du module du convertisseur complet.

Conclusion

Ce chapitre a présenté les mesures effectuées sur le convertisseur construit en assemblant les IC brique et le transformateur sur-mesure conçus précédemment. Le banc de tests utilisé a tout d'abord été présenté. Les résultats fonctionnels du convertisseur ont validé l'analyse faite de la topologie ainsi que des mécanismes de commutation douce prédits par le modèle simplifié. Le rendement obtenu pour les deux versions du convertisseur a été mesuré. Si les performances du convertisseur à basse fréquence sont en phase avec les objectifs fixés par les conditions initiales, celles-ci se dégradent rapidement à mesure que la fréquence de découpage augmente sans que cela puisse être expliqué par les pertes incluses dans le modèle simplifié décrit dans le Chapitre 4. L'origine de ces pertes a été étudié et il se pourrait qu'elles soient dues à la présence d'une importante résistance en série avec la capacité de sortie des interrupteurs de puissance. Toutefois, les performances obtenues avec les meilleurs transformateurs sont au-dessus de celles offertes par les solutions existantes, notamment pour les convertisseurs 800 V.

Conclusion Générale et Perspectives

Certaines applications requièrent un convertisseur DC/DC isolé avec une grande tension en entrée et une faible tension-puissance en sortie. Dans cette thèse, la conception d'un tel convertisseur a été discuté et des approches ont été proposés pour réduire sa taille, son coût et ses pertes.

Premièrement, une courte analyse des solutions déjà existantes a été proposée, et leurs limites ont été soulignées. Elles semblent être en partie imputable à l'architecture Flyback qui est utilisée dans la plupart des solutions isolées et basse-puissance. Ainsi, une étude topologie a été menée en se basant sur les contraintes de l'application visé et de l'approche choisie, notamment en termes de technologie d'intégration. Les convertisseurs Multi-Niveaux à Capacité Flottante ont été retenu car ils présentent un compromis intéressant entre complexité et performances de l'étage de puissance du convertisseur. Son comportement théorique a été analysé, pour identifier certains des paramètres de conception les plus important, notamment pour les mécanismes de commutation douce. Un premier prototype construit avec des composants discrets a confirmé les difficultés qui se posent pour créer une solution haute-tension basse-puissance avec un haut rendement, et a par ailleurs souligner l'importance de l'intégration de la partie active pour diminuer la taille et le nombre de composants du convertisseur. Un circuit intégré incluant les interrupteurs de puissance ainsi que les circuits pour les contrôler et les alimenter a été conçu en utilisant une technologie Silicium bas coûts. L'IC brique a été proposée pour contourner les limites en termes d'isolation de la technologie "bulk" Silicium haute-tension. Du fait des fortes contraintes qui pèsent sur ce composant, le transformateur ne peut être intégré dans un premier temps dans le même boitier, et sa conception a donc été étudié plus en détails, pour permettre de réduire sa taille et d'augmenter ses performances. En analysant l'influence de quelques paramètres de conception, plusieurs solutions ont été proposées pour ce composant en se basant sur un Plan d'Expériences. Au final, un nouveau prototype du convertisseur construit à l'aide des IC brique et des transformateurs sur-mesures crées est mesuré. Les formes d'ondes ont permis de valider les analyses faites en amont sur son comportement et ses modes de fonctionnement. Le rendement mesuré pour certaines des solutions a montré que le convertisseur peut répondre favorablement aux exigences du cahier des charges qui visaient un rendement supérieur à 85%. Cependant, il est apparu que seules les solutions opérant à des fréquences assez basses peuvent atteindre ces performances tandis que les solutions fonctionnant à moyennes et hautes fréquences présentent un rendement plus bas que prévu, sans que cela ne puisse être expliqué. Pour tenter de trouver l'origine de ces pertes additionnelles, une étude a été menée et a conduit à considérer des pertes par conduction durant les transitions pour la commutation douce - dues à la résistance en série des capacités de sortie des interrupteurs de puissance. Finalement, le rendement mesuré avec quelques-unes des solutions proposées est comparé avec celui affiché par les solutions existantes, et il apparait qu'un gain significatif de rendement est obtenu grâce à l'approche choisie, notamment pour les convertisseurs opérant avec une tension de 800 V en entrée.

Viabilité de l'approche

Avant de présenter quelques perspectives pour les conceptions futures de convertisseur haute-tension basse-puissance, il peut être intéresser de question la viabilité de l'approche sélectionnée et de la solution qu'elle a conduit à créer, dans une approche de préparation pour une éventuelle industrialisation.

Dans ma compréhension, il y a deux principaux obstacles qui pourraient freiner le développement industriel d'une solution comme celle proposée : l'intégration monolithique de plusieurs circuits intégrés et la fiabilité de l'architecture choisie basée sur les circuits Multi-Niveaux à Capacité Flottante.

Du fait des limites en termes d'isolation entre composants de la technologie d'intégration choisie (bulk Silicium haute-tension), tous les interrupteurs de puissance doivent être placés sur un substrat différent. Cependant, pour permettre d'atteindre les objectifs de faible taille et pour réduire l'influence de certains éléments parasites entre les IC brique, ces dernières devraient toutes être placées au sein d'un même boitier, en utilisant des techniques telles que le "Multi-Chip Module" (MCM). Mais les coûts de ces techniques avancées pourraient bien rentrer en contradiction avec les objectifs initiaux de bas coût utilisés comme base pour tout le développement.

Par ailleurs, la fiabilité de l'étage de puissance proposé devrait être correctement étudiée. Sans tenir compte des problèmes rencontrés lors de l'implémentation pratique pour plusieurs blocs (level-shifter, bootstrap), la complexité des convertisseurs Multi-Niveaux à Capacité Flottante devrait avoir une influence négative sur la robustesse de l'étage de puissance, comparé à une architecture Flyback qui est très robuste mais peu efficace à haute-tension. La séquence de démarrage du Multi-Niveaux à Capacité Flottante pourrait générer plusieurs types de problèmes, par exemple pour la charge de la capacité flottante, etc. Cela ne signifie pas qu'il ne faudrait pas utiliser cette solution, mais le contexte de l'application visée (sureté dans l'automobile) demandera des garanties en termes de robustesse qu'il pourrait être difficile d'atteindre avec l'architecture proposée.

Perspectives

Pour chacun des aspects du convertisseur qui a été étudié, il y a des perspectives qui s'offrent quant à ce qu'il pourrait être fait pour améliorer/modifier les solutions proposées.

Une technologie d'intégration différente

Comme discuté durant le Chapitre 2, le choix de la topologie du convertisseur est fortement influencé par le choix de la technologie utilisée pour l'intégration des composants passifs. Dans ce travail, la technologie bas-coût limite les possibilités d'intégration d'un trop grand nombre de composants, cependant, si un autre procédé était envisagé, il pourrait mener à choisir une topologie différente. Par exemple, il serait intéressant de construire un convertisseur plus optimisé avec un premier étage de type "Capacités Commutées" car cette structure permettrait de potentiellement réduire la taille du transformateur requis pour le deuxième étage.

Bien que le choix d'une technologie plus récente et plus avancée puisse affectée de manière négative le coût de fabrication, il pourrait être compensé par l'intégration facilitée des divers composants actifs au sein du méme boitier - contrairement à la technologie d'intégration actuelle qui requiert des techniques spéciales pour placer plusieurs substrats au sein d'un même boitier.

Finalement, changer la technologie de d'intégration pourrait également aider à réduire les pertes qu'il semble y avoir durant les phases de commutation douce, dues à la résistivité élevée du substrat avec le procédé actuel (Silicium "bulk" haute-tension).

Nouveau design pour l'IC brique

Pour ce qui est de l'IC brique en elle-même, une nouvelle phase de conception des blocs qui la composent pourrait permettre d'augmenter ses performances et sa robustesse, en particulier pour les level-shifters et le bootstrap. L'influence de la taille des MOSFET de puissance pourrait également être étudiée. Finalement, les blocs requis pour la phase de démarrage de l'IC brique pourrait être ajoutés pour lui permettre de démarrer sans alimentation auxiliaire, tout comme le bloc générant les signaux PWM qui pourrait être implémenté.

Transformateur

La forme du noyau magnétique du transformateur pourrait être explorée plus en détail. Par exemple, les noyaux de type EQ avec une partie centrale arrondie pourraient permettre de réduire l'empreinte du transformateur, en diminuant l'espace occupé par les enroulements. Par ailleurs, il pourrait également être intéressant de construire une comparaison entre les transformateurs planaires proposés et ceux "classiques" bobinés, pour valider l'approche choisie. D'autres paramètres pourraient également être étudiés plus en détail, comme la valeur du rapport de transformation à choisir en fonction de la tension d'entrée, ou les performances vis-à-vis du bruit électromagnétique du transformateur.

Pour réduire encore davantage la taille du transformateur, l'utilisation de technologies d'intégration avancées de ce composant pourrait être envisagé. En effet, des techniques permettent aujourd'hui d'intégrer le noyau du transformateur au coeur du circuit imprimé ou directement dans le même boitier que les composants actifs. Cependant, il pourrait demeurer difficile d'obtenir les performances visées en termes de rendement en utilisant ce type d'approches.

Contrôle du convertisseur et cahier des charges avancés

Pour le convertisseur global, le rendement pourrait être amélioré en utilisant les techniques de contrôle avancées qui lui permette de fonctionner au point de charge où il présente les meilleures performances. Le cahier des charges de l'application devrait être raffiné encore sur plusieurs aspects (volume/empreinte maximum, spectre EMI, ondulation de la tension de sortie, etc.) pour permettre de confirmer ou non les bénéfices de l'approche choisie comparée à celle "classique" basée sur l'architecture Flyback.

General introduction

The high-voltage DC buses are expending in some large-market applications like electric vehicles and renewable energies. In parallel, several applications require to be powered directly from the main input supply, often for safety reasons. The two issues combined create the need for an isolated DC/DC converter with a high-input voltage capability but a low-voltage, low-power output.

The Pyroswitch used in some electric vehicles to physically disconnect the main battery in case of accident is one example of existing safety solution. It must be supplied directly from the high-voltage battery using an isolated DC/DC converter with a low-voltage output and it requires only a small amount of power. In the automotive context, the constraints on the DC/DC converter are strong, especially regarding the size, cost and efficiency.

Due to the novelty of these application cases, such converters are not extensively covered in the literature, hence the objective of the present work to study their design.

Background and selected approach

In the vast world of low-power DC/DC converters, it is possible to distinguish two approaches in particular.

One approach is the integration which tends to increase the number of components of the converter that can be included inside a tiny module or package, with techniques like MCM (Multi-Chip Module), PSiP (Power Supply in Package), PSoC (Power Supply on Chip), etc. Recently, the use of wide band-gap components, that allow to reach a higher switching frequency than standard Silicon devices, enables a size reduction of many passive components up to the point where they can be more and more integrated in the package or on chip along with the active devices, thus allowing to decrease the converter size and cost (although the last one depends on the integration technology used). However, it remains challenging to create efficient isolated solutions that can withstand a high input voltage using this type of approach (the MCM example from [1] is limited to 100 V).

On the other hand, a different approach is to regroup many discrete components and to assemble them inside a custom module. It allows to create solutions with much greater capability, since high-performance components can be used. The maximum voltage capability can thus be increases and the isolation strength can be reinforced (power module from [2] can withstand up to 1 kV). However, this type of approach suffers from an footprint increase when compared to integrated solutions (as pictured in Figure 6) and a higher cost due to the many discrete components it is composed of.

Figure 6: Example of size comparison of a power module [2] and a Multi-Chip Module [1]

The approach that is targeted in this work is halfway between the two previous solutions. The idea is to use the possibilities offered by active components integration to propose new converter architectures and increase the switching frequency. This way the few components that could not be integrated together with the actives (due to their size or manufacturing constraints) could be shrunk, allowing to create a more compact solution than with a standard power module approach. To keep a low-cost perspective, the selected technology for the integration of the active devices will be a mere classical bulk Silicon process.

Objective and scope of the thesis

A simple set of specifications is derived from the first application indications, to create a more concrete framework for the thesis. They are summarized in Table 1. They roughly correspond to the main DC buses of today's electric cars' main battery (i.e. 400 V and 800 V). In both cases, a ±25% range is targeted for the main input voltage. The rest of the specification parameters are identical.

Table 1: Converter's general specifications

Parameters	**Value**	
Nominal input voltage [V]	400	800
Input voltage range [V]	300-500	600-1000
Output voltage [V]	12	
Output power [W]	$\sim$1	
Isolation required?	Yes	
Efficiency	$\geq 85\%$	

To meet the requirements with the selected approach, various aspects of the converter's design are explored in this work. For each of them, the particularity of the high-voltage, low output power converter under study is taken into account to come up with a suitable solution. Three aspects are discussed principally:

- Choice of the converter's topology
- Design of an integrated circuit (active components)
- Design of a custom transformer (may not be integrated, probably the bulkiest device in the system)

Structure of the thesis

Chapter 1 focuses on the exploration of topologies. First, a short summary of some potential solutions is shown and their weakness are studied. Then, a comparison based on few qualitative criteria is built between several topologies for the converter power stage and a first candidate topology is selected.

In Chapter 2, two versions of the selected topology are presented to meet the two converter specifications revealed in the general introduction. The operating mode of both versions is analyzed in details and some developments to make it more efficient emerge. A first prototype of the converter is built using discrete components to validate the power stage main functionalities.

Chapter 3 is dedicated to the design of an integrated circuit that includes most of the functional blocks required to control the targeted power stage. The objectives of the IC design are presented, the main limitations of the process (HV bulk Si) are discussed and the solution found to overcome them is described. The design and the characteristics of the main blocks included in the IC are discussed at block-level, through some simulation and experimental results. Finally, a summary of the functionalities in the IC design is made.

In Chapter 4, the design of a custom planar transformer suitable for the targeted application is discussed. The approach used for the design is presented and the influence of some design parameters is studied. It allows to identify the main trade-offs guiding the design of this key component and to build several candidate designs to be measured within the DC/DC converter.

Experimental results are presented in Chapter 5. The functionality of both versions of the power stage is validated. The performances of the converters are measured using different transformer designs and for various operating modes. Then, the results are compared to the existing solutions in the literature.

Finally, a general conclusion and some perspectives of this work are presented to conclude on the interest of the design approach and to list some options to improve the proposed solutions.

Chapter 1

Topology exploration

This chapter presents the main challenges regarding the design of a high-voltage low-power isolated DC/DC converter and offers some hints about the solutions suitable to reach the targeted specifications. It offers a quick reminder of the isolated dc/dc converter's main components and characteristics. Then, it presents a rapid overview of the existing solutions in the same voltage-power range. The limits of these solutions appear and the necessity of a topology exploration is demonstrated when analyzing the standard solution for low-power isolated converters. The exploration is based on few qualitative criteria that are used to analyze and compare few different structures. Finally, the topology that seem the most suitable for the High-Voltage Low-Power (HVLP) conversion is selected. It is the solution that has been developed and designed. The objective of the topology exploration presented in this chapter is not to build an optimized design for each different structure studied, but rather to study the intrinsic characteristics of a topology and to estimate its performances a priori based on few qualitative criteria.

1.1 State of the art

A DC/DC converter is a system that converts a DC supply to a different voltage domain. In the targeted application, the converters needs to transform the high input voltage of a DC bus (connected to a high voltage battery for example) into a low voltage to be used directly by a little system, like a small actuator or a sensor.

A converter is composed of many bricks that work together to form the complete system. The power-stage is an important brick, as it is the one that actually operates the conversion, but there are others like control, filtering and protection of the converter. The present work focuses on the power-stage of the DC/DC converter: this is why the other bricks are not discussed in details. Sometimes, an isolation is required between the input and the output of the converter. When using a non-isolated DC/DC converter, the input and the output typically share a common reference. Therefore, if a perturbation hits one side of the converter, it will probably propagate to the other side. The isolation allows to block some of these perturbations and it is often used to protect small systems, usually more fragile. Different types of isolation exist. The most popular type is the galvanic isolation that requires a magnetic device. Since the application targeted in this work requires a galvanic isolation, only the isolated DC/DC converters will be explored in this study.

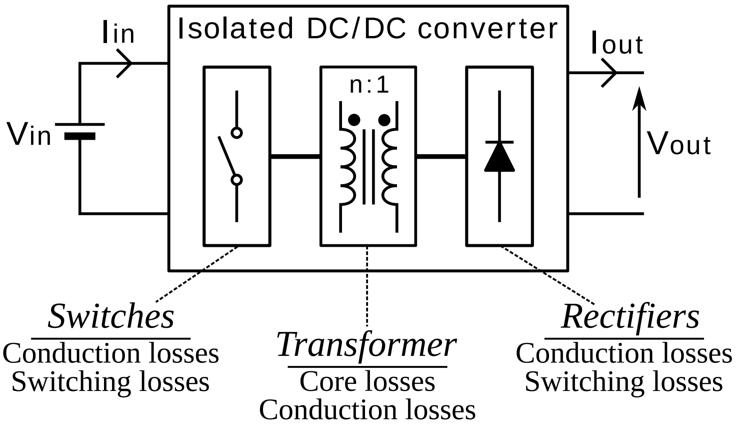


Figure 1.1: Mains elements of an isolated DC/DC converter power-stage

Some components are always present inside isolated DC/DC converters, such as a power switch, a transformer and a rectifier, as shown in Figure 1.1. The way these basic elements are combined inside the DC/DC converter is the topology of the converter. Some conventional topologies exist, with well-known properties, and are used in many DC/DC converters. Defining the topology is one important step in the design process of a converter, as it will decide the number of these basic components inside the converter, their size, their characteristics, etc. So the choice of the topology will largely influence the performances of the converter.

An isolated DC/DC converter is defined by several key characteristics, which define the applications where it can be used or not. These characteristics are common to all the DC/DC converters and are therefore used to compare them. Few of the most important characteristics are presented below to conclude this introduction to the isolated DC/DC converters.

- **Input & output voltages**: The input and output voltages that a converter can connect generally decide the components used inside the converter. For example, the switches and the capacitors used in the power-stage are rated for a maximum voltage, which sets the limit on the voltages the converter can operate with. The output voltage that a converter can provide also depends on the topology used for the power-stage. The topology should be selected such as the convert can produce the output voltage required at the targeted input voltage. Here, the main constraint comes from the high input voltage that will impose an important stress on the components of the converter.

- **Power**: Converters are usually designed for a specific power range, because the power a converter needs to deliver has a large impact on the choice of the components used. Indeed, the thermal constraints on these components will set the limits of the power a converter can handle. However, the application targeted in this work only requires a very low output power, especially when considering the high input voltage value such that the thermal constraints will not be the main concern for the design of the converter.

- **Efficiency and power losses**: Finally, another very important characteristic to describe a DC/DC converter is its efficiency. The efficiency is calculated as the ratio of the power provided by the converter over the power that it consumes to provide it. The efficiency is useful to represent the performances of a DC/DC converter in steady-state mode. It is impacted by the losses generated inside the converter. They are due to many different phenomena and each component inside the converter inevitably produces some losses as shown in Figure 1.1. Conduction losses are due to the current conducted by the devices, while turn-on and turn-off of active and passive devices create switching losses. The transformer also generates core losses due to the magnetic flux that circulate inside its core.

1.1.1 Existing solutions for HVLP converters

As presented in the general introduction of this document, the design of the DC/DC converter with the targeted specifications is challenging. To underline the reasons why the High-Voltage Low-Power (HVLP) conversion at high-efficiency is not simple, it is interesting to look at the existing solutions with characteristics similar to the targeted specifications.

Not many HVLP DC/DC converters with specifications in the range of what is targeted with this application (i.e. few hundreds volts for the input voltage, more or less 12 V for the output voltage and a power up to few watts) can be found in literature or on the market. One reason for this is because typically a high voltage is used to transmit a high power level, hence the rare cases of high-voltage converters with such little power.

Nevertheless, few examples of isolated HVLP converters already exist, like off-line converters, which role is to transform the AC-line voltage into classical low voltage (often +5 or +12V), generally with low output power.

Tables 1.1 and 1.2 gather some of these solutions. Table 1.1 summarizes the important characteristics of the DC/DC converters proposed in literature. Table 1.2 gives some details about converters available on the market or proposed as a reference design. The reason for this distinction is because the information available for a product and a solution from an article are not the same. In addition, the solutions proposed in literature works are often not optimized on all the aspects, in terms of footprint for example.

Table 1.1: Summary of existing solutions in literature

Parameters ▼	[3]	[4]	[5]	[6]	[7]	[8]
Converter type	DC-DC	DC-DC	AC-DC	AC-DC	DC-DC	AC-DC
Input voltage [V]	36-373	75-450	90-265(ac)	185-265(ac)	360-440	1200-1800
Output voltage [V]	5	5	6	12	48	24
Power [W]	1-10	0.25-1.0	1-5	5	5-65	16-60
Efficiency (at Vin)	75% (370V)	83% (400V)	70% (265Vac)	75% (265Vac)	85% (400V)	60% (1200V)
Transformer core & Size [mm*mm]	RM6 20*23	EE16 20*18	EE16 20*18	EE13 14*16	EFD25 25*26	EE35 35*35
Switching freq.	150 kHz	20 kHz	66 kHz	150 kHz	1 MHz	50 kHz
Topology	Actv clp[1] Flyback	Flyback	Flyback + snubber	Flyback + RCD[2] clamp	HB[3]-LLC	ISOP[4] Flyback

[1] Active Clamp; [2] Resistor-Capacitor-Diode; [3] Half-Bridge; [4] Input-Series Output-Parallel

Table 1.2: Summary of existing products and reference designs

Parameters ▼	**[2]**	**[9]**	**[10]**	**[11]**	**[12]**
Converter type	DC-DC	DC-DC	DC-DC	DC-DC	DC-DC
Input voltage [V]	100-1000	110-420	50-600	120-440	400-860
Output voltage [V]	5	12	15	12	16.5
Power [W]	5	4	3	6	8
Efficiency (at Vin)	75% (200V) 65% (1000V)	80% (340V)	80% (300V) 65%(600V)	85% (400V)	68% (600V)
Total size mm	70*48	28*18	59*30	35*31	?
Topology	?	Flyback	Flyback	QR[1] Flyback	Flyback
Frequency	75 kHz	?	110 kHz	25-60 kHz	75 kHz
Manufacturer Year	Cui Inc. 2018	Tamura 2016	Texas Inst. 2013	Infineon 2018	Texas Inst. 2009
Application	Renewable energies	Low stand-by supplies	Automotive	Industrial	Energy Conserving

[1] Quasi-Resonant Flyback

To analyze these existing solutions, several aspects are discussed: the maximum input voltage, the efficiency, the solution's size and the topology used.

Input voltage: Most solutions can support an input voltage up to 400 $\mathrm{V_{DC}}$, but only few of them are capable of operating for an input voltage higher than 600 V. This is because a 400 V input corresponds to the maximum DC voltage reached by the AC-line (240 $\mathrm{V_{AC}}$ in Europe), with +15% additional margin for safety, that set maximum DC voltage around 390 V. Since many of these examples are intended to be used as off-line converters, they are designed to cope with maximum 400 $\mathrm{V_{DC}}$. Another reason is because the technology of the power-switches used in these converters, typically high-voltage Silicon MOSFETs, presents some limitations for the maximum voltage stress supported by the switches. Together with the Flyback topology used in many solutions, this limit of the switch technology will set the maximum input voltage close to 400 $\mathrm{V_{DC}}$.

Efficiency: The majority of DC/DC converters presented in Tables 1.1 and 1.2 do not have performances good enough to meet the targeted specifications. The only solutions presenting a satisfying efficiency are [7] and [4, 11]. But the first is a GaN-based solution, therefore not compatible with the low cost specification, while the two others operate at low switching frequency and thus requires large passive components. Most solutions have an efficiency between 65% and 80%, even though their input voltage is still quite low ($<$ 400 V). For solutions that can support $V_{in} > 600$ V, none of them offer an efficiency higher than 65% when dealing with these voltages. This illustrates the difficulty of converting the high-voltage input into a low-voltage, low-power output with a high efficiency.

Solution size: The efficiency alone is not a good indicator, as it must also be put in line with the size of the solution. The size of the transformer is used as an indicator for the size of the overall solution, as it is usually the bulkiest component of the converter. In [3, 4, 5, 6] the transformer used is often quite small and the associated footprint on the circuit board is in the range of what is targeted for the transformer of the final solution. However, the solutions with high power [7] or high voltage [8] capabilities present a bulkier transformer. For the existing products, [2] is the only one rated for an input voltage up to 1000 V, but its module size is quite important. On the other hand, [9] that supports an input voltage up to 450 V is more compact and in the range of the targeted solution's size.

Topology: One of the main limitations for the maximum input voltage and the efficiency is the topology used for the power-stage, which is the Flyback architecture for the vast majority of the examples. The Flyback architecture is a conventional converter topology for low-power isolated applications, but it presents some serious limits especially at high input voltage.

1.1.2 Limitations of the Flyback topology

The Flyback architecture is very popular because of its simplicity, its robustness and its low cost. It has a very low number of components: only one low-side power switch is required, along with one transformer and a simple diode on the secondary side, as shown in Figure 1.2 where a schematic Flyback stage is presented.

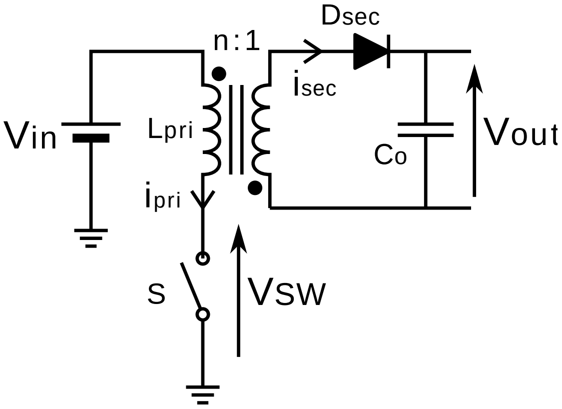


Figure 1.2: Schematic of a simple Flyback power stage

It is used in a very large panel of applications, as it can operate step-down or step-up conversion, thanks to the transformer turns-ratio and to its transfer function. But using this topology to operate a very high step-down might be challenging, because it is not optimized for this. This can still be useful when addressing a large input voltage range, as for [3, 2]. However, in the present application, the input voltage range is reduced, because the voltage variations on the DC bus connected to a battery are rather small and the output voltage is low, so it requires a large step-down operation. Therefore the Flyback main transfer function is not really suitable in this case.

The Flyback waveforms obtained in simulation (using the SIMetrix-SIMPLIS circuit simulation tool) are shown in Figure 1.3. The simulation was achieved using simplified model for the

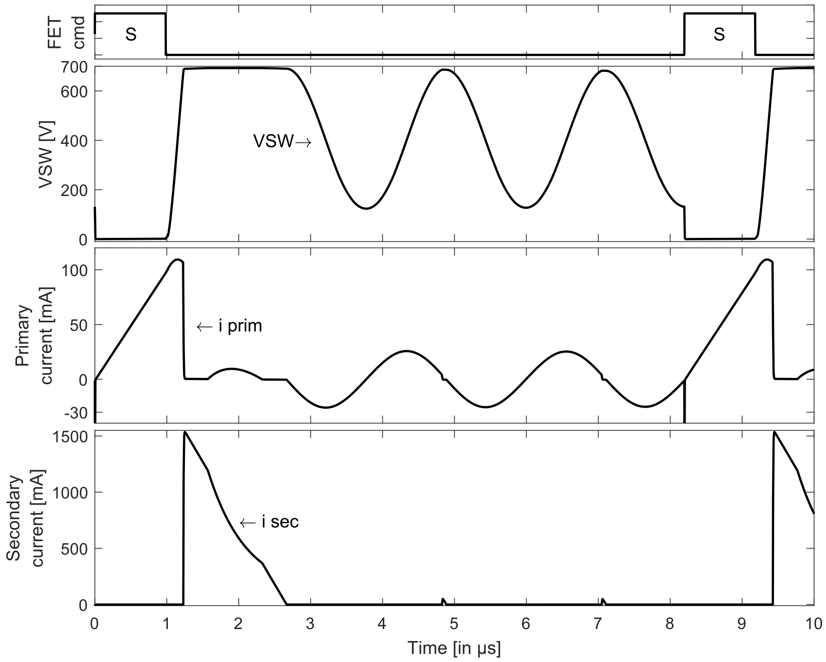


Figure 1.3: Typical simulations waveforms for a Flyback in DCM

transformer and the power switches, with the input voltage equals to 400 V, the output voltage close to 12 V and the output power around 1 W.

The switching period can be divided in three steps. In the first step, the switch S is ON, a positive voltage is applied to the primary and energy is stored inside the transformer. The second step starts when the switch S turns-off. The energy stored inside the transformer is transmitted to the output, through the rectification diode D. Once the secondary current i_{sec} becomes null, the third step starts. In this last step, primary inductance L_{pri} and parasitic capacitors resonate, creating the sinusoidal waveforms observed on the switching node V_{SW} and in the primary current i_{pri}. Note that this last step only appears when the Flyback operates in Discontinuous Current Mode (DCM), which is often the case at low power.

This simple analysis of the Flyback topology and its associated waveforms already highlights several drawbacks of the topology, which will limit the capabilities and the performances of converters based on this architecture.

The first drawback relates to the voltage-stress on the primary switch S. As shown in the waveforms in Figure 1.3, a high voltage stress is applied to the switch when the current flows in the secondary side. The maximum voltage stress on S can be computed as:

$$V_{S_{MAX}} = V_{in} + n \cdot V_{out} \tag{1.1}$$

where n is the transformer turns ratio ($n = N_{pri}/N_{sec}$) as presented in Figure 1.2.

This leads to a voltage stress on switch S that is higher than the input voltage. This is a problem when considering the design of a converter with a high input voltage (up to 1 kV). In the case of the off-line converters presented in Tables 1.1 and 1.2, it leads to choose a MOSFET with breakdown voltage close to 600/650 V when designing a converter with maximum

DC input of 400 V. This means that design for a Flyback with 500 V input voltage would require a switch with probably 800 V capability. For the case where maximum input voltage is 1 kV, this would require a device rated for 1.2 kV or higher. Such high-voltage devices exist, but they are not compatible with the low cost and integration perspectives, as they often require more complex manufacturing technologies, using wide-bandgap semiconductors like SiC.

Another issue of this architecture is the important stress on the transformer. Indeed, the core losses that occur in the magnetic core are particularly impacted by the voltage applied to the transformer. In the Flyback topology, the amplitude of the applied voltage is equal to the input voltage V_{in}, because the switching node is tight to the ground when switch S is ON. Hence the high losses in the magnetic device, especially when the input voltage is as high as 1 kV. Some techniques exist to mitigate these losses, like decreasing the switching frequency. However the loss reduction will only be limited and decreasing too much the switching frequency might require larger filtering components, increasing the solution size. Some applications will also put some limits on the minimum switching frequency of the converter, forbidding to get in the audio band for example (below 20 kHz). For these reasons, the high stress on the transformer in the Flyback stage will lead to high losses, preventing the converter to operate at the targeted efficiency.

Finally, the Flyback-based solutions will also present some limits due to the difficulty to operate in Zero Voltage Switching (ZVS) mode. This operating mode is used to greatly reduce the switching losses on the primary switch. Some alternatives exist to mitigate these losses in a Flyback configuration, as the quasi-resonant mode [11, 13], but it is still difficult to keep this operating mode on a large input voltage range. A more complex Flyback topology as the Active Clamp Flyback (ACF) can be used to enable the ZVS mode [3, 14], but it complicates the power-stage as it requires a second active device loosing the interest of the simplicity of the Flyback architecture.

In the end, this short analysis of the Flyback stage reveals why this topology is probably not a good candidate to design a HVLP converter with strong requirement on cost, size and efficiency.

1.2 Topology exploration

The previous overview of the Flyback topology has revealed some flaws in its characteristics and behavior, especially at high-voltage, making it difficult to build an efficient HVLP converter. The objective of this topology exploration is to rank different structures for the converter, in order to find those interesting in the context of the particular application at hand.

The methodology used is quite simple: using few criteria, each structure was examined to determine its expected performances when used inside a HVLP converter. Finally, the most interesting structures are compared in order to select the most suitable for the specifications and for the targeted integration technology.

The very different nature of the solutions investigated during this exploration prevent the optimization of each singular option. Therefore, to build a fair comparison without having to carefully design the power-stage of each different converter, the analysis is done qualitatively, rather than quantitatively. In other words, the aim of this exploration phase is not to design a complete (with accurate estimation of efficiency, size, etc.), but rather to study the intrinsic characteristics of each topology that transpire when analyzing its general behavior.

1.2.1 Selected criteria

The criteria are selected by translating the numerical specifications of the targeted converter, into key characteristics of the power-stage that should help to reach these objectives. The key characteristics are found analyzing the power stage of a topology and the principal voltage and current waveforms associated.

Voltage stress reduction on power switches

There are two different types of voltage stress that can occur on a power switch. The one that happens during transition periods, that is due to ringing or resonant waveforms, and the reversed-bias voltage that a power device needs to sustain when it is in OFF-state (or reverse biased). For the first type, some methods exist to reduce it, by decreasing the amount of parasitic components or by adding a clamp, as it is usually done in a Flyback converter. However, in the context of the HVLP conversion, the second type of voltage-stress is also a problem as the input voltage can be very high. Thus, the criterion focuses on the last type of voltage stress.

To be able to use the switches built in standard HV bulk silicon technologies, the voltage-stress on each switch has to be reduced with respect to the Flyback topology. Indeed, the power switches from these technologies are often rated for a voltage close to 600 V, while the Flyback topology requires switches with much higher voltage capability, especially for the 800 V range design.

Several techniques can be employed to reduce this voltage stress. Adding transistors in series is a good way of increasing the maximum voltage supported by the configuration, but then comes the problem of balancing the voltage when switches are in OFF-state. It can be done by adding some capacitors around the switches, like in Switched-Capacitor converters, to stabilize the distribution of the voltage.

Reduction of transformer's flux density

The transformer is one key component in many isolated DC/DC converters, because it has a great impact on the size and the performances of the global solution. As quickly shown in Figure 1.1, the transformer generates two types of losses: conduction losses, due to the resistivity of the windings and to currents circulating inside the transformer, and core losses that occur inside of the magnetic material.

The core losses are probably going to be one of the main sources of losses in the case of this HVLP converter, as they tend to increase with the voltage-stress applied to the transformer. To be able to improve the converter performances, it is vital to mitigate these losses. To monitor the core losses reduction, it is possible to look at the flux density, especially the peak value that is often used to compute the core losses. The peak flux density can be evaluated as:

$$B_{peak} = \frac{V \cdot D}{2 \cdot A_e \cdot N \cdot f_{SW}} \tag{1.2}$$

Where V is the amplitude of voltage excitation on the transformer (that is V_{in} in the case of the Flyback), D is the duty-cycle of this voltage excitation (here the voltage waveform is assumed to be rectangular, as it is often in the case of isolated DC/DC converters). A_e is the cross-section of the magnetic core, N the number of turns on the side of the voltage excitation and f_{SW} is the switching frequency of the converter, that defines the period of the voltage excitation. The higher this peak value, the higher core losses to be expected inside the transformer.

This formula gives some interesting leads to reduce the core losses and thus to improve the trade-off between the size and the performances of the transformer. The cross-section and the number of turns will mainly depend on the transformer geometry. Duty-cycle will be determined by the input-output voltages relation of the topology. Therefore, the two main options to achieve lower core losses are to reduce the voltage excitation amplitude or to increase the switching frequency.

Possibility of ZVS mode

The switching losses should also be taken into account during this topology exploration. They are due to charging-discharging of the parasitic capacitance of the components in the converter, that generate some losses when a power device is turned-on. For a power MOSFET, the gate capacitance and the output capacitance can both cause this type of losses. If the gate of the power MOSFET is driven by a local low-voltage supply, then switching losses should be quite low. However, in the case of the output capacitance of the device, these losses can be very high, as shown by the simplified formula:

$$P_{SW_{FET}} \approx \frac{1}{2} \cdot C_{OSS} \cdot V_{DS}^2 \cdot f_{SW} \tag{1.3}$$

Where C_{OSS} is the equivalent output capacitance of the power MOSFET, V_{DS} is the drain-source voltage of the MOSFET just before it is turned-on and f_{SW} is the frequency at which the MOSFET is controlled.

To illustrate why these losses can have a large impact on performances, let's take a numerical example. Considering the case of a MOSFET with $C_{OSS} = 20$ pF, switching at $f_{SW} = 150$ kHz, the losses can be computed as:

- for $V_{DS} = 400$ V, $P_{SW_{FET}} = 240$ mW
- for $V_{DS} = 800$ V, $P_{SW_{FET}} = 960$ mW

The losses are very high, especially considering the low output power, as they would already limit the maximum efficiency of the converter at 80% for the 400 V case or at 51% for 800 V. This simple example shows the importance of decreasing the switching losses of the power switches of the converter in order to maintain the targeted high efficiency.

To mitigate the switching losses, a popular method largely employed is called Zero Voltage Switching (ZVS), which consists in waiting until the drain-source voltage (V_{DS}) of the power device becomes null before to turn it on. This technique allows to almost cancel the switching losses due to the output capacitor.

However, not all the converter topologies can operate in ZVS mode, as it requires some specific conditions, generally linked to the current circulating inside the converter when power devices are off. A topology that cannot operate in ZVS mode will have to decrease greatly its switching frequency, to mitigate these losses. But even doing so, it will anyway present some additional losses with respect to a converter that uses the ZVS technique.

Solution's complexity

The objective of this work is to find a low cost and small size solution for low power. All these parameters tend to reveal that the simpler the selected solution, the better. Increasing the complexity of a solution can help improving its performances (i.e. the efficiency) but it should not contradict with the cost and size perspectives, so a trade-off needs to be found. Different types of complexity need to be considered, as this notion is vague and can have a lot of different meanings.

The number of active and passive devices already gives an idea of the complexity of a power-stage. For the passives, the complexity of some special components (like large capacitor, complex transformer, etc.) can also be taken into account. For the active devices, their number will be particularly important for integration perspectives, given the limited possibility of the targeted technology (HV bulk-Si) to count many isolated devices.

The complexity can also be related to the control of the converter, as some topologies will require more regulation loops than others, in order to control some specific behavior, etc.

So this criterion is used under these different forms, to identify and highlight the complexity inherent to each topology, because this complexity might conflict with the initial objectives of cost, size and efficiency.

1.2.2 Input-Series Converters

The Input-Series Converters (ISC) are a way of assembling several "granular" converters (or "brick") in order to build a complete converter with higher capabilities. One type of arrangement often used to build high voltage converters is the Input-Series Output-Parallel (ISOP) arrangement [15], shown in Figure 1.4. In this arrangement, several converters have their input connected in series, and their output all connected in parallel to the same load. The converter brick has to be an isolated architecture, such that multiple different voltage domains on the primary can be connected to the same output voltage on the secondary.

ISOP arrangement is not the only existing ISC arrangement: much variety can be found in the literature, depending on the application and the specifications of the converter [16]. Another interesting arrangement for the HVLP conversion is the ISSO (Input-Series Single-Output), that is quite similar to the ISOP, but that uses only one transformer, with a single winding for the output and multiple primary windings, as shown in Figure 1.5. This is particularly interesting in the case of HVLP converter, as the "brick" converters can share the input voltage, but they do not need to share the output current like it is often done in ISOP arrangements, since the output power is low in this case. A version with multiple outputs can also be imagined, to create several little auxiliary supplies from a main DC-source [8].

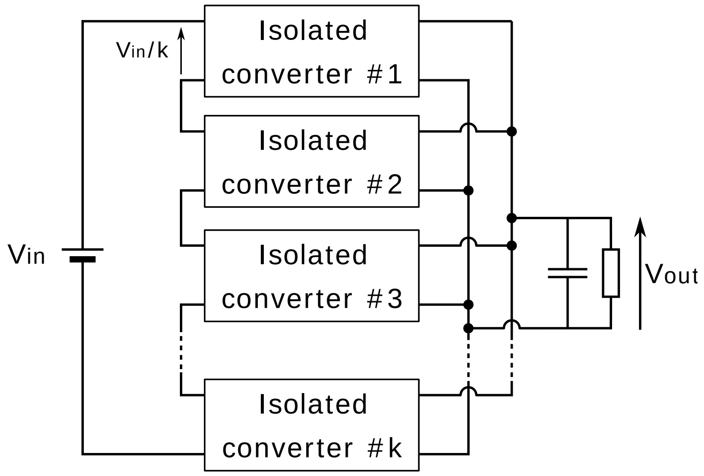


Figure 1.4: Schematic of ISOP converters

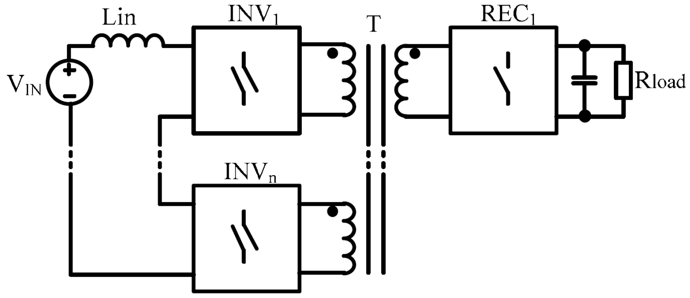


Figure 1.5: Schematic of ISSO converters arrangement as presented in [16]

Advantages of ISC arrangements

The main benefit of the ISC arrangement is that it allows to reduce the voltage at the input of the series converters. This enables a reduction of the voltage-stress on many components of the "brick" converter, as the power switches. Therefore, it becomes possible to build a converter with a high voltage capability using only converters of 400 V capability for example. This advantage is well highlighted in [8], as the ISC arrangement can support input voltage up to 1.8 kV, when each separate module only supports 600 V.

As the maximum voltage on the input of each "brick" converter is reduced, it becomes possible to use simpler topologies, leading to simpler solutions. In [8, 17], the "brick" converter uses a Flyback architecture. However, more complex architectures can be used to improve the converter performances, as a full-bridge in [18] or as a Dual-Active-Bridge (DAB) in [19], but the complexity of the full converter becomes too high.

[18, 19] also prove the possibility of operating in ZVS mode. If the brick converter can operate in this mode, most probably the ISC arrangement will be able to achieve ZVS transitions as well.

Finally, another positive aspect of using ISC arrangements is the modular approach possibility they open. If a converter brick has a well known set of specifications and behavior, it is possible to build a converter with much higher voltage and currents capabilities [20]. This type of approach could be interesting to decrease the manufacturing cost of the "brick" converter, and possibly of the global converter as well.

Limitations of ISC arrangements

In order to effectively reduce the voltage supported by each "brick" converter, the total input voltage of the converter should be well balanced between all the inputs in series. However, due to the imperfections and the small mismatch between the brick converters, it is not the case naturally. All the "brick" converters need to be well controlled or synchronized in order to ensure the correct Input Voltage Sharing (IVS). Several methods have been developed to ensure the IVS: a master/slave solution [21], a common duty-cycle technique [22, 17], etc. But this synchronization required between the brick converters will add some complexity to the global solution.

The main limitations of the ISC arrangements are related to the transformer. Indeed, in order to keep a solution in line with the low cost and small size objectives, ISC arrangements requiring only one transformer must be selected. But the design and the performances of such transformer present some hard points that it is important to highlight.

First, if a single transformer is used to transfer the energy from multiple primary windings to a single secondary winding, the design of this transformer will be of high complexity. Moreover, additional windings are sometimes required to create auxiliary supplies or EMI shields, increasing furthermore the complexity of the magnetic device. These multiple windings around the same transformer core will complicate its design, that is already quite challenging given the converter specifications.

In addition, the multiple windings required around the core will probably impact the performances of the transformer. To highlight this, the formula that gives the peak flux density reached inside the core (Equation 1.2) can be used. Taking the case of an ISC arrangement with k converters, for which a correct IVS is assumed, the voltage at the input of each converter is $1/k^{th}$ of the total input voltage. Therefore, the voltage excitation on the transformer is probably also divided by k. However, the winding window of the transformer is limited, and in the case of an HVLP converter, a high number of turns around the core is required to reduce the core losses. If N_p is the maximum number of primary turns it is possible to achieve around the transformer core, since there are k windings, one for each brick converter, the available space for each of these windings is also divided by k, and each winding can therefore only count N_p/k as maximum number of turns. In Equation 1.2, if both voltage excitation V and number of turns N are divided by k, the value of the peak density B_{peak} does not change, and core losses are not reduced.

For these reasons, the transformer design for the ISC arrangements is a complex matter, and this type of solution will probably not enable a significant reduction in core losses vital to improve the converter efficiency at high voltage.

1.2.3 Switched-Capacitor stages

Switched-Capacitor (SC) converters have received an increased attention in the past years, as a possible approach towards fully integrated DC/DC converters. They take benefit from the DC-voltage blocking capability of capacitors to easily and efficiently operate conversions with a fixed ratio.

The SC converter stage can take many different shapes, depending on the targeted conversion ratio and other parameters as the number of passive/active components required, etc. Figures 1.6 and 1.7 show two examples of step-down SC stages, with the same conversion ratio (3:1). Even though their circuit is quite different, their operating principle is similar: the power-stage alternates between two positions, that allow to keep a constant and balanced voltage on the different capacitors and to propose a reduce voltage at the output.

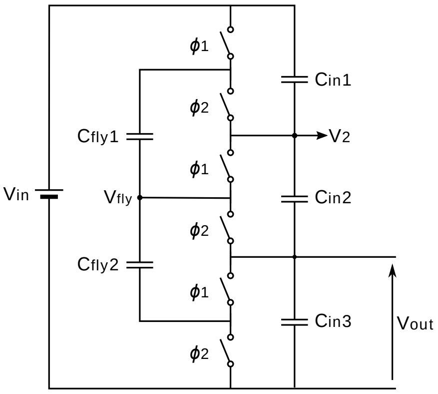


Figure 1.6: Schematic of 3:1 ladder SC stage

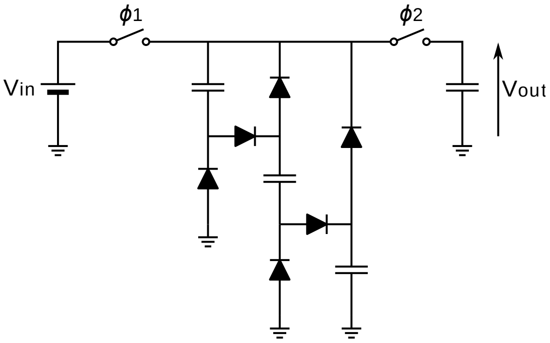


Figure 1.7: Schematic of 3:1 serie-parallel association SC stage

One of the reasons of their popularity is the high power-density that this type of converters can reach. This comes from the power-density of the capacitors themselves, that is much higher than for standard magnetic devices. But it also comes from the possibility to integrate the capacitors required on the same die as the active devices, leading to fully integrated converters and thus to very small solutions. This integration is however not possible for high voltage circuit, as these fully integrated examples are generally intended for maximum voltages in the order of few tens of volts or limited to very low output power.

However, some examples of SC circuits in high-voltage applications can also be found. In [23, 24], one or two SC stage(s) are used to convert a 380 V input voltage into a 12 V output with low-power (< 10 W). In [25], a SC stage is used to convert the 230 V ac-voltage to 3.3 V with very low power (few mW), but with a very limited efficiency. [26] presents an SC stage with a variable ratio, to extend the supported input voltage range, that goes from 25 V to 200 V. In the examples [24, 26], the SC circuit is used as a first stage, which role is to adapt the input voltage of the converter to the input voltage of the regulation stage. This type of combination presents some very interesting characteristics as it allows to take advantage of SC stages density and to release some stress on the design of the regulation stage, usually based on standard inductance-based circuits. In the context of this work, isolation is required, therefore the regulation stage would also be the isolation stage, as the SC circuit does not provide any isolation.

Advantages of SC stages

As shown with the last few examples, the SC stage in a HVLP converter can reduce the voltage at the input of the regulation/isolation stage. Therefore, it can effectively reduce the stress on the components of this stage, i.e on the power switches and the transformer. With a reduced voltage, this stage would be able to work at high efficiency and at high switching frequency, making it possible to get smaller solution for this stage, like in [24, 26].

Moreover, the voltage-stress on the devices of the SC stage can also be reduced. The reduction depends on the type of the SC circuit, for example a n:1 ladder-type SC will divide the voltage-stress on switches and capacitors by n. This can help improving the efficiency and decrease the size of the SC stage as well, as the integration possibilities are more important for lower voltages. However, in the context of this work, the voltage that the SC stage needs to support is very high (500 V or 1000 V), which still limits the possibilities because integrating many 100 V floating devices remains challenging in a standard Si HV-BCD process.

Limitations of SC stages

The absence of an inductive element in SC stages is what allow them to reach very high power density. However, this absence also has a negative impact, as it cancels any type of soft-switching, including the ZVS mode, thus generating some switching losses [27]. The absence of ZVS will force the SC stage to operate at low-frequency and to use switches with low output capacitance, as GaN FETs in [23, 26], in order to mitigate the switching losses (Equation 1.3).

The low switching frequency will furthermore limit the integration possibilities for the capacitors. With lower frequency, the value of the SC stage capacitors will have to increase, in order to keep constant DC voltages across these elements. And it is still difficult nowadays to integrate capacitors with a high value that can support high voltage as well, even more in a low-cost perspective.

Finally, the high number of devices required for the SC stage can also deteriorate the interest for this type of circuits. For a simple 2:1 stage, four switches and three capacitors are already required. The high number of switches is a problem for the integration perspectives. Not to mention the second stage needed to isolate and regulate the output, that also requires one or several power switches to operate. Note that the comment about the integration is quite dependent on the technology used, some other type of solutions might be possible using a different process (based on SOI for example) or on a different approach [28].

PCB demonstrator

To illustrate the previous study of the SC stage, a PCB prototype is built using discrete components. The chosen SC stage is a 3:1 ladder as shown in Figure 1.6. A second stage is cascaded to isolate and create the targeted output voltage. The topology for the second stage is the Asymmetrical Half-Bridge Flyback (AHBF), that is an isolated version of a buck stage. The PCB demonstrator is shown in Figure 1.8. Only the performances of the SC stage are discussed for now because the second stage is not optimized.

The performances of the SC stage are measured for an input voltage between 300 V and 500 V, for a load between 100 kΩ and 150 kΩ, with the switching frequency varying from 10 kHz to 50 kHz. The MOSFET reference is the IRF710 from Vishay, rated for 400 V. The capacitors are standard 1 µF ceramic capacitors rated for 250 V.

The waveforms measured for $V_{in} = 300$ V are shown in Figure 1.9. The results in Table 1.3 show the impact of both the switching frequency and the input voltage on the performances of the SC stage.

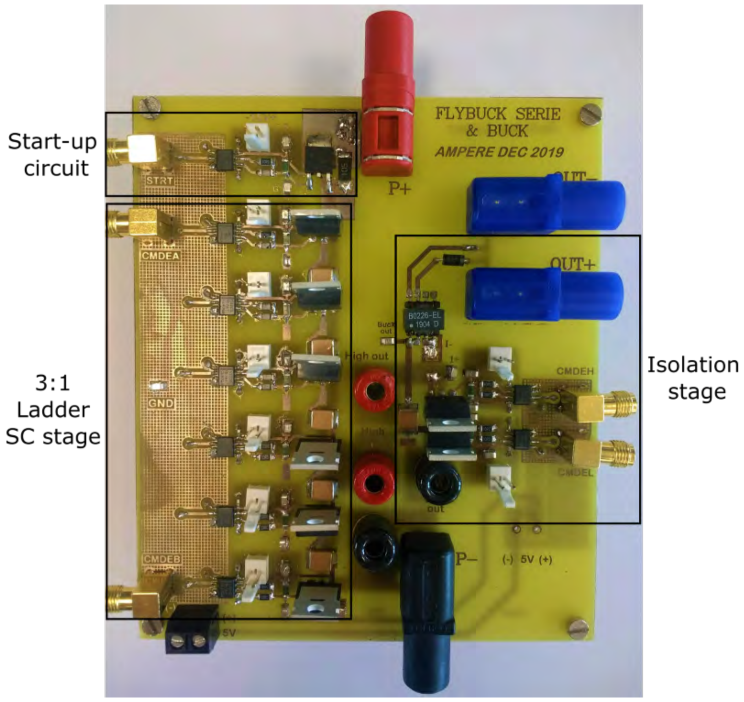
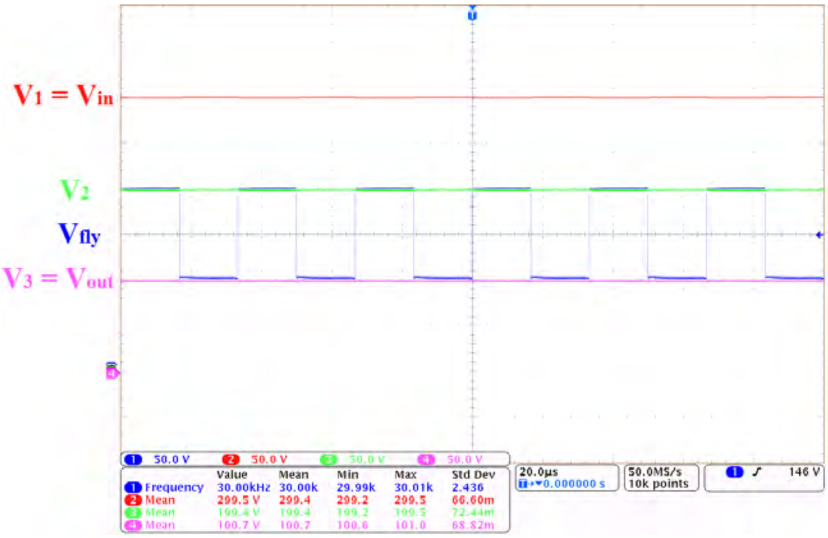


Figure 1.8: PCB demonstrator 3:1 SC stage + AHBF stage



	Value	Mean	Min	Max	Std Dev
① Frequency	30.00kHz	30.00k	29.99k	30.01k	2.436
② Mean	299.5 V	299.4	299.2	299.5	66.60m
③ Mean	199.4 V	199.4	199.2	199.5	72.44m
④ Mean	100.7 V	100.7	100.6	101.0	68.82m

Figure 1.9: Measured waveforms on the 3:1 SC stage demonstrator

The waveforms correspond to the voltages measured at different points of the capacitive ladder formed by the input series capacitors (C_{in1}, C_{in2}, C_{in3} in Figure 1.6). They show that the voltage across each capacitor is very similar, because the voltage on the top of the ladder V_1 is V_{in}, the voltage just below V_2 is $2V_{in}/3$ and the one below $V_3 = V_{out}$ is $V_{in}/3$. The voltage V_{fly} is measured at the node between the two flying capacitors (C_{fly1}, C_{fly2} in Figure 1.6) and it can be seen it alternates between two different voltage levels ($2V_{in}/3$ and $V_{in}/3$) to balance the input series capacitors. This way, the voltage on the output remains close to the expected $V_{in}/3$ value, even when some current is drawn by the output.

The results in Table 1.3 confirm that the output voltage is close to its ideal value $V_{in}/3$ over the input voltage range. The higher the switching frequency, the closer the output voltage is to the ideal value, because it enables a better balancing between the capacitor in series. Globally, these results confirm that the switched-capacitor stage operates correctly the input voltage division (3:1) without any regulation.

Table 1.3: Measurement results of the 3:1 ladder-SC stage

V_{in} [V]	f_{SW} [kHz]	V_{out} [V]	P_{in} [W]	P_{out} [W]	ΔP_{loss} [mW]	η (%)
300	50	99.5	1.15	0.985	165	85.7
400	10	132.2	1.16	1.08	80	93.3
	30	132.9	1.29	1.09	200	84.4
	50	133.1	1.42	1.09	325	77.0
500	50	166.3	2.17	1.71	460	78.9

For a given input voltage, the impact of the frequency is clearly visible looking at the total losses inside the SC stage (ΔP_{loss}). When frequency increases, the losses increase and since the output power is constant, it is not due to increased conduction losses. Therefore, the loss increase observed is probably due to the switching losses of the MOSFETs that operate in hard-switching mode. Note that the MOSFETs used for these tests are not optimized for this utilization, a reference with lower output capacitor but larger on-resistance would have given better performances.

The influence of the input voltage on the losses can also be noticed. The losses increase observed when the input voltage increases cannot be entirely explain by the conduction losses: going from 300 V to 400 V, the losses almost double (+97%) while the output power rise of only 11%. It is once again due to the switching losses occurring at the MOSFETs turn-on that grow with the square of the input voltage (Equation 1.3).

The results from this primary demonstrator illustrate well the pros and cons associated to the SC stage. With a simple stage with no regulation, the SC circuit is able to operate the expected division of the input voltage and to reduce the voltage at the input of the second stage of the converter, as well as the voltage-stress on the components of the first stage. However, the losses measured inside the SC stage show the importance of operating in ZVS mode, especially when devices with large output capacitance are used. These results also highlight the impact of a high input voltage on the converter performances and emphasize the challenge to design HVLP converters with high-efficiency.

1.2.4 Hybrid topologies: Multi-Level Flying-Capacitor converter

The hybrid topologies propose to mix different approaches and to combine them in a single stage, leading to compact solutions with increased capabilities. The hybrid stages combining Switched-Capacitor circuits and classical inductor-based converters (Buck, Boost, etc.) have been studied and used in different forms, depending on the specifications [29, 30, 31, 32, 33, 34, 35]. Some example of high-voltage low-power can be found [36] but without isolation. In particular, the Multi-Level Flying-Capacitor (ML-FC or FC-ML) topology is very popular and used in many different applications.

The ML-FC topology was first proposed by Meynard [37]. Its name comes from the possibility offered to create multiple voltage levels at the switching node of an inverter. But the ML-FC topology can also be used inside DC/DC converters, to realize different operations depending on the structure it is combined with: the ML-FC buck topology is widely used [37, 38, 39] but other varieties can be found in literature (a DAB in [40], a non-isolated bidirectional topology in [41], etc.).

In ML-FC converters, the flying capacitors allow to reduce the voltage stress on the switches and on the transformer. An example of multi-level flying-capacitor buck with n-level is presented in Figure 1.10. It is composed of $n-1$ pairs of complementary switches, $n-2$ flying capacitors and one inductance (i.e. a transformer in its isolated version).

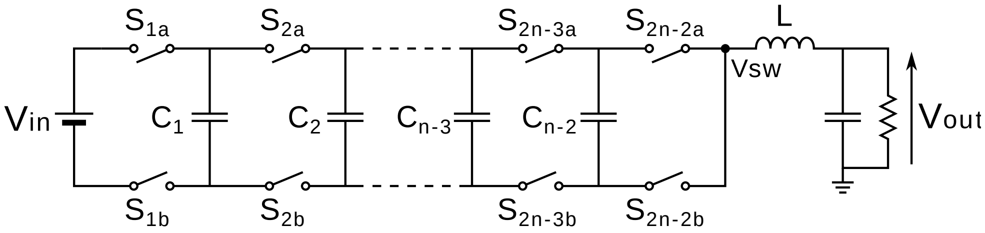


Figure 1.10: Schematic of n-Level Flying-Capacitor buck

Advantages of ML-FC converters

In steady-state, the flying capacitors are charged to a fixed portion of the input voltage, which enables a reduction in the voltage stress on all the switches. For a n-level flying-capacitor converter, the switch stress is $V_{in}/(n-1)$. Note that the version with only two levels does not include a flying capacitor and it looks like a classical half-bridge with the stress on the switches equals to V_{in}.

The DC-voltage across the flying capacitors also decreases the stress on the transformer. Using the proper driving scheme for the power switches, the amplitude of the voltage applied to the middle node (V_{SW} in Figure 1.10) of the ML-FC is also divided by $n-1$. This is something interesting about this topology, because if the voltage amplitude across the inductance of a buck is decreased, the current ripple is reduced and the inductor can be smaller. In the case of an isolated converter, the flying-capacitors will lower the amplitude of the voltage excitation on the transformer. So the use of the ML-FC topology can reduce the core losses.

The ML-FC stages including an inductive element (like the ML-FC buck) can achieve ZVS operations, using the positive and negative current peaks in the inductor to operate soft-switching mode. This is only possible if the power switches used are bi-directional in current (e.g. using MOSFETs instead of diodes).

Limitations of ML-FC converters

The main issue concerning the ML-FC converter is related to the flying capacitor voltage. [37] showed that the voltage stability is assured when the duty-cycles of the high-side power switches are equals, for a constant current flowing from the middle node. But this hypothesis is not always valid, and some analyses [42, 43] suggested that voltage across the flying capacitors of the ML-FC might be not equal to the ideal value, because of the imperfections of the input voltage source, of the mismatch in the driving of power switches etc. Some control solutions where proposed to solve this issue in [43, 44, 45] which however tend to make the final solution more complex.

Some additional issues are known with the ML-FC as the charging of the flying capacitors at start-up, that might require some special attention to prevent too high voltage stress on the switches, if ramping up of the input voltage is too high. The control of the ML-FC converter might also be delicate if the duty-cycle is too close to certain limits (50% duty-cycle for 3L-FC, 33.3% for the 4L-FC, etc.), even if some solutions exist to mitigate these problems [46].

1.2.5 Comparison and selection of a candidate topology

A comparison is built between the different topologies introduced previously with the objective of determining the best candidate to be integrated and optimized, to create the targeted HVLP converter.

To build a fair comparison between the different structures, all the solutions are compared for an equivalent ”input voltage reduction” of $V_{in}/2$. The meaning of this reduction depends on the structure: for the Input-Series Converters, it means there are two converters connected in series. For the converters with a Switched-Capacitor stage, a 2:1 SC stage is used. Finally, for the Multi-Level Flying-Capacitor converter, the input voltage reduction indicates the number of levels: a 3-level is required to obtained a input voltage reduction of $V_{in}/2$. The selected input voltage reduction is low, to keep solutions with a reasonable complexity, especially in terms of number of components.

For the ISC arrangement, the topologies selected for the ”brick” converter are the Flyback, because it is very simple, and the AHBF (Asymmetrical Half-Bridge FLyback, isolated version of a buck), because of its step-down capabilities and its relative simplicity as well. The same architectures are used for the second stage of the converters based on a SC first stage. Table 1.4 summarizes the main results.

Table 1.4: Important properties of the topologies selected for the comparison

Topologies ▶	2-ISC		2:1 Ladder SC stage		3-Level FC
Parameters ▼	Flyback	AHBF	Flyback	AHBF	AHBF
Input voltage reduction	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$	$V_{in}/2$
Switch stress	$V_{in}/2 + n.V_o$	$V_{in}/2$	$V_{in}/2 + n.V_o$	$V_{in}/2$	$V_{in}/2$
Transformer stress reduction	$--$	$-$	$+$	$++$	$+$
ZVS possibility?	No	Yes	1^{st} stg: No 2^{nd} stg: No	1^{st} stg: No 2^{nd} stg: Yes	Yes
No. switches	2	4	4+1	4+2	4
No. HV capacitors	2	4	3 + 0	3 + 1	2
Additional complexity	- complex transformer - synchronize ”bricks”				C_{FLY} charging and stability

Comparison between the different structures

All the structures allow to reduce the voltage stress on the switches quite efficiently, although the topologies using a Flyback architecture present a stress that is higher than solutions based on the AHBF topology.

The reduction of the stress on the transformer varies significantly from one topology to another. The scale used is qualitative ("$--$" symbol means there is almost no reduction while "++" indicates a good reduction), since the analysis does not allow to compute any accurate impact on the size or the efficiency of the transformer. Note that the analysis made of the Flyback topology lead to lower expectations for the transformer performances with this topology when comparing to the performances obtained with the AHBF topology that reduces the voltage stress on the transformer with a capacitor in series.

Solutions based on a SC circuit seem quite interesting, because the input voltage of the second stage is decreased significantly. On the other hand, ISC do not really offer a reduction of the voltage stress on the transformer, which make this type of solution less appealing. Finally, studies of the ML-FC converter have shown a large reduction of the stress on the inductor for non-isolated structures. The same reduction should be observed for isolated structure, as the ML-FC converters allow to decrease the voltage stress on the transformer and to increase its operating frequency.

The majority of the selected topologies offer the possibility of operating in ZVS mode, although it is harder for the Flyback-based solutions to operate in this mode, some quasi-resonant method can be used to improve this aspect. Only the SC stage itself does not present any soft-switching possibility and the results from the PCB demonstrator showed it can severely affect the performances (even though some solutions could be found to reduce their impact, like switches with smaller output capacitance, etc.).

In the end, the complexity of each solution should also be taken into account. The "complexity" criterion introduced can be interpreted in different ways and the different solutions proposed for the HVLP converter are all complex from a certain point of view. The objective of this comparison is also to understand which type of complexity will probably be more difficult to deal with and which type of complexity will be more acceptable.

The Input-Series Converter are interesting as they open the possibility to use simple topologies, with a low number of components and to copy it a few times to create the full converter. Therefore, when using the Flyback topology for the "brick" converter, the solution built is quite simple. The main complexity comes from the transformer design, but that can be limited if a low number of "brick" converters is used. Some complexity is added also with the control of the global converter, to ensure the correct IVS between the "brick" converters.

On the other hand, the SC-stage complexity is rather related to the high number of component they require. Several discrete capacitors and several power switches are required to built the first stage. In addition, the SC solution requires a second stage to isolate and regulate the output voltage, which further increase the component count. Note once again that this analysis is quite dependent on the technology considered for the integration. A different process with different constraints might open some possibilities to integrate more easily the switching devices required, leading to a more attractive solution, but the cost constraint limits the options.

To finish, the ML-FC converters complexity seem to be mostly due to the flying capacitor stability. This type of complexity seems to be less a problem because the integration offers some possibilities to deal with this issue inside the controller, where complexity will cost less space than additional external components. The number of components required for the ML-FC/AHBF hybrid is comparable to the one obtained for the AHBF ISC solution.

Selection of the topology candidate for HVLP converters

In the end, after comparing the solutions offered by these different topologies, it does not appear that one solution is clearly better than all the others. However, it can be noticed that the Multi-Level Flying-Capacitor solution is offering a fair trade-off between the complexity of the solution and the expected performances of the converter regarding the initial objectives. It is therefore selected to be the first candidate for IC integration and to build an optimized version of the converter.

For the hybrid-architecture of the ML-FC, the AHBF topology appears as a good option to keep the power-stage as simple and compact as possible, given the low number of components required on the primary and on the secondary side of the transformer. The ML-FC/AHBF hybrid is studied more in details in Chapter 2.

1.3 Conclusion

This chapter offered a quick review of the important characteristics of isolated DC/DC converters and showed the existing potential solutions in literature or on the market for a HVLP converter.

The limitations of these solutions were highlighted and a short analysis of the Flyback architecture, used by the majority of these examples, led to conclude that the Flyback topology is not suitable for the targeted application.

A topology exploration, based on few qualitative criteria was performed. It proposed a brief study of few interesting options as Input-Series Converters arrangement, converters with a Switched-Capacitor stage and hybrid Multi-Level Flying-Capacitor converters and gave an analysis of their intrinsic advantages and limitations.

A fair comparison between these different structures was carried out to evaluate the level of complexity of each solution with respect to the others. This comparison revealed the Multi-Level Flying-Capacitor converters appears as an interesting trade-off between the complexity and expected performances in a first step.

Chapter 2

Topology analysis

This chapter starts with the description of the approach used to address the two different specifications presented in the General Introduction of the thesis. Then it proposes an analysis of the main current and voltage waveforms, for the 2-level and the 3-level versions of the ML-FC-AHBF topology. A qualitative analysis of some aspects of the topology behavior completes the waveform analysis. The high level of similarity between the 2L-AHBF and the 3L-FC-AHBF is also highlighted. Finally, a practical demonstrator of the 3L-FC-AHBF is built to validate the topology analysis. The primary performance measurements give some indications on the future leads for the design of the power stage and the transformer.

2.1 General approach

Two versions of the topology for two targeted designs

At the end of Chapter 1, the ML-FC topology was selected to design the targeted converter. However, as discussed in the converter specifications presented in the General Introduction, there are two targeted designs: one centered around a 400 V input voltage and another one with a 800 V nominal input voltage.

In the case of the 800 V design, the 3-Level Flying-Capacitor (3L-FC) is selected to enable the necessary voltage stress reduction as discussed in Chapter 1. For the 400 V design, the voltage-stress on the power switches is limited, because the input voltage is smaller, so a 2-level version of the topology is used. The distribution of the targeted designs between the two versions of the ML-FC topology will also simplify the design phase, as a lot of similarities will appear between the design of a 2-level for 400 V and the design of a 3-level FC for 800 V.

Motivations and methodology for the topology analysis

The objective of this chapter is to offer a better understanding of the operating principle of the ML-FC AHBF topologies, in order to highlight the trade-offs that will be considered during the design phase. The two versions of the ML-FC AHBF topology are shown in Figure 2.1 and in Figure 2.2.

In addition, the analysis will allow to highlight the particularity of the low-power mode, that changes some of important aspects of the topology operating principles. Finally, analyzing the

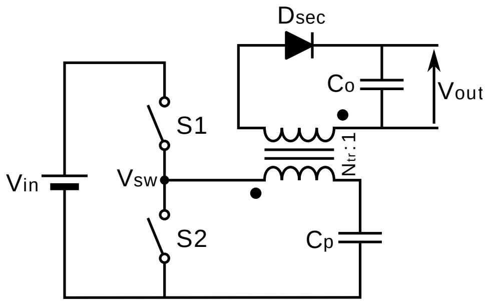


Figure 2.1: Schematic of 2-Level AHBF

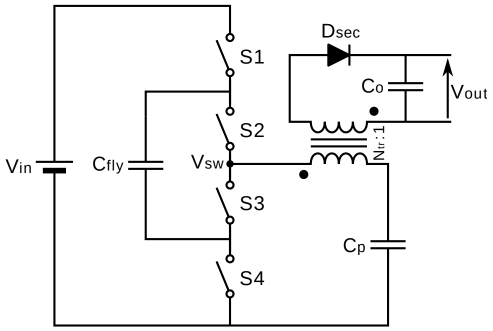


Figure 2.2: Schematic of 3-Level Flying-Capacitor AHBF

two versions of the ML-FC topology (2L-AHBF and 3L-FC-AHBF) will allow to emphasize some of the similarities that exist between them.

The analysis proposed in this chapter focuses on the behavior of the topology in steady-state. Simplifying hypotheses are made as the aim of the study is not to accurately describe the behavior of the power stage analytically but rather to identify which parameters will have an influence on the power stage performances.

First, the model and the hypotheses used for the analysis are summarized. Then, the converter's main current and voltage waveforms are described over a complete switching period. Their expressions during each state that compose a period are given. Finally, the main outcomes of the analysis are discussed, with emphasis on the ZVS mechanism, the converter's main transfer function and the flying capacitor voltage balance for the 3L-FC version. The 2L-AHBF topology is analyzed in a first step, since it can be seen as a simplified version of the 3L-FC. Then, the full 3L-FC-AHBF topology is studied and the results of a first PCB prototypes are presented.

2.2 Analysis of the 2-level AHBF topology

The Asymmetrical Half-Bridge Flyback topology (AHBF, referred in this work as the 2L-AHBF) is an architecture for isolated DC/DC converters, often used to operate step-down operations for limited power range (usually below 100 W). Its name comes from how it is built and controlled. Two switches in a half-bridge configuration interface a Flyback-mode transformer. The Half-Bridge capacitive divider, usually connected in parallel of the switches, is replaced in this structure by a single capacitor placed in series with the transformer's primary. Moreover, unlike the classical half-bridge, the switches in the 2L-AHBF are controlled with different duty-cycle values, hence the ”Asymmetrical” adjective.

Another way of presenting this topology is to see it as the isolated version of the synchronous Buck converter, with a transformer replacing the inductance. For this reason, it is also sometimes referred as the ”Fly-Buck” topology [47].

Main operating principle

With the 2L-AHBF topology, the energy is stored inside the transformer during one phase and transferred to the output during another phase. Since the secondary winding is in opposition with the primary winding, the output voltage is decided by the voltage of the primary capacitor C_p and the transformer turns ratio N_{tr} (defined as the ratio of primary and secondary number of turns $N_{tr} = N_{pri}/N_{sec}$). Like in a Buck converter, the voltage across the primary capacitor C_p is determined by the product of the input voltage and the duty-cycle of the high-side switch.

Several analyses of the AHBF topology can already be found in the literature [48, 49, 50, 51, 52, 53, ?]. However, these analyses were done with a slightly different model and for a larger output power than the targeted value for the present converter (typ. 50 W vs 1 W). The model used in the present analysis and the consideration of the low-power mode for the converter will impact some aspects of the topology behavior, in particular during the soft-switching transitions.

2.2.1 Analysis of a switching period in steady-state

The circuit diagram in Figure 2.3 shows the model used for the transformer and the power switches. The main waveforms obtained with this model, using the SIMetrix SIMPLIS circuit simulation tool, are presented in Figure 2.4.

The model used for the power switches consists in an ideal switch with a reverse diode and a capacitor connected in parallel. The switch on-resistance and the voltage drop of the body-diode are both neglected. A constant value is supposed for the output capacitor (C_{oss}), although it is quite inaccurate because the output capacitor value drastically changes with the drain-source voltage, especially for high-voltage Si MOSFETs.

The transformer's model includes the leakage inductance (L_r), the magnetizing inductance (L_{mag}), the primary-secondary parasitic capacitor (C_{ps}). C_{ps} is the only transformer's parasitic capacitor considered in a first step, although others should be added to build a more accurate model (more details are given in chapter 4). C_{ps} is connected in parallel of the transformer's primary (instead of being connected between the primary and the secondary side) to simplify the analysis (the hypothesis can be made as the secondary voltage is small with respect to the primary voltage because of the large transformer turns ratio). All these elements surround an ideal transformer that connects the primary and the secondary, with a transformer turns ratio of N_{tr}. The resistance of the windings is not considered in the first analysis.

Finally, some additional hypotheses are made to simplify the analysis:

- Primary capacitance (C_p) value is big enough to consider that its voltage is constant over a switching period. V_{Cp} is supposed to be equal to the average output voltage referred to the primary side.
- Primary-secondary parasitic capacitor (C_{ps}) value is constant and entirely referred to the primary side.
- The value of the leakage inductance is small in comparison with the value of the magnetizing inductance.

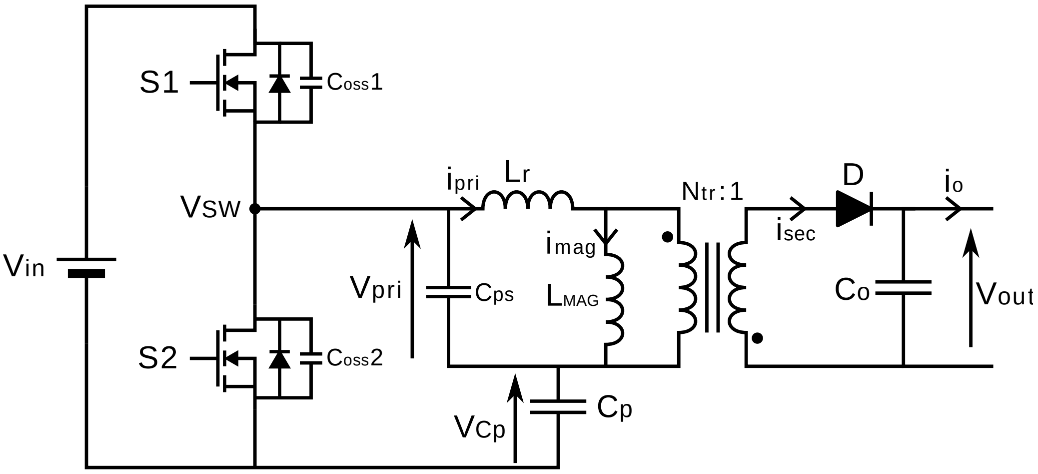


Figure 2.3: Model considered for the 2L-AHBF

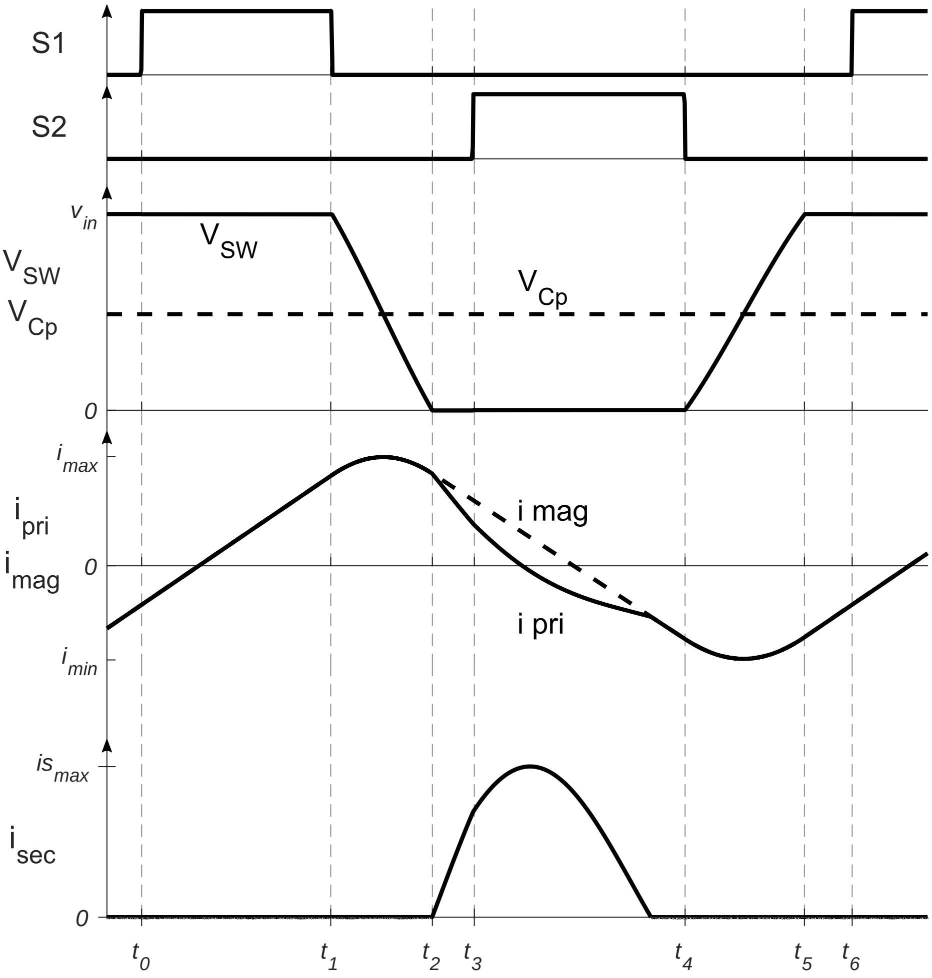


Figure 2.4: 2L-AHBF - Main waveforms in simulation

State 1 (t_0 - t_1)

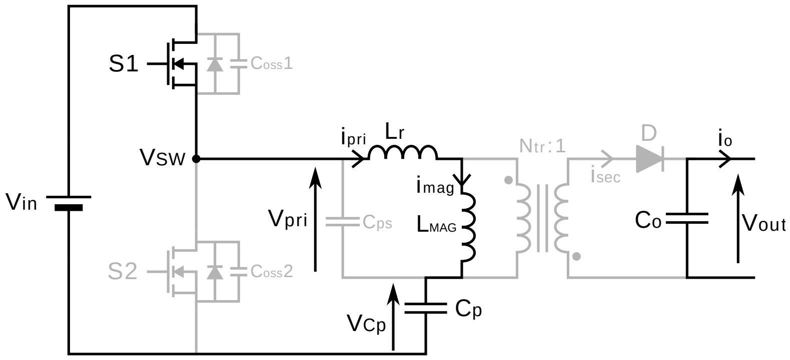


Figure 2.5: 2L AHBF - State 1 (t_0 - t_1)

$S1$ turns-on at t_0. Since $S1$ is ON, it connects the middle node (V_{SW}) directly to the input voltage (V_{in}) such that the voltage across the primary side of the transformer is:

$$V_{pri}(t) = V_{in} - V_{Cp} \tag{2.1}$$

The primary voltage is positive because V_{Cp} is a fraction of V_{in}. So the current flowing inside the primary side is increasing according to:

$$\frac{di_{pri}(t)}{dt} = \frac{di_{mag}(t)}{dt} = \frac{V_{pri}(t)}{L_{mag} + L_r} = \frac{V_{in} - V_{Cp}}{L_{mag} + L_r} \tag{2.2}$$

Since the current variation is linear, it is possible to write its expression during the state 1 as:

$$i_{pri}(t) = i_{mag}(t) = i_{pri}(t_0) + \frac{V_{in} - V_{Cp}}{L_{mag} + L_r} \cdot (t - t_0) \tag{2.3}$$

Note that the magnetizing current is the only current that flows during state 1, that ends when $S1$ turns-off.

State 2 (t_1 - t_2)

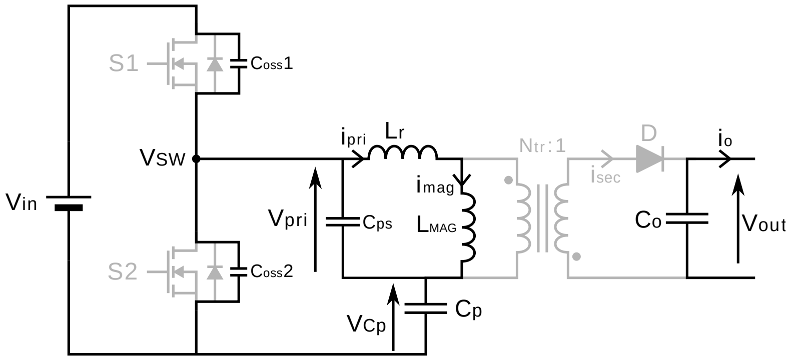


Figure 2.6: 2L AHBF - State 2 (t_1 - t_2)

State 2 starts when $S1$ turns-off at t_1. Due to the current in the primary inductance, the switching node V_{SW} moves from V_{in} to almost 0 V. The variations of the primary voltage and of the switching node voltage can be written as:

$$\frac{dV_{pri}}{dt}(t) = \frac{dV_{SW}}{dt}(t) = -\frac{i_{pri}(t)}{C_{SW}} \tag{2.4}$$

Where C_{SW} is the sum of all the parasitic capacitors connected to the switching node V_{SW}. From an AC-perspective, the output capacitors of both power switches and the primary-secondary parasitic capacitor of the transformer are all connected in parallel between the switching node and ground. Therefore, the total parasitic capacitor connected to middle can be computed as the sum of these three capacitors:

$$C_{SW} = C_{oss1} + C_{oss2} + C_{ps} \tag{2.5}$$

At the same time, the primary current also changes, because the voltage on the transformer's primary varies:

$$\frac{di_{pri}}{dt}(t) = \frac{di_{mag}}{dt}(t) = \frac{V_{SW}(t) - V_{Cp}}{L_{mag} + L_r} \tag{2.6}$$

Combining (2.4) and (2.6) it is possible to solve the differential equation, to find the formula for primary current and voltage:

$$i_{pri}(t) = i_{mag}(t) = i_{pri}(t_1) \cdot cos(\omega_0(t - t_1)) + \frac{V_{in} - V_{Cp}}{Z_0} \cdot sin(\omega_0(t - t_1)) \tag{2.7}$$

$$V_{pri}(t) = -\ i_{pri}(t_1) \cdot Z_0 \cdot sin(\omega_0(t - t_1)) + (V_{in} - V_{Cp}) \cdot cos(\omega_0(t - t_1)) \tag{2.8}$$

with $$\omega_0 = \frac{1}{\sqrt{C_{SW} \cdot (L_{mag} + L_r)}} \tag{2.9}$$ and $$Z_0 = \sqrt{\frac{L_{mag} + L_r}{C_{SW}}} \tag{2.10}$$

Equations (2.7) and (2.8) show the impact of parasitic capacitors connected to node V_{SW} and of the value of the primary inductance. Together they set the resonant frequency described by (2.9). If the dead-time duration is much shorter than the resonant period, then the primary voltage rises almost linearly, which leads to the quadratic behavior of the primary current shown in Figure 2.4.

State 2 ends when the middle switching node (V_{SW}) reaches ground, i.e. when the parasitic capacitors connected to this node are fully charged/discharged.

State 3 (t_2 - t_3)

The body-diode of $S2$ starts to conduct current at the beginning of state-3.

It forces the switching node to ground and, as a consequence, a negative voltage is applied across the transformer primary side:

$$V_{pri}(t) = -V_{Cp} \tag{2.11}$$

The magnetizing current therefore decreases:

$$\frac{di_{mag}(t)}{dt} = \frac{V_{mag}(t)}{L_{mag}} \tag{2.12}$$

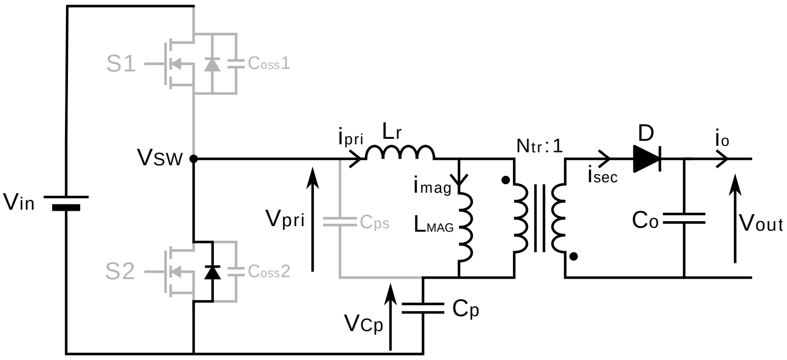


Figure 2.7: 2L AHBF - State 3 (t_2 - t_3)

Due to the small variations of the output voltage, a linear decreasing of the magnetizing current is assumed, which leads to:

$$i_{mag}(t) \approx i_{mag}(t_2) - \frac{N_{tr} \cdot (V_D + \overline{V_{out}})}{L_{mag}} \tag{2.13}$$

where $\overline{V_{out}}$ is the DC voltage across the output, V_D is the voltage drop on the secondary diode D (assumed to be constant) and N_{tr} is the transformer turns ratio defined as $N_{tr} = N_{pri}/N_{sec}$.

At the same time, due to the opposite connection of the transformer's primary and secondary windings, the positive voltage on secondary side allows the forward bias of the secondary diode D. The current can therefore flow on the secondary side and its dynamic will depend on the value of the primary leakage inductance.

During this phase, since the voltage drop due to parasitic resistances and body-diode is neglected on the primary side, it is possible to express the voltage across the leakage inductance as:

$$V_{Lr}(t) = -V_{mag}(t) - V_{Cp} = N_{tr} \cdot (V_{out}(t) + V_D) - V_{Cp} \tag{2.14}$$

In this last expression, the variations of the output voltage are taken into account. In addition, it is possible to express the relation between primary, magnetizing and secondary currents as:

$$\frac{di_{pri}(t)}{dt} = \frac{V_{Lr}(t)}{L_r} = \frac{di_{mag}(t)}{dt} - \frac{di_{sec}(t)}{dt} \cdot \frac{1}{N_{tr}} \tag{2.15}$$

On the secondary side, the output current i_o is supposed to be constant. Therefore the output voltage variations depend on the secondary current:

$$\frac{dV_{out}(t)}{dt} = \frac{i_{sec}(t) - i_o}{C_o} \tag{2.16}$$

Combining (2.14), (2.15) and (2.16) the differential equation can be found. To solve it, it is possible to assume that the voltage across capacitor V_{Cp} is equal to the average output voltage referred to the primary side (the expression is discussed in the section dedicated to the converter's main transfer function).

The solution of the differential equation gives the following formula for the secondary current:

$$i_{sec}(t) = i_o \cdot (1 - cos(\omega_1(t - t_2))) + \frac{N_{tr}}{Z_1} \cdot \frac{\Delta V_{out}}{2} \cdot sin(\omega_1(t - t_2)) \tag{2.17}$$

with $$\omega_1 = \frac{N_{tr}}{\sqrt{C_o \cdot L_r}} \tag{2.18}$$ and $$Z_1 = \sqrt{\frac{L_r}{C_o}} \tag{2.19}$$

and where ΔV_{out} is the peak-to-peak ripple of the output voltage, expressed as:

$$\frac{\Delta V_{out}}{2} = V_{Cp} - N_{tr} \cdot (V_{out}(t_2) + V_D) \tag{2.20}$$

The expression for the secondary current (2.17) seems to correspond with the general shape of the waveform obtained in simulation in Figure 2.4. It also shows the impact of the leakage inductance on the dynamic of this current: a larger leakage inductance value will result in a slower rise of the secondary current. But the formula is not very accurate, as the voltage across the leakage inductance will be also impacted by the voltage drops due to parasitic resistances, body-diodes etc. which are neglected here.

The current in the primary side of the transformer can finally expressed as:

$$i_{pri}(t) = i_{mag}(t) - \frac{i_{sec}(t)}{N_{tr}} \tag{2.21}$$

State 3 finishes when $S2$ turns-on.

State 4 t_3 **-** t_4)

State 4 starts when the switch $S2$ turns-on, which allows the current to flow through its channel rather than through its body-diode.

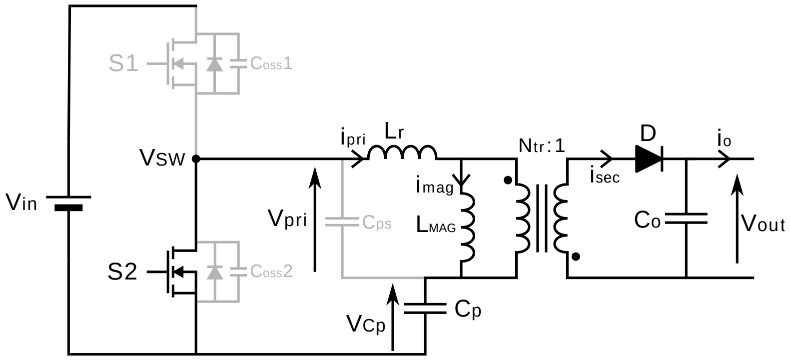


Figure 2.8: 2L AHBF - State 4 (t_3 - t_4)

The voltage and current waveforms during this phase are very similar to those in state 3, as the switching node V_{SW} is still connected to ground. Equations for the primary, the secondary and the magnetizing currents don't change and neither do the voltages, because of the hypothesis that neglect the voltage drops due to parasitic resistances and body-diodes. Hence no differences appear in these expressions between state 3 and 4.

However, the impact of the voltage drop across $S2$ can be noticed in the dynamic of the secondary current. A slight change of slope can be observed for i_{sec} in Figure 2.4. It confirms that the resistances should be taken into account in order to get an accurate expression for the secondary current. But it is not the objective of this analysis, as its goal is rather to explicit qualitatively which element of the converter will impact its behavior.

Depending on the value of the leakage inductor, the secondary current might become null during state 4, if enough energy was transmitted to the output, as it is the case in waveforms shown in Figure 2.4. Once the secondary current cancels, it does not become negative, as the secondary diode forbids it. The primary current is therefore only due to the magnetizing current, but voltages do not change before the end of state 4, that ends when the switch $S2$ turns-off.

State 5 (t_4 - t_5)

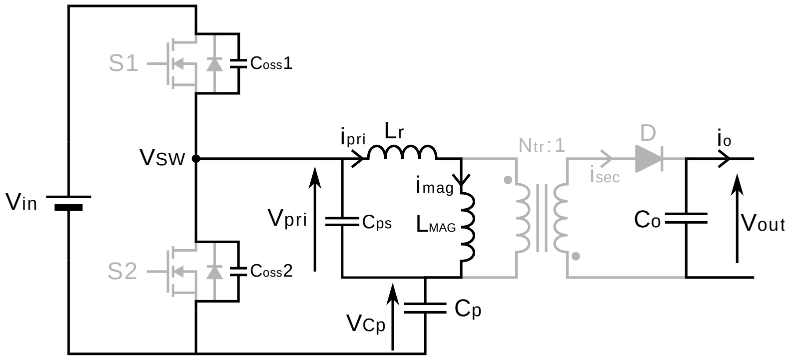


Figure 2.9: 2L AHBF - State 5 (t_4 - t_5)

When $S2$ turns-off at t_4, the switching node V_{SW} starts to move from 0 V to V_{in} due to the negative primary current.

The possible remaining secondary current drops to zero, but its impact on the ZVS transition is not taken into account. Because this current is very small, due to the low output power and its impact on ZVS transition is even less important as it is divided by the transformer turns ratio N_{tr}, that is much larger than 1.

The principle of this ZVS transition is actually very similar to the one that occurs during state 2. It is still the magnetizing current that moves the switching node, charging/discharging the same parasitic capacitors. However, the switching node V_{SW} moves up from the ground level to V_{in} during this transition. But the variations of the voltage on the primary side stay the same as in state 2:

$$\frac{dV_{pri}}{dt}(t) = \frac{dV_{SW}}{dt}(t) = -\frac{i_{pri}(t)}{C_{SW}} \tag{2.22}$$

The variations of the voltage across the transformer's primary also induce changes in the current flowing through the primary side:

$$\frac{di_{pri}}{dt}(t) = \frac{di_{mag}}{dt}(t) = \frac{V_{SW}(t) - V_{Cp}}{L_{mag} + L_r} \tag{2.23}$$

Equations (2.22) and (2.23) are the same as in state 2, solving the differential equations therefore leads to similar expressions for the primary voltage and currents:

$$i_{pri}(t) = i_{mag}(t) = i_{pri}(t_4) \cdot cos(\omega_0(t - t_4)) - \frac{V_{Cp}}{Z_0} \cdot sin(\omega_0(t - t_4)) \tag{2.24}$$

$$V_{pri}(t) = -\ i_{pri}(t_4) \cdot Z_0 \cdot sin(\omega_0(t - t_4)) - V_{Cp} \cdot cos(\omega_0(t - t_4)) \tag{2.25}$$

with $$\omega_0 = \frac{1}{\sqrt{C_{SW} \cdot (L_{mag} + L_r)}} \tag{2.26}$$ and $$Z_0 = \sqrt{\frac{L_{mag} + L_r}{C_{SW}}} \tag{2.27}$$

The impedance Z_0 and the resonant frequency are also the same, as they are set by the same components. The only differences will come from the initial conditions.

The initial voltage for V_{SW} is 0 V, instead of V_{in}. The initial current flowing through the primary of the transformer when state 5 begins ($i_{pri}(t_4)$) is also different from the one at the beginning of state 2 ($i_{pri}(t_1)$): it is negative and its absolute value is also different. It is due to the non-zero average value of the magnetizing current. This last point will make the state 5 last a little longer than state 2. This is discussed more in details in the outcomes of this analysis in section 2.2.2.

State 5 ends at the end of the voltage transition, i.e. when the switching node reaches V_{in}.

State 6 (t_5 - t_6)

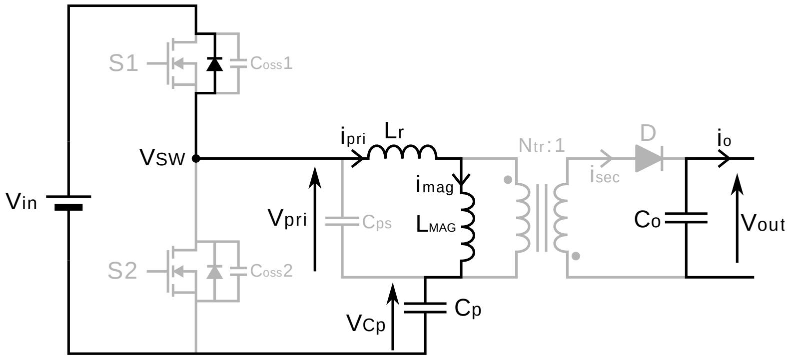


Figure 2.10: 2L AHBF - State 6 (t_5 - t_6)

As the switching node reaches V_{in}, the body-diode of $S1$ starts to conduct some current. The power stage is now in a situation close to the one in stage 1, with V_{SW} forced to V_{in} and a negative primary current:

$$V_{pri}(t) = V_{in} - V_{Cp} \tag{2.28}$$

Since the voltage across the primary side of the transformer is just as the one in state 1, the current in the primary side can be expressed as:

$$i_{pri}(t) = i_{mag}(t) = i_{pri}(t_5) + \frac{V_{in} - V_{Cp}}{L_{mag} + L_r} \cdot (t - t_5) \tag{2.29}$$

State 6 ends when the switch $S1$ turns-on, and a new switching period starts.

2.2.2 Important characteristics of the 2L-AHBF in low-power mode

From the analysis of the main current and voltage waveforms of the 2L-AHBF, it is possible to determine some important characteristics for this topology, that will be useful for the design phase.

Influence of the leakage inductance

Contrary to the analyses made for a larger power [49, **?**], the impact of the leakage inductance L_r on the ZVS transitions is reduced. That is because in low-power mode, the output current is null or small during these transitions and the quantity of energy stored inside the leakage inductor is therefore very small. Thus the role of the leakage inductance during the ZVS transitions is limited.

The leakage inductor has an influence on the secondary current dynamics (State 3 and 4). It limits the maximum energy that can be transmitted to the secondary side during a given amount of time. However, since the output power is quite low, the amount of current that needs to flow through the secondary side will be small. Therefore no strong constraint shall guide the design of this parameter, since its value should not have a large influence on the behavior of the power stage (supposing that it remains relatively small compared to the magnetizing inductance).

ZVS mechanism and dead-times' duration

As highlighted in chapter 1 during the topology exploration, the possibility for a converter to operate in ZVS mode is essential in order to reduce the switching losses. The 2L-AHBF has the advantage to offer the possibility for both power switches $S1$ and $S2$ to operate in ZVS mode.

The ZVS mechanism is described in the previous analysis: the primary current is used to move the switching node V_{SW} to discharge the output capacitor of a switch before it is turned-on. The same principle was already described in some previous analysis of the AHBF topology: [51, 53, 52] use the same mechanism to operate in ZVS mode at light-load. However, the parasitic capacitors taken into account for the study of the ZVS transitions are not the same, as none of these works study the impact of the transformer primary-secondary capacitor C_{ps} for example.

The ZVS mechanism is therefore based on the primary current that is used to charge/discharge all the parasitic capacitors connected to the switching node V_{SW}. It means that a minimum quantity of the primary current must be flowing through the magnetizing inductor in order to ensure the ZVS transition is completed. The quantity of current available for the ZVS transitions will depends on the magnetizing inductor that limits the amplitude of the magnetizing current. Hence, for a given input voltage and frequency, a maximum value for the magnetizing inductance exists that allows to operate in ZVS mode. This will be used in Chapter 4 to design the value of the primary inductance.

A consequence of using a large value for the magnetizing inductance is that the ZVS transitions will become very long. Because the higher the inductance, the smaller the primary current ripple, so the smaller the current available during the ZVS transitions. Therefore if the parasitic capacitors connected to the middle node (C_{SW}) don't change, it will translate in slow transitions of the switching node (state 2 and 5), as shown in waveforms in Figure 2.4. The dead-time required between a switch turn-off and the complementary switch turn-on must be very long to ensure ZVS mode.

When analyzing the time required for the ZVS transition of the high-side MOSFET (i.e. state 5) and of the low-side MOSFET (i.e. state 2), it can be noticed that one is shorter than the other. This imbalance is due to the quantity of current available, that is not the same for the two transitions. The magnetizing current average value is slightly higher than zero (the value of the offset is: $(i_{mag})_{AVG} = I_{out}/N_{tr}$), so the maximum primary current value is larger than the minimum primary current value in absolute. Therefore, the low-side transition (state 2) will be faster than the high-side transition (state 5).

Evolution of the primary current with the switching frequency

Another parameter that has a large impact of the primary current's ripple is the switching frequency of the power stage. To understand how the frequency changes the quantity of primary current, the ZVS transitions must be considered. If the quantity of current available during the ZVS transitions becomes small, the transitions will take a long time to be completed. In steady-state, there are two factors that limit the duration of a ZVS transition: the minimum on-time of the power MOSFETs and the switching period.

The power switches present a minimum on-time due to the constraints of the IC that include the power switches (its design is discussed in Chapter 3). In order to properly drive and supply the floating circuits, the low-side and the high-side power MOSFETs should stay in ON-state for a minimum amount of time (that is considered to be independent of the switching frequency). Note that the minimum on-time of the high-side switch can be different from the one of the low-side.

Figure 2.11 shows the switches' control signal and the voltage of the middle switching node (V_{SW}) with the division of the switching period into four different steps.

The switching frequency sets the duration of the switching period, and if the switches have a minimum on-time, then there is a maximum time allocated for the ZVS transitions. The higher the switching frequency, the shorter these transitions will have to be. The currents required to operate the ZVS transitions can be expressed as:

$$\overline{i_{ZVS\ HS}} = \frac{C_{SW} \cdot V_{in}}{dt_{HS}} \qquad (2.30) \qquad \text{and} \qquad \overline{i_{ZVS\ LS}} = \frac{C_{SW} \cdot V_{in}}{dt_{LS}} \qquad (2.31)$$

Where $\overline{i_{ZVS\ HS}}$ and $\overline{i_{ZVS\ LS}}$ are the average currents for the ZVS transitions of the high-side and the low-side switches, respectively. C_{SW} is the parasitic capacitance connected to middle node during the ZVS transitions. dt_{HS} and dt_{LS} are the duration of the ZVS transitions for the high-side and the low-side MOSFETs, respectively.

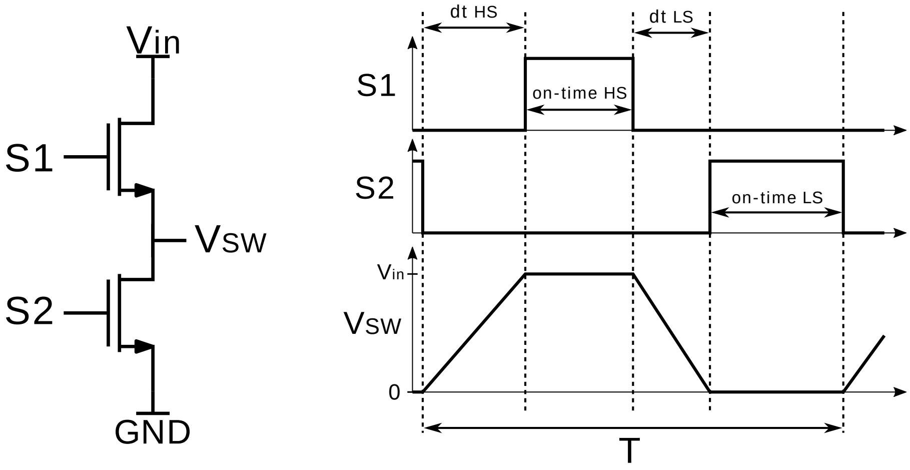


Figure 2.11: Division of the period in different steps

These two expressions show the impact of the duration of the ZVS transitions on the quantity of current: the shorter the transitions, the larger the current to operate them has to be. The positive and the negative peak currents on the primary side are reached during the ZVS transitions. A larger current during these phases will thus lead to a larger RMS primary current.

So it is possible to conclude that increasing the switching frequency will either have a negative impact on the duration of the ZVS transitions or require more current to operate these transitions in a shorter time, thus leading to extra conduction losses.

In addition, Equations (2.30) and (2.31) also reveal the importance of limiting the total capacitor connected to the switching node to reduce the current required during the ZVS transitions. The larger the capacitor, the more current will be required to operate the ZVS transition with a similar duration.

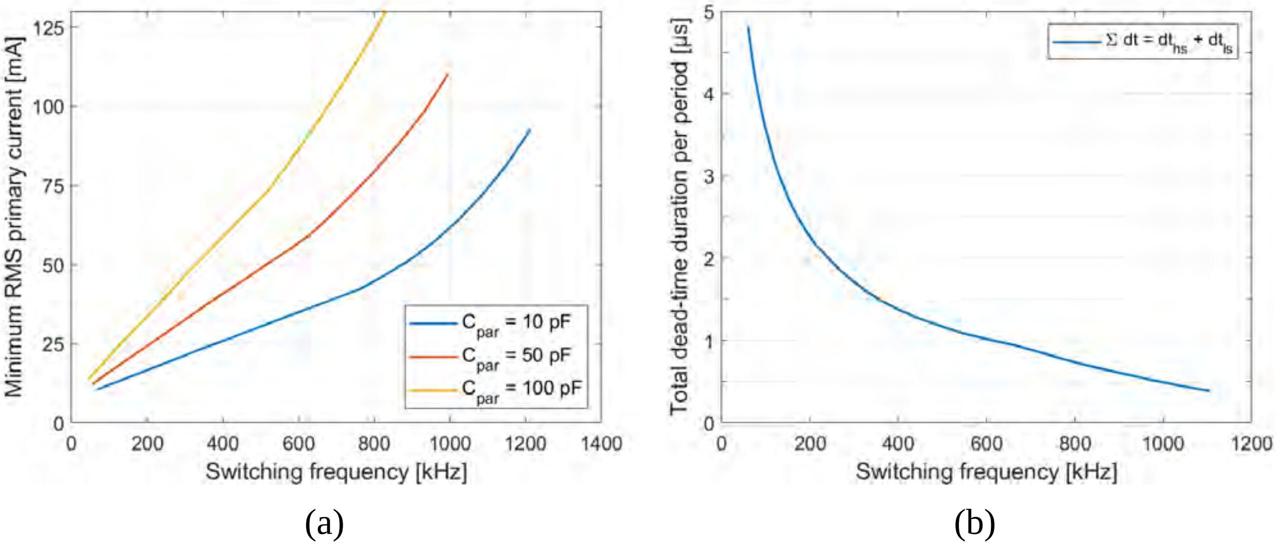


Figure 2.12: Evolution with the switching frequency of (a) Minimum RMS primary current to keep ZVS mode for different parasitic capacitances - (b) Total dead-time per period

The results shown in Figure 2.12 are obtained using a numerical model for the power stage that is further described in Chapter 4. In particular, they illustrate the impact of the switching frequency on the minimum RMS primary current required to operate in ZVS mode, in Figure 2.12 (a) reveals that the minimum current increases drastically with the frequency. It also highlights the importance of limiting the quantity of parasitic capacitance connected to the switching node to reduce the primary current.

In addition, Figure 2.12 (b) confirms the duration of the dead-time (i.e. the ZVS transitions) represent a large portion of the period: at 500 kHz, the sum of the dead-times accounts for 60% of the switching period's.

Note that the values of the current and of the dead-times depends on many design parameters, like the power switches minimum on-time. However, these results already reveal the important trends regarding the design of these parameters.

Converter main transfer function

Another important characteristic of the 2L-AHBF is the main transfer function of the converter, i.e. the relation that connects the converter's input and output voltages.

A first step is to compute the volt-second balance across the transformer's primary side to find a relation between the input voltage and the primary capacitor's voltage V_{Cp}. In steady-state, the volt-second across the transformer's primary side over a switching period is zero i.e.:

$$\int_0^T V_{pri}(t)dt = 0 \tag{2.32}$$

If a linear variation is considered for the primary voltage during the ZVS transitions (states 2 and 5), then the volt-second balance leads to the following expression:

$$V_{Cp} = V_{in} * \frac{1}{T} \cdot ((t_1 - t_0) + (t_6 - t_5) + \frac{(t_2 - t_1) + (t_5 - t_4)}{2}) \tag{2.33}$$

Where T is the switching period such that $t_6 = t_0 + T$.

Neglecting state 6, it is possible to simplify the expression considering that the switch $S1$ turns-on immediately at the end of the ZVS transition. The expression becomes:

$$V_{Cp} = V_{in} \cdot \frac{1}{T} \cdot (t_{ON_{S1}} + \frac{(t_2 - t_1) + (t_5 - t_4)}{2}) = V_{in} \cdot (D + \frac{dt_{HS} + dt_{LS}}{2T}) \tag{2.34}$$

Where $t_{ON_{S1}}$ is the on-time of switch $S1$, D is the duty-cycle of high-side switch $S1$, dt_{HS} and dt_{LS} are the dead-times for the ZVS transitions associated to the high-side and low-side power switches, respectively. The terms for the high-side switch on-time and the dead-time durations can be regrouped to compute the "effective" duty-cycle D_{eff}, leading to the following expression:

$$V_{Cp} = V_{in} \cdot D_{eff} \tag{2.35}$$

On the other hand, considering the states when power is transmitted to the output, it is possible to find a relation between the primary capacitor voltage and the output voltage:

$$V_{out} = \frac{V_{Cp}}{N_{tr}} \cdot \frac{L_{mag}}{L_{mag} + L_r} - V_D \tag{2.36}$$

Where N_{tr} is the transformer turns ratio as indicated in Figure 2.3, and V_D is the voltage drop due to the secondary diode, that is supposed constant.

Finally, using (2.34) and (2.36) is it possible to write the formula that draw the link between the input and output voltage of the 2L-AHBF converter using the "real" or the "effective" duty-cycle:

$$V_{out} = \frac{V_{in}}{N_{tr}} \cdot \frac{L_{mag}}{L_{mag} + L_r} \cdot (D + \frac{dt_{HS} + dt_{LS}}{2T}) - V_D \tag{2.37}$$

$$V_{out} = \frac{V_{in}}{N_{tr}} \cdot \frac{L_{mag}}{L_{mag} + L_r} \cdot D_{eff} - V_D \tag{2.38}$$

(2.37) is interesting because it shows how the output voltage can be controlled if the input voltage varies, by changing the duty-cycle of $S1$. Moreover, it highlights the impact of the dead-times duration (i.e. of ZVS transitions) on the output voltage, which is particularly important for a HVLP converter, as the dead-time duration will be longer than in classical converters. The impact of the dead-times can be explained considering the fact that the primary current will continue to charge/discharge the primary capacitor C_p even during the ZVS transitions, which will therefore impact the voltage across the primary capacitor and the relation between the input and output voltages.

2.3 Analysis of the 3L-FC-AHBF topology

The 3-Level Flying-Capacitor Asymmetrical Half-Bridge Flyback (3L-FC-AHBF or 3L-FC-FlyBuck) is the topology selected to operate the 800 V low-power conversion. It becomes mandatory to use the 3-level version of the topology for an input voltage higher than 600 V, when using power switches built with a standard HV bulk Si process.

The 3L-FC-AHBF topology can be constructed from the 2L-AHBF topology by simply adding a flying capacitor and two power switches to the primary bridge. The rest of the circuit is identical, as the transformer primary side is still connected between the middle switching node (V_{SW2}) and the primary capacitor (C_p). The secondary is also identical to the 2L-AHBF, with the secondary side of the transformer connected in opposition with the primary side and a diode rectifier.

The main advantages of the 3L-FC-AHBF (reduced voltage-stress on switches, reduced voltage excitation of the transformer...) comes from the DC blocking capability of the flying capacitor C_{fly}.

The primary bridge of the 3L-FC-AHBF topology is composed of two pairs of complementary switches (S1/S4 and S2/S3). The two pairs are controlled with a 180° phase shift, with the same duty-cycle value for the high-side switches. Like for the 2L-AHBF converter topology, the output voltage can be controlled by changing the duty-cycle of high-side switches $S1$ and $S2$.

Although several examples of the non-isolated version of this topology can be found in the literature ([37, 54, 55] show a 3L-FC Buck and [39, 41] a 4L-FC buck), there are less example of the isolated version of this topology used inside a DC/DC converter.

2.3.1 Circuit analysis in steady-state

Model considered, hypothesis and switching waveforms

The circuit diagram used to analyze the behavior of the 3L-FC-AHBF in steady-state is shown in Figure 2.13. The models used for the main components (i.e. power switches and transformer) are the same as for the 2L-AHBF analysis. The waveforms obtained in simulation, using the SIMetrix SIMPLIS tool, are shown in Figure 2.14.

The hypotheses made for this analysis are close to the ones made for the 2L-AHBF:

- Primary capacitance (C_p) value is big enough to consider that its voltage is constant over a switching period. $V_{C}p$ is supposed to be equal to the average output voltage referred to the primary side.
- The voltage across the flying capacitor V_{fly} is supposed constant and equal to its ideal value, that is $V_{in}/2$.
- The state in which the body-diode of a power switch conducts the current, just before the switch is actually turned-on, is neglected because the topology behavior is the same as when the switch is ON (as shown in the previous analysis).
- Primary-secondary parasitic capacitor (C_{ps}) value is constant and entirely referred to the primary side.
- The value of the leakage inductance is small in comparison with the value of the magnetizing inductance.

Quick analysis over a switching period

The transformer's voltage and current waveforms shown in Figure 2.14 are very similar to those obtained with the 2L-AHBF. That is because the expressions for these voltages and currents also have a lot in common with the 2-level version of the topology. Therefore, the complete set of equations for the voltages and currents in the power-stage is not repeated, but it is detailed in the Appendix A. Only a quick analysis of the main states that compose a switching period of the 3L-FC-AHBF topology is proposed here, to present the most important operating principles and highlight the particularity of the 3-level version of the topology.

State 1 (t_0 - t_1)

State 1 starts when the power switch $S1$ (or its body-diode) turns-on. The switch $S3$ is also in ON-state during state 1. The voltage across the transformer primary side is

$$V_{pri}(t) = V_{in} - V_{fly} - V_{Cp} = \frac{V_{in}}{2} - V_{Cp} \tag{2.39}$$

The primary current therefore increases linearly during this state, due to the constant positive voltage across the primary of the transformer (as $V_{Cp} < V_{in}/2$). The current flowing through the flying capacitor is the same as the primary current.

State 1 ends when switch $S1$ turns-off.

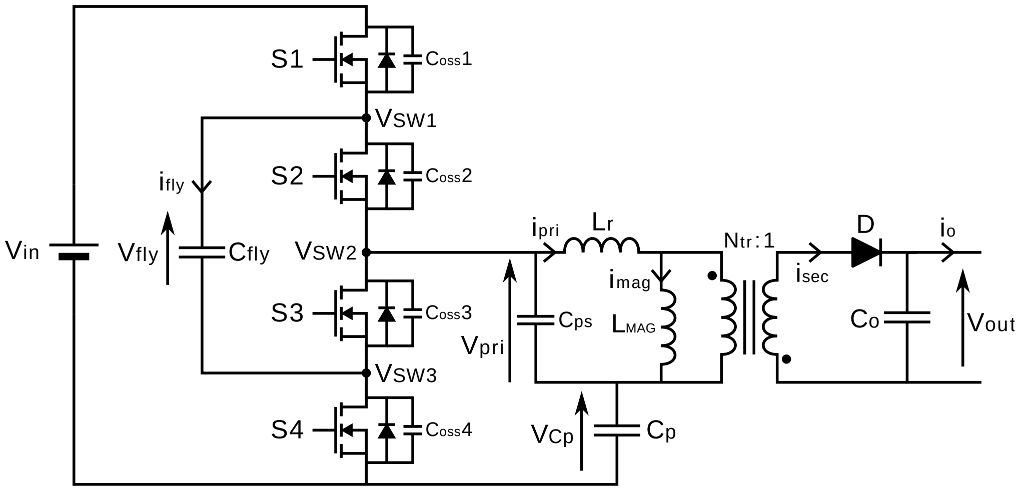


Figure 2.13: Model considered for the 3L-LC-AHBF

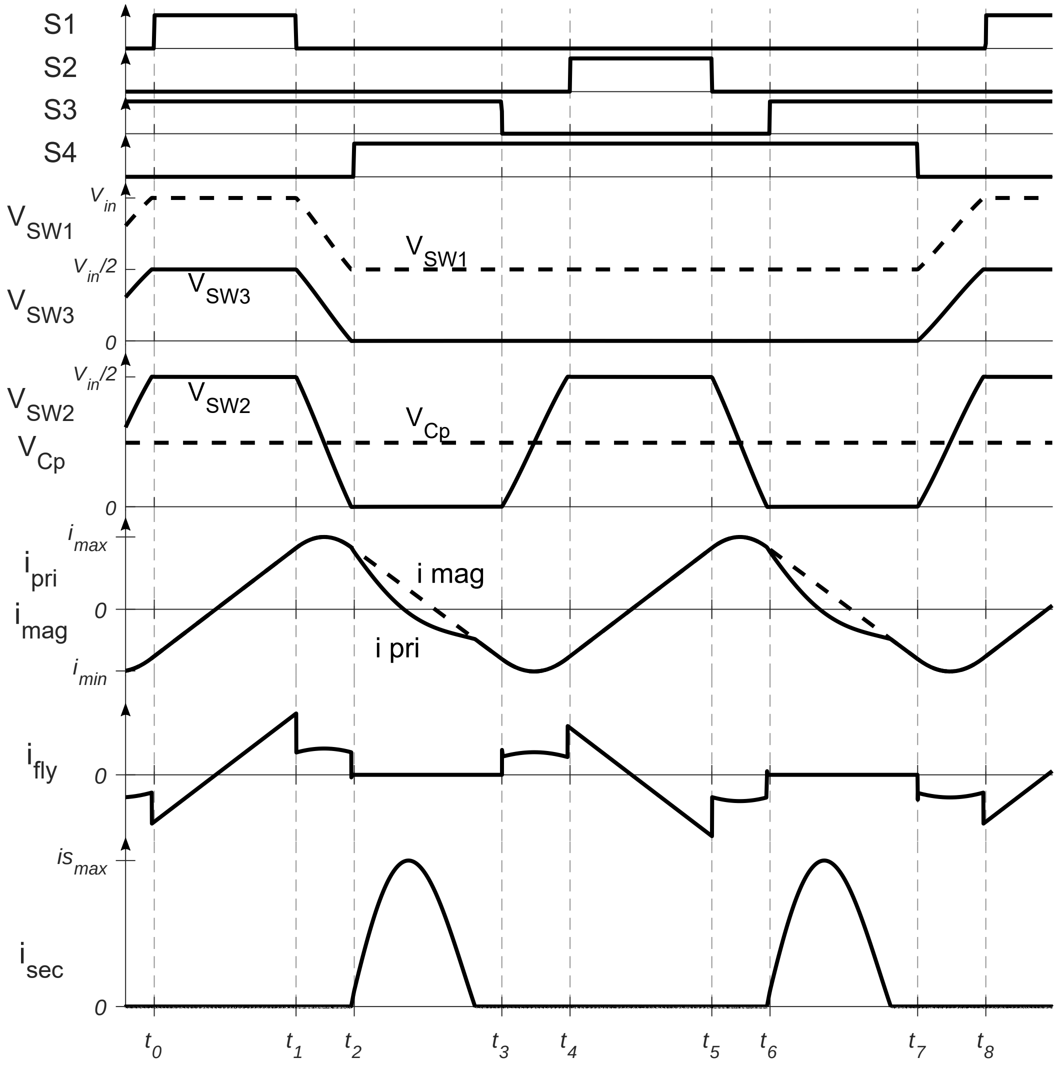


Figure 2.14: 3L-FC-AHBF - Main waveforms in simulation

State 2 (t_1 - t_2)

During state 2, the switching nodes $V_{SW1}, V_{SW2}, V_{SW3}$ are moving due to the energy stored inside the transformer's primary inductance, which charges/discharges the parasitic capacitors connected to these switching nodes. Figure 2.15 shows the equivalent model during state 2.

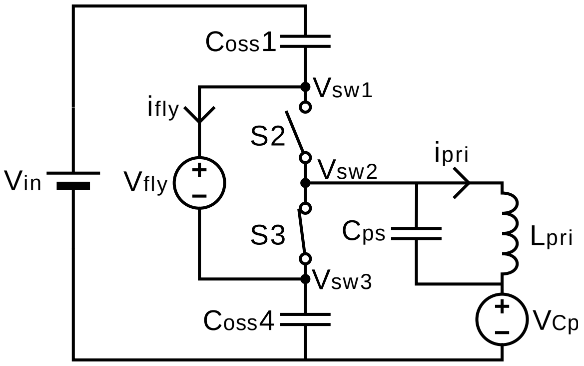


Figure 2.15: Equivalent model for 3L-FC-AHBF - State 2 (t_1 - t_2) & State 8 (t_7 - t_8)

It is interesting to note that these switching nodes are all connected together from an AC-variation perspective, because $S3$ tights V_{SW2} and V_{SW3} together and the flying capacitor forces a constant voltage between V_{SW1} and V_{SW3}. As a consequence, all the capacitors can be added to compute the total switching capacitor for this transition C_{SW0}:

$$C_{SW0} = C_{ps} + C_{oss1} + C_{oss4} \tag{2.40}$$

During this transition, the only current through the flying capacitor is the current that charges the output capacitance of the high-side switch C_{oss1}. Therefore, it is possible to express i_{fly} as a portion of the primary current:

$$i_{fly}(t) = i_{pri}(t) \cdot \frac{C_{oss1}}{C_{SW0}} \tag{2.41}$$

State 2 finishes at the end of the ZVS transition, when the switching nodes V_{SW2} and V_{SW3} reach ground.

State 3 (t_2 - t_3)

When the switching nodes V_{SW2} and V_{SW3} get to the ground level, the low-side switch $S4$ turns-on in ZVS conditions. Since both low-side switches $S3$ and $S4$ are in ON-state, the middle switching node V_{SW2} is forced to ground and the voltage across the transformer's primary is:

$$V_{pri}(t) = -V_{Cp} \tag{2.42}$$

This negative voltage across the primary side of the transformer translates into a positive voltage across the secondary side. It allows the forward bias of the secondary diode D which starts to conduct some current, as shown by the waveforms in Figure 2.14. The dynamic of the secondary current i_{sec} is decided by the voltage drop across the leakage inductance, as for the state 3 in the 2L-AHBF. The equations describing the present state will therefore be similar to the ones given for the 2L-AHBF.

Depending on the value of the leakage inductance, the current on the secondary side might cancel during state 3, as shown in Figure 2.14. Due to the secondary diode D, the secondary current is not allowed to flow in the opposite direction. On the primary side, the magnetizing current is therefore the only current that continues to flow if no current flows on the secondary side. But the secondary current cancellation does not impact the different voltage levels that stay the same until the end of state 3.

Note that the flying capacitor current is null during this period, since both high-side switches are off and the nodes where the flying capacitor is connected are not moving. The voltage on the flying capacitor prevents the voltage on the high-side switches to become too important, as it forces V_{SW1} to stay close to V_{fly}. And so the drain-source voltage on $S1$ and $S2$ during state 3 is only equal to $V_{in}/2$.

State 3 ends when the switch $S3$ turns-off.

State 4 (t_3 - t_4)

The turn-off of the switch $S3$ initiates a new ZVS transition, once again due to the energy stored in the magnetizing inductance. The equivalent model for the 3L-FC-AHBF in this state is presented in Figure 2.16. It shows the middle switching node (V_{SW2}) will move from ground level up to the flying capacitor voltage V_{fly}, charging/discharging all the parasitic capacitors connected to this node.

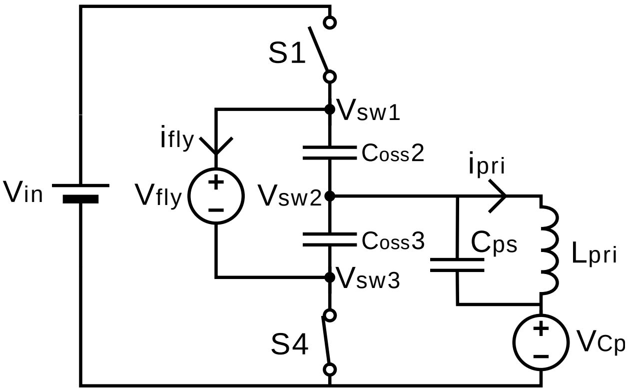


Figure 2.16: Equivalent model for 3L-FC-AHBF - State 4 (t_3 - t_4) & State 6 (t_5 - t_6)

Like for state 2, with an AC-perspective, all the parasitic capacitance contributions can be added to compute the total capacitor connected to the switching node during this transition C_{SW1}. This is possible because the flying capacitor clamps the voltage level of V_{SW1} and the switch $S4$ forces the switching node V_{SW3} to ground.

Like for the other ZVS transition, the flying capacitor current is a portion of the total primary current

$$i_{fly}(t) = -i_{pri}(t) \cdot \frac{C_{oss2}}{C_{SW1}} \tag{2.43}$$

where

$$C_{SW1} = C_{oss2} + C_{oss3} + C_{ps} \tag{2.44}$$

State 4 ends when the middle switching node V_{SW2} reaches the flying capacitor voltage.

State 5 (t_4 - t_5)

State 5 starts when $S2$ turns-on at t_4. Since both $S2$ and $S4$ are ON, the primary voltage can be written as

$$V_{pri}(t) = V_{fly} - V_{Cp} = \frac{V_{in}}{2} - V_{Cp} \tag{2.45}$$

This state is very similar to state 1, as the same voltage is applied across the transformer's primary side. It leads to the same linear increase of the primary current. However, during this state, the primary current is used to discharge the flying capacitor because the two currents flow in opposite directions, as shown in waveforms in Figure 2.14.

State 5 ends when the high-side switch $S2$ turns-off.

State 6 (t_5 - t_6)

The switch $S2$ turns-off at t_5. Due to the positive primary current the middle switching node V_{SW2} starts to move, falling from V_{fly} down to the ground level. During this state, the equivalent circuit of the power stage is the same as for state 4, shown in Figure 2.16. That is because the same parasitic capacitors that were discharged in state 4 now need to be charged (and vice versa), to enable the ZVS mode for the low-side switch.

The current through the flying capacitor is the current used to charge the output capacitance of $S2$ switch C_{oss2}, like during state 4, thus its expression is the same as in (2.43).

State 7 (t_6 - t_7)

State 7 starts when the middle switching node V_{SW2} reaches ground and the switch $S3$ turns-on.

This state is very similar to state 3, because both low-side switches are ON, leading to a negative primary voltage. Similarly to state 3, the negative primary voltage enable the secondary current to flow. The dynamic for the secondary current is still related to the voltage drop across the leakage inductor.

This state ends when the low-side switch $S4$ turns-off, which initiates a new ZVS transition.

State 8 (t_7 - t_8)

This last state consists in another ZVS transition, as the switching node V_{SW3} travels from ground to $V_{in} - V_{fly}$ when switch $S4$ turns-off at t_7. The behavior during this state 8 is very similar to the one obtained during state 2, as the equivalent model is the same for these two states (Figure 2.15).

Like during state 2, the flying capacitor current is used to discharge the output capacitor C_{oss1} of switch $S1$. It can therefore be expressed with the same expression, already given in (2.41).

2.3.2 Outcomes of the switching period analysis

Leakage influence and ZVS mechanism

The waveforms and the equations for the 3L-FC-AHBF show that the ZVS mechanism for this topology is very similar to the one of the 2L-AHBF topology studied previously. In both cases, it is the current stored in the magnetizing inductance that enables the ZVS operations.

The parasitic capacitors connected to the middle node to charge/discharge during the ZVS transitions are also quite similar - in both cases they are due to the output capacitor of two switches and to the parasitic capacitor of the transformer. Finally, the impact of the switching frequency on the dead-times duration and on the minimum RMS primary current is similar in the case of the 3L-FC-AHBF to the one identified for the 2L-AHBF.

The influence of the leakage inductance is also quite limited for the 3L-FC-AHBF topology. Its main role is to set the dynamic of the secondary current during state 3 and 7. Therefore, it is possible to make the same conclusion on the importance of the leakage inductance in the transformer design as for the 2L-AHBF. Since it does not have critical impact on the behavior of the topology, the constraint on its value can be released to improve the other parameters of the transformer.

Converter's main transfer function

Like for the 2-level version, it is possible to determine the input-output voltage relation for the 3L-FC-AHBF in steady-state.

Starting from the volt-second balance over a switching period, it is possible to find a relation between the input voltage and the primary capacitor voltage:

$$\int_0^T V_{pri}(t)dt = 0 \tag{2.46}$$

The volt-second balance on the primary voltage leads to

$$V_{Cp} = (V_{in} - V_{fly}) \cdot (\frac{t_1 - t_0}{T} + \frac{(t_2 - t_1) + (t_8 - t_7)}{2T}) + V_{fly} \cdot (\frac{t_5 - t_4}{T} + \frac{(t_4 - t_3) + (t_6 - t_5)}{2T}) \tag{2.47}$$

Note that this last expression assumes, like for the 2L-AHBF, that the variations of the primary voltage (V_{pri}) during the ZVS transitions are linear.

To simplify this expression, the flying capacitor voltage is presumed to be equal to $V_{in}/2$. If the on-time of the switch k is denoted $t_{ON_{Sk}}$, and the dead-time associated to the ZVS transition occurring just before the k switch turn-on is denoted dt_{Sk}, the expression becomes:

$$V_{Cp} = \frac{V_{in}}{2} \cdot \frac{1}{T} \cdot (t_{ON_{S1}} + t_{ON_{S2}} + \frac{dt_{S1} + dt_{S2} + dt_{S3} + dt_{S4}}{2}) \tag{2.48}$$

Since the on-time values of switches $S1$ and $S2$ are identical in steady-state in an ideal operating mode and denoted D, then the expression can be written as

$$V_{Cp} = V_{in} \cdot (D + \frac{dt_{S1} + dt_{S2} + dt_{S3} + dt_{S4}}{4T}) \tag{2.49}$$

Finally, the equations for the dead-times seem to indicate that high-side switches $S1$ and $S2$ would have a similar dead-time duration and the same applies to dead-times for $S3$ and $S4$. As a consequence, the simplified formula for the primary capacitor voltage would be

$$V_{Cp} = V_{in} \cdot (D + \frac{dt_{HS} + dt_{LS}}{2T}) = V_{in} \cdot D_{eff} \tag{2.50}$$

with D_{eff} the effective duty-cycle of the high-side switches, that takes into account the different dead-times.

On the other hand, it is possible to relate the voltage across the primary capacitor V_{Cp} to the output voltage with the same formula as for the 2L-AHBF topology:

$$V_{out} = \frac{V_{Cp}}{N_{tr}} \cdot \frac{L_{mag}}{L_{mag} + L_r} - V_D \tag{2.51}$$

Injecting (2.50) into (2.51) is giving the relation between the input and output voltages

$$V_{out} = \frac{V_{in}}{N_{tr}} \cdot \frac{L_{mag}}{L_{mag} + L_r} \cdot (D + \frac{dt_{HS} + dt_{LS}}{2T}) - V_D \tag{2.52}$$

This relation is the same as for the 2L-AHBF which shows that the two versions of this topology operate in a very similar way. Like for the 2L-AHBF, it is worth noting the impact of the dead-time duration (i.e. of the ZVS transitions) on the output voltage, that is the consequence of the primary current charging/discharging the primary capacitor C_p also during the ZVS transition phases.

Flying capacitor's balancing

One of the basic assumption made when studying the 3L-FC-AHBF and its non-isolated versions, is to assume that the flying capacitor voltage is constant and equal to $V_{in}/2$. However, due to non-ideal characteristics of the power and control circuits, it might not be the case.

This could cause several issues. If this voltage is smaller or larger than its expected value, it will lead to extra voltage-stress on the switches (for example, voltage stress on switches $S1$ and $S2$ during state 3 is equal to $V_{in} - V_{fly}$ and V_{fly}, respectively). This imbalance will therefore be an issue if the flying capacitor voltage takes a value that is very different from its expected ideal value, as it could damage the power devices. At the same time, the imbalance might also impact the performances of the converter. A non-ideal flying capacitor voltage will make waveforms asymmetrical, leading to higher currents, non-ZVS mode and even EMI issues.

The flying capacitor voltage imbalance are generally due to the imperfections in the control of the power switches [42, 43]. Indeed, the previous analysis assumed that switches were controlled without any delay, with a phase shift exactly equal to 180° and with an identical duty-cycle. In reality, some delays will appear in the control of the power switches, and they might not be the same for all of them, eventually leading to non-ideal phase shift and non identical duty-cycles.

To highlight the cases where imbalance might appear, it is possible to study the quantity of charges flowing in and out of the flying capacitor over a switching period, looking at the flying capacitor current i_{fly} shown in Figure 2.17.

The study focuses on state 1 (t_0 - t_1) and state 5 (t_4 - t_5) because no charges difference is observed in the other states.

When both low-side switches are ON (state 3 and 7), no current flows through the flying capacitor. During the ZVS transitions, the current that flows through the flying capacitor is used to discharge the parasitic capacitor of high-side switches ($S1$ or $S2$) before they turn-on.

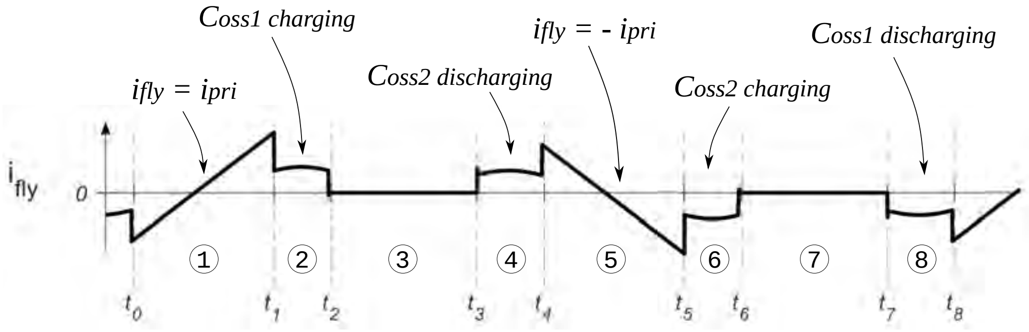


Figure 2.17: Typical waveform of flying capacitor current in the 3L-FC-AHBF

However, the same quantity of current is used to also charge the same parasitic capacitor when these switches turn-off, which lead to no difference in the flying capacitor charges over a switching period. In other word, charges difference observed during state 2 (t_1 - t_2) balances with the one occurring during state 8 (t_7 - t_8), and the same thing happens for state 4 (t_3 - t_4) and state 6 (t_5 - t_6).

The expression of the difference of charges inside the flying capacitor over a switching period ΔQ_{fly} can therefore be simplified. It can be written as the sum of the charge differences in state 1 (t_0 - t_1) and 5 (t_4 - t_5):

$$\Delta Q_{fly} = \int_0^T i_{fly}(t)\ dt\ = \Delta Q_{st1} + \Delta Q_{st5} \tag{2.53}$$

where ΔQ_{st1} and ΔQ_{st5} can be computed as:

$$\Delta Q_{st1} = i_{pri}(t_0) \cdot (t_1 - t_0) + \frac{V_{in} - V_{fly} - V_{Cp}}{L_{mag} + L_r} \cdot \frac{1}{2} \cdot (t_1 - t_0)^2 \tag{2.54}$$

$$\Delta Q_{st5} = -i_{pri}(t_4) \cdot (t_5 - t_4) - \frac{V_{fly} - V_{Cp}}{L_{mag} + L_r} \cdot \frac{1}{2} \cdot (t_5 - t_4)^2 \tag{2.55}$$

The expression for ΔQ_{fly} in these states is quite similar, except for the sign. It comes to the fact that during state 1, the primary current i_{pri} charges the flying capacitor, while during state 5, primary current discharges it, hence the minus signs in (2.55). As shown in Figure 2.17, the flying capacitor current i_{fly} and the primary current i_{pri} flow in the same direction during state 1 and in opposite directions during state 5.

One way of analyzing these equations is to consider the ideal case, for which high-side switches are controlled with an identical duty-cycle and the phase-shift between the two complementary pairs is exactly 180°. In these conditions, if the flying capacitor voltage is also close to its ideal value $V_{in}/2$, then the ΔQ_{fly} during state 1 and state 5 should cancel, leading to a stable value for the flying capacitor voltage. This is usually referred as the natural balancing of the flying capacitor. However, if one of these parameters' value is not ideal, then the charge balance will be lost, and the flying capacitor voltage will deviate critically from its ideal value.

To illustrate the impact of an invariable phase-shift error in the control of the two half-bridges, Figure 2.18 shows the flying capacitor voltage obtained in steady-state for a constant phase-shift error. The results are obtained using the SIMetrix SIMPLIS simulation tool. It reveals that an error of 1% (i.e. a 20 ns constant phase-shift error) already has a significant effect on the flying capacitor voltage in steady state, since it leads to a 8 V error for the flying capacitor voltage. It underlines the importance of matching the delays to drive the power switches, further details are discussed in chapter 3. Note that the imbalance observed on the flying capacitor voltage is independent from the value of the capacitor, so it cannot be reduced by increasing its size.

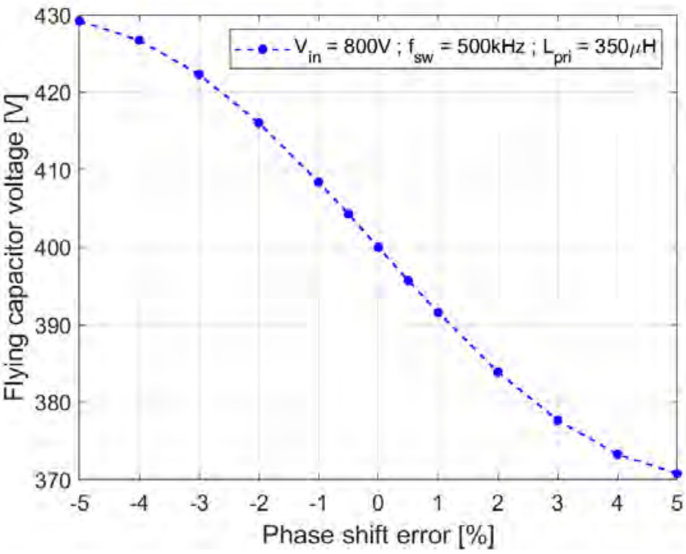


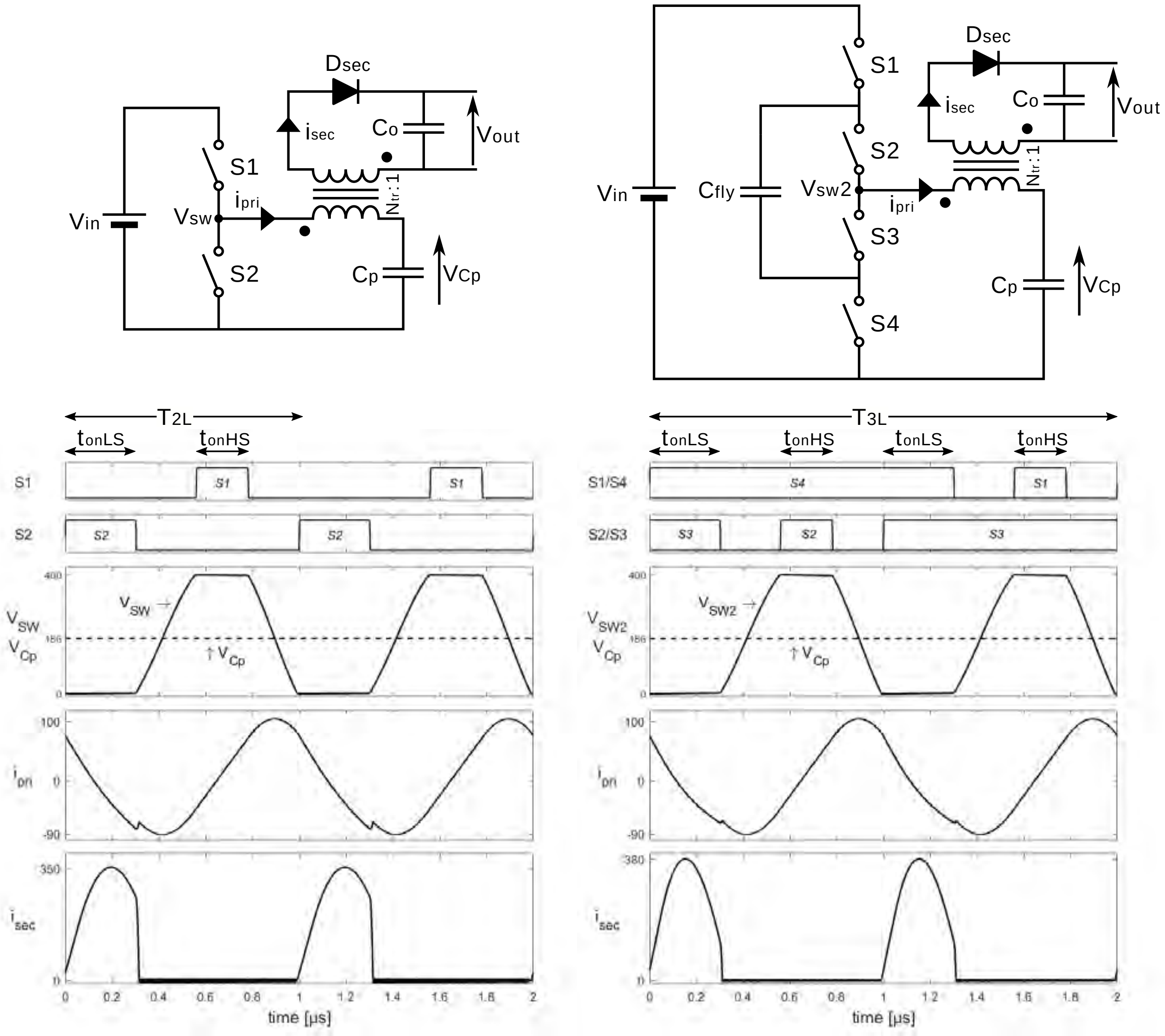
Figure 2.18: Flying capacitor voltage imbalance due to constant phase-shift error

This analysis of the balancing conditions for the flying capacitor shows the importance of the design of the control circuits of the power switches. Their design show tend to match the delays to guarantee a similar duty-cycle and a 180° phase-shift between the two half-bridges, to avoid the flying capacitor voltage to critically deviate from its ideal value.

Waveforms comparison between 2L-AHBF and 3L-FC-AHBF

The analysis of the 2L-AHBF and of the 3L-FC-AHBF operating mode conducted already revealed some similarities between the two versions of the topology: a similar ZVS mechanism, the same input-output voltage relation, etc. However, considering the input voltage of each version, it is possible to push the comparison further. The 2L-AHBF and the 3L-FC-AHBF are to be used with different input voltage ranges: the input voltage considered is 400 V for the 2L version and 800 V for the 3L-FC. Note that the maximum and the minimum voltage of the two voltage ranges are also related such that it is possible to consider that the input voltage of the 3L-FC-AHBF is the twice the input voltage of the 2L-AHBF over the complete range.

There are few aspects for which the similarities are particularly interesting that are listed below and Figure 2.19 illustrates them showing the waveforms obtained for the two versions of the ML-FC-AHBF.



(a)

(b)

Figure 2.19: Schematics and simulation waveforms for (a) 2L-AHBF, V_{in} = 400 V, f_{SW} = 1 MHz, L_{pri} = 500 µH and (b) 3L-FC-AHBF, V_{in} = 800 V, f_{SW} = 500 kHz, L_{pri} = 500 µH

- **Middle switching node voltage and parasitic capacitor**: In both version, the same voltage is applied to the middle switching node: the full input voltage is applied to this node for the 2L-AHBF but for the 3L-FC-AHBF, only half of the input voltage is applied to V_{SW2} thanks to the flying capacitor which compensate for the higher input voltage. Moreover, during the ZVS transitions, the same amount of parasitic capacitors is connected to the switching node.

- **Transformer's voltage and current**: Since the same voltage is applied to the middle switching node in both versions and since the voltage across the primary capacitor C_p is similar because the output voltage and the transformer turns ratio are the same, then the same voltage applies to the transformer windings in both versions. For the currents, if the transformer's frequency and on the inductance value are the same in both versions, then the magnetizing current should also be the same. For the secondary current, minor variations can be observed between the two versions, due to the parasitic resistances that changes the voltage across the leakage inductance and so the dynamic of the secondary current. But overall, the primary current waveforms should be alike, as illustrated in Figure 2.19.

- **Power switches on-time constraints**: Finally, the on-time constraints for the high-side and the low-side switches required to get the targeted output voltage are quite similar as well. For the high-side, the on-time required (t_{onHS}) is the same because the duty-cycle required for the 3L-FC-AHBF is half of the one needed for the 2L-AHBF which compensated for the switching period that is two times longer in the the case of the 3L-FC-AHBF ($T_{3L} = 2 \cdot T_{2L}$). For the low-side switches, the on-time constraint (t_{onLS}) of the 2L-AHBF corresponds to the time where both low-side switches are "ON" in the 3L-FC-AHBF, as shown in Figure 2.19. t_{onLS} is also the time when the energy is transmitted to the secondary side of the transformer.

The simulations results shown in Figure 2.19 reveal the important similarities that will exist between a 2L-AHBF stage operating at 400 V switching at f_{sw} and a 3L-FC-AHBF operating at 800 V switching at $f_{sw}/2$. If the transformer's characteristics are the same (turns ratio, magnetizing inductance), then the current and voltage waveforms applied to this component should be almost identical. Moreover, the constraints that exist for the power switches minimum on-time are also quite likely to be the same.

The great similarities that appear between the two targeted versions of the power stage will be particularly interesting during the design phase of the transformer. Indeed, a single transformer design used in the 2L-AHBF and the 3L-FC-AHBF should lead to the same behavior of the power stage and to performances very close in the two cases.

Therefore, most of the considerations regarding the power stage and the transformer design will be valid in both versions of the topology, such that only one converter design will be required instead of two. Nevertheless, small differences will appear between the performances of the two versions but this is discussed more into details in Chapter 4 and in Appendix B.

2.3.3 Early results from a discrete prototype

A prototype of the 3L-FC-AHBF is built in order to validate some aspects of the predicted topology behavior, like the ZVS mechanism, the input-output voltage relation, the flying capacitor stability, etc. and to get some first indications of the architecture's performances.

Main components used

The prototype of the 3L-FC-AHBF is built using discrete components assembled on a Printed Circuit Board (with a second board for the supplies), as shown in Figure 2.20. The main board is composed of the basic components to create the 3L-FC-AHBF stage (four switches, two high-voltage capacitors, a transformer, a rectification diode, an output capacitor, etc.) plus some additional circuits required for the control. A start-up circuit, that consists in a start-up resistor in parallel with a low-resistance MOSFET (that is turned-on once the input capacitor is charged) is added to limit the inrush current.

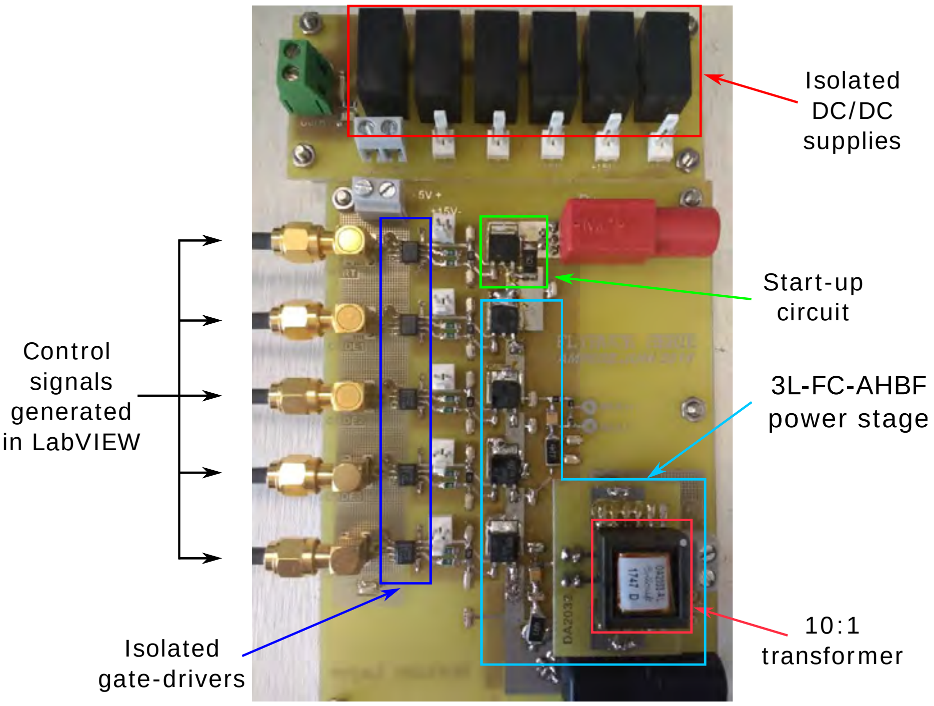


Figure 2.20: PCB boards of the discrete prototype for the 3L-FC-AHBF topology

The components used to build the 3L-FC-AHBF power stage are listed in Table 2.1. Additional components are used to control the 3L-FC-AHBF stage: isolated gate-drivers (Texas Instruments, UCC5320SC), to drive the floating power switches and isolated DC/DC converters (Murata, MEA1D1215SC), to generate the floating supplies required for the isolated gate-drivers.

Table 2.1: List of the main components used for the 3L-FC-AHBF power-stage

Component	**Characteristics**	**Reference & Manufacturer**
Power MOSFET	max V_{DS} = 600 V, R_{DS} = 6.7 Ω	STD1HN60K3 ST
Transformer	L_{mag} = 1.0 mH N_{tr} = 10:1, R_{pri} =1.1 Ω	DA2033-AL[1] Coilcraft
Secondary diode	max V_R = 100 V V_D = 0.5 V (@ 100 mA)	PMEG10020ELR Nexperia
High-voltage capacitors	22 nF, 630 V	

[1] *The transformer was used in reverse direction, as it is sold as a 1:10 coupled inductor*

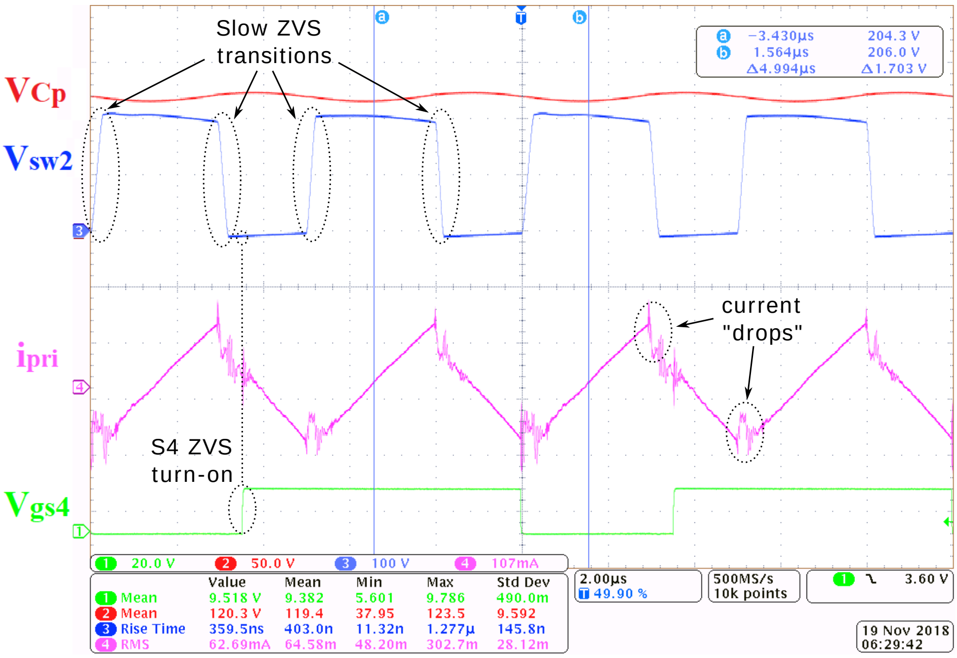
The different control signals are generated using a custom LabView software and transmitted to the board through a National Instrument IO controller. The software allows to change the duty-cycle and the frequency of the PWM signals but also to control the dead-time between complementary signals.

Note that no regulation mechanism is introduced in this prototype, it operates in open-loop. To get to the targeted output voltage value depending on the input voltage, it is possible to change the duty-cycle of the high-side switches of the converter or the dead-time, as shown previously while studying the main transfer function of the converter.

Finally, the load used on the output simply consist in a 150 Ω resistor, such that when the output voltage is at the targeted value (12 V), the output power is close to the 1 W specification.

Results

Unless specified otherwise, the analysis of the topology behavior was performed with the following parameters: $V_{in} = 400$ V, $V_{out} = 12$ V, $R_{load} \approx 150\ \Omega$, $f_{SW} = 100$ kHz, $D_{eff} = 30\%$. The maximum input voltage during the measurements is limited compared to the targeted specification (400 V instead of 800 V). It is necessary to limit the risk of a too high voltage stress on the power stage components, especially at start-up when the flying capacitor is discharged. But this limited voltage does not impact the general behavior of the converter and some interesting conclusions can still be made in these conditions. Figure 2.21 shows the main waveforms measured in steady-state.



	Value	Mean	Min	Max	Std Dev
1 Mean	9.518 V	9.382	5.601	9.786	490.0m
2 Mean	120.3 V	119.4	37.95	123.5	9.592
3 Rise Time	359.5ns	403.0n	11.32n	1.277µ	145.8n
4 RMS	62.69mA	64.58m	48.20m	302.7m	28.12m

Figure 2.21: Measured waveforms of the 3L-FC-AHBF power stage shown in Figure 2.20

The predicted ZVS mechanism can be observed on the measured waveforms, although only the low-side switch control signal (V_{GS4} in Figure 2.21) is actually measured. Indeed, the slow transitions of the middle switching node V_{SW2} from low-voltage to high-voltage indicate that the switching node rise is not due to the turn-on of the high-side switch, but to the resonant charging of the parasitic capacitors, as expected. It can also be noticed that the low-side switch $S4$ is turned-on in ZVS conditions, since the middle switching node V_{SW2} reaches the ground level before the transistor's gate voltage rises. One thing that did not appear in the simulated waveforms is the "drop" observed in the primary current waveform during the ZVS transitions.

It is probably due to the current that the transformer "steals" from the total primary current to charge the parasitic primary-secondary capacitor C_{ps}.

The converter transfer function described earlier also seem to correspond to the analysis outcome. Indeed, the voltage measured across the primary capacitor V_{Cp} is very close to the value computed using (2.50), as $V_{meas} = 120.3$ V and $V_{theo} = 400 \cdot 0.3 = 120$ V.

Some variations of the voltage across the primary capacitor (C_p) can be observed in Figure 2.21. The value of the selected capacitor is too small (22 nF) to operate at such low-frequency. However, in future designs, a larger value of capacitor can selected to avoid this issue and the penalty on increased component's size should be limited, thus the hypothesis of a constant primary voltage V_{Cp} made during the analysis is still valid (1 μF ceramic capacitor rated for 600 V can be found on the market).

Finally, the voltage across the flying capacitor, although it is not directly measured, can be deduced from the high-voltage value of the middle switching node V_{SW2}. The voltages measured at this node during state 1 (cursor ⓑ) and during state 5 (cursor ⓐ) are very close. It indicates that the flying capacitor voltage is close to its expected value of $V_{in}/2$. It is not exactly equal to the ideal value, as the voltage measured at the middle switching node is not exactly $V_{in}/2$, but it is probably due to some mismatch in the control delays and to the voltage ripple on the flying capacitor (similar to the one measured across the primary capacitor C_p).

The voltage measured across the flying capacitor is quite promising, especially considering that the power stage runs in open loop. It shows the flying capacitor voltage will naturally balance to a value that is close to its ideal value if the mismatches in the control of the power transistors are small enough, even with no pre-charging strategy or dedicated control.

Efficiency measurements

The performances obtained with the discrete prototype are also monitored, a special attention is given to the power stage efficiency. It is defined as the ratio of the power drawn by the output load to the power delivered by the main supply (V_{in}). The power that comes from the auxiliary supplies, used to power all the isolated gate-drivers, is not taken into account in the efficiency calculation.

The efficiency measurement are done with a constant 1 W load, with $V_{out} = 12$ V, for an input voltage between 300 V and 500 V. The measurements are repeated at three different switching frequencies and are summarized in Figure 2.22.

The efficiency measured for the low input voltages ($V_{in} < 400$ V) is reasonably good as it is close to the targeted value ($\eta_{spec} \geq 85\%$). However, the performances obtained at high input voltage ($V_{in} \geq 450$ V) are not sufficient, as efficiency drops below 75% when $V_{in} = 500$ V.

To explain the low efficiency observed for high input voltages, some measurements with no output load are conducted. Their objective is to get rid of losses on the secondary side of the transformer, which are difficult to estimate and to focus on the losses on the primary side and inside the transformer. Except for the output load, this new set of measurements is done with similar parameters, such that voltage and current waveforms on the primary side are not too much impacted.

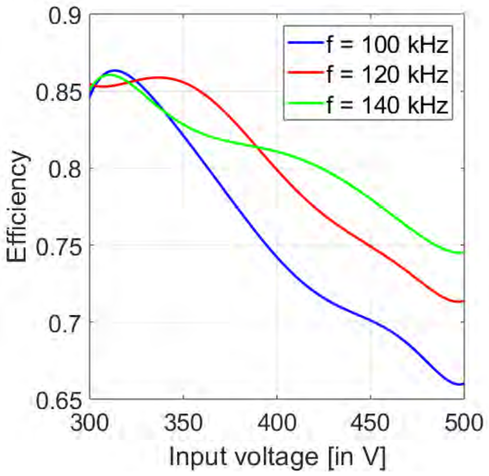


Figure 2.22: Measured efficiency for the 3L-FC-AHBF discrete prototype

The estimated loss breakdown, shown in Figure 2.23, is computed using the measured input power of the converter in steady-state with no load. The DC conduction losses are estimated by measuring the value of the primary RMS current and computing the total DC resistance on the primary side, due to the MOSFET on-resistance, the primary winding, the shunt resistor (used to measure current), etc. The rest of the losses is attributed to the transformer losses. The switching losses inside the MOSFETs are considered null because of the converter operates in ZVS mode.

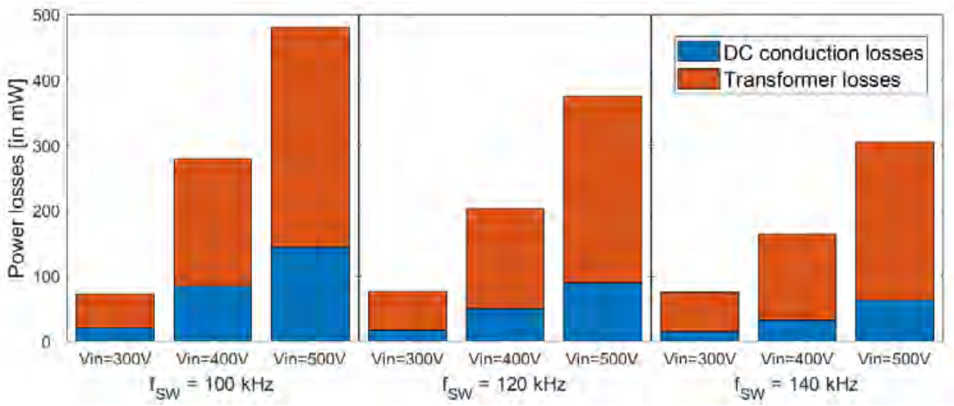


Figure 2.23: Estimated breakdown losses for no-load measurements

Using the results from these two types of measurement, it is possible to analyze the influence of some parameters on the efficiency (i.e. input voltage, switching frequency). Some estimations of the different source of losses can also be done, to help understanding which type of losses should be reduced in priority to reach a higher efficiency.

The results presented in Figure 2.22 and 2.23 outline the impact of the input voltage on efficiency. The losses breakdown shows that the loss increase observed when the voltage rises is due to both DC conduction losses and losses inside the transformer, which appear to be the main contributor.

Transformer losses can be divided into two types: AC conduction losses and core losses. The AC conduction losses are due to the resistance increase observed in the transformer windings at high frequency, due to skin effect and proximity effect. The core losses inside the magnetic core directly depend on the voltage that applied to the transformer. It is not easy to separate these two types of losses without running FEM simulations, because the measurements done with an impedance analyzer only allow to measure a global resistance increase, due to both frequency effect on the winding's resistivity and to core losses inside the magnetic material.

In both Figure 2.22 and 2.23, the benefit of an increased switching frequency appears. Indeed, increasing the switching frequency allows to reduce the primary current and so the conduction losses, but also the core losses, since volt-second decreases when the frequency increases. Although some limits will mitigate the benefit of a frequency increase on efficiency (like the AC effects on windings resistivity), these first results highlight the interest of designs operating at high switching frequency to get the targeted performances.

The transformer will be one of the key components to create a converter with high efficiency. The use of a non optimized transformer showed the limits of the converter performances for high input voltages. Note that the input voltage was limited to 500 V in the first series of tests and the efficiency is already below 75%. The challenge will be even greater when designing the converter for a 1 kV input voltage.

Nevertheless, these early results also revealed some hints on how to decrease the losses inside the converter, especially conduction and core losses. High switching frequency, low primary current and low core losses are the main ways that will be investigated to get to the targeted solution, in terms of cost, size and performances.

2.4 Conclusion

To efficiently design solutions for the two targeted input voltage ranges, it is decided to use two version of the ML-FC-AHBF topology. The 2L-AHBF will be used for the 400 V designs while the 3L-FC-AHBF is to be used for the 800 V designs. One advantage of this solution is to simplify the design phase, as a lot of similarities appear between a 2L-AHBF stage operating at 400 V and a 3L-FC-AHBF stage operating at 800 V.

The analysis of the 2L-AHBF topology allows to understand the main principles that rule the power stage behavior. In particular, the particularity due to the low-power mode are highlighted, as its impact the converter's main transfer function and the ZVS mechanism.

The analysis of the 3L-FC-AHBF shows that it is quite similar to the 2L-AHBF. Especially the ZVS mechanism and the main transfer function are the same. The flying capacitor balance is quickly studied and a general set of conditions is found to avoid issues to appear on this key component. The comparison between the transformer waveforms in a 2L-AHBF operating at 400 V and a 3L-FC-AHBF operating at 800 V show that the two versions are identical from the transformer's point of view which will facilitate the design of the two converters.

A PCB prototype is built using discrete components, to validate the choice of the 3L-FC-AHBF topology, monitor its behavior and start to measure its performances. The results seem to confirm the behavior analysis conducted and the efficiency measurements show the critical aspects that will need to be taken care of to built a solution with the targeted performances.

Chapter 3

Design of an IC brick

This chapter discusses the design of an Integrated Circuit (IC) built to reduce the area occupied by the active parts of the power stage. First, the motivations and the targets of the IC design are introduced. Then, the intrinsic limits of the low-cost process used to fabricate the IC are revealed and the solution found to come around these issues is presented. The proposed solution aims at pushing forward the degree of integration with respect to what is usually done for High-Voltage IC. Finally, the important characteristics and the challenges related to the design of the main IC blocks are discussed at block level. The measurement results reveal some fragility in some blocks of the IC that cannot be corrected with a re-design due to the limited time and resources allocated to this phase. Nevertheless, the global functionality of the IC is validated through simulation.

3.1 Motivation and objectives of the IC design

The PCB prototype of the 3L-FC-AHBF topology built using discrete components (at the end of Chapter 2) revealed that many devices are required to control and drive the power stage, increasing the solution cost and footprint. In order to reduce the number of external components the integration of the "active" parts of the power stage is targeted. Integration technologies based on silicon enable to integrate all the active parts required for the power stage (power switches, control and supply circuits) in a single package, which allows to significantly reduce the size of the solution.

Some additional constraints appear for High-Voltage Integrated Circuit (HVIC) such that they usually include only a limited number of functions (e.g. level-shifters and gate-drivers, but not the power switch and the floating supply). However, the low-power context releases the thermal constraints that usually limit the integration of these blocks, thus enabling the possibility to study the case where all these blocks are integrated in the same HVIC.

So the aim of the IC design phase is to show how power switches, control circuits and floating supplies can all be integrated to reduce the external component count. Figure 3.1 illustrates the targeted level of integration of the IC designed. It should require only a low-voltage supply and two PWM signals to control the power stage. Only external passive components would then be required to build the 3L-FC-AHBF stage (i.e. few high-voltage capacitors, a transformer, a rectification diode and an output capacitor). In a second phase, the regulation loop to generate the PWM signals could be implemented inside the IC and the low voltage supply could be generated from a transformer's auxiliary winding to create a "self-sufficient" solution, but it is not developed here.

An additional objective of the IC concerns its "flexibility" or its "modularity": the same IC should offer the possibility to build both 2L-AHBF and 3L-FC-AHBF topologies.

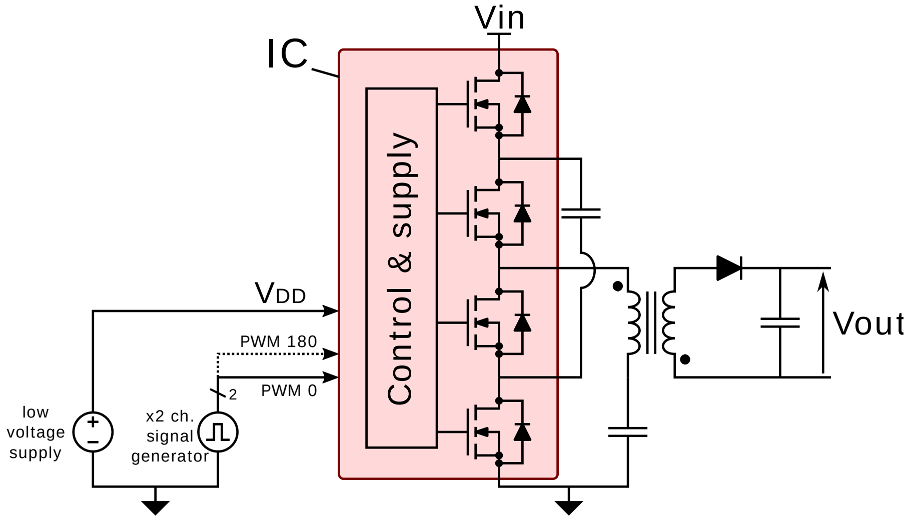


Figure 3.1: Objective of the integrated circuit

3.2 Process limitations and proposed solution

The technology is a High-Voltage bulk CMOS silicon process. It remains an interesting alternative to SOI processes (that are often used to build HVIC) as it is low-cost. However it presents serious limitations, especially in terms of isolation. Being a junction-isolated technology, it does not offer the possibility to isolate two high-voltage devices, because these devices already require the maximum isolation "strength" to withstand the high-voltage. Therefore it is not possible to place several HV devices floating at different voltage levels on the same die. In the case of the 3L-FC-AHBF, there are four power switches and three of them are floating devices. So it will not be possible to integrate all the power devices on the same die using the targeted process.

To overcome this limit, each HV power switch that composes the power stage should be placed on a separate die. Therefore two dies are required to create the 2L-AHBF and four dies are needed for the 3L-FC-AHBF. Although this solution allows to build the targeted power stage, it will have a negative impact on the cost of the solution (due to the multiple dies) and possibly on the size of the solution. The footprint increase could be mitigated using techniques that allow to package several dies together, like System-in-Package (SiP) or Multi-Chip-Module (MCM) technologies. However, the practical implementation of these types of techniques would require a specific study that was not conducted due to lack of time. In general, issues related to the packaging of the IC were not really considered in this work that focuses on the validation of the IC design. Another potential issue with this approach is that it could require more engineering work to design the different ICs, because the high-side and the low-side dies do not operate in the same way and don't require the same building blocks.

The solution found to avoid the design of multiple ICs is to design a single "IC brick", that can be "programmed" and connected to other bricks to create the targeted power stage, as illustrated in Figure 3.2. This chapter focuses on the design of the main building blocks of the IC brick required to control and supply the floating circuits.

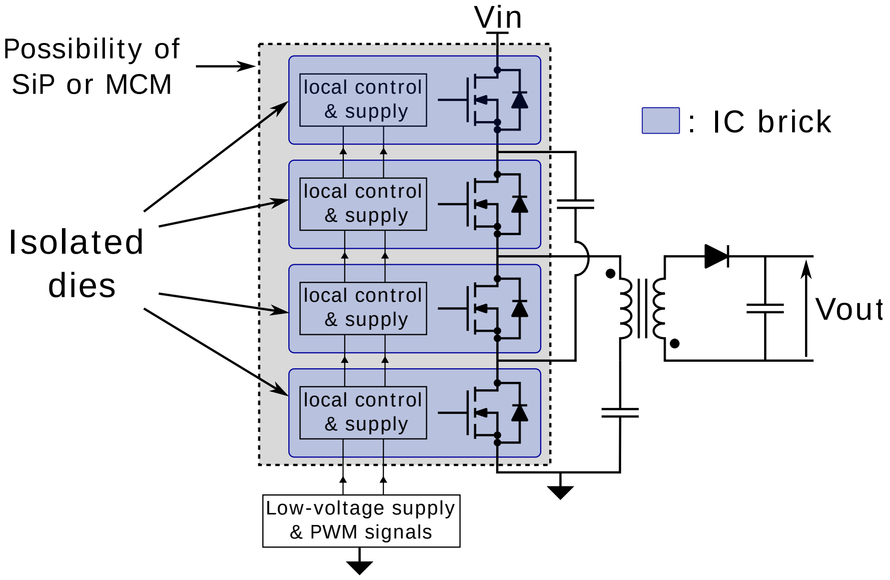


Figure 3.2: Proposed architecture for integration to overcome process limitations

To reach the targeted integration level described in Figure 3.1, the IC bricks should include some important building blocks. The first one is the HV-MOSFET used as a power switch in the power stage of the converter and the associated gate-driver. Then, a level-shifter block is required to transmit the low-side PWM signals to the floating IC bricks, to control their power switch. Finally, a bootstrap supply and a storage capacitor are needed to transfer the energy from the low-side low-voltage supply to the floating bricks and store it. Additional circuits are included but not discussed in details: input and output filters for digital signals, ESD protections, internal voltage and current references, etc. Figure 3.3 summarizes the important blocks included in the IC brick. Several blocks are still missing to create a robust IC, but time constraints made it difficult to build a complete solution. For example, a dedicated start-up circuit would be required to ensure a suitable charging of the flying capacitor and of the floating storage capacitors, especially if start-up constraints are strong (e.g. considering hot-plugging possibility).

The IC brick also includes a block dedicated to the "programming" of the IC. Input digital signals are used to enable or disable some blocks and functionalities of the IC brick. For example, it is used to determine the position of the IC in the power stage, since a die located on the low-side won't use the same building blocks as a die located on the high-side.

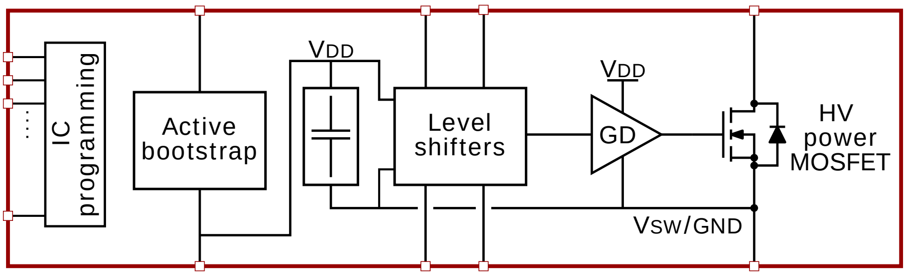


Figure 3.3: IC brick's main building blocks

A photo of the manufactured IC brick is shown in Figure 3.4. The pinout configuration is similar to what is shown on the Figure 3.3: digital input and output pins are placed on the left side of the test-chip, while the pins to connect the IC brick to other IC bricks or to the power stage are placed on the top and bottom side. The objective of such a distribution is to ease the connections of the isolated dies if they were to be packaged together. The image also reveals that a large portion of the IC is occupied by the storage capacitor, that was made as large as possible since the IC dimensions were fixed. The reason for making this large capacitor are discussed in the section dedicated to the design of the active bootstrap circuit.

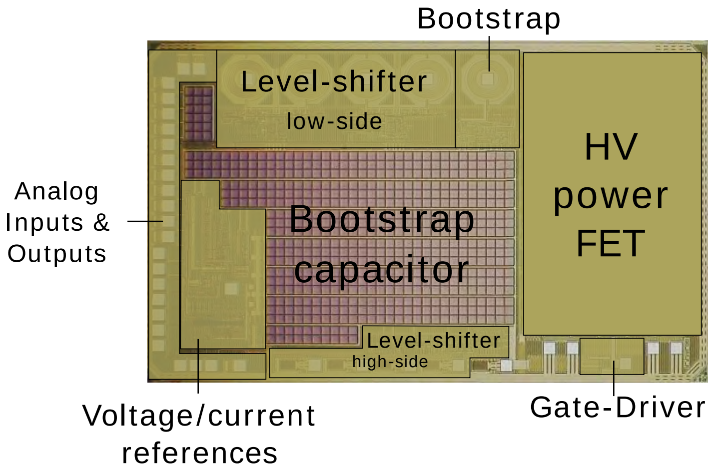


Figure 3.4: Microscope top-view of the manufactured IC brick

3.3 Design overview

In this section, the main building blocks of the IC brick as shown in Figure 3.3 are presented (except the "IC programming" block that simply consists in few logic gates to enable or disable some building blocks). Their function and important characteristics are discussed. For the more complex blocks (i.e. level-shifter and bootstrap) the main design challenges are exposed and the proposed solution described. In the end, when it is possible, the measured characteristics of the building blocks are given, to validate the design of the IC brick.

Note that the goal of this section is not to enter the design with deep details, since the schematics of the building blocks won't be presented. But the main function blocks included in each circuit are displayed to offer a better understanding of how they operate.

3.3.1 Power MOSFET

A high-voltage N-type MOSFET is selected to be the power device included in the IC brick. Due to the limits of HV CMOS bulk technology, it is not easy to design a switch with low on-resistance without making it very large. However, due to the low-power context, a higher on-resistance does not represent an issue as this device should not support large currents. On the other hand, it should remain small enough to limit the parasitic capacitors to allow the converter to reach a high switching frequency. Although the sizing of such device is usually of great importance for the behavior and the performances of the converter, time constraints made it impossible to study in details the impact of this parameter during the IC design phase. It is discussed more in details in the Appendix C.

Static measurements

The static measurement are operated using a device analyzer (IWATSU Curve Tracer CS-5400). The gate is polarized to a known voltage level and at the same time, a SMU measures the drain current and voltage. The 4-wire measurement technique is used to improve accuracy. The measurement setup is presented in Figure 3.5.

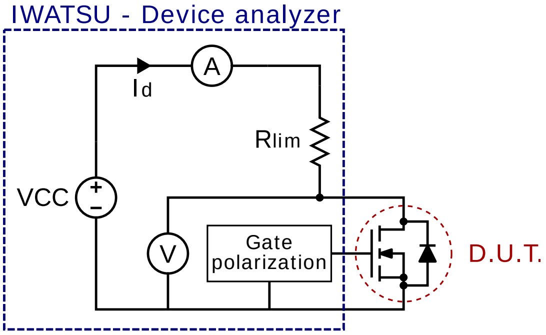


Figure 3.5: Simplified view of on-resistance measurement setup

This allows to measure the MOSFET chanel's on-resistance and its variations with the drain current, as presented in Figure 3.6. It shows the power MOSFET included in the IC brick presents, as expected, a large on-resistance value, that slightly varies with the drain current and the gate-source voltage.

The results show that for a gate-source voltage higher than 3.0 V, the on-resistance variations are quite small. Going from 3.0 V to 5.0 V, the resistance decreases of 2.5% and from 5.0 V to 7.0 V, the decrease is limited to less than 1%. The resistance measured for a 2.5 V gate-source voltage is higher than for 3.0 V and it appears to increase more rapidly when the drain current exceeds 100 mA. Overall, the value of the gate voltage should not severly impact the performances of the HV MOSFET if this voltage is higher than 3 V. This value can define the bottom limit of the voltage supply of the IC brick, to be used when designing the bootstrap circuit.

At the same time, the impact of the drain current on the on-resistance is also shown in Figure 3.6. It reveals that for the drain currents lower than 100 mA, the resistance increase is not too important (about +7% from 10 mA to 100 mA). Going from 100 mA to 200 mA, a similar increase is noted. It is probably due to the self-heating of the device, that is not

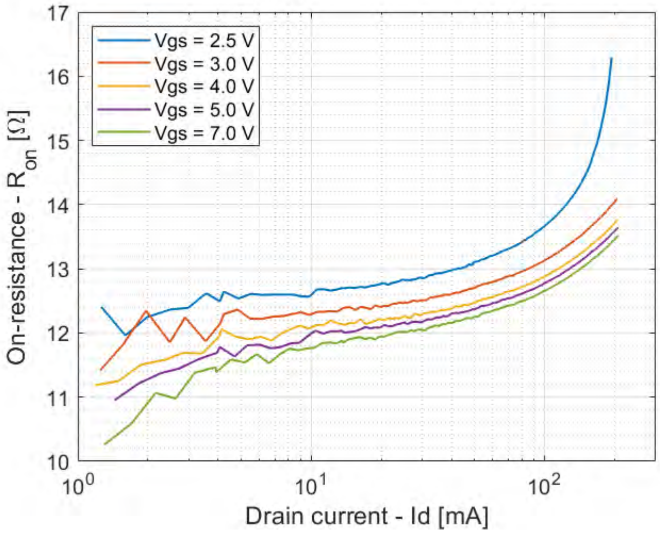


Figure 3.6: Static characteristic of power MOSFET inside the IC brick

designed to dissipate high conduction losses, but it should not be an issue for the targeted application, as the primary current value should remain lower than 150 mA.

As a result from the static measurements, a 13 Ω value is considered for the power MOSFET on-resistance model, that will be used to evaluate the conduction losses inside this device.

Dynamic measurements

To predict the dynamic behavior of the power MOSFET, its main parasitic capacitors need to be measured. In particular, the output capacitor (C_{OSS}) and the input capacitor (C_{ISS}) are often used to predict the switching behavior of a power device. The input capacitor is associated to the gate of the MOSFET, it can be seen as the equivalent capacitance that should be (dis)charged when turning the MOSFET on or off. It is important to take it into account when designing the gate-driver. The output capacitor accounts for the capacitances connected between the drain of the MOSFET and the other terminals (gate, source, bulk). As discussed in chapter 2, it is particularly important during the ZVS transitions.

The output capacitor of the power MOSFET is measured over a large range of the drain-source voltage using the measurement setup shown in Figure 3.7. Unfortunately, the input capacitor cannot be measured directly using a similar setup because of the circuits connected to the gate of the power device that forbid to measure the current entering the gate. Nevertheless, its equivalent value will be estimated when measuring the consumption of the gate-driver circuit.

The main contributors of the output capacitor are the gate-drain capacitance (C_{gd}) and the drain-source capacitance (C_{ds}) as shown in Figure 3.7. To measure the output capacitor, the device analyzer (B1505 from Keysight) first sets the static drain-source voltage. Then, it adds on top of the DC voltage a small AC signal at a fixed frequency (100 kHz). Measuring the impedance between the two terminals of the device, it evaluates the value of the output capacitor (model used is C_p, R_p that is a capacitor connected in parallel with a resistance) and it repeats the operation for several values to cover the complete drain-source voltage range. The results are shown in Figure 3.8.

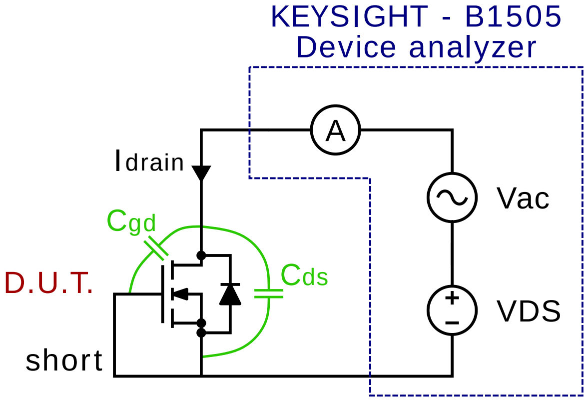


Figure 3.7: Simplified schematic of the output capacitor's measurement setup

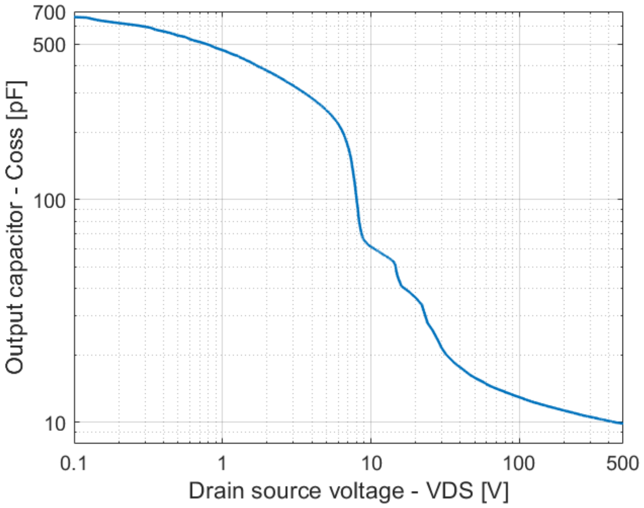


Figure 3.8: Dynamic characteristic of power MOSFET inside the IC brick

As expected, the output capacitor largely varies with the drain-source voltage and so it cannot be considered as constant (the impact of this change was discussed in Chapter 2 and is further exploited in Chapter 4). From the curve in Figure 3.8, it is possible to extract the equivalent output capacitor $C_{OSS\ eq}$ that can be defined as the capacitor that would require the same amount of charges as the real output capacitor to be completely charged:

$$C_{OSS\ eq} = \frac{1}{V_{DS}} \cdot \int_0^{V_{DS}} C_{OSS}(V)\ dV \tag{3.1}$$

For the power MOSFET inside the IC brick: $C_{OSS\ eq} = 19$ pF for $V_{DS} : 0\ \text{V} \rightarrow 500\ \text{V}$.

About the power MOSFET performances

Using the information from the static and the dynamic measurements, it would be possible to compare the performances of the present power MOSFET to power switches obtained using different process, technology or material. For example, devices built in GaN or in SiC would probably offer much better performances (e.g. for a similar output capacitor, the on-resistance would be much smaller) but these types of solution would drastically increase the cost of the converter. Moreover, the low performances of this device may not be critical to the converter's overall performances, as the losses in the MOSFETs should only represent a small portion of the losses.

However, it could be possible to use a similar process (high-voltage Si bulk CMOS) to improve the performances without increasing too much the costs. A trade-off is to be found between these two aspects, the goal of the present work is thus to explore what performances can be obtained when the low-cost issue is set as the main objective regarding the IC manufacturing.

3.3.2 Gate-driver

The gate-driver is the circuit used to reinforce the digital signal that should drive the power MOSFET gate. Its role is to limit the transition time of the gate voltage, but also the delays in the transmission of turn-on/off information and the power consumption. The gate-driver block connections are shown in Figure 3.9(a) and the main delays associated to the signal transmission and the gate transitions are described in Figure 3.9(b).

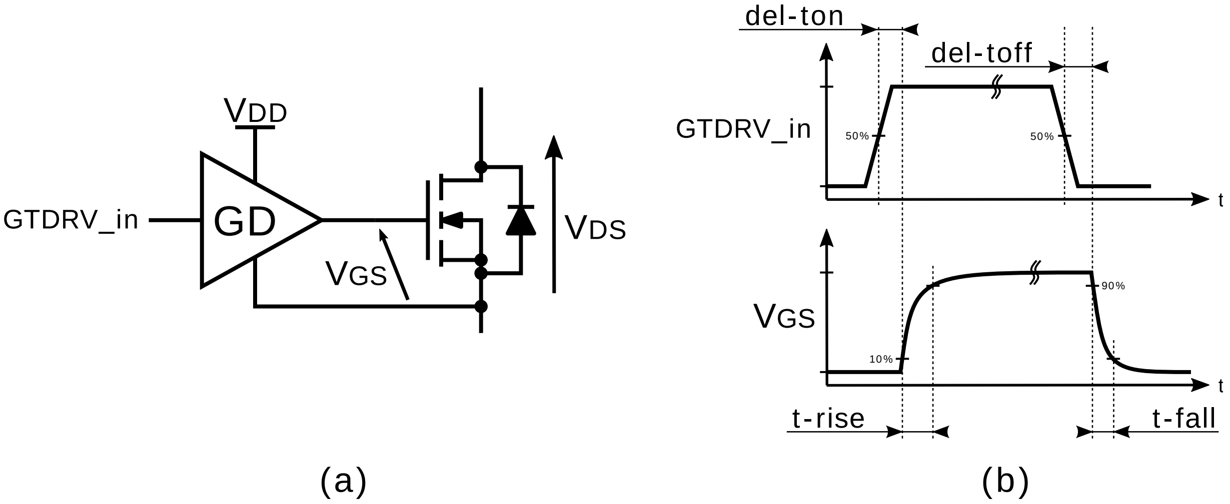


Figure 3.9: (a) Gate-driver block connection with (b) main waveforms and associated delays

The gate of the power MOSFET considered is quite small when compared to the one that can be found for devices driving more power. Thus, the design of the gate-driver circuit is simplified to its most basic form, that is a simple chain of inverters - each inverter being few times bigger than the previous to gradually amplify the signal driving the gate of the power MOSFET.

Delay measurements

To evaluate the performances of the gate-driver, the transmission delays and the gate's transition times are measured. For these measurements, the power MOSFET output is shorted ($V_{DS} = 0$ V). The gate-driver is directly driven by a PWM signal generated outside the IC brick and the power MOSFET gate voltage is measured for different supply voltage (V_{DD}). An oscilloscope is used to measure the delay associated to the transmission of the signal and the rising/falling time of the gate voltage. The transmission delays measured for the turn-on and the turn-off signals are shown in Figure 3.10. The rise-time and the fall-time of the gate voltage are depicted in Figure 3.11.

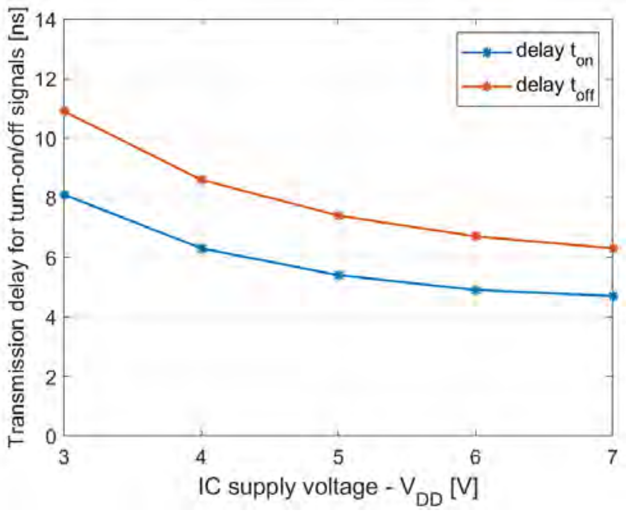


Figure 3.10: Transmission delays measured for turn-on and turn-off signals

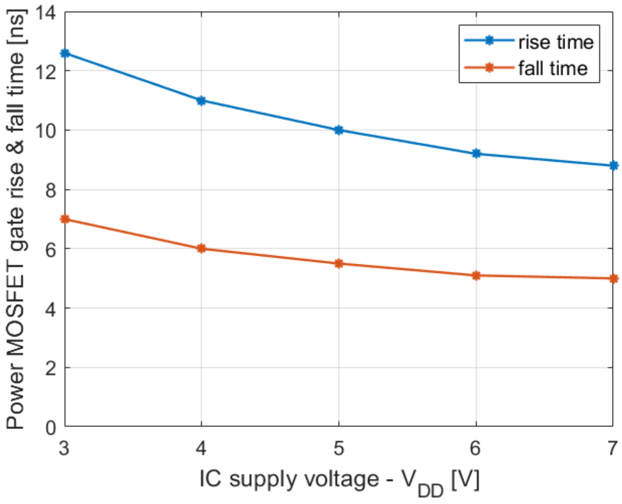


Figure 3.11: Rise and fall times of the power MOSFET gate

What can be noticed from these results is the dependency of the delays on the auxiliary supply: the higher the supply voltage, the faster the transmissions and the transitions. However, the difference remains small enough in absolute between the minimum and the maximum supply voltage (< 5 ns for the transmission delays). It is thus possible to conclude on the good functioning of the gate-driver circuit with a supply voltage from 3.0 V to 7.0 V, since the maximum targeted switching frequency is around 1 MHz.

Consumption and equivalent capacitor

Finally, it is possible to measure the power consumption of the gate-driver block, that includes the charges necessary to drive the power MOSFET. Measuring the auxiliary current supplied at different switching frequency, it is possible to evaluate the current consumption of the gate-driver. Results are shown in Figure 3.12. The supply current measured at null frequency indicates the DC power required for the IC brick to operate. The current consumption linearly increases with the frequency of the signal driving the power MOSFET gate. The power consumption can then simply be computed by multiplying the current measured by the constant supply voltage used ($V_{DD} = 5$ V here).

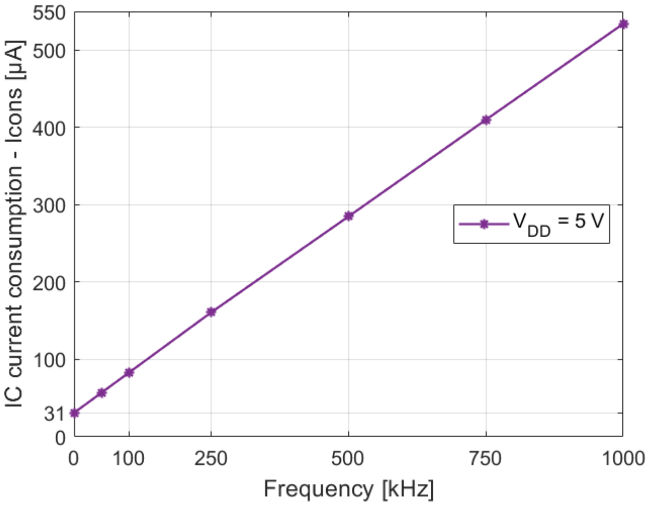


Figure 3.12: Current consumption of the gate-driver when driving the power MOSFET gate

Since the variation of the current consumed with the frequency is linear, it is possible to estimate the equivalent capacitor (C_{eq}) that this current charges during each period:

$$P_{cons} = V_{DD} \cdot I_{cons} = C_{eq} \cdot V_{DD}^2 \cdot f \tag{3.2}$$

Where I_{cons} is the current supplied to the gate-driver and f is the frequency at which the power MOSFET is driven.

Using (3.2), it is possible to compute a value for the equivalent capacitor that is charged/discharged by the gate-driver when piloting the power MOSFET gate. The computed value is about 100 pF, and it remains quite constant independently from the frequency. This value can be used as a rough estimation of the input capacitor of the power MOSFET ($C_{iss} \approx C_{eq}$). However, note that this last assumption completely neglects the current consumption of the gate-driver circuit itself, so it is only an approximation. But it can be useful to get an idea of the power consumption related to the driving of the power devices: for each power MOSFET driven at 500 kHz, the power consumed is about 1.25 mW (with $V_{DD} = 5.0$ V).

3.3.3 Level-shifters

The targeted 2L-AHBF and 3L-FC-AHBF power stages have both one (or several) switch(es) that are not referred to the ground level (i.e. switches of which source may be floating at a high-voltage). To control these floating switches using only low-side PWM signals (as stated in the IC design objectives), level-shifters are used to transmit the turn-on/off signals from the ground level up to the floating reference level of the switch to control.

First, the design principle of the level-shifter is presented. Then, the way the level-shifter block can be used to control a 2L-AHBF stage is described and validated based on simulation results. The proposed arrangement of level-shifter blocks to control a 3L-FC-AHBF power stage is discussed and the additional challenges related to this arrangement are pointed. Finally, a practical implementation of the level-shifter is performed and the measurements results reveal limitations in the operating range of the level-shifter block.

Design principle

The design principle of the level-shifter block is presented in Figure 3.13 for a simple half-bridge configuration. It reveals that the level-shifter is split into two parts. One part is located on the low-side IC brick (in blue) that is referred to ground level. The other part is located on the high-side IC brick (in red) which is referred to the middle switching node (V_{SW}).

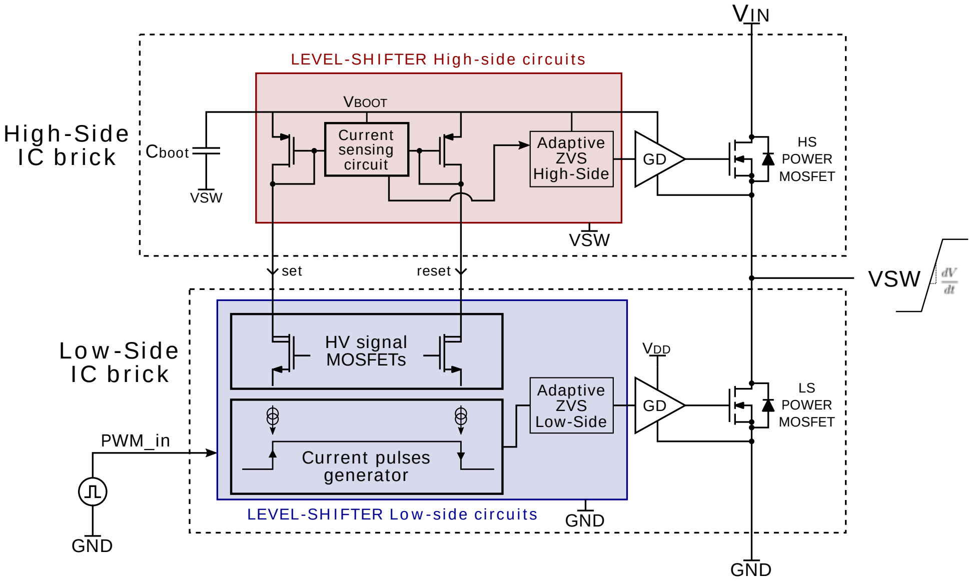


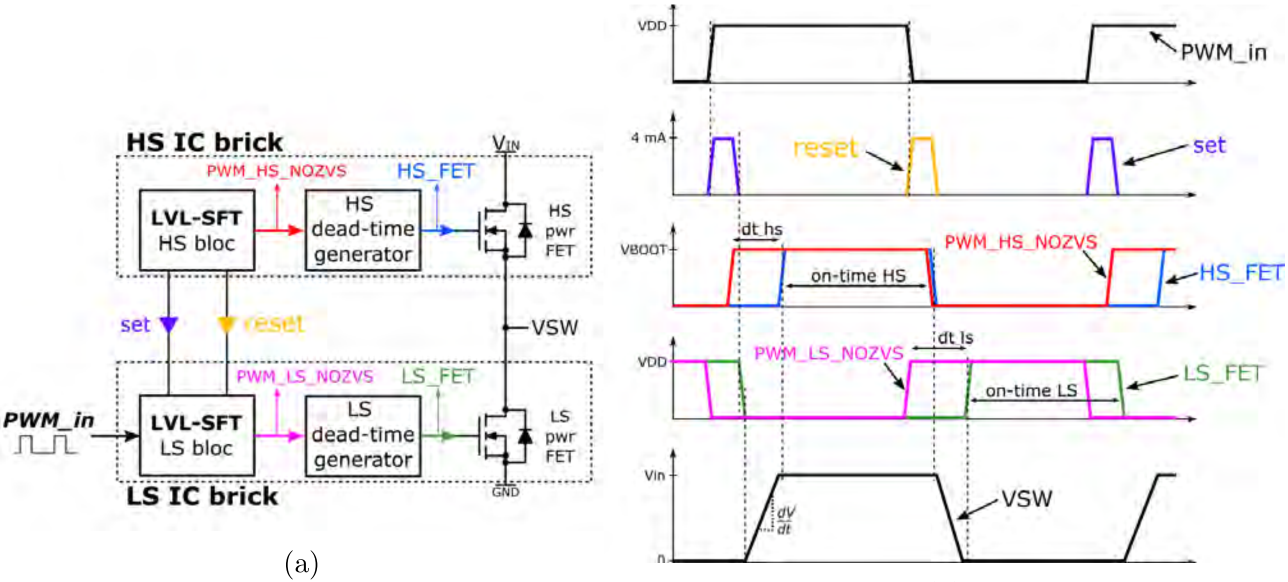
Figure 3.13: Simplified view of level-shifter's internal blocks

The role of this block is to transmit a signal from the low-side (PWM_in) to the high-side circuits. For this, current pulses are created on the rising and falling edges of the input signal. These pulses flow through the drain of the high-voltage signal MOSFETs (HV-FETs) shown in Figure 3.13. On the high-side, these currents pulses are detected and interpreted to reconstruct the original signal, except it is now referred to the switching node V_{SW}.

This type of circuits is often used to create a high-voltage level-shifter as in [56, 57]. It allows to decrease the energy required to transmit the information from the low-side to the high-side, as it limits the current sunk through the HV-FETs. Moreover, it does not require any external components to work, in contrary to expensive and bulky digital isolators or to some solutions that require an external high-voltage coupling capacitor [58].

Simulation waveforms in a 2L-AHBF configuration

In Figure 3.15(a) the main signals of the level-shifter block are highlighted and their simplified shape is shown in Figure 3.15(b) to present the selected switching strategy.



(a)

(b)

Figure 3.14: Level-shifters (a) connections ; (b) simplified waveforms in a 2L-AHBF configuration

To enhance the robustness of the level-shifter to dv/dt at the switching node, the selected strategy simply consists in sending the turn-on and the turn-off pulses outside of the transition time of V_{SW}. When transmitting the turn-on signal to the high-side, the low-side power FET (LS_FET) is kept ON to avoid that V_{SW} starts moving. No particular technique is implemented for the turn-off, as it is the reception of the turn-off on the high-side circuits that triggers V_{SW} fall.

On the rising edge of PWM_in, a current pulse is generated in the "set" branch, that is sensed on the high-side and interpreted as a signal to turn-on the local power FET. Note how LS_FET stays high during the "set" pulse, to keep V_{SW} to the ground level. Before the end of the pulse, the information is received on the high-side and stored in a latch (PWM_HS_NOZVS). At the end of the "set" pulse, LS_FET turns-off and V_{SW} rises due to the negative magnetizing current. The HS dead-time generator takes care of delaying the turn-on of the high-side FET to enable the ZVS mode. When V_{SW} reaches its high-voltage state (V_{in}), HS_FET turns-on.

On the falling edge of PWM_in, a current pulse is generated in the "reset" branch and interpreted on the high-side as a turn-off indication of HS_FET. The turn-on information of the low-side FET is received immediately (PWM_LS_NOZVS) but the low-side dead-time generator delays the actual turn-on of LS_FET to enable ZVS mode.

Figure 3.15 shows the waveforms from the simulation of the same signals, with a 2L-AHBF configuration operating at $V_{in} = 400$ V.

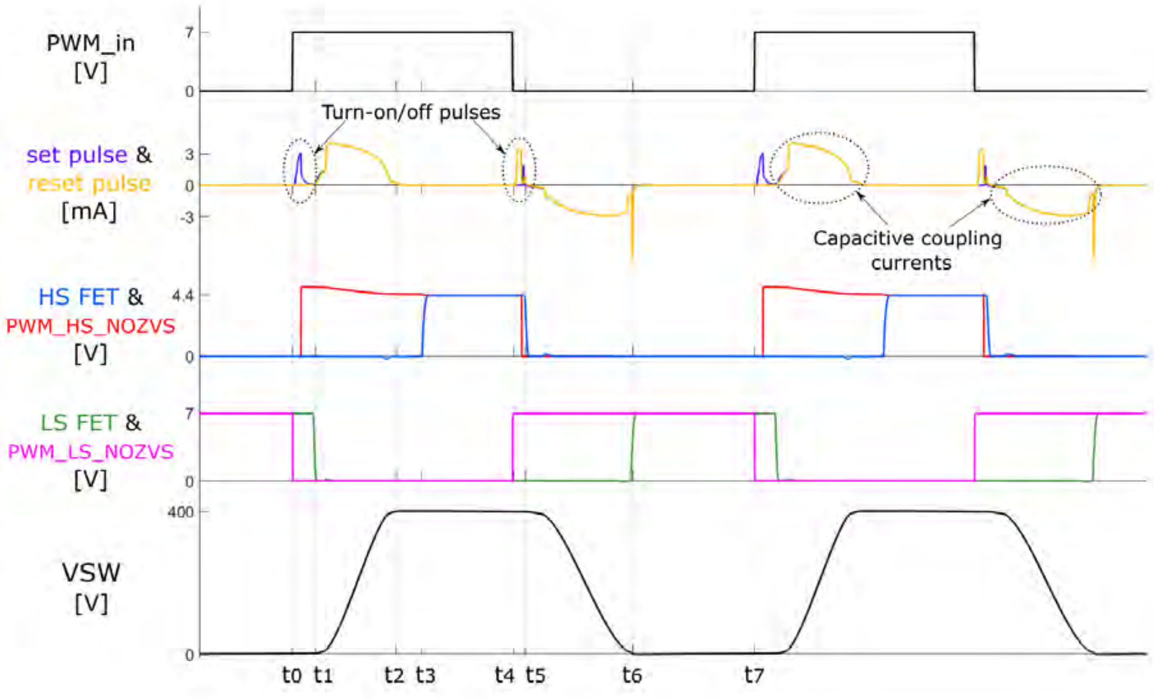


Figure 3.15: Simulation waveforms of level-shifters in a 2L-AHBF configuration

These results show that the control signals are very similar to what is expected. The low-side and high-side power switches can be controlled using a single PWM signal and a dead-time is generated to ensure the ZVS mode.

However, the waveforms of the current in the ”set” and ”reset” branches reveal that the turn-on/off pulses are short with respect to the current flowing through the same branches during the ZVS transitions. These currents are due to the charging and discharging of the parasitic capacitors connected between the low-side and the high-side level-shifter circuits. Most of the value of these parasitic capacitors is due to the output capacitor of the HV-FETs used in the low-side portion of the level-shifters, that needs to be (dis)charged when the drains of these HF-FETs move. In the next paragraphs, the currents generated during the ZVS transitions are designated as ”capacitive coupling currents”. During the rising phase of V_{SW}, their intensity (i_{cc}) can be roughly estimated as:

$$i_{cc} = C_{par} \cdot \frac{dV_{SW}}{dt} = 1.25 \text{ pF} \cdot 3.3 \text{ V/ns} = 4.13 \text{ mA} \tag{3.3}$$

Where C_{par} is the parasitic capacitance due to the HV signal MOSFETs output capacitor (C_{oss}) and dV_{SW}/dt is the slope of the switching node.

The computed value for these capacitive coupling currents seems to correspond to the value measured in simulation (4.1 mA maximum). Fortunately, the dv/dt at the switching node limited to few V/ns (due to the slow ZVS transitions) otherwise the capacitive coupling currents could be much larger.

A current pulse can also be observed at the turn-on of LS_FET (at t_6). It is due to the fact that V_{SW} did not exactly reach ground level before LS_FET turns-on, which generates a quick voltage variation and this current pulse. However, it could be easily removed by making the dead-time before LS_FET turn-on (dt_hs) slightly longer.

Overall, the simulation results validate the selected switching strategy as it allows to control the floating power switches using only a low-side PWM signal and it offers a robustness to the perturbations from common-mode currents generated during the ZVS transitions.

Delays and consumption

The transmission of the signal from the low-side to the high-side of the level-shifter is not instantaneous and a small delay appears between the rising/falling edges of the input signals and of the corresponding floating signals.

The simulation results reveal that the transmission delay is close to 18 ns for the turn-on information and to 20 ns for the turn-off. It is in the range of what can be expected from a 400 V level-shifter as shown in [57].

The power consumption associated to the level-shifter block can also be estimated using (3.4) used in [59]:

$$P_{lvlsft} = V_{DS\ max} \cdot i_{pulse} \cdot t_{pulse} \cdot f_{sw} \tag{3.4}$$

Where $V_{DS\ max}$ is the floating voltage (400 V), i_{pulse} is the current pulse value (about 3 mA), t_{pulse} is the pulse duration and f_{sw} is the converter switching frequency. For a 2L-AHBF operating at 400 V and 1 MHz, the consumption of the level-shifter is equal to 12 mW, which is low enough to not impact too much the overall converter's efficiency.

About the dead-time generators

As shown in Figures 3.13 and 3.14, a dedicated circuit is used on the high-side and the low-side to generate the dead-times required to enable the ZVS mode.

They have mainly two operating modes: "adaptive" or "externally tunable". In the "adaptive" mode, the capacitive coupling currents are sensed to detect the end of the ZVS transitions, which allows to turn-on the power MOSFETs when V_{SW} reaches its high (or low) voltage state. If the ZVS transitions become longer or shorter, the generated dead-time is automatically adapted. In the other mode, the duration of the dead-time transitions is set externally by placing a small capacitor between one of the IC brick input pins and the local reference. This capacitor is charged with a small current and it generates a constant dead-time (for a given capacitor value) that does not depend on the duration of the ZVS transitions.

The last mode is used to obtain results shown in Figure 3.15 which can explain why the turn-on of HS_FET is late and the turn-on of LS_FET is early (as V_{SW} did not exactly reached 0 V when it turns on, generating the current spike observed in the "set" and "reset" branches at t_6).

Level-shifters arrangement in a 3L-FC-AHBF configuration

There are several challenges regarding the implementation of the level-shifters in the 3L-FC-AHBF configuration. First, three floating switches are present in this configuration and they should be controlled using only two low-side PWM signals. Then, the HV signal FETs used inside the low-side level-shifters have a maximum drain-source voltage that is lower than the input voltage of the converter. It means that a single level-shifter cannot be used to transmit the PWM signal from ground level up to the top floating IC brick. The total number of level-shifter blocks required inside each IC brick must also be limited as each of them requires two bulky HV signal FETs that impact the size and the cost of the IC brick. Finally, the delays added by the various level-shifter blocks should not distort too much the PWM signals as it could lead to unequal on-time of the power FETs and to imbalance on the flying-capacitor voltage.

To overcome these difficulties, an arrangement of several level-shifter blocks to create the 3L-FC-AHBF configuration is proposed. It is presented in Figure 3.16 that shows the level-shifter blocks required at the various levels.

In the selected arrangement, there are two main paths in parallel, that are used to transmit the two PWM signals. The PWM signals travel through different level-shifter blocks and there is no ambiguity on the information received at the high-side level.

The technique employed to drive the high-side power FETs can be summarized as follows. Each PWM signal is first sent to the floating reference V_{SW3}. Then, it is transmitted to $S1$ or $S2$ through a second level-shifter block. Both level-shifter stages are built on the same principle as the one for the 2L-AHBF configuration shown in Figure 3.13.

However, due to the selected arrangement for the level-shifter, an imbalance in the turn-off delay of the low-side power MOSFETs is created. Indeed, the delay associated to $S4$ turn-off would be smaller than the delay for $S3$ turn-off, because for the last one, the PWM signal must first be transmitted from ground level to V_{SW3} reference level while for $S4$ the information is available immediately. This imbalance in turn-off delays could lead to a difference in on-time of the power FETs and in the end to an imbalance on the flying capacitor voltage. To solve the imbalance in turn-off delay, an "artificial" delay is added to $S4$ turn-off path (the block in dotted line in Figure 3.16). The duration of this delay can be set with a small capacitor placed on a dedicated input pin of the IC brick.

The simulation results of the proposed level-shifters arrangement in a 3L-FC-AHBF configuration operating at 800 V input voltage are shown in Figure 3.17.

They validate that the four power switches can be controlled using two low-side PWM signals. Like for the 2L-AHBF configuration, the dead-time of each switch can be set to operate in ZVS mode. Regarding the delay matching, notice how the phase-shift between $S1$ and $S2$ turn-off is equal to the one between the two PWM signals. For $S3$ and $S4$ turn-off, the phase-shift is almost the same as between the PWM signals, but not exactly equal (180.9° instead of 180°). It means the capacitor used to generate $S4$ artificial delay is slightly too big (a 20 pF capacitor was being used). A smaller value should be used for a better matching in the turn-off delays.

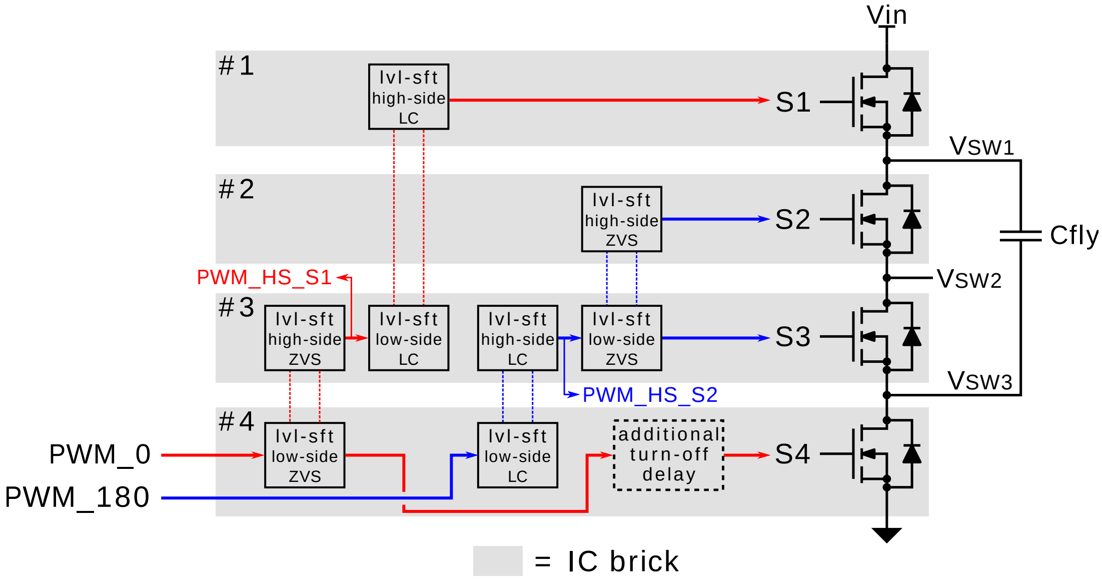


Figure 3.16: Selected arrangement of level-shifters in the 3L-FC-AHBF configuration

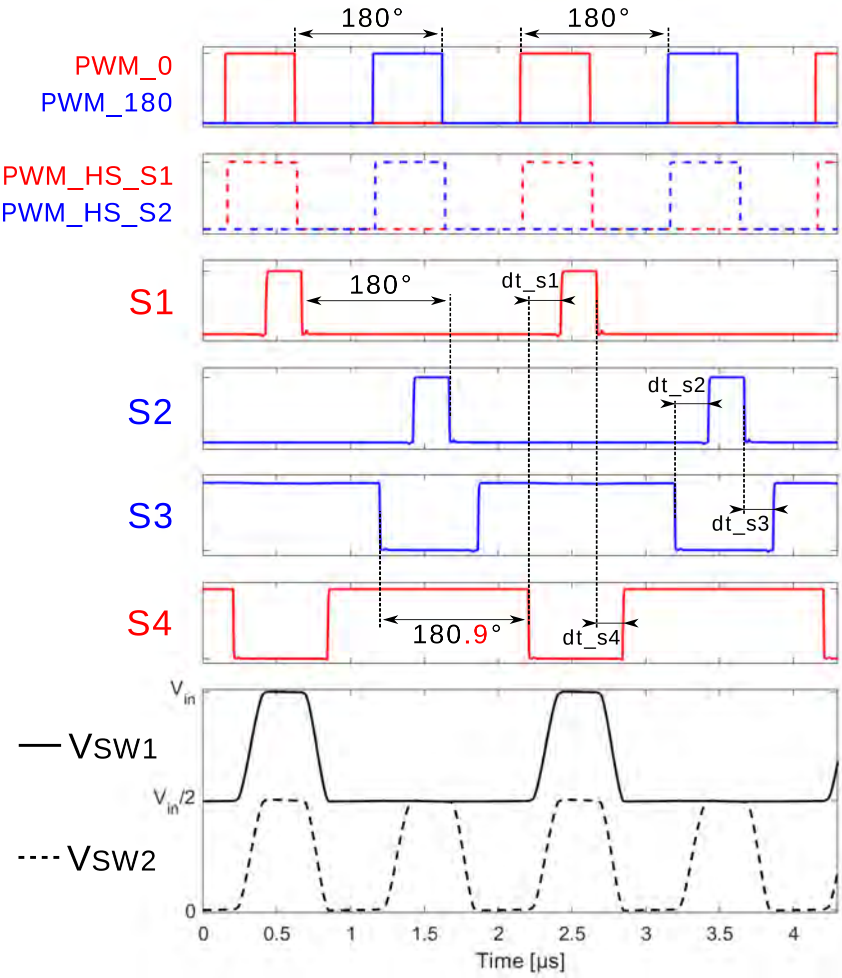


Figure 3.17: Simulation waveforms of level-shifters in a 3L-FC-AHBF configuration

Delays and HS-FETs minimum on-time

Like for level-shifters in the 2L-AHBF configuration, some delays are also observed in the 3L-FC-AHBF configuration for the signal going through the level-shifters. They are even larger since the low-side signal information must travel through two level-shifters to reach the high-side circuits.

For $S1$, the total delay that is observed between PWM_0 falling edge and the effective turn-off of the power switch is close to 52 ns. Note that this accounts also for the delays associated to the gate-driver stage, that were presented previously. For the turn-on, a similar delay should be observed (if not including the delay added by dead-time generator). Overall, the total delay for turn-on and turn-off of this power switch using a low-side signal is around 100 ns. A similar value is computed for the power switch $S2$.

To prevent any difficulties in driving the floating power-switches, it is decided to set a minimum to the on-time value. This value is "arbitrarily" fixed to be twice the total delay observed to drive the power switch, so 200 ns. The value for the minimum on-time could be refined with a more accurate set of specifications for the IC brick, but this value is used in first approximation to set a limit to the maximum switching frequency at which the IC brick can operate.

Note that for the LS-FETs, no minimum on-time value is assumed from the level-shifter constraints because a stronger constraint will appear for these power switches when considering the bootstrap circuit.

Experimental implementation and tests

To test the possibility to use the level-shifter to build the targeted power stage, it is implemented in a 2L-AHBF configuration. A photo of the board is shown in Figure 3.18. The two IC bricks are placed in two packages which are then connected to the board to allow them to communicate.

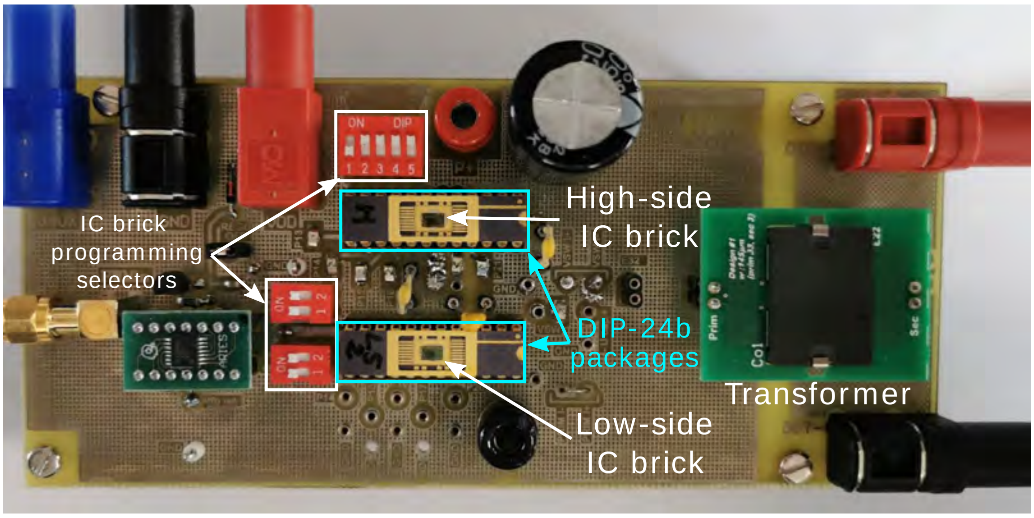


Figure 3.18: PCB for the practical implementation of level-shifter in a 2L-AHBF configuration

The measured signals are shown in Figure 3.19. The input voltage is limited to 40 V while the switching frequency is set to 60 kHz. The measured signals correspond quite well to those presented in Figure 3.15. The low-side PWM signal is correctly sent to the high-side IC before the low-side switch turns off, as shown in the zoomed portion of Figure 3.18. The same PWM signal is also used to drive the low-side power switch with a configurable dead-time. The measured delay to transmit the turn-on information from the low-side IC to the floating IC is 35 ns, while the delay for the turn-off is more important ($\approx$ 54 ns). The increased delays compared to simulation are probably due to the IC brick I/O filters and to the PCB/probe parasitic capacitances that were not taken into account in simulation.

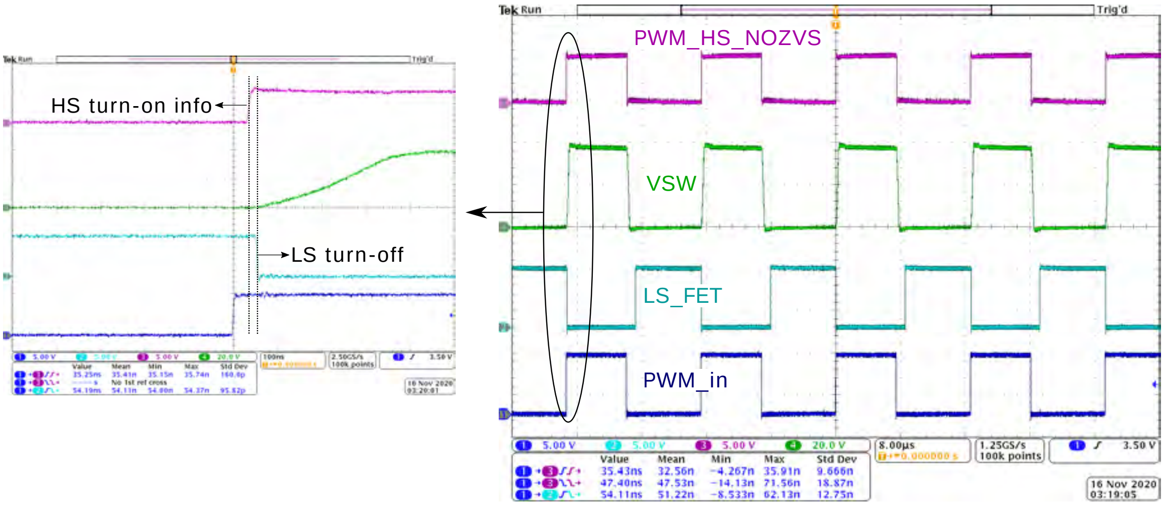


Figure 3.19: Measured waveforms for the tests of the level-shifter block at $V_{in} < 40$ V

However, a problem appears in the behavior of the level-shifter when the input voltage is higher than 40 V. Indeed, the waveforms in Figure 3.20 reveal that the turn-off information fails to be transmitted to the floating IC. As a consequence, the high-side power switch cannot be turned-off, which leads to a cross conduction in the half-bridge since both the high-side and the low-side power switches are on simultaneously (it explains why the middle switching node V_{SW} takes an intermediate value that is not 0 V or V_{in} but rather $V_{in}/2$). This could damage

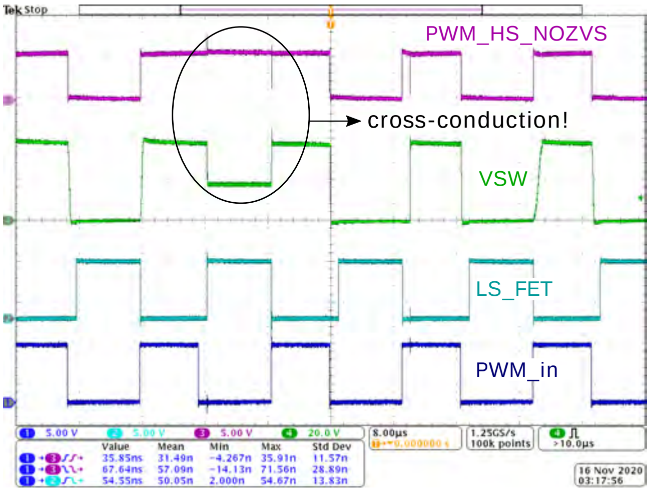


Figure 3.20: Measured waveforms for the tests of the level-shifter block at $V_{in} > 40$ V

the IC bricks (due to the high power dissipated in the power switch) and drastically reduce the converter's efficiency.

Unfortunately, the little amount of time left for the test-phase of the IC brick did not allow to solve the issue or to identify with certainty its origin. However, there are some leads that could explain the difficulty of the level-shifters to operate well when the differential voltage becomes too large. It could be due to a large parasitic inductance and/or capacitance added by the IC package and the PCB tracks. The level-shifter design and simulation were done with a lower value for the parasitic components (e.g. few nH for the parasitic inductance when it could be several tens of nH on the board used for the tests). Another potential explanation could be related to the design of the high-side portion of the level-shifter (that senses the current pulses) which may not be robust enough.

Solving this issue would require a re-design of the level-shifter block and a second silicon run, but time constraint on the PhD activity made both of these impossible. Another possibility would be to place the two IC bricks closer (ideally in the same package) to reduce the parasitics between them, to see if they can operate at high-voltage.

Due to the difficulties met during the implementation of the level-shifter in a 2L-AHBF configuration, its practical implementation in a 3L-FC-AHBF stage was not carried out. Moreover, due to the failure of the level-shifter for $V_{in} > 40$ V, this block cannot be used to control the floating IC bricks in the targeted high-voltage converter stage. Therefore, an alternative solution will be implemented with external components.

3.3.4 Active bootstrap

A floating supply is required to power the floating circuits (level-shifter, gate-driver, power switch). A common low-cost technique is the bootstrap method. It is cheaper than using an isolated DC/DC converter and it requires much smaller footprint. It is also more efficient than solutions that take the energy directly from the high voltage supply. The bootstrap technique is often used to create a floating voltage from a low-side low-voltage supply and it is used in several applications [60, 61], including multi-level converters [62, 63].

An example of how the bootstrap circuit included in the IC brick can be used to create a floating supply in a half-bridge configuration is shown in Figure 3.21. The low-side IC is supplied from an external voltage supply (V_{AUX}) and the same supply is used to power the high-side IC through the active bootstrap circuit.

First, the main blocks that compose the active bootstrap circuit included in the IC brick are described and its operating mode is detailed in a 2L-AHBF configuration. The challenges regarding the integration of this block in the IC brick are discussed. Then, the implementation of bootstrap technique in the 3L-FC-AHBF configuration is presented and some simulation results validate its functionality. Finally, the difficulties met during the measurements of this block are presented.

Main building blocks

Figure 3.21 shows how the active bootstrap circuit is connected in a 2L-AHBF configuration and presents the main blocks that are involved. The design of an active bootstrap circuit is targeted rather than using a simple diode (as it is the case in many designs) because it allows to increase the quantity of charges that can be transmitted to the floating supply. Moreover, it allows to avoid using HV-diodes that are prone to issues in HV bulk Silicon process (due to their intrinsic parasitic components that may affect the IC performances).

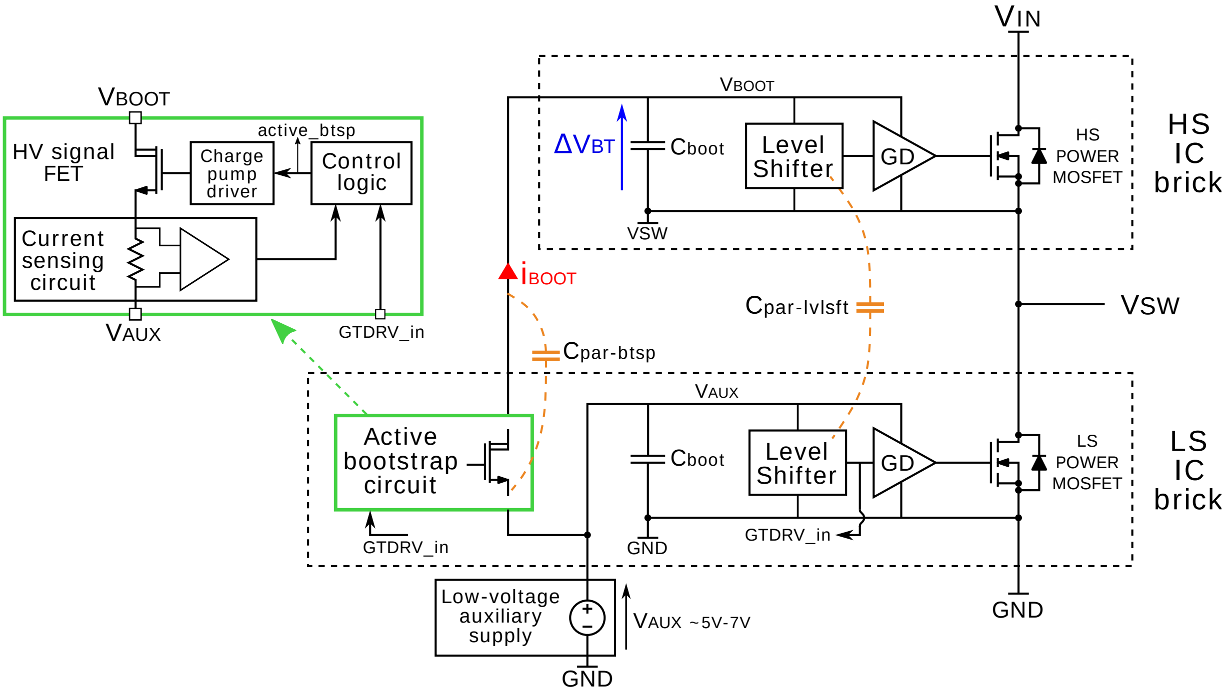


Figure 3.21: Active bootstrap connection in a half-bridge configuration and internal blocks

There are four building blocks included in the active bootstrap circuit. First, a HV signal FET (the same as the one used in the level-shifters). It must be high-voltage because the floating bootstrap supply is referred to the switching node, which may go up to 400 V in a 2L-AHBF configuration. In series with the HV-FET, a circuit is connected to sense the current flowing through the HV-FET drain. Its role is to control the HV-FET turn-off if the current starts to flow in the wrong direction (from V_{BOOT} to V_{AUX}) during the charging phase of the bootstrap. A "control logic" block is used to generate the signal to control the HV-FET, synchronizing it to the local power FET (using $GTDRV\_in$ signal) and taking into account the information received from the current sensing circuit. Finally, a charge-pump circuit is used to drive the HV-FET. It is required as the source of the HV-FET is connected to V_{AUX} so a higher voltage should be placed on its gate to be able to turn-it on.

On the floating side, a capacitor is used to keep a constant supply voltage (C_{boot}). It is usually an external component because it is difficult to integrate large capacitor with standard integration technologies. However, in the present case, the small size of the power MOSFET input capacitance ($\sim$ 100 pF) greatly decreases the amount of charges required to drive the gate. Therefore, the capacitance required on the floating IC brick may be reduced and so its integration in the IC brick is targeted. It would allow to reduce the bill of materials required to build the converter, although next paragraphs will show that it may be challenging to create a power supply with a constant voltage using only this integrated capacitor. The value of the capacitor included in the IC brick is evaluated in simulation and is close to 4.7 nF (while it already occupies a large portion of the IC brick).

Operating principle

To illustrate the challenges related to the active bootstrap integration, it is necessary to observe the variations of the floating bootstrap voltage over a switching period. Figure 3.22 shows the simulated waveforms of the bootstrap's voltage and current over a switching period in steady-state. The results are obtained in simulation for the 2L-AHBF power stage operating at $V_{in} = 400$ V and $f_{sw} = 1$ MHz. The auxiliary supply V_{AUX} is set to 7 V. The switching period can be divided in four steps that are highlighted in Figure 3.22 (next to the waveforms of the *active_btsp* control signal).

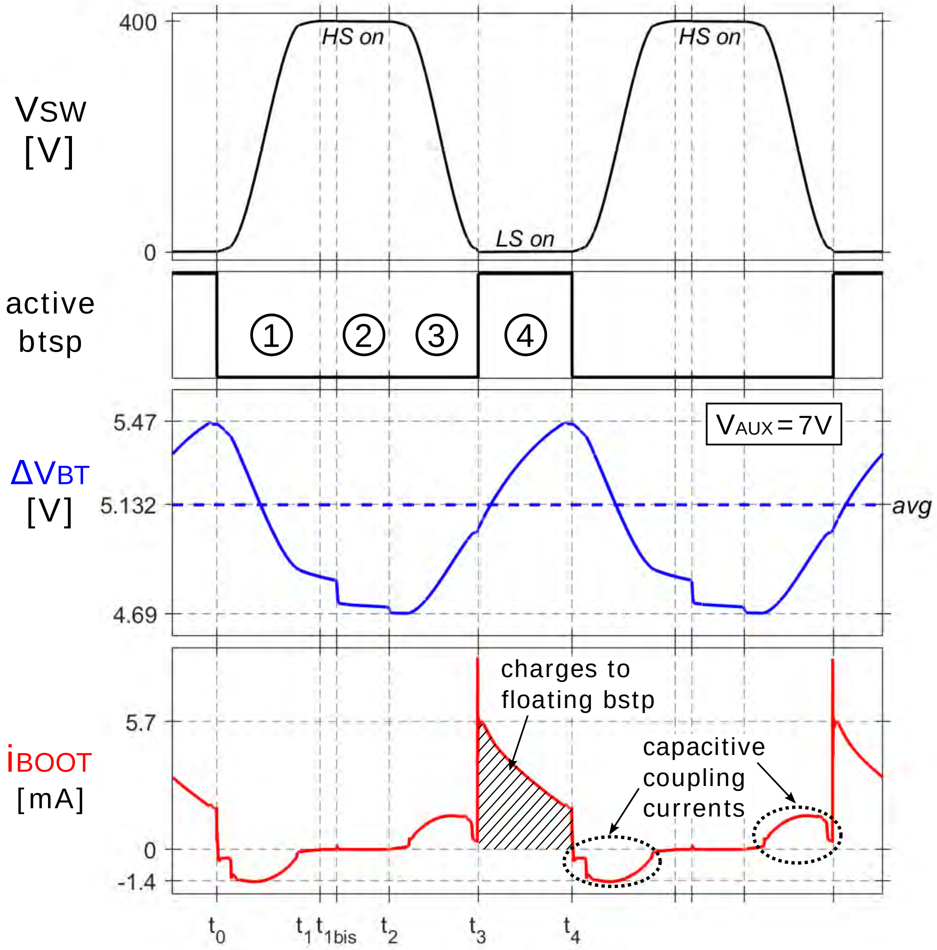


Figure 3.22: Simulation waveforms of the active bootstrap in a 2L-AHBF configuration

Mode ① - from t_0 to t_1

When the LS power FET turns off, it initiates a transition in the V_{SW} node due to the magnetizing current. The current flowing through the bootstrap HV-FET (i_{BOOT}) is negative in this mode due to the charging of the parasitic capacitor associated to the bootstrap HV-FET ($C_{par\ btsp}$ in Figure 3.21). For the voltage across the floating bootstrap capacitor (ΔV_{BT}), a large drop is observed during this mode. It is due to the capacitive coupling currents related to the parasitic capacitor of the bootstrap and the level-shifters ($C_{par\ lvlsft}$), that are indirectly connected to the node V_{BOOT}. The voltage drop that is observed on ΔV_{BT} during mode ① can be expressed as:

$$\Delta V_{BOOT}(t_1) - \Delta V_{BOOT}(t_0) = -\frac{\Delta V_{SW}}{C_{boot}} \cdot (C_{par\ btsp} + \alpha \cdot C_{par\ lvlsft}) \tag{3.5}$$

Where ΔV_{SW} is the difference between the low-voltage and high-voltage states of V_{SW}, $C_{par\ btsp}$ and $C_{par\ lvlsft}$ are the parasitic capacitors associated with the HV-FETs included in the bootstrap block and in the level-shifter block, respectively. The α factor is added to take into account that a portion of the current charging level-shifters parasitic capacitance ($C_{par\ lvlsft}$) is mirrored in the high-side block of the level-shifter and taken from the floating supply capacitor C_{boot} (therefore $\alpha > 1$).

Mode ② - from t_1 to t_2

In this mode, V_{SW} has reached its high-voltage state (V_{in}) and the HS power FET is conducting current (it effectively turns on only at $t_{1\ bis}$ but its body-diode conducts the current since t_1). Since V_{SW} is high, the voltage at V_{BOOT} node is much higher than V_{AUX} so the active bootstrap circuit is off and no bootstrap current circulates ($i_{BOOT} \approx 0$ mA). On the other hand, the floating bootstrap voltage still changes, due to the turn-on and turn-off of the HS power FET. It is possible to evaluate its voltage drop using the power FET input capacitance C_{iss} value that was roughly estimated from the gate-driver consumption measurements:

$$\Delta V_{BOOT}(t_2) - \Delta V_{BOOT}(t_1) \approx -\frac{C_{iss}}{C_{boot}} \cdot V_{GS} = -\frac{100\ \text{pF}}{4.7\ \text{nF}} \cdot 5.1\ \text{V} = -109\ \text{mV} \tag{3.6}$$

The value used for V_{GS} is the average value of ΔV_{BT} shown in Figure 3.22. The value found using (3.6) is close to what is observed in Figure 3.22 during this mode.

Mode ③ - from t_2 to t_3

The HS power FET turns off at t_2, which initiates another ZVS transition on V_{SW} node. This time, the current discharging the parasitic capacitances is charging the bootstrap capacitor (note how i_{BOOT} is positive). However, the current through the level-shifters parasitic capacitance ($C_{par\ lvlsft}$) is not mirrored when flowing in this direction. Therefore, the gain on ΔV_{BOOT} is lower than the drop observed during mode ①. The voltage difference on ΔV_{BOOT} in mode ③ can be expressed as:

$$\Delta V_{BOOT}(t_3) - \Delta V_{BOOT}(t_2) = -\frac{\Delta V_{SW}}{C_{boot}} \cdot (C_{par\ btsp} + C_{par\ lvlsft}) \tag{3.7}$$

Note that the α factor disappears because it is equal to 1. The minus sign on the right side of the equation is canceled by the negative value of ΔV_{SW} that travels from V_{in} to ground, so the voltage difference on ΔV_{BT} is indeed positive.

The value of the equivalent output capacitor of the HV signal FETs is estimated in simulation and is equal to 1.25 pF. Values of the parasitic capacitor of the bootstrap and the level-shifters are $C_{par\ btsp} = 1.25$ pF and $C_{par\ lvlfsft} = 2.5$ pF respectively. Using these values, the voltage difference on ΔV_{BOOT} computed using (3.7) is 0.32 V, which is very close to the voltage gain observed in simulation during mode ③ - that is equal to 0.33 V.

Mode ④ - from t_3 to t_4
When V_{SW} reaches ground, the LS power FET turns on. At the same time, the active bootstrap HV-FET is also turned on. Since the V_{BOOT} node is lower then V_{AUX}, the bootstrap current can flow from V_{AUX} to V_{BOOT}. It is however limited by the resistance between these two nodes that is due to the HV signal FET on-resistance and to the resistor used in the current sensing circuit (which value is close to 50 Ω) shown in Figure 3.21. The value of the HV-FET on-resistance is not easy to evaluate with accuracy (because the body-diode of this FET also conducts a portion of current), but it is very large due to the small size of the HV-FET. It can be roughly estimated around 300 Ω.

At the end of mode ④, the turn-off of the LS power FET also triggers the turn-off of the active bootstrap (i.e. of the bootstrap HV-FET) and a new switching period starts.

Challenges regarding the bootstrap circuits integration

The analysis of the voltage variations across the floating bootstrap supply revealed that they are quite significant (almost 800 mV over the complete switching period). This is due to the decision of using only the integrated bootstrap capacitor that is rather small (4.7 nF) compared to standard decoupling capacitor values (typically 100 nF). Moreover, the capacitive coupling currents observed during the ZVS transitions are quite important even though small-size HV-FETs are being used in the bootstrap and in the level-shifter blocks.

Moreover, the average value of ΔV_{BOOT} is lower than the voltage of the auxiliary supply (5.3 V vs. 7.0 V). The large voltage difference can also be explained by the small value of C_{boot} but not only.

First, the consumption of level-shifter circuits on the high-side is quite large because of the portion of the capacitive coupling current that is mirrored (and taken from C_{boot}) during mode ①.

Then, the on-time of the LS power FET is short, which limits the amount of time during which charges can be transmitted to the floating bootstrap. Combined with the high series resistance of the bootstrap HV-FET, it may explain why only a small voltage gain is observed during mode ④. The second reason is related to the voltage at V_{SW} node that significantly increases during mode ④ due to the negative current flowing in the primary side of the transformer that creates a voltage drop on the low-side power FET. For example, when $LS - FET$ turns off at t_4, the voltage measured at this node is $V_{SW} \approx 0.6$ V. This would limit ΔV_{BOOT} to maximum 6.4 V even if a much larger number of charges could be transmitted to the floating bootstrap capacitor.

To face these issues and allow the implementation of the active bootstrap circuit, several decisions were made.

For the practical implementation of the bootstrap circuit, an external capacitor is added in parallel to the internal bootstrap capacitance to create a more smoother bootstrap voltage.

Although the rest of the circuits was designed to cope with large variations of the supply voltage, the decision was made to increase the bootstrap capacitor to guarantee that the floating supply stays above the 3.0 V target (because the low-side IC brick voltage is limited to 5 V and because some additional parasitic capacitors might be added by the measurement probes, IC packages or the PCB tracks, etc.).

In addition, a minimum on-time is set for the low-side power FET to ensure the active bootstrap circuit on-time is long enough to generate a sufficient floating bootstrap voltage. Although no accurate evaluation of the influence of the minimum on-time on the bootstrap voltage was carried out, a 300 ns value is taken in a first approximation to ensure the average bootstrap voltage does not go below 3 V if V_{AUX} is limited to 5 V. This minimum on-time constraint is only used for the LS-FET in a 2L-AHBF stage.

Additional challenges and implementation in the 3L-FC configuration

In the 3L-FC configuration, there are three floating IC bricks that need to be supplied. The selected strategy is the cascaded bootstrap where each circuit supplies the floating circuit located just above, as in [63]. Like in the 2L-AHBF configuration, the low-side IC brick is supplied directly by an external low-voltage supply.

In addition to the issues encountered during the bootstrap implementation in the 2L-AHBF configuration, some difficulties are added for the 3L-FC-AHBF stage. The top IC brick cannot be directly connected to the low-side because the bootstrap HV-FET breakdown voltage is lower than the maximum voltage between their references (that is equal to V_{in}). Moreover, an increased quantity of parasitic capacitance is connected between the IC bricks: up to four level-shifter legs are connected between two IC bricks, leading to a larger voltage variation on the floating bootstrap voltage during the ZVS transitions.

Figure 3.23 shows the selected arrangement (cascaded bootstrap) to generate the bootstrap power supplies in the 3L-FC-AHBF configuration. The main interest of this arrangement is that it requires only one active bootstrap circuit inside each IC brick, since each IC brick powers only the IC brick located just above.

The arrangement is tested in simulation with $V_{in} = 800$ V, $V_{AUX} = 7$ V and $f_{sw} = 500$ kHz. In order to keep a more constant bootstrap voltage at the various level, an external 50 nF capacitor is added in parallel to each of the bootstrap capacitor (C_{boot}). Results are shown in Figure 3.24.

The constraint on the minimum on-time for the low-side power switches is implemented for the 3L-FC-AHBF stage as well, but under a slightly different form. In this configuration, the constraint is placed on the time during which both low-side FETs are on simultaneously (i.e. when V_{SW} is close to 0 V in Figure 3.24). For each half-period, this time should not be shorter than 300 ns to ensure a sufficient bootstrap voltage is created at $S1$ and $S2$ levels (ΔV_{BT1} and ΔV_{BT2}).

In these conditions, the simulation results show that a voltage larger than 3.0 V can be generated across all the bootstrap capacitors. The voltage on the IC brick at the top of the power stage (ΔV_{BT1}) is the lowest one but it remains close to 4 V. As expected, the larger bootstrap capacitor allows to smooth the floating voltages which value is more constant.

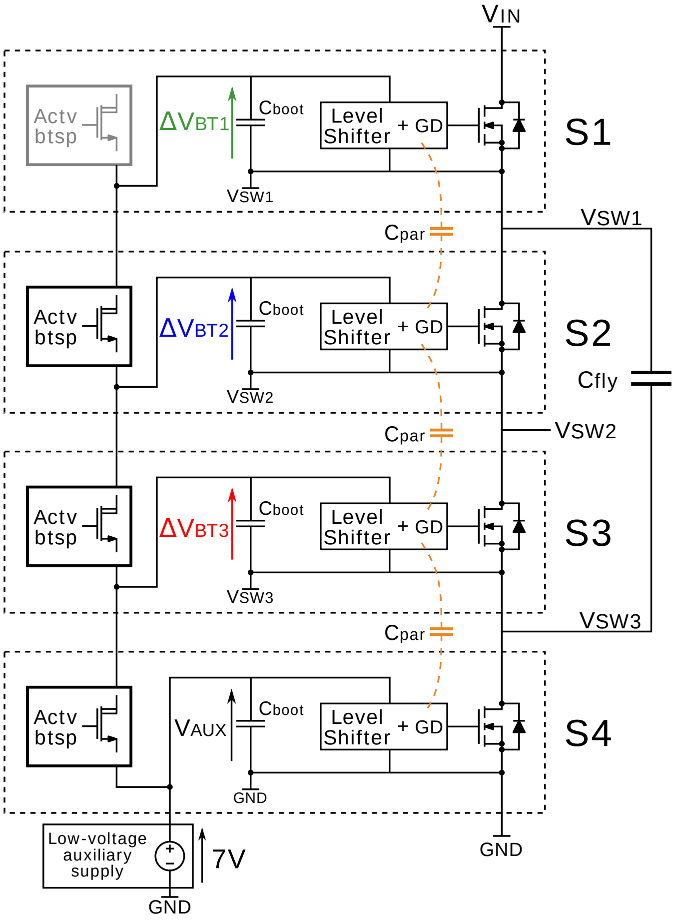


Figure 3.23: Bootstrap circuit connections in a 3L-FC configuration

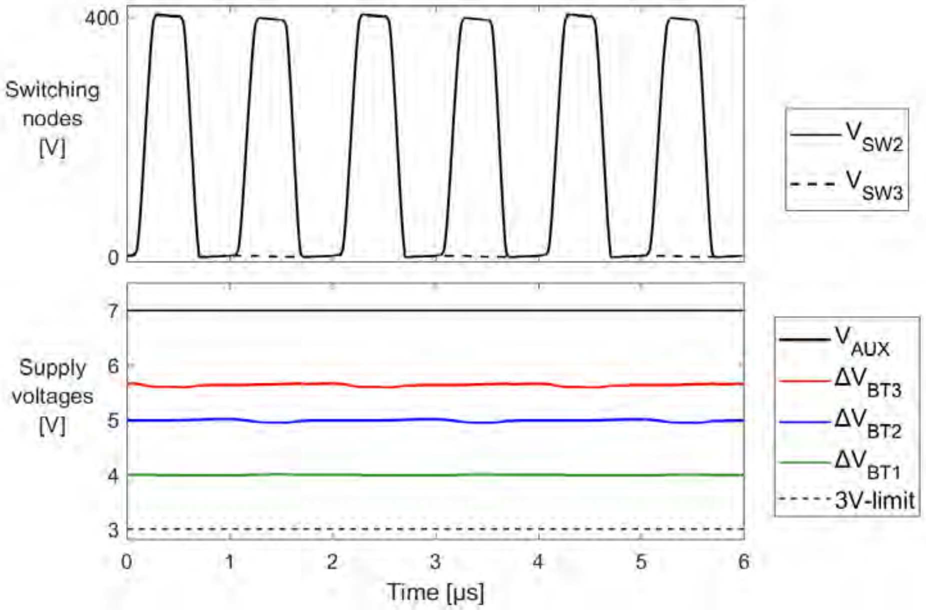


Figure 3.24: Simulated bootstrap supply voltages in a 3L-FC configuration

Difficulties in the practical implementation

The active bootstrap block is implemented in a 2L-AHBF configuration to measure the floating voltage generated. The level-shifter blocks are not used and digital isolators are used to replace them, which limits the auxiliary voltage V_{AUX} to 5 V. In order to maintain a constant bootstrap voltage on the floating IC brick, a large external capacitor (1 µF) is added in parallel to the integrated bootstrap capacitor. The input voltage is limited to 200 V in a first time and the switching frequency is set to 350 kHz.

To measure the floating bootstrap voltage, an active differential probe is used (TT-SI 9101) to improve measurements quality compared to measurements with passive probes.

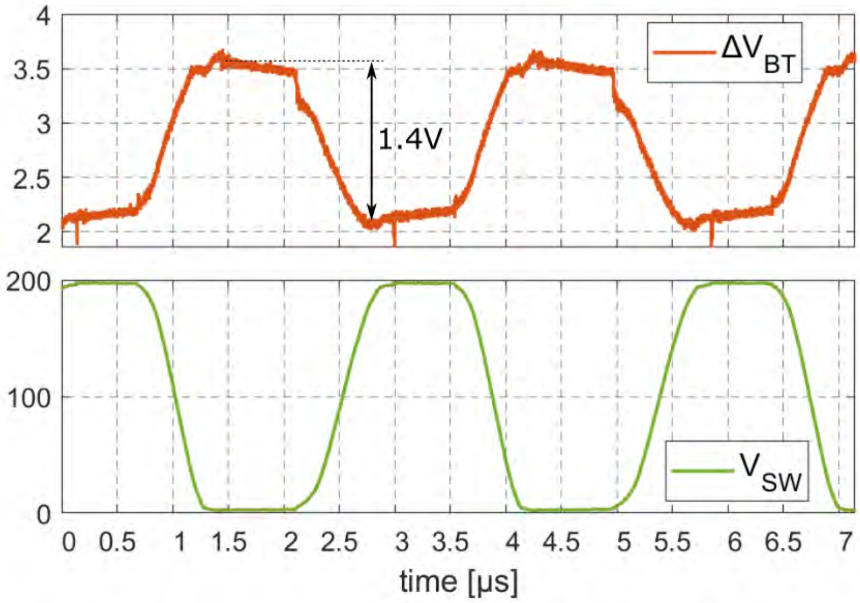


Figure 3.25: Measured bootstrap supply voltage waveforms in a 2L-AHBF configuration at $V_{in} = 200$ V

Figure 3.25 shows the voltage waveform measured across the floating bootstrap capacitor (ΔV_{BT}) and on the switching node (V_{SW}). For the last one, the waveform is very similar to those obtained in sim ulation, so it is reasonable to assume that the power stage operates as expected. On the other hand, the voltage waveform of ΔV_{BT} is not as expected. Simulation results showed that increasing the bootstrap capacitor (+50 nF) already allowed to flatten the bootstrap voltage, so with a 1 µF capacitor, it is expected to be almost constant. Yet, some large voltage variations are being measured (1.4 V peak-to-peak). These variations largely occur during the ZVS transitions of the switching node.

A possible explanation for these large variations is that they are due to the low Common Mode Rejection Ratio (CMRR) of the active probe. In the probe specifications, the CMRR at 50 Hz is about -85 dB while at 1 MHz it is only -50 dB. It means that for a 1 MHz excitation with a 200 V amplitude, the common mode that will be added to the measured value is close to 630 mV.

To measure the floating bootstrap voltage with more accuracy, probes with a better CMRR at high-frequency (like Tektronix IsoVu probes for example) should be used. But the parasitic capacitor of the probes would still be an issue. For example, each branch of the active probe used adds 7 pF to the switching node, so 14 pF total capacitor would be added, which is almost as big as the power switch parasitic capacitor ($C_{oss\ eq} \approx 19$ pF). Using these probes would prevent the power stage to operate in nominal conditions due to the impact they might have on the ZVS transitions.

Despite the large variations measured on ΔV_{BT}, the DC value can still be monitored, assuming that the impact of common-mode has no influence on the average voltage. The average voltage of ΔV_{BT} in Figure 3.25 is 2.78 V, which is lower than the targeted minimum value (i.e. 3 V). The floating bootstrap voltage appears to be smaller than the auxiliary supply ($V_{AUX} = 7$ V), the difference is even greater than what is observed in simulation (as shown in Figure 3.22). This large difference can be explained by the consumption of the digital isolator (about 1 mA) that is higher than the consumption of the floating IC brick. Moreover, the parasitic inductors added by the packages might also negatively impact the active bootstrap behavior, limiting the quantity of charges that can be transmitted (decrease in di/dt).

For all these reasons, no additional practical measurements were carried out on the bootstrap voltage. However, it was successfully implemented in the 2L-AHBF converter operating at 400 V as no changes were noticed in the overall converter performances when using the internal active bootstrap or an external bootstrap diode with a larger V_{AUX} (that ensures a $\Delta V_{BT} \geq 4.0$ V). For the 3L-FC-AHBF stage, the active bootstrap was not used as the low-side IC brick supply voltage limit (5 V) did not allow to create a sufficient bootstrap voltage on the floating IC bricks.

3.4 Conclusions on the design of the IC brick

An IC is designed to reduce the size of the selected power stage and the number of external components required. Due to the limitation of the HV bulk silicon process, the IC must be divided in several isolated dies to create the power stage. Therefore, an IC brick is designed to integrate the power switch together with its local control and supply, to allow the power stage to be controlled and powered by low-side signals. The low-power context of the converter allows to push integration further, to limit the number of external components required outside of the IC. The IC integrates several key blocks: a HV power MOSFET, the associated gate-driver, level-shifters, an active bootstrap circuit and a decoupling capacitor.

The design of the key blocks that compose the IC brick has been presented. The static and the dynamic characteristics of the power MOSFET were measured and the delays and the current consumption of the gate-driver were experimentally evaluated.

The operating mode of the level-shifter block was presented in a 2L-AHBF configuration. The arrangement of the level-shifters used to create the 3L-FC-AHBF was introduced and simulation results confirm that it can be use to control all the floating switches. However, the practical measurements on the level-shifters revealed a flaw in their operating mode (that might be related to the individual packaging of the IC bricks) which forbids to use this block to build the targeted high-voltage converter.

Finally, the active bootstrap operating mode was studied and the main challenges concerning the integration of this block (and of the bootstrap capacitor) were discussed. In particular, it appears that the value of the capacitor integrated inside the IC brick is to small to keep a constant floating bootstrap voltage. The selected method to generate the bootstrap voltage in a 3L-FC-AHBF configuration was introduced and validated through simulation. However, difficulties met during the practical measurements of the bootstrap voltage in a high-voltage power stage did not allow to fully validate the functionality of the block.

Overall, the simulation results in the 2L-AHBF and the 3L-FC-AHBF configurations confirm that the IC brick can be used to create the converter power stage with the targeted integration level (i.e. using only a low-side auxiliary supply to power all the IC bricks and one/two low-side PWM signal(s) to control all the power switches).

Perspectives for a second silicon run

Although there was not enough time or resources for a second silicon run, it is interesting to discuss how a re-design of some of the key blocks of the IC brick might improve its performances.

For the power switch or the gate-driver, no major default was identified during these initial measurements. However, the size of the FET could be reconsidered to reduce the size of the parasitic capacitors.

The level-shifter block could be improved on several aspects. First, the robustness against the parasitic inductors/capacitors should be increased, to avoid the issue of missed pulses revealed during the experimental tests for high V_{in} values. For this, it could be interesting to increase the immunity to the fast variations of the middle switching node. Then, the consumption of the block could be reduced, in particular the quantity of parasitic current mirrored during the ZVS transition should be limited.

For the active bootstrap circuit, a study could be done on the sizing of the high-voltage signal FET to find the optimal size for which the maximum bootstrap voltage is created. The variations of the bootstrap voltage should also be reduced, changing for example the node on which the drain of the HV signal FETs is connected during the ZVS transitions (like V_{SW} instead of V_{BOOT}). If these variations were sufficiently reduced, then the internal bootstrap capacitor could be used without requiring any external capacitor, which would allow to decrease the components count.

Chapter 4

Design of a transformer for HVLP converters

This chapter describes the design methodology used to create a transformer suitable for a HVLP converter operating at high frequency.

First, the limits of some of the existing approaches to design transformers are presented and the selected approach, based on a Design of Experiment (DoE), is introduced. The technological choices made at an early stage of the transformer design are listed. A simple model of the converter created to guide the transformer design is quickly described.

Then, the influence of some important design parameters is revealed and their selection is discussed. In particular, the optimization of the value of the primary inductor and of the transformer turns ratio is presented. The selection of the number of turns of the transformer winding and their arrangement on the PCB layers are also discussed.

Finally, the various designs of transformer selected during the DoE creation are regrouped in different families, depending on their targeted operating frequency. The measured value of the transformers important characteristics are summarized and a "map" of the DoE is created.

4.1 Selected approach for the transformer design

4.1.1 Introduction to the selected approach: Design of Experiments

The transformer is a key component of isolated DC/DC converters, as it largely impacts the performances but also the solution's size, since it is usually the bulkiest component of the converter. To improve the size/performances trade-off, the transformer must be carefully designed, taking into account the particularity of the HVLP application. The concerns met by the design of such component will prove to be quite different than those usually encountered in more "standard" designs, with a lower voltage or a higher power.

The design of a transformer is a complex problem: due to the various technologies, magnetic materials, windings types, etc. that can be selected to build the transformer. It is not possible to explore manually the complete design space, so finding an optimum design for the transformer can be challenging. Many different approaches can be used for the Transformer Design Optimization (TDO) problem.

Analytical approaches use a set of equations related to the operating mode of the transformer to find an optimal design [64, 65]. For example, the "area product" expression can be used to find an estimation of optimal size of the transformer required, depending on the specifications. However, this type of approach relies on the optimization of several constraints that are not significant in the HVLP context. For example, the maximum current density is often used to predict the size of the transformer windings. However, in the present case, due to the low currents, the size constraint of the transformer winding will rather guided by the minimum achievable size for the windings than by the current density inside of them.

To push the transformer design optimization forward, methods based on the use of iterative algorithms were developed. Geometric programming [66], genetic algorithms [67] or other approaches base on the use of artificial intelligence allow to explore more efficiently the design space and to find solutions optimizing one or few criteria. For example, the cost, the mass or the total losses of a transformer design can be defined as a target to be minimized by the algorithm. However, these approaches rely on a model of the transformer to optimize one or several of its aspects. But building an accurate model of the transformer to evaluate with precision its characteristics and its losses is not easy, such that it is not certain that the optimal solution found with these approaches is really the best one. To improve the model's accuracy, 2D or 3D FEM simulations can be used [68] but this solution is time consuming, so it is not suitable to evaluate a large number of designs.

In order to adapt the approach of the transformer design to the HVLP context, the impact of the important design parameters should be analyzed considering the particular operating mode of the transformer under design.

The approach used in this work is based on a "Design of Experiments" (DoE). It focuses on a limited number of parameters, which limits the number of possible solutions, monitoring the interaction and the influence of these parameters on the performances of the transformer. [69] used the DoE method to get an accurate model of a planar transformer winding parasitics. Here, the objective of the DoE is to build several transformer designs to find the most interesting solutions to create the HVLP converter with the best performances. The performances used to compare the designs are the size of the transformer and the converter's efficiency.

Although the DoE developed here does not use the same precision to "code" the different parameters, it is build with on a similar principle, that is to study the variations a several parameters independently. Selecting a discrete number of values for each parameter, it is possible to analyze their impact on the transformer characteristics and performances.

Since the objective of the DoE is to focus on a limited set of design parameters, some simplifications must be made in the design approach. Some aspects of the transformer design are therefore not studied in this work, like the thermal constraints - although it can be justified due to the low power context - or the EMI performances - for which shields are sometimes added between transformer windings - etc. In addition, some technological choices are made *a priori* (they are presented in the next section).

For most of the design parameters taken into account in the DoE, there is not a clear optimal solution that can be found. For these parameters, several values/variations can be taken into account and integrated to the DoE. Therefore, the results of the transformer design phase should not be a single optimal solution, but a short-list of interesting designs that should then be tested inside the DC/DC converter.

As highlighted in Chapter 2, the transformer current and voltage waveforms in a 2L-AHBF converter and in a 3L-FC-AHBF should be very similar. Therefore, only the design of the transformer for a 2L-AHBF operating at 400 V is considered in this analysis, since the 3L-FC-AHBF stage working at 800 V with the same transformer should lead to similar performances.

4.1.2 Technological choices

To decrease the number of possible solutions for the transformer design, some technological choices are made at the beginning of the transformer design phase, based on the low-cost, small-size and high-efficiency constraints.

The planar transformer based on the multi-layer PCB design is selected as it offers some interesting perspectives. First in terms of cost, as the windings of the transformer are created by PCB tracks that can be placed directly on the same board as the other converter's components. Planar transformers also present some interesting characteristics about easy replicability. Finally the tracks designed on PCB offer decreased losses at high-frequency, due to the limited impact of the skin effect [70].

The number of layers composing the multi-layer PCB is also limited in a low-cost perspective. In the present case, four-layer PCB designs are selected, because they are the most typical types of multi-layer PCBs. An illustration of a typical solution using these constraints is shown in Figure 4.1, although the layer distribution and the type of planar core will be different. In addition, the minimum track width and the minimum distance between two consecutive tracks are both limited to 100 µm. This constraint is similar to the standard capabilities of the PCB manufacturers to stay in-line with the low-cost perspective.

The geometry of the planar core is also selected at the beginning of the design phase. The

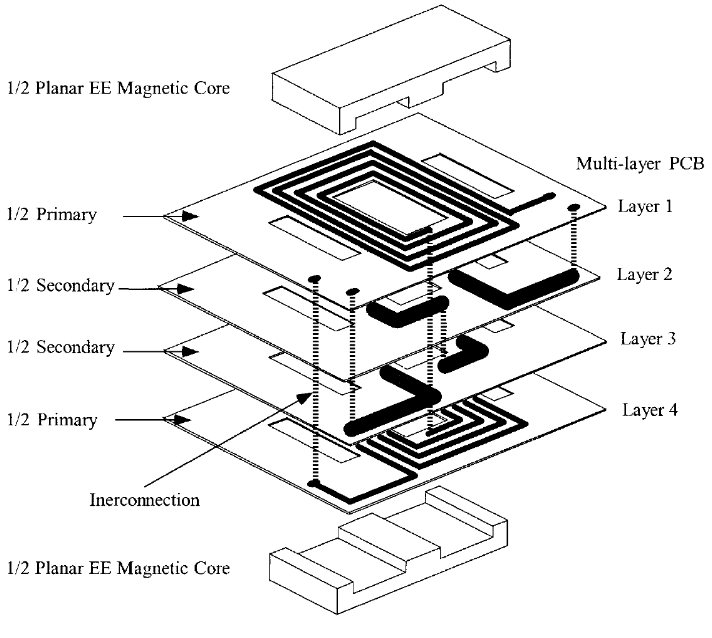
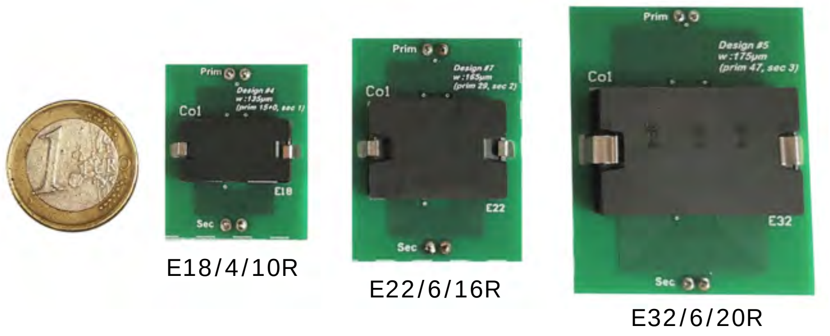


Figure 4.1: Exploded view of a planar transformer built from a multi-layer PCB [71]

standard planar E-cores seems to be the most interesting choice [70], because of their large core cross section that is useful to decrease the flux density and the core losses (compared to planar core with round center leg like ER core). To go further, the E+PLT core arrangement is selected to decrease the core volume and thus the losses. It does not impact the multi-layer PCB design since the height of the winding window for the E+PLT arrangement is higher than the standard PCB thickness (typically 1.6 mm).

Three different core sizes are selected for the E+PLT core arrangements, that are expected to show three interesting trade-offs between size and performances of the solution. The references of the selected planar E-cores from Ferroxcube are: E18/4/10R, E22/6/16R and E32/6/20R and the size of the transformer design using these different cores is shown in Figure 4.2.



E18/4/10R E22/6/16R E32/6/20R

Figure 4.2: Transformers built using the selected E-core references

Finally, the choice of the magnetic materials used for the E-core is also done at the early stage of the transformer design. MnZn soft ferrites are selected because of their low magnetic losses in the targeted frequency band that ranges from few hundreds kHz to few MHz. Three different materials are selected to be included in the DoE: 3F36, 3F4 and 3F46. The choice of the core material for each design is further discussed in Section 4.2.7.

4.1.3 Description of a simple model of the converter

A simple model of the converter is built to help validate the analytical considerations done for the power-stage and to evaluate quickly different solutions for the transformer design.

There are few reasons for creating a custom model instead of using an existing one or classical circuit simulation tools. First, the custom model can be adapted to the particularity of the High-Voltage Low-Power conversion, that is not the case for many existing models, more effective for high-voltage high-power designs or for low-voltage low-power designs. Second reason is the model should gather different types of losses that the circuit simulation tools do not always integrate: the core losses for example are rarely computed with accuracy in these tools.

Moreover, it is possible to quickly compare a large number of different designs using this type of approach. It can be used to monitor the impact of a specific parameters on the performances etc.

The simple converter's model is based on two main axes. One is the estimation of the converter's performances: the model computes the main losses inside the converter and evaluates the efficiency. The second is a routine that tends to optimize the primary inductance value (L_{pri}) depending on the switching frequency. Motivation and methodology for this optimization are discussed in section 4.2.2. The main steps composing the simple model are shown in Figure 4.3.

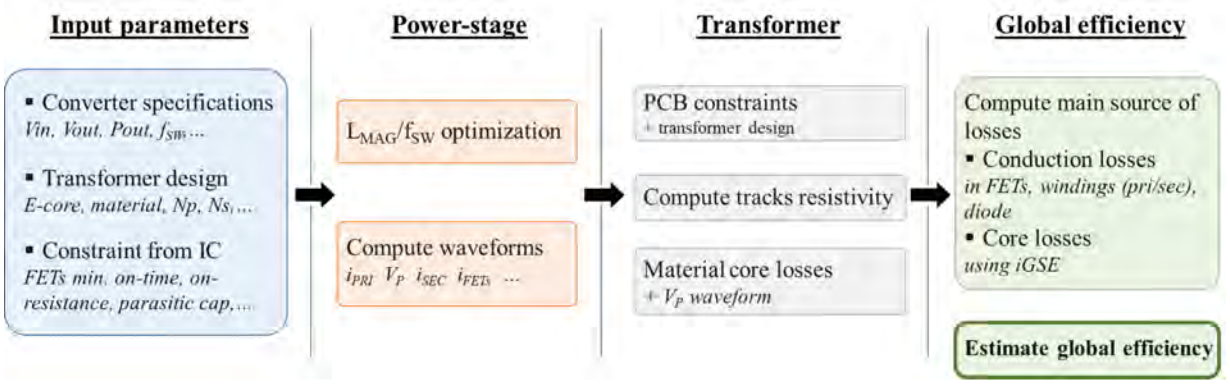


Figure 4.3: Simplified diagram of the converter model

1. **Input Parameters**

   The model takes different types of parameters as inputs. The main specifications of the converter (input and output voltages, output power, switching frequency, ...) are one type. Some information about the transformer design are also transmitted to the model: the core geometry and its material, the number of primary and secondary turns, and the estimated value for the mutual parasitic capacitor (C_{ps}). Finally, the information regarding the constraints of the IC brick are also given to the model - mainly the power MOSFET characteristics (on-resistance, output capacitor) and its minimum on-time.

2. **Power stage**

   The power stage computation phase relies on the calculation of the main converter waveforms. Using the converter main transfer function, it computes the combined evolution of the primary current and the primary voltage (as described in chapter 2) over several switching periods to reach a "steady-state". For a given primary inductance/switching frequency couple, the model concludes on the possibility to operate the targeted conversion ratio while keeping the ZVS mode. Once the inductance/frequency couple is determined, the model also computes the current in the transformer secondary and in the power MOSFETs. Note that the model computes the magnetizing current waveforms and not the primary current, due to the difficulty to evaluate the shape of the secondary current. But it is a reasonable approximation as the RMS primary current and the RMS magnetizing current values are close.

3. **Transformer**

   The model computes the DC-resistance of the windings of the transformer, using the input parameters and the constraints coming from the PCB manufacturers (number of layers, copper tracks width/isolation etc.). The AC-resistance is estimated as well, although its calculation is not accurate, as independent of the frequency (a constant factor $F_r = 1.1$ is used). Finally, the losses inside the magnetic core are computed, using the primary voltage waveform, the Steinmetz coefficients (specific to the material considered and revealed in Appendix D) and the iGSE (improved Generalized Steinmetz Equation [72]).

4. **Estimated efficiency**

   The model gathers all the information on the design to compute the different losses occurring inside the converter. The core losses are directly those computed for the transformer in the previous step. The conduction losses for the windings and the power MOSFETs are computed using the RMS value of the current flowing through these elements and their estimated resistance value. The secondary diode is assumed to have a constant voltage drop, which allow to easily compute the conduction losses in this component. Finally, the estimated efficiency is evaluated during the last step of the routine, taking into account the different types of losses enumerated. The results are computed for the 2L-AHBF power stage operating at 400 V, but a simple formula can allow to evaluate the performances of the 3L-FC-AHBF operating at 800 V taking into account the losses dissipated in the additional power switches (the formula is given in Appendix B). Note that the model does not take into account the power required to supply the active parts of the power stage. Although their power consumption should not be large, this limits the accuracy of the model.

To illustrate the model outcomes, the results obtained using a E22 core made with 3F4 material are shown in Figure 4.4. The estimated efficiency is plotted for a large frequency range (300-1000 kHz) and the number of primary turns varies from 10 to 50 - that is the maximum number of turns it is possible to achieve around a E22 core, given the manufacturing constraints of the PCB. The number of secondary turns (N_{sec}) is selected to keep the turns ratio close to the optimal value ($N_{tr} \approx 15$, this choice is discussed in a later section) depending on the number of primary turns ($N_{sec} = 1$ for left plot, $N_{sec} = 2$ for middle plot and $N_{sec} = 3$ for right plot). The results shown are for a 2L-AHBF operating with a 400 V input voltage.

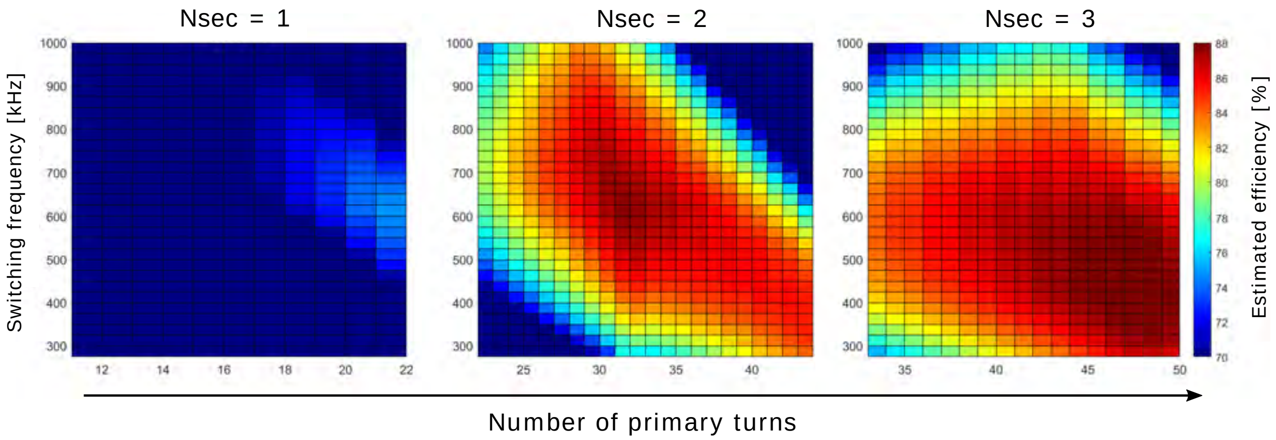


Figure 4.4: Estimated efficiency for a E22 core in 3F4 with $V_{in} = 400$ V

4.2 Influence of the main design parameters

Now that the selected approach for the transformer design was presented and the tool used to help exploring the design space was introduced, it is possible to study the influence of several parameters on the performances of the transformer.

The parameters for which an optimal value can be found are not directed included into the DoE but their optimization is discussed. For the parameters for which there is not a clear optimum, few variations are included into the DoE, to evaluate their influence on the transformer performances.

4.2.1 Example of a planar transformer design

To explicit the selected approach and illustrate the design choices, the important characteristics of a transformer designed during this phase are listed in Table 4.1.

Table 4.1: Characteristics of a transformer designed for HVLP converters

Design parameters		**Measured parameters**	
E-core size	E22 + PLT	DC r_{pri}	13.9 Ω
Core material	3F4 (MnZn)	DC r_{sec}	0.09 Ω
Primary turns N_{pri}	29 (15+14)	F_r^* at f_{opti}	1.06
Secondary turns N_{sec}	2	max. L_{pri}	2.55 mH
Turns ratio N_{tr}	14.5	C_{ps}	11 pF
Estimated f_{opti}	700 kHz	min. SRF**	0.91 MHz
Estimated L_{opti}	800 µH	$C_{self\ p}$	12 pF

* Value obtained in simulation using 3D-FEM tool

** Self Resonant Frequency measured on primary for the maximum L_{pri} value

The characteristics of the selected transformer are divided in two types: the design parameters and the measurement parameters. The design parameters illustrate and represent the choices that were made during the design phase. Their selection is discussed in the next paragraphs. On the other hand, the measured parameters represent the characteristics which value is particularly important for the behavior of the transformer inside the HVLP converter.

This design (identified as design #1 in the next paragraphs) is just one of the interesting designs that was selected during the elaboration of the DoE. It is used during this section as an example to illustrate the design choices.

4.2.2 Optimization of the primary inductance value in ZVS mode

In order to decrease the conduction losses due to the parasitic resistances located on the primary side of the converter, the RMS value of the primary current must be reduced. For this, it is possible to increase the primary inductance value to decrease the primary current ripple. However, the analysis of the ZVS mechanism conducted in Chapter 2 revealed that a minimum quantity of primary current is required to operate the ZVS transitions. So an optimal value of the primary inductance can be found that allows the power stage to operate in ZVS mode while mitigating the conduction losses.

In [51, 52, 53], an analytical expression is used to determine the optimal primary inductance value for the 2L-AHBF power stage. But it is only valid under some assumptions: constant switch's output capacitor, short duration of the ZVS transitions and constant ZVS current. In the HVLP context, these assumptions are not verified anymore so the same expression cannot be used. Therefore, a solution found is to determine the magnetizing inductance more accurately is to use an "optimization routine". This routine is included in the simple converter model presented earlier.

The routine is built using a MatLab script that computes the combined evolution of the primary current (i_{pri}) and the primary voltage (V_{pri}) over the switching period. The ZVS transitions are cut in small fractions of time ($<$ 1 ns), such that the current and the voltage behavior can be described linearly with accuracy. The equations used to determine their combined variations are the ones found during the power stage analysis in Chapter 2 (Equations (2.4) and (2.6)). This approach allows to describe with more accuracy the long ZVS transitions observed in low-power mode, as the variations of the switches output capacitor (C_{oss}) with the voltage are also taken into account (using a piece-wise linear model).

But the primary inductance's optimal value depends on many parameters, like the input voltage, the output power, the operating frequency of the power stage or the value of the parasitic capacitors. If the two first can be considered constant in a first approximation (if the design focuses on the nominal operating point of the converter), the last two can still change, as the frequency is one of the design parameters explored in this phase and the parasitic capacitors largely depend on the transformer design. Depending on the selected frequency, for a constant quantity of parasitic capacitor, the optimal value of the primary inductance will change as shown in Figure 4.5.

Results are obtained using the simplified model and they validate the evolution of the minimum primary current with the frequency highlighted in Chapter 2. Once the targeted operating frequency is chosen, the "optimal" value of the primary inductance can be found: for design #1, the targeted frequency is 700 kHz which leads to an optimal value of the primary inductance close to 800 µH.

Regarding the practical implementation, the value of the primary inductance is set by the air-gap added to the magnetic circuit that allows to decrease the inductance value. So the optimal value targeted should be smaller than the "maximum" inductance value that depends on the core material and the number of turns that is obtained when no air-gap is added, which is the case for design #1 since the maximum primary inductance value measured for a 3F4 core is close to 2.55 mH.

4.2.3 Selection of the transformer turns ratio

The transformer turns ratio (N_{tr}) also plays a role in the determination of the primary current, as it influences the power switches' on-times and the maximum time left for the ZVS transitions. The transformer's turns ratio is defined as:

$$N_{tr} = N_{pri}/N_{sec} \tag{4.1}$$

Its main impact on the converter is to set the effective duty-cycle (D_{eff}) required to obtain the targeted output voltage. The expression that links the effective duty-cycle and the turns ratio is the converter's main transfer function, revealed in Chapter 2 in Equation (2.38). If the value of the leakage inductor is small when compared to the magnetizing inductance, the formula can be rewritten as:

$$D_{eff} \approx \frac{N_{tr} \cdot (V_{out} + V_D)}{V_{in}} \tag{4.2}$$

The relations between the effective duty-cycle and the actual on-time of the power switches can be expressed as:

$$D_{eff} \cdot T = t_{on\ HS} + \frac{dt_{HS} + dt_{LS}}{2} \tag{4.3}$$

$$(1 - D_{eff}) \cdot T = t_{on\ LS} + \frac{dt_{HS} + dt_{LS}}{2} \tag{4.4}$$

Where T is the switching period, $t_{on\ LS}$ and $t_{on\ HS}$ are the actual on-times for the low-side and the high-side switches, respectively. dt_{HS} and dt_{LS} are the dead-times associated to the ZVS transitions of the high-side and of the low-side FET, respectively.

In these expressions, for a given switching period, the time left for the ZVS transitions is limited by the effective duty-cycle and the on-time of the power switches. Since the value of the effective duty-cycle is determined by the converter's main parameters (V_{in}, V_{out}, N_{tr}), it is

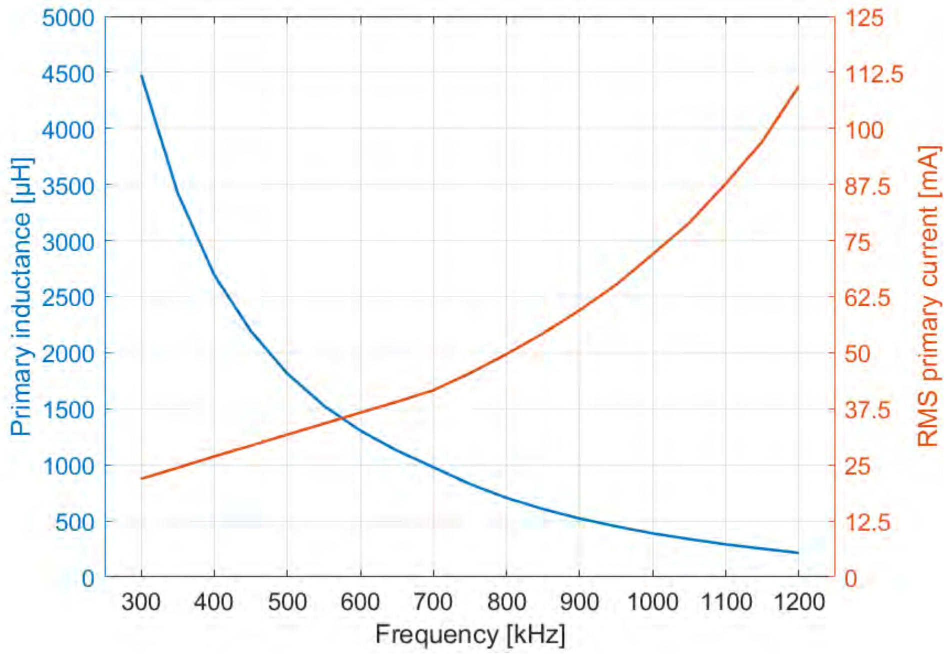


Figure 4.5: Evolution of minimum $i_{pri\ RMS}$ and optimal L_{pri} with f_{SW}

possible to write the constraints for the duration of the ZVS transitions related to the high-side and the low-side switches as:

$$max(\frac{dt_{HS} + dt_{LS}}{2})_{HS} = N_{tr} \cdot \frac{V_{out} + V_D}{V_{in}} \cdot T - t_{on\_min\_HS} \tag{4.5}$$

$$max(\frac{dt_{HS} + dt_{LS}}{2})_{LS} = (1 - N_{tr} \cdot \frac{V_{out} + V_D}{V_{in}}) \cdot T - t_{on\_min\_LS} \tag{4.6}$$

Where $t_{on\_min\_HS}$ and $t_{on\_min\_LS}$ are the minimum on-times of the low-side MOSFET and of the high-side MOSFET respectively, as introduced in Chapter 3 in the IC brick design phase.

For the high-side switch (Eq. 4.5), the constraint is particularly strong for low values of turns ratio, because most of the effective duty-cycle is dedicated to the actual on-time of the MOSFET, leaving little time for the ZVS transitions. But the maximum duration of the ZVS transition increases linearly with the transformer turns ratio.

On the other hand, for the low-side (Eq. 4.6), the constraint on the ZVS transitions is less strong for low values of turns ratio. However, the larger the turns ratio, the stronger the constraint for the low-side. For high values of the turns ratio, the effective duty-cycle gets close to 1, and so the time left for the ZVS transitions is very small.

Overall, the strongest constraint is going to limit the maximum time allowed for the ZVS transitions. The objective when selecting the transformer turns ratio is therefore to find the value that minimize both constraints, to ensure the ZVS transitions can be as long as possible and thus require a current as low as possible.

Since both constraints change linearly with the value of the transformer turns ratio in opposite directions, to minimize the two constraints at the same time, the value at their intersection should be selected. From there, (4.5) and (4.6) give the following relation for the optimal transformer turns ratio:

$$N_{tr\ opti} = \frac{V_{in}}{2 \cdot (V_{out} + V_D)} \cdot (1 - f_{SW} \cdot (t_{on\_min\_LS} - t_{on\_min\_HS})) \tag{4.7}$$

Taking for example $V_{in} = 400$ V, $V_{out} = 12$ V, $V_D = 0.5$ V, $fsw = 1$ MHz for the converter's parameters, $t_{on\_min\_HS} = 200$ ns and $t_{on\_min\_LS} = 300$ ns constraints for the switches minimum on-time, the optimal transformer turns ratio computed is: $Ntr\ =\ 14.4$.

Note that in the case of the 3L-FC-AHBF topology operating with an input voltage twice as big, the equation slightly changes but the results remain identical because the timing constraints are the same. So the optimal turns ratio value for a 2L-AHBF stage operating at 400 V is the same as for a 3L-FC-ABHF stage operating at 800 V, if the transformer's operating frequency is the same.

Using the results obtained from the converter's simple model, it is possible to compute the minimum value of the RMS current required at a given frequency, for different values of the turns ratio. The results shown in Figure 4.6 were obtained at $V_{in} = 400$ V. The minimum value of the RMS current is normalized to the value obtained at $f_{sw} = 500$ kHz and $N_{tr} = 15$ that gives $i_{pri\ RMS} = 33.7$ mA.

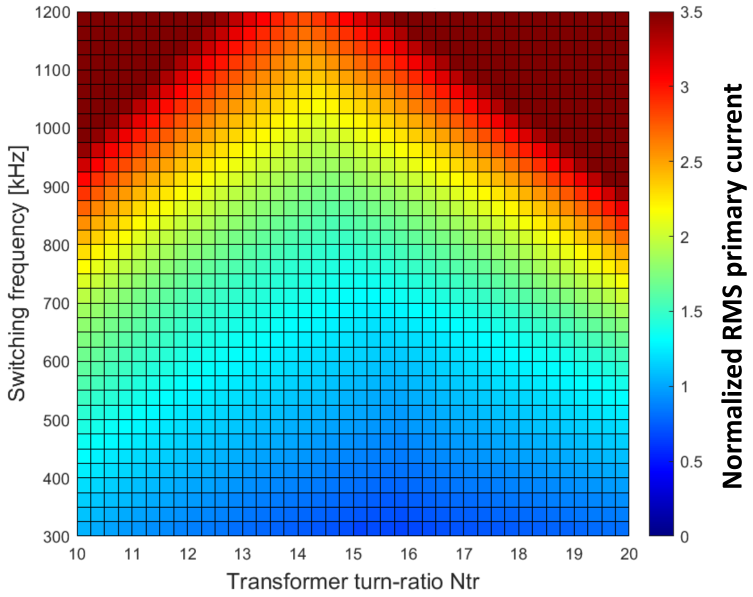


Figure 4.6: Evolution of RMS i_{PRI} with N_{tr} and frequency for $V_{in} = 400$ V

Figure 4.6 illustrates well the evolution of the primary current RMS value with the transformer turns ratio N_{tr}. It shows the existence of a turns ratio that allows to minimize the primary current that is quite close to the one obtained using (4.7). It also confirms that impact of the switching frequency on the RMS primary current: the higher the frequency, the higher the minimum primary current RMS value, as predicted in Chapter 2.

Additional considerations

The value of the input voltage largely influences the optimal turns ratio value. So if the objective of the converter design was to optimize efficiency over a large input voltage range, the optimization of the turns ratio would become more complex.

One option could be to optimize the turns ratio for the highest input voltage value, since it is where efficiency will probably be lower (worst case). The value obtained for the optimal turns ratio would be quite different: for $V_{in} = 500$ V, $N_{tr} = 19$ at 500 kHz. But none of the selected transformer designs will allow to test this possibility, due to limited number of designs that was manufactured.

Another consideration that could play a role in the choice of the turns ratio is the trade-off there is between this parameters and the number of turns. In a transformer design, the number of turns must be an integer. In the present application, the number of secondary turns is low (typically less than 5 turns). So it means that only a limited number of values can be selected for the number of primary turns to obtain the targeted turns ratio. But this number of primary turns might be different than the maximum number of turns it is possible to place around the core, that would allow to decrease the losses (for a given core geometry and the same constraints on PCB manufacturing).

For example, the maximum number of turns that can be placed around a E18 core is $N_{pri} = 40$. However, with this number of primary turns it is not possible to create a transformer with the optimal turns ratio, since $N_{sec} = 2$ would give $N_{tr} = 20$ and $N_{sec} = 3$, $N_{tr} = 13$. In that case, there would be a trade-off to find between the number of turns and the turns ratio. However, due to the limited number of designs manufactured, the study of this trade-off is not implemented.

4.2.4 Number of turns and balancing with frequency

As highlighted in [65], the number of turns is a determining design parameter for the transformer, as it influences both the core and the conduction losses. It needs to be carefully selected to ensure minimal losses in the transformer. Moreover, the HVLP context changes the paradigm that usually guides the choice of the number of turns, such that it is important to analyze the impact of this design parameter on the main types of losses. In the end, an approaches emerges to select the number of turns in accordance with the targeted switching frequency.

Impact on core losses

As presented in the first part of this work, the core losses are one of the main obstacle to build highly efficient isolated HVLP converters, because they tends to increase together with the converter input voltage and are not load-dependent. To overcome this issue, the ML-FC-AHBF topology was selected, but it is not sufficient to ensure low losses inside of the transformer core. The number of turns around the core should thus be selected to ensure the flux density inside the core remains low, in order to mitigate the core losses. Because the peak density is inversely proportional to the number of turns around the core, as discussed in Chapter 1 (Equation 1.2).

To estimate these losses, the improved General Steinmetz Formula (iGSE) is used [72]. It allows to estimate the losses inside the magnetic core for non-sinusoidal voltage excitation. The coefficients required to compute the losses are the same as for the classical Steinmetz formula, and they are sometimes given by the core manufacturer (in this case, coefficients for the 3F4 material were found on Ferroxcube's website, in the section dedicated to the design tools).

Using this method, it is possible to compute for a given material the core losses obtained when the transformer is excited by a trapezoidal voltage. The impact of the number of turns and of the frequency on core losses is shown in Figure 4.7. To highlight the evolution of the core losses with these last two parameters, the transformer turns ratio is kept constant ($N_{tr} = 15$) for all the values of the number of primary turns (N_{pri}), such that the waveform of the voltage excitation are the same.

As expected, increasing the number of turns allows to significantly reduce the core losses (note that a logarithmic scale is used for the core losses). Doubling the number of turns can indeed help divide by ten the core losses. Figure 4.7 also demonstrates that increasing the switching frequency is another possibility to decrease the core losses.

Therefore, an early outcome of the loss analysis is that the minimum number of turns around the core should be high enough to allow to decrease core losses and to build high efficiency solutions. This is quite different than more classical planar transformer designs (with higher power or lower voltage) where the number of turns can stay below 10 without drastically decreasing the efficiency.

Impact on the conduction losses

The conduction losses inside the transformer are due to the currents that flow through the primary and the secondary windings that present a non-zero resistance.

The present analysis focuses on the resistance of the primary winding, because the secondary winding resistance is much lower, due to the low number of turns. The RMS value of the secondary current is also smaller than it could be expected, as the classical relation between the primary and the secondary RMS currents ($N_{pri} \cdot I_{pri\ RMS} = N_{sec} \cdot I_{sec\ RMS}$) is not valid in the present case, since most of the primary current is due to the current in the magnetizing inductance.

The resistance of a winding drawn on a PCB can be computed like for a classical wire using only geometrical considerations regarding its section and its length. The section is determined by the thickness of the copper layer, that is typically 35 µm (sometime 17 µm for internal layers) and by the width of the track. For a given core size, the higher the number of turns, the longer the winding and the smaller its width (because the maximum width is fixed by the size of the winding window, that is decided by the core geometry) so the resistance of the winding increases very quickly. For example, the resistance of the primary winding of design #1 (for which $N_{pri} = 29$ turns) is close to 14 Ω.

The resistance of a winding will also vary with the frequency at which the transformer operates due to the skin and proximity effects.

The skin effect forces the high frequency currents to circulate only at the surface of the conducting material, thus limiting the effective conductive section, leading to a higher resistance. To make sure the resistance rise is limited, the thickness of the PCB track should be smaller

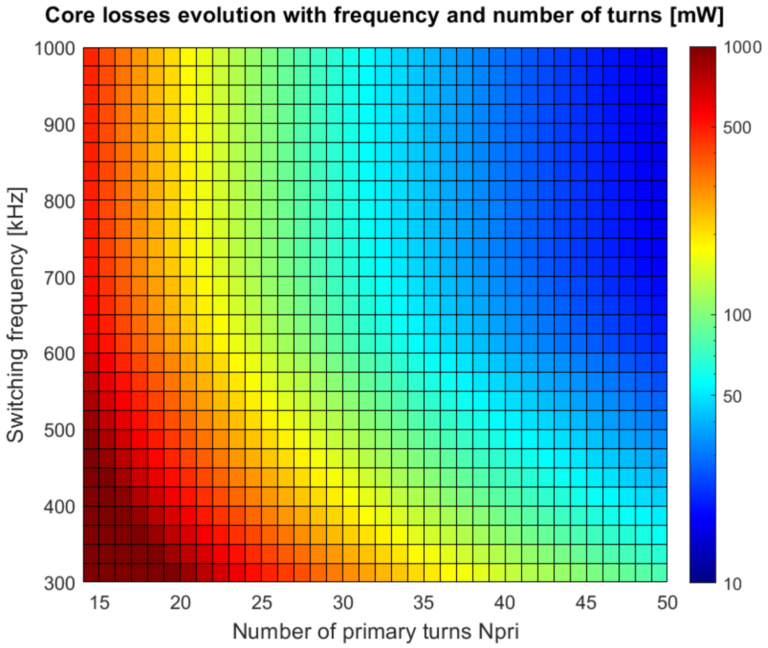


Figure 4.7: Core losses estimation for a E22+PLT core in 3F4 at $V_{in} = 400$ V

than the skin depth associated to the material at the maximum frequency excitation. For the copper, the skin depth at 1 MHz is about 65 µm. Therefore, in the case of a planar transformer, the impact of the skin effect is less important, since the tracks have a low thickness (typically 35 µm).

The proximity effect considers the impact that one current flowing inside a conductor has on the nearby conductors' resistivity, due to the eddy currents. For this reason, if two nearby tracks conduct an AC current flowing in the same direction, the resistivity of these tracks will increase. The impact of this phenomenon on the resistance increase of a transformer winding has been analyzed in many past studies, for various winding's types and shapes [73, 74, 75]. However, it remains difficult to estimate with accuracy the impact of the proximity effect for planar transformers, especially when multiple turns are placed on the same layer and the porosity factor decreases [76].

Therefore, another early design choice made during the transformer design phase was to make the distance between two consecutive tracks of a winding equal to their width. This way, the influence of adjacent tracks is reduced, and the resistance increase with frequency is limited. Note that this choice however decreases the maximum width of the track and so it increases the DC resistance. Some studies have tried to find an optimum width for the tracks around a planar E-core [77], but a simpler approach was preferred for the first design iteration.

To validate this design choice, the resistance increase with frequency is evaluated. Despite the multiple efforts to build analytical models, Finite Element Method (FEM) simulations are still often used to predict the impact of both the skin and proximity effects. In the present case, the transformer designs were simulated using the MAXWELL simulation tool (ANSYS ELECTRONICS software). The results for the current density reached inside the PCB tracks and for the resistance increase with the operating frequency are shown in Figure 4.8 and in Figure 4.9 respectively.

The results presented in Figure 4.8 are obtained using a 2D model of the planar transformer. The primary winding is located on the two top layers of the PCB while the secondary turns are on the bottom layer (the layer arrangement is discussed more in details in section 4.2.5). The current density inside the primary and secondary turns clearly changes and is no longer homogeneous for high frequency current excitations. As a consequence, the AC resistance of the windings increase.

To compare the evolution of the AC resistance for different transformer designs, the factor F_r is introduced. It is defined as the ratio between the resistance at a given frequency and the DC resistance associated. The evolution of F_r with frequency is presented in Figure 4.9 for the primary winding of different planar transformer designs.

The results in Figure 4.9 show the resistance increase with frequency is limited, thanks to the design choice made to reduce the tracks' width. Depending on the number of turns (N_p) and on the tracks' width (w_T) of a design, the F_r factor is slightly different, but is remains below 1.10 for all designs in the frequency range considered ($<$ 1 MHz). These results can thus be used to predict the additional winding losses due to the frequency at which the transformer is operated inside the complete DC/DC converter, and it can be used to estimate winding losses with more accuracy.

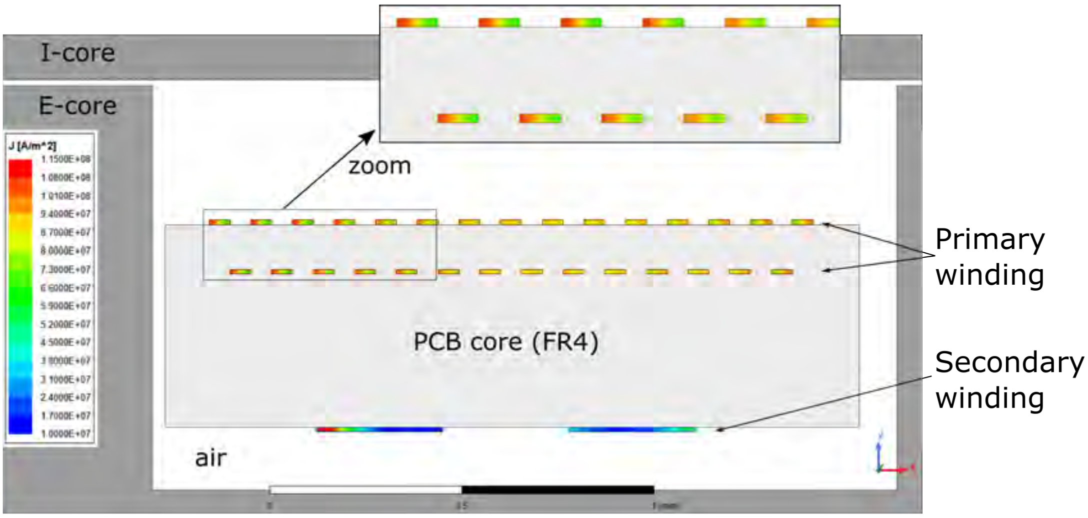


Figure 4.8: 2D-FEM axisymmetric simulation results - current density inside the transformer windings for a 1 MHz excitation

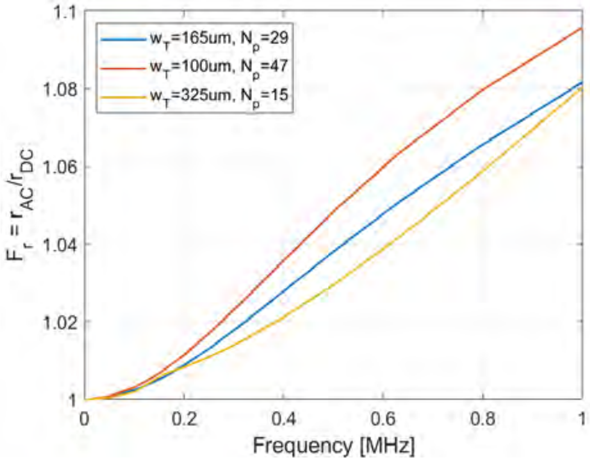


Figure 4.9: Evolution of F_r vs frequency for primary winding

Choice of the number of turns

The number of turns should thus be selected to minimize the sum of the core and conduction losses to ensure a high efficiency. However, there are other design parameters that will largely influence these losses, like the transformer's operating frequency. To be able to adapt to several values that these parameters can take, four different solutions are selected for the choice of the number of turns.

The selected solutions are placed on the DoE "map" that will regroup all the selected designs, in function of their number of turns and of the frequency at which they should operate. Note that this "optimal" frequency is only a rough estimation (computed by the simple converter model), since other design parameters might influence it (e.g. the core material).

Designs with a different number of turns will have a different optimal switching frequency, because the frequency plays a great role in determining the conduction losses. Due to the

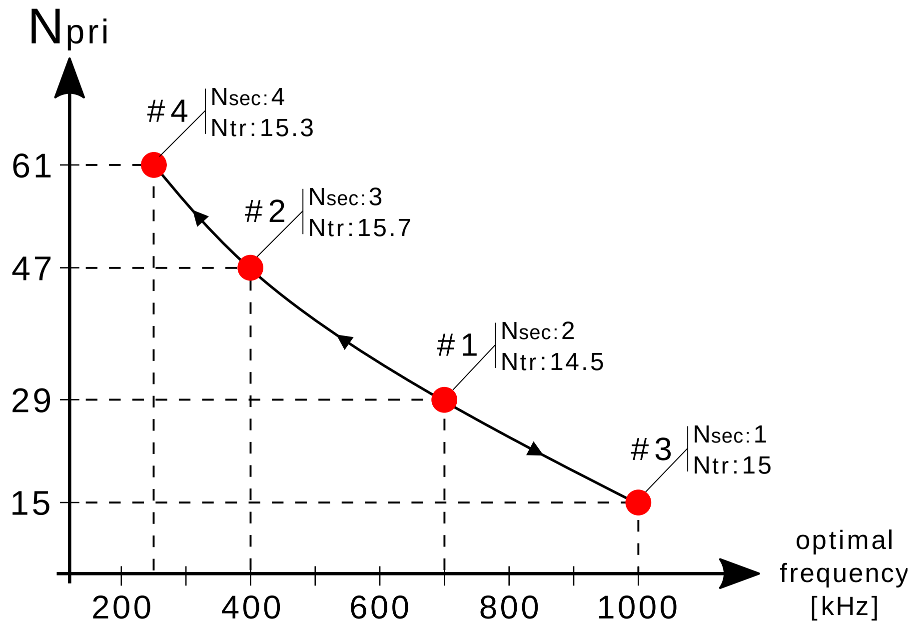


Figure 4.10: DoE map - Number of turns

resistance increase described previously, but also because the minimum RMS primary current increases with the frequency, as highlighted in chapter 2. The selected designs and their estimated optimal frequency are plotted in Figure 4.10.

Design #1 is the one presented at the beginning of the section. Its primary winding is composed of 29 turns and its secondary of 2 turns, such that the turns ratio is close to the ideal value computed earlier ($N_{tr} \approx 15$). The simplified model is used to compute the "optimal" operating frequency at which the total losses should be the lowest. It is located around 700 kHz for design #1.

From this initial design, it is possible to create few other solutions changing the number of turns placed around the core. For all the designs, the number of turns on primary and secondary is selected to keep the turns ratio close to 15.

With the design #2, an alternative solution is built with a higher number of turns (47 for the primary, 3 for the secondary). A consequence of this higher number of turns is a shift of the optimal frequency, that should be lower than for the design #1 because of the higher resistance of the primary winding of design #2. A solution with a number of turns even larger is considered: design #4 has its primary winding formed with 61 turns and its secondary with 4 turns. Targeted frequency for the last design is thus lower than design #2.

Another solution investigated is design #3 that presents a much lower number of turns (15 primary turns, 1 secondary turn) and for which the optimal operating point is shifted up to high frequency.

4.2.5 PCB layers arrangement: mitigation of parasitic capacitors

Influence of the parasitic capacitors

The use of multi-layer PCBs is targeted for the design of the planar transformer's windings. Although the number of layers is limited to 4, there are still many different ways to create the transformer windings. As described in [65], the choice of the layer arrangement is guided by a fundamental trade-off between the quantity of leakage inductance and the quantity of parasitic capacitance.

In Chapter 2, the topology analysis revealed the low influence of the parasitic inductance on the power stage's behavior. At the same time, it also showed the importance of the transformer's parasitic capacitor during the ZVS transitions, as it determines the quantity of current required to operate the soft-switching transitions. Thus the design of the transformer should aimed at reducing these parasitic capacitors as much as possible, since they can be particularly large in the case of planar transformer.

In the present analysis, two different parasitic capacitors are considered, as illustrated in Figure 4.11. The first one is the primary-secondary (or mutual) capacitor (C_{ps}), that is due to the primary and secondary winding "overlapping" surfaces. The second one is the primary self capacitor ($C_{self\ pri}$) that is created by the primary winding with itself. A similar model can be found for the transformer parasitic capacitor in [65, 78, 79]. Here, the secondary self capacitor is neglected because of the large transformer turns ratio, that will drastically reduce its influence [80].

More complete models exist, to take into account the capacitive coupling effects with more accuracy, that include up to six different parasitic capacitors, as in [81, 82], but this simple model already allows to draw some interesting conclusions. Because both types of parasitic capacitors might lower the performances of the high-frequency transformer for various reasons.

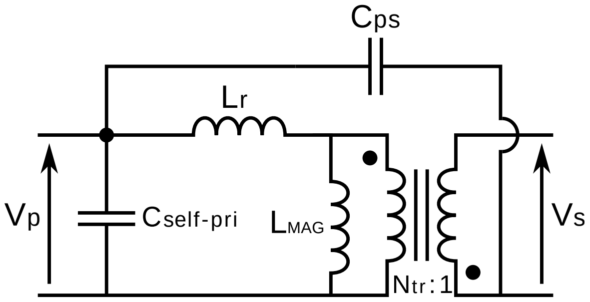


Figure 4.11: Model used for the transformer's parasitic capacitors

The impact of the mutual capacitor (C_{ps}) was already discussed in Chapter 2: the higher this capacitance, the larger the current to operate the ZVS transitions, leading to higher conduction losses, because it is added (at least partially) to the parasitic capacitor connected to the middle switching node of the power-stage.

The primary self-capacitance is also added to the switching parasitic capacitor that is charged during the ZVS transitions, since it is connected in parallel with the transformer's primary inductance. In addition, the primary self capacitor also sets the transformer SRF (Self Resonant Frequency), together with the primary inductance. The higher this capacitance, the lower the resonant frequency. Even if the SRF is higher than the operating frequency of the power stage extra losses may be generated, because the energy contained in higher harmonics of the current excitation (that is not exactly sinusoidal) might be lost. For these reasons, the primary self-capacitor should also be reduced, to ease the ZVS transitions and to push the SRF as high as possible.

Practical implementation: arrangement of the windings on the PCB layers

As presented in the transformer's primary technological choices, a 4 layers PCB is used to build the transformer windings. To mitigate the parasitic capacitors, the arrangement of the transformer windings on these layers must be done carefully. A 2D side view of three different arrangements of the tracks (that compose the transformer windings) on a 4 layer PCB are shown in Figure 4.12. It shows the how the primary and the secondary windings of the transformer can be placed on 4 layers of the PCB, with the main parasitic capacitance associated, in a cross-sectional view of the transformer in the half RZ plan.

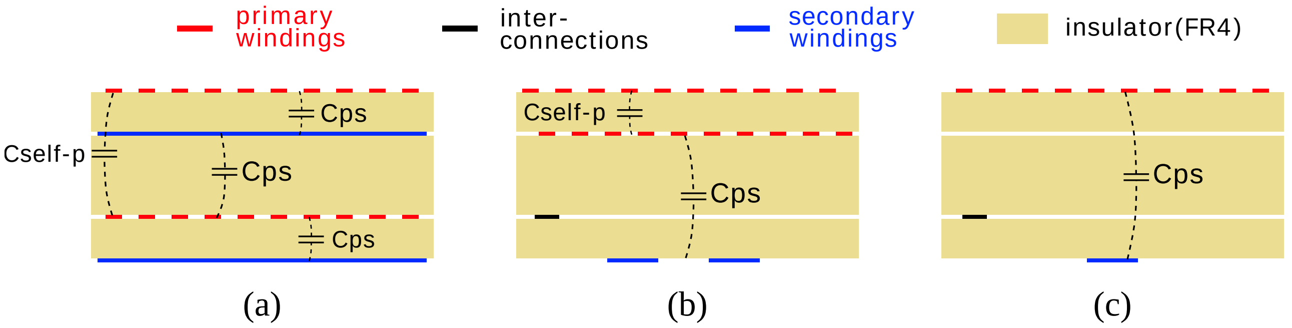


Figure 4.12: Presentation of the different layer arrangements (a) Interleaved - (b) Design for HVLP transformer - (c) Design for HVLP transformer with low capacitance

The first arrangement (a) represents the classical solution for the windings arrangement: the primary and the secondary windings are interleaved to increase the coupling and to reduce the leakage inductance and the AC resistance. However, this type of arrangement tend to present a very large mutual capacitor (C_{ps}) due to the large overlapping surfaces. On the other hand, the self capacitance ($C_{self\ p}$) is reduced, since the top portion of the secondary winding creates a "shield" between the two portions of the primary winding.

The arrangement (b) is proposed to create a HVLP transformer with lower mutual capacitor. The primary winding are now placed on the two top layers of the PCB while the secondary winding is placed only one the external bottom layer. It allows to drastically reduce the primary-secondary parasitic capacitance (C_{ps}) since the overlapping surface is smaller and the distance between the winding is increased, when compared to arrangement (a). Note that the secondary winding is now regrouped on a single layer and its width is reduced. It is not an issue in the low-power context, since the secondary current will be small it won't lead to large current density in this winding.

However, a non-negligible self capacitance ($C_{self\ p}$) will be create between the two portions of the primary winding located on the two top layers. A design technique shown in next paragraphs will allow to lower the value of this capacitance, but without being able to cancel it. The design #1 uses the arrangement (b), which is why its mutual capacitance is quite small

($C_{ps} = 11$ pF while it can be more around 100 pF with arrangement (a)). But its self primary capacitance has a value of 12 pF, which limits the SRF below 1 MHz at the maximum value of primary inductance.

To further reduce the parasitic capacitors, the arrangement (c) is proposed. It is quite similar to arrangement (b) with the primary and the secondary winding placed on the opposite layers of the PCB, but the arrangement (c) regroups all the primary winding on the top external layer. This allows to mitigate the mutual capacitor (C_{ps}) increasing the distance between the primary and the secondary winding. The self capacitance is also reduced as the overlapping surface of the primary winding is largely reduced (the only self capacitance left is between the adjacent tracks on the top layer, but it is much smaller due to the low thickness of the PCB tracks).

However, another consequence of regrouping all the primary winding on a single layer is that it drastically limits the number of turns around the core (because of the minimum track width and the isolation distance imposed by the PCB manufacturer). Therefore, this type of arrangement can be used only for designs with a low number of turns.

For the solutions with more than one layer dedicated to the primary winding, the self capacitance can be mitigated by changing the way the different portions of the winding are connected. Indeed, the value of the self capacitance depends on the overlapping surface but also on the voltage difference between the different portions of the winding. The smaller the voltage difference, the smaller the "effective" self capacitance. Figure 4.13 presents two ways of connecting the portions of the primary winding for an arrangement like in Figure 4.12 (b).

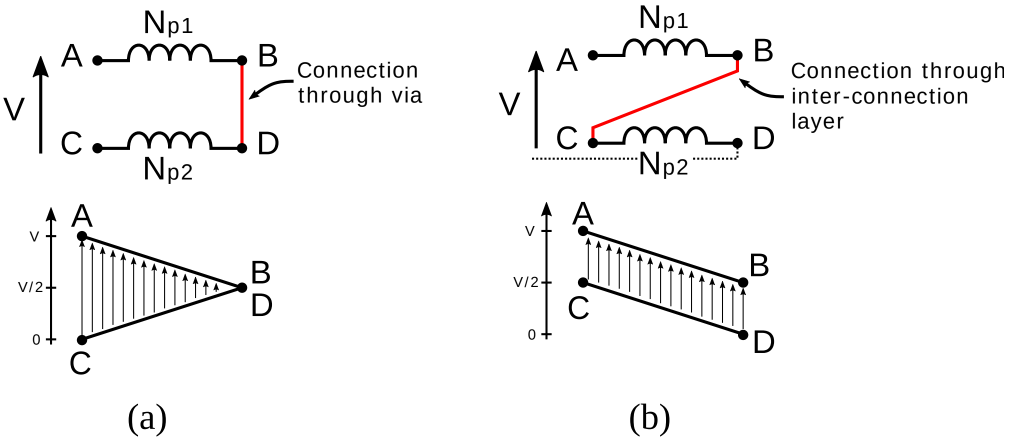


Figure 4.13: Possible connections of the two portions of the primary winding and associated voltage difference between overlapping tracks (a) Classical - (b) Low self capacitance

In standard designs, if several turns are placed on each layer, the winding goes from the outside of the core to the center on a layer, and then from the center of the core toward the outside on another layer, leading to the voltage distribution between facing windings as presented in (a). To mitigate the self-capacitance, it is possible to change the voltage distribution by connecting the layers for a same winding as shown in Figure 4.13 (b) as discussed in [65, 83]. Note that it requires an additional layer, in order to connect the different portions of the windings. More advanced techniques can be used to further reduce the self capacitance [84], but they require a more complex arrangement with many via so they are not selected here.

This technique allows to keep the primary self capacitor reasonably small: for design #1, the measured value of $C_{self\ p}$ is close to 12 pF.

In the DoE, most of the selected designs have an arrangement as in Figure 4.12 (b), since it allows to place more turns around the core than solution (c). However, to further study the impact of the layer arrangement (b) and (c), an additional point is added to the DoE.

Design #5 introduced is similar to design #3: the same E-core is used, the number of turns is the same. But design #5 uses a layer arrangement where all the primary winding are placed on a single layer, while for design #3 there are distributed on two layers. It allows to decrease the quantity of parasitic capacitors as shown in Table 4.2.

Table 4.2: Measured parasitic capacitors for designs #3 and #4

	Main design characteristics	C_{ps} [pF]	$C_{self\ p}$ (w/o core) [pF]	$C_{self\ p}$ (w core) [pF]	SRF (w core) [MHz]
#3	E22,Np15,Ns1	6.5	9.2	12.2	1.75
#5	E22,Np15,Ns1	5.4	1.8	6.5	2.4

The parasitic capacitors measured for design #5 reveal the gap between the two layer arrangement investigated. For example, the primary self capacitance measured without a E-core is much lower for design #5. However, the gap tends to decrease when the core is added, probably due to the parasitic capacitor that appears between the tracks of the PCB and the E-core that lower the Self-Resonant Frequency. But placing all the turns on the same layer like for #5 still allows to push away the SRF and to reduce the total capacitor, so the converter might operate at higher frequency.

4.2.6 Core size

At the beginning of the transformer design phase three different core references were selected to measure the impact of the size of the core on the performances and to explore several variations of the size-performances trade-off. The selected E-core references are the E22/6/16R, the E18/4/10R and the E32/6/20R, each of them being associated with the appropriate PLT core.

Increasing the size of the core will help to lower the losses in the transformer. The larger the core, the bigger its cross section and so the flux density decreases (for the same volt-second and number of turns) so the core losses are reduced. The maximum number of turns that cen be placed around the core becomes higher since the width of the winding window increases. The impact on the conduction losses is less obvious, as a larger core will not necessarily allow to decrease the winding resistivity. On the other hand, a design using a larger core will show larger parasitic capacitors because the total surface of tracks increases.

To explore the impact of the size of the E-core, several points are added to the DoE. Designs using a E18 core are added to be compared to designs using E22 with the same number of turns (designs #6 and #7 are compared to designs #1 and #3). On the other hand, a design using a E32 core is also added: design #8 has the same number of turns as design #2. Size comparison is not possible for design #4 because the other E-core geometries (E22, E18) don't allow to place enough turns around the core.

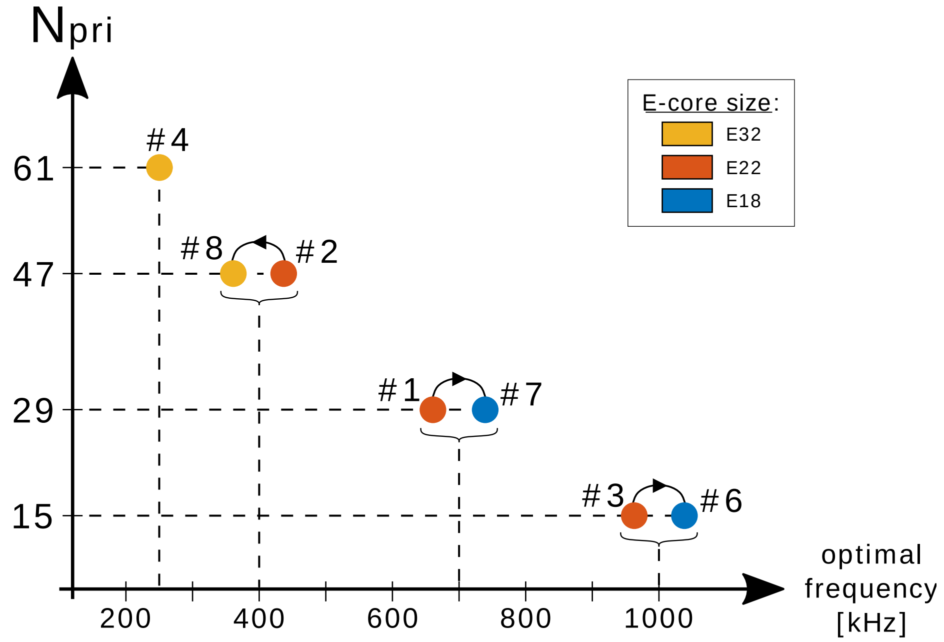


Figure 4.14: DoE map - Size of the E-core

The designs added to the DoE are shown in Figure 4.14 next to designs to which will be compared to study the influence of the core size on the transformer performances. Once again, the targeted frequency of use indicated is only a rough estimation that does not take into account the variety of magnetic core material that can be used for the different designs. Although there is not doubt that increasing the core size will allow to decrease losses and improve the efficiency, the gap between the performances of the largest and of the smallest solution will be interesting to study and quantify.

4.2.7 Core material

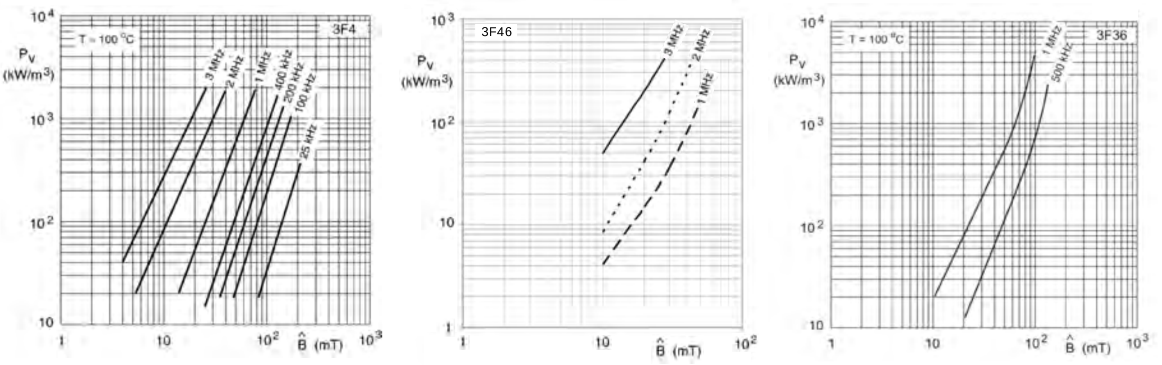
The E-core material largely influences the transformer performances. Its permeability sets the maximum inductance value, together with the number of turns and the core geometry. Moreover, the material has a critical impact on the core losses, such that is should be selected carefully.

Inside the family of MnZn cores, three materials are selected for their interesting properties and added to the DoE. The choice of the material is closely linked to the choice of the transformer's operating frequency, as each material will show different characteristics for a given frequency.

The 3F4 material is selected because it offers low losses on a large frequency band (from 200 kHz to 2 MHz). It is a material often using for high frequency transformer such that its loss model (i.e. the Steinmetz parameters) is known at many frequencies. So it is an interesting candidate to monitor the performances of a transformer at different frequencies.

The 3F36 is a material with low magnetic losses as well, that should present losses almost independent of the operating temperature. It is usually intended for designs operating at lower frequency (≤ 500 kHz). However it is quite recent so its model is still not known with accuracy.

Finally the 3F46 is a very low losses material that is intended for design with a high switching frequency (≥ 1 MHz). Although its Steinmetz parameters can be found for high operating frequency, it is not the case for low frequency. It will therefore be interesting to monitor the behavior of this material for medium or low frequency designs.



(a) (b) (c)

Figure 4.15: Core losses evolution with peak density and frequency for (a) 3F4 - (b) 3F46 - (c) 3F36 - curves copied from manufactured datasheets [85, 86, 87]

Figure 4.15 presents the volumetric core losses in function of the peak density and of the frequency for the three selected materials [85, 86, 87]. Depending on the operating frequency of a transformer design, one of these three materials is selected: for example, 3F36 should offer the lowest losses for low frequency designs while 3F46 should enable low losses only for high frequency designs.

4.3 Summary of the selected designs

4.3.1 Identifying the different types of design

Now that the main technological choices and the important design parameters are introduced, it is possible to summarize the selected designs that will be manufactured and tested inside the HVLP converter. Although all the selected designs offer a different solution, several design ”types” can be identified.

The analysis of the design parameters has revealed the influence of the transformer's frequency on the choice of these parameters. It can thus be used as a basic parameter to categorize the transformer designs into different families: solutions for low-frequency, solutions intended for high-frequency and solutions ”in-between” for medium frequency.

For low-frequency designs, a high number of turns is required in order to mitigate core losses and create a larger inductance to ensure low primary RMS current. Thus large core use is required, since small cores only have a limited winding window, which limit the number of turns. The material is also selected in consequence: 3F36 material will probably be the best candidate for these designs, although 3F4 could also offer good performances if frequency is not too low. However, constraint on the winding resistance and on the parasitic capacitor is less strong, since the primary current ripple should anyway be reduced.

On the other hand, for high-frequency designs, the number of turns can become smaller and the core losses remain acceptable if a high-frequency material with low-losses in used for the E-core (i.e. 3F46 in this case). To ensure low conduction losses, the parasitic capacitors and the winding's resistances should be as small as possible, also there is a trade-off to find between these two parameters. An alternative layer arrangement (using only one PCB layer for the primary winding) can be used to explore a different option for this trade-off. The value of the primary inductance should be small to allow a current ripple high enough to ensure ZVS transitions to complete in a short time, to met the IC design constraint regarding the minimum on-times etc.

In the end, design for medium frequency should try to explore a trade-off between these two approaches, that is half-way in terms of number of turns and of targeted frequency. For these designs, the choice of the material is not clear since the data from the manufacturer do not allow to estimate properly the performances outside of a frequency range.

4.3.2 Map of the Design of Experiments

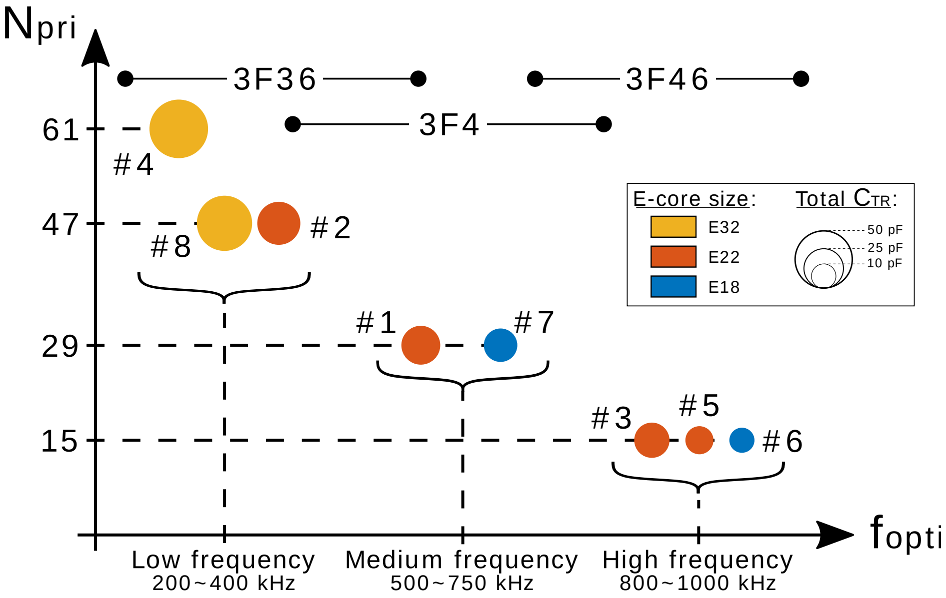


Figure 4.16: DoE map - Summary of the selected designs

Figure 4.16 summarizes the selected transformer designs to be manufactured and tested inside the HVLP converter. The different "families" of designs identified are presented and they are in-line with the previous analyses made of the design parameters. In particular, the variation of the optimal frequency with the number of turns is shown. The choice of additional design parameters in function of the frequency also appears, like the core size (color of the circles) and the transformer's total parasitic capacitor (size of the circles represent C_{TR} that is the sum of C_{ps} and $C_{p\ self}$). Finally, the choice of the core material in function of the operating frequency is highlighted on the top of the graph.

This figure will be used as a road-map for the Design of Experiment that was presented during this chapter. Comparing similar designs will allow to study the impact of specific design paramters and, in the end, to identify the design showing the best performances.

In addition to the road-map, Table 4.3 shows the measured characteristics of the selected designs more in details. These values will be used to analyze the performances of each design when it is used inside the HVLP converter.

Table 4.3: Summary of the measured characteristics of the selected designs

Design # and characteristics		f_{opti} [kHz]	L_{opti} [µH]	$r_{pri\ DC}$ [Ω]	C_{ps} [pF]	max. L_{pri} $^{(1)}$ [mH]	$SRF^{(2)}$ [MHz]	$C_{self\ p}{}^{(3)}$ [pF]
#4	E32, Np61, Ns4	250	3900	54.6	28	12.9	0.28	25
#8	E32, Np47, Ns3	375	1900	30.4	22	8.1	0.35	25.5
#2	E22, Np47, Ns3	400	2200	42.7	15	6.70	0.54	13
#1	E22, Np29, Ns2	700	800	13.9	11	2.55	0.91	12
#7	E18, Np29, Ns2	850	550	13.7	8.3	2.4	1.1	8.7
#3	E22, Np15, Ns1	1000	330	3.3	6.5	0.68	1.75	12
#5	E22, Np15, Ns1	1000	375	3.8	5.4	0.68	2.4	6.5
#6	E18, Np15, Ns1	1000	390	3.9	4.4	0.61	2.8	5.3

(1) Value measured with a 3F4 core for E22, E32 and a 3F36 core for E18
(2) Self Resonant Frequency measured on primary for the maximum L_{pri} value
(3) Self capacitor computed from SRF and max. L_{pri} values with the magnetic core

In Table 4.3, the designs are organized from lowest to highest expected optimal frequency. However, the high-frequency designs (#3, #5, #6) all have the same value for the optimal frequency ($f_{opti} = 1$ MHz). It's because the model of the targeted material (3F46) is incomplete and it does not give information for the core losses below 1 MHz, thus this frequency is used as a default value. However, it can be noticed that the last designs (#5 and #6) show an optimal inductance value that is higher than design #3 and that is because both designs have very low parasitic capacitors since they are designed using the alternative layer arrangement shown in Figure 4.12 (c).

Additional characteristics

For all the selected designs, the resistance of the secondary winding is quite small. Its typical value is close to 50 mΩ per turn, so the impact on the conduction losses should be limited, due to the low RMS secondary current expected (≤ 300 mA).

The value measured on the primary side for the leakage inductance is small as well for all the design. It has a value that varies between 0.5% up to 1.7% of the maximum primary inductor displayed in Table 4.3. Therefore, the previous hypothesis assuming the leakage inductance value was small compared to the magnetizing inductance value is correct.

As a result, the coupling between the primary and the secondary side of the transformer is computed for all the designs and it is always greater than 0.99, which can be explained by the very good coupling properties of the planar transformer.

4.4 Conclusion

This chapter has presented the design of a planar transformer suitable for the HVLP converter.

Due to the limitations of the conventional design appraoches, a DoE is used to study the influence of few design parameters and to create a short-list of interesting transformer designs. The early technological choices are introduced: planar transformers are used, with a limited number of core sizes and materials included in the analysis. The technology of the PCB on which are created the transformer windings is also limited in a low-cost perspective (4 layers, track with 100 µm isolation/width). A simple model of the converter of solutions is created to analyze the performances of various transformer design, to guide the design phase.

In a second time, the influence of several design parameters is studied. The optimization of the primary inductance (depending on the frequency) is presented and the existence of an optimal value for the transformer turns ratio is suggested. The choice of the number of turns is discussed, in particular considering its impact on the core and the conduction losses and its relation with the frequency. An arrangement of the transformer windings on the PCB layers is proposed to decrease the parasitic capacitors.

In the end, the various solutions created during the DoE are added to the DoE ”map” and will be tested inside the DC/DC converter during the experimental tests. The selected designs are regrouped in function of their optimal operating frequency (low frequency designs with a high number of turns, a high frequency designs with a small number of turns, ...) and their important characteristics are measured.

Chapter 5

Experimental measurements

In this chapter, the behavior and the performances of the DC/DC converter built using the IC brick and the planar transformers designed are measured. First, the test-bench used for the measurements is presented and the general behavior of the converter is validated upon functional results. The ZVS operating mode is then studied more in details and an optimal operating mode of the converter is identified. The performances of the various transformers designed are then compared to identify the most suitable transformer designs for a HVLP converter. Finally, the performances of the 2L-AHBF and the 3L-FC-AHBF are measured, analyzed and compared to existing solutions to conclude on the interest of the selected approach.

5.1 Tests setup

The test-bench used to supply, control and measure the DC/DC converter is shown in Figure 5.1.

It mainly consists in:

- **a high-voltage SMU** (Source Measurement Unit, 2410 from Keithley) to supply the main input voltage to the converter while measuring the DC input current of the converter
- **an electronic DC load** (BK precision 8600) that sinks a constant DC current on the output of the converter while measuring the output voltage
- **a pulse generator** (81130A from Agilent) is used to create the PWM signal(s) required to control the converter
- **a low-voltage supply** to provide the auxiliary supply of the converter

Two oscilloscopes (Tektronix) are used to monitor the converter's waveforms: one measures the non-isolated control signals while the other is used to measure various current and voltage waveforms from the converter power stage.

5.1.1 Main board

The PCB implementing the converter is presented in Figure 5.2 (photo) and in Figure 5.3 (simplified schematics). It can be divided in two sections: one devoted to the control signals and the power stage of the converter itself.

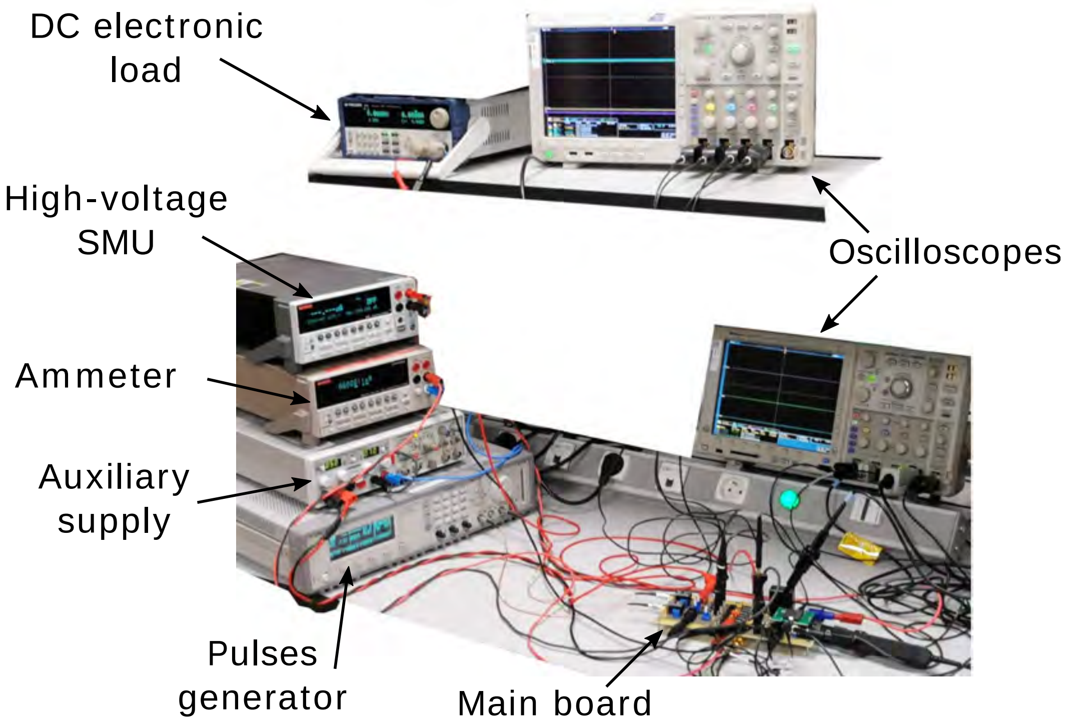


Figure 5.1: Test-bench used to measure the converter

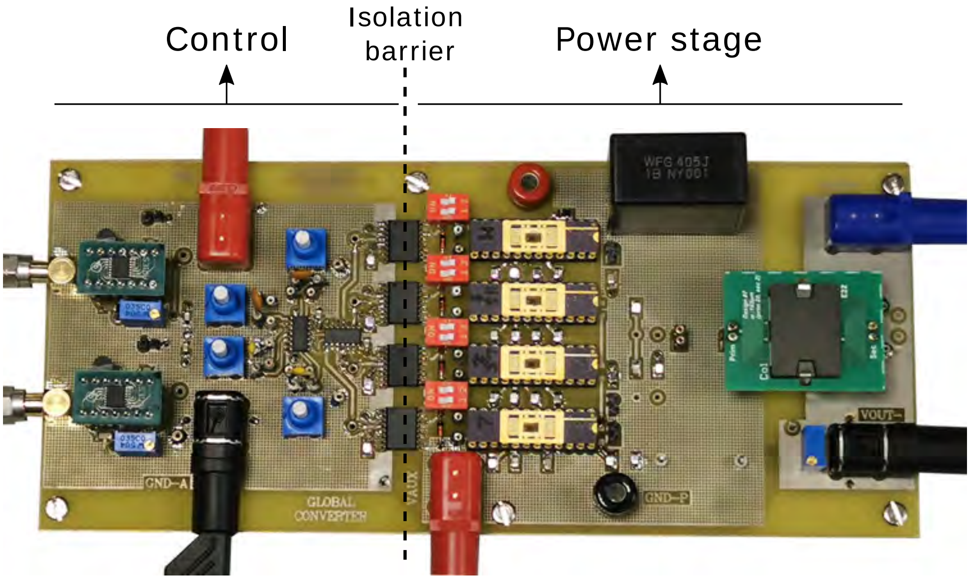


Figure 5.2: Circuit board used to measure the converter

The main role of the "control section" on the PCB is to generate the dead-time (required to operate in ZVS mode) before the power switches turn-on. Since the IC brick internal blocks that should generate these dead-time cannot be used (due to level-shifter's failure at high voltage as described in Chapter 3), circuits built using discrete components are used as a remediation. These circuits simply consist in few logic gates, small external capacitors (about 50 pF) and variable resistors to adjust the duration of the dead-time.

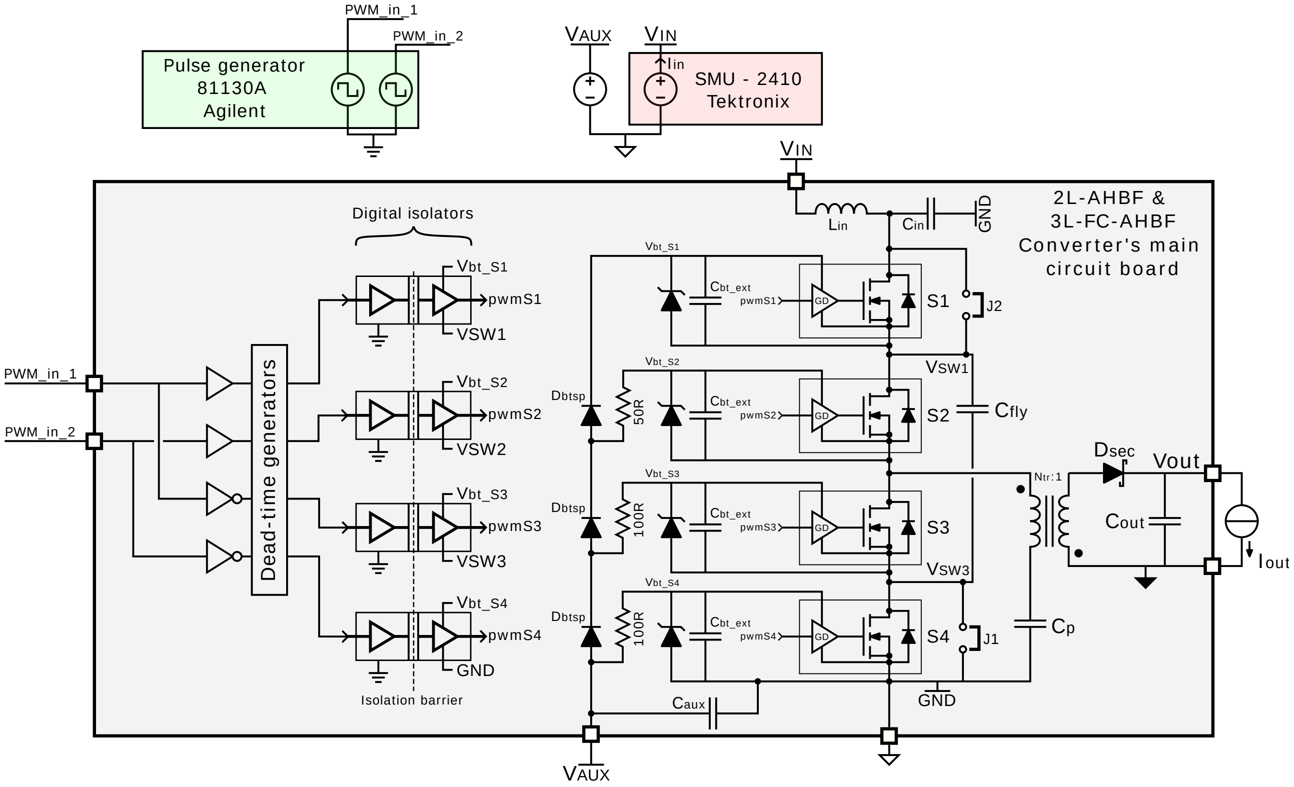


Figure 5.3: Schematic of converter's main circuit board

The control signals of the power switches are transmitted to the power stage through digital isolators. It is necessary to isolate these signals since most of the power switches are floating. Thus the digital isolators are connected to the analog ground reference on one side and to the local floating reference on the other side.

The power stage of the converter is composed of the IC bricks, the custom planar transformer and a few other components located at the bottom of the PCB (the primary capacitor C_p, the secondary diode D_{sec}, the output capacitor C_{out} and the flying capacitor C_{fly}). It can be configured to built either the 2L-AHBF or the 3L-FC-AHBF topologies, adding some jumpers to bypass the dies $S1$ and $S4$.

A simple LC filter (L_{in}, C_{in}) is connected at the main input of the converter (a large HV film capacitor can be noticed in Figure 5.2 while the inductor is at the bottom of the PCB). Its role is to ensure a quality good in measurements of the DC input current to compute the converter efficiency, but this large filter is not required to ensure the converter functionality.

Some external components are also added next to the IC bricks, to ensure their functionality or bypass some of their internal blocks. A large external bootstrap capacitor ($C_{bt\_ext} \sim 4.7$ µF) is added, to ensure a sufficient bootstrap voltage is maintained at each level despite the digital isolators large current consumption. A zener diode (5.1 V) is also added in parallel of the bootstrap supply to ensure it does not exceed the digital isolator's maximum voltage. As a consequence, the bootstrap voltage on the low-side IC bricks is limited and the internal bootstrap circuit of the IC bricks cannot be used in the case of the 3L-FC configuration, because it does not allow to develop a sufficient bootstrap voltage for the high-side IC bricks.

External bootstrap diodes are added to the circuit board to bypass the internal bootstrap circuits in the case of the 3L-FC. For the 2L configuration, the internal bootstrap circuit is used. No significant impact on the power stage behavior and performances is noticed when changing between the internal or the external bootstrap circuit.

The characteristics and references of the discrete components used in the power stage are summarized in Table 5.1.

Table 5.1: Discrete components used in the power stage

Component name	**Characteristics**	**References**
Digital isolator		ISO7710
Secondary diode D_{sec}	Schottky, 60 V, 1 A	PMEG6010CE
Bootstrap diode D_{btsp}	600 V, 0.2 A	RFU02VSM6STR
Primary capacitor C_p Flying capacitor C_{fly}	1 µF, 630 V, X7T	CKG57NX7T2J105M
Output capacitor C_{out}	1 µF, 16 V	
Input filter inductor L_{in}	10 µH, 0.55 A	LPS4012-103MRB
Input filter capacitor C_{in}	4 µF, 1.1 kV	ECWFG1B405JA

5.2 Functional results

To validate the circuit board functionality, the main control signals and power stage waveforms are monitored, for both versions of the power stage (2L-AHBF and 3L-FC-AHBF).

5.2.1 2L-AHBF configuration

The measured control signals in the 2L-AHBF configuration are plotted in Figure 5.4. The signal generated by the pulse generator (PWM_in) is used to create the signals to drive the high-side power switch (HS) and the low-side power switch (LS). These signals are measured on the non-isolated side of the digital isolators, thus they are referred to the analog ground of the circuit board.

As expected, it is possible to control the delay between the turn-off of a power switch and the turn-on of the complementary switch by changing the value of the variable resistors (dt_hs is the dead-time before HS turn-on, dt_ls before LS turn-on). On the other hand, the turn-off of the HS FET is synchronized with the falling edge of the PWM input signal and the LS FET turn-off is synchronized with the PWM input rising edge. The frequency of the control signals and the duty-cycle values can be changed by modifying the PWM input frequency and duty-cycle directly on the pulse generator.

Monitoring these waveforms, it is possible to properly set the dead-time values to allow the ZVS transitions, but also to ensure that the switches on-time does not go below the minimum targeted value (as discussed in Chapter 3), i.e. 200 ns for the high-side switch and 300 ns for the low-side one.

As a reminder, the power stage of the 2L-AHBF configuration is shown in Figure 5.5 with the measured currents and voltages highlighted.

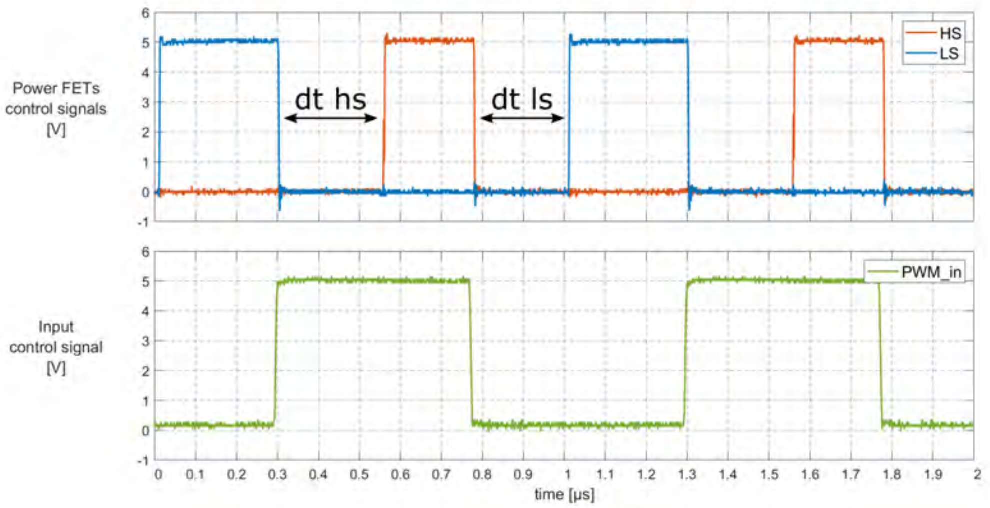


Figure 5.4: 2L-AHBF - Measured control signal waveforms

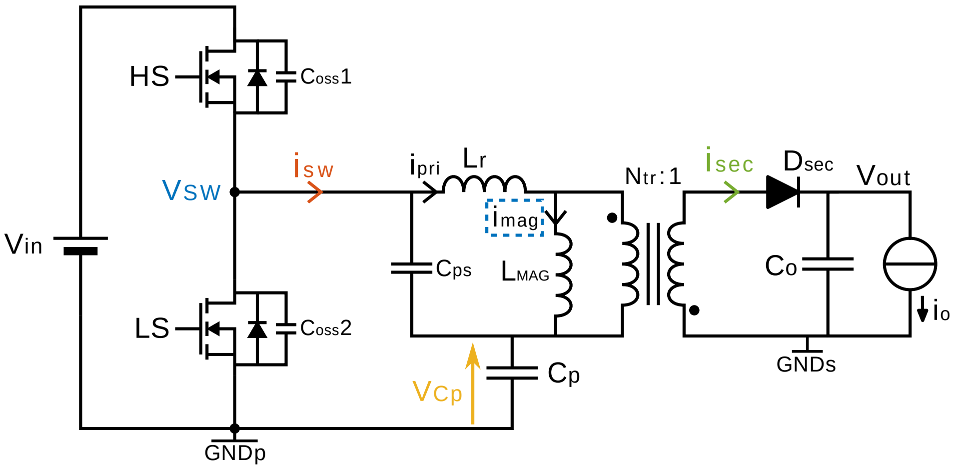


Figure 5.5: 2L-AHBF power stage

The power stage measured current and voltage waveforms are plotted in Figure 5.6 for the following set of parameters: $V_{in} = 400$ V, $V_{out} = 12$ V, $P_{out} = 1$ W, $f_{sw} = 1$ MHz and the transformer design #1 (the various transformer designs are summarized in Figure 4.16 at the end of Chapter 4). It is interesting to compare the general shape of these waveforms to the one obtained in simulation, to confirm the analysis of the power stage behavior (conducted in Chapter 2) is correct.

The voltage at the switching node (V_{SW}) and the voltage across the primary capacitor (V_{Cp}) are measured with high-voltage passive probes (P5100A from Tektronix). The current inside the switching node (i_{SW}) is measured using an AC current probe (CT2 from Tektronix) while the current on the secondary side (i_{sec}) is measured with an AC/DC current probe (TCP0030A from Tektronix). All the probes have a bandwidth higher than 100 MHz. No active differential probes were used in these measurements, as a low CMRR (Common Mode Rejection Ratio) and high parasitic capacitance of the available probes do not allow to measure with accuracy the floating bootstrap voltage or the gate-source voltage of the HS power MOSFET.

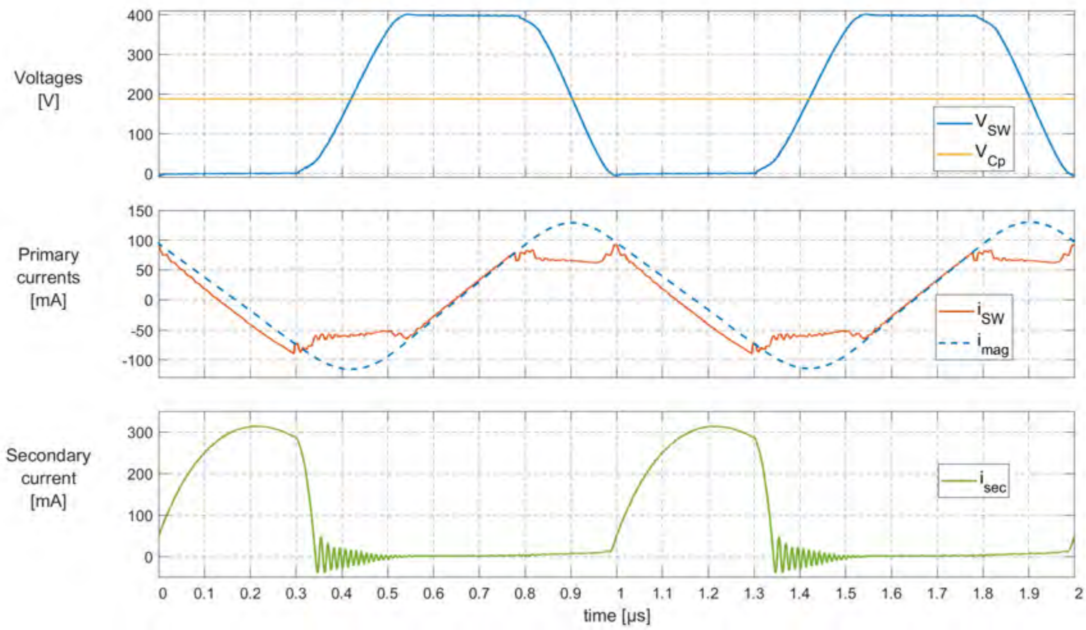


Figure 5.6: 2L-AHBF - Experimental power stage waveforms

Measuring V_{SW} is useful to ensure the converter operates in ZVS mode. Although the V_{GS} of the high-side switch is not measured, the slow transitions of V_{SW} between its low-voltage and high-voltage states reveal that the converter operates in ZVS. The ZVS mechanism and the associated currents and capacitances are discussed more in details in the next section.

The measurements of V_{Cp} can be used to evaluate the relation between input and output voltages. For this, the results predicted by the expressions found in Chapter 2 and the measurements are compared.

Using (5.1) and measuring the duration of the ZVS transitions and the switches on-time, the predicted voltage across the primary capacitor can be computed as:

$$V_{Cp} = V_{in} \cdot (D_{HS} + \frac{dt_{HS} + dt_{LS}}{2T}) = 400\ \text{V} \cdot (0.235 + \frac{250\ \text{ns} + 215\ \text{ns}}{2 \cdot 1\ \mu\text{s}}) = 187\ \text{V} \tag{5.1}$$

The measured value is $V_{Cp} = 187.8$ V, which matches very well with the expected value.

For the output voltage prediction, (5.2) is used. The value of the inductances associated with the data point are: $L_{mag} = 324$ µH and $L_r = 12$ µH. The diode drop is assumed constant at $V_D = 0.4$ V and the transformer turns ratio is $N_{tr} = 14.5$.

$$V_{out} = \frac{V_{Cp}}{N_{tr}} \cdot \frac{L_{mag}}{L_{mag} + L_r} - V_D = 12.1\ \text{V} \tag{5.2}$$

The predicted value is not too far from the measured value that is $V_{out} = 12.03$ V.

These two results show that the values predicted and measured match well. It confirms the expression (found in the power stage analysis in Chapter 2) is correct at least in a first approximation - although its accuracy is hard to evaluate as the duration of the ZVS transitions and on-times of the switches are measured with a limited precision (± 5 ns). But it confirms the impact of the duration of the ZVS transitions on the relation between input and output voltages.

The measurement of the secondary current i_{sec} reveals its shape is roughly similar to the one predicted by simulation. The slower dynamic observed at the beginning is probably due to a poor modeling of the secondary diode in the simulation tool. The ringing observed during the low-side turn-off and during the ZVS transition is also probably related to the parasitic capacitance of D_{sec} that resonates with the transformer's leakage inductance L_r. But the measured RMS value of the secondary current still matches the value obtained in simulation, so these small inaccuracy should not lead to large extra losses.

Finally, the current inside the switching node i_{SW} is measured to account for the conduction losses on the primary side of the transformer. It is not exactly equal to the current through the transformer primary side that was simulated as it does not account for the currents inside the transformer's parasitic capacitances. Thus the difference between i_{SW} and i_{pri} is noticeable only during the ZVS transitions.

The waveform of i_{SW} is also compared to the waveform of the magnetizing current i_{mag}. Even though i_{mag} is not directly measured, it can be estimated from the primary voltage $V_{pri} = V_{SW} - V_{Cp}$ and the primary inductance value. This comparison reveals that i_{SW} is quite similar to what was predicted by the 2L-AHBF analysis. i_{SW} current is equal to the magnetizing current when V_{SW} is high (i.e. when the HS FET is on). The difference between i_{SW} and i_{mag} when V_{SW} is low (i.e. when the LS FET is on) corresponds to the secondary current measured. The difference observed during the ZVS transitions is due to the current through the transformer's parasitic capacitances, that is included in i_{mag} but not in i_{SW}.

Overall, these measurements validate the functionality of the 2L-AHBF power stage. The converter operates in ZVS mode as expected, while the voltage and current waveforms can be well described using the analysis of the power stage conducted in Chapter 2.

5.2.2 3L-FC-AHBF configuration

The measured control signals of the 3L-FC-AHBF are plotted in Figure 5.7. Two PWM signals are generated by the pulse generator with a phase-shift close to 180° and a similar duty-cycle. Each of the PWM signals is then used to create the signals driving the two half-bridges of the power-stage ($S1/S4$ and $S2/S3$). The input PWM signals are not measured due to the limited number of channels on the scope.

Like for the 2L-AHBF, it is possible to set the dead-time value between the turn-off instant of a switch and the turn-on instant of the complementary switch.

As a reminder, the power stage of the 3L-FC-AHBF is shown in Figure 5.8 with the measured currents and voltages highlighted.

The power stage current and voltage waveforms are plotted in Figure 5.9 for the following set of parameters: $V_{in} = 800$ V, $V_{out} = 12$ V, $P_{out} = 1$ W, $f_{sw} = 475$ kHz and the transformer design #1. Note how the switching frequency of the power switches is almost divided by two with respect to the 2L-AHBF. The same voltage and current waveforms are measured using the same probes as in the 2L-AHBF configuration.

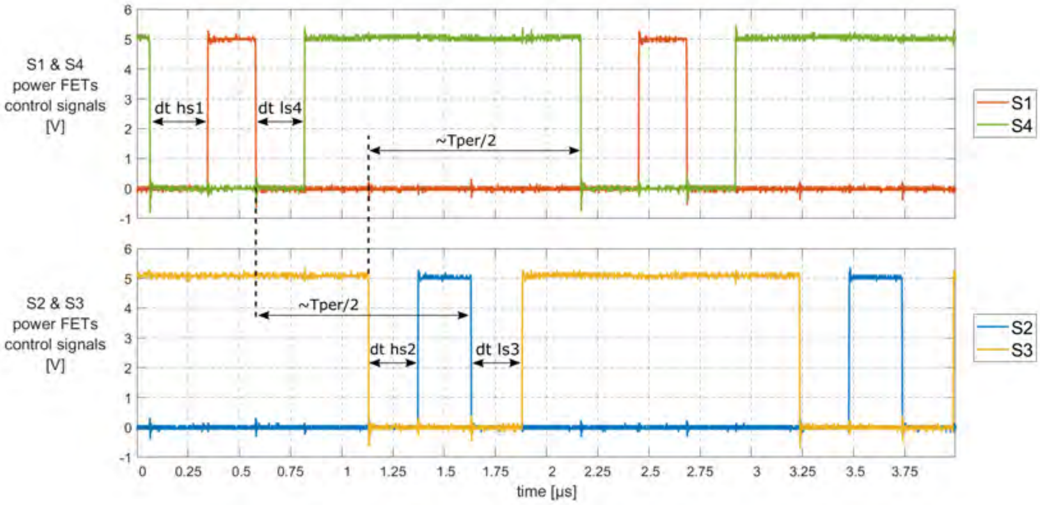


Figure 5.7: 3L-FC-AHBF - Experimental control signal waveforms

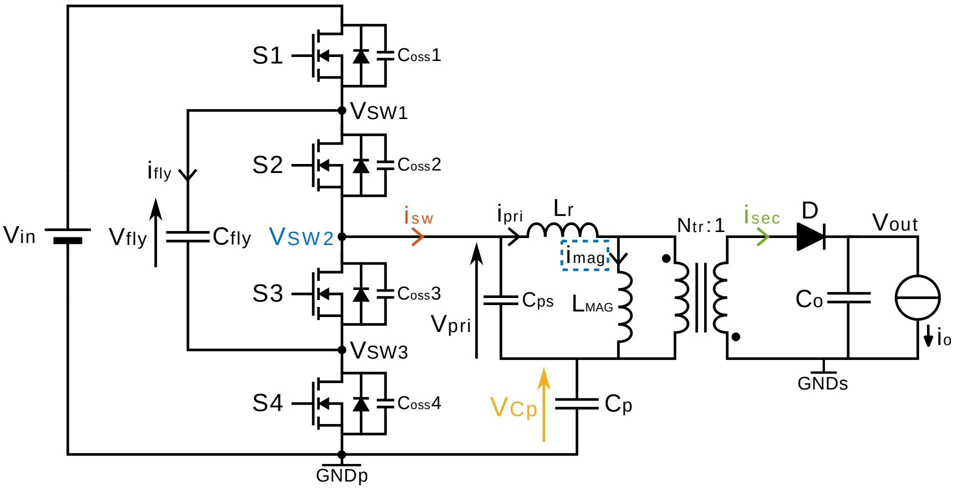


Figure 5.8: 3L-FC-AHBF power stage

The middle switching node V_{SW2} confirms the converter still operates in ZVS mode, as the transitions from its low-voltage states to its high-voltage states are still slow. However, it also reveals that the voltage across the flying capacitor (V_{fly}) is not exactly close to its ideal value ($V_{in}/2$) as V_{SW2} high-voltage values are slightly different during the two-half periods.

The voltage across the primary capacitor V_{Cp} has a value that is close to the one measured in the 2L-AHBF configuration ($V_{Cp} = 191$ V). It is expected since the transformer design #1 is the same and the targeted output voltage is the same.

The current through the switching node (i_{SW}) and the secondary current (i_{sec}) are also both quite similar to the ones measured in the 2L-AHBF converter.

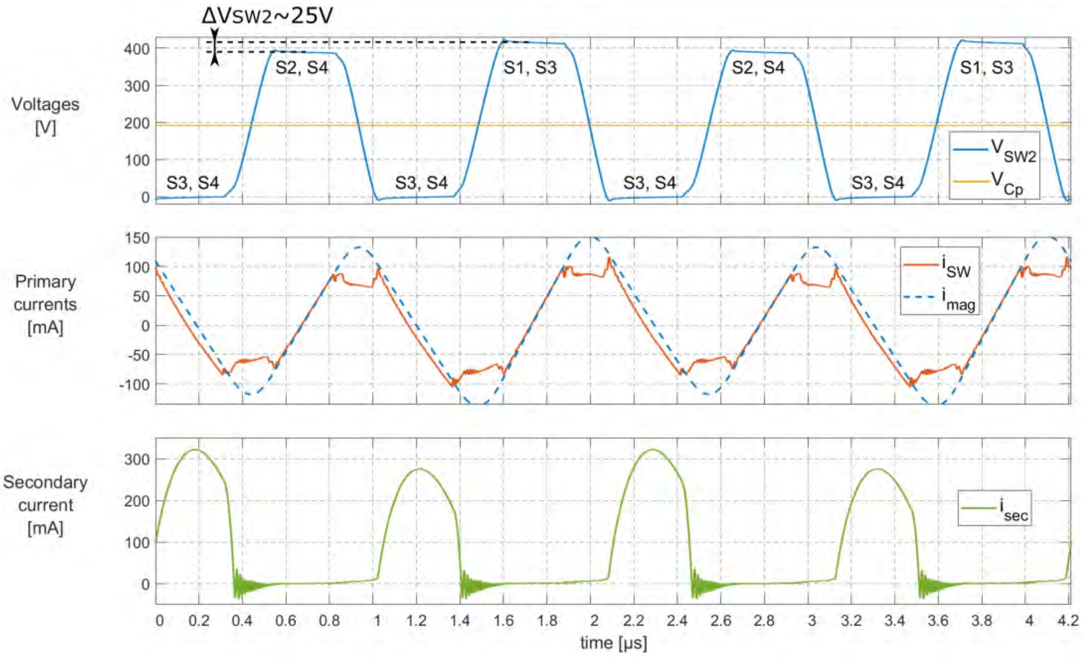


Figure 5.9: 3L-FC-AHBF - Experimental power stage waveforms with 180° phase-shift

The flying capacitor voltage can be estimated measuring V_{SW2} when $S1$ is ON and when $S2$ is ON. A voltage difference close to 25 V is measured between the two voltages, so the flying capacitor voltage is estimated to be close to 387 V (instead of 400 V). Even though this value is good enough to ensure a regular voltage stress is applied on the switches (smaller than their breakdown voltage), it could lead to other issues like increased losses (due to larger secondary current, larger voltage across the transformer) or increased EMI (due to the asymmetry between the two half-periods).

To overcome this issue, the phase-shift between the two input PWM signals is slightly changed (177° instead of 180°) and the duty-cycle of the PWM signal associated to $S1/S4$ half-bridge is slightly increased (24.7% for $S1$ vs 23.8% for $S2$). It allows to balance the time during which the power switches are effectively on. The waveforms obtained with these modifications are plotted in Figure 5.10. The flying-capacitor voltage appears to be much closer to its ideal value in this new configuration, as the difference between V_{SW2} high-voltage values is now smaller than 5 V. So the little changes in the control signals seem to allow the flying capacitor voltage to remain very close to its ideal value despite the fact the converter operates in open loop.

A possible cause of the imbalance observed with a 180° phase-shift is that the quantity of parasitic capacitance that is (dis)charged during the ZVS transitions is not the same for the two half-bridges. If the parasitic capacitance of the power FETs is well-balanced (each half-bridge being composed of two power switches which are all quite similar), the same thing is not true for the other components connected to the IC bricks, like the digital isolators and the bootstrap circuits.

For example during a ZVS transition, the $S1/S4$ half-bridge needs to charge the isolation parasitic capacitor of three digital isolators while $S2/S3$ half-bridge only has one to charge. Due to the low total capacitance value, a small mismatch between the half-bridge switching

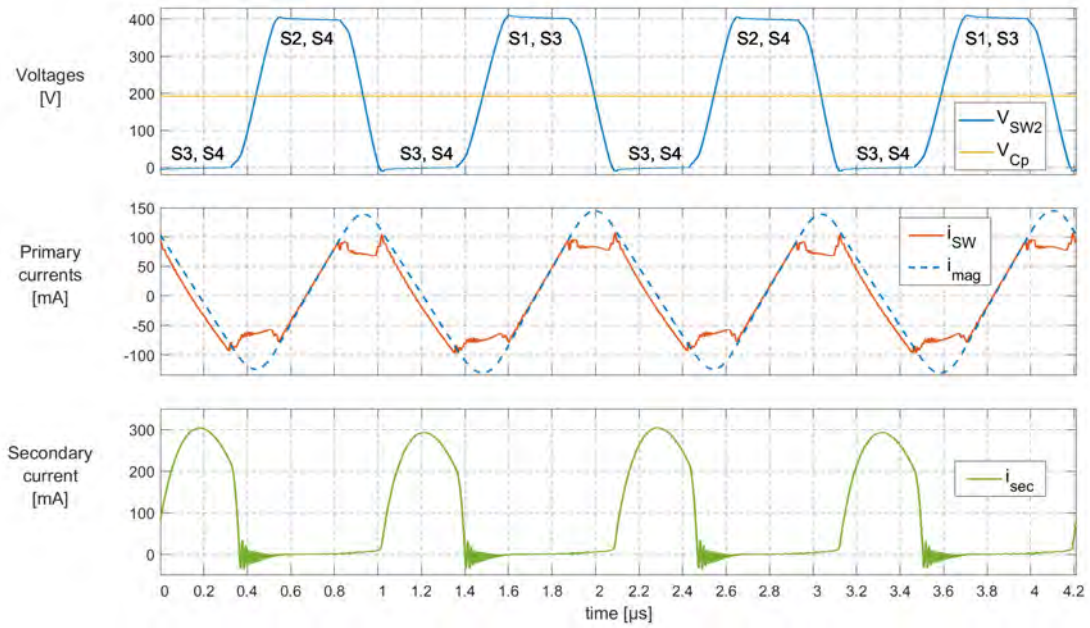


Figure 5.10: 3L-FC-AHBF - Experimental power stage waveforms with corrected phase-shift

capacitor can lead to a significant imbalance in the flying capacitor voltage, which is what is observed here. Because the more capacitance to charge, the slower the ZVS transitions and the shorter the switches on-time. If the on-time of the switches is not balanced, it leads to an imbalance in the charge flow of the flying capacitor and thus to a voltage different than the ideal value (as discussed in Chapter 2).

Nevertheless, despite this issue with the flying capacitor voltage balancing, the 3L-FC-AHBF stage behaves as predicted by the analysis done in Chapter 2. Therefore, the functionality of both power stages is validated by the first measurement results, which allows to evaluate and measure more in details the ZVS mechanism of the converter.

5.3 ZVS mechanism and frequency optimization

In Chapter 4, it was determined that the converter should operate at the limit of ZVS mode to decrease the primary current ripple while keeping low switching losses. Before studying the limit of the ZVS mode, the current and voltage waveforms during the ZVS transitions are analyzed, to evaluate the converter's parasitic capacitors and compare them to the one predicted by the previous analysis and measurements.

5.3.1 Currents and parasitic capacitors

In the converter's theoretical analysis, the role of different parasitic capacitors during ZVS transitions was studied. Measuring the current and voltage variations on the primary side of the transformer, it is possible to evaluate the total quantity of parasitic capacitors in the different portions of the power-stage. In particular, two different parasitic capacitors can be evaluated and compared to their expected value: the transformer parasitic capacitor referred to the primary (C_{TR}), that is the sum of the mutual capacitance and the self capacitance (as discussed in Chapter 4), and the switching node total parasitic capacitance (C_{SW}), that accounts for all the parasitic capacitors connected to the switching node - except the transformer parasitic capacitance.

During the ZVS transition of the HS FET, V_{SW} rises and it is possible to estimate its slew rate. In the 2L-AHBF configuration, for the operating point shown in Figure 5.6, the slew rate is measured at halfway of the ZVS transition, at $t = t_{mr}$ when $V_{SW} = V_{in}/2 = 200$ V.

$$\frac{dV_{SW}}{dt}(t_{mr}) = 2.3 \text{ V/ns} \tag{5.3}$$

At the same time, the current in the switching node i_{SW} is measured and the magnetizing current i_{mag} value is estimated:

$$i_{SW}(t_{mr}) = -61 \text{ mA} \quad (5.4) \qquad \text{and} \qquad i_{mag}(t_{mr}) = -114 \text{ mA} \quad (5.5)$$

Moreover, the relation between the current and the voltage variations across a capacitor can be written as:

$$i_C = C \cdot \frac{dV}{dt} \tag{5.6}$$

Using the measurement values and the expression (5.6), the two types of parasitic capacitor can be estimated:

$$C_{SW} = \frac{|i_{SW}|}{\frac{dV_{SW}}{dt}} = 27 \text{ pF} \quad (5.7) \qquad \text{and} \qquad C_{TR} = \frac{|i_{mag} - i_{SW}|}{\frac{dV_{SW}}{dt}} = 23 \text{ pF} \quad (5.8)$$

The value of the transformer parasitic capacitor C_{TR} can be compared to the sum of the mutual and self capacitor measured at the end of Chapter 4 for the different transformer designs. The design #1 used here features $C_{ps} = 12$ pF and $C_{self-p} = 11$ pF, which correspond quite well to the measurement results. Note that the operation was repeated for different transformer designs and for each of them the extracted C_{TR} was either close to the sum of the mutual and the self capacitors or slightly lower.

On the other end, C_{SW} is the sum of all the parasitic capacitors connected to V_{SW}. The main contributors are the power MOSFETs output capacitors ($C_{oss1,2} = 12$ pF at $V_{DS} = 200$ V). The voltage probe capacitance should be taken into account ($C_{probe} = 2.5$ pF). The sum of these capacitances is equal to 26.5 pF which is close enough to the value extracted from the measurements.

However, if the parasitic capacitors of the bootstrap circuits, of the digital isolator and of the PCB tracks are also considered, then the measured parasitic capacitance is actually lower than the expected value. No clear explanation was found for this, it could be due to the limited accuracy of the dV/dt estimation, to the current measurements or to some inaccuracy in the C_{oss} measurements (this is discussed more in details in the section dedicated to the analysis of the converter performances).

Still considering the 2L-AHBF configuration, the same calculation can be done for the other ZVS transition (when V_{SW} is falling) and the results obtained are quite similar ($C_{SW} = 26$ pF, $C_{TR} = 24$ pF).

In the 3L-FC-AHBF configuration, similar computations can be done using the waveforms shown in Figure 5.10 - obtained with a corrected phase-shift and an almost ideal flying capacitor voltage. The ZVS transition that precedes the HS FET $S1$ turn-on leads to the following results: $C_{SW} = 33$ pF, $C_{TR} = 24$ pF. However, the ZVS transitions occurring before HS FET $S2$ turn-on gives: $C_{SW} = 25$ pF and $C_{TR} = 23$ pF. The difference between the value of C_{SW} during these two transitions confirms that the imbalance of the flying capacitor might be due to the different quantity of parasitic capacitor on the switching node.

Overall, despite the little error on C_{SW} estimation, the capacitances extracted from the measurements tend to match well the values predicted by the power stage analysis and the transformer measurements. Although the limited accuracy of the measurements (due to ringing on i_{SW} and V_{SW}) does not allow to compute the values of capacitance with a great accuracy, it confirms the analysis of the main capacitive contributors to be taken into account during ZVS transitions.

5.3.2 Optimization of the switching frequency

To decrease the primary current ripple and improve the converter efficiency, it is interesting to increase the switching frequency up to the limit of the ZVS mode.

Monitoring the same power stage waveforms as earlier, it is possible to identify if the converter operate in ZVS mode or not. Figure 5.11 shows the measured waveforms if the power stage fails to operate in ZVS mode. Even though the V_{GS} voltage of the high-side FET is not measured, the moment when it turns on is clearly visible. It creates a little voltage step on the switching node V_{SW}, suddenly forcing it to reach V_{in}, and it also generates a peak and some ringing in the i_{SW} current waveform. These waveforms contrast with the ones in Figure 5.6 where the power FETs turn-on has no visible impact on the voltage and current on the primary side.

The loss of the ZVS mode revealed from these waveforms is due to the lack of energy stored in the magnetizing inductance when the LS FET turns off. As the energy stored is too low, i_{SW} becomes null and starts changing direction before the end of the ZVS transition. Therefore the switching node never reaches its high-voltage state and so the HS FET is turned-on and V_{SW} is pulled up for the last few volts.

For the designs operating at high-frequency ($f_{SW} > 800$ kHz), the limit of the ZVS mode is actually not related to the current i_{SW} becoming to small to complete the ZVS transitions, but rather to the duration of the transitions. Since the effective duty-cycle of the HS FET (computed using Eq. 5.9) is fixed, if the ZVS transition takes too long to complete (dt_{HS} and dt_{LS} become too large) then the time during which the HS FET is effectively ON ($t_{on\ HS}$) becomes shorter than the minimum on-time targeted in Chapter 3 and required to ensure the IC brick's functionality.

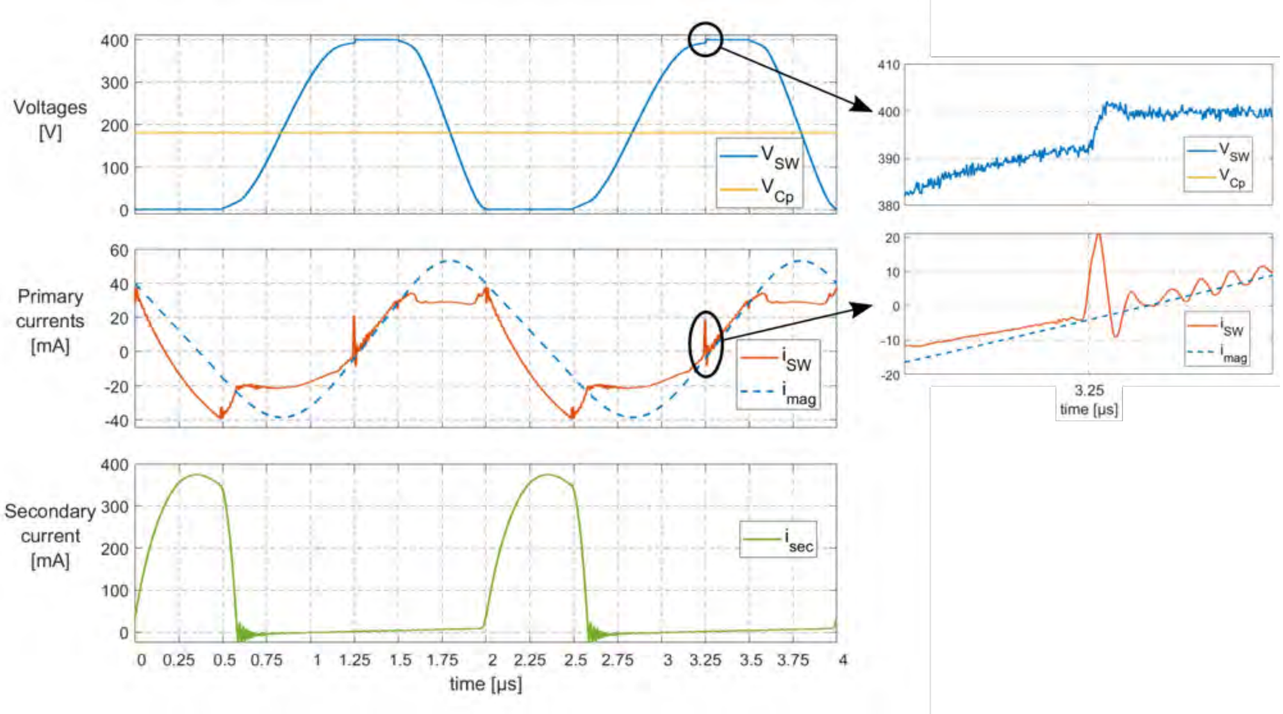


Figure 5.11: 2L-AHBF - Experimental power stage waveforms in hard-switching mode

$$D_{eff} \approx N_{TR} \cdot \frac{V_{out} + V_D}{V_{in}} \quad (5.9) \qquad D_{eff} \cdot T = t_{on\ HS} + \frac{1}{2} \cdot (dt_{HS} + dt_{LS}) \quad (5.10)$$

To avoid losing the ZVS mode, the converter should switch at a lower frequency (to increase the period T) or a smaller magnetizing inductance should be used. Both would lead to an increase in primary current ripple, thus a larger amount of energy would be stored inside the magnetizing inductance at the dawn of the ZVS transition, ensuring it can be fully completed.

For a given transformer design and a given value of the primary inductance, a sweep of the switching frequency is conducted. The RMS value of i_{SW} is measured, along with the converter efficiency. The converter behavior is also monitored to identify the frequency that is related to the limit of the ZVS mode. Then, the value of the primary inductance is changed modifying the air-gap added to the magnetic core and the same measurements are conducted. The results are plotted in Figure 5.12 and Figure 5.13.

Results in Figures 5.12 and 5.13 confirms that increasing the switching frequency of the converter (for a given L_{pri}) allows to decrease the primary current ripple and to improve the converter efficiency. Increasing the switching frequency beyond the limit of the ZVS mode can help to further improve the converter efficiency but it might also degrade its performances on other aspects, like EMC. For this reason, the efficiency data points discussed and shown in the next sections are the one measured at the limit of the ZVS mode, i.e. the dashed black line in the Figure 5.12 and 5.13.

It is possible to plot the same type of curves for the 3L-FC-AHBF converter operating at 800 V with the same transformer (design #1). Results are shown in Figure 5.14. The switching frequency displayed on the axis is the one of the middle switching node (V_{SW2}) so it is the double of the power switches operating frequency.

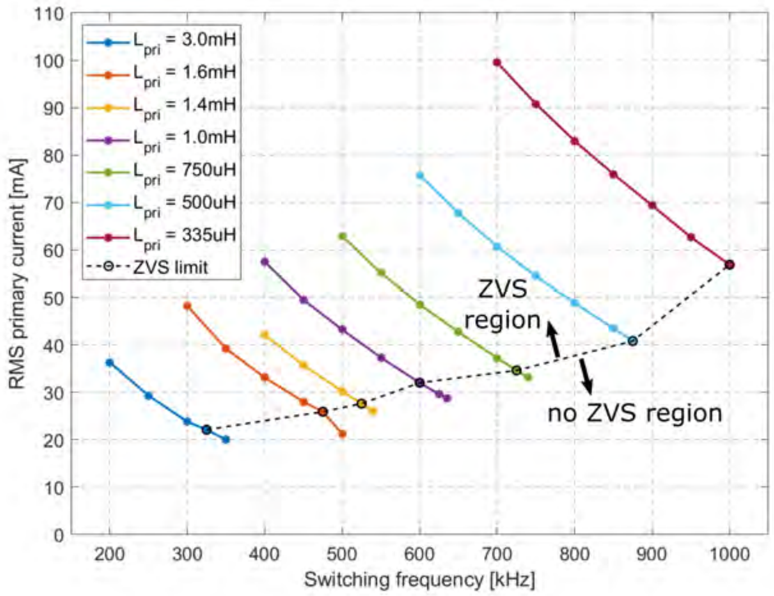


Figure 5.12: $(i_{SW})_{RMS}$ vs f_{SW} for different values of L_{pri} (2L-AHBF - design #1)

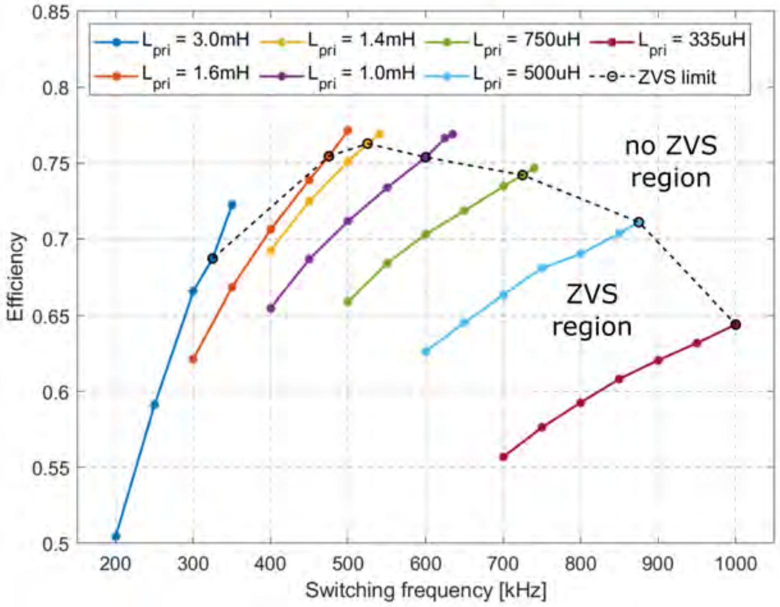
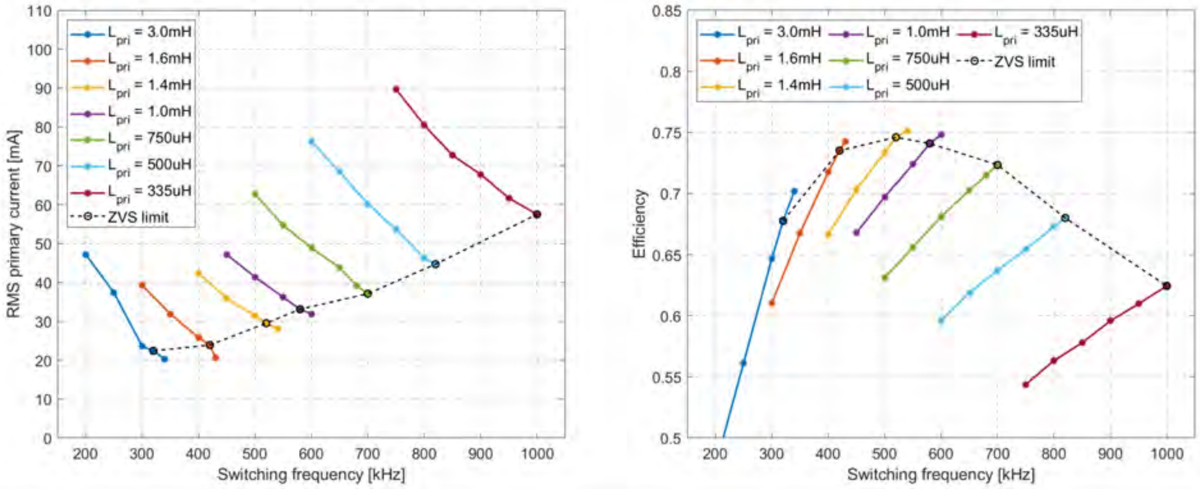


Figure 5.13: Efficiency vs f_{SW} for different values of L_{pri} (2L-AHBF - design #1)

The results in Figure 5.14 are similar to the ones obtained in the 2L-AHBF configuration: this confirms that their behavior is almost identical. The maximum frequency for a given L_{pri} is slightly lower in the 3L-FC-AHBF configuration, probably due to the additional capacitances added by the more complex power stage. Overall, the conclusion is the same as for the 2L-AHBF: for a given value of $Lpri$, increasing the switching frequency up to the ZVS limit clearly helps improve the converter efficiency.



(a) (b)

Figure 5.14: (a) $(i_{SW})_{RMS}$ vs f_{SW} and (b) efficiency vs f_{SW} for different values of L_{pri} (3L-FC-AHBF - design #1)

Maximum frequency: comparison of model's predictions and measurements

To validate the predictions of the simple converter model (described in Chapter 4) regarding the maximum frequency that can be reached for a given L_{pri}, it is possible to compare the predictions to the measured values. Figure 5.15 shows how the maximum switching frequency is related to the primary inductor value according to the model and the measurement results. It turns-out the two curves are very close, which confirms the model can predict with a good accuracy the behavior of the converter. Results plotted in Figure 5.15 are for the 2L-AHBF configuration and transformer design #1.

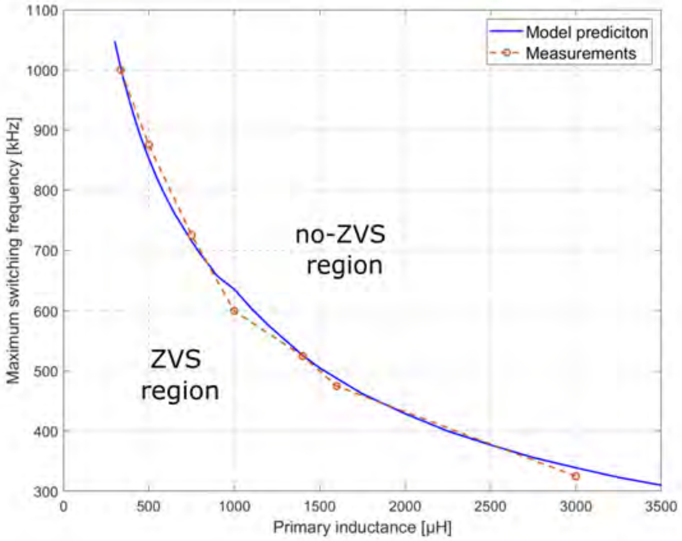


Figure 5.15: Comparison of model predictions and measurements for the maximum f_{SW} value at L_{pri} value

5.4 Transformer designs

The objective of this section is to measure the converter performances obtained for various transformer designs and to compare the results to study the influence of several design parameters and conclude on how to select a high-performance transformer. The various transformer designs studied are the one selected in Chapter 4 with a Design-of-Experiment (DoE). As a reminder, their main characteristics are summarized in Figure 5.16, while their measured characteristics are detailed in Table 4.3 at the end of Chapter 4.

To monitor the converter performances, its efficiency is estimated from the measurements of the main input voltage/current and the the output voltage/current. The data points are measured at the limit of the ZVS mode, as highlighted previously. All measurements are performed on a 2L-AHBF power stage operating with $V_{in} = 400$ V, $V_{out} = 12$ V and $P_{out} = 1$ W.

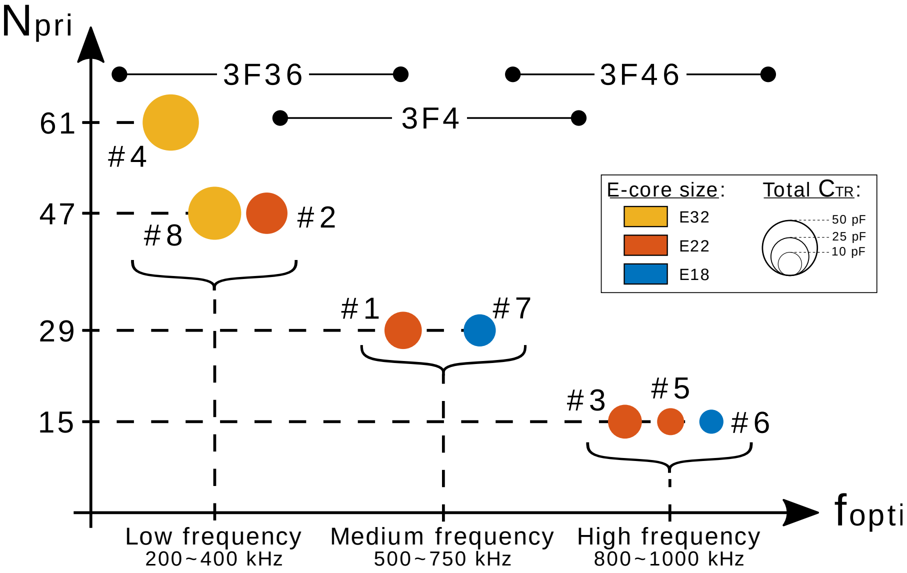


Figure 5.16: DoE - Summary of the selected designs

Several aspects of the transformer design discussed in Chapter 4 are measured through the comparison of the performances of several designs: the influence of the core material, the core size, the number of turns and their arrangement on the PCB layers of the planar transformer.

5.4.1 Core material

Three materials (3F36, 3F4 and 3F46) were considered in the DoE, as their loss model is not complete enough to compare them efficiently using the simple model built. The transformer design #1 is used to compare the performance of the three materials. For each of them, the evolution of the converter's efficiency with the switching frequency is presented in Figure 5.17.

Results show that the 3F46 material seems to offer the best performances on all the frequency range. It is particularly clear for the low-frequency data points, where the core losses are dominant, that it helps improving the converter's efficiency (81.1% peak efficiency is reached around 475 kHz). The 3F36 material is also interesting as it allows to reach lower frequency operating points thanks to its higher magnetic permeability.

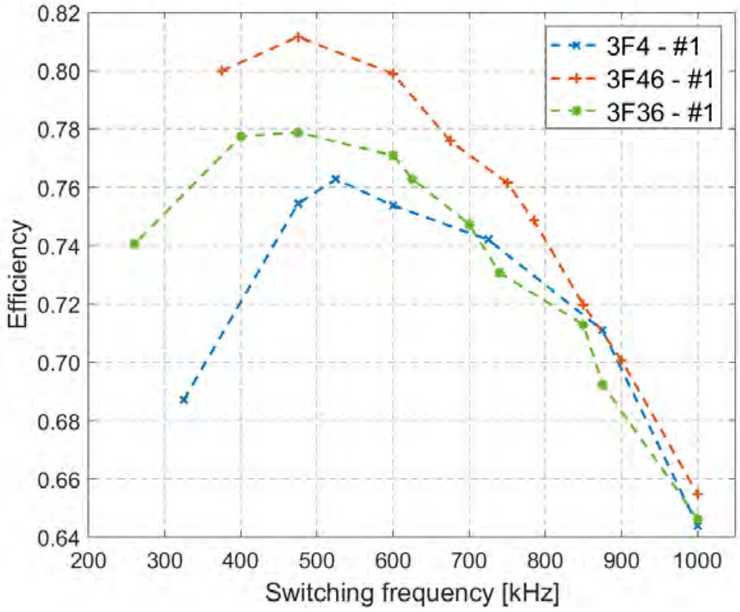


Figure 5.17: Efficiency vs f_{SW} for different core materials (in design #1)

For high frequency data points, the performances of the three materials are quite close and quite low, even though the 3F46 remains slightly more efficient at 1 MHz. The reason is probably not related to the choice of the magnetic core material - this is discussed more into details in a later section.

In conclusion, it appears that 3F46 material offers the best performances so it should be selected in priority. If it is not possible (3F46 is not available for some core sizes, at least when measurements were being done), the 3F36 material should be the second option, as it should lead to better performances than the 3F4 core material.

5.4.2 Number of turns

To analyze the influence of the number of turns of the transformer primary on the performances of the converter, the efficiency is measured for designs with the same transformer size and core material. The results plotted in Figure 5.18 are obtained with designs #1, #2 and #3, built using an E22 core. The designs #4 and #8 use a larger E32 core and their performances are presented in Figure 5.19.

As stated at the end of Chapter 4, the various transformer designs can be ranked in three families depending on their number of turns:

- Designs with a high number of turns (#2, #4 and #8) intended to work at low-frequency ("LF" solutions)
- Designs with a low number of turns (like #3) intended to work at high-frequency ("HF" solutions)
- Designs with a medium number of turns (#1) to operate at medium frequency ("MF" solutions)

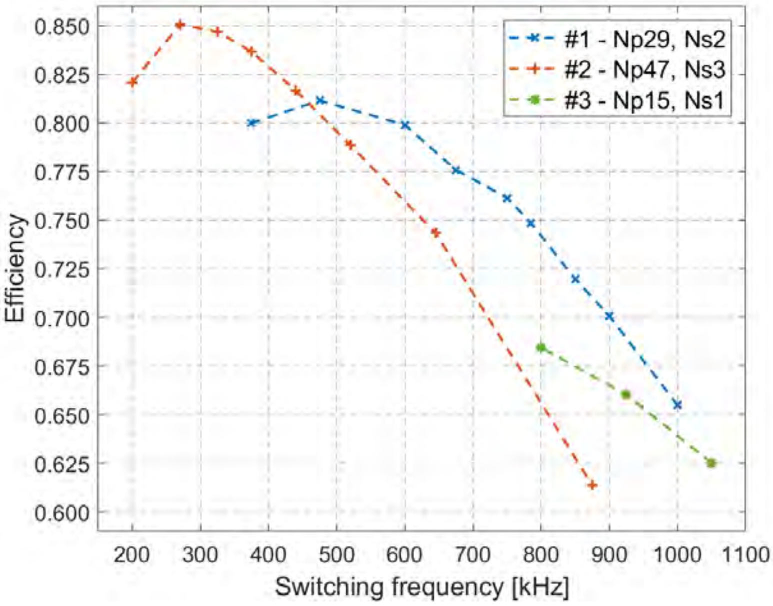


Figure 5.18: Efficiency vs f_{SW} for different N_{pri} (E-core used: E22 in 3F46)

The designs with a high number of turns (LF) seem to offer very good performances at low switching frequency: #2, #4 and #8 allow to reach $\eta \approx 85\%$ for 1 W output, which means their losses are quite small. However, as soon as the switching frequency increases, the efficiency of these solutions severely drops. This can be partially imputed to the increase in the current flowing in the primary side of the transformer (shown in Figure 5.12), that generates high conduction losses in the primary winding - since its resistance is large due to the high number of turns.

As the switching frequency increases, the solutions with a smaller number of turns (MF) become more interesting than the LF solutions, due to their smaller resistance. Note how design #1 efficiency is higher than the one of design #2 as soon as $f_{sw} > 450$ kHz. However, if the switching frequency increases more, the efficiency obtained with MF designs also drastically drops.

More surprisingly, the same phenomenon is observed for the designs with a low number of turns (HF, like #3) that should, at the opposite, gain efficiency as the switching frequency increases. Yet it is the contrary that happens as the maximum efficiency is obtained for the lowest frequency operating point - which is already quite high (800 kHz) since the maximum inductance that these designs can present is limited, due to their low number of turns. But a higher switching frequency should allow to decrease the core losses, that should be dominant for these designs as their low number of turns translate into an increased flux density, so these low-efficiency results are puzzling.

Although increasing the number of turns seems to improve the converter's efficiency, there is a limit to the efficiency gain as shown by the results in Figure 5.19. As the number of turns (for the primary winding) increases from 47 for design #8 to 61 for design #4, the efficiency associated with the two designs does not significantly improve ($\eta_{peak} = 85.1\%$ for #8 vs $\eta_{peak} = 85.5\%$ for #4). If increasing the number of turns allows to reduce the core losses (that

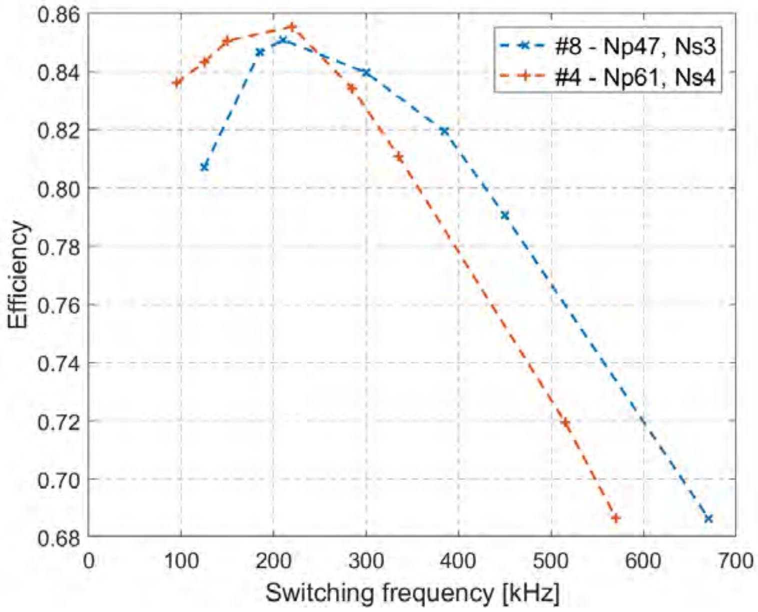


Figure 5.19: Efficiency vs frequency for different N_{pri} - E-core used: E32 in 3F36

are dominant for this converter, particularly at low frequency), it also leads to an increased winding resistance and thus to larger conduction losses. So there is no clear interest for going to solutions with a very large number of turns, especially as it requires to increase the core size which contradicts with the small-size constraints of the final converter.

Overall, the solutions with a large number of turns are the ones that enable the best converter's efficiency. There is a shift observed between the expected optimal frequency of a design family and the frequency for which the maximum measured efficiency is reached. This shift is particularly noticeable for MF and HF solutions, that are supposed to perform better at high frequency which is not what is observed. A later section is dedicated to investigate the origins of the extra losses at high frequency.

5.4.3 Core size

Three different E-core sizes are compared: E18, E22 and E32. To study the influence of the core size on the converter performances, designs with different core sizes but the same number of turns and core material are compared. The results for the E22/E32 comparison are shown in Figure 5.20 and the results for the E18/E22 comparison are plotted in Figure 5.21.

The results of both comparisons confirm that increasing the core size allows to improve the converter efficiency. However, for some specific designs, the influence of the core size on the performances can be rather small.

Looking at the E22/E32 comparison, the best efficiency is reached using an E32 core ($\eta_{peak} = 85.1\%$), although the difference between E32 and E22 peak efficiency is not large. For a high frequency operating point, the results for the E22 core even become better than the ones for the E32 core, due to the larger parasitic capacitor of the last one that lower its performances at high frequency.

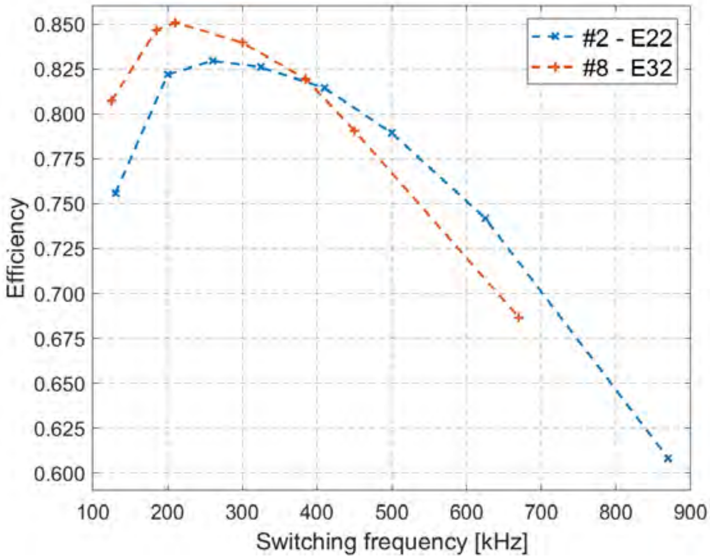
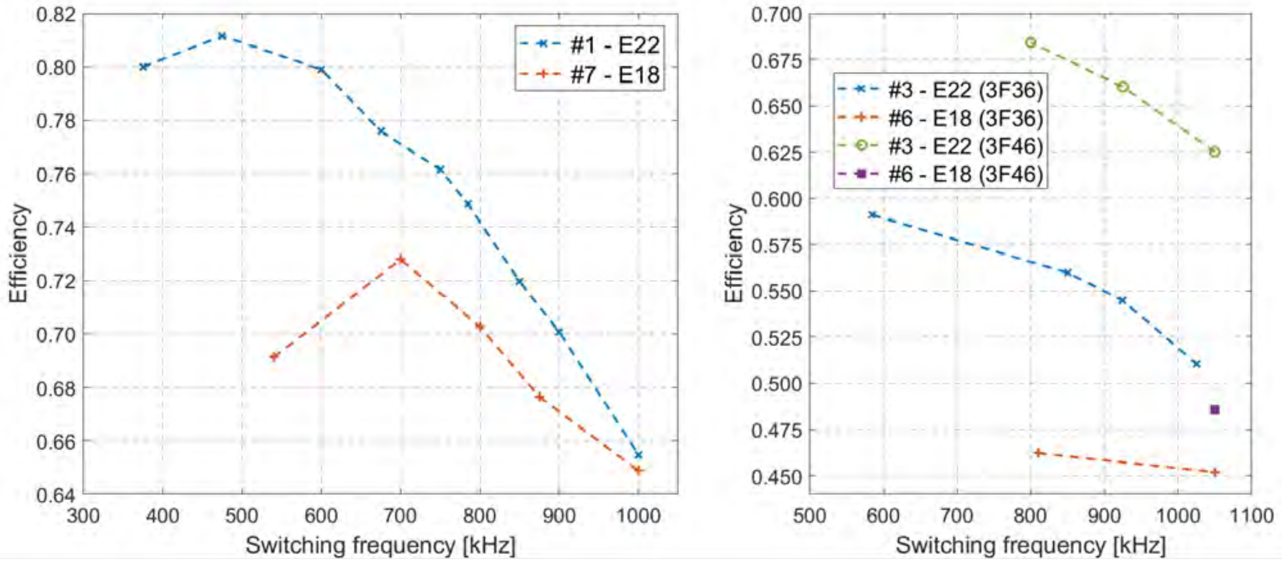


Figure 5.20: Efficiency vs f_{SW} for LF designs (with Np47, Ns3 with 3F36 core)

Moreover, the available core material associated to each core size should also be taken into account. For example, E32 core in 3F46 does not exist (as it is reserved for small E-cores), while E22 in 3F46 can be found. So the performances of the E22 core can be further improved by changing its material (3F46 instead of 3F36 in Figure 5.20). In the end, E22 performances using a better material become similar to the ones obtained with E32 and a similar peak efficiency can be reached ($\eta_{peak} = 85.0\%$). So the difference in efficiency is almost negligible while the core size increase going from E22 to E32 solutions is rather significant.



(a) (b)

Figure 5.21: Comparison of efficiency vs f_{SW} for (a) MF designs (Np29, Ns2 with 3F46 core) ; (b) HF designs (Np15, Ns1 with 3F36 and 3F46 core)

For E22 vs E18, two comparisons are being made: one between MF designs (Figure 5.20(a)) and the other between HF designs (Figure 5.20(b)). For HF designs, E18 is clearly too small to allow a good efficiency and the difference with the E22 is quite important. Even changing the core material does not help as the efficiency remains below 50% with design #6. For MF designs, E22 is better than E18 but as the frequency increases, the difference between E22 and E18 design's performances become smaller (only 0.5% difference in efficiency at 1 MHz). However, the peak efficiency reached with the E22 design #1 remains higher than for the E18 design #7 ($\eta_{peak} = 81.2\%$ vs $\eta_{peak} = 72.8\%$).

Overall, the E22 core size seems to offer a good trade-off between the size and the efficiency of the converter. However, solutions using E18 core could also be an interesting alternative as the performances at high-frequency are similar to the ones of solutions using E22 core and the use of E18 core would enable a significant reduction in the transformer footprint (-33%).

5.4.4 Winding arrangement

In Chapter 4, the main arrangement of the windings on the PCB was presented with the two top layers for the primary winding and the bottom layer for the secondary winding. It is used for all the transformer designs except for design #5. The last one has all its primary turns regrouped on the top layer and the secondary winding on the bottom layer. It allows to further decrease the mutual capacitance (C_{ps}) as well as the primary self capacitance ($C_{self\ p}$), and so to increase the maximum switching frequency.

To evaluate the impact of the alternative layer arrangement, design #5 is compared to design #3 that uses the original arrangement and has the same number of turns. Results are plotted in Figure 5.22.

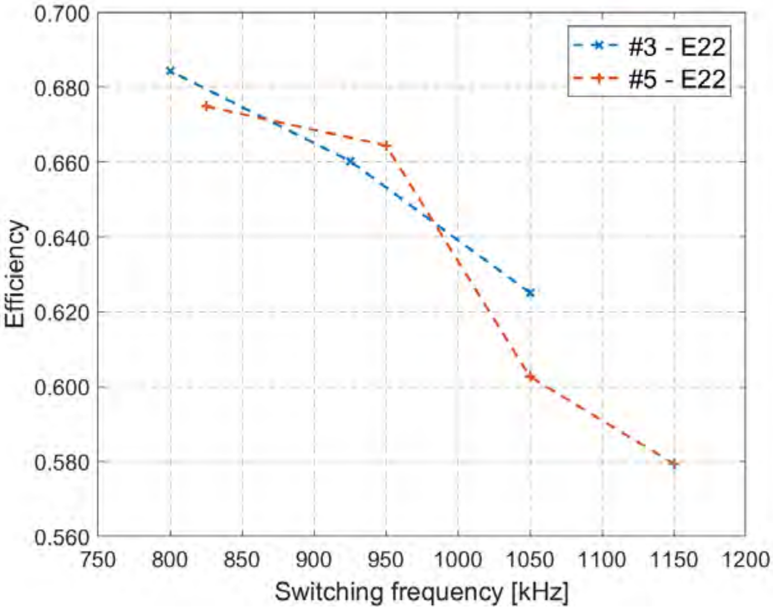


Figure 5.22: Efficiency vs f_{SW} for two designs with different layer arrangements

No major differences appear in the efficiency between the two designs. The design #5 has a switching frequency that is higher than for design #3 with a similar inductance value (or a similar frequency with a higher inductance value). However, both designs show a low efficiency, that is probably due to the same phenomenon that degrades efficiency of all HF designs. Due to these high losses (that were not expected) it is difficult to conclude on the interest of one design or the other.

5.4.5 Conclusion on the transformer designs

The comparisons built between the various transformer designs show some interesting leads on how to build an efficient transformer for the targeted HVLP converter. The 3F46 material has the lowest core losses, the E22 core shows the best trade-off between size and performances - although the E18 could offer an interesting alternative for HF solutions. Regarding the choice of the number of turns, only the LF solutions (with a large number of turns) offer good performances. The MF and HF solutions' efficiency is largely degraded (compared to the converter model predictions) so they appear to be less interesting.

5.5 Converter performances

The objective of this section is to study the performances of the two converters configurations: the 2L-AHBF operating at 400 V and the 3L-FC-AHBF operating at 800 V.

In the next paragraphs, the only indicator of a converter performances that is monitored is its efficiency. Many other parameters could be interesting to observe (EMC, output voltage ripple, etc.) but the time constraint as well as the vague specifications of the targeted converter made it difficult to add them in the analysis.

The monitored efficiency is computed as the ratio of the power sunk on the output by the electronic DC load to the power delivered by the main input voltage supply. It does not account for the power supplied to the IC bricks and their auxiliary circuits. The reason for not including this auxiliary power in the efficiency computation is because it is largely impacted by the external components added around the IC bricks (like the digital isolators), that are required due to the failure of some of the IC's internal blocks.

First, the performances of the converters for few transformer designs are monitored, in nominal operating mode but also changing some external parameters. Then, the difference between the expected and the measured performances is studied and the potential origins of the extra-losses observed at high-frequency are investigated and discussed. In the end, the performances of the converters are compared to solutions from the State-of-Art to conclude on the interest of the created solutions.

5.5.1 Overall results

Some of the transformer designs analyzed in the previous section are used to measure the converter efficiency for the 3L-FC-ABHF configuration. These designs are selected as follows: one from each solution "family" (#2 for LF, #1 for MF and #3 for HF) and at least one for the different core sizes (#7 for E18, #8 for E32, #1, 2, 3 for E22). All the transformer designs use cores in 3F46 material, except for design #8 in 3F36 material.

Nominal operating mode

First, the performances of the 2L-AHBF and the 3L-FC-AHBF are measured in their nominal operating mode: $V_{in} = 400$ V or 800 V, $V_{out} = 12$ V, $P_{out} = 1$ W. Like for the previous measurements, the efficiency is measured at the limit of the ZVS mode for different values of primary inductor, to monitor the evolution of efficiency with the operating frequency. The results for the 2L-AHBF and the 3L-FC-AHBF configurations are plotted in Figure 5.23 and in Figure 5.24 respectively.

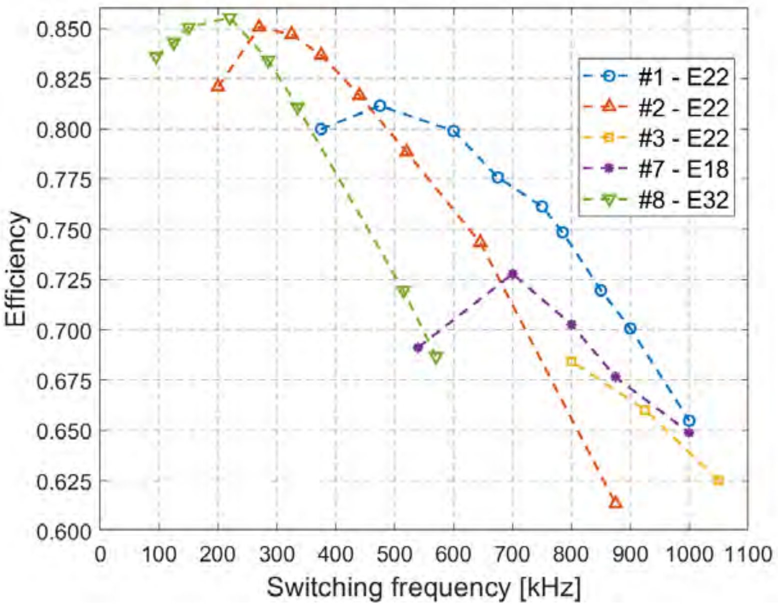


Figure 5.23: Efficiency vs f_{SW} for the 2L-AHBF configuration

The efficiency of the 2L-AHBF configuration was already discussed when comparing the transformer designs, so the outcome is the same: best designs operate a low-frequency with a large number of turns (#2, #8).

Regarding the 3L-FC-AHBF, as expected from the converter loss analysis (done in Appendix B), the efficiency values measured for the various transformer designs are comparable to the ones obtained with the 2L-AHBF. However, the performances for the 3L-FC-AHBF are in general slightly lower than for the 2L-AHBF. It can be due to the fact that the 3L-FC operates with a slightly lower frequency (due to the additional parasitic capacitors and to the flying capacitor imbalance) but also to the additional power switches in the 3L-FC-AHBF power stage, that generate additional conduction losses with respect to the 2L-AHBF.

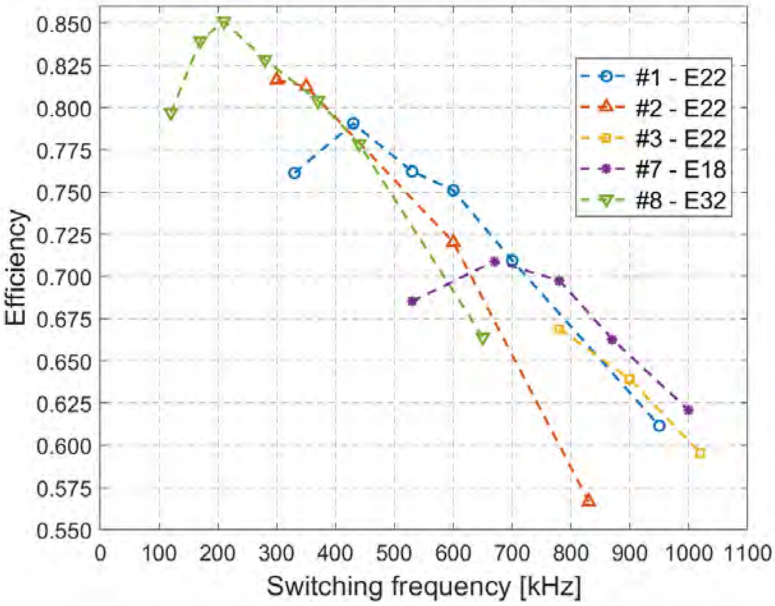


Figure 5.24: Efficiency vs f_{SW} for the 3L-FC-AHBF configuration

Different load conditions

Overall, for both configurations, it appears that only a limited number of designs allow to reach the targeted efficiency ($\eta \geq 85.0\%$). The main reason for the low efficiency (beside the high-frequency additional losses not included in the model) is that the majority of the losses in the converter are constant (i.e. they do not depend on the output power). Since in nominal operating mode, the amount of power supplied to the output is very low (1 W), it is difficult to reach a high efficiency. So if the output power increases, the efficiency of the converter should improve. It could be interesting to monitor the evolution of the efficiency with the output power for few reasons.

First, the specifications of the targeted application of the HVLP converters are still quite vague. A 1 W output load was considered in a first step, but it could be that some systems require 2 W or 3 W. Then, even if the required output power is limited to 1 W (or lower), some advanced control techniques can be implemented to sink a larger output power sporadically to operate the converter at its optimal operating point. They are often used to improve the converter efficiency at light load [4, 88, 89, 90]. Monitoring the evolution of the efficiency with the output power would show if these techniques can be of some interest for the HVLP converter. Finally, it should be interesting to notice the evolution of the efficiency with the output power for the selected transformer designs, to identify which could be used for applications requiring a larger output power and which one have their optimum operating point closer to 1 W.

The evolution of the efficiency with the output power is plotted in Figure 5.25 for the 2L-AHBF and 3L-FC-AHBF configurations. The output power ranges between 0.5 W and 4 W, the high power limit being defined by the maximum RMS current rectified in the secondary diode D_{sec}.

The measurement results confirm that an increased output power translates into a higher

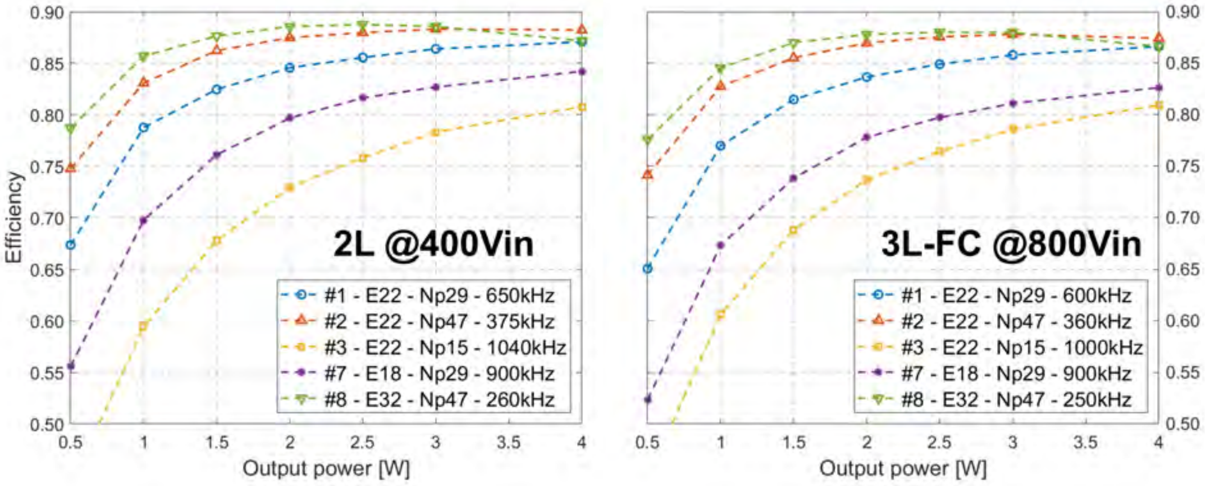


Figure 5.25: Evolution of converter's efficiency with output power

efficiency for both configurations and for the various transformer designs. It can be noticed that the efficiency gain is larger for the designs that show a low efficiency for a 1 W load. For example, the 2L-AHBF efficiency with design #7 (built using a small E18 core) increases from 70% to 84% if the load increases from 1 W to 4 W (and from 67% to 82% for the 3L-FC-AHBF counterpart). Thus the performances of this solution, that were quite low for a 1 W load, drastically improve to almost reach the targeted efficiency $\eta_{spec} = 85\%$ for a 4 W load, which confirms the potential interest of the burst mode (or similar control techniques).

The curves in Figure 5.25 also reveal how difficult it is to optimize the converters for a 1 W load: for all the transformer designs, the efficiency is better for larger output power due to the significant no-load losses. The only designs that seem to have an optimum output power lower than 4 W are the designs #2 and #8 that use a large core with many turns. All the other designs have their peak efficiency obtained for a 4 W load, making them potentially more suitable for applications requiring a larger output power.

Input voltage range

As shown when presenting the converter's specifications, the input voltage may vary over a wide range: from 300 V to 500 V for the 400 V converter and from 600 V to 1000 V for the 800 V converter. Although the transformers were designed to maximize the efficiency at the nominal input voltage, it is interesting to observe how the converters efficiency changes if the input voltage varies. Figure 5.26 shows the measured efficiency of the 2L-AHBF and the 3L-FC-AHBF configurations, operating with the same transformer design (#1) at similar frequency (450 kHz on the transformer).

The efficiency of the converters largely varies over the input voltage range and the worst case seems to be for the highest input voltage. It comes from the fact that most of the losses inside the converter increase together with the input voltage (core losses increase as the volt-second applied to the transformer is more important, conduction losses increase because a larger voltage on the transformer leads to a larger current ripple). Therefore, if the objective was to ensure the highest minimal efficiency over the input voltage range, then the converters (especially the

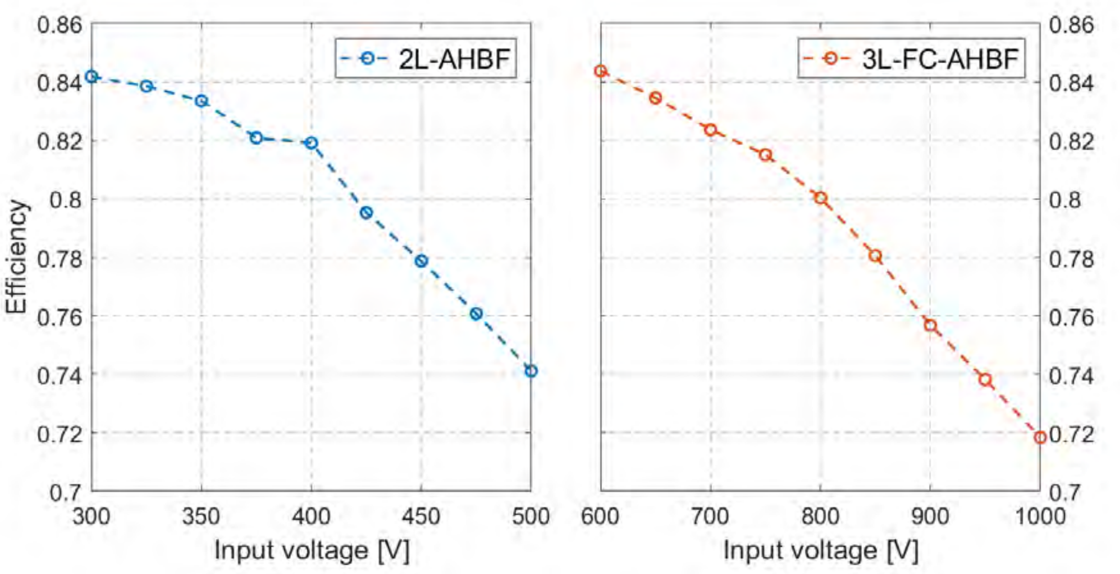


Figure 5.26: Efficiency vs input voltage range (transformer design #1, $V_{out} = 12$ V, $P_{out} = 1$ W)

transformers) should be design to optimize their performances at the highest point of the input voltage range.

5.5.2 Losses at high frequency

As highlighted in previous paragraphs, the efficiency of the converter for the various transformer designs is not as good as expected, particularly at high-frequency. Investigating the origin of the losses is important so they might be not reproduced in future designs. First, the difference between the measured losses and the ones predicted by the converter's simple model is highlighted. A breakdown of the predicted losses in shown for two particular designs and thermal measurements are performed for these two designs. Then, a more detail study of the power FET's output capacitor is conducted and additional measurements of this capacitor are done. Finally, a summary of the potential origins for the losses is presented.

Comparison between measured and predicted losses

To compare the converter's measured losses and the one predicted by the model, the evolution of both is plotted in Figure 5.27 for few transformer designs (#2 is a LF design, #3 is a HF design and #1 is a MF design). The results presented are obtained for the 2L-AHBF converter operating in nominal conditions ($V_{in} = 400$ V, $V_{out} = 12$ V, $P_{out} = 1$ W) and the transformer designs are all based on an E22 core in 3F4 (this material is selected because its loss model is known on a large frequency range).

Results show that the difference between predicted and measured losses largely depends on the frequency at which the designs operate.

For LF and MF solutions (i.e. #3 and #1), there is a good match between the losses predicted by the model and the ones measured at low frequency (below 400 kHz). However, as the switching frequency increases, the difference between the two curves becomes larger and larger.

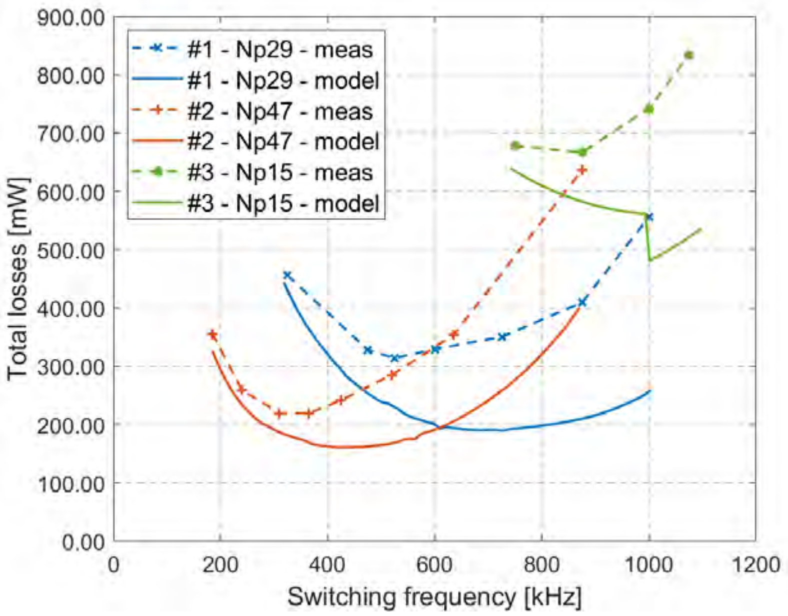


Figure 5.27: Measured and predicted losses evolution with frequency

For the high-frequency design (#3), a similar observation can be made. However, it also appears that the losses prediction abruptly changes around 1000 kHz. This quick fall in the predicted losses for design #3 is related to the change in the Steinmetz parameters (one set of parameters is used for frequencies below 1 MHz, another is used for frequencies higher than 1 MHz), that lead to different predictions of the core losses, that are largely dominant for this design. The significant difference that is observed between the two predictions makes it difficult to evaluate the relevance of the difference between the predicted and the measured losses at high frequency (since it is difficult to know which model is the most accurate). Even though the predicted and the measured losses are close below 800 kHz, it could also be due to an inaccurate model of core losses that would over-estimate these losses and bring the two curves close.

Predicted losses breakdown

To explain the variations of the difference between predicted and measured losses at low-frequency and at high-frequency, a comparison is built between two designs in the 2L-AHBF configuration (V_{in} = 400 V, V_{out} = 12 V, P_{out} = 1 W). Both of them are based on the same transformer design (#1) using the same E-core (E22 in 3F4 material). The only difference between the two designs is the transformer air-gap. For the first design the air-gap is small, such that the primary inductance is large (L_{pri} = 1.9 mH) and so it operates at low frequency (410 kHz). For the second design, a larger air-gap is used, leading to a smaller primary inductance (L_{pri} = 335 µH) and a higher operating frequency (980 kHz). Like for the previous results, both designs operate at the limit of the ZVS mode.

Figure 5.28 presents a breakdown of the predicted losses for the two selected designs and the comparison with the measured losses. The difference between model and measurements is once again significantly larger at high frequency.

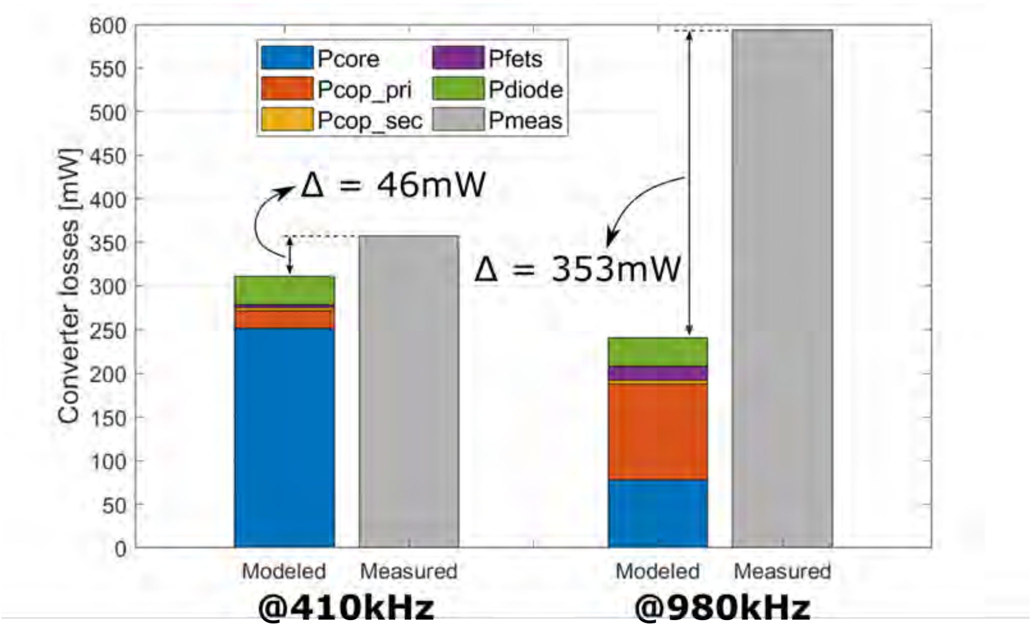


Figure 5.28: Breakdown of predicted losses and comparison with measurements

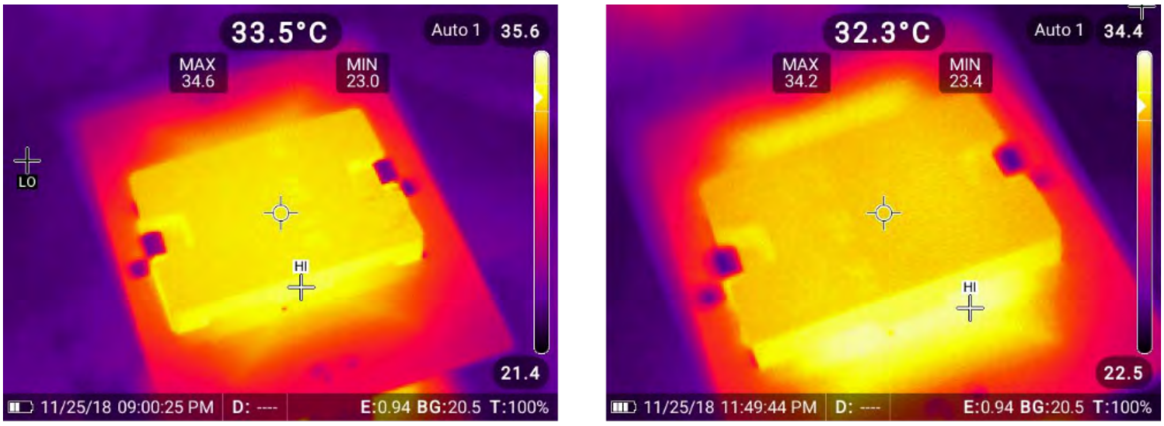
For the low-frequency case, the core losses are largely dominant (P_{core}). It can be explained by the low-frequency that leads to a large volt-second, combined with a medium number of turns ($N_p = 29$). The conduction losses in the transformer's windings (P_{cop_pri} and P_{cop_sec}) are quite small, as the current is reduced. The losses in the power FETs (P_{fets}) only take into account the conduction losses and the low current in the switching node combined with their short on-time lead to very low losses (about 4 mW).

For the high-frequency case, the dominant losses are now the conduction losses in the transformer's primary winding. Due to the higher switching frequency, the RMS primary current becomes larger and so the losses drastically increase. However, at the same time, the core losses should be significantly reduced as the increased frequency enables a large reduction in the flux density. The conduction losses in the power FETs remain quite small (about 15 mW) despite the larger current inside the switching node because their on-time is still short.

Thermal measurements

To try to identify the origin of the extra-losses observed for the high-frequency designs, some thermal measurements are performed on the two previous designs. The objective is not to estimate losses inside each components with accuracy, measuring its steady-state temperature, but rather to observe the temperature of the various power stage's components (mainly the transformer and the IC bricks) for the two cases, to see if any large difference is noticed.

The temperatures are measured using an infrared camera (Ti400 from Fluke) after leaving the converter operate for about one hour to reach thermal steady-state. Note that no particular calibration was performed prior to the measurements and no non-reflective layer was deposited on the different components, so the temperatures absolute accuracy is questionable. However, the following analysis is based only on the relative temperature measurements of which accuracy is assumed to be good enough. Figure 5.29 shows the temperature measurements on the transformer.



@410kHz **@980kHz**

Figure 5.29: Temperature measurements on the transformer for the two designs

For the low-frequency design, the core temperature is slightly higher than the one measured for the high-frequency design (33.5°C vs 32.3°C) but the difference is subtle. Looking at the winding temperature (the one visible on the PCB top layer is a portion of the primary winding), the temperature is higher for the high-frequency design, which is expected as the winding conducts a larger RMS current.

If the temperature difference between the two designs is rather small, it can be explained by the fact the both have comparable losses (when combining the core and the conduction losses in the transformer, losses of the low frequency design are 275 mW and losses in the high-frequency design are 187 mW). Moreover, the heat produced by one element of the transformer might be transmitted to the rest of the transformer (as the winding and the core are very close on some portion of the planar transformer), which could also explain the small difference of the measured temperatures.

Overall, it appears that the transformer temperature in the two designs is quite similar. Thus, it appears difficult to attribute the entirety of the ”extra losses” to this component. In addition, there are other indications that tend to show that these extra losses are not related to the transformer (and more specifically to the core losses).

First, the comparison of similar designs with a different core size (like #1 vs #7, shown in Figure 5.21) reveals the difference of losses observed between the two is rather small, whereas if these extra losses were related to core losses the difference would be quite large. Then, efficiency of the designs operating at high-frequency don't seem to depend to much on the core material (see Figure 5.17), while at low-frequency (where core losses are dominant) the 3F46 material allows to significantly reduce the converter's total losses. As it is not the case at high frequency, it probably means that the extra losses observed at high frequency are not due to the core losses. Another explanation for these losses must be found.

Thermal measurements are also carried out on the IC bricks, in the same conditions as for the transformer and for the same designs. The temperature measured on the dies while operating at high-frequency is significantly higher than when they operate at low frequency (39°C vs 32°C). In both cases, the measured temperature seems quite high with respect to the losses that power FETs are expected to generate, but it could be due to the limited precision of the temperature measurements. However, the difference in temperature is still quite significant with respect to the predicted losses difference (only +10 mW between the two cases). So it could be that there are some unexpected losses occurring in the IC bricks.

Power MOSFET's output capacitor: model and measurements

Looking more in the details at the Cadence model of the power MOSFETs, it turns out it includes a resistance in series with the output capacitor (C_{oss}) which was not accounted for in the simple model. The value of the resistance depends on the drain-source voltage: for $V_{DS} < 10$ V, the resistance value is 15 Ω while for $V_{DS} > 30$ V it is worth 70 Ω.

This reveals a flaw in the converter loss model that was elaborated in Chapter 4: it assumed that the ZVS transitions (during which C_{oss} is being (dis)charged) don't generate any losses in the power FETs, which is obviously wrong given the large resistance that appears to be connected in series with C_{oss}. Using the estimated value of the currents through the power MOSFETs during the ZVS transitions (from the measured i_{SW} current waveforms), the losses generated through the series resistance of the Cadence-model are roughly evaluated. They are estimated to be around 100 mW for the 980 kHz-case and around 20 mW for the 410 kHz-case, so less than the difference between predicted and measured losses shown in Figure 5.28. So a significant portion of the "extra" losses can be related to this series resistance. However, the value of the resistance included in the Cadence model of the power FETs is too small to explain the entirety of the "extra losses". It could be that there is another source of losses that could explain the rest of the losses or it could be that the Cadence model does not fully take into account all the parasitic series resistances connected to the output capacitor of the power FETs.

To confirm the presence of this large resistance in series with C_{oss}, some measurements of the power FETs are performed using an impedance analyzer (E4990A from Keysight with 42941A adapter). This instrument measures the impedance of a dipole and from the magnitude and phase information, it computes the value of a C_s, R_s equivalent model. The impedance analyzer internal bias system allows to create a DC-bias voltage V_{DS} on top of which an AC-voltage excitation v_{AC} is added to measure the power switch drain-source impedance ($V_{GS} = 0$ V). The frequency range of the v_{AC} excitation is between 1 kHz and 10 MHz. The bias-voltage is limited by the instrument capability to $V_{DS} \leq 30$ V. The results obtained for a 1 MHz excitation are shown in Table 5.2. The last row in the Table corresponds to the value of capacitor measured previously using the device analyzer with a C_p, R_p model (as described in Chapter 3).

These results confirm that a large resistance seems to be connected in series with the power MOSFET output capacitor. However, it is hard to measure with accuracy the value of R_s, due to its small impedance compared to the capacitor's impedance, making it difficult to compare the measured values with the ones from the Cadence model. Indeed, the measured value of R_s is relatively constant on a large frequency range only for low V_{DS} values (when the capacitance is larger and its impedance is smaller) but the value of R_s is less stable and harder to read

Table 5.2: Measured $\mathrm{C_s}$,$\mathrm{R_s}$ values in function of the bias voltage

V_{DS} [V]	2	5	10	20	30
R_s [Ω]	99	188	130	140	191
C_s [pF]	362	244	55	31	17
C_{oss} [pF]	375	250	61	36	21

for large V_{DS} values. The measured R_s values seem to be larger than the ones included in the Cadence model and could thus lead to higher losses.

Looking at the measurements of the series capacitance C_s and comparing it to the C_{oss} measurements (described in Chapter 3) based on a C_p, R_p model, some differences between the two measurements are observed. It could indicate that the prior measurements done with the C_p, R_p model are not so accurate and should be repeated taking the new model C_s, R_s into account. However, timing constraints did not allow to perform such measurements.

Conclusions on losses at high frequency

Some extra losses are measured in the converters operating at medium and high frequencies, that were not accounted for in the model. From the various transformer efficiency results and the thermal measurements conducted on the two selected designs, it appears these losses cannot be entirely attributed to the core losses. On the other hand, a deeper analysis of the power MOSFETs model revealed that they present a large resistance in series with their output capacitance. The impedance measurements conducted with a C_s, R_s model seem to confirm there is a resistance and that its value could be larger than the one included in the model.

This last assumption could explain the "extra-losses" and their variations with the frequency. At low frequency, ZVS transitions are less frequent and they are quite slow, with a low current through the power FETs, so they have a limited impact on the total losses. On the other hand, at high-frequency, the ZVS transitions are more frequent and the current that flows through the power FETs is higher, thus leading to significant extra losses.

If the presence of R_s indubitably generates losses that were not predicted by the model, it is still difficult at this stage to attribute the extra losses only to this parasitic resistance. There could be many other explanations, and some of them are discussed below.

One of the well-known issue of a highly-resistive substrate is related to the latch-up effects. The currents injected in the substrate turn on some parasitic components and some charges are collected in circuits located around the power FETs. Although some protections were placed around the power FETs in the IC brick, it could be that it is not enough to prevent all issues. Another potential issue related to the substrate is the voltage bias that can be generated on this reference, since even a mA-current can generate a large voltage drop due to its high resistivity. This bias could cause some circuits to behave in an unexpected way, leading to unpredictable losses.

Another potential explanation could be related to parasitic turn-on of the power FETs, due to the resistivity of the gate-driver's low-side MOSFET and to the currents through the power MOSFETs gate (due to the fast transitions of the power MOFETs drain during the ZVS transitions). They could generate a bias voltage on the gate that would, even partially, turn on the power MOSFET and generate losses (due to some short-circuit current spike for example). No accurate measurements were performed regarding this hypothesis, but simulations results showed that a 5 V/ns voltage variation could cause a parasitic turn-on (for a very short time though).

In all the cases, more measurements would be required to identify with more certainty the origin of the high-frequency extra losses. Unfortunately, time constraints related to the PhD activity forbid further investigations on these aspects.

5.5.3 Comparison with state-of-art

To conclude on the performances of the two DC/DC converter configurations (2L-AHBF and 3L-FC-AHBF), their efficiency is compared to few state-of-art solutions with similar specifications. For each converter, two transformer designs are selected. Design #2 that uses an E22 core in 3F46 material is chosen because it has a highest peak efficiency for this core size and its efficiency is quite good even at light load. Design #7 is also selected as it uses a small E18 core in 3F46 material, which allows to significantly reduce the footprint of the transformer and of the converter, providing a different trade-off between size and performances.

The selected state-of-art solutions are taken from articles published in the literature, datasheets of existing market solutions or reference designs suggested by IC manufacturers.

400 V converters

Table 5.3: Comparison against State-of-Art for 400 V configurations

	This work		Literature		Market	
Year/Man. ► Parameters ▼	Design **#2**	Design **#7**	2002 [3]	2001 [4]	Tamura [9]	Infineon [11]
Input voltage [V]	300-500	300-500	36-373	75-450	110-420	120-440
Output voltage [V]	12	12	5	5	12	12
Output power [W]	1-4	1-4	1-10	1	4	6
Transformer:						
- core reference	E22	E18	RM6	EE16		EFD20
- total footprint^1	34x26	27x22	23x20	20x18		23x21
Module size^1					28x18	35x31
Efficiency at full-load (at Vin)	88.2% (400 V)	84.2% (400 V)	75% (370 V)	83% (400 V)	80% (340 V)	85% (400 V)
Frequency [kHz]	375	900	150	20		25 to 60
Topology	2L-AHBF	2L-AHBF	AC^2 Flyback	Flyback	Flyback	QR^3 Flyback

^{1}: All dimensions are in *mm* ; ^{2}: Active Clamp ; ^{3}: Quasi resonant

The results of the comparison between the 2L-AHBF operating at 400 V and the state-of-art solutions are shown in Table 5.3. They reveal that in terms of efficiency, the E18-converter compares to existing solutions, while the E22-converter surpasses them. However, it also reveal that the footprint of the planar core used is larger. But the transformer's larger size could be balanced by the higher operating frequency of the converter that should reduce the size of other passive components (like input and output capacitors). Moreover, the use of planar transformers should also decrease the total height of the converter, thus leading to a decreased volume. Finally, the converters built using the AHBF topology instead of the Flyback architecture allow to increase the maximum input voltage, since the voltage stress on the switches is reduced, without using expensive wide band-gap devices.

800 V converters

Table 5.4: Comparison against State-of-Art for 800 V configurations

	This work		Literature	Market		
Year/Man. ► Parameters ▼	Design **#2**	Design **#7**	2016 [8]	Cui Inc. [2]	Texas Instruments [12]	[91]
Input voltage [V]	600-1000	600-1000	1.2k-1.8k	100-1000	400-860	56-892(ac)
Output voltage [V]	12	12	24	5	16.5	24
Output power [W]	1-4	1-4	16-60	5	8	3
Transformer:						
- core ref.	E22	E18	EE35			EFD15
- total footprint^1	34x26	27x22	35x35		18x17	17x16
Module size^1				70x48		60x50
Efficiency at full-load (@Vin)	87.4% (800 V)	82.6% (800 V)	60% (1.2 kV)	70% (800 V)	68% (600 V)	67% / 48% (630V/1.2kV)
Frequency [kHz]	360	900	50	< 75	60	32
Topology	3L-FC AHBF	3L-FC AHBF	ISMO^2 Flyback	Flyback	Flyback	2 switches ^{3} Flyback

^{1}: All dimensions are in mm; ^{2}: Input Series Multiple Outputs; ^{3}: Flyback with two cascoded switches

The results of the comparison of the 3L-FC-AHBF operating at 800 V and existing solutions are shown in Table 5.4. Looking at the efficiency of the proposed solutions, there is a significant improvement with respect to the performances of Flyback solutions. The transformer size remains acceptable, although it is still bulkier than for some of the solutions (like reference designs from Texas Instruments [12, 10]). But as for the 2L-AHBF configurations, the higher operating frequency and the lower height could compensate the footprint issue. The maximum input voltage is similar to all the existing solutions, except for [8] but this last uses a more complex design composed of three Flyback converters. One flaw of the proposed converter is its limited input voltage range, especially when compared to [2] or [10]. It is due to the selected topology that is only capable of step-down operations, while the Flyback can also operate in step-up mode. But in the end, given that the main targeted application is related to the battery of an electric vehicle, the variations of the main input voltage should be limited.

5.6 Conclusion

In this chapter, the behavior and the performances of the converters, built using the IC brick and the custom transformer designs, were measured and analyzed.

Some functional measurements validated the general behavior of the converter matches the one predicted by the analysis done in Chapter 2.

The ZVS mechanism were studied in details to evaluate the parasitic capacitances that play a role in the ZVS transitions. The measurements of the ZVS mechanism were in good agreement with the predictions made by the theoretical analysis and the simple converter model described in Chapter 4. The study of the ZVS operation also confirmed that it is interesting for the converter to operate at the limit of the ZVS mode, to enhance its efficiency.

The performances of the various transformer designs have been measured and some useful information come out of this study, regarding the choice of the material (3F46 is the best in this frequency range) and the core size. However, the efficiency of some converter designs are altered by some losses at high-frequency that don't seem to be directly related to the transformer design.

The efficiency of the two converters (2L-AHBF and 3L-FC-AHBF) are then measured for a few transformers. If the efficiency measured at low-frequency is close to the expectations, the losses are much higher when converters operated at medium or high frequency. A short study of the potential origin of these losses was conducted and a large resistance is found in series with the power FETs output capacitor that could explain (at least partially) the extra-losses.

Finally, the proposed solutions are compared to the State-of-Art for 400 V and 800 V configurations. The interest of the selected approach is particularly clear for 800 V converters for which the efficiency gain is significant.

General Conclusion and Perspectives

Some applications call for an isolated DC/DC converter with a high-input voltage and a low-voltage, low-power output. In this work, the design of such a converter was discussed and selected approaches to create a small, low-cost and highly efficient solution were presented.

First, a short review of some existing solutions was proposed, their limits were highlighted and attributed mostly to the Flyback architecture that is used in most low-power solutions. Therefore, a study of an alternative topology for the converter power stage was performed, considering the constraints due to the application and the suitability of the selected approach regarding the technology of integration. The Multi-Level Flying-Capacitor architecture was selected as it offers an interesting trade-off between the power stage complexity and the expected converter efficiency. Its behavior was studied analytically to identify the important design trends and parameters. A first prototype build with discrete components revealed the difficulty to achieve an efficient HVLP solution and highlighted the need to integrate the "active" parts of the power stage to decrease the converter size and cost. An Integrated Circuit containing the power switches and the circuits required to control and supply them was designed using the selected low-cost Si process. The IC brick solution was proposed to overcome the limitations of the HV bulk Si technology that limits the device-to-device isolation. Due to the high constraints on the transformer, its integration on silicon was not considered and so its design was discussed to improve the size/efficiency trade-off inherent to this key component. Analyzing the influence of few design parameters, several transformer designs were proposed and manufactured on a Design-of-Experiments perspective. In the end, a prototype of the converter built using the IC bricks and the custom transformers was measured. The waveforms validated the analysis regarding the behavior and operating modes described previously for the converter. The efficiency measurements revealed that some of the experimented solutions can cope with the initial efficiency target, but it is restricted to the designs operating at low-frequency. For the high-frequency designs, some extra-losses forbid to reach the expected performances and their origin could not be clearly identified - although the conduction losses occurring during the ZVS transitions are suspected. Finally, the efficiency measured with few of the transformer designs was compared to the existing solutions and showed that the gain in efficiency is significant, especially for the 800 V converters.

Viability of the solution and selected approach

Before presenting some perspectives for the design of High-Voltage Low-Power converters, it might be interesting to question the viability of the approach and of the proposed solution in preparation for a potential industrialization.

In my understanding, there are two main obstacles that could restrain the industrial development of the proposed solution: the monolithic integration of several ICs, required to reach the targeted integration level, and the reliability of the proposed architecture based on a Multi-Level Flying-Capacitor (ML-FC).

Due to the limited device-to-device isolation of the selected integration technology (HV bulk Silicon), all the power switches must be placed in a separate die. However, to reach a small size solution and to decrease the influence of parasitic components between IC bricks, they should be all co-packaged using techniques like Multi-Chip Module (MCM). But the cost of these advanced technique might contradict with the low-cost and low-complexity perspectives, that were at the base of the project.

In parallel, the reliability of the proposed power stage architecture should be assessed. Not mentioning the several issues met during the practical implementation of the power stage (in particular with the level-shifter and the bootstrap blocks), the ML-FC stage complexity inevitably decreases its reliability compared to a Flyback architecture that is very robust but less efficient under high input voltage. The start-up sequence of the ML-FC could cause several issues, for example with the charging of the flying capacitor etc. It does not mean it should not be used, but the context of the targeted application (safety/high-reliability in automotive) will require a robustness level that might be hard to reach with the proposed architecture.

Perspectives

For each of the aspects of the converter that were studied, there are some perspectives that could be interesting to explore to improve the solutions built or to propose some design variations.

A different integration technology for a different architecture

A change in the integration technology could lead to choose a different type of structure for the high-voltage, low-power converters. In particular, the performances of converters based on Switched-Capacitor stages could be satisfying. A solution with a similar structure (Multi-Level Flying-Capacitor) but with a greater number of levels could also be investigated. Both solutions could allow to further reduce the stress on the transformer and so to improve its size/performances trade-off. Although the cost of an alternative integration technology could be higher, it would offer a new perspective regarding the cost/performances trade-off of the converter. In addition, the increase in fabrication costs might be balanced by the use of a mainstream packaging technology (not requiring complex techniques such as MCM).

Additionally, changing the integration technology could also solve the issue related to losses during the ZVS transitions, as they seem to be linked, at least partially, to the highly-resistive substrate involved in the low-cost bulk HV-Si process.

IC brick re-design

Regarding the design of the IC brick, a re-design could allow to increase the robustness of some blocks (like the level-shifters and the bootstrap) and to increase the performances (reducing current consumption and delays). The influence of the size of the power MOSFET could also be studied. Some other blocks could be added to the IC brick to enhance its functionality like a start-up circuit (to allow the IC to start without requiring an auxiliary supply) or an internal PWM generator (that could create the PWM signals required to control the power stage) to close the regulation loop.

Transformer design

The shape of the transformer core should be further explored. For example, planar EQ-cores with a round center core leg could help reducing the area occupied by the windings. It could also be interesting to compare the performances of the transformers designed in this work to those obtained using conventional transformers built with thin wires, as they could allow to decrease the transformer footprint (although they seem to be less fitted to operate at high frequency). Different values of turns ratio could also be experimented to improve the performances of the converter for high input voltages. Some investigations could be leaded on how to improve the EMI performances of the transformer, by adding some shields for example.

To further reduce the size of the magnetic component, the use of advanced integration technologies could be studied. Some techniques exist today to embed the transformer core inside the PCB or to place it inside the same package as the active parts. But it could remain challenging to keep the transformer's losses to an acceptable level using this kind of approaches.

Converter's control and application requirements

For the overall converter, its efficiency could be improved using advanced control techniques to use it for the load operating point with the peak efficiency (techniques like burst mode for example). The application specifications would need to be refined on several aspects (maximum volume/footprint of the converter, EMI constraints, output voltage ripple, etc.) to make sure that the selected approach can be suitable regarding these parameters and to evaluate its interest with respect to standard Flyback-based solutions.

Appendix A

Analysis of a period of the 3L-FC-AHBF

In this appendix, a more complete analysis of the equations describing the waveforms of the 3L-FC-AHBF power stage is presented.

The model for the components used for the analysis are detailed in Chapter 2. Some hypotheses are made to simplify the analysis, similar to the one made for the study of the 2L-AHBF:

- Primary capacitance (C_p) value is big enough to consider that its voltage is constant over a switching period. V_{Cp} is supposed to be equal to the average output voltage referred to the primary side.
- The voltage across the flying capacitor V_{fly} is supposed constant and equal to its ideal value, that is $V_{in}/2$.
- The state in which the body-diode of a power switch conducts the current, just before the switch is actually turned-on, is neglected because the topology behavior is the same as when the switch is ON (as shown in the previous analysis).
- Primary-secondary parasitic capacitor (C_{ps}) value is constant and entirely referred to the primary side.
- The value of the leakage inductance is small in comparison with the value of the magnetizing inductance.

Figure A.1 presents the circuit diagram of the power stage and Figure A.2 shows the typical waveforms obtained in simulation.

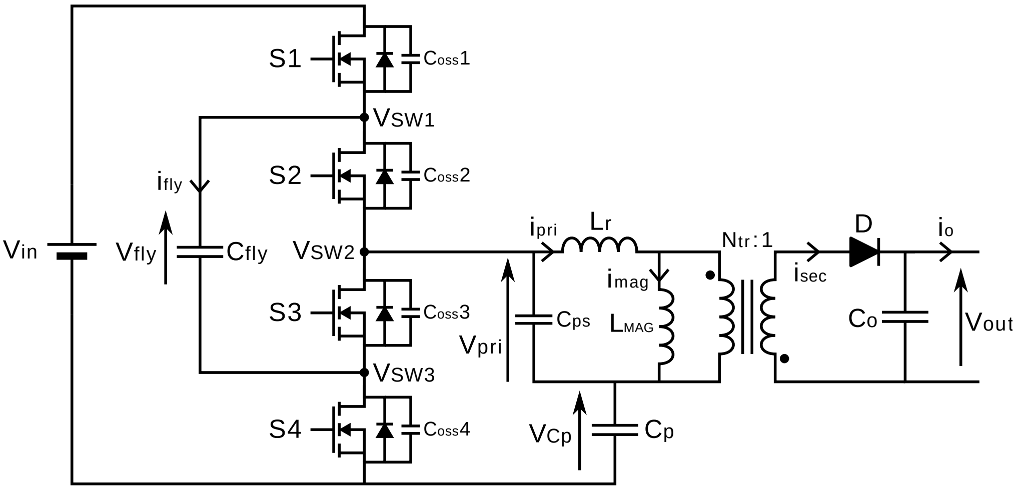


Figure A.1: Model considered for the 3-level FC AHBF

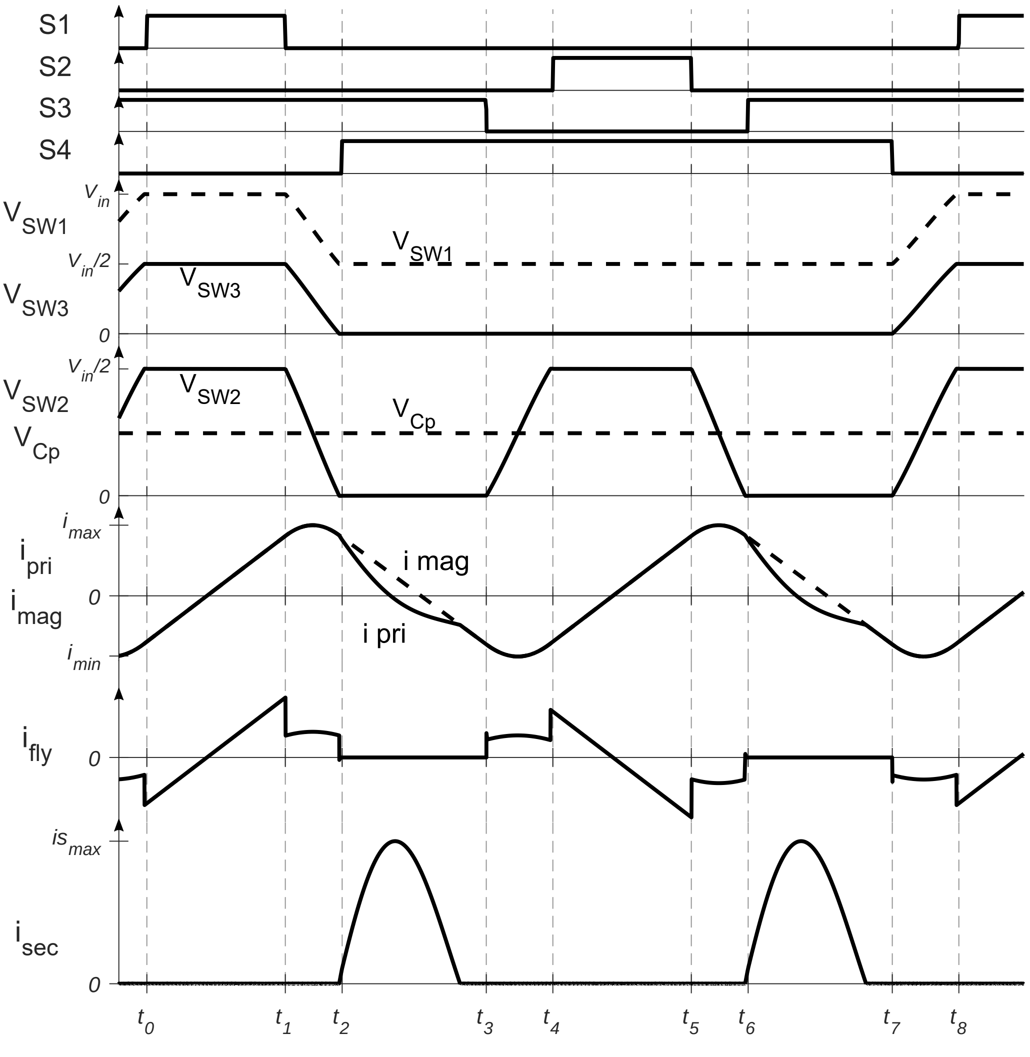


Figure A.2: 3L-FC-AHBF - Main waveforms

State 1 (t_1 - t_2)

State 1 starts when the power switch $S1$ (or its body-diode) turns-on. The switch $S3$ is also in ON-state during the state 1. The voltage on the transformer primary is:

$$V_{pri}(t) = V_{in} - V_{fly} - V_{Cp} = \frac{V_{in}}{2} - V_{Cp} \tag{A.1}$$

The positive voltage across the transformer's primary leads to a linear increase of the primary current, which can thus be written as:

$$i_{pri}(t) = i_{mag}(t) = i_{pri}(t_0) + \frac{V_{in}/2 - V_{Cp}}{L_{mag} + L_r} \cdot (t - t_0) \tag{A.2}$$

And the current flowing inside the flying capacitor, as shown in Figure A.1, is the same as this primary current, as both flows in the same direction:

$$i_{fly}(t) = i_{pri}(t) \tag{A.3}$$

State 1 ends when the switch $S1$ turns-off.

State 2 (t_1 - t_2)

During state 2, the switching nodes $V_{SW1}, V_{SW2}, V_{SW3}$ are moving due to the energy stored inside the transformer's primary, which charge/discharge the parasitic capacitors connected to these switching nodes. Figure A.3 shows the equivalent model during State 2.

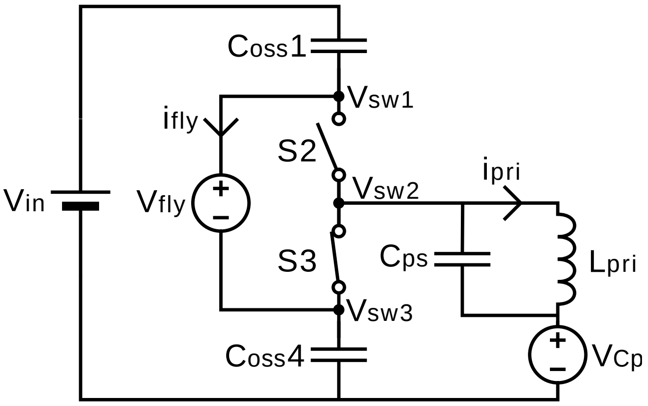


Figure A.3: Equivalent model for 3L-FC-AHBF - State 2 (t_1 - t_2) & State 8 (t_7 - t_8)

It is interesting to note that the switching nodes are all connected together from an AC-variation perspective, because $S3$ tights V_{SW2} and V_{SW3} together while the flying capacitor forces a constant voltage between V_{SW1} and V_{SW3}. As a consequence, all the capacitors can be added to compute the total switching capacitor for this transition C_{SW0}:

$$C_{SW0} = C_{ps} + C_{oss1} + C_{oss4} \tag{A.4}$$

Therefore, it is possible to write the formula giving the variations of the primary voltage and current as:

$$\frac{dV_{pri}(t)}{dt} = -\frac{i_{pri}(t)}{C_{SW0}} \tag{A.5}$$

$$\frac{di_{pri}(t)}{dt} = \frac{V_{pri}(t)}{L_{mag} + L_r} \tag{A.6}$$

It is interesting to note that these equations are similar to those obtained for the 2L-AHBF. It means that solving the differential equations should give results similar as well. When solving the differential equation, the current and voltage on transformer's primary during state 2 can be expressed as:

$$i_{mag}(t) = i_{pri}(t) = i_{pri}(t_1) \cdot cos(\omega_0(t - t_1)) + \frac{V_{in}/2 - V_{Cp}}{Z_0} * sin(\omega_0(t - t_1)) \tag{A.7}$$

$$V_{pri}(t) = -i_{pri}(t_1) \cdot Z_0 \cdot sin(\omega_0(t - t_1)) + (V_{in}/2 - V_{Cp}) \cdot cos(\omega_0(t - t_1)) \tag{A.8}$$

with $\omega_0 = \dfrac{1}{\sqrt{C_{SW0} \cdot (L_{mag} + L_r)}}$ (A.9) and $Z_0 = \sqrt{\dfrac{L_{mag} + L_r}{C_{SW0}}}$ (A.10)

These formulas are indeed quite similar to those obtained for the ZVS transition in the 2L-AHBF, as the resonant pulsation ω_0 and the impedance Z_0 have the same expression than previously. It shows that the ZVS transitions in the case of the 3L-FC and in the case of the 2L are driven by similar mechanism.

During this transition, the current through the flying capacitor is due to the current that charges the output capacitance of high-side switch C_{oss1}. It is therefore possible to express it as a portion of the primary current:

$$i_{fly}(t) = i_{pri}(t) \cdot \frac{C_{oss1}}{C_{SW0}} \tag{A.11}$$

State 2 finishes at the end of the ZVS transition, when the switching nodes V_{SW2} and V_{SW3} reach ground.

State 3 (t_2 - t_3)

As the different switching nodes get to the ground level, the switch $S4$ turns-on in ZVS conditions. As both low side switches $S3$ and $S4$ are in ON-state, the middle switching node V_{SW2} is forced to ground and the voltage across the transformer's primary is

$$V_{pri}(t) = -V_{Cp} \tag{A.12}$$

The magnetizing current therefore decreases:

$$\frac{di_{mag}(t)}{dt} = \frac{V_{mag}(t)}{L_{mag}} \tag{A.13}$$

Due to the small variations of the output voltage, a linear decreasing of the magnetizing current is assumed, which leads to:

$$i_{mag}(t) \approx i_{mag}(t_2) - \frac{N_{tr} \cdot (V_D + \overline{V_{out}})}{L_{mag}} \tag{A.14}$$

At the same time, due to the opposite connection of the transformer's primary and secondary windings, the positive voltage on secondary side allows the forward bias of the secondary diode D. The current can therefore flow on the secondary side, as shown in Figure A.2 and its dynamic will depend on the value of the primary leakage inductance.

The dynamic of the secondary current i_{sec} is decided by the voltage drop on the leakage inductance, as for the state 3 in the 2L-AHBF:

$$V_{Lr}(t) = -V_{mag}(t) - V_{Cp} = N_{tr} \cdot (V_{out}(t) + V_D) - V_{Cp} \tag{A.15}$$

In this last expression, the variations of the output voltage are taken into account. In addition, it is possible to express the relation between primary, magnetizing and secondary currents as:

$$\frac{di_{pri}(t)}{dt} = \frac{V_{Lr}(t)}{L_r} = \frac{di_{mag}(t)}{dt} - \frac{di_{sec}(t)}{dt} \cdot \frac{1}{N_{tr}} \tag{A.16}$$

On the secondary side, the output current i_o is supposed to be constant. Therefore the output voltage variations depend on the secondary current:

$$\frac{dV_{out}(t)}{dt} = \frac{i_{sec}(t) - i_o}{C_o} \tag{A.17}$$

Combining (A.15), (A.16) and (A.17) the differential equation can be found. To solve it, it is possible to assume that the voltage across capacitor V_{Cp} is equal to the average output voltage referred to the primary side (the expression was given in chapter 2 in the section dedicated to the 3L-FC-AHBF main transfer function).

The solution of the differential equation gives the following formula for the secondary current:

$$i_{sec}(t) = i_o \cdot (1 - cos(\omega_2(t - t_2))) + \frac{N_{tr}}{Z_2} \cdot \frac{\Delta V_{out}}{2} \cdot sin(\omega_2(t - t_2)) \tag{A.18}$$

with $$\omega_2 = \frac{N_{tr}}{\sqrt{C_o \cdot L_r}} \tag{A.19}$$ and $$Z_2 = \sqrt{\frac{L_r}{C_o}} \tag{A.20}$$

and where ΔV_{out} is the peak-to-peak ripple of the output voltage, expressed as:

$$\frac{\Delta V_{out}}{2} = V_{Cp} - N_{tr} \cdot (V_{out}(t_2) + V_D) \tag{A.21}$$

It can be noticed that the expression for the secondary current is the same as for the 2L-AHBF. In reality, the parasitic resistor met by the primary current will be different, so the voltage across the leakage inductor will be different. But since the influence of the parasitic components in neglected, the two expressions are the same for the 2L-AHBF and the 3L-FC-AHBF.

Finally, the primary current is computed as:

$$i_{pri}(t) = i_{mag}(t) - \frac{i_{sec}(t)}{N_{tr}} \tag{A.22}$$

Note that the flying capacitor current is null during this period, as both high-side switches are off, and the nodes where the flying capacitor is connected are not moving.

The secondary current cancellation does not impact the different voltage levels that stay the same until the end of state 3, which ends when the switch $S3$ turns-off.

State 4 (t_3 - t_4)

The turn-off the switch $S3$ initiates a new ZVS transition, once again due to the energy stored in the magnetizing inductance. The equivalent model for the 3L-FC-AHBF in this state is presented in Figure A.4. It shows the middle switching node will move from ground level up to the flying capacitor voltage V_{fly}, charging/discharging all the parasitic capacitors connected to this node.

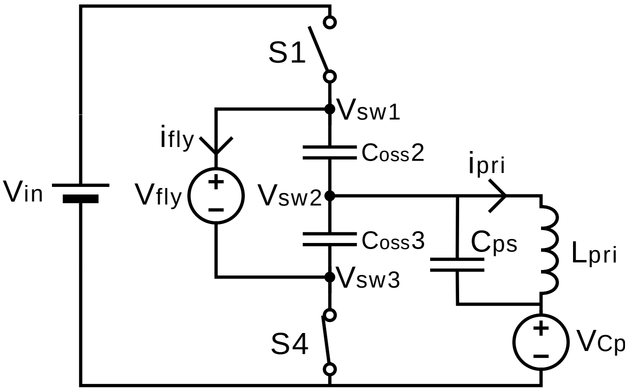


Figure A.4: Equivalent model for 3L-FC-AHBF - State 4 (t_3 - t_4) & State 6 (t_5 - t_6)

The current and voltage variations are:

$$\frac{dV_{SW2}}{dt}(t) = -\frac{i_{pri}(t)}{C_{SW1}} \tag{A.23}$$

$$\frac{di_{pri}}{dt}(t) = \frac{di_{mag}}{dt}(t) = \frac{V_{SW2}(t) - V_{Cp}}{L_{mag} + L_r} \tag{A.24}$$

where the total capacitance connected to V_{SW2} in this state is:

$$C_{SW1} = C_{oss2} + C_{oss3} + C_{ps} \tag{A.25}$$

Solving the differential equations associated to these expressions will lead to formulas for primary voltage and current as:

$$i_{pri}(t) = i_{mag}(t) = i_{pri}(t_3) \cdot cos(\omega_1(t - t_3)) - \frac{V_{Cp}}{Z_1} \cdot sin(\omega_1(t - t_3)) \tag{A.26}$$

$$V_{pri}(t) = -\ i_{pri}(t_3) \cdot Z_1 \cdot sin(\omega_1(t - t_3)) - V_{Cp} \cdot cos(\omega_1(t - t_3)) \tag{A.27}$$

with $$\omega_1 = \frac{1}{\sqrt{C_{SW1} \cdot (L_{mag} + L_r)}} \tag{A.28}$$ and $$Z_1 = \sqrt{\frac{L_{mag} + L_r}{C_{SW1}}} \tag{A.29}$$

Finally, the current through the flying capacitor is the current used to discharge the output capacitance of $S2$ switch, which leads to:

$$i_{fly}(t) = -i_{pri}(t) \cdot \frac{C_{oss2}}{C_{SW1}} \tag{A.30}$$

State 4 ends as soon as the middle switching node V_{SW2} reaches the voltage of the flying capacitor, allowing for a soft turn-on of the switch $S2$.

State 5 (t_4 - t_5)

State 5 starts as $S2$ turns-on at $t = t_4$. Since both $S2$ and $S4$ are ON, the primary voltage can be written as:

$$V_{pri}(t) = V_{fly} - V_{Cp} = V_{in}/2 - V_{Cp} \tag{A.31}$$

The constant primary voltage translates into a linear increase of the primary current. Moreover, during this state the primary current and the flying capacitor current flow in opposite directions, which leads to:

$$i_{pri}(t) = i_{mag}(t) = -i_{fly}(t) = i_{pri}(t_4) + \frac{V_{fly} - V_{Cp}}{L_{mag} + L_r} \cdot (t - t_4) \tag{A.32}$$

State 5 ends when switch $S2$ turns-off.

State 6 (t_5 - t_6)

In state 6, the positive magnetizing current inside the transformer make the switching node V_{SW2} moves from V_{fly} down to the ground level. As the low-side switch $S4$ is ON, the only node moving is V_{SW2}. For this node to move, the parasitic capacitors connected to it should be charged/discharged using the primary current. The equivalent circuit for this state is the same as for state 4, shown in Figure A.4.

Only the initial conditions of capacitance voltage and current value change. As the basic equations describing this state are the same as for state 4 (i.e. expressions (A.23) and (A.24)), solving the differential equations for these initial conditions lead to:

$$i_{pri}(t) = i_{pri}(t_5) \cdot cos(\omega_1(t - t_5)) + \frac{V_{in}/2 - V_{Cp}}{Z_1} \cdot sin(\omega_1(t - t_5)) \tag{A.33}$$

$$V_{pri}(t) = -i_{pri}(t_5) \cdot Z_1 \cdot sin(\omega_1(t - t_5)) + (V_{in}/2 - V_{Cp}) \cdot cos(\omega_1(t - t_5)) \tag{A.34}$$

With the expressions for ω_1 and Z_1 equal to those given for state 4 (Equations A.28 and A.29).

Like during state 4, the flying capacitor current is a fixed portion of the primary current, as it is used to charge the output capacitance of $S2$ switch C_{oss2}:

$$i_{fly}(t) = -i_{pri}(t) \cdot \frac{C_{oss2}}{C_{SW1}} \tag{A.35}$$

State 7 (t_6 - t_7)

State 7 starts when the middle switching node V_{SW2} reaches ground and $S3$ switch turns-on. The primary voltage is:

$$V_{pri}(t) = -V_{Cp} \tag{A.36}$$

Just like in state 3, this negative voltage is transformed to a positive voltage on the secondary side, allowing for the forward bias of the secondary diode. As a results, some current is flowing on the secondary side. The equations describing this current are the same as the ones obtained in state 3. The expression for the magnetizing current is also the same as in state 3 and so the expression of the primary current is identical to the one obtained in state 3 as well.

The current inside the flying capacitor is null also during this state. State 7 ends when the low-side switch $S4$ turns-off.

State 8 (t_7 - t_8)

This last state consists in another ZVS transition, as the switching node V_{SW3} travels from ground to $V_{in} - V_{fly}$ when switch $S4$ turns-off at $t = t_7$. The behavior during this state 8 is very similar to the one obtained during state 2, as the equivalent model is the same for these two states (see Figure A.3).

Solving the same differential equations with different initial conditions lead to the following expression for the primary current and voltage:

$$i_{pri}(t) = i_{pri}(t_7) \cdot cos(\omega_0(t - t_7)) + \frac{-V_{Cp}}{Z_0} \cdot sin(\omega_0(t - t_7)) \tag{A.37}$$

$$V_{pri}(t) = -i_{pri}(t_7) \cdot Z_0 \cdot sin(\omega_0(t - t_7)) - V_{Cp} \cdot cos(\omega_0(t - t_7)) \tag{A.38}$$

With the expressions for ω_0 and Z_0 equal to those given for state 2 (Equations (A.9) and (A.10)).

As during the state 2, the current flowing through the flying capacitor is the current used to discharge the output capacitance of $S1$ switch C_{oss1}:

$$i_{fly}(t) = i_{pri}(t) \cdot \frac{C_{oss1}}{C_{SW0}} \tag{A.39}$$

State 8 ends at t_8 when the switching node V_{SW1} reaches V_{in}. $S1$ can then turn-on in ZVS condition and a new switching period can start.

Appendix B

Performances in the 3L-FC-AHBF configuration

As discussed in Chapters 2 and 4, the behavior of the 2L-AHBF and the 3L-FC-AHBF are very similar. Moreover, the losses and the performances of these two versions are also comparable. Indeed, it is possible to find an expression that create the link between the performances of a 2L-AHBF configuration and the 3L-FC-AHBF stage. The expression is used inside the simplified model to compute losses for the 3L-FC-AHBF version of the converter simply from the performances of the 2L-FC-AHBF for a given design is shown below (B.1). The developments leading to this expression are discussed here.

$$P_{FETs\ 3L} = P_{FETs\ 2L} + r_{DS_{on}} \cdot i_{pri\ RMS}^{2} \tag{B.1}$$

For this expression to be verified, it requires that both versions of the topology operate in similar conditions (same transformer's frequency, same output voltage, etc.) except for the input voltage, that is twice bigger in the 3L-FC-AHBF than for the 2L-AHBF. Considering the different types of losses that occur in the power stage of the converter, many similarities once again appear between the two versions of the topology.

For the transformer, if the same design is used, then the associated core losses and conduction losses will be almost the same for both versions. This is because the voltage and the currents that excite the magnetic component are very similar as shown in Figure B.1 and as discussed in Chapter 2. The secondary currents being quite alike, the conduction losses in the secondary diode can also be considered equal. Finally, in both versions, no switching losses are taken into account, since they operate in ZVS mode and the power required to control and pilot the power switches is neglected in the losses breakdown.

In the end, only the conduction losses in the switches will present differences depending on the version of the topology, which can be simply explained by the number of power switches in each architecture: only two of them are present for the 2L-AHBF while four power switches compose the 3L-FC-AHBF configuration, so the total losses in these components will be different. However, studying the total conduction losses generated in the switches in the two version, it is possible to find a relation between them.

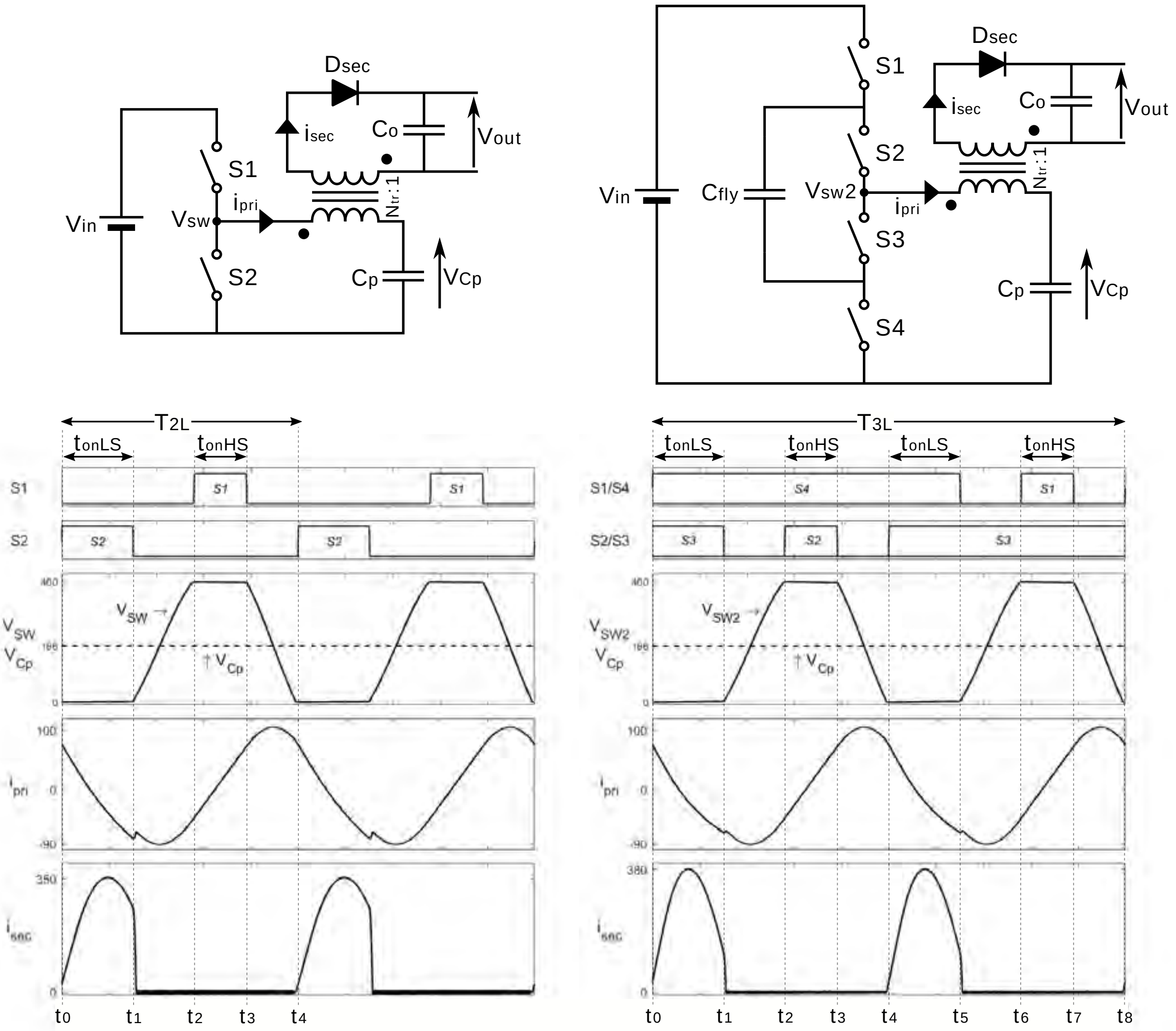
For the study of the conduction losses inside the power MOSFETs, few hypotheses are made:

- The same on-resistance is used for all the power MOSFETs ($r_{DS_{on}}$)

- The switching frequency of the 2L-AHBF is twice the one of the 3L-FC-AHBF ($T_{3L} = 2 \cdot T_{2L}$)
- The same primary current is assume in both versions, which is almost the case in waveforms shown in Figure B.1.
- The losses difference due to the MOSFETs body-diode conducting is neglected. It means the time interval in which the ZVS transition is done but the power switch is still OFF is considered null.
- The same on-time is used for the high-side and the low-side power MOSFET, as indicated in Figure B.1. The following relation are thus considered true:

  $(t_1 - t_0)_{2L} = (t_1 - t_0)_{3L} = (t_5 - t_4)_{3L} = t_{on\ LS}$; $(t_3 - t_2)_{2L} = (t_3 - t_2)_{3L} = (t_7 - t_6)_{3L} = t_{on\ HS}$

The main simulation waveforms obtained for both versions are shown in Figure B.1.



(a) (b)

Figure B.1: Schematics and simulation waveforms for (a) 2L-AHBF, $V_{in} = 400$ V, $f_{SW} = 1$ MHz, $L_{pri} = 500$ µH and (b) 3L-FC-AHBF, $V_{in} = 800$ V, $f_{SW} = 500$ kHz, $L_{pri} = 500$ µH

For the 2L-AHBF, the total conduction losses in the power FETs can be written as:

$$P_{FETs\ 2L} = r_{DS_{on}} \cdot \frac{1}{T_{2L}} \cdot \int_0^{T_{2L}} i_{S1}^2(t)\ dt + r_{DS_{on}} \cdot \frac{1}{T_{2L}} \cdot \int_0^{T_{2L}} i_{S2}^2(t)\ dt \tag{B.2}$$

Considering only the moments when the power switches conduct currents, the expression becomes:

$$P_{FETs\ 2L} = r_{DS_{on}} \cdot (\frac{1}{T_{2L}} \cdot \int_{t_2}^{t_3} i_{pri}^2(t)\ dt + \frac{1}{T_{2L}} \cdot \int_{t_0}^{t_1} i_{pri}^2(t)\ dt) \tag{B.3}$$

It can be further simplified writing it as:

$$P_{FETs\ 2L} = r_{DS_{on}} \cdot (i_{HS\ RMS}^2 + i_{LS\ RMS}^2) \tag{B.4}$$

For the 3L-FC-AHBF, the total conduction losses in the power FETs can be written as:

$$P_{FETs\ 3L} = r_{DS_{on}} \cdot \frac{1}{T_{3L}} \cdot (\int_0^{T_{3L}} i_{S1}^2(t)\ dt + \int_0^{T_{3L}} i_{S2}^2(t)\ dt + \int_0^{T_{3L}} i_{S3}^2(t)\ dt + \int_0^{T_{3L}} i_{S4}^2(t)\ dt) \tag{B.5}$$

Considering only the moments when the power switches conduct currents, the expression becomes:

$$P_{FETs\ 3L} = r_{DS_{on}} \cdot \frac{1}{T_{3L}} \cdot (\int_{t_6}^{t_7} i_{pri}^2(t)\ dt + \int_{t_2}^{t_3} i_{pri}^2(t)\ dt + \int_{t_4}^{t_1+T_{3L}} i_{pri}^2(t)\ dt + \int_{t_0}^{t_5} i_{pri}^2(t)\ dt) \tag{B.6}$$

In the case of the 3L-FC-AHBF, for the high-side switches, it is possible to notice that the sum of their contribution is equal to the contribution of the high-side switch of the 2L-AHBF:

$$\frac{1}{T_{3L}} \cdot (\int_{t2}^{t3} i_{pri}^2(t)\ dt + \int_{t6}^{t7} i_{pri}^2(t)\ dt) = \frac{1}{T_{2L}} \cdot \int_{t2}^{t3} i_{pri}^2(t)\ dt = i_{HS\ RMS}^2 \tag{B.7}$$

At the same time, for the low-side power switches, the time during which they are in on-state can be divided in two portions, to corresponds to the time when the low-side in ON in the 2L-AHBF version:

$$\int_{t_4}^{t_1+T_{3L}} i_{pri}^2(t)\ dt + \int_{t_0}^{t_5} i_{pri}^2(t)\ dt = \int_{t_4}^{t_5} i_{pri}^2(t)\ dt + \int_{t_5}^{t_1+T_{3L}} i_{pri}^2(t)\ dt + \int_{t_0}^{t_1} i_{pri}^2(t)\ dt + \int_{t_1}^{t_5} i_{pri}^2(t)\ dt \tag{B.8}$$

Which can be rewritten as:

$$\int_{t_4}^{t_1+T_{3L}} i_{pri}^2(t)\ dt + \int_{t_0}^{t_5} i_{pri}^2(t)\ dt = \int_{t_4}^{t_5} i_{pri}^2(t)\ dt + \int_{t_0}^{t_1} i_{pri}^2(t)\ dt + \int_{t_1}^{t_1+T_{3L}} i_{pri}^2(t)\ dt \tag{B.9}$$

Similarly to the high-side power switches, the sum of the two first terms of the low-side switches contribution in (B.9) is equal to the contribution of the low-side switch in the 2L-AHBF:

$$\frac{1}{T_{3L}} \cdot (\int_{t_4}^{t_1+T_{3L}} i_{pri}^2(t)\ dt + \int_{t_0}^{t_5} i_{pri}^2(t)\ dt) = i_{LS\ RMS}^2 + \frac{1}{T_{3L}} \cdot \int_{t_1}^{t_1+T_{3L}} i_{pri}^2(t)\ dt \tag{B.10}$$

Injecting (B.7) and (B.10) in (B.6), the expression of the total conduction losses in the FETs in the 3L-FC-AHBF version becomes:

$$P_{FETs\ 3L} = r_{DS_{on}} \cdot (i_{HS\ RMS}^2 + i_{LS\ RMS}^2 + \frac{1}{T_{3L}} \int_{t_1}^{t_1+T_{3L}} i_{pri}^2(t)\ dt) \tag{B.11}$$

However, the last term in (B.11) is equal to the RMS value of the primary current i_{pri} while the rest of the contributions are the same as for the 2L-AHBF. Therefore, the relation between the total conduction losses in the FETs in the 3L-FC-AHBF and in the 2L-AHBF is:

$$P_{FETs\ 3L} = r_{DS_{on}} \cdot (i_{HS\ RMS}^2 + i_{LS\ RMS}^2 + i_{pri\ RMS}^2) \tag{B.12}$$

$$P_{FETs\ 3L} = P_{FETs\ 2L} + r_{DS_{on}} \cdot i_{pri\ RMS}^2 \tag{B.13}$$

The last expression reveals that the losses in the 3L-FC-AHBF can be simply emulated from the losses of the 2L-AHBF adding a resistance $r_{DS_{on}}$ in series with the primary of the transformer.

To analyze this from a different perspective, it is possible to notice that the switching period of the 3L-FC-AHBF can be divided in two portions.

A first portion $(t_0 - t_4)$ during which the low-side switch $S4$ is always ON while $S2$ and $S3$ behaves just like the switches in a 2L-AHBF over a full-period. And a second portion $(t_4 - t_8)$ during which it is $S3$ that is always ON while $S1$ and $S4$ behaves like the switches in a 2L-AHBF. Therefore, it is just like if there was one additional switch that is always ON in the 3L-FC-AHBF with respect to the 2L-AHBF and that this switch conducts the current that flows through the primary side of the converter, and this is exactly what describes the expression (B.13).

Appendix C

A study of the power MOSFET size

The choice of the size of the power MOSFET is usually of great importance in the design of DC/DC converters. This choice is usually driven by consideration regarding the performances, the cost and sometimes the thermal constraints. However it was not possible to study the influence of the size of the power MOSFET included in the IC brick due to the time constraints of the silicon run. Nevertheless, it is possible to use the simple model described in Chapter 4 to get an idea of the impact of the power MOSFET size on performances and how it could be optimize for the next designs. However, note that this discussion does not takes into account the late measurements of the power MOSFET output capacitor that reveal a large series resistance is present (as discussed at the end of Chapter 5)

Here, only the impact of the size of the power MOSFET on the expected efficiency of the DC/DC converter is analyzed (considering lossless ZVS transitions). To study it, the input parameters given to the converter's simple model that relates to the power MOSFET size are changed (i.e. the on-resistance and the output capacitor). To try to anticipate the impact of the size of the power MOSFET, the following relations are used:

$$r_{ds_{ON}\ new} = r_{ds_{ON}\ meas}/nSizeFET \tag{C.1}$$

$$C_{oss\ new} = C_{oss\ meas} \cdot nSizeFET \tag{C.2}$$

Where $r_{ds_{ON}\ meas}$ and $C_{oss\ meas}$ are the characteristics of the power MOSFET included in the IC brick measured in chapter 3 (for the output capacitor, the complete vector that describes its variations with the drain-source voltage is considered). $nSizeFET$ is the size of the power MOSFET normalized to the size of the one included inside the IC brick (a value < 1 indicates a smaller MOSFET and a value > 1 a bigger MOSFET).

Figures C.1 and C.2 shows the evolution of the performances of the 2L-AHBF and 3L-FC-AHBF, respectively, with the size of the power MOSFET. For each version of the power stage, results are present for several design solutions that present different values of optimal operating frequency.

The results for both versions of the topology and for the various selected designs seem to point in the same direction: the performances of the converter (in nominal conditions so 400 V (or 800 V) to 12 V, 1W) would improve if the power MOSFET was smaller. The size for which the best performances would be achieved varies slightly, but for the 2L-AHBF it is located around 0.25 that is to say one quarter of the current power switch size.

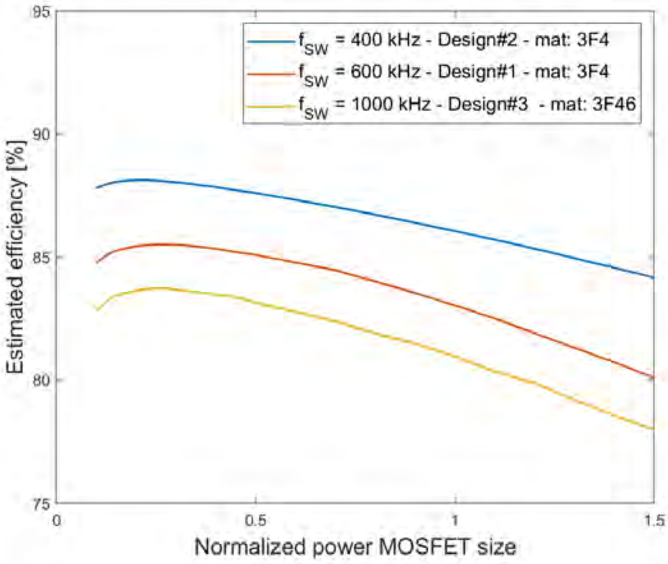


Figure C.1: Evolution of the estimated performances of the 2L-AHBF converter with the size of the power MOSFET for different designs

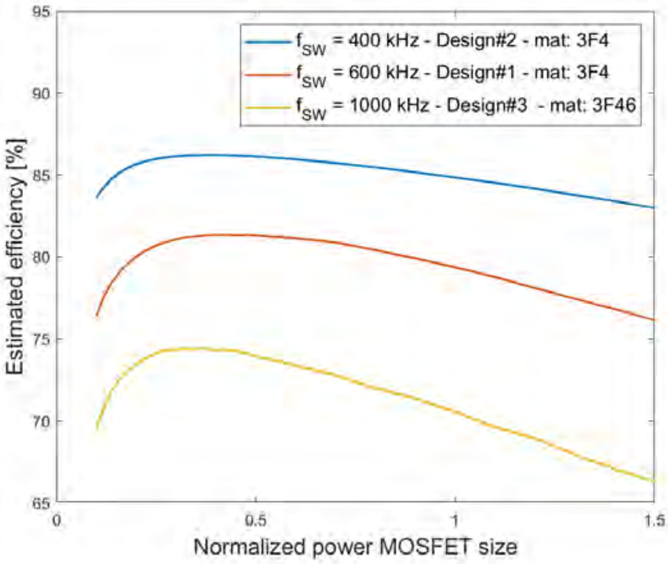


Figure C.2: Evolution of the estimated performances of the 3L-FC-AHBF converter with the size of the power MOSFET for different designs

These results can be explained by the limited on-time of the power switches, that lead to low conduction losses because it is the only moment when they generate losses. Since the on-time of the power switch is small, making their on-resistance larger does not critically increase the conduction losses. However, it allows to significantly reduce the quantity of parasitic capacitors to (dis)charge during the ZVS transitions and so to reduce the quantity of current required. Since the reduction of the current ripple allows to decrease the conduction losses in all the primary components, it is advantageous to reduce (to a certain extent) the size of the power MOSFETs.

Of course this quick analysis does not pretend to conclude on the exact size of the power MOSFET to select for the next design versions, as many other parameters would need to be taken into account like the limits of the process regarding the minimum size of the high-voltage devices, the thermal constraints, the saturation current, etc. However, the result suggest that in the context of high-voltage low-power, the importance of reducing the parasitic capacitors should not be neglected even if it translates into larger on-resistance for the power devices.

Appendix D

Steinmetz parameters for core losses estimation

The sets of Steinmetz parameters used to predict the core losses of 3F4 and 3F46 material are shown in Table D.1. The parameters were found on Ferroxcube's website, in "Design tools" section [92].

Table D.1: Steinmetz parameters for core losses estimation [92]

Material	Frequency [kHz]	k [mW/cm^3]	α	β
3F4	100-600	0.35	1.1	2.7
	600-1000	1.2×10^{-4}	1.7	2.7
	1000-3000	1.1×10^{-11}	2.8	2.4
3F46	1000-3000	5.0×10^{-11}	2.6	2.4

Bibliography

[1] Y. Nour and A. Knott, "Module integrated GaN power stage for high switching frequency operation," in *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*, IEEE, dec 2017.

[2] Cui Inc, *AE5-EW - 5 W, 10:1 Input Range, Single Regulated Output, 5 Pin DIP, 5600 Vdc Isolation, Dc-Dc Converter*, Sept. 2017.

[3] P. Alou, O. Garcia, J. Cobos, J. Uceda, and M. Rascon, "Flyback with active clamp: a suitable topology for low power and very wide input voltage range applications," in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, IEEE, 2002.

[4] N. Nielsen, "An ultra low-power off-line APDM-based switchmode power supply with very high conversion efficiency," in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, IEEE, 2001.

[5] S. Zhao, J. Zhang, and Y. Shi, "A low cost low power flyback converter with a simple transformer," in *Proceedings of The 7th International Power Electronics and Motion Control Conference*, IEEE, jun 2012.

[6] F. Cacciotto, "Off-line constant current LEDs driver using the HVLED primary controller," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, IEEE, nov 2010.

[7] A. M. Ammar, Y. Nour, and A. Knott, "A high-efficiency 1 MHz 65 w GaN-based LLC resonant DC-DC converter," in *2019 IEEE Conference on Power Electronics and Renewable Energy (CPERE)*, IEEE, oct 2019.

[8] T. Meng, C. Li, H. Ben, and J. Zhao, "An input-series flyback auxiliary power supply scheme based on transformer-integration for high-input voltage applications," *IEEE Transactions on Power Electronics*, vol. 31, pp. 6383–6393, sep 2016.

[9] Tamura Corporation, *SPM Power Modules (Power Supplies with Ultra-low Standby Power Consumption) - SPM1203SJ datasheet*, 2014.

[10] Texas Instruments, *Small Automotive High Input Voltage 3W Isolated Flyback - PMP8688 Test results*, 2013. last visited: March 2021.

[11] Infineon Technologies AG, *6W 400V-12V converter for industrial applications - demo board KIT-6W-12V-P7-950V - Engeenering report*, 2018. Last visited: march 31st, 2021.

[12] Texas-Instruments, *700V-860V input to 16.5V@0.5A output - Reference design: PMP7769 - Test results*, 2009. Last visited: march 31st, 2021.

[13] C. Wang, S. Xu, W. Shen, S. Lu, and W. Sun, "A single-switched high-switching-frequency quasi-resonant flyback converter," *IEEE Transactions on Power Electronics*, vol. 34, pp. 8775–8786, sep 2019.

[14] X. Huang, J. Feng, W. Du, F. C. Lee, and Q. Li, "Design consideration of MHz active clamp flyback converter with GaN devices for low power adapter application," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, mar 2016.

[15] J.-W. Kim, J. S. You, and B. H. Cho, "Input series-output parallel connected converter for high voltage power conversion applications employing charge control," in *SAE Technical Paper Series*, SAE International, aug 1999.

[16] R. Kosenko, A. Chub, and A. Blinov, "Feasibility study of cascading of full soft-switching current-fed naturally clamped DC-DC converters," in *2016 10th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, IEEE, jun 2016.

[17] S. Zong, Q. Zhu, W. Yu, and A. Q. Huang, "Auxiliary power supply for solid state transformer with ultra high voltage capacitive driving," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, mar 2015.

[18] X. Ma, J. Niu, and Y. Kang, "Two full-bridge input-series-output-parallel integrated-magnetic converter for high input voltage," in *2005 International Conference on Electrical Machines and Systems*, IEEE, 2005.

[19] Y. Cui and L. M. Tolbert, "High step down ratio (400 v to 1 v) phase shift full bridge dc/dc converter for data center power supplies with gan fets," in *The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications*, pp. 23–27, Oct 2013.

[20] R. Ayyanar, R. Giri, and N. Mohan, "Active input–voltage and load–current sharing in input-series and output-parallel connected modular DC–DC converters using dynamic input-voltage reference scheme," *IEEE Transactions on Power Electronics*, vol. 19, pp. 1462–1473, nov 2004.

[21] P. Grbovic, "Master/slave control of input-series- and output-parallel-connected converters: Concept for low-cost high-voltage auxiliary power supplies," *IEEE Transactions on Power Electronics*, vol. 24, pp. 316–328, feb 2009.

[22] R. Giri, V. Choudhary, R. Ayyanar, and N. Mohan, "Common-duty-ratio control of input-series connected modular DC-DC converters with active input voltage and load-current sharing," *IEEE Transactions on Industry Applications*, vol. 42, pp. 1101–1111, jul 2006.

[23] L. Fan, A. Knott, and I. H. H. Jorgensen, "A high-voltage low-power switched-capacitor DC-DC converter based on GaN and SiC devices for LED drivers," *Elektronika ir Elektrotechnika*, vol. 24, jun 2018.

[24] L. Fan, *Integrated Off-Line Power Converter.* PhD thesis, DTU, 2018.

[25] D. Lutz, P. Renz, and B. Wicht, "An integrated 3-mW 120/230-v AC mains micropower supply," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, pp. 581–591, jun 2018.

[26] S. Lim, J. Ranson, D. M. Otten, and D. J. Perreault, "Two-stage power conversion architecture suitable for wide range input voltage," *IEEE Transactions on Power Electronics*, vol. 30, pp. 805–816, feb 2015.

[27] T. McRae and A. Prodic, "Design oriented analysis of switched capacitor DC–DC converters," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 2–13, 2020.

[28] C. Le, D. L. Gerber, M. Kline, S. R. Sanders, and P. R. Kinget, "Reconfigurable hybrid-switched-capacitor-resonant LED driver for multiple mains voltages," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, pp. 1871–1883, dec 2018.

[29] A. Abdulslam and P. P. Mercier, "A symmetric modified multilevel ladder PMIC for battery-connected applications," *IEEE Journal of Solid-State Circuits*, vol. 55, pp. 767–780, mar 2020.

[30] S.-H. Kim, H. Cha, H. F. Ahmed, and H.-G. Kim, "Isolated double step-down DC-DC converter," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, IEEE, jun 2015.

[31] Y. L. . Z. Y. . R. C. N. Pilawa-Podgurski, "A gan-based 97switched-capacitor converter with lossless regulation capability," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, IEEE, sep 2015.

[32] C.-S. Leu, P.-Y. Huang, and B.-C. Lin, "A novel taiwan tech multi-level converter (TMC) for high-voltage input power conversion applications," in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, IEEE, jun 2017.

[33] X. Zhang, C. Yao, C. Li, L. Fu, F. Guo, and J. Wang, "A wide bandgap device-based isolated quasi-switched-capacitor DC/DC converter," *IEEE Transactions on Power Electronics*, vol. 29, pp. 2500–2510, may 2014.

[34] Y. Jiao and F. Luo, "N-switched-capacitor buck converter: topologies and analysis," *IET Power Electronics*, vol. 4, no. 3, p. 332, 2011.

[35] T. McRae, N. Vukadinovic, and A. Prodic, "Low-volume hybrid tap-connected SC-buck converter with shared output capacitor," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, mar 2017.

[36] C. Rindfleisch and B. Wicht, "11.3 a one-step 325v to 3.3-to-10v 0.5w resonant DC-DC converter with fully integrated power stage and 80.7% efficiency," in *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*, IEEE, feb 2020.

[37] T. Meynard and H. Foch, “Multi-level conversion: high voltage choppers and voltage-source inverters,” in *PESC ’92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, IEEE, 1992.

[38] V. Costa, P. M. dos Santos, and B. Borges, “A design methodology for integrated inductor-based DC–DC converters,” *Microelectronics Journal*, vol. 43, pp. 401–409, jun 2012.

[39] G. Noh and J. Ha, “Analysis and design of four-level flying-capacitor converter in burst mode operation,” in *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, pp. 3129–3134, 2019.

[40] H. Higa and J. ichi Itoh, “Derivation of operation mode for flying capacitor topology applied to three-level DAB converter,” in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, IEEE, nov 2015.

[41] A. Stillwell, M. E. Blackwell, and R. C. N. Pilawa-Podgurski, “Design of a 1 kV bidirectional DC-DC converter with 650 v GaN transistors,” in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, mar 2018.

[42] Z. Ye, Y. Lei, Z. Liao, and R. C. N. Pilawa-Podgurski, “Investigation of capacitor voltage balancing in practical implementations of flying capacitor multilevel converters,” in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, IEEE, jul 2017.

[43] J. Celikovic, R. Das, H.-P. Le, and D. Maksimovic, “Modeling of capacitor voltage imbalance in flying capacitor multilevel DC-DC converters,” in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, IEEE, jun 2019.

[44] E. Abdelhamid, G. Bonanno, L. Corradini, P. Mattavelli, and M. Agostinelli, “Stability properties of the 3-level flying capacitor buck converter under peak or valley current programmed control,” *IEEE Transactions on Power Electronics*, vol. 34, pp. 8031–8044, aug 2019.

[45] A. Stillwell, E. Candan, and R. C. N. Pilawa-Podgurski, “Active voltage balancing in flying capacitor multi-level converters with valley current detection and constant effective duty cycle control,” *IEEE Transactions on Power Electronics*, vol. 34, pp. 11429–11441, nov 2019.

[46] N. Vukadinovic, A. Prodic, B. A. Miwa, C. B. Arnold, and M. W. Baker, “Skip-duty control method for minimizing switching stress in low-power multi-level dc-dc converters,” in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, IEEE, jul 2015.

[47] T. Instruments, “An-2292 designing an isolated buck (fly-buck) converter (rev. c),” Application Note SNVA674C, Texas Instruments, 2014.

[48] W. Chen, P. Xu, and F. Lee, “The optimization of asymmetric half bridge converter,” in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, IEEE, 2001.

[49] T.-M. Chen and C.-L. Chen, “Analysis and design of asymmetrical half bridge flyback converter,” *IEE Proceedings - Electric Power Applications*, vol. 149, no. 6, p. 433, 2002.

[50] J. Feng, Y. Hu, W. Chen, and W. Chau-Chun, “ZVS analysis of asymmetrical half-bridge converter,” in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, IEEE, 2001.

[51] L. Huber and M. M. Jovanovic, “Analysis, design, and performance evaluation of asymmetrical half-bridge flyback converter for universal-line-voltage-range applications,” in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, mar 2017.

[52] S.-S. Lee, S.-K. Han, and G.-W. Moon, “Analysis and design of asymmetrical ZVS PWM half bridge forward converter with flyback type transformer,” in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, IEEE, 2004.

[53] M. Li, Z. Ouyang, and M. A. Andersen, “Analysis and optimal design of high frequency and high efficiency asymmetrical half-bridge flyback converters,” *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2019.

[54] D. Reusch, F. Lee, and M. Xu, “Three level buck converter with control and soft startup,” in *2009 IEEE Energy Conversion Congress and Exposition*, IEEE, sep 2009.

[55] X. Liu, P. K. T. Mok, J. Jiang, and W.-H. Ki, “Analysis and design considerations of integrated 3-level buck converters,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, pp. 671–682, may 2016.

[56] Z. Liu, L. Cong, and H. Lee, “Design of on-chip gate drivers with power-efficient high-speed level shifting and dynamic timing control for high-voltage synchronous switching power converters,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 6, pp. 1463–1477, 2015.

[57] D. Liu, S. J. Hollis, and B. H. Stark, “A new design technique for sub-nanosecond delay and 200 v/ns power supply slew-tolerant floating voltage level shifters for gan smps,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 3, pp. 1280–1290, 2019.

[58] Z. Liu and H. Lee, “A 100v gate driver with sub-nanosecond-delay capacitive-coupled level shifting and dynamic timing control for ZVS-based synchronous power converters,” in *Proceedings of the IEEE 2013 Custom Integrated Circuits Conference*, IEEE, sep 2013.

[59] F. Li, D. Giannopoulos, and I. Wacyk, “A low loss high-frequency half-bridge driver with integrated power devices using EZ-HV SOI technology,” in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, IEEE, 2002.

[60] ON Semiconductor, *AN-6076 ; Design and Application Guide of Bootstrap Circuit for High-Voltage Gate-Drive IC*, Jan. 2018. Rev. 2.

[61] Infineon - Internation Rectifier, *Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality*.

[62] B. Welchko, M. de Rossiter Correa, and T. Lipo, “A three-level MOSFET inverter for low-power drives,” *IEEE Transactions on Industrial Electronics*, vol. 51, pp. 669–674, jun 2004.

[63] Z. Ye, Y. Lei, W.-C. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, “Improved bootstrap methods for powering floating gate drivers of flying capacitor multilevel converters and hybrid switched-capacitor converters,” *IEEE Transactions on Power Electronics*, vol. 35, pp. 5965–5977, jun 2020.

[64] W. Hurley, W. Wolfle, and J. Breslin, “Optimized transformer design: inclusive of high-frequency effects,” *IEEE Transactions on Power Electronics*, vol. 13, pp. 651–659, jul 1998.

[65] Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, “Optimal design and tradeoff analysis of planar transformer in high-power DC–DC converters,” *IEEE Transactions on Industrial Electronics*, vol. 59, pp. 2800–2810, jul 2012.

[66] R. Jabr, “Application of geometric programming to transformer design,” *IEEE Transactions on Magnetics*, vol. 41, pp. 4261–4269, nov 2005.

[67] O. C. Spro, P. Lefranc, S. Park, J. M. Rivas-Davila, D. Peftitsis, O.-M. Midtgard, and T. Undeland, “Optimized design of multi-MHz frequency isolated auxiliary power supply for gate drivers in medium-voltage converters,” *IEEE Transactions on Power Electronics*, vol. 35, pp. 9494–9509, sep 2020.

[68] R. Prieto, O. Garcia, R. Asensi, J. Cobos, and J. Uceda, “Optimizing the performance of planar transformers,” in *Proceedings of Applied Power Electronics Conference. APEC*, IEEE, 1996.

[69] S. R. Cove, M. Ordonez, and J. E. Quaicoe, “Modeling of planar transformer parasitics using design of experiment methodology,” in *CCECE 2010*, IEEE, may 2010.

[70] J. S. N. T. Magambo, R. Bakri, X. Margueron, P. L. Moigne, A. Mahe, S. Guguen, and T. Bensalah, “Planar magnetic components in more electric aircraft: Review of technology and key parameters for DC–DC power electronic converter,” *IEEE Transactions on Transportation Electrification*, vol. 3, pp. 831–842, dec 2017.

[71] C. McLyman, *Transformer and Inductor Design Handbook, Third Edition.* Electrical Engineering and Electronics Series, Taylor & Francis, 2004.

[72] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, “Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters,” in *2002 IEEE Workshop on Computers in Power Electronics, 2002. Proceedings.*, IEEE, 2002.

[73] P. Dowell, “Effects of eddy currents in transformer windings,” *Proceedings of the Institution of Electrical Engineers*, vol. 113, no. 8, p. 1387, 1966.

[74] J. Ferreira, “Improved analytical modeling of conductive losses in magnetic components,” *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 127–131, 1994.

[75] A. Reatti and M. Kazimierczuk, “Comparison of various methods for calculating the AC resistance of inductors,” *IEEE Transactions on Magnetics*, vol. 38, pp. 1512–1518, may 2002.

[76] A. Fouineau, M.-A. Raulet, B. Lefebvre, N. Burais, and F. Sixdenier, “Semi-analytical methods for calculation of leakage inductance and frequency-dependent resistance of windings in transformers,” *IEEE Transactions on Magnetics*, vol. 54, pp. 1–10, oct 2018.

[77] B. Rao, Y. Zhao, Y. Yang, J. Gao, Z. Zhang, S. Zhou, M. Zhang, and Z. Chen, “Reduction of leakage inductance and AC resistance of planar transformers by optimising the current distribution,” *IET Power Electronics*, vol. 11, pp. 501–506, mar 2018.

[78] R. BARLIK, “Determination of the basic parameters of the high-frequency planar transformer,” *PRZEGLKAD ELEKTROTECHNICZNY*, vol. 1, pp. 73–80, jun 2016.

[79] P. Ranstad and H.-P. Nee, “On the distribution of AC and DC winding capacitances in high-frequency power transformers with rectifier loads,” *IEEE Transactions on Industrial Electronics*, vol. 58, pp. 1789–1798, may 2011.

[80] L. Dalessandro, F. da Silveira Cavalcante, and J. W. Kolar, “Self-capacitance of high-voltage transformers,” *IEEE Transactions on Power Electronics*, vol. 22, pp. 2081–2092, sep 2007.

[81] T. Duerbaum and G. Sauerlaender, “Energy based capacitance model for magnetic devices,” in *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181)*, IEEE, 2001.

[82] B. Ackermann, A. Lewalter, and E. Waftenschmidt, “Analytical modelling of winding capacitances and dielectric losses for planar transformers,” in *2004 IEEE Workshop on Computers in Power Electronics, 2004. Proceedings.*, IEEE, 2004.

[83] M. Prieto, A. Fernandez, J. Diaz, J. Lopera, and J. Sebastian, “Influence of transformer parasitics in low-power applications,” in *APEC '99. Fourteenth Annual Applied Power Electronics Conference and Exposition. 1999 Conference Proceedings (Cat. No.99CH36285)*, IEEE, 1999.

[84] C. K. Lee, Y. P. Su, and S. Y. R. Hui, “Printed spiral winding inductor with wide frequency bandwidth,” *IEEE Transactions on Power Electronics*, vol. 26, pp. 2936–2945, oct 2011.

[85] Ferroxcube, *3F4 Material specification*, Sept. 2008. Last visited: march 31st, 2021.

[86] Ferroxcube, *3F36 Material specification*, [online], available at: `https://www.ferroxcube.com/en-global/ak_material/index/power_conversion#6` ed., June 2013. Last visited: march 31st, 2021.

[87] Ferroxcube, *3F46 Material specification*, [online], available at: `https://www.ferroxcube.com/en-global/ak_material/index/power_conversion#6` ed., Mar. 2016. Last visited: march 31st, 2021.

[88] A. Maswood and Z. K. Yoong, “Digital burst technique in the stand-by operation of a TV power supply,” in *Conference Record of the 1999 IEEE Industry Applications Conference. Thirty-Forth IAS Annual Meeting (Cat. No.99CH36370)*, IEEE, 1999.

[89] J. ho Choi, D. young Huh, and Y. seok Kim, “The improved burst mode in the stand-by operation of power supply,” in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC*, IEEE, 2004.

[90] H.-S. Choi and D. Huh, “Techniques to minimize power consumption of SMPS in standby mode,” in *IEEE 36th Conference on Power Electronics Specialists, 2005.*, IEEE, 2005.

[91] Texas Instruments, *Three-Phase AC and DC Input to 24V at 125mA Quick-Startup Isolated Flyback Reference Design - PMP10195 – Test results*, 2016. last visited: March 2021.

[92] Ferroxcube, *Ferroxcube's materials - Steinmetz coefficients*, [online], available at: `https://www.ferroxcube.com/en-global/design_tool/index` ed. Last visited: march 31st, 2021.

FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : FORAY DATE de SOUTENANCE : 20/07/2021

Prénoms : Etienne

TITRE : Design of an integrated high-voltage low-power isolated DC/DC converter for automotive applications

NATURE : Doctorat Numéro d'ordre : 2021LYSEI043

Ecole doctorale : ELECTRONIQUE, ELECTROTECHNIQUE, AUTOMATIQUE

Spécialité : Génie Electrique

RESUME : Dans le contexte actuel de transitions écologique et énergétique, une multiplication des bus DC haute-tension est observée dans certaines applications telles que les véhicules électriques ou le photovoltaïque. En parallèle, certains systèmes requièrent d'être alimentés directement à partir de la source principale d'énergie : pour l'automobile, l'exemple du Pyroswitch peut être cité. Il s'agit d'un actionneur dont le rôle est de déconnecter physiquement la batterie haute-tension du véhicule électrique en cas d'accident et qui, pour des raisons de sécurité, doit être alimenté directement par la batterie principale (dont la tension aujourd'hui est proche de 400V voire 800V). Ainsi nait le besoin d'un convertisseur DC/DC isolé avec une forte tension d'entrée et une faible tension et puissance en sortie. De fortes contraintes liées au contexte (notamment automobile) sont placées sur le convertisseur, en termes de coût, de taille et de rendement.
Les convertisseurs actuellement disponibles sur le marché ou dans la littérature montrent une faible diversité des solutions proposées. Ils sont majoritairement basés sur une architecture similaire, qui bien qu'économique, présente de sérieuses limites en termes de performances (faible tension maximale et faible rendement). Ainsi, le design d'un convertisseur 800V-12V avec une puissance proche de 1W en sortie ne peut se satisfaire des approches utilisées classiquement, en particulier au vu du haut niveau de rendement visé (>85%).
L'approche proposée dans cette thèse se base sur deux des principales techniques utilisées pour créer des convertisseurs de puissance : l'intégration sur puce (ou au sein d'un même package) de plus en plus d'éléments du convertisseur ; et les « modules de puissance » qui assemblent une série de composants discrets. Cette thèse propose donc d'allier les avantages de chacune de ces techniques pour créer le convertisseur voulu. En particulier, l'intégration des composants actifs permet une remise en question de l'architecture de l'étage de puissance du convertisseur ainsi qu'une augmentation significative de la fréquence de fonctionnement, qui devrait contribuer à la diminution de la taille des composants passifs. Cependant, les limites des technologies d'intégration ne permettent pas de viser l'intégration des éléments les plus volumineux du convertisseur, comme le transformateur, et une attention toute particulière est donc portée à leur dimensionnement.
Dans cette thèse, une étude de différentes topologies pour l'étage de puissance du convertisseur DC/DC isolé est d'abord menée. Elle permet d'identifier les structures les plus prometteuses en comparant un nombre limité de critères qualitatifs. Une topologie est retenue compte tenu d'un bon compromis entre performances et complexité : les convertisseurs multi-niveaux à capacités flottantes. La création d'un circuit intégré (IC) permettant l'intégration des éléments actifs de l'étage de puissance est ensuite présentée. Une solution est présentée pour contourner les limites imposées par la technologie choisie (Bulk Silicium haute-tension) en termes d'isolation entre composants. Ensuite, une méthodologie de conception d'un transformateur planaire adapté au contexte et à l'application est introduite afin de prendre en compte les principaux paramètres de dimensionnement d'un tel composant. À l'issue de cette étape, quelques transformateurs sont proposés pour être mesurés au sein du convertisseur complet. Enfin, les différentes composantes du convertisseur sont assemblées et des mesures de rendement sont réalisées sur plusieurs points de fonctionnement proches de ceux définis par l'application. Les résultats des transformateurs les plus performants sont à la hauteur des attentes et offrent une nette amélioration des performances par rapport aux solutions de l'état-de-l'art, notamment en termes de rendement.

MOTS-CLÉS : Convertisseur DC-DC isolé, haute-tension basse-puissance, circuit intégré, transformateur planaire

Laboratoire (s) de recherche : Ampère UMR CNRS 5005

Directeur de thèse: Bruno Allard, Professeur des Universités, INSA de Lyon

Président de jury : Mme Ben Dhia S., Professeur, LAAS/CNRS, Toulouse

Composition du jury :

M. Lembeye Y., Professeur, G2ELab Grenoble
M. Wicht B., Professeur, Leibniz University Hannover
Mme Alonso C., Professeur, LAAS/CNRS, Toulouse
Mme Ben Dhia S., Professeur, LAAS/CNRS, Toulouse
M. Prodic A., Professeur, University of Toronto
M. Allard B., Professeur, Ampère, INSA Lyon
M. Martin C., Professeur, Ampère, UCBL