

Study of temperature and moisture impact on water diffusion in materials and on electronic circuits failure mechanisms.

Vivien Cartailler

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SPÉCIALITÉ ÉLECTRONIQUE

Par Vivien CARTAILLER

Impact de la température et de l'humidité sur la diffusion de l'eau dans les matériaux et sur les mécanismes de défaillance des circuits

Sous la direction de : Hélène FRÉMONT Co-directrice : Geneviève DUCHAMP

Soutenue le 19/10/2021

Membres du jury :

Mme. LE BIHAN, France M. GAUTIER, Gaël M. DROUIN, Dominique Mme. FRÉMONT, Hélène Mme. DUCHAMP, Geneviève M. IMBERT, Grégory Professeur des Universités, Université de Rennes 1 Professeur des Universités, INSA-CVL Professeur des Universités, Université de Sherbrooke Professeur des Universités, Université de Bordeaux Professeur des Universités, Université de Bordeaux Ingénieur, STMicroelectronics Présidente Rapporteur Rapporteur Examinatrice Examinatrice Examinateur

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Acronyms

ALD: Atomic Layer Deposition **BEOL:** Back End of Line **CMP:** Chemical mechanical polishing CVD: chemical vapor deposition **EDX:** energy dispersive X-ray spectroscopy **EELS:** Electron Energy Loss Spectroscopy FEOL: Front End of Line **FIB:** Focused ion beam **HAST:** Highly accelerated stress test HBM: Hybrid bonding metal HBV: Hybrid bonding via **IMD:** Inter-metal dielectrics **IR:** Infrared **IRDS:** International Roadmap for Semiconductors **MTTF:** Mean Time to Failure **RH:** Relative Humidity **SiCN:** Silicon Carbonitride SiN: Silicon Nitride SiON: Silicon Oxynitride SiP: System in Package **TEM:** Transmission electron microscopy **TEOS:** Tetraetoxysilane THS: Thermal and Humidity Storage Tof-SIMS: Time of Flight – Secondary Ion Mass Spectrometry TSV: Through silicon via **ULK:** Ultra Low k

USG: Undoped Silica Glass

Via: Vertical Interconnect access

General introduction

If one field has not suffered much from the recent economic crisis linked to the Covid pandemic, it is the microelectronic industry. The demand for electronic accessories has boomed and each of these devices contain multiple microelectronic chips. It encourages all actors in the field to pursue their investment in innovation to stay ahead of the concurrence (TSMC plans to invest over 100 billion over the next three years [1]). As of 2021, a few actors remain in the rat race for miniaturization such as Intel and TSMC that already announced plans for 3nm and below.

Other actors cannot afford to join this race and a second path, apart from the Moore law approach (also referred to as More Moore), emerged in the last decade. This alternative approach, called More than Moore, is based on the philosophy of adding more functionalities inside a die instead of densifying the number of transistors.

These different approaches both lead to new reliability challenges and more stringent reliability requirements. Extremely small parameter variations are enough to endanger the entire circuit functionality. In both approaches, porous insulating layers are now widely used and will be until a breakthrough occurs. These layers are challenging from a mechanical perspective and they are prone to environmental contaminations. With the More than Moore way, new dies architectures are developed. For instance, 3D integration offers the possibility to directly interconnect two dies on top of each other.

The focus of this work is put on one factor that can be particularly detrimental to device performance: moisture. Extremely small quantities of moisture degrade the overall reliability of a microelectronic chip.

As one would expect, moisture is not supposed to reach the inner part of an electronic circuit. The first protection against moisture is offered by the chip package that connects the inner circuit to the outside (Fig. 1). Both ceramic and organic packages exist; the first one only being used for specific application due to its cost. For most commercial applications, polymeric package is the norm. But these materials are not hermetic and moisture diffuses through.



Figure 1: Schemactic of a chip package (wire bonding technology)

Once moisture has diffused through the package it encounters the inner protective layers. Fig. 2 offers a simplified schematic of the protection against environmental contaminations:

- Bottom side diffusion: the entire integration is performed on silicon substrate that is known to be hermetic, thus, it protects the die from bottom diffusion.
- Top side diffusion: Dense dielectric layers like silicon nitrides, called passivation layers, are deposited and protect from top side diffusion.
- Lateral diffusion: A continuous surrounding metal ring, also called seal ring, protects the die mechanically and also from environmental contaminations.





Hence, moisture should never reach the inner part of a microelectronic chip. Yet, failure modes linked to moisture are observed occasionally. To understand how it can occur, we first describe a classical microelectronic stack.

An integrated circuit can be divided into two main parts as shown in Fig. 3:

- Front End of Line (FEOL): it is composed of the very first layers deposited on the silicon substrate. The active devices, the transistors, are located in the FEOL.
- Back End of Line (BEOL): above the FEOL layers, metallic interconnections connect the transistor with the outside (with a via/line network). Most chips use copper but aluminum can still be used for some applications. To insulate one line from another, materials with low dielectric constant are deposited.

As shown in Fig. 2 and 3, the surrounding seal ring is composed of a continuous metal via/line network. It is usually composed of several adjacent wall a shown in Fig. 3.

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Figure.3: Schematic cross section of an integrated circuit

One of the objectives of the Moore law has been to reduce the signal propagation delays on line. One of the major steps was achieved in 1997 when IBM replaced aluminum by copper for interconnections. The focus was then put on developing dielectric materials with lower permittivity. It led to porous layers more prone to moisture diffusion. These materials are located in the first BEOL levels.

As a first approach, the interconnexions can be represented as an equivalent circuit with two metal lines separated by a dielectric material. With this simplified model, the signal propagation delay is proportional to the resistivity R of the metal lines and the capacitance C between these lines. The RC product can be expressed with the physical parameters of the materials and the geometrical parameters of the line as shown in Eq. (1).

$$RC = \frac{\rho L}{hW} \times \frac{\varepsilon \varepsilon_0 L h}{d} \quad (1)$$

Where ρ is the resistivity of the metal line and L, W and h are respectively its length, width and thickness. d is the distance between two adjacent metal lines. ε_0 is the void permittivity and ε is the permittivity of the dielectric layer. Fig. 4 gives a schematic of these parameters.



Figure.4: Schematic of the parameters involved in the RC delay calculation

If a defect exists either in the surrounding seal ring or in the passivation layers, moisture can potentially reach the BEOL levels. These defects can be a crack in the passivation or an insufficient via length in the seal ring, which both give an opening for moisture to diffuse in.

When moisture diffuses into the dielectric layers, it increases the permittivity of the layer due to its high dielectric constant (around 79 while dielectric constant of common silicon dioxide is around 4). Hence, it increases the RC delays, which first translates into a performance loss. Then, the presence of moisture can lead to hard failure modes (galvanic corrosion, mechanical delamination).

The effect of moisture on porous dielectrics has been widely studied. However, there is lack of knowledge on the exact interactions between moisture and the materials depending on the temperature and humidity conditions.

The objective of this thesis is to give a better understanding of the interactions between moisture and new integrated stacks used by STMicroelectronics. These new integrated stacks are:

- 3D integrated stacks that have discontinuous seal ring at the bonding level (Chapter IV)
- Stacks with a cut in their surrounding seal ring for a potential radio frequency application (Chapter V)

The risks of moisture diffusion in these stacks need to be assessed. Starting from scratch, we follow a global approach. First, the main dielectric materials are characterized. Their diffusion parameters are determined. Then, knowing intrinsic behavior of the dielectric layers, integrated stacks are studied. Numerical simulations are used to link these two parts.

Hence, the manuscript is divided in two main parts. The first part (Chapter I and II) is dedicated to intrinsic material characterization and the second one (Chapter III to V) to the study of moisture diffusion in integrated stacks.

In Chapter I, we introduce the dielectric layers studied. They cover the main families used in the back end of line. The characterization techniques are also presented. Due to the high number of measurements, we selected simple and fast techniques. We compared three of them in this chapter. The objective is twofold. First, we want to confirm that the three techniques lead to the same value of diffusion coefficient. Second, we want to select the most appropriate technique to study an important number of wafers at the same time.

Chapter II is dedicated to the study of the different layers at different environmental conditions. First, we determine the diffusion parameters for all layers at a standard 85°C and 85% relative humidity (RH). Then, with additional characterizations, the specific behaviors of several dielectric families are investigated. These parameters will be used to explain moisture absorption in integrated stacks and to feed numerical simulation. Additionally, we investigate the influence of temperature and relative humidity on the diffusion parameters of a dense SiO₂.

In Chapter III, we provide an overview of the literature of moisture diffusion in integrated stacks followed by a brief description of 3D integration with a focus on hybrid bonding. Then, the electrical characterization used in Chapter IV and V are introduced.

In Chapter IV, we perform a complete investigation of moisture absorption in 3D integrated stacks. First, we assess the reliability of such stacks toward moisture. Then, the surrounding seal ring is sawn on one side to create a path for moisture to diffuse in. The impact of moisture diffusion is assessed with electrical measurements combined with physical and chemical

analyses and numerical simulations. The objective is to clarify moisture diffusion path in such stacks and its interactions with dielectric materials.

In the last Chapter, we investigate moisture diffusion in dies dedicated to radio frequency applications. A particular feature of these die is to include an opening in their surrounding seal ring, which constitutes a prime diffusion path for moisture. A model based on the Black law used to study electromigration is developed in order to determine moisture absorption at various environmental conditions for these structures.

Finally, the main findings of this work are gathered and several recommendations for a future work are presented.

Chapter I

Methods to characterize moisture diffusion in dielectrics

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In this chapter, the first objective is to introduce the theoretical context and the methods we use to characterize the dielectric layers present in the BEOL levels. The second objective is to select the most appropriate measurement technique to monitor an important number of wafers during environmental storage.

After a description of the equations based on Fick's laws and the process of moisture absorption in dielectric layers, we introduce the six dielectric layers selected. They cover the different families present in the BEOL levels (dense and porous inter metal dielectrics and capping layers).

Then, the measurement techniques and storage methods are presented. One of the objectives of the PhD is to characterize the six selected dielectric layers at various environmental conditions (Chapter II) as mentioned in the general introduction. Hence, in the last section of this chapter we compare three techniques described previously – gravimetric monitoring, intrinsic stress measurements and infrared spectroscopy – to determine diffusion parameters and select the most appropriate method to monitor many wafers at the same time.

I.1. Moisture diffusion in dielectric materials

Before introducing the dielectric materials selected for this study and the different techniques used to characterize their intrinsic behavior regarding moisture diffusion, we describe the general principles and theoretical context of moisture diffusion in thin dielectric layers.

The moisture absorption of dielectric materials is characterized with two parameters: the diffusion coefficient D in $cm^2.s^{-1}$ and the saturated moisture concentration C_{sat} in $mg.cm^{-3}$.

The diffusion coefficient depends on the interactions between moisture and the materials but also on the accessibility of reactive sites. Its Arrhenius behavior is well known and has been characterized for a wide range of materials. For dielectric layers, mainly SiO₂ types films have been characterized [2]–[5]. Recent studies mainly focus on the development of new moisture barrier layers for solar cells or organic light-emitting diodes with very low water vapor transmission rates [6]–[8]. This requires dense materials, hence, atomic layer deposition (ALD) is often chosen over plasma enhanced chemical vapor deposition (PECVD) due to its better conformity. Thus, there is a lack of data for the diffusion coefficient of PECVD dielectric layers widely used in the back end of line (BEOL) such as porous materials.

It is also true for the saturated moisture concentration, which corresponds to the maximal quantity of moisture that a material can absorb at a given temperature and humidity level. This parameter depends on the number of absorbing sites (nanopores, polar groups, dangling bonds).

Different types of bond can be formed between moisture and dielectric layers. Proost listed the different -OH species related to moisture for siloxane-based dielectrics with their associated dissociation energy [9] as represented in Fig. I.1.

At low temperatures, mainly physisorbed water should be present in dielectric layers due to the lower energy required. However, due to the random nature of PECVD, some layers contain dangling bonds that easily link with moisture to form covalent bonds.



Figure I.1: Types of -OH species (a) with their associated dissociation energy (b). Reproduced from [9]

The theoretical frame to study moisture diffusion is given by Fick's laws. Diffusion is the result of a concentration gradient from the high concentration to the low concentration areas. In the case of a one-dimensional diffusion, the equations linking the moisture diffusion flux F with moisture concentration C and moisture diffusion coefficient D are:

$$\frac{dC(x,t)}{dt} = D \frac{d^2C(x,t)}{dx^2} \quad (I.1)$$

and

$$F(x,t) = -D\frac{dC(x,t)}{dt} \quad (I.2)$$

Crank presented approached solutions to Eq. I.1 depending on its boundary conditions [10]. We describe the solution for a layer deposited on an impermeable substrate. All along this study we consider that the diffusion coefficient is constant and not concentration dependent.

• Solution for a layer deposited on an impermeable substrate

In this chapter and the next, we study dielectric materials directly deposited on silicon substrate as shown in Fig. I.2.



Figure I.2: Configuration used to determine diffusion properties

At the same time as studying dielectric films, we monitored the mass and bending radius of curvature of a silicon substrate alone in clean room conditions for several months. No variation was observed over time, which confirms the hermeticity of the silicon. Hence, the silicon substrate is considered impermeable in this work.

The configuration presented in Fig. I.2 corresponds to the case of a layer deposited on top of an impermeable substrate. The wafers have a diameter of 300 mm and layers thicknesses are only up to 600 nm. Thus, diffusion can be considered one dimensional (it corresponds to the case of a semi-infinite plane). The storages are performed in a clean room environment or in an environmental chamber. In both cases, the concentration of moisture is constant in the atmosphere, thus, it is maintained constant at the surface of the studied layers.

With these previous hypotheses, Crank gave the number of water molecules that has entered the layer of thickness h at time t. It is presented in [10]:

$$\frac{N(t)}{N_{\infty}} = 1 - \sum_{k=0}^{\infty} \frac{8}{(2k+1)^2 * \pi^2} e^{-\frac{D(2k+1)^2 \pi^2 t}{4h^2}}$$
(I.3)

Where N(t) is the number of water molecules per unit surface area absorbed at time t, N_{∞} is the corresponding quantity after infinite time, D is the diffusion coefficient.

This equation can be applied to any material properties X(t) that is proportional to the parameter N(t) such as the mass, the intrinsic stress, the dielectric constant.

$$\frac{X(t)}{X_{\infty}} = 1 - \sum_{k=0}^{\infty} \frac{8}{(2k+1)^2 * \pi^2} e^{-\frac{D(2k+1)^2 \pi^2 t}{4h^2}}$$
(I.4)

We use the method of least squares, under Scilab©, to find the diffusion parameters that minimize S in Eq. I.5.

$$S = \sum_{i} \left(X_{exp}(t_{i}) - X_{th}(t_{i}) \right)^{2} \quad (I.5)$$

Where X_{exp} represents the experimental values and X_{th} represents the theoretical values obtained with Eq. I.4.

Fig. I.3 presents an example of the mass uptake of a dense SiO₂:H at 85°C/85% RH as a function of the square root of time. The mass increases linearly until the saturated moisture uptake is reached. With these experimental data, both the diffusion coefficient and the saturated moisture concentration can be determined. The order of magnitude for diffusion coefficients is below 10^{-14} cm².s⁻¹ for the dielectrics studied.



Figure I.3: Relative moisture uptake of a dense SiO₂ at 85°C/85% RH fitted with a Fickian model

In this section, the theoretical context of moisture diffusion in thin dielectric layers has been introduced. In the next section, the deposition technique and the different dielectric materials investigated are presented.

I.2. Deposition techniques and materials

Several deposition techniques are used to deposit dielectric materials. For insulating layers in the back end of line, a deposition temperature below 400°C is required to avoid reliability issues. Higher temperatures would degrade active elements in the FEOL. In our case, only plasma enhanced chemical vapor deposition was used. We studied insulating layers (dense SiO₂ and low k) and capping layers (SiCN). This section starts with a description of the PECVD process. Then, the materials studied are described.

I.2.1. Plasma enhanced chemical vapor deposition (PECVD)

PECVD is widely used to obtain amorphous dielectric layers with deposition temperature under 450°C. The wafer is placed on a heating chuck under low pressure (around or below 10 Torr). Precursors are brought in the reaction chamber by carrier gas (Fig. I.4). Then, a plasma, which is generated between two electrodes, gives the necessary energy to dissociate the precursors. The dissociated molecules react at the surface of the wafer – absorption and diffusion followed by reaction between the different molecules – to create the desired layer. The main parameters to control the growth are:

- Precursors type
- Precursors ratio
- Temperature inside the chamber
- Plasma power
- Pressure inside the chamber



Figure I.4: Schematic of the PECVD process

Different Producer tools from Applied Materials or Novellus Inc were used to obtain our layers. Some of the parameters for each layer are detailed in the next section.

I.2.2. Description of the dielectric layers

We only focus on inter-metal dielectrics (IMD) and capping layers in our work. These materials are used in the BEOL of integrated circuits. In total, six materials have been studied individually.



Figure I.5: Schematic of two metal levels in BEOL

• Insulating layers

For decades, dense PECVD SiO₂ have been used to fill the gaps between metal lines. Several material changes came along with circuits miniaturization. For metals, copper replaced aluminum due to its lower electrical resistivity. The introduction of TaN and TaN/Ta, as metal barrier, followed and replaced TiN. With increasing miniaturization, the dielectric constant of inter-metal dielectrics (k ~ 4) became limiting. The development of new materials led to carbonated silicon oxides. The methyl groups reduce the permittivity due to the lower polarizability of Si-CH₃ compared to Si-O bonds [11]. They also induce free volume due to steric effect. This free volume lowers the permittivity thanks to dielectric constant of air (k = 1).

The next step to lower k is to increase the porosity of the dielectric films by introducing nano porosity. Ultra Low-k (ULK) materials are build of SiOC:H matrix in which a porogen is added. After deposition, UV cure step is performed to remove the porogen. Fig. I.6 represents the bulk structure of ULK with UV cure (reproduced from Gourhant [12]).



Figure I.6: Bulk structure of ULK. Reproduced from Gourhant [12]

• Copper diffusion barriers

Copper diffuses into IMD if they are directly in contact with [13], [14]. To prevent this phenomenon, TaNTa layers and capping layers are deposited as shown in Fig. I.5. Progressively, silicon nitrides (SiN) have been replaced by silicon carbonitrides (SiCN) due to their lower permittivity. SiN are known to be good moisture barrier [15], one of the reason being their high density. However, SiCN are less dense, and thus, they should be more sensitive to moisture diffusion.

The process parameters used during the deposition of each layer are gathered in Table I.1. The plasma frequency is 13.56 MHz for all films. In the rest of the manuscript we often refer to each layer as their name described in the column "Material".

	Material	Precursors	Deposition Temperature (°C)	RF power (W)	Thickness (nm)
Dense	USG	N ₂ O, SiH ₄	400	2 150	200-600
SiO ₂	TEOS	TEOS, He, O ₂	380	780	250
	Low k	TMS, He, O ₂	350	1100	280
SiOC	ULK	mDEOS, BCHD, O ₂	300 + UV cure at 380°C	400	320
Capping	SiCN 335	NH ₃ , TMS, He	335	465	150
layers	SiCN 350	NH ₃ , TMS, He	350	915	150

Table I.1: Process parameters for the deposition of each layer

I.3. Measurement techniques at wafer level

In this section, we detail the measurement techniques used to characterize moisture diffusion at wafer level in Chapter I and II.

I.3.1. Gravimetric monitoring

A tool from METRYX was used to perform mass monitoring. The measurement uncertainty is 40 μ g. Since materials were stored in a clean room, there was no contamination source. Hence, we assume that the mass uptake in only due to moisture diffusion and is homogeneous over the entire thickness. M₀ corresponds to the mass after deposition and M_∞ to the mass measured after saturation. With the previous assumption, the saturated mass uptake Δ M is given by:

$$\Delta M = M_{\infty} - M_0 (I.6)$$

The relative mass uptake $\Delta M_{\%}$ is given by:

$$\Delta M_{\%} = \frac{M_{\infty} - M_0}{M_0} \quad (I.7)$$

And the saturated moisture concentration C_{sat} in mg.cm⁻³ is obtained from the saturated mass uptake and layer volume V as follow:

$$C_{sat} = \frac{\Delta M}{V}$$
 (I.8)

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We monitored different thicknesses of a dense SiO_2 to confirm the homogeneous uptake assumption. The results are presented in Fig. I.7.



Figure I.7: Mass uptake of a 200 nm, 400 nm and 600 nm PECVD SIO2 (USG) as a function of square root of time (a). Relative mass uptake as a function of square root of time normalized by the thickness of each layer (b)

These results confirm that moisture is homogeneous for PECVD SiO₂. This is clearly visible in Fig. I.7(b) where the square root of time was normalized by the thickness of each layer. They all have the same relative saturated moisture concentration and the same normalized duration to reach this saturation.

Fig. I.7(a) also clearly shows that a thinner layer significantly reduces the duration required to reach saturation (around 400 hours for the 600 nm layer versus only 100 hours for the 200 nm).

Hence, the assumption of a homogeneous moisture uptake is true for PECVD SiO₂. We did not perform the same experiment for SiCN layers and SiOC:H layers. But additional results corroborate a homogeneous moisture uptake for these layers too. For SiOC:H, in section I of Chapter II, a simple calculus shows that a mass uptake over the entire free volume offered by nanopores is consistent. And in section 2 of Chapter II, a chemical analysis shows an oxygen increases over the entire thickness of SiCN when exposed to moisture. Thus, for all materials investigated in our work, an homogeneous moisture uptake is consistent.

I.3.2. Intrinsic stress

The deposition of a dielectric film on a silicon substrate induces a stress. Part of it is due to the difference of thermal expansion coefficients between the two layers as shown in Fig. I.8. The nature of the deposited layer also changes the stress, it can be referred to as intrinsic stress. It can change after deposition. For instance, when dielectric films absorb water they swell. This swelling is constrained by the silicon substrate, thus, the wafer bends.



Figure I.8: Residual stress after deposition

The bending radius of curvature was monitored on a Frontier Semiconductor Measurements tool (128L C2C). The measurement principle is described in Fig. I.9. A laser is projected on the wafer and its reflection is analyzed by a photo-detector. The laser sweeps a diameter of the wafer thanks to the displacement of the stage. It gives the bow that is related to the bending radius of curvature R and wafer diameter D with:



Figure I.9: Measurement principle of bending radius of curvature

First, the warpage of the silicon substrate alone R_0 is measured. Then, measurements are performed after dielectric layer deposition, during storage and at the end of it. Stress $\sigma(t)$ and bending radius of curvature R(t) are related with the Stoney equation [16]:

$$\sigma(t) = \frac{E_S}{6(1-\nu_S)} \frac{h_S^2}{h} \left(\frac{1}{R(t)} - \frac{1}{R_0}\right) \quad (I.10)$$

 R_0 is the bending radius of curvature before dielectric deposition, E_S , v_S and h_S are the Young's modulus, the Poisson's ratio and the thickness of the silicon wafer.

The Stoney formula requires to fulfill the following hypothesis [17]:

- Thickness of the substrate and the coating are smaller than the lateral dimensions
- Thickness of the coating is smaller than thickness of the substrate
- Deformations and rotations are infinitesimal
- Substrate and coating are both homogenous, isotropic and linear elastic

The first two points are valid due to the dimensions involved in layers deposition on 300 mm wafer. The deformations measured are in the micrometer range, which validates the third point. The coating layer is amorphous; hence, the isotropic assumption is correct. It is homogenous thanks to the deposition method and linear elastic. These three characteristics are also true for the substrate. We measured the bending radius of curvature on four axes for several wafers to confirm the spherical deformation. The convention for tensile and compressive stress is given in Fig. I.8.

I.3.3. Infrared spectroscopy

Fourier transform infrared spectrometer (QS3300 from Nanometrics) was used to obtain transmission spectra in the range of 400 to 4000 cm⁻¹ with a resolution of 6 cm⁻¹. The analysis was carried out in normal incidence transmission mode. Each spectrum was converted in absorbance baseline, then baseline was corrected as shown in Fig. I.10. Finally, the spectrum was normalized with respect to the layer thickness.





When comparing several spectra of the same layer (post deposition and post humid storage for instance), the same baseline points were used.

I.3.4. Spectroscopic Ellipsometry

Spectroscopic ellipsometry was performed to measure the thickness of the layers. This optical technique analyzes the change in polarized light upon light reflection on samples [18]. Then, an optical model, which requires the optical constant of the material, is built in order to determine the thickness of the layer.

Our measurements were performed on a KLA Tencor ellipsometric tool at a wavelength of 633 nm. For each wafer, 17 points distributed homogeneously were measured.

I.3.5. Time of Flight – Secondary Ion Mass Spectrometry (Tof-SIMS)

One of the techniques adapted to study moisture diffusion is secondary ion mass spectrometry. One of the reasons is its sensitivity and ability to detect hydrogen compared to other techniques. It has been used in order to detect moisture for years [19]. It allows to get a better understanding of the diffusion paths [20], determine diffusion coefficients [5], [21] or to compare hermiticity of different layers [22]. The principle is to sputter the sample with an ion beam (primary ions) in order to release and ionize species from the sample (secondary ions). These secondary ions are then detected and their mass is determined thanks to their time of flight from to sample to the detector. The result is the number of counts of the elements present in the analyzed sample (atom concentration can be obtained with proper calibration). It is important to underline that prior to the analysis, a vacuum is created and samples are stored overnight. In Chapter IV, we investigate the potential moisture desorption induced by vacuum.

All plots hereafter were left with the original units; counts of the mass of interest are plotted against sputtering time. The sputter profile area was $100 \times 100 \ \mu m^2$ in our analysis.

I.3.6. Storage tools

• Climatic chambers

Throughout this work, we performed environmental storages. Most of them were conducted below 100° C and the climatic chamber presented in Fig. I.11 was used. It covers temperature/relative humidity couples from (10° C/10% RH) to (95° C/98% RH).

But it only works at atmospheric pressure. Hence, we used a different tool for the experiments above 100°C with a high humidity level described in Chapter V. This second equipment is pressurized, which allowed us to perform the standard Highly Accelerated Stress Tests (HAST): 96 hours at 130°C and 85% RH.



Figure I.11: Climatic chamber used for most storages

• Oven

In order to study moisture removal, the oven displayed in Fig. I.12 was used. It covers temperatures from 25° C to 400° C, under N₂ atmosphere.



Figure I.12: Oven used for annealing experiments

I.4. Comparison of three techniques to determine diffusion coefficient

In previous sections, we introduced the techniques and equations necessary to determine the diffusion parameters of dielectric layers. However, we cannot monitor each wafer with all techniques during environmental storages due to the important number of wafers to handle. We need to select the most sensitive and practical technique to determine diffusion parameters.

Hence, before collecting diffusion parameters for the six dielectrics previously described at various environmental conditions, we compared three techniques – mass, bending radius of curvature and infrared measurements. The first objective is to confirm that all these methods lead to similar diffusion coefficient and then to select the most convenient technique to monitor an important number of wafers.

For this study, we selected an USG layer (dense PECVD SiO₂) stored at ambient conditions. We also applied the same methodology to a PECVD SiON, the results can be found in [23].

I.4.1. Procedure

One wafer was stored in clean room environment at 21°C and 40% relative humidity. The characterization tools are also located in the clean room to perform measurements in the same environmental conditions. The three techniques – gravimetric monitoring, bending radius of curvature measurements and infrared spectroscopy – were described in section I.3. They were applied first on the substrate alone (before deposition), then immediately after deposition to deduct as deposited material properties. Then, the layer was monitored over 800 hours.

The layer studied is an Undoped Silica Glass SiO₂:H (USG) deposited by PECVD. Its deposition parameters can be found in Table I.1. Table I.2 gives several as deposited material properties of USG layers.

	Thickness	Density	Intrinsic
	(nm)	(kg/m ³)	stress (MPa)
USG	600	2 110	80

Table I.2: Properties of as deposited USG

I.4.2. Results

Fig. I.13(a) shows the IR absorption spectra of USG immediately after deposition and after 800 hours in clean room. The spectra present the characteristic Si-O-Si absorption peaks: stretching mode at 1080 cm⁻¹ (v Si-O-Si), wagging mode at 800 cm⁻¹ (δ Si-O-Si) and rocking mode at 450 cm⁻¹ (β Si-O-Si) [24]. They exhibit N-H stretching mode at ~3375 cm⁻¹ (v N-H) due to the precursors. Nitrogen concentration is low and we assume it does not affect variations in the 2800-3800 cm⁻¹ range (i.e. v N-H at 3375 cm⁻¹ is constant over storage time).



Figure I.13: (a) Infrared spectra after deposition and after moisture saturation (> 800 hours) for USG (dense SiO₂). (b) focus on the 2800 to 3800 cm-1 range after deposition and after moisture saturation (> 800 hours)

After moisture saturation, the spectra evolve as shown in Fig. I.13 (b), which presents IR absorption spectra over 2800 cm^{-1} to 3800 cm^{-1} . This range corresponds to water related bonds.

The area homogeneously increases over the whole range. As our objective is to test a simple and straightforward method to determine the diffusion coefficient with infrared spectroscopy and compare it with gravimetric and intrinsic stress monitoring, we did not focus on performing a deconvolution and further investigations are required to determine the proportions of each water related bond.

Hence, the area under IR curves is integrated between 2800 cm⁻¹ and 3800 cm⁻¹ to include all type of OH species from water molecules to dissociated OH, after layer depositions and after different time intervals. Area values are then injected in Eq. (I.4).

Fig. I.14 illustrates mass uptake (a), stress variations (b) and water related infrared area variations (c) as a function of the square root of time for the USG film. The experimental data are fitted with Eq. (I.4) presented in section I.1.



Figure I.14: (a) mass uptake (b) stress variation and (c) IR area variations (corresponding to the 2800 cm⁻¹ to 3800 cm⁻¹ area) for USG layer.

The agreement between the data and the model is correct. The diffusion coefficients are extracted for each technique. Three values of diffusion coefficient are given depending on the measurement methods. Results are given in Table I.3.

Table I.3: Diffusion coefficients of moisture and saturated moisture concentrations obtained with mass, stress and infrared spectroscopy measurements at 21 °C and 40% RH.

		Mass	Stress	IR spectroscopy
USC	D (cm ² .s ⁻¹)	$2.8 imes 10^{-15}$	2.3×10^{15}	$3.6 imes 10^{-15}$
086	C _{sat} (mg.cm ⁻³)	17		

All three techniques yield to comparable values in the range $[2.3-3.6].10^{-15}$ cm².s⁻¹. The saturated moisture concentration is calculated from saturated mass uptake in Fig. I.14(a), which is injected in Eq. (I.8).

I.4.3. Discussion

I.4.3.1. Diffusion coefficients and saturated moisture concentration

The diffusion coefficient calculated with infrared spectroscopy is slightly higher than those deduced from the two other methods. This can be explained with the lower number of measurements and the higher number of steps required to process the data compared to the other methods (baseline correction, integration limits choice).

Table I.4 summarizes diffusion coefficients for similar materials found in literature. Although materials in the table are similar, they differ in their deposition parameters and storage conditions. It can explain the variation observed over the diffusion coefficient values. Nonetheless, the values found here are consistent with literature.

Material	Permeant	D (cm ² .s ⁻¹)	Env. conditions	Ref
SiO ₂ -silicone hybrid	H ₂ O	5.4×10^{-17}	38°C/90% RH	[5]
Sputtered silica	H ₂ O	$1.0 imes 10^{-13}$	25°C/100% RH	[4]
PECVD Silica	$D_2O, H_2^{18}O$	$(7\pm 2) \times 10^{-17}$	Room T°	[25]
CVD phosphosilicate glass	H ₂ O	10 ⁻¹⁴	23°C	[2]
PECVD SiO ₂ (400°C)	H ₂ O	$[2.3-2.8] \times 10^{-15}$	21°C/40% RH	This work

Table I.4: Diffusion coefficients of moisture for SiO₂ materials

Concerning saturated moisture concentration, few values at ambient are available in the literature concerning dielectric materials. Viswevaran found a normalized solubility between 2 $\times 10^{-2}$ and 3×10^{-2} g.cm⁻³.atm⁻¹ for SiO₂-silicone hybrid at ambient temperature and 100% RH (with an extrapolation from experiments at higher temperatures). It corresponds to a saturated moisture concentration between 6×10^{-1} mg.cm⁻³ and 9×10^{-1} mg.cm⁻³. More values are available for polymers. He and Fan measured a saturated moisture concentration around 4 mg.cm⁻³ at 30°C for a 70 µm bismaleimide-triazine (BT)/glass fiber laminated substrate core material [26]. Moylan found values in the range of 18 ± 7 mg.cm⁻³ to 111 ± 12 mg.cm⁻³ for four different polyimides at 22° C [27]. These values are either found for thick samples (>10µm) or with different techniques like SIMS [5]. However, our result of 17 mg.cm⁻³ is in the same range.

I.4.3.2. Method consideration

We investigated three methods to determine diffusion parameters at ambient conditions. A good agreement is found between them. Among them, the mass measurement method is the only one that provides both diffusion coefficient and saturated moisture concentration, which are key material properties to assess water diffusion. If water diffusion was only monitored regarding stress, it would lead to the diffusion coefficient and a stress variation. A calibration with a known mass uptake would be necessary to get the saturated moisture concentration.

In order to evaluate the limitation of the three methods, we monitored other common dielectric materials in the same conditions (SiO₂ and SiN type). All minimal variations are converted into mass gain to compare the three techniques. Table I.5 summarizes the results.

	Mass	Bending radius of curvature	IR
Measurement uncertainty	40 µg	0.5 µm	/
Minimal variation	> 0.25% in mass	$\label{eq:alpha} \begin{split} \Delta R &= 5 \ \mu m \\ \Delta \sigma &= 13 \ MPa \\ > 0.25\% \ in \ mass \end{split}$	> 0.8% in mass

Table I.5: Uncertainties and minimal variations to obtain diffusion parameters

We only start to observe variations with FTIR for mass uptake higher than 0.8%. Hence, infrared spectroscopy is the less sensitive techniques to determine diffusion coefficient. For mass and bending radius of curvature measurements, a similar sensitivity is observed but only gravimetric monitoring gives the saturated moisture concentration as mentioned above.

Measurement time is also three times lower for the mass, which will be important in order to minimize the time that wafers spend out of the climatic chamber in Chapter II.

I.4.3.3. Conclusions

We monitored a 600 nm USG film at ambient conditions (21 $^{\circ}$ C, 40% RH). At these conditions, we observed that moisture uptake is already significant.

The diffusion coefficient was determined with three different techniques: mass, bending radius of curvature and infrared spectroscopy measurements. An excellent agreement has been found between them. The diffusion coefficients are in the range of 2.3×10^{-15} to 3.6×10^{-15} cm² s⁻¹ for the USG (dense PECVD SiO₂) layer.

Only gravimetric monitoring gives both diffusion parameters. Moreover, it is the simplest and fastest technique. Hence, we select this method to monitor all materials at various environmental conditions in Chapter II.

I.5. Conclusions

In this chapter, we introduced the theoretical context and the measurement techniques used to study the diffusion behaviors of six dielectric materials. These layers cover the main dielectrics present in the BEOL. Their deposition parameters were extensively described.

We compared three simple techniques - mass, bending radius of curvature and infrared spectroscopy measurements - in order to confirm our choice of using gravimetric monitoring to determine diffusion parameters. We found an excellent agreement for the diffusion coefficient of a USG layer (dense SiO₂) in the range of 2.3×10^{-15} to 3.6×10^{-15} cm² s⁻¹. We also highlighted some limitations that confirm that gravimetric monitoring is the most suitable technique to determine the diffusion parameters of an important number of wafers. One of its main advantages is that it directly gives the saturated moisture concentration.

In the next chapter, we will study these six layers at different environmental conditions and we will investigate specific diffusion behaviors. Based on the present results, the diffusion parameters will be determined thanks to mass monitoring. Other analysis techniques, such as bending radius of curvature and infrared spectroscopy measurements, will only be used to complete our physical understanding of the phenomena.

Chapter II

Moisture diffusion in PECVD dielectric materials

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In this second chapter, we investigate the six dielectric materials presented in Chapter I at various environmental conditions. The main objective is to gather their diffusion parameters and explain their absorption behavior in order to explain moisture absorption in integrated stacks in the following chapters.

First, all layers are studied at 85°C/85% RH with the gravimetric monitoring presented in Chapter I. That allows us to determine their diffusion properties. Then, we use additional measurements – intrinsic stress and infrared spectroscopy – to determine their diffusion behavior.

In the second part of this chapter, we investigate the non-Fickian behavior observed for SiCN layers. In addition to the techniques mentioned above, Tof-SIMS analysis is performed to precisely monitor the presence of moisture in the layer.

Finally, we studied the influence of temperature and relative humidity on the diffusion parameters – diffusion coefficient and saturated moisture concentration – of a dense SiO_2 . The main conclusions and perspectives relative to this chapter are then presented.

II.1. Diffusion of moisture at 85°C/85% RH for common dielectric materials

In this section, the diffusion of moisture in dielectric materials at 85°C/85% RH is investigated. The two main objectives are to collect diffusion parameters (D and C_{sat}) and to explain the diffusion behaviors observed.

To do so, we use characterization tools and an environmental chamber. However, these tools are not located in the same building. It implies to transport wafers back and forth at ambient conditions. Hence, we started by investigating the effects of this practical issue to confirm the validity of our results.

II.1.1.Investigation of the time spent out of climatic chamber during mass measurement

The procedure to measure moisture diffusivity and water solubility in organic materials used in electronic devices is described in the JEDEC norm JESD22-A120A [28]. The first recommendation before starting environmental storage is:

1- "Bake the sample at 125°C for 24 hours."

The purpose of this step is to remove moisture from the samples and obtain dry samples before starting the desired experiment. Due to logistical limitations, we could not perform this step on each wafer. Ovens are not always available and their capacity was not enough, thus, we could not rely on this bake. Hence, we focused on reducing the time spent at ambient post deposition. Thus, one mass measurement was performed just after deposition to obtain the initial layer mass then the storage in environmental chamber was started. The delay between deposition and beginning of storage was around 45 minutes.

In order to evaluate the efficiency of a bake after the first hours of a storage at ambient conditions ($21^{\circ}C/40\%$ RH), we performed a short investigation with a bake at $100^{\circ}C$ for 16 hours.

We performed this bake on a dense PECVD SiO_2 and measured its mass before and after annealing as shown in Fig. II.1.



Figure II.1: Effect of a 100°C bake to remove moisture (USG layer)

Surprisingly, the mass measured after the 100°C bake was higher than the mass measured before the bake. In order to thermalize the wafer, 30 minutes elapsed between the end of the bake and the mass measurement. We attribute this higher mass uptake to moisture uptake during these 30 minutes.

It clearly shows that this 100°C bake is inefficient at removing moisture for this dense SiO_2 with the logistical limitations that we have. In the second section of this chapter we also give some results on the impossibility to remove moisture at 125°C in SiCN layers. Thus, our choice of lessening the time spent at ambient post deposition is relevant.

During the environmental storage, the JEDEC norm [28] recommends:

2- Once the storage is started, it is recommended to remove the sample and place it in contact with a heat sink. Then, mass measurement should be performed within five minutes.

This recommendation implies the proximity between environmental chamber and microbalance. In our case, this is not possible because the tools are not located in the same building. A wafer typically spends around thirty minutes out of the environmental chamber to perform one mass measurement. This duration includes the transportation time to and from the microbalance plus the measurement time.

Hence, the impact of this time spent at ambient needs to be assessed. To do so, we selected one material known to have significant moisture uptake: the USG (dense SiO₂). The environmental conditions selected is 85°C/85% RH. Two groups of samples were designed as follows:

- **Group 1**: Two wafers removed from the environmental chamber and measured periodically. It corresponds to the procedure followed in our work. In total, these wafers spend a few hours at ambient conditions for transportation and measurements.
- **Group 2**: Six wafers removed from the chamber only once after a specific storage duration. Thus, they only spend around 30 minutes maximum at ambient conditions. For instance, the wafer measured after 24 hours at 85°C/85% RH from group 1 was already measured three times before (= around one hour and a half at ambient) when the corresponding wafer from group 2 has not seen ambient conditions yet.



The procedure is summarized in Fig. II.2:



Fig. II.3 shows the gravimetric monitoring as a function of square root of time for wafers from groups 1 and 2. The comparison was stopped after about 130 hours of storage at 85°C/85% RH (the time spent at ambient becomes negligible compared to storage duration).



Figure II.3: Gravimetric monitoring obtained for groups 1 & 2

There is no difference between the two groups. And the mass uptake increases linearly. This indicates that the time spent at ambient to perform the mass measurement has no impact on the measurement itself.

Based on the results above we confirmed that the delay necessary to transport and measure wafers does not impact the measure. We also showed that the first hours post deposition are crucial since moisture uptake is fast and not reversible with low temperature bake. Hence, for all experiments we focused on lessening this time to a maximum of 45 minutes and for each storage we monitored three wafers for repeatability purpose.

II.1.2.Diffusion parameters for common dielectrics at 85°/85% RH

In this section the diffusion behaviors of the dielectric materials presented in chapter I are presented. Then, their diffusion parameters are calculated. All parameters were determined with gravimetric monitoring as presented in Chapter I.

All materials were monitored at 85°C/85% RH until the saturation was observed. The saturation was not reached only for the two SiCN even after 10 000 hours of storage.

II.1.2.1. Diffusion behaviors observations

Fig. II.4 presents the gravimetric monitoring for a 200 nm USG (a) and a 150 nm SiCN 335 (b).



Figure II.4: Gravimetric monitoring at 85°C/85% RH for USG (a) and SiCN 335 (b)

The Fickian model used here is described in Chapter I. The corresponding curves in Fig. II.4(a) and (b) were obtained with the least square method described in Chapter I. For USG, the diffusion is Fickian. However, it is not possible to fit the SiCN experimental data with this model. Two slopes can clearly be identified. Moreover, the saturation is still not reached after 9 300 hours of storage at 85°C/85% RH. This very long time to reach saturation is known for polymers, it has been documented for polymers resins by several research groups [29], [30].

It has been shown by several authors that Fickian and non-Fickian diffusion can happen simultaneously during the absorption process for polymers. For composite materials, a Langmuir-type model was proposed by Carter [31]. Another model that assumes the existence of moisture under two phases was proposed by Gurtin [32]. However, these models involve parameters that are complex to determine and they are not easily usable for numerical simulations. A simpler model was described by Placette. He showed that it was possible to model the non-Fickian model as a Fickian one for epoxy mold compounds [33].

To fit the experimental data obtained for SiCN 335, we used the dual stage model he proposed. It is mathematically described as follow in Eq. (II.1):

$$N(t) = N_{1,\infty} \left[1 - \sum_{k=0}^{\infty} \frac{8}{(2k+1)^2 * \pi^2} e^{-\frac{D_1(2k+1)^2 \pi^2 t}{4h^2}} \right] + N_{2,\infty} \left[1 - \sum_{k=0}^{\infty} \frac{8}{(2k+1)^2 * \pi^2} e^{-\frac{D_2(2k+1)^2 \pi^2 t}{4h^2}} \right]$$
(II.1)

With:

 $N_{\infty} = N_{1,\infty} + N_{2,\infty} \quad (II.2)$

Where N_{∞} is the total number of water molecule after infinite time. Under assumption that both these mechanisms affect mass uptake, we propose the following equation:

$$M(t) = M_{1,\infty} \left[1 - \sum_{k=0}^{\infty} \frac{8}{(2k+1)^2 * \pi^2} e^{-\frac{D_1(2k+1)^2 \pi^2 t}{4h^2}} \right] + M_{2,\infty} \left[1 - \sum_{k=0}^{\infty} \frac{8}{(2k+1)^2 * \pi^2} e^{-\frac{D_2(2k+1)^2 \pi^2 t}{4h^2}} \right]$$
(II.3)

Where M(t) is the mass uptake and:

$$M_{\infty} = M_{1,\infty} + M_{2,\infty} \quad (II.4)$$

Where M_{∞} stands for the total mass uptake.

This model does not describe the physical and chemical phenomenon behind the non Fickian absorption observed. These parameters are empirical parameters that helps to describe the absorption of moisture in SiCN accurately. Due to the mathematical simplicity, they can easily be implemented into finite elements modeling software. This will be done in Chapter IV with COMSOL. The physical explanations behind the non-Fickian behavior of SiCN are explored in the second section.

Table II.1 summarizes the different diffusion behaviors observed for the present study. The mass uptake for each material is presented below in Fig. II.5 and in Fig. II.6.

Table II.1: Diffusion behaviors for the dielectric materials studied

Fick	Dual Stage
 USG (dense SiO2:H) TEOS (dense SiO2:H) ULK (porous SiOC:H) 	 SiCN 335 SiCN 350 Low k (SiOC :H)

II.1.2.2. List of the diffusion parameters

In order to link observations at material level to behaviors observed in full stacks, several diffusion parameters are required for each material. As described in the previous chapter, the diffusion coefficients and the saturation values describe moisture absorption for each material. We start with the materials that have a Fickian absorption.

All the parameters are given for the following conditions: 85°C/85% RH. Table II.2 gathers all diffusion parameters for the dielectrics fitted with the Fickian model.

Material	D (cm ² /s)	C _{sat} (mg/mm ³)
USG	$3.4 (\pm 0.5) \times 10^{-15}$	132.4 ± 6.3
TEOS	$2.8 (\pm 0.1) \times 10^{-15}$	58.1 ± 0.2
ULK	$2.6 (\pm 0.0) \times 10^{-15}$	109.8 ± 1.3

Table II.2: Diffusion parameters for Fickian behaviors at 85°C/85% RH

It is important to underline that the values for ULK represent the bulk of the material. This material is known to be impacted by integration steps. It partly becomes hydrophilic due to plasma effects [34]. Moreover, in integrated stacks, ULK is deposited on top of SiCN 350. A thin layer without carbon is first created to improve adhesion between SiCN 350 and ULK (bulk). These modified areas were not studied here.

In order to have the results for the three materials (USG, TEOS, ULK) in the same figure (Fig. II.5), the data were normalized with respect to their thickness. The mass uptake is represented relatively to layers initial mass.



Figure II.5: Mass uptake at 85°C/85% RH for ULK, TEOS and USG. All experimental data are fitted with the parameters of the Fickian model presented in Table II.2

The diffusion parameters for layers fitted with the dual stage model are collected in Table II.3.

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Material	D ₁ (cm ² /s)	D ₂ (cm ² / s)	C _{sat,1} (mg/mm ³)	Csat,2 (mg/mm ³)
Low k	$8.4 (\pm 1.6) \times 10^{-14}$	$9.8 (\pm 2.6) \times 10^{-16}$	17.1 ± 2.0	11.6 ± 1.4
SiCN 335	$7.1 (\pm 1.6) \times 10^{-15}$	$1.1 (\pm 0.1) \times 10^{-18}$	71.0 ± 10.1	558.1 ± 32.3
SiCN 350	5.2×10^{-14}	$4.7 imes 10^{-18}$	17.9	58.1

Table II.3: Diffusion parameters for Dual stage behaviors at 85°C/85% RH

The values for both SiCN are the empirical values that can described moisture absorption up to the duration performed (6 500 hours for SiCN 350 and 9 300 hours for SiCN 335). Since the saturation was not reached, these parameters are not the intrinsic diffusion parameters of these layers and longer storages are required to determine them. However, they can accurately describe the diffusion process up to the duration that are higher than usual standards.

The experimental data for the three materials of Table II.3 are represented in Fig. II.6 with their dual stage model.



Figure II.6: Mass uptake at 85°C/85% RH for low-k and SiCN layers. All experimental data are fitted with the parameters of the dual stage model presented in Table II.3

The storage of the low-k layer had to be stopped after 400 hours for logistical purposes. Thus, additional points after a longer storage are required to fully confirm the non-Fickian behavior that is less apparent compared to SiCN layers.

In order to confirm our results, the diffusion parameters from the literature for dielectric materials are collected in Table II.4. In all studies these dielectrics are considered as Fickian. The studies are mainly conducted at room temperature. No values were found for SiCN materials.

Most of our values are consistent with the values from literature. As one can see, the diffusion coefficient for low-k and ULK materials varies greatly. Several values are many orders of

magnitude higher than our values. The studies from Li [35] and Lin [36] both underline the role of the interface between OSG (similar to ULK) and SiCN or silicon substrate. It could explain the higher order of magnitude of the moisture diffusion coefficient compared to our results. We will investigate this problematic in depth in Chapter IV.

Material	Solute	$D (cm^2/s)$	Env. conditions	Ref
SiO ₂ -silicone hybrid	H ₂ O	5.4×10^{-17}	38°C/90% RH	[5]
Sputtered silica	H ₂ O	1.0×10^{-13}	25°C/100% RH	[4]
PECVD Silica	D2O, H218O	$(7\pm 2) \times 10^{-17}$	Room T°	[25]
CVD phosphosilicate glass	H2O	10 ⁻¹⁴	Room T°	[2]
Low-k (10% nanoporous methyl silsesquioxane MSSQ)	Toluene	$3.1 imes 10^{-10}$	23°C	[37]
Low-k (spin-on p-MSQ)	H2O	$7.0 imes 10^{-15}$	25°C	[38]
Low-k (hydrogen silsesquioxane HSQ)	H2O	3.61×10^{-14}	25°C	[39]
Organosilicate glass (OSG)/SiCN interface	H2O	$9.8 imes 10^{-7}$	22-23°C/immersed in distilled water	[35]
Low-k SiOCH	H2O	$1.1 imes 10^{-7}$	25°C	F 4 0 1
ULK	H2O	$4.5 imes10^{-6}$	25°C	[40]
Plasma Nitride	H2O	< 10 ⁻¹⁷	Room T°	[2]

Table II.4: Diffusion parameters for common dielectric materials

The values determined is this subsection will be used in numerical simulation in Chapter IV in order to describe moisture diffusion in integrated stacks. One of the findings is the non-Fickian behavior SiCN and low-k materials. In the second section of this chapter, we investigated the reasons of this behavior for SiCN.

In the next subsection, the influence of moisture diffusion on some physical properties and the types of bonds formed between dielectric materials and moisture is discussed. We focus on dense SiO_2 and porous SiOC.

II.1.3. Moisture influence on physical and chemical properties

Some mechanical and chemical properties of dielectric materials are also influenced by humidity. Depending on the material itself, we observed different behaviors. In this subsection, we mainly focus on dense PECVD SiO_2 and SiOC:H layers. The SiCN layers will be investigated in the second section of this chapter.

The influence of moisture on their thickness, intrinsic stress and chemical bonds is presented.

II.1.3.1. Thickness variations

Thickness is a key factor in the calculations of the diffusion coefficients and intrinsic stress. Hence, any thickness variation observed during storage may influence these parameters. For dielectric materials, several research groups assumed a constant thickness during moisture absorption. McInerney calculated diffusion coefficients for several dielectric materials based on bending radius of curvature measurements but the potential thickness variation is not considered [2]. Similarly, Visweswaran determined the diffusion coefficient of a PECVD SiO₂ with capacitance and intrinsic stress measurements. The thickness of the layer is assumed constant [5]. However, the variations of thickness due to moisture are well known for other types of materials such as polymers [41], [42].

Hence, we investigated the thickness variations for the two dense SiO_2 layers (TEOS and USG) with ellipsometry in order to discuss the assumption of a constant thickness for dielectric layers. The thickness was measured post deposition and after a 85°C/85% RH storage. The duration of storage was long enough to reach moisture saturation for both layers (based on mass monitoring).

Table II.5 presents the thickness measured at each step.

	Initial thickness (nm)	Post 85/85 thickness (nm)	Relative variation
USG	198.9 ± 1.2	211.7 ± 1.2	6.4 %
TEOS	254.1 ± 1.9	257.9 ± 2.0	1.5%

Table II.5: Thickness variation for USG and TEOS at 85°C/85% RH

These two materials have similar bulk composition and their thickness variations are consistent with the mass saturation values displayed in Fig. II.4. The higher moisture content in USG causes a higher thickness increase compared to TEOS.

We investigated the impact of these variations on diffusion parameters and intrinsic stress for USG, which shows the highest variations. For intrinsic stress, the calculation is straightforward, we just replaced the layer thickness in the Stoney equation. For the diffusion parameters, the

thickness should be a function that depends on time in Eq. I.4. We simplified the calculation and considered constant thicknesses before and after storage i.e. either 199 nm or 212 nm.

	h = 199 nm	h = 212 nm
D (cm ² /s)	4.1×10^{-15}	$4.5\times10^{\text{-}15}$
C _{sat} (mg/cm ³)	130.1	123.6
σsaturation (MPa)	- 167.0	- 157.6

Table II.6: Impact of thickness variation on diffusion parameters and intrinsic stress

The variation for the diffusion coefficient and the saturated moisture concentration are equal to the standard deviations presented in Table II.2. For the intrinsic stress, the higher thickness induces a value 5% lower. Intrinsic stress variations for other layers are presented below in Table II.7. A 5% variation is negligible. Thus, even with a 13 nm increase, the diffusion parameters and intrinsic stress are only slightly modified. It validates the results obtained previously when considering a constant thickness.

We did not investigate the explanation of this thickness increase. It would be necessary to confirm the values measured with ellipsometry. This technique relies on models that use the reflective index. However, it can be impacted by moisture and this was not investigated here. A different experimental setup that involves a mechanical technique such as atomic force microscope (AFM) could help to solve this question.

II.1.3.2. Intrinsic stress

Table II.7 shows the influence of the 85°C/85% RH storage on intrinsic stress values for the dielectrics studied. Except for SiCN layers, moisture saturation was reached. For each layer, we assumed a constant thickness.

	G Reference (MPa)	σ85°C/85% (MPa)	Variation (MPa)
UGS	- 60.4	- 167.0	- 106.6
TEOS	- 160.0	- 407.3	- 247.3
Low-k	+ 46.8	+ 38.6	- 8.2
ULK	+ 70.9	+ 63.3	- 7.6
SiCN 335	- 272.6	- 1161.7	- 889.1
SiCN 350	- 327.0	- 484.0	- 157.0

Table II.7: Intrinsic stress variations due to 85°C/85% RH storage

Both SiOC:H materials (ULK and low-k) display a different behavior from other dielectrics. For these two layers, especially ULK that has significant moisture absorption, the mass uptake does not translate into a significant stress variation compared to other dielectrics.

In the next parts, we only focus on USG and ULK layers as they both have a significant mass uptake but completely different variations of their intrinsic stress. Our objective is to explain their behaviors with additional characterizations. First, with a focus on the chemical bonds formed with moisture with infrared spectroscopy. Then, by investigating the reversibility of the phenomenon with a 125°C baking.

II.1.3.3. Chemical bonds

We used infrared spectroscopy to study the impact of moisture on chemical bonds. We focus on the difference highlighted with stress measurements between SiO_2 and SiOC:H layers. To understand this difference, we first performed infrared spectroscopy on USG and ULK layers.

First, we consider USG. Fig. II.7 displays the infrared spectra before and after 85°C/85% RH storage for USG (a) with a focus on the H_2O related range (b).



Figure II.7: Infrared spectra of USG (reference and post 85°C/85% RH). A focus on the 2800-3000 cm^{-1} range related to H₂O bonds is presented (b)

Two significant variations are visible. In the 2800-3800 cm⁻¹ range, the area homogeneously increases over the entire range. This is explained with the numerous polar -OH groups present initially in these layers after PECVD. They can easily form hydrogen bonds with absorbed moisture, which explain the increase of bounded and free H_2O bonds.

The second area is below 1200 cm⁻¹ where the Si-O-Si bonds are located. These layers have dangling bonds (referring to internal STMicroelectronics reports and shown for hydrogenated polymorphous silicon by Takeda [43]). Hence, moisture can be easily absorbed in these sites. We assume the following reaction between dangling bonds and moisture to explain the increase of the Si-O-Si peaks:

$$2Si \cdot +H_2 0 \rightarrow Si - 0 - Si + H_2$$

Where Si represents a silicon atom with a dangling bond.

Secondly, we consider ULK and Fig. II.8 shows the infrared spectra before and after $85^{\circ}C/85\%$ RH storage for ULK (a) with a focus on the H₂O related range (b).



Figure II.8: Infrared spectra of ULK (reference and post $85^{\circ}C/85\%$ RH). A focus on the 2800-3000 cm⁻¹ range related to H₂O bonds is presented (b)

No sign of moisture related bonds is detected for this material. This is surprising since its mass uptake is significant (+ 9%). We propose an explanation based on the nanostructure of the layer.

As previously mentioned, the layer has not undergone any integration step. The bulk structure of ULK with UV cure was presented in Chapter I, it is reminded in Fig. II.9. Methyl groups are still present at the surface of the material, and nanopores can be found in the volume of the layer. ULK films can also contain few polar bonds (silanols). Imbert showed that it takes very long UV curing times to remove all the carbon in the SiOC:H layers [44]. With this information and with the process conditions described in Chapter I, the ULK structure studied can be described as the one presented in Fig. II.9; the layer is hydrophobic.



Figure II.9: Bulk structure of ULK. Reproduced from Gourhant [12]

We assume that all the absorbed moisture is in the nanopores of ULK and that it almost does not bond to the bulk of the layer due to its hydrophobicity. To have a first idea of the validity of this assumption we calculate the mass of water molecules absorbed if 100% of the nanopores are filled.

The porosity of ULK is around 17% (internal STMicroelectronics characterization). We obtain the mass of absorbed moisture $M_{moisture}$ with:

$$M_{moisture} = V_{pores} \times M_{vol,H20}$$
 (II. 5)

Where V_{pores} is the volume occupied by the nanopores and $M_{\text{vol, H2O}}$ is the density of water.

It leads to $M_{\text{moisture}} = 3\,850\,\mu\text{g}$. This value is consistent with the value measured experimentally (2 500 μ g). The difference can be explained with the simplicity of the assumptions made. We assumed that 100% of the pores are filled. However, some nanopores are not accessible and we did not consider the steric effects between water molecules. We also did not consider potential impact of remaining polar -OH groups on moisture absorption.

The complete absence of moisture related bonds in the infrared spectrum is not explained and requires more investigation. Multiple internal reflection (MIR) technique that is more adapted to observe low concentration bonds could help to understand this result.

II.1.3.4. Moisture removal at 125°C

To confirm our hypothesis on the type of bonds for USG and ULK layers, we performed baking at 125°C with mass monitoring and infrared spectroscopy. We chose this temperature because it can remove the weakly bonded moisture (α bonds) without removing more tightly bonded moisture (β bonds).

One wafer of USG and one of ULK were saturated at 85°C/85% RH and then placed in an oven at 125° C (N₂ atmosphere in the oven). They were periodically removed to monitor their mass and the impact on chemical bonds with infrared spectroscopy. It is described in Fig. II.10:



Figure II.10: Investigation of moisture removal in USG and ULK after 85°C/85% RH storage

Fig. II.11 shows the mass monitoring of USG and ULK during the 125°C baking post environmental storage at 85°C/85% RH. Thus, the initial values (~ 9% for ULK and ~ 6.5% for USG) correspond to the saturation obtained at 85°C/85% RH.



Figure II.11: Mass monitoring for USG (a) and ULK (b) during 125°C baking

For ULK, almost all the moisture is removed at 125°C (Fig. II.11(a)) in less than 400 hours. This corroborates the assumption of moisture mainly located in nanopores. Due to the absence of bonds with the bulk of the layer, it can easily be removed with low temperature annealing.

For USG, half of the absorbed moisture remains after 1600 hours at 125°C. As it can be seen from Fig. II.11(b), the desorption seems to still be ongoing. Two slopes can be observed, fast desorption for the first hours followed by a slower mechanism. We did not investigate the physical explanation of this behavior. Nonetheless, it shows that at least 50% of the absorbed moisture consist of weak bonds for USG layers.

As previously indicated, infrared spectroscopy was also performed, and there is again no variation for ULK layer. Hence, only USG spectra are presented hereafter. Fig. II.12 shows the infrared spectra for the USG wafer at different steps of the experiment. The spectrum post 125°C corresponds to the measurement performed after 1600 hours of baking.

Fig. II.12(c) corroborates the observations obtained with the mass monitoring. The spectrum post 125°C differs from the post 85/85 spectra in the 2800-3400 cm⁻¹ range. It corresponds to weakly bonded water and free molecular water that was removed during baking. Above 3400 cm⁻¹, the strongly bonded moisture is unaffected and higher baking temperatures are required.

An important quantity of moisture is still present after the 125°C baking as it can be seen from the difference with the reference spectrum. This is consistent with the significant amount of moisture remaining that was observed with mass measurements in Fig. II.11(b).



Figure II.12: Infrared spectra for USG (reference, post 85°C/85%RH and post 125°C baking). Inserts focus on the Si-O-SI peak (b) and H₂O related bonds (c)

II.1.3.5. Summary

We summarize the results that have been evidenced regarding the mechanisms of moisture absorption in USG and ULK layers and their effects on physical and chemical properties below.

• USG (dense SiO₂:H)

Due to the PECVD technique, USG layers have dangling bonds and polar groups after deposition. Water, as a polar molecule, can easily form hydrogen bonds with other polar groups, such as -OH. The dangling bonds also offer preferential sites for moisture to bond with. These different types of bonds were confirmed with the infrared spectra and the annealing experiments.

These bonds modify the nanostructure of USG. They cause volume increase locally. Because of the silicon substrate, the swelling of USG is constrained. Hence, it results in the bending of wafer and the built-up of a compressive stress.

• ULK (porous SiOC:H)

For ULK layers, most of the moisture is absorbed in the free volume offered by the nanopores. Due to the presence of methyl groups, the surface of ULK and its pores is hydrophobic. Hence, moisture does not bond to the bulk of the layer. Contrary to USG layers, in ULK layers there is almost no modification of the bulk of the layer, thus, no increase in the volume. It explains why there is no stress built-up even with a significant amount of absorbed moisture. After investigating moisture diffusion in Fickian layers (USG and ULK), we will study the interactions between moisture and SiCN materials that display a non Fickian behavior in the next section.

II.2. Non-Fickian behavior of SiCN

In this section, the non-Fickian behavior observed for SiCN is investigated. This behavior is observed for both versions of the SiCN (deposited at 335°C and 350°C). SiCN 335 is selected here because all the variations linked to moisture uptake are more important. The mass monitoring fitted with Fick or Dual stage model is presented in Fig. II.13.



Figure II.13: Non Fickian behavior observed for SiCN 335 fitted with Fickian (a) or dual stage model (b)

The storage presented is close to 9500 hours and yet the saturation is still not reached. As already mentioned in section II.1, the Fickian model is clearly not appropriate. It is possible to fit the experimental data with a dual stage model; however, it does not give any understanding of the physical and chemical phenomenon behind this behavior.

The objective of this section II.2 is to explain how moisture sorption occurs for such material. To do so, Tof-SIMS analyses coupled with infrared spectroscopy were performed. Three silicon substrates with a SiCN of 150 nm were used to perform the following experiments:

- Wafer 1: cut into samples of 2×3 cm² and stored at 85°C/85% RH for different durations up to 2 300 hours. A Tof-SIMS analysis was then performed to investigate oxygen profiles
- Wafer 2: stored at 85°C/85% RH up to 9 500 hours and periodically removed to measure mass and perform infrared spectroscopy
- Wafer 3: Stored 2 hours at 85°C/85% RH then annealed at 125°C for 40 hours to study moisture removal in the first hours corresponding to the first slope in Fig. II.13.

The procedure is summarized in Fig. II.14.



Figure II.14: Procedure to study moisture absorption of SiCN 335 layers

For Tof-SIMS, we cannot perform one analysis each time a sample is removed from the environmental storage as it would be too costly. Thus, we removed all samples simultaneously, so they are all analyzed together in Tof-SIMS as is it displayed in Fig. II.14. To reduce moisture uptake prior to the environmental storage, samples were stored under N_2 environment.

II.2.1.Observation of moisture absorption in SiCN layers

Fig. II.15 gives the oxygen profiles for the sample stored 2 300 hours at ambient conditions and the one stored 2 300 hours under N_2 atmosphere.





The oxygen concentration does not vary and is very low with the N₂ storage. On the contrary, the amount of oxygen significantly increases for the sample stored at ambient laboratory conditions. This confirms the efficiency of the procedure chosen; for the samples stored under N₂ environment then at 85°C/85% RH, any increase in the oxygen profile is then caused by the 85/85 storage.

The oxygen peak between the silicon substrate and the SiCN layer is present in all samples, even in the reference stored only under N_2 . It corresponds to the native oxidized surface on substrate that is only a few nanometers thick and does not vary over time.



Fig. II.16 shows all oxygen profiles for storages up to 2 300 hours at 85°C/85% RH.

Figure II.16: Tof-SIMS oxygen profiles for samples stored up to 2 300 hours at 85°C:85% RH

The oxygen concentration increases with increasing storage time. A concentration gradient is present in the thickness of the SiCN layers. This confirms a diffusion from the top side of the samples. Moreover, it shows that the samples are not saturated after 2 300 hours because the oxygen concentration is not yet uniform over the entire thickness, which is consistent with the mass uptake measurements presented in Fig. II.13.

In order to link these results to the mass observations, we integrated the area under the curves over the entire [0; 250] nm range for all oxygen profiles. Fig. II.17 represents the integrated areas as a function of the mass uptake. The durations in the figure represent the duration of the storage at $85^{\circ}C/85\%$ RH.



Figure II.17: Area integrated from oxygen Tof-SIMS profiles as a function of mass uptake for SiCN 335

A linear relationship is observed between the concentration of oxygen in the layer and the mass uptake. Hence, the dual stage behavior observed for mass uptake is also valid for the concentration of oxygen in the layer.

To understand the type of bonds in the first hours of storage, we performed two hours of storage at 85/85 immediately followed by an annealing at 125° as described in Fig. II.14 (Wafer 3). Once in an oven at 125°C, the wafer was removed periodically to measure its mass. Twenty minutes were necessary to thermalize the wafer around 20°C. Because the mass measurement is performed under control environment, any variation of the wafer temperature impacts the mass measurements (the point measured around 50 hours is an example of this effect). The mass monitoring during 125°C annealing is presented in Fig. II.18, the first point was measured just before the beginning of the annealing.



Figure II.18: Mass of absorbed moisture during the 125°C annealing for SiCN 335

The mass of the sample is not lower after 130 hours at 125°C. Hence, no moisture is removed at this temperature. We showed for ULK that most of its absorbed moisture can be removed at

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125°C because it is composed of weak bonds. This annealing shows that there are no weak bonds between SiCN and moisture even in the first hours of storage.

This result also corroborates our approach described in section II.1.1 relative to the JEDEC bake. If no moisture is removed after only two hours at 85°C/85% RH, then it is plausible that moisture would not be removed at ambient conditions neither.

From the beginning of the 85/85 storage, the moisture chemically bonds with SiCN layers. Hence, the oxygen concentration increase observed in Tof-SIMS and with mass measurements corresponds to chemically absorbed moisture.

II.2.2. Chemical bonds and reactions occurring during moisture absorption

We showed that this SiCN has a strong and not reversible moisture uptake at 85°C/85% RH but the previous analyses do not inform on the chemical bonds and the reactions occurring during moisture uptake.

Hence, we performed infrared spectroscopy in order to answer these questions. The infrared spectra presented in Fig. II.19 concern a reference SiCN layer just after deposition and one layer stored 9 300 hours at 85°C/85% RH. All the reference for the position of infrared peaks can be found in the Chapter 5 of the Handbook of Infrared Spectroscopy from Tolstoy [24]. A thorough analysis of SiCN in FTIR by Peter [45] is also used.



Figure II.19: Infrared spectra of a SiCN 335 post deposition (plain black line) and a SiCN 335 stored 9300 hours at 85°C/85% RH (orange dashed line)

Both layers have characteristic peaks of SiCN layers. They present peaks related to CH_x in the 2860-2980 cm⁻¹ range and Si-CH₃ peaks at 1250 cm⁻¹ (stretching mode). These two peaks are the only ones that are not impacted by the storage. The two negative peaks between 2300 and

 2400 cm^{-1} are typical of CO₂ present in the infrared analysis chamber, they are not related to the materials studied. All other peaks are impacted by moisture absorption.

We underlined three areas in Fig. II.19 that are discussed below: $2800 - 3800 \text{ cm}^{-1}$ (area 1), 2120 cm⁻¹ (area 2) and below 1300 cm⁻¹ (area 3).

The spectrum evolves significantly in the 2800 cm⁻¹ – 3800 cm⁻¹ range (area 1). It corresponds to the broad range related to moisture bonds (free molecular water between 3000 and 3300 cm⁻¹ and bonded H₂O from 3300 to 3600 cm⁻¹). The peak around 3700 cm⁻¹ is related to isolated Si-OH (silanols). There is also the stretching mode of N-H at 3380 cm⁻¹ but the main variations are due to moisture as shown in the previous subsection. In the case of SiCN, the increase mainly concerns the 3200-3600 cm⁻¹ range, hence the bounded Si-OH and free H₂O; the silanols show little variation.

Both layers exhibit the Si-H initially at 2120 cm⁻¹ and shifted at 2140 cm⁻¹ after 9300 hours of storage (area 2). The wavenumber shift is due to local atomic rearrangements. A sharp decrease in the intensity of the peak is also observed. This is discussed below.

In the range below 1300 cm⁻¹ several bonds exist (area 3), and a deconvolution is necessary to study this area. We used the software Fityk[©] to do so. We adopted the following methodology to perform the deconvolution:

- We listed the bonds present in that range for SiCN layers from the literature.
- We only used Gaussian function that assumes symmetrical peaks. For each peak three parameters have to be adjusted: center, intensity (height of the peak) and width. We placed each peak at their theoretical center for the reference SiCN spectrum.
- Then, each parameter was determined iteratively until a good fit was obtained.
- We reported the same peaks on the spectrum of the SiCN stored 9300 hours. First, the height and the width of the peaks were iteratively adjusted. Then, to improve the fitting we allowed the centers to be adjusted. The Si-CH₃ peak at 1250 cm⁻¹ was used as a reference.

Fig. II.20 represents the deconvolution for the reference spectrum (a) and the one stored at $85^{\circ}C/85\%$ RH (b).



Figure II.20: Deconvolution obtained for the infrared spectra of SiCN ((a) reference, (b) stored 9 300 hours at 85°C/85% RH)

In both cases, we obtained a consistent deconvolution with the same number of peaks and similar center. Hence, the choice of a Gaussian function is relevant.

The characteristic values of the infrared peaks are reported in Table II.8. Three columns with the variation relatively to the reference values were added.

	Peak Center (cm ⁻¹)		Peak Width (a. u.)		Peak Height (a. u.)				
	T0	Post 8585	Variation	T0	Post 8585	Variation	TO	Post 8585	Variation
Si-H	662	660	-0.3%	49.2	49.0	-0.4%	0.006	0.006	-3.0%
Si-C	804	808	0.5%	81.0	82.9	2.4%	0.063	0.057	-9.0%
Si-N	940	923	-1.8%	68.5	57.9	-15.5%	0.033	0.024	-28.1%
Si-O	1027	1033	0.6%	49.2	69.4	41.2%	0.023	0.052	130.7%
N-H	1139	1151	1.0%	45.3	45.0	-0.7%	0.004	0.004	-2.4%

Table II.8: Characteristic parameters of infrared peaks determined by deconvolution

Even with an adjustment of the peak centers, only small variations are observed. They are up to 20 cm⁻¹, which is consistent with the variations experimentally observed for Si-H bonds around 2100 cm⁻¹ (shift of 20 cm⁻¹). Due to the new chemical bonds, local atomic rearrangements occur and explain these shifts.

The main variations concern the oxygen and nitrogen related peaks. A significant increase in the Si-O bonds is accompanied with a decrease in the Si-N bonds. The first observation is consistent and corroborates the increase in the oxygen concentration seen with Tof-SIMS. We attribute the initial amount of oxygen before environmental storage to two factors:

- The native SiO₂ oxide that naturally forms on the silicon substrate
- The surface oxidation that directly occurs after SiCN layer deposition

Both phenomena can be observed in the Tof-SIMS oxygen profile of the reference sample in Fig. II.15.

It also corroborates the proposal of strong bonds between moisture and SiCN layers observed during the 125°C annealing trials. This is confirmed with the dissociation energies between silicon and oxygen in Table II.9. An oxidation of the SiCN layers occurs over time during environmental storage.

The decrease in the amount of Si-N coupled with the increase in Si-O bonds is consistent with the observations proposed by Lee on the oxidation mechanism of hydrogenated amorphous silicon oxynitride layers (SiON:H) [46]. The layers are progressively oxidized with the replacement of Si-N by Si-O bonds according to the following reaction:

$$Si_3N_4 + 6H_2O \rightarrow 3SiO_2 + 4NH_3$$

This reaction was used to explain the oxidation of nitride films by water vapor. In SiCN layers, there are also Si-NH and Si-NH₂ bonds that are oxidized, the corresponding reaction is:

$$Si - NH_2 + H_2O \rightarrow Si - OH + NH_3$$

These two reactions explain the results obtained with the deconvolution below 1300 cm⁻¹. We also observed the decrease in the Si-H peak around 2120 cm⁻¹. These bonds are oxidized by moisture to form more thermodynamically stable Si-O-Si and Si-OH bonds [47]. The dissociation energies are presented in Table II.9. It can be explained with the following reaction:

$$2Si - H + H_2O \rightarrow Si - O - Si + 2H_2$$

Bond	Dissociation energy (kJ /mol) at $25^{\circ}C$
Si-O	798
Si-N	439
Si-H	298
N-H	314
О-Н	428

Table II.9: Dissociation energies at 25°C of several bonds present in SiCN layers, from [48]

We explained the main chemical reactions occurring during moisture absorption for SiCN films. In the next subsection, we gather all information and propose a mechanism to explain the non-Fickian behavior of SiCN layers.

II.2.3. Moisture diffusion mechanism in SiCN layers

The objective of this section is to explain the sorption behavior observed with mass measurements in Fig. II.13(b). It is composed of two distinct slopes, one for the first 24 hours and a second one for the rest of the sorption.

With the present results, we observed that even in the first hours, oxygen concentration increases and moisture forms strong Si-O bonds with the SiCN layers. Hence, the difference between the mechanisms of the two slopes does not lie in the type of bonds. The most plausible explanation concerns the accessibility of reacting sites that bonds with moisture.

The SiCN layers comport methyl groups that create steric effects. The result is a lower density compared to SiN layers for instance as displayed in Table II.10. These densities were measured experimentally in our work.

Material	Density (kg/m ³)
SiCN 335	1870 ± 34
SiCN 350	1950 ± 38
SiN	2600 ± 7
USG (dense SiO ₂)	2140 ± 5

Table II.10: Density of several dielectric including the SiCN 335

We assume that the fast diffusion in the early hours is due to the easily accessible sites in SiCN 335 due to its nanoporosity. Once all these sites are occupied, the oxidation process is only directed by the chemical reactions presented in the last subsection.

Progressively, the nitrogen atoms are replaced by oxygen atoms. One of the consequences is that the local nanostructure changes. It can be explained with a description of the nanostructure in terms of network with rings. This explanation was proposed by Lee for SiON [46] and is adapted to our results for SiCN layers.

For dielectric films, the number of members of the rings can be various and it has been studied with ab-initio simulations. The number of members in a ring corresponds to the number of silicon atoms. Amorphous silica was studied by Bakos [49] and Kostinski [50] and silicon carbide was studied by He [51]. For SiO₂ the six members rings are the most present type. With simulation Bakos determined an activation energy for the diffusion of H₂O molecules of 0.79 eV for six members rings. When the number of members is reduced (smaller rings) the activation energy is drastically increased.

This can be done with chemical elements that have a higher coordination number. One of the differences between O and N atoms is their coordination number: 3 for nitrogen and only 2 for oxygen. As a result, the nitrogen can form more bonds which results in smaller rings. Macroscopically, the material density is higher with nitrogen atoms. The structure of SiN layers was described by Koseki [52].

We use these observations to propose a mechanism to explain the oxidation of SiCN layers. A simplified schematic is given in Fig. II.21 (carbon and hydrogen atoms are not considered).

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Figure II.21: Simplified schematic of the progressive oxidation of SICN layers. Based on Koseki [52]

We start from the structure presented by Koseki for SiN layers. We showed with the Tof-SIMS and infrared spectroscopy results that nitrogen and oxygen are the two main actors during the oxidation process. Thus, we assume that the simplified process showed in Fig. II.21 is true for SiCN.

During the oxidation of SiCN, the ring size becomes more important with the replacement of nitrogen by oxygen. It creates new diffusion pathways to access new nitrogen sites. The potential moisture diffusion path is represented with the dashed arrows in Fig. II.21; it becomes larger after oxidation. This mechanism repeats until the layer is fully oxidized. This non Fickian behavior was observed and studied for polymers. For epoxy resins, oxidation was proposed to explain the behavior observed by Wong [29].

If the layer becomes locally less dense due to the replacement of nitrogen by oxygen but its overall mass increases, then swelling must be present. The thickness of SiCN films after 9 300 hours is around 180 nm; initial thickness was around 150 nm. This corroborates our previous assumptions. However, thickness measurement is determined with spectroscopic ellipsometry. It requires the refractive index that can be modified by moisture. Hence, a second technique to assess thickness – such as Scanning Electron Microscopy performed on a cross section of the sample - is required to confirm the swelling.

For the SiCN studied, even after 9300 hours at 85°C/85% RH, the layer is still not fully oxidized. The same mechanism is probably true for the SiCN 350. One of the reasons that could explain the lower mass uptake for this layer is its higher density which plays a major role in the diffusion-reaction process.

One of the limits of this study on SiCN is the impossibility to observe any change in the first hours of storage with infrared spectroscopy. This could give more details on the mechanism in the first 24 hours.

As a perspective, additional analyses with the multiple internal reflection (MIR) technique could help to understand these first hours. This method allows the beam to be reflected multiple times in the sample and to obtain more signal for low concentration bonds. Thus, it is particularly suitable for bonds with relatively low concentrations in the layers such as H_2O related bonds. Description of the experimental setup and potential results can be found in the work of Rochat and Darnon [34], [53].

After these two first sections, we have gathered the diffusion parameters and we have explained the diffusion mechanisms in the different dielectric materials. But these investigations were performed only for the 85°C/85% RH storage. In the next section, we investigate the impact of temperature and humidity level on the diffusion parameters on one of the dielectric materials.

Effect of temperature and humidity on the diffusion **II.3**. parameters of USG

In this section, the influence of temperature and humidity level on moisture absorption is studied for the USG (dense SiO₂). We selected a dense PECVD SiO₂ for two reasons:

- The composition of this material is relatively simple and mainly consists of Si, O and H elements. We also observed a Fickian behavior in the previous section (Fig. II.4(a)), which is simpler to study.
- It is the main dielectric layer in one of the integrated stacks studied later in Chapter IV.

The description of USG can be found in Chapter I. For this study, the thickness is always 200 nm.

The objective of this section is to clarify the impact of temperature and humidity on intrinsic properties of USG that are the diffusion coefficient and the saturation value. These two parameters are determined with gravimetric measurements as described in Chapter I.

For each storage, an environmental chamber was used. Three wafers were monitored each time according to the method described in section II.1.1.

The list and the duration of each storage is given in Table II.11.

Temperature (°C)	Relative humidity (%)	Duration (h)
94	85	145
85	85	240
60	85	425
85	40	170
85	29.5	720

Table II.11: List of the environmental storages and their duration

For each storage the saturation was reached. For some storage such as 85°C/29.5% RH, the duration greatly exceeds the time to reach saturation due to logistical limitations. This longer storage confirmed that no more variation occurs once saturation is reached.

II.3.1. Diffusion coefficient

First, we consider the influence of temperature and humidity level on the diffusion coefficient. Fig. II.22 gives the influence of temperature at 85% RH (a) and relative humidity at 85° C (b) on the diffusion coefficient of USG.



Figure II.22: Temperature and relative humidity impact on diffusion coefficient for USG

• Influence of temperature

Thermal activation energy E_a can be calculated from Fig. II.22(a) that shows the diffusion coefficient between 60°C and 94°C. The diffusion coefficient D increases with temperature and follows an Arrhenius law:

$$D = D_0 \exp\left(\frac{-E_a}{RT}\right)$$
 (II. 6)

Where D_0 is the pre-exponential factor, R is the universal gas constant (= 8.314 J.mol⁻¹.K⁻¹) and T is the temperature.

From Arrhenius law, the activation energy for the diffusion coefficient is 0.75 eV and the preexponential factor is 1.1×10^{-4} cm².s⁻¹. E_a value is in the range observed by several research groups for silica-based materials as displayed in Table II.12.

Material	Temperature range (°C)	E _a (eV)	Do	Reference
PECVD SiO ₂	8-90	0.74	$3.3 imes 10^{-4}$	[25]
PECVD SiO ₂ - silicon hybrid	65-200	0.71	NA	[5]
Silica glass	160-1400	0.72	NA	[54]
Thermal SiO ₂	260-1150	0.69	NA	[55]
PECVD SiO ₂	60-94	0.75	$1.1 imes 10^{-4}$	This work

Table II.12: Arrhenius parameters for diffusion coefficients in silica-based materials. Reproduced and completed from [25]

• Influence of humidity level

The humidity level also affects the diffusion coefficient as shown in Fig. II.22(b). A linear dependency is observed; however, the variation range is smaller compared to temperature influence.

The increase in diffusion coefficient with higher relative humidity was also found by Ma [56]. In their work, they showed that moisture diffusivity along the interface between aluminum and a low-k polymeric material increases from 4×10^{-8} cm²/s at 10% RH to 6.5×10^{-8} cm²/s at 100% RH. The values are several orders of magnitude higher than the ones found in our study because it concerns interfacial diffusion. They do not interpret this diffusivity increase as a trend in their paper. Nonetheless, based on their results and the ones found in this study, we observe that the diffusion coefficient increases with increasing relative humidity.

• Interpolation at different temperatures and relative humidity

We compiled the previous data in Fig. II.23 in order to use them to determine diffusion coefficient at different temperature/RH couples.



Figure II.23: Diffusion coefficients as a function of temperature for different relative humidity for USG layers

In the following reasoning, we assume that the thermal activation energy found for diffusion (0.75 eV) is independent from the humidity level (this is represented with the parallel dashed lines in Fig. II.23). With that assumption, we can deduct by interpolation any diffusion coefficient in the range of $[60^{\circ}C - 94^{\circ}C] / [29.5\% \text{ RH} - 85\% \text{ RH}]$.

For instance, to calculate the diffusion coefficient at 60°C/40% RH, we have:

- $D = 1.7 \times 10^{-15} \text{ cm}^2/\text{s}$ at 85°C/40% RH
- $E_a = 0.75 \text{ eV}$

This leads to $D_0 = 5.6 \times 10^{-5}$ cm²/s with Eq. (II.6) Hence, at 60°C/40% RH, $D = 2.8 \times 10^{-16}$ cm²/s.

The main perspective here is to confirm that the activation energy can be considered constant when relative humidity varies. If this is validated, this should be applied to dielectric materials in order to collect their diffusion properties. One of the direct applications is to feed numerical simulations with accurate diffusion parameters over a wide range of temperatures and relative humidity levels.

II.3.2. Saturation value

Then, we investigate the influence of temperature and humidity level on the saturated moisture concentration value. Fig. II.24 gives the influence of temperature (a) and relative humidity (b) on the saturated moisture concentration of USG.



Figure II.24: Temperature and relative humidity impact on saturated moisture concentration for USG layers

• Influence of temperature

The saturated moisture concentration decreases with temperature as shown in Fig. II.24(a). This is consistent with results from Visweswaran [5].

According to the JEDEC JESD22-A120A [28], the saturated moisture concentration C_{sat} can be fitted as:

$$C_{sat}(T,P) = P_{H_2O} \times S_0 \times \exp\left(\frac{E_s}{kT}\right)$$
(II. 7)

Where P_{H2O} is the partial pressure of water vapor, S_0 is the pre-exponential factor, E_S is the activation energy of saturated moisture concentration, k is the Boltzmann constant and T is the temperature.

From Eq. II.7, we deduce an activation energy E_s of 0.48 eV and a pre-exponential factor of 4.4×10^{-10} mg.cm⁻³.Pa⁻¹.

• Influence of humidity level

Over the 29.5-85% RH range, the saturated moisture concentration is almost constant as shown in Fig. II.24(b). Fig. II.25, reproduced from Stern [57], represents different sorption isotherms.



Figure II.25: Henry, Langmuir and Dual-Mode isotherms. Reproduced from Stern [57]

The linear behavior from Henry's sorption can already be eliminated based on our experimental results (Fig. II.24(b)). To discriminate the exact mechanism between Langmuir and Dual-Mode, several points at very low relative humidity levels are required. Due to the small variations between 30% RH and 85% RH, the Langmuir sorption isotherm seems more plausible.

One of the implications of this model is that diffusing water molecules are absorbed in an immobile state in free sites of the materials [58]. In our case, due to the PECVD deposition technique, the USG layers have dangling bonds that can easily and strongly link with the diffusing molecules due to their covalent nature. Internal STMicroelectronics characterization reports around 20% of dangling bonds for this layer. This observation is consistent with the Langmuir assumption described above.

This assumption is also consistent with the decrease in C_{sat} observed with temperature in Fig. II.24(a). Takeda showed that the density of dangling bonds decreases with thermal annealing for hydrogenated polymorphous silicon [43]. With their results, we assume that the density of native dangling bonds of USG is lower at 94°C than at 60°C, which results in a lower saturated moisture concentration.

II.3.3.Summary of the diffusion parameters for USG

Table II.13 summarizes all the diffusion parameters found for the USG material at various environmental conditions.

T°/RH $D (cm^2/s)$ $C_{sat} (r)$		C _{sat} (mg/cm ³)
94°C/85%	$6.0 \ (\pm 0.5) imes 10^{-15}$	126.0 (± 1.7)
85°C/85%	$3.4~(\pm 0.5) \times 10^{-15}$	132.4 (± 6.3)
60°C/85%	$5.4~(\pm 0.3) imes 10^{-16}$	142.0 (± 1.3)
85°C/40%	$1.7~(\pm 0.1) \times 10^{-15}$	118.5 (± 0.8)
85°C/29.5%	$1.2 (\pm 0.1) \times 10^{-15}$	124.1 (± 0.4)

Table II.13: Diffusion parameters for USG (dense PECVD SiO₂)

In this section, we studied a dense PECVD SiO_2 layer under various environmental conditions. The diffusion coefficients and saturated moisture concentration were determined. We found that the diffusion coefficient does not only depend on temperature but also on humidity levels. Additionally, a thermal activation energy of 0.75 eV was found for diffusion and 0.48 eV for saturated moisture concentration both at 85% RH. From the sorption isotherm, small variations are observed for the saturated concentrations and a Langmuir mode is assumed to be dominating.

There are several objectives to complete this study:

- Validate that the activation energies determined at 85% RH are the same at 40% and 29.5% RH with storages at 60°C for instance (reasonable saturation times).
- Perform several storages at low relative humidity (below 20% RH) to validate the sorption mode.
- Confirm this method on different dielectric layers.

II.4. Conclusions

In this chapter, the diffusion of moisture in common dielectric materials used in the BEOL was experimentally studied.

Their diffusion behaviors were investigated at the standard 85°C/85% RH conditions. We identified three materials with non-Fickian absorption. This non-Fickian behavior had not been shown previously in the literature for dielectric materials. Moreover, a dual stage model used for non-Fickian polymers was adapted to fit the experimental data. Based on the diffusion models, the diffusion coefficients and saturated moisture concentrations were determined. These values will be used in Chapter IV to understand moisture diffusion in integrated stacks and implemented in numerical simulations.

Based on physical and chemical characterization techniques, we proposed explanations for the effects of moisture diffusion on dielectric properties. This includes layers with Fickian behavior, such as USG (dense SiO₂) and ULK (porous SiOC), and the SiCN layers that show a non-Fickian absorption. For the latter, we proposed a mechanism of absorption involving a fast filling of nanopores followed by a slow oxidation that consists of replacing nitrogen by oxygen atoms.

Separately, we characterize the influence of temperature and humidity on USG layers. Activation energies for diffusion coefficients (0.75 eV) and saturated moisture concentration (0.48 eV) were determined. These experiments also showed that diffusion coefficient is also impacted when the relative humidity varies. With these results, we proposed a method to extrapolate diffusion parameters over a wide range of temperature and relative humidity.

Several possibilities could be addressed in a future work:

- Application of multiple internal reflection technique to clarify phenomenon in ULK and SiCN layers
- Additional storage conditions to validate the assumption of the independency of thermal activation energy on relative humidity.
- If validated, application of the same storages to other dielectric materials to obtain a database of diffusion parameters that can be implemented in numerical simulation

In the next chapters, we use electrical characterizations to follow moisture diffusion. Hence, there is an obvious parameter lacking in this chapter: the dielectric constant. However, the dielectric constant measurements are performed externally. They were stopped early 2019 and should have restarted in 2020. It was unfortunately cancelled with the exceptional conditions brought with the Covid-19 situation.

These parameters are necessary to link the mass saturation values of this chapter to the capacitance saturation values in the next chapters. Hence, based on the material parameters determined, we will mainly discuss the kinetics of diffusion in integrated stacks.

Chapter III

Context and methods to study moisture diffusion in integrated stacks

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The philosophy of this work is to link intrinsic material properties to experimental observations on complex stacks that are similar to final products. In the previous chapters, we assessed moisture absorption behaviors for several dielectric materials. This can be considered as the first part of our work.

This chapter and the two following ones compose the second main part of our work in which we investigate moisture diffusion in integrated circuits.

The objective of this chapter is to introduce the problematic of moisture diffusion in integrated stacks and to present the techniques and the test structures used in Chapter IV to assess the impact of humidity on integrated circuits.

We start this chapter with a literature review of the problematic of moisture diffusion in integrated stacks. We also include a review of the numerical simulations that deal with moisture absorption.

In a second section, we briefly describe the 3D integration technology with a focus on the hybrid bonding Cu/SiO_2 technique. Then, the 3D integrated stacks studied in Chapter IV are presented and the sample preparation is described.

Finally, the different characterization techniques used in Chapter IV and V are introduced. Due to the complexity of integrated stacks, the simple techniques used in previous chapters are no longer relevant. Thus, to follow moisture absorption in these complex stacks, comb capacitance structures are implemented which allow us to perform electrical measurements. Additional physical and chemical analysis are also presented here.

III.1. Literature review of moisture effects on the Back End of Line reliability

In this section, a literature review of the impact of moisture on BEOL reliability is given. It is followed with studies investigating the kinetics and diffusion path of moisture. Then, a few words concerning numerical simulations are given. Several open questions in the literature are identified and are presented in the objectives of this chapter.

III.1.1. Context

Several moisture protections exist for the integrated circuits. The first one is the packaging materials. For high ends application (aerospace, military), the packaging materials consist of ceramic materials that makes them hermetic. However, for most commercial applications, it consists of polymeric materials. It is known that these materials are not hermetic and moisture can diffuse through [59], [60].

The second protection is the metallic seal ring that surrounds the die. It consists of metal lines and vias connected over the entire thickness of the die. It is schematically represented in Fig. III.1 and Fig. III.2. These metallic walls offer a mechanical protection against crack propagation that can occur during wafer dicing process. It also protects laterally from environmental contamination thanks to copper properties.

At the bottom of the die, silicon substrate, with thickness over 50 μ m, can be considered as hermetic. It was confirmed in Chapter I, where we showed that the substrate is not affected by moisture. However, the impact of moisture might need to be reassessed in the future with the introduction of new substrates like GaN, SiC.

For the topside of the die, passivation layers are deposited. They often include dense SiO_2 and SiN dielectrics. These materials are known to protect from moisture diffusion [61], [62]. A simplified schematic of a classic 2D integrated stack is given in Fig. III.1.



Figure III.1: Simplified view of a 2D integrated stack

Hence, with all these protections, integrated circuits should never be in contact with moisture. However, this is not the case and some failures observed on the field are moisture related. As mentioned, moisture will diffuse through the polymeric packages. Then, if some defects are present in the seal ring or in the passivation layers, moisture could potentially diffuse into the integrated circuits.

For the seal ring, it can be related to via not connecting to the underneath metal line. This leaves a path for moisture diffusion as displayed in Fig. III.2. For the passivation, it can be related to cracks or pads issues.



Figure III.2: Schematic of possible moisture path due to seal ring defect

III.1.2. Literature review

It has been known for a long time that moisture has detrimental effects on integrated circuits reliability. Some elements, like mesa transistors or nichrome resistors were known to be sensitive to humidity in the 60's. In 1976, Thomas cleared some "myths", as he describes them, concerning moisture effects on microelectronic packages [63]. This is one of the first paper showing the importance of surrounding humidity, i.e. moisture out of the package. With several other studies, it led to the development of encapsulation materials to protect integrated circuits from environmental contaminations.

For years, dense SiO₂ dielectric materials have been used in the BEOL of integrated circuits. Due to their high density, moisture had not been a major concern. However, to keep following the Moore's law [64] and the circuits miniaturization, new processes and materials were introduced. Insulating materials with lower permittivity than dense SiO_2 (k ~ 4.2) were required to counterbalance the increase in the interconnect resistive-capacitive (RC) delay due to device shrinkage. To achieve that goal, one way was to include new chemical elements in traditional SiO₂. The main candidates, which are now widely used, result from including carbon into SiO₂. It gave the SiOC:H, also called low-k materials ($k \sim 3$). To obtain an even lower dielectric constant, porosity was included to take advantage of the dielectric constant of air ($k_{air} = 1$). It led to Ultra Low k (ULK) materials (k < 3). These materials raise new challenges due to their lower density. After deposition, low-k and ULK are originally hydrophobic thanks to the surface methyl groups. However, they become partly hydrophilic during process integration [65], [66]. Hence, they are sensitive to the integration process during which water is present. Besides, during product lifetime, the diffusion of moisture into low-k/ULK layers through a defect will lead to a loss of performance or even to hard failure. Consequently, an increasing interest for low-k reliability regarding moisture has started in the early 2000's.

In 2000, Tsu and al. raised concerns for several aspects of the low-k reliability as shown on Fig. III.3, including moisture absorption [67]. From mechanical to electrical aspects, moisture can cause numerous failure modes. Early breakdowns and increase in the leakage current were observed in this study.



Figure III.3: Potential reliability issues. Reproduced from [67].

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These results were confirmed by Lloyd and al. who studied the time dependent dielectric breakdown (TDDB) behavior of ULK [68]. Their structures did not include a surrounding seal ring and were stored at ambient conditions for several weeks. A significant decrease in reliability was observed with an increase in both capacitance and leakage current of their comb capacitance structures. The moisture diffusion was also observed to be fast. It was possible to partially restore performances with annealing. The reliability deterioration and performance loss were confirmed by several other research groups [69]–[72]. The dissociation of water molecules was proposed to explain the increase in leakage current [73]. The damage caused by moisture diffusion on the BEOL have been studied extensively, however it was only recently that the impact of this diffusion in the BEOL leads to a loss of performance but the overall circuit lifetime is still dominated by FEOL failure mechanisms [74].

To explain the previously discussed reliability results, it is necessary to understand the interactions between moisture and integrated circuits. The possible -OH species related to moisture were studied by Proost for siloxane-based dielectrics and are represented on Fig. III.4 [9] as we already introduced in Chapter I. The impact of these different components on low k reliability was studied by Li and al. [75]. It was shown that physisorbed water (α bonds) could be removed at 190°C improving TDDB lifetime and leakage current. However, chemisorbed water (β bonds) is the main factor in the TDDB failure mechanism. These bonds can be removed at 400°C but even at this annealing temperature there is no total recovery and reliability is still degraded compared the reference samples. Guo and al. studied the question from a mechanical perspective for as-deposited and UV-cured SiOC:H [76]. One of the findings is, again, the predominant role of β bonds compared to α bonds.



Figure III.4: Types of -OH species. Reproduced from [9]

Apart from the electrical and mechanical effects due to moisture, it is important to assess the kinetics of diffusion in integrated stacks. Kubasch and al. calculated diffusion coefficients for moisture diffusion in metal-insulator-metal structures using SiOC:H and ULK materials [40]. Their results corroborate the fast diffusion observed for low-k and ULK by other researchers. The diffusion coefficients found are in the range of 10^{-11} - 10^{-12} m².s⁻¹ which is really higher than the ones we found in Chapter I for dielectric material bulks (it is not stated clearly in Kubasch's paper if it is bulk diffusion coefficients). Lin and al. found diffusion coefficients also in the range of 10^{-10} - 10^{-11} m².s⁻¹ for multilayers that include organosilicate glass (OSG) deposited on silicon substrate and capped with silicon nitride [20]. However, they associate this diffusion coefficient to interfacial diffusion. This is corroborated with the associated activation energies that are close to the activation energies for interfacial diffusion [25] (0.2-0.3 eV, three times lower than E_a for bulk diffusion). With secondary ions mass spectrometry, they conclude that

the main diffusion path is the Si/OSG interface. This also gives first insights on the diffusion paths in integrated stacks. But, as they state, "the diffusion paths in actual integrated circuits are likely to be different" and further investigation is required.

III.1.3. Numerical simulations

In most technologies, low k and ULK materials are used in deeper metal level. Hence, they are encapsulated and moisture is not supposed to reach them. As for the moisture absorbed during process steps, annealing is recommended to recover higher performances.

However, this might not be enough with the emergence of new technologies. New heterogenous integrations such as 3D integration (detailed in section III.2.2) might offer new diffusion paths for moisture. Cuts in the seal ring [77] offer solutions for RF technologies but they are prime candidates for moisture reliability issues. The spectrum of failures caused by moisture is also broad. It can be performance loss with an increase of the dielectric constant of insulating materials (global phenomenon). It can also be a very local issue such as an electrical breakdown or a mechanical delamination. In any case, it is important to have accurate models to assess local moisture diffusion path and kinetics with numerical simulations. These models would allow a finer assessment of moisture related risks. Two main categories could be explored:

- Simulations of process induced moisture. This would allow to evaluate the impact of each process step involving moisture and to adapt step durations and implement annealing properly. This implies liquid water and not only vapor.
- Simulation of the long-term diffusion. This would tackle the diffusion that can occur during product life, and that is mainly water vapor type. This would help to anticipate potential issues and to explain some failures observed on the field (modeling moisture diffusion through a passivation crack of defect in the seal ring and see if it matches experimental observations for instance). This could also lead to original designs adapted to specific applications. We adopted this approach in our work.

There is a lack of simulation for the diffusion into the die. However, the die packaging has been extensively studied with numerical simulations and the approach can be transposed. One of the issues when it comes to simulate multilayers structures is the saturated concentrations. This parameter differs from one material to another as seen in Chapter II, so it is discontinuous at the interfaces. To solve this discontinuity, the wetness fraction w was introduced [78], it is defined as:

$$w(t) = \frac{C(t)}{C_{sat}} \quad (III.1)$$

Where C represents the moisture concentration and C_{sat} is the saturated concentration that depends on temperature and humidity. The continuity obtained with w is illustrated on Fig. III.5 compared to the discontinuity of the moisture concentration.



Figure III.5: Concentration discontinuity solved with the wetness approach. Reproduced from [78]

Recently, this approach has been compared to several others and is still considered more general and able to address a broad variety of simulations [79].

There are also new challenges when it comes to integrated stacks. The geometrical ratios involved for dielectric layers can be really higher than for polymeric packages. Layers are often in the nanometer range for their thickness: a few hundred for BEOL dielectrics or a few tens for capping layers. But their other dimensions are in the millimeter range. Meshing the models becomes challenging in order to build accurate models with reasonable calculation times.

III.1.4. Objectives of our study of integrated stacks

Over the past twenty years, the sensitivity of low-k and ULK materials regarding moisture diffusion have been demonstrated. The main concern has been the moisture present in process steps. Thus, many studies include relatively short storages in temperature and humidity. They correctly represent process steps, but they might not be representative for long term moisture diffusion that can occur through defects during product life. The results differ when it comes to annealing. Some papers state that moisture removal is complete whereas in others it is only partial. One of the reasons might be that the conditions and duration of the storages differ from on paper to another. Hence, there is a need to clarify the impact of different couples (temperature/relative humidity). For instance, what differences can be observed between ambient and 85°C/85% RH conditions? Moreover, the diffusion path in actual integrated circuits needs to be clarified.

The main axes to be treated in this chapter are:

- Impact of temperature/humidity and duration of storages on moisture diffusion in integrated stacks
- Moisture diffusion path and interactions in the stacks
- Development of numerical models based on material properties determined in the Chapter II.

To study these different questions, we opted for 3D integrated test structures (Chapter IV) and structures with cuts in their seal ring (Chapter V).

III.2. 3D integration technology

III.2.1. Heterogeneous integration – More than Moore

Low-k and ULK materials have been introduced to keep up with the rhythm dictated by the Moore's Law. However, the inclusion of more porosity in these layers seems to reach a limit. The research for new candidates is ongoing. Amorphous boron nitride [80] seems promising but is still far from microelectronics fabs. Another solution could be the air gap integration but this requires a perfect hermeticity [81]. But limitations to follow Moore's Law are not restricted to the research of new materials. Devices self-heating, quantum effects, silicon's limitations are problems that need to be considered in the next miniaturization levels. And of course, even if the physics and engineering overcome these challenges, the cost of doing it might be prohibiting. As of 2020, Intel is still struggling to commercialize its 7 nm processors and only a few companies are still in this expensive race. Fig. III.6 shows how improvement in computer performance is slowing down in recent years.



1978 1980 1982 1984 1986 1988 1990 1992 1994 1996 1998 2000 2002 2004 2006 2008 2010 2012 2014 2016 2018

Figure III.6: Plateauing of computing performance. Reproduced from [82]

Consequently, a different path has been growing more and more over the past decades. It is referred to as the More than Moore approach. The idea is to include more features into a single package thanks to heterogenous integrations. The engineering philosophy is at the opposite of the one following the Moore's law. Instead of focusing on improving chip performances first and let the users adapt, it concentrates on the application desired by the end customers and the chips are selected and assembled accordingly. The components go from the microprocessor to memory, image sensor, etc. Combining complementary features into one package offers higher performance and smaller size. It is also a flexible approach that allows manufacturers to exactly meet their customers' needs. A System in Package (SiP) is the assembling of different components into a single package as shown on Fig. III.7. Chips can be placed side by side, stacked or embedded. Interconnections between different components is external. Wire bonding or flip-chip are examples of interconnection techniques. A detailed descriptions of the different heterogeneous integrations is available in the 2019 Heterogeneous Integration Roadmap [83].

Component 1	Component 4
	Component 5
Component 2	
Component 3	Component 6

Figure III.7: System in Package

As shown on Fig. III.7, the total area occupied by the components is important due to the 2D nature of the integration if components are placed side by side. Even with stacking, interconnections are still external and require space. The solution to solve these issues is a direct electrical connection between stacked integrated circuits.

III.2.2. Advantages of 3D integration

The development of 3D integration can solve the two issues mentioned previously. It is defined as "*an architecture where two or more active silicon devices are stacked and interconnected without the agency of the package*" [83]. The space gain is obvious with this integration. Connecting the different components also leads to higher performances but it is challenging. Fig. III.8 summarizes some of the 3D integration advantages.



Figure III.8: Advantages of 3D integration. Reproduced from [84]

There are several solutions to vertically interconnect the integrated circuits. Through Silicon Vias (TSV) is briefly described below and the hybrid bonding process used for our test structures is described in the next section.

• Through Silicon Vias (TSV)

TSV are vertical connections that are etched through the silicon substrate after the wafers have been thinned. A description of the different processes is available in [85]. These high aspect ratio trenches can directly interconnect two dies. Depending on the process, it can be connected to front, middle or back end of line of integrated circuits as displayed in Fig. III.9. In 3D integration, TSV is combined with direct bonding: two dielectric layers (one on each die) are bonded together to form the 3D stack.



Figure III.9: Schematic of different types of TSV [85]

There are several limitations and challenges for TSV. Due to mechanical stress, a keep-outzone of 10-20 μ m has to be kept around the TSV [86]. To maintain a correct aspect ratio while scaling to smaller dimensions is also of interest. There are few studies on the environmental impact on TSV structures reliability. In the case of a Ta barrier for TSV, moisture can react with it and degrade the TDDB performances [87].

III.2.3. Hybrid bonding Cu/SiO₂

Another approach is the hybrid bonding. As mentioned above, direct bonding can be used in 3D integration using TSV. Two dielectric materials are bonded together to assemble two separated dies. However, only mechanical connection is achieved and there is no electrical continuity at the bonding level. This is solved with hybrid bonding. We refer to the 2019 Heterogeneous Integration Roadmap for the definition of hybrid bonding:

"Hybrid bonding is defined as an inorganic dielectric-to-dielectric bond of opposing dies or wafers, where Cu pads are planarized with the inorganic dielectric, and make contact upon bonding."

Two wafers are processed separately, they follow a classical process integration until the last metal layer. After this step, a hybrid bonding via level (HBV) and hybrid bonding metal (HBM) level are added as shown in Fig. III.10. The difference with direct bonding is the presence of copper pads in the bonding levels. The dielectric material in these levels is a dense PECVD

SiO₂. The very high density of bonding pads offers many advantages in term of electrical connections. But they also rise process challenges. We briefly list some of them below:

- Surface planarity and cleanliness: This is crucial to obtain a good bonding quality. Both surfaces must be clean and plane to ensure the SiO₂/SiO₂ and Cu/Cu adherence. CMP is performed to meet the requirements. It is followed with several surface cleaning.
- **Pads alignment:** Each pad must be aligned with its counterpart on the corresponding wafer. The dimensions involved are in the μ m range, hence, alignment must be performed adequately.
- **Bonding:** The first step is performed at ambient room temperature. It results in weak bonds that are enough to maintain the two dies in place. At this stage, it is still possible to separate them. To consolidate the stack, an annealing at high temperature is applied.

Sart did a thorough description of the process and discuss some of the alternatives [88]. His work tackles several aspects of the mechanical stress involved in 3D stacks. It follows studies from Taibi [89] and Beilliard [90] at different stages of the development of hybrid bonding technology.



Figure III.10: Hybrid bonding description

As it appears in Fig. III.10, bonding pads are also used in the seal ring perimeter. Hence, there is no continuous copper barrier at the bonding levels and the dielectric material is directly exposed to moisture. Beillard had some first results on the moisture reliability of hybrid bonding. He implemented daisy chains in the bonding levels and monitored their resistance. After 168 hours of storage at 85°C/85% relative humidity, there was no significant variation. This was performed on simplified stacks and the storage duration was relatively short. To complete these first results, fully integrated stacks need to be tested for longer durations. The potential impact on the BEOL levels also needs to be assessed.

After hybrid bonding, the stack is similar to the schematic on the right in Fig. III.10. There are still several steps to perform. The first one is the silicon thinning to reach a few μ m for the top die. Then depending on the process, trenches are etched trough the silicon to connect pads on the top surface. Micro lenses can also be processed as it is one of the very interesting applications of 3D integration to directly combine image sensors on top of the circuitry treating information.

One last aspect concerning 3D integration is the possibility to perform bonding at different scales. This leads to a compromise between the number of 3D dies produced and yield. The different approaches are summarized in Fig. III.11. The die/die bonding allows to only select functional dies and obtain a yield close to 100%. Besides, it is possible to combine different sizes and shapes. However, all bonding steps are multiplied leading to a longer time compared to the wafer/wafer bonding. The backgrinding of the top die also becomes challenging. Only wafer to wafer bonding was used in our work.



Figure III.11: Different scale options for hybrid bonding, reproduced from [90]

In the next section, the test structures studied are described. We selected a 3D integrated stack normally dedicated to imaging applications. Several modifications were implemented in order to study moisture diffusion both at hybrid bonding and in BEOL levels. The interest of using such stacks also lies in the variety of materials present.

III.3. Description and preparation of 3D integrated stacks

III.3.1. Description of the test structures

The test structures studied are shown in Fig. III.12. This type of 3D integrated stack is normally designed for imaging applications. It consists of an image sensor (top die) with the logical circuitry directly below (bottom die). In our case, several modifications were made for practical purpose, some of them are detailed below. We focus our study on the dielectrics used in the BEOL, so Front End is inactive in our structures. To study the impact of moisture diffusion, copper capacitances were implemented in the first levels of BEOL on both upper and

lower sides. These capacitances are directly connected to pads on the top surface. At hybrid bonding levels, daisy chains were implemented (Fig. III.17), they are also connected to pads on the top surface that allows us to measure their resistance.



Figure III.12: 3D stack studied

A schematic top view of the test structure is given in Fig. III.13. There are six comb capacitance structures implemented on each die. Only the six from the top die are displayed, the other six are directly below in the bottom die. They are also connected to the pads on the top surface (green pads on Fig. III.13). The two daisy chains implemented at hybrid bonding levels are displayed in Fig. III.17. They are also connected to pads on the top surface (blue pads on Fig. III.13).



Figure III.13: Schematic top view of the test structures (top aluminum and silicon layers not represented)

Details concerning materials and geometrical parameters for each level are given below.

• Top die:

As mentioned, the top die is normally an image sensor. For practical purpose, the last levels with micro lenses were not processed for our study. Instead, only a layer of aluminum was deposited. It allows an easier manipulation and protects from top side diffusion. The BEOL of this die is mostly composed of two dielectrics: a dense PECVD SiO₂ called USG and a carbon doped silicon nitride deposited at 335°C simply called SiCN 335. Both were studied under the

same name in Chapter II. The thicknesses are detailed in Fig. III.12. Comb capacitance structures were implemented over three metal levels and interconnected with metal vias. A focus is given in Fig. III.14.



Figure III.14: Comb capacitance structures in the top die (USG side)

The interdigital space and the thickness of the copper fingers are given in Table III.1.

	Top die (USG side)	Bottom die (ULK side)
Finger width (nm)	100	90
Interdigital space (nm)	105	64

Table III.1: Geometrical parameters of comb structures

• Bottom die:

The comb structures are implemented in the first levels of metal (from 2nd to 5th). For these levels, the dielectrics are a porous SiOC:H called ULK and a silicon carbonitride deposited at 350°C called SiCN 350. Both were studied in Chapter II. A focus is displayed in Fig. III.15 and geometrical dimensions can be found in Fig. III.12 and Table III.1.



Figure III.15: Comb capacitance structures in the lower die (ULK side)

• Hybrid bonding level:

Fig. III.16 gives a description of the daisy chains implemented at the bonding level. The daisy chains are composed of the hybrid bonding metal (HBM) and hybrid bonding vias (HBV) of the top and bottom dies.



Figure III.16: Cross section of hybrid bonding level

These chains go from the top die to the bottom die (50 700 times). A simplified sectional view of the daisy chains is presented in Fig. III.17 (the real density is higher than on the figure). The resistance is monitored with pads on top surface. The dielectric material in these levels is a TEOS based SiO₂. The first daisy chain is located at 270 μ m from the seal ring.

Figure III.17: Sectional view of daisy chains from Fig. III.16

III.3.2. Sample preparation

As mentioned previously, wafer to wafer bonding was performed in our work. Due to the cost of such integration, we cannot use the entire integrated wafer for only one storage condition. The solution is to work at die level since there are around sixty 3D integrated dies available per wafer. Fig. III.18 represents the flow followed for each wafer.



Figure III.18: Sample preparation from hybrid bonding to sawing process

• Backgrinding

The initial thickness of silicon substrate is 770 μ m as mentioned in Chapter I. This is not acceptable for sawing process. The backgrinding step consists in removing most of the substrate thickness. In our case the final thickness is 120 μ m. This has no impact on our experiments, it just needs to be thick enough to avoid breakage during dies manipulation.

• Wafer dicing

Also called die singulation, this is the process by which die are separated from each other. This is done in two steps. First, a laser precut is applied (laser grooving). It follows the sawing paths planned and it is a few μ m deep inside the silicon substrate. Then, a mechanical sawing is performed to cut the remaining silicon substrate and singularize each die. During sawing steps, water is applied for short durations as described in Table III.2. It is removed only with blown air. The impact of this water is evaluated in section III.5.

Table III.2: Water exposure during wafer dicing

Step description	Exposure to liquid water
Before laser grooving – Cleaning	30 seconds
After laser grooving – coating removal	60 seconds
Mechanical sawing - Cooling and lubricate	5 to 10 minutes
After mechanical sawing - Cleaning	30 seconds

In order to study the reliability of 3D integrated stacks and to make sure moisture diffuses into the samples, two sawing plans were followed as described on Fig. III.19. For each plan, three integrated wafers were available. The sawing plan 1 corresponds to the normal sawing conditions. It is used here to confirm the reliability of these structures regarding moisture diffusion. With the plan 2, the sawing was performed 60 μ m inside the die. Hence, the external seal ring was fully removed on one side of the samples over the entire thickness. This side is directly exposed to moisture. The distance between the opening and the first capacitance is around 220 μ m as mentioned in Fig. III.19.



Figure III.19: Sawing plans used for 3D stacks. Seal ring remains intact with sawing 1 and fully open on one side with sawing 2 After sawing steps, two populations of samples are available and will be referred to in the next sections as:

- Intact seal ring (sawing plan 1)
- Open seal ring or damaged seal ring (sawing plan 2)

• Environmental storages

Once the dies had been individually sawn, different types of storage were performed. This requires using an equipment that can precisely control a wide range of temperature and relative humidity couples. For most of them, the climatic chamber presented in Fig. III.20 is used already presented in Chapter I). A second equipment is required for temperature above 100°C. This allows us to perform a standard Highly Accelerated Stress Test (HAST): 96 hours at 130°C and 85% RH. For ambient storages, dies were simply kept in the lab at ~23°C / 45% RH.

To study moisture removal, the samples are directly placed on a heating chuck in the capacitance measurement tool. The kinetics of annealing can then be studied. Temperatures up to 300°C degrees can be reached with this technique.



Figure III.20: Climatic chamber used for most storages

III.4. Characterization techniques

The three main techniques (mass, stress and IR characterizations) used to determine intrinsic material properties are not suitable to study 3D integrated stacks. First, it would force studies on full wafers in order to use these tools. This would reduce our flexibility and limit the number of different storages done due to the cost associated to obtain several wafers. Second, it would only give global results and it would not be possible to find moisture diffusion path and specific interactions within the stacks.

In this context, the characterizations fall into two main categories that are detailed below: on the one hand electrical characterizations and on the other hand physical and chemical analyses. Thus, for the first part, the comb capacitance and resistance structures implemented allow to study specific part of the entire stack. The voltage breakdown of capacitances was also studied. In the second category, several physical and chemical analysis were performed to understand moisture diffusion path and local interactions.

III.4.1. Electrical characterizations

Moisture affects electrical properties in several ways. It increases the overall permittivity and the leakage current. It lowers the voltage breakdown and it can also cause corrosion. There are three main parts in the 3D stacks: top die (USG as dielectric), bottom die (ULK as dielectric) and bonding level (TEOS as dielectric). For top and bottom dies, comb capacitances are studied. At hybrid bonding level, the resistance of the daisy chains is monitored. The first measurements were performed before backgrinding and wafer dicing steps. The wafers are considered dry and all variations mentioned hereafter are based on these initial reference measurements.

• Capacitance:

The capacitance depends on the dielectric materials and on the dimensions of the copper combs. For an interdigitated finger capacitor, the total value is the sum of all parallel capacitances as shown on Fig. III.21:

$$C = (N - 1)\varepsilon \frac{WL}{d}$$
(III. 2)

Where W and L are respectively the width and the length of metal plates of the finger, N is the number of fingers, d is the distance between the two plates and ε is the permittivity of the material between the two plates. The permittivity is related to the relative permittivity or dielectric constant ε_r with the vacuum permittivity ε_0 (8.85 × 10⁻¹² F.m⁻¹) as:

$$\varepsilon = \varepsilon_r \varepsilon_0$$
 (III. 3)

When moisture diffuses into the structures, it increases the permittivity of the materials due to its dielectric constant ($k_{H2O} \sim 80$). In order to assess a potential impact of temperature on the geometrical parameters (thermal dilatation), we stored one reference structure at 250°C. No

significant variation was measured; thus, the geometrical parameters are considered constant and only moisture is responsible for the capacitance variations in our study.

The total variations measured for capacitance correspond to variations of the dielectric constant for each material in presence of water.



Figure III.21: Capacitance structures (USG side is represented)

The capacitance measurements were performed with a Keysight Technologies E4980 LCR meter. To determine at which frequency the measurements will be done, the magnitude of complex impedance of several capacitances for upper dies and lower dies was studied. It is shown in Fig. III.22 for both top (USG as dielectric) and bottom die (ULK as dielectric). Only one curve for each die is presented but the same results stand for the different capacitances in each structure and from on structure to another.

The cutoff frequency was measured around 100 kHz as shown on Fig. III.22. Hence, to avoid any parasitic effect, the following capacitance measurements are all performed at 10 kHz.



Figure III.22: Magnitude of complex impedance for both upper and lower die

We adopt the same formalism as for mass to present the results. The capacitance variation due to humidity is given by:

Relative capacitance variation =
$$\frac{C(t) - C_{ref}}{C_{ref}}$$
 (III. 4)

Where C(t) is the capacitance value measured at the instant t and C_{ref} is the capacitance measured before sawing steps.

• Leakage current and voltage breakdown measurements:

As it was described previously, moisture increases the leakage current and lowers the voltage breakdown. Even though the breakdown is a local phenomenon and these measurements are destructive, it gives valuable information and it helps to assess how moisture degrades stacks.

For the current voltage curves, applied voltages were up to 70 V (that corresponds to electrical fields up to 10 MV/cm for our test structures). The electrical fields were deduced from TEM analysis that gives the real distance between metal lines and vias. These distances differ from design theoretical distances.

• Resistance measurements

The resistance of the daisy chains was monitored to determine moisture impact on hybrid bonding level. Following an I(V) characterization of the resistance, a voltage of 5 V was applied. This test however does not inform on the presence of moisture in the dielectric material as the resistance value will only change if the metal is impacted by corrosion for instance. Implementing comb capacitance structures at bonding level requires a more complex design and might complicate the bonding process because larger area needs to be aligned and bonded together. It would be of interest for future investigations.

III.4.2. Physical and chemical characterizations

Electrical characterizations give results concerning the kinetics of diffusion, the total amount of moisture diffusing in and the conduction mechanisms. However, it is not enough to determine the diffusion path and where moisture is absorbed in the materials. Additional physical and chemical analyses are required (see Chapter I for Tof-SIMS description).

• Transmission electron microscopy (TEM)

One of the drawbacks of Tof-SIMS used in our work is the size of the sputter area. When it comes to studying integrated stacks, more precision is required (capacitance fingers are separated from each other by ~100 nm). And, as mentioned above, the sputtering times are material dependent. The difference between copper and porous dielectric would make it impossible to precisely know the sputtering depth for instance. Hence, to analyze complex stacks, we used transmission electron microscopy coupled with energy dispersive X-ray (described below).

In order to perform a TEM analysis, a lamella is prepared with focused ion beam (FIB) technique. The thickness of the lamella is around 100 nm. In TEM, a high energy electron beam is used on the sample. Thanks to the interactions transmitted through the sample, an image is formed and its contrast depends on difference of atomic number of the present elements and crystallinity.

• Energy Dispersive X-Ray (EDX)

As mentioned above, TEM can be associated with EDX analysis. It gives chemical composition of the samples (except hydrogen and some other very light elements that are not detected). An incident electron beam stimulates the emission of X-rays which are characteristic of present elements. It is also proportional to the element quantity in the sample. In our study, we compare dry and moisture saturated samples. The focus is on the oxygen concentration to understand moisture diffusion. Other elements also give additional information on the existing interactions and mechanisms.

• Electron Energy Loss Spectroscopy (EELS)

TEM can also be coupled with EELS analysis. This method is similar to EDX, an electron beam is applied to the analyzed sample. The amount of energy loss due to inelastic collisions of the electrons with the sample is analyzed and gives the elemental composition. One of its advantages over EDX is that it informs on the local environment of each elements, thus, it gives information concerning the chemical bonds. However, it is less adapted than EDX for heavier elements such as tantalum in our samples.

III.4.3. Summary

From all the techniques used in the literature, we kept simple electrical analysis to obtain insights on the diffusion kinetics and quantity of moisture absorbed. The experimental data will be used to feed numerical simulations to validate several assumptions. To complete our understanding, the physical and chemical methods described above will be performed. It will allow us to test the reliability of 3D integrated stacks (industrial objective) and to understand moisture diffusion in integrated stacks in common dielectric materials (fundamental understanding). Table III.3 summarizes the techniques and their expected results.

Characterization technique	Results	
Capacitance measurements	Diffusion kinetics and saturation values Mechanisms reversibility	
I(E) tests	Degradation mechanisms Mechanisms reversibility	
Resistance measurements	Moisture presence at bonding levels	
Tof-SIMS	Moisture diffusion path (wafer level)	
TEM-EDX	Moisture diffusion path (IC level) Chemical interactions	

Table III.3: Summary of characterization techniques with their expected results

III.5. Conclusion

In the chapter, we introduced the context and we presented a state of the art of moisture diffusion in integrated stacks. This allowed to define the main areas of focus for the two next chapters:

- Impact of temperature/humidity and duration of storages on moisture diffusion in integrated stacks
- Moisture diffusion path and interactions in the stacks
- Development of numerical models based on material properties determined in the Chapter II

After a brief description of the 3D integration process, we presented the test structures studied in Chapter IV. Then, the different characterization techniques used in Chapter IV and V were introduced.

In the next chapter, we will study a 3D integrated stack at various environmental conditions. A complete investigation is presented in order to explain the interaction between moisture and the different materials present in the stack.

Chapter IV

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The aim of this chapter is to understand moisture diffusion path in the 3D integrated stacks presented in Fig. IV.1 and the underlying interactions depending on the type of storage performed.

Low-k and ULK are used as the main dielectric material in the bottom die. Their sensitivities regarding moisture diffusion have been demonstrated over the past twenty years as presented in Chapter III. However, there is a need to clarify the impact of different couples (temperature/relative humidity) on these materials. Moreover, the diffusion path in actual integrated circuits needs to be clarified.

A second objective is to qualify the reliability of 3D integrated stacks regarding moisture. With the structures selected for this work (Fig. IV.1), the hybrid bonding Cu/SiO₂ techniques lead to a seal ring discontinuity as presented in the previous chapter. This protection discontinuity forms a potential path for moisture to diffuse in. From an industrial perspective, it is necessary to assess the reliability of such structures regarding humidity absorption. This will complete the work done by Beilliard [90].



Figure IV.1: 3D integrated stack studied in this chapter

In the first section, the reliability of the 3D integrated stacks is assessed from the hybrid bonding levels to the deeper BEOL layers for top and bottom dies. Then, the seal ring is fully sawn on one side to let moisture diffuse in. Several environmental conditions, including ambient and 85°C/85% RH, are performed and followed by electrical characterizations with physical and chemical analyses. The effects of different storage conditions are then presented, it is logically followed with annealing experiments to study moisture desorption.

The moisture diffusion path and its interactions with the stacks are finally studied with Tof-SIMS and TEM EDX analysis. A discussion on some limitations linked to these techniques follows.

In the last section, finite elements modeling of our samples is performed. We used a classic analogy with thermal diffusion. The simulations combine the intrinsic material properties

determined in Chapter II with the experimental results obtained on 3D stacks. This allows us to discuss some of the phenomenon observed and to corroborate several hypotheses. Finally, a complete explanation of moisture diffusion in the integrated stacks is presented and perspectives for future work are proposed.

IV.1. Reliability of 3D integrated stacks

Fig. IV.2 gives a schematic of the protection offered by seal ring on 3D stacks. A discontinuity exists at hybrid bonding levels and dielectric material (dense PECVD SiO₂) is directly exposed in this area. In this section, the reliability of 3D integrated stacks regarding moisture diffusion is assessed with electrical measurements combined with physical and chemical analyses.



Figure IV.2: Schematic of seal ring protection on 3D stack (a) top view and (b) cross section

IV.1.1. Hybrid bonding levels

The resistance of the daisy chains implemented at the hybrid bondage levels was measured after several storage conditions. The results are displayed in Fig. IV.3.



Figure IV.3: Resistance variations of daisy chains implemented at hybrid bonding levels after ambient or 85°/85% RH storages

Almost no resistance variation is measured even after very long storage durations at ambient conditions and at 85°C/85% RH. These small variations could be explained by some equipment drift over time. It represents a diminution of around 10 ohms for a resistance of 4100 ohms. To complete these first results and ensure that no moisture is present in the daisy chains, a TEM EDX analysis was performed on a die stored several months at 85°C/85% RH. Fig. IV.4 shows a TEM view of the entire stack. A focus on the Cu/Cu interface at hybrid bonding levels is given in Fig. IV.4(b).



Figure IV.4: TEM view of the entire stack (a) and focus on the Cu/Cu interface at hybrid bonding levels (b)

Fig. IV.5 gives the results of the TEM EDX analysis performed at the Cu/Cu interface. It corresponds to the area highlighted in red in Fig. IV.4(b). Fig. IV.5(a) shows the mapping with the three main elements: copper in red, tantalum in yellow and oxygen in green. The yellow box corresponds to the area analyzed for profiles in Fig. IV.5(c) and the yellow arrow gives the direction of the profiles, from top to bottom. Fig. IV.5(b) only displays oxygen to underline its absence at Cu/Cu interface.



Figure IV.5: EDX mapping at hybrid bonding levels, (a) and (b) show respectively three elements and only oxygen. (c) gives the chemical profiles for each element across the Cu/Cu interface

There is no trace of oxygen at the Cu/Cu interface even after several months of storage as displayed in Fig. IV.4b. The chemical profile of oxygen in Fig.IV.4c shows a very low and constant oxygen concentration and confirms the absence of oxygen at the Cu/Cu interface.

We assume that this very low oxygen percentage could be attributed to the preparation of the lamella used for the EDX analysis. A schematic top view at the hybrid bonding level is given in Fig. IV.6. As the dimensions of the daisy chains are below $4 \mu m$, the placement of the EDX lamella is challenging. The lamella could include some of the SiO₂ dielectric surrounding the daisy chains in its thickness. The oxygen of this dielectric would then be detected during the EDX analysis as the entire thickness of the lamella is analyzed.



Figure IV.6: Top View at hybrid bonding level to illustrate potential spherical effects observed in TEM EDX due to lamella's thickness

No trace of oxygen is detected at copper interfaces with TEM EDX. It corroborates the electrical results. No moisture is present for structures distant from 270 μ m of the edge (Fig. III.17). This is consistent with diffusion coefficients of the dielectric material at bonding levels. From intrinsic material studies, diffusion coefficient of TEOS based SiO₂ is 2.7 x 10⁻¹⁵ cm².s⁻¹ (Chapter II). It would take hundreds of years to reach the first daisy chain at 270 μ m from the cut.

IV.1.2. Top and bottom dies

Even if there is no sign of moisture at hybrid bonding levels, it is necessary to assess the reliability of the bottom (ULK side) and top (USG based SiO₂) dies to confirm that the seal ring discontinuity at hybrid bonding levels does not lower the overall reliability of the 3D stack. To investigate this question, the capacitance structures described in Fig. IV.1 are measured after different kind of storages.

Fig. IV.7 shows the average capacitance variations after five months at ambient or at $85 \degree C/85\%$ RH for top and bottom dies.



Figure IV.7: Relative capacitance variations for top and bottom dies after five months at ambient or at 85°C/85% RH

Little variations with almost no deviation are observed here for both top and bottom dies. Values are the same after five months at ambient or at 85°C/85% RH. These variations are likely to be due to equipment drift or testing pad degradation over time and are negligible.

To complete and confirm these results, I(E) experiments are performed. I(E) curves for both oxides are shown in Fig. IV.8. For USG (dense SiO₂), breakdown occurs around 6.3 MV/cm after five months at 85°C/85% RH, which is the value measured on reference samples. Moreover, curves shape is not modified by storage.



Figure IV.8: I(E) curves for intact seal ring samples ((a) top die and (b) bottom die): reference and after five months at 85°C/85% RH

For ULK, breakdown values are around 9.3 MV/cm both for references and after five months at 85°C/85% RH. The same observation made for dense SiO_2 samples on curves shape is true for ULK samples. Hence, I(E) tests confirm that there is no significant drift for intact seal ring structures.

These results confirm that no moisture diffusion occurs from hybrid bonding levels to deeper metal layers. Moreover, seal ring is only discontinuous at hybrid bonding levels, top and bottom dies are protected with a continuous surrounding metal wall (Fig. IV.2). Thus, it also confirms that metal continuity around the die is efficient regarding moisture protection.

IV.1.3. Conclusions concerning reliability of 3D stack

A 3D integrated stack has been studied regarding moisture diffusion. Samples were stored at conditions up to 85°C/85% RH with durations exceeding usual standards. No variation was detected by means of electrical characterizations and TEM EDX analysis. The seal ring discontinuity at hybrid bonding levels does not lower the overall reliability of the stack. This does not mean that hybrid bonding levels are hermetic, but it shows that moisture diffuses slowly at bonding interface and is not a reliability issue for standard 3D product lifetime.

IV.2. Electrical characterization of the effect of temperature and humidity on moisture absorption

The previous results confirm the integrity of 3D stacks regarding moisture when no invasion is made on seal ring integrity. However, it does not help to understand how moisture diffuses into the stacks when the seal ring is damaged or if seal ring needs to be removed or partially open to satisfy technological purposes as we mentioned in Chapter III.

To investigate these interactions, the seal ring was fully removed on one side to let moisture diffuse in as described in section 3 of Chapter III. Then, several storage conditions were performed and compared thanks to electrical measurements.

There are two issues of practical interests to investigate before going further:

- The sawing process involves water and its impact needs to be assessed
- Around 60 dies were individually available after sawing process for different environmental stresses. But the different storage conditions could not be performed simultaneously. Thus, the effect of storage time at ambient on subsequent environmental stresses needs to be evaluated

IV.2.1. Investigation of potential experimental limitations

IV.2.1.1. Sawing process impact

During the sawing process, water is used at different steps as described in Chapter III. It is important to assess its impact on our samples. As mentioned in the previous chapter, sawing steps and electrical measurements are not performed in the same industrial site. It explains the 5 hours delay between the sawing and the first measurements.

The sequence followed is summarized in Fig. IV.9.



Figure IV.9: Summary of the sequence followed to study the impact of sawing steps

- Die 1 was monitored at laboratory ambient conditions (23°C/~ 45% RH).
- Die 2 was annealed at 125°C overnight then followed at laboratory ambient conditions. The objective is to see if it is possible to recover the initial performances and then to compare ambient storages with or without annealing.
- Die 3 was annealed at 250°C overnight then followed at laboratory ambient conditions with a similar objective as die 2.

We only present the results for the capacitance from bottom die (ULK) close to sawing as displayed in Fig. IV.10. The results are similar for other capacitances in bottom die, only the magnitude of variations differs. For the top die (USG as dielectric), no variation is observed.





Figure IV.10: Description of open seal ring samples (schematic top view)

Fig. IV.11 shows the recovery obtained with both annealing conditions. Because, both are performed on the same tool, the 250°C annealing was performed one day later than the one at 125°C. This explains the higher variation measured before starting the annealing.



Figure IV.11: Effect of 125°C and 250°C annealing on the ULK capacitance located at 220µm from opening

Most of the moisture is removed with both annealing, hence moisture is not strongly linked. This weakly bonded moisture was described in previous chapters as α bonds. In both cases, total recovery was not reached and the last 3% variation could not be removed. Higher temperatures are required (β bonds start to be removed around 400°C [75]). But these temperatures are close to materials deposition temperatures and might cause material modifications. Thus, it was not studied here.

After annealing, die 2 and 3 were monitored at ambient laboratory conditions. Their kinetics is compared in Fig. IV.12 with die 1 that was monitored at ambient conditions (its first point is 5 hours post sawing). The first points for die 2 and 3 correspond to C_0 in Fig. IV.9.



Figure IV.12: Comparison of kinetics for dies with and without annealing

Die 2 and 3 have variations similar to die 1 after five hours at ambient conditions (around + 12% as shown in Fig. IV.12). It shows that these variations are caused by ambient moisture and are not due to water used during sawing steps.

A difference can be observed for die 3 that was annealed at 250°C. The kinetic at ambient differs and the saturation value is lower compared to the two other dies. Thus, a 250°C annealing is already enough to cause material modifications. The kinetics of die 1 and 2 are identical, thus, 125°C should be privileged for moisture removal because it does not cause material modifications. This results for integrated stacks are consistent with several JEDEC norms for organic material used in electronic devices such as JESD22-A120A [28] (gravimetric method to follow moisture absorption in organic materials).

IV.2.1.2. Impact of waiting time at ambient prior to storage

Only one environmental chamber is available to perform storages. Each storage requires relatively long durations – several weeks in general – until saturation can be observed. Hence, most of the samples are stored at ambient lab conditions before starting storages in the environmental chamber. For the bottom dies with ULK as dielectric, capacitance variations are observed at ambient conditions (this will be discussed in more details in the next section). Hence, there are already some variations before starting other storages. The objective of this subsection is to assess the impact of the time spent at ambient conditions before starting storages in environmental chambers. To do so, we compared moisture diffusion at 85°C/85% RH for two dies:

- Die 1 was placed in the environmental chamber at 85°C/85% RH only 6 hours after sawing
- 2. Die 2 was kept 17 months at ambient conditions and then stored at 85°C/85% RH

We only present results for the bottom die in this section. We did not include the top dies with USG dielectric because no variation is observed. It will be discussed in the next section.



Figure IV.13: Monitoring of capacitances from die 1 and 2 at 85°C/85% RH

After 17 months at ambient conditions, all capacitances of die 1 are saturated around + 27%: this corresponds to the starting point of the $85^{\circ}C/85^{\circ}$ RH storage displayed in Fig. IV.13. For die 2, capacitance relative variation (~ 10% at least) is also present for the structure closest to the cut, so we can conclude that moisture is also present due to the 6 hours spent at ambient conditions (lower values correspond to capacitance further from the cut).

After 400 hours of storage at 85°C/85% RH, die 1 and 2 reach similar saturation values. Respectively, $55.6 \pm 0.8\%$ and $61.0 \pm 1.8\%$. Hence, the time spent at ambient (up to 17 months) has little impact on the saturation value reached with an 85°C/85% RH storage. More generally, based on these results, we consider that the waiting time at ambient does not impact the saturation value of subsequent environmental storages.

IV.2.1.3. Conclusions

Two possible limitations were studied in this section. First, the potential impact of water present during sawing steps was assessed. We confirmed that the variations observed in the first hours are caused by moisture present in the ambient atmosphere and not by the water present during sawing.

The second limitation concerns the storage time at ambient condition before starting storages in environmental chamber. Two dies were stored at 85°C/85% RH, one of them directly after sawing and the second 17 months post sawing. They show similar capacitance saturation values. This confirms that storage at ambient has little impact on following storages at 85°C/85% RH. We assume that this remains true for storage at relatively high temperature (> 60° C).

In the next section, the impact of temperature and humidity on moisture absorption in integrated stacks is presented.

IV.2.2. Results and discussion

In order to study the impact of temperature and relative humidity, the storage conditions and their duration presented in Table IV.1 were performed. In the rest of the chapter they can be referred to with their simplified name (1st column of table 1) to lighten the text.

Storage	Temperature (°C)	Relative humidity (%)	Duration (h)
Ambient	~23	~ 45	3 600
85/85	85	85	3 600
85/40	85	40	192
85/29.5	85	29.5	550
60/85	60	85	360
94/85	94	85	168
30/85	30	85	650 (stopped before saturation)

Table IV.1: List of the storages performed

For each storage, at least 2 samples with damaged seal ring and 1 sample with intact seal ring (serving as reference) were stored. The durations are equal or superior to the time required to reach saturation when capacitance variations are observed. The only exception is the storage at 30°C/85% RH that was stopped before saturation was observed.

For more clarity, the two sides of the 3D stack are presented separately. First, the impact of moisture on the top die with USG as dielectric is presented and discussed. Then, the results for the bottom die with ULK as dielectric are presented and discussed. All the results hereafter only concerns structures with seal ring open on one side to expose samples to moisture.

IV.2.2.1. Top die (USG)

Fig. IV.14 gives a reminder on the capacitances implemented on USG side.



Figure IV.14: Comb capacitance implemented in USG side (top die)



Fig. IV.15 shows the capacitance variations observed after each storage (n is the number of samples).



For top dies with USG as dielectric, almost no variations are observed no matter the storage performed, even after several months at 85°C/85% RH. The small variations are attributed to equipment drift over time or pad degradation. Hence, no moisture has reached the capacitance structures.

The I(E) curves presented in Fig. IV.16 corroborate the capacitance results. A sample with open seal ring stored 5 months at 85°C/85% RH is compared with an intact seal ring sample.



Figure IV.16: Comparison of I(E) curves between a top die with intact seal ring (reference) and a top die with open seal ring after five months at 85°C/85% RH

The curves and breakdown values after 5 months at 85/85 storage are identical with reference ones for capacitances with USG as dielectric. The same observations are true for other storage conditions.

The most plausible assumption is that moisture has not reached the comb capacitance structure yet. This is consistent with the diffusion coefficient, around 10^{-15} cm²/s, we found for USG in Chapter II. The formula from random walk model used in [46] gives an estimation of the diffusivity of moisture:

$$L^2 = 4Dt$$
 (IV. 1)

Considering the 220 μ m from the opening to first capacitance, it would require longer than 3 800 years for moisture to reach the first capacitance.

With the same approach, we can determine a superior limit for diffusivity in top dies based on our results. From chapter II, the coefficients for USG and SiCN are known, hence, only interfacial diffusion coefficient is unknown. No variation was observed at $220\mu m$ after 3600 hours, it leads to:

$$D_{interface} < 9 \times 10^{-12} \ cm^2/s$$

In order to validate this assumption and to observe moisture impact on capacitance with dense SiO_2 , an opening closer to capacitance structures has to be performed. We opted for a scratch made with a nanoindentation tool. Fig. IV.17 gives a description of the different indents done.



Figure IV.17: Description of the indents performed to observe moisture diffusion in top die

The thickness of the indents is already of a few microns. Hence, a minimal distance between the indents and the capacitance structures of 5 μ m was selected and the maximum is 30 μ m. The depth was adjusted with the applied force of the nanoindentation tool, a value sufficiently high to reach hybrid bonding levels was selected as shown in Fig. IV.18(a).



Figure IV.18: (a) schematic view of the depth on the indent. (b) Top view of the indent 1, 2 and 3, the indent thickness is estimated at 25 µm

The first capacitance measurements made after nanoindentation show that only the two indents distant from 25 μ m or 30 μ m still gives consistent values. We assume that indents 1, 2 and 3 damaged (< 25 μ m) comb capacitance structures due to the thickness of the indents (Fig. IV.18(b)). The sample was then placed at 85°C/85% RH.

We performed a seven months storage (~ 5 000 hours), there is still no variation for capacitance structures close to indent 4 and 5. We can apply Eq. IV.1 with these new parameters, $L = 25 \mu m$ and t = 5 000 hours. It leads to:

$$D_{interface} < 5.5 \times 10^{-14} \ cm^2/s$$

This value is close to the diffusion coefficient of USG and SiCN materials. It shows that even if moisture diffuses at the interface between SiCN and USG, then it is similar to diffusion through USG and SICN bulks. Thus, moisture diffusion is so slow that it is not a major reliability issue in those dense PECVD SiO₂ stacks.

To pursue this study, the storage is still ongoing. However, if the diffusion is in the range of 10^{-15} cm²/s, it will take many years before observing any variation. A different approach is required to perform an opening for moisture closer to the capacitance structures. FIB might be more precise in order to perform an opening only a few microns distant from the capacitances.

• Conclusions for top dies (USG)

These results show that moisture diffusion is slow in stacks with USG as dielectric. We did not observe any variation for samples with an open seal ring. Even a storage of 5 months at 85°C/85% RH, which exceeds usual standards, did not cause any electrical change. This is identical with the results obtained at hybrid bonding levels where a dense TEOS based SiO₂ is used. Both dielectrics are similar in term of composition, this shows that moisture is not a major issue because diffusion is very slow in stacks with dense PECVD SiO₂.

In the next subsection, moisture diffusion in the bottom dies with ULK as the main dielectric is investigated.

IV.2.2.2. Bottom die (ULK)



Fig. IV.19 gives a reminder on the capacitances implemented on ULK side.

Figure IV.19: Comb capacitance implemented in ULK side (bottom die)

Several samples were monitored post sawing with sawing beyond seal ring. Fig. IV.20 shows the capacitance variations for ambient storage (a) and storage at 85°C/85% RH (b). Ambient monitoring started 5 hours after sawing, which explains the initial 11% for the first points. For the 85/85 storage, the measurements done before starting the storage were also performed 5 hours post sawing. It explains the variation already up to 11% for the first points (both variations are compared to reference values prior to sawing).



Figure IV.20: Capacitance variations at ambient (a) and 85°C/85% RH (b) for bottom die with open seal ring

In both cases, the saturation values are almost reached after only 100 hours. This fast diffusion is consistent with the results observed by Lloyd on ULK stacks [68]. We also observe a difference between the capacitances depending on their position relative to the sawing path. The delay is clearly visible in the first hours and it only impacts the kinetics.

The three structures are identical, thus, after a sufficient duration, they should all saturate at similar values. This is what we observe for both storages: around 30% at ambient and 55% at 85°C/85% RH. To be more precise, there is a small difference between the three capacitance structures, the one located at 220 μ m have values slightly lower as displayed in Fig. IV.21.

This is also observed for other storages modes. We assume some desorption mechanism occur more easily for this capacitance due to its proximity with the cut. For the other capacitances, moisture is trapped by the surrounding seal ring. More investigations are required to fully understand this phenomenon. Nonetheless, the difference is small and we consider the three capacitances as one group.



Figure IV.21: Saturation values at 85°C/85% RH depending on the distance from the cut

One conclusion can be drawn from these first results. The saturation value reached at $85^{\circ}C/85\%$ RH is never obtained at ambient. This is confirmed with results in Fig. IV.22 (n is the number of samples). To simplify the results, as mentioned above, we did not differentiate the capacitances depending on their distance from the cut since they have a similar saturation value. In each case, except the $30^{\circ}C/85\%$ RH storage, we performed measurements with intervals of a few days or weeks to ensure that saturation was reached.



Figure IV.22: Capacitance saturation value post storages (storage was stopped before saturation was observed at 30°C/85% RH)

Moisture has a significant impact on capacitances with ULK as dielectric. Even at ambient, capacitance significantly increases. A clear difference is observed depending mainly on the
relative humidity levels. It is the key parameter concerning the saturation value. This is confirmed with Fig. IV.23.



Figure IV.23: Capacitance saturation value at constant relative humidity of 85% (a) and constant temperature of 85°C (b)

Only small variations exist between saturation values at constant 85% RH as displayed in Fig. IV.23(a). We also represented the value after 650 hours at 30°C/85% RH to confirm that. Even if the samples are not saturated, the value is already close to 50%. Hence, saturation value has little temperature dependence over the 30°C-95°C range. Similar findings exist for electronic packaging polymers [79], [91].

Whereas, at constant 85°C in Fig. IV.23(b), varying the relative humidity leads to significantly different saturation values. By interpolating results in Fig. IV.23(b) at 45% RH, we extract a capacitance saturation value of 31.4% at 85°C. This value is close to the one from ambient saturation in Fig. IV.22. It suggests that, at 85°C, the most appropriate storage condition to accelerate moisture saturation observed at ambient should be performed around 40-45% RH. A higher relative humidity leads to higher saturation which might lead to phenomenon that do not occur at ambient.

From Fig. IV.23(b), we can deduct the sorption type for ULK stacks. An almost linear relationship exists between the saturation value of capacitance and the relative humidity. The dielectric material permittivity, thus the capacitance, is proportional to the concentration of absorbed moisture [5]. We assume that the overall saturation value of capacitance for our structures is proportional to the concentration of absorbed moisture C_{sat} . Hence, moisture sorption in our samples seems to follow Henry's law:

$$C_{sat} = H * P_{H_2O} = H * P_{sat} * RH (IV.2)$$

Where P_{H2O} is the partial pressure of water vapor, H is the Henry's constant of solubility, P_{sat} is the saturated pressure vapor and RH is the relative humidity.

A few more points at low relative humidity levels are required to fully determine if the sorption follows Henry's law or if a dual-mode model, studied for polymers [92], [93], is more appropriate. Nonetheless, the saturation behaviors of these integrated stacks can be described with laws normally use for materials individually.

We did not study ULK in chapter II at various environmental conditions, but we assume that the Henry behavior seen here would also be observed on this layer intrinsically. To support this assumption, we refer to the explanation proposed in section 1.3.5 of Chapter II. As moisture is absorbed in the free volume offered by nanopores with weak bonds, the concentration of absorbed moisture should equilibrate with the concentration of moisture in the atmosphere. Thus, a higher relative humidity should translate into a higher absorption of ULK layers (almost linear depending on the potential dangling bonds of the layers).

The second aspect of moisture sorption concerns the kinetics. Due to experimental limitations, we only investigated the kinetics for 30°C/85% RH and 85°C/85% RH storage conditions. Their comparison is presented in Fig. IV.24. The first points at already 30% capacitance variation are due to waiting time at ambient before starting storages.



Figure IV.24: Relative capacitance variation for the capacitance located at 220 μm from the cut at 30°C or 85°C with 85% RH

The saturation is not reached at 30°C/85% RH after almost 700 hours while it is already reached at 85°C/85% RH after around 400 hours. Thus, as expected, a higher temperature leads to a faster diffusion of moisture. This is consistent with the fact that diffusion coefficients for each material follow an Arrhenius law at constant relative humidity. These results confirm that diffusion is accelerated by temperature and we assume that the same results are true between the ambient storage and a storage at 85°C/40-45% RH.

A preliminary conclusion can be drawn from these first results. In terms of moisture saturation, a storage performed at $85^{\circ}C/45\%$ RH is more appropriate than a storage at $85^{\circ}C/85\%$ RH to accelerate phenomenon observed at ambient conditions. The latter do accelerate moisture uptake, but the saturation value is far greater than the one obtained at ambient. This might bring failure modes that do not occur in the field.

The breakdown behavior was then studied to obtain more understanding. Samples were stored and saturated at different environmental conditions (saturation was checked with capacitance measurements before performing voltage ramp up). Then, a voltage stress test was performed until breakdown is observed. The results for three conditions are compared with reference curves from intact seal ring bottom dies in Fig. IV.25.



Figure IV.25: I(E) curves for open seal ring samples for ULK side: reference, after 550 hours at 85°C/29.5% RH, after five months at ambient and 85°C/85% RH

After five months at ambient conditions, a strong increase of the leakage is observed for electrical fields below 4 MV/cm. A decrease of the breakdown value is also observed. Yet, the overall shape of the curves remains similar to the reference ones. During capacitance study, we showed that the saturation values are close between the ambient and the 85°C/29.5 % RH storages. In the I(E) curves above, this similarity is found for breakdown values (between 6 and 7 MV/cm). The curve shapes are also similar at low fields, the main difference being a higher leakage at ambient. This would tend to confirm that 85/29.5 and ambient storages are equivalent.

In the next section, the effects of annealing up to 250°C are presented. One of these effects is to reduce the leakage at low electrical field (below 4 MV/cm). Hence, it can be assumed that the lower leakage observed at low field for the 85/29.5 can be attributed to temperature effect (85°C vs 23°C). This is also consistent with the lower saturation value for 85/29.5 observed in Fig. IV.22.

However, behavior is significantly different at 85°C/85% RH. Breakdown occurs at lower electrical fields. The I(E) curves have a different shape, it indicates that the conduction mechanism has changed. Moreover, the three capacitances (dashed red lines) presented show different slopes, hence, the dispersion of curve shapes is more important with this storage condition compared with ambient and 85°C/29.5 % RH.

For the three storage conditions, a degradation of breakdown values and an increase of leakage current was observed. These results were also observed on several low k and ULK stacks [67]–[72]. But most of these studies focused on the effects of one storage and did not compare the effects of different storages.

The same impact of storage observed on capacitance variations is found on breakdown values and curve shapes. Ambient and 85/85 storages are not equivalent. Different conduction mechanisms are suspected for the 85°C/85% RH storage compared to ambient and 85°C/29.5%

RH conditions. Therefore, it confirms that the standard 85°C/85% RH storage is not equivalent to ambient aging and a storage with RH close to ambient should be preferred to reach the same saturation values.

Of course, it does not mean that 85°C/85% RH is irrelevant, but it could help to explain the apparition of undesired failure modes in products qualifications as it is mentioned by the Standard of Japan Electronics and Information Technology Industries Association in their norm EIAJ ED-4701/100 [94].

IV.2.2.3. Preliminary conclusions

Moisture absorption in a 3D integrated stack was investigated. The seal ring was sawn on one side to let moisture diffuse in. Top dies with a dense PECVD SiO₂ show no sign of moisture uptake at distance as close as 220 μ m from the sawing. On the contrary, bottom dies with ULK as dielectric have significant variations in terms of capacitance and breakdown behavior.

Both USG and ULK are capped with SiCN of similar densities. The main difference between these two stacks lies in the density of USG and ULK. As mentioned in Chapter I, USG has a density above 2 while ULK is below 1.5. It is due to the presence of pores and of methyl groups. Hence, the bulk of ULK is sensitive to moisture absorption as shown in Chapter II, this is also consistent with literature on low-k and ULK. The interface is also obviously weakened for the same reasons. Especially with a capping containing carbon that lowers the chemical affinity.

In this section, we clarified the impact of temperature and humidity on moisture absorption. For a given failure mode, if moisture saturation value is the driving parameter then the standard 85°C/85% RH could lead to undesired phenomenon and a 85°C/40-45% RH storage is more appropriated.

In the following sections, two main questions will be investigated:

- Is moisture absorption in ULK stacks reversible?
- What are the diffusion path and main interactions between moisture and the stacks?

IV.3. Reversibility of moisture absorption

After investigating moisture absorption at various environmental conditions, we investigate the reversibility of the phenomenon after moisture absorption at ambient conditions and at 85°C/85% RH as it is one of the industry standards.

No moisture uptake was observed in top die (USG) and daisy chains at hybrid bonding levels. We also checked that no variation was observed after annealing. Hence, all the results in this section concern the bottom die (ULK) with open seal ring where electrical variations were observed.

Fig. IV.26 summarizes the procedure followed. Four distinct group of samples exist. Two of them were stored five months at ambient and the others at 85°C/85 % RH. Then, for each storage, two annealing conditions were performed. Finally, post bake behavior for the two groups annealed at 125°C was assessed. Baked samples were left at ambient and measurements were performed again after two months. The objective is to see if nonreversible modifications occur.



Figure IV.26: Procedure followed to study moisture removal

IV.3.1. Effect of thermal annealing up to 250°C

To study moisture removal, two bakes were performed on a hot plate (in situ capacitance measurements were possible). One group of samples was baked at 125°C and the other at 250°C. For each bake, equilibrium was observed (i.e. no more significant capacitance variation is observed after sufficient baking time). The results are presented in Fig. IV.27.



Figure IV.27: Effect of two baking temperatures on capacitance value for ULK samples with open seal ring post ambient or 85/85 storages

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For both storage conditions, a higher baking temperature leads to better capacitance recovery as shown in Fig. IV.27. This is consistent with results from Guo [76] on low-k organosilicate glass bulk. At 190°C, physisorbed water (α -bonded) can be removed while leaving tightly hydrogen-bonded water (β -bonded). To remove all moisture components, higher temperatures (> 400°C) are required. But such temperatures are equal or superior to materials deposition temperatures, which would significantly modify our samples.

Hence, even with bakes up to 250°C, a full recovery is not possible. Moreover, Fig. IV.27 shows that the quantity of moisture left after annealing depends on storage history of the sample. For storage at 85°/85% RH, capacitance equilibrium is clearly far above dry value. The most plausible explanation is that during 85°C/85% RH, moisture bonds much more tightly than at ambient.

IV.3.2. Post bake behavior

The second phase of this experiment was to store the two groups annealed at 125°C, at ambient conditions and to measure them again after several weeks. The objective here is to see how samples are impacted by moisture during the last ambient storage depending on their storage history.

Fig. IV.28 summarizes the capacitance values measured at each step of the procedure for the groups annealed at 125°C.





The values of the columns "Post storage 5 months" correspond to the values presented in Fig. IV.22. The following 125°C annealing does not remove all moisture as described previously and samples reach a capacitance value around 2.35 nF or 2.65 nF, depending on the previous storage mode. Fig. IV.28 shows that after two months at ambient post bakes, samples stored previously at 85°C/85% RH reach a saturation value around 3.1 nF (+ 43%). Whereas, a sample stored at ambient previously reaches a saturation value around 2.75 nF (+ 27%).

For the sample that has only been stored at ambient, moisture desorption is partially reversible as seen previously. However, moisture absorption is reversible. Indeed, the saturation obtained during the second ambient storage is back to around + 27%. We assume that a part of moisture absorption occurs with tightly linked bonds that explains that desorption up to 250°C does not lead to full recovery. The remaining bonds are α -bonds that are removed at 125°C and 250°C and can be recreated during following storages at ambient.

For the samples stored at 85/85 before annealing, moisture desorption is also partially reversible with bakes. Due to the higher energy brought by storage, stronger bonds are formed. This explains the higher capacitance values post bake. However, during the subsequent ambient storage, the saturation value reached is higher than the expected + 27%. To explain such behavior, we assume that the storage at 85/85 has modified the materials and created new paths for moisture to diffuse in and to be absorbed.

To complete and corroborate the previous results, I(E) measurements were performed. Fig. IV.29 presents respectively 250°C bake effect and post bake behavior on I(E) curves either after five months at ambient (a) or five months at 85°C/85% RH (b).



Figure IV.29: Effect of a 250°C bake and post bake behavior observed on I(E) curves for ULK samples with open seal ring: reference either after five months at ambient (a) or five months at 85° C/85% RH (b)

• Samples stored at ambient before the 250°C annealing

For samples stored five months at ambient (Fig. IV.29(a)), it is possible to recover the initial breakdown value thanks to annealing. Recovery was not systematically observed on every sample; thus, a statistical approach is required to clarify this point. But the fact that the breakdown value can be improved with annealing is consistent with results from Li [75].

The trend is clearer for curves shapes. While baking at 250°C leads to similar curve shapes compared to reference ones, the I(E) curves for samples stored two months at ambient after this 250°C bake are degraded again with high leakage current at low electric field values. They are similar to curves obtained on samples only stored five months at ambient. Hence, absorption and desorption seem to be partially reversible and materials do not seem to be irremediably modified after ambient storage.

• Samples stored at 85°C/85%RH before the 250°C annealing

For samples stored five months at 85°C/85% RH, baking at 250°C slightly improves breakdown values (Fig. IV.29(b)) but curve shape recovery is not achieved as it has been shown for ambient storage. The value measured for a sample stored two months at ambient after this bake is degraded again. This trend is similar to the trend observed on capacitances results in Fig. IV.28.

In this section, we showed that moisture absorption is partially reversible at ambient conditions. A total recovery back to the initial properties is not possible with annealing up to 250°C, but the capacitance saturation value and the breakdown value are not modified by storage followed by annealing.

The same is not true for the 85°C/85% RH storage. Once stored at these conditions, the samples are modified and the initial behaviors are never recovered with bakes. As previously, we attribute these differences between the two storage modes to irreversible material modifications that only occur at 85°C/85% RH. This question is investigated in the next sections.

IV.4. Moisture diffusion path and interactions of moisture with the stacks

In this section, we focus on the remaining questions concerning moisture diffusion in the 3D stacks. Moisture has a strong impact on bottom dies where ULK is used as dielectric material. The diffusion path and the local interactions leading to the previous electrical observations are investigated here. Tof-SIMS analysis combined with TEM EDX/EELS are performed to answer these questions.

IV.4.1. Characterization of moisture diffusion path with Tof-SIMS analysis

Due to the size of the sputter area of ToF-SIMS (greater than the dimensions involved in the 3D stacks), it is not possible to directly use this technique on the dies (copper density would be a major issue). Hence, the dielectric stacks with USG and ULK were reproduced separately at wafer level. Only the dielectric materials were deposited as shown in Fig. IV.30.

The objective is to find the main diffusion path for moisture. Based on literature, it is likely that diffusion occurs first in dielectric materials or at their interfaces [20], [40]. Hence, the role of copper and TaNTa barriers in moisture absorption will be investigated in a second study by means of TEM EDX/EELS techniques.

The dielectric stacks were reproduced on two silicon substrates as shown in Fig. IV.30. To reproduce the lateral diffusion happening in 3D stacks, 600 nm of hermetic SiN are deposited on top of them to protect from any moisture absorption coming from the top side.



Figure IV.30: Stacks used for Tof-SIMS analysis

Dielectrics depositions were performed on a 300mm silicon substrates. The wafers were then cut into samples of 2 by 3 cm². Samples were stored at 85°C/85% RH from 1 hour to 215 hours for ULK side and from 1 hour to 1100 hours for USG side. The Tof-SIMS sputter area was always performed at the same location on each sample (1 mm from the edge).

Fig. IV.31 shows the oxygen profiles as a function of depth for USG samples. The first 600 nm of SiN are not represented because this layer was only deposited to prevent from moisture uptake coming from top side (SiN hermiticity is presented in Appendix B). Hydrogen profiles are not represented, no variation was observed between the different samples.



Figure IV.31: Oxygen profiles in SiN/SiCN/USG/SiCN stacks after 1100h storage at 85°C/85% RH

No variation is observed between reference and the samples stored for 1100 hours at 85°C/85% RH. If moisture was present, it should be visible in SiCN layers or at the SiCN/USG interface. The sputter area is located at 1 mm from the edge. This distance is similar to the distance between the comb capacitance structures and the sawing path (Fig. IV.10). This corroborates the previous electrical results. Moisture does not reach the comb capacitance structures located in USG.

However, the question of the diffusion path is unanswered because no moisture was detected. Further analyses are required to determine the diffusion path in SiCN/USG/SiCN. It is still consistent with the diffusion coefficients of each materials presented in Chapter II.

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Fig. IV.32 shows the oxygen profiles as a function of depth for six samples of SiN/SiCN/ULK/SiCN: one as-deposited reference and five samples stored from 1 hour to 215 hours at 85°C/85% RH. Again, the first 600 nm of SiN are not represented because this layer was only deposited to protect from moisture absorption from top side.

Since oxygen is not used for SiCN deposition, the concentration is very low in the two SiCN layers for the reference sample. With increased storage time, the oxygen concentration shows a significant variation. A very distinct and symmetrical gradient is observable through SiCN layers thickness. A higher concentration is present near the SiCN/ULK interface. A concentration increase can also be observed at the top and bottom of the ULK layer.

Two assumptions could explain this phenomenon:

- Fast diffusion through interconnected pores in the ULK layer then diffusion toward SiCN layers.

- Fast diffusion at the SiCN/ULK interfaces then diffusion into SiCN and top/bottom of ULK.

However, no oxygen concentration increase is observed in ULK bulk. Thus, the second hypothesis seems to be more plausible with the present results.



Figure IV.32: Oxygen profiles in SiCN/ULK/SiCN stacks after storage at 85°C/85% RH for various storage durations

The second hypothesis is also in agreement with results from Lin [36] who showed that diffusion occurs first at the Si/Organosilicate glass (similar to ULK) then diffuses inside the porous oxide.

These results at blanket level are consistent with the electrical observations on 3D integrated stacks. For dense SiO_2 stacks, they confirm the very slow moisture diffusion. Even if the duration of the storage performed exceeds the usual qualification standards that are recommended, we showed that moisture diffusion is not a major issue in that case.

However, for SiOC:H stacks, moisture has strong impacts. The diffusion occurs very quickly and interfaces between SiCN and ULK are the most plausible diffusion paths. Based on these results, the diffusion mechanism can be divided in two steps:

- Fast diffusion at interface between SiCN and ULK.
- Diffusion in the adjacent layers according to the diffusion parameters determined in Chapter II.

This assumption will be tested with numerical simulation in section 5 of this chapter. In the next part, we focus on the interactions between moisture and the 3D stacks. Once moisture has diffused at the interface and in dielectric materials, what phenomenon can be observed and what are the differences between ambient storage and 85°C/85% RH?

IV.4.2. Interactions of moisture with 3D stack determined with TEM EDX/EELS

The comb capacitances implemented on ULK side are strongly impacted by moisture as shown with electrical results. To observe moisture impact in these structures we performed a TEM combined with EDX and EELS analyses. In the case studied, it allows to observe each chemical element except hydrogen. The entire lamella is presented in Fig. IV.33(a). Thanks to the precision of the probe, it is possible to map the area between two copper vias. Two similar mappings were performed to confirm the results. They are showed in Fig. IV.33(b). Only results for mapping 1 are presented in this subsection. Results for mapping 2 can be found in Appendix 3.



Figure IV.33: TEM view of 3D stack (a) with a focus on ULK levels (b). Mappings 1 and 2 correspond to the areas analyzed with EDX or EELS

Two series of analyses were performed separately:

- 1st series: Two lamellas were produced. One is from a die with an intact seal ring, hence there is no moisture in ULK levels. The second lamella comes from a die with open seal ring saturated at 85°C/85% RH.
- **2nd series:** Two lamellas were produced. One from an intact seal ring die and a second one from a sample with open seal ring saturated at **ambient conditions**.

Prior to sample preparation, the presence or absence of moisture was confirmed with capacitance measurements for both samples. It is also important to underline that none of the sample had voltage breakdown tests, no electrical fields were applied on them (capacitance are measured at 0V).

A schematic view of mapping 1 is given in Fig.IV.34. Two chemical profiles were performed:

- **Chemical profile 1:** vertical probing to investigate ULK/SiCN interface and to confirm the presence of oxygen in SiCN that was observed with Tof-SIMS analysis.
- **Chemical profile 2:** horizontal probing to study the presence of oxygen at Cu/TaNTa/ULK interfaces.



Figure IV.34: Schematic view of mapping 1 in Fig. IV.33

• Investigation of oxygen presence in SiCN layers

Fig. IV.35 shows the chemical profiles with the EDX mapping of oxygen for each type of sample. Only one of the two reference samples is presented.



Figure IV.35: Chemical profiles 1 as described in Fig. IV.34 and EDX mapping of oxygen of a reference sample ((a),(d)) and samples saturated at ambient ((b),(e)) and at $85^{\circ}C/85\%$ RH ((c),(f))

A small amount of oxygen is present in SiCN for samples stored at ambient and 85°C/85% RH as shown with EDX mapping for oxygen ((e) and (f)). The amount of oxygen is only around 3-4% and chemical profiles would not be enough alone to conclude on the presence of oxygen. However, it is not possible to conclude anything for other elements.

To confirm the presence of oxygen, an EELS analysis was performed on a reference lamella and the lamella stored at ambient conditions. First, three areas were scanned on the sample saturated at ambient to obtain the characteristic curves of SiCN, SiOC and SiO bonds. The SiO area corresponds to a layer called initiation layer with a thickness of a few nanometers; its purpose is to improve adhesion between porous SiOC:H bulk and SiCN.



Figure IV.36: EELS calibration of SiO, SiOC and SiCN curves

Then the SiCN curves were compared between reference and saturated samples as displayed in Fig. IV.37.



Figure IV.37: SiCN curves obtained with EELS analysis for reference and ambient saturated samples

A small peak is present around 107 eV for the sample saturated at ambient, this peak is present for SiOC and SiO curves in Fig. IV.36. Hence, some SiO bonds exist in the saturated SiCN.

All the evidence gathered together show that oxygen diffuse and bond to the SiCN layers in the 3D integrated stacks both at ambient and at 85°C/85% RH. This is consistent with the results at wafer levels both in the previous subsection and in Chapter II where we studied moisture diffusion in SiCN deposited on silicon substrate.

In Chapter II, we studied the diffusion behavior in SiCN layers and showed that moisture bonds strongly with SiCN even in the first hours of diffusion. This is to be put in relation with these results and the results from Fig. IV.27. Indeed, after annealing up to 250°C, the capacitance values remain higher than the initial ones. A part of this remaining moisture in 3D stacks is certainly located in SiCN layers. This would explain why it is not possible to obtain a full capacitance recovery.

From Chapter II, we also showed most of the moisture uptake in ULK layers can be removed, hence these behavior at wafer level help to explain moisture desorption in ULK stacks as shown in Fig. IV.38.

- Moisture removed at 125°C or 250°C is mainly located in ULK layers and consist of weak bonds (α-bonds).
- Remaining moisture is mainly bonded to SiCN layers with β -bonds. A part of this remaining moisture could also be located in ULK and TaNTa barrier.



Figure IV.38: Schematic of the main components responsible during moisture desorption in ULK stacks

It was not possible with these results to highlight the presence of moisture in ULK layers. Two reasons might explain it:

- ULK is composed of oxygen and hydrogen and variations caused by moisture are too small compared to these initial amounts.
- Tof-SIMS and TEM EDX/EELS analyses are performed under vacuum. Hence, weakly bonded moisture could be removed with this pressure gradient.

For the first hypothesis, one perspective is to replace water vapor with an isotope that is not present initially in the layer. Heavy water D_2O can be used as a tracer and combined with Tof-SIMS as several authors showed [5], [19]–[22]. The natural ratio between H₂ and D₂ is around 500, thus, D₂ increase in ULK layers can be easily followed.

The second hypothesis is investigated in one of the following sections. Table IV.2 gives a summary of the results for the chemical profile 1.

-	Ambient	85°C/85% RH	
Main results	Small increase of oxygen concentration in SiCN layers	Increase of oxygen concentration in SiCN layers	
Conclusions	 From TEM-EDX, no fundamental differences were found between the two storage modes for moisture absorption in dielectric layers Oxygen increase in SiCN is consistent with wafer level studies (Tof-SIMS and Chapter II). The strong bonds between moisture and SiCN explain that no full recovery is possible for capacitance in 3D stacks up to 250°C. 		
Perspectives	Presence of moisture in ULK layers to	be highlighted in 3D integrated stacks	

Table IV.2: Summary for chemical profile 1

• Investigation of oxygen presence in Cu/TaNTa/ULK interfaces

For the second chemical profile, the focus is put on copper and TaNTa barriers. Fig. IV.39 shows the EDX mapping of copper for each type of samples.



Figure IV.39: EDX mapping for copper for the three types of samples (color difference is due to the two analysis being performed separately)

Copper diffusion is only observed in the case of the 85°C/85% RH storage. This was also observed on the second mapping in Appendix 3. Copper diffusion was never observed for reference and ambient saturated samples. This indicates that copper is transported from vias/metal lines, through TaNTa barriers, into ULK bulk at 85/85.

Fig. IV.40 gives the chemical profile 2, as described in Fig. IV.34, and the associated EDX mapping of oxygen. The dashed black lines in the chemical profiles were placed at the depth corresponding to the peak for tantalum. They visually help to compare the oxygen concentrations at these locations. The dashed red lines in the EDX mapping correspond to the TaNTa barrier (they were superposed from the Ta profiles).



Figure IV.40: Chemical profiles as described in Fig. IV.31 and EDX mapping of oxygen of a reference sample ((a),(d)) and samples saturated at ambient ((b),(f)) and at $85^{\circ}C/85\%$ RH ((c),(e))

The chemical profiles for samples saturated at ambient and 85°C/85% RH (Fig. IV.40(b) and (c)) show a clear overlapping of the tantalum peaks by oxygen. This is not the case for the reference samples (a) where the concentration in oxygen is very low in TaNTa barrier. This is

confirmed with the EDX mapping of oxygen ((e) and (f)). Concentration gradients are visible in the TaNTa barriers except for reference samples.

The presence of copper is confirmed again for the 85°C/85% RH saturated sample in Fig. IV.40(c). Two small peaks are present and are consistent with the mapping in Fig. IV.39.

This second part of the TEM EDX analysis brings a fundamental difference between the ambient and 85°C/85% RH storage. Copper is present in the bulk of ULK layers in the latter case. In previous sections, we showed a difference in the breakdown behavior depending on the storage mode. Only ambient storage could be partially reversible with annealing (Fig. IV.29).

We propose the following explanation. After diffusing at interfaces between SiCN and ULK, moisture is absorbed in adjacent layers including TaNTa barriers. The barrier is oxidized and its initial role as a copper diffusion barrier is lowered. Ito and al. showed that Ta is easily oxidized to Ta_2O_5 and does not stop Cu diffusion anymore once oxygen is present [95]. They also showed that TaN thickness is reduced in presence of oxygen, but it still acts as a Cu diffusion barrier. However, they worked on 20 nm thick layers which is higher than barrier layers in our structures as shown in EDX mapping in Fig. IV.40. Hence, in our samples, the TaN part is reduced drastically, and the Ta part is oxidized so copper can diffuse through. A mechanism to explain the diminution of copper barrier role in Ta_2O_5 was proposed by Xiao and Watanabe [96]. H₂O molecules fill the empty space in Ta_2O_5 which are normally trapping copper ions. Hence, the presence of moisture weakens the copper barrier role of Ta_2O_5 . Their explanation from first-principles simulations fit with our experimental results.

Moisture oxidizes the TaNTa barrier, lowering its copper barrier properties, and then reaches the TaNTa/copper interface. Several mechanisms of copper transport exist. The first one is thermal diffusion of copper atoms in dielectric but it requires elevated temperatures [97]. The second mechanism is the drift of copper ions. Ions are generated when a metal oxide is formed. The driving force for the ions to drift in the dielectric is the application of an electrical field. Willis and Lang stated that only this mechanism is active for temperature lower than 450°C-500°C and electrical fields lower than 1 MV/cm for dense SiO₂ [98] but they note that thermal diffusion might need to be considered for porous dielectric layers.

For our samples, no electrical field was applied and the temperature is only up to 85° C. The presence of humidity (85% RH) and the duration of the storage could however help to explain the transport of copper. Due to the presence of moisture, it is plausible that a copper oxide is formed at the TaNTa/Cu interface. This would support the ions drift mechanism. This would also suppose that the H₂O molecules dissociate or that H⁺ and OH⁻ are already present in the diffusing moisture in order to oxidize copper. The reactions involved are [14], [99]:

$$2Cu + \frac{1}{2}O_2 \rightarrow Cu_2O \quad Cu_2O + \frac{1}{2}O_2 \rightarrow 2CuO$$
$$Cu + 2OH^- \rightarrow Cu(OH)_2 + e^- \quad Cu(OH)_2 \rightarrow CuO + H_2O$$

Once formed, the copper oxide plays the role of a source for copper ions to diffuse back into the dielectric, mostly under the form of $Cu^+[14]$.

Even though some elements match with literature, it is not possible to fully confirm the transport mechanism of copper in our sample based on the present results. Moreover, the presence of molecular or ionic moisture is not clarified. Hence, further investigations are still required to explain the driving force of the copper drift and confirm the proposed mechanism of transport.

The diffusion mechanism of copper inside the ULK layers also needs to be investigated. Rogojevic and al. showed that two transfer path need to be considered: the bulk and the surface of the pores [13]. Numerical simulations could be performed to answer the question for our samples.

Another interesting result from literature is the enhanced copper diffusion into sintered xerogel (organic capping groups removed). This can be related to our stacks. In Fig. IV.40, a detailed description of ULK layers is given. During process integration, ULK layers undergo material modifications on their sides due to the etching steps. Several nanometers are then depleted in organic groups and become hydrophilic. This is represented with the two lateral bands of plasma modified ULK in Fig. IV.41. Their thickness is not known precisely and is only estimated in the figure. The central area corresponds to unmodified hydrophobic ULK. The presence of a thin layer of SiO_2 between SICN and the bulk of ULK was discussed in previous section.



Figure IV.41: Detailed structure of ULK layers to explain copper transport

Copper does not diffuse over the entire ULK, its presence is restricted to lateral bands with a thickness around 25 nm. This is in good agreement with results on sintered xerogels. Indeed, the authors did not observe copper diffusion in xerogels with organic groups that corresponds to the bulk of ULK in our samples. Their observations help to explain the final location of

copper in ULK layers. Andsager also observed a diffusion coefficient of copper in porous silicon seven times smaller than in dense silicon [100].

Once copper has diffused in ULK layers it creates a preferential breakdown path. In ionic form, it also creates a charge build-up that causes a leakage increase. Annealing at 250°C in ambient atmosphere should only trigger molecular diffusion, a concentration gradient driven mechanism. Hence, copper should not diffuse out of ULK and the preferential path for breakdown remains present even when an annealing at 250°C is performed. This explains why no recovery was observed for the breakdown behavior.

Concerning ambient conditions, there is no copper diffusion. Thus, the increased leakage is only caused by the moisture present in dielectric materials. Annealing at 250°C removes the weakly bonded moisture that is mostly present in ULK. This process helps to recover the initial breakdown behavior observed on reference samples. Table IV.3 gives a summary of the results for the chemical profile 2.

	Tuble I (10) bullinally for enemical profile 2				
	Ambient	85°C/85% RH			
Main results	Oxygen increase in TaNTa	Oxygen increase in TaNTa Copper diffusion in ULK			
Conclusions	 Copper diffusion in ULK is only obs This fundamental difference behavior. Copper in ULK breakdown path Mostly weakly bonded is annealing removes it and breakdown behavior 	erved at 85°C/85% RH. ce explains the different breakdown creates a preferential and irreversible absorbed at ambient in ULK layers, explain the partial reversibility for			
Perspectives	Is moisture diffusing under molecula What is copper transport mode and w What is the kinetic of copper diffusio	r or ionic form mainly? vhat bonds does it form in ULK? on at 85°C/85% RH?			

Table	IV 3.	Summary	for	chemical	profile 2
rable	10.5	Summary	101	chemical	prome 2

IV.4.3. Limitations and perspectives

The previous Tof-SIMS and TEM EDX analyses give important results to understand moisture diffusion. However, these analyses need to be performed under vacuum. For Tof-SIMS, samples are stored under vacuum for several hours before analysis. For EDX analysis, the time under vacuum is shorter but the lamella is ultra-thin (~80 nm) and directly exposed to vacuum effects. Hence, it is important to assess vacuum effect.

One die with voluntarily damaged seal ring was saturated at ambient conditions and then stored under vacuum for 20 hours. Capacitance measurements were performed before and after storage to assess the impact of vacuum as shown in Fig. IV.42.



Figure IV.42: Effect of vacuum on 3D integrated stack

The comb capacitance located at 220 μ m from the cut is impacted by vacuum. The effect decreases from structures further from the cut.

These results show that part of the absorbed moisture is removed by vacuum during Tof-SIMS and EDX analysis. This could explain why no oxygen increase is seen in ULK layer. We discussed its absorption and desorption at wafer level in Chapter II. The assumption is that moisture is stored in pores with little bonding to the bulk. Hence, vacuum probably removes some of the moisture stored in ULK.

One experiment could potentially solve this desorption issue. Prior to put the samples under vacuum, it would be interesting to decrease the temperature below 0° C and then to apply vacuum. We believe that decreasing the temperature could prevent from moisture desorption by lowering its mobility.

In addition, instead of using water vapor, it would be easier to draw conclusions with a chemical element easy to follow with Tof-SIMS. Deuterated water D_2O is the perfect candidate for that experiment.

IV.5. 2D numerical simulations of moisture diffusion in integrated stacks

In order to validate the diffusion path highlighted in the previous sections, we choose to perform 2D numerical simulations.

The simulations are based on the material intrinsic parameters found in Chapter II and they include the non-Fickian behavior of SiCN layers. The previous physical analyses are also used to determine key geometrical parameters.

First, we describe the method and hypotheses used. Then, three simulations are tested:

- A simulation with interfaces between SiCN and ULK layers proposed thanks to the experimental results. The diffusion parameters of the interface are determined with the numerical simulations
- A second simulation without the interface between SiCN and ULK layers. It only uses the diffusion parameters of each material from Chapter II.
- A third simulation to test a hypothesis from the literature. Several authors proposed very high diffusion coefficients for porous SIOC:H (without mentioning any interfaces). Thus, we removed interfaces and determined if a high diffusion coefficient for ULK can fit experimental data.

Finally, some perspectives to improve these numerical simulations are proposed and discussed.

IV.5.1. Methodology and models

IV.5.1.1. Modelling and thermal analogy

We briefly introduced several key concepts in section 1.3 of Chapter III. As a reminder, the wetness fraction w(t) is defined as:

$$w(t) = \frac{C(t)}{C_{sat}} \quad (IV.3)$$

Where C represents the moisture concentration and C_{sat} is the saturated moisture concentration. It allows us to perform simulations for complex stacks with materials having their own diffusion parameters.

The Finite elements (FE) numerical simulations are all performed with Comsol Multiphysics 5.4 ©. Due to the similarities between moisture diffusion and thermal diffusion, we used the thermal module implemented in Comsol ("*Heat Transfer in Solid*"). The analogies are presented in Table IV.4:

-	Thermal diffusion	Moisture diffusion
Variable	Temperature [°C]	Wetness, w(t)
Density	ρ [kg/m ³]	1
Conductivity	k [W/m.°C]	D*C _{sat} [mg/(mm.s)]
Specific capacity	c _p	C _{sat} [mg/mm ³]

Table IV.4: Thermal analogy between moisture diffusion and thermal diffusion

As we found in Chapter II, the SiCN layers have a non-Fickian behavior. The dual stage model proposed by Placette [33] describes the experimental behavior accurately for these films.

This model proposes to describe moisture concentration C with two superposed Fickian phenomenon C_1 and C_2 :

$$C(x, y, z, t) = C_1(x, y, z, t) + C_2(x, y, z, t)$$
 (IV. 4)

This equation is perfectly adapted for numerical simulation. It is possible to apply two separated modules on a given material with COMSOL[©]. The modulus "*Heat Transfer in Solid*" solves the equation:

$$\frac{\partial C_1}{\partial t} = D\Delta C_1 \quad (\text{IV. 5})$$

Then, it is possible to apply a second module "Heat Transfer in Solid" on a material that solves:

$$\frac{\partial C_2}{\partial t} = D\Delta C_2 \quad (IV.6)$$

The last step is to superpose the results given by these two modules in order to obtain the full non-Fickian behavior of SiCN layers.

IV.5.1.2. Objective

Our objective is to simulate moisture diffusion in the 3D integrated stacks. As we only observed moisture diffusion in the ULK levels of the bottom die, we focus on this side for FE simulations.

In Chapter II, we gathered diffusion parameters for all dielectrics at 85°C/85% RH. Hence, the experimental data used to validate the numerical simulations are the ones obtained during a storage at 85°C/85% RH. Prior to that storage, a 250°C annealing was performed to remove moisture absorbed at ambient conditions. The experimental capacitance variations are presented in Fig. IV.43:





The experimental data in Fig. IV.43 corresponds to the capacitance structures of the bottom die (ULK as the main dielectric material) presented in Fig. IV.44.

The 2D simulation is based on the schematic presented in Fig. IV.44:



Figure IV.44: Schematic top view to illustrate the axis used for numerical simulation

The 2D simulation corresponds to the cross section illustrated in the simplified schematic in Fig. IV.45.



Figure IV.45: Cross section corresponding to the red dashed line in Fig. IV.44

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We assume that moisture absorption is homogeneous in the three capacitance structures on the left along the x axis. This is plausible because the sawing is performed equally along the x axis, hence, moisture diffusion should be the same all along this axis, we assume that edge effects are negligible for these three capacitances.

The real stacks are far more complex than the representations in Fig. IV.44 and IV.45. Due to design rules, there are inactive copper vias and lines between the capacitance structures to obtain a homogeneous copper density all over the die.

Moreover, depending where we place the cross section over the x axis, the copper density differs as it can be along comb finger or between two comb fingers (Fig. IV.44).

The distance between comb fingers and their width is around 60 nm while the distance along the y axis is around 2 mm. It would require an important calculus power to obtain a correct meshing. Thus, in the following models, we only considered dielectric materials and we did not represent the copper (and TaNTa barriers) inside the die.

• Model 1: Interfaces between SiCN and ULK

This first model includes an interface between SiCN and ULK layers. Its objective is to confirm the results obtained with Tof-SIMS analysis in the previous section.

The interface thickness is determined from TEM EDX analysis. It is presented in Fig. IV.46. It corresponds to the chemical profile 1 in Fig. IV.34.



Figure IV.46: Determination of the thickness of the interface between SiCN and ULK

We consider that the interface between ULK and SiCN is the area were the chemical elements gradually increase or decrease to obtain ULK or SiCN composition. The resulting thickness is 8 nm. Similar thickness was found on other samples.

Fig. IV.47 illustrates the 2D model:



Figure IV.47: First numerical model with interfaces between ULK and SiCN layers

To reduce to meshing and calculus resources we only represent half of the stack and use a symmetry to model the entire structure.

The lateral thermal insulation represents the metal seal ring as this one completely blocks moisture diffusion. We simplified the model by putting a thermal insulation at the bottom of the model. As it can be seen in Fig. IV.45, moisture can diffuse below capacitance structures. We consider this diffusion as negligible and we did not represent these additional layers to lower the number of layers to simulate.

To monitor moisture diffusion in the capacitances during FE simulation, the three areas represented in Fig. IV.47 were integrated over time (with the native "intop" function in COMSOL ©). These integrations over time give the total amount of moisture absorbed in the corresponding area.

To compare with the capacitance relative variations, all values were normalized between 0 and 1 by dividing by their saturation value.

• Model 2: No interface between SiCN and ULK and diffusion parameters from Chapter II

In this second model, the interface between SiCN and ULK was removed and the diffusion parameters are the ones determined in Chapter II.

The objective of this model is to confirm that moisture does not reach the capacitance with these hypotheses. The model is illustrated in Fig IV.48:



Figure IV.48: Second numerical model without interfaces between ULK and SiCN layers and with diffusion parameters from Chapter II

• Model 3: No interface between SiCN and ULK and fast diffusion in the ULK layers

In this third model, we investigate the assumption found in the literature that a fast diffusion can occur in the ULK layers thanks to a high moisture diffusion coefficient (Section 1.2 in Chapter III). The model is identical to the one shown in Fig. IV.48, only the diffusion coefficient of ULK differs. For this model, the approach is to determine the diffusion coefficient of ULK that gives the best fit of experimental data.

IV.5.2. Results

All the necessary parameters for the simulations are gathered in Table IV.5:

			Model 1	Model 2	Model 3
Fixed	Diffusion coefficient [cm²/s]	ULK	2.6×10^{-15}	$2.6 imes 10^{-15}$	2×10^{-7}
		SiCN (Dual stage model)	$5.2 imes 10^{-14}$	$5.2 imes 10^{-14}$	5.2×10^{-14}
			4.7×10^{-18}	$4.7 imes 10^{-18}$	4.7×10^{-18}
	Saturated moisture concentration [mg/mm ³]	ULK	109.8	109.8	109.8
		SiCN	17.9	17.9	17.9
		(Dual stage model)	58.1	58.1	58.1
	Thickness [nm]	ULK	222	222	222
		SiCN	32	32	32
		Interface	8	No interface	No interface
Free	Diffusion coefficient [cm ² /s]	Interface	3×10^{-5}	No interface	No interface
	Saturated moisture concentration [mg/mm ³]	Interface	(109.8 + 17.9 + 58.1) / 2	No interface	No interface

Table IV.5: Numerical simulation parameters

Only the interface diffusion parameters are unknown. We cannot determine the saturated moisture concentration of the interface without the dielectric constant of each layer. As mentioned in Chapter II, this characterization was aborted due to logistical issues. Hence, we fixed the saturated moisture concentration as the average between the C_{sat} of ULK and SiCN.

The diffusion coefficient of the interface was obtained iteratively until the best fit with the experimental data was obtained (Fig IV.49). For the third simulation, the diffusion coefficient of ULK was also determined iteratively.



IV.5.2.1. Interfaces between SiCN and ULK

The fitting obtained with numerical simulations is presented in Fig. IV.49.

Figure IV.49: Normalized capacitance variations with the associated FE simulations with model 1

Considering the simplifications made compared to the real stack, the fitting is consistent with the experimental data, especially in the first hours. It validates the interfacial diffusion shown with the Tof-SIMS experiments in previous section.

With this simulation, the capacitance variations are overestimated in the area highlighted in red in Fig. IV.49. However, the difference is less than 10%, which again is correct considering the simplifications. We assume that the slower diffusion is due to the presence of copper vias and lines that act as an obstacle to moisture diffusion. This was shown by Weide-Zaage in printed circuit boards [101].

Thanks to the numerical simulations, the diffusion coefficient of the interface between SiCN and ULK was found. The value of 3×10^{-5} cm².s⁻¹ is consistent with the values around $10^{-6} - 10^{-7}$ cm².s⁻¹ found by Lin for the interface between organosilicate glass (OSG) and silicon substrate [20].

IV.5.2.2. Model 2 without interface & standard D

In this model, the interface between SiCN and ULK was removed and only the diffusion parameters determined in Chapter II were implemented. The result is straightforward, after 200 hours, moisture has only diffused over $1.5 \,\mu m$ as it is shown in Fig. IV.50.



Figure IV.50: Normalized moisture concentration after 2 and 200 hours with model 2

The resulting plot fitting experimental data is given in Fig IV.51:



Figure IV.51: Normalized capacitance variations with the associated FE simulations with model 2

There is no capacitance variation with this model, while significant variations are measured experimentally. Thus, there is no surprise with this model and the diffusion parameters determined for each layer in Chapter II are not enough to explain moisture diffusion in the ULK stacks measured experimentally.

IV.5.2.3. Model 3 without interface and high D for ULK

This last model was tested to verify one assumption found in the literature. Several authors reported high diffusion coefficient for porous dielectric layers as we discussed in the first section of Chapter III. Thus, we found iteratively a diffusion coefficient for ULK that gives a good fit for capacitance 1. The results are presented in Fig. IV.53.



Figure IV.52: Normalized capacitance variations with the associated FE simulations with model 3

We obtained a diffusion coefficient of 2×10^{-7} cm².s⁻¹ for ULK. It can correctly fit the experimental data for capacitance 1. However, the experimental data of capacitance 2 and 3 cannot be fitted with this model. As one can see with the red arrow in Fig. IV.53, the first hours are underestimated of almost 50%. This shows that the diffusion with this model is far slower than the real diffusion process.

If we increase D_{ULK} to fit correctly the capacitance 2 or 3, the fit will not be correct for capacitance 1 obviously. Hence, we conclude that the assumption of a high diffusion for ULK is incorrect in our case.

To confirm that, we perform quick study based on the least square residuals method. We gathered the least square residuals for models 1 and 3 in Table 6. The least square residual is given by:

$$R = \sum \left(C_{\%,exp}(t) - C_{\%,COMSOL}(t) \right)^2$$

Where $C_{\%,exp}$ stands for the normalized experimental capacitance variations and $C_{\%,COMSOL}$ represents the normalized capacitance variations obtained with numerical simulations.

	Least square residual R			
	Capacitance 1 220 µm from sawing	Capacitance 2 800 µm from sawing	Capacitance 3 1370 µm from sawing	
Model 1	0.03	0.03	0.05	
Model 3	0.02	0.25	0.29	

Table IV.6: Least square residuals for models 1 and 3

The results presented in Table IV.6 confirms that model 1 is better than model 3 to fit the experimental data. This confirms that diffusion occurs at the interface between SiCN/ULK.

IV.5.3. Conclusion and perspectives

The previous simulations confirmed the experimental results: the main diffusion path is the interface between SiCN and ULK. It also gave us a value for the diffusion coefficient that would be challenging to obtain experimentally (the method used by Xu is a possibility [25]).

However, we did not obtain the saturated moisture concentration of the interface and we only assumed the value for the previous simulations. In order to obtain the real value, it is necessary to link the capacitance variations (electrical measurements) to the moisture concentration in the stack (simulation results). As we already have the mass measurements for each dielectric material at 85°C/85% RH, there is only one missing link: the dielectric constant of each layer.

With this additional parameter, it is possible to build a model that links moisture concentration in the stack to the capacitance variations and to determine the saturated moisture concentration of the interface.

The second main improvement concerns the evolution to 3D models. Indeed, the previous models are greatly simplified compared to real integrated stacks. We do not believe that the effect of copper can be properly simulated in 2D. With the cross sections along the x axis (Fig. IV.44), copper density varies depending if the cross section is positioned along a capacitance finger or between two fingers. With a 2D top view, it would only be possible to consider one material and the diffusion from interfaces to ULK or SiCN layers would be lost.

Hence, 3D simulations are required to simulate the effect of copper vias and line on moisture diffusion. The main challenge for these simulations is to find an appropriate meshing, considering that:

- The interface thickness is 8 nm
- The distance from the sawing to the seal ring (y axis in Fig. IV.44) is 2.2 mm
- If we only consider the three capacitance structures on the left side, the lateral dimension along the x axis is 5.5 mm

Thus, the highest aspect ratio is found at the interface between the z and x axis: 687 500. This makes the meshing of these areas very challenging if the interfaces are represented in 3D. A potential solution would be to use shell elements for interfaces. They are 2D elements that take into account a thickness during the FE calculations. This simplifies the calculations and lower the computational power required. The impact of using shell elements instead of complete 3D would need to be assessed too.

IV.6. Mechanism of moisture diffusion in ULK stacks

Finally, based on the experimental results and the numerical simulations, we propose a global mechanism of moisture diffusion in ULK stacks for ambient and 85°C/85% RH storages. The diffusion/reaction mechanism of water in silica glass was described by Doremus [102]. At high temperatures (> 700°C), the following reaction between H₂O and silica glass occurs:

$$Si - O - Si + H_2O \rightarrow 2SiOH$$

The reaction is fast and dominates water diffusion. In our case, at low temperatures, the reaction does not occur and diffusion of molecular water dominates the mechanism [103]. This justifies the choice of modeling only diffusion in numerical simulations.

We propose the following steps to explain moisture diffusion in ULK stacks:

- 1. The surface concentration of water molecules reaches an equilibrium with water molecules present in the storage chamber. In our case it corresponds to the edge of our samples where sawing was performed. Then, moisture diffuse into our samples.
- 2. The main diffusion path identified is the SiCN/ULK interfaces present at several metal levels. By means of TEM, a thickness of 8 nm is attributed to these interfaces. The numerical simulations fitting experimental data lead to a diffusion coefficient around 3×10^{-5} cm²/s.
- 3. The subsequent diffusion occurs in adjacent layers according to diffusion parameters determined in Chapter II for materials bulk. The exact diffusion parameters of materials, once they are integrated in stacks, might differ due to the different process steps (such as etching, plasma, etc). Nonetheless, the order of magnitude is assumed to be similar to 10^{-14} - 10^{-15} cm².s⁻¹ and thus, far smaller than 10^{-5} cm²/s.
- 4. The diffusing moisture oxidizes the TaNTa barrier and it lowers its copper barrier efficiency.
- 5. At 85°C/85% RH, the most plausible mechanisms, is the creation of copper oxides at the TaNTa/Cu interface. These layers serve as a source for copper ions (Cu⁺ mainly) that are transported into the ULK layers. The copper is mainly located in ULK areas that were damaged during integration causing the depletion in organic groups.

The four first steps are common between the moisture diffusion mechanism at ambient and at 85°C/85% RH. However, at ambient, the diffusion of copper is not observed. Due to the uncertainty on the copper transport mechanism, further investigations are required to identify the limiting step at ambient.

The entire moisture diffusion mechanism presented above fits the electrical measurements and the physical and chemical analyses both at wafer level and on 3D stacks. Numerical simulations helped to confirm the step 1 and 2 of the mechanism.

IV.7. Conclusions

In this chapter, the diffusion of moisture in 3D integrated stacks was investigated experimentally and with numerical simulations.

The stacks were assessed under stress conditions exceeding the usual standards. No major issue was detected at hybrid bonding levels and the overall reliability of the stacks in BEOL levels was not affected. Hence, moisture diffusion is not a reliability issue for the current architecture of the seal ring (despite its discontinuity at hybrid bonding levels).

However, when seal ring was fully sawn on one side of the structures, top dies (USG) and bottom dies (ULK) behave differently. For the top dies, no variation was measured even after several months at 85°C/85% RH. This is consistent with the results for hybrid bonding levels where a dense PECVD SiO₂ is also used. But for the bottom dies where a porous PECVD SiOC is deposited, significant variations were observed.

The electrical characterizations showed an important loss of performance and a degraded breakdown behavior even at ambient conditions. By comparing different storage modes, we showed that a storage at 85°C/40-45% RH is equivalent in terms of saturation values with ambient and only the kinetic is accelerated by temperature. This is not true for the standard 85°C/85% RH where saturation values are higher and might lead to unwanted failure mechanisms.

A diffusion path along the interface between SiCN and ULK was highlighted experimentally and validated with numerical simulations. The diffusion in adjacent layers was confirmed with TEM combined with EDX and EELS analyses and it is consistent with wafers level results. These analyses also proved fundamental difference between ambient and 85°C/85% RH storages. Copper diffusion in ULK layers is only observed in the latter one. This explains the irreversibility in breakdown behavior at 85°C/85% RH.

Based on experimental and numerical simulations, we proposed a complete mechanism for moisture diffusion in ULK stacks. However, some questions remain unanswered. Several possibilities could be tackled in a future work:

- Clarify if moisture diffuse under molecular, ionic or both forms? In what proportions depending on the storage conditions
- What is the exact transport mechanism of copper at 85°C/85% RH?
- What bonds are formed between copper and ULK layers?
- What is the kinetics of copper transport and what are the limit conditions in terms of temperature and humidity to trigger it?

To gain more understanding on these questions, we planned new test structures that are similar to the 3D stacks studied here. The approach is to target the interface between ULK and SiCN and to test different process and material modifications. Some of the modifications made are:

- Replacement of SiCN by a SiN in order to see if a non-carbonated material can limit moisture diffusion
- Modification of ULK layers in order to see if the same quantity of moisture is absorbed when the bulk is modified

- Several plasma treatments (D₂, H₂ and He) between SiCN and ULK deposition in order to densify the interface

These new test structures could not be investigated and will be studied in a future work (the samples did not come out of fab early enough). This more practical approach could suggest some simple guidelines to improve moisture reliability in low k and ULK stacks.

On a different aspect, the numerical simulation can also be greatly improved. We used 2D simulations to confirm several assumptions. The next step is to build reliable 3D simulations. This would allow to use simulations preventively in the design steps for instance.

To conclude, this study shows an example of fundamental difference between two storage modes. The samples preparation was an extreme case since the seal ring was fully removed and this is not happening for real products. A more realistic application is given in the next chapter, an opening of a few microns exists in the seal ring and comb capacitances are placed at different positions to follow moisture diffusion.

Chapter V

Empirical model to assess moisture absorption in an integrated stack

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Numerical simulations are ideal to assess moisture absorption in a microelectronic stack as discussed in the previous chapter. However, they require a complete knowledge of the diffusion parameters of each components of the stack. They also require an important calculation power due to the dimensions involved that make the meshing challenging.

Hence, it is also necessary to develop a simpler method to assess moisture absorption of a given stack. The objectives of this chapter are:

- Determine saturation values and kinetics for the structures described in the first section
- Develop a model to assess moisture absorption at different environmental conditions

In the first section, we describe the test structures used for this study. Their particularity is to have cuts in their surrounding seal ring, which are necessary for radiofrequency applications. Hence, these openings are preferential path for moisture diffusion and their reliability toward moisture needs to be assessed. Then, several characteristics of these structures – saturation values and kinetics – are presented and compared to results from Chapter IV.

In the last section, we describe an empirical model, based on similarities with electromigration phenomenon, to determine moisture absorption. The empirical parameters are then determined based on three environmental conditions. We already underline that three conditions are not enough to accurately determine all the parameters and the focus is put on the method itself. Additional storages will be performed in the future to confirm these first results.

V.1. Test structures and storage methods

This section starts with a description of the test structures. The particularity of their seal ring architecture is to include cuts over the entire seal ring thickness. This discontinuity of the seal ring can be an option for radio frequency (RF) applications. One of the reasons is to minimize unwanted noise/signal propagation, which could happen with a continuous surrounding metal seal ring [77], [104]. After introducing the different structures, we describe the storage methods to investigate moisture diffusion.

V.1.1. Seal ring designs

Figure V.1 gives a description of a $1x1 \text{ mm}^2$ structure. The surrounding seal ring is composed of three metal rings (Fig. V.1(a)). Each of them has an opening of 10 µm over its entire thickness (Fig. V.1(b)). A capacitance is placed close to the inner cut to measure moisture diffusion inside the die. Details concerning the capacitance are given below.


Figure V.1: Schematic description of the 1×1 mm² test structure. (a) Top view and (b) cross section

These cuts offer a preferential path for moisture diffusion inside the die. To maximize moisture diffusion distance, the cuts are placed as far as possible from each other. The resulting diffusion path is illustrated in Fig. V.2.



Figure V.2: Illustration of the potential moisture diffusion path inside the die

We introduce the wafer map in Fig. V.3. For each wafer, there are 77 dies available for our study. But these wafers are not only designed for our study, thus, external contributions are located in the same die with our test structures ("Die level" schematic).



Figure V.3: Description of the structures from wafer level to bloc level

Several types of structure are present in our bloc. The objective of this chapter is to study moisture diffusion with a specific seal ring design as illustrated in Fig. V.1 and V.2. Hence, several sizes of dies were implemented in order to investigate different length of moisture diffusion path. The structures illustrated in Fig. V.3 ("Bloc level") are:

- **Reference (Ref):** it corresponds to the $1 \times 1 \text{ mm}^2$ die of Fig. V.1 but there are no cuts in the seal ring, which leaves the die totally hermetic as already shown in Chapter IV.
- No Seal Ring (no SR): It corresponds to the $1 \times 1 \text{ mm}^2$ die of Fig. V.1 without surrounding seal ring. It is the worst case and it allows us to determine the saturation value faster.
- **From 3.6 to 10.8 mm:** it corresponds to the length of moisture diffusion path. These structures all have the three surrounding metal rings with the 10 μ m openings over their entire thickness. Structures go from 1 × 1 mm² to 1 × 5 mm². In the rest of this chapter, we will refer to the die by their diffusion path length (3.6, 5.4, 7.2, 9 or 10.8 mm).

V.1.2. Sawing plan

In order to let moisture diffuses inside the structures, a laser sawing is performed in front of the opening as shown in Fig. V.4. This sawing must be performed as close as possible from the opening so moisture will directly diffuse inside the structures. Contrary to the sawing in Chapter IV, dies are not singularized, which allows us to perform measurements at wafer level (sawing stops a few microns inside the silicon substrate).



Figure V.4: Description of the two sawing plan

Due to design restrictions, the 3.6 mm die could not be placed next to the other structures. The sawing performed to address this structure also opens the 10.8 mm structure. They cannot be studied on the same wafer. Hence, for each environmental condition, we use two wafers. One with sawing 1 in order to study no seal ring, 5.4 mm, 7.2 mm, 9 mm, and 10.8 mm structures. The other one with sawing 2 for the reference and 3.6 mm structures.

A top view of the area highlighted in Fig. V.4 is given in Fig. V.5. As one can see, the distance between the sawing and the opening is only of a few microns. Passivations layers (not visible in Fig. V.5) protect the die from top side diffusion.



Figure V.5: Top view of the area highlighted in Fig. IV.4

V.1.3. Capacitance structure description

The capacitance design principle is illustrated in Fig. V.6 (dielectrics and TaNTa barrier are not represented). Each metal level orientation is perpendicular to the one below. They are interconnected with metal vias. This gives two types of capacitance:

- Between two metal fingers of the same metal level (lateral capacitance)
- Between two metal fingers on top of each other (vertical capacitance)

The total capacitance is the sum of all these contributions plus the fringe capacitances that are not represented here.

The electrical alimentation is connected at the fourth metal level and metals below are connected thanks to vias.



Figure V.6: Description of the capacitance structure. (a) top view from metal 2 and (b) cross section from M1 to M5 $\,$

The geometrical dimensions are gathered in Table V.1. It gives values around 67 pF (measurements technique is described in Chapter III).

-	Dimension (nm)
Finger width	100
Interdigital space	120
Finger lengths: M1, M3 and M5	42
Finger lengths: M2 and M4	660

Table V.1: Dimensions of the capacitance structure

A simplified schematic of the dielectric layers is given in Fig. V.7.



Figure V.7: Schematic of the dielectric layers used from M1 to M5

From metal 1 to metal 5, where the capacitances are implemented, the main insulating layer is the non-porous SiOC (low-k). The capping layer is the SiCN 335 and a few nanometers of a dense SiO₂ is present between low-k and SiCN (this layer is used for chemical mechanical polishing (CMP) purposes and a few nanometers remains post CMP). A detailed description of these materials is given in Chapter I.

These layers are repeated from metal 1 to 5 then higher levels and passivation layers are deposited (including dense SiO_2 and SiN). Hence, these upper levels protect from environmental contamination from top side.

This stack is similar to the one studied in Chapter IV. The main difference is that a non-porous SiOC:H is used here. However, the chemical elements at the SiCN/low-k interface are the same. This could help us to corroborate our hypothesis of an interfacial diffusion depending on the results we obtain.

V.1.4. Storage plan

The monitoring plan is presented in Fig. V.8. As mentioned previously, two wafers are used for each environmental condition. Reference measurements are performed before laser sawing. All variations hereafter are compared to these initial measurements.



Figure V.8: Description of the monitoring plan

To address industrial obligations, Highly Accelerated Stress Tests (HAST) were performed. This standardized test corresponds to 96 hours at 130°C and 85% RH. It was repeated six times and measurements were performed at the end of each HAST.

The second conditions studied is the standard 85°C/85% RH (Thermal and Humidity Storage (THS)). Combined with the HAST results, it can be used to investigate a potential Arrhenius behavior. Wafers were removed periodically from the climatic chamber described in Chapter I to measure capacitances.

The last condition studied is simply the laboratory ambient conditions around 23°C/45% RH. It was selected because it can be performed in parallel of the other storages. From an industrial perspective, it can also help to quantify moisture diffusion inside the die during some transport or storage steps when conditions can be similar to 23°C/45% RH.

Except for a few exceptions, there are at least 30 measurements per type of structure for each series (with a maximum of 77).

V.2. Saturation values and kinetic of moisture absorption

In this section, we present the saturation values obtained for the structures without surrounding seal ring. These values are then discussed with the values obtained for the ULK stacks in Chapter IV. As mentioned in introduction, it is also necessary to assess the time required for moisture to diffuse through the seal ring path. This delay is determined for each seal ring length at three environmental conditions.

V.2.1. Saturation values

Fig. V.9 presents the drifts of the reference structure after 1500 hours at ambient, 1350 hours at $85^{\circ}C/85^{\circ}$ RH and 576h at $130^{\circ}C/85^{\circ}$ RH (n is the number of measurements).





Almost no variation is observed after long storage durations even at 130°C/85% RH. The pads degradation could explain the few points out of the distributions.

Based on these measurements, we can consider that capacitance variations above 0.10% are significant.

The capacitance variations for the structures without a surrounding seal ring are presented in Fig. V.10.



Figure V.10: Capacitance relative variation for the structure without seal ring at three environmental conditions

The saturation values are similar around 35-40 % for the two conditions at 85% RH. It is not possible to make a finer analysis because the measurements dispersion is relatively important. Moreover, due to measurements repetition, pads start to be degraded. It might explain the higher deviation observed on the last point at $130^{\circ}C/85\%$ RH.

Even though the saturation has not been reached at 23°C/45% RH, it is plausible that the value will be significantly lower than the two other conditions (only around 15% increase after 1500 hours).

As mentioned in section 1, the dielectric layers are similar to the ones investigated in Chapter IV, the main difference being the porosity of the SiOC:H. A comparison between the saturation values of the two stacks is given in Fig V.11.





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For the ULK stacks, the saturation value was almost reached after 900 hours at $23^{\circ}C/45\%$ RH. Thus, it corroborates that the value around 15% for low-k stacks is close to their saturation value.

For both storages, low-k stacks have a significantly lower saturation value as expected. This can be explained with the results from Chapter II and IV.

Indeed, both stacks are very similar except for their intermetal dielectric. At $85^{\circ}C/85\%$ RH, the bulk of ULK absorbs about 5 times more moisture than the bulk of low-k (see Chapter II – Table II.2 and II.3). Because both materials have a similar SiOC:H bulk, it is plausible that the moisture absorption mechanism is similar. One of the consequences is that moisture should affect similarly the dielectric constant of ULK and low-k. With that assumption, it is consistent that the low-k stacks have a lower capacitance saturation value than ULK stacks.

It is also consistent that this value is not five times lower, as observed for dielectric bulks. For both capacitance structures, we have 40 nm SiCN layers. And both stacks are affected by plasma during etching steps. Thus, the bulk is only a part of the overall capacitance and other contributions are similar between the two stacks.

Additional experiments with various thicknesses for each layer are required to determine the exact contributions in the overall capacitance values.

V.2.2. Kinetic of moisture absorption

The structures with cuts in their seal ring are the main focus of this chapter. One of the objectives is to determine the time necessary for moisture to reach the capacitance. The minimal distance between the external cut and the capacitance is 3.6 mm (Fig. V.4). This distance in the seal ring offers a delay before moisture is detected by the capacitance. This is illustrated in Fig. V.12.



Figure V.12: Illustration of the delay due to the seal ring path before moisture reaches the capacitance

Once moisture reaches the capacitance, its value starts to increase. Fig. V.13 shows the capacitance evolution for all seal ring paths at three environmental conditions: $23^{\circ}C/45\%$ RH (a), $85^{\circ}C/85\%$ RH (b) and $130^{\circ}C/85\%$ RH (c).



Figure V.13: Capacitance relative variation for each seal ring lengths at 23°C/45% RH (a), 85°C/85% RH (b) and 130°C/85% RH (c)

For each condition, the capacitance increases linearly as a function of square root of time in the first hours as expected for a diffusion process. However, the 3.6mm structure has a different slope from other structures, this is clearly visible at 85°C/85% RH and 130°C/85% RH. We will propose an explanation further below.

The time necessary for moisture to reach the capacitance corresponds to the intersection between the experimental slopes and the horizontal axis. This is illustrated in Fig. V. 13(c) for the 5.4 mm seal ring path.

We plotted these times as a function of the seal ring length in Fig. V.14.



Figure V.14: Time to reach the capacitance as a function of the distance between the external cut and the capacitance at 23°C/45% RH (a), 85°C/85% RH (b) and 130°C/85% RH (c)

The red dots correspond to the 3.6 mm. It is treated separately due to its different behavior shown in Fig. V.13.

These results confirm that the diffusion mechanism evolves as function of the square of the diffusion distance as expected:

$$D \sim \frac{L^2}{t}$$
 (V.1)

Of interest is also the lengths involved. The 10.8 mm structure corresponds to a $1 \times 5 \text{ mm}^2$ structure. Even at ambient, it only takes approximately 500 hours for moisture to diffuse inside the die. Many actual products are smaller than these dimensions, thus, the potential effects of moisture on reliability must be considered.

These results again echo the ones from Chapter IV. It takes less than a hundred hours for moisture to reach the capacitance for shorter structures. Thus, the diffusion kinetic is fast. A bulk diffusion with diffusion coefficient around $10^{-14} - 10^{-15}$ cm².s⁻¹ is not plausible. The hypothesis of an interfacial diffusion at the SiCN/low-k interfaces is favored here. Results from the next section will support this assumption.

- Particular behavior of the 3.6mm structure

As mentioned above, the 3.6mm structure has a different behavior compared to other structures. Moisture absorption is slightly more important as it is shown by the different slope (Fig. V.13). The only difference for this structure is its position in the block (Fig. V.4 and V.15), which results in a different sawing.

The elements in the sawing path are different between sawing 1 and sawing 2. This is important because we only performed a laser sawing. Thus, a part of the materials in the sawing path is not removed but only recast and displaced. This is illustrated in Fig. V.15.



Figure V.15: Comparison between the sawing paths of sawing 1 and 2. Aluminum dummies are only present in the sawing path of sawing 1 (copper and aluminum dummies are metal vias or lines that are only present to obtain an homogenous metal density over the entire structure)

There is no aluminum in the sawing path of sawing 2 due to design rules. Thus, there is less recast of metal in that case, which means less obstacle for moisture diffusion. This is consistent with the higher capacitance variations measured for the 3.6 mm structure. The presence of aluminum dummies could also impact the creation of cracks in the dielectric layers below (SEM views are required to confirm these assumptions). However, there is no reason for the diffusion mechanism to be fundamentally different as it is only the moisture flux that is lessen due to more metal obstacles.

V.2.3. Preliminary conclusions

In this section, we determined the saturation values for this stack at three environmental conditions. These values are consistent with results from Chapter II and Chapter IV. We also determined the minimal significant variation at 0.1%, which is important in order to study the structures with cuts in their seal ring.

Then, the time necessary to reach the first capacitance was assessed for each seal ring length and at every storage condition. It showed a fast kinetic for moisture diffusion that is again consistent with the results for ULK stacks (Chapter IV). Due to the similar chemical elements, it is very plausible that the low-k/SiCN interface is the main diffusion path.

To go further in this part of the study and to be able to evaluate moisture diffusion for different environmental conditions, we present a model based on the Black's equation.

V.3. Development of a reliability model

In this section we present a model to assess moisture diffusion inside the structures with cuts in their seal ring. The objective is to use this model to determine the evolution of the capacitance at a given environmental conditions.

First, the method is applied on the 3.6 mm structure (Fig. V.4). Then, the parameters for other seal ring length are gathered in the summary section in Table V.3.

V.3.1. Description of the model

The methodology is based on the methodology used to study electromigration. We only describe it shortly here. Further explanations on electromigration can be found in the following references [105]–[107]

During electromigration tests, samples are stored at high temperature with an imposed current. Due to the collisions with electrons, the metal atoms are moved from their initial position. It results in voids at the anode and metal accumulation at the cathode, which electrically translates into an increase in the resistivity of the metal line. This is a progressive phenomenon that involves diffusion mechanisms and that is partly reversible.

There are several similarities for moisture diffusion. The Arrhenius behavior is well-known and we also studied it in Chapter II. Instead of the current, we have the relative humidity that will bring the necessary water molecules that will increase the permittivity of the layers inducing capacitance variation. Hence, we monitor the capacitance that is a good indicator of the presence of moisture. Moisture diffusion is also progressive and partly reversible.

The influence of temperature and humidity was studied by Peck for galvanic corrosion of aluminum [108]. His model involves a classical Arrhenius dependency for temperature and a power law for relative humidity. For capacitance variations, we define the mean time to failure MTTF as the duration required for half of the samples population to reach a given drift value. Hence, the mean time to failure can be described empirically as:

$$MTTF = A \times (RH)^{-n} \times \exp\left(\frac{E_a}{kT}\right)$$
 (V.2)

Where A is a constant, n the relative humidity exponent, k is the Boltzmann's constant and E_a is the thermal activation energy.

We determine the different parameters with the following steps:

- Check that the diffusion mechanisms are similar for all storages by comparing statistical distributions and determine each MTTF
- Determine thermal activation energy E_a from the two storages at 85% RH
- Determine RH power law parameter n

In order to accurately determine each parameter, five storages are required at least (three temperatures and three relative humidity levels, one storage can be common to both). Unfortunately, it was not possible to perform more than three storages due to logistical limitations, and further experiments will be performed in future work. Hence, only two points

are available and used to determine a potential activation energy that will need to be confirmed in the future. Nonetheless, we use literature values to discuss this activation energy. For the power law parameter concerning relative humidity, we only have one storage and we use extrapolation to determine this parameter. Obviously, in the following development detailed hereafter, only the method matters, and an accurate value will be determined by future work.

V.3.2. Statistical distributions

For each capacitance, at each condition, we interpolate or extrapolate the time necessary to reach a given variation percentage with a linear regression. This is represented graphically in Fig. V.16 for a few dies at 130°C/85% RH with a variation criterion of 2%.



Figure V.16: Illustration of the interpolation at 2% increase for several dies at 130°C/85% RH

It gives a distribution of times (t_1 to t_n) required to reach a 2% capacitance increase at 130°C/85% RH. We repeated these steps for all environmental conditions with several variation criteria. The corresponding distributions are plotted with a normal scale in Fig. V.17.



Figure V.17: Statistical distributions of the storage time required to reach a given capacitance variation criterion

Several parameters of the distributions are gathered in Table V.2.

	Median time TTF50% (hour)	Standard deviation
23°C/45% RH - Criteria = 0.5%	2106	424
23°C/45% RH - Criteria = 1%	7133	1484
85°C/85% RH - Criteria = 0.5%	236	16
85°C/85% RH - Criteria = 1%	455	14
85°C/85% RH - Criteria = 2%	1099	47
130°C/85% RH - Criteria = 1%	143	6
130°C/85% RH - Criteria = 2%	442	33

Table V.2: Median time and standard deviation related to the distribution in Fig. V.16

All the points from the 23/45 distributions and the points at 2% at 85C/85% RH are extrapolated (experimental variations are only up to 0.4% after 1500 hours at 23°C/45% RH), which can explain the important deviations. More experimental data are required to improve these extrapolations.

Except for these extrapolated points, the distributions are similar. Based on these, we consider that the diffusion mechanism is the same and modifying temperature or humidity only accelerates or decelerates this mechanism for a given capacitance variation.

From chapter IV, we know that saturation values are different between ambient and 85°C/85% RH, hence, the previous assumption can only be true at low variation percentages. And further experiments are required to confirm the assumption. A simple one would be to perform an annealing at 125°C for a given variation percentage at different storage conditions (not performed here due to the lack of wafers).

As previously enounced, we then try to determine the model parameters (Ea and n).

V.3.3. Thermal activation energy (E_a)

The thermal activation energy is determined from the two storages at 85% RH. We need to compare points for the same drift criteria. The data for two drifts criteria are presented in Table V.3:

Table V.5. MITF at 85 C/85% KH and 150 C/85% KH		
	85°C/85% RH	130°C/85% RH
MTTF for criteria = 1 %	455	143
MTTF for criteria = 2 %	1099	442

Table V.3: MTTF at 85°C/85% RH and 130°C/85% RH

Then, we reported these MTTF on an Arrhenius plot in Fig. V.18:



Figure V.18: Arrhenius plot of the capacitance relative variation

The thermal activation energy is around 0.25 - 0.32 eV for this moisture diffusion mechanism. As already mentioned, at least a third point is necessary to confirm these values. One of the standard preconditioning industrial storages is performed at 60°C/90% RH, hence, a future stress at 60°C/85% RH would be relevant to complete this study.

However, we can already discuss this value around 0.3 eV by referring to the literature. Xu &al studied moisture diffusion along the TiN/PECVD SiO₂ interface [21]. They found a thermal activation energy of 0.74 eV for SiO₂ bulk diffusion (already discussed in section 3.1 in Chapter II) and a value of 0.21 eV for the interfacial diffusion (for a temperature range from 8 to 90°C).

More recently, Lin determined a thermal activation energy of 0.27 eV for moisture diffusion along the interface between silicon substrate and organosilicate glass [20] (similar to our ULK layer).

Besides, we observed in Chapter IV that the process of diffusion is occurring at the SiCN/ULK interfaces. Due to the similar nature of the interface low-k/SiCN and with the activation energy around 0.3 eV found above, it is very plausible that the main diffusion path is the low-k/SiCN interface.

V.3.4. Relative humidity dependent parameter (n)

The last parameter to determine is the exponent n for the relative humidity power law. We need to have data for three storages at the same temperature and different RH levels. However, we only have one here, thus, the purpose of this section is only illustrative and will be completed in the future to obtain a consistent value for m.

We start with the experimental measurements at 23°C. We have the MTTF for a drift of 1%. To obtain a second set of data, we extrapolate the Arrhenius plot at 23°C as shown in Fig. V.19.



Figure V.19: Extrapolation of the experimental data at 23°C/85% RH

It gives one point at 23°C /85% RH. Then, we plotted this new point with the experimental measurements at 23°C in Fig. V.20.



Figure V.20: Capacitance relative variation as a function of the relative humidity

From this graph we extract a value for the exponent n of 0.93.

To obtain a realistic value for n in a reasonable amount of time, two other storages at 85° C should be performed. For instance, a storage at 85° C/60% RH and one at 85° C/40% RH. We only present the data in this section to illustrate the method.

V.3.5. Summary

We performed the same steps for 5.4 and 7.2 mm seal ring lengths. The values are presented in Table V.3. For the 9 and 10.8 mm structures, the capacitance variations are too low and we cannot extract the parameters yet.

	E _a (eV)	n
3.6 mm	[0.25, 0.32]	0.93
5.4 mm	0.36	/ (exp. data too low)
7.2 mm	[0.33, 0.36]	/ (exp. data too low)

Table V.4: Model parameters for the 3.6, 5.4 and 7.2 mm structures

The values obtained are consistent with each other. The thermal diffusion energy is consistent with an interfacial diffusion for each case.

With the parameters above, we can calculate the ratio between two conditions for a given drift capacitance:

$$\frac{\text{MMTF}_{\text{Criteria}}(\text{T}_1, \text{ RH}_1)}{\text{MTTF}_{\text{Criteria}}(\text{T}_2, \text{ RH}_2)} = \left(\frac{\text{RH}_2}{\text{RH}_1}\right)^n \times \exp\left(\frac{\text{E}_a}{k}\left(\frac{1}{\text{T}_1} - \frac{1}{\text{T}_2}\right)\right) \quad (\text{V.3})$$

We then used Eq. V.3 to advise the future storage to perform. The storages are gathered in Table V.5. The MTTF to reach a capacitance variation of 1% are calculated from Eq. (V.3) based on the experimental data already obtained.

Storage	MTTF 1%	Objective
60°C/85% RH	~ 1000 hours	Confirm $E_a = 0.3 \text{ eV}$
85°C/60% RH	~ 630 hours	Determine n
85°C/40% RH	~ 920 hours	Determine n

Table V.5: Guidelines for future storages to perform

V.4. Conclusions

In this chapter, structures with a cut in their surrounding seal ring. Their saturation values at different environmental conditions are consistent with results at material level (Chapter II) and results for ULK stacks (Chapter IV). We showed that the diffusion mechanism is interfacial with an activation energy around 0.3 eV. It is likely that the SiOC:H/SiCN interface is again the preferential diffusion path, as it was shown in Chapter IV.

We proposed an empirical model based on electromigration phenomenon. The parameters of this model were determined with three environmental conditions. As already mentioned, more storages are necessary to confirm the results, but the main objective was to present the model and to show an application of it. Based on these first results, we advise the following storages to validate the model:

- Confirm $E_a = 0.3 \text{ eV}$ with a storage at 60°C/85% RH
- Determine n with two storages: $85^{\circ}C/60\%$ RH and $85^{\circ}/40\%$ RH

However, the empirical parameters are only valid for this design. If any change is made to the geometry of the seal ring, particularly the distance between two seal ring walls, the storages need to be performed once again. Supposing the same materials, the main diffusion mechanism will still be interfacial, but the moisture flux will be different.

This reliability approach completes the numerical simulations mentioned in Chapter IV. From an industrial point of view, it is appropriated to qualify a technology regarding moisture absorption. However, we do not know how critical the capacitance variations around 1-2% are. The performance would certainly be lowered but it could also trigger hard failures. Hence, one perspective is to assess a criterion for the capacitance variation. For electromigration tests, a criterion of 10% resistance increase is used to detect the time to failure. A similar criterion is required to study moisture absorption.

One of the conclusions of Chapter IV is also valid here. 3D numerical simulations are necessary. Due to the diffusion distances involved – at least 3.6 mm for moisture diffusion path (Fig. V.4) – and the width of the path plus layers thicknesses – a few hundred of nanometers – the finite element modeling is challenging in terms of element sizes and calculation power (2D simulations are not relevant due to the dimensions involved). These 3D simulations would allow to evaluate modifications concerning the geometry easily from simulations and determine an optimal seal ring design regarding moisture absorption and RF requirements.

General conclusions

1. Summary of results

The presence of water is known to have dramatic impacts on microelectronic devices reliability, especially with porous PECVD SiOC:H known as low-k or ULK. However, the underlying interactions between moisture and dielectric layers and moisture diffusion path are not clear. The objective of this PhD is to give a better understanding of these problematics. A global approach linking the intrinsic material properties to their behaviors in fully integrated stacks has been developed. Thus, our work was divided in two main parts:

- First, each material was studied alone in order to gather their diffusion parameters.
- Then, specific integrated stacks were investigated: 3D integrated stacks and stacks that include an opening in their surrounding metal seal ring.

• Intrinsic characterization of dielectric materials

In the first part of our work, we showed that gravimetric measurements, intrinsic stress measurements and infrared spectroscopy are equivalent in order to determine the diffusion coefficient of moisture into a given dielectric. Moreover, due to its simplicity, mass monitoring is the most appropriate method to handle an important number of samples. Hence, this technique was used to determine the diffusion properties at 85°C/85% RH of the seven dielectrics materials studied in this work.

Significant differences in the absorption behavior of dense PECVD SiO₂ compared to porous SiOC:H were highlighted. For the first ones, moisture bonds to materials thanks to dangling bonds and polar groups. This results in modifications of the nanostructure of these layers that is visible with infrared spectroscopy and also with the variations of the intrinsic stress due to a constrained swelling by the silicon substrate. Most of this absorbed moisture cannot be desorbed with temperature up to 125°C. On the contrary, for ULK layers, the mass uptake does not translate into a significant variation of the intrinsic stress. Thus, moisture is absorbed in the free volume offered by nanopores and it does not form bonds with the ULK due to its hydrophobicity. Most of the absorbed moisture can be desorbed at 125°C.

Additionally, a non-Fickian behavior was observed and investigated for SiCN layers. A dual stage model, already used for polymers, is adapted to fit the experimental data. It does not explain the underlying phenomenon, but it allows to easily reproduce the non-Fickian behavior in numerical simulations. Infrared spectroscopy combined with Tof-SIMS analysis showed a

progressive oxidation of the SiCN that correlates with the mass uptake of the layer. We proposed a mechanism that involves the progressive replacement of nitrogen by oxygen atoms to explain this non-Fickian behavior.

Finally, we characterized USG layers (dense PECVD SiO_2) under different temperature and relative humidity couples. The thermal activation energy of 0.75 eV is consistent with results from the literature. Besides, these storages also showed that the diffusion coefficient varies with relative humidity. With these results, we proposed a method to extrapolate diffusion parameters over a wide range of temperature and relative humidity.

• Moisture diffusion in integrated stacks

In the second part of our work, we investigated two types of integrated stack. As many actors of the microelectronic industry are adopting the More than Moore approach, we investigated moisture diffusion into a 3D integrated stack. Our first observations confirmed the previous results from Y. Beilliard, the seal ring discontinuity at the hybrid bonding levels is not a major reliability issue regarding moisture as diffusion is too slow in these levels (based on the diffusion coefficient found in Chapter II). However, when we exposed the top die and bottom die to moisture by sawing the seal ring on one side, two behaviors were observed:

- Top die with dense PECVD SiO₂ (USG) and SiCN as main dielectric layers: no electrical variation even after several months at 85°C/85% RH. This is consistent with the diffusion coefficients determined in Chapter II for dielectric materials alone.
- Bottom die with a porous PECVD SiOC (ULK) and SiCN as main dielectric layers: significant variations were measured even after only a few hours at ambient conditions.

The impacts of moisture on the electrical performances of low k/ULK layers are consistent with previous results from the literature. The remaining questions concern moisture diffusion path and its interactions with the stacks. Tof-SIMS analysis and numerical simulations showed that diffusion occuring at the interfaces between SiCN and ULK is the most plausible assumption. A diffusion coefficient of 3×10^{-5} cm².s⁻¹ was determined for the interface. With TEM combined with EDX and EELS analyses, a major difference was highlighted between ambient and 85°C/85% RH storages. Only in the latter one, copper diffusion into ULK layers was observed. This explains the irreversibility in breakdown behavior only observed at 85°C/85% RH.

Finally, we investigated a stack that includes an opening in its surrounding seal ring. We have developed a model to assess moisture absorption at different environmental conditions. The model is based on an analogy with Black's law used for electromigration tests. The thermal activation energy is consistent with interfacial diffusion which corroborates the results on 3D integrated stacks as dielectric materials are similar. This practical approach completes the study performed on 3D integrated stacks. From an industrial point of view, it is recommended to qualify a technology regarding moisture absorption.

2. Recommendations for future work

In this work, we have developed a global approach that led to a better understanding of the interactions between moisture and dielectric materials in advanced microelectronic devices. To do so, we tackled diverse scientific fields; thus, several aspects may serve as a starting point for a future work. We listed a few recommendations:

- The results obtained for structures with a cut in their seal ring should be followed up. This includes at least three more storages. We recommend the three following conditions: 60°C/85% RH, 85°C/60% RH and 85°C/40% RH.
- The thorough study on 3D integrated stacks raised new questions. Among them is the exact transport mechanism of copper and its interactions with ULK. It also includes the forms under which moisture diffuses. We designed new test structures similar to the 3D integrated stack studied with different material splits. These wafers should get out of fab in 2021 and they could help to answer the questions above.
- For the 3D integrated stack study, the sawing was performed over several millimeters. This allowed us to study moisture diffusion easily, but it is not representative of the real seal ring defects. Thus, a smaller seal ring sawing is required to reproduce real defects. However, with this new approach the capacitance structures used in our work might not be precise enough as they are stacked over several metal levels and very large. Charge based capacitance measurement (CBCM) could help to solve this problematic.
- The two dimensions numerical simulations developed in our work are promising. However, accurate three dimensions numerical simulations are required in the future. It implies to overcome the meshing challenges due to the high aspect ratios. But it would allow to consider moisture diffusion during integrated circuits design steps and to adapt seal ring design to avoid any moisture reliability issues. This implies also to gather the diffusion parameters of all dielectric materials at various environmental conditions which can be done following the method developed in Chapter II.
- One material parameter is still missing as mentioned several times within this work. Characterization of the evolution of the dielectric constant must be performed. With this additional parameter, the numerical simulations will be more accurate and the saturated moisture concentration of the interface between ULK and SiCN can be determined.

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Appendix A

Saturation water vapor pressure, relative humidity and environmental chambers

Environmental stress tests are performed at higher temperatures and relative humidity in order to accelerate moisture diffusion. The relative humidity RH is defined as the ratio of water partial pressure P_{H2O} to the saturation water vapor pressure P_{sat} at a given temperature.

$$RH = \frac{P_{H_2O}}{P_{sat}}$$

It can be easily understood graphically in Fig. A.1. A 10% RH at 100°C is obtained with a water partial pressure of 10 kPa.



Figure A.1: Water P(T) curve

The graph above is obtained with the Dupré equation:

$$P_{sat} = P_0 \times \exp\left(\frac{M\alpha}{R}\left(\frac{1}{T_0} - \frac{1}{T}\right) - \frac{M\beta}{R} \times \ln\left(\frac{T_0}{T}\right)\right)$$

Where M is the molar mass of water, R is the universal gas constant, P_0 is equal to 1 atm and T_0 is equal to 100°C. α and β are two constants, respectively equal to $3233 \times 10^3 \text{ J.kg}^{-1}$ and $2.639 \times 10^3 \text{ J.kg}^{-1}$.

• Temperatures below 100°C

For temperatures below 100°C, the climatic chamber presented in Chapter I is used. It functions with temperature and humidity sensors. It only operates at atmospheric pressure. Thus, it cannot be used for temperatures above 100°C. Its technical limitations are 95°C/98% RH maximum and 10°C/10% RH minimum.

• Temperatures above 100°C

A second climatic chamber is used for temperatures above 100°C. It is possible because this chamber is pressurized. Hence, water vapor pressure above 1 atm can be reached. This includes the 130°C/85% RH that corresponds to a water vapor pressure of 2.3 atm.

As it is pressurized, there is only water vapor inside the chamber. Thus, if a temperature is applied in the entire chamber then the relative humidity will increase until it reaches 100% RH. To control the relative humidity, the test space, where samples are stored, is maintained at a higher temperature than the peripheral space thanks to a heater. The temperature of the test space and the peripheral space are both monitored with temperature sensors. A schematic is given in Fig A.2.



Figure A.2: HAST equipment principle. Reproduced from [109]

The relative humidity is defined by [109]:

$$RH = \frac{Peripheral\ space\ saturated\ water\ vapor\ pressure\ (Ps)}{Saturated\ water\ vapor\ pressure\ at\ the\ temperature\ in\ partial\ area\ (Ps')}$$

To illustrate this principle, we can use the 130°C/85% RH condition. This condition is required in the main chamber. It implies a pressure of 2.3 atm. The corresponding saturation temperature

to apply in the peripheral chamber is 124.7°C (this value can be found with the Dupré equation or in [109]).

Appendix B

Hermiticity of silicon nitride layers (SiN)

As we mentioned in Chapter II and IV, SiN layers were used to ensure a protection against moisture. Prior to that, we verified the hermiticity of these layers as follow. To do so, a SiN layer was deposited on top of a PECVD SiO_2 layer known to absorb moisture. The configuration is illustrated in Fig. B.1.



Figure B.1: Schematic of the stack used to study SiN hermiticity

Due to PECVD, the SiN layer recovers the edge of the wafer, thus, it protects from lateral diffusion and the PECVD SiO_2 is totally encapsulated.

The following deposition steps were performed:

- Deposition of the PECVD SiO₂ layer.
- Since the SiN layer is deposited in a different tool, the wafer is stored at clean room conditions for some time. Thus, an annealing was performed just before deposing the SiN layer (this annealing was directly performed in the SiN deposition tool).
- Then, the SiN layer is deposited and the mass monitoring can start. The storage was performed at clean room conditions (21°C/40% RH).

In parallel, the PECVD SiO_2 layer was deposited on silicon substrate alone in order to compared with the encapsulated one. Both mass monitoring are presented in Fig. B.2.



Figure B.2: Relative mass uptake of PECVD SiO2 alone and encapsulated with PECVD SiN

Fig. B.2 confirms the mass uptake of the PECVD SiO_2 alone. However, when encapsulated there is almost no mass increase, which confirms the hermiticity of the SiN layer used in our work. The mass uptake of about 0.1% is attributed to a small moisture uptake on the surface of the SiN layer.

Appendix C

Interactions of moisture with 3D stack determined with TEM EDX/EELS – Mapping 2

The second mapping performed on the comb capacitances implemented on the ULK side with TEM combined with EDX is presented in this appendix. These results confirm the conclusion from section 4 in Chapter IV.

Fig. C.1 gives a reminder on the two mappings performed. All the results hereafter concern mapping 2.



Figure C.1: TEM view of 3D stack (a) with a focus on ULK levels (b). Mappings 1 and 2 correspond to the areas analyzed with EDX or EELS
The exact same procedure described in section 4 of Chapter IV was applied for mapping 2. Fig. X+1 shows the two chemical profiles performed:

- **Chemical profile 1:** vertical probing to investigate ULK/SiCN interface and to confirm the presence of oxygen in SiCN that was observed with Tof-SIMS analysis.
- **Chemical profile 2:** horizontal probing to study the presence of oxygen at Cu/TaNTa/ULK interfaces.



Figure C.2: Schematic view of mapping 1 in Fig. IV.33

• Investigation of oxygen presence in SiCN layers

Fig. X+2 shows the chemical profiles with the EDX mapping of oxygen for each type of sample.



Figure C.3: Chemical profiles 1 as described in Fig. IV.34 and EDX mapping of oxygen of a reference sample ((a), (d)) and samples saturated at ambient ((b), (e)) and at $85^{\circ}C/85\%$ RH ((c),(f))

A small amount of oxygen is again found for the sample stored at ambient conditions and the sample stored at 85°C/85% RH. This is consistent with the results presented for mapping 1.

• Investigation of oxygen presence in Cu/TaNTa/ULK interfaces

For the second chemical profile, the focus is put on copper and TaNTa barriers. Fig. X+3 shows the EDX mapping of copper for each type of samples.







Figure C.4: EDX mapping for copper for the three types of samples (color difference is due to the two analysis being performed separately)

Copper diffusion is only observed for the sample stored at 85°C/85% RH, which corroborates again the findings presented in Chapter IV.

The last observation concerns the presence of oxygen in the TaNTa layers. This is shown in Fig. X+4. Again, no oxygen is found in TaNTa layers only for the reference sample.

Thus, these results for mapping 2 corroborates the complete diffusion mechanism presented in Chapter IV.



Figure C.5: Chemical profiles as described in Fig. IV.31 and EDX mapping of oxygen of a reference sample ((a), (d)) and samples saturated at ambient ((b), (f)) and at 85°C/85% RH ((c),(e))

Titre : Impact de la température et de l'humidité sur la diffusion de l'eau dans les matériaux et sur les mécanismes de défaillance des circuits

Résumé : La présence d'humidité est particulièrement critique pour les applications microélectroniques : baisse globale des performances, corrosion des métaux présents dans le circuit intégré voire délaminage entre les différentes couches. Afin de protéger les puces des agressions environnementales, une structure d'interconnexion métallique continue, appelée « seal ring », est présente autour de celles-ci. Cependant, l'intégrité de cette structure de protection n'est parfois pas assurée – à la suite de difficultés pendant les étapes d'intégration par exemple - ce qui pose des problèmes évidents de fiabilité. Les effets de l'humidité sur les circuits intégrés ont été étudiés dans la littérature, en particulier pour les matériaux à faible constante diélectriques appelés « low-k ». Néanmoins, les mécanismes de diffusion et d'absorption sous-jacents restent flous. En outre, de nouvelles architectures de circuits intégrés sont développées par STMicroelectronics selon l'approche « More than Moore ». L'intégration 3D, largement utilisée aujourd'hui, en est un exemple. D'autres produits comportant une ouverture dans leur « seal ring » pourraient également être intéressants. Par leur conception, ces types de circuits présentent des risques vis-à-vis de la diffusion de l'humidité. L'objectif de cette thèse est donc d'expliquer les interactions entre l'humidité et ces nouveaux types de circuits intégrés. Pour cela, une approche globale du matériau au circuit intégré a été adoptée. Dans un premier temps, les propriétés d'absorption des principaux matériaux diélectriques utilisés dans le Back End of Line (BEOL) sont déterminées. Dans un second temps, les circuits intégrés mentionnés plus haut sont étudiés afin de proposer un mécanisme complet de diffusion/absorption d'humidité dans les circuits intégrés. Des simulations numériques par éléments finis viennent également appuyées ce mécanisme. Enfin, un modèle empirique adapté aux études industrielles, similaire au modèle de Peck, est proposé.

Mots clés : Diffusion d'humidité, mécanisme de défaillance, intégration 3D, Matériaux diélectriques, low k, fiabilité

Title: Study of temperature and moisture impact on water diffusion in dielectric materials and on electronic circuits failure mechanisms

Abstract: The presence of moisture leads to critical consequences for microelectronic applications: performance loss, metal corrosion and even delamination between the different layers of the integrated circuits. To protect microelectronic chips from environmental contaminations, a continuous surrounding metal structure, called seal ring, is implemented. However, the seal ring integrity is not always guaranteed – issues can occur during process integration steps for instance – which obviously leads to reliability problems. Moisture effects on integrated circuits have been investigated in the literature, especially for materials with a low dielectric constant, called low-k. Nonetheless, the diffusion and absorption mechanisms remain unclear. Moreover, new architectures of integrated circuits are designed at STMicroelectronics according to the "More than Moore" approach. One example of these new designs is 3D integration that is widely used nowadays. Structures with an opening in their surrounding seal ring are also considered for radio frequency applications. These types of integrated circuits are at risks regarding moisture diffusion because of their specific design. The objective of our work is to explain the interactions between moisture and these new types of integrated circuits. The philosophy of this work is to use the intrinsic material properties to explain the phenomenon occurring in integrated circuits. First, the main dielectric layers used in the Back End of Line (BEOL) are characterized and their intrinsic characteristics regarding moisture absorption are determined. Then, the integrated circuits mentioned above are studied in order to elaborate a complete diffusion/absorption mechanism of moisture into integrated circuits. Finite elements numerical simulations are used to corroborate this mechanism. Finally, an empirical model adapted to industrial approach is proposed.

Keywords: Moisture diffusion, failure mechanisms, 3D integration, dielectric materials, low k, reliability

Unité de recherche

Laboratoire de l'Intégration du Matériau au Système, UMR 5218 IMS IMS Bat A31, Université Bordeaux, 351, cours de La Libération 33405 Talence cedex