

Integration of poly-Si/SiOx contacts in silicon solar cells: Optimization and understanding of conduction and passivation properties

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Integration of poly-Si/SiO_x contacts in silicon solar cells – Optimization and understanding of conduction and passivation properties

Thèse de doctorat de l'Université Paris-Saclay préparée à l'Université Paris-Sud

École doctorale n°575 Electrical, Optical, Bio-physics and Engineering (Physique et ingénierie : Electrons, Photons, Sciences du vivant) Spécialité de doctorat: Physique

Thèse présentée et soutenue au Bourget-du-Lac, le 11 décembre 2019, par

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Contents

Acknowl	edgen	nents	5
General	introd	luction	7
Part 1. St	tate-o	f-the-art	11
I. T	oward	ds higher passivation level for c-Si solar cells	11
1.	Wor	king principle of conventional c-Si solar cells	11
2.	Mair	n loss mechanisms of a c-Si solar cell	11
3.	Cond	cept of full-area passivating contacts	13
II. P	oly-Si	contact fabrication and integration in solar cells	14
1.	Brief	historical review	14
2.	Wor	king principle of the poly-Si contact	15
3.	Fabr	ication process of the poly-Si contact	16
	a.	Growth of the thin SiO _x layer	16
	b.	Si-based layer deposition and doping	16
	c.	Annealing step	18
	d.	Hydrogenation step	18
4.	Integ	gration of the poly-Si contact in c-Si solar cells	18
	a.	Record efficiencies on small area solar cells	19
	b.	Towards industrial solar cells integrating the poly-Si contact	20
	i.	. The metallization challenge	20
	ii	i. Large area c-Si solar cells integrating the poly-Si contact	21
III. C	urren	t understanding of the passivation and transport mechanisms	22
1.	Cont	rol of the final surface passivation	22
	a.	Growth of the SiO _x layer	23
	b.	Role of doping	23
	c.	Optimization of the annealing temperature	23
	d.	Role of hydrogen	24
2.	Tran	sport of charge carriers through the SiO _x layer	25
Part 2. Ex	xperin	nental	28
I F	ahrica	ution process of R-doned poly-Si/SiO., contacts by PECVD	28

-	1.	Si-based layers by Plasma-Enhanced Chemical Vapor Deposition (PECVD)	28
2	2.	c-Si substrates and samples configuration	28
3	3.	Fabrication of in-situ doped poly-Si/SiO _x contacts	29
4	4.	SiO _x N _y :B layers for ex-situ doping of the poly-Si/SiO _x contacts	30
II.	С	haracterization techniques	31
	1.	Structural and chemical characterization	31
		a. Thickness and microstructure of the layers	31
		i. Spectroscopic ellipsometry	31
		ii. Transmission Electron Microscopy	32
		b. SiO _x chemical composition: X-ray Photoelectron Spectroscopy	33
		c. Doping profiles in a-Si:H and poly-Si layers	33
		i. Electrochemical Capacitance-Voltage	33
		ii. Secondary Ions Mass Spectroscopy	34
2	2.	Electronic characterizations	35
		a. Electrical properties of the poly-Si layer: Hall effect technique	35
		b. Lifetime measurements: Photo Conductance Decay	36
		c. Defect characterization in c-Si: lifetime spectroscopy	37
		i. SRH description of an electrically active defect center	38
		ii. Lifetime spectroscopy methods	38
		iii. Case of several SRH defect centers	39
		iv. Bulk and surface contributions to the effective lifetime	41
		v. SRH formalism at the surface	41
		d. Transport of charge carriers in the $poly-Si/SiO_x$ contact: Conductive Atom	
		Force Microscopy	
Part 3	3: Fa	abrication of the poly-Si/SiO _x contact	45
l.	0	ptimization of the in-situ doped poly-Si/SiO $_{ m x}$ contact	45
:	1.	Optimization of the deposition conditions for blister-free poly-Si(B) layers	45
		a. Effect of the deposition temperature increase	45
		b. Effect of the silane dilution in dihydrogen	46
		c. Evaluation of the poly-Si electrical properties through deposit	ion
		optimizations	46
		d. Effect of the blistering on the stability of surface passivation	47
2	2.	Crystallization and doping of the poly-Si layer	48

	a.	Crystallization of the poly-Si layer	49
	b.	Doping of the poly-Si layer	51
3.	Surfa	ace passivation properties of the in-situ doped poly-Si(B)/SiO $_{x}$ contact	54
	a.	Impact of the annealing temperature	54
	b.	Impact of the hydrogenation step	55
II. E	Ex-situ	doping of the poly-Si/SiO _x contact	56
1.	Dep	osition of the intrinsic Si layer by PECVD	56
	a.	Decrease of the in-situ B-doping	56
	b.	Optimization of the intrinsic Si layer	59
2.	Ex-si	tu doping	63
	a.	Si layer microstructure	64
	b.	Comparison of the two ex-situ doping processes	66
	į.	. Electrical properties	67
	i	i. Passivation properties	67
	c.	Doping profile of the ex-situ doped poly-Si/SiO _x contact	68
3.	Com	parison of in-situ and ex-situ doped poly-Si/SiO _x contacts	69
	a.	Si-layer microstructure	70
	i.	. After deposition	70
	i	i. After annealing	
	b.	Electrical properties	71
	C.	Surface passivation properties	
4.	Effe	ct of the doping density and hydrogen diffusion on surface passivation	74
	a.	Passivation stability upon annealing and SiN:H deposition	74
	b.	H diffusion profile in poly-Si(i) and poly-Si(B) contacts	76
	C.	Effect of the firing temperature	78
Conclusi	ion		80
Part 4. lı	nvesti	gation of the poly-Si/SiO _x interface	83
l. (Chemio	cal and structural evolution of the SiO _x layer	83
1.	SiO _x	grown at the c-Si surface	83
	a.	Ex-situ annealing in the tube furnace	83
	b.	In-situ annealing in the XPS chamber	85
	c.	Quantitative comparison of the XPS spectra after annealing	88

2.	XPS study of the poly-Si/SiO _x /c-Si stack	90
	a. Qualitative study of the oxides upon annealing	92
	b. Quantitative analysis	93
	c. Structural evolution of the SiO _x at the poly-Si/c-Si interface	95
3.	Conclusions on XPS and TEM analysis of the interface	97
II. I	nvestigation of the transport mechanism within the SiO _x layer	98
1.	Impact of the surface preparation of the sample on the C-AFM measurer	nent 98
2.	C-AFM investigation of the pinholes formation within the SiO_x layer	100
	a. Transversal measurements	101
	i. With and without interfacial SiO _x	101
	ii. Comparison of chemical and thermal interfacial ${\sf SiO_x}$ layers	102
	b. Lateral C-AFM measurements	103
3.	KPFM investigation of the pinholes formation within the SiO_x layer	104
III. S	Study of the poly-Si/c-Si interface recombination by lifetime spectroscopy .	106
1.	Sample preparation	106
2.	Extraction of the surface recombination velocity	107
3.	Linearization of τ _{surf} using Murphy's approach	110
4.	Lifetime spectroscopy for the determination of the defect parameters	111
Conclusi	ion	113
General	conclusion and perspectives	114
Appendi	ix A: Correction of ECV profiles measured on ex-situ doped poly-Si contacts	117
Appendi	ix B: Fitting procedure of the XPS Si $2p$ spectral range of a SiO_x layer	119
List of p	ublications	121
Résumé	des travaux	123
Referen	ces	134

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General introduction

Within the past few years, numerous reports from governmental agencies have emphasized the urgency to act on reducing the human-activity related greenhouse gas emissions that are responsible for climate change [1–3]. In 2019, the number of demonstrations and citizen initiatives have increased, especially among young people, showing that more and more people realize the urgency of acting on combatting climate change [4]. On **Figure 1**, one can see the average annual global temperature increase from 1850 to 2017 that especially intensified from the 90s. More specifically, in 2017, the global earth temperature had already increased by nearly 1°C compared to before the industrial revolution (that began around 1700 in the UK). If nothing is done to reduce greenhouse gas emissions, we are on a path to reach +4°C above pre-industrial levels by the end of the century. Such a rise of the global earth temperature would have dramatic environmental and social consequences [1].

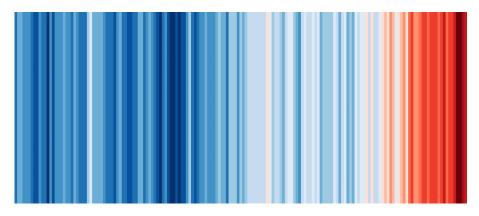


Figure 1. Annual global average temperatures from 1850 to 2018. The color scale represents the change in global temperatures covering 1.35°C (taken from [5]).

In December 2015 at the 21st Conference of the Parties (COP 21) in Paris, 55 Parties to the Convention (accounting for approximately 55 % of the total global greenhouse gas emissions) ratified the Paris agreement, whose long-term goal is to limit the increase in global average temperature to below 2°C above pre-industrial levels. In order to fulfil this goal our CO₂ emissions should be reduced by 71% by 2050 according to the report on Global energy transformation from the International Renewable Energy Agency (IRENA) released in 2019 [3]. Such a reduction requires a transition from fossil fuel energy sources to renewable ones. More particularly, the renewable energy (RE) power generation share, which represents about 25% of the total share today, would have to increase to 86% by 2050. Among the RE sources, photovoltaic (PV) and wind technologies are expected to play a major role towards a RE-based energy mix. Especially, PV technologies could support this transition by increasing the annual PV installations by a factor of three by 2050 according to IRENA's report.

Among the different PV technologies, the ones based on crystalline silicon (c-Si) have seen their production exponentially increased since the 80s (see **Figure 2**) and represent today 90% of the PV market share [6]. Due to the average c-Si module price dropping down, the PV cost

of generation is now low enough to compete with other energy sources in many regions of the world [7].

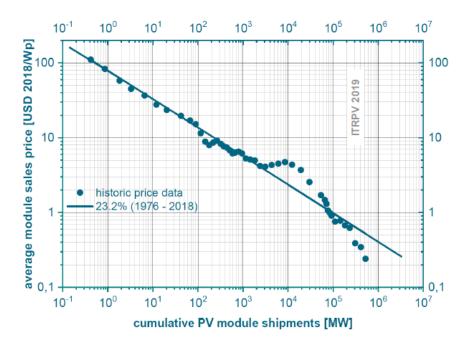


Figure 2. Learning curve for c-Si modules price versus cumulative shipments from 1976 to 2018 (taken from [6]). It indicates that when the cumulative PV module shipments increased by a factor of 1000, the average module price is divided by 10.

One remaining obstacle to a greater industrial deployment of PV technologies is the investment required to build and start a PV production facility which, combined to low margins usually observed in the PV industry, leads to a low growth rate of the manufacturing capacity [8]. One way to support the PV growth rate is to improve the c-Si solar cells (SCs) conversion efficiency, using similar facilities and equipment than the ones already implemented in current production lines.

In the currently industrialized c-Si SC architectures, a main source of current losses stems from recombination at the metal contacts. Thus, developing novel contact structures to reduce recombination at the metal/c-Si interface is currently an important topic of research among the c-Si PV community. These novel contact structures are referred to as "passivating contacts" as their main feature is to "passivate" electrically active defects at the metal/c-Si interface (e.g. by saturating them with hydrogen).

A promising passivating contact structure consists in implementing a highly-doped polycrystalline silicon (poly-Si) layer on top of a thin silicon oxide (SiO_x) layer in between the c-Si substrate and the metal electrode. The poly-Si/SiO_x contact relies on a simple fabrication process based on the growth of a thin SiO_x layer (typically ≤ 2 nm), the deposition of a Si-based layer on top of the SiO_x, and an annealing step to crystallize the Si layer into poly-Si. Such poly-Si/SiO_x contacts have already demonstrated promising performances when integrated in SCs, with conversion efficiencies of more than 25.8% obtained on small area devices ($\sim 2\times 2$ cm²) [9,10] and of 22.8% on a large area device ($\sim 156\times 156$ mm²) with screen-printed

metal electrodes [11]. Despite these promising performances, there are some remaining challenges:

- The integration of hole-selective poly-Si/SiO_x contacts at the rear surface of existing mass-produced p-type c-Si solar cells (i.e. PERC) could be one of the next significant evolutionary steps of the PV industry. So far, hole-selective poly-Si/SiO_x contacts have been mainly formed with boron-doped poly-Si layer (poly-Si(B)) and have historically demonstrated lower passivation performances compared to their phosphorus counterparts [12]. Despite recent progresses achieved with poly-Si(B)/SiO_x passivating structures on both planar and textured surfaces [13–15], boron (B) is suspected to cause more defects in the structure, especially at the interface with the SiO_x layer [16], due to low B diffusivity in SiO_x leading to B atoms piling-up at the SiO_x layer [17,18].
- The use of Plasma-Enhanced Chemical Vapor Deposition (PECVD) is interesting for single-side fabrication of the poly-Si layer, but also for optimizing the properties of the layer, notably by adding alloying elements like carbon or oxygen [19,20]. Moreover, it is already widely used in the PV industry (notably for the deposition of silicon-nitride anti-reflective layers). However, due to the hydrogen-rich precursor gases, the deposited hydrogen-rich amorphous Si (a-Si:H) layer is likely to blister, resulting in a severe degradation of the poly-Si layer after annealing [21,22]. Solving the blistering problem requires a fine tuning of the deposition conditions (especially the deposition temperature and gas ratio) [19,21,22].
- The thin SiO_x layer located at the poly-Si/c-Si interface has been shown to play a major role to ensure both excellent passivation of the c-Si substrate and a good electric contact with the metal electrode [23,24]. However, the SiO_x layer is generally less than 2 nm-thick. Therefore, due to the difficulty to study phenomena occurring in a region of a few nanometers near the SiO_x layer, the mechanisms explaining the high passivation level and the effective transport of charge carriers through the poly-Si/SiO_x contact are not fully understood yet. Moreover, despite common features, a wide range of different poly-Si fabrication processes have been demonstrated, which might not lead to the exact same mechanisms involved. Thus, an intense work of research is currently ongoing to better understand the working principle of the poly-Si/SiO_x contact.

After describing in more details the current state-of-the-art of the poly-Si/SiO $_x$ passivating contact (**Part 1**), and detailing the experimental methods on which the present work is based (**Part 2**), the two main objectives of this work will be addressed:

■ In Part 3, we elaborate on the fabrication of boron-doped poly-Si/SiO_x contacts using the PECVD route. Firstly, we focus on the optimization of the deposition of in-situ doped a-Si:H layers in the aim of reducing blistering of the poly-Si layer after annealing. After optimization, the microstructure, doping profile and passivation properties of the resulting in-situ doped poly-Si/SiO_x contact are investigated. Then, an alternative

- ex-situ doping method is considered, consisting in the deposition of a boron-rich dielectric layer on top of an intrinsic Si layer afore-deposited by PECVD.
- In Part 4, we detail the investigation of the passivation and transport mechanisms of the resulting poly-Si/SiO_x contacts, with a particular focus on the interfacial SiO_x layer. Firstly, we elaborate on the chemical and structural evolution of the SiO_x layer upon annealing for poly-Si crystallization studied by means of X-ray Photoelectron Spectroscopy (XPS) and Transmission Electron Microscopy (TEM), respectively. Then, we investigate the presence of nanometric break-ups (or pinholes) within the SiO_x layer that could enhance the transport of charge carriers using the conductive-Atomic Force Microscopy (C-AFM) technique. Eventually, we elaborate on a method based on lifetime spectroscopy techniques to model the surface recombination at the interface between the poly-Si/SiO_x and the c-Si substrate.

Part 1. State-of-the-art

I. Towards higher passivation level for c-Si solar cells

1. Working principle of conventional c-Si solar cells

In this section, a standard industrialized solar cell structure (referred to as the AI-BSF structure for Aluminum-Back Surface Field) is used to describe the working principle of a c-Si solar cell (see **Figure 3**). The AI-BSF structure is based on a p-type c-Si substrate doped with B atoms which determine the hole concentration in the c-Si. The sunlight is absorbed in this p-type c-Si and photons with energies *hv* larger than the c-Si bandgap (1.124 eV at 300 K) are converted into free charge carriers (i.e. electron-hole pairs). The c-Si substrate enables sufficiently high lifetimes for electrons and holes to allow for their transport towards the front and back side of the substrate, respectively. The front region is n-type doped by diffusion of P atoms. The high P density at the front side enhances the electron conductivity while reducing the hole conductivity and therefore enables the preferential transport of electrons in the front region and their further collection at the front metal contact. The rear side of the AI-BSF structure features a highly AI-doped region that creates the so-called Back Surface Field reducing the electron density in the highly-doped region and therefore enhancing the hole collection.

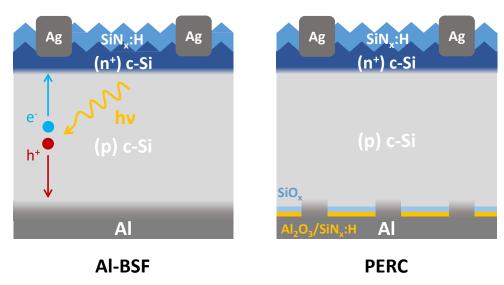


Figure 3. Schematic of Al-BSF and PERC solar cell structures.

2. Main loss mechanisms of a c-Si solar cell

The energy conversion efficiency of a SC is determined as the fraction of incident light power that is converted into electrical power. It can be expressed as:

$$\eta = rac{P_{max}}{P_{in}}$$
, eq. 1

with P_{in} the power from the incident light and P_{max} the maximum power of the SC, which is related to the open-circuit voltage, V_{oc} , and the short-circuit current density, J_{sc} , of the SC, through:

$$P_{max} = V_{OC} \times I_{SC} \times FF$$
, eq. 2

where FF is the fill-factor. Due to the intrinsic properties of c-Si, the conversion efficiency of a c-Si SC is theoretically limited to 29% [25]. When fabricating a c-Si SC device, additional loss mechanisms limit the actual conversion efficiency to a lower value. **Table 1** sums up the main loss mechanisms that impact the SC efficiency and practical solutions that have been implemented in currently industrialized c-Si SCs to overcome these losses.

Table 1. Main loss mechanisms of a c-Si solar cell and examples of solutions to tackle them.

Loss mechanism	Arising from	Impact on	Examples of technical solutions
Optical losses	Reflection of light at the front and rear (long wavelengths)	I _{sc}	Wafer texturation Anti-reflective coating
Recombination losses	Defects in the bulk or at the surface of the c-Si	V _{oc}	Gettering of impurities Hydrogenation Surface passivation
Resistive losses	High contact resistance at the metal/c-Si contact or along the metal	FF	Metallic paste optimization Surface passivation

For Si-based SCs, reducing the surface recombination offers a large potential for efficiency increases [26]. The recombination losses of a SC are described by their associated recombination (or saturation) current density J_0 . In the case of the Al-BSF structure, the recombination current density at the rear Al/c-Si contact accounts for approximatively 70% of the total recombination current density of the SC ($J_{0,rear} \sim 600 \text{ fA} \cdot \text{cm}^{-2}$) [27,28]. This limits the conversion efficiency of such devices around 20% in mass production.

A way to decrease the $J_{0,rear}$ of the Al-BSF structure is to decrease the surface area of the Al/c-Si contact. For example, the PERC (Passivated Emitter and Rear Cell) structure features an additional passivation of the rear side consisting of a SiN:H/Al₂O₃ stack, on top of which a full-area Al layer is deposited and locally opened by laser ablation to create Al/c-Si local contacts (see **Figure 3**). From Al-BSF to PERC, the reduction of the Al/c-Si surface area at the rear side enables a decrease of $J_{0,rear}$ to values lower than 100 fA·cm⁻² and thus an increase of the conversion efficiency around 22% [28,29].

Despite the reduced Al/c-Si surface area at the rear side of the PERC structure, recombination at the local Al/c-Si contacts remains one of the main limitations to a further increase of the PERC conversion efficiency. Therefore, over the past few years, a main trend in the Si PV field has been to develop contact structures to fully-passivate the metal/c-Si contacts.

3. Concept of full-area passivating contacts

As defined in the literature, the requirements for an "ideal" contact are the following [30,31]:

- The passivation of defects at the c-Si interface (e.g. Si dangling bonds) resulting in low interface recombination current density (J₀) and high implied open-circuit voltage (iV_{oc});
- The separation of charge carriers at the c-Si interface to enable the transport and further collection of one type of carrier through the contact while blocking the other type (often referred to as "carrier-selectivity");
- A low contact resistivity with the c-Si substrate to prevent resistive losses that would affect the FF.

In the currently industrialized SC structures, surface passivation of the c-Si is ensured by dielectric layers (e.g. SiN:H, Al_2O_3) that effectively saturate Si dangling bonds at the c-Si interface. Moreover, they often feature a density of fixed charges (positive or negative), which provides an additional electric field that attracts preferentially either electrons or holes. However, a dielectric layer is an insulator, i.e. it blocks both types of carriers, so the dielectric layers need to be locally opened to enable carrier collection through metal/c-Si direct contacts (e.g. at the rear side of the PERC structure).

The carrier-selectivity in homojunction c-Si SCs is classically ensured by creating highly-doped regions (e.g. by diffusion) that lead to a strong difference of local conductivity for electrons and holes and enables carrier-selectivity. However, increasing the doping density in the c-Si entails on an increased Auger recombination activity, which leads to lower V_{oc} values.

The main feature of a full-area passivating contact is to ensure both passivation and carrier-selectivity (thus, they are sometimes referred to as "passivating and carrier-selective contacts"). An interesting concept of full-area passivating contact consists of an intermediate layer to passivate the c-Si surface on top of which is deposited a highly-doped layer to ensure carrier-selectivity (see **Figure 4**).

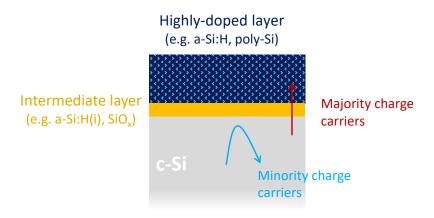


Figure 4. Full-area passivating contact concept consisting of a highly-doped layer for carrier-selectivity on top of a thin intermediate passivation layer.

The first example of such a contact has been used for years in silicon heterojunction SCs (SHJ), and consists in a thin intrinsic H-rich amorphous Si layer (a-Si:H(i)) for passivation and a doped a-Si:H layer (n- or p-type) for carrier-selectivity. The excellent surface passivation provided by the thin a-Si:H(i) layer results in Voc values as high as 750 mV and conversion efficiencies up to 26.7%, which is the current world-record for c-Si SCs [32]. However, the thermal stability of SHJ SCs is limited to 250°C due to the degradation of the surface passivation provided by a-Si:H layers for higher temperatures. Therefore, the SHJ structure is not compatible with high-temperature steps performed at the end of the current industrial process of c-Si SCs to decrease the metal/c-Si contact resistance, but also improve the carrier lifetime of the c-Si substrate (through gettering of impurities and hydrogenation). This limits the SHJ development at a larger scale because high quality n-type c-Si wafers are then required to fabricate SHJ SCs.

The next generation of full-area passivating contact consists of a thin silicon oxide (SiO_x) layer for surface passivation of the c-Si and a highly-doped polycrystalline silicon (poly-Si) layer for carrier-selectivity [33]. The main advantage of the poly-Si/SiO_x contact compared to the a-Si:H heterojunction is its resilience to high temperatures. Firstly, it promises a better compatibility with the high-temperature back-end process of existing c-Si SC production lines and therefore an easier development of the poly-Si contact at the industrial scale. Secondly, the high temperature tolerance also allows for gettering and hydrogenation treatments which makes the poly-Si/SiO_x contact compatible with a wide range of wafer materials (n- or p-type c-Si, but also multi-crystalline Si (mc-Si) or mono-like Si (ML)). In addition, the poly-Si contact itself has been shown to provide a significant gettering effect of the c-Si substrate [34,35]. In the following section, we will address the working principle of the poly-Si/SiO_x contact as well as a detailed state-of-the-art of its fabrication process and integration in c-Si SCs.

II. Poly-Si contact fabrication and integration in solar cells

1. Brief historical review

The poly-Si contact was originally developed for bipolar junction transistors (BJTs) [36]. The implementation of a highly-doped polycrystalline (poly-Si) layer (sometimes associated with an intentionally grown SiO_x layer) in n/p/n BJTs enabled to reduce the hole injection from the base to the emitter and therefore to enhance the current gain of such devices. The success of the poly-Si structure applied to BJTs led to a few attempts in the early 1980s to use it as a contact structure for c-Si SCs [37–40]. The poly-Si contact was notably implemented in the SIPOS c-Si SC [38,39] and enabled to effectively reduce J_0 at the metal/c-Si interface down to $10 \text{ fA} \cdot \text{cm}^{-2}$ and to increase V_{oc} up to 720 mV [39]. However, in the 90s, the trade-off between a low recombination current density and a low poly-Si/c-Si contact resistivity, emphasized by Gan et al. in ref. [40], was not successfully optimized at the SC level [37,39].

Interest in poly-Si contacts experienced a revival in the early 2010s through the demonstration of a 24.2% efficient IBC SC structure with patented "passivating contacts" by Sunpower Corp [41]. Shortly after, researchers from Fraunhofer-ISE and ISFH demonstrated poly-Si

contacts coupling excellent surface passivation properties and low poly-Si/c-Si contact resistivity (referred to as the TOPCon [33] and POLO [42] contacts, respectively).

2. Working principle of the poly-Si contact

In this paragraph, we will elaborate on the working principle of the poly-Si contact applied to c-Si SCs. As mentioned, a full-area passivating contact has to ensure both passivation and carrier-selectivity (i.e. enabling the transport of majority charge carriers while blocking the minority charge carriers) at the c-Si surface. It is to note that in the following, majority (minority) charge carriers refers to the doping type of the poly-Si layer, e.g. holes (electrons) for a p^+ - (n^+ -) doped poly-Si layer.

Figure 5 depicts a schematic of a p*-doped poly-Si contact on top of a p-type c-Si substrate and its associated equilibrium band diagram.

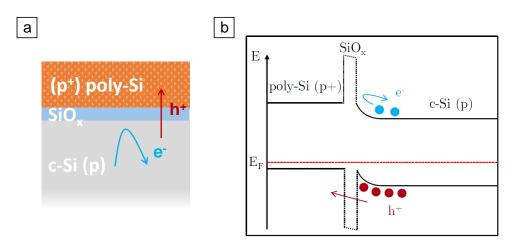


Figure 5. Schematic structure of a poly-Si(p^+)/SiOx/c-Si(p) contact (a) and corresponding equilibrium band diagram (b).

Firstly, the thin interfacial SiO_x layer is known to saturate c-Si dangling bonds, which decreases recombination at the SiO_x /c-Si interface [26]. This first phenomenon is referred to as "chemical passivation" of the c-Si surface. The transport mechanism of majority charge carriers through the SiO_x layer was already a matter of controversy among the BJT community [36] and is not fully understood for poly-Si contacts applied to c-Si SCs either. Therefore, it is currently under intense study and will be addressed in more detail in **part 1-III** of this part.

Secondly, the highly-doped poly-Si layer creates an electric field related to a band-bending in the c-Si near the interface with the poly-Si layer. It results in an accumulation of majority carriers at the c-Si surface and a depletion of minority carriers (respectively holes and electrons here), which further reduces surface recombination as one type of charge carrier is repelled from the interface. This latter phenomenon is often referred to as "field-effect passivation".

This scheme is commonly accepted to explain the general working principle of the poly-Si/SiO $_{\rm x}$ contact applied to a c-Si SC. However, an in depth characterization of the physical mechanisms involved within a few nanometers near the SiO $_{\rm x}$ /c-Si interface (e.g. evolution of the surface

passivation during the fabrication process or transport mechanism through the SiO_x layer) is quite challenging and will be addressed in more details in **part 1-III**. In the next section we will elaborate on the fabrication process of the poly-Si/SiO_x contact.

3. Fabrication process of the poly-Si contact

The fabrication of the poly-Si/SiO_x contact relies on the following process sequence:

- The growth of a thin SiO_x layer at the c-Si surface;
- The deposition of a Si-based layer on top of the SiO_x;
- The ex-situ doping of the Si-based layer (if not in-situ doped during deposition);
- A high-temperature annealing step to crystallize and/or activate dopants in the Si-based layer;
- A final hydrogenation step to enhance surface passivation of defects.

Based on this simple flow, it is possible to use different techniques at each step of the process and many combinations of techniques resulted in highly-passivating poly-Si/SiO $_x$ contacts. In the following, we will not necessarily present an exhaustive list of all the techniques that were demonstrated to form the poly-Si contact but we rather detail the most relevant ones for an industrial deployment of the poly-Si contact.

a. Growth of the thin SiO_x layer

The SiO_x thickness is targeted in the range 1-2.5 nm to allow for chemical passivation of the c-Si surface as well as transport of charge carrier in the poly-Si. The SiO_x layer is generally thermally or chemically grown at the c-Si surface. Thermal oxidation of the c-Si substrate can be achieved in a furnace with an O-rich atmosphere at moderate temperatures (600-700°C) [42]. The in-situ thermal oxidation of the c-Si directly in the LPCVD chamber used for subsequent Si layer deposition has also been demonstrated [43,44]. Chemical oxidation of the c-Si can be achieved in various ways e.g. in hot nitric acid (HNO₃) [33], or in a solution of deionized water and ozone (DIO₃) [45]. More recently different groups reported on SiO_x grown by plasma oxidation [11,46]. In particular, Nandakumar et al. reported on the SiO_x growth by plasma oxidation directly in the PECVD chamber used for the subsequent Si-based layer deposition [11]. Other dry oxidation processes involving a UV excimer or a halogen lamp system have also been demonstrated [45].

b. Si-based layer deposition and doping

The growth of the SiO_x layer is followed by the deposition of a Si-based layer which is usually performed by Chemical Vapor Deposition (CVD) either at Low Pressure (LPCVD) [42,44,47,48] or assisted by a plasma (Plasma-Enhanced-CVD or PECVD) [19,21,33,49]. Recently, the fabrication of poly-Si contacts with other deposition techniques such as Atmospheric Pressure CVD [50], Hot-Wire CVD [51] or Physical Vapor Deposition (PVD) (either sputtering [52] or e-beam evaporation [53]) was also demonstrated.

With respect to the industrial development of the poly-Si contact, the ideal deposition technique should enable:

- The single-side deposition of the layer;
- A crack-free layer;
- A homogeneous thickness and in-situ doping of the layer;
- Potential for upscale, i.e. the availability of industrial deposition tools with high throughputs.

Due to the pros and cons of each deposition technique the most promising to fabricate the poly-Si layer at the industrial scale has not been clearly identified yet. The report from ITRPV released early 2019 predicts that, for the next 5 years, industrial production of the poly-Si contact will be mainly shared between LPCVD and PECVD [6], thus, we will focus on these two techniques. **Table 2** sums up their main characteristics.

Table 2. Main characteristics of LPCVD and PECVD as deposition techniques for the fabrication of poly-Si contacts.

	LPCVD	PECVD	
Nature of the layer	a-Si for T _{dep} < 450°C	a-Si:H (or a-Si)	
Nature of the layer	poly-Si for $T_{dep} > 450$ °C	Alloying possible	
Single-side deposition	No Yes (but wrap around p		
Blister-free layers	Yes	To be optimized	
Thickness range	30 – 200 nm	< 100 nm	
Homogeneous layer			
(thickness, in-situ	To be optimized	Yes	
doping)			

Due to its widespread use in the microelectronics field, LPCVD is a mature deposition technique to obtain highly-passivating poly-Si layers. It enables the deposition of a-Si or poly-Si layers depending on the deposition temperature (T_{dep}) [54]. Moreover, a wide range of thicknesses can be targeted. However, the layer is deposited on both sides of the c-Si substrate, which can necessitate additional etching steps if the poly-Si contact is desired on only one side of the SC.

PECVD enables single-side deposition of the layer and offers the possibility to alloy the deposited layer with elements like C or O to tune the properties of the final poly-Si layer (e.g. density, optical properties) [19,55]. However, H-rich a-Si (a-Si:H) layers deposited by PECVD are prone to be inhomogeneous due to the accumulation of H_2 at the SiO_x interface, leading to the formation of voids (or blisters) [21,49]. Solving the blistering problem requires a careful optimization of the deposition conditions. Moreover, H-rich Si layers deposited by PECVD have a limited thickness of 80-100 nm, which could be linked to reappearance of the blistering problem for higher thicknesses [19,21,49,56]. The deposition of Si layers by PECVD with only SiH_4 and an inert gas (e.g. argon) as precursors was also demonstrated and is a way to limit the H-content of the deposited layer. However doping has to be performed ex-situ as doping precursors are usually highly diluted in H_2 [57,58].

Doping of the Si-based layer can be performed in-situ during the deposition step by adding dopant rich gases to the precursor mix (e.g. PH_3 , B_2H_6) [11,19,21,33] or ex-situ after deposition of an intrinsic layer. Such an ex-situ doping can be performed by conventional gaseous diffusion [42,54] or ion implantation (beam line [59] or plasma immersion [57]). As ex-situ doping involves at least one extra step, in-situ doping may be preferential for a simpler fabrication process of the poly-Si contact. However, the addition of doping precursors during LPCVD has been shown to drastically decrease the deposition rate. For PECVD, addition of H_2 -diluted doping precursors is prone to intensify the blistering of the a-Si:H deposited layer [60].

c. Annealing step

The prime aim of the annealing step is to crystallize the deposited layer (if deposited amorphous) thus stabilizing the poly-Si contact against following high-temperature back-end process steps. The crystallization annealing step is usually performed in the range $T_a = 700-1050$ °C, therefore it is also suitable for dopant activation. The effect of the annealing step on the final passivation properties of the poly-Si contact has been intensively studied and will be addressed in **part 1-III.**

d. Hydrogenation step

An additional hydrogenation step is usually performed after formation of the poly-Si contact. It results in a boost of the surface passivation properties leading to typical iV_{oc} values of 730-740 mV and minimum J_0 of 1-10 fA·cm⁻² for both poly-Si(n) and poly-Si(p) contacts (measured on symmetrical samples i.e. with the poly-Si contact on both sides of the substrate) [13,14,48,52,58,59].

Various hydrogenation processes have been investigated on the poly-Si contact: through the deposition of a H-rich dielectric layer (e.g. SiN:H or Al₂O₃) followed by a firing step, or through annealing in a H-rich atmosphere (e.g. H₂ plasma or Forming Gas Annealing (FGA)).

Most of the poly-Si fabrication processes involve an annealing step for crystallization and/or dopant activation prior to the hydrogenation process. However, Ingenito et al. demonstrated the fabrication of the poly-Si contact by omitting the annealing and performing directly SiN:H deposition on top of PECVD a-Si:H layer followed by firing [61].

4. Integration of the poly-Si contact in c-Si solar cells

In this section we will address the state-of-the-art of the poly-Si contact integration in c-Si SCs. Despite really good performances demonstrated on small-area SCs integrating the poly-Si contact, some challenges remain to further increase their efficiency and successfully achieve the transfer to large area industrialized SCs. In the following, we will detail the most promising SC structures integrating the poly-Si contact and the main challenges to their transfer at the industrial scale.

a. Record efficiencies on small area solar cells

The poly-Si contact versatility was demonstrated through its integration in numerous different c-Si SCs structures, with different Si-based wafer qualities, as well as in tandem structures coupling c-Si SCs with other technologies (e.g. III/V compounds or perovskite materials).

Figure 6 presents three successful integrations of the poly-Si contact in small-area (< 4 cm²) c-Si SCs:

- In 2013, Fraunhofer-ISE reported the very promising efficiency of 23% with their TOPCon structure, which is an n-type c-Si SC integrating an n-doped poly-Si (poly-Si(n)) contact at the rear side [33]. The TOPCon efficiency was then steadily improved up to 25.7% in 2017 [9];
- Another structure developed by the ISFH team integrates both poly-Si(n) and poly-Si(p) structures at the rear side of an Interdigitated Back Contact (IBC) p-type c-Si SC. They recently demonstrated an efficiency of 26.1% with this SC concept which is the current world-record for p-type c-Si SC [62];
- The EPFL team recently demonstrated a 22.6% bifacial p-type c-Si SC structure integrating the poly-Si contact on both sides of the SC [13].

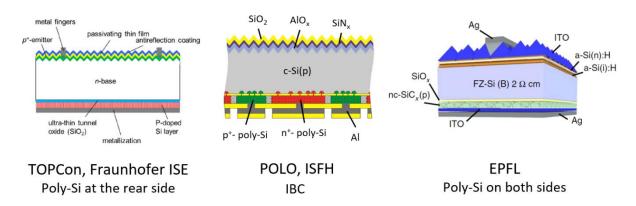


Figure 6. Integration of the poly-Si contact on small area record c-Si SCs.

The poly-Si contact has also been successfully integrated in tandem SC structures. A first example is the two terminals GaInP/GaAs on c-Si tandem SC developed by Fraunhofer-ISE reaching a conversion efficiency of 33.3% [63]. The integration of the poly-Si contact as a junction between a perovskite-based SC and a p-type c-Si SC (in the two terminals configuration) is also investigated by several groups [64,65] and recently led to a promising conversion efficiency of 25.1% [65].

Finally, the high temperature stability of the poly-Si contact is of prime interest to integrate it in SCs based on mc-Si or mono-like Si wafers. Fraunhofer-ISE currently holds the record conversion efficiency for mc-Si SCs with the demonstration of a 22.3% n-type SC integrating a TOPCon poly-Si(n) contact at the rear side [66].

However, the aforementioned SC structures have been achieved on small areas (between 1.42 and 4 cm²) with process steps that are not necessarily compatible with the current in-line production of c-Si SC (in particular the metallization process). Therefore, significant work

remains before the transfer of these promising results to the industrial scale. In the next section, we will focus on the main challenges to address when transferring the poly-Si contact to the industrial level (targeting 156 and 244 cm² area devices) and the promising results already obtained toward this goal.

b. Towards industrial solar cells integrating the poly-Si contact

i. The metallization challenge

The main challenge to transfer the poly-Si contact to the industrial scale is to find a metallization technique soft enough to avoid any damages of the poly-Si contact passivation and close to the current metallization process used in the industry. Thick poly-Si layers (> 200 nm) have been shown to be more resilient to damages induced by the metallization. However, increasing the poly-Si thickness comes at the expense of the J_{sc} value due to increasing free-carrier absorption (FCA) in the poly-Si layer. Therefore, the metallization of the poly-Si layer is driven by a trade-off between preserving the passivation properties and limiting FCA losses.

In small-area record devices, the metallization of the poly-Si layer is usually performed by thermal evaporation of metal which is a soft deposition technique but not a standard process in the PV industry. **Table 3** presents metallization processes that would be more adapted for a large-scale development of the poly-Si contact.

Table 3. Pros and cons of different metallization techniques of the poly-Si contact.

Metallization technique	Pros	Cons	
Fire through metallic	Conventional metallization	Poly-Si thickness > 100 nm to control paste penetration and	
paste + firing	process in the industry	limit R _{sheet}	
Full area metal deposition	No lateral transport required	No bifaciality	
(at the rear side)	= no R _{sheet} constraint	INO Diracianty	
TCO + low		- Passivation damages	
temperature-activated	TCO relaxes R _{sheet} constraint	induced by TCO deposition	
metallic paste		- FCA losses addition	

The current industrial metallization process of c-Si SCs relies on the deposition of a metal-based paste by screen-printing followed by a firing to form an alloy with the c-Si. For industrial Al-BSF and PERC structures, fire-through (FT) metallic pastes are used to pass through dielectric layers and contact the c-Si. Using FT pastes to contact the poly-Si layer is interesting as a H-rich dielectric layer may be used as a hydrogenation source. However, a poly-Si thickness of at least 100 nm is required to control the paste penetration in the poly-Si layer and not reach the c-Si [67]. Moreover, the thinner the poly-Si layer, the higher the sheet resistance (R_{sheet}) which is detrimental to the lateral transport of charge carriers towards local metal contacts.

An alternative rear-side metallization scheme consists in depositing a full-area metal layer on top of the poly-Si layer (with a previous etch-off of the potential H-rich dielectric layer). In this configuration, no lateral transport of the charge carriers is needed, therefore it is compatible with thin poly-Si layers which feature high R_{sheet} values. However, this approach disallows the building of a bifacial device.

Another option consists in introducing a Transparent Conductive Oxide (TCO) layer (e.g. Indium Tin Oxide (ITO) or Aluminum Zinc Oxide (AZO)) between the poly-Si layer and the metal. Using a TCO relaxes the constraint on the R_{sheet} of the poly-Si layer because the lateral transport of charge carriers will occur in the TCO layer. However, the TCO deposition can damage the poly-Si passivation, especially when deposited by sputtering [68,69]. Curing passivation damages through a subsequent annealing has been demonstrated after both AZO and ITO sputtering. However, it can lead to an increase of the ITO resistivity at temperatures higher than 300°C [68]. Moreover, TCO layers are usually not compatible with a firing step so they are contacted with low temperature activated Ag pastes that are further from the FT pastes used in the industry.

ii. Large area c-Si solar cells integrating the poly-Si contact

Table 4 below presents promising results already obtained with the integration of the poly-Si contact in large-area SCs.

Table 4. Examples of large area SCs integrating the poly-Si contact.

	c-Si SC				Poly-Si contact		
Group	c-Si type	SC structure	Surface area (cm²)	Efficiency (%)	Poly-Si layer type/deposition	Metallization	
Sunpower[70]	n	IBC	153	25.2	n/a	n/a	
Trina Solar[71]	n	IBC	239	25.0	n / LPCVD	SP Ag	
SERIS[11]	n	PERX	244.3	22.8	n / PECVD	SP FT Ag	
ECN Tempress[54]	n	PERX (PERPoly)	239	21.3	n / LPCVD	SP FT Ag	
GIT[22]	n	PERX	239	21.4	n / PECVD	Thermal evaporation Ag	
Fraunhöfer- ISE[72]	n	PERX	100	23.4	n / PECVD	PVD Ag	
Meyer Burger	n	PERX	239	21.2	n / PECVD	SP FT Ag	
Jolywood	n	PERX	246.21	23.3	n / LPCVD	SP Ag	
Jinko	n	PERX	M2	24.2	n / n/a	SP Ag	
ECN Tempress[73]	n or p	PERX (MIRACLE)	239	20.1 (n c-Si)	p / LPCVD	SP FT Ag	
Longi	р	PERX	M2	24.06	p / n/a	SP Ag	
ISFH[74]	р	Poly-Si top/rear	244	22.3	n & p / LPCVD	PVD ITO + SP low-T Ag	

One can note that the most frequent structure is a hybrid SC (sometimes referred to as "PERX") integrating the poly-Si contact at the rear side of the c-Si substrate with a standard diffused or implanted emitter at the front side. It is to note that the PERX structure is more often fabricated at the rear side of n-type c-Si which may be due to the higher maturity of poly-Si(n) contacts compared to their p-doped counterparts. However, interest in poly-Si(p) contacts is growing in view of passivating the rear side of cheaper p-type c-Si substrates and become the next generation of PERC SCs. Moreover, ITRPV predicts a growing market share of the p-type PERX structure within the next ten years [6].

There are also successful integrations of the poly-Si contact in IBC structures demonstrated for example by Sunpower or Trina Solar. To the author's knowledge only ISFH reported on a large area SC integrating the poly-Si contact on both sides of a p-type c-Si substrate reaching a conversion efficiency of 22.3%.

In conclusion, the poly-Si contact relies on a simple fabrication process and its integration in SCs led to very promising conversion efficiencies for both small and large area devices. The integration of poly-Si(p) contacts at the rear side of mass-produced PERC SCs could be one of the next significant evolutionary steps of the PV industry. Yet, poly-Si(p) contacts demonstrate lower passivation performances than their n-doped counterparts, which could arise from a lower level of maturity coupled with more B-induced defects at the interface (see part 1-III).

Despite the excellent conversion efficiencies that have been demonstrated, the good properties of the poly-Si contact to passivate the c-Si surface and enable the transport of charge carriers are still not fully understood. Therefore, within the past few years, intense research efforts have led to greater fundamental understanding of: 1) the evolution of the passivation mechanisms upon the fabrication process of the poly-Si contact and 2) the transport of charge carriers through the SiO_x layer. The main findings achieved so far will be addressed in the following section.

III. Current understanding of the passivation and transport mechanisms

1. Control of the final surface passivation

Overall, the different passivation mechanisms involved in the poly-Si contact are the following:

- The thin SiO_x layer providing chemical passivation of the c-Si surface;
- The high doping density of the poly-Si layer providing field-effect passivation;
- The additional hydrogen diffusion likely providing chemical passivation of the residual defects at the SiO_x/c-Si interface (and potentially in the c-Si).

The addition of these three mechanisms results in the aforementioned excellent surface passivation properties. However, the final passivation provided by the poly-Si contact has been shown to strongly depend on its fabrication process (e.g. the SiO_x growth or the annealing step). In the following we will address the current understanding of the interplays between the different process steps and the passivation mechanisms involved.

a. Growth of the SiO_x layer

The SiO_x growth is the first important step to control the final passivation properties of the poly-Si contact. More particularly, the SiO_x layer has been shown to play a role on the thermal stability of the surface passivation during the following annealing step. Already in the 80s, Wolstenholme et al. observed by TEM that submitting the poly-Si contact to an excessive thermal budget led to a significant break-up of the SiO_x layer [75]. More recently, other groups observed by TEM the breaking-up of the SiO_x after annealing at excessive T_a [24,76]. They correlated it with high interface recombination current density (J₀) values resulting from the increasing area of direct contact between the poly-Si layer and the c-Si substrate where the continuity of the SiO_x layer is disrupted.

Moldovan et al. also emphasized through XPS analyses the link between the SiO_x stoichiometry and the SiO_x growth technique used [45]. They demonstrated that thermally grown SiO_x are O-richer and show better surface passivation properties than their chemically grown counterparts. Poly-Si contacts featuring a thermal SiO_x layer show also more stable surface passivation properties upon annealing at high T_a [76–78].

b. Role of doping

A second important phenomenon for controlling the passivation properties is the diffusion of dopants from the poly-Si layer into the c-Si. It is well known that dopants diffuse from the poly-Si layer to the c-Si substrate during the annealing step, the length of the diffusion tail increasing with increasing T_a [19,21,79,80]. The diffusion of dopants has been shown to depend on the thickness and the method used to grow the SiO_x layer [78,81,82]. In particular, thermal SiO_x layers have been shown to better block the diffusion of dopants in the c-Si, which could result from their O-rich stoichiometry leading to a denser SiO_x phase compared to their chemical counterparts. Moreover, a shallow diffusion of dopants of a few tens of nanometers in the c-Si has been shown to improve the surface passivation properties of the poly-Si contact, which could result from an enhanced field-effect passivation.

The doping type of the poly-Si contact also plays a role on the final passivation properties. The n^+ -type poly-Si contacts (doped with P) historically demonstrated better performances than their p^+ -doped counterparts (doped with B). This difference could result from a higher segregation coefficient of B in SiO_x phases compared to P, leading to B atoms piling-up at the SiO_x interface and increasing the density of interface states (D_{it}) [16]. Recently, Young et al. demonstrated excellent surface passivation with p-type poly-Si contacts doped with Ga, which tends to confirm that B is indeed responsible for the lower surface passivation of poly-Si(p^+) contacts doped with B [16].

c. Optimization of the annealing temperature

The annealing step has been observed to involve the degradation of the thin SiO_x layer and the diffusion of dopants in the c-Si substrate. Therefore, maximizing the surface passivation properties arises from a careful optimization of the annealing temperature (T_a) to preserve

the chemical surface passivation provided by the SiO_x layer while enabling a shallow diffusion of dopants in the c-Si to enhance the field-effect passivation.

Many groups investigated the effect of T_a on the passivation properties of the poly-Si contact [33,52,79,83,84]. They usually observe a similar trend of iV_{oc} versus T_a : iV_{oc} increases with increasing T_a up to an optimal annealing temperature $T_{a,opt}$. Then, iV_{oc} decreases with further increasing T_a above $T_{a,opt}$. The underlying phenomena that gives rise to this iV_{oc} versus T_a trend are not formally established yet but some hypotheses have been proposed:

- The increase of iV_{oc} with increasing T_a up to T_{a,opt} could result from an enhanced field-effect passivation due to the shallow diffusion of dopants from the poly-Si layer to the c-Si;
- The iV_{oc} drop for $T_a > T_{a,opt}$ could result from the SiO_x disruption at too high T_a .

As mentioned before, recent studies emphasized the link between the thermal stability of surface passivation and the oxidation process used to grow the SiO_x layer, which tends to confirm that the SiO_x layer is at least partly responsible for the iV_{oc} decrease for $T_a > T_{a,opt}$. Excessive dopant diffusion in the c-Si is also sometimes proposed to explain the iV_{oc} drop for $T_a > T_{a,opt}$, as it would enhance Auger recombination in the highly-doped c-Si.

d. Role of hydrogen

As mentioned, a hydrogenation step is generally performed after annealing of the poly-Si contact to enhance the final surface passivation properties. While the benefit of the hydrogenation step on passivation has been observed at a macroscopic scale (i.e. J_0 decrease and iV_{oc} increase), a fine understanding of the mechanisms involved is still lacking.

A common hypothesis to explain the passivation gain is that H diffuses up to the SiO_x/c -Si interface and reduces interface defect density (D_{it}). Several studies reported SIMS measurements of the poly-Si contact after hydrogenation showing the accumulation of H (or D) at the SiO_x interfacial layer [16,85,86]. Interestingly, Lehmann et al. did not observe this H accumulation without a SiO_x layer intentionally grown at the poly-Si/c-Si interface. Moreover, they observed the H accumulation only at the interfaces of a 25-nm thick SiO_x grown in between the poly-Si layer and the c-Si substrate.

Another interesting observation is that intrinsic poly-Si contacts benefit as much from the hydrogenation as their highly-doped counterparts [85]. Moreover, the passivation gain after hydrogenation was shown to remain if the H-rich dielectric layer or even the poly-Si layer are etched-off [21,86]. All together, these observations tend to prove that H chemical passivation on its own provides an excellent passivation of the SiO_x/c-Si interface. However, the stability of the chemical passivation provided by H could be a matter of concern as the H is suspected to out-diffuse from the poly-Si contact in case of following high-temperature process steps performed especially after etching-off the H-rich dielectric layers [87,88].

Finally, hydrogenation processes providing atomic H (e.g. H-rich dielectric layer or H₂ plasma) have been shown to induce a better gain of passivation properties than processes providing

molecular H₂ (e.g. FGA) [19,86,89]. One hypothesis is that H in its different forms is not as efficient to diffuse through the poly-Si layer and/or passivate the c-Si interface. Despite some attempts to better understand the H diffusion and passivation mechanisms [90], the H diffusion through the poly-Si contact and the interface states it passivates are still not well understood yet.

2. Transport of charge carriers through the SiO_x layer

The mechanism explaining the transport of charge carriers through the poly-Si contact was already controversial among the BJT community. Several models to explain the charge carrier-selectivity and transport through the poly-Si contact were postulated and are detailed in ref. [36]. In some of these models, the interfacial SiO_x layer is not considered as it was not always intentionally grown at the poly-Si/c-Si interface for BJT applications.

For c-Si PV applications, a thin SiO_x layer is required at the poly-Si/c-Si interface to reach low J_0 values, therefore transport models under consideration are taking the thin SiO_x layer into account:

- The tunneling model predicts that charge carriers are transported through the SiO_x layer by tunnel effect [91];
- The pinholes model, intensively investigated by Peibst et al [92,93], postulates a direct transport of charge carriers through nanometric break-ups (or "pinholes") within the SiO_x that would appear during the annealing step for crystallization.

The pinholes model was already considered in the BJTs field in the 80s, as the SiO_x disruption was observed by TEM after annealing at high temperature ($T_a \ge 950^{\circ}C$) [75,94]. However, for PV applications, poly-Si contacts are sometimes annealed at lower temperature leading to pinholes as small as a few nanometers [76]. Moreover, Peibst et al predicted low enough J_0 values for a pinholes density in the range 8×10^5 cm⁻² to 3×10^9 cm⁻², which would lead to a distance in between two pinholes from 11 μ m to 180 nm [76,92]. Thus, imaging pinholes with local techniques like Transmission Electron Microscopy (TEM) can become very challenging.

Recently, the use of imaging techniques (like TEM or Scanning Electron Microscopy (SEM)) coupled with alternative characterization methods enabled to further investigate the transport mechanism:

Researchers from ISFH developed a chemical selective etching technique based on a Tetramethylammonium hydroxide (TMAH) solution which features a high etching rate of the poly-Si and c-Si phases compared to the SiO_x phase [95,96]. They were able to reveal pinholes in the SiO_x by etching-off the poly-Si layer and further etching in the c-Si through regions where the SiO_x is locally disrupted (i.e. through pinholes). By additional surface imaging of the sample they could estimate the pinholes density. However, Feldmann et al. recently demonstrated that this technique rather indicates a maximum value for the pinholes density as the TMAH-based solution could also etch the c-Si through regions where the SiO_x is locally thinner [97].

- Conductive Atomic Force Microscopy (C-AFM) measurements on poly-Si/SiO_x structures have recently been reported in the literature with the aim of detecting pinholes in the SiO_x layer [98–100]. Localized regions of higher current intensity (conductive spots) are observed on the resulting C-AFM current maps. Lancaster et al notably observed higher current levels when performing C-AFM on poly-Si/SiO_x structures after annealing at 950°C than after annealing at 800°C [98]. They propose that it could result from locally lower resistance as the density of pinholes in the SiO_x layer is expected to increase with increasing T_a. However, a clear link between conductive spots detected by C-AFM and the presence of pinholes within the SiO_x layer has not been established yet.
- On the other hand, Kale et al coupled the TMAH selective-etching method to Kelvin-Probe Force Microscopy (KPFM) and Electron Beam-Induced Current (EBIC) surface mappings [23,101]. Samples with a 2.2 nm-thick SiO_x layer annealed at high temperature (≥ 1025°C) featured pinholes revealed by selective-etching. On these samples they observed dark spots by KPFM and bright spots by EBIC that could respectively correspond to an inhomogeneous dopant diffusion and an enhanced carrier conduction through pinholes. By performing cross-sectional TEM on bright EBIC spots, they observed a local decrease of the SiO_x thickness from 2.2 nm to 1.4 nm. Therefore, "pinholes" could correspond to local thinning of the SiO_x rather than a complete breaking-up. Interestingly, both KPFM and EBIC mappings were homogeneous on samples featuring a 1.5 nm SiO_x layer annealed at moderate temperature (850°C).
- Some recent studies investigated the resistance of the poly-Si contact extracted from I-V curves measured at different temperatures [97,102,103]. By modeling the resistance versus temperature trend either based on the MIS theory or on the point contact theory (developed by Fisher in ref. [104]), they were able to determine if the transport of carriers is dominated by tunneling or pinholes. This procedure was performed in different configurations of current flow and pads geometry as well as on samples processed in different conditions (notably different SiO_x growth and annealing temperature). Interestingly, different groups independently observed a transition of the transport mechanism from tunneling to pinholes depending on the SiO_x growth technique and the annealing temperature.

In conclusion, investigating the transport of charge carriers through the SiO_x layer is challenging with imaging techniques due to the SiO_x thickness and the small size and low density expected for pinholes in a poly-Si contact under working conditions. The development or adaptation of other characterization techniques (e.g. TMAH selective etching, I-V(T) measurements) led to greater understanding of the transport mechanism of charge carriers through the SiO_x layer. Currently, a consensus seems to emerge: the transport mechanism of charge carriers would strongly depend on the fabrication process of the poly-Si contact (especially the SiO_x growth and the annealing temperature). Moreover, two regimes have likely been identified:

- A regime of pure tunneling through thin SiO_x layer (< 2 nm) annealed at moderate temperature (T_a < 800° C);
- A regime of transport through pinholes formed within thicker SiO_x layers (> 2 nm) exposed to high annealing temperature (T_a > 1000°C).

Part 2. Experimental

I. Fabrication process of B-doped poly-Si/SiO_x contacts by PECVD

1. Si-based layers by Plasma-Enhanced Chemical Vapor Deposition (PECVD)

The fabrication of the poly-Si contact relies on the deposition of a Si-based layer on top of the SiO_x layer, which is generally performed by LPCVD or PECVD. In this work, we chose PECVD because it enables to deposit the layer on a single-side of the c-Si wafer, which is more interesting for a lean integration of the poly-Si contact at the rear side of a p-type SC (i.e. the targeted structure). The PECVD is performed in a reactor with two 13.56 MHz capacitively coupled parallel plates (see **Figure 7**). The deposition of Si-based layers by PECVD has been extensively studied for the fabrication of SHJ SCs whose contacts consist in intrinsic and doped a-Si:H layers. For the deposition of a-Si:H layers, SiH₄ and H₂ precursor gases are introduced in the PECVD chamber where they are decomposed and ionized by the plasma. The ionized species are then attached to the substrate by chemical reaction with its surface atoms. The layer can be in-situ doped during deposition by addition of a dopant-rich precursor gas (e.g. PH₃ or H₂-diluted B₂H₆).

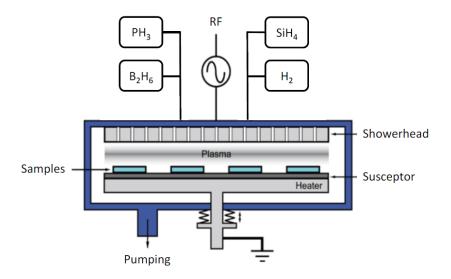


Figure 7. Schematic of a PECVD chamber for a-Si:H layer deposition (taken from [105]).

In this work, we based the fabrication of our poly-Si contact on boron-doped a-Si:H layers afore-developed in our lab for SHJ SC applications. The optimization of deposition conditions to obtain highly-passivating poly-Si contacts will be discussed in more details in **part 3**.

2. c-Si substrates and samples configuration

In this work, we fabricated samples from three types of c-Si wafers:

■ 275 μ m-thick mirror-polished 4 inch n-type Czochralski (Cz) c-Si wafers with (100) crystalline orientation and resistivity (ρ) of 2-3 Ω -cm;

- 180 μ m-thick KOH-polished 156 mm pseudo square (psq) n-type Cz c-Si wafers with (100) crystalline orientation and ρ in the range of 5-6 Ω ·cm ;
- 180 μ m-thick KOH-polished 156 mm pseudo square (psq) n-type Cz c-Si wafers with (100) crystalline orientation and ρ in the range of 2-3 Ω ·cm.

We used mirror-polished 4" wafers to optimize the poly-Si/SiO $_x$ contact fabrication (notably the deposition conditions). This type of wafers was also used for characterizations of the contact properties. For the process optimization and most of the characterizations, we fabricated the poly-Si/SiO $_x$ contact on a single side of the c-Si wafer.

The KOH-polished 156 psq wafers correspond to the size and topography for the targeted integration of the poly-Si/SiO $_{\rm x}$ contact. Therefore, we used these wafers to assess the surface passivation properties of the poly-Si/SiO $_{\rm x}$ contact. To this purpose, we fabricated the poly-Si/SiO $_{\rm x}$ contact on both sides of the c-Si wafer. In the following, we will refer to the samples with the contact on both sides as "symmetrical samples".

3. Fabrication of in-situ doped poly-Si/SiO_x contacts

A simplified schematic of the fabrication process of the in-situ doped poly-Si/SiO $_{\rm x}$ contact is presented in **Figure 8**. We first perform an RCA wet chemical cleaning of the c-Si wafers with an additional 10 min-long ozonized DI-H $_{\rm 2}$ O rinsing (DIO $_{\rm 3}$) step to grow a thin SiO $_{\rm x}$ layer (~1.3 nm) at the surface of the c-Si wafers. Then, we deposit an a-Si:H(B) layer by PECVD on top of the SiO $_{\rm x}$ layer. The thickness of the a-Si:H(B) layer is targeted in the range of 20-30 nm. Precursor gases for the deposition consist of silane (SiH $_{\rm 4}$), hydrogen (H $_{\rm 2}$), and H $_{\rm 2}$ -diluted diborane (B $_{\rm 2}$ H $_{\rm 6}$). The RF power and pressure are always kept constant for the a-Si:H(B) deposition, equal to 40 W and 1.5 Torr, respectively. Finally, we perform an annealing step at a temperature T $_{\rm a}$ in the range of 700-900°C in a tube furnace under argon atmosphere. Samples are loaded at 400°C and a ramp rate up of ~10°C/min is applied to reach T $_{\rm a}$ for a 30 min plateau. Samples are then unloaded at 700°C with a ramp rate down of ~10°C/min. In the following, we use the term "poly-Si" to refer to the layer after annealing (since structural characterizations have proven the polycrystalline nature of the layer after annealing).

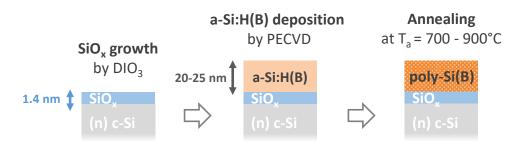


Figure 8. Fabrication process of in-situ doped poly-Si(B) contact.

We then perform an additional hydrogenation sequence (see **Figure 9**), which consists of the deposition of an 80 nm-thick H-rich silicon nitride (SiN:H) layer by PECVD on top of the poly-Si layer followed by a rapid thermal annealing (firing) step performed in a belt furnace, under air and at a temperature T_{firing} in the range of 800-900°C. A subsequent chemical etching of the

SiN:H layer is sometimes performed by dipping the samples in a concentrated HF solution for approximately 1 min.

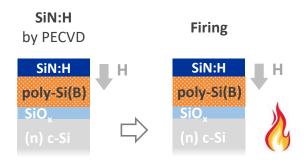


Figure 9. Hydrogenation process.

4. SiO_xN_v:B layers for ex-situ doping of the poly-Si/SiO_x contacts

We applied an ex-situ doping of the poly-Si layer based on the deposition of boron-rich dielectric layers (SiO_xN_y :B) on top of an intrinsic Si-based layer. SiO_xN_y :B layers were afore-developed in our lab for the purpose of an optimized SC process [106].

The fabrication of ex-situ doped poly-Si/SiO_x contacts is similar to the one of in-situ doped contacts described in the previous section (see **Figure 10**). First, a thin SiO_x layer (1.3 nm) is grown on the surface of the wafers by DIO₃. Then, an intrinsic Si layer is deposited by PECVD using SiH₄ and H₂ as precursor gases and targeting a thickness in the range of 20-30 nm. The high gas flow ratio between H₂ and SiH₄ used during PECVD resulted in the deposition of a microcrystalline Si layer, therefore, the layer after deposition is denoted as: μ c-Si(i). For the ex-situ doping, the B-rich dielectric layer (SiO_xN_y:B) is deposited by PECVD on top of the μ c-Si(i) layer and followed by an annealing step in the range of T_a = 700-900°C to ensure dopant diffusion and further crystallization of the layer. An additional hydrogenation step is then performed. The annealing and hydrogenation steps are similar to the ones described in the previous paragraph for in-situ doped poly-Si/SiO_x contacts.

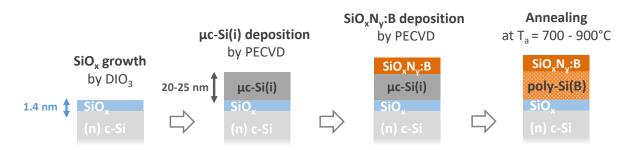


Figure 10. Fabrication process of ex-situ doped poly-Si contact.

II. Characterization techniques

1. Structural and chemical characterization

a. Thickness and microstructure of the layers

i. Spectroscopic ellipsometry

The spectroscopic phase modulated ellipsometry in the UV-visible range consists in analyzing the evolution of the polarization state of a monochromatic light reflected at the sample surface. It is particularly adapted to the determination of optical properties and thickness of thin layers.

A polarized light is impinging the sample surface with an incident angle Θ = 70°. The light reflected from the sample is analyzed with a second polarizer. The change of the polarization from the incident to the reflected light can be expressed by the Fresnel coefficients: $r_p = \frac{E_p^r}{E_p^i}$ and $r_s = \frac{E_s^r}{E_s^i}$, with $(E_p^i \; ; \; E_s^i)$ and $(E_p^r \; ; \; E_s^r)$ the perpendicular contributions to the electric field associated with the incident and reflected light, respectively.

The experimental values actually measured are referred to as the ellipsometric angles (usually denoted Ψ and Δ). They are linked to r_p and r_s according to the following equation:

$$\rho \equiv \frac{r_p}{r_s} = \tan(\Psi) \exp(i\Delta)$$
 eq. 3

From the measurement of Ψ and Δ and the knowledge of the incident angle Θ , the pseudo-dielectric function $<\epsilon>$ of the layer can be calculated (in the case of a semi-infinite material and a polished surface) according to:

$$<\varepsilon(\omega)>=\sin^2\theta\left(1+\left(\frac{1-\rho}{1+\rho}\right)^2\,\tan^2\theta\right)=<\varepsilon_r(\omega)>+\mathrm{i}<\varepsilon_i(\omega)>,$$
 eq. 4

with $\langle \epsilon_r \rangle$ and $\langle \epsilon_i \rangle$ the real and imaginary part of the pseudo-dielectric function, respectively.

The fit of the pseudo dielectric function based on theoretical models enables to evaluate the properties of the layer (e.g. optical properties, thickness, roughness).

The qualitative analysis of the imaginary part of the pseudo-dielectric function $<\epsilon_i>$ (denoted ϵ_i in the following for a matter of simplicity) as a function of the photon energy E_{ph} can also provide information about the material microstructure. **Figure 11** depicts examples of the ϵ_i versus E_{ph} signal obtained for a-Si:H, c-Si and μ c-Si materials. One can observe that the a-Si:H signal exhibits a single broad peak centered around 3.5 eV, whereas the c-Si signal shows two peaks centered around 3.4 eV and 4.2 eV. As expected, the μ c-Si signal is an intermediate between the a-Si:H and c-Si ones.

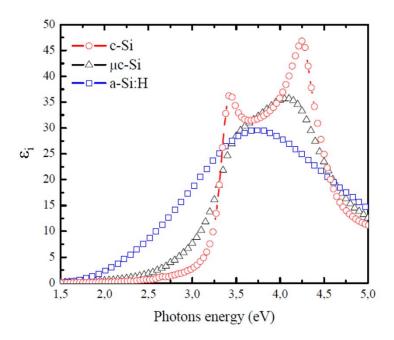


Figure 11. Imaginary part of the dielectric function ε_i as a function of the photon energy obtained by spectroscopic ellipsometry measured on c-Si, μ c-Si and a-Si:H layers (taken from ref. [107]).

In this work, ellipsometry was used to assess the thickness of the SiO_x , a-Si:H and poly-Si layers (on mirror-polished samples). The fitting model for the a-Si:H layer was based on a Tauc-Lorentz model [108]. For the fitting model of the poly-Si layer, we considered a layer consisting of a mix of crystalline clusters in an amorphous matrix (adapted from refs. [109,110]).

The thickness of the different layers assessed by ellipsometry were in good agreement with the targeted thickness (within ±2 nm) so as a matter of simplicity, only the targeted thickness will be mentioned.

ii. Transmission Electron Microscopy

Transmission Electron Microscopy (TEM) was used in this work to observe the local microstructure of a-Si:H and poly-Si layers (after deposition and after annealing, respectively) and the local homogeneity of the SiO_x layer at the poly-Si/c-Si interface.

TEM is a microscopy technique in which a high-energy beam of electrons is transmitted through a very thin sample (typically 100 nm-thick). From the interactions between the electrons and the atoms, an image of the sample is formed. As the wavelength associated to electrons is much smaller than that associated to photons, the resolution attainable with TEM is higher than the one of a conventional optical microscope.

In this work, the Scanning TEM (STEM) technique was used. STEM enables to scan a very finely focused beam of electrons across the sample in a raster pattern and permits (unlike TEM) the use of other signals e.g. electron energy loss. The Electron Energy Loss Spectroscopy (EELS) coupled to STEM observations enables an additional chemical analysis of the sample. EELS analyzes the energy loss of transmitted electrons that experiment inelastic scattering when

passing through the sample. It provides information about the interacting atoms, including elemental identity and chemical bonding. In this work, EELS was used to locate and map the oxygen concentration in the samples observed by STEM.

Devoted STEM samples were fabricated from mirror-polished c-Si wafers. They were etched using a Focused Ion Beam (FIB) to obtain 80 nm-thick and 10 µm-large lamellas.

b. SiO_x chemical composition: X-ray Photoelectron Spectroscopy

The chemical composition of SiO_x layers was investigated using X-ray Photoelectron Spectroscopy (XPS). XPS enables to analyze the extreme surface of a sample (depth-analysis of \sim 5 nm) to provide information about the chemical elements and the nature of the chemical bonds that exist between these elements.

The sample is put under ultra-high vacuum and is irradiated with an X-ray source, which results in the emission of electrons from the sample. These electrons are collected through an electrostatic analyzer that measures their kinetic energy E_{kin} . The kinetic energy of the electrons emitted by the sample depends on the initial X-ray photon energy and on the element they were ejected from as well as its local chemical environment. Knowing the initial photon energy E_{ph} , the binding energy E_{B} of electrons in the sample can be determined from the following equation [111]:

$$E_B = E_{ph} - E_{kin}$$
, eq. 5

The resulting XPS spectrum (intensity signal as a function of the binding energy E_B) features peaks at specific E_B values corresponding to the elements contained in the sample. The intensity of the peaks provides information about the relative concentration of each element in the sample. A process of peak fitting of the XPS spectra can also provide additional information on the local chemical environment of the elements in the sub-surface region of the sample.

In this work, samples analyzed by XPS were made from mirror-polished c-Si wafers. They were cut with a diamond tip into squares of approximately $1\times1~\text{cm}^2$ and fixed on the XPS sample holder with copper tape. XPS measurements were performed with a focused monochromatic Al K_{α} radiation. Spectra were calibrated using the contamination carbon C 1s emission at 285 eV. The XPS spectra were fitted using the CasaXPS software¹. In-depth XPS analyses were also performed by alternating sputtering steps to etch the sample surface (using 1 keV Ar ions) and XPS measurements.

c. Doping profiles in a-Si:H and poly-Si layers

i. Electrochemical Capacitance-Voltage

The Electrochemical Capacitance-Voltage (ECV) technique enables to measure in-depth profiles of electrically active dopants in c-Si materials. The sample surface is put in contact with an NH₄F/HF electrolyte contained in an electrochemical cell (see **Figure 12**). The resulting

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¹ More details on the peak-fitting procedure can be found in **Appendix B.**

interface between the sample and the electrolyte is equivalent to a metal/semiconductor Schottky contact. The in-depth profile is obtained by alternating steps of surface etching and C-V measurements.

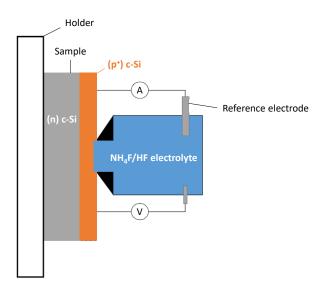


Figure 12. Schematic of an ECV set-up (adapted from ref. [105]).

The surface etching is performed by polarizing the Schottky contact to increase the hole concentration at the sample surface. When the hole concentration is high enough to enable the breaking of covalent bonds, the atoms (Si and dopants) are released in solution, which leads to surface etching. For the measurement of the active dopant concentration, an external voltage is applied, which depletes the c-Si surface of majority carriers (e.g. holes in p-type c-Si) and enables to measure the space charge layer capacitance. The doping concentration is then calculated according to the following equation [112]:

$$N = \frac{-2}{q\varepsilon_0\varepsilon_r A^2 \frac{d(C^{-2})'}{dV}}$$
 eq. 6

with C the capacitance, q the elemental charge, ϵ_0 and ϵ_r the absolute vacuum permittivity and the c-Si relative permittivity, respectively, and A the contact area.

In this work, ECV measurements were carried-out to assess the hole concentration profile of B-doped poly-Si/SiO $_{\rm x}$ contacts fabricated on top of 4" mirror-polished c-Si wafers. The resulting hole concentration profiles were approximated as the active B profile.

However, note that the etching rate implemented for the measurement is calculated for c-Si material. Therefore, active doping profiles measured on poly-Si materials, likely featuring a different etching rate than c-Si, could lead to some measurement errors.

ii. Secondary Ions Mass Spectroscopy

The secondary ions mass spectroscopy (SIMS) technique was used to assess in-depth B, O and H profiles in the a-Si:H and/or poly-Si layers (after deposition and after annealing for crystallization, respectively). The SIMS technique consists in accelerating primary heavy ions

at energies of some keV with a 45° angle to the sample surface. Due to the collisions, surface atoms are ionized and ejected out of the surface. The ejected secondary ions are detected by mass spectroscopy time-of-flight. SIMS provides information about the chemical composition of the sample surface but no details are given on the atomic configuration in the matrix or their doping activity.

In this work, SIMS measurements were performed on samples made from mirror-polished substrates. B profiles were preferentially measured with 500 eV energy O+ ions as primary ions whereas O and H profiles were measured with 1 keV energy Cs+ ions as primary ions. The atom concentration was quantified using a calibration from reference samples. As the analyzed samples consisted of stacks of different materials (e.g. a-Si:H, poly-Si, SiO_x, c-Si), the SIMS etching rate was expected to differ from one layer to another. Therefore, the SIMS sputter time was not converted into thickness.

2. Electronic characterizations

a. Electrical properties of the poly-Si layer: Hall effect technique

The free carrier density, conductivity and carrier mobility in poly-Si layers were assessed by an equipment combining the Hall effect and the van der Pauw techniques.

The Hall effect technique enables to estimate the free carrier density in a material. During the measurement, the sample is submitted to a current I and a magnetic field B with a direction perpendicular to the current flow (see **Figure 13**). In this configuration, the trajectory of free carriers is deviated due to a Lorentz force. It leads to the accumulation of electrons on one side of the sample and of holes on the opposite side. The potential difference resulting from this charge separation (referred to as the Hall voltage) is measured and enables to derive the free carrier density.

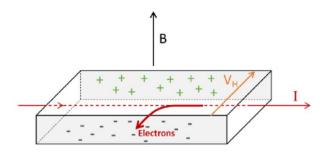


Figure 13. Working principle of the Hall effect technique (taken from ref. [113]).

The van der Pauw technique is coupled to the Hall effect technique to independently assess the conductivity in the sample [112]. From the carrier density (n) measured by Hall effect and the conductivity (σ) measured by van der Pauw, the Hall carrier mobility (μ_{Hall}) can be calculated following: $\mu_{Hall} = \frac{\sigma}{gn}$ (with q the elemental charge).

In this work, the electrical properties of p^+ -doped poly-Si layers were assessed by Hall effect measurements, the poly-Si/SiO_x contact being fabricated on top of n-type mirror-polished c-Si substrates. The samples were prepared by cutting them into squares of 2×2 cm² with a laser.

b. Lifetime measurements: Photo Conductance Decay

The Photo Conductance Decay (PCD) technique enables the determination of the effective minority carrier lifetime τ_{eff} for a wide range of excess charge carrier density Δn [114]. Under certain conditions, it can also provide information about the surface passivation quality of symmetrical samples (i.e. with similar passivation layers on both sides) through the determination of the implied open circuit voltage (iV_{oc}) and the recombination current density at the surface (J₀).

In this work, a WCT-120 Sinton tool was used (see **Figure 14**). During the measurement, a flash illumination is applied to generate extra electron-hole pairs in the sample, increasing its conductance. The light intensity and the conductance are both recorded over time through a reference cell and through a coil (part of an RF-bridge), respectively. The excess carrier density Δn is derived from the photo conductance $\Delta \sigma$ (obtained from the subtraction of the conductance in the dark to the conductance under illumination) according to:

$$\Delta n = \frac{\Delta \sigma}{q(\mu_n + \mu_p)}$$
, eq. 7

with μ_n and μ_p the mobility of electrons and holes, respectively.

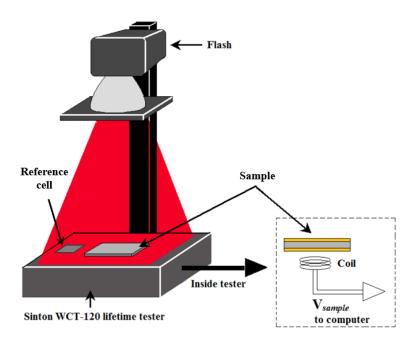


Figure 14. Schematic of an IC-PCD set-up (adapted from [115]).

The lifetime of excess minority carriers is derived from the carrier generation rate G (obtained from the reference cell) following:

$$au_{eff} = rac{\Delta n}{G - rac{d\Delta n}{dt}}.$$
 eq. 8

Then iV_{oc} is calculated according to [114]:

$$iV_{oc} = \frac{kT}{q} \ln\left(\frac{np}{n_i^2}\right),$$
 eq. 9

with n_i the intrinsic carrier concentration.

The effective minority carrier lifetime τ_{eff} represents the combined impact of different competing recombination channels. It can be written as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{intrinsic}} + \frac{1}{\tau_{surf}},$$
 eq. 10

with τ_{SRH} the lifetime related to the Shockley Read Hall recombination process linked to recombination centers in the bulk, $\tau_{intrinsic}$ the lifetime related to intrinsic recombination processes (Auger and radiative recombination) and $\tau_{surface}$ the lifetime related to surface recombination.

It can also be written as [116]:

$$\frac{1}{\tau_{eff}} - \frac{1}{\tau_{intrinsic}} = \frac{1}{\tau_{SRH}} + 2J_0 \frac{(N_{dop} + \Delta n)}{qwn_i^2}.$$
 eq. 11

with N_{dop} the dopant density of the wafer.

This latter expression enables the extraction of J_0 from the slope of the curve plotting $1/\tau_{eff}$ versus Δn after correction from the Auger and radiative contributions and at high excess carrier density $\Delta n >> N_{dop}$ (that ensures that τ_{SRH} is independent of Δn) [116].

In this work, the PCD measurement was performed on symmetrical samples (i.e. with the poly-Si/SiO $_{x}$ contact on both sides) preferentially made from n-type KOH-polished 156psq c-Si wafers. The extracted iV $_{oc}$ and J $_{0}$ values (referred to as "surface passivation properties") were mostly used in **part 3** to assess the quality of surface passivation provided by the poly-Si/SiO $_{x}$ contact in particular during optimization of the processing steps.

The iV_{oc} values were extracted at a constant excess carrier density of 1×10^{15} cm⁻³. The J_0 values were extracted at high excess carrier density (Δn larger than ten times N_{dop}) using the "Lifetime" spreadsheet provided with the WCT-120 tool. The inverse lifetime data was verified to have a linear dependence on the excess carrier density, ensuring an accurate estimation of J_0 .

c. Defect characterization in c-Si: lifetime spectroscopy

Lifetime spectroscopy (LS) enables to characterize electrically active defects in Si materials through standard minority carrier lifetime measurements (using the PCD technique) [117]. The characterization of defects relies on least-square fits of experimental minority carrier lifetime curves based on the Shockley-Read-Hall (SRH) theory of carrier generation and recombination at a defect center.

i. SRH description of an electrically active defect center

Under the assumptions of a defect introducing a single discrete energy level in the bandgap the SRH lifetime τ_{SRH} associated to the defect is given by the following equation:

$$au_{SRH} = rac{ au_{n0}(p_0 + p_1 + \Delta n) + au_{p0}(n_0 + n_1 + \Delta p)}{p_0 + n_0 + \Delta n},$$
 eq. 12

where n_0 and p_0 are the equilibrium concentrations of electrons and holes, τ_{n0} and τ_{p0} are the electron and hole capture time constants, which can be related to the defect density N_t , the thermal velocity v_{th} , and the electron and hole capture cross sections σ_n and σ_p by the following expressions:

$$\tau_{n0} \coloneqq (N_t \sigma_n \nu_{th})^{-1}$$
 , $\tau_{p0} \coloneqq (N_t \sigma_p \nu_{th})^{-1}$ eq. 13

n₁ and p₁ are referred to as the SRH densities and represent the electron and hole concentrations when the Fermi level coincides with the defect energy level E_t:

$$n_1 \coloneqq N_C \exp\left(-\frac{E_C - E_t}{k_B T}\right)$$
 , $p_1 \coloneqq N_V \exp\left(-\frac{E_t - E_V}{k_B T}\right)$ eq. 14

with E_C and E_V the energetic positions at the bottom of the conduction band and top of the valence band, respectively, and N_C and N_V the effective densities of states in the conduction and valence bands.

A defect level can therefore be described by three parameters: the time constant τ_{n0} (or τ_{p0}), the energy level E_t , and a factor of symmetry k defined as:

$$k \equiv \frac{\sigma_n}{\sigma_p} = \frac{\tau_{p0}}{\tau_{n0}}$$
. eq. 15

Introducing eq. 15 in eq. 12 and assuming negligible trapping (i.e. equal excess electron and hole concentrations $\Delta n = \Delta p$) leads to:

$$au_{SRH} = au_{n0} \left(\frac{p_0 + p_1 + \Delta n}{p_0 + n_0 + \Delta n} + k \frac{n_0 + n_1 + \Delta n}{p_0 + n_0 + \Delta n} \right).$$
 eq. 16

ii. Lifetime spectroscopy methods

The injection-dependent lifetime spectroscopy (IDLS) consists in the determination of the defect parameters (E_t , τ_{n0} and k) by fitting eq. 16 to the experimental injection-dependent lifetime curves. However, it is likely that different sets of defect parameters would enable a good fit of eq. 16 to the experimental curve.

The defect parameter solution surface (DPSS) method introduced by Rein [117] consists in finding the pair of values of k and τ_{n0} that enables the best fit between eq. 16 and the experimental curve, for a fixed E_t value across the bandgap.

Figure 15a depicts an example of DPSS analysis of an IDLS curve. The fitted k-factors are plotted together with the least-square fit error for each investigated E_t value. However, one

can observe that the DPSS analysis of a single IDLS curve still results in a broad range of least-square fit minima associated with a broad range of solutions for the defect parameters.

A way to overcome the remaining ambiguity on the defect parameters is to perform the DPSS routine on a set of lifetime curves measured at different temperatures. This method is referred to as temperature- and injection-dependent lifetime spectroscopy (T-IDLS). Superposing the DPSS diagrams obtained from the analysis of a set of T-IDLS curves enables to identify the optimal defect parameters for which the k-DPSS and τ_{n0} -DPSS curves converge into intersection points i.e. for which the relative standard deviation (RSD) of the DPSS-k values is minimized (see **Figure 15b**).

The combined DPSS/T-IDLS routine results in the exact determination of k and τ_{n0} and in the reduction of possible E_t values to two confined regions where the k-DPSS curves intersect.

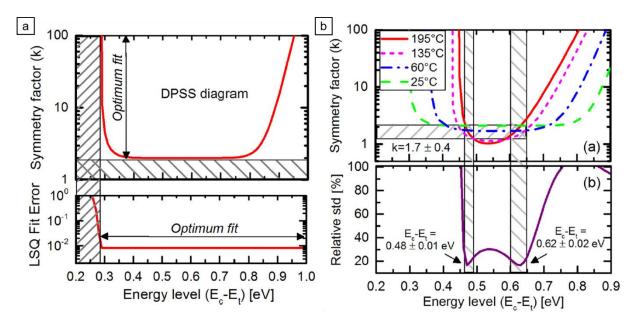


Figure 15. DPSS diagram of a single IDLS curve measured at room temperature (a). DPSS analysis of a set of IDLS curves measured at different temperatures (b). Both Figures are taken from ref. [118].

To confirm the k and τ_{n0} evaluation and determine E_t between the two remaining solutions, the use of an additional spectroscopic method is required (e.g. temperature-dependent LS which focuses on the lifetime data at low injection studied on a broader range of temperature values, or N_{dop} -IDLS which consists in analyzing several IDLS curves measured for different doping densities N_{dop} of the substrate).

iii. Case of several SRH defect centers

If more than one SRH defect is present, the SRH lifetime can be written as follows:

$$\frac{1}{\tau_{SRH}} = \frac{1}{\tau_{D1}} + \frac{1}{\tau_{D2}} + \dots + \frac{1}{\tau_{Dn}}$$
 eq. 17

with τ_{Di} the contribution of the SRH defect number i. To characterize a specific SRH defect, its contribution must first be isolated from the overall SRH lifetime.

In the literature, two kinds of defects are considered:

- Shallow defect centers (featuring an energy level Et near one of the band edges),
 dominating the carrier lifetime at high injection level;
- Deep defect centers (featuring an energy level E_t near midgap), dominating the carrier lifetime at low injection level.

Different methods exist to separate the respective contribution of shallow and deep defects to the SRH lifetime:

- Inglese et al. arbitrarily fix the deep defect parameters and perform IDLS at high injection to first characterize the shallow defect center. Knowing the shallow defect parameters, they can then perform T-IDLS to characterize the deep defect center [118];
- Murphy et al. proposed a method based on a linearization of the SRH contribution [119]. In p-type c-Si, eq. 16 can be simplified as follows:

$$\tau_{SRH} = \tau_{n0} \left(1 + \frac{p_1}{p_0} + k \frac{n_1}{p_0} + X \left(1 - k \frac{n_1}{p_0} - \frac{p_1}{p_0} \right) \right),$$
 eq. 18

with $X=\frac{n}{p}=\frac{\Delta n}{p_0+\Delta n}$. In the case of a single-level defect center, plotting the minority carrier lifetime as a function of $X=\frac{n}{p}$ enables to obtain a linear curve. If more than one defect center is active, several linear curves can be used to fit the experimental data. **Figure 16** depicts an example of such a fit in the case of two active defect centers. In n-type c-Si, one can get a similar equation replacing X by $Y=\frac{p}{n}=\frac{\Delta p}{n_0+\Delta p}$. Thus, plotting the minority carrier lifetime as a function of X or Y (in p- or n-type c-Si, respectively) and fitting the resulting plot with linear curves enables to isolate the respective contribution of several SRH defect centers.

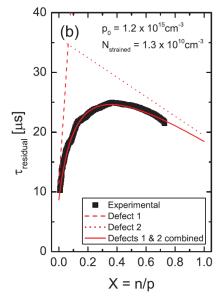


Figure 16. Minority carrier lifetime versus n/p for p-type c-Si samples (taken from ref. [119]).

iv. Bulk and surface contributions to the effective lifetime

In the frame of this study, we will focus on the recombination at the poly-Si/c-Si interface, thus, the surface contribution (τ_{surf}) is of prime interest. The following general expression (eq. 19) was proposed by Grivickas et al [117,120] for approximating τ_{eff} . In this expression, the surface contribution involves both SRH recombination at the surfaces and carrier diffusion towards the surfaces:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \left(\frac{w}{2S} + \frac{1}{D_n} \left(\frac{w}{\pi}\right)^2\right)^{-1},$$
 eq. 19

with w the wafer thickness (in cm) and D_n the diffusion constant (in cm²·s⁻¹). This approximate τ_{eff} solution was shown to deviate by less than 5% from the exact τ_{eff} solution and to be valid for a wide range of S, w and D_n values [121].

The best known expression of τ_{eff} (see eq. 20) is the simplification of eq. 19 in the case of sufficiently low S values (i.e. the carrier diffusion towards the surfaces is not the limiting process and the corresponding term can be neglected). Therefore, assuming "sufficiently well" passivated surfaces, the respective contributions of the surfaces and the bulk can be determined from PCD measurements on identically passivated substrates of different thicknesses. By plotting $\frac{1}{\tau_{eff}} = f(\frac{1}{w})$, S and τ_{bulk} can be extracted from the slope and intercept of the resulting linear curve, respectively².

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S}{w} \qquad \text{for } \frac{Sw}{D_n} < \frac{1}{4}.$$
 eq. 20

This technique will be used in **part 4-III**, where we will show the data obtained on wafers with various thicknesses that had been cut from the same ingot and were processed using the same surface treatments.

v. SRH formalism at the surface

Surface defects contribute in a similar way as bulk defects to the recombination of free carriers. They are usually described by the SRH formalism using a continuous energy distribution throughout the band gap. Thus, the interface trap density $D_{it}(E_t)$ and the capture cross-sections of electrons and holes $\sigma_n(E_t)$ and $\sigma_p(E_t)$ are energy dependent, which needs to be taken into account in an extended SRH formalism [117]. However, if one considers that the surface recombination occurs via a single-level interface state with an energy E_t , the surface recombination rate U_s (in cm⁻² s⁻¹ instead of cm⁻³ s⁻¹ for the bulk recombination rate) can then be expressed as follows [122]:

$$U_{S} = \frac{n_{S}p_{S} - n_{i}^{2}}{\frac{p_{S} + p_{1}}{S_{n0}} + \frac{n_{S} + n_{1}}{S_{n0}}}$$
eq. 21

⁻

 $^{^2}$ In practice this method results in consequent errors for τ_{bulk} due to the extrapolation to infinite wafer thickness leading to the enhancement of small measurement errors.

where n_s and p_s are the electron and hole concentrations at the surface, respectively, defined as:

$$n_{s}=n_{d}\mathrm{exp}\,(rac{qarPsi_{s}}{kT})$$
 , $p_{s}=p_{d}\mathrm{exp}\,(-rac{qarPsi_{s}}{kT})$ eq. 22

with n_d and p_d the bulk values of the concentrations of electrons and holes, and Ψ_s the surface band bending (electrostatic potential difference between the surface and the bulk).

S_{n0} and S_{p0} are the surface recombination velocity of electrons and holes defined as:

$$S_{n0} \equiv \sigma_n \nu_{th} N_{st}$$
 , $S_{p0} \equiv \sigma_p \nu_{th} N_{st}$, eq. 23

with N_{st} the number of interface states per unit area (in cm⁻²).

In analogy to the carrier recombination lifetime in the bulk, a surface recombination velocity S at the c-Si surface can be defined as:

$$U_S \equiv S \cdot \Delta n_S$$
, eq. 24

where Δn_s is the excess minority carrier concentration at the surface.

The presence of a field-effect passivation (and related surface band bending) entails on a strong difference between the surface concentration of electrons and holes. In this case, there is no analytical expression of the surface recombination velocity S, and it can rather be calculated using numerical methods based on eq. 21 [123,124].

By combining eq. 21 and eq. 24, in the case of flat-band conditions at the surface (i.e. $\Psi_s=0$) and negligible trapping ($\Delta n_s=\Delta p_s$), S can be expressed as:

$$S(\Delta n_s) = \frac{n_0 + p_0 + \Delta n_s}{\frac{p_0 + p_1 + \Delta n_s}{S_{n0}} + \frac{n_0 + n_1 + \Delta n_s}{S_{p0}}}.$$
 eq. 25

In the case of well-passivated surfaces (i.e. low S values), we have seen from eq. 20 that the surface lifetime τ_{surf} can be expressed as:

$$\frac{1}{\tau_{surf}} = \frac{2S}{W} . eq. 26$$

From the combination of eq. 25 and eq. 26 it follows:

$$\tau_{SRH,surf} = \frac{\frac{1}{2} \frac{w}{S_{n0}} (p_0 + p_1 + \Delta n_s) + \frac{1}{2} \frac{w}{S_{p0}} (n_0 + n_1 + \Delta n_s)}{n_0 + p_0 + \Delta n_s},$$
 eq. 27

which can also be written:

$$\tau_{SRH,surf} = \frac{1}{2} \frac{w}{S_{n0}} \left(\frac{p_0 + p_1 + \Delta n_s}{n_0 + p_0 + \Delta n_s} + k \, \frac{n_0 + n_1 + \Delta n_s}{n_0 + p_0 + \Delta n_s} \right), \quad \text{eq. 28}$$

when introducing the capture symmetry factor $k = \frac{\sigma_n}{\sigma_n} = \frac{S_{n0}}{S_{n0}}$

The eq. 28 describes the recombination via a single-level interface state at the c-Si surface, similarly as eq. 16 describes the recombination via a single-level bulk defect. In p-type c-Si, eq. 28 can also be written following the work of Murphy et al (see eq. 18):

$$\tau_{SRH,surf} = \frac{1}{2} \frac{w}{S_{n0}} \left(1 + \frac{p_1}{p_0} + k \frac{n_1}{p_0} + X \left(1 - k \frac{n_1}{p_0} - \frac{p_1}{p_0} \right) \right),$$
 eq. 29

with
$$X = \frac{n}{p} = \frac{\Delta n_s}{p_0 + \Delta n_s}$$
.

In n-type c-Si it becomes:

$$\tau_{SRH,surf} = \frac{1}{2} \frac{w}{S_{p0}} \left(1 + \frac{n_1}{n_0} + \frac{p_1}{k p_0} + Y \left(\frac{1}{k} - \frac{p_1}{k n_0} - \frac{n_1}{n_0} \right) \right),$$
 eq. 30

with
$$Y = \frac{p}{n} = \frac{\Delta p_S}{n_0 + \Delta p_S}$$
.

The afore-described extraction of the surface recombination velocity (S) from eq. 19 and eq. 20 and SRH formalism at the surface will be considered in **part 4-III**, to model the recombination phenomena at the interface between the poly-Si contact and the c-Si substrate.

d. Transport of charge carriers in the poly-Si/SiO_x contact: Conductive Atomic Force Microscopy

Conductive atomic force microscopy (C-AFM) is a mode of Atomic Force Microscopy (AFM) that enables to measure simultaneously the topography of the sample surface and a current flow in the sample. The AFM measurement performed in contact mode consists of scanning the sample surface with a tip attached to a cantilever. The force applied between the tip and the sample is kept constant while the deflection of the cantilever is measured with an optical system consisting of a laser and a photodiode (see **Figure 17**), resulting in a topography map of the sample surface. In C-AFM mode, an additional voltage is applied between the tip and a second contact placed on the sample. It enables to generate a current map associated to the topography map obtained by AFM.

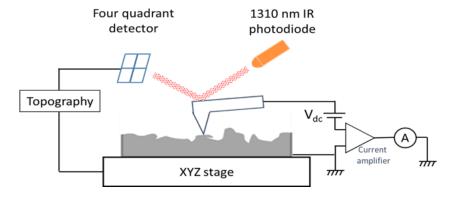


Figure 17. Schematic of a C-AFM set-up.

In this work, C-AFM measurements were performed on mirror-polished samples, in contact mode, using PtSi force modulation tips placed at the poly-Si surface, under air and dark conditions. A polarization of -1 V was applied between the tip and the second contact to limit the oxidation of the sample surface and to measure the current in reverse of the diode. C-AFM measurements were performed in two different configurations:

- In transversal configuration i.e. with the voltage applied between the AFM tip and a silver contact located at the back side of the c-Si;
- In lateral configuration i.e. with the voltage applied between the AFM tip and a silver contact localized at the poly-Si surface (implying that the current does not need to go through the poly-Si/SiO_x and SiO_x/c-Si interfaces).

The resulting current maps were analyzed using the software ImageJ to assess the density of conductive spots.

Part 3: Fabrication of the poly-Si/SiO_x contact

I. Optimization of the in-situ doped poly-Si/SiO_x contact

In this part we will focus on poly-Si/SiO $_x$ contacts through the deposition of an in-situ doped a-Si:H(B) layer by PECVD on top of a thin SiO $_x$ layer and followed by an annealing step. More particularly, we will first elaborate on the optimization of the deposition conditions of the a-Si:H(B) layer to obtain blister-free poly-Si(B) layers providing stable surface passivation properties after annealing. Then, we will address the impact of the annealing step on the crystallinity and doping of the poly-Si layer as well as on the passivation properties of the resulting poly-Si/SiO $_x$ contact.

1. Optimization of the deposition conditions for blister-free poly-Si(B) layers

Several studies have shown that poly-Si/SiO_x contacts fabricated by PECVD of a-Si:H layers on top of SiO_x are prone to blistering [19,21,22]. The blistering phenomenon is observed during both deposition of the a-Si:H layer and subsequent annealing for poly-Si crystallization. Even though a fundamental understanding of the phenomenon is still lacking, some hypotheses have been proposed. Blistering during PECVD might be related to adhesion properties of the a-Si:H film to the SiO_x layer coupled with a high amount of H incorporated in the layer, leading to the accumulation of H₂ molecules at the a-Si:H(B)/SiO_x interface [125]. Blistering during the annealing step is likely due to rapid release of H₂ at high temperature [126]. As a consequence, a severe degradation of the final poly-Si layer is observed if the deposition and annealing conditions are not optimized [21,22].

In this part, we address the optimization of the deposition temperature and gas flow ratio in order to minimize the incorporation of H in the a-Si:H(B) layer, reducing therefore blistering of the final poly-Si(B) layer. The poly-Si contact was fabricated on 4" mirror-polished n-type c-Si wafers (see **part 2-I** for more details on the process). The annealing step was systematically carried out at $T_a = 700$ °C.

The contact was fabricated either on a single side of the wafer for spectroscopic ellipsometry, optical microscope and Hall effect characterizations or on both sides (referred to as "symmetrical samples") for PCD characterization.

a. Effect of the deposition temperature increase

As a first step, 30 nm-thick a-Si:H(B) layers were deposited on top of SiO_x using a deposition temperature $T_{dep} = 220$ °C and a gas ratio $R = H_2/SiH_4 = 6$. Such deposition conditions resulted in a severe blistering of the layer after both deposition and annealing (see **Figure 18**, Step 1). The first way to minimize the incorporation of H in the a-Si:H(B) layer was to increase the deposition temperature (T_{dep}) leading to the reduction of H incorporation in the deposited layer [126,127]. In this study, the increase of T_{dep} from 220°C to 300°C (limit of the PECVD equipment) enabled to reduce the diameter of blisters from 20 µm to 8 µm after deposition

and from 30 μ m to 13 μ m after annealing (see **Figure 18**, ①). However, the blister density remained unchanged (1.5 mm⁻²).

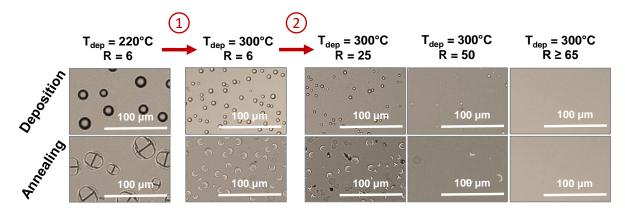


Figure 18. Optical microscope images of a-Si:H(B) layers after deposition and poly-Si(B) layers after annealing at $T_a = 700^{\circ}\text{C}$ (at a ×20 magnification). The deposition conditions were varied: ① Increase of the deposition temperature T_{dep} , ② Increase of the gas flow ratio $R = H_2/\text{SiH}_4$. For each set of conditions, the diameter of the blisters and their density were evaluated using the software ImageJ.

b. Effect of the silane dilution in dihydrogen

The second way to reduce the blistering was to increase the SiH₄ dilution in H₂ (i.e. increase of the gas flow ratio R = H₂/SiH₄) during the deposition step, as reported by Nemeth et al in ref. [21]. The increase of R led to a reduction of the blister density after deposition and after annealing, from 1.5 mm⁻² to 0.6 mm⁻² for R from 6 to 50, respectively (see **Figure 18**, ②). The further increase of R to 65 enabled to obtain blister-free poly-Si(B) layers. However, the blistering mitigation was obtained at the expense of the deposition rate (see **Figure 19a**). Indeed, the decrease of the deposition rate likely enables the H atoms to diffuse toward the layer top surface during deposition, thus reducing the blistering phenomenon. **Figure 19a** also depicts iV_{oc} as a function of the gas ratio R. For R = 25 to R = 50, an increase of iV_{oc} of 90 mV was observed, likely resulting from blistering reduction. For higher R values (> 50), iV_{oc} dropped by 20 mV. This drop was attributed to the excessive H₂ concentration in the plasma that damaged the thin SiO_x layer (either by etching [128] or by causing radiation induced charges in the SiO_x layer [129,130]).

In conclusion, an optimal gas ratio of R = 50 was found to reduce the blister density (0.6 mm⁻² for a 30 nm-thick poly-Si layer) and preserve decent iV_{oc} values after annealing. The remaining blistering was avoided by decreasing the thickness of the poly-Si(B) from 30 nm down to 25 nm, which resulted in blister-free layers. Therefore, the optimal deposition conditions retained for the following studies on the in-situ doped poly-Si/SiO_x contact are the followings: $\{T_{dep} = 300^{\circ}C; R = 50; poly-Si thickness of 20-30 nm\}$.

c. Evaluation of the poly-Si electrical properties through deposition optimizations

In this paragraph, we focus on the conductivity and carrier mobility of the poly-Si layer over T_{dep} and $R = H_2/SiH_4$ optimizations. The lateral conductivity and carrier mobility of 30 nm-thick poly-Si(B) layers were evaluated by Hall effect measurements as functions of T_{dep} and R, after annealing at $T_a = 700$ °C (see **Figure 19b**). For the different T_{dep} and R conditions investigated

in this work, we measured constant Hall carrier density of $1.1\pm0.2\times10^{20}$ cm⁻³. Consequently, the carrier mobility dominated the poly-Si(B) conductivity trend (see **Figure 19b**). The poly-Si(B) average conductivity increased from $160 \text{ S} \cdot \text{cm}^{-1}$ for $\{T_{dep} = 220^{\circ}\text{C}; R = 6\}$ to $220 \text{ S} \cdot \text{cm}^{-1}$ for $\{T_{dep} = 300^{\circ}\text{C}; R = 50\}$. This increase could result from the reduction of the poly-Si(B) blistering leading to a better lateral transport of charge carriers through the layer.

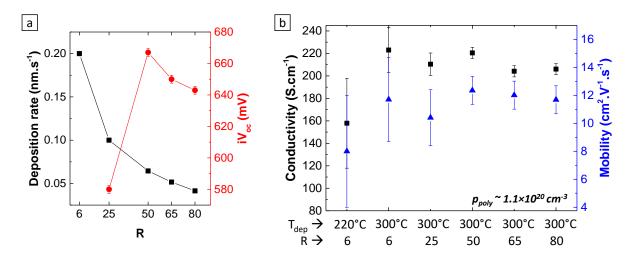


Figure 19. Deposition rate of the a-Si:H(B) layers and iV_{oc} (measured on symmetrical samples made from 4" mirror-polished c-Si wafers) as functions of the deposition gas flow ratio R = H₂/SiH₄ (a). Conductivity and carrier mobility of 30 nm-thick poly-Si(B) layers as functions of the deposition temperature (T_{dep}) and gas ratio (R) (b).

It is to note that the Hall effect technique rely on the thickness measurement by ellipsometry of the poly-Si layer. The significant uncertainty on the thickness of highly blistered poly-Si layers resulted in significant error bars for the electrical properties assessed by Hall effect. For $T_{dep} = 300^{\circ}\text{C}$ and $R \geq 50$, the blistering of the poly-Si layer decreased, leading to a decreased uncertainty on the thickness and, therefore, on the electrical properties of the layer.

d. Effect of the blistering on the stability of surface passivation

To study the impact of blistering on the surface passivation stability over time, symmetrical samples were made from mirror-polished 4" c-Si wafers using two values of the PECVD gas ratio R = SiH₄/H2 (= 25 or 50) and targeting two different poly-Si thicknesses (15 and 30 nm). It resulted in poly-Si(B) layers with different blister densities ranging from 0 to 1.1 mm⁻² after annealing at $T_a = 700$ °C. **Figure 20** depicts optical microscope images of the resulting layers (see insets) and plots the iV_{oc} measured right after samples processing, after 24 hours, and after 2 months of storage in the dark, under air. On **Figure 20**, one can observe the following trends:

Samples featuring 30 nm-thick poly-Si layers deposited with R = 25 exhibited the highest blister density. As a result, they showed the lowest initial passivation level and poorest stability (the initial iV_{oc} value of 600 mV decreased down to 540 mV after 2 months of storage);

- For R = 25, the reduction of the poly-Si thickness down to 15 nm led to a decrease of the blister density, enhancing the initial iV_{oc} value (660 mV), but it did not solve the lack of stability previously observed as iV_{oc} dropped to 620 mV after 2 months;
- For R = 50, samples with a 30 nm-thick poly-Si exhibited an initial iV_{oc} value of 665 mV, which slightly decreased to 660 mV after 2 months;
- For R = 50, the reduction of the poly-Si thickness to 15 nm enabled to obtain not only the highest initial iV_{oc} value (670 mV) but also an excellent stability of the carrier effective lifetime and iV_{oc} after 2 months.

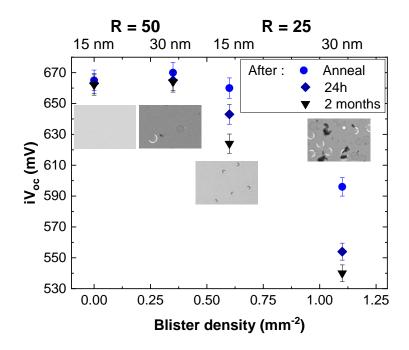


Figure 20. iV_{oc} of symmetrical samples featuring poly-Si/SiO_x contacts measured after annealing ($T_a = 700$ °C), after 24h and after 2 months of storage, as a function of the blistering density of the poly-Si layer. The poly-Si layers were fabricated using different sets of deposition conditions (gas ratio $R = H_2/SiH_4 = 25$ or 50 and poly-Si thickness = 15 or 30 nm), which resulted in different blister densities. Insets are top views of the poly-Si layer taken with an optical microscope (x 20 magnification).

These results show that the blister density is playing a role on the stability of the surface passivation over time: only poly-Si(B) layers deposited with the optimized ratio R = 50 (i.e. blister density < 0.35 mm⁻²) showed an acceptable stability.

In the following of this chapter, the optimized deposition conditions: $\{T_{dep} = 300^{\circ}C, R = H_2/SiH_4 = 50, poly-Si thickness of 20-25 nm\}$ will systematically be used to ensure blister-free poly-Si layers providing stable surface passivation over time.

2. Crystallization and doping of the poly-Si layer

In the fabrication process of the poly-Si contact, the annealing step performed after deposition aims at crystallizing the as-deposited Si-based layer thus stabilizing the poly-Si contact against following back-end process steps at high temperature. The thermal budget applied is also suitable for dopant activation. In this section, we will elaborate on the evolution of the crystallization and doping of our poly-Si(B) layer after annealing at different temperatures.

In the following, in-situ doped poly-Si(B)/SiO_x contacts were fabricated on a single-side of 4" mirror-polished c-Si wafers. The a-Si:H(B) layers were deposited with the afore-defined optimal deposition conditions { $T_{dep} = 300^{\circ}$ C, R = 50, poly-Si thickness of 20-25 nm}. The annealing temperature T_a was varied in the range 700-900°C.

a. Crystallization of the poly-Si layer

The imaginary part of the dielectric function (ϵ_i) obtained as a function of the photon energy (E_{ph}) through spectroscopic ellipsometry measurements was used to assess the crystallinity of 25 nm-thick a-Si:H(B) and poly-Si(B) layers after deposition and after annealing, respectively (see **Figure 21**).

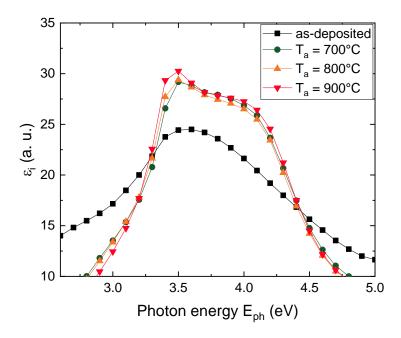


Figure 21. Imaginary part of the dielectric function (ε_i) vs. photon energy (E_{ph}) , from spectroscopic ellipsometry measurements performed on a 25 nm-thick a-Si:H(B) layer after deposition and on poly-Si(B) layers after annealing in the range $T_a = 700-900^{\circ}$ C.

After deposition of the a-Si:H(B) layer, the signal featured a broad peak centered around 3.3 eV which is characteristic of an a-Si phase [109]. It is to note that the use of a high gas flow ratio $R = H_2/SiH_4 = 50$ during PECVD of hydrogenated Si-based layers usually results in the deposition of microcrystalline layers [131]. However, here, the deposited layer was in-situ doped with B, which promotes the amorphous nature of the deposited layer and is likely to explain why the layer remained amorphous [132]. After annealing at $T_a = 700^{\circ}$ C, the signal featured two peaks centered around 3.4 eV and 4.2 eV, indicating the crystallization of the layer into a poly-Si phase. Then, the ϵ_i versus E_{ph} signal remained constant with increasing T_a from 700° C to 900° C.

Similar samples were also characterized by TEM, to observe the local microstructure of the layer after deposition and after annealing in the range 700-900°C (see **Figure 22**). TEM observations after deposition confirmed the amorphous nature of the deposited layer (see **Figure 22a**). After annealing at $T_a = 700$ °C, the layer featured crystalline domains in the range

5-10 nm with random crystalline orientations. These observations are consistent with other TEM analyses of poly-Si layers fabricated through the deposition of a-Si:H layers by PECVD, which are likely to crystallize through the growth of randomly oriented nanometric domains in the amorphous matrix [12,89,133]. After annealing at $T_a = 800^{\circ}\text{C}$ and 900°C, the poly-Si crystalline structure remained identical, with randomly oriented crystalline domains of similar size. Therefore, it seems that the crystallinity of the poly-Si layer does not significantly evolve when varying T_a in the range 700-900°C. Note that the lamella prepared for TEM were approximately 10 μ m long, therefore conclusions are obtained here at a very local scale. However, TEM observations corroborate well with ellipsometry macroscopic results, which also showed the crystallization of the layer for $T_a \ge 700^{\circ}\text{C}$ and a constant ϵ_i versus E_{ph} signal for T_a in the range 700-900°C (see **Figure 21**).

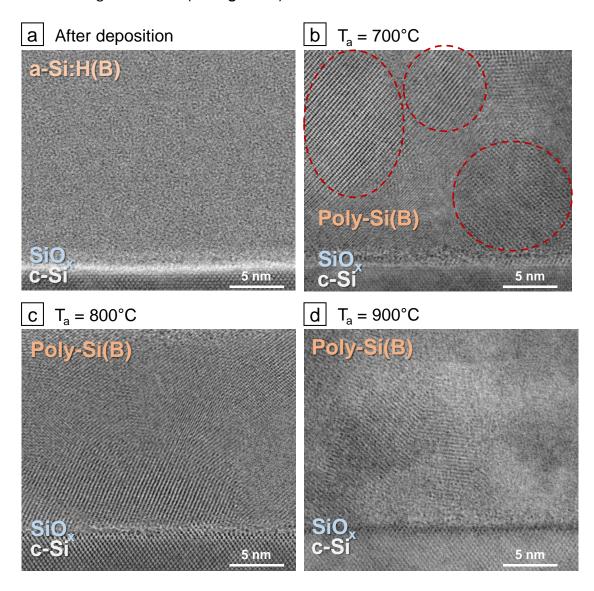


Figure 22. TEM observations of a a-Si:H(B) layer after deposition (a) and poly-Si(B) layers after annealing at $T_a = 700^{\circ}\text{C}$ (b), 800°C (c) and 900°C (d).

It is to note that the Focus Ion Beam (FIB) preparation of the samples before TEM observations could have induced an "artificial" crystallization of the Si-based layers. However, we verified

that the a-Si:H(B) layer showed no crystallized domain along the lamella prepared for TEM, so we can assume that it remained amorphous through the FIB preparation process. Therefore, we consider that the sample preparation did not significantly affect the poly-Si layers crystallinity before TEM observations.

X-Ray Diffraction (XRD) analyses were also performed to independently verify the TEM results. However, XRD signal of a 20 nm-thick poly-Si layer was not detected due to the strong background signal of the c-Si substrate. Therefore, specific samples were fabricated by performing three consecutive sequences of 20 nm-thick a-Si:H(B) deposition plus annealing ($T_a = 800^{\circ}\text{C}$), which resulted in a 60 nm-thick poly-Si stack³. The XRD measurement of the 60 nm-thick stack confirmed the polycrystalline nature of the layer with randomly oriented domains of 14 nm on average. Note that the higher size of the crystalline domains estimated by XRD compared to TEM could arise from the three consecutive annealing steps performed on the sample analyzed by XRD.

b. Doping of the poly-Si layer

The hole concentration profile was measured on samples featuring 25 nm-thick poly-Si(B) layers by means of ECV after annealing at various T_a (see **Figure 23**).

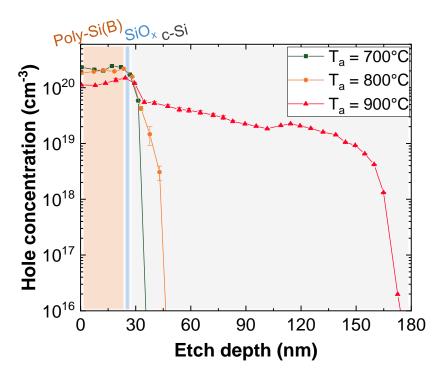


Figure 23. Hole concentration profiles measured by ECV on poly-Si contacts after annealing at T_a in the range 700-900°C. The poly-Si contacts were fabricated on a single side of 4" mirror-polished c-Si wafer targeting 25 nm-thick poly-Si layers.

For $T_a = 700$ °C, we observed a constant carrier density of $1.8\pm0.2\times10^{20}$ cm⁻³ in the poly-Si layer followed by a steep doping gradient when reaching the c-Si interface. To comfort ECV profiles,

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³ This three-sequences process enabled to avoid blistering that would have occurred with a single deposition of a 60 nm-thick a-Si:H(B).

we performed Hall effect measurements on similar samples. For $T_a = 700^{\circ}\text{C}$, we measured a Hall carrier density of $1.2\pm0.2\times10^{20}$ cm⁻³, which is in good agreement with the carrier density evaluated by ECV⁴.

The poly-Si conductivity and mobility assessed by Hall effect measurements were equal to 218.6 S·cm and 15.6 cm²·V⁻¹·s⁻¹, respectively. The order of magnitude of the values of the poly-Si carrier density, conductivity and mobility found in this work are in good agreement with values expected from the literature on electrical properties of poly-Si materials [134–136].

For $T_a = 800^{\circ}\text{C}$ and 900°C , we also observed a carrier density plateau measured by ECV in the poly-Si layer around $1.7\pm0.2\times10^{20}$ cm⁻³ and $1.15\pm0.2\times10^{20}$ cm⁻³, respectively (see **Figure 23**). Moreover, the increase of T_a to 800°C and 900°C resulted in the diffusion of B atoms in the c-Si substrate (20 nm and 137 nm-deep respectively). The slightly lower carrier density observed in the poly-Si layer annealed at $T_a = 900^{\circ}\text{C}$ could result from the significantly deeper diffusion of B in the c-Si substrate, the B source being limited here due to in-situ doping. Due to the diffusion of B in the c-Si, the evaluation of the poly-Si electrical properties by Hall effect measurements was biased for $T_a = 800^{\circ}\text{C}$ and 900°C because of current flowing in the p⁺-doped region of the c-Si (not reported here).

The total B concentration profile in a 20 nm-thick a-Si:H(B) layer and in the poly-Si layer were measured by SIMS before and after annealing at $T_a = 800^{\circ}$ C, respectively. The resulting SIMS profiles as well as the hole (approximated as active B) concentration profile measured by ECV on the same sample after annealing are depicted in **Figure 24**. After deposition, one can observe a total B concentration plateau of 10^{21} cm⁻³ in the a-Si:H(B) layer and a steep decrease of the B concentration at the c-Si interface.

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 $^{^4}$ Note that the etching rate implemented for the ECV measurement is calculated for c-Si material, which can lead to significant errors on ECV profiles obtained in poly-Si layers. However, in this case the ECV profile obtained for $T_a = 700^{\circ}$ C was in good agreement with both the poly-Si thickness and carrier density assessed by ellipsometry and Hall effect, respectively. Therefore, in this work, we consider that the ECV measurement accurately estimates the hole concentration in in-situ doped poly-Si layers.

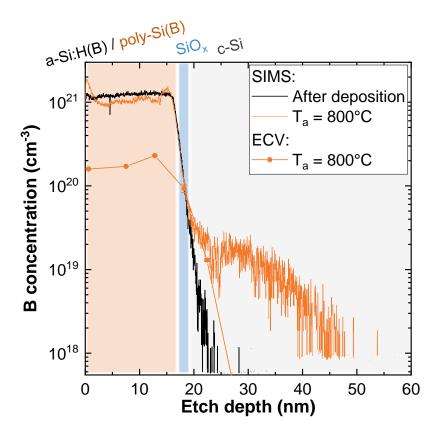


Figure 24. Total B concentration profile measured by SIMS on a sample after deposition of a 20 nm-thick a-Si:H(B) layer and on the same sample after annealing at T_a = 800°C. The hole (approximated as active B) concentration profile measured by ECV on the same sample after annealing at T_a = 800°C is also depicted.

From the comparison of total and active B concentration profiles (measured by SIMS and ECV, respectively) after annealing, one can observe:

- A partial activation of B doping in the poly-Si layer, with only 20% of the total B concentration being activated;
- An accumulation of B at the poly-Si top surface and at the c-Si interface measured by SIMS but not observed on the ECV profile;
- A slightly deeper B diffusion tail in the c-Si measured by SIMS compared to the one measured by ECV (approximately 25 nm and 10 nm-deep, respectively).

Firstly, the active doping concentration have been seen to be inferior than the total doping in poly-Si layers [134–136]. The inactive doping concentration could correspond to dopants segregating at poly-Si GBs [137] or to dopants remaining inactive in the crystalline domains due to the solubility limit being reached.

Secondly, note that the SiO_x layer depicted on **Figure 24** is only indicative. Thus, the difference of B diffusion length (of approximately 15 nm) observed between SIMS and ECV profiles could arise from a misalignment of the profiles due to the respective etch depth error of the two techniques. Moreover, the evaluation of steep doping gradient by SIMS is known to be challenging due to measurement artifacts (e.g. knock-on effects), which could explain the

deeper B diffusion length observed by SIMS. However, such effects did not affect the SIMS measurement after deposition, which showed a steep doping profile at the c-Si interface. Therefore, it seems reasonable to assume that it did not affect the SIMS measurement after annealing either.

Finally, the accumulation of B measured by SIMS at the poly-Si/c-Si interface after annealing was also reported by other groups [16,82]. It could arise from a lower diffusivity of B in the SiO_x compared to the one in poly-Si, leading to inactive B atoms piling-up at the poly-Si/SiO_x interface [17,18]. Note that this phenomenon was not observed on Ga-doped poly-Si contacts, thus, it could explain the lower surface passivation properties obtained with B-doped poly-Si/SiO_x contacts compared to their Ga-doped counterparts [16].

3. Surface passivation properties of the in-situ doped poly-Si(B)/SiO_x contact

a. Impact of the annealing temperature

The surface passivation properties provided by the in-situ doped poly-Si(B) contact were then evaluated as functions of the annealing temperature. Symmetrical samples were fabricated from 156 psq KOH-polished c-Si wafers (ρ = 5-6 Ω ·cm), which corresponds to the area and topography targeted for device integration of the poly-Si(B) contact. **Figure 25** depicts the average iV_{oc} and J₀ values measured after annealing at various temperature T_a in the range 700-850°C (on five samples per investigated T_a value). For T_a from 700°C to 800°C, iV_{oc} increased from 661 mV to 689 mV and J₀ decreased from 75 to 31 fA·cm⁻². For T_a = 850°C, iV_{oc} decreased to 664 mV and J₀ increased to 82 fA·cm⁻². An optimal T_a of 800°C was found to obtain the best surface passivation (i.e. highest iV_{oc} and lowest J₀) after annealing.

Note that the PCD technique was applied on 5 points per sample to evaluate the spatial homogeneity of the surface passivation properties after annealing. A spatial dispersion of 3 mV and $2.5 \, \text{fA} \cdot \text{cm}^{-2}$ was evaluated for iV_{oc} and J_0 , respectively, showing the good homogeneity of the poly-Si(B)/SiO_x fabrication process on large area c-Si substrates.

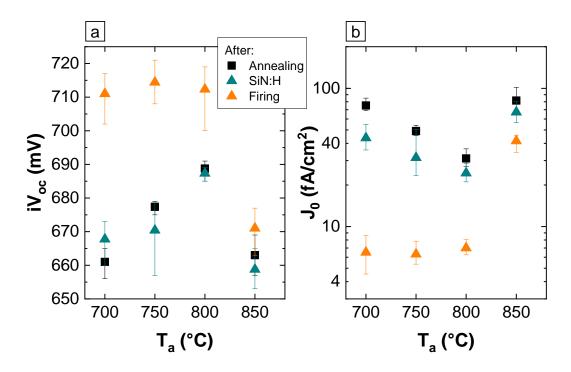


Figure 25. Surface passivation properties (iV $_{oc}$ (a) and J $_{0}$ (b)) provided by the poly-Si(B)/SiO $_{x}$ contact as functions of the annealing temperature $T_{a,}$ evaluated on symmetrical samples (made from KOH-polished 156psq c-Si wafers) after annealing, SiN:H deposition and firing (with 20 nm-thick poly-Si layers).

b. Impact of the hydrogenation step

The surface passivation properties were evaluated after deposition of the SiN:H layer on top of the poly-Si(B) (both sides), and after subsequent firing step (see **Figure 25**). More details on the hydrogenation process can be found in **part 2-I**. The SiN:H deposition did not significantly affect the iV_{oc} value over the entire T_a range although slightly decreasing the J_0 values. For every sample annealed at $T_a \le 800^{\circ}\text{C}$, performing a subsequent firing step resulted in an increase of iV_{oc} above 700 mV as well as a decrease of J_0 below 10 fA·cm⁻². A maximum iV_{oc} of 721 mV was reached for $T_a = 750^{\circ}\text{C}$, corresponding to a J_0 value of 5.3 fA·cm⁻². After firing, one can note that the lower the T_a the greater the absolute gain in iV_{oc} and J_0 .

By fabricating symmetrical samples using similar c-Si wafers with a lower resistivity ($\rho = 2-3~\Omega\cdot\text{cm}$), an average iV_{oc} of 731 mV was obtained after annealing at T_a = 700°C with a maximum of 734 mV (associated to J₀ = 7 fA·cm⁻²). This result is, to the author's knowledge, among the best values obtained so far with p⁺-poly-Si symmetrical samples on planar surface (in the range 732-735 mV and 1-10 fA·cm⁻² for iV_{oc} and J_o, respectively) [13,14,16,52].

The integration of the poly-Si(B) contact at the rear side of a p-type solar cell with a full area rear metallization implies the removal of the SiN:H layer prior to the metal deposition. Therefore, the chemical etching of the SiN:H layer was performed by dipping the samples in a concentrated HF solution for a few minutes. An average loss of iV_{oc} of less than 4 mV was estimated on all the investigated T_a range.

II. Ex-situ doping of the poly-Si/SiO_x contact

This part will focus on the development of ex-situ doped poly-Si/SiO $_x$ contacts. As a first step, we optimized the deposition of intrinsic Si layers by PECVD. Then, we investigated the impact of the ex-situ doping process on the poly-Si layer's microstructure and doping profile. We then compared the resulting ex-situ doped poly-Si/SiO $_x$ contact with the in-situ doped one (described in the previous section). Finally, we studied the surface passivation properties obtained with the poly-Si/SiO $_x$ contact, ex-situ doped or not, in order to investigate the respective effect of the passivation mechanisms related to the SiO $_x$ layer and the poly-Si high doping concentration.

1. Deposition of the intrinsic Si layer by PECVD

In this section, we elaborate on the development of intrinsic Si layers deposited by PECVD. Samples were fabricated from 4" mirror-polished c-Si wafers. The thin SiO_x layer was grown by DIO_3 followed by the deposition of the Si layer by PECVD with various values of the B_2H_6 flow and gas ratio $R = H_2/SiH_4$. An annealing step was subsequently performed at $T_a = 700^{\circ}C$ to form the poly-Si/SiO_x contact. The contact was fabricated on a single-side of 4" mirror-polished c-Si wafer for spectroscopic ellipsometry, Hall effect and ECV characterizations, and on both sides of similar wafers for PCD measurements.

a. Decrease of the in-situ B-doping

Our development of intrinsic Si layers by PECVD was based on the optimal deposition parameters of the a-Si:H(B) layer ($T_{dep} = 300^{\circ}$ C, $R = H_2/SiH_4 = 50$, B_2H_6 flow = 200 sccm). We first deposited 25 nm-thick a-Si:H(B) layers with decreasing values of the B_2H_6 gas flow (from 200 sccm to 30 sccm), in order to:

- Investigate the effect of the B-doping decrease on the properties of the final poly-Si layer. As B is known to impede the crystallization of the Si-based deposited layer [132], a B-doping decrease could lead to a larger grain size and an enhanced carrier mobility in the poly-Si layer;
- Tend to the structure of an intrinsic poly-Si layer, as the characterization of such layers by Hall effect measurement will then not be possible.

Figure 26a depicts the free-charge carrier (hole) concentration measured by the Hall effect technique after annealing at $T_a = 700$ °C. As expected, the decrease of the B_2H_6 flow from 200 sccm to 30 sccm led to a decrease of the poly-Si charge carrier concentration from 1×10^{20} cm⁻³ to 2.6×10^{19} cm⁻³. Note that a further decrease of the carrier concentration could have been achieved by increasing other precursor gases to dilute the B_2H_6 .

Figure 26b depicts the extracted poly-Si conductivity and mobility as functions of the hole concentration (after annealing at $T_a = 700^{\circ}$ C). For comparison, the conductivity and mobility in B-doped c-Si derived from the model of Klaassen [138,139] are also plotted in **Figure 26b** (black and blue lines, respectively).

One can observe an overall increase of the charge carrier mobility with decreasing hole concentration in the poly-Si layer, in good agreement with results reported in [134,140]. However, the mobility versus hole concentration trend was not linear. One can note a slight increase of the mobility from 12.3 cm²·V⁻¹·s⁻¹ to 14.5 cm²·V⁻¹·s⁻¹ for a concentration from 1×10²⁰ cm⁻³ to 4.1×10¹⁹ cm⁻³, followed by a more pronounced increase of the mobility for concentrations lower than 4.1×10¹⁹ cm⁻³. As the addition of B in the layer during deposition is playing a major role on its crystalline structure after deposition (and therefore after annealing) [132], the jump of mobility at low carrier concentration could result from a change of the layer's microstructure due to decreasing in-situ doping (e.g. larger grain size).

The poly-Si conductivity was shown to decrease from 200 S·cm⁻¹ to 100 S·cm⁻¹ for a hole concentration from 1×10^{20} to 4.1×10^{19} cm⁻³, followed by an increase up to 130 S·cm⁻¹ for 2.6×10^{19} cm⁻³. The initial decrease of conductivity likely results from the decrease of hole concentration while the following increase of conductivity must arise from the jump of mobility that overcompensates the carrier concentration decrease.

One can also observe that, for a given carrier concentration, the carrier mobility and conductivity measured in the poly-Si layer were significantly lower than values expected in B-doped c-Si. This difference is generally explained by the presence of trapping-states at the poly-Si grain boundaries (GBs) that would: 1) decrease the overall free charge carrier concentration in the poly-Si layer and 2) involve a potential energy barrier at the GB that decreases the carrier mobility in poly-Si [134,135,141].

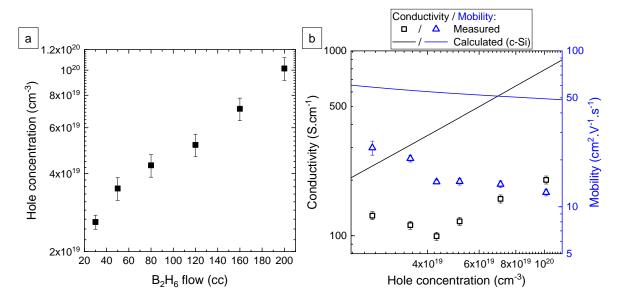


Figure 26. Hole concentration in 25 nm-thick poly-Si layers measured by the Hall effect technique after annealing at $T_a = 700^{\circ}\text{C}$ as a function of the B_2H_6 gas flow used during deposition of the layer (a). Conductivity and mobility of the poly-Si layer ($T_a = 700^{\circ}\text{C}$) as function of the hole concentration (b). In (b) is also depicted the conductivity and mobility in B-doped c-Si derived from [138,139].

Hole concentration profiles were measured by ECV on similar samples featuring poly-Si layers deposited with decreasing values of the B_2H_6 flow (see **Figure 27**). Note that the ECV measurement was not possible for $T_a = 700^{\circ}\text{C}$ due to a too high contact resistance between

the probe and the sample. Therefore, ECV was performed after annealing at $T_a = 800^{\circ}\text{C}$ for B_2H_6 flow values from 200 sccm to 80 sccm⁵. In **Figure 27**, one can observe a decreasing hole concentration in the poly-Si layer with decreasing B_2H_6 flow, which is in good agreement with Hall effect measurements presented **Figure 26a**.

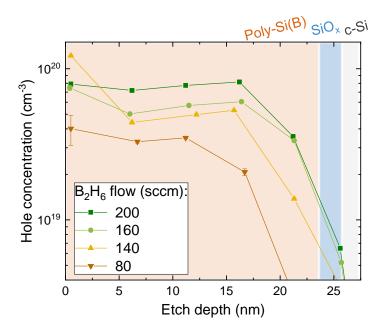


Figure 27. Hole concentration profiles measured by ECV on 25 nm-thick poly-Si layers deposited with various values of B_2H_6 flow after annealing at $T_a = 800$ °C.

The surface passivation properties were also evaluated through the decrease of the B_2H_6 flow value (on symmetrical samples made from 4" mirror-polished c-Si wafers). The resulting iV_{oc} and J_0 values are plotted in **Figure 28** as functions of the poly-Si carrier concentration.

For a hole concentration from 1×10^{20} cm⁻³ to 5.2×10^{19} cm⁻³, the iV_{oc} and J₀ values remained constant (665 mV and 72 fA·cm⁻², respectively). For hole concentration lower than 4.3×10^{19} cm⁻³, iV_{oc} decreased down to 640 mV and J₀ increased up to 180 fA·cm⁻². This loss of passivation could result from a weaker field-effect passivation of the c-Si interface due to the decreasing doping of the poly-Si layer, as hypothesized in ref. [30]. Nogay et al similarly studied the impact of their doping gas flow (trymethylboron (TMB)) on the surface passivation properties of the poly-Si/SiO_x contact [19]. They observed that low-doped poly-Si layers required a higher annealing temperature to improve the surface passivation, which they attributed to a strengthened field-effect passivation related to an enhanced B diffusion in the c-Si substrate.

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 $^{^5}$ For $B_2H_6 < 80$ sccm, the probe/sample resistance was again too high.

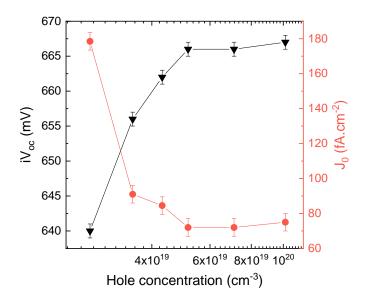


Figure 28. Surface passivation properties (iV_{oc} ; J_0) provided by the poly-Si/SiO_x contact as functions of the hole concentration in the poly-Si layer. The surface passivation properties were measured by PCD on symmetrical samples after annealing at $T_a = 700$ °C.

In conclusion, reducing the B_2H_6 flow from 200 sccm to 30 sccm led to a decrease of the poly-Si carrier concentration from 10^{20} cm⁻³ to 2.6×10^{19} cm⁻³. It was coupled with a decrease of the poly-Si conductivity and an increase of the carrier mobility. For carrier concentrations lower than 5.2×10^{19} cm⁻³ the surface passivation degraded, which was attributed to a loss of field-effect passivation.

b. Optimization of the intrinsic Si layer

In a second step, we removed B_2H_6 from the PECVD precursors in order to deposit an intrinsic Si layer. The ratio $R = H_2/SiH_4$ is known to play an important role on the morphology of the Si layer grown by PECVD [127,131]:

- Low R values (i.e. low H₂ dilution) promote the deposition of amorphous layers whereas high R values (i.e. high H₂ dilution) promote the fabrication of microcrystalline (μc) layers. The transition from a-Si:H to μc-Si depends on the deposition conditions (e.g. substrate, layer's thickness) [131];
- Reproducible deposition of μ c-Si layers by PECVD is known to require extreme caution in terms of chamber and electrode conditioning [142].

We investigated the impact of the gas flow ratio $R = H_2/SiH_4$ on the microstructure, the blistering and the reproducibility of the intrinsic Si layer deposited by PECVD. The ratio R was varied in the range of 5-50, while the other parameters were kept constant ($T_{dep} = 300^{\circ}C$, layer thickness of 25 nm). The microstructure and the blister density of the Si layer were evaluated by spectroscopic ellipsometry and optical microscopy, respectively, both after deposition and after annealing at $T_a = 700^{\circ}C$. The process reproducibility was assessed by performing three successive PECVD runs for each investigated value of R, and by comparing the spectroscopic ellipsometry results.

Figure 29 depicts the imaginary part of the pseudo-dielectric function (ϵ_i) versus photon energy (E_{ph}) obtained after deposition of the intrinsic Si layer and after annealing at $T_a = 700^{\circ}$ C for R = 5, 20, 40 and 50. After deposition, one can note that:

- For R ≤ 20, the ε_i versus E_{ph} curve featured a single broad peak around 3.3 eV, which is characteristic of an amorphous phase [109];
- For R ≥ 40, the curve featured more of a plateau shape with the apparition of two peaks centered around 3.3 and 4.2 eV, which are associated to the microcrystalline nature of the layer.

After annealing, one can observe that:

- For R ≤ 20, the $ε_i$ versus E_{ph} curve showed two peaks with an intense peak around 4.1 eV and a weaker peak around 3.5 eV, indicating a compact Si layer with relatively big grains [110];
- For R ≥ 40, the curve only slightly evolved compared to the one measured after deposition, with a small growth of the peak detected around 3.4 eV and a decrease of the peak detected around 4.2 eV. This shape indicates a Si layer featuring smaller grains and some surface porosity (indicated by the low intensity of the 4.2 eV peak) [109].

The different shape of the ε_i versus E_{ph} curves observed for various R values before and after annealing indicates a different structural evolution upon annealing:

- For R ≤ 20, the deposited layer is amorphous which likely enables the growth of big crystalline domains during annealing and result in a compact poly-Si layer;
- For R ≥ 40, the deposited layer is likely already crystalline, which lets less room for crystalline growth during annealing and results in a poly-Si layer featuring smaller grains and surface porosity.

In conclusion, in this work and using our specific reactor and deposition conditions, the transition from amorphous to microcrystalline Si layers occurred between R = 20 and R = 40 for a layer thickness of 25 nm, which is in good agreement with ref. [131].

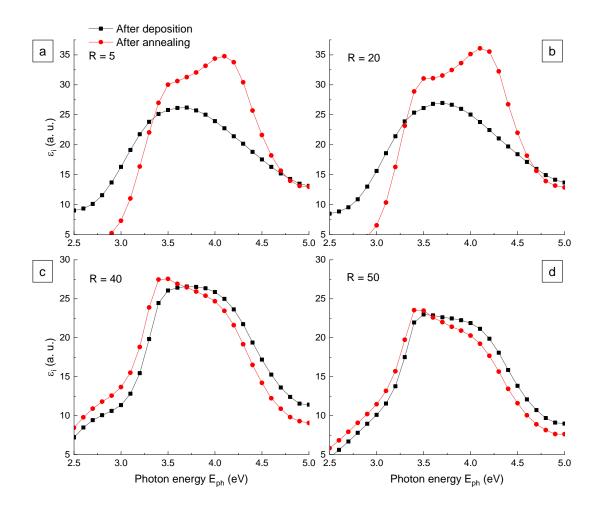


Figure 29. Imaginary part of the pseudo-dielectric function (ϵ_i) versus photon energy (E_{ph}) obtained by spectroscopic ellipsometry after deposition of 25 nm-thick intrinsic Si layer and after annealing at $T_a = 700^{\circ}\text{C}$ for different values of the gas ratio $R = H_2/\text{SiH}_4$ (5, 20, 40 and 50) used during deposition of the layer.

Figure 30a depicts optical microscope images of the intrinsic Si layer after deposition and after annealing at $T_a = 700$ °C. For R = 5 and R = 20, the layer was found to blister after each step whereas for R = 40 and R = 50, the layer remained blister-free. These observations are consistent with a lower incorporation of H during deposition of μ c-Si layers associated to the creation of more Si-Si bonds [127]. For R from 5 to 50, the deposition rate was found to decrease from 0.12 to 0.033 nm·s⁻¹, which is consistent with the increased dilution of SiH₄ in H₂ during deposition (see **Figure 30b**).

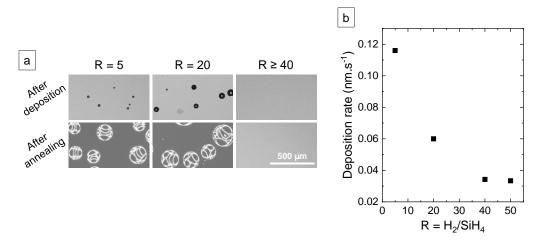


Figure 30. Optical microscope images (at x5 magnification) of 25 nm-thick intrinsic Si layers after deposition and after annealing at $T_a = 700^{\circ}\text{C}$ for different values of gas ratio $R = H_2/\text{SiH}_4$ used during deposition of the layer (a). Deposition rate of the intrinsic Si layer as a function of the gas ratio $R = H_2/\text{SiH}_4$ (b).

For each R value, three successive PECVD runs were performed to assess the reproducibility of deposition of the intrinsic Si layer. The ϵ_i versus E_{ph} signal of the layers was then measured by ellipsometry after deposition and after annealing. The average ϵ_i versus E_{ph} signal was then calculated. For R in the range 5 to 40, the ϵ_i curve exhibited good reproducibility both after deposition and after annealing; as an example, **Figure 31a** shows the data obtained for R = 40. For R = 50, despite similar curve shapes, the ϵ_i signal intensity was found to vary from one run to another (see the larger error bars **Figure 31b**), indicating poor reproducibility in these conditions.

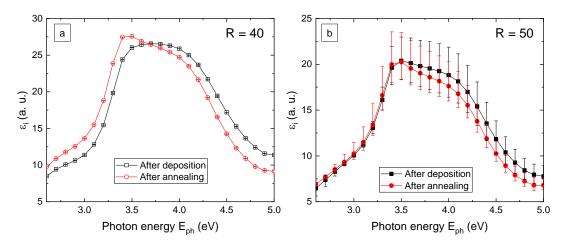


Figure 31. Imaginary part of the pseudo-dielectric function (ε_i) versus photon energy (E_{ph}) of the intrinsic Si layer deposited with a gas ratio R = H_2/SiH_4 = 40 (a) and R = 50 (b) after deposition and after annealing at T_a = 700°C. For each value of R, three consecutive deposition steps were performed and the average curve was calculated from the measurements on the three successively deposited layers. The vertical bars indicate the lowest and largest measured among the three layers.

Table 5 sums up the characteristics of the intrinsic Si layer obtained for the investigated R values. According to this table, R = 40 was chosen as the optimal ratio to ensure a reproducible and blister-free intrinsic Si layer.

Table 5. Characteristics of the intrinsic Si layer deposited with different gas ratio R = H₂/SiH₄.

	$R = H_2/SiH_4$			
Layer (after deposition)	5	20	40	50
Crystalline nature	a-Si	a-Si	μc-Si	μc-Si
Blister-free	No	No	Yes	Yes
Reproducible deposition	Yes	Yes	Yes	No

Note that the layer deposited with R = 40 being likely already microcrystalline after deposition, it will be denoted μ c-Si(i). The same layer after annealing will be denoted poly-Si(i) in order to differentiate it from the layer after deposition, even though its microstructure may not have significantly evolved after annealing.

2. Ex-situ doping

In this section, we elaborate on the ex-situ doping of the intrinsic Si layer. The ex-situ doping of the μ c-Si(i) layer is performed through the deposition of a B-rich dielectric layers (SiO_xN_y:B) on top of an intrinsic Si-based layer. The SiO_xN_y:B layer was afore-developed in our lab for the purpose of an optimized SC process [106]. In the following, it will be denoted SiON:B for a matter of simplicity.

One advantage of ex-situ doping is to separate the poly-Si crystallization from the B-doping diffusion (that could interfere with the crystallization) by performing two consecutive annealing steps. This first scheme will be referred to as the "two-annealing steps" doping process (see **Figure 32**, process 1). However, for an optimized poly-Si fabrication, an ex-situ doping process with a single annealing step for both crystallization and doping diffusion would be preferred. Therefore, we also investigated a "simplified" doping process (see **Figure 32**, process 2).

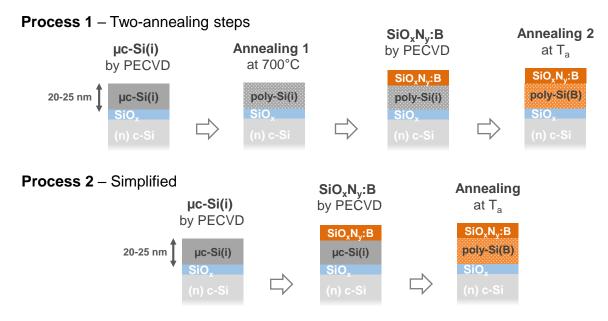


Figure 32. Ex-situ doping processes of the intrinsic Si layer (μc-Si(i)) deposited by PECVD.

First, the evolution of the Si layer microstructure through ex-situ doping was investigated. Then, we compared the electrical and passivation properties of the ex-situ doped poly-Si layers fabricated through the two processes presented in **Figure 32**. Finally, we investigated the ex-situ doping profile as a function of the annealing temperature.

a. Si layer microstructure

To confirm the μ c-Si nature of the intrinsic Si layer after deposition and to investigate the evolution of its microstructure through ex-situ doping, we performed local TEM analyses of three selected samples. Samples were made from 4" mirror-polished c-Si substrates and were processed as follows before FIB preparation and TEM observations:

- Sample 1 only saw the deposition of a 25 nm-thick μc-Si(i) layer on top of the thin SiO_x layer;
- Sample 2 saw the same deposition step as sample 1 and was subsequently annealed at 800°C resulting in a poly-Si(i) layer on top of SiO_x⁶;
- Sample 3 saw the deposition of the $\mu c\text{-Si(i)}$ layer followed by the deposition of the SiON:B layer and a final annealing step at $T_a = 800^{\circ} C^{7}$.

Figure 33 depicts images of the TEM observations and Electron Energy Loss Spectroscopy (EELS) analyses of these three samples. After deposition, the μ c-Si(i) layer appeared already crystalline with randomly oriented crystalline domains of a few nanometers (Sample 1, **Figure 33a**). The TEM observations of sample 1 confirmed that the μ c-Si(i) layer is already locally partly crystallized after deposition, which was already hypothesized from spectroscopic ellipsometry results (see **part 2-II-1b**).

After annealing at 800°C, the resulting poly-Si(i) layer appeared crystalline with a similar microstructure than the as-deposited μ c-Si(i) layer i.e. randomly oriented crystalline domains in the nanometric range (**Figure 33b**). These observations confirmed that the microstructure of the intrinsic Si layer was set from the deposition step and remained similar after subsequent annealing (which was also hypothesized based on ellipsometry results see **part 2-II-1b**).

From TEM observations of sample 3 (**Figure 33c**), one can observe that the poly-Si(B) layer featured bigger crystalline domains than the μ c-Si(i) and poly-Si(i) layers. Some crystalline domains even appear columnar along the layer thickness (25 nm here).

EELS analyses enabled to map the O concentration through the poly-Si/SiO_x contact. One can observe a peak of O concentration along the interface between the Si layer and the c-Si substrate, corresponding to the SiO_x layer (see **Figure 33 d,e,f**). No significant differences were observable between the O concentration and distribution of sample 1 and 2. However, sample 3 likely featured a broader O concentration that could indicate a thicker SiO_x layer.

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⁶ Corresponding to the two first steps of the "two-annealing steps" process (with the first annealing at 800°C).

⁷ Corresponding to the "simplified" doping process.

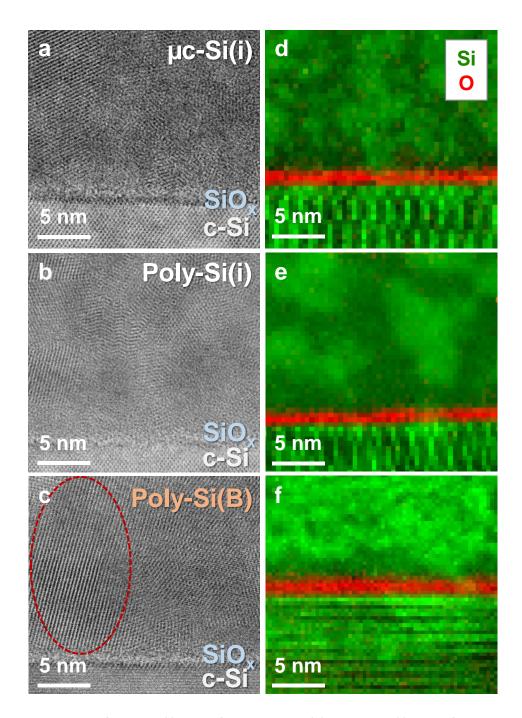


Figure 33. TEM images of the μ c-Si(i) layer after deposition (a), the poly-Si(i) layer after deposition and annealing at $T_a = 800^{\circ}$ C (b) and poly-Si(B) layer after deposition of the SiON:B doping layer on top of the μ c-Si(i) layer and annealing at $T_a = 800^{\circ}$ C (c). The respective EELS analysis of these samples are depicted beside the TEM images (d) (e) and (f).

Figure 34 depicts the EELS O concentration profiles extracted along a perpendicular axis to the samples surface⁸. This representation enabled to confirm the broader O concentration at the SiO_x interface of sample 3 (i.e. after ex-situ doping). Moreover, for this sample, one can also observe a non-negligible O concentration in the c-Si substrate. The broader O concentration

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⁸ Note that the intensity of the O concentration peaks measured by EELS depends on the measurement parameters (e.g. the counting time and the lamella thickness) and was not normalized here. Therefore, the intensities of the peaks are not comparable.

as well as the O diffusion in the c-Si observed for the ex-situ doped sample likely arises from O diffusing from the SiON:B doping layer in the SiO_x layer and in the c-Si substrate. The diffusion of species like B or O from the SiON:B layer through the poly-Si layer during ex-situ doping of sample 3 could also explain the different microstructure observed for the ex-situ doped poly-Si(B) (**Figure 33**). For example, it has been showed that poly-Si layers alloyed with O atoms consist of an amorphous SiO_x matrix with incorporation of columnar poly-Si inclusions [20,55].

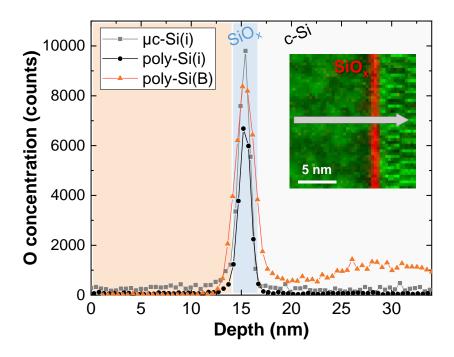


Figure 34. O concentration profiles assessed by EELS on samples made from 4" mirror-polished c-Si wafers after μ c-Si(i) deposition, after annealing at $T_a = 800$ °C (poly-Si(i)) and after SiON:B deposition plus annealing at $T_a = 800$ °C (poly-Si(B)). Profiles are extracted along a direction perpendicular at the samples' surface (see inset).

In conclusion, the TEM observations of selected samples enabled to confirm that the intrinsic Si layer (deposited with R = 40) was already crystalline after deposition. Moreover, the μ c-Si(i) and poly-Si(i) layers showed similar microstructure, emphasizing the negligible effect of the intermediate annealing step on the layer's microstructure. This could indicate that the intermediate annealing step has only a negligible effect on the final ex-situ doped poly-Si/SiO_x contact. To confirm this hypothesis, the following section will focus on the comparison of electrical and passivation properties of poly-Si layers fabricated with the "two-annealing steps" doping process and with the "simplified" one.

b. Comparison of the two ex-situ doping processes

Ex-situ doped poly-Si/SiO_x contacts were fabricated following the two processes described in **Figure 32** on a single side of 4" mirror-polished for Hall effect measurements and on both sides of 156psq KOH-polished c-Si wafers (ρ = 5-6 Ω ·cm) for PCD measurements to evaluate the electrical and passivation properties of the resulting contact, respectively.

i. Electrical properties

For accurately assessing the poly-Si electrical properties by Hall effect measurements, samples were annealed at $T_a = 700$ °C, in order to minimize the diffusion of B in the c-Si substrate. Results are summarized in **Table 6**.

Table 6. Electrical properties of the ex-situ doped poly-Si layer fabricated with the "two-annealing steps" or "simplified" doping process.

Process	Hole concentration (cm ⁻³)	Conductivity (S·cm)	Mobility (cm ² ·V ⁻¹ ·S ⁻¹)
2-annealing steps	1.2×10 ¹⁹ ±0.1	54±5	29±3
Simplified	1.2×10 ¹⁹ ±0.1	49±5	26±3

The carrier concentration, conductivity and mobility of the poly-Si(B) layers processed with and without intermediate annealing were found to be similar. This is in good agreement with TEM observations showing a negligible impact of the intermediate annealing step on the microstructure of the deposited μ c-Si(i) layer. Thus, the doping of the μ c-Si(i) layer with and without prior annealing step led to similar electrical properties for the resulting poly-Si(B) layers.

ii. Passivation properties

The iV_{oc} values obtained after annealing at $T_a = 700^{\circ}C$ and 800°C and after hydrogenation (consisting of SiN:H deposition plus firing) are reported in **Table 7**.

Table 7. iV_{oc} of samples featuring ex-situ doped poly-Si/SiO_x contacts fabricated with the "two-annealing steps" or "simplified" doping process.

	iV _{oc} (mV)				
	After annealing		After annealing + hydrogenation		
Process	T _a = 700°C	T _a = 800°C	T _a = 700°C	T _a = 800°C	
2-annealing steps	667	681.5	706	683.5	
Simplified	654	670.5	703.5	694.5	

After annealing at both T_a , iV_{oc} was approximately 10 mV higher for the "two-annealing steps" doping process compared to the "simplified" one, leading to iV_{oc} values up to 681.5 mV for the "two-annealing steps" process with $T_a = 800$ °C.

After hydrogenation, one can observe:

- For the "two-annealing steps" process, an iV_{oc} increase of 40 mV for $T_a = 700$ °C but no significant increase for $T_a = 800$ °C;
- For the "simplified" process, an iV_{oc} increase of 50 mV and 40 mV for T_a = 700°C and 800°C respectively.

Overall, the iV_{oc} values obtained with the two different doping processes after hydrogenation were comparable.

In conclusion, the electrical and passivation properties of the poly-Si contact doped according to the "two-annealing steps" or the "simplified" process were similar. It confirmed that the additional annealing step performed during the "two-annealing steps" process had only a negligible impact on the final poly-Si/SiO $_{\rm x}$ contact. Therefore, in the following, we will systematically use the "simplified" process to fabricate ex-situ doped poly-Si/SiO $_{\rm x}$ contacts as it enables a lower thermal budget.

c. Doping profile of the ex-situ doped poly-Si/SiO_x contact

This paragraph focuses on the evolution of the B-doping profile of the ex-situ doped poly-Si/SiO $_x$ contact with increasing the annealing temperature T_a .

The poly-Si/SiO_x contact was fabricated on a single side of c-Si substrates with the annealing temperature T_a varied in the range 700-850°C. The hole (approximated as active B) concentration profiles were measured by ECV after etching the SiON:B doping layer by dipping the samples in a concentrated HF solution. The total B concentration profiles were measured by SIMS without previous etch of the SiON:B layer. For SIMS measurements, 1 keV energy Cs⁺ ions were used as primary ions. Note that an O⁺ primary ion source is usually preferred to measure B concentration profiles by SIMS, but Cs⁺ ions are more accurate to measure the H and O profiles that were also of interest here (see part 4).

Figure 35 depicts the "corrected⁹" active B concentration profiles measured by ECV (symbols) as well as the total B concentration profiles measured by SIMS¹⁰ (dotted lines) after annealing in the range $T_a = 700-850$ °C.

Focusing on the active B profiles, one can note:

- For $T_a = 700$ °C and 750°C, a gradient of B concentration in the poly-Si(B) layer from 2×10^{19} cm⁻³ to 2×10^{18} cm⁻³;
- For T_a = 800°C and 900°C, a doping plateau around 2×10¹⁹ cm⁻³ in the poly-Si(B) layer coupled with a thin B-diffusion in the c-Si substrate of 20 nm and 60 nm, respectively.

These observations emphasize the gradual filling of the poly-Si(B) layer with active B dopants with increasing T_a up to 750°C (consistent with the diffusion-based doping process applied here), and the further diffusion of B in the c-Si for $T_a \ge 800$ °C.

Comparing the total and active B profiles, one can observe an overall good agreement, except for:

A higher total B concentration in the poly-Si(B) layer for the whole investigated T_a range;

¹⁰ Note that the SiON:B layer was not etched before SIMS analysis but is not represented in the graph. The sputter time related to the SIMS measurement was kept as-measured on the top axis of **Figure 35**.

 $^{^9}$ The as-measured ECV profiles were not consistent with Hall effect measurements (on similar samples for $T_a = 700$ and 750° C) and were therefore corrected according to the hole concentration measured by Hall effect. For more details on the correction of the ECV profiles, see **Appendix A**.

• For T_a = 700°C, a B diffusion tail of approximately 20 nm measured by SIMS in the c-Si but no B diffusion measured by ECV.

A higher total dopant concentration compared to the active one is plausible in poly-Si layers due to inactive dopants segregating at GBs [134–136]. The difference of active and total B concentration could also arise from the respective uncertainties of the ECV and SIMS measurements i.e. an error on the determination of the etch area for ECV and/or certain effects (e.g. knock on effect) creating artificial dopant diffusions for SIMS. Moreover, the ECV profiles were here corrected according to the Hall effect measurements, which could also lead to a significant error on the active B concentration. Therefore, such SIMS and ECV measurements of the ex-situ doped poly-Si/SiO_x contact should be reproduced to evaluate if the different B diffusion tail is systematic or not and if a potential correction could be applied.

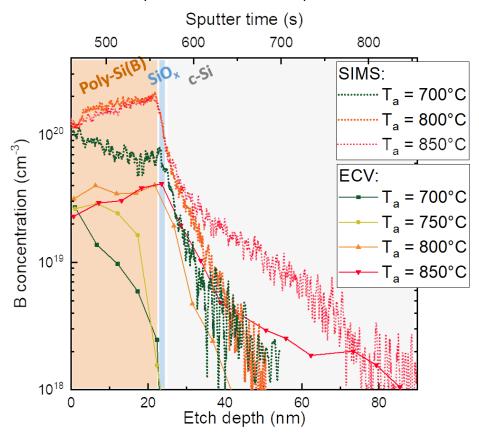


Figure 35. Active and total B concentration profiles measured by ECV and SIMS, respectively, on ex-situ doped poly-Si/SiO $_{\rm x}$ contacts after annealing at various annealing temperature T $_{\rm a}$.

3. Comparison of in-situ and ex-situ doped poly-Si/SiO_x contacts

In this section, we aim at comparing the properties of the ex-situ doped poly-Si/SiO $_{\rm x}$ contact with the reference in-situ doped one. We will first focus on the Si layer microstructure after deposition and after annealing, then on the electrical properties and finally on the passivation properties.

a. Si-layer microstructure

i. After deposition

In this paragraph, we compare the microstructure of the in-situ doped and intrinsic Si layers after deposition by PECVD. The optimal deposition conditions found for each layer are summarized in **Table 8**. They are overall similar except for the addition or not of the doping precursor B_2H_6 and a slightly different H_2 flow.

Table 8. PECVD parameters used for the deposition of a-Si:H(B) and μ c-Si(i) layers.

Deposited layer	RF power (W)	Pressure (Torr)	SiH ₄ (cc)	H ₂ (cc)	B ₂ H ₆ (cc)
a-Si:H(B)	40	1.5	100	5000	30
μc-Si(i)	40	1.5	100	4000	0

As already mentioned, the use of high gas ratio $R = H_2/SiH_4$ during PECVD is known to promote the deposition of μ c-Si layers [127] but the addition of B during deposition of the layer has been shown to impede its crystallization, thus leading to an amorphous layer [132].

Figure 36 depicts TEM images and ε_i versus E_{ph} curves (obtained by ellipsometry) for each layer after deposition. From local TEM observations, the in-situ doped layer was found amorphous (a-Si:H(B)), whereas the intrinsic layer was already crystalline (μ c-Si(i)). These observations were confirmed by ellipsometry: the ε_i versus E_{ph} curve showed a single peak for the in-situ doped layer and more of a plateau shape for the intrinsic layer respectively indicating a-Si and μ c-Si phases [109].

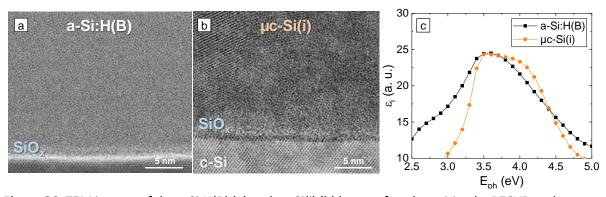


Figure 36. TEM images of the a-Si:H(B) (a) and μ c-Si(i) (b) layers after deposition by PECVD and ϵ_i versus E_{ph} curve measured on each layer by spectroscopic ellipsometry (c).

ii. After annealing

Figure 37 depicts TEM images and ϵ_i versus E_{ph} curves obtained on in-situ and ex-situ doped poly-Si layers after annealing at $T_a = 800^{\circ}C^{11}$. Despite the quite different microstructure of the a-Si:H(B) and μ c-Si(i) layers after deposition, a very similar microstructure was observed by

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 $^{^{11}}$ Note that we compared TEM observations after annealing at $T_a = 800^{\circ}$ C because only this T_a was investigated for the ex-situ doped poly-Si contact.

TEM for in-situ and ex-situ doped poly-Si(B) layers after annealing at T_a = 800°C. Local TEM observations were confirmed by similar ellipsometry curves obtained after annealing at T_a = 700°C.

It is worth emphasizing that, despite their similar microstructure, the crystallization mechanism of in-situ and ex-situ doped poly-Si layers appeared to be different:

- The in-situ doped a-Si:H(B) layer is crystallizing during the annealing step, probably through the growth of randomly oriented grains in the amorphous matrix;
- The intrinsic μc-Si(i) layer is already crystalline after deposition. Although some grains appeared columnar after ex-situ doping (see **Figure 37b**), the growth mechanism during deposition and evolution of the microstructure through ex-situ doping remains unclear.

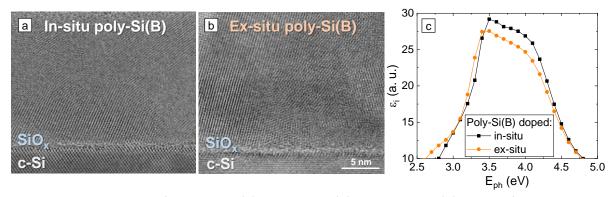


Figure 37. TEM images of the in-situ (a) and ex-situ (b) doped poly-Si(B) layers after annealing at $T_a = 800^{\circ}\text{C}$ and ε_i versus E_{ph} curve measured on each layer (c).

b. Electrical properties

In this section, we compare electrical properties of the in-situ and ex-situ doped poly-Si(B) layers. **Table 9** summarizes the hole concentration, conductivity and mobility assessed by Hall effect measurements on both types of layers after annealing at $T_a = 700^{\circ}C^{12}$.

The hole concentration was found to be almost ten times lower in the ex-situ doped poly-Si layer compared to the in-situ doped one. This different carrier concentration likely explains the lower conductivity of the ex-situ doped poly-Si layer compared to the in-situ doped one. On the contrary, the mobility was higher in the ex-situ doped poly-Si layer, which is probably due to the lower doping concentration of the ex-situ layer, similarly to what would happen in c-Si (see **Figure 26b**).

Table 9. Electrical properties of the in-situ and ex-situ doped poly-Si layers after annealing at $T_a = 700$ °C.

Doping	Hole concentration (cm ⁻³)	Conductivity (S·cm)	Mobility (cm ² ·V ⁻¹ ·S ⁻¹)		
In-situ	1.06×10 ²⁰	218.6	11.7		
Ex-situ	1.18×10 ¹⁹	49.2	26.1		

 $^{^{12}}$ T_a = 700°C was chosen to avoid any B-diffusion in the c-Si substrate, that would induce current flowing in the c-Si and lead to an inaccurate estimation of the poly-Si electrical properties.

The hole concentration profiles measured by ECV on both in-situ and ex-situ poly-Si/SiO $_{\rm x}$ contacts were also compared after annealing in the range T_a = 700-800°C (see **Figure 38**). It is worth recalling that the ECV profiles of ex-situ doped contacts were corrected and are therefore subjected to a certain error. Consequently, only a qualitative comparison is proposed here.

For $T_a = 700-750$ °C, a plateau was observed in the in-situ doped layer whereas a gradual doping density was observed in the ex-situ doped layer. These observations are consistent with the respective doping method used:

- In-situ through direct addition of dopants during the layer's deposition;
- Ex-situ through a gradual diffusion of B from the SiON:B layer.

For $T_a = 800$ °C, the shape of the in-situ and ex-situ doping profiles converged, with a similar B-diffusion length in the c-Si.

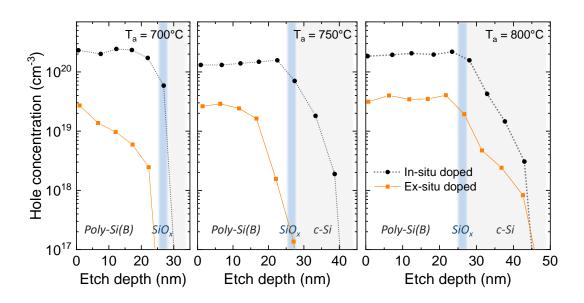


Figure 38. Hole (approximated as active B) concentration profiles measured by ECV on in-situ and ex-situ doped poly-Si/SiO $_{\rm x}$ contacts after annealing at different temperatures $T_{\rm a}$.

c. Surface passivation properties

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The surface passivation provided by in-situ and ex-situ doped poly-Si/SiO_x contacts was then compared (in terms of iV_{oc} and J₀ values). In-situ and ex-situ doped poly-Si/SiO_x contacts were fabricated on both sides of 156psq c-Si wafers with respective resistivity of ρ = 5-6 Ω ·cm and ρ = 2-3 Ω ·cm¹³. For both contacts, the surface passivation properties were measured by PCD after annealing at various T_a values in the range of 700-850°C and after subsequent SiN:H deposition and firing (for hydrogenation). Resulting iV_{oc} values are depicted in **Figure 39**.

¹³ Note that surface passivation properties of ex-situ doped poly-Si contacts presented in **part 2b** were assessed on 156psq c-Si wafers with ρ = 5-6 Ω -cm, which likely explains the lower values obtained.

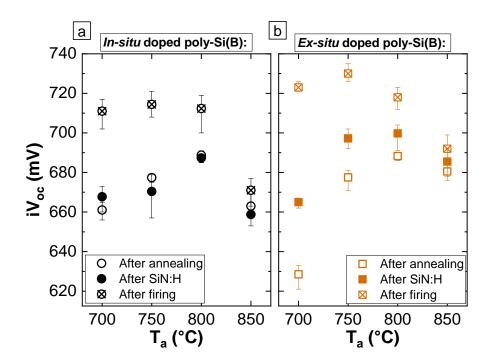


Figure 39. iV_{oc} as a function of the annealing temperature T_a measured (after annealing, after SiN:H deposition and after firing at $T_{firing} \sim 860$ °C) on samples with in-situ (a) and ex-situ (b) doped poly-Si/SiO_x contacts.

After annealing, one can observe:

- A similar iV_{oc} versus T_a trend for both contacts, with iV_{oc} increasing from $T_a = 700^{\circ}$ C to 800°C and then decreasing for $T_a > 800^{\circ}$ C;
- Similar iV_{oc} values for both contacts except for $T_a = 700^{\circ}C$ (iV_{oc} of 661 mV and 628.5 mV for in-situ and ex-situ contacts, respectively).

The lower iV_{oc} value measured for the ex-situ doped contact after annealing at $T_a = 700^{\circ}C$ could result from a lower field-effect passivation provided by the ex-situ poly-Si layer that appeared only partially doped in these conditions (see **Figure 38**).

The subsequent SiN:H deposition involved only slight changes of iV_{oc} for in-situ doped contacts whereas it enabled an iV_{oc} gain in the whole T_a range for the ex-situ doped ones (up to 30 mV for T_a = 700°C). This resulted in slightly higher passivation level provided by the ex-situ doped poly-Si/SiO_x contact after SiN:H deposition, with a maximum iV_{oc} of 702 mV.

After firing, a significant iV_{oc} gain was observed in the whole T_a range for both in-situ and ex-situ doped poly-Si/SiO_x contacts. Best iV_{oc} values of 721 mV and 733 mV were measured with in-situ and ex-situ contacts, respectively, after annealing at $T_a = 750$ °C (both corresponding to $J_0 = 6$ fA.cm⁻²)¹⁴.

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¹⁴ Note that the different final iV_{oc} values obtained with in-situ and ex-situ doped contacts could arise from the slightly different substrate resistivity used (ρ = 5-6 Ω ·cm and 2-3 Ω ·cm, respectively). iV_{oc} up to 734 mV were obtained with in-situ doped poly-Si contacts deposited on lower resistivity substrates (see **part 3-l-3**).

Overall, the iV_{oc} versus T_a trend was similar for both in-situ and ex-situ doped poly-Si/SiO_x contacts. This trend is not straightforward to explain due to the three different passivation mechanisms involved, related to the SiO_x layer, the poly-Si high doping and the hydrogen diffusion, respectively. In the next part, the surface passivation properties provided by the poly-Si contact with and without ex-situ doping are compared in order to better understand the respective effect of these different passivation mechanisms.

4. Effect of the doping density and hydrogen diffusion on surface passivation

Developing the ex-situ doping process gave the opportunity to fabricate intrinsic poly-Si/SiO $_{\rm x}$ contacts by omitting the SiON:B deposition before the annealing step. In this section, the surface passivation of intrinsic and ex-situ doped poly-Si/SiO $_{\rm x}$ contacts are compared to better understand the impact of the high-doping density of the poly-Si layer on the overall final surface passivation provided by the poly-Si contact. The impact of the H diffusion is also investigated by SIMS measurements as a function of the annealing temperature.

- A first set of samples featuring ex-situ doped poly-Si/SiO_x contacts (poly-Si(B)) on both sides of 156psq KOH-polished c-Si wafers were fabricated according to the process described part 2-I-4 (with a poly-Si thickness of 25 nm). After deposition of the SiON:B layer, the annealing temperature was varied in the range of T_a = 700-850°C;
- A second set of samples was similarly fabricated by omitting the SiON:B deposition, leading to symmetrical samples featuring intrinsic poly-Si/SiO_x contacts (poly-Si(i));
- Poly-Si(B) and poly-Si(i) samples were then hydrogenated through the standard process (SiN:H deposition plus firing), with a peak firing temperature varied in the range of T_{firing} = 800-900°C;
- Monitoring samples were fabricated with poly-Si(B) or poly-Si(i) contacts on a single-side of 4" mirror-polished c-Si wafers for SIMS characterization of H and O profiles.

a. Passivation stability upon annealing and SiN:H deposition

The ex-situ doping relies on thermal diffusion, which is less likely to induce damages in the poly-Si layer than ion implantation for example. Moreover, the poly-Si(i) and poly-Si(B) layers' microstructure were found to be comparable (see **Figure 37**). Therefore, in the following we assume that the only significant difference between the poly-Si(i) and poly-Si(B) contacts was the diffusion of B atoms through the doped one.

The passivation level provided by poly-Si(i) and poly-Si(B) contacts was evaluated (in terms of iV_{oc}) as a function of T_a in the range 700-850°C before and after SiN:H deposition (first without firing). Results are displayed in **Figure 40**.

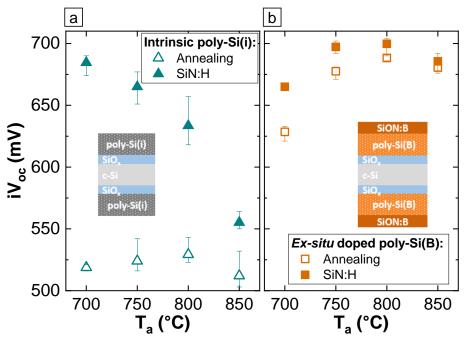


Figure 40. iV_{oc} measured by PCD on symmetrical samples (with poly-Si/SiO_x structures fabricated on each side of the c-Si wafer, see inset schematics) as a function of the annealing temperature T_a . The measurement was performed on samples with 25 nm-thick intrinsic poly-Si layers (poly-Si(i)) (a) and B-doped poly-Si layers (poly-Si(B)) (b).

After annealing, one can note that:

- The poly-Si(i) contact showed poor iV_{oc} values (< 530 mV) in the investigated T_a range whereas poly-Si(B) demonstrated decent iV_{oc} values (up to 690 mV for T_a = 800°C);
- A similar trend of iV_{oc} versus T_a was obtained for both poly-Si(i) and poly-Si(B) contacts with the iV_{oc} increasing from $T_a = 700^{\circ}\text{C}$ to 850°C and then decreasing for $T_a = 850^{\circ}\text{C}$.

The poor surface passivation obtained with the poly-Si(i) contact evidences a negligible chemical passivation provided by the SiO_x layer alone (as similarly observed in ref. [30]). It also emphasizes the importance of the field-effect passivation related to the high B-doping of the poly-Si layer to obtain decent iV_{oc} values after annealing.

Regarding the iV_{oc} versus T_a trend:

- For the poly-Si(i) contact the only surface passivation is provided by the thin SiO_x layer. Therefore, the passivation trend is likely explained by an improvement of the SiO_x interface at moderate T_a in the range 700-800°C followed by a degradation of the interface for $T_a \ge 800$ °C;
- For the poly-Si(B) contact, the field-effect passivation related to the high B-doping has to be taken into account. The increase of iV_{oc} from T_a = 700°C to 800°C could result from a combination of the afore-mentioned improvement of the SiO_x interface coupled with an increased field-effect passivation due to the gradual filling of the poly-Si layer with B dopants (see **Figure 35**). The decrease of iV_{oc} at high T_a is generally attributed to a combination of the degradation of the SiO_x homogeneity at the interface and an excessive B diffusion in the c-Si substrate leading to enhanced Auger recombination in the highly doped c-Si region.

After SiN:H deposition, one can observe for both poly-Si(i) and poly-Si(B) contacts:

- An increase of iV_{oc} in the whole investigated T_a range;
- A decreasing gain in iV_{oc} with increasing T_a.

The deposition of a SiN:H layers is known to provide both field-effect passivation due to positive fixed charges and chemical passivation due to H-diffusion in the sample [143]. However, for both poly-Si(i) and poly-Si(B) contacts, the surface passivation properties (iV $_{oc}$ and J $_{o}$) were found to be stable after etching of the SiN:H layer by dipping the samples for a few seconds in a concentrated HF solution. This result indicates that the iV $_{oc}$ increase observed here is mostly linked to H diffusing from the SiN:H in the samples.

Although the poly-Si(i) contact showed a greater iV_{oc} gain after SiN:H deposition (up to 160 mV for $T_a = 700$ °C), the poly-Si(B) contact showed a better thermal stability of surface passivation at high $T_a \ge 750$ °C ($iV_{oc} > 675$ mV). This latter observation is likely due to the additional field-effect passivation related to the high B-doping.

The decreasing gain in iV_{oc} with increasing T_a observed after SiN:H deposition could arise from a less efficient hydrogenation of the interface at high T_a due to e.g. a lower H diffusivity through the poly-Si layer and/or an evolution of the SiO_x interface. In the next paragraph, the diffusion of H in poly-Si(i) and poly-Si(B) contacts is further investigated by SIMS measurements.

b. H diffusion profile in poly-Si(i) and poly-Si(B) contacts

H and O profiles were measured by SIMS after SiN:H deposition on poly-Si(i) and SiON:B capped poly-Si(B) layers annealed at the lowest (700°C) and highest (850°C) T_a over the investigated range. The resulting profiles are depicted in **Figure 41**. It is to note that, as the samples consisted of a stack of different layers, we expected the SIMS etching rate to differ from one layer to another so the SIMS sputter time was not converted into thickness but the O profiles were used to locate the interfacial SiO_x layer. Also note that for a matter of simplicity, the H and O profiles were only represented in the region of interest that is the poly-Si contact plus the c-Si top surface.

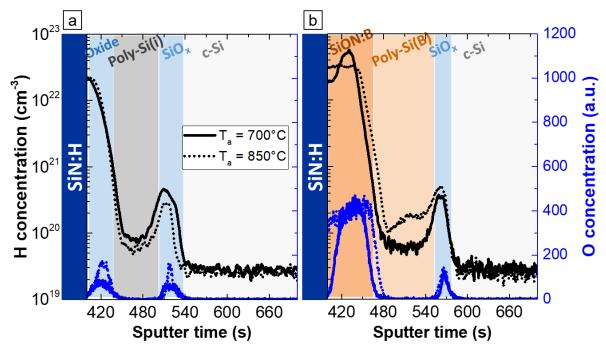


Figure 41. H and O depth-profiles measured by SIMS on samples featuring the poly-Si(i)/SiO_x (a) and the poly-Si(B)/SiO_x contact (b). The measurement was performed after SiN:H deposition for T_a = 700°C (solid curves) and 850°C (dashed curves).

Focusing on the H profiles, one can observe:

- For both poly-Si(i) and poly-Si(B) contacts:
 - o An accumulation of H for a sputter time of 420 s, i.e. in the oxide layer at the poly-Si(i) top surface and in the SiON:B layer, respectively;
 - A similar accumulation of H at the SiO_x interface with a concentration of approximately 3×10²⁰ cm⁻³;
- For the poly-Si(B) contact, a higher H concentration in the poly-Si layer after annealing at $T_a = 850$ °C compared to $T_a = 700$ °C.

The SiN:H capping layer was not removed from the samples' surface before SIMS measurements. Therefore, the H accumulation detected for a sputter time of 420 s is likely due to the presence of the SiN:H layer (not shown in Figure 41) on top of the oxide and the SiON:B layer for the poly-Si(i) and poly-Si(B) samples, respectively.

The accumulation of H at the SiO_x interface confirms that H atoms diffusing from the SiN:H layer are passivating the SiO_x interface¹⁵, which is in good agreement with results obtained by other groups [16,86]. However, the similar H concentration observed at the SiO_x interface of the different samples invalidates the hypothesis that the lower gain from hydrogenation at high T_a (see **Figure 40**) resulted from a lower H diffusivity in the poly-Si layer. Yet, it highlighted that the SiON:B doping layer did not impede the H diffusion through the poly-Si(B) contact. The higher H content in the poly-Si(B) layer annealed at $T_a = 850$ °C could indicate a higher

¹⁵ Note that such an H accumulation was not measured by SIMS at the SiO_x interface of a monitoring sample before SiN:H deposition (not shown here).

concentration of defects passivated by H in the layer but this point would require further investigations.

Focusing on the O profiles measured on the poly-Si(i) samples, one can note that:

- An oxide layer was detected at the poly-Si(i) top surface, likely resulting from a residual O concentration in the tube furnace in which the annealing for poly-Si crystallization was performed;
- For $T_a = 850$ °C, the O peaks detected at the sample's top surface and at the poly-Si(i)/c-Si interface were more intense and better defined than for $T_a = 700$ °C.

This latter observation could indicate an evolution of the oxide layers towards O-richer phases upon annealing at higher T_a . As O-richer SiO_x has been shown to provide better passivation of the c-Si surface [144], it could explain the increasing iV_{oc} of poly-Si(i) contacts after annealing at T_a from 700°C to 800°C (see **Figure 40a**). The chemical and structural evolution of the SiO_x layer upon annealing will be studied in more details using XPS measurements in **part 4-I**.

The O profiles obtained on poly-Si(B) samples showed:

- A high O concentration at the poly-Si(B) top surface corresponding to the SiON:B doping layer;
- A similar O signal related to the interfacial SiO_x layer after annealing at $T_a = 700$ and $850^{\circ}C$.

For both T_a = 700 and 850°C, the O signals detected at the interface of the poly-Si(B) contacts were similar as the one obtained on the poly-Si(i) contact for T_a = 850°C. The O-richer SiO_x observed in the case of ex-situ doped poly-Si(B) contacts is likely linked to O diffusing from the SiO_x interface, as already evidenced by EELS analyses (see **Figure 34**).

c. Effect of the firing temperature

As mentioned, a firing step is usually performed consecutively to the SiN:H deposition to enhance the diffusion of H toward the SiO_x interface and improve the final surface passivation [12,13,21]. In this paragraph, the surface passivation properties provided by poly-Si(i) and poly-Si(B) contacts were evaluated as functions of the peak firing temperature T_{firing} in the range 800-900°C (see **Figure 42**).

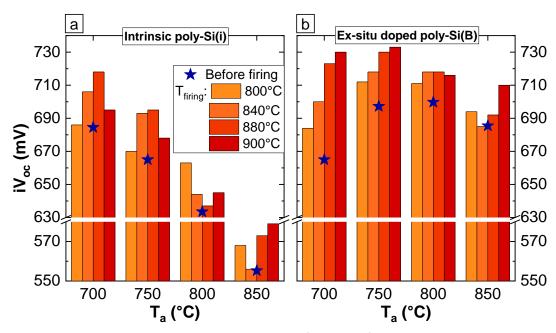


Figure 42. iV_{oc} measured on symmetrical samples as a function of the poly-Si annealing temperature T_a . The measurement was performed on samples with poly-Si(i) (a) and poly-Si(B) contacts (b) after different firing peak temperature T_{firing} in the range 800-900°C.

Focusing on the effect of the firing on the poly-Si(i) contact (Figure 42a), one can note that:

- For $T_a \le 750$ °C, the firing step was found to be beneficial, with an optimum firing temperature $T_{firing} = 880$ °C, resulting in maximum iV_{oc} values of 718 mV and 695 mV for $T_a = 700$ °C and 750°C, respectively. This improvement is likely due to further H diffusion toward the SiO_x interface. For $T_{firing} \ge 880$ °C, the drop of passivation could be due to the degradation of the SiO_x homogeneity leading to direct interfaces between the poly-Si layer and the c-Si substrate where H has been seen to not accumulate [145];
- For $T_a \ge 800^{\circ}\text{C}$, the iV_{oc} versus T_{firing} curve showed a U-shape i.e. iV_{oc} increased for $T_{firing} = 800^{\circ}\text{C}$, but then decreased for $T_{firing} = 840^{\circ}\text{C}$ and increased again for $T_{firing} \ge 880^{\circ}\text{C}$. For $T_a \ge 800^{\circ}\text{C}$, the SiO_x interface may have been degraded during crystallization annealing and the subsequent firing was expected to only further degrade it. Thus, the iV_{oc} improvement observed for $T_{firing} \ge 880^{\circ}\text{C}$ remains unclear.

Now focusing on the effect of the firing on the poly-Si(B) contact (Figure 42b):

- For $T_a \le 750^{\circ}$ C, we observed a steady increase of iV_{oc} with increasing T_{firing} . A maximum iV_{oc} of 733 mV was obtained for $(T_a; T_{firing}) = (750^{\circ}\text{C}; 900^{\circ}\text{C})$ (corresponding to a J_0 value of $6 \text{ fA} \cdot \text{cm}^{-2}$), which is among the best values reported so far with hole-selective poly-Si/SiO_x passivated contacts [13–16];
- For T_a = 800°C, iV_{oc} remained almost constant around 715 mV in the whole investigated T_{firing} range;
- For T_a = 850°C, the iV_{oc} versus T_{firing} curve showed a U-shape with an iV_{oc} decrease for T_{firing} = 800-840°C followed by an increase up to 715 mV for T_{firing} = 900°C, similarly to what was observed with the poly-Si(i) contact annealed at T_a ≥ 800°C.

When comparing iV_{oc} versus T_{firing} trends measured on poly-Si(i) and poly-Si(B) contacts, one can note:

- An overall higher surface passivation and better thermal stability provided by poly-Si(B) compared to poly-Si(i), resulting from the additional high-doping related field-effect passivation, which likely compensates the loss of surface passivation due to SiO_x degradation at too high T_a and/or T_{firing};
- A better absolute gain after firing for both poly-Si(i) and poly-Si(B) contacts previously annealed at $T_a \le 750$ °C compared to contacts annealed at $T_a \ge 800$ °C (similarly to what was observed after SiN:H deposition, see **Figure 41**).

To explain the latter observation, the H diffusion was investigated by SIMS but it did not emphasize a clear difference of H accumulation at the SiO_x interface. Therefore, we concluded that the reduced gain from hydrogenation on samples annealed at high T_a was not linked to a limited H diffusion in these samples. This trend could rather result from an evolution of the SiO_x interface quality upon annealing e.g. an improvement of the SiO_x stoichiometry at moderate T_a (700-800°C) and/or a degradation of the SiO_x thickness homogeneity at higher T_a (> 800°C). A further investigation of the evolution of the SiO_x layer upon annealing will be addressed in the next chapter that focuses on the characterization of the poly-Si/c-Si interface.

Conclusion

In this part, we elaborated on the fabrication and characterization of boron-doped poly-Si/SiO_x contacts. First, the deposition conditions were optimized to decrease the H content in the boron-doped a-Si:H layer and overcome the blistering of the poly-Si after annealing. The crystallization and doping of the poly-Si layer were then investigated. The in-situ doped poly-Si layer was shown to crystallize through the growth of randomly oriented nanometric domains in the amorphous matrix upon annealing. The total and active B concentration were found homogeneous in the poly-Si layer, and were estimated around 1×10^{21} cm⁻³ and 1×10^{20} cm⁻³, respectively. A diffusion of B in the underlying c-Si substrate was observed for annealing temperatures $T_a \ge 800^{\circ}$ C. The surface passivation properties provided by the resulting in-situ doped poly-Si/SiO_x contact were evaluated on c-Si substrates with desired area (156 psq) and topography (KOH-polished) for integration of the contact at the rear side of a p-type c-Si SC. A maximum iV_{oc} value of 734 mV (J₀ = 7 fA·cm⁻²) was obtained after subsequent hydrogenation process. This result, which is among the best values reported so far for p⁺-poly-Si contact, is very promising for device integration.

The addition of a H-rich doping precursor gas during deposition likely enhancing the blistering problem, an alternative ex-situ doping method was also considered, consisting in the deposition of a B-rich dielectric layer on top of an intrinsic Si-layer afore-deposited by PECVD. The electrical and passivation properties of the resulting ex-situ doped poly-Si/SiO_x contact were found equivalent to the ones of the reference in-situ doped contact, although the crystallization and doping mechanisms involved were different. Indeed, the intrinsic Si layer

deposited by PECVD was found to be crystalline after deposition and its microstructure was observed to be stable after annealing for doping diffusion.

Eventually, the comparison of poly-Si/SiO_x contacts, ex-situ doped or not, emphasized the importance of the field-effect passivation (related to the poly-Si high doping) to enable decent passivation properties after annealing for crystallization (see **Figure 43**). The diffusion of H from the SiN:H layer in the ex-situ doped poly-Si/SiO_x contact was also investigated by SIMS profiling. Results emphasized the accumulation of H at the poly-Si/c-Si interface for both doped and undoped structures, confirming that the H atoms are passivating the remaining defects at this interface (see **Figure 44**). However, we observed a similar H concentration at the SiO_x interface of samples annealed at different temperature, thus, we could not conclude on the different passivation properties obtained for these samples.

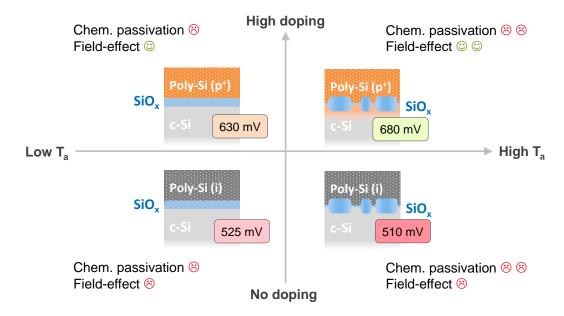


Figure 43. Schematic of the different surface passivation levels obtained and the respective effects of each passivation mechanism after annealing for poly-Si crystallization with and without high doping of the poly-Si layer and as a function of the annealing temperature (T_a) .

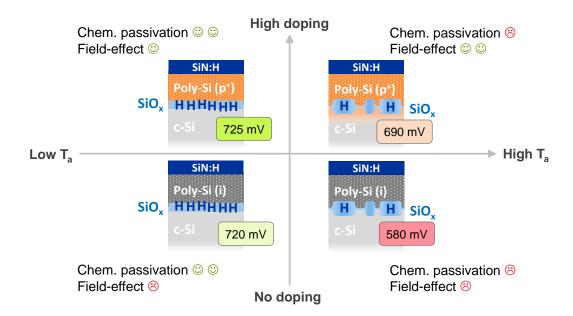


Figure 44. Schematic of the different surface passivation levels obtained and the respective effects of each passivation mechanism after hydrogenation with and without high doping of the poly-Si layer and as a function of the annealing temperature for poly-Si crystallization (T_a).

Part 4. Investigation of the poly-Si/SiO_x interface

I. Chemical and structural evolution of the SiO_x layer

TEM studies of the poly-Si/SiO_x interface after annealing for poly-Si crystallization have evidenced a degradation of the thin SiO_x layer at high annealing temperatures (typically 900-1000°C) [24,75,146]. This degradation could at least partly explain the loss of surface passivation observed after annealing at such temperatures. Recently, X-ray Photoelectron Spectroscopy (XPS) studies of the chemical composition of thin SiO_x layers grown by different methods on top of c-Si substrates were also reported in the literature [144,147,148]. XPS is a non-destructive technique that enables to study the chemical state of atoms located at the extreme surface of a sample (~ 5 nm depth-analysis for a measurement angle of 45°).

In this work, we investigated the chemical evolution of the thin SiO_x layer upon annealing. A preliminary study consisted in performing XPS measurements on a simple sample consisting of a chemical SiO_x layer grown at the surface of a c-Si substrate, before and after annealing. Then, we studied the chemical evolution of the thin SiO_x layer located at the poly-Si/c-Si interface during annealing for poly-Si crystallization. To do so, in-depth XPS measurements were performed. In this mode, etching steps and XPS measurements were alternated. TEM observations of the interface were additionally performed to correlate the chemical and structural evolutions of the interfacial SiO_x layer.

1. SiO_x grown at the c-Si surface

a. Ex-situ annealing in the tube furnace

A preliminary study was performed to investigate the chemical evolution of the SiO_x layer at the surface of a c-Si substrate upon annealing in different conditions. The SiO_x layer was grown at the surface of 4" mirror-polished c-Si wafers through the afore-described DIO₃ step (see part 2-I). Samples were annealed in a tube furnace at $T_a = 800^{\circ}C$ under argon (which corresponds to the annealing conditions of the poly-Si layer). They were then cut with a diamond tip into squares of approximately 1×1 cm² and fixed on the XPS sample holder with copper tape. Figure 45 depicts the XPS survey spectra recorded between 0 and 1100 eV before and after annealing. On these survey spectra, one can observe a strong signature of silicon (Si 2p, 2s) and oxygen (O 1s, and the Auger characteristic line KLL) as well as traces of carbon (C 1s) and fluorine (F 1s).

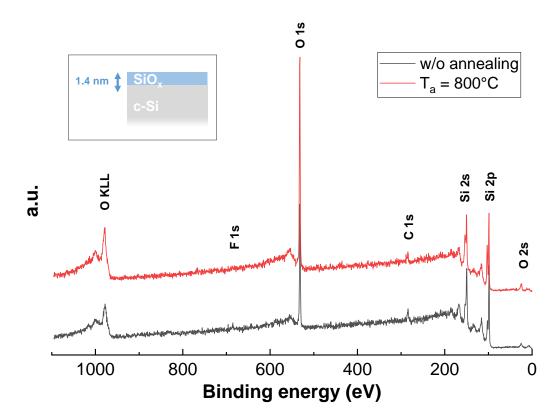


Figure 45. XPS survey spectra recorded between 0 and 1100 eV on a sample consisting of a $SiO_x/c-Si$ stack (see inset) before and after annealing at $T_a = 800$ °C.

Figure 46 displays the high energy resolution spectra in the Si 2p, O 1s and C 1s core level spectral range before and after annealing at $T_a = 800^{\circ}$ C. While the presence of Si and O was expected in the samples, no C was intentionally incorporated and its presence likely results from surface contamination.

The Si 2p spectral range consists of:

- A peak around 98.8 eV, corresponding to the zero valence Si (denoted Si⁰), which exhibits an asymmetric shape due to the Si 2p_{3/2-1/2} spin-orbit splitting associated to the ideal Si structure (see arrows in **Figure 46**);
- A peak around 102.8 eV, corresponding to elemental SiO₂ i.e. Si atoms bonded with four O atoms (denoted Si⁴⁺).

The shape of the Si 2p signal in between the Si⁰ and Si⁴⁺ peaks depends on the presence of suboxide species (Si atoms bonded with one, two or three O atoms denoted Si⁺, Si²⁺, and Si³⁺, respectively) [149].

Comparing the XPS spectra obtained before and after annealing, one can note:

■ A higher intensity of the Si⁴⁺ peak, relative to the Si⁰ one after annealing, which reveals a thicker SiO_x layer at the surface of the annealed sample compared to the non-annealed one (confirmed by a higher O 1s peak intensity after annealing);

- A more symmetric Si⁴⁺ peak after annealing, indicating a better SiO₂-like stoichiometry of the SiO_x layer;
- A better-defined Si 2p_{3/2-1/2} doublet for the Si⁰ peak after annealing, indicating a better crystallinity of the c-Si surface.

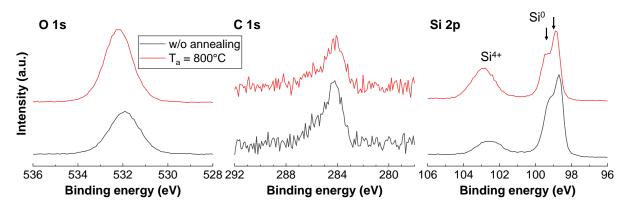


Figure 46. XPS Si 2p, O 1s and C 1s core level peaks (recorded in the range 94 eV and 120 eV; 525 eV and 543 eV; 278 eV and 298 eV, respectively) on a sample consisting of a SiO_x/c -Si stack.

The improved stoichiometry of the SiO_x layer and higher crystallinity of the c-Si surface after annealing in the tube furnace reveals a rearrangement of the Si-O bindings resulting in a better quality of the SiO_x /c-Si interface. The increase of the SiO_x thickness, which was not expected during annealing in an inert atmosphere, may indicate that a residual oxygen concentration remained in the tube furnace, enhancing the oxidation of the c-Si surface.

b. In-situ annealing in the XPS chamber

The XPS set-up used in this work offers the possibility to perform in-situ annealing up to 800° C through a hotplate coupled to the sample holder. Thus, XPS measurements were performed upon in-situ annealing (under vacuum) of the SiO_x/c -Si sample, in order to study the SiO_x chemical evolution upon annealing. The in-situ annealing temperature profile is depicted in **Figure 47**. XPS measurements were performed every 100° C from 400° C to 800° C (see arrows **Figure 47**). Five consecutive XPS measurements were also performed upon cooling of the sample from 800° C to 30° C.

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¹⁶ Note that 800°C being the maximum temperature allowed by the hotplate system, this temperature was not hold more than a few seconds as it could involve set-up degradations.

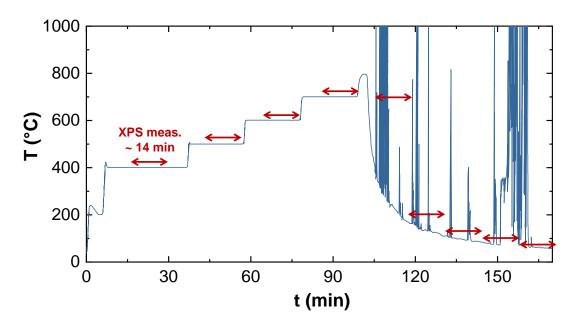


Figure 47. Temperature profile applied during in-situ annealing of the SiO_x/c -Si sample in the XPS chamber.

Figure 48 depicts the XPS spectra in the Si 2p, O 1s and C 1s spectral range measured during in-situ annealing from 400°C to 700°C. Spectra measured on the SiO_x/c -Si sample before annealing are also depicted as a reference. Firstly, one can observe the disappearance of the C 1s peak with increasing in-situ annealing temperature, which indicates desorption of C from the sample and confirms that the detected C concentration resulted from surface contamination.

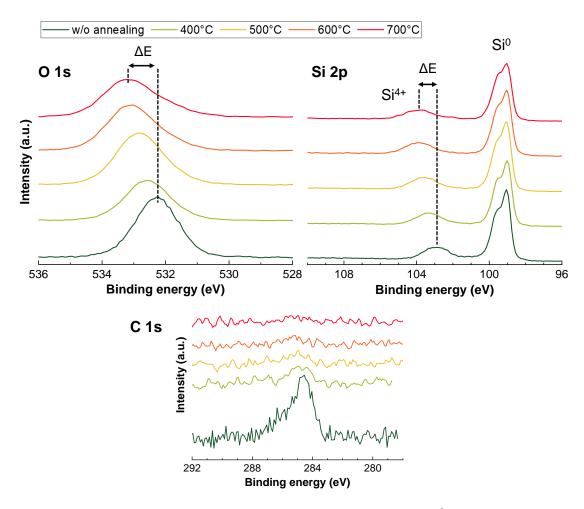


Figure 48. XPS Si 2p, O 1s and C 1s core level peaks measured on a SiO_x/c -Si sample during in-situ annealing of the sample in the XPS chamber.

Then, focusing on the evolution of the Si 2p and O 1s spectral range with increasing in-situ temperature, one can note:

- A constant relative intensity of the Si⁴⁺ peak, indicating a constant SiO_x thickness during in-situ annealing;
- An evolution of the Si⁴⁺ signal towards an asymmetrical peak (also observed on the O 1s signal), coupled with a loss of definition of the Si 2p_{3/2-1/2} doublet shape, likely indicating a disturbance of the SiO_x/c-Si interface upon annealing;
- A shift of the Si⁴⁺ peak position towards higher energies (also observed for the O 1s signal), resulting in an energy difference ΔE of approximately 1 eV between the Si⁴⁺ and O 1s peaks measured before annealing compared to the ones measured after in-situ annealing at 700°C. This slight energy shift may be due to a change of the surface band bending due to local rearrangement of Si-O bindings at the SiO_x/c-Si interface [150].

Figure 49 depicts the XPS spectra in the Si 2p, O 1s and C 1s spectral range measured upon cooling from 800°C to 30°C. One can observe an increase of the C 1s peak intensity, indicating the reabsorption of C at the sample surface. However, no other significant changes could be

observed: the Si⁰, Si⁴⁺ and O 1s peak relative intensities, shapes and positions remained similar, indicating a stable binding configuration of SiO_x after in-situ annealing.

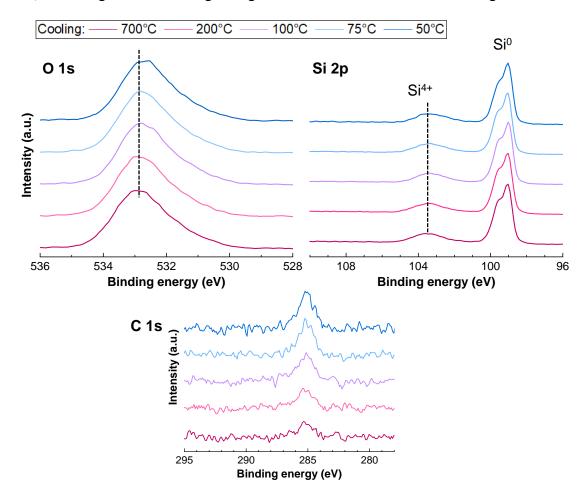


Figure 49. XPS Si 2p, O 1s and C 1s core level peaks measured on a SiO_x/c -Si sample after in-situ annealing of the sample in the XPS chamber. Five consecutive XPS measurements were performed upon cooling from 800°C to 30°C (the temperature associated to each spectrum is approximate, see **Figure 47**).

The evolution of the SiO_x layer observed upon in-situ annealing in the XPS chamber was found to be quite different from the evolution observed after ex-situ annealing in the tube furnace. To better emphasize the differences, a quantitative comparison of the XPS spectra obtained before and after annealing under the different conditions tested (tube furnace and XPS chamber) is proposed in the next paragraph.

c. Quantitative comparison of the XPS spectra after annealing

Table 10 presents the relative atomic concentration of Si, O and C, calculated from the ratio of the area of their respective core peaks (Si 2p, O 1s and C 1s) to the sum of all the core peak areas.

Table 10. Quantitative analysis of the XPS spectra measured on SiO_x/c-Si samples before and after annealing (ex-situ in the tube furnace and in-situ in the XPS chamber).

	Relative atomic concentration (%)				Relative percentage (%)				
Sample SiO _x /c-Si	Si	0	С	Si ⁰	Si⁺	Si ²⁺	Si ³⁺	Si ⁴⁺	
Before annealing	67.4	26.4	6.2	67.6	9.2	0	3.0	20.2	
After ex-situ annealing	59.3	35.0	5.7	49.6	9.1	0	0	41.3	
After in-situ annealing	70.8	26.4	2.8	70.0	7.4	0	5.2	17.4	

As qualitatively observed, an increase of the O relative concentration occurred during ex-situ annealing in the tube furnace, while it remained constant after in-situ annealing in the XPS chamber. This difference must result from a residual O concentration in the tube furnace whereas no significant O concentration likely remained in the XPS chamber.

The fit of Si 2p signal with full width at half maxima (FWHM) and peak positions in the range of the typical values of a silicon dioxide material¹⁷ also enabled to estimate the relative percentage of Si⁰, Si⁺, Si²⁺, Si³⁺ and Si⁴⁺ species (see **Table 10**). When comparing the relative percentage of species before and after ex-situ annealing in the tube furnace, one can observe:

- An increase of the Si⁴⁺ percentage and a decrease of the Si⁰ percentage, confirming the growth of the SiO_x layer during ex-situ annealing;
- A disappearance of the Si³⁺ suboxide to the benefit of Si⁴⁺, confirming the better stoichiometry of the SiO_x layer towards SiO₂.

On the contrary, after in-situ annealing in the XPS chamber, one can observe a similar distribution of the species compared to before annealing. The only slight differences were a decrease of the $\mathrm{Si^{4+}}$ percentage and increase of the $\mathrm{Si^{0}}$ and $\mathrm{Si^{3+}}$ ones, which likely indicates the degradation of the $\mathrm{SiO_{x}/c\text{-}Si}$ interface upon annealing under vacuum (already hypothesized from the preliminary qualitative analysis).

In conclusion, the evolution of the SiO_x/c -Si interface upon annealing was observed to strongly depend on the annealing atmosphere (see **Figure 50**). After annealing in the tube furnace under argon, a thicker and more SiO_2 -like layer was obtained, likely due to a residual O concentration in the furnace. On the contrary, upon in-situ annealing in the XPS chamber under vacuum, the SiO_x showed almost no variations except for a slight degradation of the SiO_x/c -Si interface. In the absence of an extra O source, two mechanisms could explain such an evolution of the SiO_x/c -Si interface:

■ A transversal diffusion of O towards the SiO_x surface, leading to a homogeneous SiO_x/c-Si interface of lower quality compared to before in-situ annealing;

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 $^{^{\}rm 17}$ see $\mbox{\bf Appendix B}$ for more details on the fitting procedure.

A lateral diffusion of O along the c-Si surface, leading to local regions of O-richer SiO_x and local regions of O-poorer SiO_x.

However, due to the large surface area analyzed by XPS ($^{\sim}$ 100 μm^2), this technique alone does not enable to discriminate which mechanism explains the SiO_x/c-Si evolution upon in-situ annealing.

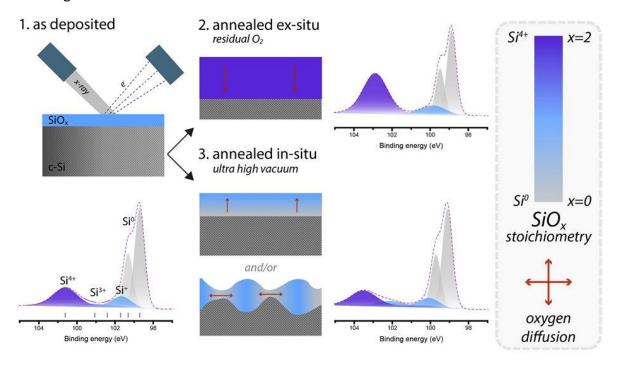


Figure 50. Schematic of the evolution of a thin SiO_x layer grown at the surface of a c-Si substrate upon annealing under different conditions.

2. XPS study of the poly-Si/SiO_x/c-Si stack

In this part, we elaborate on the in-depth XPS analysis of the complete poly-Si/SiO_x/c-Si stack. In-situ doped poly-Si/SiO_x contacts were fabricated on top of 4" mirror-polished c-Si wafers following the process described in **part 2-I-3** (targeting 15 nm-thick a-Si:H(B) and poly-Si layers). In-depth XPS measurements were performed after a-Si:H(B) deposition and after annealing for poly-Si crystallization at $T_a = 700^{\circ}$ C, 800° C and 900° C. Note that, in this part of the study, only ex-situ annealing in the tube furnace (under argon) is considered. The in-depth XPS analyses were performed by alternating etching steps (using 1 keV Ar ions) and XPS measurements. Knowing the thickness of the a-Si:H(B) and poly-Si layers, the XPS etching rate was estimated to be $0.03 \text{ nm} \cdot \text{s}^{-1}$.

The in-depth XPS spectra in the Si 2p and O 1s spectral range measured after a-Si:H(B) deposition and after annealing at $T_a = 700^{\circ}$ C are depicted in **Figure 51**.

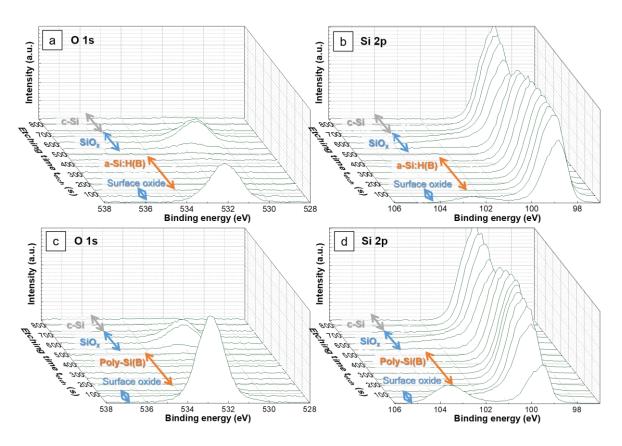


Figure 51. In-depth XPS O 1s and Si 2p respective core level peaks measured on samples consisting of a a-Si:H(B)/SiO_x/c-Si stack (a),(b) and a poly-Si(B)/SiO_x/c-Si stack (after annealing at $T_a = 700$ °C) (c),(d).

For an etching time of $t_{etch} = 0$ s (corresponding to the first XPS measurement), the Si 2p range featured two peaks characteristic of Si^0 and Si^{4+} . It indicates the presence of an oxide layer at the surface of the a-Si:H(B) and poly-Si(B) layers (confirmed by the detection of a peak in the O 1s range). For t_{etch} from 60 s to 480 s, the only peak detected was the Si^0 signature in the Si 2p range, corresponding to the a-Si:H(B) and poly-Si(B) layers (in which no significant O concentration is expected). For t_{ecth} from 540 s to 720 s, the presence of the interfacial SiO_x layer was evidenced by the reappearance of a small Si^{4+} peak in the Si 2p range and a peak in the O 1s range. For $t_{etch} \ge 780$ s, the Si^{4+} and O 1s peak disappeared again, indicating that the c-Si substrate was reached. The different layers/materials detected by XPS and their respective t_{etch} range are summarized in **Table 11**.

Table 11. Layers/materials detected by in-depth XPS measurement on a-Si:H(B) or poly-Si(B)/SiO $_x$ /c-Si stacks.

Etching time (s)	Peaks detected by XPS	Layer/Material
0	Si ⁰ ; Si ⁴⁺ ; O _{1s}	Surface oxide
60 - 480	Si ⁰	a-Si:H(B)/poly-Si(B)
540 – 720	Si ⁴⁺ ; O _{1s}	Interfacial SiO _x
> 780	Si ⁰	c-Si substrate

In the following, we will focus on the evolution of the two oxide layers (located at the sample surface and at the poly-Si/c-Si interface, respectively) upon annealing at various T_a values.

a. Qualitative study of the oxides upon annealing

Figure 52 depicts the O 1s and Si 2p spectral range of the XPS spectra measured in the region of the surface oxide and of the interfacial SiO_x (for $t_{etch} = 0$ s and $t_{etch} = 600$ s, respectively) before and after annealing. The XPS measurement performed at $t_{etch} = 0$ s corresponds to the first 5 nm at the top surface of the samples (i.e. the surface oxide layer and a few nanometers of the a-Si:H(B) or poly-Si layer underneath). The XPS measurement performed at $t_{etch} = 600$ s corresponds to the most intense O 1s peak detected in the interfacial SiO_x region ($t_{etch} = 540 - 720$ s).

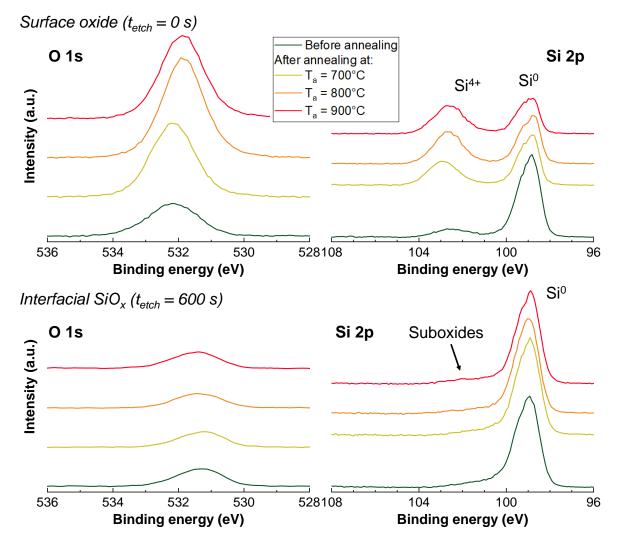


Figure 52. XPS O 1s and Si 2p core level peaks measured in the region of the surface oxide and of the interfacial SiO_x of a-Si:H(B)/SiO_x/c-Si and poly-Si(B)/SiO_x/c-Si samples before and after annealing at T_a , respectively. Note that the intensity scale is not depicted but was similarly set for the two O 1s and the two Si 2p graphs to enable a qualitative comparison of the peaks.

If one compares the XPS spectra measured in the O 1s range for the surface oxide and for the interfacial SiO_x, one can observe:

- A more intense O 1s signal for the surface oxide on all the investigated T_a range;
- An increase of the O 1s peak intensity with increasing T_a for the surface oxide, whereas the O 1s peak associated to the interfacial SiO_x remained constant.

In the Si 2p spectral range, one can observe:

- A more intense and better defined Si⁴⁺ peak for the surface oxide compared to the interfacial SiO_x, which exhibited only a small peak associated to suboxide species (see arrow in Figure 52);
- An increase of the Si⁴⁺ peak relative intensity and symmetry for the surface oxide, whereas the peak associated to suboxides in the interfacial SiO_x remained constant.

These observations of the O 1s and Si 2p spectral range evolution with increasing T_a indicate:

- An increase of the surface oxide thickness coupled with an improvement of its stoichiometry towards SiO₂, which is consistent with preliminary results obtained on the SiO_x/c-Si sample annealed at 800°C in the same tube furnace (see part 4-I-1);
- A constant thickness and stoichiometry of the interfacial SiO_x.

Moreover, the Si 2p signal measured at the sample surface before annealing featured a broad Si⁰ peak centered on 98.8 eV, characteristic of the amorphous Si layer (a-Si:H(B)) underneath the surface oxide. After annealing at T_a = 700°C and 800°C, one can observe the appearance of the Si $2p_{3/2-1/2}$ doublet shape, indicating the crystallization of the a-Si:H(B) layer into poly-Si. For T_a = 900°C, the doublet shape appeared less resolved, which could arise from the thicker oxide layer at the poly-Si surface, reducing the poly-Si thickness analyzed. On the contrary, the Si⁰ peak measured in the region of the interfacial SiO_x after annealing did not feature a doublet shape due to the etching process used that likely disturbed the sample structure.

In the next paragraph, we detail the quantitative analysis of the XPS spectra measured in the surface oxide and interfacial SiO_x regions.

b. Quantitative analysis

A quantitative analysis of the XPS spectra displayed **Figure 52** was performed. The relative atomic concentration of Si and O and the suboxide relative percentages were calculated from the peak areas and from the fit of the Si 2p spectral range (see **Appendix B**), respectively. The ratio of the sum of the O-rich sub oxides percentages (Si⁴⁺ and Si³⁺) on the sum of Si-rich sub oxides ones (Si²⁺ and Si⁺) was additionally calculated. Results are summarized in **Table 12** and **Table 13** for the surface oxide and for the interfacial SiO_x, respectively.

For the surface oxide (see **Table 12**), one can note that increasing T_a led to:

■ An increase of the relative O concentration at the sample surface up to 39.8% for $T_a \ge 800$ °C, confirming the growth of the surface oxide layer;

■ A decrease of the Si⁰ and Si⁺ relative percentage to the benefit of the Si⁴⁺ one, verified by the increase of the ratio of O-rich on Si-rich suboxide percentages. This result confirms the evolution of the surface oxide stoichiometry toward SiO₂.

Interestingly, from $T_a = 800^{\circ}\text{C}$ the O concentration (relative to Si) remained similar whereas the ratio of O-rich on Si-rich suboxides increased. This could indicate that, for $T_a \ge 800^{\circ}\text{C}$, the surface oxide saturates in O but its stoichiometry keeps improving toward SiO₂.

Moreover, it is worth recalling that whatever the T_a targeted, samples were loaded and unloaded at the same temperature¹⁸. Therefore, the increase of the surface oxide thickness with increasing T_a confirms that the surface oxidation of the samples occurred in the tube furnace, likely due to a residual O concentration.

Table 12. Quantitative analysis of XPS spectra measured at the surface (i.e. for $t_{etch} = 0$) of a-Si:H(B)/SiO_x/c-Si and poly-Si(B)/SiO_x/c-Si samples before and after annealing at T_a, respectively.

		atomic ation (%)		Relative	(Si ⁴⁺ +Si ³⁺)/				
Sample a-Si:H or poly-Si/SiO _x /c-Si	Si	О	Si ⁰	Si ⁺	Si ²⁺	Si ³⁺	Si ⁴⁺	(Si ²⁺ +Si ⁺)	
Before annealing	81.3	18.7	74.7	10.8	0	3.3	11.2	1.34	
T _a = 700°C	65.2	34.8	49.1	8.9	0.5	1.3	40.3	4.47	
T _a = 800°C	60.2	39.8	43.6	8.6	0	0	47.9	5.60	
T _a = 900°C	60.2	39.8	38.8	7.4	0	3.8	50	7.23	

For the interfacial SiO_x layer an example of the fit of the Si 2p range is depicted **Figure 53.** The quantitative analyses of the XPS spectra measured in the region of the interfacial SiO_x (see **Table 13**) showed that:

- The Si and O relative concentration remained constant with increasing T_a, at approximately 92% and 8%, respectively. This indicates that the residual O concentration in the tube furnace did not reach the interfacial SiO_x layer;
- The ratio of O-rich on Si-rich suboxides slightly increased with increasing T_a (from 0.38 to 0.52).

This last observation could arise from the evolution of the interfacial SiO_x layer toward an O-richer phase with increasing T_a , as already hypothesized in the literature [26]. However, the evolution of the suboxides distribution observed here is relatively small. Moreover, the XPS spectra obtained in the region of the interfacial SiO_x layer were measured after etching the sample with 1 keV Ar ions, which probably induced some modifications of the sample structure. Therefore, to confirm this observation, the in-depth XPS measurements should be reproduced with a softer etching method (e.g. using argon clusters) or with a higher energy

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 $^{^{\}rm 18}$ Only the time of ramp up and ramp down is varied to reach a different $T_{\rm a}.$

photon source that would enable a long enough depth-analysis to investigate the SiO_x interface without previous etching.

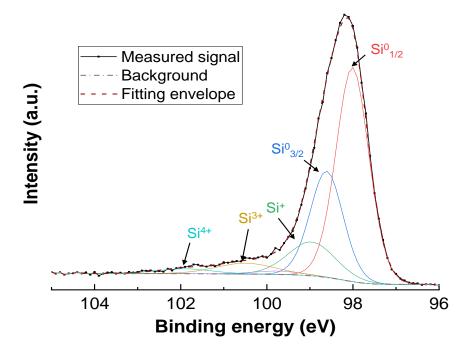


Figure 53. Fit of the Si 2p spectral range of the XPS spectra measured at the SiO_x interface ($t_{etch} = 600 s$) on poly-Si/SiO_x/c-Si sample after annealing at $T_a = 800$ °C.

Table 13. Quantitative analysis of the XPS spectra measured at the SiO_x interface ($t_{etch} = 600$ s) on a-Si:H/SiO_x/c-Si and poly-Si/SiO_x/c-Si samples before and after annealing at T_a , respectively.

		atomic ation (%)		Relative percentage (%)				(Si ⁴⁺ +Si ³⁺)/	
Sample a-Si:H or poly-Si/SiO _x /c-Si	Si	0	Si ⁰	Si ⁺	Si ²⁺	Si ³⁺	Si ⁴⁺	(Si ²⁺ +Si ⁺)	
Before annealing	91.5	8.5	75.4	17.7	0.2	5.9	0.9	0.38	
T _a = 700°C	92.4	7.7	82.9	9.4	3.0	4.8	0	0.38	
T _a = 800°C	92.6	7.5	79.9	12.1	1.2	4.8	2	0.51	
T _a = 900°C	91.4	8.6	78.4	11.8	2.4	5.1	2.3	0.52	

c. Structural evolution of the SiO_x at the poly-Si/c-Si interface

To investigate the structural evolution of the interfacial SiO_x layer upon annealing, TEM observations of the interface were performed on similar samples featuring the poly-Si-SiO_x contact before and after annealing at T_a in the range 700-900°C (see **Figure 54**).

After deposition, the interface between the a-Si:H(B) and the SiO_x layer was not well visible due to the amorphous nature of both layers. However, the formation of interference fringes at the SiO_x /c-Si interface enabled to detect a homogeneous bright zone along the c-Si surface, likely indicating that the interfacial SiO_x layer was continuous.

After annealing, the SiO_x layer was easier to detect at the poly-Si/c-Si interface. From the closer observation of the interface, one can observe that:

- For $T_a = 700$ °C, the SiO_x layer appeared continuous along the poly-Si/c-Si interface with a homogeneous thickness;
- For $T_a = 800$ °C, the SiO_x layer was still visible at the interface but its continuity and its thickness homogeneity seemed altered;
- For $T_a = 900$ °C, the interface appeared severely altered and remaining SiO_x regions at the poly-Si/c-Si interface were difficult to detect.

Note that, for $T_a = 900^{\circ}\text{C}$, the inability to observe the SiO_x at the poly-Si/c-Si interface could also result from a slight tilt of the lamella prepared for TEM. However, observations of this sample at a larger scale enabled to detect both regions with and without SiO_x at the poly-Si/c-Si interface, which confirms that the SiO_x layer was indeed locally disrupted (see **Figure 55**). Moreover, such a degradation of the SiO_x homogeneity at the interface after annealing at high T_a (typically in the range 900-1000°C) was already evidenced by TEM by several other groups [24,75,146,151].

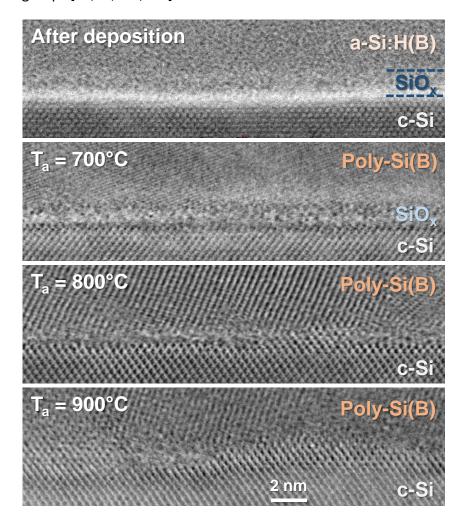


Figure 54. TEM images of the SiO_x interface of an a-Si:H(B)/SiO_x/c-Si sample after deposition, and of poly-Si(B)/SiO_x/c-Si samples after annealing at various T_a values in the range 700-900°C.

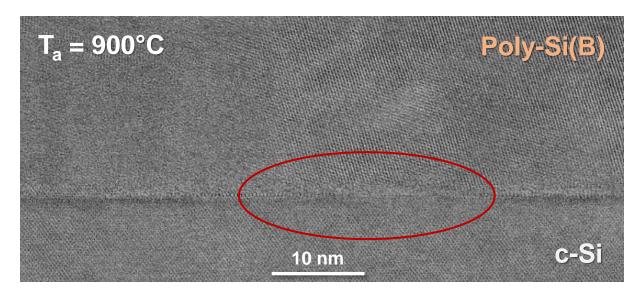


Figure 55. TEM image of the SiO_x interface of a poly- $Si(B)/SiO_x/c$ -Si sample after annealing at $T_a = 900$ °C.

3. Conclusions on XPS and TEM analysis of the interface

In this paragraph, the chemical and structural evolutions of the SiO_x layer (investigated by XPS and TEM, respectively) with increasing T_a are assessed. If one summarizes:

- The in-depth XPS analysis of the interfacial SiO_x layer indicated a constant O concentration in the SiO_x layer and a potential improvement of its stoichiometry towards SiO₂ with increasing T_a (which would need to be confirmed);
- The TEM observation of the SiO_x layer showed the degradation of the SiO_x homogeneity along the poly-Si/c-Si interface with increasing T_a .

These two results could be explained by a mechanism of local diffusion of the O atoms contained in the SiO_x layer. Indeed, a local O diffusion along the poly-Si/c-Si interface would lead to the formation of O-richer SiO_x local regions at the interface, combined to the formation of local direct poly-Si/c-Si interfaces. This hypothesis could explain that the macroscopic XPS measurement of the SiO_x interface (~ $100 \, \mu m^2$ top surface analysis) likely indicated a global improvement of the SiO_x layer stoichiometry towards SiO_2 whereas local observations of the interface by TEM rather emphasized the degradation of the SiO_x homogeneity. This hypothesis is supported by the observation made by Wolstenholme et al in ref. [75] of a "balling-up" effect of the SiO_x layer at the poly-Si/c-Si interface after annealing at even higher T_a value ($T_a = 1100$ °C). As the surface area of SiO_x balls after annealing corresponded to the surface area of the homogeneous SiO_x layer before annealing, they hypothesized that the transition occurred through the local diffusion of O atoms.

II. Investigation of the transport mechanism within the SiO_x layer

The transport of charge carriers through the poly-Si/SiO_x contact has recently been a matter of intense investigation [95,101,102,152]. More particularly, two hypotheses are likely to explain the transport of charge carriers through the thin SiO_x layer:

- The tunneling model predicts that charge carriers are transported through the SiO_x layer by tunnel effect [91];
- The pinholes model postulates a direct transport of charge carriers through nanometric break-ups (or "pinholes") within the SiO_x that would appear during the annealing step for poly-Si crystallization [92,93].

Conductive-Atomic Force Microscopy (C-AFM) has been identified as an interesting technique to investigate the presence of conductive pinholes within the SiO_x layer [98–100]. By performing C-AFM measurements on top of the poly-Si/SiO_x contact, localized regions of higher current intensity (conductive spots) can be observed on the resulting current maps. However, a clear link between these conductive spots and the presence of pinholes within the SiO_x layer has not been established yet.

In the present study, we first evaluated the impact of the surface preparation of the sample on the current levels obtained by C-AFM. Then, we investigated the link between conductive spots observed on C-AFM current maps and the presence of pinholes in the interfacial SiO_x layer by performing measurements in different configurations (transversal or lateral), with and without SiO_x layer at the poly Si/c Si interface.

1. Impact of the surface preparation of the sample on the C-AFM measurement

The in-depth XPS measurements performed on poly-Si contacts emphasized the presence of an oxide layer at the surface of the poly-Si layer, likely resulting from a residual oxygen concentration in the tube furnace used for crystallization annealing (see **part 5-I**). A preliminary study consisted in evaluating the impact of this surface oxide on the current levels detected by C-AFM.

In-situ doped poly-Si/SiO_x contacts were fabricated on the single-side of 4" mirror-polished c-Si substrates according to the process described in **part 2-I**. A first C-AFM measurement was performed in transversal configuration (i.e. the voltage was applied between the AFM tip and a contact located at the back side of the c-Si) on a sample featuring a 20 nm-thick poly-Si(B) layer after annealing at 700°C and storage in air for about a month. The oxide at the poly-Si(B) top surface was then removed through an HF cleaning step and followed by several transversal C-AFM measurements performed from 30 min to 5h after HF cleaning, the samples being stored under air in the meantime. The resulting current maps measured after annealing and at different times after HF cleaning are depicted in **Figure 56**. From the current maps, the histogram of current distribution was extracted (see **Figure 57**). After annealing, the current distribution curve features a peak at 3.9 pA corresponding to the mean current intensity (I_{mean})

and a maximum current intensity (I_{max}) detected at 5.8 nA. The C-AFM mapping performed 30 min after HF cleaning showed an increase of I_{mean} and I_{max} up to 0.25 nA and 114.7 nA respectively. The C-AFM mapping performed 2h after the HF cleaning step showed then a decrease of I_{mean} and I_{max} (down to 4.9×10^{-2} nA and 88.7 nA respectively) due to the re-growth of an oxide layer at the sample surface stored under air. The measurement performed 5h after cleaning showed similar values of I_{mean} and I_{max} than after 2h, indicating that the surface oxide layer did not evolve significantly in between these two measurements.

These results emphasized the impact of the oxide at the surface of the samples after annealing that decreased the current levels detected by C-AFM. To avoid any misinterpretation due to a different surface state, C-AFM measurements presented in the following part are performed with a constant delay between the HF cleaning of the sample and the measurement.

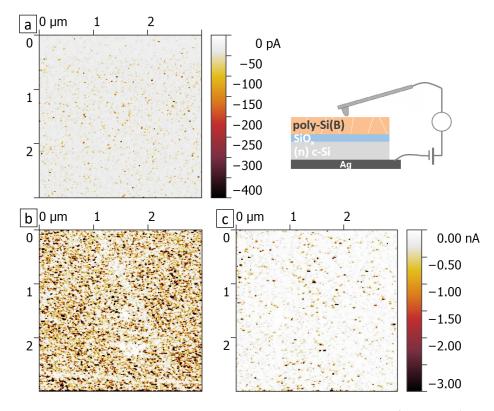


Figure 56. Current maps obtained by C-AFM measurement in transversal configuration (see schematic) on a 20 nm-thick poly Si(B) layer annealed at 700°C (stored in air for a month) (a) and at two different times after HF cleaning the poly-Si(B) surface (30 min (b) and 5h (c)).

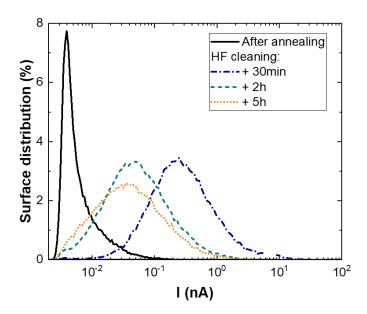


Figure 57. Histogram of current distribution (featuring 40 points per decade) extracted from C-AFM current maps measured at the poly-Si(B) surface in transversal configuration after annealing at 700°C and stored in air for a month and at different times after HF cleaning the poly-Si(B) surface (from 30 min to 5h).

2. C-AFM investigation of the pinholes formation within the SiO_x layer

In this paragraph, the link between the conductive spots detected by C-AFM (see **Figure 56**) and the presence of pinholes within the SiO_x layer is investigated. To this purpose, C-AFM measurements were performed on poly-Si/SiO_x contacts with SiO_x layers grown by different methods as well as without SiO_x layer at the poly-Si/c-Si interface.

In-situ doped poly-Si/SiO $_x$ contacts were fabricated on the single-side of 4" mirror-polished c-Si substrates. In this case, the interfacial SiO $_x$ layer was grown through two different methods:

- Either through the standard DIO₃ step at the end of the wafer cleaning process resulting in a 1.3 nm-thick chemical SiO_x layer;
- Or through a thermal oxidation of the c-Si substrates (performed at 840°C in a tube furnace with N_2 and O_2 as precursor gases), resulting in a 4 nm-thick thermal SiO_x layer.

Then, 20 nm-thick in-situ doped poly-Si(B) layers were fabricated on top of the chemical or thermal SiO_x layer. The annealing temperature for poly-Si crystallization was varied in the range $T_a = 700-900$ °C.

Samples "without interfacial SiO_x " were prepared by dipping the c-Si wafers in HF prior to the PECVD step for a-Si:H(B) deposition (delay < 5 min) in order to remove the interfacial SiO_x layer, leading to a poly-Si(B)/c-Si stack after annealing.

a. Transversal measurements

i. With and without interfacial SiO_X

C-AFM measurements were first performed in transversal configuration on samples featuring the standard chemical SiO_x layer after annealing at T_a = 700°C and 900°C (**Figure 58a** and **Figure 58b**, respectively). A constant delay of 2h was applied between the HF-cleaning of the sample and the C-AFM measurements.

For T_a from 700°C to 900°C, the density of conductive spots (> 1 nA) was found to increase from 55 μ m⁻² to 215.4 μ m⁻², respectively. The average current level (background and conductive spots) was also found to increase with increasing T_a , which is in good agreement with observations of Lancaster et al in ref. [98]. As hypothesized by Lancaster et al, the increase of the C-AFM current with increasing T_a could result from a lower electrical resistance of the SiO_x layer due to an enhanced formation of pinholes in the layer upon annealing at higher T_a . Moreover, the increase of conductive spot density with increasing T_a is consistent with the increase of pinhole density with increasing T_a observed by TMAH-based selective etching [95]. These observations could lead to the hypothesis that the conductive spots detected by C-AFM are mirroring pinholes within the interfacial SiO_x layer.

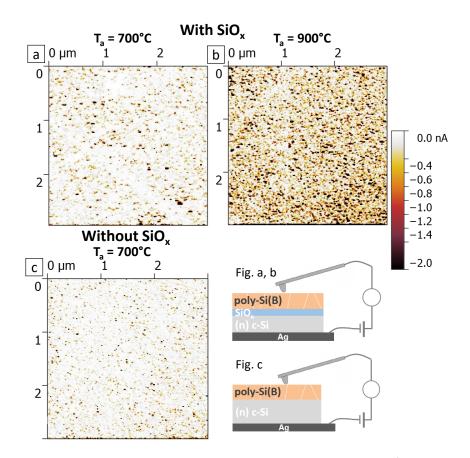


Figure 58. Current maps obtained by C-AFM measurements in transversal configuration at the surface of samples with an intentionally grown chemical SiO_x layer at the poly-Si(B)/c-Si interface after annealing at $700^{\circ}C$ (a) and at $900^{\circ}C$ (b). The same measurement was performed on a sample without interfacial SiO_x layer (after annealing at $700^{\circ}C$) (c). C-AFM measurements were performed 2h after HF-cleaning of the samples to ensure a similar surface state during measurement.

To further investigate the correlation between conductive spots and pinholes within the SiO_x layer, C-AFM measurements were performed in similar conditions on a poly-Si(B) layer ($T_a = 700^{\circ}\text{C}$) without interfacial SiO_x layer underneath (see **Figure 58c**). The C-AFM mapping was again performed 2h after HF-cleaning the sample. The pattern of the resulting current map was similar to the one obtained in the case of an intentionally grown interfacial SiO_x layer (**Figure 58a**), with a density of conductive spots in the same range ($50.8 \, \mu \text{m}^{-2}$). However, lower current levels were detected, although the resistance of the poly Si/c-Si stack was expected to be lower with the absence of the interfacial SiO_x layer. The slightly lower current levels obtained here could result from a larger resistance of the poly-Si layer itself as the crystalline structure of the poly-Si layer is expected to depend on the surface state of the c-Si wafer (oxidized or HF-cleaned) before deposition.

Despite the lower current levels, the detection of conductive spots when performing C-AFM measurements on a sample without interfacial SiO_x layer is disproving the hypothesis that conductive spots could mirror pinholes in the SiO_x layer.

ii. Comparison of chemical and thermal interfacial SiO_x layers

Similar transversal C-AFM measurements were performed on poly-Si/SiO_x contacts featuring a 1.3 nm-thick chemical SiO_x layer and a 4 nm-thick thermal SiO_x layer. Both samples were annealed for poly-Si crystallization at the intermediate temperature T_a = 800°C to enable the potential formation of pinholes in the chemical SiO_x layer while avoiding any break-ups of the thermal SiO_x. Resulting current maps are depicted in **Figure 59**. Higher current levels were measured on the sample featuring the thermal SiO_x compared to the chemical SiO_x, although the thicker thermal SiO_x layer was expected to induce a higher transverse resistance. Note that a lower conductive spot density was measured on the sample with the thermal SiO_x compared to the chemical SiO_x (110.2 μ m⁻² and 166.3 μ m⁻², respectively) but the average conductive spot size was found to be larger for the former sample compared to the sample with the chemical SiO_x.

Despite the different current levels, a similar pattern was observed on the C-AFM current maps measured on samples featuring chemical and thermal SiO_x layers. This observation also invalidates the potential link between conductive spots and pinholes as the formation of pinholes could potentially occur within the thin chemical SiO_x layer but was not expected in the thick thermal SiO_x .

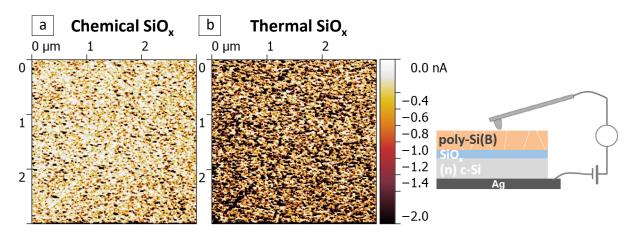


Figure 59. Current maps obtained by C-AFM measurements in transversal configuration at the surface of samples with a 1.3 nm-thick chemical SiO_x layer (a) and a 4 nm-thick thermal SiO_x layer (b) at the poly-Si(B)/c-Si interface after annealing at $T_a = 800$ °C. C-AFM measurements were performed 2h after HF-cleaning of the samples.

b. Lateral C-AFM measurements

To further investigate the origin of the conductive spots observed on C-AFM current maps, additional measurements were performed in lateral configuration (i.e. the voltage was applied between the AFM tip and a silver contact localized at the poly-Si(B) surface), with and without chemical SiO_x layer at the poly-Si/c-Si interface ($T_a = 700$ °C). C-AFM measurements were performed with a delay of 5h after HF cleaning of the sample. Resulting current maps are depicted in Figure 60. The current maps showed conductive spots (> 1 nA) with a density of 24.9 μm^{-2} and 11.2 μm^{-2} with and without SiO_x respectively. The current levels detected on the sample with interfacial chemical SiO_x were slightly higher than the ones detected without SiO_x layer, which is consistent with the transversal C-AFM measurements on similar samples (Figure 58a and Figure 58c, respectively) and supports the hypothesis that it could be related to changes in the conduction properties of the poly-Si layer. Note that the lower current levels and lower conductive spot densities detected in lateral configuration (Figure 60) compared to measurements in transversal configuration (Figure 58) probably result from the longer delay applied between the sample HF-cleaning and the lateral measurements (measured 3h later). A qualitative comparison of the lateral and transversal current maps is nevertheless possible. One can notice a similar current pattern in both configurations although the current is expected to flow principally in the poly Si layer in lateral configuration. These observations suggest that the conductive spots observed on C-AFM current maps are linked to the poly-Si microstructure rather than mirroring pinholes in the SiO_x layer. Conductive spots could be the result of a different local conduction in the poly-Si layer, e.g. the crystalline grains conducting differently than the grain boundaries (or remaining amorphous phases), as observed in ref. [153].

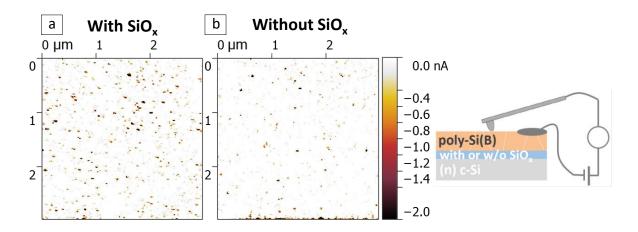


Figure 60. Current maps obtained by C-AFM measurements in lateral configuration on 20 nm-thick poly-Si(B) layers ($T_a = 700$ °C) with (a) and without (b) SiO_x layer at the poly-Si(B)/(n)c-Si interface. C-AFM measurements were performed 5h after HF-cleaning of the sample.

In conclusion, this C-AFM study emphasized the impact of the oxide layer at the sample surface on the detected current levels. It highlighted that, in order to compare C-AFM current maps measured on different samples, one must ensure a similar surface state of the samples during measurement. Moreover, the comparison of C-AFM measurements performed on poly-Si/SiO $_{\rm x}$ contacts with SiO $_{\rm x}$ layers grown by different methods, as well as without interfacial SiO $_{\rm x}$ layer, disproved the hypothesis that conductive spots detected by C-AFM mirror pinholes within the SiO $_{\rm x}$ layer.

3. KPFM investigation of the pinholes formation within the SiO_x layer

The Kelvin Probe Force Microscopy (KPFM) technique, which enables to measure the surface potential difference between the AFM tip and the sample, was applied by Kale et al on the SiO_x layer after etching of the poly-Si layer [23]. They could detect local regions of surface potential drops that they correlated with pinholes in the SiO_x (independently detected by TMAH selective-etching [95]).

In the frame of another PhD project, KPFM measurements of the poly-Si/SiO $_{x}$ contact developed in this work are ongoing (on similar samples than the ones investigated by C-AFM). In contrast to Kale's work, KPFM measurements were performed directly on top of the poly-Si layer. Results obtained so far showed that, after a similar HF cleaning of the poly-Si surface as the one applied before C-AFM measurements, local regions of surface potential drops could be observed (see **Figure 61a**). A density of local potential drops of 2.5×10^7 cm⁻² was estimated, which is in the same range as the pinhole density estimated by TMAH selective-etching (in the range of 5×10^6 cm⁻² to 1×10^8 cm⁻², depending on T_a). One can also note that the density of KPFM potential drops is significantly lower than the density of conductive spots measured by C-AFM (in the range of 1×10^9 cm⁻² to 3×10^{10} cm⁻²). This observation confirms that conductive spots measured by C-AFM are not exclusively the signature of pinholes in the SiO $_x$ layer but are also mirroring other phenomena linked to the poly-Si layer.

Moreover, KPFM measurements performed on samples without SiO_x layer at the poly-Si/c-Si interface resulted in homogeneous surface potential maps (see **Figure 61b**). This latter result suggests that local potential changes revealed by KPFM are related to local changes induced by the SiO_x layer. Whether these changes are related to pinholes in the SiO_x layer or to local changes of its thickness or composition should be further investigated.

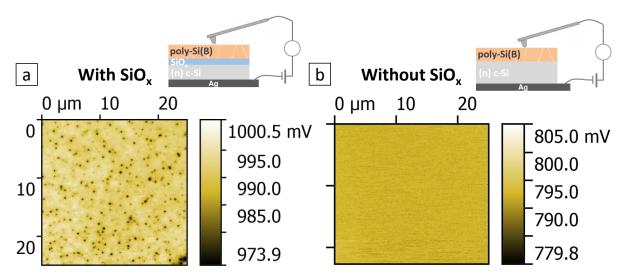


Figure 61. KPFM maps obtained on the poly-Si contact with (a) and without (b) SiO_x layer at the poly-Si/c-Si interface. Both samples were annealed at $T_a = 800$ °C. The KPFM measurements were performed approximately 2h after HF-cleaning of the samples.

III. Study of the poly-Si/c-Si interface recombination by lifetime spectroscopy

This part aims at characterizing the recombination activity at the SiO_x interface (between the poly-Si layer and the c-Si substrate) using injection dependent lifetime spectroscopy at different temperatures (T-IDLS). Such a method is conventionally used for bulk defects inducing discrete SRH recombination centers in the silicon band-gap. In the case of interface recombination, the defects (or interface states) at play are described by a continuous energy distribution throughout the band gap. Nonetheless, in the present work, we consider the simplifying option of modelling the recombination activity at poly-Si/c-Si interface by one or two single-level "apparent" SRH defects (see **part 2-II-2c**). The following paragraphs are focused on:

- The extraction of the surface recombination velocity (S in cm·s⁻¹) and corresponding surface-limited lifetime (τ_{surf} in s);
- The application of Murphy's approach of linearization of SRH equations [119], that allows to distinguish one or two individual defects driving the τ_{surf} dynamic;
- The application of T-IDLS fit routine to these individual defects in order to determine their most probable SRH parameters: their energy level in the band gap (E_t) and their ratio of capture cross-sections for electrons and holes (k).

In this study, we consider the following assumptions:

- Flat-band conditions;
- Low enough S values;
- Approximation of single-level interface state(s) limiting τ_{surf} .

Under these assumptions, the Murphy linearization and T-IDLS should be valid methods for characterizing the "apparent" single-level interface state(s) that drive τ_{surf} . The aim is then to find the most probable energy level E_t , symmetry factor k, and minority carrier surface recombination velocity (S_{p0} in the case of n-type c-Si) of the interface state(s) involved.

In order to meet the aforementioned assumptions, we considered the case of an intrinsic poly-Si(i)/SiO $_x$ contact after hydrogenation as the intrinsic poly-Si layer is expected to involve a smaller band bending in the c-Si compared to a highly-doped poly-Si(B) layer. Applying the method after hydrogenation ensures a better surface passivation (i.e. lower S values).

1. Sample preparation

Samples were made from a Cz(n) ingot sawed at INES with a dedicated sawing set-up involving alternate saw pitches, in order to get 440 μ m and 180 μ m-thick wafers from the same ingot. The wafers selected for the study had a resistivity of 2 Ω ·cm. The subsequent saw damage removal chemical step was done with various time durations in order to get three different thicknesses. Eventually, a common KOH-polishing step was applied to all the wafers to obtain the same surface roughness and to have similar surface properties for all samples. The final samples were thus 400 μ m, 160 μ m and 110 μ m-thick (with 5 wafers per group).

A chemical cleaning coupled with DIO_3 rinsing was performed to grow the thin SiO_x layer at the sample surfaces. Then, 30 nm-thick μ c-Si(i) layers were deposited by PECVD on both sides of the samples. The annealing step was subsequently performed at $T_a = 800^{\circ}$ C to obtain poly-Si(i)/SiO_x contacts. Eventually, the hydrogenation process (consisting of SiN:H deposition on both sides plus firing) was carried out on all the samples.

The effective minority carrier lifetime was measured as a function of the excess carrier concentration Δp by PCD at different temperatures T_{meas} ranging from 30°C to 170°C, to obtain the so-called injection dependent lifetime curves. Each sample was heated up to 170°C with a hotplate coupled to the PCD system. The PCD measurement was then performed every 5°C upon cooling. The sample passivation was verified to be thermally stable during the PCD heating process by performing PCD measurements at room temperature before and after the heating process. Moreover, the effective lifetime obtained by PCD on samples of similar thickness showed a good reproducibility, with a dispersion of less than 20% for each thickness batch. This indicates that the surface recombination velocities provided by our surface treatment are reproducible, and that the wafers having different thicknesses should have the same surface recombination velocities since they experienced the very same surface preparation.

2. Extraction of the surface recombination velocity

Firstly, the general eq. 19 was used to derive the S values and to verify if the condition $(S\,w)/D_h < 1/4$ that enables the use of the simplified eq. 20 was valid.

The $(S w)/D_h$ values obtained for T_{meas} from 30°C to 100°C are presented in **Figure 62.** The temperature dependence of the hole diffusivity in silicon $(D_h$, in $m^2 \cdot s^{-1})$ was calculated from [154]:

$$D_h = 0.218 \, T^{-0.9} \tag{eq. 31}$$

One can note that the resulting S values verify the condition $(S\,w)/D_h < 1/4$ only for $\Delta p > 3.10^{14}\,cm^{-3}$. For lower Δp values, the comparison of S values calculated from eq. 19 and eq. 20 shown a deviation of less than 20 %. Therefore, we considered the carrier diffusion towards the wafer surfaces as a negligible contribution to τ_{surf} , which is thus taken equal to 2S/w in the following.

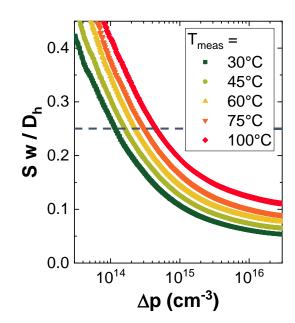


Figure 62. Surface recombination velocity (S) calculated from eq. 19 for the intermediate thickness $w = 160 \mu m$.

The simplified eq. 20 was used to extract the dependence of S versus Δp on our samples. **Figure 63** illustrates the procedure applied to the PCD measurement performed at $T_{meas} = 30^{\circ}\text{C}$. **Figure 63b** plots $\frac{1}{\tau_{eff}} = f\left(\frac{1}{w}\right)$ curves constructed from effective lifetimes measured at given carrier injection Δp of 1×10^{14} , 1×10^{15} and 1×10^{16} cm⁻³. The linear fit of such curves allows the extraction of S from the slope of the linear fit. However, the extraction of τ_{bulk} was not possible in this case because of the lifetime being limited by the surfaces. Therefore, the τ_{bulk} value was large compared to τ_{surf} and its extraction from the intercept was subjected to a significant error¹⁹.

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 $^{^{19}}$ As an example, for $\Delta p = 1 \times 10^{14}$ cm $^{-3}$, an error of 5% on the slope induces an error greater than 80% on the intercept.

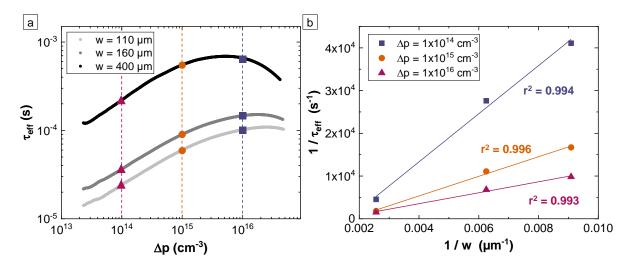


Figure 63. Effective minority carrier lifetime (τ_{eff}) versus minority carrier injection (Δp) measured at $T_{meas} = 30$ °C on symmetrical samples with hydrogenated poly-Si(i)/SiO_x contact fabricated from c-Si wafers of different thicknesses (w = 110, 160 and 400 μm) (a). Examples of $1/\tau_{eff} = f(1/w)$ curves for constant values of the carrier injection ($\Delta p = 1 \times 10^{14}$, 1×10^{15} and 1×10^{16} cm⁻³) (b).

The surface recombination velocity S at $T_{meas} = 30^{\circ}\text{C}$ is presented in **Figure 64a** as a function of Δp (in the range 2×10^{13} cm⁻³ to 5×10^{16} cm⁻³). For every T_{meas} considered, the r-square value associated with each linear fit was always superior to 0.98, indicating a good fit of the experimental data. **Figure 64b** depicts the whole set of S versus Δp curves obtained from lifetime data measured in the range 30-100°C. We focused the study on this T_{meas} range for the following reasons:

- Stay close to real-life PV module operating conditions;
- Avoid any transition to another temperature-activated surface recombination regime that could change the apparent limiting interface state(s), and prevent their analysis by lifetime spectroscopy.

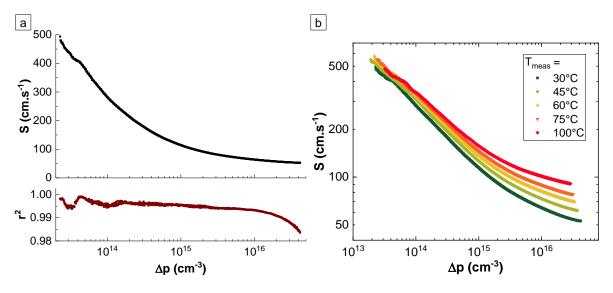


Figure 64. Surface recombination velocity (S) at the interface between the c-Si substrate and the poly-Si(i) contact versus the carrier injection (Δp) for $T_{meas} = 30^{\circ}C$ (upper graph). S was extracted from the linear fit of $1/\tau_{eff} = f(1/w)$ curves for each Δp value, r-squared (r^2) value associated to each linear fit

(lower graph) (a). S versus Δp curves extracted at different measurement temperatures T_{meas} in the range 30-100°C (b).

3. Linearization of τ_{surf} using Murphy's approach

The extraction of S at different temperatures T_{meas} enabled to derive the surface contribution τ_{surf} according to eq. 26. For the derivation of τ_{surf} we chose w = 400 µm because it corresponds to the highest τ_{eff} measured, thus minimizing the impact of noise on the measured τ_{eff} signal. Figure 65 depicts an example of τ_{surf} as a function of Y = p/n for T_{meas} = 30°C. The τ_{surf} versus Y curves obtained for other investigated T_{meas} values showed a similar trend (not displayed here). As the resulting τ_{surf} versus Y curves were not linear, the surface recombination could not be modeled via one single-level defect [119]. The presence of two independent single-level defects was thus assumed. For each T_{meas} , we investigated the least square fit of the τ_{surf} versus Y curves with two affine functions associated to the two defects.

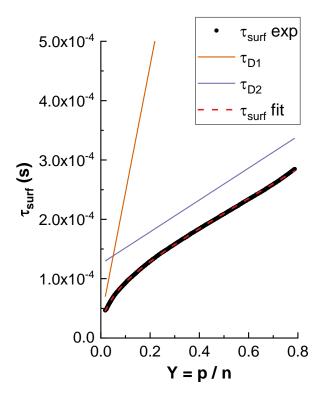


Figure 65. Surface-limited lifetime (τ_{surf}) versus Y = p/n for T_{meas} = 30°C. The curve was fitted with affine functions associated with two deep defects denoted D_1 and D_2 .

An example of the resulting fit is represented **Figure 65**. One can note that the slopes of the two affine functions where both positive indicating the detection of two deep defects (i.e. with energy levels near midgap). The defects associated with the affine function featuring high and low slopes are denoted D_1 and D_2 , respectively. For each T_{meas} , the coefficients $(a_i;b_i)$ of the two affine functions of equations $(a_iY + b_i)$ fitting the τ_{surf} versus Y curve are summarized in **Table 14** (with i = 1 and 2 for D_1 and D_2 , respectively).

Table 14. Coefficients of the two affine functions found for the fit of τ_{surf} (surface-limited lifetime) versus Y curves extracted at different temperatures (T_{meas}) in the range 30-100°C.

T _{meas} (°C)	a ₁	b ₁	a ₂	b ₂
30	2.14×10 ⁻³	3.11×10 ⁻⁵	2.69×10 ⁻⁴	1.25×10 ⁻⁴
45	1.54×10 ⁻³	3.15×10 ⁻⁵	1.99×10 ⁻⁴	1.46×10 ⁻⁴
60	1.28×10 ⁻³	3.24×10 ⁻⁵	1.90×10 ⁻⁴	1.38×10 ⁻⁴
75	1.31×10 ⁻³	3.59×10 ⁻⁵	1.69×10 ⁻⁴	1.34×10 ⁻⁴
100	1.18×10 ⁻³	3.96×10 ⁻⁵	1.37×10 ⁻⁴	1.21×10 ⁻⁴

4. Lifetime spectroscopy for the determination of the defect parameters

Subsequently, the parameters (E_t , k and S_{p0}) of the two interface states were determined through the Defect Parameter Solution Surface (DPSS) method (see **part 2-II-2c**). In this case, we worked with n-type c-Si, so the DPSS routine enables to determine the optimal fit values of ($\frac{1}{2}\frac{w}{s_{p0}}$; k) for a given E_t . The convergence of the DPSS diagrams calculated from a set of IDLS curves obtained at different temperatures enabled to identify the optimal values of parameters associated to D_1 and D_2 (see **Figure 66**). The combined relative standard deviation (RSD) of the DPSS-S_{p0} and DPSS-k curves featured two minima corresponding to the most probable energy levels ($E_t - E_v$) for D_1 and D_2 . Unique values of k and k0 could also be determined²⁰ and are reported in **Table 15**.

Table 15. Energy level (E_t - E_v), hole surface recombination velocity (S_{p0}) and symmetry factor (k) of discrete defects D_1 and D_2 used to model surface-limited lifetime at the interface between the c-Si and the poly-Si(i)/SiO_x contact.

	E _t – E _v (eV)			
Interface state	Solution 1	Solution 2	S _{p0} (cm·s ⁻¹)	k
D_1	0.35±0.02	0.62±0.02	8.1×10 ² ±2.7	53.4±20
D ₂	0.35±0.02	0.72±0.02	1.5×10 ² ±0.4	2.1±0.8

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 $^{^{20}}$ A 15% error margin was applied to the RSD minima value leading to the determination of the error margins on the two (E_t - E_v) solutions and subsequently on the S_{p0} and k values (see light blue domains in **Figure 66**).

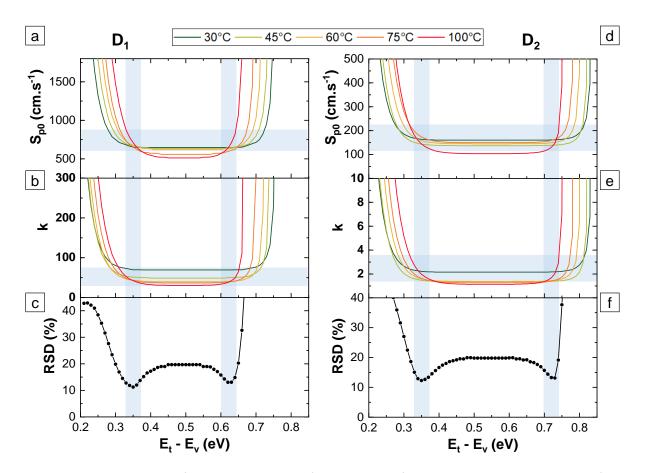


Figure 66. DPSS analysis of the contributions of the two interface states D_1 and D_2 extracted from injection-dependent lifetime curves measured at different temperatures T_{meas} in the range 30-100°C. For the interface state D_1 : superposition of all the DPSS- S_{p0} (a) and DPSS-k (b) curves and combined relative standard deviation (RSD) of the DPSS- S_{p0} and DPSS-k curves (c) as a function of the energy level (E_t - E_v). Similar curves are displayed for the interface state D_2 (d), (e) and (f).

In conclusion, in this work, we could model the recombination activity at the interface between an intrinsic poly-Si/SiO_x contact and the c-Si substrate. We first isolated the contribution of the lifetime limited by the surfaces (τ_{surf}) based on its dependence on the wafer thickness. Then, we could linearize the resulting τ_{surf} versus injection curves to separate the contribution of two independent single-level defects at the interface. The application of lifetime spectroscopy methods on the lifetime contribution associated to these defects finally enabled to determine, for each of them, two solutions of energy levels E_t in the bandgap and a single value of ratios of electron and hole capture cross sections²¹. The application of additional lifetime spectroscopy methods (TDLS or N_{dop} -IDLS) could enable to:

- Verify the solutions (E_t; k) obtained by T-IDLS;
- Discriminate the most probable energy level between the two solutions found.

-

²¹ Note that this study was performed with the poly-Si contact fabricated on n-type c-Si substrates. Although the defects at the interface between the poly-Si contact and a p-type c-Si substrate could be the same, their impact on the interface recombination activity would probably be different e.g. due to a strong dissymmetry of the capture cross sections.

Moreover, note that, even if we worked with intrinsic poly-Si contacts, the solutions of apparent single-level defects found in this work could be a first step to model the recombination activity at the interface between a doped poly-Si/SiO_x contact and the c-Si substrate.

Conclusion

In this part, we elaborated on the investigation of the transport and passivation properties of the poly-Si/SiO $_x$ contact with a particular focus at the poly-Si/c-Si interface.

Firstly, the chemical and structural evolutions of the interfacial SiO_x during annealing for poly-Si crystallization were studied by means of in-depth XPS and TEM, respectively. Preliminary XPS results indicated that the evolution upon annealing of a SiO_x layer at the surface of a c-Si substrate strongly depends on the annealing atmosphere. Then, in-depth XPS analyses on the complete poly-Si/SiO_x/c-Si stack enabled to study the surface oxide and the interfacial SiO_x upon annealing for crystallization. For the surface oxide, we observed a thickness increase and a stoichiometry improvement toward SiO_2 with increasing annealing temperature, whereas for the interfacial SiO_x , no significant changes were observed except for a slight improvement of its stoichiometry. Additional TEM observations of the SiO_x interface also evidenced a degradation of the SiO_x homogeneity along the interface with increasing T_a , which could result from a mechanism of lateral O diffusion at the interface.

Secondly, we investigated the presence of nanometric break-ups (or pinholes) within the SiO_x layer (that would help the transport of charge carriers through the contact) by means of C-AFM measurements. We showed the need to remove the oxide layer at the samples surface as it mitigated the current levels measured by C-AFM. Moreover, we emphasized the limit of the C-AFM technique to detect pinholes within the SiO_x layer. However, preliminary results obtained by KPFM indicated that this technique could be more adapted to the detection of pinholes.

Finally, a method for characterizing recombinant defects at the interface between an intrinsic poly-Si contact and the c-Si substrate was developed. This method is based on lifetime spectroscopy techniques applied to the lifetime limited at the c-Si surface. This surface method enabled to model the recombination phenomena at the poly-Si/c-Si interface via two apparent discrete defects. For each defect, two solutions of energy levels E_t in the bandgap and a single value of ratios of electron and hole capture cross sections could be estimated. The application of an additional lifetime spectroscopy methods (e.g. TDLS or N_{dop} -IDLS) could enable to: (i) verify the solutions of E_t and k given by T-IDLS and (ii) discriminate the most probable energy level among the two solutions found.

General conclusion and perspectives

In the context of high-efficiency c-Si solar cells, the integration of passivating contacts consisting of a poly-Si layer on top of a thin SiO_x layer is sparking interest to further reduce the recombination at the interface between the metal electrode and the c-Si substrate.

The objectives of this work were to fabricate, optimize and analyze the properties of boron-doped poly-Si/SiO_x passivating contacts. We first elaborated on the state-of-the-art of poly-Si/SiO_x contacts in **part 1**. Then, we introduced the many different experimental techniques on which the present work was based in **part 2**.

The work was then shared between two main objectives that were addressed in the two following parts.

In **part 3**, we investigated two routes for the fabrication of highly-passivating poly-Si/SiO_x contacts using various layers deposited by PECVD: (i) from annealing of an in-situ doped a-Si:H(B) layer on top of the thin SiO_x layer, and (ii) from an intrinsic microcrystalline silicon layer that was ex-situ doped by annealing after deposition of a top boron-rich SiO_xN_y:B layer.

In the case of the in-situ doped route, the optimization of the deposition conditions of a-Si:H(B) layers enabled to obtain blister-free poly-Si(B) layers after annealing, providing stable surface passivation properties over time. The surface passivation properties obtained with the resulting in-situ doped poly-Si/SiO_x contact were evaluated on ~156 mm² wet-oxidized c-Si substrates with PV compatible surface roughness (i.e. KOH-polished), for a facilitated integration at the rear side of a p-type c-Si solar cell. A maximum iV_{oc} value of 734 mV (associated to $J_0 = 7 \text{ fA·cm}^{-2}$) was obtained after subsequent hydrogenation process using a top SiN:H layer. This result is among the best ones reported so far for p⁺-poly-Si contacts, and is very promising for device integration.

The ex-situ doped route was originally motivated by the fact that the H-rich boron precursor gas used for in-situ doping is likely enhancing the blistering phenomenon. Interestingly, we found that the electrical and passivation properties of the ex-situ doped poly-Si contact could be at the same high level as that of the reference in-situ doped ones, although the crystallization and doping mechanisms involved were different.

The excellent passivation properties provided by the poly-Si contact results from the combination of (i) the thin SiO_x layer, (ii) the high doping of the poly-Si layer and (iii) the additional hydrogenation of the poly-Si/SiO_x contact from the top SiN:H layer. However, the respective effect of these different contributions is difficult to discriminate. In this work, the comparison of the surface passivation properties provided by poly-Si/SiO_x contacts, either being ex-situ doped or not, underlined the importance of the field-effect passivation (related to the poly-Si high doping level) on the stability of passivation upon following high temperature steps (e.g. annealing for crystallization, firing for hydrogen diffusion). The diffusion of H from the top SiN:H layer in the ex-situ doped poly-Si/SiO_x contact was

investigated by SIMS profiling. Results emphasized an accumulation of H at the SiO_x interface for both doped and undoped contacts, confirming that H atoms are providing an additional chemical passivation of the interface. However, a similar H concentration was observed at the SiO_x interface of samples annealed at different temperatures T_a . Thus, the drop of passivation observed at high T_a could not be explained by a different H diffusivity in these samples.

In **part 4**, the transport and passivation mechanisms of the resulting poly-Si/SiO $_x$ contacts were investigated in more details, with a particular focus on the interfacial SiO $_x$ layer.

Firstly, the chemical and structural evolutions of the interfacial SiO_x during annealing for crystallization were analyzed by means of in-depth XPS and TEM, respectively. In-depth XPS analyses of the complete poly-Si/SiO_x/c-Si stack enabled to study both surface oxide and interfacial SiO_x upon annealing for crystallization. For the surface oxide, we observed a thickness increase and a stoichiometry improvement toward SiO_2 with increasing annealing temperature, whereas for the interfacial SiO_x , no significant changes were observed except for a slight improvement of its stoichiometry. However, the etching method used for in-depth XPS could have induced modifications of the samples structure, thus, these measurements should be reproduced with a softer etching method (e.g. using argon clusters) or with a higher energy photon source that would avoid etching. Complementary TEM observations of the interfacial SiO_x layer also evidenced a degradation of the SiO_x homogeneity along the interface with increasing annealing temperature (for poly-Si crystallization), which could result from a mechanism of lateral O diffusion.

Secondly, we investigated the presence of nanometric break-ups (so called pinholes) within the SiO_x layer (that would help the transport of charge carriers through the contact) by means of C-AFM measurements. We showed the need to remove the oxide layer forming at the sample surface as it mitigated the currents measured. We demonstrated that, after removal of the surface oxide, the high current dots observed in the C-AFM current maps are not representative of pinholes within the SiO_x layer but are rather linked to the poly-Si surface and microstructure properties.

Finally, a method for characterizing recombining defects at the interface between intrinsic poly-Si and the c-Si substrate was proposed. This method is based on lifetime spectroscopy techniques (SRH linearization and T-IDLS), which were used in the literature for the determination of bulk defects. They were extended in this work to determine surface properties through measurements on wafers of various thicknesses. A simplified approach enabled to model the recombination phenomena at the poly-Si/c-Si interface via two apparent discrete defects. For each defect, two solutions of energy levels Et in the bandgap and a single value of ratios of electron and hole capture cross sections could be determined.

This thesis work opens up many perspectives. One of the most important is the integration of poly-Si contacts into solar cells. Ongoing research in the frame of another PhD project at INES

is focused on the integration of the in-situ doped poly-Si contact at the rear side of a p-type c-Si solar cell. Due to the high sheet resistance of the thin poly-Si layer (< 30 nm), a full area metallization of the poly-Si layer is targeted. The deposition of Ag by PVD on top of the poly-Si layer was so far the best compromise between preserving the surface passivation and enabling a good electrical contact [155].

Moreover, preliminary results obtained in this work suggested that H atoms diffusing from the SiN:H layer are accumulating within the interfacial SiO_x layer. However, the mechanisms of H diffusion and interaction with the interface are not fully understood yet, which is mainly due to the difficulty of characterizing light and mobile H atoms. Therefore, the investigation of H-related mechanisms will be the main focus of a coming PhD project.

Regarding the characterization of the transport mechanism of charge carriers through the SiO_x layer, preliminary results obtained from another AFM-derived technique, Kelvin Probe Force Microscopy, suggested that this technique is likely more adapted to the pinhole detection. Moreover, it has been shown in the literature that I-V measurements performed as a function of temperature could enable to discriminate the dominating transport mechanism (i.e. tunnel effect or pinholes-related). This kind of measurements is thus ongoing to further investigate the dominating transport mechanism within the in-situ doped poly-Si/SiO $_x$ contact fabricated in this work.

Finally, regarding the characterization of recombining defects at the interface, the application of additional lifetime spectroscopy methods (e.g. TDLS or N_{dop} -IDLS²²) in future works could enable to verify the validity of the parameters found for the two apparent discrete defects and to discriminate the most probable energy level among the two solutions extracted by T-IDLS. Although the work was performed with intrinsic poly-Si contacts, the defect parameters we found could also be used in future work as a first estimation to model the recombination activity of the poly-Si contact integrated in a solar cell (i.e. featuring a highly-doped poly-Si layer).

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 $^{^{22}}$ TDLS focuses on low-injection lifetime data on a broad temperature range, and N_{dop}-IDLS consists in analyzing several IDLS curves measured for different doping densities of the substrate.

Appendix A: Correction of ECV profiles measured on ex-situ doped poly-Si contacts

Active B doping profiles were measured by ECV on ex-situ doped poly-Si contacts as a function of the annealing temperature T_a . Samples were made from 4" mirror-polished c-Si wafers, the ex-situ doped poly-Si/SiO_x contact was fabricated according to the process described **part 2-I-4**. The annealing temperature T_a was varied in the range 700-850°C. The SiON:B doping layer was etched through a HF dip step before performing the ECV measurement.

The as-measured ECV profiles are depicted in **Figure 67a**. For $T_a = 700^{\circ}\text{C}$, we observed a gradient of B concentration in the poly-Si layer ranging from 2×10^{20} cm⁻³ to 2×10^{19} cm⁻³. For $T_a \geq 800^{\circ}\text{C}$, the active B doping concentration in the poly-Si layer converged to a plateau centered around 3×10^{20} cm⁻³ and B dopants started diffusing in the c-Si substrate.

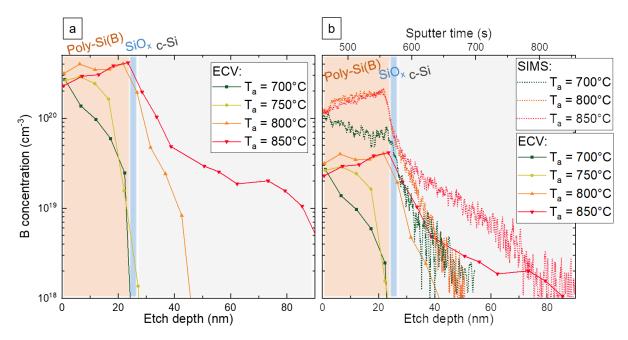


Figure 67. As-measured hole (approximated as active B) concentration profiles obtained by ECV on exsitu doped poly-Si contacts after annealing in the range T_a = 700-850°C (a). Similar ECV active B profiles corrected according to the active B concentration assessed by Hall effect measurement and total B concentration profiles measured by SIMS (b).

The active doping concentration, conductivity and mobility were evaluated by Hall effect measurements on similar samples (see **Table 16**). Note that the Hall effect measurement was only performed after annealing at T_a =700 and 750°C to ensure no B diffusion in the c-Si substrate as it would lead to current flowing in the B-doped region of the c-Si and would result in an inaccurate evaluation of the poly-Si electrical properties.

The Hall B doping concentration was evaluated around 1.2×10^{19} cm⁻³ and 1.5×10^{19} cm⁻³ for T_a = 700 and 750°C respectively. These values appeared to be ten times lower than the active B concentration assessed by ECV.

Table 16. Electrical properties of ex-situ doped poly-Si layer obtained by Hall effect measurement after annealing at $T_a = 700$ and 750°C.

T _a (°C)	Active B concentration (cm ⁻³)	Conductivity (S.cm)	Mobility (cm ² .V ⁻¹ .s ⁻¹)
700	1.2×10 ¹⁹	49.2	26.1
750	1.5×10 ¹⁹	54.0	23.9

The total B concentration was measured by SIMS on similar samples annealed at T_a = 700, 800 and 850°C (see **Figure 67b**). For T_a = 700°C, we observed a gradient of total B concentration in the poly-Si layer that followed well the active B profile measured by ECV. However, the total B concentration was ranging from 1×10^{20} cm⁻³ to 5×10^{19} cm⁻³, which is lower than the active B concentration measured by ECV. Similarly, for T_a = 800 and 850°C, the shape of the SIMS total B profile was in good agreement with the one of the ECV active B profile but again the total B concentration in the poly-Si layer appeared lower than the active one (plateau centered around 1.6×10^{20} cm⁻³ and 3×10^{20} cm⁻³ respectively). Thus, ECV and SIMS results are not in good agreement, as we expect the active B concentration to be lower than the total B concentration, especially in highly defective poly-Si layers.

In conclusion, the active B concentration in the ex-situ doped poly-Si layer measured by ECV appeared ten times higher compare to Hall effect measurement. Moreover, it appeared higher than the total B concentration obtained by SIMS. Therefore, the ECV seems to overestimate the active B concentration in the ex-situ doped poly-Si layer, which could arise from a misestimated etching rate of the poly-Si phase during the measurement. Hall effect and SIMS measurements appeared in better agreement, with the Hall active B concentration found approximately ten times lower than the SIMS total B concentration in the poly-Si layer.

For $T_a = 750^{\circ}\text{C}$, the active B profile in the poly-Si layer showed the most plateau-like shape coupled with no B diffusion in the c-Si. Therefore, in a first approximation, this profile was corrected according to the active B concentration measured by Hall effect under the same conditions ($T_a = 750^{\circ}\text{C}$). The ECV profiles measured at $T_a = 700$, 800 and 850°C were shifted accordingly (see **Figure 67b**), as their active B concentration could not be assessed accurately by Hall effect measurement due to a B gradient in the poly-Si layer for $T_a = 700^{\circ}\text{C}$ or B diffusion in the c-Si for $T_a \ge 800^{\circ}\text{C}$. One can observe on the ECV profile measured for $T_a = 750^{\circ}\text{C}$ that the poly-Si layer was not completely filled with active B. Therefore, the correcting method based on this profile is still subjected to a certain error. A better correction of the ECV profiles could consist in estimating a more accurate etching rate of the poly-Si layer with the ECV etching solution.

Appendix B: Fitting procedure of the XPS Si 2p spectral range of a SiO_x layer

This appendix aims at presenting the fitting procedure used for the deconvolution of the Si 2p spectral range measured by XPS on a silicon dioxide (SiO_x) layer.

There are five possible oxidation states for silicon (Si): elemental Si and SiO₂ that are denoted Si⁰ and Si⁴⁺, respectively and suboxide species characterized by a Si atom bonded with one, two or three O atoms that are denoted Si⁺, Si²⁺, and Si³⁺, respectively[149].

The typical XPS spectra in Si 2p core level spectral range associated to a SiO_x layer consists of (i) a peak around 98.8 eV, which is the signature of Si⁰ and (ii) a peak around 102.8 eV attributed to Si⁴⁺ (see **Figure 68**). The shape of the Si 2p signal in between the Si⁰ and Si⁴⁺ peaks depends on the presence (or not) of the other suboxides (Si⁺, Si²⁺, and Si³⁺). Therefore, the fit of the Si 2p band with full width at half maxima (FWHM) and peak positions in the range of the typical values of a SiO_x material enables to estimate the relative percentages of the suboxides present in the SiO_x phase (Si⁰, Si⁺, Si²⁺, Si³⁺ and Si⁴⁺). **Figure 68** shows an example of such a deconvolution of the Si 2p band with Gaussian curves associated to the different oxidation states of Si.

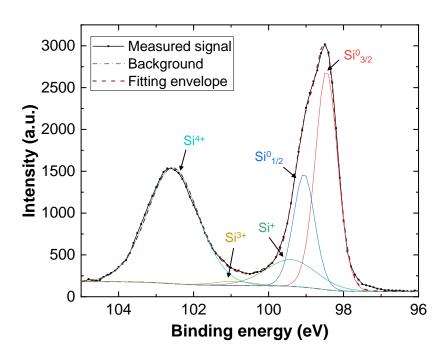


Figure 68. Example of the deconvolution of the Si 2p spectral range measured by XPS on a SiO_x layer.

In this work, the fit of the Si 2p band measured by XPS on SiO_x layers was performed with the CasaXPS software. The fitting procedure was carried out as follows:

■ The Si⁰ peak was fitted with two Gaussian curves associated to the Si 2p doublet (Si 2p_{3/2-1/2} associated to the spin-orbit coupling). A chemical shift of 0.6 eV was applied

- to the Si $2p_{3/2}$ peak relatively to the Si $2p_{1/2}$ peak. The area of the Si $2p_{3/2}$ peak was set as half the Si $2p_{1/2}$ one ;
- The suboxide species (Si⁺, Si²⁺, Si³⁺ and Si⁴⁺) were fitted with one Gaussian curve each, with a respective chemical shift of 0.95 eV, 1.75 eV, 2.48 eV and 3.9 eV relatively to the Si $2p_{3/2}$ peak. The FWHM of each sub-oxide peak was set in the range 1.2-1.6 eV.

List of publications

Publications in peer-reviewed journals

<u>A. Morisset</u>, R. Cabal, V. Giglia, B. Grange, J. Alvarez, S. Dubois, M.-E. Gueunier-Farret, J.-P. Kleider, SiO_xN_y:B Layers for Ex-Situ Doping of Hole-Selective Poly-Silicon Contacts, *AIP Conf. Proc. 2147* (2019) 040012.

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<u>A. Morisset</u>, R. Cabal, B. Grange, C. Marchat, J. Alvarez, M.-E. Gueunier-Farret, S. Dubois, J.-P. Kleider, Conductivity and Surface Passivation Properties of Boron-Doped Poly-Silicon Passivated Contacts for c-Si Solar Cells, *Phys. Status Solidi A.* (2018) 1800603.

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Contributions in conferences

<u>A. Morisset</u>, R. Cabal, V. Giglia, B. Grange, J. Alvarez, S. Dubois, M.-E. Gueunier-Farret, J.-P. Kleider, " SiO_xN_y :B Layers for Ex-Situ Doping of Hole-Selective Poly-Silicon Contacts", 9th International Conference on Silicon Photovoltaics, Leuven (Belgium) – **Poster presentation**

<u>A. Morisset</u>, R. Cabal, B. Grange, C. Marchat, J. Alvarez, M.-E. Gueunier-Farret, S. Dubois, J.-P. Kleider, "Highly Passivating & Blister-free PECVD Poly-Silicon for Large Area Silicon Solar Cells", 35th European PV Solar Energy Conference and Exhibition (EUPVSEC), Brussels (Belgium) – **Oral presentation**

<u>A. Morisset</u>, R. Cabal, B. Grange, C. Marchat, J. Alvarez, M.-E. Gueunier-Farret, S. Dubois, J.-P. Kleider, "Conductivity and Surface Passivation Properties of Boron-Doped Poly-Silicon Passivated Contacts for c-Si Solar Cells", 2018 Spring Meeting of the European Materials

Research Society (E-MRS), Strasbourg (France) – **Oral presentation** – **Young scientist award for symposium I**

<u>A. Morisset</u>, R. Cabal, B. Grange, C. Marchat, J. Alvarez, M.-E. Gueunier-Farret, S. Dubois, J.-P. Kleider, "Improvement of the Conductivity and Surface Passivation Properties of Boron-Doped Poly-Silicon on Oxide", 8th International Conference on Crystalline Silicon Photovoltaics (Silicon PV), Lausanne (Switzerland) – **Poster presentation**

<u>A. Morisset</u>, R. Cabal, B. Grange, C. Marchat, J. Alvarez, M.-E. Gueunier-Farret, S. Dubois, J.-P. Kleider, "Développement de poly-silicium dopé Bore par voie PECVD pour la passivation des contacts des cellules solaires", Journées Nationales du Photovoltaïque 2017, Dourdan (France) – **Poster presentation**

Résumé des travaux

I. Contexte et objectifs

Dans le contexte actuel d'urgence climatique, il apparaît indispensable d'opérer une transition vers des sources d'énergie renouvelable. La production d'électricité photovoltaïque (PV) est en forte croissance au niveau mondial, et cette source d'énergie renouvelable est amenée à jouer un rôle majeur dans les futurs scénarios de mix énergétique. Le marché du PV est largement dominé par les cellules PV à base de silicium car elles allient hautes performances, bas coûts de production et stabilité à long terme, ce qui permet un coût de production d'électricité compétitif. Le développement à encore plus grande échelle des technologies PV silicium repose sur : 1/ l'augmentation des performances des cellules et modules PV et 2/ l'amélioration des procédés de fabrication (simplification et réduction des coûts). Les cellules PV silicium actuellement fabriquées à l'échelle industrielle affichent des rendements de l'ordre de 22%. L'augmentation des performances de ces cellules passe par le développement de nouvelles structures de contacts dits « passivés » afin de limiter les pertes par recombinaisons des porteurs de charge notamment à l'interface entre le métal et le substrat de silicium cristallin (c-Si).

Une approche de contacts passivés consiste à intégrer entre le métal et le c-Si une jonction composée d'une couche de silicium poly-cristallin (poly-Si) fortement dopée sur une mince couche (< 2 nm) d'oxyde de silicium (SiO_x). Cette jonction combine des effets avancés de passivation de l'interface métal/c-Si tout en permettant une collecte efficace des porteurs de charge. L'intégration de cette jonction en cellule PV est en plein essor, et a déjà montré des performances très prometteuses sans alourdir les procédés de fabrication [62,156]. Cependant, les mécanismes physiques qui expliquent le bon fonctionnement de la jonction sont encore mal maîtrisés. Le transport des charges au travers de la couche SiO_x est notamment activement étudié afin de comprendre s'il s'agit d'un transport par effet tunnel ou d'un transport direct par le biais d'ouvertures nanométriques formées au sein de la couche pendant le procédé de fabrication de la jonction. Les phénomènes de recombinaisons des charges à l'interface entre la jonction et le substrat c-Si sont aussi difficiles à caractériser car ils sont sujets à des évolutions au cours du procédé de fabrication.

Les objectifs de la thèse sont d'une part de développer une jonction poly-Si/Si O_x compatible avec la fabrication industrielle des cellules PV, et d'autre part d'améliorer la compréhension des mécanismes de transport des charges au sein de la couche Si O_x ainsi que des phénomènes de recombinaisons à l'interface entre la jonction et le c-Si.

- II. Développement du contact poly-Si/SiO_x
 - 1. Poly-Si dopé in-situ
 - a. Réduction du phénomène de cloquage

Le premier objectif de la thèse était de développer une jonction poly-Si/SiO_x à intégrer entre le métal et le c-Si afin de réduire les recombinaisons à cette interface et d'augmenter le potentiel de rendement des cellules PV silicium développées au laboratoire.

Le procédé développé consiste en la croissance d'une couche de SiO_x de 1,3 nm d'épaisseur réalisée par rinçage ozoné du substrat. Une couche de silicium amorphe hydrogéné (a-Si:H) de 30 nm d'épaisseur est ensuite déposée par voie chimique assistée par plasma (PECVD) à 220°C. Cette couche de a-Si:H est dopée au bore pendant le dépôt par ajout de diborane aux gaz précurseurs. L'échantillon est ensuite recuit entre 700°C et 900°C sous argon afin de cristalliser le silicium amorphe en poly-Si. Le recuit permet aussi d'activer les atomes de bore, c'est-à-dire de libérer les porteurs de charges supplémentaires (trous) qui leurs sont associés. Le dépôt PECVD a été choisi car il est répandu dans l'industrie PV et il permet de déposer d'un seul côté du substrat et donc de s'affranchir d'une étape additionnelle de gravure de la couche de poly-Si sur la face opposée. Cependant, la voie PECVD implique une forte incorporation d'atomes d'hydrogène dans la couche de a-Si:H déposée, qui sont mobiles et tendent à former des cloques à l'interface entre la couche de a-Si:H et le c-Si. Ce phénomène de cloquage induit une dégradation de la couche de poly-Si à l'issue du recuit de cristallisation, qui s'accompagne d'une chute des propriétés de passivation de la jonction poly-Si/SiO_x [21,49].

Dans le cadre de la thèse, le problème de cloquage de la couche de a-Si:H a été résolu en deux temps :

- Dans un premier temps, la température de dépôt (T_{dep}) de la couche de a-Si:H a été augmentée afin de permettre l'exo diffusion des atomes d'hydrogène de la couche pendant le dépôt [127]. L'augmentation de T_{dep} de 220°C à 300°C (maximum de l'équipement) a permis la réduction de la taille des cloques après dépôt et après recuit (voir Figure 69, étape 1).
- Dans un deuxième temps, le ratio entre les gaz précurseurs, hydrogène et silane, R = H₂/SiH₄, a été augmenté de 6 à 65, ce qui a permis la diminution de la densité de cloques après dépôt et après recuit (voir Figure 69, étape 2). L'augmentation de R s'est accompagnée d'une division par quatre de la vitesse de dépôt, ce qui permettrait de libérer plus d'hydrogène de la couche pendant le dépôt et pourrait expliquer la réduction du phénomène de cloquage. Cependant, pour des ratios supérieurs à 50, une chute des propriétés de passivation a été observée, qui pourrait provenir de la détérioration de la couche de SiO_x due à l'importante concentration d'hydrogène dans le plasma [129].

Les paramètres de dépôt ont finalement été choisis tels que : T_{dep} = 300°C, $R = H_2/SiH_4 = 50$, afin de permettre une réduction du phénomène de cloquage tout en préservant les propriétés de passivation de la jonction poly-Si/SiO_x.

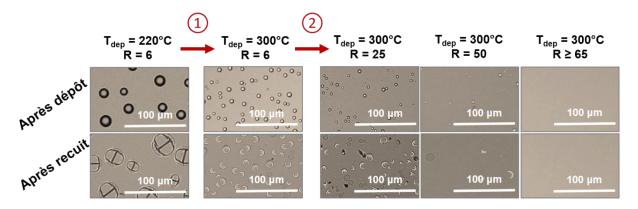


Figure 69. Images au microscope optique (grossissement x20) de couches a-Si:H(B) de 30 nm d'épaisseur et de couches de poly-Si(B) (respectivement après dépôt et après recuit à T_a = 700°C). Les conditions de dépôt ont été optimisées pour diminuer le cloquage de la couche : ① Augmentation de la température de dépôt T_{dep} , ② Augmentation du ratio de débit de gaz R = H_2/SiH_4 .

b. Evaluation des propriétés de passivation

Les propriétés de passivation de la jonction poly-Si/SiO_x ont ensuite été évaluées en fonction de la température de recuit (permettant la cristallisation de la couche amorphe en poly-Si). Pour ce faire, la jonction est fabriquée de chaque côté de substrats en c-Si de 156 mm². La durée de vie des porteurs minoritaires peut être mesurée en fonction de l'injection de porteurs excédentaires générés par un flash lumineux par mesure IC-PCD (Inductively-Coupled Photoconductance Decay). Cette mesure permet d'extraire des paramètres qui renseignent sur la qualité de la passivation de surface : la tension de circuit ouvert implicite iVoc et la densité de courant de recombinaison Jo. La Figure 70 représente les valeurs de iVoc et Jo extraites après recuit dans la gamme T_a = 700-850°C. On peut observer une augmentation de la qualité de la passivation de surface de 700°C à 800°C (augmentation de iVoc et diminution de J₀) suivie d'une dégradation pour T_a = 850°C. L'augmentation des propriétés de passivation pour T_a = 700-800°C pourrait provenir de l'amélioration de la qualité de l'interface (notamment la couche SiO_x [144]) couplée à la diffusion d'atomes de bore à l'extrême surface du substrat de c-Si (améliorant la passivation par effet de champ liée au fort dopage de la couche de poly-Si [81]). La dégradation de la passivation pour T_a > 800°C proviendrait quant à elle de la dégradation de l'homogénéité de la couche de SiO_x à l'interface (qui assure une passivation chimique de la surface du c-Si en saturant les liaisons pendantes) due à un budget thermique trop élevé [75,76,97].

L'ajout d'une étape d'hydrogénation de la jonction poly-Si/SiO_x est connue pour améliorer les propriétés de passivation de surface car elle permet la diffusion d'atomes H qui diffusent jusqu'à l'interface avec le c-Si et passivent les défauts résiduels [86]. Après hydrogénation par le biais d'un dépôt d'une couche de nitrure de silicium riche en H (SiN:H) suivi d'une étape de recuit rapide (firing), une amélioration des propriétés de passivation a en effet été observée.

Les propriétés de passivation de surface finalement obtenues sont au niveau de l'état de l'art de la passivation avec jonction poly-Si/SiO_x [13,14,16,52].

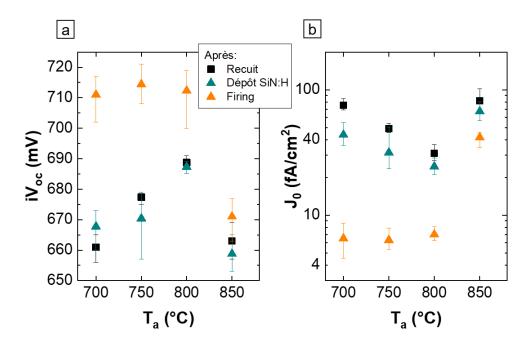


Figure 70. Propriétés de passivation de surface ((a) iV_{oc} et (b) J_0) fournies par la structure poly-Si(B)/SiO_x (avec poly-Si de 20 nm d'épaisseur) en fonction de la température de recuit T_a , évaluées sur des échantillons symétriques après recuit de cristallisation, dépôt de SiN:H et firing.

2. Poly-Si dopé ex-situ

a. Procédé de dopage ex-situ

Une deuxième voie de dopage ex-situ a été explorée afin de supprimer le B_2H_6 des gaz précurseurs et réduire l'apport en hydrogène pendant le dépôt de la couche. Dans les conditions de dépôt de la couche dopée in-situ, l'ajout de bore pendant le dépôt avait pour effet d'empêcher la cristallisation de la couche ce qui donnait lieu à un dépôt amorphe (a-Si:H(B)) [132]. La suppression de B_2H_6 des gaz précurseurs a mené au dépôt d'une couche intrinsèque microcristalline (μ c-Si(i)) [131] et a permis d'augmenter l'épaisseur maximale sans cloques jusqu'à 50 nm. Le dopage ex-situ de la couche de μ c-Si(i) a ensuite été réalisé grâce à une couche diélectrique riche en bore (SiON:B) précédemment développée au laboratoire [106]. Le procédé de dopage ex-situ de la couche de poly-Si est détaillé Figure 71.

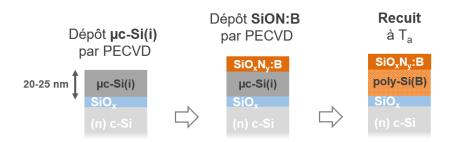


Figure 71. Procédé de dopage ex-situ de la jonction poly-Si/SiO_x.

b. Propriétés de passivation

Les propriétés de passivation de la jonction poly-Si/SiO_x dopée ex-situ ont été évaluées après recuit de cristallisation et après hydrogénation en fonction de la température de recuit T_a et ont été comparées aux propriétés obtenues avec la jonction de référence dopée in-situ (voir Figure 72). Une tendance similaire de iV_{oc} en fonction de T_a a pu être observée après recuit pour la jonction dopée ex-situ en comparaison de la jonction in-situ de référence. L'étape d'hydrogénation a également permis une amélioration de iV_{oc} jusqu'à une valeur maximale de 733 mV (associée à une valeur de J_0 de 6 fA.cm⁻²), résultat qui fait partie des meilleurs publiés dans la littérature.

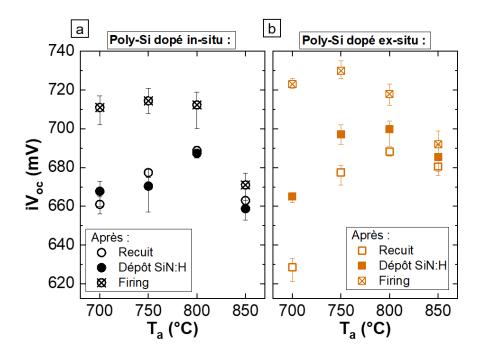


Figure 72. iV_{oc} évalué sur des échantillons symétriques avec jonctions poly-Si/SiO_x (a) dopées in-situ et (b) dopées ex-situ, en fonction de la température de recuit T_a après différentes étapes du procédé (recuit de cristallisation, dépôt de SiN:H et firing).

III. Caractérisation avancée de l'interface entre la jonction poly-Si et le substrat c-Si

Le deuxième axe de la thèse consistait à étudier les mécanismes de passivation et de transport des charges au niveau de la fine couche de SiO_x située à l'interface entre le poly-Si et le c-Si. Dans un premier temps, l'évolution de la couche de SiO_x pendant le recuit de cristallisation a été étudiée par le biais des techniques de spectroscopie photo-électronique par rayons X (XPS) et de microscopie électronique à transmission (TEM). Dans un deuxième temps, la méthode de microscopie à force atomique à pointe conductrice (C-AFM) a été appliquée à la jonction poly-Si/SiO_x afin d'étudier le mécanisme de transport des charges au travers de la couche de SiO_x. Enfin, les phénomènes de recombinaison des charges à l'interface SiO_x/c-Si ont été

caractérisés par des méthodes de spectroscopie de durée de vie, s'appuyant sur une évaluation de la durée de vie des porteurs près de la surface du c-Si.

1. Evolution de la couche de SiO_x pendant le recuit

L'évolution chimique et structurale de la couche de SiO_x pendant le recuit de cristallisation a été étudiée respectivement par XPS et TEM.

Des mesures par XPS en abrasion ont été réalisées sur des empilements a-Si:H(B)/SiOx/c-Si et poly-Si/SiO_x/c-Si, respectivement avant et après recuit dans la gamme T_a = 700-900°C. Il est à noter que de telles mesures en abrasion sur jonction poly-Si/SiO_x n'avaient jusqu'à présent jamais été rapportées dans la littérature. Les résultats ont montré la présence d'un oxyde en surface des couches a-Si:H(B) et poly-Si dont l'épaisseur augmentait et dont la stœchiométrie s'améliorait (vers une stœchiométrie SiO₂) avec l'augmentation de la température de recuit T_a. La mesure en abrasion a aussi permis d'étudier l'évolution de la couche de SiO_x à l'interface en fonction de T_a. Une épaisseur constante a été observée pour la couche de SiO_x après recuit à différentes valeurs de Ta. Les résultats semblent aussi indiquer une amélioration de la stœchiométrie de la couche de SiO_x avec l'augmentation de T_a. Cependant, le signal XPS obtenu à l'interface est moyenné sur une épaisseur de 5 nm (alors que la couche de SiOx a une épaisseur de 1,3 nm) et le canon d'abrasion à 1 keV utilisé pourrait induire une modification de la structure de l'échantillon. Ainsi, l'amélioration de la stœchiométrie de la couche de SiOx avec l'augmentation de Ta nécessiterait d'être confirmée à l'aide de mesures XPS à haute énergie et/ou à l'aide d'une technique d'abrasion plus douce (par exemple avec des molécules d'argon).

Des observations locales en TEM ont montré une dégradation de l'homogénéité en épaisseur de la couche de SiO_x à l'interface poly-Si/c-Si avec l'augmentation de T_a (voir Figure 73). Pour $T_a = 900^{\circ}$ C, la couche de SiO_x semblait même localement interrompue, laissant place à des interfaces directes entre le poly-Si et le c-Si.

La confrontation des résultats obtenus par XPS et par TEM a permis d'émettre une hypothèse sur l'évolution de la couche de SiO_x avec l'augmentation de T_a : les atomes d'oxygène diffuseraient à l'interface pour former des phases SiO_x plus riches en O (i.e. stœchiométrie plus proche de SiO_2) mais ce mécanisme de diffusion induirait des interfaces directes entre le poly-Si et le c-Si, ce qui pourrait expliquer la chute de passivation observée à haute température de recuit [75].

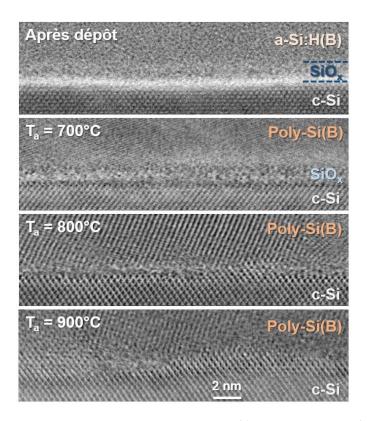


Figure 73. Images TEM autour de la couche de SiO_x d'échantillons a-Si:H(B)/SiO_x/c-Si et poly-Si(B)/SiO_x/c-Si, respectivement avant et après le recuit de cristallisation à T_a dans la gamme 700-900°C.

2. Etude du transport des charges par C-AFM

La technique C-AFM a été identifiée comme une technique intéressante pour l'étude des mécanismes de transport de charges à travers la couche de SiO_x [98,100]. Dans la littérature, il a été montré que les courants détectés par mesures de C-AFM de la jonction poly-Si augmentent lorsque la température de recuit augmente, ce qui pourrait être lié à la diminution de la résistance de la couche de SiO_x due à la formation d'ouvertures nanométriques (appelées « pinholes ») pendant le recuit de cristallisation [98]. De plus, en réalisant des mesures de C-AFM sur la jonction poly-Si/SiO_x, des points de plus fort courant peuvent être observés (voir Figure 74).

Dans cette étude l'impact de l'oxyde en surface de la couche de poly-Si (observé par XPS) sur les niveaux de courant mesurés par C-AFM a d'abord été étudié. Les résultats ont montré que l'oxyde surfacique atténuait les niveaux de courant détectés. Ainsi, un nettoyage chimique de la surface du poly-Si a été ajouté au protocole expérimental afin d'assurer un état de surface similaire pendant les mesures de C-AFM des différents échantillons étudiés. Ensuite, le lien entre les points de fort courant détectés par C-AFM et la présence de pinholes au sein de la couche de SiO_x a été étudié. Pour ce faire, des mesures de C-AFM ont été réalisées sur des jonctions poly-Si avec et sans couche de SiO_x à l'interface, et ce, pour différentes températures de recuit de cristallisation T_a (voir Figure 74). Des points de plus fort courant ont été détectés sur l'ensemble des cartographies en courant obtenues, ce qui indique que les points de fort courant ne reflètent pas la présence de pinholes au sein de la couche de SiO_x. De plus, des

mesures de C-AFM ont été réalisées en configuration latérale (c'est-à-dire avec la tension appliquée entre la pointe et un contact métallique à la surface du poly-Si) sur des échantillons similaires afin de permettre au courant de passer majoritairement dans la couche de poly-Si, sans passer à travers la couche de SiO_x. Ces mesures latérales ont aussi révélé la présence de points de plus fort courant, indiquant qu'ils pourraient être liés à des différences de conduction des charges au sein de la couche de poly-Si.

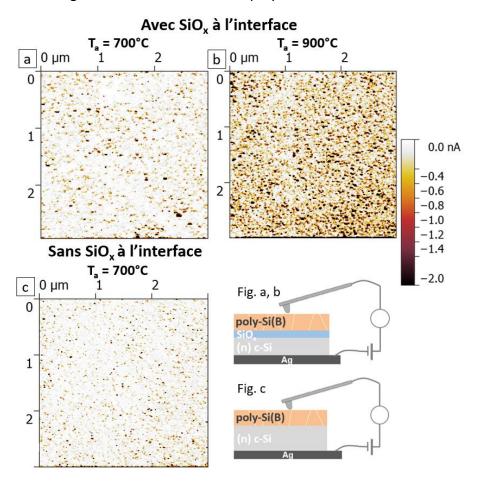


Figure 74. Cartographies en courant obtenues par C-AFM sur la jonction poly-Si/SiO $_x$ après recuit à T_a = (a) 700°C et (b) 900°C. La même mesure a été effectuée sur un échantillon sans couche de SiO $_x$ à l'interface (T_a = 700°C) (c). Les mesures C-AFM ont été effectuées 2h après nettoyage chimique de la surface des échantillons afin de garantir un état de surface similaire pendant la mesure.

3. Etude des phénomènes de recombinaison à l'interface

L'étude des phénomènes de recombinaison à l'interface SiO_x/c-Si s'est appuyée sur des méthodes de spectroscopie de durée de vie [117]. Ces méthodes permettent de caractériser des défauts électriquement actifs, elles ont notamment été appliquées à la caractérisation des défauts dans le volume du c-Si [118,119]. Elles reposent sur l'ajustement des courbes de durée de vie (mesurées par IC-PCD) par l'expression théorique de la durée de vie limitée par les défauts de type Shockley-Read-Hall (SRH). Les défauts électriquement actifs limitant la durée de vie peuvent ainsi être caractérisés par la détermination de leur niveau d'énergie dans la

bande interdite E_t et leur ratio de sections efficaces de capture : $k = \frac{\sigma_n}{\sigma_p}$ (où σ_n et σ_p sont les sections efficaces de capture respectives des électrons et des trous).

Dans cette étude, les méthodes de spectroscopie de durée de vie ont été appliquées à la surface du c-Si afin de caractériser les défauts localisés à l'interface SiO_x/c-Si (appelés « états de surfaces »). Cependant, l'application de ces méthodes en surface nécessite d'être en conditions de bandes plates près de la surface du c-Si. Afin de satisfaire au mieux cette condition, l'approche surfacique a donc été appliquée à une jonction poly-Si/SiO_x intrinsèque (c'est-à-dire non dopée).

Pour des échantillons aux surfaces suffisamment bien passivées, la mesure de durée de vie sur substrat de c-Si d'épaisseurs différentes permet l'extraction de la vitesse de recombinaison en surface du c-Si (S_{eff}), ce qui permet ensuite le calcul de la durée de vie limitée aux surfaces (τ_{surf}) [117]. Après recuit de cristallisation, la jonction poly-Si/SiO_x intrinsèque démontrait des niveaux de passivation de surface trop faibles pour permettre cette extraction. Cependant, après hydrogénation des échantillons, de meilleurs niveaux de passivation de surface ont été obtenus, ce qui a permis d'évaluer τ_{surf} à différentes températures de mesure dans la gamme 30-100°C. De telles courbes de τ_{surf} ont pu être décomposées comme la contribution de deux défauts apparents discrets notés D_1 et D_2 (associés à des niveaux d'énergie unique) [119]. La Figure 75a représente un exemple de cette décomposition pour une température de mesure de 30°C. Les courbes en température associées à chaque défaut apparent ont ensuite été ajustées par l'expression théorique SRH afin d'estimer leurs valeurs de E_t et k associées (voir Figure 75b). Des gammes de niveau de défaut $E_{t1} = [0.35\pm0.02 \text{ eV}\,; 0.62\pm0.02 \text{ eV}]$ et $E_{t2} = [0.35\pm0.02 \text{ eV}\,; 0.72\pm0.02 \text{ eV}]$ et des valeurs uniques de $k_1 = 53.4\pm20$ et $k_2 = 2.1\pm0.8$ ont pu être évaluées respectivement pour D_1 et D_2 .

Ainsi, une approche innovante de caractérisation des défauts recombinants à l'interface entre une jonction de poly-Si intrinsèque et le substrat de c-Si a été mise en œuvre. L'application étendue de cette approche aux jonctions de poly-Si/SiO_x fortement dopées (hors conditions de bandes plates) nécessiterait de développer le calcul de la concentration des porteurs en surface du c-Si par le biais de méthodes numériques [123].

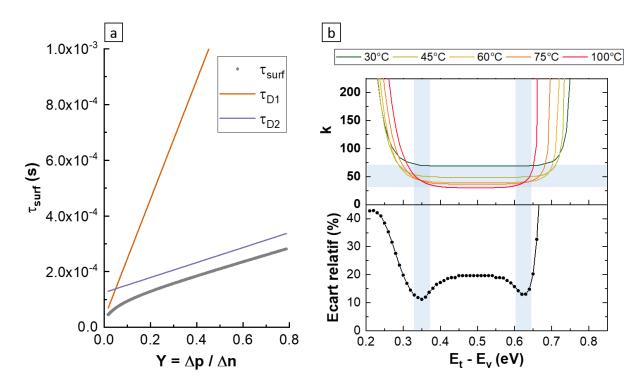


Figure 75. (a) Exemple de la décomposition de la composante de durée de vie limitée aux surfaces (τ_{surf}) en la contribution de deux défauts apparents (D_1 et D_2) pour une température de mesure de 30°C. (b) Diagramme de k-DPSS (en haut) et écart relatif entre les courbes calculées à différentes températures (en bas). Les minimas de l'écart relatif ont permis d'estimer une gamme de niveau de défaut E_{t1} = [0.35±0.02 ; 0.62±0.02] et une valeur unique de k_1 = 53.4±20 pour le défaut D_1 .

IV. Conclusions et perspectives

En conclusion, une jonction de poly-Si/SiO_x a été développée par la voie PECVD qui présente l'avantage de permettre la fabrication de la jonction sur une seule face du substrat de c-Si. Cependant, cette voie de dépôt induit une forte concentration d'hydrogène dans la couche déposée, ce qui entraîne la formation de cloques à l'interface avec le c-Si et tend à dégrader les propriétés de passivation de surface après recuit de cristallisation. L'optimisation des conditions de dépôt (température de dépôt et ratio de gaz H₂/SiH₄) a permis d'obtenir des jonctions poly-Si/SiO_x intègres. De plus, une méthode de dopage alternative, par le biais du dépôt d'une couche diélectrique riche en bore, a été développée, ce qui a permis de réduire l'apport en hydrogène pendant le dépôt et d'obtenir des couches de poly-Si intègres plus épaisses. L'ajout d'une étape d'hydrogénation a permis d'obtenir des propriétés de passivation de surface au niveau de l'état de l'art pour les deux types de jonctions poly-Si/SiO_x développées. Ces résultats sont prometteurs pour l'intégration de la jonction en face arrière de cellules solaires en c-Si. Des recherches sont en cours pour trouver une voie de métallisation de la jonction qui préserveraient ses propriétés de passivation tout en assurant un bon contact électrique [155].

Le deuxième axe de la thèse portait sur la caractérisation des mécanismes de recombinaison et de transport des charges au niveau de la couche SiO_x à l'interface entre le poly-Si et le c-Si.

L'étude de l'évolution chimique et structurale de la couche de SiO_x pendant le recuit a montré une possible amélioration de sa stœchiométrie vers SiO2 ainsi que la dégradation de son homogénéité en épaisseur à haute température, phénomènes qui pourraient s'expliquer par une diffusion des atomes d'oxygène à l'interface. L'étude du mécanisme de transport des charges au travers de la couche de SiO_x a été réalisée par C-AFM. Les résultats ont montré que la technique C-AFM ne permettait pas de conclure sur la présence ou non d'ouvertures localisées (pinholes) susceptibles d'assurer le transport des charges au travers de la couche de SiO_x. Cependant, des mesures de microscopie à force de sonde de Kelvin (KPFM) en cours dans le cadre d'une autre thèse ont permis de détecter des puits de potentiel en densités cohérentes avec celles attendues lors de la formation de pinholes dans la couche de SiO_x [76]. Enfin, une méthode de caractérisation des défauts recombinants à l'interface entre une jonction de poly-Si intrinsèque et le substrat de c-Si a été mise en œuvre. Cette méthode a permis de caractériser deux défauts discrets apparents à l'interface via leur niveau d'énergie dans la bande interdite et leur ratio de sections efficaces de capture des électrons et trous. L'application étendue de la méthode aux jonctions de poly-Si/SiO_x fortement dopées nécessiterait, quant à elle, le développement du calcul de la concentration des porteurs en surface du c-Si via des méthodes numériques.

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Titre : Intégration de jonctions poly-Si/SiO_x sur cellules solaires silicium – Optimisation et compréhension des propriétés de conduction et de passivation de surface

Mots clés: Silicium, Cellules solaires, Contacts passivés, Poly-Si

Résumé: Dans le contexte des cellules photovoltaïques (PV) à base de silicium cristallin (c-Si), le développement de structures de contacts dits « passivants », qui permettent de limiter les pertes par recombinaisons des porteurs de charge à l'interface entre le métal et le c-Si, est un des principaux leviers vers l'obtention de plus hauts rendements. Une approche de contacts passivés consiste à intégrer entre le métal et le c-Si une jonction composée d'une couche de silicium poly-cristallin (poly-Si) fortement dopée sur une mince couche d'oxyde de silicium (SiO_x \leq 2 nm). Les objectifs de ce travail sont d'une part de développer une jonction poly-Si/SiO_x compatible avec la fabrication industrielle des cellules PV, et d'autre d'améliorer la compréhension des mécanismes de passivation et de transport des charges au niveau de la fine couche de SiOx située à l'interface entre le poly-Si et le c-Si.

Dans ce travail, une jonction de poly-Si/SiO_x dopée au bore a été développée, le dopage de la couche étant dans un premier temps réalisé insitu pendant l'étape de dépôt chimique en phase vapeur assisté par plasma (PECVD) de la couche poly-Si. La méthode de dépôt PECVD est répandue dans l'industrie PV et permet la fabrication de la couche poly-Si d'un seul côté du substrat c-Si. Cependant, elle induit une forte concentration d'hydrogène dans la couche déposée, ce qui entraine la formation de cloques à l'interface avec le c-Si et tend à dégrader les propriétés de passivation de surface de la cristallisation. jonction après recuit de L'optimisation des conditions (température de dépôt et ratio de gaz H₂/SiH₄) a

permis d'obtenir des couches de poly-Si dopées in-situ intègres.

Par la suite, une méthode de dopage alternative, par le biais du dépôt d'une couche diélectrique riche en bore sur le poly-Si, a été appliquée afin de réduire l'apport en hydrogène pendant le dépôt et d'obtenir des couches de poly-Si intègres plus épaisses. L'ajout d'une étape d'hydrogénation a permis d'obtenir des propriétés de passivation de surface au niveau de l'état de l'art pour les deux types de jonctions poly-Si/SiO_x développées.

A la suite du développement de la jonction poly-Si/SiO_x, la caractérisation physico-chimique de la couche SiO_x a été réalisée et a démontré une possible amélioration de la stœchiométrie de la couche vers SiO₂ ainsi qu'une dégradation de son homogénéité en épaisseur sous l'effet du recuit de cristallisation à haute température. Ces phénomènes pourraient s'expliquer par une diffusion des atomes d'oxygène à l'interface. D'autre part, l'étude du transport des charges à travers le SiO_x par C-AFM a mis en évidence les limites de cette technique quant à la détermination de nano-ouvertures au sein de la couche SiO_x (qui favoriseraient le transport des charges). Enfin, une méthode de caractérisation des défauts recombinants à l'interface entre une jonction de poly-Si intrinsèque et le c-Si a été mise en œuvre. Cette méthode a permis de modéliser les recombinaisons à l'interface poly-Si/c-Si via deux défauts discrets apparents dont les niveaux d'énergie dans la bande interdite et les ratios de sections efficaces de capture des électrons et des trous ont été déterminés.





Title : Integration of poly-Si/SiO_x contacts in silicon solar cells – Optimization and understanding of conduction and passivation properties

Keywords: Silicon, Solar cells, Passivated contacts, Poly-Si

Abstract: In the context of high efficiency solar cells (SCs) based on crystalline silicon (c-Si), the development of "passivating" contact structures to limit the recombination of charge carriers at the interface between the metal electrode and the c-Si has been identified as the next step to further improve the photovoltaic conversion efficiency. Passivating contacts consisting of a highly doped polycrystalline silicon layer (poly-Si) on top of a thin layer of silicon oxide (SiO_x \leq 2 nm) are particularly sparking interest as they already demonstrated promising conversion efficiency when integrated in SCs.

The objectives of this work are to develop a poly-Si/SiO_x passivating contact compatible with the industrial production of c-Si SCs, and to investigate the passivation and charge transport mechanisms in the region of the thin SiO_x layer located at the interface between the poly-Si and the c-Si.

In this work, a boron-doped poly-Si/SiO_x contact was fabricated. The doping of the layer was first performed in-situ during the deposition of a hydrogen-rich amorphous silicon (a-Si:H) layer by plasma-enhanced chemical vapor deposition (PECVD). The PECVD step was followed by an annealing step for crystallization of the poly-Si layer. The PECVD presents the advantages of being widespread in the PV industry and enabling the fabrication of the poly-Si contact on a single side of the c-Si substrate. However, it induces a high concentration of hydrogen in the deposited layer, which causes the formation of blisters at the interface with the c-Si and tends to degrade the surface passivation properties of the contact annealing for crystallization. optimization of the deposition conditions (temperature and H₂/SiH₄ gas ratio)

enabled to obtain blister-free in-situ doped poly-Si layers. An alternative doping method consisting in the deposition of a boron-rich dielectric layer on top of the poly-Si layer was also considered to reduce the hydrogen content of the deposited layer. The diffusion of hydrogen in the contact after annealing is known to provide a further chemical passivation of the poly-Si/c-Si interface. In this work, the addition of a hydrogenation step through the deposition of a top H-rich silicon nitride (SiN:H) layer enabled to obtain state-of-the-art surface passivation properties for the two types of poly-Si/SiO_x contact fabricated.

After developing the poly-Si/SiO_x contact, a study of the effect of the annealing step on the chemical and structural properties of the SiO_x layer was performed. Results indicated a possible improvement of the stoichiometry of the SiO_x layer towards SiO₂ as well as a degradation of its homogeneity at the poly-Si/c-Si interface after annealing at high temperature. These phenomena could be explained by a lateral diffusion of the oxygen atoms at the interface. The transport mechanism of charge carriers through the SiO_x layer was conducted by C-AFM. This study revealed the limits of this technique to determine the presence of pinholes (that would help the transport of charge carriers) within the SiO_x layer. Finally, a method for characterizing recombinant defects at the interface between an intrinsic poly-Si contact and the c-Si has been developed. This method enabled to model the recombination phenomena at the poly-Si/c-Si interface via two apparent discrete defects. Their associated energy levels in the bandgap and ratios of electron and hole capture cross sections were estimated.

