Low-power and radiation resilient approaches for spectrum sensing

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Abstract

The advancement of technology has enabled a great increase in the number of users and the amount of information to be transmitted. In recent years, the demand for high download rates, massive connection, low latencies, and energy efficiency has increased, mainly due the popularization of IoT devices and the introduction of industry 4.0. This has led to a significant increase in demand for the frequency spectrum to accommodate new services or to improve existing ones.

One of the alternatives to deal with this problem is the use of cognitive radios (CRs). They are able to sense the spectrum and see which bands are not currently being used. Among the various challenges related to CR, spectrum sensing is one of the most important and one of the primary functions of these radios.

Wideband spectrum sensing presents several challenges, including antennas and processing a lot of data. However, in several moments the spectrum can be considered sparse allowing the use of compressive sensing (CS) in order to reduce the amount of samples required and thereby reducing processing resources.

In terms of hardware, the use of CS can be translated in analog-to-information converters (AICs) instead of implementing analog-to-digital converters (ADCs) with high sampling rates. Furthermore, it is interesting to implement low-power devices. Downscaling transistors to nanometers helps to reduce consumption and area. However, other alternatives have been studied to decrease the leakage power. Among these alternatives, Magnetic Tunnel Junction (MTJ) has been very promising. In addition, the downscaling transistors makes circuits more sensitive to single event transient (SET), and although MTJ is more robust than transistors to radiation, it is necessary to study how this impact is and how to reduce it.

In this context, this thesis focuses on the SET effects analysis and MTJ applications which can be used in an AIC to perform the wideband spectrum sensing. The main contributions of this thesis are the analysis of SET effects in a comparator which is one of the main components of an ADC, analysis of SET effects in MTJ structures, and the proposition of an MTJ-based ADC which can be used in an AIC to perform the wideband spectrum sensing.

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List of Acronyms

ADC Analog-to-Digital Converter.

AIC Analog-to-Information Converter.

AIQ Adaptive Intermittent Quantizer.

AP Anti-Parallel state.

AQR Adaptive Quantization Rate.

AWGN Additive White Gaussian Noise.

BL Bit Line.

BOX Buried OXide.

BP Basis Pursuit.

BPF Bandpass Filter.

CAF Cyclic Autocorrelation Function.

CMOS Complementary Metal Oxide Semiconductor.

CP Cyclic Prefix.

CPU Central Processing Unit.

CR Cognitive Radio.

CS Compressive Sensing.

CSD Cyclic Spectrum Density.

DAC Digital to Analog Converter.

DC Direct Current.

DIBL Drain Induced Barrier Lowering.

DNL Differential Nonlinearity.

DRAM Dynamic Random-Access Memory.

DSP Digital Signal Processor.

ECG Electrocardiogram.

ENOB Effective Number of Bits.

FA Full Adder.

FCC Federal Communications Commission.

FDSOI Fully Depleted Silicon-On-Insulator.

FF Flip-Flop.

FFT Fast Fourier Transform.

FPGA Field Programmable Gate Array.

GMR Giant Magnetoresistance.

HM Heavy Metal.

IEEE Institute of Electrical and Electronic Engineers.

INL Integral Nonlinearity.

IoT Internet of Things.

IRLS Iterative Reweighted Least Squares.

LAN Local Area Network.

LET Linear Energy Transfer.

LFSR Linear Feedback Shift Register.

LLG Landau-Lifshitz-Gilbert.

LO Local Oscillator.

LTE Long-Term Evolution.

LUT Lookup Table.

LVT Low Threshold Voltage.

MC Multi-coset Sampling.

MeRAM Magnetoelectric Random Access Memory.

MOS Metal–Oxide–Silicon.

MP Matching Pursuit.

MRAM Magnetic Random Access Memory.

MRS Multirate Sampling.

MTJ Magnetic Tunnel Junction.

MUSIC Multiple Signal Classification.

MWC Modulated Wideband Converter.

NMOS N-type Metal-Oxide-Semiconductor.

NSS Narrowband Spectrum Sensing.

NUS Non-Uniform Sampling.

NVM Non-Volatile Memory.

OFDM Orthogonal Frequency-Division Multiplexing.

OMP Orthogonal Matching Pursuit.

P Parallel state.

PMA Perpendicular Magnetic Anisotropy.

PMOS P-type Metal-Oxide-Semiconductor.

PSD Power Spectral Density (PSD).

PU Primary User.

PV Process Variation.

QoS Quality of Service.

QR Quantization Resolution.

RD Random Demodulation.

RF Radio Frequency.

RL Read Line.

RMPI Random-Modulation Preintegrator.

RVT Regular Voltage Threshold.

S&H Sample-and-Hold.

SAR Successive-Approximation-Register.

SET Single Event Transient.

SFDR Spurious Free Dynamic Range.

SHE Spin Hall Effect.

SHM Spin Hall Metal.

SINAD Signal-to-Noise-and-Distortion Ratio.

SL Source Line.

SNN Spiking Neural Network.

SNR Signal-to-Noise Ratio.

SoC System On Chip.

SOT Spin–Orbit Torque.

SR Sampling Rate.

SRAM Static Random-Access Memory.

SS Spectrum Sensing.

STI Shallow Trench Isolation.

STT Spin Transfer Torque.

SU Secondary User.

TCAD Technology Computer-Aided Design.

THD Total Harmonic Distortion.

TMR Tunnel Magnetoresistance.

VCMA Voltage-Controlled Magnetic Anisotropy.

VCSO Voltage-Controlled Stochastic Oscillator.

WiMAX Worldwide Interoperability for Microwave Access.

WL Word-Line.

WRAN Wireless Regional Area Network.

WSS Wideband Spectrum Sensing.

Chapter 1

Introduction

This chapter addresses the motivation, objectives, and contributions of the present work.

1.1 Motivations

Methods for storing coded information have been present throughout the entire history of humankind. Drawings first appeared in the caves followed by the use of hieroglyphics in Ancient Egypt. Then, with the invention of the printing press, books dominated the storage of information for centuries. Only in the 20th century did the floppy disk, hard disk, and optical disk revolutionize the way we store data.

Likewise, the broadcast, or transmission, of coded information has a long history. Egyptians and Greeks used a type of correspondence as a starting point to transmit information such as couriers with messengers or birds. Other long distance transmission methods include drums, smoke signals or flags. However, these methods had their limitations as they depended on the human sense of sight or hearing which were required for their detection.

The revolution of information transmission began at the end of 18th century with the beginning of electricity. Only one century later, in the last decade of the 19th century, Marconi developed the first practical radio transmitters and receivers.

Over the last few decades, frequencies considered allocable for international organizations have increased. Nowadays, a vast set of services and radio technologies have drowned the spectrum for example local wireless networks, IoT, and smart city devices (see Fig. 1.1). Since 2011, the planet has more interconnected devices than the number of people [1]. In 2020, there are more than 3.5 billion smartphone users in the world [2]. The increase in the number of devices has also

resulted in the increase of data that needs to be captured, processed, stored, and communicated. Moreover, the demand in terms of download speed, small latencies, and power efficiency have been increasing in recent years.

Figure 1.1 – Wireless equipments.

In wireless communication systems, the spectrum is one of the most valuable resources as it is a finite resource. The frequency bands used by the communication systems nowadays are usually overloaded [3, 4]. The license models usually use a static way to divide the spectrum. This results in an inefficient usage of the spectrum (see Fig. 1.2 from [5]). This static way to allocate the spectrum limits data transmission capacity and the number of users. Moreover, with the increasing number of higher data rate devices, it is difficult to accommodate all the requirements with static frequency allocation schemes. Therefore, new strategies to efficiently exploit the available spectrum and overcome the spectrum scarcity have captured scientists' interest, and thus increased research and development, over the last decades.

Cognitive Radio (CR) is viewed as an approach for improving the utilization of the radio spectrum. The concept of CR was firstly proposed by J. Mitola in [6]. Cognitive radio is a device capable of learning and adapting to the electromagnetic environment in which it operates, being able to adjust its operational parameters autonomously and dynamically, to maximize data flow, mitigate interference, facilitate interoperability, and opportunistically explore frequency bands without use or underutilized.

Normally, some parts of the spectrum, which were previously allocated for some users, are not being used on a full-time basis. The key feature of CR is its ability to recognize the communication environment and independently adapt the parameters of their communication scheme to maximize the quality of service (QoS), for the secondary (unlicensed) users (SU), while minimizing the

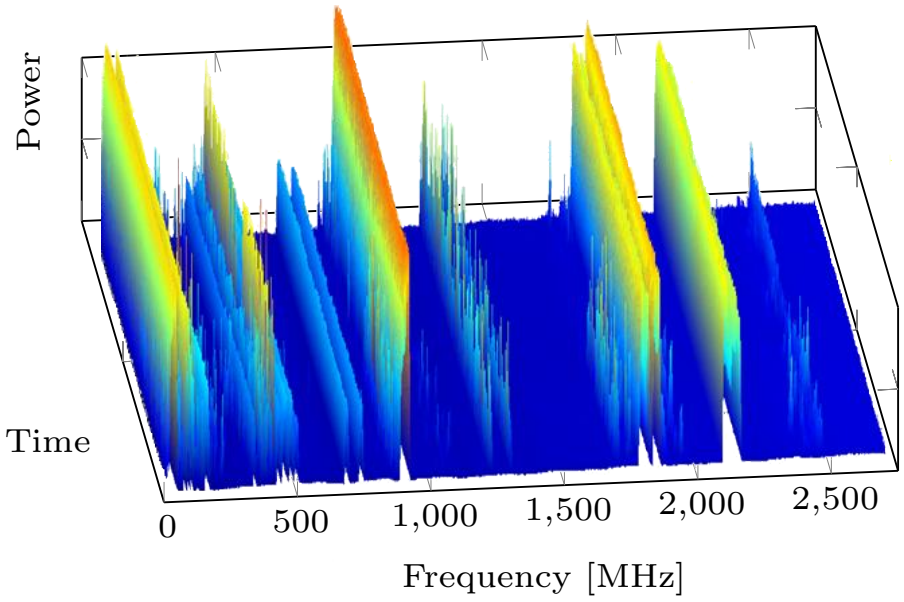


Figure 1.2 – Example of spectrum occupancy: received power versus the frequency for 24 hours.

interference to the primary users (PU) and the total power consumption opportunistically exploring frequency bands without use or underutilized. Therefore, using radio transceivers with cognitive abilities, it is possible to exploit unused spectrum to provide a better spectrum access due to spectrum opportunities.

The spectrum opportunity can be defined as "a band of frequencies that are not being used by the primary user of that band at a particular time in a particular geographic area" [7]. Hence, to efficiently use any available opportunity, a CR can interact with the environment, sensing and measuring the spectrum. It can make decisions to adapt its transmitter or receiver parameters to the environment allowing secondary users to occupy some of the spectrum available (see Fig. 1.3). In order to do this, an accurate estimation of spectrum utilization and assessment of potential vacant spectrum holes have to be done.

One of the main challenges of the efficient design of CR networks include spectrum sensing (SS). Based on the size of the band of interest, spectrum sensing techniques are divided to narrowband sensing and wideband sensing. While narrowband spectrum sensing (NSS) only considers a part of the band, in which it is assumed to be used by a signal, to be sensed; the wideband spectrum sensing (WSS) observes a wideband in order to identify the parts of such bands which are occupied or free. The spectrum sensing has three main practical challenges: robust sensing algorithms, blind detectors, and wideband spectrum sensing [8].

This thesis focuses on wideband spectrum sensing. According to the Nyquist–Shannon sam-

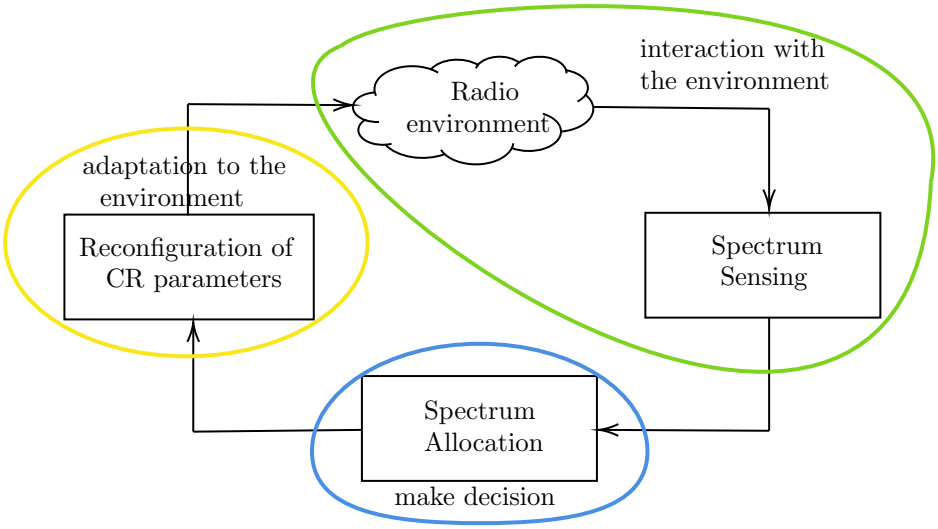


Figure 1.3 – Cognitive radio cycle.

pling theorem, a signal can be perfectly reconstructed from its samples if it is sampled by the Nyquist rate, that is, a rate equal to twice the bandwidth of the signal [9]. Wideband spectrum sensing techniques can be categorized in Nyquist wideband sensing and sub-Nyquist wideband sensing. They will be cover in the next chapters. The sub-Nyquist approaches aims to reduce the hardware cost and the computational complexity compared to the high sampling rate implementations. Moreover, it allows signal conversions of very high rates where state-of-the-art implementations in Analog-to-Digital Converters (ADC) do not allow Nyquist rate sampling directly.

The classic ADC approach is based on the Nyquist-Shannon criterion. Therefore, the use of ADC may require high sampling rates and many samples to be treated. It may not be adequate for low-power or lattency-critical applications. One of the main challenges related to CR is the development of wideband spectrum sensing without depending on the implementation of high sampling rate ADCs, decreasing processing, and hardware consumption. An alternative is the utilization of input signal features to decrease the time, hardware, and energy resources required. It can be done through the implementation of an Analog to Information Converters (AIC) based on the Compressive Sensing theory (CS) to replace the classic ADC reducing the hardware cost. Compressive Sensing uses the sparse representation of a signal in a given domain to perform its estimation more efficiently.

Starting with the study of spectrum sensing techniques and analog to information converts, this thesis aims at contributing to the development of approaches in hardware for spectrum sensing in

order to improve cognitive radio networks capabilities, including reliability analysis against radiations based on single event transient (SET). Fig. 1.4 summarizes the principal topics addressed here.

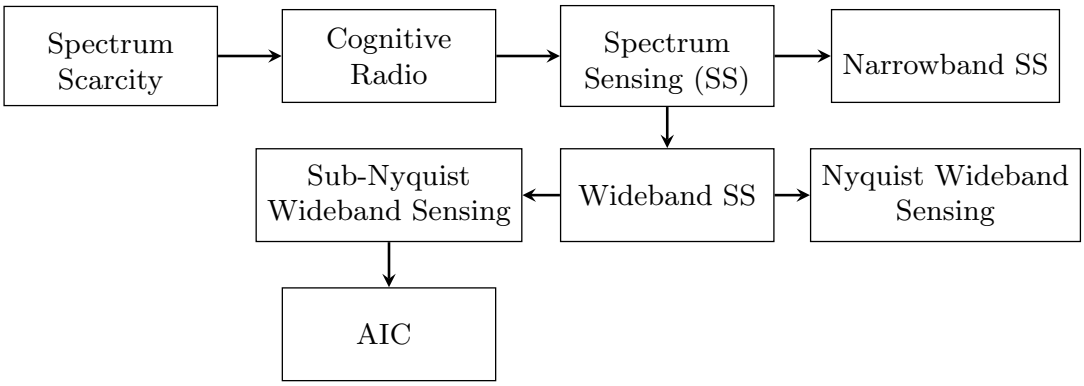


Figure 1.4 – Principal topics related to this thesis.

1.2 Thesis Contributions

This thesis is focused on hardware approaches for spectrum sensing. The main contributions are as follow:

- Review of MTJ applications (see Section 4.4).
- Analysis of SET effects on a comparator using FDSOI technology (see Section 5.1).
- Investigation of SET effects on a VCMA-MTJ-based bit-cell (see Section 5.2).
- Reliability analysis of NAND-Like spintronic structure (see Section 5.3).
- Proposition of an MTJ-based ADC (see Section 5.4).
- Analysis of wideband spectrum sensing using an AIC (see Section 5.5).

1.3 Organization of the Thesis

This report is organized into the following chapters:

Chapter 2 - Cognitive Radio and Spectrum Sensing: Chapter 2 introduces the background of this thesis. Firstly, Cognitive Radio is addressed followed by the techniques of spectrum sensing. They are classified in narrowband and wideband spectrum sensing.

Chapter 3 - Spectrum Sensing based on Compressive Sensing: This thesis focuses on wideband spectrum sensing. Among the techniques leading to wideband spectrum sensing, this work deals with spectrum sensing based on compressive sensing. Chapter 3 reviews some key concepts on compressive sensing. Analog-to-information converters and analog-to-digital converts are also discussed.

Chapter 4 - Hardware Challenges: Chapter 4 focuses on the challenges associated to hardware device implementations. Concerns about device area and power are also addressed along with alternatives to deal with these issues. Moreover, this chapter provides information on FDSOI technology and MTJ along with MTJ applications.

Chapter 5 - Hardware Analysis and Propositions: This chapter presents the main contributions of this thesis. Firstly, the SET effects on an FDSOI comparator and on two different structures involving MTJ and its writing methods are analyzed. Then, an MTJ-based ADC is proposed. Finally, wideband spectrum sensing using an AIC is presented and discussed.

Chapter 6 - Conclusion and Perspectives: The last chapter concludes the work accomplished during this thesis and presents some perspectives of future research directions.

Chapter 2

Cognitive Radio and Spectrum Sensing

This chapter introduces some concepts related to the thesis subject. Firstly, some characteristics of cognitive radio are addressed. Then, spectrum sensing techniques are discussed. In the cognitive radio domain, spectrum sensing involves obtaining the spectrum usage characteristics considering the space, time, frequency, and type of signals which are occupying the spectrum (bandwidth, modulation, carrier frequency, etc.) [10]. Spectrum sensing can be divided into: narrowband spectrum sensing and wideband spectrum sensing.

2.1 Cognitive Radio (CR)

The electromagnetic spectrum is a limited resource. The licensing of frequency bands is done by the competent authorities for different activities and technologies. Although the spectrum is mostly reserved, only a small fraction of these frequencies are being used for communication over large geographic areas or for significant time intervals. Therefore, there are parts of the spectrum that are used inefficiently, with overused bands suffering from excessive traffic and users while there are bands with low or zero usage that could improve the quality and capacity of services for which the frequencies allocated are insufficient. In addition, the growing volume of data accessed from mobile devices suggests a bottleneck in the capacity of current networks in the near future.

The use of cognitive radio (CR) can contribute to mitigate spectrum scarcity through a more efficient use of the spectrum. The first definition of a CR was made by Mitola [6]. The FCC defines a CR as: “a radio or system that senses its operational electromagnetic environment and can dynamically and autonomously adjust its radio operating parameters to modify system operation, such as to maximize throughput, mitigate interference, facilitate interoperability, and access sec-

ondary markets." [11]. The spectrum is allocated to licensed users, called, in this context, primary users (PUs). They have the priority to use the spectrum. On the other hand, the unlicensed users, known as secondary users (SUs), have lower priority. Besides being an alternative approach solving the under-utilization of the spectrum, the CR can also be a solution for the devices which need to use the spectrum intelligently, for example finding an opportunity in the spectrum that improves its communication performance.

The main changes from a cognitive radio to conventional radios are in the physical and link layers, which implement the capacity for spectrum monitoring and how the access to the medium is performed. A CR can adjust its transmission depending on other existing transmissions and available frequency spectrum. Therefore, selected frequencies could be used without causing interference and improve the efficiency of wireless communication systems. Fig. 2.1 illustrates the cognitive radio concept, where the blocks are spectrum occupied by primary users. Spectrum holes are areas available to secondary users that do not have a frequency defined by the standard.

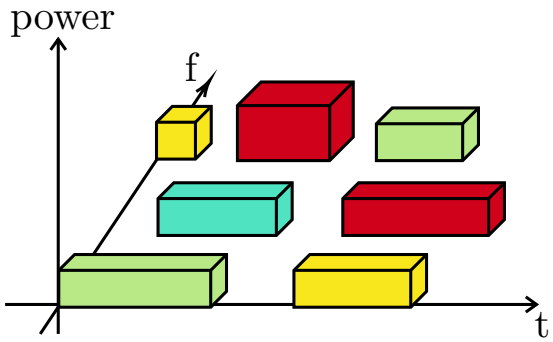


Figure 2.1 – Cognitive radio concept.

Basically, CR improves the spectrum usage, by changing from the static spectrum allocation into the dynamic spectrum allocation. CR allows for the increase in the number of users without the need for more telecommunications infrastructure. Its use has already been standardized in IEEE 802.21, IEEE 802.22 WRAN [12], IEEE 802.11af for wireless LANs, IEEE 802.11k [13], IEEE 802.16h-Cognitive WiMAX, IEEE 802.22 [14], Bluetooth [15], and LTE [16, 17].

Fig. 2.2 illustrates the key functions of CR networks [18]:

- Spectrum sensing: this is the most important cognitive task. It aims at determining which parts of the spectrum are available. It is performed across different dimensions such as time, frequency, angle, geographical area, code, and signal (see Fig. 2.3). Considering all these dimensions, more opportunities can be found to be used by a SU. The spectrum sensing can

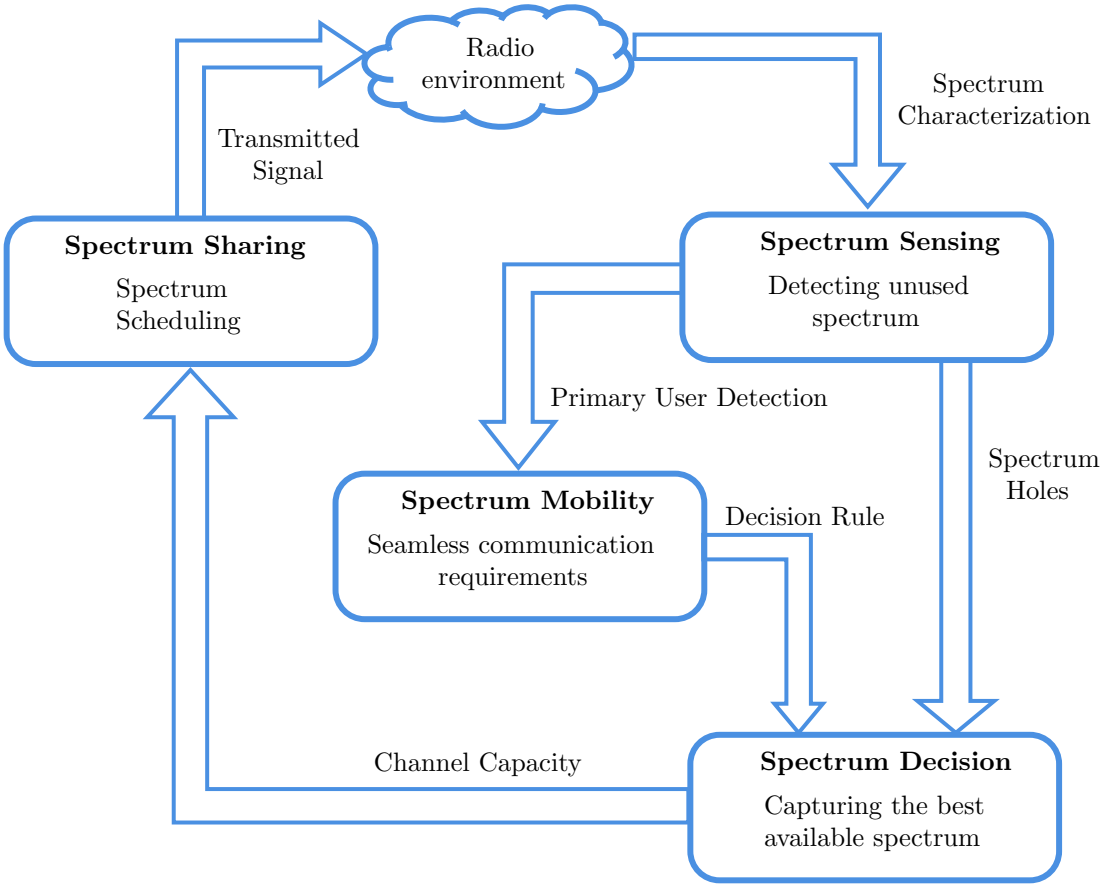


Figure 2.2 – Key functions of cognitive radio.

be also done in a collaborative way where various SUs sense the spectrum and share their information. It can decrease the sensing time [19]. Collaborative spectrum sensing can be centralized or distributed.

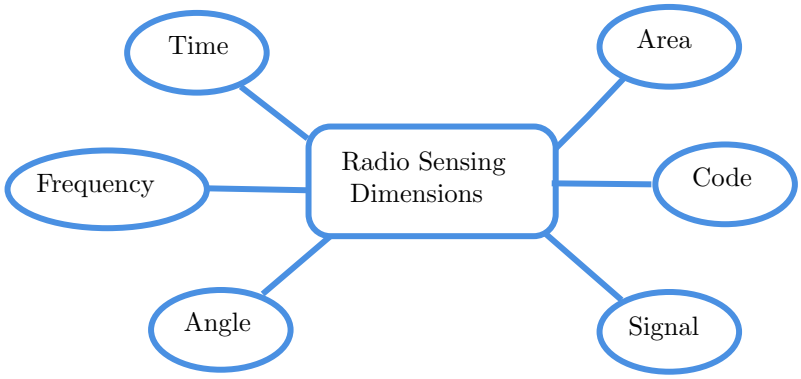


Figure 2.3 – Radio sensing dimensions.

- Spectrum management and decision: after locating the available spectrum bands, the CR should select the best one considering bandwidth, transmit power, coding schemes, mod-

ulation schemes, and QoS. Machine learning techniques can be used to make decisions in order to adapt and develop strategies to maximize certain performance measures [6, 20–22].

- Spectrum mobility: this involves the capacity of CRs that seamlessly hop among different spectrum holes while relying on the conditions. For example, the SUs have to move to another spectrum hole when the current spectrum band is required by a PU because of the priority of the spectrum access for this licensed user.

- Spectrum sharing: in order to avoid collisions between users, access to the spectrum must to be coordinated. In this case, the spectrum holes have to be divided among different CR devices and PUs. It may be performed in code, space dimensions, frequency, and time. Using the interweave strategy, the SU uses the spectrum only when the PU is idle. On the other hand, SU and PU use the spectrum together with the underlay and overlay spectrum sharing [23]. In the underlay approach, the SU transmits with transmission power constraint while the overlay technique uses the unoccupied fractions of the spectrum [24].

This thesis focuses on spectrum sensing. Spectrum sensing techniques are classified according to the size of the band of interest in narrowband spectrum sensing and wideband spectrum sensing (see Fig. 2.4). The first one aims at deciding if the analysed part of the spectrum is occupied or not. On the other hand, the wideband spectrum sensing aims to find which parts of the spectrum are vacant. The following sections provide a brief review of the most commonly used techniques.

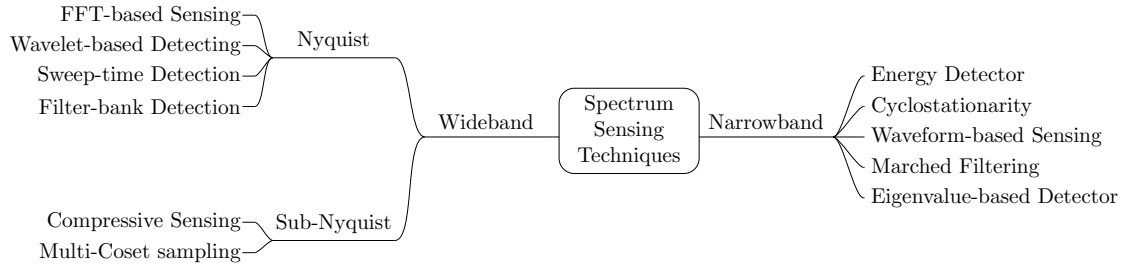


Figure 2.4 – Spectrum sensing techniques.

2.2 Narrowband Spectrum Sensing

A narrowband spectrum sensing method exploits spectral opportunities over a narrow frequency range. Its aim is to identify if the range is occupied by a PU or not. It can be represented by binary hypotheses tests where H_0 represents the vacancy and H_1 denotes the presence of a PU:

$$x(t) = \begin{cases} w(t) & H_0 \\ p(t) + w(t) & H_1 \end{cases} \tag{2.1}$$

where $x(t)$ is the received signal at the CR at the t^{th} sampling instance, $w(t)$ is the Additive White Gaussian Noise (AWGN), and $p(t)$ is the PU's signal.

The most common narrowband spectrum sensing techniques are illustrated in Fig. 2.4 and discussed below [4, 25].

2.2.1 Energy Detector

Energy Detector is the most popular narrowband spectrum sensing technique [26–40]. In order to determine if the PU signal is present, the square of the received signal $x(t)$ is calculated and averaged over a period of time, aiming at obtaining more reliable decision statistics. The energy detector's output is compared to a specific energy threshold which depends on the noise floor (see Fig. 2.5). Therefore, energy detector does not require previous information about the PU signal to perform sensing.

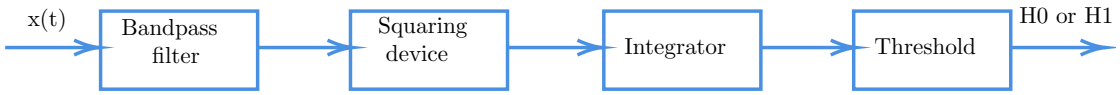


Figure 2.5 – Energy Detector.

Considering Eq. (2.1), the energy detector's decision metric can be calculated as:

$$M = \sum_{t=0}^{N} |x(t)|^2 \tag{2.2}$$

where N is the observation vector's size. Therefore, M is compared to a fixed threshold λ_E in order to determine if the spectrum is occupied by the PU. A large probability of detection P_D (see Eq. (2.3)), that is, the probability of detecting a signal when it's truly present, is desired.

$$P_D = Pr(M > \lambda_E | H_1) \tag{2.3}$$

On the other hand the probability of a false alarm P_F, that is, the detector determines that the PU occupies the spectrum but it is not true, can be calculated as:

$$P_F = Pr(M > \lambda_E | H_0) \tag{2.4}$$

Since the threshold depends on the noise variance, significant performance loss can be caused by a small noise power estimation error. To overcome this problem, the multiple signal classification (MUSIC) algorithm dynamically estimates the noise level by separating the signal and noise subspaces [41].

The noise uncertainty degrades the performance of the energy detector [42, 43]. To overcome this problem, the noise level can be cooperatively estimated reducing the uncertainty to its minimal level [44]. Several works analyse the energy detector performance in different scenarios: fading conditions [45], $k\mu$ extreme fading [46], Hyper-Rayleigh fading [39], and cascaded Rayleigh fading [38] for example.

The main advantages of this technique is its implementation and computational simplicity [47]. However, it faces some challenges such as the selection of the energy threshold, performance degradation at a low signal to noise ratio, difficulty in sensing spread spectrum PUs, and incapacity to distinguish PU interference from noise.

2.2.2 Cyclostationarity - Spectral Correlation

This technique exploits the signal cyclostationary features which are intentionally introduced or are generated by the periodicity in the signal or in its statistics such as autocorrelation and mean (see Fig. 2.6) [47–57]. Since the noise is wide-sense stationary with no correlation and modulated signals are cyclostationary with spectral correlation, this technique can differentiate PU's signal from noise. In order to do this, it analyses the Cyclic Autocorrelation Function (CAF) of the received signal. The CAF of the received signal $x(t)$ can be expressed as [58]:

$$R_x^{\beta}(\tau) = E[x(t)x^*(t-\tau)e^{-j2\pi\beta t}] \tag{2.5}$$

where β is the cyclic frequency, τ is the lag value, $E[.]$ is the expectation operator, and $(.)^*$ is the complex conjugation.

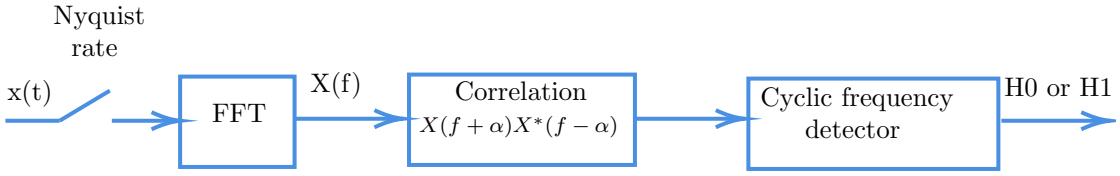


Figure 2.6 – Cyclostationarity.

The CAF can also be represented by the Cyclic Spectrum Density (CSD) function using the

Fourier series expansion:

$$S(f,\beta) = \sum_{\tau=-\infty}^{\infty} R_x^{\beta}(\tau) e^{-j2\pi ft} \tag{2.6}$$

This function has peaks when the cyclic frequency β is equal to the PU fundamental frequency. When there is no PU, the CSD does not have a peak because the noise is non-cyclostationary.

One advantage of this technique is that the cyclostationary detector can distinguish between the noise and the PU even at a very low SNR. However, this technique requires calculating all cycle frequencies thus increasing its computational complexity. In [52], the authors also propose the use of the cyclostationary detection to wideband spectrum sensing. Some works aims at reducing the implementation complexity of the cyclostationary detectors [51, 54].

2.2.3 Waveform-based Sensing

Also known as coherent sensing, it exploits the patterns sent with the PU signal, for example, pilot patterns, preamble, and spreading sequences [59–61]. They are purposefully added to the signal for synchronization and detection. Therefore, this technique correlates the received signal with these known patterns and compares the correlator's output with a specific threshold. One constraint of this method is its susceptibility to synchronization errors. Moreover, longer signal patterns are required in order to improve sensing performance, which decreases the spectrum efficiency.

2.2.4 Matched Filtering

It is considered the optimal spectrum sensing technique when the PU signal information (bandwith, frequency, modulation, and pulse shaping) is known by the SU [34, 62–64]. This technique requires the perfect knowledge of the PU signaling features such as operating frequency, bandwidth, modulation type, frame format, and pulse shaping. It correlates the received signal with a known primary signal and compared to a threshold (see Fig. 2.7).

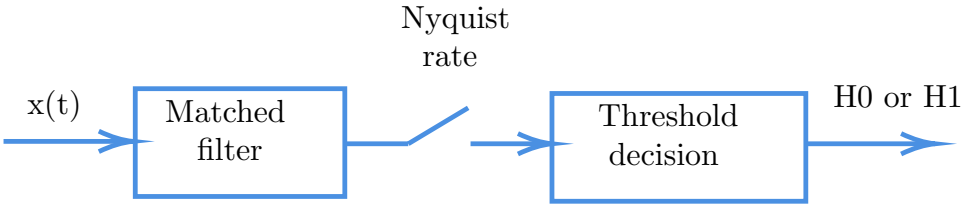


Figure 2.7 – Matched Filtering.

The short detecting time required while resulting in a optimal sensing performance is the main advantage of this technique. Nonetheless, matched filter performance decreases if the SU does not have sufficient knowledge about the PU signal. Moreover, it requires an exclusive receiver for each PU signal type, leading to high implementation complexity, and large power consumption.

2.2.5 Eigenvalue-based Detector

This technique obtains the covariance matrix based on the correlation among the received signal samples [65, 66]. Then, it uses the min to max eigenvalue of the covariance matrix as the test statistics that are finally compared to a threshold in order to decide on the PU presence. To do this, previous information of PU signals and/or the transmission channel are not required to overcome problems related to noise uncertainty [65]. Eigenvalue-based Detector can be classified into [67]:

- Max-min eigenvalue detection: the test statistic denotes the ratio of maximum and Minimum eigenvalue of covariance matrix.
- Energy with min eigenvalue: the test statistics is the ratio of received signal average power to Minimum eigenvalue.
- Max eigenvalue detection: the test statistics is provided by the maximum eigenvalue.

Although the main techniques have been presented, there are other narrowband spectrum sensing techniques such as multi taper spectral estimation [68] and radio identification-based sensing where the CR knows the technology used by PU.

2.2.6 Discussion

The waveform-based sensing outperforms energy detector in convergence time and reliability [59]. On the other hand, since matched filtering has robust performance in low SNR, it can assist the energy detector for very weak signals [63]. In [34], the authors compare performances of the matched filtering technique and the energy detector. The results show that the sensitivity and efficiency for matched filtering rapidly decrease with rising in average fluctuation of noise power. To overcome this problem, the threshold can be adjusted.

Fig. 2.8 illustrates a comparison of the narrowband spectrum sensing techniques addressed above in terms of accuracy and complexity [19]. Comparison in terms of advantages and disadvantages are presented in Table 2.1 [4, 69, 70].

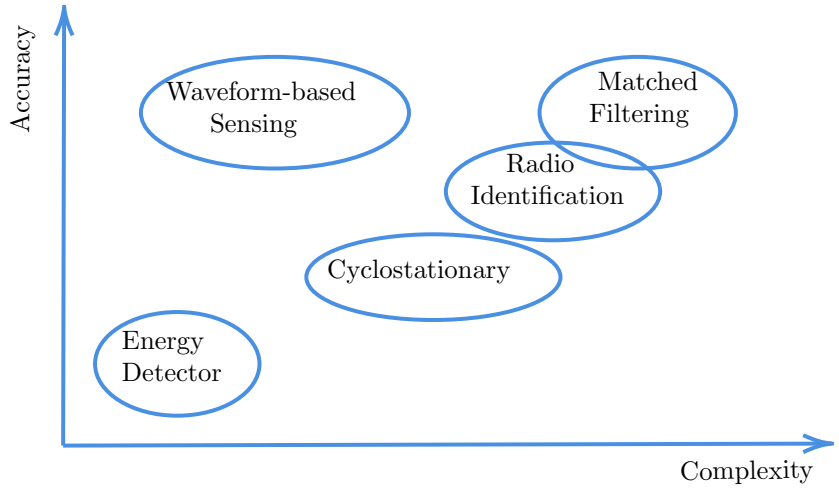


Figure 2.8 – Comparison of the narrowband spectrum sensing techniques in terms of accuracy and complexity.

2.3 Wideband Spectrum Sensing

In the narrowband spectrum sensing, only a narrow frequency range is exploited. However, to increase the chance of finding more spectrum opportunities, a wide frequency range normally is used [25]. While in the narrowband spectrum sensing techniques the interest is only to know if the band is occupied or not (a single binary decision for the whole spectrum), in the wideband spectrum sensing techniques the knowledge of which part of the spectrum is not being used now is required. Therefore, the narrowband spectrum sensing techniques can not be directly employed in the wideband spectrum sensing.

Wideband spectrum sensing faces several technical challenges. One of the main challenges is to lead with very high sampling rates required by conventional spectral estimation methods. According to the Nyquist theorem, in order to perfectly recover a signal, it is necessary for the rate to be, at least, equal to twice the maximum signal frequency. That is, it would be necessary to implement analog-to-digital converters (ADCs) with a high sampling rate to down-converter wideband signals [23]. This can generate a large number of samples and so requires large sensing time, a great deal of storage space and high power consumption. Moreover, implementing this sampling hardware could be very costly, complex, and even physically impractical due to high data rates and speed of the hardware required.

However, in several situations, the range of the spectrum analysed is not fully utilized and it can be considered sparse or compressible, that is, the majority of the signal coefficients in its

Table 2.1 – Comparison of the narrowband spectrum sensing techniques.

Technique	Advantage	Disadvantage
Energy Detector	• Non-coherent • Implementation and computational simplicity • Does not require previous information about PU	• Vulnerable to noise uncertainty • Poor performance for low SNR • Cannot differentiate users and noise
Cyclostationarity	• Robust against interference • Performs efficiently in very low SNR	• High computational complexity • Requires previous information about PU
Waveform-based Sensing	• Robust to noise uncertainty • Can detect signals with low SNR • Fast sensing as compared to energy detection	• Requires previous information about PU • Susceptibility to synchronization errors • Higher accuracy requires a longer length of known sequences that results in lower efficiency of the spectrum
Matched Filtering	• Short detecting time • Optimal performance • Less time required to achieve high processing gain	• Large power consumption • Requires previous information of the PU • Exclusive receiver for each PU signal type
Eigenvalue-based Detector	• Non-coherent • Robust to noise uncertainty • Can detect signals with low SNR	• High computational complexity

discrete representation are equal or near to zero. In other words, even if a large bandwidth is analysed, only a part of the information is actually relevant, that is, it has a low "information rate" [71].

In these scenarios, Compressive Sensing (CS) theory (see Section 3.1) can be applied to reduce the sampling rate and thus reduce the energy consumption. CS allows for the recovery of sparse or compressible signals from a lower sample rate than the Nyquist rate [72]. Moreover, with fewer samples required, the storage memory space and the signal processing decrease. In order to acquire a signal at rates close to its information rate, and which have a more energy-efficient spectrum sensing, several Analog-to-Information Converters (AICs) have been proposed (see Section 3.2).

Therefore, to deal with the wideband spectrum sensing problem, two main classes of solutions are possible: Nyquist Wideband Sensing and Sub-Nyquist Wideband Sensing [4, 25]. This section presents the more common wideband spectrum sensing techniques (see Fig. 2.4).

2.3.1 Nyquist Wideband Sensing

Nyquist Wideband Sensing methods use the Nyquist rate to sample the spectrum. An approach is to use a standard ADC to directly acquire the wideband signal [73]. Other approaches "divide" the large spectrum into several narrowband spectrum to be analysed. However, normally, these methods encounter high sampling rates, high computational complexity and processing delays [4, 74–76]. Some Nyquist wideband sensing techniques are [4, 25]:

- Multiband joint detection or FFT-based sensing [73, 74, 77]: firstly, the wideband signal $x(t)$ is sampled by an ADC at a high sampling rate (see Fig. 2.9). The sampled data is divided into parallel data streams by a serial-to-parallel conversion circuit (S/P). Then, the Fast Fourier transform (FFT) converts the wideband signals to the frequency domain. The wideband spectrum $X(f)$ is divided into the narrowband spectrums $X_1(f),\ldots,X_n(f)$. Optimization techniques choose the optimal detection thresholds. Finally, in order to detect spectrum opportunities, binary hypotheses tests are performed considering H_0 and H_1. Some limitations of this technique are the power consumption and a high sampling ADC. In order to reduce these limitations, the authors in [74] developed an adaptive multiband spectrum sensing procedure composed by two phases: the exploration phase and the detection phase. In the former, the accumulated statistic of each channel is used to progressively eliminate parts of the available channels. Then, the detection phase identifies the spectrum holes among the remaining channels.

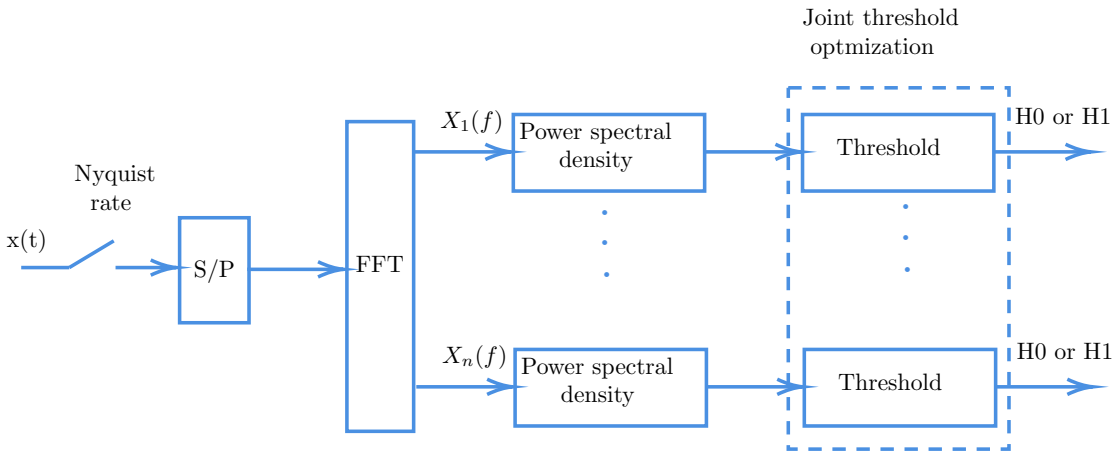


Figure 2.9 – Multiband joint detection or FFT-based sensing.

- Wavelet-based detecting [75, 78–80]: this method uses an ADC at a Nyquist sample rate and then FFT (see Fig. 2.10). Next, the power spectral density (PSD) of the wideband spectrum $S(f)$ is modeled as consecutive frequency sub-bands, where the PSD is smooth inside each sub-band, although it shows irregularities and discontinuities on the boundary of two neighboring sub-bands. Finally, the wavelet transform is used to detect the singularities of the wideband PSD. According to the PSD level of each channel, the bands are classified as vacant or occupied.

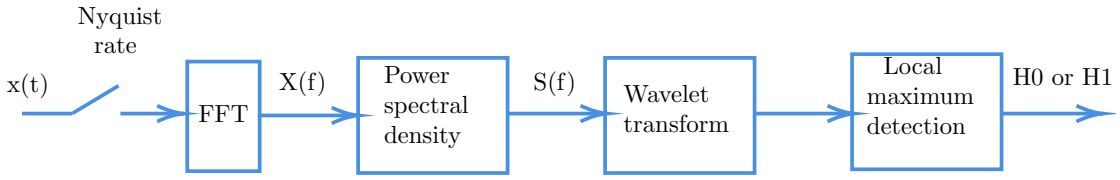


Figure 2.10 – Wavelet-based detection.

- Sweep-tune detection: this technique tries to reduce the high sampling rate using frequency mixing which "sweeps" across the frequency range (see Fig. 2.11). The local oscillator (LO) generates a sine wave which mixes with the wideband signal and then down-converts it to a lower frequency. A bandpass filter (BPF) filters the resulting signal. Then, a narrowband spectrum sensing technique can be used.

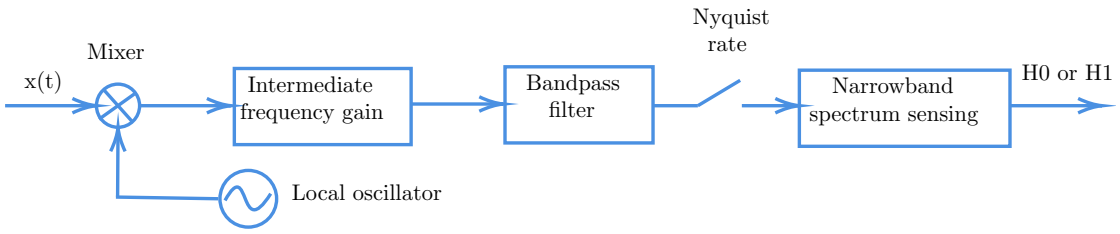


Figure 2.11 – Sweep-tune detection.

- Filter-bank detection [76, 81, 82]: this technique uses a bank of filters with different shifted central frequencies (see Fig. 2.12). In each band, the analysed part of the spectrum for the wideband signal is down-converted and low-pass filtered. Therefore, a lower sampling rate can be used in which branch. Then, a narrowband spectrum sensing technique is applied. The parallel structure of the filter bank leads to a large number of RF components in its implementation.

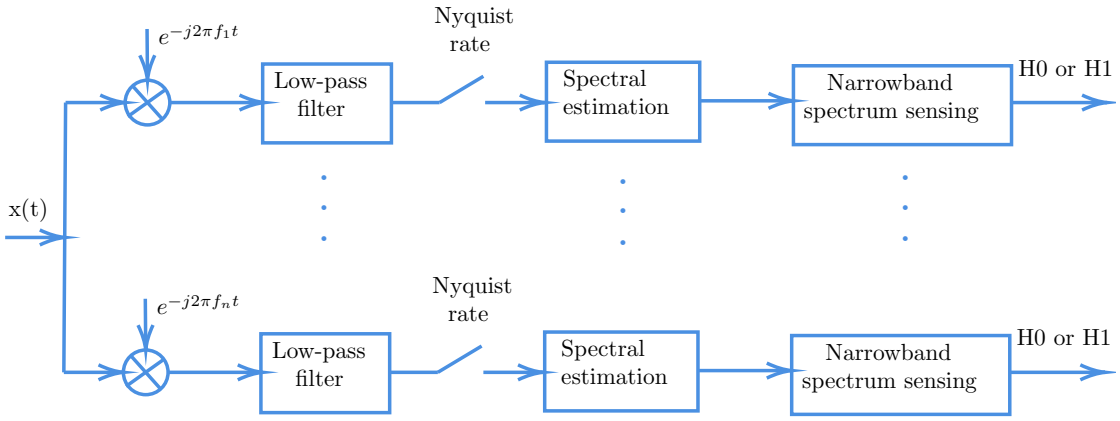


Figure 2.12 – Filter-bank detection.

2.3.2 Sub-Nyquist Wideband Sensing

These methods acquire wideband signals using sub-Nyquist rates, in other words, sampling rates that are lower than the Nyquist rate. In order to do this, compressive sensing can be used to recover the spectrum from fewer samples. Multi-cosets techniques can also reconstruct the spectrum from fewer samples choosing a sampling sequence that enables this reconstruction. Normally, these approaches can achieve lower computational complexity, decrease the sensing delay or reduce the hardware cost due to a high sampling rate in Nyquist-based implementations [4, 83, 84]. Some sub-Nyquist wideband sensing methods are [4, 25]:

- Compressive sensing-based wideband sensing [8, 84–93]: this uses the fact that, for several

times, the wideband spectrum can be considered sparse due to its low spectrum utilization. Then, it is possible to sense the wideband spectrum through fewer samples, closer to the information rate. More details are presented in Chapter 3.

- Multi-coset sampling (MC) [83, 94, 95]: it can be considered as a case of the general periodic non-uniform sub-Nyquist sampling method for acquiring sparse multi-band signals. In this technique some samples are chosen from a uniform grid (see Fig. 2.13). This grid can be generated using a sampling rate f_s higher than the Nyquist rate. Then, the samples are divided into blocks of n consecutive samples, and $p(p < n)$ samples are kept in each block. In order to do this, p sampling channels with the sampling rate of f_s/n can be used to implement Multi-coset sampling. Therefore, the sampling rate in each channel is n times lower than the Nyquist rate. One challenge of this approach is the channel synchronization.

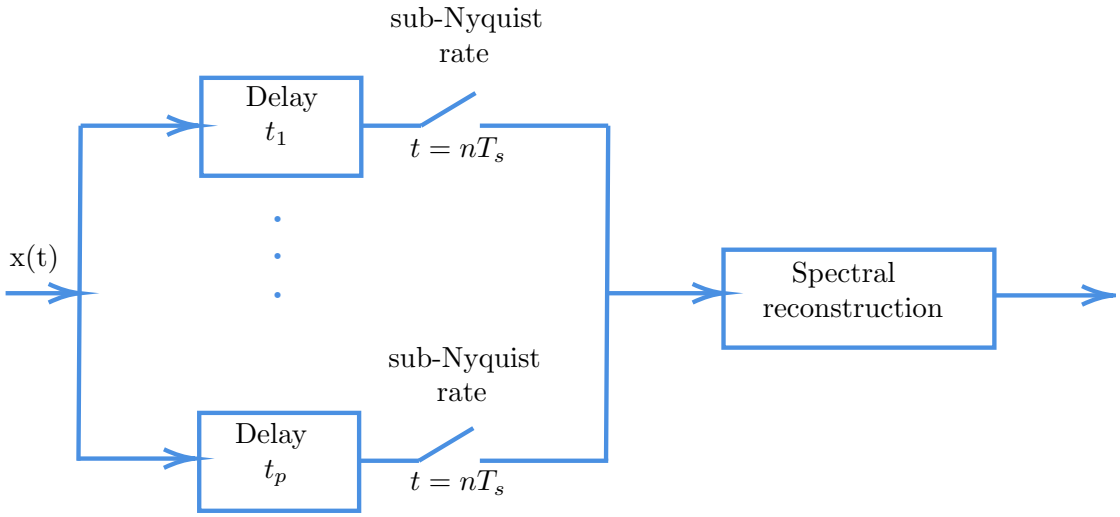


Figure 2.13 – Multi-coset sampling.

The wideband signal's sparsity can be time-varying and difficult to estimate resulting from the time-varying channels and the dynamic activities of PUs. Therefore, a challenge related to sub-Nyquist wideband spectrum sensing is to find the spectrum opportunities without previous knowledge about it sparsity.

2.3.3 Discussion

In [87], the authors proposed to sense the spectrum in two steps. Firstly, the actual sparsity is estimated and then the compressed measurements are adjusted. Differently, an adaptive compressive sensing approach which does not require sparsity estimation is presented in [91] . On the other

hand, the authors in [92] propose a power spectrum estimation method. Another approach is to select adequate measurements using compressive sensing based on the covariance [93].

Table 2.2 presents a comparison between the wideband spectrum sensing techniques addressed above [4].

This thesis focuses on wideband spectrum sensing. After the study of the spectrum sensing techniques, the sub-Nyquist wideband sensing was chosen specifically compressive sensing-based wideband sensing. More details are provided in the next chapter.

Table 2.2 – Comparison of the wideband spectrum sensing techniques.

Technique	Advantage	Disadvantage
FFT-based sensing	• Non-coherent • Reasonable complexity	• Require high sampling rate
Wavelet-based detecting	• Non-coherent • Edge detector	• High computational complexity
Filter-bank detection	• Non-coherent • High performance	• High computational complexity
Compressive Sensing-based wideband sensing	• Non-coherent • Low power • Low sampling rate	• Sparsity assumption • High computational complexity • Dynamic behaviours for sparsity level
Multi-coset sampling	• Non-uniform sampler • Can reconstruct the spectrum	• Require sychronization circuits

Chapter 3

Spectrum Sensing based on Compressive Sensing

This chapter begins with key concepts related to compressive sensing theory. Then, several analog-to-information converter architectures are discussed. Finally, some analog-to-digital converters are addressed.

3.1 Compressive Sensing Theory

Compressive Sensing (CS) theory can be used in situations where the signal is sparse or compressible [72, 96]. Combining the acquisition and compression processes and exploiting the signals' sparsity, the signal can be recovered from fewer measurements than what is required by the Nyquist theorem.

In order to do this, firstly, the signal of interest $\mathbf{z}$ with size N is represented as a linear combination of just s basis vectors, with $s \ll N$, that is, $\mathbf{z} = \Psi\mathbf{h}$, where $\mathbf{h}$ is the sparse signal. Then, $\mathbf{z}$ is measured by sampling it with respect to a matrix $\Phi \in \mathbb{C}^{M \times N}$:

$$\mathbf{y} = \Phi\mathbf{z} + \mathbf{n} = \Phi\Psi\mathbf{h} + \mathbf{n} = \mathbf{A}\mathbf{h} + \mathbf{n} \tag{3.1}$$

where $\mathbf{y}$ denotes the received signal with size M ($M < N$), and $\mathbf{n}$ is the noise.

Finally, the signal is reconstructed through a sparse recovery algorithm [97] such as Basis Pursuit (BP) [98], Orthogonal Matching Pursuit (OMP) [99], and Iterative Reweighted Least Squares (IRLS) [100]. Here, only the OMP algorithm is described in more details because it was used in

the simulations presented in Chapter 5.

The Orthogonal Matching Pursuit algorithm This algorithm is an improvement of the Matching Pursuit (MP) algorithm [99]. It can be stated as follows:

- Step 1: Initialize $\mathbf{b}_0 = \mathbf{y}$, $\Lambda_i = \emptyset$, and $i = 1$.
- Step 2: Find l that solves the maximization problem $\max_l ||P_{a_l}\mathbf{b_{i-1}}||_2 = \max_l \frac{\mathbf{a}_l{}^H \mathbf{b}_{i-1}}{||\mathbf{a}_l||_2^2}$ and update $\Lambda_i = \Lambda_{i-1} \cup \{l\}$.
- Step 3: Calculate $\hat{\mathbf{h}}_i = \mathbf{A}^{\dagger}(\Lambda_i)\mathbf{y}$ and update $\mathbf{b}_i = \mathbf{y} - \mathbf{A}(\Lambda_i)\hat{\mathbf{h}}_i$.
- Step 4: Stop the algorithm if the stopping condition is achieved (e.g. $||\mathbf{b}_i|| \leq \varepsilon$). Otherwise, set $i = i + 1$ and return to Step 2.

In the OMP algorithm, the residual vector $\mathbf{b}_i$ is always orthogonal to the columns that have already been selected. Therefore, there will be no columns selected twice and the set of selected columns is increased through the iterations [97].

The compressive sensing theory can be applied in several areas such as spectrum sensing [97]. Since usually only some of the available bands of frequencies are occupied by the users, the signal of interest is normally sparse in the frequency domain. Hence, the CS can be used to sense a wider spectrum with reduced sampling requirements, resulting in more power efficient systems [4, 25, 97, 101, 102].

Spectrum Sensing based on Compressive Sensing This technique samples the spectrum close to their information rate, reducing the high cost of performing the sampling at a high Nyquist rate. Fig. 3.1 illustrates the main steps to do spectrum sensing based on compressive sensing. Firstly, a sub-Nyquist sampler obtain few measurements of the spectrum. Then, the spectrum is recovered from the measured samples. Finally, the occupied sub-bands are localized and identified. A narrowband spectrum sensing technique can be applied to identify which band is occupied. Then, the SU can decide in which band it will transmit.

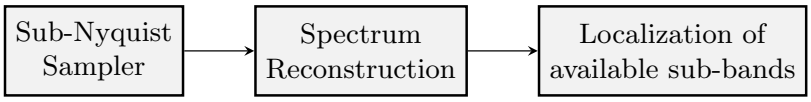


Figure 3.1 – Spectrum sensing based on compressive sensing.

Therefore, reducing the sampling requirements, it is possible to achieve cheaper and more power efficient systems. An alternative approach to the conventional ADC is the use of an analog-to-information converter (AIC) to carry out the analogue compressive sensing. AICs have been developed in order to digitize only the information as a solution to the Donoho's inquiry: "The phenomenon of ubiquitous compressibility raises very natural questions: why go to so much effort to acquire all the data when most of what we get will be thrown away? Can we not just directly measure the part that will not end up being thrown away?" [72].

3.2 Analog-to-Information Converter (AIC)

Analog-to-Information Converters are based on compressive sensing to acquire and extract the spectral activity information. The AIC enables faster processing, is less expensive, and has more energy-efficient solutions than the conventional ADC [103]. Indeed, high sampling has a major impact in the system consumption. Moreover, reducing the amount of samples sent increases the information transmission rate and this reduces hardware area, storage memory, and computational power. Hence, it is an alternative to be used in many latency-critical, cost-sensitive, and low-power devices such as IoT, cognitive radios, and electrocardiograms (ECGs) [103]. Fig. 3.2 shows the AIC architectures addressed in the next sections.

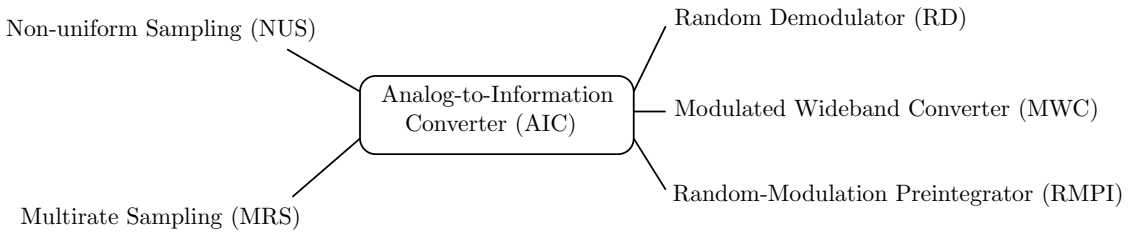


Figure 3.2 – Analog-to-Information Converters.

3.2.1 Multirate Sampling (MRS)

Fig. 3.3 illustrates the schematic of a Multirate Sampling. The input signal is undersampled with different sampling rates. Then, the signal passes through a bank of parallel bandpass sampling stages whose each branch has a different sampling rate [104, 105]. Since MRS avoids any randomness during the sampling stage, it is relatively simple in terms of hardware implementation.

An asynchronous multirate wideband sensing approach is discussed in [106]. It does not require perfect synchronization between the channels because the interest is only in the magnitudes of sub-Nyquist spectra.

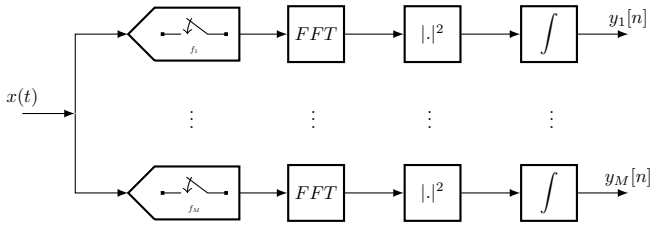


Figure 3.3 – Multirate Sampling (MRS).

3.2.2 Modulated Wideband Converter (MWC)

A Modulated Wideband Converter is showed in Fig. 3.4 [107–109]. As can be seen, the product of the multiplication between the input signal and a bank of periodic waveforms is lowpass filtered and then uniformly sampled at a low rate. Fig. 3.5 illustrates a spectrum of a signal $x(t)$ and the spectrum of the outputs $y_i[n]$ and $y_{i'}[n]$.

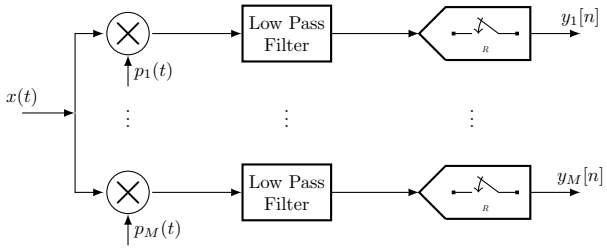


Figure 3.4 – Modulated Wideband Converter (MWC).

3.2.3 Non-Uniform Sampling (NUS)

Fig. 3.6 illustrates a Non-uniform sampling. In this AIC, a random number of samples is taken by sampling the input signal at irregularly spaced time intervals. It consists of a sample-and-hold (S&H) stage and an ADC [103, 110, 111]. Since the sampling rate has a big influence on the total system energy consumption, random sampling drastically decreases the energy by capturing the significant samples based on the signal feature.

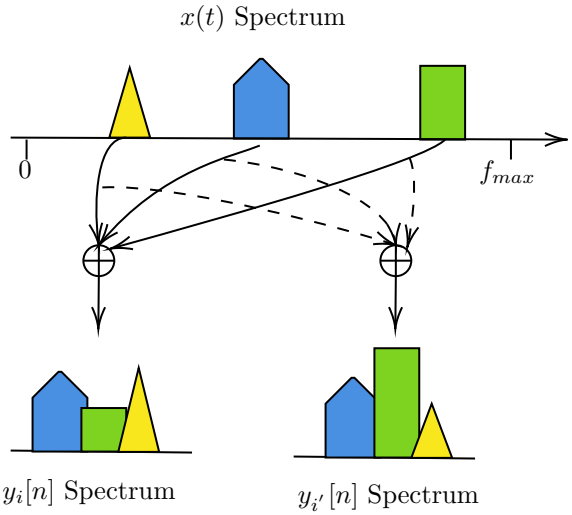


Figure 3.5 – The linear combination in base band of 2 banks of the MWC.

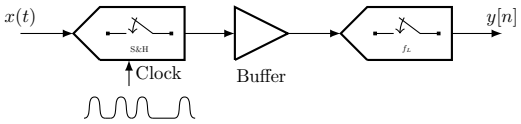


Figure 3.6 – Non-Uniform Sampling (NUS).

3.2.4 Random-Modulation Preintegrator (RMPI)

A Random-Modulation Preintegrator is exemplified in Fig. 3.7. The input signal is multiplied by several pseudo-random sequences and the product of each multiplication is integrated. After that, it is sampled [112]. This architecture is relatively universal, since it works with signals that are sparse in any fixed domain [113].

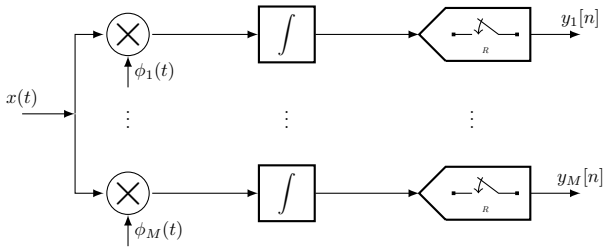


Figure 3.7 – Random-Modulation Preintegrator (RMPI).

3.2.5 Random Demodulator (RD)

Fig. 3.8 illustrates a Random Demodulator. It is a single branch of the RMPI [86, 114–116]. Firstly, a high-rate pseudonoise sequence $\phi_1(t)$ multiplies the input signal $x(t)$ to smear the tones

across the entire spectrum [86]. Therefore, the information contained in $x(t)$ also spreads across the spectrum. Then, the result is integrated and finally it is sampled at a low sampling rate.

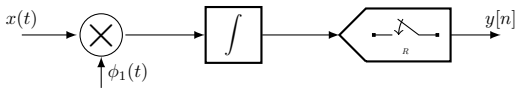


Figure 3.8 – Random Demodulator (RD).

Since the high frequency contents of the chipping sequence satisfies the Nyquist rate, the ADC operates at sub-Nyquist rates. According to [86], for an s-sparse input signal whose highest frequency is $W/2$, the RD AIC with a sample rate of $O(s \cdot log(W/s))$ Hz can acquire enough information to recover the input signal. Therefore, high speed hardware components are only required for the generation of the $\phi_1(t)$. Moreover, it is worth mentioning that it is less complex to generate the chipping sequence at the Nyquist rate than to implement the ADC at the Nyquist rate.

3.2.6 Discussion

As can be noticed, the AIC aims at acquiring information decreasing the number of measurements while still enabling faithful recovery. The AIC architectures which require random sequences have to take into account the memory necessary to store the sequences or efficient means for generating them. Some challenges related to AIC are:

- efficient methods for generating pseudo-random sequences or memory to store the random sequences;
- high signal processing complexity and power consumption with the utilization of fast linear transforms (such as the FFT) in the recovery algorithm;
- large number of branches resulting in high power consumption and large silicon area;
- noise folding impairing the use of AIC in applications which require high sensitivity, such as activity detection of low-SNR;
- adaptability to the application, that is, the possibility of flexible configuration that prioritizes the most important features for the application.

It can be seen that each AIC architecture has advantages and limitations. While the MRS AIC has noise folding, once wideband noise in the input signal is aliased into the compressive

measurements, a reduced sensitivity is delivered as a consequence, the NUS AIC is sensitive to timing jitter, i.e., for input signals which change rapidly, a small error in the sampling time can lead to a significant error in the sample value. As the MRS AIC, MWC AIC, and RMPI AIC require a large number of branches, they require synchronization among the branches. While the sampling functions of the RD AIC have infinite spectral support and finite temporal extent, the sampling functions used in the MWC AIC have finite spectral support and infinite temporal support [101].

Nevertheless, the lower number of acquired measurements makes the reliability of AIC becoming a major issue. The comparator or the set of them is normally an essential component in ADCs. Therefore, their minimum consumption and correct functioning are of great importance for the correct functioning of the entire system. It is possible to reduce the total consumption of an AIC through the use of comparators of lower energy consumption that are also robust against SET. With this in mind, a dynamic comparator in 28 nm FDSOI technology is analysed in terms of robustness to SET in the Section 5.1.

3.3 Analog-to-Digital Converter (ADC)

As can be seen in Section 3.2, all these AIC architectures require an ADC. The choice of an ADC can be made taking into account the resolution (number of bits), sample rate, gain, offset, DNL (differential nonlinearity), INL (integral nonlinearity), SINAD (signal-to-noise-and-distortion ratio), SFDR (spurious free dynamic range), THD (total harmonic distortion), among others. In the next sections, a brief description of the main ADC architectures is presented.

3.3.1 ΣΔ ADC

The ΣΔ ADC is based on the principle of oversampling the input signal. It contains a group of analog electronics (a comparator, voltage reference, a switch, and one or more integrators and analog summing circuits), and significant digital computational circuitry which has a digital signal processor (DSP) which acts as a filter (see Fig. 3.9) [117]. In other words, it consists of a loop system allowing the input to be oversampled beyond the output sample rate (Kf_s), and a digital filter (decimator) which ensures a reconstruction of the binary word at the output sample rate (f_s) and removes out-of-band noise.

Oversampling the analog input and then filtering the digital output while keeping only the useful band of the signal minimizes the power of the quantization noise in the useful band of the

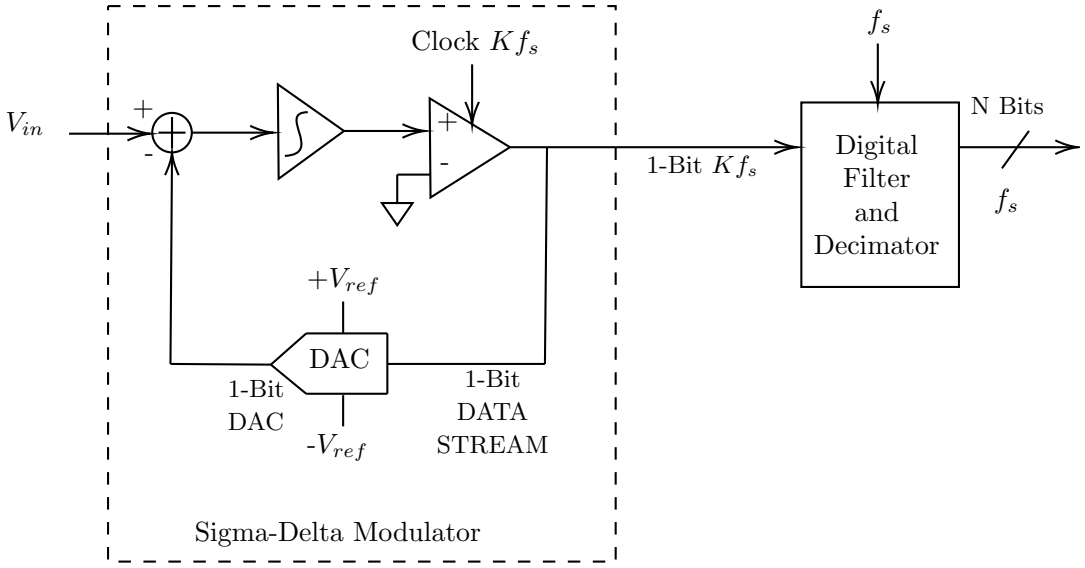


Figure 3.9 – First-order ΣΔ ADC.

signal and consequently increases the SNR. In addition to the oversampling technique, this ADC uses the Sigma-Delta modulation which shapes the quantization noise in order to reduce its energy in the useful band and to further increase the SNR. This technique is called Noise Shaping: the noise will be reduced at low frequency and rejected towards the high frequencies. After digital low pass filtering and decimation (decimator filter), the out-of-band noise will be removed and the operation of the system will be reduced to the output sample rate f_s. Due to its characteristics, ΣΔ ADC is still a topic in constantly development [118, 119].

3.3.2 Successive-Approximation-Register (SAR) ADC

Fig. 3.10 shows the SAR ADC topology. It consists on a sample-and-hold (S&H) stage, a comparator, a Digital to Analog Converter (DAC) and a control component called "SAR logic". As can be seen, a SAR ADC feeds the decision made back to compensate for the result of the previous comparison.

The S&H stage is responsible for hold the voltage of the input signal when it was sampled until the next sampling instance. The comparator generates the output by deciding which of its input signals is larger. It is a key component of the ADC. The accuracy of the comparator determines the conversion quality of the ADC. Moreover, as during the ADC process several comparisons are made, the comparator speed is decisive in the speed of the whole ADC. Several types of comparators have been proposed. One of the most popular used in SAR ADC is the StrongARM

comparator due to high speed and low power consumption [120–123].

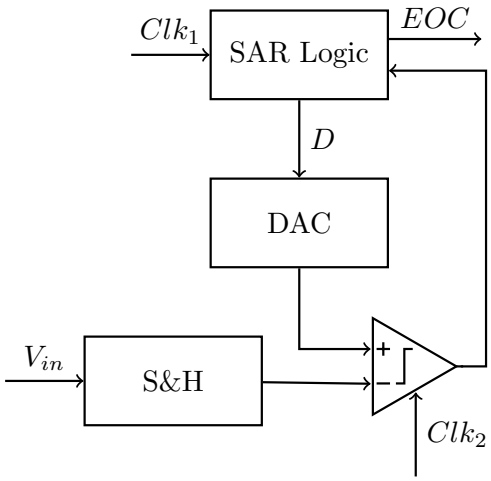


Figure 3.10 – SAR ADC topology.

The SAR logic component controls the operation of the whole ADC. Its mainly functions are: clock generation, memory, and the state machine. All the clock signals required for the operation of the ADC (for example the clocks for the comparator and for sampling) are generated by the clock generation. The comparison outputs are stored in the memory and they are used to feed back information of previous decisions. And the state machine is responsible for control all the operation, it means it controls when each clock signal should be active or not and where the data should be stored in the memory. Finally, the DAC generates the feedback reference voltage to be compared with the input signal in the comparator.

One of the advantages of the SAR ADC is that it is not necessary have amplifiers which require biasing [124, 125]. However, the linearity of the DAC used in the generation of the reference voltage influences on the linearity of the ADC. Moreover, the speeds of the comparator and the control logic component are constraints in the SAR ADC operation speed.

3.3.3 Pipeline ADC

This ADC spreads the conversion over several clock cycles. For each stage, one or a few reference voltage levels can be required performing a coarse quantization per stage, the subtraction of the corresponding value from the analog input, and then the signal amplification before the next stage [126]. A digital logic is required to delay the data given by the first stages because the first stages outputs arrive many clock cycles before the data from the last stages (see Fig. 3.11 and Fig. 3.12 where each stage gives two bits of data) [127].

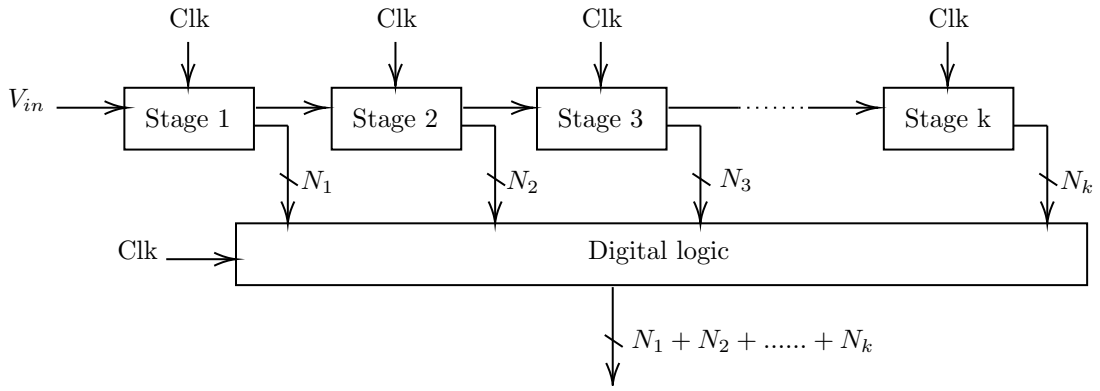


Figure 3.11 – Pipeline topology.

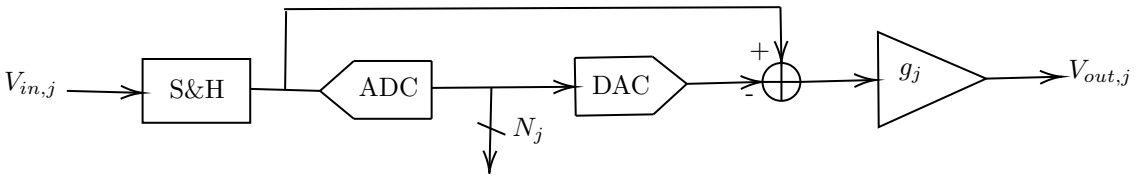


Figure 3.12 – Pipeline stage topology.

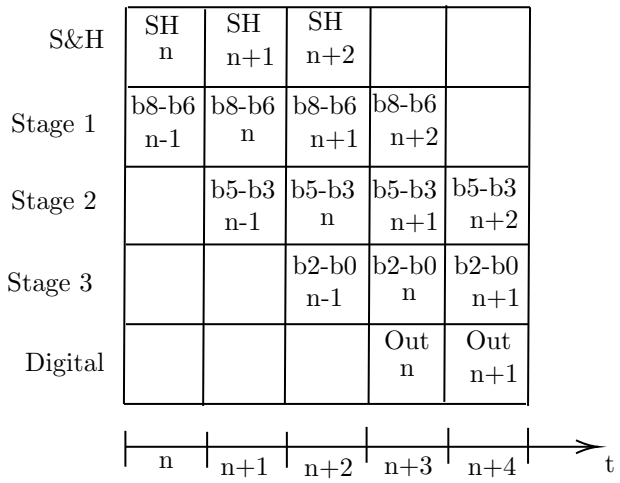


Figure 3.13 – Timing diagram for pipeline topology.

Fig. 3.13 illustrates the timing diagram for pipeline topology. The multi cycle behaviour leads necessary to re-sampling the signal in between each stage. In other words, for N-bit to be converted and M bits per stage, N/M sample and hold circuits, N/M amplifiers and DACs together with $(N/M)2^M$ comparators are required. The stages in a pipeline ADC can be a SAR or a flash ADC and it can be different in each stage. Moreover, the stages can have different resolutions [126]. Normally, the flash ADC are chosen for the stages. The gain of the amplifier and the linearity of the sub-ADCs and DACs are the critical factors of the pipeline ADC. To overcome the linearity

problems, 1-bit stages can be used. The biasing current required in the amplifiers result in high power consumption. In addition, the multiple instances lead to large footprint [128].

3.3.4 Flash ADC

This ADC gives the output in a single clock cycle. It compares the input signal with all the decision levels [126]. These results are encoded with zeros when the input signal is lower than the reference voltage, and with ones otherwise. Then, the encoded data is usually converted into binary encoding (see Fig. 3.14).

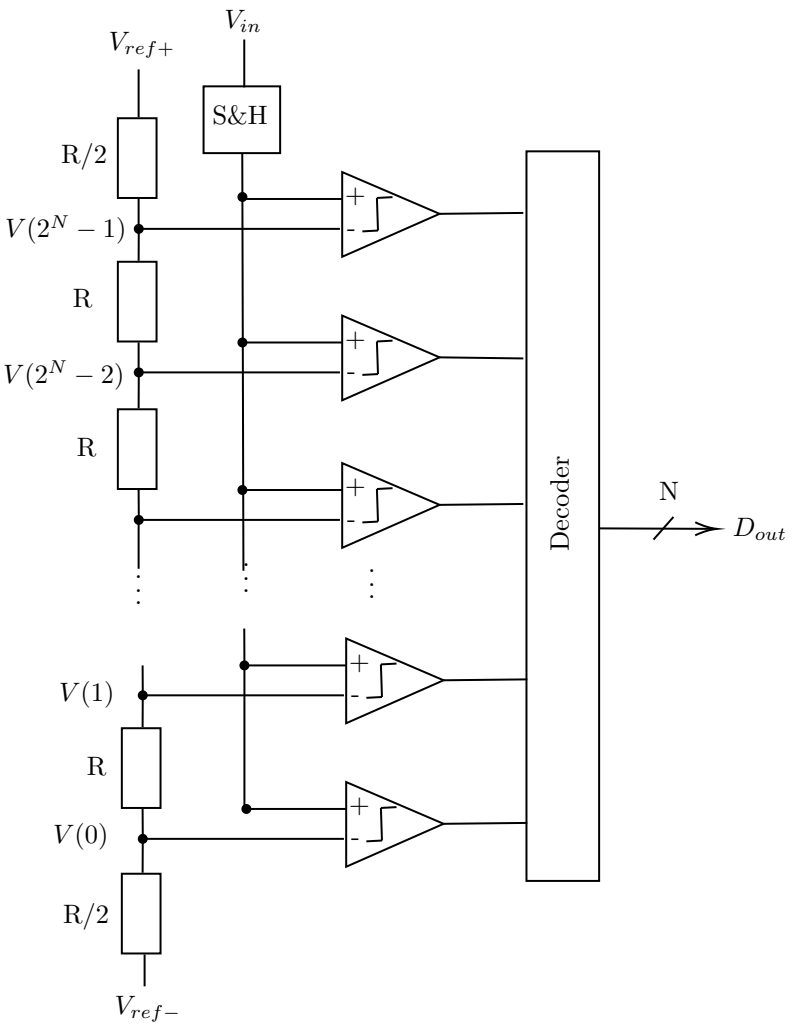


Figure 3.14 – Flash ADC.

In this ADC, the decisions are taken simultaneously. Therefore for each decision level, one comparator and a unique reference voltage level to compare the input are required. A resistive network can generate the reference voltages (see Fig. 3.14) [127]. However, generating them

in this way can cause several problems. Since the direct path from positive to negative voltage supply causes a constant DC current, it leads to a high power consumption [127]. Furthermore, the resistive network suffers from random mismatch and global processing variations due to the large area required for implementing this reference voltage divider. Therefore, these mismatch problems result in a non-linear response [127].

3.3.5 Discussion

The flash ADC and SAR ADC architectures are the most used in high-speed applications. The flash and pipeline ADC require a single comparison per sampling instance, while the SAR ADC needs N successive comparisons between each sampling instance [127]. However, while the flash ADC needs a clock cycle to converter, the pipeline ADC requires several clock cycles leading to a latency from the signal is sampled until the result.

The power consumption of the flash ADC exponentially increases with resolution [124]. On the other hand, the pipeline ADC suffers from their amplifiers and sample and hold circuits which lead to high power consumption. The SAR ADC can be considered for the lowest power consumption due to its absence of amplifiers [124]. That's the reason the SAR ADC is widely used in low-power implementations [129].

Fig. 3.15 reproduces a simplified comparison in terms of bandwidth and resolution presented in [130]. The sampling rate can reach multiples of GHz while resolutions can range from a minimum of 1 bit to more than 20 bits per sample [129]. Normally, the ADCs which can have a high sampling rate are those that have the lower bit resolution. Although Fig. 3.15 represents the most implementations presented in the literature, it is worth mentioning that there are $\Sigma\Delta$ ADCs with high sampling rates [119, 131] as well as flash ADCs with high bit resolution [132].

In this chapter, some types of AIC and ADC were addressed. The traditional ADCs have faced several challenges in terms of sampling rate, bandwidth, and power consumption [129, 133]. Moreover, with the downscaling of CMOS, the increased static energy consumption has to be avoided. To overcome these issues and increase the ADC performance to attend the demands of IoT devices, cognitive radios, and other applications in terms of ADC constraints such as area, sampling rate, bandwith, and power consumption, new technologies and new device designs have been developed [134].

In the next chapter, challenges related to the hardware implementation of these devices are presented, such as how to reduce the consumption and the problem of the Single Event Transient

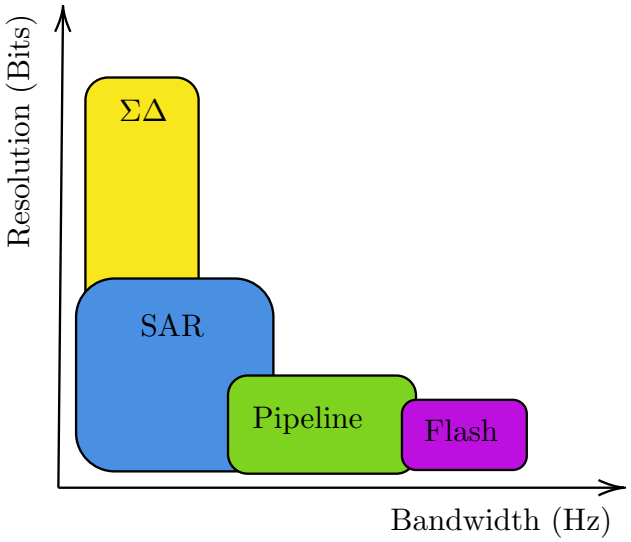


Figure 3.15 – ADC architectures.

(SET). As it is discussed in Chapter 4, Magnetic Tunnel Junction (MTJ) has appeared as one of the promising candidates due to its low power consumption and great scalability [135]. Indeed, MTJ has been explored in order to reduce the power consumption and save area of the ADCs (see Section 4.4.7). Moreover, in this thesis, an MTJ-based ADC is proposed and presented in Section 5.4.

Chapter 4

Hardware Challenges

Some of the hardware requirements related to spectrum sensing for cognitive radio applications are: large dynamic range for input analog signal, high sampling rate, high ADC resolution, and heavy signal processing. In other words, the RF components, such as antennas and power amplifiers, have to be able to operate over a range of wide operating frequencies. Moreover, the signal processing should have relatively low delay requiring sometimes high speed and configurable processing units (such as DSPs or FPGAs). As presented in Chapter 2 and in Chapter 3, AIC is an alternative approach to overcome high-speed ADCs which have huge power consumption. It is also desired reduce area and decrease the power dissipation.

FDSOI technologies can be used in order to implement high-speed/low-power devices as well as be less susceptible to radiations effects in terms of Single Event Transient (SET). On the other hand, the discovery of Giant Magnetoresistance (GMR) [136, 137] led to the development of spintronics [138]. Studies in this area have resulted in several important advances. With CMOS downscaling, the need of viable alternatives for reducing the leakage of power increases and spin-based devices appear as one of the most promising approaches to deal with this issue. Magnetic Tunnel Junction (MTJ) has a significant role in the spintronics development [135]. Downscaling transistors to nanometers makes them more vulnerable to transient disturbances as SET [139] and thereby makes MTJ-cell more prone to errors. Although concerns about SET are related to circuits for satellites, space, and aeronautics mainly due to the direct effects of cosmic radiation, its ground-level study has been a growing concern for many years [140]. SET effects become even more relevant with advanced technologies, as their devices with nanometric dimensions have greater active areas in the circuits and high sensitivity to current and voltage variations.

This chapter begins with some FDSOI technologies characteristics. Then, the single event

transient is discussed. Finally, the magnetic tunnel junction and its applications are addressed.

4.1 Fully Depleted Silicon-On-Insulator (FDSOI)

Fig. 4.1 illustrates the implementation of a fully depleted silicon-on-insulator (FDSOI) CMOS and a standard bulk CMOS. As can be noticed, in FDSOI process a thin oxide layer isolates the channel and the bulk. Thanks to this, the undesirable effects related to the floating substrate are eliminated [141]. In addition, the insulator formed by the buried oxide (BOX) makes it possible to reduce in depth the surface of the source and drain diffusions. Consequently, the value of the junction capacitors of the transistor decreases, leading to better dynamic consumption of a switching logic gate compared to the bulk technology. Static consumption is also improved despite the short length of the channel because the effect of Drain Induced Barrier Lowering (DIBL) is minimized by increasing the electrostatic control of the channel by the grid. FDSOI transistors do not suffer from "latch-up" effects because they are electrically isolated from the substrate and adjacent transistors thanks to the buried oxide layer and Shallow Trench Isolation (STI) [142].

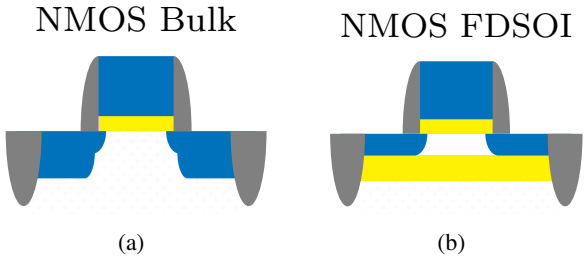


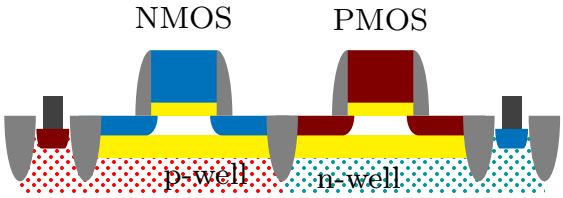
Figure 4.1 – Transistor structure in (a) Bulk CMOS (b) FDSOI CMOS.

The reduced input capacitance allows for increased speed and lower power consumption. Moreover, the use of FDSOI technologies result in higher performance while maintaining low leakage. Therefore they are attractive due to their high-speed/low-power features and its reliability has been extensively studied [143–147].

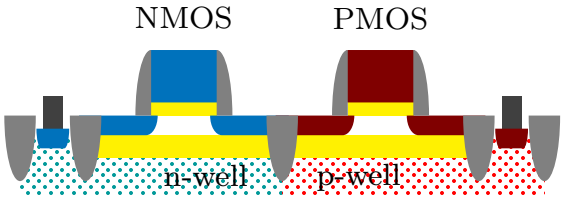
In addition, it is possible to use lower voltage source values for circuits using FDSOI technology. This technology has an intrinsic advantage to its structure when separating the channel from the body of the transistor. This allows the effects of SET due to radiation to be less than in bulk technology as the accumulated charge is limited to the region of the channel that is isolated from the body. Thus, the total effective energy that can directly cause disturbances in the functioning

of the reached transistor is reduced. Because of that, the 28 nm FDSOI technology is used in this thesis.

The PMOS and NMOS can have two different threshold voltage which are determined according to the type and concentration level of the doping of the area implanted under the BOX. These configurations are illustrated in Fig. 4.2. The initial value of the threshold voltage and the maximum voltage that can be applied to their grid are different in these structures. LVT transistors are widely used when fast switching speeds are required (amplifier, comparator, sampler) [142].



(a) Architecture RVT.



(b) Architecture LVT.

Figure 4.2 – Transistor structure: (a) Regular Voltage Threshold (RVT) (b) Low Voltage Threshold (LVT).

4.2 Single Event Transient (SET)

SET is important to be considered for device reliability, especially for space electronics [148]. SET results of deposited charge when ionizing energetic particles hit a sensitive region of the circuit. The data stored may be flipped causing an error when enough charge is collected.

The most widely used model considers that a SET can be described by a double-exponential current pulse $I_{inj}(t)$ on the transistor [149–152]. The current $I_{inj}(t)$ is defined by (4.1) where Q_{inj} is the charge injection level calculated by (4.2), K is related to the material characteristics and the radiation intensity, τ_1 is the collection time constant for a junction, and τ_2 is the ion track establishment time constant [149–151].

After a certain level of injected current, the voltage across the struck node can go beyond the power supply rails when the circuit-level SET simulations employ the independent current

models. However, this is a physically not reasonable behavior and it represents a disadvantage of this model. As showed in [153], the SET current waveforms obtained from TCAD simulations do not go beyond the power supply rails.

$$I_{inj}(t) = K.(e^{\frac{-t}{\tau_1}} - e^{\frac{-t}{\tau_2}}) \tag{4.1}$$

$$Q_{inj} = \int I_{inj}(t)dt \tag{4.2}$$

From TCAD simulation, it can be seen that for higher Linear Energy Transfer (LET) values, the SET-induced current pulse can not be well represented by a simple double-exponential expression [153, 154]. It has a *plateau* region after a very short high-amplitude current peak when higher levels of charge are generated [154]. To deal with this issue, some voltage-dependent SET current models has been developed [153, 155–157].

In this thesis, SET is generated by a voltage-dependent current model based on conventional double-exponential current pulse on the transistor taking into account the voltage across the node [157]. The current $I_{inj}(t)$ is defined by (4.3) where V_{DS} denotes the voltage between the drain and the source of the transistor. Fig. 4.3 shows the current source and transistor modelling SET event.

$$I_{inj}(t) = K.V_{DS}.(e^{\frac{-t}{\tau_1}} - e^{\frac{-t}{\tau_2}}) \tag{4.3}$$

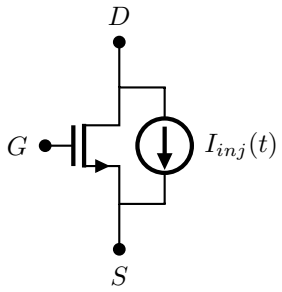


Figure 4.3 – Modelling the SET in NMOS.

Fig. 4.4 shows I_{inj} and V_D when a SET with $Q_{inj} = 1$ fC reaches the access transistor. It can be seen that when (4.1) is used to represent I_{inj} (curves in red), a strange phenomenon appears in V_D. In other words, during some time $V_D < 0$ showing an erratic behavior, the voltage goes beyond the power supply rails. On the other hand, this behavior does not occur when (4.3) is used to simulate

I_{inj} (curves in blue).

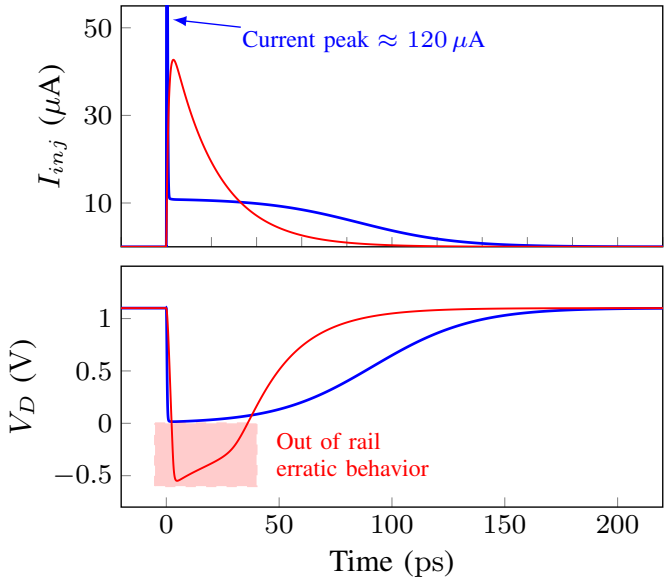


Figure 4.4 – I_{inj} and V_D when a SET with $Q_{inj} = 1\,\text{fC}$ reaches the access transistor. I_{inj} is defined by (4.1) and (4.3) in the red and blue curves, respectively.

4.3 Magnetic Tunnel Junction (MTJ)

Fig. 4.5 illustrates the basic MTJ structure. It consists of two ferromagnetic layers separated by the insulator layer MgO. The reference layer has unchangeable magnetization direction, while the magnetization direction can be changed in the free layer. Therefore, the magnetic field determines electrical properties of the MTJ. For applications, the difference of the conductance, resulted from the variations of the magnetic field in the ferromagnetic layers, is employed. The magnetization orientations (m_z) of the two ferromagnetic layers are related to a level of the MTJ resistance: low-resistance R_P at a parallel (P) state and high-resistance R_{AP} at an anti-parallel (AP) state. With these two stable states of the MTJ, it can be easily used to represent logic 0 or logic 1 [158–161].

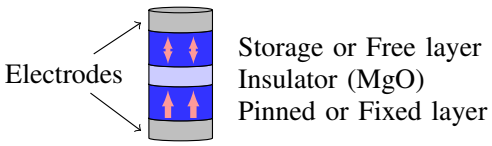


Figure 4.5 – Magnetic Tunnel Junction (MTJ).

In order to control the electrical characteristics of MTJs, some methods have been developed for switching their stable states. The three main MTJ magnetization switching mechanisms are

considered below.

4.3.1 Spin Transfer Torque (STT)

Spin transfer torque (STT) was presented in [162] as an alternative to improve the density of the first proposed MTJ circuits. The STT effect allows switch the MTJ state by a bidirectional current I when the current is bigger than a critical current I_{c0}. It improves the scalability of the circuit with MTJs allowing a denser layout and a simpler design due the use of the same line to write and read the MTJ state. However, using the same path can lead to unexpected writing when reading is in progress. Another disadvantage of the STT is that the current required to switch the states of the MTJ is not symmetrical (going from P to AP requires a bigger current than going from AP to P). Moreover, when using STT, a larger access transistor size is required, thus limiting the application density. Yet another challenge with scaling down using STT is that the thermal stability factor scales down linearly with the area and the increase in retention failures due to thermal instability results in unreliable operations [163]. STT-based applications also face problems when high write speed is required because the switching current of STT is inversely proportional to the write pulse width [163]. The MTJ behavior model is given by [164, 165]:

$$I_{co} = \alpha \frac{\gamma e}{\mu_B g}(\mu_0 M_s) H_k V \tag{4.4}$$

$$E = \frac{\mu_0 M_s H_k V}{2}, \tag{4.5}$$

where α is the magnetic damping constant, γ is the gyromagnetic ratio, e is the elementary charge, μ_B is the Bohr magneton, g is the spin polarization efficiency factor, μ_0 is the permeability of free space, M_s is the saturation magnetization, H_k is the effective anisotropy field, and V is the volume of the free layer. Equation (4.6) gives the average MTJ state switching delay time (τ) [164, 165].

$$\tau = \tau_0 exp\left(\frac{E}{k_B T}\left(1 - \frac{I}{I_{c0}}\right)\right), \text{ when } I < I_{c0} \tag{4.6}$$

$$\frac{1}{\tau} = \left[\frac{2}{C + ln(\frac{\pi^2 \varepsilon}{4})}\right] \frac{\mu_B P_{ref}}{e m_m (1 + P_{ref} P_{free})}(I - I_{c0}), \text{ when } I > I_{co}, \tag{4.7}$$

where τ_0 is the attempt period, k_B is the Boltzmann constant, T is the temperature, C is Euler's constant, ε is the thermal stability factor, m_m is the magnetization moment, P_{ref} and P_{free} are the

tunneling spin polarizations.

4.3.2 Voltage-Controlled Magnetic Anisotropy (VCMA)

Magnetoelectric effects have been studied with the aim at efficiently switching the MTJ state consuming less energy [166]. Efficient energy consumption and reduced area can be achieved if a voltage-controlled MTJ with an electric field (or a voltage) is used [167, 168]. With the VCMA effect, an electric field is used in order to switch the MTJ state. It occurs by an accumulation of electron charges induced by the electric field changing the occupation of atomic orbitals at the interface. This and the spin-orbit interaction lead to a change of magnetic anisotropy [166, 169, 170].

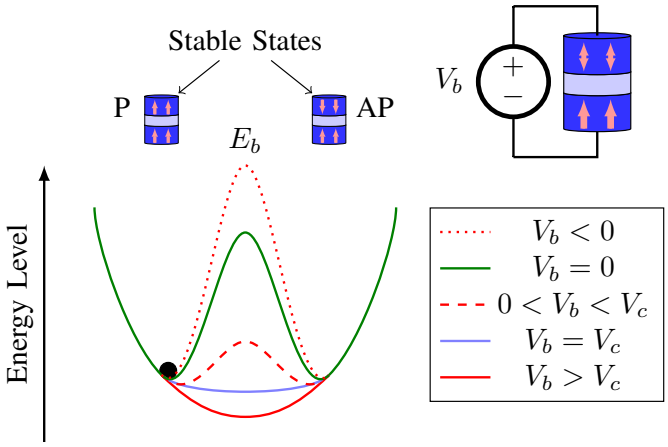


Figure 4.6 – Structure and stable states of the Voltage-Controlled Magnetic Anisotropy (VCMA)-MTJ device.

Fig. 4.6 outlines the VCMA-MTJ operational characterization. As the switching is performed through voltage, the increasing of the barrier thickness can decrease the parasitic conductance and so the effect of current-induced torques [163]. The energy barrier between the P and AP states can be reduced with the use of VCMA. Therefore, a voltage applied across the MTJ terminals facilitates the switch of its states. When the MTJ critical voltage V_c is smaller than the switching voltage V_b, the energy barrier E_b between two stable magnetization states can be eliminated. Equation (4.8) gives the minimum V_c for successful VCMA-MTJ switching [171]:

$$V_c = \Delta(0) k_B T t_{ox} / \xi A, \tag{4.8}$$

where ξ is the VCMA coefficient to weigh the perpendicular magnetic anisotropy (PMA) change under V_b, $\Delta(0)$ is the thermal stability under zero voltage, A is the sectional area of the MTJ, T is

the temperature, t_{ox} is the MTJ oxide layer thickness, and k_B is the Boltzmann constant.

The VCMA-MTJ dynamics changes continuously through its unstable states, once V_c is achieved [172]. The E_b of the intermediate states comes back to a greater value than the stable states leading to stabilize the MTJ in its P or AP state when the excitation of its terminals has finished. Compared to STT, VCMA does not require large currents facilitating the scalability of its applications and resulting in a lower power consumption. However, practical VCMA devices face reliability issues which have to be better understood [173]. To use the VCMA-MTJ in memory devices, a precise control of the writing process is required as will be discussed in Section 5.2.1.

4.3.3 Spin-Orbit Torque (SOT)

With the SOT technique, three terminals are used to separate the write and read paths allowing for a symmetrical switching current between the MTJ states. With that, the possibility of a bit flip during the read operation is reduced, therefore increasing the read stability [163]. When a current crosses the non-magnetic layer, spins are accumulated and a torque switching is generated over the magnetization of the ferromagnetic layer. A faster switching can occur using SOT with the elimination of the time-demanding precessional motion [174]. However, one disadvantage of SOT is that it requires bigger cell size than STT-based applications due to its three terminal structure, so it can be not compatible with high-density applications.

4.4 MTJ Applications

MTJ has excellent scalability, low power consumption, and potentially infinite endurance. In addition, unused MTJs can be completely powered off without the loss of data resulting in saving energy which render the MTJ suitable for several applications [135] such as memory devices and analog-to-digital converter. MTJ-based non-volatile memories (NVMs) have shown superior performance with respect to many relevant figure of merits such as energy efficiency and endurance [175]. MTJ-based memories allow for a ten year retention time operating at extremely low energy levels making them appropriate for batteries or low powered applications as internet of things (IoT) applications, specifically for sensor nodes located in difficult environmental conditions [176].

MTJ applications can also be found in several domains where data require processing and storage [177–180]. In radio frequency, spectrum-optimizing applications based on compressive

sensing [97] desire to reduce the area of their circuits and decrease power consumption. In order to do this, MTJs can be used in mixed signal applications, such as comparators and analog-to-digital converters [179, 180]. Relevant progress has been done in MTJ research and it is expected to develop even further into commercial products in the near future. This section reproduces some important MTJ applications discussed in [181].

4.4.1 Memory

One of the most known MTJ applications is the MTJ-based memory. Magnetic Random-Access Memory (MRAM) aims at combining the best characteristics of dynamic random-access memory (DRAM), static random-access memory (SRAM), and flash memory in order to become the "universal memory" [182, 183]. Using the intrinsic spin of electrons as a storage unit and the difference of the MTJ resistance in its parallel and antiparallel states to represent the "0" and "1" in the binary system, MTJs are applied as the basic elements in information storage.

The structures of MTJ-based MRAM differ in the write operation approach and the number of MOS transistors [184–187] used to build a unit cell of memory. Fig. 4.7a illustrates the spin transfer torque MTJ-based MRAM (STT-MRAM) bit-cell structure. Each bit-cell has only one transistor with the STT-MTJ allowing higher density memories. As it is shown in Fig. 4.7a, while the bi-directional current I_w is responsible for switching the MTJ state during the write operation, the MTJ state is defined comparing the read current I_r with a reference current [161]. It is worth mentioning that STT-MRAM is characterized by an asymmetric write operation. This occurs because the current required to switch from the AP to P state is smaller than that of switching from the P to AP state [186]. Therefore, in order to achieve the requirement of worse case of the write operations, the access transistor has to be large [185, 186, 188].

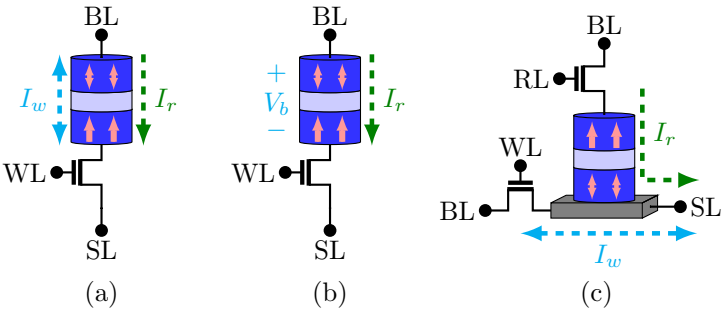


Figure 4.7 – Memories devices: (a) STT-MRAM (b) VCMA-MeRAM (c) SOT-MRAM.

Furthermore, STT-MRAM has intrinsic problems in terms of long latency and high write

power when compared with other mechanisms limiting its application for low power and high-speed working memories [172]. On the other hand, MTJ with VCMA provides magnetization flipping upon a voltage pulse [167, 189]. Using voltage for writing data into an MTJ instead of a charge current can result in a lower energy dissipation [172]. Moreover, the required driving current decreases for the write operation allowing a reduction of the access transistor size [172]. The VCMA effect enables rather fast precessional switching of an MTJ (down to hundreds of picoseconds) by lowing the energy barrier between the two magnetization states of the MTJ [172]. VCMA-MTJ-based memory performs better than STT-MRAM with respect to switching energy, energy consumption, access speed, density, and scalability [166, 172, 190, 191].

The VCMA-MeRAM structure is illustrated in Fig. 4.7b. Just like STT-MRAM, it has 1 MTJ and 1 access transistor in series. Its write operation consists of either maintaining the MTJ state or switching it. An extra circuit is responsible for checking the MTJ state and deciding to switch or maintain the MTJ state.

Another structure is the SOT-MRAM. Its bit-cell design is represented in Fig. 4.7c. As can be seen, its integration density capacity is reduced due to the two access transistors in each bit-cell [185, 187]. In this MTJ-based MRAM, the write path and the read path are different. The write current I_w is generated by the voltage applied between the source line (SL) and the bit line (BL). It is polarized and it switches the magnetization direction of the MTJ free layer. On the other hand, during the read operation, the MTJ state is read according to the magnitude of I_r [192].

Some works suggest that SOT-MRAM requires a lower write time and a lower write energy than STT-MRAM [193–196]. The results presented in [172] show that VCMA-MeRAMs outperform STT-MRAM in terms of area, speed and energy consumption. Table 4.1 reproduces some comparisons presented in [197]. However, it should be highlighted that they are developing technologies. Even if products based in STT MTJ is already in commercialization, intensive research and development are being done in this field especially regarding VCMA and SOT.

Table 4.1 – Comparison between some MTJ-based memories.

	STT-MRAM	**SOT-MRAM**	**VCMA-MeRAM**
Read Time (ns)	1-5	1-5	1-5
Write Time (ns)	5-10	<1	<1
Cell Size (area in F^2)	40-50	50-70	20-30
Bit Density (Gb/cm^2)	1	0.75	2
Read Energy/Bit (fJ)	10-20	10-20	1-5
Write Energy/Bit (fJ)	100-200	<10	<5

Some other memories using multiples mechanisms to write and read MTJ device have also been proposed. NAND-SPIN is an example of MTJ-based memory [185] which uses more than one of the cited switching mechanisms (see Fig. 4.8). The idea is to take advantages of both STT and SOT mechanisms, while aiming at better performance. Compared to SOT-MRAM, NAND-SPIN memory has a better integration density. It occurs because the transistors are shared by several MTJs. On the other hand, compared to STT-MRAM, NAND-SPIN leads to better energy performance [185].

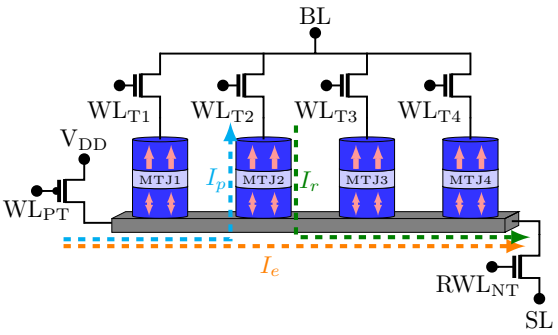


Figure 4.8 – 4-bit NAND-SPIN structure.

Fig. 5.18 illustrates the timing diagram for the write and read operations over MTJ2. As can be noticed, the write operation of the NAND-SPIN has two phases:

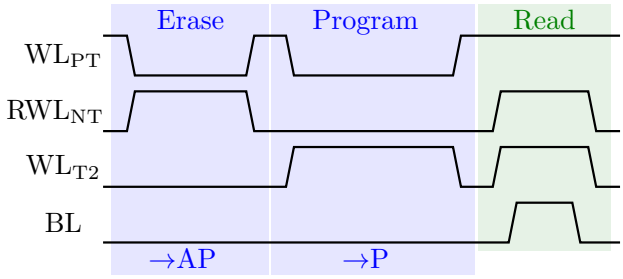


Figure 4.9 – Timing diagram of write and read operations for the NAND-SPIN over MTJ2.

- Erase: this phase initializes the MTJs at their AP states. Moreover, the transistors NT and PT are on, while the access transistors are off. Then, a write current I_e goes through the shared metal strip.
- Program: in this phase, the transistor PT and the corresponding access transistor are on (for the case represented in Fig. 5.18, the corresponding access transistor is T2). Therefore, a current I_p flows through the MTJ from the free layer to the pinned layer switching the MTJ state to P by the STT mechanism.

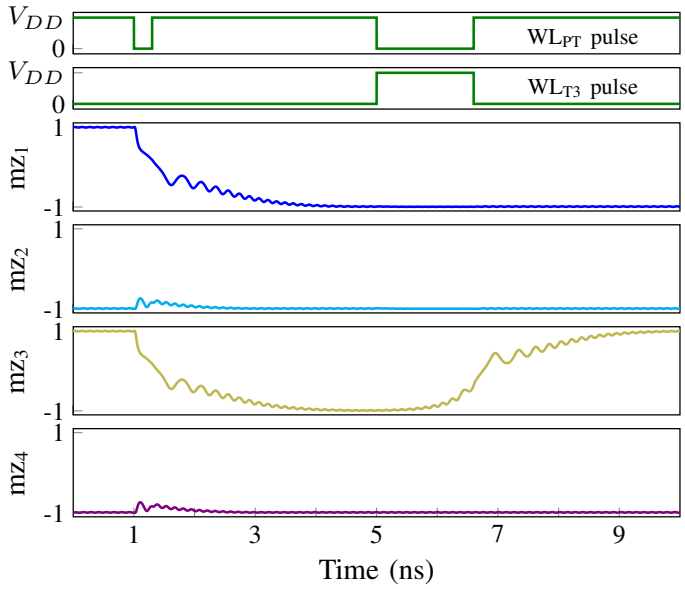


Figure 4.10 – Timing diagram of write operation on MTJ3.

Fig. 4.10 illustrates the write operation on MTJ3. mz_i is the magnetization orientation of MTJi. The corresponding P and AP states are represented by $mz \approx 1$ and $mz \approx -1$, respectively. In this example, the initial states of the MTJs are different. However, after the erase step, all MTJs go to AP state. And after the program step, only MTJ3 changes to P state ($mz \approx 1$).

During the read operation, the access transistor corresponding to the MTJ which will be read and the transistor NT are on. The reading of the MTJ state is made by comparing a reference current with I_r.

Even if MTJ has high tolerance to radiation [198], the MOS access transistors in MTJ-based memory structures may be impacted by radiation. Among other factors, tolerance to radiation is one important and studied field [199–202] when it is necessary to take into account performance and risks of MRAM in the integration process of MOS technology. Indeed, a soft error occurring at the MOS transistor can cause a disturbance on the MTJ switching voltage result in an incorrect value stored in the MeRAM [171].

Radiation hardening techniques with the respect of particle strike on transistors in sense circuit block are presented in [203]. However, the radiation-induced SET should most likely occurs on the access transistors of memory cells since the number of access transistor is much larger than the number of transistors in the sense circuit block [199]. Therefore, it is interesting to analyse how the SET striking time impacts the minimal SET charge that can lead to an error. In special, [171] investigates failure mitigation in VCMA-MTJ based 1T-1MTJ MeRAM bit-cell on 28 nm FDSOI

technology. However, the relationship between the effect of a given SET and its striking time during the writing process is not deeply explored.

In Section 5.2, SET effects on a 28 nm FDSOI VCMA-MTJ based MeRAM bit-cell are investigated. It focuses on write failures due to a SET strike on the access transistors of memory cells. SET effects on STT-MRAM and SOT-MRAM have been reported in [199, 201]. In this thesis, SET effects on a 28 nm FDSOI NAND-SPIN are investigated in Section 5.3.

4.4.2 Logic Gates

Non-volatile logic gates are other MTJ applications which allow for the reduction in area and power consumption.

Fig. 4.11 illustrates the NV-AND / NV-NAND structure. Q and $\overline{Q}$ represent AND and NAND operations, respectively. The truth table is given by Table 4.2 and the logic functions are illustrated by (4.9) and (4.10). This structure gives correct functions for any resistive level of MTJ.

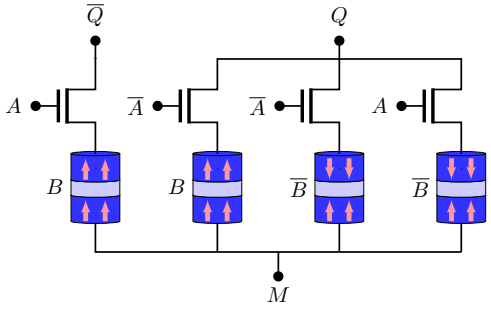


Figure 4.11 – NV-AND / NV-NAND structure.

Table 4.2 – Truth table of AND/NAND.

A	**B**	Q **(AND)**	$\overline{Q}$ **(NAND)**
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

$$Q = AB \tag{4.9}$$

$$\overline{Q} = \overline{AB} = \overline{A} + \overline{B} = \overline{A}B + \overline{AB} + A\overline{B} \tag{4.10}$$

The NV-OR / NV-NOR structure is shown in Fig. 4.12. Q and $\overline{Q}$ represent OR and NOR operations, respectively. The truth table is given by Table 4.3 and the logic functions are illustrate by (4.11) and (4.12).

$$Q = \overline{A}B + A\overline{B} + AB \tag{4.11}$$

$$\overline{Q} = \overline{A}.\overline{B}. \tag{4.12}$$

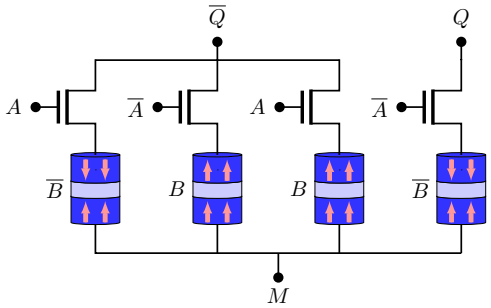


Figure 4.12 – NV-OR / NV-NOR structure.

Table 4.3 – Truth table of OR/NOR.

A	**B**	Q **(OR)**	$\overline{Q}$ **(NOR)**
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

Fig. 4.13 presents the NV-XOR / NV-NXOR structure. Q and $\overline{Q}$ represent XOR and NXOR operations, respectively. The truth table is given by Table 4.4 and the logic functions are illustrate by (4.13) and (4.14).

Table 4.4 – Truth table of XOR/NXOR.

A	**B**	Q **(XOR)**	$\overline{Q}$ **(NXOR)**
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

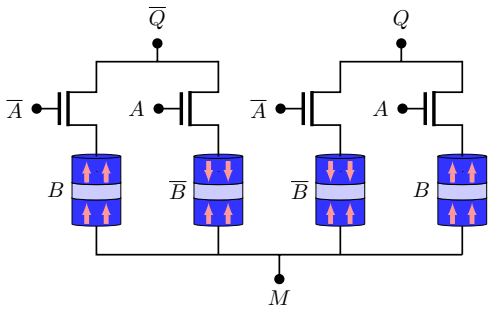


Figure 4.13 – NV-XOR / NV-NXOR structure.

$$Q = \overline{A}B + A\overline{B} \tag{4.13}$$

$$\overline{Q} = \overline{A}.\overline{B} + AB \tag{4.14}$$

In [204], the author proposes some logic gate structures that reduce the number of NMOS transistors and the MTJ when compared with the logic gate structures presented. However, for their proper operation, some NMOS and MTJ settings need to be matched such as their resistance configurations.

4.4.3 Lookup Table (LUT)

One of the main components of FPGAs are Lookup Tables (LUTs) which are usually composed by SRAM cells [205]. Nevertheless, SRAM-based LUTs have limitations such as low logic density, volatility, and high static power [206]. On the other hand, in MTJ-based LUT only the data processing portion is active, whereas other parts are powered off reducing the power consumption and mutual disturbance.

Table 4.5 reproduces the comparison of some MTJ-based LUTs presented in [207]. While the spin-based LUTs presented in [207–211] require a clock, in [206], a 6-input fracturable non-volatile Clockless LUT (C-LUT) using a spin Hall effect (SHE)-based MTJ is proposed for combinational logic operations without needing a clock. This C-LUT eliminates the sense amplifier generally employed and decreases the area compared to the STT-MTJ-based C-LUT.

Table 4.5 – Characteristics of LUT designs.

Design	Write / Read Operation	Features and Challenges
FIMS-LUT [212]	Magnetic Field / TMR	High Speed High Power Consumption High Area Overhead
TAS-LUT [208]	Magnetic Field / TMR	Relatively High Speed High Power Consumption Medium Area Overhead
STT-LUT [207]	STT / TMR	High Speed Low Power Consumption Low Area Overhead
A-LUT [207]	STT / TMR	High Speed Scalable Power Consumption Low Area Overhead

4.4.4 Flip-Flop (FF)

The loss of the data due to power failures and system crashes can be avoided using flip-flop based on non-volatile memory. In [213], one of the first non-volatile flip-flop based on MTJ for FPGA and System On Chip (SoC) circuits is proposed. All the data processed is permanently stored in the Spin-MTJ memory cells making these circuits fully non-volatile. Fig. 4.14 illustrates its full schematic, that is, the sense amplifier with the bidirectional current source.

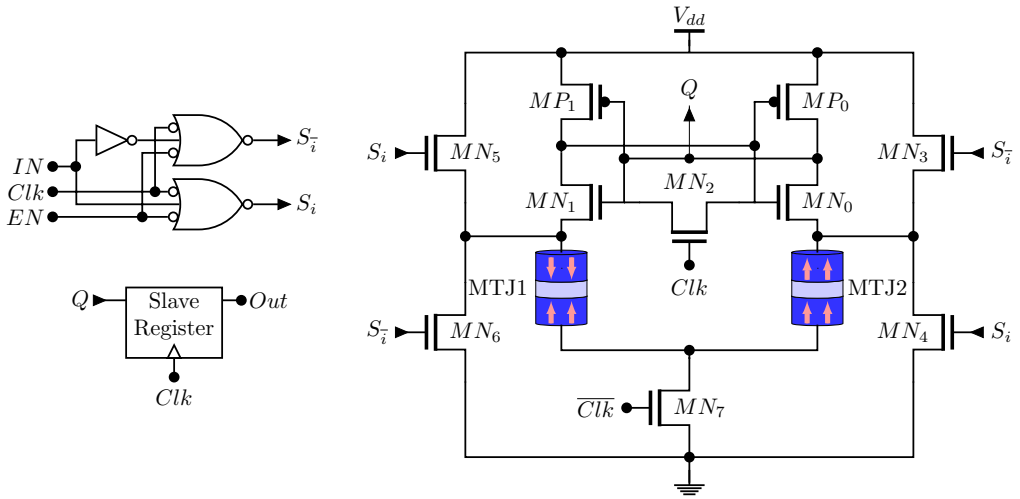


Figure 4.14 – Spin-MTJ based non-volatile Flip-Flop.

The NOR gates control the activation of the transistors MN3, MN4, MN5, MN6. Each time, two of them are active. The signal EN enables the current source thus reducing the power dissi-

pation as the circuit is in static mode. The signal IN writes the pair of MTJs and gives the current direction. MN7 switches between the writing and reading mode. When $Clk = 1$, the slave register keeps the previous data and the input data is stored. On the other hand, when $Clk = 0$, the data stored is read by the sense amplifier and the slave register updates with Q. Other non-volatile flip-flop implementations can be found in [165, 214–216].

4.4.5 Full Adder (FA)

Fig. 4.15 illustrates a single-bit full adder structure. It consists of three inputs (A, B and C_i) and two outputs (S and C_o) given by (4.15) and (4.16). FA is a basic unit to an arithmetic operation in a CPU. Low-power and high-density FA are desirable.

$$S = A \oplus B \oplus C_i = ABC_i + A.\overline{B}.\overline{C_i} + \overline{A}.B.\overline{C_i} + \overline{A}.\overline{B}.C_i \tag{4.15}$$

$$C_o = AB + AC_i + BC_i \tag{4.16}$$

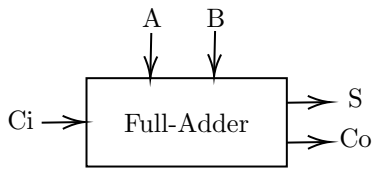


Figure 4.15 – Single-bit full adder (FA) schematic.

Fig. 4.16 presents the SUM and the CARRY sub-circuits proposed with MTJ elements [204]. Several other non-volatile full adders were proposed in [178, 217–219].

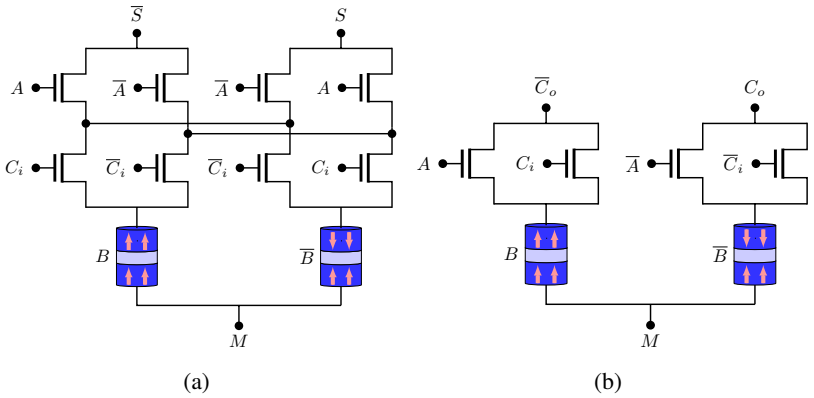


Figure 4.16 – Full adder structure: (a) SUM sub-circuit (b) CARRY sub-circuit.

4.4.6 Comparator

One of most important components of an ADC is the comparator. A low-power and high-speed comparator is essential to build a high-speed ADC. Traditional comparators have several stages of latches and amplifiers [133].

In [134], an MTJ comparator is proposed using one transistor and one spin Hall driven MTJ (see Fig. 4.17). The spin Hall metal (SHM) is in contact with the free layer of the MTJ. Consequently, a spin current transversely can be produced by a charge current flowing in the SHM, hence applying spin-transfer torque on the free layer for switching.

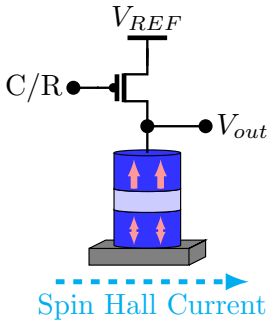


Figure 4.17 – Comparator.

4.4.7 Analog-to-Digital Converter (ADC)

The ADC poses many challenges depending on its application. For example, compact ADCs could be important in parallel data conversion for image processing [220]. Furthermore, with the downscaling of CMOS, the increased static energy consumption has to be avoided. The traditional architecture and operation mode of the ADCs are not suitable for improvement on resolution and power consumption [129, 133]. New technologies and new device design are required to meet the demands of IoT devices, cognitive radios, and other applications in terms of ADC constraints related to sampling rate, area, power consumption, and bandwith [134]. Even if a lot of data converters are based on CMOS [221], in recent years, spintronic devices have been explored in order to save area and reduce the power consumption of the ADCs [134, 180, 220].

In [134], the comparator illustrated in Fig. 4.17 is used to design a 3-bit spin-based ADC (see Fig. 4.18). It can be noticed that 8 comparators are used to provide a 3-bit resolution. The conversion is composed of three phases: reset, conversion and read. Fig. 4.19 shows the timing diagram of ADC operations. During the reset phase, all MTJs go to their AP state. In the conversion phase,

the transistors are on. The voltages on MTJs are different due to the resistors. The VCMA effect in MTJ results in the increase of switching currents from left to right on the comparator, leading to bit levels. A pulse on EN1 samples the input signal and transmits it through the SHM, thus switching some of the MTJs. Finally, in the read phase, the transistors are off and the results are read. This ADC presents improvements in terms of power consumption compared to Flash ADC presented in the literature [134].

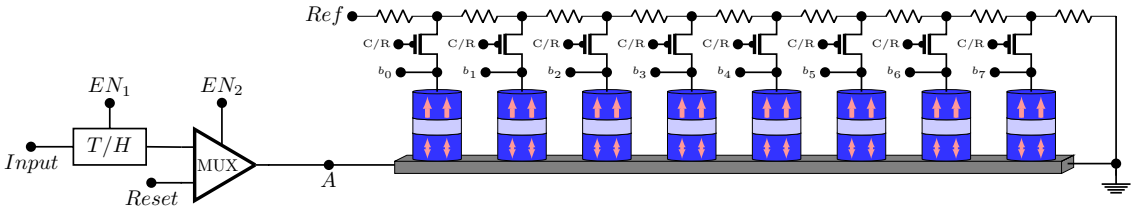


Figure 4.18 – MTJ-based ADC.

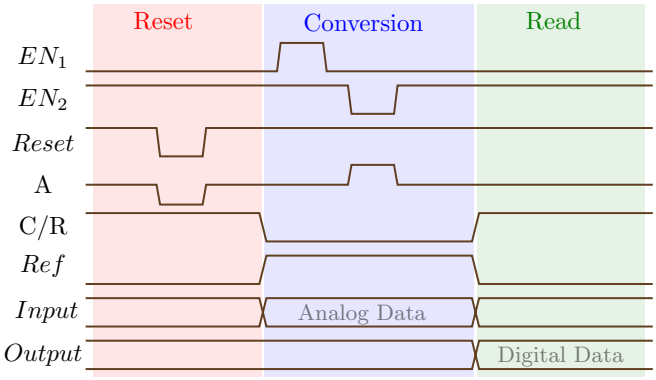


Figure 4.19 – Timing diagram of the ADC operations.

In order to do approximate analog-to-digital conversion at low voltages, a voltage-controlled stochastic switching device based on a superparamagnetic nanomagnet is proposed in [180]. Fig. 4.20 illustrates the schematic of the ADC. It is composed by a counter, two MTJs, and two back-to-back inverters. As shown, the analog input enters in the ME oxide terminal of the MTJ and the counter output gives the digital output. When the input voltage increases, the probability of the MTJ2 in the AP state increases too. When the MTJ2 is in its AP state $C_{in} = 1$, otherwise $C_{in} = 0$. At the positive edge of the clock, the counter counts up if $C_{in} = 1$. Finally, the digital count is translated to a binary code through lookup tables. The results of [180] show that the proposed ADC is suitable for sensors which require low-voltage conversions. Moreover, compact and lower power can be achieved using this proposition.

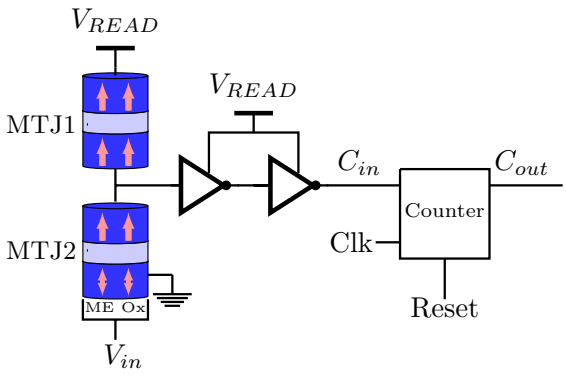


Figure 4.20 – Voltage-controlled stochastic switching device based ADC.

4.4.8 Non-Uniform Clock Generator

Non-uniform sampling (NUS) analog-to-information converters (AIC) generally have a non-uniform clock generator. Normally, a pseudo-random generator Linear Feedback Shift Register (LFSR) integrates an asynchronous clock generator used in non-uniform sampling techniques to randomly select a clock signal. However, this circuit can require a large number of CMOS transistors leading to significant power dissipation and area consumption.

In [222], the authors propose a non-uniform clock using VCMA-MTJs which outperforms the CMOS-based ones in terms of area and power. Fig. 4.21 illustrates the MTJ-based voltage-controlled stochastic oscillator (VCSO) proposed in [222]. The voltage V_B is related to the maximum frequency of an analog input signal. M1, M2 and M3 are responsible for maintaining the voltage on the N1 node independent of the variations of the MTJ resistance. With that, V_B direct defines the voltage across the MTJ controlling its switching rate. In other words, V_B increases if the input signal frequency is high. This will reduce the MTJ energy barrier, resulting in a higher rate of state switching. On the other hand, when the input signal frequency is low, V_B is also low and the MTJ energy barrier continues to be high, reducing the state switching rate. The MTJ's resistance is sensed by the amplifier. After that, a voltage variation on the N3 node related to the MTJ's resistance fluctuation is amplified. Finally, the N4 node is sent to a buffer in which an asynchronous ADC is connected to.

It can be noticed that the amount of transistors is drastically reduced using the VCMA-MTJ instead of the traditional CMOS-based non-uniform clock generators. However, this generator considers the signal's frequency to generate the sampling clock. Therefore, it is not suitable for signals where their frequency is unknown or those with a large bandwidth.

On the other hand, the non-uniform clock generator using MRAM-based stochastic oscillator

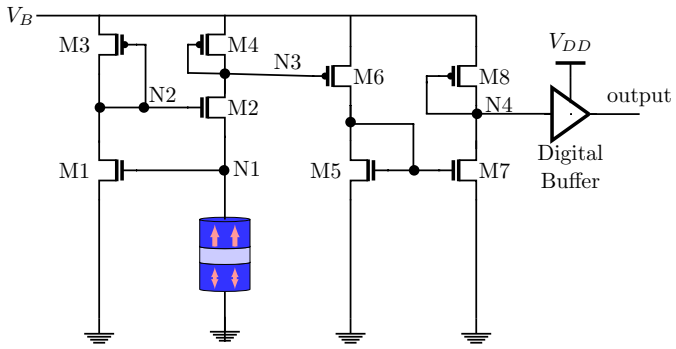


Figure 4.21 – The MTJ-based voltage-controlled stochastic oscillator (VCSO).

devices called Adaptive Quantization Rate (AQR) generator proposed in [223] takes into account the signal's sparsity to generate the sampling clock. Thus, the number of samples is reduced leading to more energy savings.

Fig. 4.22 illustrates the AQR. The stochastic behavior of the VCMA-MTJ provides the non-uniform clock generation capability. The voltage V_{SR} is related to the signal's sparsity that can be known or can be estimated before. Therefore, the V_{SR} applied to the NMOS of the AQR will generate a stochastic bit-stream by the MRAM-based stochastic oscillator device [223]. The Asynchronous Clock (A-Clk) is given by the result of the NAND gate between the actual clock and the output of the D-Flip-Flop (D-FF). It can be noticed that using AQR, large LFSR circuits which has many multiplexers, logic gates, and D-FFs are avoided.

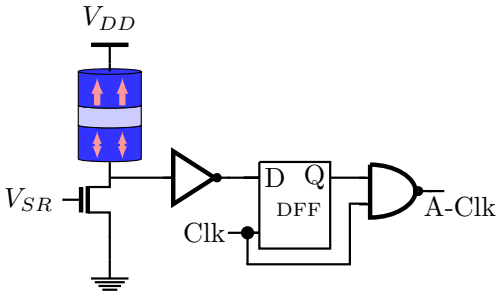


Figure 4.22 – Adaptive Quantization Rate (AQR) generator.

4.4.9 Adaptive Intermittent Quantizer (AIQ)

In [179], the authors propose a spin-based Adaptive Intermittent Quantizer (AIQ) in order to have an adaptive signal sample and quantization. Compressive sensing (CS) theory and spin-based devices are applied for energy-aware acquisition of spectrally sparse signals. Compared to conventional CMOS designs, the use of VCMA-MTJ allows reducing the energy consumption via

an instant on/off operation. It does not require the use of a backing store and it leads to a fast sampling rate (SR), an adaptive quantization resolution (QR), and area reduction.

Fig. 4.23 shows the Q-level AIQ architecture proposed in [179], where Q is the number of QR levels. The quantization levels of the AIQ are given by changes in the energy barrier of the VCMA-MTJs.

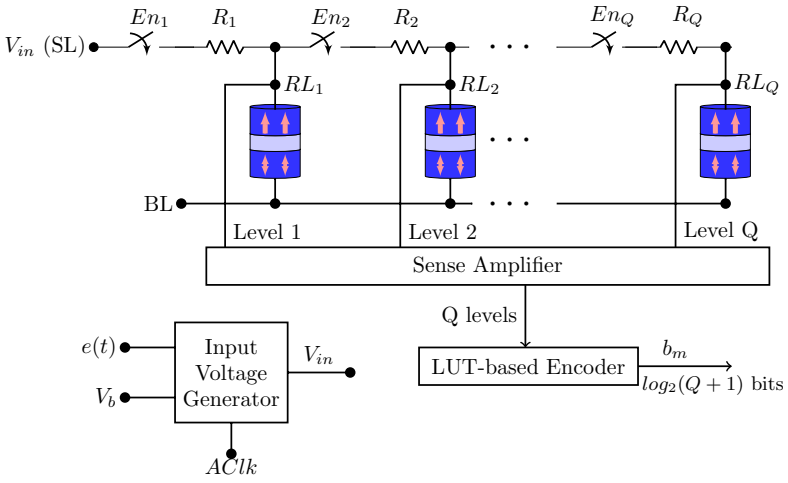


Figure 4.23 – Q-level Adaptive Intermittent Quantizer (AIQ) architecture.

There are three main steps during the AIQ operation [179]:

- Reset: all active VCMA-MTJs go to their parallel state, that is, they are reset to zero. In order to do this, the source line (SL) is set to "0", the bit line (BL) is set to "1", and the read lines (RLs) are in high impedance.
- Sampling: the active VCMA-MTJs are written. In other words, the energy barrier of the active VCMA-MTJs are modified and set by the bias voltage V_b applied across the active VCMA-MTJs followed by the analog input $e(t)$. The sampling rate of $e(t)$ is controlled by the Adaptive Clock (AClk). In addition, SL is set to V_{in}, BL is set to "0", and RLs are in high impedance.
- Read or Sensing: in this step, the sense amplifier reads the data stored in each VCMA-MTJ. SL is in high impedance and BL is set to "0".

The switches and resistors presented in Fig. 4.23 are responsible for the adaptive quantization resolution levels. With the resistors, different MTJs have different V_b. Thus, while some MTJs require lower input voltages to turn on; others switch their state only with higher input voltages. The switches allow for the optimization of the QR by turning off the MTJs which are not used.

In [179], the authors used 255 VCMA-MTJs to realize a range of quantization resolutions from 1-bit to 8-bit ADC operations.

4.4.10 Sensors

With the increase of transistor scaling and power density, the temperature monitoring and the analysis of heating effects are very important, leading temperature sensors to become a relevant component in SoC. MTJ can also be used as a sensor resulting in high conversion, compact, and low energy consumption devices. In [224], an MTJ-based temperature sensor is proposed (see Fig. 4.24). The SOT switching mechanism is used to stochastically switch the MTJ state according to the operating temperature in the presence of thermal noise. The MTJ probabilistic switching characteristics of the MTJ can be given by the Landau-Lifshitz-Gilbert (LLG) equation [224]:

$$\frac{d\hat{m}}{dt} = -\gamma(\hat{m} \times H_{eff}) + \alpha(\hat{m} \times \frac{d\hat{m}}{dt}) + \frac{1}{qN_s}(\hat{m} \times I_s \times \hat{m}), \tag{4.17}$$

where $\hat{m}$ is the vector of free layer magnetization, $\gamma = \frac{2\mu_B\mu_0}{h}$ is the gyromagnetic ratio for electron, μ_B is Bohr magneton, H_{eff} is the effective magnetic field including the shape anisotropy field for elliptic disks, α is Gilbert's damping ratio, $N_s = \frac{M_s V}{\mu_B}$ is the number of spins in a free layer of volume V, M_s is saturation magnetization, and I_s is the spin current generated by the heavy metal layer.

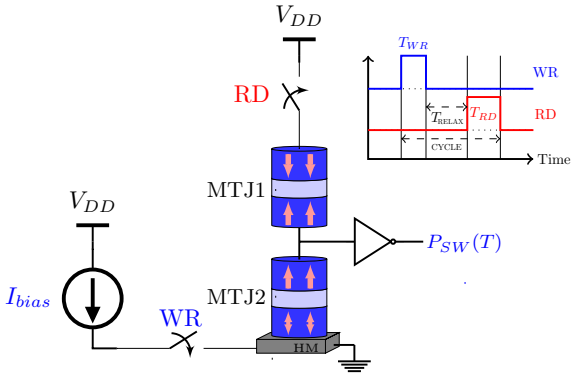


Figure 4.24 – The MTJ-based temperature sensor.

As can be seen in Fig. 4.24, the sensor MTJ (MTJ2) and the reference MTJ (MTJ1 - fixed at its AP state) form a voltage divider circuit. The switching probability ($P_{SW}(T)$) is given by the inverter output. The control signals RD and WR active the read and write current paths respectively. In the write operation, WR is on and then the I_{bias} current probabilistically switches the

magnet depending on the temperature. On the other hand, during the read operation, *RD* is on and the sensor MTJ final state is determined. Between the write and the read operations, there is a "relaxation" period (T_{RELAX}) in order to stabilize the magnetization directions after the write operation. This MTJ-based temperature sensor achieves better results than state-of-the-art CMOS temperature sensors in terms of throughput and energy consumption [224].

Regarding a frequency sensor, [225] proposes an MTJ-based microwave detector that can be used, for example, as a spectrum analyzer. The ferromagnetic resonance in MTJs can determine the microwave frequency. With this, the mixer circuit is not required in conventional RF diode detection.

This section addressed several MTJ applications. However, there are still many other domains where MTJ can be applied. Using, for example, its stochastic behavior, MTJ can also be used as a memristive probabilistic device and to implement the activation function [226] for Spiking Neural Networks (SNNs). As SNN intends to mimic the computational efficiency of the human brain, non-volatile resistive memories can be found in the literature to mimic a stochastic one-bit synapse [226, 227]. The MTJ conductance is used to modulate the voltage spike produced by a pre-neuron resulting in a post-synaptic current.

This chapter dealt with concepts, models, and devices that are used to obtain the results presented in Chapter 5. Indeed, the SET model is used to analyse the SET effects on a dynamic comparator on 28 nm FDSOI CMOS technology (see Section 5.1). In addition, MTJ-based devices under VCMA effects (see Section 5.2) and SOT/STT effects (see Section 5.3) have their vulnerability to SET discussed. Moreover, the study of the MTJ applications presented in the literature led to the proposition of an MTJ-based ADC (see Section 5.4).

Chapter 5

Hardware Analysis and Propositions

This chapter presents the hardware analysis and propositions made throughout this thesis. The SET effects on a dynamic comparator on 28 nm FDSOI CMOS technology, on a voltage-controlled magnetic anisotropy MeRAM bit-cell, and on a NAND-Like spintronic memory are analysed in Sections 5.1, 5.2, and 5.3, respectively. Then, an MTJ-based ADC is proposed in Section 5.4. Finally, Section 5.5 presents an application case where an AIC is used to wideband spectrum sensing.

5.1 Analysis of the SET Effects on a Dynamic Comparator on 28 nm FDSOI CMOS Technology

The comparator is a pivotal component of an ADC. Its accuracy, speed, and power consumption determine the conversion efficiency. Therefore, high quality-demand, low power or critical applications as aerospace and radar sensors require highly effective comparators [228]. According to the comparator operation, that is, if it is controlled by clock signal or not, a comparator can be classified into dynamic or static [229]. In order to overcome low-speed and high-power consumption issues generally dynamic comparators are used instead of static comparators [230].

Another aspect of comparators in research is related to nanometer dimensions of devices, which make circuits become more susceptible to temporary faults. SET effects of a dynamic comparator were evaluated in [121] and [122] for 90 nm and 65 nm CMOS bulk technologies, respectively. The results show that circuit vulnerability strongly depends on technology, topology, and individual transistor currents.

As many others, the works above do not deeply explore the relationship between the effect of

a given SET and the striking time or the transistor concerned by that SET. However, it could be interesting to assess how striking time impacts the minimal SET's charge needed to change the comparator's output. Likewise, information either SET in different transistors/locations leads to different impacts on the comparator's output would enable implementation of effective reliability improvement strategies.

In this thesis, SET effects on a dynamic comparator in 28 nm FDSOI CMOS technology are investigated. The sensitivity of the circuit is simulated combined with the polarity of differential inputs and the working phases of the comparator. Moreover, the body-bias and the transistor channel modulation impact were analysed. These results were published in [147].

5.1.1 Comparator Design

Fig. 5.1 shows the schematic diagram of the comparator considered in this thesis [120]. This is the StrongArm comparator, which is extensively used in ADCs [121–123]. This circuit produces an output V_{op} (and this opposite V_{on}) which is according to the difference between the input voltages (V_{ip} and V_{in}). Its working principle includes two phases:

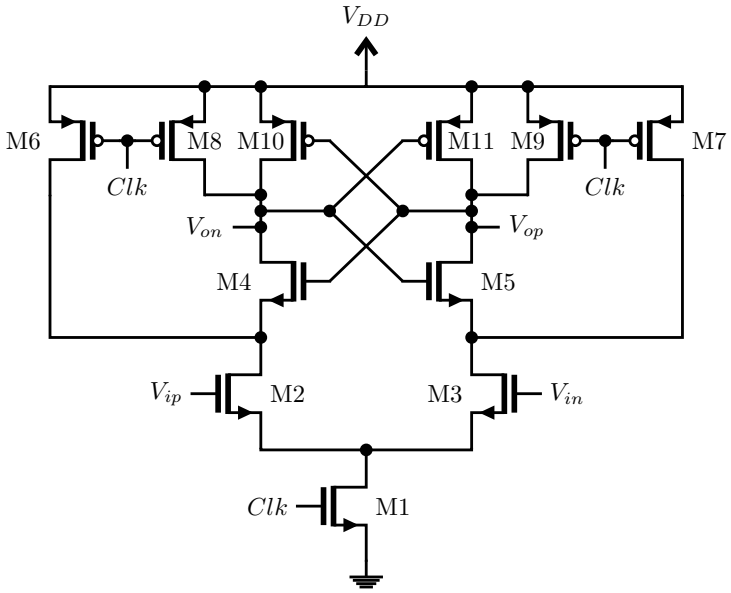


Figure 5.1 – StrongArm comparator.

- Reset phase: when $Clk = 0\,\text{V}$, $M1$ is off, while $M6$, $M7$, $M8$, and $M9$ are on. V_{op} and V_{on} are pre-charged to V_{DD} by $M9$ and $M8$.
- Comparison phase: when $Clk = V_{DD}$, $M1$ is on, while $M6$, $M7$, $M8$, and $M9$ are off. For

$V_{ip} > V_{in}$, V_{on} decreases until $V_{on} = 0\,\text{V}$ and $V_{op} = V_{DD}$. Otherwise, when $V_{in} > V_{ip}$, V_{op} decreases until $V_{op} = 0\,\text{V}$ and $V_{on} = V_{DD}$.

5.1.2 Simulation Setup

The SET model used in these simulations is given by (4.3), where $\tau_1 = 20\,\text{ps}$ and $\tau_2 = 1\,\text{ps}$. Low threshold voltage (LVT) transistors using n-well below nFET and p-well below pFET devices were used. This flipped-well configuration was used to improve the power-delay performance [231].

Only one SET is considered each time. Critical charge Q_c is denoted as the minimum charge in a transistor that leads to incorrect output values. The SET charge in each transistor was set to vary from 0 C to 20 fC, and the striking time was varied during one period of clock.

The circuit outputs are considered correct, in the falling clock edge, if:

- $V_{op} - V_{on} > V_{DD}/2$ when $V_{ip} > V_{in}$;
- $V_{on} - V_{op} > V_{DD}/2$ when $V_{in} > V_{ip}$.

Fig. 5.2 illustrates the output V_{op} for different SET charge values considering a SET which occurs at the rising clock edge [147]. It can be noticed that depending on the SET charge applied, the output can flip.

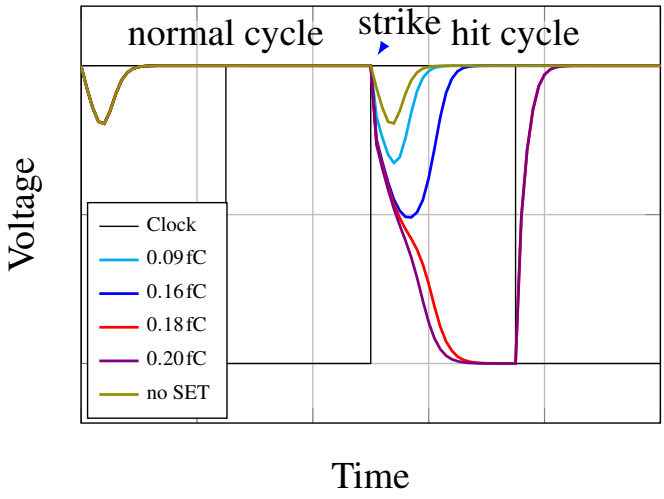


Figure 5.2 – Comparator output V_{op} when a SET occurs at the rising clock edge.

5.1.3 Simulation Results

The SET impact of the comparator is analysed for two setups. In the simulations, the input voltages of the circuit were set as $V_{cm} + \Delta V_{in}/2$ and $V_{cm} - \Delta V_{in}/2$, where V_{cm} is the common-mode voltage

and ΔV_{in} is the differential-mode voltage.

5.1.3.1 Setup 1

In Setup 1, each transistor is set to width $W = 80\,\text{nm}$ and length L_i, where L_i varies according to the simulation. The clock frequency is $f_{clock} = 200\,\text{MHz}$, $V_{DD} = 1.0\,\text{V}$, $V_{cm} = 0.6\,\text{V}$, and $\Delta V_{in} = 100\,\text{mV}$. Back gates of transistors are connected to 0 V.

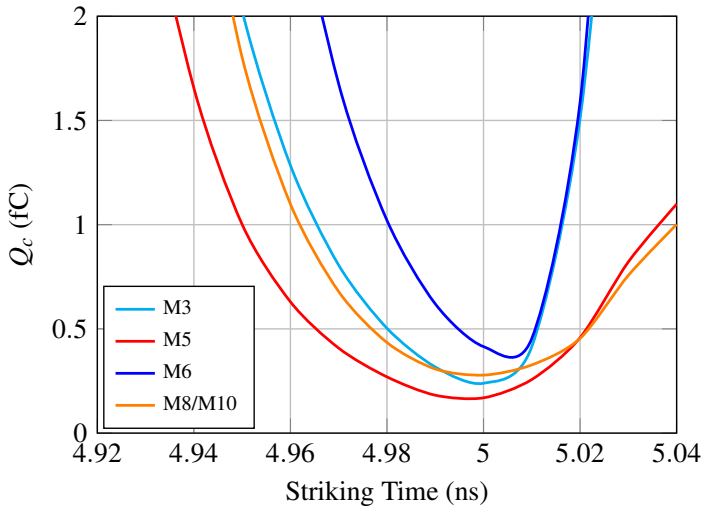


Figure 5.3 – Value of Q_c (fC) for Setup 1 and $V_{ip} > V_{in}$.

The striking time was varied from 2.5 ns (first falling clock edge) to 7.5 ns (second falling clock edge). Fig. 5.3 shows the Q_c value for the transistors that have Q_c lower than 2 fC when $V_{ip} > V_{in}$ and $L_i = 30\,\text{nm}$ [147].

The SET robustness is evaluated varying the L_i value. Using poly biasing, i.e., modulation of body gate length, it can achieve leakage power reduction at the expense of lower speed [177]. The length gate value was increased up to 16 nm (i.e., L_i varies until 46 nm). It was observed that the most sensitive transistors are the same than in the simulation with $L_i = 30\,\text{nm}$. Table 5.1 presents the minimum Q_c value for each transistor in all simulations performed. The results show that depending on the transistor location/role reached by the SET, the SET robustness of the circuit can increase or decrease. For example, with $L_i = 46\,\text{nm}$, if a SET occurs in the M3, the circuit is less robust than if $L_i = 30\,\text{nm}$. Otherwise, if M8 is reached by the SET, the comparator is more robust with $L_i = 46\,\text{nm}$. In addition, it can be seen that increasing the L_i value allows the comparator to become more robust, that is, the minimum Q_c value increases by 4.3 % compared to the minimum Q_c when $L_i = 30\,\text{nm}$ [147].

Table 5.1 – Minimum Q_c (fC) values for Setup 1.

$V_{ip} > V_{in}$	M3	M5	M6	M8	M10
$V_{in} > V_{ip}$	M2	M4	M7	M9	M11
$L_i = 30\,\text{nm}$	0.238	**0.163**	0.375	0.277	0.277
$L_i = 34\,\text{nm}$	0.237	**0.168**	0.414	0.297	0.297
$L_i = 40\,\text{nm}$	0.228	**0.170**	0.439	0.327	0.327
$L_i = 46\,\text{nm}$	0.227	**0.170**	0.453	0.347	0.347

The simulations results point out that the comparator presents different behaviours according to the transistor reached by the SET and the striking time. Moreover, it can be noticed similarity of some results due to the symmetry in the comparator structure. It can be seen that $M4$ and $M5$ are the most critical transistors, as they present the lowest Q_c value [147].

5.1.3.2 Setup 2

Similarly to [122], Setup 2 considers $f_{clock} = 2.5\,\text{GHz}$, $V_{cm} = 0.73\,\text{V}$, and $\Delta V_{in} = 300\,\text{mV}$. The transistors sizes have been adapted to 28 nm FDSOI CMOS technology, as shown in Table 5.2.

Table 5.2 – Size of the transistors in Setup 2.

Transistors	W (nm)	L (nm)
M1, M8, M9	1500	30
M6, M7	1000	30
M4, M5, M10, M11	1500	30
M2, M3	2000	40

Fig. 5.4 illustrates the back-bias of FDSOI device used in this Setup. In the Flip-well configuration (Case 1), the NMOS and the PMOS body are connected to 0 V. Otherwise, the NMOS body is connected to V_{DD} and PMOS body is connected to 0 V in Flip-well with back-bias configuration (Case 2).

The striking time is varied from 200 ps (first falling clock edge) to 600 ps (second falling clock edge). Fig. 5.5 shows the Q_c value for the transistors with Q_c lower than 20 fC when $V_{ip} > V_{in}$. In Fig. 5.5, the continuous lines represent the simulations of Case 1, while the broken lines denote the simulations of Case 2 [147].

Table 5.3 shows the minimum Q_c value for each transistor. In Case 1, if a SET occurs in M8 or M10, the SET charge must be greater than 20 fC ($Q_c > 20\,\text{fC}$) for an error to occur at the comparator's output. Otherwise, in Case 2, if a SET occurs in M8 or M10 with a charge more than 14.9 fC at the critical striking time, there will be incorrect output values. It can be noticed that for

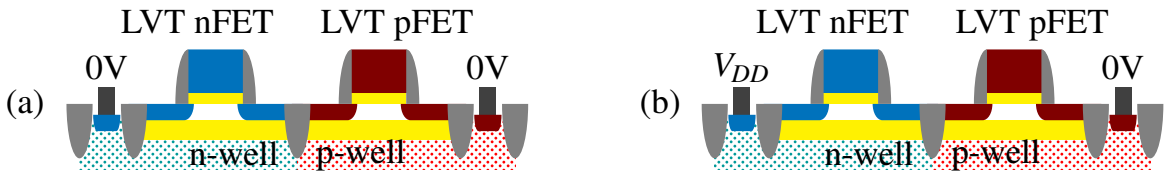


Figure 5.4 – FDSOI device configurations: (a) Flip-well (b) Flip-well with back-bias.

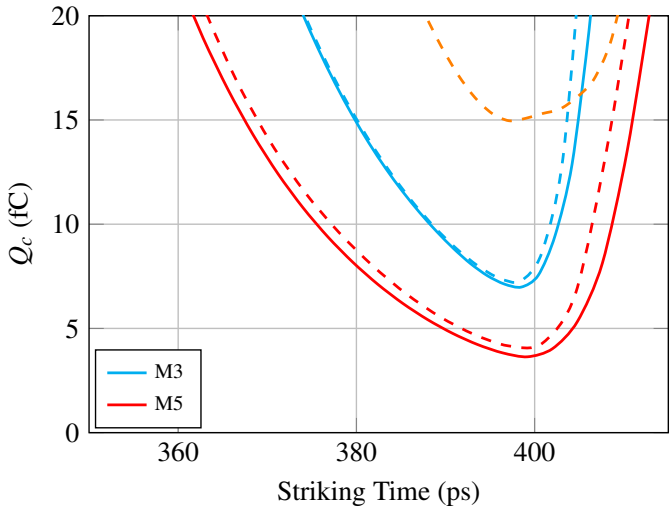


Figure 5.5 – Value of Q_c (fC) for Setup 2 in different body-bias.

the NMOS transistors (M2, M3, M4, and M5), the Case 2 configuration improves the comparator SET robustness which was indicated by the increase of the Q_c value when a SET occurs in a NMOS. At the critical striking time, the flip-well with back-bias configuration increases Q_c by 12.4 % if the M5 is reached by the strike. On the other hand, when a SET occurs in a PMOS transistor (M8, M9, M10, and M11), the circuit is more robust with Case 1 configuration [147].

Table 5.3 – Minimum Q_c (fC) value for Setup 2.

$V_{ip} > V_{in}$	M3	M5	M8	M10
$V_{in} > V_{ip}$	M2	M4	M9	M11
Case 1	6.9	**3.6**	> 20	> 20
Case 2	7.2	**4.0**	14.9	14.9

Furthermore, it can be seen that the critical transistors are the same in the two cases. The transistors with the minimum Q_c values at the critical striking time are M4 and M5, that is, they are the most critical transistors of the circuit.

The results show that the robustness of the circuit against SET depends on the striking time and the transistor involved by the strike. In addition, the Q_c at the critical striking moment has

relevant variation when different body-bias are applied to the transistors.

In summary, it can be said that the analysis of the SET impact allows to check if the circuit complies with the application requirements. If the circuit is not SET robust enough, Q_c results enable ranking transistors and therefore an appropriate redesign of the circuit [147].

5.2 Voltage-Controlled Magnetic Anisotropy MeRAM Bit-Cell over Event Transient Effects

Magnetic tunnel junction (MTJ) with voltage-controlled magnetic anisotropy (VCMA) effect has been introduced to achieve robust non-volatile writing control with an electric field or a switching voltage. The reliability of VCMA-MTJ-based magnetoelectric random access memory (MeRAM) can be impacted by environmental disturbances because a radiation strike on the access transistor could introduce write and read failures in 1T-1MTJ MeRAM bit-cell.

In this section, SET effects on a VCMA-MTJ-based MeRAM in 28 nm FDSOI CMOS technology are investigated. These results were published in [200].

5.2.1 VCMA-MTJ based MeRAM Bit-cell

A 28 nm FDSOI CMOS design-kit is utilized to implement and simulate the VCMA-MTJ based MeRAM bit-cell illustrated in Fig. 4.7(b). The performance of the memory device can be influenced by a SET occurrence on the access transistor leading to write failures [171, 232]. Write failures occur when the MTJ in the bit-cell does not appropriately switch between parallel and anti-parallel states. In other words, because of the SET, the MTJ does not switch when it has to or the MTJ switches when it should not to do.

In order to analyse the vulnerability of the bit-cell against SET, this thesis considers low threshold voltage (LVT) transistor as access transistor with width $W = 80\,\text{nm}$. The flipped-well configuration is usually used to improve the power-delay performance [231].

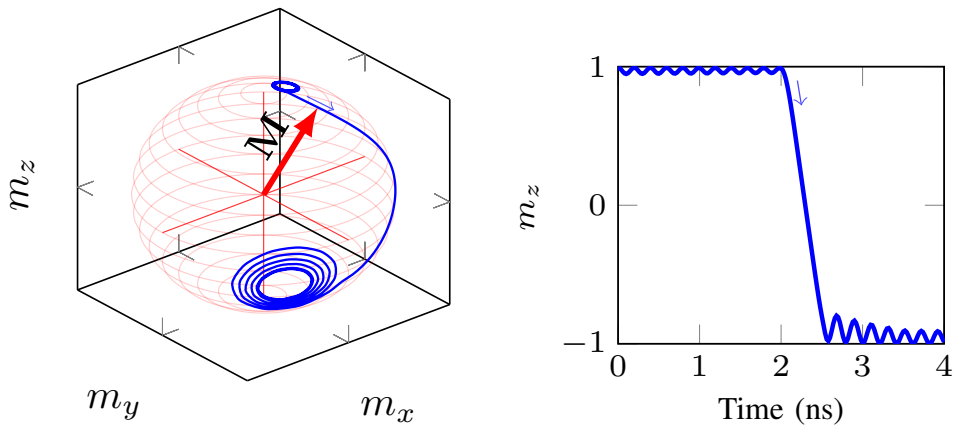
Table 5.5 lists the design parameters of VCMA-MTJ compact model [233]. The VCMA has two stable opposite states, parallel and anti-parallel, represented by $m_z \approx 1$ and $m_z \approx -1$, respectively.

Although normally the write pulse is applied in the BL, the authors in [234] showed that to apply the write pulse in the WL leads to a better pulse shape compared to when the write pulse is applied in the BL of the MeRAM. Moreover, it improves the switching probability and

Table 5.4 – Design specification of VCMA-MTJ compact model.

Parameter	Description	Value
T	Temperature	300 K
TMR(0)	TMR ratio at $V_b = 0$	100%
R_P, R_{AP}	MTJ resistance	100 kΩ, 200 kΩ
$\Delta(0)$	Thermal stability at $V_b = 0$	40
V_h	1/2 TMR Bias voltage	0.5 V
T_{ox}	MgO oxide thickness	1.4 nm
T_{fl}	Free layer thickness	1.1 nm
d	MTJ diameter	50 nm
α	Damping factor	0.02
K_i	Interfacial PMA	$0.32 \times 10^{-3}\ J/m^2$
M_s	Saturation magnetization	$0.625 \times 10^{6}\ A/m$
ξ	VCMA coefficient	60 fJ/V·m
H_x	External magnetic field	400 Oe

minimizes the area overhead (e.g., driver size) [234]. Fig. 5.6 gives an example of the precession of magnetization under the influence of a voltage between the MTJ's terminals. Due to the fluctuation of magnetization, the initial state of the free layer magnetic moment (represented by the angle between M and m_z) is different at each measurement. This leads to the stochastic reversal of free layer magnetization. As can be seen in Fig. 5.6, M had m_z value approximately equals to 1 before a write pulse occurs in WL (at 2 ns). The pulse lasted 0.5 ns and it was sufficient to change the M position from $m_z \approx 1$ to $m_z \approx -1$.



(a) (b)

Figure 5.6 – The precession of magnetization under the influence of a voltage between the MTJ's terminals: (a) The reversal process of magnetic moment. (b) Time dependence of m_z.

In this thesis, the voltage pulse delay and the voltage pulse duration were analysed to guarantee

a successful writing considering $V_{DD} = V_{BL} - V_{SL} = 1.1\,\text{V}$.

One of the intrinsic characteristics of the MTJ is a small variation of its state related to the fluctuation of the magnetization of the free layer magnetic moment. The circuit in which the MTJ is inserted could not be as fast as these variations. Therefore, a SET robustness analysis must take into account this peculiar behavior of the MTJ magnetic state.

Fig. 5.7 illustrates this variation of state and its effects on possible switching failures [200]. It can be seen that a successful writing (represented by the "successful switch region" in Fig. 5.7) depends on the voltage pulse amplitude, duration, and the instant in which the voltage pulse is applied.

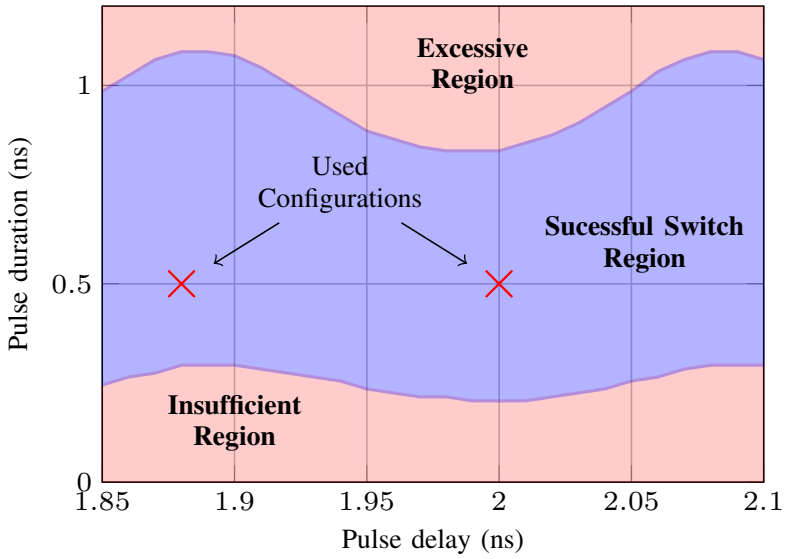


Figure 5.7 – Variation of write pulse on MTJ, from P state to AP state. The pink area denotes the switching failure.

Voltage pulses with various durations are studied to explore the switching characteristics. Fig. 5.8 presents the time dependence of m_z when a pulse with delay of 2 ns is applied with different voltage pulse durations [200]. From Figs. 5.7 and 5.8, it can be noticed that the voltage pulse has to have a minimum duration to lead to a successful switch. If the voltage pulse duration is relatively short (represented by the "insufficient region" in Fig. 5.7 and the orange curve in Fig. 5.8), m_z can not switch and m_z backs to the initial stage. On the other hand, if it has a longer pulse duration (represented by the "excessive region" in Fig. 5.7 and the red curve in Fig. 5.8), initially m_z changes to the other state but then it switches back to the initial state, so at the end, the desirable switch will not occur. Therefore, to achieve deterministic MTJ switching, a precise control of the voltage pulse duration is required, that is, a shorter or longer voltage pulse duration

may cause a switching failure.

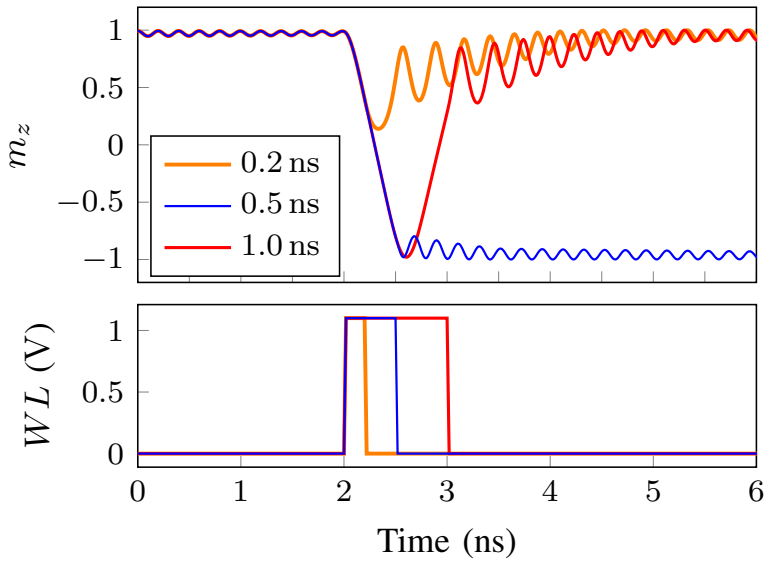


Figure 5.8 – Magnetization dynamics of the free layer from P state to AP state switching with different pulse durations.

In this thesis, the voltage pulse amplitude and duration were properly selected based on the results presented in Fig. 5.7. Two different voltage pulses for writing are considered in the SET effects analysis. They were chosen taking into account the variations of the MTJ magnetic state so that possible effects related to the small difference in the synchronism between the write pulse delay and MTJ can be analysed. These chosen configurations are pointed out in Fig. 5.7. In both cases, the voltage pulse duration is 0.5 ns.

5.2.2 SET Analysis

For writing each bit in an 1T-1MTJ cell, a voltage is applied through the MTJ and the free layer will change its state (P $\rightarrow$ AP or AP $\rightarrow$ P). The resulted voltage bias from BL to SL must be carefully considered to ensure the correctness of the operations.

Critical charge Q_c is denoted here as the minimum SET charge that leads to an undesirable MTJ state switching when it reaches the access transistor. It can occur due to an insufficient or an excessive excitation of MTJ magnetic vector **M** in the free layer with the objective of changing the stable state.

In this thesis, it is considered that a SET reaches the access transistor of the bit-cell. In other words, a current pulse modeling SET is applied to the access transistor at different times with different charges to analyse which charge value would lead to an error in the MTJ stored state.

Simulations were carried out to identify the sensitivity of the circuit against SET considering three cases.

5.2.2.1 Case 1: without write pulse

It is considered that there is no write pulse. In other words, Q_c is the minimum SET charge that leads to an undesirable switching of MTJ state without a write request has been made. It is also equivalent to a writing in an adjacent bit-cell. For Case 1, the write failure is only due to SET.

Fig. 5.9 shows the Q_c value for the scenario that there is no write pulse, that is, there is no intention of writing in this bit-cell [200]. It can be seen that if a SET charge greater than 1.9 fC reaches the access transistor, an undesirable switch $AP \rightarrow P$ can occur. On the other hand, if the MTJ is in the P state, it will be necessary a SET charge at least greater than 2.2 fC to lead to an undesirable switch $P \rightarrow AP$. Fig. 5.9 shows how Q_c depends on the strike time moment. In the worst case, $Q_c = 1.9$ fC.

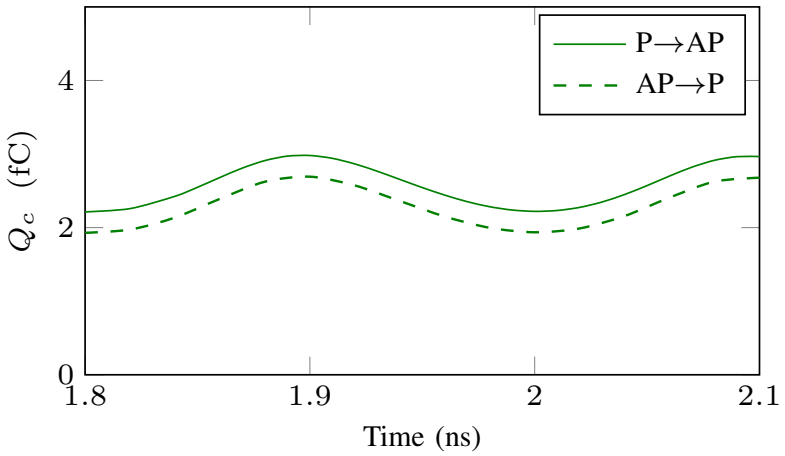


Figure 5.9 – Value of Q_c when there is no write pulse.

5.2.2.2 Case 2: with write pulse

The minimum charge Q_c is analysed when there is an intention of writing in this bit-cell, that is, when there is a write pulse. In this scenario, a write failure occurs when there is no switch after the writing process. In this case, the write failure is due to SET combined with the voltage pulse.

Fig. 5.10 shows the time dependence of m_z when a SET with $Q_{inj} = 1$ fC reaches the access transistor at 2.2 ns (blue curve) and 2.6 ns (red curve) for a voltage pulse delay of 1.88 ns [200]. It can be noticed that when the SET occurs after the end of the voltage pulse (red curve), there is no

switch, which means a writing error occurrence. Comparing with Fig. 5.9, Fig. 5.10 shows that the circuit is less SET robust when there is a write pulse [200]. In other words, when there is a write pulse, a low SET charge ($Q_{inj} = 1\,\text{fC}$) can lead to a write failure while in the case in which there is no write pulse, a $Q_{inj} > 1.9\,\text{fC}$ (see Fig. 5.9) is necessary to lead to a write failure.

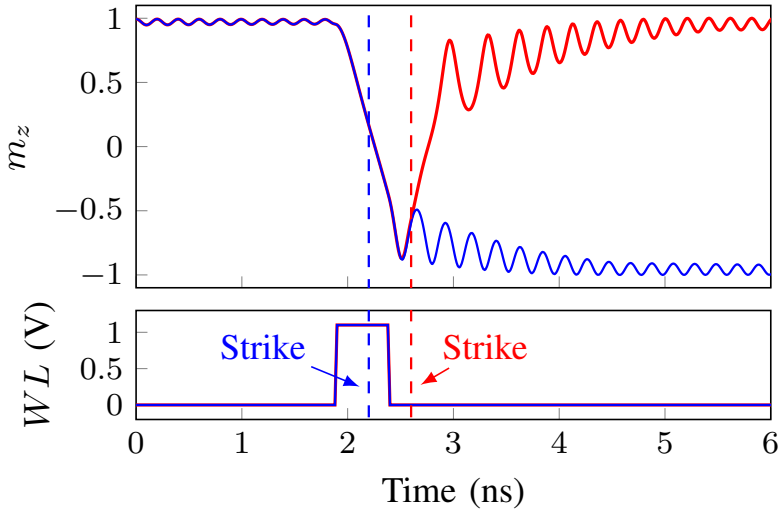


Figure 5.10 – The time dependence of m_z when a SET with $Q_{inj} = 1\,\text{fC}$ reaches the access transistor at 2.2 ns and 2.6 ns.

As can be seen in Fig. 5.10, the striking time influences the circuit behavior. In order to analyse this influence, the SET charge in the access transistor was varied to find the critical charge Q_c required to lead to an error at different striking times.

Fig. 5.11 shows the Q_c value as a function of the striking time when the voltage pulse delay is 1.88 ns (red curves) and 2 ns (blue curves) [200]. In both cases, the voltage pulse duration is 0.5 ns. In Figs. 5.11 and 5.12, the continuous lines represent the simulations of the transition $P \rightarrow AP$, while the dashed lines denote the simulations of the transition $AP \rightarrow P$.

From Fig. 5.11, it can be noticed that when the SET reaches the access transistor during the pulse duration, it is necessary a higher Q_c value to have an unsuccessful switch. This shows the robustness of the MeRAM write circuit to SET during the write pulse. On the other hand, if the SET reaches the access transistor before or after the write pulse, a much lower Q_c value can lead to an unsuccessful switch (write failure).

Figs. 5.12a and 5.12b show the Q_c value for the time just before the beginning of the voltage pulse and just after the end of the voltage pulse, respectively [200]. The referenced times (0 ps) represent the beginning of the voltage pulse in Fig. 5.12a and the end of the pulse in the Fig. 5.12b.

The results show how the robustness of the bit-cell against SET is highly dependent on the

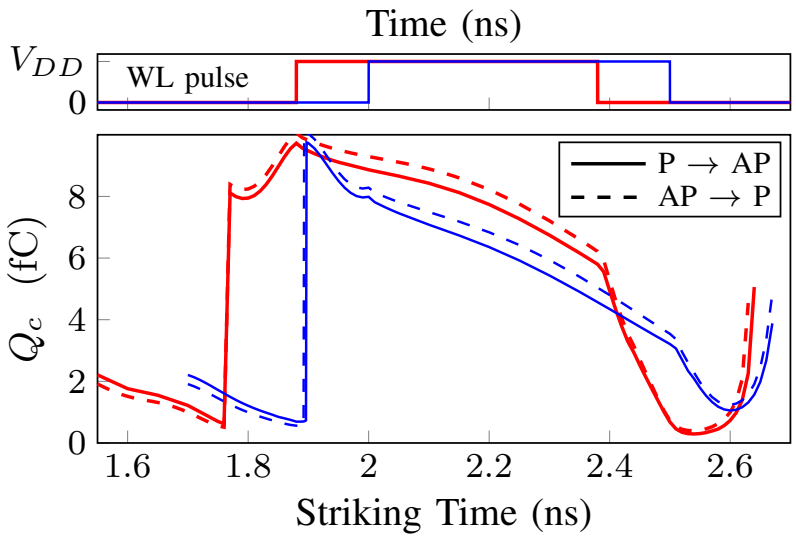


Figure 5.11 – Value of Q_c for a voltage pulse delay of 1.88 ns and 2 ns.

striking time. Moreover, the writing process is less robust against SET effects when the SET occurs near to the voltage pulse occurrence (before or after the write pulse) [200]. Considering these simulations, when a SET occurs before the write pulse, the worst critical charge was $Q_c \approx 0.5$ fC for both configurations (see Fig. 5.12a). It is basically four times lower than the Q_c required when there is no write pulse (see Fig. 5.9). On the other hand, for a SET occurrence after the write pulse, while in one case $Q_c = 1.05$ fC (blue curve) can lead to a write failure, values as low as $Q_c = 0.29$ fC (red curve) can result in a writing error in the other case, showing a significant decrease of the circuit robustness against SET (see Fig. 5.12).

The results show that even if it has some advantages to apply the pulse in BL [234], it is important that the other writing lines (BL and SL) are not activated much before the beginning of the WL pulse (worst Q_c at 100 ps before - see Fig. 5.12a). In addition, BL and SL should be deactivated as soon as possible, that is, not much after of the end of the WL pulse (worst Q_c at just over 150 ps - see Fig. 5.12b). Those measures can contribute decisively to increase the robustness of the write operation in the bit-cell against SET. In other words, even if a SET reaches the access transistor, a current coming from a SET that crosses the MTJ would not be boosted by the difference of potential between BL and SL [200].

5.2.2.3 Case 3: modulation of the transistor channel width (W)

The SET robustness was analysed varying the width W of the access transistor for voltage pulses with delays of 1.88 ns and 2 ns as shown in Fig. 5.13 [200]. The worst Q_c values that lead to a

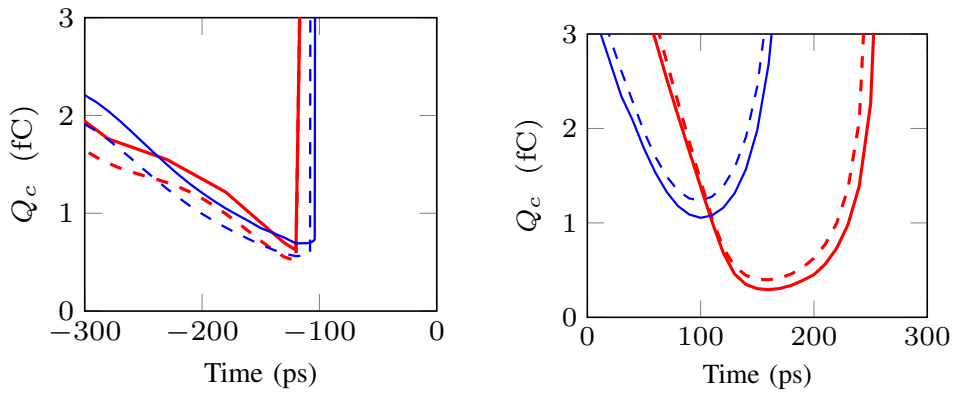


Figure 5.12 – Q_c values related to: (a) The beginning of the voltage pulse with delays of 1.88 ns and 2 ns. (b) The end of the voltage pulse with delays of 1.88 ns and 2 ns.

write failure considering a SET before and after the write pulse for the transitions $P \rightarrow AP$ and $AP \rightarrow P$ are presented in Fig. 5.13. It can be seen that with the increase of the W value, the circuit is more robust against SET, that is, Q_c is bigger. Moreover, varying the W value, the importance of taking into account variations of the instant of the pulse in relation to the magnetic state of the MTJ is highlighted. For example, regarding only the most critical points, when the delay is 1.88 ns (red curves) the Q_c can increase from 0.29 fC ($W = 80$ nm) to 0.70 fC ($W = 400$ nm) which would mean an increase in robustness relative to the minimum Q_c. On the other hand, if the delay is 2 ns (blue curves), the gain of robustness is smaller, Q_c varies from 0.56 fC ($W = 80$ nm) to 0.72 fC ($W = 400$ nm).

It is also worth mentioning that as the size W of the access transistor increases, inferences about the increase in SET robustness may change in relation to the critical Q_c. For example, while with $W = 80$ nm the most critical point when the SET occurs before the write pulse (continuous curves in Fig. 5.13) is associated with the delay of 1.88 ns, for bigger W values, the critical part is related to the delay 2 ns [200].

On the other hand, it can be seen in Fig. 5.13 that when the SET pulse occurs after the end of the write pulse (dashed curves in Fig. 5.13), the greatest disparity in terms of critical charge variance appears. That is, if the analysis has been made only by considering a possible SET after the end of the write pulse, the conclusions could mask a minimum Q_c value of 0.29 fC (delay 1.88 ns and $W = 80$ nm) by 1.05 fC (delay 2 ns and $W = 80$ nm), which would mean an erroneous analysis of the SET robustness.

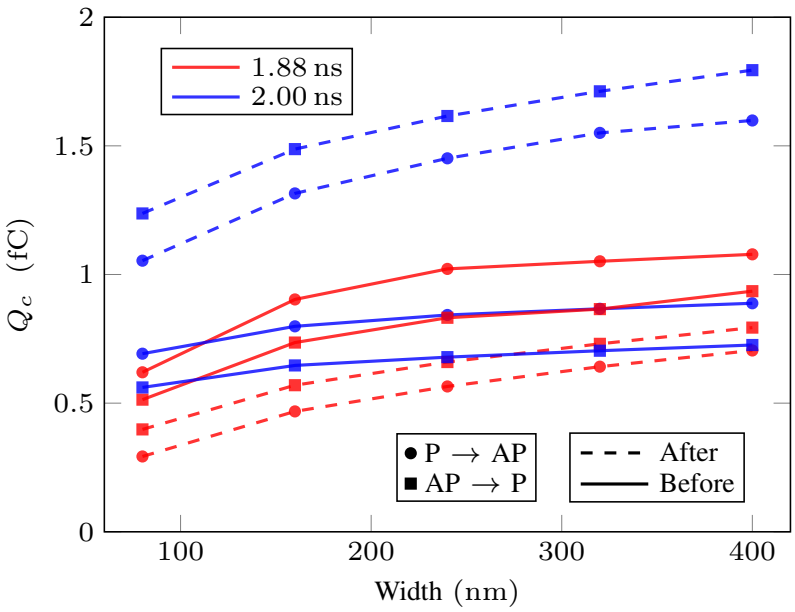


Figure 5.13 – Q_c values for different width W.

The results presented in Fig. 5.13 highlight that resizing the width of the access transistor can increase the robustness of the circuit against SET. However, it is worth remembering that larger transistors also mean overhead in the circuit area. It is also clear the importance of the temporal analysis done in this thesis, not only between the striking time and the write pulse, but also the one of the write pulse moment and the minimum fluctuations of the MTJ [200].

The above results expose that an attention to the circuitry surrounding the write pulse generation is necessary to not create more critical points in the circuit with an MTJ in terms of SET robustness. Although a simple circuit based on MTJ is being considered, these results indicate that in order to obtain the advantages related to the robustness against SET, detailed analysis and attention have been considered regarding the set of components and their functions around the MTJ under the penalty of ending up generating a circuit as sensitive the equivalent in CMOS.

5.3 Reliability Analysis of NAND-Like Spintronic Memory

This section analyses the reliability of NAND-Like spintronic memory. These results were published in [202]. The SET model is given by (4.3).

A 28 nm FDSOI CMOS design-kit is also utilized to implement and simulate the 4-bit NAND-SPIN memory architecture in Fig. 4.8. $V_{DD} = 1.2V$, the access transistors have channel width $W = 100\,\text{nm}$ and channel length $L = 30\,\text{nm}$. The SET charge was varied until 10 fC and the

considered MTJ device has design parameters as listed in Table 5.5 [185].

Table 5.5 – Design specification of MTJ compact model.

Parameter	Value
Free layer thickness	1 nm
Heavy metal thickness	4 nm
Damping factor	0.02
Resistance-area product	$5\,\Omega\mu m^2$
Saturation magnetization	$1.15 \times 10^6\ A/m$
Spin Hall angle	0.3
Tunneling spin polarization	0.62
Heavy metal resistivity	$200\,\mu\Omega$ cm
Exchange bias	15 mT

5.3.1 Failure Condition

Write failures occur when the MTJ in the bit-cell does not appropriately switch between parallel and anti-parallel states. In other words, because of the SET, the MTJ does not switch when it has to or the MTJ switches when it should not to do.

Similarly to the previous section, the critical charge Q_c is the minimum SET charge that leads to an undesirable MTJ state switching when it reaches the access transistor. To analyse the sensitivity of the circuit against SET, a SET pulse is simulated to strike an access transistor.

Fig. 5.14 illustrates the occurrence of a SET with 2 fC in T1 in two different striking times [202]. The yellow curve represents the normal operation of MTJ1, that is, after the erase pulse, its state changes from P ($mz_1 \approx 1$) to AP ($mz_1 \approx -1$). The red and the blue curves represent the operation of MTJ1 after a strike at 1.1 ns and 1.2 ns, respectively. As can be seen, even if both strikes have the same charge, an error appears only for the red curve, proving that the failure occurrence depends on the striking time as in the analysis of VCMA-MTJ based MeRAM [202].

5.3.2 Simulations Results

This section presents the SET analysis on the NAND-SPIN for erase and program steps.

5.3.2.1 SET during the erase step

In this step, a correct operation means that after the write pulse, all MTJs will be at AP state. Therefore, a write failure means that at least one of the MTJs is not at AP state. Two (extreme) cases are considered [202]:

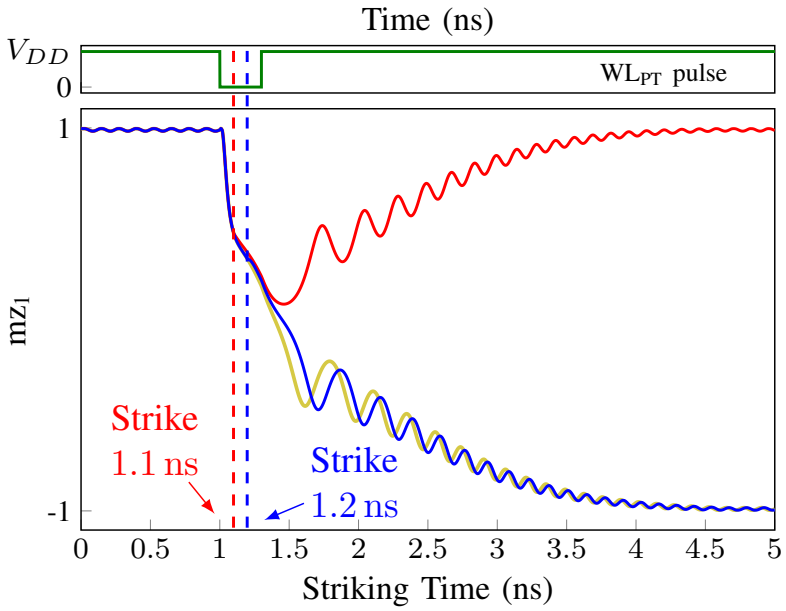


Figure 5.14 – Time diagram with SET in two different striking time.

- Case 1: all MTJs are at P state before the write pulse.
- Case 2: all MTJs are at AP state before the write pulse.

Fig. 5.15 shows the Q_c value at different striking times for Case 1 [202]. A write pulse is applied in PT (green curve) and the SET is simulated over the transistors T1 (blue curve), T2, T3, and T4 (red curve), one at a time. The striking time is related to the write pulse, that is, striking time equal to 1 ns means that the striking time is exactly at the beginning of the write pulse. The shaded areas represent the safe regions of write operation. In other words, charge values in these regions do not lead to write failure [202].

This figure also shows that the critical striking time (lowest Q_c value) is 1.05 ns, that is, 50 ps after the beginning of the write pulse. Moreover, different Q_c values are required to lead to a write failure depending on which access transistor is reached by the SET [202]. While a SET with a charge greater than 1.39 fC in T1 can result in a write failure (i.e. at least one MTJ don't switch to AP state), a SET with a charge only greater than 1.05 fC that reaches T4 is enough to lead to a writing error.

Furthermore, it can be noticed that when a SET reaches the access transistor during the write pulse, the circuit is not SET robust (small Q_c can lead to a write failure). On the contrary, if the SET reaches the access transistor before or after the write pulse, even with level of charge as big as 10 fC, it does not result in a failure. This is because without write pulse during the erase step,

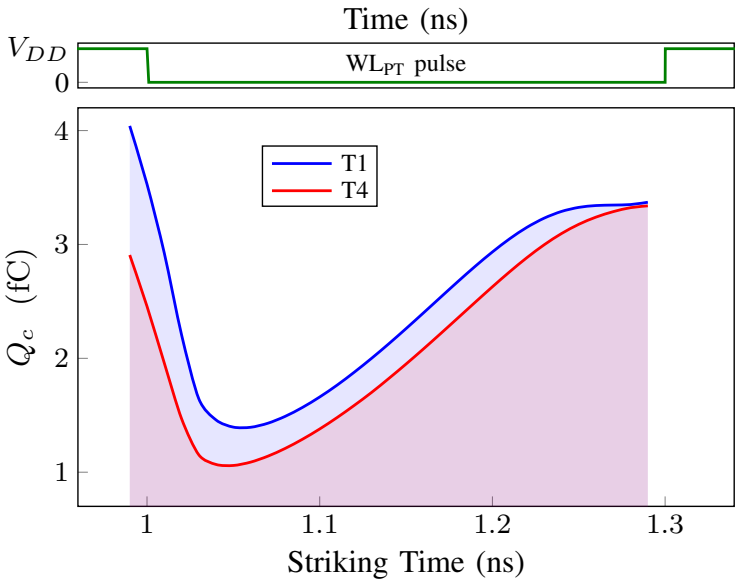


Figure 5.15 – Value of Q_c during the erase step for Case 1.

PT and NT transistors are off and no current goes through the MTJs [202]. However, it is worth pointing out that if the SET occurs just before the beginning of the write pulse, it can lead to some write failure, because some charge can be accumulated until the write pulse starts.

Considering Case 2, no failure was observed, even with SET charges up to 10 fC. This shows that the circuit is robust for this configuration [202].

The obtained results show when the NAND-SPIN is more vulnerable during this phase of the write process. A strategy to increase its robustness consists into setting BL to V_{DD} during the write pulse of the erase step, since it prevents any MTJ from getting into P state. In other words, even if a SET reaches an access transistor, it will not generate a current I_p that leads the MTJ to its P state [202].

5.3.2.2 SET during the program step

In this step, a correct operation means that, after the write pulse, the MTJ concerned by the write operation changes its state from AP to P. Therefore, a write failure means that the MTJ concerned by the write operation still continue at AP state or that any other MTJ not concerned by the write operation changes its state. Two representative cases are analysed [202]:

- Case 1: the MTJ1 is the device concerned by the write operation and the SET reaches T1.
- Case 2: the MTJ1 is the device concerned by the write operation and the SET reaches T4.

For Case 1, the SET occurrence will not negatively impact the circuit operation because the SET will increase the current I_p. Therefore, MTJ1 will continue to change to its P state and this SET will not influence any other MTJ since the other correspondent access transistors will be off [202].

For Case 2, three different situations can lead to a write failure [202]:

- The SET generates a current that decreases the current through the MTJ1. This maintains MTJ1 at AP state (that is, a write failure). However, the SET will not change the state of any other MTJ.
- The SET generates a current that decreases the current through the MTJ1. This maintains MTJ1 at AP state (that is, a write failure). Moreover, the SET can change the state of at least one other MTJ so leading at least one other MTJ to P state.
- The SET generates a current that changes the state of at least one other MTJ to P state while maintaining MTJ1 at P state.

The situations above were analysed varying the SET charge. Fig. 5.16 shows the Q_c value at different striking times for Case 2. The green curve represents the write pulse in WL of T1. The shaded area represents the safe region of write operation. The critical striking time (lowest Q_c value) is 1.12 ns, that is, 0.12 ns after the beginning of the write pulse. For this striking time, if a SET with charge greater than 0.3 fC reaches T4, it will lead to a write failure [202].

The results show that the robustness of the NAND-SPIN against SET is highly dependent of the striking time. The SET robustness also depends on the step of the write operation (see Fig. 5.15 and Fig. 5.16). Comparing Fig. 5.15 and Fig. 5.16 at critical striking time, it can be seen that the critical charge in erase step is bigger than in program step. However, in both steps, the write process is significantly more sensitive to SET effects when the SET occurs during the write pulse, specially during its beginning [202].

It is worth mentioning that STT-MRAM are prone to writing failures similar to those of the Case 2, since BL and SL are both activated for various bit-cells during the write operation. For example, suppose that the selected device for write operation is MTJ_a and let MTJ_b be another MTJ in any adjacent bit-cell. If a SET reaches the access transistor related to MTJ_b, this SET can lead to a change in the MTJ_b value so resulting in a write failure.

The width of the access transistors were changed in order to verify the influence of this parameter on the SET robustness during the program phase. Table 5.6 presents the critical striking

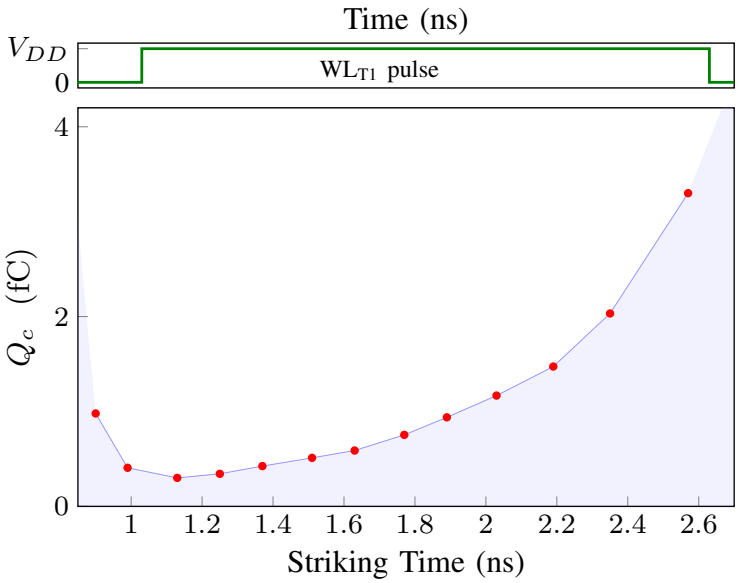


Figure 5.16 – Value of Q_c during the program step for Case 2.

time (T_c) and the corresponding Q_c for Case 2 considering different widths of the access transistors [202].

Table 5.6 – Critical striking time and Q_c for the program step varying W.

	$W = 100\,\text{nm}$	$W = 120\,\text{nm}$	$W = 140\,\text{nm}$
T_c	1.12 ns	1.12 ns	1.12 ns
Q_c	0.3 fC	1.5 fC	2.7 fC

It can be noticed that any analysed width value of the access transistors leads to the same critical striking time, suggesting that changes in the width of these transistors do not influence the instant in which critical charge is minimal.

As the access transistors width increases, their current-absorbing capacity is expected to increase due to its bigger capacitance, as seen in Table 5.6. Hence, transistors resizing may be a suitable strategy to harden NAND-SPIN structure against SET. Despite the area overcost, hardened NAND-SPIN remains less expensive than SOT-MRAM (which requires two transistors per bit-cell) [202] and a faster increase in the minimal Q_c than in VCMA-MTJ based MeRAM. When comparing to the CMOS comparator analysed before, the increase in the minimal Q_c with transistors resizing indicates that circuits based in 1T1MTJ can achieve a better protection in presence of SET.

5.4 Proposed MTJ-based ADC

In [134], a 3-bit spin-based ADC is proposed. However, the proposed architecture leads to a current leak that crosses each MTJ during the conversion phase, resulting in an extra energy consumption. On the other hand, a voltage-controlled stochastic switching device based on a superparamagnetic nanomagnet is proposed in [180]. It uses the probability of MTJ be in a determined state and a counter to determine which is the level of the input voltage. Therefore, the maximum frequency of operation is limited since several cycles of a counter are required to generate the output based on the stochastic analysis. In [220], the spin Hall effect (SHE)-driven domain wall motion devices are used to create a logic-in-memory ADC.

In this section, a k-bit MTJ-based ADC using SOT to change the MTJ state is proposed. Unlike existing designs, in this proposition the SOT mechanism is used in the two phases of the write operation. In addition, for the read operation, each MTJ has a separate read port improving the read reliability. This work was published in [235].

5.4.1 Architecture

This section presents the proposed k-bit MTJ-based ADC. It consists of n MTJs, $n-1$ resistors and $n+1$ NMOS, where $n = 2^k - 1$ as showed in Fig. 5.17 [235]. Each NMOS connected to the respective MTJ is also connected to a sensor amplifier (SA) circuit. The analog input current I_{in} is converted into a digital output.

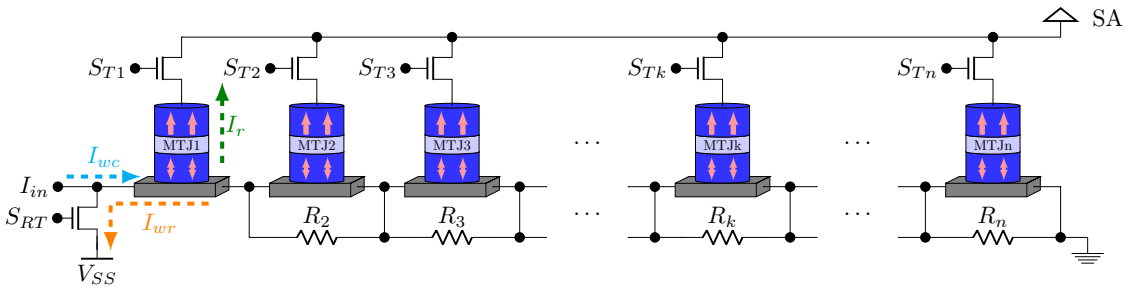


Figure 5.17 – Proposed k-bit MTJ-based ADC architecture.

Fig. 5.18 illustrates the timing diagram for the write and read operations over MTJk. As can be noticed, the write operation has two phases [235]:

- Reset: all MTJs are initialized at their AP states. In order to do this, RT is on and the access transistors are off. Then, a write current I_{wr} goes through the HM.

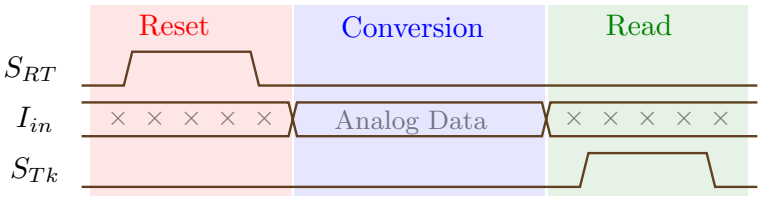


Figure 5.18 – Timing diagram of write and read operations for the MTJ-based ADC.

- Conversion: in this phase, both RT and the access transistors are off. Therefore, a current I_{wc} flows through the HM and the resistors. Only some MTJs will have their states changed depending on the current which passes through the HM below each MTJ. A small current I_{wc} will change the first MTJs (MTJ1, MTJ2,...) to their P states. Consequently, the analog input current I_{in} will be represented by the quantity of switched MTJs.

It can be noticed that the two phases of the write operation use the SOT mechanism to impose the MTJs state.

Concerning the read operation, the access transistor corresponding to the MTJ which will be read is on, and the others are off. The reading of the MTJ state is made by comparing a reference current with I_r. In the proposed MTJ-based ADC, the current I_r doesn't pass through the HM of all MTJs. In other words, each MTJ has a specific read port through which the current I_r will flow as illustrated in Fig. 5.19.

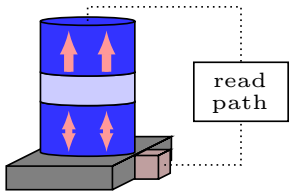


Figure 5.19 – MTJ structure with the read port.

Binary search can be used to optimize the reading process. For example, considering a 3-bit MTJ-based ADC, firstly the MTJ4 will be read. Depending on its state, the first partition (where MTJ2 is central) or the second one (where MTJ6 is central) is chosen and its central MTJ will be read. The process is repeated in a new search space limited by the MTJs previously read in the second read phase. It can be noticed that only 3 phases of the read operation are required to know the state of the 7 MTJs. Fig. 5.20 shows the next MTJ that will be read, according to the state of the MTJ that was read in the previous read phase. Table 5.7 presents the representation of the MTJ states and the ADC's output for the proposed 3-bit MTJ-based ADC.

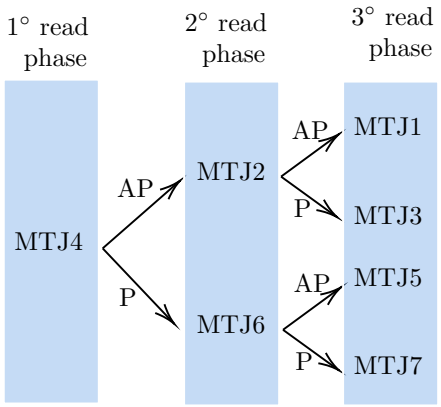


Figure 5.20 – MTJ read in each read phase for the proposed 3-bit MTJ-based ADC.

Table 5.7 – MTJ state and ADC's output for the 3-bit MTJ-based ADC.

MTJ1	MTJ2	MTJ3	MTJ4	MTJ5	MTJ6	MTJ7	output
AP	AP	AP	AP	AP	AP	AP	000
P	AP	AP	AP	AP	AP	AP	001
P	P	AP	AP	AP	AP	AP	010
P	P	P	AP	AP	AP	AP	011
P	P	P	P	AP	AP	AP	100
P	P	P	P	P	AP	AP	101
P	P	P	P	P	P	AP	110
P	P	P	P	P	P	P	111

Let R_M be the resistance of the HM below of one MTJ, I_c be the current required to change the MTJ state, and I_d be the difference of current between each level of the ADC. Since MTJk ($k \neq 1$) has a current divider and each MTJ is associated to an ADC level, the values of the resistors are calculated as (5.1) for $k \geq 2$. While I_d is related to the ADC characteristics, I_c depends on the MTJ and HM characteristics.

$$R_k = \frac{R_M I_c}{(k-1) I_d} \tag{5.1}$$

5.4.2 Simulation Results

This section addresses the simulation results of the proposed k-bit MTJ-based ADC [235]. Firstly, the influence of the HM and MTJ characteristics on the I_c value is performed. Then, the setup is given. Finally, the performance of the proposed MTJ-based ADC is discussed and compared with other ADCs presented in the literature.

5.4.2.1 I_c Analysis

The I_c current is responsible for changing the MTJ state. The characteristics of the HM and MTJ influence the I_c value as shown in Fig. 5.21. In the x-axis, different HM configurations are considered, for example HM with different width, length, and thickness. Given a determined HM configuration, a process variation (PV) considering 3σ Gaussian and 1% changes in MTJ parameters is performed and its impact on the I_c value is shown on the y-axis representing the I_c variation due to the manufacturing process.

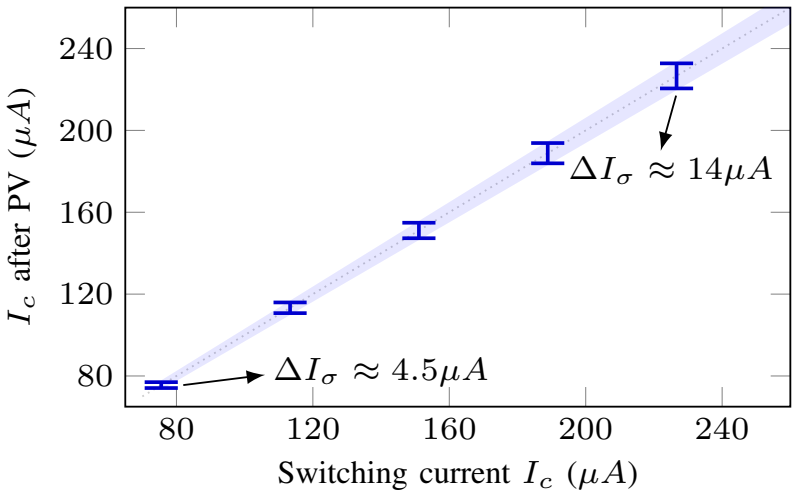


Figure 5.21 – I_c variation due to the manufacturing process.

It can be noticed that a big I_c increases the current variation (ΔI_σ), which reflects limitations due to the manufacturing process. While a determined HM configuration leads to $I_c \approx 78\,\mu$A and $\Delta I_\sigma \approx 4.5\,\mu$A, another configuration results in $I_c \approx 230\,\mu$A with $\Delta I_\sigma \approx 14\,\mu$A. The proposed MTJ-based ADC aims to reduce this influence by using a minimum and equal switching current I_c for all MTJs. This leads to less susceptibility to the effects of the process variation.

5.4.2.2 Setup

A 28 nm FDSOI CMOS design-kit is utilized to implement and simulate the proposed MTJ-based ADC illustrated in Fig. 5.17. The MTJ design parameters are listed in Table 5.8.

5.4.2.3 Performance

In order to analyse the proposed MTJ-based ADC, the architecture was simulated for 3-bits and 4-bits resolution considering the parameters given in Section 5.4.2.2. As presented before, the

Table 5.8 – Design specification of MTJ compact model.

Parameter	Value
Heavy metal thickness	1.5 nm
Heavy metal width	40 nm
Heavy metal length	40 nm
Damping factor	0.03
Resistance-area product	$10\,\Omega\mu m^2$
Saturation magnetization	$10^6\ A/m$
Spin Hall angle	0.3
Heavy metal resistivity	$150\,\mu\Omega$ cm
Exchange bias	15 mT

number of switching MTJs determines the output of the proposed MTJ-based ADC.

For these simulations, the range of the analog input current desired to convert varies from the minimum current required to switch a single MTJ using SOT effect ($\approx 80\,\mu$A for this configuration) up to a maximum current predefined $I_{max} = 180\,\mu$A. The 3-bit MTJ-based ADC transfer function is illustrated in Fig. 5.22. In addition, ΔI_σ is illustrated considering the PV. Since the current switching levels are decided independently by each MTJ, the differential nonlinearity (DNL) of all the ADC levels is limited by the same factors related to ΔI_σ. For the implemented 3-bit MTJ-based ADC, $DNL = \pm 0.18 LSB$ is achieved.

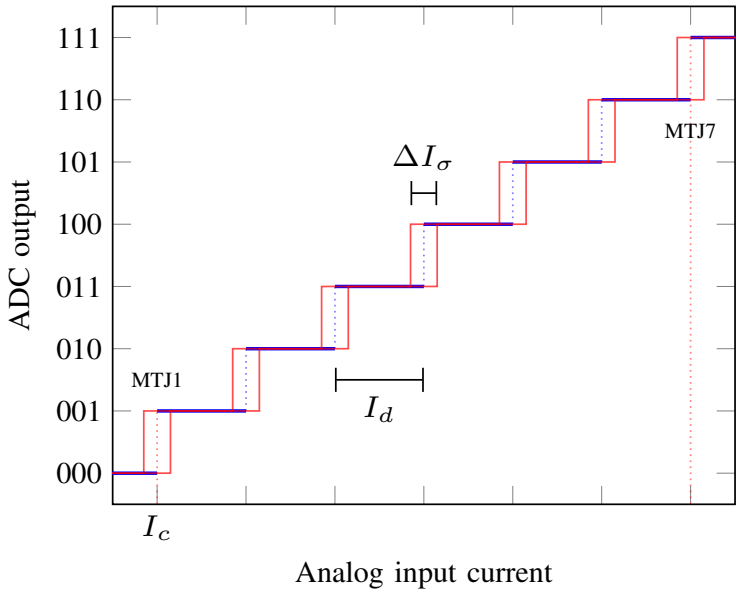


Figure 5.22 – 3-bit MTJ-based ADC transfer function.

Table 5.9 presents the range of energy consumption during the conversion phase (Ec_{min} to Ec_{max}), the energy consumption during the reset phase (E_{reset}), the total energy consumption,

and the power achieved for different resolution in bits (N_b) considering the maximal reachable frequency of 10 GHz in the conversion phase. For example, considering 3-bit MTJ-based ADC, the energy consumption for switching the MTJs states varies from 2.2 fJ to 16.5 fJ, while the total energy consumption in the worst case is 37.3 fJ.

Table 5.9 – MTJ-based ADC performance.

N_b	Ec_{min}	Ec_{max}	E_{reset}	Energy	Power
3	2.2 fJ	16.5 fJ	19.8 fJ	37.3 fJ	0.363 mW
4	5.0 fJ	32.7 fJ	32.4 fJ	66.1 fJ	0.651 mW

5.4.2.4 Comparison

Table 5.10 gives a performance comparison between the proposed k-bit MTJ-based ADC and other ADCs presented in the literature in terms of technology, maximum frequency (F_{max}), resolution in bits (N_b), energy, and power consumption. Some of them use only CMOS [236, 237] and others use spin-based technologies [134, 180, 220, 238–240]. It can be noticed that the proposed MTJ-based ADC leads to a better performance in terms of energy-efficient compared to the ADC presented in this table [235].

Table 5.10 – ADC performance comparison.

Reference	Technology	F_{max}	N_b	Energy	Power
[134]	22 nm	9 GHz	3	350 fJ	-
[220]	22 nm	1 GHz	2	201.48 fJ	0.285 mW
[220]	22 nm	2 GHz	2	196.65 fJ	0.549 mW
[238]	32 nm	20 MHz	8	21 fJ	0.096 mW
[180]	45 nm	100 kHz	8	-	0.034 mW
[239]	45 nm	1 GHz	3	-	6.56 mW
[240]	45 nm	1 GHz	3	480 fJ	1.9 mW
[236]	65 nm	20 MHz	4	-	30 mW
[237]	90 nm	2 GHz	3	270 fJ	3.9 mW
This work	28 nm	10 GHz	3	37.3 fJ	0.363 mW
This work	28 nm	10 GHz	4	66.1 fJ	0.651 mW

Since a separate read port is connected to each MTJ in the proposed MTJ-based ADC, there is an improvement in the read reliability compared with the other ADCs presented in the literature such as the ADC presented in [134] which has a bigger dependency in the use of the HM to the read operations. In addition, the separate read port allows the use of a read circuit simpler than the required in [134, 220] which require different reference resistances.

Finally, it is worth highlight that in the proposed MTJ-based ADC, all MTJs have the same

parameters and a minimal current is required to change the MTJ state regardless of the value of the analog input signal. With this, the effects of variability in the switching current are minimized since this variation is greater with the increase of the level of the switching current.

5.5 Application Case

This section deals with wideband spectrum sensing using an RMPI AIC. RMPI AIC was chosen because it is the most general device for compressive sensing. The objective is to simulate the conditions of an AIC for the recovery of spectrum which has relatively low activity, that is, a sparse spectrum in frequency.

5.5.1 Simulation Setup

The simulations considered the direct analysis of a 3 GHz band that may correspond to a baseband or may have been extracted from higher frequencies in a spectrum. Spectrum scarcity is illustrated through 4 independent sources randomly spread within the 3 GHz range. The sources were generated using OFDM symbols, 64 sub-carriers, cyclic prefix (CP) equivalent to 16 symbols, and symbol period equals to 3.2 μs. This setup leads to a signal band of 80 MHz within the analysed spectrum, representing a relatively high degree of sparseness ($80/3000 < 3\%$).

The considered RMPI has M branches. Each branch has a different sequence $\phi_n(t)$ with size N resulting into an unique information collected. The pseudo-random sequences used in the mixes of the RMPI can be approximated by a random signed Bernoulli matrix that is a good sensing matrix [97].

The sparse recovery algorithm can be chosen according to the recovery needs in terms of time complexity, energy consumption, and/or offline signal recovery. The OMP algorithm was chosen for recovery the spectrum because it is a widely used measure of comparison. Although the OMP complexity may become prohibitive for very large matrices, the fact that it achieves excellent results [97] allows it be a basis for how far signal recovery can go. Of course, other algorithms and even some neural networks can be used for spectrum recovery in order to reduce complexity and/or estimation time [241, 242].

The performance metric is the probability of detection P_d (percentage of the band occupied found correctly). Notice that, according to the recovery algorithm used, the probability of false alarm allowed is a factor that needs to be adjusted. Some recovery algorithms rely on iterative fea-

ture of selecting and deselecting a given frequency throughout the iterations, so these algorithms may get the wrong sense of finding the right frequencies and may have overestimated the spectrum occupied. In other words, the algorithm can success at finding the right frequencies but with a high false alarm incident rate. OMP algorithm does not permit to deselect a frequency already identified, therefore it allows a strong control of false alarm. This control comes through a stop criterion based, for example, on the maximum band to be detected.

5.5.2 Simulation Results

The simulations were performed varying the ADC resolution (number of bits N_r), the number of branches of the RMPI AIC (M), the number of samples (S), and the rate N/M. The rate N/M represents the sampling rate reduction achieved by using an AIC instead of directly using an ADC for spectrum sensing.

In order to illustrate the simulations, Fig. 5.23 shows an example of a spectrum to be estimated (in blue) and the bands of the spectrum which were estimated as being occupied (in red).

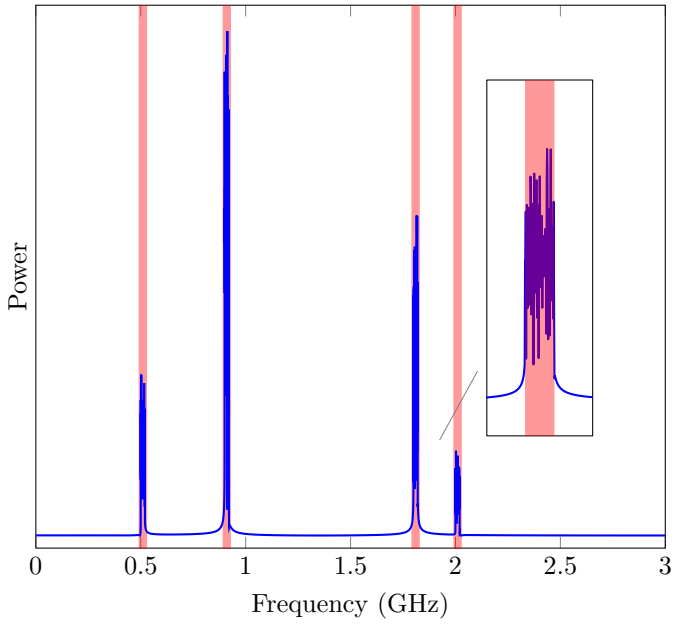


Figure 5.23 – Example of the spectrum to be estimated and the bands of the spectrum classified as occupied.

5.5.2.1 Varying the ADC resolution

Fig. 5.24 shows the P_d values as a function of the ADC resolution used in the RMPI AIC. It considers $S = 150$ for an RMPI with 4, 8, 12, and 16 branches.

It can be seen that for the simplified signal recovery task, the ADC resolution can considerably decrease without significant reducing in the P_d value. Indeed, the objective is not to fully recover the signal, but only to estimate which frequencies are occupied.

The results show that an ADC with 4 bit resolution leads to P_d values close to those obtained using an ADC with 12 bit resolution. This shows that ADC resolution can be lowered to reduce its complexity without significant degrading performance.

In addition, the influence of the number of branches of the RMPI can be noticed. It is important to emphasize that the implementation of a larger number of branches brings with it the challenges of AIC synchronization. The results show that an RMPI with 8 branches achieves results close to that obtained using an RMPI with 16 branches.

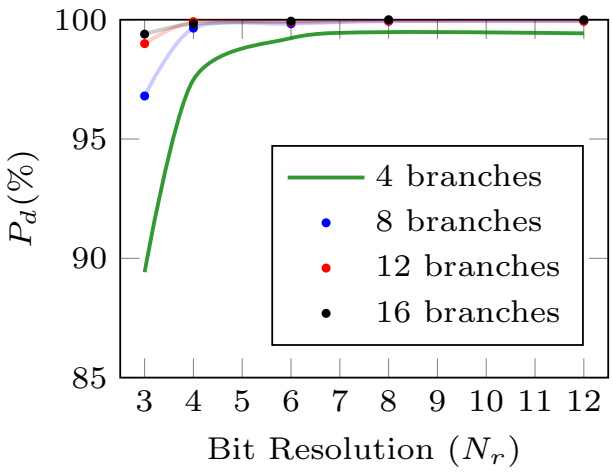


Figure 5.24 – $N_r \times P_d$ varying the number of branches in the RMPI.

5.5.2.2 Varying the number of branches of the RMPI AIC

Fig. 5.25 shows the P_d values as a function of the number of RMPI AIC branches (M) considering $S = 150$ for 3, 4, 6, 8, and 12 bit resolution.

These results suggest that using an ADC with only 3 bits of resolution leads to low P_d values. Even using an RMPI with 12 branches, a 3-bit ADC greatly reduces the accuracy of detection. On the other hand, it is noticeable that a proper detection is achieved (good P_d values) from 4-bit ADC upwards.

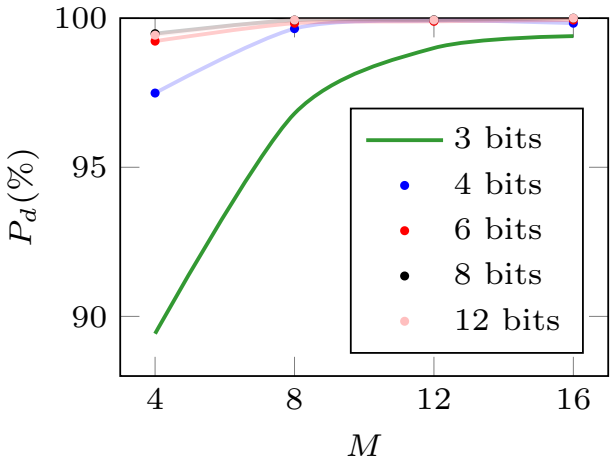


Figure 5.25 – $M \times P_d$ varying the number of bits.

5.5.2.3 Varying the number of samples

Fig. 5.26 shows the P_d values as a function of the number of samples considering $N_r = 4$, $N/M = 2.5$, and $M = 8$.

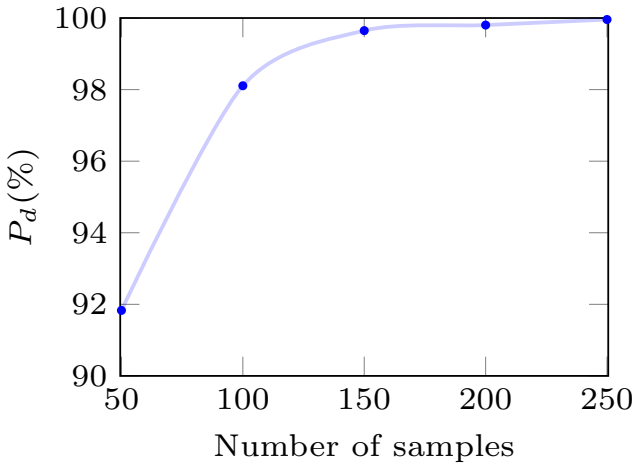


Figure 5.26 – Number of samples $\times P_d$.

In this figure, it can be observed the minimum amount of samples required for a good estimation of the bands of the spectrum that are being occupied. Increasing the number of samples doesn't reduce the detection capacity, however it leads to more energy consumption by both the AIC and the spectrum recovery. The value of 150 samples shows to be sufficient. Smaller sample quantities lead to degradation of the detection rate (low P_d values).

It is worth mentioning that as much as the number of samples is related to the sensing time, it is not the only factor when it comes to compressive sensing. The compression rate (N/M) is also

relevant when calculating the time between samples. Therefore, for a shorter sensing time, it is possible to reduce the number of samples or to reduce the compression rate since the higher the compression rate, the time interval between samples is longer. On the other hand, the lower the compression rate, more samples must be converted by the ADC increasing the power consumption of the AIC. Thus, a tradeoff between the sensing time and the increase of energy consumption brought by the compression needs to be established as a design parameter.

5.5.2.4 Varying the rate N/M

Fig. 5.27 shows the P_d values varying the rate N/M considering $N_r = 4$, $M = 8$, and $S = 150$.

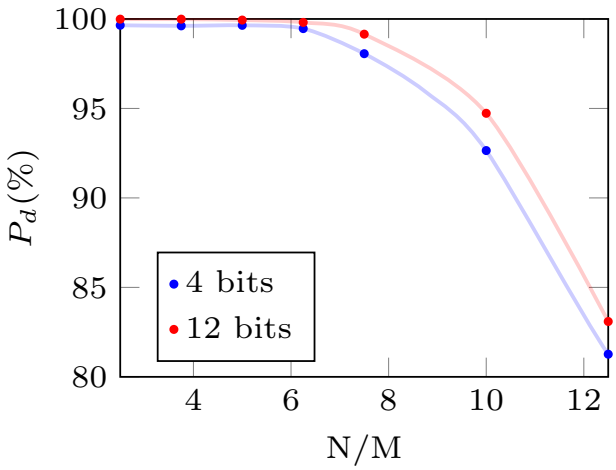


Figure 5.27 – $N/M \times P_d$.

Given the importance of the compression rate that the system may require in order to reduce the AIC consumption, it should be remembered that the compressive sensing literature itself presents certain conditions of use. Fig. 5.27 shows how the probability of detection of occupied frequency bands decreases after a given N/M value. Moreover, it can be noticed that there is not much degradation in the probability of detection P_d when reducing the ADC resolution from 12 bits to 4 bits.

Through these simulations, it can be seen that it is possible to use an RMPI AIC whose ADC has low bit resolution to wideband spectrum sensing. In order to obtain a device with low consumption and high reliability, MTJ-based ADC and transistors with FDSOI technology can be used due to the good characteristics of the FDSOI and MTJ as presented throughout this work.

Chapter 6

Conclusion and Perspectives

This chapter summarizes the work undertaken, recalls its main contributions, and presents its conclusions as well as avenues for future work.

6.1 Conclusions

The scarcity and the inefficient allocation of the spectrum limit the data transmission capacity and the number of users. Cognitive radio (CR) has been considered as a solution to one of the most important challenges in the wireless communication nowadays: the spectrum scarcity.

This thesis dealt with spectrum sensing, which is a major concern for CR. The research was aimed at overcoming some issues related to wideband spectrum sensing when the spectrum occupancy can be considered sparse. With this in mind, the work has mainly focused on analog-to-information converters, the magnetic tunnel junction, and the single event transient.

Starting from the state of the art study, the main spectrum sensing techniques were studied and summarized in Chapter 2. Then, spectrum sensing based on compressive sensing was studied in Chapter 3 and several sparse recovery algorithms were analysed in [97].

Challenges related to the hardware implementation of AIC were presented in Chapter 4, focusing on single event transient impact. This led to the analysis of the SET effects on a dynamic comparator using 28 nm FDSOI CMOS technology. Results showed that the circuit vulnerability is a function of the striking time, the rule of the concerned transistor in the circuit, the transistor channel modulation, and body-bias.

In order to reduce the energy consumption and make the circuit more robust to SET, the characteristics of the MTJ and its applications were studied. This led to the SET impact analysis

on a VCMA-MTJ based MeRAM bit-cell during the writing process. Moreover, the vulnerability of the NAND-SPIN structure was also investigated considering the SET striking time.

The study of MTJ applications presented in Section 4.4 led to propose an MTJ-based ADC. The performance of the proposed ADC was analysed for 3-bit and 4-bit resolution using a 28 nm FDSOI CMOS design-kit. It achieved good results in terms of maximum frequency, energy, and power consumption compared with other ADCs presented in the literature.

The results of this thesis reinforce the suitability of MTJ-based ADC in an AIC for wideband spectrum sensing as an alternative to the high sampling ADC.

Most of the works carried out in this thesis were published in appropriate conferences and journals, as listed in Appendix A.

6.2 Perspectives

As an extension of this thesis, some perspectives are addressed below.

- The models used for MTJ have a great influence on the quality of the robustness estimation. Thus, it would be interesting to further study the influence of the variation of the MTJ parameters in the effective robustness of spectrum sensing circuits against SET.
- In practical applications, simplified calculation structures with a limit on the accuracy of calculation units is a strategy widely used to achieve low-power structures. In order to decrease the power consumption during the calculation performed by the recovery algorithm, an analysis can be made of how the use of fixed point influences the performance recovery of the free frequency bands.
- The use of MTJ in this thesis has been shown to be effective in reducing energy consumption. However, this use was restricted to the converter. It would be interesting to explore the use of MTJ extended to other parts of the spectrum sensing circuit.
- As presented in this work, SET effects can have a negative impact on circuit performance. Since redundant circuits allow these effects to be masked, it would be interesting to study their use in a spectrum sensing context.
- The sensing matrix is very important in the sparse signal recovery. Thus, different sensing matrix strategies as well as different pseudo-random generators and their effects on the spectrum sensing performance could be analysed.

Appendix A

List of Publications

Journal papers

1. MACIEL, N.; MARQUES, E.; NAVINER, L.; ZHOU Y.; CAI, H. “Magnetic Tunnel Junction Applications”. Sensors, vol. 20, no. 1, p. 121, Dec 2019. doi: 10.3390/s20010121.

2. MACIEL, N.; MARQUES, E. C.; NAVINER, L.; CAI, H.; YANG, J. “Reliability Analysis of NAND-Like Spintronic Memory”. In Microeletronics Reliability Journal, 2019. doi: 10.1016/j.microrel.2019.06.024.

3. MACIEL, N.; MARQUES, E. C.; NAVINER, L.; CAI, H.; YANG, J. “Voltage-Controlled Magnetic Anisotropy MeRAM Bit-Cell over Event Transient Effects”. In Journal of Low Power Electronics and Applications, vol. 9, 2019. doi: 10.3390/jlpea9020015.

4. MACIEL, N.; MARQUES, E. C.; NAVINER, L. A. B.; CAI H. “Single-Event Transient Effects on Dynamic Comparator in 28nm FDSOI CMOS Technology”. In Microeletronics Reliability Journal, vol. 88-90, pp. 965-968, 2018. doi: 10.1016/j.microrel.2018.07.114.

5. MARQUES, E. C.; MACIEL, N.; NAVINER, L.; CAI, H.; YANG, J. “A Review of Sparse Recovery Algorithms”. In IEEE Access, vol. 7, pp. 1300-1322, 2018. doi: 10.1109/ACCESS.2018.2886471.

Conference papers

1. MACIEL, N.; MARQUES, E.; NAVINER, L.; CAI, H. “Magnetic Tunnel Junction-Based Analog-to-Digital Converter Using Spin Orbit Torque Mechanism”. In IEEE International

Conference on Electronics Circuits and Systems (ICECS 2020), Glasgow, Scotland, 2020. doi: 10.1109/ICECS49266.2020.9294780.

2. MARQUES, E. C.; MACIEL, N.; NAVINER, L.; CAI, H.; YANG, J. "Nonlinear Functions in Learned Iterative Shrinkage-Thresholding Algorithm for Sparse Signal Recovery". In IEEE International Workshop on Signal Processing Systems (SiPS 2019), Nanjing, China, 2019. doi: 10.1109/SiPS47522.2019.9020469.

3. MARQUES, E. C.; MACIEL, N.; NAVINER, L.; CAI, H.; YANG, J. "Deep Learning Approaches for Sparse Recovery in Compressive Sensing". In International Symposium on Image and Signal Processing and Analysis (ISPA 2019), Dubrovnik, Croatia, 2019. doi: 10.1109/ISPA.2019.8868841.

4. MARQUES, E. C.; MACIEL, N.; NAVINER, L.; CAI, H.; YANG, J. "Compressed Sensing for Wideband HF Channel Estimation". In International Conference on Frontiers of Signal Processing (ICFSP 2018), Poitiers, France, pp. 1-5, 2018. doi: 10.1109/ICFSP.2018.8552050.

5. MACIEL, N.; MARQUES, E. C.; NAVINER, L. "Sparsity Analysis using a Mixed Approach with Greedy and LS Algorithms on Channel Estimation". In International Conference on Frontiers of Signal Processing (ICFSP 2017), Paris, France, pp. 91-95, 2017. doi: 10.1109/ICFSP.2017.8097148.

Appendix B

Résumé en Français

B.1 Introduction

Ce chapitre présente la motivation, les objectifs et les contributions du présent travail.

Les méthodes de stockage des informations codées ont été présentes tout au long de l'histoire de l'humanité. Les dessins sont apparus pour la première fois dans les grottes, suivis par l'utilisation des hiéroglyphes dans l'Égypte ancienne. Puis, avec l'invention de l'imprimerie, les livres ont dominé le stockage de l'information pendant des siècles. Ce n'est qu'au XXe siècle que la disquette, le disque dur et le disque optique ont révolutionné la façon dont nous stockons les données.

De même, la diffusion ou la transmission d'informations codées a une longue histoire. Les Égyptiens et les Grecs ont utilisé un type de correspondance pour transmettre des informations telles que des courriers avec des messagers ou des oiseaux. D'autres méthodes de transmission longue distance comprennent les tambours, les signaux de fumée ou les drapeaux. Cependant, ces méthodes avaient leurs limites car elles dépendaient du sens humain (de la vue ou de l'ouïe) qui était nécessaire pour leur détection.

La révolution de la transmission de l'information a commencé à la fin du XVIIIe siècle avec le début de l'électricité. Seulement un siècle plus tard, dans la dernière décennie du XIXe siècle, Marconi a développé les premiers émetteurs et récepteurs radio pratiques.

Au cours des dernières décennies, les fréquences considérées comme attribuables aux organisations internationales ont augmenté. De nos jours, un vaste ensemble de services et de technologies radio ont inondé le spectre, par exemple les réseaux sans fil locaux, IoT (*Internet of Things*) et les équipements de ville intelligente. Depuis 2011, la planète compte plus d'objets interconnectés

que le nombre de personnes [1]. En 2020, il y a plus de 3,5 milliards d'utilisateurs de smartphones dans le monde [2]. L'augmentation du nombre de dispositifs a également entraîné une augmentation des données qui doivent être capturées, traitées, stockées et communiquées. De plus, la demande en termes de vitesse de téléchargement, de faibles latences et d'efficacité énergétique a augmenté ces dernières années.

Dans les systèmes de communication sans fil, le spectre est l'une des ressources les plus précieuses car il s'agit d'une ressource limitée. Les bandes de fréquences utilisées aujourd'hui par les systèmes de communication sont généralement surchargées [3, 4]. Les modèles de licence utilisent généralement une méthode statique pour diviser le spectre. Il en résulte une utilisation inefficace du spectre. Cette manière statique d'attribuer le spectre limite la capacité de transmission de données et le nombre d'utilisateurs. De plus, avec le nombre croissant de dispositifs à débit de données plus élevé, il est difficile de répondre à toutes les exigences des schémas d'attribution de fréquences statiques. Par conséquent, de nouvelles stratégies pour exploiter efficacement le spectre disponible et surmonter la rareté du spectre ont capté l'intérêt des scientifiques, et donc accru la recherche et le développement, au cours des dernières décennies.

La radio cognitive (*Cognitive Radio* - CR) est considérée comme une approche pour améliorer l'utilisation du spectre radioélectrique. Le concept de CR a d'abord été proposé par J. Mitola dans [6]. La radio cognitive offre à un appareil la capacité d'apprendre et de s'adapter à l'environnement électromagnétique dans lequel il fonctionne, d'être capable d'ajuster ses paramètres opérationnels de manière autonome et dynamique, de maximiser le flux de données, d'atténuer les interférences, de faciliter l'interopérabilité et d'explorer de manière opportuniste les bandes de fréquences sans utilisation ou sous-utilisées.

Certaines parties du spectre, ayant été attribuées à certains utilisateurs, ne sont pas utilisées à plein temps. La caractéristique clé de CR est sa capacité à reconnaître l'environnement de communication et à adapter indépendamment les paramètres de son schéma de communication pour maximiser la qualité de service (QoS), pour les utilisateurs secondaires (sans licence) (*Secondary User* - SU), tout en minimisant les interférences avec les principaux utilisateurs (*Primary User* - PU) et la consommation électrique totale en explorant de manière opportuniste les bandes de fréquences sans utilisation ou sous-utilisées. Par conséquent, en utilisant des émetteurs-récepteurs radio dotés de capacités cognitives, il est possible d'exploiter le spectre inutilisé pour fournir un meilleur accès au spectre en raison des opportunités de spectre.

L'opportunité de spectre peut être définie comme "une bande de fréquences qui n'ait pas uti-

lisée par l'utilisateur principal de cette bande à un moment donné dans une zone géographique particulière" [7]. Par conséquent, pour utiliser efficacement toute opportunité disponible, une CR peut interagir avec l'environnement, détecter et mesurer le spectre. Elle peut prendre des décisions pour adapter ses paramètres d'émetteur ou de récepteur à l'environnement permettant aux utilisateurs secondaires d'occuper une partie du spectre disponible. Pour ce faire, une estimation précise de l'utilisation du spectre et une évaluation des éventuels trous de spectre vacants doivent être effectuées.

L'un des principaux défis de la conception efficace des réseaux de CR comprend la détection de spectre (*Spectrum Sensing* - SS). Sur la base de la taille de la bande d'intérêt, les techniques de détection de spectre sont divisées en détection à bande étroite et détection à large bande. Alors que la détection de spectre à bande étroite (*Narrowband Spectrum Sensing* - NSS) ne considère qu'une partie de la bande, dans laquelle elle est supposée être utilisée par un signal, à détecter, la détection de spectre large bande (*Wideband Spectrum Sensing* - WSS) observe une large bande afin d'identifier les parties de cette bande qui sont occupées ou libres. La détection de spectre présente trois principaux défis pratiques : des algorithmes de détection robustes, des détecteurs aveugles et une détection de spectre à large bande [8].

Cette thèse se concentre sur la détection de spectre à large bande. Selon le théorème d'échantillonnage de Nyquist-Shannon, un signal peut être parfaitement reconstruit à partir de ses échantillons s'il est échantillonné par le taux de Nyquist, c'est-à-dire un taux égal à deux fois la bande passante du signal [9]. Les techniques de détection de spectre à large bande peuvent être classées en détection à large bande de Nyquist et détection à large bande sous-Nyquist. Elles seront traitées dans les prochains chapitres. Les approches sous-Nyquist visent à réduire le coût du matériel et la complexité de calcul par rapport aux implémentations à taux d'échantillonnage élevé. De plus, elles permettent des conversions de signaux à des débits très élevés là où les implémentations des ADC (*Analog-to-Digital Converter*) de l'état de l'art ne permettent pas l'échantillonnage direct à la fréquence de Nyquist.

L'approche classique des convertisseurs analogique-numérique (ADC) est basée sur le critère de Nyquist-Shannon. Par conséquent, l'utilisation de ADC peut nécessiter des taux d'échantillonnage élevés et de nombreux échantillons à traiter. Cela n'est pas judicieux pour les applications à faible consommation telles que les CR et IoT. L'un des principaux défis liés à la CR est le développement de la détection de spectre à large bande sans dépendre de la mise en œuvre des ADCs à un taux d'échantillonnage élevé et d'une diminution de la consommation de matériel. Une alterna-

tive est l'utilisation des caractéristiques du signal d'entrée pour réduire le temps, le matériel et les ressources énergétiques nécessaires. Cela peut être fait grâce à l'implémentation d'un convertisseur analogique-information (AIC) basé sur la théorie de l'acquisition comprimée (*Compressive Sensing* - CS) pour remplacer le classique ADC en réduisant le coût du matériel. L'acquisition comprimée utilise la représentation parcimonieuse d'un signal dans un domaine donné pour effectuer sa numérisation plus efficacement.

À partir de l'étude des techniques de détection de spectre et des convertisseurs analogique-information, cette thèse vise à contribuer au développement d'approches matérielles pour la détection de spectre afin d'améliorer les capacités des réseaux radio cognitifs, y compris l'analyse de fiabilité contre les radiations.

B.2 Radio Cognitive et Détection du Spectre

Cette section introduit quelques concepts importants pour la compréhension de cette thèse. Premièrement, certaines caractéristiques de la radio cognitive sont abordées. Ensuite, les techniques de détection de spectre sont discutées. Dans le domaine de la radio cognitive, la détection du spectre consiste à obtenir les caractéristiques d'utilisation du spectre en tenant compte de l'espace, du temps, de la fréquence, du type de signaux qui occupent le spectre (bande passante, modulation, fréquence porteuse, etc.) [10]. La détection de spectre peut être divisée en : détection de spectre à bande étroite et détection de spectre à large bande.

Radio Cognitive (CR) L'utilisation de la radio cognitive (CR) peut contribuer à atténuer la rareté du spectre grâce à une utilisation plus efficace du spectre. La première définition d'une CR a été faite par Mitola [6]. Le FCC définit une CR comme : "une radio ou un système qui détecte son environnement électromagnétique opérationnel et peut ajuster de manière dynamique et autonome ses paramètres de fonctionnement radio pour modifier le fonctionnement du système, comme pour maximiser le débit, atténuer les interférences, faciliter l'interopérabilité et accéder aux marchés secondaires." [11]. Le spectre est alloué aux utilisateurs avec licence, appelés, dans ce contexte, les utilisateurs primaires (PUs). Ils ont la priorité pour utiliser le spectre. En revanche, les utilisateurs sans licence, appelés utilisateurs secondaires (SUs), ont une priorité inférieure. En plus d'être une approche alternative résolvant la sous-utilisation du spectre, la CR peut également être une solution pour les appareils qui ont besoin d'utiliser le spectre intelligemment, par exemple trouver une opportunité dans le spectre qui améliore ses performances de communication.

Fondamentalement, la CR améliore l'utilisation du spectre, en passant de l'allocation statique du spectre à l'allocation dynamique du spectre. La CR permet d'augmenter le nombre d'utilisateurs sans avoir besoin de plus d'infrastructure de télécommunications. Les fonctions clés des réseaux de CR sont [18] :

- Détection du spectre (*spectrum sensing*) : c'est la tâche cognitive la plus importante. Elle vise à déterminer quelles parties du spectre sont disponibles. Elle est effectuée sur différentes dimensions telles que le temps, la fréquence, l'angle, la zone géographique, le code et le signal. Compte tenu de toutes ces dimensions, plus d'opportunités peuvent mises à disposition d'un SU. La détection du spectre peut également être effectuée de manière collaborative où divers SUs détectent le spectre et partagent leurs informations. Cela peut réduire le temps de détection [19]. La détection de spectre collaborative peut être centralisée ou distribuée.

- Gestion du spectre et décision (*spectrum management and decision*) : après avoir localisé les bandes de spectre disponibles, la CR doit en sélectionner la meilleure en tenant compte de la bande passante, de la puissance d'émission, des schémas de codage, des schémas de modulation et de QoS. Des techniques d'apprentissage automatique peuvent être utilisées pour prendre des décisions afin d'adapter et de développer des stratégies pour maximiser certaines métriques de performance [6, 20–22].

- Mobilité spectrale (*spectrum mobility*) : ele implique la capacité des CRs qui sautent de manière transparente entre différents trous spectraux tout en se basant sur les conditions. Par exemple, les SU doivent se déplacer vers un autre trou de spectre lorsque la bande de spectre actuelle est requise par un PU en raison de la priorité d'accès au spectre pour cet utilisateur sous licence.

- Partage du spectre (*spectrum sharing*) : afin d'éviter les collisions entre utilisateurs, l'accès au spectre doit être coordonné. Dans ce cas, les trous de spectre doivent être divisés entre différents CRs et PUs. Cela peut être mis en oeuvre dans le code, les dimensions de l'espace, la fréquence et le temps. En utilisant la stratégie d'entrelacement, le SU utilise le spectre uniquement lorsque le PU est inactif. D'un autre côté, le SU et le PU utilisent le spectre avec le partage de spectre sous-jacent (*underlay*) et superposé (*overlay*) [23]. Dans l'approche sous-jacente, le SU transmet avec une contrainte de puissance d'émission tandis que la technique de superposition utilise les fractions inoccupées du spectre [24].

Cette thèse se concentre sur la détection du spectre. Les techniques de détection du spectre sont classées en fonction de la taille de la bande d'intérêt dans la détection de spectre à bande étroite et la détection de spectre à large bande (voir Fig. B.1). La détection de spectre à bande étroite vise à identifier si la partie analysée du spectre est occupée ou non. D'autre part, la détection de spectre à large bande vise à déterminer quelles parties du spectre sont vacantes. Les sections suivantes présentent un bref aperçu des techniques les plus couramment utilisées.

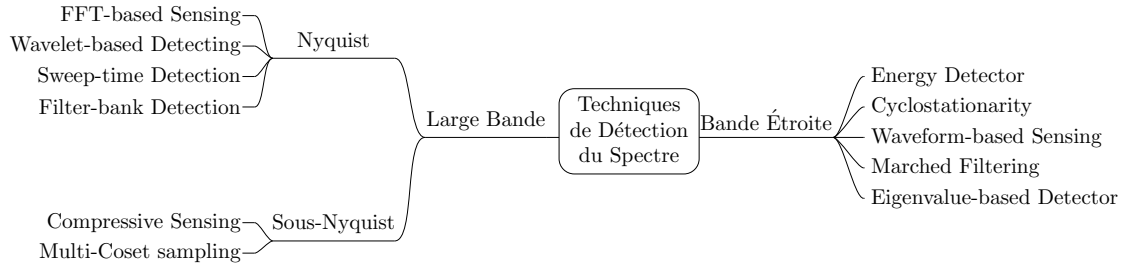


FIGURE B.1 – Techniques de détection du spectre.

Détection de spectre à bande étroite Une méthode de détection de spectre à bande étroite exploite les opportunités spectrales sur une gamme étroite de fréquences. Son but est d'identifier si la bande est occupée par un PU ou non. Elle peut être représentée par des tests d'hypothèses binaires où H_0 représente la vacance et H_1 dénote la présence d'un PU :

$$x(t) = \begin{cases} w(t) & H_0 \\ p(t) + w(t) & H_1 \end{cases} \tag{B.1}$$

où $x(t)$ est le signal reçu à la CR au t^{th} instance d'échantillonnage, $w(t)$ est le bruit gaussien blanc additif (*Additive White Gaussian Noise* - AWGN), et $p(t)$ est le signal de PU.

Les techniques de détection de spectre à bande étroite les plus courantes sont :

- *Energy Detector* ;
- *Cyclostationarity - Spectral Correlation* ;
- *Waveform-based Sensing* ;
- *Matched Filtering* ;
- *Eigenvalue-based Detector.*

Détection de spectre large bande Dans la détection de spectre à bande étroite, seule une gamme de fréquences étroite est exploitée. Cependant, pour augmenter les chances de trouver plus d'opportunités de spectre, une large gamme de fréquences est normalement utilisée [25]. Alors que dans les techniques de détection de spectre à bande étroite, l'intérêt est seulement de savoir si la bande est occupée ou non (une seule décision binaire pour tout le spectre), dans les techniques de détection de spectre à large bande, la connaissance de quelle partie du spectre n'est pas utilisée actuellement est requise. Par conséquent, les techniques de détection de spectre à bande étroite ne peuvent pas être directement employées dans la détection de spectre à large bande.

La détection du spectre large bande fait face à plusieurs défis techniques. L'un des principaux défis est les taux d'échantillonnage très élevés requis par les méthodes d'estimation spectrale conventionnelles. Selon le théorème de Nyquist, pour récupérer parfaitement un signal, il est nécessaire que le taux d'échantillonnage soit au moins égal au double de la fréquence maximale du signal. Autrement dit, il serait nécessaire de mettre en œuvre des convertisseurs analogique-numérique (ADCs) avec une fréquence d'échantillonnage élevée [23]. Cela peut générer un grand nombre d'échantillons et nécessite donc un temps de détection important, beaucoup d'espace de stockage et une consommation d'énergie élevée. De plus, la mise en œuvre de ce dispositif d'échantillonnage pourrait être très coûteuse, complexe et même physiquement peu envisageable en raison des taux de données élevés et de la vitesse d'opération imposée au matériel.

Cependant, dans plusieurs situations, la bande du spectre analysée n'est pas pleinement utilisée et elle peut être considérée comme parcimonieuse ou compressible, c'est-à-dire que la majorité des coefficients du signal dans sa représentation discrète sont égaux ou proches de zéro. En d'autres termes, même si une large bande passante est analysée, seule une partie de l'information est réellement pertinente, c'est-à-dire qu'elle a un faible "taux d'information" [71].

Dans ces scénarios, la théorie de l'acquisition comprimée (CS) (voir la section 3.1) peut être appliquée pour réduire le taux d'échantillonnage et ainsi réduire la consommation d'énergie. CS permet la récupération de signaux parcimonieux ou compressibles à partir d'une fréquence d'échantillonnage inférieure à la fréquence de Nyquist [72]. De plus, avec moins d'échantillons requis, l'espace mémoire de stockage et le traitement du signal diminuent. Afin d'acquérir un signal à des taux proches de son taux d'information, et ayant une détection spectrale plus économe en énergie, plusieurs convertisseurs analogique-information (AICs) ont été proposés (voir la section 3.2).

Par conséquent, pour traiter le problème de la détection du spectre à large bande, deux classes

principales de solutions sont possibles : la détection à large bande de Nyquist et la détection à large bande sous-Nyquist [4, 25].

Les méthodes de détection à large bande de Nyquist utilisent la fréquence de Nyquist pour échantillonner le spectre. Une approche consiste à utiliser un ADC standard pour acquérir directement le signal large bande [73]. D'autres approches "divisent" le large spectre en plusieurs spectres à bande étroite à analyser. Cependant, normalement, ces méthodes rencontrent des taux d'échantillonnage élevés, une complexité de calcul élevée et des retards de traitement [4, 74–76]. Quelques exemples de techniques de détection à large bande de Nyquist sont [4, 25] :

- *Multiband joint detection or FFT-based sensing* ;
- *Wavelet-based detecting* ;
- *Sweep-tune detection* ;
- *Filter-bank detection*.

Les méthodes de détection large bande sous-Nyquist acquièrent des signaux large bande en utilisant des taux inférieurs à Nyquist, en d'autres termes, des taux d'échantillonnage inférieurs au taux de Nyquist. Pour ce faire, la détection compressive peut être utilisée pour récupérer le spectre à partir de moins d'échantillons. Les techniques multi-cosets peuvent également reconstruire le spectre à partir de moins d'échantillons en choisissant une séquence d'échantillonnage qui permet cette reconstruction. Normalement, ces approches peuvent réduire la complexité de calcul, diminuer le délai de détection ou réduire le coût du matériel en raison d'un taux d'échantillonnage élevé dans les implémentations basées sur Nyquist [4, 83, 84]. Certaines méthodes de détection à large bande sous-Nyquist sont [4, 25] :

- *Compressive sensing-based wideband sensing* ;
- *Multi-coset sampling (MC)*.

Cette thèse se concentre sur la détection de spectre à large bande. Après l'étude des techniques de détection de spectre, la détection à large bande sous-Nyquist a été choisie spécifiquement la détection à large bande basée sur l'acquisition comprimée. Plus de détails sont fournis dans le Chapitre 3.

B.3 Détection de Spectre basée sur l'Acquisition Comprimée

Ce chapitre s'ouvre sur les concepts clés liés à la théorie de l'acquisition comprimée. Dans un second temps, une discussion autour de plusieurs architectures de convertisseur analogique-information est articulée. Enfin, certains convertisseurs analogique-numérique sont présentés.

Acquisition Comprimée La théorie de l'acquisition comprimée (CS) peut être utilisée dans des situations où le signal est parcimonieux ou compressible [72, 96]. En combinant les processus d'acquisition et de compression et en exploitant la rareté des signaux, le signal peut être récupéré à partir de moins de mesures que ce qui est requis par le théorème de Nyquist.

La théorie de l'acquisition comprimée peut être appliquée dans plusieurs domaines tels que la détection de spectre [97]. Étant donné que généralement seuls certains des canaux disponibles sont occupés par les utilisateurs, le signal d'intérêt est normalement parcimonieux dans le domaine fréquentiel. Par conséquent, CS peut être utilisé pour détecter un spectre plus large avec des exigences d'échantillonnage réduites, ce qui se traduit par des systèmes plus économes en énergie [4, 25, 97, 101, 102].

Fig. B.2 illustre les principales étapes de la détection de spectre basée sur l'acquisition comprimée. Tout d'abord, un échantillonneur sous-Nyquist obtient peu de mesures du spectre. Ensuite, le spectre est récupéré à partir des échantillons mesurés. Enfin, les sous-bandes occupées sont localisées et identifiées et le SU peut décider dans quelle bande il émettra. La transformée en ondelettes du spectre estimé peut être utilisée pour obtenir les discontinuités spectrales. Leurs positions déterminent les frontières des bandes vacantes et occupées. Une technique de détection de spectre à bande étroite peut être appliquée pour identifier la bande occupée.

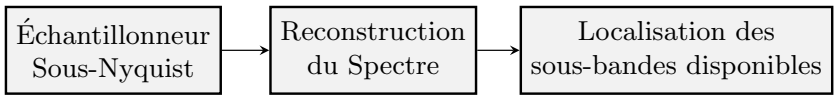


FIGURE B.2 – Détection de spectre basée sur l'acquisition comprimée.

Par conséquent, en réduisant les exigences d'échantillonnage, il est possible de réaliser des systèmes moins chers et plus économes en énergie. Une approche alternative au ADC conventionnel est l'utilisation d'un convertisseur analogique-information (AIC) pour effectuer l'acquisition comprimée.

Convertisseur Analogique-Information (AIC) Les convertisseurs analogique-information (AICs) sont basés sur l'acquisition comprimée pour acquérir et extraire les informations d'activité spectrale. L'AIC permet un traitement plus rapide, est moins coûteux et offre des solutions plus éco-énergétiques que l'ADC [103] classique. En effet, un échantillonnage élevé a un impact majeur sur la consommation du système. De plus, la réduction de la quantité d'échantillons envoyés augmente la vitesse de transmission des informations, ce qui réduit la surface matérielle, la mémoire de stockage et la puissance de calcul. Par conséquent, il s'agit d'une alternative à utiliser dans de nombreux systèmes à latence critique, sensibles au coût et à faible consommation tels que les IoTs, les radios cognitives et les électrocardiogrammes (ECGs) [103]. Les principales architectures AIC sont :

- *Multirate Sampling* (MRS) ;
- *Modulated Wideband Converter* (MWC) ;
- *Non-uniform Sampling* (NUS) ;
- *Random-Modulation Preintegrator* (RMPI) ;
- *Random Demodulator* (RD).

Le faible nombre de mesures obtenues fait de la fiabilité de AIC un problème majeur. Le comparateur est un élément clé des convertisseurs analogique-information. Dans la section 5.1, la fiabilité d'un comparateur dynamique sur la technologie 28 nm FDSOI CMOS est analysée.

Convertisseur Analogique-Numérique (ADC) Comme l'on peut le voir dans la section 3.2, toutes ces architectures AIC nécessitent un ADC. Le choix d'un ADC peut être fait en prenant en compte la résolution (nombre de bits), la fréquence d'échantillonnage, le gain, l'offset, DNL (non-linéarité différentielle - *differential nonlinearity*), ENOB (nombre effectif de bits - *effective number of bits*), INL (non-linéarité intégrale - *integral nonlinearity*), SINAD (rapport signal sur bruit et distorsion - *signal-to-noise-and-distortion ratio*), SFDR (bande dynamique sans parasites - *spurious free dynamic range*), THD (harmonique totale distorsion - *total harmonic distortion*) entre autres. Les principales architectures ADC sont :

- $\Sigma\Delta$ ADC ;
- *Successive-approximation-register* (SAR) ADC ;

- *Pipeline* ADC ;
- *Flash* ADC.

Dans le Chapitre 3, certains types de AIC et ADC ont été abordés. Les ADC traditionnels ont été confrontés à plusieurs défis en termes de taux d'échantillonnage, de bande passante et de consommation d'énergie [129, 133]. De plus, avec la réduction d'échelle de CMOS, il faut éviter une augmentation de la consommation d'énergie statique. Pour surmonter ces problèmes et augmenter les performances de ADC pour répondre aux demandes des appareils IoT, des radios cognitives et d'autres applications en termes de contraintes ADC telles que la surface, le taux d'échantillonnage, la bande passante et la puissance consommation, de nouvelles technologies et de nouveaux designs d'appareils ont été développés [134].

Dans le Chapitre 4, les défis liés à la mise en œuvre matérielle de ces appareils sont présentés, tels que la réduction de la consommation et le problème du transitoire à événement unique. Comme indiqué au chapitre 4, *Magnetic Tunnel Junction* (MTJ) est apparu comme l'un des candidats prometteurs en raison de sa faible consommation d'énergie, de sa grande évolutivité et de son endurance potentiellement infinie [135]. En effet, le MTJ a été exploré afin de réduire la consommation d'énergie et d'économiser la surface des ADC (voir la section 4.4.7). De plus, dans cette thèse, un ADC basé sur MTJ est proposé et présenté dans la section 5.4.

B.4 Défis de l'Implantation Matérielle

Certaines des exigences matérielles liées à la détection de spectre pour les applications radio cognitives sont : une grande bande dynamique pour le signal analogique d'entrée, une fréquence d'échantillonnage élevée, une résolution ADC élevée et un traitement de signal conduisant à une complexité de calcul importante. En d'autres termes, les composants RF, tels que les antennes et les amplificateurs de puissance, doivent pouvoir fonctionner sur une large bande de fréquences. De plus, le traitement du signal devrait avoir un retard relativement faible nécessitant des unités de traitement à grande vitesse (DSPs ou FPGAs). Comme présenté dans le chapitre 2 et dans le chapitre 3, AIC est une approche alternative pour surmonter les ADCs à grande vitesse qui consomment beaucoup d'énergie. Il est également souhaitable de réduire la surface et de diminuer la dissipation de puissance.

Les technologies FDSOI peuvent être utilisées pour implémenter des périphériques à haut débit/faible consommation. D'autre part, la découverte de la magnétorésistance géante (*Giant Ma-*

gnetoresistance - GMR) [136, 137] a conduit au développement de la spintronique [138]. Les études dans ce domaine ont abouti à plusieurs avancées importantes. Avec la réduction d'échelle de CMOS, le besoin d'alternatives viables pour réduire la consommation due aux courants de fuite augmente et les dispositifs basés sur le spin apparaissent comme l'une des approches les plus prometteuses pour résoudre ce problème. *Magnetic Tunnel Junction* (MTJ) a un rôle important dans le développement de la spintronique [135]. La réduction d'échelle des transistors en nanomètres les rend plus vulnérables aux perturbations transitoires appelées *Single Event Transient* (SET) [139] et rend ainsi MTJ-cell plus sujet aux erreurs. Les SET peuvent avoir un impact sur plusieurs domaines où les communications sont essentielles, comme les satellites, l'espace et l'aéronautique.

Le chapitre 4 commence par quelques caractéristiques des technologies FDSOI. Ensuite, SET est discuté. Enfin, le MTJ et ses applications sont abordés.

***Fully Depleted Silicon-On-Insulator* (FDSOI)** Dans le processus FDSOI, une fine couche d'oxyde isole le canal et le volume. Grâce à cela, les effets indésirables liés au substrat flottant sont éliminés [141]. De plus, l'isolant formé par l'oxyde enterré (BOX) permet de réduire en profondeur la surface des diffusions de source et de drain. Par conséquent, la valeur des condensateurs de jonction du transistor diminue, conduisant à une meilleure consommation dynamique d'une porte logique de commutation par rapport à la technologie bulk. La capacité d'entrée réduite permet une vitesse accrue et une consommation d'énergie inférieure. De plus, l'utilisation des technologies FDSOI se traduit par de meilleures performances tout en maintenant de faibles fuites. Par conséquent, ils sont attrayants en raison de leurs caractéristiques haute vitesse/faible puissance et leur fiabilité a été largement étudiée [143–147, 171].

***Single Event Transient* (SET)** Le SET est un facteur important à prendre en compte pour la fiabilité des appareils, en particulier pour l'électronique spatiale [148]. Le SET résulte de la charge déposée lorsque des particules énergétiques ionisantes atteignent une région sensible du circuit. Les données stockées peuvent être retournées provoquant une erreur lorsqu'une charge suffisante est collectée.

***Magnetic Tunnel Junction* (MTJ)** Un MTJ se compose de deux couches ferromagnétiques séparées par la couche isolante MgO. La couche de référence a une direction de magnétisation inchangeable, tandis que la direction de magnétisation peut être modifiée dans la couche libre. Par conséquent, le champ magnétique détermine les propriétés électriques du MTJ. Pour utiliser les

MTJ on contrôle la différence de conductance, résultant des variations du champ magnétique dans les couches ferromagnétiques. Les orientations de magnétisation (m_z) des deux couches ferromagnétiques sont liées à un niveau de la résistance MTJ : faible résistance R_P à un état parallèle (P) et haute résistance R_{AP} à un état anti-parallèle (AP). Avec ces deux états stables du MTJ, il peut être facilement utilisé pour représenter la logique 0 ou la logique 1 [158–161].

Afin de contrôler les caractéristiques électriques de MTJs, certaines méthodes ont été développées pour changer leurs états stables. Les trois principaux mécanismes de commutation de magnétisation MTJ sont :

- *Spin Transfer Torque* (STT) ;
- *Voltage-Controlled Magnetic Anisotropy* (VCMA) ;
- *Spin-Orbit Torque* (SOT).

Un dispositif MTJ possède une excellente évolutivité, une faible consommation d'énergie et une endurance potentiellement infinie. De plus, les MTJs non actifs peuvent être complètement éteints sans perte de données, ce qui permet d'économiser de l'énergie, ce qui rend le MTJ adapté à plusieurs applications [135] telles que : Mémoire, Portes logiques, Table de vérité (*Lookup Table* - LUT), *Flip-Flop* (FF), *Full Adder* (FA), Comparateur, Convertisseur analogique-numérique (ADC), Générateur d'horloge non uniforme, Quantificateur intermittent adaptatif (AIQ), Capteurs, etc.

L'étude de SET a conduit à l'analyse des effets SET sur un comparateur dynamique sur la technologie 28 nm FDSOI CMOS (voir la Section 5.1). De plus, l'étude des applications MTJ présentées dans la littérature a conduit à l'étude des effets de SET sur un VCMA-MTJ-based MeRAM (voir la Section 5.2) et une mémoire spintronique NAND-Like (voir la Section 5.3).

B.5 Solutions Matérielles Proposées

Ce chapitre présente les approches de solutions matérielles proposées dans cette thèse. Les effets SET sur un comparateur dynamique sur la technologie 28 nm FDSOI CMOS, sur un VCMA MeRAM bit-cell, et sur La mémoire spintronique NAND-Like sont analysées dans les Sections 5.1, 5.2 et 5.3 respectivement. Ensuite, un ADC basé sur MTJ est proposé dans la Section 5.4.

Analyse des effets SET sur un comparateur dynamique sur la technologie 28 nm FDSOI CMOS Les effets SET sur un comparateur dynamique de la technologie 28 nm FDSOI CMOS sont étudiés. La sensibilité du circuit est simulée combinée à la polarité des entrées différentielles et aux phases de fonctionnement du comparateur. De plus, le *body-bias* et l'impact de la modulation du canal du transistor ont été analysés. Ces résultats ont été publiés dans [147]. L'analyse de l'impact SET permet de vérifier si le circuit est conforme aux exigences de l'application. Si le circuit n'est pas suffisamment robuste aux SET, les résultats Q_c permettent de classer les transistors et donc une refonte appropriée du circuit.

VCMA MeRAM *bit-cell* sur effets transitoires d'événement MTJ avec VCMA a été introduite pour obtenir un contrôle d'écriture pour une cellule de mémoire non volatile robuste avec un champ électrique ou une tension de commutation. La fiabilité de la MeRAM basée sur VCMA-MTJ peut être affectée par des perturbations environnementales car un rayonnement sur le transistor d'accès pourrait introduire des échecs d'écriture et de lecture dans la structure 1T- 1MTJ MeRAM *bit-cell*. Les effets de SET sur une VCMA-MTJ MeRAM dans une technologie 28 nm FDSOI CMOS sont étudiés. Ces résultats ont été publiés dans [200].

Les résultats montrent qu'une attention aux circuits entourant la génération d'impulsion d'écriture est nécessaire pour ne pas créer plus de points critiques dans le circuit avec une MTJ en termes de robustesse SET. Bien qu'un simple circuit basé sur MTJ soit envisagé, ces résultats indiquent que pour obtenir les avantages liés à la robustesse par rapport aux SET, une analyse détaillée et une attention doit être portée sur l'ensemble des composants et leur fonctionnement autour du MTJ sous peine de finir par générer un circuit aussi sensible que l'équivalent dans CMOS.

Analyse de fiabilité de la mémoire spintronique NAND-Like Cette section analyse la fiabilité de la mémoire spintronique NAND-Like. Ces résultats ont été publiés dans [202]. Le redimensionnement des transistors peut être une stratégie appropriée pour durcir la structure NAND-SPIN face aux SET. Malgré le surcoût de surface, le NAND-SPIN renforcé reste moins cher que SOT-MRAM (qui nécessite deux transistors par *bit-cell*) et une augmentation plus rapide du Q_c minimal que dans MeRAM basée sur VCMA-MTJ. En comparant au comparateur CMOS analysé auparavant, l'augmentation du Q_c minimal avec le redimensionnement des transistors indique que les circuits basés sur 1T1MTJ peuvent obtenir une meilleure protection en présence de SET.

Proposition de ADC basé sur MTJ Dans cette section, un ADC de k-bit basé sur MTJ et utilisant SOT pour changer l'état de MTJ est proposé. Les résultats ont été publiés dans [235]. Contrairement aux conceptions reportées dans la littérature, dans cette proposition, le mécanisme SOT est utilisé dans les deux phases de l'opération d'écriture. De plus, chaque MTJ a un port de lecture séparé améliorant la fiabilité de l'opération de lecture.

Le ADC de k-bit basé sur MTJ proposé contient n MTJs, $n-1$ résistances et $n+1$ NMOS, où $n = 2^k - 1$ comme le montre la Fig. B.3. Chaque NMOS connecté au MTJ respectif est également connecté à un circuit d'amplification de capteur (SA). Le courant d'entrée analogique I_{in} est converti en sortie numérique.

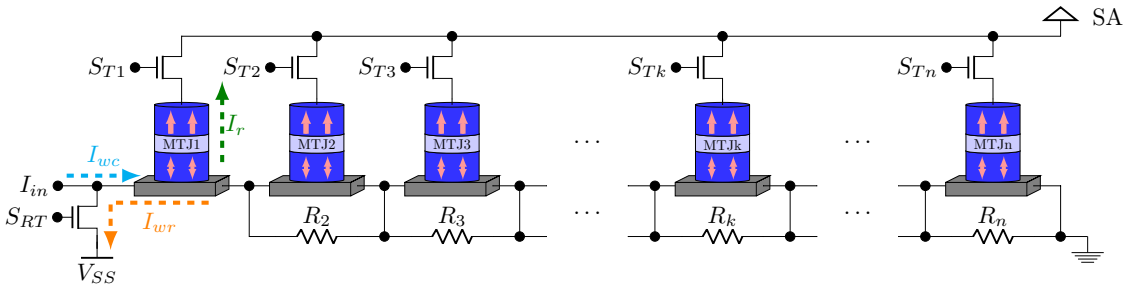


FIGURE B.3 – Architecture du k-bit ADC basé sur MTJ proposé.

La Fig. B.4 illustre le chronogramme des opérations d'écriture et de lecture sur MTJk. Comme l'on peut le remarquer, l'opération d'écriture comporte deux phases :

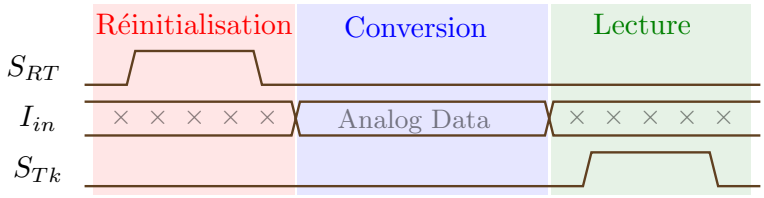


FIGURE B.4 – Diagramme de temps des opérations d'écriture et de lecture pour l'ADC basé sur MTJ proposé.

- Réinitialisation (*Reset*) : tous les MTJ sont initialisés à leur état AP. Pour ce faire, le transistor RT est activé et les transistors d'accès sont désactivés. Ensuite, un courant d'écriture I_{wr} passe par le HM.

- Conversion : dans cette phase, les transistors RT et d'accès sont tous bloqués. Par conséquent, un courant I_{wc} traverse le HM et les résistances. Seuls certains MTJ verront leur état changé en fonction du courant qui passe par le HM sous chaque MTJ. Un petit courant I_{wc}

changera les premiers MTJs (MTJ1, MTJ2, ...) en leur état P. Par conséquent, le courant d'entrée analogique I_{in} sera représenté par la quantité de MTJ commutés.

On peut remarquer que les deux phases de l'opération d'écriture utilisent le mécanisme SOT pour imposer l'état du MTJ.

Concernant l'opération de lecture, le transistor d'accès correspondant au MTJ qui sera lu est passant, et les autres sont bloqués. La lecture de l'état du MTJ se fait en comparant un courant de référence avec I_r. Dans l'ADC basé sur MTJ proposé, le I_r actuel ne passe pas par le HM de tous les MTJs. En d'autres termes, chaque MTJ a un port de lecture spécifique à travers lequel le courant I_r circulera comme illustré sur la Fig. B.5. La recherche binaire peut être utilisée pour optimiser le processus de lecture.

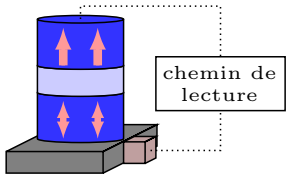


FIGURE B.5 – Structure MTJ avec le port de lecture.

Soit R_M la résistance du HM en dessous d'un MTJ, I_c le courant requis pour changer l'état du MTJ et I_d la différence de courant entre chacun niveau de l'ADC. Puisque MTJk ($k \neq 1$) a un diviseur de courant et que chaque MTJ est associé à un niveau ADC, les valeurs des résistances sont calculées comme (B.2) pour $k \geq 2$. Alors que I_d est lié aux caractéristiques ADC, I_c dépend des caractéristiques MTJ et HM.

$$R_k = \frac{R_M I_c}{(k-1)I_d} \tag{B.2}$$

L'ADC basé sur MTJ proposé conduit à une meilleure performance en termes d'efficacité énergétique par rapport plusieurs ADCs présentés dans la littérature.

Puisqu'un port de lecture séparé est connecté à chaque MTJ dans l'ADC basé sur MTJ, il y a une amélioration de la fiabilité de lecture par rapport aux autres ADCs présentés dans la littérature telle que l'ADC présenté dans [134] qui a une plus grande dépendance dans l'utilisation de HM aux opérations de lecture. De plus, le port de lecture séparé permet l'utilisation d'un circuit de lecture plus simple que celui requis dans [134, 220] qui nécessite des résistances de référence différentes.

Enfin, il convient de souligner que dans l'ADC basé sur MTJ proposé, tous les MTJs ont les

mêmes paramètres et un courant minimal est nécessaire pour changer l'état du MTJ indépendamment de la valeur du signal d'entrée analogique. Avec cela, les effets de variabilité du courant de commutation sont minimisés puisque cette variation est plus grande avec l'augmentation du niveau du courant de commutation.

Cas d'application Cette section traite de la détection de spectre large bande en utilisant un RMPI AIC. L'objectif est de simuler les conditions d'un AIC pour la récupération d'un spectre qui a une activité relativement faible, c'est-à-dire, un spectre parcimonieux en fréquence. Les simulations ont considéré l'analyse directe d'une bande de 3 GHz qui peut correspondre à une bande de base ou qui peut avoir été extraite de fréquences plus élevées dans un spectre. La rareté du spectre est illustrée par 4 sources indépendantes réparties aléatoirement dans la bande de 3 GHz. Les sources ont été générées avec symboles OFDM.

La métrique de performance est la probabilité de détection P_d (pourcentage de la bande occupée trouvé correctement). Les simulations ont été effectuées en faisant varier la résolution de l'ADC (nombre de bits N_r), le nombre de branches du RMPI AIC (M), le nombre d'échantillons (S) et N/M. Ces simulations montrent qu'il est possible d'utiliser un RMPI AIC dont l'ADC a une faible résolution en bits pour la détection de spectre large bande. Afin d'obtenir un dispositif à faible consommation et à haute fiabilité, des ADC basés sur MTJ et des transistors avec la technologie FDSOI peuvent être utilisés grâce aux bonnes caractéristiques des FDSOI et MTJ comme présenté tout au long de ce travail.

B.6 Conclusion et Perspectives

Ce chapitre résume chaque contribution et comprend quelques remarques finales sur le travail actuel et les perspectives.

La rareté et l'attribution inefficace du spectre limitent la capacité de transmission des données et le nombre d'utilisateurs. La radio cognitive a été considérée comme une solution à cette rareté du spectre qui constitue l'un des défis les plus importants de la communication sans fil. La détection de spectre est un problème fondamental pour la CR. Cette thèse portait sur la détection du spectre en particulier avec des approches pour la détection du spectre à large bande lorsque l'occupation du spectre peut être considérée comme parcimonieuse. Dans cet esprit, cette thèse s'est principalement concentrée sur les convertisseurs analogique-information, le MTJ et le SET.

Partant de l'état de l'art, les principales techniques de détection du spectre ont été étudiées et

résumées dans le Chapitre 2. Ensuite, la détection de spectre basée sur l'acquisition comprimée a été étudiée au Chapitre 3 et plusieurs algorithmes de récupération clairsemés ont été analysés dans [97].

Les défis liés à l'implantation matérielle de ces fonctions ont été présentés dans le Chapitre 4, en particulier l'impact d'un événement transitoire unique (SET). Ceci a conduit à l'analyse des effets du SET sur un comparateur dynamique utilisant la technologie 28 nm FDSOI CMOS. Les résultats ont montré que la vulnérabilité du circuit est fonction du temps de frappe, du transistor atteint, de la modulation du canal du transistor et du *body-bias*.

Afin de réduire la consommation et de rendre le circuit plus robuste aux SET, les caractéristiques et les applications des dispositifs MTJ ont été étudiées. Cela a conduit à l'analyse d'impact du SET sur une MeRAM basée sur VCMA-MTJ pendant le processus d'écriture. De plus, la vulnérabilité de la structure NAND-SPIN a également été étudiée en considérant le temps de frappe du SET.

L'étude des applications MTJ présentées dans la Section 4.4 a conduit à la proposition d'un ADC basé sur MTJ. Les performances de l'ADC proposé ont été analysées pour une résolution de 3 bits et 4 bits avec la technologie 28 nm FDSOI CMOS. Cette proposition a obtenu de bons résultats en termes de fréquence maximale, d'énergie et de consommation d'énergie par rapport aux autres ADCs présentés dans la littérature.

Les résultats de cette thèse mettent en exergue la pertinence de l'utilisation de ADC basé sur MTJ dans un AIC pour la détection de spectre large bande comme alternative à un ADC avec fréquence d'échantillonnage élevé.

La plupart des travaux couverts par cette thèse ont été publiés dans des conférences et des journaux du domaine. Ces publications sont répertoriées dans l'annexe A.

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ECOLE
DOCTORALE

Titre : Approches Basse Consommation et Résistantes aux Rayonnements pour le Sondage du Spectre

Mots clés : Radio Cognitive ; Solutions Matérielles ; Magnetic Tunnel Junction

Résumé : Les progrès de la technologie ont permis une forte augmentation du nombre d'utilisateurs et de la quantité d'informations à transmettre. Ces dernières années, la demande de taux de téléchargement élevés, de connexions massives, de faibles latences et d'efficacité énergétique a augmenté, principalement en raison de la multiplication des appareils IoT et de l'introduction de l'industrie 4.0. Cela a conduit à une augmentation significative de la demande du spectre pour accueillir de nouveaux services ou pour améliorer les services existants. Une des alternatives pour traiter ce problème est l'utilisation de radios cognitives (CR). Elles sont capables de détecter le spectre et de voir quelles bandes ne sont pas actuellement utilisées. Parmi les divers défis liés à la CR, la détection du spectre est l'une des fonctions les plus importantes de ces radios. La détection de spectre à large bande présente plusieurs défis, notamment en ce qui concerne les antennes et le traitement d'un grand nombre de données. Cependant, en plusieurs instants, le spectre peut être considéré comme parcimonieux, ce qui permet l'utilisation de l'acquisition comprimée (CS) afin de réduire la quantité d'échantillons nécessaires et ainsi réduire les ressources de traitement. En termes de matériel, l'utilisation de CS peut être traduite en convertisseurs analogique-information (AIC) au lieu d'implémenter des convertisseurs analogique-numérique (ADC) avec des taux d'échantillonnage élevés. De plus, il est intéressant de mettre en œuvre des dispositifs basse consommation. La réduction d'échelle des transistors en nanomètres permet de réduire la consommation et la surface. Cependant, d'autres alternatives ont été étudiées pour diminuer la puissance liée aux courants de fuite. Parmi ces alternatives, l'utilisation de dispositifs *Magnetic Tunnel Junction* (MTJ) est considérée prometteuse. De plus, les transistors de réduction d'échelle rendent les circuits plus sensibles au SET, et bien que le MTJ soit plus robuste aux rayonnements que les transistors, il est nécessaire d'étudier l'impact de ces derniers et comment le réduire. Dans ce contexte, cette thèse se concentre sur l'analyse des effets SET et l'utilisation des MTJ dans un AIC pour effectuer la détection de spectre large bande. Les principales contributions de cette thèse sont l'analyse des effets SET dans un comparateur qui est l'un des principaux composants d'un ADC ; l'analyse des effets SET dans les structures MTJ, et la proposition d'un ADC basé sur MTJ qui peut être utilisé dans un AIC pour effectuer la détection de spectre large bande.

Title : Low-power and Radiation Resilient Approaches for Spectrum Sensing

Keywords : Cognitive radio ; Hardware Implementation ; Magnetic Tunnel Junction

Abstract : The advancement of technology has enabled a great increase in the number of users and the amount of information to be transmitted. In recent years, the demand for high download rates, massive connection, low latencies and energy efficiency has increased, mainly due the multiplication of IoT devices and the introduction of industry 4.0. This has led to a significant increase in demand for the frequency spectrum to accommodate new services or to improve existing ones. One of the alternatives to deal with this problem is the use of cognitive radios (CRs). They are able to sense the spectrum and see which bands are not currently being used. Among the various challenges related to CR, spectrum sensing is one of the most important and one of the primary functions of these radios. Wideband spectrum sensing presents several challenges, including antennas and processing a lot of data. However, in several moments the spectrum can be considered sparse allowing the use of compressive sensing (CS) in order to reduce the amount of samples required and thereby reducing processing resources. In terms of hardware, the use of CS can be translated in analog-to-information converters (AICs) instead of implementing analog-to-digital converters (ADCs) with high sampling rates. Furthermore, it is interesting to implement low-power devices. Downscaling transistors to nanometers helps to reduce consumption and area. However, other alternatives have been studied to decrease the leakage power. Among these alternatives, Magnetic Tunnel Junction (MTJ) has been very promising. In addition, the downscaling transistors makes circuits more sensitive to SET, and although MTJ is more robust than transistors to radiation, it is necessary to study how this impact is and how to reduce it. In this context, this thesis focuses on the SET effects analysis and MTJ applications which can be used in an AIC to perform the wideband spectrum sensing. The main contributions of this thesis are the analysis of SET effects in a comparator which is one of the main components of an ADC ; analysis of SET effects in MTJ structures, and the proposition of a MTJ-based ADC which can be used in an AIC to perform the wideband spectrum sensing.

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