



HAL
open science

Impact of noise and electromagnetic coupling in sequential 3D technologies: study, modeling and impact on circuit performance

Petros Sideris

► **To cite this version:**

Petros Sideris. Impact of noise and electromagnetic coupling in sequential 3D technologies: study, modeling and impact on circuit performance. Micro and nanotechnologies/Microelectronics. Université Grenoble Alpes [2020-..], 2021. English. NNT: 2021GRALT029 . tel-03506283

HAL Id: tel-03506283

<https://theses.hal.science/tel-03506283v1>

Submitted on 2 Jan 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITE GRENOBLE ALPES

Spécialité : **Nano Electronique et Nano Technologies**

Arrêté ministériel : 25 mai 2016

Présentée par

Petros SIDERIS

Thèse dirigée par **Gilles SICARD**, Ingénieur de recherche, HDR, **CEA-LETI**, et encadrée par **Christoforos THEODOROU**, chargé de recherche, **CNRS**, laboratoire **IMEP-LAHC** et **Perrine BATUDE**, Ingénieure de recherche, **CEA-LETI**

préparée au sein du **CEA-LETI** et de l'**IMEP-LAHC**
dans l'**École Doctorale Electronique, Electrotechnique, Automatique et Traitement du Signal (EEATS)**

Impact de bruit et couplages électromagnétiques dans les technologies 3D séquentielles : Etudes, modélisation et parade

Thèse soutenue publiquement le **4 mars 2021**,
devant le jury composé de :

Pr. Pierre MAGNAN

Professeur des Universités, ISAE, Toulouse (Président)

Pr. Cristell MANEUX

Professeure des Universités, laboratoire IMS, université de Bordeaux (Rapporteur)

Pr. Per-Erik HELLSTRÖM

Professeur des Universités, KTH, Stockholm, Suède (Rapporteur)

Pr. Gérard GHIBAUDO

Directeur de recherche, CNRS, laboratoire IMEP-LAHC, Grenoble (Examineur)

Dr. Gilles SICARD

Ingénieur de recherche HDR au CEA-Leti, Grenoble (Directeur de thèse)

Dr. Christoforos THEODOROU

Chargé de recherche, CNRS, laboratoire IMEP-LAHC, Grenoble (Co-encadrant)

Dr. Perrine BATUDE

Ingénieure de recherche au CEA-Leti, Grenoble (Co-encadrante)



“Per aspera ad astra”

ACKNOWLEDGEMENTS

I carried out my three years thesis research at IMEP-LAHC and CEA-LETI. During this time, I had the opportunity to meet experts from different laboratories, who were always willing and benevolent to help me and share their knowledge with me. Hence, I would like to start by thanking all these people who helped me deepen my knowledge within the complex subject of this thesis and gain many new skills. Alexandre Siligaris, your contribution to my thesis has been very important, thank you for the significant remarks you have made in Chapter 4 of my thesis. Joris Lacord and Josep Segura, thank you for the fruitful discussions.

I would like also to thank the members of my jury, Pr. Cristell Maneux, Pr. Per-Erik Hellström, Pr. Pierre Magnan and Pr. Gérard Ghibaudo, for reading my manuscript, attending the defense and for all the significant remarks that helped me improve the quality of this manuscript. It was an honor having you all in my jury.

I would certainly like to express my warmest gratitude to my supervisors. Gilles Sicard, smart imager expert, you were always encouraging me in all steps of this thesis and I really enjoyed working in your lab. You were very supportive and eager to help me in every aspect of this thesis.

Perrine Batude, process integration expert, I would like to thank you for all your support, you always provided stimulating discussions. I am so grateful you gave me the opportunity to work in this technology. Thank you also for challenging me and pushing me to enhance my communication skills as I have always been more of an introvert.

Christoforos Theodorou, device noise expert, my gratitude is beyond words. You have set an example for me of excellence as a researcher, mentor and instructor. Thank you for guiding, encouraging and advising with a good humor always. Your constant passion and enthusiasm for research always motivated me to overcome myself. Thank you all, for the guidance and the rehearsals and review of papers/manuscript/presentations especially during the “end-of-contract” period. I hope I will have the pleasure to work with you again in the future!

I am also very grateful to my friends, especially Spiros, Manos, Angeliki, Miltos & Despina, who supported me so much through all these years. I have so many wonderful memories from you that will accompany me my whole life. Spiros, my best friend, your support and mental encouragement

was very important for me to carry out this work! I should not forget to mention also all the people in CEA-LETI and the people in the IMEP-LAHC laboratory that I interacted with, whether it was in meetings, lunch, coffee or just discussions in the office.

I am incredibly grateful for those of you who stood by to support me along the way. Thank you for helping me during my PhD journey.

Lastly, I would like to thank of course my dearest family in Greece for their support throughout all the years of my education. Thank you for your unconditional support and constant encouragement!

Sincerely

Petros Sideris

ABBREVIATIONS

<i>Acronym</i>	<i>Definition</i>
3DSI	3D Sequential Integration
3DCO AR	3D Contact Aspect Ratio
AC	Alternative current
APS	Active Pixel Sensors
AR	Aspect Ratio
BG	Back Gate
BEOL	Back End Of Line
BF	Body Factor
BOX	Buried OXide
BSI	Back Side Illumination
BTI	Bias Temperature Instability
CCD	Charge Coupled Device
CDS	Correlated Double Sampling
CG	Conversion Gain
CIS	CMOS Image Sensors
CMOS	Complementary Metal Oxide Semiconductor
CNF	Carrier Number Fluctuations
CNF/CMF	Carrier Number Fluctuations with Correlated Mobility Fluctuations
C-V	Capacitance-Voltage
DC	Direct Current
DIBL	Drain Induced Barrier Lowering
DPS	Digital Pixel Sensor
DR	Dynamic Range
DUT	Device Under Test
EOT	Equivalent Oxide Thickness
FBB	Forward Back Bias
FDSOI	Fully Depleted Silicon-On-Insulator

FEOL	Front End Of Line
GP	Ground Plane
HK	High-K
HT	High-Temperature
HV	High-Voltage
iBEOL	Intermediate Back End Of Line
ILD	Inter-Layer Dielectric
ITRS	International Technology Roadmap for Semiconductors
I-V	Current-Voltage
LFN	Low Frequency Noise
LT	Low-Temperature
LV	Low-Voltage
MG	Metal Gate
mmW	Millimeter wave
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NBTI	Negative Bias Temperature Instability
PBTI	Positive Bias Temperature Instability
PSD	Power Spectral Density
PPD	Pinned Photo-Diode
RBB	Reverse Back Bias
RF	Radio frequency
RO	Ring Oscillator
RS	Row Selector
RST	Reset transistor
RTS	Random Telegraph Signal
S/D	Source/Drain
SCE	Short-Channel Effects
SF	Source Follower
SN	Sense Node
SOI	Silicon-On-Insulator

SRAM	Static Random-Access Memory
TB	Thermal Budget
TCAD	Technology Computer Aided Design
TG	Transfer Gate
TEM	Transmission Electron Microscopy
TSV	Through Silicon Via
UTBB	Ultra-Thin Body and Buried oxide
VTC	Voltage Transfer Characteristics

CONTENTS

Acknowledgements	4
Abbreviations	6
CHAPTER 1 Introduction.....	14
1.1 A brief historical review of CMOS technology	14
1.2 3D integration technologies overview	16
1.3 Electrical measurement and analysis methods	20
1.4 Challenges & Motivation	21
1.5 State-of-the-art studies on electromagnetic coupling in 3D technologies	23
1.6 Main contributions and thesis outline	24
CHAPTER 2 Physics of MOSFETs and coupling effects	28
2.1 The MOSFET transistor	28
2.1.1 Metal-Oxide-Semiconductor Capacitor operation regimes	29
2.1.2 Definition of MOSFET electrical parameters	32
2.1.3 Body effect	34
2.1.4 Short-channel effects	34
2.2 The FD-SOI device architecture	36
2.2.1 SOI substrate technology	36
2.2.2 FDSOI device geometry	36
2.2.3 Front/Back interface charge coupling	38
2.3 Electromagnetic coupling and transfer of energy between electrical components	40
2.4 Noise sources in devices and circuits	41
2.4.1 Intrinsic noise sources	42
2.4.2 Extrinsic noise sources	45
2.4.3 Noise coupling in circuits.....	50
2.5 Conclusion	54
CHAPTER 3 Investigation of 3DSI electromagnetic coupling effects at a device level	56

3.1 3D sequential structure description	56
3.1.1 Mixed-signal opportunities by the use of 3DSI	58
3.1.2 3DSI process flow for digital devices.....	59
3.1.3 Characteristic dimensions and performance of 3DSI devices under test	61
3.1.4 Structure layout of 3DSI devices under test	61
3.2 Impact of DC coupling on top/bottom device performance	63
3.2.1 Experimental results.....	63
3.2.2 Simulation results.....	70
3.2.3 Impact of static coupling on the performance of top-tier digital devices ($V_{DD}=1V$)	79
3.2.4 Impact of static coupling on the performance of top-tier analog devices ($V_{DD}=2.5V$).....	82
3.3 Impact of AC coupling on top/bottom device performance	84
3.3.1 Small-signal analysis	85
3.3.2 Transient response of top-tier devices to bottom-tier device aggressor signals.....	91
3.3.3 Inter-tier versus intra-tier coupling.....	95
3.4 Conclusion	97
CHAPTER 4 Coupling effects in 3DSI circuits: Impact on operation and proposed solutions	98
4.1 Impact of inter-tier coupling on circuit operation.....	98
4.1.1 2-bitcell Sequential 3D SRAM (Digital on Digital case)	100
4.1.2 RO stacked on top of an analog tier (Mixed-Signal/RF on Analog case)	109
4.1.3 RO stacked on top of a digital tier (Mixed-Signal/RF on Digital case)	110
4.2 Methods and techniques to mitigate inter-tier coupling effects in 3DSI	112
4.2.1 Critical dimensioning of 3DSI structures and 3D design rules.....	112
4.2.2 Inter-tier shielding through GP: challenges and solutions	117
4.3 Conclusion	129
CHAPTER 5 Analysis of coupling effects in a 3DSI CMOS Image Sensor	130
5.1 Introduction.....	130
5.2 Principles and operation of a CMOS imager.....	131
5.2.1 CIS standard architectures	131

5.2.2	Pixel metrics	133
5.2.3	Pixel noise parameters	137
5.2.4	Process integration optimization	140
5.3	Inter-tier Coupling at Device Level	142
5.3.1	Simulation Setup	142
5.3.2	Impact on electrical parameters	143
5.4	Inter-tier Coupling at Pixel Level	145
5.4.1	Read-out circuit block and pixel metrics.....	145
5.4.2	Impact of TG coupling on pixel electrical parameters	147
5.4.3	Inter-tier GP necessity	149
5.5	Conclusion	150
CHAPTER 6	Parasitic extraction and modeling of coupling effects in 3DSI	152
6.1	Parasitic extraction of lumped coupling elements in 3DSI.....	152
6.1.1	Definition of coupling capacitances in 3DSI.....	153
6.1.2	Effect of 3D contacts on coupling capacitances	157
6.2	Coupling-induced V_{TH} shift modeling for stacked devices.....	163
6.2.1	Charge-coupling factor expression for long-channel top-tier devices	164
6.1.1	Modeling the effective ILD capacitance of stacked devices ($C_{ILD,eff}$).....	170
6.3	Inter-tier dynamic coupling effects modeling	184
6.4	Inter-tier GP shielding modeling.....	186
6.4.1	DC modeling of inter-tier GP – Impact on coupling induced ΔV_{TH} of the stacked devices	186
6.4.2	AC modeling of inter-tier GP	190
6.5	Conclusion	194
CHAPTER 7	Conclusions and perspectives	196
BIBLIOGRAPHY	200
List of publications	216
Abstract	218
Résumé	220

CHAPTER 1

INTRODUCTION

This chapter aims to provide a brief overview of the topic of the thesis. We will start by exploring the evolution of CMOS technology and the prevailing future trends. Afterwards, the three-dimensional integration technologies will be presented, focusing on the sequential 3D integration. Then, the analysis methods and tools that helped to carry out this work will be outlined. Finally, the challenges that motivated me to study this topic will be presented, along with the major contributions of this thesis to the state of the art.

1.1 A brief historical review of CMOS technology

Since the early 1960s, when the first metal-oxide-silicon field effect transistor (MOSFET) was discovered, it has become the driving force in electronics. Digital integrated circuits nowadays utilize billions of MOSFETs to implement complex systems on the same chip (System on Chip - SoC) with great computing power, facilitating life and boosting the development of modern societies. The increasing need for high performance, accompanied with low power consumption and cost reduction, has led to the continuous miniaturization of these devices [1].

“Moore’s Law” has been the guiding light for the evolution of microelectronics and in particular of the MOSFET transistor until nowadays. It relies on the predictions made by Gordon Moore about the density of integrated components in a chip following an exponential trend [2].

Unlike its name, “Moore’s Law” was in fact an empirical relationship based on the financial cost reduction per components of integrated circuits every year. Nevertheless, the increase of the integration density implies the dimension scaling of the components, which by turn reduces their gate delay and power consumption.

However, the microelectronics industry has been facing many challenges arising by the ongoing dimensional scaling of the electronic components. These challenges set barriers to “Moore’s Law” and emerge from several aspects of the device manufacturing such as:

- The need for better electrostatic control of the device channel by its gate electrode. It is crucial that the transistor operates as a switch in digital design, therefore it must always approximate the ideal behavior [3].
- The device must facilitate the flow of the current without posing obstacles and reducing the carrier mobility, when it is in the on-state [3].
- The previous is also true for the interconnections, which must allow the maximum current density to flow. However the device miniaturization has impacted negatively the performance of interconnect wires [4]–[7]. As the wires cross-sections, their pitch and length to traverse a chip increases, the resistance and the capacitance of these lines are also rising resulting in a significant increase in signal propagation (RC) delay. As a consequence the performance of advanced ICs is limited [4]–[7].
- The limits posed by lithography and the unavailability of sufficiently small light wavelengths to pattern the minimum feature size [8].

Fortunately, research in device engineering in recent years has led to new device architectures comprised of innovative and efficient materials, or structure designs. Planar transistors that have been used for years faced certain limitations with scaling due to Short-Channel-Effects (SCE).

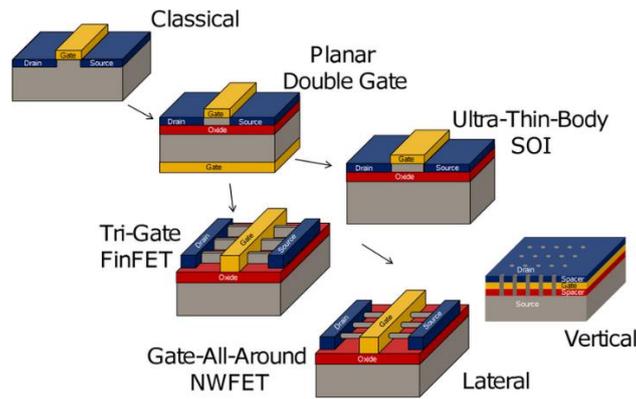


Fig. 1.1 Evolution of the Field Effect Transistor (FET) Architecture (Courtesy of [9]).

For that reason, device architectures as FinFETs, Fully-Depleted Silicon-On-Insulator (FD-SOI) and more recently Gate-All-Around (GAA) emerged offering approximately ideal electrostatics with the advantage of further dimensional scaling (Fig. 1.1).

Moreover, the use of materials such as High-K (HK) dielectrics permit the increase of the gate capacitance, mitigating problems resulting from ultrathin gate dielectrics such as the high gate leakage current due to direct tunneling of electrons through the SiO₂, a difficulty in manufacturing ultra-thin films, and the reliability of SiO₂ films against electrical breakdown [10]. On the other hand, Metal Gates (MG) are extensively used between the gate electrode, made out of degenerately doped polycrystalline silicon and the gate dielectric, adjusting the threshold voltage of the device by its work function while providing a higher carrier density and a depletion depth of less than one Angstrom [10].

1.2 3D integration technologies overview

Despite the development of new device architectures, capable of overcoming scaling issues, Moore's law is running out of steam and a potential end is envisioned. The latter is mainly because the feature size of the devices is approaching the fundamental limit of an atom. The foreseeable reach of Moore's Law limits, the increased needs in terms of performance, space saving and low power consumption as well as the growing menace of RC delay in recent times led in the 80's to the concept of integrating functionalities in three-dimensional modules [11]–[17]. These constitute a System in Package (SiP) combining conventional digital technologies (processor, memory controller, graphics solution, inputs / outputs, network connections, microsystems electromechanical) fabricated in different processes.

Conventional planar integration can be considered as two-dimensional. Thus, three-dimensional integration refers to the stacking of integrated circuit layers, interconnected vertically. The dominant approaches for three-dimensional integration in a single package can be encapsulated in 2 categories: parallel and sequential. The former term is referring to a method where the two wafers are processed separately and stacked -and contacted- afterwards (Fig. 1.2 (a)). In that case the alignment is made during the bonding and its $3\text{-}\sigma$ error is nowadays around 200nm [18]. In brief, the $3\text{-}\sigma$ error accounts for nearly 100% of the total alignment variation and is determined by calculating the standard deviation of the normal (Gaussian) distribution of the variation and multiplying it by three. There are several types of wafer bonding, the most prominent ones being copper-to-copper (Cu-to-Cu) and Hybrid bonding and Through-Silicon Via (TSV).

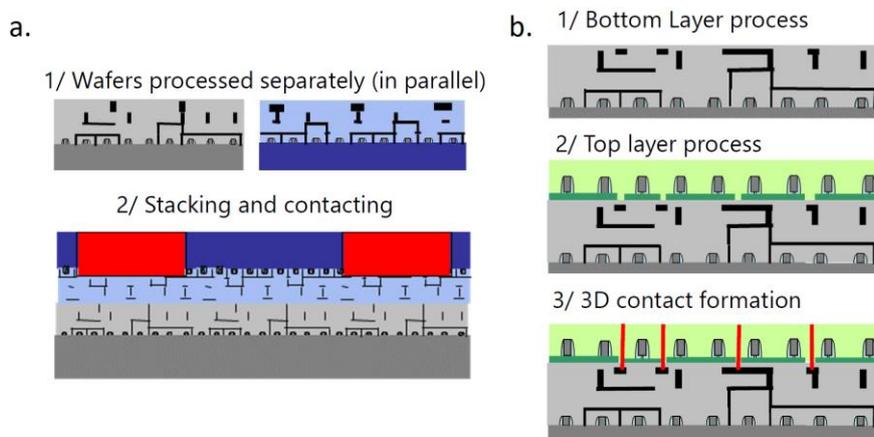


Fig. 1.2 Parallel (a) versus Sequential (b) 3D integration.

On the contrary, 3D sequential integration technology (3DSI - also named 3D monolithic integration or 3D VLSI) refers to the vertical stacking of active devices that are processed sequentially, i.e. each tier of devices is processed over a pre-patterned one (Fig. 1.2 (b)). This imposes that the alignment is made by lithography and the $3\text{-}\sigma$ error is around 5nm for a 28nm node [19]. Consequently, 3DSI can offer the highest density of vertical interconnects ($>5 \times 10^6$ 3D via/mm² in [20] and up to 10^8 3D via/mm² in [19], [21]), when compared to the other alternatives [22], [23], as shown in (Fig. 1.3).

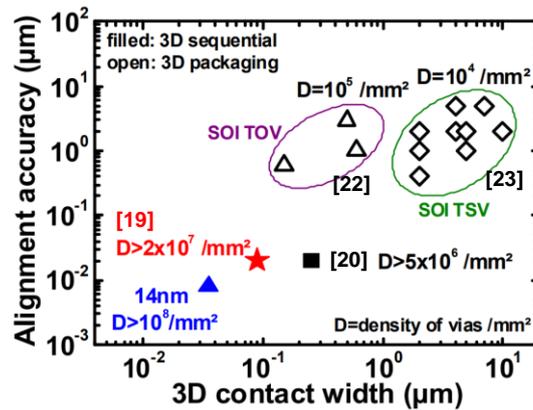


Fig. 1.3 Alignment capability versus 3D contact width in parallel and sequential integration (adopted from [19]).

There are multiple levels of partitioning a circuit following a three-dimensional integration: core-level, block-level, gate-level and ultimately transistor-level partitioning (Fig. 1.4). The latter, being the last one in the granularity scale can be realized exclusively with 3DSI. Furthermore, 3DSI is the only 3D technology to enable partitioning with all granularity scales.

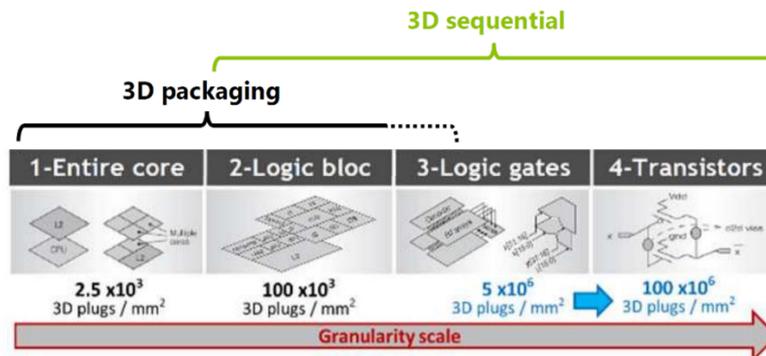


Fig. 1.4 Partitioning types in three-dimensional integration.

3DSI offers plenty of opportunities. Traditionally, the main virtue resulting from three-dimensional integration has been on the “More Moore” direction, attributed to the drastic decrease in the length of interconnects in an integrated circuit. Indeed, as shown in Fig. 1.5, assuming a planar integrated circuit with an area A , the longest interconnect (i.e., the line between the points X and Y) has a length $L_{\max} = 2\sqrt{A}$. Partitioning the same circuitry in two layers, each having an area of $A/2$, the length of the longest interconnect is now $L_{\max} = \sqrt{2A}$.

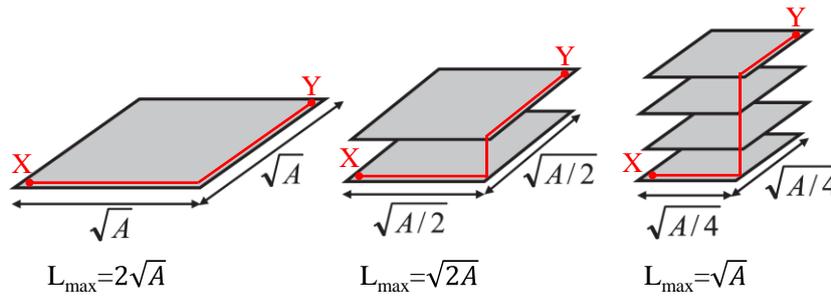


Fig. 1.5 Reduction in wire length where the original 2-D circuit is composed of two and four tiers.

Following the same logic, increasing the number of layers to four, the area of each die is further reduced to $A/4$, and the longest interconnect would have a length of $L_{\max} = \sqrt{A}$. By this simplified example it can be seen that there is a significant reduction of the wiring length and consequently the interconnection RC delay, leading to considerable advantages over conventional planar integration. Specifically, it has been reported that for a two-tier 3DSI there is 50% area reduction, 20% power limitation and 26% performance boost owing to the interconnect length reduction [24], [25]. Consequently, 3DSI has been envisioned as an alternative to the dimensional scaling of devices which is reaching its limits.

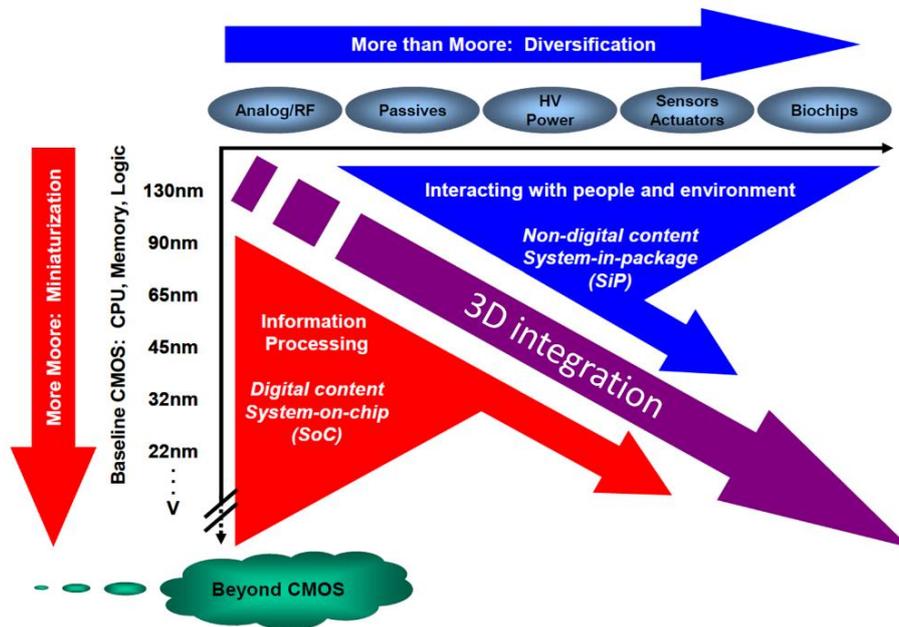


Fig. 1.6 The trends of “More than Moore” as compared to “More Moore” [26].

Nowadays, the versatility of applications that can be integrated in each sequential tier is emphasized towards the “More than Moore” direction. The latter enables the possibility to integrate heterogeneous complex systems with a large number of functionalities in a reduced form factor,

while increasing the circuit performance (in terms of enhanced bandwidth and reduced power consumption) as shown in Fig. 1.6.

A highly anticipated application within the More than Moore approach is the smart sensors which embed the sensor interface with all the processing and memory elements stacked on top of it. In this manner, applications fabricated in different technologies that are connected with low-latency vertical interconnections, enable the acceleration of the signal processing in a reduced form factor. An example of that is the smart imager that incorporates pixels with stacked analog and digital processing units as illustrated in Fig. 1.7.

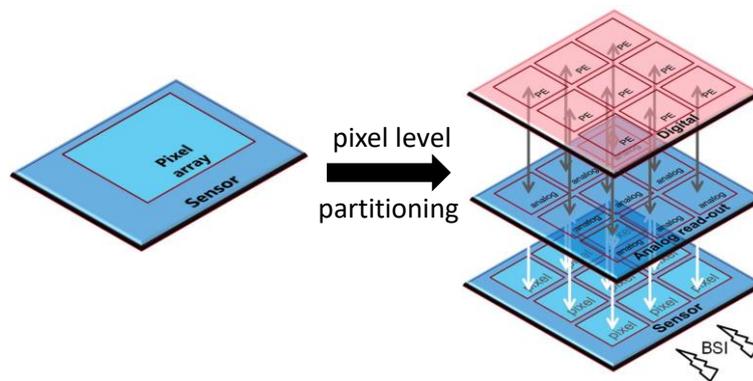


Fig. 1.7 Partitioning a pixel of an image sensor through 3D heterogeneous integration [27].

Although 3D stacking technologies are widely used for 3D CIS [28], [29], constraints of traditional 3D stacking alignment capabilities forbid the more aggressive pixel miniaturization required for future generations of CIS [30], [31]. The feasibility of Back-Illuminated CIS with miniaturized pixels realized in 3DSI has been investigated in [31], where a 44% increased photodiode area for 1.4 μm pitch was reported owing to the 3D partitioning at the pixel level. Moreover, 3DSI is the dominant pathway for pixel partitioning with pitch in the 1 μm range [32].

1.3 Electrical measurement and analysis methods

For the purpose of this study, electrical measurements were performed on 3D sequentially integrated wafers, processed with the CoolCube™ technology in CEA-LETI (Fig. 1.8).

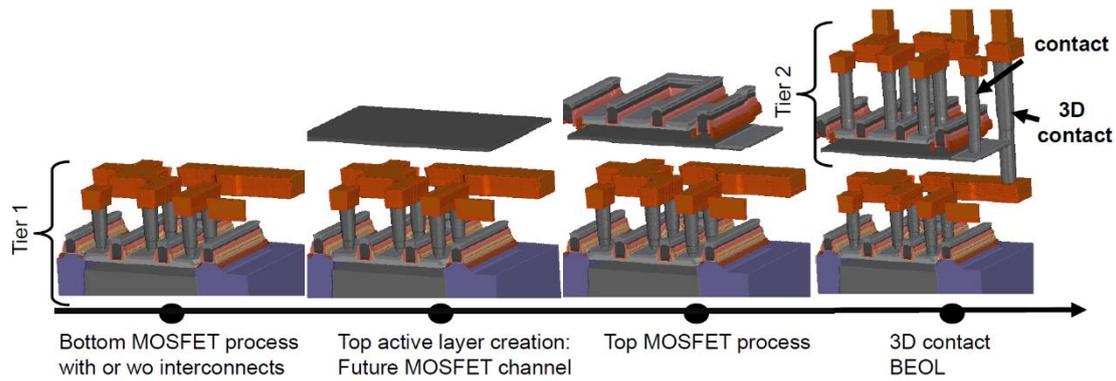


Fig. 1.8 CoolCube™ technology process flow [21].

The simulation study was conducted with the aid of leading EDA tools. For the electrostatic coupling analysis, numerical simulations were performed using Silvaco ATLAS [33], a generic TCAD tool for physically-based two (2D) and three-dimensional (3D) simulation of semiconductor devices. Additionally, Silvaco CLEVER [34] was used to extract the parasitic capacitances within the monolithic 3D structures. This tool is a field solver, intended for complex arbitrary structures where layout effects dominate, providing accurate results in a sufficient amount of time.

Due to the small electrical size of the structures simulated (i.e., the ratio between the largest distance between two points in the structure divided by the wavelength of the electromagnetic fields) being in the range up to 1/10, quasi-static formulations have been used to carry out this study. By using this approximation, the wave propagation delays are small enough to be neglected. Hence, even for frequencies up to the GHz regime, quasi-static tools provide accurate description of the coupling fields without the need of dedicated high frequency simulations. Therefore, the above-mentioned simulation tools are adequate for an accurate analysis particularly in the low-frequency domain. Yet, Ansys HFSS (High Frequency Electromagnetic Field Simulation) [35], a full-wave EM simulator that predicts non-quasistatic effects, has been utilized for the validation of the TCAD simulations in the high-frequency domain.

Lastly, the circuit simulations were performed within the Cadence Virtuoso Platform [36] using a parametrized version of the Leti-UTSOI model [37]. The proper parametrization of the model was employed to reproduce the experimental behavior and also to include the electrostatic coupling via the Back Gate (BG) of the transistor model.

1.4 Challenges & Motivation

The primary and main challenge of Monolithic 3D integration is associated with the fabrication of the top active layer (or layers) in such manner to preserve the electrical characteristics of the bottom one. Therefore, there is a temperature barrier (Thermal Budget (TB)) in order to avoid the degradation of the bottom tier's device, therefore the classical processing steps for the top tier's device fabrication are forbidden. To cope deal with this obstacle, the TB of the top devices is kept below 500°C to preserve the bottom FET from any degradation [19], [21].

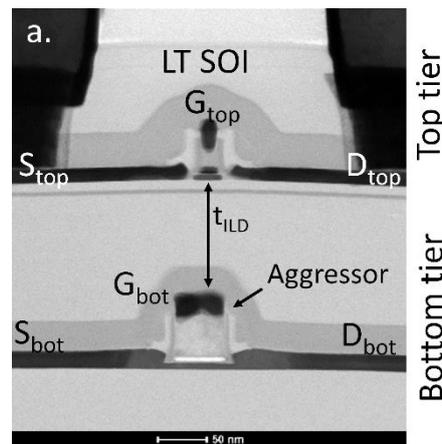


Fig. 1.9 TEM cross-section of two stacked transistors fabricated in 3DSI.

Furthermore, the different tiers are linked with 3D contacts, as shown in Fig. 1.10, which has limits in its aspect ratio (AR). This type of contact is a conventional one (Tungsten plug in oxide), however it has a greater height, predominantly defined by the ILD thickness (illustrated in Fig. 1.9). The AR of the 3D contact is expressed as

$$AR_{3DCO} = \frac{W_{3DCO}}{H_{3DCO}} \quad (1-1)$$

where W_{3DCO} is the width of the 3D contact which scales with the stacked device technology and H_{3DCO} is its height. Due to limits imposed by etching, the shape of a standard and 3D contacts is a trapezoid, thus a high AR reduces its bottom-end area. This by turn limits the maximum allowed current density, hence the lowest possible AR is preferable. An AR close to the one of standard contact, is required nowadays in terms of processing, hence the solution to achieve that is to keep the ILD thickness below 350nm.

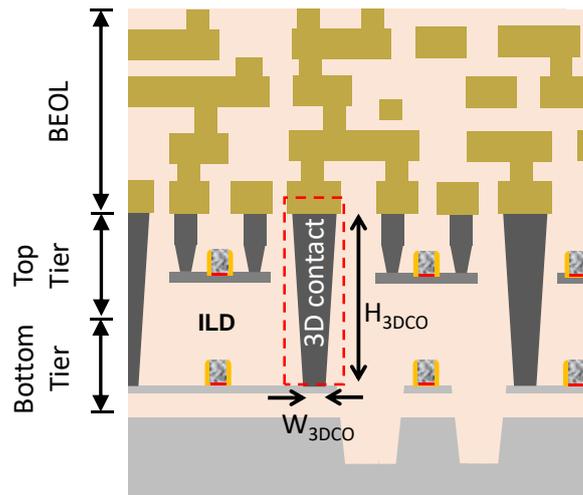


Fig. 1.10 Schematic cross-section view of 3DSI scheme indicating the characteristic dimensions of a 3D contact.

Another significant challenge of this technology, which is also the topic of this thesis, is the danger of electromagnetic interference between the sequential tiers. As explained previously, the ILD separating the top-tier device from the bottom one is very thin (few hundreds of nm), so that a good 3D contact AR is preserved. Therefore, the ILD can become a pathway for DC and electromagnetic coupling between adjacent tiers, limiting their performance as a result, or shifting the circuit's operating point.

1.5 State-of-the-art studies on electromagnetic coupling in 3D technologies

The design of systems in a single chip is one of the current obstacles in the semiconductor industry. Numerous compatibility issues in terms of materials, process integration and functionality, emerge in this contemporary scheme. Over and above, associating circuits of different nature, functioning and operating frequency range within the same chip, and more importantly placed at close distances, is a major challenge.

It is well known from conventional planar integration that the design of circuits operating within a highly noisy environment is extremely critical and presents many challenges. To minimize the noise impact on the sensitive active parts of a circuit, the solutions often consist in oversizing the critical distances between the functional blocks. However, these solutions limit the benefits of the technological advances (form factor and interconnection delay reduction). For these reasons, the characterization and modeling of noise coupling is of increasing interest.

In the general context of 3D integration, numerous studies have been reported regarding the electromagnetic interference between sensitive parts of the chip, however the majority of them

concerns parallel integration. In particular, TSV to active device coupling has been extensively characterized [38]–[41] and modeled [42]–[47] whereas its impact on the device and circuit performance has been in-depth analyzed in several studies [41]–[44], [46], [48]–[50].

On the other hand, to date there is poor amount of literature concerning coupling between the different tiers and particularly active devices in sequential 3D integration. Electrostatic coupling effects in 3DSI have been already presented in principle [51]–[56] and experimentally verified [57], whereas performance analysis taking into account the impact of electrostatic coupling has been performed in [52], [55], [58]–[61]. However, these studies cannot provide significant conclusions about the critical dimensioning of the stacked devices. Moreover, they consider homogeneous integration (specifically the tiers are comprised exclusively of digital circuits) and more importantly they partition the circuit in different tiers of 3DSI.

Several modeling considerations have been reported in [44], [62] concerning capacitive coupling in TOV technology. This process scheme is similar to 3DSI since it refers to stacked SOI devices separated by an oxide medium with Through-Oxide-Vias (TOVs) being the vertical contacts. The models reported evaluate the coupling capacitances formed between TOVs and active devices placed at the upper tiers, however they cannot evaluate the coupling impact between stacked devices. Nonetheless, although some modeling considerations are reported in [59]–[61] for the coupling between active devices in monolithic logic circuits, these models rely mainly on parasitic extraction and don't predict the impact of arbitrary geometric configurations and scaling of the devices (layout effects).

Lastly, solutions to coupling effects in 3DSI have also been considered in [63], [64], where the inter-tier shielding methods are investigated. Additionally, [64] experimentally presents their technological achievement on a buried metal line, functioning as a shielding layer between two tiers of a 3DSI scheme.

1.6 Main contributions and thesis outline

This thesis aims to provide a deep understanding of the underlying physical mechanisms responsible for the electromagnetic coupling between the different tiers in 3DSI as well as a complete study how these coupling effects may impact a circuit's operation. For the latter, a comparative study among planar and 3DSI has been performed. The most critical cases of digital, analog and mixed-

signal/RF circuit designs have been examined, in order to draw a reliable conclusion for every case. Lastly, several techniques to mitigate the impact of coupling effects are suggested for the most sensitive circuits, targeting an efficient process flow, compatible with sequential 3D as well as convenient rules for the design of monolithic 3D circuits.

To highlight, this thesis differentiates from the existing works in the following:

- Utilizes 28nm node FDSOI process for the sequential stacking.
- Incorporates also the heterogeneous integration concept for the different tiers. By that each tier can consist either of exclusively digital, analog and mixed-signal/RF circuit designs or a combination of them.
- Provides reliable conclusions on the critical dimensioning of the 3DSI structures. To accomplish that, the impact of coupling effects on the most prominent metrics at a device and circuit level are examined to ensure their normal operation.
- Solution challenges and methods are in-depth analyzed, employing a thorough simulation analysis for the first time. Moreover, a novel integration scheme is suggested with the integration of an inter-tier shielding layer comprised of a semi-conductive material.
- Provides a novel modeling approach, which predicts accurately the impact of layout effects on the inter-tier capacitive coupling between active devices and merges the gap between pre- and post-layout simulations. Our modeling approach can potentially be integrated in SPICE as a Verilog-A model that predicts accurately the coupling effects. As a consequence, the analysis of complex and large-scale monolithic 3D circuits with SPICE tools can become easier, enabling the circuit designer to take into account any degradation due to the parasitic effects.

The thesis is organized in seven chapters as follows:

- **Chapter 1** introduces the topic of this thesis along with the state-of-the-art approaches in the field. The main motivations behind this work, as well as its main contributions are also presented.
- **Chapter 2** provides a comprehensive introduction to the theoretical background utilized within this work. The MOSFET device physics, the electromagnetic coupling theory as well as the specificities of noise coupling in digital and analog systems are reviewed.

- **Chapter 3** presents an experimental and simulation study concerning the electromagnetic coupling between active devices separated in sequential tiers, as well as the coupling's impact on the performance. The devices that are more susceptible to coupling effects are investigated in terms of the critical alteration of their characteristic electrical parameters in both static and high frequency domain.
- **Chapter 4** studies the impact, circuit performance-wise, of the inter-tier electromagnetic coupling. The most critical circuits in digital, analog and mixed-signal/RF design have been selected to construct monolithic 3D circuits that are comprised solely by one kind or a combination thereof.
- **Chapter 5** examines a Rolling Shutter (RS) CMOS imager realized in 3DSI technology. At first, a brief disambiguation of the imager functioning is presented, focusing on the circuit operation of a single pixel. Moreover, the figures of merit of each pixel are analyzed and exploited to examine the impact of the inter-tier electromagnetic coupling for each pixel separately and as whole, the interrelation between them.
- **Chapter 6** presents the results of parasitic extraction in 3DSI structures and focuses on the modeling of the inter-tier coupling effects. To do so, the coupling through the electric field is modeled utilizing RC networks. Analytic and empirical expressions for the coupling effects are presented for a wide range of channel geometries along with several top/bottom active device configurations.
- In **Chapter 7**, all the conclusions of the research performed in the framework of the present thesis are presented, along with suggested directions for future research on the field.

CHAPTER 2

PHYSICS OF MOSFETs AND COUPLING EFFECTS

In this chapter, a description of the ideal MOSFET transistor (i.e. without any parasitic effects) in the conventional BULK architecture will be presented [65], as well as a more advanced transistor architecture, namely the Fully Depleted Silicon On Insulator (FDSOI) MOSFET [66]. The latter architecture is a promising candidate for monolithic 3D circuits and the one that this thesis focuses on. Moreover, the theory of electromagnetic coupling under a circuit analysis approximation [67] will be detailed to allow a deeper understanding of coupling effects in 3DSI. Finally, the basic methods for noise analysis in analog and digital systems will be reviewed [68], [69].

2.1 The MOSFET transistor

The Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) is the basic building block of CMOS (Complementary Metal Oxide Semiconductor) integrated circuits. This device is comprised of four electrodes, the Gate (G), the Drain (D), the Source (S) and the Body (B), illustrated in Fig. 2.1. The Gate stack is composed of a bilayer structure consisting of a metal on the top of an oxide. The Source and Drain electrodes are comprised of highly doped semiconductor regions (10^{20} cm^{-3}), P or N-type for PMOS or NMOS device respectively, accessed by metallic contacts.

The minimum distance between the S/D metallic contacts, also referred to as CPP (Contacted Poly Pitch), is a technology parameter that sets the transistor pitch and hence the density of an integrated circuit. Moreover, the channel area of the semiconductor is doped, with doping concentration N_A at a level between 10^{16} cm^{-3} and 10^{18} cm^{-3} and polarity depending on the MOS type:

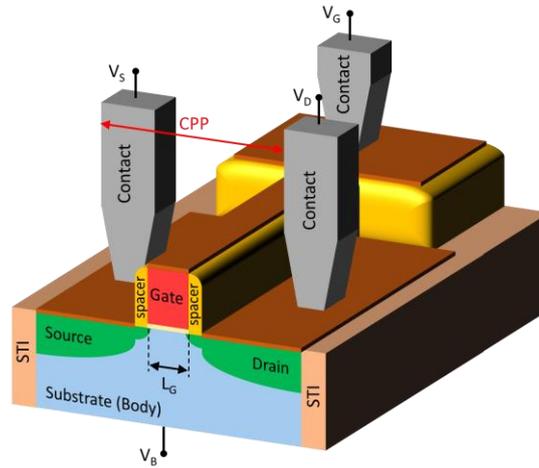


Fig. 2.1 3D representation of a BULK MOSFET.

N-type well for P-MOS and P-type well for N-MOS devices. Lastly, the Body features a highly doped semiconductor substrate (10^{20} cm^{-3}) and the applied bias to its rear face is denoted V_B .

The MOSFET operation takes advantage of the field effect induced by the applied Gate electrode bias. By that, it can block or allow a current to flow between the Source and the Drain, operating as a switch controlled by voltage. Indeed, the vertical electric field due to the polarization of the Gate electrode, modulates the density of carriers in the semiconductor, leading in two states of operation for the ideal MOSFET transistor as follows: [7]

- The blocked state: no current flows between source and drain
- The passing state: a conduction channel is induced by the gate vertical electric field and under the influence of the horizontal field (due to the higher biasing of the drain against the source), the carriers of the channel (electrons for a NMOS and holes for a PMOS device) form a current flowing between source and drain electrodes (I_{DS}).

2.1.1 Metal-Oxide-Semiconductor Capacitor operation regimes

The MOSFET owes its voltage-controlled switching properties to the MOS capacitor (Fig. 2.2 (a)). Applying a positive voltage bias at the gate ($V_G > 0$) will cause a voltage drop across the oxide (ΔV_{ox}) and the semiconductor (ΔV_{si}), hence

$$V_G = \Delta V_{ox} + \Delta V_{si} \quad (2-1)$$

Supposing that the substrate (body) is grounded, ΔV_{si} is equal to the surface potential ψ_s . The voltage drop across the oxide ΔV_{ox} can be calculated from

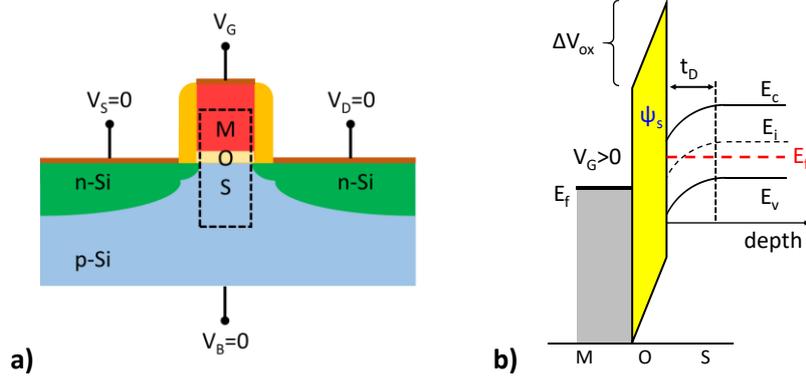


Fig. 2.2 (a) Cross-section schematic view of a MOSFET indicating the MOS capacitor and (b) its energy band diagram for $V_G > 0$.

$$\Delta V_{ox} = E_{ox} t_{ox} \quad (2-2)$$

where E_{ox} is the vertical electric field and t_{ox} is the thickness of the oxide. Applying Gauss's law at the surface layer of the semiconductor we obtain

$$D_{ox} = \epsilon_{ox} E_{ox} = -Q_s(\psi_s) \quad (2-3)$$

with Q_s being the charge at the surface layer of the semiconductor creating the displacement field D_{ox} , which is a function of the surface potential ψ_s . From (2-2) and (2-3) we can write

$$\Delta V_{ox} = -\frac{Q_s(\psi_s)}{\epsilon_{ox}} t_{ox} \quad (2-4)$$

and by defining the oxide capacitance per unit area, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$, we can get the expression for the applied gate voltage

$$V_G = -\frac{Q_s(\psi_s)}{C_{ox}} + \psi_s \quad (2-5)$$

Fig. 2.2 (b) illustrates the energy band diagram for the applied bias at the gate electrode, where E_c is the conduction band energy level, E_f is the Fermi energy level, E_v is the valence band energy level and E_i is the intrinsic energy level. The difference between the Fermi level E_f and the intrinsic level E_i is denoted ψ_B and is given by

$$\psi_B = \frac{k_B T}{q} \ln\left(\frac{N_A}{n_i}\right) \quad (2-6)$$

where q is the elementary charge, k_B is Boltzmann constant, T the temperature and n_i is the intrinsic carrier concentration.

The flat band voltage equals the gate voltage for which the energy bands across the semiconductor are flat. In any structure it occurs at a finite voltage and is the outcome of two effects. It can be calculated by

$$V_{FB} = \phi_{ms} + \frac{Q_F}{C_{ox}} \quad (2-7)$$

where ϕ_{ms} is the metal-semiconductor work-function difference, Q_F is the sheet charge at the oxide-silicon interface and C_{ox} is the oxide capacitance per unit area.

To understand qualitatively the response of the MOS capacitor to the applied gate voltage, we should have a look at the value of the electrostatic potential at the oxide-semiconductor interface. Relating the value of the surface potential ψ_s to ψ_B , the operation of the MOS capacitor can be broken down into three separate regimes (Fig. 2.3). In the case of an NMOS capacitor (the majority carriers are the holes and the minority are electrons) the operation is divided in:

- **Accumulation region ($\psi_s < 0$):** The vertical field imposed by the gate electrode, is oriented upwards, the electrons are pushed away from the oxide-semiconductor interface, while the holes are attracted towards the oxide where they accumulate. The variation of the accumulation charge Q_A is exponential and increases with $|\psi_s|$.
- **Depletion region ($0 < \psi_s < \psi_B$):** The gate vertical field has the opposite direction and is facing down. Electrons from the substrate are attracted to the oxide-semiconductor interface, filling the holes creating a zone without free carriers, called depletion zone. This zone is negatively charged, because it is solely composed of ionized dopants (acceptors in this example because the silicon is of type P). The variation in depletion charge Q_D is proportional to $\sqrt{\psi_s}$.
- **Inversion region ($\psi_s > \psi_B$):** The depletion zone stops increasing in depth and the vertical field is strong enough to attract free electrons (minority carriers) to the oxide-semiconductor interface to the oxide-semiconductor interface. The charge variation of type P silicon is then due to minority carriers; thus, the polarity of the channel is inverted. This region is divided into two parts, the weak and the strong inversion. In weak inversion ($\psi_s < 2\psi_B$) the inversion charge Q_I remains proportional to $\sqrt{\psi_s}$.

However, when in strong inversion ($\psi_s > 2\psi_B$) the Q_{inv} reversal charge growth increases exponentially with ψ_s .

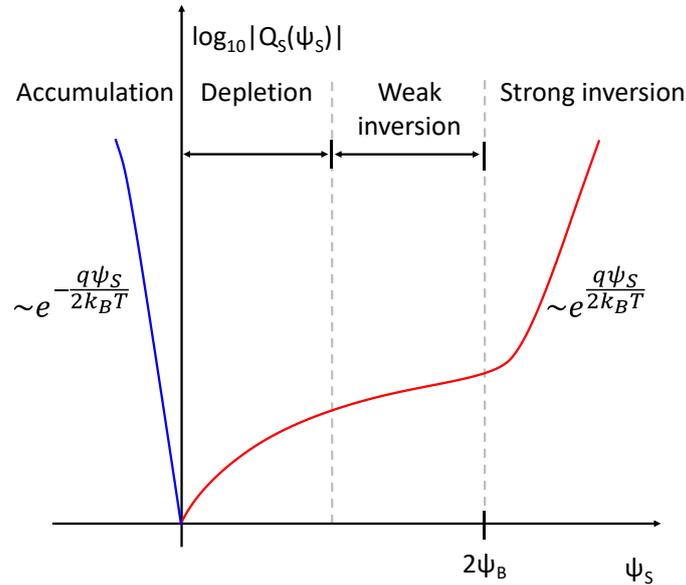


Fig. 2.3 Variation of surface charge density (accumulation charge and inversion charge) as a function of surface potential.

For a PMOS capacitor the majority carriers are electrons and the minority carriers are holes. The principle of operation remains the same except that the polarity of the voltage applied to the Gate electrode is reversed.

2.1.2 Definition of MOSFET electrical parameters

Fig. 2.4 (a) presents the drain current to gate voltage (I_D - V_G) dependence, named also input characteristics of the MOSFET transistor. On the other hand, the output characteristics that show the drain current versus drain voltage (I_D - V_D) are demonstrated in Fig. 2.4 (b).

The drain current of a MOSFET can be modeled as a function of the gate-to-source and drain-to-source voltages and depending on the region of operation, it can be written as:

$$I_{DS} = f(V_{GS}, V_{DS})$$

$$= \begin{cases} \sim 0, & V_{GS} < V_{TH} & \text{[cutoff]} \\ \frac{W}{L} \cdot \mu \cdot C_{ox} \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}, & \left(V_{GS} \geq V_{TH} \ \& \ V_{DS} < V_{GS} - V_{TH} \right) & \text{[linear]} \\ \frac{W}{L} \cdot \mu \cdot C_{ox} \frac{(V_{GS} - V_{TH})^2}{2}, & \left(V_{GS} \geq V_{TH} \ \& \ V_{DS} \geq V_{GS} - V_{TH} \right) & \text{[saturation]} \end{cases}$$

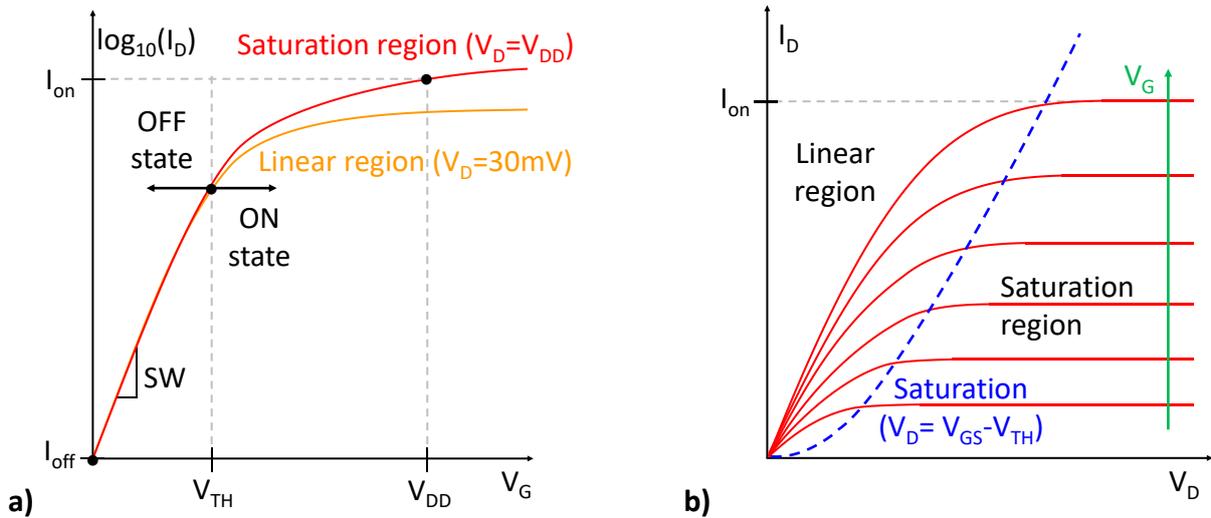


Fig. 2.4 I_D - V_G input (a) and output (b) characteristics of a MOSFET.

Threshold voltage (V_{TH}): The threshold voltage of a MOSFET is the gate to source voltage V_{GS} at which the conduction channel between source and drain is formed, thus the device turns on. Quantitatively, this means that the amount of minority carriers must be greater than the number of ionized dopants in the channel (acceptors for an NMOS), of density equal to the doping level N_A . The threshold is therefore given by the equality between these two quantities. In terms of the surface potential, the threshold is the voltage at which strong inversion occurs, thus when the value of the surface potential is $\psi_s = 2\psi_f$.

$$V_{TH} = V_{FB} + 2\psi_B + V_S + \gamma\sqrt{V_{SB} + 2\psi_F} \tag{2-8}$$

where $\gamma = \frac{\sqrt{2q\epsilon_{si}N_A\psi_s}}{C_{ox}} = \frac{Q_D}{C_{ox}}$.

Subthreshold swing (SW): Below threshold voltage ($V_G < V_{TH}$), the drain current is not zero due to the subthreshold conduction (Fig. 2.4 (a)), instead it is increasing exponentially. The subthreshold swing, is defined as the inverse of the slope of the $I_D(V_G)$ curve in the subthreshold regime, presented on a semi-logarithmic plot. It is expressed in volts or millivolts per decade and an approximation for BULK MOSFETs is given by

$$SW = \ln(10) \frac{kT}{q} \left(1 + \frac{C_d}{C_{ox}} \right) \tag{2-9}$$

where C_d and C_{ox} are the depletion layer and oxide capacitance respectively.

OFF-State current (I_{off}): is the drain current for zero gate bias. It is a leakage current and its level is a function of the threshold voltage of the device in conjunction with the subthreshold slope.

ON-State current (I_{on}): is the drain current when both the drain and gate bias equals the power supply voltage, V_{DD} ($V_{GS} = V_{DS} = V_{DD}$). The latter is a technology dependent parameter, i.e., determined by the characteristic dimensions of the device.

2.1.3 Body effect

The bias at the body electrode of a MOSFET is conventionally set to the ground potential. Hence, if the source electrode is also grounded, which is the typical case for amplifying transistors, then there is no voltage difference between the two. However, in a Source Follower (SF) configuration of the MOSFET, the source of the transistor is at a higher voltage. Thus, there is a source-body voltage V_{SB} which changes the threshold voltage of the MOSFET given by (2-8). The influence of source-bulk voltage in the drain current due to the change of the threshold voltage is named body effect.

As observed from (2-8) the variation of the threshold voltage with the V_{SB} is not linear. However if it is linearized, a simplified expression for the drain current can be defined in linear region [66],

$$I_{DS,lin} = \frac{W}{L} \cdot \mu \cdot C_{ox} \left(V_{GS} - V_{TH} - n \frac{V_{DS}}{2} \right) V_{DS} \quad (2-10)$$

and in saturation region

$$I_{DS,sat} = \frac{W}{L} \cdot \mu \cdot C_{ox} \frac{(V_{GS} - V_{TH})^2}{2n} \quad (2-11)$$

where $n = 1 + \frac{Q_D}{C_{ox}} = 1 + \frac{\epsilon_{si}/x_{depl}}{C_{ox}}$ is the Body Factor (BF).

2.1.4 Short-channel effects

So far, the ideal MOSFET device behavior was considered. However, there is a significant impact of the dimensional scaling of the MOSFET device on its electrical parameters, hence on its current-voltage characteristics.

As illustrated in Fig. 2.5, the depletion zone formed by the source and drain diffusion areas extends on the side of the junction which is the least doped, therefore in the substrate. For long channel transistors, this extension of the depletion zones is negligible compared to the total gate length and this effect has negligible impact on the electrical behavior of the transistor (Fig. 2.5 (a)). However, with the downscaling of the gate length, the extension of the depletion zones becomes comparable to the channel length and the gate loses partially the electrostatic control of the channel (Fig. 2.5 (b)). As a result, there is a “ V_{TH} roll-off” effect in short lengths (Fig. 2.6).

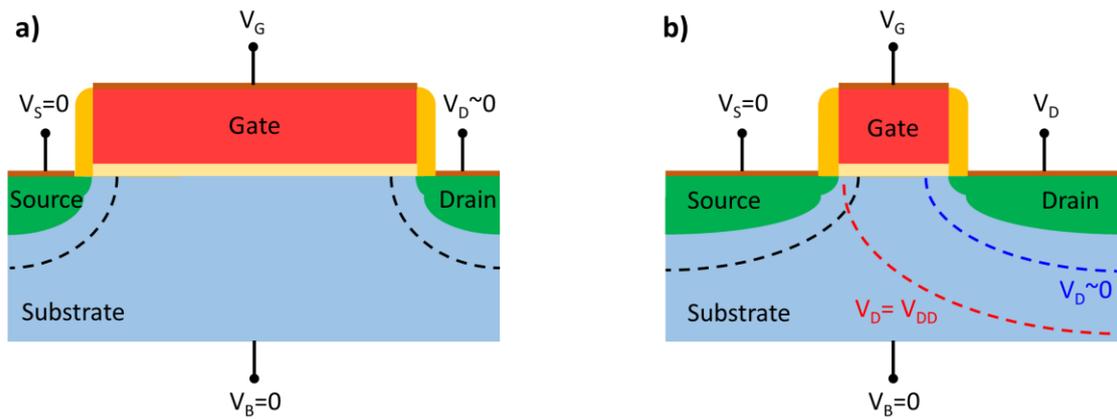


Fig. 2.5 Depletion regions indicated by the dashed lines for a long channel (a) and a short channel (b) MOSFET.

In addition, if a bias is applied to the drain (the source is conventionally grounded), the depletion zone on the drain diffusion area increases deeper inside the channel, decreasing the effective gate length (“Channel Length Modulation” effect) and therefore not allowing the current to saturate above $V_{DS}=V_{GS}-V_{TH}$. For even higher V_{DS} values, the drain depletion zone extends even further into the substrate until it overlaps with the source depletion zone.

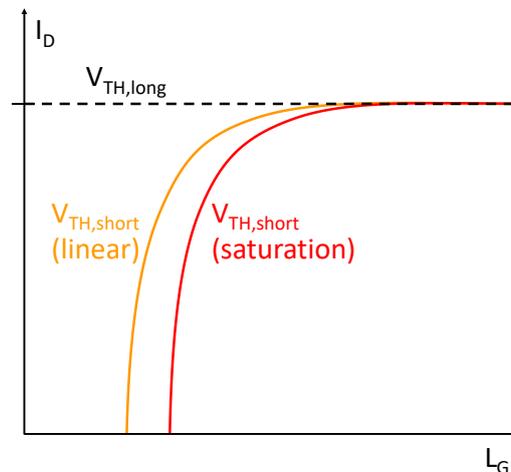


Fig. 2.6 The threshold voltage of a Long channel transistor ($V_{TH,long}$) remains constant versus the gate length, however short channel transistors experience an exponential decrease of their threshold voltage ($V_{TH,short}$). Nevertheless, due to DIBL effect, the threshold voltage of a short channel transistor is further reduced for a strong drain bias.

As a result, the electrostatic control of the gate is further reduced by the drain bias in the case of a short channel transistor. This overlapping of the source/drain depletion zones due to a strong drain bias results in a potential barrier lowering at the source-body junction. The resulting threshold voltage reduction defines the DIBL. The overall result is a decrease in the threshold voltage with the downscaling of the gate length which is more evident when the transistor is in the saturation region (Fig. 2.6).

2.2 The FD-SOI device architecture

2.2.1 SOI substrate technology

The SOI technology refers to a silicon semiconductor device in a layered silicon–insulator–silicon substrate (Fig. 2.7).

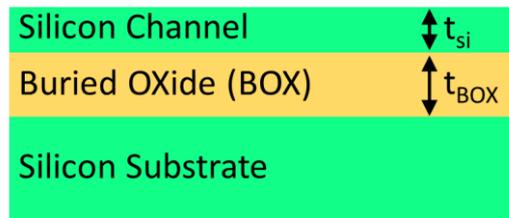


Fig. 2.7 Schematic view of the SOI substrate.

Transistors on SOI substrates were used for the first time in military and space fields applications [70], [71] thanks to their immunity to radiation. Nowadays, in consumer electronics, SOI transistors have been commercialized since the 28nm node [72]. In particular the FD-SOI (Fully Depleted Silicon On Insulator) in the UTBB (Ultra-Thin Body and BOX) configuration is the MOSFET architecture that is widely preferred for low-power/low-voltage CMOS applications due to superior performance against the BULK architecture (low Sub-Threshold Swing, low DIBL, Body-Biasing efficiency, reduced S/D coupling).

2.2.2 FDSOI device geometry

The three-dimensional representation of a FDSOI MOSFET is illustrated in Fig. 2.8 (a) while the characteristic dimensions are presented in Fig. 2.8 (b).

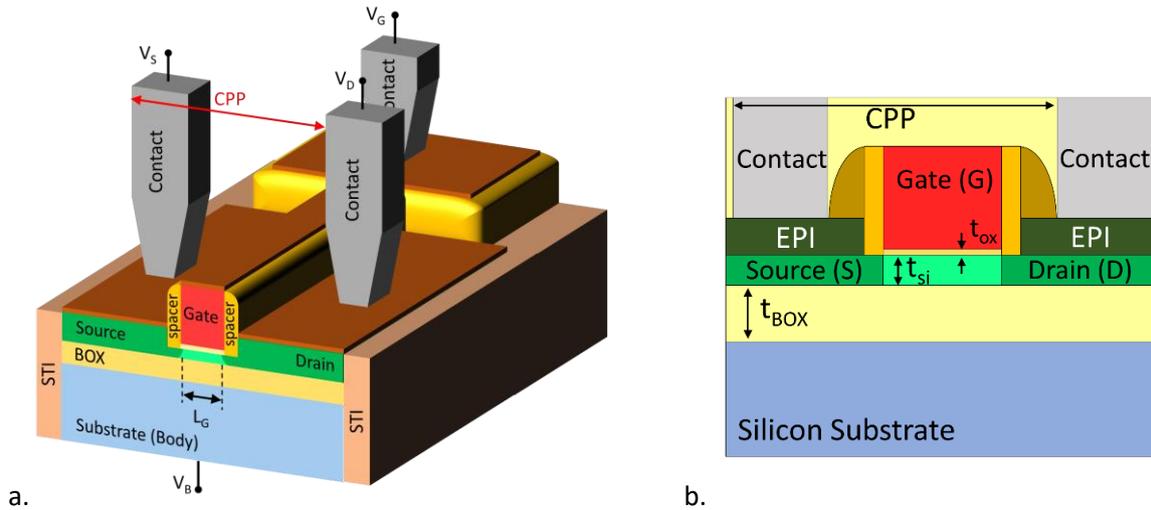


Fig. 2.8 3D representation of (a) a SOI MOSFET and (b) a cross-section schematic view of that.

It is evident that the device structure is similar to the BULK architecture, however there are major differences. The most prominent one is the drastic reduction of the silicon film which constitutes the channel alongside with the presence of the buried dielectric layer (Buried OXide - BOX) which physically limits the depth of the depletion region inside the channel to the thickness of the silicon film.

As a consequence, the FDSOI structure presents excellent Short Channel Effect (SCE) control allowing decreasing gate length down to 24nm. Moreover, it enables the possibility of utilizing an undoped silicon channel. This allows FDSOI devices to overcome the main source of variability in BULK transistors which is the Random Dopant fluctuation (RDF). With the absence of dopants, the threshold voltage becomes mainly a function of the gate-metal workfunction and the back-gate (V_B) bias. Thus the variability is reduced drastically, with values of $\Delta\Delta V_{TH}$ reported, as low as $1.6 \text{ mV}\cdot\mu\text{m}$ [72].

Due to the thin silicon film, the Source and Drain are elevated to limit the series resistance. In order to accomplish that, the raised S/D regions are epitaxial processed upon the thin silicon film of the active layer as shown in Fig. 2.8 (b).

Finally, the field lines from the source and drain diffusion regions penetrate the BOX resulting in a capacitive coupling between drain and channel, causing DIBL effect to elevate. To limit this effect, the BOX thickness must be as thin as 25nm along with a doped layer (namely Ground Plane (GP)) [73] of the type opposite to the source/drain regions under the thin BOX. The latter limits the effective thickness of the BOX to its physical thickness and eliminates the capacitive coupling effect between the source and drain regions.

2.2.3 Front/Back interface charge coupling

In SOI MOSFETs, the charge coupling between the front and back interface is characterized by the charge-coupling factor r that expresses the sensitivity of the threshold voltage (V_{TH}) to changes in the BG voltage (V_B). Due to the existence of the front and back interfaces, there is a front/back channel threshold voltage ($V_{TH,f}$, $V_{TH,b}$), dependent on the front/back-gate biases ($V_{G,f}$, $V_{G,b}$), as well as the other physical quantities ($V_{FB,f}$, $V_{FB,b}$ etc.).

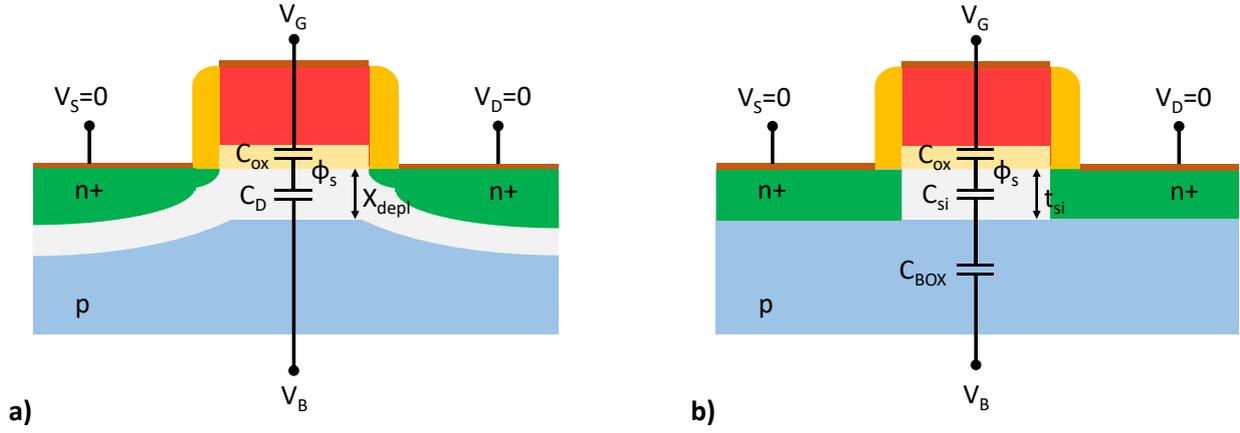


Fig. 2.9 The channel capacitance network formed in a BULK (a) and a SOI (b) MOSFET.

For long-channel devices, early models [74] have solved the electrostatics of FDSOI MOSFETs in 1-D employing two fundamental “classical” assumptions. The first concerns the depletion approximation, which assumes $|Q_b| \gg |Q_i|$, where $Q_b = -qt_{si}N_B$ is the depletion charge density and Q_i is the inversion-charge density within the silicon film. By this assumption, free carriers cannot sufficiently screen the applied potential within t_{si} , and hence the potential distribution in the entire body is virtually independent of Q_i . The second assumption considers inversion-charge sheets at the front and/or back surfaces of the silicon film, due to the high transverse electric field imposed by the gate electrode, which confines the inversion charge carriers near the surfaces in a region much thinner than the silicon film thickness. Since Q_i and its effect on the potential distribution are negligible, the charge-sheet approximation is superfluous for subthreshold analysis. Solving the (1-D) Poisson equation with the charge sheet and the depletion approximation, one can easily obtain the two equations in the Lim and Fossum model [74]:

$$V_{GfS} - V_{FBf} = \left(1 + \frac{C_{si}}{C_{ox}}\right) \phi_{sf} - \frac{C_{si}}{C_{ox}} \phi_{sb} \quad (2-12)$$

$$V_{Gbs} - V_{FBb} = -\frac{C_{si}}{C_{box}} \varphi_{sf} + \left(1 + \frac{C_{si}}{C_{box}}\right) \varphi_{sb} \quad (2-13)$$

where φ_{sb} is the back-surface potential, $C_{si} = \frac{t_{si}}{\epsilon_{si}}$ being the silicon film capacitance per unit area and the subscripts f and b refer to front and back gates of the device respectively. With φ_{sb} from (2-13) and $\varphi_{sf}=2\varphi_B$ (for NMOS), as long as the back surface remains depleted, (2-12) becomes[74]:

$$V_{Gfs} = V_{TH,f} = V_{FBf} + rV_{FBb} + (1+r)2\varphi_B - rV_{Gbs} \quad (2-14)$$

where

$$r = \frac{C_{box}C_{si}}{C_{ox}(C_{box} + C_{si})} \quad (2-15)$$

is the slope of the linear region of the front-gate coupling characteristic (variation of the front gate threshold voltage $V_{TH,f}$ with the back-gate voltage V_{Gb}). The above expression is referred in the literature as the charge-coupling factor. From the latter, it is evident that the threshold voltage of one gate varies linearly (Fig. 2.10) with the opposite gate bias as long as the back silicon film interface is depleted and saturates with onsets of strong accumulation or inversion at the opposite interface.

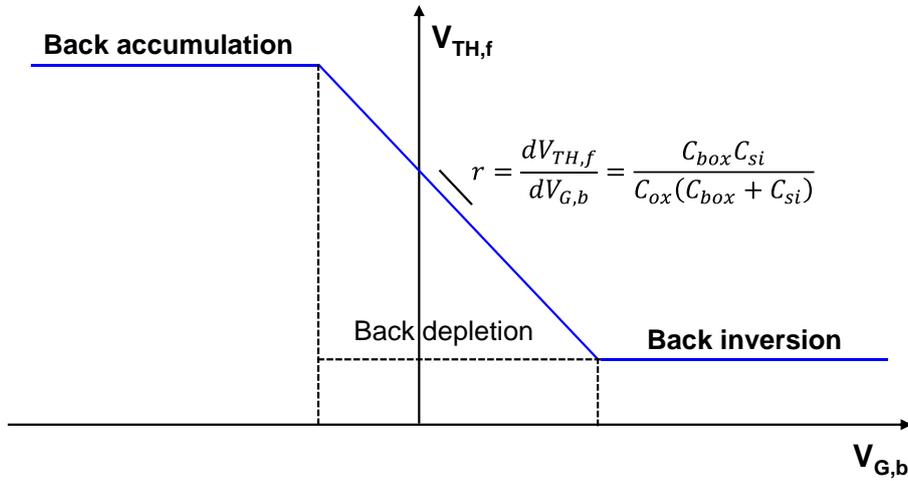


Fig. 2.10 Schematic diagram of the Threshold voltage sensitivity of the front-gate versus the back-gate bias in the Lim-Fossum model.

Similarly to the BULK MOSFET, the BF of SOI MOSFET is defined as

$$n = 1 + \frac{Q_D}{C_{ox}} = 1 + \frac{C_{box}C_{si}}{C_{ox}(C_{box} + C_{si})} = 1 + r \quad (2-16)$$

2.3 Electromagnetic coupling and transfer of energy between electrical components

Any circuit element of a network can be coupled with an adjacent one even when they are not physically connected by a conductive material. The transfer of energy can be induced by the electric and magnetic fields that surround the two circuit elements.

Electric fields are caused by electric charges, described by Gauss's law or varying magnetic fields, described by Faraday's law of electromagnetic induction. In the same manner, magnetic fields are formed by changing currents as described by Ampere's circuital law. These principles characterize the complementary nature of the electric and magnetic fields and are summarized in the form of the Maxwell equations, presented in Table 2.1. The vector fields \vec{E} (V/m) and \vec{H} (A/m) represent the intensity of the electric and magnetic field respectively, whereas \vec{D} (C·m⁻²) is the electric displacement field and \vec{B} (Wb) is the magnetic flux density.

Table 2.1 Maxwell's Equations

	Differential Form	Integral Form
Gauss' law	$\nabla \cdot \vec{E} = \rho/\epsilon_0$	$\oint_S \vec{D} \cdot d\vec{A} = \int_V \rho dV$
Gauss' law (magnetism)	$\nabla \cdot \vec{B} = 0$	$\oint_S \vec{B} \cdot d\vec{A} = 0$
Faraday's law	$\nabla \times \vec{E} = -\frac{\partial \vec{B}}{\partial t}$	$\oint_C \vec{E} \cdot d\vec{l} = -\frac{\partial}{\partial t} \int_S \vec{B} \cdot d\vec{A}$
Ampere's circuital law	$\nabla \times \vec{H} = \vec{j} + \frac{\partial \vec{D}}{\partial t}$	$\oint_C \vec{B} \cdot d\vec{l} = \int_S \vec{j} \cdot d\vec{A} + \frac{\partial}{\partial t} \int_S \vec{D} \cdot d\vec{A}$

As a consequence, in order to assess how any electric circuit behaves, the exact solution of Maxwell's equations is needed. These equations constitute a four-dimensional problem (x, y, z, t), so even the simplest problems can be proven highly complex.

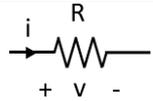
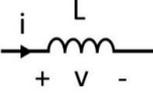
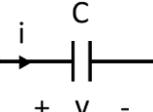
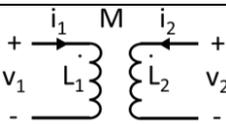
To simplify things, an approximation is often used in circuits, named circuit analysis. This technique facilitates the problem considering a discrete representation of the electric and magnetic fields coupling by lumped electric components (i.e., capacitors and inductors) where voltage and current do not vary significantly over the physical dimension of the elements. The analysis considers the following:

- All electric fields are confined to the interiors of capacitors.
- All magnetic fields are confined to the interiors of inductors.
- Dimensions of the circuit are small compared with the wavelength under consideration. Specifically, the electrical size of the structures (i.e., the ratio of the largest distance between two points in the structure divided by the wavelength of the electromagnetic fields) must be in the range up to 1/10.

Utilizing this technique, any coupling problem can be described accurately by considering victim-aggressor pairs that consist a network of passive elements within a circuit. It is important to emphasize that in the case where the physical dimensions of the network are comparable to the electrical wavelength, circuit analysis is not valid. Instead, transmission line theory must be used in which the circuit is considered as a distributed-parameter network, where voltages and currents can vary in magnitude and phase over its length.

The most basic lumped elements, adequate to describe any coupling effect in a circuit analysis are summarized in table 2.2.

Table 2.2 Basic passive elements

	Symbol	I-V relation	Unit
Resistance (R)		$v = Ri \quad (1)$	Ohm [Ω]
Inductance (L)		$v = L \frac{di}{dt}$	Henry [H]
Capacitance (C)		$i = C \frac{dv}{dt}$	Farad [F]
Mutual Inductance (M)		$v_1 = M \frac{di_2}{dt} + L_1 \frac{di_1}{dt}$ $v_2 = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt}$	Henry [H]

2.4 Noise sources in devices and circuits

Every fluctuation existing in an electrical signal other than the desired one can be considered as noise. We can classify the noise sources as intrinsic and extrinsic. The former is generated in the

electronic circuit element itself whereas the second, called also coupled noise, is induced by external interferences.

2.4.1 Intrinsic noise sources

The intrinsic noise of an electronic circuit element is a random process, characterized by stochastic properties such as its variance, distribution, and Power Spectral Density (PSD). The spectral distribution of noise can vary with frequency, so its PSD is measured in Watts per Hertz (W/Hz). Since power in a resistive element is proportional to the square of the voltage across it, noise voltage (density) can be described by taking the square root of the noise power density, resulting in volts per square root hertz (V/\sqrt{Hz}). Different types of intrinsic noise sources exist generated by different electronic components. These types are:

Thermal noise or Johnson noise: is caused by the random thermal motion of the charge carriers (holes or electrons), and the voltage PSD associated with it, is given from the expression

$$S_{V,thermal} = 4 \cdot k \cdot T \cdot R \quad (2-17)$$

where R the resistance in Ohms, k is the Boltzmann constant, T is the temperature of the conductor in Kelvin degrees. It is also known as Johnson or Nyquist noise. Integrating the PSD of thermal noise over the noise bandwidth ΔF and taking the square root of it, the voltage noise RMS (root mean square) that a resistive element generates is given from the expression

$$v_n = \sqrt{4 \cdot k \cdot T \cdot R \cdot \Delta F} \quad (2-18)$$

Shot noise: is a type of noise that originates from the discrete nature of electric charge in semiconductor devices like p-n junctions. It consists of random fluctuations of a DC current I, characterized by a PSD

$$S_{I,shot} = 2qI \quad (2-19)$$

Low Frequency Noise (LFN): is a type of noise occurring in semiconductor devices with a $1/f^{\alpha}$ PSD and is often used for the characterization of material or interfaces quality. The dominant mechanism is the Generation – Recombination (G-R) noise that results in the fluctuation of free carriers inside the

channel (Δn) whereas the second mechanism is scattering which leads to mobility fluctuations ($\Delta\mu$). In the literature, the LFN modeling is subject to the following three approaches:

1. Carrier Number Fluctuations (CNF) model

In the CNF approach [75], the drain current fluctuations are related to the free carriers located inside channel close to the oxide-semiconductor interface that are tunneled into dielectric traps under a trapping and de-trapping activity.

Individual traps or a group of traps with same characteristics lead to a Lorentzian shaped ($1/f^2$) PSD (Fig. 2.11 (a)) contrary to $1/f$ in the case of a uniform spatial trap distribution (Fig. 2.11 (b)). In the case of an uneven distribution, it can be considered as a summation of Lorentzian spectra as depicted for instance in Fig. 2.12 (a) and Fig. 2.12 (b).

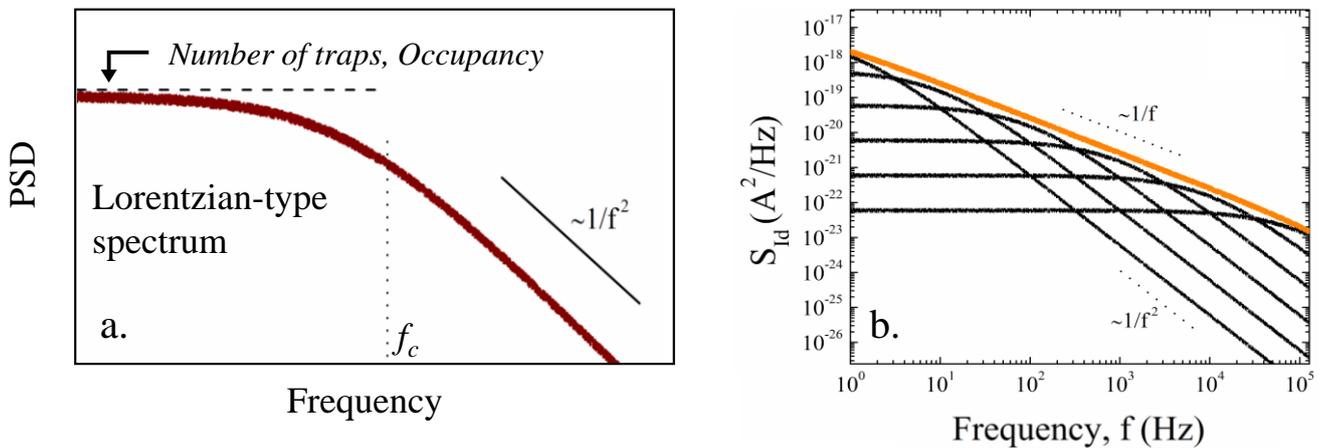


Fig. 2.11 (a) Lorentzian type spectrum example and (b) result of adding two six uniform different level Lorentzians [76].

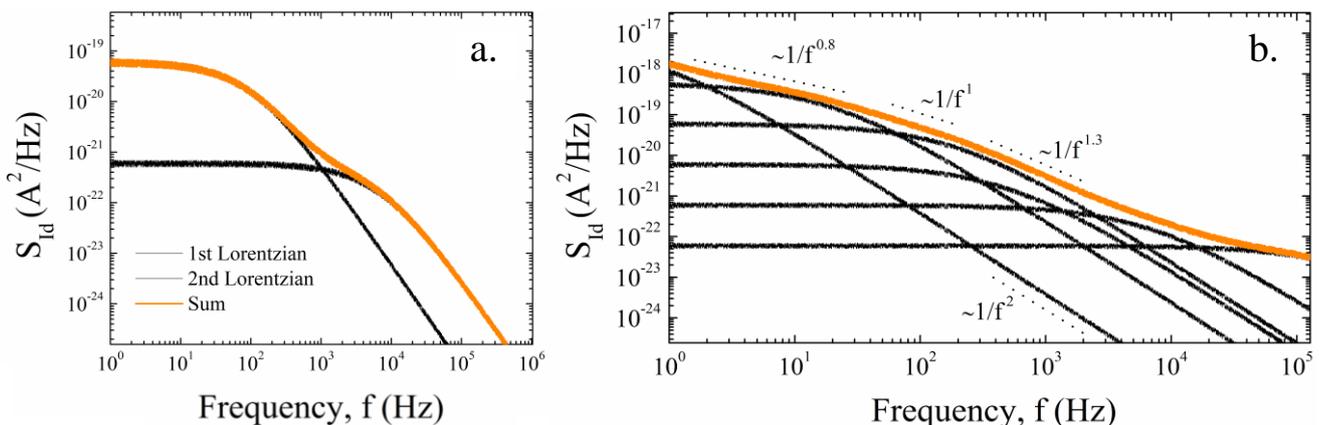


Fig. 2.12 (a) Spectrum result of adding two different level Lorentzians and (b) result of adding non-uniform Lorentzians [76].

2. Mobility Fluctuations or Hooge model

The Hooge noise model [77] suggests that the $1/f$ noise is the result of bulk mobility fluctuations due to phonon scattering. It is an empirical model that tends to explain better the observed $1/f$ noise in p-channel MOSFETs, contrary to n-channel devices.

3. Carrier Number Fluctuations with correlated Mobility Fluctuations (CNF/CMF) model

The CNF/CMF is a unified model that extends the CNF theory to include the Coulomb scattering of free carriers by trapped oxide charges. Consequently, apart from the fluctuation in the number of carriers in the channel (Δn), their mobility also fluctuates ($\Delta\mu$). Because the two events have the same origin, they are correlated and hence we consider the mobility fluctuations with respect to the carrier number fluctuations ($\Delta\mu/\Delta n$). A simplified schematic view of the CNF/CMF model approach is illustrated in Fig. 2.13 (c).

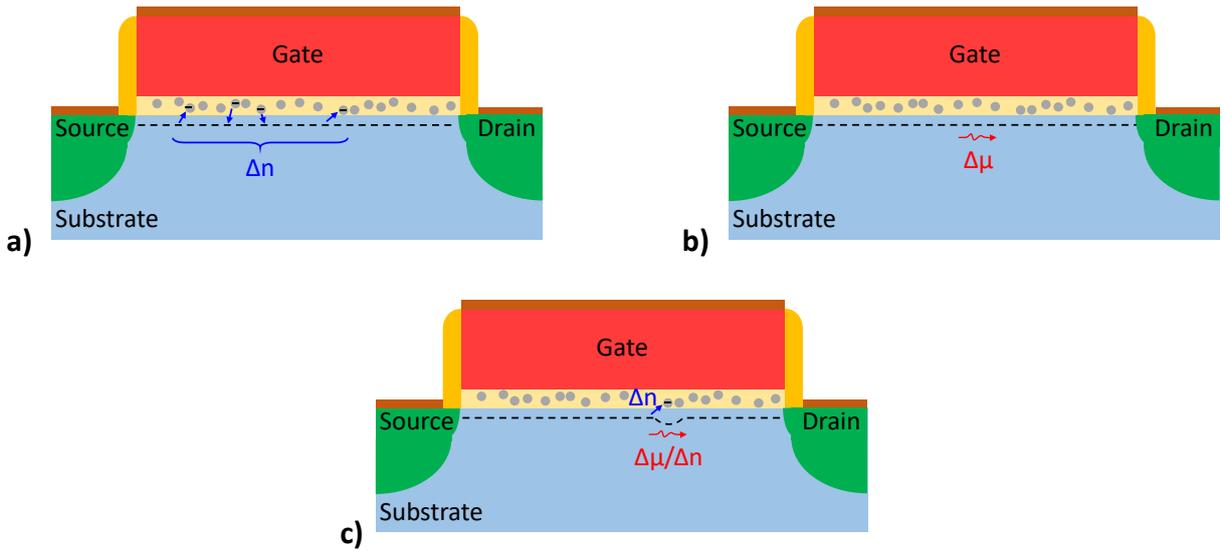


Fig. 2.13 Schematic representation of (a) the CNF model (b) The Hooge model and (c) the unified CNF/CMF model.

The interface charge variation δQ_{it} can be translated into a flat band voltage variation as

$$\delta V_{FB} = -\frac{\delta Q_{it}}{WLC_{ox}} \quad (2-20)$$

with C_{ox} being the oxide capacitance per unit area and WL the device area. The overall drain current fluctuations become for the linear operation region [78], [79]

$$\delta I_D = -g_m \delta V_{FB} - a_{sc} I_D \mu_{eff} \delta Q_{it} \quad (2-21)$$

where g_m is the transconductance, μ_{eff} is the effective mobility and a_{sc} is the Coulomb scattering coefficient. The normalized drain current noise is

$$\frac{S_{I_D}}{I_D^2} = S_{V_{fb}} \left(\frac{g_m}{I_D} \right)^2 \left(1 + a_{sc} \mu_{eff} C_{ox} \frac{I_D}{g_m} \right)^2 \quad (2-22)$$

which can be converted to an input-referred gate voltage noise as

$$S_{V_G} = \frac{S_{I_D}}{g_m^2} = S_{V_{fb}} \left(1 + a_{sc} \mu_{eff} C_{ox} \frac{I_D}{g_m} \right)^2 \quad (2-23)$$

with $S_{V_{fb}}$ being the flat band voltage PSD.

2.4.2 Extrinsic noise sources

In general, noise energy can be coupled into a circuit from many sources of the external environment (light, cell phones, mechanical vibrations etc.). Thus, in our analysis we will focus exclusively on the extrinsic noise originated by adjacent circuit elements. This type of noise is often named crosstalk in electronics and the aggressor is the crosstalk source within a circuit, as opposed to the victim being the receptor of the interference. It can be characterized as capacitive coupling when the transfer of energy is induced by the electric field, contrary to the inductive coupling which is attributed to the magnetic field created by the aggressor. Contrary to intrinsic noise which has a stochastic nature, extrinsic noise originated by adjacent circuit elements has deterministic properties and thus may be predictable.

2.4.2.a Capacitive coupling

Fig. 2.14 illustrates two conductors in such proximity that the electric field of conductor 1 is coupled to conductor 2. The transfer of energy on the receptor conductor, induced by the electric field, is represented as a coupling capacitance C_{12} , R is the load connected to conductor 2 and C_{1G} , C_{2G} represent the stray capacitance of the respective conductor to ground. The coupled voltage picked by conductor 2, is given by [67],

$$V_2 = \frac{j\omega(C_{12}/(C_{12} + C_{2G}))}{j\omega + 1/R(C_{12} + C_{2G})} V_1 \quad (2-24)$$

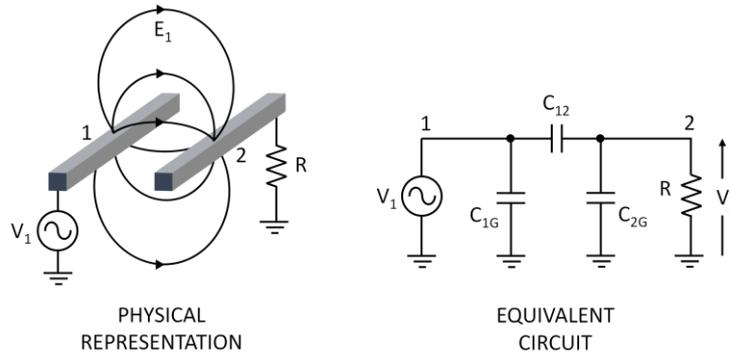


Fig. 2.14 Capacitive coupling between conductors 1 and 2.

In the case that $\omega \gg 1/R(C_{12} + C_{2G})$ equation (2-24) becomes

$$V_2 = \left(\frac{C_{12}}{C_{12} + C_{2G}} \right) V_1 \quad (2-25)$$

However, in the low-frequency case that $\omega \ll 1/R(C_{12} + C_{2G})$, the voltage picked by conductor 2 is

$$V_2 = j\omega R C_{12} V_1 \quad (2-26)$$

which is proportional to the frequency of the aggressor's signal and of lower magnitude than the one of (2-25). Therefore the capacitive coupling can be modeled as a current source connected between the receptor and ground, of magnitude given by [67],

$$I_2 = j\omega C_{12} V_1 \quad (2-27)$$

2.4.2.b Capacitive shielding

From EMC theory it is well known that a conductive surface surrounding the 'victim' can act as a shield against the electromagnetic coupling from the 'aggressor'. To understand the effect of shielding against the capacitive coupling, the case of two coupled conductors shall be considered, with the aggressor being the noise source and the victim surrounded by a shield as shown in the equivalent circuit of Fig. 2.15. The shield consists of a conductive material and encloses completely the receptor conductor.

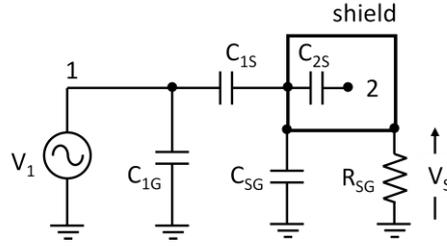


Fig. 2.15 Equivalent circuit model of capacitive coupling shielding between conductors 1 and 2.

In case that the shield is not terminated, R_{SG} is infinitely large. Therefore the capacitance network consists in a voltage divider and hence the noise voltage on the shield is given by [67],

$$V_S = \left(\frac{C_{1S}}{C_{1S} + C_{SG}} \right) V_1 \quad (2-28)$$

where C_{1S} is the capacitance between conductor 1 and the shield whereas C_{SG} is the stray capacitance of the shield to ground. Since conductor 2 is floating, there is no current flowing through C_{2S} , thus the noise voltage picked from the shield is transferred to the receptor conductor ($V_S=V_N$). However, if the shield is grounded properly ($R_{SG}=0$), the voltage on the shield is $V_S=0$ and so is the noise voltage picked by conductor 2.

In most practical cases, conductor 2 extends beyond the shielding surface so there is a coupling capacitance C_{12} between conductors 1, 2 and also a stray capacitance C_{2G} of conductor 2 to the ground. In that case the voltage picked by conductor 2 is

$$V_2 = \left(\frac{C_{12}}{C_{12} + C_{2G} + C_{2S}} \right) V_1 \quad (2-29)$$

As observed from (2-29), V_2 depends primarily on C_{12} . The latter may be due to the exposed area of conductor 2 as well as the efficiency of the shielding material to suppress the electromagnetic field of conductor 1. Hence for an effective shielding of the capacitive coupling between two conductors, it is mandatory to properly ground the shield and minimize C_{12} .

In most cases the conductor 2 has a finite resistance to ground (Fig. 2.15), and also $R_{2G} \ll \frac{1}{j\omega(C_{12}+C_{2G}+C_{2S})}$, so the noise voltage picked by conductor 2 is

$$V_2 = j\omega R_{2G} C_{12} V_1 \quad (2-30)$$

which is the same as for an unshielded conductor, however C_{12} is reduced significantly due to the presence of the shield.

2.4.2.c Inductive coupling

A conductor which carries an electric current produces a magnetic field with a form of concentric circles surrounding the conductor. The direction of the magnetic field is perpendicular to the conductor and the magnetic flux is proportional to the current. The ratio of the total magnetic flux Φ_T to the current that produces it, determines the self-inductance of the conductor given by [67],

$$L = \frac{\Phi_T}{I} \quad (2-31)$$

When current flows also in an adjacent conductor 2, the magnetic field produced from conductor 1 is coupled to conductor 2, creating a mutual inductance M_{12} defined as

$$M_{12} = \frac{\Phi_{12}}{I_1} \quad (2-32)$$

where Φ_{12} is the magnetic flux in conductor 2 from current I_1 flowing through conductor 1. Applying Faraday's law to the closed loop or area \vec{A} , the coupled voltage V_2 induced by the magnetic field is derived as

$$V_2 = -\frac{d}{dt} \int_S \vec{B} \cdot d\vec{A} \quad (2-33)$$

If the conductor 1 is stationary and the magnetic flux density is harmonically varying with time but constant over the area of the loop, (2-33) becomes

$$V_2 = j\omega BA \cos \theta \quad (2-34)$$

where θ is the angle between \vec{B} and \vec{A} . Considering that the term $BA \cos \theta$ represents the total magnetic flux Φ_{12} coupled to the receptor circuit, (2-32) and (2-34) can be merged and the coupled noise voltage is expressed ultimately as

$$V_2 = j\omega M_{12} I_1 \tag{2-35}$$

The physical representation as well as the equivalent circuit of inductive coupling is illustrated in Fig. 2.16.

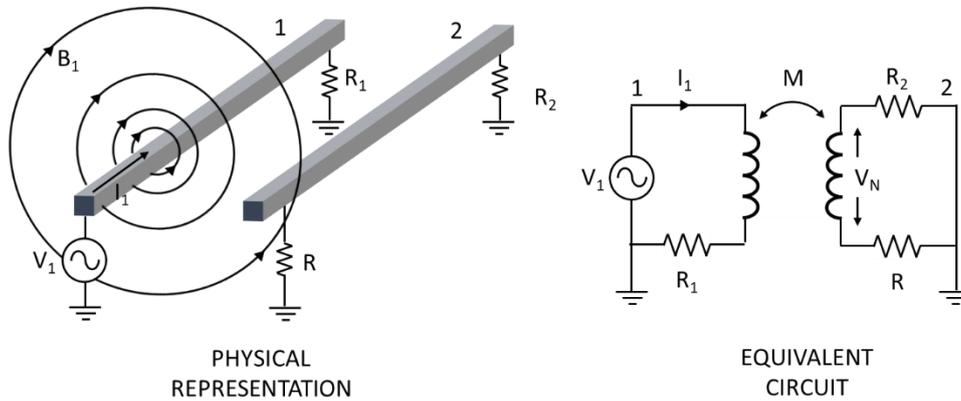


Fig. 2.16 Inductive coupling between conductors 1 and 2.

2.4.2.d Inductive shielding

As opposed to the capacitive coupling shielding, the inductive coupling is way more difficult to be reduced. A non-magnetic conductive surface enclosing the receptor conductor 2 has no effect on the geometry or magnetic properties of the medium between conductors 1 and 2, and consequently has no effect on the voltage induced into conductor 2. However, a voltage is coupled to the shield because of the current I_1 flowing through conductor 1, given by [67],

$$V_S = j\omega M_{1S} I_1 \tag{2-36}$$

where M_{1S} is the mutual inductance between the conductor 1 and the shield. A ground connection at one end of the shield has no impact on this magnetically induced voltage. On the contrary, if the shield is grounded at both ends, the voltage V_S will cause a current to flow through the shield. As an outcome, the shield current will induce a second noise voltage into the receptor conductor 2, which can potentially worsen its noise coupling level.

Following that, the magnetic field decoupling analysis is rather complex and goes beyond the scope of this thesis. Each case must be treated separately, taking this into account the geometry of the problem. A shield can be effective only if the induced shield current that produces the magnetic field is, cancels a large percentage of the direct induction into conductor 2. In any case the key to

reducing magnetic coupling is to avoid loop configurations of both the receptor and aggressor conductors.

2.4.3 Noise coupling in circuits

Analog systems differ substantially from digital ones in terms of signal processing. An analog signal can obtain any value within the power supply range counter to digital signal which has a value between two logic levels.

2.4.3.a Digital noise

Due to the fact that signals in nature are analog, digital electronics utilize by convention the minimum and maximum values of the power supply range to represent the “low” and “high” of a digital signal. As a consequence, the power supply range is divided into the logical high and logical low range and any other value within the two falls into the indeterminate range (Fig. 2.17).

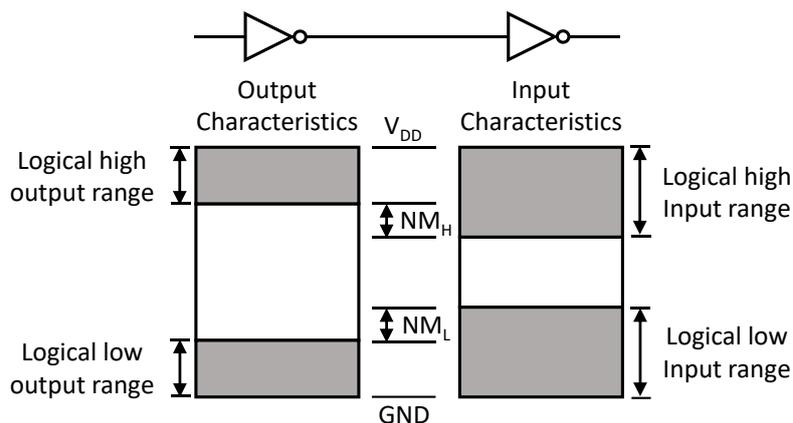


Fig. 2.17 Noise margin of a driving (left) and a receiving (right) device.

In general digital circuits present an inherent immunity to noise injected from external sources. This property emanates from the input-output noise margins, NM_L and NM_H , which refer to the ability of a logic gate to accommodate input noise without producing a faulty logic output.

The methodology for the noise margins estimation in CMOS technology has been presented in [68]. Following that, the noise margins of a CMOS logic gate can be found by first examining the DC transfer curve shown in Fig. 2.18. The input noise threshold levels, V_{IL} and V_{IH} are defined as the input voltages that result in a slope of -1 in the dV_{out}/dV_{in} response.

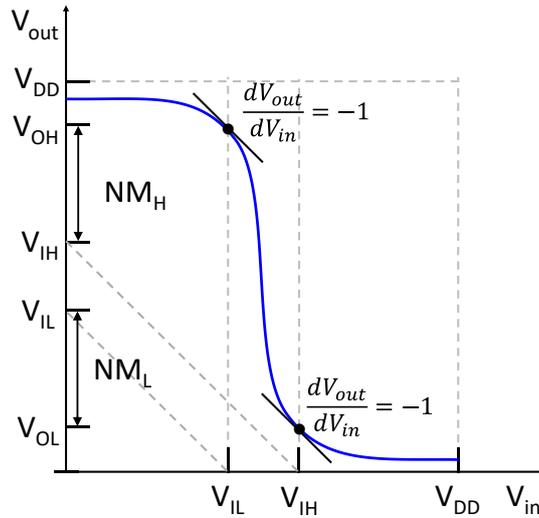


Fig. 2.18 DC transfer curve of an inverter.

From graphical analysis, V_{IL} occurs when the PMOS is in its linear regime and the NMOS is in its saturation regime. Since a CMOS gate is complementary in operation, V_{IH} by symmetry occurs when the PMOS is in its saturation regime and the NMOS is in its linear regime. Considering first the CMOS V_{IL} , equating the NMOS and PMOS currents gives [68]:

$$k_n \frac{W_n}{L_n} \frac{(V_{in} - V_{THn})^2}{2} = k_p \frac{W_p}{L_p} \left(V_{in} - V_{DD} - V_{THp} - \frac{V_{out} - V_{DD}}{2} \right) (V_{out} - V_{DD}) \quad (2-37)$$

where $k_{n/p} = \mu_{n/p} \cdot C_{ox}$. Assuming that the inverter is designed to have a balanced transfer curve such that

$$k_n \frac{W_n}{L_n} = k_p \frac{W_p}{L_p} \quad (2-38)$$

then (2-37) can be reduced yielding the form [68]:

$$V_{IL} = \frac{3V_{DD} + 3V_{THp} + 5V_{THn}}{8} \quad (2-39)$$

Considering next the CMOS V_{IH} , equating the NMOS and PMOS currents results in:

$$k_n \frac{W_n}{L_n} \left(V_{in} - V_{THn} - \frac{V_{out}}{2} \right) V_{out} = k_p \frac{W_p}{L_p} \frac{(V_{in} - V_{DD} - V_{THp})^2}{2} \quad (2-40)$$

Again, using the previous assumption, this expression can be simplified such as

$$V_{IH} = \frac{5V_{DD} + 5V_{THp} + 3V_{THn}}{8} \quad (2-41)$$

The noise margins are given as

$$NM_L = V_{IL} - V_{OL} \quad (2-42)$$

$$NM_H = V_{OH} - V_{IH} \quad (2-43)$$

where V_{OL} and V_{OH} are 0 and V_{DD} respectively for CMOS technology. Consequently, equations (2-42) and (2-43) become

$$NM_L = \frac{3V_{DD} + 3V_{THp} + 5V_{THn}}{8} \quad (2-44)$$

$$NM_H = V_{DD} - \frac{5V_{DD} + 5V_{THp} + 3V_{THn}}{8} \quad (2-45)$$

2.4.3.b Analog noise

From an analog system perspective, noise is typically characterized by its impact as a small-signal fluctuation. Considering that, noise is modeled as an independent alternating current (AC) source (Fig. 2.19). In a small signal noise analysis, the noise PSD is utilized in order to obtain the noise magnitude (either voltage V_N or current I_N) and compare that to the signal magnitude.

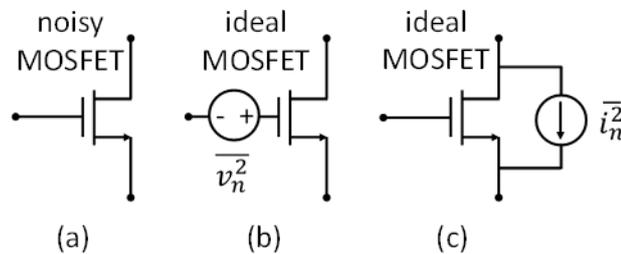


Fig. 2.19 (a) noisy MOSFET and its equivalent model comprised of an ideal MOSFET and (b) voltage or (c) current noise source.

Hence, a significant quantity for determining the impact of noise in analog circuit is the Signal-to-Noise-Ratio (SNR). The SNR represents the ratio of the useful signal to the unwanted parasitic signals. Therefore, it must be as high as possible, achieved by increasing the system's sensitivity and more importantly, by decreasing the noise.

The dominant noise in analog circuits is the intrinsic noise of the MOSFET transistors. The two major sources are the thermal and the LFN, both of them explained in §(2-4). The latter is not only important in conventional analog circuits like operational amplifiers, but also in RF circuits like Voltage Controlled Oscillators (VCOs), where the LFN up-converts to phase/jitter noise [80]. Furthermore, a special case of LFN, namely the Random Telegraph Signal (RTS) noise, becomes of

high importance with the MOSFET device downscaling [81], and consequently for highly miniaturized sensor applications like the pixel readout part of an imager circuit [82], [83].

2.4.3.c Mixed-Signal noise coupling

The mixture of analog and digital applications within the same chip, implies an electromagnetic interference between them unless there is proper shielding. Thus, each of them can be considered as an aggressor or victim to the other. As presented in §2.4.2, the electromagnetic coupling depends both on the amplitude and the frequency of the aggressor's signal. Thus, it is evident that high speed electronic circuits can be an intense noise source, while their amplitude is limited to the power supply range.

Analog microwave circuits, called also RF more commonly, utilize bandpass signals at frequencies above 1GHz [84], whereas there is a special distinction for circuits at frequencies above 30 GHz which are designated for mmW applications. Except for individual transistors they can also feature micro-strip transmission lines, filters, matching networks and other elements. In the frequency domain, transistors are characterized by the "transition frequency" f_T and the f_{max} which set their maximum frequency limit.

On the other hand, digital circuits employ pulse switching signals above 100MHz reaching sub-nanosecond rise time [85] nowadays. The harmonic content of a pulse shaped signal extends to infinity; however, its energy content fades with increasing frequency. Hence, there is a point beyond which it can be neglected and occurs at the break point where the Fourier coefficients start to decay at 40 dB/decade, instead of 20 dB/decade [67]. As a result, the bandwidth of a digital signal can be given by

$$BW = \frac{1}{\pi t_R} \quad (2-46)$$

where t_R is the rise time of the pulse shaped signal. For instance in 28nm FDSOI technology, rise times of 10ps have reported [72], resulting in an equivalent bandwidth of 31.8GHz for a digital signal.

Therefore, the limitation of the harmonic content of digital signals to a certain bandwidth for a given technology, in conjunction with the maximum operating frequency of RF devices can help estimate the impact of electromagnetic coupling in mixed-mode monolithic 3D circuits.

2.5 Conclusion

In this chapter the MOSFET device physics have been reviewed accompanied by the specificities of the SOI versus the conventional BULK architecture. Accounting for the MOSFET device operation, the basic electrical parameters utilized within this work, have been highlighted for the two architectures. In addition, the noise sources existing in electronic devices alongside with the noise coupling mechanisms have been assessed. In particular, the PSD generated from an electronic component has been evaluated for each noise mechanism while it has been demonstrated how this noise can be propagated to adjacent components in terms of voltage or current. Nonetheless, noise analysis methods for analog and digital systems have been noted, emphasizing on the noise susceptibility of each one.

CHAPTER 3

INVESTIGATION OF 3DSI

ELECTROMAGNETIC COUPLING EFFECTS

AT A DEVICE LEVEL

First of all, this chapter describes the 3D sequential process schemes and their main characteristics. Moreover, a detailed overview of the structures utilized in our experiments is presented. Electrical measurements on the structures under test reveal the susceptibility of each active tier to electromagnetic coupling. Regarding the inter-tier electrostatic coupling effects in 3DSI, although prior works have already presented them in principle [51], [52], [54], [55] and experimentally verified [57], this chapter presents the first analytical study examining the coupling between the top and bottom tiers of 3D sequential technology stacking 28 nm FDSOI MOSFETs, under normal circuit operation ($V_{DD} = 0.9$ V) and its impact on LFN behavior of the stacked devices. Additionally, concerning the inter-tier dynamic coupling and RF crosstalk of digital circuits in 3DSI, experiments in conjunction with TCAD simulations reveal the parasitic capacitances responsible for dynamic coupling effects and its impact at device level is investigated. Lastly, the results of this analysis are utilized to conclude on the critical dimensioning of the structures in order to tolerate the inter-tier electromagnetic interference.

3.1 3D sequential structure description

3DSI can feature different technologies at each tier in order to take full advantage of a given technology's potential for a specific application (digital, analog, mixed-signal/RF), as illustrated in Fig.

3.1. A good candidate for 3DSI is any stackable device that follows the SOI device architecture and especially thin-film devices. The last suggests that the devices can be implemented for example using the FD-SOI structure, described in chapter 2.

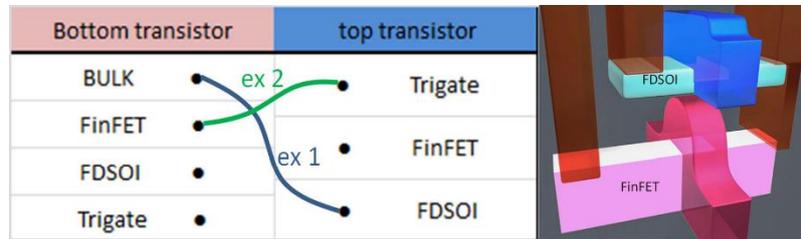


Fig. 3.1 Device architectures for top and bottom tiers in a 3DSI scheme [27].

In summary the FD-SOI structure presents the following differences compared to the conventional BULK MOSFET:

- The channel is un-doped (or very lightly doped). As a result, the short channel effects, as well as the variability of electrical parameters among devices with major source the random dopant fluctuations, are greatly reduced.
- The Body of the transistor is made ultra-thin for better electrostatic control.
- The Source/Drain diffusion areas are elevated to reduce series resistance.
- In order to reduce the capacitive coupling of the Source/Drain diffusion areas, the BOX thickness is reduced and a highly doped silicon layer is placed beneath, commonly called the GP. This more advanced architecture is used widely nowadays and is named Ultra-Thin Body and BOX (UTBB) FD-SOI.
- The GP doping can also help tune the threshold voltage value.

As in a conventional planar process, in 3DSI there are two major sections, the Front-End-Of-Line (FEOL) and the Back End Of line (BEOL). In the former active devices (transistors) and passive elements (capacitors, resistors, etc.) are patterned in a semiconductor layer whereas the latter contains all the metal layers used to interconnect the FEOL devices.

A schematic cross-section view of a 3D sequentially integrated structure is presented in Fig. 3.2. The top tiers of devices can be stacked right after the bottom tier process as shown in Fig. 3.2 (a), or there can be an intermediate Back-End-Of-Line (iBEOL) between the active device tiers, as depicted in Fig. 3.2 (b). The direct stacking of devices (Fig. 3.2(a)) is considered as the ultimate level

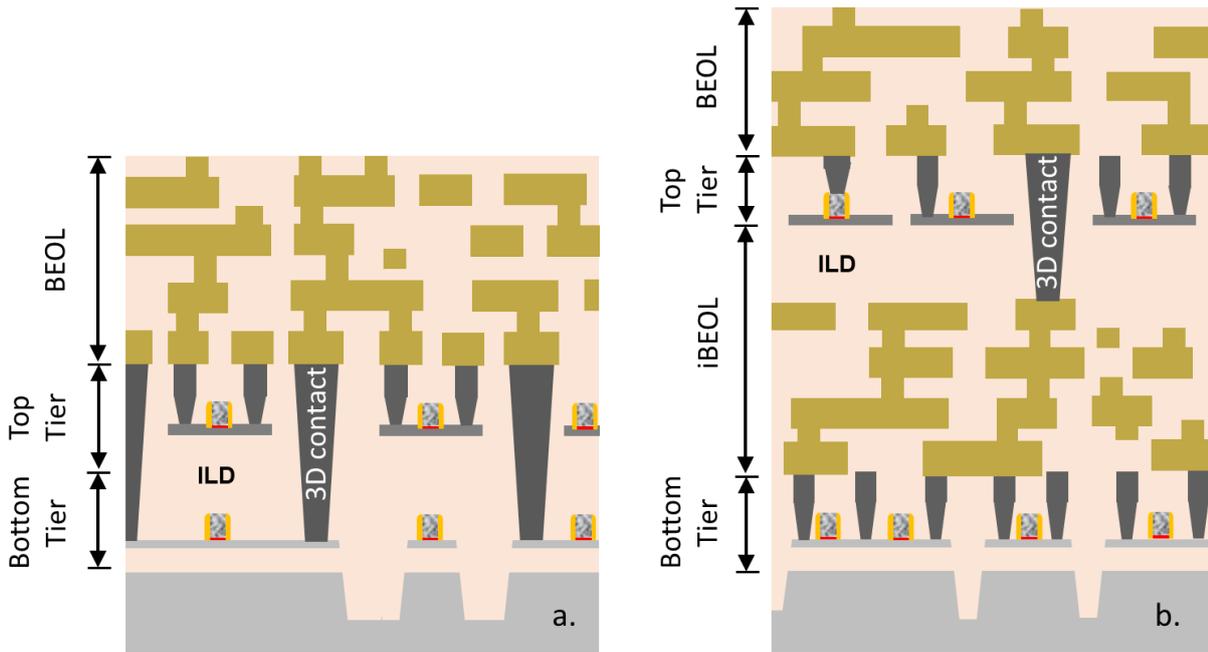


Fig. 3.2 Arrangement scheme of sequential tiers in 3DSI. (a) Direct device stacking (b) Tiers separated by an iBEOL.

of 3D integration, enabling the highest density of 3D contacts. In this scheme the Contacted Poly Pitch (CPP) can reach the value of the one in planar integration.

3.1.1 Mixed-signal opportunities by the use of 3DSI

In 3DSI each tier can host either digital, analog or mixed-signal/RF applications separated by an ILD with thickness in the range of 100nm to 1 μ m, as shown in Fig. 3.3.

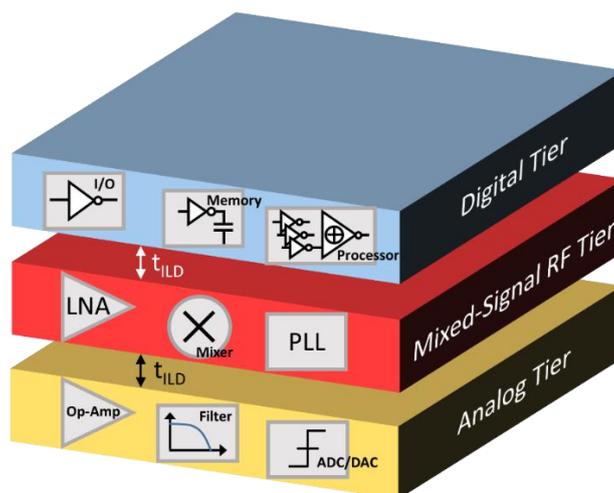


Fig. 3.3 Heterogeneous tier stacking in 3DSI.

In particular, the digital tier can consist of logic gates, memory circuits, processors while an analog tier can have op-amps, filters, ADCs/DACs. Mixed-Signal tiers can have all the previous with

additional RF blocks such as mixers, PLLs, LNAs. The key parameters that differentiate each tier in terms of electromagnetic interference with its adjacent ones are the maximum voltage swing and the frequency band that they utilize, with typical 28nm node values presented in Table 3.1.

Table 3.1 Typical 28nm node power supply range and frequency band utilized by each tier

	V _{DD}	Typical frequency band
Digital	1V	> 1 GHz
Analog	2.5V	< 1 MHz
Mixed-Signal/RF	1V/2.5V	> 1 GHz

The objective of this chapter is to examine the immunity of each tier to the electromagnetic interference by the adjacent one at a device level. However, this does not ensure that a hard conclusion can be drawn for all cases of applications unless the electromagnetic coupling at a circuit level is examined. For instance, digital circuits like logic gates have an inherent immunity to noise in principle, yet there are sensitive digital circuits like memories that noise can be harmful for their stability [86].

3.1.2 3DSI process flow for digital devices

The 3DSI process flow scheme [19] for digital devices (EOT≈1nm, V_{DD}=1V) is depicted in Fig. 3.4. On the bottom tier, standard high temperature (maximum TB of 1050°) CMOS devices are fabricated on 300mm SOI wafers with raised source and drain junctions activated at 1050°C. In addition, the bottom device gate stack is comprised of a HfSiON/TiN/Poly-Si sequence. Afterwards, NiPt_{10%} silicidation and pre-metal dielectric deposition are done, followed by a Chemical-Mechanical Polishing (CMP) process which planarizes the whole structure surface.

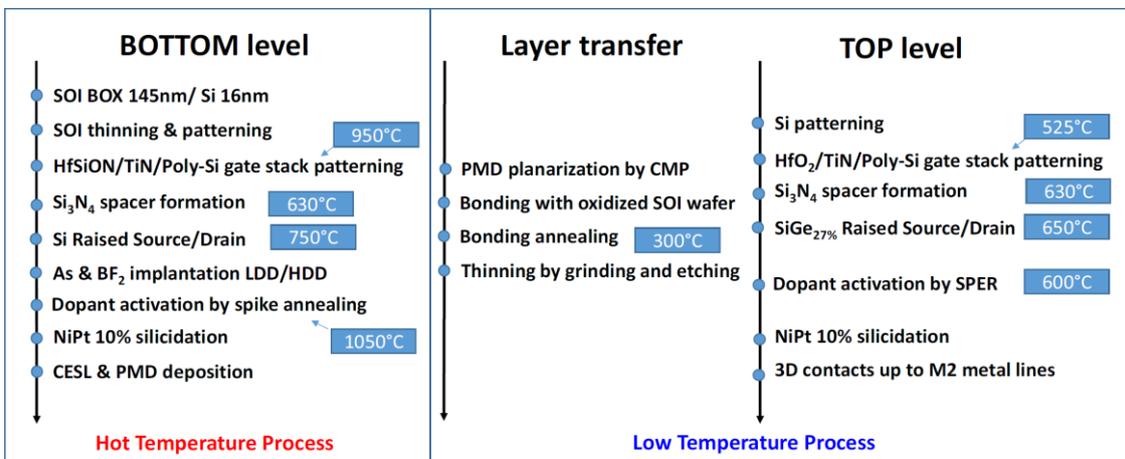


Fig. 3.4 3D sequential process flow [19].

In order to process the upper tier, conventional high temperature methods can degrade the bottom tier device performance. It has been reported in [87], [88] that a 950°C annealing results in such degradation. This restricts the TB for the top tier to a time-temperature window (Fig. 3.5) which prevents the bottom tier from any degradation [89].

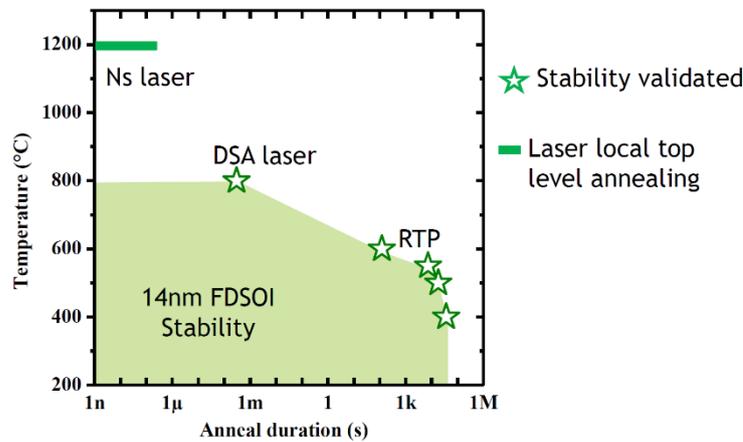


Fig. 3.5 TBs tested on FDSOI technology with SiGe channel for pFET and SiGe:B/ SiC:P RSD with preserved N & PFET I_{ON} I_{OFF} performance [89].

Taking this into account, a 10nm thin silicon layer of an oxidized SOI wafer is then transferred by direct bonding, through a low temperature 300°C bonding annealing. Grinding combined with sequential wet and dry etching is utilized to thin down the entire structure. Next, the HfO₂/TiN/Poly-Si gate stack is formed followed by a spacer zero deposition at 630°C and a selective SiGe_{27%} raised source drain epitaxy at 650°C for both NMOS and PMOS transistors. Lastly, Solid Phase Epitaxy Regrowth (SPER) [89] is used to activate the junctions at a relatively low temperature (600°C for 1 minute) while keeping low variability [90].

As observed from Fig. 3.5, the maximum TB for the top tier process, not resulting in a bottom tier device degradation, is 650°C for 20min, due to the raised source/drain processing. As a consequence, compared to the bottom TB, the top tier devices can be referred to as “Low Temperature” (LT) devices.

In case there is an iBEOL between the tiers, refractory metals are preferred, such as tungsten. The 3D contacts that are used to link the two tiers, called also Monolithic inter-Vias (MIVs), are done sequentially after the top LT process using standard tungsten plug in oxide connecting iBEOL to the final BEOL, which is a standard Cu/Low-k back-end. It is worth mentioning that the 3D contact scales with the device technology (e.g for a 28nm node it has 40nm width) while it has a higher AR than

normal contacts, determined by the ILD thickness. As a result, it is preferred to keep a small 3D contact AR by limiting the ILD thickness to several hundreds of nanometers.

3.1.3 Characteristic dimensions and performance of 3DSI devices under test

The characteristic dimensions of the devices are shown in Fig. 3.6 (a). Both devices at the top/bottom tiers feature a gate oxide of equivalent thickness $EOT=1.12\text{nm}$ for a power supply voltage $V_{DD}=1\text{V}$, a silicon film of thickness $t_{\text{si}}=7\text{nm}$ and a nominal gate length of 28nm . The BOX of the bottom devices has thickness $t_{\text{BOX}}=145\text{nm}$ while the tiers are separated with an ILD of a thickness equal to $t_{\text{ILD}}=130\text{nm}$ without iBEOL. A Transmission Electron Microscopy (TEM) cross-section of the 3DSI devices under test is presented in Fig. 3.6 (b), showing an excellent alignment precision of the 3D contacts between tiers.

The static performance and reliability of top/bottom devices in the 3DSI scheme under study have been analyzed in depth in [91], highlighting a minor impact of the top-tier processing on the performance and reliability of the bottom-tier devices.

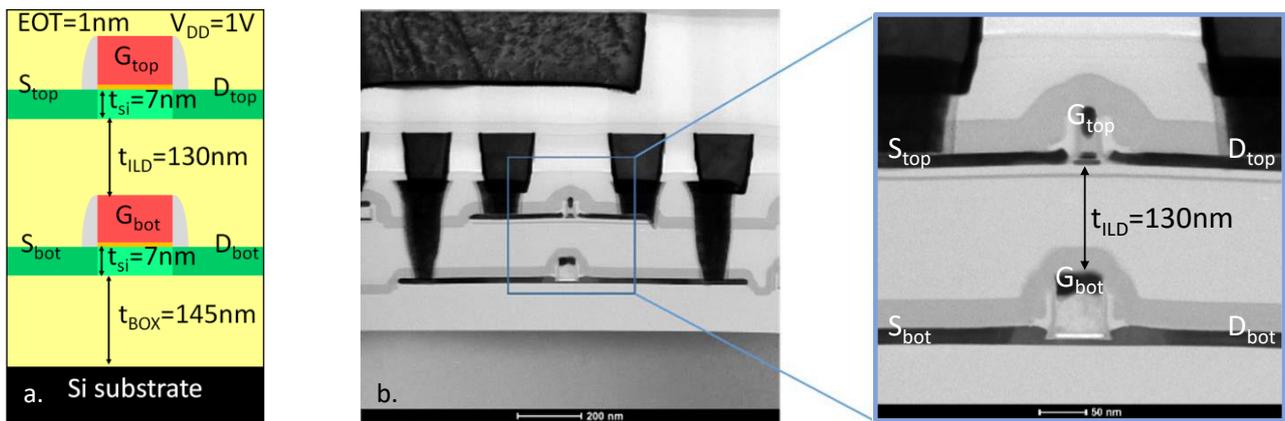


Fig. 3.6 (a) Schematic of the structure under study (b) TEM cross-section of two stacked transistors in 3DSI [19].

Regarding the top-tier devices, their performance has been shown to be comparable to the bottom ones while they satisfy the BTI reliability requirements. In addition, the RF performance of the top/bottom-tier devices has been investigated in [92]. The authors highlight state-of-the-art RF Figures Of Merit for the present 3DSI scheme, with the top tier PMOS devices featuring $f_t=55\text{GHz}$ and $f_{\text{max}}=80\text{GHz}$ at $V_{DD}=1\text{V}$, without altering those of bottom tier devices.

3.1.4 Structure layout of 3DSI devices under test

The structure of Fig. 3.2 (a) can be characterized as the most critical in terms of electromagnetic coupling due to the direct stacking of active device layers, i.e., each one can be an

aggressor to the other. Thus, for the purpose of this study, top-bottom devices were selected in the layout configuration of Fig. 3.7. The minimum gate length of the masks is 30nm as in 28nm FDSOI process, however the density of both the top tier and 3D contacts, is similar to that of a 65nm node.

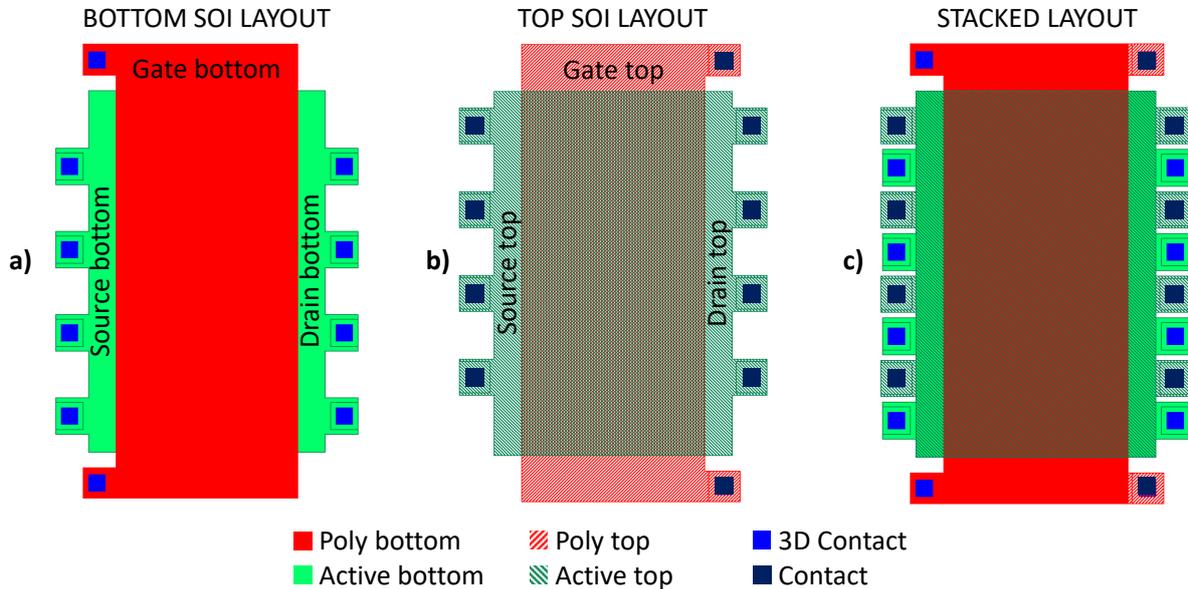


Fig. 3.7 Layout view of (a) bottom device and (b) top device. (c) Combined top+bottom layout view.

To maximize coupling effects, the gates of top/bottom devices were designed to be equal in dimensions while maintaining the same footprint for the two devices. Indeed, devices placed on the top tier in a 3DSI technology must respect the positioning of bottom tier devices. To accomplish that, the active area is patterned in such a manner that the 3D contacts have been placed between the contacts of the top tier devices (Fig. 3.8).

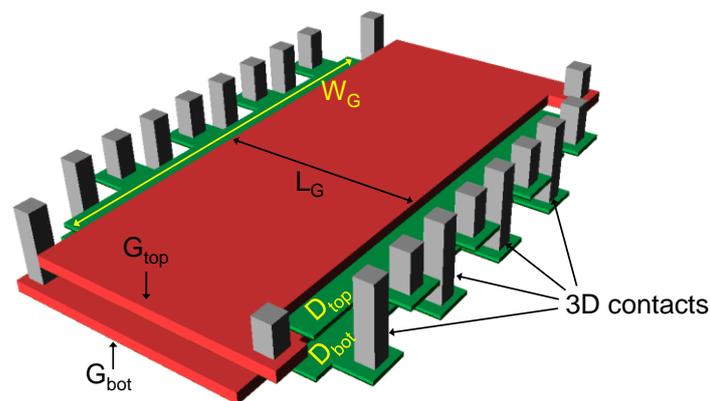


Fig. 3.8 3D Schematic view of the structure under test.

To assess the susceptibility to electromagnetic coupling, it is adequate to begin by selecting the same device type (NMOS or PMOS) for the two tiers in order to observe if there is any coupling impact. Thus for this study, NMOS devices were selected for both top and bottom tiers. Nonetheless,

the impact of the device type on the coupling induced effects will be investigated in section 3.2.2.a. The static measurements were performed with the Agilent B1500A device parameter analyzer and the low-frequency noise measurements with the NOISYS7 equipment by Synergie Concept [93].

3.2 Impact of DC coupling on top/bottom device performance

In this section, the impact of static (DC) coupling among top and bottom tier devices is investigated experimentally. Two cases are examined, one where the top device is the aggressor and the bottom one is the victim (Fig. 3.9 (a)) and vice versa (Fig. 3.9 (b)).

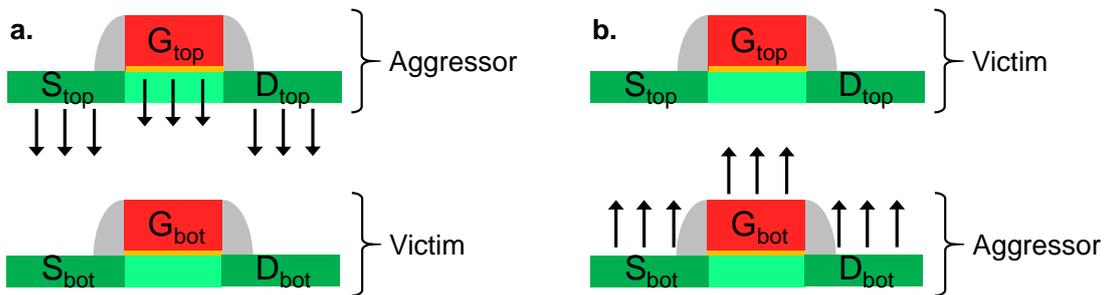


Fig. 3.9 Cases studied for the interference of adjacent devices in 3DSI. Aggressor is the top device while victim is the bottom one in (a) and vice versa in (b).

3.2.1 Experimental results

3.2.1.a Bottom-tier device electrostatic results

The impact of the static polarization applied to the top tier NMOS device on the performance of the bottom tier NMOS device was studied extracting the input characteristics of the latter while varying the top device gate bias (V_{Gtop}) from 0 to V_{DD} (0.9V). The results are shown in Fig. 3.10 (a) for

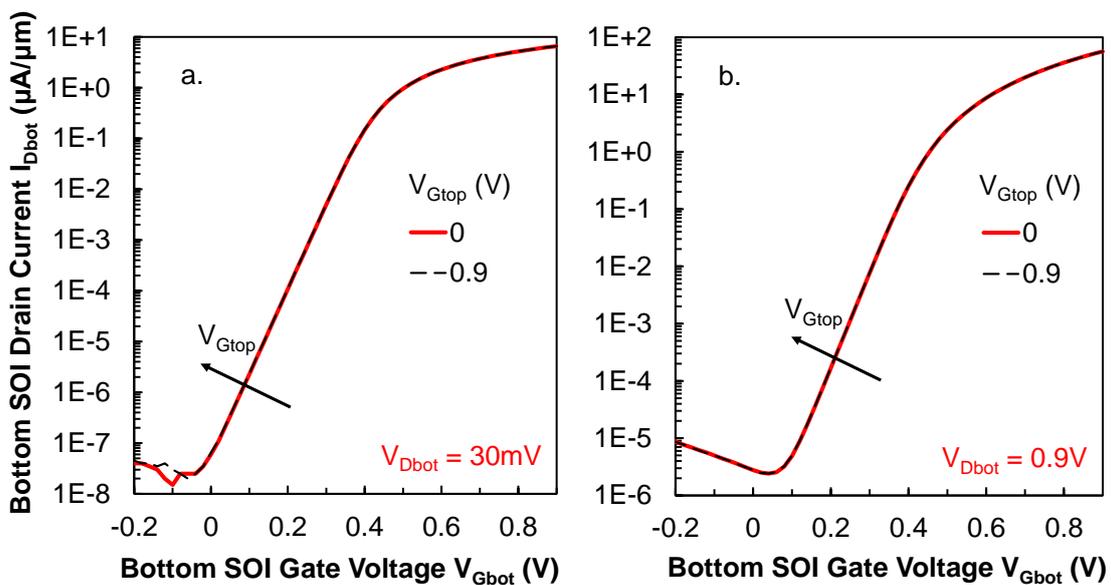


Fig. 3.10 Drain current versus gate voltage for bottom tier NMOS device with $L_G=1\mu m$.

a $V_{Dbot}=30mV$ and for $V_{Dbot}=0.9V$ in Fig. 3.10 (b).

As observed, there is no impact of V_{Gtop} on the bottom device input characteristics. This result is quite reasonable considering that the bottom device electrodes being polarized, shield the bottom device channel from the top-tier device electrodes electric field (Fig. 3.11).

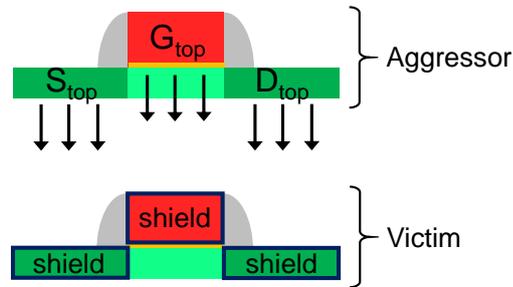


Fig. 3.11 The bottom-tier device channel is shielded effectively against static coupling from the top-tier device.

3.2.1.b Top-tier device electrostatic results

Applying the same concept but this time inverting the victim-aggressor role for the two devices as shown in Fig. 3.9 (b), the input characteristics of the top device are obtained now varying the bottom device gate bias from 0 to V_{DD} (0.9V). Fig. 3.12 (a) demonstrates the experimental results for a $V_{Dbot}=30mV$ and Fig. 3.12 (b) for $V_{Dbot}=0.9V$.

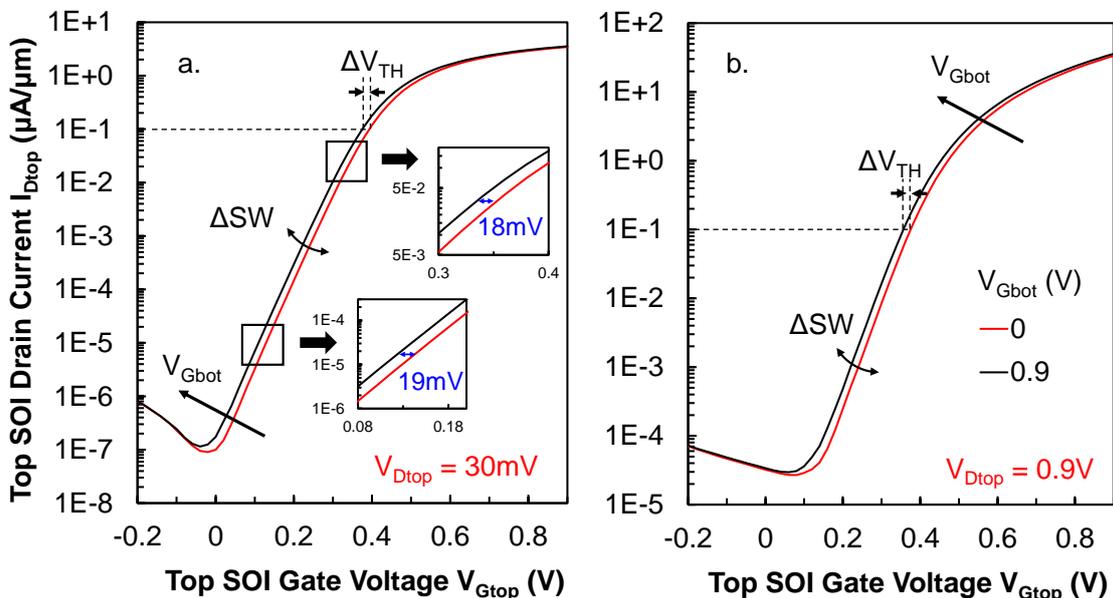


Fig. 3.12 Drain current versus gate voltage for top tier NMOS device with $L_G=1\mu m$.

As can be observed there is a shift of the top device I_D-V_G curve with the application of a positive bias at the bottom device gate electrode resulting in a threshold voltage shift ΔV_{TH} , as well as a slight change in the sub-threshold swing ΔSW . This behavior is attributed to the asymmetrical SOI

MOSFET structure of the top devices, having an equivalent BOX thickness equal to the one of the ILD separating the two tiers. Thus, each one of the bottom device electrodes (G_{bot} , D_{bot} , S_{bot}) may act like a Back-Gate for the top device modifying its performance. However, the bottom device gate electrode dominates over the other two electrodes due to its proximity to the top device channel. Hence, the maximum impact on the top device performance occurs when the bottom gate bias equals the power supply voltage (V_{DD}).

In order to extract the values for the coupling-induced ΔV_{TH} and ΔSW for the given process, statistical measurements were performed with a large set of experimental data at different gate bias of the bottom transistor, i.e., $V_{Gbot} = 0$ V (bottom device OFF), 0.9 V (bottom device ON) and -0.9 V (lower voltage limit for further verification of $V_{Gbot} = 0.9$ V), as shown in Table 3.2. The gate voltage of the top tier devices was varied from $V_{Gtop} = 0$ V to 0.9 V in linear region of operation with the application of a 30 mV to the drain voltage V_{Dtop} in order to avoid saturation effects that might mislead our conclusions.

Table 3.2 Bottom-tier NMOS gate biasing cases

	Bottom OFF		Bottom ON
V_{Gbot}	-0.9 V	0	0.9 V

For the purpose of this study, we selected a set of 126 dies for the top tier device displaying good characteristics. Fig. 3.13 shows the I_{Dtop} - V_{Gtop} characteristics of NMOS devices with $L_G = 1 \mu m$ with the black trace being the best die characteristic (in terms of I_{on}/I_{off}).

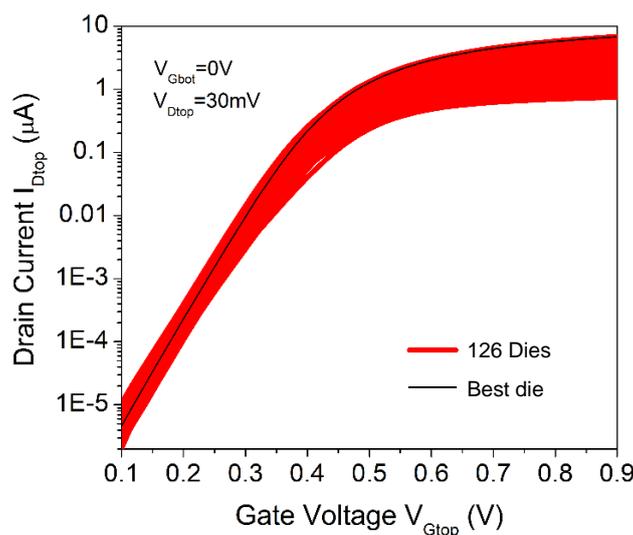


Fig. 3.13 Drain current versus gate voltage for top-tier NMOS devices stacked on bottom-tier NMOS devices, both with $2 \mu m^2$ area (total of 126 dies) where the black trace refers to the best die characteristic (in terms of I_{on}/I_{off}).

A modified Y-function method [94] was applied to extract the threshold voltage, V_{TH} , values for all 126 dies. As shown in Fig. 3.14, the coupling-induced V_{TH} shift, ΔV_{TH} , was found to be equal to $-15.6\text{mV} \pm 3\text{mV}$ and $14.7\text{mV} \pm 2.4\text{mV}$ for positive and negative V_{Gbot} bias, respectively.

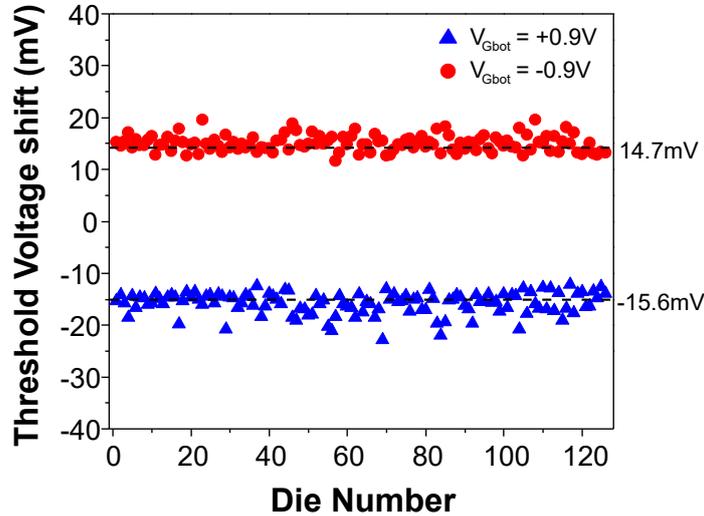


Fig. 3.14 Threshold voltage shift of top-tier NMOS devices in linear regime ($V_{Dtop} = 30\text{mV}$), at different bottom-tier NMOS biases.

3.2.1.c Top-tier device LFN results

The drain current noise spectral density was measured from weak to strong inversion for all bottom gate bias cases shown in Table 3.2. In order to neglect the shift in the DC value of I_{Dtop} , the measured noise was normalized by I_{Dtop}^2 . Fig. 3.15 illustrates the corresponding spectra for three V_{Gtop} values. Fig. 3.16 shows the normalized PSD value as extracted at $f = 10\text{Hz}$ versus drain current for all the bottom gate bias cases shown in Table 3.2 for two different device gate lengths $L=1\mu\text{m}$ and $L=0.1\mu\text{m}$.

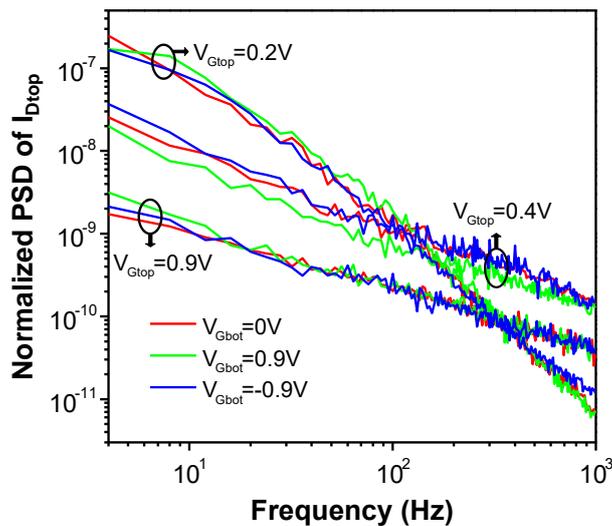


Fig. 3.15 Normalized drain current PSD vs frequency for a top-tier NMOS with $W = 2\mu\text{m}$, $L = 1\mu\text{m}$, for all the bottom-tier NMOS biases shown in Table 3.2.

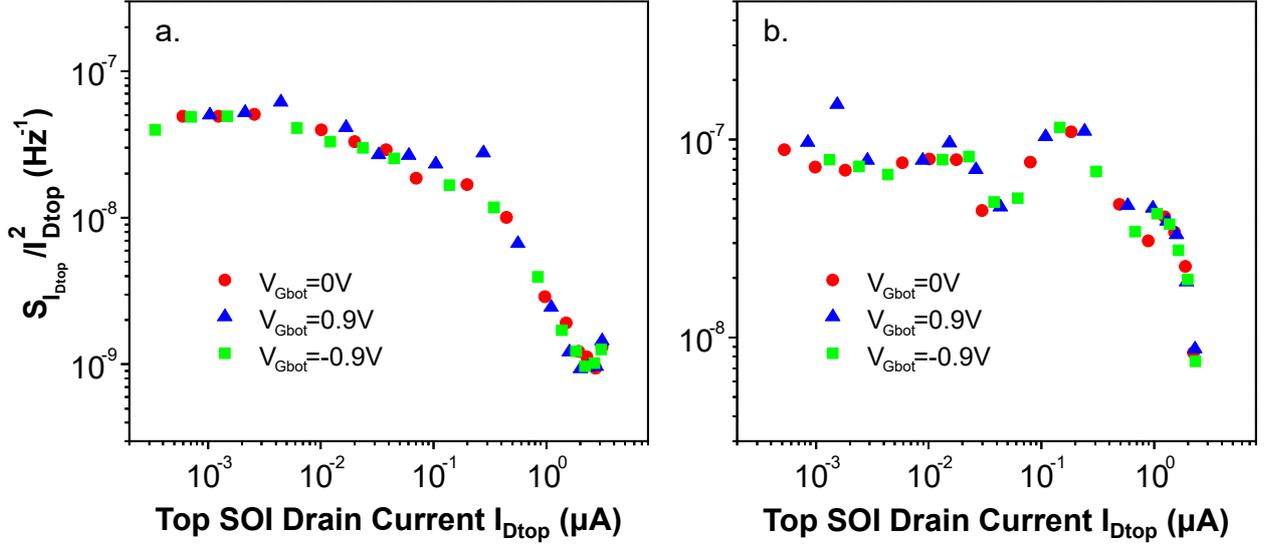


Fig. 3.16 Normalized PSD at $f = 10$ Hz vs drain current for a top NMOS with $W = 2 \mu\text{m}$, $L = 1 \mu\text{m}$ (a) and $L = 0.1 \mu\text{m}$ (b), for all the V_{Gbot} cases shown in Table 3.2.

Fig. 3.15 and Fig. 3.16 show that, contrary to the impact on the static behavior, no noticeable coupling effect is observed in the current-normalized LFN spectra behavior. As Fig. 3.16 (a) shows, the LFN level at $L = 1 \mu\text{m}$ can be considered unchanged whatever the bottom-tier gate bias, from subthreshold to strong inversion region. The same is true for the top-tier devices with $L = 0.1 \mu\text{m}$, however, as shown in Fig. 3.16 (b), the general LFN dependence on top-tier gatebias is not the same. The latter is a typical behavior for sub- μm MOSFETs, where the noise spectra are not $1/f$ -like in most cases, but dominated by Lorentzian noise, responsible for the observed humps [95].

In previous studies, it has been shown that the bottom gate bias of a FDSOI MOSFET can strongly affect the remote Coulomb scattering between carriers and trapped charge [96], [97], leading to a change in the Correlated Mobility Fluctuations (CMF) factor Ω in the $1/f$ noise model given by [98]:

$$\sqrt{S_{Vg}} = \sqrt{S_{Vfb}} \left(1 + \Omega \frac{I_d}{g_m} \right) \quad (3-1)$$

where $S_{Vg} = S_{Id}/g_m^2$ is the input-referred gate voltage noise PSD, S_{Vfb} the flat-band voltage noise PSD and g_m the transconductance.

Therefore, in order to verify if the bottom transistor gate bias under normal operation can affect the CMF factor Ω , we plotted the square root of the input-referred gate voltage noise, S_{Vg} , versus I_d/g_m for the top-tier device. As one can observe in Fig. 3.17, in all three cases (

Table 3.2), there is the same linear dependence, so that the extracted Ω factor (inset) can be considered constant with V_{Gbot} .

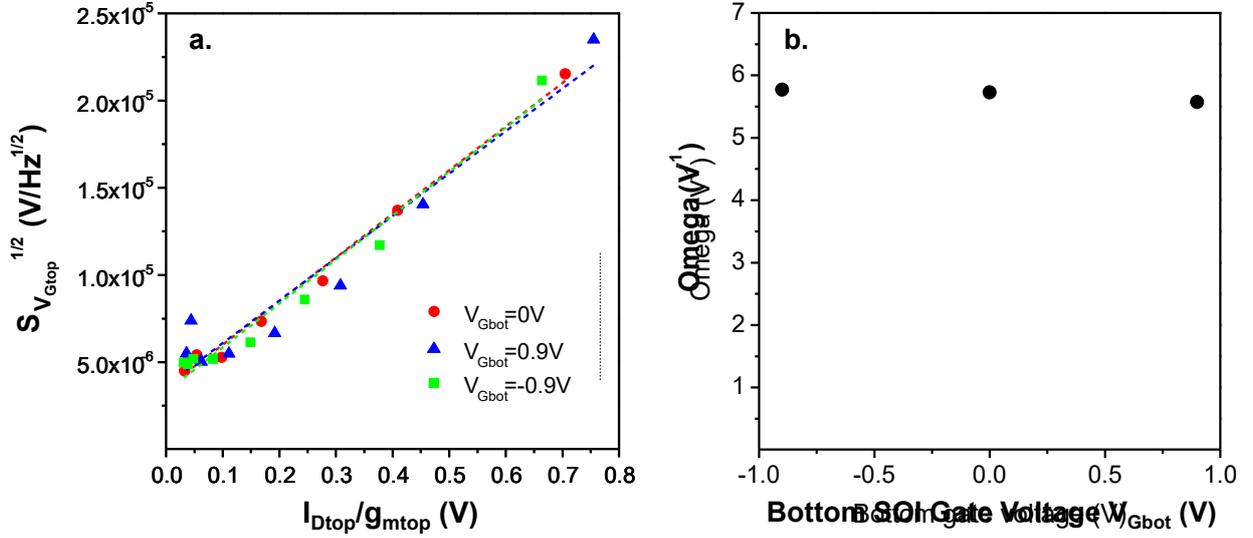


Fig. 3.17 Square root of input-referred gate voltage PSD SV_g versus I_d/g_m for a top NMOS with $W=2\mu\text{m}$, $L=1\mu\text{m}$, for all the bottom-tier NMOS biases shown in Table 3.2.

3.2.1.d Charge-coupling factor extraction and influence of SCE

As analyzed in chapter 2, the back to front interface charge coupling of the depleted silicon film is attributed on the capacitive network formed between the front and back gate electrode of the FD-SOI device. The charge-coupling factor r (mV/V) describes the sensitivity of V_{TH} to changes in the back-gate voltage (in our structure the bottom device gate voltage) and flat-band voltage [99]. It is an inherent property of the device structure and is defined by

$$r = \frac{C_{b(eff)}}{C_{ox}} \quad (3-2)$$

where $C_{b(eff)}$ is the effective body capacitance and C_{ox} is the gate oxide capacitance, both per unit area.

To experimentally extract the charge-coupling factor for the top devices, the bottom SOI gate voltage was swept from -20V to +20V with a step of 2V while extracting the top NMOS device input characteristics. Following the same procedure as previously for the threshold voltage extraction, the results for each bottom gate bias are shown in Fig. 3.18. As observed, the threshold voltage of the top device decreases with a positive bottom gate bias because of the weak inversion occurring at the

back interface. On the contrary, for a negative bottom gate bias the back interface is gradually going from depletion to accumulation. The $\Delta V_{TH,top}/\Delta V_{Gbot}$ slope for the negative and positive gate bias describes the rate of change of the top device threshold voltage with the bottom gate bias.

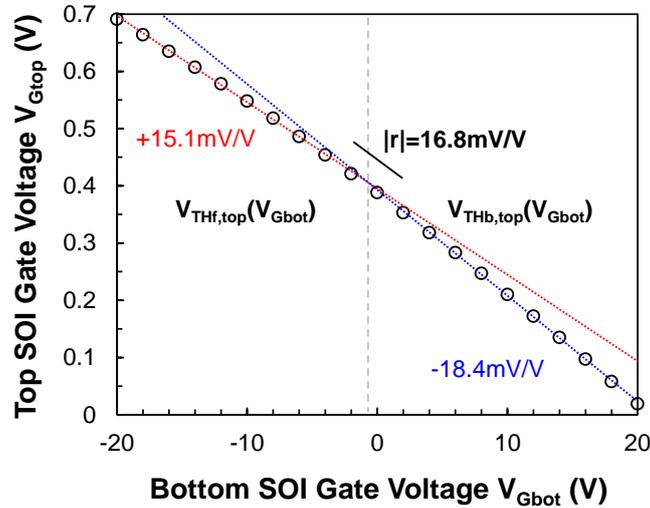


Fig. 3.18 Top SOI Gate Voltage versus the Bottom SOI Gate Voltage. The charge-coupling factor is the slope of the curve.

The median of the slopes in the two different modes of back-gate operation yields a value of the charge-coupling factor $|r|=16.8\text{mV/V}$. This value is in line with the extracted threshold voltage shift median value from the statistical measurements, presented in the previous section. Additionally, Fig. 3.18 reveals the coupling-induced threshold voltage shift by an analog device placed at the bottom tier with $V_{DD}=2.5\text{V}$. Therefore, a $\Delta V_{Gbot}=2.5\text{V}$ corresponds to a $\Delta V_{TH,top}=44\text{mV}$.

Since the charge-coupling factor relies on the device and generally the structure geometry, parameters such as the electron/hole mobility, series resistance and temperature have no influence on the coupling-induced Threshold Voltage shift ΔV_{TH} of the device. In contrast, it has been demonstrated that there is a dependence of the charge-coupling factor on Short Channel Effects (SCEs) and Quantum Mechanical (QM) effects [99], [100]. These two effects result in a widening of the back (bottom in our structure) gate-bias range for charge coupling, as they tend to move the inversion-charge centroid away from the two interfaces [99].

To assess the impact of SCE, the charge-coupling factor was extracted for devices with $1\mu\text{m}$ and 100nm gate length corresponding to the same die, for 5 dies in total and the results are shown in Fig. 3.19. An apparent decrease of $\sim 1.2\text{mV}$ is observed, attributed to the reduction of the BG effective length of the top device.

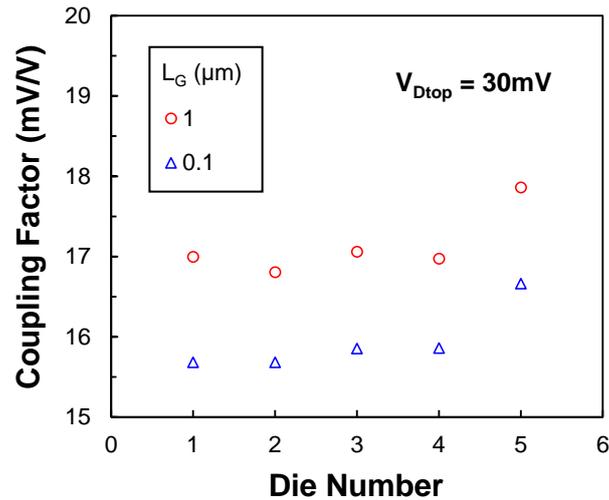


Fig. 3.19 Extracted charge-coupling factor for top devices with $L_G=1\mu\text{m}$ and $L_G=100\text{nm}$ (Total of 5 dies).

Moreover, Fig. 3.20 shows the influence of a top device high drain bias on the charge-coupling factor under the scaling effect. It is worth mentioning that the coupling induced ΔV_{TH} values for the top-tier device were extracted here with the constant current method [101] at $I_D = 100 \cdot \frac{W}{L} \text{ nA}$ since the Y-function method is not valid in the saturation region. As seen in Fig. 3.20, while there is no change in the charge-coupling factor with the drain bias regarding the $1\mu\text{m}$ device, a slight increase is observed for the devices with 100nm gate length. An intuitive explanation of this effect may be the worsening of the top device gate electrostatic control of the channel as the drain voltage increases, while the bottom device gate control strength remains the same.

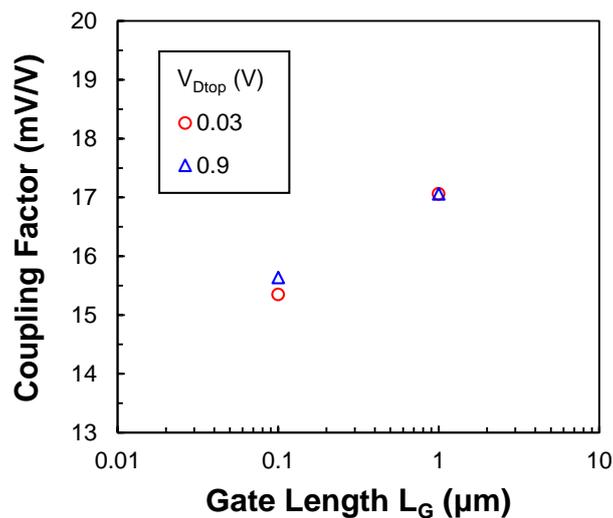


Fig. 3.20 Extracted median value of the charge-coupling factor for top devices versus the gate length, under $V_D=30\text{mV}$ and $V_D=0.9\text{V}$.

3.2.2 Simulation results

To further extend the analysis at device level, numerical simulations were performed using

Section 3.2 - Impact of DC coupling on top/bottom device performance

Silvaco TCAD device simulation tool ATLAS. The experimental structure was simulated (Fig. 3.21) setting the geometry and the materials used in the process while the parameters extracted from the experimental characterization were utilized to calibrate the simulation results. In addition, the necessary physics models (carrier continuity, drift, diffusion, generation-recombination, QM effects) were included in the device electrical simulation, to reproduce the observed experimental behavior.

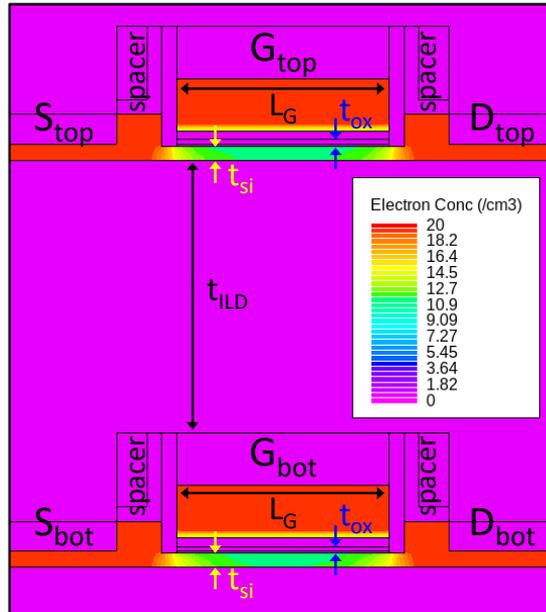


Fig. 3.21 Cross-section view of the TCAD structure simulated comprised by stacked NMOS devices showing the electron concentration.

The results (Fig. 3.22) show very good fitting between measurements and simulations concerning the static characteristics for the required transistor biasing. In detail both linear and saturation behavior as well as the 15.6mV shift of the top transistor’s threshold voltage due to bottom gate coupling, are accurately captured.

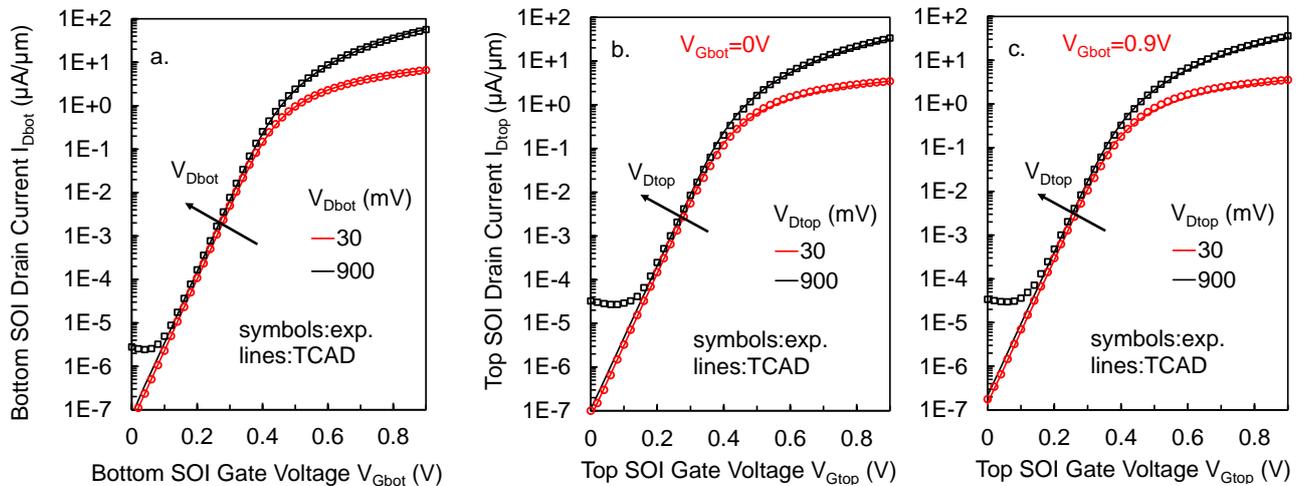


Fig. 3.22 Drain current versus gate voltage for a bottom-tier NMOS device (a) and a top-tier NMOS device for $V_{Gbot}=0V$ (b) and $V_{Gbot}=0.9V$ (c). Circles and lines denote experimental and simulation results.

3.2.2.a Impact of device type

The coupling induced threshold voltage shift ($\Delta V_{TH}(V_{Gbot})=V_{TH}(V_{Gbot})-V_{TH}(V_{Gbot}=0V)$) was extracted with the aid of TCAD simulations for NMOS and PMOS device type, while the bottom SOI gate voltage was swept from -20V to +20V with a step of 2V and the results are shown in Fig. 3.23.

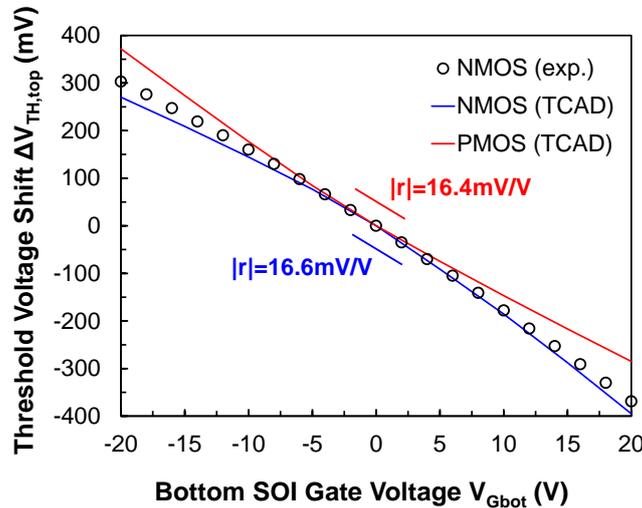


Fig. 3.23 Coupling induced ΔV_{TH} for top tier devices (blue and red lines for NMOS and PMOS device type respectively).

As observed while the two curves yield nearly the same charge-coupling factor, the rate of change $\Delta V_{TH}/\Delta V_{Gbot}$ alters between each device type under positive and negative V_{Gbot} . For instance, considering a positive V_{Gbot} , which is the actual scenario under circuit operation, PMOS devices yield a lower sensitivity to coupling effects. Consequently, assuming that the maximum power supply of the bottom devices is 2.5V for analog applications, PMOS experience a ΔV_{TH} slightly reduced by 1.25mV. An intuitive understanding of that effect can be obtained by extracting the carrier concentration versus the silicon film depth for the top-tier device in the threshold voltage condition ($V_{Gtop}=V_{TH}(V_{Gbot})$), as shown in Fig. 3.24 (a) for NMOS and in Fig. 3.24 (b) for PMOS.

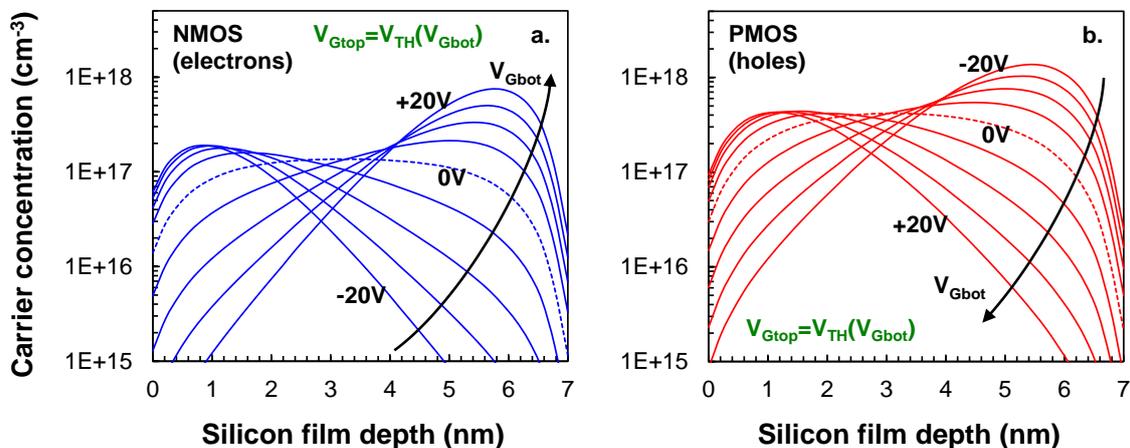


Fig. 3.24 Carrier concentration versus silicon film depth for NMOS (a) and PMOS device (b).

As observed, for PMOS the conduction path (charge centroid) moves from the center of the channel to the front/back interface in the reverse direction than in NMOS devices. Due to majority carriers being holes in a PMOS device channel, a negative bottom gate bias attracts the holes at the back channel while the front interface is depleted, enhancing the modulation by the bottom gate. On the other hand, a positive bottom gate bias depletes further the back interface setting the conduction path to the front interface, thus the front gate gains a better control of the carriers.

3.2.2.b Influence of SCE on the coupling induced ΔV_{TH}

As remarked in the experimental part, there is a reduction in the coupling induced threshold voltage shift by 1.2mV as the gate length of both top and bottom devices decreases from 1 μ m to 100nm. Extending the analysis by TCAD simulations, the threshold voltage shift (ΔV_{TH}) due to electrostatic coupling was extracted as a function of gate length (Fig. 3.25) and is in line with the experimentally extracted values. The static coupling decreases with the gate length due to the screening by the high source/drain electric field of the top-tier transistor and results in a reduction of the coupling-induced ΔV_{TH} by around 5mV for nominal gate length devices in 28nm FDSOI technology.

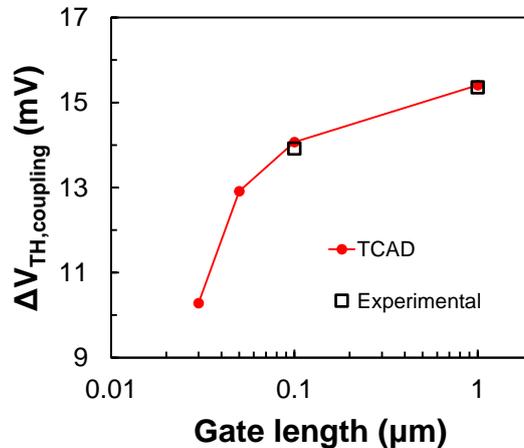


Fig. 3.25 $\Delta V_{TH,coupl}$ vs. gate length for a top tier device. 28FD nominal L_{Gtop} devices show better immunity to inter-tier DC coupling.

In order to assess how the top device threshold voltage reacts to higher bottom device gate bias in case of a 28nm nominal gate length device, the bottom SOI gate voltage was swept from -20V to +20V with a step of 2V while extracting the input characteristics for both NMOS and PMOS type of device (Fig. 3.26). Comparing in the same diagram the results for a 1 μ m gate length device, the decrease of the charge-coupling factor with the gate length is apparent for both devices. It is evident from Fig. 3.26 that in the case of higher power supplied devices being at the bottom tier, the coupling-induced threshold voltage shift can have a significantly reduced value. For instance, in the case of a

bottom analog device with $\Delta V_{Gbot}=2.5V$ the reduction of the coupling-induced ΔV_{TH} can be as high as 21mV for NMOS devices and 16.7mV for PMOS devices, when going from μm - to nm-range lengths.

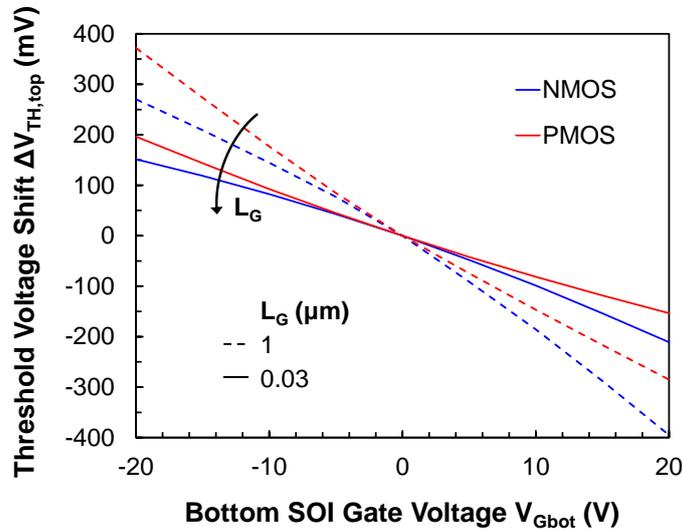


Fig. 3.26 Impact of gate length on the coupling induced ΔV_{TH} vs. V_{Gbot} for NMOS and PMOS top tier devices.

However, it must be noted that for operation in the saturation region, the coupling induced ΔV_{TH} is elevated for short channel devices ($L_G < 1\mu m$), as obtained from the TCAD simulations (Fig. 3.27), confirmed also by the experimental results in the previous section. This implies that in the saturation region there is a minimal increase of the coupling induced threshold voltage shift compared to the linear region. Again, the overall ΔV_{TH} decrease, from linear to saturation, obtained by using nominal gate length devices is valuable: 18.35mV for NMOS and 13.8mV for PMOS under a $\Delta V_{Gbot}=2.5V$.

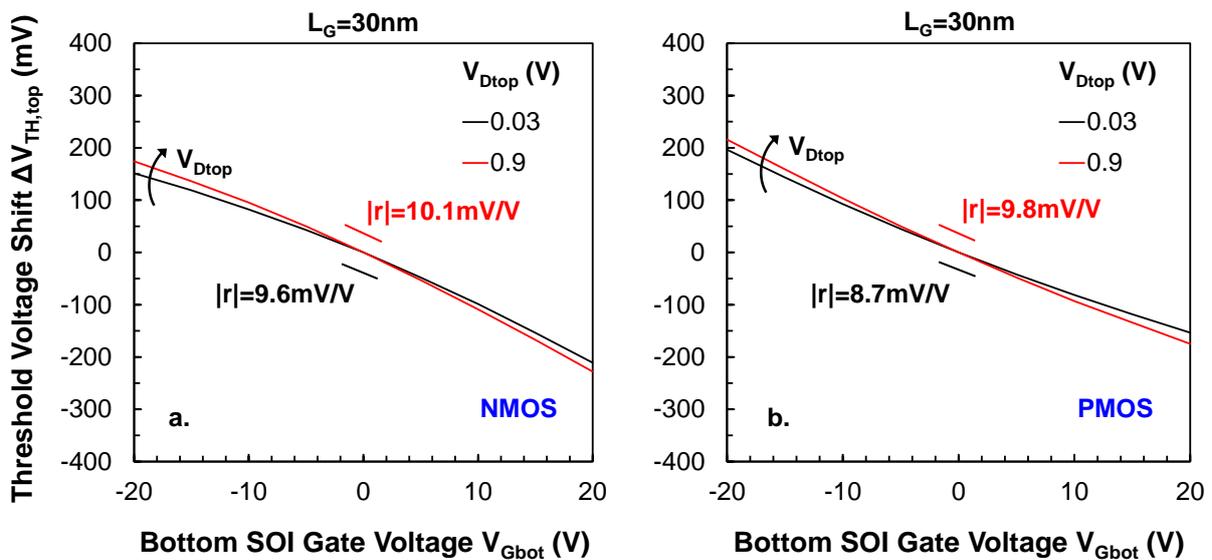


Fig. 3.27 Coupling induced ΔV_{TH} vs. V_{Gbot} for NMOS (a) and PMOS (b) top tier devices with $L_G=30nm$ under low and high V_{Dtop} .

3.2.2.c Impact of bottom/top length ratio on CF with regard to scaling

The impact of bottom/top length ratio (i.e., cases where the gate length of the stacked devices are not equal) on the charge-coupling factor will be investigated in this section. For the purpose of this analysis, an accurate extraction of the front- and back-channel threshold voltage is required, which can be performed by many methods (Constant Current (CC), transconductance, etc). Although the CC method has been utilized so far in order to compare experiments to simulations (unavailability of experimental structures for capacitance measurements), in this section the $\max(dC_{gc}/dV_g)$ method will be used from split C-V simulations.

With the aid of the $\max(dC_{gc}/dV_g)$ method, the threshold voltage has been determined from the position of the derivative peak of the top-tier device gate-to-channel capacitance (C_{gt-cht}) with respect to the gate voltage V_{Gtop} while varying the bottom-tier device gate voltage V_{Gbot} [100], under $V_{Dtop}=30mV$. This way the V_{TH} value is only influenced by the electrostatic (charge-related) behavior and not any transport-related effects (gate-voltage dependent mobility etc.). The procedure used to extract the coupling characteristics is illustrated in Fig. 3.28 for devices with $L_G=1\mu m$.

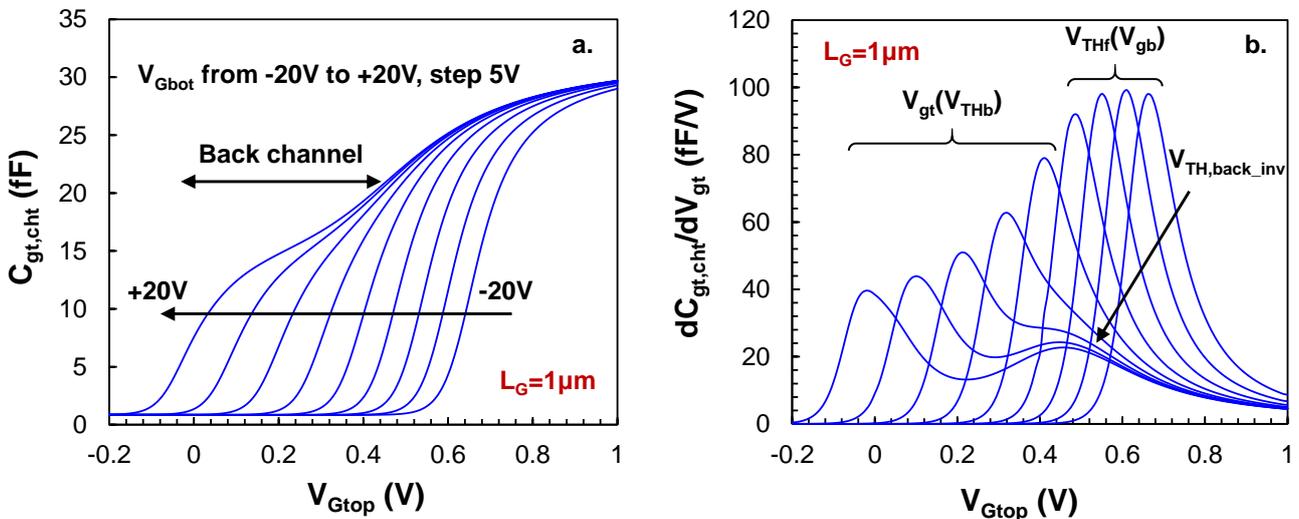


Fig. 3.28 TCAD results of the gate-to-channel capacitance C_{gt-cht} of the top-tier device versus its gate voltage (a) and their derivatives (b) for various bottom-tier gate voltages V_{gbot} , illustrating the procedure for extracting coupling characteristics ($L_G=1\mu m$).

Analyzing the results, for high positive values of V_{Gbot} , the C-V curves exhibit an additional curvature at low V_{Gtop} related to the inversion channel at the back interface; therewith, the corresponding dC_{gt-cht}/dV_{Gtop} curves reveal two clearly pronounced peaks:

- The first, is due to the activation of the back-channel, with its position at various V_{Gbot} yielding a relationship between V_{Gtop} and the back-channel threshold voltage $V_{TH,b}$.

- The second, whose position is invariable with V_{Gbot} , corresponds to the activation of the front channel, yielding the front-gate threshold voltage for the inverted back interface $V_{TH,back_inv}$.

For $V_{Gbot} \leq 0$, only a single peak in dC_{gt-cht}/dV_{Gtop} curves appears, corresponding to the activation of the front channel, and its shift with V_{Gbot} gives the $V_{THf}(V_{Gbot})$ dependence (i.e., the front-gate coupling characteristic). The extracted results concerning the coupling-induced ΔV_{TH} for NMOS devices can be seen in Fig. 3.29 along with the constant current method results. A difference among the two can be observed for strong negative and positive device gate bias, becoming more pronounced in the second case.

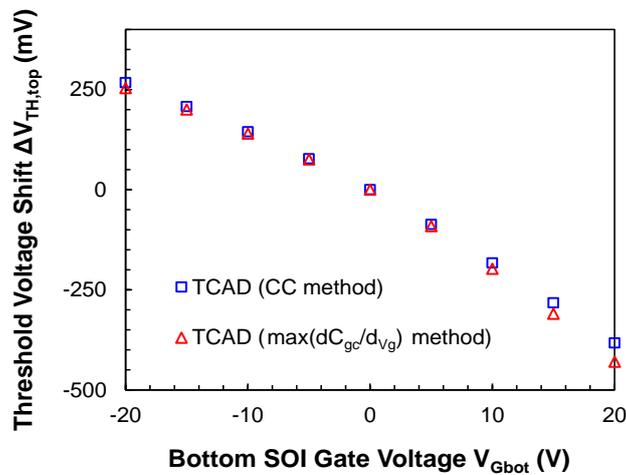


Fig. 3.29 Top SOI Gate Voltage versus the Bottom SOI Gate Voltage extracted from the C-V method described in this section compared to the I-V method followed in chapter 3.

Fig. 3.30 (a) shows the C-V results with its derivative in Fig. 3.30(b) for the critical case of stacked devices having both $L_G=30\text{nm}$, where an evident decrease of the back-bias sensitivity is observed. The latter corresponds to the impact of SCE as investigated in §3.2.2.b.

Carrying out the same procedure for a wide range of the top/bottom-tier device gate length combinations, the obtained charge-coupling factor values are plotted versus the ratio L_{Gbot}/L_{Gtop} in Fig. 3.31. Interpreting the results, one can observe that the top-tier devices with $L_{Gtop}=1\mu\text{m}$ approach the long-channel behavior, i.e., when $L_{Gbot} \geq L_{Gtop}$ the charge-coupling factor remains at a constant value, whereas for $L_{Gbot} < L_{Gtop}$ there is a reduction related to the top-tier channel/bottom-tier gate overlapping area. However, for sub-micrometer devices, the charge-coupling factor behavior deviates from the long channel one. As the top-tier device gate length approaches 30nm, the curve shifts towards the right of the diagram while the charge-coupling factor reaches higher values for both extreme cases of $L_{Gbot} \gg L_{Gtop}$ and $L_{Gbot} \ll L_{Gtop}$.

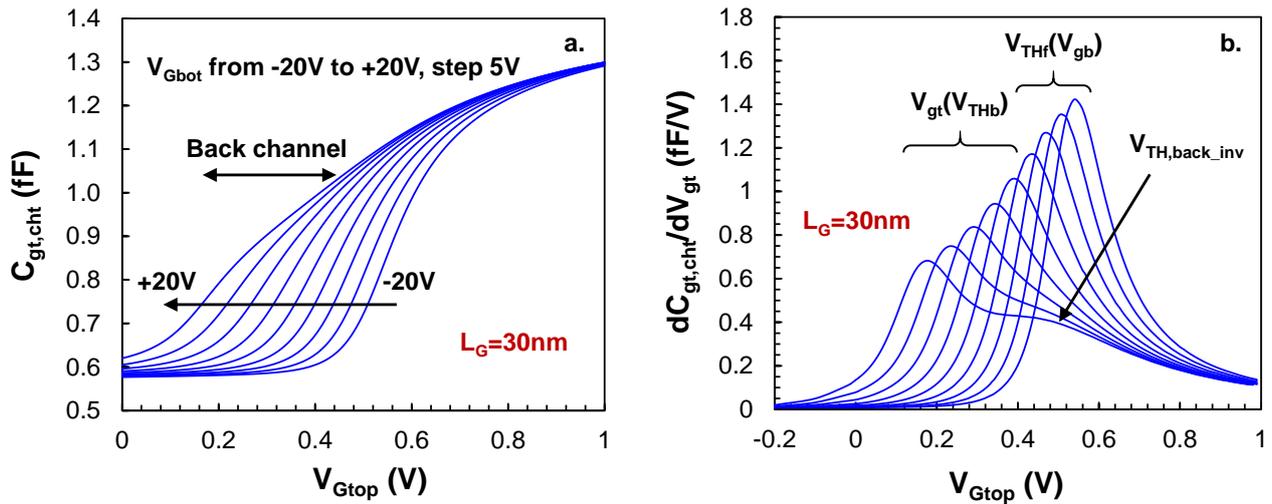


Fig. 3.30 TCAD results of the gate-to-channel capacitance C_{gt-cht} of the top-tier device versus its gate voltage (a) and their derivatives (b) for various bottom-tier gate voltages V_{gbot} , illustrating the procedure for extracting coupling characteristics ($L_G=30nm$).

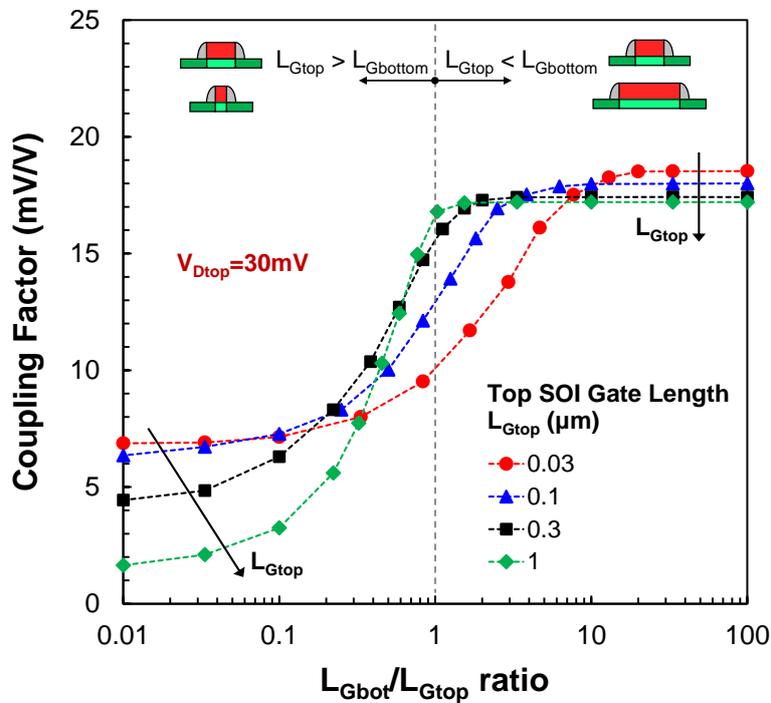


Fig. 3.31 Charge-coupling factor versus L_{Gbot}/L_{Gtop} ratio for different top-tier device gate length as extracted from TCAD simulations.

As a result, when $L_{Gbot}=L_{Gtop}$ the charge-coupling factor and hence the coupling-induced V_{TH} shift of the short-channel top-tier device appears to be reduced compared to a long-channel one (results of Fig. 3.25).

The above behavior is attributed to the SCE which decrease both the effective oxide capacitance ($C_{ox,eff}$) and ILD capacitance ($C_{ILD,eff}$) of top-tier devices. Indeed, electric field vector plots obtained from TCAD simulations (Fig. 3.32) reveal the impact of the fringing fields induced by the top

source and drain diffusion areas on the bottom-tier gate electrode electric flux. These fringing fields cause ultimately a reduction of the top device effective back-gate length $L_{G_{bot,eff}}$.

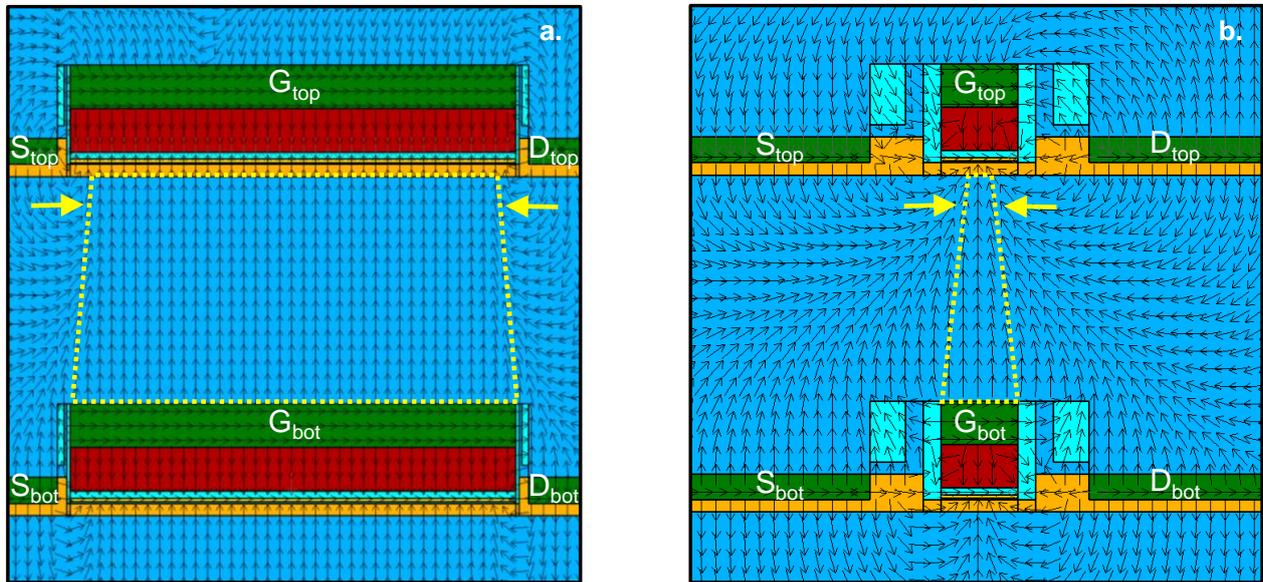


Fig. 3.32 Electric field vector plot showing the shape of the flux induced by the bottom-tier device gate electrode to the top-tier device channel for devices with equal gate length of (a) $L_G=1\mu\text{m}$ and (b) $L_G=30\text{nm}$.

3.2.2.d Impact of top/bottom device misalignment on CF

The relative misalignment of devices is an effect that can also impact the charge-coupling factor of the top-tier device. Misplacing by Δx the gates of two stacked devices, the charge-coupling factor is reduced since it depends on the overlapping area between the top-tier device channel and the bottom-tier device gate electrode (Fig. 3.33 (a)).

For stacked devices having equal gate length ($L_{G_{top}}=L_{G_{bot}}$), the impact of their misalignment on the charge-coupling factor is shown in Fig. 3.33 (b) as extracted from TCAD simulations, varying the gate length in the sub-micrometer range.

The concept of the effective front/back gate length for the top-tier device can be also applied here, as described in the previous section. Fig. 3.34 shows the electric field vector plot of two stacked devices with $L_G=100\text{nm}$ and 50% relative misalignment towards the drain direction. Because of the offset, the effective BG length for the top-tier device should be proportional to the overlapping area between the top-tier device channel and the bottom-tier device gate, and thus $L_{G_{bot,eff}}=L_{G_{bot}}/2$. However as observed, $L_{G_{bot,eff}}$ is degraded due to the electric field deformation from top-tier drain diffusion area as shown in Fig. 3.34.

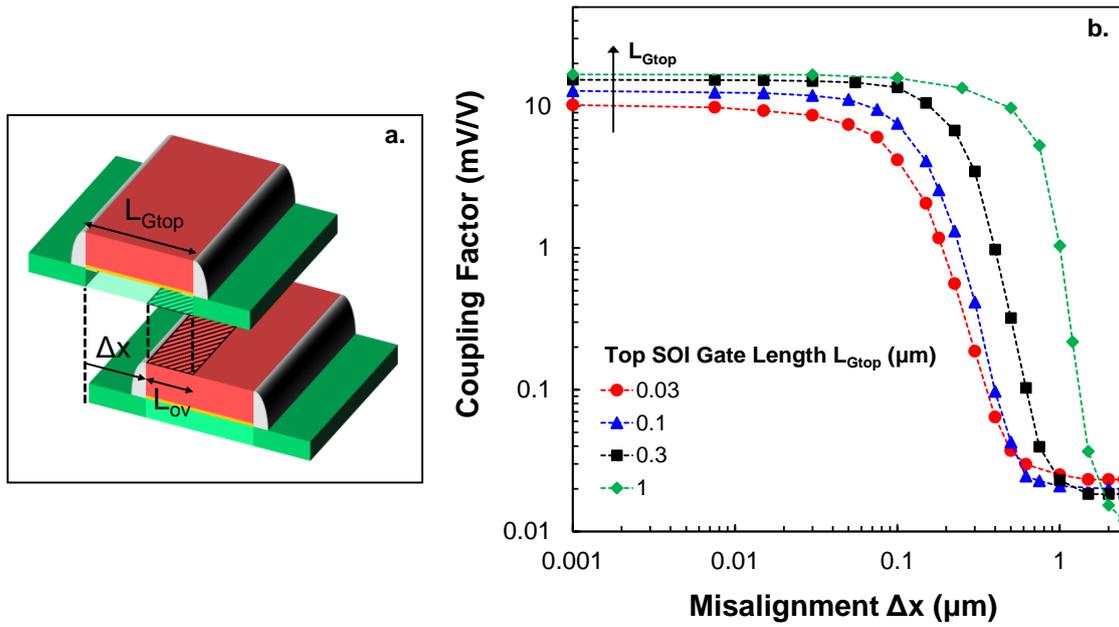


Fig. 3.33 (a) Schematic 3D illustration of the stacked devices with the top-tier having a relative misalignment from the bottom one and (b) Charge-coupling factor versus misalignment for different gate length ($L_{Gtop}=L_{Gbot}$) as extracted from TCAD simulations

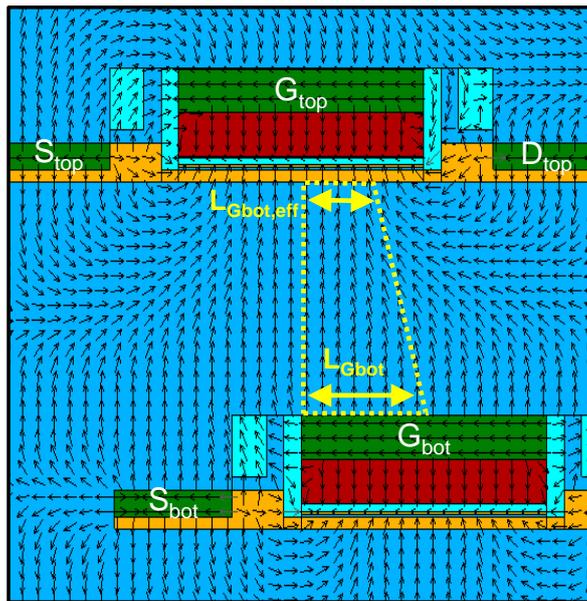


Fig. 3.34 Electric field vector plot showing the shape of the flux induced by the bottom-tier device gate electrode when the bottom device is misaligned by 50% relatively to the top-tier device.

3.2.3 Impact of static coupling on the performance of top-tier digital devices ($V_{DD}=1V$)

3.2.3.a Digital devices at the bottom tier ($V_{DD}=1V$)

The small difference between the measured absolute values of the coupling-induced V_t shift at positive and negative bottom-tier biases (Fig. 3.14) is attributed to the weak bottom interface

accumulation for negative V_{Gbot} , while the $\approx 15\%$ ΔV_{TH} variability is attributed to the variability in t_{ILD} (estimated to be $\pm 20\text{nm}$ for the wafer under study), due to the SOI coupling relation [74]:

$$\frac{\Delta V_t}{\Delta V_{Gbot}} = - \frac{C_{si(top)} C_{ILD}}{C_{ox(top)} (C_{ILD} + C_{si(top)})} \quad (3-3)$$

where $C_{si(top)}$, $C_{ox(top)}$, C_{ILD} are the top-tier channel, the top-tier oxide, and the ILD capacitances per unit area, respectively.

Fig. 3.35 (a) shows the expected amount of threshold shift at 1- σ (black line) and at 3- σ (red line) due to mismatch of 28nm FDSOI technology [72], as a function of the reciprocal of the geometrical mean of the device dimensions. The extracted average ΔV_{TH} of around 15 mV is also plotted (blue line). Although there is a dependence of the coupling-induced ΔV_{TH} on the device gate length, here it will be considered constant and equal to the maximum value for the simplicity of the analysis. At an ILD thickness of 130nm, the maximum gate area for which the coupling-induced ΔV_{TH} does not exceed the mismatch variations is much higher than the typical gate areas used in digital circuits. This is due to the power supply rails (V_{DD} and GND) distance limitations the device gate is restricted to an area below $0.01 \mu\text{m}^2$.

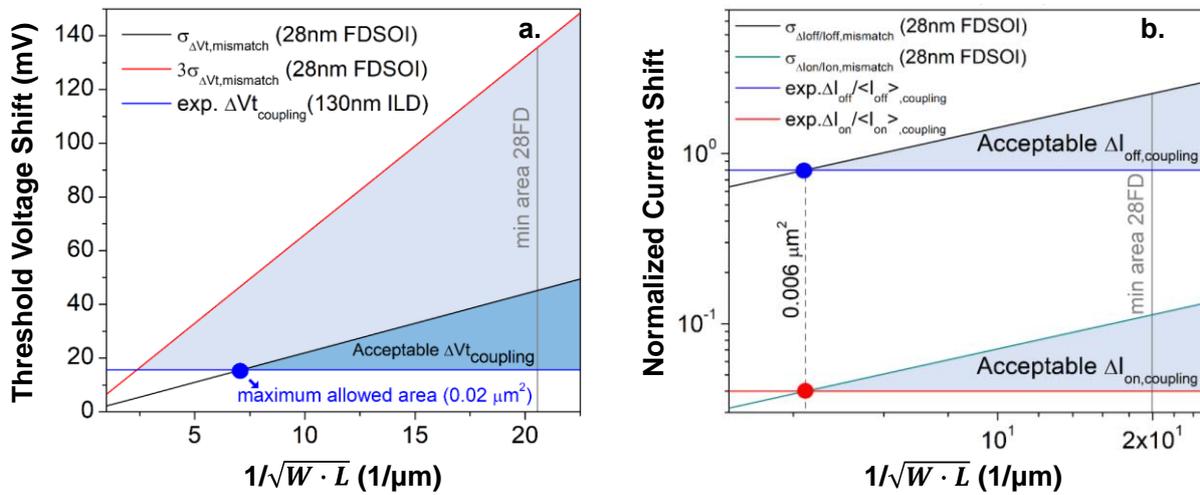


Fig. 3.35 (a) Coupling-induced shift and mismatch-related variations (28nm FDSOI versus reciprocal of gate area square root) for a) threshold voltage and (b) I_{off} and I_{on} current shift. The vertical marker in figure (a) indicates the mismatch standard deviation for the minimal transistor surface in 28 nm FDSOI ($W = 80\text{nm}$, $L = 30\text{nm}$).

Indeed, digital designs utilize the minimum gate length of each technology node, while the gate width varies from the minimum allowed value of the design rules up to a typical value limited by the power supply rails distance. The latter is demonstrated schematically in Fig. 3.36, considering that in digital design the design follows a common pattern –the power supply rails, GND and V_{DD} , extend throughout the whole design and between them the devices are placed, with NMOS devices always

at the upper region of the design next to the GND rail, as opposed to PMOS devices next to V_{DD} rail. Therefore, for 28nm FDSOI technology, the gate width has a typical maximum of 320nm, while the minimum allowed gate length and width are 30nm and 80nm respectively.

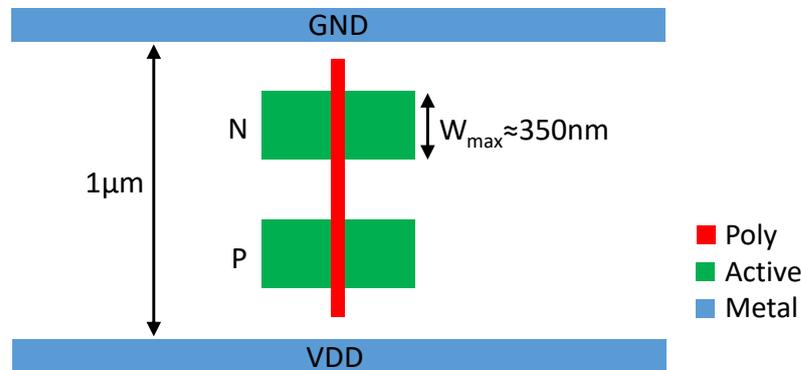


Fig. 3.36 Schematic top layout view of a digital standard cell in 28nm FDSOI technology. The distance limitations between the power supply rails (V_{DD} and GND) restrict the gate area of the devices below $0.01 \mu\text{m}^2$.

The relative weight of variability on the normalized off-currents (green curve) and on-currents (black curve) is demonstrated in Fig. 3.35 (b). Due to the exponential behavior of current in the subthreshold region, the weight is much larger for off-currents than for on-currents. Despite the fact that both on- and off-current seem to be more sensitive to electrostatic coupling the shifts ΔI_{off} and ΔI_{on} , are within the calculated normalized mismatch variations of I_{off} and I_{on} in 28 nm FDSOI technology, for a typical range of gate areas in digital design, even for the 1- σ consideration.

3.2.3.b Analog devices at the bottom tier ($V_{DD}=2.5V$)

Devices used in analog design typically possess a thick EOT and thus have a higher power supply. For 28nm node devices with EOT in 5nm range, their power supply is $V_{DD}=2.5V$. Therefore, if they are placed at the bottom tier underneath top digital devices, the maximum level of bias at the bottom device gate electrode can be 2.5V. Fig. 3.37 shows the Threshold Voltage shift due to coupling versus the ILD thickness extracted by TCAD simulations, for the two cases of bottom tier devices. The experimentally extracted values for both cases are denoted with the open symbols while an exponential decrease as a function of the ILD thickness is evident.

Furthermore, the dashed blue line shows the most critical case of the threshold voltage local variability in the 28 nm FDSOI process, which is the 1-sigma limit for the minimum gate area. From the study presented in the previous section, the threshold voltage shift for 130nm thick ILD is well within

the local variability limit and can define a safe coupling-to-mismatch margin for the 3DSI of other applications. Hence, as observed, the values of the Digital1V on Analog2.5V case are higher than the Digital1V on Digital1V case, so in order to maintain the same coupling-to-mismatch margin, the ILD thickness must be greater than 350nm.

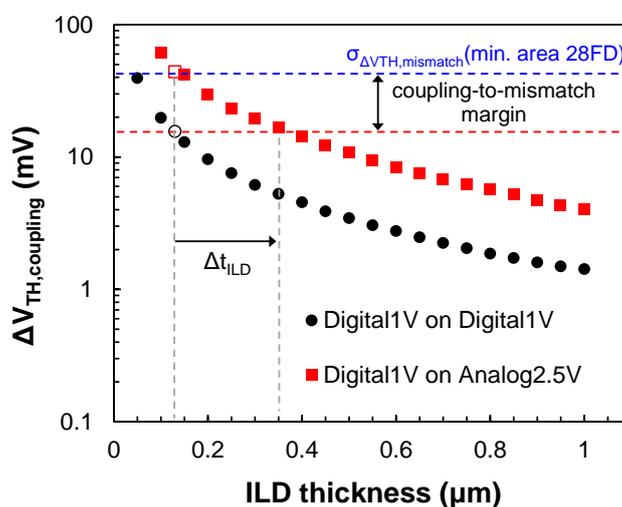


Fig. 3.37 Threshold voltage shift due to static coupling for 2 different stacks of devices. To preserve the same coupling-to-noise margin for Analog bottom-tier devices a thicker ILD ($\geq 350\text{nm}$) is needed.

3.2.4 Impact of static coupling on the performance of top-tier analog devices ($V_{DD}=2.5\text{V}$)

Devices with power supply of 1V are intended for low power/low voltage digital applications, however they are not preferred for analog design because of their limited voltage swing. Furthermore, the use of a thicker silicon body enables a higher g_m/I_d ratio, enhancing the performance of analog circuits. To date, LT devices have been successfully processed for Low-Voltage (LV) [19] as well as High-Voltage (HV) [102] applications. The latter suggests a process scheme for FDSOI devices with 30nm thick undoped channel, 25nm BOX, and $\text{SiO}_2 = 6\text{nm}/\text{TiN}/\text{Poly-Si}$ gate stack (Fig. 3.38).

Moreover, the in-depth characterization of analog HV devices with thick EOT has been investigated in the same work revealing a performance comparable to high temperature reference s and passing the PBTI reliability criteria. The coupling induced threshold voltage shift when top device is an analog one for the two cases where the bottom device is either digital or analog, was examined with the aid of TCAD simulations.

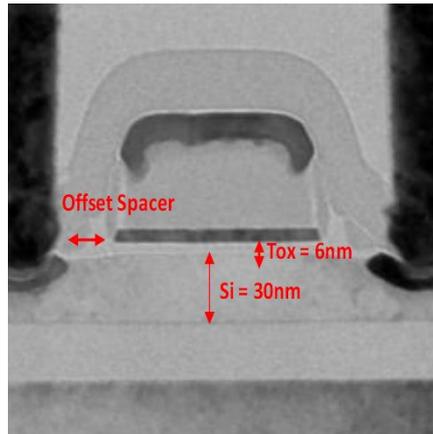


Fig. 3.38 TEM cross-section of the fabricated analog SOI architecture using LT processing [102].

For analog devices being at the top tier, their coupling behavior to the bottom devices deviates from the one studied for digital devices so far, due to their thicker EOT as well as silicon body. Indeed as Fig. 3.39 shows, the coupling induced ΔV_{TH} is shifted to significantly higher values. Taking into account that analog circuits are extremely sensitive to threshold voltage variations, solutions to mitigate the coupling effects must be incorporated (the reader is encouraged to refer to § 4.2).

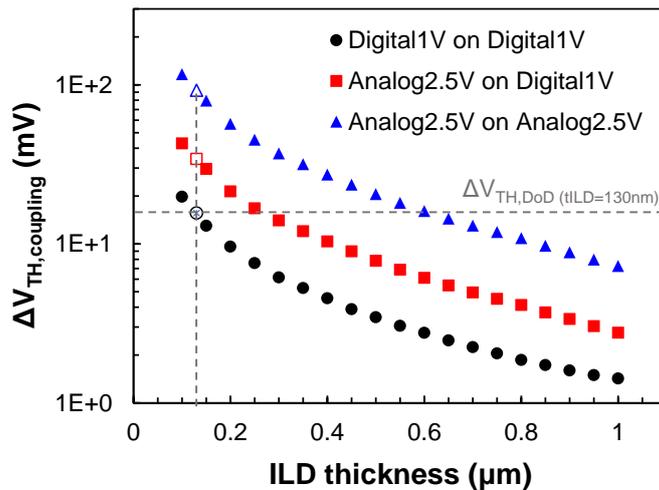


Fig. 3.39 Threshold voltage shift due to static coupling for 2 different stacks of devices with analog on top. The black markers recall the results obtained for digital device stacking.

Indeed, analog circuits such as current mirrors and differential amplifiers, require pairs of transistors, which are identically designed and laid out in an identical environment, in order to ensure the same electrical performances. As explained in the previous section, real devices suffer from random local variations in the electrical parameters (mismatch), and from Fig. 3.35 (a) it can be observed that these variations decrease as the gate area of the device increases. Adding to that also the fact that analog designs often tend to utilize transistors of a large gate area, it is apparent that the

coupling-induced threshold voltage shift has a stronger impact compared to mismatch, that cannot be tolerable.

Although the obvious solution is the thickening of ILD, this is actually not practical as it will worsen the 3D contact AR dramatically. From a circuit design perspective, the coupling-induced threshold voltage shift can be alternatively viewed as a DC offset for the victim top-tier device, which can be corrected with offset cancellation techniques [103]. Yet, this is not valid in the cases that the offset is random and cannot be predicted, e.g., the bit storage value of a SRAM cell.

3.3 Impact of AC coupling on top/bottom device performance

The electromagnetic interference between active devices in different tiers is a serious concern in mixed-signal circuits and especially in 3DSI that offers a platform for the heterogeneous integration of applications. Nowadays, digital applications that have been the primary driving force of 3DSI, feature high speed switching signals with a rising/falling edge of several picoseconds. The rise/fall time of a switching clock signal is defined as the time required for the signal to go commonly from 10% to 90% of the LOW to HIGH level difference. This transition time is limited by the gate delay of transistors and the propagation delay of the interconnections. The gate delay expresses the time delay in the path of a signal, from the digital gate's input to the output, and is depended on the ON-state resistance of the transistors and their capacitive loads. It can be divided in a low-to-high ($t_{p,LH}$) and high-to-low ($t_{p,HL}$) propagation delay as shown in Fig. 3.40.

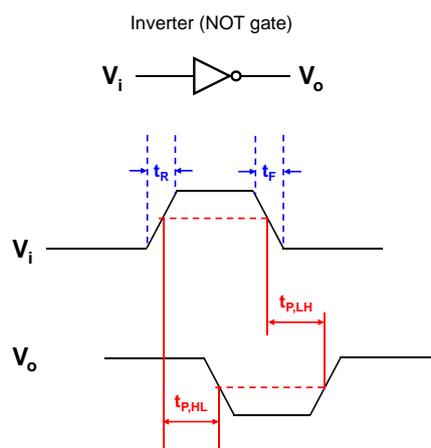


Fig. 3.40 Rise/fall time of a pulse shaped signal and propagation delay of a NOT gate.

On the other hand the propagation delay of interconnects depends on their resistivity and length. Hence, global interconnects that are used to connect systems within a chip, have a length in

the millimeter range, introducing a high propagation delay in the transmitted signals, contrary to local interconnects that are used to connect adjacent devices and their delay is even lower than the gate delay [85]. This implies that the limitation for the rise time of the switching clock signals emanates from the gate delay. Fig. 3.41 shows the typical delay for global and local Cu interconnects compared to the nominal gate delay in each technology node [85].

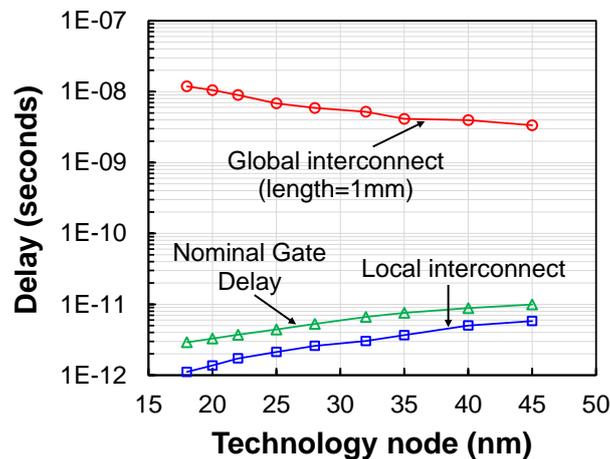


Fig. 3.41 Typical delay for global and local Cu interconnects compared to the nominal gate delay in each technology node [85].

As observed from Fig. 3.41, for a 28nm node the rise/fall time of clock signals can be as low as 8ps. The significant frequency of a digital signal, i.e., the highest frequency up to which the amplitude of the corresponding frequency components is significant, is much higher than the frequency of the clock in a digital system. Consequently, the significant frequency for 28nm node clock signals can be as high as 32GHz, as estimated by (2-46).

Furthermore, the concept of a hybrid integration of RF and logic functions on adjacent tiers, presents an emerging interest to the electronics community nowadays [104], [105]. Nevertheless, these applications can be an intense source of RF crosstalk for noise-sensitive analog applications placed among the adjacent tiers.

3.3.1 Small-signal analysis

Before proceeding to the analysis, it is crucial to choose the simulation tool in order to carry out the dynamic coupling analysis. It is true that in order to have an accurate calculation of the electromagnetic coupling between different components, a full-wave approach, i.e. solving the complete set of Maxwell equations without any simplifying assumptions, is necessary. However, since the electrical size of the coupled structures in 3DSI is much smaller than the wavelength in the frequency range under study (<300GHz the upper limit of the mmW band), the analysis can be carried

out using quasi-static approximation of Maxwell equations. Under this assumption, the electric and magnetic fields produced by an aggressor signal are not interacting with each other, hence capacitive and inductive coupling can be analyzed separately.

Over and above that, semiconductor-based problems require incorporating the associated physics such as drift, diffusion and generation-recombination, within the solving procedure. TCAD semiconductor device software such as Silvaco ATLAS appears to be the appropriate tool for this type of problem under the previous assumptions. However, TCAD AC simulations calculate the conductance and capacitance between each pair of electrodes, thus focusing on the electric field (capacitive) coupling and neglecting the one occurring from the magnetic field (inductive).

It has been stated in [63] that in monolithic 3D-ICs, capacitive coupling dominates the inter-tier coupling, as opposed to the inductive coupling being negligible due to the small geometries of the interference source. However, in the particular layout configuration studied in this chapter (Fig. 3.7), the inductive coupling between the drain terminals of each top/bottom device may be significant.

3.3.1.a Impact of inductive coupling

To assess the strength of the inductive coupling in the structures under study, the methodology used in [44] has been followed. In this work, by artificially modifying the permeability of all materials to be 0.01 times the vacuum permeability, the authors estimated the strength of the inductive coupling by extracting the relative error of the g_{21} parameter by considering a two-port network configuration. While the S_{21} scattering parameter (Fig. 3.42) which describes the power transferred from one tier to the other, has been widely used for electromagnetic coupling studies in

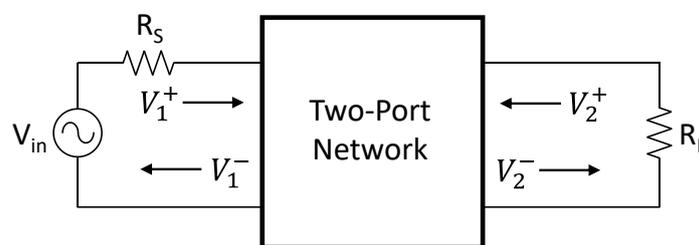


Fig. 3.42 Equivalent circuit of a two-port network in terms of s -parameters.

mixed-signal 3D circuits, other network parameters such as g_{21} which represents the forward voltage

gain ($g_{21} = \frac{V_2}{V_1} \Big|_{I_2=0}$) can be used for this study interchangeably.

ANSYS High Frequency Structure Simulator is a pure electromagnetic simulator that can be used to analyze these effects. The structure under test, shown in Fig. 3.43 (a), is the same as the one studied in the static coupling analysis, and the permittivity, permeability and bulk conductivity of the materials have been calibrated accordingly from TCAD simulations. Specifically, the highly doped semiconductor regions are treated as conductors with a bulk conductivity of 1.14×10^5 S/m, accounting for n-type doping of 10^{20} cm⁻³. The channel region is considered for both devices to be in the on-state, in order to allow for a conductive path between the drain-source electrodes. The gate length and width, noted in Fig. 3.43 (a), where varied to observe the impact of geometry on the coupling behavior.

Considering the two-port configuration of Fig. 3.43 (b), ports 1 and 2 are assigned to the drain electrodes of the bottom and top device respectively. The source and gate electrodes of both devices have been assigned to the common reference node. Under small-signal analysis, when $V_{GS} > V_{TH}$ in linear region of operation ($V_{DS} < V_{GS} - V_{TH}$), the MOSFET is considered as a resistor. On the contrary, in saturation ($V_{GS} > V_{TH}$ and $V_{DS} > V_{GS} - V_{TH}$), the transistor behaves as a current source with $i_{ds} = g_m \cdot v_{gs}$, where g_m is the transconductance of the device and v_{gs} is a small voltage signal applied at the gate of the device. In this case, the output resistance of the transistor becomes considerably large.

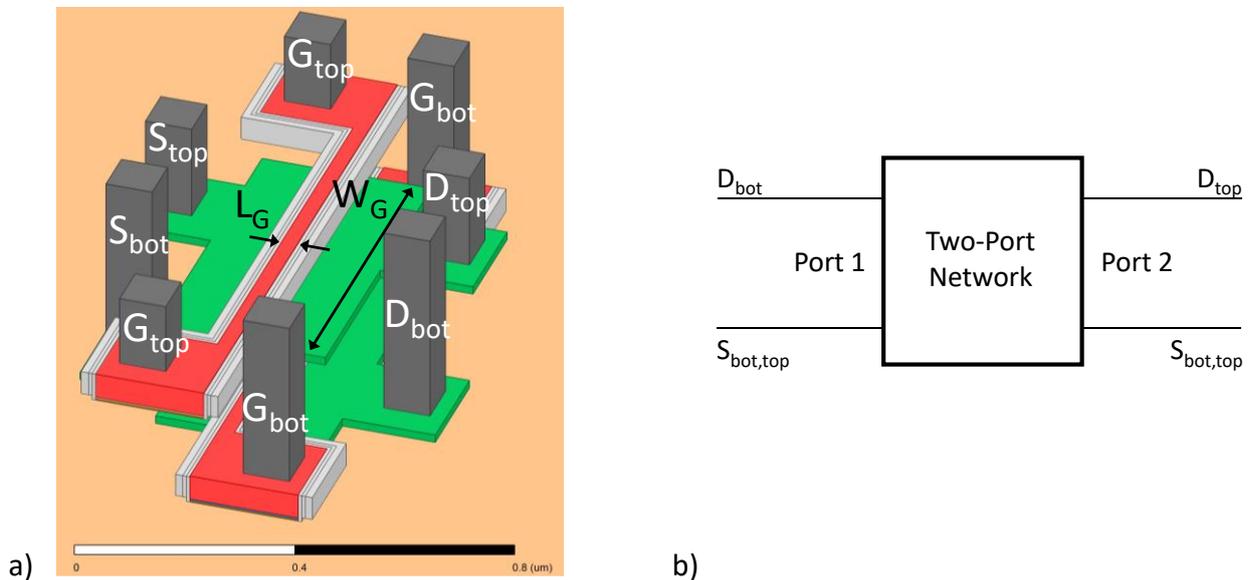


Fig. 3.43 Simulated structure in HFSS (a) and port configuration for the network parameter extraction (b).

Therefore, the lowest value of the resistance from drain to the common source node occurs in the linear region of operation for $V_{GS} = V_{DD}$. The resistance value in this biasing state was obtained with the aid of a TCAD small signal simulation, and was used to calibrate the resistance seen by the D_top electrode to the reference electrodes S_top, S_bot in HFSS.

Extracting the g_{21} parameter of the two-port network, the results are shown in Fig. 3.44, for a device with $W=0.5\mu\text{m}$ and $L=30\text{nm}$. The data labeled as "no inductive" have been extracted by setting the permeability of all materials to be 0.01 times the vacuum permeability, thus excluding the inductive coupling mechanism from the power transmission. The difference between the two is negligible (less than 0.01%) and gets even smaller for a larger gate length (Fig. 3.45 (a)) On the other hand, varying the gate width the relative shift of g_{21} increases, indicating that magnetic fields become stronger (Fig. 3.45 (b)).

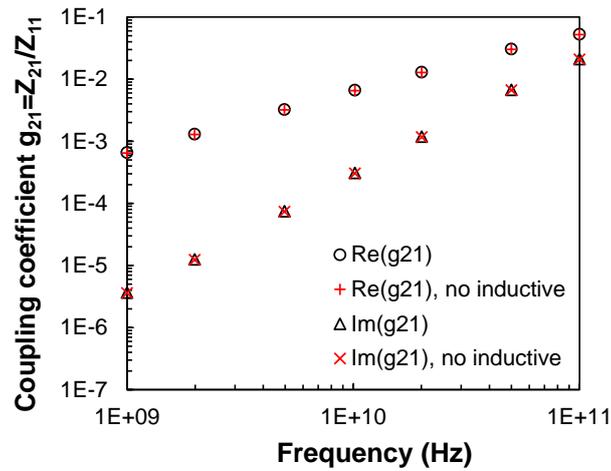


Fig. 3.44 Extracted g_{21} parameter from HFSS simulation for a device with $L_G=30\text{nm}$ and $W_G=0.5\mu\text{m}$. The g_{21} parameter indicates the noise voltage at the top device drain terminal divided by the bottom device drain terminal.

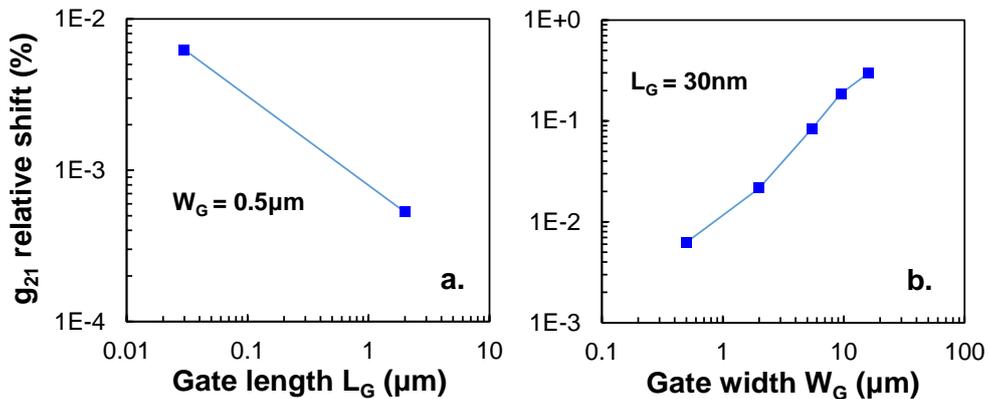


Fig. 3.45 Variation of the g_{21} parameter with the gate length (a) and width (b) of both devices.

From the above analysis it is evident that capacitive coupling is the dominant mechanism of power transmission between active devices. Yet, layout-aware techniques must be followed to limit magnetic fields in the direct stacking of short and wide active devices with current flowing in loop paths. Hence, to pursue the dynamic coupling analysis, the inductive coupling will be neglected henceforth.

3.3.1.b Impact of capacitive coupling

TCAD simulations were used to obtain the crosstalk S_{21} (dB) parameter values by considering each electrode of the bottom/top device as an aggressor (port 1) to the other one (port 2). For the sake of conciseness, the crosstalk levels of top devices will be presented here as they are the same for the opposite case due to the reciprocity of the network. Moreover, for top devices there is the additional back-gate effect from the bottom device electrodes, making them more susceptible to noise coupling, prominently in the saturation region.

Fig. 3.46 shows the crosstalk level in the frequency range from 1MHz to 100GHz, for both devices having equal gate length and width of $1\mu\text{m}$, whereas the top device is in cutoff (Fig. 3.46 (a)) and in saturation region of operation (Fig. 3.46 (b)).

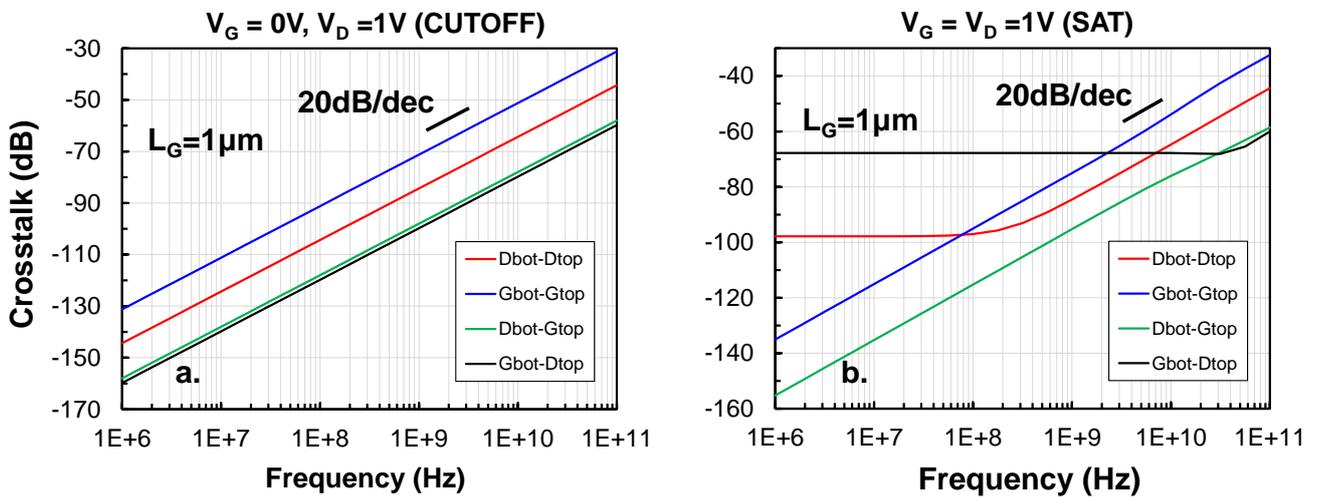


Fig. 3.46 Crosstalk levels for the top-tier device electrodes of $L_G=1\mu\text{m}$, in cutoff (a) and saturation region (b), extracted by the S -parameter technique. A small-signal noise voltage is applied in each electrode of the bottom device.

In cutoff mode, for all victim-aggressor electrode pairs, there is an increase of the crosstalk level by 20dB/dec, attributed to the capacitive network between them. In detail, the top device gate electrode is the most susceptible to crosstalk from the bottom device gate electrode as they have a parallel plate capacitance that is essentially the C_{ILD} which dominates in the series combination with C_{ox} , C_{si} as it is weaker than the other two. Regarding the crosstalk between the drain electrodes of the top and bottom device, it is $\sim 12\text{dB}$ lower than the previous one and is attributed to the summation of the parallel plate capacitance from the diffusion area of the two electrodes with the capacitance between the 3D contacts. The crosstalk levels for the two other electrode pairs are weak, associated with fringing field capacitances between them.

In saturation region for the top device, there is a plateau of the crosstalk level at low frequencies between the bottom device aggressor electrodes G_{bot} , D_{bot} to the top device drain electrode, due to the BG effect. Indeed, G_{bot} (similarly D_{bot}) acts as a back-gate of the top-tier device, thus it injects a small-signal current $i_{D_{top}} = g_{m,G_{bot}} \cdot V_{G_{bot}}$, where $g_{m,G_{bot}}$ is the back-gate transconductance of the top-tier device due to G_{bot} given by

$$g_{m,G_{bot}} = \frac{dI_D}{dV_{G_{bot}}} \quad (3-4)$$

Moreover, the gate of the top device G_{top} is partially screened by the inversion channel within the top device silicon film, so the crosstalk level is reduced by ~ 5 dB. The most critical pair of nodes in this region of operation is thus G_{bot} - D_{top} .

Shrinking the gate length of the top/bottom device to 30nm, nominal L_G in 28nm FDSOI technology, the simulation was repeated and the crosstalk level for each victim-aggressor electrode pair was obtained as shown in Fig. 3.47. Now, the crosstalk level of the G_{bot} - G_{top} electrodes decreases while the one of the D_{bot} - D_{top} electrodes remains the same (Fig. 3.47 (a)).

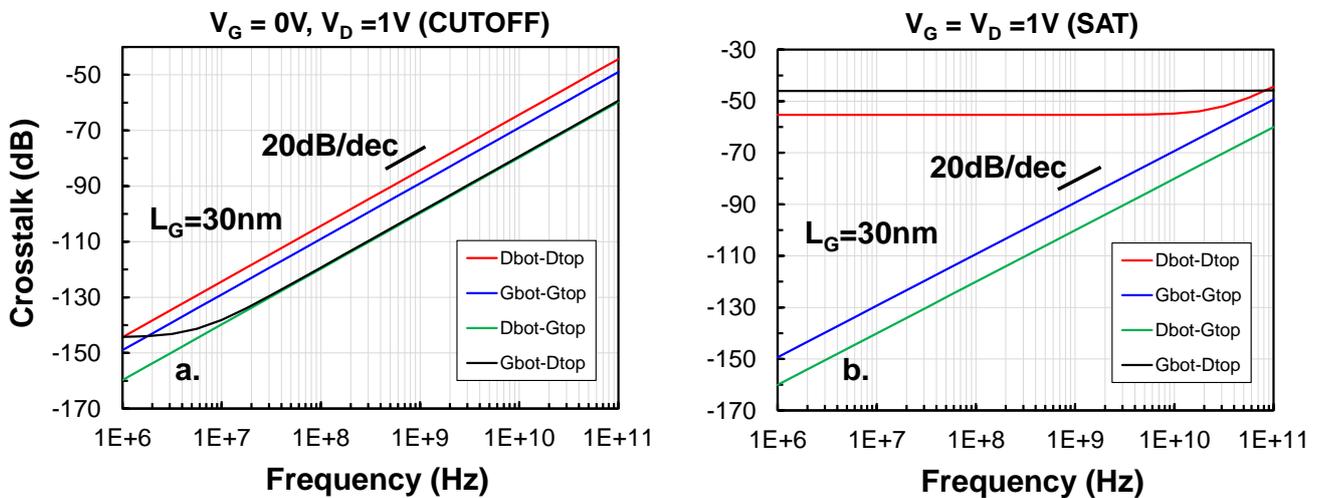


Fig. 3.47 Crosstalk levels for the top-tier device electrodes of $L_G=30$ nm, in cutoff (a) and saturation region (b), extracted by the S-parameter technique. A small-signal noise voltage is applied in each electrode of the bottom device.

Entering the saturation region of operation (Fig. 3.47 (b)), the top device drain electrode becomes sensitive to the G_{bot} , D_{bot} electrodes due to the BG effect, as explained before. In that case, the crosstalk between the gate of the bottom device and the drain of the top device is the most significant with a high plateau level of -46dB in the frequency range studied.

3.3.2 Transient response of top-tier devices to bottom-tier device aggressor signals

As identified in the previous section, the most critical capacitive coupling for two stacked active devices in 3DSI occurs between the drain of the top device and the gate/drain of the bottom. Considering a CMOS digital circuit, the bottom device gate bias can switch from 0 to V_{DD} , driven by a clock signal. This pulse-shaped switching of the bottom transistor gate bias, can lead to an important dynamic coupling to the top transistor channel. In order to experimentally determine the importance of this effect, high-speed drain current sampling measurements for a top-tier device were performed using the fast IV module (down to 10ns time resolution) of the Agilent B1530A device parameter analyzer, with the application of a pulse bias from 0 to 1V at the bottom device gate electrode (setup shown in Fig. 3.48).

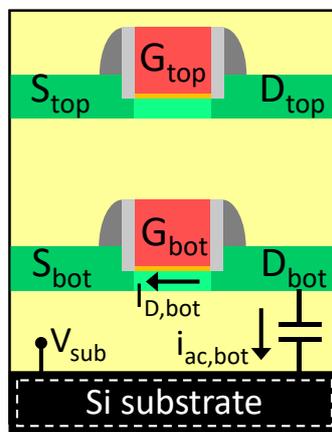


Fig. 3.48 Setup for bottom-tier SOI dynamic coupling characterization.

A bottom instead of a top tier device was chosen, because it has a BOX capacitance almost 5 times higher than the ILD, allowing us to capture more accurately the capacitance-related effects. As shown in Fig. 3.49 (a), it is evident that a parasitic spike occurs in the drain current at the beginning of the back-gate voltage pulse. This spike corresponds to the charging current of the drain-substrate capacitance ($C_{d,bg}$) and the peak amplitude, i_{ac} , is given by Ohm's law for capacitors. In order to further shrink the rise time of the applied bias, the experimental setup was repeated in TCAD. It can be seen from Fig. 3.49 (b) that as the rise time of the switching event at the BG gets shorter, i_{ac} is increased, making the dynamic more critical than the DC coupling.

Fig. 3.50 shows the amplitude of the parasitic spike due to the dynamic coupling versus the rise time of the applied pulse at the BG, both in log scale, the circles indicate the experimental results while the dashed line refers to the TCAD simulation results. The agreement between the two is apparent and also the extrapolation to shorter rise times reveals the Ohms law dependence of this

effect. As the accuracy of the TCAD simulation has been confirmed, the analysis was extended for the top devices.

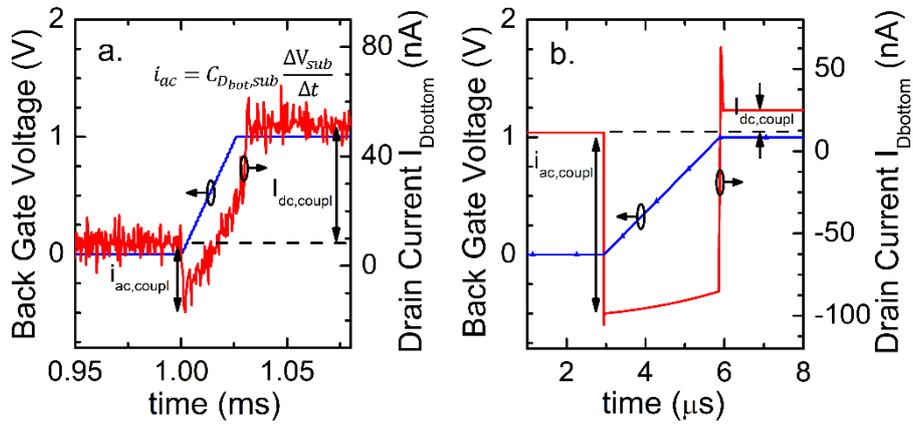


Fig. 3.49 Dynamic coupling transient results for a bottom tier SOI ($W_G=30\mu\text{m}$, $L_G=0.5\mu\text{m}$) at $V_G=0.1\text{V}$. (a) Experimental transient for $t_r=30\mu\text{s}$ with the applied pulse at the BG of the device (blue) and the measured drain current (red) revealing the parasitic spike $i_{ac,coupl}$. (b) TCAD simulation for a shorter rise time ($t_r=3\mu\text{s}$) shows that the $i_{ac,coupl}$ becomes greater than the coupling-induced DC shift ($I_{dc,coupl}$).

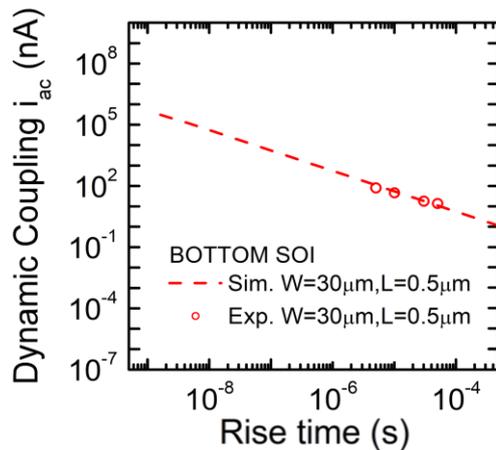


Fig. 3.50 Peak amplitude of $i_{ac,coupl}$ vs rise time of the applied pulse at the BG of the bottom SOI for Fig. 3.48 case. TCAD simulations are in-line with experimental results.

In order to assess the top device response to the dynamic coupling effect, the architecture of Fig. 3.51 was simulated applying the same bias conditions as previously. The effect appears to be the same with the bottom tier devices, however in this case the capacitance of interest is due to the fringing fields between the top device drain and the bottom device gate electrode.

3.3.2.a Impact of top device biasing

The impact of the top device operating region on the dynamic coupling effect between the bottom device gate electrode and the top device channel, was assessed via TCAD simulations. The top/bottom devices were selected to have equal gate length $L_G=30\text{nm}$ and width $W_G=1\mu\text{m}$. A periodical trapezoidal signal was applied at the bottom device gate electrode, emulating a clock signal

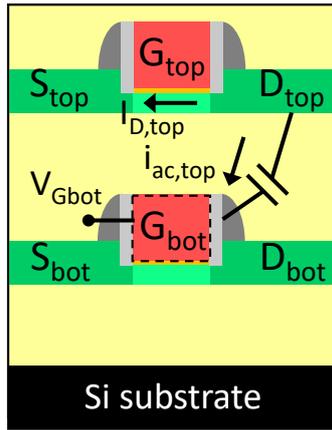


Fig. 3.51 Setup for top-tier SOI dynamic coupling characterization.

with a swing voltage of $V_{swing}=1V$, a frequency of $f_{clk}=5GHz$, a rise/fall time of 8ps, and a pulsewidth of 92ps as shown in Fig. 3.52 (a). The transient response of the top device drain current to the applied clock signal was then obtained for the top device under biasing in the 3 regions of operation, cutoff in Fig. 3.52 (b), linear in Fig. 3.52 (c) and saturation in Fig. 3.52 (d).

In cutoff region, since the drain current of the device is very small (3pA) due to the sub-threshold conduction, the dynamic coupling parasitic spikes have a high amplitude (1 μ A) due to the very short rise/fall time of the applied clock signal at the bottom device gate electrode.

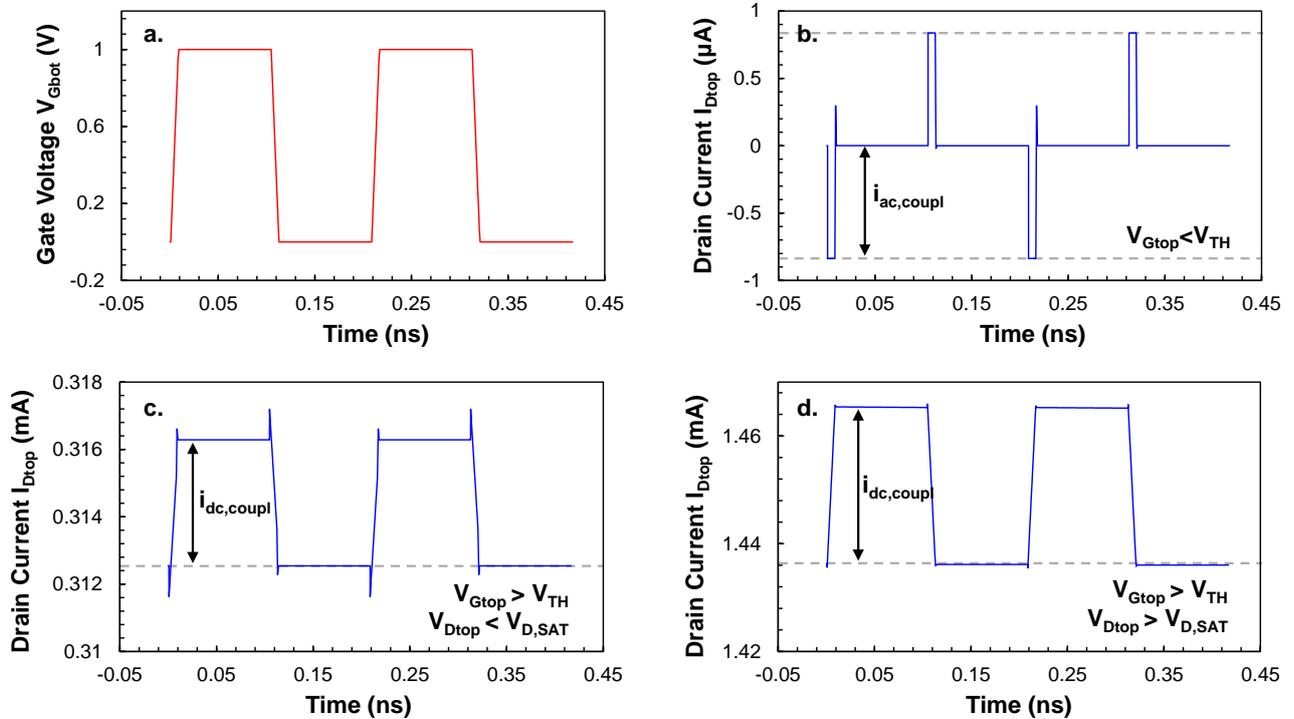


Fig. 3.52 Transient response of the top-tier device drain current to the applied clock signal ($V_{swing}=1V$, $f_{clk}=5GHz$, $t_R/t_F=8ps$, $t_{pulse}=92ps$) at the bottom device gate electrode (a), for 3 different regions of operation, cutoff (b), linear (c) and saturation (d).

Biasing the device in the linear region (Fig. 3.52 (c)), due to the high ON-state current of the device, the threshold voltage modulation by the static capacitive coupling induces a pulse of the same frequency as the clock signal and magnitude of $I_{dc,coupl}$. Entering the saturation region (Fig. 3.52 (d)), the parasitic spike induced by the dynamic capacitive coupling vanishes, and the threshold voltage modulation dominates.

3.3.2.b Impact of device geometries and position

To investigate the impact of the geometrical parameters the width W_{Gtop} and the length L_{Gtop} of the top top-tier devices were varied. As shown in Fig. 3.53, there is an evident increase of i_{ac} with W_{Gtop} , while there is no dependence on L_{Gtop} . This increase of the dynamic coupling only with the gate width indicates that the dominating capacitance in this effect is the one between the gate of the bottom and the drain of the top device.

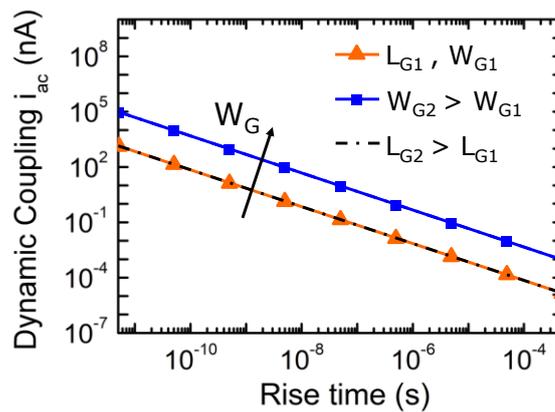


Fig. 3.53 Peak amplitude of $i_{ac,coupl}$ vs rise time of the applied pulse at the BG of the bottom SOI for Fig. 3.51 case.

To assess the impact of the relative positioning on the dynamic coupling effect, the setup of Fig. 3.54 was simulated in TCAD, with the top device position shifted in the gate length direction, so that its drain electrode gradually overlaps with the bottom gate.

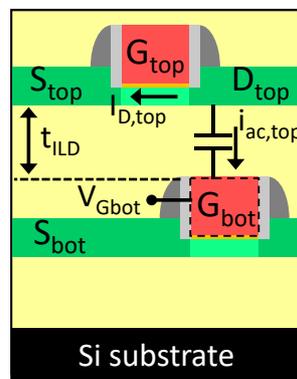


Fig. 3.54 Setup for top-tier SOI dynamic coupling characterization under the worst case scenario (max. $C_{Dtop,Gbot}$).

Extracting the amplitude of the parasitic spike due to the dynamic coupling versus the misalignment between the two devices, it was found to be maximized (Fig. 3.55 (a)). Consequently, the maximum value of the $C_{D_{top},G_{bot}}$ capacitance can be given by the classic parallel plate capacitor expression and it can be reduced either by increasing the ILD thickness or decreasing the gate width as well as the drain region length. The latter is a process parameter determined by the Contacted Poly Pitch (CPP) (Fig. 3.55 (b)) which is further reduced with the scaling of the technology.

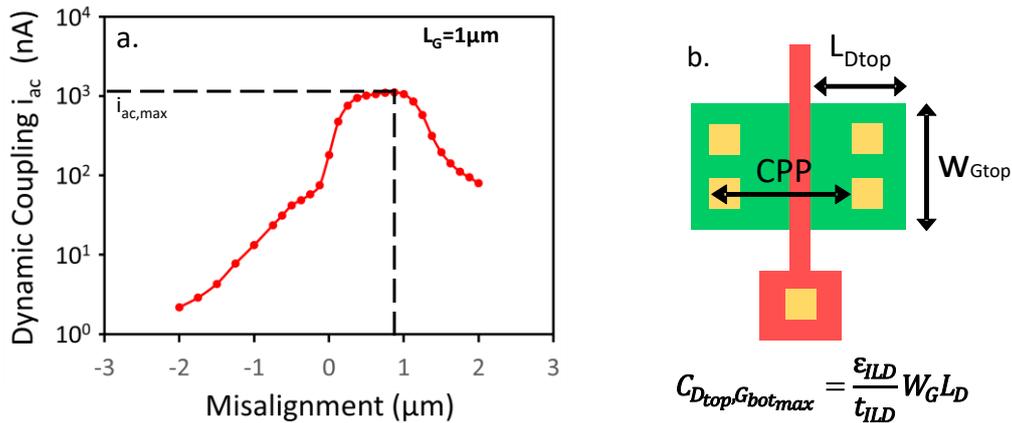


Fig. 3.55 (a) Peak amplitude of $i_{ac,coupl}$ vs relative misalignment between the gates of the devices. (b) top-tier SOI layout view.

3.3.3 Inter-tier versus intra-tier coupling

Crosstalk between active devices is a common issue in every technology and is always better if it can be minimized. In conventional planar integration, the substrate crosstalk is the primary cause of interference in mixed-signal circuits. SOI planar technology is known to provide lower substrate crosstalk than the bulk CMOS process [106], because of the BOX presence and the use of resistive ($>1\text{k}\Omega\text{-cm}$) [107] or highly-resistive substrate ($>1\text{k}\Omega\text{-cm}$) [108]. In addition, the GP underneath the SOI devices added nowadays, effectively shields them from substrate crosstalk [109]. With that, mixed-signal interference is limited to the horizontal direction (intra-circuit) coupling through the dielectric medium, an issue that can be solved by proper layout placement of the devices and isolation techniques [108], [110], [111].

In 3DSI, a device placed at one tier can suffer both from horizontal coupling from adjacent devices within the same tier (intra-tier) as well as coupling from the stacked devices (inter-tier), which has been analyzed so far. In order to estimate the relative strength of the two, the simulation setup of Fig. 3.56 was performed in HFSS. Fig. 3.56 (a) examines the inter-tier crosstalk employing two stacked devices that consist a two-port network where the drain of the bottom device D_{bot} is selected as port 1 and the drain of the top D_{top} as port 2, whereas the rest of the electrodes are set to the

common ground.

On the other hand, the setup of Fig. 3.56 (b) features a critical case of adjacent devices in planar SOI technology. It consists of two devices placed at the same tier (intra-tier), mirrored to each other and separated by the minimum distance dictated by the technology. This time, the drain of the left device is assigned to port 1 while the drain of the right device is set to port 2 and all the other electrodes are set to common ground.

The devices simulated in both cases have equal gate length $L_G=30\text{nm}$ and widths $W_G=620\text{nm}$, while the density of the contacts in the first case is reduced due to the direct stacking of the devices. The medium that surrounds the devices is SiO_2 . Metal lines at the BEOL layer above the devices have been excluded in order to restrict the analysis at the active device level.

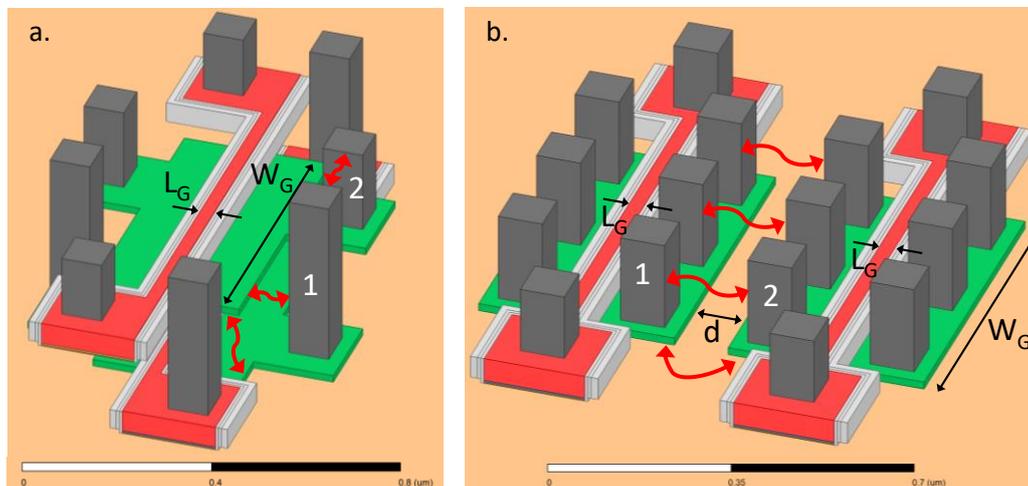


Fig. 3.56 Simulation setup in HFSS to estimate the relative difference between inter-tier (a) and intra-tier coupling.

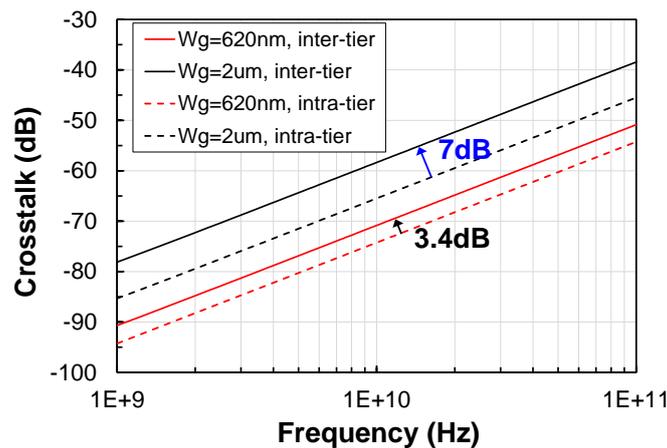


Fig. 3.57 Crosstalk levels for the victim device drain electrodes of a device with $W_G=620\text{nm}$ (red) in the case of inter-tier coupling (continuous line) and intra-tier coupling (dashed line). Increasing the width of the two devices in each case to $W_G=2\mu\text{m}$ (black), the crosstalk difference gets increased

The simulation results of the S_{21} parameter that illustrate the crosstalk for each case are given in Fig. 3.57. For $W_G=620\text{nm}$, the inter-tier crosstalk is 3.4dB greater than the intra-tier, as the former

is enhanced by the vertical coupling from the diffusion area plus the horizontal coupling from the 3D contact. On the contrary, the intra-tier crosstalk is associated mostly with the horizontal coupling of the contacts rather than the weak fringing capacitances of the diffusion areas. Furthermore, increasing the width of the two devices in each case to $W_G=2\mu\text{m}$, the crosstalk difference is even more amplified. From this comparison it is sensible that in order to obtain comparable inter-tier crosstalk values with the intra-tier ones, decoupling techniques are needed and are investigated in §4.2.

3.4 Conclusion

In this chapter the vertical electrical coupling between devices placed in two different tiers of a 3D sequential structure has been characterized experimentally and further analyzed with the aid of TCAD simulations. This interference has been demonstrated to cause noise coupling among the two devices and unwanted threshold voltage variations for stacked devices.

All the geometry and biasing related dependencies of these effects have been explored and it has become evident that the static coupling effects are reduced when the two devices are misaligned, as opposed to the dynamic coupling effects. Moreover, regarding noise coupling (crosstalk) it is evident that it is of higher levels for stacked devices with a high W/L ratio, due to the back-gate coupling effect.

Furthermore, a study of the coupling-induced effects in the static and noise behavior of 3D sequential top tier transistors has been presented. Through both measurements and TCAD simulations, it was shown that the coupling-induced ΔV_{TH} , ΔI_{off} and ΔI_{on} have high values considering analog applications, however they are well within the local variability limits of 28 nm FDSOI technology for digital circuits, where sub- μm devices are used. Using these values as a metric for the 3DSI of other applications we have concluded that for digital applications stacked on top of analog applications, the ILD thickness has to be greater than 350nm. Concerning the low-frequency noise performance of the top tier transistor, no coupling-induced impact was observed regardless the transistor area.

CHAPTER 4

COUPLING EFFECTS IN 3DSI CIRCUITS: IMPACT ON OPERATION AND PROPOSED SOLUTIONS

This chapter analyzes the effect of inter-tier capacitive coupling on monolithic 3D circuits. The most critical combinations of tier stacking with heterogeneous integration are investigated in order to conclude on the critical dimensioning of the structures and the necessity of inter-tier isolation. More specifically, the digital tier stacking which has been studied at device level in chapter 3, is further analyzed with the aid of a 2-bitcell Sequential 3D SRAM under the influence of both static and dynamic coupling. Additionally, the sensitive case of a Mixed-Signal/RF circuit like the Ring Oscillator (RO) is examined on top of either a digital or an analog application tier at the bottom with a power supply of 1V and 2.5V respectively. Lastly, for the stacking of sensitive applications where the inter-tier coupling cannot be tolerated, decoupling methods and techniques are explored targeting an efficient process flow compatible with 3DSI.

4.1 Impact of inter-tier coupling on circuit operation

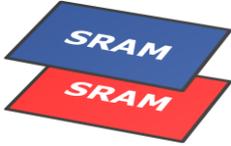
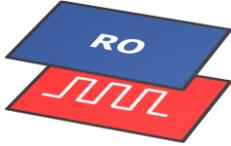
3DSI offers the flexibility of placing circuits on different tiers to achieve high performance and ultimate integration density. However, this is at cost of the undesirable vertical coupling through the ILD having a thickness of several hundreds of nanometers. In Chapter 3, the coupling effects have been deeply examined at device level, resulting in several significant conclusions that can enable to pursue the analysis at circuit level. A brief recapitulation is as follows:

- In monolithic 3D-ICs, capacitive coupling induced by the electric field dominates the inter-tier coupling whereas the inductive one is negligible because of the small geometries of active devices having rectangular shapes in conjunction with the low current densities that result in weak magnetic fields.
- The inter-tier capacitive coupling can cause signal transmission among the devices placed in different tiers and unwanted threshold voltage variation for stacked devices.
- In particular, the coupling induced threshold voltage shift of stacked devices, is identified as the strongest interference as it can potentially increase leakage current/power and decrease the ON-current.
- At a device level, it was proved that for digital device stacking the inter-tier static coupling is negligible compared to the mismatch variations in 28nm FDSOI technology. Thereby, the presence of the inter-tier coupling is not widening much the process corners in digital design and thus can be considered as tolerable.
- Additionally, digital devices stacked on top of analog devices having $V_{DD}=2.5V$, must employ a thicker ILD (around 350nm) to result in the same level of coupling-induced ΔV_{TH} as digital on digital devices. This thickness of the ILD is tolerable for the 3D contact processing.
- Finally, analog devices stacked on top of either digital or analog devices have been characterized as critical cases of inter-tier coupling as their coupling-induced ΔV_{TH} is shifted to higher values due to their thicker silicon body (higher g_m/I_d ratio) and oxide (larger voltage swing), compared to top-tier digital devices. Adding to that also the fact that analog circuits are commonly more sensitive to noise and particularly to V_{TH} variations, it is preferable to place analog circuits at the bottom tier of a 3DSI process scheme, or to utilize inter-tier isolation methods to decouple effectively their body potential.

With the above being mentioned, the inter-tier coupling analysis (both static and dynamic) has to be further extended at a circuit level, in order to draw conclusions regarding the necessity of electrical isolation for the remaining cases of tier stacking under a heterogeneous integration scheme. Tiers comprised of either exclusively Digital or Mixed-Signal/RF can be stacked on top of Digital and Analog tiers resulting in the combinations demonstrated in Table 5.1. Except for the case of Digital applications stacked on top of Analog applications where an ILD thicker than 350nm can limit the inter-tier coupling to tolerable levels, the influence of the inter-tier coupling effects for the rest of the cases is examined in this section with the aid of sensitive circuits in each category.

Specifically, for the victim top-tier applications, the SRAM is selected as a representative example for digital circuits and a RO for the case of Mixed-Signal/RF circuits. An aggressor at the bottom tier can be either a DC voltage equal to the power supply level of either digital or analog circuits, or a high-speed switching pulse such as a digital clock in order to study the impact of dynamic coupling effects.

Table 4.1 Possible stacking combinations under heterogeneous integration in 3DSI

		TOP TIER (EOT=1nm, $V_{DD}=1V$)	
		Digital	Mixed-Signal/RF
BOTTOM TIER	Digital ($V_{DD}=1V$)		
	Analog ($V_{DD}=2.5V$)		

Under the foregoing analysis, the stacked circuit examples which will be studied in the following sections are presented in Table 4.1. In detail, a 2-bitcell Sequential 3D SRAM is selected for the “digital on digital” case and a RO on top of a DC bias of 2.5V for the “Mixed-Signal/RF on Analog” case. Moreover, in order to construct a solid conclusion for the Mixed-Signal/RF on digital circuits, the impact of dynamic coupling has also been studied featuring a digital clock at the bottom tier.

4.1.1 2-bitcell Sequential 3D SRAM (Digital on Digital case)

Within the More-than-Moore paradigm, 3DSI SRAM cells are framed as an extremely appealing architecture as they can provide denser and faster memory blocks, co-integrated among various components (heterogeneous integration). Related works [112]–[117] clearly demonstrate the virtues of this option. Therefore, in order to study the possible impact of the coupling-induced V_{TH} shift on a circuit’s operation, a 6-Transistor (6T) SRAM cell has been selected as a reference. Thus, for our analysis, the configuration of a 3DSI 2-bitcell SRAM is examined, i.e. two stacked SRAM cells

that are identical in layout design, so that the inter-tier static coupling effects are maximized.

4.1.1.a SRAM bitcell architecture

Before proceeding to the analysis of coupling effects, the reader shall be familiar with the SRAM bitcell architecture. An SRAM bitcell is the basic building block of the SRAM array. Each bitcell circuit is capable of storing single bit of information. It provides non-destructive read operation, write capability and data storage as long as the SRAM bitcell is powered up. Fig. 4.1 shows a schematic view of a 6T SRAM bitcell which can be either at the top- or bottom-tier of the 3DSI process scheme. However, because of the asymmetrical SOI structure of the top-tier devices, their back-gates will be tied to the bias of the respective bottom-tier devices.

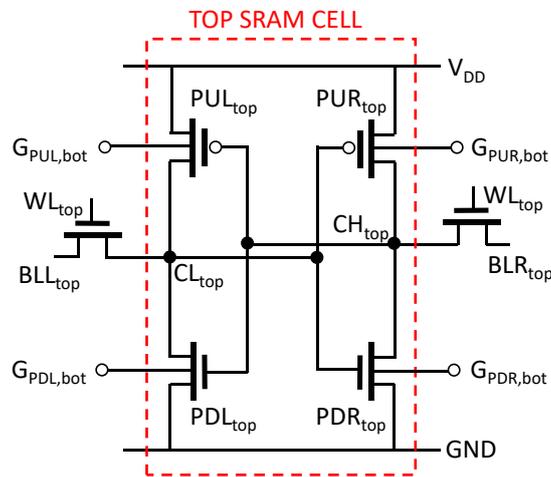


Fig. 4.1 Schematic view of the top-tier SRAM cell

The 6T SRAM bitcell configuration of Fig. 4.1 consists of two identical cross coupled inverters (left: INV 1, right: INV 2) and two access transistors connected to each data storage node. The inverter pair is connected in a positive feedback loop that forms a latch and holds the binary information. It can be in one of the two stable states of an SRAM bitcell, corresponding to the bit value stored '1' and '0'. The data in the SRAM bitcell is stored as long as the power is maintained to the bitcell.

The access transistors are controlled by the wordline (WL) and serve as switches between the inverter pair and the complementary pair of bitlines (BLL, BLR), which are used to read in or write to the bitcell. The bitcells are accessed horizontally by asserting the wordline during read and write operation. When the wordline of a row is asserted 'HIGH', all the memory bitcells in the selected row are enabled and can be ready for read and write operations. Therefore, an SRAM bitcell can be in three different states: Reading, writing or standby (bit retention).

Fig. 4.2 shows the voltage transfer characteristics of inverter 1 (VTC) and voltage transfer characteristics of inverter 2 (VTC⁻¹) in a 6T SRAM during the read cycle. The metric to quantify the stability of an SRAM bitcell during the read cycle and in hold state is the Read Static Noise Margin (RSNM). The RSNM is defined as the maximum amount of static noise that can be tolerated by the cross-coupled inverter pair so that the bitcell retains its data [94]. Between the two stable states of of an SRAM bitcell there is the meta-stable point, a temporary state that the bitcell content can be flipped to one of the two stable states.

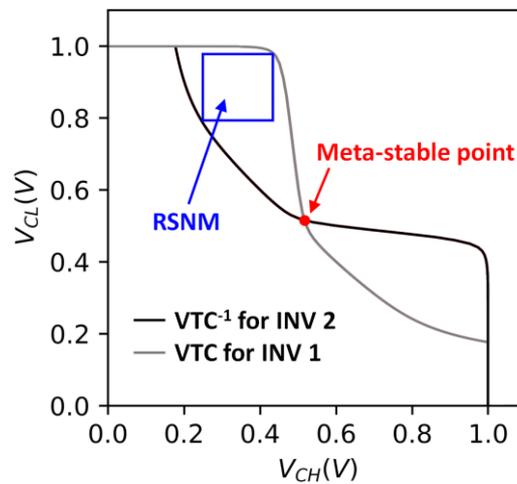


Fig. 4.2 The VTC and inverse VTC of the cross-coupled inverter pair in a 6T SRAM during the read cycle.

4.1.1.b Simulation setup description

As presented in Chapter 3, the inter-tier coupling results in a Threshold Voltage shift (ΔV_{TH}) for the stacked devices and decreases exponentially with the ILD thickness. For digital device stacking – i.e. top/bottom tier contain purely digital devices with $V_{DD}=1V$ – it has been demonstrated that the coupling induced threshold voltage shift is nearly 16mV for $t_{ILD}=130nm$. Except for using coupling advantageously [118], previous work considering undesirable coupling impact [119] has been carried out only for a single S3D SRAM bitcell having half of the transistors in each tier. Fig. 4.3 shows a simplified layout representation of the S3D 2-bitcell SRAM under study. Because of the asymmetric double-gate SOI structure of the top-tier transistors, the Interlayer dielectric functions as their BOX and therefore their BG terminals are indeed the front gate terminals of the respective bottom tier transistors.

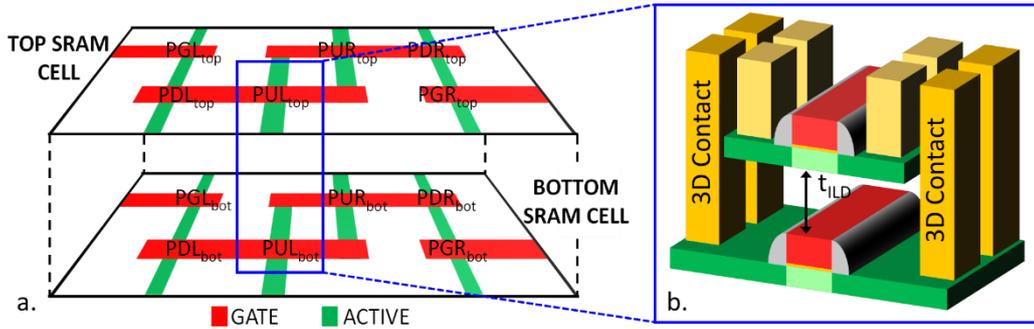


Fig. 4.3 (a) Simplified layout representation of the superimposed monolithic 3D SRAM bitcells under study with (b) a zoom-in view of the stacked device configuration.

In order to assess whether the bottom SRAM cell operation can significantly affect the top SRAM cell performance, some of the most common stability metrics were investigated: the Read and Write Static Noise Margin (RSNM & WSNM) and the Supply Read Retention Voltage (SRRV), that can provide a deep overview of the top SRAM cell static stability [120], [121]. The impact of bottom-tier coupling was studied and compared to that due to mismatch-induced variations, using SPECTRE [36] simulations of the circuit with or without the bottom-tier coupling.

The model chosen to describe the behavior of the top-tier transistors is the LETI-UTSOI MOSFET model (version 2.11) [37] that accurately captures the device characteristics after proper parametrization with the experimental data presented in § 3.2.1. The results (Fig. 4.4) show very good fitting between measurements and model concerning the static characteristics for the required transistor biasing. In detail both linear and saturation behavior as well as the 15.6mV shift of the top transistor's threshold voltage due to bottom gate coupling, are accurately captured.

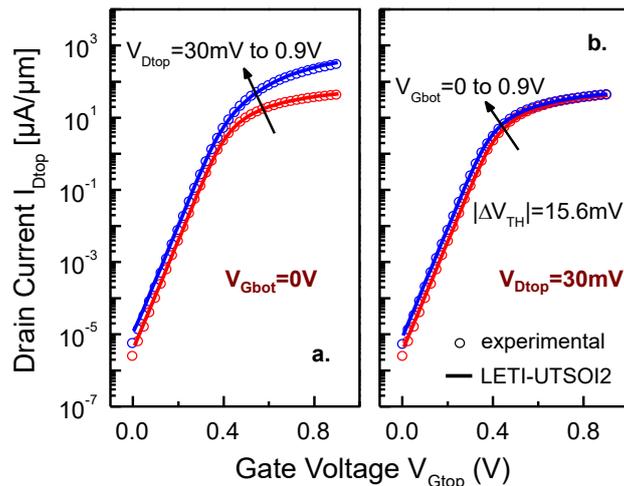


Fig. 4.4 Drain current versus gate voltage for a top-tier NMOS device ($L = 0.1 \mu\text{m}$). Circles and lines denote experimental and simulation results, respectively.

For the bottom SRAM cell operation 3 cases were examined: 1) no operation (zero power supply), 2) a stored '0' ($V_{\text{CLbot}}=0\text{V}$, $V_{\text{CHbot}}=1\text{V}$), 3) a stored '1' ($V_{\text{CLbot}}=1\text{V}$, $V_{\text{CHbot}}=0\text{V}$). Table 5.2

summarizes the bottom transistor gate bias for each of the 3 cases. These conditions were applied in the BGs of the respective top transistors to emulate the inter-tier coupling effect.

Table 4.2 Cases of bottom transistor gate bias.

	Bottom	Bottom SRAM ON	
	SRAM OFF	Stored '0'	Stored '1'
$V_{PULbot} & V_{PDLbot}$	0 V	1 V	0 V
$V_{PURbot} & V_{PDRbot}$	0 V	0 V	1 V

4.1.1.c SRAM stability metrics analysis

The RSNM represents the maximum tolerable DC noise voltage at each storage node before causing a read upset. The extraction of the RSNM was performed by applying mismatch-related Monte Carlo simulations to capture the impact of the mismatch variations. The SRAM cell can be repeated over 1 million times in memory circuits resulting in 6σ of mismatch variations. However, the 3σ limit is critical enough to compare it with the coupling-induced shift and requires 1000 runs rather than over 1 million in the case of the 6σ limit. From the obtained butterfly curves (Fig. 4.5 (a)), the mean represents the typical behavior while the blue curve shows the worst-case of mismatch among the 1000 runs.

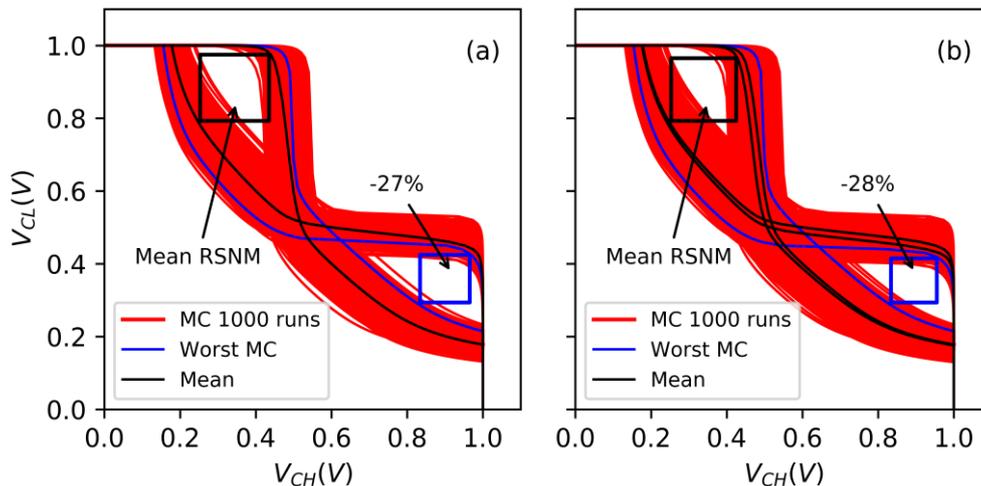


Fig. 4.5 (a) Impact of V_{TH} mismatch on RSNM of a top-tier SRAM bitcell, (b) Addition of the static coupling because of the bottom tier SRAM operation.

Following the same methodology as for the RSNM, we also extracted the WSNM that characterizes the write-ability of the SRAM bitcell (Fig. 4.6). Concerning both RSNM and WSNM, the largest square was fit for the worst set to estimate the mismatch related SNM degradation. Additionally, the mean SNM was extracted and comparing the two values, we extracted the impact

of V_{TH} mismatch (-27% for RSNM, -10% for WSNM). As shown in Fig. 4.5 (b) and Fig. 4.6 (b), the coupling-induced V_{TH} shift can further reduce both the RSNM and the WSNM by 1%.

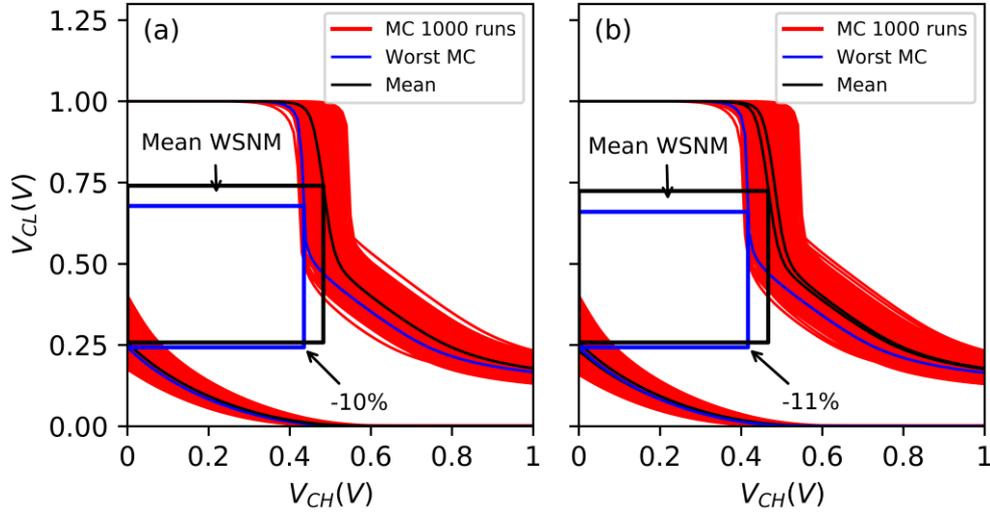


Fig. 4.6 (a) Impact of V_{TH} mismatch on WSNM of top tier SRAM, (b) Addition of the static coupling because of the bottom tier SRAM operation.

Regarding the SRRV, it is defined as the maximum allowed reduction of cell supply voltage for which the read stability is not affected. It is an equally important stability metric for SRAM cells [120]. It can be estimated measuring the bitline current I_{BL} while the power supply of the cell (V_{CELL}) is ramped down. At a specific value of the V_{CELL} (called V_{flip}), the stored bit is flipped and I_{BL} drops suddenly. Then the SRRV is extracted as

$$SRRV = V_{DD} - V_{flip} = 1 - V_{flip} \quad (4-1)$$

The simulation results for a typical top-tier bitcell at the three bottom-tier bitcell operation cases are shown in Fig. 4.7 (a). The impact of mismatch can be seen in Fig. 4.7 (b), while with the addition of the coupling induced shift is shown in Fig. 4.7 (c). In this latter case, we obtain an additional SRRV reduction of 3.5% (-34.5%→-38%). From Fig. 4.7, the effects of the value stored in the bottom-tier SRAM on the bitline discharge of the top-tier SRAM can be evaluated. The latter mimics a readout for a stored '1' and for SRRV, it is apparent that the most critical case is when a '1' is stored at the bottom cell. Due to symmetry reasons, the most critical case for a stored '0' will be when a '0' is stored at the bottom cell. Nevertheless, the effect of inter-tier coupling on the SRAM stability metrics (1 to 3.5%) looks negligible compared to the mismatch-induced variations. In conclusion, the fact that SRAM features devices with very small sizes and thus significantly affected by device variability seems to allow for a safe superimposing of SRAM arrays with $V_{DD} = 1V$ across tiers with an ILD of 130 nm thickness.

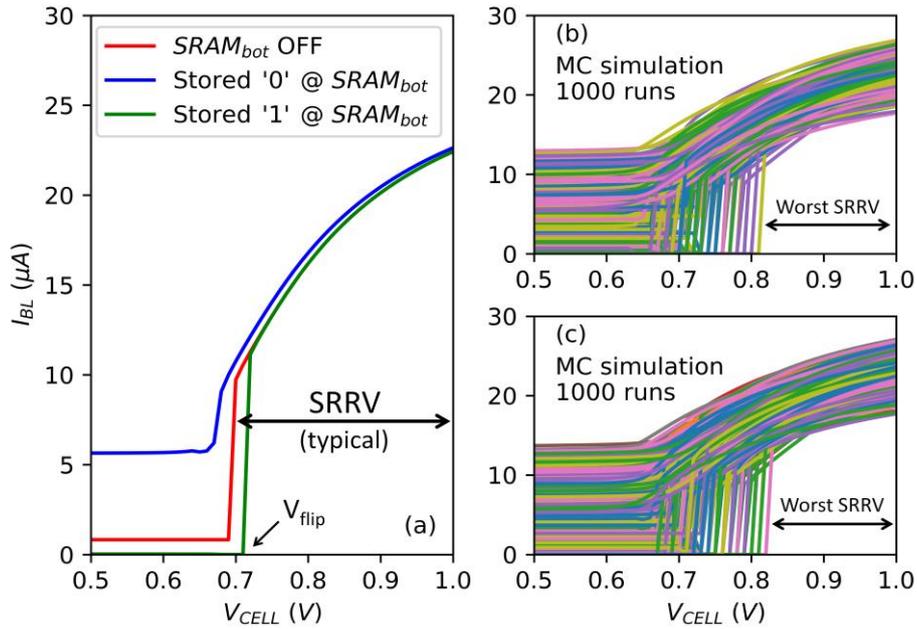


Fig. 4.7 Bit-line current versus cell supply voltage. (a) Typical results for the three bottom-tier bitcell operation cases (b) Monte Carlo simulations with mismatch variations (c) Monte Carlo with the same random number generation seed, adding also the static coupling induced shift.

4.1.1.d Impact of relative misalignment for the stacked SRAM cells

The impact of the relative positioning was also studied, by placing each top-tier transistor drain in different distances with respect to the bottom-tier transistor gate. For the purpose of this study, mixed-mode TCAD simulations were performed on a circuit containing the stacked SRAM cells. A simplified layout of the top-tier circuit is shown in Fig. 4.8: each transistor is composed by a TCAD structure including the stacked transistors and all the necessary physical models. Moreover, we considered two cases: a gate overlap=1 when all bottom- and top-tier transistor gates are perfectly aligned (Fig. 4.8 (a)) and a gate overlap=0 when the bottom-tier gates are aligned below the respective top-tier transistor drain regions (Fig. 4.8 (b)).

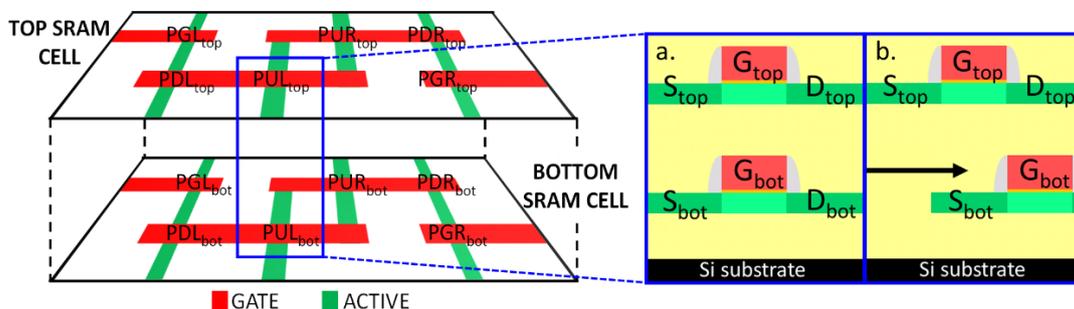


Fig. 4.8 Simplified layout representation of the superimposed SRAM. Each top-tier SOI is comprised by the TCAD structure shown here

The DC characteristics of the top-tier SRAM circuit for each case of bottom-tier operation (no power supply, stored'0', stored'1') and for the two positioning scenarios (gate overlap=0/1), are

shown in Fig. 4.9 It is evident that the maximum coupling induced SNM reduction of 10 mV for the top tier SRAM occurs when there is no misalignment between the stacked SRAM cells.

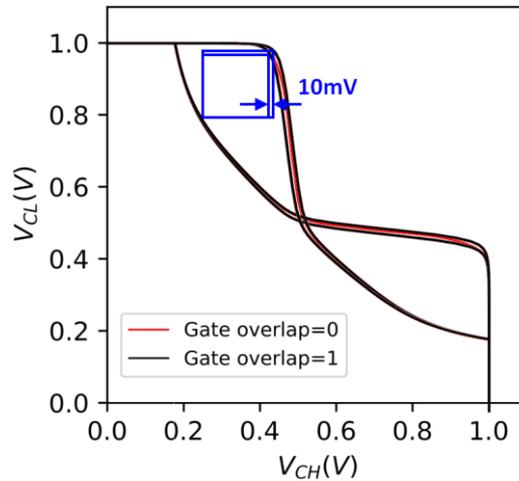


Fig. 4.9 Butterfly diagram of a top-tier SRAM bitcell for the two cases of relative misalignment between stacked devices

4.1.1.e Impact of dynamic coupling effects on top-tier SRAM bit retention

The immunity of the top-tier SRAM cell to dynamic coupling from the bottom SRAM cell can be studied with transient analysis. As seen from the butterfly curve marked in black color in Fig. 4.10 (a), the intersection point of the voltage transfer characteristic of the SRAM cell is a meta-stable state. This means that the static SRAM operation can potentially move to any of the two stable states so that any noise applied can cause the bitcell content to flip.

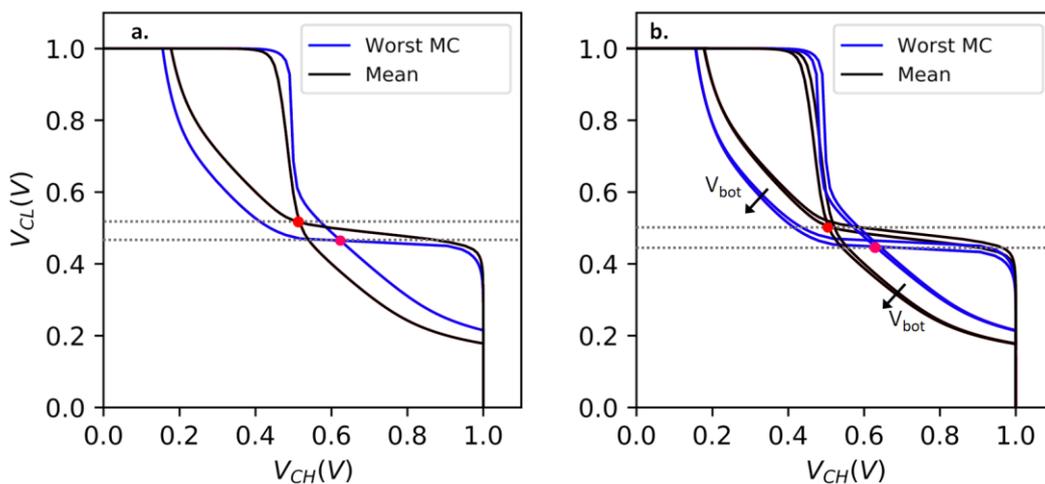


Fig. 4.10 (a) Mean and worst MC butterfly diagram of a top-tier SRAM bitcell indicating the meta-stable point (b) Addition of the static coupling because of the bottom tier SRAM operation.

The impact of the mismatch is observed in the same figure, by causing the inverse VTC of the right inverter to move downward and the VTC of the left inverter to move to the right direction which

practically results in a lowering of the meta-stable point. Moreover, the static coupling influences the threshold voltage of the SRAM transistor resulting in a further shifting of the butterfly curves as studied in the previous sections (Fig. 4.10 (b)). As an outcome the meta-stable point for both the typical and the worst mismatch case of the SRAM cell, is even lowered, yet by a small amount.

The meta-stable point can be considered as a critical stability point during transient read operation. Implementing the setup schematically illustrated in Fig. 4.11, the impact of the dynamic coupling was assessed emulating a READ operation for the top SRAM while the bottom one attempts a WRITE operation at the same time.

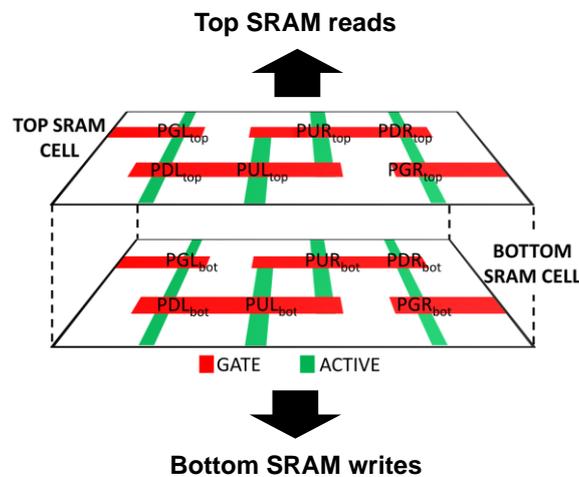


Fig. 4.11 Simplified layout representation of the superimposed SRAM where the top SRAM reads at the moment that the bottom SRAM attempts a write operation.

Without loss of generality, it is assumed that the output node of the left inverter, Channel-Low (CL) node initially is at '0' and thus the Channel-High (CH) node is at '1'. When both the Bit-Lines (BL and BLL) are pre-charged and Word-Line (WL) is enabled, BL should be pulled down through the transistors PGL and PDL, since they form a potential divider and raise the CL node potential to ΔV (Fig. 4.12 (a)). At that time t_1 , the bottom SRAM can be OFF or write '0' or '1' with the shortest switching time in 28 nm FDSOI, that is $t_R \sim 10\text{ps}$ [72]. As seen from Fig. 4.12 (b), the potential difference in the CL node of the top SRAM is not exceeding 5 millivolts for all write operation cases of the bottom SRAM cell, remaining well below the meta-stable point even for the worst mismatch case.

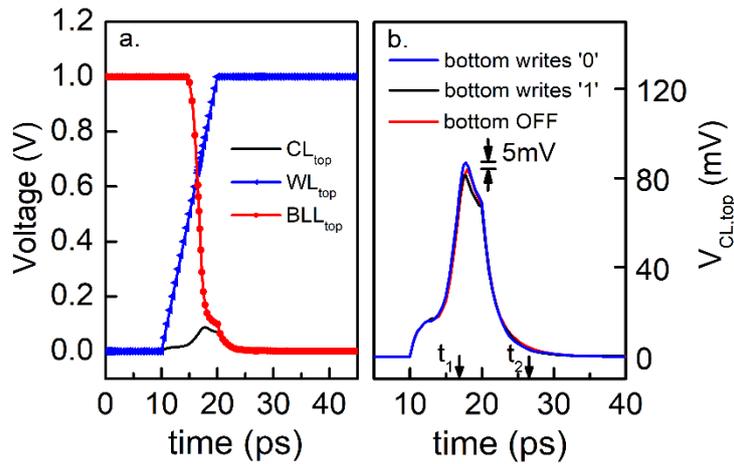


Fig. 4.12 (a) Read operation for top-tier SRAM cell: The WL_{top} is enabled and BLL_{top} discharges to $V_{CL,top}$. (bottom SRAM off). (b) $V_{CL,top}$ during a write operation ($0 \rightarrow 1V$ and $1 \rightarrow 0V$ from t_1 to t_2) with 10ps rise time (shortest in 28FD) at the bottom SRAM.

As an outcome, dynamic coupling effects induced by the bottom-tier SRAM cell operation do not result in a read destructive operation for the top-tier SRAM cell. Consequently, the demonstrated immunity of a sensitive digital circuit like the SRAM to both static and dynamic coupling shows that digital on digital circuits with 130 nm thick ILD do not necessarily need an inter-tier GP.

4.1.2 RO stacked on top of an analog tier (Mixed-Signal/RF on Analog case)

In order to assess the sensitivity of top-tier Mixed-Signal/RF circuits on electrostatic coupling due to the direct stacking on top analog tier circuits, the circuit example of a 3-stage RO (Fig. 4.13) has been selected.

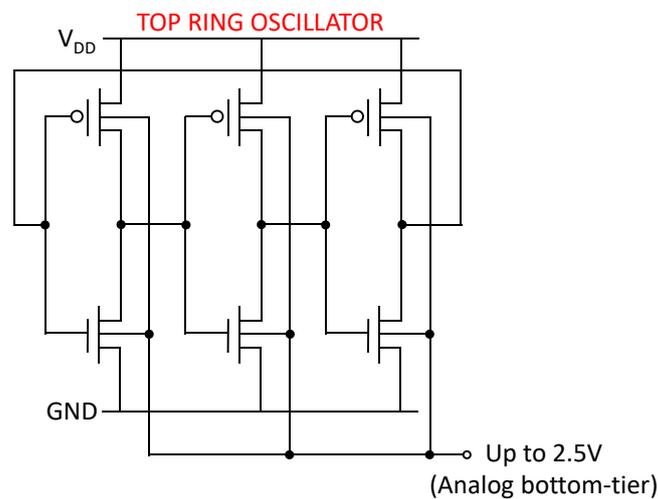


Fig. 4.13 Top tier RO composed of three NOT gates. The back-gate bias of each SOI device can go up to either 1V (V_{DD} for bottom-tier SOI with $EOT=1nm$) or 2.5V (V_{DD} for bottom-tier SOI with $EOT=5nm$)

In this configuration, each top-tier device is considered to have its back-gate tied to the voltage bias of the bottom gate electrode which can go up to 2.5V. Fig. 4.14 shows a frequency shift of 510MHz for a 30.2 GHz oscillating signal due to the 2.5V shift of the bottom-tier electrode bias.

This 1.68% shift of the fundamental frequency of the RO is far from negligible for RF applications, therefore an inter-tier isolation is necessary. However, regarding the phase noise of the top RO, there is no observable impact of DC coupling from the bottom Analog tier electrode bias (Fig. 4.15).

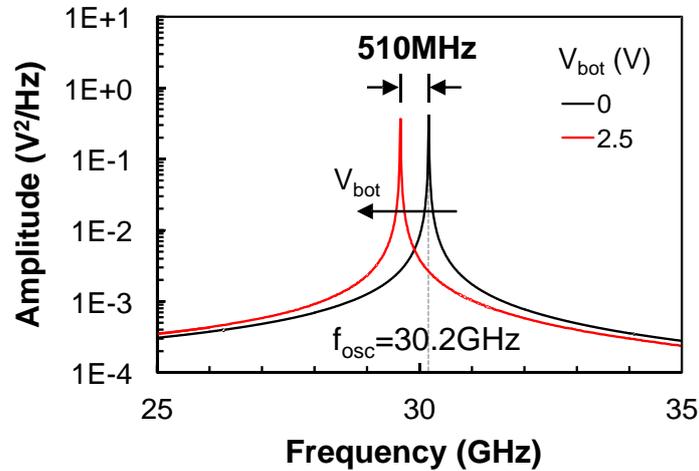


Fig. 4.14 FFT for top-tier RO with 0V, 1V and 2.5V bias application at each SOI back-gate.

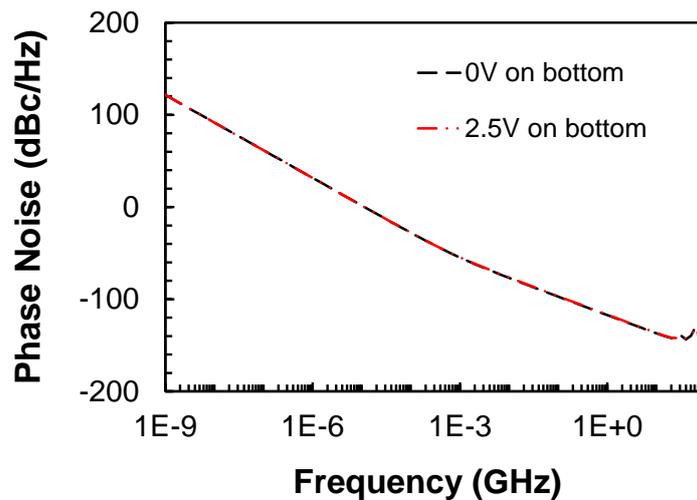


Fig. 4.15 Phase noise shift for top-tier RO with 0-2.5V bias application at each SOI back-gate.

4.1.3 RO stacked on top of a digital tier (Mixed-Signal/RF on Digital case)

Clock generators are an essential part of digital circuits, as they coordinate actions and synchronize different parts of the circuit. A clock signal produced by a clock generator, is a high-speed switching signal between two logic levels, 0 and 1. In particular, for an EOT in the 1 nanometer range the logic 1 coincides the 1V of the power supply. As a consequence, the high frequency content of a clock signal can be an intensive source of noise coupling for stacked Mixed-Signal/RF.

To evaluate the impact of a digital clock operating at the bottom tier on the top-tier RO, a periodical trapezoidal voltage signal was applied at the BG each top-tier device (Fig. 4.16) with a

Section 4.1 - Impact of inter-tier coupling on circuit operation

swing voltage of $V_{swing}=1V$, a frequency of $f_{clk}=5GHz$, a rise/fall time of $t_R=8ps$ and a pulsewidth of 92ps.

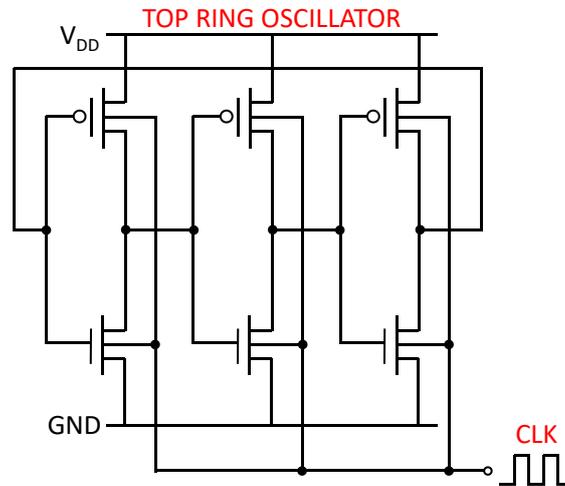


Fig. 4.16 Top tier RO composed of three NOT gates. The back-gate bias of each SOI device is tied to a bottom-tier digital clock signal.

The result in the frequency domain (Fig. 4.17) is a mixing product with a frequency shift (pulling) of 80MHz and several spurious harmonics appearing in the signal’s spectrum. However, it may be noted that the scenario of each top-tier device being stacked upon a digital gate with an applied clock signal is an extreme case and rather unrealistic.

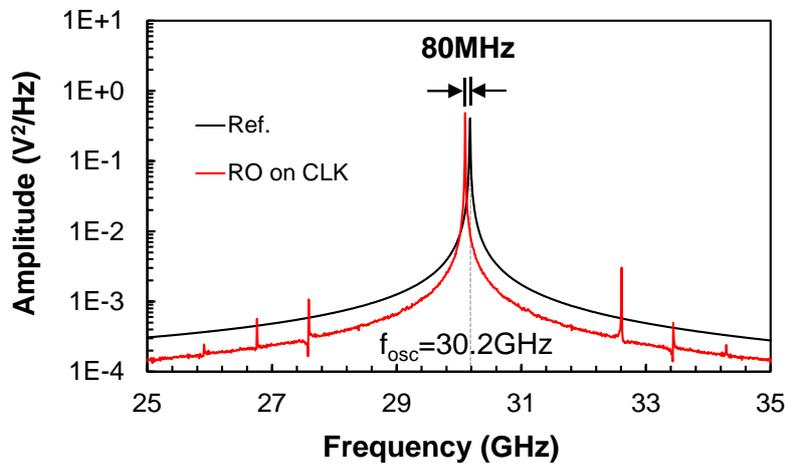


Fig. 4.17 FFT for top-tier RO with the clock signal applied at each SOI back-gate along with the reference case

On the contrary, it is quite possible that a single device of the three-stage RO can be influenced by a clock signal at the bottom-tier. Fig. 4.18 shows the result of the RO spectrum after enabling the clock signal at the BG of one of the PMOS or NMOS devices of the three RO stages independently. As observed, the frequency deviation from the reference state can be around 340MHz while the harmonic purity of the oscillating signal worsens.

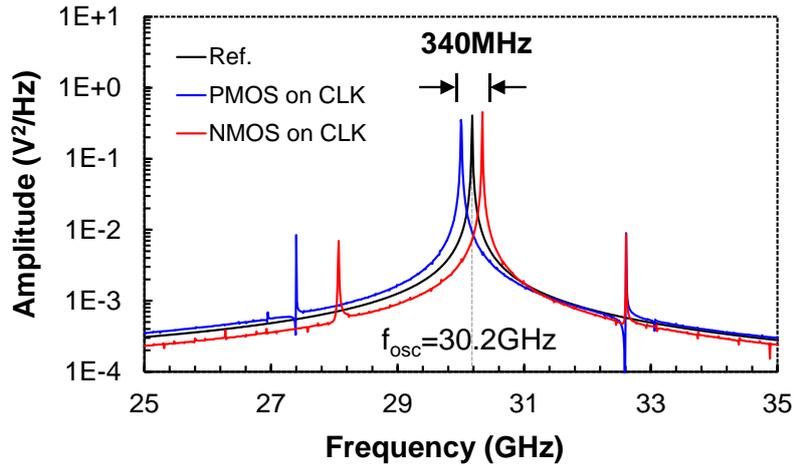


Fig. 4.18 FFT for top-tier RO with the clock signal applied at PMOS or NMOS back-gate along with the reference case

Taking into account the foregoing analysis, it is rather reasonable to conclude that a decoupling layer is mandatory to ensure the desired operation of Mixed-Signal/RF being stacked on digital circuits.

4.2 Methods and techniques to mitigate inter-tier coupling effects in 3DSI

4.2.1 Critical dimensioning of 3DSI structures and 3D design rules

The inter-tier coupling effects depend strongly on the characteristic dimensions of a 3D sequentially integrated structure. These are process depended parameters, i.e., they are determined by the process flow (etching, deposition) and a circuit designer cannot control them. On the other hand, there are certain parameters related to the top layout view of a device which are under the control of a circuit designer, such as the width and the length of an active device.

Fig. 4.19 recalls the characteristic dimensions of a 3DSI structure comprised of 2 stacked devices under a specific layout configuration A. In particular, Fig. 4.19 (a) illustrates the top layout view whereas the respective cross-section A'A is shown in Fig. 4.19 (b). The parameters affecting the inter-tier coupling which can be altered by a circuit designer are the gate width and length of the two devices (here they are considered identical in dimensions), the distance of the 3D contact to the top active (3DCO-RX) as well as the distance of the 3D contact to the top gate electrode (3DCO-PC). The minimum allowed values for the last two parameters are process depended.

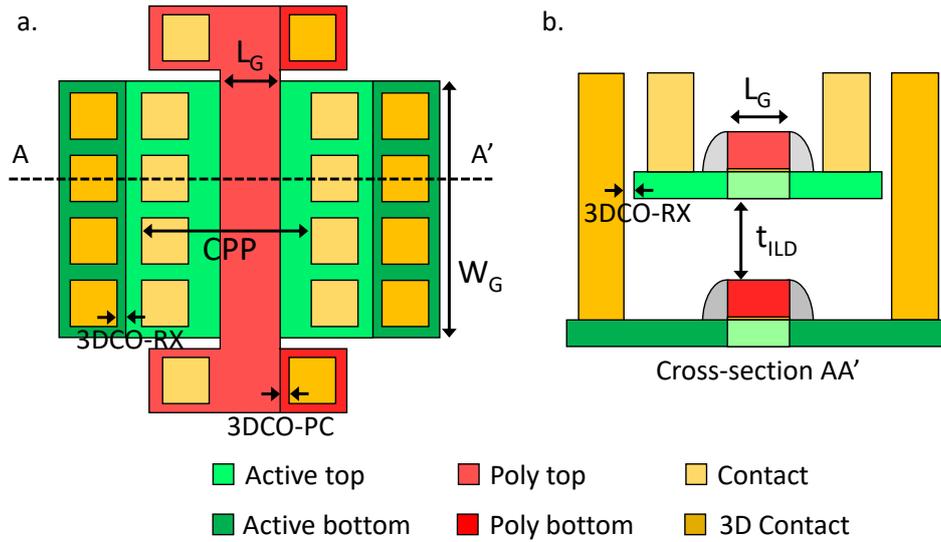


Fig. 4.19 Layout configuration A of two stacked devices in 3DSI with the characteristic dimensions. (a) Top layout view and (b) Cross-sectional AA' view

Alternatively, the layout configuration B of Fig. 4.20 can be adopted in case of direct device stacking. This configuration provides a smaller form factor for the stacked structure and the same footprint for both devices. In addition, layout B provides slightly lower crosstalk between top/bottom drain electrodes (4 dB difference for $W_G=1\mu\text{m}$). However, the drawbacks are that: i) the contact density upon the active region is decreased compared to the layout configuration A and ii) the bottom-tier drain electrode can be capacitively coupled to the top-tier gate electrode. The latter is a function of the 3DCO-PC distance with a minimum value determined by the CPP parameter of the technology node.

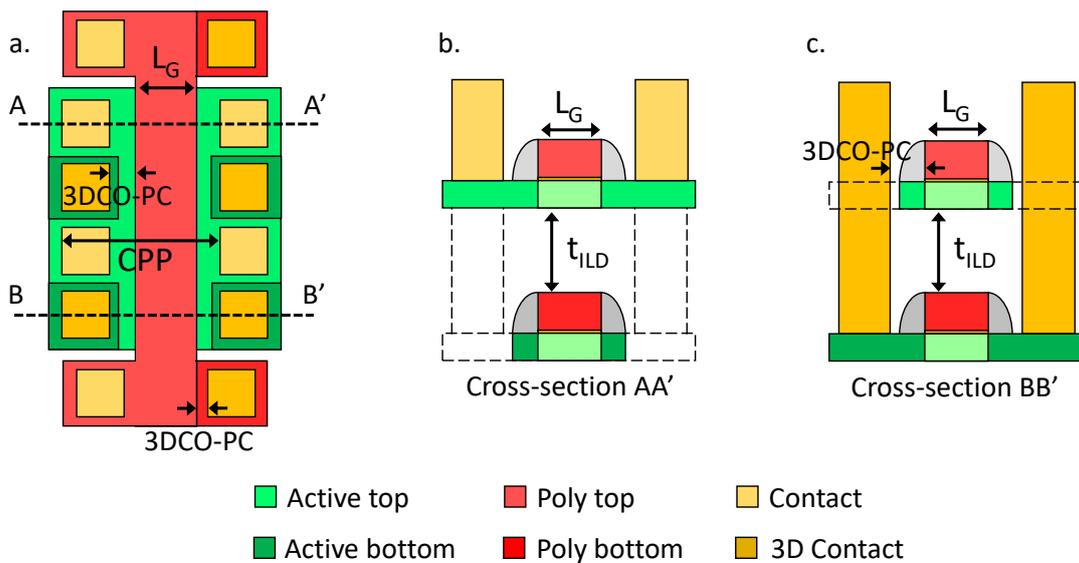


Fig. 4.20 Layout configuration B of two stacked devices in 3DSI with the characteristic dimensions. (a) Top layout view, (b) Cross-sectional AA' view and (c) Cross-sectional BB' view

Fig. 4.21 plots the crosstalk results extracted at 1GHz for the layout configuration B versus the 3DCO-PC distance. It becomes apparent that the crosstalk between $D_{bot}-D_{top}$ gets further decreased with the downscaling of the 3DCO-PC distance, while the $D_{bot}-G_{top}$ crosstalk gets enhanced. Therefore, it is on the designer's hands to choose the layout configuration of the top-tier devices with respect to the bottom ones, identifying the most critical nodes in his circuit design and isolating them.

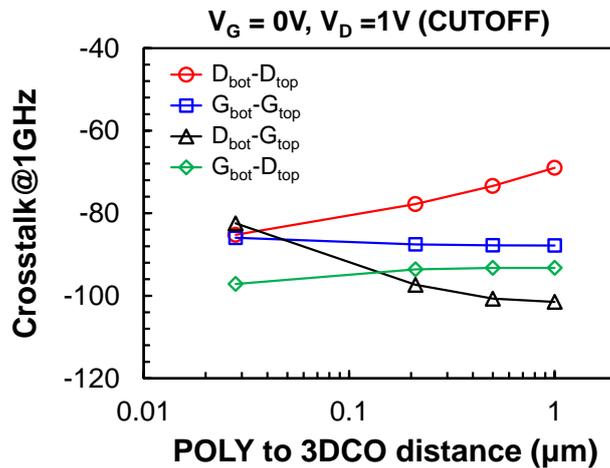


Fig. 4.21 Crosstalk at 1GHz between different electrodes of the two stacked devices under the layout configuration B (Fig. 4.20) versus the distance between the top-tier gate electrode and the 3D contact connected to the bottom-tier drain diffusion area.

4.2.1.a ILD thickness optimization

The ILD thickness t_{ILD} is a process parameter which can be tuned accordingly in order to limit the inter-tier coupling effects. The charge-coupling factor of top-tier digital and analog devices decreases exponentially with the ILD thickness (Fig. 4.22), hence the acceptable level of the threshold voltage modulation at a device level for each application (see chapter 3) sets the minimum limit for the ILD thickness.

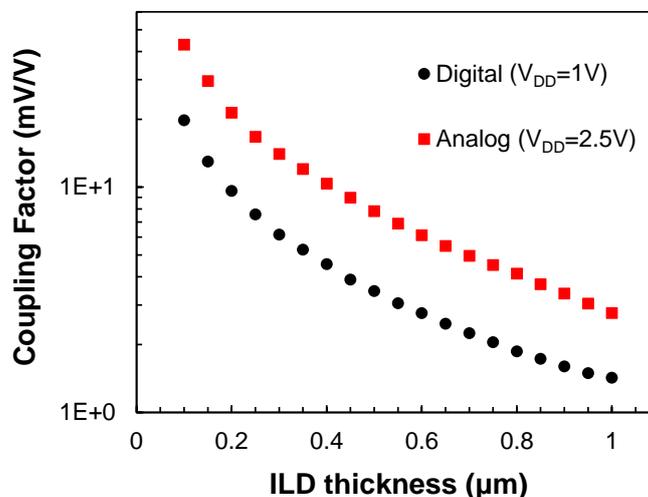


Fig. 4.22 Charge-coupling factor of top-tier digital and analog devices versus the ILD thickness

The impact of the ILD thickness on the crosstalk performance between the stacked tiers was also examined with the aid of TCAD simulations. Using the simulation setup of Fig. 4.23 (a) and varying the ILD thickness, the extracted crosstalk levels are plotted in Fig. 4.23 (b). It is apparent that increasing the ILD thickness from 0.2 to 1µm, a crosstalk suppression of 17dB can be achieved.

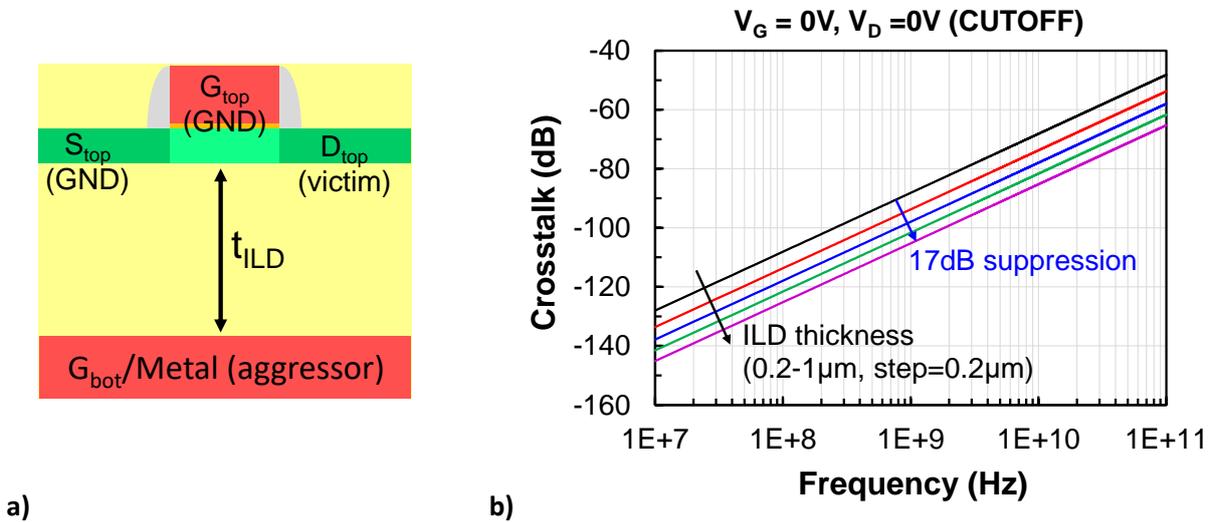


Fig. 4.23 (a) Simulation setup in TCAD for evaluation of crosstalk dependence on ILD thickness (b) Crosstalk levels between the top-tier active device and the bottom-tier electrode versus frequency for different ILD thickness

On the other hand, increasing the ILD thickness worsens the 3D Contact AR (3DCO AR) as depicted in the schematic cross-section illustration of Fig. 4.24. Hence ILD thickness is limited by the 3DCO AR with a preferred maximum at 350nm for the digital top-tier devices on analog bottom-tier ones. For greater reduction of the coupling-induced threshold voltage shift and the crosstalk levels between the stacked tiers, other decoupling methods must be investigated to keep the 3DCO AR at low values.

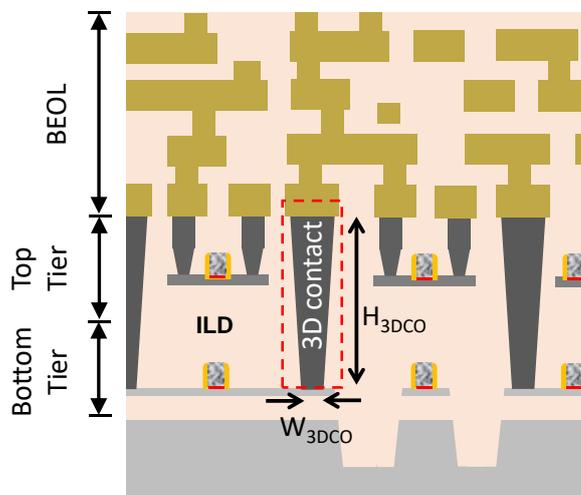


Fig. 4.24 Schematic cross-section view of 3DSI scheme indicating the characteristic dimensions of a 3D contact

4.2.1.b Top/bottom device misalignment

The inter-tier static coupling impact may be efficiently reduced when there is a misalignment between top and bottom device positions. Indeed, implementing the simulation setup shown in Fig. 4.25 (a) for a device with $L_G=1\mu\text{m}$, the bottom device can be misaligned from the top by Δx either along the gate length or width direction. The potential contour plot of Fig. 4.25 (b), as obtained from TCAD simulations, reveals the deformation of the electric field induced by the bottom-tier gate electrode due to the relative misalignment of the two devices. The overlapping area region indicated by the dashed rectangle defines the coupling-induced ΔV_{TH} as shown in the extracted TCAD results (Fig. 4.26).

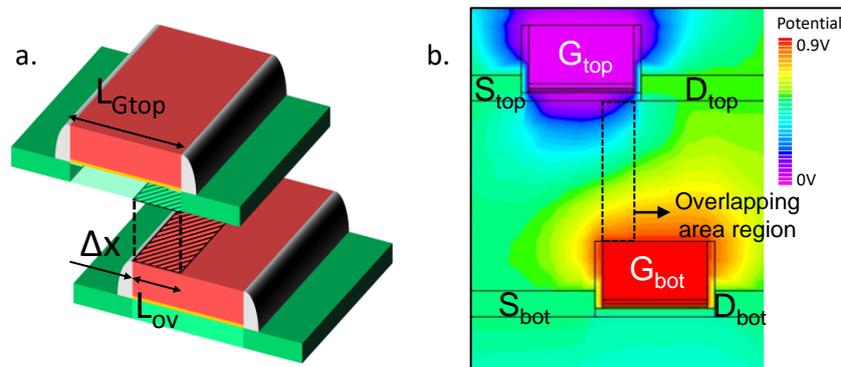


Fig. 4.25 Relative misalignment by Δx between two stacked devices (a) Schematic 3D representation (b) Potential contour plot of the structure extracted from TCAD simulations.

As observed in Fig. 4.26, TCAD simulations revealed that in cases where the bottom-to-top overlapping area ratio is lower than 0.5, the coupling-induced ΔV_{TH} can be decreased by a factor of 3. This observation may function as a guideline for 3D design rules in the near future.

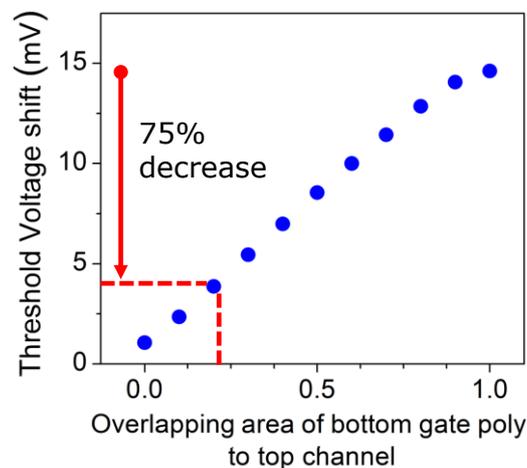


Fig. 4.26 Coupling-induced ΔV_{TH} of top-tier digital devices vs overlapping area of bottom gate poly to top channel ratio.

4.2.2 Inter-tier shielding through GP: challenges and solutions

In 3DSI, vertical coupling between active device tiers has been identified as critical for analog and mixed-signal/RF applications. Therefore, further decoupling is needed for the stacking of tiers incorporating these sensitive applications.

Several methods have been reported concerning the isolation of active devices targeting planar and 3D technologies. Specifically for planar technologies, in [122] a Faraday-Cage isolation structure was presented that can suppress substrate coupling. It consists of a ring of substrate VIAs connected to the grounded backplane at the bottom of the substrate and shorted together by a ring of metal at the top. On the substrate coupling also, Kim et al. [123] have demonstrated RF crosstalk isolation by the use of through-the-wafer porous Si (PS) trenches because of their semi-insulating property. Furthermore, in [124], a method to suppress substrate noise for future RFIC design has been investigated using heavily doped pocket structures.

On the other hand, in SOI technology that incorporates a buried WSi_2 (Tungsten disilicide) metal GP beneath the BOX layer, Stefanou et al. [111] have achieved substrate crosstalk isolation using a metal Faraday cage structure where the isolation region is surrounded completely by solid metal walls. In detail, the Faraday cage is comprised of a buried metal tungsten silicide GP beneath the BOX layer as the bottom of the cage, and vertical metal-lined n polysilicon-filled trenches in the active silicon layer as the cage walls. Although the above-mentioned methods provide efficient crosstalk suppression, they require complex process techniques and large form factor structures that are not suitable for 3DSI where the highest possible density is desired.

Recently, [64] demonstrated a buried metal (TiN) line implementation in a 3DSI process scheme (Fig. 4.27). This inter-tier metal layer acts not only as a back-gate to the top-tier device through the back oxide, but also limits the vertical coupling with the bottom-tier device.

In this section an efficient way of inter-tier electrical isolation is investigated with the insertion of an inter-tier thin conductive layer, i.e. a GP, between the sequential tiers made of a semiconductive material. The necessity for an inter-tier GP integration results from the specifications targeted for each application and the estimation of the trade-off between the process complexity and the inter-tier coupling sensitivity. The screening effectiveness of an inter-tier GP against vertical coupling is investigated taking into account its material properties and the FEOL compatibility.

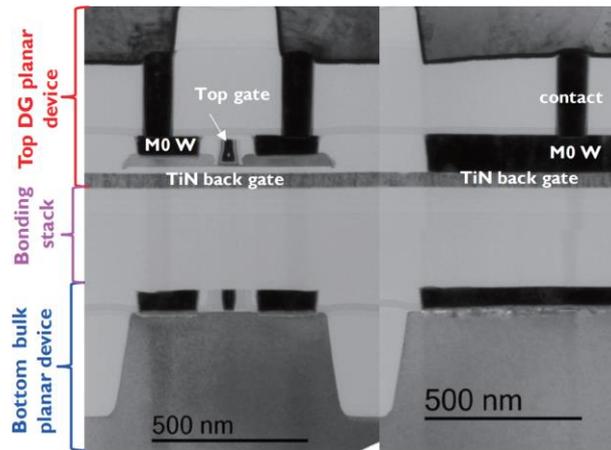


Fig. 4.27 Cross-sectional TEM image of fabricated 3D stacked devices with an inter-tier BG (Courtesy of [64])

Targets for the GP properties are the suppression level and frequency response, minimum thickness and front-end of line compatibility. The simulation setup that was used, is shown in the 3D illustration of Fig. 4.28 (a) and the corresponding cross section AA' in Fig. 4.28 (b). It consists of a digital device ($EOT=1\text{nm}$, $V_{DD}=1\text{V}$) on top of an electrode that can be either the bottom gate or a metal line and in between a layer made of either SiO_2 (no GP case), silicon, polysilicon or copper. The obvious choice for a shield against electric field coupling is a metal, however the use of a semi-conductive material has several advantages that will be discussed in detail in the next section. It is worth mentioning that in order to avoid the GP being floating, a grounded contact (GP_CO) has been placed on it. This qualitative analysis can help conclude on the GP material choice, its dimensions and the ground contact pitch.

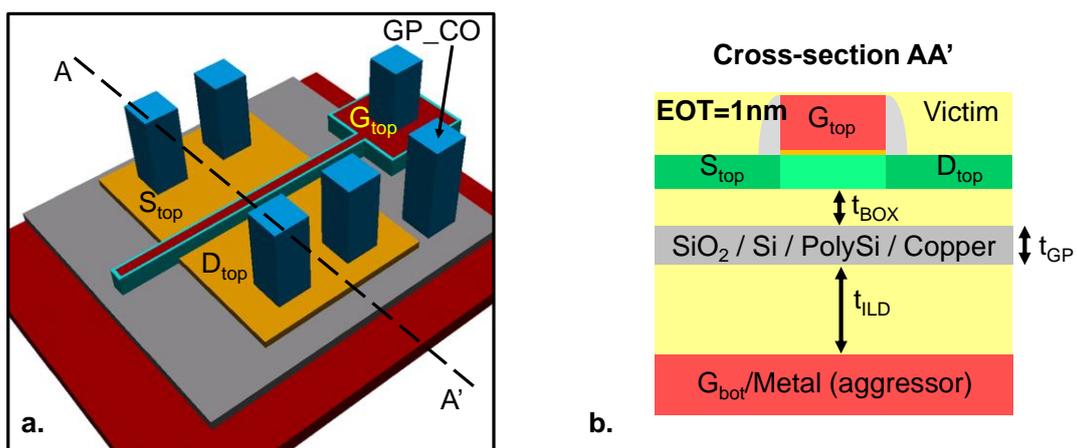


Fig. 4.28 (a) Simulation setup to determine the GP decoupling efficiency. The GP area is 2x the top active area with 1 GND contact. (b) Cross-section AA' view.

For the purpose of the analysis, TCAD simulations have been performed. Although TCAD provides accurate answers on problems employing semiconductors, its quasistatic approach may not

be appropriate for high frequency analysis. For that reason, HFSS has been utilized for the validation of the TCAD simulations in the high-frequency domain.

4.2.2.a Electrostatic screening

As studied in chapter 3, the capacitive coupling of the bottom-tier gate electrode to the top device channel can cause a shift of the top-tier device V_{TH} . This is the most significant coupling mechanism as it provides a direct modulation of the top-tier device drain current by the bottom-tier device electrodes both in DC as well in AC domain via the back-gate transconductance.

With the insertion of an inter-tier GP, the vertical electric fields responsible for the static coupling can be suppressed as seen by equation 4.2, supposing that the GP has a sufficient coverage of the bottom tier bias electrode and contains at least one grounded contact with low resistance. Then the top-tier device threshold voltage shift induced by the bottom-tier gate electrode, becomes a function of the remaining fringing fields as the GP covers only the bottom part of the active device.

In order for a semiconductor to act as a shield, its conductivity must be comparable to a metal. Fig. 4.29 shows experimental data [125] for the resistivity of monocrystal and polycrystal silicon (polysilicon) versus their concentration of phosphorus dopants (n-type). It is apparent that for low doping concentrations, polysilicon presents an enhanced resistivity compared to monocrystal silicon especially, yet for doping concentrations greater than 10^{18} cm^{-3} the difference in the resistivity of the two materials decreases exponentially, becoming negligible above 10^{20} cm^{-3} .

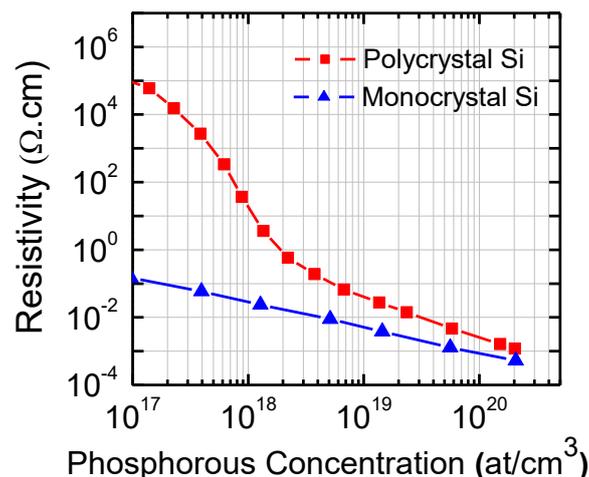


Fig. 4.29 Resistivity of phosphorus-implanted, low pressure poly-crystal silicon films as a function of average dopant concentration. The resistivity of n-type, single-crystal silicon is shown for comparison [125].

TCAD simulations were carried out to probe the impact of doping concentration on the coupling-induced ΔV_{TH} for an inter-tier GP made of silicon. Three cases of GP covering were

simulated, the first (1) for a GP area 2 times the active area and a large bottom-tier gate electrode (Fig. 4.30 (a)), the second (2) for the same GP area as previously and equal areas of top/bottom-tier gate electrodes (Fig. 4.30 (b)) whereas the last one (3) features a very large GP (Fig. 4.30 (c)) covering completely the top device active area. The results are shown in Fig. 4.31.

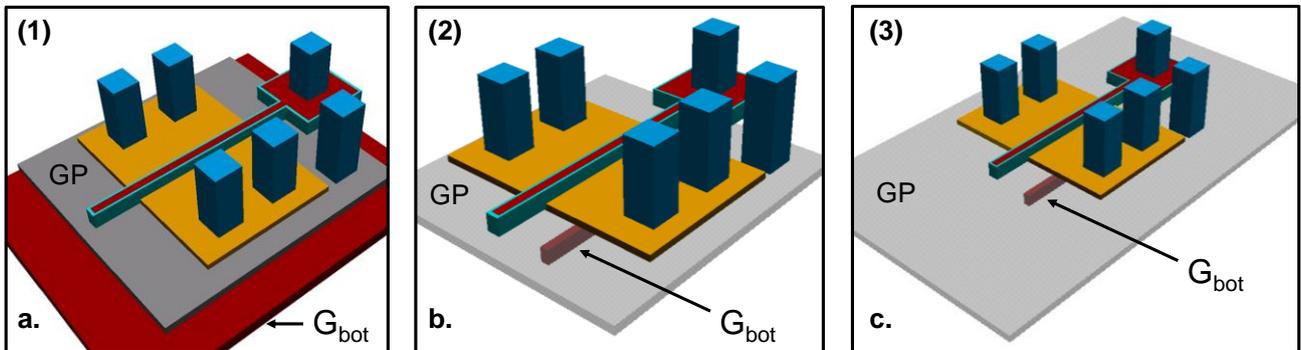


Fig. 4.30 Simulation setup in TCAD to evaluate the decoupling efficiency of the inter-tier GP when it has an area 2 times the active one and the bottom-tier gate electrode is (a) large or (b) equal in area with the top-tier gate electrode, and (c) when the GP is very large, covering completely the top device active area

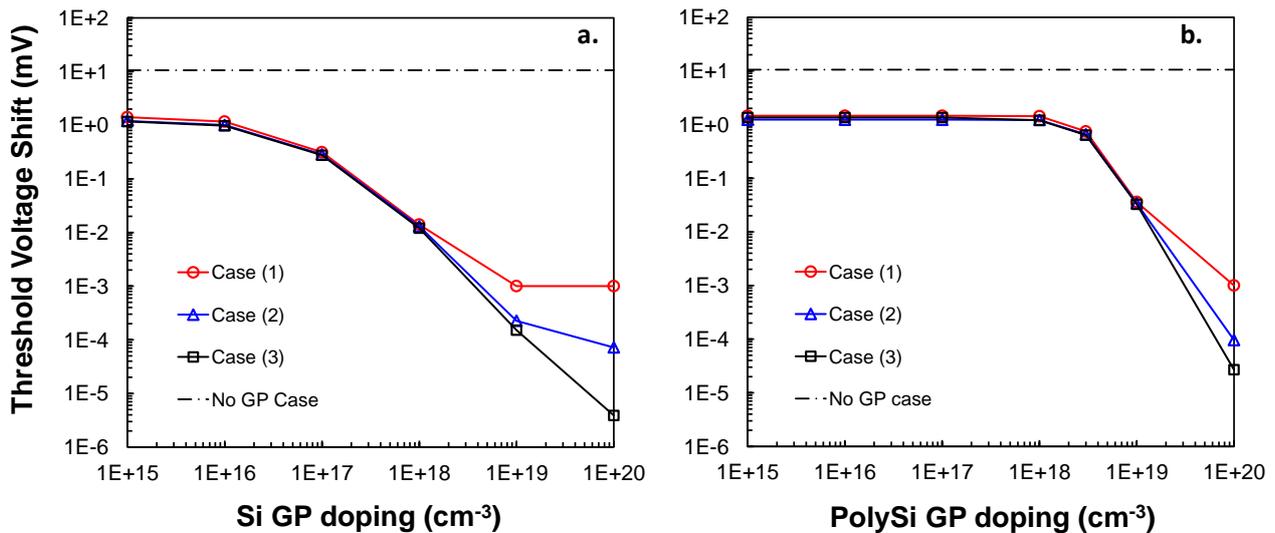


Fig. 4.31 Coupling-induced ΔV_{TH} of the top-tier device to the bottom-tier electrode versus average dopant concentration in the inter-tier GP made of (a) silicon and (b) polysilicon

Before analyzing the impact of GP doping level, it is worth noticing how even the sole presence of an undoped (or lightly doped) grounded GP layer (either Si or polySi) causes a suppression of one order of magnitude, regardless its area. Nevertheless, if a stronger decoupling is necessary, it is evident that for doping concentrations above 10^{17} cm⁻³ the static coupling suppression is exponential, reaching 5 orders of magnitude for 10^{20} cm⁻³ n-type doping when the GP is very large (limited fringing fields). On the other hand, for $Area_{G_{bot}} > Area_{GP}$, the suppression obtained by the insertion of the inter-tier GP exhibits a plateau for doping concentrations above 10^{19} cm⁻³ due to

fringing electric fields. Nonetheless, for the intermediate cases where the GP is not very large compared to the top-tier device channel, yet the bottom-tier gate electrode is significantly covered by the GP, the suppression follows the trend of the blue line in Fig. 4.31 (a).

Alternatively, Fig. 4.31 (b) shows TCAD simulation results obtained by choosing Polysilicon as the material of the inter-tier GP. As observed, the trend is the same for the three cases of GP covering as for the Silicon GP, however higher doping concentrations are needed in order to reach a quasi-metallic behavior for the PolySi GP and therefore act as a shield. For comparison, a copper GP was also simulated and the coupling-induced ΔV_{TH} results for the three materials are plotted in Fig. 4.32, considering a doping concentration of 10^{20} at/cm³ for both silicon and polysilicon GP.

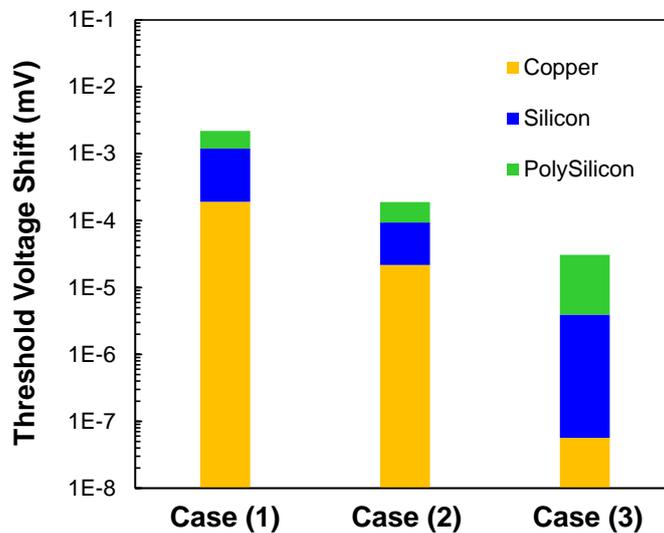


Fig. 4.32 Coupling-induced ΔV_{TH} results comparison between silicon, polysilicon and copper as the material in the GP layer region

The insertion of a silicon GP between the active device tiers yields a superior static decoupling performance compared to the plain increase of the ILD thickness when there is no GP as seen from Fig. 4.33. From the lowest to the highest doping concentration of a Si GP the suppression level can be respectively 1-5 orders of magnitude greater than a 1 μ m thick ILD. Moreover, even the scenario of a very lightly doped (10^{15}) GP layer, combined with minimum ILD thickness, provides better decoupling than almost all cases of ILD thickness when no GP is introduced.

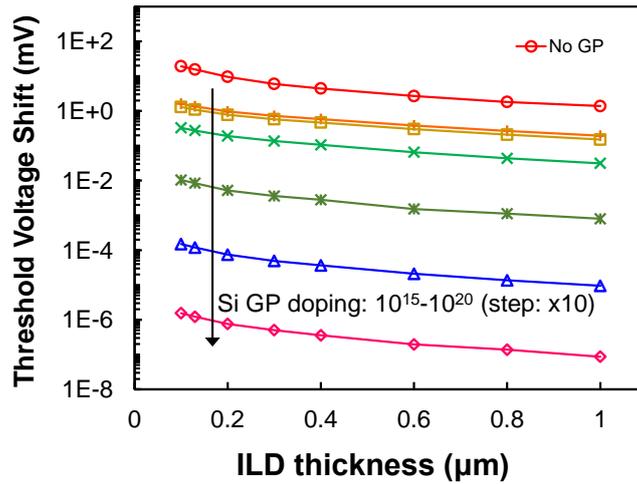


Fig. 4.33 Coupling-induced ΔV_{TH} of the top-tier device to the bottom-tier electrode versus the ILD thickness for different doping concentrations of a silicon inter-tier GP. The insertion of the Si GP (10^{20} cm^{-3}) reduces the DC coupling by $\sim 10^7$

4.2.2.b High-Frequency electric field screening

An inter-tier GP must provide crosstalk isolation between the sequential tiers, especially when heterogeneous integration is desired. High crosstalk immunity is critical to enable the sequential stacking of tiers that integrate noisy logic and sensitive low-noise RF and analog applications. In order to estimate the RF decoupling efficiency of an inter-tier GP, the methodology proposed in [126] and [64] was followed, implementing the simulation setup of Fig. 4.34 (a) and testing various materials for the GP region (SiO₂, Si, PolySi, Copper). The S₂₁ parameter that indicates the forward voltage gain from the in-port (bottom SOI gate) to the out-port (top SOI drain) as represented in Fig. 4.34 (b), was used to analyze the inter-tier crosstalk. The rest of the electrodes have been set to ground (GND).

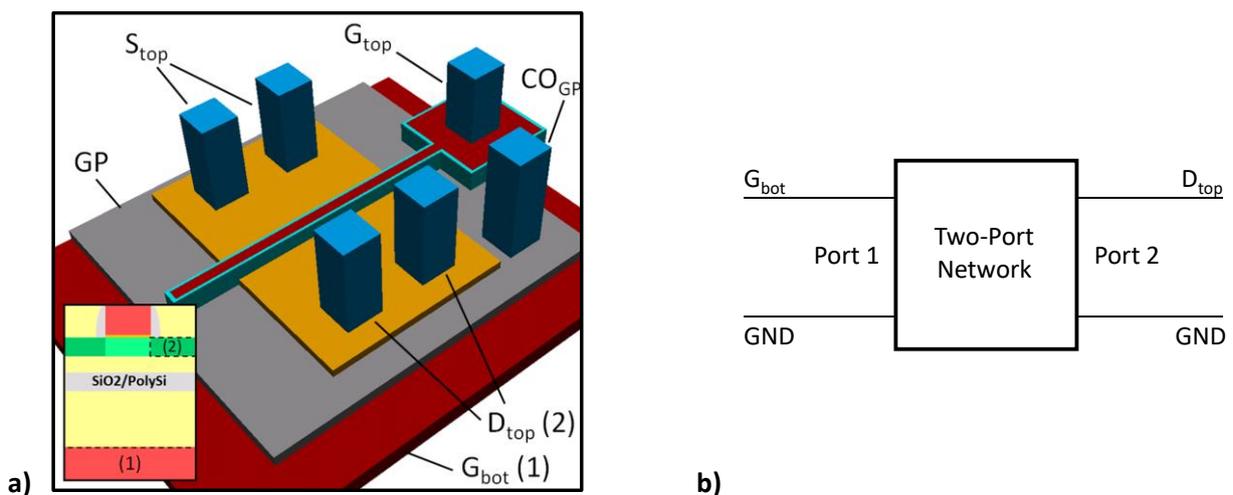


Fig. 4.34 (a) Simulation setup to determine the GP decoupling efficiency for a GP area 2x the top active. (b) Port configuration for the S₂₁ network parameter extraction

Fig. 4.35 shows the TCAD simulation results for the S21 parameter in the frequency range of 1 MHz – 100 GHz for SiO₂ (no GP) and a Si GP. Two biasing conditions were studied for the top-tier device, cutoff (Fig. 4.35 (a)) and saturation region (Fig. 4.35 (b)).

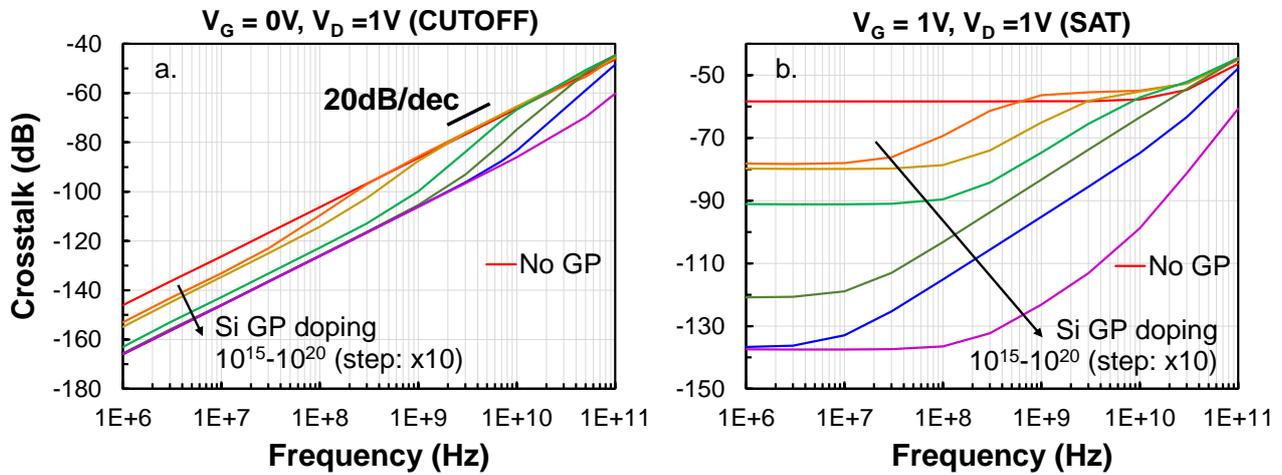


Fig. 4.35 Crosstalk vs. frequency for the top-tier device in cutoff (a) and saturation region (b) and a GP made of silicon.

As observed in Fig. 4.35 (a), the decoupling performance of a silicon GP reveals two significant properties. First, there is an increase of the suppression level with higher doping levels of the silicon GP, a behavior also observed in DC. Considering the semi-conductive nature of silicon, a portion of the electric field manages to get through the GP layer for low frequencies. A second remark is that there is a certain frequency after which the GP layer appears to be capacitively transparent. This can be directly attributed to the resistivity of the inter-tier GP, which is enhanced for higher doping concentration. The frequency beyond which the slope of the S21 parameter gets greater than 20dB/dec can be defined as the maximum decoupling frequency $f_{D,max}$. Fig. 4.36 (a) and (b) mark $f_{D,max}$ for the minimum and maximum doping concentrations respectively of the silicon GP simulated.

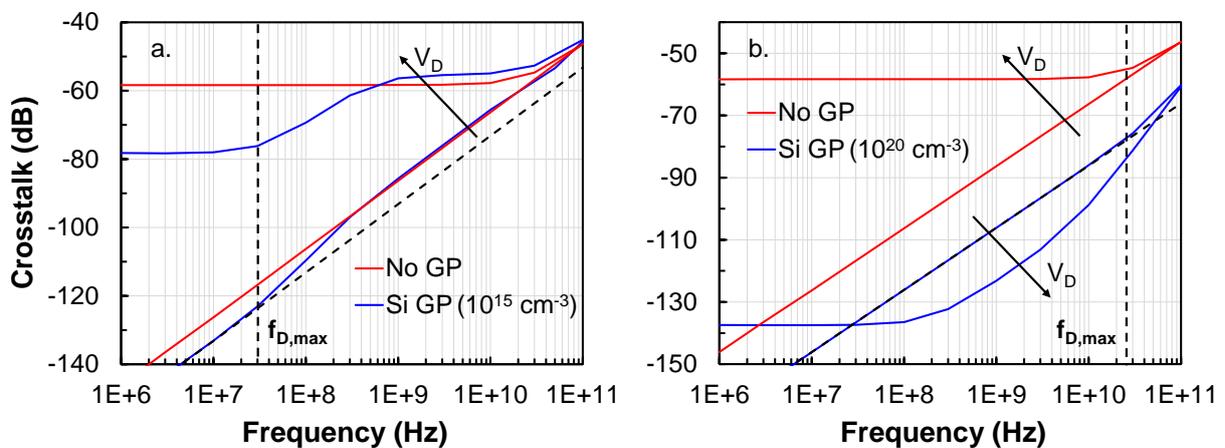


Fig. 4.36 Crosstalk vs. frequency for the top-tier device in cutoff and saturation region for No GP case (red trace) and a silicon GP (blue trace) with doping concentration of (a) 10^{15} cm^{-3} and (b) 10^{20} cm^{-3} . The frequency beyond which the slope of the S21 parameter gets greater than 20dB/dec is defined as the maximum decoupling frequency $f_{D,max}$

When the device is biased in the saturation region (Fig. 4.35 (b)), the inter-tier GP screens out the coupling through the BG transconductance with a suppression level greater than 70dB. The effectiveness of the GP is again determined by the maximum decoupling frequency as defined for the cutoff region of operation.

The validity of TCAD simulations in the high-frequency domain can be confirmed by employing the full-wave EM simulator HFSS, as long as the bias current of the top-tier device is low (cutoff region). For that scope the simulation setup was repeated in HFSS for three cases: the first excluding the GP and filling the area with SiO₂, the second for a silicon GP (10^{20} cm^{-3} n-type doping) and the last for a copper GP. Specifically for the highly doped silicon GP, the material properties had to be defined, assigning a bulk conductivity of $1.23 \times 10^5 \text{ S/m}$ as calculated from the experimental data of Fig. 4.29. The S_{21} parameter results obtained by both HFSS and TCAD are shown in Figure Fig. 4.37 (a) and they are in line. This confirms the validity of TCAD simulations for the high-frequency EM analysis in our structures.

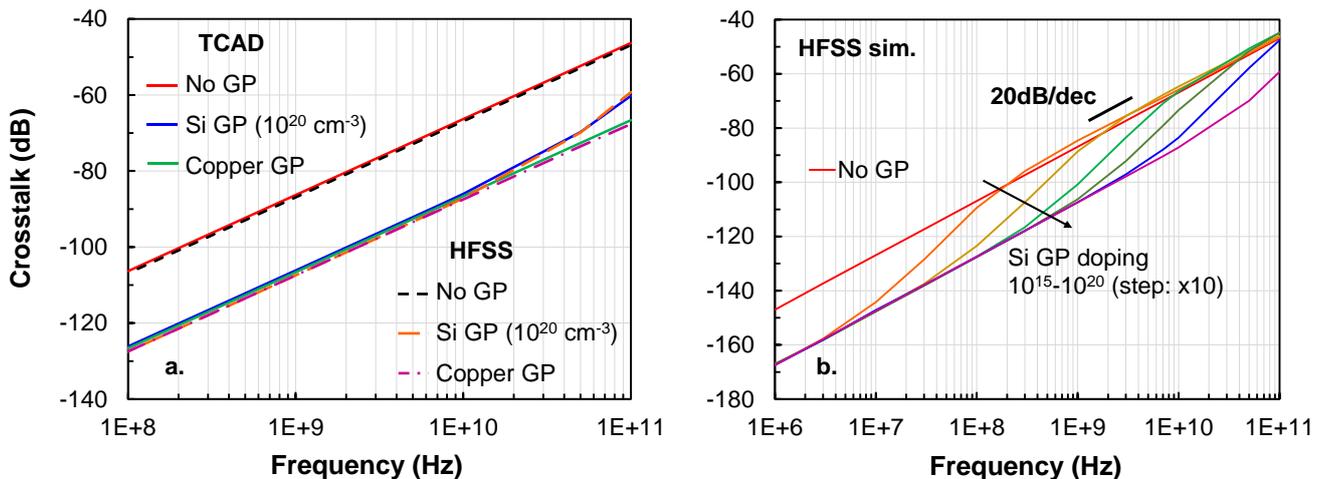


Fig. 4.37 (a) Comparison between TCAD and HFSS simulations to validate the results of the former in the high-frequency domain. (b) The results obtained by TCAD are reproduced calibrating the resistivity of the GP material from data of Fig. 4.29.

On the contrary, calibrating the conductivity of the GP layer in HFSS to account for lower doping concentrations of silicon, the simulation results are shown in Fig. 4.37 (b). Although there is an agreement with TCAD simulations concerning the maximum decoupling frequency as a function of the conductivity, the same is not true for the suppression level. The latter is overestimated in HFSS indicating that it is related to the conduction mechanisms being different in semiconductive materials than metals. Consequently, TCAD is the appropriate tool to further evaluate the properties of the GP.

In the case where the material of the inter-tier GP is polysilicon, its decoupling performance is shown in Fig. 4.38 (a) and (b) for the device being in cutoff and in saturation region respectively, as obtained

by TCAD simulations. It is evident that greater doping concentrations are needed for the GP to function as an effective shielding layer, directly related to the resistivity of polysilicon (Fig. 4.29).

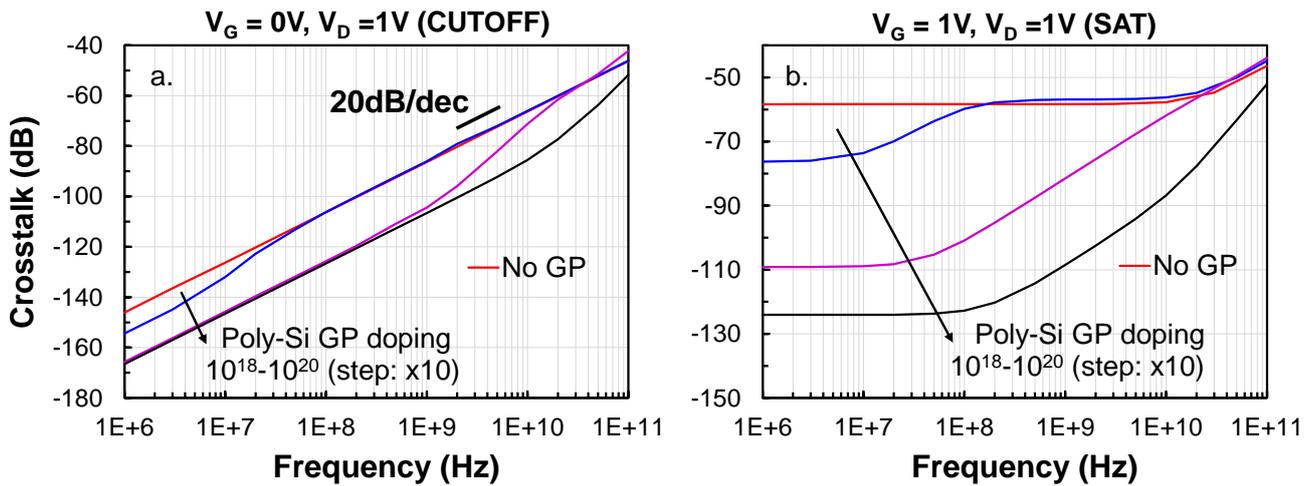


Fig. 4.38 Crosstalk vs. frequency for the top-tier device in cutoff (a) and saturation region (b) and a GP made of polysilicon.

The above extracted results can be visualized with the aid of the cross-sectional electric field contour plots obtained by HFSS simulations for an excitation by a 1GHz signal of 1V amplitude upon the bottom-tier gate electrode. Results without and with an inter-tier n⁺ Si GP (10²⁰ cm⁻³) are shown in the figure. As seen in Fig. 4.39 (b), the GP isolates and attenuates nearly the entire electric field induced from the bottom-tier gate electrode whereas in Fig. 4.39 (a) without a GP a large portion of the induced electric field reaches the upper active region.

On the other hand, it is worth noticing that the cross-sectional magnetic field contour plot in Fig. 4.40 reveals the transparency of the GP to the bottom-tier RF signal. Indeed, the magnetic field penetrates the GP layer reaching the upper active region. In most cases, magnetic field coupling is considered negligible, yet careful layout-aware design techniques must be followed in 3DSI to keep magnetic fields as low as possible.

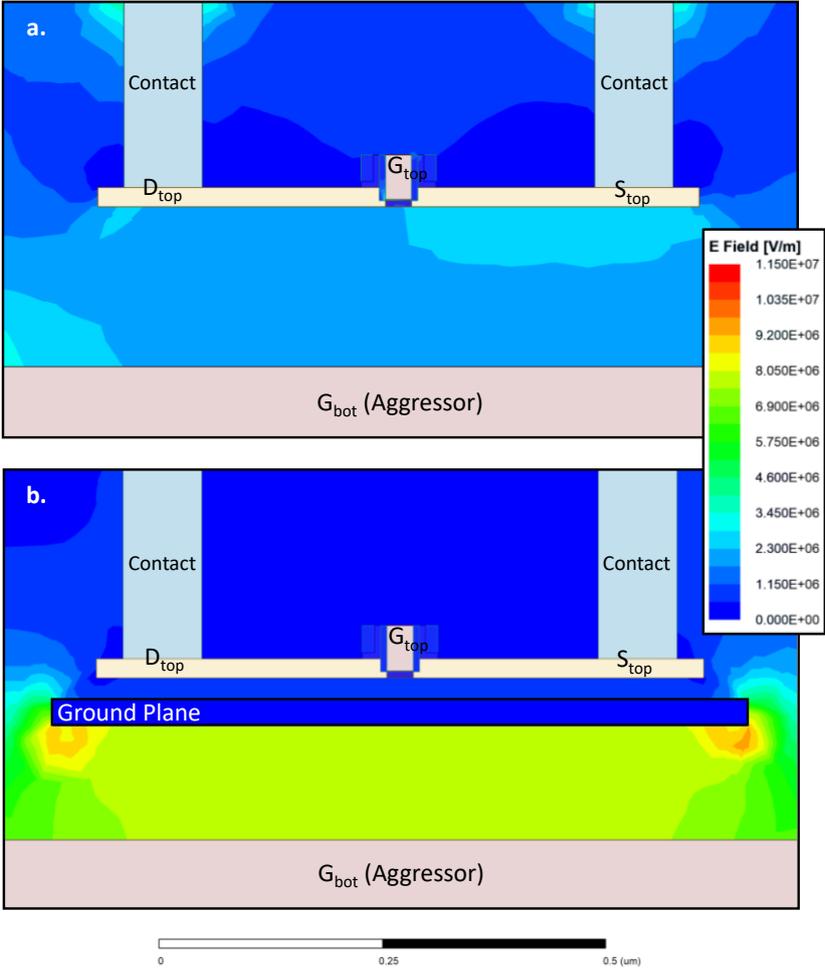


Fig. 4.39 HFSS simulation of electric field contour plots showing the magnitude of electric fields without (a) and with (b) n^+ Si GP. A 1-GHz, 1-V signal is excited upon the lower metal line. As seen on the bottom, the n^+ GP shadows the upper active region from the electric field induced by the metal line.

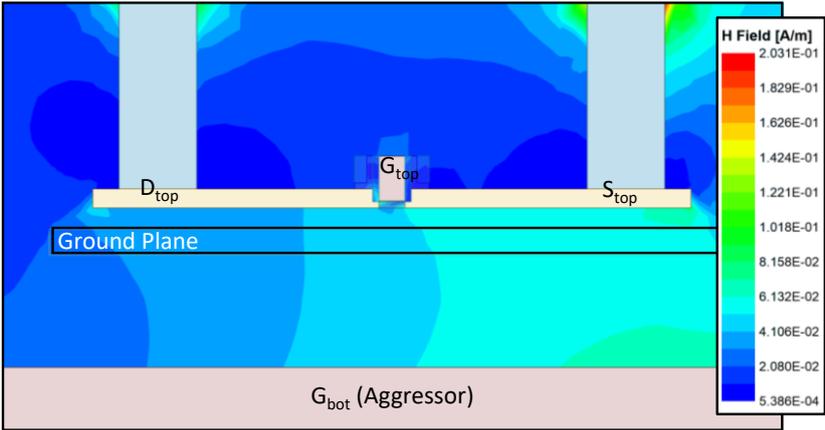


Fig. 4.40 HFSS simulation of magnetic field contour plots showing the magnitude of magnetic fields for a n^+ Si GP. A 1-GHz, 1-V signal is excited upon the lower metal line. The magnetic field penetrates the GP reaching the upper active region.

4.2.2.c Impact of inter-tier GP dimensions and GND contact pitch

Repeating the simulation setup of Fig. 4.34 in TCAD and expanding the GP area with respect to the top tier device active region, the crosstalk suppression was extracted as a function of the well GP coverage of the top tier active device region (Fig. 4.41).

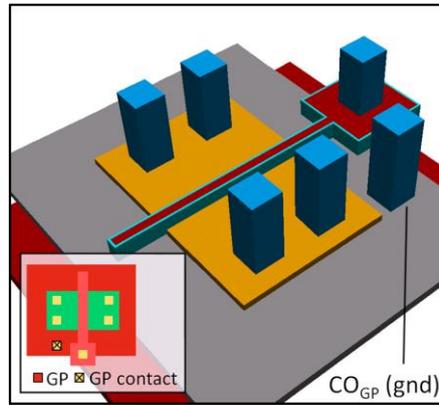


Fig. 4.41 The GP area now is 3x the top active with one GND contact. Inset: Top-tier layout view

As Fig. 4.42 (a) shows, expanding the GP area with respect to the top active region the crosstalk suppression increases and reaches a maximum attenuation level for a certain GP sizing. On the contrary the maximum decoupling frequency has the inverse trend as shown in Fig. 4.42 (b). Thus, the increase of the GP area yields a decrease of the decoupling frequency range, related to the potential attenuation across the GP for one ground (GND) contact on it.

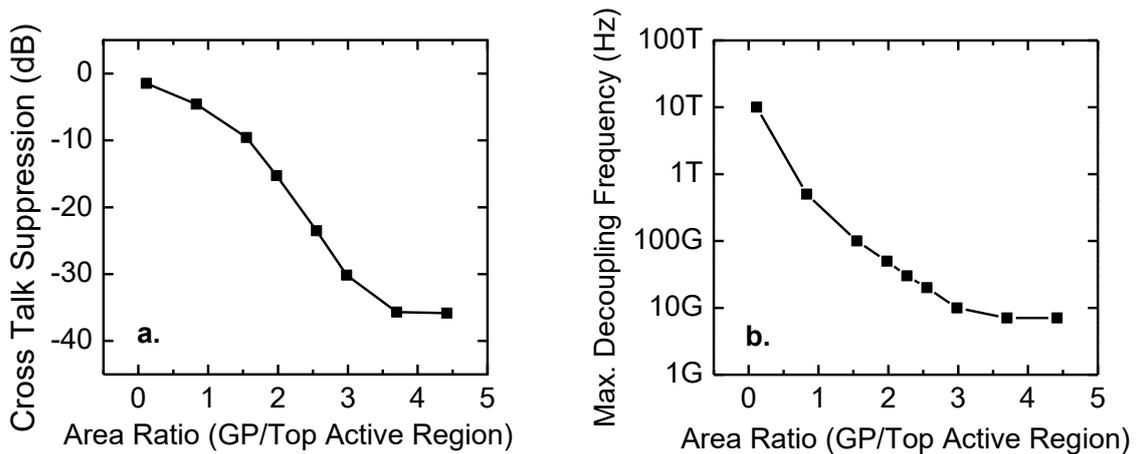


Fig. 4.42 (a) Crosstalk suppression and (b) Maximum decoupling frequency versus the ratio of the inter-tier GP area with respect to the top active region for one GND contact

To address this issue, the number of GND contacts for the GP layer can be increased, so that the TCAD simulation setup becomes that of Fig. 4.43 (a). The results plotted in Fig. 4.43 (b) show how the decoupling band of the GP is enhanced by adding gradually up to 6 GND contacts. As a result,

when expanding the GP area, the density of grounding contacts must be the same in order to retain the decoupling band. Moreover, the addition of GND contacts increases the suppression level as shown in Fig. 4.43 (b). The latter is can be attributed the resistance reduction and also to the Faraday Cage behavior of the structure as the vertical contacts form walls that block the induced fringing electric fields by the bottom-tier electrode.

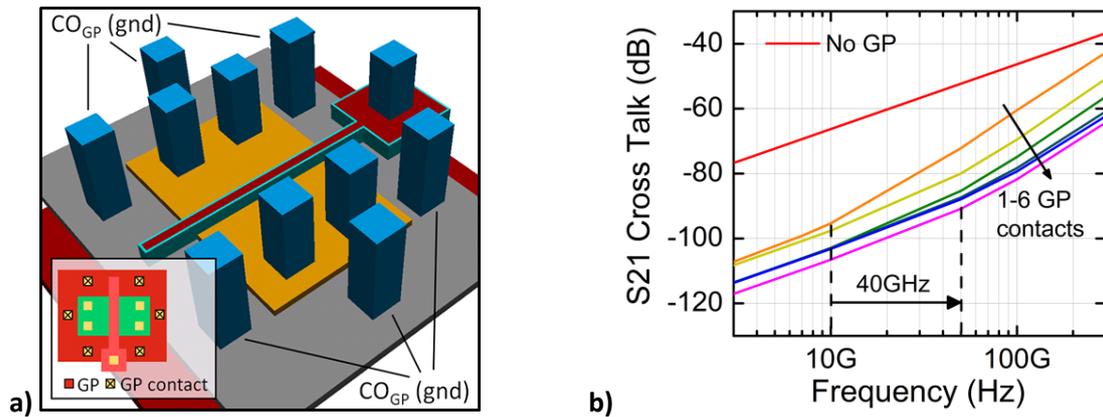


Fig. 4.43 (a) The GP remains 3x the top active and gradually up to 6 gnd taps are added. Inset: Top-tier layout view. (b) Extracted crosstalk vs. frequency. A larger n^+ Si GP needs greater number of GND contacts to maintain the decoupling frequency up to 100GHz

4.2.2.d Inter-tier GP processing challenges and solutions

A polysilicon GP offers several advantages compared to a metallic GP. First, it is compatible in terms of Front-End-Of-Line (FEOL) contamination environment for top MOSFET processing. Second, it offers the possibility of dual doping type to propose several V_{TH} flavors without requiring gate stack engineering or channel doping. With the insertion of the inter-tier GP, the top BOX thickness is in the 20/25 nm range in order to ensure good SCE control for L_G in the 30nm range. The latter enables also the Back-Gate bias flexibility as in planar SOI technology, which allows the designer to modify the threshold voltage dynamically.

However, especially for RF applications a high GP doping level is required. As a consequence, traditional GP doping through the top channel cannot be applied (Fig. 4.44). To increase the GP doping concentration above this limit, the polysilicon needs to be doped directly after its deposition or deposited using in-situ doped epitaxy. With GP direct doping, a doping concentration of 1.8×10^{20} at/cm³ has been reached, enabling one to reach a sheet resistance of 295 Ω /sq for a 34nm-thick polysilicon layer (Fig. 4.29). Therefore, this type of GP answers to all the specifications in terms of doping level and sheet resistance (-20 dB up to 100GHz for 1 GND contact to the GP), as well as thickness (to preserve the 3DCO AR) and FEOL contamination category.

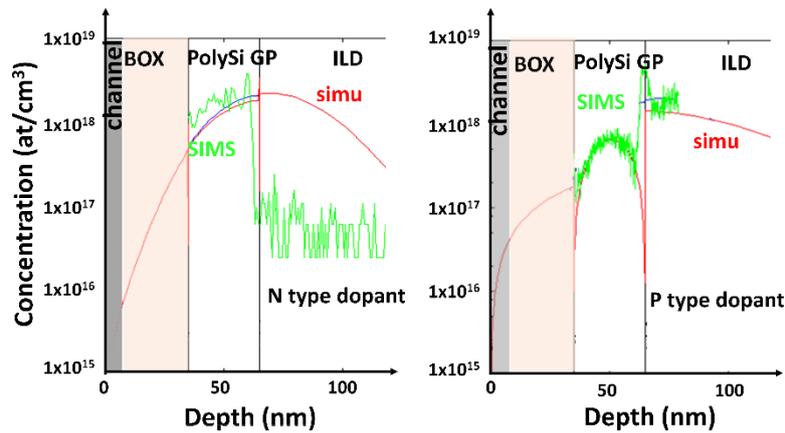


Fig. 4.44 Examples of GP doping conditions (N&P type) through thin channel for SOI devices. GP concentration cannot exceed the $1 \times 10^{18} \text{ at/cm}^3$ in order to avoid top channel parasitic doping [127].

4.3 Conclusion

In this chapter the coupling effects have been further examined at a circuit level, providing significant results regarding the heterogeneous integration of applications in 3DSI. The overall conclusion is that concerning purely digital 3D sequential circuits there is no major coupling between top and bottom tiers, therefore inter-tier isolation methods and techniques are not necessary. However, when it comes to mixed signal and RF applications, further decoupling is needed so that the inter-tier coupling. The latter can be achieved either by process optimization (ILD thickness increase) or proper layout (misalignment of the stacked devices, 3D contact positioning). In order to obtain even greater reduction of the capacitive coupling, an inter-tier decoupling layer (GP) is required. By exploring the decoupling efficiency of semiconductive materials, it is demonstrated that even the lowest doping concentration provides greater static decoupling than a $1 \mu\text{m}$ thick ILD. Consequently, the use of the inter-tier GP maintains the 3DCO AR below 350nm. Concerning high frequency electric field screening, it is shown that the decoupling frequency band of the inter-tier GP is a function of its resistivity, hence for RF applications a high doping concentration is needed. As a consequence, a technological solution is proposed to create experimentally a 34nm-thick polysilicon GP of $1.8 \times 10^{20} \text{ at/cm}^3$ n-doping and $295 \Omega/\text{sq}$ sheet resistance.

CHAPTER 5

ANALYSIS OF COUPLING EFFECTS IN A 3DSI CMOS IMAGE SENSOR

This chapter examines the impact of 3D Sequential Integration on the performance of a CIS partitioned in different tiers. The CIS serves as an ideal case study of coupling effects as it consists of highly sensitive parts to noise and threshold voltage variations, while it presents also an extremely appealing use of 3DSI to the semiconductor industry. The first section of the chapter is devoted on the contemporary trends of CIS and their operating principles. Afterwards, the coupling effects analysis is conducted for a CIS realized in 3DSI technology, analyzing the impact on the most critical figures of merit at pixel level. The goal of this chapter is to ensure the normal operation of the CIS, underlining the potential advantages emerging from the 3DSI technology.

5.1 Introduction

The emergence of user interactive applications is driving the electronics industry towards heterogeneous technologies, in which the analog sensing part is co-integrated with digital processing parts. Key enabler of heterogeneous integration nowadays is the transistor dimensional scaling following Moore's law [2] within the More-than-Moore direction (details in Chapter 1). The latter involves a wide variety of applications that enables the interaction with people and the environment [26].

One of the major driving applications within the More-Than-Moore direction is the CIS, as they require the heterogeneous integration of different technologies. In detail, the sensing interface consists of a photon-to-electron converter (photodiode) in the pixel array, the readout part is made

with the aid of an analog circuit which in turn outputs the sensing information to a digital circuit for processing. Thanks to the development of PPDs, CIS have been dominating the consumer electronics market over the last decade. This breakthrough invention, in conjunction with a lower cost fabrication and higher data rates made CIS more appealing than the Charge-Coupled Devices (CCD) that were the primary choice for imaging applications at earlier years. Moreover, due to the increased commercialization of digital cameras integrated in smartphones, the CIS market grows steadily over the years. As reported by Yole Development [128], the mobile market is the main driver occupying the 69.2% of the CIS Revenue which has increased from \$15.5B in 2018 to \$19.3B in 2019 (Fig. 5.1) and is expected to reach \$24B in 2023.

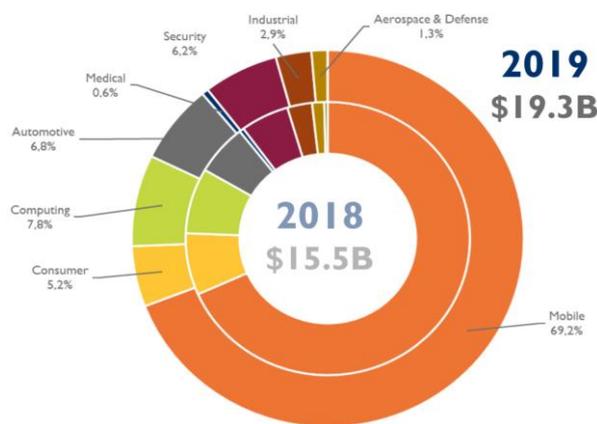


Fig. 5.1 CIS Revenue breakdown by market in 2019 (Courtesy of [128])

5.2 Principles and operation of a CMOS imager

5.2.1 CIS standard architectures

- **Passive Pixel Sensor (PPS)**

The PPS architecture [129] contains passive pixels (without amplification) consisting of only a photodiode for detection and an addressing transistor that acts as a switch for row selection as shown in Fig. 5.2.

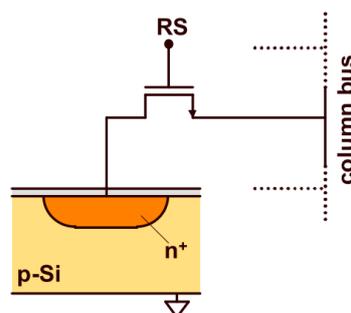


Fig. 5.2 Passive CMOS pixel based on a single in-pixel transistor [30].

This pixel architecture suffers from poor image quality, slow readout, and high KTC noise level resulting from the mismatch between the small pixel capacitance and the large vertical bus capacitance.

- **Active Pixel Sensor (APS)**

The Active Pixel Sensor (APS) [130] was a major improvement to the PPS architecture, adding to every pixel its own in-pixel amplifier. Consequently, the pixel is composed out of a photodiode (PD), a reset transistor (RST) and the source-follower (SF) amplifier as shown in Fig. 5.3. The current source of the source-follower is placed at the end of the column bus. The readout output of an APS is a voltage instead of charge transfer, resulting in a reduced power consumption, random access, and high-speed readout. On the contrary adding a transistor per pixel degrades the Fill-Factor. Furthermore, while it solves a lot of noise issues, the kTC noise generated by the photodiode reset, still remained.

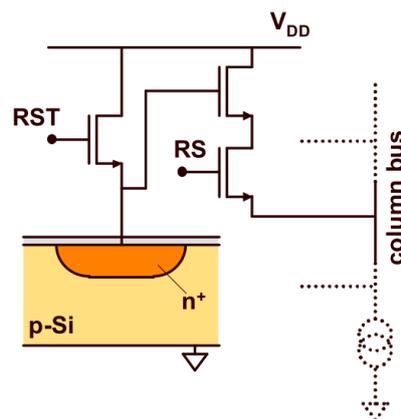


Fig. 5.3 Active CMOS pixel based on an in-pixel amplifier [30].

- **Active Pixel Sensor with Pinned-Photodiode (4T-APS)**

To solve the high reset noise issue of the APS architecture a PPD pixel was introduced [131]. This concept was already popular in CCD image sensors and allowed the pixel to have considerable reduction of dark current, increase of saturation level and improved sensitivity. The architecture, displayed in Fig. 5.4, is the same as APS with the PPD connected to the readout circuit by means of an extra Transfer Gate (TG) and a Sense Node (SN). Furthermore, the 4T-APS architecture offers the possibility of implementing the Correlated Double Sampling (CDS) technique. With this, two sequential measurements of the output voltage are performed, one after reset of the readout node is and a second after the transfer of the integrated charge from the photodiode to the SN. Adding to

the above also the superior noise performance of the PPD [30], the 4T-APS is the preferred choice for CIS pixels nowadays.

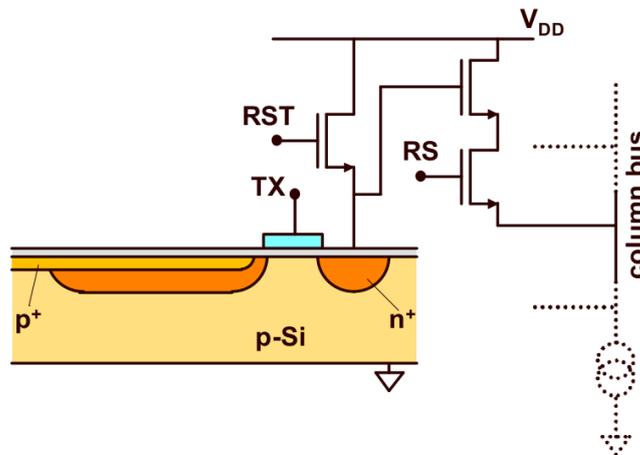


Fig. 5.4 Active CMOS pixel based on an in-pixel amplifier in combination with a pinned-photodiode [30].

➤ Pixel operation

The voltage output of a 3T-APS pixel is presented schematically in Fig. 5.5, where the operation sequence is indicated and consists in three stages:

1. Reset (reset transistor ON): The photodiode voltage is set to a reference voltage V_{ref} .
2. Exposure (reset transistor OFF): Impinging photons decrease the reverse voltage across the photodiode during a fixed integration time (t_{int}).
3. Readout (RS and SF ON): The output voltage level is sampled and further processed at the column.

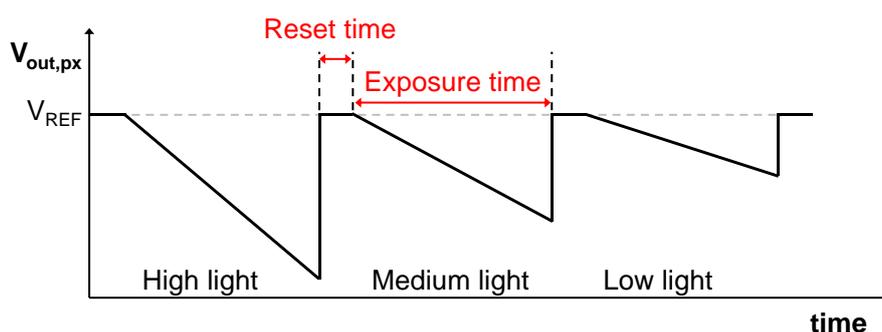


Fig. 5.5 Operation of a 3T-APS pixel

Depending on the integration time, more or less charges are collected at a given time which in turn affects the sensitivity and DR of the sensor.

5.2.2 Pixel metrics

- **Size & Fill Factor (FF)**

One of the main advantages of using CMOS compatible technology is the reduction in size following the scaling law [132]. As shown in Fig. 5.6, due to the shrink of transistor gate length and development of advanced process node, the pixel size was reduced, and the power consumption lowered. Today, commercialized consumer electronics pixels are in the micron range. However, the CMOS process evolution could not be directly used in CIS. The high leakage at small dimension, and the dielectrics used in the BEOL, are some of the reasons that led to the development of a process specific to CIS.

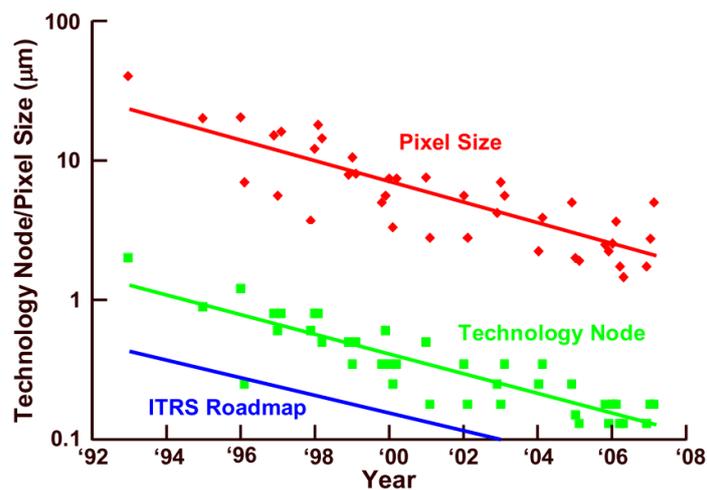


Fig. 5.6 Evolution of pixel size, CMOS technology node used to fabricate the devices and the minimum feature size of the most advanced CMOS logic process [30].

As can be observed from Fig. 5.6, there is a gap between the CIS process and the main stream CMOS process of about three generations [30] however the scaling rate is almost identical.

Also, using Front Side Illumination (FSI) configuration where the pixel is illuminated from the top through the metal layers, with the increase of pixel density the metallization design has become more difficult to deal with. The distance between metal lines is shortened and the light path focused by the micro-lenses might get reflected on the metal lines which causes crosstalk. Therefore, other solutions have been proposed such as integrating waveguides between the microlens and the photodiode to obtain better focus of the light [133], [134]. However, the best solution came as a natural evolution, consisting in Back Side Illuminated (BSI) sensor, where the light is incident on the back surface of the sensor after thinning it down.

The reduction in pixel size results in better spatial resolution at the expense of lower sensitivity. Also, the Signal to Noise ratio (SNR) will be lower due to smaller pixel area and thus less photon absorbed. Reducing the pixel size will also affect the Full Well Capacity (FWC) and thus the DR. All these parameters will be presented in the following sections.

Another important parameter related to the pixel size and scaling is the Fill Factor (FF). FF is defined as the ratio or percentage of photosensitive area to the total pixel area. It represents how much of the total pixel area is used to collect photons, or inversely the area that is shadowed by either transistors or metal lines. A high FF results in a higher sensitivity since more charges are collected by the pixel, therefore it should be maximized. Since the pixel transistors followed the scaling law, their dimensions were reduced which allowed the improvement of the FF. To overcome the reduced FF, micro-lenses are added to the pixel to focus the light on the photodiode area and reduce optical cross talk between pixels.

- **Sensitivity & Quantum efficiency**

The sensitivity of a linear response sensor such as the 3T/4T-APS, is defined as the slope of the transfer function in $V/\text{lux}\cdot\text{s}$ or $e^-/\text{lux}\cdot\text{s}$. It represents the potential change for a given light intensity and integration time. Therefore, it is highly dependent on the Quantum efficiency (QE) of the sensor.

The QE is what quantifies how efficiently the incident photons are collected and converted to electrons. It is wavelength dependent since it depends on the absorption of the photosensitive material, but also accounts for all the optical losses that might occur due to reflection, refraction, and absorption of the incident light before it reaches the photosensitive area. To maximize it, anti-reflecting coating are used, and the stack between the surface of the sensor and the photodiode is optimized to avoid reflections at the interfaces. Also, the reflections on the metal lines must be minimized when using FSI. For example, using micro-lens greatly improves the QE and thus the sensitivity of the sensor. Using BSI improves the QE by avoiding these reflections.

- **Dynamic range**

The dynamic range (DR) quantifies the range of light intensity detectable and measurable by the sensor. It is calculated as the ratio between the highest detectable signal (S_{max}) and the lowest one (S_{min}), which is essentially the noise floor. Therefore, it can be expressed as

$$DR = 20 \log \frac{S_{max}}{S_{min}} \quad (5-1)$$

A high DR is desired to ensure image quality at the low and high end of the light intensity. The highest detectable signal is limited by the Full Well Capacity (FWC) and pixel saturation. A common linear pixel sensor exhibits a DR of about 60dB.

- **Conversion gain**

The conversion gain (CG), measured in V/e-, characterizes the charge-to-voltage conversion. Hence, a high CG increases the sensitivity especially at low light. It is expressed as:

$$CG = \frac{\Delta V_{out}}{N_e} \quad (5-2)$$

where ΔV_{out} is the pixel output ($V_{out,int} - V_{out,ref}$) as a response to the number N_e of electrons in a single packet. The latter depends on the quantum efficiency and the photon flux. Equation (5-2) can be also expressed as:

$$CG = \frac{q}{C_{SN} + C_P} \quad (5-3)$$

with C_{SN} being the SN capacitance and C_P is any additional parasitic capacitance. Experimentally, the CG is measured by considering the photon shot noise and dividing it by the mean output signal of the pixel.

- **Full well capacity**

The Full Well Capacity (FWC) is a metric of the charge amount which can be detected before the sensor saturates, measured in number of charges, and determines the DR of the sensor. When the noise is not considered, the number of charges that the well can contain, can be roughly approximated by

$$FWC = q \cdot C_{PD} \cdot V_{PD} \quad (5-4)$$

where C_{PD} is the photodiode capacitance, V_{PD} the applied voltage across it and q the elementary charge. From (5-4) it is evident that increasing the capacitance increases the number of charges that can be collected. However, increasing the capacitance will also decrease the CG. The higher is the FWC the higher is the DR, however, the loss in sensitivity due to the reduction in CG will decrease the

range at the low intensity end. This results in the well-known DR/sensitivity tradeoff. Also, with the reduction of pixel size, the capacitance of the photodiode is also reduced, which negatively affected the FWC.

- **Signal-to-Noise Ratio (SNR)**

It represents the ratio of the useful signal to the undesirable noise signals and essentially defines the image quality. Thus, it must be as high as possible, either by increasing sensitivity and CG, or by decreasing the noise floor. For the SNR evaluation, the main noise parameters in a pixel are explained in the following section.

5.2.3 Pixel noise parameters

The noise sources in an image sensor can be divided into the following categories:

- Temporal noise: this includes photon shot noise, dark current shot noise (Q_{shot}), amplifier flicker $1/f$ noise, and reset kTC noise (Q_{reset}).
- Spatial noise: mainly Fixed Pattern Noise (FPN) (QFPN) that includes Dark FPN, the FPN of the in-pixel SF and the column FPN.
- System noise: more related to readout ($Q_{readout}$), such as line noise and crosstalk, as well as ADC quantization noise.

The total pixel noise is the sum of the mentioned components and can be expressed as:

$$Q_n = Q_{shot} + Q_{reset} + Q_{readout} \quad (5-5)$$

The FPN contribution (QFPN) is not included in (5-5) since it can easily be corrected using CDS techniques. As illustrated in Fig. 5.7, dark current noise is dominant at low illumination, while the shot noise, particularly the photon shot noise that increases with the signal, is dominant at higher light intensities. We will define in more details the major contributor to pixel noise in our case: dark current, reset kTC noise, and FPN.

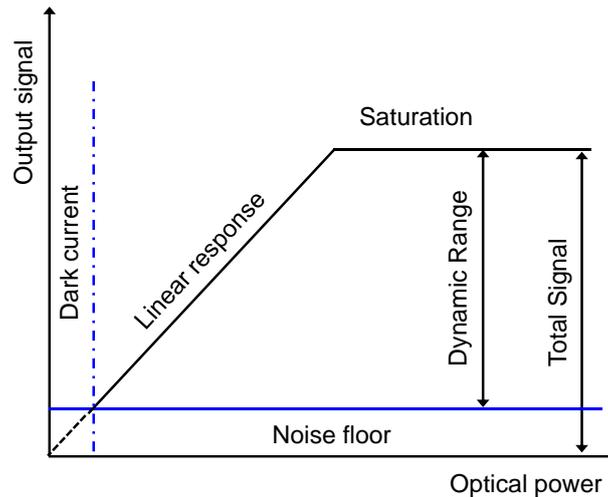


Fig. 5.7 Output voltage curve of a CMOS APS for a given integration time with the main noise components

- **Dark current noise**

Dark current noise is defined as the unwanted output signal when no light is present at the photodiode, hence it is result of a thermal generation process and not of a photo-generation one. The major causes of dark current are the defects generated in the lattice during fabrication, that generate traps at the interfaces (Si/SiO₂), the recombination due to drift in depletion region, and diffusion in the quasi-neutral regions of the diode. Dark current has always been a noise source difficult to deal with, since its underlying physics are not fully understood to date. It depends primarily on temperature variations due to its thermal SRH (Shockley-Read-Hall recombination) component.

To account for the dark current, pixels that are shielded from the incident light (dark pixels), are implemented to measure the dark current variation and apply a correction algorithm to the image. Another way to reduce the dark noise is to subtract a dark frame from the following frames. This takes into account the dark signal dependence on integration time and gain, however not considering the temperature increase. The progress achieved by the contemporary process technologies and the development of different techniques to reduce it, enable the reduction of the dark signal component. The introduction of the PPD where the pinning layer passivated the interface states [135], drastically improved the presence of dark current noise. Nowadays, it is possible using advanced nodes, to achieve dark current noise in the range of tens of pA/cm² for pixels smaller than 4μm [136].

- **Reset or kTC noise**

This type of noise is the result of the thermal noise generated at the reset transistor that switches the capacitive node. Concerning the 4T-APS, this node is the SN. As explained in Chapter 2, the voltage noise that a resistive element generates is defined as:

$$v_{R,n} = \sqrt{4 \cdot k \cdot T \cdot R \cdot \Delta F} \quad (5-6)$$

where R the resistance in Ohms, k is the Boltzmann constant, T the temperature in Kelvin and ΔF is the noise bandwidth

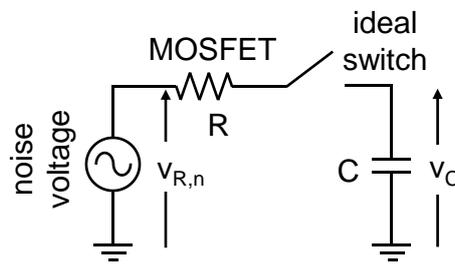


Fig. 5.8 Equivalent circuit of the reset transistor connected at the SN.

Considering the equivalent circuit of Fig. 5.8, it consists a low-pass filter with cut-off frequency

$$f_c = \frac{1}{2\pi RC} \quad (5-7)$$

and transfer function given by

$$H(\omega) = \frac{1}{1 + j\omega RC} \quad (5-8)$$

Consequently, the total noise voltage generated across the capacitor will be

$$v_{C,n}^2 = \int_0^{\infty} 4kRT \cdot |H(\omega)|^2 d\omega = 4kRT \cdot \frac{\pi}{2} \cdot \frac{1}{2\pi RC} = \frac{kT}{C} \quad (5-9)$$

with C being the integration node capacitance. It can also be measured as an amount of charge in Coulomb as:

$$Q_{C,n} = \sqrt{kTC} \quad (5-10)$$

It is evident that kTC noise decreases with temperature. To reduce $Q_{C,n}$, the capacitance must be reduced (opposite for $v_{C,n}$). However, the CG increases by reducing the capacitance. Besides that, a lower capacitance value increases the necessary supply voltage, so it is eventually a tradeoff. In the

4T-APS the reset noise can be almost completely canceled with the introduction of the PPD and the use of CDS.

- **Fixed Pattern Noise (FPN)**

The fixed pattern noise is a spatial noise resulting from the mismatch between pixel parameters due to process variations. It results either in a gain or offset variation. For a standard APS circuit, it can be divided as:

1. Pixel FPN, which includes FPN due to photodetector variation (eg. area, C_{PD} , etc.), and the amplifier variation (V_{TH} , W/L ratio, etc.)
2. Column FPN resulting from column current bias variations.

The offset FPN can be evaluated by measuring the variance of the output voltage under uniform illumination condition (including dark) without taking into consideration the temporal noise and is not signal dependent. On the other hand, the gain increases with the signal since it is defined by the variance of the pixel gain multiplied by its photo response. FPN is given in a percentage of the output voltage swing or a percentage of the full well capacity. The gain FPN which includes DSNU (dark signal non-uniformity) and PRNU (pixel response non-uniformity) is more complex to address than the offset FPN. The offset FPN can easily be removed using CDS techniques, while the gain FPN can be limited by using process integration techniques to reduce its dominant sources, such as dark current.

5.2.4 Process integration optimization

- **Back-Side Illumination (BSI)**

The BSI integration scheme consists in flipping the sensor so that the light will be incident directly on the photodiode without going through the BEOL of the pixel. The process was initially developed in the 70's, intended to specific application that required higher QE such as astronomy imaging. It became mainstream for high-end consumer applications, as the pixel size decreased below $2\mu\text{m}$, resulting from the mobile phone market demand where higher resolution at the same sensor size is required [137]–[139]. When Front-Side Illumination is used, the optical path will include the total thickness of the BEOL. The reflection on the metal lines induced losses and crosstalk between pixels. The optimization of the FSI BEOL techniques [140] were no longer enough to adjust to the scaling of the CMOS technology and reduction in pixel pitch, making the distance between

metal lines shorter and shorter. Therefore, BSI came as a natural solution to increase the QE, but also to allow the use of more advanced standard BEOL technologies. The industries developed foundry compatible processes, and thanks initially to the contribution of Sony and Omnivision, this technology is now mainstream. The first to implement BSI in mobile phone cameras were OmniVision in 2007 [141]. Nowadays, more than half of the mobile phone market utilize BSI integration [128].

- **Three-dimensional integration**

Within the More-Than-Moore context, 3D CIS enable the possibility of smarter and more advanced sensors through the co-integration of different blocks (Analog, Digital, RF) in various tiers. Today industry has shifted to the 3D stack process integration which allows the integration of the CMOS processing part on top of the pixel enabling the possibility of using more advanced technology nodes for the processing circuit. Since 2010, the trend is the combination of BSI and 3D stack to reach ultimate performance maintaining a small pixel size. Therefore, combined with BSI, it allows the addition of more functionalities without degrading the fill factor.

Nowadays heterogeneous integration of different processing blocks is the main target for a 3D stacked CIS. In 2017, Sony announced their 3-level 3D stack image sensor [142] composed of the back illuminated pixel array, a DRAM level, and the digital processing level. The proximity of the DRAM allows fast processing and fast frame rate. Millet et al. [28] recently presented a vision chip in a 3D stacked BSI implementation with an in-focal-plane matrix parallel communication, exhibiting a frame rate of 5500 frames/s and demonstrates heterogeneous processing features on captured images.

Although 3D stacking technologies have been predominantly used for 3D CIS nowadays, constraints of traditional 3D stacking alignment capabilities forbid the more aggressive pixel miniaturization required for future generations of CIS [30], [31]. This drawback can be overcome by using 3DSI which is the leading pathway for pixel partitioning with pitch in the sub- μm range. Another great opportunity that 3DSI offers is the outstanding high-density of the 3D contacts between the tiers (up to 10^8 3D via/ mm^2) which enables the partitioning of different processing blocks with high connectivity and low latency (Fig. 5.9). Taking that into consideration, 3DSI offers not only the possibility to integrate dense logic and memory layers but also heterogeneous technologies like MEMS/NEMS for tight coupling of sensing and computing [32].

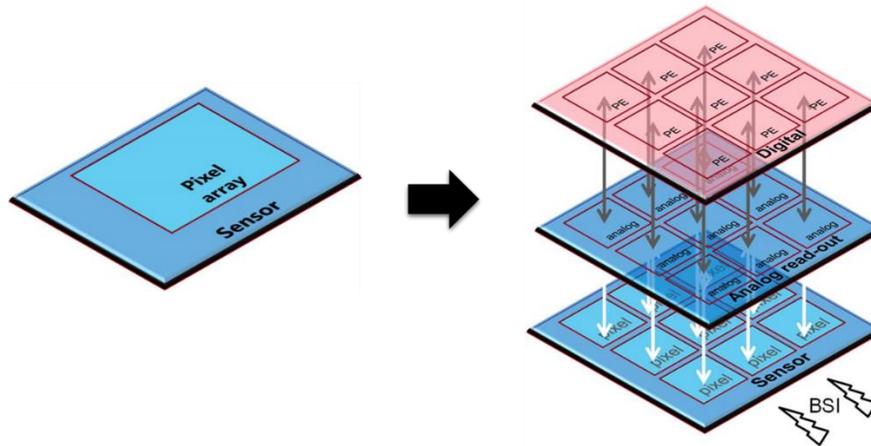


Fig. 5.9 Realization of a CIS with planar (left) and three-dimensional partitioning (right)

While offering great opportunities in the CIS domain, 3DSI deals with many challenges at the moment. As already mentioned in the previous chapters, the major challenge for the sequential processing is the limited TB for the fabrication of the stacked devices. To date, LT devices have been successfully processed for LV [19] as well as HV [102] applications. The feasibility of Back-Illuminated CIS with miniaturized pixels realized in 3DSI has been investigated in the work of Coudrain et al. [143] in which the 3D partitioning of the CIS at the pixel level led to an increase of the photodiode area by 44% for a $1.4\mu\text{m}$ pitch.

5.3 Inter-tier Coupling at Device Level

As studied in the previous chapters, the electrical coupling between the sequential tiers due to the ILD that acts as a BG oxide for the top stacked devices is of great concern in 3DSI. Consequently, if no inter-tier GP is introduced, the top devices are asymmetrical SOI MOSFETs, sensitive to the bottom tier electrode voltage variations.

The scope of this section is to analyze the immunity of HV analog devices with $V_{DD}=2.5\text{V}$ in the top tier when the bottom tier electrode voltage variations can go up to $V_{DD}=2.5\text{V}$, for a BSI 3D pixel. With the aid of TCAD simulations, a comparison against the impact of temperature variation on the top-tier stacked devices will be used to draw conclusion on the necessity to introduce an inter-tier GP.

5.3.1 Simulation Setup

For the TCAD simulation setup we consider the cross-section illustrated in Fig. 5.10 (a). It consists of a 4T pixel partitioned in two tiers, the PPD and the TG at the bottom whereas the readout

transistors are placed at the top. The two tiers are separated by a 200nm thick ILD, and a 3D contact connects the SN with the drain of the RST transistor and the gate of the SF. In the most critical case of inter-tier coupling, each one of the top devices is placed above the TG electrode as shown in Fig. 5.10 (b).

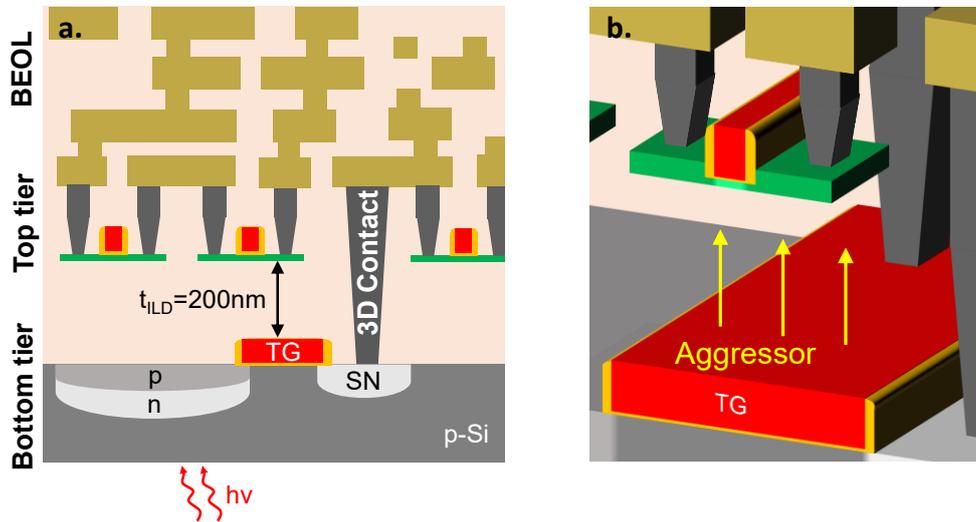


Fig. 5.10 Cross-section of 4T pixel, partitioned in 3DSI. (b) In the most critical case, the top device is placed right above the TG electrode carrying a voltage that can go up to $V_{DD}=2.5V$.

5.3.2 Impact on electrical parameters

The TG placed at the bottom tier toggles from 0V to V_{DD} and vice versa. This voltage node is coupled via a capacitive path to the exposed top device channel resulting in a shift of the I_D-V_G characteristics, as seen in Fig. 5.11 (a). This is a non-linear effect that becomes more evident in the sub-threshold region and slightly decreases to a fixed value when the device operates in strong inversion [144].

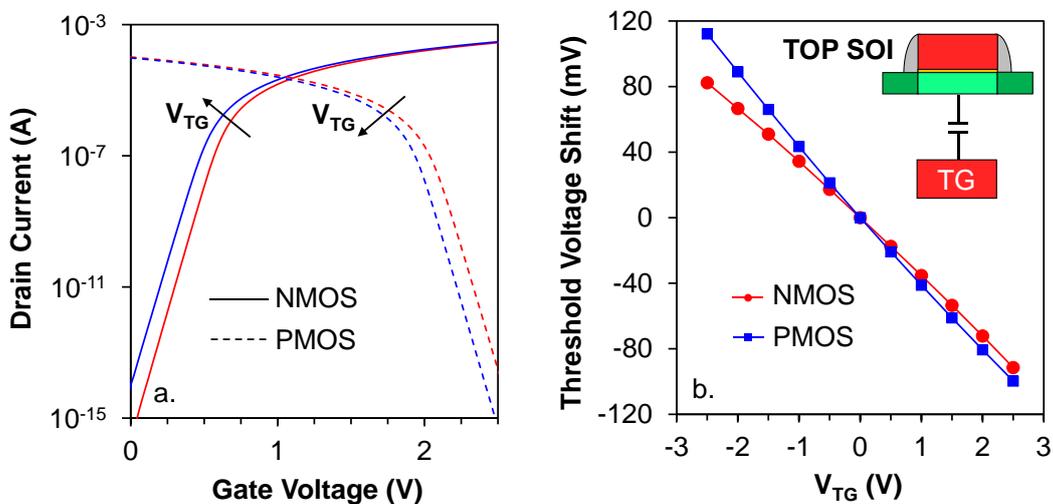


Fig. 5.11 (a) Impact of TG coupling ($V_{TG}=0-2.5V$) on the input characteristics for NMOS and PMOS devices (b) Extracted threshold voltage shift versus TG voltage bias (-2.5V to 2.5V with 0.5V step).

Extracting the threshold voltage shift induced by the TG voltage bias sweep from -2.5V to 2.5V (Fig. 5.11 (b)), the charge-coupling factor was obtained, 35mV/V for NMOS and 42mV/V for PMOS.

To assess the impact of the TG coupling on the top tier device, we chose to compare it against the temperature dependence of the device electrical characteristics. Unlike the capacitive coupling, the effect of temperature has a complex behavior depending on the gate voltage V_G . As seen in Fig. 5.12 (b), increasing the temperature of the device from 253 K to 353 K (-20 °C to 80 °C) – extended temperature range in commercial electronics – we observe an increase of the subthreshold conduction current as well as a decrease of the saturation current while there is a gate voltage around threshold for which the drain current remains constant. This behavior is attributed to the increase in carrier concentration with temperature for low gate bias, as opposed to the decrease in carrier mobility for high gate bias [145]. At a specific V_G these two mechanisms are counterbalanced resulting in a Zero Temperature Coefficient (ZTC) point.

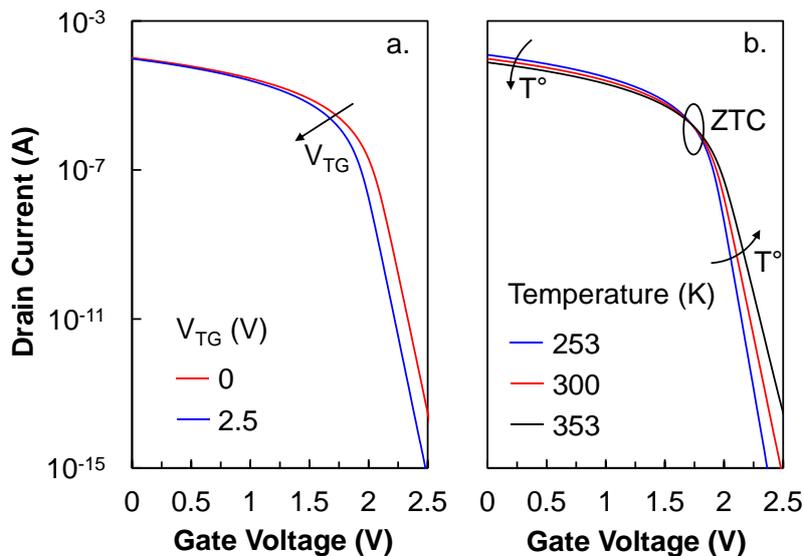


Fig. 5.12 Impact of coupling (a) and temperature variation (b) on the top-tier SOI input characteristics

The impact of both coupling and temperature variation can be expressed through the change in the device electrical parameters, i.e. the Threshold Voltage (V_{TH}), OFF-state current (I_{OFF}) and the ON-state current (I_{ON}). Fig. 5.13 and Fig. 5.14 show the comparison of V_{TH} and I_{OFF} , I_{ON} respectively, for the two effects. It is evident that they are in the same order of magnitude whereas the slight prominence of the coupling impact regarding the Threshold Voltage Shift is due to the decrease of the temperature impact near the ZTC point at V_{TH} . For switch transistors the most important

parameter is the leakage current I_{OFF} which is shifted significantly with the TG coupling. The latter can be critical for memory blocks placed at the top-tier above the TG.

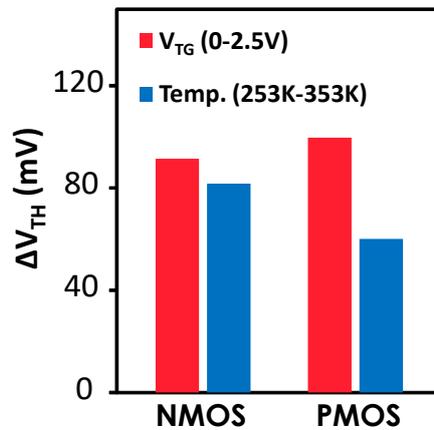


Fig. 5.13 Comparison of the V_{TH} variation of the top-tier NMOS and PMOS due to TG coupling or due to a 100K temperature increment.

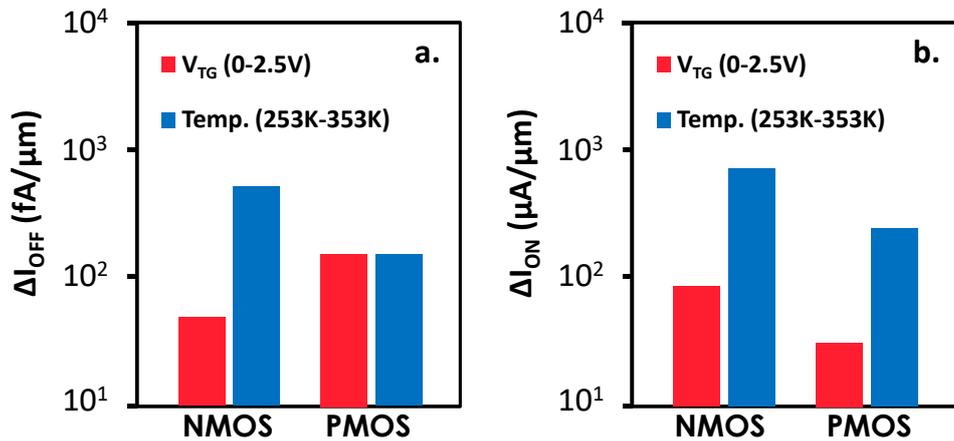


Fig. 5.14 Comparison of the I_{OFF} , I_{ON} variation of the top-tier NMOS and PMOS due to TG coupling or due to a 100K temperature increment.

5.4 Inter-tier Coupling at Pixel Level

5.4.1 Read-out circuit block and pixel metrics

Our 4T pixel contains the NMOS-TG as well as the RST, SF and RS in a PMOS circuit configuration shown in Fig. 5.15 (a). The SF is an amplifying transistor connected in common drain configuration with an approximate gain of unity. Fig. 5.15 (b) shows the chronogram of the 4T pixel read-out operation. During the read-out, the SN is reset, then the TG is switched ON allowing photo-generated electrons to diffuse to the SN. The accumulated electrons cause a voltage drop at the input of the SF resulting in nearly the same voltage drop at its output.

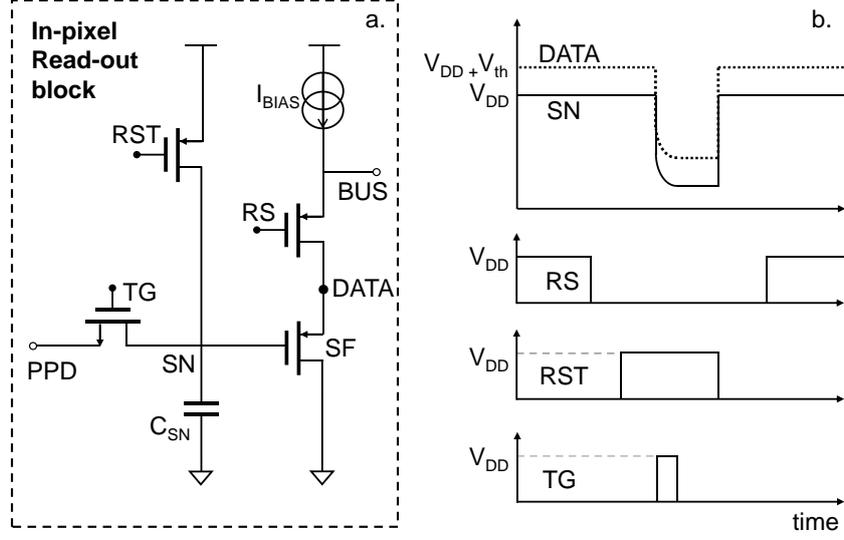


Fig. 5.15 4T pixel read-out circuit (b) Chronogram of a read-out cycle.

The CG evaluates the efficiency of this mechanism and for a 4T-APS is given by [146],

$$CG = \frac{qG_{SF}}{C_{SN} + C_{GD} + (1 - G_{SF})C_{GS}} \quad (5-11)$$

where q is the elementary charge, G_{SF} is the SF gain, C_{SN} is the sum of parasitic capacitances at the SN node and C_{GS} , C_{GD} are the gate to source and gate to drain capacitances of the SF.

The gain G_{SF} of the SF is expressed as:

$$G_{SF} = \frac{g_{m,SF}}{g_{mS,SF}} = \frac{1}{n} \quad (5-12)$$

where $g_{m,SF}$ and $g_{mS,SF}$ is the gate and source transconductance respectively and n is the body factor of the SF. In the case where the BG of the SF can be tied to the source then the gain is approximately equal to unity, otherwise it is process-dependent and is given as $n=1+r$, where r is the charge-coupling factor of the top-tier SOI. As the ILD thickness is increased, n approaches unity. In our case, for the r values extracted previously, the gain G_{SF} of the NMOS device is 0.97 and for a PMOS one is 0.96.

The cutoff frequency of the SF is given by [146]:

$$f_c = \frac{g_{m,SF}}{2\pi \cdot C_{out,SF} \cdot G_{SF} \cdot (C_{SN} + C_{GD} + C_{GS})} \quad (5-13)$$

where $C_{out, SF}$ is the capacitance seen at the source of the SF, that is the column-level capacitance if there is no other stage in between.

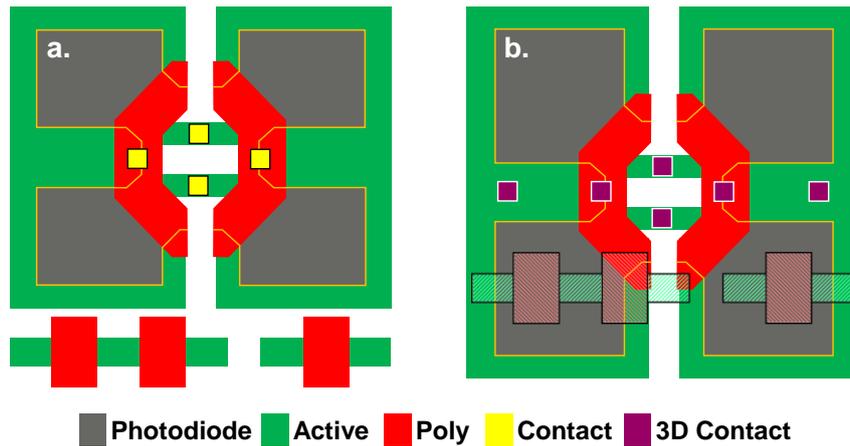


Fig. 5.16 Shared pixels at photodiode layer: 2D (a.) vs. 3D (b.). Photodiode area (in grey) is increased by 44% when the three readout transistors are placed at the top tier. Courtesy of [4].

Parasitic extraction was performed concerning a single-tier (2D) and a two-tier layout (3D) implementation of our pixel as illustrated in Fig. 5.16, to evaluate the impact of the latter on CG and f_c . The parasitic capacitances contributing to C_{SN} , C_{GD} , C_{GS} , $C_{out,SF}$ and also the CG are presented in Table 5.1. As evaluated, the sum of C_{SN} and C_{GD} as well as C_{GS} are slightly enhanced by 48aF and 44aF respectively. An even smaller increase of 10aF for the column-level capacitance is obtained. This shows a negligible difference in the conversion gain and the AC response of the 3D pixel (yielding in a ΔCG of $0.377\mu V/e^-$ and a Δf_c of 0.244Hz) compared to the one processed in planar SOI technology as long as the BOX (equivalently the ILD in 3DSI) thickness is the same. The low 3D impact on the CG also implies that noise performance will not be deteriorated.

Table 5.1 2D vs 3D parasitic capacitances & CG

	$C_{SN} + C_{GD}$ [fF]	C_{GS} [fF]	$C_{out,SF}$ [pF]	CG ($\mu V/e^-$)
2D	4.432	1.093	2	34.319
3D	4.48	1.137	2	33.942

5.4.2 Impact of TG coupling on pixel electrical parameters

Fig. 5.17 shows the voltage at the output of the in-pixel SF transistor versus the number of photo generated electrons at the SN for the voltage bias limits of the bottom tier TG (0V-2.5V). The CG is the slope of the latter and is not altered with the TG coupling. The constant vertical shift can be considered as an offset that can be easily corrected during the read-out process.

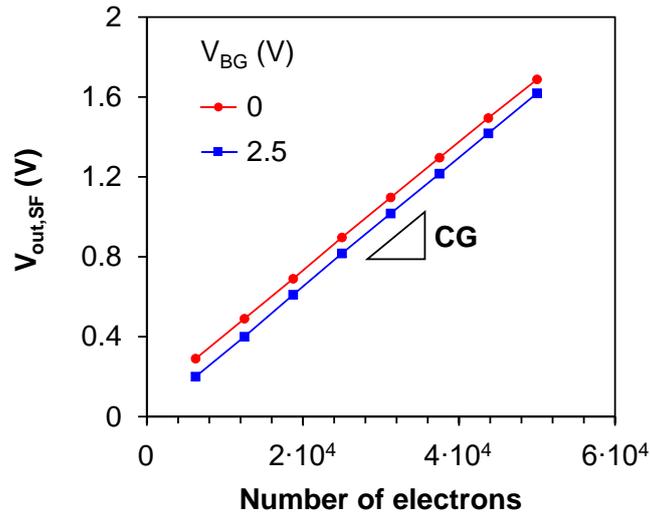


Fig. 5.17 Output voltage of the in-pixel SF transistor versus the number of photo generated electrons at the SN for the voltage bias limits of the bottom tier TG (0V-2.5V). The slope gives the CG that is not altered with the TG coupling.

To evaluate the impact of the TG coupling on the pixel readout operation, we simulated a readout cycle as the one shown in Fig. 5.15 (b). We examined two cases, one where the SF is placed at the top-tier above a TG which belongs to the same pixel as in Fig. 5.18 (a), and one for which the SF is placed above a TG of an adjacent pixel, illustrated in Fig. 5.18 (b). In the first case the TG switches ON during the transfer of e^- from the PPD to the SN and the sampling is thus performed at t_1 , t_2 without resulting in a readout error. In the second case, where the TG switching is not synchronized with the top-tier SF device, the sampling value may be compromised due to the TG switched ON.

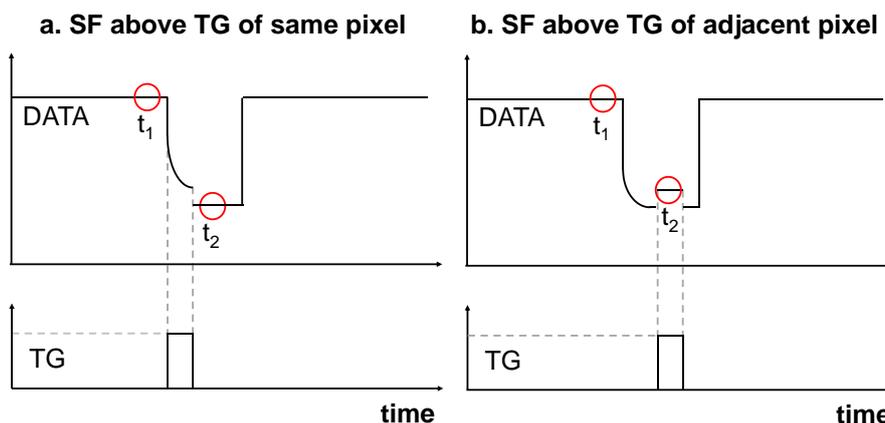


Fig. 5.18 For TG corresponding to the SF above, the TG switches ON during the transfer of e^- from PPD to the SN. The sampling is thus performed at t_1 , t_2 without read-out error. (b) In the scenario of a TG not corresponding to the SF above, the sampling can contain erroneous value due to TG coupling.

Fig. 5.19 (a) shows the readout error resulting from the non-corresponding TG-SF case versus the number of photo generated electrons at the SN, for three bias currents of the SF, from low to

medium. As expected, a low SF bias current at low light intensity can cause the highest readout error at the output of the SF.

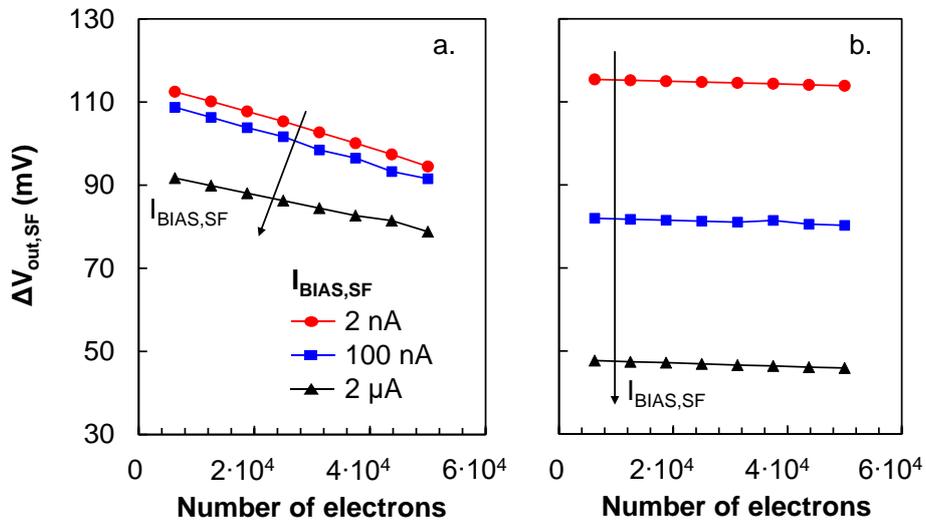


Fig. 5.19 Read-out error of the in-pixel SF transistor versus the number of photo generated electrons at the SN resulting from (a) the SF-TG coupling of Fig. 5.18(b), and (b) the sensor temperature variation.

To assess the strength of this error we compared it with the readout error caused by temperature variation (253 K - 353 K), with the impact of the latter shown in Fig. 5.19(b). As observed, the temperature effect is in the same order of magnitude and for a low SF bias current it can even be worse than the coupling effect. However, because it remains constant with the light intensity it is easier to compensate for it later in the circuit.

5.4.3 Inter-tier GP necessity

The decoupling efficiency of an inter-tier GP between sensitive tiers in 3DSI has been thoroughly examined in §4.2.2, where it has been shown to reduce the vertical static coupling by five orders of magnitude. The necessity for an inter-tier GP integration results from the specifications targeted for each application and is eventually a trade-off between the process complexity and the inter-tier coupling sensitivity.

Fortunately, in a typical rolling readout, each row of a pixel array is enabled sequentially, so there is no overlapping of timing diagrams for adjacent pixels. Consequently, there is no probability of a readout error due to TG coupling. Moreover, the Correlated Double Sampling (CDS) stage that exists commonly after the readout circuit, eliminates possible readout errors. This means that even with no intermediate isolating Ground Plane, the 3DSI CIS readout is immune to inter-tier coupling effects. However, if additional blocks are intended to be placed above the photodiode area, like in-

pixel frame memory, where the leakage current is a significant parameter, then an inter-tier GP is mandatory.

5.5 Conclusion

A simulation study of coupling-induced effects in a PMOS pixel realized in 3DSI has been presented. At a device level it is shown that the impact of the TG coupling can result in an alteration of the electrical parameters as significant as the one resulting from a temperature variation of 100 degrees, especially for switch transistors for which leakage is a critical parameter. Regarding the in-pixel SF transistor at circuit level, it was shown that there is negligible impact on the conversion gain and the AC performance due to the 3DSI compared to a planar one. Furthermore, the SF-TG coupling can result in a readout error only when the SF is placed above a TG of an adjacent pixel, therefore not synchronized with the pixel readout. However, in a typical rolling readout this is not possible due to the sequential pixel activation. Moreover, possible readout errors are eliminated if a CDS stage is included after the readout circuit. Consequently, we demonstrated that despite the strong electrical coupling and consequently high ΔV_{TH} ($\sim 100\text{mV}$) for top-tier devices, there is an inherent readout error immunity of a sequentially integrated 3D CIS.

CHAPTER 6

PARASITIC EXTRACTION AND MODELING OF COUPLING EFFECTS IN 3DSI

In this chapter, the results of parasitic extraction on 3DSI structures comprised of stacked devices is presented. In detail, the coupling capacitances that are formed between different electrodes are analyzed. Since the precision of TCAD simulations has been validated against experimental results in Chapter 3, the present analysis has been conducted solely with the aid of TCAD tools. In addition, a comprehensive modeling approach of inter-tier coupling effects between active devices in 3DSI is presented. Our modeling approach predicts accurately the impact of layout effects on the inter-tier capacitive coupling between active devices concerning a wide range of geometries along with several top/bottom device configurations. Consequently, it can help facilitate the analysis of complex and large-scale monolithic 3D circuits with SPICE tools and merge the gap between pre- and post-layout simulations.

6.1 Parasitic extraction of lumped coupling elements in 3DSI

Prior to modeling the coupling effects between active devices in 3DSI, one must identify victim-aggressor pairs. Each device is considered as a black box with its terminals (D, G, S, B) exposed. As a consequence, for the coupling elements extraction between two stacked devices (Fig. 6.1 (a)), the intrinsic capacitances of each device (Fig. 6.1 (b)) shall be neglected.

From the previous chapters it has been proven that quasi-static methods are valid for the analysis of the inter-tier coupling effects between active devices. Additionally, the validity of TCAD simulations in the high-frequency domain has been confirmed against full-wave simulations by HFSS.

As a result, the parasitic extraction at the device level will be accomplished in this chapter with the use of TCAD (Silvaco ATLAS) and quasi-static field solver (Silvaco CLEVER).

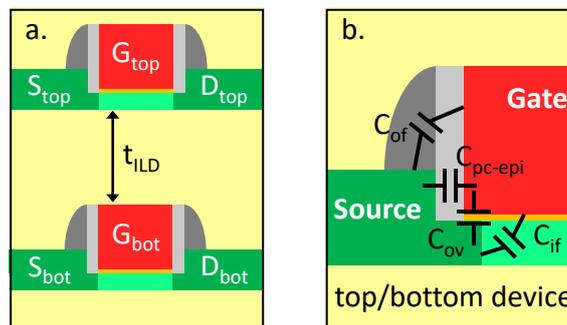


Fig. 6.1 (a) Stacked device structure in 3DSI (b) Zoom-in view of a top/bottom-tier device illustrating its intrinsic trans-capacitances.

Although in the conventional parasitic extraction schemes, TCAD is used for the FEOL evaluation (device trans-capacitances including semiconductor material, not dependent on layout) and field solvers for the BEOL (from contact to top back-end level, layout dependent metal/insulator capacitances), here the line between the two is blurred. For that reason, both tools will be used in conjunction. The parasitic elements model the transfer of energy between the devices and can be divided in:

- Capacitors for the capacitive coupling modeling
- Mutual inductances for the inductive coupling modeling

Since in §3.3.1.a it has been proven that inductive coupling can be considered negligible in monolithic 3D circuits, the extraction and modeling of mutual inductances will be excluded from our analysis.

6.1.1 Definition of coupling capacitances in 3DSI

A 3D illustration of two stacked devices in 3DSI is presented in Fig. 6.2(a), where the coupling capacitances between the electrodes of the two devices are highlighted. For the simplicity of the analysis, the symmetry of the structure has been exploited (source/drain electrodes can be used interchangeably), hence the coupling capacitances can be defined as seen in the schematic cross-section of Fig. 6.2 (b).

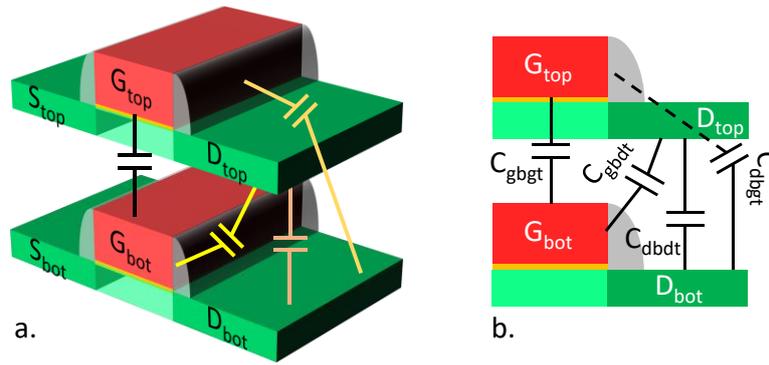


Fig. 6.2 (a) Schematic 3D illustration of 2 stacked devices in 3DSI (b) respective cross-section cut by the symmetry axis

For the bottom-tier device, none of the coupling capacitances is depended on the respective bias, as long as its body potential is shielded by its polarized electrodes. Consequently, for the stacked top-tier device the bias-dependency of the capacitances needs to be investigated. Considering at first stacked devices without relative misalignment, Fig. 6.3 demonstrates C-V TCAD simulations results, sweeping the top-tier device gate voltage in the range from -1V to 1V.

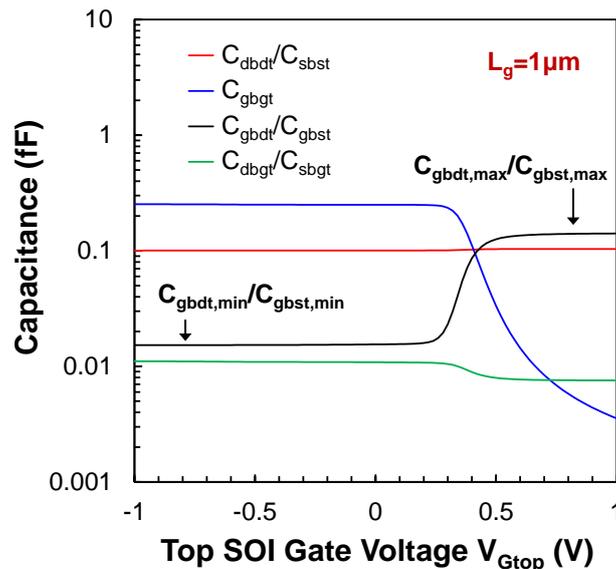


Fig. 6.3 Gate bias dependency of coupling capacitances for the stacked top-tier device with $L_g=1\mu\text{m}$.

The coupling capacitances between the electrodes of the stacked devices can be analyzed as follows:

- C_{dbdt}/C_{sbst} : This capacitance can be considered as a bias independent parallel plate capacitance between the bottom-tier drain to the top-tier drain electrode. It is related to the drain diffusion length but not the gate length.

- C_{gbgt} : This is also a parallel plate capacitance between the bottom-tier gate to the top-tier gate electrode, but it varies with the top-tier gate voltage. It dominates over the others since it is gate area depended, thus it further increases for long devices. As observed from Fig. 6.3, this capacitance has a fixed value below threshold, while above V_{TH} it is screened by the inversion charge formed in the top-tier channel.
- C_{gbdt}/C_{gbst} : This is the most critical coupling capacitance since it is responsible for the back-gate effect of the top-tier device. In the absence of the inversion charge within the top-tier device channel, the capacitance has a minimum value $C_{gbdt,0}/C_{gbst,0}$ due to the fringing electric field between the bottom-tier gate and the top-tier source/drain. For $V_{Gtop} > V_{TH}$, the formed inversion channel maximizes the capacitance value ($C_{gbdt,max}/C_{gbst,max}$) so that we can define the effective oxide capacitance as:

$$C_{ILD,eff} = (C_{gbdt,max} - C_{gbdt,min}) + (C_{gbst,max} - C_{gbst,min}) \quad (6-1)$$

- C_{dbgt}/C_{sbgt} : The fringing fields created by the bottom-tier drain/source electrodes reach the top-tier device gate electrode through its depleted channel forming C_{dbgt}/C_{sbgt} respectively for $V_{Gtop} > V_{TH}$. However, above threshold these fringing fields are screened by the inversion channel, thus this capacitance is limited.
- Lastly, there is an additional capacitance C_{dbst}/C_{sbdst} not shown in Fig. 6.3. This capacitance forms between the bottom-tier drain and top-tier source electrode and is extremely small since it is screened by the electric field of the adjacent electrodes.

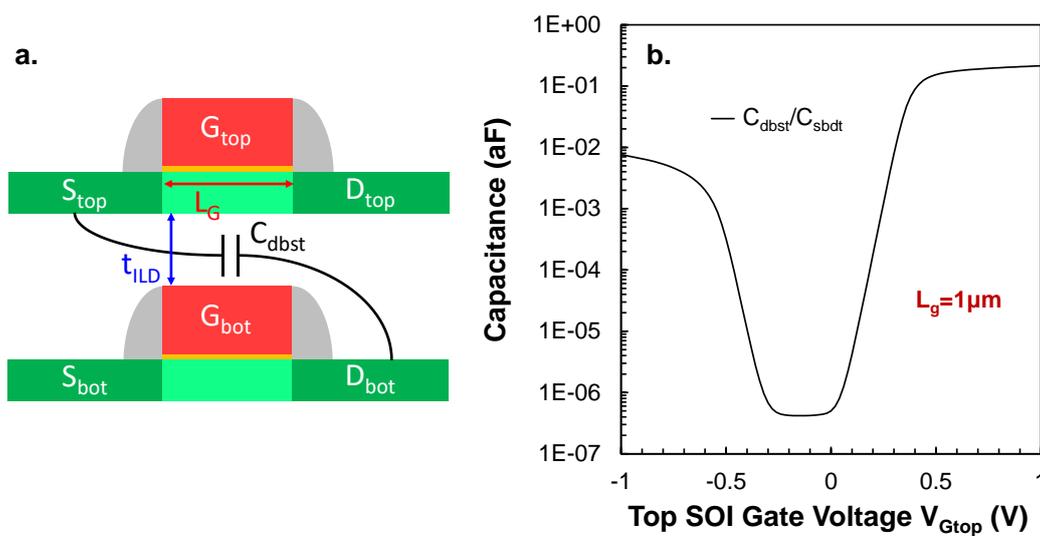


Fig. 6.4 Schematic illustration of the coupling capacitance C_{dbst}/C_{sbdst} along with its geometric dependencies (b) C_{dbst}/C_{sbdst} versus the top-tier device gate voltage

Moreover, it depends on the diagonal of the structure (Fig. 6.4 (a)) and thus proportional to $\approx \sqrt{L_G^2 + t_{ILD}^2}$, so that it is even more limited when the gate length increases. TCAD simulations reveal the variation of C_{dbst}/C_{sbdst} with the top-tier device gate voltage and the results are shown in Fig. 6.4 (b).

To further analyze the C_{gbdt}/C_{gbst} capacitance of the top-tier device, Fig. 6.5 shows the potential contour plot of the stacked devices when the gate of the bottom-tier device is at $V_{DD}=1V$. The OFF-state ($V_{G_{top}} = 0V$) and the ON-state ($V_{G_{top}} = V_{DD}$) of the top-tier device are demonstrated in Fig. 6.5 (a) and Fig. 6.5 (b) respectively. Concerning the OFF-state, the C_{gbdt}/C_{gbst} capacitance can be decomposed in an outer fringe component $C_{gbdt,of}/C_{gbst,of}$ as well as an inner fringe component $C_{gbdt,if}/C_{gbst,if}$ as noted in Fig. 6.5 (a). On the contrary, when the top-tier device is ON, the inner fringe component of C_{gbdt}/C_{gbst} is screened by the inversion channel and the $C_{ILD,eff}$ capacitance is formed.

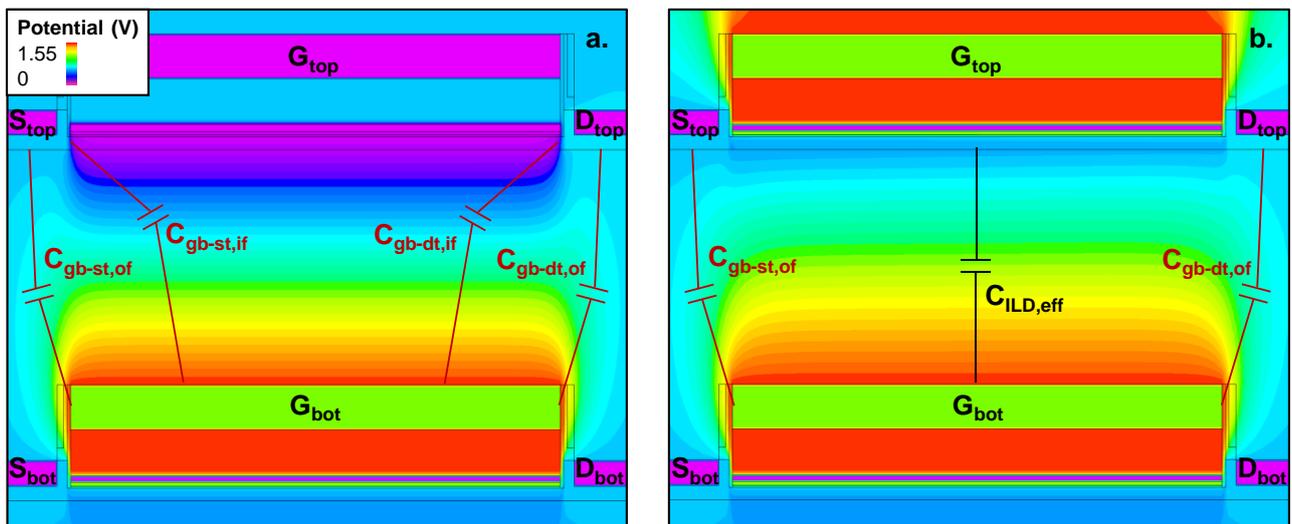


Fig. 6.5 C_{gbdt}/C_{gbst} components in (a) OFF-state of the stacked top-tier device and (b) in the ON-state

Moving on to short channel devices and repeating the TCAD simulations, the coupling capacitances versus the top device gate voltage are shown in Fig. 6.6. Now the dominant coupling capacitance is C_{dbdt} . The drastic reduction of the gate area is reflected in the values of C_{gbgt} and the maximum values of C_{gbdt}/C_{gbst} , hence C_{gb-cht} . On the other hand, an increase can be observed for C_{dbst}/C_{sbdst} with the downscaling of the gate length, however this capacitance remains very weak. Ultimately, for the rest of the coupling capacitances there is no major difference.

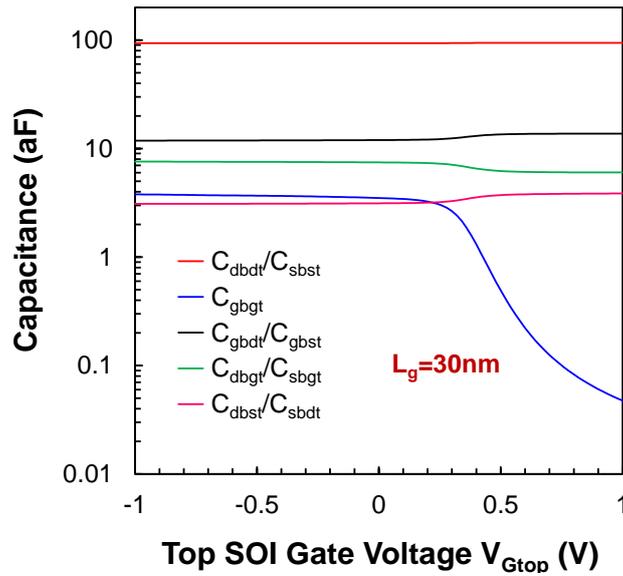


Fig. 6.6 Gate bias dependency of coupling capacitances for the stacked top-tier device with $L_g=30nm$

6.1.2 Effect of 3D contacts on coupling capacitances

So far, the coupling capacitances have been analyzed without the impact of the 3D layout. The influence of 3D contacts on each coupling capacitance shall be investigated in this section. Fig. 6.7 recalls a 3DSI structure comprised of 2 stacked devices under a specific layout configuration.

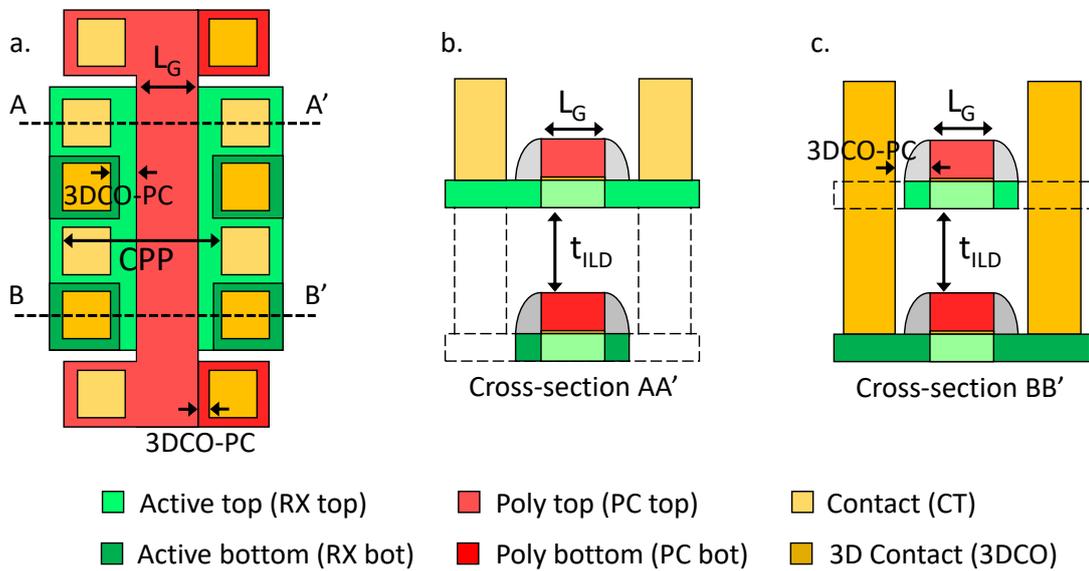


Fig. 6.7 (a) Schematic top layout view of two stacked devices with the respective cross-sections (b) AA' and (c) BB'.

In particular, Fig. 6.7 (a) demonstrates the top layout view whereas the respective cross-sections A'A and B'B of that are shown in Fig. 6.7 (b) and (c).

It is worth mentioning that this 3D layout configuration represents just a critical case study where the impact of 3D contacts can be examined, however it is not restrictive and a designer can in

fact exploit a variety of possible configurations. Over and above, this layout configuration can provide the minimum form factor of the stacked structure as the distance of 3D contacts to the gate of the top-tier device (depicted in Fig. 6.7 (c) as 3DCO-PC) has the minimum value allowed by the technology. The latter is defined by 65nm-node design rules for the structures analyzed in this work.

The analysis can be carried out by splitting each capacitance into different components, based on the layout layer levels (RX, POLY, CT, 3DCO), as follows:

- **Bottom-tier Drain electrode to Top-tier Drain Electrode Capacitance (C_{dbdt})**

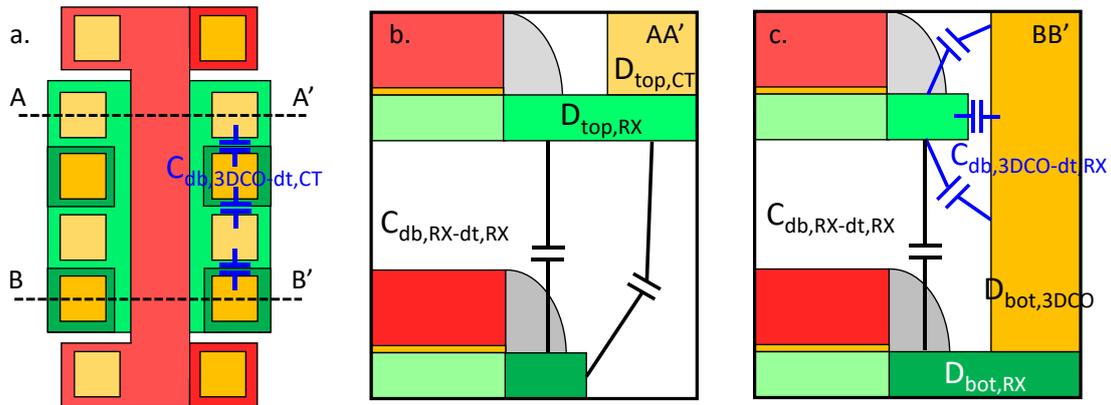


Fig. 6.8 C_{dbdt} decomposition

This capacitance can be divided into the components depicted in Fig. 6.8. In detail, $C_{db,RX-dt,RX}$ is the capacitance between the bottom-tier device drain diffusion and the top-tier device drain diffusion, as analyzed in the previous section. It is mainly a parallel plate capacitance that depends on the ILD thickness and the RX layout pattern. The 3D contacts that extend vertically from the BEOL to the bottom active tier, create the additional capacitances $C_{db,3DCO-dt,RX}$ and $C_{db,3DCO-dt,CT}$. The former is the capacitance between the 3D contact and the top-tier device drain diffusion whereas the latter is the one between the 3D contact and the top-tier device drain contact. Therefore, the overall contribution of the 3D contact to C_{dbdt} is

$$C_{db,3DCO-dt} = C_{db,3DCO-dt,RX} + C_{db,3DCO-dt,CT} \quad (6-2)$$

- **Bottom-tier Gate electrode to Top-tier Gate Electrode Capacitance (C_{gbgt})**

Fig. 6.9(a) shows the top layout view of the structure while Fig. 6.9 (b) and Fig. 6.9 (c) show the respective cross-sections AA' and BB'. The component of C_{gbgt} consisting the bottom-tier gate poly to top-tier gate poly capacitance ($C_{gb,POLY-gt,POLY}$) can be distinguished in Fig. 6.9 (b) and Fig. 6.9 (c).

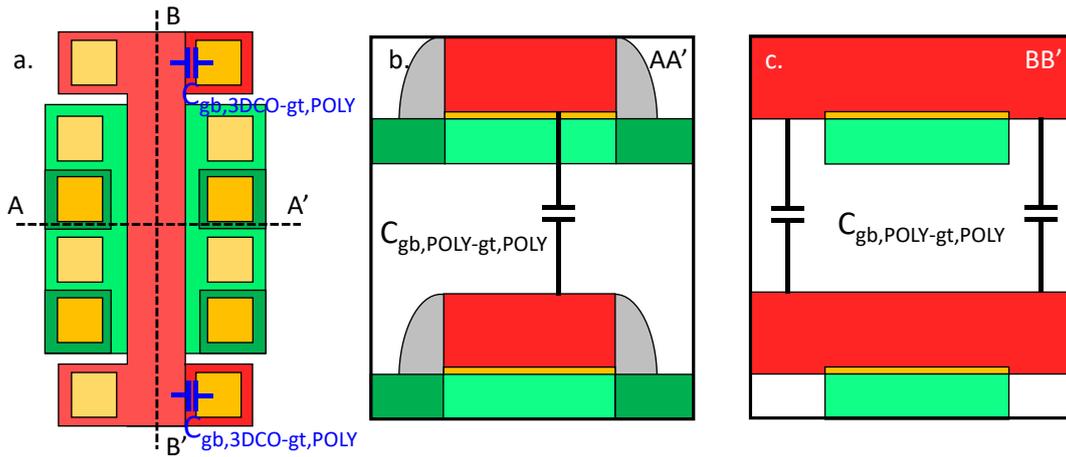


Fig. 6.9 C_{gbgt} decomposition

It is a parallel plate capacitance and depends on W_G , L_G as described in the previous section. The 3D contact passing nearby the top-tier gate poly forms the additional capacitance component $C_{gb,3DCO-gt,POLY}$.

- **Bottom-tier Gate electrode to Top-tier Drain Electrode Capacitance (C_{gbdt})**

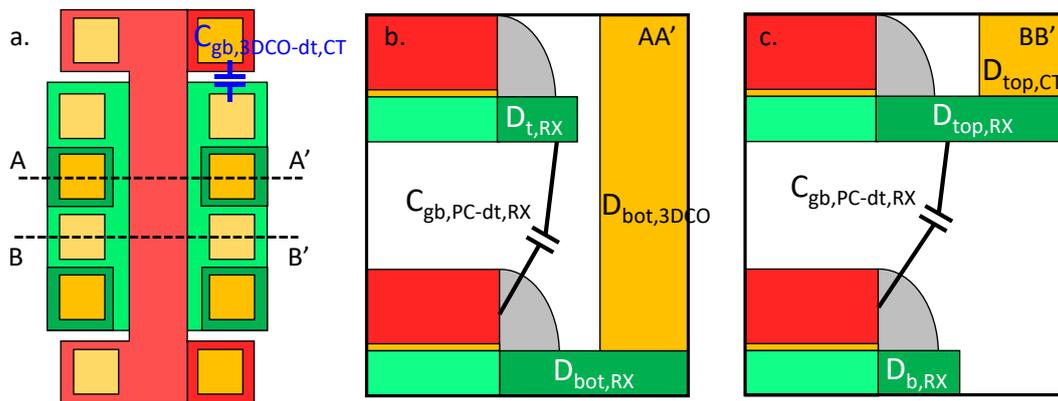


Fig. 6.10 C_{gbdt} decomposition

The C_{gbdt} capacitance components are depicted in the cross-sections AA' (Fig. 6.10 (b)) and BB' (Fig. 6.10 (c)) of the top-view layout (Fig. 6.10 (a)). The capacitance component of C_{gbdt} between the bottom-tier gate poly to the top-tier drain diffusion consists $C_{gb,PC-dt,RX}$ and is a fringe capacitance under zero relative misalignment of the stacked devices. The other capacitance component of C_{gbdt} is the one between the 3D contact on the bottom-tier device gate and the contact on the top-tier device drain, namely $C_{gb,3DCO-gt,POLY}$.

- **Bottom-tier Drain electrode to Top-tier Gate Electrode Capacitance (C_{dbgt})**

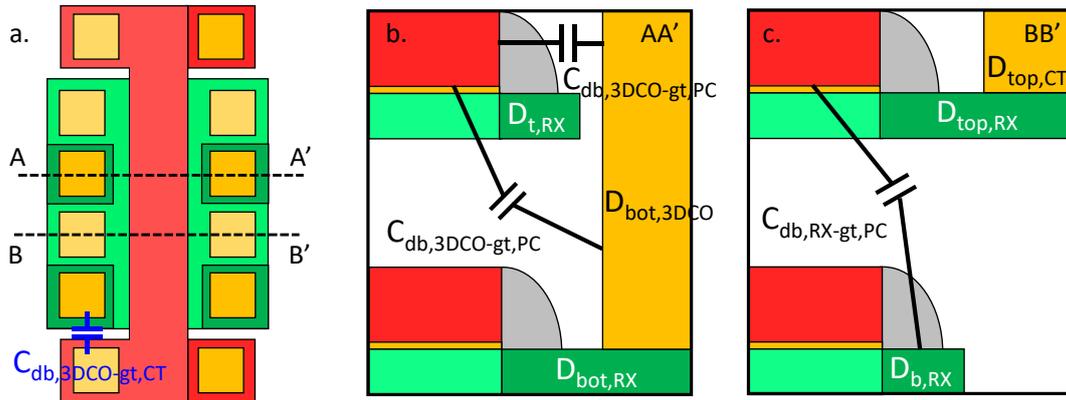


Fig. 6.11 C_{dbgt} decomposition

Lastly, in order to assess the capacitance components of C_{dbgt} , Fig. 6.11 (b) and Fig. 6.11 (c) show the respective cross-sections AA' and BB' of the structure top layout view (Fig. 6.11 (a)). From the cross-section Fig. 6.11 (c) it can be seen that there is a weak capacitance component of C_{dbgt} forming between the bottom-tier device drain diffusion and the top-tier device gate poly ($C_{db,RX-gt,PC}$), attributed to fringing electric fields through the top-tier device channel. On the other hand, concerning the 3D contact on the bottom-tier device drain electrode, one component is formed with the top-tier gate poly ($C_{db,3DCO-gt,PC}$) and the other with the top-tier gate contact ($C_{db,3DCO-gt,CT}$). Hence, the overall contribution of the 3D contact to C_{dbdt} is

$$C_{db,3DCO-gt} = C_{db,3DCO-gt,PC} + C_{db,3DCO-gt,CT} \quad (6-3)$$

Parasitic extraction was performed on the structure of Fig. 6.12, which contains the stacked devices in the layout configuration analyzed above with both devices in cutoff mode.

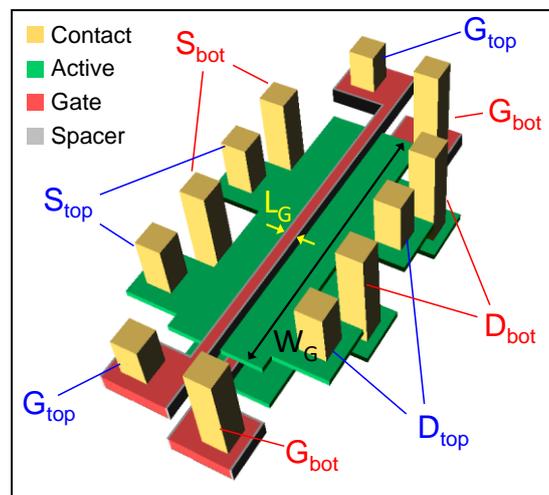


Fig. 6.12 Structure simulated in TCAD for the 3D contact capacitance contribution evaluation.

The results of the parasitic extraction are shown in Fig. 6.13 (a) in which the gate length of both devices was varied with constant gate width ($W_G=1\mu\text{m}$), whereas in Fig. 6.13 (b) the gate width was varied under a constant gate length ($L_G=1\mu\text{m}$).

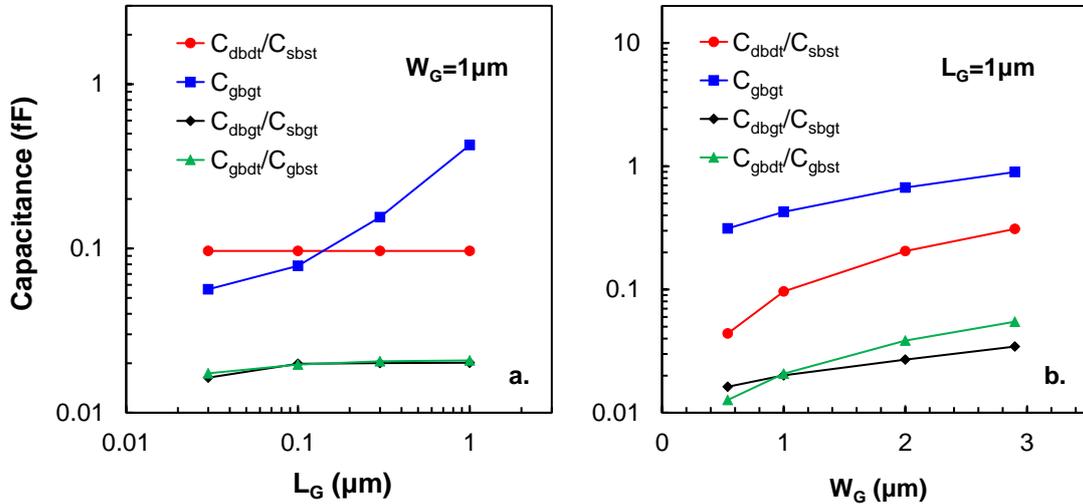


Fig. 6.13 Variation of coupling capacitances when both devices are in cut-off mode, versus (a) gate length for constant gate width ($W_G=1\mu\text{m}$) and (b) gate width for constant gate length ($L_G=1\mu\text{m}$)

The results reveal an approximately linear dependence of C_{gbgt} on the gate length of both devices while the rest of the capacitances can be considered constant with L_G . Additionally, all the capacitances increase with the gate width, as expected. To estimate the contribution of the 3D contacts to the total coupling capacitance of each top/bottom electrode pair, parasitic extraction was performed on the stacked device structure with the devices having the nominal gate length of 28FD (30nm).

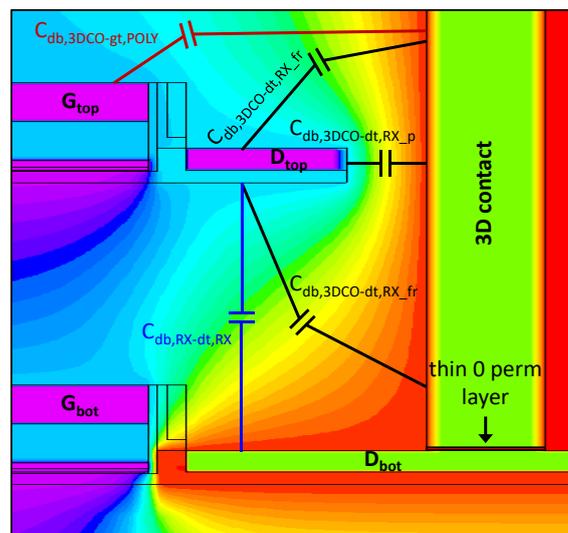


Fig. 6.14 Simulation setup for the evaluation of the C_{dbdt} capacitance component concerning the 3D contact

Then, each capacitance component was obtained adding a thin 0 permittivity layer between the source/drain diffusion area and the 3D contact as Fig. 6.14 shows. By this method the electric field shaping of each component is not disturbed and the extraction is accurate.

As Fig. 6.15 shows, 3D contacts can contribute by 18% to C_{dbdt}/C_{sbst} , 58% to C_{dbgt}/C_{sbgt} while for C_{gbdt}/C_{gbst} there is negligible contribution. Practically, this means that in C_{dbdt}/C_{sbst} and C_{gbdt}/C_{gbst} the vertical coupling dominates, whereas in C_{dbgt}/C_{sbgt} both vertical and horizontal coupling co-exist.

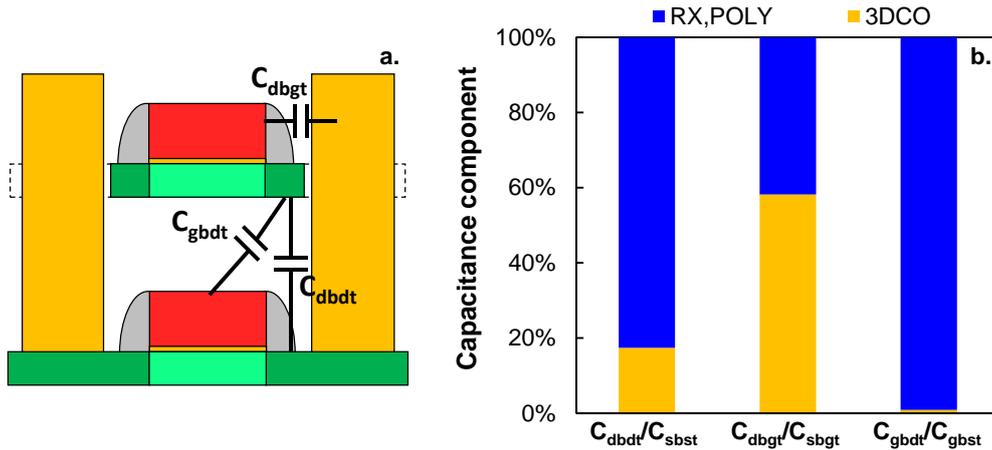


Fig. 6.15 Contribution of 3D contacts for each coupling capacitance with respect to the total one

The coupling capacitances also depend on the distance between the 3D contact on the bottom-tier active and the top-tier device gate (3DCO-PC) as Fig. 6.16 (a.) illustrates. The minimum value of this distance follows the highest density allowed in each technology node, thus moving from a 65nm- to 28nm-node the density increases.

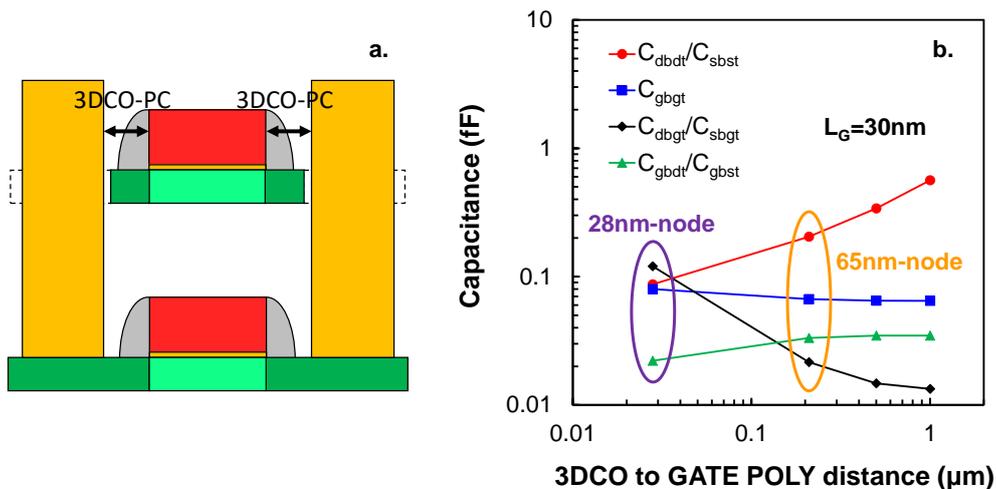


Fig. 6.16 Variation of the coupling capacitances as a function of the distance between 3D contact and the top-tier device gate

To determine the influence of the 3DCO-PC distance, the coupling capacitances were extracted varying d and the results are shown in Fig. 6.16 Fig. 6.16(b). It can be seen that for stacked devices with equal gate length having 28nm-node 3D contact density, C_{dbdt}/C_{sbst} is limited effectively while C_{dbgt}/C_{sbggt} increases abruptly.

These two capacitances can be further analyzed by estimating the contribution of the 3D contacts to each total capacitance. For that reason, the previous extraction was repeated following the methodology described previously for the capacitance decomposition. As Fig. 6.17 (a) shows, decreasing the distance between the 3D contact and the gate of the top-tier device, the contribution of 3D contacts to C_{dbdt}/C_{sbst} increases reaching 38% for 28nm-node. Accordingly, the same is true for C_{dbgt}/C_{sbggt} (Fig. 6.17 (b)) however in that case the 3D contact capacitance component essentially accounts for the total capacitance value.

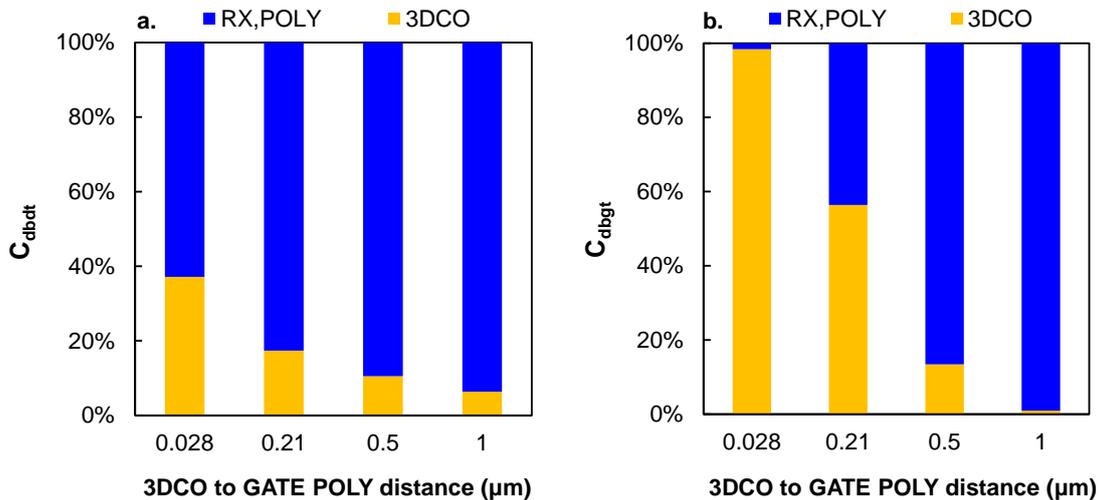


Fig. 6.17 Contribution of the 3D contact capacitance component with respect to the total one, versus the distance between 3D contact and the top-tier device gate, for (a) C_{dbdt} (b) C_{dbgt}

6.2 Coupling-induced V_{TH} shift modeling for stacked devices

The underlying physical mechanisms causing the BG effect of SOI MOS devices, are well studied and modeled in the literature. Accounting for long channel devices where the vertical fields from the front and back gate dominate, the problem of charge coupling between the front and back interface of the Si film becomes one-dimensional (1D) and one of the earliest solutions is the model proposed by Lim-Fossum [74] (the reader is encouraged to refer to §2.2.3). This model considers that the inversion of the silicon film due to the front/back gate bias forms a conductive channel at the front/back interface respectively. However, the charge centroid, i.e., the position of the maximum conduction path, is a function of the gate bias strength and moves progressively from the silicon film

center towards the interface, in the subthreshold region. For SOI MOS transistors with an ultra-thin silicon film (<10nm) the charge centroid is further confined at the center of the silicon film [99], [100], due to the Quantum Mechanical (QM) effects.

In this section, an efficient way of modeling the inter-tier coupling between active devices is suggested, considering the impact of both inter-tier static and dynamic coupling on the performance of victim top-tier digital devices ($EOT=1.12\text{nm}$, $t_{si}=1\text{nm}$, $t_{BOX}=130\text{nm}$). To accomplish this, both static and dynamic coupling effects are modeled through capacitance networks formed between the active devices and in particular to the BOX capacitance of the stacked devices.

This work is therefore organized as follows: in the first part, a first order approximation of the charge-coupling factor expression between the front and back interfaces of the stacked device is derived for low V_{Dtop} (uniform channel). Then, the effective oxide and ILD capacitance ($C_{ox,eff}$ and $C_{ILD,eff}$ respectively) for the stacked device are extracted from TCAD simulations for a wide range of top/bottom device geometries and positioning combinations. Afterwards, the capacitances are modeled with the aid of electrical field decomposition, considering an effective front and back gate area. The resulting capacitance models are inserted to the charge-coupling factor model which is later compared to the extracted values from I_D-V_G TCAD simulations.

6.2.1 Charge-coupling factor expression for long-channel top-tier devices

The behavior of the charge-coupling factor in SOI devices as predicted by the classic Lim-Fossum model [74] has been reviewed in §2.2.3, however it is observed that in UTBB (Ultra-Thin Body and Buried oxide) architectures with $t_{si}<20\text{nm}$, it differs significantly [100], [147]–[149]. Among these deviations are the increased slope and the absence of saturation in the experimentally measured coupling curves.

Advanced models [150], have corrected this error by taking into account the fact that an inversion charge can appear at the back interface when a strong Forward Back Bias (FBB) is applied. In particular, the BG bias $V_{G,b}$ modulates the position of the inversion charge conduction path, i.e. the charge centroid. Fig. 6.18 presents qualitatively the threshold voltage versus back-gate voltage diagram for UTBB SOI devices, assuming the critical cases where the conduction channel is formed either at the front or at the back interface for a reverse or FBB, respectively.

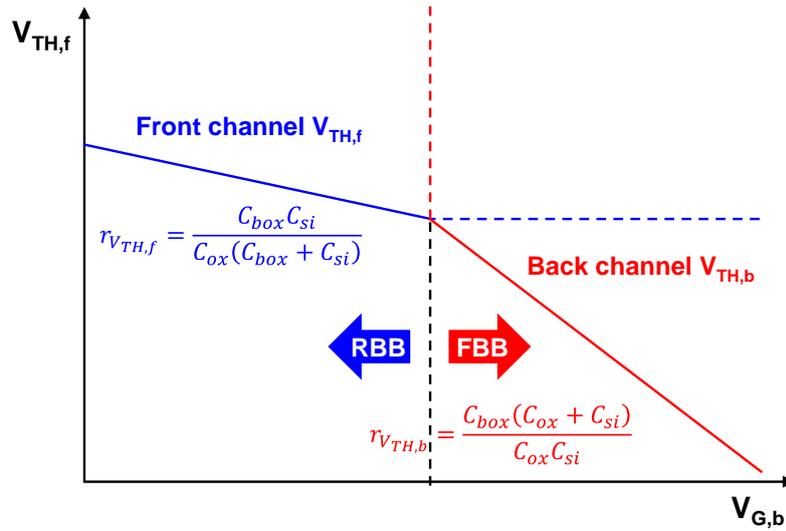


Fig. 6.18 Schematic diagram of the Threshold voltage sensitivity of the front-gate versus the back-gate bias in an FDSOI device taking into account the effect of back-gate inversion.

Obviously, the transition between these two regions is not abrupt and the charge centroid moves progressively across the channel thickness towards the front/back interface under a reverse/forward BG bias respectively. The work of [151], [152] exploits the above-mentioned behavior, capturing effectively the back-bias influence on the I-V characteristics of UTBB SOI devices. Indeed, these models can accurately provide the charge centroid position by using relatively complex analytical expressions. A simpler expression for the charge centroid has been presented in [153], to model the SCE in FDSOI devices. However, a common characteristic of all these models is the need for an accurate calculation of the surface potential ϕ_s or the localized surface charge Q_{iy} .

To examine the influence of the back-bias on the charge centroid of stacked FDSOI devices in 3DSI, Fig. 6.19 recalls the TCAD simulation results for the carrier concentration of N and P-type FDSOI MOSFETs under threshold voltage bias condition, varying the bottom SOI gate voltage from -20V to +20V with a step of 5V. From the extracted carrier concentration $n(x)$ (and $p(x)$) for both types of the top-tier devices, the charge centroid x_c can be calculated as

$$x_c = \frac{\int_0^{t_{si}} n(x) x dx}{\int_0^{t_{si}} n(x) dx}, x_c = \frac{\int_0^{t_{si}} p(x) x dx}{\int_0^{t_{si}} p(x) dx} \quad (6-4)$$

The calculated charge centroid from TCAD simulations is shown in Fig. 6.20 (a) as a function of the back-gate bias in the range of -20V to 20V, whereas a zoom-in view in the range of -2.5V to 2.5V is presented in Fig. 6.20 (b). It is evident that the charge centroid gradually moves across the channel thickness according to the polarity and the strength of the back-gate bias, as explained

previously. However, one can easily observe that for a back-gate bias in the range of -2.5V to 2.5V, the position of the charge centroid remains relatively close to the center of the channel (3.5 nm) with a slight deviation.

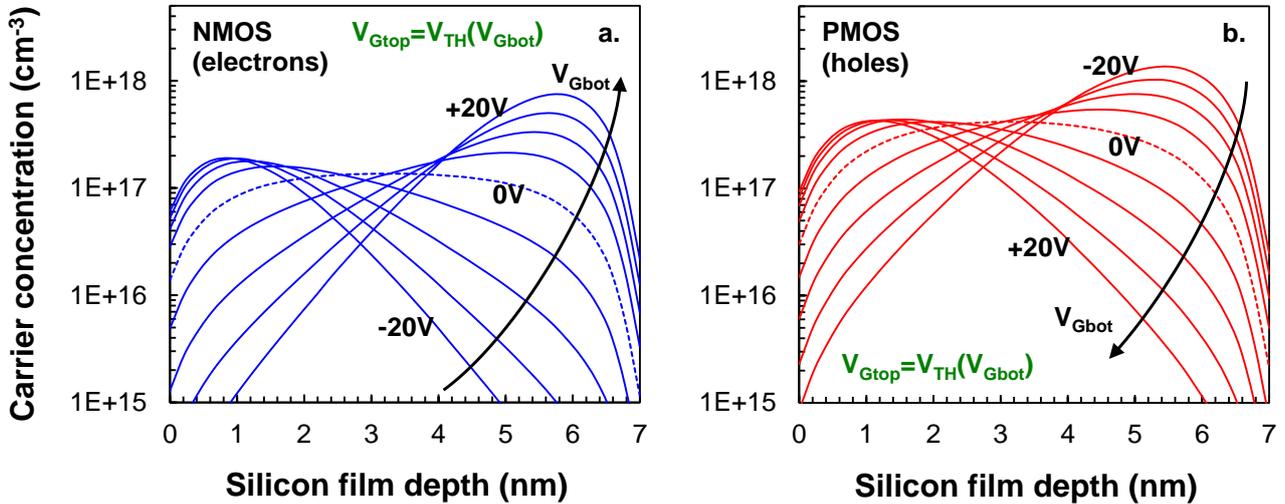


Fig. 6.19 Carrier concentration versus the distance along channel for NMOS (a) and PMOS device (b)

In addition, Fig. 6.21 shows the extracted charge centroid position versus the front gate bias of the top-tier device under zero bottom-tier device gate bias. It can be seen that the charge centroid position is placed around the center of the top-tier device channel until its gate bias overcomes the threshold voltage V_{TH} where it moves significantly towards the front interface

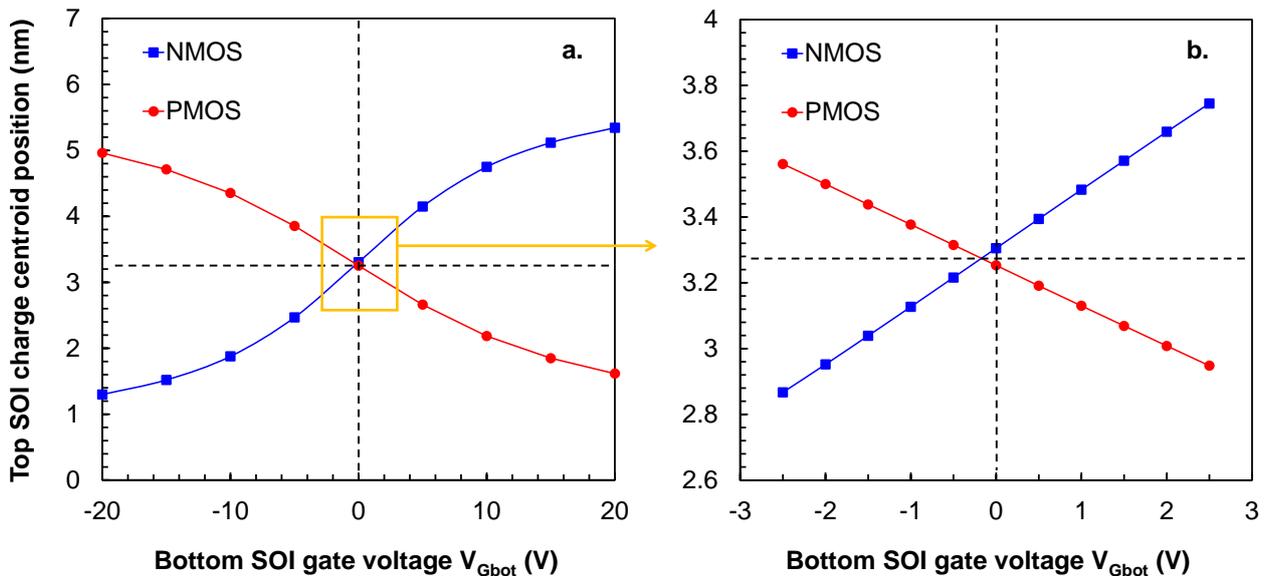


Fig. 6.20 Top-tier device carrier centroid position as a function of the applied bias at the bottom-tier device gate electrode with a range (a) of -20V to 20V and (b) -2.5V to 2.5V.

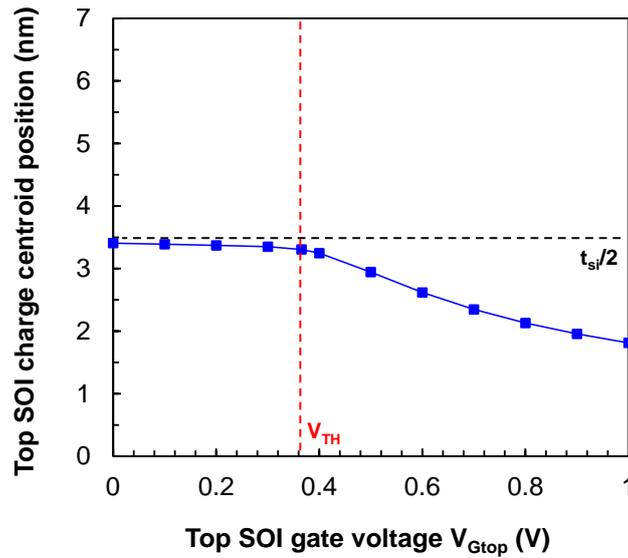


Fig. 6.21 Top-tier device carrier centroid position as a function of its gate voltage under zero V_{Gbot}

In order to investigate the impact of the calculated charge centroid position at the threshold voltage condition on the charge-coupling factor expression, the 1-D solution obtained by the Lim-Fossum model can be modified following the charge sheet and depletion approximation and taking into account that the inversion charge is concentrated to the point of the charge centroid (x_c) as depicted in Fig. 6.22.

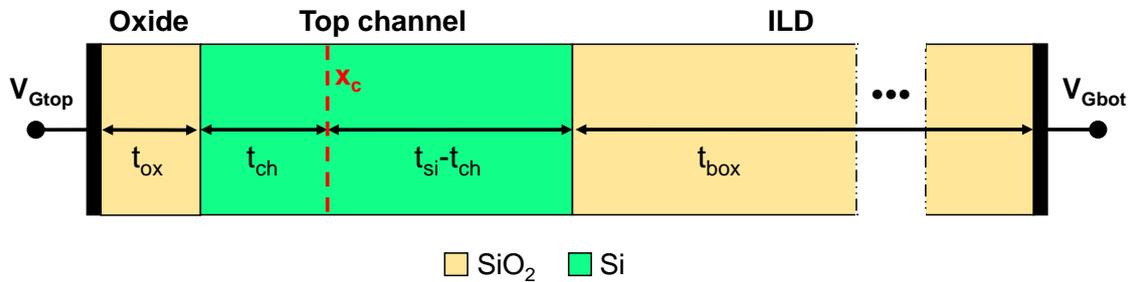


Fig. 6.22 Simplified schematic view of the carrier centroid position under 1-D approximation (Long channel device).

That being so, the equivalent oxide capacitance becomes

$$C_{ox,eq} = \left(\frac{1}{C_{ox}} + \frac{1}{C_{ch}} \right)^{-1} \quad (6-5)$$

whereas the equivalent silicon film capacitance can be considered as

$$C_{si,eq} = \left(\frac{1}{C_{si}} - \frac{1}{C_{ch}} \right)^{-1} \quad (6-6)$$

with $C_{ch}=\epsilon_{si}/t_{ch}$ being the capacitance of the hypothetically depleted silicon film with thickness t_{ch} , i.e. the distance of the charge centroid position from the front interface. Consequently, the charge-coupling factor expression becomes

$$r = \frac{dV_{th,top}}{dV_{Gbot}} = \frac{C_{box}C_{si,eq}}{C_{ox,eq}(C_{box} + C_{si,eq})} = \frac{\frac{1}{C_{ox}} + \frac{1}{C_{ch}}}{\frac{1}{C_{box}} + \frac{1}{C_{si}} - \frac{1}{C_{ch}}} \quad (6-7)$$

Inserting the calculated charge centroid position (Fig. 6.20) into the above simplified generic expression for the charge-coupling factor, the threshold voltage shift ΔV_{TH} of the top-tier device can be obtained as a function of the bottom-tier device gate bias. The results are plotted in Fig. 6.23, along with the TCAD data extracted from the CC and $\max(dC_{gc}/dV_g)$ methods previously. As expected, (6-7) captures efficiently the sensitivity of the top-tier device threshold voltage to the bottom-tier device gate bias variation.

The aforementioned analysis enables two useful assumptions for the charge-coupling expression to be used in our modeling approach. First, the charge centroid position can be considered unaffected of the bottom-tier device gate bias due to the relatively thick ILD. Indeed, assuming that the range of the bottom-tier device gate bias is limited to the power supply voltage (V_{DD}), the maximum value of the latter can be as high as 2.5V for bottom-tier analog devices.

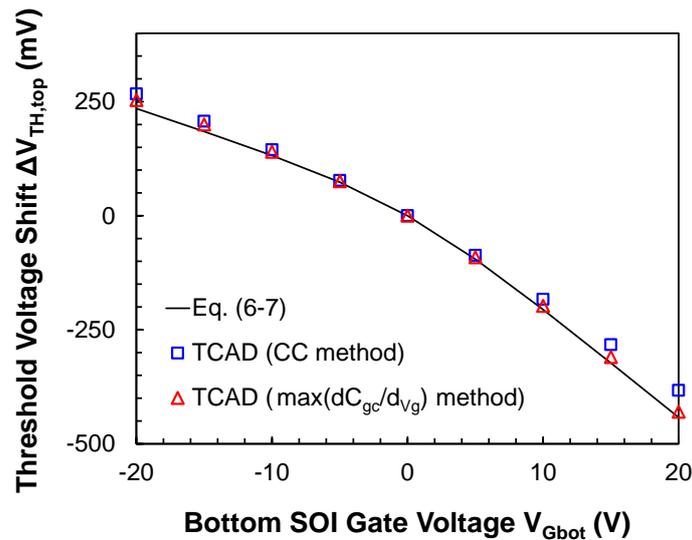


Fig. 6.23 Comparison of calculated threshold voltage shift using the obtained centroid values and the extracted results from I-V, C-V simulations, versus the bottom SOI gate voltage.

The aforementioned analysis enables two useful assumptions for the charge-coupling expression to be used in our modeling approach. First, the charge centroid position can be considered unaffected of the bottom-tier device gate bias due to the relatively thick ILD. Indeed, assuming that the range of the bottom-tier device gate bias is limited to the power supply voltage (V_{DD}), the maximum value of the latter can be as high as 2.5V for bottom-tier analog devices.

Furthermore, a second simplification can be made by placing the charge centroid at the center of the channel. Having that in mind, the distance of the charge centroid position from the front interface t_{ch} is now $t_{si}/2$, thus (6-7) becomes

$$r = \frac{dV_{th,top}}{dV_{Gbot}} = -\frac{C_{box}(2C_{si} + C_{ox})}{C_{ox}(2C_{si} + C_{box})} \tag{6-8}$$

Fig. 6.24 shows the comparison between (6-7) (varying centroid position) and (6-8) (fixed centroid position), along with the TCAD data obtained with CC and $\max(dC_{gc}/dV_g)$ methods. As observed, within the power supply range of bottom-tier devices, the simplifications adopted for the charge-coupling factor expression yield only a minor error (<4%) for the negative edge of V_{Gbot} , which is actually unrealistic, since the bottom-tier device gate shall always vary between 0 and 2.5V (maximum V_{Gbot} in the case of analog bottom-tier devices with $V_{DD}=2.5V$) regardless the MOSFET polarity.

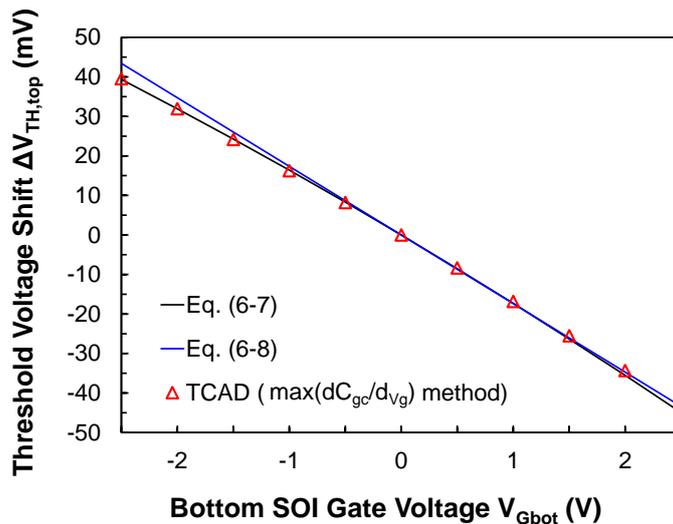


Fig. 6.24 Comparison of calculated threshold voltage shift from eq. (6-7), eq. (6-8) and the TCAD results extracted with CC and $\max(dC_{gc}/dV_g)$ methods, versus the bottom SOI gate voltage.

6.1.1 Modeling the effective ILD capacitance of stacked devices ($C_{ILD,eff}$)

6.1.1.a Impact of bottom/top length ratio with regard to scaling

The expression (6-8) derived for the charge-coupling factor in the previous section is valid for long-channel top-tier devices that have their back-gate being the bottom-tier device gate electrode. However, this is an ideal case and in reality the charge-coupling factor value can deviate from the calculated one as shown in Chapter 3, due to the impact of SCE and the relative misalignment.

To describe the dependency of the top/bottom length ratio vs with regard to L_{Gtop} scaling, the effective ILD capacitance ($C_{ILD,eff}$) was extracted from TCAD simulations and an effective length for the bottom-tier device gate electrode was associated, as if $C_{ILD,eff}$ was an equivalent parallel plate capacitance with value

$$C_{ILD,eff} = \frac{\epsilon_{ox}}{t_{ILD}} W_G L_{Gbot,eff} \quad (6-9)$$

Beginning with a long-channel top-tier device of $L_{Gtop}=30\mu\text{m}$ (no impact of SCE), Fig. 6.25 (a) shows the corresponding $L_{Gbot,eff}$ values plotted versus the designed gate length of the bottom-tier devices. As expected, when the bottom-tier device gate length is equal or greater than the length of the top-tier device channel (L_{Gtop}), the effective bottom-tier device gate length $L_{Gbot,eff}$ is fixed to the value of L_{Gtop} and represents the upper limit. On the contrary, the lower limit of $L_{Gbot,eff}$ is imposed by the fringing electric fields when $L_{Gbot} \ll L_{Gtop}$. For instance, a top-tier device with gate length $30\mu\text{m}$ stacked on top of a bottom-tier device with gate length 30nm , experiences an effective back-gate length $L_{Gbot,eff} = 150\text{nm}$.

Moving on to top-tier devices with sub-micrometer gate length, Fig. 6.25 (b) shows their effective back-gate length $L_{Gbot,eff}$ versus the actual gate length of the respective bottom-tier device. While the $L_{Gbot,eff}$ versus L_{Gbot} trend seems similar to the long channel top-tier devices, as L_{Gtop} scales down, the bottom-tier device gate length for which $L_{Gbot,eff} = L_{Gbot}$, becomes greater. As a consequence, a top-tier device with gate length 30nm will experience the maximum effective back-gate length when the bottom-tier device is equal or greater than 500nm . On the other hand, the lower limit ($L_{Gbot} \ll L_{Gtop}$) of the top-tier device effective back-gate length, is again determined by the fringing fields of the bottom, which are however dramatically limited due to the charge sharing effect of the bottom-tier device gate electrode with the top device diffusion regions of D_{top} , S_{top} .

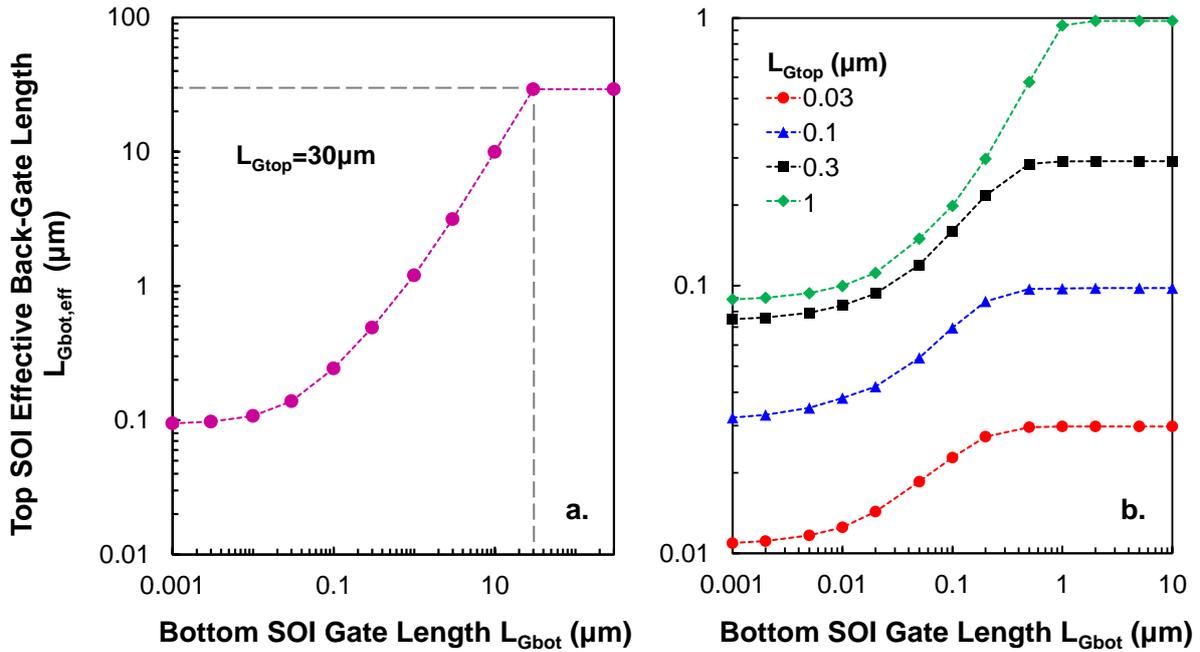


Fig. 6.25 Extracted effective gate length versus the designed gate length for the bottom-tier device when (a) $L_{Gtop}=30\mu\text{m}$ (long-channel behavior) and (b) for sub- μm gate lengths of the top device.

This effect of the bottom-tier gate electrode length variation can be visualized qualitatively in Fig. 6.26, where it is illustrated schematically. For $L_{Gtop} > L_{Gbot}$ the effective bottom-tier gate length is always larger than the actual value due to fringing electric fields. When L_{Gbot} increases, $L_{Gbot,eff}$ is always smaller and there is a critical length where $L_{Gbot,eff}$ saturates. The latter is equal to L_{Gtop} for long channel devices, yet for sub-micrometer devices it is much greater than L_{Gtop} .

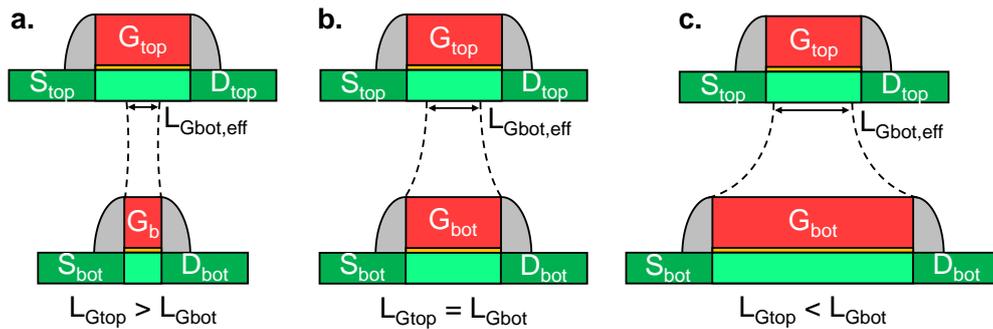


Fig. 6.26 Schematic view of the “effective back-gate length” for the top-tier device when the bottom-tier device gate length is (a) smaller (b) equal and (c) larger than the top gate length.

The behavior described above is further enhanced due to the presence of the source and drain diffusion areas of the bottom device. Indeed, Fig. 6.27 (a) shows the electric field vector plot generated in TCAD for a structure where the bottom device is a regular SOI MOSFET and Fig. 6.27 (b) shows another one where the bottom device source and drain diffusion areas are replaced by dielectric. The electric field induced by the bottom device gate bias of 1V appears more confined in

the first case due to the high electric field created by the bottom device source and drain diffusion areas.

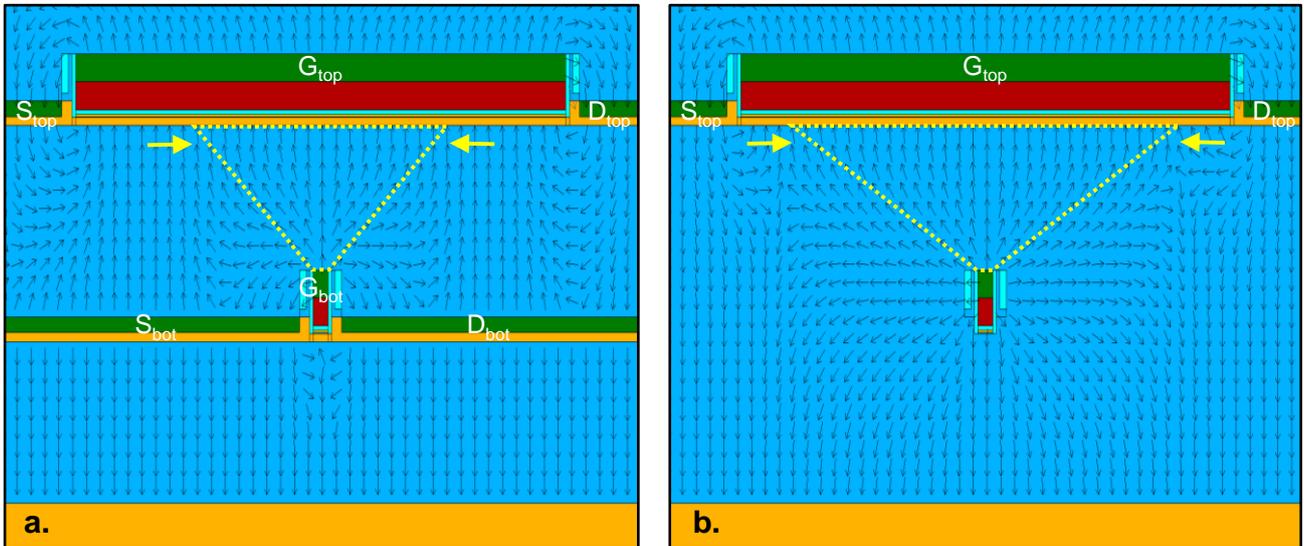


Fig. 6.27 Electric field vector plot showing the shape of the flux induced by the bottom-tier device gate electrode of $L_{Gbot}=30\text{nm}$ to the top-tier device channel (a) w/ and (b) w/o the bottom-tier S/D regions.

The extracted values for the effective back-gate length of top-tier devices with (w/) and without (w/o) the bottom-tier device source/drain regions are shown in Fig. 6.28. It can be seen that the presence of the bottom-tier source/drain regions reduces the effective back-gate length of $L_{Gbot,eff}$ of top-tier devices by a factor of ~ 1.6 for $L_{Gbot} \ll L_{Gtop}$.

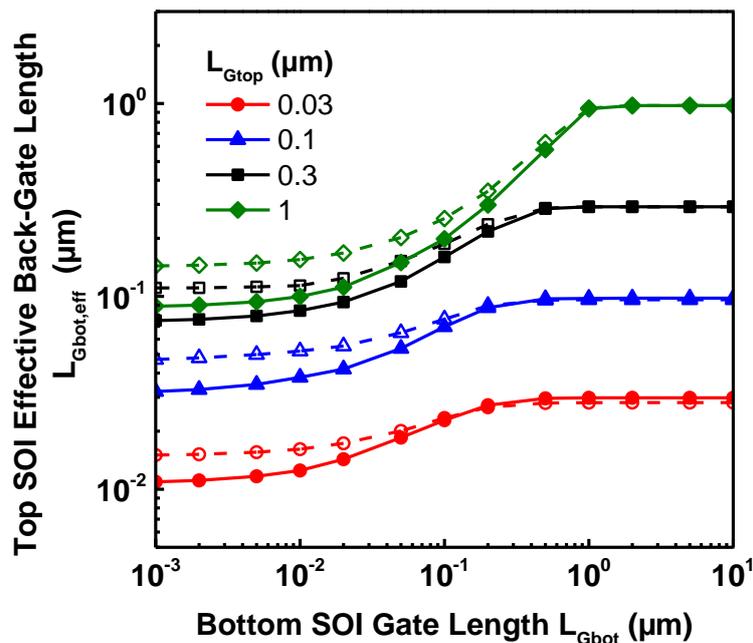


Fig. 6.28 Extracted effective back-gate length for the top-tier device versus the designed bottom-tier gate length, varying L_{Gtop} . Solid and open symbols indicate a structure w/ and w/o the bottom-tier S/D regions respectively.

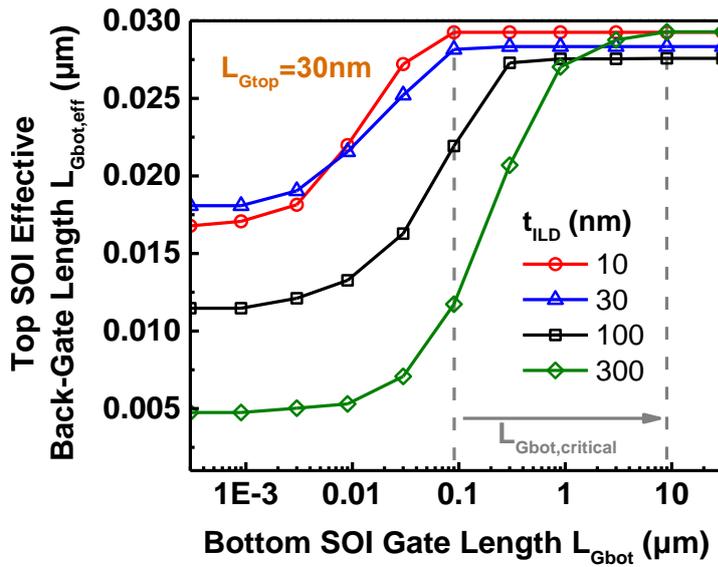


Fig. 6.29 Extracted effective back-gate length for the top-tier device versus the designed bottom-tier gate length, varying t_{ILD} for $L_{Gtop}=30\text{nm}$. The critical effective bottom gate length increases as a function of the ILD thickness.

On the other hand, the critical bottom gate length, $L_{Gbot,critical}$, is a function only of the ILD thickness as shown in Fig. 6.29. Thus, in our case ($t_{ILD}=130\text{nm}$), $L_{Gbot,critical}\sim 300\text{nm}$.

Similarly to the effective length of the bottom-tier device gate electrode $L_{Gbot,eff}$, an expression for the effective length of the top-tier device gate electrode $L_{Gtop,eff}$, can be derived. Indeed, $L_{Gtop,eff}$ is extracted from $C_{ox,eff}$ according to

$$C_{ox,eff} = \frac{\epsilon_{ox}}{t_{ox}} W_G L_{Gtop,eff} \quad (6-10)$$

with the results shown in Fig. 6.30.

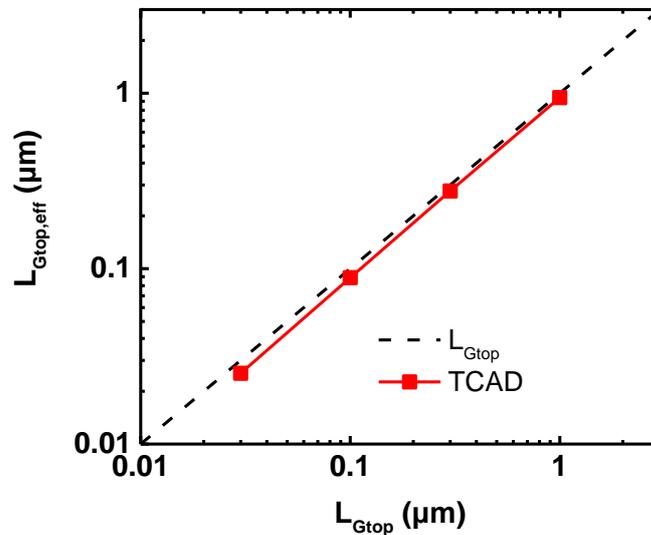


Fig. 6.30 Effective front-gate length for the top-tier device versus its designed gate length.

The slight deviation from the designed gate length of the top-tier device in Fig. 6.30, attributed to SCE, is responsible for the increase in the charge-coupling factor when $L_{Gbot} \gg L_{Gtop}$, observed in Fig. 3.31. With the above analysis, it is obvious that in order to efficiently model the effective lengths of both top- and bottom-tier gate which are virtually seen at the front/back interface of the top-tier device channel, analytic expressions for $C_{ox,eff}$ and $C_{ILD,eff}$ are needed.

In the case where there is asymmetry between top- and bottom-tier device gate areas, the capacitance values in expression (6-8) have to be replaced with the effective ones, i.e., to be multiplied by the effective “back-gate” area seen by the top-tier device. Considering two stacked long channel devices as in Fig. 6.31, when the bottom-tier device gate length is larger than the top-tier device gate length, the BOX capacitance of the latter is due to the overlapping area of the top-tier device channel over the bottom-tier device gate electrode, noted C_{ov} in Fig. 6.31 (a). Therefore, the top-tier device effective back-gate length $L_{Gbot,eff}$ remains constant at the value of L_{Gtop} .

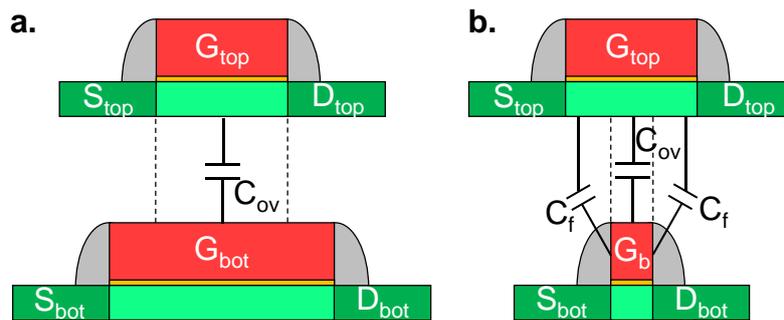


Fig. 6.31 Schematic view of the $C_{ILD,eff}$ components (C_{ov} , C_f) when the bottom device gate length is (a) smaller and (b) larger than the top device gate length.

On the contrary, in the case where the bottom-tier device gate length is smaller than the top-tier device gate length, the BOX capacitance is reduced and can be split in a parallel plate capacitance component C_{ov} as well as fringe capacitance components C_f as shown in Fig. 6.31 (b). Alternatively, the same concept is valid if there is an asymmetry in the gate width of the devices, so that the overlapping area of the top-tier device channel to the bottom-tier device gate electrode defines $C_{ILD,eff}$.

It becomes rather obvious that the parallel component of $C_{ILD,eff}$, has to be proportional to the overlapping area of the top-tier device channel to the bottom-tier device gate electrode (Fig. 6.31 (a)), given by the parallel plate capacitance equation

$$C_{ov} = \frac{\epsilon_{ox}}{t_{ox}} W_{ov} L_{ov} \tag{6-11}$$

with W_{ov} , L_{ov} being the overlapping width and length respectively between the top-tier device channel and the bottom-tier device gate electrode. The maximum value of this capacitance is reached when the bottom-tier device gate electrode area is equal or greater to the top-tier device channel area and so (6-11) becomes

$$C_{ov} = \frac{\epsilon_{ox}}{t_{ox}} W_{Gtop} L_{Gtop} \tag{6-12}$$

Since the device geometrical parameters such as gate mask width and length are not bias-dependent, there shall be no discontinuity issues in a SPICE simulation even if we utilize regional functions. Such a function can has been introduced to handle the case of the overlapping capacitance component C_{ov} , as

$$C_{ov}(L_{Gbot}) = \begin{cases} \frac{\epsilon_{ox}}{t_{ox}} W_{Gbot} L_{Gbot}, & L_{ov} < L_{Gtop} \\ \frac{\epsilon_{ox}}{t_{ox}} W_{Gtop} L_{Gtop}, & L_{ov} \geq L_{Gtop} \end{cases} \tag{6-13}$$

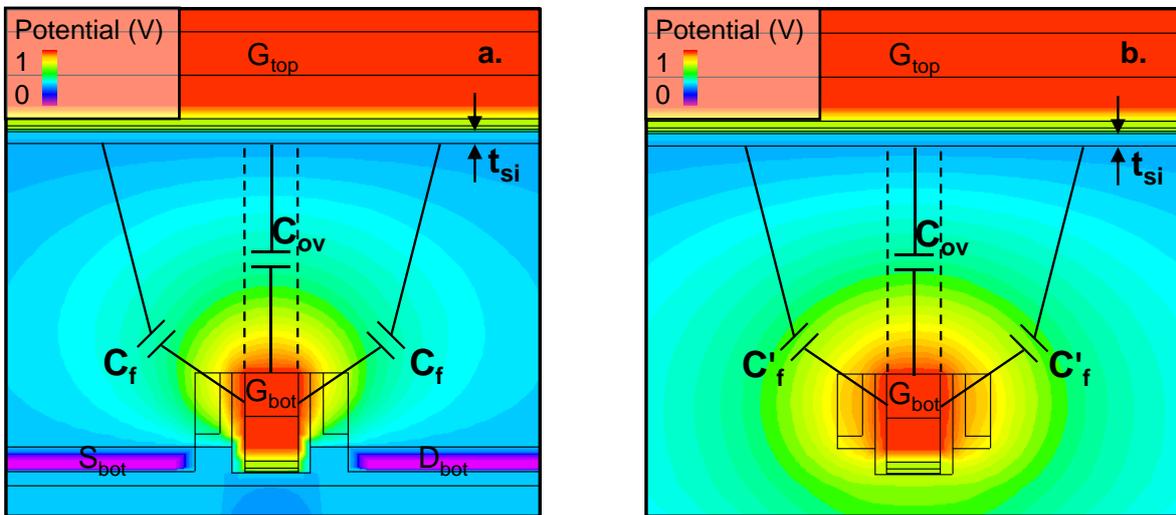


Fig. 6.32 Potential contour plot generated in TCAD for stacked devices with $\frac{L_{Gbot}}{L_{Gtop}} = 0.001$, in order to extract the fringe capacitance components of $C_{ILD,eff}$. The bottom-tier device has been simulated (a) w/ and (b) w/o the bottom-tier S/D region, in order to assess their impact on C_f .

For the calculation of the fringe capacitance, analytic expressions can be utilized from prior modeling approaches in CMOS devices [154]–[158]. These models define as a fringe capacitance the electric field lines between two perpendicular electrodes separated by an insulator. As opposed to a parallel-plate capacitance, the electric field lines of a fringe capacitance are not linear but elliptical.

The majority of the existing models use conformal mapping to perform an accurate fringe modeling. The exact formulations of this transformation are beyond the scope of this work and thus can be excluded.

Lacord et al. [157] suggested in his model (which will be referred as [Lacord 12] henceforth) two expressions for the evaluation of the fringe capacitance between two perpendicular conductors C1 and C2, as Fig. 6.33 shows.

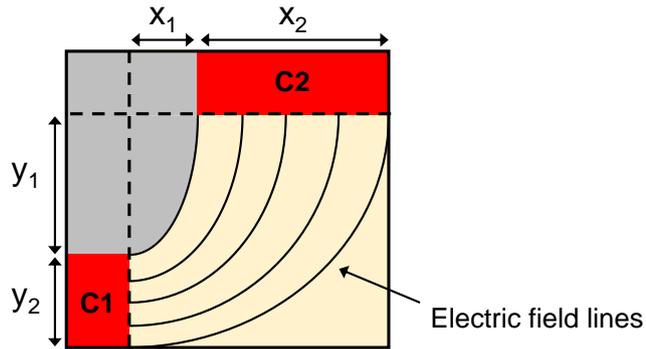


Fig. 6.33 Electric field lines between two perpendicular electrodes.

Considering that the two conductors are separated by dielectric (e.g., SiO₂), the capacitance due to elliptical electric field lines is given by

$$C_{f,1} = 2W_G \frac{\epsilon_{ox}}{\pi} \left[\sinh^{-1} \left(\frac{\sqrt{x_1^2 + \min(y_2, x_2)^2 + 2 \cdot y_1 \min(y_2, x_2)}}{\sqrt{|x_1^2 - y_1^2|}} \right) - \sinh^{-1} \left(\frac{x_1}{\sqrt{|x_1^2 - y_1^2|}} \right) \right] \quad (6-14)$$

whereas the capacitance due to the region $x < x_1$ and $y < y_1$ (gray area in Fig. 6.33) where electric field lines are neither elliptical nor regular, the model suggests the equation

$$C_{f,2} = 0.35 \cdot W_G \frac{\epsilon_{ox}}{2\pi} \ln \left(\frac{\pi \cdot W_G}{t_{ILD}} \right) \quad (6-15)$$

Therefore, the total fringe capacitance is the sum of (6-14) and (6-15)

$$C_f = C_{f,1} + C_{f,2} \quad (6-16)$$

In our case the dimensions in (6-14) and (6-15) must be replaced by the ones presented schematically in Fig. 6.34, so that $x_1=0$, $x_2 \approx L_{G_{top}}/2$ (since $L_{G_{bot}} \ll L_{G_{top}}$), $y_1=t_{ILD}$ and $y_2=H_G$ (height of the bottom-tier gate electrode).

Under the above modeling approach, respectively substituting the values of x_1 , x_2 , y_1 , y_2 in (6-14) and (6-15), one gets

$$C_{f,1} = 2W_G \frac{\epsilon_{ox}}{\pi} \sinh^{-1} \left(\sqrt{\frac{H_G^2 + 2 \cdot t_{ILD} H_G}{t_{ILD}}} \right) \quad (6-17)$$

and

$$C_{f,2} = 0.35 \cdot W_G \frac{\epsilon_{ox}}{2\pi} \ln \left(\frac{\pi \cdot W_G}{t_{ILD}} \right) \quad (6-18)$$

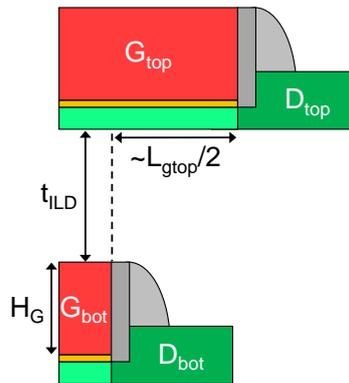


Fig. 6.34 Schematic cross-section view of the stacked devices with the dimensions used in the equations of Lacord et al.

The model can be compared to the accurate value of C_f in our structures, which can be extracted from TCAD simulations in the case where the bottom-tier device gate length $L_{G_{bot}}$ is significantly smaller than the top-tier device gate length $L_{G_{top}}$. For that purpose, a ratio of $\frac{L_{G_{bot}}}{L_{G_{top}}} = 0.001$ was selected, so that C_f dominates over C_{ov} . In order to estimate the impact of the bottom-tier S/D regions, on the fringe capacitance component, the setup was repeated excluding them.

The calculated value of the total fringe capacitance from the model of [Lacord 12] and the one obtained from TCAD simulations (labeled w/ bottom S/D) are presented in the diagram of Fig. 6.35. As shown, the extracted value from simulations appears to be smaller, approximately half the value of the one calculated from the analytical equations. Apparently, this reduction is an outcome of the charge sharing effect in the presence of multiple electrodes on both sides of the bottom-tier gate electrode (S_{bot} , D_{bot}) [156].

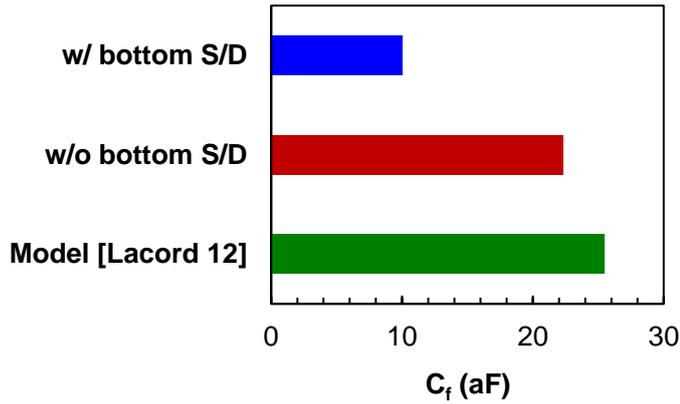


Fig. 6.35 Fringe capacitance component of $C_{ILD,eff}$

For comparison, Fig. 6.35 includes also the value of the fringe capacitance C_f extracted from TCAD simulations for the same structure, yet excluding the S/D diffusion regions of the bottom-tier device (Fig. 6.32 (b)). Evidently, the C_f value in the latter case is closer to the one calculated analytically. Continuing our analysis, the total back-gate oxide capacitance is given by

$$C_{ILD,eff} = C_{ov} + 2 \cdot C_f \quad (6-19)$$

Fig. 6.36 (a) shows the values for the effective ILD capacitance ($C_{ILD,eff}$) obtained from TCAD simulations (open circles), and our long-channel model. Furthermore, the resulting effective back-gate length of the long-channel top-tier device is demonstrated in Fig. 6.36 (b) along with the extracted data from TCAD. The very good agreement between the two validates our modeling approach.

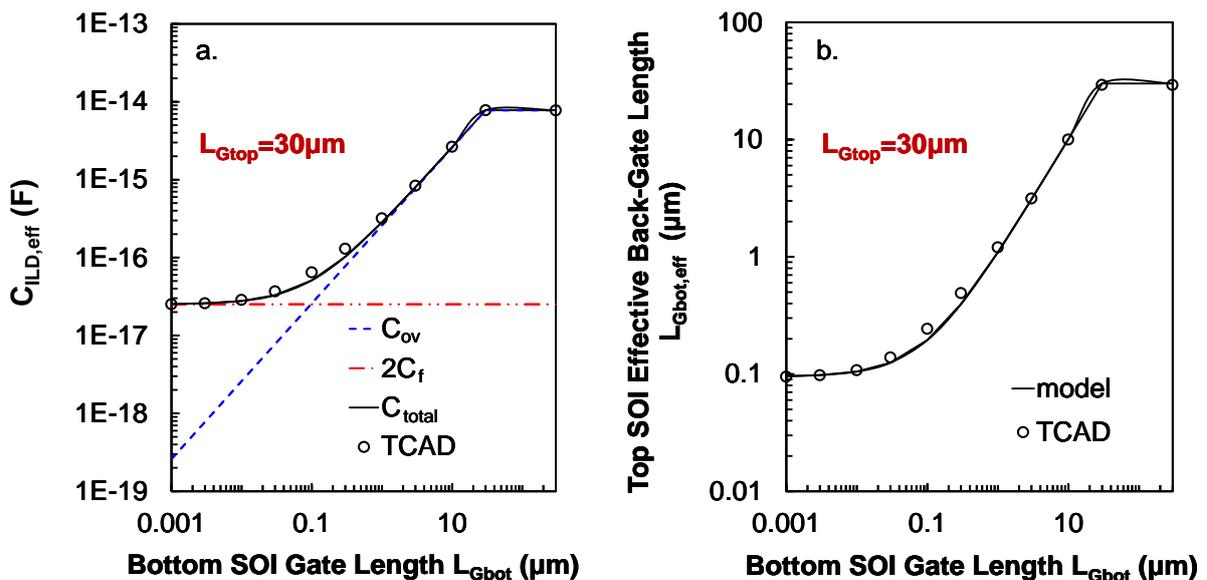


Fig. 6.36 (a) $C_{ILD,eff}$ and (b) effective gate length versus the designed gate length for the bottom tier device for a long channel top device. The symbols indicate the TCAD capacitance values in (a) from which the effective back-gate length for the top-tier device has been extracted in (b). The C_{ov} component has been calculated from (6-13) and C_f has been extracted from TCAD.

So far, only long channel top-tier devices have been considered in our modeling approach. However, in order to model the $C_{ILD,eff}$ capacitance for a wide range of dimensions of top/bottom tier devices, the impact of the gate length scaling needs to be included. For that reason, the total $C_{ILD,eff}$ as well as its components (C_{ov}, C_f) were extracted with TCAD while decreasing the gate length of the top-tier devices in logarithmic scale from $1\mu\text{m}$ (Fig. 6.37 (a)) to 30nm (Fig. 6.37 (b)).

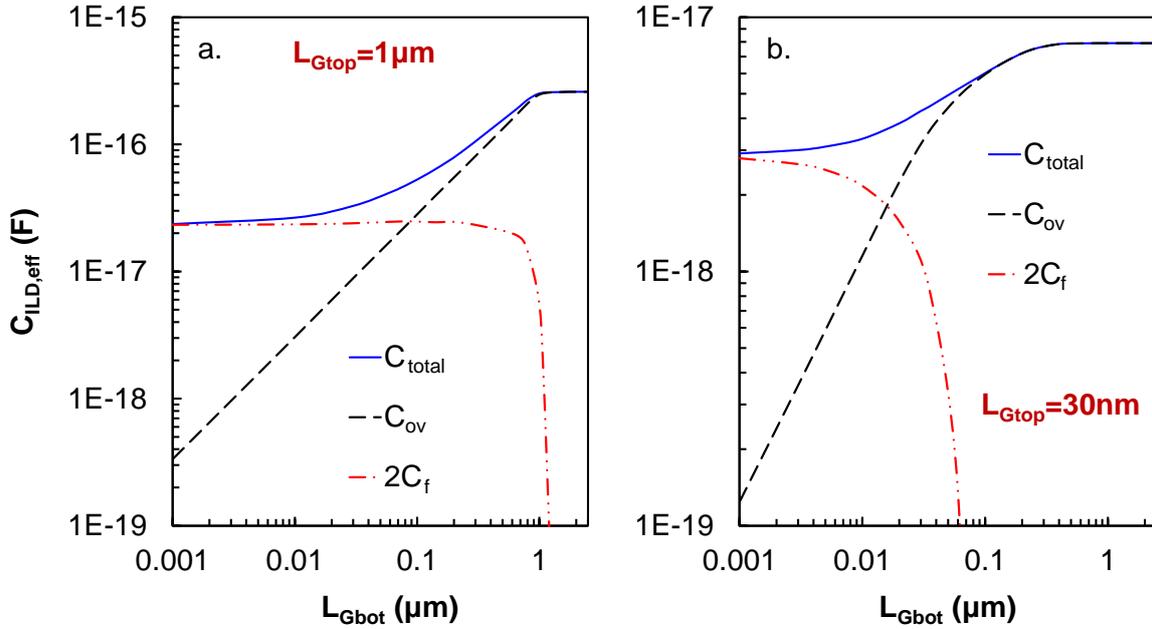


Fig. 6.37 Effective ILD capacitance versus the designed gate length for the bottom tier device and its respective parallel and fringe components as extracted from TCAD for (a) $L_{Gtop}=1\mu\text{m}$ and (b) $L_{Gtop}=30\text{nm}$.

While for a $1\mu\text{m}$ long top-tier device the $C_{ILD,eff}$ components follow the behavior of a long-channel device, this is not the case for a top-tier device having 30nm gate length. For the latter, as the gate length of the bottom-tier device is enlarged, the fringe capacitance component gradually degrades while the overlap capacitance component seems to increase according to

$$C_{ov} = \alpha \frac{\epsilon_{ox}}{t_{ILD}} W_{ov} L_{ov} \quad (6-20)$$

where α is an empirical fitting parameter. For top-tier device of $L_{Gtop}=30\text{nm}$ this parameter has a value of 0.45 and increases with the top-tier device gate length until it reaches unity (long-channel behavior).

Furthermore, as the bottom-tier device gate length reaches the critical value where $L_{Gbot,eff}$ saturates, the overlap capacitance component progressively approaches its maximum value, differing from the abrupt transition in long-channel devices. The maximum value of the overlap capacitance is again given by (6-12) and is independent of the short channel effects.

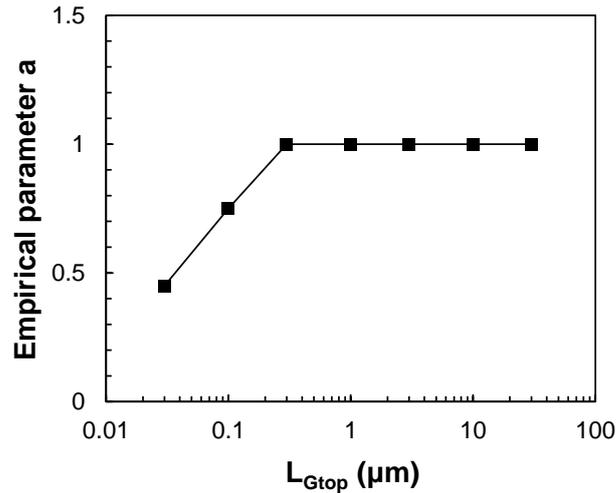


Fig. 6.38 Variation of the empirical parameter a used in equation (6-20) versus the top-tier device gate length.

Fig. 6.39 shows the fringe capacitance component of $C_{ILD,eff}$ versus the top-tier device gate length, plotting the values obtained from TCAD simulation (with and without the bottom-tier source/drain region) together with the ones calculated from the model [Lacord 12]. It can be observed that the TCAD results deviate significantly from the calculated values and the difference becomes more pronounced as L_{Gtop} reaches 30nm in the presence of the bottom-tier device source/drain regions.

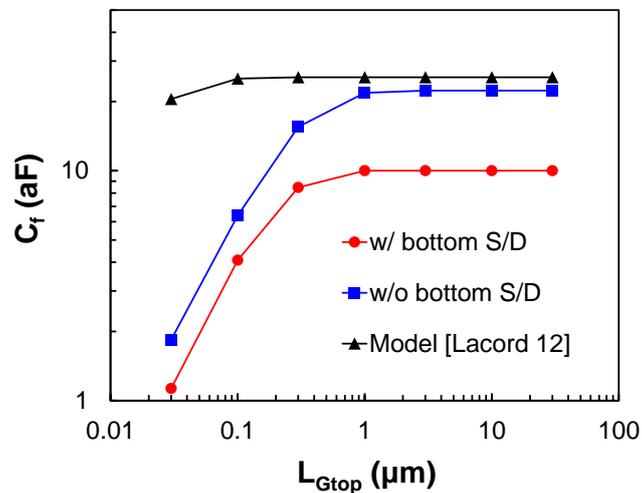


Fig. 6.39 Variation of the fringe capacitance component of $C_{ILD,eff}$ with the top-tier device scaling. For the accurate extraction of C_f , L_{gtop} is considered to be 1000x greater than L_{gbot} .

Indeed, as it has been shown in Fig. 6.27 (a), the electric field is shaped in such a way that needs complex analytical equations to be modeled. This task is beyond the scope of this thesis; hence a table model can be utilized to capture the variation of the C_f component with the top-tier device scaling. Our modeling approach can be compared next to the charge-coupling factor results as

extracted from I-V simulations (Fig. 6.40), where a good match among the two can be observed. This validates our simplifications concerning the charge-coupling factor expression and the effective gate length concept for the front/back interface of the top-tier devices.

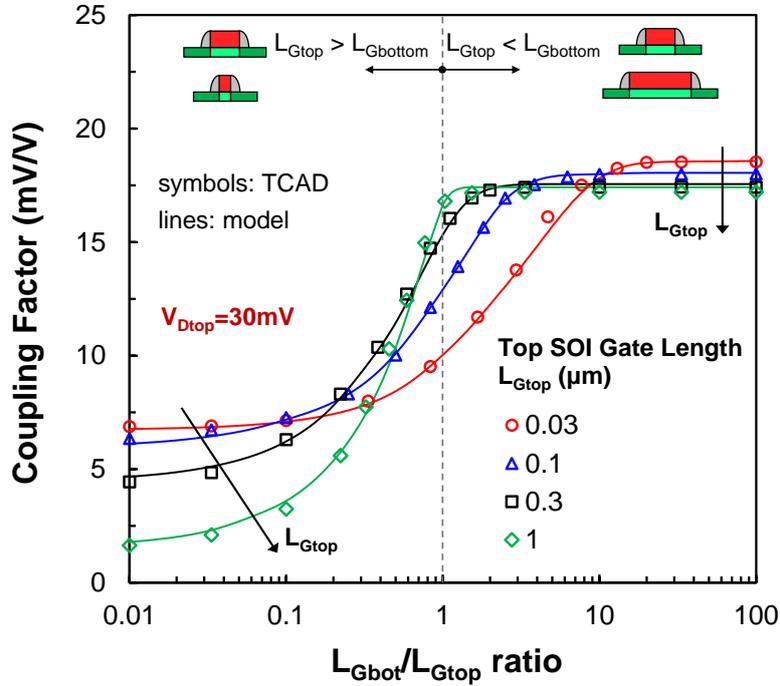


Fig. 6.40 Charge-coupling factor versus L_{Gtop}/L_{Gbot} ratio for different top-tier device gate length as extracted from TCAD simulations along with our modeling approach

6.1.1.b Impact of top/bottom device misalignment

The relative misalignment of devices is another parameter that should be accounted for in the charge-coupling factor modeling. Misplacing by Δx the gates of two stacked devices, the charge-coupling factor is reduced since it depends on the overlapping area between the top-tier device channel and the bottom-tier device gate electrode (Fig. 6.41 (a)).

Once again, $C_{ILD,eff}$ can be modeled by splitting it in two capacitance components, C_{ov} and C_f as illustrated in Fig. 6.41. Hence, it can be calculated by

$$C_{ILD,eff} = C_{ov} + C_f \tag{6-21}$$

where the overlap capacitance component is a parallel plate capacitance, given by

$$C_{ov} = \frac{\epsilon_{ox}}{t_{ILD}} W_G L_{ov} \tag{6-22}$$

where $L_{ov}=L_G-\Delta x$.

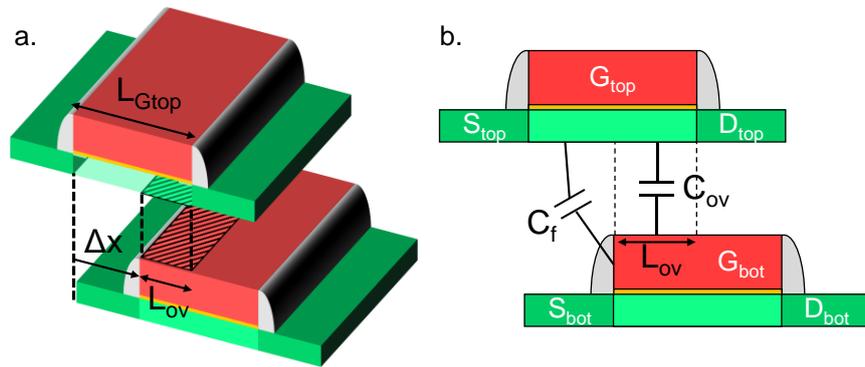


Fig. 6.41 Schematic view of the (a) stacked devices with a misalignment of the bottom-tier device in its length direction and (b) the $C_{ILD,eff}$ components (C_{ov} , C_f) under the misalignment.

Fig. 6.42 shows $C_{ILD,eff}$ as well as its components (C_{ov} , C_f), extracted with TCAD versus misalignment of two stacked devices having gate length of 30nm (Fig. 6.42 (a)) and 1 μ m (Fig. 6.42 (b)). For both cases, the decrease of the overlap capacitance component follows the decrease of the overlapping area between the top-tier device channel and the bottom-tier gate given by (6-22).

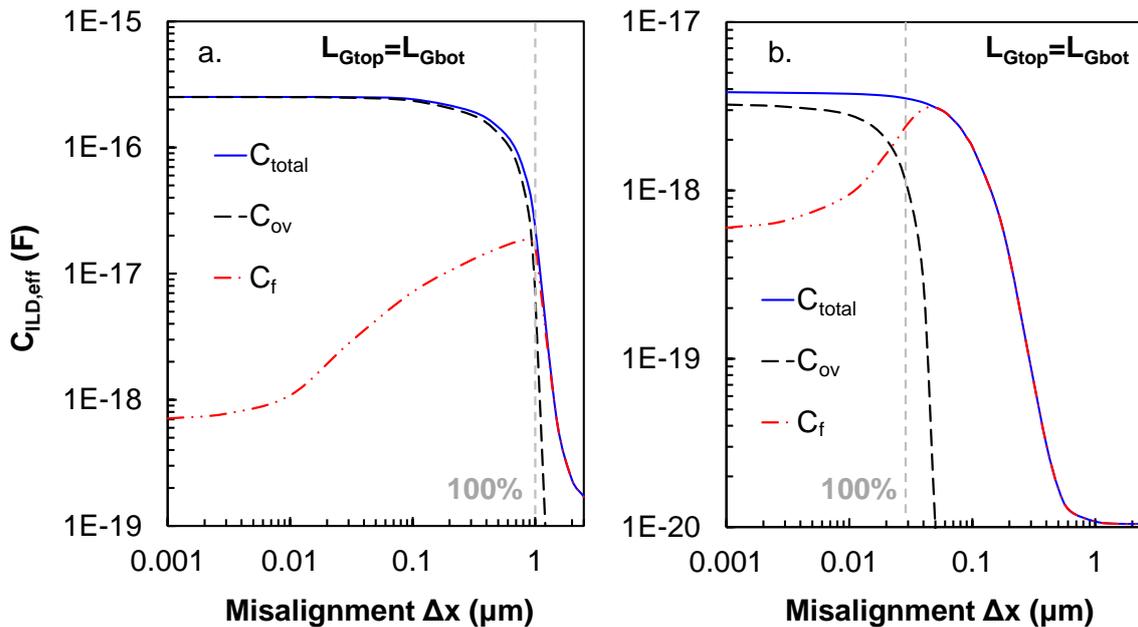


Fig. 6.42 Effective ILD capacitance versus the relative misalignment of the bottom tier device with respect to the top-tier device and its corresponding parallel and fringe components as extracted from TCAD for (a) $L_{Gtop}=1\mu m$ and (b) $L_{Gtop}=30nm$

On the other hand, the fringe capacitance component increases exponentially reaching its peak when there is 100% misalignment. Specifically for 30-nm stacked devices the maximum value of the fringe capacitance will be approximately equal to the overlap capacitance under zero misalignment.

Nevertheless, in a more general scheme, two stacked devices being misaligned can have different gate lengths as depicted in Fig. 6.43, hence the derived effective back-gate length $L_{Gbot,eff}$ in the previous section must handle this asymmetry. To address this issue, the top-tier device can be split in two parts with the axis of symmetry at its center (Fig. 6.43), while the bottom-tier device is divided in two regions having gate length $L'_{Gbot}/2$ and $L''_{Gbot}/2$, so that

$$L_{Gbot} = \frac{L'_{Gbot}}{2} + \frac{L''_{Gbot}}{2} \tag{6-23}$$

as if half of the top-tier device was stacked upon a device with $L'_{Gbot}/2 < L_{Gtop}/2$, when the other half being stacked upon a device with $L''_{Gbot}/2 > L_{Gtop}/2$.

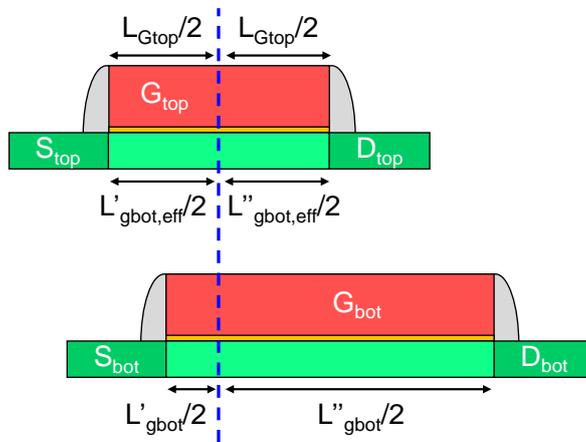


Fig. 6.43 Splitting the top/bottom-tier device length as well as the $L_{Gbot,eff}$ by the top-tier device axis of symmetry when there is relative misalignment.

This enables to set an effective back-gate length $L_{Gbot,eff}/2$ for each half top-tier device channel region, from the extracted values in the previous section. Under this approach, the overlap capacitance component of $C_{ILD,eff}$ can be further split into $C_{ov,1}$ and $C_{ov,2}$ as Fig. 6.44 illustrates.

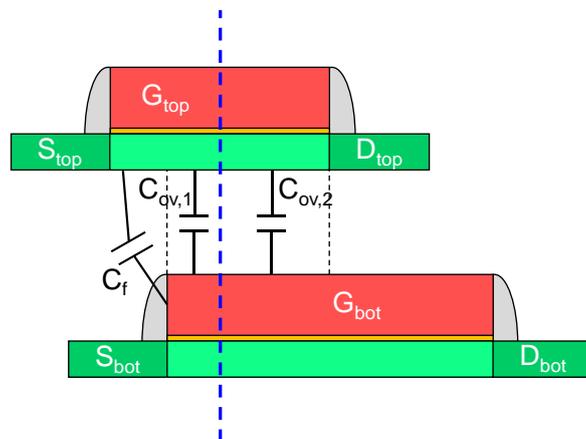


Fig. 6.44 Capacitance component modeling under the relative misalignment of stacked devices splitting the overlap capacitance component by the top-tier device axis of symmetry

The model along with the TCAD simulation results are displayed in Fig. 6.45, where a nice match between the two can be observed.

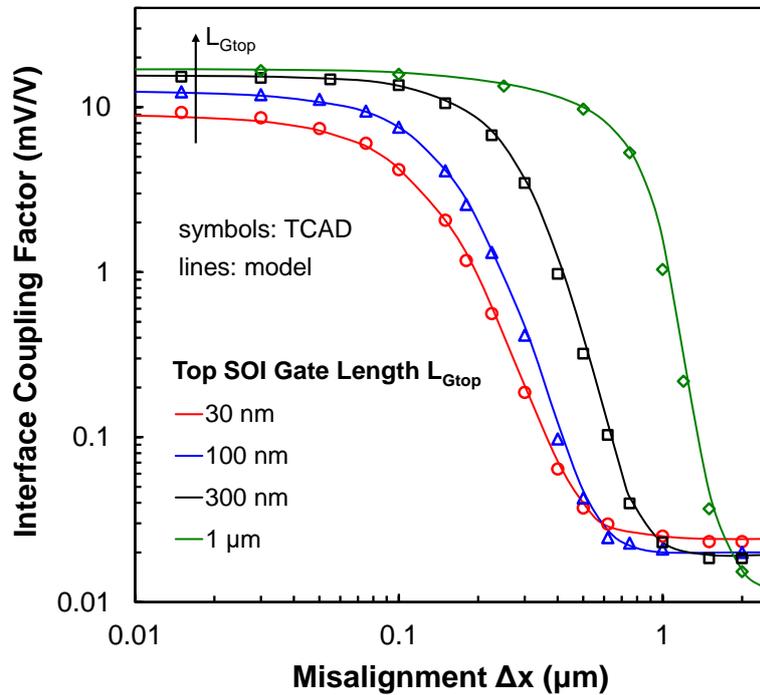


Fig. 6.45 Charge-coupling factor versus misalignment for different gate length ($L_{Gtop}=L_{Gbot}$) as extracted from TCAD simulations along with our modeling approach

Concerning the misalignment in the width direction of the devices, there shall be no SCE or S/D related impact, so the long channel modeling is valid regardless the scaling of the device.

6.3 Inter-tier dynamic coupling effects modeling

The inter-tier dynamic coupling effects emanate from the coupling capacitances created between the stacked devices. Consequently, the values obtained from the parasitic extraction can be utilized to evaluate the importance of dynamic coupling effects. The simplest equivalent model to describe the inter-tier dynamic coupling effects of the stacked structure illustrated in Fig. 6.46 (a), is shown in Fig. 6.46 (b). Considering first the simple case of the coupling between the bottom-tier device gate and the top-tier device drain, C_{12} represents C_{dbdt} , and C_{2G} , R_{2G} are the capacitance and resistance respectively of the top-tier drain electrode to the ground.

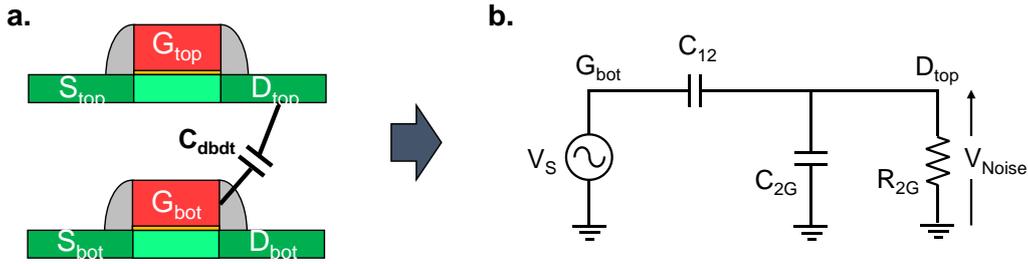


Fig. 6.46 (a) Schematic view of C_{dbdt} in the stacked device configuration with (b) an equivalent circuit model

The coupling transfer function of this equivalent circuit (the reader is encouraged to refer to Chapter 2) is given by:

$$H(f) = \frac{V_{Noise}}{V_s} = \frac{2\pi f \left(\frac{C_{12}}{C_{12} + C_{2G}} \right)}{2\pi f + \left(\frac{1}{R_{2G}(C_{12} + C_{2G})} \right)} \quad (6-24)$$

Therefore, the crosstalk S_{21} parameter can be calculated transforming the transfer function to s-parameters [159] with the two port network illustrated in Fig. 6.47, where $V_{01}=V_s$, $V_2=V_{Noise}$ and when $Z_1=Z_2=50\Omega$.

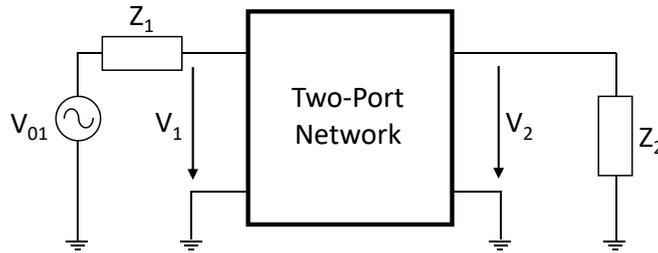


Fig. 6.47 Two-port network configuration for the estimation of S-parameters via the transfer function transformation method.

Consequently, the S_{21} parameter is given by

$$S_{21} = 2 \cdot \frac{V_2}{V_{01}} = 2 \cdot H(f) \quad (6-25)$$

By treating each pair of top/bottom electrodes as two port-networks, the transfer function can be obtained by (6-24) replacing the parameters C_{12} , C_{2G} , R_{2G} with the respective values from the parasitic evaluation. Fig. 6.48 shows the TCAD results versus the simple capacitive modeling indicating that there is a perfect agreement.

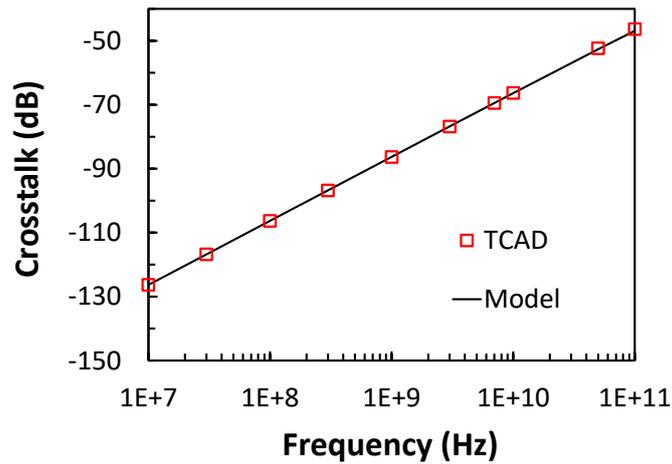


Fig. 6.48 TCAD results for the crosstalk between D_{bot} - D_{top} and the equivalent circuit model results

6.4 Inter-tier GP shielding modeling

The impact of the inter-tier GP on both the coupling-induced ΔV_{TH} of the stacked devices as well as the noise coupling between both devices is investigated in this section. Specifically, a first-order equivalent circuit model is targeted examining the decoupling properties of the inter-tier GP in both DC and AC. This is accomplished by associating capacitive and resistive networks which depend on the material and geometry of the GP layer. Thus, the inter-tier GP can be viewed as a capacitive network forming between the stacked active device and an aggressor, e.g., an iBEOL metal line as Fig. 6.49 illustrates or a bottom-tier active device.

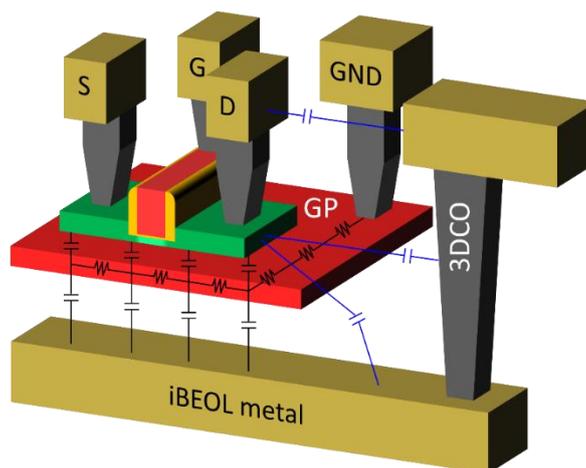


Fig. 6.49 3D schematic view of a top-tier device stacked on top of the last metal of the iBEOL, having in-between an inter-tier GP. Additionally, the formed RC network is illustrated, with the blue lines indicating the remaining coupling components of C_{gbdt}

6.4.1 DC modeling of inter-tier GP – Impact on coupling induced ΔV_{TH} of the stacked devices

Under DC conditions, the decoupling efficiency of an inter-tier GP inserted between two active devices is determined exclusively by the capacitive network formed between the two active

devices, hence the resistance of the GP can be neglected in our modeling approach. However, this does not imply that there is no need for the optimum conductivity of the GP as it has a direct impact on the decoupling efficiency (Chapter 4).

Based on the theoretical concepts presented in Chapter 2, Fig. 6.50 illustrates the equivalent capacitive network between the stacked devices with the insertion of an n-type inter-tier GP. The GP is coupled to the back-interface of the top-tier device channel through C_{GP-cht} , given by

$$C_{GP-cht} = \frac{\epsilon_{ox}}{t_{BOX}} W_{Gtop} L_{Gtop} \quad (6-26)$$

where $t_{BOX}=25\text{nm}$.

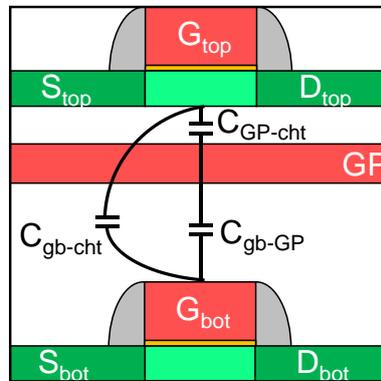


Fig. 6.50 Schematic cross-section view of two stacked devices with inter-tier GP and the capacitances forming among them

Furthermore, the bottom-tier device gate electrode is coupled to the GP through C_{GP-cht} , which can be considered a parallel plate capacitance supposing that it dominates over fringing electric fields between them, given by

$$C_{gb-GP} = \frac{\epsilon_{ox}}{t_{ILD}} W_{Gbot} L_{Gbot} \quad (6-27)$$

with t_{BOX} being 130nm. Lastly there is also the capacitance between the bottom-tier device gate and the top-tier device channel, C_{gb-cht} , with a value that depends on the GP decoupling effectiveness. The latter depends on the GP area with respect to the bottom-tier device gate area and the material resistivity, as analyzed in chapter 4.

Fig. 6.51 recalls the structures under study of §4.2.2.a which were utilized to examine the DC decoupling behavior of the inter-tier Si-GP. The TCAD simulation results extracting C_{gb-cht} from C-V characteristics of the top-tier device are shown in Fig. 6.52.

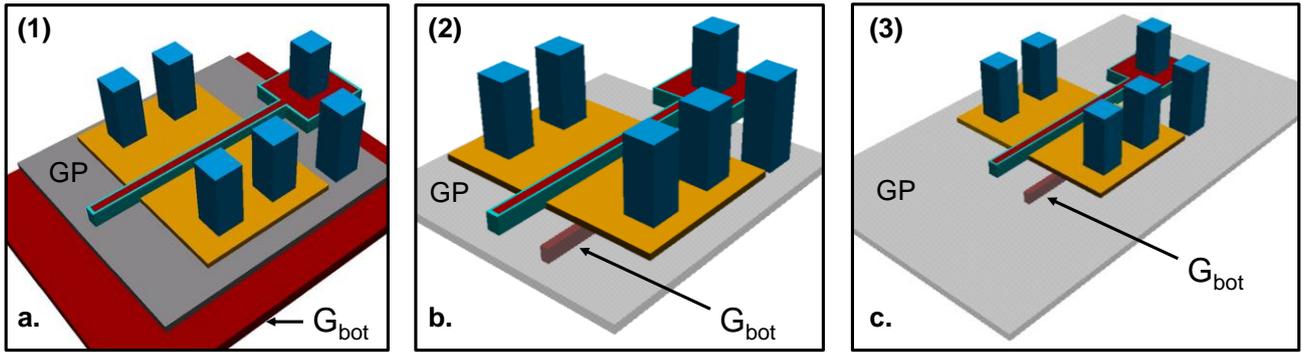


Fig. 6.51 Recall of the simulation setup cases utilized in §4.2.2.a to determine the DC decoupling efficiency of the inter-tier Si-GP.

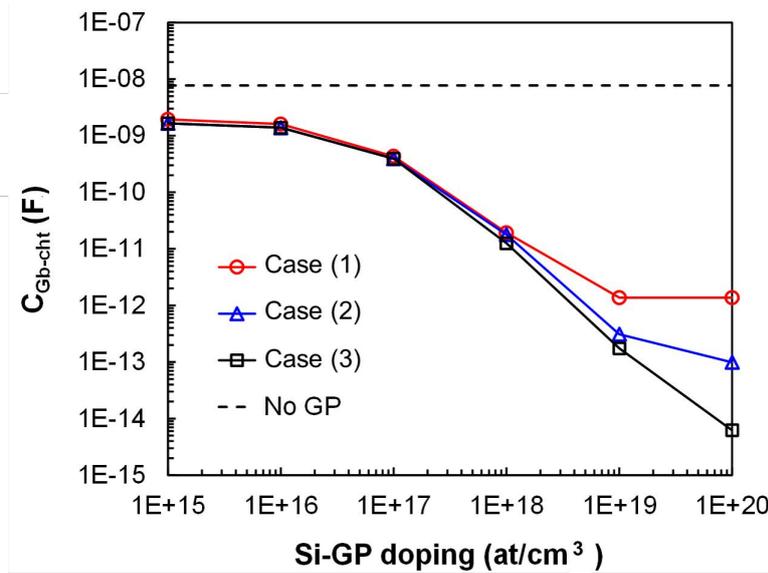


Fig. 6.52 Extracted C_{gb-cht} values from the parasitic extraction versus the doping concentration of the inter-tier Si-GP.

In order to obtain the charge-coupling factor under the influence of the inter-tier GP, the split C-V method was once again followed with the aid of TCAD simulations and the threshold voltage was obtained as a function of V_{Gbot} using the $\max(dC_{gc}/dV_g)$ method. The results are shown in Fig. 6.53 and Fig. 6.54 for various values of Si-GP (10^{15} - 10^{20} at/cm³). In the same diagrams the charge-coupling factor is plotted for comparison, which was calculated from eq. with the extracted values of C_{gb-cht} for each doping concentration of the Si-GP.

From Fig. 6.53 (a) it can be seen that for 10^{15} at/cm⁻³ n-type doping concentration the decoupling behavior of the GP varies with the bottom-tier device gate bias. In detail, when $V_{Gbot} < 0$, the GP becomes essentially transparent to the bottom-tier gate electric field and there is no decoupling. This behavior is the outcome of an electron concentration decrease within the GP in the presence of a negative bias at the bottom-tier gate electrode. On the contrary, when $V_{Gbot} > 0$, accumulation of electron takes place at the back side of the GP layer, enhancing its shielding

behavior. Thus, in that case, the calculated charge-coupling factor is only valid under a small-signal approach and for positive V_{Gbot} .

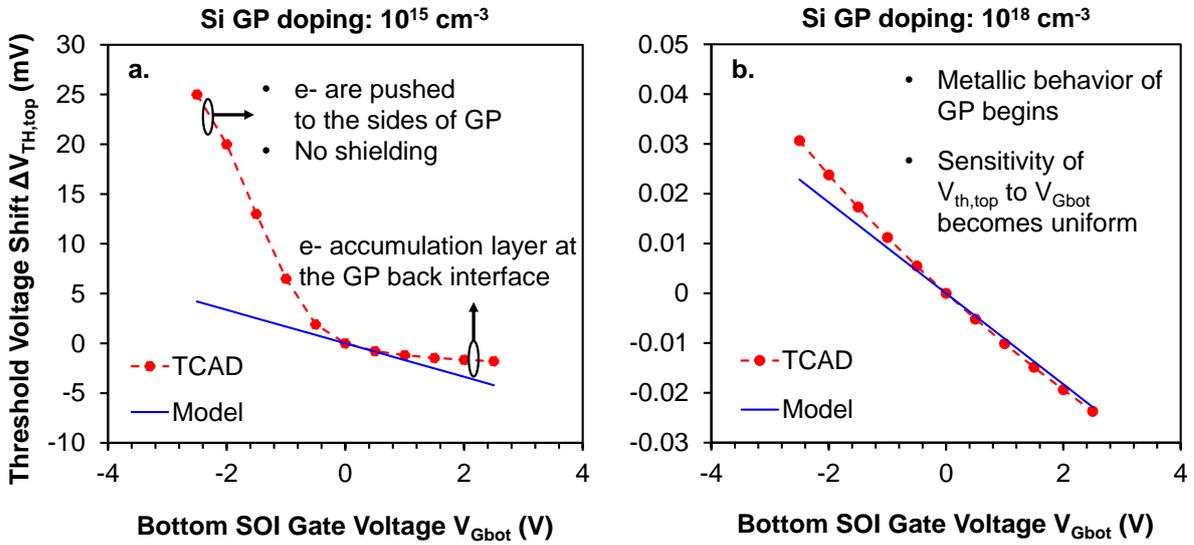


Fig. 6.53 Coupling induced ΔV_{TH} for top devices vs V_{Gbot} for an inter-tier Si-GP with doping concentration of (a) 10^{15} and (b) 10^{18} cm^{-3} .

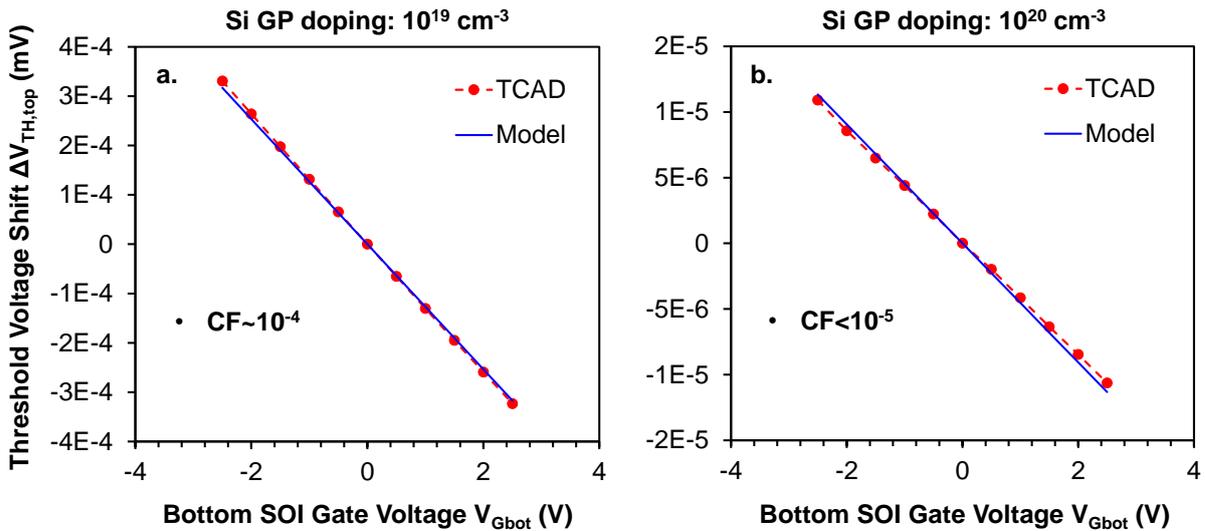


Fig. 6.54 Coupling induced ΔV_{TH} for top devices vs V_{Gbot} for an inter-tier Si-GP with doping concentration of (a) 10^{19} and (b) 10^{20} cm^{-3} .

As analyzed in chapter 4, in order to reach a metal-like behavior, the n-type concentration of the Si-GP must be greater than 10^{18} at/cm^3 . This is reflected in Fig. 6.53 (b) where it is evident that the sensitivity of the top-tier device threshold voltage to bottom-tier gate bias variations becomes uniform. The error between the calculated charge-coupling factor and the TCAD is reduced especially for positive V_{Gbot} . Further increasing the doping concentration of the Si-GP (Fig. 6.54) results in a linear dependence of $\Delta V_{TH,top}$ on V_{Gbot} , and the estimated charge-coupling factor presents minor errors from TCAD results.

All the above can be summarized in Fig. 6.55 where the coupling induced ΔV_{TH} of the stacked devices is plotted against the Si-GP doping for two different cases, the first (Fig. 6.55(a)) when there is a digital device at the bottom-tier ($V_{DD}=1V$) and the second (Fig. 6.55(b)) for a bottom-tier analog device ($V_{DD}=2.5V$). It is evident that in both cases, as the Si-GP doping concentration increases, the calculated $\Delta V_{TH,top}$ from our modeled charge-coupling factor expression matches well the extracted values.

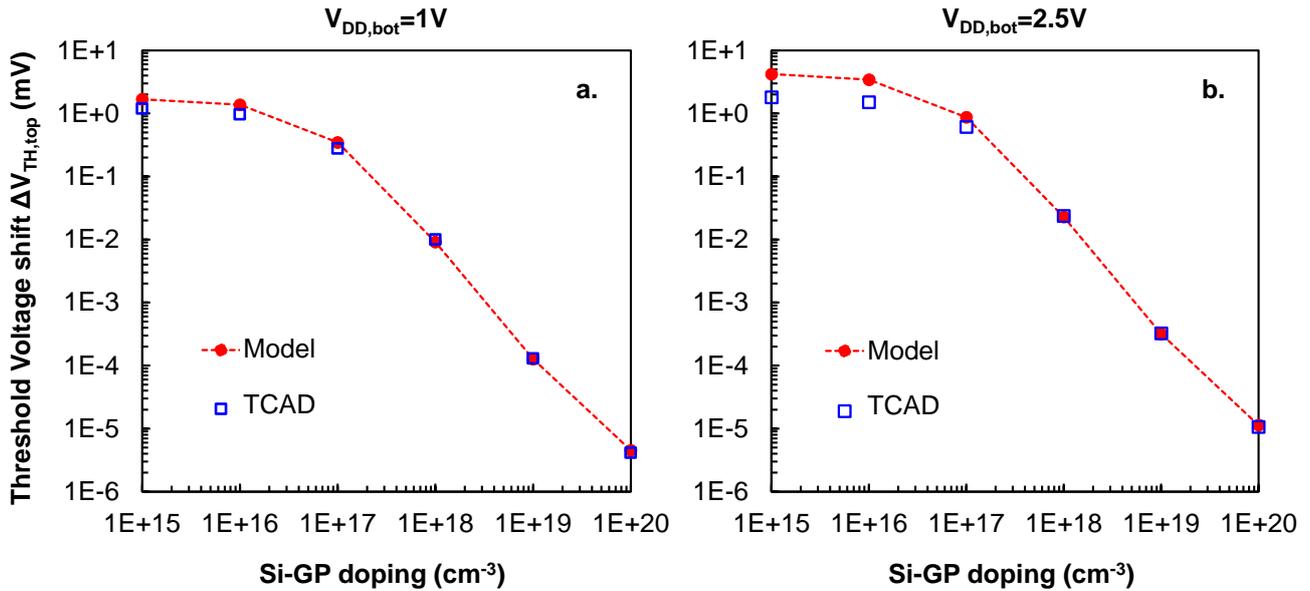


Fig. 6.55 Coupling induced ΔV_{TH} for top-tier devices varying the doping concentration of the inter-tier Si-GP when the bottom-tier gate bias is at (a) 1V and (b) 2.5V.

6.4.2 AC modeling of inter-tier GP

Contrary to the static, the AC modeling of the decoupling efficiency of the inter-tier GP must incorporate the resistance of the GP to the AC ground. Considering in Fig. 6.56 (a) a simplified schematic view of the structure studied in Chapter 4, the top-tier digital device ($EOT=1nm$, $V_{DD}=1V$) is stacked on top of an electrode that can be either the bottom gate or a metal line and in between a GP made of silicon/polysilicon. A simple equivalent circuit that can be adequate to describe the decoupling efficiency offered by the inter-tier GP is suggested in Fig. 6.56(b). Here, the capacitance between the bottom-tier gate electrode (G_1) and the GP is represented by $C_{g1,gp}$, the capacitance between the top-tier drain electrode (D_2) and the GP is defined as $C_{gp,d2}$ and finally the coupling capacitances between G_1 - D_2 and G_1 - S_2 , decoupled by the GP layer, are displayed as $C_{g1,d2}$ and $C_{g1,s2}$ respectively. Additionally, a single lumped resistance $R_{GP,gnd}$ models the distributed resistance of the GP to the AC ground.

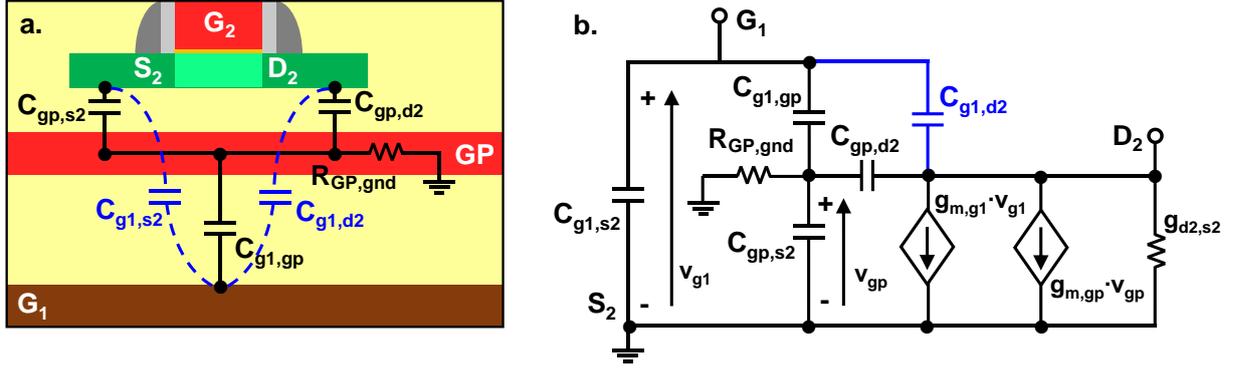


Fig. 6.56 Schematic view of the capacitance network forming with the integration of an inter-tier GP (b) corresponding equivalent circuit of the GP shielding.

To model the active device behavior, two current sources are included, controlled by V_{g1} and V_{gp} via the transconductances $g_{m,g1}$ and $g_{m,gp}$ respectively. Specifically, V_{gp} is the noise voltage generated within the GP layer induced by V_{g1} . Considering this simplified circuit, the aggressor input signal is applied at node G_1 whereas the noise voltage is generated at the victim output node D_2 . Applying Kirchhoff's current law at the output node D_2 , we derived the noise transfer function of the equivalent circuit as

$$H(s) = \frac{V_{d2}}{V_{g1}} = H_0(s) \frac{1 + \alpha(s) \frac{sC_{g1,gp}}{sC_{g1,d2} - g_{m,g1}}}{1 - \alpha(s) \frac{sC_{g1,d2}}{sC_{gp,d2} + sC_{g1,d2} + g_{ds} + G_L}} \quad (6-28)$$

where $\alpha(s) = \frac{sC_{gp,d2} - g_{m,gp}}{sC_{g1,gp} + sC_{gp,d2} + sC_{gp,s2} + \frac{1}{R_{GP,gnd}}}$, and $H_0(s)$ is the suppression level offered by the inter-

tier GP, derived as

$$H_0(s) = \frac{sC_{g1,d2} - g_{m,g1}}{s(C_{gp,d2} + C_{g1,d2}) + g_{ds} + G_L} \quad (6-29)$$

Transforming the transfer function to s-parameters, the S_{21} parameter with matched input-output impedance ($Z_1=Z_2=50\Omega$) is given by

$$S_{21} = 2 \cdot \frac{V_{Noise}}{V_S} = 2 \cdot H(s) \quad (6-30)$$

and for sinusoidal signals $s=j2\pi f$.

The maximum decoupling frequency $f_{D,max}$ can be defined as the frequency limit beyond which the GP layer appears to be capacitively transparent (as explained in §4.2.2.b).

$$f_{D,max} = \frac{1}{4\pi} \frac{C_{g1,d2}}{k} \quad (6-31)$$

where $k=(C_{g1,gp}C_{gp,d2}+C_{gp,d2}C_{g1,d2}+C_{g1,d2}C_{g1,gp})R_{gp,gnd}$.

To validate equations (6-28)-(6-31), an accurate parameter extraction from our simulation data is needed. The capacitances $C_{g1,gp}$, $C_{gp,d2}$, $C_{g1,d2}$ shown in Fig. 6.57 where extracted from the split CV simulations for the two biasing states of the top-tier device. To extract $R_{GP,gnd}$ from the simulation data the input admittance extraction method at high frequency was used from the small-signal equivalent circuit of Fig. 6.56(b). The results are shown in Fig. 6.58, varying the number of GND contacts on the GP. It can be noticed that there is a dependency on the biasing conditions of the top-tier device for doping concentrations below 10^{18} cm^{-3} , related to the non-metallic behavior of the GP.

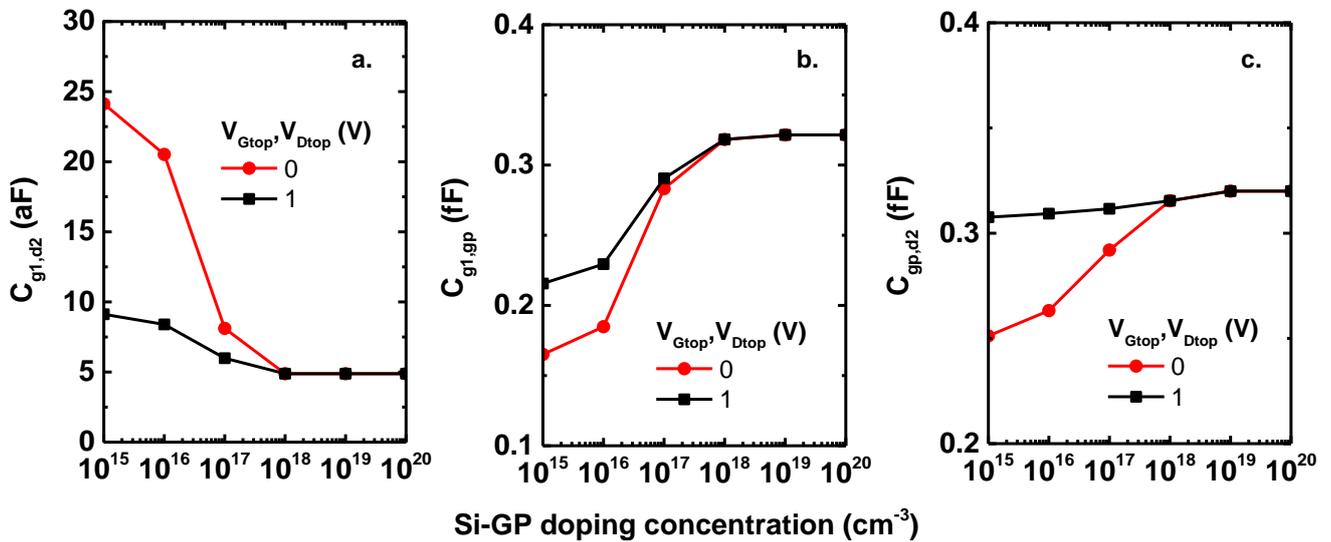


Fig. 6.57 Extracted capacitances $C_{g1,gp}$, $C_{gp,d2}$, $C_{g1,d2}$ versus doping concentration of the inter-tier Si-GP.

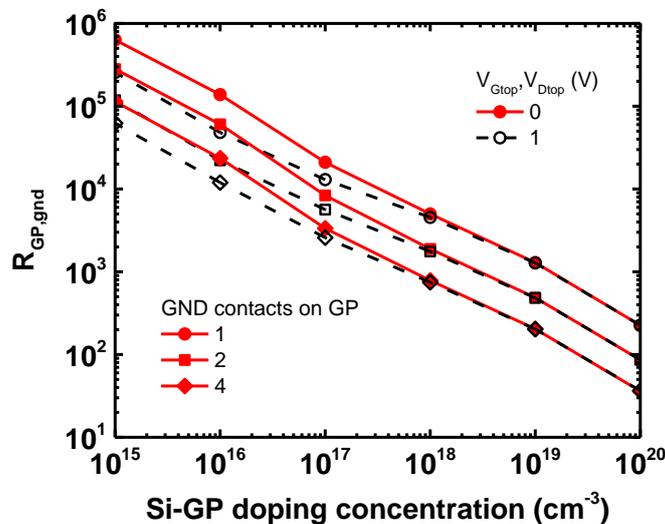


Fig. 6.58 Extracted lumped resistance $R_{GP,gnd}$ values versus doping concentration varying the number of GND contacts on the GP.

The extracted parameters were inserted into equation and the results are plotted in Fig. 6.59. The well-fitting of the calculated and extracted crosstalk levels versus frequency for different doping concentration of the GP and biasing states of the top-tier device, validates our simple equivalent circuit for the frequency range studied. However, larger device geometries may need a more complex circuit representation due to distributed effects.

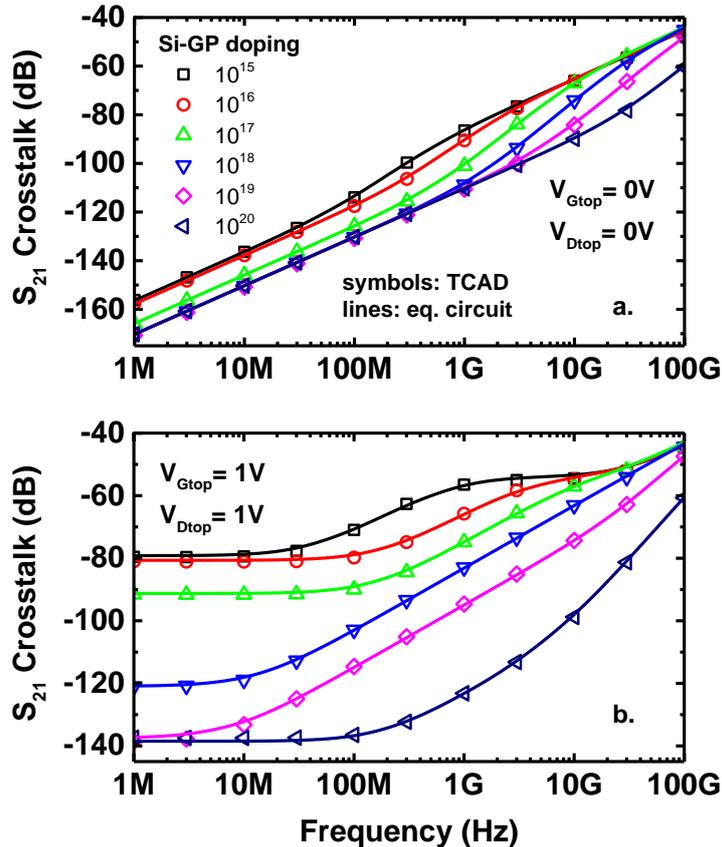


Fig. 6.59 Crosstalk vs. frequency for the top-tier device (a) in cutoff and (b) in saturation with an inter-tier GP made of silicon. Lines indicate the equivalent circuit results whereas symbols show TCAD data.

Furthermore, the resistivity of the GP can be estimated from the values of the lumped resistance $R_{GP,gnd}$ used to fit the TCAD data for each doping concentration of the Si-GP. For that reason, the distance of the grounding contact on the GP to the active device was utilized, and the results are demonstrated in Fig. 6.60. The comparison with the experimental data [125] for the resistivity of monocrystal silicon reveals the validity of our equivalent model.

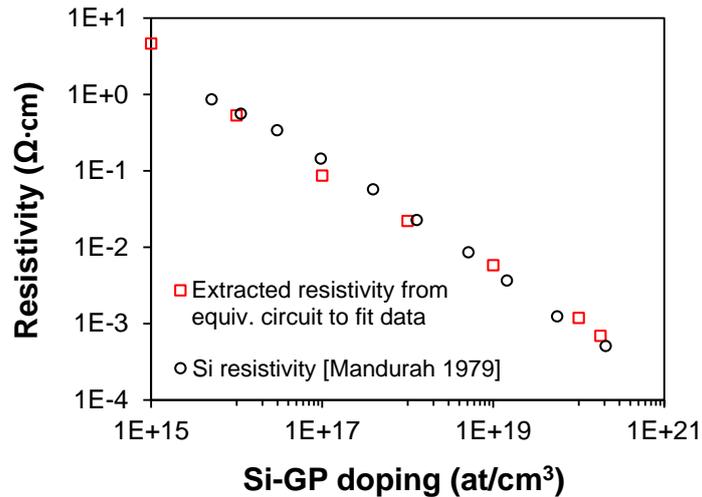


Fig. 6.60 Resistivity of the inter-tier GP extracted from the equivalent circuit (rectangles) compared to the experimental data in [125].

6.5 Conclusion

In this chapter the coupling capacitances between active devices have been thoroughly investigated through an extensive TCAD analysis, mainly focusing on the capacitive coupling effects. Through a parasitic extraction procedure, the bias and layout dependency of the coupling capacitances has been assessed. Furthermore, the contribution of 3D contacts on the total capacitance has been evaluated for different density values. The results prove that the 3D via density of a 28nm-node limits significantly C_{dbdt} , which is responsible for dynamic coupling effects between the devices. Nevertheless, as the density of 3D contacts increases ($CPP/2=28\text{nm}$), their contribution to the overall coupling capacitances is enhanced, since the lateral coupling dominates over the vertical (inter-tier) one due to the ILD thickness being 130nm.

Moreover, a modeling approach of the inter-tier coupling effects has been presented focusing on the coupling-induced ΔV_{TH} of stacked digital devices. Under our analysis, two critical simplifications for the charge centroid have been considered:

- It is confined near the center of the top-tier device channel under zero gate bias.
- It remains near the center of the top-tier device channel for the maximum bias range of the bottom-tier devices (0V-2.5V) due to the thick ILD.

Along with the above approximations, the concept of the effective front/back gate length has been employed in our analysis for the top-tier device to handle the electric field deformation due to SCE and the presence of the bottom-tier S/D regions. The result of our modeling approach covers a

wide range of top/bottom—tier device gate areas and under various geometric configuration. The comparison with the extracted threshold voltage shift from I-V simulations confirms our initial simplifications. Lastly, modeling considerations have been suggested for the AC coupling between the stacked devices as well as the capacitive network formed by the insertion of an inter-tier GP.

CHAPTER 7

CONCLUSIONS AND PERSPECTIVES

Through this work the impact of noise and electromagnetic coupling has been investigated at both a device and a circuit level in a 3DSI process scheme. The dominant mechanism of the coupling effects has been identified as the capacitive one, contrary to the inductive which has been evaluated as weak between active devices.

Moreover, the inter-tier static coupling results in a threshold voltage modulation for the stacked devices due to their channel being exposed at their back-interface. The coupling induced threshold voltage shift of stacked devices, has been identified as the strongest interference as it can potentially increase leakage current/power and decrease the on-state current. Exploring critical device parameters such as the V_{TH} , I_{off} and I_{on} it has been demonstrated that their coupling-induced shift can be considered as tolerable concerning purely digital circuits. This implies that the static coupling effects are not widening much the process corners in digital design. On the contrary, in the case that digital are stacked upon analog devices, an ILD of 350nm thickness shall maintain the coupling effects to tolerable levels. On the bright side, the impact of static coupling on the LFN of stacked digital devices is negligible.

In contrast, analog devices stacked on top of either digital or analog devices are critical cases of inter-tier coupling with their coupling-induced ΔV_{TH} resulting in higher values. Considering that analog circuits such as current mirrors and differential amplifiers require matched transistors, the high coupling-induced ΔV_{TH} values prohibit the direct stacking above other devices. Hence, analog devices must be placed at the bottom-tier of a 3DSI process scheme, or employ an inter-tier GP so that their body potential is sufficiently decoupled from the aggressor devices.

Additionally, the inter-tier dynamic coupling effects have been investigated at a device level, exploring both the small-signal and large-signal response of victim devices to the aggressor signals. Again, the stacked devices and specifically the ones with a high W/L ratio reveal greater noise coupling levels, due to their back-gate coupling effect.

Over and above, all the geometry and biasing related dependencies of both static and dynamic coupling effects have been assessed. It has been proven that the coupling induced ΔV_{TH} can be significantly limited when the two devices are misaligned. Yet, dynamic coupling effects must be taken into consideration since they are enhanced due to the direct overlapping of the top-tier drain with the bottom-tier gate electrode. As a consequence, the switching noise can be increased.

Concerning the results at a circuit level, different combinations of tier-stacking have been studied under a heterogeneous integration scheme. For the purpose of this analysis sensitive circuits in digital (SRAM) and mixed-signal/RF (RO) design have been selected as victim cases. In addition, aggressor signals have been selected to emulate a bottom-tier device being either digital, analog, mixed-signal/RF. The results confirm that inter-tier isolation methods and techniques are not mandatory for purely digital 3D sequential circuits. On the contrary, mixed signal/RF applications require further decoupling as the coupling effects impact significantly their normal operation and coincide in the frequency spectrum. The proper decoupling can be achieved either by process optimization (ILD thickness increase) or proper layout (misalignment of the stacked devices, 3D contact positioning).

In order to get an even greater reduction of the vertical capacitive coupling, the integration of an inter-tier decoupling layer (GP) is suggested for sensitive tier stacking combinations. The decoupling efficiency of the inter-tier GP has been thoroughly evaluated as a function of its material properties, its size and the number of grounding contacts. Specifically, the use of a semiconductive material has been evaluated with its resistivity defined by the doping concentration. Additionally, the inter-tier GP also functions as a back-gate for the top-tier devices, adjusting their threshold voltage via its workfunction and also by utilizing the back-biasing technique. Therefore, depending on the top-tier device (Digital, Analog, Mixed-Signal/RF) different flavors of GP can be utilized, optimizing their performance. Specifically for RF applications a high doping concentration of the inter-tier GP is needed in order to achieve the maximum decoupling efficiency. As a result, this work proposes a technological solution to create experimentally a 34nm-thick polysilicon GP of 1.8×10^{20} at/cm³ n-doping and 295Ω/sq sheet resistance.

This work has also evaluated the impact of the coupling-induced effects on the performance of a RS CIS with its pixels partitioned in different tiers of a 3DSI process. The device electrical parameters (V_{TH} , I_{off} and I_{on}) of a single pixel were initially studied comparing their coupling-induced shift with the one resulting from temperature variation in sensing circuits. The results prove that the coupling-induced effects can result in a shift of the device electrical parameters as significant as a temperature variation of 100 degrees. This deviation is far from negligible especially for switch transistors for which leakage is a critical parameter. Concerning the in-pixel SF transistor at circuit level, it was shown that there is negligible impact on the CG and the AC performance due to the 3DSI partitioning compared to the conventional single-tier one. Furthermore, the SF-TG coupling can result in a readout error only when the SF is placed above a TG that wouldn't be synchronized with the pixel readout. However, for RS exposure mode this is not possible due to asynchronous pixel activation. Therefore, although the electrical coupling has proven to be strong, the special case of a RS CIS presents an inherent immunity to coupling effects in a 3DSI partitioning.

Lastly, parasitic extraction was performed on 3DSI structures at a device level. The coupling capacitances responsible for the inter-tier coupling effects, were analyzed in depth. Through the electric field decomposition method, the components of each coupling capacitance were evaluated investigating also all their biasing/geometry related dependencies. Moreover, the impact of 3D contacts was studied, proving that their contribution to the overall coupling capacitances can be significant when their density is increased. In addition, a comprehensive modeling approach of inter-tier coupling effects was presented. Though an extensive simulation study, expressions were suggested to describe the impact of layout effects on the inter-tier coupling. The models predict accurately the amount of the coupling-induced ΔV_{TH} for stacked devices for a wide range of device geometries and layout configurations of the top/bottom devices. Additionally, some considerations were suggested concerning the modeling of AC coupling and also the impact of an inter-tier GP on the coupling effects.

BIBLIOGRAPHY

- [1] S. Borkar, "Design challenges of technology scaling," *IEEE Micro*, vol. 19, no. 4, pp. 23–29, 1999, doi: 10.1109/40.782564.
- [2] G. E. Moore, "Cramming More Components Onto Integrated Circuits, Electronics, April 19, 1965," *Electronics*, 1965.
- [3] H.-S. P. Wong, "Beyond the conventional transistor," 2002.
- [4] M. T. Bohr, "Interconnect scaling-the real limiter to high performance ULSI," in *Proceedings of International Electron Devices Meeting*, pp. 241–244, doi: 10.1109/IEDM.1995.499187.
- [5] J. D. Meindl, "Low Power Microelectronics: Retrospect and Prospect," *Proc. IEEE*, vol. 83, no. 4, pp. 619–635, 1995, doi: 10.1109/5.371970.
- [6] S. Y. Oh and K. J. Chang, "Looking at the materials and thermal alternatives for scaled, next-century VLSI/ULSI interconnects," *IEEE Circuits Devices Mag.*, vol. 11, no. 1, pp. 16–21, 1995, doi: 10.1109/101.340307.
- [7] M. T. Bohr and Y. A. El-Mansy, "Technology for advanced high-performance microprocessors," *IEEE Trans. Electron Devices*, vol. 45, no. 3, pp. 620–625, 1998, doi: 10.1109/16.661223.
- [8] L. R. Harriott, "Limits of lithography," *Proc. IEEE*, vol. 89, no. 3, pp. 366–374, 2001, doi: 10.1109/5.915379.
- [9] H. M. Fahad and M. M. Hussain, "Are nanotube architectures more advantageous than nanowire architectures for field effect transistors?," *Sci. Rep.*, vol. 2, pp. 2–8, 2012, doi: 10.1038/srep00475.
- [10] J. Robertson, "High dielectric constant oxides," *Eur. Phys. J. Appl. Phys.*, vol. 28, no. 3, pp. 265–291, Dec. 2004, doi: 10.1051/epjap:2004206.
- [11] M. W. Geis, D. C. Flanders, D. A. Antoniadis, and H. I. Smith, "CRYSTALLINE SILICON ON INSULATORS BY GRAPHOEPIITAXY.," in *Advances in Chemistry Series*, 1979, pp. 210–212, doi: 10.1109/jedm.1979.189581.

- [12] J. P. Colinge and E. Demoulin, "ST-CMOS (STACKED TRANSISTORS CMOS): A DOUBLE-POLY-NMOS-COMPATIBLE CMOS TECHNOLOGY.," in *Technical Digest - International Electron Devices Meeting*, 1981, pp. 557–560, doi: 10.1109/iedm.1981.190144.
- [13] G. T. Goeloe, E. W. Maby, D. J. Silversmith, R. W. Mountain, and D. A. Antoniadis, "VERTICAL SINGLE-GATE CMOS INVERTERS ON LASER-PROCESSED MULTILAYER SUBSTRATES.," in *Technical Digest - International Electron Devices Meeting*, 1981, pp. 554–556, doi: 10.1109/iedm.1981.190143.
- [14] S. Kawamura, N. Sasaki, T. Iwai, M. Nakano, and M. Takagi, "Three-Dimensional CMOS IC's Fabricated by Using Beam Recrystallization," *IEEE Electron Device Lett.*, vol. 4, no. 10, pp. 366–368, 1983, doi: 10.1109/EDL.1983.25766.
- [15] S. Akiyama, S. Ogawa, M. Yoneda, N. Yoshii, and Y. Terui, "MULTILAYER CMOS DEVICE FABRICATED ON LASER RECRYSTALLIZED SILICON ISLANDS.," in *Technical Digest - International Electron Devices Meeting*, 1983, pp. 352–355, doi: 10.1109/iedm.1983.190514.
- [16] K. Sugahara, T. Nishimura, S. Kusunoki, Y. Akasaka, and H. Nakata, "SOI/SOI/Bulk-Si Triple-Level Structure for Three-Dimensional Devices," *IEEE Electron Device Lett.*, vol. 7, no. 3, pp. 193–195, 1986, doi: 10.1109/EDL.1986.26341.
- [17] T. Kunio, K. Oyama, Y. Hayashi, and M. Morimoto, "Three dimensional ICs, having four stacked active device layers," in *Technical Digest - International Electron Devices Meeting*, 1989, pp. 837–840, doi: 10.1109/iedm.1989.74183.
- [18] J. Jourdon *et al.*, "Hybrid bonding for 3D stacked image sensors: Impact of pitch shrinkage on interconnect robustness," in *Technical Digest - International Electron Devices Meeting, IEDM*, Jan. 2019, vol. 2018-December, pp. 7.3.1-7.3.4, doi: 10.1109/IEDM.2018.8614570.
- [19] L. Brunet *et al.*, "First demonstration of a CMOS over CMOS 3D VLSI CoolCube™ integration on 300mm wafers," *Dig. Tech. Pap. - Symp. VLSI Technol.*, vol. 2016-Sept, pp. 12–13, 2016, doi: 10.1109/VLSIT.2016.7573428.
- [20] P. Batude *et al.*, "Enabling 3D Monolithic Integration," *ECS Trans.*, vol. 16, no. 8, pp. 47–54, Dec. 2019, doi: 10.1149/1.2982853.
- [21] P. Batude *et al.*, "3D sequential integration: Application-driven technological achievements

and guidelines,” in *Technical Digest - International Electron Devices Meeting, IEDM*, Jan. 2018, pp. 3.1.1-3.1.4, doi: 10.1109/IEDM.2017.8268316.

- [22] P. Garrou, C. Bower, and P. Ramm, *Handbook of 3D Integration*, vol. 1–2. Wiley, 2008.
- [23] B. Banijamali, S. Ramalingam, K. Nagarajan, and R. Chaware, “Advanced reliability study of TSV interposers and interconnects for the 28nm technology FPGA,” in *Proceedings - Electronic Components and Technology Conference*, 2011, pp. 285–290, doi: 10.1109/ECTC.2011.5898527.
- [24] F. Clermidy, O. Billoint, H. Sarhan, and S. Thuries, “Technology scaling: The CoolCube™ paradigm,” Nov. 2015, doi: 10.1109/S3S.2015.7333504.
- [25] J. Shi, D. Nayak, M. Ichihashi, S. Banna, and C. A. Moritz, “On the design of ultra-high density 14nm finfet based transistor-level monolithic 3d ics,” in *Proceedings of IEEE Computer Society Annual Symposium on VLSI, ISVLSI*, Sep. 2016, vol. 2016-September, pp. 449–454, doi: 10.1109/ISVLSI.2016.94.
- [26] W. Arden, M. Brillouët, P. Cogez, M. Graef, B. Huizing, and R. Mahnkopf, “‘More-than-Moore’ White Paper,” 2010.
- [27] J.-E. Michallet, “CoolCube™: A True 3DVLSI Alternative to Scaling | 3D InCites,” 2015. <https://www.3dincites.com/2015/03/coolcube-a-true-3dvlsi-alternative-to-scaling/> (accessed Dec. 01, 2020).
- [28] L. Millet *et al.*, “A 5500-frames/s 85-GOPS/W 3-D Stacked BSI Vision Chip Based on Parallel In-Focal-Plane Acquisition and Processing,” *IEEE J. Solid-State Circuits*, vol. 54, no. 4, pp. 1096–1105, Apr. 2019, doi: 10.1109/JSSC.2018.2886325.
- [29] H. Kim *et al.*, “A 1/2.65in 44Mpixel CMOS Image Sensor with 0.7μm Pixels Fabricated in Advanced Full-Depth Deep-Trench Isolation Technology,” in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, Feb. 2020, vol. 2020-February, pp. 104–106, doi: 10.1109/ISSCC19947.2020.9062924.
- [30] A. Theuwissen, “CMOS image sensors: State-of-the-art and future perspectives,” *ESSCIRC 2007 - Proc. 33rd Eur. Solid-State Circuits Conf.*, pp. 21–27, 2007, doi: 10.1109/ESSCIRC.2007.4430242.

- [31] P. Coudrain *et al.*, "Investigation of a sequential three-dimensional process for back-illuminated CMOS image sensors with miniaturized pixels," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2403–2413, 2009, doi: 10.1109/TED.2009.2030990.
- [32] P. Vivet *et al.*, "Advanced 3D Technologies and Architectures for 3D Smart Image Sensors," in *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Mar. 2019, no. July, pp. 674–679, doi: 10.23919/DATE.2019.8714886.
- [33] Silvaco, "ATLAS User ' s Manual," vol. II, no. 408, pp. 567–1000, 2014.
- [34] Silvaco, "Clever User ' s Manual," no. 408. 2014.
- [35] Ansoft Corporation, "User's guide – High Frequency Structure Simulator." p. 801, 2005, [Online]. Available: <http://anlage.umd.edu/HFSSv10UserGuide.pdf>.
- [36] Cadence, "Spectre ® Circuit Simulator Components and Device Models Reference," no. November. 2017.
- [37] T. Poiroux, O. Rozeau, S. Martinie, and M. Jaud, "Leti - UTSOI 2.2.0 User's Manual," no. October. 2016.
- [38] X. Gu *et al.*, "Characterization of TSV-induced loss and substrate noise coupling in advanced three-dimensional CMOS SOI technology," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 3, no. 11, pp. 1917–1925, 2013, doi: 10.1109/TCPMT.2013.2264755.
- [39] M. Brocard *et al.*, "Characterization and modelling of Si-substrate noise induced by RF signal propagating in TSV of 3D-IC stack," *Proc. - Electron. Components Technol. Conf.*, pp. 665–672, 2012, doi: 10.1109/ECTC.2012.6248903.
- [40] C. Bermond *et al.*, "RF characterization of the substrate coupling noise between TSV and active devices in 3D integrated circuits," *Microelectron. Eng.*, vol. 130, pp. 74–81, 2014, doi: 10.1016/j.mee.2014.09.025.
- [41] Y. Araga *et al.*, "Measurements and analysis of substrate noise coupling in TSV-based 3-D integrated circuits," *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 4, no. 6, pp. 1026–1037, 2014, doi: 10.1109/TCPMT.2014.2316150.
- [42] K. Yoon *et al.*, "Modeling and analysis of coupling between TSVs, metal, and RDL interconnects in TSV-based 3D IC with silicon interposer," *Proc. Electron. Packag. Technol.*

- Conf. EPTC*, vol. 3, pp. 702–706, 2009, doi: 10.1109/EPTC.2009.5416458.
- [43] C. Xu, H. Li, R. Suaya, and K. Banerjee, “Compact AC modeling and performance analysis of through-silicon vias in 3-D ICs,” *IEEE Trans. Electron Devices*, vol. 57, no. 12, pp. 3405–3417, 2010, doi: 10.1109/TED.2010.2076382.
- [44] C. Xu and K. Banerjee, “Compact capacitance and capacitive coupling-noise modeling of through-oxide vias in FDSOI based ultra-high density 3-D ICs,” *Tech. Dig. - Int. Electron Devices Meet. IEDM*, pp. 817–820, 2011, doi: 10.1109/IEDM.2011.6131674.
- [45] P. Le Maitre, M. Brocard, A. Farcy, and J. C. Marin, “Device and electromagnetic co-simulation of TSV: Substrate noise study and compact modeling of a TSV in a matrix,” in *Proceedings - International Symposium on Quality Electronic Design, ISQED*, 2012, pp. 404–411, doi: 10.1109/ISQED.2012.6187525.
- [46] Z. Chen *et al.*, “Modeling and analysis of signal transmission with Through Silicon Via (TSV) noise coupling,” *Proc. - IEEE Int. Symp. Circuits Syst.*, pp. 2646–2649, 2013, doi: 10.1109/ISCAS.2013.6572422.
- [47] Y. Ma, “First order Electro-thermal compact models and noise considerations for three-dimensional integration circuits,” INSA Lyon, May 2018. Accessed: Nov. 30, 2020. [Online]. Available: <http://theses.insa-lyon.fr/publication/2018LYSEI042/these.pdf>.
- [48] M. Rousseau, M. A. Jaud, P. Leduc, A. Farcy, and A. Marty, “Impact of substrate coupling induced by 3D-IC architecture on advanced CMOS technology,” *2009 Eur. Microelectron. Packag. Conf. EMPC 2009*, 2009.
- [49] X. Duan, X. Gu, J. Cho, and J. Kim, “A through-silicon-via to active device noise coupling study for CMOS SOI technology,” *Proc. - Electron. Components Technol. Conf.*, pp. 1791–1795, 2011, doi: 10.1109/ECTC.2011.5898756.
- [50] M. Lee, J. Cho, and J. Kim, “Noise coupling analysis between TSV and active circuit,” *2012 IEEE Electr. Des. Adv. Packag. Syst. Symp. EDAPS 2012*, no. 2, pp. 45–48, 2012, doi: 10.1109/EDAPS.2012.6469428.
- [51] O. Thomas, M. Vinet, O. Rozeau, P. Batude, and A. Valentian, “Compact 6T SRAM cell with robust read/write stabilizing design in 45nm monolithic 3D IC technology,” in *2009 IEEE*

International Conference on Integrated Circuit Design and Technology, ICICDT 2009, 2009, pp. 195–198, doi: 10.1109/ICICDT.2009.5166294.

- [52] A. Koneru and K. Chakrabarty, “Analysis of electrostatic coupling in monolithic 3D integrated circuits and its impact on delay testing,” in *Proceedings of the European Test Workshop*, Jul. 2016, vol. 2016-July, doi: 10.1109/ETS.2016.7519292.
- [53] K. C. Yu, M. L. Fan, P. Su, and C. Te Chuang, “Evaluation of monolithic 3-D logic circuits and 6T SRAMs with InGaAs-n/Ge-p ultra-thin-body MOSFETs,” *IEEE J. Electron Devices Soc.*, vol. 4, no. 2, pp. 76–82, Mar. 2016, doi: 10.1109/JEDS.2016.2524567.
- [54] Y. S. Yu, S. Panth, and S. K. Lim, “Electrical Coupling of Monolithic 3-D Inverters,” *IEEE Trans. Electron Devices*, vol. 63, no. 8, pp. 3346–3349, 2016, doi: 10.1109/TED.2016.2578946.
- [55] J. Hattori, K. Fukuda, T. Irisawa, H. Ota, and T. Maeda, “Interlayer coupling effect on the performance of monolithic three-dimensional inverters and its dependence on the interlayer dielectric thickness,” in *Japanese Journal of Applied Physics*, Apr. 2017, vol. 56, no. 4, p. 04CC02, doi: 10.7567/JJAP.56.04CC02.
- [56] P. Chaourani, “Sequential 3D Integration - Design Methodologies and Circuit Techniques,” 2019.
- [57] F. Andrieu *et al.*, “Design technology co-optimization of 3D-monolithic standard cells and SRAM exploiting dynamic back-bias for ultra-low-voltage operation,” in *Technical Digest - International Electron Devices Meeting, IEDM*, Jan. 2018, pp. 20.3.1-20.3.4, doi: 10.1109/IEDM.2017.8268428.
- [58] A. Koneru, S. Kannan, and K. Chakrabarty, “Impact of electrostatic coupling and wafer-bonding defects on delay testing of monolithic 3D integrated circuits,” *ACM J. Emerg. Technol. Comput. Syst.*, vol. 13, no. 4, pp. 1–23, 2017, doi: 10.1145/3041026.
- [59] T. J. Ahn, R. Perumal, S. K. Lim, and Y. S. Yu, “Parameter extraction and power/performance analysis of monolithic 3-D inverter (M3INV),” *IEEE Trans. Electron Devices*, vol. 66, no. 2, pp. 1006–1011, 2019, doi: 10.1109/TED.2018.2885817.
- [60] T. J. Ahn, B. H. Choi, S. K. Lim, and Y. S. Yu, “Electrical coupling and simulation of monolithic 3D logic circuits and static random access memory,” *Micromachines*, vol. 10, no. 10, pp. 1–

- 11, 2019, doi: 10.3390/mi10100637.
- [61] T. J. Ahn and Y. S. Yu, "Circuit simulation considering electrical coupling in monolithic 3D logics with junctionless FETs," *Micromachines*, vol. 11, no. 10, pp. 1–10, 2020, doi: 10.3390/mi11100887.
- [62] C. Xu and K. Banerjee, "Physical modeling of the capacitance and capacitive coupling noise of through-oxide vias in FDSOI-based ultra-high density 3-D ICs," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 123–131, 2013, doi: 10.1109/TED.2012.2227966.
- [63] J. Jiang, K. Parto, W. Cao, and K. Banerjee, "Ultimate Monolithic-3D Integration With 2D Materials: Rationale, Prospects, and Challenges," *IEEE J. Electron Devices Soc.*, vol. 7, no. April, pp. 878–887, 2019, doi: 10.1109/jeds.2019.2925150.
- [64] A. Vandooren *et al.*, "Buried metal line compatible with 3D sequential integration for top tier planar devices dynamic V_{th} tuning and RF shielding applications," *Dig. Tech. Pap. - Symp. VLSI Technol.*, vol. 2019-June, pp. T56–T57, 2019, doi: 10.23919/VLSIT.2019.8776490.
- [65] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, no. 1. Hoboken, NJ, USA: John Wiley & Sons, Inc., 2006.
- [66] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*. Springer US, 2004.
- [67] H. W. Ott, *Electromagnetic Compatibility Engineering*. 2009.
- [68] N. R. S. R. L. Geiger, P. E. Allen, "VLSI design techniques for analog and digital circuits," *Microelectronics J.*, vol. 23, no. 4, pp. 317–318, Jul. 1992, doi: 10.1016/0026-2692(92)90033-W.
- [69] Y. Tsividis, *Mixed Analog–Digital VLSI Devices and Technology*. WORLD SCIENTIFIC, 2002.
- [70] J. L. Leray *et al.*, "CMOS/SOI hardening at 100 Mrad(SiO₂)," *IEEE Trans. Nucl. Sci.*, vol. 37, no. 6, pp. 2013–2019, 1990, doi: 10.1109/23.101223.
- [71] L. R. Hite, H. Lu, T. W. Houston, D. S. Hurta, and W. E. Bailey, "An SEU Resistant 256K SOI SRAM," *IEEE Trans. Nucl. Sci.*, vol. 39, no. 6, pp. 2121–2125, 1992, doi: 10.1109/23.211411.
- [72] N. Planes *et al.*, "28nm FDSOI technology platform for high-speed low-voltage digital applications," in *2012 Symposium on VLSI Technology (VLSIT)*, Jun. 2012, pp. 133–134, doi:

10.1109/VLSIT.2012.6242497.

- [73] T. Ernst and S. Cristoloveanu, "The ground-plane concept for the reduction of short-channel effects in fully-depleted SOI devices," *Electrochem. Soc. Proc.*, vol. 99, no. 3, p. 329, 1999, Accessed: Dec. 01, 2020. [Online]. Available: <https://books.google.com/books?hl=en&lr=&id=E3eSvSu2S6IC&oi=fnd&pg=PA329&dq=+The+ground-plane+concept+for+the+reduction+of+short-channel+effects+in+fully+depleted+SOI+devices&ots=1r3AV4QMb&sig=P-z--lxJKz424SHtgShaDpsvpP8>.
- [74] Hyung-Kyu Lim and J. G. Fossum, "Threshold voltage of thin-film Silicon-on-insulator (SOI) MOSFET's," *IEEE Trans. Electron Devices*, vol. 30, no. 10, pp. 1244–1251, Oct. 1983, doi: 10.1109/T-ED.1983.21282.
- [75] A. L. McWhorter, "1/F Noise and Germanium Surface Properties," *Semiconductor Surface Physics*. pp. 207–228, 1957, Accessed: Dec. 01, 2020. [Online]. Available: <https://ci.nii.ac.jp/naid/10013093640/>.
- [76] C. Theodorou, "Low-frequency noise in advanced CMOS/SOI nanoscale multi-gate devices and noise model development for circuit applications," Αριστοτέλειο Πανεπιστήμιο Θεσσαλονίκης, 2013.
- [77] F. N. Hooge, T. G. M. Kleinpenning, and L. K. J. Vandamme, "Experimental studies on 1/f noise," *Reports Prog. Phys.*, vol. 44, no. 5, pp. 479–532, May 1981, doi: 10.1088/0034-4885/44/5/001.
- [78] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A Unified Model For The Flicker Noise In Metal-Oxide-Semiconductor Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 654–665, 1990, doi: 10.1109/16.47770.
- [79] G. Ghibaudo, O. Roux, C. Nguyen-Duc, F. Balestra, and J. Brini, "Improved Analysis of Low Frequency Noise in Field-Effect MOS Transistors," *Phys. status solidi*, vol. 124, no. 2, pp. 571–581, Apr. 1991, doi: 10.1002/pssa.2211240225.
- [80] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998, doi: 10.1109/4.658619.

- [81] G. Ghibaudo, O. Roux-dit-Buisson, and J. Brini, "Impact of Scaling Down on Low Frequency Noise in Silicon MOS Transistors," *Phys. status solidi*, vol. 132, no. 2, pp. 501–507, 1992, doi: 10.1002/pssa.2211320226.
- [82] K. M. Findlater *et al.*, "Source follower noise limitations in CMOS active pixel sensors," in *Detectors and Associated Signal Processing*, Feb. 2004, vol. 5251, p. 187, doi: 10.1117/12.512969.
- [83] C. Leyris, F. Martinez, M. Valenza, A. Hoffmann, J. C. Vildeuil, and F. Roy, "Impact of random telegraph signal in CMOS image sensors for low-light levels," *ESSCIRC 2006 - Proc. 32nd Eur. Solid-State Circuits Conf.*, no. 2, pp. 376–379, 2006, doi: 10.1109/ESSCIR.2006.307609.
- [84] B. Razavi, *RF Microelectronics*. Pearson Education, Inc, 2012.
- [85] K. Banerjee, S. Im, and N. Srivastava, "Interconnect modeling and analysis in the nanometer era: Cu and beyond," *Adv. Met. Conf.*, no. January 2006, pp. 25–31, 2006.
- [86] K. Takeuchi *et al.*, "Direct observation of RTN-induced SRAM failure by accelerated testing and its application to product reliability assessment," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 189–190, 2010, doi: 10.1109/VLSIT.2010.5556222.
- [87] C. Fenouillet-Beranger *et al.*, "FDSOI bottom MOSFETs stability versus top transistor thermal budget featuring 3D monolithic integration," in *European Solid-State Device Research Conference*, Nov. 2014, pp. 110–113, doi: 10.1109/ESSDERC.2014.6948770.
- [88] F. Deprat *et al.*, "First integration of Ni_{0.9}Co_{0.1} on pMOS transistors," in *2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference, IITC/AMC 2016*, Jul. 2016, pp. 133–135, doi: 10.1109/IITC-AMC.2016.7507708.
- [89] P. Batude *et al.*, "3DVLSI with CoolCube process: An alternative path to scaling," *Dig. Tech. Pap. - Symp. VLSI Technol.*, vol. 2015-Augus, pp. T48–T49, 2015, doi: 10.1109/VLSIT.2015.7223698.
- [90] L. Pasini *et al.*, "High performance CMOS FDSOI devices activated at low temperature," in *Digest of Technical Papers - Symposium on VLSI Technology*, Sep. 2016, vol. 2016-September, doi: 10.1109/VLSIT.2016.7573407.
- [91] A. Tsiara *et al.*, "Performance and reliability of a fully integrated 3D sequential technology,"

in *Digest of Technical Papers - Symposium on VLSI Technology*, Oct. 2018, vol. 2018-June, pp. 75–76, doi: 10.1109/VLSIT.2018.8510625.

- [92] X. Garros *et al.*, “RF Performance of a Fully Integrated 3D Sequential Technology,” in *Technical Digest - International Electron Devices Meeting, IEDM*, Dec. 2019, vol. 2019-December, doi: 10.1109/IEDM19573.2019.8993512.
- [93] SYNERGIE CONCEPT, “NOISYS.7, Low-Frequency Noise Measuring System.” <http://synergieconcept.eu/> (accessed Dec. 10, 2020).
- [94] N. Subramanian, G. Ghibaudo, and M. Mouis, “Parameter extraction of nano-scale MOSFETs using modified Y function method,” in *2010 Proceedings of the European Solid State Device Research Conference, ESSDERC 2010*, 2010, pp. 309–312, doi: 10.1109/ESSDERC.2010.5618348.
- [95] C. G. Theodorou *et al.*, “Low-frequency noise behavior of n-channel UTBB FD-SOI MOSFETs,” 2013, doi: 10.1109/ICNF.2013.6578986.
- [96] C. G. Theodorou *et al.*, “Impact of front-back gate coupling on low frequency noise in 28 nm FDSOI MOSFETs,” in *European Solid-State Device Research Conference, 2012*, pp. 334–337, doi: 10.1109/ESSDERC.2012.6343401.
- [97] E. G. Ioannidis, C. G. Theodorou, T. A. Karatsori, S. Haendler, C. A. Dimitriadis, and G. Ghibaudo, “Drain-current flicker noise modeling in nMOSFETs from a 14-nm FDSOI technology,” *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1574–1579, 2015, doi: 10.1109/TED.2015.2411678.
- [98] E. G. Ioannidis *et al.*, “Analytical low-frequency noise model in the linear region of lightly doped nanoscale double-gate metal-oxide-semiconductor field-effect transistors,” *J. Appl. Phys.*, vol. 108, no. 6, p. 064512, Sep. 2010, doi: 10.1063/1.3483279.
- [99] J. G. Fossum and V. P. Trivedi, *Fundamentals of Ultra-Thin-Body MOSFETs and FinFETs*, vol. 9781107030. Cambridge: Cambridge University Press, 2013.
- [100] T. Rudenko, “Revision of interface coupling in ultra-thin body silicon-on-insulator MOSFETs,” *Semicond. Phys. Quantum Electron. Optoelectron.*, vol. 16, no. 3, pp. 300–309, Sep. 2013, doi: 10.15407/spqeo16.03.300.

- [101] M. Tsuno, M. Suga, M. Tanaka, K. Shibahara, M. Miura-Mattausch, and M. Hirose, "Physically-based threshold voltage determination for MOSFET's of all gate lengths," *IEEE Trans. Electron Devices*, vol. 46, no. 7, pp. 1429–1434, 1999, doi: 10.1109/16.772487.
- [102] C. Cavalcante *et al.*, "Low temperature high voltage analog devices in a 3D sequential integration," *2020 Int. Symp. VLSI Technol. Syst. Appl. VLSI-TSA 2020*, pp. 155–156, 2020, doi: 10.1109/VLSI-TSA48913.2020.9203691.
- [103] B. Razavi, *Design of Analog CMOS Integrated Circuits*. 2005.
- [104] D. Choudhury, "3D integration technologies for emerging microsystems," *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1–4, 2010, doi: 10.1109/MWSYM.2010.5514747.
- [105] V. Deshpande *et al.*, "DC and RF characterization of InGaAs replacement metal gate (RMG) nFETs on SiGe-OI FinFETs fabricated by 3D monolithic integration," *Solid. State. Electron.*, vol. 128, pp. 87–91, Feb. 2017, doi: 10.1016/j.sse.2016.10.034.
- [106] J. P. Raskin, A. Viviani, D. Flandre, and J. P. Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Trans. Electron Devices*, vol. 44, no. 12, pp. 2252–2261, 1997, doi: 10.1109/16.644646.
- [107] C. Raynaud *et al.*, "Is SOI CMOS a promising technology for SOCs in high frequency range?," in *Proceedings - Electrochemical Society*, Feb. 2005, vol. PV 2005-03, no. 12, pp. 331–344, doi: 10.1149/ma2005-01/12/571.
- [108] K. Ben Ali, C. R. Neve, A. Gharsallah, and J. P. Raskin, "RF performance of SOI CMOS technology on commercial 200-mm enhanced signal integrity high resistivity SOI substrate," *IEEE Trans. Electron Devices*, vol. 61, no. 3, pp. 722–728, 2014, doi: 10.1109/TED.2014.2302685.
- [109] J.-P. Raskin, "Analogue and RF performances of Fully Depleted SOI MOSFET Performances analogiques et RF de MOSFETs SOI complètement désertés," 2019.
- [110] H. S. Kim, K. A. Jenkins, and Y. H. Xie, "Effective crosstalk isolation through p+ Si substrates with semi-insulating porous Si," *IEEE Electron Device Lett.*, vol. 23, no. 3, pp. 160–162, 2002, doi: 10.1109/55.988824.
- [111] S. Stefanou *et al.*, "Ultralow Silicon Substrate Noise Crosstalk Using Metal Faraday Cages in

- an SOI Technology,” *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 486–491, 2004, doi: 10.1109/TED.2003.822348.
- [112] C. Liu and S. K. Lim, “Ultra-high density 3D SRAM cell designs for monolithic 3D integration,” 2012, doi: 10.1109/IITC.2012.6251581.
- [113] D. Bhattacharya and N. K. Jha, “Ultra-High Density Monolithic 3-D FinFET SRAM with Enhanced Read Stability,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 63, no. 8, pp. 1176–1187, Aug. 2016, doi: 10.1109/TCSI.2016.2565641.
- [114] M. Brocard *et al.*, “High density SRAM bitcell architecture in 3D sequential CoolCube™ 14nm technology,” Jan. 2017, doi: 10.1109/S3S.2016.7804376.
- [115] J. Kong, Y. H. Gong, and S. W. Chung, “Architecting large-scale SRAM arrays with monolithic 3D integration,” Aug. 2017, doi: 10.1109/ISLPED.2017.8009157.
- [116] S. Srinivasa, X. Li, M. F. Chang, J. Sampson, S. K. Gupta, and V. Narayanan, “Compact 3-D-SRAM Memory with Concurrent Row and Column Data Access Capability Using Sequential Monolithic 3-D Integration,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 26, no. 4, pp. 671–683, Apr. 2018, doi: 10.1109/TVLSI.2017.2787562.
- [117] S. Rangachar Srinivasa *et al.*, “ROBIN: Monolithic-3D SRAM for Enhanced Robustness with In-Memory Computation Support,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 66, no. 7, pp. 2533–2545, Jul. 2019, doi: 10.1109/TCSI.2019.2897497.
- [118] P. Batude *et al.*, “3D CMOS integration: Introduction of dynamic coupling and application to compact and robust 4T SRAM,” in *Proceedings - 2008 IEEE International Conference on Integrated Circuit Design and Technology, ICICDT, 2008*, pp. 281–284, doi: 10.1109/ICICDT.2008.4567296.
- [119] M. L. Fan, V. P. H. Hu, Y. N. Chen, P. Su, and C. Te Chuang, “Stability and performance optimization of heterochannel monolithic 3-D SRAM cells considering interlayer coupling,” *IEEE Trans. Electron Devices*, vol. 61, no. 10, pp. 3448–3455, Oct. 2014, doi: 10.1109/TED.2014.2348856.
- [120] Z. Guo, A. Carlson, L. T. Pang, K. T. Duong, T. J. K. Liu, and B. Nikolić, “Large-scale SRAM variability characterization in 45 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp.

3174–3192, Nov. 2009, doi: 10.1109/JSSC.2009.2032698.

- [121] J. Singh, S. P. Mohanty, and D. K. Pradhan, *Robust SRAM designs and analysis*. 2013.
- [122] J. H. Wu, J. Scholvin, J. A. Del Alamo, and K. A. Jenkins, “A Faraday cage isolation structure for substrate crosstalk suppression,” *IEEE Microw. Wirel. Components Lett.*, vol. 11, no. 10, pp. 410–412, Oct. 2001, doi: 10.1109/7260.959312.
- [123] H. S. Kim, K. A. Jenkins, and Y. H. Xie, “Effective crosstalk isolation through p+ Si substrates with semi-insulating porous Si,” *IEEE Electron Device Lett.*, vol. 23, no. 3, pp. 160–162, Mar. 2002, doi: 10.1109/55.988824.
- [124] T. S. Chen, C. Y. Lee, and C. H. Kao, “An efficient noise isolation technique for SOC application,” *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 255–260, Feb. 2004, doi: 10.1109/TED.2003.821565.
- [125] M. M. Mandurah, K. C. Saraswat, and T. I. Kamins, “Phosphorus Doping of Low Pressure Chemically Vapor-Deposited Silicon Films,” *J. Electrochem. Soc.*, vol. 126, no. 6, pp. 1019–1023, Jun. 1979, doi: 10.1149/1.2129167.
- [126] S. K. Kim, C. C. Liu, L. Xue, and S. Tiwari, “Crosstalk reduction in mixed-signal 3-D integrated circuits with interdevice layer ground planes,” *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1459–1467, 2005, doi: 10.1109/TED.2005.850641.
- [127] P. Sideris *et al.*, “Inter-tier Dynamic Coupling and RF Crosstalk in 3D Sequential Integration,” in *Technical Digest - International Electron Devices Meeting, IEDM*, Dec. 2019, vol. 2019-December, doi: 10.1109/IEDM19573.2019.8993493.
- [128] Yole Developpement, “Status of the CMOS Image Sensor Industry 2020,” 2020. https://s3.i-micronews.com/uploads/2020/11/YDR20106-Status-of-the-CMOS-Image-Sensor-Industry-2020_sample.pdf (accessed Dec. 08, 2020).
- [129] G. P. Weckler, “Operation of p-n Junction Photodetectors in a Photon Flux Integrating Mode,” *IEEE J. Solid-State Circuits*, vol. 2, no. 3, pp. 65–73, 1967, doi: 10.1109/JSSC.1967.1049795.
- [130] O. Yadid-Pecht, R. Ginosar, and Y. S. Diamand, “A Random Access Photodiode Array for Intelligent Image Capture,” *IEEE Trans. Electron Devices*, vol. 38, no. 8, pp. 1772–1780, 1991,

doi: 10.1109/16.119013.

- [131] R. M. Guidash *et al.*, "0.6 μm CMOS pinned photodiode color imager technology," in *Technical Digest - International Electron Devices Meeting, IEDM*, 1997, pp. 927–929, doi: 10.1109/iedm.1997.650533.
- [132] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. Leblanc, "Design of Ion-Implanted MOSFET's With Very Small Physical Dimensions," *IEEE J. Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, 1974, doi: 10.1109/JSSC.1974.1050511.
- [133] G. Agranov *et al.*, "Pixel continues to shrink... Pixel Development for Novel CMOS Image Sensors."
- [134] K. Lee *et al.*, "SNR Performance Comparison of 1.4 μm Pixel : FSI, Light-guide, and BSI."
- [135] N. Teranishi, A. Kohono, Y. Ishihara, E. Oda, and K. Arai, "NO IMAGE LAG PHOTODIODE STRUCTURE IN THE INTERLINE CCD IMAGE SENSOR.," in *Technical Digest - International Electron Devices Meeting*, 1982, pp. 324–327, doi: 10.1109/iedm.1982.190285.
- [136] D. Mcgrath and S. Tobin, "Dark Current Limiting Mechanisms in CMOS Image Sensors," 2018, doi: 10.2352/ISSN.2470-1173.2018.11.IMSE-354.
- [137] S. Iwabuchi, Y. Maruyama, Y. Ohgishi, M. Muramatsu, N. Karasawa, and T. Hirayama, "A back-illuminated high-sensitivity small-pixel color CMOS image sensor with flexible layout of metal wiring," 2006, doi: 10.1109/isscc.2006.1696162.
- [138] B. Pain, "Fabrication and Initial Results for a Back-illuminated Monolithic APS in a Mixed SOI Bulk CMOS Technology," in *IEEE Workshop on CCDs and Advanced Image Sensors*, 2005, pp. 102–104.
- [139] S. G. Wu and R. ; Tsmc, "BSI Technology with Bulk Si Wafer," 2009.
- [140] M. Cohen *et al.*, "Fully optimized Cu based process with dedicated cavity etch for 1.75 μm and 1.45 μm pixel pitch CMOS Image Sensors," 2006, doi: 10.1109/IEDM.2006.346976.
- [141] H. Rhodes *et al.*, "The Mass Production of BSI CMOS Image Sensors."
- [142] T. Haruta *et al.*, "A 1/2.3inch 20Mpixel 3-layer stacked CMOS Image Sensor with DRAM," in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, Mar. 2017, vol.

60, pp. 76–77, doi: 10.1109/ISSCC.2017.7870268.

- [143] P. Coudrain, “Contribution au développement d’une technologie d’intégration tridimensionnelle pour les capteurs d’images CMOS à pixels actifs,” *Microelectron. - sensors*, 2009.
- [144] A. Amara and O. Rozeau, *Planar Double-Gate Transistor*. Dordrecht: Springer Netherlands, 2009.
- [145] G. Groeseneken, J. P. Colinge, H. E. Maes, J. C. Alderman, and S. Holt, “Temperature Dependence of Threshold Voltage in Thin-Film SOI MOSFET’s,” *IEEE Electron Device Lett.*, vol. 11, no. 8, pp. 329–331, 1990, doi: 10.1109/55.57923.
- [146] B. Fowler, “Single Photon CMOS Imaging Through Noise Minimization,” vol. 160, P. Seitz and A. J. Theuwissen, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2011, pp. 159–195.
- [147] A. Ohata, S. Cristoloveanu, A. Vandooren, M. Cassé, and F. Daugé, “Coupling effect between the front and back interfaces in thin SOI MOSFETs,” in *Microelectronic Engineering*, Jun. 2005, vol. 80, no. SUPPL., pp. 245–248, doi: 10.1016/j.mee.2005.04.075.
- [148] T. Poiroux *et al.*, “New and accurate method for electrical extraction of silicon film thickness on fully-depleted SOI and double gate transistors,” in *Proceedings - IEEE International SOI Conference, 2004*, pp. 73–74, doi: 10.1109/soi.2004.1391561.
- [149] S. Eminente, S. Cristoloveanu, R. Clerc, A. Ohata, and G. Ghibaudo, “Ultra-thin fully-depleted SOI MOSFETs: Special charge properties and coupling effects,” *Solid. State. Electron.*, vol. 51, no. 2, pp. 239–244, Feb. 2007, doi: 10.1016/j.sse.2007.01.016.
- [150] V. P. Trivedi and J. G. Fossum, “Scaling fully depleted SOI CMOS,” *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2095–2103, 2003, doi: 10.1109/TED.2003.816915.
- [151] N. Fasarakis *et al.*, “Analytical modeling of threshold voltage and interface ideality factor of nanoscale ultrathin body and buried oxide SOI MOSFETs with back gate control,” *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 969–975, 2014, doi: 10.1109/TED.2014.2306015.
- [152] T. Poiroux *et al.*, “Leti-UTSOI2.1: A compact model for UTBB-FDSOI technologies - Part II: DC and AC model description,” *IEEE Trans. Electron Devices*, vol. 62, no. 9, pp. 2760–2768, Sep. 2015, doi: 10.1109/TED.2015.2458336.

- [153] G. Hibliot, J. Lacord, M. Akbal, Q. Rafhay, F. Boeuf, and G. Ghibaudo, "Compact model of short-channel effects for FDSOI devices including the influence of back-bias and fringing fields for Si and III-V technology," *Solid. State. Electron.*, vol. 107, pp. 1–7, 2015, doi: 10.1016/j.sse.2015.02.001.
- [154] A. Bansal, B. C. Paul, and K. Roy, "Modeling and optimization of fringe capacitance of nanoscale DGMOS devices," *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 256–262, 2005, doi: 10.1109/TED.2004.842713.
- [155] T. Ernst, R. Ritzenthaler, O. Faynot, and S. Cristoloveanu, "A model of fringing fields in short-channel planar and triple-gate SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 6, pp. 1366–1375, 2007, doi: 10.1109/TED.2007.895241.
- [156] W. Zhao, X. Li, S. Gu, S. H. Kang, M. M. Nowak, and Y. Cao, "Field-based capacitance modeling for sub-65-nm on-chip interconnect," *IEEE Transactions on Electron Devices*, vol. 56, no. 9, pp. 1862–1872, 2009, doi: 10.1109/TED.2009.2026162.
- [157] J. Lacord, G. Ghibaudo, and F. Boeuf, "Comprehensive and accurate parasitic capacitance models for two- and three-dimensional CMOS device structures," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1332–1344, 2012, doi: 10.1109/TED.2012.2187454.
- [158] G. Hibliot, Q. Rafhay, L. Gaben, G. Ghibaudo, and F. Boeuf, "Optimization of Trigate-On-Insulator MOSFET aspect ratio with MASTAR," in *European Solid-State Device Research Conference*, Nov. 2015, vol. 2015-November, pp. 242–245, doi: 10.1109/ESSDERC.2015.7324759.
- [159] S. S. Lu, Y. S. Lin, H. W. Chiu, Y. C. Chen, and C. C. Meng, "The determination of S-Parameters from the poles of voltage-gain transfer function for RF IC design," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 52, no. 1, pp. 191–199, 2005, doi: 10.1109/TCSI.2004.840084.

LIST OF PUBLICATIONS

International Conferences

- **P. Sideris**, L. Brunet, G. Sicard, P. Batude and C. Theodorou, "Impact of Inter-Tier Coupling on Static and Noise Performance in 3D Sequential Integration Technology," 2019 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), Grenoble, France, 2019, pp. 1-4, doi: 10.1109/EUROSOI-ULIS45800.2019.9041871.
- **P. Sideris**, J. Lugo-Alvarez, P. Batude, L. Brunet, P. Acosta-Alba, S. Kerdiles, C. Fenouillet-Beranger, G. Sicard, O. Rozeau, F. Andrieu, J-P. Colinge, G. Ghibaudo and C. Theodorou, "Inter-tier Dynamic Coupling and RF Crosstalk in 3D Sequential Integration," 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2019, pp. 3.4.1-3.4.4, doi: 10.1109/IEDM19573.2019.8993493.
- **P. Sideris**, A. Peizerat, P. Batude, C. Theodorou and G. Sicard, "Inter-tier Coupling Analysis in Back-illuminated Monolithic 3D Image Sensor Pixels", International Conference on Modern Circuits and Systems Technologies (MOCAST) on Electronics and Communications (accepted).

Peer-reviewed Journals

- **P. Sideris**, L. Brunet, L. Ciampolini, G. Sicard, P. Batude, C. Theodorou, Inter-tier electrostatic coupling effects in 3D sequential integration devices and circuits, *Solid-State Electronics*, Volume 168, 2020, 107715, ISSN 0038-1101, doi: 10.1016/j.sse.2019.107715.
- T. Mota Frutuoso, **P. Sideris**, J. Lugo-Alvarez, X. Garros, L. Brunet, C. Fenouillet-Beranger, P. Batude, C. Theodorou, P. Ferrari and F. Gaillard, "RF Performance of Devices Processed in Low-Temperature Sequential Integration," in *IEEE Transactions on Electron Devices*, doi: 10.1109/TED.2021.3080669.
- **P. Sideris**, P. Batude, G. Sicard, G. Ghibaudo and C. Theodorou, "A Modeling Approach for Inter-Tier Coupling Effects in 3D Sequential Integration" (submitted).
- **P. Sideris**, A. Siligaris, P. Batude, and C. Theodorou, "Shielding Properties of Inter-Tier Si/PolySi-GP Layers in Sequential 3D Technologies" (submitted).

ABSTRACT

Impact of noise and electromagnetic coupling in sequential 3D technologies: Study, modeling and impact on circuit performance

As an alternative to the scaling-down of transistor feature-size in order to keep up the Moore's law, three dimensional (3-D) integration technologies offer higher integration density, lower power consumption and provide a unique platform for heterogeneous integration of different active-layer materials through the vertical stacking of integrated circuit tiers. 3-D Sequential Integration, (also named 3-D monolithic integration or 3-D VLSI), is a type of 3D integration scheme, where the multiple stacked tiers are fabricated sequentially on top of each other on the same wafer. Each tier consists of active and BEOL layers insulated by interlayer dielectric (ILD) layers. The fundamental property that differentiates this technology is the very close distance between the 2 (or more) layers which introduces very small parasitic capacitances allowing digital signals to have a high frequency while at the same time being generated with a low energy. As a result, 3-D Sequential Integration brings new possibilities for mixed architectures with performances in both speed and low power consumption that cannot be easily met with other 3-D technologies schemes (TSV, copper to copper bonding etc.). However, the high frequency signals, the spatial localization, the strong interconnection density can all be a major source of interference between stacked tiers, modulating the expected behavior of devices as well as adding noise. Therefore solutions and techniques have to be found in order to limit these effects. This work, aims to respond to this challenge and ensure the technology robustness. The impact of the electromagnetic and noise interference between stacked tiers in 3-D Sequential Integration technology is thoroughly investigated in this work at both device and circuit level. To accomplish that, the most critical digital, analog and mixed-signal/RF designs have been selected to construct monolithic 3-D circuits. Experiments in conjunction with TCAD simulations reveal the coupling mechanisms responsible for the electromagnetic and noise propagation between stacked tiers. Additionally, the strength of the propagated signals is assessed and its impact on the device/circuit performance is deeply explored. This study also examines the impact of 3-D Sequential Integration is examined on the performance of a CMOS Image Sensor (CIS) partitioned in different tiers. The CIS serves as an ideal case study of the coupling effects as it consists

of highly sensitive parts to noise while it presents also an extremely appealing use of 3DSI to the semiconductor industry. The most critical figures of merit are therefore analyzed at a pixel level to ensure the normal operation of the circuit. Lastly, a comprehensive modeling of inter-tier coupling effects is presented. The models predict accurately the impact of layout effects on the inter-tier capacitive coupling between active devices, and can be integrated in SPICE tools to analyze complex and large-scale monolithic 3-D circuits, merging the gap between pre- and post-layout simulations.

RESUME

Impact de bruit et couplages électro magnétiques dans les technologies 3D séquentielles : Etudes, modélisation et parade

Au lieu de réduire la taille des transistors pour respecter la loi de Moore, les technologies d'intégration tridimensionnelle (3-D) offrent une densité d'intégration plus élevée, une consommation d'énergie plus faible et fournissent une plateforme unique pour l'intégration hétérogène de différents matériaux de couches actives par l'empilement vertical des couches de circuits intégrés. L'intégration séquentielle 3-D (également appelée intégration monolithique 3-D ou VLSI 3-D) est un type de schéma d'intégration 3-D, dans lequel les multiples couches empilées sont fabriquées séquentiellement l'un sur l'autre sur la même plaquette. Chaque niveau est constitué de couches actives et de couches BEOL isolées par des couches diélectriques intercouches (ILD). La propriété fondamentale qui différencie cette technologie est la réduction importante de la distance entre les 2 (ou plus) couches, qui conduit à des très petites capacités parasites permettant aux signaux numériques d'avoir une haute fréquence tout en étant générés avec une faible énergie. En conséquence, l'intégration séquentielle 3-D apporte des nouvelles possibilités pour les architectures mixtes avec des performances en termes de vitesse et de faible consommation d'énergie qui ne peuvent pas être facilement satisfaites avec d'autres schémas de technologies 3-D (TSV, copper to copper bonding, etc.). Cependant, les signaux à haute fréquence, la localisation spatiale, la forte densité d'interconnexions peuvent tous être une source majeure d'interférence entre les niveaux empilés, modulant le comportement attendu des dispositifs ainsi qu'ajoutant du bruit. Il faut donc trouver des solutions et des techniques pour limiter ces effets. Ce travail vise à répondre à ce défi et assurer la robustesse de la technologie. L'impact de l'interférence électromagnétique et du bruit entre les niveaux empilés dans la technologie d'intégration séquentielle 3-D est étudié de manière approfondie dans ce travail, tant au niveau des dispositifs que des circuits. Pour ce faire, les designs digital, analogiques et signaux mixtes/RF les plus critiques ont été sélectionnés pour construire des circuits 3-D monolithiques. Des mesures électriques, en conjonction avec des simulations TCAD, révèlent les mécanismes de couplage responsables pour la propagation électromagnétique et du bruit entre les niveaux empilés. De plus, la force des signaux propagés est évaluée et son impact sur

les performances du dispositif / circuit est étudié en profondeur. Cette étude présente également l'impact des effets de couplage sur la performance d'un capteur d'image CMOS (CIS) en intégration séquentielle 3-D partitionné en différents niveaux, est examiné. Le CIS constitue un cas d'étude idéal des effets de couplage car il est constitué de parties très sensibles au bruit, tout en présentant une utilisation extrêmement attrayante de l'intégration séquentielle 3D pour l'industrie de semi-conducteurs. Les chiffres de mérite les plus critiques sont donc analysés au niveau du pixel pour assurer le fonctionnement normal du circuit. Enfin, une approche de modélisation des effets de couplage entre les niveaux est présentée. Les modèles prédisent avec précision l'impact des effets de disposition sur le couplage capacitif inter-niveaux entre les dispositifs actifs, et peut être intégré dans les outils SPICE pour analyser des circuits 3-D monolithiques complexes et à grande échelle, en fusionnant le fossé entre les simulations de pré et post-disposition.