Investigation and Modeling of High Frequency Effects in SiGe HBTs

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Par Bishwadeep SAHA

Investigation and Modeling of High Frequency Effects in SiGe HBTs

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ABSTRACT

Investigation et Modélisation de la Haute Fréquence Effets dans les HBT SiGe

Résumé: Ce travail de thèse présente une étude concernant la caractérisation des effets haute fréquence dans les transistors bipolaires à hétérojonction (HBT) en SiGe. Lors de ces travaux, le transistor du procédé BiCMOS B55 (55nm) de STMicroelectronics a été principalement analysé. Cette technologie à l'état de l'art est caractérisée par une fréquence de transition de 320 GHz et une fréquence maximale d'oscillation (f_{MAX}) de 370 GHz. Les travaux se divisent en trois sous-thèmes dont les objectifs sont une meilleure caractérisation et une meilleure modélisation de ces composants. Une première partie concerne l'extraction de la f_{MAX} des transistors miniaturisés. En effet, cette fréquence f_{MAX} est une figure de mérite de première importance qui est utilisée pour valoriser une technologie. Malheureusement, on observe que la méthodologie utilisée pour extraire f_{MAX} en utilisant directement la formule de gain de Mason sur les données mesurées donne des résultats très incertains sur les composants très avancés. Ceci complexifie l'analyse des lots de fabrication de transistors. Il a été démontré qu'un modèle petit signal simple extrait à partir des paramètres Y supprime les incertitudes d'extraction et permet l'évaluation fine d'une technologie. La seconde partie concerne le substrat du transistor. En effet, cette zone du transistor est la plus importante en terme de géométrie entrainant des effets distribués dont la contribution est plus importante à haute fréquence. Celui-ci joue donc un rôle essentiel dans la modélisation des caractéristiques des paramètres S à haute fréquence des HBT SiGe modernes. Dans ce travaux, nous avons donc étendu et validé le modèle du substrat du transistor et nous avons confronté les simulations de type SPICE et les mesures jusqu'à des fréquences supérieures à 300 GHz. Finalement, dans une troisième partie, nous avons cette fois orienté nos travaux de modélisation vers les accès de base, collecteur et émetteur ainsi que sur le transistor intrinsèque. En effet, à très haute fréquence, c'est-à-dire au-delà de 100 GHz pour cette technologie, les accès du transistor doivent être modélisés par des éléments distribués. Le transistor intrinsèque est quant à lui sujet à des effets dits non-quasi-statiques. Des études de sensibilité des paramètres haute fréquences du modèle HICUM ont été menées permettant d'établir une stratégie d'extraction de paramètres. Les paramètres haute fréquence sont extraits à l'aide de la simulation TCAD et comparés aux mesures des paramètres S jusqu'à 500 GHz.

Mots-clés : SiGe HBT, f_{MAX}, Impédance de sortie, Effets haute fréquence, TCAD, HICUM

Investigation and Modeling of High Frequency Effects in SiGe HBTs

Abstract: This thesis presents a study concerning the characterization of high frequency effects in bipolar heterojunction transistors (HBT) in SiGe. During this work, the transistor of the BiCMOS B55 process (55nm) from STMicroelectronics was mainly analyzed. This state-of-the-art technology is characterized by a transition frequency of 320 GHz and a maximum oscillation frequency (f_{MAX}) of 370 GHz. The work is divided into three sub-themes, the objectives of which are better characterization and better modeling of these components. The first part concerns the extraction of f_{MAX} from miniaturized transistors. Indeed, this f_{MAX} frequency is a figure of merit of the first importance which is used to promote a technology. Unfortunately, it is observed that the methodology used to extract f_{MAX} by directly using Mason's gain formula on the measured data gives very uncertain results on very advanced components. This complicates the analysis of transistor manufacturing batches. It has been shown that a simple small signal model extracted from the Y parameters removes the extraction uncertainties and allows the fine evaluation of a technology. The second part concerns the substrate of the transistor. In fact, this zone of the transistor is the most important in terms of geometry, leading to distributed effects, the contribution of which is greater at high frequency. This therefore plays an essential role in the modeling of the characteristics of the high frequency S parameters of modern HBT SiGe. In this work, we therefore extended and validated the transistor substrate model and we compared the SPICE-type simulations and measurements up to frequencies above 300 GHz. Finally, in a third part, we have oriented our modeling work towards the base, collector and emitter accesses as well as on the intrinsic transistor. Indeed, at very high frequency, that is to say above 100 GHz for this technology, the transistor accesses must be modeled by distributed elements. The intrinsic transistor is itself subject to so-called non-quasi-static effects. Sensitivity studies of the high frequency parameters of the HICUM model were carried out to establish a parameter extraction strategy. The high-frequency parameters are extracted with the support of the TCAD simulation and compared with S parameters measurements up to 500 GHz.

Keywords: SiGe HBT, f_{MAX}, Output impedance, High frequency effects, TCAD, HICUM.

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QUOTATIONS

"Live as if,

you were to die tomorrow.

Learn as if,

you were to live forever."

MAHATMA GANDHI

DEDICATION

To My Parents and sister...

List of Publications

The publications arising out of the work mentioned in this thesis are given as follows:

I. REFEREED JOURNALS BASED ON THE THESIS

1. Bishwadeep Saha, Sébastien Frégonese, Bernd Heinemann, Patrick Scheer, Pascal Chevalier, Klaus Aufinger, Anjan Chakravorty, Thomas Zimmer. Reliable Technology Evaluation of SiGe HBTs and MOSFETs: f_{MAX} Estimation From Measured Data. *IEEE Electron Device Letters*, 42, 14-17, (2021).
2. Bishwadeep Saha, Sébastien Frégonese, Anjan Chakravorty, Soumya Ranjan Panda, Thomas Zimmer. Sub-THz and THz SiGe HBT Electrical Compact Modeling *Electronics*, 10, 1397, (2021).

II. PRESENTATIONS IN CONFERENCES

1. Bishwadeep Saha, Sébastien Frégonese, Soumya Ranjan Panda, Anjan Chakravorty, Thomas Zimmer. Collector substrate modeling of SiGe HBTs up to THz range. *2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS)*, 1-4, (2019).

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ABBREVIATIONS

AC	Alternating Current
ADC	Analog to Digital Converter
BC	Base-Collector
BE	Base-Emitter
BEM	Boundary Element Method
BEOL	Back-End-Of-Line
BiCMOS	BIpolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
CB	Common Base
CC	Common Collector
CE	Common Emitter
CMC	Compact Model Coalition
DAC	Digital to Analog Converter
DC	Direct Current
DEMUX	Demultiplexer
DTI	Deep Trench Isolation
DUT	Device Under Test
EDA	Electronic Design Automation
EM	Electro Magnetic
EU	European Union
FDSOI	Fully Depleted Silicon On Insulator
FEM	Finite Element Method
FET	Field Effect Transistor
FoM	Figure of Merit
GICCR	Generalized Integral Charge Control Relation
HBT	Heterojunction Bipolar Transistor
HF	High Frequency
HICUM	HIgh CUrrent Model

HICUM L2	HIgh CUrrent Model Level2
IRDS	International Roadmap for Device and System
ISS	Impedance Standard Substrate
LAN	Local Area Network
LNQS	Lateral Non-Quasi-Static
MAG	Maximum Available Gain
MUX	Multiplexer
MSG	Maximum Stable Gain
NF	Noise Figure
NQS	Non-Quasi-Static
PAN	Personal Area Network
PDK	Process Design Kit
QS	Quasi-Static
RF	Radio Frequency
SGPM	SPICE Gummel Poon Model
SiGe	Silicon-Germanium
SNR	Signal-to-Noise-Ratio
SoC	System on Chip
SOLT	Short-Open-Load-Through
SPICE	Simulation program with Integrated Circuit Emphasis
ST	STMicroelectronics
STI	Shallow Trench Isolation
TCAD	Technology Computer Aided Design
TEM	Transmission Electron Microscope
TRL	Thru-Reflect-Line
VNQS	Vertical Non-Quasi-Static
WLAN	Wireless Local Area Network

NOTATION

Physical constant

k	Boltzmann's constant (= 1.38×10^{-23} JK^{-1})
q	Electronic charge (= 1.602×10^{-19} C)
ϵ_0	Permittivity of the free space (= 8.85×10^{-12} C^2/Nm)

English Symbols

B', C', E'	Internal base, collector, and emitter nodes respectively in HICUM
B^*	External base node in HICUM
BV_{CEO}	Open base collector emitter breakdown voltage
ΔE_C	Conduction band offset
ΔE_G	Bandgap difference
ΔE_V	Valence band offset
C_{BC}	Base collector capacitance
C_{BCx}	External base collector capacitance
C_{JCx}	External base collector junction capacitance
C_{BE}	Base emitter capacitance
C_{μ}	Base collector capacitance of the small-signal hybrid-π model
C_{j0}	Zero bias collector substrate diode junction capacitance
C_{js}	Collector substrate diode junction capacitance
C_{per}	Collector substrate peripheral capacitance
C_{RBi}	Internal base shunt capacitance in HICUM
$C_{BE,par}$	Base emitter parasitic capacitance in HICUM
$C_{BE,par,eff}$	Effective base emitter parasitic capacitance
$C_{BC,par}$	Base collector parasitic capacitance in HICUM
d_C	Buried layer and depth of collector substrate space charge region
f	Operating frequency
f_C	Cut-off frequency
f_T	Unity current gain transit frequency
f_{MAX}	Unity power gain transit frequency or maximum oscillation frequency
g_m	Transconductance
g_{m0}	DC Transconductance
i_{AVL}	Base collector avalanche current
I_C	Collector Current
i_{BEti}	Internal base emitter tunneling current
i_{jBEi}, i_{jBCi}	Internal base emitter and base collector junction currents respectively
i_T	Transfer current
J_C	Collector Current density
K	Stability factor
Q_f	Forward minority charge
Q_r	Inverse minority charge

Q_{jEi}, Q_{jCi}	Internal base emitter and base collector junction charge respectively
Q_{rBI}	Charge across internal base resistance
Q_{JEp}	Peripheral base emitter charge
$Q_{BE,par}$	Parasitic base emitter charge
r_b	Base resistance
R^*_{bi}	Internal base resistance in HICUM
R_{Bx}	External base resistance in HICUM
R_{BiT}	External and internal base resistance in small-signal hybrid-π model
R_{per}	Collector substrate peripheral resistance
r_c	Collector resistance
r_π, C_π	Internal base emitter resistance and capacitance of the small-signal hybrid-π model
r_0	Collector emitter resistance of the small-signal hybrid-π model
R_{su}, C_{su}	Substrate resistance and capacitance respectively in HICUM
V_A	Early voltage
V_{BC}	Base-collector voltage
V_{BE}	Base-emitter voltage
T	Thermal voltage
U	Unilateral gain
v_{sat}	Saturation velocity
W_{BC}	Base collector depletion region width

Greek Symbols

β	Current gain in the common emitter configuration
τ_b	Base transit time
τ_d	Overall delay time
τ_e	Emitter transit time
ρ	Resistivity
ϵ	Permittivity
ω	Angular frequency

Miscellaneous

$\tilde{\gamma}$	Position-averaged quantities across the base profile
$\tilde{\eta}$	Minority electron diffusivity ratio
β_i	Function of small-signal parameters
c_i	Function of β_i
α_i	Normalization function of c_i

CHAPTER 1

PRINCIPLES OF BIPOLAR TRANSISTOR AND EVALUATION OF BICMOS TECHNOLOGY

Promising progress has been made in the field of semiconductor technology today, due to the revolutionary invention of the transistor. In its early days, Germanium was used to manufacture transistors. However, Germanium was quickly replaced by Silicon due to reliability issues and operation at high temperatures. Texas Instruments invented the first Silicon-based transistor in 1954, and its mature of technology, low cost, and mass integration capabilities made Silicon the basis for manufacturing transistors for industrial and commercial purposes. Today, the number of transistors in a chip from leading smartphone manufacturers such as Apple, Huawei, etc. exceeds 10 billion.

Mostly the semiconductor market is dominated by one type of transistors, the field-effect transistor (FET). However, for specific applications related to very high frequencies, the bipolar transistor (BJT) is still the corner stone and it is primarily responsible for the rapid development in the last decade of ultra-high data transfer systems. Moreover, it was long time employed for the output stage of mobile phones and is considered as the key element for next 6G generation and finally it will be the heart of the long distance radar systems for autonomous car drive.

The progress in frequency is mainly due to the continuous changes and applications of the various semiconductor devices. These changes can be broadly divided into two categories: (i) structural changes and (ii) technological changes. In structural modification, heterojunctions were introduced after considering a suitable material from the periodic table (mainly group III, IV or V). Following this idea, IBM first demonstrated the result of a SiGe HBT at the IEDM conference in 1987 Iyer *et al.* (1987). Technological modifications, on the other hand, merge different technologies into a single platform. Complementary metal-oxide semiconductors (CMOS) are known for their low power dissipation due to the complementary switching process. Coupling CMOS with the bipolar technology results in the BiCMOS technology which combines the advantages of both technologies: High integration density, low power and high speed.

In the last decade, various EU countries have contributed to improve the performance of SiGe-HBT technology. For example, IHP reported a maximum oscillation frequency (f_{MAX}) of up to 500 GHz Heinemann *et al.* (2010) in the DOTFIVE project and 720 GHz Heinemann *et al.* (2016) in the DOTSEVEN project, which is considered the highest f_{MAX} value for SiGe-HBTs. It has been predicted that the performance of the transistor may be even more aggressive in the coming years due to the continuous downsizing of the device dimensions. The IRDS (International Roadmap for Device And Systems) community has predicted the future performance metrics of SiGe-HBTs (Figs. 1.1). Based on the progress in the SiGe technology, it is expected that the SiGe HBTs will be able to overcome the THz-limit.

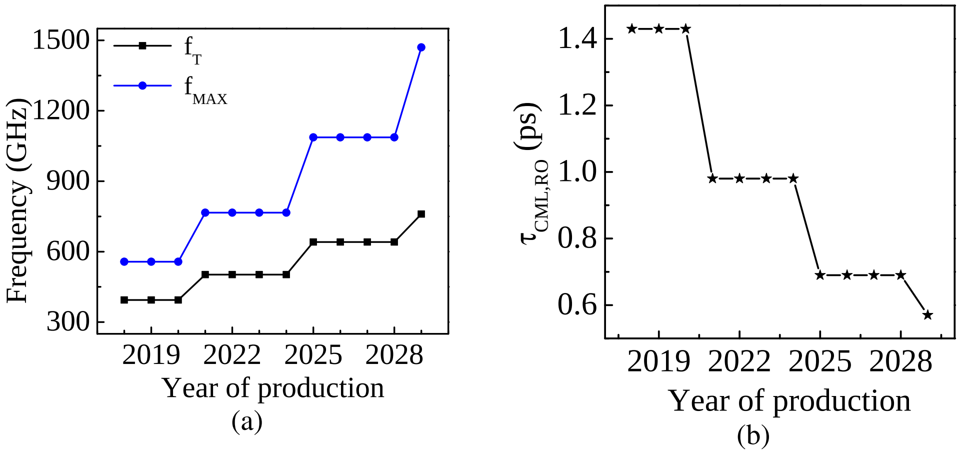


Fig. 1.1: High-speed SiGe HBT f_T and f_{MAX} roadmap (a), and ring oscillator gate delay (b) versus year of production (source: ird (2020)).

1.1 Basic of bipolar transistor device physics

1.1.1 Bipolar junction transistor

The term 'bipolar' in the bipolar junction transistor reflects the fact that both types of carriers, namely electrons and holes, are involved in the operation. Although minority carrier diffusion plays a critical role. The sections in a BJT are the emitter, base, and collector with the alternate doping concentration i.e. the complete device structure is either n-p-n or p-n-p. As electrons have greater mobility than holes, n-p-n transistors are often used to offer greater trans-conductance and speed. As per the application point of view, a transistor can be operated in four possible regions of operations (Table. 1.1) with any one of possible circuit configurations (Table. 1.2). Commercially a transistor is mainly used as an amplifier so we discuss here the forward active mode of operation.

Table 1.1: Possible regions of operation and application of bipolar transistor.

Possible region of operation	Applied bias (n-p-n)	Application
Forward active	$V_{BE} > 0$V, $V_{BC} < 0$V	analog amplifier
Inverse active	$V_{BE} < 0$V, $V_{BC} > 0$V	resonator
Saturation	$V_{BE} > 0$V, $V_{BC} > 0$V	digital circuits
Cut-off	$V_{BE} < 0$V, $V_{BC} < 0$V	digital circuits

Table 1.2: Possible circuit configuration for bipolar transistor.

Possible circuit configuration	Input terminal	Output terminal	Common terminal
common emitter (CE)	Base	Collector	Emitter
common base (CB)	Emitter	Collector	Base
common collector (CC)	Base	Emitter	Collector

As shown in Table. 1.1, in forward active mode, the base-emitter junction is forward biased while the base-collector junction is reverse biased. A large number of electrons (for n-p-n transistor) are thus injected from the emitter into the base. Then diffusion of electrons from the base to the collector occurs as a result of the formation of a concentration gradient in the base. Of course, the width of the neutral base region should be considered equal to or smaller than the diffusion length of the electrons otherwise, a significant recombination current will generate and no electrons will reach the edge of the base-collector space charge region. In the other case, upon reaching the base-collector space charge region and due to the presence of a large electric field, electrons are quickly swept across the space charge region and become available in the collector region. On the other hand, the majority of holes from the base inject into the emitter generating base current. To minimize the base current (for sustaining the total current gain), emitter doping can be increased compared to base doping. The current flow components for a n-p-n transistor under a forward active mode of operation are shown in Fig. 1.2.

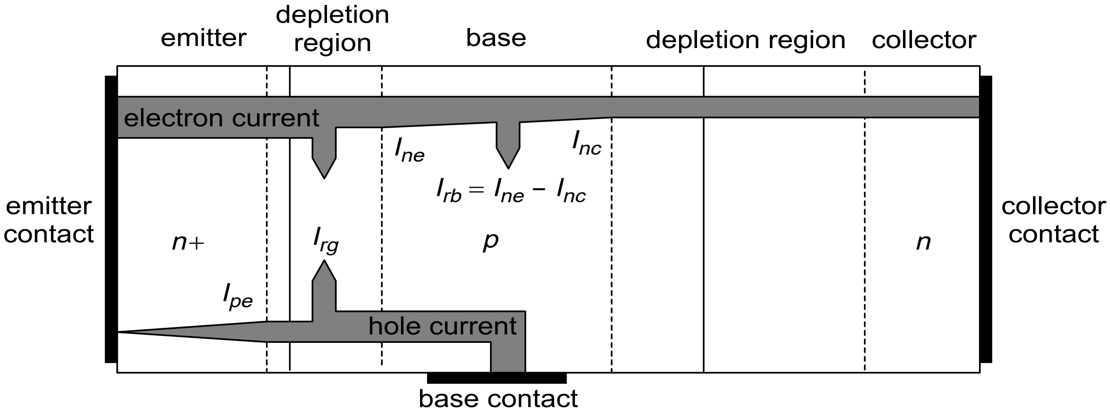
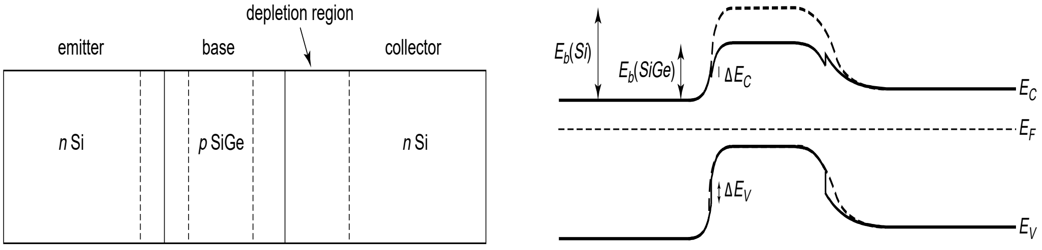


Fig. 1.2: Current components inside the n-p-n bipolar transistor operating in the forward active mode (source: Ashburn (2003)).

1.1.2 The SiGe HBT transistor

Following the general design procedure, a silicon BJT hardly manages to operate at cut-off frequencies higher than 50 GHz. This is mainly because of the considerable base transit time of minority carriers. Therefore, in order to reduce the base transit time, a narrow heavily doped base should be considered. Note that a heavily doped base results in low base resistance. However, at the same time, the base current increases, thus reducing the total current gain. The trade-off in between gain and base transit time is so-called *bandgap engineering*. This methodology was introduced in BJTs to improve their performance.

Heterojunction bipolar transistor (HBT) is a kind of bipolar transistor in which one of the two junctions (or both) can be formed with a different kind of semiconductor material. In general, a narrow bandgap and a wide bandgap material are used in the base and emitter, respectively to form such heterojunction. This results in a lower energy barrier for the carriers moving from emitter to base and higher for the carriers moving towards the emitter. Since SiGe has a lower bandgap than silicon, a thin epitaxial layer of SiGe is grown on the base of silicon BJT (Fig. 1.3a). The energy band diagram, in Fig. 1.3b, shows that the conduction band barrier is much smaller in SiGe HBT than in



(a) (b)

Fig. 1.3: Basic cross-sectional view of a SiGe HBT structure (a), and comparison of energy band diagram in between silicon BJT (dashed line) and a SiGe HBT (solid line) (b) (source: Ashburn (2003)).

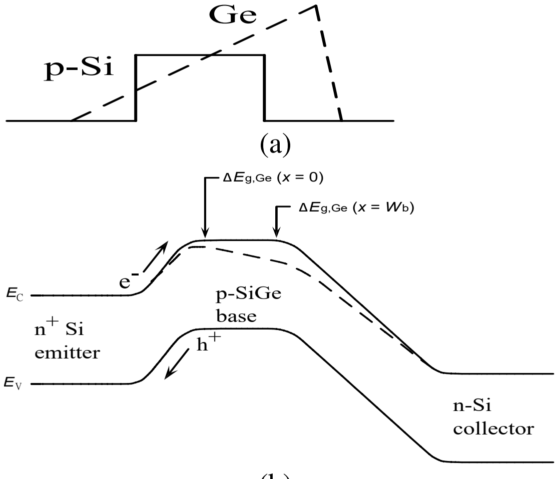
Si BJT. This low barrier height in SiGe HBT results in a much higher collector current to silicon BJT at the same operating point. In addition to having desired gain, the base resistance of HBT can be reduced to decrease input power consumption. High current gain with low base resistance helps to achieve high input signal-to-noise (SNR) ratio leading to a low noise figure (NF$_{min}$).

In modern *bandgap engineering*, instead of using box type germanium (Ge) profile in the base, a graded profile is used. This means that the Ge content is linearly graded from 0% near the base-emitter junction to some maximum value of Ge content near the collector-base junction than rapidly ramped down to 0% Ge. Unlike the constant baseband lowering, as shown in Fig. 1.3b, graded Ge profile lowers most of the base bandgap at the collector side. Moreover, the built-in electric field further reduces the base transit time. A triangular Ge-profile and resulting non-uniform change in the base bandgap are shown in Figs. 1.4a and 1.4b respectively.

Due to the incorporation of graded Ge profile in the base, it leads to positive influences in both DC and AC operation. They are summarized as follows:

(a) Since both the base-emitter and base-collector junctions bandgaps become narrower, for the same applied V_{BE}, more electrons inject into the base resulting in higher collector current and gain, provided base current remain unchanged. In fact, the presence of Ge gives a new order of freedom to adjust the current gain, which is only dependent on the base doping in the conventional BJT. This is the added flexibility to customize the base resistance with the same current gain.

(b) Since the Ge content at the base-collector junction is finite (generally high com-



(a)

(b)

Fig. 1.4: Triangular Ge profile for a graded base SiGe HBT (a), and energy band diagram showing silicon BJT (solid line) and a SiGe HBT (dashed line) (b) both biased at forward active mode with low injection operation (source: Cressler (2008)).

pared to the base-emitter junction in Fig. 1.4a), it restrains the base-collector space charge region to move further into the quasi-neutral base region with increasing V_{BC}. This results in higher early voltage and output conductance compared to silicon BJT.

(c) The dynamic operation in silicon BJT is limited due to the substantial basic transit time. However, an HBT with a graded Ge profile can efficiently handle this issue by featuring a higher built-in field such that this field accelerates all the injected minority carriers across the base. Hence base transit time is decreased significantly.

Considering such graded Ge incorporated bandgap engineering, the normalized DC figure-of-merits (gain β, early voltage V_A, transit time τ_b) are summarized as follows Cressler (2008):

$$\frac{\beta_{SiGe}}{\beta_{Si}} = \{\frac{\tilde{\gamma}\tilde{\eta}\Delta E_{g,Ge}(grade)/kT e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}\} \tag{1.1}$$

$$\frac{V_{A,SiGe}}{V_{A,Si}} = e^{\Delta E_{g,Ge}(grade)/kT}\{\frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\} \tag{1.2}$$

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}}\frac{kT}{\Delta E_{g,Ge}(grade)}\{1 - \frac{kT}{\Delta E_{g,Ge}(grade)}[1 - e^{-\Delta E_{g,Ge}(grade)/kT}]\} \tag{1.3}$$

The AC figure-of-merits are also positively influenced. The unity gain cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}) can be written Cressler (2008):

$$f_T = \frac{1}{2\pi}[\frac{kT}{qI_C}(C_{BE} + C_{BC}) + \tau_b + \tau_e + \frac{W_{BC}}{2v_{sat}} + r_c C_{BC}]^{-1} \tag{1.4}$$

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi C_{BC} r_b}} \tag{1.5}$$

The transit time improvement results in an increase of f_T and thus an improvement of f_{MAX} also.

1.2 Micrometer to THz waves and application

Silicon offers integration capabilities on a very large-scale and the miniaturization of the device geometries makes it possible to obtain high cut-off frequencies. These two benefits along with Ge's integration make SiGe HBT capable of capturing the RF wireless communication market and become one of the contenders relatively in a short period of time. For those key reasons, SiGe HBT can cover a wide variety of applications. Below we have classified the different applications into the respective frequency spectrum.

Fig. 1.5 shows the electromagnetic spectrum primarily with a focus from microwaves to THz waves. Although there is no stated convention about the range of the frequency spectrum, we do categorize the various applications in the respective bands. Generally, the spectrum from 300 MHz to 30 GHz term as microwave spectrum which mainly serves the purpose of ground wave long-distance communication. The next range is from 30 GHz to 300 GHz and is termed as a millimeter (mm) wave spectrum where high-speed and radar applications have taken place. Following mm-wave, the spectrum from 300 GHz to 3 THz is known as sub-millimeter (sub-mm) range (or THz range) which is primarily used for imaging and sensing applications.

Since microwaves are hardly affected by environmental hazards hence this spectrum finds applications in the television and radio broadcasting related long-distance communication. However, because of the higher wavelength (by comparing its high-frequency neighbors), signals from this spectrum have a low rate of data transmission.

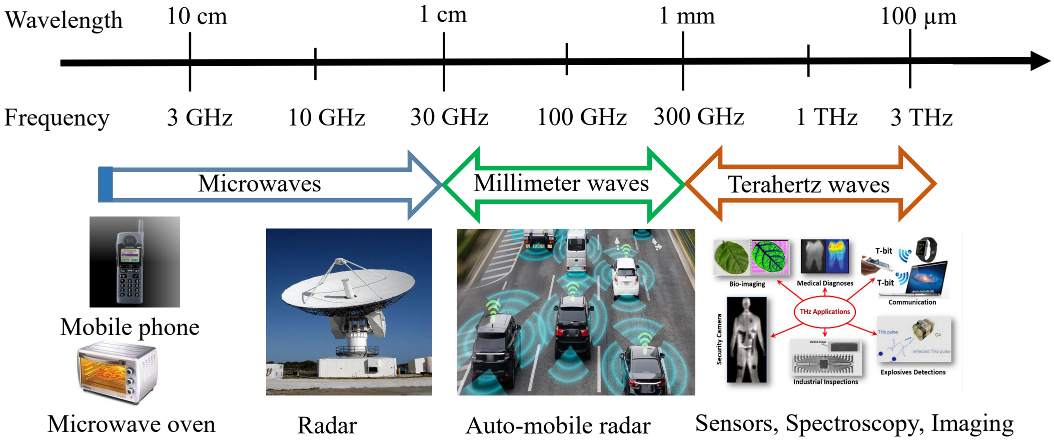


Fig. 1.5: Micro, millimeter, and sub-millimeter wave range.

For wireless, digital and space communications, the mm-wave of the electromagnetic spectrum is used. Wireless applications include inter-satellite, inter-building (use E-band 71-76 and 81-86 GHz signals), and personal and local area network (PAN/LANs) related communications. On the other hand, data switch (MUX/DEMUX) and analog-to-digital conversion (ADC/DAC) are included in the digital communication category. Space communication mainly uses the 94 GHz spectrum of the band and use in airport aviation for safety and ground control. Except for these applications, the mm-wave spectrum also includes some applications in automotive radar and the industrial environment. The signal of this spectrum having 77 GHz is used for long-range radar and 77 to 81 GHz bands are used for short-range radar application. These short-range and long-range radars are used in road and satellite vehicles respectively, to avoid collision and predict the road conditions. Signals belong to this spectrum have a high data transmission rate but as shown in Fig. 1.6, this spectrum faces moderate signal attenuation in the Earth's atmosphere.

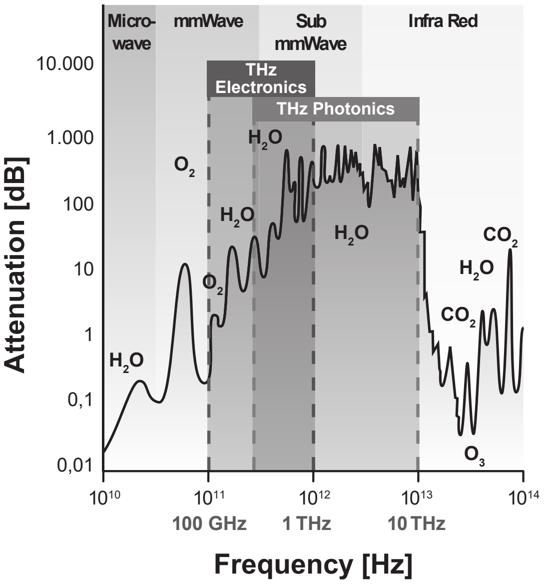


Fig. 1.6: Impact of atmosphere on the electromagnetic spectrum (source: Pfeiffer and Öjefors (2010)).

The spectrum in between the mm-wave and the infrared is called sub-mm or THz spectrum (300 GHz to 3 THz) Siegel (2002). With very fast data communication, Kukutsu *et al.* (2010), Huang and Wang (2011), this spectrum can hold other applications. Since THz wave can penetrate through material, (ceramic, plastic, clothes, etc.) it finds application in security screening Kawase *et al.* (2003), Woolard *et al.* (2007) and non-destructive detection Mittleman *et al.* (1997), Zhong *et al.* (2005). THz waves are not ionizing hence it can be allowed to pass through the skin tissues with low water content and finds various applications in medical, biological and drugs industries Nagel *et al.* (2002), Woodward *et al.* (2002), Fischer *et al.* (2005).

Without any ambiguity, it can be said that the THz wave opens new fields in research either for industrial, commercial, or day-to-day life. Although in communication prospective THz communication is limited since existing sources and detectors can not work more than twenty meters. Moreover, due to higher attenuation (Fig. 1.6), long-distance communication can not be performed using this spectrum Piesiewicz *et al.* (2007). The shortcomings like THz signal generation, processing, and detection are often called "THz-gap".

1.3 SiGe BiCMOS technology, HBT device modeling and limitation

1.3.1 Technology Evaluation

SiGe HBT technology meets the requirements necessary for mm-wave applications. This progress is achieved through tireless efforts by the various research groups. The results obtained by the various research laboratories are shown in Fig. 1.7.

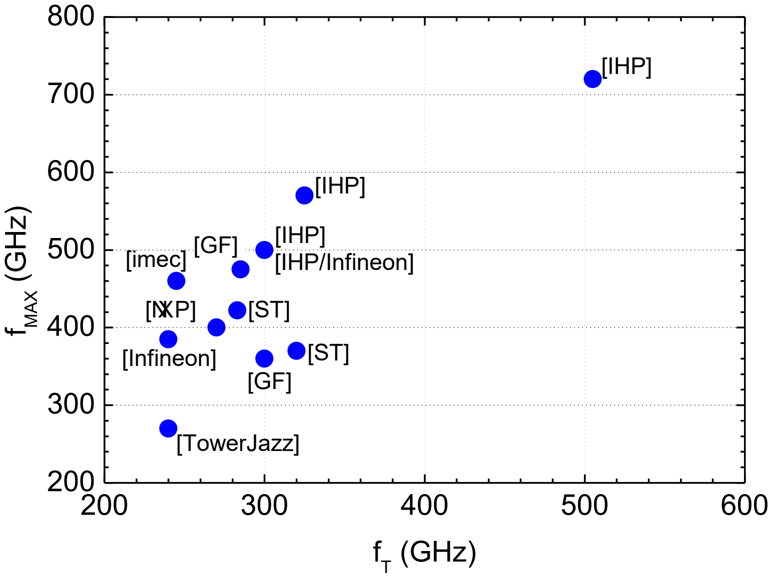


Fig. 1.7: Peak f_{MAX} and f_T of the SiGe HBT from various companies (source: Chevalier *et al.* (2018)).

In BiCMOS technology, Bipolar technology and CMOS technology are merged into one to achieve the benefits of both Alvarez (1993), bic (1996). Bipolar usually provides a higher speed and lower noise margin and on the other hand, CMOS provides lower power dissipation and higher packing density. Therefore, in BiCMOS technology, it is possible to have a higher speed than the CMOS and a lower power dissipation than the Bipolar. The reasons why BiCMOS technology plays a key role in the radio spectrum, competing with CMOS technology, are discussed below Chevalier *et al.* (2018):

(1) To minimize the parasitic contribution, the back-end-of-line (BEOL) configuration can be optimized in the BiCMOS technology, unlike in the CMOS technology.

(2) Due to having higher breakdown voltage, larger transconductance, and lower $\frac{1}{f}$ noise, BiCMOS technology featuring superior reliability compared to CMOS technology in which reliability is limited by hot carrier injection, resulting reduction in threshold voltage and trans-conductance.

(3) To benefit from the development and cost of wafers, BiCMOS technologies are used to build on noncompetitive CMOS technologies (at least 2 generations of delay).

(4) In CMOS technology, the metallization layers are usually stacked with an MOS transistor which leads to degrade the overall high-frequency performance. Moreover, parasitic gate capacitance in FinFET like MOS devices can further deteriorate the radio frequency performance. On the other hand, the impact of de-embedding on the bipolar transistor performance is negligible Voinigescu *et al.* (2012).

Table 1.3 shows the key FoMs of the transistors fabricated in STMicroelectronics (ST) by following various BiCMOS technologies. The first STMicroelectronics technology that could deal with wireless communication was BiCMOS6G Monroy *et al.* (1999). With high-quality passive components, this technology offers double-poly SiGe HBT (FoMs are shown in Table. 1.3). Later in 2001, robust double polysilicon with quasi self-aligned SiGe technology (BiCMOS7 Baudry *et al.* (2001)) was reported which primarily addressed the optical communication at 40 Gbit/s. Without changing the CMOS node and to improve the noise figure, ST reported BiCMOS7RF Baudry *et al.* (2003) SiGe technology. In terms of FoM, since the improvements achieved only in BV$_{CEO}$ and f_{MAX} (about 10%), in the same year, a different CMOS node was used to develop a new SiGe technology (BiCMOS9 Laurens *et al.* (2003)). A remarkable frequency performance has been achieved (Table 1.3), although this technology still offers optical and radiofrequency communication at 40 Gbit/s. Later to address the applications like 60 GHz WLAN, 77 GHz automotive radar, and 80 Gbit/s optical communication, a fully self-aligned architecture with selective epitaxial growth of base was reported. This new technology, BiCMOS9MW Chevalier *et al.* (2007), is fully dedicated for millimeter-wave application with f_T/230 GHz and f_{MAX}/280 GHz.

Although this conquistador suffers from the parasitic effects, mainly coming at the millimeter-wave regime, originating from BEOL configuration. Hence, following a

Table 1.3: Evaluation of SiGe BiCMOS technology in STMicroelectronics.

BiCMOS Technology (CMOS node)	f_T (GHz)	f_{MAX} (GHz)	J_C at peak f_T & f_{MAX} (mA/μm^2)	BV_{CEO} (V)
6G Monroy *et al.* (1999) (350 nm)	45	60	1	3.6
7 Baudry *et al.* (2001) (250 nm)	70	90	3	2.6
7RF Baudry *et al.* (2003) (250 nm)	65	99	2	3
9 Laurens *et al.* (2003) (130 nm)	166	175	8.5	1.8
9MW Chevalier *et al.* (2007) (120 nm)	230	280	10.5	1.6
B55 Chevalier *et al.* (2014) (55 nm)	326	376	19	1.5

modified BEOL design (Fig. 1.8), BiCMOS055 Chevalier *et al.* (2014) technology was reported which features improve radio-frequency (RF) performances due to reduced parasitic contribution. Moreover, care has been taken in the lithography and etching process which not only reduced the net area (of the transistor) by 40% Chevalier *et al.* (2015) but also increased the packing density by 5 times compared to BiCMOS9MW technology. Additionally, due to featuring high gain, low-noise, and low-power consumption, this technology (BiCMOS055) is useful for optical, wireless, and high-performance analog applications. Fig. 1.9a shows the cross-section view of the main devices and Fig. 1.9b shows the cross-section view of the device structure.

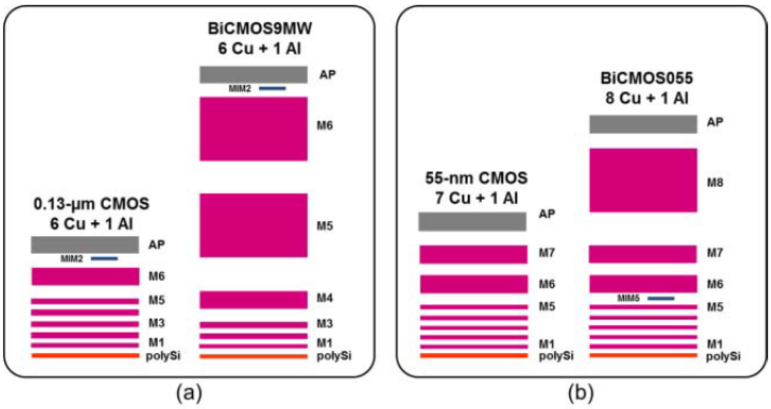
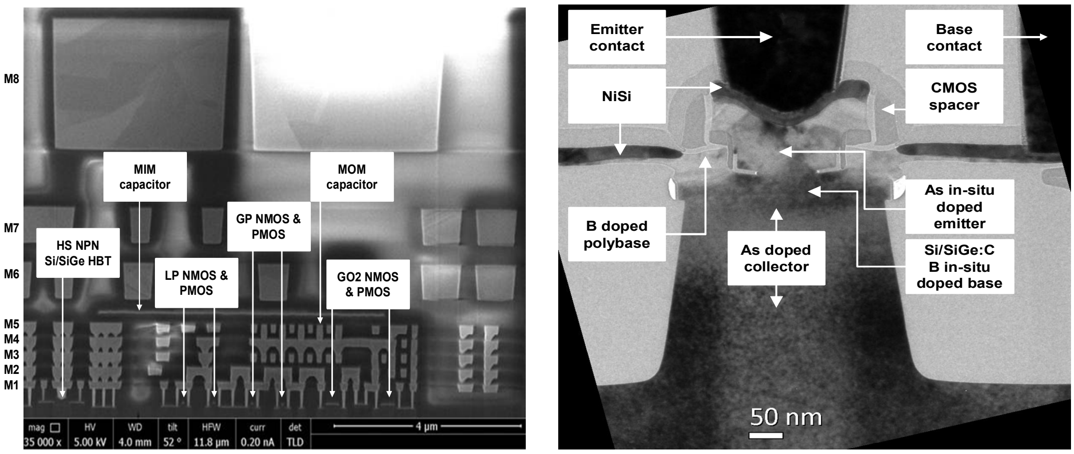


Fig. 1.8: BEOL modification in between digital CMOS and derived BiCMOS: 130 nm BiCMOS9MW (a), and 55 nm BiCMOS055 (b) (source: Chevalier *et al.* (2018)).



(a) (b)

Fig. 1.9: SEM cross-section of the main devices with BEOL up to Metal 8 (a), and TEM cross-section (zoom in emitter-base part) of a 0.1 μm $\times$ 4.9 μm high-speed SiGe HBT fabricated in BiCMOS055 process technology (source: Chevalier *et al.* (2014)).

1.3.2 HBT device modeling and limitation

The overall device modeling can be categorized into the following four basic types: Schröter and Chakravorty (2010)

(i) table & fitting models

(ii) physics-based compact models

(iii) semi-numerical models

(iv) device simulation.

Primarily, these models are the function in between complexity and physical basic; it means that both increase as one moves from table & fitting based model to device simulation-based model. Although in this thesis HICUM (under the physics-based compact model's category) based simulation is used and compared with other simulation or measured data. Except HICUM, SPICE (Simulation Program with Integrated Circuit Emphasis) based results are also used in various research industries and laboratories mainly for rapid evaluation of large-scale integrated circuits. The importance of the SPICE and HICUM based modeling approaches have been discussed in the following sub-sections.

BiCMOS technology allows building mixed-signal (analog and digital) system-on-chip (SoC) which has a potential market in millimeter-wave to TeraHertz consumer application. A few years ago, a European research project (RF2THz SiSoC) was carried out in which the primary goal was to fabricate silicon-based SoC in a 300 mm wafer (large diameter in a production unit) to address the wide-range consumer applications. But for such SoC design, one of the most critical issues is the simulation of the integrated circuits all at a time. Following a detailed compact model or TCAD based simulations attempts end up with functional failure. Hence to overcome this issue, a quick and reliable SPICE-based simulation approach is often considered. Some key advantages of the SPICE modeling approach are

(a) physical and complex formulations can be ignored

(b) relevant approximation can be considered

(c) model complexity and hence the computational effort are reduced

However, to make the model simple, imposed approximations and constrained should be examined carefully. THz HBT modeling via SPICE based approach has been detailed in Stein (2014). A brief discussion regarding the compact modeling approach is presented in the following section.

A compact model is a physics-based mathematical description of the electrical behavior of a device that is incorporated in the circuit simulator. Typically, a compact model features (i) a high-level accuracy over a wide temperature and bias range, (ii) stability on numerical computation, (iii) minimum number of scalable model parameters, and (iv) low-execution time. Additionally, there should exist a reliable model parameter extraction approach. Physics-based well-known models for bipolar transistor are Gummel-Poon Getreu (1976), VBIC McAndrew *et al.* (1995), MEXTERM Kloosterman (1996), and HICUM Schröter (2005). HICUM L2 has been considered in this work for HBT modeling. Therefore in the next part, we discuss the evaluation of HICUM and the important physical effects that have been incorporated in the model.

HICUM (HIgh CUrrent Model) is a compact model for the description of the high-current behavior of the bipolar transistor. Nowadays HICUM is available in a wide range of circuit simulators like ADS, HSPICE, ELDO, SPECTRE, APLAC, AnalogOffice, GoldenGate, etc. The motivation behind the HICUM was the inaccurate behavior of the SPICE Gummel-Poon-Model (SGPM) mainly at the high current densities. HICUM model development was started at mid eighties Schröter and Rein (1985), Rein *et al.* (1985) and first large-signal dynamic behavior was reported just after two years Rein and Schroter (1987), Schröter and Rein (1989). After experimentally verified the small-signal formulation Koldehoff *et al.* (1993), the model is first implemented into a commercial circuit simulator (in ELDO and SPECTRE). Further to simply the model implementation and to set the standard interfaces (to obtain the same implementation and results across all commercial circuit simulators) compact model coalition (CMC) was formed in the late nineties. After evaluating model accuracy through various process technologies, in 2003 HICUM was considered as one of two standard models although due to the unavailability of a standard simulator interface (and compiler), model simulation became an immediate burden. But later in 2004, an advanced model compiler (takes high-level Verilog-A as input and translates it to C as output code) was developed and the burden of compact model implementation into any kind of circuit simulator was significantly reduced. As a result, HICUM has been employed in production design fabricated at leading SiGe foundries around the world.

In HICUM, the extended and generalized integral charge-control-relation (GICCR) has been employed Schröter *et al.* (1993). HICUM takes into account the following important physical effects:

- emitter current crowding (via bias-dependent internal base resistance)
- emitter periphery injection and associated charge storage
- distributed high-frequency model for the external base-collector region
- high-current effects
- two and three dimensional collector current spreading
- vertical non-quasi-static effect for transfer current and minority charge
- tunneling at the base-emitter junction

- weak avalanche breakdown at the base-collector junction
- parasitic capacitance between base-emitter and base-collector terminal
- parasitic substrate transistor
- bandgap difference
- temperature difference and self-heating
- lateral (geometry) scalability

The large-signal equivalent circuit of HICUM is shown in Fig.1.10. The internal transistor is shown in the dotted box including the nodes E', B', and C'. The base-emitter diode part is modeled by the diode current i_{jBEi} and junction charge Q_{jEi}. The diffused forward base-emitter minority charge is modeled by Q_f. Same for the base-collector side are i_{jBCi}, Q_{jCi}, and Q_r. Base-emitter tunneling current and base-collector avalanche current are modeled by i_{BEti} and i_{AVL} respectively. The collector-emitter transfer current is modeled by i_T. These above-mentioned components are included in the internal transistor. On one side, the external base node (B*) is connected to B' via internal base resistance (R^*_{bi}) and on the other side B* is connected to base contact (B) via external base resistance (R_{Bx}). The peripheral and parasitic components between the base-emitter and base-collector terminals are modeled between B and B* nodes. Finally, the substrate network (R_{su} and C_{su}) is connected to the internal collector node (C') via the internal substrate node (S') and collector-substrate diode network.

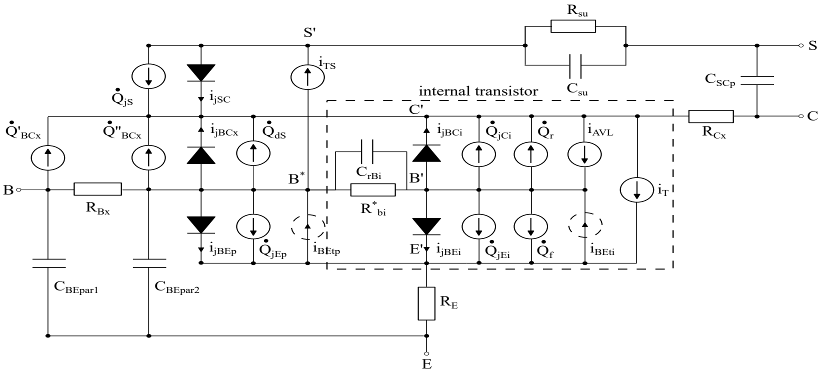


Fig. 1.10: Large-signal equivalent circuit of HICUM L2v2.4 compact model Schröter and Pawlak (2017).

Working in the advanced technology node offers attractive FoMs with a cost of increased process complexity and packing density. Typically, modern integrated circuits contain more than 1 billion transistors with the other circuit elements. So in this regime, the performance of the entire chip is more crucial than the discrete components. To achieve reliable performance and reduce the overall manufacturing cost, a first-pass design methodology can be one of the key solutions. However, this methodology requires an accurate characterization method, improved compact models, and robust & accurate parameter extraction tool.

The purpose of device modeling is to provide a design kit to the foundry consumers for the mixed-signal circuit simulation. A mixed-signal/RF PDK (process design kit), a set of data, enables circuit designers to simulate integrated circuits in widely available software using various tools. Electronic device automation (EDA) for a given process can also be done having such PDK. To accurately replicate the device characteristics with growing processing technologies, compact models have to hold on to improved model equations and associated model parameters. Compact model parameters, a part of PDK, are considered sufficient data to achieve first-pass design success. However, to track an aggressively scaled device operating in extreme bias conditions, a compact model often faces limitations Celi (2006), meaning that the compact model response becomes unacceptable. Although some of such limitations can be defeated Pawlak *et al.* (2009), Huszka *et al.* (2011*a*), Huszka *et al.* (2011*b*).

1.4 Project

This work is part of the TARANTO (ECSEL RIA) European project. Although here we briefly discuss the previous projects which were devoted to the development of SiGe BiCMOS technology.

- DOTFIVE (FP7 HBTPoC) DOT (2008-2010):
  With support from the European Government, this project aimed to develop SiGe HBT architecture with a cut-off frequency up to 500 GHz. For the silicon-based transistor, this project mainly addresses the required key technologies for the pro-

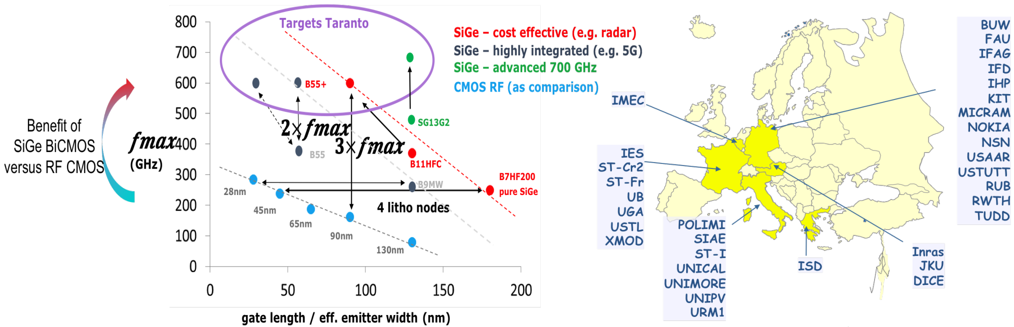
duction in large volume. Transistors are fabricated under this project, can suitable for millimeter-wave applications like 77 GHz automotive radar, 60 GHz wireless local network, etc. In collaboration with five European countries and various partners from industry and academia, this project was successfully reached its goal Heinemann *et al.* (2010). The partners were STMicroelectronics (France), Infineon (Germany), IHP (Germany), IMEC (Belgium), XMOD Technologies (France), IMS Laboratory (France), TU Dresden (Germany), University Wuppertal (Germany), Bundeswehr University Munich (Germany), TU Delft (Netherlands), University of Naples (Italy), etc.

- RF2THZ SiSoC (CATRENE) RF2 (2011-2013):
  To fulfill the demand for future RF and high-speed equipment, this project aimed to develop millimeter-wave and THz consumer applications mainly on silicon-based bipolar transistor platforms. The partners, involved in the projects were STMicroelectronics (France), NXP Semiconductors (France, Netherlands), IHP (Germany), Alcatel Lucent (Germany), BOSCH (Germany), Agilent Technologies (Germany), XMOD Technologies (France), IMS Laboratory (France), TU Dresden (Germany), Fraunhofer (Germany), TU Delft (Netherlands), TU Eindhoven (Netherlands), ESIEE (France), ENSICAEN (France), IEMN (France), NEWTEC (Belgium), etc.

- DOTSEVEN (FP7 HBTPoC) DOT (2012-2014):
  Like DOTFIVE, in this project, the target was set to reach the cut-off frequency up to 700 GHz. With successful participation of the partners in the industry and academia (Infineon (Germany), Dice Danube Integrated Circuit Engineering (Austria), IHP (Germany), XMOD Technologies (France), IMS Laboratory (France), TU Dresden (Germany), University Wuppertal (Germany), TU Delft (Netherlands), University of Naples (Italy), etc.), the goal was reached Heinemann *et al.* (2016).

- TARANTO (ECSEL RIA) TAR (2017-2020):
  The acronym TARANTO stands for **T**ow**AR**ds **A**dvanced bicmos **N**ano **T**echnology platforms for rf to the applicati**O**ns.

The main objectives of this project were to explore the possibilities of the HBTs that were developed in the previous projects along with required adjustments between the BiCMOS and CMOS technologies (Fig. 1.11a). Following DOT-SEVEN, TARANTO aimed to develop a more robust fabrication process to achieve high-level transistor performance. Based on the application, such fabrication has been categorized into two types; first, to address the millimeter-wave applications (like automotive radar, wireless local area network, imaging, etc.), SiGe HBT is fabricated on the low-cost CMOS (130/90 nm), and second to improve the data communication rate (like 5G, 6G, and beyond) SiGe HBT is fabricated on the advanced CMOS node (55/28 nm). Apart from such ideas, TARANTO also targets to develop the device characterization tools and improved modeling perceptive to achieve quick technology evaluation mainly for designing millimeter-wave integrated circuits. Currently, 6G precursor and transceiver are developed under this project. Fig. 1.11b shows the members from the various participating countries.



(a) (b)

Fig. 1.11: European project TARANTO (ECSEL RIA): roadmap (a), and participating industry and academia (b) (source: TAR (2017-2020)).

1.5 This thesis

With emerging BiCMOS technologies, rapid evaluation of the figure-of-merit (FoM) of modern transistors is one of the serious challenges. Generally to qualify for RF applications (e.g., power amplifier or low-noise amplifier), technologist often attempts to estimate the f_{MAX} quickly from measured data. However, f_{MAX} shows noisy behavior with significantly uncertain values when calculated from measured y-parameters leading to a serious problem while evaluating a technology. Therefore, a methodology is required which can effectively mask the noisy data and help in predicting an accurate f_{MAX} without delaying the technology evaluation. Hence for a quick and reliable estimation of f_{MAX}, we propose an analytical approach Saha *et al.* (2021) based on the small-signal hybrid-π model of SiGe HBTs. Frequency-dependent y-parameters polynomials are formulated into corresponding real and imaginary forms. Once this is done, Mason's gain formula is used to calculate f_{MAX}. The model is interpolated directly on the measured data with the least-mean square-based interpolation technique. We have also verified this model by measuring f_{MAX} following a structure having a different back-end-of-lines.

Modern BiCMOS technologies not only pose serious challenges in accurate device characterization, but also bring out significant second-order effects such as the ones arising from graded doping in the substrate. For example, 55 nm BiCMOS process Chevalier *et al.* (2014) has a deep trench in its architecture and it is placed in between the substrate contact and the buried layer. Comparing the measured data from this technology, we observed a significant inaccuracy in predicting the frequency-dependent output scattering parameter s_{22} by the state-of-the-art compact model, HICUM. Since an inaccurate output impedance model affects the circuit's gain, a corresponding model improvement is in high demand. Therefore, we present an improved collector-substrate model that takes care of the associated impacts of the peripheral substrate region in a deep trench isolated structure [Saha *et al.* (2019)]. The proposed model is implemented into HICUM with a SPICE base approach and studied the overall impact in high-frequency characteristics up to 330 GHz with de-embedded measured data at cold and peak f_T forward bias condition.

At the high-frequency regime, non-ideal effects (e.g. vertical and lateral non-quasi-static effects) show up in the device characteristics which need to be modeled appropriately to improve the accuracy of the compact model. In the existing literature, limited model evaluation has been performed mainly using TCAD data only. Also, the effects of certain capacitance partitioning factors were not elaborately presented. From these perspectives, we investigated the very high-frequency behavior of the modern BiCMOS 55 nm SiGe HBT process using measured data till 500 GHz, calibrated TCAD simulation and suitable parameter extraction approaches Saha *et al.* (2021). Extracted HICUM based high-frequency compact model parameters are ***alit***, ***alqf***, ***fcrbi***, ***fbepar***, and ***fbcpar***.

1.6 Thesis organization

The aim of the thesis is to investigate and model the high-frequency effects in SiGe HBT and to improve the state-of-the-art compact model. Chapter 2 reviews the survey on the available state-of-the-art literature. Based on an analytical model, an approach is shown in chapter 3 to estimate f_{MAX}. In chapter 4, we present a proposal for an improved collector-substrate model. In chapter 5, we discuss the high-frequency behavior of SiGe HBT and present an approach to extract some of the specific high-frequency compact model parameters. Finally, conclusions are drawn in chapter 6.

CHAPTER 2

AVAILABLE STATE-OF-THE-ART IN LITERATURE

2.1 Introduction

From the last few decades, especially after successful completion of DOTFIVE and DOTSEVEN projects from European Union, silicon germanium heterojunction bipolar transistor (SiGe HBT) has been treated as one of the main high-frequency devices in radio frequency applications. Although, in high-frequency regime non-ideal effects come into play and degrade the overall device performance. In spite of such barriers, modern SiGe HBTs have been demonstrated 700 GHz maximum oscillation frequency f_{MAX}. However, it is found that noisy measurements and inaccurate modeling especially at high-frequencies hinders the technology assessment and reliability in circuit design.
In this chapter, we intend to give a review of existing modeling approaches and techniques that are used either for extraction of figure-of-merits (FoMs) or to check the accuracy of the compact model. This served as a motivation for the work presented in later chapter of this thesis. In subsection 2.2.1, conventional techniques for f_{MAX} extraction is presented. Subsection 2.2.2 reviews the modeling approaches that are used for deep trench-based HBT architecture. The existing high-frequency compact modeling evaluation approach is discussed in subsection 2.2.3. Finally, this chapter concludes by stating the objectives of the present work.

2.2 Review

2.2.1 Conventional f_{MAX} extraction approach

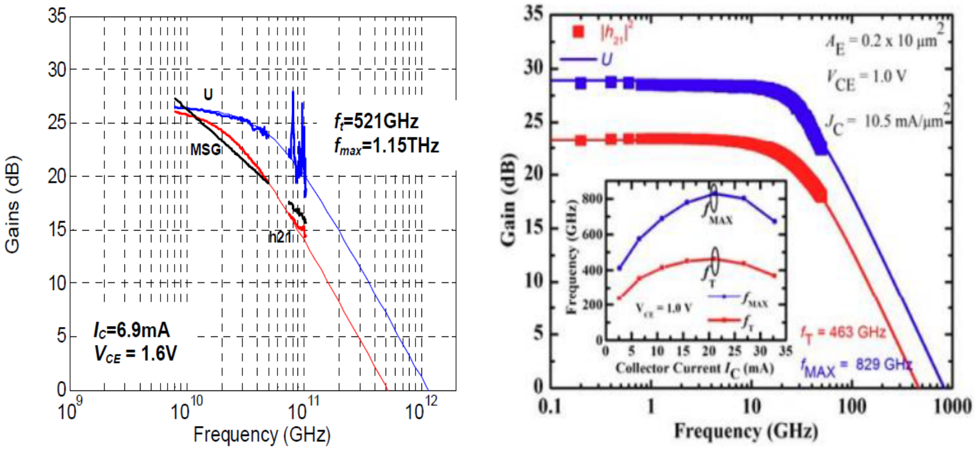
The f_{MAX} is the frequency at which the power gain (in decibel scale) is reduced to zero. Generally, f_{MAX} is extracted from the unilateral gain versus frequency plot. In terms of y-parameters the unilateral gain is expressed as,

$$U = \frac{|y_{21} - y_{12}|^2}{4[Re\{y_{11}\}Re\{y_{22}\} - Re\{y_{12}\}Re\{y_{21}\}]}. \tag{2.1}$$

where y_{ij} are the two-port y-parameters. Once this is done, f_{MAX} is calculated using the following relation

$$f_{MAX} = f\sqrt{U} \tag{2.2}$$

where f is the frequency of measurement. In Urteaga *et al.* (2011), f_{MAX} is extracted following the conventional approach, but such extraction is limited because (i) extrapolation is sensitive to measurement noise (ii) the extracted f_{MAX} value is 1 decade higher than the measurement range (Fig. 2.1a). Therefore, from the perspective of technology assessment, the extracted value is unreliable. In another approach Arabhavi *et al.* (2018), a single pole transfer function was fitted on the measured frequency-dependent unilateral gain characteristics (Fig. 2.1b). Note that a single pole transfer function possesses a constant slope of -20 dB/decade in a given frequency regime. On the other hand, due to the presence of second order and substrate coupling effects, the observed roll-off in the measured f_{MAX} at the high-frequency regime is higher than -20 dB/decade. Considering this issue, the fitted single pole transfer function approach is not suitable for trustworthy f_{MAX} extraction.



(a)

(b)

Fig. 2.1: Examples of f_{MAX} extraction following the conventional process: U-based extrapolation Urteaga *et al.* (2011)(a), and single pole transfer function fitted on U Arabhavi *et al.* (2018)(b).

2.2.2 Substrate model of bipolar transistor

For design of the high-speed circuit, accurate substrate modeling is very important, especially in the structure with a deep trench near the substrate contact. This is due to the fact that inaccurate modeling affects the circuit gain that is directly dependent on the output impedance. Moreover, graded doping at the peripheral region results the non-uniform current flow in the substrate and substrate material properties (resistivity and permittivity) determine the substrate cut-off frequency which is essential for high-speed circuit design. Adverse substrate effects and reported potential modeling approaches are addressed here. At high-frequency, typical substrate effects include coupling to circuit elements and cross-talk from parasitic components.

In Pfost *et al.* (1996), numerical simulator was used to calculate the substrate effects, but it was verified up to 20 GHz. Using the guard ring was proposed in Strahle and Pfost (2003) only for critical circuit components since the substrate coupling is not uniform between all components in the circuits.

Due to time and cost constraints, possible substrate effects cannot be calculated by measuring dedicated structures. For simple geometries, analytical formulations are used. On the other hand, due to long simulation time, computer aided programs are not well-suited for rapid and reliable circuit design. Hence, to overcome such situations, special computer-assisted programs have been developed. These are the finite element method (FEM) Kerns *et al.* (1996), Pfost *et al.* (1996), Hermann *et al.* (2000) and the boundary element method (BEM) Gharpurey and Meyer (1996), Brandtner and Weigel (2004).

As the name indicates in FEM, the entire volume is partitioned into distinct small or large volumes. This leads not only to accurate modeling, but also to local variation of electrical properties that can be accurately taken into account. Then the device with various features like deep trenches, graded doping and stop channel can be modeled properly by FEM. However, due to incorporation of many distinct volumes, this process is restricted to a few tens of circuit elements in order to avoid long simulation time.

In practical circuit design, the relationship between current and voltage is more consistent. BEM approach is based on this principle. Since the interactions of the components with the substrate are not uniform, a particular volume with the greatest interaction can be partitioned using this method. Although in terms of computation time and stored simulated data (related to memory space) BEM is superior to FEM. However, the BEM approach is limited to only a few thousands volumes because of computing time. Since BiCMOS technology features both high-packing density (advantage from CMOS) and high-speed (advantage from Bipolar); therefore the applicability of both approaches is limited in the design of high-speed circuits.

In contrast to such volume-based approaches (FEM and BEM), the part of the substrate can be modeled by considering an equivalent circuit. In general, the components of the equivalent circuit are resistance and capacitance, while resistance models DC behavior and capacitance model AC behavior such that the product

$$RC = \rho\epsilon \tag{2.3}$$

where ρ is the resistivity and ϵ is the permittivity of the material. Using equation 2.3 the substrate cut-off frequency (f_C) can be calculated as

$$f_C = \frac{1}{2\pi\rho\epsilon}. \tag{2.4}$$

From the very basic bipolar transistor model (such as SPICE Gummel-Poon) to advanced models (such as VBIC, MAXTERM and HICUM) all considered the equivalent circuit approach to model the substrate.

Such lumped element based approach was used in Fregonese *et al.* (2005) for modeling deep trench based architectures by comparing the simulation result with 110 GHz measured data. Due to advances in process technology, the frequency of operation of the transistor is growing rapidly, so the verification of the model proposed in Fregonese *et al.* (2005) is in high demand.

2.2.3 Compact model evaluation

The more precise the compact model response, greater the accuracy in the circuit design. Due to the presence of non-idealities in the behavior, especially at high-frequency, circuit performance is degraded unless it is modeled correctly. As the frequency of operation heading towards the transit frequency (f_T), non-quasi-static effects (NQS) begin to influence the frequency-dependent small-signal and transient large-signal characteristics due to delays experienced by the stored minority charge. Like NQS, proper partitioning of the parasitic capacitances is also important. Since in the last two decades HICUM has been used as a standard compact bipolar model for the transistor, hence we have further checked the accuracy of this compact model with high-frequency measured data and calibrated TCAD simulation.

In Voinigescu *et al.* (2012) different versions of the HICUM model (Level 0 and Level 2) were analyzed as well as the description of the high-frequency parameter extraction approach. However, the observation was made only in s_{21}, h_{21} and Mag (U) up to 325 GHz by scaling the junction capacitances and partitioning the resistances which were considered as sufficient measures for accurate modeling. In fact, accurate extraction of junction capacitances, internal and external resistances along with the partitioning of the parasitic capacitances are essential for accurate modeling of the compact model but as of now no methodologies have been reported.

In Galatro *et al.* (2017), considering an integrated thru-reflect-line (TRL) calibration/de-embedding kit, a transistor was measured in the millimetre wave regime and then compared with latest HICUM L2. However, compact model accuracy was observed only in one frequency band.

2.3 Objective of this work

To summarize, first, we discussed the issues regarding the f_{MAX} extraction following the conventional methods. Since the extraction following the method of extrapolation is prone to noise, hence the extracted value hardly reliable. On the other hands, substrate and high-frequency effects lead to f_{MAX} roll-off higher than -20 dB/decade, therefore f_{MAX} extraction following a unilateral gain versus frequency characteristics with a fitted single pole transfer function based approach cannot be followed. In the case of collector-substrate model, we saw that in Fregonese *et al.* (2005) the necessary model elements were extracted but had not been verified with very high-frequency measured data. Next, concerning the accuracy of the HICUM compact model, the work shown in the existing litterateurs seem limited in terms of presenting data. Therefore, in this thesis we have addressed these cases.

- For f_{MAX} extraction method:

  The main objective is to develop an analytical model for fast and reliable extraction of f_{MAX}. Additionally, our aim is to formulate a model which can not only extract f_{MAX} in the low-frequency noise regime, but also track f_{MAX} in the high-frequency regime where the roll-off is higher than -20 dB per decade.

- For an improved collector-substrate model:

  Following the formulation in Fregonese *et al.* (2005), our objective is to check the very high-frequency response of the state-of-the-art compact model HICUM and incorporate the components into the equivalent circuit of the compact model.

- For compact model evaluation and high-frequency parameter extraction:

  Finally, here our objective is to extract some high-frequency compact model parameters based on TCAD based calibrated structure than using those extracted values accuracy of the state-of-the-art compact model has been analyzed up to 500 GHz.

CHAPTER 3

FAST EVALUATION OF f_{MAX} FOR SiGe HBTs

3.1 Introduction

The demand for increased functionality and speed of modern communication system drives the evaluation of various transistor technologies Bennett *et al.* (2005). These unique technologies differ from one another in terms of doping profiles, geometries and structures. In this rapid development, heterojunction bipolar transistors (HBTs) or advanced CMOS technologies find applications in millimeter and sub-millimeter range Rieh *et al.* (2004), Orner *et al.* (2006), Joseph *et al.* (2018). In this region of applications, realizations of power amplifiers and low-noise amplifiers are limited by transit frequency (f_T) and maximum oscillation frequency (f_{MAX}). Also to achieve the required functionality, f_T and f_{MAX} should be at least three to four times higher than the operating frequency. The present state-of-the-art SiGe HBTs are shown to have f_T above 500 GHz and f_{MAX} above 720 GHz at room temperature Heinemann *et al.* (2016), and additional studies reveal these parameter values heading towards terahertz level Schroter *et al.* (2011), Chevalier *et al.* (2018). For a trustworthy evaluation of such a technology under development, it would be very useful to have a quick and reliable estimation methodology for the corresponding f_T and f_{MAX}.

In fact, the maximum oscillation frequency, f_{MAX}, is one of the most important figure of merits of the bipolar junction transistor. Since as of now, direct measurement of f_{MAX} is often not possible. Measurement equipment up to 750 GHz are very rare in research labs and not available at all in industry where the SiGe-HBT development is carried out. Thus, f_{MAX} has been calculated following the Mason's gain formula Mason (1954) based on y- or s-parameters. Due to significantly small amplitude of measured admittance (or y)-parameters Rimmelspacher *et al.* (2019), Teppati *et al.* (2014), it is extremely difficult to measure these parameters correctly even using highly calibrated measurement benches. Hence, calculated f_{MAX} comes out noisy mainly at the low frequency regime. Therefore, to get rid-off the measurement noise, it is desirable to adopt a strategy which can bring the frequency independent f_{MAX} and predicting the technology specific designed value. So, in this chapter following a standard physics based analytical small-signal hybrid π-model Giacoletto (1969) we propose a methodology to predict the technology specific f_{MAX} Saha *et al.* (2021). The analytical formulations are interpolated using the well-known least-mean square based interpolation technique and the f_{MAX} value has been estimated.

3.2 State-of-the-art f_{MAX} extraction

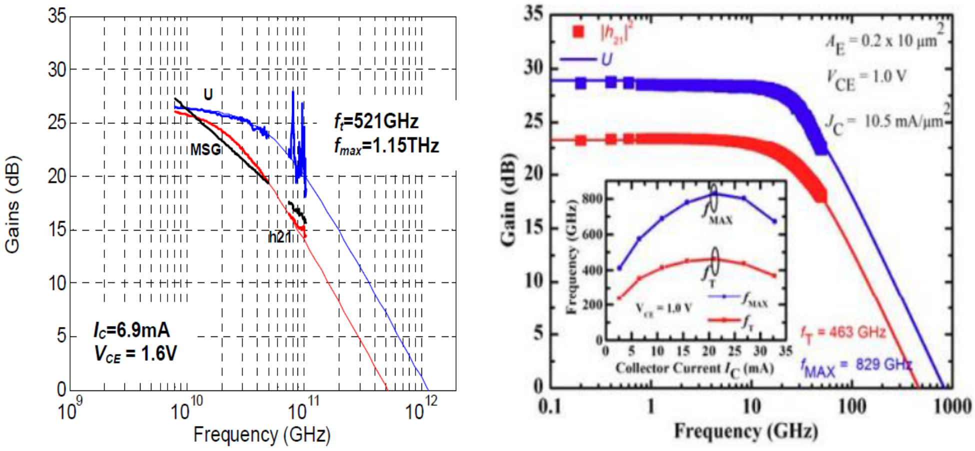
The traditional approach for the determination of f_{MAX} consists extrapolation to zero from the frequency dependent characteristics of unilateral gain (U) or maximum available gain (MAG) or maximum stable gain (MSG). Conventionally, to extract the f_{MAX} a line of slope (-20 dB/decade) is drawn either using a fitting function Urteaga *et al.* (2011) or using a single pole transfer function Arabhavi *et al.* (2018) on the U(f) curve. From Fig.3.1, we can see that the predicted f_{MAX} comes more than 1 decade higher than the measurement range and such extrapolated values are prone to under- or overestimation from the real value since extrapolation is very sensitive to measurement errors.

Another method to obtain f_{MAX} is to calculate following the formula square-root of U(f) multiplied with frequency Voinigescu *et al.* (2012), Heinemann *et al.* (2016), Yau *et al.* (2012).

$$f_{MAX} = f\sqrt{U} \tag{3.1}$$

where f is the frequency of measurement and U being the Mason's gain Mason (1954) expressed in two-port parameters as

$$U = \frac{|y_{21} - y_{12}|^2}{4[Re\{y_{11}\}Re\{y_{22}\} - Re\{y_{12}\}Re\{y_{21}\}]}. \tag{3.2}$$



(a) (b)

Fig. 3.1: Examples of f_{MAX} extraction following the conventional methods: RF gains of 0.13 μm $\times$ 2 μm InP HBT, from Urteaga *et al.* (2011) (a) and Short circuit current gain mag (h_{21}) and Mason's unilateral gain U from 2 to 50 GHz. f_T and f_{MAX} are extrapolated from a single pole transfer function (inset: dependence of f_T on I$_C$ at V$_{CE}$=1V), from Arabhavi *et al.* (2018) (b).

In a first approximation f_{MAX} is supposed to be independent of frequency since U varies inversely with the square of frequency in (3.1). It appears that f_{MAX} starts to decrease slightly from the mid-frequency range where the -20dB/decade roll-off approximation of the power gain is no more valid. This decrease is mainly due to the influence of the substrate capacitance, and dependent on the technology, its influence is more or less pronounced. Other second order effects can also play role in the decrease of f_{MAX}, when the measured frequency approaches f_{MAX}. But even in the lower frequency range, it is quite difficult to obtain a nearly constant f_{MAX} using (3.1) over frequency mainly because of the extremely low magnitude and measurement uncertainty of some of the measured y-parameters Teppati *et al.* (2014), Rimmelspacher *et al.* (2019). As a consequence, the extracted f_{MAX} is very noisy over frequency. Such a fluctuation poses serious confusion to the technologist while evaluating and optimizing a given technology. Very often, an already obtained performance improvement is masked by the measurement and estimation error in f_{MAX}; subsequently an unambiguous announcement of the actually obtained technology advancement is hindered. Hence, it is desirable to adopt a strategy that quickly estimates a frequency-independent f_{MAX} even from a noisy experimental data.

Fig. 3.2 from Heinemann *et al.* (2016) underlines the above statement. It represents the world record data in terms of f_{MAX} for a SiGe HBT technology. The same device was measured at two different locations (at IHP and Infineon). The results appear to be similar, but a large fluctuation is observed (f_{MAX} varies from below 600 GHz to above 800 GHz for the IHP measurements, and between 700 GHz to 800 GHz for the Infineon measurements). A straightforward determination of the actual f_{MAX} value seems impossible, but is mandatory for the assessment of technology performance.
Note that the f_{MAX} calculation at the individual frequency point gives a clear idea in which frequency range a true f_{MAX} belongs.

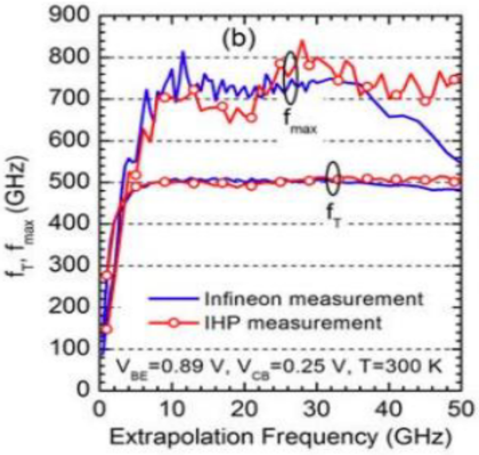


Fig. 3.2: Dependence of f_T and f_{MAX} on extrapolation frequency for the same HBT measured at IHP and Infineon. SOLT calibration with an impedance standard substrate (ISS) is applied from Heinemann *et al.* (2016).

3.3 Model Development strategy

First to address the question what is a model, we say that based on some equations with assumptions and constraints, a model describes a system and it is based on mathematics. The main job of the scientific model is to do the simulation to understand the behavior of the device under study. Such developing models should always reference to the exiting and accepted models. Broadly there are four types of model in scientific community, they are conceptual model, operational model, mathematical model and graphical model. Fig. 3.3 describes the cycle of modeling approach used in scientific community. In this chapter, we have used the small-signal hybrid π-model (as a conceptual model) to develop the analytical formulations (as a mathematical model) for the rapid evaluation of a specific technology.

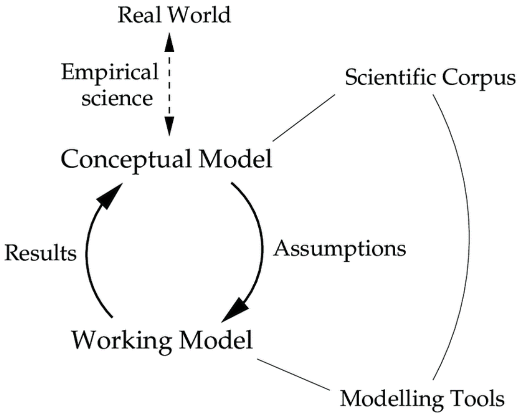


Fig. 3.3: Cycle of scientific modeling (source: Bryden (2007)).

3.3.1 Basic model: small-signal hybrid π-model and approximations

To develop our model, we took the standard physics-based small-signal hybrid π-model of the bipolar transistor, shown in Fig. 3.4 where R_{Bx} and R_{Bi} are the external and internal base resistance respectively and r_π and r_0 are the internal base-emitter and collector-emitter resistance respectively. R_c and r_E are the external collector and emitter series resistance respectively. While C_{bc}, C_μ and C_π are the external base-collector, internal base-collector and internal base-emitter capacitors and g_m is representing the trans conductance.

Now to simplify the analytical formulations, Fig. 3.4 is further modified to Fig. 3.5, where the resistance R_{BiT} stands for a single resistance considering the external (R_{Bx}) and internal base resistance (R_{Bi}) and we neglect the impact of emitter resistance (r_E). Merging the external (R_{Bx}) and internal base resistance (R_{Bi}) is possible because distributed effects are only important for measurement beyond 100 GHz, which is not the case in this study.

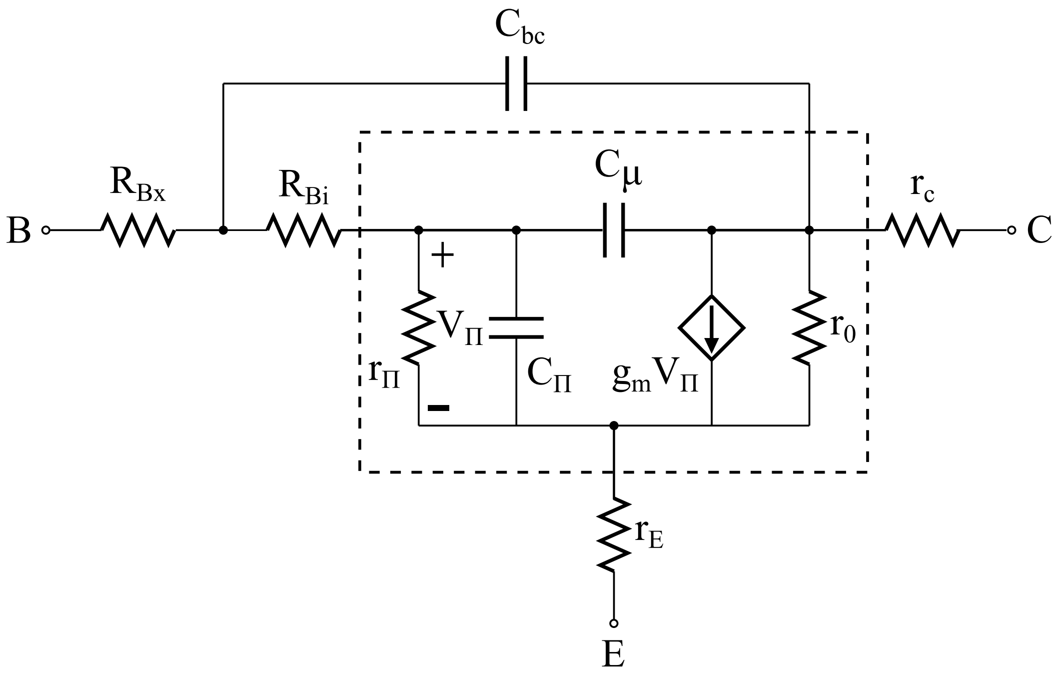


Fig. 3.4: Conventional hybrid π-equivalent circuit model for HBT. Dashed box represents the intrinsic transistor model.

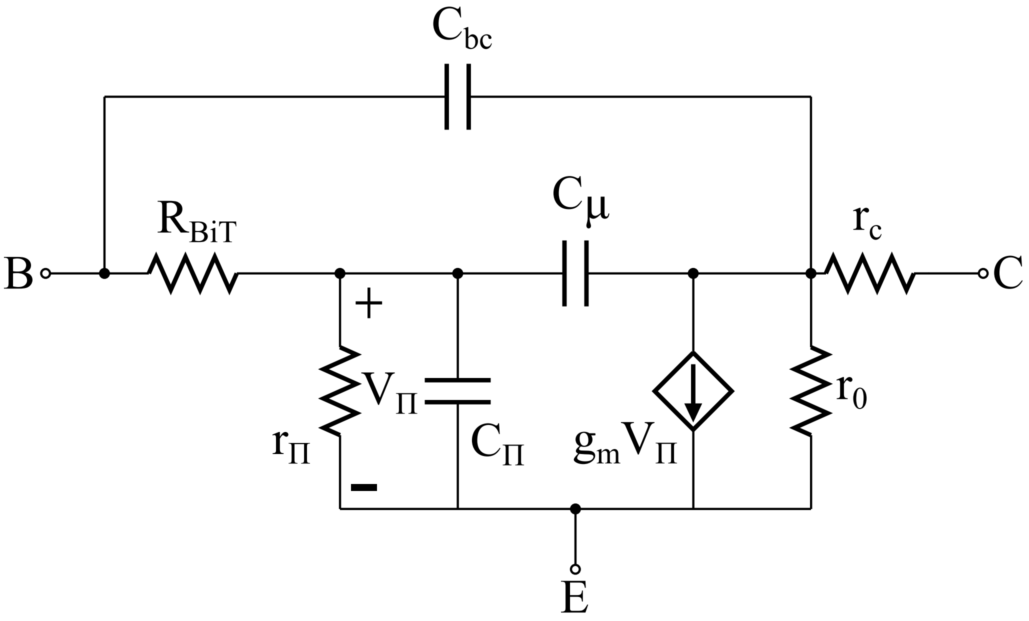


Fig. 3.5: Simplified hybrid π-model of HBT.

3.3.2 Y-parameters in high-frequency analysis and its significance

In a next step, the circuit shown in Fig. 3.5 is described analytically with small-signal parameters. From the various small-signal parameters available (z-, h-, y-, $ABCD$- or s-parameters), we have chosen the admittance parameters or y-parameters, which are most frequently used by electrical engineers to evaluate the circuit characteristics. They are defined as the ratio of current to voltage at the short-circuit hybrid condition, hence the name short-circuit admittance parameter. (Table 3.1) represents the four y-parameters of a two-port network.

Table 3.1: Definition of the four y-parameters of a two-port network.

y-parameters	Ratio (i/v)	Hybrid condition
y_{11} (input admittance)	(i_1/v_1)	Output short circuit (v_2=0)
y_{21} (forward transfer admittance)	(i_2/v_1)	
y_{12} (reverse transfer admittance)	(i_1/v_2)	Input short circuit (i_1=0)
y_{22} (output admittance)	(i_2/v_2)	

Where i_1,v_1 (i_2,v_2) are the input (output) current and voltage respectively.

In the present study, the Mason gain is expressed as a function of the y-parameters (equation 3.2), so an analytical expression based on the equivalent circuit (Fig. 3.5) will be the starting point for our analysis.

3.3.3 Model formulation

As already mentioned, f_{MAX} is calculated following equation (3.1) where unilateral gain is expressed in equation (3.2) with y_{ij} being the y-parameters obtained at a frequency of operation.

In order to be able to predict f_{MAX} using (3.1) and (3.2), here we attempt to express the overall y-parameters of the equivalent circuit model of Fig. 3.5 starting from the intrinsic model given within the dashed box of Fig. 3.4. Two-port analysis of the intrinsic model of Fig. 3.4 (given within the dashed box) yields the angular frequency (ω) dependent complex y-parameters as,

$$y_{11i} = \frac{1}{r_\pi} + j\omega(C_\pi + C_\mu) \tag{3.3}$$

$$y_{12i} = -j\omega C_\mu \tag{3.4}$$

$$y_{21i} = g_m - j\omega C_\mu \tag{3.5}$$

$$y_{22i} = \frac{1}{r_0} + j\omega C_\mu. \tag{3.6}$$

Considering base series resistance (R$_{BiT}$) and collector-base capacitance (C$_{bc}$) from Fig. 3.5, y-parameters expressions are modified to,

$$y_{11x} = \frac{y_{11i}}{1 + R_{BiT}y_{11i}} + j\omega C_{bc} \tag{3.7}$$

$$y_{12x} = \frac{y_{12i}}{1 + R_{BiT}y_{11i}} - j\omega C_{bc} \tag{3.8}$$

$$y_{21x} = \frac{y_{21i}}{1 + R_{BiT}y_{11i}} - j\omega C_{bc} \tag{3.9}$$

$$y_{22x} = \frac{y_{22i} + R_{BiT}\Delta y_i}{1 + R_{BiT}y_{11i}} + j\omega C_{bc} \tag{3.10}$$

where $\Delta y_i = y_{11i}y_{22i} - y_{12i}y_{21i}$. Further considering r$_C$ in series with internal collector, the modified expressions of y-parameters become

$$y_{11T} = \frac{y_{11x} + r_c\Delta y_x}{1 + r_c y_{22x}} \tag{3.11}$$

$$y_{12T} = \frac{y_{12x}}{1 + r_c y_{22x}} \tag{3.12}$$

$$y_{21T} = \frac{y_{21x}}{1 + r_c y_{22x}} \tag{3.13}$$

$$y_{22T} = \frac{y_{22x}}{1 + r_c y_{22x}} \tag{3.14}$$

where $\Delta y_x = y_{11x}y_{22x} - y_{12x}y_{21x}$.

Formulations (3.11) to (3.14) yield the complete y-parameters of the equivalent circuit of Fig. 3.5. Now, in order to use these equations for predicting f$_{MAX}$ using (3.1) along with (3.2), we express (3.11) to (3.14) into real and imaginary parts.

The analytical treatment leads to long expressions and is presented in APPENDIX A for the sake of readability of this document. To sum up, we arrive at the following equations, which show the compact representation of the equations above derived in the real and imaginary forms of the y-parameters.

$$\mathrm{Re}\{y_{ij}\} \simeq \frac{a_{1,ij} + a_{2,ij}\omega^2}{1 + a_{3,ij}\omega^2}, \tag{3.15}$$

$$\mathrm{Im}\{y_{ij}\} \simeq \frac{b_{1,ij}\omega}{1 + b_{2,ij}\omega^2}. \tag{3.16}$$

Where $a_{1,ij}$, $a_{2,ij}$, $a_{3,ij}$ and $b_{1,ij}$, $b_{2,ij}$ are the coefficient and the function of small-signal parameters. Note that for $\mathrm{Re}\{y_{12}\}$, $a_{1,12}$ = 0. The determination of the parameters in (3.15) and (3.16) are done in the following way. First, the technique of division of polynomial is performed to normalize with respect to the first term in the denominator up to second order in ω. Secondly, the quadratic regression is applied to obtain the parameters. The advantages of this procedure are that (i) the interpolated y-parameters are obtained immediately and (ii) the measured noise is eliminated. Also use of optimization procedures such as the well-known Levenberg-Marquardt algorithm yields comparable results.

3.4 Results and discussion

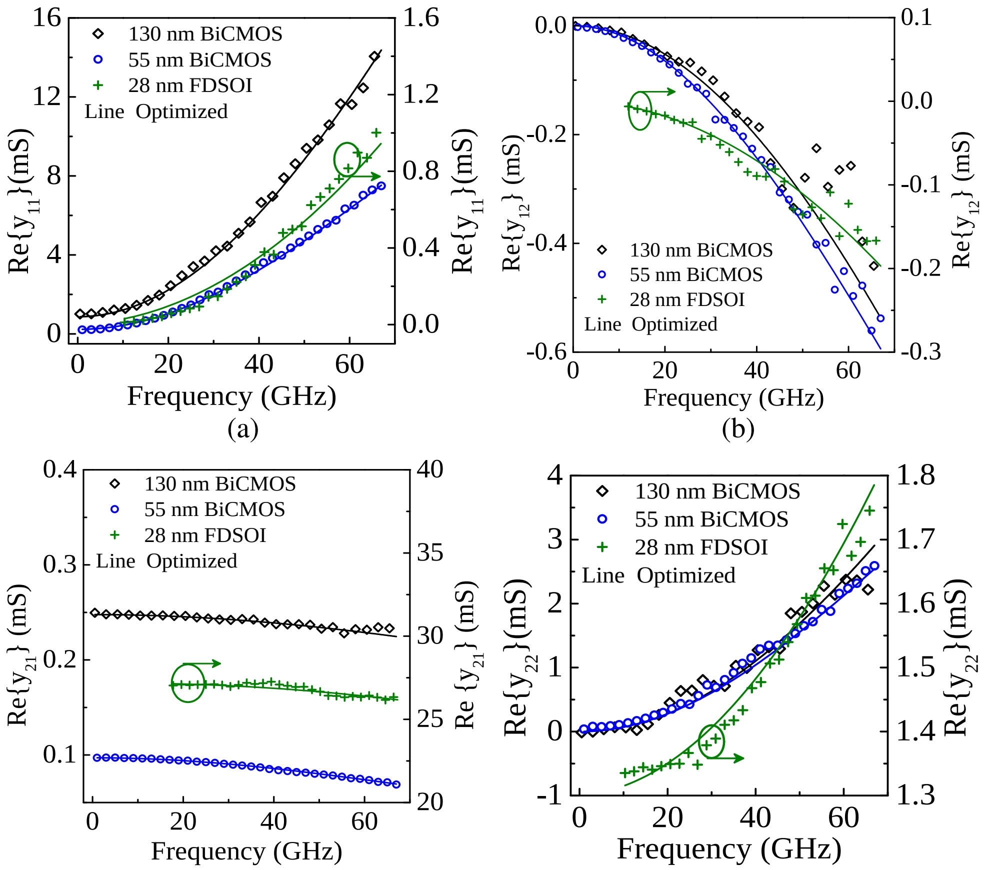
To test the utility of the closed-form equations, small-signal s-parameter measurements of SiGe HBT are performed on two different technologies. One of them represents an intermediate status of HBT developments Böck *et al.* (2015) based on a 130 nm BiCMOS platform. The corresponding 8-finger transistor with an effective emitter area of 8 × (0.105 µm × 1 µm) is biased at V_{CB} = 0.25 V and V_{BE} = 0.89 V. The second technology concerns a 55 nm BiCMOS platform Chevalier *et al.* (2014) and the corresponding SiGe HBT with an effective emitter area of 0.09 µm × 4.8 µm is biased at V_{CB} = 0.5 V and V_{BE} = 0.88 V. Measurements of both the devices are carried out from 1 GHz to 67 GHz using Agilent network analyzer (E8361A) and Agilent DC source (E5270B). The generality of this work is also verified by employing measured data from 28 nm FDSOI technology Planes *et al.* (2012). The measured MOS transistor contains 40 fingers of 0.5 µm width and nominal gate length of 30 nm. The technological summary is given in (Table 3.2). Figs. 3.6 and 3.7 depict the interpolation results for the real and imaginary of measured admittance parameters of all three technologies using equations (3.15) and (3.16).

Table 3.2: Transistors from different fabrication process: BiCMOS and FDSOI and comparison of the measured and interpolated f_{MAX} value.

Technology	Node (nm) $W_E \times W_L$ (µm) emitter fingers	Peak f_T bias condition	f_{MAX} @30 GHz (measured)	f_{MAX} @30 GHz (interpolation)
BiCMOS	130 0.105×1 8	V_{BC}= 0.25 V, V_{BE}= 0.89 V	721	664
	55 0.09×4.8 1	V_{BC}= 0.5 V, V_{BE}= 0.88 V	353	373
FDSOI	28 0.5×0.03 40	V_{DS}= 1 V, V_{GS}= 0.6 V	328	348

Convincing agreement was obtained over the entire frequency range. Fig. 3.8 shows the f_{MAX} value resulting from the interpolated y-parameters for the three technologies. It can be observed that the use of the analytical formulae discussed above leads to an unambiguous determination of f_{MAX} and thus to a clear technology assessment. The results are summarized in (Table 3.2), right column and compared to the obtained values applying eq. 3.1 directly on the measured data. A significant difference can be observed.

When taking a closer look to the frequency-dependent f_{MAX} behavior for the different technologies in Fig. 3.8, apparently the measured f_{MAX} for the 130 nm BiCMOS technology comes noisy compared to 55 nm BiCMOS technology in the given frequency regime. However, this is initially due to scaling of the y-axis. For all three technologies presented in Fig. 3.8, we observe a variation around the interpolated value of about 10%; see also (Table 3.2), the two right columns. Hence, to get the real f_{MAX} value from a high f_{MAX} transistor (like 130 nm BiCMOS) measurement beyond 100 GHz must be carried out, but note that in the industrial environment where the actual SiGe HBT development has been done, not such high-frequency measurement equipment is available. A detailed discussion about limitations and possible errors is given in the next section.



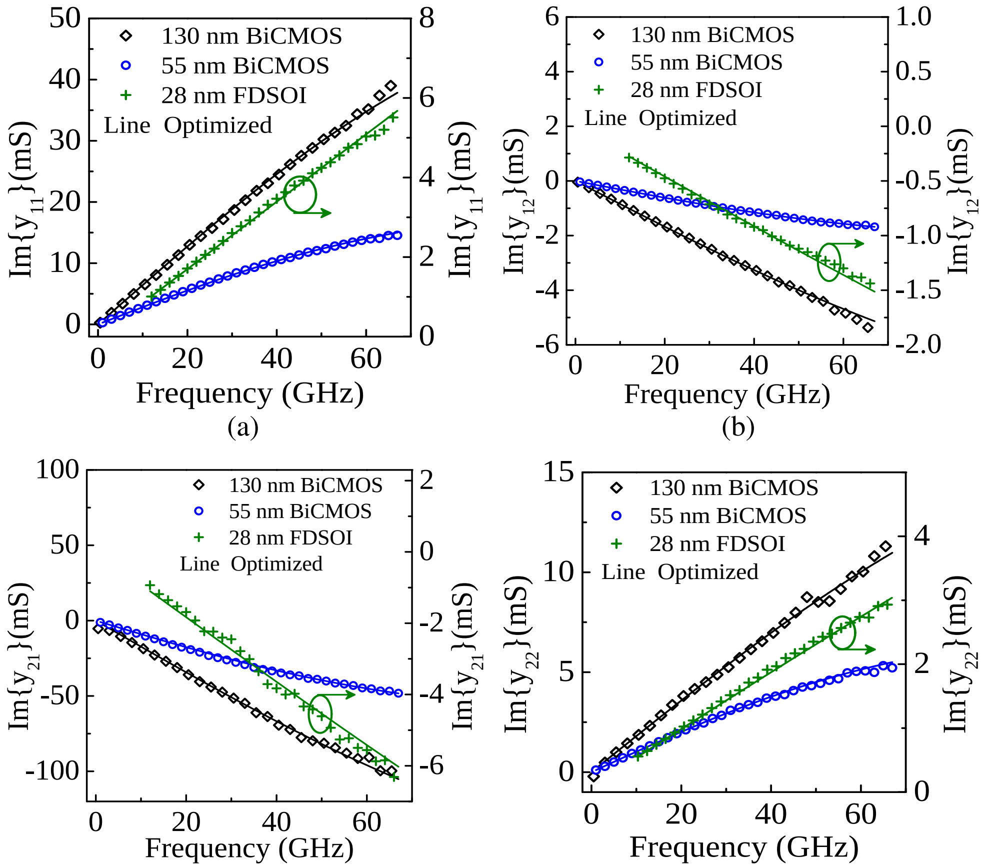
(a)

(b)

(c)

(d)

Fig. 3.6: Frequency-dependent real of admittance parameters for 130 nm BiCMOS SiGe HBT (0.105 μm $\times$ 1 μm) biased at V_{BE} = 0.89 V and V_{CB} = 0.25 V and 55 nm BiCMOS SiGe HBT (0.09 μm $\times$ 4.8 μm) biased at V_{BE} = 0.88 V and V_{CB} = 0.5 V and 28 nm FDSOI MOS transistor (on right y-axis) biased at V_{GS} = 0.6 V and V_{DS} = 1 V.



(a) (b)

(c) (d)

Fig. 3.7: Frequency-dependent imaginary of admittance parameters for 130 nm BiCMOS SiGe HBT (0.105 μm × 1 μm) biased at V_{BE} = 0.89 V and V_{CB} = 0.25 V and 55 nm BiCMOS SiGe HBT (0.09 μm × 4.8 μm) biased at V_{BE} = 0.88 V and V_{CB} = 0.5 V and 28 nm FDSOI MOS transistor (on right y-axis) biased at V_{GS} = 0.6 V and V_{DS} = 1 V.

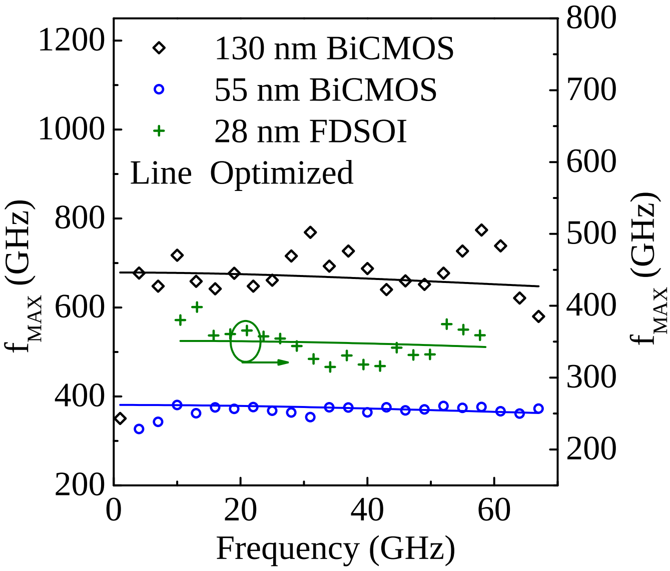


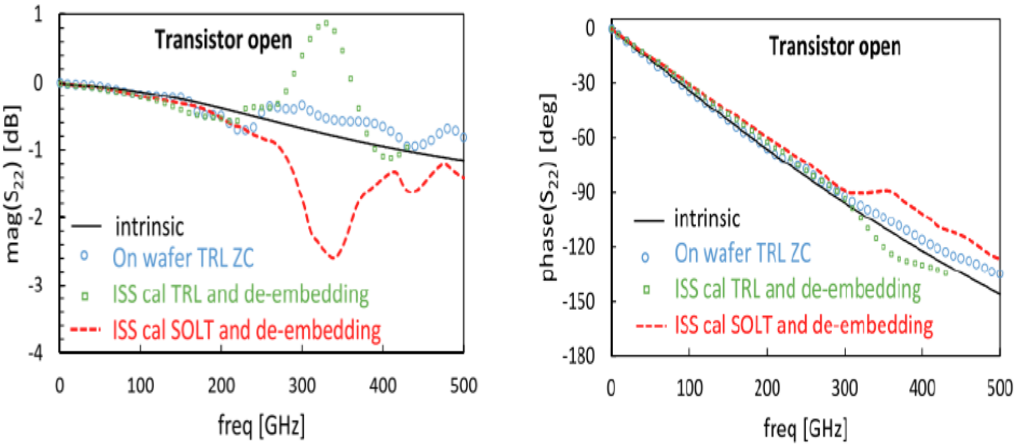
Fig. 3.8: Maximum oscillation frequency as a function of frequency for different flavors of various transistor technologies (symbols) and the least square regraded optimized f_{MAX} (solid line).

3.5 Limitation

The proposed method is valid if the measured s-parameters have only random measurement errors but no systematic measurement errors. Even in the latest measurement equipment, systematic errors can be observed due to coupling of the probes with the wafer surface for a given frequency range Fregonese *et al.* (2020). Accordingly, in the frequency range, in which the elimination of the systematic measurement error is guaranteed, this approach can be used. In order to deepen the understanding of the limitations of the proposed approach, in the next sections we analyze step by step the possible calibration, de-embedding and measurement issues.

3.5.1 Choice of Calibration method

Two types of calibration have been followed in the high-frequency measurement bench. They are SOLT (short-open-load-through) and TRL (through-reflect-line). In terms of measurement accuracy, the TRL method was preferred to the SOLT method for very high-frequency measurement, as the SOLT method is strongly dependent on probe placement and the exact definition of the standards although results shown in Fregonese *et al.* (2019) depict that for Si based devices, on-wafer TRL and SOLT calibration bring similar results up to 150 GHz (see Fig. 3.9). Below 110 GHz, the SOLT calibration is sufficient in term of accuracy and very efficient due to its broadband capability. Hence the SOLT calibration is used in the following work.



(a) (b)

Fig. 3.9: EM simulation prediction of the transistor-open magnitude (a) and phase (b) of S_{22} parameter versus frequency. Included results are for SOLT ISS calibration with pad-open pad-short de-embedding (red dashed line); TRL ISS calibration with pad-open pad-short de-embedding (green square); on-wafer TRL calibration (blue circle) and intrinsic simulation without pad and probe (black line) (from Fregonese *et al.* (2019)).

3.5.2 De-embedding accuracy

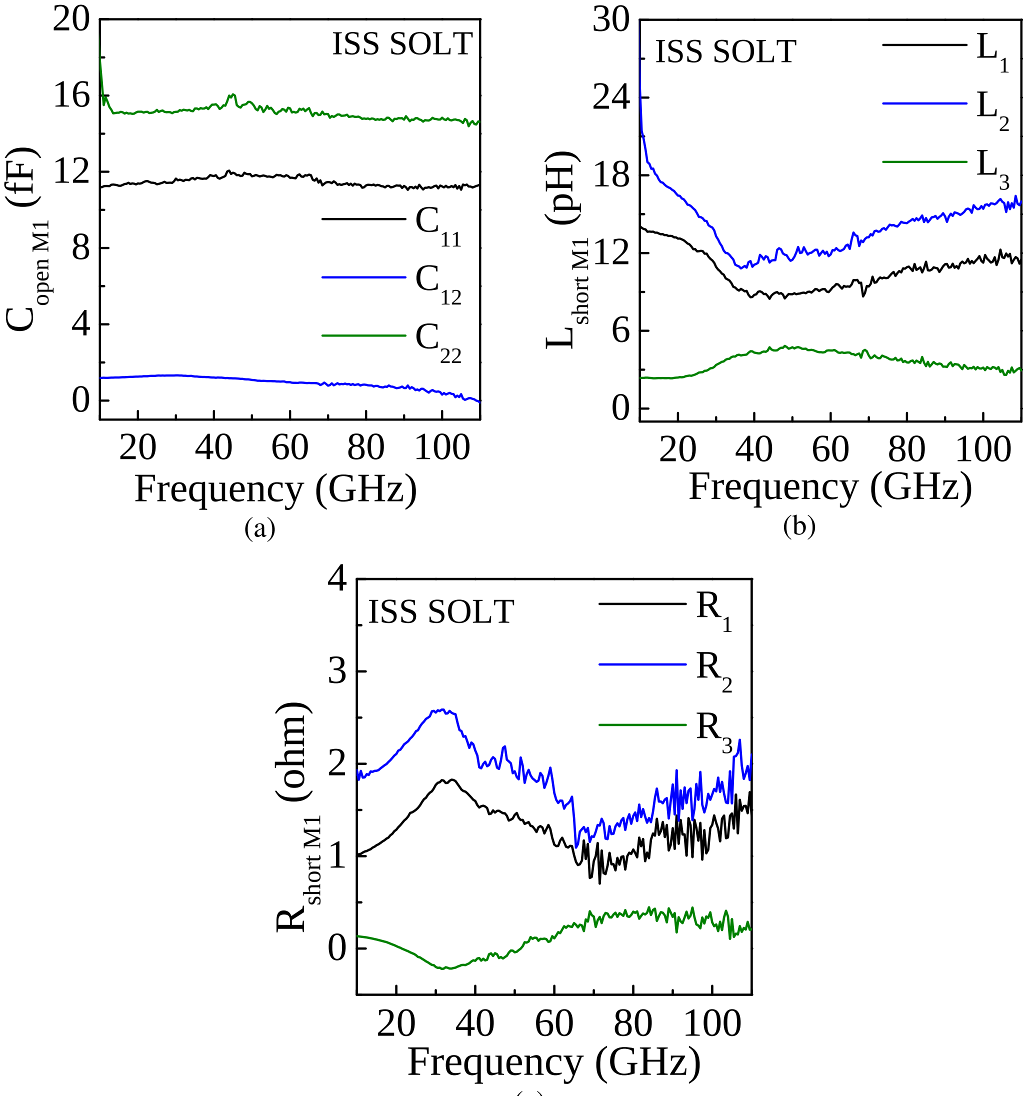
After SOLT calibration, OPEN-SHORT de-embedding has employed to remove the contribution of external capacitances and inductances down to first metal layer (M_1) using specific de-embedding test-structures. We have shown in Fig. 3.10 the frequency-dependent capacitance and inductances/resistances of the OPEN-SHORT de-embedding test-structures respectively. We have estimated the precision in the capacitances determination to higher than 1 fF. A slight increase of the inductance values can be observed starting from 40 GHz. The de-embedding structures are not symmetrical explaining why C_{11} and C_{22}, L_1 and L_2, R_1 and R_2 having different values. Equations (3.17) to

(3.19) have been used to calculate the capacitance, inductance and resistance values.

$$C_{11} = \frac{\mathrm{Im}\{y_{11} + y_{12}\}}{2\pi f}; \quad C_{22} = \frac{\mathrm{Im}\{y_{22} + y_{21}\}}{2\pi f}, \tag{3.17}$$

$$L_1 = \frac{\mathrm{Im}\{z_{11} - z_{12}\}}{2\pi f}; \quad L_2 = \frac{\mathrm{Im}\{z_{22} - z_{21}\}}{2\pi f}, \tag{3.18}$$

$$R_1 = \mathrm{Re}\{z_{11} - z_{12}\}; \quad R_2 = \mathrm{Re}\{z_{22} - z_{12}\}. \tag{3.19}$$



(a)

(b)

(c)

Fig. 3.10: Capacitances (a), inductances (b) and resistances (c) of OPEN-SHORT de-embedding structures; measurements from the B55 technology from ST Microelectronics.

Inspecting Fig. 3.10, overall, the variations are small; especially for the capacitances, but also for the resistances: here the variations are in the range of 0.5 Ω. The variations for the inductances seem to be slightly higher, but their values are very small: the pH-range, so they do not play a major role during the de-embedding process. These results give us confidence in the lumped element approach used for de-embedding and confirms the finding that distributed de-embedding only comes into play after 100 GHz Fregonese *et al.* (2019).

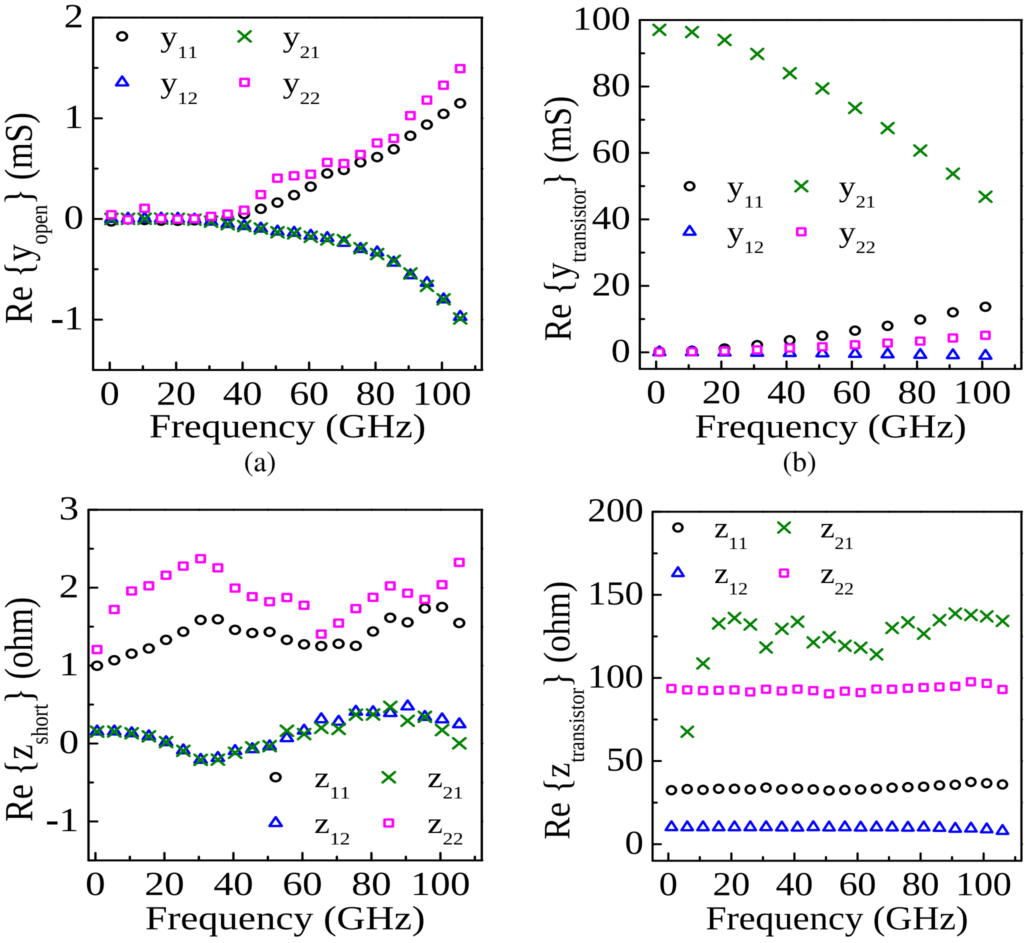
3.5.3 Comparison of de-embedding structures to transistor measurements

It is of interest to perform a comparison of the measured small-signal parameters of the de-embedding structures to the measured small-signal parameters of the transistor. Indeed, if the small-signal parameters of the OPEN or SHORT are much larger than the small-signal parameters of the transistor itself, a small error in the former can introduce a large error in the transistor parameters due to the de-embedding process, thus calling into question the obtained results.

In Fig. 3.11 we show the frequency-dependent conductance values or impedance values of the OPEN-SHORT test-structures, respectively and compare them with the transistor. Again, equations (3.17) to (3.19) have been used to calculate the capacitance, inductance and resistance values.

For the OPEN-structure, the real part of the y-parameters is very small (Fig. 3.11a). The conductance values between Port-1 and Port-2 and Port-1 and -2 to ground are given by the dielectric isolating layer. These values are smaller than those observed in transistor measurements (Fig. 3.11b).

For the SHORT structure, the equivalent electric circuit is a T-like circuit, with R and L in series in each branch, so it is useful to examine the real part of the z-parameters to get the physical meaning. In the Fig. 3.11c and 3.11d we have compared the z-parameters of the SHORT structure and the z-parameters of the transistor. Except $\mathrm{Re}\{z_{12}\}$, all the z-parameters for the transistor are much larger compared to the z-parameters of the SHORT de-embedding structures.

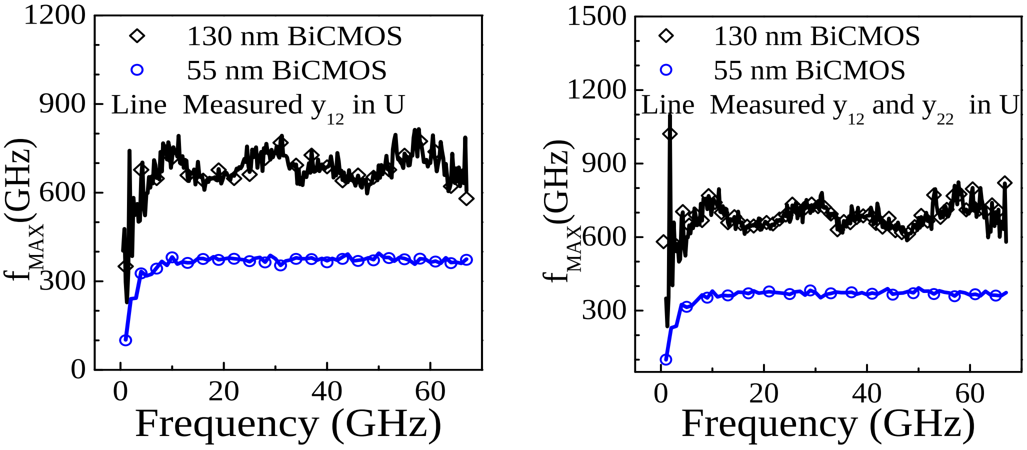


(a) (b) (c) (d)

Fig. 3.11: Real parts of admittance or y-parameters for OPEN de-embedding structure (a) and with transistor (b) and real parts of impedance or z-parameters for SHORT de-embedding structure (c) and with transistor (d).

3.5.4 Interpolated and measured y-parameters in Mason's gain formula: measurement accuracy

Now that we have confidence in the measured data, let us further analyze the proposed interpolation method. In particular, we try to find out which one of the eight y-parameters plays the main role and introduces the most fluctuations in f_{MAX}. To do this, we replace the measured y-parameters one after the other in the interpolated y-parameter data set. Fig. 3.12a shows the frequency dependent f_{MAX} with measured $\mathrm{Re}\{y_{12}\}$ and interpolated form of the other y-parameters inserted into the Mason's gain formula. Similarly, Fig. 3.12b shows the case where measured $\mathrm{Re}\{y_{12}\}$ and $\mathrm{Re}\{y_{22}\}$ with interpolated form of other y-parameters were inserted into in the Mason's gain formula.



(a) (b)

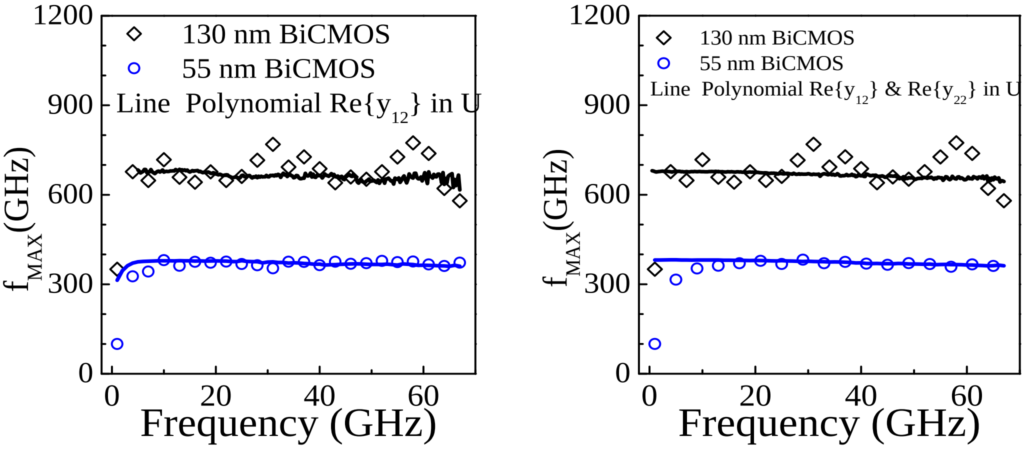
Fig. 3.12: f_{MAX} as a function of frequency showing dominance impact of specific measured y-parameter; only y_{12} (a) and both y_{12} and y_{22} (b) with other interpolated y-parameters in the Mason's gain formula.

We deduce that $\mathrm{Re}\{y_{12}\}$ and $\mathrm{Re}\{y_{22}\}$ play an important role and this allows us to conclude that the noisy behavior of the measured f_{MAX} in the low and high frequency range is due to the $\mathrm{Re}\{y_{12}\}$ and $\mathrm{Re}\{y_{22}\}$, respectively.

Identifying these two y-parameters as the main contributors for the noisy f_{MAX} behavior over frequency, further we have plotted f_{MAX} with interpolated form of $\mathrm{Re}\{y_{12}\}$ and both $\mathrm{Re}\{y_{12}\}$ and $\mathrm{Re}\{y_{22}\}$ in Fig. 3.13a and 3.13b, respectively, with considering other y-parameters as a measured data in the Mason's gain formula. Hence, we can say that it is not at all necessary to interpolate all the y-parameters in the Mason's gain formula.

Only with the interpolated form of $\mathrm{Re}\{y_{12}\}$ in the Mason's gain formula, f_{MAX} comes noisy in the high-frequency regime which can also be attributed by observing the frequency dependent behavior of $\mathrm{Re}\{y_{12}\}$ in Fig. 3.6. This noisy behavior is due to certain measurement issues in this given frequency range e.g., coupling of the probe tip with wafer surface etc.

In order to deepen this analysis, we calculated for the 55 nm and 130 nm BiCMOS technology the mean value (Mean) of f_{MAX}, the maximum (Max), the minimum (Min) and the f_{MAX}-Swing, given by the equation: Swing=(Max-Min)/Mean. We did the same, when applying the interpolation method on (i) all y-parameters, (ii) only on $\mathrm{Re}\{y_{12}\}$



(a) (b)

Fig. 3.13: f_{MAX} as a function of frequency showing dominance impact of specific interpolated y-parameter; only y_{12} (a) and both y_{12} and y_{22} (b) with other measured y-parameters in the Mason's gain formula.

and finally (iii) on the couple $\mathrm{Re}\{y_{12}\}$ & $\mathrm{Re}\{y_{22}\}$. The results are shown in (Tables. 3.3) and (3.4).

Table 3.3: Impact on measured y-parameters on f_{MAX}: data shown for 55 nm BiCMOS technology.

f_{MAX}	In Mason's gain formula			
	Measured	Optimized polynomial (upto 2^{nd} order in frequency)		
	Measured y_{ij}	All y_{ij}	Only $\mathrm{Re}\{y_{12}\}$	Only $\mathrm{Re}\{y_{12}\}$ and $\mathrm{Re}\{y_{22}\}$
Maximum (GHz)	340.9	336.4	333.4	335.5
Mean (GHz)	325.4	326.9	324	326.7
Minimum (GHz)	289.6	316.9	289.4	302.7
Swing [(Max-Min)/Mean]	0.16	0.06	0.13	0.1

We can observe in both cases, that the use of the interpolation method drastically reduces the Swing-value. Furthermore, we see, that applying the interpolation method only to the couple $\mathrm{Re}\{y_{12}\}$ & $\mathrm{Re}\{y_{22}\}$ gives similar results in terms of mean value and Swing-value compared to the full interpolation method, which confirms the hypothesis that the simplified interpolation only based on the couple $\mathrm{Re}\{y_{12}\}$ & $\mathrm{Re}\{y_{22}\}$ may be sufficient.

Table 3.4: Impact on measured y-parameters on f_{MAX}: data shown for 130 nm BiCMOS technology.

f_{MAX}	In Mason's gain formula			
	Measured	Optimized polynomial (upto 2^{nd} order in frequency)		
	Measured y_{ij}	All y_{ij}	Only $\mathrm{Re}\{y_{12}\}$	Only $\mathrm{Re}\{y_{12}\}$ and $\mathrm{Re}\{y_{22}\}$
Maximum (GHz)	824.4	676.5	681.5	677.1
Mean (GHz)	684.2	664.2	660.6	664
Minimum (GHz)	586	648.9	634.9	644.2
Swing [(Max-Min)/Mean]	0.35	0.04	0.07	0.05

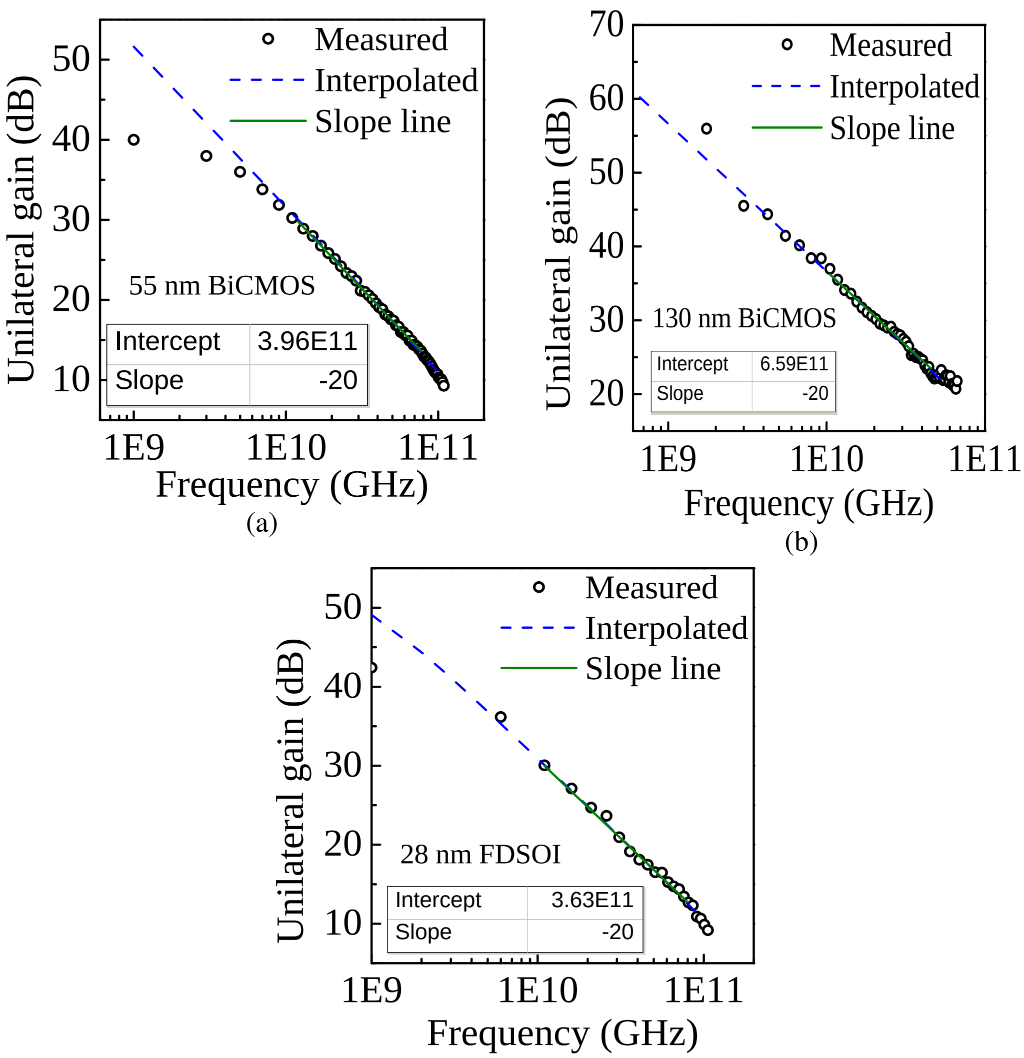
3.6 Comparison and limits of the traditional method for f_{MAX} determination

(a) f_{MAX} from U based presentations

As already discussed in the introduction part, traditionally f_{MAX} is determined by extrapolation to zero from the frequency-dependent characteristics of unilateral gain (U(f)) or maximum available gain (MAG(f)) or maximum stable gain (MSG). First, we applied this approach on the unilateral gain (U(f)). Fig. 3.14 shows the measured U and the U obtained from interpolated y-parameters for the three technologies. Additionally, a straight line with a slope of -20 dB/decade has been superimposed, the extrapolation of which allowed identification of f_{MAX}. The extracted f_{MAX} agrees roughly with the values obtained by our interpolation method. The reader may now ask why the new method was developed when the traditional method gives the acceptable results. This question will be answered in the next section.

(b) Limitation of the traditional f_{MAX} determination method

For 55 nm BiCMOS technology, we have chosen a bias point (far below from the peak f_T) at which measured f_{MAX} is below 67 GHz. Following Fig. 3.15b we have observed that the slope of the line is about -29 dB/decade instead of -20 dB/decade,



(a)

(b)

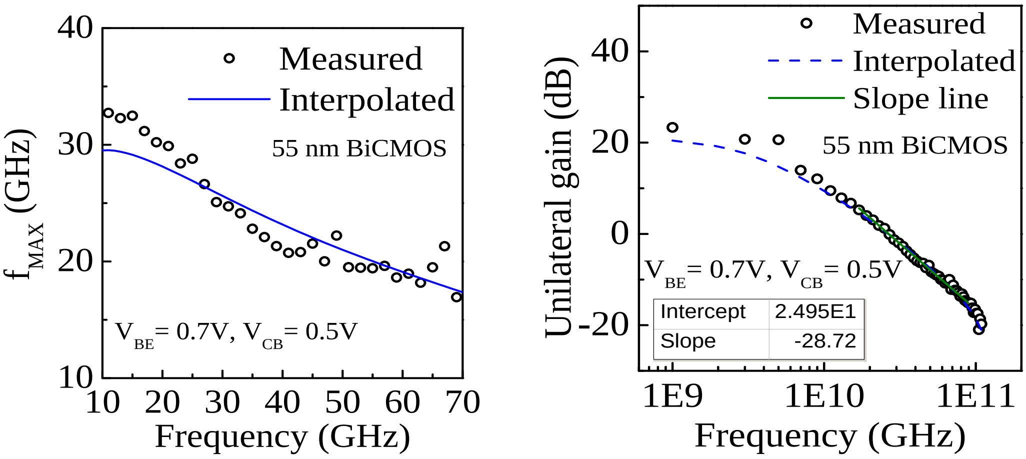
(c)

Fig. 3.14: Justification of predicted f_{MAX} from optimized U(f) with slope of -20 dB/decade for 55 nm BiCMOS (a), 130 nm BiCMOS (b) and 28 nm FD-SOI (c) technology.

hence, theoretically it cannot be f_{MAX}. Thus, the variation shown in the measured f_{MAX} cannot be predicted from the U-based extraction. In contrast to this, the interpolation method is able to show the f_{MAX} variation at this low-bias point, see Fig. 3.15a.

(c) f_{MAX} from maximum stable gain (MSG) and maximum available gain (MAG)

Instead of using the Mason gain (U) for f_{MAX} determination, sometimes the maximum stable gain (MSG) and maximum available gain (MAG) are used. The formula defining these quantities are given below in equations 3.22, 3.23 and 3.24,



(a) (b)

Fig. 3.15: Measured and interpolated f_{MAX} as a function of frequency (a) and extracted from measured $U(f)$ characteristics (b) biased at V_{BE} = 0.7 V and V_{CB} = 0.5 V for 55 nm BiCMOS process.

respectively, as a function of the s-parameters. We plotted these expressions as function of frequency in Fig. 3.16 for the three technologies. On the y-axes, MAG or MSG were chosen dependent on the stability factor K (see also expressions 3.23 and 3.24).

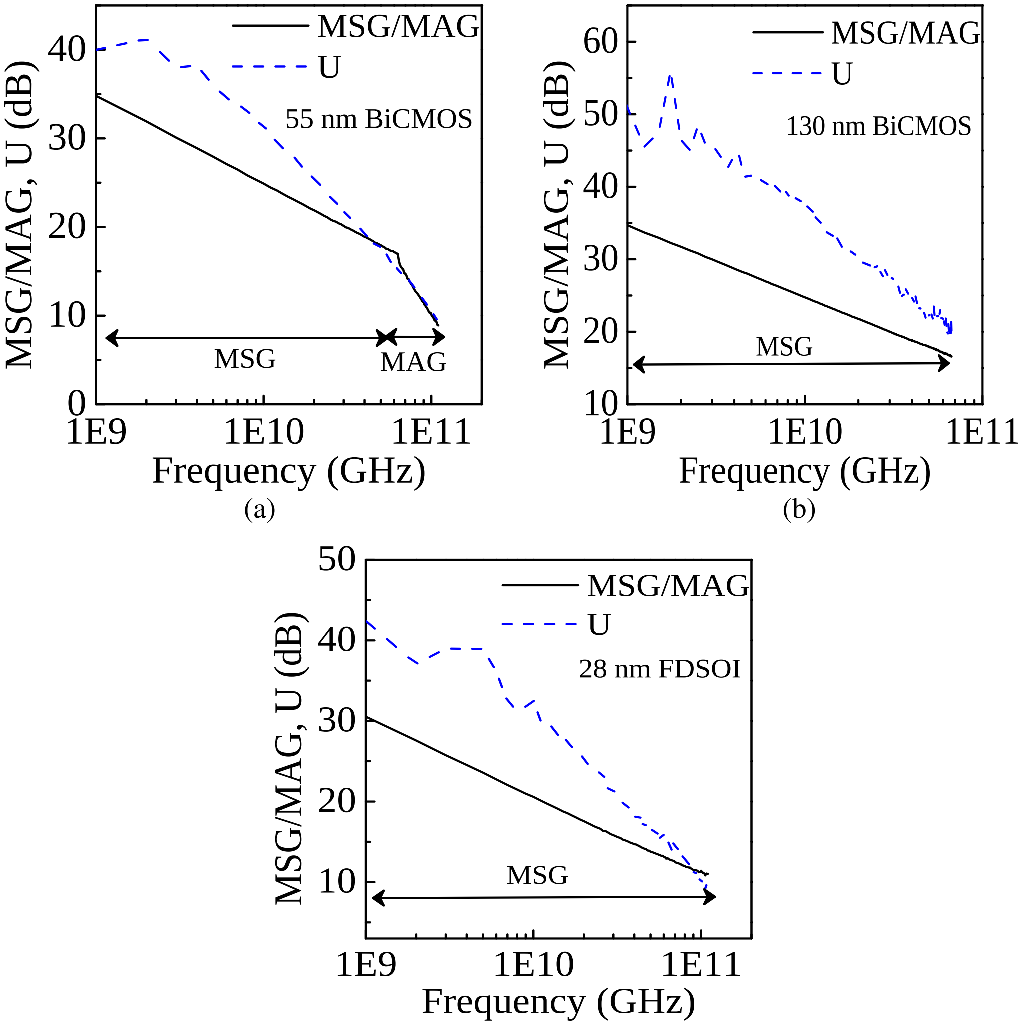
$$Stability factor\ (K) = \frac{1+|s_{11}s_{22}-s_{12}s_{21}|^2-|s_{11}|^2-|s_{22}|^2}{2|s_{12}||s_{21}|}. \tag{3.20}$$

$$\Delta = |s_{11}s_{22}-s_{12}s_{21}|,\quad Unconditional\ stability : K < 1\ and\ \Delta > 1. \tag{3.21}$$

$$Mason's\ Gain\ (U) = \frac{\left|\frac{s_{21}}{s_{12}}-1\right|^2}{2K\left|\frac{s_{21}}{s_{12}}\right|-2\mathrm{Re}(\frac{s_{21}}{s_{12}})}; \qquad K\ independent \tag{3.22}$$

$$Maximum\ Stable\ Gain\ (MSG) = \frac{|s_{21}|}{|s_{12}|}; \qquad K < 1 \tag{3.23}$$

$$Maximum\ Available\ Gain\ (MAG) = \frac{|s_{21}|}{|s_{12}|}(K - \sqrt{K^2 - 1}); \qquad K > 1 \quad (3.24)$$



(a) (b) (c)

Fig. 3.16: MSG/MAG(f) and U(f) for three technologies: 55 nm BiCMOS (a), 130 nm BiCMOS (b) and 28 nm FDSOI (c).

We observe a superposition of MAG(f) and U(f) only for 55 nm BiCMOS technology after 70 GHz, in Fig. 3.16a. For 130 nm BiCMOS and 28 nm FDSOI technology, it was not possible to calculate MAG(f) since in the measured frequency range stability factor (K) is less than 1, see Fig. 3.16b and 3.16c. Hence, we can say that f_{MAX} extraction from U(f) characteristics is more robust than MAG(f) characteristics.

Instead of the extrapolation method presented above, we can also use the formula square-root (gain) multiplied by frequency, as given in equation 3.2. The corresponding result is shown in Fig. 3.17. For the choice of the gain term, MAG or MSG was chosen depending on the stability factor K, as before.

Like the findings in Rimmelspacher *et al.* (2019), we saw that the product sqrt (gain) times frequency is not constant in the given frequency regime as shown in Fig. 3.17. Moreover, we have observed a decrease of the product sqrt (gain) times frequency after 80 GHz which can be attributed due to the coupling of the probe tips with the wafer surface as investigated in Fregonese *et al.* (2020) and like in Rimmelspacher *et al.* (2019) we also conclude that below 10 GHz f_{MAX} determination is not useful.

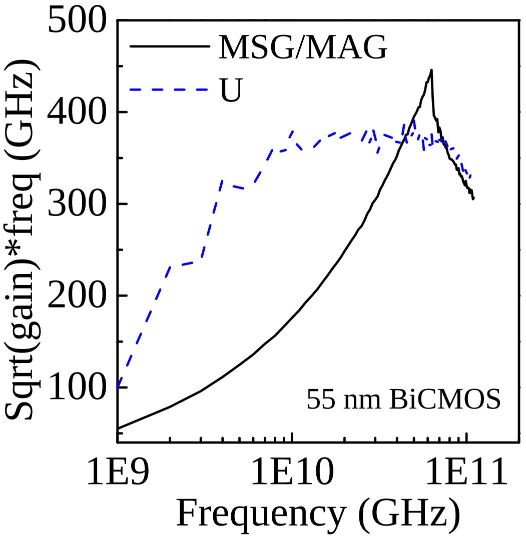


Fig. 3.17: $\sqrt{MSG/MAG(f)} \times frequency$ and $\sqrt{U(f)} \times frequency$ for 55 nm BiCMOS technology.

3.7 Case study: Impact of Back-end-of-line (BEOL) on measured f_{MAX}

In order to highlight the need for reliable f_{MAX} determination method, we consider some specific HBT structures (with thermally aware BEOL design) realized in a state-of-the-art SiGe BiCMOS HBT technology from Infineon (B11HFC) having an f_T = 250 GHz, f_{MAX} = 370 GHz and 6 levels of metallization Böck *et al.* (2015). The investigated test-structures consist of a transistor cell having specially designed metal stacks in the BEOL, which act as heat spreaders, as can be observed in Fig. 3.18. The test-structures under study are designed in-house and consist of a single transistor having a CBEBC arrangement for the contacts and are connected in common emitter configuration. Different configurations for BEOL metallization upon the active part of the component have been fabricated. For the first set of test-structures the metal bars are stacked one on top of the other and connected by vias; the additional metal dummies have a gradually increasing width till reaching 1.52 µm for the $M4$ structure as shown in Fig. 3.18b. These structures are named $M2_{wide}$, $M3_{wide}$ and $M4_{wide}$, where the number stands for the level of the last metal stack that is added and M indicates that the metal dummies are placed above the emitter contact. A complete DC and RF electrical characterization is performed on this test-structures (and de-embedded using the same open- and short- structures for all the transistors under study) in order to investigate the performance improvements. This transistor operates at high power and the addition of metal stacks above the heat source significantly improve the electro-thermal behavior. The design of these test-structures and their characterization have been carried out in a former Ph.D. work by R. D'Esposito D'Esposito (2016). The results for the f_{MAX} determination using (3.1) and (3.2) are plotted in Fig. 3.19a. Although we can identify an impact of the contact configuration, a clear assessment is not possible due to the noisy nature of the data. Next, we applied our new method on the measured data. Fig. 3.19b shows the f_{MAX} results obtained from the interpolation for the technology flavors. It is observed that the use of the analytical formulations results in a clear technology assessment concerning the improvement obtained by the addition of BEOL metals highlighting the efficiency of the proposed method.

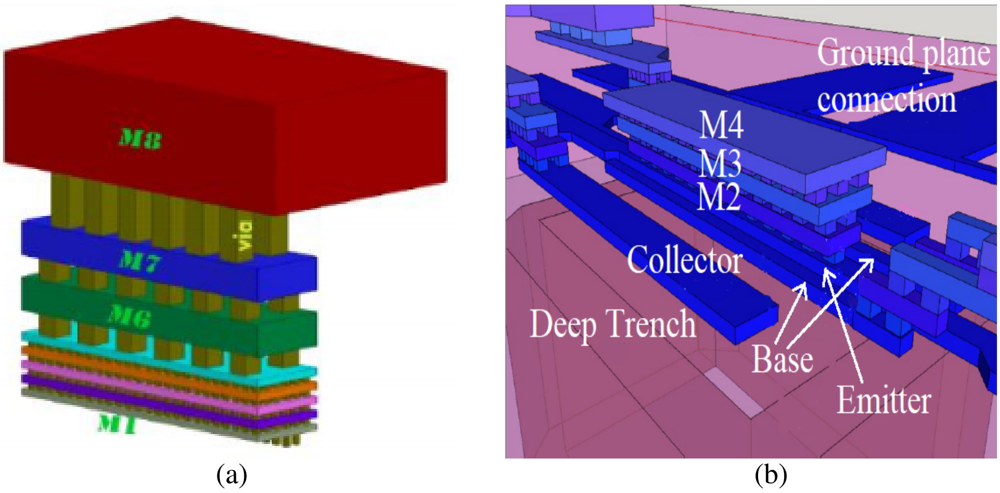


Fig. 3.18: Back-end-of-line (BEOL) contact configuration: cross-sectional view of eight (8) metal layers architecture (a) and 3D representation of the M_{4wide} test structure with drawn emitter window 5 μm × 0.34 μm (b) used in work.

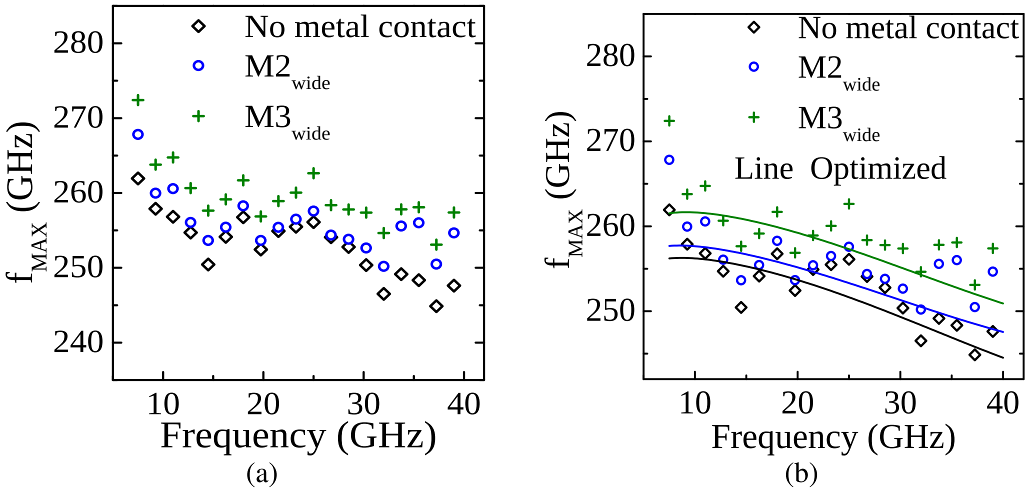


Fig. 3.19: Frequency-dependent f_{MAX} for the different BEOL contact configurations (a) and obtained by interpolated y-parameters represented by solid line (b).

3.8 Conclusion

In this chapter, we have demonstrated a quick and reliable approach to predict f_{MAX} by formulating analytical equations of admittance parameters (y_{11}, y_{12}, y_{21}, y_{22}) based on the small-signal hybrid π-model. The proposed approach addresses the problem of predicting f_{MAX} in the low-frequency regime in spite of noisy measurement data, in particular due to very small magnitude of the $\mathrm{Re}\{y_{12}\}$ and $\mathrm{Re}\{y_{22}\}$. To that aim the least-mean-square based interpolation technique is applied to obtain the most reliable estimation in contrast to the traditional method that is very sensitive to the measurement noise. Our approach also takes care of the f_{MAX} roll-off mainly observed in the high-frequency regime which cannot be obtained following the conventional f_{MAX} extraction from the unilateral gain versus frequency characteristics with a fitting line having a slope of -20 dB/decade. Smooth f_{MAX} has been obtained when the observations were carried on 130 nm and 55 nm BiCMOS as well as on 28 nm FDSOI technologies that leads to the conclusion that the use of rational function in the Mason's gain formula can provide accurate, robust and reliable estimation of f_{MAX}. This is extremely important for a reliable assessment of a technology under evaluation. However, there is still some uncertainty in the f_{MAX} value estimated from the low-frequency measurements. In order to obtain the true f_{MAX} value, measurement beyond 100 GHz (close to the f_{MAX}) needs to be carried out.

CHAPTER 4

SUBSTRATE MODELING FOR SiGe HBTs

4.1 Introduction

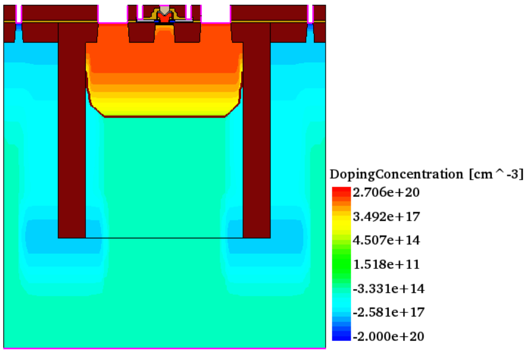
In this chapter, we focus on the adverse effects of the substrate in device's characteristics Pfost *et al.* (1996), Strahle and Pfost (2003) and assess the substrate model incorporated in the state-of-the-art HICUM L2v2.4 Schröter and Pawlak (2017). For high-speed circuit design, substrate and the related substrate parasitic play a significant role in determining the output impedance of the device which directly impacts the gain of the amplifier. For a highly dense structure, the substrate couples with the neighboring elements. The substrate coupling can be broadly categorized by two types Fregonese *et al.* (2015); one is coupling between the device to the substrate and the other is the coupling between surrounding devices. In both types of coupling the current flow lines are non-uniform which makes the coupling even more complex and difficult to model mainly at sufficiently high-frequency regime Pfost and Rein (1998), Fregonese *et al.* (2005). However, when using additional test structures - which results in a higher costs due to additional Silicon surface, a study in Fregonese *et al.* (2015) showed that an accurate substrate modeling and related parameter extraction can be performed.

On the other hand, with the aim of having higher figure-of-merits (FoMs) and minimizing the parasitic contributions, self-aligned integrated base structures have been fabricated which uses the deep trench in their architecture Jagannathan *et al.* (2002), Rieh *et al.* (2002). Moreover, various transistor technologies like BiCMOS 0.25 μm Baudry *et al.* (2003), BiCMOS 0.13 μm Laurens *et al.* (2003), BiCMOS 55 nm Chevalier *et al.* (2014) and BiCMOS 90 nm Chevalier *et al.* (2004) consider the deep trench in spite of having higher self-heating and trench capacitance. Considering the measured data from BiCMOS 55 nm technology transistor as a reference, we investigate the state-of-the-art collector-substrate model incorporated in HICUM L2v2.4 up to 330 GHz using the physics-based formulations reported in Fregonese *et al.* (2005).

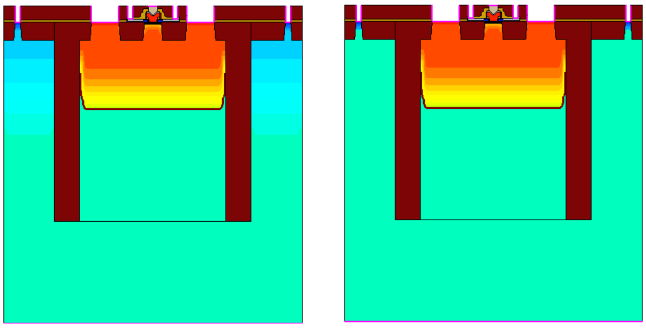
The chapter is organized as follows: in section 4.2, we discuss the frequency-dependent output device parameters by considering TCAD based structures in which the structural parameters concerning the collector-substrate region are varied. In section 4.3, a brief study of the existing collector-substrate model incorporated in the state-of-the-art compact model HICUM L2v2.4 is discussed along with the model limitation drawn in section 4.4. An improved collector-substrate model proposal is presented in section 4.5. The modeling results are compared with the measured data and presented in sections 4.6. Finally, the conclusions are drawn in section 4.7.

4.2 TCAD based simulations considering different structures

Based on measured data, the device structure has been calibrated in sentaurus TCAD Panda *et al.* (2019). The complete TCAD structure with region-specific doping concentration is shown in Fig. 4.1a. This is called here structure-1. To showcase the impact of the collector-substrate region on the frequency-dependent output characteristics, we will use different forms of the TCAD based structures with a focus on the collector-substrate region. To that aim and following structure-1, two different structures have been considered. In Fig. 4.1b we present a structure in which the stop channel below the deep trench and the surrounding doped region across the bottom of the deep trench have been removed on both sides of the emitter. This structure has been called structure-2. Note that the response obtained from structure-2 ignores the impact coming from the stop channel in the frequency-dependent output characteristics. Further in Fig. 4.1c, the doped region around the deep trench and the peripheral region just below the substrate contacts are removed leaving behind only the substrate contact. This structure is labeled as structure-3. Hence the response following the structure-3 only takes into account the impact of substrate contact.



(a) Structure-1.

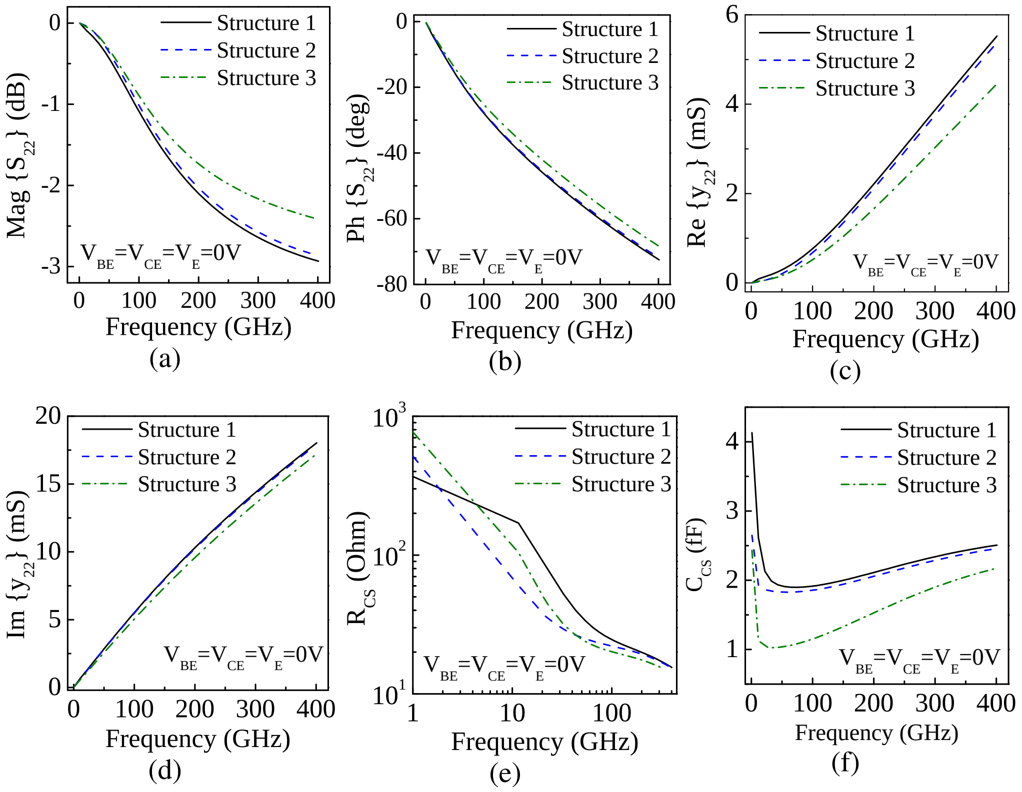


(b) Structure-2.

(c) Structure-3.

Fig. 4.1: Different collector-substrate-based TCAD structures: full calibrated structure (a), structure without stop channel and surround doped region (b), and structure without heavily doped substrate (c).

In Fig. 4.2, we compare the frequency-dependent output related parameters obtained following the TCAD based structures shown in Fig. 4.1. In terms of output reflection scattering parameter (s_{22}), structure-1 is superior compare to structures-2 or 3 (Fig. 4.2a, 4.2b). This is due to consideration of complete substrate-peripheral region in structure-1. In general, reducing the substrate doping results in higher substrate resistance (Figs. 4.2c and 4.2e) and lower collector-substrate capacitance (Figs. 4.2d and 4.2f). Comparing structure-1, structure-2 offers higher substrate resistance and lower junction capacitance which are due to the low doped region and wider collector-substrate space-charge region respectively. Except for the frequency-dependent collector-substrate capacitance characteristics below 10 GHz (see Fig. 4.2f), the difference in the behavior obtained from structure-2 comparing structure-1 is minimal which implies that the stop channel surrounding region has very little significance on the substrate characteristics. Below 10 GHz, a reduction (from 4 fF to 2.5 fF in Fig. 4.2f) is observed in the frequency-dependent collector-substrate capacitance characteristics which can be attributed to the reduced junction capacitance for removal of the peripheral doping in structure-2 compared to structure-1 (see the corner region formed between the deep trench and the buried layer). On the other hand, the response obtained from structure-3 has a significant impact comparing structure-1 (or structure-2) which is due to increased peripheral and substrate resistance along with reduced collector-substrate junction capacitance.



(a) (b) (c)

(d) (e) (f)

Fig. 4.2: Frequency-dependent characteristics: magnitude of s_{22} (a), phase of s_{22} (b), real part of y_{22} (c) imaginary part of y_{22} (d), collector-substrate resistance R_{CS}=Re$(y_{22} + y_{21})^{-1}$ (e), and collector-substrate capacitance C_{CS}=1/(ωIm$(y_{22}+y_{21})^{-1}$) (f) for the different TCAD structures shown in Fig. 4.1.

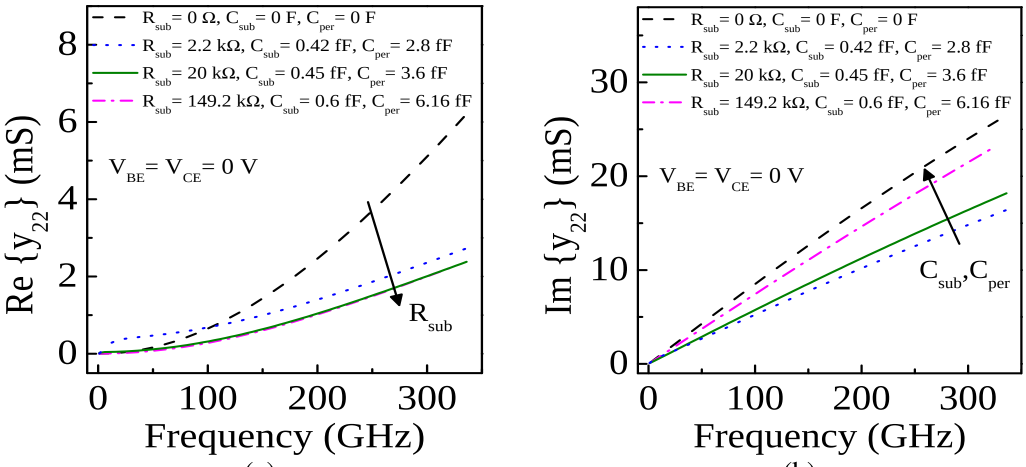
4.3 Collector-substrate model in HICUM and doping dependent substrate coupling

The region from collector-substrate space charge region to substrate contact offers an impedance path due to the permittivity of the substrate as well as the material used in the deep trench for isolation. The coupling in between the substrate contact and the collector-substrate space charge region is often called as *"intra-device"* substrate coupling Schröter and Chakravorty (2010). The design of the coupling network which is used to model the collector-substrate impedance can vary significantly depending on the geometry of substrate and the isolation schemes. In general, the time constant of the substrate (τ_{su}) is calculated following the formula as τ_{su}= $\epsilon_{su} \times \rho_{su}$, where ϵ_{su} is the permittivity of the substrate. Then having known τ_{su}, the cut-off frequency ($\frac{1}{2\pi\tau_{su}}$) of the substrate network can be estimated. However, such estimation becomes difficult for a complex substrate structure in which substrate parameters are partitioned into the perimeter and area components in order to achieve improved model accuracy. Although, in HICUM state-of-the-art compact model, the substrate network has been implemented by considering a parallel combination of RC circuit (R_{sub}-C_{sub}) in series with collector substrate junction capacitance C_{js}.

The bulk substrate (R_{sub}-C_{sub}), collector-substrate junction capacitance (C_{js}) and the peripheral parameter (C_{per}) depend on substrate doping. Hence we have chosen some typical values of substrate doping and corresponding parameters are calculated and shown in the Table. 4.1. Based on these calculated values, Fig. 4.3 shows the impact of substrate coupling on the frequency-dependence output admittance parameter (y_{22}). Substrate conductance decreases with decrease in substrate doping which is shown in Fig. 4.3a. Similarly, increase in substrate resistivity with decrease in substrate doping results increase in substrate capacitance which is depicted in Fig. 4.3b. Also, it is important to note that a trade-off is required between the substrate resistance (R_{sub}), collector-substrate junction capacitance (C_{js}) and peripheral capacitance (C_{per}) since decreasing the doping allows the increase R_{sub}, decrease C_{js} but increase C_{per}. The case with zero substrate parameter value, (R_{sub}= 0 Ω and C_{sub}= 0 F), ideally represence no substrate coupling while the other three cases take into account a finite substrate coupling. Note for the no substrate coupling case, higher conductance is observed (Fig. $4.3a$) since conductance varies inversely to the resistance.

Table 4.1: Substrate parameters as a function of substrate doping.

N_{sub} (cm^{-3})	ρ_{sub} ($\Omega - cm$)	R_{sub} ($k\Omega$)	C_{sub} (fF)	C_{per} (fF)	C_{js} (fF)
1.5×10^{14}	88.6	149.2	0.6	6.16	0.57
1.5×10^{15}	9	20	0.45	3.6	1.73
1.5×10^{16}	0.88	2.2	0.42	2.8	5.31



(a) (b)

Fig. 4.3: Frequency-dependent output admittance showing intra-device substrate coupling: real (a) and imaginary (b) for different set of substrate parameters.

4.4 State-of-the-art model and limitation

The large-signal equivalent circuit of the state-of-the-art HICUM L2v2.4 considering the substrate network is shown in Fig. 4.4. Considering only the collector-substrate part we see, in Fig. 4.5, that the HICUM L2v2.4 considers a PN-junction diode in parallel with a capacitance for modeling the internal collector-substrate region and they are connected in series with a parallel RC network for modeling the substrate region and only a capacitance is used to model the peripheral region. In Fig. 4.5, R_{cx} is the resistance that connects the internal collector to the collector contact, C_{js} is the collector-substrate junction capacitance, R_{sub} and C_{sub} are the substrate resistance and capacitance respectively and C_{per} is the peripheral capacitance. The nodes E_x,B_x, C_x and S_x are the emitter, base, collector and substrate contact respectively while the node C_i and S_i are the internal collector and substrate contact respectively.

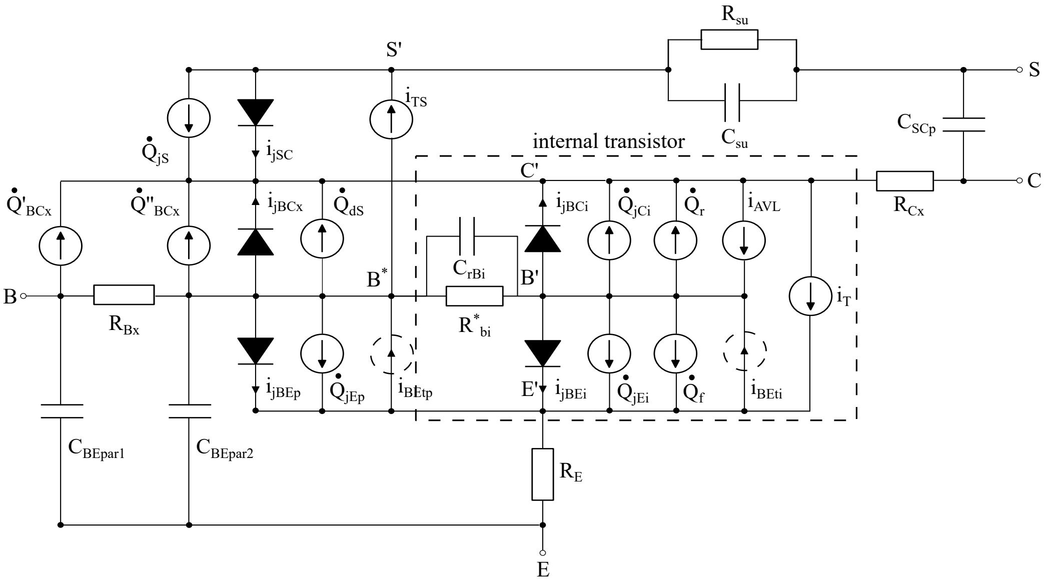


Fig. 4.4: Large-signal equivalent circuit of HICUM L2v2.4 compact model Schröter and Pawlak (2017).

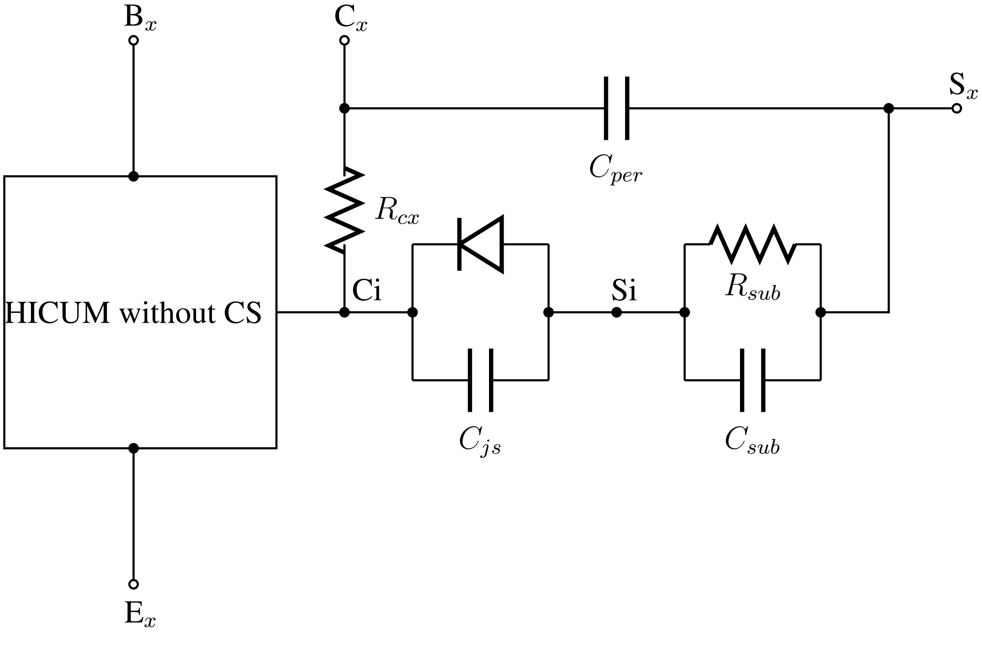
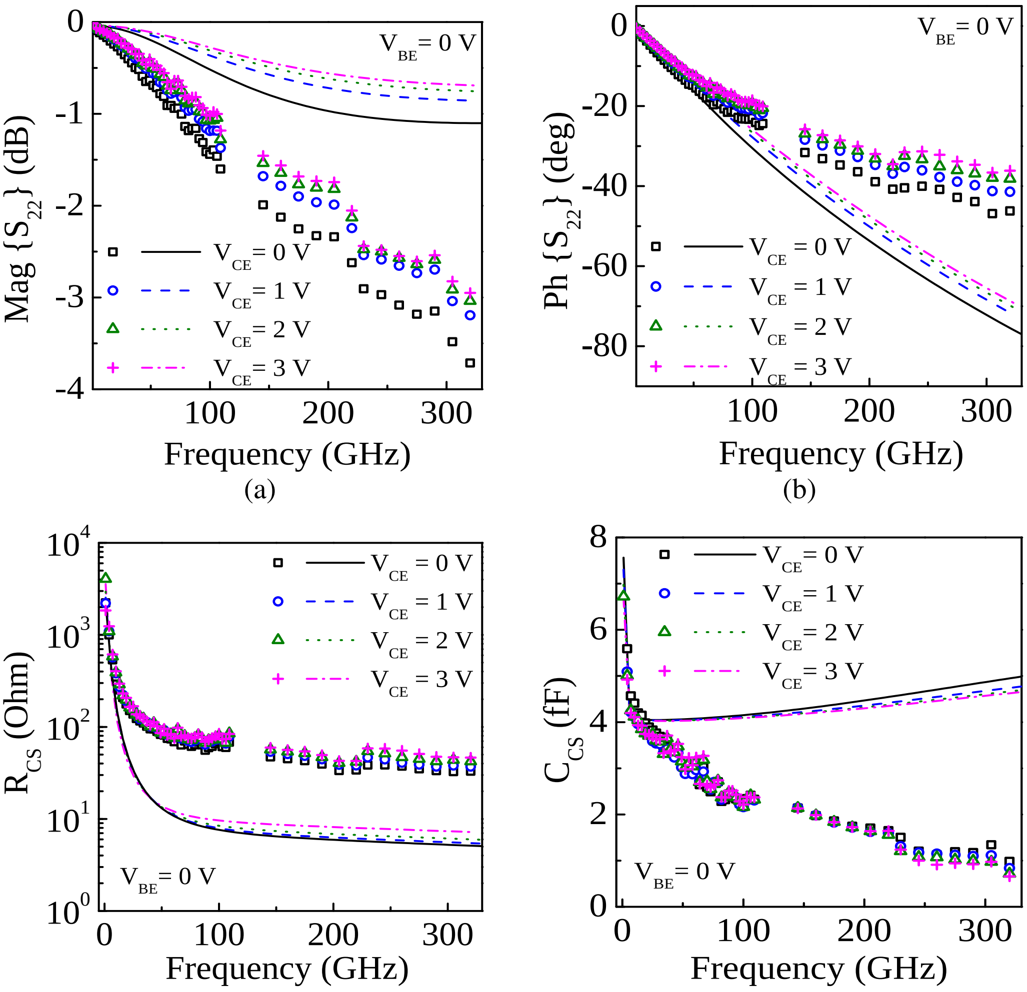


Fig. 4.5: Collector-substrate network of state-of-the-art HICUM L2v2.4.

Now to study the substrate model, first we measured the HBT under the bias condition V_{BE}= 0 V at varying V_{CE} from 0 to 3 volts. Out of four scattering parameters, in Figs. 4.6a and 4.6b, we only show the frequency-dependent scattering parameter s_{22} since s_{22} is mostly influenced by the parameters related to the collector-substrate region. In addition, in Figs. 4.6c and 4.6d, we have shown the collector-substrate resistance (R_{CS}) and capacitance (C_{CS}). The formulation of these resistance and capacitance (see equation 4.4) are represented in the next section following the simple cold transistor model.



(a) (b) (c) (d)

Fig. 4.6: Frequency-dependent magnitude of s_{22} (a), phase of s_{22} (b), collector-substrate resistance R_{CS}=Re$(y_{22}+y_{21})^{-1}$ (c) and collector-substrate capacitance C_{CS}=1/(ωIm$(y_{22}+y_{21})^{-1}$) (d) for $0.09\ \mu m \times 4.8\ \mu m$ SiGe HBT: comparison between measurement (symbols) and HICUM L2v2.4 (lines).

Following the collector-substrate geometry and analytical formulations (discussed in section 4.5.1 and Fregonese *et al.* (2005)) collector-substrate parameters are extracted. The parameters are C_{per}= 3.6 fF, R_{per}= 0 Ω, R_{sub}= 20 kΩ, C_{sub}= 0.5 fF, C_{j0}= 8.5 fF and V_{j0}= 0.84 V. Since this is the state-of-the art HICUM simulation we consider R_{per}= 0 Ω in the model card and the simulation result has been compared with the measured data. In all the four bias points, HICUM is unable to track the measured data and shown in

Fig. 4.6. Although, up to 50 GHz the simulation results of phase of s_{22} are correctly modeled which can be attributed to the fact that C_{per} has been considered in the HICUM equivalent circuit. But we note significant model inaccuracy in the frequency-dependent behavior of R_{CS} and C_{CS} (in Figs. 4.6c and 4.6d respectively) in the whole frequency regime which drives us to focus on to the existing output impedance model of HICUM compact model.

4.5 An advanced collector-substrate model

For the derivation of collector-substrate resistance and capacitance, we consider the cold transistor model shown in Fig. 4.7, where C_{be}, C_{bc} and C_{CS} are the base-emitter, base-collector and collector-substrate capacitance respectively and R_{CS} is the collector-substrate resistance.

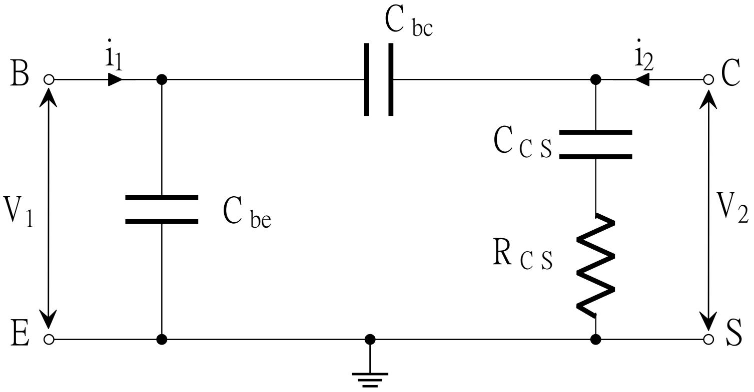


Fig. 4.7: A simple cold transistor model in common-emitter configuration for determination of the substrate parameters.

From the two-port approximation of admittance parameter, the following formulations are formed:

$$y_{22} = \frac{1}{R_{CS} + \frac{1}{j\omega C_{CS}}} + j\omega C_{bc}, \tag{4.1}$$

$$y_{12} = -j\omega C_{bc}. \tag{4.2}$$

Where ω (=2×π×frequency) is the angular frequency. Now using eq. 4.2 into eq. 4.1 and rearranging it reads

$$\frac{1}{y_{12} + y_{22}} = R_{CS} + \frac{1}{j\omega C_{CS}}. \tag{4.3}$$

Real and imaginary part of equation 4.3 yield,

$$R_{CS} = \mathrm{Re}\{y_{12} + y_{22}\}^{-1}; \quad C_{CS} = -\frac{1}{\omega\,\mathrm{Im}\{y_{12} + y_{22}\}^{-1}}, \tag{4.4}$$

Fig.4.8 shows the cross-sectional view of the investigated HBT of the B55 process and this is a CBEBC structure. Considering one symmetrical half, two regions have been identified around the deep trench (see Fig. 4.9a). Considering the deep trench the collector-substrate region can be divided into two parts; that is, the left side of the deep trench contains substrate contact and peripheral region while the right side contains collector contact, collector sinker, and buried layer. The doping profile in the left side of the deep trench varies very differently from $5 \times 10^{17}\ cm^{-3}$ at the substrate contact to the $1 \times 10^{15}\ cm^{-3}$ at the depth of the deep trench. Such non-uniform variation in doping gives birth to non-uniform peripheral resistance R_{per}, the effect of which has not been considered in the HICUM compact model.

Besides with the help of different TCAD based structures, in Fig. 4.2 we have shown the impact of peripheral-substrate region on the frequency-dependent output parameters. Hence, we identified that this may be the possible reason why in Fig. 4.6 HICUM is unable to represent the measured data. Hence, we propose an additional resistance R_{per} in series with the existing capacitance C_{per} with the cost of one extra node. On the half symmetric device cross-section (see Fig. 4.9b), the modified collector-substrate network has been shown. To implement the modified collector-substrate model into HICUM, we have used a SPICE based circuit. The corresponding parameter extraction will be discussed in the next sub-section.

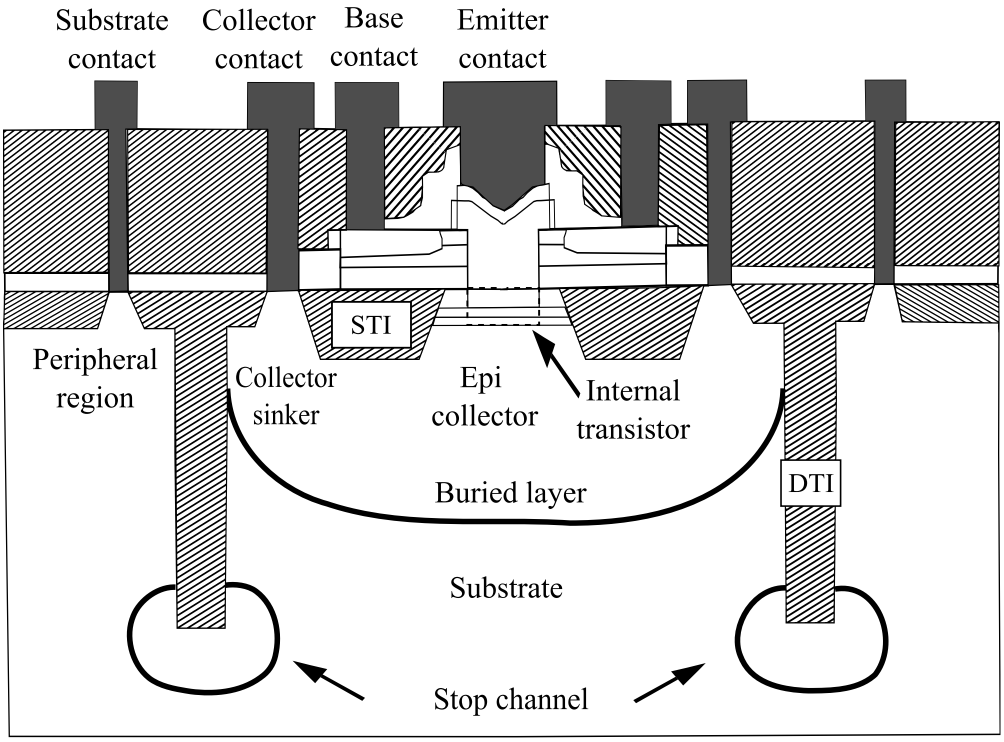
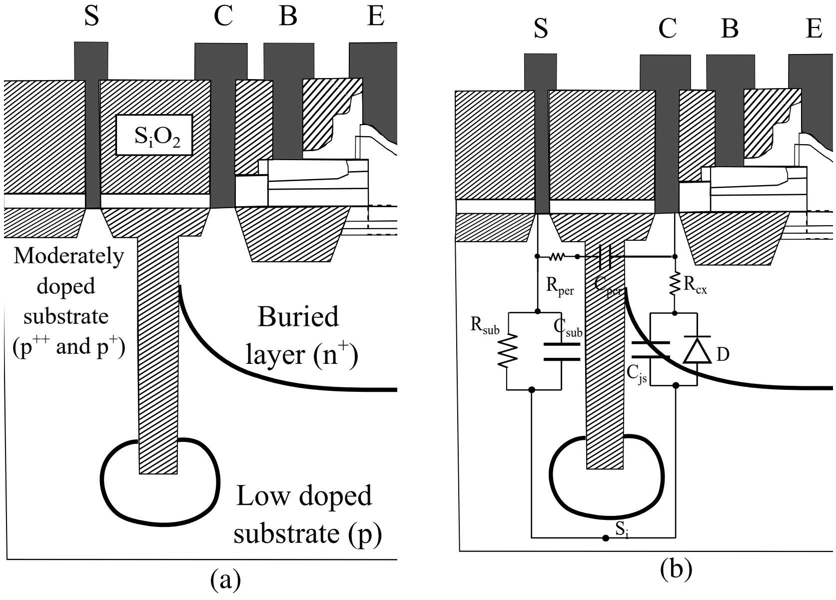


Fig. 4.8: Cross-sectional view of B55 device structure



(a)

(b)

Fig. 4.9: Symmetric half-structure of the investigated HBT : different portions in the collector-substrate region (a) and equivalent SPICE circuit implemented in the collector-substrate region (b).

4.5.1 Substrate network and model formulation

The layout, structural dimension, and doping concentration of the different regions are represented in (Table 4.2). An equivalent lumped collector-substrate model has been represented in Fig. 4.9b where we can see the two regions around DT. Modeling the internal part has been done through a diode in parallel with a capacitor which is further connected in series with a parallel RC network to reach the substrate contact.

Table 4.2: 55 nm BiCMOS technological data.

Structural parameters	**Values**
Layout width (W)	2.78 μm
Layout length (L)	5.12 μm
Width of deep trench	0.42 μm
Depth of deep trench	3.5 μm
Depth access	1 μm
Substrate contact from DT	0.8 μm
Width of substrate contact	0.1 μm
N$_{sub}$	1.5×10^{15} cm^{-3}
N$_{pwell}$	4.5×10^{16} cm^{-3}
N$_{buriedlayer}$	5×10^{19} cm^{-3}

Modeling of the deep trench capacitance (C_{per}) can be done considering a simple parallel plate capacitor, following the well-known equation

$$C = \frac{\varepsilon_o \varepsilon_r A}{e} \tag{4.5}$$

where A is the effective area of the corresponding region and e is the thickness, ϵ_0 is the absolute permittivity and ϵ_r(=3.9) is the relative permittivity of SiO_2. The capacitance in the peripheral region originates due to the presence of the deep trench and it is directly proportional to the perimeter of the deep trench. Following Fig. 4.9a, we see that the total depth of the DT includes the depth of the buried layer, the width of the collector substrate space charged region, and a significant depth in the substrate. Although, calculation of the C_{per} concerns only the depth associated with the buried layer and the collector-substrate space charge region because below the collector-substrate space charge region the voltage difference in both sides of the deep trench (except the part associated with the buried layer and the collector-substrate region) is zero which means charge storage is zero. Considering this fact the peripheral capacitance C_{per} comes to be:

$$C_{per} = \frac{\varepsilon_o \varepsilon_r 2 d_C (W + L)}{e} \tag{4.6}$$

where W and L are the buried layer width and length, and d_C is the buried layer depth plus the depth of the collector-substrate space charge region.

Since the doping below the substrate contact is not uniform, it results in not only in a distributed behavior of R_{per} but also a non-uniform current flows in the substrate. In Fregonese *et al.* (2005) an analytical expression of R_{per} has been presented but the model had not been verified experimentally beyond 110 GHz; hence in this work, we have used this expression to check the model validity up to 330 GHz.

4.5.2 Parameter extraction

Considering the distributed behavior of the substrate-peripheral region which has been discussed in the previous sub-section, we have incorporated a resistance (R_{per}) in series with the existing capacitance C_{per} (see Fig. 4.10) and the model is implemented in HICUM via SPICE based approach. With the basis of technological parameters and layout information, SPICE circuit parameters have been extracted and presented in (Table 4.3). Note the zero-bias collector-substrate diode capacitance (C_{j0}) has been extracted from low-frequency measurement below 10 GHz.

Table 4.3: SPICE model parameters.

Model parameters	**HICUM L2V2.4**	**This work**
C_{per}	3.6 fF	3.6 fF
R_{per}	Not included	540 Ω
R_{sub}	20 kΩ	20 kΩ
C_{sub}	0.5 fF	0.5 fF
C_{jo}	8.5 fF	8.5 fF
V_{jo}	0.84 V	0.84 V

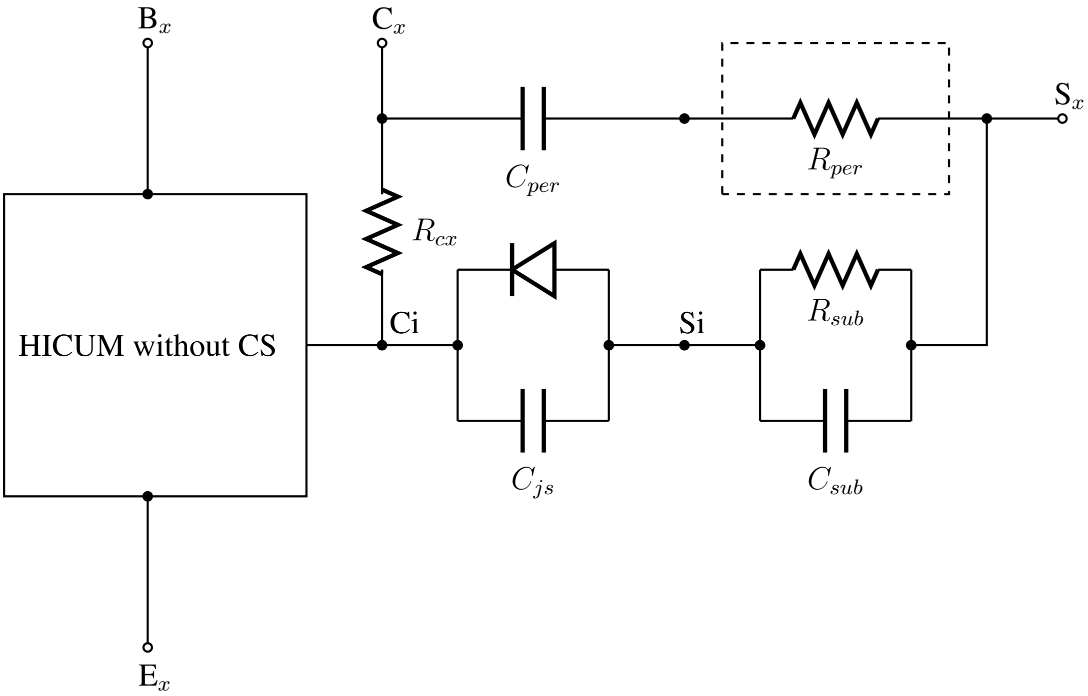
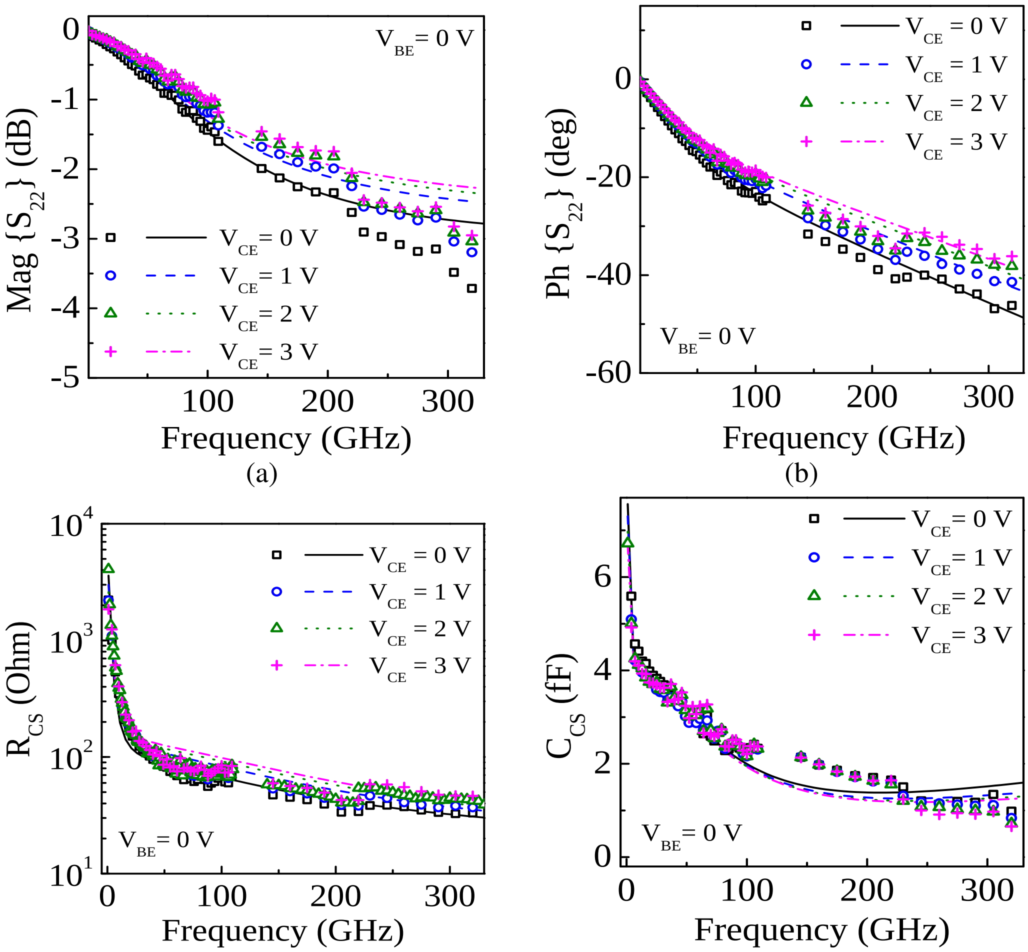


Fig. 4.10: Improved substrate network with the element inside the dashed box has been incorporated in HICUML2.

4.6 Results

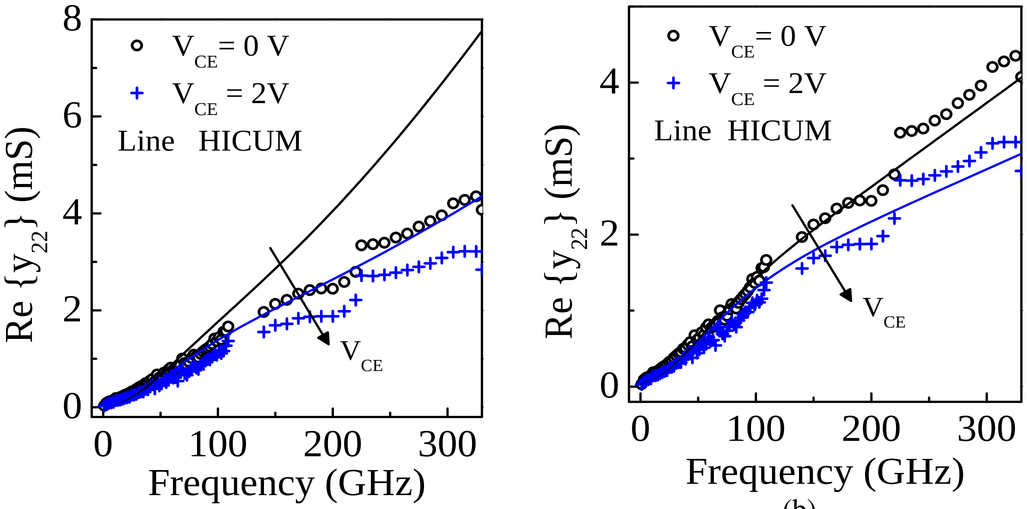
Before comparing the results, an 55 nm BiCMOS SiGe HBT of effective emitter area of $0.09\ \mu m \times 4.8\ \mu m$ has been measured under the cold bias condition of V_{BE} = 0 V and V_{CE} = 0,1,2 and 3 Volts. The HBT has been measured up to 330 GHz and three dedicated measurement benches have been used. These benches are dedicated for 1 to 110 GHz (with extenders from 67 GHz), 140 to 220 GHz, and 220 to 330 GHz frequency range. The major difference in the different benches is the probe geometry and dimension. Before measuring the HBT, the network analyzer has to be well-calibrated and depending on the frequency range of operation calibration type has been set. For operating frequency up to 110 GHz, off-wafer SOLT (Short-Open-Load-Through) calibration has been performed on ISS (Impedance Standard Substrate) and for 140 to 220 GHz and 220 to 330 GHz on-wafer TRL (Through-Reflect-Line) calibration has been preferred. Generally, for the SOLT calibration, the reference plane is set just after the probe tips and for TRL calibration the reference plane is set after the pad. Since the position of the reference plane is calibration type dependent, we do OPEN-SHORT de-embedding after the SOLT calibration for removing the pad capacitance and line inductances and SHORT-OPEN de-embedding after the TRL calibration to remove the effects of access lines and vias Fregonese *et al.* (2019). The magnitude and phase of the proposed s_{22} parameter are shown in Figs. 4.11a and 4.11b respectively. Comparing Fig. 4.6, in Fig. 4.11 a sound agreement can be observed. Note the improved modeling result of the collector-substrate resistance (R_{CS}) is due to the consideration of the peripheral resistance (R_{per}) in the model.



(a) (b) (c) (d)

Fig. 4.11: Frequency-dependent magnitude (a), phase (b) of s_{22}, collector-substrate resistance R_{CS}=Re$(y_{22} + y_{21})^{-1}$ (c) and collector-substrate capacitance C_{CS}=1/(ωIm$(y_{22} + y_{21})^{-1}$) (d) for $0.09\ \mu m \times 4.8\ \mu m$ SiGe HBT: comparison between measurement (symbols) and proposed collector-substrate model that is implemented in L2v2.4 (lines).

To showcase the impact of the substrate network on the frequency-dependent output conductance, we consider the two cases; in the first case we have turned the substrate network off and in the second case we implemented the substrate network into HICUM at two different bias points of $V_{BE} = 0$ volt and $V_{CE} = 0$ and 2 volts. In Fig. 4.12, it is observed that HICUM overestimates the measured data because of consideration of zero value of the substrate parameters while in the second case suitable values of the substrate parameters (R_{sub}= 20 kΩ and C_{sub}= 0.5 fF) leads to a reasonable agreement with the measured data.



(a) (b)

Fig. 4.12: Real of frequency-dependent output conductance (y_{22}): without substrate network R_{sub},C_{sub} (a) and with substrate network (b) in HICUM.

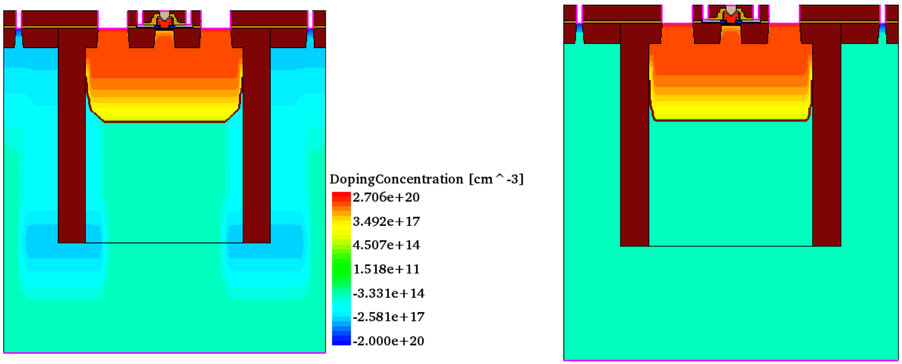
For evaluation of the high-frequency performance of a transistor, we often consider maximum oscillation frequency (f_{MAX}) as a figure of merit. However, accurate estimation of f_{MAX} is very critical in the frequency range of operation because of small magnitudes of admittance parameters Teppati *et al.* (2014), Rimmelspacher *et al.* (2019). Hence the f_{MAX} extraction following Mason's gain formula and extrapolation with -20 dB/decade slope approach become erroneous. Rather, a polynomial-based approach Saha *et al.* (2021) shows a better comparison with the measured data. In the next subsection, we will discuss the impact of collector and substrate parameters on the f_{MAX}.

4.6.1 Variation of collector-substrate parameters on f_{MAX}: observation from TCAD based structures

Based on TCAD based device structure, the impact of the collector-substrate region on f_{MAX} has been observed in this section. The structure shown in Fig. 4.13a is the complete device structure calibrated with high-frequency de-embedded measured data. This is labeled here as structure-1. The blue doped region (at the far most left and right side) shown in structure-1 incorporates substrate contact, peripheral region, and stop channel. Since the impact of the collector-substrate region on f_{MAX} is significant in the high-frequency regime, hence in this part we have varied some of the device parameters (such as doping and material) and to see their impact on f_{MAX}. In the first case, the moderately doped region just below the substrate contact has been removed, leaving behind only the substrate region (see Fig. 4.13b) and the corresponding structure is called structure-2. Comparing structure-1, f_{MAX} obtained from structure-2 is improved significantly and shown in Fig. 4.13e. This is due to the low junction capacitance obtained from the collector-substrate region close to the deep trench. Moreover, we have observed that the peripheral region shows a more dominant impact compared to the region close to the stop channel (the region where the deep trench ends).

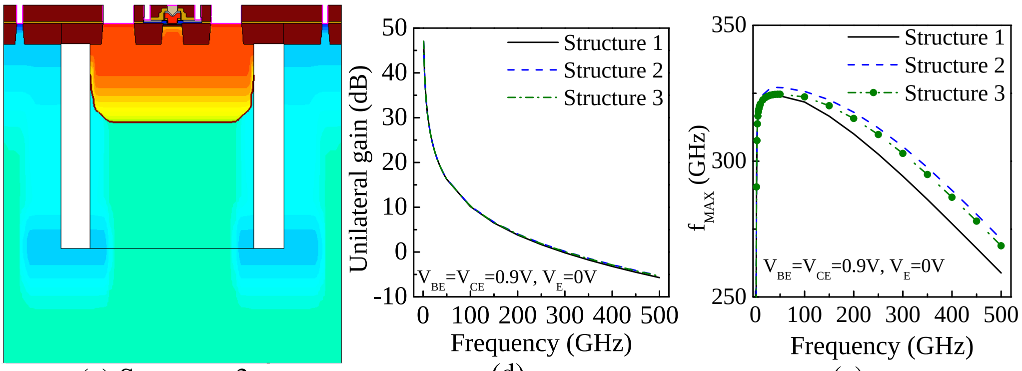
Further to study the impact of the material used in the deep trench on f_{MAX}, we have considered a structure is shown in Fig. 4.13c, labeled as structure-3, wherein the deep trench we have used air (ϵ=1) as a material instead of $Si0_2$ (ϵ=3.9). Once this is done, the trench capacitance has been reduced due to the reduction of the permittivity of the material, and the corresponding f_{MAX} is shown in Fig. 4.13e. Comparing structure-1, f_{MAX} is improved by 5% and 3.9% (seen at 500 GHz) following structure-2 and structure-3 respectively. However, note that the up to 50 GHz no such change in f_{MAX} has been observed which suggests doing the simulation beyond 100 GHz.

Based on this study, it is clear that the collector-substrate peripheral region and the deep trench play a role in the device characteristics. Concerning the collector-substrate region, it appears that the f_{MAX} can be improved by optimizing the doping in the stop channel and using a low-permittivity material in the deep trench. Hence, a good negotiation is required for choosing a proper material and doping the collector-substrate region.



(a) Structure-1.

(b) Structure-2.



(c) Structure-3.

(d)

(e)

Fig. 4.13: Dependence of substrate doping and deep trench material on f_{MAX} following different TCAD structures: full calibrated structure (a), structure without heavy doped substrate (b), deep trench with air (c), frequency dependent unilateral gain (d) and f_{MAX} (e).

Of course, the parameters improving f_{MAX} are the peripheral resistance, the peripheral collector-substrate junction capacitance, and the collector-substrate impedance.

4.6.2 Variation of collector-substrate parameters on f_{MAX}: observation from HICUM

R_{sub} and C_{sub} are the main parameters of the substrate region, and both the parameters depend on substrate doping. In this section, we have varied substrate doping and using the formulations from Fregonese *et al.* (2005), substrate parameters are calculated and shown in (Table 4.4). Note in each of the three cases, R_{sub}-C_{sub} network posses different cut-off frequencies, and f_{MAX} of the device has been changed significantly, observed at the peak f_T bias condition. From Fig. 4.14 we see that for high to moderately doped substrate f_{MAX} is improved which is due to higher resistivity and lower chance of substrate coupling but for extremely low-doped substrate, a higher value of C_{sub} leads to possible non-idealities in the behavior. In each of these three cases, we see a drop of f_{MAX} (approx. 9.4% in Fig. 4.14) which is due to low to high substrate coupling (note that C_{sub} varies with substrate doping from 0.6 fF to 0.42 fF).

Table 4.4: Varying RC time constants of R_{sub}-C_{sub} network.

N_{sub} (cm^{-3})	C_{js} (fF)	C_{per} (fF)	R_{sub} (kΩ)	C_{sub} (fF)	$R_{sub}\times C_{sub}$ (ps)
1.5×10^{16} cm^{-3}	5.31	2.8	2.2	0.42	0.9
1.5×10^{15} cm^{-3}	1.73	3.6	20	0.5	10
1.5×10^{14} cm^{-3}	0.57	6.16	149.2	0.6	89.52

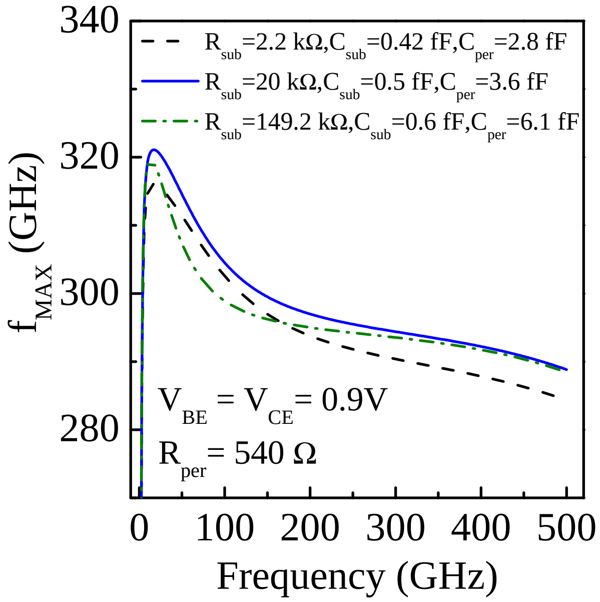


Fig. 4.14: Impact of different time constant of R_{sub}-C_{sub} on f_{MAX} at peak f_T bias condition of V_{BE} = V_{CE} = 0.9V in HICUM.

In the second case, to showcase the individual impact of R_{sub} and C_{sub} parameter on f_{MAX}, we have considered some R_{sub}-C_{sub} combinations but each of such combination leads to identical time constant (see (Table 4.5)). Considering these values, f_{MAX} has been plotted in Fig. 4.15. It is observed that the higher value of C_{sub} leads to significant degradation in the f_{MAX} behavior. Comparing the other two cases (solid line and dashed-dot line in Fig. 4.15), we note that below 100 GHz this reduction is below 2.3% and at and around 500 GHz f_{MAX} reduces approximately by 8.6%.

Table 4.5: Constant RC time constants of R_{sub}-C_{sub} network.

R_{sub} (kΩ)	C_{sub} (fF)	$R_{sub}\times C_{sub}$ (ps)
1	10	10
20	0.5	10
40	0.25	10

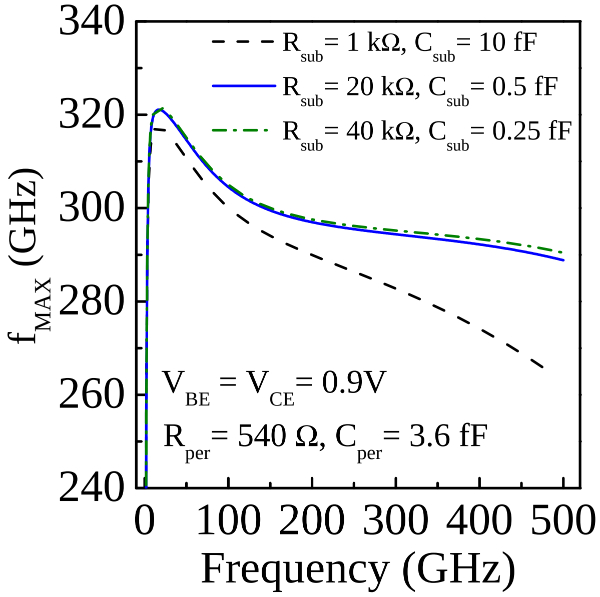


Fig. 4.15: Observation of different R_{sub}-C_{sub} with same time-constant on f_{MAX} at peak f_T bias condition of V_{BE} = V_{CE} = 0.9V in HICUM.

In the third case, we show the impact of the peripheral components (R_{per} and C_{per}) on f_{MAX}. In fact, R_{per} depends on the doping of the p-well, width of the substrate contact, position of the substrate contact from the deep trench, the width of the deep trench, and the depth of the buried layer. On the other hand, C_{per} depends on the material used in the deep trench, deep trench width, and the depth of the buried layer. Considering both the peripheral components, here we check only the impact of deep trench width on f_{MAX}. Hence, considering the given deep trench width (0.42 μm), further we have varied it by $\pm 25\%$ (see (Table 4.6)) and frequency-dependent f_{MAX} plots are shown in Fig. 4.16. Considering the three cases, low f_{MAX} is due to the high C_{per} obtained from the low deep trench structure since C_{per} varies inversely to the width of the deep trench.

Table 4.6: R_{per}-C_{per} as a function of deep trench width.

W_{DT} (μm)	C_{per} (fF)	R_{per}(Ω)
0.315	4.6	553
0.42	3.6	540
0.525	3.1	528

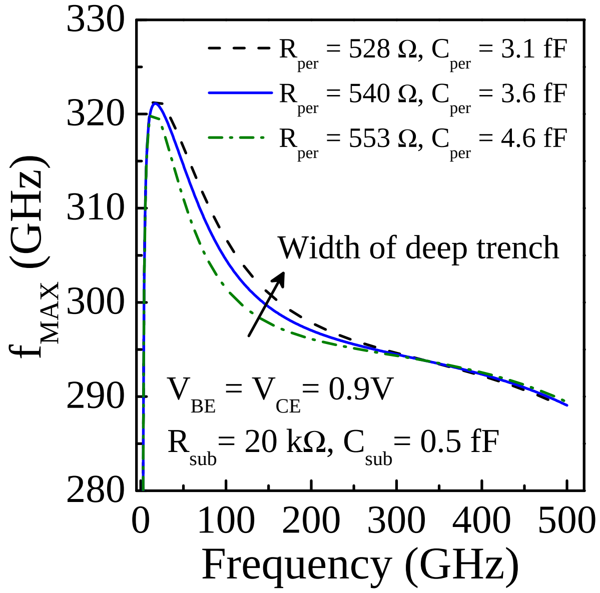


Fig. 4.16: Impact of change in deep trench width on f_{MAX}.

4.6.3 Observation in the forward bias

In this section, we check the overall collector-substrate model in the forward bias. To bring the confidence in the proposed model, first we have considered different models which are shown in Fig. 4.17a and 4.17b. Note in the model 4.17a, the total peripheral part has been masked along with the zero substrate capacitance. This leaves behind only the substrate resistance in series with the internal collector-substrate components. In the second model (in Fig. 4.17b), we add only the collector-substrate capacitance in parallel to the substrate resistance and the third model, (in Fig. 4.17c), is the proposed collector-substrate model which incorporates the peripheral components, i.e., a resistance in series with the capacitance in between the substrate contact and the internal collector node. All these models are incorporated in HICUM and simulation results are compared directly with the measurement at the two operating points V_{BE} = V_{CE} = 0.8 and 0.85V. The simulation result following the model in Fig. 4.17a is obtained consid-

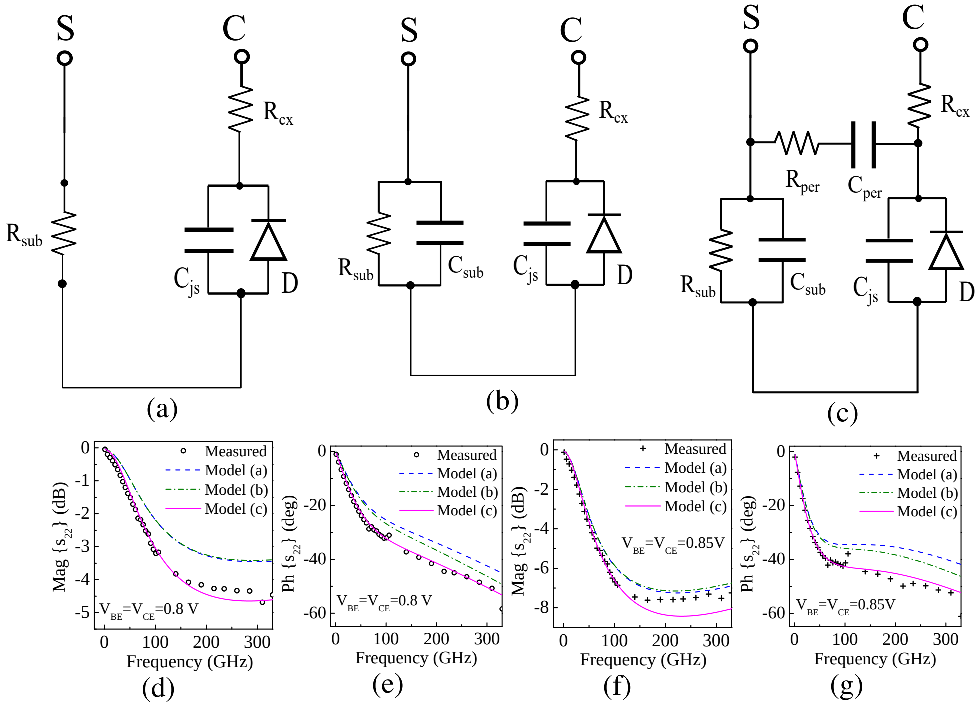


Fig. 4.17: Comparison with measured data in the forward bias following step-by-step incorporation of the collector-substrate model components in the HICUM: only R_{sub} with the internal collector (a), only R_{sub} and C_{sub} with the internal collector (b), complete collector-substrate network (c), magnitude (d) and phase (e) at bias V_{BE}=V_{CE}=0.8V and magnitude (f) and phase (g) at bias V_{BE}=V_{CE}=0.85V of the s_{22} parameter of the investigated HBT.

ering R_{sub} = 20 kΩ with C_{sub} = R_{per} = C_{per} = 0 in the model card. Similarly for the second model, we consider R_{sub} = 20 kΩ, and C_{sub} = 0.5 fF with R_{per} = C_{per} = 0. The first two models (only R_{sub} and R_{sub} with C_{sub} along with the internal collector components) bring a similar kind of response in the frequency-dependent magnitude characteristics and slightly improved response (obtained from the model in Fig. 4.17b) in the frequency-dependent phase characteristics which is due to due to consideration of substrate capacitance with substrate resistance. Unlike first two models, the third model shows a sound agreement in all frequency-dependent magnitude and phase characteristics for both the bias points up to 330 GHz. Comparing the response obtained from the three models, we must say that the peripheral region shows a vital role for modeling the magnitude and phase of s_{22} mainly for the deep trench isolated structures.

4.7 Conclusion

One of the main factors determining the accuracy of the high-frequency circuit design is the output impedance. In general, modeling the output impedance becomes complex if the device structure under consideration contains a deep trench since the peripheral region (the region close to substrate contact and the deep trench) plays a significant role in determining the output impedance. Besides, the FoM of the device can also affected due to inaccurate modeling of the output impedance. We have presented the impact of collector-substrate components on the maximum oscillation frequency (f_{MAX}). Considering the measured data as a reference, first, we have checked the modeling accuracy of the industry-standard compact model HICUM L2v2.4 and it appears that HICUM is unable to track not only the collector substrate resistance and capacitance but also modeling inaccuracy has been observed in the frequency-dependent output scattering parameter (s_{22}). Identifying the peripheral region as a reason for such modeling inaccuracy, in this chapter, we propose an improved model which has been implemented in HICUM with a SPICE based approach. Physics-based circuit model parameters have been calculated directly from the technological data. HICUM with the proposed model shows a reasonable model accuracy up to 330 GHz.

CHAPTER 5

HIGH-FREQUENCY BEHAVIOUR OF SiGe HBTs: HICUM, TCAD AND MEASURED DATA

5.1 Introduction

In the field of radio-frequency (RF) applications, SiGe HBT has been proved as a promising candidate. Hence using such SiGe HBTs for designing very high-frequency circuits requires a physics-based reliable compact model including the significant high-frequency effects in order to ensure first-pass success and thus save the overall fabrication cost and time. Although, an accurate high-frequency model claims a very accurate quasi-static model including the DC and junction capacitances of the internal transistor that determine the fundamental behavior of the transistor. As the operating frequency reaches near the unity current gain transit frequency (f_T), the vertical non-quasi-static (VNQS) effects begin to influence the frequency-dependent small-signal and transient large-signal characteristics due to the delay in the response of the stored minority charge. Such delays are observed at the input (Input NQS effect) as well as at the output (output NQS effect) dynamic (high frequency or fast transient) characteristics. Other than these VNQS effects, the holes in the base of n-p-n SiGe HBT experience a delay while laterally crossing through the internal base region due to a finite voltage drop across them. The DC counterpart of this effect is the so-called emitter current crowding and is known as the AC current crowding or lateral NQS (LNQS) effect in the high-frequency operation. Along with these NQS effects, high-frequency effects can also be dominated by the parasitic base-emitter (BE) and base-collector (BC) capacitances and their accurate partitioning between the internal and external components, which are not precisely investigated so far.

In this chapter, we present the very high-frequency behavior of state-of-the-art silicon germanium heterojunction bipolar transistors (SiGe HBTs) fabricated in 55 nm BiCMOS process technology from STMicroelectronics Chevalier *et al.* (2014) with the help of high-frequency de-embedded measured data, TCAD simulation, and the compact model. In order to make the HICUM customizable for this specific BiCMOS technology as well as to obtain a reasonable agreement, a few selected high-frequency compact model parameters are extracted following the calibrated TCAD based customized structures which are simulated at unique biasing conditions since otherwise such parameters extraction either would be difficult or bound oneself to follow the cost-prone specific test-structures.

The chapter is organized as follows. In section 5.2, we discuss the NQS models which are already incorporated in the state-of-the-art HICUM L2v2.4 along with several model proposals from various research groups to improve the overall model accuracy in the high-frequency regime. In Section 5.3, we describe the high-frequency measurement techniques and TCAD device calibration. Quasi-static analysis and related parameter extraction have been presented in section 5.4. In section 5.5, we show the high-frequency model-related parameter extraction along with the sensitivity analysis of the extracted parameters. In section 5.6, we present the very high-frequency modeling results till 500 GHz after analyzing bias-dependent stored charge and parasitic charge behavior . Finally, the conclusion is drawn in section 5.7.

5.2 State-of-the-art HICUM NQS models and discussion

State-of-the-art HICUM incorporates the input and output NQS effects considering delay times for excess stored charge (using a C-R subcircuit, see Fig. 5.1a) and transfer current (using an LCR subcircuit, see Fig. 5.1b), respectively Schroter *et al.* (2013), Koldehoff *et al.* (1993), Schroter *et al.* (2007). Modeling LNQS effect involves 2-D current flow at the high-frequency regime Pritchard (1958). In HICUM, a parallel RC (C$_{RBi}$ in parallel to R$_{Bi}$) network has been considered to cater to the small-signal LNQS effect. It was also found out that a multi-transistor network can accurately model the

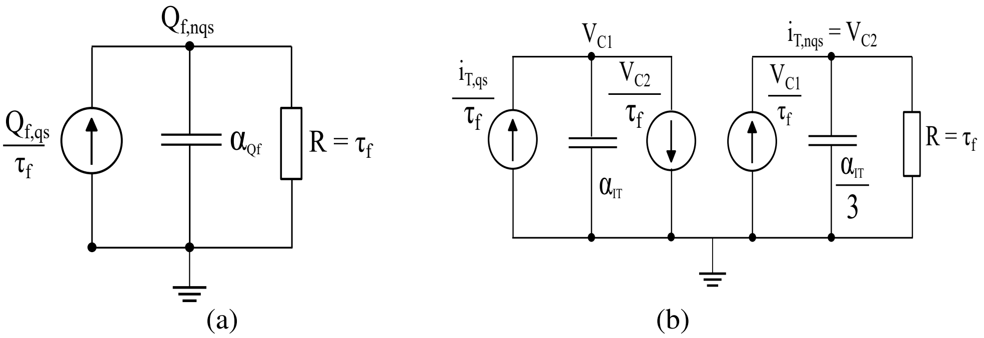


Fig. 5.1: VNQS models incorporated in the state-of-the-art HICUM L2v2.4: input VNQS (a), and output VNQS (b) (source: Schröter and Pawlak (2017)).

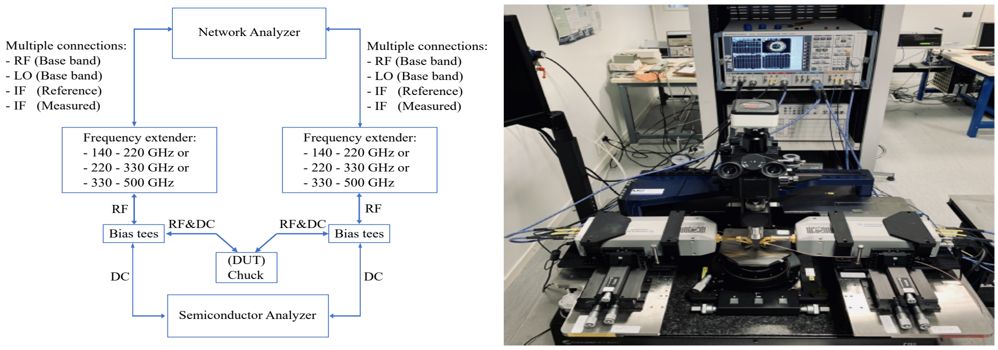
LNQS effect Schröter and Krattenmacher (2019) although not preferred in compact model implementation. Instead, a two-section model Yadav *et al.* (2016) employing charge partitioning across the internal base resistance (R_{Bi}) shows results with comparable accuracy in small as well as large-signal domain.

However, in most of the reported results, the model comparison is done either with only TCAD simulation or the measurement performed at not so high-frequency. Here, we attempt to access the efficacy of the state-of-the-art SiGe HBT model, HICUM, not only with calibrated TCAD simulation but also with high-frequency de-embedded measured data till 500 GHz.

5.3 High-frequency measurement environment and TCAD device calibration

Different measurement benches are used to carry out high-frequency measurements. Like so, four benches are used to cover the whole spectrum of 500 GHz. First, to cover up to 110 GHz, we used a vector network analyzer (E8361A) accompanied with a extender (N5260-60003) above 67 GHz. Next, to cover the higher frequency bands (140-220 GHz, 220-330 GHz, and 325-500 GHz), we used a four-port Rohde & Schwarz ZVA24 vector network analyzer which is coupled with Rohde & Schwarz extenders (ZC220-ZC330-ZC500). Through a block diagram, we show a typical high-frequency (140-500 GHz) measurement set-up in Fig. 5.2a. The extenders are installed on a PM8 Cascade probe station. Fig. 5.2b shows a photograph of the probe station for the 140 GHz to 500 GHz measurements. Either to measure the active and passive elements or to retrieve the some of DUT (device under test) parameters, the power level should be set appropriately at the output of the mmW head in the four bands. In this work, a power level of less than -32 dBm was used.

In such high-frequency measurement, the role of the measuring probes is also important. In fact, the probe's geometry and dimension are frequency bands specific. Typically, a probe with 100 μm pitch (distance between two probe tips) is used for the measurement up to 110 GHz while a probe with 50 μm pitch is used for the rest 140 to 500 GHz measurement. Frequency bands dependent different probes geometries are shown in Fig. 5.3.



(a) (b)

Fig. 5.2: Block diagram of the 140 to 500 GHz measurement set-up (a), and the photograph of the probe station for the 140 to 500 GHz measurements (b) (source: Cabbia (2021)).

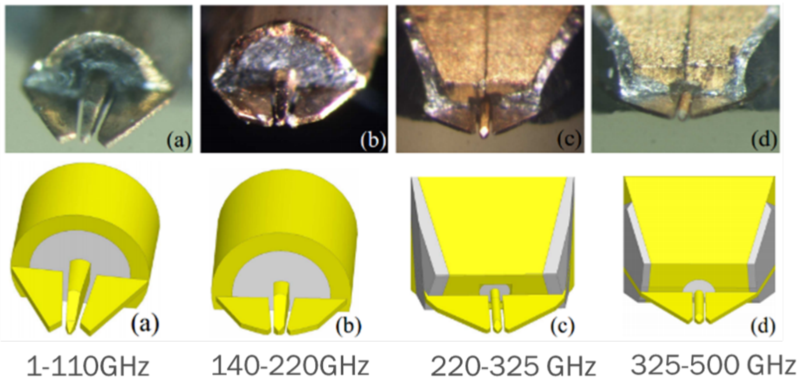
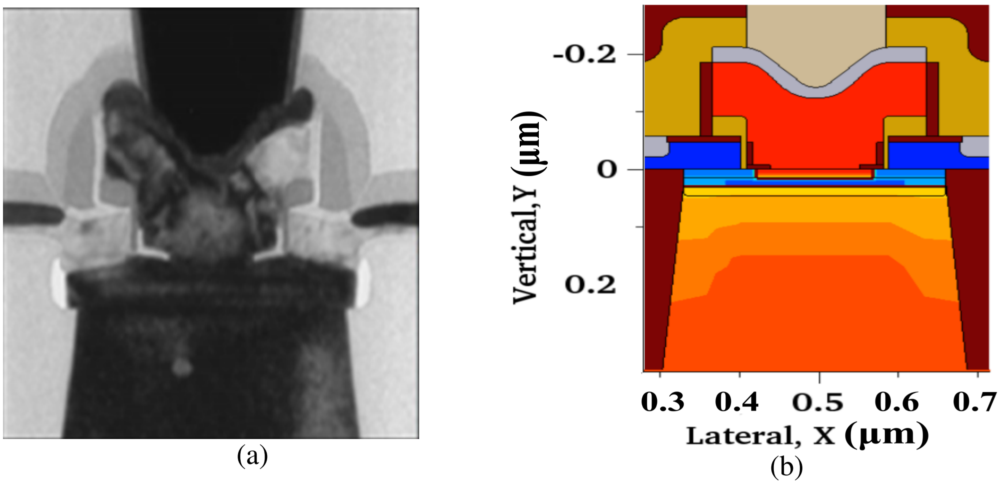


Fig. 5.3: Frequency band specific probes geometry used for high-frequency measurement.

Finally, before measuring the transistor, TRL (Through-Reflect-Line) calibration with an impedance correction based on Williams and Marks (1991) has been performed followed by SHORT-OPEN de-embedding. To minimize the distributed behavior of the de-embedding structures and also to eliminate the contributions from the access lines, the reference plane of the probes is set close to the DUT. The RF measurement setup is utilized for both DC and s-parameters characterization following state-of-the-art calibration and deembedding techniques Fregonese *et al.* (2019), Cabbia *et al.* (2020).

Based on the BiCMOS 55 nm technological data and layout information, parameters are extracted in Saha *et al.* (2019) and these are used for TCAD device calibration. Following the TEM device structure (Fig. 5.4a) showed in VU *et al.* (2016), a suitable meshing and corresponding parameter adjustment has been performed in Panda *et al.* (2019) and resulting TCAD-based B55 device cross-section is shown in Fig. 5.4b.



(a)

(b)

Fig. 5.4: B55 device cross-section in TEM Raya (2008) (a), and sentaurus TCAD (b).

5.4 Quasi-static (QS) model parameter estimation

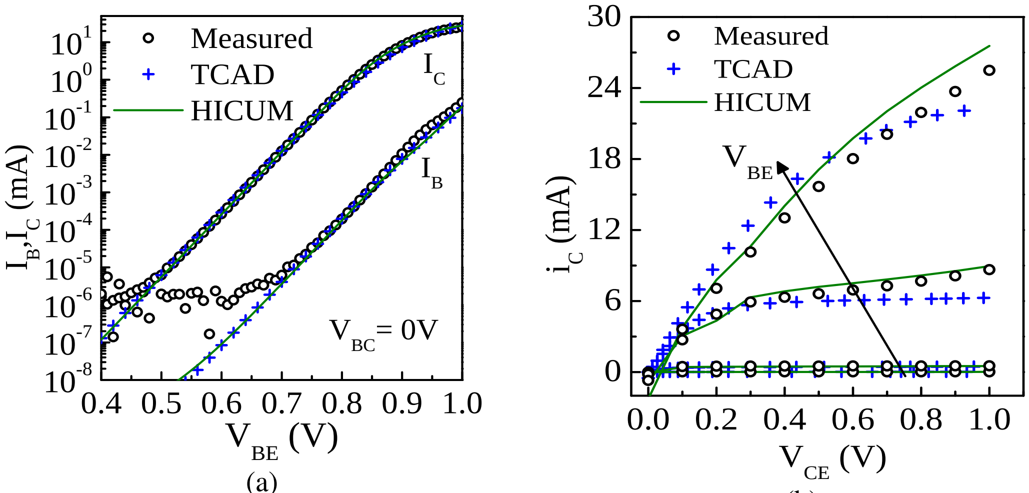
Before investigating the high-frequency behavior of HICUM, we extract the DC and low-frequency compact model parameters including the BE and BC capacitances using the approaches mentioned below.

On the basis of the cold transistor model, y-parameters are formulated in the real and imaginary form Ardouin *et al.* (2001). The total BE and BC capacitances can be calculated from the imaginary of y-parameters taken at the low-frequency regime where the capacitance values are more or less constant with frequency. On the other hand, it can be shown that the intrinsic capacitances are calculated from the real of y-parameters. Once these are done, extrinsic capacitances are obtained by subtracting intrinsic capacitances from the total capacitances. Since this extraction methodology is based on measured data, therefore it is limited for the transistor with small-emitter geometry because obtaining the reliable measured data may be an issue, therefore a scaling approach is used. In the direct method described in Raya *et al.* (2007), first the total BE and BC capacitances have been measured and these capacitances can be considered as a sum of three components. The components are metal contact capacitance, parasitic capacitance, junction capacitance. Moreover, the junction capacitance can be divided into the peripheral junction component and the area junction component. For calculating the metal contact capacitances, different structures (like CBEBC and CBE) with identical emitter geometry and back-end-of-line (BEOL) configurations are used. This extraction is done by simply subtracting the total measured capacitances obtained from the different structures. Note that the other two capacitance components (parasitic and junction) remain the same for the two structures under consideration. Next, to extract the parasitic and the junction capacitances, the scaling approach has been followed. In this approach, first, the corresponding peripheral and area components of the capacitances are separated and grouped. Secondly, the total capacitance is normalized with respect to the effective perimeter of the device. After subtracting the contact capacitance, the BE capacitance becomes Raya *et al.* (2007)

$$\frac{C_{BE} - C_{PE}}{P_0} = CL_{BEPAR} + CLjP_{BE} + CAjA_{BE}\frac{A_0}{P_0} \tag{5.1}$$

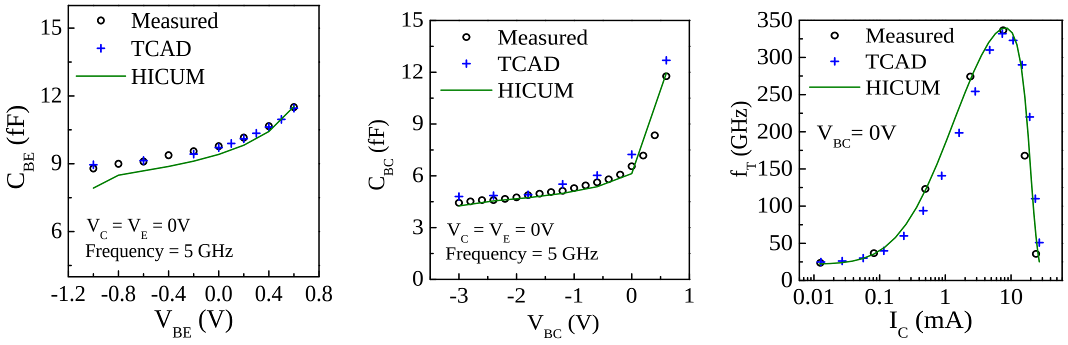
where C_{BE} and C_{PE} are the net BE capacitance and the metal contact capacitance respectively and P_0 (A_0) is the effective emitter perimeter (area). The first two components of 5.1 are linked to the perimeter while the third component is linked to the area of the device. Therefore from the plot, one can have the junction component from the slope and total peripheral component from the intercept at the y-axis for any given geometry measured data. A detailed study regarding capacitance splitting and scaling has been done in Raya (2008).

Following these approaches, parameters are extracted and cold and quasi-static simulation of HICUM model is performed in IC-CAP. In Fig. 5.5, we show the Gummel and output characteristics with measured data and already calibrated TCAD simulation and in 5.6, we present the bias-dependent cold capacitances and the transit frequency characteristics. The cold and quasi-static model agreement appears reasonable and this benchmark model agreement with TCAD will be helpful to further pursue an in-depth investigation and extraction of the specific high-frequency model parameters which will be discussed in the subsequent sections.



(a) (b)

Fig. 5.5: Bias-dependent gummel plots (a), and output characteristics (b) for 0.09 μm × 4.8 μm SiGe HBT: comparison between measured data ("o" symbol), calibrated TCAD simulation ("+" symbol) and HICUM model (solid lines).



(a) (b) (c)

Fig. 5.6: Bias-dependent cold base-emitter capacitance (a), base-collector capacitance (b), and transit frequency characteristics (c) for 0.09 μm × 4.8 μm SiGe HBT: comparison between measured data ("o" symbol), calibrated TCAD simulation ("+" symbol) and HICUM (solid lines).

5.5 High-frequency compact model parameter estimation

Fig.5.7 shows the equivalent circuit of bipolar transistor compact model HICUM with an improved collector-substrate model Saha *et al.* (2019). The dashed box represents the internal transistor while the remaining ones are used to model the external and parasitic effects. Based on the physics-based model equations, model elements are implemented in the equivalent circuit. Although to customize HICUM for a specific technology, one has to extract the HICUM parameters related to each model equation. Parasitic, DC and quasi-static model parameters extraction are well reported in the literature Ardouin *et al.* (2001),Fregonese *et al.* (2006). But, to extract some of the high-frequency model parameters, a specific extraction procedure needs to be followed. With the help of TCAD based structure, we have extracted the vertical (***alit***, ***alqf***) and lateral (***fcrbi***) NQS parameters as well as partitioning factor related to base-emitter (***fbepar***) and base-collector (***fbcpar***) parasitic capacitance.

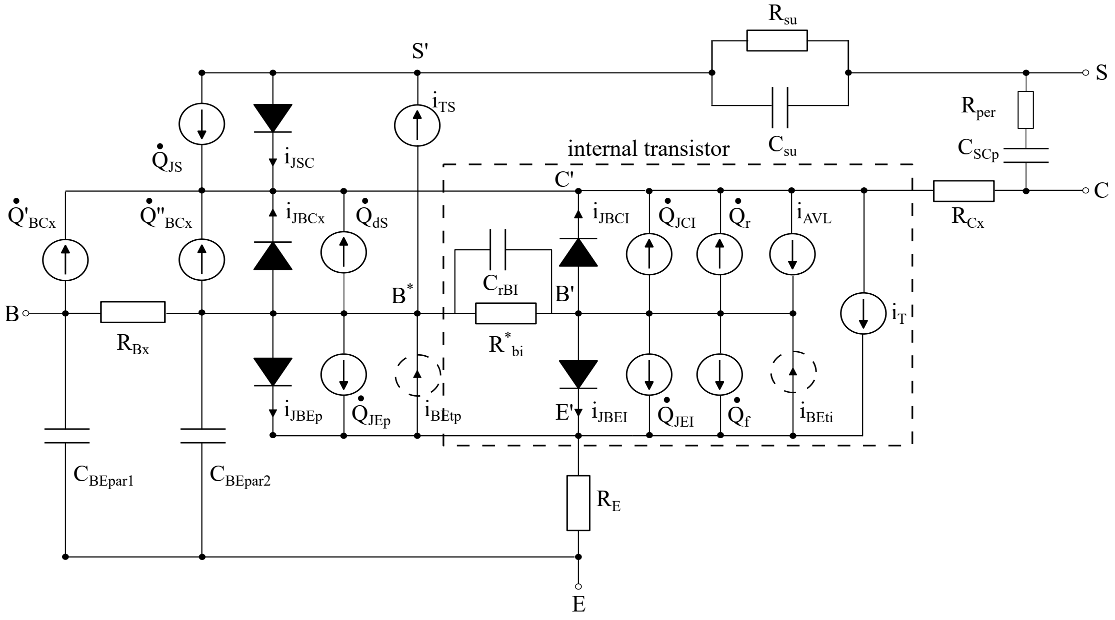
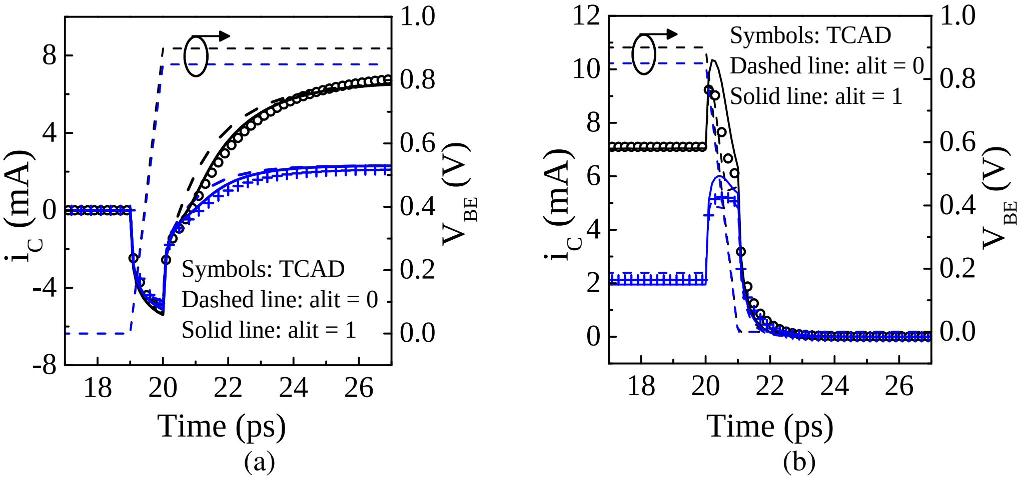


Fig. 5.7: Large-signal equivalent circuit of HICUM with an improved substrate network Saha *et al.* (2019).

5.5.1 NQS parameter

Extraction of the V-NQS parameter (***alit***):

Parameter ***alit*** in HICUM represents a factor for additional delay time of minority charge. We have performed a large-signal transient simulation of the calibrated TCAD device for the extraction of vertical NQS parameters. To make the transition very fast, both the turn-on and turn-off pulse have been considered a transition interval of 1 ps. The resulting turn-on and turn-off collector current ($i_C(t)$) versus time plots are shown in Figs. 5.8a and 5.8b respectively for two different bias conditions of V$_{BE}$ = V$_{CE}$ = 0.9 V and 0.85 V. In the turn-on behavior, $i_C(t)$ becomes negative for some time interval due to the charging of base-collector depletion capacitance. But, after that time interval, $i_C(t)$ increases with time. Comparing TCAD as reference, similar simulation in HICUM shows a high-level of agreement for the NQS parameter ***alit*** = 1. Simulation result for ***alit*** = 0, is also shown with the dashed line (in Fig. 5.8) which can not able to track the required dalay in the time-dependent characteristics. On the other hand, such a high value of ***alit*** is convincing since for very narrow base width and triangular slope of the Ge profile from emitter to collector induces a high drift field which claims almost all the incoming electrons (for n-p-n transistor) from the emitter to the collector.

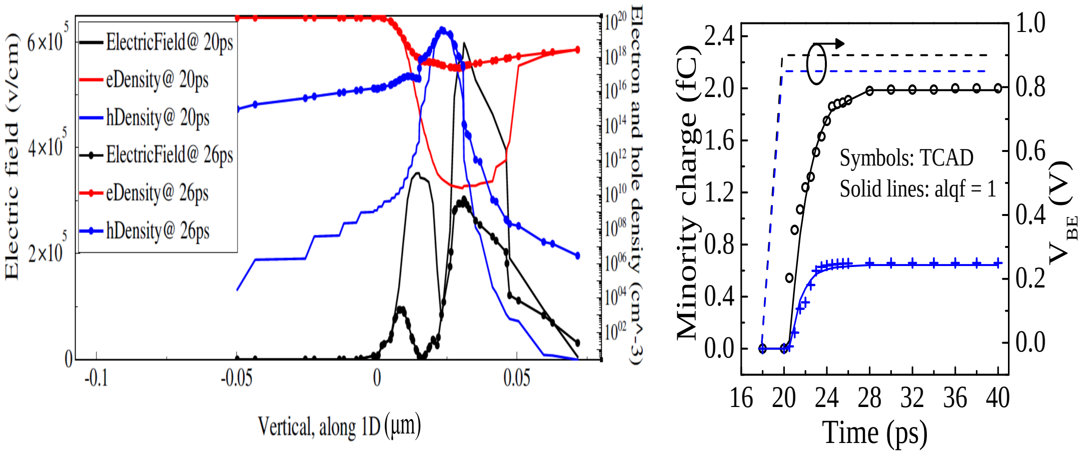


(a) (b)

Fig. 5.8: Turn-on (a), and turn-off (b) characteristics for the collector current $i_C(t)$: comparison between TCAD (symbols) and HICUM (solid line with $alit$=1, and dashed line with $alit$=0) for a 0.09 μm × 4.8 μm SiGe HBT biased at constant V_{CE}= 0.9 V (circles) and 0.85V (plus). $V_{BEs}(t)$ have been shown as a dashed-dot line to the right Y-axis.

Extraction of the V-NQS parameter (***alqf***):

Parameter ***alqf*** in HICUM represents a factor for additional delay time of minority charge Schröter and Chakravorty (2010). This parameter is extracted by analyzing the time-dependent behavior of the minority charge stored in the base region. Fig. 5.9a shows the excess carriers and electric field profiles at different time instants as the base-emitter voltage is ramped up from 0 V to 0.9 V from 18 ps to 20 ps (with 2 ps rise time). Note that the effects of higher V$_{BE}$ on the electric field and concentrations of electrons and holes are not visible immediately after 20 ps; instead delayed effects are observed at around 26 ps when field peaks are reduced allowing a wider quasi-neutral base region flooded with excess electrons and holes. Fig. 5.9b shows the time-dependent behavior of the stored charge at two different bias conditions. The surface integration tool available in TCAD is used to calculate the total minority carriers. Similar simulation result obtained from HICUM is also shown in Fig. 5.9b with ***alqf = 1***. Different delay times are taken by the stored charge to reach the steady-state which is also modeled accurately by HICUM.



(a) (b)

Fig. 5.9: Variation of electric field (left axis) and carrier density (right axis) captured at 20 ps (solid line) and 26 ps (solid line with symbols). The bias voltages V_{BE} = V_{CE} are ramped up from 0 V to 0.9 V at 18 ps with a rise time of 2 ps. The value $'0'$ in the X-axis refers to the position where poly-emitter and mono-emitter meet (a), and time dependent turn-on stored minority charge (in the emitter and base): comparison between TCAD (symbols) and HICUM (solid line with $alqf$ = 1) for the 0.09 μm × 4.8 μm SiGe HBT biased at V_{BE} = 0.9 V (circle) and V_{BE} = 0.85 V (plus), V_{BC} = 0 V. $V_{BEs}(t)$ have been shown as a dashed line to the right Y-axis.

Extraction of the L-NQS parameter (***fcrbi***):

The parameter ***fcrbi*** in HICUM represents the ratio between the capacitance (C_{rBi}) parallel to the internal base resistance to the total internal capacitance (junction and diffusion capacitance) Schröter and Chakravorty (2010). In the low-frequency regime, this parameter value is considered as 0.2. But in the high-frequency regime, the value of this parameter increases to consider the AC current crowding. The transistor used in this work has a small emitter width (0.2 μm) compare to length (5 μm), hence a value of 0.5 has been considered to this parameter.

5.5.2 Parasitic parameters

Extraction of the BE capacitance partitioning parameter (***fbepar***):

In HICUM, the parameter ***fbepar*** is the ratio between the internal BE parasitic capacitance component to the total BE parasitic component. To obtain the accurate transistor's characteristics, parasitic capacitances need to be as small as possible Wakimoto and Akazawa (1990). In general, for a given transistor geometry, there are mainly two types of parasitic capacitances which are related to the BE (C$_{BE,par}$) and BC region (C$_{BC,par}$). In Fig. 5.10a, a structure has been considered to calculate the parameter ***fbepar*** related to the C$_{BE,par}$. This customized structure is done in a way such that impacts coming from the shallow trench, epi-collector, and the internal transistor can be ignored in the simulation results. To compensate for the structural loss, we have considered the material as air (ϵ = 1). Once this is done, the resulting structure is simulated at an open collector terminal with V$_{BE}$ = 0 V. The resulting RC equivalent circuit of this customized structure (in Fig. 5.10a) is shown in Fig. 5.10b.

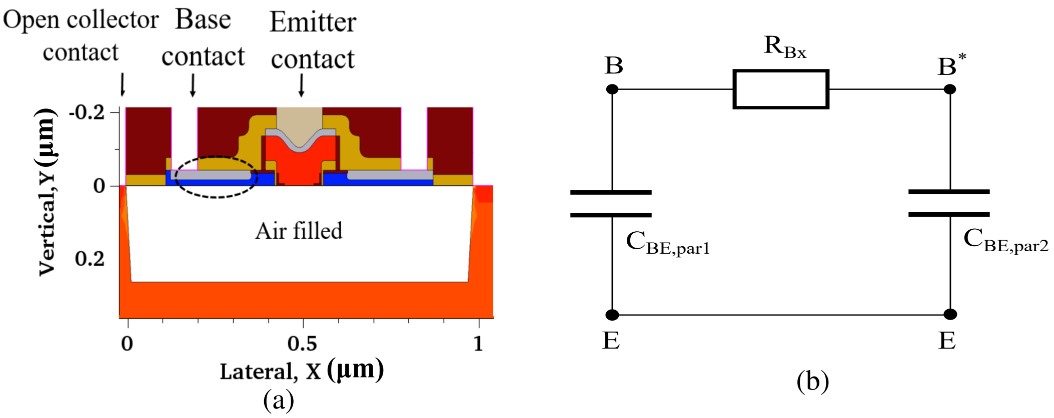


Fig. 5.10: Customized TCAD structure (grey: silicite, blue: p-type poly-Si) (a), and RC equivalent circuit representing the circled region in (a) for the determination of base-emitter parasitic capacitance partitioning factor ($fbepar$). Here B denotes the external base node (b).

Following Fig. 5.10b, the frequency-dependent effective BE capacitance can be deduced and represented in the following form:

$$C_{BE,par,eff} = \frac{(C_1 + C_2) + \omega^2 C_1 C_2^2 R_{Bx}^2}{1 + \omega^2 C_2^2 R_{Bx}^2} \tag{5.2}$$

with C_1=$C_{BE,par,1}$ and C_2=$C_{BE,par,2}$. Formulation (5.2) yields $C_{BE,par1} + C_{BE,par2}$ when $\omega \rightarrow 0$ and $C_{BE,par1}$ when $\omega \rightarrow \infty$. Following the TCAD based structure (Fig. 5.10a), frequency-dependent capacitance characteristic is plotted (Fig. 5.11) and partitioning factor (***fbepar***) is calculated. Following the model equation from HICUM, ***fbepar***(=C$_{BE,par2}$/(C$_{BE,par1}$+C$_{BE,par2}$)) is calculated as 0.93. Note that this value of ***fbepar*** also means that most of the BE parasitic capacitance is partitioned in to the internal transistor.

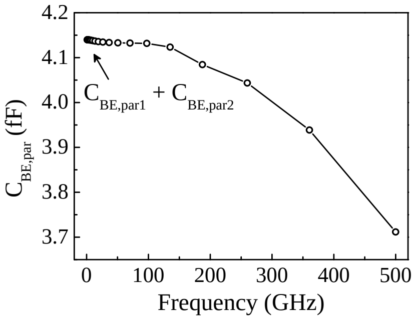
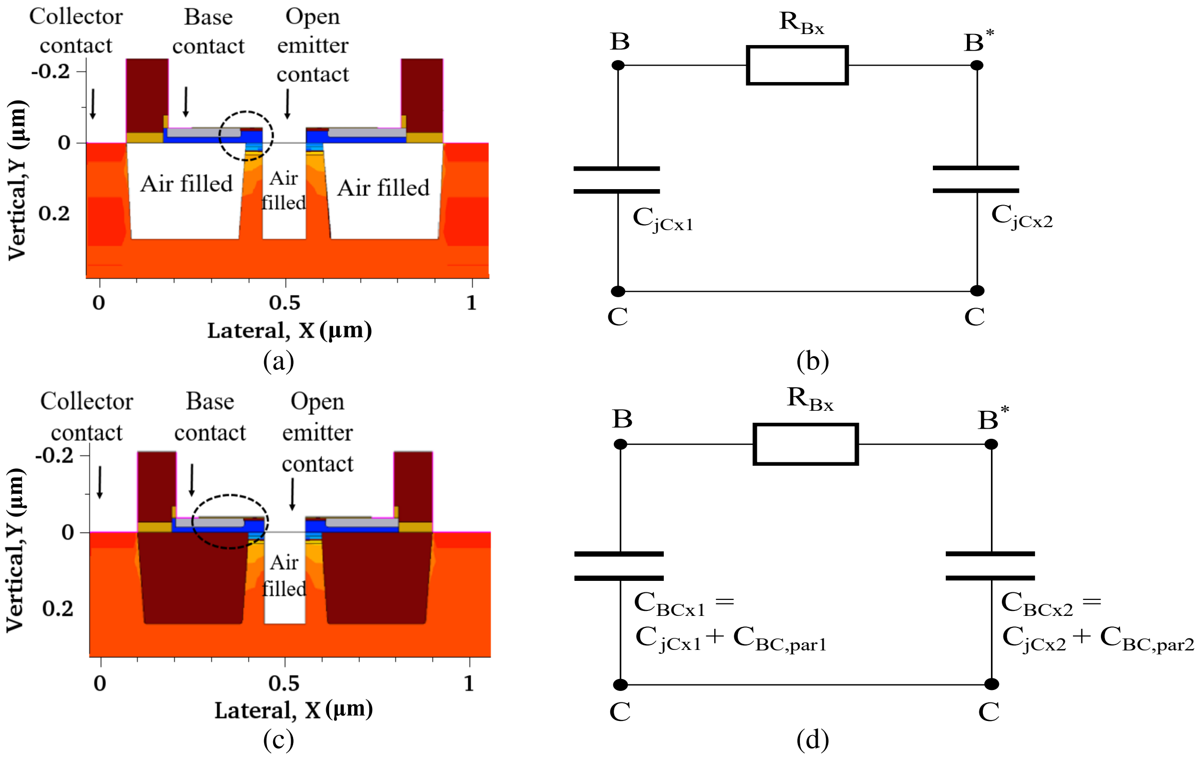


Fig. 5.11: Frequency-dependent capacitance characteristic for $fbepar$ extraction following the customized TCAD structure shown in Fig. 5.10a.

Extraction of the BC capacitance partitioning parameter (***fbcpar***):

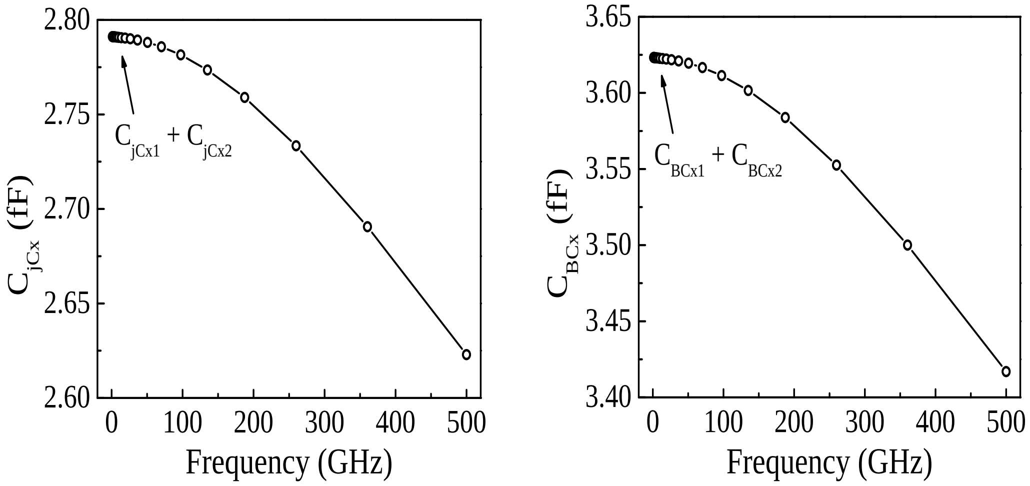
Following the same methodology like ***fbepar***, ***fbcpar*** is also extracted from the TCAD simulated frequency-dependent capacitance characteristics. As can be seen from Fig. 5.7, the total external base-collector capacitance (C$_{BCx}$) has two components: C$_{BCx1}$ from Q'$_{BCx}$ and C$_{BCx2}$ from Q''$_{BCx}$. Each of these components is again divided into two parts: namely the external base-collector junction capacitance (C$_{JCx}$) and parasitic base-collector capacitance (C$_{BC,par}$). To subtract the impact of parasitic components in the external BC capacitance, a customized TCAD structure is considered (Fig. 5.12a) for the calculation of C$_{JCx}$ only. The corresponding RC equivalent circuit, considering the external base resistance with the two partitioning capacitances, is shown in the Fig. 5.12b. Once these are done, the external BC junction capacitance can be calculated and following the similar approach with the TCAD customized structure (Fig. 5.12c) and equivalent RC circuit (Fig. 5.12d), the total external BC capacitance is calculated. While carrying out the TCAD simulation of both the structures (Figs.5.12a and 5.12c), the emitter terminal is kept open and V$_{BC}$ = 0 V is used. Since C$_{JCx}$ is calculated individually, C$_{BC,par}$ is calculated by subtracting C$_{JCx}$ from the total C$_{BCx}$.

Figs. 5.13a and 5.13b show the TCAD simulated frequency-dependent capacitance plots of the structures of Figs. 5.12a and 5.12c respectively. In (5.2), if $C_1 = C_{jCX1}$ and $C_2 = C_{jCX2}$ are used, one obtains the low-frequency approximation as C$_{jCx1}$ + C$_{jCx2}$ from Fig. 5.13a and C$_{jCx1}$ by fitting formulation (5.2). Similarly, Fig. 5.13b yields the low-frequency capacitance as C$_{BCx}$ = C$_{BCx1}$ + C$_{BCx2}$ and high-frequency capacitance as C$_{BCx1}$. From these TCAD results, we obtain C$_{BCx1}$ = 0.85 fF, C$_{BCx2}$ = 2.75 fF, C$_{jCx1}$ = 0.05 fF and C$_{jCx2}$ = 2.75 fF. Therefore, one obtains C$_{BCpar1}$ = 0.8 fF and C$_{BCpar2}$ = 0 fF. Since the capacitance C$_{BCx1}$ is close to Metal-1, an additional 1 fF capacitance has been added to C$_{BCx1}$. From these information, the value of the parameter **fbcpar**(=C$_{BCx2}$/(C$_{BCx1}$+C$_{BCx2}$)) is calculated as 0.6. Therefore it is noted that the internal part of the total BC capacitance is dominant.



(a) (b) (c) (d)

Fig. 5.12: Customized TCAD structure (a) and RC equivalent circuit (b) representing the left circled region for the determination of C_{jCx}, and the same (in (c) and, (d) respectively) for the determination of $C_{BCx} = C_{jCx} + C_{BC,par}$. B denotes the external base node.



(a) (b)

Fig. 5.13: Frequency-dependent capacitance characteristic following the customized TCAD structure shown in Fig. 5.12a (a) and 5.12c (b) for $fbcpar$ extraction.

5.5.3 Sensitivity analysis

Considering the above mentioned approach and tool, the extracted parameters are ***fbepar*** = 0.93, ***fbcpar*** = 0.6, ***alit*** = 1, ***alqf*** = 1, and ***fcrbi*** = 0.5. In this section, we perform the sensitivity analysis of the extracted parameters on the frequency-dependent small-signal parameters ($y-$,$h-$ or $z-$ parameters). Selective small-signal parameters are chosen in a way such that possible variation, with a change in value, can be easily identified. We have chosen a close peak f_T bias point which is V_{BE}= 0.85 V and V_{BC}= 0 V and sensitivity is observed by varying each of the parameters at a time keeping the other parameters at their initial extracted values. For example, while analyzing the effect of ***fbepar***, we keep ***fbcpar*** = 0.6, ***alit*** = 1, ***alqf*** = 1 and ***fcrbi*** = 0.5. We plot frequency-dependent $\mathrm{Im}\{y_{11}\}$ in Fig. 5.14 to showcase the possible variations for different values of the parameter ***fbepar***. Beyond 100 GHz, the low values of ***fbepar*** leads to an overestimation in $\mathrm{Im}\{y_{11}\}$. Although, note that below 100 GHz no variations are observed in the frequency-dependent characteristics.

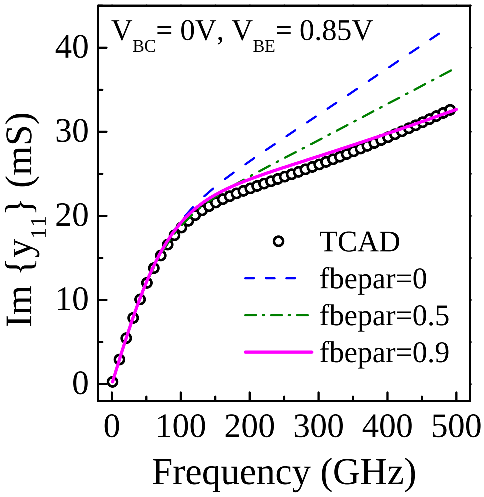
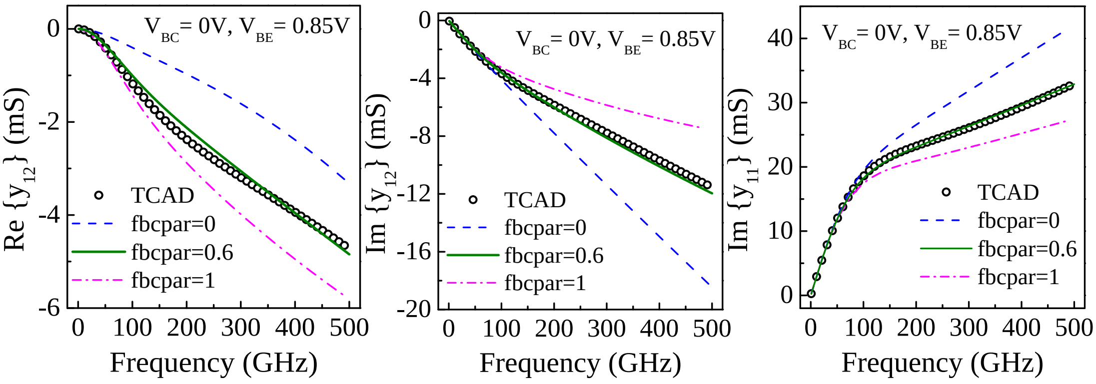


Fig. 5.14: Sensitivity of $fbepar$ on frequency-dependent $\mathrm{Im}\{y_{11}\}$ for the 0.09 μm × 4.8 μm SiGe HBT biased at V_{BC} = 0 V with V_{BE} = 0.85 V: comparison between TCAD (circles) and Hicum L2v2.4 (lines).

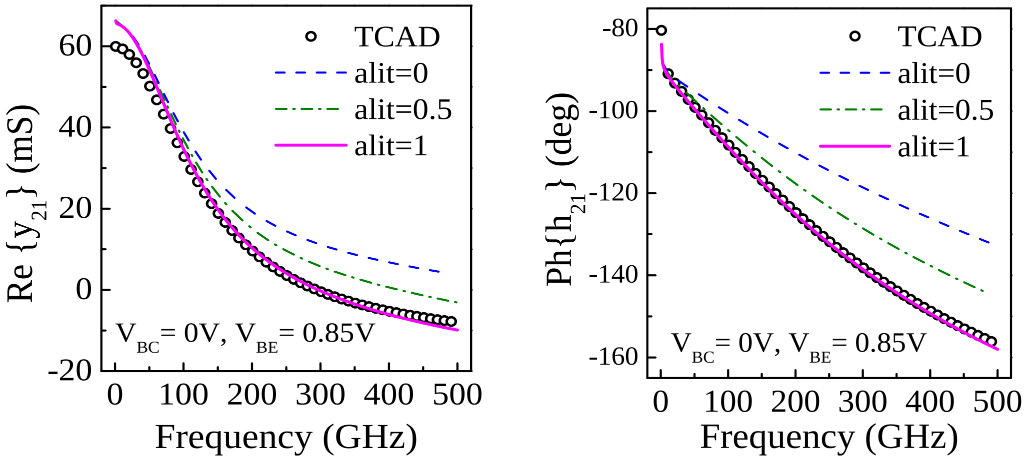
Similarly, we plot $\mathrm{Re}\{y_{12}\}$, $\mathrm{Im}\{y_{12}\}$ and $\mathrm{Im}\{y_{11}\}$ versus frequency in Figs. 5.15a, 5.15b, and 5.15c respectively to analyze the the sensitivity of the parameter ***fbcpar*** with keeping the other extracted parameters with their predetermined values. With varying ***fbcpar***, the frequency-dependent characteristics of $\mathrm{Im}\{y_{12}\}$ and $\mathrm{Im}\{y_{11}\}$ are remain unaffected up to 50 GHz but beyond that regime significant variations are observed. On the other hand, $\mathrm{Re}\{y_{12}\}$ varies significantly onwards from the low-frequency characteristics (Fig. 5.15a).



(a) (b) (c)

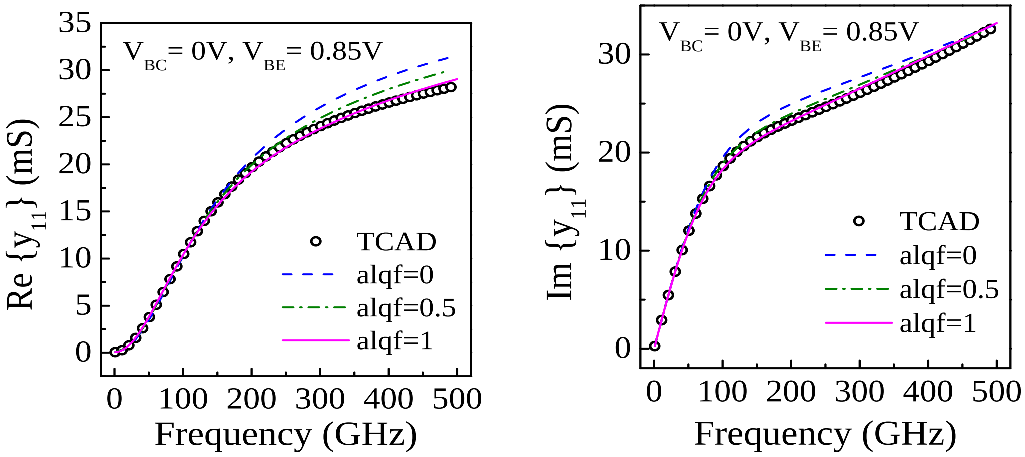
Fig. 5.15: Sensitivity of $fbcpar$ on frequency-dependent $\mathrm{Re}\{y_{12}\}$ (a), $\mathrm{Im}\{y_{12}\}$ (b) and $\mathrm{Im}\{y_{11}\}$ (c) for the 0.09 μm $\times$ 4.8 μm SiGe HBT biased at V_{BC} = 0 V with V_{BE} = 0.85 V: comparison between TCAD (circles) and Hicum L2v2.4 (lines).

The impact of **alit** is captured on the frequency dependent $\mathrm{Re}\{y_{21}\}$ characteristics where a significant overestimation has been observed at the lower values of **alit**. Like $\mathrm{Re}\{y_{21}\}$, $Ph\{h_{21}\}$ also shows the variation with **alit**. Fig. 5.16b depicts that a small value of **alit** results a smaller phase-shift at 500 GHz in h_{21}. Similarly the sensitivities of frequency-dependent $\mathrm{Re}\{y_{11}\}$ and $\mathrm{Im}\{y_{11}\}$ plots for various values of **alqf** are observed in Figs. 5.17a and 5.17b, respectively. Lower values of **alqf** tends to overestimate in particular $\mathrm{Re}\{y_{11}\}$, but it is only visible after 200 GHz. The impact of **alqf** on $\mathrm{Im}\{y_{11}\}$ is not very pronounced. Finally, Figs. 5.18a and 5.18b show the effect of different values of the parameter **fcrbi**, respectively, on the frequency-dependent $\mathrm{Re}\{z_{11}\}$ and $\mathrm{Im}\{z_{11}\}$ characteristics till 500 GHz. Unlike frequency-dependent $\mathrm{Im}\{z_{11}\}$ characteristics, $\mathrm{Re}\{z_{11}\}$ is slightly overestimated beyond 200 GHz with the variation of ***fcrbi***.



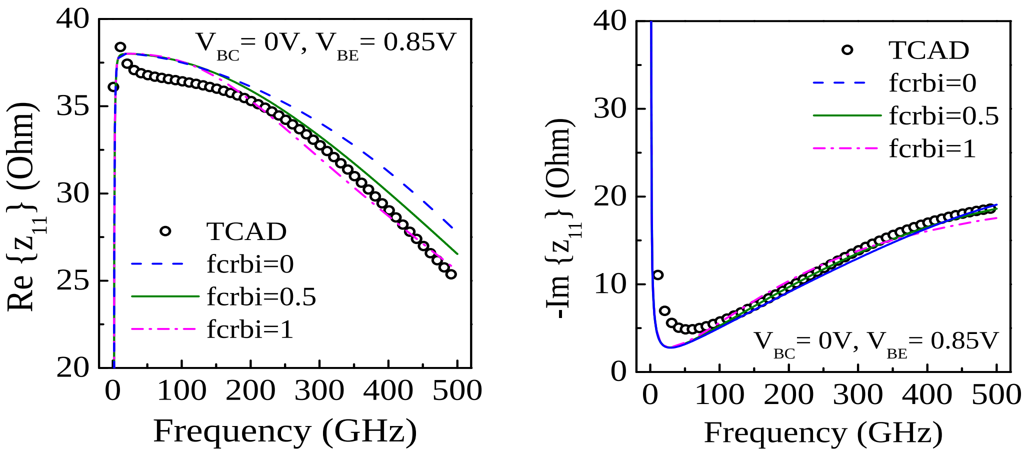
(a) (b)

Fig. 5.16: Sensitivity of $alit$ on frequency-dependent $\mathrm{Re}\{y_{21}\}$ (a), and $Ph\{h_{21}\}$ (b) for the 0.09 μm × 4.8 μm SiGe HBT biased at V_{BC} = 0 V with V_{BE} = 0.85 V: comparison between TCAD (circles) and Hicum L2v2.4 (lines).



(a) (b)

Fig. 5.17: Sensitivity of $alqf$ on frequency-dependent $\mathrm{Re}\{y_{11}\}$ (a) and $\mathrm{Im}\{y_{11}\}$ (b) for the 0.09 μm × 4.8 μm SiGe HBT biased at V_{BC} = 0 V with V_{BE} = 0.85 V: comparison between TCAD (circles) and Hicum L2v2.4 (lines).



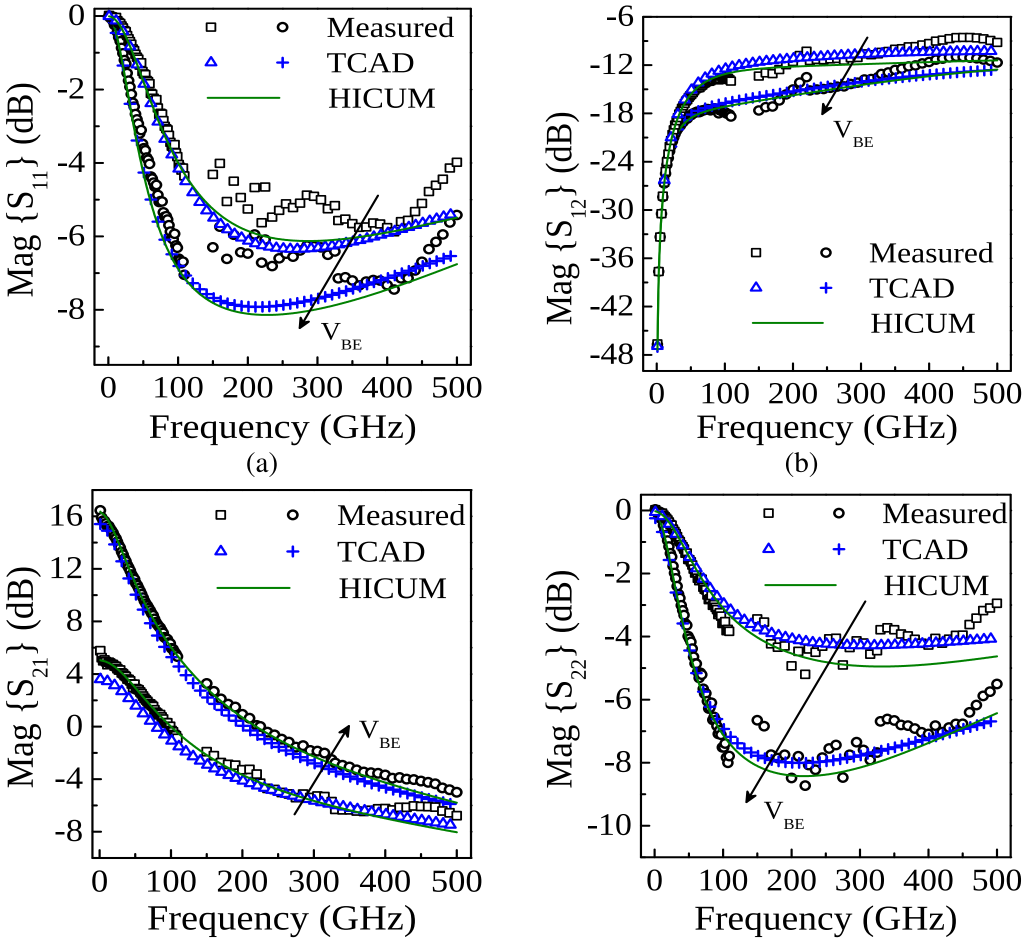
(a) (b)

Fig. 5.18: Sensitivity of $fcrbi$ on frequency-dependent $\mathrm{Re}\{z_{11}\}$ (a) and $\mathrm{Im}\{z_{11}\}$ (b) for the 0.09 μm × 4.8 μm SiGe HBT biased at V_{BC} = 0 V with V_{BE} = 0.85 V: comparison between TCAD (circles) and Hicum L2v2.4 (lines).

Based on the sensitivity analysis, it turns out that the extracted values of these five parameters are reliable. Unlike the variations shown by the parameters ***alqf*** and ***fcrbi*** on their respective frequency-dependent small-signal parameters, a significant variation is observed while varying the parameters ***fbepar***, ***fbcpar*** and ***alit***.

5.6 State-of-the-art compact model evaluation

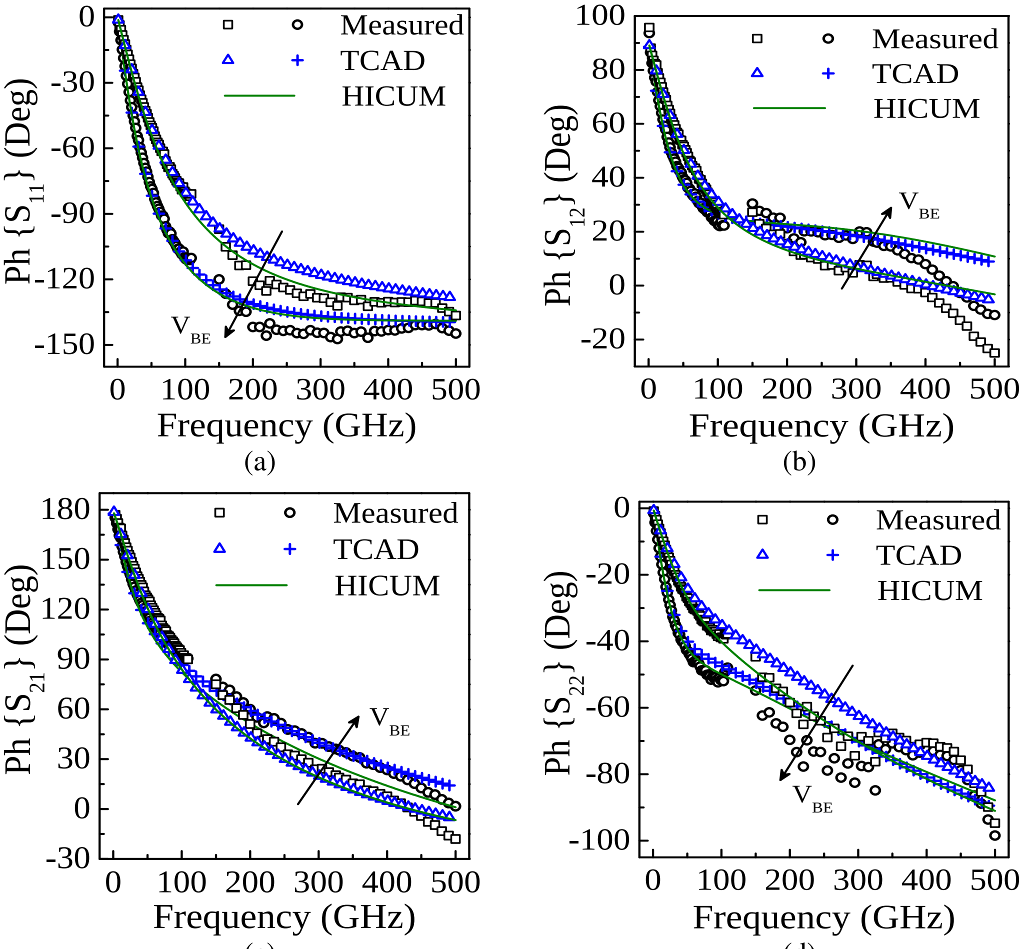
With the HICUM equivalent circuit (Fig. 5.7) and considering the extracted parameters, here we present a comparison among the results obtained from measurement, TCAD and, HICUM. In Figs. 5.19 and 5.20, we show the frequency-dependent $s-$ parameter's magnitude and phase respectively up to 500 GHz. Note that such high-frequency comparison is done for the first time comparing the existing literatures where either limited small-signal parameters (S_{21}, H_{21}, $MAG(U)$) Voinigescu *et al.* (2012) or only one frequency band Galatro *et al.* (2017) are reported. Observing the characteristics, it appears that the HICUM shows a high level of model agreement in the amplitude and phase of all s-parameters for two different bias points near the peak f_T. In the next sub-section, we are analyzing the HICUM based bias-dependent charges and validating the extracted values of the high-frequency parameters that are discussed in the previous sections.



(a) (b)

(c) (d)

Fig. 5.19: Frequency-dependent magnitude of scattering parameters for the 0.09 μm × 4.8 μm SiGe HBT biased at V_{BC} = 0V with V_{BE} = 0.8 V and 0.85 V: comparison between measured data (rectangles and circles), TCAD (triangle and cross) and HICUM (solid lines).



(a) (b) (c) (d)

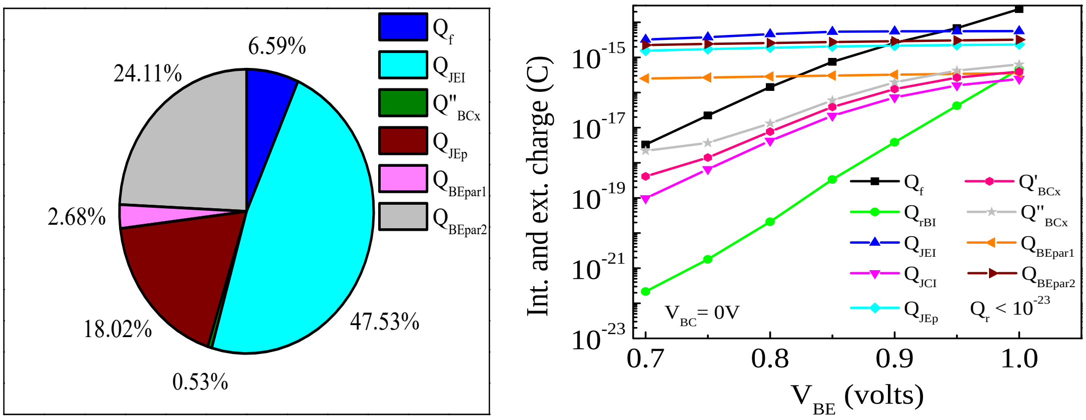
Fig. 5.20: Frequency-dependent phase of scattering parameters for the 0.09 μm × 4.8 μm SiGe HBT biased at V_{BC} = 0V with V_{BE} = 0.8 V and 0.85 V: comparison between measured data (rectangles and circles), TCAD (triangle and cross) and HICUM (solid lines).

5.6.1 Observation from internal, junction and parasitic charges

As we have observed that the relevant characteristics are nearly insensitive to a large variation in the parameters ***alqf*** and***fcrbi***; whereas those characteristics representing the sensitivity of***fbepar***,***fbcpar*** and ***alit*** show significant variations. This can be explained from the amount of charge assigned to each charge elements (Fig. 5.21) corresponding to the HICUM model equivalent circuit (Fig. 5.7). Since HICUM is large-signal model, the model elements are represented in the form of current and charge. Hence, we present those charge elements which are equivalent to the capacitances shown in Figs. 5.10b, 5.12b, and 5.12d. For the BE region, the charge $Q_{BE,par1}$ and $Q_{BE,par2}$ are calculated using the expression *cbepar1×V(br_be)* and *cbepar2×V(br_bpe)* respectively, where the formulation-terms are taken from the HICUM Verilog-A code. For the BC region, the charge Q'_{BCx} and Q''_{BCx} are related to the capacitances C_{BCx1} and C_{BCx2} respectively, each of which can be partitioned into junction and parasitic components. For the first part, the junction charge is calculated by strobing the term *qjcx0_t_i* and the parasitic charge is calculated using the expression *cbcpar1×V(br_bci).* As a same manner for the second part, strobing the term *qjcx0_t_ii* yields the junction charge and the parasitic charge *qbcpar2* is calculated using the expression *cbcpar2×V(br_bpci).* Additionally, the total diffused charge (Q_f), the charge across the internal-base resistance (Q_{rBI}), and the peripheral BE charge (Q_{JEp}) are calculated using the term $Qdei$, $qrbi$ and $Qjep$ respectively. And the internal BE and BC junction charge (Q_{JEI} and Q_{JCI}) are calculated following the expressions *Cjei×V(br_biei)* and *Cjci×V(br_bici)* receptively.

Fig. 5.21a depicts the share of total charge available for each charge element at bias point of V_{BE} = 0.85 V and V_{BC} = 0 V. It is observed that the share of the diffusion charge Q_f is much smaller (6.59%) compared to BE junction charge (Q_{jEi} that responds quasi-statically with the input excitation) and other external charge components. Notably the share of BE parasitic charge ($Q_{BE,par1}$ and $Q_{BE,par2}$) is significantly high (2.68% and 24.11%). Fig. 5.21b shows the bias-dependent variations of different charge elements. Here also we observe that the share of Q_f is quite small compared to Q_{jEi}, $Q_{BE,par1}$ and $Q_{BE,par2}$ until V_{BE} = 0.95 V where transit frequency drops significantly. One can note that the share of Q_{rBI} is insignificantly small compared to the other charge components at different bias regimes shown in Fig. 5.21b. Since the share of Q_f and Q_{rBI} are small, effects of their variations under fast transient are masked by the junction and parasitic charges assigned at the base side in the equivalent circuit. This makes the characteristics insensitive to the variation of ***alqf*** and ***fcrbi***.

On the contrary, the characteristics are highly sensitive to ***fbepar*** and ***fbcpar***. Comparatively a higher sensitivity is observed in the frequency-dependent $\mathrm{Re}\{y_{21}\}$ and $Ph\{h_{21}\}$ under the variation of the parameter ***alit***. This is because the output NQS model is implemented by delaying the collector current using an LCR sub-circuit and the parasitics at the collector side are not significantly large unlike those at the base side. It is, therefore, clear that the vertical input and lateral NQS effects are masked by the dominating external and parasitic charge components, unlike the vertical output NQS effect.



(a) (b)

Fig. 5.21: Two-dimensional π-chart showing the distribution for the charge amounts in each charge elements (having more than 0.5% share) in HICUM equivalent circuit at bias V_{BE} = 0.85 V and V_{BC} = 0 V (a), and V_{BE}-dependent comparative variations of different charges assigned to deployed HICUM charge elements (b).

5.6.2 Limitations at HF measurement and possible source of error

Although this part has been presented in Saha *et al.* (2021), we discuss this part here too. The overall modeling results are shown in Figs. 5.19 and 5.20 are quite reasonable but we have observed some unpredictable measurement trend appears in the specific frequency bands. Such behavior is mainly due to the adopted calibration and de-embedding tools. The calibration used to get the result has been evaluated in Fregonese *et al.* (2020). Nevertheless, some inaccuracies still appear in this measurement because TRL calibration is an 8 error terms algorithm that does not allow for cross-talk correction. If de-embedding partially corrects the cross-talk, some inaccuracies can still be observed.

For example, in s_{12} from 70 GHz to 220 GHz, unexpected results appear and can be explained by the scaling of the probes. Indeed, the Picoprobe DC-110 GHz and 140-220 GHz probes do not properly confine the EM fields to the device under test (DUT). The stray fields directly couple ports-1 and -2 as well as the port to ground. Therefore, the validity range of the measurement is from 1 to 70 GHz and from 220 to 350 GHz. In this range, a very good agreement is observed between the measurement, TCAD, and HICUM. The trend in the s_{12} phase measurement above 350 GHz that deviates from TCAD and HICUM is not representative of the intrinsic device and is attributed to a measurement artifact Fregonese *et al.* (2020). In this case, HICUM still appears to be reliable since it shows good agreement with the TCAD simulation.

Other inaccuracies appear on the magnitude of s_{11} and s_{22}. This can be attributed to the quality of the contact on the aluminum pad and the ability of the user to achieve a reproducible probe placement on each structure, which can alter the probe-substrate coupling. This leads to a deviation of about $\pm$ 1dB above 140 GHz, but the accuracy of the measurement is sufficient to validate the model. We can observe that the magnitudes of s_{11} and s_{22} decrease till 200 GHz and increases afterward. We attribute this behavior to the distributed lateral effect. Variation in s_{11} is very well captured by HICUM when ***fbepar*** and ***fcrbi*** are correctly set. Concerning the phase parameter of the reflection, the $Ph\{s_{11}\}$ is well measured without any strong discontinuity up to 500 GHz, which is less the case for s_{22}. Also note that the magnitude of s_{22} can be affected by the chosen value of R_{Cx}, the collector-substrate model elements, and the distributed effect within the substrate Saha *et al.* (2019). Hence, these parameters should be calculated accurately.

Another source of inaccuracy is the bias tees, which are different from one frequency band to another (resistance varying from 1.7 Ω to 2.5 Ω) which can slightly modify the

bias point of the transistor. At a very high bias, this can lead to some discontinuities on the magnitude of s_{21}. Except for this fact, the magnitude and phase of the s_{21} parameter are very well measured and the HICUM modeling result is perfectly reliable. This would not be the case without the NQS and external parasitic model in place.
In summary, the unexpected trends of those characteristics that deviate strongly from TCAD simulation are correlated to the calibration procedure and more generally to the measurement environment as shown in Fregonese *et al.* (2020); Panda *et al.* (2020). Finally, this work demonstrates that the HICUM model produces reasonable simulation results beyond f_T (=340 GHz), f_{MAX} (=370 GHz) and presents a good compromise between complexity and accuracy.

5.7 Conclusion

In this chapter, considering HICUM as a vehicle, a high-frequency investigation of the modern 55 nm BiCMOS SiGe HBT has been performed. To customized HICUM for this technology transistor, some specific high-frequency compact model parameters have been extracted following a calibrated TCAD based structure. Extracted high-frequency parameters are ***alit*** (for vertical output NQS), ***alqf*** (for vertical input NQS), ***fcrbi*** (for lateral NQS), ***fbepar*** (for external BE parasitic capacitance partitioning factor), and ***fbcpar*** (for external BC parasitic capacitance partitioning factor). Extracted parameters are further verified by the two approaches; viz. sensitivity and the bias-dependent charge analysis. The sensitivity analysis has been carried out on specific frequency-dependent small-signal parameters up to 500 GHz while for the charge analysis, we have plotted the stored, junction, and parasitic charges as a function of bias.
Considering the transistor from BiCMOS 55 nm technology, this study draws a limit on the frequency regime up to which the behavior remains quasi-static and it shows to obtain the actual behavior observations should be performed beyond 100 GHz.

CHAPTER 6

CONCLUSION

6.1 Summary of the work

For evaluating the high-frequency performance of a certain technology, the maximum oscillation frequency (f_{MAX}) is considered one of the most important performance indicators of the millimeter-wave transistor. However, due to measurement uncertainties in admittance parameters, it is difficult to determine f_{MAX}. Moreover, the extraction of f_{MAX} by the conventional methods (U-based extrapolation or using a single-pole transfer function) seems limited due to measurement noise and larger roll-off. Therefore, for a reliable and fast evaluation of a particular technology under development, there is no method to estimate f_{MAX}. Thus, we have developed an analytical model that can reliably extract f_{MAX} despite the noisy measurement data (Saha *et al.* (2021)). This approach is presented in Chapter 3. It is shown that based on the small-signal hybrid-π model, the admittance parameters are formulated in their real and imaginary parts, respectively. After this step, the formulations are directly interpolated into the measured data using the least mean squares technique, and f_{MAX} is calculated using Mason's gain formula. The proposed approach solves two important issues: first, the problem of predicting f_{MAX} in the low-frequency range, and second, this process accounts for the higher roll-off of f_{MAX} observed mainly in the high-frequency range, which cannot be achieved with the conventional f_{MAX} extraction from, unilateral gain versus frequency characteristics with a fitting line having a slope of -20 dB per decade.

This technological assessment is reliable if the device characterization and modelling can be performed accurately. However, modern BiCMOS technologies pose a critical challenge to accurate characterization due to high-frequency secondary effects, such as those arising from graded doping in the substrate. Since inaccurate substrate modeling affects the device output impedance and thus the overall gain, an accurate model is required. Therefore, we proposed an improved collector-substrate model using the SPICE-based approach, which was implemented in the state-of-the art HICUM compact model (Saha *et al.* (2019)). This improved model is presented in Chapter 4. This model mainly considered the peripheral effect, which is important in the deep trench based device structure. After calculating the physical model parameters from the technological data and layout information, the proposed model is implemented into the state-of-the-art HICUM compact model. The validity of the equivalent circuit was verified by on-wafer measurements on a SiGe HBT up to 330 GHz in the cold state and active forward bias condition.

Finally, we have investigated the high-frequency behavior of a transistor fabricated in the 55-nm BiCMOS process. This is mainly done to accurately deal with the non-ideal high-frequency effects (vertical and lateral non-quasi static effects) occurring in the device characteristics and then model them appropriately to improve the accuracy of the compact model. Existing literature has reported on the evaluation of compact models, but the results have been limited in terms of high-frequency data. In addition, no valuable partitioning of the dominant parasitic capacitances has been performed. From these perspectives, we have investigated the high-frequency behavior of SiGe HBTs using measured data up to 500 GHz, calibrated TCAD simulation, and special parameter extraction techniques (Saha *et al.* (2021)). This work is presented in Chapter 5 and mainly aims at modeling the high-frequency non-quasistatic (NQS) effect along with accurate partitioning of the parasitic capacitances. To extract the NQS-based compact model parameters, a large-signal transient simulation is performed. To extract the partitioning factors of the parasitic capacitances, custom TCAD structures are used to obtain frequency-dependent characteristics. Before the extracted parameters are used for s-parameter simulation in HICUM, sensitivity analysis and bias-dependent charge analysis are performed to gain confidence in the extracted values. This study highlights two important issues: First, since the specific low-frequency-dependent characteristics remain invariant when the high-frequency parameters are varied, so high-frequency measurements should be performed for an actual evaluation (above 100 GHz), and second, specific compact model parameters can be calculated using such TCAD-based custom structures.

6.2 Scope for the future research

The proposed collector-substrate model presented in chapter 4 can be further verified up to 500 GHz. Additionally, since we have observed the impact of back-end-of-line (BEOL) on the device's figure-of-merit in chapter 3 therefore the present TCAD structure can be further integrated with BEOL to get more realistic simulation results comparing the measured data. The study about the high-frequency effects, presented in chapter 5, can be further investigated in the high current regime (V_{BE} > 0.9V, when f_T starts to drop) with various transistor dimensions.

APPENDIX A

FAST EVALUATION OF f_{MAX} FOR SiGe HBTs

A.1 Analytical development of the small-signal y-parameters

Formulations (3.11) to (3.14) yield the complete y-parameters of the equivalent circuit of Fig. 3.5. Now, in order to use these equations for predicting f_{MAX} using (3.1) along with (3.2), we express (3.11) to (3.14) into real and imaginary parts in the form of polynomial functions,

$$\mathrm{Re}\{y_{11T}\} = \frac{c_2 + c_3\omega^2 + c_4\omega^4 + c_5\omega^6}{c_6 + c_7\omega^2 + c_8\omega^4 + c_9\omega^6} = \frac{\alpha_1 + \alpha_2\omega^2 + \alpha_3\omega^4 + \alpha_4\omega^6}{1 + \alpha_5\omega^2 + \alpha_6\omega^4 + \alpha_7\omega^6} \tag{A.1}$$

$$\mathrm{Im}\{y_{11T}\} = \frac{c_{10}\omega + c_{11}\omega^3 + c_{12}\omega^5 + c_{13}\omega^7}{c_6 + c_7\omega^2 + c_8\omega^4 + c_9\omega^6} = \frac{\alpha_8\omega + \alpha_9\omega^3 + \alpha_{10}\omega^5 + \alpha_{11}\omega^7}{1 + \alpha_5\omega^2 + \alpha_6\omega^4 + \alpha_7\omega^6} \tag{A.2}$$

$$\mathrm{Re}\{y_{12T}\} = \frac{c_{14}\omega^2 + c_{15}\omega^4}{c_{16} + c_{17}\omega^2 + c_{18}\omega^4} = \frac{\alpha_{12}\omega^2 + \alpha_{13}\omega^4}{1 + \alpha_{14}\omega^2 + \alpha_{15}\omega^4} \tag{A.3}$$

$$\mathrm{Im}\{y_{12T}\} = \frac{c_{19}\omega + c_{20}\omega^3}{c_{16} + c_{17}\omega^2 + c_{18}\omega^4} = \frac{\alpha_{16}\omega + \alpha_{17}\omega^3}{1 + \alpha_{14}\omega^2 + \alpha_{15}\omega^4} \tag{A.4}$$

$$\mathrm{Re}\{y_{21T}\} = \frac{c_{21} + c_{22}\omega^2 + c_{23}\omega^4}{c_{16} + c_{17}\omega^2 + c_{18}\omega^4} = \frac{\alpha_{18} + \alpha_{19}\omega^2 + \alpha_{20}\omega^4}{1 + \alpha_{14}\omega^2 + \alpha_{15}\omega^4} \tag{A.5}$$

$$\mathrm{Im}\{y_{21T}\} = \frac{c_{24}\omega + c_{25}\omega^3}{c_{16} + c_{17}\omega^2 + c_{18}\omega^4} = \frac{\alpha_{21}\omega + \alpha_{22}\omega^3}{1 + \alpha_{14}\omega^2 + \alpha_{15}\omega^4} \tag{A.6}$$

$$\mathrm{Re}\{y_{22T}\} = \frac{c_{26} + c_{27}\omega^2 + c_{28}\omega^4}{c_{16} + c_{17}\omega^2 + c_{18}\omega^4} = \frac{\alpha_{23} + \alpha_{24}\omega^2 + \alpha_{25}\omega^4}{1 + \alpha_{14}\omega^2 + \alpha_{15}\omega^4} \tag{A.7}$$

$$\mathrm{Im}\{y_{22T}\} = \frac{c_{29}\omega + c_{30}\omega^3}{c_{16} + c_{17}\omega^2 + c_{18}\omega^4} = \frac{\alpha_{26}\omega + \alpha_{27}\omega^3}{1 + \alpha_{14}\omega^2 + \alpha_{15}\omega^4} \tag{A.8}$$

where the coefficient c_i are based on the small-signal model parameters (represented below via the parameter 'β_i') and α_i is the normalization factor with respect to c_i. Interpolating and optimizing the equations from (A.1) to (A.8) and comparing the coefficients values calculated from the technology specific small-signal model parameters (shown in the sub-section), we note that the high frequency coefficients (beyond ω^2) are very small in magnitude compared to low frequency counterpart. Therefore, we represent c_i (up to ω^2) as,

$c_2 = \beta_1\beta_6^2$

$c_3 = \beta_1\beta_6(2\beta_8 + \beta_3\beta_6 + r_c\beta_0\beta_3 + r_c\beta_4\beta_7) - r_c\beta_0\beta_4(\beta_2\beta_6 + \beta_1\beta_{10}) + \beta_2\beta_5\beta_6^2 + \beta_1\beta_{10}^2$

$c_6 = \beta_1^2\beta_6^2$

$c_7 = 2\beta_1^2\beta_6\beta_8 + \beta_2^2\beta_6^2 + \beta_1^2\beta_{10}^2$

$c_{10} = \beta_1\beta_5\beta_6^2 + r_c\beta_0\beta_1\beta_4\beta_6 - \beta_2\beta_6^2$

$c_{14} = \beta_4\beta_{10} - \beta_3\beta_6$

$c_{16} = \beta_6^2$

$c_{17} = 2\beta_6\beta_8 + \beta_{10}$

$c_{19} = -\beta_3\beta_6$

$c_{21} = \beta_0\beta_6$

$c_{22} = \beta_0\beta_8 - \beta_3\beta_6 + \beta_7\beta_{10}$

$c_{24} = \beta_6\beta_7 - \beta_0\beta_{10}$

$c_{26} = \frac{\beta_1\beta_6}{r_0}$

$c_{27} = \frac{\beta_1\beta_8}{r_0} + \frac{\beta_6\beta_8}{r_c} + \beta_9\beta_{10}$

$c_{29} = \beta_6\beta_9 - \frac{\beta_1\beta_{10}}{r_0}$

where the parameters β_i relate to the small-signal model parameter by the following means,

$\beta_0 = g_{m0} r_\pi$

$\beta_1 = r_\pi + R_{BiT}$

$\beta_2 = r_\pi R_{BiT}(C_\pi + C_\mu)$

$\beta_3 = -r_\pi R_{BiT} C_{bc}(C_\pi + C_\mu)$

$\beta_4 = -(r_\pi C_\mu + r_\pi C_{bc} + R_{BiT} C_{bc})$

$\beta_5 = r_\pi(C_\pi + C_\mu) + (r_\pi + R_{BiT})C_{bc}$

$\beta_6 = r_\pi + R_{BiT} + \frac{r_c r_\pi}{r_0} + \frac{r_c R_{BiT}}{r_0}$

$\beta_7 = -(r_\pi C_{bc} + r_\pi C_\mu + R_{BiT} C_{bc} + r_\pi g_{m0} \tau_d)$

$\beta_8 = -r_c r_\pi R_{BiT}(C_\pi C_\mu + C_{bc}(C_\pi + C_\mu) - g_{m0} \tau_d C_\mu)$

$\beta_9 = R_{Bit} C_\mu + r_\pi C_\mu + R_{BiT} C_{bc} + r_\pi C_{bc} + r_\pi R_{BiT} C_\mu g_{m0} + \frac{r_\pi R_{BiT}}{r_0}(C_\mu + C_\pi)$

$\beta_{10} = r_\pi R_{BiT}(C_\pi + C_\mu) + r_c R_{Bit} C_\mu + r_c r_\pi C_{bc} + r_c R_{BiT} C_{bc} + r_c r_\pi C_\mu + r_c r_\pi R_{BiT} C_\mu g_{m0} + \frac{r_c r_\pi R_{BiT}}{r_0}(C_\pi + C_\mu).$

Here we represent the polynomials up to second order in ω as,

$$\mathrm{Re}\{y_{11}\} \simeq \frac{a_{1,11} + a_{2,11}\omega^2}{1 + a_{3,11}\omega^2} \tag{A.9}$$

$$\mathrm{Im}\{y_{11}\} \simeq \frac{b_{1,11}\omega}{1 + b_{2,11}\omega^2} \tag{A.10}$$

$$\mathrm{Re}\{y_{12}\} \simeq \frac{a_{2,12}\omega^2}{1 + a_{3,12}\omega^2} \tag{A.11}$$

$$\mathrm{Im}\{y_{12}\} \simeq \frac{b_{1,12}\omega}{1 + b_{2,12}\omega^2} \tag{A.12}$$

$$\mathrm{Re}\{y_{21}\} \simeq \frac{a_{1,21} + a_{2,21}\omega^2}{1 + a_{3,21}\omega^2} \tag{A.13}$$

$$\mathrm{Im}\{y_{21}\} \simeq \frac{b_{1,21}\omega}{1 + b_{2,21}\omega^2} \tag{A.14}$$

$$\mathrm{Re}\{y_{22}\} \simeq \frac{a_{1,22} + a_{2,22}\omega^2}{1 + a_{3,22}\omega^2} \tag{A.15}$$

$$\mathrm{Im}\{y_{22}\} \simeq \frac{b_{1,22}\omega}{1 + b_{2,22}\omega^2}. \tag{A.16}$$

The following equations show the compact representation of the above derived equations in the real and imaginary forms,

$$\mathrm{Re}\{y_{ij}\} \simeq \frac{a_{1,ij} + a_{2,ij}\omega^2}{1 + a_{3,ij}\omega^2}, \tag{A.17}$$

$$\mathrm{Im}\{y_{ij}\} \simeq \frac{b_{1,ij}\omega}{1 + b_{2,ij}\omega^2}. \tag{A.18}$$

Where $a_{1,ij}$, $a_{2,ij}$, $a_{3,ij}$ and $b_{1,ij}$, $b_{2,ij}$ are the coefficient and the function of small-signal parameters.

A.2 Parameter verification and f_{MAX} variation

Following y- and z-parameter based parameter extraction procedure Jun (2009), we have extracted the small-signal parameters (see (Table.A.1)) of both technology devices (55 nm BiCMOS and 130 nm BiCMOS). The DC trans-conductance (g_{m0}) has been extracted from the measured data at the low-frequency.

Table A.1: Extracted small-signal parameters of both BiCMOS technologies.

Small-signal parameters	55 nm BiCOMS	130 nm BiCOMS
g_{m0} (mS)	98.5	248
τ_d (ps)	0.2	0.8
R_{BiT} (Ω)	30.5	1.5
r_π (kΩ)	3	0.95
r_c (Ω)	23.5	8.5
c_π (fF)	30	55
c_μ (fF)	3	12
c_{bc} (fF)	1.8	1.5

In the following (Table A.2), the coefficients of the polynomials have been compared.

Table A.2: Co-efficients in formulated model: Interpolated and calculated from small-signal parameters.

Coefficients (in equation)	Interpolate		Cal. from small-signal parameters	
	55nm BiCMOS	130nm BiCMOS	55nm BiCMOS	130nm BiCMOS
α_1 (A.1)	2.43 e-4	9.91 e-4	3.29 e-4	10.5 e-4
α_2 (A.1)	5 e-26	7.28 e-26	5.15 e-26	-7.7 e-27
α_3 (A.1)	1.89 e-49	1.66 e-48	5.91 e-50	7.92 e-52
α_4 (A.1)	9.74 e-73	8.29 e-71	2.9 e-76	2.33 e-78
α_5 (A.1,A.2)	3.16 e-24	1 e-25	2.6 e-24	1.15 e-25
α_6 (A.1,A.2)	3.73 e-47	1 e-45	1.6 e-48	1.48 e-51
α_7 (A.1,A.2)	2.01 e-72	7.78 e-70	4.07 e-75	4.28 e-78
α_8 (A.2)	4.49 e-14	9.87 e-14	4.51 e-14	9.66 e-14
α_9 (A.2)	1.25 e-37	2.79 e-37	5.67 e-38	1.55 e-38
α_{10} (A.2)	9.07 e-61	8.69 e-59	3.89 e-63	8.27 e-65
α_{11} (A.2)	1 e-92	1.26 e-82	2.51 e-90	6.82 e-93
α_{12} (A.3)	-4.3 e-27	-3.35 e-27	-4.49 e-27	-3.26 e-27
α_{13} (A.3)	-1.11 e-57	-1.01 e-54	-1.14 e-52	3.1 e-54
α_{14} (A.3-A.8)	2.06 e-24	8.33 e-25	1.61 e-24	1.05 e-25
α_{15} (A.3-A.8)	-9.34 e-49	-1 e-55	4.1 e-51	4.25 e-52
α_{16} (A.4)	-5.03 e-15	-1.32 e-14	-4.77 e-15	-1.35 e-14
α_{17} (A.4)	-2.2 e-39	-7.69 e-39	-2.06 e-39	-3.16 e-40
α_{18} (A.5)	9.68 e-2	0.25	9.75 e-2	0.25
α_{19} (A.5)	-2.63 e-27	4.87 e-26	-1.07 e-26	1.84 e-27
α_{20} (A.5)	-1.04 e-49	-5.09 e-57	-1.15 e-52	3.1 e-54
α_{21} (A.6)	-1.51 e-13	-2.85 e-13	-1.33 e-13	-7.61 e-14
α_{22} (A.6)	-1 e-42	-1 e-42	-2.06 e-39	-3.16 e-40
α_{23} (A.7)	1.89 e-26	1.93 e-26	1.54 e-26	6.97 e-27
α_{24} (A.7)	9.53 e-52	1 e-50	1.75 e-52	5 e-53
α_{25} (A.7)	1.64 e-14	2.84 e-14	1.37 e-14	1.79 e-14
α_{26} (A.8)	4.17 e-39	1.2 e-38	2.72 e-39	-2.43 e-40

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