Optimization of GaN-based Series-Parallel Multilevel Three-Phase Inverter for Aircraft applications

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Résumé détaillé en français

Optimisation d'un Onduleur GaN Multiniveaux Série-Parallèle Triphasé pour des applications Aéronautiques

Cette thèse traite de la thématique d'électrification des avions. En synthèse, le poids de l'avion a une relation directe avec la consommation de carburant et donc avec les émissions de gaz polluants. En remplacent des lourds systèmes mécaniques par les d'équivalents électriques, on arrive à une réduction de masse de l'avion et à une augmentation du rendement, parmi d'autres points positifs. Théoriquement, il existe deux architectures : l'avion 100 % électrique qui est très performent mais il y a une limitation de systèmes de stockage de l'énergie ainsi que l'avion plus électrique, nommé en anglais *MEA*(*More Electric Aircraft*) , c'est-à-dire un avion intermédiaire dans lequel quelques systèmes mécaniques sont remplacés par des systèmes électriques.

En ce qui concerne l'électrification des avions, le projet Epowerdrive a été conçu en 2017 par les industrielles et les centres de recherche français. Le but de ce projet a été de mieux comprendre l'usage des composants grands gap, comme Mosfet SiC et GaN, et leur intégration dans les convertisseurs de puissance. Des modèles et des méthodologies ont été développées pour augmenter le rendement, la densité de puissance et la fiabilité des chaînes électromécaniques qui représentent un système de l'avion ; par exemple, le système de ventilation (*ECS*). Ainsi, une chaîne électromécanique est composée par un onduleur (filtres et système de refroidissement compris), des câbles et une machine électrique comme le montre la Figure 1 ci-dessous.

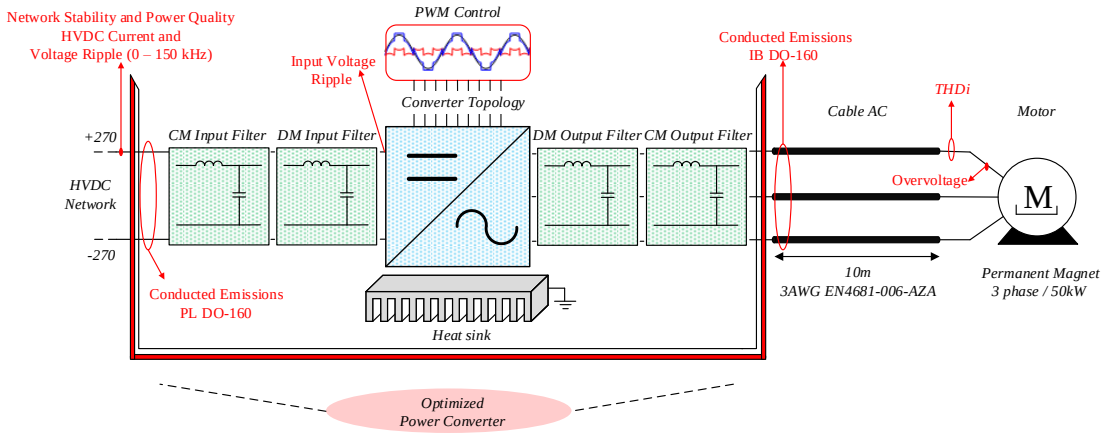


Figure 1 – Chaîne életromécanique d'un avion plus électrique.

Par conséquent, l'objectif de ce travail est d'identifier et de réaliser un onduleur avec une densité de puissance supérieure à 8 kW/kg et un rendement supérieur à 98.5 % pour une chaine électromécanique de 70 kVA comment on a montré dans la Figure 1. Pour y arriver, des différentes contraintes de projet ont été considérés :

- La tension de bus HVDC : 540 V;
- L'ondulation de tension de 5% à l'entrée de l'onduleur (27 V) ;
- La norme Airbus *HVDC Power Quality* (0 – 150kHz) pour l'ondulation de tension et le courant à l'entrée de l'onduleur ;

- Le niveau de surtension maximal aux bornes de la machine électrique : 850 V;
- Le taux de distorsion harmonique de courant de sortie (THD_i): 7%;
- Les limites d'émissions conduites proposés par la norme RTCA/DO-160G (150 kHz – 152 MHz) – *Load Category L, M, et H. Power Lines limits* et *Interconnecting Bundles* sont considérés pour l'entrée et pour la sortie de l'onduleur, respectivement ;
- Les émissions conduites sont due uniquement par le courant de mode commun.
- La valeur maximale de la capacité en mode commun de 150 nF en raison de la limitation du courant de foudre ;
- Le système de refroidissement à air force ;
- Un câble aéronautique triphasé non blinde de 10 mètres - 3AWG EN4681-006-AZA;
- 50 kW/70 kVA une machine électrique triphasé à ima permanent ;
- Le point d'opération nominal de la machine : 3600 rpm/132 N.m/70 kVA kW/130 Arms;
- La température ambiante de 70°C;
- Uniquement des filtres passifs.

D'après ces contraintes, le premier chapitre de cette recherche présente les différents blocs de conception pour évaluer l'impact des différentes topologies d'onduleurs multiniveaux et des technologies de semi-conducteurs sur le poids et les performances globales d'un onduleur de 70 kVA qui répond aux critères cités auparavant. La Figure 2 ci-dessous montre les topologies qui ont été retenues lors de l'optimisation.

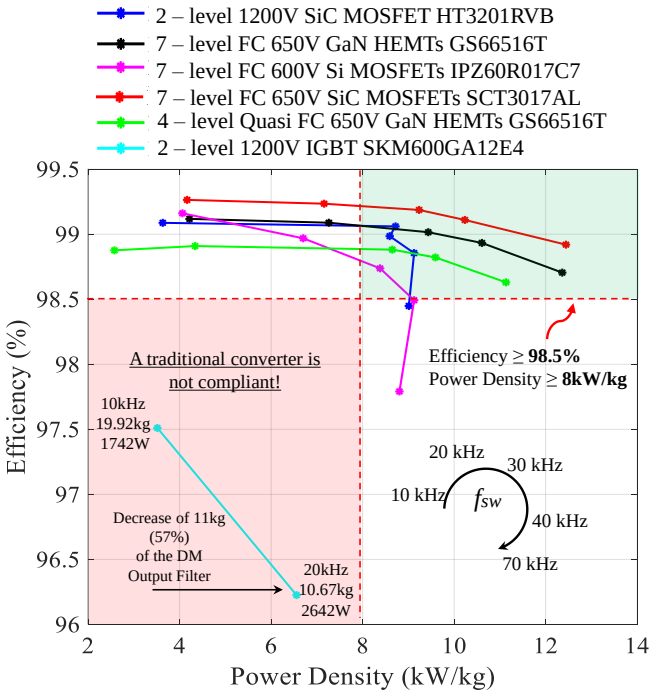


Figure 2- Les résultats d'optimisation de différentes topologies d'onduleurs (7-level FC, 4 – level Quasi-FC and 2-level) avec différentes technologies de semi-conducteurs (IGBT-Si, SiC MOSFETs, et GaN HEMT) pour des fréquences de découpage entre 10 kHz et 70 kHz. Notez que la topologie IGBT à 2 niveaux n'est pas conforme aux objectifs de densité de puissance et de rendement. Puissance nominale = 70 kVA, V_{bus} = 540 V, et DPWM1.

La Figure 2 montre que les semi-conducteurs WBG sont la clé pour augmenter l'efficacité des onduleurs à des niveaux supérieurs à 99 %. Un onduleur traditionnel avec 1200 V IGBT (dernière génération) à 10 kHz a atteint 97,8 %, tandis que 99,4 % a été réalisé avec un module 1200 V SiC (onduleur sans filtres).

Les topologies à multiniveaux ont un impact direct sur l'augmentation de la densité de puissance de l'onduleur de 3,63 kW/kg à 4,21 kW/kg à 10 kHz pour les topologies à 2 et 7 niveaux, respectivement. En passant à 70 kHz, cette augmentation est encore plus élevée. Elle passe de 9 kW/kg à 12,36 kW/kg, montrant que si le critère le plus important était la densité de puissance, il y aurait un gain considérable avec l'utilisation de topologies multiniveaux, notamment avec l'augmentation de la fréquence de découpage.

De cette façon, la topologie choisie pour une étude plus détaillée des modèles et de leur réalisation est représentée par la Figure 3. C'est une topologie de 7 niveaux composée par 3 bras *Flying Capacitor* en parallèle par phase à travers des inductances non couplées. De plus, elle a un total de 144 composants GaN GS66516T avec 4 composants en parallèle par switch.

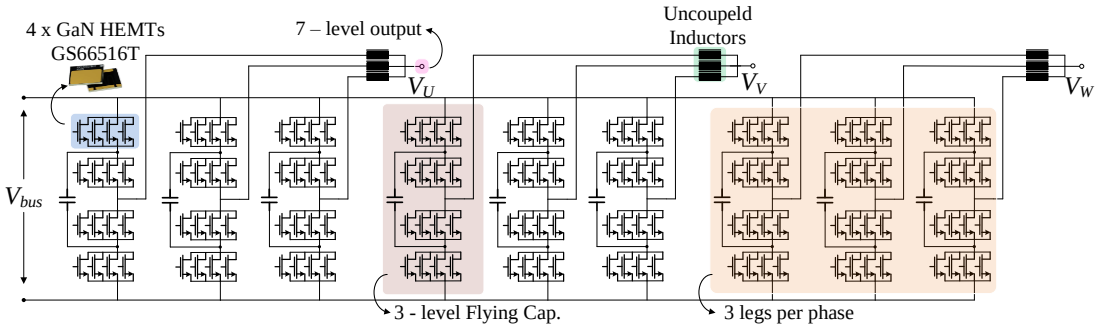


Figure 3 – Topologie d'onduleur choisi pour l'amélioration des modèles et de la réalisation.

Concernant le Chapitre 3, une méthodologie de modélisation des convertisseurs multiniveaux et d'autres éléments associés, tels que les câbles et le moteur vis-à-vis du mode commun (MC), ont été présentés. L'objectif de ce chapitre est de proposer un circuit MC équivalent pour des topologies d'onduleurs multiniveaux en tenant compte du couplage entre l'entrée et la sortie, visant une conception des filtres CEM plus précise. Le modèle proposé est composé de deux sources de tensions comme indiqué sur la Figure 4. La source $V_{CM,Out}$ considère les sources de tensions connectées à la sortie du convertisseur. La source $V_{CM,S}$ prend en compte des sources de tension intermédiaires non connectées à la sortie du convertisseur, c'est-à-dire, au câble de sortie.

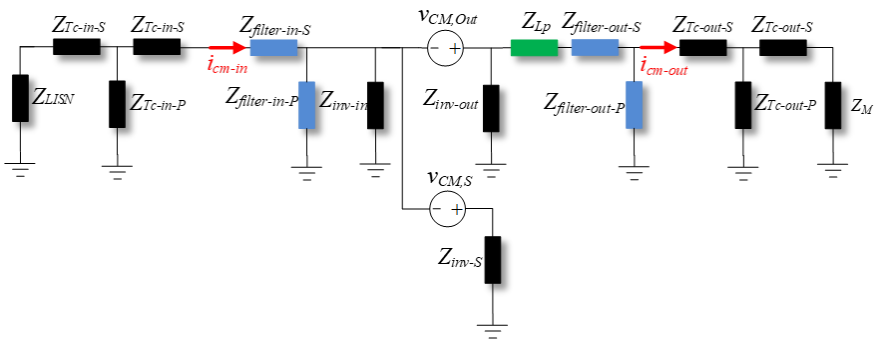


Figure 4 – Le modèle CEM proposé en considérant le couplage entre l'entrée et la sortie des topologies multiniveaux.

Ce modèle a été appliqué à la topologie 7 niveaux choisi dans le but de vérifier l'impact sur la conception des filtres CEM. Le filtre CEM a montré une augmentation de 85 % (276 g) sur le poids, en comparant le modèle non couplé présenté dans la Figure 2 et le modèle couplé pour les mêmes conditions. Cela renforce le besoin d'un modèle plus précis pour concevoir des filtres CEM pour les convertisseurs multiniveaux. De plus, une étude paramétrique de la topologie et de la répartition des filtres MC a mis en évidence que la solution la plus légère (600 g) trouvait une self MC sur l'entrée et une self MC sur la sortie. L'utilisation de la capacitance $C_{Y\text{-}out}$ permet une réduction de poids significative de 66,7% (1,2 kg) par rapport à l'autre topologie présentée sans elle.

Dans une suite logique, le Chapitre 4 présente l'impact de différentes techniques PWM y compris le FCPWM et l'ILPWM qui ont été proposées pour la réduction du poids et les pertes globales de la topologie 7 niveaux. Les procédures et les conditions de conception étaient les mêmes que celles considérées dans le Chapitre 2, à l'exception du modèle EMI qui utilisait le modèle couplé proposé. De plus, l'ondulation de courant superposée à la composante fondamentale a été prise en compte pour la conception des inductances de sortie. Il augmente le courant de crête de l'inductance, il y a donc une prise du poids du noyau pour la même inductance. La technique DPWM3 a présenté la densité de puissance gravimétrique la plus élevée parmi les différentes techniques (8,99 kW/kg) à 40 kHz et DPWM2 (9,53 kW/kg) à 70 kHz. L'utilisation du modèle EMI suggéré dans le Chapitre 3 pour la conception des filtres d'entrée et de sortie CM et l'impact de l'ondulation de courant sur la conception des inductances de sortie a conduit à une prise de 22 % du poids global de l'onduleur (DPWM1) par rapport à celui montré au Chapitre 2 (voir ci-dessous la Figure 5).

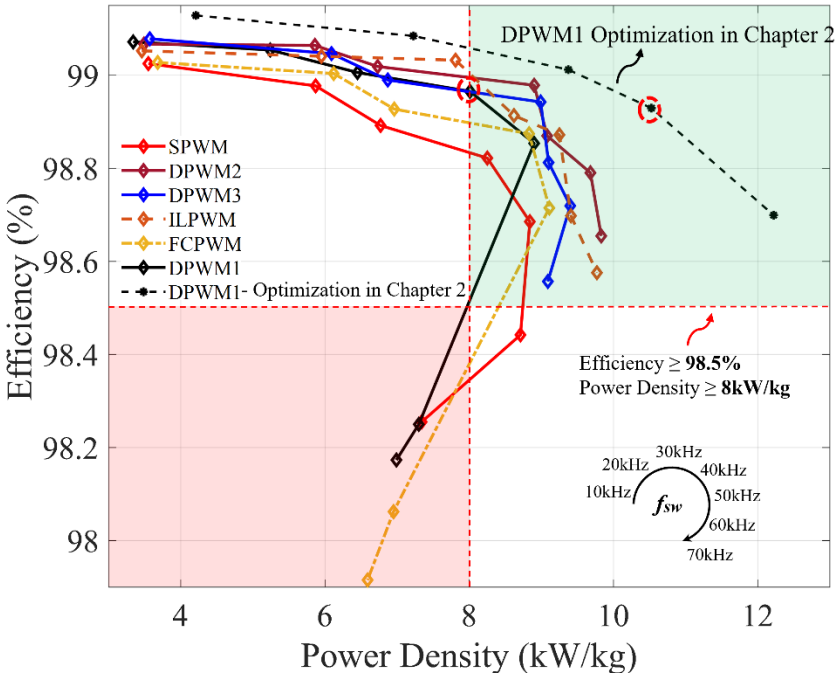


*Figure 5 – Résultats d'optimisation de la topologies 7 niveaux pour différentes techniques PWM et fréquences de découpages. Puissance nominale = 70 kVA, V_{bus} = 540 V, Index de Modulation = 0.9428 and décalage entre tension et courant = 36.67°.*Equation Chapter (Next) Section 1

Le Chapitre 5 aborde la réalisation de l'onduleur à partir des résultats obtenus dans le chapitre 4 pour une fréquence de découpage de 40 kHz et la technique DPWM3. L'onduleur est composé de 14 PCBs (9 bras FC, 1 carte mère, 1 filtre d'entrée, 1 filtre de sortie, 1 carte de contrôle et 1 carte de ventilateurs) et il est représenté dans la Figure 6.

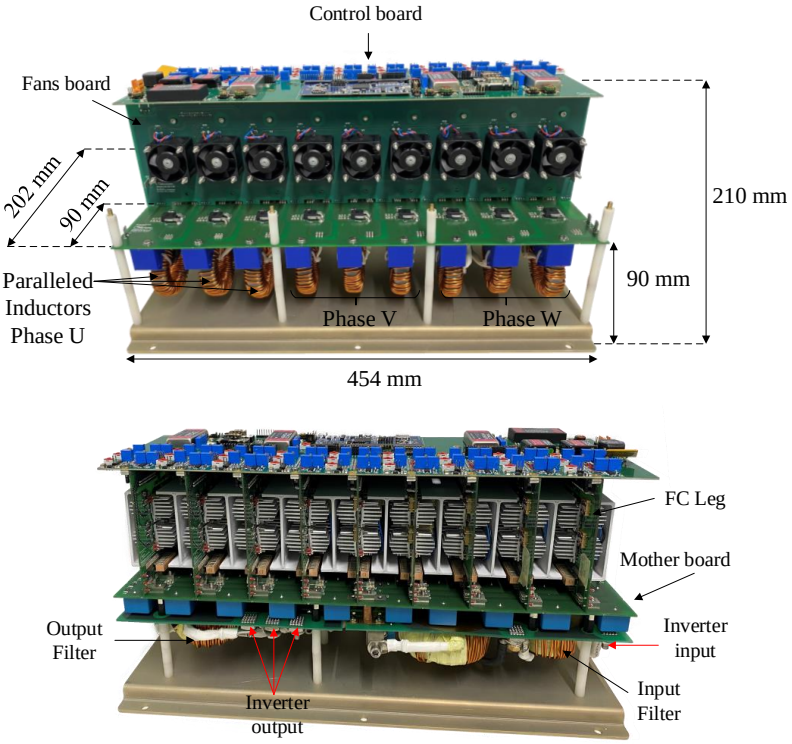
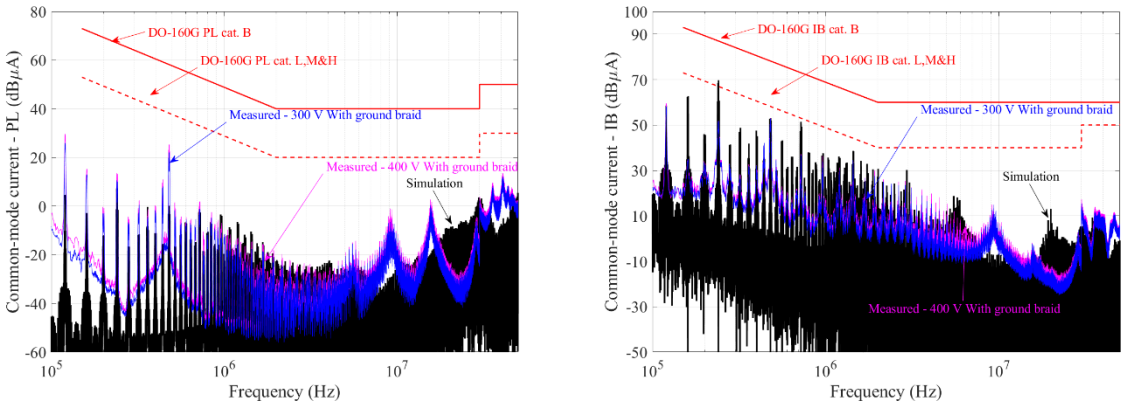


Figure 6 – Le prototype de l'onduleur 7 niveaux

Le convertisseur fait environ 10,04 kg et 14 litres. Sans la base métallique et la carte de contrôle, pièces non prises en compte lors de l'optimisation au chapitre 2 et au chapitre 4, il fait 8,35 kg. Le poids mesuré est supérieur de moins de 4 % compte tenu le poids calculé. Un convertisseur traditionnel de 2 niveaux utilisant 1200 V SiC Mosfet pour les mêmes conditions de fonctionnement doit être 74 % plus lourd que l'onduleur à 7 niveaux, avec une densité de puissance 43,4 % plus petite.

Ainsi, l'onduleur a atteint un rendement mesuré de 98,6 % à 24,6 kVA dans la validation expérimentale. En raison des courants circulants entre les bras en parallèle, des pertes supplémentaires sont ajoutées à l'onduleur ainsi qu'un déséquilibre de tension du condensateur flottant à courant élevé. Il compromet le fonctionnement en sécurité ce qui a limité le point de fonctionnement maximal à 500 V/38 kVA/87 A - fonctionnement nominal 70 kVA/130 A - avec un contrôle en boucle ouverte.

Des mesures d'émissions conduites ont été faites selon le RTCA/DO-160-G dans l'intention de valider le circuit équivalent CEM proposé au Chapitre 3. D'après les mesures, le modèle proposé offre une bonne correspondance jusqu'à 5 à 6 MHz pour PL et IB comme nous le voyons dans la Figure 7.



(a) Entrée *(b) Sortie*

Figure 8 - Mesures des émissions conduites (CE) de l'onduleur 7 niveaux, avec 10 mètres de câble non blindé et une charge RL.

De toute façon, une enquête plus approfondie doit être menée pour évaluer les différences en basse fréquence qui peuvent être liées à la connexion des radiateurs au plan de masse décrit dans la norme.
Enfin, en ce qui concerne l'originalité et les apports scientifiques des travaux présentés dans ce manuscrit de thèse, certaines considérations ressortent :

- L'optimisation d'un onduleur pour une application aéronautique dans une chaîne électromécanique, avec des modèles précis pour différentes topologies d'onduleur et différentes contraintes de conception, telles que CEM, stabilité du réseau et qualité de l'énergie, surtension et taux de distorsion harmonique de courant de sortie.

- La proposition d'un circuit équivalent en ligne de transmission bifilaire d'un câble triphasé pour estimer les niveaux de surtension dans les systèmes triphasés. Le modèle proposé a été vérifié expérimentalement pour différentes longueurs de câble dans une chaîne électromécanique réelle.

- La modélisation des sources de tension de mode commun pour les topologies d'onduleurs à plusieurs niveaux peut être utilisée pour estimer le courant de mode commun et aider la conception précise des filtres CEM. Il faut souligner que les modèles équivalents proposés ont été validés expérimentalement.

- La proposition de deux techniques PWM, basées sur l'injection de composants homopolaires, utilisées pour réduire le poids global d'un onduleur triphasé multiniveaux parallèle composé par des bras *Flying Capacitor*. La première technique vise à réduire l'ondulation de tension du condensateur flottant directement proportionnelle à son poids, tandis que la seconde vise à réduire le courant de crête vu par les inductances de sortie du convertisseur. L'ondulation du courant de sortie a un effet négligeable sur les pertes globales, de sorte que le facteur limitant des inducteurs de sortie s'avère être la saturation du noyau magnétique - directement proportionnelle au courant de crête de l'inducteur - qui détermine le poids de l'inducteur. La technique de réduction du poids du condensateur flottant a été =vérifiée expérimentalement, validant la méthodologie utilisée pour créer les deux techniques PWM proposées.

- La mise en parallèle de quatre transistors GaN dans une cellule de commutation *Flying Capacitor* et la généralisation du routage de cette solution pour augmenter le nombre de niveaux de sortie

pour la même topologie. Deux solutions de routage ont été conçues et vérifiées expérimentalement en termes de rendement, de vitesse de commutation et de surtension.

Différentes perspectives ont été identifiées au cours du projet de recherche qui pourraient contribuer à la conception prédictive des convertisseurs de puissance, ainsi qu'à augmenter le rendement des convertisseurs et la densité de puissance, comme présenté dans les sujets ci-dessous :

- Semi-conducteurs : l'avancée des nouvelles technologies des transistors WBG peut simplifier la conception et augmenter encore la densité de puissance de l'onduleur présenté en réduisant les nombres de composants.

- Technologies d'intégrations de PCBs : L'intégration de semi-conducteurs à l'intérieur du PCB est une technologie prometteuse pour réduire les boucles de commutations et augmenter les performances thermiques des cellules de commutations.

- La prédiction de surtensions : Malgré une estimation raisonnable de la surtension (erreur inférieure à 5%) et la validation expérimentale, le modèle propose est limité à un câble triphasé non blindé. Par conséquent, un modèle plus générique devrait être développé pour considérer les câbles non blindés et n conducteurs. De plus, ce modèle doit être inversé et il doit aussi représenter la forme d'onde de tension dans le domaine temporel sur les bornes de charge à n phases.

- Modélisation CEM : Le Chapitre 3 a abordé un circuit équivalent MC générique qui peut être utilisé sur des topologies multiniveaux. Cette méthodologie a été vérifiée expérimentalement pour un onduleur à 2 niveaux avec une réponse satisfaisante jusqu'à 20 MHz et un onduleur à 7 niveaux avec une réponse satisfaisante de 500 kHz à 6 MHz. Au-dèla les tests présentés, il serait nécessaire de mesurer les courants MC dans le domaine temporel et de les comparer avec le modèle proposé pour renforcer sa validité.

- Contrôle et commande : Afin d'augmenter la puissance de fonctionnement de l'onduleur proposé, il est nécessaire de mettre en œuvre un contrôle en boucle fermée pour limiter les courants de circulation et le déséquilibre de tension des condensateurs flottants.

CONTENTS

GENERAL INTRODUCTION

During the last decade, air traffic has increased by over 60%, responsible for 2% of the CO_2 emissions. In 2015, the global aircraft fleet consumed 276 million jet fuel tonnes, representing 7% of the global oil products. Despite aircraft efficiency increases (1% of fuel burn reduction), the aircraft fleet grows at around 4.5% annually. Looking at the net effect, it is estimated that aviation may produce around 24% of global CO_2 emissions by 2050. Even though a hypothetical acceleration of aircraft efficiency to around 2.65%, aviation could produce 19% of global CO_2 emissions by 2050.

Foreseeing this situation, some objectives were defined in the European Commission's Flightpath 2050 vision by giving the guidelines to foster clean, innovative, and competitive technologies that could significantly reduce air transport's environmental impact. Concerning the 2000 baseline, at 2050, a 75% reduction in CO_2 emissions, 90% reduction in NOx (oxides of nitrogen emissions), and 65% reduction in aircraft noise is expected.

Two significant factors drive the aviation industry's growth path over the last decade to attend the European Commission's Flightpath 2050 vision guidelines: sustainability and integration of underway technology. The first aims to make the growth in air traffic acceptable by decreasing its environmental impact. To reach environmental impact reduction, despite air traffic increasing, new aircraft designs and business models paved by new technologies must meet several expectations: increase mobility, resolve urban centers congestions, and satisfy the need for transportation in regions lacking road and rail networks. Both trends encouraged the increase of electrification of new aircraft. They raised the more electric aircraft (MEA) concept by replacing conventional non-propulsive hydraulic and pneumatic systems with their electric counterparts that are more compact, reliable, and flexible.

The development of an MEA increases high-power electrical loads, which are mainly motors being part of a power drive systems. These are composed of filters, power converters, cables, and electric motors. Power drive systems used in MEA are found in systems such as braking, air conditioning, electric taxing, etc. Moreover, to switch to MEA, the concerned electrical systems must have higher power densities than those currently used.

Breakthrough technologies are therefore necessary to drastically increase the power density of these systems. Wide band gap (WGB) semiconductors such as Silicon Carbide (SiC) and Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) have been the subject of extensive research to exploit their physical properties. Highly efficient converters have been reported under high temperatures with WBGs transistors due to their improved switching performance, leading to increased switching frequencies and loss reduction. Consequently, reducing the size of passive components and heat sinks. Nevertheless, WBGs may increase conducted and radiated electromagnetic emissions due to their high switching speed. Besides electromagnetic emissions, other domains are closely related to semiconductors switching speed, such as lightning protection, partial discharges, losses, and insulators aging. These phenomena require mastering multi-physical coupling models to propose practical solutions to guarantee MEA power drive systems safe operation.

The research work presented in this thesis was carried out through a collaboration between IRT Saint Exupéry and the Power Electronics and Integration group (EPI) of the laboratory SATIE. This thesis's primary goal is to identify and design a power inverter topology with filters included with a power density superior to 8 kW/kg and efficiency higher than 98.5% for the 70 kVA MEA power drive system application. Significant weight and volume savings in MEA power drive systems are possible by considering a global optimization of the entire system for a given thermal, electrical, and mechanical environment. Therefore, this thesis requires knowledge of the following areas: semiconductors, power converter, filter topologies, magnetic materials, electric motor and converter control, cables, and multi-physical modeling.

In this context, this thesis manuscript is divided into five chapters. The first chapter comprises the introduction, where the MEA context is presented as well as the power drive application considered in this thesis. The constraints and objectives imposed on a three-phase inverter in the EPowerDrive project are also presented. Multi-physical models necessary to evaluate the best inverter topology are described. Finally, the thesis contributions are listed at the end of this chapter.

Chapter 2 presents the state-of-the-art multi-physical models, semiconductors, inverter topologies, passive elements for filter design, cooling system, and pulse width modulation (PWM) techniques. Based on the state of art models, previous optimization results using Pareto front are presented, and one inverter solution with filters comprised that attend all constraints and objectives is presented. A seven-level inverter topology composed of three paralleled legs per phase of a three-level flying capacitor (FC) topology is presented as the optimal solution. Each FC leg switch comprises four 650V/60A GaN HEMTs in parallel, totalizing 144 transistors in the final inverter. Three research axes related to the presented inverter are identified and used to guide the final inverter's precise and robust design:

- Axis 1: Modeling of a common-mode voltage source for multilevel power converters and EMI filter repartition analysis considering the optimal inverter.

- Axis 2: Optimized Pulse Width Modulation Techniques to reduce output inductors and flying capacitors.

- Axis 3: Master the paralleling of four GaN HEMTs in a flying capacitor multilevel commutation cell by reducing and ensuring symmetry of power loop inductances.

Chapter 3, relating to axis 1, presents the modeling and experimental verification of common-mode current for two-level inverters and a multilevel converters model. It also verifies the best common-mode filter repartition (input and output) regarding filter weight and losses.

Chapter 4, relating to axis 2, evaluates two PWM techniques generated by an optimization algorithm to reduce output inductors and flying capacitors. The PWM technique to reduce flying capacitors was verified experimentally to validate the optimization algorithm. This chapter also evaluates different PWM techniques to reduce global inverter weight and increase its efficiency. From this study, the optimal solution is defined with all passive device values and design.

Chapter 5, divided into two major parts, presents the inverter design and experimental results. The first one is dedicated to axis 3, where simulation and experimentally two routing layouts are compared. The best one is selected to be implemented in the final converter. The second part of this chapter presents the final converter design and experimental results regarding inverter operation, efficiency, and conducted emissions according to RTCA/DO – 160G.

Finally, some perspectives are presented in the Conclusions and Perspectives section.

Touching the originality and the scientific contributions of the work presented in this thesis manuscript, stand out:

- Optimization of an MEA power drive system inverter with precise models for different inverter topologies and a large number of design constraints, such as EMI, Network Stability and Power Quality, Overvoltage, and THDi.

- Proposal for an equivalent circuit in a bifilar transmission line of a three-phase cable for estimating overvoltage in three-phase systems. The proposed model was verified experimentally for different cable lengths in a real power drive system.

- Modeling an equivalent common-mode voltage source for multilevel inverter topologies can be used to estimate common-mode current and assist the precise design of EMI filters. The proposed equivalent models were validated experimentally.

- Proposal of two PWM techniques, based on zero-sequence component injection, used to reduce the global weight of a multilevel parallel three-phase flying capacitor inverter. The first technique aims to reduce the flying capacitor's voltage ripple, directly proportional to its weight. While the second aims to reduce the peak current seen by the converter output inductors. The output current ripple has a negligible effect on overall losses, so the limiting factor of the output inductors turns out to be the magnetic core saturation (directly proportional to the inductor peak current) that determines the inductor's weight. The technique for reducing the flying capacitor's weight was verified experimentally, validating the methodology used to generate the two proposed PWM techniques.

- Paralleling of four GaN transistors in a multilevel flying capacitor commutation cell and the generalization of routing this solution for increasing the number of output levels for the same topology. Two routing solutions were designed and verified experimentally in terms of efficiency, switching speed, and overshoot.

CHAPTER 1

Aircraft Electrification and Power Electronics Challenges

THIS chapter introduces the context of the present thesis subject. Aircraft electrification subject is introduced as the concept of More Electric Aircraft. Next, the role of efficient and compact power drive systems applications on aircraft is presented. After that, EPowerdrive project objectives and design constraints that orientate this thesis work are shown. The necessary multi-physical models are identified according to the state-of-the-art to achieve project design objectives. Finally, this thesis's contributions are highlighted, such as multi-physical model improvements, propositions, and technological solutions.

Summary

1.1 More Electric Aircraft

1.1.1 History of aircraft electrification

Electric aircraft are considered a futuristic transportation facility. However, the first flying machine electrically powered first flew in 1883 with Gaston Tissandier, seventeen years before the Wright Brothers flight at Kitty Hawk. Charles Renard and Arthur Krebs used a more powerful motor to another airship in 1884. However, the airship suffered from a lack of performance due to its weight [1]. Nearly ninety years after Tissandier, Heino Brditschka flew roughly 300m above the ground for around nine minutes with an electric motor powered by a pack of nickel-cadmium (NiCad) batteries that generated 100V [2]. Several projects were developed using solar-powered aircraft associated with batteries in the following years, as the QinetiQ Zephyr set an endurance of 336hours in 2010. The most noteworthy feats of a solar-powered aircraft, Solar Impulse II, flew 26 000 miles to promote clean technologies [2].

Aviation was driven to use oil derivative compounds due to the internal combustion engine and the gas turbine's subsequent invention. However, the 20th Century scales up in the electrification of all human activity. The first limiting factor for electric aircraft was battery weight, which redirects many experimental and research designs to electrical propulsion systems. The light aircraft market was a good starting point to test systems, prove electric aviation viability, and other technology.

In the aviation domain, this electrification was driven in two strands [1]:

- More Electric Aircraft (MEA) is considered an evolutionary trend in which each successive generation of aircraft employs more electrical equipment in mechanical, hydraulic, or pneumatic systems.

- Electrical Propulsion – a potentially revolutionary new approach that may lead to new aircraft architectures by affecting aircraft propulsion and all aircraft systems.

In the 1940s, the Boeing B-29 Superfortress had relatively high electrification levels, including landing gear actuation. However, the use of electrical systems for non-propulsive commercial aircraft did not appear until 1967. This year, the first Boeing 737 flight introduced the first electrical cabin and avionics, representing the concept of the MEA. Another aircraft electrification milestone introduced the “Fly by Wire” system in the Airbus A320 in the 1980s, followed by the Boeing 777 in 1994. This technology allowed electrical transmissions of instructions from the cockpit to the flight control surfaces, eliminating the need for mechanical linkages and significantly providing weight reduction and space release [1].

The next big step towards the MEA concept came with the Airbus A380 by implementation of electrically actuated thrust and hybrid electro-hydraulic actuation systems for wing and tail flight control surfaces. After that was the Boeing 787 with an electrically powered air-conditioning system, electrically actuated brakes, and de-icing. When it comes to the military domain, the F-35 presents a fully hybrid electro-hydraulic actuation system and a high voltage direct current electrical distribution

system that allows weight reduction and high electrical power generation capacity. This electrical generating capacity is also verified in the Boeing 787[1][3][4].

1.1.2 Evolution to the MEA

Traditionally, aircraft non-propulsive energy systems represent around 5% of the engine's output power of the A330 aircraft [2], as presented in Figure 1. Three engine options are available, from Rolls Royce, Pratt & Whitney, and General Electric

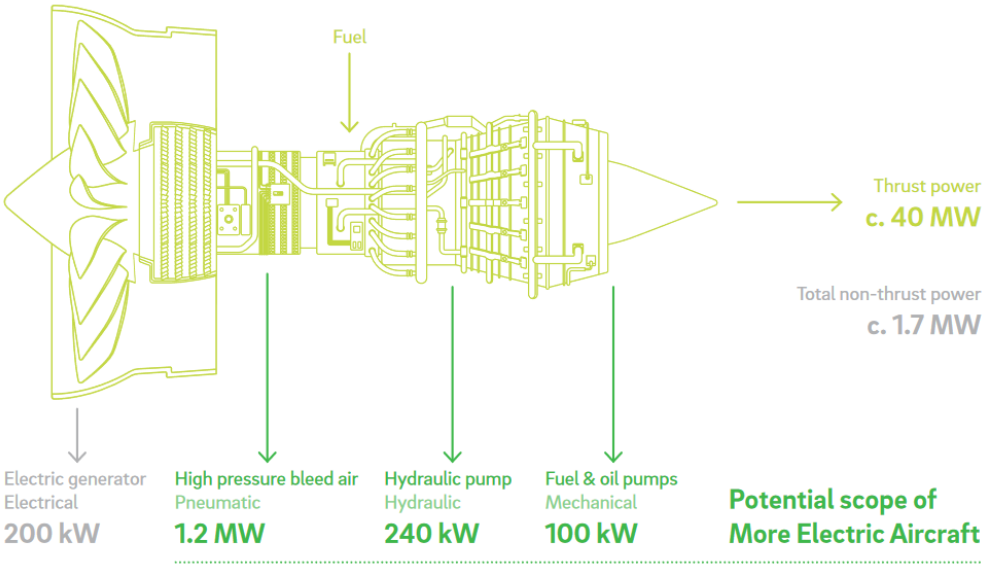


Figure 1 - Engine Power Output for A330 – Sized Aircraft [1].

These non-propulsive energies installed systems are divided as listed below [5], [6]:

Mechanic - Most mechanical energy is used in the engine's systems, fuel, and oil pumps motioned by the engine itself. It represents around 0.25% of the A330 engine's total output power.

Hydraulic – It represents the energy transported as a pressurized liquid to motion other systems. A pump driven by the engine does the liquid pressurization, representing 0.58% of the A330 engine's total output power. Hydraulic systems are robust and can generate enormous forces, but they have often suffered from a lack of reliability and high maintenance costs. Some loads using hydraulic energy are:

- Flight Control: They are divided into two categories, primary and secondary flight control. The primary changes the orientation of the aircraft around its center of gravity. The secondary flight control allows the modification of the lift and drag forces applied to the aircraft.

- Landing Gear System: It ensures the aircraft's taxi and braking operation on the ground. The Nose Landing Gear ensures the aircraft's direction, and the Main Landing Gear supports the significant aircraft weight on the ground. The breaks are located on the Main Landing Gear.

Pneumatic – It represents the energy transported as compressed air into aircraft and distributed through the aircraft by the pneumatic network, named Bleed Network. Hot air is taken from the engine's compressor stages for the bleed network before fuel is added. Pneumatic systems power consumption represents around 2.9% of 5% of engine total output power used for non-propulsion systems. Most pneumatic systems have the drawbacks of low efficiency and like hydraulic systems, miles of complex and heavy pipes, and ducting running throughout the aircraft. They are often challenging to locate and sometimes hard to trace, and time-consuming to repair. Any interruption in operation may ground the aircraft, generating extra cost and inconvenience for operators and passengers. The main loads consuming pneumatic energy are:

- Environmental Control System (ECS): It keeps the air inside the cabin at sufficient pressure and temperature for passengers at high altitudes. The air is taken from compressors then injected into the ECS system. This air is treated via a compressor assembly and Bleed Network, making it possible to control air flow thermodynamic properties.

- Wing Ice Protection System (WIPS): This system prevents ice formation on the wings and engine's nacelles. It is imperative to avoid ice on the wings because, besides the additional weight, the ice modifies the wing's aerodynamic profile.

- Motor Starting: The motor start-up is performed by a turbine working with hot air injection from the Auxiliary Power Unit (APU).

Electric – Electric systems receive power via a mechanical transition through the engine gearbox to an electric generator. These systems do not suffer from many shortcomings in the hydraulic, pneumatic, and mechanical systems. Electrical systems are relatively flexible, light, and have higher efficiency. They consume around 0.48% of the engine total output power of the A330. The electrical loads on the current state-of-the-art civil aircraft are:

- Fuel pumps: They transport the fuel from the tanks to the engines.

- Anti-icing system for cockpit: Ensure good visibility for the pilots (Windshield Systems).

- The ventilation system of the ECS: Includes all fans for hot air extraction and ventilation.

- Avionics: Calculators and instrumentation installed on the aircraft.

- Cabin Systems: It includes all necessary electrical systems for the aircraft cabin, such as galleys, lighting, and passenger comfort systems (entertainment, etc.). These systems depend on aircraft configuration and airline choices.

Load diversity on some state-of-the-art commercial aircraft is presented in Figure 2. Many aircraft now employ electric systems and/or a mix of hydraulic and electrical systems. The transition to a fully electric aircraft is ideally the goal since its theoretical efficiency would reach 100%. Even though a fully electric aircraft results in a 97% electrical efficiency due to resistive heating, it is still far more efficient than combustion engines, which may present an ideal 70% thermal efficiency [7]. However, a fully electric aircraft idea comes up against energy storage systems limitations (batteries). Batteries have in the order of 50 times lower specific energy than liquid fuels [7]. Lithium-ion batteries present around 250 Wh/kg [8] while Jet-A fuel has 11900 Wh/kg [9], and they will reach, theoretically, near 400-1000 Wh/kg for advanced concepts [10]. The comparison between Jet fuel and Lithium-Ion batteries showed in [11] presents that the last one has a much lower volumetric energy density than Jet fuel.

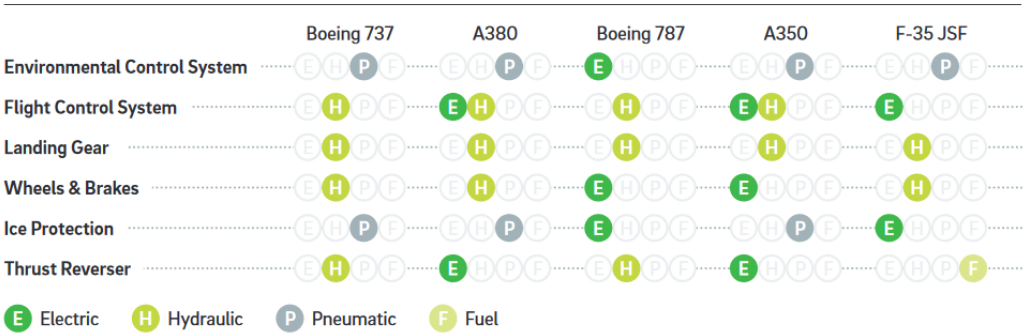


Figure 2 - Penetration of electrical systems by aircraft type. Source: Airbus, Boeing, Lockheed Martin, and Roland Berger [1].

In this way, many aircraft manufacturers decided to adopt an intermediate step, the MEA concept for large aircraft, to increase aircraft profitability and respond to environmental constraints. The main gains by replacing pneumatic and hydraulic systems with their electrical correspondents are listed by [6], as:

- *Easier Energy Management:* efficient management of the engine's energy is easier since there is only one energy vector on the aircraft.

- *Weight saving:* electrical systems are systematically smaller and lighter than pneumatic and hydraulic ones.

- *Protection:* electric failures due to segregation and isolation are more superficial and faster than other systems, such as fluid leakage on an aircraft pipe.

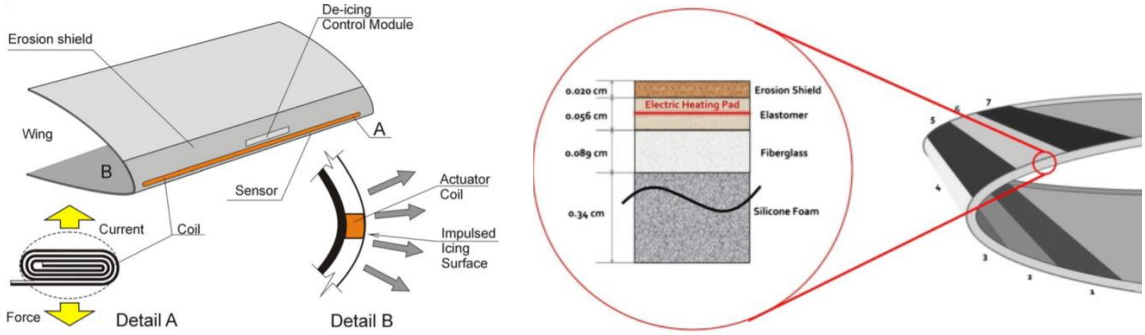
- *Maintenance:* electrical systems are easily monitored. As a consequence, the failure is more easily detected, and it reduces maintenance time and costs.

- *Synergy:* Different Industrial sectors are pushing towards developing cheaper, more efficient, integrated, and robust electric equipment. This synergy reduces equipment costs due to a more significant market, like automotive and energy domains.

Hydraulic-less and Bleed-less architectures match the corresponding electric systems that substitute hydraulic and pneumatic systems, respectively. The use of both architectures leads towards a fully electric aircraft where all non-propulsive systems become electric. The Bleed-less is considered more affordable technologically than the Hydraulic-less, and it corresponds recently to the most contemplated architecture. Some pneumatic systems that have been electrified on the Boeing 787 are presented in [13] and [14] and are listed below:

- *Main Engine Start*: The use of main engine generators as electrical motors to perform engine staring functions. In traditional aircraft, the engines are started by a turbine driven by compressed air provided by the Auxiliary Power Unit (APU).

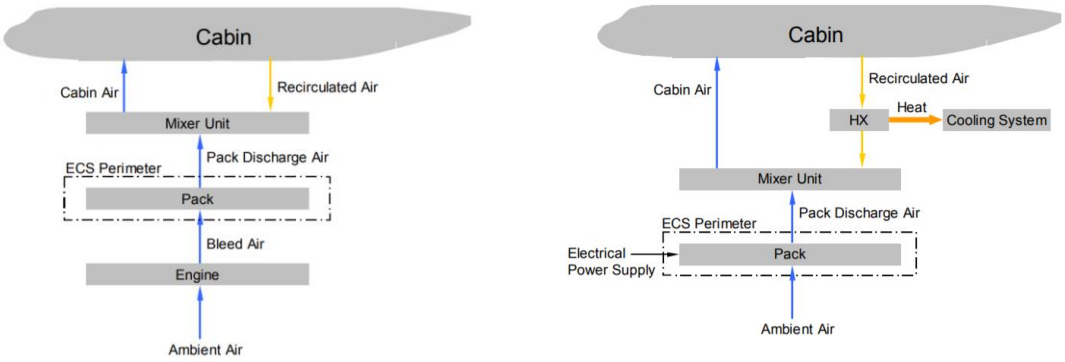
- *Electrical Wing Ice Protection System (eWIPS)*: Two solutions can be used to prevent or eliminate ice creation on the aircraft wings, as shown in Figure 3. The first one, called electromechanical solution, consists of using electromagnetic devices to produce mechanical vibrations to eliminate the ice. The second consists on placing electric wires on the wing surface. The heat dissipated by the Joule effect melts the ice. This solution is also called electro-thermal and removes the need to bleed hot air extracted from the engine, which is the traditional approach to protect against in-flight icing.



a) Electro-mechanical [14] *b) Electro - thermal* [15]

Figure 3 - Electrical Wing Ice Protection System.

- *Environmental Control System (eECS)*: Air is taken from the outside and compressed using electric power. The main engine's bleed air is used for the ECS in traditional aircraft, as shown in Figure 4.



a) Bleed – Pneumatic *b) Electrical*

Figure 4 - Environmental Control System [16].

The electrification tendency of different aircraft systems translates naturally to an increase of aircraft embedded electrical power. According to Figure 5, the Airbus 380 has 600kVA on board installed power, while the Boeing 787 presents more than 1 MVA. In [3], it is estimated that an MEA will have 1.6MVA minimum electrical power for a 300 passengers aircraft.

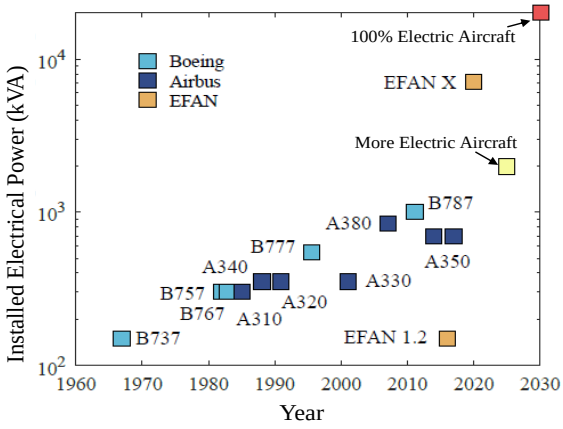


Figure 5 - Evolution of aircraft on board electrical power [17].

1.1.3 MEA Power Generation and Distribution

The increase of electric energy distribution on typical aircraft is fundamentally based on one or more levels of the voltages listed below [4]:

a) 28 V DC – low power loads and small aircraft;
b) 270 V DC (± 135 V) – military aircraft;
c) 115 V AC at 400Hz – civil aircraft.

The increase of aircraft embedded power created a new challenge. In order to not increase cable weight, it was necessary to rethink the aircraft's electric distribution system. Two leading solutions were proposed based on limiting the current level by increasing the network voltage[18].

First Solution: Based on the conversion of the aircraft alternative network, the 115 V AC phase-to-neutral at a variable frequency from 360 Hz to 800 Hz was switched to a 230 V AC at 400 Hz or variable frequency distribution, named HVAC (High Voltage Alternative Current). This architecture is already implemented on the Airbus A350 and Boeing 787, as presented in Figure 6. This last one uses a 28 V DC network for loads such as avionics [19].

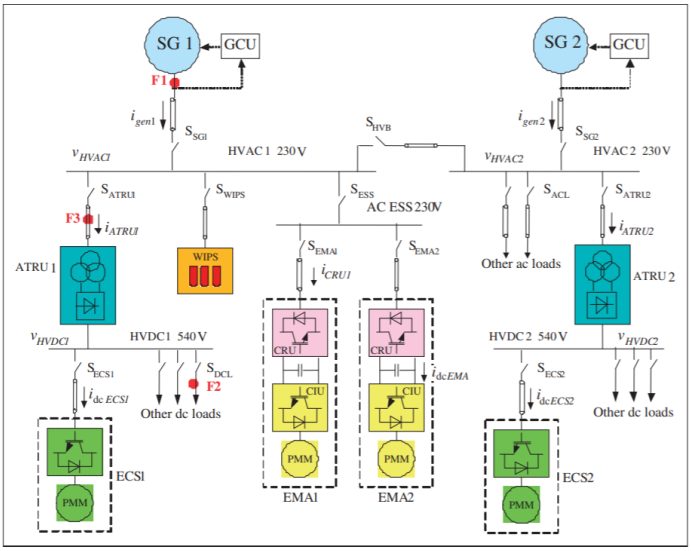


Figure 6 - Boeing 787 power system with AC and DC busses [4].

Second Solution: This architecture switches to a continuous high voltage distribution known as HVDC (High Voltage Direct Current). A differential voltage level of 540 V DC or +/- 270 V DC. The main advantage is that HVDC removes all rectifier stages inserted before loads that incorporate inverters, like motors and electric flight controls. This solution is presented in [20] as a lighter distribution architecture compared to the others. Promising flight tests were carried out in 2016 on an ATR 72-600 (see Figure 7) and an Airbus A320 with these architectures as part of the European Clean Sky project [17]. Nevertheless, HVDC distribution may generate quality problems and network instabilities, as reported in [10] and [11].

Figure 7 - ATR 72-600 prototype testing aircraft (Clean Sky Project).

The change to an MEA significantly increases the electrical power demanded by the aircraft, going from 100 - 200 kW to over 1 MW for a civilian aircraft [4]. This increase in power requirement from the generation system encouraged several developments to make it more competitive and reliable. Generation systems are classified as CSCF (Constant Speed/Constant Frequency) and VSVF (Variable Speed/Variable Frequency) [20], their main characteristics are listed below:

- *CSCF*: The generator is connected to the engine through a Constant Speed Drive (CSD) gearbox, as shown in Figure 8. This equipment creates a constant speed shaft from the variable input speed. Therefore, the electrical frequency is fixed mostly at 400Hz. The main disadvantages of this architecture are the high cost and weight of the gear box.

- *VSVF*: In this architecture, the generator is directly connected to the engine, according to Figure 8. In that case, the bus frequency changes with the engine speed, around 320 to 800 Hz. A more reliable and straightforward generation configuration is achieved with this architecture. Nevertheless, most aircraft loads will require power converters to control the variable frequency, which already exists to control failures and remove the electrical system's loads. In that case, as the power converters can be placed close to the loads, it may allow a better aircraft weight distribution.

Beyond the traditional CSCF and VSVF systems listed above, two other architectures based on the VSVF, Figure 8, are also relevant to be pointed out: DC Link and VSCF (Variable Speed Constant Frequency):

- *DC Link*: This solution is being exhaustively studied to be implemented in the next generation of aircraft. In that case, the VSVF generator's output is connected to a power rectifier to form a DC Link (Ex: 540V), where DC/DC and DC/AC converters will be connected to supply aircraft loads.

- *VSCF*: In this architecture, the VSVF generator output is connected to an AC/AC or AC/DC – DC/AC converter that guarantees constant output frequency. This topology is applied in Boeing 737 and Airbus A340.

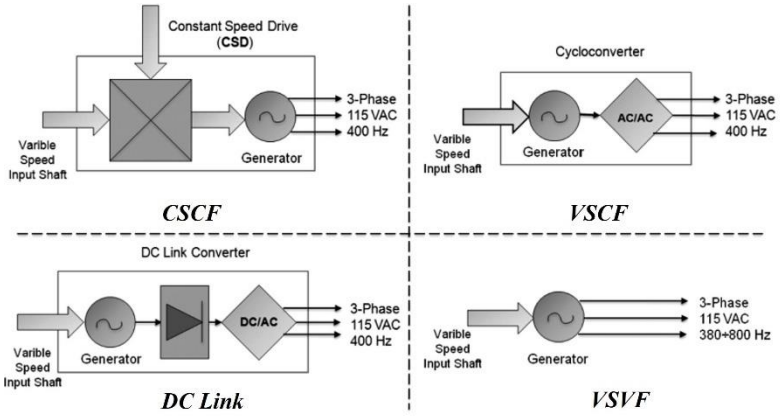


Figure 8 - Electric Power Generation of state-of-the-art civilian aircraft[23]

Nowadays, there is an effort to use the HVAC 230 V generators (Airbus A350 and Boeing 787) and classical diode rectifier stages to lead to the 540 V HVDC network explained before (DC Link generation architecture). A classic electric system with different loads connected to the HVDC through inverters is presented in Figure 9 (a). The aircraft manufacturers presented a new electric architecture concept that uses power cabinets to centralize modular power electronics modules to achieve even more weight savings of the overall electrical system [5] [6]. These power cabinets are connected to a HVDC bus while the loads are connected to the power cabinets bus. Loads have different profiles, allowing all modules connected to the power cabinet to be placed in parallel and share the necessary power, as shown in Figure 9 (b). Therefore, the power module is not designed for a specific load and can be generalized, reducing power converter cost [24]. This architecture also offers redundancy and reconfiguration modes, which supply loads on degraded mode or even isolate the defective load. However, this architecture's main drawback, where power converters are centralized and shared, is that they are not located in the same place. Therefore, power cabinets and loads will be connected through long cables and may increase electromagnetic disturbances.

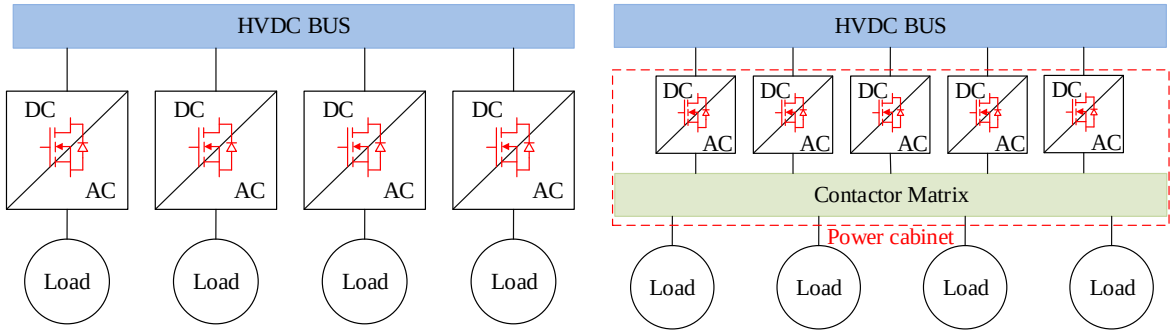


Figure 9 - MEA electrical systems.

Voltage range and types used in different aircraft are presented in Figure 10, showing the convergence to the HVDC architecture for the future MEA. In the 2000s, A DC link was one encouraging solution. However, with the aircraft's growing power demands, medium voltage HVDC is being considered, passing from 540 V to 1000 V or even 3000 V [24] [25].

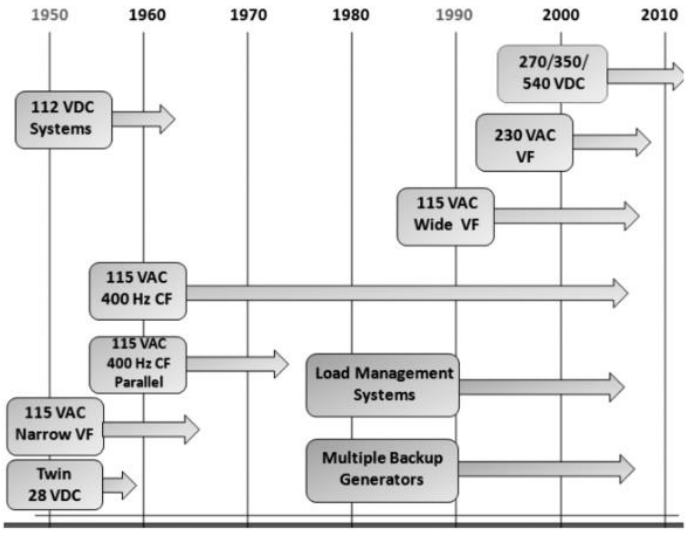


Figure 10 - The evolution of aircraft electric network [23].

1.2 Aircraft Power Drive Systems

Many electric loads that substitute pneumatic and hydraulic systems are power drive systems. These loads can represent air conditioning, pressurization, landing gear, de-icing, ventilation systems, etc. A power drive system connected to a HVDC network comprises four elements as shown in Figure 11: an inverter, input and output filters, power cables, and the load, which is usually an electric motor.

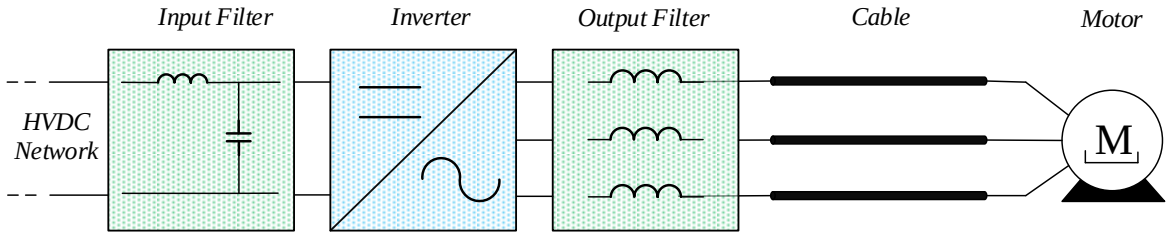


Figure 11 - MEA power drive system.

Cable length is determined by aircraft manufactures according to the application and aircraft integration. It may comprise between 0 and 20 m, as identified by [17]. Cables characteristics substantially affect electromagnetic interference (EMI), whether it is related to conducted or radiated emissions [27]. Another phenomenon directly related to cable characteristics on power drive systems is the overvoltage on motor terminals [25] [26], which may reduce the motor's electrical insulation lifetime and cause partial discharges and breakdown. This phenomenon is even more evident considering aeronautical constraints, such as low pressure and the new HVDC distribution system.

Electric motor is a key component in any power drive system, especially in the aircraft domain, where reliability and power density requirements are prioritized. Excluding electric generators and focusing only on actuators, engine pumps, and landing gear, three electric motor technologies are commonly considered for aircraft applications: Induction Motors (IM), Reluctance Motors (RM), and Permanent Magnet Synchronous Motors (PMSM). This last one dominates aircraft research and development since it offers the smallest actuator solution among other technologies [30]. Recent studies show Permanent Magnet Synchronous Motors (PMSM) gravimetric power densities going from 1.4 kW/kg to 6 kW/kg for MEA applications [29]–[32]. The weight on board the aircraft is related to CO_2 emissions, 1 kg in each flight is responsible for 5.4 tons of CO_2 emitted per year from world air traffic [28] [29]. Therefore, the reduction of power drive systems weight is critical to reducing CO_2 emissions.

Inverters must control and interface the power flowing from the HVDC network to the load. These inverters can be designed from 1 kW to few hundreds of kW, and input/output filters must be designed to reduce global inverter weight, and consequently, increase the entire power density. Recent research shows that inverter topologies substantially impact filter weight, increasing filter power density from 5.3 kW/kg to 7.9 kW/kg passing from a 2-level to a 3-level inverter topology [32]. Increasing inverter output voltage levels also increases system efficiency by ≈ 33% [32]. Table 1 presents the state-of-the-art of recent three-phase power converters and their gravimetric power density for MEA applications. It goes from 2.79 kW/kg to 6.99 kW/kg for low voltage HVDC, reinforcing the interest of reducing inverters weight. It also shows a 22 kW/kg power converter designed considering a medium voltage HVDC bus, a 26 kW/kg two-level converter with liquid cooling, and a two-level SiC-based converter that claims 50 kW/kg without any filter. Works presented in Table 1 focus on specific objectives, often the design of the converter without the filters, or only with EMI filters or low-

frequency output filters. Alternatively, some works considers liquid cooling system, which makes one represents a significant theoretical increase in the inverter power density. It reinforces the essentiality of a design with several criteria applied in a real converter used in aircraft to represent a feasible solution with the available technologies.

Table 1 - MEA Power Drive systems gravimetric power density state-of-art.

Topology	Application	Power Density	Efficiency	Reference
2 - Level	48 kW 3-phase inverter	3.15 kW/kg	-	[33]
2 - Level	70kW 3-phase inverter	4.1 kW/kg	-	[34]
2 - Level	50 kVA 3-phase inverter	6.49 kW/kg (no EMI filter)	97.7%	[35]
3-Level	45 kW 3-phase bidirectional DC/AC	5.2 kW/kg	98.5%	[32]
2 - Level		3.9 kW/kg	98.2%	
2 - Level	60 kW 3-3-phase inverter	6.99 kW/kg (no EMI filter, excludes the weight of dc-dc balancer circuit)	≈ 95%	[36]
3-Level		4.92 kW/kg (no EMI filter)		
3-Level		5.81 kW/kg (no EMI filter)		
3-Level	60kW 3-phase back-to-back converter	2.79 kW/kg (no EMI filter)	≈ 95%	[37]
2 - Level	45kW 3-phase multicell converter	22.8 kW/kg (Medium Voltage Application and no EMI filter)	≈ 99%	[25]
2 - Level	50 kW 3-phase inverter	26 kW/kg (no EMI filters included and liquid cooled)	≈ 98.7%	[38]
2 - Level	35 kW 3-phase inverter	50 kW/kg (no filters included)	≈ 98.6%	[39]

1.3 EPowerdrive Project

France benefits from a strong base of skills around the aeronautics, rail, and automotive industries, ranging from component manufacturers, equipment manufacturers, and integrators. However, it suffers from a delay in the manufacturing, in the knowledge and use of Wide bandgap (WBG) semiconductors, directly impacting electromagnetic compatibility, cooling technologies, and actuators driven by these new devices.

The EPowerDrive project was created in 2017 to enable the French industrial and academic communities to improve their knowledge in using SiC and GaN power components and their integration into high power converters. It also makes it possible to optimize technological bricks' design and evaluate these new concepts performance compared to old technologies. The main and ambitious objectives of the EPowerdrive project are listed below:

- Develop methodologies, models, specification tools for each brick aiming for the overall optimization of a power drive system to increase efficiency, power density, and reliability (control, electromagnetic compatibility, filters, power electronics, cables, motor) but also compliance with current standards and network stability;
- Characterize, evaluate emerging SiC and GaN semiconductor components;
- Characterize/develop technological building blocks for the power drive system using WBG components (topology, control, filters, cables, cooling, motors, etc.)
- Develop technological demonstrators,
- Test all the work on a representative power drive system in order to assess its performance.

EPowerdrive project comprises academic and industrial members presented in Figure 12. It is organized in five work packages (WP) in a V cycle, as shown in Figure 13.

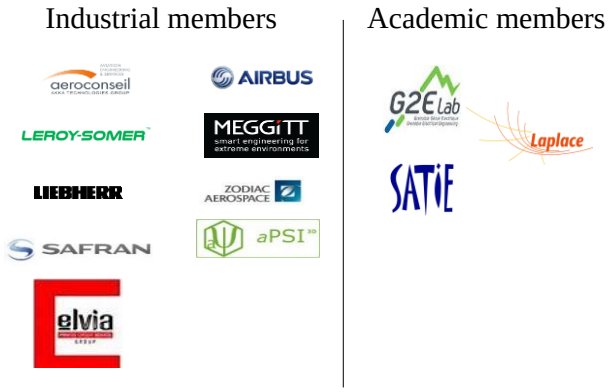


Figure 12 - EPowerdrive project members .

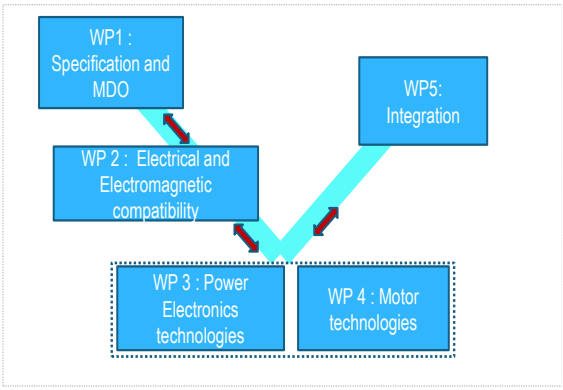


Figure 13 - EPowerdrive project research axes.

The top-down phase WP1 considers project member's requirements and specifies the needs in terms of tools, models, and then synthesizes the developed models in the Multi-objective Design Optimization (MDO) approach. WP 2-4 are responsible for developing the models and demonstrators, considering the electrical and electromagnetic compatibility requirements listed by WP1. WP5 is responsible for integrating all developed bricks (power converters, motors, filters, etc.) by WP2-4 in a power drive system and experimentally validate their overall performance.

The present thesis comprises the interests and objectives of WP 2 and 3 that concern the predictive design and realization of a high power density 70 kVA DC – AC converter that meets the objectives presented in Section 1.3.1 and comply with MEA environment constraints listed in Section 1.3.2.

1.3.1 Thesis objectives

This thesis was developed to pursue the general objective set by the EPowerdrive project. In contrast, the specific objectives were identified, aiming at the academic and technological contribution in the accurate design of power converters for the future MEA.

- *General Objective*: Identify and design a DC – AC converter with gravimetric power density superior to 8 kW/kg (filters and the cooling system included) and efficiency higher than 98.5% for a 70 kVA MEA power drive system. The inverter solution must comprise design constraints presented in Section 1.3.2.

- *Specific Objectives*:

  a) Identify and improve the multi-physics models to estimate common-mode currents, overvoltage at motor terminal, semiconductor losses to allow a predictive design of the inverter and filters with an accurate estimation of losses and weight;

  b) Evaluate the use of WBG semiconductors technologies and multilevel converter topologies;

  c) Evaluate filter topologies and common-mode filter distribution in the converter;

  d) Verify the possibility of weight reduction of passive inverter elements through Pulse Width Modulation (PWM) techniques;

  e) Experimentally evaluate compliance with Section 1.3.2 constraints, such as inverter overall weight and efficiency.

1.3.2 DC – AC converter design constraints

The study and design of the DC – AC converter must follow the guidelines raised by EPowerdrive WP1 listed below:

- HVDC bus rated voltage: 540 V;
- Inverter input voltage ripple of 5% of nominal HVDC bus voltage = 27 V;
- Airbus HVDC Power Quality Standard (0 – 150kHz) for inverter input voltage and current ripples;
- Maximum overvoltage on motor terminals: 750 V/850 V/1000 V;
- Output current total harmonic distortion (THD_i): 5%/7%/10%;
- Conducted Emissions RTCA/DO-160G Standard (150 kHz – 152 MHz) – Load Category L, M, and H. Power Lines limits and Interconnecting Bundles limits must be considered in the inverter input and output, respectively;
- Conducted Emissions are mainly due to common-mode currents;
- Common-mode filter capacitance maximum value of 150 nF (WF5A - impedance 100Ω at 10kHz usually considered for calculators) due to lightning current limit;
- Forced air cooling;
- Fixed unshielded aeronautic cable - 3AWG EN4681-006-AZA (10 meters long);
- 50 kW/70 kVA three-phase permanent magnet synchronous motor;
- Motor nominal operation point: 3600 rpm/132 N.m/70 kVA kW/130 A_{rms};
- Room temperature: 70°C;
- Passive filters only.

1.4 Necessary models for the DC- AC converter design

A power converter design to meet aircraft constraints described in the previous sections consists of a multi-physical coupled problem. According to the phenomenon to be represented, different models must be used for a predictive design of a power converter. A compromise must be identified between the multi-physical models and the manufacturer's available information in the different devices datasheets, such as semiconductors, magnetic cores, capacitors, fans, etc. These devices behavior and physical characteristics are essential for a reliable representation of the phenomena. In this context, seven different design bricks are identified in Figure 14 to be necessary for a precise predictive design of the power converter, they are:

1. *Multilevel Inverter Modelling*: the mathematical representation of different converter topologies, as the traditional two-level, multilevel series, and parallel is necessary. This representation must estimate the converter's output voltage waveform and its input current in the time domain. It is also necessary to know each component's current, whether it is an active component such as semiconductors or passive devices such as floating capacitors or output inductors.

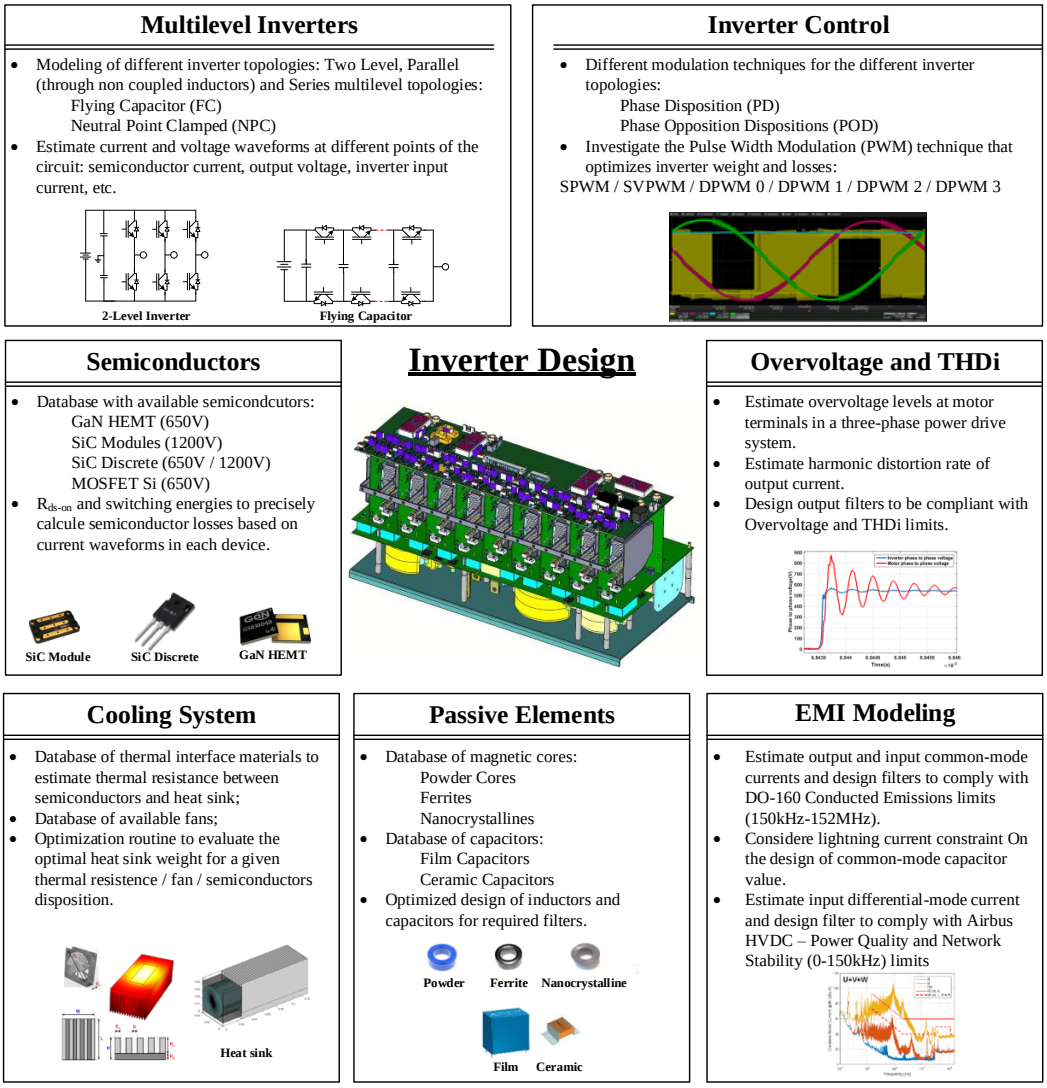


Figure 14 - Power converter necessary multi-physics models for a predictive design.

2. *Inverter control*: The mathematical representation of different converter topologies must consider different PWM techniques, with different carrier generation techniques such as Phase Disposition (PD) and Phase Opposition Disposition (POD). PWM techniques substantially impact passive element design and semiconductors losses, so different PWM techniques should be evaluated to improve converter gravimetric power density.

3. *Semiconductors*: Power converter losses are mainly due to semiconductors losses. An accurate estimation of semiconductor losses should consider each device's characteristics, such as turn-on and turn-off energies for each current level and temperature, as well as the drain-source resistance, in the case of GaN HEMTs and Metal Oxide Filed Effect Transistors (MOSFETs). A static and dynamic characterization of each device would be the ideal solution. However, this predictive study will stick to the information provided by the manufacturers in the datasheets. A database with the most recent components was considered to evaluate the different semiconductor technologies containing GaN HEMTs, Si (Silicon) MOSFETs, and SiC (Silicon Carbide) MOSFETs.

4. *Cooling system*: The direct impact of semiconductor losses is seen on converter losses, but its secondary impact is on the cooling system, which may have a significant impact on converter weight. Therefore, cooling system weight estimation is one of the critical parameters to increase converter power density. The thermal interface material (TIM) isolates semiconductors and the heat sink, and fans consider the manufacturer's datasheet information. For the heat sink, cooling system third component, an optimization routine is considered to estimate overall weight based on the thermal resistance required by semiconductors to guarantee a given junction temperature. Cooling system optimization routine considers different physical parameters, such as base plate thickness, heat sink length, width, and the number of fans.

5. *Passive devices*: This thesis will consider only passive filters, which means that the filters will be composed of inductors, capacitors, and resistors. Each phenomenon limited by filters requires different specificities, such as low parasitic or current level for capacitors, and keep its characteristics at high frequency for magnetic cores used for inductors. Optimization routines were developed to design capacitors and inductors required to filter each phenomenon, such as EMI, overvoltage at the motor terminals, and current ripple at the converter input and output currents. Each optimization routine is based on a database of different technologies, such as film and ceramic capacitors and iron powder, ferrite, and monocrystalline magnetic cores. These routines allow passive devices to be designed with their behavior close to the real application's expectations. Also, a precise estimation of these elements weight is possible since they are based on the market components.

6. *EMI Modelling*: Common-mode current is responsible for conducted emissions that may cause electromagnetic interference (EMI) on MEA systems. This current comes from the path formed by the parasitic capacitances of cables, semiconductors, and electric motor to a reference plane (the chassis, for example). To respect the limits imposed by the aircraft standard RTCA/DO-160G (only Conducted Emissions are considered), filters are used in the converter's input and output. Nevertheless, as this phenomenon occurs in high-frequency current components (150 kHz-152 MHz), it is essential to understand high-frequency behavior and couplings between the different parts that compose the power drive system. Since the inverter is connected to a HVDC bus, it must also respect low-frequency limits to avoid network instability and power quality issues. Airbus HVDC standard limits inverter input current and voltage ripples between 0 Hz – 150 kHz. Therefore, filters can be designed based on the

Passive devices brick from inverter common-mode current and input differential-current to comply with standard limits.

7. *Overvoltage and THD_i*: Two constraints were imposed to guarantee electric motor protection and reliability. Overvoltage on motor terminals combined with low pressure and high temperature (aircraft application) can be fatal for motor electrical insulation, where partial discharges shall reduce its lifetime. This phenomenon is mainly due to inverter output voltage transient associated with cable input and output impedance mismatch that may cause propagation and reflection phenomena along with the harness. Based on semiconductor switching speed, harness characteristics, and motor differential mode impedance, overvoltage on motor terminals should be limited by using passive filters (using *Passive devices* brick) in the inverter's output close to the electric motor. This filter shall also limit current total harmonic distortion (THD_i) injected in the electric motor to limit motor heating due to iron (hysteresis and eddy current) and copper losses. This overheating can reduce motor efficiency and shorten motor lifetime. Besides, the harmonic injection may also affect torque and increase mechanical vibration and load noises.

Complete optimization of a power converter must consider issues, requirements and objectives other than those described above. Cost, reliability and robustness, modularity, and integration are as important factors as those listed. However, the work developed in this thesis adheres to the axes described in Figure 14.

1.5 Chapter Conclusions

The electrification of transportation is a challenging reality that has taken over the scene over the years. The socio-environmental impact of burning fossil fuels and their future scarcity guided sustainable and versatile energy consumption development efforts. The aerospace domain has set ambitious goals regarding gas emissions limitation, leading to new concepts and system architectures in several sectors. The interest in the electrification of transportation was revived, aiming at the concept of MEA, whose interests are known since 1883.

The replacement of heavy systems, such as mechanical, pneumatic, and hydraulic systems, reduces aircraft weight and fuel consumption with their electrical equivalents. Several projects have emerged in the last decades aiming to replace these systems using new technologies. The EPowerdrive project is a French project that aims to identify and study new topologies of power converters, semiconductors, and electrical machines in MEA.

This thesis is part of EPowerdrive project, whose main objective is to design a DC – AC converter (filters included) with gravimetric power density superior to 8 kW/kg and efficiency higher than 98.5% for a 70 kVA MEA power drive system. Technological bricks identified in Section 1.4 comprise the first part of the work developed in this thesis, detailed in Chapter 2 and used to select a power converter topology capable of meeting the constraints determined in Section 1.3.2.

CHAPTER 2

Multicriteria Optimization of a More Electric Aircraft Power Drive System

THIS chapter presents the state-of-art design bricks presented in Chapter 1 and the filters necessary to meet the criteria imposed in Section 1.3.1 and Section 1.3.2. An optimization based on the Pareto front is used to evaluate different converter topologies and semiconductor technologies for the MEA power drive systems. After that, one converter topology is chosen for a more detailed study in the following chapters.

Summary

2.1 Introduction

The object of the study of this thesis was discussed in Chapter 1 as a DC-AC converter for an MEA power drive system application. This system consists of a converter with 10 meters of unshielded cable and a 50 kW permanent magnet electric motor. The study will involve an individual optimization of each device that makes up the converter to assess the power density and efficiency of different topologies later. In this study, the characteristics of the cables and the electric motor must be considered. In the state of the art of optimizing the power density of MEA power drive systems, the following work stands out:

[39] [40]: In these works, a multi-objective optimization using a genetic algorithm uses multi-physics models and the MDO approach. The authors stick to a two-level converter topology with IGBT that is directly connected to the HSPMSM (High-Speed Permanent Magnet Synchronous Motor) without the use of cables. The authors consider optimizing the differential input filter to respect the Network Stability and Power Quality criteria defined by Airbus HVDC, using simple models to estimate the inductors and capacitors parameters. The heat sink considers a liquid cooling system, and HSPMSM weight optimization is also considered. On the other hand, the EMI filter design is not considered to reduce conducted emissions, nor is the overvoltage phenomenon at the motor terminals considered, probably because the system does not have cables.

[32]: In this work, a bidirectional SiC-based DC-AC converter is optimized for a three-phase load of 45 kW (nature of the load not specified). The optimization is done individually for each filter and the heat sink. Each element's lighter solution is considered to compose the converter's final solution for a given point of operation. No specific optimization algorithm is used. Two-level and three-level power converter topologies are evaluated. EMI filters are designed to limit conducted emissions, as differential filters at the converter input and output reduce voltage and current ripples. However, the HVDC criteria for Network Stability and Power Quality are not mentioned. The converter is also connected directly to the load without cables, and consequently, the Overvoltage levels are not evaluated. The author considers the need for 500 g for 500 W of semiconductors losses to calculate the heat sink. Filters passive elements design uses accurate models based on datasheet information.

[17]: The author presents an MDO approach with the use of a genetic algorithm for the optimization of a 15 kW two-level converter with SiC module. The impact of shielded and unshielded cables and the permanent magnet motor characteristics on the EMI filter design are also considered. Network Stability and Power Quality HVDC criteria and the Conducted Emissions criteria are also considered. The design routines of the filters passive elements are based on a database of components and their datasheets, allowing an accurate design of these elements. The cooling system also uses a precise optimization routine, which relates the heat sink dimensions, number of fins, and fan characteristic with the equivalent thermal resistance. Semiconductor loss calculations are based on the semiconductor characterization data, allowing an accurate loss calculation. However, the overvoltage levels at the motor terminals and the output current harmonics are not evaluated.

[25]: This work considers the optimization based on the Pareto-front of MMC (Modular Multicell) converters with different numbers of cells in series for a 45 kW application and a 1000 V HVDC bus. Various solutions are calculated for different operation points, and the lighter solution is considered. SiC and GaN technologies are considered. Conducted Emissions are not evaluated, nor are

the Grid Stability and Power Quality criteria. Cables are not considered between the converter and the machine. Thus Overvoltage levels at the terminals of the motor are also not evaluated. LC filters at the converter output are used to limit the output current ripple. Regarding the cooling system, CSPI (Cooling System Performance Index) method is used [42].

Some works are listed above regarding the criteria to be evaluated in this thesis are presented in Table 2. It is noteworthy that none of the works evaluates overvoltage levels at motor terminals and do not evaluate at least two criteria of what comes to be considered in this work.

Table 2 - State-of-art MEA power drive system design criteria and characteristics.

Criteria	[39] [40]	[32]	[17]	[25]
Converter Topology	2 - Level	2 - Level 3-Level	2 - Level	Multilevel
Semiconductor Technology	IGBT Si	SiC	SiC	GaN SiC
EMI Filter CE DO -160 (150 kHz – 152 MHz)	No	Yes	Yes	No
Network Stability and Power Quality HVDC	Yes	No	Yes	No
Cooling System	Yes (Moderate)	Yes (Moderate)	Yes (Precise)	Yes (Moderate)
Output Cables	No	No	Yes	No
Overvoltage level	No	No	No	No
THD_i	Yes (via motor project)	Yes	No	Yes
Year	2016	2016	2019	2018

To meet the criteria defined in Section1.3.2, in addition to the different converter topologies, semiconductor technologies, the PWM control technique, and the heat sink, four independent passive filters will be considered according to Figure 15. More details on the filter topologies will be covered in the following sections of this chapter.

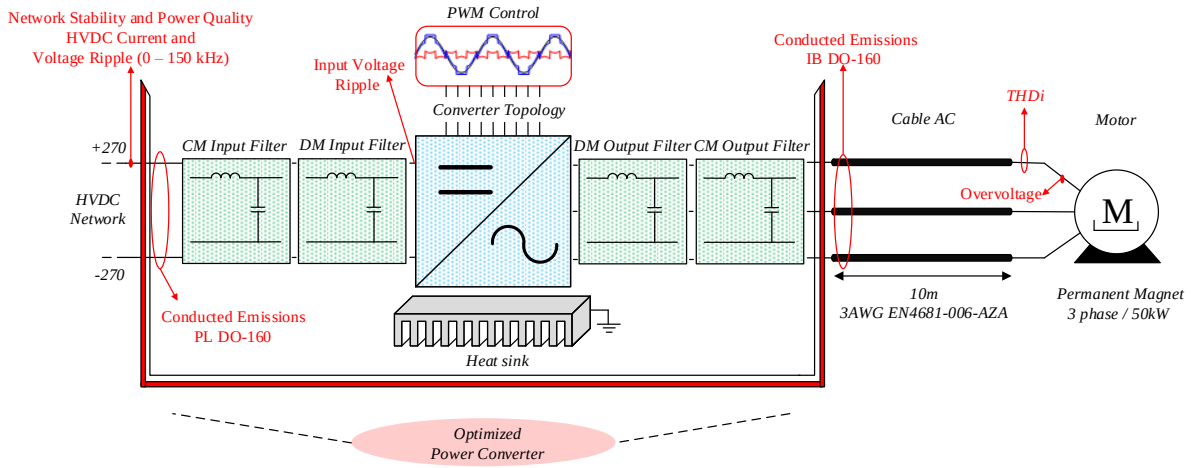


Figure 15 - Targeted converter with its respective filters to be evaluated through optimization.

- Common-Mode (CM) Input Filter and CM Output Filter to comply with Power Lines (PL) and Interconnecting Bundles (IB) CE limits imposed by the standard DO - 160;

- Differential-Mode (DM) Input Filter to comply with Network Stability and Power Quality HVDC criteria for current and voltage ripples between 0 to 150 kHz;

- DM Output Filter to limit output current harmonics and Overvoltage on the motor side.

Considering the filters above, the converter optimization blocks will be detailed in the following sections.

2.2 Multilevel Converter Topologies

The traditional 2-level inverter is widely used because of its simplicity and low cost. This topology usually uses semiconductors with a larger blocking voltage of 50% to 100% larger than DC bus voltage. The higher the blocking voltage in most semiconductor technologies, the higher the switching and conduction losses for given switched voltage and current. For that reason, a lower switching frequency should be used to balance conduction and switching losses [42] and increase overall inverter efficiency. However, low switching frequencies may increase the size of passive devices. This deadlock is resolved using multilevel inverters. They reduce voltage steps in inverter output voltage, reducing filtering needs.

Moreover, some multilevel inverters may increase the output voltage's effective switching frequency, reducing filter size [42] [43]. Another advantage is lower blocking voltage semiconductors, which present lower intrinsic capacitances related to semiconductor losses [45]. During the transistor switching process, semiconductor input capacitance C_{iss} is charged faster (for the same gate resistance) than higher voltage semiconductors. The longer the time to charge $C_{iss,}$ the longer it reaches $V_{GS\text{-}th}$ (gate to source threshold voltage), which causes an extension of dead time and a supplementary increase in conduction losses during this dead time. On the other hand, output capacitance C_{oss} has a direct impact on switching losses. The relation between parasitic capacitance and switching energies is exemplified in [46], where 4 GaN transistors are paralleled with the same gate driver, and turn-on and turn-off energies are higher than two devices in parallel for the current level, due to the higher equivalent C_{oss}.

The impact of multilevel inverters is also verified when considering differential-mode input filters and EMI filters. In [32], it is shown that replacing a traditional 2-level inverter with a 3-level inverter can achieve values of up to 33% reduction in the overall inverter weight.

2.2.1 Multilevel Series

Power inverter topologies universe is eclectic and diverse, and the topology choice is related to the application, semiconductor technology, and complexity. The traditional 2-level topology comprises most of the industrial applications due to the simple control. The use of 1200V SiC MOSFETs allows this topology to have efficiency higher than 99%. The efficiency criteria are essential and were the starting point for new topologies to be developed, with superior performance to reduce losses of silicon-

based semiconductors (IGBT-Si) used in the past. Noteworthy is the emergence of the three-level T-type topology [47], which allowed a performance increase and reduce switching losses and magnetic elements of traditional two-level inverters.

The use of power inverters in medium and high voltage applications was also one of the starting points for developing multilevel topologies due to the maximum voltage limit supported by semiconductors. Thus, other topologies such as Neutral Point Clamped (NPC) [48], active neutral point clamped (ANPC) [49], Flying Capacitor (FC) [50], [51], cascaded H-bridge (CHB) [52], modular multilevel inverter (MMC) [53] have appeared as inverter alternatives in the industry applications [54]. Recently, some multilevel topologies have been used with low voltage semiconductors for low voltage photovoltaic applications [55]. It allows to significantly increase the inverter output levels (3,4,5,6,7...), substantially minimizing the volume and weight of magnetic components. In conjunction with GaN technology, multilevel topologies can increase inverter power density considerably, as exemplified by the Google Little Box Challenge, where a 7-level FC-based 2kW inverter achieved a power density of 13.2 kW/dm^3 (216 W/in^3 at 97.6% peak efficiency [56].

The topologies mentioned above, presented in Figure 16, are grouped into the multilevel series inverters. They are directly related to the use of low voltage components and the gain in the inverter output voltage levels, which significantly reduces the size of the magnetic element. The number of required devices per the number of each topology's output level is described in Table 3, and their main advantages and disadvantages are shown in Table 4.

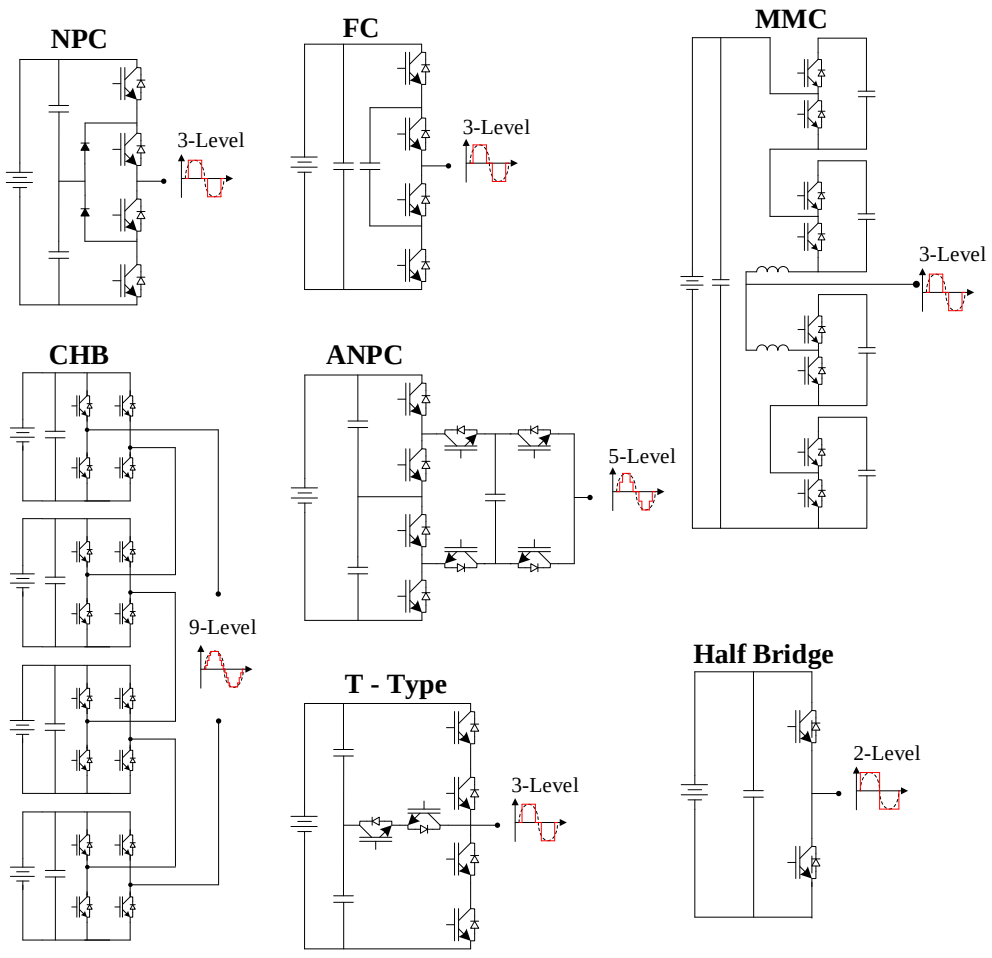


Figure 16 - Single-phase structure for multilevel series topologies and the traditional 2-Level Half Bridge.

Table 3 - Multilevel series topologies characteristics per phase.

Topology	# Output Levels	# Switches	# External Diodes*	# Capacitors	# Power Sources
NPC (Neutral Point Clamped)	m	2.(m-1)	(m-1) .(m-2)	m-1	1
FC (Flying Capacitor)		2. (m-1)	-	m-2	1
T - Type		***	-	**	1
ANPC (Active Neutral Point Clamped)		4+(m-1)	-	(m+1)/2	1
MMC (Modular Multilevel Converter)		4. (m-1)	-	2.(m-1)	1
CHB (Cascaded Halfbridge)		2. (m-1)	-	**	(m-1)/2

* Same voltage level devices

** Capacitors placed in parallel with the power supply were not considered.

*** In the literature was found only 3-Level, the 3-Level T-Type legs are usually associated in series to increase the voltage output levels.

Among the different inverter topologies presented above, five were selected to be considered in the optimization: the regular 2 - level cell (HB), Flying Capacitor (FC 3-level and 5 - level), and Neutral Point Clamped (NPC 3-level and 5 - level).

The CHB topology was not considered since it needs individual voltage sources for each half-bridge (the setup is fixed to one input voltage source, refer to Section 1.3.2.

MMC topology is commonly used for applications with some kV, and MVA [56] [57], [25] describes the use of this topology for MEA applications for 1 kV HVDC bus. This topology was discarded since a low voltage bus is used in this thesis (540 V).

ANPC and T-Type topologies need to directly associate transistors in series (at least 2), which can be problematic using 650 V GaN devices. Direct series connection of power transistors reduces switching speed, increasing switching losses [59] due to stray inductance increase in commutation cell (especially for discrete components as TO-247 packaging). Another problem is that simultaneous switching is necessary for series-connected semiconductors. Even a tiny delay in switching could cause significant damage to the circuit by setting all the bus voltage across a single switch, which is generally higher than the switch's breakdown voltage. Therefore, these two series topologies were not considered in this thesis study.

Table 4 - Multilevel series topologies advantages and disadvantages.

Topology	Advantages	Disadvantages
NPC [56] [57]	• All phases share a common dc bus, facilitating a back-to-back arrangement, where the same converter is used on the inverter and rectifier side. • Capacitors can be pre-charged as a group using only a preload circuit. • Topology is **widely disseminated in literature** and industry due to its robustness linked to the inherent clamping of the power semiconductors' blocking voltage.	• It is necessary to **monitor and control the voltage balance in bus capacitors** because DC intermediary levels tend to carry or unload the positive or negative bus individually. • The number of required clamping diodes increases with the square of the number of voltage levels. Thus, for the sake of cost, it is necessary to use components with higher blocking voltage. • Limitation on switching frequency due to the use of higher blocking voltage components has higher switching losses. • Switching **losses** and loops are **not evenly distributed** between all semiconductors. • The topological interconnection structure is complex when compared to examples of modular cascading topologies and others.
FC [49][57][58]	• Redundancy of topological states available to balance levels of capacitor voltage. • Enables **modular organization** between capacitive levels. • A large number of capacitors makes it possible to operate during short-term interruptions or voltage dips. • Snubbers are generally not used as capacitors inherently act by reducing *dV/dt*.	• It is necessary to **balance the voltage across all capacitors** during operation or even during pre-load. • A large number of capacitors makes this **expensive** and **bulky** converter. • FC capacitors have high capacitance, so their voltage does not vary abruptly with load current that will pass through them during the switching period.
T – Type [57][59]	• All phases share a common dc bus., facilitating a back-to-back arrangement, where the same converter is used on the inverter and rectifier side. • Capacitors can be pre-charged as a group using only a preload circuit. • Features balanced total losses and reduced switching losses by half in series devices (compared to NPC), increasing the switching frequency or switching capacity power. • **Switching loops are symmetrical and balanced** and connect directly with the converter output, facilitating the mechanical design and allowing a natural reduction in parasitic inductances.	• Like the NPC, it is necessary to monitor and control the voltage across bus capacitors. • Series devices present the difficulty of blocking voltages sharing. It is necessary to use passive snubbers or active forms to ensure correct voltage sharing between devices. • **Complexity increases** the high output voltage levels.
ANPC [57][60]	• The same as NPC. • Higher power and switching frequency compared to the NPC.	• The same as NPC, except for the fact of control bus capacitor voltage unbalance. • The **need for more active components**, together with its control apparatus compared to NPC
MMC [62][63]	• **Modularity** to meet any voltage level requirements. • **High efficiency**, which is essential for high-power applications, • Superior harmonic performance, specifically in high-voltage applications with many identical submodules (SMs) stacked with low-voltage ratings, can reduce the size of passive filters.	• The same as FC. • Circulating current on the double of the fundamental frequency may increase semiconductors losses if not suppressed.
CHB [64][65]	• The number of output voltage levels is **more than double** the number of AC - DC converters. • Allows modular organization and thus facilitates the manufacturing process. • Each module has low working voltages and makes it possible to use components with lower blocking voltage. • Inherent application in photovoltaic systems, fuel cells, where their numerous DC sources.	• One AC – DC is required for each Half-bridge. It makes the application more complicated, as it requires multiple rectifiers. • Complexity and **cost** of manufacturing the transformer with multiple secondary. • Many operations states also increase the **control complexity** since controlling many components separately individually will be necessary.

In the universe of high-efficiency and high-power converters, another group of converters is commonly studied, as it allows an increase in load for traditional components: Multilevel Parallel topologies. Switching cell parallelism reduces the output current ripple and increases the converter's dynamic performance [70]. That group of converters is presented in Section 2.2.2.

The converters modeling from switch's logic states (open or closed) allows the converter behavior generalization regardless of the PWM control technique. It can also extract the output voltage waveforms, input current, output current, and switches current waveforms analytically. This information is crucial for calculating losses in semiconductors and filters, whether DM or CM.

A two-level three-phase inverter is presented in Figure 17 (a). According to the output current I_{ph} of the single-phase leg presented in Figure 17 (a), it is possible to write the equations that relate inverter input current I_{bus} and output voltage $V_{ph\text{-}ref}$ with the output current through switches states (S =1 switch on or S = 0 switches off) and the I_{ph}. Since semiconductor losses are equally distributed on switches, only one switch current waveform can be considered to estimate all semiconductor losses.

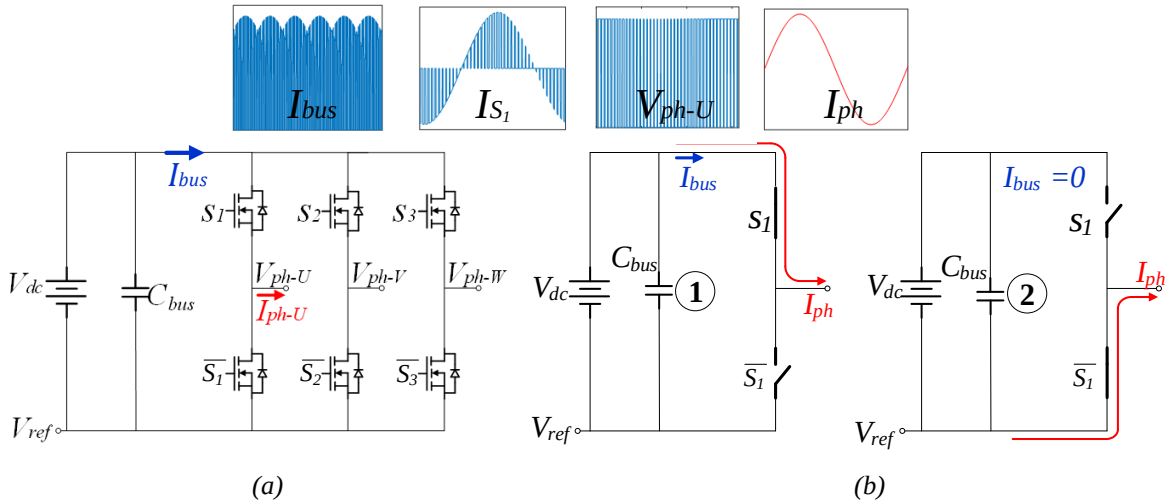


Figure 17 - Two-level converter. (a) Three-phase inverter and (b) Switches states and I_{bus} for I_{ph} leaving the converter.

The FC topology modeling is described in [71]. For a "*q*" level monophase inverter, the equivalent circuit is presented in Figure 18, where *k* is the switch number.

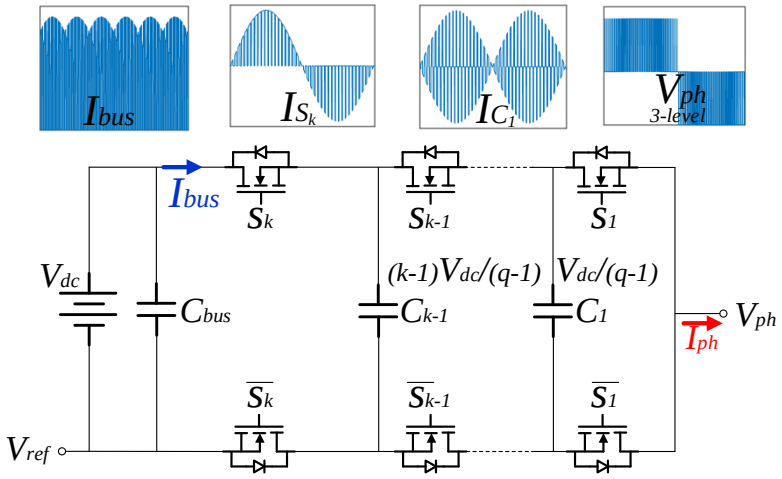


Figure 18 - Leg FC with "q" output levels.

The top switches are complementary to the switches right below, and the converter analysis can be done by considering only the top devices. This topology also presents equally divided losses between all switches. Knowing the current waveform of only one switch can estimate the total inverter losses, as the two-level inverter.

The NPC analysis is not as direct as the two-level and the FC topologies since the current is not equally divided between all devices. There is also the presence of the diodes that require a middle point connection in the bus capacitors. The switches above the converter output point are complementary to those below that point [72]. To illustrate the NPC's behavior and the relation between the output current and semiconductors current, Figure 19 presents one leg of a 5-level NPC.

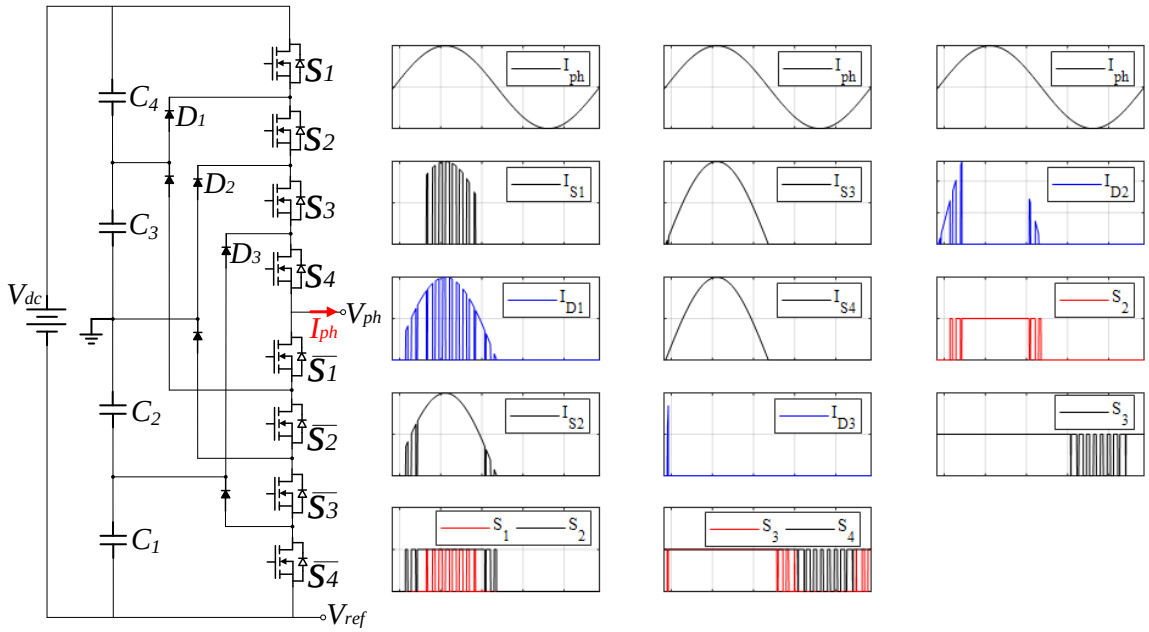


Figure 19 - Monophase 5-level NPC leg.

The modeling of series topologies described in this section is well known in the literature and is presented in Appendix A. The equations consider the relation between switches states and output current to determine the inverter input current Ibus, which is essential for designing a DM input filter. It also considers semiconductors current, used to estimate semiconductors losses, and flying capacitor current, used to designed FC topology capacitors. These equations were developed for "*q*"- level NPC/FC topologies.

The following section presents the group of multilevel parallel topologies, their particularities and how these topologies will be considered in the development of this thesis.

2.2.2 Multilevel Parallel

Another group of multilevel inverters have emerged to solve the problem of high current applications, named parallel multilevel or interleaved topologies. They help achieve systems capable of handling large amounts of power [73]–[76]. Switching cells are connected in parallel through coupled or uncoupled inductors, as presented in Figure 20. It allows each leg's current to be a portion of the inverter output current and increases the apparent ripple frequency of output voltage and current. Directing a reduction of passives weight and volume [77]. Among the advantages of paralleling switching cells stand out the increase of power density and the increase in the converter face of disturbances [78].

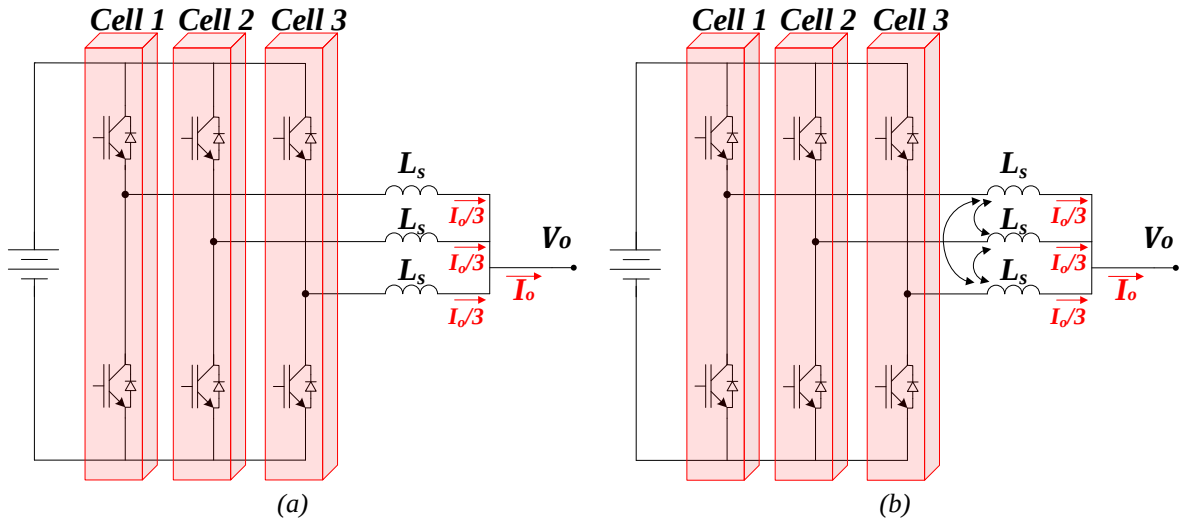


Figure 20 - Multilevel Parallel topologies with (a) uncoupled and (b) coupled inductors.

On the other hand, the appearance of circulating currents between the inductors is one of the main obstacles in controlling this type of converter, where much effort is devoted to ensuring stability and reliability. This circulating current appears when switching cells share the same DC-link [79]. One commonly used technique to suppress circulating currents is to use multiple phase-shifted carriers and use current ripple cancelation, allowing an even more significant reduction of the output inductor's weight [80]. Other techniques are described in [81] with the use of an input CM filter, isolation transformer [81] [82], or intercell transformers [84].

A trade-off between coupled and uncoupled solutions is presented in Table 5. For the development of this thesis, it was considered to associate the inverter switching cells through not coupled inductors by the factors described below:

- Estimating the output inductor's weight and stray elements that critically impact high frequencies is more straightforward. The main objective is to optimize a power converter vis-a-vis the weight, especially precisely. Intercell transformers design is quite complex to put in an optimization loop with all the constraints in Section 1.3.2.

- The possibility to work in degraded mode and open-loop control.

Table 5 - Comparison between coupled and uncoupled inductors for multilevel parallel topologies

Uncoupled Inductors	Coupled Inductors
✓ It makes the converter configuration modular and easily expandable to a different number of legs connected in parallel.	× A new design is necessary if the number of legs connected in parallel changes.
× Heavier	✓ Lighter and smaller inductors for the same current ripple than uncoupled inductors
✓ Easier to estimate the inductor's design and characteristics.	× More challenging to estimate the inductor's weight and stray parameters than the uncoupled inductors.
✓ Operational safety: in the event of an arm fault, it is easier to control without coupling. It is an essential point in aeronautics.	× Harder to control.
× Higher Losses.	✓ Lower Losses
× Low-frequency components of the output current also flow through the inductor	× Lower reliability than uncoupled inductors

The following section will describe the modeling of uncoupled inductors for interleaved converters considered in the optimization calculation.

2.2.2.1 Modeling of uncoupled inductors for interleaved converters

Based on a symmetrical system, the control to guarantee equal current sharing between paralleled legs consists of imposing the same duty cycle (same current waveform = same losses) with their corresponding carriers phase-shifted by $2\pi/p$, where p is the number of paralleled legs [73]. It is exemplified in Figure 21 for $p = 3$, and the first conclusion is that, theoretically, output current I_O has no ripple.

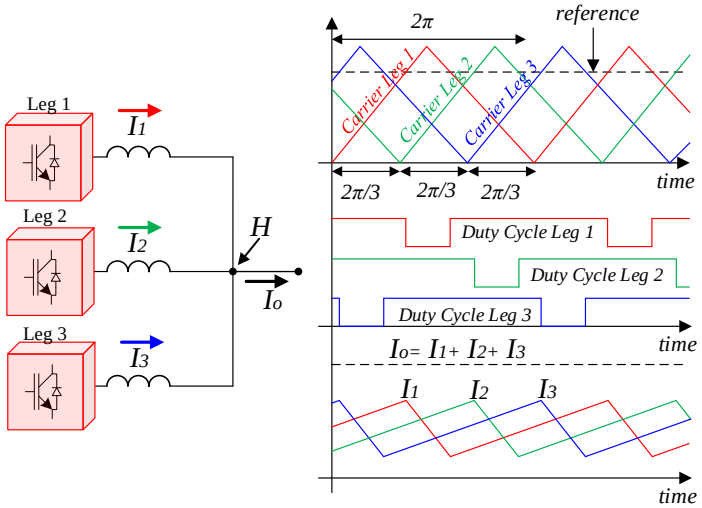


Figure 21 - Phase shift carriers and current ripple for a three legs parallel converter with uncoupled inductors.

The works cited in Section 2.2.2 always address an LC filter or a capacitor between interleaved converters and the load. A capacitor in the converter's output will impose a low-frequency sinusoidal voltage (240 Hz – electric machine nominal operation) on the paralleled inductor's common terminal (point *H* in Figure 21), which increases the I_o current ripple. The high the current ripple, the high conductor, semiconductors, and core losses. In this case, output inductors must be designed for low current ripple to reduce adverse effects caused by current ripple to increase the inductor's weight/volume. In this thesis application, there is no need for a sinusoidal output voltage. The converter will be directly connected to an electric motor, which presents a high inductance value (around 330µH per phase). It can maintain a harmonic current distortion (THD_i) rate of around 5% (for a 2-level three-phase inverter with SPWM – Sinus PWM - and f_{sw} = 20 kHz). Therefore, the following ***hypothesis*** is considered: DM output filter will be designed regarding overvoltage on machine terminals. Then, the output filter capacitor can have a low value, not maintaining sinusoidal voltage on the *H* point. This hypothesis implies that the voltage in *H* can also be multilevel. It is reasonable to think that paralleled inductors can have a high current ripple since I_o will not see this high-frequency ripple. This approach is presented in Figure 22 (multilevel voltage on motor terminals). A high inductive impedance Z_o is connected on the output of three paralleled legs that presents an output voltage V_o.

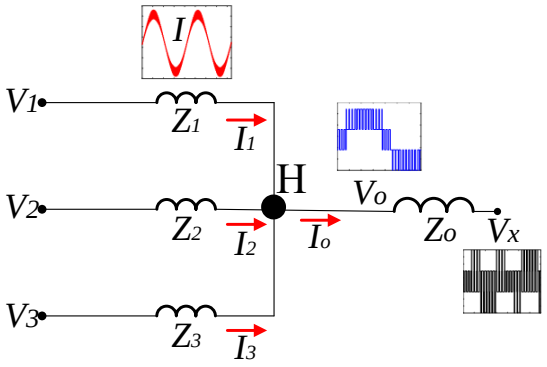


Figure 22 - Three legs in parallel through uncoupled inductors with multilevel output voltage at high inductive load terminal.

The voltages V_1, V_2, and V_3 represent each leg's output voltage in parallel, and Z_1, Z_2, and Z_3 present the impedance of the output inductors. The output current I_o is calculated as:

$$I_o = I_1 + I_2 + I_3, \tag{2.1}$$

and the output voltage V_o:

$$V_o = I_o.Z_o, \tag{2.2}$$

but also, as a function of each phase output voltage:

$$\begin{aligned} V_o &= V_1 - I_1.Z_1, \\ V_o &= V_2 - I_2.Z_2, \\ V_o &= V_3 - I_3.Z_3. \end{aligned} \tag{2.3}$$

From the equations above, I_o can be expressed as:

$$\begin{aligned} V_o &= (I_1 + I_2 + I_3).Z_o \\ 3.V_o &= V_1 + V_2 + V_3 - (I_1.Z_1 + I_2.Z_2 + I_3.Z_3) \\ I_o &= \frac{V_1 + V_2 + V_3}{3.Z_o} - \frac{(I_1.Z_1 + I_2.Z_2 + I_3.Z_3)}{3.Z_o}. \end{aligned} \tag{2.4}$$

Since V_o is a multilevel voltage as $V_{1,2,3}$, and assuming $V_{1,2,3} \gg I_{1,2,3} * Z_{1,2,3}$, then V_o can be expressed as:

$$I_o = \frac{V_1 + V_2 + V_3}{3.Z_o} \rightarrow V_o = \frac{V_1 + V_2 + V_3}{3}. \tag{2.5}$$

Due to V_o and $V_{1,2,3}$ multilevel voltages, I_o presents a low ripple, which means that high-frequency components of $I_{1,2,3}$ stay in the path of impedances $Z_{1,2,3}$. Therefore, current I_1 can be calculated:

$$I_1 = \frac{1}{L_1}.\int (V_1 - V_o).dt = \frac{1}{L_1}.\int \frac{(2V_1 - V_2 - V_3)}{3}.dt\ . \tag{2.6}$$

To maximize I_1, V_2 and V_3 must be 0, and V_1 has its highest value (bus voltage E). In a general way, inductors current I_{Ls} can be solved from I_1, for p paralleled cell as:

$$\begin{aligned} I_{L_s} &= \frac{1}{L_s}.\int (V_s - V_o).dt = \frac{1}{L_s}.\frac{(p-1)}{p}.\int E.dt\ ; \\ E &= \frac{p}{(p-1)}.\frac{L_s.dI_{L_s}}{dt}\ , \end{aligned} \tag{2.7}$$

where s is the leg number and:

$$dI_{L_s} = \Delta I_{L_s}\ ;\ dt = \Delta T\ ;\ T = \frac{1}{(N-1).f_{sw}}. \tag{2.8}$$

N represents the number of inverter output voltage levels for one leg, f_{sw} is the switching frequency, and D is the duty cycle. It is shown that output voltage apparent frequency is proportional to (N-1), then inductors current ripple is calculated as:

$$\Delta I_{L_s} = \frac{(p-1)}{p}.\frac{E.D}{L_s.(N-1).f_{sw}}. \tag{2.9}$$

The inductance L_s to guarantee the more significant current ripple $\Delta I_{Ls(max)}$ can be calculated by considering the duty cycle $D_{\Delta iLmax}$ max value.

$$L_s = \frac{(p-1)}{p} . \frac{E.D_{\Delta iLmax}}{\Delta I_{L_{s(max)}} . (N-1) . f_{sw}} . \tag{2.10}$$

As presented in Appendix B, for two paralleled legs, the greater ripple will occur for D = 0.5, while for three paralleled legs, it occurs for D = 0.33. Therefore, D_{max} is inversely proportional to N_p:

$$D_{\Delta iLmax} = \frac{1}{p}, \tag{2.11}$$

$$L_s = \frac{(p-1)}{p^2} . \frac{E}{\Delta I_{L_{s(max)}} . (N-1) . f_{sw}} . \tag{2.12}$$

The calculation of paralleled legs inductances is exemplified by circuit simulation waveforms presented in Figure 23. In this example it was considered a 2-level inverter, with three paralleled legs per phase, I_o = 184 A (I_{Ls} = 61.33 A), E = 540 V, f_{sw} = 20 kHz, f_f = 240 Hz and $\Delta I_{Ls(max)}$ = 40%. It implies in L_s = 244 µH according to the previous equation. It is verified that the maximum current ripple occurs for D = 0.33, and the simulated current ripple at this point is close to the considered (40%) on the design of L_s.

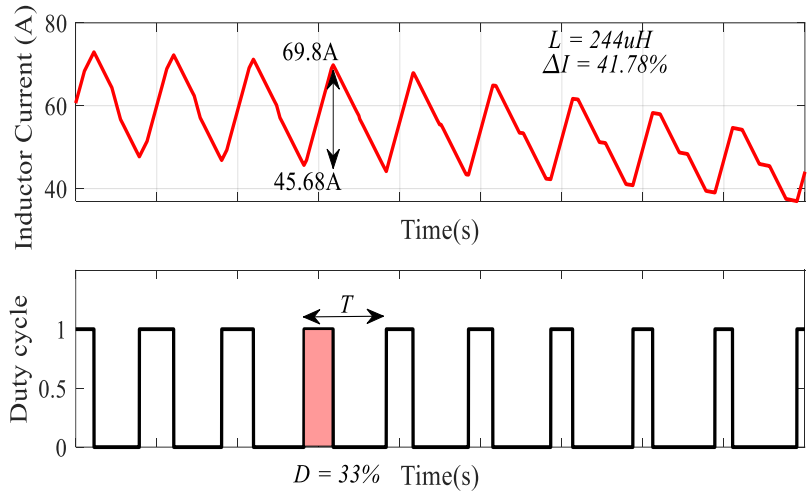


Figure 23 - Inductor current ripple for a 2-level inverter with three paralleled legs with L_s = 244 µH for I_o = 184 A, E = 540 V, f_{sw} = 20 kHz, f_f = 240 Hz and $\Delta I_{Ls(max)}$ = 40%.

This section presented the mathematical modeling for the design of uncoupled inductors used on multilevel parallel inverters. Concerning the existing works, the main contribution of this section is the absence of a capacitor at the inverter output. In this way, the output inductors deal with multilevel voltages at both terminals. The following section contemplates the presentation of semiconductors technologies, characteristics, and selection procedure to be used in the optimization.

2.3 Semiconductors

Wide bandgap (WBG) semiconductor materials are the result of the quest of the R&D activity (Research and Development) for smaller, faster, more reliable power electronic components and with higher efficiency than Si (silicon-based) counterparts. Among the WBG high-efficient devices, the silicon carbide (SiC) and gallium-nitride (GaN), high electron mobility (HEMT) semiconductor, concentrate the efforts of researchers and companies in the last two decades. They can operate in higher temperatures (SiC mainly), voltages, and switching frequencies while reduces weight, volume, and life-cycle cost [85] in power applications compared with the conventional semiconductor materials. They lead to significant energy saving in industrial applications, electric vehicles, fuel cells, integration of renewable energy onto the electric grid.

Among semiconductor's physical and electrical properties presented in Table 6, the greater the band gap energy, the higher the sustainable semiconductor operating temperature. As temperature rises, the thermal energy of electrons in the valence band increases, and they pass to the conduction band once the threshold temperature (150 ^{o}C for Si) is reached. GaN and SiC semiconductors have almost 3 and 2 times the bandgap energy than Si, therefore preferred for high-temperature applications (if the packaging and the surrounding environment also hold high temperature). SiC semiconductors have higher thermal conductivity than GaN, so they are preferred for high voltage and temperature applications.

Table 6 - Physical property constants of Si and main wide-band-gap semiconductors [86].

Property	Unit	*Si*	*SiC*	*GaN*	*GaAs*	*Diamond*
Band gap	eV	1.12	2.23	3.39	1.43	5.47
Electron mobility μ_e	cm^2/V_s	1400	1000	900	8500	2200
Hole mobility μ_h	cm^2/V_s	600	50	150	400	1600
Electric breakdown field E_c	V/cm	3.0×10^5	1.5×10^6	3.3×10^6	4.0×10^5	1.0×10^7
Thermal conductivity λ	W/cmK	1.5	4.9	2.0	0.5	20
Saturated electron drift velocity V_{sat}	cm/s	1.0×10^7	2.7×10^7	$2.7x10^7$	2.0×10^7	2.7×10^7
Relative dielectric constant ε		11.8	9.7	9.0	12.8	5.5

On the other hand, the high electron mobility and electric breakdown field of GaN semiconductors make them the optimal material where high frequency is required. Diamond devices, being the least mature of WBG semiconductor materials, are inhibited by the process necessary to make them fit for electronics [84] [85]. Considerable work is needed on commercial semiconductor processes to enable widespread applicability and high-volume usage. Although GaAs (gallium arsenide) semiconductors have higher electron mobility than Si, it has severe processing limitations, including less stability during thermal processing, insufficient native oxide, high cost, and much higher defect densities.

Figure 24 illustrates the opportunity space for WBG (dashed area) associated with Si performance limitations (red line) and possible applications that WBG may dominate.

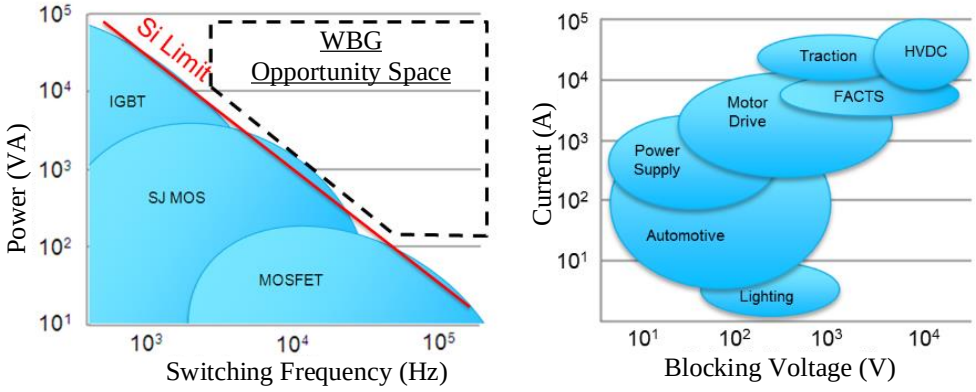


Figure 24 - WBG possible applications: (a) Relationship between power and switching frequency. (b) Application areas that lie within the dotted line area include [89].

The energy gap of SiC and GaN devices is more significant than Si's, which leads to higher blocking voltage ability in the same die size. It means that the die can have a smaller size for the same blocking voltage value. Additionally, the small the die size, the smaller the parasitic capacitances (e.g., C_{oss}) and gate charge. Thus, it improves WBG operating at higher frequencies because of the lower switching losses [90]. On-resistance is another parameter commonly used to compare different semiconductors since it directly relates to semiconductor losses. WBG specific on-resistance is at least an order of magnitude lower than Si and up to several kilovolts of blocking capability according to [91] and presented in Figure 25.

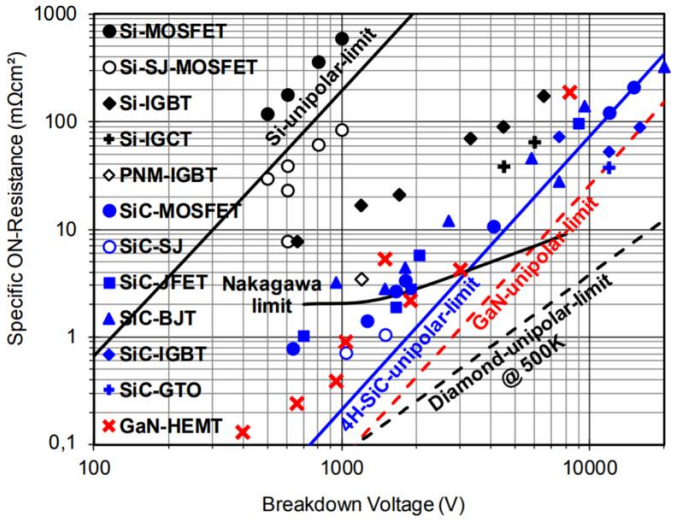


Figure 25 - Specific on-resistance(R_{on}. A)of various Si, SiC, and GaN semiconductors at 25 °C together with the respective limits [91].

The characteristics described in the previous paragraphs make GaN and SiC semiconductors used in the short and medium-term in most applications that demand high performance. In [89] is presented the latest market-analysis forecasts for WBG devices. With a compound annual growth rate (CAGR) of about 30% over ten years, it will bring global sales to US$3.7 billion in 2025, up from US$210 million in 2015.

This thesis fits in power semiconductors applications and not in a deep analysis of each semiconductor's characteristics. Thus, the bibliographic review here aims to justify using these new technologies due to the significant increase in efficiency and reduction in weight and volume of electrical systems, representing aircraft electrification's main objectives. The following are some of the gains found in the literature regarding the use of SiC and GaN to Si:

- SiC can reduce on-resistance to two magnitudes orders compared to existing Si devices and reduce switching losses by ten times [92].

- GaN is grown on top of a Si substrate that limits the operation temperature (150 ºC) but with a chip area around five times shorter than SiC and Si. On the other hand, there are SiC applications that reach 400 ºC [93].

- GaN, its lateral device structure, and majority carrier diode provide deficient gate and zero source-drain recovery charges. As a result, GaN devices can handle tasks with high switching speeds. GaN can present two times lower losses than SiC [94] and may switch between 2 to 4 times faster, while it may have a factor superior to ten compared to Si devices.

- Si's heatsink can be around five times heavier than GaN's and almost ten times than SiC's for the same application [95].

- Replacing Si devices by WBG can represent around 17% of energy savings in Data Centers that can represent 28.7 TWh/year [96];

- The penetration of WBG in photovoltaic inverters could lead to the increased energy production of 10.3 TWh/year, representing around 2% of energy savings in these applications. On the other hand, the energy savings in wind energy can be 3% [97].

- The use of WBG on battery electric vehicles can increase energy savings to 17% compared to Si devices. It represents 767 kWh/year per car [97].

WBG's promising advantages come with one significant drawback: the increase of electromagnetic interference (EMI) associated with the high *dV/dt* and *dI/dt* during switching transient. Severe voltage and current ringing are verified on circuit stray elements responsible for semiconductor reliability issues and increased radiated and conducted emissions [94] [95]. Therefore, WBG semiconductors emerged with the reinforcement of the inability to dissociate different design disciplines, as PCB (Printed Circuit Board) routing, EMI modeling, Cooling systems, Filters, etc. Considering the arguments aforementioned, it is noticeable that this thesis fits singularly in this scenario.

2.3.1 Semiconductors Selection

With the intent of increasing power drive system efficiency and power density, semiconductors must be chosen considering their respective losses. One method to choose a semiconductor is to

consider a given share on conduction and switching losses and, from the current level, estimate the conduction losses based on semiconductor on-state resistance $R_{DS(on)}$ (for Si or SiC MOSFETs or HEMT GaN). Figure 26 shows the $R_{DS(on)}$ of different transistor technologies (Si, SiC, and GaN) and different breakdown voltages for $T_{j\text{-max}}$ – 15°C.

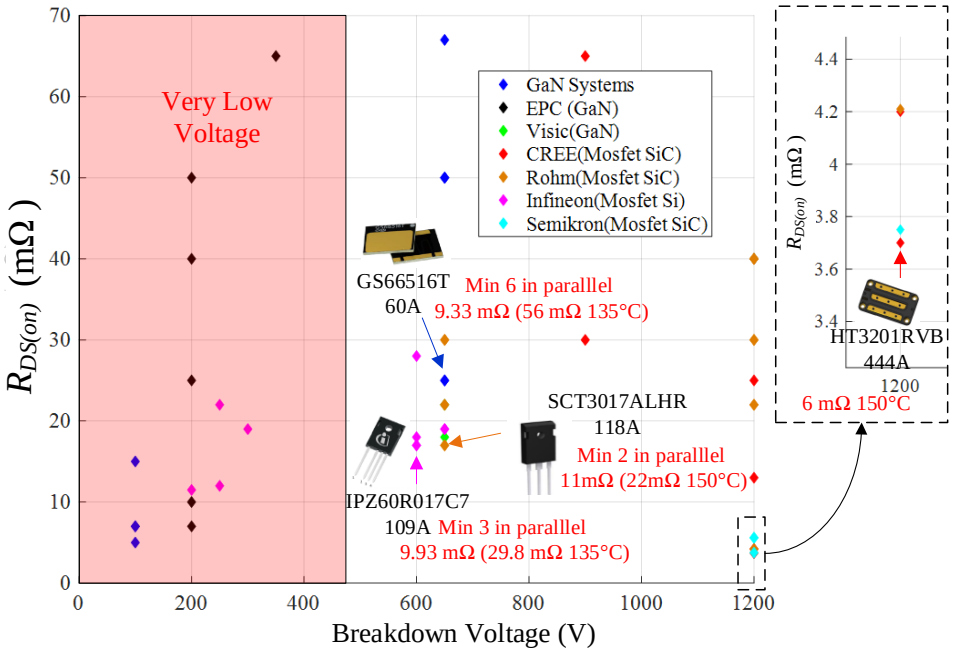


Figure 26 - Semiconductors Trade-off. Four components were chosen to be compared, one from each technology.

Semiconductor series connection is inherently necessary for FC and NPC inverters. However, it is also possible to use low voltage (200V, for example) components connected in series to hold the bus voltage. The number of transistors in series N_s to hold bus voltage V_{bus} is given by:

$$N_s = round\left(\frac{2.V_{bus}}{V_{DS(\max)}}\right). \tag{2.13}$$

Where V_{DSmax} is transistor breakdown voltage. Suppose a maximum value of $R_{DS(on\text{-}desired)}$ is desired in the current path. In that case, the number of transistors is parallel N_p per switch can be expressed from transistor $R_{DS(on)}$ as and the number of transistors in series $N_{s\text{-}path}$, on conduction state forming the current path, as:

$$N_p = round\left(N_{s-path}.\frac{R_{DS(on)}}{R_{DS(on-desired)}}\right). \tag{2.14}$$

Thereby, the total number of transistors N_t, per switch, is given by:

$$N_t = N_s.N_p. \quad (2.15)$$

In the case that 200 V components are used, in 3-level FC topology, for example, at least three transistors must be used in series per device to hold 540 V (2*V_{FC}), totalizing six series transistors for the two top switches (N_s = 3 and $N_{s\text{-}path}$ = 6). Each device is selected to hold at least double the applied voltage for security reasons (e.g., V_{bus} in aircraft applications can reach 900 V for a short period). The top switch's equivalent series resistance represents the output current path's resistance ($R_{DS(on\text{-}desired)}$). By considering each device with $R_{DS(on)}$ = 10 mΩ, and $R_{DS(on\text{-}desired)}$ of 10 mΩ for the current path, six transistors are needed in parallel per device (N_p). So, with four switches per phase, each switch is composed of 18 transistors (N_s * N_p), totaling 216 transistors for a three-phase 3-level FC inverter. A high number of devices reduces inverter reliability drastically, then only components with blocking voltage higher than 600 V were considered for the optimization.

Assuming an inverter efficiency of 99%, approximately 700 W of transistor losses for the current 70 kVA power converter. In a hypothetical case that the conduction losses represent 70% (490 W) of total losses, the transistor shall have a maximum resistance of approximately 9.66 mΩ (163 W per phase and a current of 130 A_{rms}) in the current path. Table 7 summarizes the total number of transistors in parallel, considering the selection presented in Figure 26 for $T_{j\text{-}max}$ -15ºC. For the 1200V SiC module HT3201RVB, there is no need for devices in parallel.

Table 7 - Number of transistors in parallel to reach 9.66 mΩ based on the components selected in Figure 26.

Part Number	Breakdown Voltage	$R_{DS(on)}$	N_p
HT3201RVB	1200V	6 mΩ (150 ºC)	1
GS66516T	650V	56 mΩ (135 ºC)	6
IPZ60R017C7	600V	30 mΩ(135 ºC)	3
SCT3017ALHR	650V	22 mΩ(150 ºC)	2

If two devices must be connected in series (650 V devices) to hold the application bus voltage of 540V, it is necessary to double the number of components in parallel. Therefore, the inverter should have around 12 components in parallel per switch using GS66516T, representing exactly 48 components per phase and 144 of the complete inverters. In contrast, 24 per phase and 72 for the entire inverter could be used considering SCT3017ALHR (it would be 11 mΩ against the required 9.66 mΩ). For IPZ60R017C7, 36 devices are needed per phase, totalizing 108 devices for the entire inverter.

Semiconductors research compiled in Figure 26 was done until Jan. 2019, and the optimization was done considering those devices. At this point, there was also a 900V SiC MOSFET family designed by CREE:

- C3M0065090J with 65mΩ (25 ºC) in the TO-263-7 package.
- C3M0030090K with 30mΩ (25 ºC) in TO-247-4 package.
- CPM3-0900-0010A with 10mΩ (25 ºC) in bare die.

Both transistors in the TO package present on-resistance higher than SCT3017ALHR, and CPM3-0900-0010A is only available in bare dire. Thus, the CREE 900V SiC MOSFET family was not considered in Figure 26.

A 1200V IGBT-Si transistor (SKM600GA12E4) was also considered on a 2-level topology as a traditional reference inverter. This component was chosen since it presents conducted losses relatively close to the 1200V SiC MOSFET HT3201RVB for the same topology. Table 8 represents the semiconductors considered for the efficiency trade-off between different multilevel topologies presented in Section 2.2.

Table 8 - Power semiconductors selected based on the components present in Figure 26.

Part Number	Breakdown Voltage	$R_{DS(on)}$ (25ºC)	Technology	Packaging
SKM600GA12E4	1200 V	-	IGBT	Module
HT3201RVB	1200 V	3.7 mΩ	SiC MOSFET	Module
GS66516T	650 V	25 mΩ	GaN HEMT	GaNPX®
IPZ60R017C7	600 V	17 mΩ	Si MOSFET	TO-247
SCT3017AL	650 V	17 mΩ	SiC MOSFET	TO-247

Regarding power diodes for NPC topologies, the SiC Diode C5D50065D was selected among others due to low conduction losses proportional to the equivalent diode forward resistance $R_{diff\text{-}135°C}$. The number of devices in parallel is calculated for the application output peak current of 184 A_{pk}, as presented in Table 9.

Table 9 - SiC Power Diode selection for NPC topology.

Part Number	Breakdown Voltage	I_F (25ºC)	Supplier	Nº diodes for 184A	R_{diff} (135ºC)
C5D50065D	1200 V	46 A	CREE	4	21.6 mΩ
UJ3D06560KS	1200 V	60 A	USCi	3	33.4 mΩ
SC3S05430A	650 V	30 A	Rectron	6	34.9 mΩ
SCS240AE2	650 V	40 A	Rohm	5	44.1 mΩ
STPSC40065C	650 V	40 A	ST	5	35.1 mΩ

Semiconductor losses are the main criteria for a high-efficiency converter design. In addition to the semiconductor characteristics presented in this section, the control technique applied to the converter greatly influences the losses. It is shown that Discontinuous Pulse Width Modulation (PWM) methods can reduce total losses of up to 31% compared to Continuous PWM methods. The following section will present different modulation techniques for controlling different converter topologies.

2.4 Pulse Width Modulation Techniques

The control of the power converters switches has a strong influence in several areas around the converter, such as losses in the semiconductors, current and voltage ripple on passive devices, and EMI.

This section is responsible for a quick review of the different modulation techniques used to control the topologies selected in Section 2.2. In general, high-frequency modulation techniques can be divided into two main groups: Space Vector Pulse Width Modulation (SV-PWM) and Carrier-Based PWM (CB-PWM), as presented in Figure 27. This thesis focuses on CB-PWM due to the simple implementation of analytical equations that can be used for multilevel series and parallel converters and the degrees of freedom introduced by this technique.

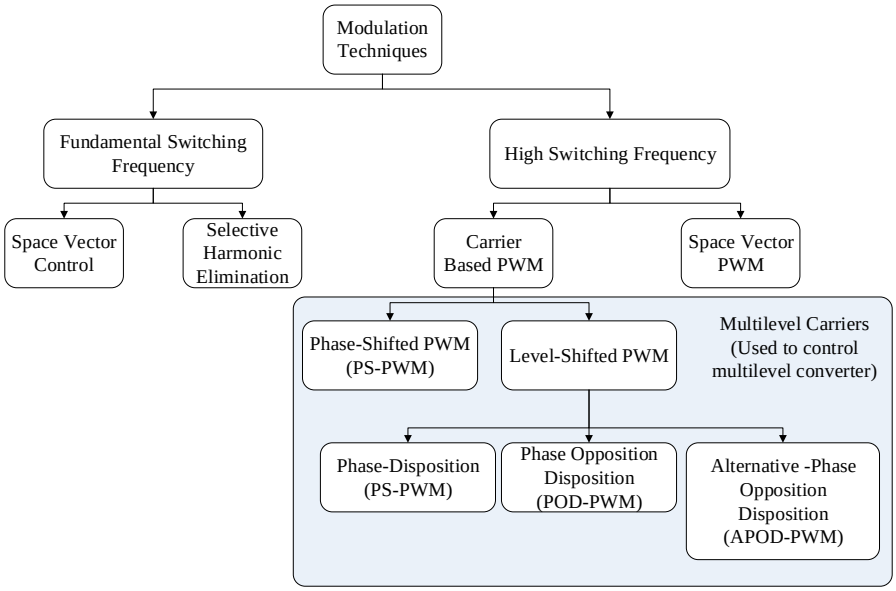


Figure 27 - Classification of modulation techniques [75].

In CB-PWM, control signals are generated by comparing a reference signal (named modulating signal) with a carrier to determine the semiconductors switching frequency. These carriers are usually formed by triangular edges, saw-tooth edges, or random edges. The most common technique is the SPWM (sinusoidal PWM), where the reference signal is sinusoidal. This technique's output voltage will be calculated according to the modulation index (m_a), representing the ratio between the amplitude of the reference and the carrier signal.

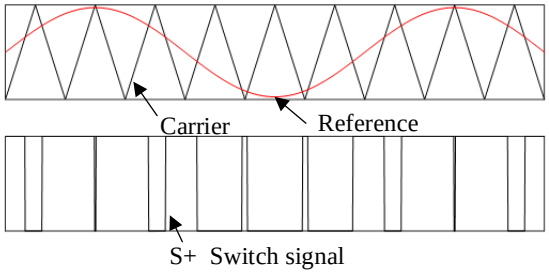


Figure 28 - Comparison between the reference and the carrier signals and equivalent switching signal.

One advantage of this technique is using the Zero Sequence Injection (ZSI) to modify the reference signal to increase the converter's performance. This injection is represented in the modulator in Figure 29. By correctly selecting the zero-sequence signal, it can extend the volt-second linearity range of SPWM, improve the waveform quality, and reduce the switching losses significantly [100]–[103].

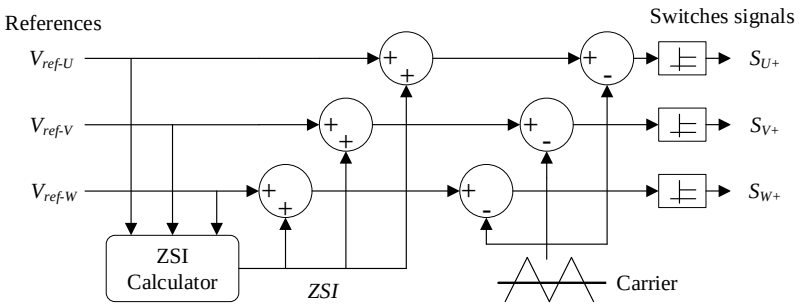


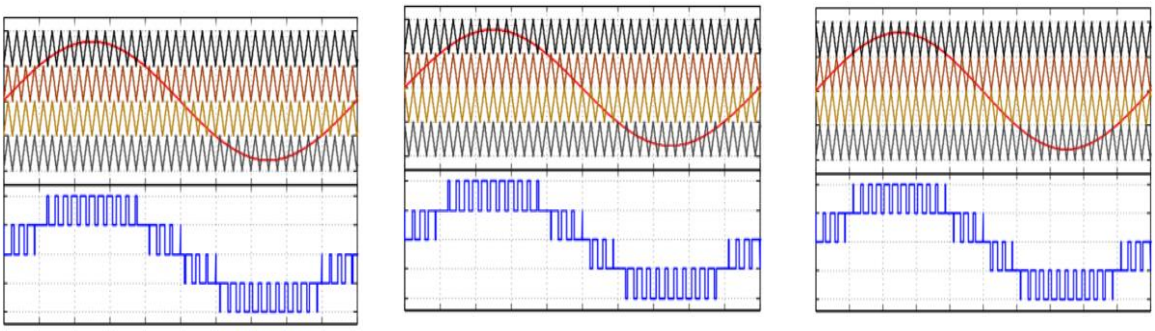
Figure 29 - PWM-ZSI generalized signal block diagram.

These techniques that used different ZSI (PWM- ZSI) are commonly divided into continuous (SPWM or SVPWM) and discontinuous techniques (e.g., DPWM0, DPWM1, DPWMMAX, and DPWMMIN), and their main characteristics are described in [97] and [98]. These techniques can be calculated analytically, facilitating their implementation on FPGA (Field Programmable Gate Array) or DSPs (Digital Signal Processors). Each technique has its particularities that make them more or less interesting for each application. However, a preliminary assessment of the optimal technique for the converter design is not possible. In addition to the efficiency, they directly impact the sizing of the filters. A study dedicated to PWM techniques and the impact of different techniques on the whole converter design (cooling system and filters) will be presented in Chapter 4. The following section will show the multicarrier method for use in multi-level (series and parallel) topologies.

2.4.1 Multicarrier Carrier PWM

Multicarrier PWM techniques are used for three-level or more than three levels converter topologies. They are classified into types: Level-Shifted (LS-PWM) and Phase-Shifted (PS-PWM). The number of carriers $N_{carrier}$ is calculated as $N_{levels} - 1$, where N_{levels} are the output levels.

LS-PWM is divided in Phase Disposition PWM (PD-PWM), where all carriers are in phase; Phase Opposition Disposition PWM (POD-PWM), where all the carriers above zero are out of phase with those below the zero by 180º; Alternative Phase Opposition Disposition (APOD-PWM), where all the adjacent carrier signals are out of phase by 180º. These divisions are presented in Figure 30.



PD - PWM *POD - PWM* *APOD - PWM*

Figure 30 - Level Shifted PWM (LS-PWM)[104].

For NPC topologies PD-PWM technique was considered in this thesis since, among the LS techniques, the output voltages have better spectra [102][103]. Nevertheless, LS-PWM is not recommended for FC topologies since flying capacitors present high voltage deviations. The spectral quality of the output voltage waveform is adversely affected, and losses are not equally divided between the semiconductors [107].

PS-PWM technique uses multiple carriers which equally phase or time-shifted from each other. There is constant phase angle delay α_c between carriers that are expressed as $180/N_{carriers}$. This technique allows the reduction of flying capacitors and an equal division of losses between semiconductors on FC topologies. Therefore, it will be considered for the control of FC topologies. Figure 31 shows an example of a five-level FC with four carriers shifted by a quarter of the switching frequency period.

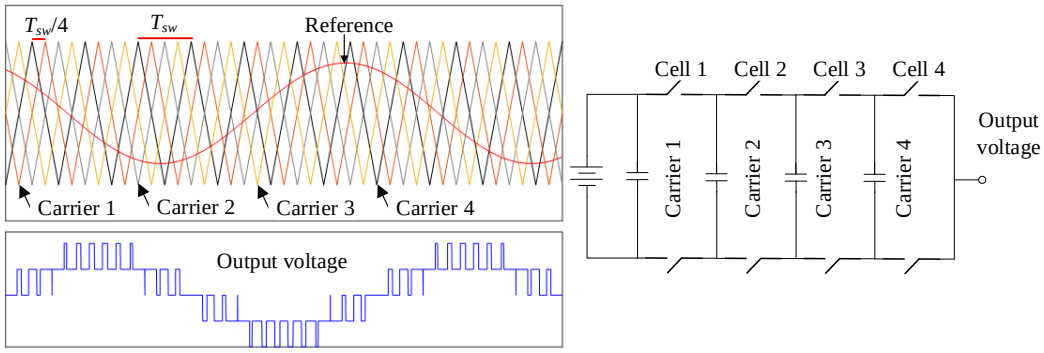


Figure 31 - Phase Shifted PWM (PS-PWM). Five-level Flying Capacitor.

This technique is also used for multilevel parallel topologies, as described in Section 2.2.2. In that case, for each carrier used to control multilevel series topologies (PD- PWM or PS-PWM), it is necessary another carrier phase-shifted of $2\pi/p$ on the switching frequency period for each one of the paralleled legs.

2.5 Semiconductors Losses Calculation

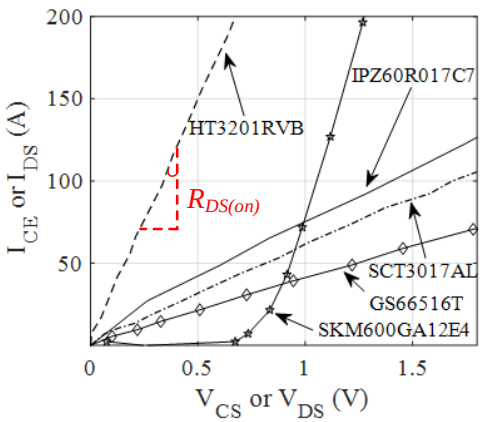
Power converter losses are composed of different parts, as PCB losses, magnetics losses, gate driver losses, and semiconductors losses. Semiconductor losses may represent the largest share of the converter overall losses. Therefore, semiconductors practically dictate converter efficiency, influencing converter weight due to a cooling system's necessity.

An accurate calculation of semiconductor losses is necessary to decide about semiconductor technology and converter topology. Some precise methods measure converter losses using a calorimetric chamber, but it must have the whole converter [105] [106]. A predictive estimation of semiconductor losses is a crucial point to an optimized design of a power converter. This predictive design must consider the semiconductor's static and dynamic characteristics, the type of modulation techniques used to control the power converter, and the load characteristic.

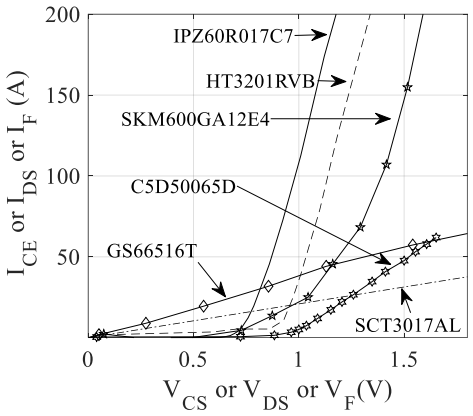
Semiconductor losses are mainly divided into conduction losses and switching losses. Some converter topologies, as the NPC, can present different losses between the switches. Therefore, it is

necessary to identify each device's current waveform to precisely estimate losses and then compute all switches' losses.

Conduction losses ($P_{switch,cond}$) are calculated using semiconductors' static characteristics (as presented in Figure 32), as the curves V_{DS} x I_{DS} for MOSFETs, V_{CE} x I_{CE} for IGBTs, and V_F x I_F diodes.



(a) IGBT, MOSFET, and GaN HEMT first quadrant static characteristic

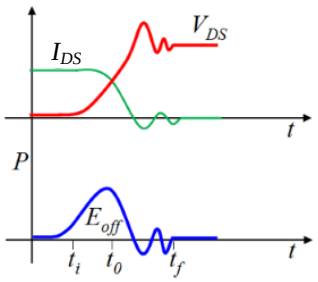


(b)IGBT, MOSFET, and GaN HEMT third quadrant and Diode static characteristics

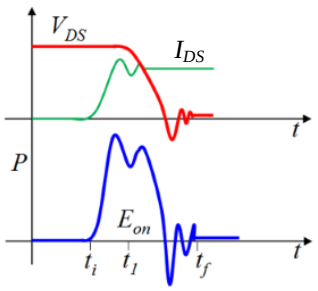
Figure 32 - Static characteristics of the semiconductors considered in this thesis: SKM600GA12E4 (IGBT), HT3201RVB (1200V MOSFET SiC), GS66516T (GaN HEMTs), IPZ60R017C7 (600V MOSFET Si), SCT3017AL (650V MOSFET SiC) and C5D50065D(650V Diode SiC).

For MOSFETs, this curve can be linearized as an equivalent $R_{DS(on)}$. This equivalent resistance is temperature-dependent, and a temperature correction must be used. In IGBTs and Diodes, the same approach can be made for the conduction zone with an equivalent resistance R_{CE} (IGBT) or R_F (Diode) (also called transconductance characteristic). However, a voltage drop V_{CE0} (IGBT) or V_{F0} (Diode) at zero current will be part of these devices conduction losses. The static characteristics (first and third quadrant) of the devices used in this thesis are presented in Figure 32 at 25ºC for the highest gate voltage available on datasheets. The third quadrant characterizes the antiparallel diode characteristic that will contribute to conduction losses during dead time.

Switching losses occur due to the simultaneous presence of significant drain-source voltage and drain current during each transient from the turn-off state into a turn-on state and vice versa. These situations are presented in Figure 33.



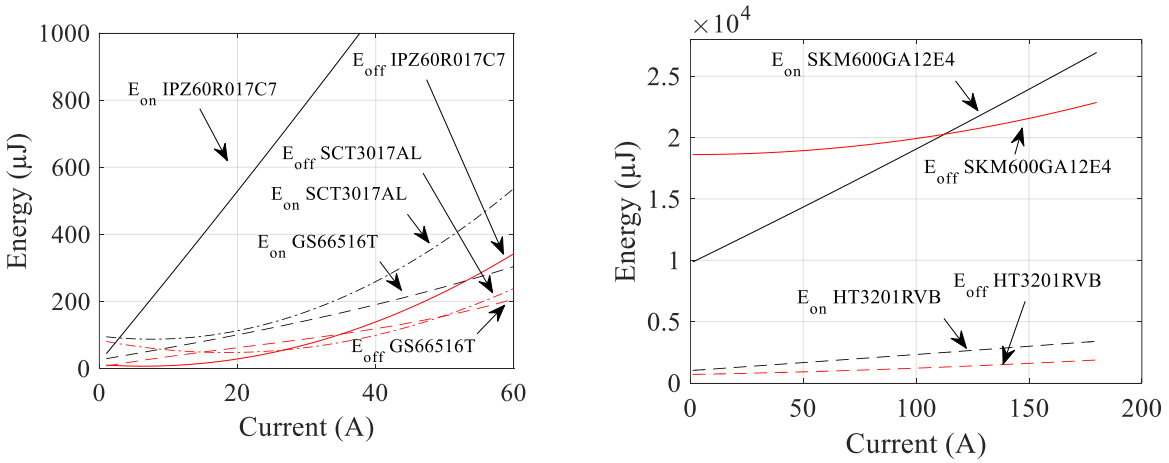
(a) Turn off



(b) Turn on

Figure 33 - Semiconductor commutation and the energies associated during turn on and turn off.

The energies associated with these situations, E_{off} and E_{on}, are the energy stored on switches parasitic capacitances. This information is measured by manufacturers using the double pulse test [110] for a given bus voltage and different current levels. This method has been questioned in the last years due to some drawbacks that can distort real values of switching energies[46], [111]–[113]. A precise method to characterize switching energies is described in [45] and improved by [109], named Modified Opposition Method, which compensates for the double pulse test drawbacks. On the other hand, it is necessary to characterize each device that prevents a more precise calculation in this thesis due to time constraints. Thus, switching energies provided by devices datasheets were used, as shown in Figure 34, by applying bus voltage correction where $V_{dc\text{-}datasheet}$ is the voltage used on the device characterization and V_{dc} bus voltage applied to the device in the current application as described in Eq. 2.16.



(a) MOSFET Si and SiC and GaN HEMT 650V for V_{dc} = 270V.

(b) Module SiC and IGBT 1200 V for V_{dc} = 540 V

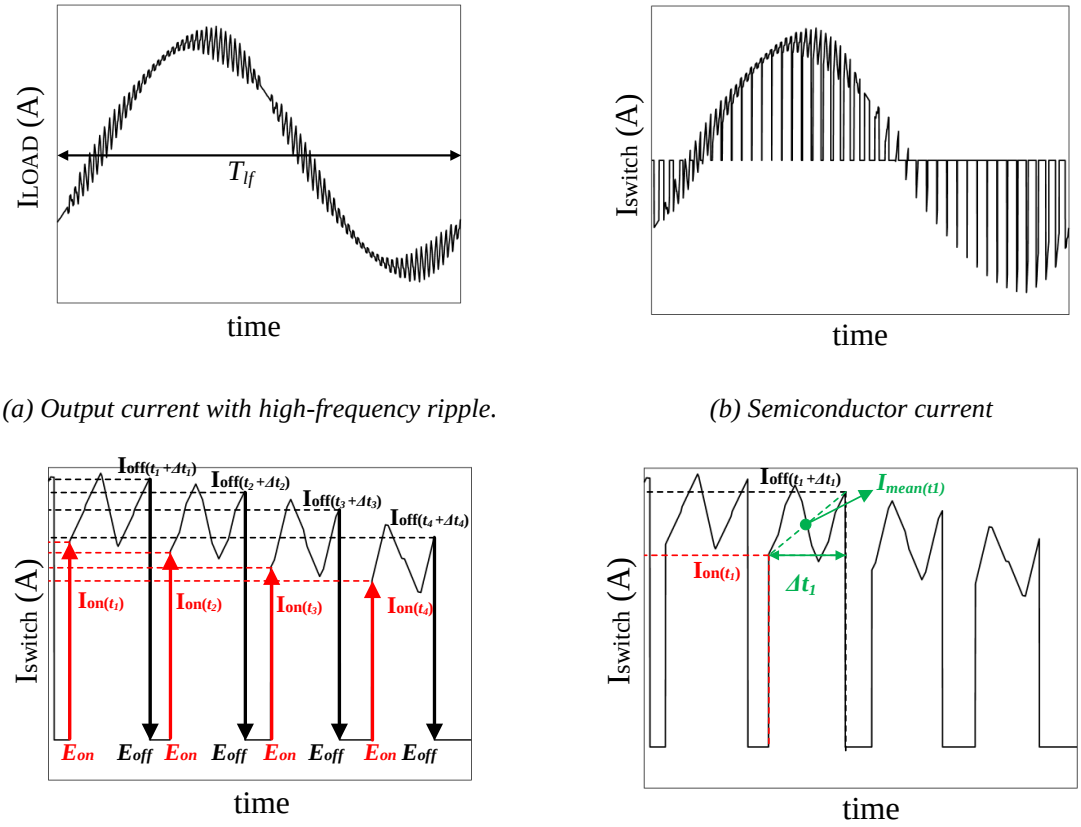
Figure 34 - Turn-on (E_{on}) and turn-off (E_{off}) energies considered in this thesis: SKM600GA12E4 (IGBT), HT3201RVB (1200V MOSFET SiC), GS66516T (GaN HEMTs), IPZ60R017C7 (600V MOSFET Si), SCT3017AL (650V MOSFET SiC) and C5D50065D (650V Diode SiC).

$$E_{on,off}(V_{dc}, I) = \frac{V_{dc}}{V_{dc,datasheet}} . E_{on,off}(I), \tag{2.16}$$

2.5.1 Losses Calculation Approach

Conduction and switching losses depend on the output current waveform, composed of a fundamental frequency f_{lf} (with period T_{lf}) and the ripple according to Figure 35 - a). The fundamental part depends mainly on the load (typically a sinusoidal current at low frequency). In contrast, the ripple depends on each switching period's duty cycle and the inductance in each converter leg's output. In a three-phase system where the neutral point of the load is floating, the current ripple of phase *U*, for example, depends not only on the duty cycle of phase *U* but also on the neutral point voltage, which depends on the duty cycle of the three phases [114]. For the theoretical study presented in this chapter, the neutral point will be considered fixed as presented in Figure 35 - a) since it represents the worst case with more current ripple than with floating neutral point. Since different topologies (series and parallel)

are considered in this thesis, the losses are computed considering each switch's current waveform presented in Figure 35 - b). The total losses are calculated considering the losses of all switches.



(a) Output current with high-frequency ripple.

(b) Semiconductor current

(c) Switching energies as a function of load current.

(d) Calculation of mean current value in a switching period t_{sw}.

Figure 35 - Output and switch current waveforms.

For each commutation with switching frequency $f_{sw,}$ the current level is identified for the turn on and turn off, presented in Figure 35 – c), as the instant time when switching happens since current ripple can change significantly switching losses [111]. Therefore, switching losses $P_{sw,switch}$ can be calculated as:

$$P_{sw,switch} = \frac{f_{lf}}{2} \sum_{x=1}^{n_c} \left(E_{on}\left(t_x\right) + E_{off}\left(t_x + \Delta t_x\right) \right), \tag{2.17}$$

Where n_c is the commutation number, t_x is the time instant where there is a turn on, and after $\Delta t_{x,}$ there is the turn off for the exact switching period. Considering $|Iswitch|$ waveform, switching losses will be calculated two times. The current negative semi cycle will not be switched by the referred switch but by the complementary one. Therefore, the 1/2 factor is considered. For IGBT and MOSFETs, there is also energy lost by the diode in parallel with the complementary switch when a turn-on occurs. This energy is known as reverse recovery energy (E_{rr}). Manufacturers datasheets provide this information, and it is accounted on E_{on} as following:

$$E_{on}\left(t_x\right)=E_{on,switch}\left(t_x\right)+E_{rr}\left(t_x\right), \tag{2.18}$$

Conduction losses can be calculated by considering the current *RMS* value of low frequency and ripple as presented in [114] for a two-level three-phase inverter. Nevertheless, this calculation is generalized in this thesis independent of the inverter topology by calculating the conduction losses associated with each switching period with the current mean. For MOSFETs and GaN HEMTs, it is calculated as:

$$P_{cond,switch}=\frac{R_{ds(on)}}{T_{lf}}\sum_{x=1}^{n_c}\left[\left(\frac{I_{on}\left(t_x\right)+I_{off}\left(t_x+\Delta t_x\right)}{2}\right)^2.\Delta t_x\right], \tag{2.19}$$

While for IGBTs, it is calculated as follows:

$$P_{cond,switch}=\frac{1}{T_{lf}}\sum_{x=1}^{n_c}\left\{\left[\begin{array}{l}V_{CE0}.\left(\frac{I_{on}\left(t_x\right)+I_{off}\left(t_x+\Delta t_x\right)}{2}\right)+\ldots\\ \ldots+R_{CE}.\left(\frac{I_{on}\left(t_x\right)+I_{off}\left(t_x+\Delta t_x\right)}{2}\right)^2\end{array}\right].\Delta t_x\right\}. \tag{2.20}$$

Since IGBT cannot conduct reverse current, the third quadrant characteristic has performed a diode placed parallel with the switch. Diode conduction loses for IGBT, and clamped diodes of NPC topology is calculated as:

$$P_{cond,diode}=\frac{1}{T_{lf}}.\sum_{x=1}^{n_c}\left\{\left[\begin{array}{l}V_F.\left(\frac{I_{on,diode}\left(t_x\right)+I_{off,diode}\left(t_x+\Delta t_x\right)}{2}\right)+\ldots\\ \ldots+R_F.\left(\frac{I_{on,diode}\left(t_x\right)+I_{off,diode}\left(t_x+\Delta t_x\right)}{2}\right)^2\end{array}\right].\Delta t_x\right\} \tag{2.21}$$

NPC clamping diode C5D50065D is a SiC Schottky diode with zero reverse recovery current. Therefore, the switching losses of this device were assumed 0.

An indefinite number of solutions can be evaluated from the different series and parallel topologies and the different semiconductor technologies presented in the previous sections. PWM techniques also play an essential role in the converter's performance, either in the efficiency and the cooling system or in the design of filters passive elements. Thus, there is a need for disruption in presenting the technological blocks described in this work. The calculation of the cooling system has a strong dependence on the number and distribution of the semiconductors in the heat sinks, making it difficult to generalize the model that will be presented. Thus, it has opted for a preliminary study of the performance of different topologies of converters. The number of legs in parallel, semiconductors in parallel, and levels in series will be varied. The following section presents this study of pre-selection of topologies that will guide the choice and development of technological blocks referring to the cooling system and filters to be designed.

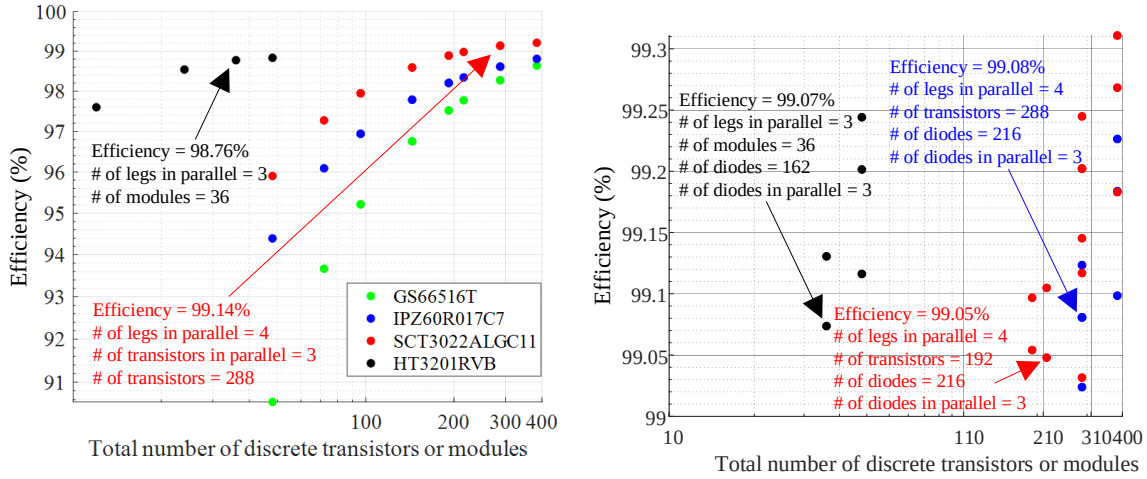
2.6 Multilevel topologies trade-off: Efficiency x Number of Semiconductors

A study for the preselection of inverter topologies was made considering the presented inverter models, PWM control, and datasheet information of semiconductors listed in Section 2.3.1. This study aims to select different inverter topologies based on the number of devices necessary to reach an efficiency of 99%. For this study, the motor considered in this thesis has an operating point of 3600 rpm/132 N.m/50 kW/130 A_{rms} with a bus voltage of 540 V. Those pieces of information lead to an inverter with nominal power of 70 kVA, fundamental frequency of 240 Hz, a power factor of 36.67° and modulation index of 0.9414. For this preliminary calculation, a switching frequency was fixed at 20 kHz while the following parameters were varied:

- Legs connected in parallel = 1 to 4;
- Inverter topologies: 2-level, NPC (3-level and 5-level) and FC (3-level and 5-level);
- Semiconductors in parallel (transistors and diodes) = 1 to 4.

Inverter control was performed with the DPWM1 technique [97][112]. With this technique, semiconductors are not switched when the current reaches its highest value, reducing switching losses and overall inverter losses. The impact of different PWM techniques on semiconductor losses will be addressed in Chapter 4. The optimal technique will be chosen for the final design of the converter proposed at the end of Chapter 2. Transistors losses were calculated from datasheet information for $T_{j\text{-max}} - 15°C$. The choice for high-temperature operation is to reduce cooling system weight addressed in this chapter's following section. An increment of 15% was considered in the inverter losses to roughly estimate the filter losses, which will be precisely calculated in this chapter's following sections.

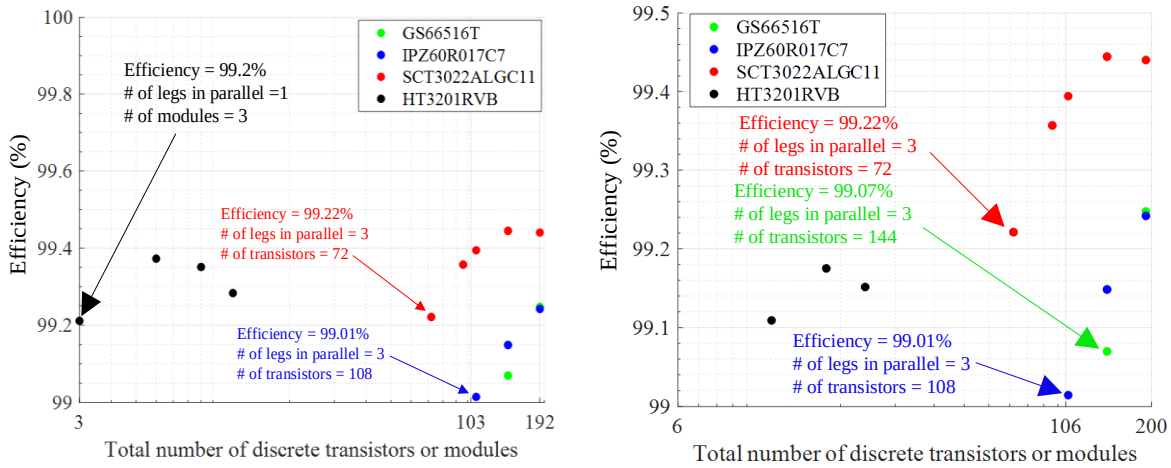
Almost 288 transistors are required to make a 5-level FC inverter with an efficiency over 99% with 650 V SiC MOSFET transistor, whereas 192 transistors and 216 diodes are required for a 5-level NPC inverter, as shown in Figure 36. For all solutions with efficiency levels above 99%, the number of legs per phase is 3. Many transistors in series, added to the paralleled legs, further complicate inverter control and integration. Therefore, these topologies will not be considered for future analysis.



(a) 5 - level FC *(b) 5 - level NPC*

Figure 36 - Calculated efficiency for a different number of transistors used in 5-level inverter topologies.

Figure 37 (a) presents the results for the 2-level topology with the 1200 V SiC MOSFET (black). The series association of 650 V components is also considered, while Figure 37(b) presents the solutions for 3-level FC topology.



(a) 2 - level *(b) 3-level FC*

Figure 37 - Calculated efficiency for a different number of transistors used in 2-level and 3-level FC inverters.

A 2-level converter is traditionally composed of 2 transistors per leg. If low voltage devices are used, it is necessary to associate some devices in series. In 650 V devices, two devices must be connected in series per switch to handle the desired blocking voltage. These devices should switch simultaneously to ensure that the input voltage is equally shared among series devices. In this context, the Quasi FC topology was proposed by [116], and it was based on a Quasi 2-level created from a 3-level NPC. In this topology, the flying capacitor of the FC topology, which has a high capacitance to generate output levels, is substituted for a small capacitor (C_{QFC}) responsible for transient voltage balancing (C_{QFC} voltage ≈ 0 V), so the schematic is identical to a 3-level FC topology as shown in Figure 38.

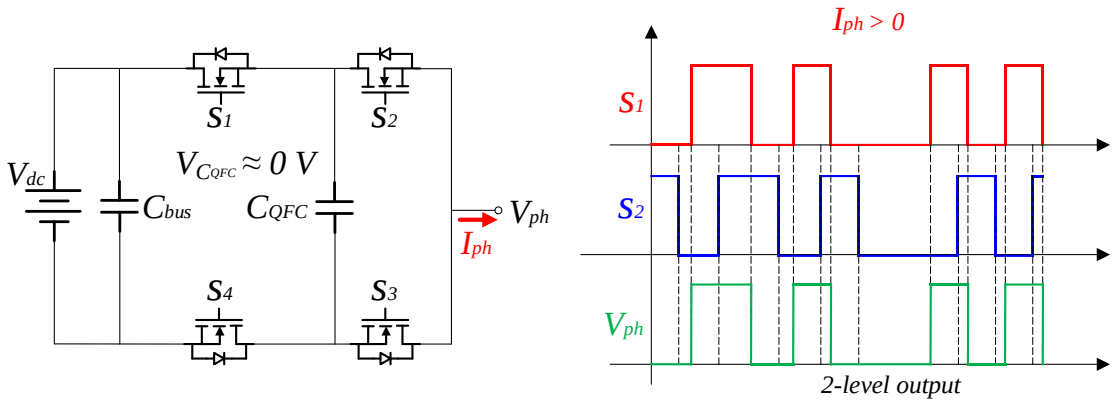


Figure 38 - Quasi FC switching states and output voltage.

Thus, the total voltage is equally shared among the series devices, and, thus, all switch block and switch the same voltage. This topology facilitates series connections of semiconductors with low blocking voltage, reduces drastically flying capacitors weight, and has no severe capacitor voltage balancing. The Quasi FC considered in this study is created from a 3-level FC that will generate only two output levels per leg but with the same number of losses as a 3-level FC with the same modulation carriers as presented in Figure 38.

The results of the Quasi FC topology are represented by the solutions in green, blue, and red in Figure 37 (a), which corresponds to the 650 V devices. The number of output levels per phase, with a Quasi FC topology, $N_{level,\ phase}$ as a function of the number of legs in parallel (p), and the number of output voltage levels of one leg (N) is calculated as:

$$N_{level,\ phase} = (N-1).p+1. \tag{2.22}$$

The solutions in Figure 37 for 2-level topologies with 650 V devices and 3-level FC are identical regarding the efficiency, transistors, and parallel legs. This equality is because they are controlled with the same carries.

Figure 39 presents the solutions for 3-level NPC. The total number of transistors for the highlighted topologies equals the number of transistors for 3-level FC topology solutions. However, besides using a considerable number of diodes (at least 36), NPC solutions efficiency is slightly lower than the 3-level FC solutions.

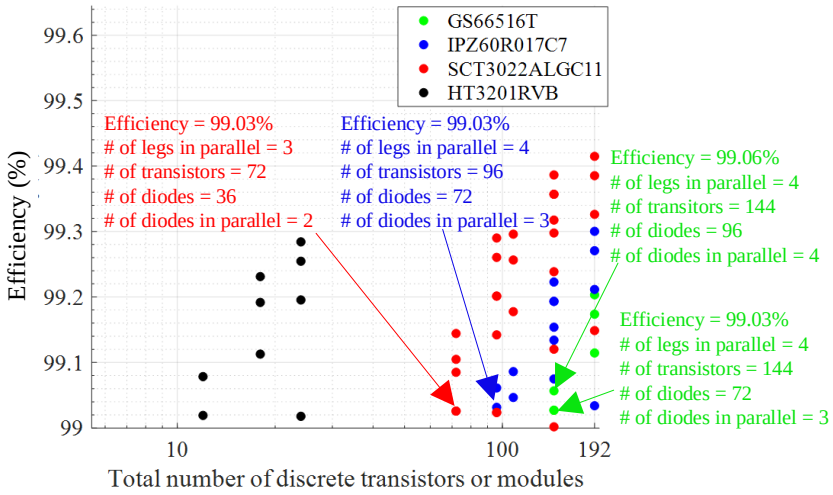


Figure 39 - Calculated efficiency for a different number of transistors used in a 3-level NPC inverter.

This lower efficiency is due to NPC topology higher conduction losses of the inner switches. The solutions with the same number of transistors in Figure 39 with higher efficiencies have different clamping diodes in parallel. The high the efficiency, the high the number of paralleled diodes.

Calculation results of different inverter topologies and semiconductors resulted in 709 different combinations. Ten topologies were selected based on the number of semiconductors and efficiency; they are summarized in Table 10. The 1200V SiC MOSFET 2-level inverter presents a calculated efficiency of 99.21% from datasheet information, while the 1200 V IGBT 2-Level, 97%. Due to the challenges in using and integrating GaN transistors and the possibility of inverter compression due to this transistor's size, four topologies were initially selected: one Quasi FC, one 3-level FC and two 3-level NPC.

Table 10 - Power Inverter possibilities selected from Efficiency x Number of Semiconductors trade-off

Topology	Semiconductor	Legs/phase	# Transistors/Modules	# Diodes
2-level	1200V IGBT SKM600GA12E4	1	3	-
2-level	1200V SiC MOSFET HT3201RVB	1	3	-
Quasi FC	650V GaN GS66516T	3	144	-
FC 3-level	650V GaN GS66516T	3	144	-
FC 3-level	600V Si MOSFET IPZ60R017C7	3	108	-
FC 3-level	650V SiC MOSFET SCT3017AL	3	72	-
NPC 3-level	650V GaN GS66516T	4	144	72
NPC 3-level	650V GaN GS66516T	3	72	36
NPC 3-level	600V Si MOSFET IPZ60R017C7	4	96	72
NPC 3-level	650V SiC MOSFET SCT3017AL	3	72	72

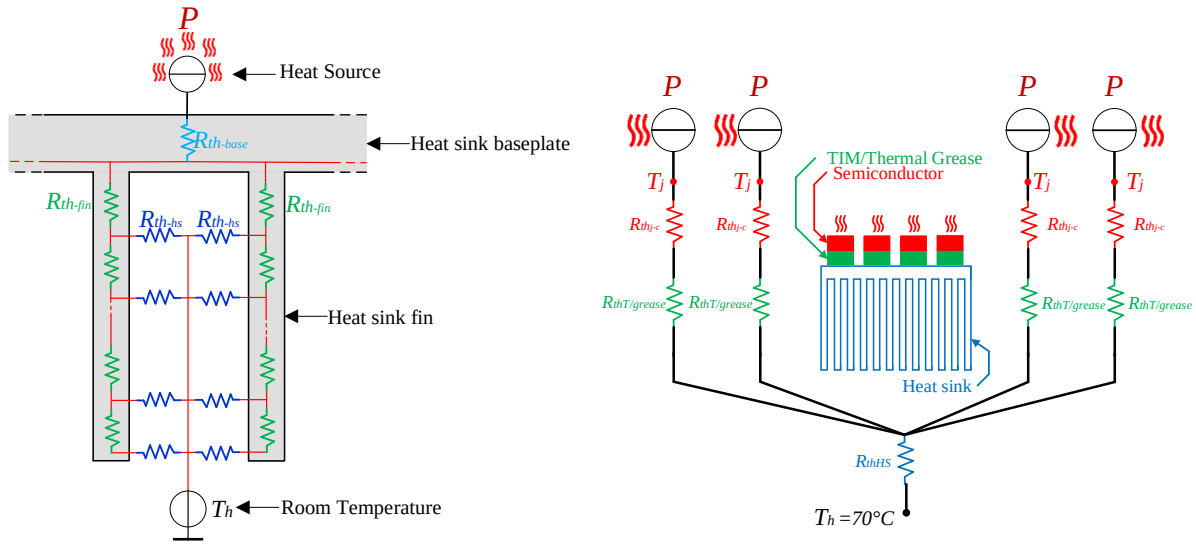
Topologies selected in this section will be used for global inverter optimization at the end of this chapter. In this way, it will be possible to verify the impact of multilevel topologies on overall inverter efficiency, power density, and the influence of different transistor technologies. Due to the high efficiency required, many transistors (in the case of 650V components) must reduce the inverter's

conduction losses. Parallel legs are also necessary since switches' direct parallel connection to reduce total on-state resistance remains challenging, especially for GaN transistors [114][115]. Furthermore, parallel legs increase the number of inverter voltage levels, and some problems can be mitigated, such as overvoltage at the motor terminals and maximum output current ripple.

On the other hand, the number of gate drivers is increased, and controller I/O ports and current balancing control must be used to ensure equal division of currents between paralleled legs. In this case, current sensors must be placed in each leg output [75], increasing control complexity. These factors are causally related to an inverter weight increase.

2.7 Cooling Systems

The cooling system must be with forced air as presented in Section 1.3.2, and the traditional cooling system composed of a finned heat sink with fans will be considered. According to [119], [120], this system can be analytically modeled, and the relation between heat sink thermal resistance and the respective weight of the cooling system can be calculated. The heat sink project is generally considered from an equivalent thermal resistance based on the circuit model shown in Figure 40 (a). The resistance $R_{th\text{-}base}$ (in light blue) represents the heat resistance of the heatsink base plate. This resistance does not consider the 2D effects in the baseplate when several heat sources (several power components on the same sink, which is often the case presented in Figure 40 (b)). Resistances $R_{th\text{-}fin}$ (in green) describe the conduction phenomenon in the fins.

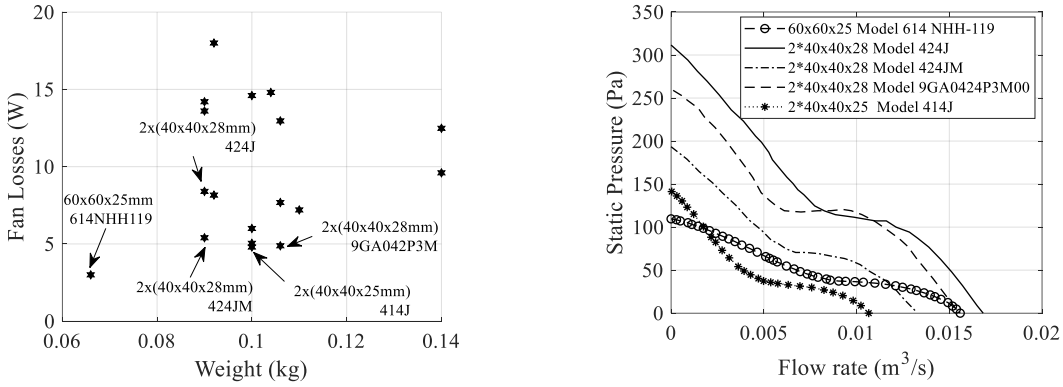


(a) Heat sink equivalent thermal circuit *(b) Heat sink multi-source*

Figure 40 - Heat sink modeling.

The resistors $R_{th\text{-}hs}$ (in dark blue) describe the phenomenon of convective exchange between the fins and the air flowing between them. Heat exchanges between the fins and the air circulating between them were modeled by a network of 10 modules composed of a resistance $R_{th\text{-}fin}$ with a resistance $R_{th\text{-}hs}$ in parallel. This modeling allows us to consider the temperature gradient effect and the fins and model the heat sink as equivalent thermal resistance $R_{th\text{-}HS}$.

The cooling system design is a compromise between the heat sink and fan characteristics. This procedure is precisely described in [120], which compose the work investigated deeply [119]. Another thesis, as [121] and [17] used the same procedure. A preselection of fans (see Figure 41) regarding their losses and pressure *x* air flow rate characteristics was used to input the cooling system design. The procedure consists of various optimization parameters (see Figure 42), such as the number of fins and heat sink dimensions (fin height, baseplate thickness, etc.). Several solutions are calculated as the relation between heat sink plus fan minimal weight thermal resistance R_{th} as presented in Figure 43. The heat source surface was calculated considering one equivalent source with each semiconductor's surface and the number of conductors presented in Section 2.6. It was considered one heat sink per phase containing one-third of the total semiconductors. NPC topologies considered two heat sinks per phase, one for the transistors and the other for the diodes.



(a) *(b)*

Figure 41 - Fans selection characteristics: (a) Losses x Weight trade-off and (b) pressure drop profiles.

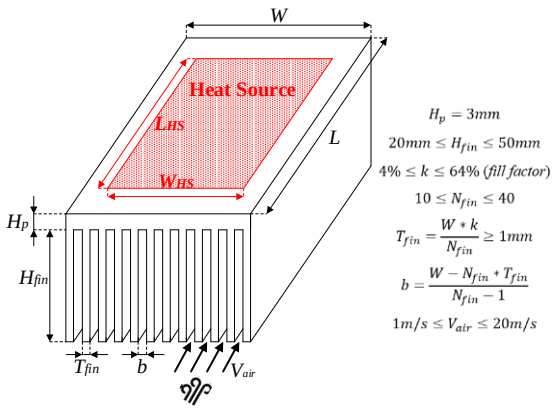


Figure 42 - Heat sink dimensions and parameters used to calculate the equivalent thermal resistance.

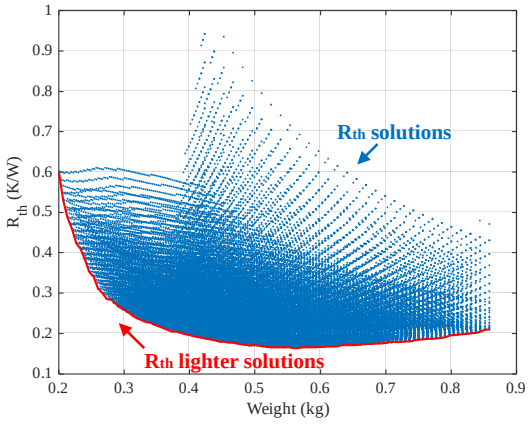


Figure 43 - Evolution of the overall thermal resistance of the heat sink as a function of weight. The Pareto front shown in red indicates the whole optimal solutions for the criteria of the problem.

The thermal exchange between discrete transistor and heat sink is commonly made by a lead frame, named thermal pad, electrically connected to the Drain pad on MOSFETs. On the other hand, in

GaN transistors, this thermal pad can be electrically insulated (GaNPX package from GaN Systems) from Drain and Source pads or even internally connected to the Source pad of GS66516T from GaN Systems. It implies that the connection between the heat sink and different transistors, connected in series, must be done through an electrically insulating material. These materials are commonly referred to as Thermal Interface Materials (TIMs). They must present a high thermal conductivity, so the temperature difference between the heat sink and transistor thermal pad is minimized. However, due to microscopic imperfections on the transistor thermal pad surface, a thermal paste with high thermal conductivity (Ex: 1.8 W/m·K, for thermal grease 8616 from MG Chemicals) is used between the semiconductor and the TIM or heat sink. These imperfections can trap air that has low thermal conductivity (0.02572 W/m.K in 25°C), hamper semiconductor heat exchange and lead to overheating.

Different TIMs were identified to be used for the discrete semiconductors, as presented in Table 11. This table presents the equivalent thermal resistance of each TIM for each semiconductor. Hi-Flow 300P is not the one with lower resistance, but it can be easily bought from internet distributors, then it will be considered in this thesis.

Table 11 - Thermal Interface Material (TIM) Resistance (K/W).

	Hi-Flow 300P	Sil-Pad® 1500ST	SARCON® XRm	GAP3000S30R	Mica
C5D50065D (Diode)	0.369	0.654	0.102	0.491	10.094
GS66516T (GaN)	1.366	2.418	0.378	1.815	4.045
IPZ60R017C7(Si Mosfet)	0.369	0.654	0.102	0.491	1.094
SCT3017ALHR (SiC Mosfet)	0.369	0.654	0.102	0.491	1.094
HT3201RVB	Insulated interface (no need of TIM)				

From semiconductors losses and their respective junction to case thermal resistance ($R_{thj\text{-}c}$) available in the datasheet, the necessary cooling system thermal resistance R_{thHS} can be calculated according to:

$$R_{thHS} = \frac{T_j - T_h}{n.P} - \frac{R_{thj-c}}{n} - \frac{R_{thT/grease}}{n}. \tag{2.23}$$

T_j is semiconductor junction temperature, T_h is the ambient temperature (fixed in 70°), n is the number of semiconductors per heat sink, P is the loss of one semiconductor. $R_{thT/grease}$ is the equivalent series thermal resistance of the TIM and thermal grease calculated considering each semiconductor thermal pad surface.

Figure 44 presents the evolution of cooling system weight with switching frequency for the topologies listed in Section 2.6 for different PWM techniques. Since NPC topologies also have clamping diodes, they present the heaviest heat sinks. Whatever the PWM technique, the hierarchy of the curves remains the same, pink curves (NPC topologies) are always heavier than the others, the blue (2-level with the 1200 V SiC) is the lightest at low frequencies etc. Another interesting point is that the growth of the curves with the switching frequency depends on inverter topologies and semiconductor technologies. Each solution, composed of an inverter topology and the number of semiconductors, is

associated with a different R_{th} x Weight curve, strongly dependent on heat sink dimensions and the heat source (formed by the surface of semiconductors).

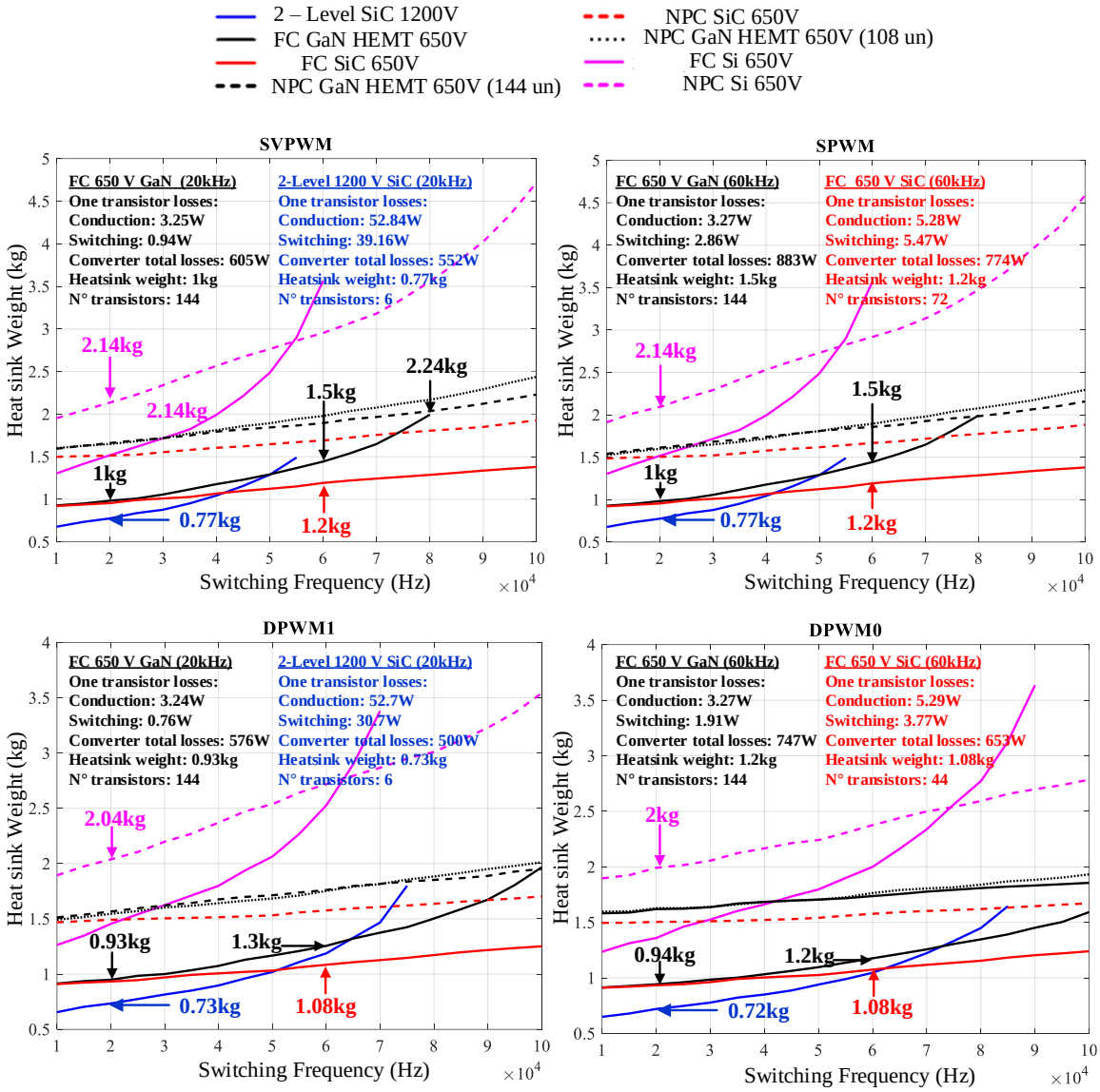


Figure 44 - Heat sink optimal weight as a function of switching frequencies for the eight different possibilities described in Section 2.6.

Around 2 kg at 20 kHz with DPWM1 is verified for the topology with 600 V Si MOSFET, while the FC topology with the same number of transistors has 1.5 kg. Heat sinks for 600 V Si MOSFETs are heavier than other solutions with different semiconductors for identical topologies due to the number of transistors and their respective heat surface (1.72×10^{-4} m^2 - packaging TO-247). It is 50% heavier for the same topology for FC topologies with 650 V SiC MOSFET and 650 V GaN HEMT for 20 kHz and SVPWM. For switching frequencies until 20 kHz and FC topologies, heat sinks for 650 V SiC MOSFET and 650 V GaN HEMT present the same weight. The 2-level topology with 1200V SiC MOSFET presents lighter solutions since conduction losses are much lower than the other solutions. The difference is about 230 g (25%) at 20 kHz compared with FC solutions. Quasi FC topology will have the same losses as FC with 650 V SiC MOSFET. Then, the heat sink is considered the same. In the case of the 2-level with 1200V IGBT that is not presented in Figure 44, the heat sink

weight was calculated as 1.3 kg for 10 kHz and 3.83 kg for 20 kHz, it represents almost 2x and 4x respectively, the weight for the 2-level with 1200 V SiC MOSFET for the same condition (DPWM1 technique).

According to heat sink results, the FC topology with 650 V SiC MOSFET seems incredibly attractive, with 653 W against 747 W compared to the same topology with 650 V GaN HEMT for DPWM0 at 60 kHz. Nevertheless, it is worth pointing out that 650 V SiC MOSFET is on the TO 247 package with non-negligible terminals stray inductance. Switching losses for the 650 V GaN HEMT FC converter represent 36.8% of the total semiconductor losses. This ratio is 63.4% for the 1200 V SiC MOSFET, while for the 650 V SiC MOSFET, it represents only 42%. The main advantage of GaN transistors is the low switching losses, and according to the results, the difference ratio is not that important between these two 650 V devices. The data for switching energies is questionable for the SCT3017AL since switching energies are performed with gate resistor for 0 Ω. A detailed characterization of this device is may be necessary for a more reasonable losses calculation.

The lightest solutions were found for DPWM1 and DPWM0, while for SVPWM and SPWM, the solutions were similar. DPWM1technique will be considered for the filter design in the following sections. Chapter 3 of this thesis will consider a more detailed study about the impact of different PWM techniques on the overall weight and efficiency of the selected topology presented at the end of this chapter.

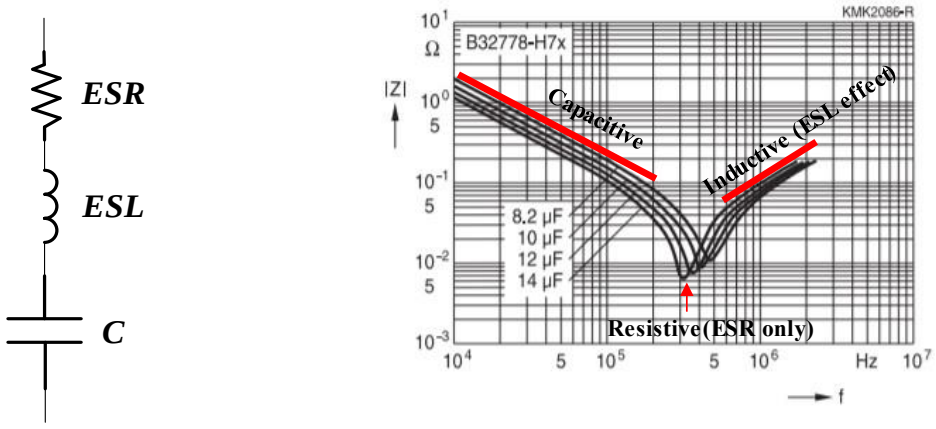
Until this point, this thesis manuscript presented a pre-selection of semiconductors technologies and inverter topologies that guarantee at least 99% efficiency. Additionally, the estimation of the cooling system weight for the pre-selected topologies was evaluated. The following section will present the design procedures of passive elements, such as capacitors and inductors, to design different filters to meet the different constraints listed in Section 1.3.2.

2.8 Passive components

The study described in this chapter considers only passive elements for filter design. These passive elements are divided into two big groups: magnetic cores and capacitors. The parasitic related to these devices significantly impact filter response, as ESL (equivalent series inductance) and ESR (equivalent series resistance) for capacitors. While for inductors, the main parameters that limit filter response and design are stray capacitances, leakage inductance contribution on core saturation, the frequency response of core permeability, and conductor skin effect. Therefore, it is essential to consider the model closer to the real device. This section presents design procedures for capacitors and inductors based on datasheet information and devices databases, input and output filters, and the different materials recommended for each application.

2.8.1 Capacitor Design

Ideal capacitors shall present stable impedance that decreases with frequency. Consequently, it reduces the parasitic voltage in high frequencies. However, real devices present dielectric and electrode losses modeled by an equivalent resistance (ESR). High-frequency impedance increases and has an inductive behavior modeled by an equivalent inductance (ESL). Figure 45 presents the equivalent circuit of a real capacitor and the increase of its impedance with the frequency.



(a) *(b)*

Figure 45 - Real capacitor (a) equivalent circuit and (b) impedance dependency with the frequency for the B32778H family of TDK.

Capacitor parasitic elements depend on capacitor technology as well as the capacitance varies with applied voltage. The capacitor technology choice depends on the desired application, and some parameters must be considered to a proper capacitor design, like frequency response, voltage, and current levels. The most common capacitor technologies used for EMC [119][120] are:

- Paper type capacitors (epoxy impregned paper);
- Metallized polyester film capacitors (MKT);
- Metallized polypropylene capacitors (MKP);
- Ceramic capacitors.

Ceramic capacitors are the most compact with lower ESL than others but only for low capacitance values. Epoxy impregned paper capacitors are more reliable and support higher temperatures, but they can be 30% to 90% bigger than other technologies for the same capacitance value. They also present high ESR and consequently higher losses. MKP capacitors present lower ESR and are commonly used for high-frequency filtering. Therefore, MKP capacitors are more indicate for EMC filters, while Ceramic capacitors are used where fast switching is needed. Table 12 presents capacitor technologies considered in this thesis for the different filters and flying capacitors.

Table 12 - Capacitor technologies used for filter design and flying capacitors.

Technology	Application	Voltage Range	# Partnumbers in database	Supplier
MKP DC Link (B32774H ... B32778H)	DM Input filter	450V – 1000V	256	TDK®
MKP Y2 (B32032 ... B32036)	CM Input and Output filter	350V	16	TDK®
MKP X2 (B32921C/D ... B32928C/D)	DM Output filter	630V	21	TDK®
Ceramic (B58035U)	Flying capacitor	500V- 1000V	9	TDK® Ceralink®

Capacitor databases present voltage and current levels for each part number and respective ESR and ESL, which the supplier gives. Therefore, it is possible to estimate capacitors losses and impedance frequency response. The calculation of the desired capacitor based on the database was implemented according to:

First, one part number is selected with the respective blocking voltage $U_{nominal}$, the number of series capacitors N_{CS} is calculated to block the voltage U_{max}.

$$N_{CS} = \frac{U_{max}}{U_{nominal}} \tag{2.24}$$

The number of paralleled capacitors $N_{CP\text{-}V}$ is calculated based on N_{CS} to have the desired capacitance C based on the device's nominal capacitance $C_{nominal}$.

$$N_{CP\text{-}V} = \frac{C}{C_{nominal}}.N_{CS}\text{, } if \frac{C}{C_{nominal}}.N_{CS} < 0.8.\ Otherwise\ N_{CP\text{-}V} = 1. \tag{2.25}$$

Nevertheless, the current level must also be evaluated. The number of paralleled capacitors $N_{CP\text{-}I}$ to hold nominal current I_{rms} is calculated as based on the nominal current $I_{nominal}$ of the device:

$$N_{CP\text{-}I} = \frac{I_{rms}}{I_{nominal}} \tag{2.26}$$

The number of paralleled capacitors is calculated as the highest between $N_{CP\text{-}I}$ and $N_{CP\text{-}V}$. The number of total capacitors is calculated as N_{CS}*$N_{CP,}$ and C_{eq} defines the part number's equivalent capacitor.

$$N_{CP} = \max\left(N_{CP\text{-}V}, N_{CP\text{-}I}\right), \tag{2.27}$$

$$C_{eq} = \frac{C_{nominal}}{N_{CS}}.N_{CP} \tag{2.28}$$

This procedure is done for all part numbers of the database, and the equivalent ESR, ESL, and capacitance of the lightest solution are calculated. Figure 46 represents this procedure in a flowchart for the DM Input filter. The other capacitors follow the same procedure, especially for the flying capacitor calculation.

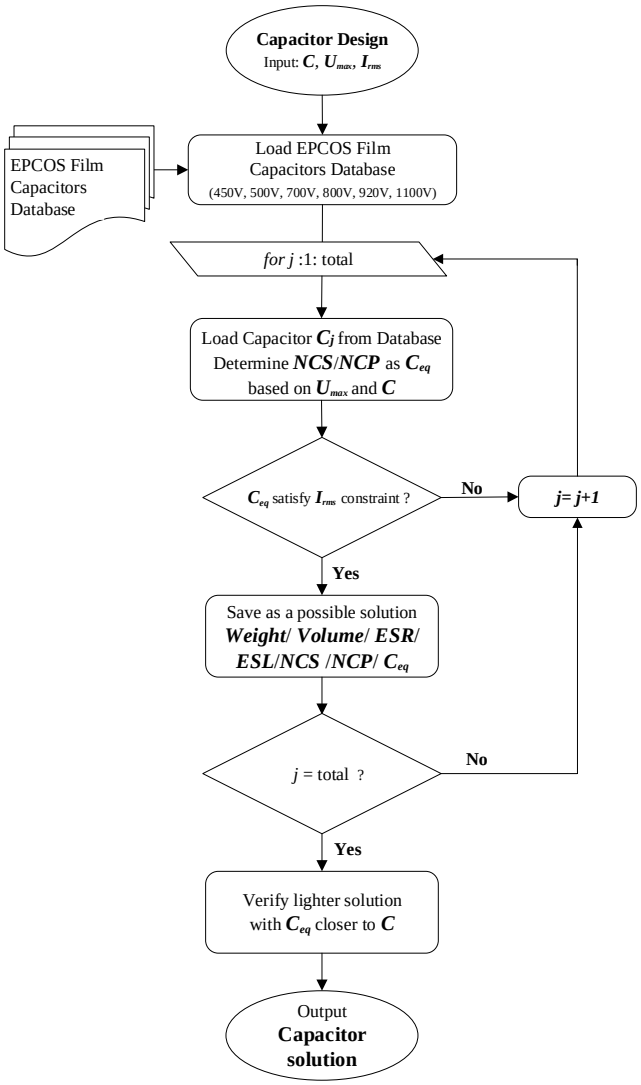


Figure 46 - Capacitor flow chart design for the lightest solution comprises design input constraints based on a database with devices of different current and blocking voltage levels.

The procedure described above is based on the association of capacitors in parallel and series to meet the voltage and current input criteria. Thus, a given part number will always have an association of capacitors that will meet these criteria. Nevertheless, the predominant convergence criteria are the ratio between C_{eq}/C. The capacitor association C_{eq} can diverge in just 5% to C.

This section presented the procedure to estimate the capacitor's weight based on the database, among input parameters such as capacitor current, blocking voltage, and desired capacitance. However, this last parameter must be estimated according to acceptable voltage ripple criteria for the application. The calculation of the capacitance necessary to guarantee the maximum voltage ripple is addressed in the following section, considering the flying capacitor and DC-Link capacitor.

2.8.1.1 Flying Capacitor and DC-Link Capacitor Design

Capacitance C_{FC} is unrelated to the fundamental frequency of the output voltage[1] [2] and has the inherent self-voltage balancing property of flying capacitors [126]–[128]. High values of C_{FC} directly impact the weight and losses of the power converter and make the converter sensitive to factors that can cause an imbalance [127]. In [129], a minimum acceptable voltage ripple is discussed for flying capacitors to avoid parasitic switching states in paralleled FC converters working as a DC-DC converters. These states will provide one undesirable current path to generate a surplus charge on flying capacitors and abruptly discharge back to the voltage source. This surplus charge can increase semiconductor conduction losses but also overstress semiconductors and flying capacitors. No works were found relating the impact of flying capacitor voltage ripple and circulating currents on DC-AC parallel converters, and it could be one research area of interest. Considering the optimization propose in this chapter, the same criteria were considered for the inverter input voltage ripple (ΔV_{FC} = 5%). The capacitance to guarantee a maximum ripple value is determined by the current passing through this capacitor as:

$$C_{FC} = \frac{1}{\Delta V_{FC(max)}} . \int \tilde{i} dt. \tag{2.29}$$

The current that passes through this capacitor must have a mean value equal to zero. Otherwise, the voltage in this capacitor will increase indefinitely. Then, this capacitor will be charged for half of the period, and the other half will be discharged according to the current sense. It means that the mean value of the voltage ripple must be zero. Then, voltage ripple can be understood as:

$$\Delta V_{FC(max)} = V_{ripple(max)} - V_{ripple(\min)} = \frac{q_{(max)} - q_{(\min)}}{C} = \frac{\left[max\left(\int \tilde{i} dt \right) - min\left(\int \tilde{i} dt \right) \right]}{C}, \tag{2.30}$$

and

$$mean(\Delta V_{FC(max)}) = \frac{V_{ripple(max)} + V_{ripple(\min)}}{2} = \frac{q_{(max)} + q_{(\min)}}{2.C} = 0, \tag{2.31}$$

leading to

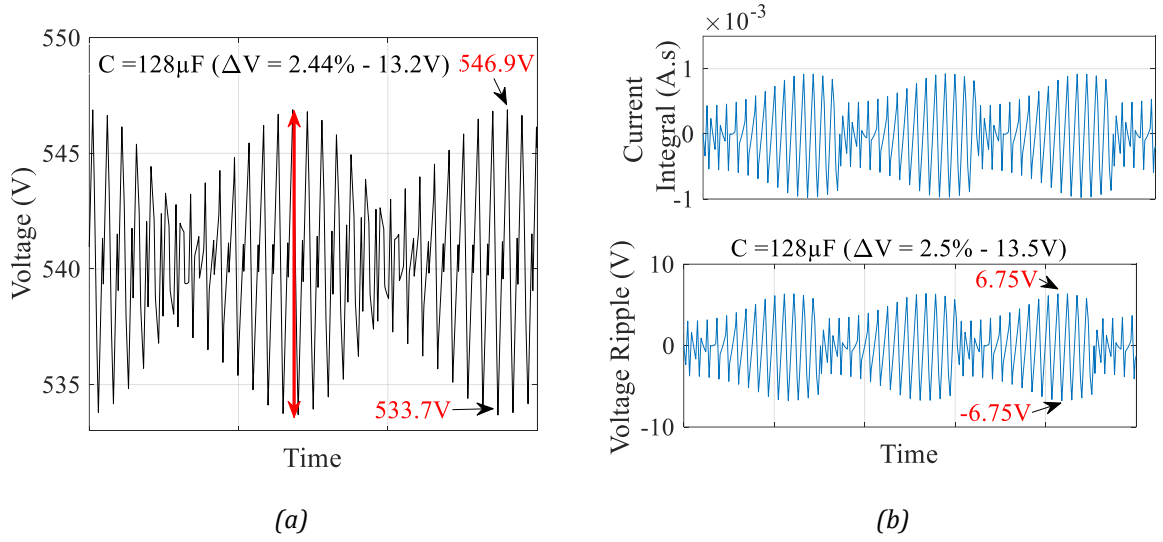
$$\left| max\left(\int \tilde{i} dt \right) \right| = \left| min\left(\int \tilde{i} dt \right) \right| \therefore \Delta V_{FC(max)} = \frac{2.max\left(\int \tilde{i} dt \right)}{C}. \tag{2.32}$$

Thus, the maximum voltage ripple in a capacitor, either a flying capacitor or a DC link capacitor, can be expressed as:

$$C = \frac{2.max\left(\int \tilde{i}dt\right)}{\Delta V_{FC(max)}}. \tag{2.33}$$

The validity of Equation 2.33 to calculate DC link capacitor is intrinsically related to DC bus upstream impedance in parallel with the capacitor. The design of the DC link capacitor in this thesis considered that the bus impedance is sufficiently big, which means that the voltage ripple is mainly due to the inverter input current. Thus, it allows the use of Equation 2.33.

The waveform presented in Figure 47 (a) represents the simulation on PSIM® of a 3-level FC in a three-phase configuration for V_{dc} = 540 V, f_{sw} = 20 kHz, SPWM, 70 kVA, and power factor of 36°. In that case, the equations developed above are evaluated for the bus capacitor presented in Figure 47 (b), considering the modeling of FC presented previously. According to circuit simulation, a 2.44% voltage ripple is expected for C_{bus} = 128 µF, while considering the maximum value of the capacitor current integral for the same C_{bus}, the same voltage ripple is identified. It also reinforces the idea that the maximum and the minimum value of the current integral has the same value in the module.



(a) *(b)*

Figure 47 - DC link capacitor voltage ripple (a)PSIM simulation and (b) Current integral validation for a 2-level inverter operating with V_{dc} = 540 V, f_{lf} = 240 Hz, f_{sw} = 20 kHz, SPWM, 70 kVA, cos(ϕ) = 0.6435 and C_{bus} = 128 µF.

The same procedure and operating point used for Figure 47 was applied regarding the flying capacitor. Figure 48 shows the current passing through C_{FC} calculated to have ΔV_{FC} = 5% for the FC topologies with three-legs in parallel per phase selected in Section 0.

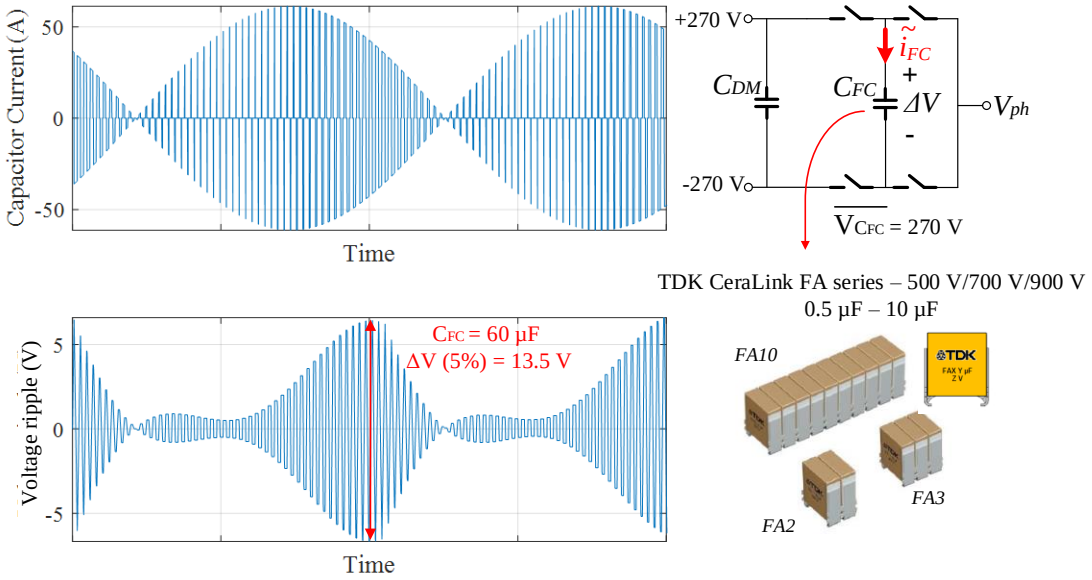


Figure 48 - Flying Capacitor voltage ripple for a 3-level FC inverter with 3 paralleled legs per phase operating with V_{dc} = 540 V, f_{lf} = 240 Hz, f_{sw} = 20 kHz, SPWM, 70 kVA, cos(ϕ) = 0.6435 and C_{FC} = 60 µF.

For the inverter nominal power, weight, losses, and capacitances for one leg of the selected FC topologies were calculated, as presented in Figure 49, for different switching frequencies considering the database of TDK® Ceralink FA capacitors and the optimization procedure presented in 2.8.1.

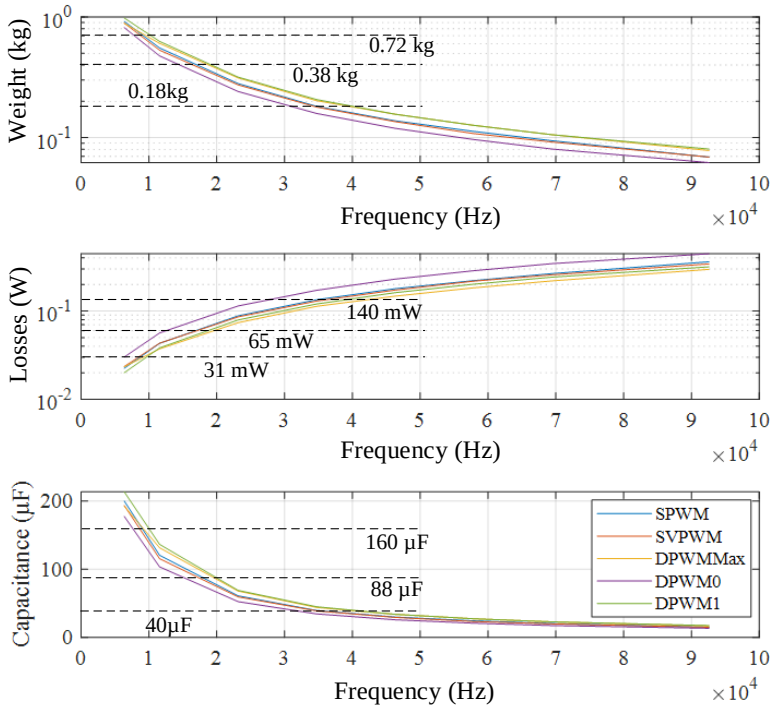


Figure 49 - Flying Capacitor voltage ripple for a 3-level FC inverter with 3 paralleled legs per phase operating with V_{dc} = 540 V, f_{lf} =240 Hz, f_{sw} = 70 kVA, cos(ϕ) = 0.6435 and C_{FC} = 60 µF.

At 10 kHz, 160 µF is necessary to hold voltage ripple with 0.72 kg, which means 6.5 kg for the entire converter with nine legs for the DPWM1 technique. In the case of 40 kHz, its weight is reduced to 1.6 kg. On the other hand, the losses are almost negligible due to the low ESR of ceramic capacitors.

Another essential technological brick necessary for the passive filter design comprises the inductors. Each filter specificity demands different magnetic materials, and this problem is addressed in the following section regarding inductors design.

2.8.2 Inductor Design

Any magnetic core's fundamental purpose is to provide an easy path for flux to facilitate flux linkage, or coupling, between two or more magnetic elements. Magnetic core materials are classified as hard and soft materials. Magnetic soft materials have lower losses, can be easier magnetized, and has higher permeability than rigid materials. Therefore, they are used mainly in power electronics applications.

The universe of soft magnetic materials is subdivided into two other groups: Iron-based alloys and Ferrites. The first group is characterized by low electrical resistivity and high saturation limits (around 1.1 T to 1.5 T). On the other hand, Ferrites have high electrical resistivity and low saturation limits (around 0.45 T). Each material has its advantages and disadvantages; thus, the application requirements define the magnetic core materials used. Figure 50 presents different magnetic materials regarding their saturation flux density B_{sat} and their losses.

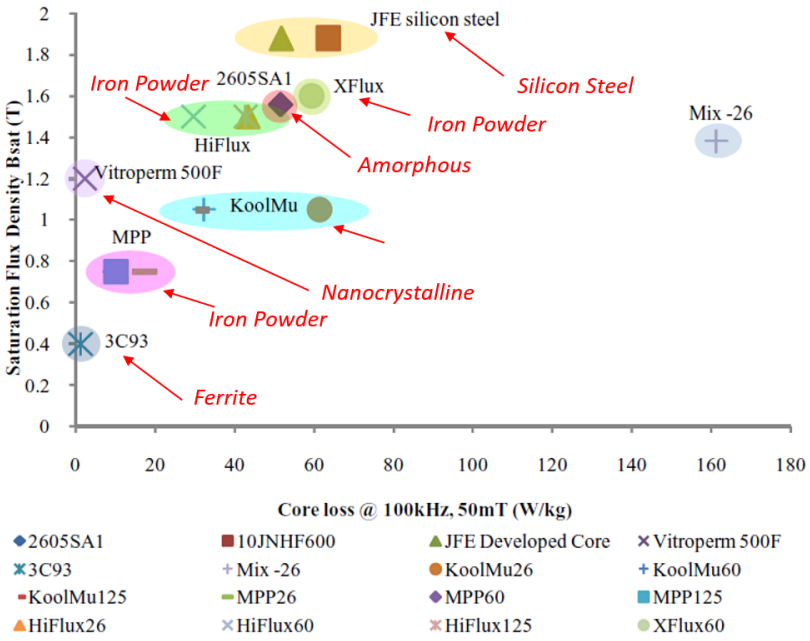


Figure 50 - Magnetic materials saturation flux x loss [130].

In general, Ferrites have lower losses than other materials but low saturation flux density. On the other hand, Nanocrystalline allows increased saturation flux density with lower core losses than

Ferrites. Iron Powder or Powder cores can achieve even higher saturation flux density values with much lower losses than Silicon steel materials used for low-frequency transformers.

Another method of comparing magnetic materials is presented in [131]. The volume of a magnetic core necessary to deliver a power P depends on the maximal allowable values of B_{sat} and f_{sw} (switching frequency). Then, the product of these two parameters (Λ) consists of a valuable figure of merit to compare magnetic materials used in power electronics. It is presented in Figure 51 that Λ increases for ferrites (3C96 and N27) and powder cores (permalloy), but it decreases for nanocrystalline (SNC), with switching frequency. Therefore, nanocrystalline materials are well suited to high induction and relatively low frequency (15 – 40 kHz) applications.

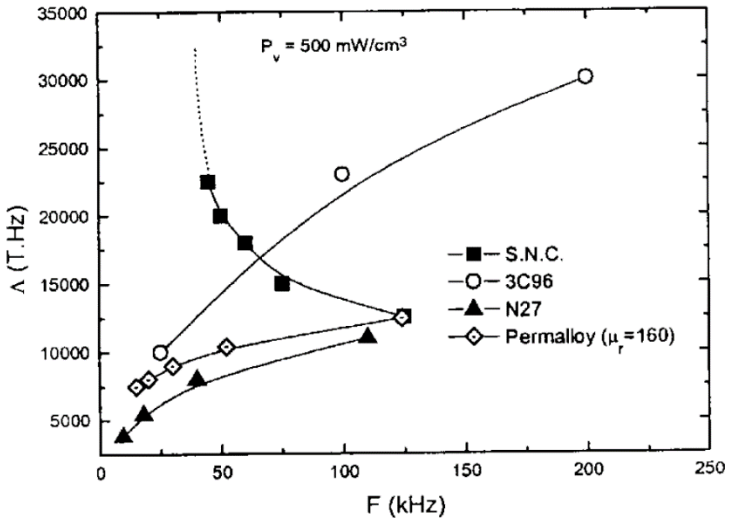


Figure 51 - Figure of merit for fixed losses as a function of frequency for stress nanocrystalline core (SNC), MnZn ferrites (3C96 and N27), and permalloy (powder core)[131].

Regarding the application of magnetic materials, the conducted emissions defined by the RTCA/DO-160G standard aim to limit electromagnetic interference (EMI) due to common mode currents until 150 MHz. Filter behavior must have high attenuation, even in high frequencies. Since parasitic plays an important role, the higher the core's permeability, the fewer turns necessary to achieve the desired inductance. In this case, Ferrites and Nanocrystalline cores are good candidates. Nanocrystalline cores are part of the Iron-based alloys and present higher permeability than ferrites (until 10x higher), as presented in Figure 52.

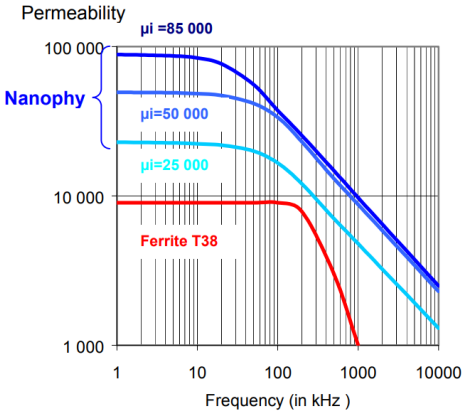


Figure 52- Permeability for Ferrite and Nanocrystalline Nanophy® cores.

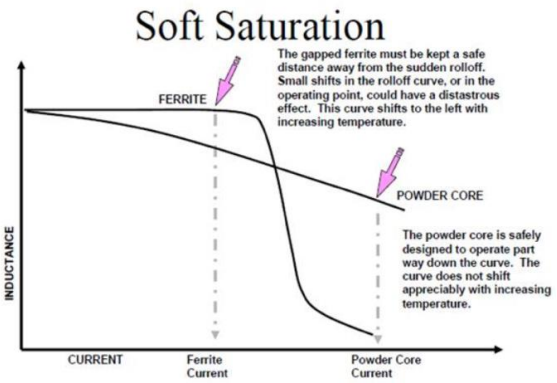


Figure 53 - Advantage of Powder cores against Ferrite for high current [132].

They have lower coercivity and less marked reduction of permeability at higher frequencies compared to Ferrites. With high permeability, the number of turns can be reduced, and winding losses and stray capacitances. Besides is has higher values (1.1 T) of saturation flux that will be crucial for not saturating the magnetic material. Another advantage of using Nanocrystalline is that the permeability does not change too much with temperature, while Ferrites permeability can be reduced by 40% at temperatures above 100 ºC [133]. The listed features show that Nanocrystalline cores are the best option for CM filters. Beyond the price, a disadvantage of this magnetic material is that there are only on toroid geometry due it is made by thin metallic tape-wound. Different geometries were analyzed by cutting this material [134], but magnetic characteristics are negatively impacted. Almost all the works on CM filter design consider this type of geometry, and then it is easier to calculate the filter's electrical characteristics. A database with 108 magnetic cores from VAC® and ArcelorMittal is considered in this thesis to design CM inductors, also called CM chokes.

In filters for Network Stability and Power Quality standard from 0 to 150 kHz, limit overvoltage on motor terminals and output inductors of multilevel parallel inductors. Low permeability magnetic cores are recommended. These devices will carry the power current to contribute to the core saturation and have non-negligible winding losses contributing to the core temperature rise. Another Iron-based alloy is commonly used for these types of applications, the powder cores. These materials have higher saturation limits (up to 1.5 T) than ferrites, and permeability does not change too much with temperature. They are even cheaper. Another advantage of powder cores is the gradual inductance drop when the core saturates (soft saturation). In ferrites, the inductance abruptly drops (hard saturation) when the magnetic core is saturated, as presented in Figure 53. Therefore, powder cores are more common in custom applications requiring soft saturation and higher saturation currents. This thesis uses a database of powder cores from Magnetics® with 106 cores based on the information available in [135]. Different powder core materials are considered, as MPP, Kool Mμ, and High Flux. MPP and Kool Mμ have lower permeability in higher frequencies, while High Flux has higher saturation limits [17][123].

Based on this section's information, we can synthesize that it is necessary to design a CM choke procedure for EMI filters with Nanocrystalline cores. Another design procedure is considered for DM filters, and output inductors handle high current values using Powder cores. Only toroid core was

considered for the design procedures, and the main physical parameters for the design of the inductors are listed in Table 13, referred to in Figure 54.

Table 13 - Parameters for the design of inductors.

Variable	Description	Unit
OD	Tore external diameter	(m)
ID	Tore internal diameter	(m)
H_c	Tore thickness	(m)
A_w	Window area	(m^2)
A_e	Tore cross area	(m^2)
l_e	Mean length of the magnetic flux	(m)
B	Magnetic flux density	(T)
B_{sat}	Maximum magnetic flux density	(T)
N	Number of turns	-
d_w	Wire diameter	(m)
MLT	Mean length turn	(m)

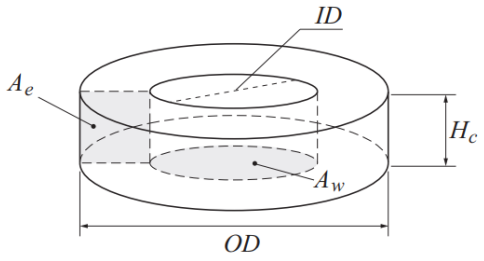


Figure 54 - Geometric dimensions of the magnetic tore[136].

2.8.2.1 DM input and output inductors design

The design of DM input and output inductors considers a database of Powder cores. The design procedure is represented in Figure 55. It has four input arguments: desired inductance L, switching frequency f_{sw}, inductor current waveform in the time domain (then peak current I_{pk} and RMS current I_{rms} can be calculated), and ambient temperature T_h (fixed 70 ºC). This procedure is similar to the one used in [17]. The core database is organized from lighter to heavier, according to area product equation design:

$$A_w.A_e \geq \frac{L.I_{pk}.I_{rms}}{k_w.B_{max}.J_{max}} \tag{2.34}$$

This equation relates the feasibility of the inductance with respective core physical characteristics A_w and A_e. B_{max} is considered 80% of nominal saturation flux density. J_{max} is the current

density considered on the windings (assumed as 5 A/mm^2 for enameled copper wire in free air used in toroid applications), and k_w represents the fill factor representing the ratio between A_w and total winding transversal section (commonly used as 40%).

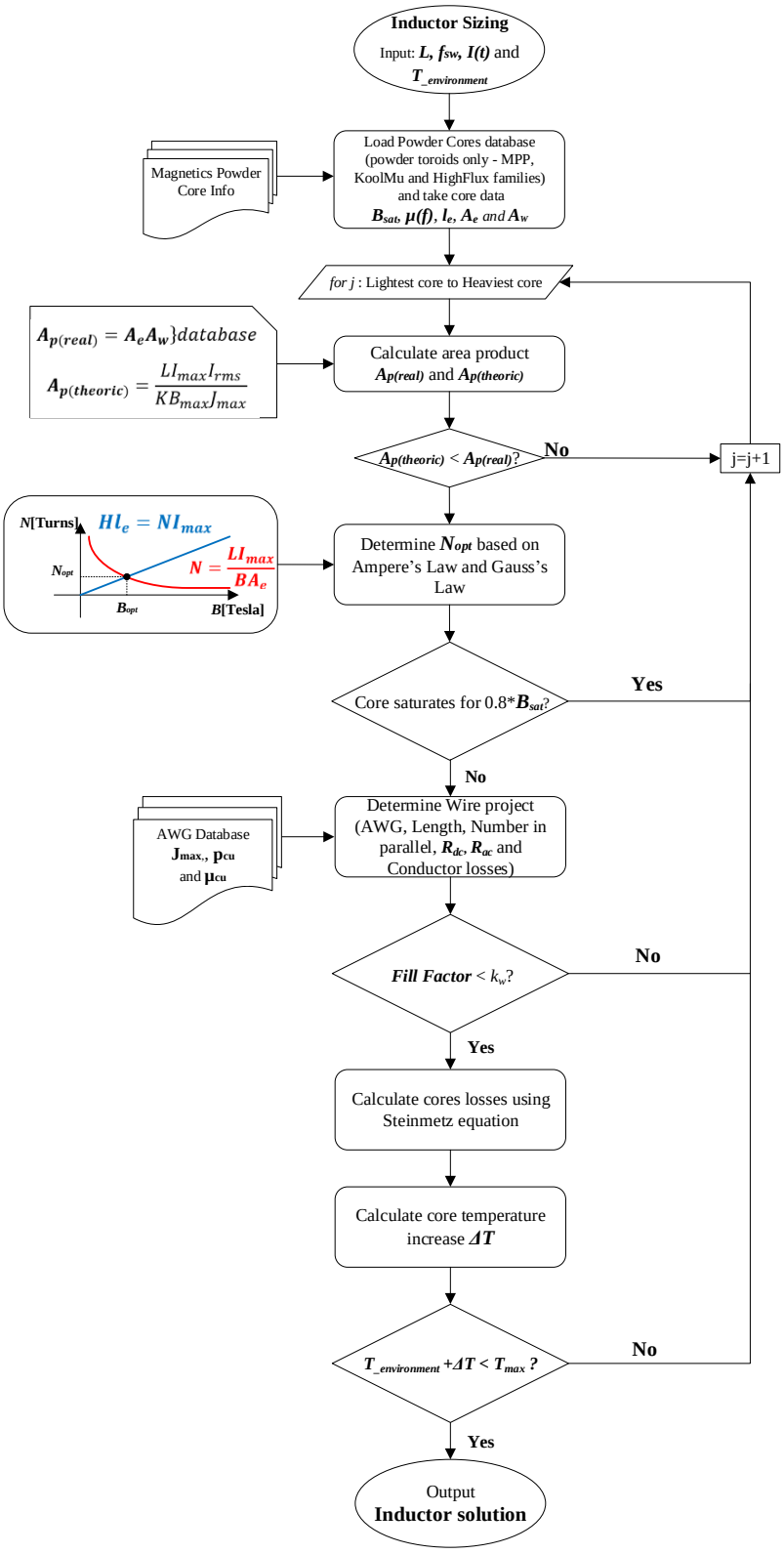


Figure 55 - DM Inductor Optimization Flowchart.

For each core, the optimal number of turns N_{opt} is calculated, then core saturation is verified:

$$B_{max} > \frac{L.I_{max}}{N_{opt}.A_e} \tag{2.35}$$

Then windings are designed respecting J_{max} with copper wire. From this calculus, the weight, volume, equivalent dc, and ac resistances (R_{dc} and R_{ac} are calculated according to [17] based on Dowel formulation[137]), and conductor losses P_w is calculated:

$$P_w = R_{dc}.I_{rms}^2 + \frac{1}{2}.\sum_{n=1}^{\infty} R_{ac_n}.I_n^2 \tag{2.36}$$

If this solution respects the fill factor limit k_w, core losses are evaluated according to *iGSE* (improved Generalized Steinmetz Equation) method [138]. This method can estimate core losses P_{core} based on non-sinusoidal time-domain waveforms of voltage or current applied to the inductor and Steinmetz parameters. This method is detailed in [139], and the design function is available in [140]. Core losses will increase core temperature; thus, it is verified if it does not exceed T_{max} (fixed at 100 ºC) recommended by [135]). Heat dissipation generated by conductor and core losses is influenced by different factors, which means there is no simple way to precisely predict the temperature rise. In [135] and [136], empirical equations are claimed to give a valuable estimation of temperature rise for an inductor in still air and with a 40% fill factor (the same value considered in this thesis). The equation provided by Magnetics® [135], which corresponds to the database considered on the design procedure, is given by:

$$\Delta T\left(^{o}C\right) = \left(\frac{\text{Core losses (mW)}}{\text{Core Surface Area (cm}^2\text{)}}\right)^{0.833} \tag{2.37}$$

Temperature rise is added to ambient temperature (T_h) to estimate core maximum temperature T_{max}. Core losses are estimated using the iGSE method, and core surface area is calculated from core dimensions.

The first solution that satisfies all design constraints in the design procedure, considering the database list from the lightest to the heaviest core, is considered the lightest solution. If one constraint is not satisfied, the following core on a database is evaluated until one solution is found. From this procedure, the inductor has a precise value of weight comprising core and windings, losses composed by winding and core losses (P_w+ P_{core}), R_{ac} and inductance variation with frequency. Since these inductors are not used for high frequencies attenuation, stray capacitances are not evaluated, and core equivalent resistance. Therefore, the DM inductor's equivalent circuit is represented as an *RL* series circuit with frequency-dependent parameters.

The design procedure presented above was validated experimentally according to Figure 56, where a 75.7 µH inductor was designed considering the High Flux 58585 core with 30 turns split into two coils. For the frequency range considered for the Power Quality and Network Stability (0 to 150 kHz), the measured impedance (red curve) is remarkably close to the designed (blue curve), even when it is connected to an interface PCB with power connectors. The difference between measured and

calculated impedance until 300 Hz can be addressed because exceptionally low impedances are being measured (under 100 mΩ), and contact connections may influence the measurement. It also shows that the calculated impedance has good representativeness until 2 MHz, even though windings parasitic capacitances are not considered.

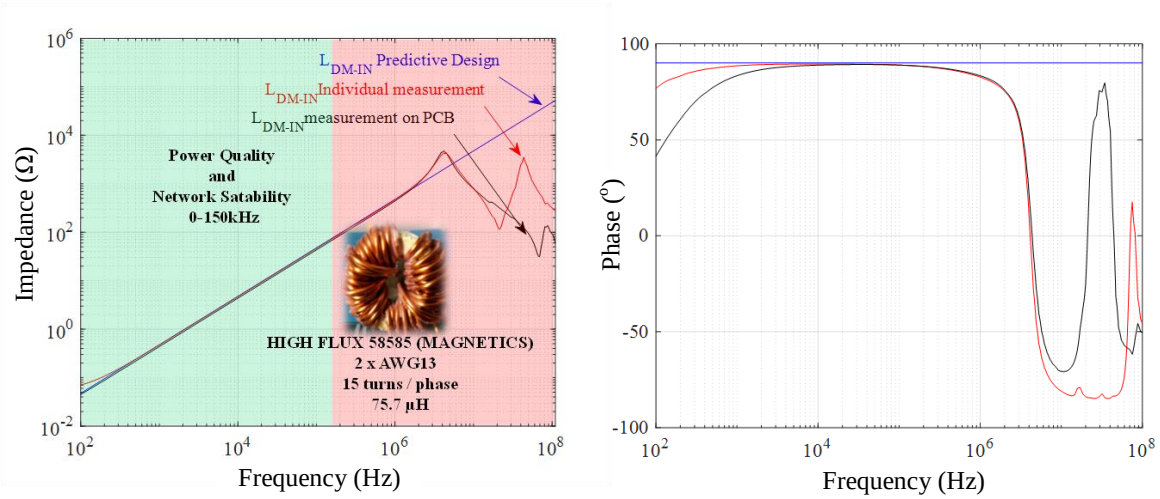


Figure 56 - Experimental verification of DM inductor design.

This section focused on the design procedure of DM inductors based on powder cores. The following section will describe the procedure and particularities of designing CM inductors, commonly called CM chokes.

2.8.2.2 CM input and output inductors design

The switching nature of power converters gives rise to high-frequency ground leakage current flow through parasitic capacitances resulting in the CM EMI [141]. Semiconductor, cables, and electric machine capacitances to the ground make the preferred path for these currents. Common-mode inductors or CM chokes are extensively used in applications where it is necessary to attenuate CM currents in passive or active filtering systems. Two different CM chokes used in the input of a power converter are presented in Figure 57 (a) and Figure 57 (b) with different winding designs.

(a) *(b)* *(c)*

Figure 57 - Common mode choke (a)half-moon, (b) dual wire wound, and (c) simplified magnetic field path for the leakage field.

These inductors can represent 25% [130][131] overall size of a motor drive system resulting in a meaningful impact on power density. Thus, it represents a critical element to reduce a power drive system weight. It has been the object of study of plenty of research groups around the world [17], [136], [141], [143]–[149] aiming to understand the behavior of these devices, as the impact of parasitic capacitances, core saturation, the principle of operation, etc. The impact of most of these parameters is intrinsically related to windings disposition on the magnetic core, as presented in Figure 57 (c). This thesis needs to consider one input and one output CM filter to limit Conducted Emissions on Power Lines and Interconnecting bundles. A CM choke with two coils is considered for inverter input, and three coils for output are considered.

According to the literature, the equivalent electric circuit in CM and DM of input and output chokes that should be considered satisfactorily represent these devices' real behavior is presented in Figure 58. Beyond the inductance drop with the frequency and R_{ac}, three other parameters are necessary for the CM choke model: stray capacitance C_s, core equivalent resistance $R_{core,}$ and leakage inductance L_{lk}.

The leakage inductance calculation of a CM choke is detailed in [146] for a two coil choke (input) and in [141], [144] for a three-phase choke. It has an essential impact on the core saturation that depends not only on CM flux but also the leakage flux according to the following equation:

$$B_{pk} = B_{cm} + B_{dm} = \frac{L_{cm} I_{cm\_pk} + L_{lk}\left(I_{cm\_pk} + I_{dm\_pk}\right)}{2A_e N}. \tag{2.38}$$

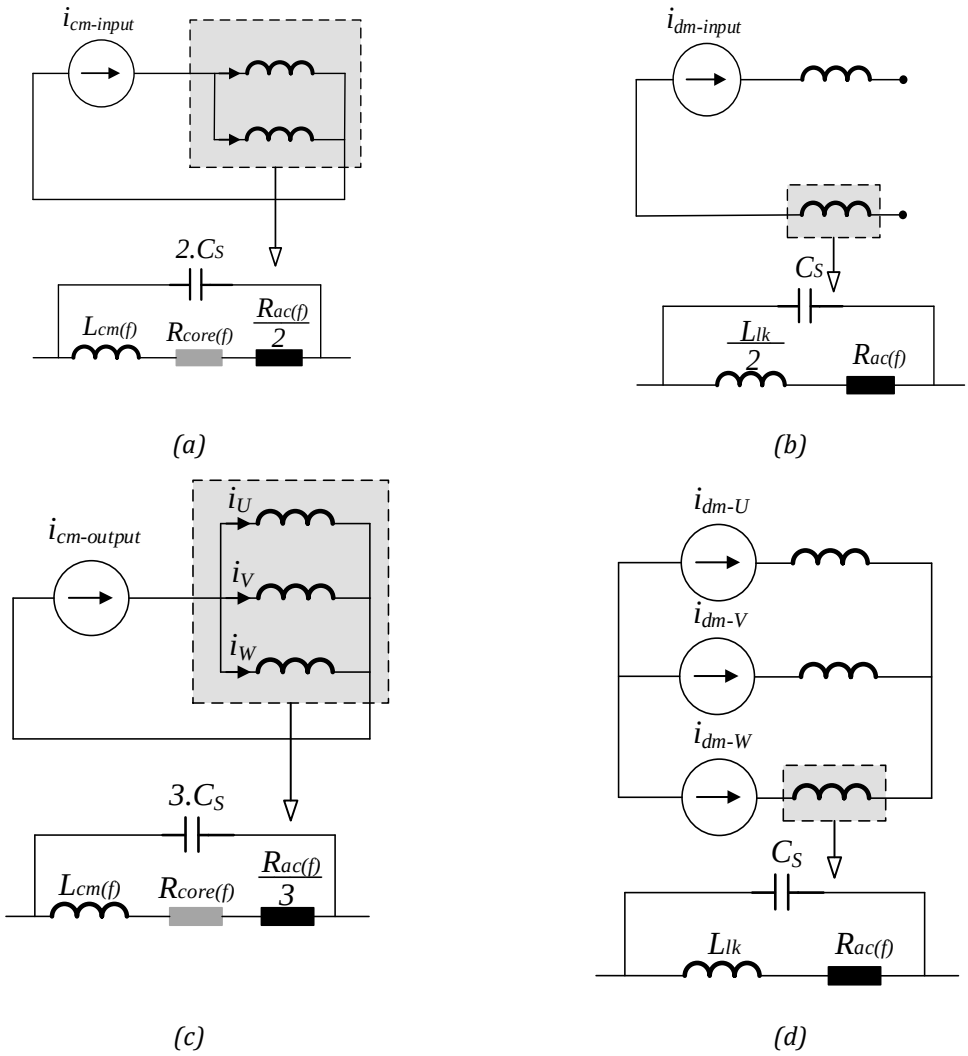


Figure 58 - Equivalents circuits for input and three-phase output CM inductors. (a) Equivalent circuit for input CM.(b) Equivalent circuit for input DM. (c) Equivalent circuit for output CM. (d) Equivalent circuit for output DM.

N is the number of turns, I_{cm_pk}, and I_{dm} as the peak CM and DM current amplitude. Leakage inductance depends mainly on the winding coverage θ (see Figure 57) and core physical parameters as presented in the following equation:

$$L_{lk} = 2.5\mu_0 N^2 \frac{A_e}{l_{cm}} \left(\frac{l_e}{2} \sqrt{\frac{\pi}{A_e}} \right)^{1.45} . \tag{2.39}$$

Where l_{cm} represents the mean length of the leakage path of each phase winding as described in [136]. Due to the lack of information about μ'' on datasheets, that is necessary information to estimate R_{core}:

$$R_{core} = A_L N^2 \omega . \frac{\mu''}{\left| \overline{\mu}(f = 0Hz) \right|}, \tag{2.40}$$

An approximation was made for all cores according to the information of the T6000-6-L2025-W380 core for ten mA, presented in Figure 59. For frequencies above 2 MHz, an extrapolation was considered.

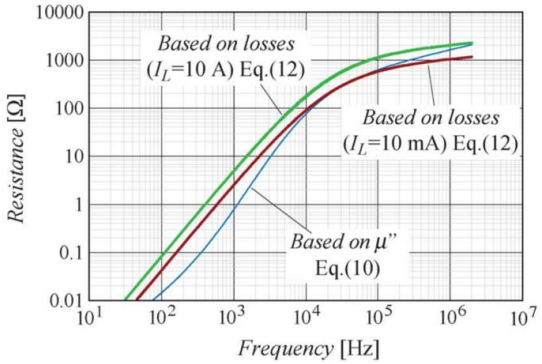


Figure 59 - Core resistance due to core losses for material VITROPERM 500 F, core T6000-6-L2025-W380, and windings of seven turns [136].

Core losses are typically neglected when performing the CM chokes' thermal design unless a very high switching frequency is employed or installing inductors between three-phase inverters and motors, where substantial CM voltages occur [150]. Thus, core losses of the CM choke were not calculated for the CM input filter. In contrast, for the output CM chokes, due to lack of information about Steinmetz parameters for Nanocrystalline cores, it was not considered either.

Stray capacitances of inductors remain one complex subject since they depend on the distance between turns, the number of winding layers, wire insulation materials, etc. It negatively impacts CM choked impedance since the resonance between the impedance decay is presented in Figure 60. Thus, low parasitic capacitance is desirable to guarantee high impedance in high frequency. In [151], and the analytical equation is proposed for single layer and multi-layer windings. This method is commonly referenced in works that model CM chokes [126][129]. A similar approach is presented in [152], and it was experimentally validated.

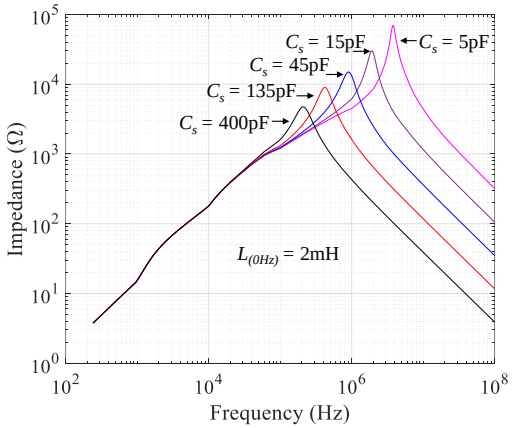


Figure 60 - Influence of inductor stray capacitance C_s on CM choke impedance.

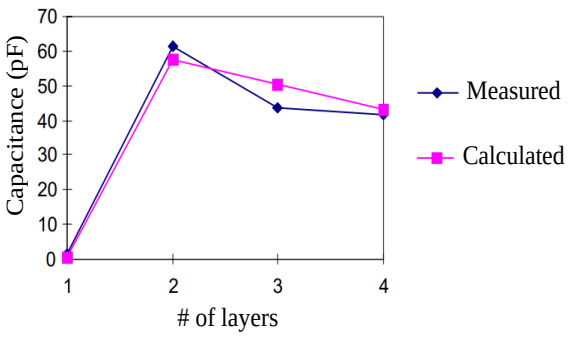


Figure 61 - Measurements and theoretical calculations of stray capacitance for different layers of windings [153].

In this thesis, the approach used in [153] was considered. It is based on analytical equations and presented good results even for several layers more significant than one, as presented in Figure 61,

which can be used to estimate stray capacitances of DM inductors. In the case of CM chokes, there is a convergence in the bibliography to use only one layer to reduce stray capacitances, and then it was also considered in this thesis. The flow chart used to design CM chokes is presented in Figure 62, where a database of 108 part numbers was considered from VAC® and ArcelorMittal, organized from the lighter to the heavier core. This procedure considered that winding minimum diameter is also designed to support I_{dm_rms} current level. The fill factor considers that the CM choke coils (2 for the input and 3 for the output) must be placed in a maximum of 80% of the core internal circumference length with one winding layer.

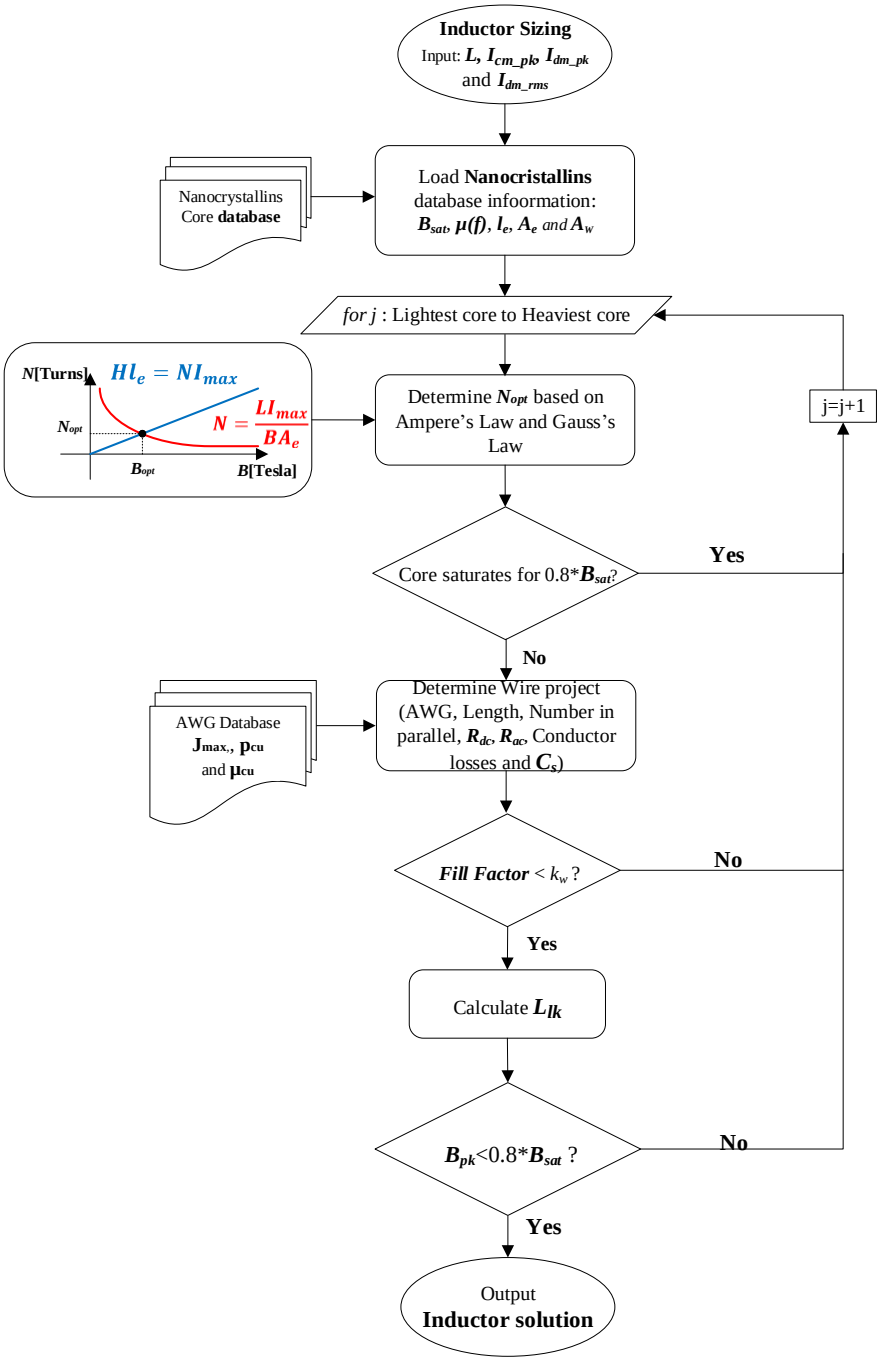


Figure 62 - Input and Output CM Choke Design .

According to Figure 63, three inductors were built for the input filter and two for the output (one with a single wire per coil and another with flexible cable) to evaluate the model considered to the input and output CM chokes. The differences between calculation and measurement are acceptable because of the lack of information of R_{core} for different cores, and that permeability is given only until 1 MHz. For higher frequencies, an extrapolation was performed. In the case of stray capacitance estimation, it is noticeable that the resonance for the output CM choke occurs for almost the same frequency for both measurement and calculation. It gives an idea that the capacitance is similar. The calculated and measured input CM choke presents a more evident difference, but it is still an acceptable predictive model for optimization routines.

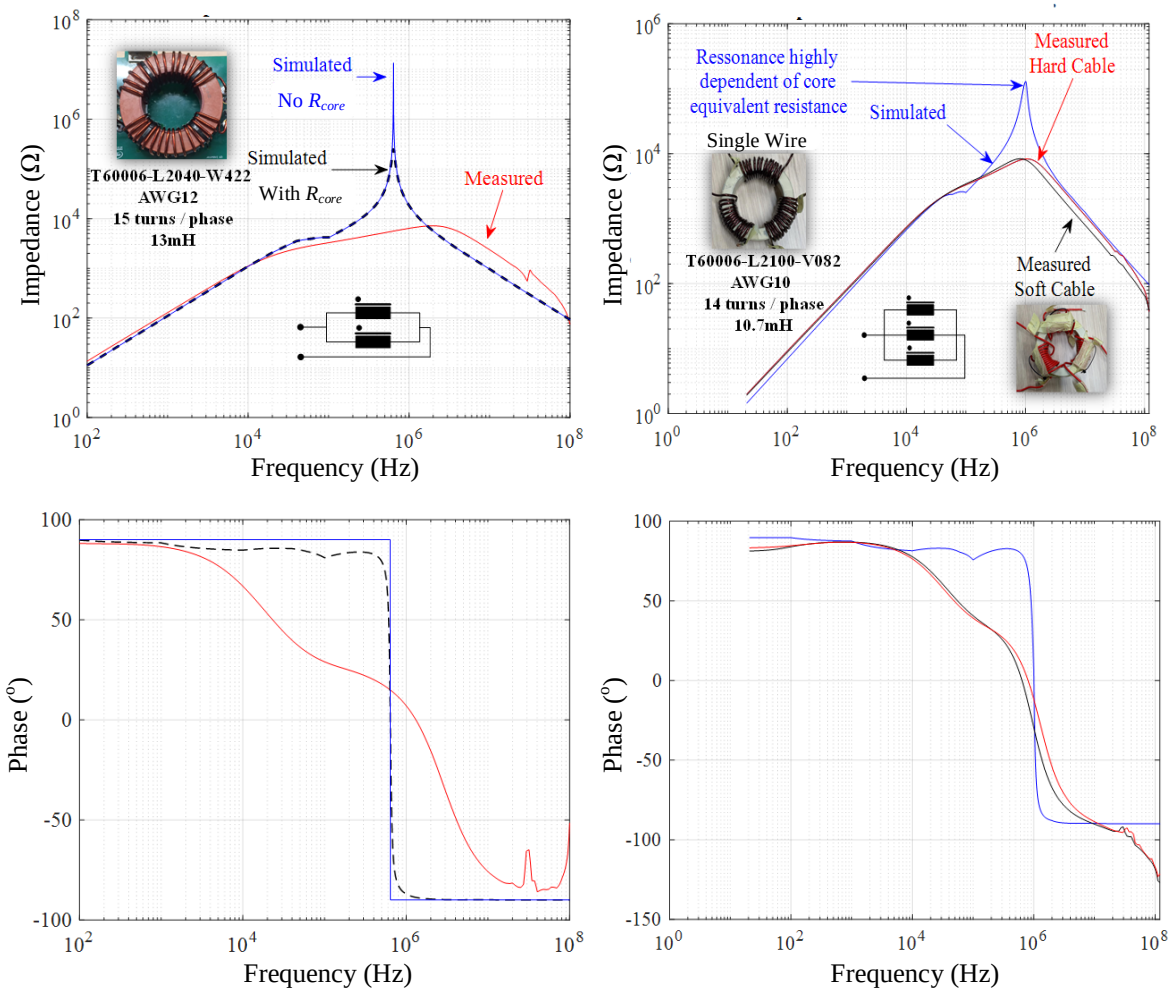


Figure 63 - Experimental verification of input and output CM chokes design.

Regarding leakage inductance calculation, that plays an essential role in core saturation. Both parameters were measured for the input and output CM chokes, as presented in Figure 64. The difference is around 0.9 µH (less than 2%) for the input choke, while there is a difference of 10.3 µH (less than 20%) for the output choke. This indirect measurement may contain not only wire resistance R_{ac} but also R_{core} that is not negligible. Then, since L_{lk} is estimated by considering 2/3 of choke differential mode impedance, which may overestimate leakage inductance, as shown in Figure 64.

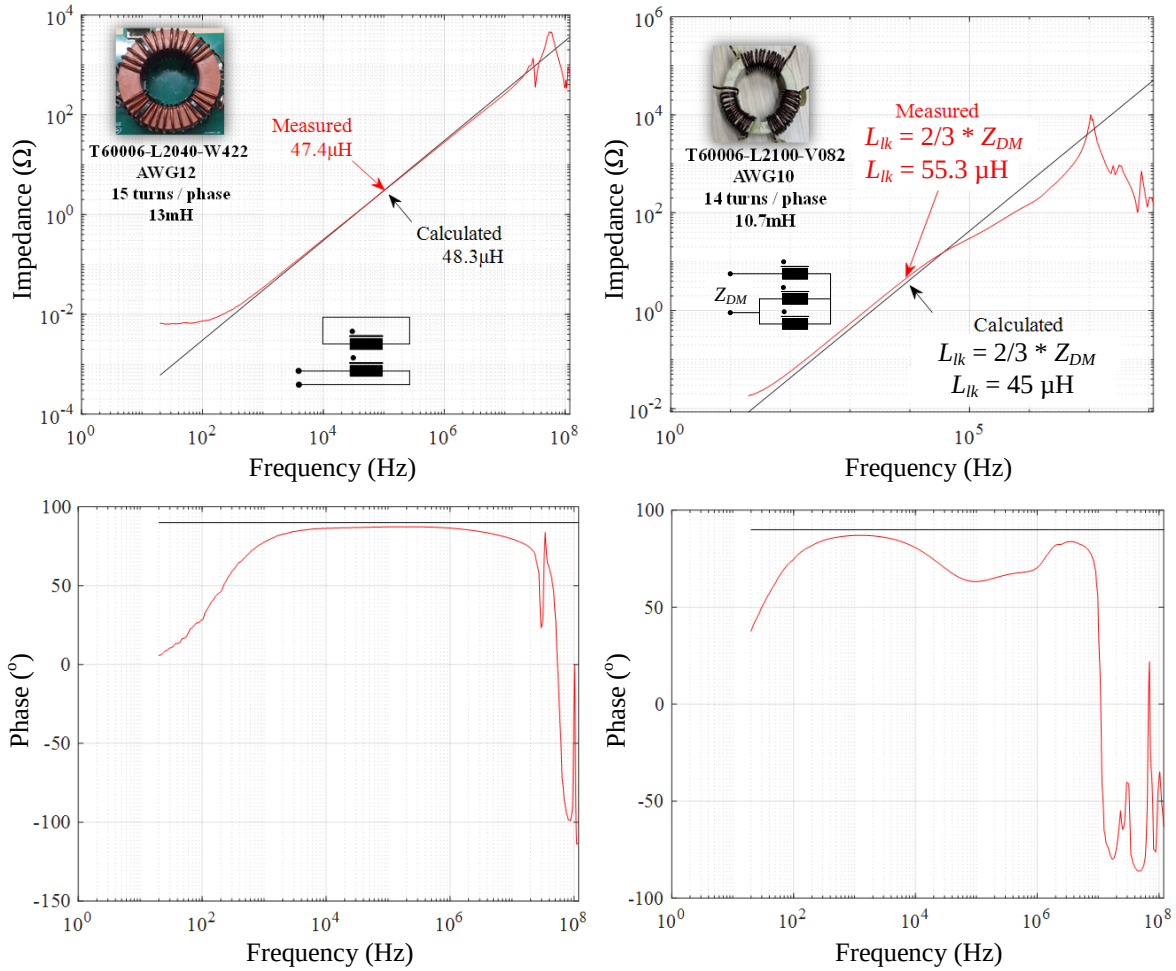


Figure 64 - Experimental verification of leakage inductance for input and output CM chokes.

This section presented the design procedure for input and output CM choke. The design procedure considers the decrease of core permeability with the frequency, parasitic capacitances estimation, and the influence of leakage inductance on core saturation. The equivalent impedance due to these parameters was evaluated experimentally, giving a considerably acceptable behavior for a predictive design. The lack of information on the nanocrystalline core datasheets is worth pointing out, especially regarding R_{core} and core losses such as the Steinmetz parameter. It has a substantial impact on CM chokes impedance behavior beyond 20 kHz.

Sections 2.8 and 2.8.1.1 presented the design procedures based on passive devices datasheets. These procedures are used on the technological bricks responsible for designing the filters to meet the different aircraft design constraints listed in Section 1.3.2. The following section discusses these technological bricks regarding different phenomena, such as conducted emissions, overvoltage at motor terminals, output current harmonic content, power quality, and network stability at inverter input terminals.

2.9 Filters Design

Aircraft manufacturers specify the electrical characteristics of equipment connected to the HVDC network, as is the power drive system studied in this thesis. These requirements define the network's characteristics, installation constraints, quality of the installed power, network stability, and selectivity of protection. The loads connected to the aircraft HVDC network must respect certain limits concerning courant harmonics to safe operation without creating instabilities. As resonances, that may cause errors in measurement systems and voltage regulation. These limits can be divided mainly into two groups: low frequencies harmonics, mainly due to differential-mode currents, and high frequencies harmonics that are commonly associated with common-mode currents [17], [41], [154]. Then, a DM filter is expected in the input of the inverter, while CM filters must be placed both on input and output.

Also, other constraints are essential to guarantee the safe operation of electrical systems in the aircraft. Lightning current is a critical phenomenon that aircraft manufacturers consider, and it is well explained in [155]. Aircraft faraday cage effect protects systems mounted inside by conducting impulse current along the airframe outer skin to exit via wing or tail structure. An increase in composite materials leads to disturbances in aircraft systems. Aircraft manufacturers also address this phenomenon on Environmental Conditions and Test Procedures for Airborne Equipment RTCA/DO-160G standard. The impedance limits imposed by WF5A must be respected between the load and aircraft structure. In this thesis, the EPowerdrive project's constraint was to fix a maximum CM capacitance of 150 *nF* as an equivalent value for both input/output capacitors. This value represents the standard value used to connect calculators to aircraft metallic structures where any CM inductors were considered. For power drive systems, cables, electrical motors, and CM inductors will play an essential role in the path of lightning currents. It will probably change the equivalent CM capacitance value for this kind of application. The discussion about this problem is addressed in Appendix C.

New issues arise with the advance of WBG semiconductors in electrical motors, increasing switching frequency and fast dynamics, and inverter loss reduction. Regarding system reliability and functional expectancy, switched voltages that feed electrical motors cause enhanced bearing current issues and electrical stress on motor insulation. Bearing currents are not a recent phenomenon, and there are reports of them causing failures as far back as the 1930s. They are formed due to the current from the rotor and shaft to the earth from bearing. It causes metal to be transferred between the balls and the races. The cumulative effect of bearing currents leads to increased levels of noise and vibration. This subject will not be addressed in this thesis.

On the other hand, electrical stress on motor insulation emerges due to voltage reflection across feeding cables generating overvoltage on the motor terminal. This stress can generate partial discharges in winding insulation, leading to early insulation degradation and/or failure [156]. This subject is not new, especially in applications where long cables are used. Nevertheless, the increase of semiconductor switching speed and aircraft electrification intensified the research on this area, as presented in [28], [29], [157]–[159]. This thesis will evaluate the overvoltage level of 800 V on the design of the DM output filter.

Another electrical motor problem concerns rotor overheating and failure in PMSM motors[160]–[162]. Rotor losses usually are small for this motor techno. However, with the advent of machine optimization algorithms, new solutions converge to increased motor speed and concentrated

windings to increase power density. This new tendency increases asynchronous harmonic that is converted to rotor supplementary losses. Sinusoidal filters are commonly used in inverters to suppress current harmonics by imposing a quasi-sinusoidal voltage on motor terminals. One criterion commonly used to design sinusoidal filters is the maximum current THD_i (total harmonic distortion ratio) provided by electrical motor manufacturers. The IEEE Standard 519-1992 limits voltage THD_u by 5% for systems with 69kV or below, but this criteria will not be considered in this thesis.

On the other hand, current *THD* limits vary based on the short circuit strength of the system they are injected into [163]. This thesis considers a *THDi* of 7%, recommended by the machine manufacturer. Therefore, the DM output filter should guarantee a maximum overvoltage value on motor terminals and a maximum *THDi* on phase current.

The following sections will describe different phenomena modeling and filter design, based on the models available on the literature, to meet the following constraints:

- Overvoltage on motor terminals and *THDi* on phase current (DM output filter).
- EMI Conducted Emissions respecting $C_{CM(max)}$ = 150nF (CM input and output filters).
- HVDC: Network Stability and Power Quality (DM input filter).

2.9.1 Motor high-frequency impedances

To evaluate overvoltage on motor terminals, cables, and motor accurate high-frequency models are necessary. There are dedicated works for high-frequency modeling of motors regarding CM and DM mode impedances [164]–[166]. In [159], these models are investigated as an equivalent circuit. Another approach is described in where the vector fitting technique is used. In [167], the motor equivalent circuit is decomposed into different elements to generate the expected frequency response. This approach is recently used in [17] due to its simplicity and good results.

Nevertheless, it is necessary to know motor characteristics, as DM and CM impedances on frequency domain. If a predictive model is needed, some analytical equations estimate some parasitic capacitances from the windings and stators by considering motor integration that can be used to estimate motor CM impedance [151]. The main advantage of these two latest techniques is to reduce time calculation since there is no need to interpolate motor impedance data.

This thesis's scope does not include electric motor modeling and will use the impedance measurement of CM and DM impedances of the proposed 50 kW PSMS machine. Figure 65 presents measured DM and CM impedances of the 50 kW used in this thesis.

The CM impedance measurement is proposed by [168] using an impedance analyzer between the three phases connected and the motor frame with the floating neutral. This technique is commonly used, as noted in [169], [170], and it is considered in this work, as presented in Figure 65 (b). In the case of the DM impedance, the measurement method is not clear. In [170], it is measured with an impedance analyzer between two phases, while the third phase is disconnected and the neutral is floating. The work presented in [171] describes another test setup used for EMC analysis. This method

considers measuring the impedance between one phase and the other two phases, as presented in Figure 65 (c).

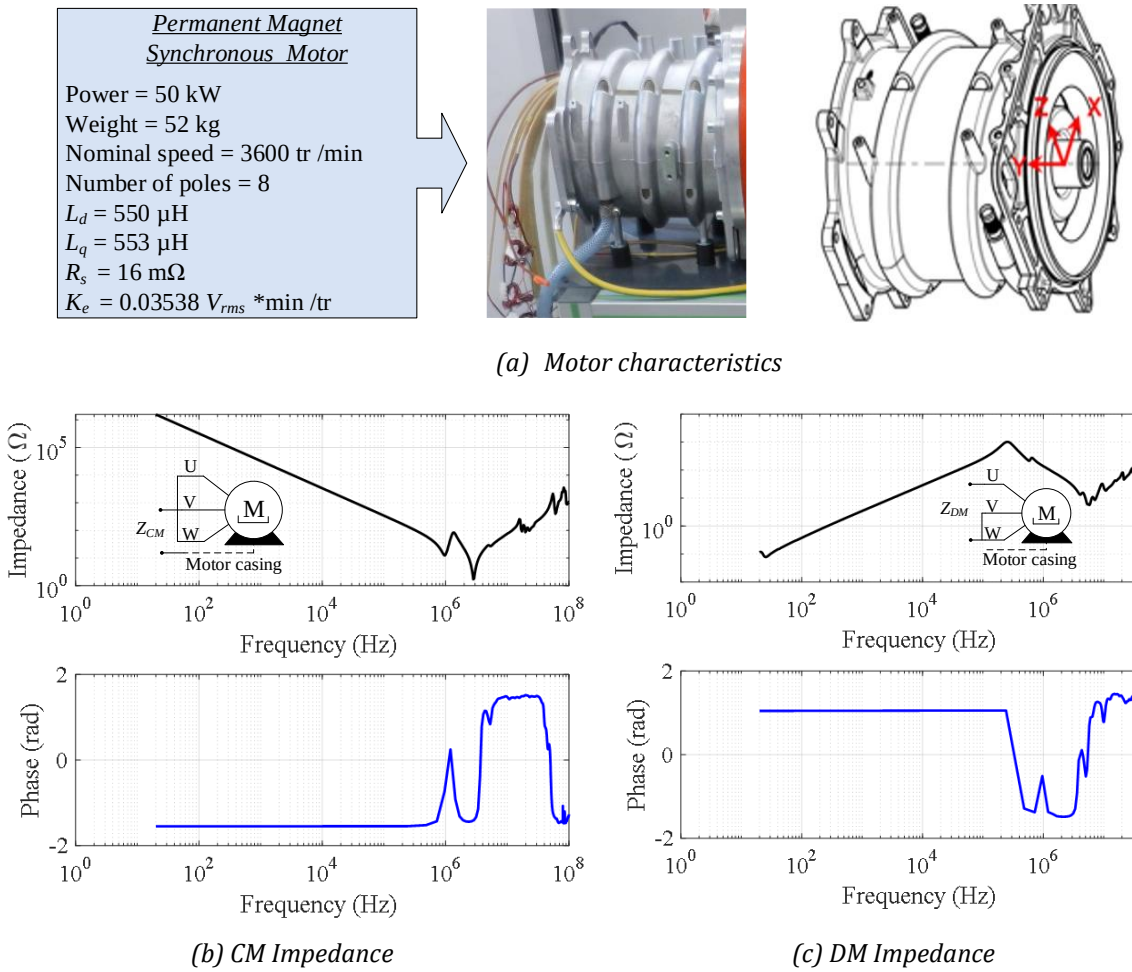


Figure 65 - 50kW PSMS electric machine considered in this thesis and CM and DM measured impedances.

The work developed in this thesis considers that motor DM impedance (Z_{DM}) plays an essential role in estimating the overvoltage at its terminals. In this context, the measurement method presented in Figure 65 is applied, assuming the ***hypothesis*** that high-frequency components (not the low frequency) of the phase *U* current will be likewise shared between the two adjacent phases *V* and *W*, just after the commutation. This hypothesis is verified by simulation in Figure 66. The ideal two-level inverter top switches states are shown for two-time instants: t_1 and t_2. At t_1, phase *V* output voltage passes from 0 to V_{Bus}, while phase *U* and *W* voltages remain unaltered and equal to zero. High-frequency current components appear on the three phases at switching time, and they go to zero after a certain period. I_V has two times the amplitude of I_U and I_W, and it is also phase-shifted from 180° from the other two, which means that $I_{phase\text{-}V}$ is divided by two and returns from phase *U* and *W*, which reinforces the hypothesis. At t_2, phase *V* output voltage passes from V_{Bus} to 0, while phase *U* and *W* voltages remain unaltered and equal to $V_{Bus,}$ and the hypothesis is still valid. These simulations were performed in PSIM by considering the 3-phase AC cable model that considers propagation and reflection effects. The cable was connected to a three-phase *RL* load in a Y connection.

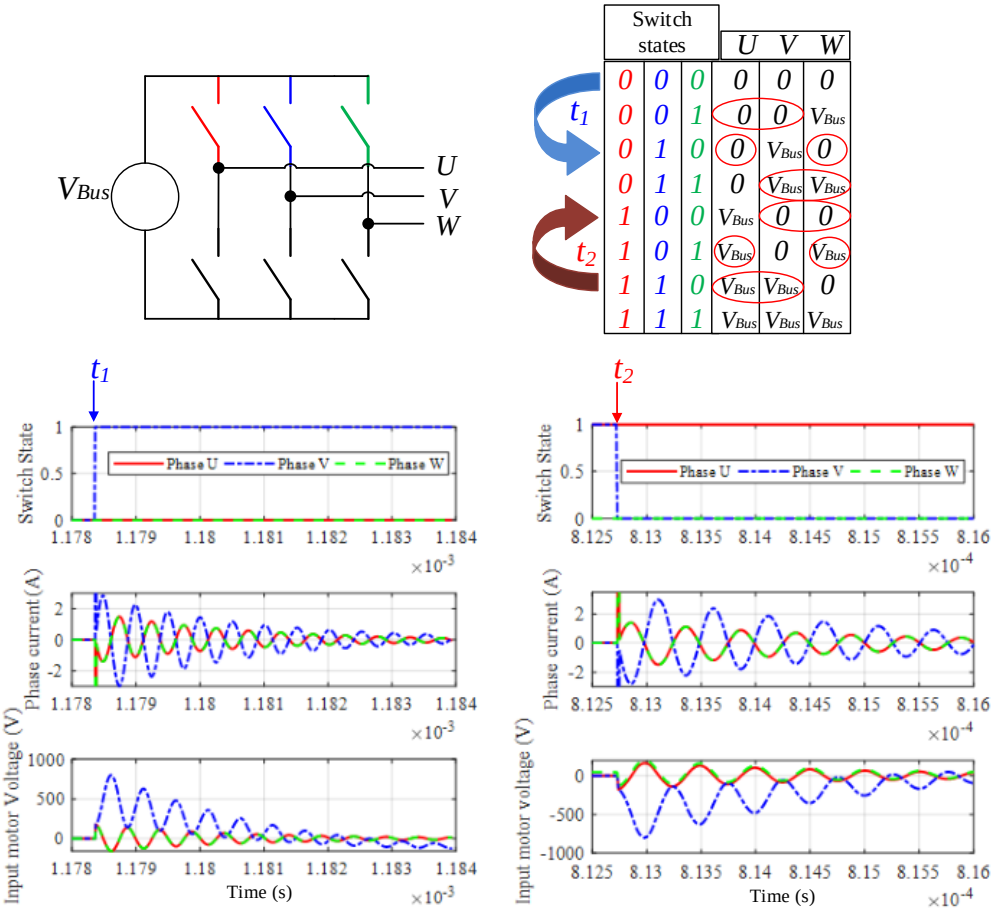


Figure 66 - DM proposed circuit for the instant of phase voltage transition on inverter output.

This hypothesis corroborates the presented measuring method in Figure 65 (c), and it will be taken up on the definition of output cable DM impedance in the following section.

2.9.2 Cable high-frequency modeling

Regarding cable characteristics, different approaches are found in the literature, such as time-domain and frequency-domain. The time-domain approach is presented in considering cable equivalent circuits composed of distributed or lamped parameters[172]–[177]. In that case, for good accuracy, it is necessary to consider an adequate number of cells or lamped parameters correspond to the elementary cable length as presented in Figure 67.

Circuit parameters can be extracted by measurements or calculated using the finite-element method [17], [28], [169], transmission line theory, modal transformation [177], or even by applying evolutionary algorithms [178]. The time-domain approach is commonly used on circuitry simulation tools.

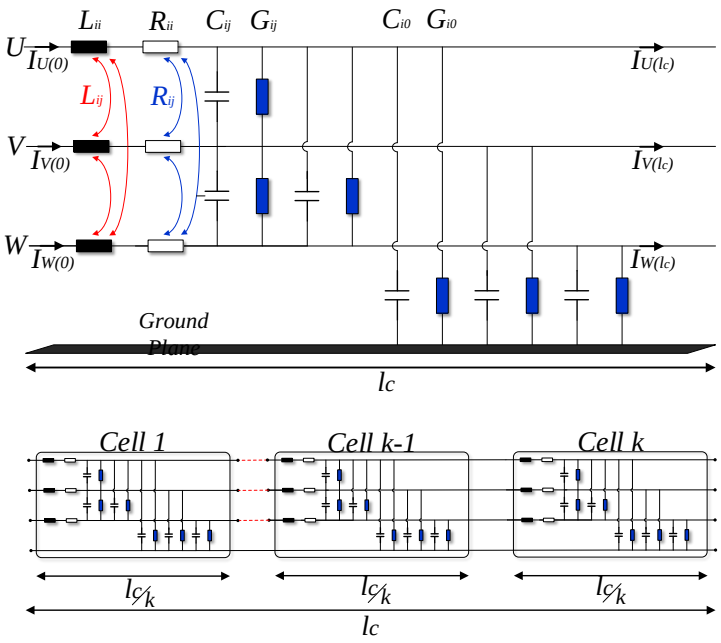


Figure 67 - Three-phase cable equivalent circuit and the split in k elementary cells.

Frequency-domain cable modeling avoids the convolution product used in time domain problems. Only a simple product can resolve the spectrum of the input signal and transfer function in linear systems. According to [28], the problem's frequency resolution can be made six times faster than the time domain's circuit simulation. Moreover, using the multiconductor transmission line theory [179], the cables' exact behavior in the frequency domain is achieved, which means that no approximation is needed for propagation, reflection, and frequency dispersion (as used by cascading elementary cells in the time domain). This modeling can be used to find a cable equivalent two-wire circuit that can be used to calculate common-mode currents [17], [27], or overvoltage [172] in the frequency domain. Considering the facility and speed of calculation using frequency-domain that can be easily implemented in optimization algorithms, this method is considered in this thesis to estimate cable CM and DM mode impedances.

2.9.2.1 Cable modeling: Transmission line theory

The transmission line theory represents multiconductor cables into an equivalent two-port circuit which further simplifies the three-phase cable modeling for CM and DM [164]. This theory is based on the propagation of a TEM (Transverse Electro-Magnetic) wave. It is valid if the cross-section of cables and the distance between them are smaller than one-fourth of the shortest wavelength λ that composes the wave propagation. According to [113], inverter output ringing is around 30 MHz, which means that λ = 30 m considering the light speed as $3 \cdot 10^8$ m/s. Considering that a cable with a cross-section of 5.19 mm (AWG 4) is used on the power drive system (J = 6.2A/mm^2 considering the nominal operation for 130 A_{rms}), the transmission line constraint is mainly satisfied.

The solution using telegraphists equations for a bifilar circuit, represented in Figure 68, is detailed in [179], and it can be represented as a T equivalent circuit.

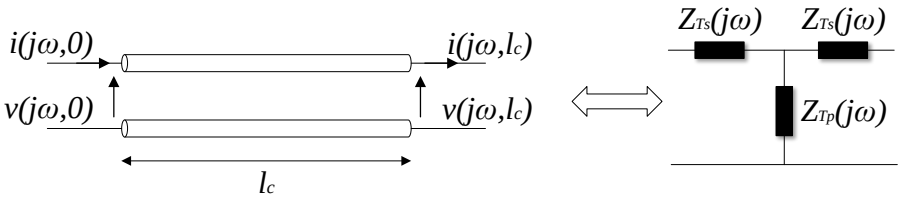


Figure 68 - Transmission line theory for a bifilar circuit and T-type cable equivalent circuit.

A cable with a length equal to l_c can be represented by the chain matrix $ABCD_c$ that comprehends the solution of two-wire propagation equations [179]. These parameters depend on cable line parameters RLCG ($j\omega$), propagation function γ_c, and the characteristic impedance Z_c, where j ($j^2 = 1$) is the complex operator and ω is the angular frequency.

$$\begin{bmatrix} v(j\omega,l_c) \\ i(j\omega,l_c) \end{bmatrix} = \begin{bmatrix} A_c & B_c \\ C_c & D_c \end{bmatrix} . \begin{bmatrix} v(j\omega,0) \\ i(j\omega,0) \end{bmatrix}, \tag{2.41}$$

$$\begin{aligned} A_c &= \cosh\left(\gamma_c(j\omega).l_c\right) \\ B_c &= -Z_c(j\omega).\sinh\left(\gamma_c(j\omega).l_c\right) \\ C_c &= -\sinh\left(\gamma_c(j\omega).l_c\right)/Z_c(j\omega), \\ D_c &= \cosh\left(\gamma_c(j\omega).l_c\right) \end{aligned} \tag{2.42}$$

$$\begin{aligned} Z_c(j\omega) &= \sqrt{\left(R(j\omega)+j\omega.L(j\omega)\right).\left(G(j\omega)+j\omega.C(j\omega)\right)} \\ \gamma_c(j\omega) &= \sqrt{\left(R(j\omega)+j\omega.L(j\omega)\right)/\left(G(j\omega)+j\omega.C(j\omega)\right)} \end{aligned}$$

T type equivalent circuit comprises cable propagation as presented in [172], and circuit impedances are calculated as:

$$\begin{aligned} Z_{Ts}(j\omega) &= -C_c^{-1} \\ Z_{Tp}(j\omega) &= C_c^{-1}.(1-D_c) \end{aligned} \tag{2.43}$$

The following section will describe how to determine the *RLCG* parameters that compose the T equivalent circuit presented in Figure 68 regarding CM and DM cable equivalent circuit.

2.9.2.2 Cable *RLCG* parameters

According to [179], *RLCG* parameters can be calculated analytically by finding the exact solution of Maxwell's equations. Numerically, considering the 2D/3D discretization of Maxwell's equations provides an approximate solution or experimentation. These three methodologies were investigated and validated for the CM impedance of three-phase non-shielded cables [17], [27]. In

[172] and [28], the numerical approach of a 2D problem was implemented in FEMM and validated experimentally for a bifilar unshielded cable. Due to the facility to drive FEMM through MATLAB, this approach was considered in this thesis to calculate *RLCG* parameters.

As defined in Section 1.3.2, this thesis setup was fixed considering 10 meters of a non-shielded cable 3 x EN24681-AZA from Draka. This cable belongs to the family Hook up and Airframe Wiring Light Weight and UltraLight Weight, used for 230 V High Voltage Networks. This cable is composed of three layers, as presented in Figure 69.

1) Stranded conductor in nickel-plated aluminum with 5.83 mm of diameter (AWG3).
2) Polyimide material (Epoxy) with 55 µm thick.
3) PTFE (Polytetrafluoroethylene) insulating material with 595 µm thick.

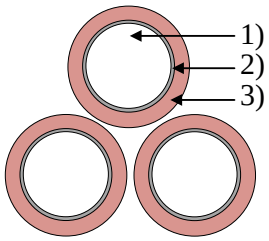


Figure 69 - Geometrical cable specifications

2.9.2.2.1 Cable CM equivalent circuit

CM problem considers that cable input current is split equally between the three conductors for a three-phase unshielded cable, as presented in Figure 69. It returns from the ground plane described on the Conducted Emissions setup of RTCA/DO-160G. CM currents are mainly related to CM voltages, which means that mutual inductances and resistances are neglected. A bifilar CM equivalent circuit per length unit (Δl_c) of a three-phase unshielded cable is presented in Figure 71.

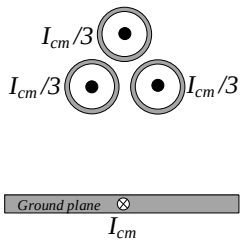


Figure 70 - The 2D problem for three-phase cable CM impedance.

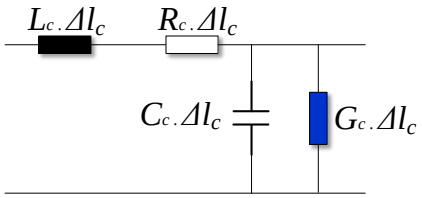


Figure 71 - Bifilar equivalent circuit per length unit of a three-phase unshielded cable.

Numerical solution returned by FEMM comprehends square matrix of *R*, *L*, and *C*, where the diagonal lines of *R* and *L* represent line parameters per length unit. The other elements represent mutual components that are neglected for the CM impedance. Then, *RLCG* parameters for the unshielded three-phase cable presented in Figure 67 can be calculated as:

$$L_{CM-c} = \frac{L_{11} + L_{22} + L_{33}}{3} \;,\; R_{CM-c} = \frac{R_{11} + R_{22} + R_{33}}{3},$$
$$C_{CM-c} = C_{11} + C_{12} + C_{13} + C_{22} + C_{21} + C_{23} + C_{33} + C_{31} + C_{32}, \quad (2.44)$$
$$G_{CM-c} = C_{CM-c}.\omega.\tan\varepsilon_c$$

$C_{cm\text{-}c}$ is demonstrated in [26]. Using the method of images, G_c represents the conductance due to leakage current passing through insulators, and tanε represents a dissipation factor provided by cable datasheets. The high the tanε, the low the material efficiency. The power cables considered in this thesis (EN24681-AZA) are composed of two layers of insulating materials: Polymide and PTFE. Since polyimide presents a higher tanε (around 0.003 [180]) than PTFE (0.0002 [181]), its value was considered in the simulation.

Aeronautical cables are usually composed of a certain quantity of wire strands, which allows a more malleable cable, and different insulating layers, as presented in Figure 72. As addressed in [27], cable geometry, illustrated in, strongly influences *RLCG* parameters and computation time. Considering the cable as a round solid wire, the numerical calculation can be more than 70 times faster than a trapezoidal strand cable and round strand cable, with a good result until 10 MHz.

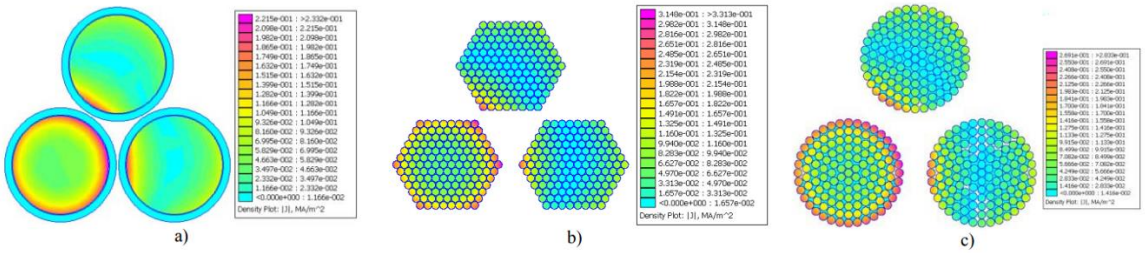


Figure 72 - Cable geometry used on 2D simulation in FEMM [27].

2.9.2.2.2 Cable DM equivalent circuit

In cable DM impedance, mutual inductances and resistances will play an essential role in the equivalent circuit. They cannot be neglected as considered for CM impedance. The Transmission Line theory described previously is valid only for a bifilar equivalent circuit. It is necessary to determine a bifilar equivalent circuit that represents the three-phase cable in DM. In [172], the same equivalent circuit is considered as the one showed in Figure 67 for CM, but only two cables are used. The same circuit is also discussed in [164] for a three-phase cable. It is assumed that two cables are connected in parallel, and the third becomes the current returning path. This approach can be justified by the operation of an inverter in which, at a given moment, two switches are connected to one pole of the DC bus, and 1 is connected to the other pole.

On the other hand, the currents which circulate are not equal for the two switches. Therefore, it is necessary to consider cable mutual couplings. This model is validated experimentally, but it is necessary to cascade elementary cable cells and use time-domain simulation to improve accuracy. Circuit parameters are only estimated considering measurements, making it challenging to estimate cable characteristics and overvoltage on motor terminals. A similar approach is verified in [175] with

cascaded cables elementary cells and time-domain simulation. Both [175] and [164] consider motor two phases connected in parallel, and any information about motor operating point is presented, as output current, motor speed, or charge. So, it is not clear if the experimental validation was done with a turning machine.

This thesis aims to easily implement models in an optimization ambient for all converters predictive design with filters included. Then, frequency-domain problem resolution proposed in [172] seems to be a good approach. In that case, it is necessary to determine an equivalent bifilar circuit of the three-phase cable. The ***hypothesis*** mentioned for the motor DM impedance in the previous section is resumed. It considers that high-frequency components (not the fundamental frequency) of I_{phase} will be likewise shared between the two adjacent phases, as presented in Figure 73. This hypothesis is valid only for the exact instant when a voltage transitions on the inverter output phase to neutral voltage.

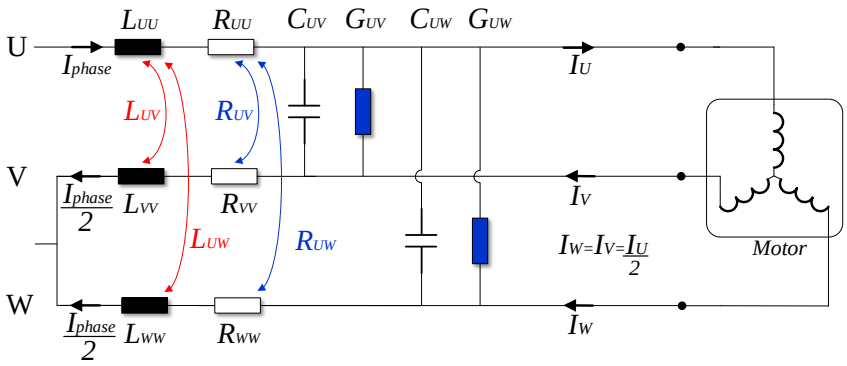


Figure 73 - DM proposed circuit for the instant of phase voltage transition on inverter output.

Therefore, *RLCG* parameters for the proposed DM equivalent circuit can be simulated as a 2D problem in FEMM according to Figure 74, and the equivalent *RLCG* is calculated according to the following equations.

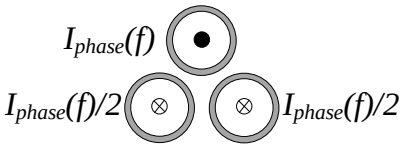


Figure 74 - The 2D problem for cable DM impedance.

$$
\begin{aligned}
L_{DM-c} &= L_{UU} + L_{UV} + L_{UW} + \frac{(L_{VV} + L_{VU})*(L_{WW} + L_{WU})}{(L_{VV} + L_{VU}) + (L_{WW} + L_{WU})}, \\
R_{DM-c} &= R_{UU} + R_{UV} + R_{UW} + \frac{(R_{VV} + R_{VU})*(R_{WW} + R_{WU})}{(R_{VV} + R_{VU}) + (R_{WW} + R_{WU})}, \\
C_{DM-c} &= 2.\ C_{UV} \leftrightarrow C_{UV} = C_{UW}, \\
G_{DM-c} &= C_{DM-c}.\omega.\tan\varepsilon.
\end{aligned}
\tag{2.45}
$$

Knowing the RLCG of the bifilar equivalent circuit for DM and CM per length unit makes it possible to estimate the cable T circuit presented in Section 2.9.2.1. These impedances are used to estimate CM currents and Overvoltage presented in the following sections.

2.9.3 Overvoltage and THDi

Inverters used to feed electrical motors are one of the causes that accelerate winding insulation deterioration. The inverter output's impulse voltages associated with the switching speed of rising and falling edges may create nonlinear voltage distribution along feeding motor windings. This fact associated with the difference between cables characteristic impedance on both connections (inverter output and motor terminals), also called impedance mismatch, causes the propagation and reflection phenomena along the cable [172], causing an overvoltage at motor terminals[182]–[185]. The advent of WBG semiconductors and the use of electrical machines on aeronautical operating constraints, such as low pressure and high temperature, highlight research related to insulation aging due to partial discharges and breakdown [152][169]. Figure 75 represents the overvoltage phenomena in motor terminals associated with partial discharges and breakdown of windings insulation.

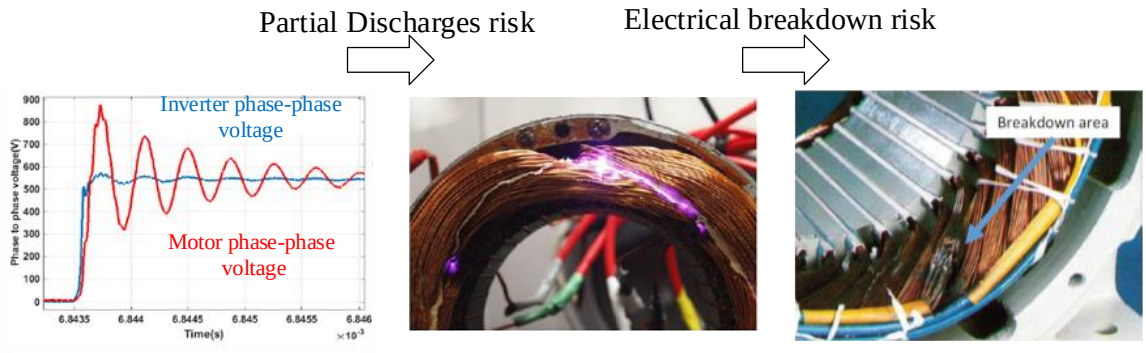


Figure 75 - Overvoltage in motor terminals responsible for causing partial discharge and breakdown.

Overvoltage phenomena are strictly related to cable characteristics, motor impedances, and semiconductor switching speed. Theoretically, overvoltage caused by a voltage pulse should not exceed twice the bus voltage (2 p.u) [187], as presented in Figure 76.

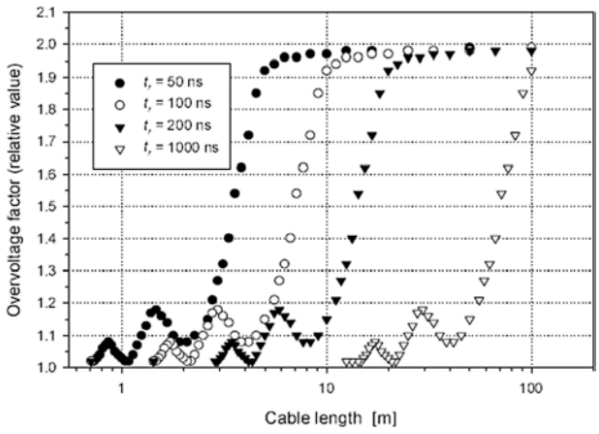


Figure 76 - Overvoltage ratio in function of cable length proposed in EIC Standard (60034-18-41).

In reality, it can even reach higher values caused by inverter reversal polarity [188] or by two pulses that are close to each other in inverter output voltage [28]. In [172], it is experimentally validated that for an ideal trapezoidal waveform, the two p.u is respected. However, considering the output voltage ringing due to fast commutation of WBG semiconductors may increase overvoltage to higher than three p.u. for cables with less than 3 meters long as presented. On the other hand, this phenomenon is significantly reduced for longer lengths due to cable loss.

For a predictive estimation of overvoltage on motor terminals, it is necessary to know motor and cable behavior in high frequencies as presented in Section 2.9.2 and Section 2.9.1 and semiconductor characteristics. Semiconductors switching speed and transients (ringing) depends on gate circuit characteristics, as V_{gs} (gate to source voltage) and R_g, converter integration, semiconductor output capacitance C_{oss} and switched current as presented in [17], [112], [113], [189]. The study carried out in this thesis considers semiconductors characteristics available in datasheets, in the case of overvoltage calculation, *dV/dt* for a given current, as presented in Table 14. For a more precise estimation of overvoltage, transistors characterization on the final converter is necessary. It is worth pointing out that the 650V SiC SCT3017AL has a low switching speed while the 600V Si IPZ60R017C7 is as fast as the 650V GaN GS66516T for the conditions presented in the datasheet.

Table 14 - Transistors dV/dt provided by the datasheet.

Part Number	*dV/dt*	*Current*	*Rising time* t_R	$V_{gs\,(+)}/R_g$
SKM600GA12E4	6.7 kV/µs	600 A	90 ns	15 V/ 2 Ω
HT3201RVB	17 kV/µs	300 A	35.2 ns	20 V/2 Ω
GS66516T	32 kV/µs	16 A	12.4 ns	6 V/5 Ω
IPZ60R017C7	30 kV/µs	58 A	13 ns	13 V/1.8 Ω
SCT3017AL	6.9 kV/µs	18 A	44 ns	18 V/0 Ω

2.9.3.1 Overvoltage and *THDi* Modelling

Overvoltage calculation in the frequency domain is explained in [172] with a bifilar equivalent circuit presented in Figure 77 for the T equivalent circuit of the DM cable impedance presented in Section 2.9.2.2.2.

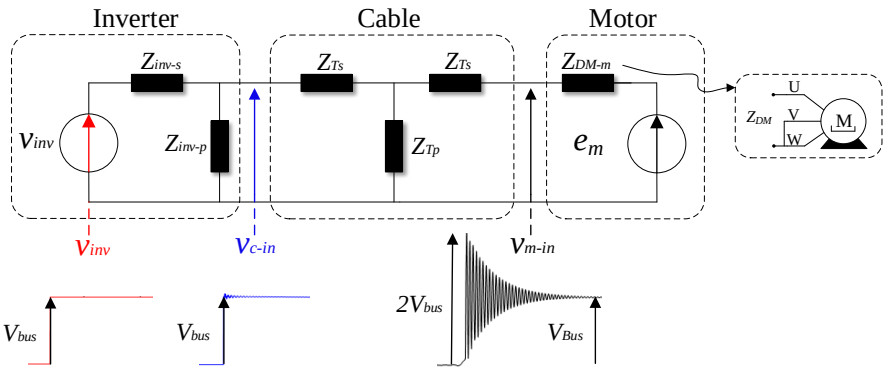


Figure 77 - Frequency-domain equivalent circuit to estimate overvoltage[172].

The inverter is modeled as a voltage source v_{inv} with a series impedance $Z_{inv\text{-}s}$, which comprises undesirable impedances due to electronic integration and semiconductor, usually called loop impedance. This loop impedance is composed of resistive and inductive parameters, while $Z_{inv\text{-}p}$ represents parallel inverter impedance due to the inverter's output capacitance (PCB + semiconductor). These two impedances will determine the oscillation on cable input voltage $v_{c\text{-}in}$.

The electric motor is modeled as a differential mode impedance Z_{DM} in series with a back-EMF (electromotive force). The overvoltage of motor terminals is represented by cable output voltage $v_{m\text{-}in}$. This model was validated for a bi-phase cable [172], while this thesis proposes a new approximation for a three-phase cable represented as an equivalent T circuit. As presented in Section 2.9.2.2.2., this approximation is valid only for the voltage rising/falling time instant. An experimental setup was considered to verify the overvoltage estimation using this cable equivalent circuit, as presented in Figure 78.

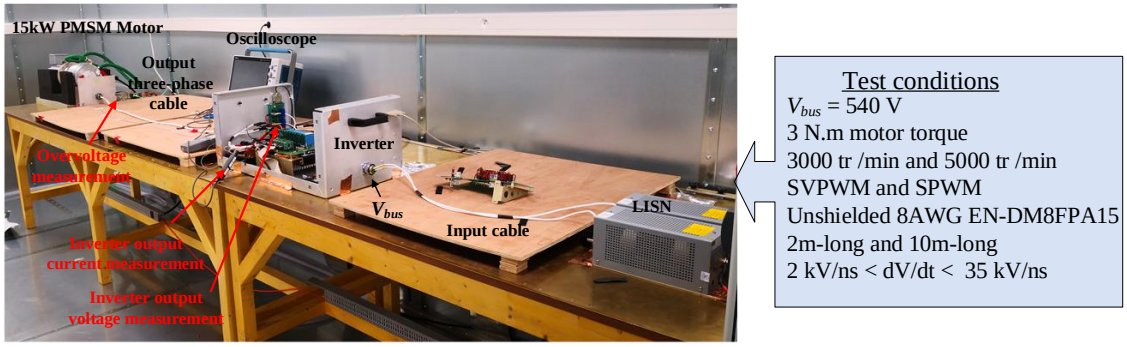


Figure 78 - Overvoltage: Test setup and conditions.

Regarding the simulation, the inverter model parameters are highly dependent on inverter integration and were neglected for the simulation ($Z_{inv\text{-}p} \approx \infty$ and $Z_{inv\text{-}s} \approx 0$). The aeronautical cable EN-DM8FPA15 AWG8 was simulated in FEMM to extract *RLCG* parameters per length unit. For the electric motor, Z_{DM} impedance was measured considering an impedance analyzer from 0 to 50 MHz. According to Figure 79 for a dV/dt = 30 kV/µs, the simulated model generates an overvoltage of 1007 V while the measured reached 997 V on phase-to-phase voltage on motor terminals a ten m-long cable. The difference between the oscillating frequencies is related to cable equivalent *RLCG* calculation, considering that the equivalent circuit shown in Figure 73 is valid for the voltage transition period only. Nevertheless, it presents a reasonable estimation of the overvoltage level, representing one of the DM output filter design constraints.

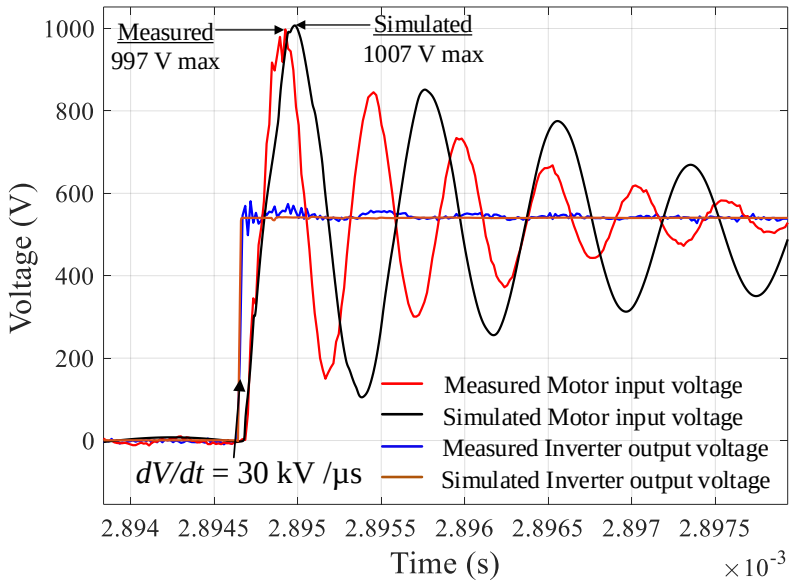
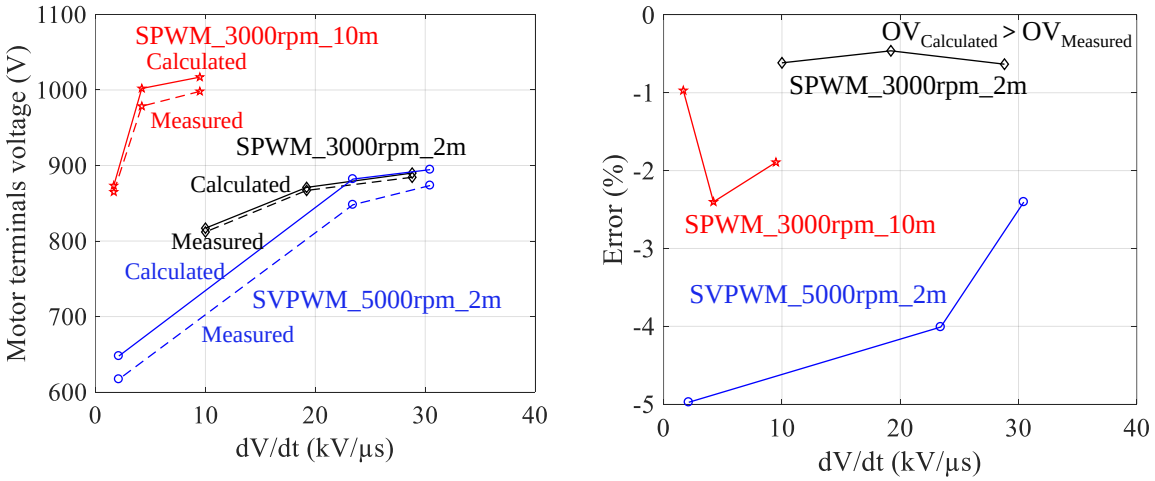


Figure 79 - Overvoltage: Simulation x Measurement for dV/dt = 30kV/µs and 10m-long.

Other tests were carried out for different switching speeds, cable lengths, and motor speeds. Among the measurements, error inferior to 5% for different *dV/dt* values is verified for all results in Figure 80. Motor speed may influence motor Z_{DM} impedance that increases error between simulation and measurement. Cable length also influences overvoltage estimation, passing to almost 2.4% error for a cable of 10 meters. Nevertheless, the proposed cable model is satisfactory for estimating overvoltage in a three-phase motor drive system in nominal operation and will be considered for the DM output filter design.



a) Motor terminals overvoltage *b) Error between calculation and measurement*

Figure 80 - Overvoltage modeling experimental validation

The overvoltage level depends on the voltage transition on inverter output. In a 2-level topology, voltage transition goes from 0 to V_{bus}. It implies an overvoltage of V_{bus} superposed to bus voltage, so $2*V_{bus}$ is verified in motor terminals. In the case of multilevel topologies, inverter voltage transition is reduced according to the number of output levels. In the 4 - level Quasi FC and the 7 -level

FC/NPC presented in Section 0, output voltage transition is 1/3 and 1/6 of V_{bus}. Then, overvoltage seen by motor terminals will be the voltage V_{bus} superposed by the voltage transition of each topology as presented in Figure 81. Considering the overvoltage limit of 800 V, multilevel topologies are already type mitigation dispositive, and no additional filtering is needed. This hypothesis is true if the two p.u overvoltage theoretical limit is considered. This thesis will not consider any abnormal conditions that increase overvoltage beyond the two p.u for DM output filter design.

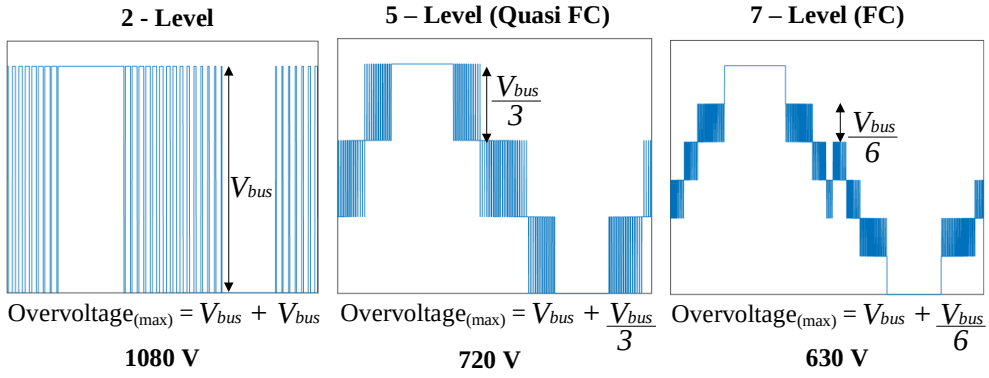


Figure 81 - Maximum theoretical overvoltage for inverter topologies proposed in Section 2.6.

The DM output filter limits the overvoltage at motor terminals, but it will also act on the output current THD_i . Therefore, the DM output filter optimization procedure must consider these two parameters to calculate the filter solution. THD_i is calculated based on motor input voltage $v_{m\text{-}in,}$ and it must be under 7%. Cable series inductance and resistance are much lower than the ones of the motor. The input current ripple will be mainly defined by motor impedance. To calculate I_U, $v_{m\text{-}in}$ is applied to 4/3*Z_{DM} (the impedance of two phases in series). For the 2 - level inverter without any filter, THD_i is 14.8% for nominal condition, DPWM1, and f_{sw} = 10 kHz. For the Quasi-FC topology (4 - level) is 3.4% and for the FC/NPC topologies (7-level) is 2.3%. Then, the *THDi* constraint is applied only for 2 - level topology.

2.9.3.2 Filter topologies

Passive filters are common and practical solutions for mitigating overvoltage on motor terminals and reducing current harmonics by paying the system weight. According to the filter's role, the universe of three-phase output passive filters is divided into two groups.

The first group is called *dV/dt* filters. They are specially designed to reduce overvoltage in long cable applications because their natural frequency is much higher than inverter switching frequency f_{PWM} but smaller than the cable resonance frequency. The main topologies of *dV/dt* filters are summarized according to the passive devices' placement: on inverter output or motor input. These topologies comparison is presented in [190] regarding different characteristics.

Topology 1: Inverter Output: *N/A* - Motor Input: *RC* [191], [192]
This topology is shown in Figure 82, and it is commonly used to reduce overvoltage. It has an attractive price compared to topologies with inductances, and it

is placed just on motor terminals, reducing the motor input impedance. This topology cannot change the wavefront of the pulse, so it cannot improve intercoil and inter-turn voltage distributions in the motor. It will also increase the high-frequency CM current to the ground through motor bearings.

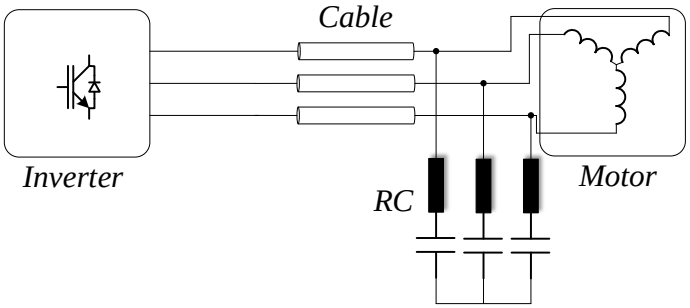


Figure 82 - dV/dt filter - Topology 1.

Topology 2: Inverter Output: *L* - Motor Input: *RC* [190]
Inductor placed on inverter output reduces inverter *dV/dt*, which reduces *dV/dt* on motor terminals, as shown in Figure 83. In contrast, RC on motor terminals suppresses overvoltage as Topology 1, but in this case, lower losses are expected due to *dV/dt* attenuation by inductor *L*. It is also expected attenuation of CM current as well as inter-turn voltage and coil voltages distributions.

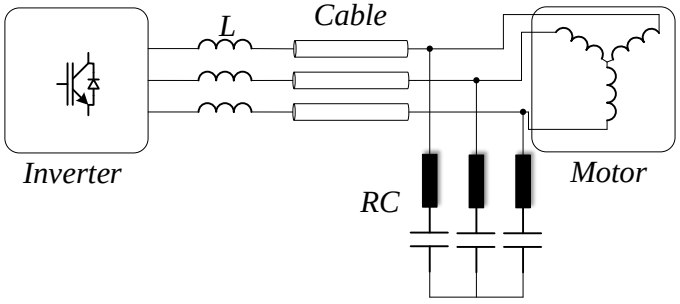


Figure 83 - dV/dt filter - Topology 2.

Topology 3: Inverter Output: *RL* - Motor Input: *C* [193]
This topology gathers the advantages of Topology 2 by changing *dV/dt* and suppressing motor overvoltage. The insertion of *R* in parallel with *L* allows increase filter losses by reducing the value of *L*, as shown in Figure 84.

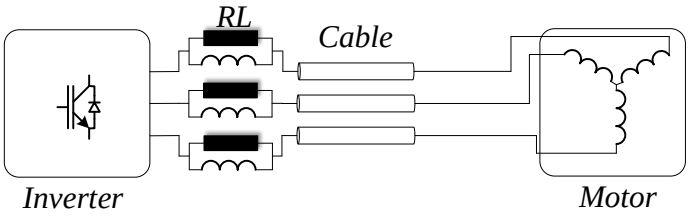


Figure 84 - dV/dt filter - Topology 3.

Topology 4: Inverter Output: *RL* - Machine Input: *RC* [190]

This topology gathers all advantages of topologies 1 and 3, and it is shown in Figure 85.

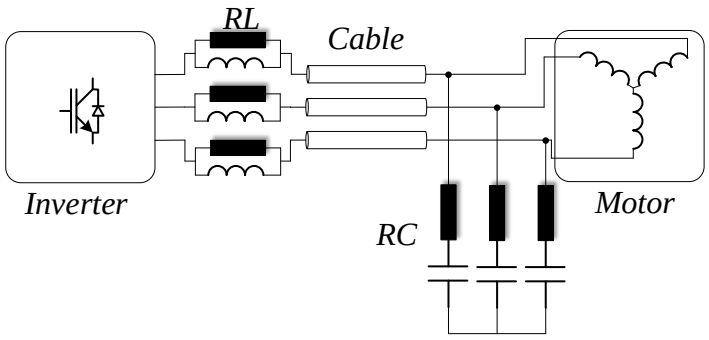


Figure 85 - dV/dt filter - Topology 4.

Sinusoidal filters compose the second group. They are designed to impose a quasi-sinusoidal voltage on motor terminals, reducing current harmonics. Consequently, they have lower cut-off frequencies (some kHz) compared to *dV/dt*. Implicitly the overvoltage problem is non-existent with the price of using large and heavy inductors. This filter is designed considering an *LC* or *LCL* filter on inverter output. Due to quasi sinusoidal waveforms, motor losses and inverter losses may also be reduced. According to [190], this traditional solution may be optimal for small and medium cable lengths despite weight and cost. Another essential advantage of this topology is that it can be used as a hybrid CM and DM filter due to a common point connection of DM filter capacitors C_x, as presented in Figure 94. This connection can be used to connect a C_Y capacitor to the ground of the CM output filter. This solution is used in [32] and in a range of EMI filters for motor drive applications from Schaffner, FN3287, and FN3258. Usually, C_y may have some nF and cannot hold DM currents due to fundamental frequency. Then, C_x is used in the order of a few hundreds of nF (EPCOS MKP EMI Suppression Cap. X2) or some µF (EPCOS MKP DC-Link Cap.), being able to handle DM current but also changing inverter output voltage to a more quasi sinusoidal waveform. If $C_x >> C_y$, CM's current path will see C_y impedance to the ground. By considering an output CM capacitor, it is possible to reduce the value of $L_{CM\text{-}out}$ and increase inverter power density.

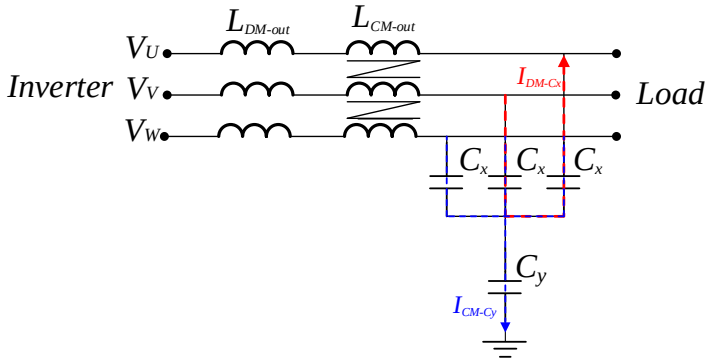


Figure 86 - Hybrid output filter composed of DM and CM passive devices.

This topology is considered on the optimization design of the DM output filter presented in the following section. It gathers low current harmonic attenuation that is not verified for *dV/dt* topologies and allows a C_y capacitor for CM output filter. The impact of removing the C_y of the CM output filter will be evaluated in Chapter 3, where the CM filter's weight is investigated for different conditions. DM

output filter impedance is reduced to an equivalent bifilar, considering the same hypothesis used for the cable. The equivalent circuit presented in Figure 87 is placed between inverter and cable circuits of Figure 77 and composes the Overvoltage and THD_i model.

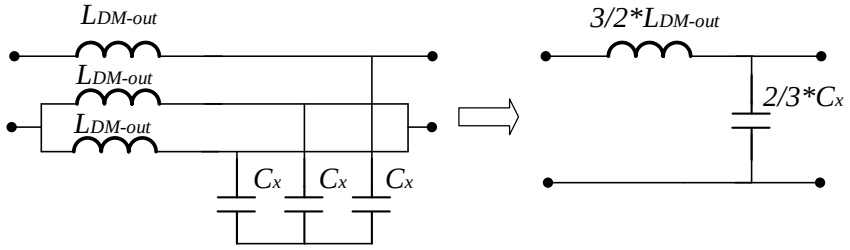


Figure 87 - DM output filter bifilar equivalent circuit.

The following section will present the optimization procedure for the DM output filter considering overvoltage and THD_i phenomena and the filter topology presented in Figure 86.

2.9.3.3 Optimization Results

DM output filter optimization considers the variation of $L_{DM\text{-}out}$ and C_x, and for each combination of LC, the overvoltage level and THD_i are evaluated. $L_{DM\text{-}out}$ and C_x design consider the methodology presented in Section 2.8.2.1 for the powder core and Section 2.8.1 for EPCOS MKP EMI Suppression Cap. X2 (C_x min value = 100 nF).

In total, 500 possibilities are calculated by varying $L_{DM\text{-}out}$ (10 µH to 1 mH) and C_x (100 nF to 10 µF) as presented in the flowchart in Figure 88 for the 2-level inverter. Additionally, the voltage drop due to filter and cables was considered a filter design constraint due to a strong influence on PSMS control [194], [195]. DM output filter must be designed considering that the voltage drop does not surpass 5% of V_{bus} (27 V). The solution is selected among others considering the idea proposed in [196], named R-dominance. The solution is chosen by considering the shortest distance between all solutions and a utopian solution. In the present study, the utopian solution is considered as one with no losses and no weight. Weight and losses are normalized according to the mean value of all solutions.

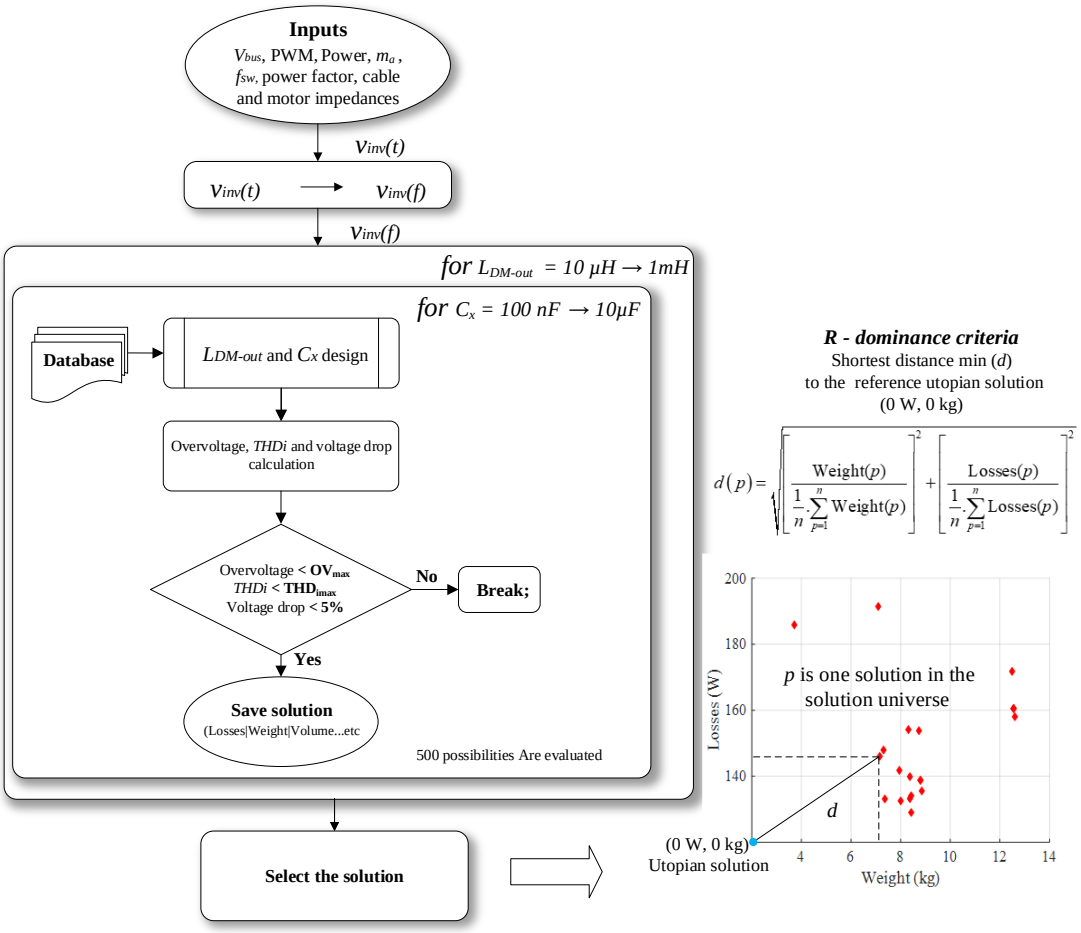


Figure 88 - DM output filter optimization design for the 2 – level topology.

Optimized results are presented in Figure 89, considering THD_{imax} = 7% and OV_{max} = 800 V for the 2-level topology in nominal operation (DPWM1) and different switching frequencies.

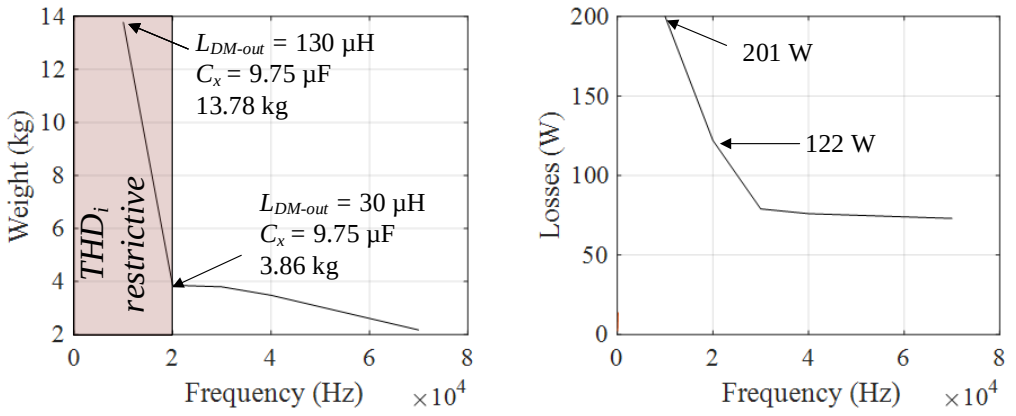


Figure 89 - DM output filter weight and losses for the 2- level topology in nominal operation and different switching frequencies.

At 10 kHz, THD_i is more restrictive, and the solution with 13.78 kg with 201W is selected. Different parameters play a role in $L_{DM\text{-}out}$ design, especially maximum temperature rise due to magnetic

losses in powder cores and voltage drop. By increasing the switching frequency to 20 kHz, $L_{DM\text{-}out}$ decreases from 130 µH to 30 µH since THD_i is not that restrictive. Then, the DM output filter passes to 3.86 kg and 122 W. It is verified that C_x tends to saturate in the maximum value to reduce $L_{DM\text{-}out}$. The maximum value of C_x (10 µF) was fixed to limit capacitance reactive power on 5% of nominal power (50 kW) to avoid the system from excess power factor decrease [197], [198].

In multilevel topologies described in Section 2.6, the DM output filter comprises inductors to parallel inverter legs and C_x capacitors. The optimized design of these uncoupled inductors follows the modeling presented in Section 2.2.2.1 and the powder core tool described in Section 2.8.2.1. The design considered a current ripple of 60%. The figure shows the inductor's weight and losses for the 4 - level Quasi FC and 7-level FC/NPC hole converter (9 legs). At 10 kHz, the inductors of the 4-level topology have 20.7 kg/243 W.

In comparison, the 7 – level inductors have 6.17 kg/66 W. By increasing switching frequency to 40 kHz, the weight and losses pass to 3.5 kg/110 W for the 4-level topology and 1.47 kg/30 W for the 7-level topologies. The increase of the number of inverter output levels from 4 to 7 levels may represent a gain of 70% on weight savings and reduce losses by a factor of almost 4, at 10 kHz. At 40kHz, there is a gain of 58% weight and a reduction of 72% on inductor losses. Reflecting gravimetric power density, 4 - level topology inductors have 20 kW/kg while the 7-level have 46.7 kW/kg, at 40kHz.

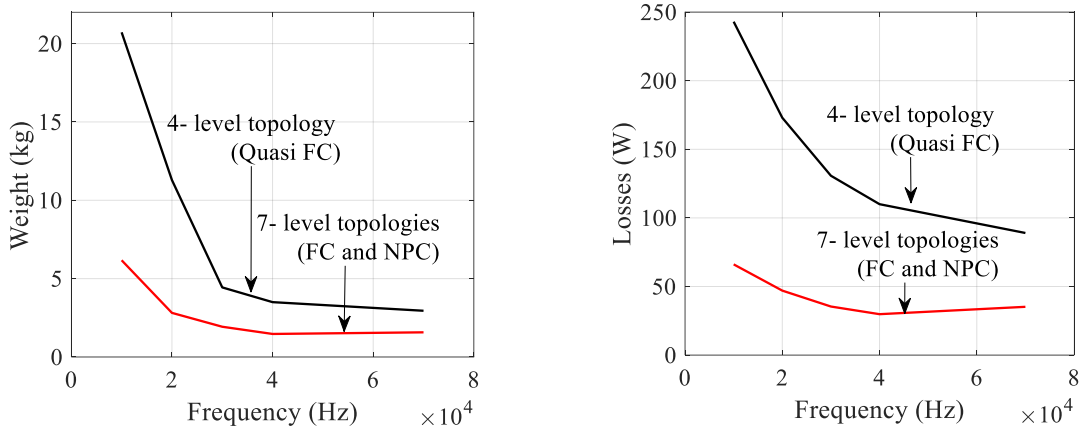


Figure 90 - Inductors weight and losses of 4 - level Quasi FC and 7- level FC and NPC for nominal operation and 60% of current ripple.

C_x capacitors were calculated for the minimum affordable value that guarantees that $C_x >> C_y$, then 100 nF, was considered per phase, representing 300 nF in series with C_y. Capacitors C_x total weight is 50 g (B32921C3104).

Finally, according to Figure 91, the maximum voltage drop for the 7-level is 9.88 V, while for the 4 - level is 19.4 V, and for the 2 - level is 26.6 V (27 V is the limit). Nevertheless, the switching frequency increase to higher than 20 kHz makes voltage drop lower than 5 V for all solutions. It means that voltage drop constraint is not restrictive for this application if the switching frequency is increase. If the fundamental frequency is increased from 240 Hz (nominal) to 400 Hz, a factor of 1.7 is applied at voltage drop, and output inductors for the 2 - level and 4 - level topologies must be redesigned for 10 kHz, since voltage drop will rise to 45.2 V and 33 V, respectively.

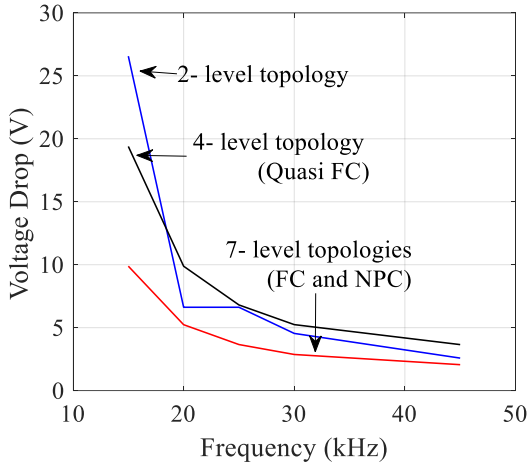
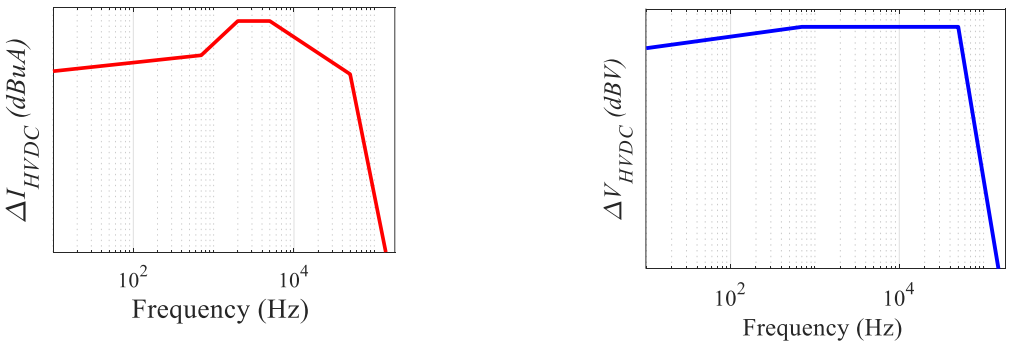


Figure 91 - Voltage drop on output inductors and cable for the three different topologies.

The DM output filter designed in this section and the output inductors to parallel the FC and NPC legs determine the inverter output current (together with motor characteristics). Therefore, it indirectly influences the semiconductors switched current, which in turn determines inverter input current. The design of the DM input filter is linked to the inverter input current, and its procedure is described in the following section.

2.9.4 HVDC: Network Stability and Power Quality

Current low frequencies harmonics, or ripple ΔI_{HVDC}, must be kept under the Airbus HVDC standard limits shown in Figure 92 (a) from 0 to 150 kHz. Current harmonics must also be limited if voltage ripple ΔV_{HVDC} is present on HVDC network voltage, according to Figure 92 - b). Many works in the literature investigate the placement of a passive filter between the inverter and HVDC bus to guarantee power quality and network stability by considering the criteria of a load minimum impedance $Z_{HVDC} = \Delta V_{HVDC}/\Delta I_{HVDC}$ [6][17][21][22] [157].



a) Current ripple ΔI_{HVDC} *b) Voltage ripple ΔV_{HVDC}*

Figure 92 - Low-frequency harmonics limited by Airbus HVDC standard.

This thesis resonates in this same direction by considering one DM input filter to guarantee nominal load operation. The inverter will not generate current harmonics on an HVDC network more

extensive than specified by standard limits. The power drive system must also be immune to the input voltage ripple, according to the test setup presented in Figure 93. The same standard limits DM voltage ripple ($\Delta V_{DC(max)}$) in around 5% of standard conditions (without voltage ripple ΔV_{HVDC}) for an HVDC of 540 V. This limit is considered to design the minimum value of the DC-link capacitor on inverter input voltage V_{bus}.

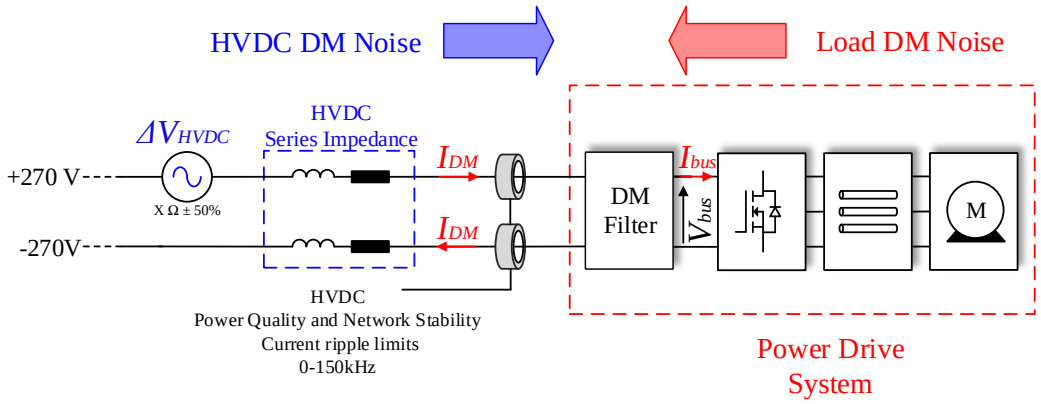


Figure 93 - DM input filter design problematic.

The first step to designing a DM input filter is to calculate the inverter input current I_{bus} based on inverter topology, PWM control, and machine nominal operating point. Ideally, high-frequency harmonics of I_{bus} are provided by DC-Link capacitor, and the current from HVDC Network I_{DM} is mainly DC, as shown in Figure 94. Therefore, the minimum DC-Link capacitance $C_{(min)}$ to reach 5% of voltage ripple is calculated according to the procedure presented in Section 2.8.1.1.

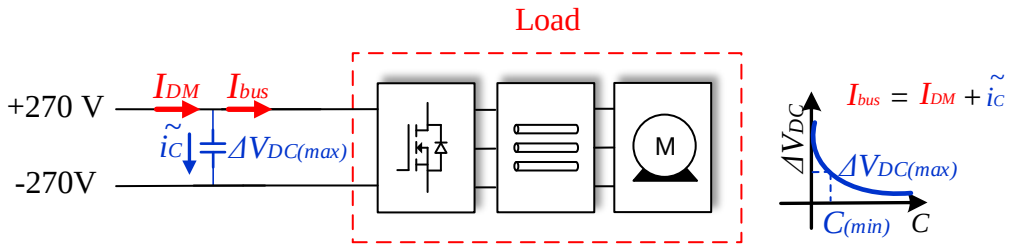


Figure 94 - Minimum DC-link capacitance to guarantee minimum $\Delta V_{DC(max)}$.

By knowing $C_{(min)}$, the filter can be designed to attend Z_{HVDC} and ΔI_{HVDC} criteria. For this study, only two order filters composed of one capacitor C and one inductor L are considered, as seen in most literary works. The LC filter's main problem remains the intrinsic resonance of this circuit that can present an abrupt decay of filter impedance that can destabilize the connection to the HVDC network or increase current harmonics. Then, the use of damping circuits is almost a consent in the works of the area [137][149][150]. This damping circuit comprises one inductor or capacitor associated with a damping resistor R_d, and Figure 95 presents the three traditional DM filters with damping.

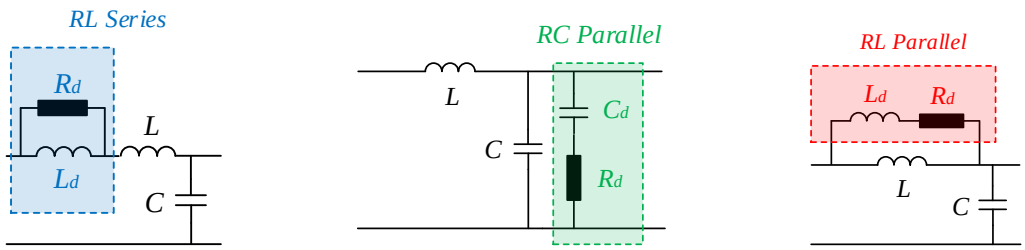


Figure 95 - DM input filter topologies with damping circuit.

The advantages and disadvantages of each topology are discussed in [149] and [202], as well as the optimal relation between damping parameters (C_d, L_d, and R_d) and values of L and C. This thesis considers all three topologies for the optimization procedure. For each case, the optimal topology is selected according to the trade-off between losses and weight. Most high frequencies harmonics are provided by C, and only a tiny part passes through R_d. In that case, R_d losses will be neglected for this study. Simultaneously, the other damping devices are designed according to the procedures for powder cores and film capacitors described in Section 2.8.1.1 and Section 2.8.1, respectively.

The flowchart presented in Figure 97 represents the optimization procedure implemented to find the lightest solutions for the DM input filter for the topologies selected in Section 2.6.

This procedure is divided into the following parts:

1) Inverter topology and PWM technique are selected, I_{bus} is calculated for the frequency domain's nominal operating point.

2) $C_{(min)}$ is calculated to guarantee a voltage ripple of 5% on the inverter input voltage.

3) Ideal LC filter cutoff frequency is determined according to [203] by comparing each harmonic of I_{bus} and ΔI_{HVDC} limits.

Three loops vary filter parameters, as f_{cutoff} around the ideal value calculated in step 3 (loop A), the value of C starting with $C_{(min)}$ (loop B), and the damping parameter that is described in [202] to estimate the optimized damping values (loop C) for the three topologies. In total, loop steps were selected to evaluate 6300 filter possibilities.

4) Inductance L is calculated considering the value of C and f_{cutoff}. Then, L and C designs are carried out considering the procedures for powder cores and film capacitors described in Section 2.8.1.1 and Section 2.8.1, respectively.

5) Damping parameters R_d, C_d, and L_d are calculated for all three topologies, and filter passive elements are designed (same functions used in step 4).

6) By considering the real filter model, the impedance test Z_{HVDC} is carried out according to Figure 96. The impedance Z_{DC} of the electrical motor seen by the inverter DC side is crucial in evaluating the system's stability. The calculation of Z_{DC} for a PMSM was based on the works of [204], [205], which depends on inverter modulation index m_a, motor synchronous resistance R_s (16 mΩ), and quadrature inductance L_d (550 µH). Z_{DC} associated with filter

impedance, solved from the impedance quadrupole, determines Z_{in} that associated with HVDC line impedance Z_{Line} (1 mΩ + 0.5 µH) must be higher than Z_{HVDC} limit

$$Z_{DC} = \frac{8}{3} \cdot \frac{(R_s + j\omega L_d)}{m_a^2}. \tag{2.46}$$

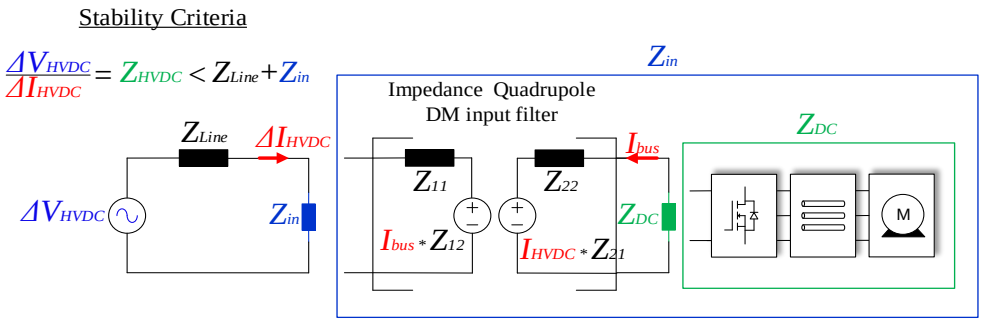


Figure 96 - DM input filter Z_{HVDC} criteria.

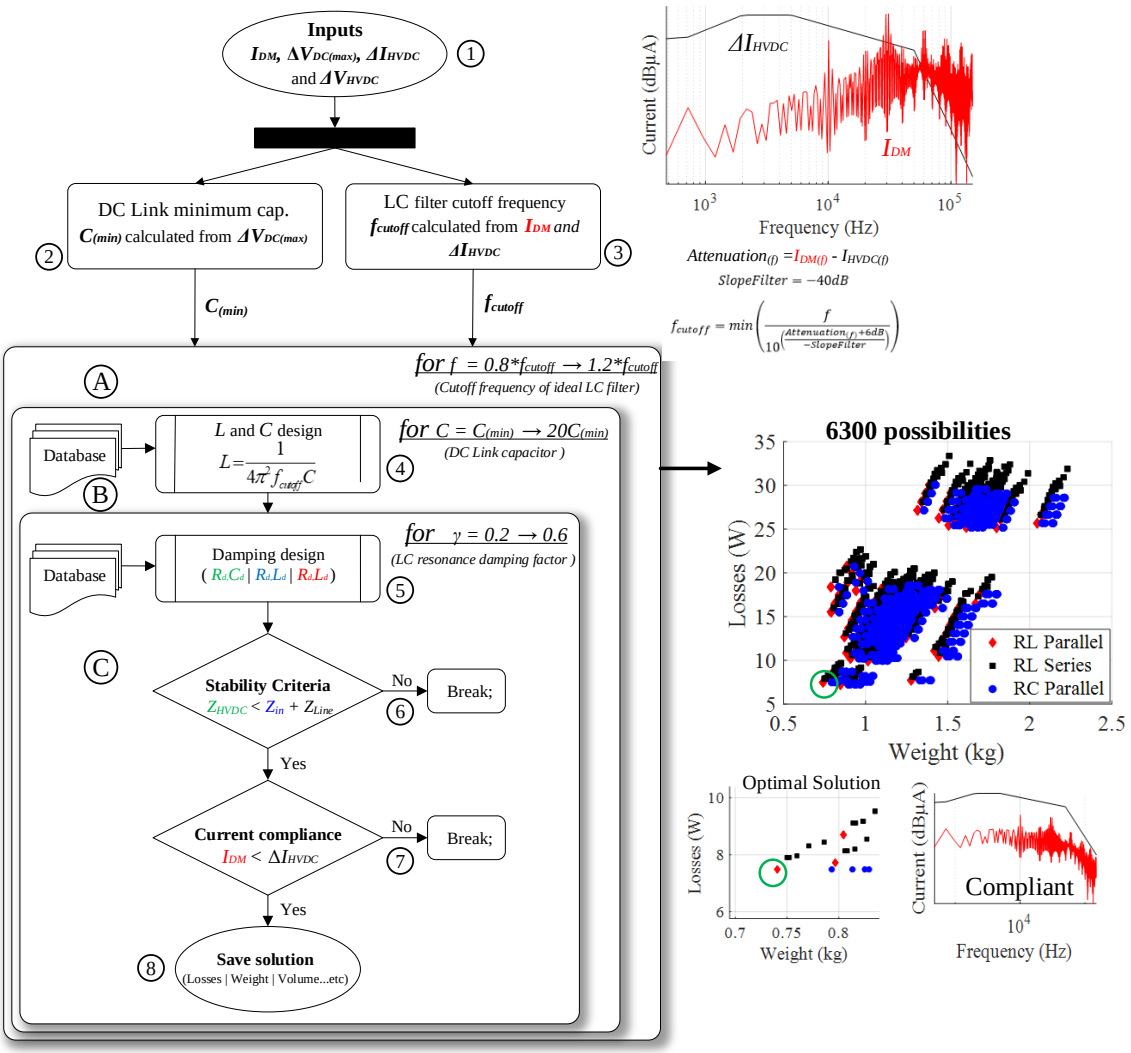


Figure 97 - DM input filter design flowchart.

7) If impedance criteria are satisfied, I_{DM} is compared with ΔI_{HVDC} considering an ideal DC bus voltage.

8) By meeting both criteria, solutions are saved, and the one with the best compromise between losses and weight is selected as the optimal solution.

Figure 98 present the results for the nominal operating point for the topologies previously selected. It is noticed that the DM input filter for the Quasi FC and the 3 – level FC, both with three legs in parallel per phase, have the same DM input filter with the same $C_{(min)}$. Even if the number of voltage levels is different for these topologies since they have the same PWM control, the input current demanded from the DC-Link capacitor for both solutions is the same. The 2 – level topology has heavier solutions with almost 928 g (close to 200 g difference compared to the multilevel topologies) until 30 kHz. Nevertheless, since the current spectra of I_{DM} move to the right with the increase of switching frequency, it is seen that for 70 kHz, the harmonic difference that set filter f_{cutoff} is almost two times compared to the Quasi FC and FC topologies. For this switching frequency, f_{cutoff} reached 1157 Hz for the 2- level topology, while the multilevel topologies DM filter was designed for 9188 Hz.

Consequently, the weight for the 2 –level topology increases to almost 2 kg. The fact of using multilevel topologies allows some harmonic cancelations making that DM input filter can be reduced. Semiconductor technologies do not influence low-frequency behavior, then the results for the 3 -level FC were considered independently of the semiconductor technology (MOSFET Si, MOSFET SiC, or GaN HEMTs).

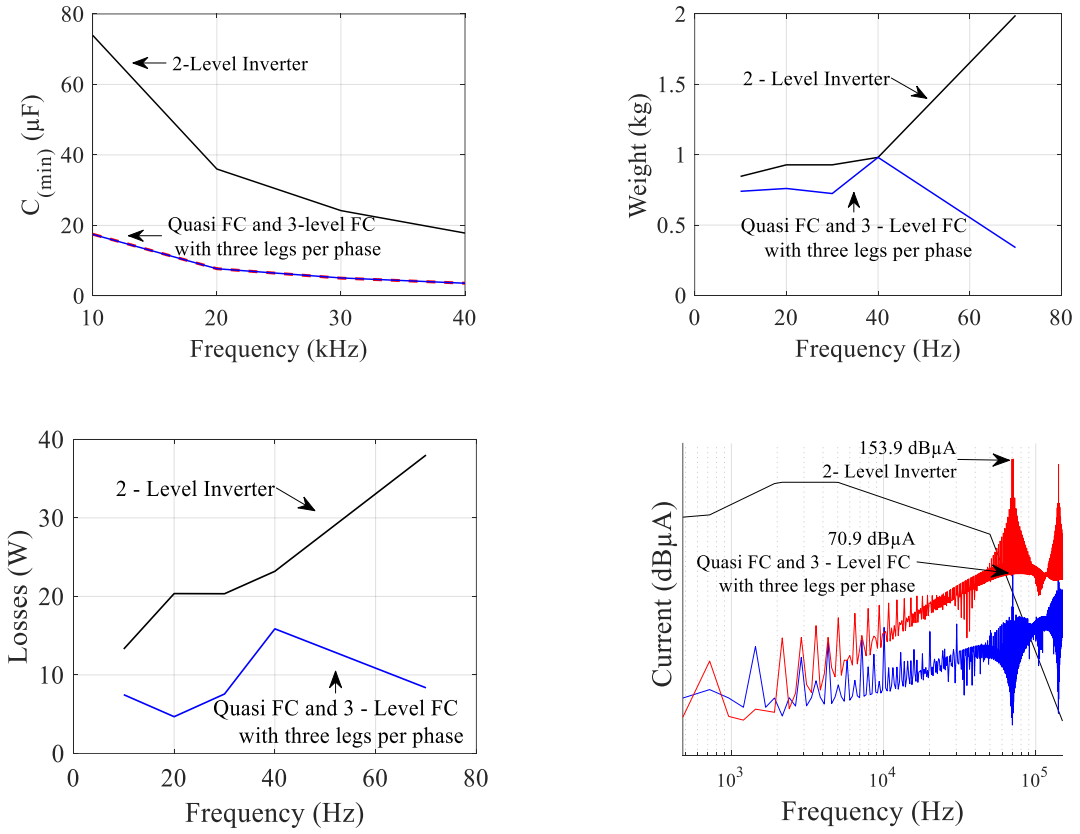


Figure 98 - DM input filter results for V_{bus} = 540 V, DPWM1, 70 kVA, f_{lf} = 240 Hz, m_a = 0.9428 and cos(ϕ) = 0.6435.

On the other hand, one particularity was observed concerning C(min) design for the NPC topologies. Since this topology has the clamped neutral, it was considered connected to the electrical motor's neutral point. There is a current third harmonic (see Figure 99) injected through this point to the DC-Link capacitors. It makes the voltage from each capacitor (C_1 and C_2 in Figure 100) to the neutral to reach high oscillation. This behavior is presented in Figure 100 for the nominal operating point. Even though V_{bus} has an acceptable voltage ripple, the output voltage is highly distorted. $C_{(min)}$ must then be designed to have the desired voltage ripple between the HVDC network connection to the neutral point. In that case, the DC-Link capacitor increases to 917 µF (1834 µF for C_1 and C_2) against 76 µF necessary for the 2-level topology at 10 kHz. This value does not change too much with the switching frequency (at least not between 10 kHz and 70kHz) since it is linked to the system's fundamental frequency (240Hz).

The DC Link capacitor's weight is calculated as 3.28 kg, representing more than three times the weight for the hole DM filter for the 2-level topology. Considering this phenomenon that drastically increases DM input filter weight for the NPC topologies added that this topology also presents a heavier cooling system(at least 50% heavier than FC topologies), it was decided that the global optimization of the inverter will not consider NPC topologies.

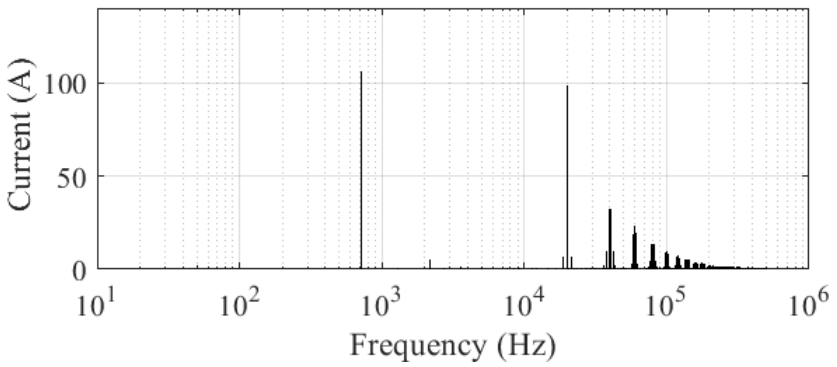


Figure 99 -Third harmonic (720Hz) current injection through the clamped point on NPC topologies.

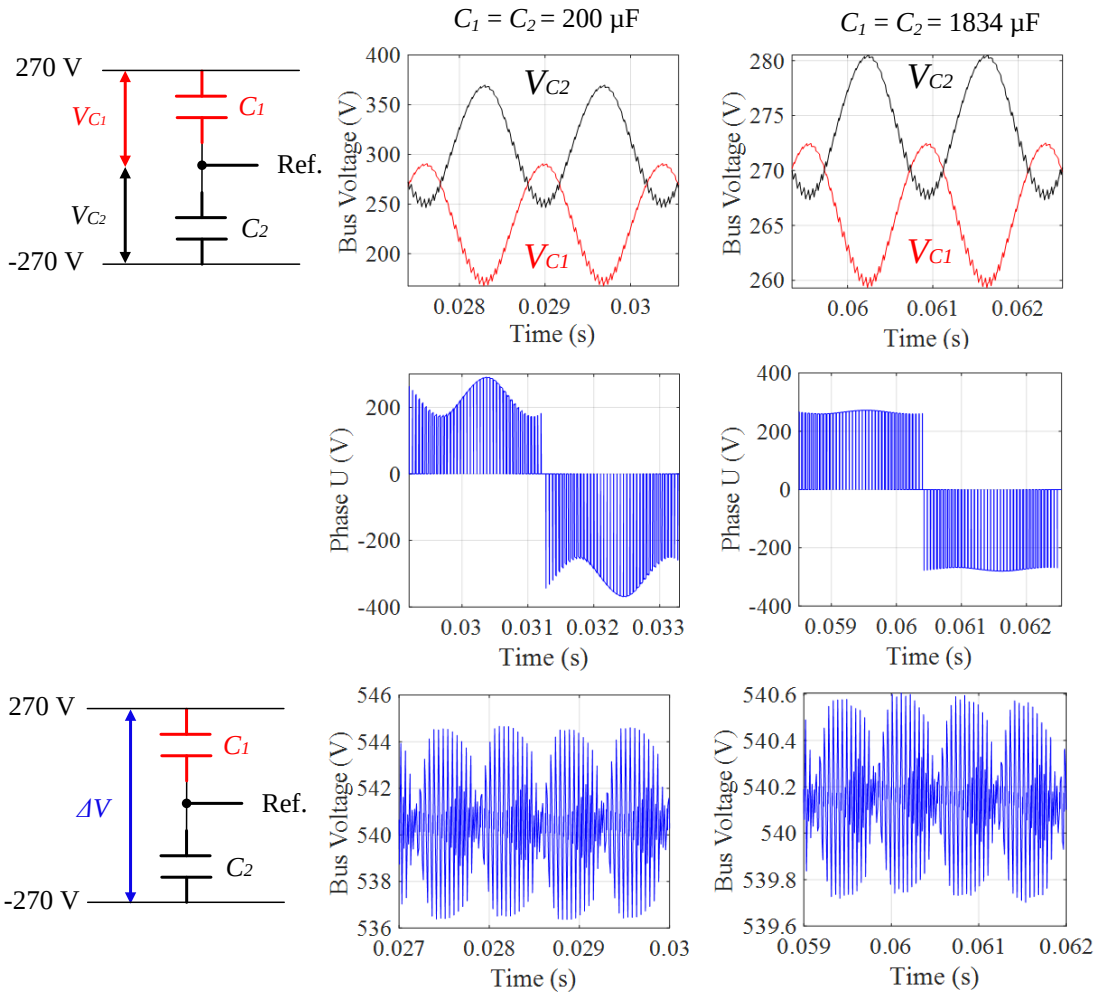
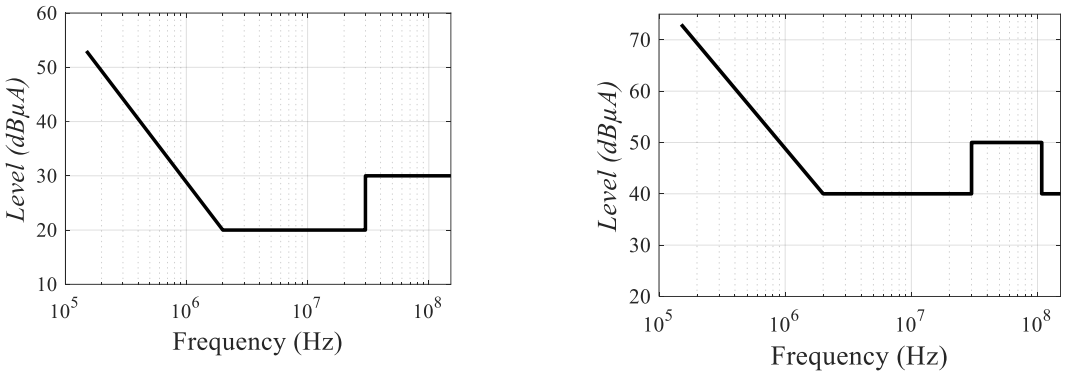


Figure 100 - NPC DC-Link capacitor design problematic.

The following section will present the modeling of CM currents and the design of EMI filters to meet Conducted Emissions (CE) constraints defined by the RTCA/DO-160G. It is worth pointing out that CE in aircraft is mainly due to CM currents, as discussed in [17]. Thus, beyond the decoupling between DM and CM modes, DM input current will not be evaluated with CE, limiting its analysis to the low-frequency criteria presented for the DM input filter.

2.9.5 EMI Modelling: Conducted Emissions – RTCA/DO-160G

Current high-frequency harmonics are considered responsible for EMI Conducted Emissions. Their limits are described in the Environmental Conditions, and Test Procedures for Airborne Equipment, Section 21 – Emission of Radio Frequency Energy – RTCA/DO-160G standard from 150 kHz to 152 MHz for category L, M & H. The limits are separated according to the load characteristic and location. Between the HVDC network and the inverter, the Power Lines limits are considered while Interconnecting Bundles limits are used from the inverter to the electric machine, as presented in Figure 101.



a) Power Lines *b) Interconnecting Bundles*

Figure 101 - Maximum Level of Conducted Emissions RTCA - DO-160G - Category L, M & H.

RTCA/DO-160G imposes a test setup to measure Conducted Emissions (CE), as represented in Figure 102. The tests must be performed with a Faraday chamber to block external and undesirable electromagnetic fields. The power supply is located out of the cage, and it is connected to a Line Impedance Stabilization Network (LISN) that will feed the device under test (DUT). Usually, the load can be emulated outside the chamber, but the electric motor is considered inside the chamber in the present thesis. The main idea is to evaluate the total power drive system contribution in conducted emissions. Current probes are placed 5 cm from the DUT input and output connectors. In the case of the power drive system, the DUT is the power converter with filters that are designed in this thesis.

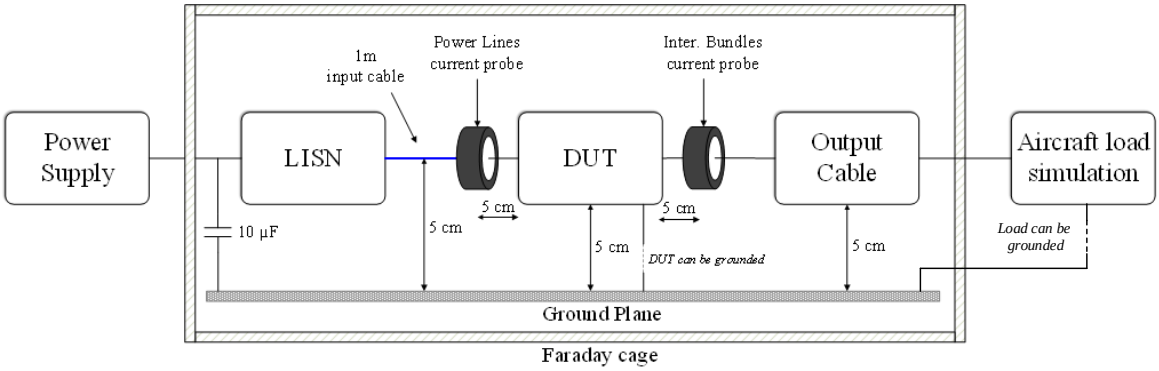


Figure 102 - Conduction Emissions setup described on RTCA/DO-160G.

The DUT, current probes, cables must be 5 cm distant from the reference ground plane. This ground plane corresponds to the aircraft structure and represents the return path for common-mode currents. For the present application, the electric motor carcass is considered directly connected to the ground plane. Loads with a metallic case should also be connected to the ground plane to guarantee equipotentiality and protect against electric shock. Power converters metallic structures are generally connected to heatsink for the same motive. The heat sink is also grounded to reduce Radiated Emissions (RE) as presented in [206] since it can become an efficient antenna if it is not grounded [207]. Nevertheless, this grounding provides an alternative path for capacitive currents between the semiconductor's thermal pad to the ground plane. Figure 103 presents input ($i_{cm\text{-}in}$) and output ($i_{cm\text{-}out}$) CM current preferred path through the different subsystems that compose the power drive system based on the test setup presented in Figure 89.

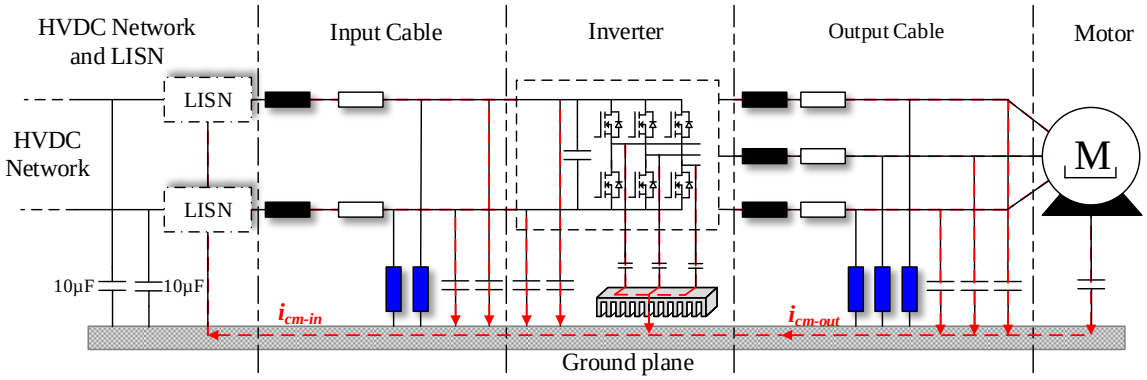


Figure 103 - CM current path in a power drive system based on test setup in Figure 102.

The following sections will present the modeling of each subsystem presented in Figure 103. Motor's preferred CM current path is represented by CM impedance measured and presented in Figure 65. Output three-phase cable modeling and bifilar equivalent circuit were presented in Section 2.9.2.2.1. The other elements as power drive system EMI modeling background, input cable, LISN, and power converters models, are presented below.

2.9.5.1 Power drive system EMI modeling background

EMC is a discipline that becomes more present during power conversion design stages since it is necessary to predict system emissions and susceptibility behavior. In the last 20 years, plenty of works [17], [57], [208]–[212] have been done to understand disturbances and couplings due to EMI CE associated with CM currents in power electronics. In general, EMI modeling is divided into two categories: indirect and direct methods.

Indirect methods are based on time-domain simulation through a circuit simulation tool, and frequency analysis is done in a second moment. This method simulates complex systems by considering the effect of transient due switches stray elements, low-frequency phenomena as motor control, PWM technique, and stability issues. It is also possible to consider non-linearities associated with the different subsystems that compose the primary system (magnetic materials, semiconductor junction temperature, etc.). These reasons make this approach one of the most used in the power electronics domain. This approach's main issue is related to converging numerical methods used to solve the time-domain simulation. Simple modifications on circuit parameters can lead to calculations divergences. Additionally, the finesse of time-domain simulations is associated with using exceedingly small calculation time steps, which increase reasonable calculation time and data volume. Another point against indirect methods is the difficulty of implementing a computationally expensive system in an optimization environment in which several parameters are varied and evaluated.

Direct methods are based on frequency-domain problem resolution. This approach makes it possible to reduce simulation time, data volume by reducing results precision. The simplicity of implementation comes from the predictive modeling of the CM current propagation path. The current path is difficult to establish since it depends entirely on integrating different power drive systems.

Capacitive couplings between heatsink, converters, filters, cables, and motor and ground plane are the main path for CM currents, and prior modeling remains a limiting point. Nevertheless, it is possible to find specialized literature on modeling each capacitive coupling: electric motor [165], [167]; cables [27], [176]; filters[145], [213] and converters[214], [215].

Beyond capacitive coupling, the power converter represents the source of CM noise. Several works present different approaches to model CM propagation path with power converters, as:

1) Modular Terminal Behavior (MTB): It considers one commutation cell as two Norton equivalent circuits. Current sources represent the switch transistor current, and paralleled impedances represent switch stray elements such as parasitic capacitances, inductances, etc. Many measurements are needed to build this model. It becomes challenging to use in the design phase and predictive simulations[216], [217].

2) Unterminal Behavioral Model (UBM): This approach considers a black box impedance quadrupole where the system's different characterization is needed. It is impossible to use this model during the design phase and predictive simulations [218], [219].

3) CM voltage source and input/output impedances: Commonly used in quadrupole and transfer function approached. The main idea is to model an inverter as an input and output impedance and a voltage source as a function of inverter output voltages. Different works are found considering this last approach since it can be easily implemented in a predictive design without much information. One drawback of this technique was extensively used for 2 - level inverters only [17], [208], [210] or for multilevel parallel/parallel switching cells based on 2 - level switching cells [81], [220] that have a similar approach. In the case of multilevel series topologies, the following works were found:

- In [221]–[223], the 2 – level inverter approach is used to propose an equivalent inverter model for MMC topology, but it cannot be used for other topologies as FC or NPC.

- An equivalent model is presented by [224] for a 7 – level cascaded HB (Half-bridge) for photovoltaic application. Each HB has an equivalent CM circuit, and the current return path does the coupling. It is a generic approach that considers one voltage source for each switching cell. However, the coupling with the inverter input considers only the switching cell connected to the inverter output. The other switching cells' current path does not influence input CM current, only output CM current. It is a strong hypothesis, and it was not evaluated in work.

- In the case of FC topology, the work presented by [225] considers only the output voltages of each cell as it is traditionally considered for 2-level topologies. The stray capacitances of the other switching cells not connected to the output do not contribute to CM currents.

The EMI modeling considering the CM voltage source and impedances seems to be the appropriate approach for a predictive design due to its simplicity when there is a lack of information concerning the converter topology. Therefore, this method will be considered in this thesis. On the other hand, there are not many references around multilevel series topologies. A straightforward approach will be made in this chapter to generalize EMI equivalent circuits for any power converter topology.

The goal is to have an estimation of CM input and output filter weight and losses. Deep mode analysis of EMI modeling of multilevel topologies will be presented in Chapter 3.

2.9.5.2 Input cable modeling

Input cables (non-shielded) connect the LISN to the inverter, and the standard fixes it as 1 m, 5 cm away from the ground plane. The same cable used to the output is considered (EN24681-AZA), and modeling comprehends the same procedure of a three-phase cable, but with two conductors, and it can also be represented as a T circuit. It means that CM current will be divided by two and come back through the ground plane, as presented in Figure 104. Then, *RLCG* parameters generated by FEMM simulation, for the equivalent bifilar circuit per unit length, are calculated as:

$$\begin{aligned} L_{CM-c} &= \frac{L_{11}+L_{22}}{2} \;,\; R_{CM-c} = \frac{R_{11}+R_{22}}{2}, \\ C_{CM-c} &= C_{11}+C_{12}+C_{22}+C_{21}, \\ G_{CM-c} &= C_{CM-c}.\omega.\tan\varepsilon_c \end{aligned} \tag{2.47}$$

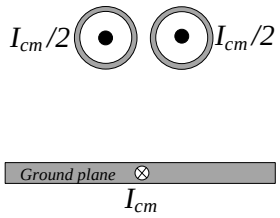


Figure 104 - The 2D problem for input cable CM impedance.

2.9.5.3 Line Impedance Stabilization Network modeling

Almost all normative tests specify Line impedance Stabilization Network (LISN). It guarantees a known impedance in a frequency range and isolates HVDC network impedance from DUT to allow a reproducible measurement. LISN impedance is standardized by CISPR (*Comité International Spécial des Perturbations Radioélectriques*) in section 16.1.1 over the frequency range 150 kHz to 152 MHz. One LISN shall be connected to each power connection (two), leading to the equivalent circuit in CM according to the standards values. This figure also shows the equivalent CM impedance of 2 LISNs (ESH3-Z6) and the calculation using the ideal *RLC* recommended by the standard. The input capacitance of 10 µF is specified from RTCA/DO-160G G to filter CM currents from the HVDC network.

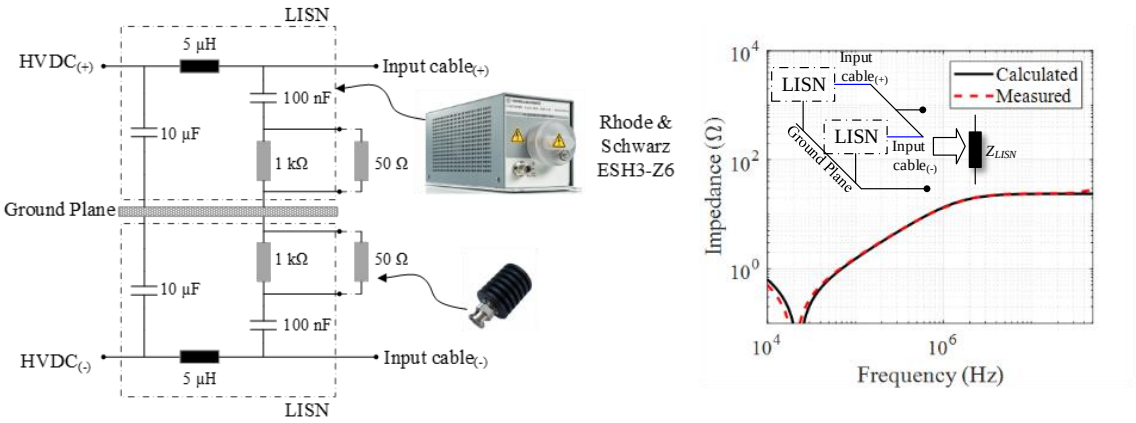


Figure 105 - LISN equivalent circuit and impedance compliant with RTCA/DO-160G.

2.9.5.4 Power Converter EMI modeling

In the present thesis, it will be neglected the CM to DM mode transfer phenomena. Additionally, as already highlighted at the end of Section 2.9.4, EMI filters are mainly determined by CM currents. Therefore, the focus in this section will be given to the modeling of these currents.

Input and output CM current is inherently coupled through the ground plane, as presented in Figure 103. According to the background section's works, a three-phase 2-level inverter topology can be modeled as an input impedance $Z_{inv\text{-}in}$ (mainly due to DC bus PCB tracks), a CM voltage source V_{cm} and one output impedance $Z_{inv\text{-}out}$ as presented in Figure. PCB integration is responsible for inverter input impedance, while semiconductors stray capacitances to the heat sink (grounded) are responsible for inverter output impedance. Heat sink can be connected directly to converter metallic or through a ground braid or an impedance, represented by Z_{braid}.

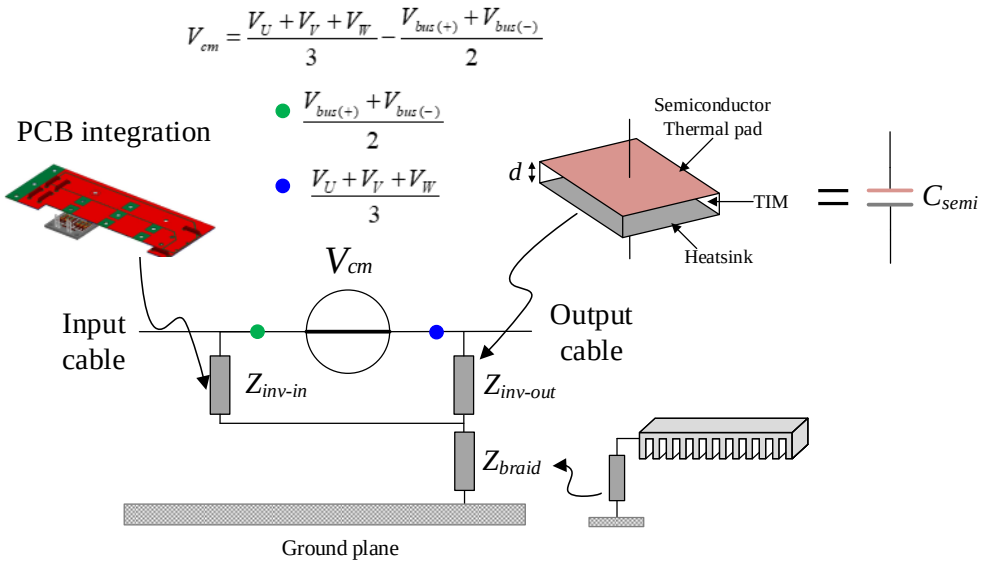


Figure 106 - Three-phase inverter EMI equivalent model.

CM equivalent voltage source V_{cm} is calculated considering the difference between the mean value of inverter output voltage (V_U, V_V, and V_W) and inverter input voltage (positive and negative bus voltages). This equivalent voltage source is considered in [17], [226]. The input voltage can be neglected for an ideal converter where bus impedances (positive and negative connections) are equilibrated.

Therefore, the equivalent model to estimate input and output CM current in a power drive system can be represented as a bifilar circuit according to Figure 107, where input and output filter impedance is already considered. CM input filter is composed of a series impedance $Z_{filter\text{-}in\text{-}S}$ that limit CM current from the input (it also helps limit CM current from the HVDC Network in the real application). It represents the impedance of the input CM choke ($L_{CM\text{-}in}$) described in Section 2.8.2.2. The paralleled impedance $Z_{filter\text{-}in\text{-}P}$ provides a preferred path for the returning current generated from the inverter output. It represents the impedance of two paralleled $C_{y\text{-}in}$ capacitors (MKP Y2 family) presented in Section 2.8.1.

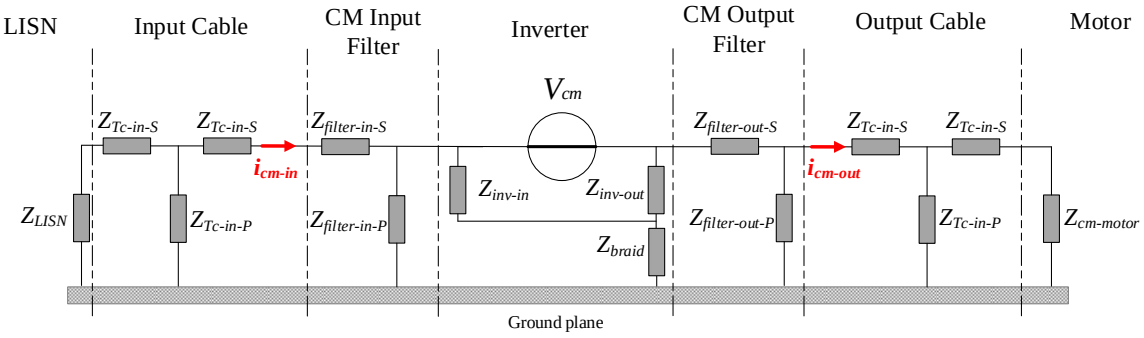


Figure 107 - EMI equivalent model of a power drive system with test setup DO-160G.

CM output filter is composed of $L_{CM\text{-}out}$ presented in Figure 86 and represents the series impedance $Z_{filter\text{-}out\text{-}S}$. It concerns the three-phase CM choke designed in Section 2.8.2.2. It increases the impedance on the output current path due to output cables and motor impedances. On the other hand, the parallel impedance $Z_{filter\text{-}out\text{-}P}$ provides a preferred path for output current $i_{cm\text{-}out}$ and limits part of this current that returns through $i_{cm\text{-}in}$. This impedance represents the C_y in Figure 86. Figure 108 shows both input and output CM filter topologies considered in this thesis.

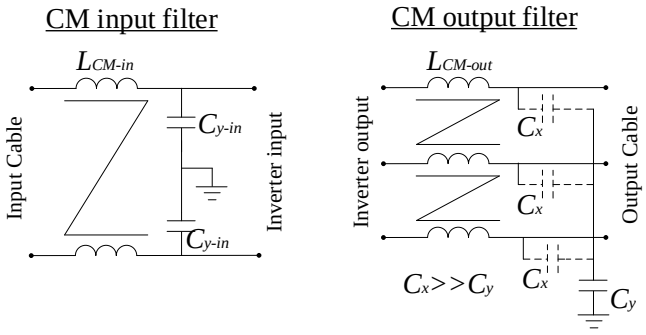


Figure 108 - Input and output CM filter topologies considered in this thesis.

The main limitation of the equivalent model presented in Figure 107 is that only the parasitic capacitances connected to each leg output voltage are considered. For example, in the case of a flying

capacitor topology, the parasitics capacitances in blue in Figure 109 connected to the flying capacitor will also have a *dV/dt*. Thus, a CM current will pass through these capacitances, contribute to icm-input and represent a path to the return of $i_{cm\text{-}out}$.

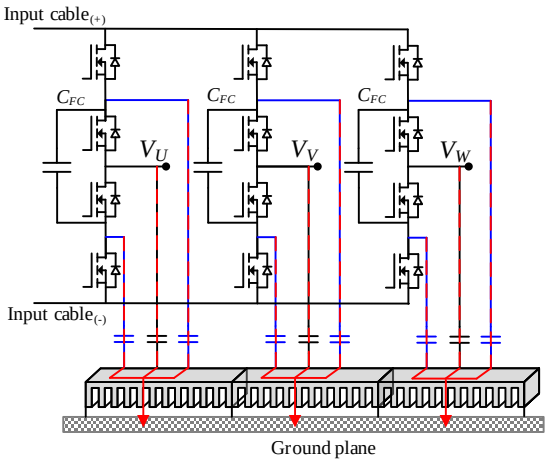


Figure 109 - Input and output CM filter topologies considered in this thesis.

For a preliminary estimation of input and output CM filters weight and losses, this problem is divided into two subcircuits decoupling $i_{cm\text{-}in}$ and $i_{cm\text{-}out}$. By decoupling these two currents, it is possible to consider current passing through capacitances not connected to inverter output connecting. The first circuit considers that $i_{cm\text{-}in}$ is generated mainly due to inverter impedances ($Z_{inv\text{-}in}$ and $Z_{inv\text{-}out}$) since it is supposed that $Z_{filter\text{-}out\text{-}S} >> Z_{inv\text{-}out} + Z_{braid}$. On the other hand, the second circuit only considers that the icm-out path is formed by output cable and motor impedances. This approach is presented in the following sections, as well as the optimization procedure. Optimization was carried out with the coupled model presented by varying input and output CM filter parameters to identify the discrepancy against the proposed model.

2.9.5.4.1 Input CM current modeling

Input CM current is calculated according to the circuit presented in Fig. Ground braid impedance was considered 1 mΩ and 1 µH. Inverter input impedance $Z_{inv\text{-}in}$ was modeled as a 970 pF capacitance according to a power converter [17].

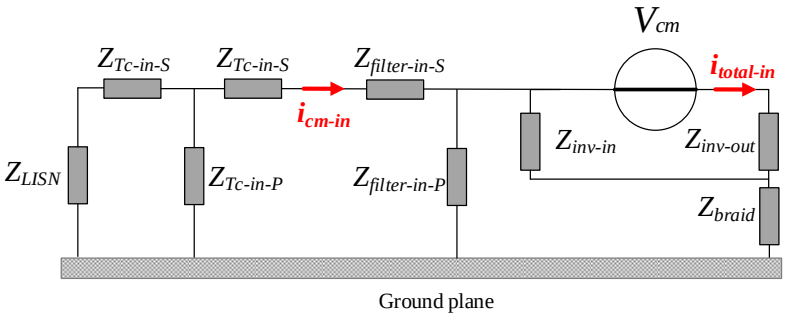


Figure 110 - Decoupled proposed model to calculate input CM current.

$V_{cm\text{-}in}$ is calculated considering the total current $i_{total\text{-}in}$ leaving this voltage source, assuming $Z_{inv\text{-}in} >> Z_{filter\text{-}in\text{-}P}$ and $Z_{inv\text{-}out} << Z_{filter\text{-}in\text{-}P}$:

$$i_{total-in} = \sum_{n=1}^{k} i_{c-semi}(n) = \sum_{n=1}^{k} \frac{V_{c-semi}(n)}{Z_{braid} + Z_{c-semi}}$$
$$i_{total-in} = \frac{1}{Z_{braid} + Z_{c-semi}} . \sum_{n=1}^{k} V_{c-semi}(n) \quad (2.48)$$
$$V_{cm-in} = \sum_{n=1}^{k} V_{c-semi}(n) \therefore Z_{inv-out} = Z_{c-semi}$$

Where $i_{c\text{-}semi}$ corresponds to the current passing to each semiconductor parasitic capacitance ($C_{c\text{-}semi}$) to the heatsink and $Z_{c\text{-}semi}$ corresponds to the impedance due to this parasitic capacitance. Then $V_{cm\text{-}in}$ is calculated as the sum of all voltage waveforms applied to all $C_{c\text{-}semi}$ present in the circuit. This parasitic capacitance depends on the surface of the semiconductor thermal pad and TIM material. According to HI-Flow300P considered in the Cooling System design (Section 2.7), $C_{c\text{-}semi}$ is calculated for each converter topology in Table 15, considering the capacitor with two paralleled plates:

$$C_{c-semi} = N_p . \frac{\varepsilon_{TIM} . A_{semi}}{d_{TIM}} \quad (2.49)$$

N_p is the number of transistors in parallel. A_{semi} is the semiconductor surface in contact with TIM that depends on the semiconductor package, d_{TIM} (0.102 mm) ε_{TIM} (3.984×10^{-11} F/m) are TIM thickness and permittivity, respectively.

Table 15 - Calculation of each inverter topology considering HI-Flow300P.

Topology	Semiconductor	N_p	A_{semi} (mm^2)	$C_{c\text{-}semi}$ (pF)
2-level	1200 V SiC MOSFET HT3201RVB	1	-	403*
2-level	1200 V IGBT SKM600GA12E4	1	-	403**
Quasi FC	650 V GaN GS66516T	4	46.6	186.56
FC 3-level	650 V GaN GS66516T	4	46.6	186.56
FC 3-level	600 V Si MOSFET IPZ60R017C7	3	172.4	517.2
FC 3-level	650 V SiC MOSFET SCT3017AL	2	172.4	344.8

* Given by supplier

**Considered as the same as the 1200V SiC MOSFET HT3201RVB

The optimization flowchart for the CM input filter is presented in Figure 111. The calculation of f_{cutoff} is like the one used for the DM input filter design but with the Power lines limits ($I_{PL(RTCA/DO\text{-}160G)}$) showed in Figure 101 - a). The same selection process described for the DM output filter selects a CM input optimized solution. $L_{DM\text{-}in}$ and $C_{y\text{-}in}$ design considered the procedures and equivalent circuits presented in Section 2.8.2.2 and Section 2.8.1, respectively.

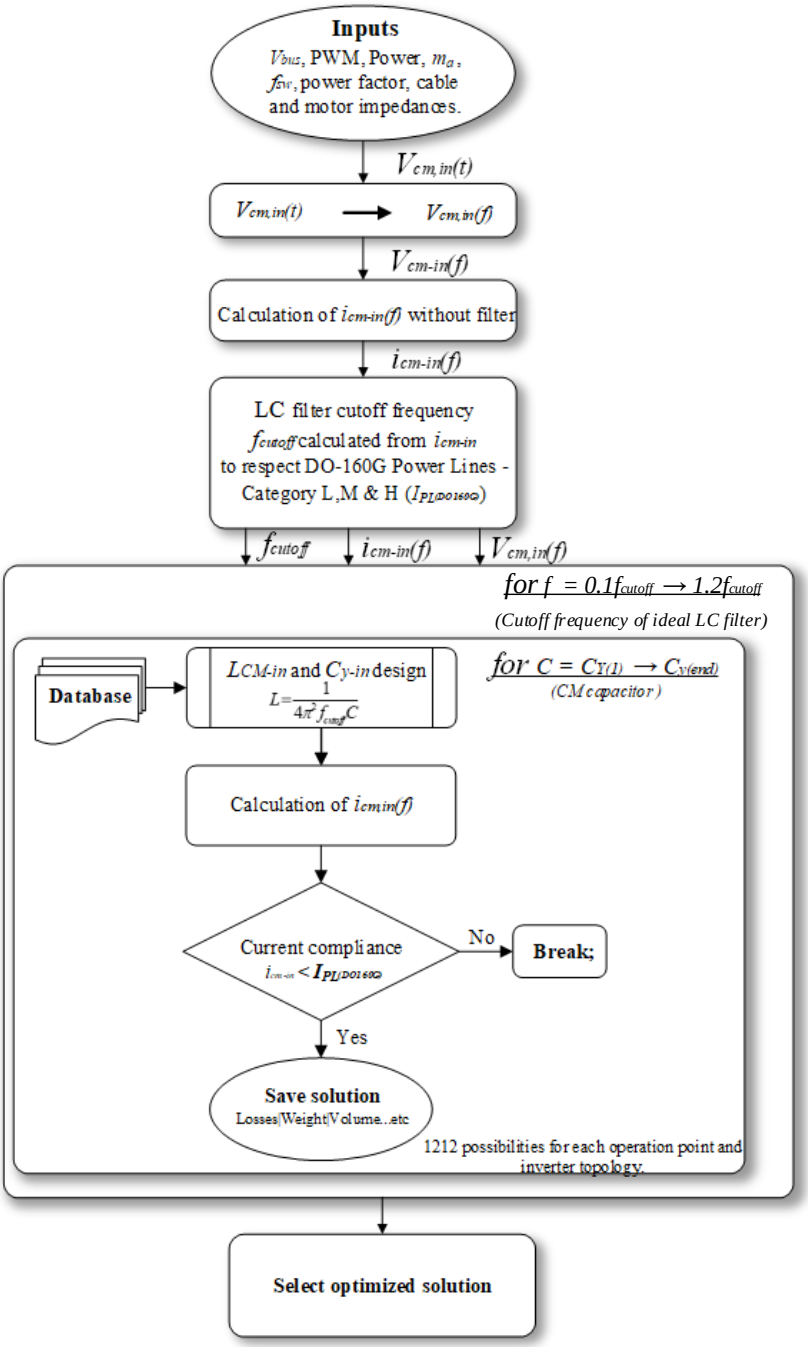


Figure 111 - CM input filter design flowchart.

The following section will present the modeling of the inverter output CM current used to design the output CM filter.

2.9.5.4.2 Output CM current modeling

CM output current i_{cm-out} is calculated considering that the current path is mainly due to output cable and motor, and the equivalent circuit is presented in Figure 112. Additionally, it is considered that

the CM input filter imposes an inverter input impedance ($Z_{inv\text{-}in}$) ≈ 0. In that case, $V_{cm\ out}$ is calculated as the weighted sum of the 3 voltages of the inverter's output, as (V_U + V_V + V_W)/3. The optimization procedure of the CM output filter is like the CM input filter presented in Figure 111. Beyond the equivalent circuit to estimate CM output current, the limit to be respected is the Intercon. Bundles are presented in Figure 101 – b). $L_{DM\text{-}out}$ and C_y design considered the procedures and equivalent circuits presented in Section 2.8.2.2 and Section 2.8.1, respectively.

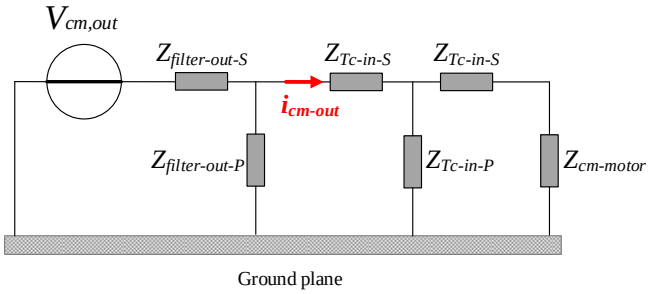


Figure 112 - Decoupled proposed model to calculate output CM current.

Once the modeling of CM input and output currents is presented, the following section will present the optimization results considering both models separately and solved through transfer function.

2.9.5.5 Optimization Results

Optimization solutions as a function of switching frequency are presented in Figure 113 by varying different optimization flowchart parameters for CM input and output filter.

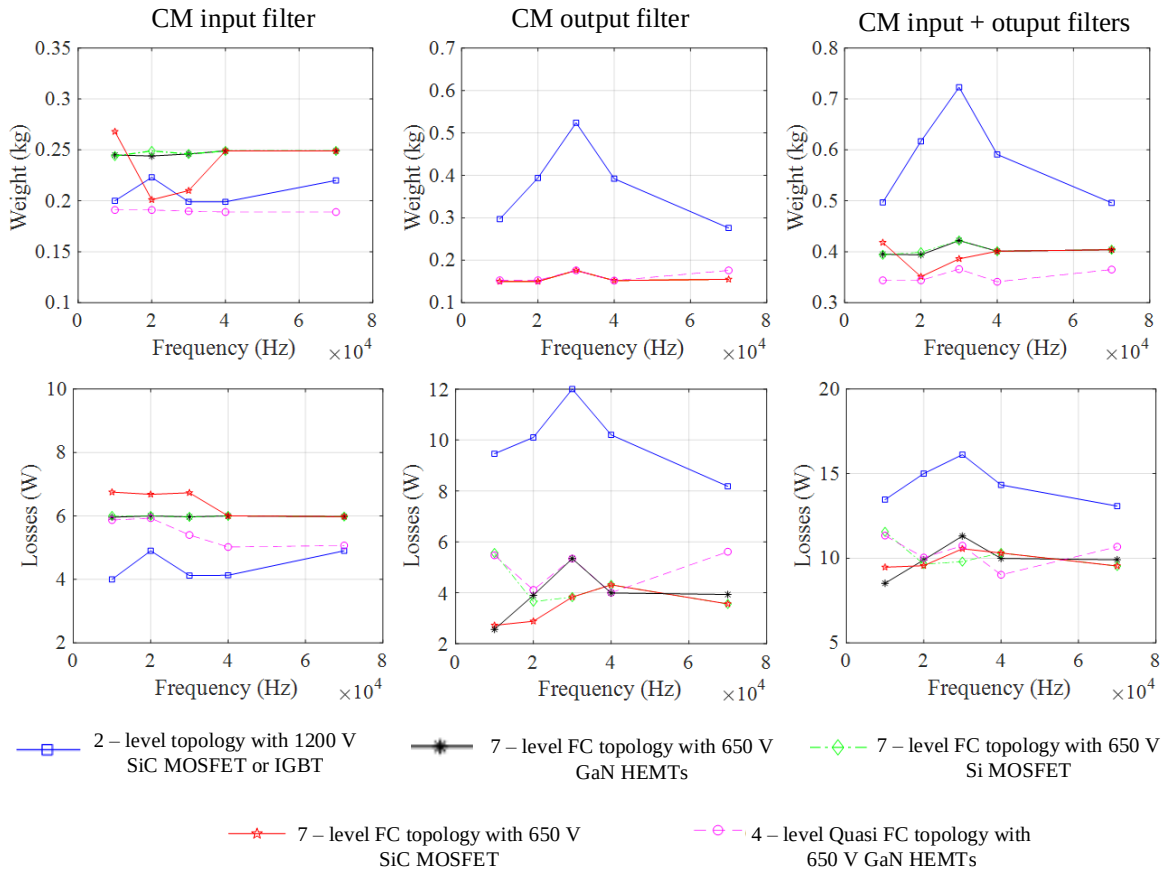


Figure 113 - Optimized CM input and output filters weight and losses for uncoupled models.

The same inverter condition presented in the DM input filter design was considered. Semiconductors switching speed CM was also considered for each solution according to Table 14.

CM input filter solutions have between 200 g and 300 g with losses in the range of 4 W and 7 W. In that case, only winding losses were considered due to a lack of information about Steinmetz parameters for nanocrystalline cores. The difference between multilevel topologies and 2 – level inverters is more evident in the output CM filter, with 510 g against 176 g for multilevel topologies at 30 kHz. Considering both input and output filters, it is necessary around 723 g against 386 g for the 7 – level FC with 650 V GaN HEMTs, at 30 kHz to respect CE limits. It represents a difference of 46.6%, while losses difference is around 33.7% (5.5 W). It is worth pointing out that the input CM filter is designed according to the resonance between Z_{braid} and $Z_{inv\text{-}out}$ for all inverter topologies. It is exemplified in Figure 114 for the 2 -level topology at 30kHz. This fact calls attention to the importance of a good connection between the heatsink and the ground plane.

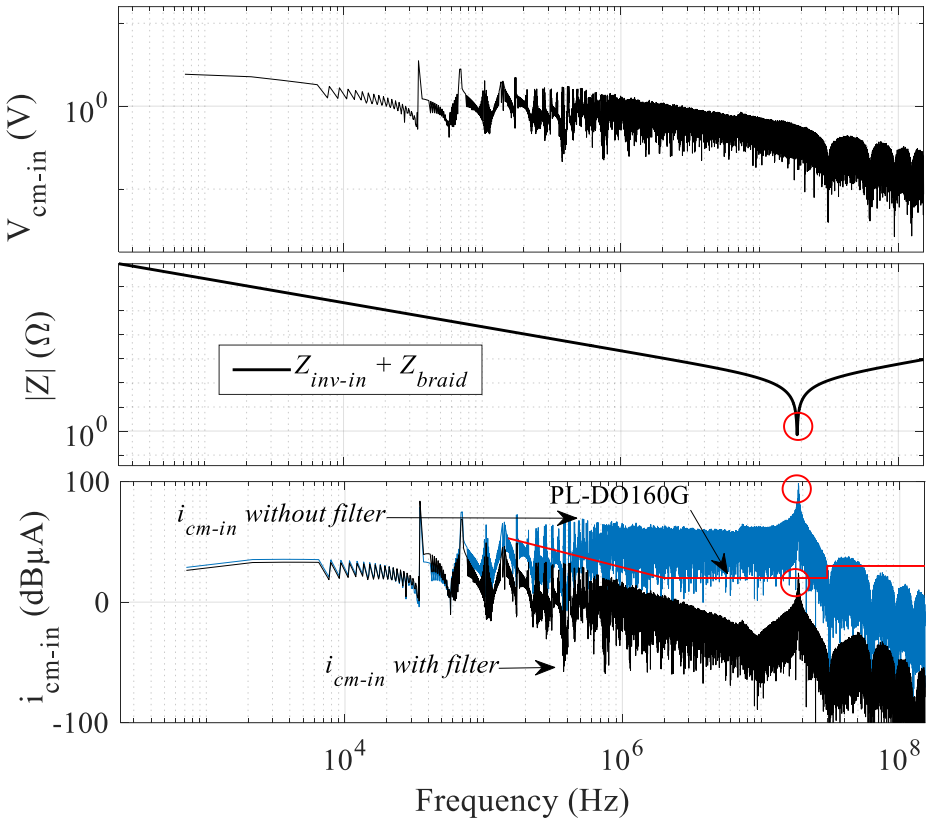


Figure 114 - Effect of resonance between Z_{braid} and $Z_{inv\text{-}out}$ on the design of CM input filter.

In order to verify the discrepancy in filters weight and losses by decoupling input and output CM currents proposed in this section, the optimization procedure was also applied for the coupled system shown in Figure 107 that is valid for 2 – level topology, among the topologies that are studied in this thesis. This optimization procedure considers the variation $L_{DM\text{-}in}$, $L_{DM\text{-}out}$, $C_{y\text{-}in,}$ and C_y simultaneously, then verifies the input and output current compliance for all possibilities. This procedure was implemented for the 2 – level topology with 1200 V SiC MOSFET for the same operating condition to generate Figure 115. The results are presented in Figure 115 compared to those with the uncoupled model presented in Figure 113. In general, coupling input and output CM currents reduce output filter weight, whereas the input filter becomes heavier. It happens because the current path will see the input cable, LISN, and CM input filter impedances of $i_{cm\text{-}out}$. It will increase current path impedance and reduce $i_{cm\text{-}out}$.

Consequently, filter weight is also reduced. On the other hand, part of $i_{cm\text{-}out}$ will return through these identical impedances and increase $i_{cm\text{-}in}$, increasing the CM input filter. The maximum difference was verified at 30 kHz and 40 kHz with an increase of 100 g (50%) on the coupled model's input CM filter. Nevertheless, regarding the maximum difference between global results (both filters together), there is a difference of 146 g (22%) for 70 kHz and 60 g (9%) for 40 kHz. Regarding losses, the maximum difference is verified at 40 kHz. CM filter losses represent less than 3% of semiconductor losses, then the impact of inverter overall efficiency with all filters and cooling systems are less impacted.

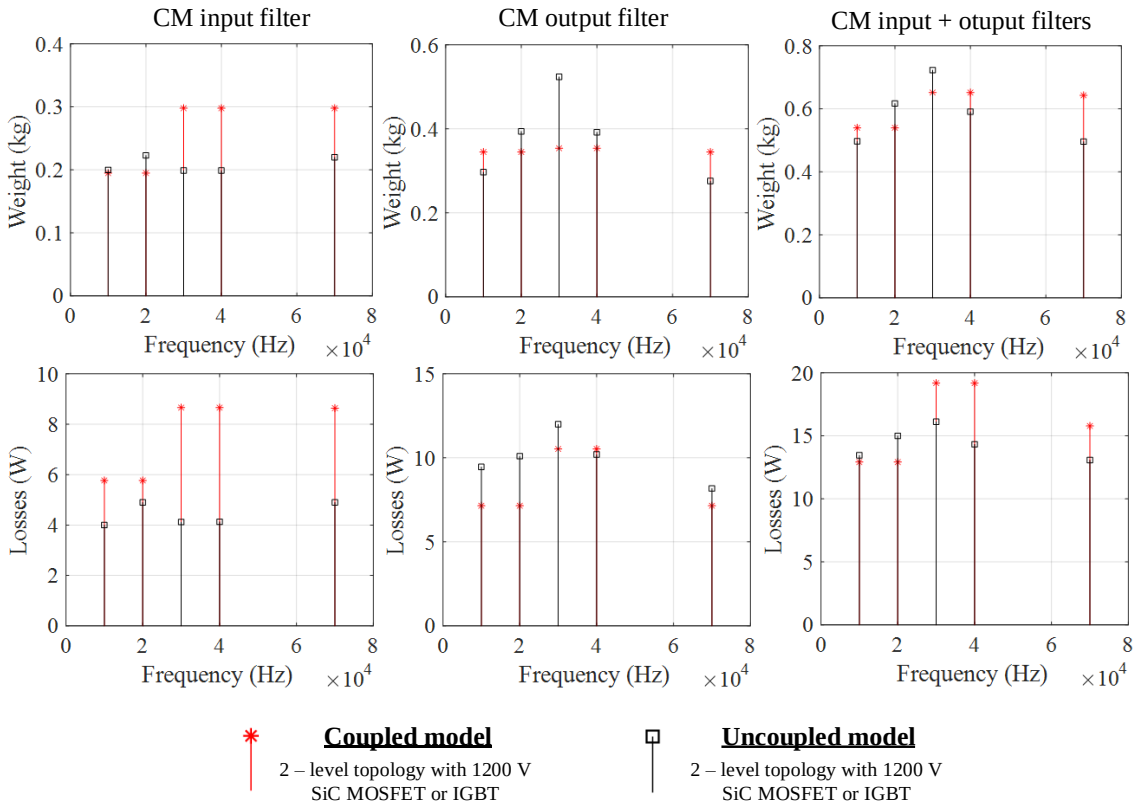


Figure 115 - Optimized CM input and output filters weight and losses for uncoupled models.

Compared to the coupled model, the proposed uncoupled model approximates CM input and output filter weight with a maximum error of 22% verified at 70%. The following section presents the global optimization results considering the models presented until this point, with the pre-selected semiconductors and inverter topologies.

2.10 Global Optimization Results

Previous sections were dedicated to the present literature and the models used to form the design bricks necessary to compose a power converter to meet different aeronautical constraints. This section presents the global results of the complete inverter with all filters and cooling systems. Generally, each design brick varies with different parameters to find the best solution considering weight and losses. This study's main objective is to identify an excellent topology to be deeply investigated in this thesis's following chapters. To select this topology, the criteria η-ρ Performance Space evaluated in [227] is considered. This methodology considers Pareto curves of efficiency (η) and power density (ρ) for different conditions or possibilities. This thesis aims to identify a power converter with gravimetric power density superior to 8 kW/kg with an efficiency superior to 98.5%.

According to semiconductor losses calculation, DPWM1 may present lower losses than other techniques resulting in a lighter cooling system. Since semiconductor losses may represent more than 60% of solution losses, this technique compared pre-selected inverter solutions in Section 2.6. NPC

topologies were not considered due to overweight, mainly due to the DM input filter, as presented in Section 2.9.4.

The flowchart presented in Figure 116 represents the optimization sequence for each condition, switching frequency, and inverter topology. Motor and cable impedances were previously measured and calculated with the FEMM tool, respectively. Each design block optimizes its respective devices separately, except for flying capacitors, semiconductor losses, cooling system, and DM input filter. These blocks are highly dependent on the inductors' current ripple to connect legs in parallel or DM output filter. These devices were then designed, then each leg current was calculated with ripple and transferred to calculate semiconductor losses, cooling system, flying capacitor, and DM input filter.

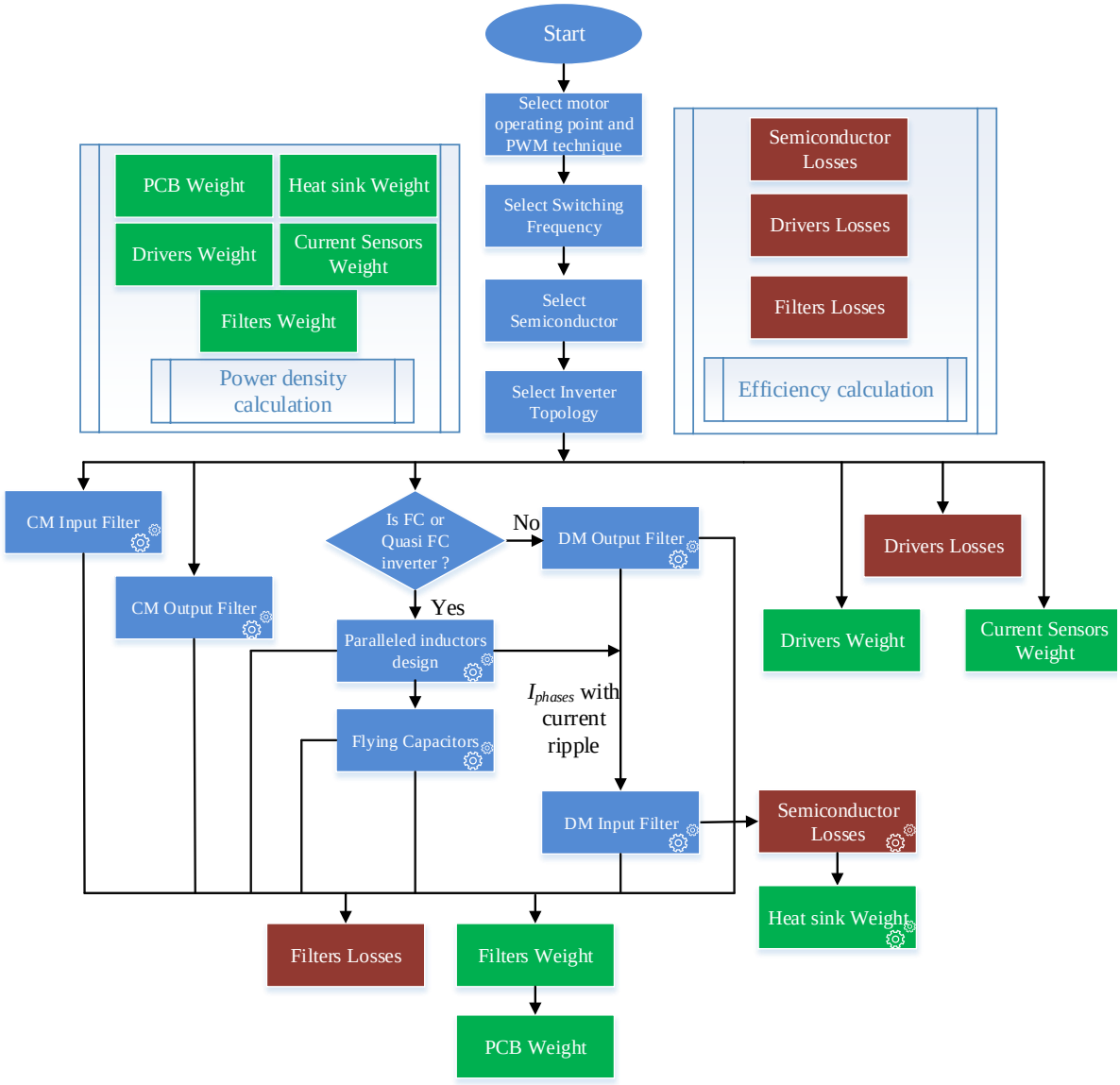


Figure 116 - Optimization flowchart with design blocks presented in this chapter to design an inverter to meet aeronautical constraints presented in Section 1.3.2.

Current sensors weight was estimated considering LEM® products:

- DC link voltage and current: 55 g (voltage sensor DVC 100-B) + 40 g (current sensor LA200) for all topologies.

- Output current sensor (from LEM®): LA200 (40 g) used per phase for 2 – level topology while LA55 (18 g) is used per leg, for 7 – level and 4 – level topologies.

Driver weight estimation is based on the converter designed by IRT Saint Exupery. For a 2 – level topology with a SiC power module, each switch's driver is around 64 g. For topologies with TO-240 devices (600 V Si and 650 V SiC MOSFET), it is considered 32 g per switch, while 16 g was considered for topologies with GaN HEMT. Driver's losses were neglected for this study due to a lack of information.

PCB weight estimation is divided into three parts. The first part considers a motherboard that will be the interface board between switching cells and filters PCBs. A fixed weight was considered 465 g based on a 70 kVA inverter designed by IRT Saint Exupery. The second part considers the PCB used to connect each filter. In that case, an estimation of 176 g/kg of the filter is considered. This estimation is also based on a previously designed filter for a power converter. The third part considers the switching cell or converter leg for the multilevel topologies with different PCBs, approximating the copper weight. Each topology has a different number of semiconductors than different dimensions. By considering a 4 - layer PCB (each layer with 70 µm of copper), different dimensions according to the equivalent semiconductor surface per inverter leg (copper density approximately 0.00896 g/mm^3), leads to 23 g per leg for 7- level and 4 - level topologies with GaN HEMTs. The other 7 - level topologies have around 37 g and 33 g, using 600 V Si and 650 V SiC MOSFET.

Figure 117 shows η-ρ for switching frequency and different inverter selection topologies. The traditional 2 - level topology based on 1200 V IGBT (light blue) does not reach the minimum efficiency and gravimetric power density values. At 10 kHz, this inverter has 19.9 kg and 1742 W of losses, which leads to power density and efficiency of 3.51 kW/kg and 97.5%, respectively. The designed filters for this topology are practically identical to those designed for the 1200 V SiC 2 - level, so the weight difference between these solutions is due to the cooling system. The IGBT solution's cooling system has 1.3 kg, while the 1200 V SiC solution has half this weight at 10 kHz. The significant difference in vertical between solution curves is due to semiconductor losses, 1516 W and 412 W for the solutions with IGBT and SiC, in that order.

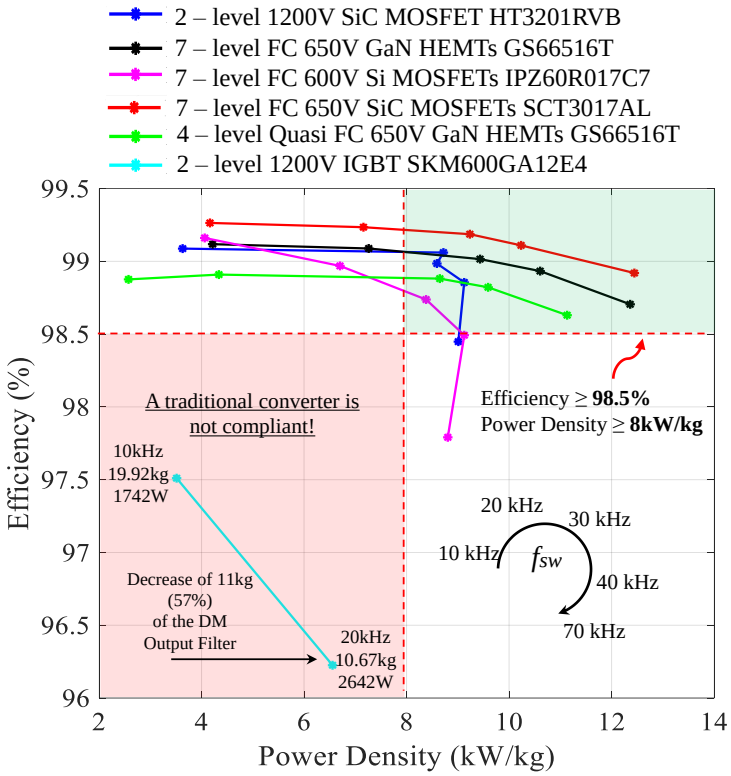


Figure 117 - Optimization results of different inverters topologies (7-level FC, 4 – level Quasi-FC and 2-level) with different semiconductor technologies (IGBT-Si, SiC MOSFETs, and GaN HEMT) for switching frequencies from 10 kHz to 70 kHz. Note that IGBT 2-level topology does not comply with power density and efficiency objectives. Nominal power = 70 kVA, V_{bus} = 540 V, and DPWM1.

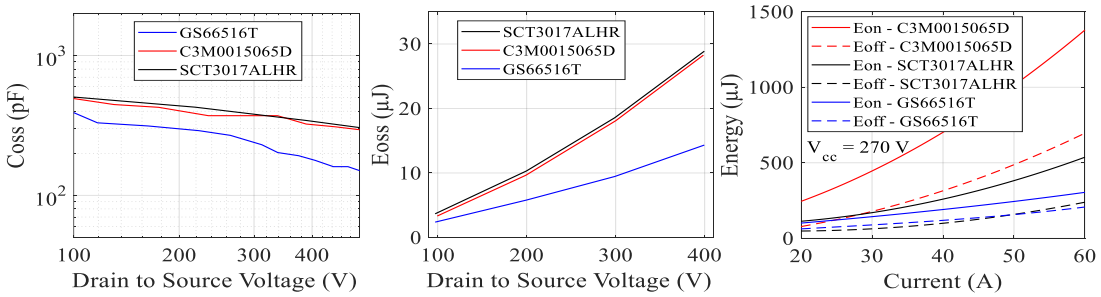
At the switching frequency of 20 kHz, there are a considerable weight reduction in the DM output filter (13.78 kg to 3.86 kg) for 2 - level inverter solutions. At the same time, semiconductor losses increase from 1516 W to 2485 W (IGBT solution). Semiconductor losses increase the high switching frequency. Since the 1200 V IGBT inverter does not satisfy efficiency criteria even for 10 kHz, the switching frequency was limited to 20 kHz for this solution.

Red, black and pink curves present the same multilevel topology, formed by nine legs of a 3-level FC topology, connected three by three via uncoupled inductors. The difference between the curves is the semiconductor technology, 650 V SiC MOSFET (red), 650 V GaN HEMT (black), and 650 V Si MOSFET (pink). It implies that filter weight, PCBs, and drivers for these topologies have similar values. The difference between the curves is directly related to the semiconductor losses and the cooling system weight.The impact of transistors technologies on filter weight is caused by *dV/dt* and overvoltage at the inverter output. Nevertheless, this will only change behavior for frequencies above 30 MHz [17], and it is strongly related to inverter integration. Since this study does not consider PCB routing and inverter integration, filters for these topologies were considered equal.

The solution with 650 V SiC MOSFET has lower losses than the GaN solution, 432W against 525 W at 10 kW and 690 W against 566 W at 40 kHz. According to the datasheet of the SCT3017ALHR (650 V SiC MOSFET), the tests carried out for switching energies considered a gate resistance equal to 0 Ω. Low values of gate resistance increase *dV/dt* and overshoots in inverter output connections [228].

High-speed switching (high *dV/dt*) can increase EMI problems [122], [146] and overvoltage in motor terminals.

The questioning of the information for the 650 V/17 mΩ SiC MOSFET SCT3017ALHR available on its datasheet, regarding switching losses, are based on the information shown in Figure 118, comparing this device with the new 650 V/15 mΩ SiC MOSFET C3M0015065D (released after January 2019, after the study presented in Figure 117) and the 650 V/25 mΩ GaN GS66516T. The SiC devices have the same packaging and similar C_{oss} and E_{oss} as presented in Figure 118 (a) and (b). The GaN, on the other hand, has almost half of E_{oss} compared to SCT3017ALHR, at 300V. In the 3-level FC leg, these devices handle 270 V in nominal operating point, and switching energies for the three devices, for this voltage, are presented in Figure 118 (c).



(a) C_{oss} *(b) E_{oss}* *(c) E_{on} and E_{off}*

Figure 118 - Comparison between 650V SiC MOSFETs SCT3017ALHR, C3M0015065D, and 650V GaN GS66516T.

At 40 A, the E_{on} is ≈ 2.8 times superior for the C3M0015065D and ≈ 2.6 times superior at 60 A. The tests were carried out with $R_{G\text{-}external}$ = 2.5 Ω ($R_{G\text{-}internal}$ = 1.5 Ω) and V_{GS} = 15/-4 V for the C3M0015065D, which characterizes a real application. At the same time, SCT3017ALHR considers $R_{G\text{-}external}$ = 0 Ω ($R_{G\text{-}internal}$ = 4 Ω) and V_{GS} = 18/0 V. If compared to the GaN, the SCT3017ALHR has almost the same values for E_{off} and quite close for E_{off} until 40 A, even if the C_{oss} of the GaN is around 85% of SiC. Regarding C_{iss} (based on datasheet information), SCT3017ALHR has around 2.9 nF while the C3M0015065D has 5 nF, suggesting that the C3M0015065D has higher switching energies, but not by a factor of 2.6 to 2.8 times. According to the datasheet, the GS66516T has only 18% of the SCT3017ALHR C_{iss}, but they are still supposed to have similar switching energies. Therefore, SCT3017ALHR characterization is required with gate resistance value used in a real application to estimate more reliable switching energies. Another critical factor is that this SiC has a TO-247 package, a parasitic inductance in the terminals of approximately 7 nH [229], and it does not have a Kelvin connection.

600 V Si MOSFET solution (pink in Figure 117) has higher losses than the other multilevel solutions for switching frequencies higher than 20 kHz (660 W versus 576 W - solution with GaN HEMT 30 kHz). Therefore, it presents lower efficiency and consequently higher heat sink weight than the others (1455 g versus 913 g - solution with GaN HEMT transistor - at 30 kHz). It is noteworthy that the difference in heat sink weight is related to semiconductor losses and all semiconductors thermal exchange surface area. The solution with Si MOSFET comprises 108 transistors with 20.70 mm x 15.87

mm each, while the solution with GaN HEMT transistors has 144 components, each with 9 mm x 7.6 mm. Finally, the Si MOSFET solution is only compliant for 30 kHz, which comprises 98.7% efficiency and a gravimetric power density of 8.38 kW/kg. Si and SiC MOSFET solutions present many semiconductors with the TO - 247 package, which indicates a more incredible difficulty in integrating these components and reducing parasitic inductances that can considerably increase switching losses in these components in a real inverter.

The solution represented by the green curve, a 4-level Quasi FC, is the black curve FC topology. Both have the same number of transistors and losses (considering phase-shifted triangular carriers - PS PWM). However, the floating capacitor's value is reduced to allow only the series connection of GaN transistors (synchronize their commutations) but no longer provides the same number of voltage levels at the inverter output. The Quasi FC inverter operates as a FB inverter (same number of output voltage levels). However, in this case, with three legs per phase, it enables four levels on the inverter output voltage. This reduction in the number of output levels (compared to the FC possibilities) strongly impacts the inductors weight of paralleled legs, which goes from 6.17 kg (FC) to 20.72 kg (Quasi FC) at 10 kHz and from 1.5 kg (FC) to 3.5 kg (Quasi FC) at 40 kHz. The 7 – level FC solution still has a lower overall weight, even considering the floating capacitor weight (6.48 kg at 10 kHz and 1.6 kg at 40 kHz), which is non-existent in Quasi FC. The most significant difference is noticed in the inverter efficiency. As the Quasi FC topology has higher output inductors, higher losses are present (110 W at 40 kHz) than the inductors of the FC topology (30 W to 40 kHz) decreases inverter efficiency. The Quasi FC topology is compliant with design criteria for switching frequencies superior to 30 kHz.

2.10.1 Inverter weight and loss distribution

To better understand weight and loss distribution on the elements that compose inverters solutions, the results of the 2 - level with 1200 V SiC and 7 – level FC with 650 V GaN HEMT topologies are detailed in this section. The impact of increasing the switching frequency on each element is also verified. The impact of multilevel topology on each filter, compared to a traditional 2-level topology, is another point covered in this section.

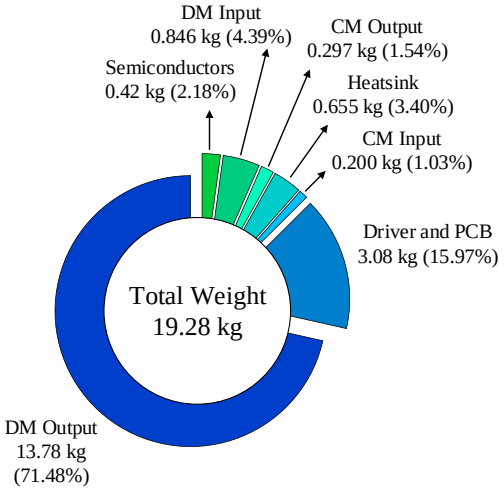
The pie charts in Figure 119 show the overall distribution of weight and losses on 2 - level with 1200 V SiC (blue curve in Figure 117) for 10 kHz and 40 kHz. Increasing the switching frequency in this inverter allows a reduction of the overall weight of different components, despite the increase in semiconductor losses and cooling system weight, as summarized below:

- Decrease of 60% on global weight;
- Decrease of 75% on DM output filter weight. DM output filter represents 45.4% of global weight at 40 kHz and 71.5% at 10 kHz;
- Decrease of 56% on PCB weight. PCB represents 17% of global weight at 40kHz and 16% at 10 kHz;
- Increase of 37% on heat sink weight and 67% on semiconductors losses. Heat sink represents 11% of global weight at 40 kHz and 3.4% at 10 kHz;

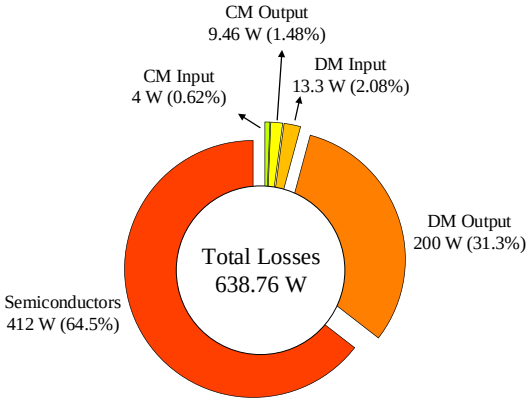
- Increase of 32% on CM output filter weight. CM output filter represents 5.1% of global weight at 40 kHz and 1.5% at 10 kHz;

- Filter losses represent 14.2% of global losses at 40 kHz and 35.5% at 10kHz.

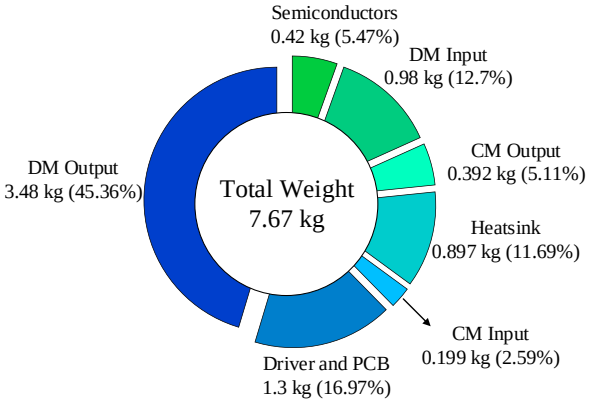
DM output filter has been designed for THD_i = 7% and a maximum overvoltage level at motor terminals of 750 V. At 10 kHz, THD_i is the criterion that designs the filter. In contrast, for higher frequencies (in this case, 40 kHz), this is no longer the dominant criterion in selecting the optimal solution but the trade-off between losses and weight of the various solutions calculated during the filter optimization.



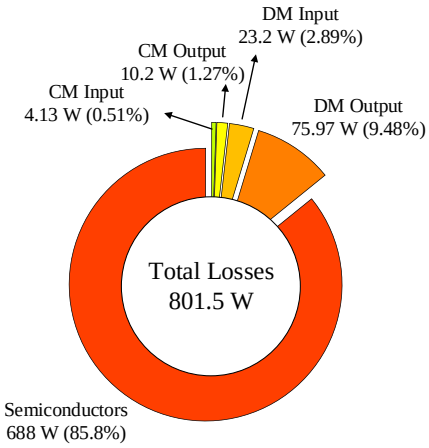
(a) Weight distribution for 10kHz



(b) Losses distribution for 10kHz



(c) Weight distribution for 40kHz

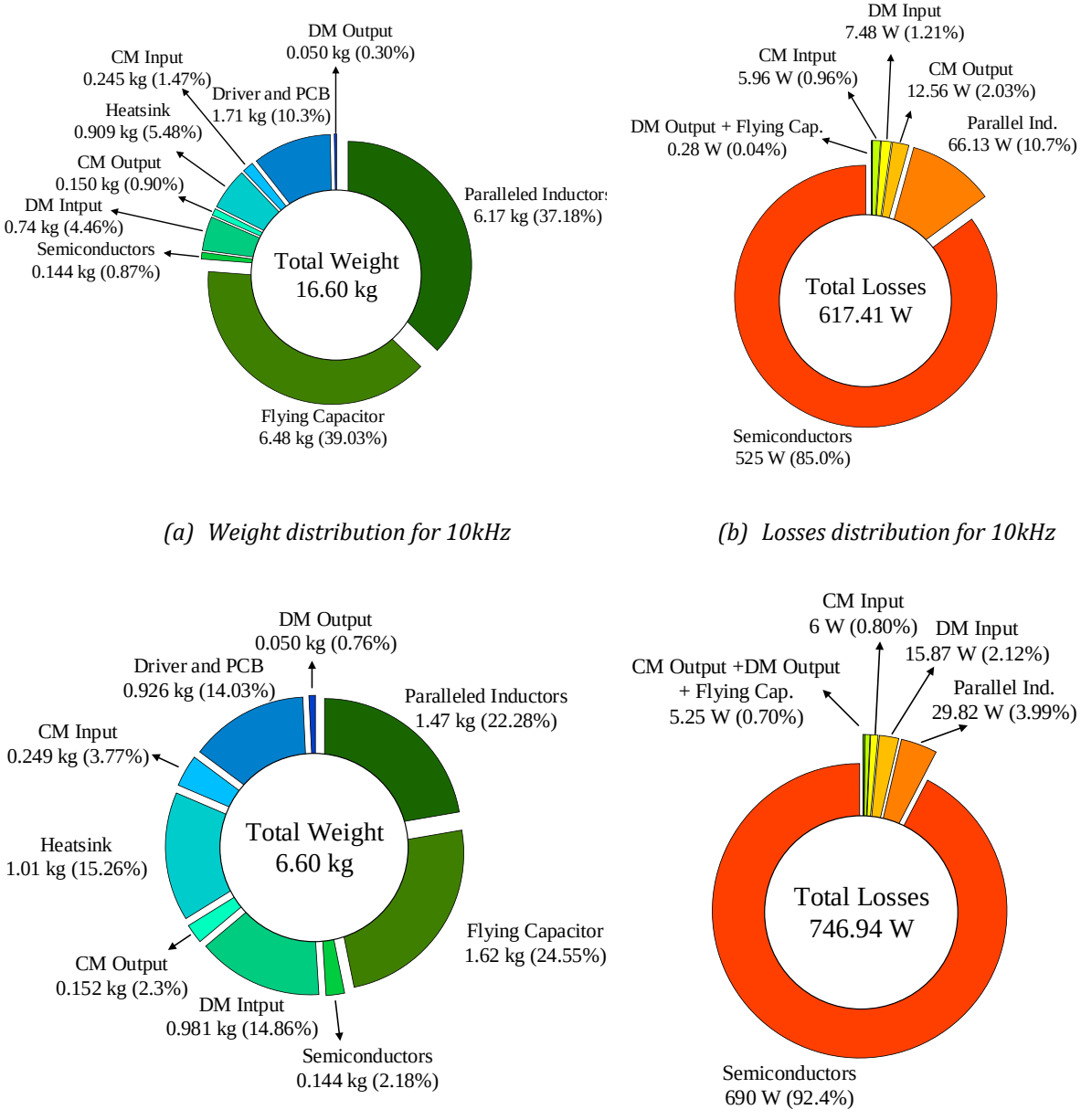


(d) Losses distribution for 40kHz

Figure 119 - Weight and Loss distribution for 1200V SiC 2-level topology and two switching frequencies:10kHz and 40kHz. Nominal power = 70kVA, V_{bus} = 540V and DPWM1.

On the other hand, Figure 120 shows the weight and losses overall distribution of the 7 – level FC with 650 V GaN HEMT (black curve in Figure 117) for 10 kHz and 40 kHz, whose impact is shown below:

- Decrease of 60% on global weight (as 2-level topology);
- Decrease of 75.5% on paralleled inductors + flying capacitors weight. Paralleled inductors and flying capacitors represent 46.8% of global weight at 40 kHz and 76.18% at 10 kHz;
- Decrease of 46.2% on PCB weight. PCB represents 14% of global weight at 40 kHz and 10% at 10 kHz;
- Increase of 10% on Heat sink weight and 31.4% on semiconductors losses. Heat sink represents 15.26% of global weight at 40 kHz and 5.5% at 10 kHz;
- Increase of 1.3% on CM output filter weight. CM output filter represents 2.3% of global weight at 40 kHz and 0.9% at 10 kHz;
- Filter losses represent 7.6% of global losses for 40 kHz and 15% for 10 kHz.



(a) Weight distribution for 10kHz

(b) Losses distribution for 10kHz

(c) Weight distribution for 40kHz

(d) Losses distribution for 40kHz

Figure 120 - Weight and Loss distribution for FC-3Lvl-3Par GaN 650V topology and two switching frequencies:10kHz and 40kHz. Nominal power = 70 kVA, V_{bus} = 540 V and DPWM1

By comparing the 2 - level topology with the SiC module and the 7-level FC with GaN at a switching frequency of 40 kHz, the multilevel topology is 13% (almost 1.2 kg) lighter than the 2 - level topology. This gain is fractionated into 150 g in the cooling system, 400 g in PCB, and 380 g in the DM output filter (in the multilevel topology, the interleaved inductors and floating capacitors were considered) 190 g in the CM filters. This result can be translated into fuel saving. In 2007, the fuel cost per mass unit, in the lifetime of an aircraft, was about 1500 €/kg to 2000 €/kg [74], which means that the 7 – level FC with GaN could represent again between 1800 € and 2400 €, in fuel savings, compared to the 2 - level topology.

The work described in [6] shows that for an aircraft system with a power of 45 kW, an optimized three-phase bidirectional inverter with the EMC filters included has a power density of 5.3 kW/kg and 99.2% of efficiency. The study presented in this chapter shows that for a 70 kVA system, it is possible to obtain an inverter with a weight-optimized filter and heat sink (forced-air) with a gravimetric power density and efficiency superior to 10 kW/kg and 98.5%.

2.10.2 Impact of reducing the number of GaN HEMT on the 7 – level FC topology and junction temperature.

The 7 – level FC with GaN comprises 144 GaN HEMTs, with nine legs, 16 transistors per leg, and four parallel transistors per switch. Reliability is not addressed in this thesis, as well as semiconductors price. An additional study was carried out to verify the impact of reducing from 4 to 3 paralleled transistors, totalizing 108 transistors for the same topology. Then, only inverter losses and cooling system weight have a direct impact on this changeset. The comparison of these two solutions is presented by considering different junction temperatures.

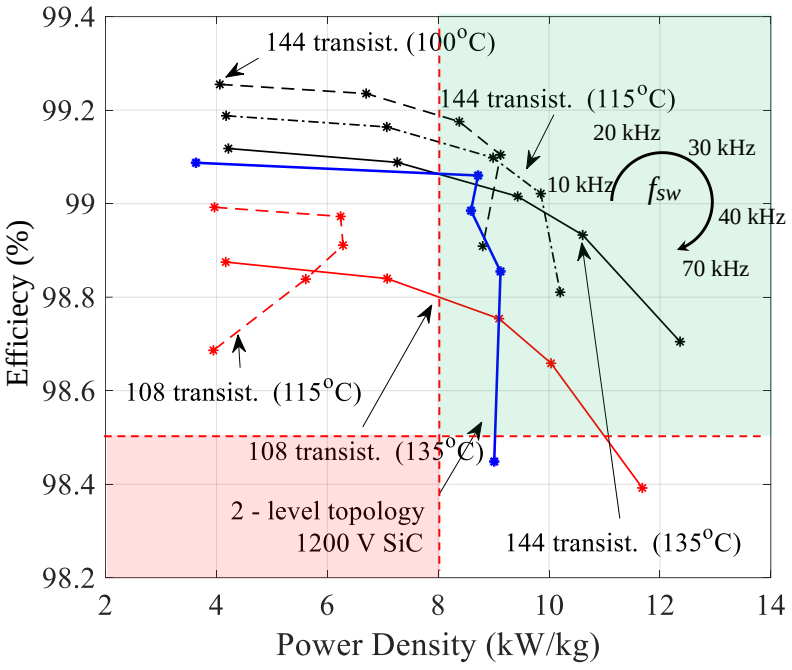


Figure 121 - Impact of the number of paralleled GaN HEMTs on efficiency and weight of the 7 – level FC topology for different junction temperatures for nominal converter operation and DPWM1.

The reduction of junction temperature substantially impacts cooling systems due to the high ambient temperature imposed by aeronautical constraints (70 ºC). Considering a junction temperature of 115 ºC, finding one solution that guarantees minimum gravimetric power density with 3 GaN HEMTs in parallel is impossible. The increase of junction temperature from 100 ºC to 135 ºC for the topology with 3 GaN HEMTs in parallel represents a reduction of 42% (1850 kg to 1.07 kg) on cooling system weight at 40 kHz while efficiency goes from 99.1% to 98.9%. Considering solutions with 4 and 3 GaN HEMTs in parallel for 135 ºC, the cooling system weight difference is 400 g (an increase of 41%) at 40

kHz and 630 g (an increase of 46%) at 70 kHz. The impact on power density is not that expressive. On the other hand, there is a considerable impact on semiconductor losses, 826 W and 634 W, representing an increase of 30.3% on semiconductors losses at 30 kHz. It is leading to reduce efficiency from 99.05% to 98.75%. Therefore, the topology with 144 GaN HEMTs seems to be still more interesting than the one with 108 transistors regarding the efficiency point of view.

2.10.3 Impact of using the recent 650 V SiC devices: C3M0015065D and UF3SC065007K4S.

The 650 V SiC devices C3M0015065D (15 mΩ) and UF3SC065007K4S (6.7 mΩ) were released after January 2019, then, after the study was performed in the previous sections to select an inverter topology and semiconductor technology. In this study, the topology with 144 GaN HEMTs was selected to be built. Nevertheless, Figure 122 shows the impact of using these devices regarding efficiency and power density for the same inverter topology of 7-level FC used for the 650 V device. In C3M0015065D, two devices in parallel per switch are necessary to guarantee minimum $R_{DS\text{-}on}$ presented in Section 2.3.1, while for UF3SC065007K4S, only one is needed. Therefore, 72 C3M0015065D and 36 UF3SC065007K4S are necessary for the hole converter.

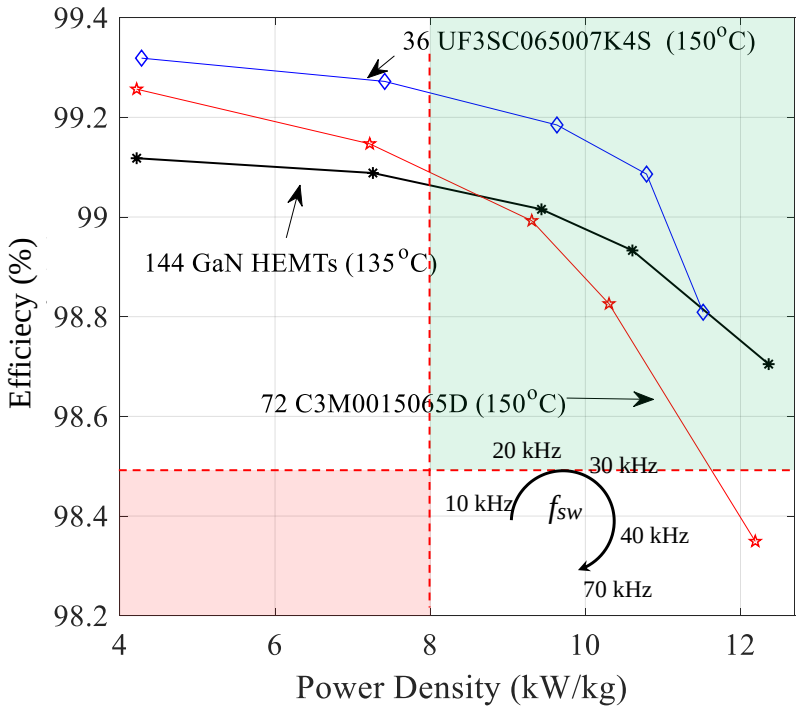


Figure 122 - Impact of the number of UF3SC065007K4S and C3M0015065D on efficiency and weight of the 7-level FC topology for nominal converter operation and DPWM1.

GaN HEMTs seem to be interesting higher than 70 kHz since the tendency shows that they will reach a higher power density than the other. From 10 kHz until 40 kHz, it seems that all solutions have a nearby power density. However, the solution with only one per switch seems more interesting until

40 kHz, with efficiency higher than the other two. The solution with C3M0015065D is more efficient than the solution with GaN HEMTs until ≈ 27 kHz. At 30 kHz, the solution with UF3SC065007K4S has 515 W of semiconductor losses, while the solution with GaN and C3M0015065D has 634 W and 650 W (20.7% higher than UF3SC065007K4S), respectively.

Thus, it seems that the use of the new UF3SC065007K4S is promising since it reduces by four times the number of semiconductors, no need for paralleled devices, which increases inverter reliability and with efficiency superior to 99% (hole converter) until 40 kHz.

2.11 Chapter Conclusions

This chapter has presented different design blocks to evaluate the impact of multilevel inverter topologies and semiconductor technologies on the weight and overall performance of a 70 kVA inverter that meets the future's more electric aircraft requirements. WBG semiconductors are the key to increase the efficiency of power inverters to levels above 99%. A traditional inverter with 1200 V IGBT (latest generation) at 10 kHz has reached 97.8%, while 99.4% was achieved with a 1200 V SiC module (inverter without filters).

Multilevel topologies directly impact increasing inverter power density from 3.63 kW/kg to 4.21 kW/kg at 10 kHz for 2 - level and 7-level topologies, respectively. By passing to 70 kHz, this increase is even higher. It passes from 9 kW/kg to 12.36 kW/kg, showing that if the most important criteria are the power density, there is a considerable gain with the use of multilevel topologies, especially with the increase of switching frequency.

Switching frequency directly impacts the inverters' passive elements, such as the DM output filter inductors, the FC topology capacitors, and the inductors to parallel inverters legs. Considering only the weight of these devices, a reduction from 13.78 kg to 3.48 kg has been seen with the increase from 10 kHz to 40 kHz for the 2 - level 1200 V SiC module (only DM output filter inductors to respect Overvoltage and THD_i limits).

For the 7-level FC topology, the weight drops from 12.7 kg to 3.1 kg (flying capacitors and inductors to parallel inverters legs). It suggests that the increase of inverter power density is intrinsically related to power inverter switching frequency, even if an individual weight increase is observed for a specific filter. For example, 2 - level topology with 1200 V SiC MOSFET CM output filter weight increase from 0.297 kg at 10 kHz to 0.524 kg at 30 kHz.

The higher power density presented by the 7-level FC topology shown in Figure 123, compared to the traditional 2-level inverter, justified the choice of this topology to be designed.

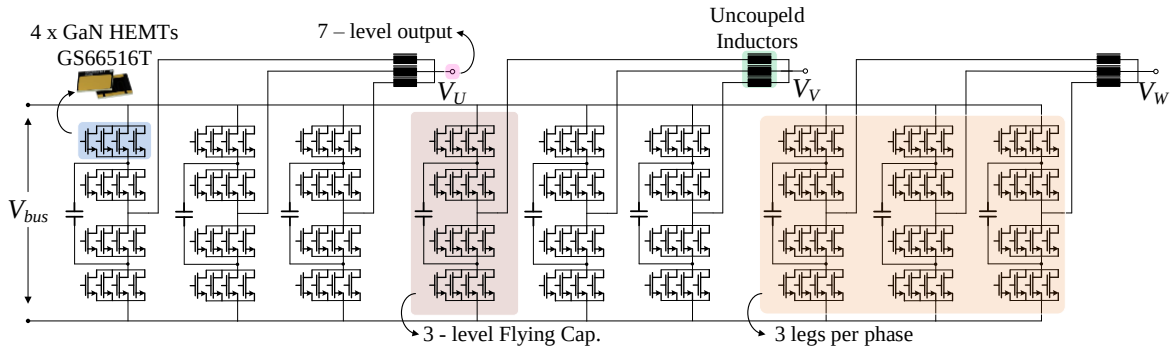


Figure 123 - Selected 7-level Flying Capacitor topology to be designed in this thesis.

Beyond the gain of power density, by using the multilevel inverter, we highlight the challenges related to:

- The parallel of GaN transistors;
- Lack of work related to a multilevel GaN cell with this number of parallel transistors;
- Problems of integration WBG transistors in a power inverter;
- The degrees of freedom in control due to the number of legs in parallel, which can allow a reconfiguration to operate in degraded mode;
- The operation as a Quasi FC inverter (removing a large part of the inverter floating capacitors).

Another challenge is evaluating EMI CE for multilevel converters considering the coupling between inverter input and output CM currents. Since the multilevel converter is composed of various switching cells, there is the possibility of investigating CM filters split among these switching cells to reduce CM's entire filter weight. Rather than using only one filter in the input and another in the output, CM capacitors are used remarkably close to the switching cell can guarantee a CM current circulation loop in the cell itself, reducing the current portion at the converter input.

From this topology, three research axes are identified and will be addressed in the following chapters, aiming to:

- Improve the EMI model used in Chapter 2 for multilevel topologies and determine the lightest repartition of CM filter on the 7-level FC (Axis 1);

- Evaluate different PWM techniques in order to increase inverter overall power density and efficiency (Axis 2);

These two axes are developed in Chapter 3 and Chapter 4 to determine the final inverter components.

- The third axis is addressed in Chapter 5, aiming to investigate the final converter's realization regarding the integration/parallelism of GaN HEMTs, filters, and the converter's performance against defined criteria.

CHAPTER 3

EMI modeling of multilevel power converters

THIS chapter presents an EMI model for multilevel power converters, and the optimal disposition of CM filters between the inverter input and output for the inverter topology is selected in Chapter 2.

Summary

3.1 Common-Mode Voltage Source Modeling for Multilevel Inverter Topologies

The EMI model presented in Section 2.9.5.4 for the multilevel converter has considered the uncoupling between input and output CM currents. In general, only inverter output phase voltages are considered for the equivalent voltage source of multilevel topologies. Therefore, the stray capacitances from the semiconductor to the heat sink that are not connected to inverters output are neglected. This consideration is verified in [230] for three-level and five-level T-Type converters and [231] for a five-level modular composited converter. On the other hand, [224] considers one voltage source connected to the respective parasitic capacitance for each switching cell of a 7-level cascade Half-Bridge (H4) in a PV (Photovoltaic) system connected to the grid. In this case, three H4 are connected in series, and three parasitic capacitances are considered to form the inverter CM equivalent circuit. This paper considers a coupling between the input and output circuit, but it is limited to this inverter topology, and it is developed for a single-phase application. No further explanation is performed for the three-phase application.

MMC topology CM voltage source is addressed in [221], [222], [232]. In [232], the CM voltage source is calculated considering the path formed only by the parasitic capacitances connected on inverter output connections. The parasitic capacitances not connected to the output are considered in the models presented in [221], [222], as submitted to different *dV/dt* due to each switching cell. However, the equivalent circuit proposed in [222] has only one voltage source, as proposed for a two-level topology presented in Figure 107. The parasitics capacitances of the semiconductors are split between the voltage source input and output connections. Nevertheless, no experimental or simulation validation was performed. In [221], each switching cell's parasitics capacitances are considered in parallel, so it is assumed that all capacitances will be connected in parallel in inverter output. No equations or validation are presented to define the equivalent model.

This section is dedicated to present mathematical modeling of an equivalent CM voltage source that can be generalized to any parallel or series multilevel inverter topologies. This model should provide the coupling between inverter input, and output currents, respecting the current paths of the parasitic capacitances that are not connected to the inverter output. In this case, a more precise design of input and output EMI filters can be performed.

The complete setup of DO-160 standards for Conducted emissions is considered, as shown in Figure 124. In this case, all blocks will be addressed separately, and a CM equivalent circuit will be mathematically described from the DM circuit. This methodology is formalized in [226] for a two-level converter.

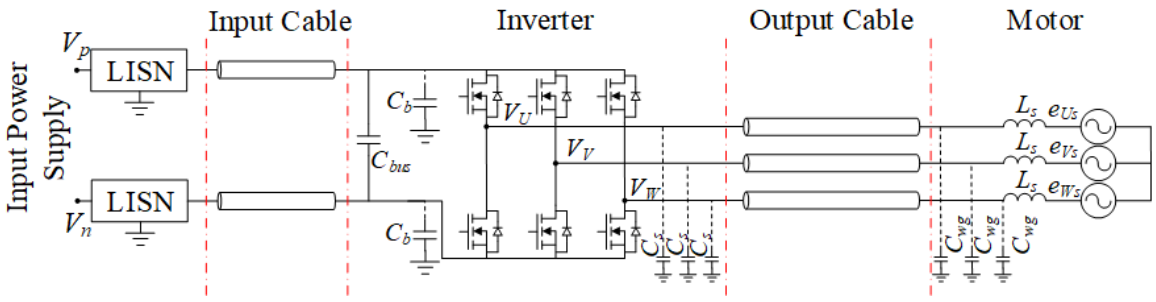


Figure 124 - More Electric Aircraft power drive system architecture.

A specific point does not define the CM modeling proposed by [215] (e.g., ground plane), but to a reference point *P* is completely arbitrary, facilitating the construction of CM models of systems formed by different components. This modeling approach comprises two essential steps: generate CM equivalent circuits for each system component and then connect these equivalent circuits to the entire system's CM model.

The first step to model each component CM equivalent circuit is to identify the parasitic couplings that provide CM current path and add these paths to the DM model, forming a mixed-mode model. Then, line voltages for this mixed-mode model are defined according to the arbitrary point *P*. Thus, line voltage equations are averaged to define CM equivalent circuit. It is worth pointing out that [215] did not consider semiconductors stray capacitances, either input and output cables. Therefore, this chapter will apply the methodology in a more complex problem to propose a simplified CM voltage source model applied to any inverter topology for EMI filter predictive design.

3.2 Common-mode and Differential Mode definitions

Circuit operation can be briefly described by two modes: differential-mode and common-mode. Differential-mode is the desired operation of the circuit that is commonly represented in circuitry schematics. Common-mode is considered an unwanted operation mode resulting from environmental interference, asymmetric design, or parasitic couplings [226]. Common-mode and differential-mode currents are defined according to the schematics presented in Figure 125, for a two-wire circuit as [233]:

$$i_{CM} \triangleq i_1 + i_2$$
$$i_{DM} \triangleq \frac{i_1 - i_2}{2} \text{ (two wire)} \tag{3.1}$$

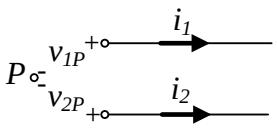


Figure 125 – Common-Mode and Differential-Mode definitions.

Common-mode and differential-mode voltages are defined referent to an arbitrary reference point *P* as:

$$v_{CM} \triangleq \frac{v_{1P} + v_{2P}}{2},$$
$$v_{DM} \triangleq v_{1P} - v_{2P}. \tag{3.2}$$

If v_{1P} and v_{2P} are balanced in reference to *P*, generally connected to bus DC link midpoint, v_{CM} is zero (i.e., $v_{1P} = V_{dc}/2$ and $v_{2P} = -V_{dc}/2$).

The definitions presented above are applied only for a pair of lines regarding the differential-mode. By regarding the common-mode definitions, they can be generalized for *K* lines as:

$$i_{CM} \triangleq \sum_{k=1}^{K} i_k,$$
$$v_{CM} \triangleq \frac{1}{K}\sum_{k=1}^{K} v_{kP}. \tag{3.3}$$

It is necessary to point out that the DM model described in Section 2.9.2.2.2 for a three-wire circuit is a particular consideration used to described the overvoltage modeling during the transistor switching time. This definition cannot be applied to EMI modeling since the procedure considers steady-state behavior. The modeling described in this chapter adheres to the CM modeling, the main responsible for EMI conducted emissions as described in Chapter 2.

The averaging equations above are used to determine the CM voltage, and current based on the DM referenced to an arbitrary point *P*. This methodology considers one arbitrary point between each block connection, represented by the red lines in Figure 124. These arbitrary shared points will be used to connect each block's equivalent CM circuit between each other. This methodology will be first applied in a 2-level inverter, and then it will be presented the modeling for a multilevel inverter.

3.3 Common-Mode Modeling Approach for a 2 - level Inverter

The equations and hypotheses described in the previous section are considered to model a 2-level inverter, and each block of the power drive test setup is presented in Figure 124. The ground plane described in the RTCA/DO-160G standard will be considered in an equipotential voltage v_g.

3.3.1 LISN Modeling

The LISN described in Section 2.9.5.3 can be represented by a series impedance $Z_{LISN,S}$ connected to the bus lines (V_p and V_n), and a parallel impedance due to the standard ground plane as

presented in Figure 126 (a). The power supply connected to the bus lines is considered isolated from the ground plane.

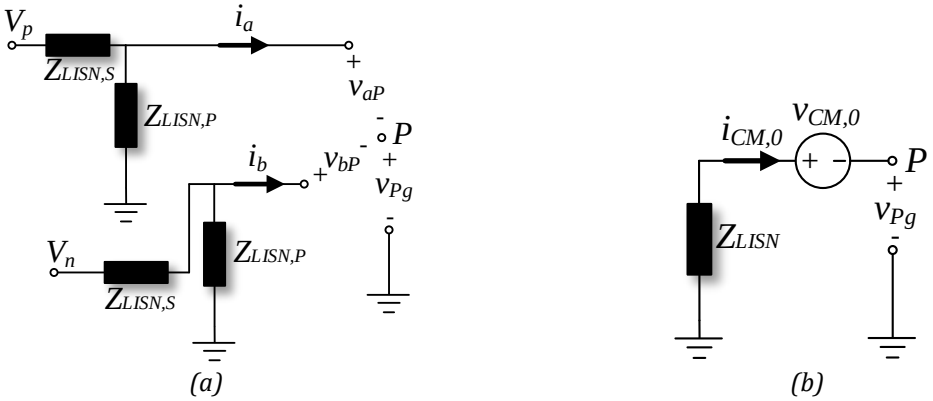


Figure 126 - LISN Modeling: (a) DM and equivalent (b) CM.

Considering Kirchhoff's voltage law (KVL) and assuming that the CM current does not pass through the series impedances $Z_{LISN,S}$, the two circuit loops formed by the ground connection are described as:

$$\begin{aligned} v_{Pg} + v_{aP} &= -i_a.Z_{LISN,P} \\ v_{Pg} + v_{bP} &= -i_b.Z_{LISN,P} \end{aligned} \tag{3.4}$$

Averaging the two equations above gives:

$$v_{Pg} + \frac{(v_{aP} + v_{bP})}{2} = -\left(\frac{i_a + i_b}{2}\right).Z_{LISN,P}. \tag{3.5}$$

Where v_{Pg} is the voltage between the arbitrary point P to the ground plane. Considering the following averaging equations:

$$\begin{aligned} i_{CM,0} &= i_a + i_b, \\ v_{CM,0} &= \frac{v_{aP} + v_{bP}}{2}, \\ Z_{LISN} &= \frac{Z_{LISN,P}}{2}, \end{aligned} \tag{3.6}$$

The equivalent CM circuit or the LISN is described in Figure 126 (b), referred to *P*.

3.3.2 Input Cable Modeling

The two-wire cable equivalent circuit was presented in Section 2.9.5.2 as an equivalent T circuit. In that case, the same CM impedance of the cable will be considered. Cable input left connections in Figure 127 (a) are connected to the LISN.

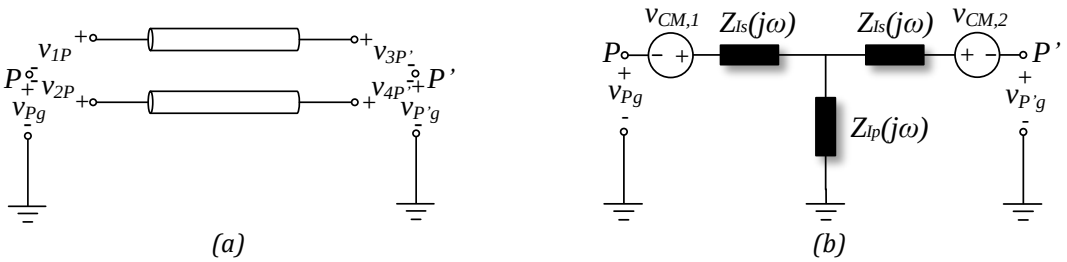


Figure 127 - Input Cable Modeling : (a) DM and equivalent (b) CM.

The same arbitrary point *P* is used to estimate the equivalent voltage source $v_{CM,1}$ between cable connections and *P*, as*:*

$$v_{CM,1} = \frac{v_{1P} + v_{2P}}{2}, \tag{3.7}$$

The right input cable connections are connected to the inverter, then another reference point *P'* is considered to determine $v_{CM,2}$.

$$v_{CM,2} = \frac{v_{3P'} + v_{4P'}}{2}. \tag{3.8}$$

Thus, the equivalent CM circuit for the input cable is presented in Figure 127 (b).

3.3.3 Two-level Inverter Modeling

The inverter is split into two circuits, the input regarding the input cable's connection and the output connected to the three-phase output cable. The circuit is shown in Figure 128 (a) represents the connections to the input cable on the left, with the arbitrary point *P'*, and C_b represents the parasitic capacitances of the inverter bus connections to the ground plane. The right side is the DC link internal inverter connection that will be directly converted to the three-phase output voltage. In this case, another arbitrary point *P''* is considered. No stray inductances of resistances will be considered in the inverter. However, the present method can also be applied if any impedance is considered.

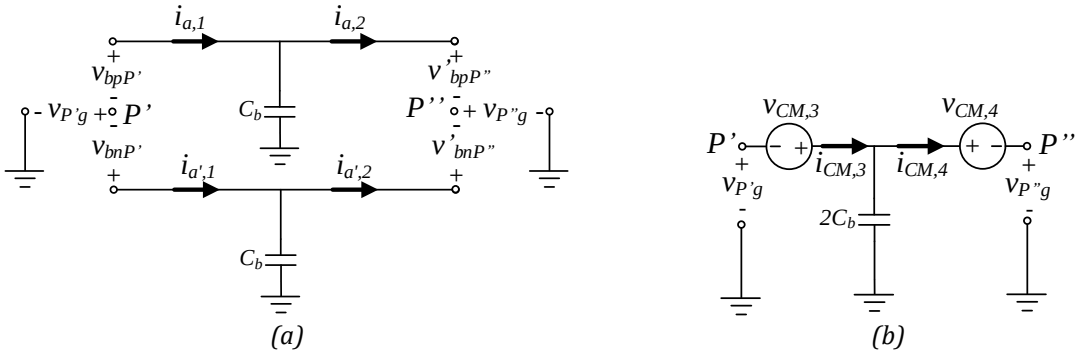


Figure 128 - Inverter input lines Modeling: (a) DM and equivalent (b) CM.

Considering Kirchhoff's voltage law (KVL), on the right side of Figure 128 (a):

$$\begin{aligned} v_{P'g} + v_{bpP'} &= \frac{1}{C_b}\int \left(i_{a,1} - i_{a,2}\right).dt, \\ v_{P'g} + v_{bnP'} &= \frac{1}{C_b}\int \left(i_{a',1} - i_{a',2}\right).dt, \end{aligned} \tag{3.9}$$

Averaging the two equations above gives:

$$v_{P'g} + \frac{\left(v_{bpP'} + v_{bnP'}\right)}{2} = \frac{1}{2.C_b}\int \left(\left(i_{a,1} + i_{a',1}\right) - \left(i_{a,2} + i_{a',2}\right)\right).dt. \tag{3.10}$$

.

Applying the definition of i_{CM} and v_{CM}:

$$\begin{aligned} v_{CM,3} &= \frac{\left(v_{bpP'} + v_{bnP'}\right)}{2}, \\ i_{CM,3} &= i_{a,1} + i_{a',1}. \end{aligned} \tag{3.11}$$

It gives the equivalent CM circuit seen by the input cable and presented in Figure 128 (b). The same procedure applies to the inverter connection (right side of Figure 128 (a)). Therefore, $i_{CM,4}$ and $v_{CM,4}$ are as follows, completing the equivalent CM circuit in Figure 128 (b).

$$\begin{aligned} v_{CM,4} &= \frac{\left(v_{bpP''} + v_{bnP''}\right)}{2}, \\ i_{CM,4} &= -\left(i_{a,2} + i_{a',2}\right). \end{aligned} \tag{3.12}$$

For simplification, it is considered that the heat sink is directly connected to the ground plane, so no ground braid is used. Therefore, C_s represents the capacitance connected to the output of the inverter. In the case of the 2-level inverter, it represents the capacitance from the semiconductor to the ground. In the left, the circuit Figure 129 (a) represents the inverter output connected to semiconductors capacitances referenced to the arbitrary point P''. On the other hand, the right connection in the circuit referred to P''' represents the inverter's connection to the output three-phase cable.

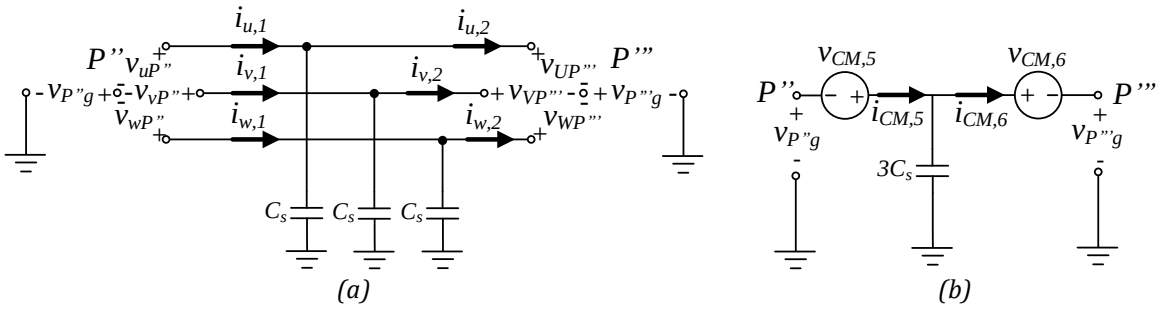


Figure 129 - Inverter output lines Modeling : (a) DM and equivalent (b) CM.

Applying Kirchhoff's voltage law (KVL) on the left side of Figure 128 (a):

$$\begin{aligned} v_{P"g} + v_{uP"} &= \frac{1}{C_s}\int \left(i_{u,1} - i_{u,2}\right).dt, \\ v_{P"g} + v_{vP"} &= \frac{1}{C_s}\int \left(i_{v,1} - i_{v,2}\right).dt, \\ v_{P"g} + v_{wP"} &= \frac{1}{C_s}\int \left(i_{w,1} - i_{w,2}\right).dt. \end{aligned} \tag{3.13}$$

Averaging the three equations above gives:

$$v_{P"g} + \frac{\left(v_{uP"} + v_{vP"} + v_{wP"}\right)}{3} = \frac{1}{3.C_s}\int \left(\left(i_{u,1} + i_{v,1} + i_{w,1}\right) - \left(i_{u,2} + i_{v,2} + i_{w,2}\right)\right).dt, \tag{3.14}$$

Applying the definition of i_{CM} and V_{CM}:

$$\begin{aligned} v_{CM,5} &= \frac{\left(v_{uP"} + v_{vP"} + v_{wP"}\right)}{3}, \\ i_{CM,5} &= i_{u,1} + i_{v,1} + i_{w,1}. \end{aligned} \tag{3.15}$$

It gives the equivalent CM circuit seen by the inverter output and is presented in Figure 129 (b). The same procedure applies to the converter connection (right side of Figure 129 (a)). Therefore, $i_{CM,6}$ and $v_{CM,6}$ are as follows, completing the equivalent CM circuit in Figure 129 (b).

$$\begin{aligned} v_{CM,6} &= \frac{\left(v_{UP"} + v_{VP"} + v_{WP"}\right)}{3}, \\ i_{CM,6} &= -\left(i_{u,2} + i_{v,2} + i_{w,2}\right). \end{aligned} \tag{3.16}$$

3.3.4 Output Cable Modeling

Output cable was also described in Figure 68 as an equivalent T circuit based on transmission line theory. The equivalent circuit of the output three-phase cable is presented in Figure 130 (a).

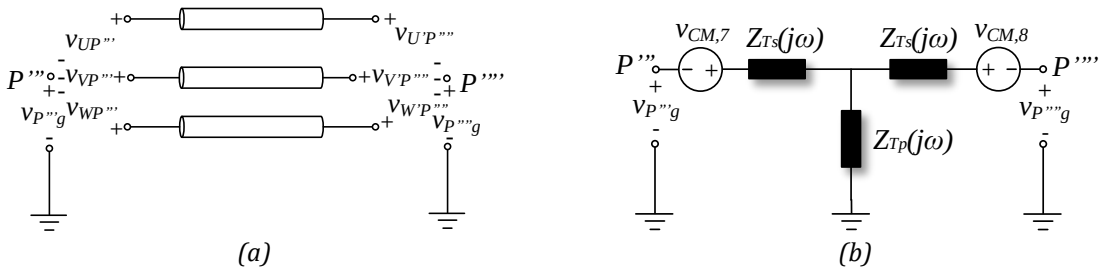


Figure 130 - Output Cable Modeling : (a)DM and equivalent (b)CM.

The same arbitrary point P''' is used to estimate the equivalent voltage source $v_{CM,7}$ between output cable input connections and inverter output, as:

$$v_{CM,7} = \frac{v_{UP'''} + v_{VP'''} + v_{WP'''}}{3}. \tag{3.17}$$

The right connections of output cable are connected to the electric motor, then another reference point P'''' is considered to determine $v_{CM,8}$, as:

$$v_{CM,8} = \frac{v_{UP''''} + v_{VP''''} + v_{WP''''}}{3}. \tag{3.18}$$

The equivalent CM circuit for the output cable is presented in Figure 130 (b).

3.3.5 Motor Modeling

The equivalent circuit of a typical electric motor is presented in Figure 131 (a). It is considered that zero-sequence impedance has a negligible effect on motor CM behavior. Moreover, the motor CM impedances are due to winding impedance (Z_{Ms}) and stator to ground capacitances (C_{wg}). This modeling can incorporate additional parasitics, as leakage paths through the rotor and machine bearings. Nevertheless, according to [226], it can be neglected for simplicity due to its higher impedance than the stator winding to ground coupling. The motor DM model presented in Figure 131 (a) considers winding impedances, phase inductance, and motor electromotive forces (e_{Us}, $e_{Vs,}$ and e_{Ws}).

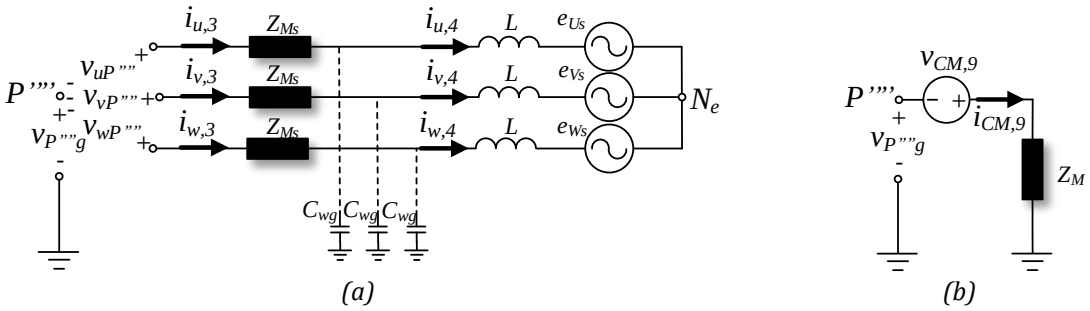


Figure 131 - Inverter output lines Modeling : (a)DM and equivalent (b)CM.

Applying Kirchhoff's voltage law (KVL), on the left side of Figure 129 (a) regarding the arbitrary point P'''' that is also considered for the output cable output, gives:

$$\begin{aligned} v_{P''''g} + v_{uP''''} &= Z_{Ms}.i_{u,3} + \frac{1}{C_{wg}}\int\left(i_{u,3} - i_{u,4}\right).dt, \\ v_{P''''g} + v_{vP''''} &= Z_{Ms}.i_{v,3} + \frac{1}{C_{wg}}\int\left(i_{v,3} - i_{v,4}\right).dt, \\ v_{P''''g} + v_{wP''''} &= Z_{Ms}.i_{w,3} + \frac{1}{C_{wg}}\int\left(i_{w,3} - i_{w,4}\right).dt. \end{aligned} \tag{3.19}$$

Averaging the three equations above gives:

$$\begin{aligned} v_{P''g} + \frac{\left(v_{uP''''} + v_{vP''''} + v_{wP''''}\right)}{3} &= \frac{Z_{Ms}}{3}.\left(i_{u,3} + i_{v,3} + i_{w,3}\right) + ... \\ ... + \frac{1}{3.C_{wg}}\int\left(\left(i_{u,3} + i_{v,3} + i_{w,3}\right) - \left(i_{u,4} + i_{v,4} + i_{w,4}\right)\right).dt, \end{aligned} \tag{3.20}$$

Moreover, applying the definition of i_{CM} and V_{CM}:

$$\begin{aligned} v_{CM,9} &= \frac{\left(v_{uP''''} + v_{vP''''} + v_{wP''''}\right)}{3}, \\ i_{CM,9} &= i_{u,3} + i_{v,3} + i_{w,3}. \end{aligned} \tag{3.21}$$

Moreover, utilizing Kirchoff's current law in N_e ($i_{u,4} + i_{v,4} + i_{w,4} = 0$), one obtains the motor equivalent circuit presented in Figure 131 (b). Where Z_M is motor CM impedance, given by:

$$Z_M = \frac{Z_{Ms} + Z_{C_{wg}}}{3}. \tag{3.22}$$

3.3.6 Common-Mode equivalent circuit

The second part of this modeling approach connects the CM equivalent circuits developed in sections above to form the entire CM system. This connection is made by selecting the shared reference points P for the components to be connected, leading to the power drive system equivalent circuit in Figure 132.

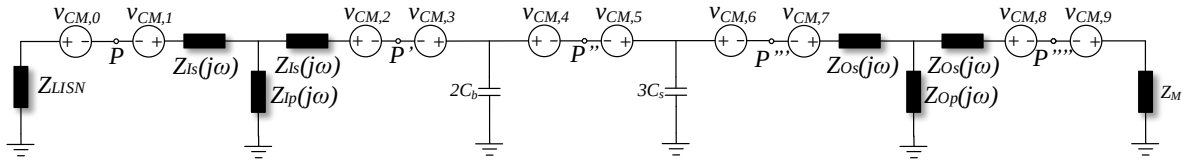


Figure 132 - Power drive system CM complete model.

Assuming that the connection point's voltage is the same for the adjacent systems (e.g., the positive connection between the input cable and the LISN), the voltage between these points is zero. Another hypothesis can also be applied, considering that the switching of the semiconductors determines the source of noise in the system, then the voltage sources between the passive elements that compose the system are equal to zero. Leading to the following simplifications:

$$\begin{aligned} V_{CM,0} + V_{CM,1} = 0 \text{ or } V_{CM,0} = V_{CM,1} = 0 \\ V_{CM,2} + V_{CM,3} = 0 \text{ or } V_{CM,2} = V_{CM,3} = 0 \\ V_{CM,6} + V_{CM,7} = 0 \text{ or } V_{CM,6} = V_{CM,7} = 0 \\ V_{CM,8} + V_{CM,9} = 0 \text{ or } V_{CM,8} = V_{CM,9} = 0 \end{aligned} \tag{3.23}$$

CM voltage sources $V_{CM,4}$ and $V_{CM,5}$ share the same arbitrary point P'', but inverter input and output are not directly connected. Therefore, the equivalent circuit for the power drive system of Figure 124 is presented in Figure 133, where $V_{CM,4} = v_{CM,DC}$ and $V_{CM,5} = v_{CM,AC}$. Inverter input impedance modeled as C_b is represented by the impedance $Z_{inv\text{-}In}$. The impedance $Z_{Inv\text{-}Out}$ represents the semiconductors parasitic capacitances to ground C_s. The $i_{cm\text{-}in}$ and $i_{cm\text{-}Out}$ represent the input and output current that should be measured to respect the RTCA/DO-160G CE limits presented in Figure 101 (a) and Figure 101 (b).

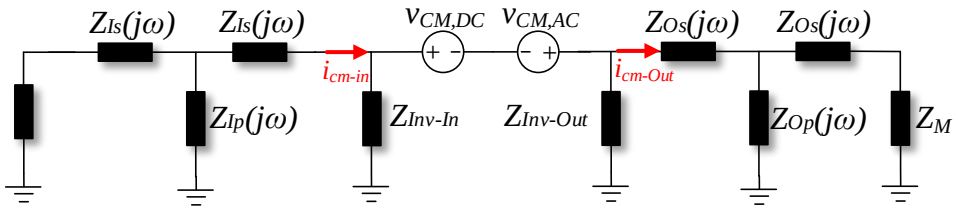


Figure 133 - Power drive system CM equivalent model.

Assuming that inverter input impedances are balanced, the following simplification is valid:

$$v_{CM,DC} = \frac{\left(v_{bpP"} + v_{bnP"}\right)}{2} = \frac{v_{dc}}{2}, \tag{3.24}$$

where v_{dc} is the DC Link voltage. Therefore, if P'' is selected to be the midpoint of the DC Link voltage, then:

$$v_{CM} = v_{CM,AC} + v_{CM,DC} = \left(\frac{\left(v_u + v_v + v_w\right)}{3} - \frac{v_{dc}}{2}\right) + \left(\frac{v_{dc}}{2} - \frac{v_{dc}}{2}\right). \tag{3.25}$$

Where v_u,v_v, and v_w are inverter output voltages referred to as DC-Link negative rail of the inverter input.

The equivalent model presented in Figure 133 is essentially the same in Figure 107, except for the ground braid connection and filters. The main advantage of reasoning in arbitrary voltage potential between different systems is that, in the case of many power converters (multiple sources) composing the system (e.g., one microgrid), it is relatively simple to determine the equivalent CM circuit, as exemplified in [226]. The following section presents the experimental verification for this model for a 2-level inverter in a RTCA/DO-160G standard setup.

3.3.7 Experimental Verification

The equivalent circuit to determine EMI Conducted Emissions presented in Figure 133 was verified experimentally on a 15 kW power drive system presented in Figure 134, inside of a Faraday cage. This power drive system is composed of a VCS (Vapor Cycle System) PSMS motor used on the Airbus A380, with a nominal speed of 9000 tr/min and a couple of 10 N. m. This motor is electrically insulated coupled with a generator.

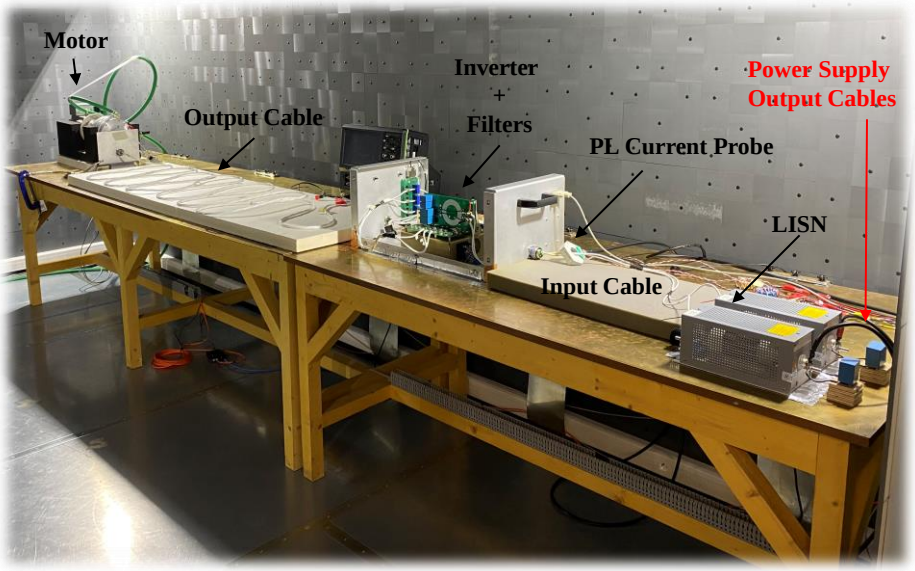


Figure 134 - Test setup used to validate a 15 kW power drive system for the 2-level CM equivalent circuit.

A 2-level inverter was used to control the motor, composed of a 1200 V/50 A SiC Module (CREE CCS050M12CM2), with a C_{bus} of 150 µF and an input voltage of 540 V (power supply externally connected). The 1-meter input cable (AWG 8 - EN 2267-008A090P) connects the LISNs (ESH3-Z6) to the inverter input.

The LISN characteristics are the same as presented in Figure 105. The output cable is formed for three unshielded cables AWG 8 - EN 2267-008A090P (the same as the input cable) and connected inverter output to the motor through Souriau 8D5-21K48ST600L connectors. CM currents ($i_{cm\text{-}in}$ and $i_{cm\text{-}out}$) were measured using the current probe EZ17 M02 (20 Hz to 200 MHz) connected to the EMI Receiver ESR 3-Rohde & Schwarz. The setup disposition and EMI Receiver configuration were performed according to the standard RTCA/DO-160G.

Cable T circuit impedances used in the theoretical model were achieved by simulation according to the procedure presented in Section 2.9.2. Motor (Z_M) and inverter CM ($Z_{Inv\text{-}In}$ and $Z_{Inv\text{-}Out}$) impedances were measured using the Analyser Keysight E4990A. Motor impedance was measured according to the circuit presented in Figure 65 (b). The inverter impedances, on the other hand, consider the setup shown in Figure 135. The heat sink was considered directly connected to the ground plane. The capacitive behavior is observed for input and output until 10 MHz approximately, with equivalent capacitances of 700 pF and 978 pF, respectively. These values were used for the simulation to reinforce the predictive design. Motor impedance was the only part of the model that used the real impedance measurement.

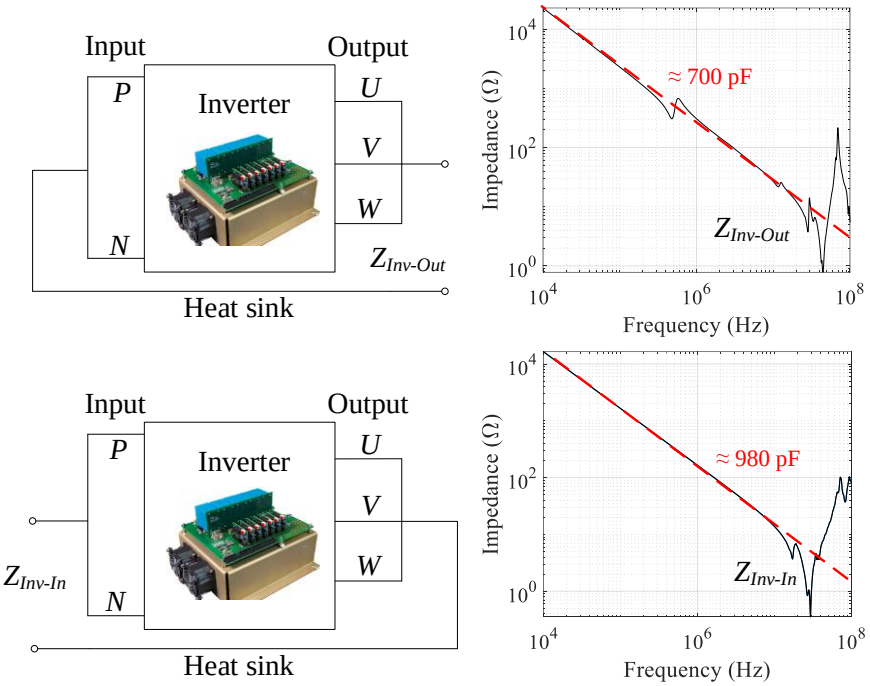


Figure 135 - Inverter input ($Z_{Inv\text{-}In}$) and output ($Z_{Inv\text{-}Out}$) impedance measurement.

The tests were carried out considering different conditions of switching frequency (100 kHz and 20 kHz), output cable length (2 meters and 10 meters), and couple (11 N. m and 0 N. m). Motor speed was fixed at 5000 tr/min for the SPWM technique. The curves presented in Figure 136 shows in black the theoretical estimation (based on Fast Fourier Transformation - FFT) of $i_{cm\text{-}in}$ and $i_{cm\text{-}out}$, and in blue the respective measurements (EMI Receiver) for switching frequency of 100 kHz, 10 m output cable length, and 11 N. m of the couple. The current spectrum behavior is quite similar until 20 MHz, with the simulation slightly higher than the measurement.

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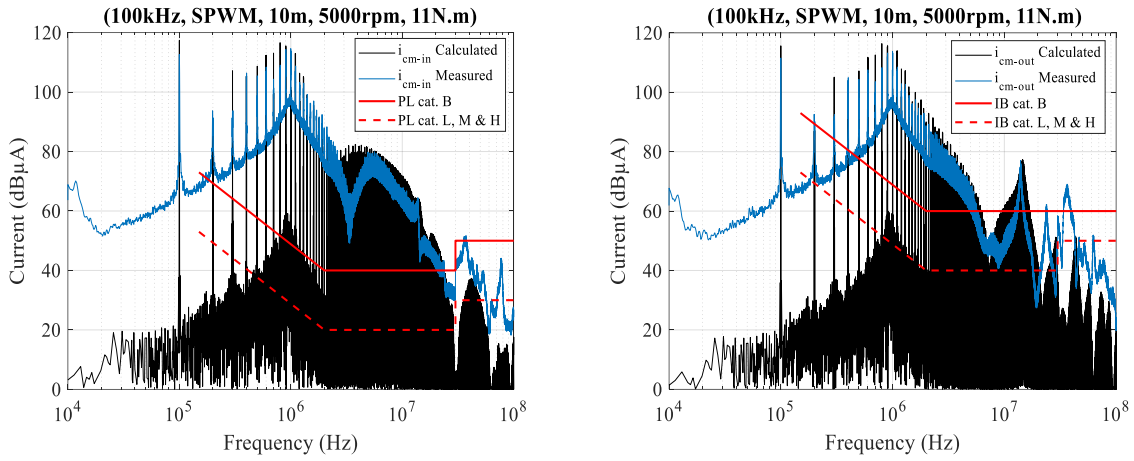


(a) Power Lines – $i_{cm\text{-}in}$ *(b) Interconnecting Bundles – $i_{cm\text{-}out}$*

Figure 136 - Common-mode current measured (blue) and calculated (black) of the 15kW power drive system according to the setup described in DO-160G standard. The inverter's switching frequency was fixed in 100 kHz, SPWM technique, 10 meters of non-shielded cable and motor at 5000 rpm and 11N.

The resonance seen around 1 MHz for both currents is due to motor + cable CM impedances shown on the black curve in Figure 132. The motor + cable CM impedance is presented in black, and the entire power drive system impedance is connected between v_{cm} terminals in red. Due to the uncoupling between input and output considered in Section 2.9.5.4.1, this resonance, characteristic in motor drive systems, did not appear in the input current. This resonance is described in [17] as the harmonic that designs the CM input filter, reinforcing the importance of a coupled model for a more precise filter design.

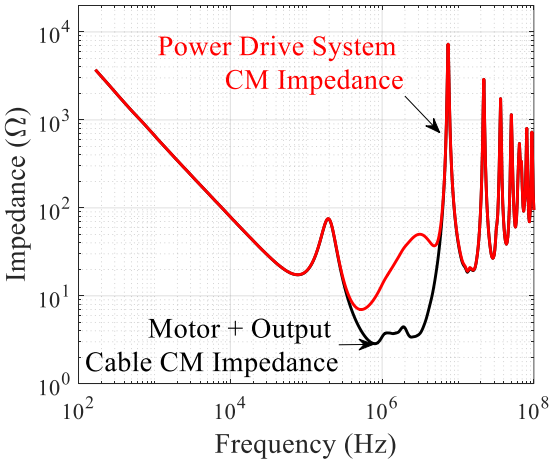


Figure 137 - Power drive CM impedance connected between v_{cm} terminals (red) and motor + cable CM impedances (black).

The differences seen over 20 MHz are due to some elements that were not considered in the model, such as connections, the modeling of inverter input and output impedances as ideal capacitors, and the output voltage of the inverter modeled as a trapezoidal waveform with fix rising and falling times (32 ns). It is shown in [17] that the inverter output voltage behavior is dictated by switching speed (see Figure 138), which depends on the gate to source voltage, gate resistance, and the switching current.

The high the switching speed (the low rising/falling time), the greater the high frequencies components over 1 MHz. Additionally, the power loop inductance with devices output capacitances creates a voltage ringing with resonance frequencies higher than 30 MHz, as illustrated in Figure 139.

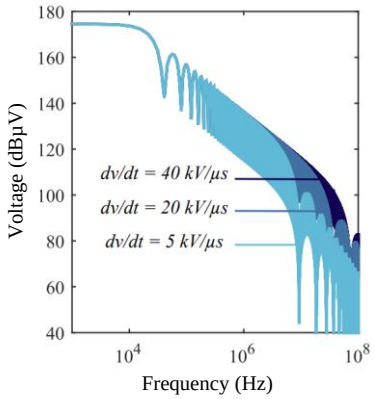


Figure 138 - Impact of switching speed on inverter output voltage spectra[17].

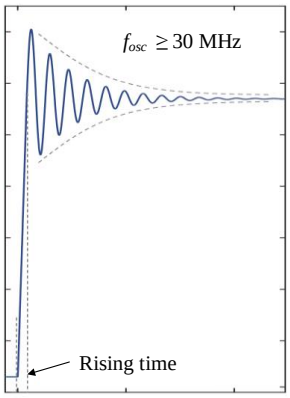
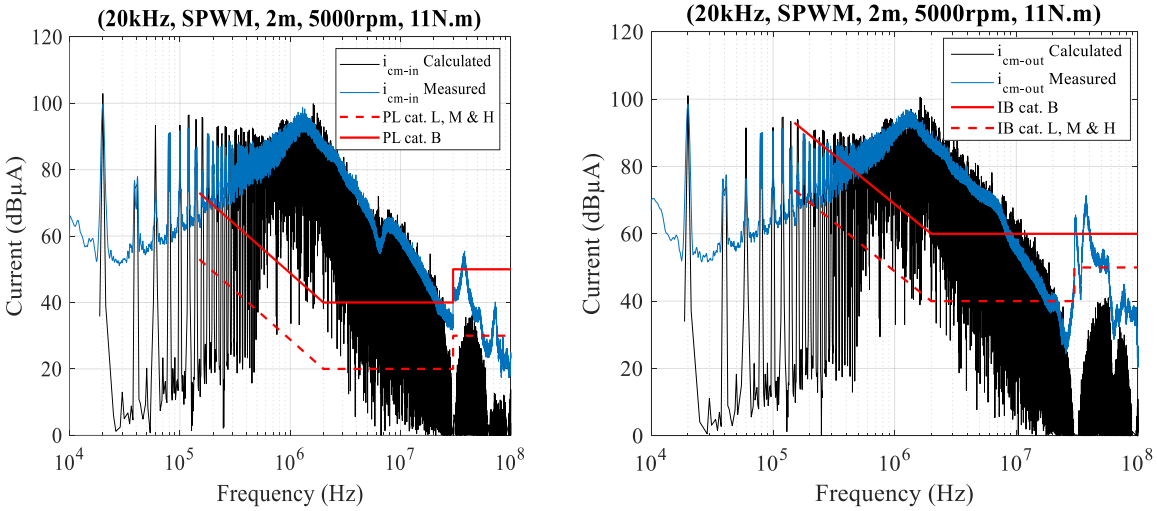


Figure 139 - Voltage ringing present on inverter output voltage[17].

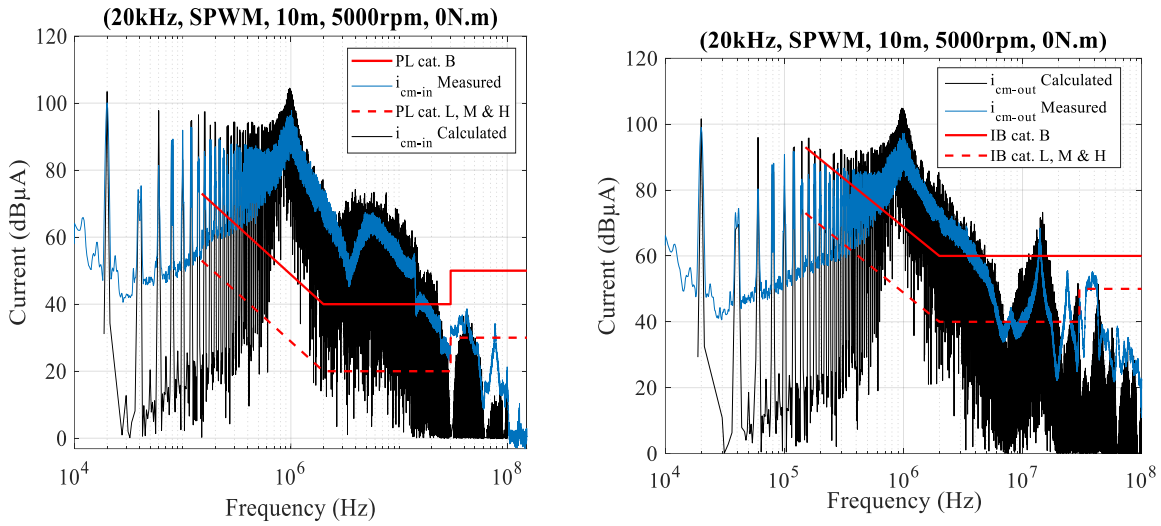
Therefore, the model and measurement differences are also due to the commutation behavior that was not considered. To have a more specific behavior out inverter output voltage, it is necessary to characterize the final inverter with the gate driver for different current levels. However, it makes it difficult for a predictive inverter design.

The curves shown in Figure 140 present the input and output CM currents for the switching frequency of 20 kHz and output cable of 2 meters. The model has an even better current representation than the previous condition until close to 30 MHz.



(a) Power Lines – $i_{cm\text{-}in}$ (b) Interconnecting Bundles – $i_{cm\text{-}out}$

Figure 140 - CM current measured (blue) and calculated (black) of the 15kW power drive system according to the setup described in DO-160G standard. The inverter switching frequency was fixed in 20 kHz, SPWM, 2 - m of non-shielded cable and motor at 5000 rpm and 11N. m



(a) Power Lines –$i_{cm\text{-}in}$ (b) Interconnecting Bundles–$i_{cm\text{-}out}$

Figure 141 - CM current measured (blue) and calculated (black) of the 15kW power drive system according to the setup described in DO-160G standard. The inverter's switching frequency was fixed in 20 kHz, SPWM, 10-m of non-shielded cable and motor at 5000 rpm and 0 N. m.

The curves in Figure 141 were taken for switching frequency of 20 kHz, output cable of 10 meters, and no couple was considered (0 N .m). The differences between the measurement and calculation seem to be even more significant than the previous results, mainly due to the couple's nonexistence. It still presents a closer behavior, mainly due to the motor + cable resonances around 1MHz and 13 MHz for the $i_{cm\text{-}out}$.

The modeling presented in this section and its experimental verification presented a good approximation, especially regarding motor and output cables' resonances. The circuit in Figure 133 can be solved using the transfer function or quadrupole, which was implemented by [17]. The following sections will focus on modeling the equivalent circuit of multilevel inverter topologies based on the theory applied in this section.

3.4 Common-mode Voltage Source for Multilevel Power Converters

3.4.1 Multilevel Parallel

Multilevel Parallel topologies are formed by paralleling converters legs through coupled or uncoupled inductors, as discussed in Section 2.2. The converter shown in Figure 142 will be used to exemplify the modeling of a CM voltage source for a multilevel parallel topology. A traditional 2-level three-phase inverter composes this converter with three legs in parallel through uncoupled inductors L_p. Each phase has a parasitic output capacitance to the reference C_s. This application will be considered the same arbitrary point P'' for the 2-level inverter, placed at $v_{dc}/2$.

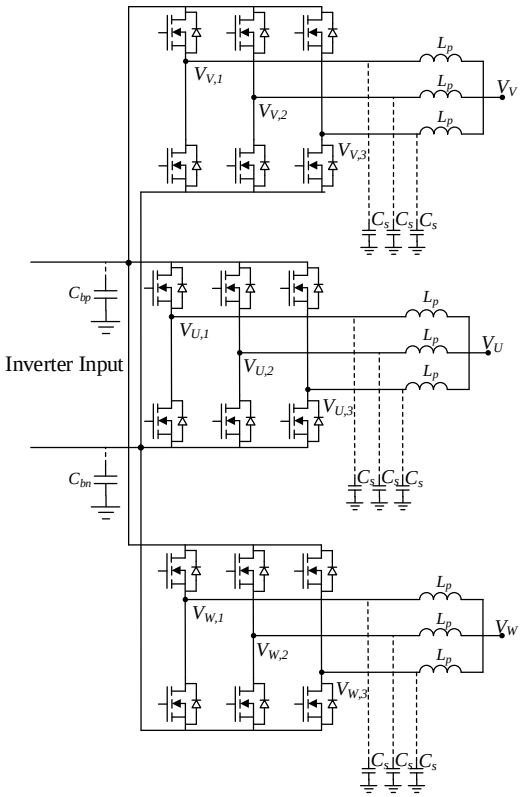


Figure 142 - Multilevel Parallel Inverter with three legs per phase.

Applying the KLV for each loop in this circuit, nine equations will be determined. Averaging these equations will determine $v_{CM,5}$:

$$v_{CM,5} = \frac{1}{9} \cdot \left(\sum_{p=1}^{3} V_{U,pP'''} + \sum_{p=1}^{3} V_{V,pP'''} + \sum_{p=1}^{3} V_{W,pP'''} \right). \tag{3.26}$$

Where p is the paralleled leg number, the equivalent CM circuit of a multilevel parallel converter is presented in Figure 143. The voltage source $v_{CM,6}$ will compensate $v_{CM,7}$ of the output cable as presented in the modeling of the 2-level topology. The output inductor connected to each leg was represented with an ideal inductance L_p. However, the equivalent circuit of the inductor with their parasitics can be used for the same situation.

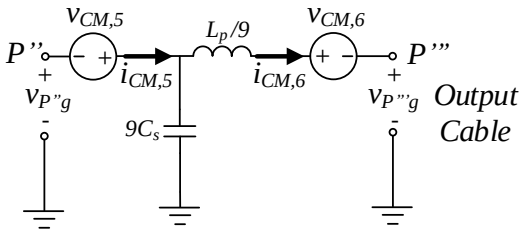


Figure 143 - Multilevel Parallel Inverter CM circuit.

Substituting the equivalent circuit presented in Figure 143 in the power drive system circuit shown in Figure 132 and generalizing N paralleled legs per phase, the equivalent circuit of the multilevel parallel topology in a power drive system is presented in Figure 144, where $v_{CM,AC} = v_{CM,5}$.

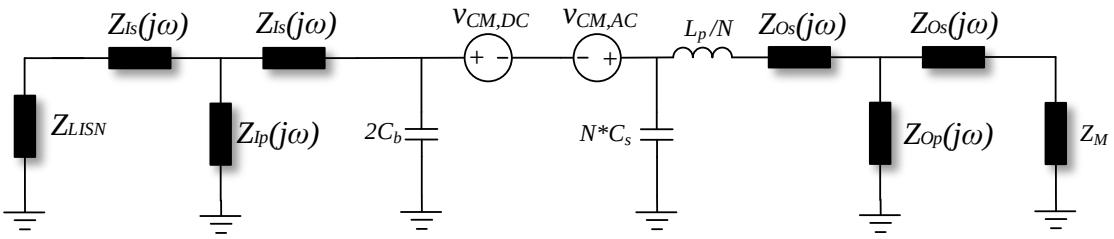


Figure 144 - Multilevel Parallel Inverter Modeling for N legs - Power drive system CM equivalent circuit.

3.4.2 Multilevel Series

The main difference between the 2-level topology, or multilevel parallel topologies considering 2-level paralleled legs and multilevel series topologies, is that the CM current path is not connected to the inverter output connections. These paths are mainly due to semiconductors to heat sink parasitic capacitances. They are in order of some pF, and their high-frequency impedance is higher than cables and motor impedances. Therefore, they are commonly neglected in power drive systems analysis. However, the converter presented in Chapter 1 has many semiconductors (144 devices) that can significantly increase these parasitics and influence EMI filter design. The procedure described in this section aims to determine an equivalent CM circuit for multilevel series topologies. It will be addressed for a FC topology, but it can be equally applied for other multilevel series topologies, as NPC, T-type, etc.

A 5-level FC three-phase inverter is presented in Figure 145. C_s represents the semiconductor to heat sink parasitic capacitance, and $C_{bp} = C_{np}$ is DC-Link parasitic capacitances of the inverter input. This inverter modeling is split into three parts but was developed considering the previous section's methodology.

The first part considers the inverter input connection similar to a 2-level converter presented in Section 3.3.3. For this case, the same *P'* arbitrary point is considered for the input cable and inverter input connection and determines the voltage source $v_{CM,In}$ presented in Figure 146. The second part considers the arbitrary point *P''* to model the CM current path for the parasitic capacitances connected to the inverter output. The modeling of these current paths is similar to the 2-level inverter and multilevel parallel. The equivalent CM voltage source is defined by $v_{CM,Out}$ as the average sum of each leg's output voltage. The output C_s define the output equivalent capacitance in parallel.

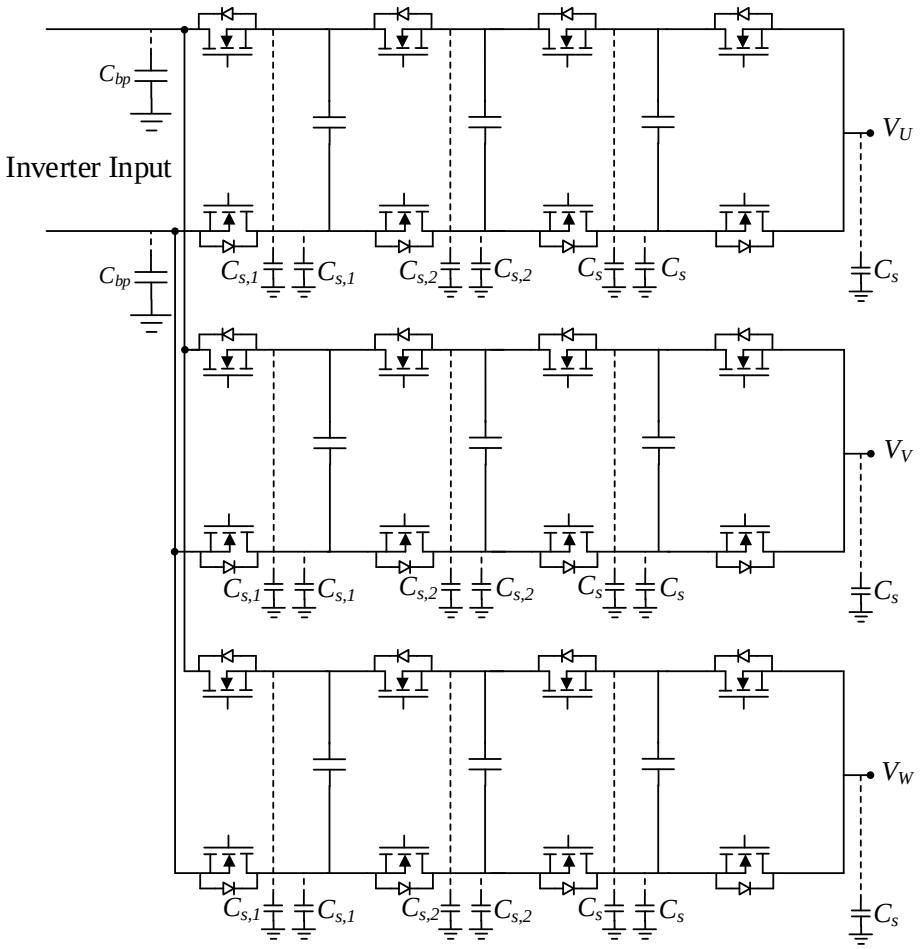


Figure 145 - Multilevel Series Inverter: 5- level Flying Capacitor per phase.

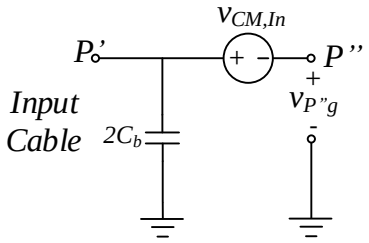


Figure 146 – Multilevel Series Inverter Input equivalent circuit.

The third part is defined by the parasitic capacitances current path not connected to the inverter output. The equivalent voltage source is also defined by the averaging of the voltages applied to each of these capacitances, referred to *P''*. These voltage sources represent the points where there is a *dV/dt*, and the CM current is mainly due to semiconductor parasitic capacitances since there is no load connected to this points. In the case of the FC topology, these points are the connections of the flying capacitors. For the present application, if $C_s = C_{s,1} = C_{s,2}$, the equivalent circuit of these current paths can be represented by $v_{CM,S}$ in series with $18*C_s$ in parallel, as shown in Figure 147.

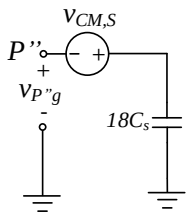


Figure 147 - Multilevel Series Inverter equivalent circuit: CM current path through $C_{s,1}$, $C_{s,2}$, and C_s.

By connecting the three-part referred for the same arbitrary point *P''*, the inverter equivalent CM circuit is presented in Figure 148.

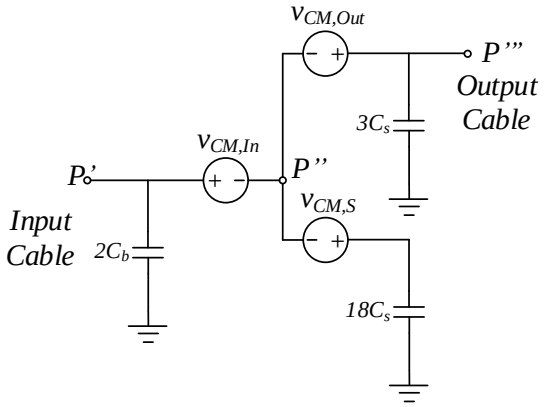


Figure 148 - Multilevel Series Inverter : CM current path for $C_{s,1}$ and $C_{s,2}$ = C_s.

If semiconductors parasitic capacitances are different, which can be due to other inverter topologies, it is necessary to create different average voltage sources connected to identical capacitances. For example, if $C_s \neq C_{s,1} \neq C_{s,2}$, different voltage sources are assembled, referenced to the same arbitrary point allowing the coupling between different current paths as exemplified in Figure 149.

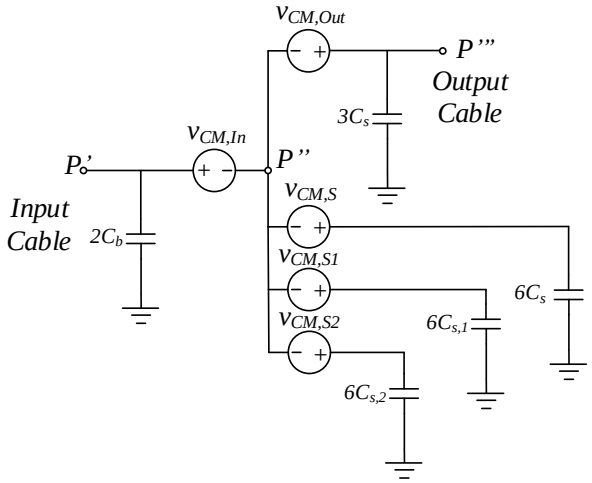


Figure 149 - Multilevel Series Inverter: CM current path for $C_{s,1} \neq C_{s,2} \neq C_s$.

The equivalent CM circuit for the power drive system with the 5-level FC topology is presented in Figure 150. The same approach for the 2-level inverter can be applied, making $v_{CM,In} = 0$, if $P'' = v_{dc}/2$ is referred to as average DC-Link voltage.

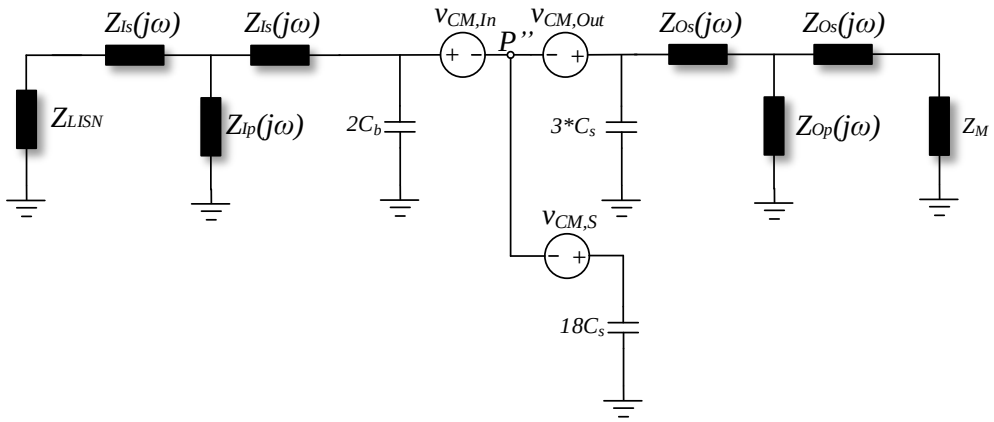


Figure 150 - Multilevel Series Inverter Power drive system CM equivalent circuit for $C_{s,1}$ and $C_{s,2} = C_s$.

The modeling methodology presented can be combined to determine $v_{CM,Out}$, $v_{CM,S,}$ and respective impedances associated with these CM voltage sources by considering a multilevel series and parallel topology. Contrarily to the 2-level topology, the model considering $v_{CM,Out,}$ and $v_{CM,S}$ is easier to be solved by transfer function than by quadrupole association.

3.4.3 EMI Filter design considering the equivalent circuit for multilevel inverters

According to the previous sections, the schematic in Figure 151 shows the equivalent circuit for the proposed 7- level FC topology presented in Chapter 1, with the respective impedances on input and output CM filters. The input and output filters are defined by series and parallel impedances (in blue) similar to those shown in Section 2.9.5.4.1 and Section 2.9.5.4.2. $Z_{filter\text{-}in\text{-}S}$ and $Z_{filter\text{-}out\text{-}S}$ define the input and output CM chokes, and $Z_{filter\text{-}in\text{-}P}$ and $Z_{filter\text{-}out\text{-}P}$ represent CM input and output capacitors. The output inductors (9 in total) to parallel the 3-level FC legs are represented by the equivalent impedance Z_{Lp}. This impedance is mainly defined by each leg inductance divided by the number of legs (40 µH/9 ≈ 4.5 µH at 40 kHz), representing less than 2% of the CM output choke value designed in Section 2.9.5.4.2 (300 µH at 40 kHz). Therefore, Z_{Lp} will be neglected for the calculation of CM currents.

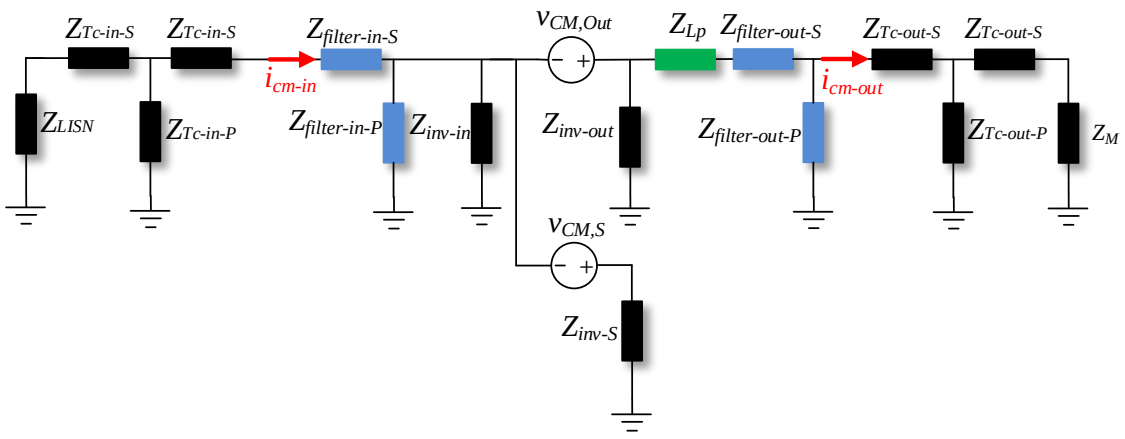


Figure 151 - Proposed coupled model to calculate input and output CM current.

The inverter input impedance $Z_{filter\text{-}in}$ was fixed as the capacitance of 950 pF as considered in Section 2.9.5.4.1. $Z_{inv\text{-}out}$ is defined by the impedance of 9 parasitic capacitances (C_{semi} = 46.5 pF – defined in Section 2.9.5.4.1) in parallel connected to the output of each leg. $Z_{inv\text{-}S}$ represents the impedance of the semiconductor capacitances connected to the flying capacitor connections; then, 18 * C_{semi} capacitances (2* C_{semi} per leg) are considered. Inverter CM voltage sources $v_{CM,Out}$, out, and $v_{CM,S}$ is defined as:

$$v_{CM,Out} = \frac{1}{9}.\left(\sum_{p=1}^{3} V_{U,p} + \sum_{p=1}^{3} V_{V,p} + \sum_{p=1}^{3} V_{W,p}\right),$$
$$v_{CM,S} = \frac{1}{18}.\left(\sum_{l=1}^{2}\sum_{p=1}^{3} V_{FC-U,p,l} + \sum_{l=1}^{2}\sum_{p=1}^{3} V_{FC-V,p,l} + \sum_{l=1}^{2}\sum_{p=1}^{3} V_{FC-W,p,l}\right), \quad (3.27)$$

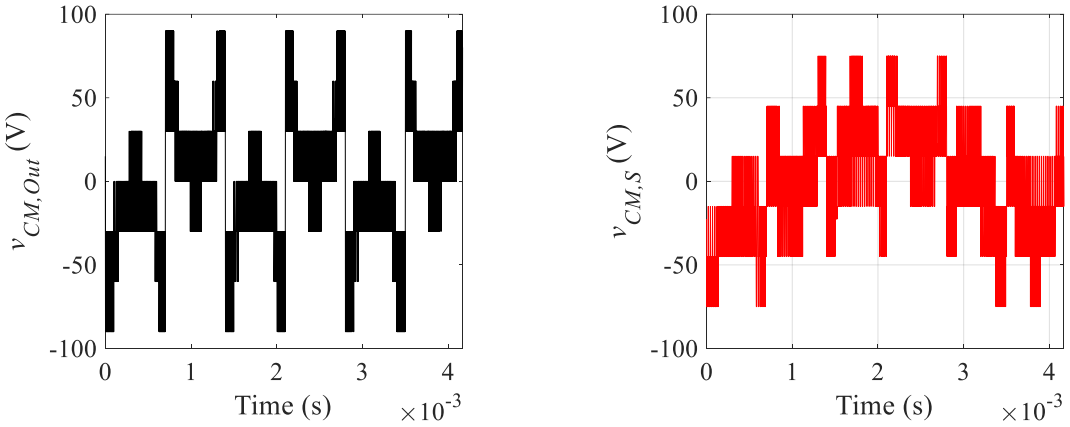
Where p is the number of the paralleled leg (3 max), and l is the flying capacitor connection (2 max for each 3 – level FC leg).

The current path's importance due to the additional CM voltage source ($v_{CM,S}$) and parasitic capacitances not connected to inverter output can be evaluated considering $i_{cm\text{-}in}$ and $i_{cm\text{-}out}$ peak values. The peak value of CM current is one crucial parameter used to design input/output CM chokes. Table 16 presents the three conditions considering the topology described above without filters (impedances in blue). Inverter operation point is the same considered in Chapter 2: 70 kVA, DPWM1, m_a = 0.94, I_{phase} = 130 A_{rms}, V_{bus} = 540 V and power factor of 36.36º. The results verify the impact of considering only $v_{CM,Out}$ (named as *Traditional Model*, with $Z_{inv\text{-}S} = \infty$) and with CM voltage sources - $v_{CM,Out}$ and $v_{CM,S}$ - (named as *Proposed Model*, with $Z_{inv\text{-}S}$ = 18 * C_{semi}).

Table 16 - Impact of Traditional Model and Proposed model on $i_{cm\text{-}in}$ and $i_{cm\text{-}out}$ peak value.

Setup					Proposed Model		Traditional Model	
					$i_{cm\text{-}in}$	$i_{cm\text{-}out}$	$i_{cm\text{-}in}$	$i_{cm\text{-}out}$
Nº	f_{sw}	cable	C_{semi}	$C_{Zinv\text{-}in}$	A_{pk}	A_{pk}	A_{pk}	A_{pk}
1	40 kHz	10 m	46.5 pF	950 pF	2.92 A	0.84 A	1.59 A	0.64 A
2	40 kHz	10 m	46.5 pF	300 pF	2.97 A	0.84 A	1.58 A	0.64 A
3	40 kHz	10 m	100 pF	950 pF	4.56 A	0.92 A	2.79 A	0.64 A

According to the results presented in Table 16, for setup *Nº* 1, which was the same conditions for the inverter's optimal solution in Chapter 2, there is an increase of 84% on $i_{cm\text{-}in}$ by considering the proposed model. On the other hand, an increase of 32% is verified on $i_{cm\text{-}out}$. These results reinforce the importance of considering the parasitic capacitances current path not connected to the inverter output. In other words, the *Proposed Model* with both $v_{CM,Out}$, and $v_{CM,S}$, which waveforms are shown in Figure 152.



a) *b)*

Figure 152 - Voltage sources $v_{CM,\,Out,}$ and $v_{CM,\,S}$ for setup Nº 1

Setup *Nº* 2 evaluate the impact of inverter input capacitance responsible for $Z_{inv\text{-}in}$. Passing from 978 pF to 300 pF (reduction of 61%), it is verified an increase of 50 mA on $i_{cm\text{-}in}$ by considering the proposed model, referred to the setup *Nº* 1. No difference was verified on $i_{cm\text{-}out}$. Therefore, inverter input impedance has a negligible impact on CM currents. However, this conclusion is valid only if this capacitance is higher than a few hundred pF. The differences between the *Proposed Model* and the *Traditional Model* are close to the ones verified for setup *Nº* 1.

Setup *Nº* 3 evaluate the impact of semiconductor parasitic capacitance C_{semi}. Passing from 46.5 pF to 100 pF, it is verified an increase of 1.64 A (56%) on $i_{cm\text{-}in}$ by considering the proposed model, referred to the setup *Nº* 1. On the other hand, an increase of 80 mA (9%) was verified on $i_{cm\text{-}out}$. Regarding the differences between the *Traditional Model* and *Proposed Model*, one increase of 63% and 44% is verified for $i_{cm\text{-}in}$ and $i_{cm\text{-}out}$. This condition highlights the importance of semiconductors parasitic capacitance on the calculation of CM input and output currents.

The optimization of CM input and output filters considering the *Proposed Model* was performed according to the flowchart shown in Figure 153. This routine considered the LISN, motor, input, and output cables impedances identical to those presented in Section 2.9.5, together with CM chokes and capacitors design functions of Section 2.8. The inverter nominal operation point is the same as setup *N*º1.

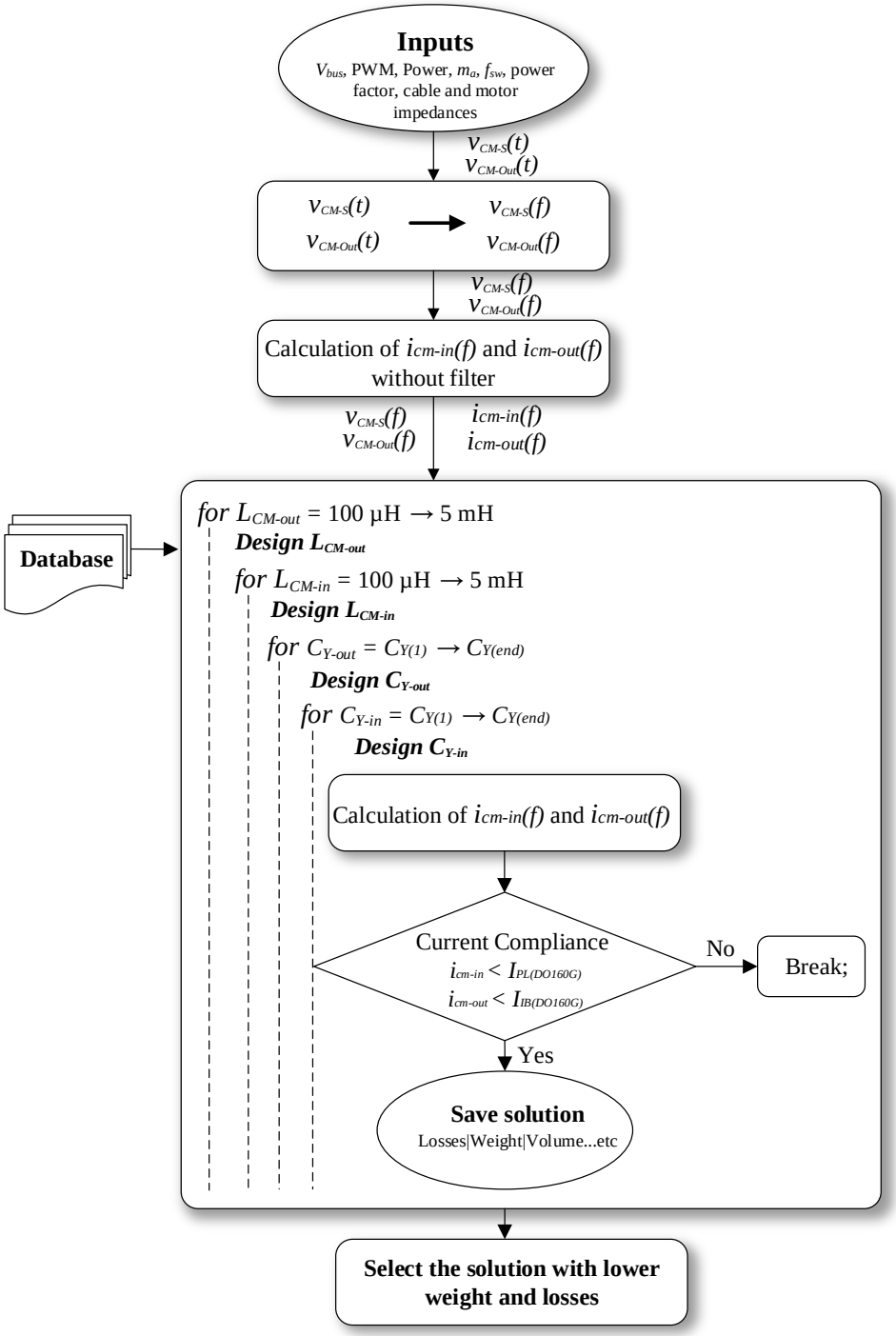


Figure 153 - EMI filter design – input and output - flowchart considering the proposed coupled model.

Additionally, different EMI filter dispositions were considered in this study, with the intent to identify not only the lightest topology but the best way to distribute these filters in the multilevel converter. The different distributions are listed below:

1) The same topology is used in Chapter 2, considering one CM choke on inverter input and another on inverter output. Both CM chokes are associated with CM capacitors, $C_{Y\text{-}in}$ and $C_{Y\text{-}out}$. This topology is named Topology 1, and it is shown in Figure 154.

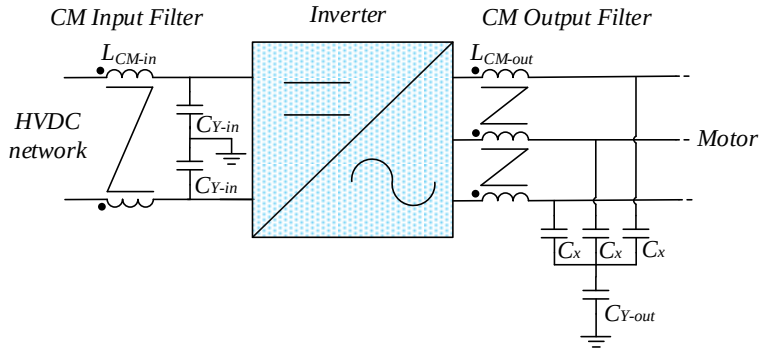


Figure 154 - EMI filter Topology 1.

2) Topology 2 also considers two CM chokes (on inverter input and output), but CM capacitors are considered only on inverter input ($C_{Y\text{-}in}$ only). This topology is the traditional one considered in [17], presented in Figure 155. This topology's main advantage is that there is no need for C_x capacitors on inverter output to create the middle point to connect $C_{Y\text{-}out}$. On the other hand, $L_{DM\text{-}out}$ tends to be increased, as the entire filter weight, due to the reduction of the CM filter order.

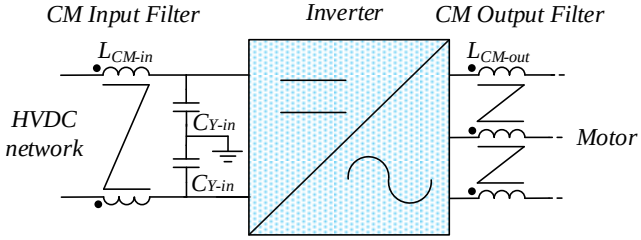


Figure 155 - EMI filter Topology 2.

3) Topology 3 considers the same output filter as Topology 1 ($L_{DM\text{-}out}$ and $C_{Y\text{-}out}$), but a different approach is applied for the input filter. Theoretically, the filter should be placed as close as possible to the noise source, the inverter, in this case. The inverter proposed in Chapter 2 comprises nine switching cells (3 FC legs p/phase), representing 9 different noise sources. Then, one CM choke is considered for each switching cell, totalizing nine ideally paralleled but as close as possible to each switching cell, as shown in Figure 156. $C_{Y\text{-}in}$ is also split between the nine legs. Beyond placing the filter close to the noise source, another advantage of this filter disposition is considering a lower DM current level. The DM current defines the winding copper section for the CM choke and contributes to the core saturation, as presented in Sectio 2.8.2.2. Therefore, by reducing DM current, the

size of the CM choke is also reduced. In this application, the inverter input DM current is around 110 A; considering nine paralleled CM chokes, around 12 A is expected in each choke.

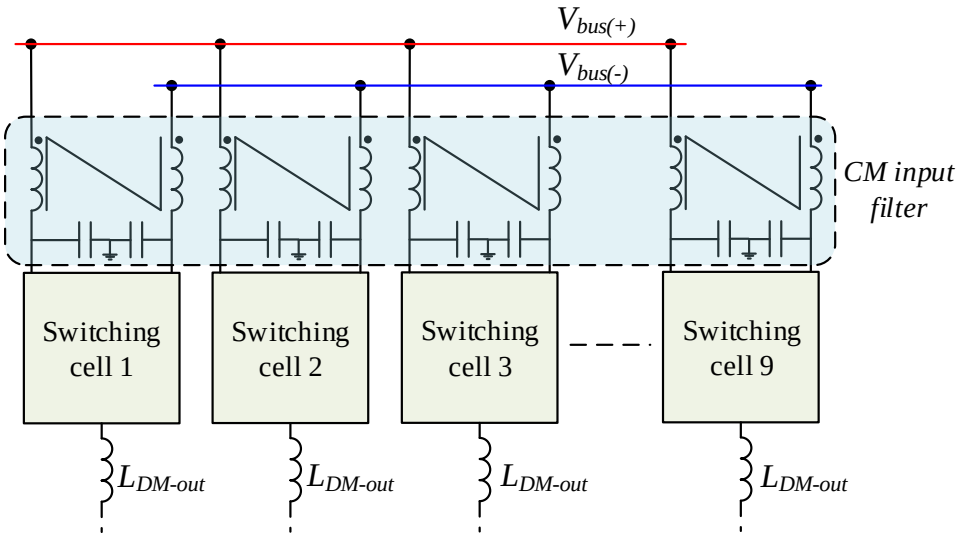


Figure 156 - EMI input filter split between the inverter nine legs.

4) The output CM choke windings are designed to handle inverter DM input current (110 A), making it challenging to coil the choke. In high current applications, power connections are commonly made using copper bars, preventing CM chokes winding. The use of single-turn feed-though chokes in series is one practical solution investigated in [234]. It is evaluated in Topology 4 for $L_{CM\text{-}in}$ and $L_{CM\text{-}out}$, as exemplified for $L_{CM\text{-}out}$ in Figure 157. The inductance L is proportional to the number of cores in series T. It is proportional to the square of the number of turns N = 1. The winding design constraint was substituted to guarantee 2*WD (wire diameter) ≤ 90%*ID (internal core diameter). This same consideration was used for $L_{CM\text{-}in}$. The calculation of winding resistance R_{dc} considered the wire length $T*B$. The other design parameters were the same described in Section 2.8.2.2.

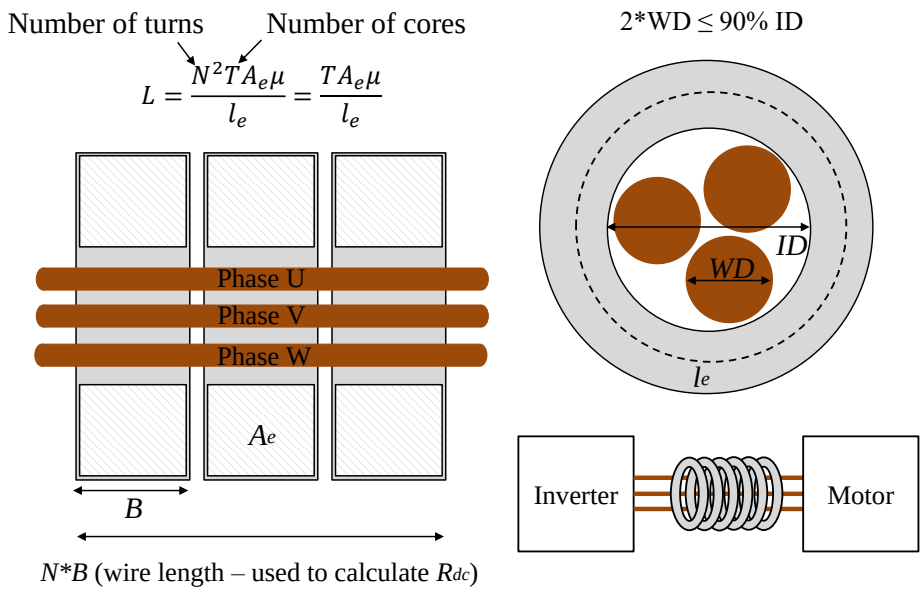


Figure 157 - Design of single-turn feed-though chokes in series.

5) Topology 5 considers single-turn feed-through chokes in series for $L_{CM\text{-}in}$ only, while $L_{CM\text{-}out}$ considered the traditional multi-turn CM choke used in Topology 1.

The optimization results for the five topologies described above are shown in Table 17. Topology 1 is the lightest solution with 600 g. Regarding the uncoupled design of EMI filters in Chapter 2, there was an increase of 85% (276 g) on filter weight (input + output) considering the proposed model. This increase is seen mainly on the input CM choke that handles CM mode current due to output cables and motor path, as presented in the experimental verification for the 2-level inverter. Therefore, a precise EMI filter design must use the coupling between input and output CM currents.

$C_{Y\text{-}out}$ allows a weight reduction of 66.7% (1.2 kg) and loss reduction of 9.4 W (Comparison between Topology 1 and Topology 2). It impacts both input and output CM chokes, reducing $L_{DM\text{-}out}$ from 3.4 mH to 500 µH and $L_{DM\text{-}in}$ from 1.25 mH to 300 µH.

On the other hand, the idea of split CM input chokes between the nine legs increases 95% (570 g) of EMI filter weight (comparison between Topology 3 and Topology 1). Single turn feed-though chokes have a powerful impact on filter weight since many cores must be associated in series. In Topology 4, 10 cores (T60004-L2050-W625) are necessary for $L_{DM\text{-}in}$ and 24 for $L_{DM\text{-}out}$. In terms of weight, it represents an increase of 2.4 kg (400%) compared to Topology 1. In topology 5, the weight increase is around 100% (1 kg). Therefore, it is verified that $L_{DM\text{-}out}$ substantially impacts filter weight considering single turn feed-though chokes. These solutions are not attractive from the point of view of gravimetric power density.

Table 17 - EMI filter solutions for different filter repartition at 40 kHz.

Topology	Solution	Weight (kg)	Losses (W)
1	$L_{cm\text{-}in}$ = 300 µH | $L_{cm\text{-}out}$ = 500 µH $C_{Y\text{-}in}$ = 94 nF | $C_{Y\text{-}out}$ = 36 nF	0.6	6.7
2	$L_{cm\text{-}in}$ = 1.25 mH | $L_{cm\text{-}out}$ = 3.4 mH $C_{Y\text{-}in}$ = 132 nF	1.8	16.1
3	$L_{cm\text{-}in}$ = 300 µH p/leg | $L_{cm\text{-}out}$ = 700 µH $C_{Y\text{-}in}$ = 63 nF/9 legs | $C_{Y\text{-}out}$ =33 nF	1.17	4.5
4	$L_{cm\text{-}in}$ = 200 µH * | $L_{cm\text{-}out}$ = 500 µH** $C_{Y\text{-}in}$ = 94 nF | $C_{Y\text{-}out}$ = 36 nF	3	8.6
5	$L_{cm\text{-}in}$ = 200 µH * | $L_{cm\text{-}out}$ = 500 µH $C_{Y\text{-}in}$ = 94 nF | $C_{Y\text{-}out}$ = 36 nF	1.2	7.3

* 10 cores T60004-L2050-W625

**24 cores T60004-L2050-W625

3.5 Chapter Conclusions

This chapter presented a methodology for modeling power converters and other associated elements, such as cables and motor vis-a-vis common-mode. This modeling is presented by [226], and it was applied in this thesis to model each element that composes the power drive system. This section's objective was to propose an equivalent CM circuit for multilevel inverter topologies considering the coupling between input and output, aiming for a more precise EMI filter design. This subject was identified in Chapter 1 as the first research axis.

The equivalent circuit for a 2-level inverter was validated experimentally, and it is very close to the circuit presented in [17]. Then, this methodology was applied to model multilevel parallel and series inverters, generating an equivalent circuit composed of at least two CM voltage sources. One is connected to inverter output, and another is connected to the semiconductors parasitic capacitances subjected to *dV/dt.* This equivalent can be generalized for different multilevel topologies beyond FC.

This proposed model was applied to the 7 – level topology proposed in Chapter 2, intending to verify the impact on EMI filter design. The EMI filter optimization design shows an increase of 85% (276 g) on filter weight (input + output), comparing the uncoupled model presented in Chapter 2 and the coupled model for the same conditions. It reinforces the need for a more precise model to design EMI filters for multilevel converters. Additionally, a parametric study of CM filter topology and repartition showed that the lightest solution (600 g) found was one CM choke on inverter input and one

CM choke on inverter output. The use of $C_{Y\text{-}out}$ allows a significant weight reduction of 66.7% (1.2 kg) compared to the topology without it.

The next chapter presents the impact of different PWM techniques on the weight and efficiency of the 7 – level topology proposed in Chapter 2.

CHAPTER 4

Evaluation of PWM techniques on the inverter design

THIS chapter evaluates different PWM techniques and their impact on the overall power density and efficiency of the 7-level inverter topology proposed in Chapter 3. This evaluation considered the EMI model described in Chapter 3. Two PWM techniques are proposed and evaluated to reduce flying capacitor and output inductors weight and increase the final inverter gravimetric power density.

Summary

4.1 PWM Optimization

The second research ax identified in Chapter 2 considered evaluating different PWM techniques to increase inverter overall power density and efficiency. Section 2.4 briefly presented traditional PWM techniques using Zero Sequence Injection (ZSI) to modify the modulating signal to increase the inverter performance.

With the complexity increase in electric systems in the last decades referring to efficiency, reliability, and safety, new challenges were inherently associated with power electronics. The electric stress reduction on capacitors, in the form of voltage ripple, the current ripple in inductors and electric motors, and other phenomena associated with long-cable systems are recurring themes. Adding to that, their impact on semiconductor losses and colling systems pushes the development of new technologies and ways of controlling the power converters.

PWM techniques directly impact capacitor voltage ripple, inductor current ripple, and, consequently, power converter losses. SVPWM techniques have become popular in motor drive applications due to some key points: the utilization of DC-link voltage, lower output line voltage, and output current *THD*; ease of implementation and design flexibility. On the other hand, the DPWM techniques present higher-modulation range performance and lower semiconductor losses than SVPWM. Despite their positive points, it is not easy to point the PWM technique with the highest performance for each application since it depends on different and numerous constraints. In this thesis, two main constraints guided the work presented in Chapter 2: gravimetric power density and efficiency.

The 7-level topology proposed in Chapter 2 presents 690 W loss at 40 kHz for the DPWM1 technique (lower semiconductor losses according to Section 2.7), being the semiconductor responsible for 91.5% of total loss. DPWM techniques usually develop lower losses on power converters since they present lower commutations than SPWM and SVPWM techniques. The selection of the best DPWM technique to reduce semiconductor losses depends on the system power factor. Consequently, the creation of a new PWM technique is focused on inverter weight reduction. Among the different devices which compose the inverter, flying capacitors and output paralleled inductors represent 63%, at 10 kHz, and 36%, at 40 kHz, of the entire inverter weight. These devices weights are directly related to the voltage ripple for the flying capacitors and the current waveform for the output inductors.

Due to the lack of works on using PWM techniques to reduce flying capacitor and output paralleled inductors weight, these subjects were investigated and are presented in this section. The creation of different PWM techniques to reduce flying capacitors and output inductors of the 7-level topology proposed in Chapter 2. The impact of these techniques on the other devices of the inverter and its efficiency will be evaluated and compared to other PWM techniques. The PWM technique, which presents the highest gravimetric power density, will be chosen for the inverter realization presented in Chapter 5.

4.2 PWM Creation Methodology

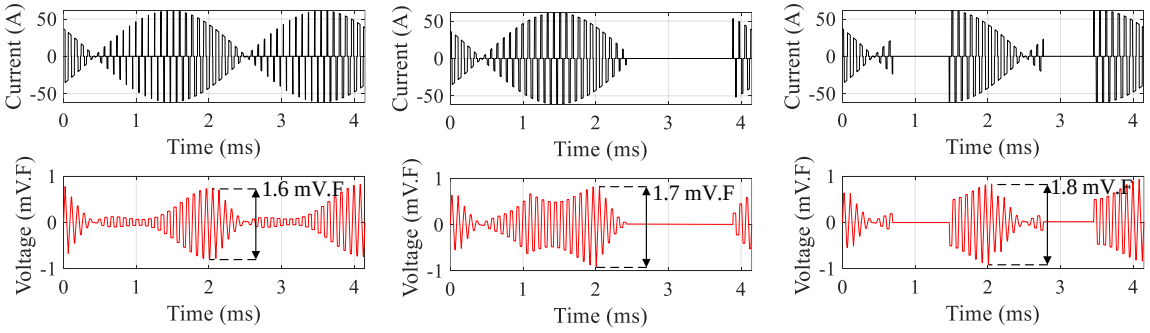
The work presented in [70] and [224] shows a methodology to define an optimal common-mode offset (CMO) for the ZSI to define the PWM technique that reduces the magnetic flux of coupled inductors in parallel inverters. When a CMO is added to the reference signal of a multilevel converter, it may allow several improvements, such as the increase of the linearity range of the output voltage and the reduction of the output current THD_i and commutation losses. It may also reduce flying capacitor voltage unbalance [236]. This section focuses on applying this methodology to find the optimal CMO to reduce flying capacitors and output inductors weight. Firstly, the mathematical formulation for the design of flying capacitors and output paralleled inductors are presented, and then the methodology is explained.

4.2.1 Flying capacitor formulation

Flying capacitor weight is related to the required capacitance value, voltage, and current levels presented in the design procedure in Section 2.8.1.1. Since voltage level and current on flying capacitor are fixed considering the application, the voltage ripple (ΔV_{FC}) defines its weight, and it is calculated according to:

$$\Delta V_{FC} = \frac{1}{C_{FC}} . \int \tilde{i}_{FC} dt. \tag{4.1}$$

So it depends on the capacitor's current (i_{FC}) and applied duty cycle, as presented in Figure 158, for SPWM, DPWMMIN, and DPWM1, in mV.F. Since the duty cycle behavior depends on the PWM technique, the flying capacitor ripple will change.



(a) SPWM *(b) DPWMMIN* *(c) DPWM1*

Figure 158 - Flying capacitor current and voltage ripple in mV.F for the 7-level 70 kVA/540 V inverter, m_a = 0.9428, PFA = 36.67°, f_{sw} = 10 kHz and f_{lf} =240 Hz.

4.2.2 Output paralleled inductors formulation

The uncoupled inductors to parallel the FC legs were designed according to the max current ripple, as described in Section 2.2.2.1. The equation developed in this section showed that the inductance only depends on the number of paralleled legs, current ripple, the number of output levels, bus voltage, and inverter switching frequency. The considered current ripple is obtained in situations in which the duty cycle causes maximum current oscillation. These ripple values for a 3-level FC converter occur for the duty cycle between 1/6 - 1/3 and between 2/3-5/6, as shown in Figure 158 for a linear variation of the duty cycle between 0 and 1.

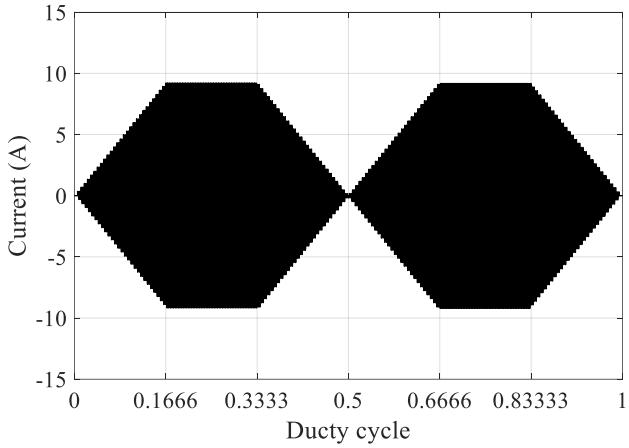
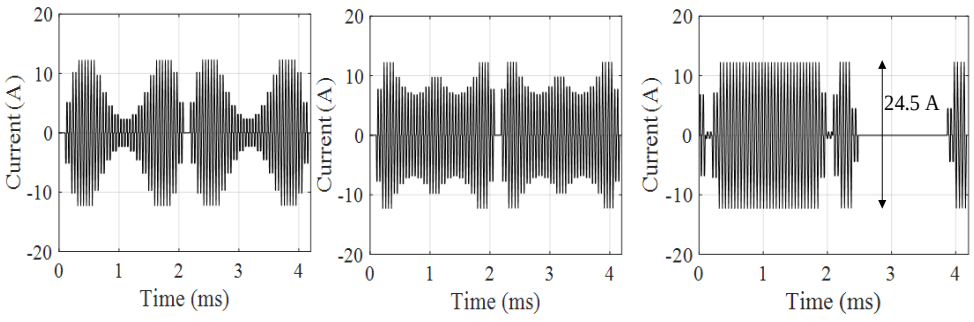


Figure 159 - Output inductor current ripple as function of dutycycle for the 7-level 70 kVA/540 V inverter, L =30 µH, m_a = 0.9428, PFA = 36.67°, f_{sw} = 40 kHz and f_{lf} =240 Hz.

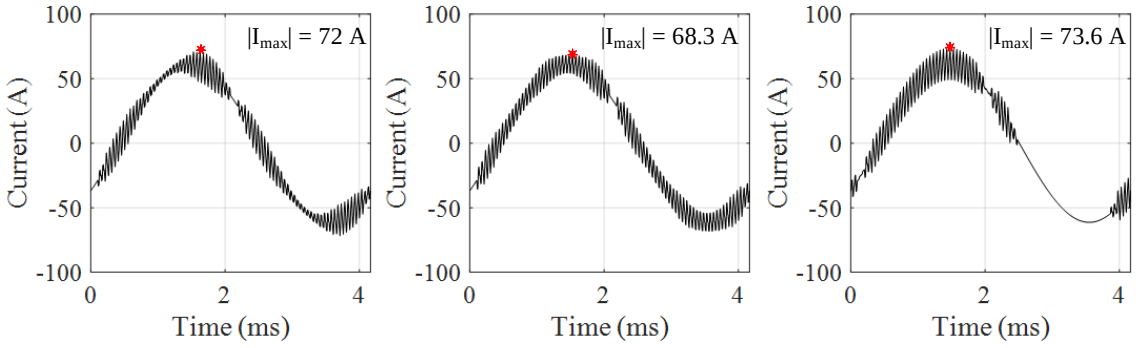
Most of the operating points of an inverter, on steady-state, are carried out at high modulation index values, including the one defined in this thesis (m_a = 0.9428). Therefore, the inverter operation will pass between the duty cycles in which the maximum current ripple is achieved. Then, for high modulation index values, the maximum current ripple does not change independently of the PWM technique for the same inductance value. This hypothesis is presented in Figure 160 for SPWM, SVPWM, and DPWMIN. In that case, the maximum current ripple is around 24.5 A for all techniques.



(a) SPWM *(b) SVPWM* *(c) DPWMMIN*

Figure 160 - Output inductor current ripple for the 7-level 70 kVA/540 V inverter, L =121 µH, m_a = 0.9428, PFA = 36.67°, f_{sw} = 10 kHz and f_{lf} =240 Hz.

The inductor current is formed by the sum of the ripple and the sinusoidal component of the output current. Although the ripples have equal amplitudes, each modulation technique has a different peak current since the maximum ripple occurs at different times for each technique, according to Figure 161.



(a) SPWM *(b) SVPWM* *(c) DPWMMIN*

Figure 161 - Output inductor current for the 7-level 70 kVA/540 V inverter, L =121 µH, m_a = 0.9428, PFA = 36.67°, f_{sw} = 10 kHz and f_{lf} =240 Hz.

As shown in Figure 2.8, the design of the output inductor depends on the windings and the magnetic core. The wire gauge considers inductors *RMS* current, it defines the windings, the number of wires in parallel, and the number of turns. The magnetic core is determined by its saturation, related to current peak value and the number of turns, and the temperature increase due to core losses. As core selection is related to the inductor's peak current, it is considered the optimization variable to reduce the output inductor's weight.

4.2.3 Optimal CMO Methodology

The recursive algorithm proposed by [70] and [224] is implemented to obtain the optimal CMO according to the flowchart in Figure 162. An offset is added to the three phases sinusoidal references to calculate the maximum voltage ripple on the flying capacitors (ΔV_{FC}) and the peak current on the paralleled inductors ($I_{Loutput\text{-}pk}$) for each angle of the fundamental output voltage, modulation index, and power factor.

The offset resulting in the lowest value of the maximum ΔV_{FC} and $I_{Loutput\text{-}pk}$ among the three phases is selected for each angle. The whole optimal zero sequences can be found by recomposing these offsets. This algorithm occurs in four loops. The innermost loop 4 represents the offset variation added to the sinusoidal reference, while loop 3 indicates the variation of the reference angle to traverse the 360 ° of the sinusoidal reference. Thus, loop 4 varies the offset between values that, when added to the sinusoidal reference at a given angle, give the results for one modulation index (m_a). The two loops together are responsible for identifying the offsets that generate the optimal CMO.

Loop 2 occurs with the variation of the modulation index, and loop 1, the most external, represents the variation of the power factor (*FPA*), defined as the angle between the voltage and current. A change in any of these two loops implies a different CMO.

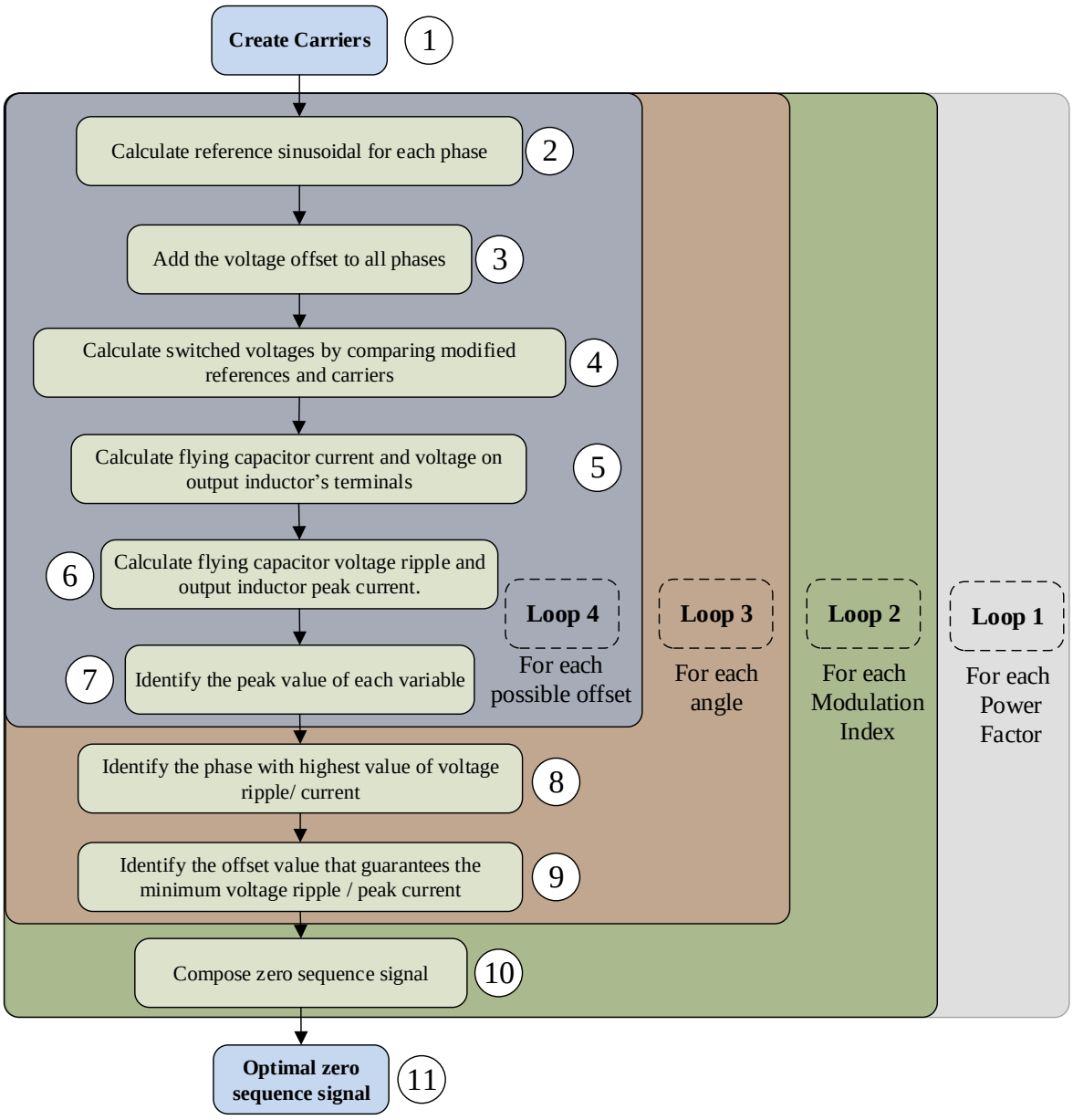


Figure 162 - Algorithm flowchart to find the optimal CMO to optimize a given characteristic

The first step of the algorithm is constructing the triangular carriers according to the modulation technique, as shown in Figure 163. By comparing the modulation wave with those carriers, it is possible to determine each switch conduction status and define the currents that pass through the converter components.

The converter studied in this thesis comprises 3-level FC legs, and each leg has two switching cells, leading to the need for two carriers per leg. The Phase Shift (PS) modulation technique is adopted since it presents switching periods for each transistor distributed symmetrically over time. It allows the

natural balance of the flying capacitor voltage [237] — contrarily compared to Phase Disposition (PD) and Phase Opposition Disposition (POD).

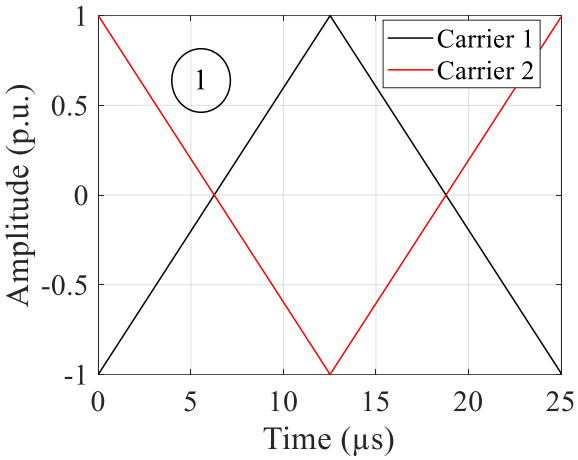


Figure 163 - Step 1: Create Carriers

After the carriers are created, sinusoidal references with the peak value of 1 are constructed in the second step. For a given angle, the values of the three sine waves are taken (the points highlighted in Figure 164). The one with the highest absolute value is selected (angle represented by the green rectangle), and from this value, the difference to 1 is calculated. This difference is what determines the range of variation of the offset in loop 3. For example, for an instant, when the highest absolute value among the references is 0.8, the corresponding allowed offset absolute value variation is 0.2, meaning that the selected reference varies between 0.6 and 1.

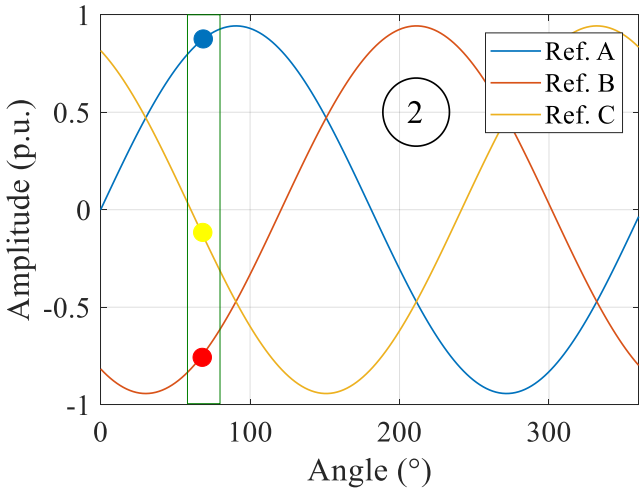


Figure 164 - Step 2: Create sinusoidal references

In step three, the same range of offset variation is applied to the three references, and the exact value is added simultaneously to the three of them, represented by the points in Figure 165. After this, it is made a comparison between these points and the carriers. This comparison is possible because the sine wave is sampled with a number of points equal to the ratio between the switching frequency and

the fundamental frequency, ensuring that each point in loop 2 is compared with the carrier's entire period. This comparison, given in step 4, is the conduction states of each switch of the converter.

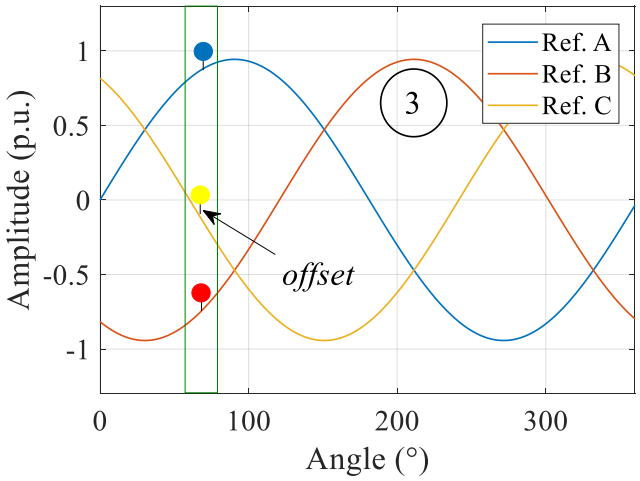


Figure 165 - Step 3: Add voltage offsets on sinusoidal references

Figure 166 (a) illustrates the 3-level FC leg composed of two switching cells and their respective switches. On the other hand, Figure 166 (b) shows the FC leg's conduction states in an instant in which the keys S_1 and S_2 do not conduct simultaneously. It means that, at that moment, the sinusoidal reference imposes a duty cycle lower than 0.5 [51].

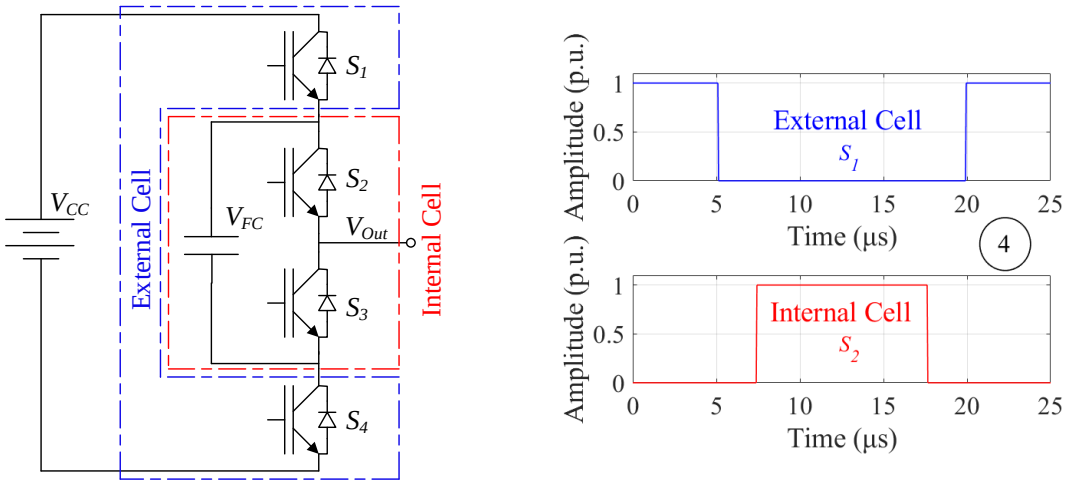
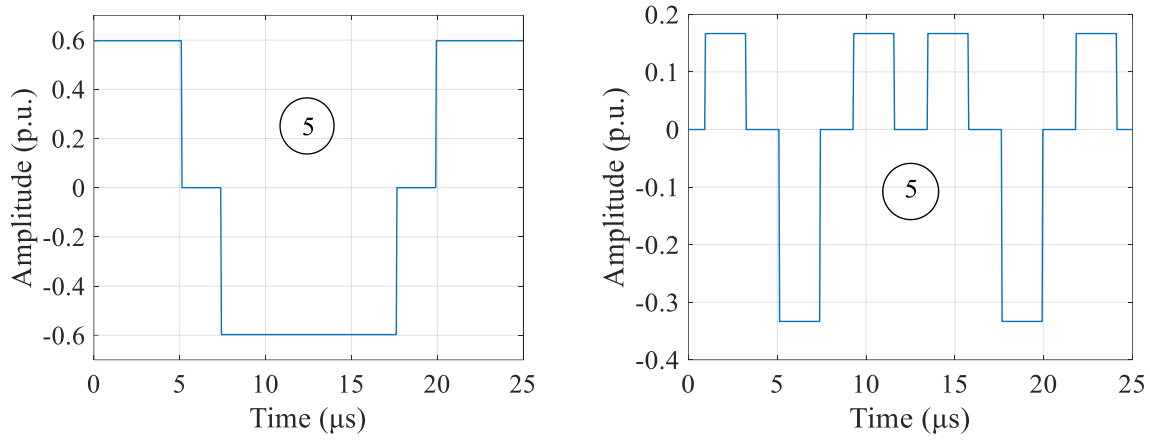


Figure 166 - (a) Three-level leg of a 3-level FC converter and (b) Step 4 of the flowchart: switch conduction states.

From these conduction states determined on the flowchart's 4th step, and knowing the combinations presented in [238] that guarantee the current circulation through each flying capacitor, it is possible to estimate the current that passes through the capacitor, resulting in the flowchart's 5th step. The current that passes through the capacitor $I_{FC,j}$, is given by the following equation, as defined in [238], and it is shown in Figure 167 (a) for one switching period.

$$I_{FC,j} = \left(S_{2j} - S_{1j}\right).I_{phase,j} \tag{4.2}$$

S_{2j} is the conduction state of the top switch of the internal cell and S_{1j} is the conduction state of the external cell's top switch. The index *j* indicates the converter leg, which varies from 1 to 3, since there are three legs in parallel per phase, while $I_{phase,j}$ is the leg output current per phase (a sinusoidal reference). It is worth mentioning that the process is identical for all phases and parallel legs since it is considered the ideal current division. Besides, it is necessary to obtain the voltage on the output inductors terminals of each leg, shown in Figure 167 (b). As discussed in Section 2.2.2.1, output inductors terminals voltage is given by the difference between the phase output voltage V_o and leg output voltage.



(a) *(b)*

Figure 167 - Step 5: determine a) flying capacitor current and b) voltage on output inductor terminals.

According to the flowchart, the voltage and current ripples on the flying capacitors and output inductors are obtained in step 6. For this, it is necessary to use Equations (4.3) and (4.4). The inductor peak current ($I_{Loutput\text{-}pk,j}$) is obtained through the voltage integral (current ripple) and the given angle's current value. The second equation can obtain the voltage over the capacitor ($\Delta V_{FC,j}$) from the current integral. In both equations, the values of the capacitor and the inductor are indifferent. Since these are constant, they do not imply any change in the values calculated over time. However, the results of these integrals represent the complete electrical variables and not just the ripple. Therefore, it is necessary to subtract its average value so that only the ripple is obtained.

$$\begin{aligned} \Delta I_{Loutput-pk,j} &= \int V_{Loutput,j}.dt - mean\left(\int V_{Loutput,j}.dt\right), \\ I_{Loutput-pk,j} &= \max\left|\Delta I_{Loutput-pk,j} + I_{phase,j}\right|. \end{aligned} \tag{4.3}$$

$$\Delta V_{FC,j} = \int I_{FC,j}.dt - mean\left(\int I_{FC,j}.dt\right). \tag{4.4}$$

Once this is done, exemplified in Figure 168 for the flying capacitor voltage ripple, have their maximum values stored for each offset (step 7) value considered in a given angle of the fundamental. These values calculated in loop 1 generate the curves presented in Figure 169 for the three phases.

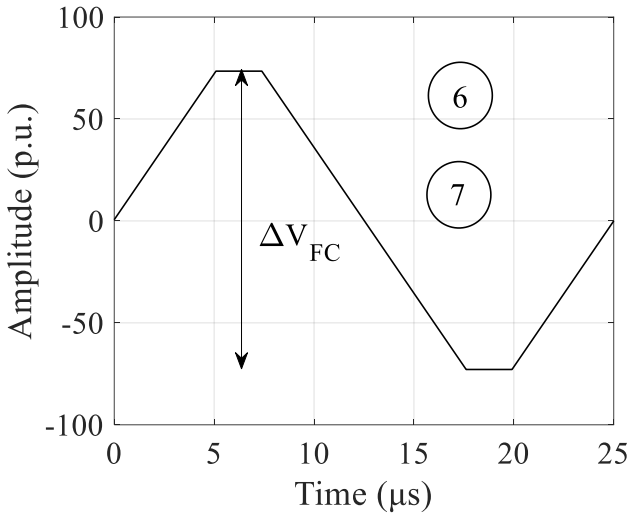


Figure 168 - Steps 6 and 7: Calculate and identify the maximum voltage ripple on the floating capacitor.

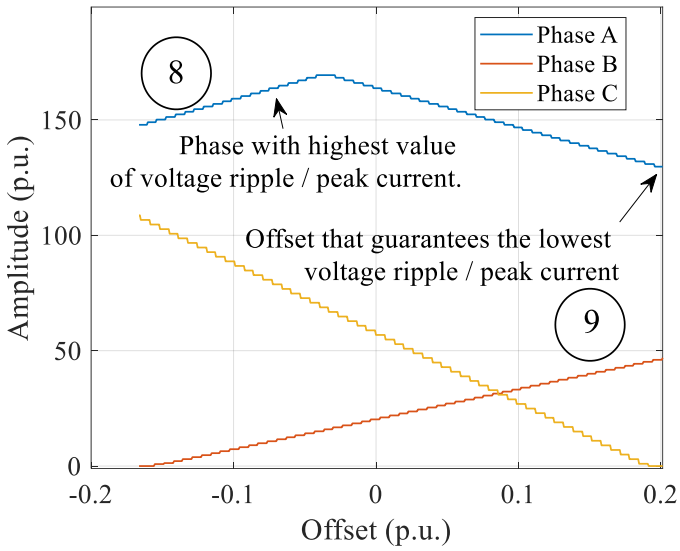
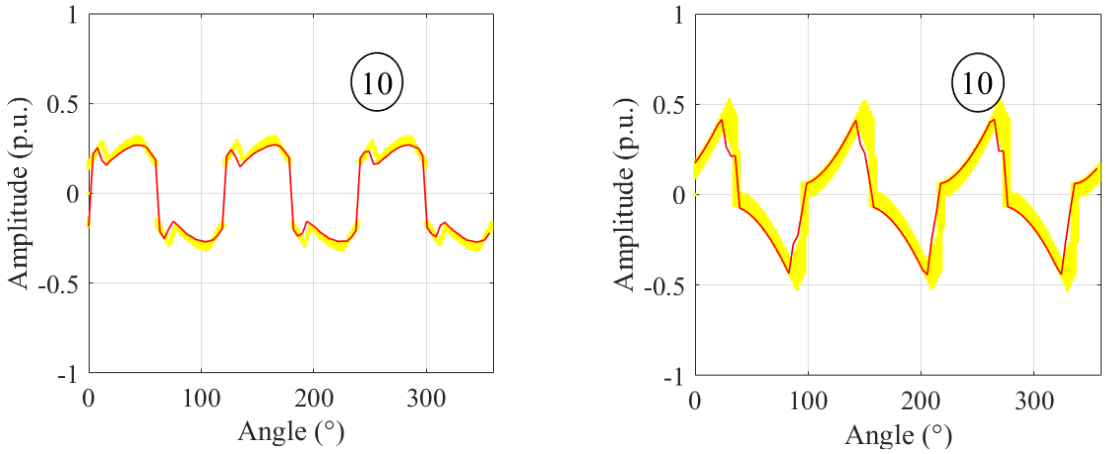


Figure 169 - Steps 8 and 9: Identifying the phase with the highest ripple and the offset causes the lowest flying capacitor voltage ripple or output inductor peak current.

Step 8 identifies the phase with the highest value of voltage ripple (or current peak for the output inductors). Then, the value of offset that guarantees the lowest value of voltage ripple/peak current is selected, as shown in Figure 169. This process is done to ensure that, at all times, the phases have the smallest possible value because when choosing the minimum point of the phase that has the highest value, the others will always be smaller than this one. Once the offset value that guarantees the slightest voltage ripple/peak current for a given angle is obtained, this value is stored in a variable.

Then, this procedure is repeated for the next angle of the sinusoidal reference until it reaches 360 °, thus completing loop 3.

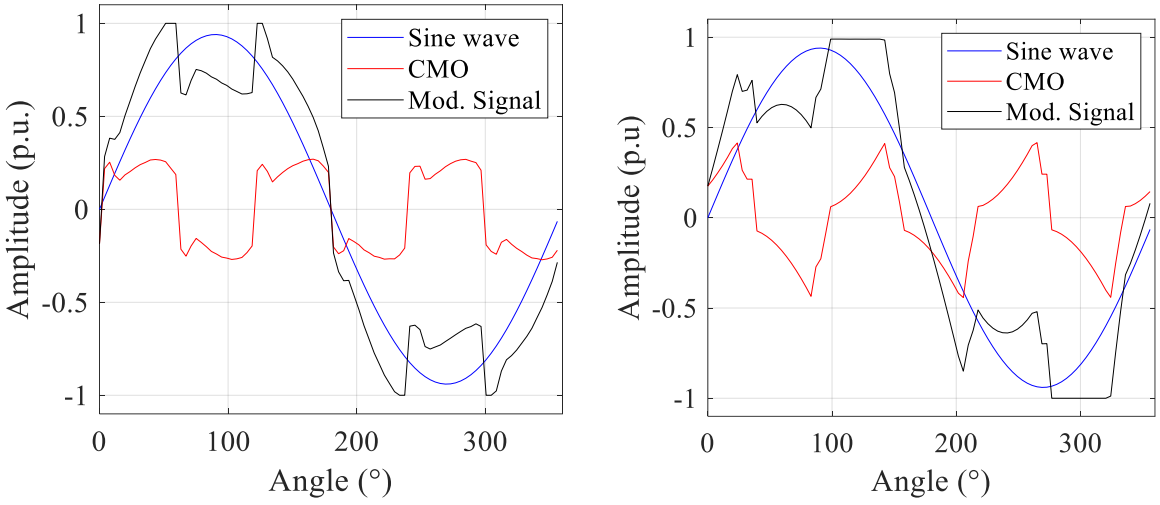
An essential factor to be considered is the difficulty of constructing the zero sequence components obtained from the Digital Signal Processor (DSP) and their practical application. To avoid this problem or minimize it, offsets are stored that cause a maximum increase of 2% in the voltage ripple/peak current. From these points, indicated in Figure 170, the software selects those that do not have sudden variations, to prevent the converter from having an operation with great stress on the switches. The red curve represents the CMO calculated from the yellow points and the algorithm step 10.



(a) *(b)*

Figure 170 - Step 10: Optimized CMO (in red) to reduce (a) flying capacitor voltage ripple and (b) output inductor peak current. In yellow it is shown the points with 2% variation generated by the algorithm.

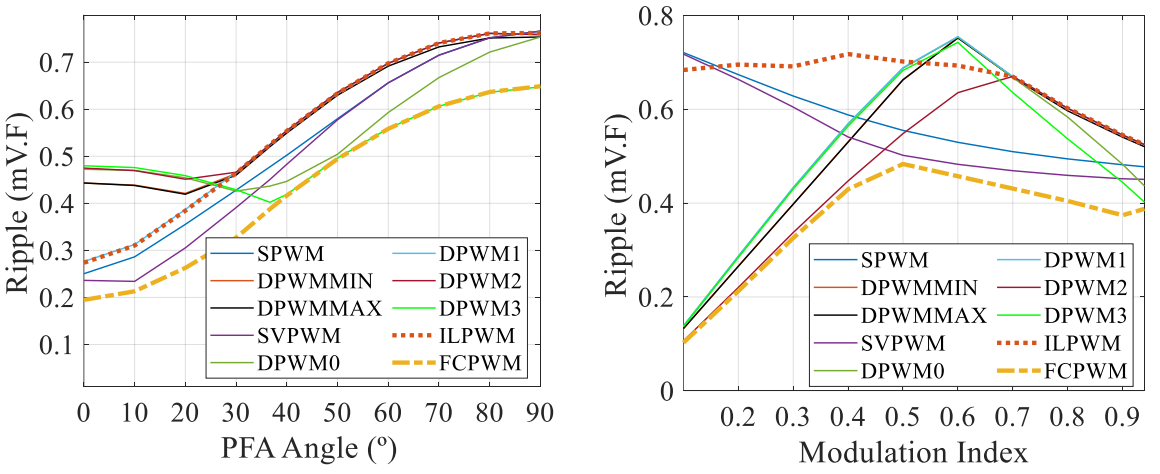
The optimized PWM techniques (step 11) are presented in Figure 171 (a) for the flying capacitor voltage ripple and Figure 171 (b) for the inductor peak current. These techniques will be referred to as FCPWM and ILPWM in the next section and were achieved considering the modulation index and *PFA* used in Chapter 2.



(a) *(b)*

Figure 171 - Optimized CMO (in red) and Modulation signals (in black) to reduce (a) FCPWM and (b) ILPWM. These signals consider the operating point of the optimization of Chapter 2 (m_a = 0.9428, PFA = 36.67 º, f_{sw} = 40 kHz and f_{lf} = 240 Hz).

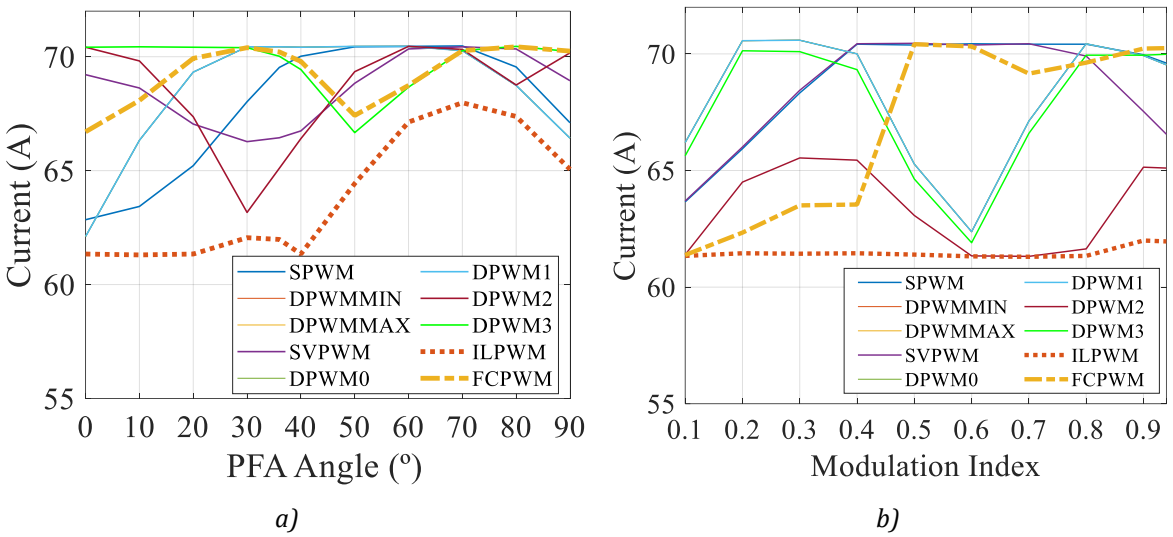
The optimal CMOs generated by the methodology previously presented guarantee the minimum voltage ripple, among other techniques, on the flying capacitor independently of the value considered for power faction angle and modulation index, as shown in Figure 172 (a) and Figure 172 (b). The FCPWM technique (dashed yellow) stands out for 0 º < *PFA* < 40º and m_a = 0.9428, while it has the same values for the DPWM 3 for higher values of *PFA*. On the other hand, it is superior for 0.4 < m_a < 0.9 and PFA 36.67 º, while the ripple is very close for the DPWM2 techniques for lower m_a values.



(a) *(b)*

Figure 172 - Maximum flying capacitor voltage ripple in mV.F for different PWM techniques: (a) 0 < PFA <90 and fixed m_a = 0.9428; (b) 0.1 < m_a < 0.9428 and fixed PFA = 36.67 º. Both with f_{sw} = 40 kHz and f_{lf} = 240 Hz.

The same conditions were employed to verify the output inductor's peak current, as shown in Figure 173, for L = 30 µH.



a) *b)*

Figure 173 - Output inductors peak current in A for L = 30 µH and different PWM techniques: (a) 0 < PFA <90 and fixed m_a = 0.9428; (b) 0.1 < m_a < 0.9428 and fixed PFA = 36.67 º. Both with f_{sw} = 40 kHz and f_{lf} = 240 Hz.

The ILPWM (orange dashed) also presented the lowest peak current values, especially for *PFA* different values. On the other hand, it presents similar results to DPWM2 for 0.6 < m_a < 0.8. It is worth pointing out that these results are related to the combination (*PFA*, m_a), and for each pair of values, a new CMO is generated. Nevertheless, the CMO may resemble some existing technique if, by chance, that technique presents the smallest voltage ripple and current output inductors peak current.

Theoretically, it was verified in this section that the optimal CMO generated by the proposed algorithm optimizes the variables of interest, even if the CMO is of an existing technique. The innovative character of the proposal of a PWM technique to reduce flying capacitors voltage ripple stands out. Then the following section will present one experimental investigation to evaluate this technique (FCPWM) compared to the traditional techniques.

4.3 Experimental Investigation: FCPWM

The experimental investigation intends to confirm that the algorithm presented in the preceding section generates the CMO that develops the lowest voltage ripple in the flying capacitors. Therefore, the FCPWM is compared with different traditional techniques: SPWM, DPWMMIN, DPWMMAX, SVPWM, and DPWM (0, 1, 2, and 3). Different *PFA* and m_a are considered, then one different CMO is generated for each condition, but they are addressed as FCPWM, reinforcing the algorithm's generalization. The other interest is verifying if the simulated waveforms have the same behavior as the one predicted by the algorithm with ideal sinusoidal reference and conditions. This section also presents the influence of voltage probe placement, specifically the PCB resistance, on voltage ripple measurement.

4.3.1 Test Setup

The tests were carried out in a 6 kVA 3-phase inverter composed of one 3-level flying capacitor leg per phase, as presented in Figure 174. This converter comprises twelve 1200 V SiC C3M0016120K (16 mΩ), three paralleled film capacitors, the DC Link (120 µF), and one film capacitor of 30 µF that composes each flying capacitor.

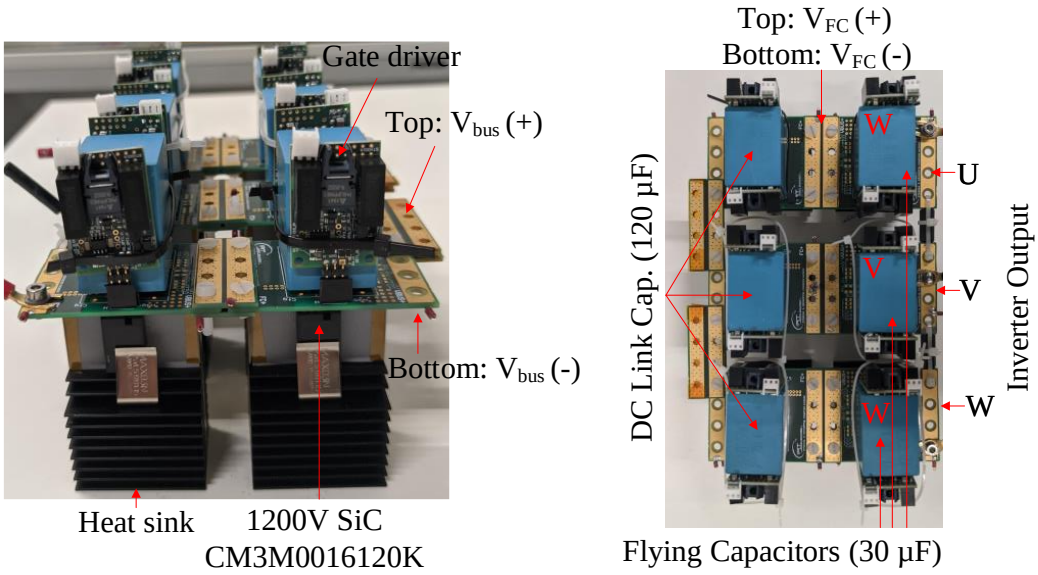
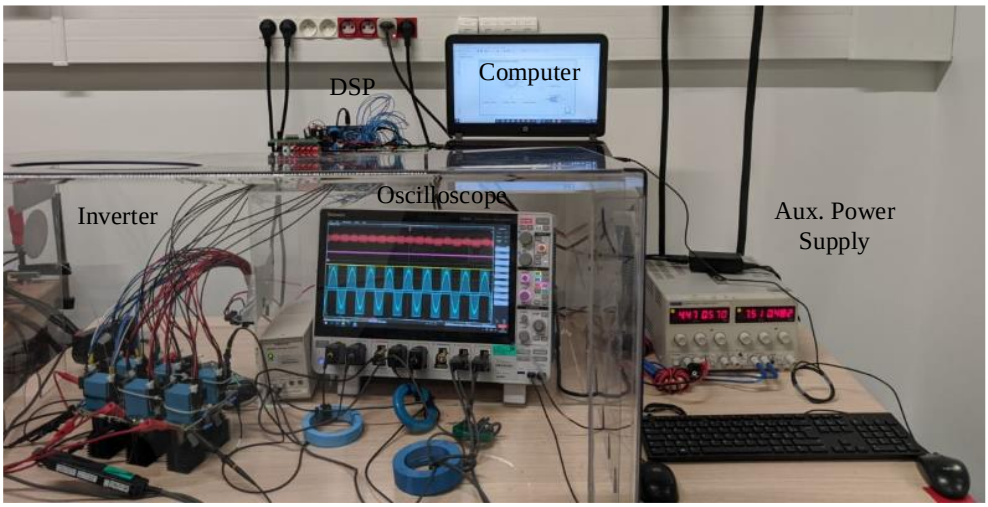


Figure 174 - 1200V SiC 3-phase inverter composed by one 3-level flying capacitor leg per phase

Gate drivers are driven optical fibers from an auxiliary board. This auxiliary board receives the signals from a DSP TMDSDOCK2837D from Texas Instruments controlled by one computer, as presented in the test setup in Figure 175. The input power supply (not presented in the figure) was configurated for a DC Link of 540 V. One variable 3-phase RL load (externally of the building) was used to control the power factor angle. Additionally, one auxiliary power supply was considered for the gate driver input voltage.



3-phase Load and DC Link power supply are connected externally

Figure 175 - PWM experimental investigation test setup.

The proper functioning of the inverter is shown in Figure 176 for phase output current ($I_{ph\text{-}U}$) of 16.16 A_{rms}. Three voltage levels are verified on the output voltage ($V_{ph\text{-}U}$) with a negligible flying capacitor unbalance. The V_{FC} ripple is presented in orange (it is not V_{FC}), in yellow $V_{bus,}$ and pink, the inverter input current (before DC-Link capacitors).

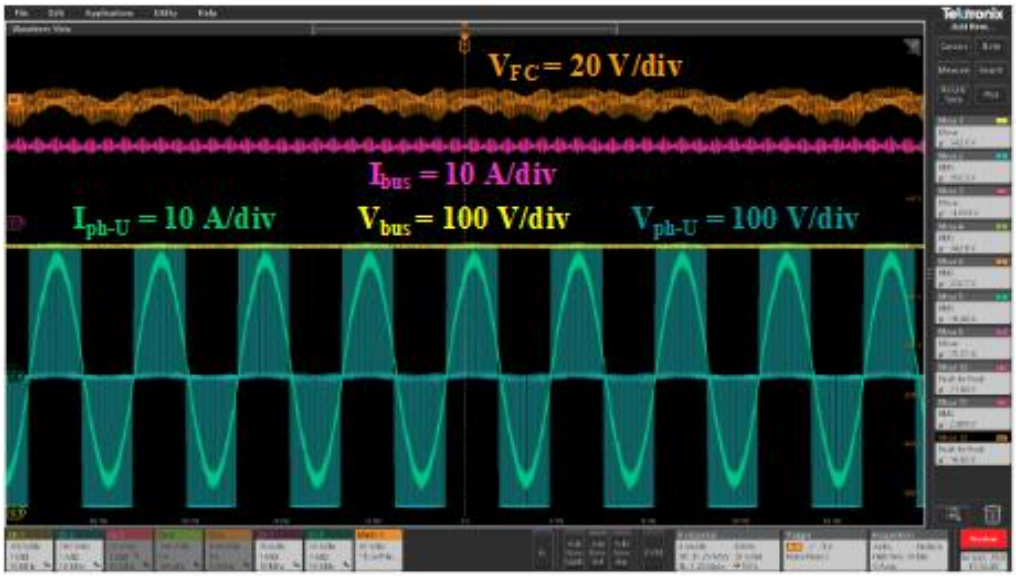


Figure 176 - Measurement seen on the oscilloscope for the phase U and following conditions: SPWM, m_a = 0.94, PFA = 0°, f_{lf} = 220 Hz, f_{sw} = 20 kHz and $I_{ph\text{-}U}$ = 16.16A_{rms}.

Flying capacitor voltage V_{FC} was measured using a differential probe (TT-SI 9101) with a bandwidth of 100 MHz, then the mean value was removed. Therefore, the orange waveform presents only the voltage ripple. For a fair comparison between the simulation and measurement, high frequencies noisy were filtered. A bandpass filter was considered with inferior and superior cutoff frequencies of f_{lf} and 2*$f_{sw.}$ Figure 177 shows flying capacitor voltage ripple with and without noise

filter. The peak value of the voltage ripple passes from almost 10 V to 5 V by removing the high frequencies components.

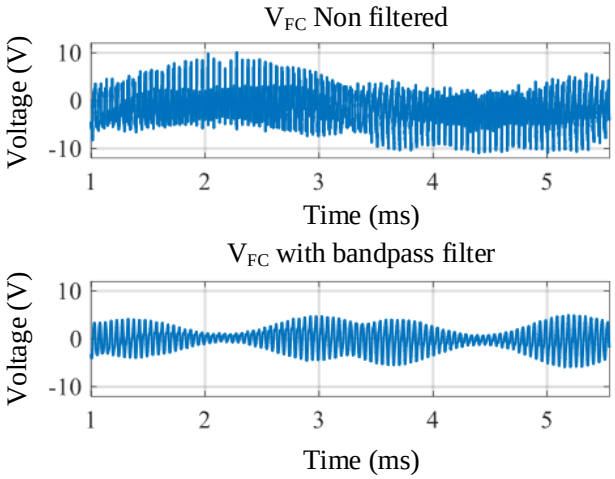


Figure 177 - Flying capacitor voltage ripple without and with noise filter

Noise can be injected in the measurements due to internal or external sources, and it can be related to the converter design, voltage probe connections, and the oscilloscope. Other phenomena may appear in the measurements, such as circuit integration, especially electrical connections. The following section presents the impact of PCB resistances due to electrical connections on the measurement carried out.

4.3.2 Influence of PCB connections on voltage ripple measurement

As discussed in the previous section, different parameters can influence the flying capacitor voltage ripple. Figure 178 presents the measured waveform of voltage ripple, in black, without the bandpass filter for some switching periods, and in red, it is presented the filtered waveform.

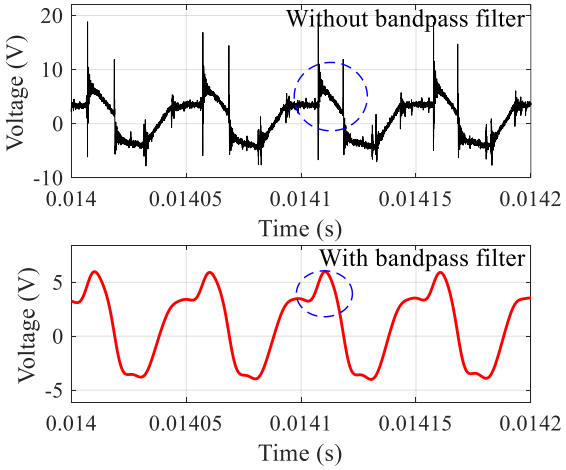


Figure 178 - Voltage spikes on flying capacitor voltage ripple measurement for the SPWM technique. In black it is shown the waveform without bandpass filter, and in red, the filtered signal.

The voltage spike, circled in blue, is verified on the voltage fall for each ripple period. In that case, the current leaves the inverter leg in the positive semicycle of the fundamental period. These spikes are also present on the filtered waveform, but this phenomenon is not expected in the ideal simulation of the circuit. The flying capacitor leg is formed by two switching cells connected by two PCBs in the form of a sandwich, as presented in the photo in Figure 179. The PCB placed on the top represents the connection between the source of S_1 and the drain of S_2 (V_{FC}(+) potential). The bottom PCB connects the source of S_3 and the drain of S_4, and it is placed on the V_{FC}(-) potential. These connections introduce some stray resistances and inductances on the inverter leg circuit. The simulation verified that the behavior verified in the measurements is mainly due to the resistive behavior, generically represented by R_{PCB} on the schematic in Figure 179. According to the probe pin connections represented in the picture, the current passing through this path will generate a voltage drop on these resistances.

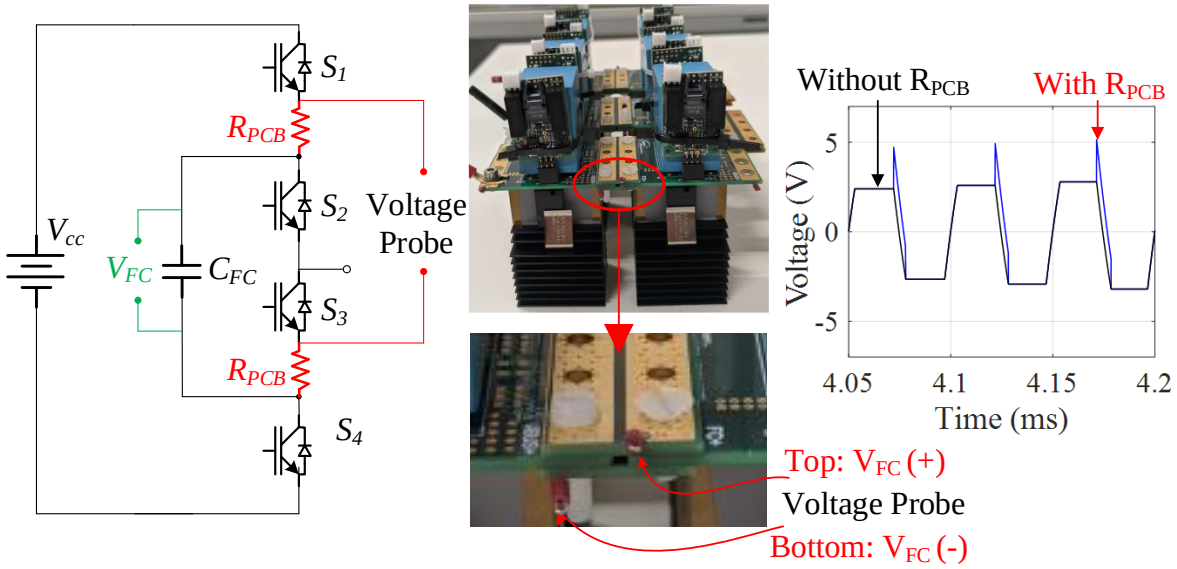


Figure 179 - Impact of contact resistances R_{PCB} on flying capacitor voltage ripple

This voltage drop due can be theoretically added to voltage ripple calculation in Equation (4.5) and verified in the blue waveform in Figure 172. It is directly related to the switched current of S1 if it is positive and with S3 if it is negative.

$$\Delta V_{FC,j} = \begin{cases} \frac{1}{C_{FC}} \int I_{FC,j}.dt - R_{PCB}.I_{S1,j}, if\ \ I_{FC,j} \geq 0, \\ \frac{1}{C_{FC}} \int I_{FC,j}.dt - R_{PCB}.I_{S3,j}, if\ \ I_{FC,j} < 0. \end{cases} \quad (4.5)$$

The value R_{PCB} is dependent on the converter integration, as it is distributed on the equivalent circuit. Therefore it is not easy to estimate it or measure it. This section aimed to identify the cause of voltage drop phenomena and consider it on the theoretical calculation for a more fair comparison between the measured and calculated voltage ripple. For the simulated results presented in the following section, an R_{PCB} of 50 mΩ was considered since it gave a good approximation to the measurements. The

impact of considering R_{PCB} in the simulation can lead to an increase of at least 5% on the voltage ripple estimation.

4.3.3 Measurements results

This section presents the measured results of the flying capacitor voltage ripple, and it is confronted with the simulation. As explained in the previous sections, a bandpass filter was considered for the measured waveforms. The effect of contact resistances was implemented on the simulation to a more close comparison between results. One of the objectives is to verify the waveform correspondence, verified in Figure 180 for SPWM, SVPWM, and FCPWM techniques.

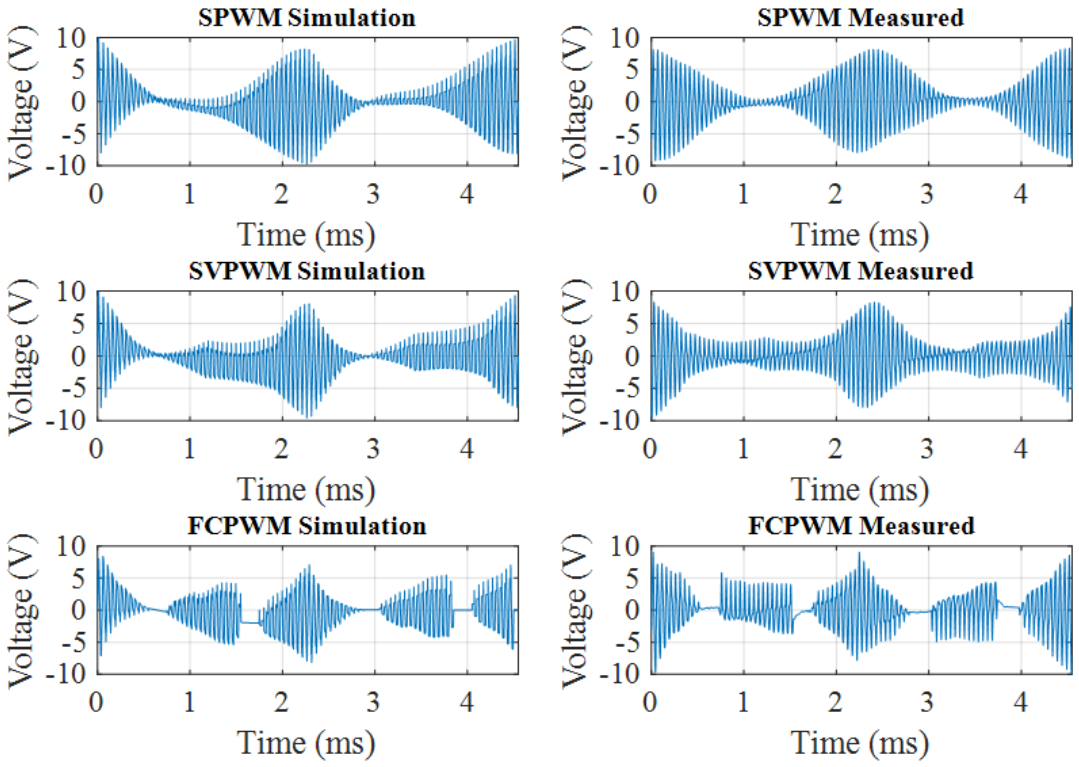


Figure 180 - Flying capacitor voltage ripple waveform comparison between simulation and measurement for SPWM, SVPWM, and FCPWM techniques. The tests were carried out for m_a = 0.94, f_{lf} = 220 Hz, f_{sw} = 20 kHz, PFA = 0º, V_{bus} = 540 V and I_{PH} = 16.16 A_{rms}.

The other objective was to compare the maximum voltage ripple. Figure 181 shows the maximum values for the FCPWM technique and different values of *PFA* and m_a. Good correspondence is verified between measured (orange) and simulated (blue) voltage ripple with a maximum error of 16.8 % for 52º and m_a = 0.94. At this condition, the measured voltage reached around 15 V, and the simulated 12.5 V. On the other hand, the minimum error of 7.1% is verified for 0º and m_a = 0.94, when the measured and simulated voltage reached 9.8 V and 9.1 V. For the *PFA* = 30º, that is the closest condition for the application described in Chapter 2, this difference is around 8.7%. Due to load power limitation, the tests for *PFA* = 30º were carried out with V_{bus} = 400 V, f_{lf} = 60 Hz, and I_{PH} = 15.76 A_{rms}.

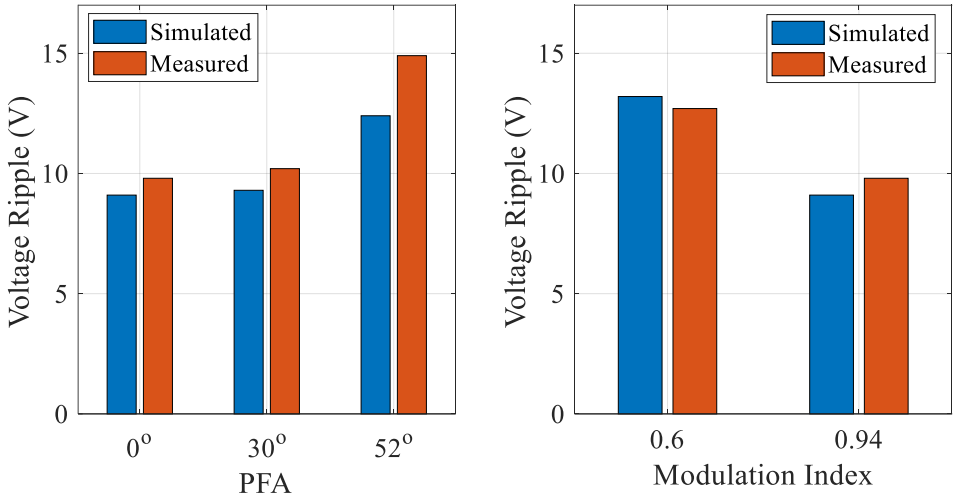


Figure 181 - Flying capacitor voltage ripple for FCPWM techniques, different PFA (m_a = 0.94) and m_a (PFA = 0°).

According to Figure 181 b), low m_a suggests a higher voltage ripple, which can be explained considering switches states. The high the m_a, the switches S_1 and S_2 (Figure 179) will conduct together (S_1 ON/S_2 ON) more time and provide output current from DC link if the current is positive (the same reasoning is applied for S_3 and S_4 if the current is negative). At this condition, the flying capacitor current is 0 A. The low the modulation index, the period that switches S_1 and S_2 conduct together reduces. Then, to guarantee output current level, the time that the current passes through the flying capacitor increases (S_1 ON/S_2 OFF and S_1 OFF/S_2 ON) as presented in Figure 182. It increases the flying capacitor *RMS* current and current integral, which increases voltage ripple for the same output current.

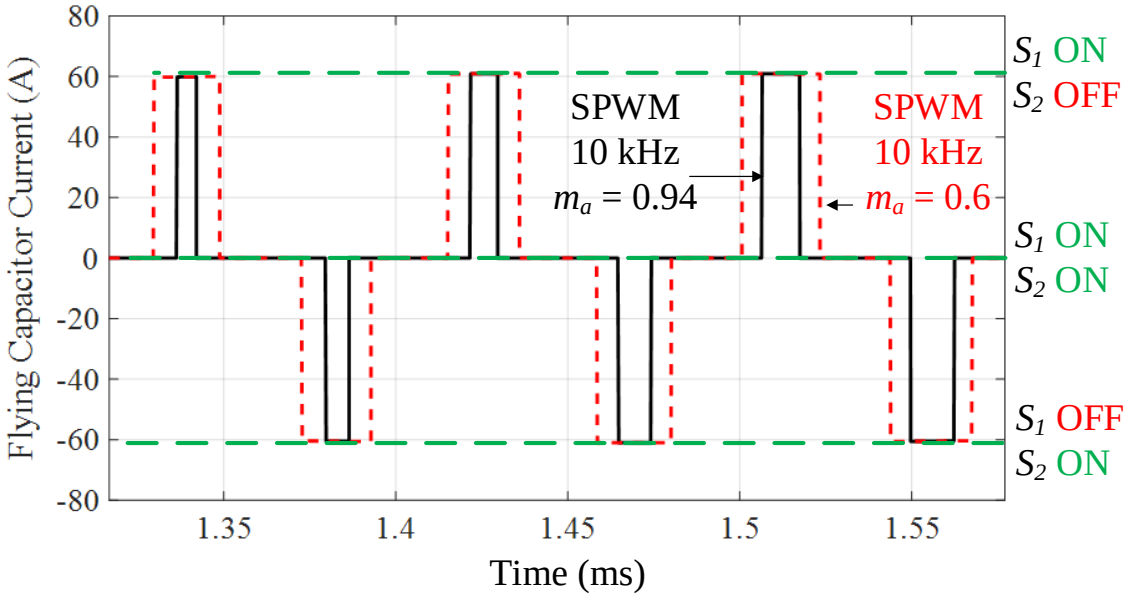


Figure 182 - Flying capacitor currenton a three-level topology for SPWM technique, f_{sw}= 10 kHz, PFA = 36.67°, I_{ph} = 60 A and V_{bus}= 540 V.

The flying capacitor voltage ripple comparison between different PWM techniques and different *PFA* is presented in Figure 183. This figure confirms that the FCPWM technique develops the smallest voltage ripple among the others. It represents an 8.7% voltage ripple reduction compared to SPWM for *PFA* = 0º, and 16.4% for *PFA* = 30º. SVPWM technique develops almost the same voltage ripple as FCPWM for *PFA* = 0º, with a 2% difference. On the other hand, for this same condition, the biggest difference to FCPWM is 37.4% compared to DPWM0.

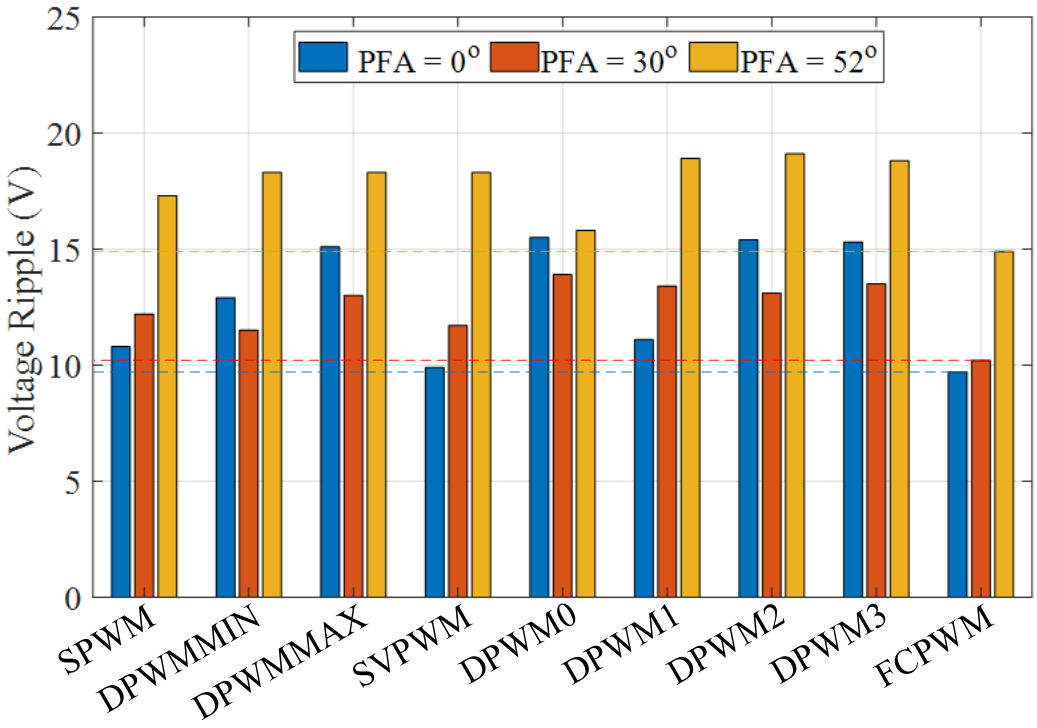


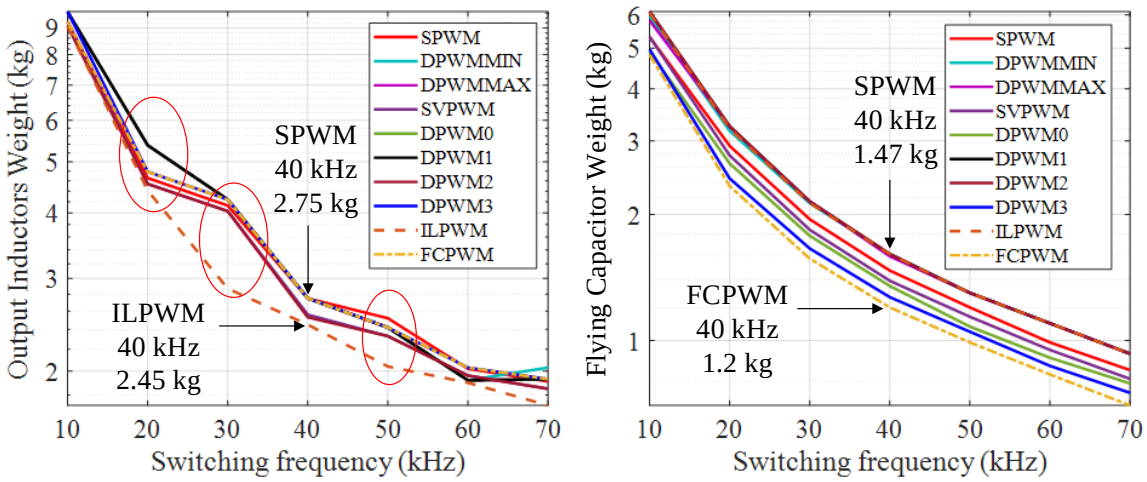
Figure 183 - Flying capacitor voltage ripple measurements for different PWM techniques and PFA (m_a = 0.94, flf = 220 Hz, fsw = 20 kHz, V_{dc} = 540 V and I_{PH} = 16.16 Arms).

For *PFA* = 30º, DPWM0 also presents the highest value of voltage ripple of 13.9 V, representing a difference of 26.6% compared to FCPWM. On the other hand, DPWM2 presents the highest value for *PFA* = 52º (19.1 V), with a difference of 22% regarding FCPWM technique.

The experimental verification presented in this section showed the correspondences between simulated and measured flying capacitor voltage ripple and the impact of PCB parasitic resistances on voltage measurement. Additionally, experimentally verified that the FCPWM technique develops the lowest flying capacitor voltage compared to the traditional techniques. These results corroborate the effectiveness of the methodology to calculate the optimal CMO to reduce flying capacitor voltage ripple. The following section will present the impact of different PWM techniques, including the FCPWM and the ILPWM, on the weight and losses of the inverter proposed in Chapter 2. The technique that presents the best compromise of gravimetric power density and efficiency will be chosen for the final inverter design is in Chapter 5.

4.4 Impact of PWM techniques on inverter weight and loss

The optimal techniques proposed in the previous section reduces the inductor's output peak current (ILPWM) and flying capacitor voltage ripple (FCPWM) compared to the traditional techniques. Figure 184 shows the impact of each technique on output inductors and flying capacitor weight for the nine legs of the 7-level inverter proposed in Chapter 2. A current ripple of 60% was considered for the output inductors, designed considering the procedure used in Section 2.9.3.3. It is worth pointing out that the inductance value does not change with the PWM technique for the same f_{sw}. Then, the difference is due to the inductor design, more specifically, the peak current. On the other hand, a voltage ripple of 5% was considered for flying capacitors, designed considering the procedure presented in Section 2.8.1.1. For both phenomena, the optimal PWM techniques present the lightest solutions.



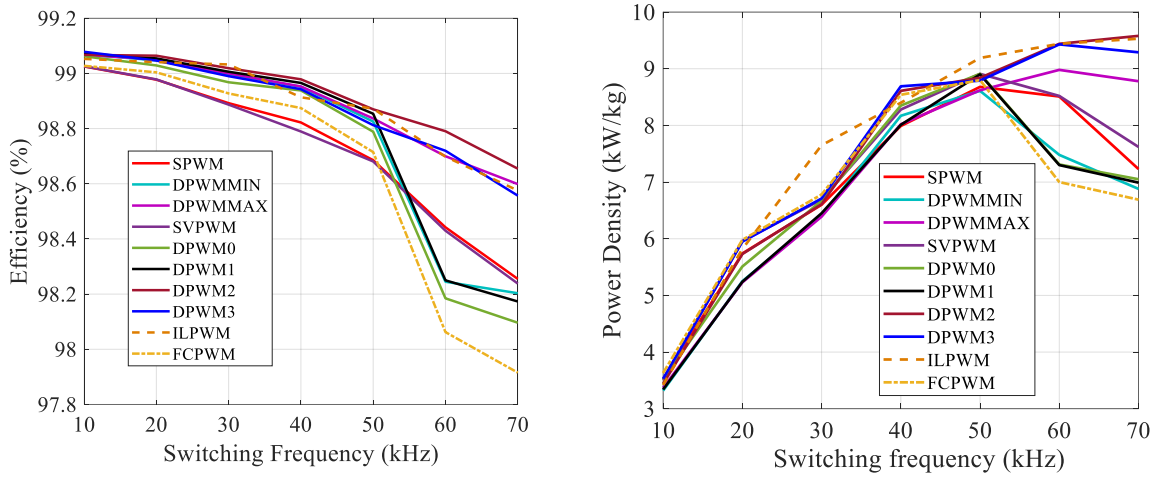
(a) *(b)*

Figure 184 - Weight of (a) output inductors (60% current ripple - I_{pk} = 60 A) and (b) flying capacitor (5% voltage ripple – V_{FC} = 270 V) of the 7-level inverter topology proposed in Chapter 2. Simulation considered f_{sw}= 40 kHz, m_a = 0.9428 and PFA = 36.67º.

In the case of output inductors in Figure 184 (a), ILPWM (2.45 kg) is 11% lighter than SPWM (2.75 kg) at 40 kHz, and 3% lighter than DPWM2 (2.56 kg) and SVPWM (2.56 kg). The differences highlighted inside the red ellipses (20 kHz, 30 kHz, and 40kHz) are due to the inductor design algorithm. This algorithm assumed that the magnetic core weight would always be much higher than the winding weight. The lightest solution considers the lightest magnetic core, not the weight of core + windings. This hypothesis can oversize inductors weight in the case where the winding is heavier than the core. Regarding flying capacitors weight in Figure 184 (b), FCPWM (1.2 kg) is 18.4% lighter than SPWM (1.47 kg) at 40 kHz, 5.5% lighter than DPWM3 (1.27 kg) and 30% lighter than DPWM2 (1.61 kg).

PWM techniques impact the entire system weight, and gravimetric power density is presented in Figure 185. It considers the different parts which compose the filter proposed 7-level inverter proposed in Chapter 2. The EMI filters (CM Input and Output) design considered the model proposed in Section 3.1 of this chapter for the multilevel topology. According to Figure 185 (a), DPWM2 presented the highest efficiency from 10 kHz to 70 kHz, reaching 98.97% at 40 kHz. At this frequency,

DPWM techniques present relatively similar efficiencies (between 98.93% – 98.97%). However, they start to differ the high the switching frequency, and DPWM2 stands out with 98.65% efficiency at 70kHz.



(a) *(b)*

Figure 185 - Optimized a) efficiency and b) power density results of the 7-level inverter topology proposed in Chapter 2 for switching frequencies from 10kHz to 70kHz. Nominal power = 70kVA, V_{bus} = 540V, m_a = 0.9428 and PFA = 36.67º.

Gravimetric power density presented in Figure 185 (b) shows that DPWM3 reaches 8.99 kW/kg, the highest value at 40 kHz. DPWM2 follows it with 8.9 kW/kg and FCPWM with 8.83 kW/kg. At 30 kHz and 50 kHz, ILPWM presents the highest values due to the inductors design particularity, related to the red ellipses in Figure 184 (a). With the increase of switching frequency, DPWM3, DPWM2, and ILPWM present the highest values. At 70 kHz, DPWM2 presents 9.83 kW/kg, 34% higher than SPWM and 8.2% than DPWM3. FCPWM presents the lowest power density values for f_{sw} > 50 kHz, while ILPWM presents almost the same value as DPWM2 for f_{sw} > 60 kHz.

According to the curves presented in Figure 185, DPWM2 and DPWM3 present the best compromise between efficiency and gravimetric power density. Beyond presenting higher losses, mainly due to semiconductor losses, ILPWM and FCPWM present very close values of gravimetric power density between the two DPWM techniques. This analysis is presented in Figure 186, where it is shown that the SPWM technique respects the design constraints for 40 kHz and 50 kHz but with higher losses and weight than the other techniques. At 40 kHz, DPWM3 has 8.7 kW/kg , 700 g (8%) lighter than SPWM, and 75 g (1%) lighter than DPWM2. On the other hand, it has 4% (28 W) losses higher than the DPWM2, mainly due to output inductor losses. FCPWM presents 8.54 kW/kg, 140 g heavier than DPWM3, and 6.6% (50 W) higher losses. ILPWM presents 8.4 kW/kg, 275 g heavier than DPWM3, and 2.8% (21 W) lossier.

With the increase to 70 kHz, DPWM2 and ILPWM present the highest gravimetric power density of 9.53 kW/kg, while the lowest value concerns the FCPWM technique with 6.69 kW/kg. The difference between DPWM2 and FCPWM is around 30% (3.16 kg), and it is mainly due to cooling system weight (1.36 kg DPWM2 and 4.19 kg FCPWM). In that condition, FCPWM presents 61% (520W) higher losses than DPWM2.

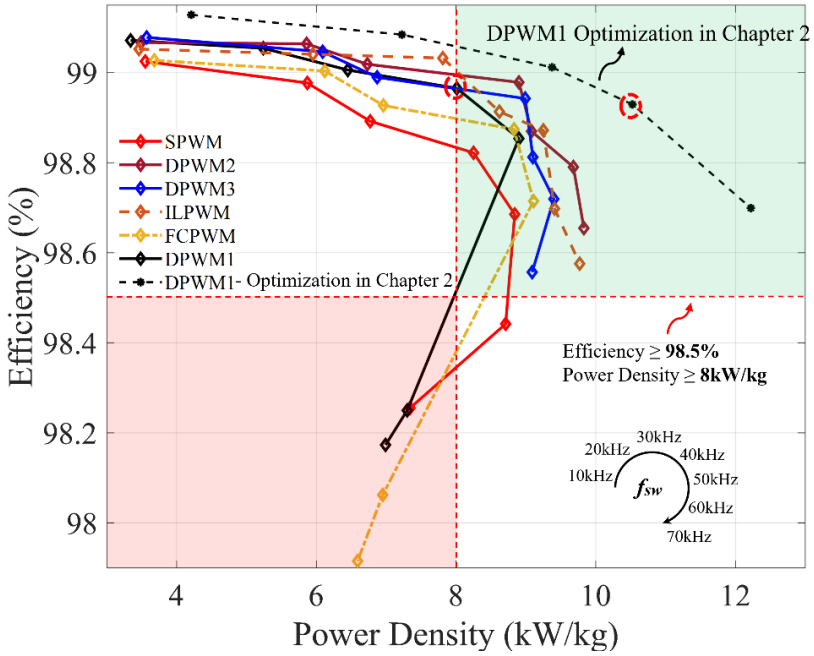


Figure 186 - Optimization results of the 7-level inverter topology proposed in Chapter 2 for switching frequencies from 10 kHz to 70 kHz. Nominal power = 70 kVA, V_{bus} = 540 V, m_a = 0.9428 and PFA = 36.67º.

It is also presented that the improvements of CM filter design and the consideration of current ripple on the output inductors have a very strong impact on the design, specially this last one. This is exemplified by the DPWM1 results of Chapter 2 (dashed black curve) and the results for the same techniques but with improved models (black curve). The models improvements lead an increase of 22% on inverter weight at 40kHz. To conclude, DPWM3 and DPWM2 have similar results at 40 kHz, the selected frequency in Chapter 2. Despite the proposition of the ILPWM and FCPWM, with exciting results, the fact that the optimized CMO depends on the operating point and the need to implement lookup tables on DSP it is costly. Therefore, considering the results presented for different PWM techniques, the DPWM3 was chosen to design the final converter at 40 kHz due to its simplicity of implementation and the highest gravimetric power density.

The pie charts in Figure 187 show the overall distribution of weight and losses for the 7-level inverter topology at 40 kHz. It presents the results of the DPWM3 technique considering the EMI model proposed in this chapter to design a CM Input/Output filter. It considers the current ripple superposed on the fundamental component to design output inductors to parallel the legs of the same phase. This figure also shows the results presented in Chapter 2 for 40 kHz. The improvements on the models, the use of DPWM3, and using the comparison established between the results presented in Chapter 2, it is noticed:

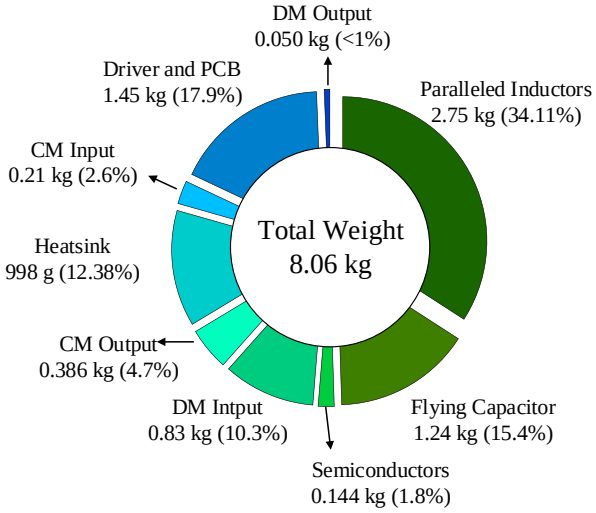
- Increase of 22% (1.460 kg) on global weight;
- Reduction of 2.2% (17 W) on global losses and 1.2% on cooling system weight.
- Decrease of 38% (380 g) on flying capacitor weight. Passing from 24.5% to 15.4% of global weight;

- Increase of 87% (1.28 kg) on output inductors weight. They are passing from 22.3% to 34.1% of the global weight. In contrast, the losses reduced from 29.8 W to 26.3 W.

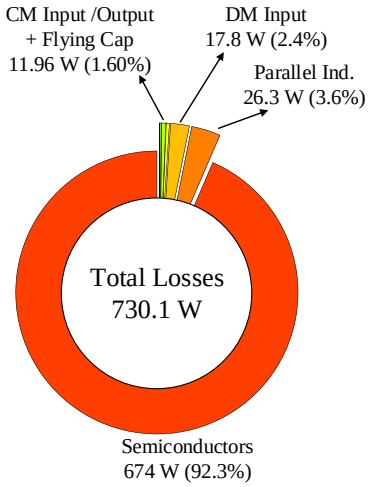
- Increase of 50% (200 g) on CM Input/Output filter weight. CM input filter remained almost unchanged, while CM output filter increased 153%.

- Increase of 56.5% (524 g) on PCB weight due to the increase of output inductors weight;

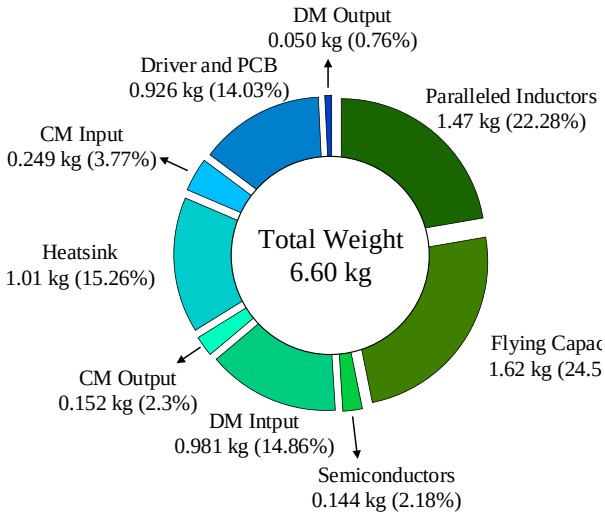
- Decrease of 15.4% on DM input filter weight. In contrast, its losses increase by 12.6%.



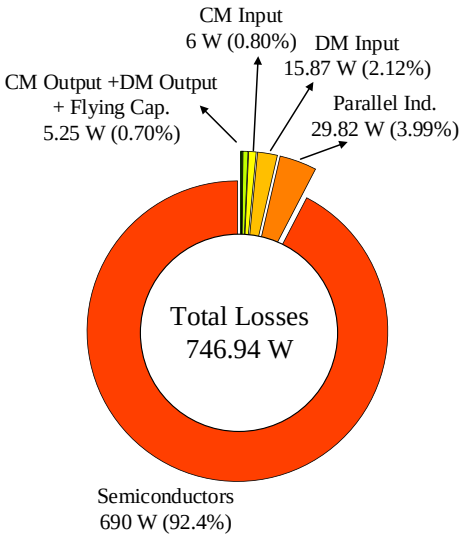
(a) Weight distribution– DPWM3



(b) Losses distribution– DPWM3



(c) Weight distribution – DPWM1 – Chapter 2



(d) Losses distribution– DPWM1 – Chapter 2

Figure 187 - Weight and Loss distribution for 7-level inverter proposed in Chapter 2. Nominal power = 70kVA, V_{bus} = 540V, and f_{sw} = 40 kHz.

The optimization procedure increased the weight of the converter proposed in Chapter 2 by 22%, considering the DPWM3 technique, which presents the highest gravimetric power density at 40 kHz for the present application. This weight increase is mainly due to the increase of output inductors weight. The leading cause of this increase is using the current ripple superposed on the fundamental component to design output inductors. It increases the inductor peak current, so there is an increase in the weight of the core for the same inductance. The increase of 50% on the CM Input/Output filters weight points out the impact of considering the coupled model proposed in Chapter 3 for multilevel topologies. The output results for DPWM3 at 40 kHz, such as magnetic cores and capacitors part number that composes the different filters, will be presented on the final converter realization presented in Chapter 4.

4.5 Chapter Conclusions

The second axis proposed in Chapter 2 was to evaluate different PWM techniques to increase inverter overall power density and efficiency. This subject was addressed in the present chapter. One methodology to find the optimal common-mode offset (CMO) was described to reduce flying capacitors and output inductors weight. These techniques were named FCPWM and ILPWM and guaranteed the minimum flying capacitor voltage ripple and output inductors peak current compared to different PWM techniques for different modulation index and power factors.

The experimental investigation presented in this section verified the correspondences between simulated and measured flying capacitor voltage ripple and the impact of PCB parasitic resistances on voltage ripple measurement. These results corroborate the efficacy of the methodology to calculate the optimal CMO to reduce flying capacitor voltage ripple. The proposal of these two techniques and the experimental verification comprise another contribution of this thesis. The applied methodology was used to reduce flying capacitor voltage ripple and inductors weight based on its current peak value. FCPWM reduced 18.4% flying capacitors weight for the present application, while ILPWM reduced 11.8% of the output inductors weight, both compared to the SPWM at 40 kHz. No other works were found in the literature regarding these topics, except the one proposing this methodology to reduce the magnetic flux of coupled inductors [235].

The final part of this section presented the impact of different PWM techniques, including the proposed FCPWM and ILPWM, on inverter overall weight and losses. The design procedures and conditions were the same as those considered in Chapter 2, except for the EMI model that used the proposed coupled model described in Section 3.1. Additionally, the current ripple superposed on the fundamental component was considered for the design of output inductors. It increases the inductor peak current, so there is an increase in the weight of the core for the same inductance. DPWM3 technique presented the highest gravimetric power density among the different techniques (8.99 kW/kg) at 40 kHz and DPWM2 (9.53 kW/kg) at 70 kHz. The use of the EMI model proposed in Chapter 3 for the design of CM input and output filters, and the impact of current ripple on the design of output inductors, led to an increased of 22% on inverter global weight compared to the one presented in Chapter 2. Despite the good results of FCPWM and ILPWM, the fact that the optimized CMO depends on the operating point, the need to implement lookup tables on DSP is costly.

A work developed in parallel at IRT Saint Exupery used the models presented in this thesis on an internal computational platform using multidisciplinary design optimization (MDO) [239], [240]. The MDO is defined as a field of using numerical optimization to design systems composed of multiple disciplines. The most significant advantage of using the MDO is considering the coupling between the different models in the global optimization, such as the contribution of the dispersion inductance of the CM chokes in the DM filters, which was not considered in the optimization of this thesis. In this context, the same converter presented in the section was optimized using MDO for the same conditions (only the filters were considered). A difference of 10% was observed between the mass calculated in Section 4.4 and using the MDO, up to 40 kHz, while that difference goes to 3.6% up to 30 kHz. The calculation time was around 1.6 hours for the methodology considered in this thesis (uncoupled models and parameter variation) and 2.5 hours for the calculation using the MDO (surrogate and coupled models).

The improvement on the models presented in Chapter 4 leads to an increase of 22% on inverter weight (DPWM3 at 40 kHz) and reduced 2% on inverter losses compared to the one presented in Chapter 2. The realization of the 7-level inverter with the filter design results presented in this chapter for DPWM3 at 40 kHz will be addressed in Chapter 5.

CHAPTER 5

Multilevel Power Inverter Design and Experimental Results

THIS chapter presents the GaN-based 7–level inverter resulting from the optimization presented in Chapter 3. Different filters and PCBs that compose the entire inverter will be presented. This topology comprises nine cells of 3–level flying capacitor leg with 4 paralleled GaN HEMTs per switch, which means three legs in parallel per phase. The routing and specification of the 3–level leg will be addressed in detail given the challenges of parallel connection of GaNs and the composition in a series multilevel switching cell. This chapter also presents the experimental results regarding the switching cell and the entire inverter.

Summary

5.1 Multilevel Inverter Design

The 7-level inverter prototype is composed of 14 PCBs (9 FC legs, 1 Motherboard, 1 Input filter, 1 Output filter, 1 Control board and 1 Fans board), and it is shown in Figure 188. The input and output filters are located in boards under the Mother board, which handles the nine inverter legs (FC Leg) and paralleled inductors. On vertical, the Fans board is placed under of the Control board, and a metallic base is considered to structure and facilitate handling.

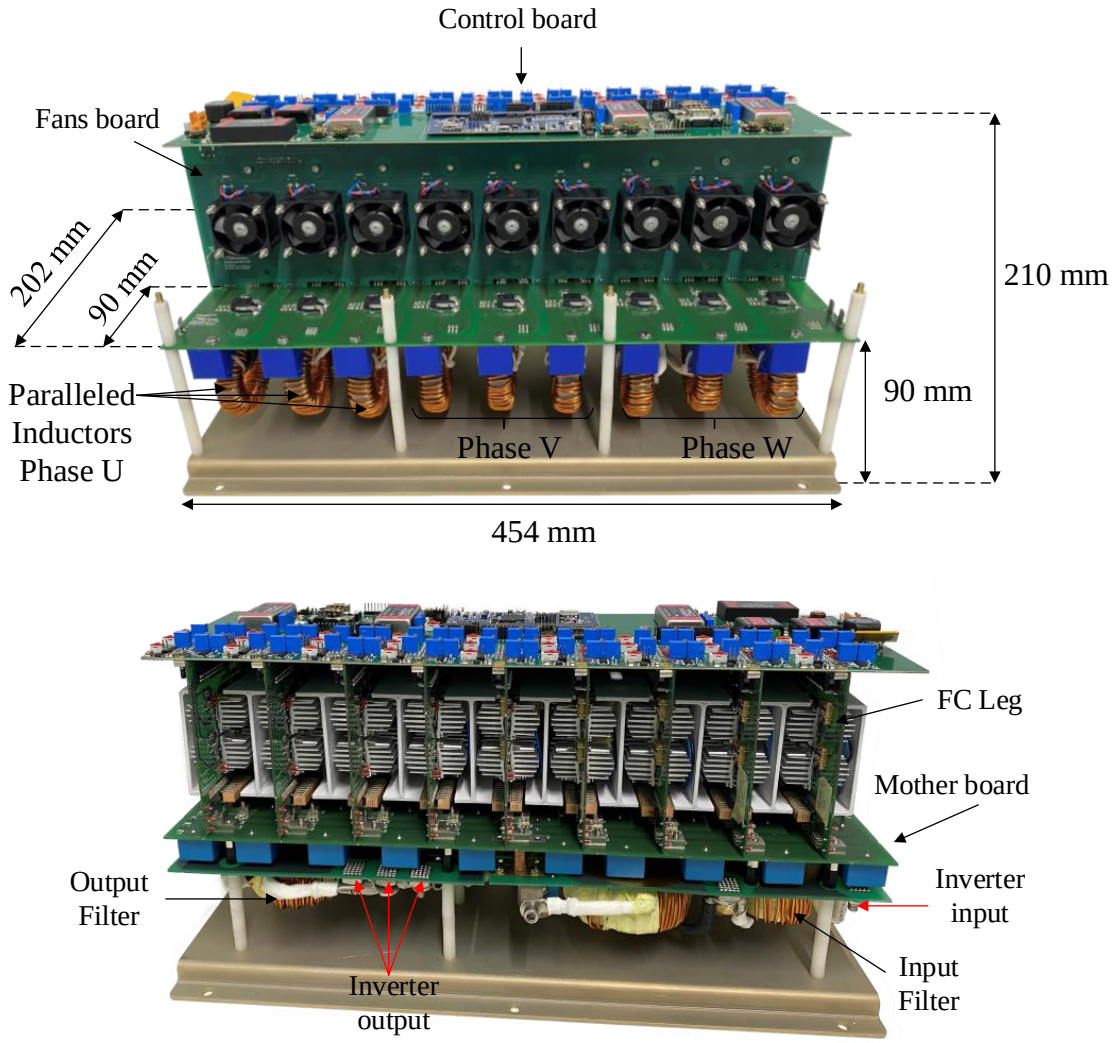


Figure 188 – 7-level inverter prototype.

The prototype presents around 14 liters and 10.04 kg (6.97 kW/kg). Without the metallic base, the inverter has 8.96 kg while the Control board has 610 g. Both metallic base and Control board were not considered during the optimization in Chapter 2 and Chapter 4. Therefore, the inverter without these two parts has 8.35 kg (8.38 kW/kg), which is less than 4% heavier than the solution proposed shown in Figure 187 (a) in Chapter 4. It corroborates the precision of models used in the optimization procedure.

For comparison purpose, Figure 189 shows a 2-level inverter considering three 1200 V SiC modules HT3201RVB designed at the EpowerDrive project, for the same application as the 7-level GaN-based inverter. Without any filters, this converter has 6.06 kg. Assuming that all filters represent around 66% of inverter total weight (based on the optimization results in Chapter 2), it leads to a final inverter with 17.8 kg or 3.9 kW/kg at 40 kHz. Therefore, 74% heavier than the entire 7-level inverter, or with a power density 43.4% smaller than the multilevel topology.

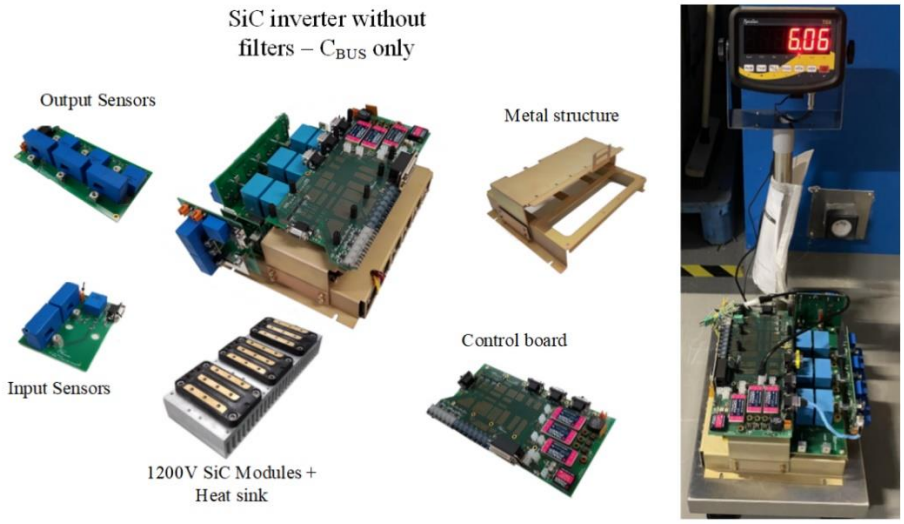


Figure 189 – 2 - level inverter weight with the 1200V SiC Module HT3201RVB without filters.

The Control board is presented in Figure 190, and its dimensions are 134 mm x 454 mm. This board is fed by 28 V (orange connection on the left side of the board) and generates 24 V for the fans, 12 V for the isolated power supplies on FC legs, and 5 V for the auxiliary electronics. The inverter control is performed using the DSP F28379D, which operates 18 PWM output pins and ADC (Analog-to-Digital Converter) input pins that receive measurements signals of input voltage, flying capacitor voltages and paralleled leg current.

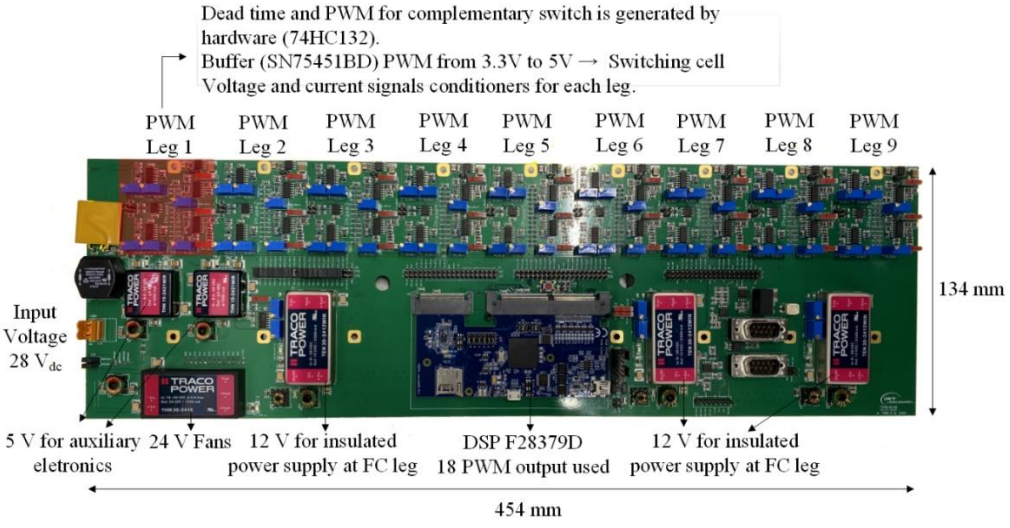


Figure 190 – 7-level inverter: Control board

Each inverter leg is composed of four switches, then a total of 36 PWM signals are required for the entire inverter: 18 independent signals, and 18 signals for the complementary switches. Due to the number of PWM signals, the deadtime and the complementary PWM signals were generated by hardware using the 74HC132 (quad 2-input NAND gate with Schmitt-trigger inputs – similar to the circuit considered in the GS665MB-EVB evaluation board from GaN Systems). PWM signals were converted from 3.3 V (DSP output pin) to 5 V through a buffer (SN75451BD) to be sent to the FC legs. These PWM circuitries are presented in the red region in Figure 190.

The Fan board is shown in Figure 191, measuring 115 mm x 454 mm. It comprises nine fans 414 JH (one for each leg) and air guide pieces made in a 3D printer. These pieces are made by an insulating material (Acrylonitrile butadiene styrene); it guide the airflow from the fan to the corresponding leg, and it also provides an insulating layer between legs. This board receives the 24 V from Control board to feed the fans (white connector on the board top side), and it is an interface between the leg current measurement circuit from the Mother board (9 connectors on the board bottom side) and the Control board (black connector on the board top side).

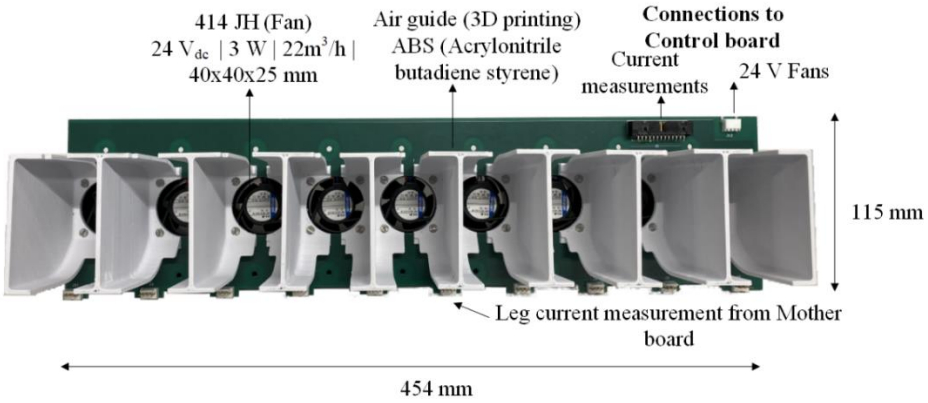


Figure 191 – 7-level inverter: Fans board.

The board shown in Figure 192 comprises DM and CM input filters and the connection between power supply V_{bus} (540 V) and the Mother board.

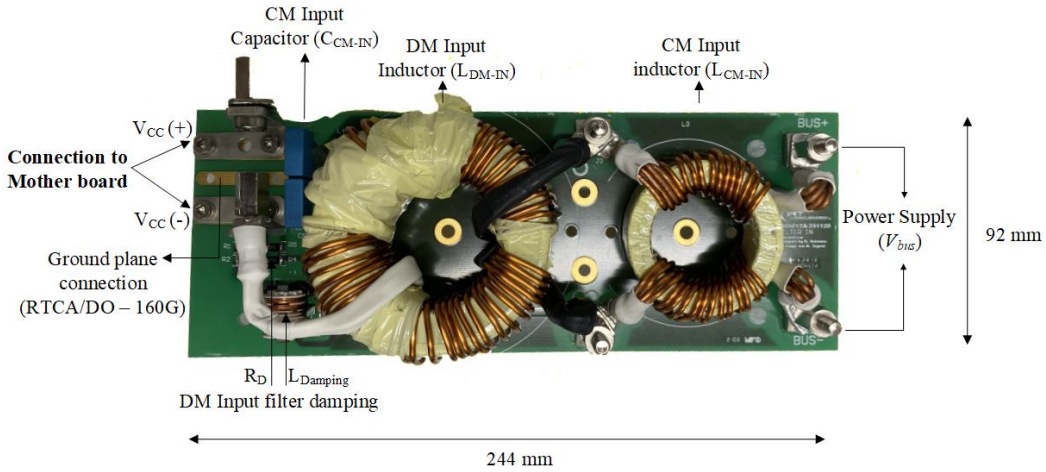


Figure 192 - 7-level inverter: Input filter board.

The circuit schematic of the Input filter board and the characteristics of each device, based on the optimization in Chapter 4, are presented in Figure 193.

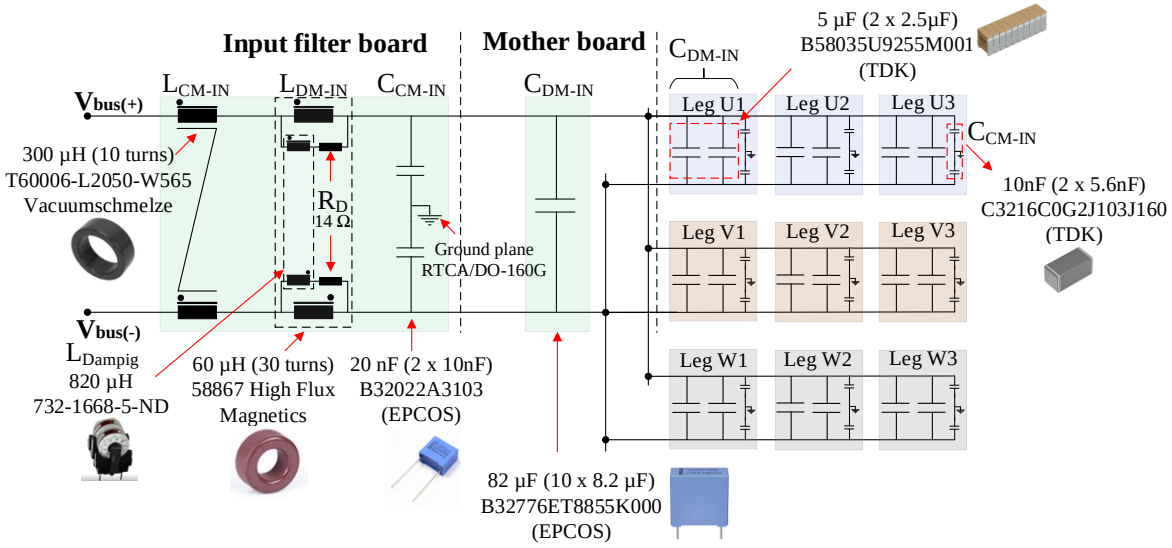


Figure 193 - 7-level inverter: Input filter and Mother board passive devices.

The Mother board is presented in Figure 194, measuring 202 mm x 454 mm. It comprises different power connections and measurement circuits.

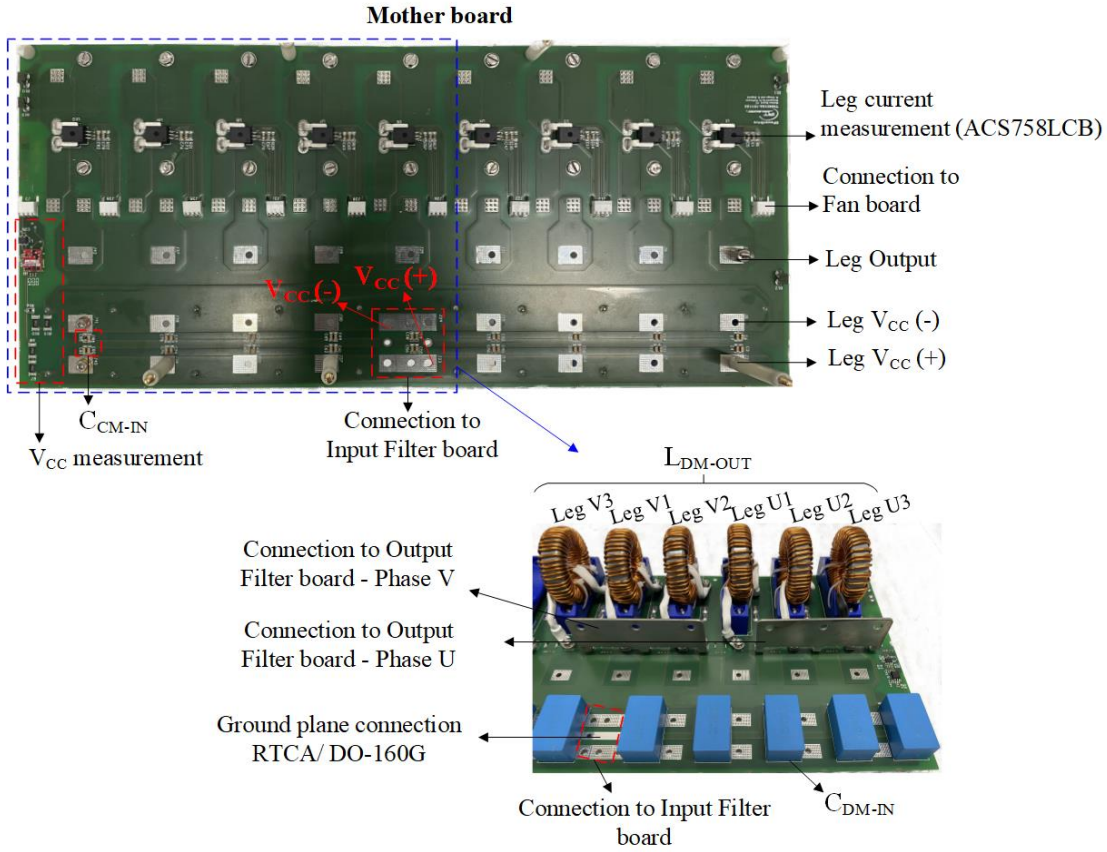


Figure 194 - 7-level inverter: Mother board.

$L_{DM\text{-}OUT}$ inductors are placed under the mother board, and they are connected 3-by-3 to a metallic plate representing the inverter output phases going to the output filter board. The passive devices considered for $L_{DM\text{-}OUT}$ and output filter, calculated by the optimization procedure, are shown in Figure 195.

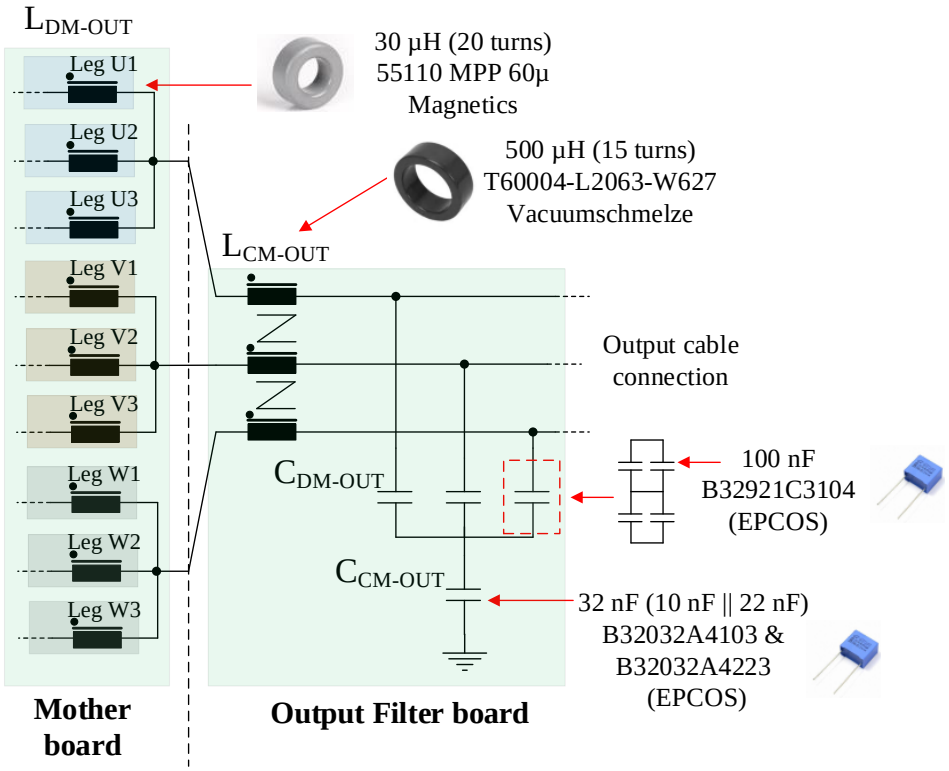


Figure 195 - 7-level inverter: Leg inductors and Output filter board passive devices.

Output filter board is shown in Figure 196, measuring 93 mm x 205 mm, with inverter output connections.

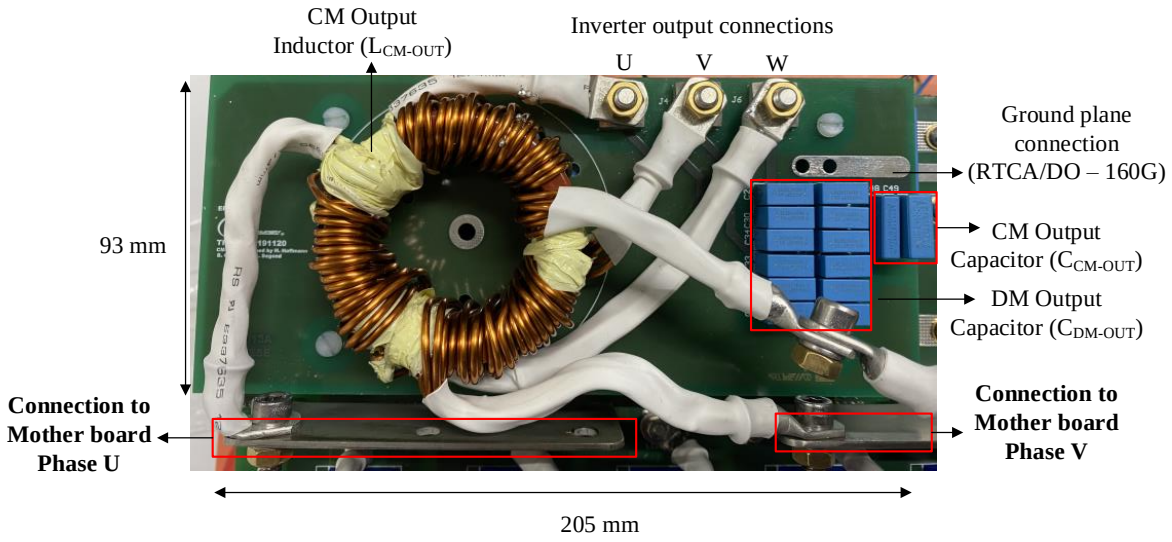


Figure 196 - 7-level inverter: Output filter board.

The 3-level FC leg is the most complex component of the entire inverter. As highlighted in the end of Chapter 2, the integration and parallel connection of GaNs in a multilevel switching cell is the third axis of this thesis. The insights referring to the optimized design of the FC leg with 4 paralleled GaNs per switch, totalizing 16 devices, are addressed in the following section based on different PCB designs, simulation, and experimental investigation.

5.1.1 Inverter flying capacitor leg design

The structure of the 3-level FC leg with four 650 V/60 A GaN HEMTs GS66516T in parallel per switch is presented in Figure 197, totalizing 16 semiconductors (Q1-Q16).

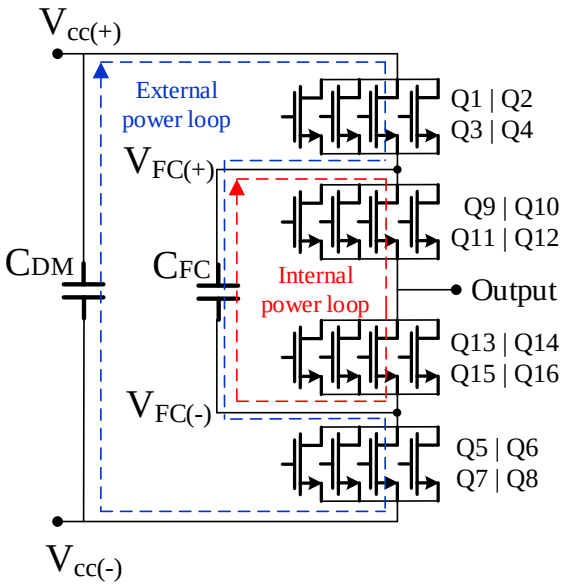


Figure 197 - Three-level FC switching cell with four 650 V/60 A GaN HEMTs (GS66516T) in parallel.

The state of the art of GaN HEMT applications presented in [241] compiles more than 162 technical reports and research papers and highlight the main advantages of GaN HEMT to Silicon-based power switches: excellent temperature capabilities allowing much higher power density (580 kW/l) and efficiency (up to 99.8%) on power converters. One of the main characteristics of Wide bandgap (WBG) semiconductors, as Silicon Carbide (SiC) MOSFETs and GaN HEMTs, is to present lower output capacitance. It implies a high switching speed of 100 V/ns for GaN HEMTs [242]. Due to high *dV/dt* and *dI/dt*, parasitic inductances of printed circuit board traces (PCB) are critical to the safe operation of GaN HEMTs, by reducing voltage spikes on the drain and source voltage, EMI noise, and switching losses [243]–[245].

Reducing commutation loop inductances is probably the most affordable solution to reduce the voltage across stray loop inductances due to high *dI/dt* [118] if packaged devices are used since it only depends on PCB routing. The challenges of paralleling four GaN HEMTs 650 V/60 A (GS66516T) are presented in [118] and [246] for a half-bridge topology. Besides power loop reduction (0.7 nH [118] and 0.81 nH [246]), gate driver loop must also be optimized (4.2 nH [118] and 2.5 nH/3.6 nH [246]) to reduce V_{GS} ringing and overshoot. An additional degree of complexity is inserted in power loop

optimization for multilevel series topologies since the power loop is defined by more than one commutation cell. In the three-level FC topology presented in Figure 197, the external power loop (in blue) is formed by all switches, C_{DM} and C_{FC}. While only inner switches (Q9 – Q16) and C_{FC} form the internal power loop (in red). The number of power loops is defined by cascading FC switching cells by the number of output voltage levels -1. The flying capacitor of the innermost commutation cell will be part of the preceding commutation cell power loop.

The use of 650 V/30 A GaN HEMTs in multilevel series topologies, with no paralleled devices, is presented in a 1 kW three-level Active Neutral Point Clamped (ANPC) [247] achieving 3.51 nH and 5.37 nH for power loops. On the other hand, FC topology is presented in [248] and [249] for a nine-level and a ten-level topology, respectively, with no paralleled devices. In order to reduce power loop inductances (2.32 nH [248] and 2.7 nH [249]), the complementary switches are oppositely placed on PCB top and bottom layers with ceramic flying capacitors placed in the input and output of each switching cell.

Among the reviewed papers, despite the parallel connection of GaN HEMTs and their use in series multilevel converters, the two issues have not been addressed together: parallel connection of GaN HEMTs in multilevel series converters. It is the main subject addressed in this section. As discussed, the key to connect parallel multiple devices is to guarantee a symmetric layout. In [118] and [246], a similar schematic for a two-level with two paralleled GaN as shown in Figure 198.

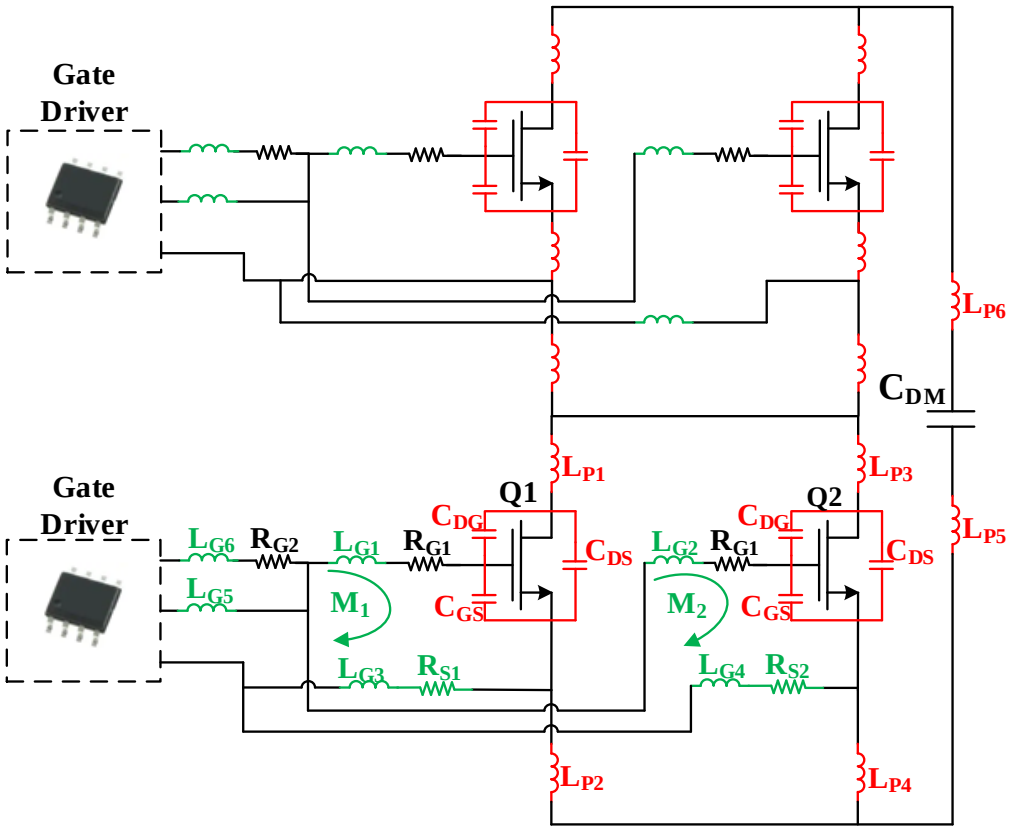


Figure 198 - Two paralleled GaN HEMTs in a two-level switching cell and their respective gate and power loop stray inductances.

Current sharing between the devices is strongly dependent on gate loop inductances, in green, L_{G1}~L_{G4}, power loop inductances L_{P1}~L_{P5} and the mutual M_1 and M_2. Connecting more devices in parallel, the same approach can be used. So, with four devices in parallel as shown in Figure 197, will double the number of parasitics elements of Figure 198 . To guarantee paralleled devices equal current sharing, the layout must consider minimizing these inductances and $L_{G1} = L_{G2}$ and $L_{G3} = L_{G4}$, as $L_{P1} = L_{P3}$, $L_{P2} = L_{P4,}$ and $L_{P5} = L_{P6}$. Next, the details of the gate and loop layout developed in this work are explored.

5.1.1.1 Gate driver design

Gate loop inductances (L_{G1}~L_{G4}) presented in Figure 198 substantially impact V_{GS} ringing and overshoot that can be increased if a strong unbalance between these loops is verified [118]. To reduce V_{GS} ringing, it is interesting to split R_{G1} between C_{iss} (input capacitance) of paralleled devices, resulting in an $R_{G\text{-}on}$ (turn-on resistance) equal to R_{G1} + R_{G2} per device. On the other hand, $R_{G\text{-}off}$ (turn-off resistance) is defined only by R_{G1}. The same idea of splitting resistors is employed with four paralleled transistors, so R_{G1} = 1 Ω is connected to each transistor in series with R_{G2} = 5 Ω for the present application. These values were used in [246], [250] and guarantee the proper functioning of four paralleled GS66516T.

In the present project, the isolated gate driver Si8271BBD-IS controls the four GaN HEMTs in parallel, totalizing four gate driver circuits for the 3-level FC leg. The gate driver circuit layout is presented in Figure 199 with four paralleled devices (two on the top layer and the other two on the bottom layer) based on the disposition proposed by [246], [250]. Turn-on gate loops were estimated using Ansys Q3D Extractor as 2.3 nH (green path in Figure 199) and 2.5 nH for top and bottom devices, respectively. On the other hand, turn-off gate loops reached 3.6 nH for both top and bottom devices (red path in Fig. 3). These gate loops symmetry and values are achieved due to decoupling capacitors placed close to each device on both the bottom and top layers (680 nF for eachtransistor), as shown in Figure 199. This capacitor split also guarantees the balance between the quasi-common-source inductance (L_{G3} and L_{G4} showed in Figure 198) discussed in [118] since the same distance between source connection of each GaN to respective decoupling is reached.

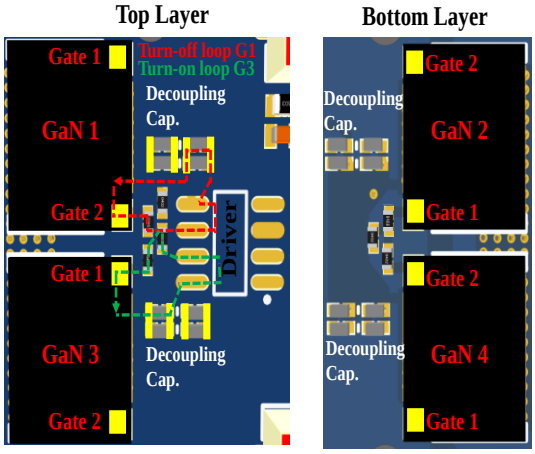


Figure 199 - Gate driver circuit responsible to drive four paralleled 650 V/60 A GaN HEMTs (GS66516T) in parallel with equivalent $R_{G\text{-}on}$ = 6 Ω (1 Ω + 5 Ω) and $R_{G\text{-}off}$ = 1 Ω per transistor. The Turn-on gate loop path of GaN 3 is presented in green, and the turn-off loop of GaN 1 is presented in red.

Another essential part of the gate driver design is the isolated power supply that will provide the 6 V (turn-on voltage) and -4 V (turn-off voltage) for each switch (four GaN HEMTs). This power supply must have an isolation parasitic capacitance as small as possible to attenuate the common-mode current passing through the gate driver to the auxiliary power supply [251]. This common-mode current can distort the output of the isolated power supply and gate driver, resulting in a risk to the integrity of the gate drive circuit and the converter itself [251]. The isolated power supply used in the project is the 2 W/12 V NXE2S1212MC from Murata, which presents only 3 pF parasitic capacitance. To regulate 12 V output voltage from the isolated power supply, two zener diodes are connected in series, TDZ6V2J (6.2 V) and TDZ3V9J (-3.9 V), with a 400 Ω resistor as presented on the gate driver circuit in Figure 200, used to design the PCB shown in Figure 199.

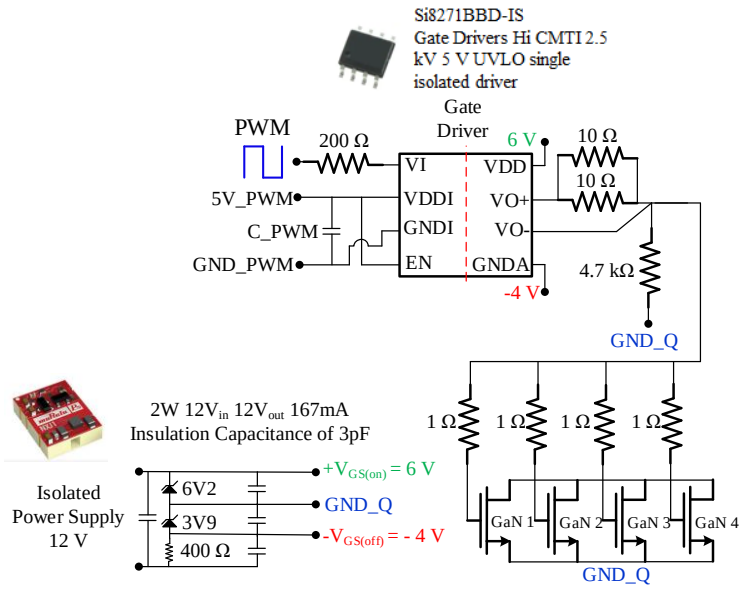


Figure 200 - Gate driver voltage circuit for four paralleled devices.

The gate driver project and routing are essentially the same as presented in [246], [250], experimentally validated for a half-bridge topology with four GS66516T in parallel. The main objective of the design of the FC switching cells in this thesis is to investigate the disposition of transistors and capacitors (C_{DM} and C_{FC}) to reduce internal and external power loops stray inductances of FC topology presented in Figure 197. This subject is addressed in the following section.

5.1.1.2 Power loop design

Reduce power loop stray inductances can be done in different ways, such as reducing the length of bus bars and supply terminals of the commutation cell or choosing capacitors with low *ESL* (equivalent series inductance). However, the most effective way is to place ceramic capacitors close to the switching cell [252]. These ceramic capacitors must have enough capacitance to provide the necessary energy lost and stored during a switching instant, almost the same as the turn-on energy [189]. In the case of the designed switching cell presented in Figure 197, in the worst case for C_{DM}, there would be eight GS66516T (Q1-Q4 and Q9-Q12 or Q5-Q8 and Q13-Q16) turning on at 270 V (half of the bus voltage: 540 V) and 15 A for each transistor, totalizing 60 A, at the same time. The total energy lost at

these conditions, according to the GS66516T datasheet, would be E_t = 8* 81 µJ = 648 µJ. In the case of C_{FC}, there would be only four devices in the worst case (Q9-Q12 or Q13-Q16), totalizing 324 µJ. The final voltage level V_f at C_{DM} (or C_{FC}) providing the energy E_t at initial voltage V_{CC} is presented by [189], as:

$$V_f = \sqrt{V_{CC}{}^2 - \frac{2 * E_t}{C_{DM\ or\ FC}}} \tag{5.1}$$

By considering the maximum accepted voltage drop ($V_{CC} - V_f$) of 1% (5.4 V) for C_{DM} and 2% (5.4 V) for C_{FC}, a minimum value of 220 nF is needed for each one. Since these capacitors will be part of the power loops, the large the contact surface of these devices with the PCB tracks, the lower the loop inductance. Then, 8*220nF (CGA8M1X7T2J224K) of them in 630 V were used for $C_{DM,}$ and 6*220 nF (C3225X7T2W224K) of 450 V were used for C_{FC}, being half on the bottom layer and the other half in the top layer to ensure symmetry between paralleled devices.

According to Figure 197, C_{FC} is part of the external power loop with C_{DM}. Therefore, C_{FC} positioning directly impacts the current high-frequency path during the commutation of Q1-Q4 and Q5-Q8. The challenge consists on placing C_{FC} as close as possible to C_{DM} to reduce the external power loop. However, it must consider a safe distance between them since they will be at different electric potentials, and it should not compromise internal power loop inductance. The proposed solution in this thesis is to split C_{FC} into two parts, based on the proposition made by [248], [253], that reduces voltage ringing during the switching in FC topologies with GaN devices. The first part is placed so the internal power loop is reduced as close as possible between Q9-Q12 and Q13-Q16 (see in fig. 198). The second part, named $C_{FC'}$ and $C_{FC''}$, is electrically in parallel with C_{FC}. However, they are placed close to C_{DM}, as presented in Figure 201, allowing the reduction of the external power loop. They will provide a preferable path during Q1-Q4 and Q5-Q8 switching regarding C_{FC}. On the other hand, since they are "electrically" far from Q9-Q12 and Q13-Q16, their contribution to the internal loop is low compared to C_{FC}.

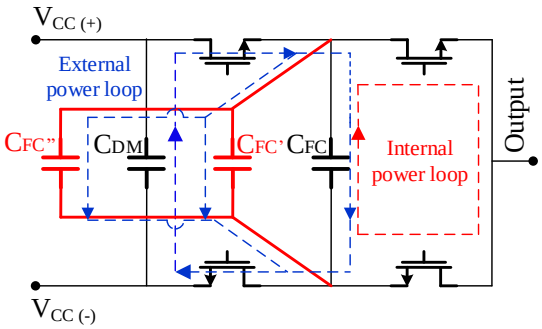


Figure 201 - $C_{FC'}$ and $C_{FC''}$ location in a 3-level FC switching cell.

Power loop reduction is directly related to device choice and position. The first approach considered that film capacitor (DC-Link and flying capacitor) and output connecors should be placed on an external PCB so that the 3-level FC switching cell works as a pluggable PCB. The interface between the switching cell and the film capacitors PCB is done by a power connector 46114-1032 from Molex with five power connections: $V_{CC(+)}$, $V_{CC(-)}$, $V_{FC(+)}$, $V_{FC(-),}$ and output connection. This connector is also used to transfer PWM signals, 12 V for the isolated power supplies and 5 V for the gate driver (non-isolated side).

Different solutions were evaluated for different positions of other devices (driver circuits, power connectors, ceramic capacitors, and the 16 GaN HEMTs) through simulations with the Ansys Q3D extractor. Two solutions were selected based on the disposition of the switching cells on the PCB, external and internal power loop inductances as other characteristics presented in Table 18, these solutions are named Vertical and Horizontal versions.

Table 18 - Three-level flying capacitor switching cell versions characteristics.

Characteristics	*Vertical Version*	*Horizontal Version*
External Power Loop Inductance	6.4nH	4.4nH
Internal Power Loop Inductance	5.7nH	3.6nH
Dimensions	112mm x 94mm	132mm x 103mm
Number of layers	6	8
Power direction	Vertical	Horizontal
Gate Signal	Shielded	Shielded
Symmetry	Symmetric	Asymmetric
Higher output levels	Difficult	Easy
Signal and Power	Separated	Mixed

Both solutions present positive and negative points that can be used to justify using one over the other. Besides the differences of loop inductances, dimensions, and the number of layers, three other characteristics must be pointed out:

1) Symmetry: This characteristic implies that the high-frequency current path for both top and bottom paralleled devices are identical. This characteristic may suggest that all paralleled devices will see the same impedance and switch with the same characteristics.

2) Increase the number of output voltage levels. Despite the objective of a 3-level FC switching cell, there is the interest of a PCB routing that can be generalized so that FC cells can be easily cascaded in series to increase the number of output voltage levels of the converter.

3) Signal and Power paths: Separate signal and power tracks is a good design rule for PCBs. It prevents noise propagation on signal tracks that can disrupt proper circuit operation. Typically, the circuit is divided into regions with only signals and other regions for high current circulation.

The Vertical version shown in Figure 202 is formed by six layers (70 µm copper thickness), and the power flow between the external and internal cells is vertical. Signals tracks (green arrows) are placed on the borders of the PCB, while power (yellow arrows) remains in the center. Half of all devices are placed on each PCB layer (bottom or top) and measurement points were placed close to the power connector to evaluate switching cell performance. External power loop inductance (represented in red) was estimated by simulation as 6.4 nH with $C_{FC'}$ (0.9 µF) and 10.8 nH without $C_{FC'}$. It consists of a 40.7% reduction of loop inductance. On the other hand, the internal power loop achieved 5.7 nH with

$C_{FC'}$ and 5.8 nH without it. These results confirm that splitting ceramic flying capacitors can significantly reduce external power loop inductance and has a minor impact on the internal power loop.

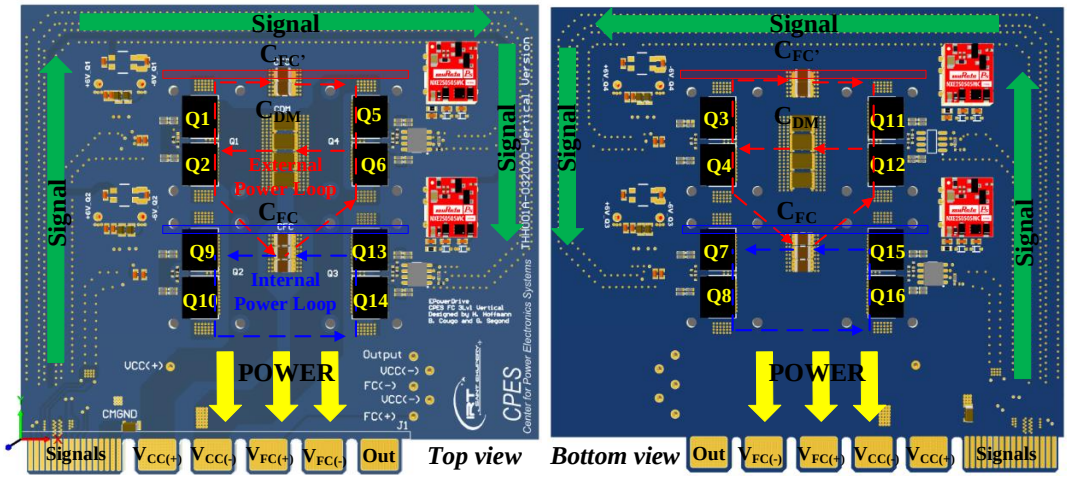


Figure 202 - Vertical version switching cell (top and bottom views). The external power loop is presented in red, and the internal power loop is in blue. The green and yellow arrows show signal and power separated paths on the PCB.

Vertical solution PCB has 112 mm x 94 mm, and the layers were selected to ensure symmetry. In Figure 203, two transversal cuts (red and blue translucid rectangles in Figure 202) are presented as well as the high-frequency current path during commutation for the external (in red) and internal (in blue) power loops.

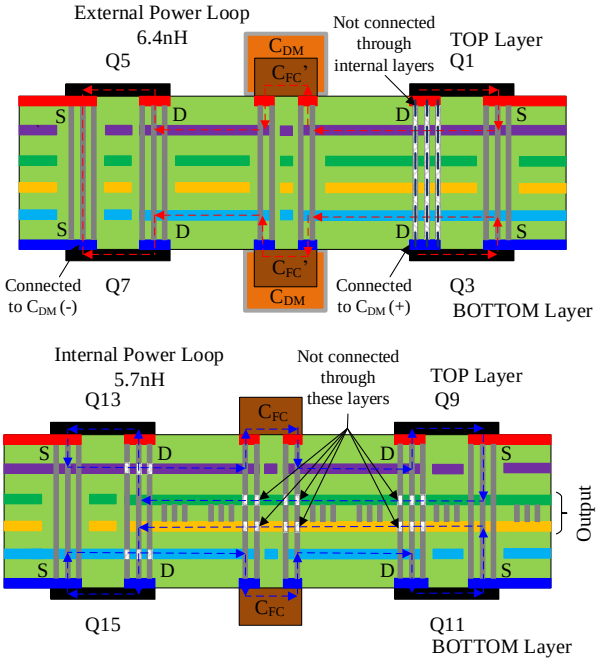


Figure 203 - PCB transversal view representing part of high frequencies current symmetric path for the Vertical version through PCB layers. The figure on the top represents part of the external power loop path (6.4 nH), and the figure on the bottom represents part of the internal power loop path (5.7 nH).

Given the ceramic capacitors on both sides of the PCB, the current is equally divided between top and bottom paralleled devices. However, this disposition with vertical power flow complexifies cascading other FC cells in series without increasing the number of PCB layers. It is mainly due to the power connector location down on the PCB since all flying capacitor connections must be connected to external film capacitors placed in an external board.

The Horizontal solution shown in Figure 204 is formed by eight layers (70 µm copper thickness), and the power flow between the external and internal cells is in a horizontal sense. Signals and power tracks are superposed for Q5-Q8 and Q13-Q16. In that case, the layer stack has a different disposition in such a way power and signal tracks are distant between each other (in the region close to the power connector).

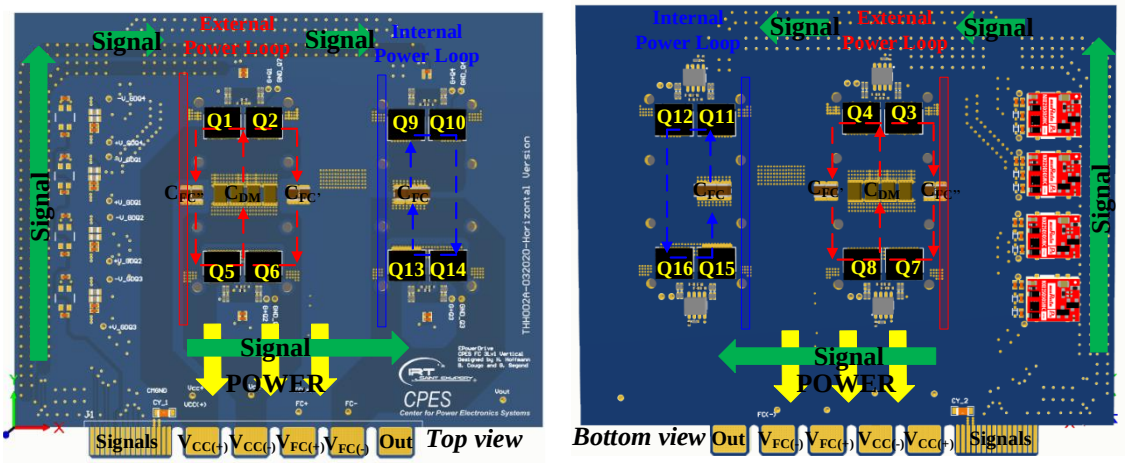


Figure 204 - Horizontal version switching cell (top and bottom layer views). The external power loop is presented in red, and the internal power loop is in blue. The green and yellow arrows show the signal and power crossed path on the PCB close to the power connections.

Horizontal version PCB has 132 mm x 103 mm. The three bottom layers were reserved to signal and to solder bottom GaN HEMTs. It allows a shield to be made between PWM signals and power supply passing through the seventh layer between the sixth and eighth (bottom), as shown in Figure 205.

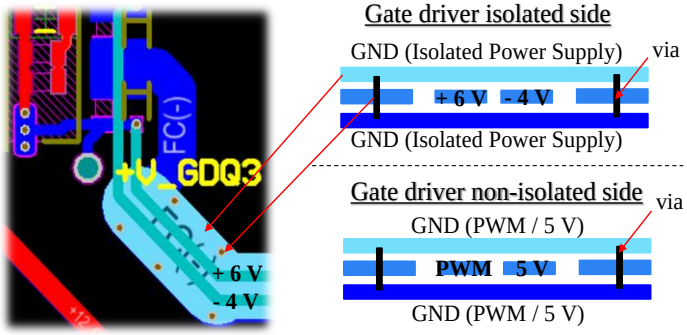


Figure 205 - Signal and auxiliary power supply shielding idea used in Horizontal and Vertical versions to prevent coupling between power and signal tracks.

Due to signal shielding and signal mix with power tracks, it is impossible to accomplish current symmetry between top and bottom devices as presented in Figure 206 (red and blue translucid rectangles in Figure 204) for both external and internal loops.

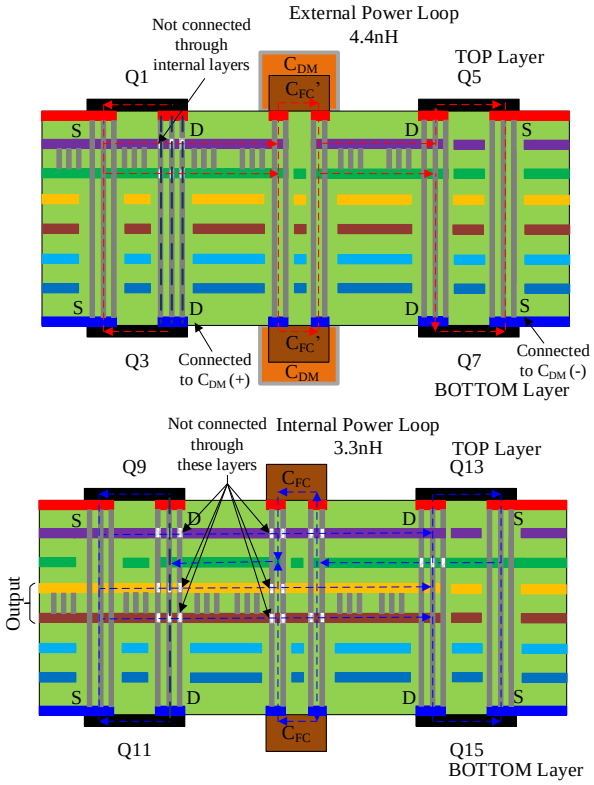


Figure 206 - PCB transversal view representing part of high frequencies current asymmetric path for the Horizontal version through PCB layers. The figure on the top represents the external power loop path (4.4 nH), and the figure on the bottom is the internal power loop path (3.3 nH).

Nevertheless, the Horizontal version is easier to cascade flying capacitor cells in series with the same PCB layers as presented in Figure 207.

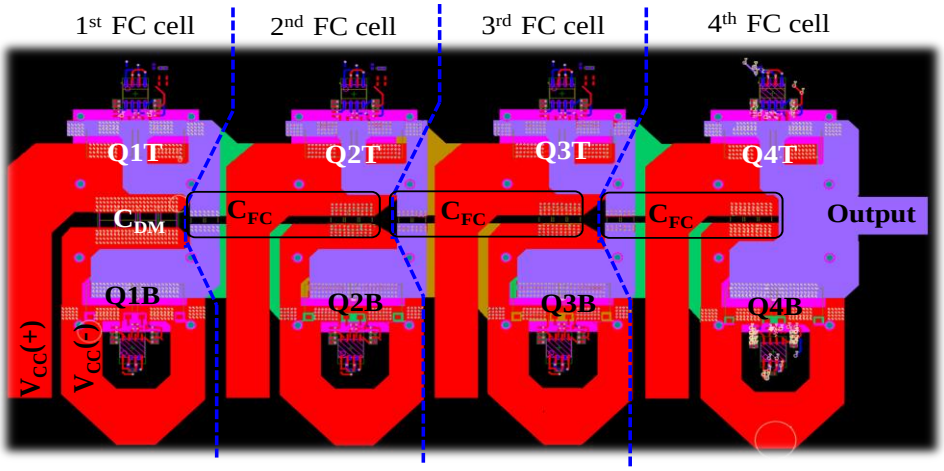


Figure 207 - Four FC cells connected (five-level FC topology) in series based on the Horizontal version routing with 8 layers (5 layers used for power tracks).

5.1.1.3 Parasitic Inductance Characterization

Both PCBs were built to be evaluated considering the measurement of loop inductance to validate simulations. An impedance analyzer was used with an impedance pin probe presented in . All drain to source connections were shorted with conductor copper tape soldered to the respective connections. The probe was placed in the internal power loop case between C_{FC} connections, as presented in . For external power loop measurement, C_{FC}/C_{FC}'/C_{FC}'' were shorted and pin probe was placed between C_{DM} connections.

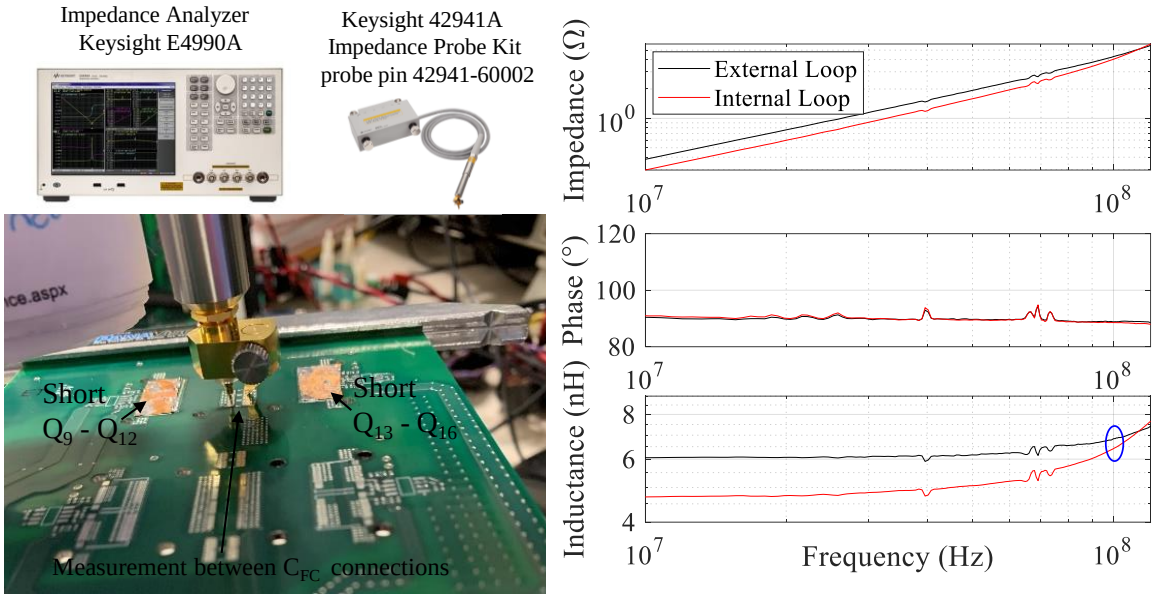


Figure 208 - Power loop inductance (a) measurement setup for the internal loop considering an impedance analyzer and (b) measurements for the Vertical version.

A good approximation is verified between measurements and simulated values according to at 100 MHz. A maximum difference of 16% was observed for the Internal loop of the Horizontal Version.

Table 19 – Simulated and measured power loop inductance for Vertical and Horizontal versions.

Inductance	Calculated (100 MHz)	Measured (100 MHz)
External Loop Horizontal Version	4.4 nH	4.9 nH
Internal Loop Horizontal Version	3.6 nH	4.2 nH
External Loop Vertical Version	6.4 nH	6.8 nH
Internal Loop Vertical Version	5.7 nH	6.4 nH

The Vertical version was considered for the operational tests, thermal characterization, and efficiency measurement due to the symmetry between top and bottom paralleled devices and the separation between power and signal tracks. Experimental verification is presented in the following sections.

5.1.1.4 Thermal Characterization

An important constraint on the inverter cooling system was set in Section 1.3.2. It must consider air cooling only. Due to the power handle by the inverter, natural air cooling is unfeasible, and then it was decided to adopt forced air cooling. Two pure copper heat sinks from Cool Innovations (4-100708U-F) were considered for the four paralleled devices, as shown in Figure 209, totalizing 8 for the leg and two fans. Thermal pad of the paralleled devices are connected to the source terminal, and they are electrically connected. Initially, isolation between the two heat sinks connected to the paralleled devices was not considered.

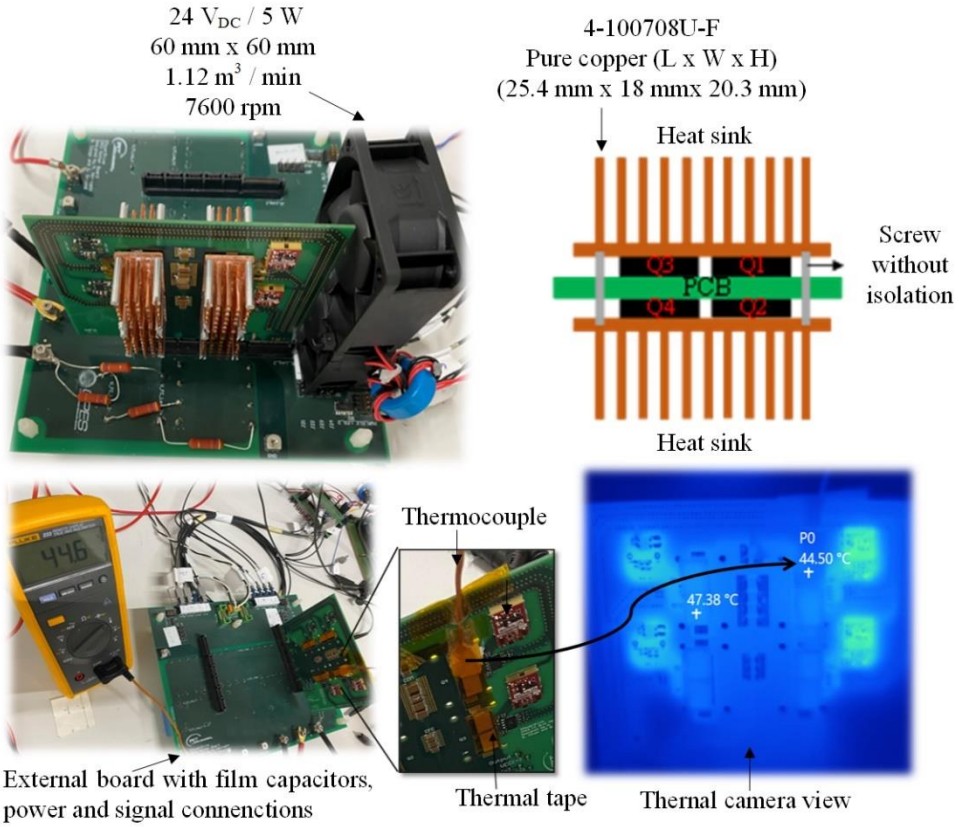


Figure 209 - Thermal characterization setup of 3-level FC leg with two non-isolated heat sinks per 4 devices.

The thermal characterization test aims to estimate the device junction temperature by measuring its $R_{DS(on)}$ and determine the cooling system's equivalent thermal resistance. Then this information can be used to estimate the semiconductors junction temperature (T_j) for the nominal operation. To perform this characterization, it is assumed that, without a heat sink, device loss will be mainly dissipated by the

PCB since the case to ambient thermal resistance is very high due to the small surface of thermal exchange. Therefore, T_j can be assumed as the case temperature. Then, the following procedure is applied:

1) Without heat sink and fans, short circuit all 16 devices and impose a continuous current by controlling the power supply and verify devices temperature with a thermal couple or a thermal camera, as shown in Figure 209.

2) When the temperature of all devices is stabilized, measure the V_{DS} of all devices to see the current distribution among them. Calculate the mean value of V_{DS} and estimate $R_{DS(on)}$ with the input current.

3) Trace $T_j\,(R_{DS(on)}) \approx T_{case}\,(R_{DS(on)})$ by increasing input current.

4) With heat sink and fan, increase the current, measure V_{DS}, estimate $R_{DS(on)}$, and with T_j $(R_{DS(on)})$ relation without heat sink, estimate T_j.

One first remark is that without a fan and heat sink, the heat is mainly dissipated by the copper layers of the PCB to the air (all tests were done with fixed V_{GS}). Devices close to the power connector have lower temperatures than those at upper region, as presented in Figure 210, for an input current of 13.5 A. This behavior is due to the heat preferable path created from the leg to the board with film capacitors (Auxiliary board) through power connectors. Nevertheless, it is possible to identify that paralleled devices have almost the same temperature, implying that they handle nearly the same current. By connecting the heat sinks and fan, this temperature unbalance between devices in the upper and lower regions goes from around 12 ºC (at 13.5 A) to 5 ºC.

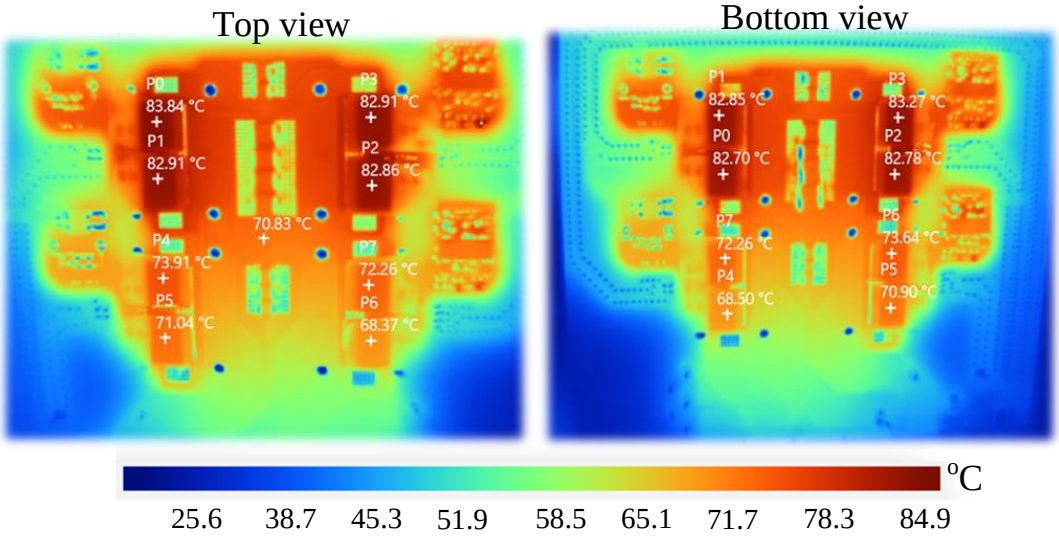


Figure 210 - Thermal camera view from Top and Bottom layer of the Vertical version without heat sinks and input current of 13.5 A.

Thermal characterization results are presented in Figure 211 for the leg without a cooling system, heat sink only, and heat sink + fan. Curves on the right show the measured (points inside of

blue area) and calculated $R_{DS(on)}$ (linear extrapolation) values as a function of the input current in each device. The leg's nominal current inverter application is around 43 A so that each device will handle about 10.75 A. In the case of the heat sink + fan setup, measurements were performed up to 40 A. Curves on the right show the relation between T_j and device current. Temperature was measured only without the cooling system, and the relation between T_j and $R_{DS(on)}$ was considered to estimate the other two situations. By considering 10 A per device, the estimated T_j (T_h 25 ºC), and the calculated $R_{DS(on)}$, the cooling system thermal resistance ($R_{TH\text{-}HS} = (T_j - T_h)/(I^2*4*R_{DS(on)})$) is 5.06 K/W with heat sink only, and 1.56 K/W with heat sink + fan. It means that each device will be at 103 ºC for the inverter operating point (T_h = 70 ºC and 674 W semiconductor losses) with the complete cooling system shown in Figure 209.

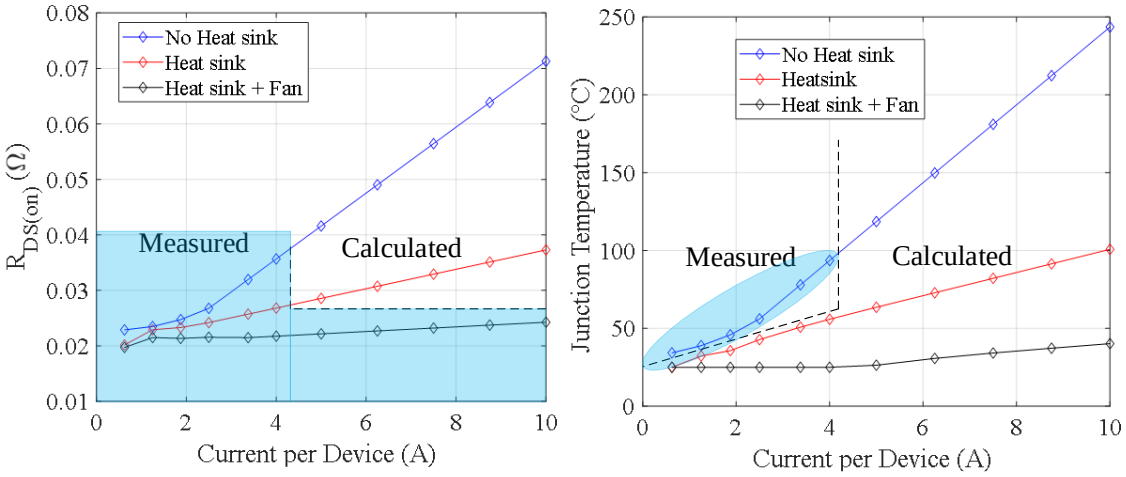


Figure 211 - Measured (inside of light blue area) and calculated (linear extrapolation) $R_{DS(on)}$ and junction temperature (T_j) per device as a function of input current.

After verifying that the cooling system can handle the leg nominal power, the next section will bring FC leg functional tests and efficiency measurements.

5.1.1.5 Operational and Efficiency Results

Operational tests considered the FC leg working initially as a dc-dc buck converter, as shown in Figure 212, connected to a variable RL load. For a duty cycle < 0.5, and the current I_{Out} leaving the leg (direction shown in Figure 212), V_{Out} is a switched voltage with 2 * f_{sw}. In that condition, S1 and S2 do not conduct simultaneously, and V_{Out} is either V_{FC} (S1 on and S2 off) or V_{bus} - V_{FC} (S1 off and S2 on). These two devices switch the current and generate switching losses, while conduction losses are divided between S1, S2, and their complementary switches according to the duty cycle value. Output current ripple is determined by the output inductance of 600 µH, which is connected in series with a variable power resistor.

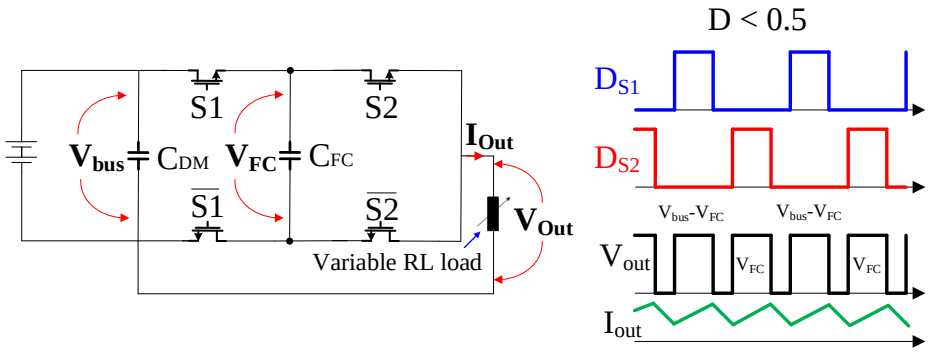


Figure 212 - FC leg behavior as a dc-dc converter with D < 0.5 connected to a variable RL load.

The test setup to perform the operational tests and measure switching speed, overvoltage, and efficiency, is shown in Figure 213, where the FC leg is placed above an Aux. board where film capacitors are placed ($C_{DM\text{-}film}$ = 60 µF and $C_{FC\text{-}film}$ = 100 µF) and input (power and signal) and output power connectors. Voltage measurements were taken in the FC leg (after power connector) with the intention to verify waveforms as close as possible of the GaN HEMTs. The control of the FC leg was performed by considering the DSP (Digital signal processor) TMDSDOCK28379D and one electrical to optical interface board.

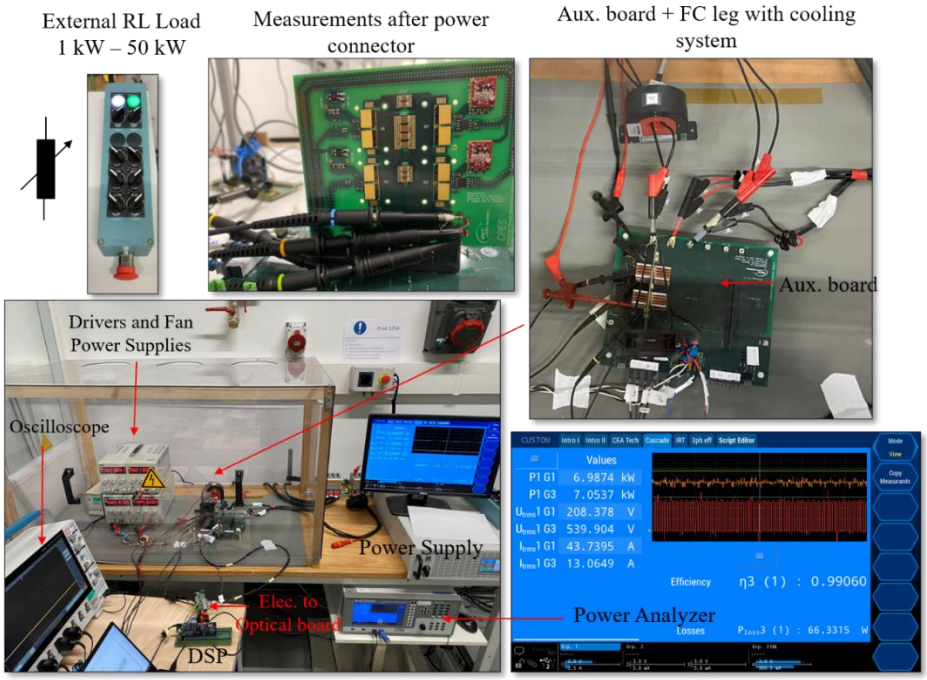


Figure 213 - Test setup with the FC leg (Vertical version) connected to the Aux. board. Power supply (540 V) and an RL load are connected to the motherboard, and PWM signals are generated by a DSP (TMDSDOCK28379D) with optical interface.

Waveforms in Figure 214 show the output voltage in light blue for 43 A (I_{Out} light green), D = 0.3, and the V_{FC} in orange with an unbalance of around 1 V at f_{sw} = 40 kHz. The output voltage has an equivalent switching frequency of 80 kHz. Each voltage step is related to the external loop S1 device switching and the following stage with the S2 device of the internal loop, highlighted in red. The

overvoltage also identifies the difference between the commutation of devices from both power loops during commutation. The larger the loop inductance, the larger the oscillations as the overvoltage observed as investigated in [254].

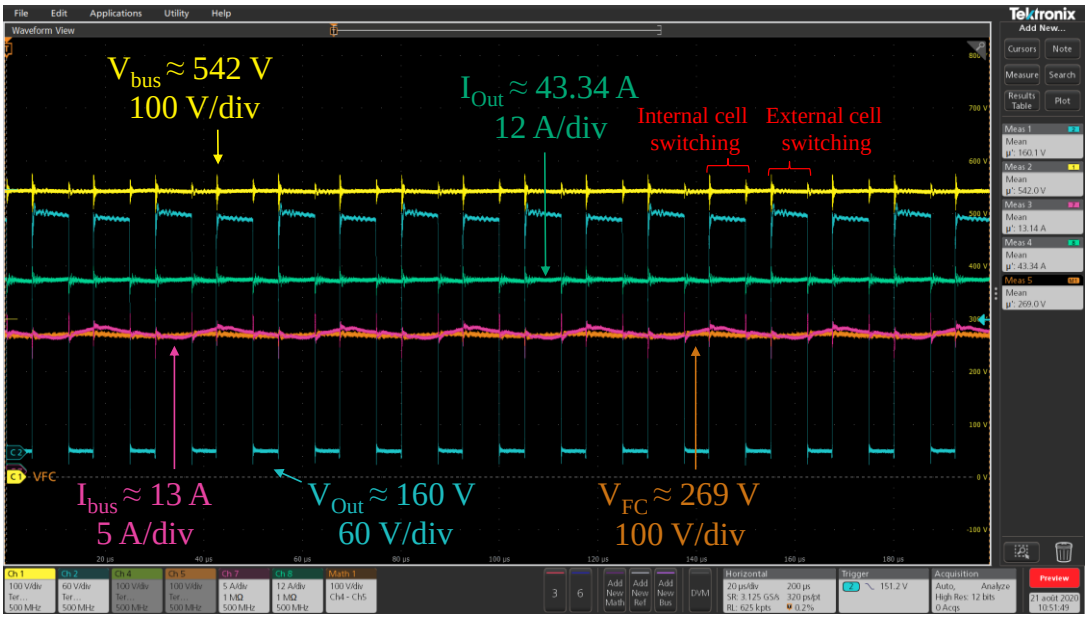


Figure 214 - Measured waveforms of Vertical version working as a buck converter with V_{bus} = 540 V (yellow), D = 0.3, I_{Out} = 43.34 A (light green) at 40 kHz. The output voltage V_{Out} is shown light blue and flying capacitor V_{FC} in orange.

Overvoltage due to the commutation can be divided into two parts, as shown in Figure 215. The first is called HF (High frequency). It is related to power loop inductance resonance with the device's stray capacitances. The second, highlighted in green, is due to the resonance of film capacitors placed in the Aux. board, and it is named LF (Low frequency). These two resonances causing the overvoltage were measured as 33 MHz for HF and 1.5 MHz for LF.

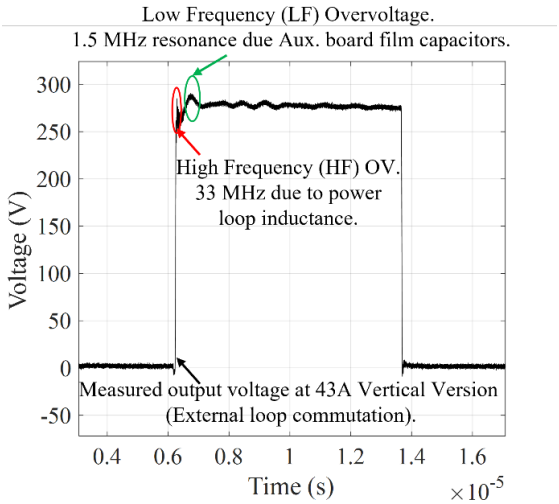
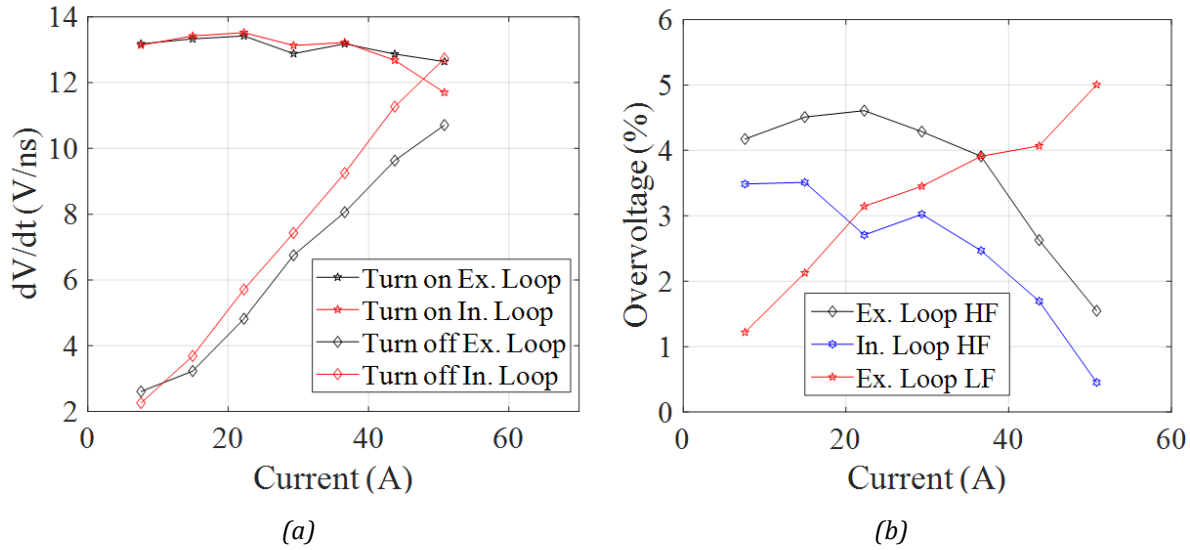


Figure 215 - Overvoltage according to the oscillation frequency of 33MHz (HF) due to power loop inductance and 1.5MHz (LF) due to the resonance with the film capacitors placed on Aux. board.

Measured switching speed is presented in Figure 216 (a), for turn-on and turn-off, from 7 A to 51 A, for the commutation of both internal (S2) and external (S1) cells. The speed of turn-on switching is mainly controlled by gate charge current, depending on V_{GS} (V_{DR} -V_{GSP}), $R_{G\text{-}on,}$ and C_{GD}. The isolated power supply defines gate drive voltage $V_{DR,}$ and V_{GSP} is the Miller plateau voltage that increases with the current [255]. Therefore, a minor decay is verified in turn on switching speed with current increase. However, both switching cells present closer switching speed values, reaching their maximum of 13.22 V/ns at 22 A.



(a) *(b)*

Figure 216 - Measured (a) switching speed and (b) output voltage peak value for the turn-on and turn-off of each switching cell for different current levels. Tests were performed with the switching cell working as a buck converter with V_{bus} = 540 V, Duty cycle = 0.3, and f_{sw} = 40 kHz.

On the other hand, turn-off speed depends on output current and C_{oss} as presented in [255], [256]. This behavior is valid if channel current (I_{Out}) does not reach the minimum value to guarantee $V_{GS} > V_{TH}$, then the channel is not formed, characterizing the absence of the miller effect. For high current values the miller effect occurs, and dV/dt is less dependent on I_{Out}. In that case, the impact of the loop inductance is more evident. As an example, the internal loop switching (which has the lowest loop inductance) reaches 11.27 V/ns at 43 A, while the switching of the external loop reaches 9.63 V/ns. Unlike other works about the switching speed of GaN HEMTs reaching values higher than 50 V/ns, the FC leg reaches the maximum of 13.5 V/ns at 22.2 A. The leading cause is the increase of C_{GS} (gate to source capacitance) due to the paralleling of four devices of 650 V and the gate driver (Si8271BBD-IS) peak current limitation of 4 A. Nevertheless, the other insulated gate drivers recommended by GaN Systems for the 650V devices (ACPL-P346-000E, ADUM4121ARIZ, and HEY1011) have even lower peak current, limited to 2 A.

In Figure 216 (b), it is verified that the external loop causes a higher overshoot than the internal power loop when a device is switched. The maximum value of 4.7% on the steady-state output voltage (around 270 V) at 23 A. It reinforces the impact of the more significant power loop inductance effect of the external switching cell. On the other hand, the overvoltage caused by HF reduces with the current level, whereas the one caused by LF increases. Nevertheless, for the highest tested current level, it is around 5% (13.5 V), which is not an issue for the final converter operation.

Gate to source voltage (before gate resistor of 1 Ω) waveform is presented in Figure 217 for 22 A and duty cycle = 0.7. The voltage probe was connected through 2 cm long twisted cables, the smallest length, without making a short circuit with the heat sink. Despite the oscillations, caused mainly by the measurement apparatus, V_{GS} reaches its maximum peak value of 6.57 V and the minimum peak value in - 3.47 V. Actually, the real V_{GS} (on devices gate and source connections) should have even lower overvoltage and oscillations, which the 1 Ω resistor should attenuate. No overvoltage was verified that could harm the device. Nevertheless, it is worth pointing out that $V_{GS\text{-}off}$ in the steady-state is considerably lower (3 V) than first designed (3.9 V). This behavior is caused by the resistor placed in series with the two zeners in the gate driver circuit, which limits zener current. According to the device datasheet, zener voltage is reached for 5 mA, but it does not have a satisfying voltage regulation. So, any variation of zener reverse current can cause a large changeset in zener voltage, even if the current is increased. On the other hand, the 6.2 V Zener has an excellent regulation even with 1 mA. Tests were carried out with this setup, and no issues were observed.

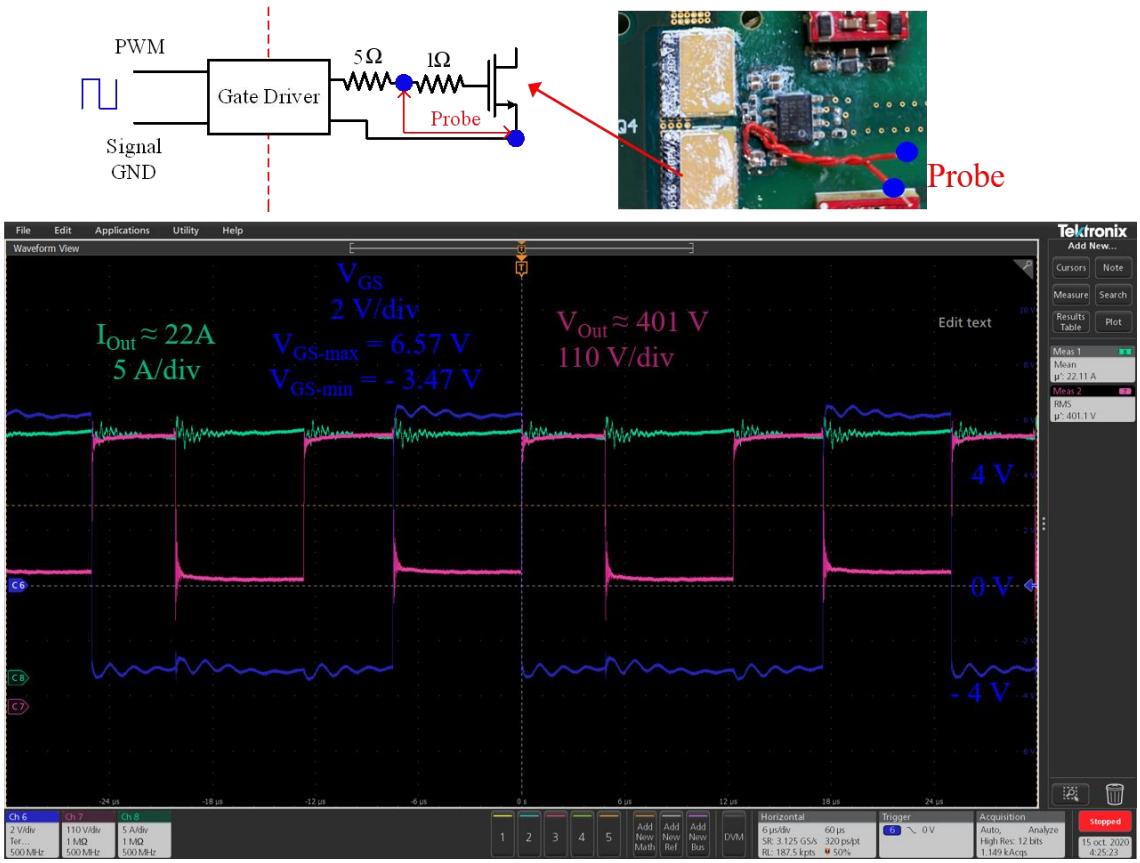


Figure 217 - Gate to source measured voltage (in blue), V_{Out} = 401 V (in pink) and I_{Out} = 22 A (in green) for V_{bus} = 540 V, D = 0.7, at 40 kHz, and deadtime of 50 ns.

Efficiency measurements were performed using a Power Analyzer (ZES Simmer LM G670), measuring input power (V_{bus} and I_{bus}) and the power delivered to the RL load (V_{out} and I_{out}) as presented (in red) in the circuit schematic in Figure 218. Bus voltage was fixed in 540 V, D = 0.3, f_{sw} = 20 kHz and 40 kHz, and the load was varied, generating I_{Out} from 7 A to 53 A. Four power resistors (dashed yellow resistors in Figure 218, $R_{pre\text{-}FILM}$ = 47 kΩ) were used for the pre-charge of flying capacitor C_{FC} between $V_{bus\,(+)}$ | $V_{FC\,(+)}$, $V_{FC\,(+)}$ | V_{Out}, V_{Out} | $V_{FC\,(-)}$, and $V_{FC\,(-)}$ | $V_{bus\,(-)}$.

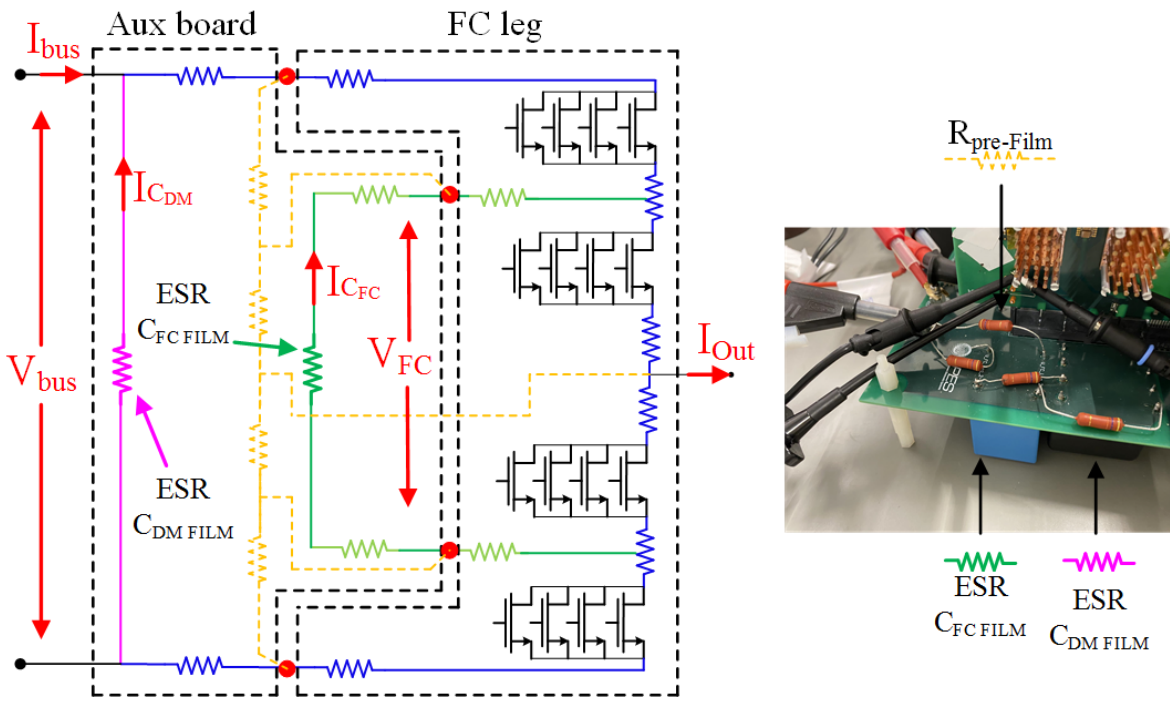


Figure 218 - Resistive path for the dc-dc buck test setup considered for loss calculation.

Theoretical calculation of losses was also evaluated considering the same information of switching energies and on-resistance of the considered in Chapter 2 for the GS66516T. Losses due to connections, film capacitors, and PCB tracks were considered for a fair comparison. Loss composition can be divided into five parts based on the resistive elements presented in Figure 218:

1) Due to precharge resistors R_{pre} (dashed yellow resistance):

$$P_{R_{pre}} = \frac{V_{bus}^{\ 2}}{4 * R_{pre-FILM}} . \tag{5.2}$$

2) Due to *ESR* (pink resistor) of $C_{DM\ FILM}$ film capacitors, carrying the current I_{CDM}:

$$P_{C_{DM\ FILM}} = ESR_{C_{DM\ FILM}} * I_{C_{DM}}^{\ 2} . \tag{5.3}$$

3) Due to PCB resistances in blue (R_{Blue}) carrying I_{Out}. Output current will circulate part of the time on the blue resistances above the output connection point and the other part on the resistors below the output connection point. Therefore, losses are calculated considering the mean value of R_{Blue} for the operation as an inverter. In the case of the buck converter with the current leaving from the leg, blue resistances above the output connection point (and the one between V_{FC}(-) and V_{Out}) will be lossy. Therefore, the equation can be approximated to the inverter operation:

$$P_{PCB} = \frac{R_{Blue} * I_{Out}^{\ 2}}{2} . \tag{5.4}$$

4) Due to I_{FC} passing into the green path formed $C_{FC\ FILM}$ film capacitors (green resistor) and the power connector (light green resistors = R_{Green}) between Aux. board and the FC leg:

$$P_{FC} = \left(R_{Green} + ESR_{C_{FC\ FILM}}\right) * I_{C_{DM}}{}^{2} \quad (5.5)$$

5) Semiconductor losses are divided in conduction losses (P_{cond}) and switching losses (P_{sw}):

$$P_{semi} = P_{cond} + P_{sw} \quad (5.6)$$

Switching losses are calculated considering that in one period of the apparent switching frequency ($2*f_{sw}$) of the output voltage, there will be a turn-on and turn-off of four devices, and the loss due to reverse conduction of the complementary switch during the dead time. This last part of losses can be modeled as an equivalent switching energy E_{DT} that will happen twice in a switching period (one in a turn-on and the other in a turn-off):

$$P_{sw} = 8 * \left(E_{on}(I_{Out}) + E_{off}(I_{Out}) + 2 * E_{DT}\right) * f_{sw} \quad (5.7)$$

Switching energies are based in Figure 34, and E_{DT} can be estimated as the power calculated considering I_{Out} the reverse drain to source voltage $V_{ds\text{-}reverse}$ (I_{Out}) multiplied by the dead time period, $t_{dead\text{-}time}$ (50 ns was considered), as:

$$E_{DT} = I_{Out} * V_{ds-reverse}(I_{Out}) * t_{dead-time} \quad (5.8)$$

In the case of conduction losses, it is necessary to know the exact junction temperature of the device, in steady-state, to determine drain to source resistance as follows:

$$P_{cond} = R_{ds(on)}(T_j) * I_{Out}{}^{2} \quad (5.9)$$

An iterative method to estimate $R_{ds(on)}(T_j)$ is considered as presented in Figure 219. T_j is approximate by P_{semi} $*R_{TH\text{-}HS}$ + T_h, where $R_{TH\text{-}HS}$ is the cooling system thermal temperature (1.3 K/W) determined in the previous section, and T_h is the ambient temperature (25 ^{o}C). It consider the relation $R_{ds(on)}(T_j)$ of device datasheet and *i* iterations until $T_j(i)$ - $T_j(i\text{-}1)$ < 1^{o}C.

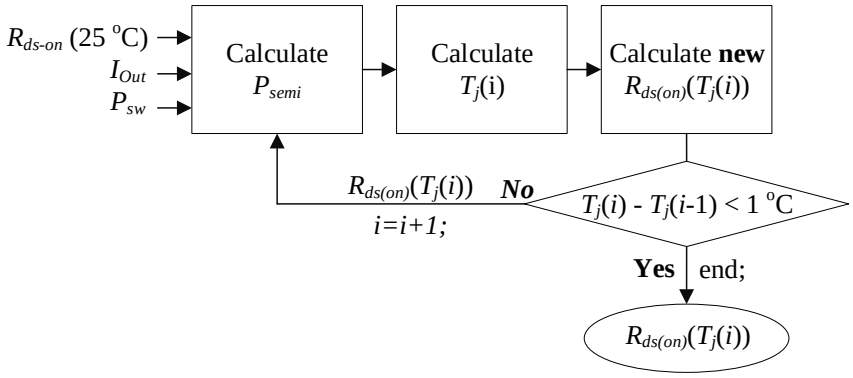


Figure 219 - Iterative procedure to determine $R_{ds(on)}$ (T_j) based on semicondutor losses and thermal circuit

.

I_{CDM} and I_{FC} are determined by circuit simulation, and R_{Blue} and R_{Green} were measured considering the same procedure used on the thermal characterization. An input current of 1 A was injected in the circuit with all switches short-circuited, the voltage of each path was measured, and the respective resistances were calculated. Therefore, the FC leg losses can be estimated as:

$$P_{FC-leg} = P_{R_{pre-film}} + P_{C_{DM\ FILM}} + P_{PCB} + P_{FC} + P_{semi}. \quad (5.10)$$

Good agreement is verified between measured and calculated losses in Figure 220 (a) and efficiency in Figure 220 (b), at f_{sw} = 20 kHz (black) and 40 kHz (red), for the current range.

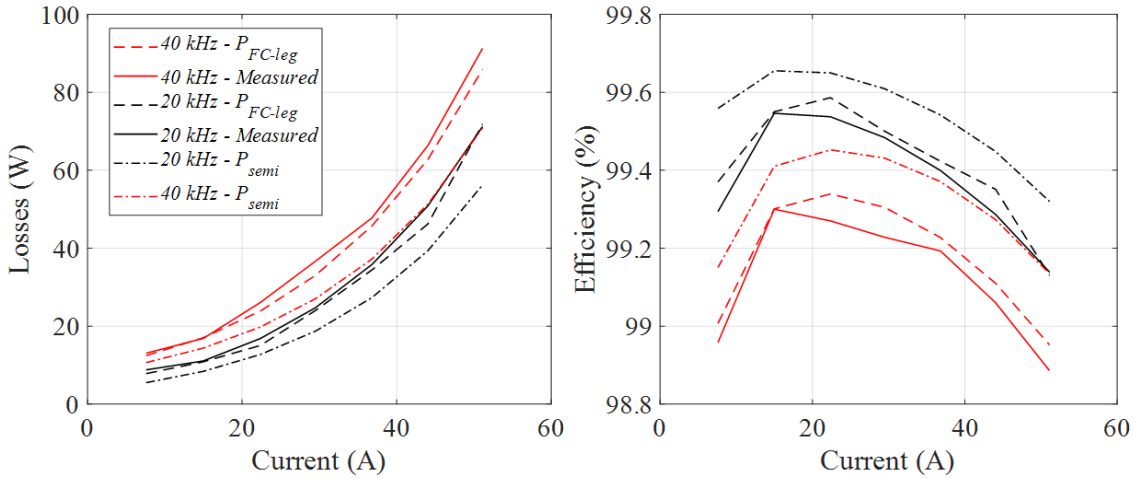


Figure 220 - FC leg as a dc-dc buck converter measured and calculated (a) losses and (b) efficiency for V_{bus} = 540 V, D = 0.3, 7 A < I_{Out} < 51 A at f_{sw} = 20 kHz and 40 kHz, and deadtime of 50 ns.

The dashed curves represent the calculation considering Eq. (5.10), while the dashed-pointed curves represent only P_{semi}. The error between measurements and $P_{FC\text{-}leg}$ is 5.9% (5.38 W) at 51 A, and 22.3% (20.38 W) considering only P_{semi} at 40 kHz. At 20 kHz, $P_{FC\text{-}leg}$ is even closer to the measured losses, with a difference of < 1% at 51 A. The impact of not considering connections, PCB, and the

other resistive paths is evidenced by comparing P_{semi} at 40 kHz and measured losses at 20 kHz (the curves are almost superposed). Precise loss calculation impact is also presented in the form of efficiency, as shown in Figure 220 (b). The curves considering $P_{FC\text{-}leg}$ are much closer to the measurement than those using P_{semi}.

FC leg was also evaluated as a single-phase inverter for the same conditions used for the buck converter. The main difference is the load connection to the middle point created with two aluminum capacitors ($C_{bus\ ALU}$ = 8.2 mF each – LXR451LGC822MFK0M) connected to V_{bus} presented in Figure 221. In addition, two precharge resistors ($R_{pre\text{-}Alu}$ dashed brown resistors) of 67 kΩ are connected in parallel with each $C_{bus\ ALU}$. Therefore, the loss calculation must consider the losses of these extra devices, mainly because the *ESR* of $C_{bus\ ALU}$ (brown resistors) is around 16 mΩ (equivalent *ESR* of $C_{bus\ FILM}$ is approximately 0.6 mΩ). The resistive path of the new test setup is presented in Figure 221, and the loss calculation procedure is similar to the one given for the buck converter. Nevertheless, P_{sw} is calculated with the process described in Section 2.5.1, but considering the addition of two E_{DT} per switching period. The losses of $R_{pre\text{-}Alu}$ are estimated similarly to the Equation (5.2) but with two resistors.

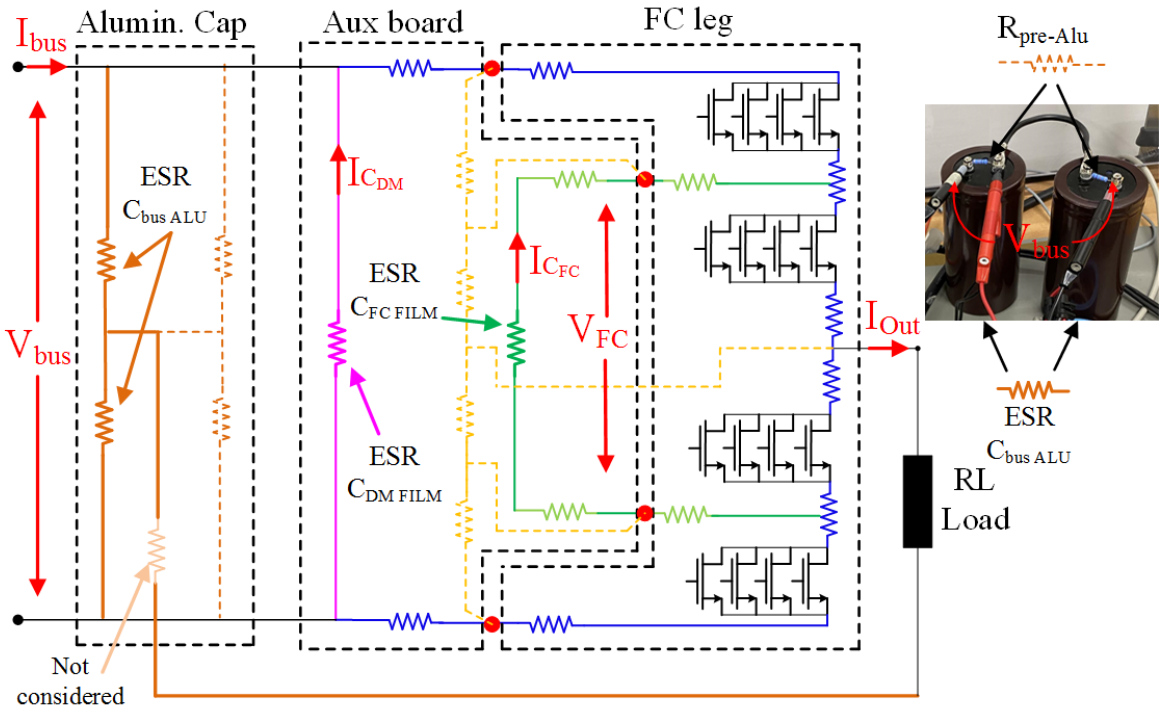


Figure 221 - Resistive path for the monophase inverter test setup considered for loss calculation.

Since the middle point will be I_{Out} return path, it will flow through $C_{bus\ ALU}$. Therefore, the losses on $C_{bus\ ALU}$ (P_{Alu}) are estimated as:

$$P_{Alu} = \left(\frac{ESR_{C_{DM\ ALU}}}{2} \right) * I_{Out,rms}{}^{2} \quad (5.11)$$

The behavior of the FC leg as a single-inverter is presented in Figure 222, V_{Out} is shown in blue and I_{Out} in light green, for a modulation index of 0.95 and a fundamental frequency of 220 Hz. The

flying capacitor voltage unbalance is evident, around 8.5% (23 V), leading to V_{FC} = 249 V instead of 270 V (theoretical).

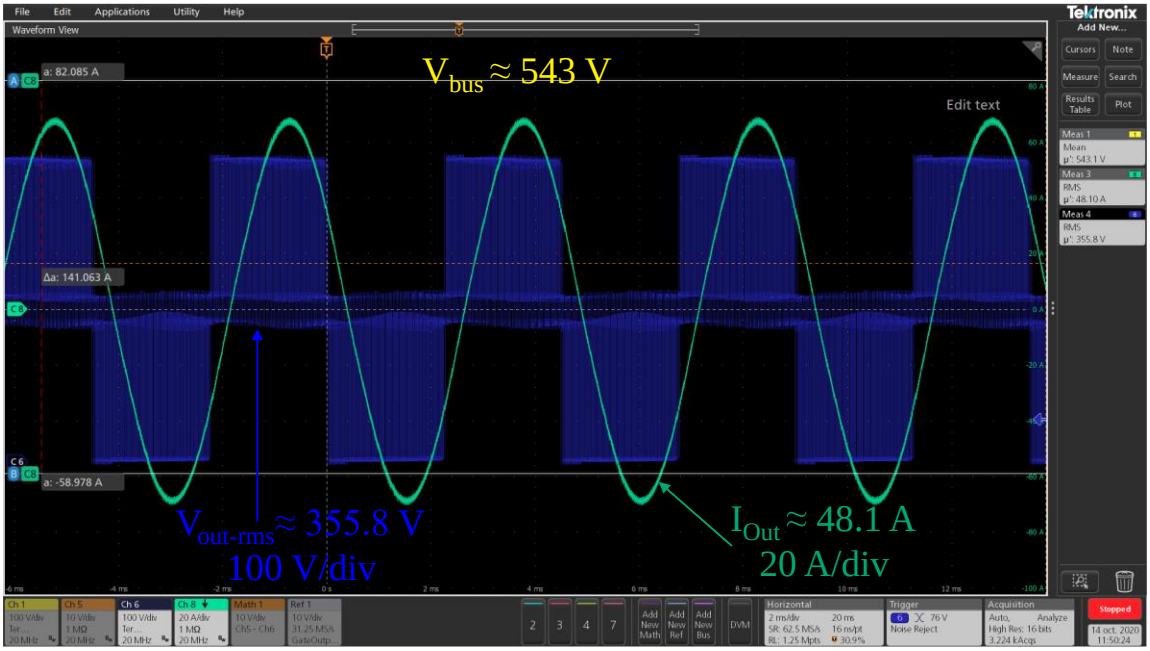


Figure 222 - Measured waveforms of Vertical version working as a monophase inverter with V_{bus} = 540 V (blue), Modulation Index = 0.95, I_{Out} = 48 A_{rms} (light green) at 40 kHz.

Flying capacitor unbalance did not compromise the operation of the inverter, and it was observed that it was pretty sensitive to any touch of pressure applied in the FC leg. Therefore, the power connection was improper, mainly because the leg was removed and replaced at the Aux. board several times. The measured and calculated losses and efficiency of the FC leg are presented in Figure 223. The error between measured and computed losses is 26% (5.8 W) at 8.3 A, and it reduces to 3% (2.56 W) at 42 A (inverter final operation condition). The measured and calculated efficiency at 42 A is 98.82% and 98.77%.

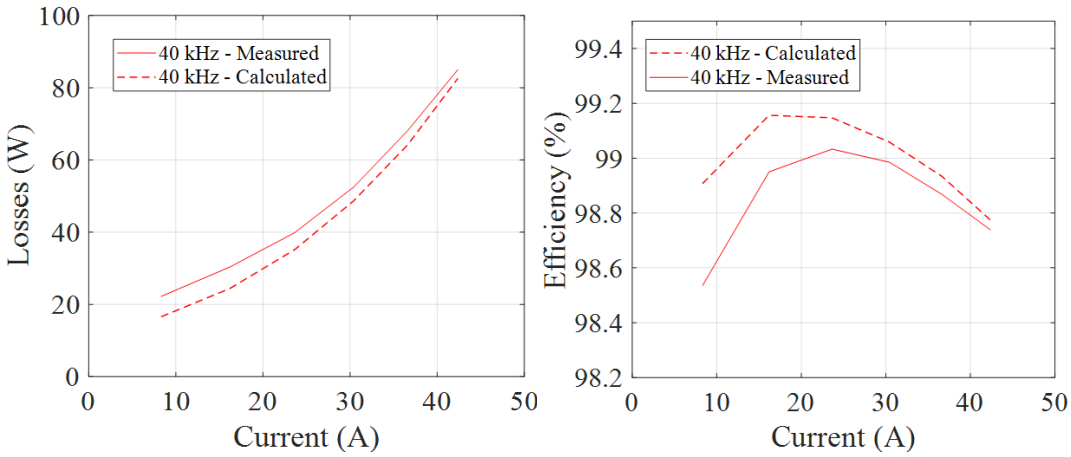


Figure 223 - FC leg as a single-phase inverter measured and calculated (a) losses and (b) efficiency for V_{bus} = 540 V, Modulation index = 0.95, 7 A < $I_{Out,rms}$ < 51 A at f_{sw} = 40 kHz, and deadtime of 50 ns.

The functional validation of the design FC leg showed good matching between measured and calculated losses, except for the flying capacitor voltage unbalance of around 8.5%, which was strongly affected by the power connector. The leg reached experimentally 98.77% of efficiency for the final inverter operation point. The following section brings the general conclusions from the experimental verification of the FC leg and the proposed improvements.

5.1.1.6 Section conclusions

Section 5.1.1 presented the design of a three-level flying capacitor leg with four GaNs in parallel, which composes the final inverter. Two solutions (Horizontal and Vertical) were evaluated by simulation according to the power loop inductance reduction and layer symmetry. The key to reducing power loop inductances in flying capacitor topologies with paralleled GaN devices is to split ceramic capacitors C_{FC} and consider part of these capacitors close to precedent capacitors (close to C_{DM} in the case of a three-level topology). This technique reduced power loop inductance by around 41% in the Vertical solution board. Both solutions present the same gate circuit design and the same gate loop (approximately 2.5 nH). The Horizontal version shows lower loop inductances (4.4 nH/3.6 nH) but 8 layers and asymmetry between top and bottom paralleled devices. The main advantage of this solution is the possibility to easily cascade FC cells in series. At the same time, the proximity of the signal and power tracks goes against PCB's good design practices.

On the other hand, the Vertical version comprises 6 layers and a symmetrical arrangement of the components that compromises loop inductance (6.4 nH/5.7 nH). This solution allows the separation between signal and power tracks, reaching an utterly symmetrical circuit between the top and bottom devices and layers disposition. For these reasons, the Vertical version was selected to be built and experimentally evaluated.

Power loop inductances were measured using an impedance analyzer, and a maximum error compared to the simulation of 11% was verified for the internal loop and 6% for the external loop. The thermal characterization showed that the cooling system used on the tests had an equivalent junction to ambient thermal resistance of 1.3 K/W (heat sink + fan) and 5.06 K/W (heat sink only). It means that each device will be at 165 ºC with heat sink only, and 103 ºC considering the heat sink + fan, for the inverter operating point (T_h = 70 ºC and 674 W semiconductor losses). Therefore, it is necessary the use of forced air cooling.

The FC leg reached a switching speed of 11.27 V/ns at 43 A and V_{bus} = 540 V due to the gate driver (Si8271BBD-IS) peak current limitation of 4 A. Nevertheless, the other insulated gate drivers recommended by GaN Systems for the 650V devices (ACPL-P346-000E, ADUM4121ARIZ, and HEY1011) have even lower peak current, limited to 2 A. Regarding the overshoot on the output voltage, two phenomena were evaluated: the resonance (1.5 MHz) due to the film capacitor placed in an Aux. board (named LF) and the resonance (33 MHz) between the power loop inductance and devices parasitic capacitances (named HF). The maximum overshoot value of 4.7% was measured on the steady-state output voltage (around 270 V) at 23 A (HF). On the other hand, the overvoltage caused by HF reduces with the current level, whereas the one caused by LF increases. Nevertheless, LF overshoot reached around 5% (13.5 V). It shows that the final converter will have good switching behaviour, far from dangerous values which could destroy devices.

The proposed solution was evaluated as a dc-dc buck converter and a single-phase inverter for V_{bus} = 540 V and output current from 7A until 53A. An Aux. board with film capacitors (DC-Link and flying capacitor) was used so that the FC leg worked as a pluggable PCB. During the tests, no unbalance on flying capacitor voltage was noticed as a dc-dc converter, while an unbalance of 8.5% (23 V) was noticed for the single-phase inverter test at 42 A. This unbalance did not compromise the inverter operation, and it was observed that it was quite sensitive to any touch of pressure applied in the FC leg. Therefore, the power connection was improper, mainly because the leg was removed and replaced at the Aux. board several times. Calculated and measured losses (at 40kHz) presented a good matching with an error of 5.9% for the dc-dc buck test (at 51 A) and 3% for the monophase inverter test (at 42 A_{rms}, which is close to the inverter operation point). The impact of not considering connections, PCB, and the other resistive paths on loss calculation can underestimate the leg losses up to 20%. Regarding the efficiency, the FC leg reached almost 99.2% at 38 A (dc-dc buck test) and 98.8% in the single-phase test for the final inverter operation point (42 A_{rms}), both at 40 kHz. At this last, the loss value not related to the semiconductors represented 36% of total losses.

A second version of the FC leg was proposed in the inverter prototype presented in Figure 188 regarding the results and remarks concerning the experimental verification presented above, as shown in Figure 224. In this version, signal connections were placed above the leg to connect with the Control board, and screwed metallic connectors (Wurth 74622104) were used for power connections, intending to reduce connector wear of placing and removing the FC leg and guaranteeing good electrical contact.

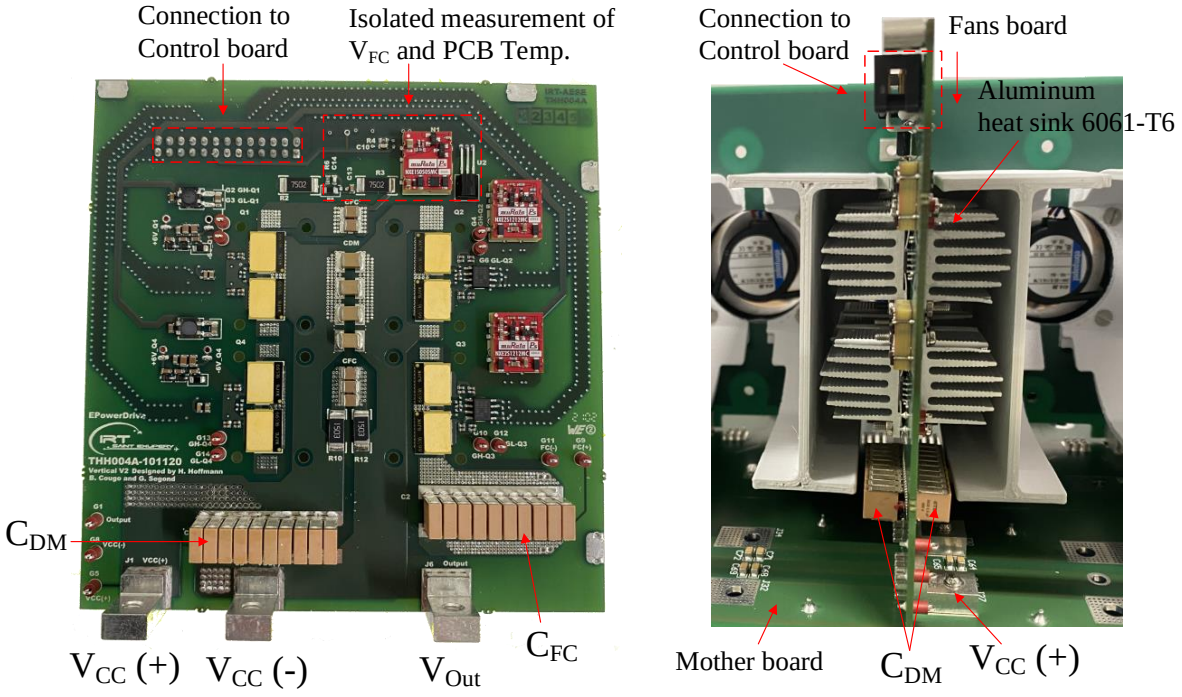


Figure 224 - Second version of the inverter flying capacitor leg.

Ceramic capacitors from the family TDK Ceralink were placed directly on the leg for the DC – Link (C_{DM} = 5 µF (900 V) – 2 x B58035U9255M001) and the flying capacitor (C_{DM} = 20 µF (500 V) – 2 x B58035U5106M001). Therefore, reducing V_{bus} oscillation on the leg input voltage and the film capacitors need on the Mother board. It also removes the need for power connections for flying capacitors, reducing the stray inductances and guaranteeing a better balance on V_{FC}. Besides the

modifications described above, an additional circuit to measure V_{FC} was implemented intending to verify the possibility of implementing inverter closed-loop control. The following section will present the experimental verification of the entire inverter described in Section 5.

5.2 Inverter Experimental Results

Experimental verification of the proposed inverter is divided into two major parts. The first consisted of evaluating the proper operation of the proposed multilevel inverter regarding flying capacitor voltage balance, the influence of non-equal current sharing between paralleled legs, and inverter efficiency. The second part considered the inverter in the Conducted Emissions setup described into RTCA/DO-160-G, intending to validate the EMI model proposed in Chapter 3 for multilevel topologies. Due to internal infrastructure limitations and the complexity of controlling an electric motor in a closed-loop with the proposed inverter, the experimental evaluation considered a three-phase 50 kW RL load.

5.2.1 Operational Characterization

The setup presented in Figure 225 was used to perform the operational characterization. A computer controls the power supply and the DSP, while an Aux. Power Supply (28 V) was used to feed the Control board. A Power Analyser (Zimmer LMG670) was used to measure the efficiency of the inverter (input and output voltages were measured in inverter connections) connected to an external RL load. For monitoring, an oscilloscope was used with isolated voltage probes set to a 1/1000 scale.

Figure 225 - Inverter operational characterization setup.

Figure 226 shows the output voltage and output current waveforms for an input voltage of 340 V, 21 kVA (77 A), f_{sw} = 40 kHz, m_a = 0.76, f_{lf} = 50 Hz and SPWM technique. Both output voltage and current RMS values are balanced. Current waveforms present no visible ripple (due to 600 µH connected to each load phase), while output voltage ripple is essentially sinusoidal with superposed high-frequency ripple.

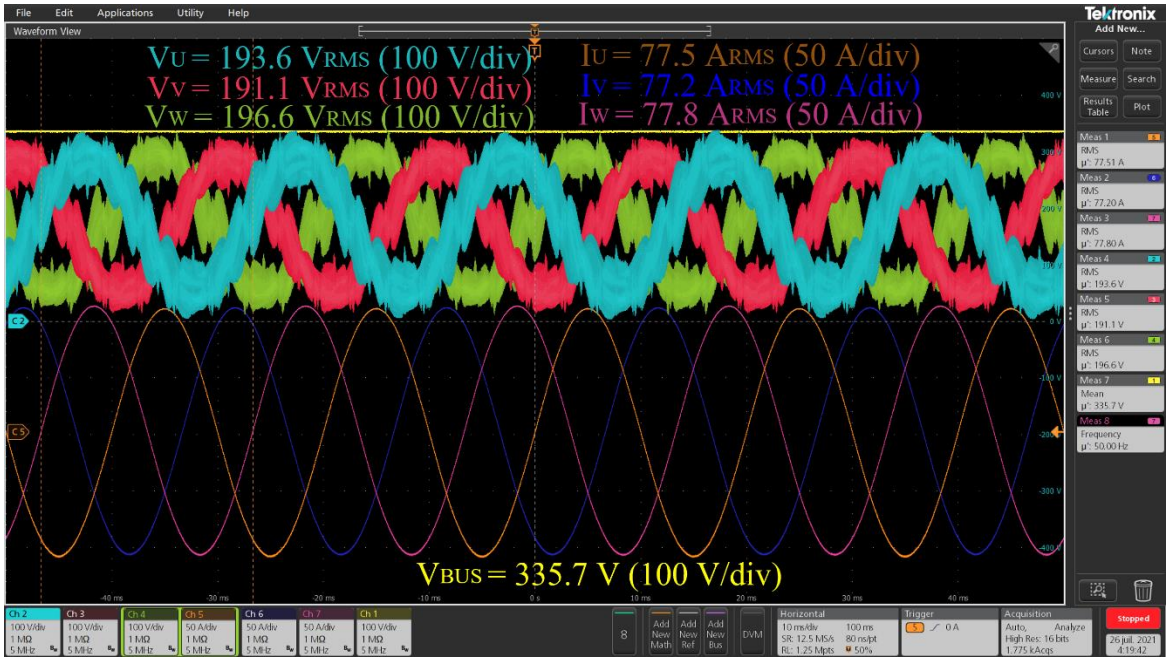
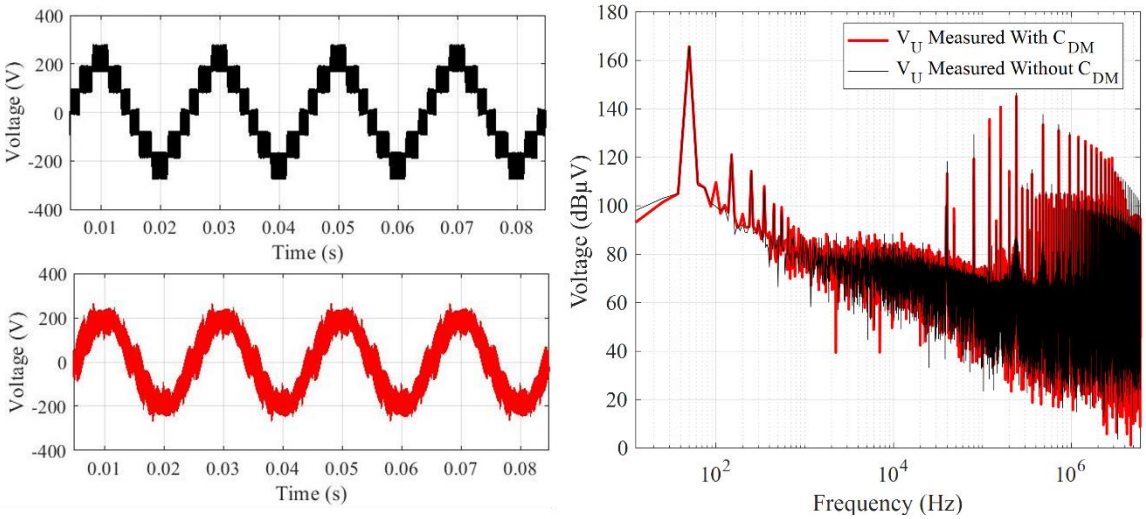


Figure 226 - Inverter output voltage and current for 340 V input voltage, 21 kVA and output current of 77 A_{rms}. Tests were carried out with 40 kHz, m_a= 0.76, f_{lf} = 50 Hz, and SPWM.

The phase to neutral voltage waveform is mainly composed of 7-levels as the measurement presented in Figure 227(a) if no differential mode capacitors ($C_{DM\text{-}Out}$) are used on inverter output (theoretically expected). By connecting $C_{DM\text{-}Out}$, a low-pass filter is applied on inverter output, resulting in the red waveform in Figure 227(a). Nevertheless, in Figure 228(b) in the frequency domain, both waveforms have the same harmonic content until 5 MHz, showing a similar behavior to the EMI voltage source considered on the CM filter design in Chapter 3. The red waveform will present lower harmonics after 5 MHz; thus, CM filter design considering the multilevel output voltage without $C_{DM\text{-}Out}$ (as considered in the previous chapters), figures a more conservative strategy.



(a) Time domain *(b) Frequency domain*

Figure 227 - Measured output voltage with (red) and without (black) $C_{DM\text{-}Out}$ capacitors.

The proper operation of the inverter is directly related to the inverter output voltage and current, as presented above. However, flying capacitor voltage unbalance and different current sharing among paralleled legs phenomena can be hidden if only output electrical quantities are observed. Current on paralleled legs shall be equal on magnitude and phase. However, due to PWM delays and dead time, circulating currents appear between paralleled legs because of the voltage between the paralleled legs output connection. This phenomenon is constantly discussed in multilevel parallel inverters. These circulating currents may not affect phase output current but may generate current unbalance among paralleled legs, leading to extra losses (inductors and semiconductors) and flying capacitor voltage unbalance. However, the modeling of this phenomenon is not addressed in this thesis.

Figure 228 shows the measured output voltage of the three paralleled legs of phase U (400 V input voltage and 66 A output current) with different levels at the intermediate voltage reference, which characterizes flying capacitor voltage unbalance and considerable ripple. Nevertheless, summing the three voltages waveforms generate the theoretically expected seven-level (purple waveform) output voltage, and no visible impact is visible on the inverter output current. Therefore, flying capacitor voltage unbalances, and ripple has a minor effect on the inverter output voltage and current.

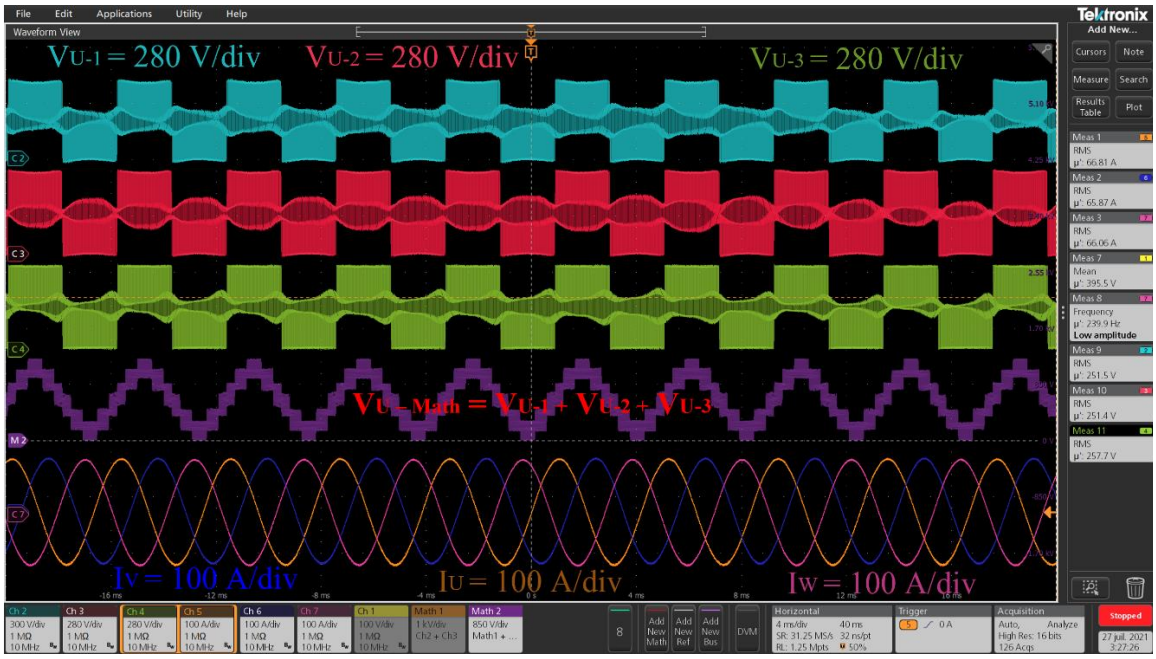


Figure 228 - Inverter output voltage and current for 400 V input voltage and output current of 66 A. Tests were carried out with 40 kHz, m_a = 0.76, f_{lf} = 240 Hz, and SPWM.

Correspondent flying capacitor voltage waveforms are presented in Figure 229 for the same operating point of Figure 228. Mean values of V_{FC} are different among paralleled legs, with different waveforms, being 19.5% to 24% higher than the expected value (200 V). Voltage behavior in a capacitor is directly related to the current integral on this capacitor. Then, since V_{FC} differs among paralleled legs, it implies that the current on each leg is different (phase and/or amplitude).

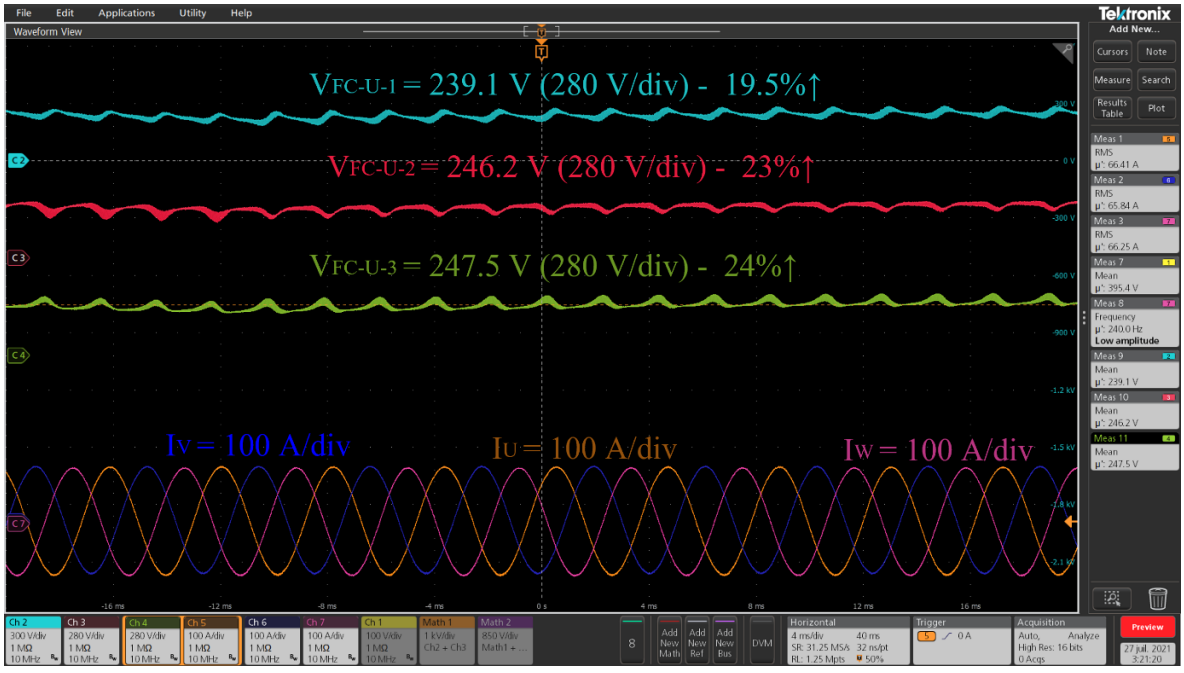


Figure 229 - Flying capacitor voltage of phase U for 400 V input voltage and output current of 66 A. Tests were carried out with 40 kHz, m_a = 0.76, f_{lf} = 240 Hz, and SPWM.

Figure 230 presents the measured waveforms of the output current of the three paralleled legs of phase U for 360 V and 25 A phase current. Theoretically, each leg should handle around 8.33 A, but their values and waveforms differ due to the circulating currents [257], [258], which adds additional losses on semiconductors. A maximum difference of 1.35 A (15.6%) is verified between currents, representing around 34% on loss increase for the leg with 10 A compared to the one with 8.65 A (close to nominal operation).

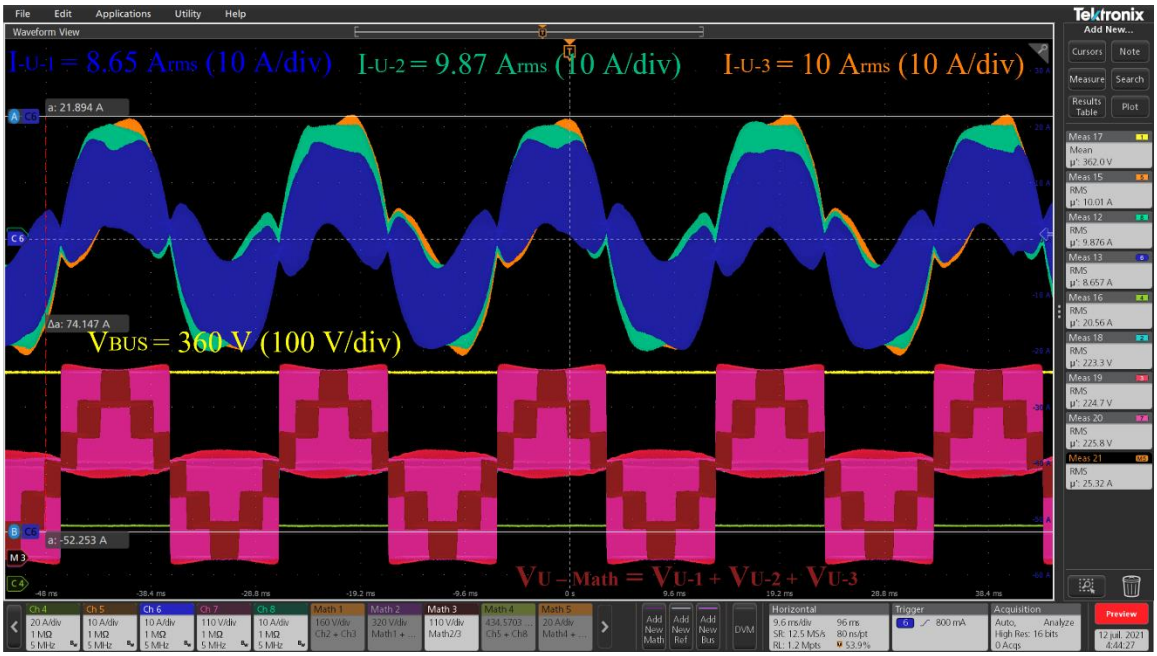


Figure 230 - Paralleled legs current of phase U for 360 V input voltage and output current of 25 A. Tests were carried out with 40 kHz, m_a = 0.76, f_{if} = 50 Hz, and SPWM.

Despite not affecting leg output voltage waveform ($V_{U\text{-}Math}$) for the presented condition, this affirmation becomes less representative if the input voltage and output current are higher, as well as if the load becomes less resistive. Figure 231 shows the inverter output voltage and current for an input voltage of 500 V and output current of 86 A (38 kVA – *PF*= 0.64). Compared to Figure 226 (21 kVA – *PF* = 0.95), output voltage presents a higher distortion, characterizing one distortion of the output voltage of each leg, mainly due to the circulating currents increase, which leads to flying capacitor voltage unbalance.

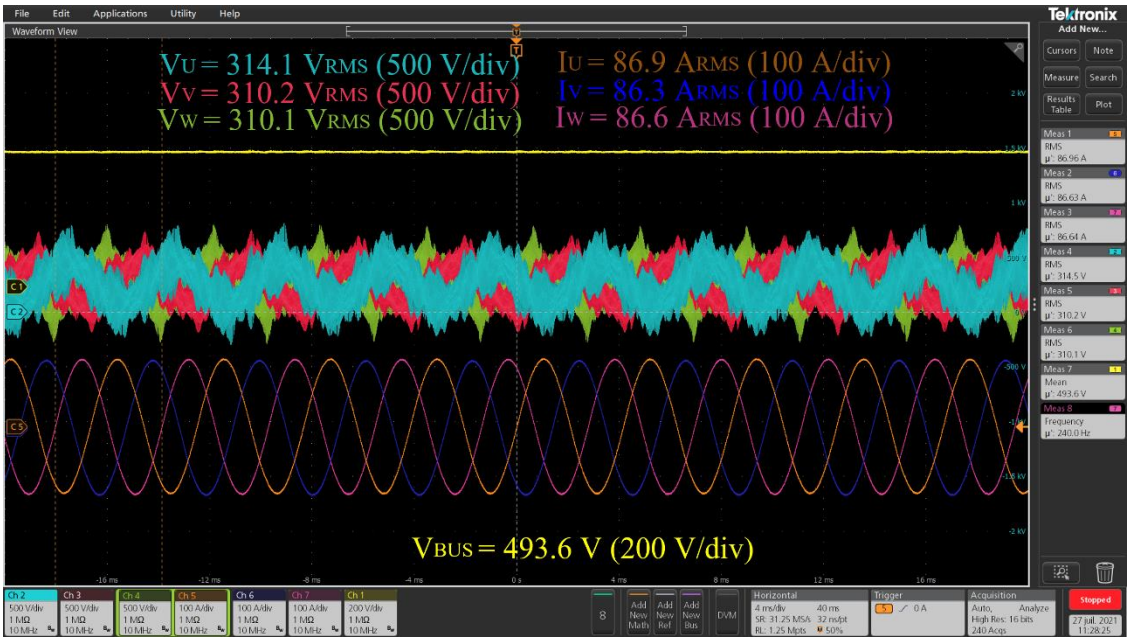


Figure 231 - Inverter output voltage and current for 500 V input voltage, 38 kVA and output current of 86 A. Tests were carried out with 40 kHz, m_a = 0.76, f_{lf} = 240 Hz, and SPWM.

Circulating currents constitute the major issue on parallel topologies, especially in interleaved converters. These currents flow through paralleled legs due to an effective DC bus voltage short circuit through output inductors [259], and they are composed of high-frequency and low frequencies components. The first is highly dependent on leg output impedance value and interleaving angle among the carrier signals. At the same time, the low-frequency component depends on the mismatch between inductor values and core properties. Different modulation techniques were proposed to reduce these currents in open-loop control, but these techniques mainly deal with high-frequency components. In contrast, closed-loop control is needed to correct low-frequency components [257]. Close-loop control is out of the scope of this thesis. Then, for safety reasons and the fact that the thermal behavior of semiconductors was not being monitored, the tests were limited to the maximum operating point of 38 kVA/87 A (70 kVA/130 A nominal operation) with open-loop control.

For the maximum operating point, it is shown in Figure 232, on the power analyzer screen, that inverter output voltage presents a high harmonic distortion compared to the curves presented in Figure 231. It leads to unbalanced output voltage effective values (15 V ≈ 10%) despite not showing an evident output current imbalance or distortion. The measurements performed with the isolated voltage probes considered the V_{BUS} (-) connection as a reference, while a floating neutral point was created for the power analyzer.

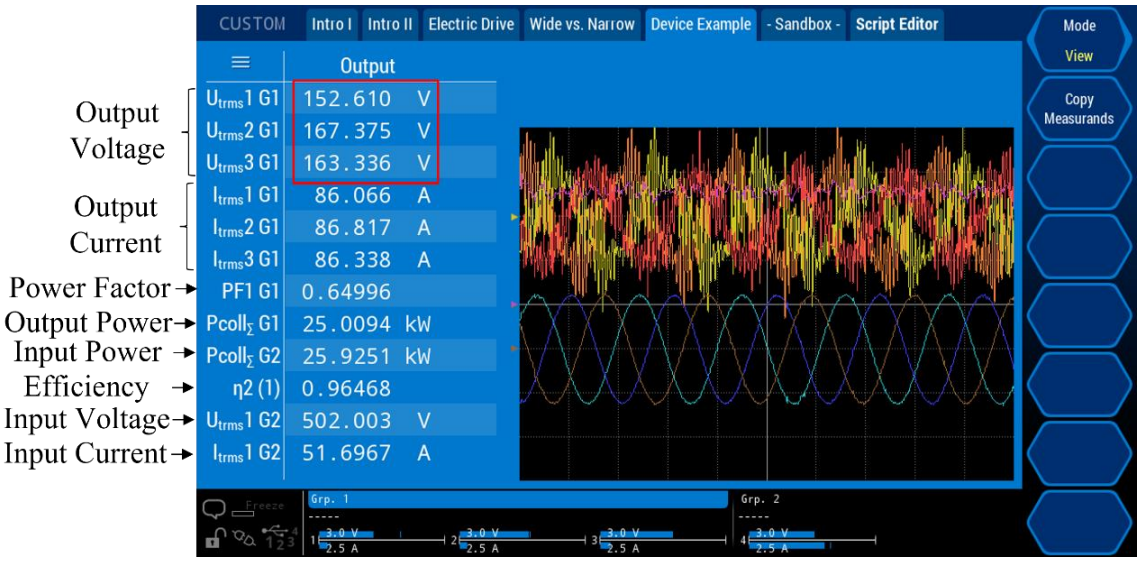


Figure 232 - Efficiency measurement for 500 V input voltage, 38 kVA, and output current of 86 A_{rms}. Tests were carried out with 40 kHz, m_a = 0.76, f_{lf} = 240 Hz, and SPWM.

In this condition, the entire power conversion system presented an efficiency of 96.4% (ratio between output and input active power). In contrast, the inverter efficiency can be expressed as a function of the absolute values of the handled power (S) and inverter losses ($Loss_{inverter}$), as:

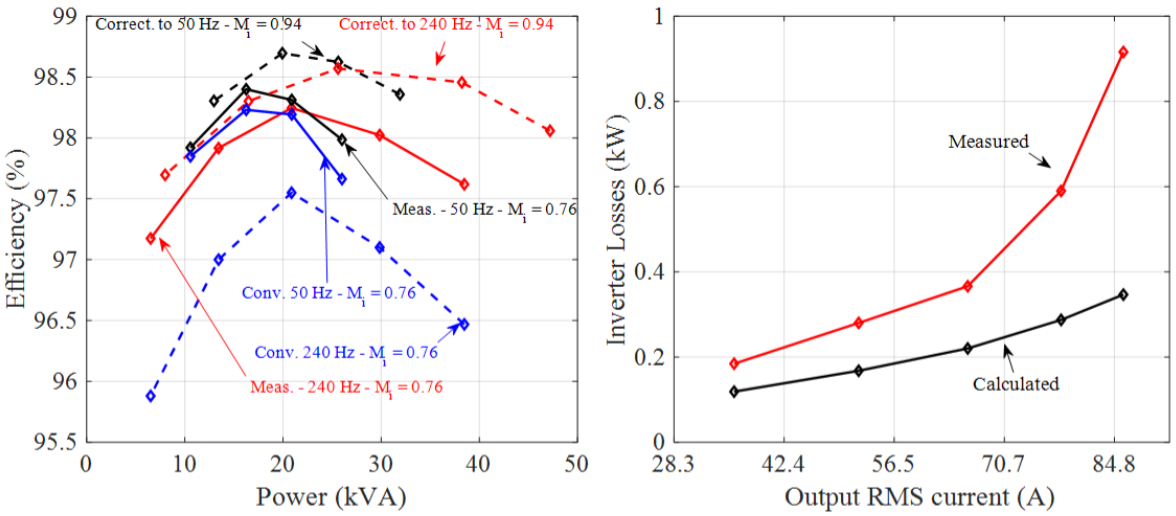
$$\eta_{inverter} = \frac{|S| - |Loss_{inverter}|}{|S|} \quad (5.12)$$

This notation is interesting to evaluate the inverter efficiency since it was one of the design constraints (98.5%) listed in Chapter 1 for the inverter design. For the condition presented in Figure 232, the inverter efficiency is calculated as 97.6%.

Inverter measured efficiency as a function of inverter output power are presented in Figure 233 (a) for f_{lf} = 50 Hz (black) and f_{lf} = 240 Hz (red), both for m_a = 0.76. At 50 Hz, the inverter reaches its highest efficiency of 98.4% at 16 kVA, while at 240 Hz, this value goes to 98.2% at 21 kVA. In contrast, power conversion efficiency presented 98.23% (blue) and 97.75% (dashed blue), respectively.

Given the inverter's final operating condition for m_a = 0.94, the output power will significantly increase, maintaining the same amount of losses for the same bus voltage and current value. Therefore, increasing the modulation index from 0.76 to 0.94 will increase the output power by 23.7%. Then, a more realistic inverter efficiency could be indirectly calculated considering this m_a increase as presented in black (50 Hz) and red (240Hz) dashed curves in Figure 233 (a). For this condition, inverters efficiency reaches its maximum of 98.7% at 20 kVA (50 Hz) and 98.6% (240 Hz) at 24.6 kVA.

The reduction of inverter efficiency with the increase of output power can be related to the rise of circulating currents on the inductors of paralleled legs and the extra losses due to this phenomenon. Curves shown in Figure 233 (b) corroborate this hypothesis, presenting measured losses in red and theoretical loss estimation in black.



(a) Efficiency x Power *(b) Inverter losses x Output RMS current*

Figure 233 - Inverter measured efficiency and losses.

Loss estimation considered the data of semiconductors (described in Chapter 2) and passive devices series resistance calculated at the end of Chapter 4. When output current is low, measured and calculated losses present closer values, while this difference becomes more significant for higher output current. Besides not considering connection and cables losses, which gives the difference in low currents, measured losses increase almost exponentially while calculated losses follow a quasi-linear increase. This loss difference can be understood as the extra losses due to the rise of circulating currents between paralleled legs with the output current increase (all 144 semiconductors were working correctly).

This section shown that the design inverter works properly and reached 98.6% (240 Hz) at 24.6 kVA. Due to circulating currents between paralleled legs, extra losses are added to the inverter as flying capacitor voltage unbalance increases for higher currents. It compromises inverter safe operation, which limited the maximum operating point to 500 V/38 kVA/87 A (70 kVA/130 A nominal operation) with open-loop control. The following section will present the conducted emissions experimental tests intending to validate the EMI equivalent circuit for multilevel converters in Chapter 3.

5.2.2 Conducted Emissions - RTCA/DO-160G

Last section showed the proper functioning of the 7-level inverter for an input voltage of 500 V and output current of 87A, which corroborates the predictive inverter design of the preceding chapters of this thesis. Despite experimental verification for the equivalent EMI circuit of a 2 – level inverter presented in Chapter 3, the generic EMI model for the multilevel series/parallel was not verified at that time. Therefore, this section presents the conducted emissions measurements according to the RTCA/DO-160G considering an RL load aiming to evaluate the proposed model.

The EMI model proposed in Chapter 3 considered the connection of heat sinks to the RTCA/DO-160G ground plane (named GND DO-160G in this thesis) as the connections of $C_{Y\text{-}In}$ and $C_{Y\text{-}Out}$. The inverter comprises 72 heat sinks, and the connections to GND DO-160G were made according to Figure 234.

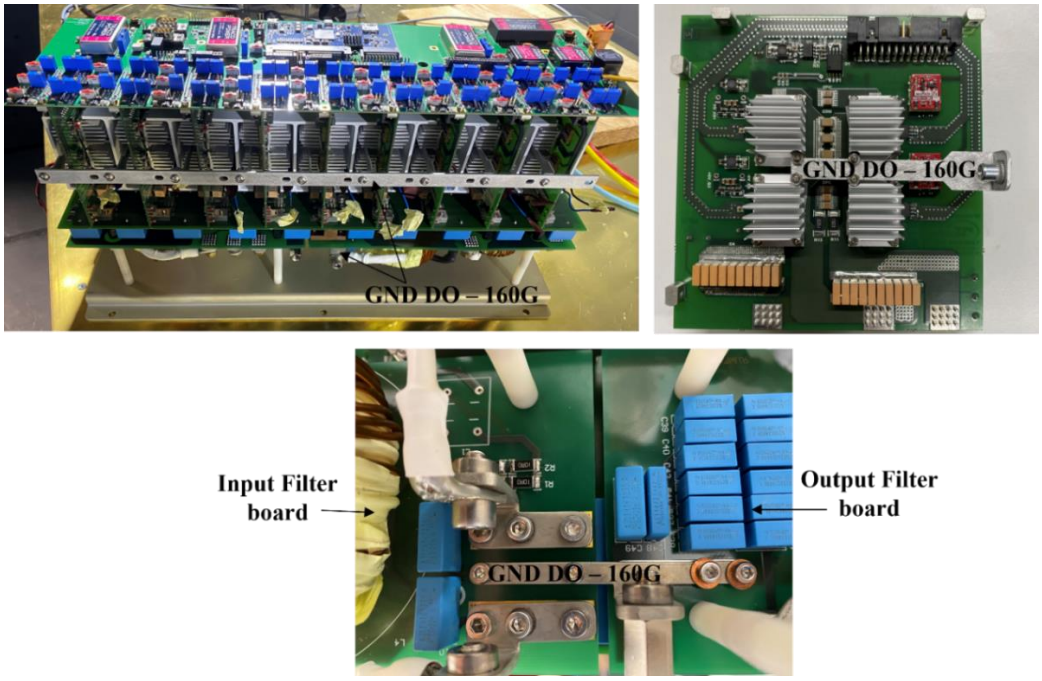


Figure 234 - GND DO-160G connection from each heat sink and input and output filters.

Conducted emissions setup is shown in Figure 235. Tests were performed into a semi-anechoic chamber where power supplies and RL load are placed externally.

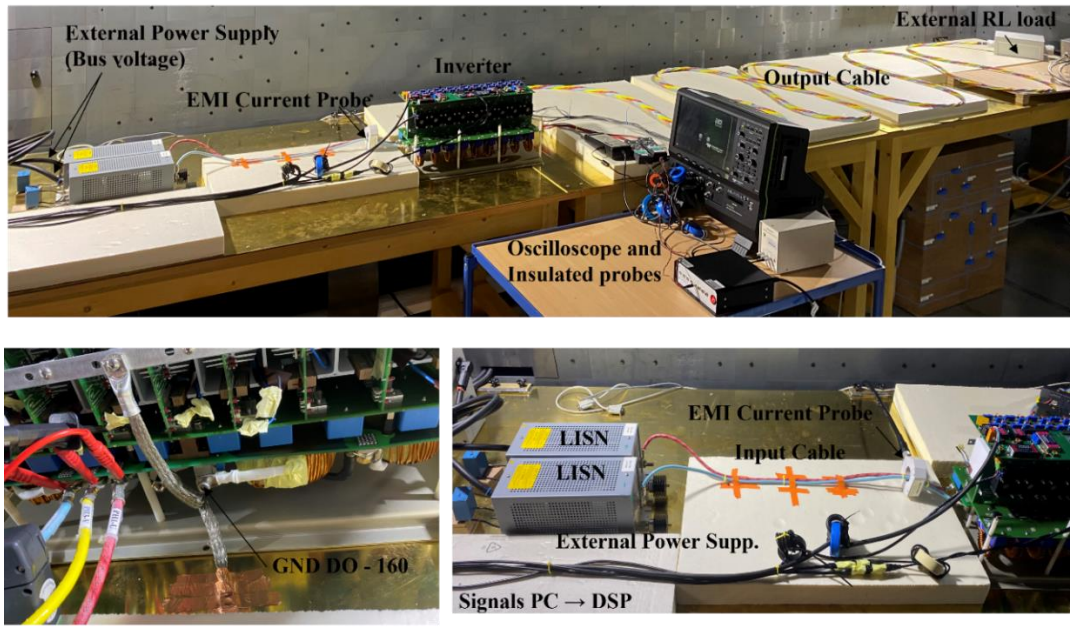


Figure 235 - Conducted Emissions test setup – 10-m long output cable and external RL load.

The input cable is 1 m long and the output 10 m long (4 AWG-EN24681-AZA from Draka), placed 5 cm above the ground plane. LISN characteristics (Rohde & Schwarz ESH3-Z6) were presented in Section 2.9.5.3. Conducted emissions (CE) measurements were performed using a Rohde & Schwarz ESR 3 EMI receiver (time domain scan mode using FFT – the same method used on the analysis in Chapter 3) and the current probe R&S®EZ-17 (20 Hz to 100 MHz – Max peak current 300 A).

CE measurements are divided into two groups: Power Lines (PL) taken up to 5 cm from inverter input connection and Interconnecting bundles (IB) on the three-phase output. Figure 236 and Figure 237 shows CE measurements up to 50 MHz in blue for an input voltage of 300 V (14 A output current) and in pink for 400 V (18 A output current), with f_{lf} = 240 Hz, f_{sw} = 40 kHz and m_a = 0.76.

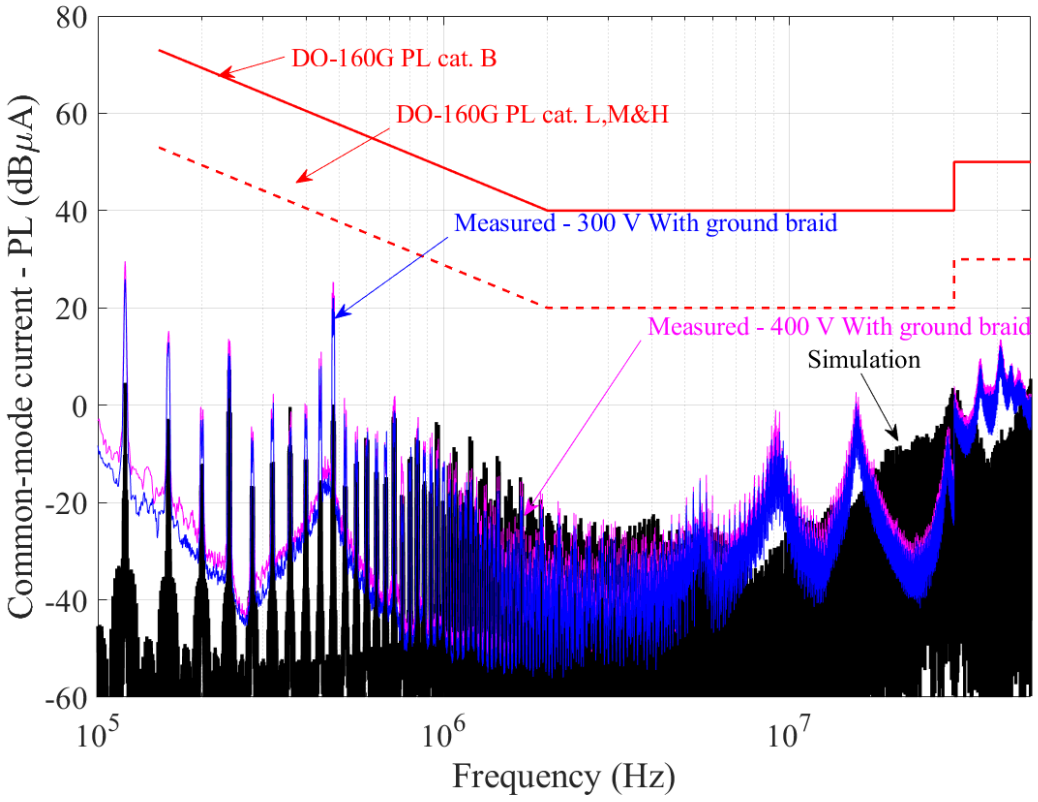


Figure 236 - Power Lines – Input. Conducted Emissions – 10-m long output cable and external RL load.

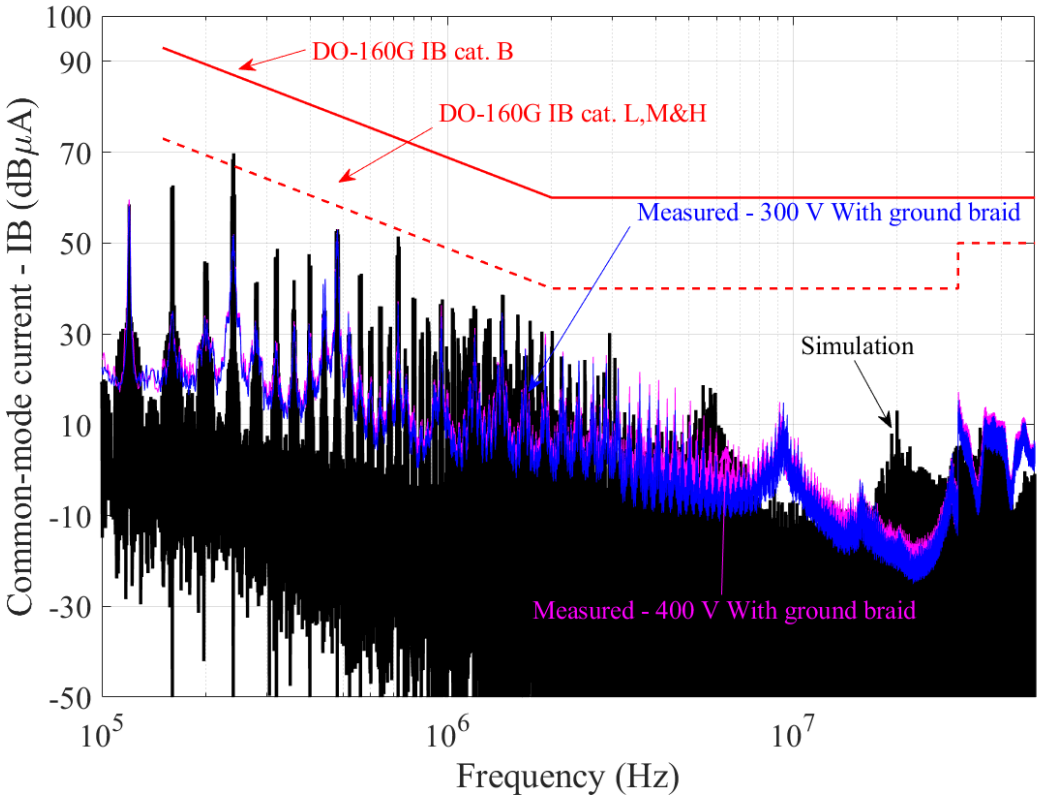


Figure 237 - Interc. Bunddles – Output. Conducted Emissions – 10-m long output cable and external RL load.

The difference between the two measurement points (blue and pink curves) is theoretically defined as 20*log(400/300) = 2.5 dB. Simulation results are shown in black, considering the EMI model shown in Figure 151 in Chapter 3 and measured impedances of input and output filters and cables, as the CM impedance of the RL load. The simulated currents (input voltage of 300 V) correspond well with measurements until 5 to 6 MHz for PL and IB. Due to the non-modeling of connections, PCBs, and ground braid, different resonances are not seen in simulation, like in 9 MHz and 15 MHz, as the differences between measured and simulated results in low frequency (150 kHz – 500kHz). Even though CM filters were designed for the machine impedance, it is seen that the inverter is compliant with the standard limits for both equipments categories (B and L, M & H). Therefore, the generic EMI model composed of two equivalent voltage sources presented in Chapter 3 can give a good tendency of CE for multilevel converters and assists CM filters predictive design (specially between 500 kHz – 6 MHz).

The inverter nominal input voltage is 540 V, implying an offset of 20*log(540/300) = 5.1055 dB (approximation for the common-mode) in the measurements done at 300 V as presented in the purple curves in Figure 238 and Figure 239. Nevertheless still, IB and PL CE are under the standard limits reinforcing the filter design. In this case, the current level was assumed to have a minor impact on CE, an acceptable hypothesis for frequencies under 20 MHz [17].

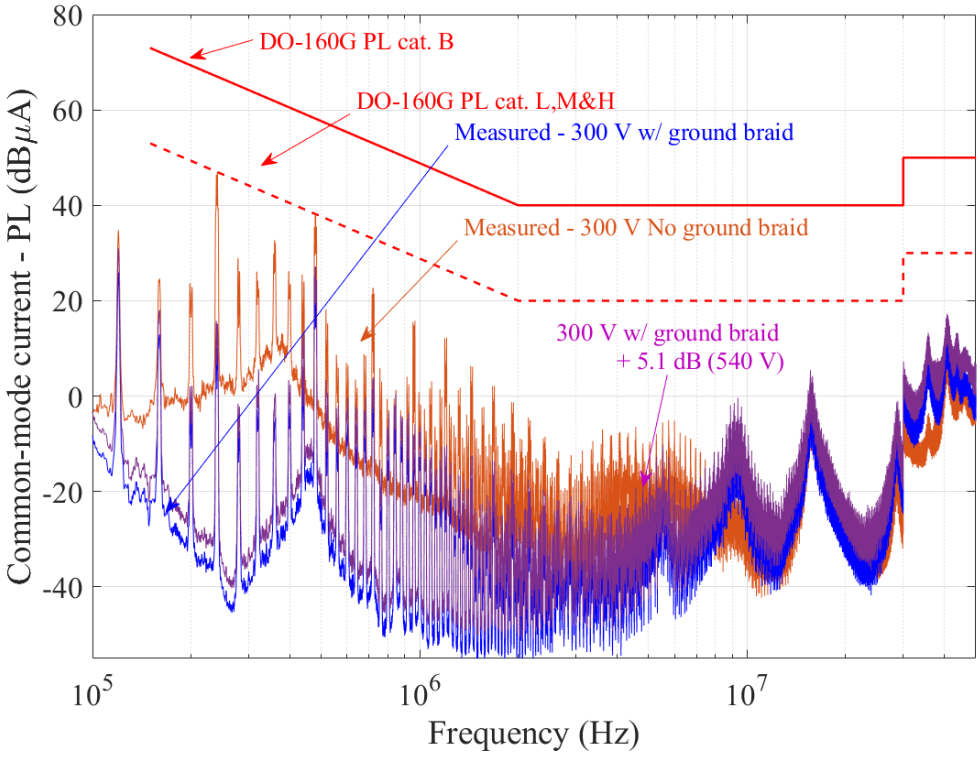


Figure 238 - Power Lines – Input. Impact of ground plane connection on Conducted Emissions.

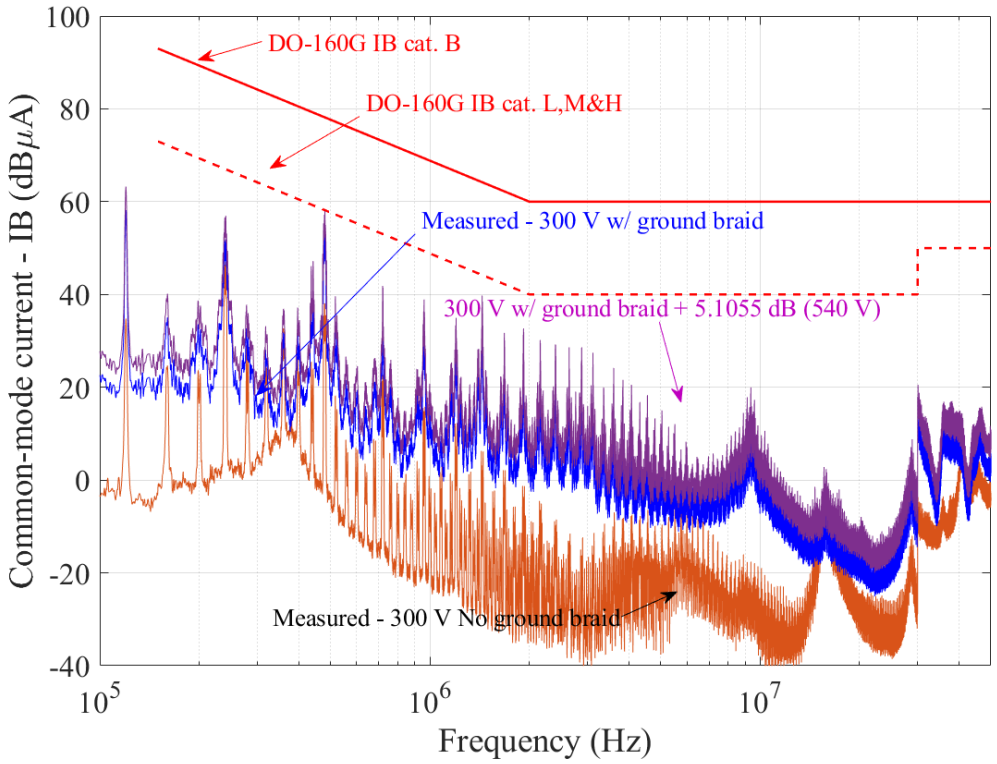
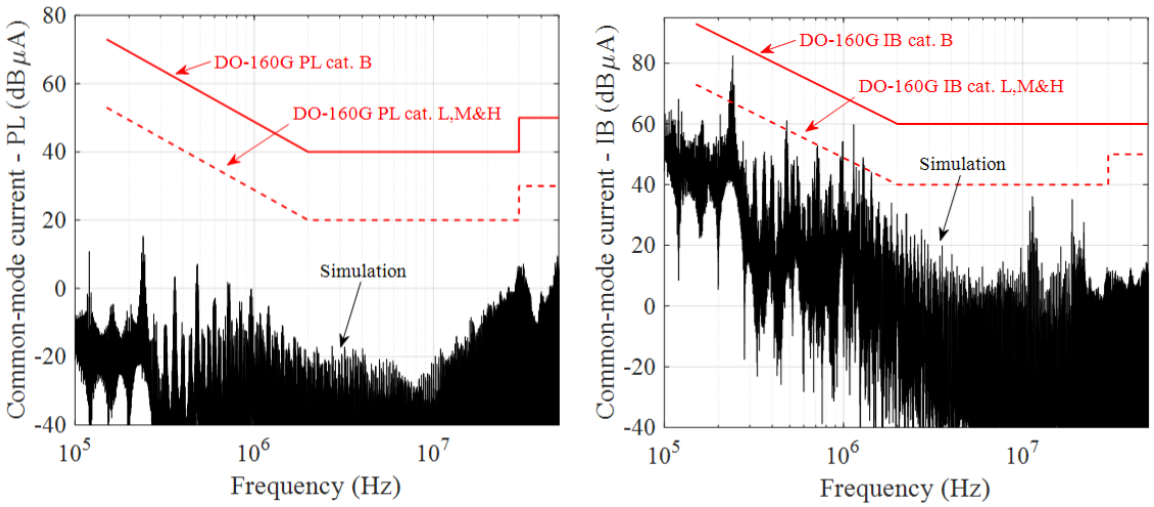


Figure 239 - Interc. Bunddles – Output. Impact of ground plane connection on Conducted Emissions.

Additionally, the proposed model considered a connection between heat sinks and C_Y capacitors to the standard ground plane. The orange curves presented in Figure 238 and Figure 239 presents CE for the same conditions of the blue curves, except for the ground braid connection to the ground plane. Removing the inverter ground connection shows a considerable increase (around 32 dB at 240 kHz and 18 dB at 720 kHz) on PL, especially until 4 MHz.

On the other hand, IB CE is considerably attenuated until around 10 MHz. The increase in PL and the attenuation in IB CE are due to suppressing the low impedance path provided by $C_{Y\text{-}In}$. Therefore, CM output current will return through LISN and input cables impedances, increasing input CM current (PL CE) even though CM output current is attenuated due to impedance path increase. That said, ground plane connection characteristics significantly impact CM filter design and should be carefully considered in EMI modeling.

Finally, considering the measured impedances of the CE test setup as the motor CM impedance in the EMI model proposed in Chapter 3, Figure 240 shows the simulated PL and IB CE for nominal inverter operation (540 V, DPWM 3, f_{lf} = 240 Hz, f_{sw} = 40 kHz and m_a = 0.94).



(a) Power Lines – Input *(b) Interc. Bunddles - Output*

Figure 240 - Conducted Emissions – 10-m long output cable and motor impedance for the inverter operating point (540 V, DPWM 3 and m_a = 0.94).

PL CE limits are largely satisfied while IB exceeds cat. L, M & H limits, especially at 240 kHz (12 dB) and 1.13 MHz (15 dB). On the other hand, these peaks shall be attenuated in the measurements as verified comparing the measurement and model in Figure 237 where 18 dB attenuation is verified at 240 kHz and 16 dB at 1.13 MHz. Therefore, the CM filter design using the EMI model for multilevel converters is considered satisfactory until 50 MHz.

5.3 Chapter Conclusions

This chapter presented the design and experimental verification of the 7–level inverter proposed in Chapter 4. The prototype presented around 14 liters and 10.04 kg, as shown in Figure 188 . The inverter presented 8.35 kg without the metallic base of the inverter and the Control board (parts not considered during the optimization in Chapter 2 and Chapter 4). The measured weight is less than 4% higher considering the solution proposed in Figure 187 (a). A traditional 2-level converter using 1200 V SiC Mosfet for the same operating conditions shall be 74% heavier than the 7-level inverter, with a power density 43.4% smaller than the multilevel topology.

Section 5.1.1 presented the design of a three-level flying capacitor leg with four GaNs in parallel, which composes the final inverter. Two solutions (Horizontal and Vertical) were evaluated by simulation according to the power loop inductance reduction and layer symmetry. The key to reducing power loop inductances in flying capacitor topologies with paralleled GaN devices is to split ceramic capacitors C_{FC} and consider a portion close to capacitors of the outter switching cell (close to C_{DM} in the case of a three-level topology). This technique reduced power loop inductance by around 41%. Both solutions present the same gate circuit design and the same gate loop (around 2.5 nH). The Horizontal version presents lower loop inductances values (4.4 nH/3.6 nH) but 8 layers and asymmetry between top and bottom paralleled devices. The main advantage of this solution is the possibility to easily cascade FC cells in series. At the same time, the proximity of the signal and power tracks goes against PCB good design practices. On the other hand, the Vertical version comprises 6 layers and a symmetrical arrangement of the components that compromises loop inductance (6.4 nH/5.7 nH). This solution allows the separation between signal and power tracks, reaching an utterly symmetrical circuit between the top and bottom devices and layers disposition. For these reasons, the Vertical version was selected to be built and experimentally evaluated.

Power loop inductances were measured using an impedance analyzer, and a maximum error compared to the simulation of 11% was verified for the internal loop and 6% for the external loop. Regarding electrical characterization, the Vertical solution was evaluated as a dc-dc buck converter and a single-phase inverter for V_{bus} = 540 V and output current from 7A until 53A. Calculated and measured losses (at 40 kHz) presented an excellent matching with an error of 5.9% for the dc-dc buck test (at 51 A) and 3% for the single-phase inverter test (at 42 A_{rms}, which is close to the inverter operation point). The impact of not considering connections, PCB, and the other resistive paths on loss calculation could underestimate the leg losses up to 20%. Regarding the efficiency, the FC leg reached almost 99.2% at 38 A (dc-dc buck test) and 98.8% in the single-phase test for the final inverter operation point (42 A_{rms}), both at 40 kHz. At this last, the parcel not related to the semiconductors represented 36% of total losses. The final version of the FC leg was proposed to be used in the inverter prototype. In this new version, signal connections were placed above the leg to connect with the Control board, and screwed metallic connectors (Wurth 74622104) were used for power connections, intending to reduce connector wear of placing and removing the FC leg and guaranteeing good electrical contact.

Section 5.2.1 presented the experimental verification of the 7-level inverter properly functioning, which reached 98.6% efficiency at 24.6 kVA (f_{lf} = 240 Hz, f_{sw} = 40 kHz and m_a = 0.76). Due to circulating currents between paralleled legs, extra losses are added to the inverter as well as flying capacitor voltage unbalance at high current. It compromises inverter safe operation, which

limited the maximum operating point to 500 V/38 kVA/87 A (70 kVA/130 A nominal operation) with open-loop control.

Finally, Section 5.2.2 presented Conducted Emissions measurements according to the RTCA/DO-160-G, intending to validate the EMI equivalent circuit for multilevel converters proposed in Chapter 3 to design CM filters. According to CE measurements, the proposed model of two equivalent voltage sources presents a good correspondence until 5 to 6 MHz for PL and IB. It was also shown that ground plane connection characteristics significantly impact CM filter design and should be carefully considered in EMI modeling. The 7-level inverter largely satisfies PL CE limits while IB exceeds cat. L, M & H limits, especially at 240 kHz (12 dB) and 1.13 MHz (15 dB). This evaluation was made considering the EMI equivalent circuit proposed in Chapter 3 at the nominal operating point and measured impedances (cables, LISN, and motor). These peaks that pass IB limits shall be attenuated in real measurements as verified comparing the measurement and model in Figure 237 , where 18 dB attenuation is verified at 240 kHz and 16 dB at 1.13 MHz. Therefore, the CM filter design using the EMI model for multilevel converters is considered satisfactory until 50 MHz.

CONCLUSIONS AND PERSPECTIVES

5.4 General Conclusions

Electrification of transportation is a challenging reality that has taken over the scene over the years. The socio-environmental impact of burning fossil fuels and their future scarcity guided sustainable and versatile energy consumption development efforts. The aerospace domain has set ambitious goals regarding gas emissions limitation, leading to new concepts and system architectures in several sectors. The replacement of heavy systems, such as mechanical, pneumatic, and hydraulic systems, reduces aircraft weight and fuel consumption with their electrical equivalents. Several projects have emerged in the last decades aiming to replace these systems using new technologies. The EPowerdrive project is a French project that aims to identify and study new topologies of power converters, semiconductors, and electrical machines in MEA. This thesis was part of the EPowerdrive project with the SATIE Laboratory, whose main objective was to design a DC – AC converter (filters included) with gravimetric power density superior to 8 kW/kg and higher efficiency than 98.5% for a 70 kVA MEA power drive system.

Different design blocks to evaluate the impact of multilevel inverter topologies and semiconductor technologies on the weight and overall performance of a 70 kVA inverter that meets the future's MEA requirements were presented in Chapter 2. WBG semiconductors are the key to increase the efficiency of power inverters to levels above 99%. A traditional inverter with 1200 V IGBT at 10 kHz has reached 97.8%, while 99.4% was achieved with a 1200 V SiC module (inverter without filters). Multilevel topologies directly impact increasing inverter power density from 3.63 kW/kg to 4.21 kW/kg at 10 kHz for 2-level and 7-level topologies, respectively. By passing to 70 kHz, this increase is even higher. It passes from 9 kW/kg to 12.36 kW/kg, showing that if the most important criteria are the power density, there is a considerable gain with the use of multilevel topologies, especially with the increase of switching frequency. The higher power density presented by the 7-level FC topology (composed by three paralleled legs of 3-level FC topology per phase with 4 GaNs in parallel per switch), added to different challenges listed below, justified the choice of this topology as the object of study of this thesis:

- The parallel of GaN transistors;
- Lack of work related to multilevel GaN switching cells with parallel transistors;
- Issues of integration of WBG transistors in a power inverter;
- The degrees of freedom in control due to the number of legs in parallel, which can allow a reconfiguration to operate in degraded mode;
- Lack of work on modeling of EMI for multilevel converters and filters design for these applications.

An equivalent CM circuit for multilevel inverter topologies considering the coupling between inverter input and output CM currents for a more precise EMI filter design was proposed in Chapter 3. This model was applied to the 7 – level topology proposed in Chapter 2 and presented an 85% (276 g) increase in filter weight (input + output), comparing to the uncoupled model used in Chapter 2. It reinforced the importance of a precise model to design EMI filters for multilevel converters.

Additionally, a parametric study of CM filter topology and repartition showed that the lightest solution was one CM choke on inverter input and another CM choke on inverter output and split C_Y between input and the output filters. It allowed a significant weight reduction of 66.7% (1.2 kg) compared to the traditional filter topology with only C_Y placed in the input filter (no C_Y in the output filter).

Different PWM techniques to increase overall power density and efficiency inverter were evaluated in Chapter 4. One methodology to find the optimal common-mode offset (CMO) was described to reduce flying capacitors and output inductor weight. These techniques were named FCPWM and ILPWM and guaranteed the minimum flying capacitor voltage ripple and output inductors peak current compared to PWM techniques for different modulation index and power factors. The applied methodology was used to reduce flying capacitor voltage ripple and inductors weight based on its current peak value. FCPWM reduced 18.4% flying capacitors weight for the present application, while ILPWM reduced 11.8% of the output inductors weight, both compared to the SPWM at 40 kHz. No other works were found in the literature regarding these topics, except the one proposing this methodology to reduce the magnetic flux of coupled inductors. The improvement on the models presented in Chapter 4 led to an increase of 22% on inverter weight going from 6.06 kg (10.6 kW/kg) with DPWM1 to 8.06 kg (8.7 kW/kg) for the DPWM 4 technique, which presented the highest power density at 40 kHz.

Finally, Chapter 5 presented the design and experimental verification of the 7–level inverter proposed in Chapter 4. The prototype presented around 14 liters and 10.04 kg. The inverter presented 8.35 kg without the metallic base and the Control board (parts not considered during the optimization in Chapter 2 and Chapter 4). The measured weight is less than 4% higher than the solution proposed in Chapter 4, which corroborates the precision of the models used in the optimization procedure in this thesis. A traditional 2-level converter using 1200 V for the same operating conditions shall be 74% heavier than the 7-level inverter, with a power density 43.4% smaller than the multilevel topology. The design of a three-level flying capacitor leg with 4 GaNs in parallel per switch was extensively explored, and the solution reached almost 99.2% of measured efficiency, at 38 A (DC-DC buck test) and 98.8% in the single-phase inverter test for the final inverter operation point (42 A), both at 40 kHz. The experimental verification of the entire converter led to 98.6% efficiency at 24.6 kVA (f_{lf} = 240 Hz, f_{sw} = 40 kHz and m_a = 0.76). Due to circulating currents between paralleled legs, inverter safe operation was limited to 500 V /38 kVA /87 A (70 kVA /130 A nominal operation) with open-loop control. The second part of experimental verification has shown that the EMI equivalent circuit for multilevel topologies proposed in Chapter 2 had a good matching until 5 to 6 MHz for PL and IB according to CE measurements, which indicates a good CM filter predictive design.

5.5 Perspectives

Different perspectives were identified during the research project which could contribute to the predictive design of power converters, as well as to increase converter efficiency and power density as presented in the topics below:

1. Semiconductors
    - Different semiconductors were launched in the market during the design of the 3-level FC leg of Chapter 5, as the 650 V/6.7 mΩ UF3SC065007K4S (SiC in TO-247 package) and 650 V/10 mΩ GS-065-150-1-D (GaN). Using these devices may facilitate the

integration and reduce the number of devices in parallel for the same losses (36x UF3SC065007K4S and 72x GS-065-150-1-D are needed for the entire inverter, instead of 144x GS66516T). Therefore, the advance of new technologies of WBG transistors can simplify the design further increase the power density of the presented inverter.

2. PCB Embedding Technology

- The cooling system and the reduction of power loop stray inductances were evaluated in Chapter 5, and make up a limiting factor for solutions with thin devices and a large number of those in parallel. Embedding semiconductors inside the PCB has been a promising technology to reduce power loops and increase thermal performance. The research performed in IRT Saint Exupery (Figure 241) showed that embedding packaged GaNs can lead to 20% reduction of thermal resistance compared to devices placed in the PCB top layer. This reduction goes up to 40% using the bare die instead of packaged devices. It is an interesting solution to increase power density for the present application, especially if the number of devices in parallel is reduced and the semiconductors are available in bare die, as the GS-065-150-1-D.

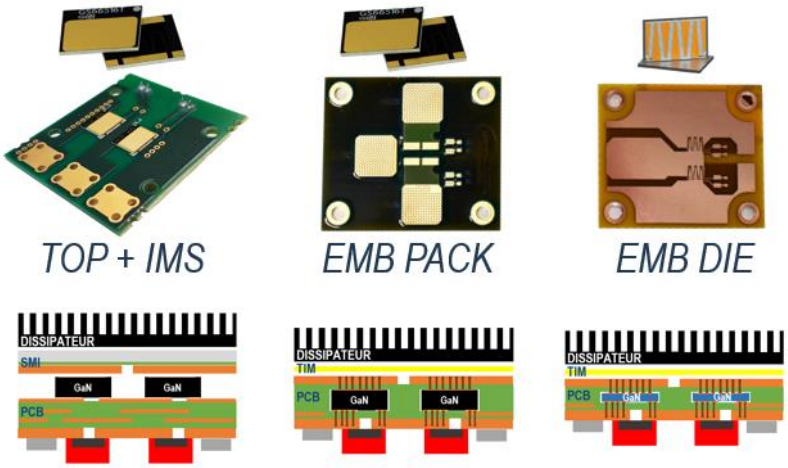


Figure 241 - Different PCBs with GS66516T packaged and in bare die embedded the PCB.

3. Overvoltage prediction

- The model to estimate overvoltage on motor terminals presented in this thesis considers the solution of transfer functions on the frequency domain, which facilitates the integration of the model in an optimization routine. This method was presented for a two-wire equivalent circuit using transmission line theory. This thesis proposed an equivalent two-wire circuit of a three-phase cable to get a more precise estimation of overvoltage in motor terminals using the transmission line theory. Despite giving a reasonable estimation of overvoltage (error lower than 5%) and the experimental validation, this model is limited to a three-phase unshielded cable. Therefore, a more generic model should be developed to consider unshielded cables and *n* conductors. Additionally, this model must be to be inversed and represent the time-domain voltage waveform on the *n*-phase load terminals.

4. EMI modeling and Filter Design
    - Chapter 3 presented a generic CM equivalent circuit that can be used on multilevel series and parallel topologies. This methodology was experimentally verified for a 2-level inverter with a satisfactory response until 20 MHz and a 7-level inverter based on FC topology with a satisfactory response from 500kHz to 6 MHz. Besides the presented tests, it would be necessary to measure the CM currents in the time domain and compare them with the proposed model to reinforce its validity. As presented in the experimental verification in Chapter 5, ground plane connection significantly impacts CM currents. Therefore, the imperfections of this connection (represented by parasitic resistances and inductances, for example) shall be considered in the equivalent CM circuit for a more precise estimation of CM currents. Additionally, the stray elements of DM input and output filters can be added to the CM proposed model to predict CE better, as the leakage inductance of CM chokes shall be considered on DM filter design. As presented in , input CM currents largelly satisfy CE limits, while output CM currents are very close to the standart limits. It suggests that input CM filter shall be over designed. Therefore, CM filter repartition should be explored in more detail to reduce CM filter weight and volume.

    - Core loss estimation was based on the i2GSE method, which has been used in different works, especially for DM inductors. Nevertheless, the loss estimation in CM chokes using nanocrystalline materials does not have a well-defined model that uses datasheet information. Losses are typically estimated using experimental characterization. That makes the predictive design of CM chokes difficult with a reasonable loss estimation, especially for the output filter that is constantly submitted to voltage variation. So, this is an open subject that may have a considerable impact on inverter optimization.

5. Inverter Control
    - The methodology presented in Chapter 4 to find the optimal PWM technique was validated experimentally regarding flying capacitor voltage ripple. Nevertheless, this methodology was explored to optimize one device at a time (flying capacitor voltage ripple or output inductor peak current). Due to the complexity of designing power converters with different constraints and the coupling among different systems (filters, cooling system, semiconductor losses, etc.), it would be worth evaluating the methodology with coupled problems. Such as reducing overvoltage in motor terminals and conducted emissions, evaluating the impact of inverter losses and passive devices weight or volume.

    - The inverter operating power was limited during the experimental evaluation in Chapter 5 because of the circulating currents between paralleled legs and the additional losses that could not be monitored in real-time. Therefore, to increase the inverter operating power, it is necessary to implement a closed-loop control to limit circulating currents and flying capacitor voltage unbalance since the increase of impedance (inductance value) between paralleled legs will drastically increase inverter weight. However, it is necessary to evaluate the DSP or other platform capable of generating the PWM signals and input ports necessary for all measurements.

5.6 Published Papers

Published papers

H. H. Sathler, L. Nagano, B. Cougo, F. Costa and D. Labrousse, "Impact of multilevel converters on EMC filter weight of a 70 kVA power drive system for More Electrical Aircraft," CIPS 2020; 11th International Conference on Integrated Power Electronics Systems, 2020, pp. 1-8.

H. H. Sathler, B. Cougo, J. -P. Carayon, F. Costa and D. Labrousse, "Modeling of Common-Mode Voltage Source for Multilevel Inverter Topologies," 2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE, 2020, pp. 1-3, doi: 10.1109/EMCEUROPE48519.2020.9245681.

B. Cougo, H. H. Sathler, R. Riva, V. D. Santos, N. Roux and B. Sareni, "Characterization of Low-Inductance SiC Module With Integrated Capacitors for Aircraft Applications Requiring Low Losses and Low EMI Issues," in IEEE Transactions on Power Electronics, vol. 36, no. 7, pp. 8230-8242, July 2021, doi: 10.1109/TPEL.2020.3014529.

H. H. Sathler; T. Zhao, F. Costa, B. Cougo, G. Segond, R. Burgos and D. Labrousse, "Design of three-level flying-capacitor commutation cells with four paralleled 650 V/60 A GaN HEMTs," 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), 2021, pp. 2277-2284, doi: 10.1109/APEC42165.2021.9487160.

H. H. Sathler H. H. Sathler, C. Mendes, B. Cougo, F. Costa, D. Labrousse and M. Stopa, “Impact of PWM Techniques in Efficiency and Power Density of a 70kVA Multilevel Inverter for More Electric Aircrafts,” 23rd European Conference on Power Electronics and Applications (EPE 2021 ECCE Europe), 2021.

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APPENDIX A

Inverter topologies analytical equations.

5.6.1.1 Two-Level Topology Modelling

A 2- level inverter input current (I_{bus}) is a piece of the essential information necessary to design the input DM filter. It can be calculated from the output current of each phase (*U, V, W*), referring to Figure 17, that pass through the switches connected to the positive bus (s_1,s_2,s_3), as:

$$I_{bus} = s_1 * I_{ph-U} + s_2 * I_{ph-V} + s_3 * I_{ph-W} .$$

On the other hand, the switch current waveform in s_1 is defined by:

$$I_{s1} = s_1 * I_{ph} \ .$$

Moreover, the phase leg output voltage is calculated based on the switch that is connected to the positive bus, as:

$$V_{ph-ref} = s_1 * V_{dc}$$

5.6.1.2 Flying Capacitor Topology Modelling

Flying capacitor in FC topology will handle the output current I_{ph} depending on the top switches connected to these capacitors (referred to Figure 18). The current that passes through each capacitor, $I_{C(k)}$, is essential information to design the flying capacitors. Therefore, $I_{C(k)}$ is determined by:

$$I_{C(k)} = (s_{(k+1)} - s_{(k)}) * \left(I_{ph}\right).$$

To design the flying capacitors, it is also essential to know the mean voltage applied to the device (capacitor), which is related to the top switch number *k*, input voltage V_{dc} and *q*:

$$v_{C(k)} = \frac{k * V_{dc}}{q-1}.$$

Like the two-level topology, the switch current waveform depends only on the output current I_{ph} and the switch state:

$$I_{s(n)} = I_{s(k)} = s_{(n)} * I_{ph},$$

while the output phase output voltage is given as an equivalent of the sum of the bus voltage and the floating capacitor voltages:

$$V_{ph-ref} = s_k * V_{dc} + \sum_{n=1}^{k-1} \left((s_{(n)} - s_{(n+1)} \right) * V_{C(n)}.$$

For a "q" level FC three-phase inverter, the input current of the inverter can be calculated similarly to the 2-level three-phase inverter, as the sum of each phase (U, V, W) current multiplied by the switch state of $s_{k\text{-}phase}$ connected to the positive bus, as:

$$I_{bus} = s_{k-U} * I_{ph-U} + s_{k-V} * I_{ph-V} + s_{k-W} * I_{ph-W}.$$

5.6.1.3 Neutral Point Clamped Topology Modelling

In this analysis, intending to generalize the equations for q-level NPC topology, the top switches of a generic NPC converter are presented in Figure 242. For the NPC topology, a new term for the input current (I_{DM}) is necessary since, in that case, I_{bus} does not comprehend all the current drained from V_{dc}. In that case, I_{DM} should be considered to design a DM input filter.

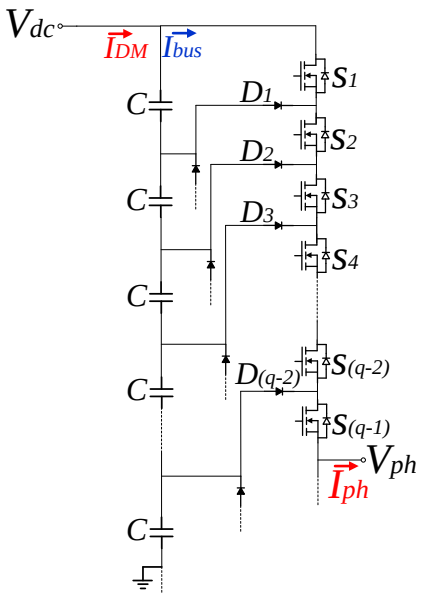

Figure 242 - Monophase q-level NPC top devices

Diodes currents are a crucial parameter to select this semiconductor, and the states of the two switches can describe that it is connected to (Example: the states of s_1 and s_2 give I_{D1}):

$$I_{d(k-1)} = s_{(k)} * not\left(s_{(k-1)}\right) * I_{ph} * sign\left(I_{ph}\right),$$

where k is the switch number and:

$$sign(I_{ph}) = 1,\ I_{ph} > 0 \text{ or } sign(I_{ph}) = 0,\ I_{ph} \le 0\ .$$

On the other hand, since losses on the top switches are different between them, it is necessary to consider each switch's current waveform. It is represented by $I_{s(k)}$, as:

$$I_{s(k)} = s_{(k)} * I_{ph}\ ,\ \ if\ k = 1;$$

$$I_{s(k)} = s_{(k)} * I_{ph} * sign\left(I_{ph}\right),\ \ if\ k > 1;$$

One exception to the equations above is identified for s_2 of the 3-level topology. It happens because s_2 is connected to inverter output, and the previous switch (s_1) is directly connected to the positive bus. Therefore, $I_{s(2)}$ is calculated as follows:

$$I_{s(2)} = (s_{(2)} * I_{ph} * sign\left(I_{ph}\right) \| (s_{(1)} * I_{ph} * not\left(sign\left(I_{ph}\right)\right))$$

The number of bus capacitors is directly proportional to (q-1), where it is subjected to a voltage V_C calculated according to:

$$V_C = \frac{V_{dc}}{q-1}.$$

The output voltage $V_{ph\text{-}ref}$ depends on all top switches states and the capacitor voltage V_C:

$$V_{ph-ref} = V_C * \left(\sum_{k=1}^{q-1} s_{(k)} \right).$$

Finally, inverter input current $I_{DM\text{-}in}$ is calculated according to:

$$I_{DM-in} = \frac{I_{ph}}{q-1} \left[\sum_{k=1}^{\left(\frac{q-1}{2}\right)} s_{(k)} - \sum_{k=\left(\frac{q+1}{2}\right)}^{q-1} \bar{s}_{(k)} \right].$$

The equations described above were identified regarding the input current for the 3,5, and 7-level topologies presented in Figure 243, Figure 244, and Figure 245.

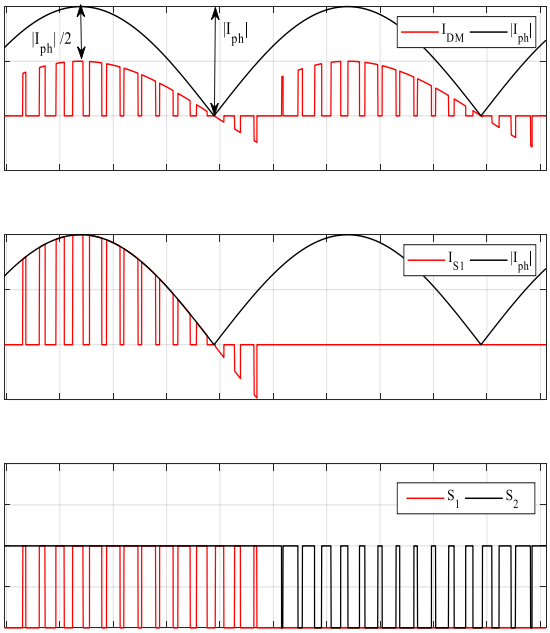

Figure 243 Single-phase 3Lvl NPC currents/switch states waveforms to estimate IDM, φ < 0

$I_{DM} = \frac{I_{S1}}{2} = s_1 \frac{I_{ph}}{2}$ During the first semi cycle and

$$I_{DM} = \frac{I_{S4}}{2} = -\bar{s}_2 \frac{I_{ph}}{2}$$ during the second semi cycle,

$$I_{DM,q=3} = \frac{I_{ph}}{2}\left(s_1 - \bar{s}_2\right)$$

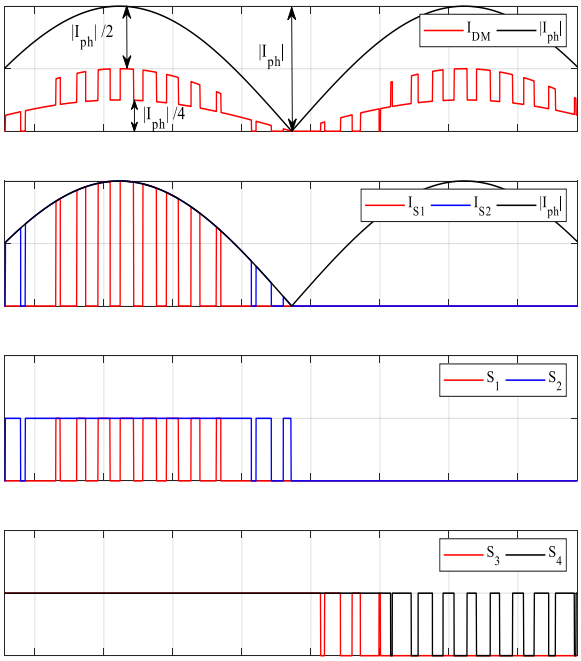

Figure 244 - Single-phase 5Lvl NPC currents/switch states waveforms to estimate IDM, φ < 0

$$I_{DM} = \frac{I_{S1}}{4} + \frac{I_{S2}}{4} = \left(s_1 + s_2\right)\frac{I_{ph}}{4}$$ During the first semi cycle and

$$I_{DM} = \frac{I_{S7}}{4} + \frac{I_{S8}}{4} = -(\bar{s}_3 + \bar{s}_4)\frac{I_{ph}}{4}$$ during the second cycle.

$$I_{DM,q=5} = \frac{I_{ph}}{4}\left[\left(s_1 + s_2\right) - (\bar{s}_3 + \bar{s}_4)\right].$$

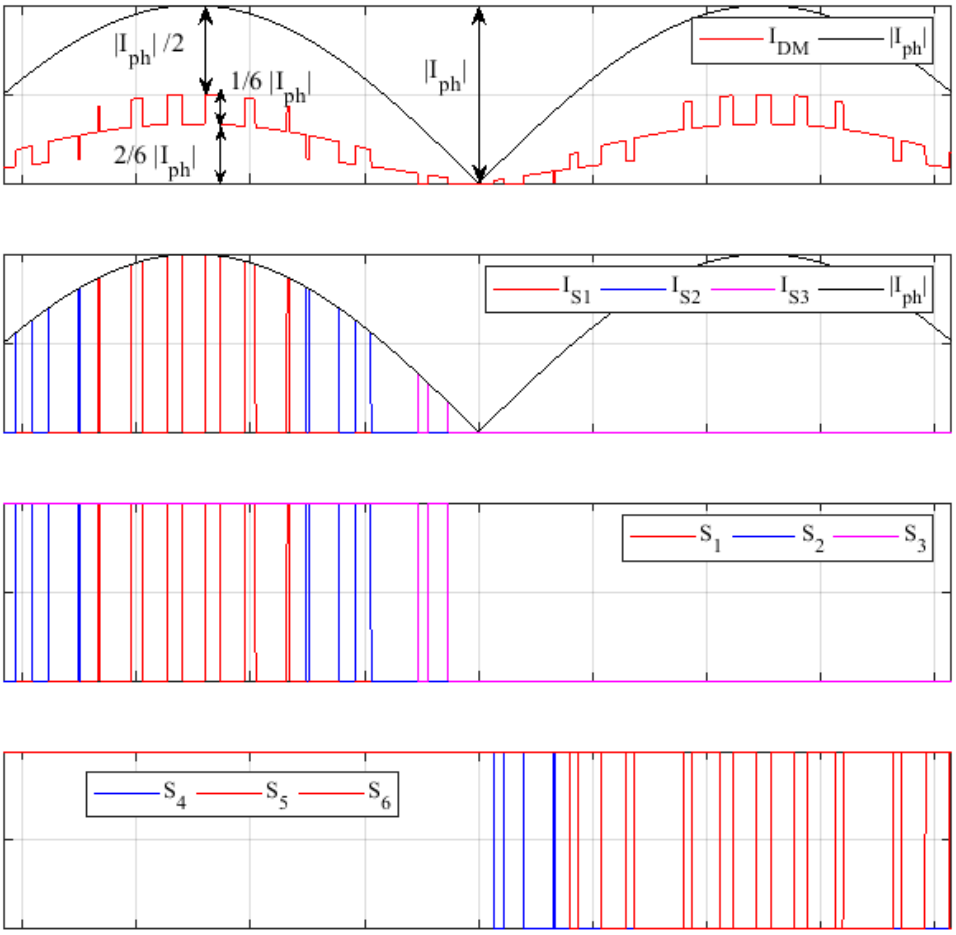

Figure 245 - Single phase 7Lvl NPC currents/switch states waveforms to estimate IDM, φ < 0

$I_{DM} = \frac{I_{S1}}{6} + \frac{I_{S2}}{6} + \frac{I_{S3}}{6} = (s_1 + s_2 + s_3)\frac{I_{ph}}{6}$, during the first semi cycle and

$I_{DM} = \frac{I_{S10}}{6} + \frac{I_{S11}}{6} + \frac{I_{S12}}{6} = -(\overline{s}_4 + \overline{s}_5 + \overline{s}_6)\frac{I_{ph}}{6}$ during the second semi cycle,

$$I_{DM,q=7} = \frac{I_{ph}}{6}\left[(s_1 + s_2 + s_3) - (\overline{s}_4 + \overline{s}_5 + \overline{s}_6)\right],$$

$$I_{DM} = \frac{I_{ph}}{q-1}\left[\sum_{k=1}^{\left(\frac{q-1}{2}\right)} s_{(k)} - \sum_{k=\left(\frac{q+1}{2}\right)}^{q-1} \overline{s}_{(k)}\right].$$

APPENDIX B

D_{max} calculation for *2 and 3* legs in parallel without uncoupled inductors.

The output voltage waveforms V_1 and V_2 for two paralleled legs (2-level topology) and the leg current ripple is shown inFigure 246. The greater ripple will occur for $D = 0.5$.

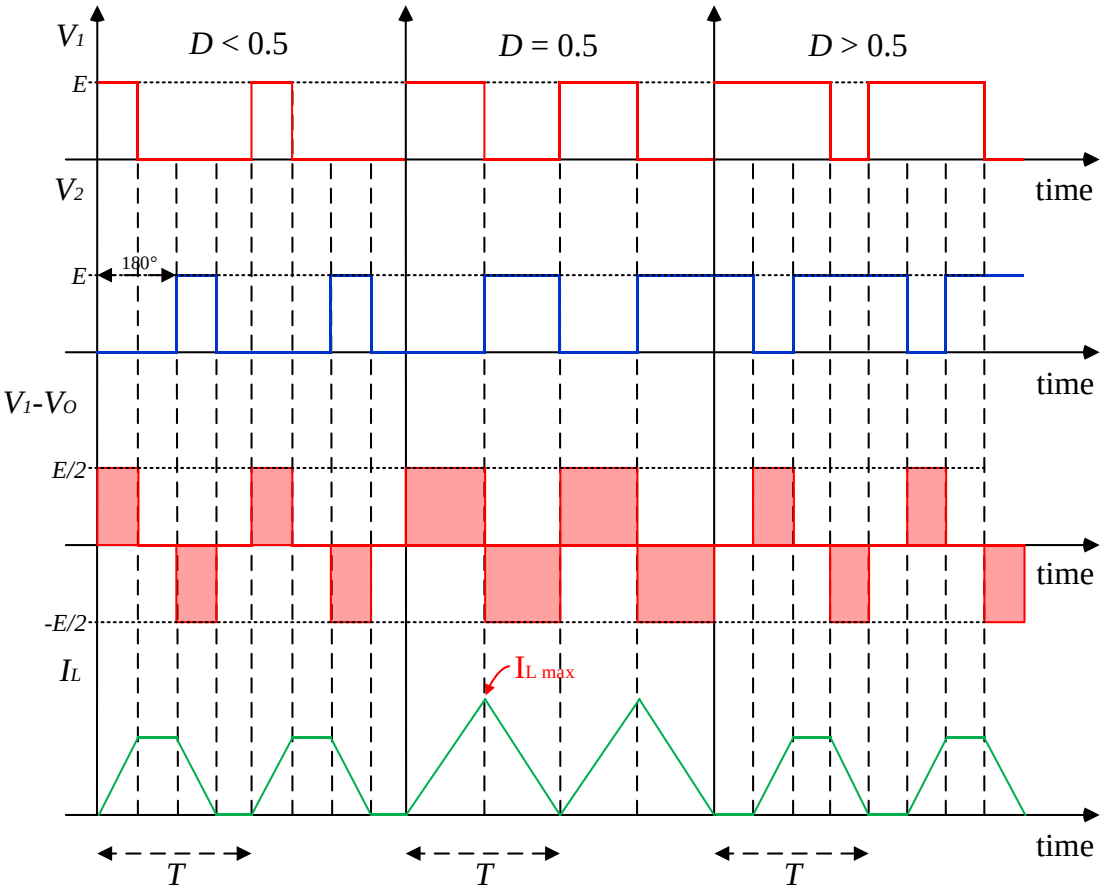

Figure 246 - Current ripple for two paralleled legs

While for three paralleled legs, it occurs for $D = 0.33$ as shown in Figure 247. Therefore, it is shown that D_{max} is inversely proportional to N_p.

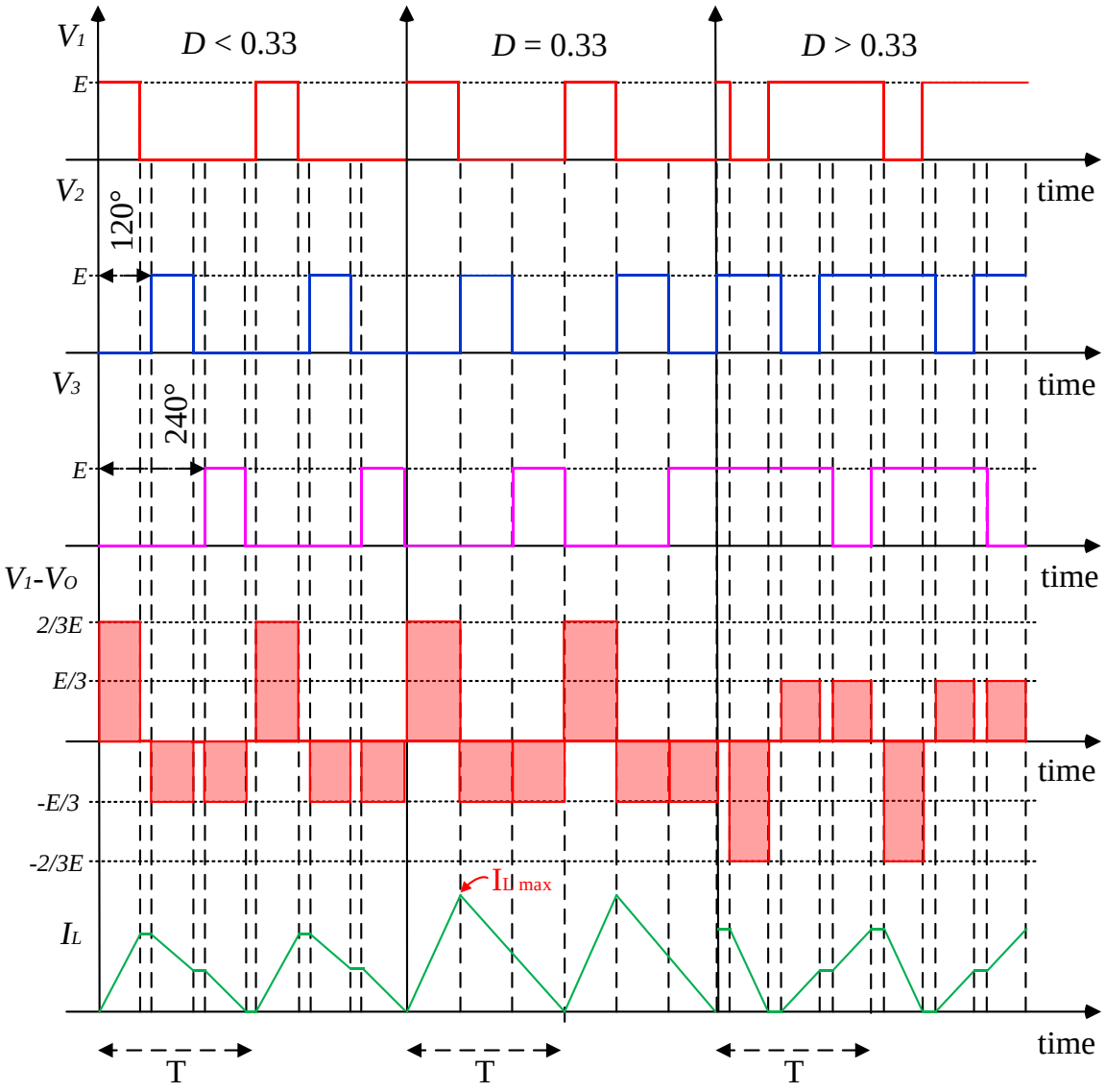

Figure 247 - Current ripple for three paralleled legs

APPENDIX C

Lightning current and CM capacitors

The electricity distribution on aircraft is composed of different voltage levels in different locations, as shown in Figure 248. In this example, four voltage levels make up the electrical installation on the aircraft: V_1 (Nose fuselage), V_2 (Cabin), V_3 (Wing), and V_4 (Tail cone). Lightning effects are critical phenomena that aircraft manufacturers consider, and it is well explained by [155]: "*When lightning strikes a metallic aircraft in flight, the Faraday cage effect protects systems mounted inside by conducting impulse current along the airframe outer skin to exit via wing or tail structures, according to Figure 249. Modern aircraft use significant amounts of composite material in the basic structure. This, combined with the increasing reliance on electronics, leads to problems not experienced in the past. Significantly higher disturbances are induced into the systems and many miles of cabling that carry both power supplies and data communication throughout an aircraft structure*".

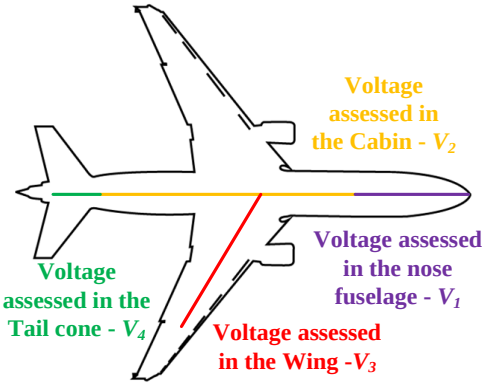

Figure 248 - Different voltage levels in an aircraft electrical installation

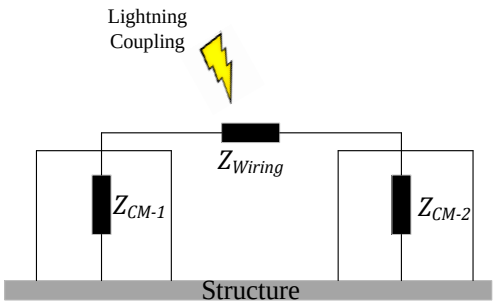

Figure 249 - Lightning coupling between two circuits referenced to the aircraft structure

This induced current I_{LH} is proportional to the impedance Z_{Loop} of the loop formed between the respective circuits of different installations and the aircraft structure according to:

$$I_{LH} = \frac{V_{LH}}{Z_{Loop} + Z_{Wiring}}.$$

VLH is the voltage across the load. The schematic shown in Figure 250 presents the coupling between a non-insulated load on the load connected to V_2 and another insulated load connected to V_3. In this case, the voltage loop V_{LH} is the sum of V_2 and V_3 according to Figure 251 in common-mode (it is also the same value for differential-mode).

The currents induced in this circuit can reach several hundred amps, making it necessary to use protection semiconductors with a high current gauge. These devices are expensive and very heavy since they have bulky cooling systems. To work around this problem, two solutions are commonly used:

1. The distribution circuit is made to two wires in exposed areas (Ex: Wing and landing gear circuits);
2. Insulation between load and enclosure that is connected to the aircraft structure.

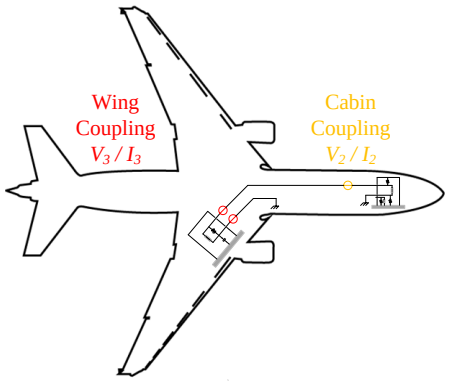

Figure 250 - Lightning coupling between Wing and Cabin circuit loads

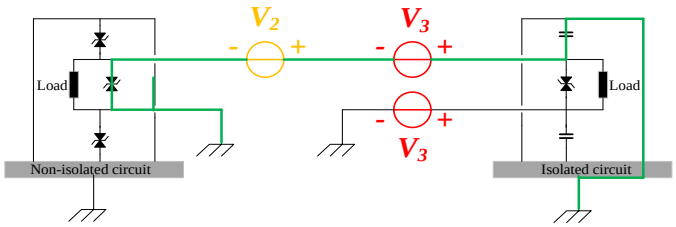

Figure 251 - Common-mode coupling between loads with different voltage levels

This insulation is responsible for limiting common mode current and must comply with the tests required by aircraft manufacturers (WF5A – DO 160G). Aircraft manufacturers sometimes require one impedance of 100Ω for a frequency of 10kHz to maintain lightning current below a specific value. Capacitors are commonly used to make this insulation roll and attend impedance criteria on calculators as presented in Figure 27 (Isolated circuit). By considering this protection circuit, an equivalent common-mode capacitor C_{CM} maximum value of 150nF is defined.

$$C_{CM} = \frac{1}{2\pi * 10kHz * 100\Omega} = 150nF$$

However, on power drive systems applications, cables are placed on the inverter's input and output, which means that the WF5A – DO 160 should be applied both at the input and output. It is also necessary to consider that the common mode filter impedance, usually composed of inductors and capacitors, will be seen by the lightning current. Figure 252 presents the common-mode circuit of a two-level inverter. Common mode capacitances are in some nF and inverters parasitic capacitances ($C_{Inv\text{-}In}$ and $C_{In\text{-}Out}$) some pF. Common mode inductances present a high impedance path, then lighting current path for the WF5A – DO 160 input and output test most preferable paths are presented in Figure 253 and Figure 254, respectively. Regarding the input, $C_{Y\text{-}In}$ can be increased to reduce $L_{CM\text{-}In}$ value and consequently entire filter weight. Nevertheless, $C_{Y\text{-}Out}$ will handle all lightning current, and its value should be limited regarding the desired current level for and specified frequency.

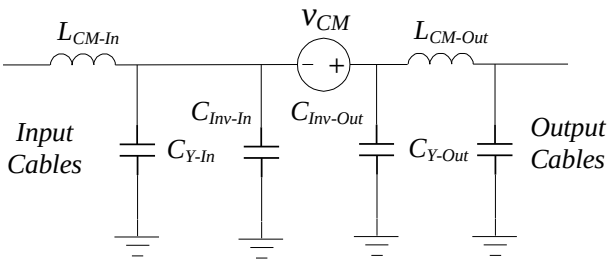

Figure 252 – Common mode circuit of a two-level inverter with both input and output CM filter.

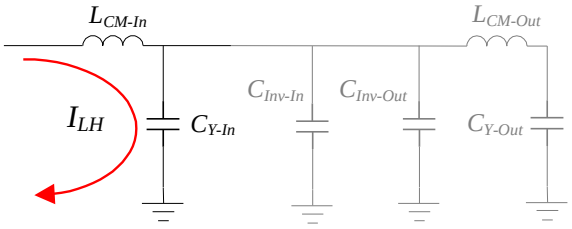

Figure 253 - Lightning current preferable path for WF5A – DO 160 input test. Inverter input.

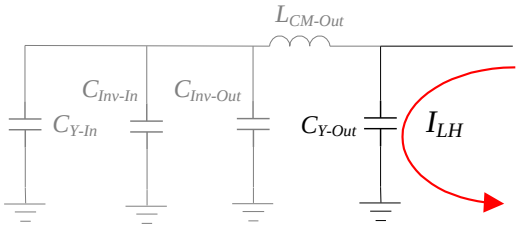

Figure 254 - Lightning current preferable path for WF5A – DO 160 input test - inverter output.

In this thesis, the EPowerdrive project's constraint was to fix a maximum common-mode capacitance of 150nF as an equivalent value for both input/output capacitors. As presented in Table 12, a database with 16 different part numbers of EMI suppression capacitors (MKP) Y2 class (line to ground interference suppression) from TDK® will be considered for CM filter optimization.

université PARIS-SACLAY
ÉCOLE DOCTORALE
Physique et ingénierie : Electrons, Photons, Sciences du vivant (EOBE)

Titre : Optimisation d'un Onduleur GaN Multiniveaux Série-Parallèle Triphasé pour des applications Aéronautiques

Mots clés : Optimisation, GaN, Onduleurs Multiniveaux, Comptabilité Electromagnétique, Applications Aéronautiques.

Résumé : L'électrification des moyens de transport est une réalité qui s'est imposée au fil des ans. L'impact socio-environnemental de l'usage de combustibles fossiles et son potentiel risque d'épuisement ont guidé les efforts de développement de la consommation d'énergie durable. Le domaine aérospatial s'est fixé des objectifs ambitieux en matière de limitation des émissions de gaz polluants, conduisant à de nouveaux concepts et architectures de systèmes dans plusieurs secteurs. Le remplacement des systèmes lourds, tels que les systèmes mécaniques, pneumatiques et hydrauliques avec leurs équivalents électriques réduit le poids et la consommation de carburant des avions. Plusieurs projets ont été conçus au cours des dernières décennies visant le remplacement de ces systèmes par de nouvelles technologies.

Ainsi, cette thèse présente une conception optimisée d'un convertisseur DC-AC (tous filtres inclus) avec une densité de puissance gravimétrique supérieure à 8 kW/kg et un rendement supérieur à 98,5% pour une chaine électromécanique de 70 kVA d'un avion plus électrique (MEA). Parmi les différentes topologies d'onduleurs et technologies de semi-conducteurs, un onduleur triphasé à 7 niveaux, composé de trois branches en parallèle d'une topologie à condensateurs flottants 3 niveaux par phase avec 4 HEMT GaN en parallèle par commutateur, a été sélectionné pour être construit. Le prototype présente environ 14 litres et 10 kg (il comprend des filtres, la structure métallique et une carte de commande).

Le poids mesuré est supérieur de moins de 4% à la solution proposée en simulation ce qui corrobore la précision des modèles utilisés dans la procédure d'optimisation. Un convertisseur traditionnel à 2 niveaux utilisant des composants actifs 1200 V pour les mêmes conditions de fonctionnement est 74% plus lourd que l'onduleur à 7 niveaux, avec une densité de puissance 43,4% inférieure à la topologie à plusieurs niveaux. Le bras d'onduleur (condensateurs flottants trois niveaux avec 4 GaN en parallèle par commutateur) a été largement exploré, et la solution a atteint près de 99,2% de rendement mesuré à 38 A / 5,8 kW à la sortie du convertisseur (test en configuration Buck DC-DC) et 98,8% dans le test en onduleur monophasé à 42 A / 6,6 kW, tous les deux à 40 kHz avec une charge RL (résistance + inductance). La vérification expérimentale de l'ensemble du convertisseur triphasé a conduit à un rendement de 98,6% à 24,6 kVA (f_{lf} = 240 Hz, f_{sw} = 40 kHz and M_i = 0,76). En raison des courants de circulation entre les bras en parallèle, le fonctionnement sûr de l'onduleur a été limité à 500 V/38 kVA/87 A (70 kVA/130 A condition nominale) avec contrôle en boucle ouverte. En ce qui concerne la modélisation EMI, cette thèse a proposé un modèle générique de circuit équivalent de convertisseur multiniveau avec une bonne correspondance jusqu'à 5 à 6 MHz (soutenu par des résultats expérimentaux) et certainement aidera la conception prédictive du filtre EMI.

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ÉCOLE DOCTORALE
Physique et ingénierie : Electrons, Photons, Sciences du vivant (EOBE)

Title : Optimization of GaN-based Series-Parallel Multilevel Three-Phase Inverter for Aircraft applications.

Keywords : Optimization, GaN, Mutilevel Inverters, Electromagnetic Compatibility and Aircraft applications.

Abstract : The electrification of means of transport is a challenging reality that has taken over the scene over the years. The socio-environmental impact of burning fossil fuels and their future scarcity guided sustainable and versatile efforts of energy consumption development. The aerospace domain has set ambitious goals regarding gas emissions limitation, leading to new concepts and system architectures in several sectors. The replacement of heavy systems, such as mechanical, pneumatic, and hydraulic systems, reduces aircraft weight and fuel consumption with their electrical equivalents. Several projects have emerged in the last decades aiming to replace these systems using new technologies.

This thesis presents an optimized design of a DC – AC converter (filters included) with gravimetric power density superior to 8 kW/kg and higher efficiency than 98.5% for a 70 kVA MEA power drive system. Among different inverter topologies and semiconductors technologies, a 7-level flying capacitor three-phase inverter, composed of three paralleled legs of 3-level flying capacitor topology per phase with 4 GaNs in parallel per switch, was chosen to be built. The prototype presented around 14 liters and 10.04 kg (it comprises filters, metallic structure, and control board).

The measured weight is less than 4% superior considering the solution proposed in simulation, which corroborates the precision of the models used in the optimization procedure. A traditional 2-level converter using 1200 V for the same operating conditions shall be 74% heavier than the 7-level inverter, with a power density 43.4% smaller than the multilevel topology. On three-level flying capacitor leg with 4 GaNs in parallel per switch was extensively explored, and the solution reached almost 99.2% of measured efficiency, for 38 A / 5.8 kW at the output of the converter (DC-DC Buck test) and 98.8% in the monophase inverter test (42 A / 6.6 kW at the output of the converter), both at 40 kHz with an RL load (resistor + inductor). The experimental verification of the entire converter led to 98.6% efficiency at 24.6 kVA (f_{lf} = 240 Hz, f_{sw} = 40 kHz and M_i = 0.76). Due to circulating currents between paralleled legs, inverter safe operation was limited to 500 V/38 kVA/87 A (70 kVA/130 A nominal operation) with open-loop control. Regarding EMI modeling, this thesis proposed a generic model for multilevel converter equivalent circuit with good correspondence until 5 to 6 MHz (supported by experimental results) and can assist predictive design of EMI filter.